Distributed and Scalable Uplink Processing for LIS: Algorithm, Architecture, and Design Trade-offs

Jesús Rodríguez Sánchez ⊙, Student Member, IEEE, Fredrik Rusek ⊙, Member, IEEE, Ove Edfors ⊙, Senior Member, IEEE, and Liang Liu ⊙, Member, IEEE

Abstract—The Large Intelligent Surface (LIS) is a promising technology in the areas of wireless communication, remote sensing and positioning. It consists of a continuous radiating surface located in the proximity of the users, with the capability to communicate by transmission and reception (replacing base stations). Despite of its potential, there are numerous challenges from implementation point of view, being the interconnection data-rate, computational complexity, and storage the most relevant ones. In order to address those challenges, hierarchical architectures with distributed processing techniques are envisioned to be relevant for this task, while ensuring scalability. In this work we perform algorithm-architecture co-design to propose two distributed interference cancellation algorithms, and a tree-based interconnection topology for uplink processing. We also analyze the performance, hardware requirements, and architecture trade-offs for a discrete LIS, in order to provide concrete case studies and guidelines for efficient implementation of LIS systems.

I. INTRODUCTION

LIS has been identified as one of the key technologies for beyond 5G [3]–[6]. In Fig. 1 we show the concept of a LIS serving multiple users simultaneously. The LIS is a continuous radiating surface located in the proximity of the users. Each part of the surface is capable of receiving and transmitting electromagnetic (EM) waves with a certain control, so the EM waves can be focused in 3D space with high resolution, opening the door of a new world of possibilities for power-efficient communication.

Apart from LIS, another type of intelligent surface has been studied in the literature, which can be classified within the smart radio environment paradigm [7], by which the wireless channel can be controlled to facilitate the transmission of information, as opposite to traditional wireless communication systems, where the channel is imposed by nature, and transmitter and receiver adapt to changes in it. One example of this new trend is the reconfigurable surfaces, known as intelligent reflecting surfaces, programmable metasurfaces, reconfigurable intelligent surfaces (RIS), and passive intelligent mirrors among others 1, which consist of electronically passive surfaces with the capability to control how the waves are reflected when hitting their surface. Furthermore, the term LIS has also been recently used for such a passive surfaces [10]–[12], with the subsequent risk of confusion. While RIS can be seen as part of the radio channel, LIS acts as an active basestation/access point. LIS contains full transmitters and receivers chains, together with baseband processing capabilities to transmit and receive. A list of the main differences between RIS and LIS is shown in Section II-B.

Most of the research on LIS has been focusing on concept exploration [3]–[6], system performance [13], [14], and channel modeling [15], [16]. However, the questions from implementation point of view have not yet been answered. This paper aims to cover this area, by identifying and addressing implementation challenges, and providing design guidelines for an efficient implementation of LIS.

The first step to make LIS implementable is to make it discrete (based on discrete antennas). It is known [3] that a continuous LIS can be replaced by a discrete one with no practical difference in achieved capacity. However, an efficient implementation of a discrete LIS is still very challenging, as it is expected to be made up of a very large number of antennas with the corresponding receiver (and transmitter) chains, which translates into a tremendous amount of interconnection data-rate, that needs to be routed to the Central Digital Signal Processor (CDSP) through the backplane network. This centralized approach has already been employed in the LuMaMi Massive MIMO testbed [17], with a need of 100 bidirectional links, and a total aggregated interconnection bandwidth of 5GB/s. In case of LIS this number is much higher. To illustrate, let’s assume a 1.2m × 1.2m array containing 1,024 antennas in the 4GHz band (assuming spacing of half wavelength), with the corresponding radio frequency (RF) and analog-to-digital converter (ADC) blocks. Then, if each ADC uses 12bits per I and Q, that makes a total rate of ~ 48Tb/s 1. This is 3 orders of magnitude higher than the massive MIMO counterpart [17], where this issue has been

1 Assuming 5G-NR standard, and sampling rate of 480,000 · 4,096 ∼ 2Gs/s.
previously addressed [18]–[21]. Therefore there is a need to come up with specific architectures and algorithms in order to overcome this bottleneck.

We propose to tackle those challenges by algorithm and architecture co-design. At the algorithm level, we explore the unique features of LIS (e.g., very large aperture) to develop distributed algorithms that enable the processing being performed locally, near the antennas. This will significantly relax the requirement for interconnection bandwidth. At the hardware architecture design level, we propose to panelize the LIS in order to facilitate processing distribution, scalability, manufacturing, and installation. A hierarchical interconnection topology is developed accordingly to provide efficient and flexible data processing, and data exchange between panels and CDSP. Based on the proposed algorithm-architecture, extensive analysis has been performed to enable trade-offs between system capacity, interconnection bandwidth, computational complexity, and processing latency. This will provide high-level design guidelines for the real implementation of LIS systems. The contributions of this work are originated from our previous work in [1], [2], [22], being considerably extended in the present paper.

This article is organized as follows: Section II introduces the LIS concept, then the system model is presented in Section III. Our proposed algorithms are described in Section IV, and the architecture description in Section V. Analysis and design trade-offs are presented in Section VI, and finally conclusions in Section VII.

Notation: In this paper, lowercase, bold lowercase and upper bold face letters stand for scalar, column vector and matrix, respectively. The operations $(\cdot)^T$, $(\cdot)^*$ and $(\cdot)^H$ denote transpose, conjugate and conjugate transpose respectively. $I_K$ represents the identity matrix of size $K \times K$. Operator diag$(\cdot)$ returns a block diagonal matrix built with the list of matrices in the argument.

II. LARGE INTELLIGENT SURFACES

This section describes the key features of LIS, by comparing with massive MIMO and RIS. We also present the general concept of panelized LIS, which is proposed to ensure scalability and implementation feasibility.

A. Differences with Massive MIMO

Multi-antenna technology has evolved in recent years in the form of Massive MIMO, where the number of antennas in the Base-Station (BS) grows up to $\sim 100$, bringing many benefits from communication and energy consumption points of view [23]. LIS wants to go further by increasing the number of antennas one or two orders of magnitude more, altogether with the physical size of the array, which brings gains beyond Massive MIMO can provide. This results in fundamental differences between these two technologies, which are listed as follows:

- Users are close to the LIS in relation to its size, what makes them being in the near field, as opposite to Massive MIMO (and others cellular access technologies) where users are in the (Fraunhofer) far field region. Being in the near field requires the use of channel models based on spherical waveforms, rather than the planar wave approximation, whose use is generalized in Massive MIMO (and other cellular technologies).
- Due to the lower path loss (due to the close proximity between users and LIS), and the large antenna gain, transmit power is expected to be relatively small for both sides of the communication, opening the door for extensive use of low-cost and low-power analog components.
- Received power distribution from users is not uniform throughout the surface as illustrated in Fig. 1. The same user is received with different signal intensity from different parts of the LIS. This can be exploited by the use of localized digital signal processing, leading to a more efficient use of computational resources, and interconnection bandwidth, without significantly sacrificing the system performance. This is in contrast with Massive MIMO (and other cellular technologies), where users are seen with same power across the antenna array (which is in fact connected to the planar wave approximation).

B. Differences with RIS

As commented in the Introduction, LIS and RIS are fundamentally different technologies. In this section we summarize the main differences between these two:

- RIS acts as a programmable reflector between the radio access point and the users, forming part of the channel. Typically it is configured in a way to improve a certain quality metric, such as capacity. LIS acts as a radio access point capable to communicate directly to users.
- LIS contains full receivers (in contrast to most of RIS) and baseband processing capabilities to obtain CSI from pilots transmitted by users. This allows an accurate calculation of the corresponding equalization matrix, and further detection within LIS.

C. Panelized Implementation of LIS

Given that LIS is large in physical size and there is a need for distributed processing close to the antennas, we propose to divide the LIS in square units or panels. Panelization allows the LIS to adapt to a wide range of scenarios by adding, moving, or removing panels as desired, varying consequently the size and form of the LIS. Different shapes can be achieved by placing the panels in different ways: square, rectangular or distributed (panels not physically together, but covering a certain area). It also simplifies the system design, verification, and fabrication by only focusing on the panel as building block, instead of covering all possible LIS sizes and forms. Additionally, the installation becomes also simpler as the panel weights less, being easy to lift and mount.

A high level overview of the LIS architecture components, processing distribution, and interconnection is shown in Fig. 2. Panels are composed of a group of antennas forming a
Fig. 2: LIS architecture components in the form of a) panel, b) each with internal analog and digital processing resources, synchronization, and digital back-haul. Identical panels can be combined in arbitrary configurations, e.g., fully or partially connected. Each panel contributes with its own processing resources, making the available resources for distributed processing fixed per area unit.

squared array as shown in Fig. 2a. Each panel contains internal processing resources in the analog and digital domains, and inter-connection capabilities to connect the panel to other panels (Fig. 2b). As said before, panels provide freedom to assemble the LIS. As an example, Fig. 2c shows 16 panels fully connected, forming a 1024-antennas LIS, while in Fig. 2d, 6 physically distant panels are connected in a distributed fashion (e.g: covering a certain volume in space, such as an office, or theater).

III. SYSTEM MODEL

A conceptual view of a discrete LIS system is presented in Fig. 3. We consider $K$ users transmitting to the LIS, which is divided in three parts: front-end, backplane, and CDSP. We will use the term front-end to refer to the per-antenna processing which is performed locally at each panel, and backplane to the related processing involving data aggregation, distribution, and processing for further dimensionality reduction. Backplane can be made of multiple levels and processing nodes as we will present in Section V. The processing unit in the front-end is the Local DSP (LDSP), while the one in backplane is the Backplane DSP (BDSP). The data is finally collected by the CDSP for detection. In the present section we also introduce a mathematical model for the communication and the LIS-baseband processing.

We consider the transmission from $K$ single antenna users to the LIS containing $M$ active antenna elements (input dimensionality). The LIS is divided into $P$ squared panels, each with $M_p$ elements, such that $M_p \cdot P = M$. Each panel has an output with $N_p$ dimensions, and the total number of them is $N$, such that $N = N_p \cdot P$. Panels are connected to the backplane, which collects their output data, process it, and provides the CDSP with $K$ values to ensure proper detection. The data dimensionality is reduced from the antenna elements interface (vector $y \in \mathbb{C}^M$ in the figure) to the backplane input ($z \in \mathbb{C}^N$) due to front-end, and from this to the CDSP interface ($s \in \mathbb{C}^K$) due to backplane processing. We assume $M \gg K$ for the rest of the article.

The $M \times 1$ received vector at the LIS is given by

$$y = \sqrt{\rho} H x + n,$$

(1)

where $x$ is the transmitted $K \times 1$ user data vector, and $\mathbb{E}\{xx^H\} = I_K$. $H$ is the channel matrix, and $n \sim \mathcal{CN}(0, I)$ is a $M \times 1$ noise vector, that we assume with identity covariance for simplicity without loss of generality. This convention leaves $\rho$ as the "transmit" SNR and therefore it is dimensionless.

Assuming the location of user $k$ is $(x_k, y_k, z_k)$, where the LIS is at $z = 0$. The channel between this user and a LIS antenna at location $(x, y, 0)$ is given by the complex value [3]

$$h_k(x, y) = \frac{\sqrt{\pi}}{2 \sqrt{\pi \sigma^3_k}} \exp \left( -\frac{2\pi j d_k}{\lambda} \right),$$

(2)
where \( d_k = \sqrt{z_k^2 + (x_k-x)^2 + (y_k-y)^2} \) is the distance between the user and the antenna, and Line of Sight (LoS) propagation between them is assumed. \( \lambda \) is the wavelength. The channel matrix can be expressed as

\[
\mathbf{H} = [\mathbf{H}_1^T, \mathbf{H}_2^T, \cdots, \mathbf{H}_p^T]^T,
\]

where \( \mathbf{H}_i \) is the \( M_p \times K \) channel matrix of the \( i \)-th panel. We assume each panel has perfect knowledge of its local channel.

**A. Dimensionality reduction: A lossless or lossy process**

As commented previously, our LIS architecture can be seen as a system to reduce the dimensionality of the very large incoming signal \( (M \times 1) \) down to a value required for detection at the CDSP \( (K \times 1) \). We can classify this process attending to the criteria of preserving information as: lossless and lossy. A lossless process maintains the mutual information between CDSP input and user’s data, formally

\[
I(s; x) = I(y; x),
\]

so the system can achieve channel capacity performance if optimal processing is done in CDSP. Initial progress on the trade-offs of distributed processing for MIMO systems in lossless approach can be seen in [24], and more recently in [25]. In this regime \( N_p \geq \min\{M_p, K\} \).

In despite of the attractiveness of achieving optimal performance, lossless presents a high cost from implementation point of view, as it requires larger panel output dimensionality, which translates in higher interconnection bandwidth throughout the backplane. In this article we look for a good compromise between implementation cost and performance, which leads us to explore the case \( N_p \leq M_p \), and especially \( N_p \ll M_p \). By selecting this regime we expect to reduce significantly interconnection bandwidth at the cost of a loss in performance, which can be expressed formally as

\[
I(s; x) \leq I(y; x).
\]

Our approach is to include enough flexibility into the system to obtain enough working points to establish a rich trade between implementation cost and performance, which in fact, allows the system to adapt to a large variety of scenarios during the deployment phase. As we will see in Section VI, it is possible achieve close to channel capacity conditions with significant reduction in implementation cost.

1) Filtering: In order to achieve dimensionality reduction, we employ linear filtering in the incoming data, while to achieve enough flexibility we consider separate filters for front-end and backplane.

Let us consider the panelized architecture shown in Fig. 3, where each panel performs local per-antenna processing on the received signal and delivers the result to the backplane. There is not cooperation among panels during front-end filtering, therefore the filter matrix \( \mathbf{W}_p \) has the following structure

\[
\mathbf{W}_p = \text{diag}(\mathbf{W}_{p,1}, \mathbf{W}_{p,2}, \cdots, \mathbf{W}_{p,p})
\]

(4)

where \( \mathbf{W}_{p,i} \) is the \( M_p \times N_p \) matrix filter of the \( i \)-th panel.

Then the front-end output is given by

\[
\mathbf{z} = \mathbf{W}_p^H \mathbf{y} = \sqrt{\rho} \mathbf{W}_p^H \mathbf{H} \mathbf{x} + \mathbf{n},
\]

(5)

where \( \mathbf{n} = \mathbf{W}_p^H \mathbf{n} \) is the filtered noise. Mind that size of \( \mathbf{z} \) is \( N \), and \( N \leq M \) according to the reasoning in this section. Finally, the backplane filters \( \mathbf{z} \) in order to obtain \( \mathbf{s} \) as

\[
\mathbf{s} = \mathbf{W}_p^H \mathbf{z},
\]

(6)

which is used by CDSP for detection.

**B. Sum-Rate Capacity**

The mutual information between \( \mathbf{z} \) and \( \mathbf{x} \) is \( I(\mathbf{z}; \mathbf{x}) = I(H(\mathbf{z}) - H(\mathbf{z}|\mathbf{x})) \). Assuming white Gaussian signaling transmitted by users, the mutual information for a given \( \mathbf{H} \) and \( \mathbf{W}_p \) can be further expanded as

\[
\begin{align*}
I(\mathbf{z}; \mathbf{x}) &= \log_2 |\Sigma_{zz}| - \log_2 |\Sigma_{nn}| \\
&= \log_2 |\rho \mathbf{W}_p^H \mathbf{H} \mathbf{H}^H \mathbf{W}_p + \mathbf{W}_p^H \mathbf{W}_p| \\
&- \log_2 |\mathbf{W}_p^H \mathbf{W}_p|,
\end{align*}
\]

(7)

where \( \Sigma_{zz} \) and \( \Sigma_{nn} \) are the covariance of the multivariate complex gaussian vector \( \mathbf{z} \) and \( \mathbf{n} \) respectively. If \( \mathbf{W}_p \) is full-rank matrix, and taking into account that \( M \geq N \), then \( (\mathbf{W}_p^H \mathbf{W}_p)^{-1} \) exists and we can rewrite (7) as

\[
I(\mathbf{z}; \mathbf{x}) = \log_2 |\mathbf{I}_K + \rho \mathbf{H}^H \mathbf{W}_p (\mathbf{W}_p^H \mathbf{W}_p)^{-1} \mathbf{W}_p^H \mathbf{H}|.
\]

(8)

We are interested in maximize the sum-rate capacity for this front-end architecture, and it will be the maximum of (8) over all possible \( \mathbf{W}_p \) for a given \( \mathbf{H} \). If we take into account the block structure of \( \mathbf{H} \) and \( \mathbf{W}_p \) presented in (3) and (4) respectively, the sum-rate capacity at \( \mathbf{z} \) interface is given by

\[
C_z = \max_{\mathbf{W}_p} \log_2 |\mathbf{I}_K + \rho \sum_{i=1}^p \mathbf{H}_{p,i} \mathbf{W}_p,i (\mathbf{W}_p,i^H \mathbf{W}_p,i)^{-1} \mathbf{W}_p,i^H \mathbf{H}_{p,i}|,
\]

(9)

where \( \mathbf{Q}_i \) is a \( M_p \times N_p \) semi-unitary matrix, consisting of the \( N_p \)-first singular vectors of \( \mathbf{W}_p,i \). For the last expression in (9), it is assumed that all matrices \( \mathbf{W}_p,i \) are full-rank, so the inverse exists.

As we will show in next section, selection of \( \{\mathbf{W}_p,i\} \) is done in a way that each element is semi-unitary, which leads to white noise at the front-end output. Therefore, once the front-end filters are selected, they can be seen as part of the channel by the backplane, and we can apply same reasoning to obtain \( \mathbf{W}_B \), leading to

\[
C_z = \max_{\mathbf{W}_B} \log_2 |\mathbf{I}_K + \rho \mathbf{H}^H \mathbf{W}_B (\mathbf{W}_B^H \mathbf{W}_B)^{-1} \mathbf{W}_B^H \mathbf{H}|,
\]

(10)

A detailed explanation of this process can be found in Section V.
IV. DISTRIBUTED ALGORITHMS FOR DIMENSIONALITY REDUCTION

In this section we introduce two algorithms to obtain the filtering matrices \( \{ W_{P,i} \} \) and \( W_B \), which are executed in the LDSP and BDSP respectively. The way the algorithms are explained here refers to the panels for simplicity, but can be extended to the backbone by using as channel matrix the equivalent one \( \tilde{H} \), presented before, and \( P \) equal to the number of processing nodes in backbone. More details about the backbone case can be found in Section V.

The first of the algorithms is a straightforward approach with relatively low computational complexity based on the known Matched Filter (MF) method, which we select conveniently as a comparison baseline for our proposed algorithm.

A. Reduced Matched Filter (RMF)

RMF consists of a reduced version of the known MF method. In this case, the filter \( W_i \) is built by the \( N_p \) strongest columns of \( H_i \). The strenght of a column \( h_n \) is defined as \( \| h_n \|^2 \). The \( M_p \times N_p \) filtering matrix of the \( i \)-th panel is then expressed as

\[
W_{RMF,i} = [h_{k_1}, h_{k_2}, \ldots, h_{k_{N_p}}],
\]

(11)

where \( h_{k_n} \) is the \( M_p \times 1 \) channel vector for the \( n \)-th user, and \( \{ k_n \} \) the set of indexes relative to the \( N_p \) strongest users \(^4\).

When RMF is applied at the panel level as local filtering, each output is associated to a certain user. Therefore, nodes in the backbone can combine data coming from the same user, in a similar fashion as in distributed MF \(^26\). The result of the filtering is available at CDSP input for final detection (hard or soft). It is important to notice that in this method front-end processing nodes can work independently, without sharing channel related information. This saving in interconnection bandwidth comes with a performance loss as we will see in Section VI.

B. Iterative Interference Cancellation (IIC)

The IIC algorithm aims to solve the optimization problem described in (9). It is an iterative algorithm based on a variant of the known multiuser water-filling method \(^27\). The pseudocode is shown in Algorithm 1. The algorithm splits the joint optimization problem (9) into \( P \) small ones, which are solved in a sequential basis. The goal of the algorithm is to calculate the \( M_p \times N_p \) matrices \( \{ Q_i \} \). The product \( Q_i Q_i^H \) is low-rank as \( N_p \leq M_p \), which exploits the fact that only a few users are conveniently seen by each panel (ideally this number is \( N_p \)). The fundamental difference between our current algorithm and \(^27\) is due to the low-rank constraint present in our proposed algorithm.

At each iteration of the algorithm, \( K \times K \) matrix \( Z_i \) is obtained as intermediate result, which contains contribution from the rest of panels, and plays the role of noise covariance in the sum-rate optimization problem formulated in line 4.

\(^4\)This is connected to the non-uniform user power distribution in the LIS, described in Section II-A, which translates to the fact that a panel may not see all users with same power, which depends on their physical proximity.

\(^5\)For simplicity and to limit latency, we consider only one iteration to the set of panels throughout the rest of this article. We are aware that increasing the number of iterations improves the performance.

\[
\text{Algorithm 1: IIC algorithm pseudocode}
\]

| Preprocessing | \( Q_i = 0, i = 1 \ldots P \) |
|---------------------------------|---------------------------------|
| Input | \( \{ H_i \}, i = 1 \ldots P \) |
| repeat | |
| for | \( i = 1, 2, \ldots, P \) do |
| \( Z_i = I_K + \rho \sum_{j=1,j\neq i}^P H_j^H Q_j H_j \) |
| \( Q_i = \arg \max_{Q_i} |Q_i^H Q_i H_i + Z_i| \) |
| subject to | \( Q_i^H Q_i = I_{N_p} \) |
| end | |
| until sum-rate converges; |
| Output | \( \{ Q_i \}, i = 1 \ldots P \) |

The algorithm iterates over all panel indexes, as many times as needed until a certain convergence criteria is achieved.

C. Processing Distribution

It is natural to map each iteration of the IIC algorithm to each panel, as it requires local CSI, while \( Z_i \) can be computed also locally as an update of \( Z_{i-1} \). Therefore, each panel computes and shares \( Z_i \) with the neighbor panel, \( i+1 \), while \( Q_i \) is stored locally for further filter calculation, and not shared.

We propose that panels are connected by fast local and dedicated connections for the exchange of data related to matrix \( Z \). In general, we can say that "the matrix \( Z \) is passed from panel to panel" using the dedicated connections depicted in Fig. 3. This decentralized approach is described in Algorithm 2 for a certain panel \( i \) \(^5\).

\[
\text{Algorithm 2: Decentralized IIC algorithm at } i\text{-th panel}
\]

| Preprocessing | \( Z_0 = I_K \) |
|---------------------------------|---------------------------------|
| Input | \( \{ H_i, Z_{i-1} \} \) |
| 1 | \( Q_i = \arg \max_{Q_i} \left[ \rho H_i^H Q_i H_i + Z_{i-1} \right] \) |
| subject to | \( Q_i^H Q_i = I_{N_p} \) |
| 3 | \( Z_i = Z_{i-1} + \rho H_i^H Q_i H_i \) |
| Output | \( \{ Q_i, Z_i \} \) |

The solution to the local optimization problem at \( i \)-th panel is \( Q_i = [u_1, u_2, \ldots, u_{N_p}] \), where \( u_n \) is the \( n \)-th left-singular vector of \( H_i = H_i U_i \Sigma_i^{-1/2} \) corresponding to the \( n \)-th ordered singular value, and \( Z_{i-1} = U_i \Sigma_i U_i^H \) the eigen-decomposition of \( Z_{i-1} \) (see Appendix-B for proof).

The pseudocode for the processing at the \( i \)-th panel is shown in Algorithm 3, where \( \tilde{U} \) is the left unitary matrix of \( H \), and \( Q_i \) is made by the eigenvectors associated to the \( N_p \) strongest singular values.

D. Selection of \( W \) in IIC Algorithm

In the single panel case (centralized LIS), the optimal selection of \( Q \) leads to \( Q = \tilde{U}_H^H \), where \( \tilde{U}_H \) is a \( M \times N \)
AlGORITHM 3: Decentralized IIC algorithm processing steps for i-th panel

\begin{itemize}
  \item \textbf{Input}: \{H_i, Z_{i-1}\}
  \item \[ U_z, \Sigma_z = \text{svd}(Z_{i-1}) \]
  \item \[ H_i = H_i U_z \Sigma_z^{-1/2} \]
  \item \[ \tilde{U} = \text{svd}(H_i) \]
  \item \[ Q_i = \tilde{U}(:, 1 : N_p) \]
  \item \[ Z_i = Z_{i-1} + \rho \tilde{W} H_i Q_i \Sigma_i H_i^T \]
\end{itemize}

Output: \{Q_i, Z_i\}

semi-unitary matrix made by the \(N\)-first left singular vectors of \(H\). Then, capacity will be given by the first \(N\) largest singular values of \(H\). Once \(Q\) is known, in order to select \(W\), we notice that \(W = Q \Sigma_W V_{\text{sh}}^T\), where \(\Sigma_W\) is a diagonal \(N \times N\) matrix containing the \(N\) largest singular values of \(W\). Selection of \(\Sigma_W\) and \(V_W\) does not play any role in the sum-rate capacity, but the right choice can provide some benefits in other areas. In this work we choose \(\Sigma_W = I_N\) to make \(W\) semiunitary matrix, which brings a benefit in terms of reduction of interconnection bandwidth, that will be explained in next section. Selection of \(V_W\) can be arbitrary, and for simplicity we choose \(V_W = I_N\). However, other unitary matrices are also valid, and could offer some advantages, but we do not cover this in the present work.

In the multiple panel case, (9) represents a joint optimization problem among the matrices in the set \(\{Q_i\}\). Similarly to the single panel case, \(W_i = Q_i \Sigma_{W,i} V_{W,i}^T\). Therefore, once \(Q_i\) is obtained, the selection of \(\Sigma_{W,i}\) and \(V_{W,i}\) will follow identical considerations, this is: \(\Sigma_{W,i} = I_{N_p}\), and \(V_{W,i} = I_{N_p}\).

V. INTERCONNECTION TOPOLOGY AND DSP ARCHITECTURE

In this section we describe the proposed LIS architecture, including interconnection topology, and LDSP internal architecture able to support both RMF and IIC algorithms.

A. Tree-based Global Interconnection and Processing

In order to further increase the dimensionality reduction of the incoming data, while performing spatially localized processing, we propose a hierarchical interconnection based on tree topology. The tree represents a distributed backplane, where front-end processing nodes are the leaves, and their outputs are combined in backplane nodes through multiple levels, reducing the total inter-connection bandwidth each time, until the resulting data is delivered to the CDSP. This process if shown in Fig. 4. The main idea is to enable system scalability by adding levels in the tree as the LIS grows (more panels), while keeping the CDSP resources demand constant (dependent only on \(K\)) regardless of the LIS size. Another benefit of the tree topology is its low latency (the latency grows logarithmically with the number of panels).

As shown in the figure, the LIS backplane constitutes a 4-ary tree, which acts as an adaptation between the panels and the CDSP, introducing an extra dimensionality reduction of the incoming signal down to a level which can be efficiently transferred and handled by the CDSP, but high enough to allow good detection performance. Each node in the backplane contributes to \(W_B\), and aggregates data from 4 nodes, processes, and delivers the output to the next node. The dimensionality of the output is lower or equal to the input, this is: \(N_{b(i+1)} \leq 4N_{b(i)}\), \(i = 1, 2\), and \(N_{b(1)} \leq 4N_p\).

Let as assume the panels, during the formulation phase and after they obtain their local filtering matrix \(W_{P,i}\) (according to the selected algorithm), deliver the product \(W_{P,i}^T H_i (N_p \times K)\) to the corresponding node in the backplane. This can be seen as the result of filtering over the incoming pilot signals, which requires same amount of data as the filtering phase does. This product is the equivalent channel between the panel output and the users. A node aggregating outputs from 4 panels (4\(N_p\)) can see those incoming values as an equivalent channel including the wireless channel and the 4 panels combined. The dimensionality of this equivalent channel is \(4N_p\), which is lower compared to the 4\(M_p\) at the antenna level, but we expect it carries most of the captured channel capacity. If we take into account the selection of \(W_i\) in the panels as semiunitary matrices according to Subsection IV-D, then the noise will be also white at the panel output. And filtered noise from 4 adjacent panels is still white due to the independence property of noise of different antennas/panels. Therefore at any node in the backplane connected to the panels we have same model as in (1) with the equivalent channel instead of \(H_i\).
and the filtered noise instead of \( n \), but with same covariance (identity matrix) \(^6\). See Appendix-C for proof. This means that (5) and (6), and the sum-rate capacity derivation is also valid in this case with the equivalent channel, and the filter \( W_i^{(1)} \) can be found by solving the optimization problem (9). To obtain the filtering matrices, we follow the same problem described in Section III-B, with the same considerations as in IV-D for \( W_i \) selection. Because we have the same problem for dimensionality reduction as in the front-end, both algorithms described in Section IV can also be used in this case. This process can be repeated recursively for all levels of the tree up to the CDSP, which receives the total equivalent \( K \times K \) channel matrix between the CDSP input interface and the users. This is used by the CDSP for detection. The general formulation algorithm to be executed at a certain LDSP or BDSP follows the steps shown in Algorithm 4, where \( H_{eq} \) is the equivalent channel matrix from current node input interface to users \(^7\).

| Algorithm 4: General formulation algorithm for tree-based LIS |
|---------------------------------------------------------------|
| **Input**: \( \{H_{eq}, Z\} \) |
| 1. if \( algorithm == \text{IIC} \) then |
| 2. \( W = \text{IIC}(H_{eq}, Z) \) |
| 3. else |
| 4. \( W = \text{RMF}(H_{eq}) \) |
| end |
| **Output**: \( \{W^H H_{eq}, Z\} \) |

**B. DSP in panel and backplane nodes**

The internal architecture of the panel together with LDSP is depicted in Fig. 5. LDSP comprises all digital signal processing involved in the uplink tasks. After the RF and ADC, digitalized incoming signal is processed by FFT blocks to perform time-frequency domain transformation. During the formulation phase, the Channel Estimation block (CE) estimates a new \( H_i \) for each channel coherence interval. In this paper we assume perfect channel estimation. The Spatial Processing Unit (SPU), and specifically the Formulation Unit (FU) block receives \( H_i \) and computes the filtering matrix \( W_{P,i} \) (in the figure we drop the subscript \( P \) for convenience). FU performs complex conjugate transpose in the case of RMF, and follows steps in Algorithm 3 in the case of IIC. \( W_{P,i} \) is then written to the memory. During the filtering phase, incoming data vector gets multiplied by \( W_{P,i} \), and its dimensionality reduced from \( M_p \times 1 \) to \( N_p \times 1 \) (\( N_p \ll M_p \)), which is sent to the backplane for further processing.

The SPU is shown in the figure as part of the LDSP, but it also is present in the BDSP architecture. SPU is in charge of data collection, filtering, and distribution. It also performs matrix filtering calculation and its storing. In case of the BDSP architecture, SPU is its main processing element, as in this case FFT and channel estimation is not needed \(^8\). The filter can be either \( W_{B,i}^{(1)} \), or \( W_{P,i}^{(1)} \), depending on weather it is part of BDSP or LDSP respectively, and it supports both algorithms. The multiplexers allow to switch between filtering and formulation phase. It is important to notice that same input and output data ports are used during both phases. The dimensionality in both phases is the same. This design decision of using the same SPU architecture throughout the LIS is highly desirable, as it simplifies considerably the design time, verification, and cost of the system. Furthermore, by using the same unit, some or all the backplane nodes may potentially be mapped onto the panels, therefore reducing the number of physical units in the system (in the expense of increasing the workload in panels).

**VI. PERFORMANCE ANALYSIS AND DESIGN TRADE-OFFS**

In this section, we analyze the performance and implementation cost of the proposed uplink detection algorithms with the corresponding implementation architecture. More in detail:

- Performance is analyzed based on sum-rate capacity.
- Implementation cost in terms of computational complexity, interconnection bandwidth, and processing latency.

The trade-offs between sum-rate capacity and implementation cost is then presented to give high-level design guidelines.

**A. Performance: Optimality and capacity bounds**

Closed-form sum-rate expression for multi-panel LIS and IIC algorithm is out of the scope of this work, however we present two upper bounds which provide useful insights. Numerical evaluation of the bounds is shown in next subsection.

**Proposition 1.** For a certain channel realization \( H \), an upper bound for \( C_Z \) is given by

\[
C_Z \leq \min\{C_{ub1}, C_{ub2}\}, \quad (12)
\]

where

\[
C_{ub1} = K \log_2 \left( 1 + \rho \frac{S_{N_r}}{K} \right), \quad (13)
\]

and

\[
C_{ub2} = \sum_{n=1}^{K} \log_2(1 + \rho \lambda_n), \quad (14)
\]

where \( S_{N_r} = \sum_{i=1}^{P} \sum_{n=1}^{N_p} \lambda_n \), \( \lambda_n \) is the \( n \)-th eigenvalue of \( H^H H \), \( P \) is the number of panels, \( N_p \) is the number of users, and \( \rho \) is the effective channel gain. \( P N_p \geq K \) is assumed.

**Proof.** \( C_{ub2} \) corresponds to the single panel case, then it acts as an upper bound, as always outperforms the multiple-panel case under the same conditions of \( P \) and \( N_p \). See Appendix-A for proof of \( C_{ub1} \).

**B. Performance: Experimental results and simulation**

The scenario for simulation is shown in Fig. 6. It consists of 64 users (\( K = 64 \)) uniformly distributed in a \( 10m \times 10m \times 3m \) volume.

\(^6\)In case of not using semistochastic matrices, the noise gets colored and the covariance needs to be taken into account for sum-rate capacity optimization, therefore this noise covariance matrix needs also to be transferred between nodes in the tree. Selecting semistochastic matrices for the filters saves from this requirement.

\(^7\)Our experimental results shows no performance improvement by sharing \( Z \) among backplane nodes. Due to this reason we skip its use in Figure 4.

\(^8\)Even tough the SPU as a processing unit is identical at each node, data dimensionality may differ from one level to another in the system tree.
of the system, and then averaged across all realizations. The first analysis consists of studying the relation between sum-rate and SNR, and the validity of the bounds in different SNR regions for visual clarity.

For each realization, sum-rate capacity is calculated at different SNR values is shown in Fig. 7, which has been divided in two SNR regions for visual clarity. The first analysis consists of studying the relation between sum-rate and SNR, and the validity of the bounds in different SNR regions for visual clarity.

Selection of $N_p = 2$ allows us to have enough output panel dimensionality $^{11}$, specifically: $N = 128 > K$. Averaged values of the bounds are also shown for comparison. It is clear as $C_{ub1}$ is tight in the low SNR region, while both bounds follow the same slope ($K$) as the sum-rate for high SNR values, with $\sim 5dB$ offset in this case. $C_{ub2}$ is better bound than $C_{ub2}$ in this scenario.

The sum-rate capacity at CDSP input interface depends on the individual selection of the reduction factor at each node in the system, which leads to a considerable number of possibilities. In order to simplify the analysis and show in a clear form how this individuals selection affects the system performance, let as consider a tree with 3 levels (as in Fig. 4) where we constraint the reduction factors as follows: $\beta_2 = \beta_3$, and $\beta_3/\beta_2/\beta_1/\beta_p = K/M_p$, where $\beta_i = N_i/4M_i$. $\beta_p = N_p/M_p$, and $\beta_{b1} = N_p/4M_p$. By doing so, we ensure there is dimensionality $K$ at the CDSP input for every combination. Therefore, $\beta$ represents the dimensionality reduction at a certain level of the system (all nodes in a certain level are assumed to have same $\beta$ for simplicity$^{12}$), and may take values from 0 (total reduction) to 1 (no reduction). Under this constraint, $\beta_p$ and $\beta_{b1}$ are free to be chosen. Each possible combination provides different sum-rate at CDSP interface, in exchange of different complexity cost $^{13}$. Fig. 8 shows the relation between these two parameters and the normalized sum-rate (value 1 refers to channel capacity measured at antenna interface, and consequently it is the same for both algorithms) for RMF and IIC. It is important to note as multiple ($\beta_p$, $\beta_{b1}$) working points on the same contour level provide the same performance.

$^{11}$ $N_p > 2$ also meet this requirement, but at the expense of an increase interconnection bandwidth.

$^{12}$ We foresee a non-uniform $\beta$ case can be more adequate for scenarios with non-uniform user distribution, which allows to spend resources where it is needed. This is left for further analysis.

$^{13}$ Computational complexity and interconnection bandwidth.
(a) Low SNR

(b) High SNR

Fig. 7: Average sum-rate capacity at panels output interface vs SNR. Upper bounds in Proposition 1 also shown in low and high SNR regimes. $M = 1024$, $M_p = 16$, $N_p = 2$, and $K = 64$.

(a) RMF

(b) IIC

Fig. 8: Sum-rate capacity normalized by channel capacity at CDSP interface for different values of $\beta_b$ vs $\beta_p$. $\beta_b = \beta_b = \beta_b = \beta_b$. $M = 1024$, $M_p = 16$, $K = 64$, $\rho = 10$. Black dots represent simulated cases. Rest is obtained by linear interpolation.

We verify as a lower reduction (higher $\beta$) leads to higher capacity (but higher interconnection bandwidth), reaching the maximum (or close to it) if no reduction is taking place in the first two levels (point (1,1) in the figure). It is evident as IIC allows higher reduction for same performance compared to RMF, which translates in lower complexity during filtering, in exchange of higher formulation complexity (computational due to SVD dependency, and interconnection due to the panel-panel local exchange of data).

C. Computational Complexity

We consider number of complex multiplications (MAC) as a metric to measure computational complexity. Our analysis includes both phases: formulation and filtering. In the filtering phase, the operations are the same for RMF and IIC, which consists of applying a linear filter in the panels, of size $N_p \times M_p$, to the $M_p \times 1$ input vector, and similar for the BDSP nodes (with different sizes). The total computational complexity for filtering is given by (in MAC/s)

$$C_{\text{filt}} = f_B P C_{\text{filt}}^{(0)} + \sum_{n=1}^{L} N_{\text{SPU}}^{(n)} C_{\text{filt}}^{(n)} + \sum_{n=1}^{L} N_{\text{SPU}}^{(n)} C_{\text{filt}}^{(n)}$$

where $f_B$ is the signal bandwidth, $C_{\text{filt}}^{(0)} = M_p N_p$ is the computational complexity per panel to filter one subcarrier, $C_{\text{filt}}^{(n)} = 4 N_b^{(n)} N_b^{(n)}$ is the corresponding in a node at level $n$, $L$ is the number of levels in the tree, $N_{\text{SPU}}^{(n)}$ is the number of SPUs at level $n$, this is $N_{\text{SPU}}^{(n)} = \frac{L}{b}$, and $N_b^{(0)} = N_p$ for notation commodity.

The formulation phase of RMF includes the computation of $\|h\|^2$ for each user. For the IIC algorithm, the steps required for the formulation phase are shown in Algorithm 3 for each
Fig. 9: Sum-rate capacity normalized by channel capacity at CDSP interface versus computational complexity (9a) and interconnection data-rate (9b). In all cases, results for different panel sizes are shown, together with both algorithms. For both cases: $\beta_1 = \beta_2$. Simulated points represent different $N_p$ values. Sum-rate capacity versus computational complexity (9c), and versus interconnection data-rate for different LIS size (9d). $M_p = 64$, IIC method, and $\rho = 10$. $K = 64$ in all cases.

This algorithm relies on singular value decomposition (SVD), which we assume is based on 2 steps: Householder bidiagonalization and QR method by Givens rotations. Bidiagonalization is dominant in terms of complexity, so the total computational complexity of SVD of a $M \times N$ complex matrix can be approximated by $2M^2N$. For step 1 of the Algorithm 3, SVD of a $K \times K$ Gramian matrix $Z_{i-1}$ is required, with complexity $2K^3$. Step 2 has a complexity of $(M_p + 1)K^2$, step 3 combined together with 4 require a complexity of $2N_p d_0^2$, where $d_0 = \max\{K, M_p\}$. $H_{eq}^H W H$ consists of $N_p M_p K$ products, and step 5 of $N_p K^2$. The total computational complexity for IIC is given by (in MACs)$^{15}$

$$C_{form,IIC} = N_{PRB} PC_{(0)}^{(0)}_{form} + N_{PRB} \sum_{n=1}^{L} N_{SPU} C_{(n)}^{(n)}_{form}$$ (16)

For backend there is no exchange of $Z$ as explained in Section V, so the computational complexity is highly reduced.

$^{14}$We assume one channel estimate per PRB, and therefore one filtering matrix calculation per PRB.

$^{15}$We assume one channel estimate per PRB, and therefore one filtering matrix calculation per PRB.
LIS, where aggressive reduction can be used. In summary, the small LIS \((M = 1024)\) is harvesting a significant fraction of the available channel capacity, while the larger LIS is only exploiting a very small fraction of it. This presents a very interesting design trade-off.

### D. Interconnection bandwith

In this section we analyze the inter-connection bandwidth during filtering phase, covering panel-node and node-node links. This bandwidth is given by (in bps)

\[
R_{\text{inter}} = 2w_f B P N_p + 2w_f B \sum_{n=1}^{N} N_{\text{SPU}}^{(n)} N_b^{(n)} ,
\]

where \(w\) is the bit-width of the SPU input/output (real and imaginary parts). In our analysis we also consider the movement of data happening internally at panels/nodes level, which covers the data transfer between the inputs ports to the SPU, for processing, and from it to the output ports. We name this transfer data-rate as \(R_{\text{intra}}\) as intra-connection data-rate or \(R_{\text{intra}}\) \(^{16}\), and

\[
R_{\text{intra}} = 2w_f B P (M_p + N_p)
\]

\[
+ 2w_f B \sum_{n=1}^{N} N_{\text{SPU}}^{(n)} / 4 N_b^{(n-1)} + N_b^{(n)}. \]

In order to take both magnitudes into consideration in our analysis, we define the relative cost \(\alpha\), as

\[
\alpha \triangleq \frac{\text{cost}(R_{\text{intra}})}{\text{cost}(R_{\text{inter}})},
\]

and the cost equivalent inter-connection data-rate \(R_{\text{eq}}\) as:

\[
R_{\text{eq}} \triangleq R_{\text{inter}} + \alpha R_{\text{intra}}.
\]

In this analysis, we take power/data-rate as cost magnitude. If we assume serial link (serdes) technology for intra-connection, and Ethernet for inter-connection, then we obtain a power consumption of \(1.29 - 24.8\text{mW/Gbps}, \) and \(40\text{mW/Gbps} \) respectively according to different sources \([29]-[32]\). The serdes power range is very wide, so as an example we take \(4\text{mW/Gbps}\) as reference, which gives \(\alpha \approx 1/10\). \(^{17}\)

Figure 9b shows normalized sum-rate capacity versus equivalent inter-connection bandwidth during filtering for different LIS size (IIC assumed). Similar conclusions can be extracted compared to Fig. 9c.

### E. Processing Latency

The processing latency represents the time between when the estimated channel of a subcarrier is available at panels and when the data of that subcarrier is filtered and available at the CDSP input for detection. The latency can be expressed as

\[
L_{\text{tot}} = L_{\text{form}} + L_{\text{filt}},
\]

where \(L_{\text{form}}\) is the formulation latency, and \(L_{\text{filt}}\) is the latency for data filtering. More specifically, \(L_{\text{form}} = \sum L_{\text{form}} + (N_p - 1) L_{\text{com}}_{\text{local}} + (L + 1) L_{\text{com}}_{\text{global}}\), where \(L_{\text{form}}\) is the time needed to calculate the filter coefficients, \(L_{\text{com}}_{\text{local}}\) refers to panel-to-panel communication latency (only in IIC), and \(L_{\text{com}}_{\text{global}}\) refers to panel-to-node, and node-to-node link communication latency. \(N_p\) is the number of panels involved \((n_p = 1)\) in RMF and \(P\) in IIC for the worst case \(^{18}\). For filtering latency we have: \(L_{\text{filt}} = L_{\text{filt}}^f + L_{\text{com}}_{\text{local}}\), which accounts for filtering in panels and nodes, and communication latency. We assume the IIC formulation is done sequentially along all panels (worst case) using local connections, and then across nodes in the tree.

The latency for processing highly depends on the hardware architecture used to implement the algorithms. Here we assume highly optimized accelerators (e.g., ASIC) are used that the available data parallelism \((N_{\text{paral}})\) can be explored using \(N_{\text{proc}}\) processing units \((N_{\text{proc}} < N_{\text{paral}})\), i.e., the \(N_{\text{proc}}\) PEs will take \(N_{\text{paral}} / N_{\text{proc}}\) clock cycles to iteratively process \(N_{\text{paral}}\) parallel operations. Moreover, the channel matrix (of the subcarrier that is being processed) is cached in registers (the latency for memory access is hidden). The main component of \(L_{\text{form}}\) is the time needed to perform SVD which is implemented by Householder bidiagonalization followed by QR method based on Givens rotations. The processing of each column and row can be done in parallel, while sequential processing is needed between columns and rows due to the data dependency.

With these assumptions, the total processing latency in formulation phase is \(L_{\text{form}} = \frac{C_{\text{form}} T_{\text{CLK}}}{N_{\text{proc}}}\), where

\[
C_{\text{form}} = n_{\text{paral}} C_{\text{form}}^{(0)} + \sum_{n=1}^{N} C_{\text{form}}^{(n)}.
\]

The first term in \(C_{\text{form}}\) represents the serial processing in the front-end, and the second term represents the computational complexity of one branch of the tree, \(C_{\text{form}}^{(0)}\) and \(C_{\text{form}}^{(n)}\), are defined after \((16)\). \(T_{\text{CLK}}\) is the clock period, and we assume that one complex multiplication and accumulation (MAC) can be done within one clock cycle. In case of filtering, processing latency is given by \(L_{\text{filt}} = \frac{C_{\text{filt}} T_{\text{CLK}}}{N_{\text{proc}}}\), where \(C_{\text{filt}} = \sum_{n=0}^{N} C_{\text{filt}}^{(n)}\) is the computational complexity corresponding to a path between a panel and the CDSP, and \(C_{\text{filt}}^{(n)}\) is defined after \((15)\).

### F. Case study and discussion

Performance has been analyzed, together with computational complexity, inter-connection data-rate, and processing latency. General expressions for these different magnitudes

\(^{16}\)We are aware that \(R_{\text{data}}\) does not include all internal data-rate in a real system, as this is highly dependent on the specific implementation, internal topology, and type of processing unit employed in the panel. However, the spirit of this work is to provide a general analysis and first order approximation of the complexity required, applicable to all possible implementations, instead of being attached to an specific hardware implementation, and provide exact analysis numbers.

\(^{17}\)These numbers are dependent on the technology used, however, the method still holds.

\(^{18}\)Depending on the users distribution we may not need to go through all panels \((n_p < P)\) with the subsequent benefits. We leave both items for future work.
have been presented based on general system parameters, such as number of users, number of antennas, number of panels, and signal bandwidth among others; what makes it easy to particularize for concrete implementations. Nevertheless, based on the trade-off analysis shown in Fig. 9a and Fig. 9b, we can see $M_p = 64$ as an attractive option, as it provides higher capacity than $M_p = 16$ for same computational complexity and interconnection data-rate, while it is able to reach channel capacity in our analysis scenario. It is also of a reasonable size in case we want to distribute the LIS in a certain area. On top of that, its physical dimensions makes it easy to handle and mount (30cm $\times$ 30cm at 4GHz). For this panel size we present numerical values of the analyzed complexity in Table I. The following parameter values are assumed: $N_p = 16$, $T_{CLK} = 1\text{ns}$, $N_{paral} = 100$, $T_{local} = 100\text{ns}$ (serdes technology assumed [29, 30]), and $L_{global} = 300\text{ns}$ (ethernet assumed [31–33]). Assuming 12 subcarriers per PRB, the subcarrier spacing in our example is: $\frac{32768}{12\times30}$ = 30KHz, and the OFDM symbol duration is therefore $\approx 33\mu$s.

The benefits of the distributed architecture are evident in terms of interconnection data-rate reduction. If we look at the CDSP input interface, the reduction is easily obtained as: $\frac{M}{M_p} \approx 20x$. Of course, this is in exchange of a performance loss due to dimensionality reduction, but as we have explained before the system is fully configurable, offering a rich performance-complexity trade-off. It is important to consider that even tough computational complexity and inter-connection data rates numbers may seem large, they are distributed among all processing units in the LIS. This LIS contains 21 SPUs (panels + backplane nodes).

Regarding latency, $L_{form,RMF}$ and $L_{filt}$ values seem reasonable for NR frame structure. We observe as $L_{form,IC}$ shows much higher value due to the higher computational complexity required in this method (in this example equivalent to 3 OFDM symbols). For a certain LIS system this latency is sensitive to the $\beta$ used in panels and nodes (which translates into complexity cost), and $K$ (system capacity). Therefore we can foresee a trade-off between these system parameters and how often filters are updated in panels and nodes. It is important to remark that we analyzed latency from a worst case point of view, where all panels in the LIS are serially connected and jointly contribute to formulation. In reality we do not think this is the best approach as this may only be helpful in cases with very high density of users with dominant interference over noise. We foresee groups of panels performing serial processing within, but parallel among groups, reducing considerably the formulation latency.

We are aware that depending on the implementation latency may be different (selection of memory system, hardware, interconnection), and here we provide high level analysis assuming we use dedicated accelerators without any overhead.

### VII. Conclusions

In this article we have presented distributed uplink processing algorithms and the corresponding hardware architecture for efficient implementation of large intelligent surfaces (LIS). The proposed processing structure consists of local panel processing units to reduce incoming data dimensionality without losing much information, and hierarchical backplane network with distributed processing-combining units to support flexible and efficient data aggregation. We have systematically analyzed the system capacity and implementation cost with different design parameters, and provided design guidelines for the implementation of LIS.

## APPENDIX

### A. Proof of Proposition 1

**Proof.** The sum-rate capacity with the multi-panel architecture is given by

$$ C = \log_2 |I_K + \rho A|, \quad (17) $$

where $A = \sum_{i=1}^P H_i^H Q_i H_i$. For a certain channel realization, the maximum capacity is achieved if all eigenvalues of $A$ are equal, this is: $\lambda_n = \bar{\lambda}, 1 \leq n \leq K$. In that case, the capacity would be: $C_{nh1} = K \log_2(1 + \rho \bar{\lambda})$. Now, let us find the maximum value for $\bar{\lambda}$ as follows

$$ \bar{\lambda} = \max_{\{Q_i\}} \frac{1}{K} \sum_{i=1}^P \max_{\{H_i\}} \text{tr}\{H_i^H Q_i H_i\} = \frac{1}{K} \sum_{i=1}^P \sum_{n=1}^{N_E} \lambda_n^{(i)}, $$

and then: $C \leq C_{nh1}$, so the proposition is proven.\footnote{Note that we assume $\text{rank}(A) = K$, and $P N_P \geq K$.}

### B. Proof of solution to local optimization in Algorithm 2

**Proof.** We drop the panel index for simplicity. The objective function to maximize is

$$ |\rho H^H Q Q^H H + Z| = |Z| \text{tr}\{I_K + \rho Z^{-1/2} H H^H Q Q^H H Z^{-1/2}\} = |Z| \text{tr}\{I_{N_E} + \rho Q H Z^{-1} H^H Q\} = |Z| \text{tr}\{Q^H (\rho H Z^{-1} H^H + I_{M_F}) Q\}. $$

$|Z|$ does not depend on $Q$, therefore the solution to our problem is the same as the solution of the maximization of the second determinant, which consists of the ordered eigenvectors (in descent order of corresponding eigenvalue) of the matrix: $H Z^{-1} H^H$.\footnote{We remark this bound may not be attained in practice, as it needs a favorable set of $\{H_i\}$, or in other way, there may not be such $\{Q_i\}$ that provides uniform eigenvalues in $A$.}

| Method | $C_{\text{form}}$ | $C_{\text{filt}}$ | $R_{\text{inter}}$ | $R_{\text{intra}}$ | $L_{\text{form}}$ | $L_{\text{filt}}$ |
|--------|----------------|----------------|----------------|----------------|---------------|---------------|
| IIC    | 3.1            | 2.3            | 1.0            | 5.4            | 110.2         | 1.0           |
| RMF    | 0.02           | 2.3            | 1.0            | 5.4            | 1.2           | 1.0           |

TABLE I: Values of total complexity for a LIS: $M = 1024$, $M_p = 64$, $K = 50$, $\beta_p = 1/4$, $\beta_{M_p} = 1/2$. $w = 12$ bits. $N_{PRB} = 275$. $f_{\text{fb}} = 100\text{MHz}$. Units are as follows: $C_{\text{form}}$ [GMAC], $C_{\text{filt}}$ [TMAC/s], $R_{\text{inter}}$ [Tb/s], $R_{\text{intra}}$ [Tb/s], $L$ [\mu s].
C. Proof of white filtered noise

As an example, the filtered noise due to the first four panels and the node connected to them is denoted as \( n_{1-4} \) and obtained as:

\[
\begin{align*}
\mathbf{n}_{1-4}^{(1)} &= \mathbf{W}_{1}^{(1)H} \mathbf{W}_{P,1-4} \mathbf{n}_{P,1-4},
\mathbf{w}_{P,1-4} &= \text{diag}(\mathbf{W}_{P,1}, \mathbf{W}_{P,2}, \mathbf{W}_{P,3}, \ldots, \mathbf{W}_{P,4}),
\end{align*}
\]

and \( n_{1-4} \) is the aggregated input noise vector corresponding to the first four panels and it is defined as:

\[
\begin{align*}
n_{1-4} &= [n_1, n_2, n_3, n_4]^T.
\end{align*}
\]

The covariance is given by:

\[
\begin{align*}
\mathbb{E} \left\{ \mathbf{n}_{1-4}^{(1)H} \mathbf{n}_{1-4}^{(1)} \right\} &= \mathbf{W}_{1}^{(1)H} \mathbf{W}_{P,1-4} \mathbb{E} \left\{ \mathbf{n}_{1-4} \mathbf{n}_{1-4}^H \right\} \mathbf{W}_{P,1-4}^{(1)H} \\
&= \mathbf{W}_{1}^{(1)H} \mathbf{W}_{P,1-4} \mathbf{I}_4 \mathbf{M}_p \mathbf{W}_{P,1-4}^{(1)H} \\
&= \mathbf{W}_{1}^{(1)H} \mathbf{I}_4 \mathbf{N}_p \mathbf{W}_{1}^{(1)H} = \mathbf{I}_n^{(1)}
\end{align*}
\]

REFERENCES

[1] J. R. Sánchez, O. Edfors, F. Rusek, and L. Liu, “Processing Distribution and Architecture Tradeoff for Large Intelligent Surface Implementation,” in 2020 IEEE International Conference on Communications Workshops (ICC Workshops), 2020, pp. 1–6.

[2] J. R. Sánchez, F. Rusek, O. Edfors, and L. Liu, “An Iterative Interference Cancellation Algorithm for Large Intelligent Surfaces,” arXiv e-prints, p. arXiv:1911.10804, Nov. 2019.

[3] S. Hu, F. Rusek, and O. Edfors, “Beyond Massive MIMO: The Potential of Data Transmission With Large Intelligent Surfaces,” IEEE Transactions on Signal Processing, vol. 66, no. 10, pp. 2746–2758, May 2018.

[4] S. Hu, F. Rusek, and O. Edfors, “The Potential of Using Large Antenna Arrays on Intelligent Surfaces,” in 2017 IEEE 85th Vehicular Technology Conference (VTC Spring), June 2017, pp. 1–6.

[5] S. Hu, K. Chiu, F. Rusek, and O. Edfors, “User Assignment with Distributed Large Intelligent Surface (LIS) Systems,” in 2018 IEEE 29th Annual International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC), Sep. 2018, pp. 1–6.

[6] S. Hu, F. Rusek, and O. Edfors, “Beyond Massive MIMO: The Potential of Positioning With Large Intelligent Surfaces,” IEEE Transactions on Signal Processing, vol. 66, no. 7, pp. 1761–1774, April 2018.

[7] M. Di Renzo, A. Zappone, M. Debbah, M. S. Alouini, C. Yuen, J. de Rosny, and S. Tsytaev, “Smart Radio Environments Empowered by Reconfigurable Intelligent Surfaces: How It Works, State of Research, and The Road Ahead,” IEEE Journal on Selected Areas in Communications, vol. 38, no. 11, pp. 2450–2525, 2020.

[8] E. Basar, M. Di Renzo, J. De Rosny, M. Debbah, M. Alouini, and R. Zhang, “Wireless Communications Through Reconfigurable Intelligent Surfaces,” IEEE Access, vol. 7, pp. 116753–116773, 2019.

[9] C. Huang, S. Hu, G. C. Alexandropoulos, A. Zappone, C. Yuen, R. Zhang, M. D. Renzo, and M. Debbah, “Holographic MIMO Surfaces for 6G Wireless Networks: Opportunities, Challenges, and Trends,” 2019.

[10] A. Taha, M. Alrabeiah, and A. Alkhateeb, “Enabling Large Intelligent Surfaces with Compressive Sensing and Deep Learning,” arXiv e-prints, p. arXiv:1904.10136, Apr. 2019.

[11] Y. Han, W. Tang, S. Jin, C. Wen, and X. Ma, “Large Intelligent Surface-Assisted Wireless Communication Exploiting Statistical CSI,” IEEE Transactions on Vehicular Technology, vol. 68, no. 8, pp. 8328–8342, Aug. 2019.

[12] C. Huang, G. C. Alexandropoulos, A. Zappone, M. Debbah, and C. Yuen, “Energy Efficient Multi-User MISO Communication Using Low Resolution Large Intelligent Surfaces,” in 2018 IEEE Globecom Workshops (GC Wkshps), Dec 2018, pp. 1–6.

[13] M. Jung, W. Saad, Y. Jung, G. Kong, and S. Choi, “Performance Analysis of Large Intelligent Surfaces (LISs): Asymptotic Data Rate and Channel Hardening Effects,” IEEE Transactions on Wireless Communications, vol. 19, no. 3, pp. 2052–2065, 2020.

[14] J. V. Alegria and F. Rusek, “Achievable Rate with Correlated Hardware Impairments in Large Intelligent Surfaces,” in 2019 IEEE 8th International Workshop on Computational Advances in Multi-Sensor Adaptive Processing (CAMSAP), 2019, pp. 559–563.

[15] D. Dardari, “Communicating with Large Intelligent Surfaces: Fundamental Limits and Models,” IEEE Journal on Selected Areas in Communications, pp. 1–1, 2020.