The Design of High Precision Arbitrary Waveform Generator Based on DDS Technology and FPGA

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Abstract: Combining with the IP core advantage of FPGA, a signal generator which can generate arbitrary waveform is designed on the basis of direct digital synthesis technology in this paper. The INTEL company’s Cyclone IV series EP4CE6F17C8N is used as the control core and the front-end interface design is carried out by XMAL. The software control operation of the logical processing interface is realized through C#. The signal generator has the characteristics of single cycle waveform with 256 sampling points, clear spectrum analysis, high purity and high precision. The arbitrary waveform displayed on oscilloscope is wonderful after filtering out high frequency signal by seven order butter worth filter.

1. Introduction

Signal generator is a kind of equipment instrument which can generate repeat or not repeat frequency electrical signal. It is a common signal source and widely used in scientific research, medical treatment, daily communication, mechanical and aerospace engineering and all kinds of maintenance engineering. Similar functionality and digital type sampler, signal generator, the image signal generator.

Since the 1960s, the signal generator has developed very rapidly. Both at home and abroad, a large number of studies have been carried out on it. A new type of signal generator, such as scanning type signal generator, program-controlled signal generator and synthetic signal generator emerged successively. What’s more, the signal generator has also made significant progress in simplifying the mechanical structure, miniaturization, easy to use etc.

2. Overall design of system

2.1 System analysis

Common DDS signal generator designed by FPGA has a shortcoming, which cannot generate arbitrary waveform. The basic working principle of DDS is based on the look-up table. The ROM storage block corresponding to the waveform must be generated in advance, and cannot be switched to arbitrary waveform during use. The general overall framework of DDS is shown in figure 1. The waveform used in this design method is the waveform stored by DDS in advance, and it cannot realize arbitrary waveform in the real sense such as random number noise wave, which has great limitations.
2.2 The project design

In order to change the waveform arbitrarily in the process of use, a dual-port RAM in the IP core can be used. Because it can be asynchronous separated in reading and writing, reading and writing are irrelevant, which greatly facilitate the design. The control core of this design is FPGA. Complex data operation is processed by the upper system and then sent back to FPGA by serial interface. FPGA carries out specific regulation of frequency and waveform according to received back data and instructions. Theoretically, as long as the waveform period data to be displayed is given, the implementation of any waveform can be completely regulated within a certain frequency range.

According to the sampling theorem, the maximum undistorted frequency obtained should be 0.5 times of the sampling frequency. To instantaneously generated waveform data and written to RAM of FPGA, the data calculated according to the waveform equation can be written to RAM directly in real-time in the upper system. Because the received data of the console is a series of string, Mathematica can be used to convert the string to functions and external platform is used to call the core to calculate and return to the host system. PC host software block diagram is shown in figure 2.

3. Upper computer design

Development of the upper computer has a variety of options, Matlab, Mathematica, Python, Labview development, or C/C++, VB, C# etc. Each development method has its own advantages, C# is used to develop the upper computer in this design.

The frequency control word of the module is calculated by the upper computer software, and the data is segmented by C#.

Because the serial port cannot receive 32-bit data at one time, data is needed to be segmented, and then a complete frequency control word can be obtained by using FPGA to integrate the data after internal reception.

The core design of upper computer is to provide equation to the kernel by the upper computer first, then to calculate by the kernel, next to callback to the upper computer when the calculation is completed, finally to send the data to the lower computer by serial port after the data processed by the upper computer.
4. Lower computer design

4.1 Serial port module

The serial port module includes sending module and receiving module. The sending module uses FPGA to send test data to the serial port. In order to facilitate the observation of the results, the sending module and the receiving module were connected and tested.

4.2 DDS control module

DDS control module is the core of this design, including the core control module, phase accumulation module and dual port RAM read-write module.

Direct digital frequency synthesis technology is a new type of frequency synthesis technology that combines the concept of phase accumulation and uses the phase accumulation characteristics to generate the required waveform. By using this technology, the frequency, amplitude and phase can be adjusted and controlled conveniently. Frequency calculation formula of DDS output signal is as follows:

\[ F_{out} = \frac{2^N}{F_{dk}} \times F_{out} \]  

(1)

\( F_{out} \) is the output frequency, \( B \) is the frequency control word, \( F_{dk} \) is the clock frequency.

If the clock frequency \( F_{dk} = 50 \text{MHZ} \), \( N = 8 \), \( B = 1 \), the output waveform frequency of ROM obtained \( F_{out} \) is 195.3125Khz.

The frequency control word is calculated by the PC upper computer. After calculation, it is sent back to FPGA by using the serial port. FPGA stores it in a 32-bit register. According to RS232 protocol, frequency control word is needed to be converted to 32-bit hexadecimal number and divided into four 8-bit hexadecimal number and then sent to FPGA internal register according to the order. Register integrates it to 32-bit hexadecimal number according to the data received successively, then the data is transferred to the DDS control core. After successful receiving the data is used to carry out phase accumulation.

The schematic diagram of frequency control word test circuit is shown in figure 3.

![FIG.3 frequency control word test circuit](image)

In order to verify whether the data is received successfully, the logic analyzer Modelsim can be used for simulation before actual use. SignalTap II is used in all simulation tests of the design, and the test results are shown in figure 4.

![FIG.4 the sampling results of SignalTap II](image)

It can be seen from figure 7 that the program correctly reads the data received from the serial port and integrates it into 32-bit hexadecimal data.
4.3 Dual port RAM read-write module

ROM is generally used in traditional DDS waveform storage, which cannot change waveform during device operation. Dual-port RAM can solve this problem, because it has the function of asynchronous reading and writing.

A dual-port RAM with 256 data depths, asynchronous data reading and writing, 8-bit address widths, and M9K storage type is instantiated by using the quartus IP core. Dual-port RAM is used to receive the data sent from PC, and the waveform data is stored in the RAM, and then taken out from RAM by using phase accumulation, after D/A transformation, a complete waveform can be generated.

4.4 Top-level design of the lower computer

Modular design method is used in the main program of the lower computer, and its top-level design schematic is shown in figure 5.

![FIG. 5 schematic diagram of the top-level design of the lower computer](image)

5. Analysis of real-time data sampling waveform

5.1 Commonly used output waveform

Signal Tap II is adopted to sample and analyze the system, and the typical sine waves obtained are shown in FIG. 6.

![FIG.6 real-time data sampling waveform of sine wave in Signal Tap II](image)

As can be seen from the figure above, the resulting sine wave is smooth and clean, with almost no burrs. In order to analyze the performance of the design, the logic analyzer is used to collect several kinds of waveforms commonly used. Both sine wave, square wave, triangular wave and sawtooth wave show good effect.

5.2 Output waveform of compound function

In addition to the common basic waveform, this design can also generate a complex functional waveform such as a function composed of sine wave and triangular wave by using the arbitrary waveform generation mode of the upper computer. The function equation is $\text{TriangleWave} \left( \frac{x}{2\pi} \right) + \sin(x + 0.5\pi)$, the waveform is shown in figure 7.
The arbitrary waveform generation mode of the upper computer is adopted to generate a compound functional waveform composed of square wave and triangular wave, as shown in FIG.8. The function equation is: 

\[ \text{TriangleWave}\left(\frac{x}{2\pi}\right) + \text{SquareWave}\left(\frac{x}{2\pi} + 0.5\pi\right). \]

5.3 Arbitrary output waveform

Most waveform does not have functional expressions except for the basic waveform commonly used, such as manually edited waveform, random number waveform, audio waveform, natural waveform and so on. At this point, the corresponding waveform is needed to be generated by waveform data.

To use the random number generation function of Wolfram, 256 random numbers are generated and sent to FPGA. The collection results using Signal Tap II are shown in figure 9.

5.4 Hand-drawn waveform

Hand-drawn waveform is also a way to generate waveform. Drawing on the middle and high-end signal generator, this design manually draws waveform through ROM tool MifMake of FPGA, as shown in FIG. 16. After processing with the generated .Mif file, the corresponding data is extracted and sent to FPGA for display, and the display result is shown in FIG.10.

5.5 Oscilloscope display of waveform

Finally oscilloscope is used to see the actual effect. The actual performance has a certain relationship to the sampling depth, the actual use should also be combined with D/A converter and high-pass filter. AD9708 chip produced by AD company is used to carry out D/A convert ion in this design. The filter is a seven-order butter-worth filter with a bandwidth of 40MHz. The combined waveform of triangle wave and square wave which is shown in figure 11 is realized by connecting signal generator with oscilloscope.
FIG. 11 the actual display of compound wave of triangle wave and square wave on oscilloscope

In order to detect the display effect of waveform under various frequencies, the digital oscilloscope is used to show the results of various waveform, as shown in figure 12-15 below.

FIG.12 Triangular wave with a frequency of 500KHz
FIG.13 Sinusoidal wave with a frequency of 4MHz
FIG.14 Sinusoidal wave with a frequency of 1M
FIG.15 composite waveform with a frequency of 1200Hz

It can be seen from the oscilloscope that whether it is the basic waveform or the composite waveform, the overall waveform display is smooth. The display effect is very good which has no distortion, high bandwidth and excellent anti-interference characteristics. The comparison of theoretical and measured values of various waveform is showed in table 1.

| waveform         | theoretical output value (Hz) | actual measured value (Hz) | Error rate    |
|------------------|-------------------------------|-----------------------------|---------------|
| Sine wave        | 1000                          | 999.973                     | 0.00027%      |
| Square wave      | 1200                          | 1199.97                     | 0.00025%      |
| Triangle wave    | 500K                          | 499.989K                    | 0.00022%      |
| Composite wave   | 3.8M                          | 3.79992M                    | 0.00021%      |
Theoretically, the output range of the waveform is -5v ~ 5V (10Vpp), but due to the inaccuracy of the 5K potentiometer used by the module, the top elimination error will occur when the frequency is too high, the error rate is <3.5%, and it will only occur when the frequency exceeds 37MHz. The communication speed of the serial port is 9600bps. According to the calculation, it takes 4.58ms to switch the frequency once at this speed, and 0.29s to switch the waveform once.

Compared with common signal generators, signal generators with DDS as the core technology based on FPGA can flexibly generate more accurate, more stable and wider frequency range of sine wave, square wave, triangle wave and saw-tooth wave and other compound signals.

6. Conclusion

This design makes up for the short board of DDS chip, using RAM instead of ROM. Any waveform with high bandwidth and high precision can be realized with the special upper computer. Combined with D/A module, the amplitude can be adjusted conveniently. Moreover, the display effect on the oscilloscope is intuitive and the signal purity is good. The signal generator designed combined with its parallel operation, high execution speed, rich IP soft core and other advantages is better than the signal generator made with MCU whether in speed, performance or usability.

Acknowledgments
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