Approximate adder design with simplified lower-part approximation

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Abstract This letter presents a novel approximate adder that reduces energy and power consumption by leveraging a simplified lower-part approximation. The proposed scheme reduces hardware costs while providing an acceptable accuracy performance. Implemented in a 32-nm CMOS technology, the proposed adder achieves area and power reductions of 67% and 91%, respectively, compared to a conventional adder. In terms of energy, it improves the power-delay and energy-delay products by 13.1% and 17.0%, respectively, compared to the other approximate adders considered herein. In addition, when adopted in a digital image processing application, the proposed adder shows a very promising output quality compared to that produced by an exact adder while providing excellent energy efficiency.

Keywords: approximate adder, error tolerant adder, energy efficiency
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Addition is one of the heavily used arithmetic operations in many applications, and adders consume a significant amount of power and energy, which leads to hot-spot locations on processors [1]. Computationally intensive applications, such as image processing, machine learning, and data mining, may have inherent error tolerance, and a certain amount of computation error is acceptable in these applications [2, 3, 4, 5, 6]. Therefore, the design of efficient approximate adders that reduce power and energy has drawn great attention, and a large number of approximate adders have been proposed in the recent years [7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29].

The lower-part OR adder (LOA) divides an adder into two: accurate and inaccurate parts [7]. The accurate part uses a precise adder, such as a ripple carry adder (RCA), for normal additions on higher-order bits, whereas the inaccurate part exploits an OR operation to approximately add lower-order input bits. The optimized lower-part constant OR adder (OLOCA) is further improved the LOA by outputting “1” on a few least significant bit (LSB) outputs of the inaccurate part, regardless of the input [8]. The error tolerant adder I (ETAI) is also split into two parts as the LOA and OLOCA do. The key difference with the LOA stems from the inaccurate part where a modified XOR operation is used [9]. Additionally, the ETAI does not include any care predicate scheme for the precise adder, whereas the LOA does an AND-based carry prediction, which enhances the overall accuracy. Hence, a couple of ETAI variants that include a carry prediction technique to improve the accuracy were proposed in [10, 11]. The ETAI sequentially checks the input bits from the most significant bit (MSB) position to the LSB; therefore, the delay of the inaccurate part is a bit longer than that of the LOA and its variants [7, 8, 12]. In other words, the critical path delay will likely exist in the inaccurate part when its size is larger than the accurate part, resulting in overall speed degradation and poor energy efficiency.

This letter proposes a new energy and power efficient adder by simplifying the lower-part approximation of the ETAI to reduce hardware cost while maintaining a good computation accuracy. We systematically analyze the proposed design to obtain an optimal adder configuration, and extensively compare our design with other adders in terms of accuracy and hardware performance.

2. Proposed approximate adder design

Fig. 1 shows the general architecture of the proposed n-bit adder, termed the simplified error tolerant adder (SETA).

The n-bit adder consists of a k-bit precise adder to accurately add k MSB input (i.e., $S_{n-1:n-k} = A_{n-1:n-k} + B_{n-1:n-k}$) and an approximation logic simplified from the ETAI for the remaining lower-order $n-k$ inputs. The lower-part (i.e., inaccurate part) addition is basically achieved through the OR operation, which is similar to that of the LOA and ETAI. The proposed approximation logic checks the two $(i)^{th}$ input bits only by using an AND gate. If both bits are “1” (i.e., $A_i = B_i = 1$), then the lower-order output from the $(i-1)^{th}$ to $(0)^{th}$ bit positions (i.e., $S_{i-1:0}$) are set to “1” otherwise, the output does not change and keeps the OR gate output (i.e., $S_{n-1:k-1} = A_{n-k-1:0}$ OR $B_{n-k-1:0}$). Note that the bit position $i$ can be anywhere in $n-k-1 \leq i < 0$. We will seek an optimal position by systematically examining the accuracy and circuit performance in Section 3.

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The ETAI successively investigates the input bits from the MSB to LSB of the inaccurate part; thus, its delay \( t_{\text{inaccurate,ETAI}} \) is obtained by [10]

\[
t_{\text{inaccurate,ETAI}} = t_{\text{AND}} + (n - k - 3) \cdot t_{\text{OR}}.
\]

where \( n \) is the size of the entire adder, \( k \) is that of the precise adder, and \( t_{\text{AND}} \) and \( t_{\text{OR}} \) are the delays of a two-input AND gate and an OR gate, respectively.

In the proposed adder, only two gate delays are required to produce the output of the inaccurate part. As a result, the delay \( t_{\text{inaccurate,SETA}} \) is further reduced by

\[
t_{\text{inaccurate,SETA}} = \max(t_{\text{AND}}, t_{\text{OR}}) + t_{\text{OR}}.
\]

The proposed SETA produces an incorrect output when both inputs of any bit position of the inaccurate part are “1”. Hence, the error rate (ER) of the proposed adder under random input patterns \( ER_{\text{SETA}} \) is obtained by

\[
ER_{\text{SETA}}(n, k) = 1 - \left( \frac{3}{4} \right)^{n-k}.
\]

\( ER_{\text{SETA}} \) is independent of \( i \), and the ERs of the LOA, ETAI, and the proposed adder are identical because an error occurs at the same condition.

### 3. Experimental Results

The proposed adder together with an accurate adder (RCA) and other three approximate adders (LOA, OLOCA, and ETAI) were designed in Verilog HDL and synthesized with a 32-nm CMOS technology to determine the circuit performance in terms of area, delay, and power. The 16-bit adders were implemented using an 8-bit RCA based precise adder (i.e., \( n=16, k=8 \)). We also developed a simulator to evaluate the accuracy by extracting error metrics including the ER and normalized mean error distance (NMED). These metrics were estimated under 10 million (i.e., \( 10^7 \)) input pairs, each of which was uniformly generated random number.

### Table I  Power, NMED, and Power-NMED product (PNP) with various \( i \).

| \( i \) | 7 | 6 | 5 | 4 | 3 |
|---|---|---|---|---|---|
| Power (\( \mu W \)) | 30.60 | 30.53 | 30.45 | 30.38 | 30.31 |
| NMED (1e-3) | 2.81 | 2.87 | 2.90 | 2.92 | 2.93 |
| PNP (1e-3) | 86.08 | 87.71 | 88.42 | 88.67 | 88.87 |

First, we varied the design parameter \( i \) from 7 to 3 to seek the best tradeoff between accuracy and power. Table I shows the performance of the proposed approximate adder with various values of \( i \). The power decreases as \( i \) decreases because a smaller \( i \) requires less OR gates. In contrast, the accuracy degrades. Note that the delay and ER do not change as \( i \) varies. The power-NMED product (PNP) can be used to jointly evaluate the accuracy and power of the adder [30]. According to the product in Table I, the adder shows the best accuracy and power tradeoff at \( i = 7 \). Hence, our design with \( i = 7 \) is considered for comparison with the other adders. Note that they have a similar trend with \( i \) when \( k \) varies.

Table II summarizes the performances of the proposed adder and the other four adders. The RCA has the longest delay caused by the bit-by-bit carry propagation and consumes the most area and power. The lack of carry prediction allows the ETAI and SETA to be better in speed than the LOA and OLOCA; however, it degrades the NMED performance. The LOA occupies slightly more area than the SETA because the prediction requires a full adder at the LSB of the accurate part, whereas a half adder is formed at the corresponding bit in the SETA. Although the ER of the OLOCA reaches over 99%, the NMED is similar to the LOA. The accuracy of our adder is comparable to that of the ETAI, and it exhibits a better performance in area and power.

We obtain the power-delay product (PDP) and energy-delay product (EDP) to further evaluate the energy efficiency of our adder when compared with those of the other adders.

### Table II  Performance summary of various adders with \( n=16 \) and \( k=8 \).

| Design | Area (\( \mu m^2 \)) | Delay (ns) | Power (\( \mu W \)) | ER (%) | NMED (1e-3) |
|---|---|---|---|---|---|
| RCA | 190.4 | 1.79 | 58.5 | - | - |
| LOA | 115.8 | 0.88 | 33.4 | 89.99 | 1.71 |
| OLOCA | 102.1 | 0.88 | 30.9 | 99.12 | 1.77 |
| ETAI | 131.2 | 0.85 | 33.5 | 89.99 | 2.74 |
| SETA | 114.2 | 0.85 | 30.6 | 89.99 | 2.81 |

Fig. 2 shows the PDP and EDP of the proposed and three approximate adders. The LOA exhibits the worst energy efficiency, whereas our design is the most efficient. The OLOCA is comparable to the ETAI in both the PDP and EDP. The proposed adder improves the PDP and EDP by 13.1% and 17.0%, respectively, over the LOA. Clearly, our adder outperforms the others in terms of energy efficiency.

We applied an exact adder and our adder to a 5 x 5 Gaussian filter to build an accurate and an inaccurate filters and determine the impact of the approximation errors on real applications [23]. The peak signal-to-noise ratio (PSNR) is commonly used to evaluate the output image quality [19, 20], and was measured with the two adders. Fig. 3 depicts the output images with an exact adder (i.e., RCA) and the proposed adder. The PSNRs of the output processed by both adders are greater than 20dB. The exact and proposed adders produce visually indistinguishable output images, proving that the approximation errors generated by our adder negligibly affect the quality of the digital image processing application.

### 4. Conclusions

This letter proposed a new energy efficient approximate adder that adopts a simplification of the existing approximation scheme to reduce hardware costs. Implemented in a 32-nm CMOS process, our adder reduced the area and
power by 67% and 91%, respectively, over the RCA. Furthermore, the proposed design showed 13.1% and 17.0% better PDP and EDP, respectively, compared to the LOA. The effectiveness of the proposed adder was shown through a digital image processing application. Therefore, the proposed adder is highly suitable for designing energy efficient applications.

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Fig. 3 Original image and Gaussian filter output with two adders.