A Partial Order Reduction Technique for Event-driven Multi-threaded Programs

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1. Introduction

Event-driven multi-threaded programming is fast becoming a preferred style of developing efficient and responsive applications. In this concurrency model, multiple threads execute concurrently, communicating through shared objects as well as by posting asynchronous events that are executed in their order of arrival. In this work, we consider partial order reduction (POR) for event-driven multi-threaded programs. The existing POR techniques treat event queues associated with threads as shared objects and thereby, reorder every pair of events handled on the same thread even if reordering them does not lead to different states. We do not treat event queues as shared objects and propose a new POR technique based on a novel backtracking set called the dependence-covering set. Events handled by the same thread are reordered by our POR technique only if necessary. We prove that exploring dependence-covering sets suffices to detect all deadlock cycles and assertion violations defined over local variables. To evaluate effectiveness of our POR scheme, we have implemented a dynamic algorithm to compute dependence-covering sets. On execution traces obtained from a few Android applications, we demonstrate that our technique explores many fewer transitions — often orders of magnitude fewer — compared to exploration based on persistent sets, wherein, event queues are considered as shared objects.

Abstract

Event-driven multi-threaded programming is fast becoming a preferred style of structuring concurrent computations in many domains. In this model, multiple threads execute concurrently, and each thread may be associated with an event queue. Threads may post events to each other’s event queues, and a thread can post an event to its own event queue. For each thread with an event queue, an event-loop processes the events from its event queue in the order of their arrival. The event-loop runs the handler of an event only after the previous handler finishes execution but interleaved with the execution of all the other threads. Further, threads can communicate through shared objects; even event handlers executing on the same thread may share objects. Event-driven multi-threaded programming is a staple of developing efficient and responsive smartphone applications [22]; a similar programming model is also used in distributed message-passing applications, high-performance servers, and many other settings.

Stateless model checking [12] is an approach to explore the reachable state space of concurrent programs by exploring different interleavings systematically but without storing visited states. In practice, the success of stateless model checking depends crucially on partial order reduction (POR) techniques [5, 11, 29, 36]. Stateless search with POR defines an equivalence class on interleavings, and explores only a representative interleaving from each equivalence class (called a Mazurkiewicz trace [21]), but still provides certain formal guarantees w.r.t. exploration of the complete but possibly much larger state space. Motivated by the success of model checkers based on various POR strategies [2, 3, 7, 10, 12, 13, 28, 31, 41], in this work, we propose an effective POR strategy for event-driven multi-threaded programs.

Motivating example. We first show why existing POR techniques may not be very effective in the combined model of threads and events. Consider a partial execution trace of an event-driven program shown in Figure 1. The operations are executed from top to bottom. The operations in the trace are labeled $r_1$ to $r_5$ and those belonging to the same event handler are enclosed within a box labeled with the corresponding event. These operations are executed by the threads $t_1$, $t_2$ or $t_3$. Figure 1 enumerates all the operations executed by a thread on a vertical line below the thread. An operation $post(e)$ under thread $t$ denotes the enqueuing of an event $e$ by thread $t$. The destination event queue can be identified by mapping the event posted with the corresponding event label against an event handler. For example, the operation $r_1$ executed by thread $t_1$ posts an event $e_1$ to thread $t_1$’s event queue. In this trace, threads $t_2$ and $t_3$ respectively post events $e_1$ and $e_2$ to thread $t_1$’s event queue. The event handler of $e_1$ in turn posts an event $e_3$ to $t_1$’s queue. The event handlers of $e_2$ and $e_3$ respectively write to shared variables $y$ and $x$.

Figure 2 shows the state space reachable through all valid permutations of operations in the trace in Figure 1. Each node indicates a state of the program. An edge is labeled with an operation and indicates the state transition due to that operation. The interleaving corresponding to the trace in Figure 1 is highlighted with bold lines and shaded states. For illustration purposes, we explicitly show the contents of the event queue of thread $t_1$ at some states. Events in a queue are ordered from left to right. Pictorially, an event is removed from the queue when it is dequeued for handling.

Existing POR techniques (e.g., [2, 10, 11, 31, 34]) recognize that $r_2$ and $r_5$ (also $r_1$ and $r_4$) are independent (or non-interfering) and that it is sufficient to explore any one of them at state $s_6$ (respectively, $s_{10}$). The dashed edges indicate the unexplored transitions. However, existing POR-based model checkers will explore all other states and transitions. Since no two handlers executed on the thread...
Our approach. Realizing a partial order reduction technique effective for event-driven programs requires reviewing of various elements of POR and redesigning them to be suitable in the context of event-driven programs. To realize the reduction outlined through motivating example, we do not consider event queues as shared objects. Equivalently, we treat a pair of post operations as independent with sequence events posted to an event queue, and transitions compared to existing techniques.

Figure 1: A partial trace of an event-driven program.

$\text{Figure 2: The state space reachable through all valid permutations of operations in the trace given in Figure 1. The leftmost event in an event queue is the front of the queue.}$

$t_1$ modify a common object, all the interleavings reach the same state $s_5$. Thus, the existing techniques explore two redundant interleavings. This happens because these techniques treat event queues as shared objects and so, mark any two post operations that enqueue events to the event queue of the same thread as dependent. Consequently, they explore both $r_1$ and $r_2$ at state $s_0$, and $r_2$ and $r_3$ at state $s_1$. These result in unnecessary reorderings of events.

More generally, if there are $n$ events posted to an event queue, these techniques may explore $O(n!)$ permutations among them, even if exploring only one of them may be sufficient. Therefore, a POR technique that can avoid redundant event orderings can be significantly more scalable. We exploit this observation. For the state space in Figure 2, our approach explores only the initial trace (the leftmost interleaving) and thus visits substantially fewer states and transitions compared to existing techniques.

Given a notion of POR, a model checking algorithm such as DPOR [10] uses persistent sets [11] to structure the state space exploration to only explore representative transition sequences from each Mazurkiewicz trace. As we show now, DPOR based on persistent sets is unsound when used in conjunction with the dependence relation in which posts are independent. Let us revisit the state space given in Figure 4. Assume DPOR to explore this state space starting with the leftmost branch of the state space in Figure 4, which corresponds to sequence $w$ shown in Figure 3. Then, DPOR identifies the set $\{r_1\}$ as persistent in state $s_0$, because exploring any transition other than $r_1$ from state $s_0$ does not hit a transition dependent with $r_1$. This set is tagged as PS in Figure 4. However, a selective exploration using this set explores only one ordering between $r_3$ and $r_6$, even though the two orderings are not equivalent.
Our third contribution is the notion of dependence-covering sets as an alternative to persistent sets. A set of transitions \( L \) at a state \( s \) is said to be dependence-covering (formalized in Definition 2.6) if a dependence-covering sequence \( u \) starting with some transition in \( L \) can be explored for any sequence \( v \) executed from \( s \). We prove that selective state-space exploration based on dependence-covering sets is sufficient to detect all deadlock cycles and violations of assertions over local variables. The dependence-covering sets at certain states are marked in Figure 4 as DCS. In contrast to PS, DCS at state \( s_0 \) contains both \( r_1 \) and \( r_2 \). The set \( \{r_1, r_2\} \) at \( s_0 \) is a dependence-covering set because for any transition sequence \( u \) starting from \( s_0 \), there exists a dependence-covering sequence \( v \) starting with a transition in \( \{r_1, r_2\} \). Let \( v \) be the transition sequence along the rightmost interleaving in Figure 4. The sequence \( u \) (the leftmost interleaving) is not a dependence-covering sequence of \( v \) since the dependent transitions \( r_3 \) and \( r_6 \) appear in a different order. We therefore require \( r_2 \) to be explored at \( s_0 \). Note that, \( \{r_2\} \) is another dependence-covering set at \( s_0 \) as both the orderings of dependent transitions \( r_3 \) and \( r_6 \) can be explored from \( s_{10} \) reached on exploring \( r_2 \).

Our final contribution is a dynamic algorithm called EM-DPOR to compute dependence-covering sets. EM refers to the Event-driven Multi-threaded concurrency model. EM-DPOR follows the DFS based exploration strategy of DPOR [10] but the key steps of our algorithm are different. In particular, EM-DPOR incorporates several non-trivial steps (1) to reason about both multi-threaded dependences as well as dependent transitions from different event handlers on the same thread (single-threaded dependences), and (2) to identify events for selective reordering and infer appropriate backtracking choices to achieve the reordering. We have implemented and evaluated this adaptation in a proof-of-concept model checker. Further, we have provided a sketch outlining the proof of correctness of our algorithm in Appendix B.

We now briefly explain how EM-DPOR computes the dependence-covering sets and explores the state space shown in Figure 4 starting with sequence \( w \). On exploring a prefix of sequence \( w \) and reaching state \( s_5 \), EM-DPOR identifies \( r_6 \) to be dependent with \( r_3 \) and hence tries to reorder \( r_6 \) w.r.t. \( r_3 \). It does so by attempting to execute transitions that happen before \( r_6 \) prior to \( r_3 \), ultimately leading to the execution of \( r_6 \) prior to \( r_3 \). When attempting to compute backtracking choices at state \( s_2 \) (the state where \( r_3 \) is explored) to reorder \( r_3 \) and \( r_6 \), EM-DPOR finds \( r_4 \) to happen before \( r_6 \). However, \( r_4 \) is not enabled at \( s_2 \) because both \( r_3 \) and \( r_4 \) execute on the same thread \( t_1 \), and \( r_4 \) is a transition of the handler of \( e_2 \) while \( e_1 \) is at the front of the queue (see the event queue shown at \( s_2 \) in Figure 4). Because EM-DPOR is aware of the event-driven semantics and knows that \( r_3 \) and \( r_4 \) come from handlers of two different events \( e_1 \) and \( e_2 \), it attempts to reorder the events themselves. We call this a step to reschedule pending events because \( e_2 \) is pending in the queue of the thread \( t_1 \) at \( s_2 \). EM-DPOR then starts another backward search to identify the backtracking choices that can reorder \( e_1 \) and \( e_2 \). It identifies that the corresponding post operations \( r_1 \) and \( r_2 \) can be reordered to do so. It therefore adds \( r_2 \) to the backtracking set at \( s_0 \) (from Figure 4 \( r_1 \) is already in the backtracking set at \( s_0 \) since the exploration started with \( w \)), exploring which leads to \( s_8 \) where event \( e_2 \) precedes \( e_1 \) in the event queue as required. EM-DPOR then reaches state \( s_{10} \) where \( r_3 \) and \( r_6 \) are co-enabled. Being dependent, EM-DPOR explores both the ordering between \( r_3 \) and \( r_6 \) from \( s_{10} \). Note that even while considering only \( r_3 \) and \( r_6 \) from different threads as dependent, EM-DPOR is able to identify a seemingly unrelated pair of posts at \( r_1 \) and \( r_2 \) for reordering.

**Experiments.** We have evaluated EM-DPOR on Android applications which are a class of multi-threaded event-driven programs. We have implemented a proof-of-concept model checking framework called EM-Explorer which simulates the non-deterministic behaviour exhibited by Android applications given individual execution traces. We implemented EM-DPOR which performs a selective state-space exploration based on dependence-covering sets, in EM-Explorer. For comparison, we also implemented DPOR which performs exploration based on persistent sets, where posts to the same thread are considered dependent. We performed experiments on traces obtained from 5 Android applications. Our results demonstrate that our POR technique explores many fewer transitions — often orders of magnitude fewer — compared to using persistent sets.
2. Formalization

We now formalize our notion of partial order reduction for event-driven programs. Some of the definitions below follow the conventions in [10]. Any reference to persistent sets henceforth, assumes usage of the dependence relation defined in [11] as it is, which marks two \( \text{post} \) operations to the same event queue as dependent.

2.1 Transition System

We consider an event-driven multi-threaded program \( A \) which has the usual sequential and multi-threaded operations such as assignments, conditionals, synchronization through locks and thread creation. In addition, the operation \( \text{post}(t_1, e, t_2) \) posts an asynchronous event \( e \) from the source thread \( t_1 \) to (the event queue of) a destination thread \( t_2 \). However in the execution traces given in the paper, we omit the source and destination threads of \( \text{post} \) operation (e.g., Figure 1 and 3) when apparent from the diagram. Each event has a handler which runs to completion on the thread to whose event queue the event is posted. However, the event handler of one thread may interleave operations of other threads. Operation \( \text{deq}(e) \) denotes the dequeuing of an event \( e \), and \( \text{end}(e) \) indicates the completion of execution of an event handler. We consider \( \text{deq} \) and \( \text{end} \) as the first and the last operation of an event handler. In the traces considered in this paper, all the operations belonging to the same event handler are grouped inside a box (e.g., Figure 1 and 3). The operations \( \text{deq} \) and \( \text{end} \) are omitted but implicitly assumed as the first and the last operation inside the box. We omit the formal syntax and semantics of various operations relevant in the context of a multi-threaded event-driven program; they can be found in [20].

An operation is visible if it accesses an object shared between at least two threads or two event handlers (possibly running on the same thread). The first operation (\( \text{deq} \)) of an event handler is also considered a visible operation. All other operations are invisible.

The local state of an event handler is a valuation of the stack and the variables or heap objects that are modified only within the event handler. The local state of a thread is the local state of the currently executing event handler. If a handler running on a thread has finished executing, but the thread has not started executing the next handler (if any), we say that the thread is idle; the local state of an idle thread is undefined. A global state of the program \( A \) is a valuation to the variables and heap objects that are accessed by multiple threads or multiple handlers. Even though event queues are shared objects, we do not consider them in the global state (as defined above). Instead, we define a queue state of a thread as an ordered sequence of events that have been posted to its event queue but are yet to be handled. This separation allows us to analyze asynchronous posts more precisely. Event queues are FIFO queues with unbounded capacity, that is, a \( \text{post} \) operation never blocks. For simplicity, we assume that every thread is associated with an event queue. If a thread does not have an event queue in reality then its state is determined by the default procedure that runs on it in response to some initial event, and no other events are enqueued to its event queue subsequently.

Let \( L, G \) and \( Q \) be the set of all local states, global states and queue states respectively. Let \( Th \) be the set of all threads in \( A \). Then, a state \( s \) of an event-driven program \( A \) is a triple \((l, g, q)\) where (1) \( l \) is a partial map from \( Th \) to \( L \), (2) \( g \) is a global state and (3) \( q \) is a total map from \( Th \) to \( Q \). A transition by a thread \( t \) updates the state of \( A \) by performing one visible operation followed by a finite sequence of invisible operations ending just before the next visible operation; all of which are executed on \( t \). We identify a transition by its visible operation, e.g., we say “\( \text{post} \) operation” to mean a transition whose first operation is a \( \text{post} \). Let \( R \) be the set of all transitions in \( A \). A transition \( r_{t,\ell} \) of a thread \( t \) at its local state \( \ell \) is a partial function, \( r_{t,\ell} : G \times Q \rightarrow L \times G \times Q \). A transition \( r_{t,\ell} \in R \) is enabled at a state \( s = (l, g, q) \) if \( \ell = l(t) \) and \( r_{t,\ell}(g, q) \) is defined. We may use \( r_{t,\ell}(s) \) to denote application of a transition \( r_{t,\ell} \), instead of the more precise use \( r_{t,\ell}(g, q) \). The first transition of the handler of an event \( e \) enqueued to a thread \( t \) is enabled at a state \( s \), if \( e \) is at the front of \( t \)’s queue at \( s \) and \( t \) is idle in \( s \). We assume that if a transition is defined for a state then it deterministically maps the state to a successor state.

We formalize the state space of \( A \) as a transition system \( \mathcal{S}_C = (S, s_{init}, \Delta) \), where \( S \) is the set of all states, \( s_{init} \in S \) is the initial state, and \( \Delta \subseteq S \times S \) is the transition relation such that \((s, s') \in \Delta \) iff \( \exists r \in R \) and \( s' = r(s) \). We also use \( s \in \mathcal{S}_C \) instead of \( s \in S \). Two transitions \( r_1 \) and \( r_2 \) may be co-enabled if there may exist some state \( s \in S \) where they both are enabled. Two events \( e \) and \( e' \) handled on the same thread \( t \) may be reordered if there exist states \( s, s' \in S \) such that \( s = (l, g, q) \), \( s' = (l, g', q') \), \( q(t) = e \cdot w \cdot e' \cdot w' \) and \( q'(t) = e' \cdot v \cdot e' \cdot v' \). In Figure 2, events \( e_1 \) and \( e_2 \) may be reordered but not \( e_1 \) and \( e_3 \).

For simplicity, we assume that all threads and events in \( A \) have unique IDs. We also assume that the state space is finite and acyclic.

This is a standard assumption for stateless model checking [10]. The transition system \( \mathcal{S}_C \) collapses invisible operations and is thus already reduced when compared to the transition system in which even invisible operations are considered as separate transitions. A transition system of this form is sufficient for detecting deadlocks and assertion violations [12]. We note that the event dispatch semantics can be diverse in general. For example, Android applications permit posting an event with a timeout or posting a specific event to the front of the queue. We over-approximate the effect of posting with timeout by forking a new thread which does the \( \text{post} \) non-deterministically but do not address other variants in this work. We leave a more general POR approach that allows such variants to event dispatch, to future work.

Notation. Let \( next(s, t) \) give the next transition of a thread \( t \) in a state \( s \). Let \( thread(r) \) return the thread executing a transition \( r \). If \( r \) executes in the handler of an event \( e \) on thread \( t \) then the task of \( r \) is \( task(r) = (t, e) \). A transition \( r \) on a thread \( t \) is blocked at a state \( s \) if \( s = next(s, t) \) and \( r \) is not enabled in \( s \). We assume that only visible operations may block. Function \( nextTrans(s) \) gives the set of next transitions of all threads at state \( s \). For a transition sequence \( w : r_1, r_2 \ldots r_n \) in \( \mathcal{S}_C \), let \( dom(w) = \{1, \ldots, n\} \). Functions \( getBegin(w, e) \) and \( getEnd(w, e) \) respectively return the indices of the first and the last transitions of an event \( e \)’s handler in \( w \), provided they belong to \( w \). For a transition \( r \), \( index(w, r) \) gives the position of \( r \) in \( w \).

Deadlock cycles and assertion violations. A pair \( (DC, \rho) \) in a state \( s \in S \) is said to form a deadlock cycle if \( DC \subseteq nextTrans(s) \) is a set of \( n \) transitions blocked in \( s \), and \( \rho \) is a one-to-one map from \( [1, n] \) to \( DC \) such that each \( \rho(i) \in DC \), \( i \in [1, n] \), is blocked by some transition on a thread \( t_{i+1} = thread(\rho(i+1)) \) and may be enabled only by a transition on \( t_{i+1} \), and the transition \( \rho(n) \in DC \) is blocked and may be enabled by two different transitions of thread \( t_1 = thread(\rho(1)) \). A state \( s \) in \( \mathcal{S}_C \) is a deadlock state if all the threads are blocked in \( s \) due to a deadlock cycle.

An assertion \( \alpha \) is a predicate over local variables of an event handler and is considered visible. A state \( s \) violates an assertion \( \alpha \) if \( \alpha \) is enabled at \( s \) and evaluates to false.

2.2 Dependence Relation

The notion of dependence between transitions is well-understood for multi-threaded programs. It extends naturally to event-driven programs if event queues are considered as shared objects, thereby, marking two \( \text{post} \)s to the same event queue as dependent. To enable more reductions, we define an alternative notion in which two
post operations to the same event queue are not considered dependent. One reason to selectively reorder events posted to a thread is if their handlers contain dependent transitions. This requires a new notion of dependence between transitions of event handlers executing on the same thread, which we refer to as single-threaded dependence.

In order to explicate single-threaded dependences, we first define an event-parallel transition system which over-approximates the transition system \( S_C \). The event-parallel transition system \( P_G \) of a program \( A \) is a triple \( (S_P, s_{init}, \Delta_P) \). In contrast to the transition system \( S_C = (S, s_{init}, \Delta) \) of Section 2.1 where events are dispatched in their order of arrival and execute till completion, a thread with an event queue in \( P_G \) removes any event in its queue and spawns a fresh thread to execute its handler. This enables concurrent execution of handlers of events posted to the same thread. Rest of the semantics remains the same. Let \( Th \) and \( Th_P \) be the sets of all threads in \( S_C \) and \( P_G \) respectively. For each state \( (l, g, q) \in S \), there exists a state \( (l', g', q') \in S_P \) such that (1) for each thread, reflexive and symmetric relation \( \Delta_P \). The relation \( D_P \) is a valid event-parallel dependence relation iff for all \( (r_1, r_2) \in R_P \times R_P \), \( (r_1, r_2) \notin D_P \) implies that the following conditions hold for all states \( s \in S_P \):

1. If \( r_1 \) is enabled in \( s \) and \( s' = r_1(s) \) then \( r_2 \) is enabled in \( s' \) iff it is enabled in \( s' \).
2. If \( r_1 \) and \( r_2 \) are both enabled in \( s \) then there exists \( s'' = (l'', g'', q'') = r_1(r_2(s)) \) such that \( l'' = l' \) and \( g'' = g' \).

This definition is similar to the definition of dependence relation in [12] except that we do not require equality of the states \( q' \) and \( q'' \) in the second condition above. Clearly, any pair of post-transitions, even if posting to the same event queue, are independent according to the event-parallel dependence relation.

Definition 2.2. Let \( R \) be the set of transitions in the transition system \( S_G \) of a program \( A \). Let \( D \subseteq R \times R \) be a binary, reflexive and symmetric relation. The relation \( D \) is a valid dependence relation iff for all \( (r_1, r_2) \in R \times R \), \( (r_1, r_2) \notin D \) implies that the following conditions hold:

1. If \( r_1 \) and \( r_2 \) are transitions of handlers of two different events \( e_1 \) and \( e_2 \) executing on the same thread then the following conditions hold:
   (A) Events \( e_1 \) and \( e_2 \) may be reordered in \( S_G \).
   (B) \( ep(r_1) \) and \( ep(r_2) \) are independent in \( D_P \), i.e., \( \langle ep(r_1), ep(r_2) \rangle \notin D_P \).
2. Otherwise, conditions 1 and 2 in Definition 2.1 hold for all states \( s \in S \).

In the definition above, we use the event-parallel dependence relation \( D_P \) to formalize single-threaded dependence between transitions of two handlers in \( S_C \) and apply the constraints in Definition 2.1 in states in \( S_C \) to define (1) dependence among transitions of the same event handler and (2) multi-threaded dependence. From the second condition in Definition 2.2, all post operations are considered independent of each other in \( S_C \).

Example 2.3. The transitions \( r_5 \) and \( r_6 \) in Figure 5 run in two different event handlers but on the same thread \( t \). Since in the event-parallel transition system, the handlers execute concurrently, we can inspect the effect of reordering \( r_5 \) and \( r_6 \) on a state where they are co-enabled. In particular, at state \( s_3 \) in Figure 6, the sequence \( r_6, r_5 \) reaches state \( s_{14} \), whereas, \( r_5, r_6 \) reaches \( s_{12} \) which differs from \( s_{14} \) in the value of \( x \). Therefore, \( (r_5, r_6) \in D_P \) and by condition 1.B of Definition 2.2, \( (r_5, r_6) \notin D \).

The condition 1.A of Definition 2.2 requires that the ordering between \( e_1 \) and \( e_2 \) should not be fixed. Suppose the handler of \( e_1 \) posts \( e_2 \) but the two handlers do not have any pair of transitions that are in \( D_P \). Recall that we do not track dependence through event queues. Nevertheless, since a post transition in \( e_1 \) enables \( e_2 \), the transitions in the two handlers should be marked as dependent. This requirement is met through condition 1.A. Intuitively, it serves a purpose analogous to condition 1 of Definition 2.1.

In practice, we over-approximate the dependence relation, for example, by considering all conflicting accesses to shared objects as dependent.

2.3 Dependence-covering Sets

Mazurkiewicz trace [21] forms the basis of POR for multi-threaded programs and event-driven programs where post operations are considered dependent. Two transition sequences belong to the same Mazurkiewicz trace if they can be obtained from each other by reordering adjacent independent transitions. The objective of POR is to explore a representative sequence from each Mazurkiewicz trace. As pointed out in the Introduction, the reordering of post operations (dependent as per Definition 2.2) in a transition sequence \( w \) may not yield another sequence belonging to the same Mazurkiewicz trace (denoted \( [w] \)) for two reasons: (1) it may reorder dependent transitions from the corresponding event handlers and (2) some new transitions, not in \( w \), may be pulled in.

We elaborate on the second point. Suppose in \( w \), a handler \( h_1 \) executes before another handler \( h_2 \), both on the same thread, such that \( h_2 \) is executed only partially in \( w \). Let us reorder the post operations for these two and obtain a transition sequence \( w' \). Since the handlers run to completion, in order to include all the transitions of \( h_1 \) (executed in \( w \)) in \( w' \), we must complete execution of \( h_2 \). However, as \( h_2 \) is only partially executed in \( w \), this results in including new —previously unexplored— transitions of \( h_2 \) in \( w' \). This renders \( w \) and \( w' \) inequivalent by the notion of Mazurkiewicz equivalence which expects the set of transitions in two equivalent sequences to be identical.

We therefore propose an alternative notion, suitable to correlate two transition sequences in event-driven programs, called the dependence-covering sequence. The objective of our reduction is to explore a dependence-covering sequence \( u \) at a state \( s \) for any transition sequence \( w \) starting at \( s \).

Let \( w : r_1, r_2, \ldots, r_n \) and \( u : r_1', r_2', \ldots, r_m' \) be two transition sequences from the same state \( s \) in \( S_C \) reaching states \( s_n \) and \( s_m' \), respectively. Let \( R_w = \{ r_1, \ldots, r_n \} \) and \( R_u = \{ r_1', \ldots, r_m' \} \).
covering sequence among the following conditions holds: can have more transitions than \( w \). The transition sequence \( w \) also requires all the dependences in \( w \) to satisfy these criteria w.r.t. \( w \). Both \( w \) be seen in Figure 7(a), their dependence graphs are identical. Also, checking of event-driven programs where postconditions permit dependence-covering sequence to be a relaxation from nodes not in the subgraph. Transition sequences in Figure 6 which correspond to valid sequences in the transition system \( S \). For transitions \( i \) dependent then we draw an edge from \( i \). If a transition \( i \) is executed in \( i \) is not executed in \( i \) executes before \( i \). If a transition \( i \) is not in \( i \) is executed in \( i \) not in \( i \). Irrespective of whether \( i \) is executed in \( i \) or not, \( i \) is not in \( i \). The condition (i) above allows new transitions, that are not in \( w \), to be part of \( u \). The condition (ii) restricts how the new transitions may interfere with the dependences exhibited in \( w \) and also requires all the dependences in \( w \) to be maintained in \( u \). These conditions permit dependence-covering sequence to be a relaxation of Mazurkiewicz trace, making it more suitable for stateless model checking of event-driven programs where ports may be reordered selectively.

Example 2.5. As an example, let \( w_1, w_2 \) and \( w_3 \) be the three transition sequences in Figure 6 which correspond to valid sequences in the transition system \( S \) of the program in Figure 5. The sequences of transitions in \( w_1, w_2 \) and \( w_3 \) are listed in Figure 7. To illustrate dependence-covering sequences, we visualize the dependences in these sequences as directed graphs, called dependence graphs, in Figure 7. The nodes in the dependence graph of a transition sequence \( w \) represent transitions in \( w \). If a transition \( r_i \) executes before another transition \( r_j \) in \( w \) such that \( r_i \) and \( r_j \) are dependent then we draw an edge from \( r_i \) to \( r_j \). The sequences \( w_1 \) and \( w_2 \) are dependence-covering sequences of each other. As can be seen in Figure 7(a), their dependence graphs are identical. Also, both \( w_1 \) and \( w_2 \) are dependence-covering sequences of a sequence \( w_4 \). The dependence graph of \( w_4 \) is isomorphic to a subgraph (enclosed in a rectangular box) of Figure 7(a). For transitions \( r_1, r_3, r_4 \) and \( r_5 \) which do not belong to this subgraph, there are no restrictions on dependences among themselves. However, by Definition 2.4, there can be no incoming edge to the subgraph from nodes not in the subgraph. Transition sequences \( w_1 \) and \( w_2 \) satisfy these criteria w.r.t. \( w_4 \) and hence are dependence-covering sequences of \( w_4 \). However, we note that \( w_3 \) and \( w_1 \) (or \( w_2 \)) do not belong to the same Mazurkiewicz trace. The sequence \( w_3 \) is not a dependence-covering sequence of \( w_4 \) since there is an interfering dependence \( (r_6, r_5) \in D \) to the transition \( r_5 \) executed in \( w_4 \). Pictorially, we can see an incoming edge from \( r_6 \) to \( r_5 \) in Figure 7(b).

Note. An important takeaway from the above example is that a dependence-covering sequence \( u \) of a transition sequence \( w \) can reorder event handlers seen in \( w \) so long as the relative ordering of dependent transitions in \( w \) are not altered. Hence, in addition to identifying similarities between thread schedules, dependence-covering sequences enable identification of similar ordering between events as well. Recognizing similar event orderings was not possible with the Mazurkiewicz way of identifying equivalence between transition sequences.

Definition 2.6. A non-empty subset \( L \) of transitions enabled at a state \( s \) in \( S \) is a dependence-covering set in \( s \) iff, for all non-empty sequences of transitions \( w : r_1 \ldots r_n \) starting at \( s \), there exists a dependence-covering sequence \( u : r_1' \ldots r_m' \) of \( w \) starting at \( s \) such that \( r_m' \in L \).

Example 2.7. All the transition sequences connecting state \( s_2 \) to state \( s_3 \) in Figure 2 are dependence-covering sequences of each other. Thus, each of \( \{ r_1 \}, \{ r_2 \} \) and \( \{ r_1, r_2 \} \) are dependence-covering sets at \( s_2 \). Even if we take a prefix \( \sigma \) of any of these sequences, the shaded sequence in Figure 2 is a dependence-covering sequence of \( \sigma \).

In Figure 4, \( \{ r_2 \} \) and \( \{ r_1, r_2 \} \) are individually dependence-covering sets at state \( s_0 \), whereas, \( \{ r_1 \} \) is not a dependence-covering set at \( s_0 \).

For efficient stateless model checking of event-driven programs, we can explore a reduced state space using dependence-covering sets.

Definition 2.8. A dependence-covering state space of an event-driven program \( A \) is a reduced state space \( \bar{S} \subseteq S \) obtained by selectively exploring only the transitions in a dependence-covering set at each state in \( S \). The objective of a POR approach is to show that even while exploring a reduced state space, no concurrency bug is missed w.r.t. the complete but possibly much larger state space. The exploration of a dependence-covering state space satisfies this objective. The following theorem states this guarantee.

Theorem 2.9. Let \( S \) be a dependence-covering state space of an event-driven program \( A \) with a finite and acyclic state space \( S \).

Figure 5: Pseudo code of an event-driven program.

Figure 7: Dependence graphs of some sequences in \( S \) of the program in Figure 5.
Then, all deadlock cycles in $S_G$ are reachable in $S_R$. If there exists a state $v$ in $S_G$ which violates an assertion $\alpha$ defined over local variables then there exists a state $v'$ in $S_R$ which violates $\alpha$.

The proof follows from the appropriate restrictions on allowed dependences in a dependence-covering sequence $u$ compared to the dependences in $w$ where $w$ is required to reach a deadlock cycle or an assertion violation in the complete state space. We provide a complete proof of the above theorem in Appendix A.

The set $\{r_1, r_2\}$ is both a persistent set and a dependence-covering set at state $s_0$ in Figure 2. We observe that in general, a persistent set $P$ at a state $s \in S_G$ is also a dependence-covering set at $s$. Here, persistent set is defined using the dependence relation where posts to the same event queue are dependent, whereas, dependence-covering set is defined using the dependence relation where they are not (more formally, using Definition 2.2). We present a proof of this claim in Appendix A.3. Note that a dependence-covering set need not be a persistent set. As seen in Example 2.7. $\{r_1\}$ and $\{r_2\}$ individually are both dependence-covering sets at $s_0$ in Figure 2 but they are not persistent sets.

3. Dynamic Algorithm to Compute Dependence-covering Sets

This section describes the EM-DPOR algorithm for model checking event-driven multi-threaded programs to explore a dependence-covering state space (see Definition 2.8). EM-DPOR extends DPOR [10] to compute dependence-covering sets. However, it differs from DPOR in many key steps.

3.1 Comparison between DPOR and EM-DPOR

DPOR performs depth first traversal on the transition system of a program. Instead of exploring all the enabled transitions at a state, it only explores transitions added as backtracking choices by the steps of the algorithm which guarantees exploring a persistent set at each visited state. On exploring a sequence $w$ reaching a state $s'$, and seeing dependence between a transition $r' \in nextTrans(s')$ and a transition $r$ executed at a state $s$ reached by a prefix of $w$, DPOR adds backtracking choices at state $s$, so as to reorder $r$ and $r'$ eventually. However, not every pair of dependent transitions can be reordered. For example, a pair of dependent transitions where one transition enables the other, cannot be reordered. DPOR uses a dependence relation which implicitly considers every adjacent pair of transitions executed on the same thread as dependent, because executing a transition on a thread enables the execution of the next transition. Hence, DPOR only attempts to reorder dependent transitions which may be co-enabled, i.e., atleast executed on different threads. However, a pair of dependent transitions executed on different threads may have a strict ordering between them in a given execution, making them unsuitable for reordering at any state reached in that execution. DPOR uses happens-before relation, a partial order relation on dependent transitions, to capture the ordering between dependent transitions in a transition sequence. DPOR reorders only those may be co-enabled dependent transitions which are not ordered by happens-before relation over the explored sequence.

EM-DPOR, extends the DPOR [10] algorithm and computes dependence-covering sets. However, it differs from DPOR in several ways. In particular, EM-DPOR incorporates several non-trivial steps (1) to reason about both multi-threaded dependences as well as dependent transitions from different event handlers on the same thread (single-threaded dependences), and (2) to identify events for selective reordering and infer appropriate backtracking choices to achieve the reordering. In order to perform these steps, EM-DPOR uses the dependence relation defined in Definition 2.2, to identify dependent transitions. A happens-before relation based on this dependence relation does not totally order all the transitions executed on the same thread, and restricts the total ordering only within a task (due to the second condition in Definition 2.2). A task refers to an event handler or a thread without an event queue. Analogously, EM-DPOR attempts to reorder a pair of dependent transitions which may be co-enabled or executed in the handlers of may be reordered events (see Section 2.1) on the same thread. Typically, dynamic POR algorithms only reorder dependent transitions i.e., they add backtracking choices only at a state which executes a transition $r$ dependent with another transition $r'$ such that $r$ and $r'$ are identified for reordering. This is not the case with EM-DPOR. Due to atomic execution of event handlers and FIFO processing of events in a queue, reordering a pair of dependent transitions from different handlers on the same thread would require reordering their corresponding posts. Transitions posting to the same event queue may have to be reordered even to reorder dependent transitions on different threads, as shown for the state space in Figure 4. Hence, EM-DPOR selectively reorders posts to the same event queue even though the dependence relation used by EM-DPOR considers all the pairs of posts to be independent. When attempting to reorder a transition $r$ executed at a state $s$ and a dependent transition $r'$, if EM-DPOR fails to add backtracking choices at state $s$ then, EM-DPOR employs a recursive strategy to dynamically identify and re-order certain posts to the same event queue. As will be explained in Example 3.5, EM-DPOR requires the enforced ordering between such selectively reordered post operations to be captured. Hence, the happens-before relation that we use with EM-DPOR is defined to be a partial order on dependent transitions as well as selectively reordered posts.

3.2 Definitions

We now define (selectively) reordered posts and the happens-before relation used by our algorithm. We also define a few functions that will be used in the rest of the section, and a notion of diverging posts that will be used by EM-DPOR to reorder a pair of transitions from different event handlers on the same thread.

Reordered posts. We define a function reorderedPosts($p, w$) which takes a transition $p$ posting an event to a thread $t$’s event queue and a sequence $w$ explored by EM-DPOR where $p$ is executed in $w$, as input, and returns a set $P$ of transitions such that a transition $p'$ is a member of $P$ if the following conditions hold:

1. $p'$ posts an event to thread $t$’s event queue.
2. There exists a prefix $w_1$ of $w$ such that $w = w_1, w_2, w_3$ reaches a state $s$, $p$ is executed in $w_2$, and the following holds:

   (A) EM-DPOR has already explored a sequence $w_1, w_3$ where $w_3 = p.a_1 ... a_i.p'.a_{i+1} ... a_m$, each $a_i$ for $1 \leq i \leq m$ is a transition, and has added backtracking choices at state $s$ to reorder the posts transitions $p$ and $p'$, and

   (B) $p'$ is a transition in $w_2$ such that $index(w_2, p') < index(w_2, p)$.

Happens-before relation. In the concurrency model assumed, the events posted to the same event queue are handled in FIFO order. Hence, we extend the happens-before relation defined in [10] with a rule to reason about FIFO ordering and a rule to capture ordering between reordered posts.

Definition 3.1. For a transition sequence $w = r_1, r_2 ... r_n$ in $S_G$ explored by EM-DPOR, the happens-before relation $\rightarrow_w$ is the smallest relation on dom($w$) such that the following conditions hold:

1. If $i \leq j$ and $r_i$ is dependent with $r_j$ then $i \rightarrow_w j$.
2. If $r_i$ and $r_j$ are two different transitions posting events $e$ and $e'$ respectively to the same thread, such that $i \rightarrow_w e$ and the
helper function e has finished and that of e' has started in w, then getEnd(w,e) → w getBegin(w,e'). This is the FIFO rule.

3. If r_j is a post transition and r_i ∈ reorderedPosts(r_j,w) such that i = max{l | r_l ∈ reorderedPosts(r_j,w)} then i → w j.

4. → w is transiitively closed.

The relation → w is defined over transitions in w. We overload → w to relate transitions in w with those in the nextTrans set in the last state, say s, reached by w. For a task (t, e) having a transition in nextTrans(s), i → w (t, e) if either (a) task(r_i) = (t, e) or (b) 3k ∈ dom(w) such that i → w k and task(r_k) = (t, e).

We note that unlike the happens-before relation defined in [10], the happens-before relation defined above captures some information related to sequences rooted at states reached by prefixes of w explored by EM-DPOR prior to exploring w. This is required to add happens-before mapping between reordered posts.

**Diverging posts.** For a transition sequence w in S_{obs} reaching a state s and a transition r in w or nextTrans(s), let postChain(r,w) = p_{mw}, p_{mw-1}... p1 be the maximal sequence of post transitions in w such that p_{m-1} is a transition in the handler of the event posted by p_m for m ≥ i > 1, and p_i posts the event whose handler executes r. Let r and r' be transitions of two handlers running on the same thread such that postChain(r,w) = p_{m}... p1 and postChain(r',w) = q_{n}... q1. Then, divergingPosts(r, r', w) is a pair of posts (p_i, q_j) where i is the smallest index in the post-chains of r and r' in sequence w such that thread(p_i) ≠ thread(q_j). In Figure 3, divergingPosts(r_3, r_4, r_1... r_6) = (r_1, r_2). Diverging posts are undefined if there exists an index j such that task(p_j) = task(q_j) and for all i < j, thread(p_i) = thread(q_j).

The order of execution of diverging posts of r and r' uniquely determines the order of execution of r and r'. In Figure 3, the order of execution of r_1 and r_2 uniquely determines the order of execution of r_3 and r_4. If r and r' do not have diverging posts, their relative order of execution is fixed.

**Helper functions and data structures.** Function enabled(s) gives the set of threads whose next transitions are enabled at a state s. Consider a transition sequence w : r_1... r_m from the initial state s_{init} of a given event-driven multi-threaded program. The function last(w) gives the last state reached by w. If w is empty, it is the initial state. For an index k ∈ dom(w), pre(w,k) is the state before executing transition r_k. The function getPost(w, e) gives the transition in w which posted the event e. Function event(r) gives the event corresponding to the handler which executes r (this is nil if r is executed by a thread without an event query). For a thread t with an event query, the function executable(s,t) returns the event whose handler can perform the next transition on t in a state s, whereas blockedEvent(s,t) returns the set of events present in t's queue in state s that are not executable. We say that a task (t, e) is executable at a state s if t is a thread without a queue (e = nil), or e = executable(s,t). Function execTasks(s) returns the set of tasks whose events are executable in state s, whereas blockedTasks(s) returns the set of tasks whose events are blocked in state s. Function dest(r) takes a transition r posting an event as input and returns the destination thread. Data structures backtrack(s) and done(s) respectively track the threads added as backtracking choices at a state s, and the threads already explored from a state s during the DFS traversal. Another data structure the algorithm populates is the set RP maintained at every visited state. The set RP(s) corresponding to a state s is a set of ordered pairs of transitions where a pair (a, b) ∈ RP(s) is such that a and b are posts to the same thread such that a and b have been identified for reordering in an execution where a is executed prior to b. The set RP will be implicitly looked up to compute the set reorderedPosts of a post operation, and in turn derive happens-before ordering between posts as per condition 3 in Definition 3.1.

### 3.3 Overview of EM-DPOR Algorithm

This section describes the EM-DPOR algorithm to explore a dependence-covering state space (see Definition 2.8) of event-driven programs obeying the concurrency model described in Section 2.1.

The EM-DPOR algorithm has two components: (1) a depth first search based state space explorer called Explore, and (2) a recursive routine called FindTarget to compute backtracking points and choices for a pair of reorderable dependent transitions. We note that the algorithms presented in this section assume dependence even between transitions reading from the same shared variable, even though the dependence relation defined by Definition 2.2 considers such non-conflicting transitions to be independent. In Appendix C, we present modifications to the Algorithm Explore which makes EM-DPOR capable of treating such transitions including a few more types of transitions as independent. We now give an overview of Explore and FindTarget.

**Explore.** Algorithm Explore, given as Algorithm 1, takes a transition sequence w and a set rp of posts identified for reordering, as input and obtains the current state s = last(w) (line 1). Also, the set RP(s) corresponding to state s is initialized to rp. Initially, i.e., when Explore is invoked for the first time, w is empty. The loop at lines 2–6 iterates over all threads t and identifies transitions from w that have a race with next(s,t). A transition r_i has a race with next(s,t) if they are dependent and may be co-enabled (both thread(r_i) ≠ thread(r_j) or may be reordered (if event(r_i) and event(next(s,t)) may be reordered), and r_i does not happen before any transition in the task that executes next(s,t). The algorithm selects a transition r_i which satisfies the above requirements and has the highest index in w. It then invokes the recursive routine FindTarget at line 4 to compute backtracking choices to reorder r_i and next(s,t), and if required, identify posts to same thread for selective reordering.

Lines 7–19 perform a selective depth first traversal starting at state s reached by w. The algorithm Explore is called recursively by extending the current transition sequence with an outgoing transition r of a thread t ∈ backtrack(s) from s, such that t is not already explored from s i.e., t ∉ done(s). Lines 11–16 are effective only if the transition r executed at state s reached by w, is a post transition. Line 15 removes those members from the set RP(s) where the recently executed transition r is the first transition in the ordered pair. This is because after the execution of post operation r, any remaining post identified to be reordered w.r.t. r cannot be reordered by extensions of the sequence w.r. Hence, we do not track such pairs anymore. We now explain intuitions for lines 12 and 13 which add t’s thread as a backtracking choice at a state from where t’s nearest reordered post is executed.

On inspecting the members of the form (r, _) in the set RP(s) and checking the post transitions in w, the posts which have been successfully reordered w.r.t. the post transition r can be identified, i.e., reorderedPosts(r,w,r) can be computed with the help of RP. If the transition r = next(s,t) has a post operation such that a transition r_k in w is its nearest reordered post then, condition 3 in Definition 3.1 adds a happens-before mapping from r_k to r. The happens-before mapping from r_k to r initiates FIFO and transitive ordering between transitions across some of the handlers corresponding to post chains originating from r_k and r; consequently, dependent transitions which could otherwise be identified by line 3 for reordering may get ordered by happens-before.
Transition \( r \) is enabled in \( \text{pre}(w, k) \) — state from which \( r_k \) is executed, because \( r_k \in \text{reorderedPosts}(r, w, r) \) which means EM-DPOR has already seen an execution where \( r \) is executed from a state reached by a prefix of \( w \) but prior to or at \( \text{pre}(w, k) \) which makes \( r \) the next transition on its thread at \( \text{pre}(w, k) \) (see definition of reordered posts in Section 3.2). Hence, line 13 adds thread \( t \) as a backtracking choice at \( \text{pre}(w, k) \), so as to not miss alternate orderings between dependent transitions across post chains of \( r_k \) and \( r \). For example, consider a sequence \( w.r_1 ... r_1 ... p_1 ... p_2 ... p_n ... w' \) explored by EM-DPOR where \( w \) and \( w' \) are transition sequences, and \( p_i \) for \( 1 \leq i \leq n \) and \( r \) are transitions posting to the same event queue. Assume that the handlers of \( p_1 ... p_{n-1} \) and \( p_n \) contain transitions dependent with transitions in \( r \)'s handler, and EM-DPOR identifies \( p_1, p_2, ..., p_n \) to be reordered with \( r \). Let EM-DPOR eventually explore \( v = w ... p_1 ... p_n ... r.w' \). Since \( p_n \) is the nearest reordered post w.r.t. \( r \) in sequence \( v \), a happens-before mapping is added between \( p_n \) and \( r \). As a result the handlers corresponding to \( p_n \) and \( r \) get ordered by FIFO rule, due to which the dependent transitions in the handlers of \( p_n \) and \( r \) will not be selected for reordering by line 3 in Algorithm 1. Since line 13 adds \( r \)'s thread to the backtracking set at the state prior to \( p_n \) in sequence \( v \), EM-DPOR will still be able to explore a dependency-covering sequence for \( w ... p_1 ... p_{n-1} ... r ... p_n, w' \). This may be missed otherwise.

FindTarget. Explore invokes FindTarget (Algorithm 2) to compute backtracking choices to reorder a dependent transition \( r \) and \( r' \). Let \( i \) be the index of \( r \) in \( w \) and \( s \) be the state from which \( r = r_i \) is executed (line 1). If FindTarget fails to identify backtracking choices to be added to backtrack\((s)\), then it identifies posts for selective reordering and recursively invokes itself to compute corresponding backtracking choices. Among other criteria, a recursive call terminates when a happens-before ordering between \( r \) and \( r' \) is detected (line 2). Transitions \( r \) and \( r' \) may be co-enabled or they may belong to different event handlers on the same thread. In the latter case, we first identify a pair of post operations executed on different threads which need to be reordered so as to reorder \( r \) and \( r' \). FindTarget operates in four main steps explained below, of which Steps 2 - 4 are applicable only when \( \text{thread}(r) \neq \text{thread}(r') \) and Step 1 only when \( \text{thread}(r) = \text{thread}(r') \).

Step 1. Transitions \( r \) and \( r' \) may be from different tasks on the same thread. Such transitions can only be reordered by reordering their diverging posts. Line 4 therefore recursively invokes FindTarget on post operations of \( r \) and \( r' \). This way it simultaneously walks up postChain\((r, w)\) and postChain\((r', w)\) on each recursive call to FindTarget till it finds divergingPosts\((r, r', w)\). On reaching the diverging posts, the condition \( \text{thread}(r) = \text{thread}(r') \) — where \( r \) and \( r' \) are diverging posts — evaluates to false and the control goes to Step 2.

Step 2. This step is reached only when \( \text{thread}(r) \neq \text{thread}(r') \). Similar to the algorithm DPOR’s [10] computation of backtracking choices, this step computes threads to be added to backtrack\((s)\) to facilitate executing \( r' \) before \( r \) in a future run. Lines 6–10 compute a set candidates consisting of task\((r')\) and tasks that have a transition, executed after \( r \), with a happens-before ordering with \( r' \). Tasks in set candidates are restricted to only those which are either executable or blocked in state \( s \). Additionally, only those tasks whose threads are enabled at \( s \) are added, so that one such thread can be explored from \( s \) to eventually achieve the reordering.

Threads whose transitions are already explored from state \( s \) are added to done set at \( s \) by line 17 in Algorithm 1. For a task \( (t, e) \in \text{candidates} \), it is possible that its thread \( t \) is already in done\((s)\). If all the tasks in the set candidates are in done\((s)\) then in case of a purely multi-threaded program, this would imply that the intended order between \( r' \) and \( r \) has already been explored. However, this reasoning need not hold in the presence of events. This is because for a task \( (t, e) \in \text{candidates} \) such that \( t \in \text{done}(s) \), event \( e \) may be blocked on its queue in state \( s \) — which means \( t \in \text{done}(s) \) due to exploration of the executable task on \( t \) in a prior run. However, the executable task on \( t \) may not even have any happens-before ordering with \( r' \). In which case exploring it from state \( s \) would either not have explored the required order between \( r' \) and \( r \), or would not have preserved the required order between other pairs of dependent transitions when \( r' \) is executed before \( r \) in a prior run.

Hence, lines 12–16 compute unexplored to be a set of threads corresponding to tasks in candidates which are not in
Step 3. In this step, line 17 computes a set pending which is a subset of tasks in candidates whose events are blocked in their event queues in state s. If set pending is not empty, line 18 invokes ReschedulePending. Intuitively, ReschedulePending identifies a set of events blocked in s to be reordered with their corresponding executable events i.e., it performs selective reordering of posts to same thread so as to eventually reorder r and r′ executed on different threads. We present its details in Section 3.4.

3.4 Selective Reordering of Blocked and Executable Events

ReschedulePending (Algorithm 3) is invoked by Algorithm 2 on line 18 in Step 3 of FindTarget when a transition r executed from a state s in sequence w explored by EM-DPOR has already been reordered on different threads. A pair of event handlers executed on the same thread may have to be reordered so as to reorder a pair of events, say $r'$ and r that are already explored in a past run as all the threads in s are already in done(s) (due to lines 12–16), and the algorithm trivially adds any thread from ts to backtrack(s) (line 21). If ts = ∅ which means candidates = ∅, FindTarget invokes BacktrackEager (see Algorithm 4) at line 21.

Example 3.2. In sequence $w$ of Figure 3, transitions $r_3$ and $r_6$ are dependent, may be co-enabled and do not have a happens-before ordering. When Explore invokes FindTarget to compute backtracking choices to reorder $r_3$ and $r_6$, Step 1 is skipped as thread($r_3$) ≠ thread($r_6$). Step 2 computes candidates = {$(t_1, e_2)$} as $t_1$ is enabled at $s_2$ (see Figure 4), and $r_4$ executed in $(t_1, e_2)$ forks $t_4$ and thus happens before $r_6$. However, $t_5$ is already executed and $s_2$ and is in done($s_2$). Yet, as can be seen in Figure 4, $r_3$ and $r_6$ can be reordered; but by reordering $r_1$ and $r_2$ posting events $e_1$ and $e_2$ respectively. But adding thread $t_1$ corresponding to the only task $(t_1, e_2)$ in candidates will not achieve this reordering. Step 3 explains our technique to handle such cases.

Step 4. Finally, the set pending being empty implies that all the tasks in candidates are executable at state s or candidates itself is empty. FindTarget computes a set of threads ts corresponding to each task in candidates. If the set ts is non-empty, it only means that another ordering of r and r′ is already explored in a past run as all the threads in ts are already in done(s) (due to lines 12–16), and the algorithm trivially adds any thread from ts to backtrack(s) (line 21). If ts = ∅ which means candidates = ∅, FindTarget invokes BacktrackEager (see Algorithm 4) at line 21.

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### Algorithm 2: FindTarget

**Input:** a transition sequence $w$: $r_1, ..., r_n$, a transition $r$ from $w$ and a transition $r'$ which may or may not belong to $w$

1. Let $i = \text{index}(w, r)$ and $s = \text{pre}(w, i)$
2. If $r' \notin \text{nextTrans}(\text{last}(w))$ and $i \rightarrow_w \text{index}(w, r')$ then return // Step 1: Recursively search for diverging posts
3. If $\text{thread}(r) = \text{thread}(r')$ then
   4. $\text{FindTarget}(w, \text{getPost}(w, \text{event}(r)), \text{getPost}(w, \text{event}(r')));$ return
5. end
6. // Step 2: Reorder transitions from distinct threads
7. If $r' \in \text{nextTrans}(\text{last}(w))$ then
   8. Let candidates = \{task(p) ∈ execTasks(s) ∪ blockedTasks(s) | thread(p) ∈ enabled(s)
      and $p = r'$ or ($\exists k \in \text{dom}(w) : k > i$ and $k \rightarrow_w \text{task}(r')$ and $p = r_k$)\}
9. end
10. end
11. end
12. Let unexplored = \{t | (t, e) ∈ candidates\} \ done(s)
13. If unexplored ≠ ∅ then
14. Add any $t$ ∈ unexplored to backtrack(pre(w, i))
15. If $r'$ and r are post operations then $\text{RP}(s) = \text{RP}(s) \cup \{(r, r')\}$ return
16. end
17. // Step 3: Recursively search for backtracking choices to make a pending (blocked) event executable
18. If pending ≠ ∅ then $\text{ReschedulePending}(w, \text{pending}, r)$ // See Algorithm 3
19. else // Step 4: All the tasks in candidates are executable, or candidates = ∅
20. Let ts = \{t | (t, e) ∈ candidates\}
21. If ts ≠ ∅ then Add any $t$ ∈ ts to backtrack(pre(w, i)) else $\text{BacktrackEager}(w, i, r')$ // See Algorithm 4

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Input: a transition sequence $w$: $r_1, ..., r_n$, a transition $r$ from $w$ and a transition $r'$ which may or may not belong to $w$

1. Let $i = \text{index}(w, r)$ and $s = \text{pre}(w, i)$
2. If $r' \notin \text{nextTrans}(\text{last}(w))$ and $i \rightarrow_w \text{index}(w, r')$ then return // Step 1: Recursively search for diverging posts
3. If $\text{thread}(r) = \text{thread}(r')$ then
   4. $\text{FindTarget}(w, \text{getPost}(w, \text{event}(r)), \text{getPost}(w, \text{event}(r')));$ return
5. end
6. // Step 2: Reorder transitions from distinct threads
7. If $r' \in \text{nextTrans}(\text{last}(w))$ then
   8. Let candidates = \{task(p) ∈ execTasks(s) ∪ blockedTasks(s) | thread(p) ∈ enabled(s)
      and $p = r'$ or ($\exists k \in \text{dom}(w) : k > i$ and $k \rightarrow_w \text{task}(r')$ and $p = r_k$)\}
9. end
10. end
11. end
12. Let unexplored = \{t | (t, e) ∈ candidates\} \ done(s)
13. If unexplored ≠ ∅ then
14. Add any $t$ ∈ unexplored to backtrack(pre(w, i))
15. If $r'$ and r are post operations then $\text{RP}(s) = \text{RP}(s) \cup \{(r, r')\}$ return
16. end
17. // Step 3: Recursively search for backtracking choices to make a pending (blocked) event executable
18. If pending ≠ ∅ then $\text{ReschedulePending}(w, \text{pending}, r)$ // See Algorithm 3
19. else // Step 4: All the tasks in candidates are executable, or candidates = ∅
20. Let ts = \{t | (t, e) ∈ candidates\}
21. If ts ≠ ∅ then Add any $t$ ∈ ts to backtrack(pre(w, i)) else $\text{BacktrackEager}(w, i, r')$ // See Algorithm 4

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Algorithm 2: FindTarget
is in a task whose event is blocked in $p_1$’s thread in state $s$ (similar to the scenario presented for Figure 4).

(b) Any transition sequence rooted at state $s$ cannot preserve the relative ordering between two events. When reordering $p_1$ and $p_n$, even though this can be achieved by reordering some relevant pairs of events. This may be the case if a transition that happens before $p_1$ is in a task whose event is blocked in $p_1$’s thread in state $s$. In such a case executing $p_n$ prior to $p_1$ by adding backtracking choices at state $s$ breaks the ordering between transitions in the blocked task on $p_1$’s thread and $p_n$. More generally case (b) can occur if a transition in a task blocked on $p_1$’s thread in state $s$ happens before a transition in the executable task on another thread, say $t_s$, such that a transition in a task blocked in $s$ on $t_s$ happens before $p_1$.

In general there may be any number of such blocked – executable tasks between $p_1$ and $p_n$, with happens-before mapping from transitions in blocked tasks to transitions in executable tasks on different threads, as depicted in Figure 8(a). Clearly, reordering $p_1$ and $p_n$ by exploring thread $t_s$ (see Figure 8) from state $s$ breaks the happens-before ordering between a transition in a blocked task on thread $t_{s-1}$ and transition $p_n$ in the executable task on $t_s$.

**Figure 8:** Partial dependence structure of sequence $v$. Directed edges indicate dependence or relation by $\rightarrow_v$. Even though $p_n$ is indicated inside task $(t_s, e_n)$, it may only have a happens-before relation with a transition in $(t_s, e_n)$.

In both cases (a) and (b) it is intuitive to identify the event corresponding to the blocked task that happens before $p_1$ for reordering with its corresponding executable event. Also, this blocked task will be in set $\textit{candidates}$ computed by Step 2 of Algorithm 2 invoked to reorder $p_1$ and $p_n$ when exploring sequence $v$. From the structure given in Figure 8(a), reordering tasks $(t_s, e_n)$ and $(t_s, e_n')$ seems to reorder $p_1$ and $p_n$ without disturbing the happens-before ordering between any $p_i$ and $p_{i+1}$, for $1 \leq i < n$. Now assume tasks $(t_s, e_n)$ and $(t_s, e_n')$ to contain a pair of dependent transitions, say $q$ and $q'$, in which case reordering these tasks so as to reorder $p_1$ and $p_n$ breaks the ordering between $q$ and $q'$. In such a scenario reordering events $e_i - e_i'$ for some $1 \leq i \leq n - 1$, such that the corresponding tasks of these event pairs do not have dependent transitions, would aid in reordering $p_1$ and $p_n$ without affecting any other pairs of dependent transitions (see Figure 8(b)). However, identifying one right pair of events for reordering among various available relevant pairs of events is hard, as the dependent transitions that may be affected by the reordering of a pair of events may not even be present in the handlers of these events. Hence, we have designed EM-DPOR to reorder all the relevant pairs of events.

**Insights on reordering relevant event pairs.** In case of scenario presented for Figure 8(a) EM-DPOR eventually explores every thread $t_i$, for $1 \leq i \leq n$ from state $s$. This is because exploring any thread $t_i$ from $s$ eventually explores a sequence where the order between transitions $p_i$, $p_{i+1}$ and $p_n$ is reversed compared to what is required, while the remaining blocked to executable task happens-before mapping is as required. As a result FindTarget adds thread $t_{i+1}$ to backtrack$(s)$ eventually exploring it. Even after exploring every $t_i$, $1 \leq i \leq n$, from state $s$, one pair of transitions from executable and blocked tasks respectively on different threads are out of order. FindTarget invoked to reorder this pair finds threads corresponding to all tasks in $\textit{candidates}$ to be explored from $s$ resulting in a call to ReschedulePending. Then, ReschedulePending identifies relevant blocked – executable event pairs for reordering by checking for happens-before mapping from blocked tasks to executable tasks such that the threads corresponding to these tasks are already explored from $s$. The details of this process is explained below.

**Algorithm ReschedulePending.** Algorithm 3 takes a sequence $v$ explored by EM-DPOR, a set of tasks $\textit{pending}$ (same as $\textit{pending}$ computed by FindTarget), and a transition $r = r_i$ identified by FindTarget to be reordered with a transition $r'$ as input. Since ReschedulePending is invoked by the step 3 of FindTarget (Algorithm 2), we refer to the steps of ReschedulePending as 3a, 3b and 3c. In Algorithm 3, variable $\textit{worklist}$ stores a subset of executable tasks in state $s$ and $\textit{swapMap}$ maintains a map from threads to a subset of events blocked on their respective queues at $s$. Lines 2 and 3 in Step 3a pick any task $(t_s, e_k)$ from set $\textit{pending}$ passed as argument, initialize $\textit{worklist}$ with the executable task on thread $t_k$ and add $e_j$ to the set of blocked events maintained for thread $t_k$ in $\textit{swapMap}$. Step 3b (lines 4–11) initiated by a non-empty $\textit{worklist}$ identifies other relevant blocked events for reordering. This is required as it is hard to pick exactly one pair of relevant blocked – executable events for reordering, as explained earlier. Line 5 removes some executable task $(t_j, e_j)$ from the $\textit{worklist}$. Line 6 computes a set $C$ of tasks blocked in $s$ such that, a blocked task $(t, e)$ is added to $C$ if there exists a transition $t_i$ in the handler of $e$ which happens before a transition in $(t_j, e_j)$. This essentially checks for the blocked task on one thread to executable task on another thread happens-before pattern, illustrated through Figure 8. Additionally, line 6 only retains those blocked tasks whose threads are already explored from state $s$. Lines 7–10 iterate on each blocked task in $C$, add corresponding executable task to $\textit{worklist}$ for further processing and store the event corresponding to blocked task in $\textit{swapMap}$. We note that in case of scenario presented for sequence $v$ in Figure 8, if $t_n \in \textit{done}(s)$ then, FindTarget called to reorder dependent transitions $p_1$ and $p_n$ reach Step 3, compute $\textit{pending} = \{(t_n, e_n')\}$ and invoke ReschedulePending. Step 3a of Algorithm 3 adds event $e_n'$ corresponding to a pending task $(t_n, e_n')$ to the set $\textit{swapMap}[t_n]$ and initializes $\textit{worklist}$ with the executable task $(t_n, e_n)$. Initiated by the executable task $(t_n, e_n)$, Step 3b iteratively adds $e_i'$ to $\textit{swapMap}[t_i]$ and $(t_i, e_i)$ to $\textit{worklist}$ starting from $i = n - 1$ to $i = 1$. The while loop exits on processing executable task $(t_1, e_1)$ and not finding any more blocked events satisfying the constraints in line 6.

Lines 12–16 (Step 3c) iterate over each thread $t$ for which the set of blocked events $\textit{swapMap}[t]$ is non-empty, pick an event among events in set $\textit{swapMap}[t]$ and invoke FindTarget to reorder the post transition for the executable event at state $s$ on thread $t$ with that of the selected blocked event.

**Example 3.3.** Continuing Example 3.2, Step 2 in FindTarget called to reorder $t_3$ and $t_6$ (Figure 3) fails to add any backtracking choices at state $s_2$ (Figure 4). Then, Step 3 computes...
pending = \{(t_1, e_2)\} as e_2 is blocked in s_2, and invokes ReschedulePending(r_1 \ldots r_5, \{(t_1, e_2)\}, \{\})—Algorithm 3 adds e_2 to swapMap[t_1]. Step 3b adds no more blocked events to swapMap. Step 3c calls FindTarget(r_1 \ldots r_5, r_1, r_2) to reorder blocked event e_2 with executable event e_1 at state s_2 on t_1. In the recursive call, state s_0 (where r_1 is executed) is identified as the backtracking point and Step 2 adds thread t_3 to backtrack(s_0) as t_3 executes r_2. Thus in a future run where t_2 is explored before r_1, r_3 and r_6 are reordered as shown in Figure 4.

3.5 Simulating DPOR

Call to BacktrackEager(w, i, r') is performed by line 21 in Algorithm 2 when Steps 2 and 3 of Algorithm 2 fail to identify backtracking choices to reorder transitions r (same as r_i) executed at state s and a transition r'. When the DPOR algorithm fails to identify candidate threads using the HB relation so as to reorder a pair of racing transitions in the multi-threaded setting, it includes all the threads enabled at s as backtracking choices, initiating exploration of all thread interleavings rooted at s. In our event-driven setting, in addition, EM-DPOR must initiate all possible reordering of events in each queue which are posted prior to reaching state s. BacktrackEager (Algorithm 4) achieves the same.

It initializes a temporary HB relation \(\sim\) which will only be used in the current invocation of BacktrackEager, with the HB ordered pairs in the relation \(\rightarrow_w\). Given a transition sequence \(w\), an index \(i\) and a transition \(r'\), BacktrackEager treats every nearest pair \((r_j, r_k)\) of transitions with no happens-before between them as per \(\sim\), and posting to the same event queue as \(\text{dependent}\), provided \(j, k < i\) (Algorithm 4 line 4). We consider \(r_j\) to be nearest to \(r_k\) if \(j < k\) and \(r_j\) has the highest index in \(w\) among all other transitions satisfying the given constraints. BacktrackEager then simulates the DPOR approach with this dependence relation from the initial state along \(w\) up to \(r_i\). Note that dependence through shared objects is already considered in Algorithm 1. Lines 5–8 add backtracking choices at state \(\text{pre}(w, j)\) to reorder \(r_j\) and \(r_k\), and mark \(r_j\) to happen before \(r_k\). The new happens-before mapping added to \(\sim\) induces additional transitive and FIFO mappings to be added to \(\sim\) (see line 8 in Algorithm 4). Hence, we call \(\sim\) as the extended HB relation. If \(r_i\) is established to happens before \(r'\) as per \(\sim\), then BacktrackEager returns (line 9), because \(r_i\) and \(r'\) have got related by happens-before by considering a pair of post operations \((r_j, r_k)\) as dependent. Thus, \(r_i\) and \(r'\) will get reordered when \(r_j\) and \(r_k\) get reordered on exploring backtracking choices added by line 6. Otherwise, the algorithm iterates until \(r_i\) is reached, and computes backtracking choices to reorder \(r_j\) and \(r'\) similar to DPOR (lines 12–19) using the extended HB relation \(\sim\). Lines 7 and 20 update the \(\text{RP}\) sets of different states since the \(\text{post}\) transitions executed from these states were identified to be reordered w.r.t. \(\text{posts}\) executed later. As explained earlier \(\text{RP}\) sets will be queried to identify the set of \(\text{reorderedPosts}\) in subsequent explorations. Below is an example illustrating the working of BacktrackEager.

Example 3.4. For the purpose of this example, consider an implementation of EM-DPOR which does not track happens-before ordering between a fork operation and the initialization of the spawned thread. Assume exploring a sequence \(w\) given in Figure 3 with such an implementation of EM-DPOR. On reaching state \(s_0\) (see Figure 4) Explore invokes FindTarget to reorder dependent transitions \(r_3\) and \(r_6\). As thread \(t_4\) executing \(r_6\) is not enabled at \(s_2\) and missing happens-before mapping between \(r_4\) and \(r_5\) causes candidates computed on line 7 of Algorithm 2 to be an empty set. Setting is also empty as it is a subset of candidates. This causes the control flow of FindTarget to reach Step 4 invoking BacktrackEager(r_1 \ldots r_5, r_6). Then, lines 4–6 in Algorithm 4 pick transitions \(r_1\) and \(r_2\) posting events to the same event queue, as the nearest co-enabled \(\text{posts}\) not ordered by \(\sim\), and add \(t_3\) executing \(r_2\) to backtrack(s_0). This is because \(r_3\) is explored at \(s_0\) in \(w\). On backtracking to \(s_0\), EM-DPOR explores a run where events \(e_1\) and \(e_2\) are reordered which eventually reorders \(r_3\) and \(r_6\) as shown in Figure 4.

3.6 Role of HB Order Induced Between post Transitions

We now give another example to illustrate the end-to-end working of EM-DPOR along with highlighting the role played by happens-before mappings added between reordered post operations by rule 3 in Definition 3.1.

Example 3.5. Consider an execution trace \(z\) shown in Figure 9, of a program in which two threads \(t_1\) and \(t_2\) have event queues.
Transitions $r_1$ and $r_2$ respectively post events $e_1$ and $e_2$ to the event queue of the thread $t_1$, and the transitions $r_3$ and $r_4$ respectively post events $e_3$ and $e_4$ to the event queue of the thread $t_2$. Transitions $r_5$ and $r_9$ post events $e_5$ and $e_6$ respectively to the same event queue. However, the event handlers corresponding to $e_5$ and $e_6$ are not shown in the figure. We assume that the event handlers of $e_3$ and $e_4$ contain dependent transitions. Figure 10 shows a partial state space explored by various permutations of transitions in $z$. For economy of space, we merge prefixes of certain transition sequences and represent them by single edges. Event queue state of threads $t_1$ and $t_2$ are indicated for some of the states reached on executing the post operations in various orders. The events in an event queue are ordered from left to right, which makes the leftmost event the front of the queue. The sequences of interest are labeled as $z, z_1, z_2$ and $z_3$ in Figure 10. The shaded states correspond to states explored by $z$. Sequence $z$ has two pairs of may be co-enabled dependent transitions — $(r_8, r_{10})$ and $(r_9, r_{11})$, and a pair of may be reordered dependent transitions in the handlers of $e_5$ and $e_6$. Assume that EM-DPOR initially explores sequence $z_1$ in which the relative order of events $e_3$ and $e_4$ is reversed compared to that in $z$. We show how EM-DPOR eventually explores a dependence-covering sequence of $z$, rather $z$ itself, when the model checking starts with $z_1$. A dependence-covering sequence of $z$ must maintain
the relative ordering of all pairs of dependent transitions in $z$ (see Definition 2.4). Clearly, $z_1$ is not a dependence-covering sequence of $z$ as the relative order of dependent transitions in the event handlers of $e_5$ and $e_6$ posted respectively by the transitions $r_6$ and $r_5$ is reversed w.r.t. that in $z$. We will be showing the pair of dependent transitions or post transitions in a transition sequence $z_1$, whose order is problematic for $z_1$ to be a dependence-covering sequence of $z$, in an enlarged form.

When exploring $z_1$, Algorithm 1 invokes $\text{FindTarget}$ (Algorithm 2) to compute backtracking choices to reorder dependent transitions in the handlers of $e_6$ and $e_5$ (not shown in Figure 10). Step 1 of $\text{FindTarget}$ identifies $r_6$ and $r_7$ as corresponding diverging posts and recursively invokes $\text{FindTarget}$ to reorder $r_6$ and $r_7$. In the recursive call, Step 2 of $\text{FindTarget}$ adds thread $t_2$ to $\text{backtrack}(\sigma_7)$ since $r_6$ is executed from state $\sigma_7$, and EM-DPOR eventually explores a sequence $z_2$. Since $z_3 \in \text{reorderedPosts}(r_6, z_2)$, $r_6$ and $r_5$ are related by $\rightarrow_{s_2}$. Again, $z_2$ is not a dependence-covering sequence of $z$ as the relative order of dependent transitions $r_9$ and $r_{11}$ is reversed compared to that in $z$. On exploring a prefix of $z_2$ till state $s_{17}$ where $r_9 = \text{next}(s_{17}, t_1)$, $\text{FindTarget}$ is invoked to reorder $r_{11}$ and $r_9$. Step 2 of $\text{FindTarget}$ computes $\text{candidates} = \{(t_1, e_2)\}$. Since $t_1$ is in $\text{done}(s_2)$ due to sequence $z_1$, Step 3 of $\text{FindTarget}$ is reached which computes $\text{pending} = \{(t_1, e_2)\}$. Then, $\text{ReschedulePending}$ is invoked by line 18 of $\text{FindTarget}$ to reorder relevant blocked events with executable events at state $s_7$. Event $e_2$ is added to $\text{swapMap}[t_1]$ and $(t_1, e_1)$ to $\text{worklist}$ (line 3 in Algorithm $\text{ReschedulePending}$). On processing $(t_1, e_1)$ in $\text{worklist}$, Step 3(b) of $\text{ReschedulePending}$ adds blocked event $e_3$ to $\text{swapMap}[t_2]$ and $(t_2, e_2)$ to $\text{worklist}$, as $r_6$ in the task $(t_2, e_2)$ blocked at state $s_7$ happens before $r_6$ in the task $(t_1, e_1)$ executable at state $s_7$, and $t_2 \in \text{done}(s_7)$. No task is added to $\text{worklist}$ on processing $(t_2, e_2)$. Then, Step 3c invokes $\text{FindTarget}$ to reorder posts of events $e_1$ and $e_2$ and posts of $e_4$ and $e_3$. Reordering $e_1$ and $e_2$ allows us to explore $z$ — our target sequence.

As mentioned earlier, arbitrarily selecting a blocked event for reordering w.r.t. an executable event, among the set of blocked events identified by Steps 3a - 3b of $\text{ReschedulePending}$ may not yield a dependence-covering sequence for a target sequence. For example, any sequence explored after reordering events $e_1$ and $e_2$ reverses the order of dependent transitions $r_9$ (executed by the thread $t_6$) and $r_{10}$ (executed by the handler of $e_2$ on $t_1$) as shown in sequence $z_3$, making such sequences non dependence-covering w.r.t. $z$. This example also demonstrated the necessity to capture the ordering in reordered posts. The happens-before mapping from $r_5$ to $r_6$ helped in identifying event $e_3$ as a relevant blocked event to be reordered with its corresponding executable event $e_4$, leading to the exploration of a dependence-covering sequence of $z$.

3.7 Formal Guarantees and Variants of EM-DPOR

in Appendix B we provide a sketch outlining the proof of correctness of EM-DPOR. Through this proof sketch we show that whenever $\text{Explore}$ backtracks from a state $s$ to a prior state in the search stack, it must have explored a dependence-covering sequence (see Definition 2.4) for any sequence $w$ in $\mathcal{S}_C$ from state $s$. This equivalently proves that EM-DPOR explores a dependence-covering set at each visited state $s$.

Appendix C discusses a few variants of the Algorithm $\text{Explore}$ capable of identifying more pairs of independent transitions than assumed in this section (see the beginning of Section 3.3). We have incorporated these optimizations in our EM-DPOR implementation used for experimental evaluation of EM-DPOR.

4. Implementation

This section describes a vector clock based implementation of EM-DPOR on a prototype stateless model checking framework called EM-Explorer. Since we evaluate EM-DPOR over Android application traces, EM-Explorer has been designed to handle the concurrency behavior of Android applications.

Vector Clock Based Implementation of EM-DPOR

Happens-before relation (see Definition 3.1) over a given transition sequence which in turn captures the order between dependent transitions in the sequence, plays a vital role in various steps of EM-DPOR such as identifying unordered dependent operations to be reordered, computing backtracking choices and so on. We use vector clocks data structure to compute the happens-before relation. We have designed the implementation of EM-DPOR similar to the implementation of the DPOR [10] algorithm which too uses vector clocks to capture the HB relation over traces of multi-threaded programs to dynamically computes persistent sets [12]. In a multi-threaded setting where all the operations executed on the same thread are totally ordered, each component (or clock) of a vector clock corresponds to a thread. Hence, the vector clock timestamp of an operation $z$ denotes the last known operation (as known by $z$) performed by each thread of the program. In an event-driven program, the operations from different event handlers on the same thread need not be totally ordered. Hence in the vector clocks we use, each clock corresponds to a task in the program where a task is either an event or a thread. In order to compute the vector clock timestamps of operations of a task, we maintain a vector clock with each task. Most of the computations on vector clocks described in [10] are lifted in a straightforward manner to task-based vector clocks. As defined by rule (2) of Definition 3.1, EM-DPOR orders events executed on the same thread if their corresponding posts have a happens-before ordering, so as to respect the FIFO ordering of events. FIFO ordering is specific to the event-driven concurrency model considered in this work and is not handled by the vector clock based implementation of DPOR. The treatment of FIFO closure requires a special design explained below.

Computing FIFO closure. Initially all the components (scalar clocks) of the vector clocks of all the tasks are initialized to zero. Let $V_1$ be the vector clock of a task in which the transition with visible operation $\text{post}(e, t)$ is executed. Let $V_2$ be the vector clock of the task $(t, e)$. On executing $\text{post}(e, t)$, the component $(t, e)$ in the vector clock $V_1$, i.e., $V_1((t, e))$, is incremented making this component of $V_2$ non-zero, and the vector clock $V_2$ of task $(t, e)$ is initialized with the same value as that of $V_1$. After initialization $V_2$ remains unmodified till event $e$ is dequeued. When dequeuing event $e$ we check the value of each component corresponding to events posted to the thread $t$, in vector clock $V_2$. If the value of any such component of $V_2$, say $(t', e')$, is non-zero, we update $V_2$ by performing a vector clock join between $V_2$ and the vector clock of the task $(t, e')$. A non-zero component value for a task $(t, e')$ in $(t', e')$’s vector clock $V_2$ indicates that $\text{post}(e', t)$ happens-before $\text{post}(e, t)$, and thus FIFO rule in Definition 3.1 is applicable. Since the event $e'$ is handled prior to $e$ on the thread $t$, the vector clock of $(t, e')$ has a value corresponding to the VC timestamp of $\text{end}(t, e')$ when it is used to update $V_2$. Thus the event handler of $e$ gets ordered w.r.t. that of $e'$.

EM-Explorer Framework

The order of execution of operations in an Android application is influenced not only by the sources of non-determinism in the application, but also by the Android framework and the inter-process communication between the applications running in different processes on an Android device. Interpreting or modeling various con-
currency relevant APIs and operations from application/framework code, makes building a full fledged model checker for Android applications a challenge in itself. Tools such as JPF-Android [38] and AsyncDroid [27] take promising steps in this direction. However, presently they either explore only a limited number of sources of non-determinism [27] or require a lot of framework libraries to be modeled [37, 38]. We have therefore built a prototype exploration framework called EM-Explorer, which emulates the semantics of visible operations like post, read, acquire and so on.

Our framework takes an execution trace generated by an automated testing and race detection tool for Android applications, called DroidRacer [20], as input. Since DroidRacer has the capability to run on real-world applications, we can experiment on real concurrency behaviors seen in Android applications and evaluate different POR techniques on them. DroidRacer records all concurrency relevant operations and memory reads and writes. EM-Explorer emulates such a trace based on their operational semantics and explores all interleavings of the given execution trace permitted by the semantics. Android permits user and system-generated events apart from programmatically generated events by the application. EM-Explorer only explores the non-determinism between program and system generated events while keeping the order of user events fixed. This is analogous to model checking w.r.t. a fixed data input. EM-Explorer does not track variable values and is incapable of evaluating conditionals on a different interleaving of the trace. EM-Explorer is a stateless model checker, i.e., it does not store program states which can be restored when backtracking to a state. Hence, backtracking is performed by re-executing the prefix of the last explored sequence up to the backtracking point.

Android supports different types of component classes, e.g., Activity class for user interface, and enforces a happens-before ordering between handlers of lifecycle events of component classes. EM-Explorer seeds the happens-before relation for such events in each trace before starting the model checking, to avoid exploring invalid interleavings of lifecycle events. Android applications may post events in different modes such as associating a delay with an event or posting an event to the front of the queue. We over-approximate the effect of posting with delay by forking a new thread which does the post non-deterministically, as mentioned in Section 2.1. We leave handling of other variants of posting events as future work.

We subject the execution trace generated by DroidRacer to post-processing. Specifically, we recursively remove empty event handlers (event handlers which only execute deq and end with either no other visible operations in between or only posting events whose event handlers are empty) from the traces obtained from DroidRacer before model checking. This is done to facilitate fair comparison with DPOR which does not inspect the contents of the handlers before reordering events. DPOR would otherwise unnecessarily reorder even such events.

5. Experimental Evaluation

We evaluate the performance of EM-DPOR which computes dependence-covering sets, by comparing with DPOR [10] which computes persistent sets. DPOR is designed to use a dependence relation in which transitions with operations posting to the same event queue are considered dependent. Whereas, EM-DPOR uses the dependence relation given in Definition 2.2. Both the algorithms are implemented in the EM-Explorer framework described in Section 4 and evaluated on post-processed execution traces of Android applications obtained by running DroidRacer.

We evaluated these two POR techniques on execution traces generated by DroidRacer on 5 Android applications obtained from the Google Play Store [1]. Table 1 presents statistics like the number of visible operations in the trace (which is same as the count of concurrency relevant operations logged by DroidRacer), threads, events, threads with event loops and (shared) memory locations in the collected execution trace of each of these applications. We only report the threads created by the application, and the number of events excluding events with empty event handlers.

We analyzed each of the traces described in Table 1 using both the POR techniques. Table 2 gives the number of interleavings (listed as “Traces”) and distinct transitions explored by DPOR and EM-DPOR. It also gives the time taken for exploring the reduced state space for each execution trace. If a model checking run did not terminate within 4 hours, we force-kill it and report the statistics for 4 hours. The statistics for force-kill run are marked with * in Table 2. Since EM-DPOR does not track variable values, it cannot prune executions that are infeasible due to conditional sequential execution. However, both DPOR and EM-DPOR are implemented on top of EM-Explorer and therefore operate on the same set of interleavings. The difference in their performance thus arises from the different POR strategies.

In our experiments, DPOR’s model checking run terminated only on two execution traces among the five, whereas, EM-DPOR terminated on all of them. Except for the execution trace from My Tracks application, EM-DPOR finished state space exploration within a few seconds. As can be seen from Table 2, DPOR explores a much larger number of interleavings and transitions, often orders of magnitude larger compared to EM-DPOR. While this is a small evaluation, it does show that significant reduction can be achieved for real-world multi-threaded event-driven programs by avoiding unnecessary reordering of events.

Performance. Both the techniques used about the same memory and the maximum peak memory consumed by EM-DPOR across all traces, as reported by Valgrind, was less than 50MB. The experiments were performed on a machine with Intel Core i5 3.2GHz CPU with 4GB RAM, and running Ubuntu 12.04 OS.

6. Related Work

Exploring all possible interleaving of transitions executed by threads (or processes) is one of the causes of state explosion problem faced by state space exploration based verification techniques. Partial order reductions consisting of techniques like stubborn sets, persistent sets and sleep sets [11, 36] alleviate this problem by trying to explore only a representative interleaving of each Mazurkiewicz trace [21] (an equivalence class on thread interleavings). Traces are partial orders of a dependency relation [11, 18] over transitions which classifies a pair of non-interfering transitions as independent. A POR enabled state space explorer only orders dependent transitions, and this has been proved to visit all deadlocks and safety violations present in the original non-reduced space of thread interleavings [11]. Practically, dependent transitions are identified based on the operations performed on communication objects like shared memory, FIFO buffers and so on. Dynamic partial order reduction (DPOR) [10] is an algorithm to compute persistent sets by checking for dependences during runtime, thus improving the precision of the persistent sets computed and resulting in greater reductions in state space explored, while the older techniques [12] inspect static program structures.

A few works [7, 25] in the past have combined POR with bounded exploration [9, 24] of the state space. Coons et al. [6, 7] have extended persistent sets to account for various bound func-

| Application       | Trace length | Threads | Events | Memory locations |
|-------------------|--------------|---------|--------|------------------|
| Remind Me         | 414          | 4       | 9      | 90               |
| My Tracks         | 465          | 6       | 24     | 68               |
| Music Player      | 465          | 4       | 22     | 40               |
| Character Recogni| 600          | 5       | 30     | 30               |
| Aard Dictionary   |              |         |        |                  |
tions such as context bounding and preemption bounding, and have soundly combined the DPOR algorithm with various search bounding techniques. They achieve this by conservatively identifying more backtracking points where backtracking choices computed to reorder a pair of dependent transitions can be added than the default one computed by DPOR, so that a partial order between transitions which could be explored within the bound is not missed. Their algorithm which performs bounded POR dynamically is integrated with the CHESS [26] model checker.

Recent algorithms guarantee optimality in POR [2, 30], i.e., they explore exactly one transition sequence per Mazurkiewicz trace [21]. Whereas prior POR techniques guarantee exploring at least one member from each equivalence class of execution traces and provided no such optimality guarantees. Abdulla et al. [2] have devised an optimal DPOR technique based on a novel backtracking set called source set and a data structure called wakeup tree. However, the notion of source sets and the optimal DPOR algorithm assume total ordering between transitions executed on the same thread. Hence, integrating our new dependence relation with source sets will involve significant changes to the definitions and algorithms presented in [2]. Rodríguez et al. [30] describe unfolding semantics parametrized on the commutativity based classical independence relation [11], and present an unfolding based optimal POR algorithm. The unfolding semantics identifies dependent transitions with no ordering relation between them to be in conflict. Their POR algorithm backtracks and explores a new transition sequence \( w \) from a state \( s \) only if every prior transition explored from \( s \) is in conflict with some transition in \( w \). This is problematic in our setting where posts are considered independent and hence trivially non-conflicting, causing unfolding based POR to miss reordering posts when required. Establishing optimality in our setting is an interesting but non-trivial future direction.

Huang [14] has developed a state space reduction technique for multi-threaded programs based on a notion called maximal causality [15, 33], where an explored thread interleaving is guaranteed to have an operation that reads a value different from all the prior interleavings. Whereas Mazurkiewicz trace based conventional POR techniques explore different thread interleaving so as to explore different partial order of dependent transitions without any constraints on the values observed. Hence, exploration based on maximal causality are capable of reducing the number of equivalence classes over execution traces even further, compared to Mazurkiewicz trace based equivalence. Unlike dynamic POR based techniques which explore the thread interleavings using depth-first search of the state space, this technique identifies the interleavings by starting from a seed interleaving and generate other interleavings by encoding the interleaving and the allowed variations as a quantifier-free first-order logic formula. Solving the constraints of the generated formula using an SMT solver identifies an interleaving from another equivalence class. While the number of explorations by maximal causality based reduction technique can be much smaller, the constraint solving may be time consuming. However this technique is shown to be parallelized where multiple interleavings are explored in parallel, and the constraint solving corresponding to various interleavings can also be carried out in parallel.

Sen and Agha [31] and Tasharofi et al. [34] describe dynamic POR techniques for distributed programs with actor semantics where actors execute concurrently. Actors do not have shared memory and communicate only via asynchronous message exchanges. Both the POR techniques for the actor model explore all possible interleavings of messages sent to the same process. Sen and Agha [31] present a way of combining concolic execution [32] with partial order reduction in the context of actor based systems, thus being able to reason about various data input as well as thread interleavings. The dynamic partial order reduction technique outlined in [31] is adapted in a tool called Basset [19] which is a model checker for actor programs built on top of Java PathFinder [40]. Tasharofi et al. [34] identify the dependence relation defined in the context of actor programs to be transitive, which is not the case for dependence relation over transitions of multi-threaded programs. The authors have adapted the DPOR algorithm [10] given for multi-threaded programs to be sensitive to this transitive dependence relation, causing it to explore fewer transitions than a naive adaptation of DPOR for actor programs. Reduction techniques and model checking algorithms for MPI programs are described in [28, 35]. MPI programs too use message-passing constructs like non-blocking send and receive to exchange data between processes, and use global synchronization constructs like barriers. However, the message processing semantics of actor programs and MPI programs are quite different compared to the event handling semantics of event-driven programs such as Android applications. \( R^4 \) [17] is a stateless model checker for event-driven programs such as client-side web applications. \( R^4 \) adapts persistent sets [12] and the DPOR algorithm to the domain of single-threaded event-driven programs where enqueued events are non-deterministically dequeued in any order and each event handler is atomically executed to completion without interference from other handlers. As described in [17], the concurrency model handled by \( R^4 \) allows an entire event handler to be considered as a single transition. In contrast, the focus of our POR technique is on multi-threaded programs with event queues, and thus needs to be sensitive to interference from multiple threads. Mirzaei et al. [23] and Merwe et al. [39] model Android libraries and extend Java PathFinder [40] to model check Android applications. However, these works do not model various concurrency aspects of Android present in real-world applications. AsyncDroid [27] is a systematic concurrency testing tool for Android applications which explores various thread schedules for a given sequence of UI events.

While most of the state space reduction techniques in the literature assume the target programs to be run under a sequentially consistent (SC) memory model, recently, many efficient stateless model checking techniques have been developed for weaker memory models as well [3, 4, 8, 16, 41]. The challenges faced when developing efficient exploration techniques for event-driven programs are orthogonal to those faced when handling different memory models.

| Application       | Traces | Transitions | Time | Traces | Transitions | Time |
|-------------------|--------|-------------|------|--------|-------------|------|
| Remind Me         | 24     | 1964        | 0.18s| 3      | 875         | 0.06s|
| My Tracks         | 1610684 | 1132999029 | 4h*  | 405013 | 26745327    | 101m  |
| Music Player      | 1508413 | 93254810    | 4h*  | 266    | 343333      | 4.15s|
| Character Recognition | 1284788 | 670625250 | 199m  | 756    | 394222      | 6.58s|
| Aard Dictionary   | 359961 | 14397143    | 4h*  | 14     | 4772        | 1.4s  |

7. Conclusions and Future Work

The event-driven multi-threaded style of programming concurrent applications is becoming increasingly popular. We considered the problem of POR-based efficient stateless model checking for this concurrency model. The key insight of our work is that more reduction is achievable by treating operations that post events to the same thread as independent and only reordering them if necessary.
Towards this, we presented new formulations of dependence-covering sequences and sets such that exploring only dependence-covering sets suffices to provide certain formal guarantees. We also presented EM-DPOR—a dynamic algorithm to perform POR by computing dependence-covering sets for event-driven multi-threaded programs. Our experiments provide empirical evidence that EM-DPOR explores orders of magnitude fewer transitions compared to DPOR for event-driven multi-threaded programs.

In future, we plan to develop further optimizations and a practical tool to model check these programs. Also, we aim to achieve better reductions by defining a notion of sleep sets suitable for this concurrency model and combining it with dependence-covering sets. Another non-trivial but interesting problem would be to establish optimality in our event-driven setting on the similar lines as [2, 30]. A few other directions are to extend [14] to develop maximal causality based state space exploration technique for event-driven programs, and to explore bounded POR for event-driven programs.

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In the following discussion, let \( w \) be a transition sequence from a state \( s \in S_G \) to reach a deadlock cycle \( (DC, \rho) \). Let \( u \) be a dependence-covering sequence (see Definition 2.4) of \( w \) starting from \( s \). Further, \( R_u \) and \( R_w \) be the sets of transitions executed in \( w \) and \( u \) respectively, and \( s_u \) and \( s_w \) be the last states reached by \( u \) and \( w \) respectively.

**Lemma A.1.** Let \( s_1 \) be a state reached by a prefix of \( w \) where a transition \( b \in DC \) is blocked and not enabled later in \( w \). Then, there exists a prefix of \( u \) which reaches a state \( s'_2 \) where \( b \) is blocked and not enabled later in \( u \).

**Proof.** Let \( R_0 \subseteq R_w \) denote the transitions which have a direct dependence with \( b \) or a dependence with some other transition which directly or transitively has a dependence with \( b \). Clearly, all the transitions in \( R_b \) are executed prior to \( b \) since the transition \( b \) is blocked by a prefix of \( w \) and never enabled as per the premise of the lemma. By the definition of dependence-covering sequence (see Definition 2.4), \( R_w \subseteq R_u \) and hence, \( R_b \subseteq R_u \). Further, the relative ordering of dependent transitions in \( R_b \) is maintained in \( u \). Let \( s'_1 \) be the state reached after executing all transitions in \( R_b \) in \( u \). Since \( b \in \text{nextTrans}(s_u) \), there can be a transition \( r'_k \in u \) such that \( r'_k \not\in R_w \) and \( r'_k \) is dependent with \( b \), in particular, \( r'_k \) enables \( b \). Since \( w \) is a dependence-covering sequence of \( w \) starting from \( s \), \( r'_k \) exists only if \( w \) can be extended so that \( r'_k \) executes before \( b \). By the definition of deadlock cycle, this is not possible. Hence, the transition \( b \) will be blocked at \( s'_2 \) and there is no transition in \( u \) which enables \( b \) after \( s'_2 \). 

**Lemma A.2.** The pair \( (DC, \rho) \) is a deadlock cycle at the state \( s'_m \) reached by \( u \).
Proof. By Lemma A.1, for any \( b \in DC \), there exists a state \( s'_i \) reachable from \( s \) by some prefix of \( u \) such that \( b \) is blocked at \( s'_i \) and not enabled later in \( u \). Thus, all the transitions in \( DC \) are blocked at \( s'_i \).

Let \( DC \) contain \( k \) transitions and \( b = \rho(a) \) for some \( a \in [1,k] \). Let \( t \) be the thread blocked on the transition \( b' = \rho(a+1) \) at \( s_n \) where \( k+1 \) is taken to be 1. In \( u \), let \( r_i \) be the transition of \( t \) that blocks \( b \) after which it is never enabled. Clearly, \( r_i \in R_b \) for the set \( R_b \) defined in the proof of Lemma A.1. Since the state \( s'_i \) is reached in \( u \) once all the transitions in \( R_b \) are executed and in the same relative order between themselves, \( r_i \) blocks \( b \) before or at \( s'_i \) in \( u \). Since \( b \) remains blocked from \( s'_i \) onwards (Lemma A.1), there is no other transition in \( u \) that can enable \( b \). By Lemma A.1, the thread \( t \) itself subsequently blocks on \( b' \in DC \) in \( u \). Thus, \( (DC,\rho) \) is also a deadlock cycle at \( s'_i \).

Theorem 2.9.1. [Part of Theorem 2.9] Let \( S_R \) be a dependence-covering state space of a program \( A \) with a finite and acyclic state space \( S_G \). Then, all deadlock cycles in \( S_G \) are reachable in \( S_R \).

Proof. Let \( (DC,\rho) \) be a deadlock cycle at a state \( d \in S_G \), reachable from \( s_{init} \). Let \( s \) be a state which is common to both \( S_G \) and \( S_R \) such that there exists a transition sequence \( w \) from \( s \) to \( d \) in \( S_G \). In the least, the initial state \( s_{init} \) is such a state.

Let \( L \) be a dependence-covering set at \( s \). By definition (see Definition 2.6), there exists a transition sequence \( u \) from \( s \), starting with a transition \( r \in L \) such that \( u \) is a dependence-covering sequence of \( w \) with \( \rho(a) \). Let \( u \) eventually reaches the deadlock cycle \( (DC,\rho) \). Let \( s' = r(s) \). Since \( r \in L, s' \) is in \( S_R \). If \( u \equiv r \cdot u' \) then \( u' \) is a transition sequence from \( s' \) in \( S_G \) to a state with deadlock cycle \( (DC,\rho) \). There exists a dependence-covering sequence for \( u' \) from \( s' \) in \( S_R \). With a similar argument, there exists a successor state \( s'' \) of \( s' \) in \( S_G \) from which the same deadlock cycle can be reached and so on. Since the state space is finite and acyclic, eventually a state \( d' \) is reached in \( S_R \) where \( (DC,\rho) \) is a deadlock cycle.

A dependence-covering state space only preserves all the deadlock cycles and not deadlock states present in \( S_G \). Suppose \( w \) is a transition sequence in \( S_G \) reaching a deadlock state \( d \). Let \( u \) be a dependence-covering sequence of \( w \). Since \( u \) may contain some transitions not in \( w \) (Definition 2.4) and those may modify some shared objects, \( u \) may reach another state \( d' \) with the same deadlock cycle as \( d \). But \( d \) and \( d' \) may not be the same. Note that exploration of the dependence-covering state space does detect the set of transitions involved in each deadlock in \( S_G \).

A.2 Assertion Violations

Theorem 2.9.2. [Part of Theorem 2.9] Let \( S_R \) be a dependence-covering state space of an event-driven multi-threaded program \( A \) with a finite and acyclic state space \( S_G \). If there exists a state \( v \) in \( S_G \) which violates an assertion \( \alpha \) defined over local variables then there exists a state \( v' \) in \( S_R \) which violates \( \alpha \).

Proof. The state \( v \) is reachable from the initial state \( s_{init} \) in \( S_G \). Let \( s \) be a state which is common to both \( S_G \) and \( S_R \) such that there exists a transition sequence \( w \) from \( s \) to \( v \) in \( S_G \). In the least, the initial state \( s_{init} \) is such a state.

Let \( L \) be a dependence-covering set at \( s \). By the definition of dependence-covering set (see Definition 2.6), there exists a transition sequence \( u \) from \( s \), starting with a transition \( r \in L \) such that \( u \) is a dependence-covering sequence of \( w \). Let \( R_w \) and \( R_u \) be the sets of transitions executed in \( u \) and \( v \) respectively. Let \( R_u \subseteq R_w \) denote the set of transitions which have a direct dependence with \( \alpha \) or a dependence with some other transition which directly or transitively has a dependence with \( \alpha \). By definition (see Definition 2.4), \( R_u \subseteq R_u \) and hence, \( R_u \subseteq R_u \). Further, the relative ordering of dependent transitions in \( R_u \) is maintained in \( u \). Let \( u' \) be the state reached after executing all transitions in \( R_u \) in \( u \). Since \( \alpha \) is an assertion on local variables, no new transition \( r' \in R_u \), i.e., \( r' \in R_u \setminus R_w \) can have a dependence with \( \alpha \). Thus state \( u' \) violates the assertion \( \alpha \).

Let \( s' = r(s) \). Since \( r \in L, s' \) is in \( S_G \). If \( u \equiv r \cdot u' \) then \( u' \) is a transition sequence from \( s' \) in \( S_G \) to a state which violates \( \alpha \). With a similar argument, there exists a successor state \( s'' \) of \( s' \) in \( S_R \) from which a state which violates \( \alpha \) is reachable and so on. Since the state space is finite and acyclic, eventually a state is reached in \( S_R \) which violates \( \alpha \).

A.3 Relation between Persistent Sets and Dependence-covering Sets

Theorem A.3. If \( P \) is a persistent set in a state \( s \in S_G \) according to the standard dependence relation which considers \( \text{post} \) to the same event queue to be dependent, then \( P \) is a dependence-covering set in \( s \) according to the dependence relation of Definition 2.2.

Proof. Let \( w : r_1, r_2, \ldots, r_n \) be any transition sequence in \( S_G \) from a state \( s \). As \( w \) is a dependence-covering sequence of itself, if \( r_1 \in P \) then \( P \) is also a dependence-covering set in \( s \).

If \( r_1 \not\in P \) then by Lemma 6.8 in [11] we can infer that either (a) there exists a sequence \( u' \in \text{[w]} \) ([w] is the Mazurkiewicz trace of \( w \)) such that the first transition in \( u' \), say \( u'_1 \), is in the persistent set \( P \), or (b) all the transitions in \( P \) are independent with all the transitions in \( w \). We prove the lemma for the two cases (a) and (b) identified.

Case (a): We show that \( u' \) is a dependence-covering sequence of \( w \) even according to dependence relation of Definition 2.2. Since \( u' \in \text{[w]} \), the relative ordering of each pair of dependent transitions in \( u' \) is the same as that in \( w \). The only difference between the dependence relation of Definition 2.2 and the standard dependence relation resulting in Mazurkiewicz traces is that, Definition 2.2 considers \( \text{post} \) to be independent and does not totally order transitions executed by different event handlers on the same thread. However, if interfering (non-\( \text{post} \)) transitions are executed on two different threads, then both these dependence relations identity such pairs to be dependent. Since \( \text{post} \) are considered dependent as per the dependence relation resulting in \([w] \), the relative ordering of all \( \text{post} \) in \( w' \) posting to the same event queue is consistent with that in \( w \). As a result, the relative ordering of operations across event handlers executed on the same thread is the same in both \( w' \) and \( w \). Thus, the relative orderings of all dependent transitions in \( w \) are preserved in \( w' \) even according to Definition 2.2. Additionally, \( R_u = R_w \) because of the property of Mazurkiewicz trace. Thus, \( w' \) is a dependence-covering sequence of \( w \) such that \( w' \in P \) (assumption of this case). Therefore, \( P \) is a dependence-covering set in \( s \) as per Definition 2.6.

Case (b): Consider a state \( s' = r(s) \) such that \( r \in P \). As per the assumptions of this case, \( r \) is independent with all the transitions in \( w \) as per the standard dependence relation which considers \( \text{post} \) to the same event queue dependent. Then, sequence \( w \) is enabled at \( s \) making \( r \cdot w \) a valid sequence in \( S_G \). If any transition \( r \) in \( w \) has a \( \text{post} \) operation, then \( r \) cannot be a transition posting to the same event queue as \( r \). Otherwise, \( r \) would be dependent with \( r \), contradicting the assumption of this case. Also, if \( r \) is executed on a thread \( t \) then, no transition in \( w \) is executed on thread \( t \), because \( \text{next}(s,t) \) is unique. A pair of transitions from different threads considered independent by the standard dependence relation, are considered independent even by Definition 2.2 (see condition 2 of the definition). Hence, \( r \cdot w \) is a dependence-covering sequence of
B. Correctness of EM-DPOR

This section presents a sketch to prove the correctness of the
algorithm EM-DPOR to dynamically compute dependence-covering
sets (see Definition 2.6), presented in Section 3. Algorithm
Explore (Algorithm 1) performs a depth first traversal of the state
space. We want to prove that whenever Explore backtracks from
a state \( s \) to a prior state in the search stack, it must have explored a
dependence-covering sequence (see Definition 2.4) for any se-
quence \( w \in S_G \) from state \( s \). We equivalently prove that EM-
DPOR explores a dependence-covering set at each visited state \( s \).
Theorem B.24 given towards the end of this section formally states
this property.

We organize this section as follows. Section B.1 gives the proof
strategy for the Theorem B.24. Section B.2 provides a complete
proof or a proof sketch for the lemmas related to the cases in-
troduced in the proof strategy, and Section B.3 presents the main
proof. The variables and notation introduced in Section B.1 will be
used in the rest of this section.

Even though in Section 3.2 we had defined helper functions
such as \( \text{last}(w) \), \( \text{pre}(w) \) and a few others over a transition sequence
starting from the initial state \( s_{init} \), we may abuse the notation
in two ways. First, we may use dependence relation in its
context is the one defined in Definition B.1. The EM-DPOR algorithm explores a dependence-
covering sequence for every transition sequence \( w \in S_G \) from a state \( s \) reached by Explore(\( S \)).

Induction hypothesis H1. For every transition sequence \( w : s \rightarrow r_1 \rightarrow r_2 \rightarrow \ldots \rightarrow r_n \) in \( S_G \) that all the non-
post transitions in \( w \) are dependent with some \( \epsilon \) such that \( \epsilon \) has
started in \( w \), then \( \text{getEnd}(w, \epsilon) \rightarrow w \).

We prove the inductive case by doing an exhaustive case analy-
asis of the contents of set \( L \). Set \( L \) satisfies the properties presented
in one of the following five cases.

A. \( \exists p \in L \) such that \( p \) is a non-post transition and \( p \) is indepen-
dent with all the transitions in \( w \).

B. \( L \) contains a non-empty subset of non-post transitions such that all the non-post transitions in \( L \) are dependent with some
transition in \( w \), and no transition in \( L \) is in \( w \).

C. \( L \) contains a non-empty subset of non-post transitions such that all the non-post transitions in \( L \) are dependent with some
transition in \( w \), and the first transition in \( w \) from \( L \) is a non-
post transition.

D. \( L \) contains only post transitions and no transition in \( L \) is in \( w \).

E. The first transition in \( w \) from \( L \) is a post transition. In this case
if \( L \) contains non-post transitions we assume all of them to be dependent with some transition in \( w \). Note that the presence of non-post transitions in \( L \) does not affect the proof in this case.

Section B.2 presents lemmas reasoning the induction step for
each of the five cases above. Lemma for case A is proved by

\( w \) in conjunction with dependence relation of Definition 2.2. Thus,
\( P \) is a dependence-covering set in \( s \). □
deriving contradiction to our assumption on non-existence of a dependence-covering sequence of \( w \) starting with any transition in \( L \) from \( s \). Lemmas for cases B, C, D and E are proved by deriving contradictions to the assumptions made on the contents of \( L \), when we assume non-existence of a dependence-covering sequence of \( w \) starting with any transition in \( L \) from \( s \). This in turn proves the existence of a dependence-covering sequence of \( w \) in \( S_R \) from state \( s \).

**B.1.2 Common Construction for Cases B, C, D and E**

As shown in Figure 11 we construct a transition sequence \( z: s \xrightarrow{r_1} s'_1 \xrightarrow{r_2} s'_2 \xrightarrow{r_m} s'_m \) in \( S_C \), such that (a) \( r_1 \in L \) and (b) \( \exists r \in \text{nextTrans}(s_m) \) where \( r \) is a transition in \( w \), say \( r_m = r \) for \( 1 \leq l \leq n \) in \( w \), and \( r \) is dependent with a transition \( r_1 \) in \( s \) such that \( r_1 \) is the nearest may be co-enabled or may be reordered transition that does not happen before \( r \). Additionally, \( r_1 \) may or may not be executed in \( w \). If \( r_1 \) is executed in \( w \) then \( \text{index}(w, r) < \text{index}(w, r_1) \). We use \( z \) which is not a dependence-covering sequence of \( z \) in our proof arguments, provided \( z \) is valid in \( S_C \). We reason about the validity of \( z \) in each of cases B, C, D and E separately. In cases D and E we generate a set of relevant non-dependence-covering transition sequences of \( w \) with the help of \( z \), all of which will be used by the proofs related to cases D and E.

Figure 11 pictorially depicts some of the key states, transitions, sequences and function calls required when reasoning about cases B, C, D and E. Any other properties of \( r_1 \) specific to the case B, C, D or E considered, will be presented in Section B.2.2. Let \( Z = z.z'.r \) where \( z' \) is the shortest sequence in \( S_C \) which enables \( r \). If there exists no such \( z' \) then \( Z = \emptyset \). Note that \( z' = \emptyset \) if \( \text{thread}(r) \notin \text{enabled}(s_m) \). Let \( v \) be a suffix of \( Z \) from state \( s'_1 \) i.e., \( v = r_2.r_3...r_m.z'.r \) if \( Z = z.z'.r \) or \( v = r_2.r_3...r_m \) if \( Z = \emptyset \). Since \( s \in S_R \) and \( r_1 \in L \), state \( s'_1 = (s_1(s)) \) is in \( S_R \). Then by induction hypothesis H1, EM-DPOR explores a dependence-covering sequence \( u \) of \( v \) from \( s'_1 \). Since \( r_1 \in L \) algorithm explores \( r_1, u \). Clearly, \( r_1, u \) is a dependence-covering sequence of \( Z = r_1, v \) from state \( s \).

Let \( \delta_1 \in S_R \) be the state reached by \( S_r \gamma \) where \( \gamma \) is a prefix of \( u \) such that \( r_1 \) is a transition in \( r_1, \gamma \), and transition \( r \) dependent with \( r_1 \) in \( \text{nextTrans}(\delta_1) \). Due to the characteristics of \( r_1 \) and \( r \) described in constraint (b) given earlier on sequence \( z \), and \( r_1, u \) being a dependence-covering sequence of \( Z \) whose prefix is \( z \), \( \text{Explore}(S_r, \gamma, r_1, r) \) invokes \( \text{FindTarget}(S_r, \gamma, r_1, r) \) (line 4 in Algorithm 1). With this being a common scenario for cases B, C, D and E, we present specific arguments for each of the cases in their respective lemmas in Section B.2, and derive contradictions to the assumptions made on the contents of \( L \).

**Notation.** Given transition sequences \( w_1 \) and \( w_2 \), let \( w_1 \backslash w_2 \) denote transitions which are in sequence \( w_1 \) but not in sequence \( w_2 \). For a set of tasks \( tks \), \( \text{threadSet}(tks) = \{ t | t, c \in tks \} \), i.e., \( \text{threadSet} \) gives a set of threads corresponding to a set of tasks. Whenever we need to reason about multiple instances of variables like \( \text{candidates} \) and \( \text{pending} \) from Algorithm 1, 2, 3 or 4 in our proofs, we use numerical subscripts to distinguish one instance from the other (e.g., \( \text{candidates}_1 \) is different from \( \text{candidates}_2 \) and so on). We do not add any subscripts for variable instances corresponding to the first \( \text{FindTarget} \) call (\( \text{FindTarget}(S_r, \gamma, r_1, r) \)) from \( \text{Explore}(S_r, \gamma, r) \).

**B.2 Supporting Lemmas**

We use the induction hypothesis H1 and prove induction step separately for each of the cases A – E introduced in section B.1.1.

**B.2.1 Case A**

**Lemma B.2.** EM-DPOR explores a dependence-covering sequence of \( w \) from state \( s \) when set \( L \) satisfies case A.

**Proof.** Case A states that, \( \exists p \in L \) such that \( p \) is a non-post transition and \( p \) is independent with all the transitions in \( w \). Then, no transition in \( w \) is executed on the same thread as \( p \). This is because, \( p = \text{next}(q, \text{thread}(p)) \) for any state \( q \) visited by a prefix of \( w \). Since the next transition of a thread at any state is unique, no transition in \( w \) is executed on \( \text{thread}(p) \). Then, by the second condition of the dependence relation (Definition 2.2), \( p \) commutes with all the transitions in \( w \) and \( w \) is enabled at state \( s' = p(s) \). Since \( \delta \in S_R \) and \( p \in L \), \( s' \in S_R \). Then by induction hypothesis H1, EM-DPOR explores a dependence-covering sequence \( u \) of \( w \) from \( s' \). Therefore, \( pu \) is a dependence-covering sequence of \( w \) at state \( s \).

**B.2.2 Case B**

Case B states that the backtracking set \( L \) in state \( s \) contains a non-empty subset of non-post transitions such that all the non-post transitions in \( L \) are dependent with some transition in \( w \), and no transition in \( L \) is in \( w \). With the help of the transition sequence \( z \) described in Section B.1.2 we prove that EM-DPOR identifies a transition in \( w \) to be reordered with a non-post transition in \( L \), due to which a transition in \( w \) gets added to the set \( L \). This establishes contradiction to the property of set \( L \) which in turn proves that our primary assumption of absence of a dependence-covering sequence of \( w \) starting from a transition in set \( L \), does not hold.

To suit the case under consideration, we refine the construction of sequence \( z \) as follows.

**Construction B.3.** Let \( z: s \xrightarrow{r_1} s'_1 \xrightarrow{r_2} s'_2 \xrightarrow{r_m} s'_m \) in \( S_C \) be a sequence satisfying the following constraints:

1. \( r_1 \in L \) is a non-post transition.
2. For all \( r' \) in \( z, i \neq 1, r' \) is a transition in \( w \) and \( r'_i = r_i-1 \).
3. Recall that \( w = r_1,r_2,...,r_m \).

**Proof.** Consider a sequence \( z \) in \( S_C \) constructed as per Construction B.3. Then, as explained in the proof strategy (Section B.1.2) let \( Z = z.z'.r \) or \( Z = z \) based on the existence of shortest \( z' \) that enables \( r \). EM-DPOR explores a dependence-covering sequence \( u \) for \( v = r_2,r_3...r_m.z'.r \) or \( v = r_2,r_3...r_m \), making \( r_1 \) a dependence-covering sequence of \( Z \). Note that in this case \( r \) only consists of transitions from \( w \) and if there exists a \( z' \) satisfying the criteria considered, \( v \) also has transitions from \( z' \). Also, \( r_1 = r'_i \) (see Figure 11). From Section B.1, \( \delta_1 \in S_R \) is the state reached by \( S_r, \gamma \) where \( \gamma \) is a prefix of \( u \) such that \( r \in \text{nextTrans}(\delta_1) \).
Then set $\text{index}(S,r_1,\gamma) = |S| + 1$. This is due to line 14 in Algorithm 2, and even if $\text{index}(S, r_1, \gamma, \emptyset) < \text{index}(S, r_1, u, p')$, such that $p$ is dependent with a thread from $u$, such that $p$ is dependent with $r$. Hence there exists no $p \in \gamma \setminus v$ such that $p$ happens before $r$. Since $z'$ is a sequence to enable $r$ from state $s_m$ reached by $z$, no transition in $z'$ happens before any transition of $\text{thread}(r')$ executed in $z$. Also, $r$ is not yet executed in $S$.r'.\gamma$ and hence by Definition 3.1, no transition in $z'$ happens before $r$ in $S$.r'.\gamma$. Set candidates only consists of those tasks whose threads are enabled at state $s$, and in this case only those tasks whose enabled transition are in sequence $v \setminus z'$ and thus in $w$. Now there are two cases.

1. $\text{candidates} \neq \emptyset$ Then $\text{threadSet}(\text{candidates}) \cap \text{backTrack}(s)$ is not an empty set. This is due to line 14 in Algorithm 2, and even if $\text{threadSet}(\text{candidates}) \subseteq \text{done}(s)$, $\text{done}(s) \subseteq \text{backTrack}(s)$ at any point of execution of the algorithm. This contradicts the assumption that set $L$ has no transition from sequence $w$.

2. $\text{candidates} = \emptyset$ Then set pending computed at line 17 in Algorithm 2 is an empty set since $\text{pending} \subseteq \text{candidates}$. This results in a call to $\text{BacktrackEager}(S, r_1', \gamma, |S| + 1, r)$ on line 21. Note that $\text{index}(S, r_1', \gamma, r_1') = |S| + 1$.

$\text{BacktrackEager}(S, r_1', \gamma, |S| + 1, r)$ (Algorithm 4) temporarily copies the HB relation in $\rightarrow S. r_1', \gamma$ to $\rightarrow$ (see line 1 in $\text{BacktrackEager}$). Then, it orders each pair of co-enabled post transitions in $S$ posting events to the same destination thread, and closes the happens-before relation $\rightarrow$ with FIFO and transitivity due to newly added post to post mappings (lines 4-8). We refer to the modified happens-before relation as extended happens-before relation. We show that the extended happens-before relation does not order $r_1'$ and $r$ i.e., $i \not\rightarrow \text{task}(r)$ where $i = |S| + 1$. This is because, sequence $S.w$ executes $r$ and not $r_1'$ whereas, sequence $S.r_1'.\gamma$ executes $r_1'$ and not $r$. Hence with a common prefix $S$, sequences $S.w$ and $S.r_1'.\gamma$ explore both the ordering between $r$ and $r_1'$. Thus the order of post operations in $S$ does not determine the order of $r_1'$ and $r$. However $\text{BacktrackEager}$ only orders post operations in $S$ and their respective handlers in $S.r_1'.\gamma$.

Since $i \not\rightarrow \text{task}(r)$, Algorithm 4 does not return via line 9 and proceeds to compute set $\text{candidates}_{t_1}$ on line 14 using extended happens-before relation. Due to FIFO the handlers posted to the same thread execute in the order in which they are posted. Since $S$ is a prefix of both $S.w$ and $S.r_1'.\gamma$, the relative execution order of event handlers in $w$ and $r_1'.\gamma$ whose events are posted in $S$ is the same. $\text{BacktrackEager}$ only augments happens-before mappings between transitions of handlers posted in $S$. Thus any new happens-before mappings in the extended happens-before relation, between a transition $p$ in $r_1'.\gamma$ and $r$ is such that $p$ is a transition in $w$, and $\text{index}(S.w, p) < \text{index}(S.w, r)$. This along with our earlier reasoning on the dependence-covering property of $S.r_1'.\gamma$ proves that $\text{candidates}_{t_1}$ computed by line 14 only contains threads whose enabled transitions at $s$ are executed in sequence $w$. If $\text{candidates}_{t_1} \neq \emptyset$ then line 18 of Algorithm 4 adds a thread from $\text{candidates}_{t_1}$ to $\text{backTrack}(s)$. This contradicts the assumption that sequence $w$ has no transition from set $L$. If $\text{candidates}_{t_1} = \emptyset$, then $\text{backTrack}(s) = \text{enabled}(s)$ (line 19). Then, $\text{thread}(t_1) \in \text{backTrack}(s)$ which implies $t_1 \in L$. Transition $t_1$ being the first transition in $w$ contradicts the assumption that sequence $w$ has no transition from set $L$.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure11.png}
\caption{Illustration of key components in the proof strategy of cases B, C, D and E. Transition sequences $w$ and $Z$ start at state $s$, and sequences $v$ and $u$ start at state $s_1$. A solid circle in the proof strategy denotes a state in $S.w$. States coloured yellow correspond to sequence $w$.}
\end{figure}

B.2.3 Case C

Case C states that $L$ contains a non-empty subset of non-post transitions such that all the non-post transitions in $L$ are dependent with some transition in $w$, and the first transition in $w$ from $L$ is a non-post transition. With the help of the transition sequence...
Then set $P4$. Construction B.5 differs from Construction B.3 in constraints $M1$ with some transition $r$.

Let II.

To suit the case under consideration, we refine the definition of $w$.

Construction B.5. Let $z : s \xrightarrow{r_1} s_1 \xrightarrow{r_2} s_2 \xrightarrow{r_3} \ldots \xrightarrow{r_m} s_m$ be a sequence satisfying the following constraints:

M1. $r'_1 \in L$ is a non-post transition and $r'_1$ is the first transition in $w$ from $L$. Let $k = \text{index}(w, r'_1)$.

M2. For all $r'_i$ in $z$, $i \neq 1$, $r'_i$ is a transition in $w$ and $r'_i = r_{i-1}$.

M3. $\exists \gamma \in \text{nextTrans}(s_m)$ such that $r = r_w$ is in $w$ such that $\omega < k$, and $r$ is the first transition in $\alpha : r_1, r_2 \ldots r_{k-1}$ to be dependent with $r'_1$.

Construction B.5 differs from Construction B.3 in constraints M1 and M3. Following properties can be inferred for a sequence $z$ as constructed as per Construction B.5.

P1. All the transitions in $z$ are in $w$.

P2. Transitions $r'_1$ and $r$ may be co-enabled i.e., $\text{thread}(r'_1) \neq \text{thread}(r)$. This is because, $r'_1 = \text{next}(q, \text{thread}(r'_1))$ at any state $q$ visited by a prefix of sequence $\alpha$, including the state $s_{w-1}$, where $r = r_w$ is executed. Since both $r'_1$ and $r$ are in nextTrans$(s_w)$, $\text{thread}(r'_1) \neq \text{thread}(r)$.

P3. A sequence $z$ satisfying M1, M2 and M3 exists only if $\exists r'_1 \in L$ such that $r'_1$ is dependent with some transition prior to its index in $w$. In such a case $z$ can at least consist of $r'_1$ if $r'_i$ is dependent with some transition in nextTrans$(s_w)$ which is executed prior to $r'_i$ in $w$. If $r'_i$ is not dependent with any transition prior to it in $w$, then $z$ does not exist. Nevertheless, as will be shown in Lemma B.6, we get a dependence-covering sequence of $w$ from $s$ in $S_R$ without constructing $z$ in such a case.

P4. $z$ is not a dependence-covering sequence of $w$ at state $s$ as the dependence between $r'_1$ and $r$ does not satisfy any constraints of a dependence-covering sequence (Definition 2.4).

Lemma B.6. EM-DPOR explores a dependence-covering sequence of $w$ from state $s$ when set $L$ satisfies case C.

Proof. In the context of case C two sub-cases exist:

I. Assume there exists a transition $r'_1 \in L$ executed in $w$ such that $k = \text{index}(w, r'_1)$ and $r'_1$ is independent with all the transitions $r_i$ in $w$ for $1 \leq i < k$. Then by Definition 2.2 transition $r'_1$ commutes with all such transitions and hence $r_{k-1} \cdots r_2(r'_1(s)), \ldots) = s_k$. Since $r_{k+1}, \ldots, r_n = \text{findReschedulePending}(s)$ is a dependence-covering sequence of $w$ from state $s$.

II. Assume no transition in $L$ executed in $w$ satisfies sub-case I. Let $r'_1$ be the first transition in $w$ from $L$, and let $r'_i$ be dependent with some transition $r_i$ in $w$ where $1 \leq i < k$ where $k = \text{index}(w, r'_i)$. Consider a sequence $z$ in $S_R$ constructed as per Construction B.5. Sequence $z$ exists as sub-case II satisfies the pre-condition of property P3 of Construction B.5 as explained in Section B.1.2, let $Z = z, z', r$ or $Z = z$ based on the existence of shortest $z'$ that enables $r$. EM-DPOR explores a dependence-covering sequence $u$ for $v = r'_2, r'_3 \ldots, r_m, z', r$ or $v = r'_2, r'_3 \ldots, r_m$ making $r'_1, u$ a dependence-covering sequence of $Z$. Note that here $r'_1 = r'_1$. From Section B.1, $\delta_{y} \in S_R$ is the state reached by $S'_{r'_1}, \gamma$ where $\gamma$ is a prefix of $u$ such that $r \in \text{nextTrans}(\delta_y)$.

By Construction B.5 and its properties, transition $r'_1$ is the nearest dependent and may be co-enabled transition which does not happen before $r$. Then, $\text{Explore}(S, \gamma)$ invokes $\text{FindTarget}(S, \gamma, r_1, r)$. Line 3 in $\text{FindTarget}$ is skipped since $\text{thread}(r'_1) \neq \text{thread}(r)$. Step 2 of $\text{FindTarget}$ identifies state $s$ from where $r'_1$ is executed, as the state to add backtracking choices to reorder $r'_1$ and $r$. We show that the line 7 computes candidates $\subseteq \{\text{task}(r_1), \text{task}(r_2), \ldots, \text{task}(r_{k-1})\}$ i.e., candidates has no task $(t, e)$ such that transition next$(s, t)$ is in $\gamma \cap \alpha$. The reason for this is similar to a corresponding step in the proof of Lemma B.4. Set candidates only consists of those tasks whose threads are enabled at state $s$, and in this case only those tasks whose enabled transition at $s$ are in $\alpha : r_1, r_2 \ldots r_{k-1}$, a prefix of $w$. Now there are two cases.

1. $\text{candidates} \neq \emptyset$ Then $\text{threadSet(candidates)} \cap \text{backTrack(s)}$ is not an empty set. This is due to line 16 in Algorithm 2. This contradicts the assumption that $r'_1$ is the first transition in $w$ from $L$, as index of any transition in $\alpha$ is less than $k = \text{index}(w, r'_1)$.

2. $\text{candidates} = \emptyset$ Then set pending computed at line 17 in Algorithm 2 is also an empty set as pending $\subseteq$ candidates. This results in a call to $\text{BacktrackEager}(S, r'_1, \gamma, |S| + 1, r)$ on line 21 in Algorithm 2. Then, we can use a reasoning similar to that in the proof of Lemma B.4 to derive contradiction for the assumption that $r'_1$ is the first transition in $w$ from $L$.

B.2.4 Case D

Case D assumes all the transitions in the set $L$ to be of the type post such that none of the transitions in $L$ are in the transition sequence $w$. Unlike the lemmas related to cases B and C proving which involved reasoning about non-post transitions in the set $L$, case D requires reasoning about post transitions in the set $L$. Similar to the proof strategy of cases B and C we will show that EM-DPOR identifies some transition in $w$ to be reordered with a post transition in the set $L$. Since EM-DPOR considers a post transition to be independent w.r.t. all the transitions, the Explore algorithm never invokes $\text{FindTarget}$ to reorder a post with some other transition. However, a recursive call to $\text{FindTarget}$ may reorder a pair of posts to the same event queue (see step 1 of Algorithm 2 ($\text{FindTarget}$) and step 3c of Algorithm 3 ($\text{ReschedulePending}$)). For this to happen the pair of posts will have to be somehow related to a pair(s) of dependent transitions which are originally identified for reordering by Explore. However, establishing this relation between a pair(s) of dependent transitions and a pair of post transitions is non-trivial and may involve reasoning about a set of transition sequences ultimately leading to the identification of posts to be reordered starting from a transition sequence which identifies a pair of dependent transitions to be reordered.

With the help of the transition sequence $z$ described in Section B.1.2 we will be generating a set of transition sequences of interest, which will lead to the identification of a post in $w$ to be reordered with a post in the backtracking set $L$. After identifying these posts and establishing that $\text{FindTarget}$ will be called to reorder them, we will show that a transition from $w$ gets added to the set $L$ by invoking arguments similar to the proofs of Lemma B.4 and B.6. This establishes contradiction to the property of set $L$, and in turn establishes the existence of a dependence-covering sequence of $w$ starting from some transition belonging to the set $L$.

We make the following assumptions to simplify the proof sketch.

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**Assumption B.6.1.** For any transition sequence \( \alpha \) executed from state \( s \) considered henceforth (including sequence \( w \) and \( z \)) we make the following assumptions. Let \( K_\alpha \) be the set of transitions in \( \alpha \) such that for each \( k \in K_\alpha \), \( k \notin w \). Then,

1. Transitions in \( K_\alpha \) do not form a deadlock cycle consisting only of transitions in \( K_\alpha \).
2. Every lock acquired inside a task is released within the same task (thread or event handler). This assumes that a lock acquire and release does not span multiple event handlers.
3. If a transition \( p \in K_\alpha \) is disabled at a state, then it does not require a transition in \( w \) to be executed for \( p \) to eventually enable.

Reasoning about this case requires a few new definitions which we introduce below.

**Definition B.7.** A function \( DG(p, \alpha, s') \) which defines a dependence graph of a transition w.r.t. a sequence, takes a transition \( p \) and a sequence \( \alpha \) executed from a state \( s' \) where \( p \in R_\alpha \) or \( p \in nextTrans(last(\alpha)) \), and returns a set \( P \) such that \( P \subseteq R_\alpha \) and for each transition \( a \in P \), if \( p \in R_\alpha \) then \( index(\alpha, a) \rightarrow_\alpha index(\alpha, p) \) else either \( index(\alpha, a) \rightarrow_\alpha task(p) \) or \( a \) is dependent with \( p \).

The following definition gives the criteria when dependence graphs of a transition w.r.t. two different sequences are equivalent.

**Definition B.8.** Predicate \( identicalDG(p, \alpha, \beta, s') \) takes a transition \( p \), and transition sequences \( \alpha \) and \( \beta \), both executed from the same state \( s' \), such that \( p \in R_\alpha \cup nextTrans(last(\alpha)) \), \( p \in R_\beta \cup nextTrans(last(\beta)) \), and the predicate evaluates to TRUE only if \( DG(p, \alpha, s') = DG(p, \beta, s') \).

**Definition B.9.** A set \( future(r) \) is a set of transitions such that a transition \( r' \in future(r) \) if, (1) there exists a sequence \( \alpha \) in \( S_C \) such that \( r' \) is executed by the handler of the event posted by \( r \) in \( \alpha \), or (2) \( r' \in future(r'') \) such that \( r'' \) is a post operation and \( r'' \in future(r) \).

**Definition B.10.** A set \( enabledFuture \) of a post operation \( r \), i.e., \( enabledFuture(r) \) is a set of transitions such that a transition \( r' \in enabledFuture(r) \) if, (1) \( r' \in future(r) \), or (2) there exists a sequence \( \alpha \) in \( S_C \) reaching a state \( s' \) such that a transition \( r'' \in future(r) \) is blocked in \( s' \) and \( r'' \) is the first transition of a shortest sequence from \( s' \) which enables \( r'' \), or (3) \( r' \in enabledFuture(r'') \) such that \( r'' \) is a post operation and \( r'' \in enabledFuture(r) \).

**Construction B.11.** Let \( z : s \xrightarrow{c_1} s_1 \xrightarrow{c_2} s_2 \cdots \xrightarrow{c_m} s_m \) in \( S_C \), where \( r'_1 \in L \) and \( v = r'_2 \cdots r'_m \), be a sequence satisfying the following constraints:

1. Sequence \( v \) consists of transitions belonging to \( w \) as well as transitions outside \( w \). For a transition \( r'_1 \in v \), if \( r'_1 \notin \) then \( identicalDG(r'_1, w, z, s) \).
2. For a transition \( r'_1 \in v \), if \( r'_1 \notin \) then \( r'_1 \) is the first transition of a shortest sequence from the state \( s_{i-1} \).\( \) comprising only of transitions which do not belong to \( w \), to be executed to make an event \( e \) which was dequeued in \( w \) but blocked in \( s_{i-1} \) executable.

**M2.** There exists no extension to any prefix of \( z \) which results in a transition sequence \( \alpha, \gamma \) such that there exists a pair of dependent transitions \( c \) and \( d \) with the following properties:

- (i) Either \( c \) and \( d \) are transitions in \( w \) such that they are ordered differently in \( \gamma \) compared to their order in \( w \), or
- (ii) \( c \notin w \), \( c \in \) is a transition in the \( enabledFuture \) set of a post in \( w \), and \( d \in w \) such that \( c \) is executed prior to \( d \) in \( \alpha, \gamma \), and

(b) Attempting to reorder \( c \) and \( d \) through some other extension to \( \alpha \) will only result in a transition sequence \( \alpha, \gamma' \) which breaks the order between another pair of dependent transitions \( c' \) and \( d' \) such that either (i) \( c', d' \notin w \), or (ii) \( d' \notin w \), \( c' \) is a transition in the \( enabledFuture \) set of a post in \( w \), and \( c' \) is executed prior to \( d' \) in \( \alpha, \gamma' \).

M3. There exists a transition \( r \in nextTrans(s_{m-1}) \) such that \( r \) is a transition in \( w \) and \( r \) is dependent with a transition \( r'_1 \notin \) executed in \( v \) such that \( r'_1 \in enabledFuture(r'_1) \).

M4. \( z \) is a sequence with maximum transitions from \( w \) while satisfying the constraints M1, M2 and M3.

From the constraints given in Construction B.11, a pair of transitions in \( w \) posting to the same event queue can be reordered in sequence \( z \) so long as the properties M1 and M2 are respected. We now present a lemma describing the property of transitions not in \( w \) but present in \( v \).

**Lemma B.12.** In a transition sequence \( z = r'_1.v \) constructed by only following the constraint M1 of Construction B.11, a transition \( r'_1 \notin \) such that \( r'_1 \notin \) satisfies one of the following properties.

1. \( r'_1 \in enabledFuture(r'_1) \), or
2. \( r'_1 \in enabledFuture(r'_2) \) where \( r'_2 \) is a post transition in \( w \).

**Proof.** We prove this by inducting on the order in which transitions not belonging to \( w \) are added to \( v \).

**Base case.** Let \( r'_1 \) be the first transition in \( v \) which does not belong to \( w \). Recall that \( r'_1 \in L \) is the first transition of \( z \), and from the property of case D we know that \( r'_1 \notin \) and it is a post transition. This makes \( r'_1 \) the second transition in \( z \) to not be from the sequence \( w \). As per constraint M1 of Construction B.11, a transition not belonging to \( w \) is added to \( v \) only to make an event dequeued in \( w \) executable. Assume that \( r'_1 \) has been added to make an event \( e \) blocked in the state \( s_{i-1} \) and dequeued in \( w \), executable. Let \( E \) be the set of events on \( thread(e) \) such that for each event \( e' \in E \), either \( e' \) is the executable event on \( thread(e) \) at state \( s_{i-1} \) or \( e' \) is an event blocked in \( e \)'s event queue in state \( s_{i-1} \).\( s_{i-1} \) such that \( e' \) is dequeued prior to \( e \). If any of the events in \( E \) is dequeued in \( w \), then executing \( r'_1 \) breaks the property M1. This is because in such a case, the shortest sequence to make \( e \) executable will also comprise of transitions from \( w \). Also, if any event \( e' \in E \) is posted by a transition in sequence \( S \) prior to reaching the state \( s \) from where \( w \) is assumed to be executed, then due to FIFO ordering we can infer that \( e' \) is dequeued prior to \( e \) in sequence \( w \) as well. By elimination, each event in \( E \) is either (a) the event posted by \( r'_1 \), since \( r'_1 \) is the only transition in \( z \) that does not belong to \( w \) when state \( s_{i-1} \) is reached, or (b) an event posted by a transition in \( w \) but was not dequeued in \( w \). The shortest sequence to make \( e \) executable will atleast comprise of the transitions in the handlers of the events in \( E \), and \( r'_1 \) could be the deque transition of the executable event on \( thread(e) \) which too is in \( E \). However, if a transition, say \( b \), in the handler of \( e' \in E \) is blocked on some transition outside the handler of \( e' \) (e.g., if it is a transition acquiring a lock held by some other thread), then the shortest sequence to make \( e \) executable will also include transitions to enable \( b \); transition \( r'_1 \) could be a transition executed to eventually enable \( b \). In either case, \( r'_1 \) satisfies the constraints to be in \( enabledFuture(r'_1) \) or \( enabledFuture(r'_2) \) where \( r'_2 \) is a transition posting an event in \( E \). Hence proved.

**Induction hypothesis.** All the transitions up to \( k^{th} \) transition added to \( v \) which do not belong to \( w \) either belong to \( enabledFuture(r'_1) \), or belong to \( enabledFuture(r'_2) \) where \( r'_2 \) is a post transition in \( w \).
Induction step. We need to show that one of the two properties specified in the lemma holds even for the \((k + 1)\)th transition, say \(r'_1\), that does not belong to \(w\) but is added to \(v\). Then from the condition M1, \(r'_1\) should be the first transition in a shortest sequence comprising only of transitions not in \(w\), to make an event \(e\) executable such that \(e\) is dequeued in \(w\) but is currently blocked in the state \(s'_1\). Then, either \(r'_1\) is a transition in the executable task on \(thread(e)\), or it is a transition that must be executed so as to eventually enable a transition \(b \not\in w\) in the executable task on \(thread(e)\) or the handler of an event prior to \(e\) in \(e\)'s event queue. Otherwise, \(r'_1\) can be removed to obtain a shorter sequence executing which can make \(e\) an executable event. Let us firstly reason about the case where \(r'_1\) is a transition in the executable task on \(thread(e)\), and let \(e'\) be the corresponding event of the executable task. Then, \(post(e')\) which is clearly executed prior to \(r'_1\), is either a transition in \(w\) or a transition not in \(w\). In the latter case due to induction hypothesis, \(post(e')\) satisfies one of the two properties listed in the lemma. If \(post(e')\) is a transition in \(w\) or \(post(e')\) is a transition in the \(enabledFuture\) set of a \(post\) transition in \(w\) (as per property 2 listed by the lemma), then by Definition B.10 transition \(r'_1\) too belongs to the \(enabledFuture\) set of a \(post\) transition in \(w\) thus satisfying condition 2. If \(post(e')\) \(\in\) \(enabledFuture(r'_1)\) (as per property 1 listed in the lemma), then \(r'_1\) being in the handler of \(e'\) satisfies the constraints to be in \(enabledFuture(r'_1)\).

Now consider the case where \(r'_1\) has been added to eventually enable a transition \(b \not\in w\) in the executable task on \(thread(e)\) or the handler of an event prior to \(e\) in \(e\)'s event queue. Let \(e'\) be the event corresponding to the handler in which the transition \(b\) is executed. Now we can show that \(r'_1\) belongs to \(enabledFuture(r'_1)\) or \(enabledFuture(r'_1)\) where \(r'_1\) is a \(post\) transition in \(w\), by reasoning about \(post(e')\) similar to the first case presented above.

**Lemma B.13.** A transition sequence \(z = r'_1, v\) which satisfies the constraints M1, M2 and M3 exists in \(S_G\).

**Proof.** A transition sequence \(z = r'_1, v\) satisfying the constraint M1 in Construction B.11 trivially exists in \(S_G\). One such sequence can be constructed by concatenating \(r'_1\) with a prefix of \(w\) till the next transition to be executed in \(w\) is a \(def\) transition whose event \(e\) is blocked on \(dest(r'_1)\), such that the event posted by \(r'_1\) must be dequeued and handled for \(e\) to become executable. If there is no such prefix then we must be able to execute \(r'_1\), \(w\) which clearly is a dependence-covering sequence of \(w\), since \(r'_1\) being a \(post\) transition is independent w.r.t. all the transitions in \(w\) as per the dependence relation defined in Definition 2.2.

Now, let \(z = r'_1, v\) be a transition sequence in \(S_G\) satisfying the constraints of M1. Our main assumption is that there exists no transition sequence starting from any transition in the backtracking set \(L\) at \(s\) which is a dependence-covering sequence of \(w\). Then, the sequence \(z\) must reach a state \(s'_m\) where a transition \(r \in nextTrans(s'_m)\) such that \(r \in w\), \(identicalDG(r, w, z, s) = FALSE\) and no extension \(\gamma\) to \(z\) can result in \(identicalDG(r, w, z, \gamma, s)\). Otherwise, we can obtain a sequence \(z\) which is a dependence-covering sequence of \(w\). Since all the transitions belonging to \(w\) in the constructed sequence \(z\) have their \(DG\) identical to that found in \(w\), there can be only two causes for the \(DG(r, z, s)\) to be different from that w.r.t. \(w\) — (1) a transition \(r' \not\in w\) present in \(v\) is dependent with \(r\), or (2) \(r \in nextTrans(s'_m)\) must be executed so as to execute a dependent transition \(r' \in w\) such that \(r'\) is executed prior to \(r\) in \(w\). From Lemma B.12, if it is case (1) then there can be two subcases: (1.a) \(r' \in enabledFuture(r'_1)\), or (1.b) \(r' \in enabledFuture(r'_1)\) where \(r'_1\) executed prior to \(r'\) in \(v\) is a \(post\) transition in \(w\).

Let us assume that any sequence \(z = r'_1, v\) satisfying the constraints of M1 can only satisfy the cases 1.b or 2 defined above. We will establish a contradiction for this assumption thus establishing the validity of constraint M2 and M3 given in Construction B.11. Towards this, we construct a sequence \(z\) by strengthening the constraints of M1. Let \(z = r'_1, v\) be a transition sequence constructed as per M1 as well as a constraint that for every pair of posts \(p_1 \in P_1\) and \(p_2 \in P_2\) executed in \(z\) and posting events to the same event queue, \(index(z, p_1) < index(z, p_2)\) iff \(index(w, p_1) < index(w, p_2)\). Let \(z\) be the longest such sequence. Then, \(z\) reaches a state \(s'_m\) where a transition \(r \in nextTrans(s'_m)\) is such that \(r \in w\) and \(r\) satisfies one among the cases 1.b or 2 or (3) \(r\) is a \(post\) transition which must be executed so as to execute a \(post\) transition \(r' \in w\) posting to the same event queue as \(r\) such that \(r'\) is executed prior to \(r\) in \(w\). If \(z\) satisfies condition 3 then \(r\) at \(s'_m\) violates the constraint on ordering between \(post\) transitions.

The reasoning for cases 2 and 3 are similar. Let us firstly assume that \(r\) satisfies either of case 2 or 3. This indicates the existence of a transition \(r' \in w\) either dependent with \(r\) (if case 2) or posting to the same event queue as \(r\) (if case 3) such that \(r\) must be executed to eventually execute \(r'\), even though \(r'\) was executed prior to \(r\) in \(w\). Let a sequence \(\gamma\) from \(s'_m\) be the shortest sequence such that \(r' \in nextTrans(last(z, \gamma))\). Let \(P\) be a set of transitions such that a transition \(p \in P\) iff \(index(S, z, \gamma, p) \rightarrow s, \gamma, task(r'p)\) and \(p \in \gamma\). Since \(r'\) is a transition in \(w\), all the transitions in the set \(P\) too are in \(w\). We argue that either there exists a transition \(p \in P\) such that \(task(p)\) is blocked on \(thread(r)\) at state \(s'_m\), or attempting to reorder \(r\) and \(r'\) by executing transitions related to \(r'\) (for example those in the set \(P\) or in event handlers executed prior to handlers containing some transitions in \(P\)) prior to \(r\) breaks the ordering between another pair of transitions from \(w\) such that these transitions are either dependent or post to the same event queue. In the latter case we argue that attempting to reorder the new adversely ordered transitions in turn breaks the ordering between some other pair of transitions from \(w\) and so on. Since the state space we consider is finite and acyclic, continuing this process of reordering adversely ordered transitions eventually causes \(r\) to execute prior to \(r'\). If this is not the case then \(r'\) can be executed prior to \(r\) which indicates the existence of some other sequence longer than \(z\) and satisfying the constraints M1 and ordering restriction between posts. This violates our assumption of \(z\) being the longest such sequence. All these pairs of transitions including \(r\) and \(r'\) were ordered as desired in sequence \(w\). This indicates the presence of a pair of events posted to the same event queue by a pair of transitions in \(z\) such that these events were differently ordered in \(w\). This contradicts the constraints of \(z\) which should have preserved the relative ordering between transitions in \(w\) posting to the same event queue. Hence, \(z\) does not satisfy case 2 or 3.

Now consider the case 1.b according to which \(r\) is dependent with \(r'_1 \in enabledFuture(r'_1)\) such that \(r'_1 \not\in w\) and \(r'_1\) is a \(post\) transition in \(w\). We choose nearest such \(r'_1\) w.r.t. \(r'_1\). In other words, if \(r'_1 \not\in enabledFuture(r'_1)\) and \(r'_1 \in enabledFuture(r'_1)\) such that \(r'_1 \not\in enabledFuture(r'_1)\) where \(\{r'_1, r'_1\} \subseteq z\) are \(post\) transitions in \(w\), then we choose \(r'_1 = r'_1\). From (i) the constraints of Definition B.10, (ii) knowing that a subset of transitions in \(enabledFuture(r'_1)\) executed in \(z\) were not executed in \(w\) and (iii) \(r'_1\) being the nearest such \(post\) to whose \(enabledFuture\) set \(r'_1\) belongs, we infer that a suffix of the handler of the \(post\) \(r'_1\) in \(w\) is not executed in \(w\). Let \(e\) be the event posted by \(r'_1\). Either a set of transitions from such a suffix of \(e\)'s handler are included in \(z\), or \(r'_1\) is a transition executed to eventually enable a transition from such a suffix of \(e\)'s handler. In either case since these transitions do not belong to \(w\), these transitions have been added to \(z\) so as to make an event \(e'\) dequeued in \(w\) executable such that \(e'\) is blocked on \(e\)'s event queue when \(e\) is the executable event. From the concurrency semantics of the event-driven model considered, an event handler is executed to completion before the next
event on the corresponding event queue is dequeued. We know that both the events $e$ and $e'$ are posted to $w$. Then, at least one among the handlers of $e$ and $e'$ must have been executed to completion. Since we have assumed that $e'$'s handler is partially executed in $w$, clearly event $e$'s handler has been executed to completion in $w$. This implies that $\text{index}(w, \text{post}(e')) < \text{index}(w, \text{post}(e))$ (due to FIFO processing of events). This inference contradicts their ordering in $z$ since $e'$ is blocked when $e$ is executable in $z$. This in turn violates the constraints assumed on $z$. Thus, we have shown that a transition sequence $z$ constructed this way cannot satisfy case 1.b.

From the above arguments we have established the existence of a transition sequence $z = r'_1.v$ constructed as per the constraint M1 for which neither of cases 1.b or 2 holds. Then, such a transition sequence must satisfy the case 1.a according to which a transition $r \in \text{nextTrans}(s_m)$ is dependent with a transition $r'_1 \not\in w$ such that $r'_1 \in \text{enabledFuture}(r_1)$. This shows that a transition sequence satisfying the constraints M1, M2 and M3 of Construction B.11 exists in $S_2$. 

Lemma B.14. Reordering $r$ and $r'_1$ identified by Construction B.11 by reordering some pair of transitions in $v$, is either not possible or will only result in a sequence $v'$ (executed from state $s'_1$) such that for $v'$ and any extension $\gamma$ to $v'$ one of the following holds: (i) the dependence graph of a transition $r'_1 \in \text{nextTrans}(last(v'))$ such that $r'_1$ is executed in both $w$ and $z$, becomes non identical to $\text{DG}(r'_1, w, s)$, or (ii) there exists a pair of dependent transitions $p \in v'.\gamma$ and $q \in \text{nextTrans}(last(v'))$ such that $q$ is executed prior to $p$ in $w$, or (iii) there exists a pair of dependent transitions $p \in v'.\gamma$ and $q \in \text{nextTrans}(last(v'))$ such that $q \in w$, $p \not\in w$ and $p \in \text{enabledFuture}(p')$ where $p'$ is a post in $w$.

Proof. We prove this by contradiction. Assume that a resulting transition sequence $v'$ executes $r$ before $r'_1$ such that $\text{identicalDG}(r, w, r'_1, v', s)$ holds, and without resulting in any scenario listed in (i), (ii) or (iii) above. Then such a transition sequence $r, v'$ clearly has more number of transitions from $w$ compared to $z = r'_1.v$, with their dependence graphs consistent with that found in the context of $w$. Also, since no extension to $v'$ satisfying (ii) or (iii) is possible when $r$ and $r'_1$ are reordered as per our assumption, an extension to $r, v'$, say $\gamma$, must hit a state where a transition $r'' \in \text{nextTrans}(last(v'), \gamma)$ belonging to $w$ is dependent with a transition $r'' \in v'$ such that $r'' \not\in w$. If not, an extension to $r, v'$ will result in a dependence-covering sequence for $w$. Then, $r', v'.\gamma$ is a transition sequence satisfying the constraints M1, M2 and M3 of Construction B.11, and having more transitions from $w$ than $z$. This implies that $z$ did not satisfy the constraint M4 of Construction B.11. Thus, one of the properties (i), (ii) or (iii) must hold on any such sequence $r', v'$.

Lemma B.15. Transition $r'_1$ must be reordered w.r.t. some transition $r''_1 \in v$ (where $z = r'_1.v$) belonging to $w$ such that $r''_1$ posts an event to the same destination event queue as $r'_1$, so as to obtain a transition sequence $z'$ from the state $s$ which satisfies the following properties — (1) either $r$ is executed prior to $r'_1$ in $z'$ or only $r$ is executed in $z'$, (2) every transition $r'_1$ in $z$ which also belongs to $w$ is executed in $z'$ such that $\text{identicalDG}(r'_1, w, z', s)$, (3) there exists atleast one extension $\gamma$ to $z'$ where neither of the following hold: (a) there exists a pair of dependent transitions $p \in z'.\gamma$ and $q \in \text{nextTrans}(last(z')).$ such that $q$ is executed prior to $p$ in $w$, or (b) there exists a pair of dependent transitions $p \in z'.\gamma$ and $q \in \text{nextTrans}(last(z')).$ such that $q \in w$, $p \not\in w$ and $p \in \text{enabledFuture}(p')$ where $p'$ is a post in $w$.

Intuition to prove that EM-DPOR explores a dependence-covering sequence for case D. In the cases B and C the transition $r'_1$ belonging to the backtracking set $L$ and executed at state $s$, was a non-post transition. Hence a transition in $w$, say $r$, which was dependent with $r'_1$ could be easily identified leading to a non-dependence-covering sequence of $w$. We then argued that EM-DPOR would attempt to reorder $r'_1$ and $r$, and add a backtracking choice at state $s$ which would break the property assumed on the backtracking set $L$ at $s$. Thus we were able to prove the existence of a dependence-covering sequence of $w$ starting from a transition in the set $L$, through proof by contradiction.

In case D however $r'_1 \not\in L$ executed at state $s$ is a post transition, which makes it harder to identify a transition in $w$ that must be reordered with $r'_1$ to obtain a dependence-covering sequence of $w$. This is because even though ordering between events posted to the same queue affect the ordering between dependent transitions, the ordering between transitions posting to the same event queue are not directly captured in a dependence-covering sequence. Hence, the influence of $r'_1$ on the non-post transitions in $w$ can only be identified through the interference from non-post transitions in the $\text{enabledFuture}$ set of $r'_1$. Lemma B.15 establishes that $r'_1$ must be reordered with a transition $r''_1 \in v$ posting to the same event queue as the destination of $r'_1$ where $r''_1 \not\in w$, so as to execute more transitions from $w$ in the resulting sequence but without resulting in adversarial scenarios i, ii and iii listed in Lemma B.14. This could eventually lead to a dependence-covering sequence of $w$. In order to identify such an $r''_1$, we systematically generate a set $\Gamma$ of transition sequences starting from $z$ by flipping the ordering between certain dependent transitions and transitions posting to the same event queues belonging to $R \cup \text{nextTrans}(\text{last}(S.z))$. A few pairs of dependent transitions and transitions posting to the same event queues and seen in transition sequences of the set $\Gamma$, are encoded as a tree called $\Gamma$-tree. Intuitively the $\Gamma$-tree encodes all pairs of dependent transitions and post operations explored in the subspace reached from $s'_1$ (state reached on executing $r'_1$) such that exploring every pair of transitions in $\Gamma$-tree in a manner consistent to obtain a dependence-covering sequence of $w$, requires reordering $r'_1$ with $r''_1$. We will then show that EM-DPOR too is capable of identifying all the transition pairs of $\Gamma$-tree ultimately leading to the identification that $r''_1$ must be reordered with $r'_1$.

To aid the proof we define a tree called $\Gamma$-tree which can encode certain transition pairs which are of interest to the proof.
Definition B.16. $\Gamma$-tree is a tree with each of its nodes being a set of ordered pairs of transitions and its root node being $(\{r'_1, r'_2\})$. Let $\Gamma_{\text{node}} = \{(c_1, d_1), (c_2, d_2), \ldots, (c_8, d_8)\}$ be a non-root node in the $\Gamma$-tree. Then,

N1. For all $i \in [1, 8]$, $d_i \in w$ and $c_i$ may or may not be a transition of $w$ such that if $c_i \in w$ then $d_i$ is executed prior to $c_i$ in $w$. If $c_i \notin w$ then either $c_i \in \text{enabledFuture}(r'_1)$ or $c_i \in \text{enabledFuture}(r'_j)$ where $r_j$ is a post transition in $w$.

N2. Each pair $(c_i, d_i)$ is such that either $c_i$ and $d_i$ are dependent transitions, or $c_i$ and $d_i$ are transitions posting events to the same event queue.

N3. If $\Gamma_{\text{node}}$ is a leaf node of $\Gamma$-tree then it only contains pairs of dependent transitions as its members. If it is a non-leaf node then it contains atleast one pair of transitions posting to the same event queue.

N4. Transition pairs $c_i$ and $d_i$ can either be from two different threads or two different handlers on the same thread. If it is the latter then $\Gamma_{\text{node}}$ is a singleton set. However, if $\Gamma_{\text{node}}$ has multiple transition pairs then each pair $(c_i, d_i)$ are such that $\text{thread}(c_i) \neq \text{thread}(d_i)$.

N5. There exists a subspace $S_{cd}$ of $S_C$ reachable from the state $s'_i$ (reached on executing $r'_i \in L$), such that in $S_{cd}$ it is not possible for $d_i$ from every pair of transitions in $\Gamma_{\text{node}}$, to execute prior to $c_i$. In other words, there always exists one pair of transitions $c_i$ and $d_i$ such that $d_i$ cannot be executed prior to $c_i$ in $S_{cd}$ even when for all the other pairs $(c_j, d_j)$, $j \neq i$, $d_j$ executes prior to $c_j$ in $S_{cd}$. Attempting to reoder $(c_i, d_i)$ within $S_{cd}$ will alter the order between other pair of transitions in $\Gamma_{\text{node}}$, thus making the resultant transition sequence non dependence-covering w.r.t. $w$.

N6. In the subspace $S_{cd}$, the transitions $c_i$ and $d_x$ satisfy one of the following criteria — (a) $c_1$ and $d_x$ are transitions of two different event handlers on the same thread such that event($\text{task}(d_x)$) is blocked when event($\text{task}(c_1)$) is executable, or (b) a transition prior to $d_x$ in the task of $d_x$ is enabled in the event handler blocked on thread($c_1$) when $c_1$ is the next transition on that thread, or (c) $c_1$ needs to be executed to enable a transition $q$ blocked in an event handler such that either event($\text{task}(d_x)$) is blocked on thread($q$) when $q$ is the next transition on that thread, or a transition prior to $d_x$ in the task of $d_x$ is enabled by a transition in the event handler blocked on thread($q$) when $q$ is the next transition on that thread.

N7. Let $e_o$ and $\text{cd}$ respectively be the executable event related to $c_1$ and the blocked event related to $d_x$ (as identified by N6 above) in the subspace $S_{cd}$. The events $e_o$ and $\text{cd}$ posted to the same thread are such that, either $e_o$ is not posted in the transition sequence $S:w$ whereas $\text{cd}$ is posted in $w$ or $\text{cd}$ is posted prior to $e_o$ in $w$.

N8. The parent node of $\Gamma_{\text{node}}$ in $\Gamma$-tree is a node $\Gamma_{\text{par}}$ which contains (post($e_o$), post($\text{cd}$)) as a transition pair. Reordering post($e_o$) and post($\text{cd}$) results in a state space where every transition $d_x$ in the transition pairs of the $\Gamma_{\text{node}}$ can be executed prior to corresponding $c_i$ thus making them consistent w.r.t. ordering observed in $w$. We refer to $\Gamma_{\text{node}}$ as the child of $\Gamma_{\text{par}}$ obtained on exploring post($e_o$) prior to post($\text{cd}$).

N9. $\Gamma_{\text{node}}$ has the same number of child nodes as the number of pairs of $\text{post}$ in $\Gamma_{\text{node}}$.

N10. Every path in the tree from the root to a node containing atleast one pair of dependent transitions encodes a non dependence-covering sequence of $w$ from state $s$, say $v_h$, which identifies one pair of dependent transitions which either are ordered differently compared to their ordering in $w$ or form a new incoming dependence into a transition in $w$.

We can systematically construct certain interesting non dependence-covering transition sequences of $w$ using $\Gamma$-tree paths, each of which have a transition $b$ belonging to $w$ whose DG over the constructed transition sequence does not match DG$(b, w, s)$.

Construction B.17. A transition sequence $v_h$ is constructed using a path of $\Gamma$-tree by performing steps I, II and III below. The order between those transitions in $v_h$ which are not explicitly specified by the step II below can be arbitrary but valid w.r.t. the orders fixed for transitions reasoned in step II and consistent w.r.t. dependence graph over $w$.

Step I. Start from the root of the $\Gamma$-tree.

Step II. At each node $\Gamma_{\text{node}} = \{(c_1, d_1), (c_2, d_2), \ldots, (c_8, d_8)\}$, pick a pair of transitions $(c_i, d_i)$ such that $c_i$ will be executed prior to $d_i$ in the sequence $v_h$ while the order of other transition pairs (if can be executed in $v_h$) are consistent w.r.t. $w$ i.e., $d_i$ is executed prior to $c_i$ for $j \neq i$.

Step III. If the pair $(c_i, d_i)$ selected are non-post dependent transitions then the construction of $v_h$ is complete, else move to the child obtained on exploring $c_i$ prior to $d_i$ and repeat Step II.

Observations for Construction B.17. From the step III of Construction B.17 we note that the process of constructing a transition sequence of interest can stop even at an intermediate node. A transition sequence $v_h$ identified by this construction has one transition $d_i \in w$ (corresponding to the last pair of transitions selected from a $\Gamma$-tree node) which has dependence with a prior executed transition $c_i$ such that either $c_i \notin w$ or $d_i$ is executed prior to $c_i$ in $w$. Hence, this construction cleanly identifies a pair of transitions in $v_h$ which need to be reordered so as to eventually obtain a dependence-covering sequence of $w$.

Lemma B.18. A $\Gamma$-tree defined by Definition B.16 can be constructed in the state space $S_C$.

Proof. We prove this by giving a sketch for constructing $\Gamma$-tree starting with the transition sequence $z = r'_iv$ constructed as per Construction B.11.

Figure 12 pictorially represents the $\Gamma$-tree. The variables $a$ and $b$ in the root stand respectively for $r'_1$ and $r'_w$. We annotate the only child of the root node as $\Gamma_0$. Except the root node, every other node $\Gamma_{[k_1..k_j]}$ contain transition pairs of the form $(a[j_1..j_k], b[k_1..k_j])$, such that exploring the transition $a[j_1..j_k] \text{ before } b[k_1..k_j]$ in a transition sequence results in the discovery of the subtree rooted at $\Gamma_{[k_1..k_j]}$. This makes $(a[j_1..j_k]\text{ prior to } b[k_1..k_j])$ the transition pair corresponding to $\Gamma_{[k_1..k_j]}$ in its parent node. The last pair of transitions in the set corresponding to $\Gamma_{[k_1..k_j]}$ is identified as $(a[k_1..k_j]b[k_1..k_j], a[k_1..k_j]b[k_1..k_j])$, (where $(ab)$ denotes the count of the number of transition pairs in the node $\Gamma_{[k_1..k_j]}$).

From the constraint M3 of Construction B.11, $r'_i$ is in the set enabledFuture($r'_1$). Based on this and the Definition B.10 we can identify a chain of post transitions related to $r'_i$, which is a subsequence of $z = r'_iv$ identified henceforth as $p_0 \ldots p_m$. The chain of posts $p_0 \ldots p_m$ is such that (i) $p_0 = r'_1$, (ii) for any $i \in [1, m - 1]$, $p_i$ is either in the handler of the event posted by $p_{i+1}$ or $p_0$ has been added to enable a blocked transition in the handler of the event posted by $p_{i+1}$, and (iii) the transition $r'_i$ is either in the handler of the event posted by $p_i$ or $r'_i$ is a transition added to enable a blocked transition in the handler of the event posted by $p_1$. We encode each of the transitions in the chain $p_0 \ldots p_m$ and $r'_i$ as the first transition in the ordered pair of transitions belonging to different $\Gamma$-tree nodes in the leftmost branch of the $\Gamma$-tree in Figure 12. Through this construction sketch we will reason that for
any \(i \in [1, \eta - 1]\), \(p_i\) is the first transition in a pair belonging to a node whose parent node contains the transition \(p_{i+1}\) in a member pair. Similarly, \(r'_t\) is a transition in a pair belonging to a node whose parent node contains the transition \(p_1\) in a member pair.

In case of \(r'_t\), \(r\) is the transition occupying the second position in the pair corresponding to \(r'_t\). Figure 12, the node annotated \(\Gamma_{1...1}\) identifies the \(\Gamma\)-tree node containing the pair \((r'_t, r)\). In this node we use \((a_{1...1}, b_{1...1})\) to denote \((r'_t, r)\), where \(\varphi\) denotes the count of \(\Gamma\)'s in the first part of the subscript. Indeed we will reason that \(\varphi = \eta - 1\) and for \(\vartheta \in [1, \eta - 1]\), \(a_{1...1\vartheta-1}\) = \(p_{\eta-\vartheta}\).

Let us now see how to identify the rest of the transition pairs in the node \(\Gamma_{1...1}\). Assume \(\text{thread}(r'_t) \neq \text{thread}(r)\). Let \(P\) be a set of transitions such that a transition \(p \in P\) if \(\text{index}(S, z, p) > \text{index}(S, z, r'_t)\). Clearly, all the transitions in \(P\) were executed prior to \(r\) in \(w\) as well (by M1 in Construction B.11). Now in order to execute \(r\) prior to \(r'_t\), all the transitions in the set \(P\) also need to execute prior to \(r\). However, attempting to explore transitions in set \(P\) from the state \(s'_{1...1}\) (from where \(r'_t\) is executed in sequence \(z\)) will result in one of the three scenarios listed in Lemma B.14. Concretely, this happens because of one of the following reasons.

S1. A non-post transition \(c\) belonging to \(P\) or belonging to a task \(h\) on whose thread the task of some transition in \(P\) is blocked, gets shifted prior to \(r'_t\) even though \(c\) has dependence with a transition \(d \in w\) such that \(d\) can be executed only after \(r'_t\) and \(d\) is executed prior to \(c\) in \(z\), or

S2. A post transition \(c\) belonging to \(P\) or belonging to a task \(h\) on whose thread the task of some transition in \(P\) is blocked, gets shifted prior to \(r'_t\) and gets reordered w.r.t. a post transition \(d \in w\) such that \(d\) can be executed only after \(r'_t\) and \(d\) is executed prior to \(c\) in \(z\). The reordering of posts \(c\) and \(d\) in turn breaks the \(DG\) of a transition \(d' \in w\) making it non-identical to \(DG(d', w, s)\) either by reordering it w.r.t. a dependent transition \(c' \in w\) or by exploring a dependent transition \(c' \notin w\) prior to \(d'\).
We note that if thread(r_i') = thread(r) then Γ_{1...w} would be a singleton set consisting only the pair (r_i', r), and the parent node would be identified as the node with transition pair (p_i, post(c_{event(r)})). In general, for any pair of transitions on the same thread but different handlers we identify the parent node as the node with the pair of transitions posting the events corresponding to these handlers, as a member.

If c and d identified by the scenario S2 introduced earlier, are post transitions, then the dependent transition pair (c', d') identified by this scenario becomes a transition pair in one of the nodes in the subtree that can be generated by exploring c prior to d in a transition sequence, say v_k, from state s_1'. Transition pairs belonging to the nodes of this subtree can be systematically identified by attempting to reorder c' explored in v_k w.r.t. d' by doing as described in the context of reordering transitions a_{1...w}[i] and b_{1...w}[j] belonging to the node Γ_{1...w}. By only reordering transitions in the subspace obtained when the post transition c is explored prior to post transition d, will end up breaking the DG of some transition in w thus resulting in non-dependence-covering sequences of w. If this is not the case then it implies that the transition pairs in Γ_{1...w} added prior to (c, d) can be explored in a manner consistent w.r.t. w which makes such a transition sequence dependence-covering w.r.t. w, or contain more transitions from w than in z thus breaking the constraint M4 of Construction B.11.

For each pair of transitions in the nodes of Γ-tree and the entire node itself, we assign a level called Γ-idx defined as below.

**Definition B.19.** The Γ-idx of a tree node, say Γ_i, referred as Γ-idx(Γ_i) is assigned a level same as the Γ-idx of a transition pair in Γ_{1...w} which has the highest Γ-idx among all the transition pairs in Γ_i. The Γ-idx of a pair (c, d) of dependent transitions is considered to be 0 and referred as Γ-idx((c, d)). Let (c, d) be a pair of post transitions in a Γ-tree node, say Γ_{par}, such that Γ_{kid} be the child node of Γ_{par} discovered on executing c prior to d in a transition sequence from state s_1'. Then, Γ-idx((c, d)) = Γ-idx(Γ_{kid}) + 1.

**Note.** Γ-tree essentially identifies all the pairs of transitions (dependent or posting to the same event queue) which will have to be systematically identified for reordering by EM-DPOR (by invoking FindTarget) in order to discover a dependence-covering sequence of w, assuming that EM-DPOR initially explored only the members of L from state s. Also during the process, EM-DPOR needs to adequately set up data structures such as backtrack, done and RP sets at the explored states in the subspace reachable from s_1 so as to eventually invoke FindTarget(r_i', v', r_i''o) where r_i', v' is a transition sequence constructed from Γ-tree using Construction B.17. After establishing this we can use the arguments used to prove lemmas corresponding to cases B and C (Lemma B.4 and B.6) to show that some transition executed in w prior to r_i'' or r_i' itself gets added to the backtracking set L at state s, thus contradicting the property assumed for L as per the case D. Note that all the transition sequences which can be constructed by running the Construction B.17 on the Γ-tree in Figure 12, have r_i' as their first transition. Hence by induction hypothesis H1, EM-DPOR explores dependence-covering sequences of all these transition sequences. The challenge however is to show that FindTarget gets invoked to reorder r_i' and r_i'. We achieve this by proving the following property by inducting on the Γ-idx levels of the Γ-tree nodes.

**Lemma B.20.** For each node Γ_node = \{(c_i, d_i), (c_2, d_2) ... (c_k, d_k)\} in the Γ-tree generated from the sequence z, EM-DPOR explores a sequence r_i'u whose prefix reaches a state s' such that the following properties hold.

- **P1.** For every transition pair (c_i, d_i) in Γ_node, for i ∈ [1, k], c_i = next(s', thread(c_i)) and either thread(c_i) ∈ done(s') or thread(c_i) is not enabled in s'.
- **P2.** There exists a pair (c_i, d_i) in Γ_node, for i ∈ [1, k], such that c_i is executed at s' and FindTarget(r_i', u, c_i, d_i) is invoked such that for j ∈ [i + 1, k], index(r_j', u, d_j) < index(r_j', u, c_j).
- **P3.** For each transition pair (c_i, d_i) in Γ_node, for i ∈ [1, k], where c_i and d_i are post transitions, either (c_i, d_i) ∈ RP(z') or FindTarget has been invoked to reorder c_i executed at s' and the later executed transition d_i.

**Proof.** We prove the above property by inducting on the Γ-idx level of nodes.

**Base case (Γ-idx = 0).** We present an outline on how to reason about this case. Only leaf nodes of Γ-tree belong to Γ-idx level 0. Let Γ_node = \{(c_1, d_1), (c_2, d_2) ... (c_k, d_k)\} be a leaf node. Let v_i be a transition sequence constructed over Γ-tree starting from the root and ending with a suffix where c_i is explored prior to dependent transition d_i ∈ w. Let (dependence-covering sequence of) v_i be the first transition sequence related to Γ_node to be explored by EM-DPOR. Exploration of v_i by EM-DPOR is guaranteed due to induction hypothesis H1, since the first transition of v_i is r_i' which is a transition in the set L. We will then have to show that c_i and d_i will be identified as racing transitions by the Algorithm Explore leading to invocation of FindTarget(S(v_i, d_i, c_i)). Exploring backtracking choices thus added results in exploring c_{i+1} prior to d_{i+1}. Again these will be identified as racing transitions and so on. Ultimately, FindTarget(S(v_{i+1}, c_{i+1}, d_{i+1})) gets invoked when threads of all the other c_i transitions are either in done set at the state, say s', from where c_{i-1} is executed or disabled in s'. This proves property P1 and P2. Property P3 is not relevant for the base case because a leaf node does not contain any pair of post transitions.

**Induction hypothesis.** For a node Γ_node such that Γ-idx(Γ_node) = 0, the properties P1, P2 and P3 hold.

**Induction step (Γ-idx = θ + 1).** Let Γ_node = \{(c_1, d_1), (c_2, d_2) ... (c_k, d_k)\} be a node in Γ-tree such that Γ-idx(Γ_node) = θ + 1. This indicates that the highest Γ-idx of any pair of transitions in Γ_node is θ + 1. Let (c_i, d_i) ∈ Γ_node be a pair of post transitions with its corresponding child node being Γ_i = \{(c_{i1}, d_{i1}), (c_{i2}, d_{i2}) ... (c_{ik}, d_{ik})\}. Then by our assumption on the Γ-idx of \{(c_i, d_i) and the definition of Γ-idx, we can establish that Γ-idx(Γ_i) can be at most θ.

Then, with the help of induction hypothesis we can show that FindTarget gets invoked to reorder a transition c_{ij} and later executed transition d_{ij} with suitable constraints over done and RP sets (as established by P1 and P3), resulting in the invocation of ReschedulePending by the Step 3 of FindTarget (see line 18). This in turn invokes FindTarget to reorder the post transitions c_i and d_i. Note that it is important for the RP set to be adequately set up since the HB relation computed by EM-DPOR adds edges based on RP set as well (see Definition 3.1). After backtracking choices are computed at the state from where c_i is executed, (c_i, d_i) get added to the RP set at that state. On eventually reordering c_i and d_i, c_{i+1} and d_{i+1} get reordered. Based on whether these are post or non-post transitions we can apply suitable reasoning to show how done and RP set gets populated. Ultimately, we can show that FindTarget gets invoked to reorder the last pair of transitions belonging to the set Γ_node with the corresponding done and RP sets appropriately set up as required.

**Lemma B.21.** EM-DPOR explores a dependence-covering sequence for w from state s when set L satisfies case D.
Proof. From Lemma B.18, $\Gamma$-tree exists and a $\Gamma$-tree can be generated using the transition sequence $z$ constructed as per Construction B.11 which too has been proven to exist (see Lemma B.13). From the definition of a $\Gamma$-tree the transition pair $(r'_1, r'_2)$ is the only element of the singleton set at the root of the $\Gamma$-tree generated from $z$. Then, from the property P2 established by Lemma B.20, $\text{FindTarget}(S, r'_1, u, r'_1, r'_2)$ is invoked for some transition sequence $r'_1, u$ which is a dependence-covering sequence of a sequence constructed using Construction B.17. Since $r'_2 \in w$ we can use the arguments used to prove Lemma B.4 to show that some transition executed in $w$ prior to $r'_2$ or $r'_2$ itself gets added to the backtracking set $L$ at state $s$, thus contradicting the property assumed for $L$ as per the case D. This in turn proves the existence of a dependence-covering sequence of $w$.

B.2.5 Case E

Case E assumes a subset of transitions in the backtracking set $L$ to be present in $w$ such that the first transition in $w$ from the set $L$ is of type post. This case additionally assumes that if there are non-post transitions in the set $L$ then all such transitions are dependent with some transition in $w$. This is because if there exists a non-post transition independent w.r.t. all the transitions in $w$ then this case becomes equivalent to case A which has already been shown to result in a dependence-covering sequence of $w$ (see Lemma B.2). Note that we had considered a variant of case E in case C where we had assumed the first transition in $w$ from the set $L$ to be a non-post transition. However, a post transition being the first transition in $w$ from $L$ makes the reasoning of this case very similar to that used to establish contradiction to the property of $L$ in case D.

Construction B.22. Let $z : s \xrightarrow{r'_1} s'_1 \xrightarrow{r'_2} s'_2 \ldots \xrightarrow{r'_m} s'_m$ in $\Sigma_G$, where $r'_1$ is the first transition in $w$ from the set $L$ and $v = r'_2 \ldots r'_m$, be a sequence satisfying the following constraints:

M1. Sequence $v$ consists of transitions belonging to $w$ as well as transitions outside $w$. For a transition $r'_1 \in v$, $i$, if $r'_1 \in w$ and $r'_1 \not\in \text{enabledFuture}(r'_1)$ then identicalDG($r'_1, w, z, s$). For a transition $r'_1 \in v$, if $r'_1 \in w$ and $r'_1 \not\in \text{enabledFuture}(r'_1)$ then either identicalDG($r'_1, w, z, s$) or $r'_1$ is the first transition of a shortest sequence from the state $s'_{i-1}$ comprising only of transitions which do not belong to $w$ or belong to enabledFuture($r'_1$), to be executed to make an event $e$ blocked in $s'_{i-1}$ executable such that $e$ was dequeued in $w$. Finally, for a transition $r'_1 \in v$, if $r'_1 \not\in w$ then $r'_1$ is the first transition of a shortest sequence from the state $s'_{i-1}$ comprising only of transitions which do not belong to $w$ or belong to enabledFuture($r'_1$), to be executed to make an event $e$ blocked in $s'_{i-1}$ executable such that $e$ was dequeued in $w$.

M2. There exists no extension to any prefix of $z$ which results in a transition sequence $\alpha \cdot \gamma$ such that there exists a pair of dependent transitions $c$ and $d$ with the following properties:

(a) (i) Either $c$ and $d$ are transitions in $w$ such that $c \not\in \text{enabledFuture}(r'_1)$, $\text{index}(w, d) < \text{index}(w, c)$ but $\text{index}(\gamma, c) < \text{index}(\gamma, d)$, or (ii) $c \not\in w$, $c \not\in \text{enabledFuture}(r'_1)$, $\text{index}(w, d') < \text{index}(w, c')$ but $\text{index}(\gamma', c) < \text{index}(\gamma', d)$, or (ii) $d' \in w$, $c' \not\in \text{enabledFuture}(r'_1)$, $\text{index}(w, d') < \text{index}(w, c')$

(b) Attempting to reorder $c$ and $d$ through some other extension to $\alpha$ will only result in a transition sequence $\alpha \cdot \gamma'$ which breaks the order between another pair of dependent transitions $c'$ and $d'$ such that either (i) $c', d' \in w$, $c' \not\in \text{enabledFuture}(r'_1)$, $\text{index}(w, d') < \text{index}(w, c')$ but $\text{index}(\gamma', c) < \text{index}(\gamma', d)$, or (ii) $d' \in w$, $c' \not\in \text{enabledFuture}(r'_1)$, $\text{index}(w, d') < \text{index}(w, c')$ but $\text{index}(\gamma', c) < \text{index}(\gamma', d)$.

M3. There exists a transition $r \in \text{nextTrans}(s'_m)$ such that $r$ is a transition in $w$, $r \not\in \text{enabledFuture}(r'_1)$ and $r$ is dependent with a transition $r'_1$ executed in $w$ such that (i) $r'_1 \in \text{enabledFuture}(r'_1)$ and (ii) if $r'_1 \in w$ then $r$ is executed prior to $r'_1$ in $w$.

M4. $z$ is a sequence with maximum transitions from $w$ while satisfying the constraints M1, M2 and M3.

We now present the lemma which establishes that a dependence-covering sequence of $w$ from state $s$ gets explored even when the set $L$ satisfies the property stated in case E. The proof sketch of this lemma is similar to that outlined for Lemma B.21 which reasons about the case D. However, the proof for this case will use a transition sequence $z$ constructed as per Construction B.22 to generate the $\Gamma$-tree.

Lemma B.23. EM-DPOR explores a dependence-covering sequence for $w$ from state $s$ when set $L$ satisfies case E.

B.3 Main Result

Theorem B.24. In a finite and acyclic state space $\Sigma_G$, whenever Explore (Algorithm 1) backtracks from a state $s$ to a state prior to $s$ in the search stack, EM-DPOR has explored a dependence-covering sequence for any sequence $w$ in $\Sigma_G$ from $s$, i.e., the set of transitions explored from a state $s$ is a dependence-covering set in $s$.

Proof. The proof for this theorem is by induction on the order in which states visited by EM-DPOR are backtracked, as explained in the proof strategy in Section B.1.

Base case. The first backtracked state is a state with no transitions enabled. Such a state is reached as Algorithm Explore performs a depth first search on the state space of $\Sigma_G$ which is finite and acyclic. The induction hypothesis H1 vacuously holds for such a state with no outgoing transitions.

Induction hypothesis (same as induction hypothesis H1 in Section B.1). Let $S$ be a sequence from $s_{init} \in \Sigma_G$ reaching state $s$, explored by Algorithm Explore of EM-DPOR. Let $L$ be the set of transitions explored by EM-DPOR from the state $s$. Then, for every transition sequence from a state reached on each recursive call Explore$(S, r)$, for all $r \in L$, the algorithm explores a corresponding dependence-covering sequence.

Induction step. Lemmas B.2, B.4, B.6, B.21 and B.23 prove the induction step for the exhaustive cases based on the contents of the set $L$, introduced in Section B.1.

Thus EM-DPOR explores a dependence-covering sequence for any sequence $w$ in $\Sigma_G$ from a state $s$ reached on Explore$(S)$, which in turn establishes that the set of transitions $L$ explored from $s$ is a dependence-covering set as per Definition 2.6.

C. Optimizations to EM-DPOR

This section presents two main optimizations that we have applied to EM-DPOR (see Section 3) to further prune the exploration of redundant states and transitions. Both of these optimizations refine the set of pairs of dependent transitions and thus reduce the number of pairs of transitions considered dependent. We present modifications to EM-DPOR so as to not miss exploring interesting transition sequences when using the refined notion of dependence.

C.1 Eliminate read - read Dependence

EM-DPOR algorithm presented in Section 3.3 needs to consider each pair of read operations to the same shared variable as depen-
### C.1.1 Problematic Cases

**Example C.1.** Consider an execution trace $z_1$ given in Figure 13(a), of an Android program. Among the threads $t_1$, $t_2$ and $t_3$ and $t_4$, only $t_1$ is associated with an event queue. Sequence $z_1$ has two pairs of may be co-enabled or may be reordered dependent transitions: $(r_3, r_5)$ and $(r_4, r_5)$, assuming every pair of read transitions to be independent.

Assume EM-DPOR to initially explore the sequence $z_1$ given in Figure 13(a). On exploring a prefix of $z_1$ up to $r_4$, line 3 of Algorithm 1 (Explore) identifies $r_3$ and $r_5$ to be nearest pair of dependent and may be reordered transitions executing on different handlers on the same thread. FindTarget invoked to compute backtracking choices to reorder $r_4$ and $r_5$ identifies $r_1$ and $r_2$ to be the corresponding diverging posts to be reordered. Thus, thread $t_4$ is added to backtracking set at the state $pre(z_1, r_1)$, i.e., the state from which $r_1$ is executed in sequence $z_1$. This eventually reorders $r_1$ and $r_2$ and results in exploring sequence $z_2$ (Figure 13(b)). On executing a prefix of $z_2$, transitions $r_3$ and $r_5$ are identified to be nearest dependent and co-enabled transitions. FindTarget reorders these two, eventually exploring sequence $z_3$ (Figure 13(c)). EM-DPOR does not explore any other partial orders over $r_3$, $r_4$ and $r_5$ after sequence $z_3$.

We note that, on seeing sequence $z_1$ EM-DPOR does not attempt to reorder $r_3$ and $r_5$, as $r_3$ is not the nearest reorderable dependent transition corresponding to $r_5$ in sequence $z_1$. As a result, Algorithm Explore considering a read to be only dependent with a conflicting write operation, misses exploring a sequence similar to $z$ (Figure 14), where $r_3$ reads the write performed by $r_5$ while $r_4$ does not.

**Analysis of Example C.1.** A DFS based explorer explores all paths originating at a state in the state space before backtracking to a prior state in the stack and exploring other branches. EM-DPOR is a POR algorithm which prunes some redundant transition sequences explored by a naïve DFS based state space explorer. Hence, EM-DPOR should explore all the interesting interleaving of dependent transitions originating, say at some state $s_i$, before backtracking to a prior state in the stack, say $s_j$, and exploring other branches. This is because, after backtracking to state $s_j$ from $s_i$, the subspace rooted at $s_i$ will not be visited again. Thus, any interleaving of dependent transitions that could be explored only from $s_i$ will be missed, if not explored before backtracking to $s_j$. This is pictorially depicted in Figure 15. In Figure 15 triangles represent state space reachable from the states to which the triangles are connected. Even though not shown in the figure, some of the states may overlap. The thick directed arrows depict the way in which state exploration proceeds. In case of Example C.1, EM-DPOR backtracked from a state even before exploring all the non-redundant interleaving of dependent transitions reachable from that state. This is the cause of missing some interesting sequences.

We can solve this issue with EM-DPOR without having to consider every pair of read operations to the same memory location as dependent, as follows. In the context of line 3 of Algorithm Explore, when the next transition on a thread $t$ in state $s$ is a write, its dependent transition can either be a read or a write to the same shared variable. Instead of invoking FindTarget to
Figure 16: An example illustrating challenges in reordering dependent read-write operations even when a write is attempted to be reordered with multiple prior reads.

Figure 17: An interesting sequence \( z \) corresponding to Example C.2, not explored by EM-DPOR when reads to same variable are considered independent.

reorder a write operation \( r' \) with its nearest executed dependent transition, we identify all the may be co-enabled or may be unordered dependent transitions up to nearest executed write operation, and compute backtracking choices to reorder all these identified dependent transitions with the write operation \( r' \).

**Example C.2.** Consider an execution trace \( z_1 \) given in Figure 16(a), of an event-driven multi-threaded program. Among the threads \( t_1, t_2, t_3 \) and \( t_4 \), only \( t_1 \) is associated with an event queue. Sequence \( z_1 \) has two pairs of may be co-enabled dependent transitions: \((r_3, r_4) \) and \((r_3, r_5)\), assuming any pair of read operations to be independent.

Assume EM-DPOR initially explores sequence \( z_1 \) in Figure 13(a). Algorithm Explore identifies transition pairs \((r_3, r_4)\) and \((r_3, r_5)\) as dependent, identifies backtracking choices using FindTarget, and eventually explores sequences \( z_2 \) and \( z_3 \) (Figure 17(b) and (c) respectively). However, EM-DPOR does not explore any more interleaving of transitions \( r_3, r_4 \) and \( r_5 \), even if we use the modification discussed in the analysis presented for Example C.1 (this modification computes backtracking choices to reorder \( r_3 \) with both \( r_4 \) and \( r_5 \) in sequence \( z_3 \), but is ineffective in this case). As a result, EM-DPOR misses exploring a transition sequence similar to \( z \) (Figure 17), where \( r_4 \) reads the write performed by \( r_3 \) while \( r_5 \) does not.

**Analysis of Example C.2** A scenario in case of a pure multi-threaded program analogous to that in Figure 16, is shown in Figure 18. Transitions \( r_8, r_6 \) and \( r_7 \) executed on threads \( t_1, t_2 \) and \( t_3 \) respectively in Figure 18 correspond to transitions \( r_3, r_4 \) and \( r_5 \) respectively in Figure 16. Relative order of transitions \( r_5, r_6, r_8 \) and \( r_7 \) in Figure 18(a), (b) and (c) correspond to relative order of \( r_3, r_4 \) and \( r_5 \) in Figure 16(a), (b) and (c) respectively. On exploring sequence \( z_1 \) (Figure 18), DPOR (even EM-DPOR) adds thread \( t_6 \) to backtracking set at state prior to executing \( r_1 \), when computing backtracking choices to reorder \( r_1 \) and \( r_6 \). This leads to exploring sequence \( z_4 \) (Figure 18(d)) whose analogue is not explored by EM-DPOR in case of Example C.2 when considering read operations to be independent. Thus, for EM-DPOR to explore sequence \( z \) (Figure 17), FindTarget called to reorder \( r_3 \) and \( r_5 \) in sequence \( z_1 \), should be able to identify the presence of reads to same variable between the transitions \( r_3 \) and \( r_5 \) and coming from other handlers on the same thread. FindTarget should then reorder posts of such handlers with post of \( e_2 \). However, this involves modifications to Algorithm FindTarget. Instead of modifying FindTarget, we provide minor modifications to Algorithm Explore to identify relevant event handlers to be reordered in such scenarios. In case of Example C.2, our modification identifies events \( e_1 \) and \( e_2 \) for reordering on exploring sequence \( z_3 \) (Figure 16(c)) up to the transition \( r_5 \).

In addition to the modification we discussed under analysis for Example C.1, we do the following in Algorithm Explore. After computing backtracking choices to reorder a write transition \( r' \) with its nearest executed reorderable dependent transition \( r \), we assume a temporary happens-before mapping from \( r \) to \( r' \). We invoke FindTarget to reorder \( r' \) with other conflicting read transitions up to the nearest executed conflicting write. Invoking FindTarget assuming such a happens-before relation from \( r \) to \( r' \), enables FindTarget to add tasks corresponding to \( r' \) into the set candidates computed by the steps of FindTarget (refer Algorithm 2). In scenarios similar to sequence \( z_3 \) in Example C.2, this enables FindTarget to reach Step 3, invoke ReschedulePending (line 18 in Algorithm 2) and identify post operations of relevant event handlers for reordering. The modified version of Algorithm Explore is presented as Algorithm 5.

**C.1.2 Modifications to Algorithm Explore**

Algorithm Explore (given in Algorithm 5) modified to consider any pair of reads to the same variable to be independent, is similar to Algorithm 1 presented in Section 3 except for lines 5-12 in Algorithm 5. The line numbers referred henceforth correspond to Algorithm 5. Function optType(r) finds the type of visible operation in transition \( r \). After invoking FindTarget on line 4 to compute backtracking choices and backtracking state to reorder \( next(s, t) \) with the nearest may be co-enabled or reordered dependent transition, lines 6-11 are executed only if \( next(s, t) \) has a write as visible operation.

Line 6 adds a temporary happens-before mapping from nearest dependent transition \( r_1 \) to \( next(s, t) \). Note that the happens-before relation defined in Definition 3.1 does not allow such a mapping. However, we can achieve the mapping \( i \rightarrow w.\ task(next(s, t)) \) by assuming each transition to be prefixed by a NOP operation which does not alter the state. We execute the NOP operation and add a happens-before mapping from \( r_1 \) to this NOP, which results in the required \( i \rightarrow w.\ NOP.\ task(next(s, t)) \). Line 7 computes the index of the most recent conflicting write and stores it in \( i' \). Absence or prior writes to the variable accessed by transition \( next(s, t) \),
Input: a transition sequence $w: r_1 \ldots r_n$ and a set $\mathcal{RP}$ of posts to be reordered

1. Let $s = \text{last}(w)$; \( \mathcal{RP}(s) = \mathcal{RP} \)
2. foreach thread $t$ do
   3. if $\exists i = \max \{i \in \text{dom}(w) \mid r_i$ is dependent and \( \text{may be co-enabled or reordered}$ \)
      with $\text{next}(s, t))$ and $i \notin w$. $\text{task}(\text{next}(s, t))$) \} then
         // Identify backtracking point and choice to reorder $r_i$ and $\text{next}(s, t)$
        4. $\text{FindTarget}(w, r_i, \text{next}(s, t))$
   5. if $\text{opType}(\text{next}(s, t)) = \text{WRITE}$ then
      6. Add a happens-before edge between $r_i$ and $\text{next}(s, t)$
      7. Let $i' = \max \{i' \in \text{dom}(w) \mid \text{opType}(r_{i'}) = \text{WRITE}$ \)
         and $\text{var}(r_{i'}) = \text{var}(\text{next}(s, t))\} \} \cup \{-1\}$
      8. foreach $j \in \text{dom}(w)$ \( \mid r_j$ is dependent and \( \text{may be co-enabled or reordered}$ \)
         or reordered with $\text{next}(s, t))$ and $i \notin w$. $\text{task}(\text{next}(s, t))$ and $j \geq i'$ do
           9. $\text{FindTarget}(w, r_j, \text{next}(s, t))$
   10. end
   11. Remove the happens-before edge between $r_i$ and $\text{next}(s, t)$
   12. end
   13. end
14. if $\exists t \in \text{enabled}(s)$ then
   15. Let $\text{backtrack}(s) = \{t\}$ and $\text{done}(s) = \emptyset$
      // Perform selective depth-first traversal
   16. while $\exists t \in (\text{backtrack}(s) \setminus \text{done}(s))$ do
      17. Let $r = \text{next}(s, t)$; Execute transition $r$
      18. if $r$ is a post operation then
         19. if $\exists k = \max \{k \in \text{dom}(w) \mid r_k \in \text{reorderedPosts}(r, w, r))\} \} then
            20. Add thread $t$ to backtrack$(\text{pre}(w, k))$
         21. end
         22. $\mathcal{RP} = \mathcal{RP}(s) \setminus \{(r, \cdot) \in \mathcal{RP}(s)\}$
      23. end
      24. Add $t$ to done$(s)$; Explore$(w \cdot r)$
   25. end
   26. end
   27. end

Algorithm 5: Explore

assigns $-1$ to $t'$. Lines 8–10 compute backtracking choices and backtracking states to reorder $\text{next}(s, t)$ with all the prior may be co-enabled or reordered dependent transitions up to $t'_i$ with no happens-before mapping between them. Line 11 removes the HB mapping between $t'_i$ and $\text{next}(s, t)$.

Addition of temporary HB mapping and computing backtracking information for all the relevant dependent transitions when $\text{next}(s, t)$ is a write operation, solves the issues explained through Examples C.1–C.2. In case of Example C.2, line 4 of Algorithm 5 invokes FindTarget to reorder transition $r_5$ and $r_3$ when exploring sequence $z_3$ (see Figure 16). Then, line 6 adds a temporary happens-before mapping from $r_5$ to $r_3$. Lines 8 and 9 identify $r_3$ as a relevant dependent transition to be reordered with $r_3$ and invoke FindTarget. Due to happens-before mapping from $r_5$ to $r_3$, Step 2 of FindTarget (see Algorithm 2 in Section 3) compute set candidates = $\{(t_2, \perp), (t_1, e_2)\}$. Since both threads $t_1$ and $t_2$ corresponding to candidates are in done set at the state from where $r_4$ is executed, Step 3 is reached. Step 3 of FindTarget computes pending = $\{(t_1, e_2)\}$ and invokes ReschedulePending which reorders events $e_1$ and $e_2$, eventually exploring the sequence given in Figure 17. Thus, modified Algorithm Explore enables EM-DPOR to consider a read operation to be dependent only with conflicting write operations, and thus avoids exploring some redundant transition sequences reaching same final states.

C.2 Eliminate Dependence Between Non-conflicting lock Operations

Dependence relation for an event-driven program with a state space $S_G$ and given in Definition 2.2, considers every pair of lock operations on the same lock object to be dependent. This holds even for lock acquires on different event handlers on the same thread. This is because such operations disable each other in the event-parallel transition system $\mathcal{P}_G$, introduced in Section 2.2 and are thus considered dependent in $\mathcal{P}_G$ (see Definition 2.1). When identifying dependent transitions in different event handlers on the same
thread, the dependence relation (see Definition 2.2) defined for \( S_C \) uses the dependences identified over \( P_C \). Hence, lock acquires on a common lock by different event handlers on the same thread will be considered dependent in \( S_C \) as well. We assume each lock acquired within an event handler to be released within the same event handler. This is a reasonable assumption as some widely used programming language features like Java’s synchronized construct for nested acquire and release of lock objects support this assumption. Also, acquiring and releasing locks in different event handlers can be hard to reason and problematic if the event handler acquiring the lock is not guaranteed to always precede the handler releasing the lock. With this assumption, any pair of lock operations on the same lock object executed on different event handlers on the same thread can never contend or deadlock with each other, as (1) operations executing on the same thread are never co-enabled, (2) each handler is assumed to execute to completion before the execution of another handler, and (3) a lock acquired in an event handler is released within the same event handler as per our assumption. Hence, lock acquires from different event handlers on the same thread cannot simultaneously involve in interesting states like deadlocks. We thus consider lock operations executed on different event handlers on the same thread, even if acquiring the same lock object, to be independent. Consequently, we consider any unlock operation \( r \) to be independent with subsequent lock operations in other event handlers on the same thread as \( r \).

However in theory, considering operations acquiring the same lock \( l \) in two different handlers \( h \) and \( h' \) on the same thread to be independent is problematic — especially if the same shared variable is accessed (read-write / write-write) by some transitions, say \( r \) and \( r' \), in the critical sections protected by the lock \( l \) in \( h \) and \( h' \) respectively, resulting in exploring different states on different ordering of \( h \) and \( h' \). This is because \( r \) and \( r' \) accessed within critical sections protected by the same lock in \( h \) and \( h' \) respectively, are trivially considered independent in \( P_C \) (see Definition 2.1) as they are never co-enabled. Hence, \( r \) and \( r' \) may be considered independent in \( S_C \) too. However, exploring different ordering of \( h \) and \( h' \) is essential to explore possibly different states due to conflicting accesses \( r \) and \( r' \). In such scenarios, considering lock acquires corresponding to critical sections of \( r \) and \( r' \) to be dependent enables a POR technique to reorder \( h \) and \( h' \) even though the actual conflicting transitions \( r \) and \( r' \) are not marked dependent. This will not be possible with our selective lock dependence proposed above. However in practice, considering all pairs of lock acquires on different handlers on the same thread to be independent does not result in aforementioned problem. This is because, EM-DPOR over-approximates the set of pairs of dependent transitions by considering pairs of transitions (a) making conflicting accesses to shared variables with or without holding a protective lock, or (b) enabling/disabling each other, to be dependent. Hence, lock operations on the same object executed on different handlers on the same thread need not be considered dependent in practice, to enable EM-DPOR to reorder their respective handlers in case they access the same shared variable in their critical sections. In the rest of the section we refer to this over-approximated dependence relation but additionally considering all the pairs of lock operations and unlock-lock operations executed on different handlers of the same thread to be independent, as modified dependence relation.

The modified dependence relation preserves dependence between pairs of lock operations and unlock-lock operations on same lock objects and executed on different threads. This is because, a lock acquire disables all other co-enabled lock operations contending for the same lock, and unlock enables lock operations waiting for the same lock; making such transitions dependent due to condition 2 in Definition 2.2. Similar to the proof for Theorem 2.9.1, we can prove that a dependence-covering state space \( S_R \) of an Android program \( A \) obtained by the modified dependence relation, preserves all deadlock cycles seen in the original state space \( S_C \) of \( A \). This is because, a dependence-covering sequence \( u \) of a
transition sequence \( w \) must preserve the relative order between all
the pairs of lock operations acquiring or contending for the same
lock object and executing on different threads in \( w \), because lock
operations are considered dependent. Thus, if \( w \in S_{DC} \) reaches a
deadlock cycle \((DC, \rho)\) then \( w \) being its dependence-covering se-
quence reaches the same deadlock cycle, as \( w \) must preserve the rel-
ative order of acquiring locks among threads involved in the dead-
lock cycle.

Modifications to EM-DPOR to Incorporate Modified
Dependence Relation

EM-DPOR should be able to explore all valid interleaving of op-
erations acquiring the same lock object and executed on differ-
ent threads, even when using modified dependence relation. Ex-
ample C.3 demonstrates that achieving this requires some modifi-
cations to EM-DPOR similar to those introduced in Algorithm 5
described in Section C.1.2.

\textbf{Example C.3.} Consider an execution trace \( z \) explored by EM-
DPOR and given in Figure 19(a), of an event-driven multi-threaded
program. Among the threads \( t_1, t_2, t_3 \) and \( t_4 \), only \( t_1 \) is attached
with an event queue. EM-DPOR is assumed to use modified depen-
dence relation, thus making transition pairs \((r_7, r_{10})\) and \((r_9, r_{10})\)
independent. Sequence \( z \) has two pairs of may be co-enabled
dependent transitions with no happens-before mapping between
them: \((r_3, r_7)\) and \((r_3, r_{10})\). Note that EM-DPOR does not in-
voke \texttt{FindTarget} on transition pairs \((r_6, r_9)\) and \((r_4, r_{11})\) as they
are ordered by happens-before due to happens-before mapping be-
tween \( r_9 \rightarrow r_7 \) and \( r_5 \rightarrow r_{10} \) respectively.

On exploring sequence \( z \) Algorithm \texttt{Explore} identifies transi-
tion pairs \((r_3, r_7)\) and \((r_3, r_{10})\) as dependent, identifies back-
tracking choices using \texttt{FindTarget}, and eventually explores se-
quences \( z_2 \) and \( z_3 \) (Figure 19(b) and (c) respectively). However,
EM-DPOR does not explore any more interleaving of transitions
\( r_3 \rightarrow r_7 \rightarrow r_{10} \) and thus misses exploring a sequence similar to \( z \)
(Figure 20), where the locking order of lock 1 is different com-
pared to that explored by sequences \( z_1, z_2 \) and \( z_3 \). Also, \( z \) reaches
a new state (compared to states reached by \( z_1, z_2 \) and \( z_3 \)) where
variables \( x \) and \( y \) are assigned values 1 and 5 respectively. Even if
Algorithm \texttt{Explore} is modified to compute backtracking choices to
reorder a lock operation with all the prior executed \texttt{may be co-
enabled} lock operations with no happens-before relation (instead
of only the nearest lock operation), EM-DPOR will not be able to
explore sequence \( z \).

\textbf{Analysis of Example C.3} The scenario represented in Exam-
ple C.3 is similar to that in Example C.2. Specifically, in Exam-
ple C.3 lock in transition \( r_3 \) is dependent with transitions \( r_7 \) and \( r_{10} \) executed in different handlers on the same thread while \( r_7 \) and
\( r_{10} \) are mutually independent, similar to the way \texttt{write} in transi-
tion \( r_3 \) is dependent with \texttt{read} operations in \( r_4 \) and \( r_5 \) executed
in different handlers on the same thread in Example C.2. Hence,
we propose modifications to Algorithm \texttt{Explore} similar to those
explained in Section C.1.

In the initial phase of Algorithm \texttt{Explore} which invokes
\texttt{FindTarget}, we do the following if \( \textit{next}(s,t) \) contains a
lock operation. We compute backtracking choices (by invoking
\texttt{FindTarget}) to reorder \( \textit{next}(s,t) \) with the nearest \texttt{may be co-
enabled} (i.e., not executed on thread \( t \)) lock operation, say \( r \), ac-
quiring the same lock object. If \( r \) is executed in an event handler
(i.e., \( r \) is executed on a thread with an event queue), we add a
temporary happens-before mapping from \( r \) to \( \textit{next}(s,t) \). We then
compute backtracking choices and backtracking states to reorder
\( \textit{next}(s,t) \) with all the prior lock operations executed in various
handlers on \( r \)'s thread which do not have a happens-before map-
ping with \( \textit{next}(s,t) \), till we find a lock operation, say \( r' \), exe-
cuted on a thread other than \texttt{thread}(\( r' \)) such that index of \( r' \) is
lesser than the index of the lock operations on \( r \)'s thread reodered
with \( \textit{next}(s,t) \). After computing backtracking choices to reorder
\( \textit{next}(s,t) \) with all the relevant lock operations, we remove the
temporary happens-before mapping between \( r \) and \( \textit{next}(s,t) \) and
continue with the remaining steps in \texttt{Explore}.