Design and Experimental Verification of a Novel Error-Backpropagation-Based Background Calibration for Time Interleaved ADC in Digital Communication Receivers

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Abstract—A novel background calibration technique for Time-Interleaved Analog-to-Digital Converters (TI-ADCs) is presented in this paper. This technique is applicable to equalized digital communication receivers. As shown by Tsai et al. [1] and Luna et al. [2], in a digital receiver it is possible to treat the TI-ADC errors as part of the communication channel and take advantage of the adaptive equalizer to compensate them. Therefore calibration becomes an integral part of the channel equalization. No special purpose analog or digital calibration blocks or algorithms are required. However, there is a large class of receivers where the equalization technique cannot be directly applied because other signal processing blocks are located between the TI-ADC and the equalizer. The technique presented here generalizes earlier works to this class of receivers. The error backpropagation algorithm, traditionally used in machine learning, is applied to the error computed at the receiver slicer and used to adapt an auxiliary equalizer adjacent to the TI-ADC, called the Compensation Equalizer (CE). Simulations using a dual polarization optical coherent receiver model demonstrate accurate and robust mismatch compensation across different application scenarios. Several Quadrature Amplitude Modulation (QAM) schemes are tested in simulations and experimentally. Measurements on an emulation platform which includes an 8 bit, 4 Gs/s TI-ADC prototype chip fabricated in 130nm CMOS technology, show an almost ideal mitigation of the impact of the mismatches on the receiver performance when 64-QAM and 256-QAM schemes are tested. An absolute improvement in the TI-ADC performance of $\sim$15 dB in both SNDR and SFDR is measured.

Index Terms—Background calibration, error backpropagation, optical coherent receiver, TI-ADC, TI-ADC mismatch calibration.

I. INTRODUCTION

This paper proposes a novel background calibration technique for Time-Interleaved Analog-to-Digital Converters (TI-ADCs) used in equalized digital communication receivers. It generalizes a previously proposed technique [1]–[3]. Current and emerging digital receivers for ultra high-speed communication systems [4]–[10] require large bandwidth, high sampling rate Analog-to-Digital Converters (ADCs).

The TI-ADC [11], [12] has been the technique predominantly used to meet the demanding sampling rate and bandwidth requirements of high-speed transceivers.

The performance of TI-ADCs is affected by mismatches among the interleaves [13], [14]. Mismatches of sampling time, gain, bandwidth, as well as DC offset, are the most common impairments. Many calibration techniques have been proposed in the literature. Please see [15]–[30] and references therein for a thorough review and discussion.

Calibration techniques for general purpose TI-ADCs in general require dedicated calibration blocks and algorithms. On the other hand, several authors [1]–[3] have shown that in the special case of an equalized digital receiver, it is possible to treat the TI-ADC errors as integral part of the communication channel and take advantage of the already existing adaptive equalizer to compensate them. Therefore calibration becomes an integral part of the channel equalization. No special purpose analog or digital calibration blocks or algorithms are required.

Equalizer-based compensation can compensate static as well as frequency-dependent errors such as bandwidth limitations and bandwidth or frequency response mismatches among the interleaves of the ADC. Because the equalizer is adaptive, it also compensates time-dependent effects such as those caused by temperature and voltage variations, or by aging. Therefore, equalization becomes the TI-ADC compensation technique of choice in digital communication receivers.

Tsai et al. [1] provide a thorough description of the equalization technique and its advantages. However, there is a large class of receivers where this technique cannot be directly applied because other signal processing blocks are located between the TI-ADC and the equalizer. A block diagram of a typical receiver for high-speed digital communications is shown in Fig. 1.

An effective compensation of the TI-ADC errors has been achieved in the referenced works [1]–[3] because the main receiver equalizer, or Feedforward Equalizer (FFE) is immediately located after the TI-ADC (in other words, the Signal Pre-Processing block of Fig. 1 is not present). Hence, the FFE can access and directly compensate the impairments of the
different interleaves. Also, the slicer error carries information about the impairments of the individual interleaves and therefore the FFE adaptation algorithm can drive its coefficients to a solution that jointly compensates the channel and the TI-ADC impairments. Unfortunately, the application of Tsai’s technique to most types of receivers (e.g., for coherent optical communications) has been limited by the presence of signal pre-processing blocks (e.g., Timing Recovery (TR), Carrier Recovery (CR), or Bulk Chromatic Dispersion Equalizer (BCD)). These blocks cause signal components associated with different interleaves of the TI-ADC to be combined in a way that makes the use of the FFE unsuitable to compensate them.

The main contribution of this work is a new background technique [31] that overcomes the aforementioned limitations, and is especially well suited for complex digital receivers. The basic idea consists in the use of an auxiliary, low complexity adaptive equalizer, called the Compensation Equalizer (CE), to compensate the mismatches of the TI-ADC. Slicer error components associated with different interleaves are also combined by the signal pre-processing blocks. Thus, the slicer error is not directly applicable to adapt the CE.

In this work we propose to adapt the CE using a post processed version of the error at the slicer of the receiver. The post processing is based on the backpropagation algorithm [32], widely used in machine learning applications [33]. Its main characteristic is that, in a multi-stage processing chain where several cascaded blocks have adaptive parameters, it is able to determine the contribution to the error generated by each one of these blocks and their associated parameters for all the stages. Backpropagation is used in combination with the Stochastic Gradient Algorithm (SGD) to adjust the coefficients of the CE in order to minimize the slicer Mean Squared Error (MSE). The use of the CE in combination with the backpropagation algorithm results in robust, fast converging background calibration. As we shall show, this proposal is not limited to the compensation of individual TI-ADCs (which is the case for most calibration techniques), but it extends itself to the entire receiver Analog Front End (AFE), enabling the compensation of impairments such as time skew, quadrature, and amplitude errors between the in-phase and the quadrature components of the signal in a receiver based on Phase Modulation (PM) or QAM.

Because ultrafast adaptation is usually not needed, the backpropagation algorithm can be implemented in a highly subsampled hardware block which does not require parallel processing. Therefore, the implementation complexity of the proposed technique is low, as will be discussed in detail. Although the technique presented here is general and can be used in digital receivers for different applications, the primary example in this paper is a receiver for coherent optical communications. State-of-the-art coherent optical receivers operate at symbol rates around 96 Giga-Baud (GBd) and require ADC sampling rates close to 150 GS/s and bandwidths of about 50 GHz. In the near future symbol rates will increase to 128–150 GBd or higher, requiring bandwidths in the range of 65–75 GHz and sampling rates in the 200–250 GS/s range. High-order Quadrature Amplitude Modulation (QAM) schemes (e.g., 64-QAM, 256-QAM and higher) will be deployed to increase spectral efficiency [34]. High-order modulation schemes increase the resolution and overall performance requirements on the ADC.

The benefits of the proposed technique are experimentally verified using 64-QAM and 256-QAM schemes. The core of the experimental setup is an 8 bit, 4 GS/s TI-ADC test chip [35].

The rest of this paper is organized as follows. Section II presents a discrete time model of the TI-ADC system in a Dual-Polarization (DP) optical coherent receiver. The error backpropagation based adaptive CE is introduced in Section III. Simulation results are presented and discussed in Section IV. The experimental evaluation is performed in Section V and conclusions are drawn in Section VI.

II. SYSTEM MODEL OF HIGH-SPEED DIGITAL RECEIVERS BASED ON TI-ADC

Communication channels of interest in this work include, among others: i) wireline, ii) wireless, or iii) optical. The primary example of application of the backpropagation-based compensation technique considered in the next sections is a DP coherent optical receiver [41]-[46]. However, it can be used in any high-speed digital receiver with minor modifications. A block diagram of the Optical Front End (OFE) and the AFE for a DP coherent receiver is shown in Fig. 2. The optical input signal is decomposed by the OFE into four signals, the in-phase and quadrature (I/Q) components of the horizontal and vertical (H/V) polarizations. Photodetectors are used to convert the optical signals to photocurrents which are amplified by Trans-Impedance Amplifiers (TIAs). Then, the AFE acquires the electrical signals and translates them to the digital domain. Digital receivers with a certain degree of oversampling (e.g., $T_s = \frac{T}{2}$ where $T_s$ and $T$ are the sampling and symbol periods, respectively) are used to compensate...
of this paper.

Let \(a_k^{(P)} = a_k^{(P,I)} + j a_k^{(P,Q)}\) be the transmitted QAM symbol in polarization \(P \in \{H,V\}\) at time instant \(k\). The Chromatic Dispersion (CD) and Polarization-Mode Dispersion (PMD) effects of an optical fiber link can be modeled as a \(2 \times 2\) Multiple-Input Multiple-Output (MIMO) complex-valued channel \([36]\) encompassing four complex filters with impulse responses \(h_{m,n}(t)\) where \(m, n = 1, 2\). For a comprehensive description of the effects of the optical channel, please see \([37]\).

Then, the noise-free electrical signals provided by the optical demodulator in the receiver can be expressed as \([36]\)

\[
s^{(H)}(t) = s^{(H,I)}(t) + j s^{(H,Q)}(t) = e^{j \omega_0 t} \left[ \sum_k a^{(H)}_k h_{1,1}(t - kT) + a^{(V)}_k h_{1,2}(t - kT) \right],
\]

\[
s^{(V)}(t) = s^{(V,I)}(t) + j s^{(V,Q)}(t) = e^{j \omega_0 t} \left[ \sum_k a^{(H)}_k h_{2,1}(t - kT) + a^{(V)}_k h_{2,2}(t - kT) \right],
\]

where \(\omega_0\) is the optical carrier frequency offset (or frequency difference between the transmitter and the local oscillator) and \(1/T\) is the symbol rate.

A. AFE and TI-ADC Discrete-Time Model

A discrete-time model for the AFE and the TI-ADC system of Fig. 2 with their impairments is introduced in this section. A simplified representation of the analog path for one component \(C \in \{I,Q\}\) in a given polarization \(P \in \{H,V\}\) is shown in Fig. 3. The response of the electrical interconnections between the optical demodulator and the TIA, the TIA response itself, and any other components in the signal path up to a TI-ADC system is represented with a filter with impulse response \(c^{(P,C)}(t)\). Time delay or skew between components \(I\) and \(Q\) of a given polarization \(P\) is caused by mismatches between \(c^{(P,I)}(t)\) and \(c^{(P,Q)}(t)\), and degrades the receiver performance. As we shall show, the proposed background calibration algorithm is able to compensate not only the mismatches of the TI-ADC, but also the I/Q skew, the quadrature and amplitude errors, and other impairments among the signal paths.

Blocks \(f_{m}^{(P,C)}(t)\) \((m = 0, \cdots, M-1)\) model the independent responses of the \(M\) Track and Hold (T&H) circuits in an \(M\)-channel TI-ADC system \(M/T\)\(s\) Each one of the \(M\) interleaved channels is sampled every \(M/f_s = M/T_s\) seconds with a proper sampling phase. Sampling time errors and the DC offsets are represented with \(\delta_{m}^{(P,C)}\) and \(\delta_{m}^{(P,C)}\), respectively. Every path gain/attenuation is modeled by

\[
\gamma_{m}^{(P,C)} = 1 + \Delta_{m}^{(P,C)},
\]

where \(\Delta_{m}^{(P,C)}\) is the gain error.

Fig. 3. Analog-front-end model for polarization \(P \in \{H,V\}\) and component \(C \in \{I,Q\}\) in a TI-ADC-based DP coherent optical receiver.

The quantizer is modeled as additive white noise with uniform distribution since the resolution of the ADC is considered sufficiently high. Also, at high-frequency (i.e., \(1/T_s\)), the DC offsets \(\delta_{m}^{(P,C)}\) generate an \(M\)-periodic signal denoted as \(\delta^{(P,C)}[n]\) such that \(\delta^{(P,C)}[n] = \delta^{(P,C)}[n + M]\) with

\[
\delta^{(P,C)}[m] = \delta_{m}^{(P,C)}, \quad m = 0, \cdots, M - 1.
\]

The digitized high-frequency samples can be written as (see Appendix A)

\[
y^{(P,C)}[n] = \sum_{l} \tilde{h}_{m}^{(P,C)}[l] s^{(P,C)}[n - l] + \delta^{(P,C)}[n] + q^{(P,C)}[n],
\]

where \(\tilde{h}_{m}^{(P,C)}[l]\) is the impulse response of a time-varying filter, which is an \(M\)-periodic sequence such \(\tilde{h}_{m}^{(P,C)}[l] = \tilde{h}_{m}^{(P,C)}[l]\) defined by (29), and \(q^{(P,C)}[n]\) is the quantization noise.

B. Compensation of AFE Mismatch and TI-ADC Impairments

Errors and mismatches of the TI-ADC can be compensated by using digital finite impulse response (FIR) filters applied to each interleaved branch. In the case of a communication receiver, the digitized signal could be applied to a time-varying equalizer immediately following the TI-ADC (see \([1]\) for more details). The practical implementation of this periodically time-varying equalizer is briefly addressed in Section III-A, and in more detail in \([3]\).

Similarly to what was done in previous works \([1,3,20]\), the backpropagation-based architecture introduced in this paper we propose to adaptively compensate the TI-ADC mismatch, after the mitigation of the offset, using a filter with an \(M\)-periodic time-varying impulse response:

\[
x^{(P,C)}[n] = \sum_{l=0}^{L_q-1} \tilde{z}_{m}^{(P,C)}[l] w^{(P,C)}[n - l],
\]

where \(\tilde{z}_{m}^{(P,C)}[l]\) is the \(M\)-periodic time-varying impulse response of the compensation filter (i.e., \(\tilde{z}_{m}^{(P,C)}[l] = \tilde{z}_{n+M}[l]\)), \(L_q\) is the number of taps of the compensation filters, and \(w^{(P,C)}[n]\) is the DC offset-free signal given by

\[
w^{(P,C)}[n] = y^{(P,C)}[n] - \delta^{(P,C)}[n],
\]
III. ERROR-BACKPROPAGATION-BASED COMPENSATION OF AFE AND TI-ADC IMPAIRMENTS IN DIGITAL RECEIVERS

A block diagram of the AFE+TI-ADC in a DP optical coherent receiver with the CE for mitigating the effects of both AFE mismatches and TI-ADC impairments.

**Figure 4.** Block diagram of a DP optical coherent receiver with the CE for mitigating the effects of both AFE mismatches and TI-ADC impairments.

with  \( \tilde{\sigma}^{(P,C)}[n] \) being the \( M \)-periodic offset sequence estimation. The combination of the offset compensation blocks and the compensation filters  \( \tilde{g}^{(P,C)}[l] \) constitutes the CE (see Fig. 4).

The adaptation algorithm of the CE as proposed in [1] or [2] cannot be implemented in coherent optical communication receivers. This is because of the presence of several signal pre-processing blocks placed between the CE and the slicers, such as the Bulk Chromatic Dispersion Equalizer (BCD) or the MIMO FFE that compensates PMD [4]. Thus, since the slicer errors are not available at the outputs of the CE, a proper strategy has to be defined to adapt the CE response. On the other hand, it is worth to highlight that mismatches between the \( I \) and \( Q \) signal paths cannot be mitigated using adaptive compensation techniques based on a reference ADC, such as [20]. In the next section, we apply the backpropagation technique to adapt the CE coefficients.

A parallel implementation of the Compensation Equalizer

**A. Parallel Implementation of the Compensation Equalizer**

Before explaining the adaptation of the CE coefficients  \( \tilde{g}_m^{(i)}[l] \), it is important to highlight that no additional complexity is added to implement the CE with independent responses multiplexed in time when they are implemented as a parallel architecture. Let  \( g_m^{(i)}[l] \) with  \( i = 1, \cdots, 4 \) be the filter impulse response  \( \tilde{g}_m^{(i)}[l] \) in one period defined as

\[
g_m^{(i)}[l] = \tilde{g}_m^{(i)}[l], \quad m = 0, \cdots, M-1, \quad \text{(8)}
\]

where  \( l = 0, \cdots, L_g-1 \) and  \( n_d \) is an arbitrary time index multiple of  \( M \). Thus, notice that the application of the CE in coherent receivers (see Fig. 4) comprises 4 sets of real valued Finite Impulse Response (FIR)  \( g_n^{(i)}[l] \) with  \( i = 1, 2, 3, 4, m = 0, \cdots, M-1, \) and  \( l = 0, \cdots, L_g-1 \).

In high speed optical communication applications, the use of parallel implementations is mandatory. Typically, a parallelism factor on the order of 128 or higher is adopted. Furthermore, given the number of interleaves of the TI-ADC  \( M \), the parallelism factor  \( P \) can be selected to be a multiple of  \( M \), i.e.,  \( P = q \times M \) with  \( q \) an integer. In this way, the different time multiplexed taps are located in fixed positions of the parallel implementation, and we do not incur significant additional complexity when compared to a filter with just one set of coefficients (see [2] for more details). The complexity of the resulting filter is similar to that of the I/Q-skew compensation filter already present in current coherent receivers [4]. Moreover, the typical skew correction filter can be replaced by the CE without adding significant penalties in area or power since our proposal is also able to correct time skew.

**B. All Digital Compensation Architecture**

The filter coefficients of the impulse response in (8) are adapted using the slicer error at the output of the receiver DSP block. We denote  \( e_k^{(j)} \) as the slicer error, defined as

\[
e_k^{(j)} = u_k^{(j)} - \hat{u}_k^{(j)}, \quad j = 1, \cdots, 4, \quad \text{(9)}
\]

where  \( u_k^{(j)} \) and  \( \hat{u}_k^{(j)} \) are the  \( k \)-th slicer input and output, respectively (see Fig. 4).  \( u_k^{(j)} \) is also called the detected symbol. Since the slicer operates at 1/\( T \) sampling rate, a subsampling of  \( T/T_s \) is needed after the receiver DSP block. Then, the total squared error at the slicer at time instant  \( k \) is defined as

\[
E_k = \sum_{j=1}^{4} |e_k^{(j)}|^2. \quad \text{(10)}
\]

Let  \( E\{E_k\} \) be the MSE at the slicer with  \( E\{\cdot\} \) denoting the expectation operator. In this work we iteratively adapt the real coefficients of the CE defined by (8) by using the Least Mean Squares (LMS) algorithm, in order to minimize the MSE at the slicer:

\[
g_m^{(i),+1} = g_m^{(i)} - \beta \nabla_{g_m^{(i)}} E\{E_k\}, \quad \text{(11)}
\]

**References**: The optical coherent receivers can see [4], [5], [9] and references therein.
where $i = 1, \ldots, 4$; $m = 0, \ldots, M - 1$; $p$ denotes the number of iteration, $g_{m,p}^{(i)}$ is the $L_g$-dimensional coefficient vector at the $p$-th iteration given by

$$g_{m,p}^{(i)} = \left[ g_{m,p}^{(i)}[0], g_{m,p}^{(i)}[1], \ldots, g_{m,p}^{(i)}[L_g - 1] \right]^T, \quad (12)$$

where $\beta$ is the adaptation step, and $\nabla g_{m,p}^{(i)} E \{ E_k \}$ is the gradient of the MSE with respect to the vector $g_{m,p}^{(i)}$.

We highlight that the key obstacle of the previous analysis is the computation of the MSE gradient since $E_k$ is not the error at the output of the CE block. To address this problem, we propose the use of the backpropagation algorithm, extensively used in machine learning applications [32], [33]. By applying this algorithm to the slicer errors, we are now able to generate the error samples needed to adapt the coefficients of the filters, as expressed in (11). Consequently, the gradient $\nabla g_{m,p}^{(i)} E \{ E_k \}$ can be estimated as usual in the traditional LMS algorithm, using these backpropagated errors.

**C. Error Backpropagation**

Without loss of generality, we consider that the receiver DSP block can be modeled as a real time-varying $4 \times 4$ MIMO T/2 fractionally spaced equalizer (i.e., $T_s = T/2$), which is able to compensate CD and PMD among other optical fiber channel effects. Then, we can write the downsampled output of the $T/2$ receiver DSP block (see Fig. 5) as

$$u_k^{(j)} = \sum_{i=1}^{4} \sum_{l=0}^{L_g-1} \Gamma_{2k}^{(j)(i)}[l] x^{(i)}[2k - l], \quad j = 1, \ldots, 4, \quad (13)$$

where $\Gamma_{2k}^{(j)(i)}[l]$ is the time-varying impulse response of the filter with input $i$ and output $j$, $L_g$ is the number of coefficients of the filter, whereas $x^{(i)}[l]$ is the signal at the DSP block input $i$ given by (6), i.e.,

$$x^{(i)}[n] = \sum_{l'=0}^{L_g-1} g_{[n,l']}^{(i)} w^{(i)}[n-l'], \quad i = 1, \ldots, 4, \quad (14)$$

where $g_{m}^{(i)}$ is the impulse response defined by (3), $\lfloor . \rfloor_M$ denotes the modulo $M$ operation, and $w^{(i)}[n]$ is the DC compensated signal given by (7).

The gradient of the MSE, $\nabla g_{m,p}^{(i)} E \{ E_k \}$ can be replaced by a noisy estimation $\nabla g_{m,p}^{(i)} E_k$, as usual with the SGD based adaptation. As we show in Appendix A, an instantaneous gradient of the squared error (10) can be expressed as

$$\nabla g_{m,p}^{(i)} E_k = \alpha e^{(i)}[m + kM] w^{(i)}[m + kM], \quad (15)$$

where $\alpha$ is a certain constant, $w[n]$ is a vector with $L_g$ input samples of the CE, i.e.,

$$w^{(i)}[n] = \left[ w^{(i)}[n], w^{(i)}[n-1], \ldots, w^{(i)}[n-L_g+1] \right]^T,$$

where the backpropagated error, $\hat{e}^{(i)}[n]$ is expressed as

$$\hat{e}^{(i)}[n] = \sum_{j=1}^{4} \sum_{l=0}^{L_g-1} \Gamma_{n+l}^{(j)(i)}[l] e^{(j)}[n+l], \quad (17)$$

with $e^{(j)}[n]$ being the oversampled slicer error generated from the slicer error at the baud-rate $e_k^{(j)}$ in (9) as

$$e^{(j)}[n] = \begin{cases} e_{n/2} & \text{if } n = 0, \pm 2, \pm 4, \ldots \\ 0 & \text{otherwise} \end{cases}. \quad (18)$$

Then, we can derive an all-digital compensation scheme using an adaptive CE with coefficients updated as

$$g_{m,p+1}^{(i)} = g_{m,p}^{(i)} - \mu \nabla g_{m,p}^{(i)} E_k, \quad (19)$$

where $\mu = \alpha \beta$ is the adaptation step-size. Moreover, it is possible to estimate the DC offsets in the input samples, using the backpropagated error defined in (17), as follows

$$o_{m+1}^{(i)} = o_{m}^{(i)} - \mu_o \hat{e}^{(i)}[n + m], \quad m = 0, \ldots, M - 1, \quad (20)$$

where $o_{m}^{(i)}$ is the DC offset sequence estimation in one period (see (7)) at the $p$-th iteration, and $\mu_o$ is the step-size of the DC offset estimator.

In order to avoid possible instability due to competition between the CE and any adaptive DSP blocks in $\Gamma_{2k}^{(j)(i)}[l]$ (e.g., the FFE), an adaptation constraint must be included. This can be achieved by limiting one of the $4M$ sets of the CE coefficients to only be a time delay line. For example, $g_0^{(0)}[l] = \delta_{l,l_d}$ where $l = 0, \ldots, L_g - 1$ and $l_d = \frac{L_g+1}{2}$ ($L_g$ is assumed odd).

The coefficient updates given by (19) and (20) do not need to operate at full rate, because channel impairments change slowly over time. Then, subsampling can be applied. In this way, the implementation complexity can be significantly reduced. Further complexity reduction is enabled by: i) storing the algorithms once they have converged, and/or ii) implementing them in firmware in an embedded processor, typically available in coherent optical transceivers.

**D. Mixed-Signal Calibration Architecture**

The Error Backpropagation (EBP) algorithm just described also enables a mixed-signal calibration technique. A block diagram of this calibration is depicted in Fig. 6. With this
variant, sampling phase, gain, and DC offsets are adjusted prior to the ADC [4] by using the gradient of the backpropagated slicer error. With this calibration approach the DC offsets are compensated using (20), similar to the full digital variant. The gain coefficient is updated using

\[ z_{m,p+1}^{(i)} = z_{m,p}^{(i)} - \mu \varepsilon^{(i)}[m+kM]w^{(i)}[m+kM], \quad \forall k, \quad (21) \]

where \( m = 0, \ldots, M - 1 \) and \( i = 1, \ldots, 4 \). Finally, the sampling phase can be calibrated using the MMSE timing recovery algorithm [40], since the backpropagated slicer error is available at the ADC outputs, i.e.,

\[ z_{m,p+1}^{(i)} = z_{m,p}^{(i)} - \mu \varepsilon^{(i)}[m+kM] \times \left( w^{(i)}[m+kM+1] - w^{(i)}[m+kM-1] \right), \quad \forall k \]

with \( m = 0, \ldots, M - 1 \). The calibration algorithm has the advantage of tuning analog elements already present in most implementations of the TI-ADC [23], [41], [42]. For example, the clock sampling phase is adjusted with variable delay lines, gain and offset can be corrected in the comparator or with Programmable Gain Amplifiers (PGA), if required.

IV. SIMULATION RESULTS

In this section the proposed backpropagation based mismatch compensation technique is tested using simulations. The simulation setup is shown in Fig. 7. The simulated parameters are summarized in Table I. TI-ADC mismatches are modeled as Uniformly Distributed Random Variables (UDRV). The electrical analog path responses [26] are modeled by first-order low-pass filters with 3dB-bandwidth defined by

\[ B^{(i)}_m = B_0 + \Delta B^{(i)}_m, \quad i = 1, 2, 3, 4; \quad m = 0, \ldots, M - 1, \quad (23) \]

where \( B_0 \) is the nominal BW and \( \Delta B^{(i)}_m \) is the BW mismatch. Sampling phase errors and I/Q time skew are modeled by Lagrange interpolation filters. The I/Q time skew of each polarization is evenly distributed between its corresponding components (see Fig. 7). Errors of the TI-ADC are modeled as detailed in Section II-A. In particular, time skews among the interleaves are modeled using Lagrange interpolation filters (not to be confused with those used to model the I/Q skews). We consider a DP optical coherent system with a 64-QAM modulation scheme, and a symbol rate of \( 1/T = 96 \) Gbd. Raised cosine filters with roll-off factor 0.10 for transmit pulse shaping are simulated (i.e., the nominal BW of the channel filters is \( B_0 = 1.1 \times 96 \text{GHz} \approx 53 \text{GHz} \)). The Optical Signal-to-Noise Ratio (OSNR) is set to that required to achieve a Bit-Error-Rate (BER) of \( \sim 1 \times 10^{-3} \) (see [43], [44] for the definition of OSNR). The oversampling factor in the DSP blocks is \( T/T_s = 2 \). The fiber length is 100 km with 10 ps of Differential Group Delay (DGD) and 1000 ps² of Second-Order PMD (SOPMD). Rotations of the State of Polarization (SOP) of 2 kHz and 10 kHz are included at the transmitter and receiver, respectively. Please see [57] for a comprehensive description of the aforementioned optical channel parameters. TI-ADCs with 8-bit resolution, 192 GS/s sampling rate, and \( M = 16 \) are simulated. The number of taps of the digital compensation filters is \( L_g = 7 \).

A. Montecarlo Simulations of the Adaptive CE

Each Montecarlo test consists of 500 cases where the impairment parameters are obtained from a UDRV random number generator. Figs. 8 and 9 show the histograms of the BER for the receiver with and without the CE in the presence of sampling phase errors, gain errors, I/Q time skew, and BW mismatches. Only one effect is exercised in each case. Results for sampling phase and gain errors uniformly distributed in the interval \( \delta^{(i)}_m \in [\pm 0.075]T \) and \( \Delta B^{(i)}_m \in [\pm 0.15] \) (see [43]), respectively, are depicted in Fig. 8 whereas Fig. 9 shows results

![Fig. 6. Block diagram of the mixed-signal calibration variant. The calibration with analog elements enables power consumption reduction. The EBP is the same as the all-digital variant. For simplicity the iteration index is omitted in the calibration parameters.](image)

![Fig. 7. Block diagram of the system model used in simulations.](image)

**TABLE I**

| Parameter | Value |
|-----------|-------|
| Modulation | 64-QAM |
| Symbol Rate \( (f_0 = 1/T) \) | 96 Gbd |
| Receiver Oversampling Factor \( (T/T_s) \) | 2 |
| Fiber Length | 100 km |
| Differential Group Delay (DGD) | 10 ps |
| Second Order Pol. Mode Disp. (SOPMD) | 1000 ps² |
| Speed of Rotation of the Pol. at the Tx | 2 kHz |
| Speed of Rotation of the Pol. at the Rx | 10 kHz |
| TI-ADC Resolution | 8 bit |
| TI-ADC Sampling Rate (all interleaves) | 192 GS/s |
| Number of Interleaves of TI-ADC (M) | 16 |
| Number of Taps of CE \( (L_g) \) | 7 |
| Roll-off Factor | 0.10 |
| Nominal BW of Analog Paths \( (B_0) \) (see [43]) - UDRV | 53 GHz |
| Sampling Phase Errors - UDRV | \( \Delta \delta^{(i)}_m \in [\pm 0.075]T \) |
| Gain Errors (see [43]) - UDRV | \( \Delta B^{(i)}_m \in [\pm 0.075]B_0 \) |
| Bandwidth Mismatches (see [27]) - UDRV | \( \tau_{H}^{(i)} \tau_{V}^{(i)} \in [\pm 0.075]T \) |
| I/Q Time skew - UDRV | \( \delta^{(i)}_m \in [\pm 0.023] \) |
| DC Offsets - UDRV | \( V_{FS} \) |
Fig. 8. Histogram of the BER for 500 random cases with and without the CE for a reference BER of $\sim 1 \times 10^{-3}$. Left: sampling phase errors (only). Right: gain errors (only). See simulation parameters in Table I.

Fig. 9. Histogram of the BER for 500 random cases with and without the CE for a reference BER of $\sim 1 \times 10^{-3}$. Left: I/Q time skew (only). Right: BW mismatch (only). See simulation parameters in Table I.

Fig. 10. Histogram of the BER for 500 random cases with combined impairments as defined in Table I. Reference BER of $\sim 1 \times 10^{-3}$. Top: without CE. Middle: CE $w/L_g = 7$ taps. Bottom: CE $w/L_g = 13$ taps.

Fig. 11. Convergence of the CE in the presence of combined impairments for different block decimation factors $D_B$ with $N = 8192$.

for random BW mismatches (see (23)) and I/Q time skews uniformly distributed in the interval $\Delta B_{25} \in [\pm 0.075]B_0$ and $\tau_H, \tau_V \in [\pm 0.075]T$, respectively. For all the evaluated cases the proposed compensation technique is able to mitigate the impact of all the impairments on the performance of the receiver when they are exercised separately. Moreover, a BER improvement of up to $10 \times$ can be achieved with this proposal. In particular, notice that the serious impact on the receiver performance of the I/Q time skew values of Table I is practically eliminated by the proposed CE with $L_g = 7$ taps.

BER histograms for the receiver with and without the CE in the presence of the combined effects are shown in Fig. 10. Results of 500 cases with random gain errors, sampling phase errors, I/Q time skews, BW mismatches, and DC offsets as defined in Table I are presented. Fig. 10 also depicts the performance of the CE with $L_g = 13$ taps. Without CE, a severe degradation on the receiver performance as a consequence of the combined effects of the TI-ADC mismatches is observed. However, note that the CE is able to compensate the impact of all combined impairments improving the BER in some cases by almost 100 times. Moreover, note that a slight performance improvement can be achieved increasing the number of taps $L_g$ from 7 to 13.

In multi-gigabit transceivers, the impairments of the AFE and TI-ADCs change very slowly over time, as mentioned in Section III-C. Hence, decimation can be applied since the coefficient updates given by (19) and (20) do not need to be made at full rate. In ultra high-speed transceiver implementations (e.g., for optical coherent communication), block processing and frequency domain equalization based on the Fast Fourier Transform (FFT) are widely used [4]. Therefore, we propose

\[ e^{i[nK/D_B + n]}, \quad n = 0, 1, \cdots, N - 1, \forall k, \tag{24} \]

with $k$ integer. By using this approach, Fig. 11 shows an example of the temporal evolution of the BER in the presence of combined impairments according to Table I for different values of $D_B$ with $N = 8192$. A moving average filter of length 10 has been used to process the instantaneous BER. Gear shifting is used to reduce the steady-state MSE and speedup the convergence of the algorithm. We highlight that the impact on the resulting BER is negligible when block decimation is applied. Therefore, its adoption will drastically reduce the implementation complexity.

B. Mixed-Signal Calibration of TI-ADC with Highly Interleaved Architectures

The mixed-signal approach described in Section III-D is investigated considering a TI-ADC architecture typically used in high speed receivers. In such applications, a hierarchical TI-ADC achieves the ultra high-speed and the best power
efficiency [41], [42], [45]. Successive Approximation Register (SAR) ADCs are commonly used in this architecture due to their power efficiency at the required sampling rate and resolution. The hierarchical TI-ADC organizes the T&H into two or more ranks with a large number of sub-ADCs. In this way the requirements for the generation and synchronization of the sampling clocks are relaxed. Additionally, a massive number of sub-ADCs with low sampling rate and high power efficiency can be used. Furthermore, the impact on the input bandwidth is reduced in contrast to T&H with direct sampling [46]. An example with two ranks, including the calibration elements required by our proposal in this variant is depicted in Fig. 12. Rank 1 comprises \( M_1 \) switches each of which feeds \( M_2 \) T&H stages of rank 2. Then, \( M_1 \times M_2 \) sub ADCs are used to digitize the input signal. In order to evaluate the performance of the mixed-signal calibration of Section III-D we model a hierarchical TI-ADC with \( M_1 = 16 \) and \( M_2 = 8 \) (i.e., \( M_1 \times M_2 = 128 \) sub ADCs). Clock signals with 100 fs RMS white-noise jitter are considered in this simulation. We emphasize that the sampling phases of the \( M_1 \) switches in the first rank, and the \( M_1 \times M_2 \) gains and offsets of the sub-ADCs are adjusted with this approach.

The temporal evolution of the BER and the mean Signal-to-Noise-and-Distortion-Ratio (SNDR) is shown in Fig. 13. A 54 GHz input tone is used in this measurement. Since a larger number of converters is used (i.e., 128 vs 16), a slightly slower convergence is observed with respect to previous simulation. Nonetheless, the impact of the mismatches in a hierarchical TI-ADC performance is mitigated with the proposed back-propagation based mixed-signal calibration. In particular, note that the SNDR can be improved from \( \sim 12 \) dB to \( \sim 30 \) dB by using the proposed background technique.

Figure 14 shows a comparison of the FFTs pre and post calibration with a 54 GHz sinusoidal input. Spectrum is generated from \( 2^{13} \) samples from the ADC of polarization \( H \), component \( I \). Measured amplitudes are normalized to Full-Scale (FS) [47]. Without calibration the mismatches introduce a large number of spurs with significant amplitude all across the spectrum. After the calibration, the spurs are greatly reduced. Hence, the SNDR is improved from 12.3 dBFS to 30.6 dBFS. The Spurious-Free Dynamic Range (SFDR) is also boosted from 23.6 dBFS to 51.2 dBFS.

The SNDR and the SFDR with and without the calibration are shown in Fig. 15. Prior to calibrate, the SNDR and SFDR are below 20 dBFS and 31 dBFS, respectively. With the calibration enabled, the SNDR remains above 40 dBFS until 10 GHz. At higher frequencies the SNDR is limited by the jitter asymptote. The SFDR is above 50 dBFS for the evaluated frequencies. Thus, a significant improvement in the ADC is obtained with the proposed technique.

A comparison with other calibration techniques is summarized in Table III. We emphasize that our proposal operates in background, does not require reference channels, a particular type of input signal, or a modified sampling sequence. Furthermore, the calibration can be applied in either analog or digital domain. In addition, the calibration engine is not limited to estimate and correct only sampling time errors, but
also gain, DC offset, bandwidth, and the I/Q time skew present in coherent communication systems. Moreover, the technique is able to adjust the errors simultaneously (i.e., a calibration sequence is not needed).

### V. EXPERIMENTAL RESULTS

We demonstrate the benefits of our proposal using a digital communication platform especially designed to evaluate TI-ADC mismatch calibration techniques. The platform allows the capabilities of our proposal to be evaluated in communication links using several different modulation schemes. Some key differences with more traditional TI-ADC evaluation platforms described in the literature are the following:

1) Test signals are not limited to sinusoids, but they also include realistic communications signals.

2) Characterization of the TI-ADC output is not limited to spectral estimation, but it additionally incorporates a complete communications receiver DSP.

3) The samples generated by the TI-ADC are not decimated as is usually done in experiments described in the literature. This is important in our experiments, since the receiver DSP mentioned in [2] requires contiguous samples and it cannot operate properly with decimated samples.

The test chip has programmable delay cells that allow the mixed-signal sampling phase calibration variant of our proposal to be tested too. We highlight that the following results can be ported to the high-speed optical coherent transceiver application scenario exercised in Section IV since both the receiver and EBP blocks are the same as those used in previous simulations.

### A. HIGH-SPEED TIME-INTERLEAVED SAR ADC

A block diagram of the 4 GS/s, 8 b TI-ADC architecture [35] is shown in Fig. 16. A photograph of the test chip, which is fabricated in a 130 nm CMOS process from Global Foundries, is shown in Fig. 17. The TI-ADC core area is 1 mm$^2$ whereas the total area of the chip is 2 mm$\times$2 mm. The design is composed of an input matching network, a hierarchical, non-buffered T&H, a TI-ADC core, a high-speed Low-Voltage Differential Signaling (LVDS) interface, and a clock sampling phase generator. The input matching network includes 50 Ω resistors and an 8 nH inductor to enhance the tracking bandwidth. The T&H spans two sampling hierarchies.

The first sampling hierarchy has $M_1 = 4$ switches whereas the second has $M_2 = 8$, which are included in the sub-ADCs. Since this T&H architecture avoids the use of sampling buffers, the noise sources in the signal path are minimized, and power consumption is reduced [41]. As mentioned in Section IV-B, in a hierarchical T&H architecture the sampling time errors mainly depend on the clock signals of the first hierarchy. Then, in order to adjust the sampling phases of the first hierarchy, capacitor-based programmable delay cells are included. The maximum calibration range of the delay cells is approximately ±50 ps, with a minimum calibration step of 260 fs. The core of the architecture is comprised of an array of 32 power efficient asynchronous SAR ADCs operating at 125 MS/s with 8 b resolution. A strongARM comparator with on-chip DC offset calibration is used to quantize the samples. The common-mode voltage, $V_{CM}$, is generated on-chip as the mean of the external reference voltages, $V_{refp}$ and $V_{refn}$. The 256 digital outputs of the ADC core are time-multiplexed and sent off-chip using a 16-channel LVDS driver. The data is transferred without any decimation at 32 Gb/s. An additional LVDS channel is used to transmit a clock reference in order to achieve synchronization with the LVDS receiver. To configure and control the different blocks in this architecture, 254 configuration registers are used.

The prototype chip achieves a peak ENOB of 7.09 bit (5.47 bit at Nyquist), 1.3 GHz bandwidth, and 93 mW power consumption from a 1.2 V power supply. The SAR ADC of each interleave achieves a Figure of Merit (FOM) of 123 fJ/conv – step. The efficient interleaved architecture allows the TI-ADC to achieve a peak FOM of 171 fJ/conv – step (526 fJ/conv – step at Nyquist). The achieved efficiency and sampling rate are comparable to de-
B. Reconfigurable Experimental Platform

A block diagram of the experimental setup is shown in Fig. 18. A high-performance Field-Programmable Gate Array (FPGA) [48] is used to generate the symbols to be transmitted. The FPGA is also in charge of collecting the samples from the ADC and sending them to the receiver DSP, which is implemented on a host computer. The receiver architecture, including the proposed compensation technique, has been introduced in Fig. 5 and simulated in Section IV. Multiple Pseudo-Random Binary Sequences (PRBSs) with configurable length and seed are generated in the FPGA. The amplitude of the symbols and the Additive White Gaussian Noise (AWGN) can be set through the coefficients $G_S$ and $G_N$, respectively. Then, we are able to evaluate different Signal-To-Noise Ratio (SNR) scenarios. The symbol with added noise is sent to a commercial, 16-bit Digital-to-Analog Converter (DAC) board [49] using an LVDS interface. The DAC synthesizes the samples at $1/T = 1$ GS/s. This sampling rate is adopted due to limitations on the FPGA and DAC clocks. The communication channel is modeled as a low-pass filter with a $-3$ dB cut-off frequency of 650 MHz [50].

Figure 19 shows the measured eye diagrams at the input and output of the channel with Binary Phase Shift Keying (BPSK) modulation. Notice that significant ISI is added by the channel. Although not explicitly shown, the impact of the ISI is even more significant for the higher order modulations used in the experiments, such as 8-PAM/64-QAM and 16-PAM/256-QAM. This ISI is an important part of the experiment since it enables the verification of the backpropagation technique, as discussed later in this section. On the receiver side, the signal is acquired by the TI-ADC, as described in Section V-A operating at a sampling rate of 2 GS/s (i.e., an oversampling ratio of $T/T_s = 2$ is used in the DSP blocks). The clocks for both DAC and ADC are generated from a single 10 MHz clock reference. Therefore, the frequency error due to the part per million tolerance of the oscillators in the receiver and transmitter clocks is avoided.

Fig. 18. Experimental setup used to test the proposal. A prototype TI-ADC with 8b and 2 GS/s acquires the symbols synthesized by the DAC. To emulate the operation of the optical coherent system, several sets of samples are collected. Each set corresponds to a signal component and is obtained after setting the platform with different PRBS lengths and delay cell values.

Fig. 19. Measured eye diagrams at the input and output of the channel.

Fig. 20. Received (a, b) 64-QAM, and (c, d) 256-QAM constellation diagrams in the presence of TI-ADC mismatches where the proposed compensation technique is (left) disabled and (right) enabled. A noiseless channel is set to evaluate the impact of the TI-ADC mismatches on the receiver performance.

C. Measurements

In this section we present measurement results using the test chip and the communication platform already described. Since the test chip has flexible timing calibration capabilities,
we focus on the calibration of sampling phase errors. In addition, gain errors are also compensated to demonstrate how this technique is able to simultaneously compensate different types of mismatches. Although the DC offset mismatch causes severe degradation on the performance of both TI-ADC and receiver, we do not consider such calibration here since it is already calibrated on-chip [35].

First, we illustrate the effectiveness of our proposal considering only the impairments of the TI-ADC for a receiver using 64-QAM and 256-QAM schemes. Toward this end, a noiseless channel has been set up. The resulting constellation diagrams are shown in Fig. 20 for the aforementioned modulations. In the absence of compensation, the mismatch among the interleaves is large enough to enlable the constellation points considerably. For a 256-QAM (see Fig. 20(b)) the degradation is such that the symbols in the received constellation are not distinguishable. With the proposed technique, a great improvement is observed for the modulations tested.

The comparison of the BER curves for the receiver with and without the proposed technique is shown in Fig. 21. Both all digital and mixed-signal variants are evaluated using 64-QAM and 256-QAM schemes. The performance of the receiver is severely affected when the TI-ADC mismatch is not mitigated. A sampling phase error of 4% has been set for Fig. 21(a), whereas 1% is set for Fig. 21(b). Setting a larger sampling phase error for QAM-256 would incur in issues related to the convergence of the receiver. A considerably high SNR penalty of 3 dB is measured for a 64-QAM modulation at a BER of $1 \times 10^{-3}$. A similar penalty can be observed for a 256-QAM scheme, although the mismatch in this case is much smaller than in the previous case. After enabling the proposed technique, the performance of the receiver is restored to almost replicate the case without mismatch with both implementation variants. This result indicates that our proposal is able to nearly eliminate the receiver penalty introduced by the mismatches of the TI-ADC.

An example of the convergence for the mixed-signal calibration using a 64-QAM scheme is shown in Fig. 22. Reported measurements are taken from polarization $H$. I/Q time skew has been introduced in each component by initially shifting all the delay cells by the same amount. An initial I/Q time skew of $\pm 4 \mu s$ has been set in this test. Gain mismatch is added to the samples in the post processing to exacerbate its effect on the receiver performance. The gain error is also adjusted in the post processing routine using the EBP block. The delay cells and post processed gain mismatch are updated according to the estimation obtained in each iteration of the test. We emphasize that the proposal is able to mitigate the I/Q time skew by tuning all the delay cells present in the test chip. In this measurement the target BER is $1 \times 10^{-4}$. The instantaneous BER is computed after performing a calibration step, and then processed by a moving average filter of size 6. The target BER is reached after 12 iterations, which implies the processing of $1.5 \times 10^6$ received symbols or 1.5 ms in a 1 Gb/s link. Considering a high-speed optical coherent application, such as the 96 Gb/s link exercised in Section IV the convergence would be achieved after 16 ms. The SNDR is measured applying a $\sim 500$ MHz sinusoidal input and setting the delay cells and post processed gain mismatch according to their evolution in the experiment just described. As a result, the SNDR is improved from 24 dB to 40 dB. We highlight that in Fig. 22 the estimators of all the errors for all the interleaves are adjusted simultaneously. Hence, a sequence of calibration steps (e.g., calibrate the sampling phase first, then the gain) is not needed, thus improving the speed of convergence. Finally, since the proposed technique runs in background, the mismatches are reduced concurrently with the convergence of the receiver.

The spectrum comparison for a sinusoidal input at 972 MHz pre and post calibration is shown in Fig. 23. Samples from a single channel, (i.e., from polarization $H$, component $J$) have been used to generate the spectra. $\pm 4 \% T$ of mismatch in the sampling phase and $\pm 5 \%$ of gain mismatch with respect to the unity gain have been included. Since the mismatches in the first sampling hierarchy are predominant, we observe $M_1 - 1 = 3$ spurs with high amplitude in the spectrum. Notice that the spurs caused by the mismatches among the interleaves seriously degrade both the SNDR and SFDR to 19.4 dBFS.

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**Fig. 21.** Measured BER comparison for (a) 64-QAM, and (b) 256-QAM with and without the proposed calibration. A mismatch of $\pm 4 \% T$ for (a), and $\pm 1 \% T$ for (b) is set using the delay cells.

**Fig. 22.** Example of calibration convergence of I/Q channels of horizontal polarization in a 64-QAM scheme with an SNR of $\sim 25$ dB. The subfigures from top to bottom are: I/Q time skew, sampling phase error, gain error, BER, and SNDR.
and 21.9 dBFS, respectively. After applying the proposed technique, the performance of the TI-ADC is boosted to 39 dBFS and 46.6 dBFS, for SNDR and SFDR, respectively.

The measurement of the SNDR and SFDR as a function of the input frequency with and without the proposed technique is shown in Fig. 24. Mismatches of sampling phase and gain are distributed as in the previous measurement. Without any calibration, the SNDR and SFDR are below 28 dBFS and 32 dBFS, respectively, for all the frequency range. After applying the backpropagation-based calibration the performance of the converter is significantly improved. For all the Nyquist range the SNDR is higher than 39 dBFS while the SFDR remains above 46 dBFS in the same frequency range. At least 15 dB of improvement in both measurements is achieved with this proposal.

VI. CONCLUSIONS

A novel background calibration technique for TI-ADC mismatches based on the backpropagation algorithm has been introduced in this paper. The characteristics of the backpropagation algorithm are exploited in a digital communication receiver application, where the algorithm is used to generate a suitable error signal, which is processed to effectively mitigate the mismatches of a high-speed TI-ADC. This technique can be extended to compensate impairments of the entire AFE (e.g., I/Q time skew). This proposal can be implemented either with a fully digital or a mixed-signal approach. Simulations performed in an application example with a DSP-based, DP optical coherent receiver have shown a fast, robust and almost ideal compensation/calibration of different TI-ADC mismatches. Sampling time, gain, offset, and bandwidth mismatches as well as I/Q time skew errors have been exercised both individually and combined. Measurements have been performed using an emulation platform based on an 8 bit, up to 4 GS/s TI-ADC test chip. We have shown that the degradation in the receiver performance is highly mitigated with this proposal for 64-QAM and 256-QAM schemes. Moreover, an SNDR improvement of at least ~15 dB is measured for all the Nyquist range. We highlight that this proposal is able to compensate mismatches of several types simultaneously (i.e., a sequence of calibration is not needed). Hardware complexity is minimized using decimation and serial processing in the backpropagation blocks. As the technique runs in background, the proposed technique is able to track parameter variations caused by temperature, voltage, aging, etc., without operational interruptions.

APPENDIX

APPENDIX A: TI-ADC MODEL

Next we review the model of the TI-ADC with impairments used in this paper (see Fig. 23). The effects of the sampling time errors $\delta_m^{(P,C)}$ and gain errors $\gamma_m^{(P,C)}$ can be modeled by analog interpolation filters with impulse responses $p_m^{(P,C)}(t)$ followed by ideal sampling [2], [3], as depicted in Fig. 25. The digitized high-frequency samples can be written as

$$y_m^{(P,C)}[n] = r_m^{(P,C)}[n] + y_m^{(P,C)}[n] + q_m^{(P,C)}[n],$$

where $r_m^{(P,C)}[n]$ is the signal component provided by the $M$-channel TI-ADC, and $q_m^{(P,C)}[n]$ is the quantization noise.

The total impulse response of the $m$-th interleaved channel is defined as

$$h_m^{(P,C)}(t) = c_m^{(P,C)}(t) \otimes f_m^{(P,C)}(t) \otimes p_m^{(P,C)}(t),$$

where $m = 0, \ldots, M-1$ and $\otimes$ is the convolution operator. Let $H_m^{(P,C)}(j\omega)$ and $S_m^{(P,C)}(j\omega)$ be the Fourier Transforms (FTs) of $h_m^{(P,C)}(t)$ and $s_m^{(P,C)}(t)$, respectively. The spectral shaping commonly used in digital communication systems results in $|S_m^{(P,C)}(j\omega)| \approx 0$ for $|\omega| \geq \pi/T_s$. Then, the analog filtering of Fig. 25 can be replaced (assuming $|H_m^{(P,C)}(j\omega)| \approx 0$ for $|\omega| \geq \pi/T_s$) by a real discrete-time model, as depicted in Fig. 26, resulting

$$h_m^{(P,C)}[n] = T_s h_m^{(P,C)}(nT_s), \quad m = 0, \ldots, M-1.$$  

Therefore, it can be shown that the digitized high-frequency signal can be expressed as:

$$r_m^{(P,C)}[n] = \sum_l \tilde{r}_m^{(P,C)}[l] s_m^{(P,C)}[n-l],$$

where $\tilde{r}_m^{(P,C)}[l]$ and $s_m^{(P,C)}[n-l]$ are the discrete-time models of the digitized high-frequency and quantization noise, respectively.
where \( s^{(P,C)}[n] = s^{(P,C)}(n T_s) \) and \( \tilde{h}^{(P,C)}[l] \) is the impulse response of a time-varying filter, which is an \( M \)-periodic sequence such that
\[
\tilde{h}^{(P,C)}[l] = \tilde{h}^{(P,C)}[M + l], \quad n = 0, \ldots, M - 1, \forall l,
\]
with \( h^{(P,C)}[l] \) given by (27).\(^5\) We highlight that the impact of both the AFE impairments and the \( M \)-channel TI-ADC mismatches are included in (28). Finally, the digitized high-frequency sequence is obtained by replacing (28) in (25),
\[
y^{(P,C)}[n] = \sum_{l} \tilde{h}^{(P,C)}[l] s^{(P,C)}[n - l] + \delta^{(P,C)}[n] + q^{(P,C)}[n].
\]

### APPENDIX B: DSP MIMO BACKPROPAGATION DETAILS

In this Appendix we derive an expression for the stochastic gradient of the squared error defined by (15). The total squared error (10) is
\[
\mathcal{E}_k = \sum_{j=1}^{4} \left| e^{(j)}_k \right|^2 = \sum_{j=1}^{4} \left( u^{(j)}_k - \tilde{a}^{(j)}_k \right)^2,
\]
where \( u^{(j)}_k \) is given by (13). We define the average squared error as
\[
\mathcal{E}_N = \frac{1}{2N + 1} \sum_{k=-N}^{N} \sum_{j=1}^{4} \left( u^{(j)}_k - \tilde{a}^{(j)}_k \right)^2.
\]

The derivative of \( \mathcal{E}_N \) with respect to \( g^{(io)}_{m0}[l] \) can be defined as
\[
\frac{\partial \mathcal{E}_N}{\partial g^{(io)}_{m0}[l]} = \frac{2}{2N + 1} \sum_{k=-N}^{N} \sum_{j=1}^{4} e^{(j)}_k \frac{\partial u^{(j)}_k}{\partial g^{(io)}_{m0}[l]},
\]
where \( l_0 \in \{0, 1, \ldots, L_g - 1\} \), \( m_0 \in \{0, 1, \ldots, M - 1\} \), and \( i_0 \in \{1, 2, 3, 4\} \). From the slicer error \( e^{(j)}_k \) specified by (9), define the \( T_s = T/2 \) oversampled slicer error as
\[
e^{(j)}[n] = \begin{cases} 
e^{(j)} / 2 & \text{ if } n = 0, \pm 2, \pm 4, \ldots \\ 0 & \text{ otherwise} \end{cases}
\]
Then, (33) can be rewritten as
\[
\frac{\partial \mathcal{E}_N}{\partial g^{(io)}_{m0}[l]} = \frac{2}{2N + 1} \sum_{n=-N}^{N} \sum_{j=1}^{4} e^{(j)}[n] \frac{\partial u^{(j)}[n]}{\partial g^{(io)}_{m0}[l]},
\]
where \( u^{(j)}[n] \) is the oversampled output of the DSP block given by
\[
u^{(j)}[n] = \sum_{l=0}^{4} L_{p-1} \Gamma_n^{(j,i)}[l] x^{(j)}[n - l], \quad j = 1, \ldots, 4.
\]
The time index \( n \) can be expressed as
\[
n = m + k'M, \quad m = 0, 1, \ldots, M - 1; \quad \forall k',
\]
with \( k' \) integer. Then, omitting the constant factor \( \frac{2}{2N+1} \), we can express the derivative (35) as
\[
\frac{\partial \mathcal{E}_N}{\partial g^{(io)}_{m0}[l]} \propto \sum_{k'}^{M-1} \sum_{m=0}^{M-1} e^{(j)}[m + k'M] \frac{\partial u^{(j)}[m + k'M]}{\partial g^{(io)}_{m0}[l]}.
\]

Next we evaluate the derivative \( \frac{\partial u^{(j)}[m + k'M]}{\partial g^{(io)}_{m0}[l]} \). Considering that the DSP filter coefficients \( \Gamma^{(i)}_n[l] \) and the CE coefficients \( g^{(io)}_{m0}[l] \) are independent, from (36) and (37) we verify that
\[
\frac{\partial u^{(j)}[m + k'M]}{\partial g^{(io)}_{m0}[l]} = \sum_{l=0}^{4} L_{p-1} \sum_{m=0}^{M-1} \Gamma^{(j,i)}_m[k'M + l] \frac{\partial x^{(j)}[m + k'M - l]}{\partial g^{(io)}_{m0}[l]}.
\]

By using (37), the signal at the \( i \)-th DSP block input given by (14) can be rewritten as
\[
x^{(i)}[m + k'M] = \sum_{l=0}^{L_g-1} g^{(i)}_{m0}[l'] w^{(i)}[m + k'M - l'].
\]
Therefore,
\[
\frac{\partial x^{(i)}[m + k'M]}{\partial g^{(io)}_{m0}[l]} = \sum_{l=0}^{L_g-1} \Gamma^{(j,i)}_m[k'M + l] u^{(io)}[m + k'M - l - l_0] \delta_{m_m, m_0} \delta_{i, i_0},
\]
where \( \delta_{m,m} \) is the Kronecker delta function (i.e., \( \delta_{n,m} = 1 \) if \( n = m \) and \( \delta_{n,m} = 0 \) if \( n \neq m \)). Replacing (41) in (39) we obtain
\[
\frac{\partial u^{(j)}[m + k'M]}{\partial g^{(io)}_{m0}[l]} = \sum_{l=0}^{L_g-1} \Gamma^{(j,i)}_m[k'M + l] u^{(io)}[m + k'M - l - l_0] \delta_{m,m_0}.
\]

Then introducing (42) in (38), we get
\[
\frac{\partial \mathcal{E}_N}{\partial g^{(io)}_{m0}[l]} \propto \sum_{k'}^{M-1} \sum_{m=0}^{M-1} e^{(j)}[m_0 + k'M] \times \sum_{l=0}^{L_g-1} \Gamma^{(j,i)}_m[k'M + l] u^{(io)}[m_0 + k'M - l - l_0] \delta_{m,m_0}.
\]
Finally, we set \( kM = k'M - l \) resulting
\[
\frac{\partial \mathcal{E}_N}{\partial g^{(io)}_{m0}[l]} \propto \sum_{k'}^{M-1} \sum_{m=0}^{M-1} e^{(j)}[m_0 + kM] w^{(i)}[m_0 + kM - l_0],
\]
where
\[
e^{(i)}[n] = \sum_{j=1}^{4} L_{p-1} \sum_{l=0}^{L_g-1} \Gamma^{(j,i)}_n[l] e^{(j)}[n + l]
\]
is the backpropagated error. Notice that $$E_{l}(g)$$ is the average of the instantaneous gradient component given by $$\hat{e}(i)[m_0 + kM]w[i][m_0 + kM - l_0]$$. As a consequence, we can write an instantaneous gradient of the square error as

$$\nabla_{w[i]}E_{l}(g) \propto \hat{e}(i)[m + kM]w[i][m + kM],$$

(46)

with $$w[n]$$ being the $$L_g$$-dimensional vector with the samples at the CE input defined by (16).

ACKNOWLEDGMENT

The authors would like to thank MOSIS for fabricating their design through the MEP research program.

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