Suspended-ultrathin Si membrane on SOI: a novel structure to reduce thermal stress of GaN epilayer

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Abstract. A 30nm-thick suspended-ultrathin silicon membrane based on SOI (silicon-on-insulator) substrate for GaN epitaxial growth is fabricated and analysed. We demonstrate that thermal stress of GaN in the effective area on this novel substrate can be reduced 44% more than that in normal SOI substrate, which can reduce the dislocation and crack density in GaN. The absence of BOX (buried oxide) layer are confirmed as main factors to result in reduction of thermal stress in GaN layer. This work provides a promising approach to obtain high-quality GaN by utilizing mechanical structure.

1. Introduction

Wide band gap III-V nitride based semiconductors, especially gallium nitride, has emerged as an eminently promising semiconductor material for their potential application in high-power, high-frequency transistors and optoelectronic devices [1-3]. Due to the insufficient of native substrate, commercial GaN materials generally grow on sapphire or SiC substrate, but these substrates are relatively expensive and GaN epitaxial material is generally poor [4]. Although silicon substrate has specific advantages such as low cost, high thermal conductivity and potential to integration, the quality of GaN is hindered by large difference in lattice mismatch and thermal expansion coefficients between silicon and GaN [5].

Compliant substrate is long considered as one of promising substrate for lattice mismatch in heteroepitaxy. SOI wafer has the advantage of the compliant top silicon layer which can reduce mismatch stress and improve the quality of GaN film [6-8]. Characteristics of the GaN growth on SOI substrates have been reported by many research groups which further demonstrate the compliant feature of SOI substrate [9, 10]. Yet, the potential of SOI substrate as a compliant substrate remains unrealized: (1) the top silicon layer is restrained by the buried oxide layer which intercepts the concept of complaint [11]; (2) the buried oxide layer can introduce extra thermal stress during cooling process. Besides, it has been proposed that the reduction of the substrate thickness can increase the critical thickness of the epitaxial layer, but the approach to fabricate a suspended or fully compliant silicon layer under 30nm is difficult to fabricate and is rarely studied.

In this paper, we proposed a suspended-ultrathin Si membrane with holes which can increase critical thickness and reduce thermal stress of GaN epitaxial layer. Theoretical background is present in Section 2. Detailed fabrication process is given in Section 3. Finite element method results were used to analyse the thermal stress characteristics in GaN during cooling process in Section 4. In Section 5, we explored the role of BOX layer, holes on the four edges of the suspended area and
distance between holes in thermal stress reduction by comparing with normal SOI substrate and other reported structures [12, 13]. It should be pointed out that this suspended-ultrathin Si membrane structure proposed in this paper is a generic structure and can be used to grow other hetero-epitaxial semiconductor materials such as AlN, GaAs, InP on SOI substrate. For simplicity, this paper focuses on the application of GaN growth on this new suspended-ultrathin Si membrane on SOI structure.

2. Theoretical background of the proposed novel SOI substrate

In the case of hetero-epitaxial layer growth of foreign material on a conventional bulk substrate, the epitaxial layer is usually much thinner than the substrate which is usually in the range of hundreds of micros, so most strain would reside in the epitaxial layer instead of the substrate. One theory builds relationship between strain distribution and thickness of substrate and epitaxial layer [14]. According to this idea, compliant substrate is proposed to reduce the strain of epitaxial film. As the thickness of the compliant substrate is on the order of that of the epitaxial layer, the strain can be accommodated between a thin substrate and epilayer. In this case, the strain produced during growth can be partitioned between substrate and lattice-mismatched epilayer. The strain partitioning in a structure containing two or more thin layers is theoretically calculated [15]. Neglecting the difference in the elastic coefficients of materials, the strain in epilayer can be approximately calculated in equation (1)

\[ \epsilon_f = \frac{h_z}{h_f + h_z} \epsilon_0 \]  

where \( \epsilon_f \) is the strain in the epitaxial film, \( \epsilon_0 \) representing the total misfit strain, and \( h_f \) and \( h_z \) representing respectively the thickness of the film and substrate. From another perspective, Y. H. Lo builds relationship between the critical thickness of epilayer and substrate thickness as shown in Fig. 1 [16]. With the decline in the substrate thickness, the critical thickness increases towards infinity. This means we can obtain infinitely thick dislocation-free epitaxial film on a sufficiently thin substrate.

![Figure 1. Relationship between effective critical thickness and the substrate thickness [16].](image)

Based on these two theories, we proposed a novel suspended-ultrathin Si membrane with holes which was freestanding and thinner than normal substrate. We supposed that this novel substrate was able to increase the critical thickness of GaN epilayer in some extent and reduce the thermal stress in GaN during cooling process. Fig. 2(a) shows a schematic of this novel suspended-ultrathin SOI structure. Fig. 2(b) schematically presents an ideal state of dislocation distribution after subsequent growth of GaN epitaxial layer on novel SOI and normal SOI structure.
Figure 2. Schematic of novel suspended-ultrathin SOI structure (a) and dislocation distribution after subsequent growth of GaN epitaxial layer on novel SOI and normal SOI structure.

3. Sample fabrication procedure

The SOI wafer was prepared by the SIMOX-Technologies with a thin silicon (111) layer, a BOX layer, and a handle silicon (100) of thickness ~110nm, ~670nm, and ~740μm, respectively. For the ultimate objective of GaN film growth, Si (111) layer was used for lattice structure matching purpose. The unstrained SOI wafer was cleaved into 1 cm x 1 cm pieces. Fig. 3 (a)-(d) schematically depicts the fabrication flow of the suspended-ultrathin silicon membrane with a series of holes on the four edges of the suspended area: (a) cutting SOI in small pieces; (b) reducing the thickness of top silicon; (c) inductively coupled plasma (ICP) etching after standard photolithography to form holes for subsequent wet etching; (d) Isotropic etching of the BOX layer through the holes using BOE (HF: NH4OH=6:1), stopping when top silicon layer was totally freestanding.

Figure 3. Schematic fabrication process of ultrathin silicon membrane on SOI (a)-(d).

This process to fabricate suspended-ultrathin Si membrane was much easier than the conventional approach to obtain silicon membrane by etching hundreds of microns bottom silicon from the back of the substrate. We could etch the buried oxide layer from the holes for a few minutes and precisely control the thickness of the top silicon to nanometres as SOI acted as a self-stop layer. The suspended-ultrathin silicon membrane was totally departed from BOX layer in order to achieve the freestanding of the bottom silicon surface. Optical microscope (OM) images of the fabricated samples with different top silicon thickness of 80nm, 40nm and 30nm were shown in Fig. 4. We defined the area surrounded by holes as the effective area where high-quality GaN can be grown.

Figure 4. Plan view of optical microscopy (OM) images of samples after BOE etching procedure on the novel SOI substrate with different top silicon thickness of 80nm (a), 40nm (b) and 30nm (c).
4. Simulation method

For heteroepitaxy growth, the thermal stress is a very critical factor in dislocation formation and material quality improvement, and thus is a focus of study in this paper. In order to investigate the thermal stress during the heteroepitaxy growth of foreign material (such as GaN) on this novel suspended-ultrathin Si membrane structures introduced in Section 3, finite element method was used to simulate the thermal strain distribution in GaN layer on our novel structure during cooling process. Simulation was performed in the framework of linear isotropic elasticity. Coefficient of Thermal Expansion (CTE), Young’s moduli (E), Poisson’s ratios (ν) and Density (ρ) for different films were prepared in Table 1 [7]. The simulation used solid mechanics model and assumed that all materials were linear elastic materials. The reference temperature was set to 1070°C and temperature loaded to all nodes was set to 25°C.

| Material | CTE(10⁻⁶K⁻¹) | Poisson’s ratio | Young’s modulus(GPa) | Density(kgm⁻³) |
|----------|--------------|----------------|----------------------|---------------|
| GaN      | 5.59         | 0.18           | 195.9                | 2330          |
| Si       | 3.59         | 0.262          | 169.2                | 6070          |
| SiO2     | 0.55         | 0.16           | 71.7                 | 2200          |

In order to simplify the calculation, we used a 30μm x 30μm square multilayer model including GaN epitaxial layer, Si (111) layer, BOX layer and bottom Si layer. The thickness of GaN epitaxial layer and Si device layer in the model were set to 1μm and 100nm, respectively (shown in Fig. 5). We simulate two types of structure models: the normal SOI substrate (Fig. 5a) and our novel SOI substrate (Fig. 5b). Especially, the novel substrate had a 10μm x 10μm suspended effective area which was surrounded by holes. The diameter of a hole and the width between two holes were respectively set at 3 and 4μm.

5. Results and discussion

Von-mises stress was used to characterize the thermal stress distribution in these two models, as shown in Fig. 6 (a) and (b). The stress distribution on the cross-section along the diagonal line was also presented in the Fig. 6 (c) and (d). The thermal stress of top surface of GaN on the novel substrate was obviously lower than that on the conventional SOI, especially in the effective area surrounded by holes. Yet, the thermal stress around the hole on the novel substrate was obviously more concentrated than any other area.
Figure 6. Strain field distribution for normal substrate (a), (c) and our novel substrate (b), (d).

We extracted the data of Von-mises stress along the diagonal line of the square mesa model to characterize thermal stress data for top surface of GaN. The section indicated by red arrow was the thermal stress in the effective area, as shown in Fig. 7. The blue square plotted simulation result of the novel SOI substrate, indicating that central effective part of GaN layers have 44.4% less thermal stress (~0.25GP) than that on normal SOI substrate showed by hollowed circle (~0.45GP) and 28.6% less thermal stress than that on back-etching substrate [12] showed by hollowed circle (~0.35GP). This result demonstrated that our novel substrate could release thermal stress more effectively than normal SOI substrate and back-etching structure during cooling process.

To explore why the novel structure could release thermal stress more effectively, the effects of the lack of BOX layer and the existence of surrounding holes on thermal stress of GaN layer were investigated respectively. Compared normal SOI substrate with Ref.13, the thermal stress in effective area was reduced from 4.5GP to 3GP due to the absence of the BOX layer in the bottom-side patterning and bonding substrate [13]. The BOX layer in normal SOI substrate impeded the migration of top silicon layer during the cooling process as the thermal expansion coefficient of BOX layer was less than that of top silicon layer. It was also clear that the existence of surrounding holes enabled the thermal stress to decrease from 3GP to 2.5GP when compared the model proposed by Ref.13 with the novel substrate due to the thermal stress concentration effect of the holes on the silicon film.
Figure 7. Thermal stress on top surface of GaN among different structures: normal SOI substrate (hollowed circle), our novel SOI substrate (blue square), back-etching substrate (red triangle [12]), and bottom-side patterning and bonding substrate (green circle [13]).

In order to further explore the effect of holes on thermal stress in our novel substrate, we kept the size of holes unchanged but changed the spacing between holes to expand the effective area. By setting the spacing at 2.5, 3, 3.5, 4, 4.5 and 5 μm respectively, different thermal stress distribution on GaN surface along the diagonal line was extracted, as shown in Fig. 8. With the increase in the spacing from 2.5 μm to 5 μm, the thermal stress on GaN layer in the effective area was gradually decreased.

Figure 8. Thermal stress on the top surface of GaN with different spacing between holes.

6. Conclusion

In summary, we have proposed a novel suspended-ultrathin Si membrane with holes which can increase critical thickness and reduce thermal stress during the subsequent growth of GaN epilayer. We illustrated that reducing the thickness of top silicon to nanoscale could significantly increase the critical thickness of GaN epilayer by analysing the theory and by simulation. Besides, the process to fabricate suspended-ultra thin silicon membrane was much simpler and easier. Furthermore, we systematically studied the role of the BOX layer and holes in our novel substrate. The absence of BOX
layer and existence of holes can effectively reduce the thermal stress in GaN epilayer. This structure provided a promising approach to facilitate high-quality GaN based devices fabrication. The same suspended-ultrathin Si membrane structure can be used to grow other advanced semiconductor materials such as AlN, GaAs, InP on SOI substrates.

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