Design of Ka band MMIC limiter low noise amplifier

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Abstract. A Ka band GaAs MMIC limiter low noise amplifier is presented. According to high power limiting and low noise requirements, PIN diodes and low noise PHEMT transistors are integrated in the same GaAs substrate. Finally, a high-power PIN limiter low noise amplifier integrated chip is obtained. The limiter has two-stage anti-parallel structure. The insertion loss is lower than 1.3dB, while the input and output standing wave ratio is lower than 1.5. The LNA has self-bias and parallel negative feedback structure. Simulation results indicate that the LNA has average gain 22dB, noise figure less than 2.2dB, input voltage standing wave ratio less than 1.2, output voltage standing wave ratio less than 2 from 33GHz to 37GHz. The integrated limiter and LNA has average gain 22dB, noise figure less than 3.5dB, input/output voltage standing wave ratio less than 2 from 33GHz to 37GHz.

1. Introduction

Low noise amplifier (LNA) is the key component in a branch of transceiver. The noise figure of LNA determines the performances of the entire receiving system. LNA is the first block in receivers. LNA is more vulnerable to be damaged by high-power input signals from transmitter output. So limiters are needed to protect LNA from damaging by high-power input signal. Previously limiter and low noise amplifier are designed with 50Ω input and output matching networks separately, and the limiter chip and the LNA chip are connected externally[1]. Output matching network of limiter, input matching network of LNA introduce loss and parasitic in the circuit, external connections and matching networks not only increase the area of circuit, but also influence circuit performances. Therefore, designing and integrating limiter and LNA in the same substrate simultaneously can reduce the area of circuit and the cost of fabrication, improve the capability.

In this paper, analysis and design procedure for a MMIC limiter-LNA are presented based on 0.15μm GaAs PIN diode and PHEMT transistor technology from Nanjing electronic devices institution. Simulation results show that it has average gain 22dB, noise figure less than 3.5dB, input/output voltage standing wave ratio less than 2 from 33GHz to 37GHz.

2. The design of PIN limiter

In this paper, PIN limiter has two stages anti-parallel diodes structure. Fig.1 shows the limiter circuit structure. The first stage has two branches of PIN diodes. Each branch has three series connected diodes. The series-connected configuration increases the first-stage’s turn-on to higher input power levels. The second stage has a single anti-parallel pair[2]. The distance between the first stage diodes and the second stage diodes is 1/4 wavelength. When input port has signal, the second stage PIN diodes turn on first. After 1/4 wavelength impedance transformation, the first stage diodes turn on later.
This structure lowers the total limiter input resistance, increasing the reflected power and lowering the dissipated power of each diode[3].

![Figure 1. PIN Limiter topology](image)

The withstanding power of limiter is mainly determined by the first stage. Assuming that the number of the identical PIN diodes at first stage is \( n \), the on-resistance of each diode is \( R_f \) (ignoring reactance), the line voltage is \( V_f \). The relationship between the power consumption \( P_a \) of limiter and the consumption power \( P_d \) of each diode is[4]:

\[
P_a = \frac{|nR_f Z_o + (nR_f + Z_o)Z_L|^2}{4R_f Z_o |Z_L|^2} P_d
\]  

(1)

The absorbed power by \( Z_L \) is:

\[
P_L = \frac{4R_f Z_o |Z_L|^2}{|nR_f Z_o + (nR_f + Z_o)Z_L|^2} P_a
\]  

(2)

Reflected power is:

\[
P_r = \left[ 1 - \frac{4nR_f Z_o (Z_L^2 + nR_f)}{|nR_f Z_o + (nR_f + Z_o)Z_L|^2} \right] P_a
\]  

(3)

The on-resistance of the diode must be considered:

\[
R_f = \frac{W_1}{\sqrt{D/\omega \beta_f}}
\]  

(4)

The consumption \( P_d \) increases as transistor size increases. Large size PIN diodes should be selected in the first stage to increase the withstanding power of limiter. But the large PIN diode has large parasitic capacitance, it will cause bandwidth to narrow and large insertion loss. In order to solve this problem, an inductor which resonates with capacitor was connected. In this paper 0.15μm GaAs PIN technology from Nanjing electronic devices institution is used to design the limiter. I layer thickness of PIN diodes is 1.20μm. The final limiter layout is shown in the figure 2. Figure 3 shows the small signal simulation results of the PIN limiter. The insertion loss is lower than 1.3dB; while the input and output standing wave ratio is lower than 1.5.
3. The design of low noise amplifier

0.15μm GaAs low noise PHEMT technology from Nanjing electronic devices institution is used to design the LNA in this paper. In order to meet the requirement of gain, the proposed LNA consists of 4 stages. The long gate width transistor has poor gain linearity at high frequency, while the short gate width transistor has good linearity. The first two levels have transistors whose gates contain 2 fingers of 50μm width and the last two levels have a transistor whose gates contain 4 fingers of 30μm width.

After determining the size of transistors, the bias point needs to be confirmed. In general, the noise of a transistor increases as the transistor current increases, while a large current is required to ensure the output power at high frequency. The bias current is generally chosen to be around 10%~20% \(I_{dss}\). By analyzing the relationship between frequency and noise at different bias point, it can be seen that when the bias current increases, the transistor noise increases simultaneously. In order to ensure the output power of the amplifier, the bias point was chosen at \(V_{ds}=3V, I_{ds}=15mA\).
The bias circuit determines transistor’s offset point. Bias circuits generally include active bias circuits and passive bias circuits. The active bias circuit uses active devices to provide the bias voltage for the amplifier[5]. Passive bias circuit is composed of resistance network and has simple structure. The self-biased circuit topology used in the amplifier is shown in the figure 5. Rs the resistance connected with source not only constitute the bias circuit, but also introduce the series negative feedback. It improves the stability of drain current and reduces the effect of temperature on drain current at the same time.

![Figure 5. Self-biased circuit topology](image)

Noise figure is the most important index of LNA. The manufacturing process and circuit matching are the key factors affecting the noise figure of amplifier. According to the noise equation (4) of cascaded circuit noise and gain performance of the first stage amplifier influence the overall amplifier noise most. Therefore, the best noise matching is applied in the input port. According to equation (5), when (source reflection coefficient) is equal to (optimum reflection coefficient), the first stage amplifier has the least noise figure. As shown in figure 6, m1 is the maximum gain matching point and m2 is the best noise matching point of the first amplifier at 35GHz. In order to get optimum noise figure, m2 is selected as the point of source impedance.
Figure 6. The equal gain circle and equal noise circle of the first stage amplifier.

\[
F_{\text{total}} = F_1 + \frac{F_2-1}{G_{A1}} + \frac{F_3-1}{G_{A1}G_{A2}} + \frac{F_4-1}{G_{A1}G_{A2}G_{A3}} + \ldots 
\]

(4)

\[
F_1 = NF_{\text{min}} + N_0 \frac{|\Gamma_x - \Gamma_{x,\text{opt}}|^2}{1 - |\Gamma_x|^2} 
\]

(5)

Circuit self-excitation is one of the main problems affecting the operation of the amplifier. In order to prevent the LNA from self-exciting, the micro-strip line is connected in series at the PHEMT source. The parallel negative feedback is introduced at the last two stages to increase the stability of the circuit. Parallel negative feedback can also widen the amplifier’s working bandwidth. The LNA topology is shown in figure 7.

Figure 7. Topology of low noise amplifier

After determining the amplifier circuit structure, all components were painted in the layout. The length of the transmission line, capacitances and resistances value were optimized in the layout. Finally, PHEMT small signal models were placed in the layout to get the layout simulation results. LNA layout is shown in figure 8. Simulation results indicate that the LNA has average gain 22dB, noise figure less than 2.2dB, input voltage standing wave ratio less than 1.2, output voltage standing wave ratio less than 2 from 33GHz to 37GHz. Simulation results are shown in figure 9.
4. Codesign of limiter and LNA
Input port of limiter is connected to the output port of the LNA. Before connected limiter with LNA, the limiter output impedance matches to the input impedance of LNA. Therefore two matching networks can be replaced with one matching network. The limiter low noise amplifier layout is shown in the figure 10.

The simulation results indicate that limiter doesn't influence the performance of LNA. Due to the insertion loss of limiter, the noise figure of limiter LNA is 1.3 dB higher than that of the amplifier. It is basically equal to the insertion loss of the limiter. The simulation results are shown in figure 11.
5. Conclusion
One-piece limiter low noise amplifier integrated circuit is proposed in this paper. One-piece limiter low noise amplifier doesn’t influence the performance of limiter and LNA. It can increase chip yield and transceiver assembly efficiency. The simulation results show that the performance of limiter LNA is in accordance with the expectation.

References
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