OpenCL + OpenSHMEM Hybrid Programming Model for the Adapteva Epiphany Architecture

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Abstract. There is interest in exploring hybrid OpenSHMEM + X programming models to extend the applicability of the OpenSHMEM interface to more hardware architectures. We present a hybrid OpenCL + OpenSHMEM programming model for device-level programming for architectures like the Adapteva Epiphany many-core RISC array processor. The Epiphany architecture comprises a 2D array of low-power RISC cores with minimal uncore functionality connected by a 2D mesh Network-on-Chip (NoC). The Epiphany architecture offers high computational energy efficiency for integer and floating point calculations as well as parallel scalability. The Epiphany-III is available as a coprocessor in platforms that also utilize an ARM CPU host. OpenCL provides good functionality for supporting a co-design programming model in which the host CPU offloads parallel work to a coprocessor. However, the OpenCL memory model is inconsistent with the Epiphany memory architecture and lacks support for inter-core communication. We propose a hybrid programming model in which OpenSHMEM provides a better solution by replacing the non-standard OpenCL extensions introduced to achieve high performance with the Epiphany architecture. We demonstrate the proposed programming model for matrix-matrix multiplication based on Cannon’s algorithm showing that the hybrid model addresses the deficiencies of using OpenCL alone to achieve good benchmark performance.

Keywords: OpenCL, OpenSHMEM, hybrid programming model, single-board computer, Network-on-Chip (NoC)

1 Introduction and Motivation

The emergence of a wide range of parallel processor architectures continues to present the challenge of identifying an effective programming model that provides access to the capabilities of the architecture while simultaneously providing the programmer with familiar, if not standardized, semantics and syntax. The programmer is often left with the choice of using a non-standard programming model specific to the architecture or a standardized programming model that yields poor control and performance. The parallel RISC processor investigated
in this work has presented precisely this challenge as suitable programming models matched to the architecture have been explored.

The Adapteva Epiphany RISC array architecture \[1\] is a scalable 2D array of low-power RISC cores with minimal uncore functionality supported by an on-chip 2D mesh Network-on-Chip (NoC) for fast inter-core communication. The Epiphany architecture is scalable to 4,096 cores and represents an example of an architecture designed for power-efficiency at extreme on-chip core counts. Processors based on this architecture exhibit good performance/power metrics \[2\] and scalability via the 2D mesh network \[3\] \[4\], but require a suitable programming model to fully exploit these capabilities. A 16-core Epiphany-III coprocessor \[5\] has been integrated into the Parallella mini-computer platform \[6\] where the RISC array is supported by a dual-core ARM CPU and asymmetric shared-memory access to off-chip global memory.

RISC array processors such as those based on the Epiphany architecture may offer significant computational power efficiency in the near future with requirements in increased floating point performance, including long-term plans for exascale platforms. The power efficiency of the Epiphany architecture has been specifically identified as both a guide and prospective architecture for such platforms \[7\]. The Epiphany-IV processor has a performance efficiency of 50 GFLOPS/W (single precision) \[2\] making it one of the most efficient fully divergent parallel processors based on general-purpose cores. This approaches the threshold for exascale computing requirements of a power budget of 20 megawatts \[8\]. This architecture has characteristics consistent with future processor predictions arguing hundreds \[9\] and thousands \[10\], \[11\] of cores on a chip.

One aspect of the low-power design of the Epiphany architecture is the use of a cache-less distributed on-chip memory architecture that for the Epiphany-III provides 32 KB of local memory per core for both instructions and data. Utilizing this core local memory and managing inter-core communication is critical to achieving good performance and this is a central element in the design of the architecture. In previous work, these technical challenges were the primary factors in achieving good performance with threaded MPI and less favorable results using OpenCL. Here we revisit OpenCL with a hybrid model that uses OpenSHMEM to resolve the deficiencies of OpenCL in the context of this architecture. Our main contributions are the presentation of a hybrid OpenCL + OpenSHMEM programming model with benchmarks for the application to matrix-matrix multiplication.

An outline of the remainder of the paper is as follows. Section \[2\] describes the Epiphany architecture and previous work using OpenCL and OpenSHMEM as parallel programming models. Section \[3\] presents the proposed hybrid OpenCL + OpenSHMEM programming model for device-level programming. Section \[4\] discusses the application of the proposed programming model to Cannon’s algorithm for matrix-matrix multiplication, including benchmark results. Section \[5\] discusses conclusions and future work.
2 Background

Interest in exploring hybrid OpenSHMEM + X programming models has been expressed recently within the OpenSHMEM community [12]. Just as the two-tier parallel hybrid OpenMP + MPI model handles both symmetric multiprocessing (SMP) execution within a node and distributed message passing for attached network nodes, it is assumed that similar hybrid models may benefit from mixing code with OpenSHMEM. In the specific case detailed within this paper, the hybrid OpenCL + OpenSHMEM model exists at the same parallelism tier and the combination of the programming models address the deficiencies of each within the context of the Parallella platform and Epiphany architecture. While OpenCL may do well addressing SMP architectures with hierarchical memory, it does not provide semantics for inter-processor communication between processing elements or multiprocessors. OpenSHMEM provides the semantics for non-uniform memory access (NUMA) across a partitioned global address space (PGAS) and may not be ideal for SMP architectures. The OpenSHMEM concept of memory exists virtually in a flat one-dimensional domain and lacks the semantics of the tiered memory hierarchy found in the SMP-based OpenCL programming model. Fundamentally, the Epiphany device-level architecture has characteristics of both SMP and PGAS platforms so it makes sense to address the architecture with a hybrid SMP and PGAS programming model.

2.1 Epiphany Architecture

The Adapteva Epiphany MIMD architecture is a scalable 2D array of RISC cores with minimal uncore functionality connected with a fast 2D mesh Network-on-Chip (NoC). Processors based on this architecture exhibit good energy efficiency and scalability via the 2D mesh network, but require a suitable programming model to fully exploit the architecture. The 16-core Epiphany-III coprocessor has been integrated into the Parallella minicomputer platform where the RISC array is supported by a dual-core ARM CPU and asymmetric shared-memory access to off-chip global memory. Figure 1 shows the high-level architectural features of the coprocessor. Each of the 16 Epiphany-III mesh nodes contains 32 KB of shared local memory (used for both program instructions and data), a mesh network interface, a dual-channel DMA engine, and a RISC CPU core. Each RISC CPU core contains a 64-word register file, sequencer, interrupt handler, arithmetic logic unit, and a floating point unit. Each processor tile is very small at 0.5 mm\(^2\) on the 65 nm process and 0.128 mm\(^2\) on the 28 nm process. Peak single-precision performance for the Epiphany-III is 19.2 GFLOPS with a 600 MHz clock. Fabricated on the 65 nm process, the Epiphany-III consumes 594 mW for an energy efficiency of 32.3 GFLOPS per watt [Olofsson, personal communication]. The 64-core Epiphany IV, fabricated on the 28 nm process, has demonstrated energy efficiency exceeding 50 GFLOPS per watt [2].

The raw performance of currently available Epiphany coprocessors is relatively low compared to modern high-performance CPUs and GPUs; however, the Epiphany architecture provides greater energy efficiency and is designed to
be highly scalable. The published architecture road map specifies a scale-out of the architecture to exceed 1,000 cores in the near future and, shortly thereafter, tens of thousands of cores with an energy efficiency approaching one TFLOPS per watt. Within this context of a highly scalable architecture with high energy efficiency, we view it as a competitive processor technology comparable to GPUs and other coprocessors.

While architecture energy efficiency is important, achievable performance with a compelling programming model is equally, if not more, important. Key to performance with the Epiphany architecture is data re-use, requiring precise control of inter-core communication since the architecture does not provide a hardware cache at any level. The cores can access off-chip mapped memory with a significant performance penalty in both latency and bandwidth relative to accessing on-chip core memory of any core.

Fig. 1. Adapteva Epiphany-III architecture diagram

2.2 OpenCL for Epiphany

OpenCL is an industry standard API for parallel programming accelerators or coprocessors on heterogeneous platforms [13]. Designed primarily for computing with general-purpose graphics processing units (GPUs), the API may be used to access the compute capability of other types of devices including multi-core CPUs and other accelerators. OpenCL support is provided for most mainstream high-performance computing accelerators including Nvidia and AMD GPUs, Intel and AMD multi-core CPUs, Intel Xeon Phi, and mobile CPU+GPU hybrid
processors. In this context, there is merit in exploring the use of OpenCL for exposing the compute capability of the Epiphany coprocessor on the Parallella.

OpenCL consists of a kernel programming API used to program the coprocessor device and a run-time host API used to coordinate the execution of these kernels and perform other operations such as memory synchronization so that parallel computationally intensive work can be offloaded from the host platform. The OpenCL programming model is based on the parallel execution of a kernel over many threads to exploit SIMD or SIMT architectures. From the perspective of the host platform, parallel kernels are enqueued for execution on the coprocessor device. Each kernel is executed over a global n-dimensional range of work items logically partitioned into local workgroups. Threads of execution within a workgroup are allowed limited synchronization through the use of barriers, and no synchronization between workgroups is allowed.

OpenCL was the first standard parallel programming API implemented for the Epiphany architecture, and partial support for the OpenCL 1.1 standard was available as part of the COPRTHR-1.5 SDK for Epiphany [14]. The selection of OpenCL was supported by several factors. The Epiphany-III coprocessor was available as part of a heterogeneous mini-computer (Parallella) that included a dual-core ARM CPU host running Linux. As a result, the OpenCL co-design programming model premised on the host-directed offload of parallel work to a coprocessor was well suited to the platform.

The focus of the implementation of OpenCL for Epiphany was to leverage the API to support effective parallel programming and take advantage of the underlying architecture. As with other non-GPU architectures, limitations and constraints exist in the use of OpenCL for targeting the Epiphany architecture. OpenCL was designed for massively multithreaded architectures such as GPUs. However Epiphany has no hardware support for multithreading and early experiments with software supported multithreading were not successful due in part to resource constraints. As a result, implementation of the OpenCL device execution model for Epiphany must constrain the workgroup size to the number of physical cores on the device.

The most significant technical issue encountered in the implementation of OpenCL for Epiphany was reconciling the physical memory architecture of the Epiphany coprocessor with the logical memory model defined by the OpenCL standard, shown in Figure 2. OpenCL address space qualifiers co-mingle the concepts of physical locality and visibility. For the Epiphany architecture, the physical memory co-located with each core executing a thread in an OpenCL workgroup is best described as symmetric distributed shared memory. This memory is physically local to the executing thread while also having shared visibility with all other threads since remote cores have non-uniform memory access to the local memory of any core. Managing the use and re-use of this symmetric distributed memory is critical to performance with the Epiphany architecture. An implementation treating this memory as OpenCL local may prove functionally correct and consistent within the standard, but the programmer will be left with poor performance without an interface to treat the memory correctly. Therefore,
an interface for the symmetric distributed shared memory is needed to properly manage on-chip data movement.

For this reason extensions were initially provided within the OpenCL implementation for Epiphany. A set of inter-thread memory copy routines were provided to allow for the direct copying of data between the local memory of one core to another. These routines resolved the problem with OpenCL in a non-standard way that nevertheless enabled algorithms to be implemented with good performance. At the time of this development the OpenSHMEM standard was close to publication but not yet released. In hindsight, OpenSHMEM was precisely the interface that was needed to resolve this critical issue that arises from the use of OpenCL for Epiphany.

2.3 OpenSHMEM for Epiphany
An implementation of OpenSHMEM targeting the Epiphany architecture was recently developed [15]. The interface provides access the complete OpenSHMEM 1.3 standard for Epiphany device-level execution. It fills the void left by the lack of a standard programming model able to achieve good performance with on-chip memory distributed through the NoC. Conceptually, the physical memory of the Epiphany architecture maps directly to the OpenSHMEM and PGAS memory model (shown in Figure 3). The OpenSHMEM interface for Epiphany does not address the concept of coprocessor offload or off-chip memory. For applications requiring these concepts, a hybrid programming model is required.

3 Hybrid OpenCL + OpenSHMEM Programming Model
Based on this prior work we propose a hybrid programming model that combines OpenCL with OpenSHMEM for device-level programming of parallel pro-
cessors like those based on the Epiphany architecture. In the simplest terms, OpenSHMEM directly resolves the most critical technical issue encountered in the implementation of OpenCL for such architectures, and replaces the non-standard extensions that were originally introduced to support inter-core data reuse and achieve good performance when implementing algorithms for Epiphany. At the same time, OpenCL complements OpenSHMEM in that for hybrid platforms that employ a parallel coprocessor, OpenCL provides support for the offload of parallel work to the coprocessor while there is no equivalent operation defined within the OpenSHMEM standard.

OpenSHMEM for Epiphany provides the inter-core communication between the OpenCL concept of a processing element or multiprocessor. In the case of the Epiphany architecture, they are one in the same. There is a single processing element per multiprocessor in order to address the hierarchical memory concept of local memory within the OpenCL specification. The OpenCL interface defines the global or constant memory (shown in Figure 4).

The hybrid OpenCL + OpenSHMEM programming model uses OpenCL for the development of host code that controls the overall application and directs the operations of the coprocessor through the offload of parallel computational kernels. The OpenCL kernel programming language, closely related to standard C, is used for the implementation of kernels. The distributed shared memory for which OpenCL provides no suitable API is then exposed using OpenSHMEM from within the OpenCL kernel. The OpenSHMEM programming model is nested within OpenCL and may be thought of as extending the latter. Developing applications with this hybrid programming model will follow closely the approach taken with OpenCL.

From an application development perspective, the OpenCL co-design model is still used with no change in the development of OpenCL host code. It is the OpenCL device programming API that is extended with OpenSHMEM. In this way each OpenCL kernel would contain within it a unique OpenSHMEM parallel
job with a context inherited from the OpenCL kernel. All initialization and allocation requirements in support of the OpenSHMEM API are performed within the OpenCL kernel each time it is enqueued for execution. Whereas OpenCL kernels are permitted to communicate through global memory, no communication using the OpenSHMEM API is permitted between kernels or between OpenCL work groups. This follows from the OpenCL execution model that allows synchronization within a work group but disallows synchronization between work groups. The restriction upon synchronization between OpenCL work groups has limited significance since the nested parallelism of OpenCL mode in which work is distributed across multiple work groups containing multiple work items can be ignored if a single work group is used. This simplification is employed in the application of OpenCL to the Epiphany architecture. Since the OpenSHMEM API is contained within the OpenCL device kernel context, all OpenSHMEM memory allocation is only visible within a kernel and is not persistent across multiple kernel invocations. This aspect of the hybrid programming model could be revisited in the future but was unnecessary for the initial demonstrations reported here.

It is worth addressing the issue of portability in the context of the proposed hybrid programming model. As with the case of the use of non-standard extensions originally employed to achieve good performance for OpenCL development targeting Epiphany, the use of a hybrid OpenCL + OpenSHMEM programming model will not be compliant with the OpenCL standard and will not be portable to other architectures for which only a pure OpenCL implementation exists. This issue cuts directly to the relevance of standards in the development of high-performance code across differing architectures. The very concept of performance-portability is questionable and completely separate from that of portability in general. A code that is non-standard and utilizes architecture-specific features is no less useful than a code that is completely portable and compliant with a given programming standard but achieves poor performance.
For this reason, we contend that the utility of programming standards such as OpenCL has less to do with portability and more to do with providing programmers familiar syntax and semantics for creating architecture-specific code. Therefore the lack of general portability of our proposed programming model is not a significant concern for programmers developing high-performance code.

4 Application and Results

Multiplication of matrices is a central building block in many scientific applications. We apply the hybrid OpenCL + OpenSHMEM programming model to matrix-matrix multiplication using the Cannon algorithm [16]. Cannon’s algorithm exemplifies the use of 2D parallel decomposition to effectively exploit this type of parallel architecture. The algorithm decomposes a square matrix-matrix multiplication problem (\( C = A \times B \)) across an \( N \)-by-\( N \) collection of processing elements. Sub-matrices are shared between neighboring processing elements after each submatrix-submatrix multiplication. As illustrated in Figure 5, the communication pattern begins by skewing the columns of matrix \( A \) left and the rows of \( B \) upward within the 2D mesh network topology.

For reference, a purely OpenCL implementation is benchmarked in which each thread per core must read in submatrices from global memory. This imple-
mentation lacks the data re-use that will lead to higher performance. Instead of communicating submatrices for A and B to the left and upward, respectively, equivalent bookkeeping is used to allow each thread to simply read in the submatrix that is needed from global memory. The performance using OpenCL alone achieves up to 794 MFLOPS for a matrix sizes of 128x128. It is worth noting that the architecture is quite limited by the off-chip bandwidth, particularly when loading memory directly rather than by using the off-chip DMA engine (a feature not addressed by either OpenCL or OpenSHMEM standards).

The same OpenCL code is then modified with OpenSHMEM. No changes are required for the OpenCL host code. The OpenSHMEM header is included in the OpenCL kernel, and the core-local buffers for matrices A, B and C are allocated using OpenSHMEM semantics for symmetric shared memory. The OpenCL kernel is further modified to use an OpenSHMEM put call with appropriate barrier synchronization between threads to implement the shifting of submatrices. The result is that a submatrix is read once from global memory and then re-used. This is known to be necessary to achieve optimal performance on the Epiphany architecture. The performance of the hybrid OpenCL + OpenSHMEM programming model achieves up to 1812 MFLOPS. With data re-use supported by OpenSHMEM the hybrid implementation easily outperforms the reference OpenCL-only implementation. Performance for this application is still limited by off-chip bandwidth, however, the inclusion of the inter-core communication with the OpenSHMEM interface increases performance by a factor of 2.3x. Results for various matrix sizes are shown in Table 1.

Table 1. On-chip matrix-matrix multiplication performance with pure OpenCL and hybrid OpenCL + OpenSHMEM programming model

| Matrix Size | Programming Model Performance (MFLOPS) | Speedup |
|-------------|----------------------------------------|---------|
|             | OpenCL | OpenCL + OpenSHMEM |                 |
| 32 x 32     | 218    | 504                  | 2.3x              |
| 64 x 64     | 424    | 1000                 | 2.4x              |
| 128 x 128   | 794    | 1817                 | 2.3x              |

5 Conclusions and Future Work

We have proposed and demonstrated a hybrid OpenCL + OpenSHMEM programming model for device-level parallel programming architectures like the low-power Epiphany RISC array processor. This hybrid model directly resolves the most critical deficiency encountered in the use of OpenCL alone for this architecture. The introduction of OpenSHMEM allows the proper management of the on-chip distributed symmetric shared memory, which is critical for obtaining high performance with this architecture. Benchmarks for matrix-matrix
multiplication demonstrate that the hybrid programming model can achieve better performance for this architecture and substantially outperforms the use of OpenCL alone.

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