Brief Announcement: Efficient Distributed Algorithms for Convolutional Neural Networks

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ABSTRACT
Several efficient distributed algorithms have been developed for matrix-matrix multiplication: the 3D algorithm, the 2D SUMMA algorithm, and the 2.5D algorithm. Each of these algorithms was independently conceived and they trade-off memory needed per node and the inter-node data communication volume. The convolutional neural network (CNN) computation may be viewed as a generalization of matrix-multiplication combined with neighborhood stencil computations. We develop communication-efficient distributed-memory algorithms for CNNs that are analogous to the 2D/2.5D/3D algorithms for matrix-matrix multiplication.

CCS CONCEPTS
• Theory of computation → Distributed algorithms; Parallel algorithms.

KEYWORDS
distributed algorithms; neural networks; communication optimization

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1 INTRODUCTION
The design of efficient distributed-memory parallel algorithms is much more challenging than shared-memory parallel algorithms. A number of recent research efforts have focused on utilizing shared-memory parallelism for Convolutional Neural Networks (CNN) [3, 9, 11, 16, 17] and high-performance library implementations are also available from vendors, e.g., oneDNN from Intel [12] and cuDNN from Nvidia [4]. However, only very simple and restricted schemes have been implemented for distributed-memory parallel systems [1, 6, 10, 13]. This is in contrast to matrix-matrix multiplication, for which a number of communication-optimal distributed-memory parallel algorithms have been developed, including the 3D algorithm [2, 5, 7], the 2D SUMMA algorithm [15], and the 2.5D algorithm [14].

In this paper, we synthesize efficient distributed-memory algorithms for CNN:

\[ \text{Out}[b, k, w, h] = \sum_{r, s} \text{In}[n][c][w+r][h+s] \ast \text{Ker}[k][c][r][s] \]

where Out is the output feature map, In is the input feature map, Ker is the kernel, b indexes the batch dimension, k the output feature, c the input feature, h, w the vertical and horizontal pixel index, and r, s the vertical and horizontal stencil index; \( \sigma_w \) and \( \sigma_h \) are strides.

Our key insight is that prior work on analytical modeling of data movement for tile-size optimization for CNN on shared-memory parallel systems [8] can be adapted for synthesis of communication efficient distributed-memory algorithms. The synthesis involves two steps: (1) formulation and solution of a 2-level tile-size optimization problem under a virtual global-memory model (Sec. 2.1), and (2) synthesis of initial data distribution and inter-processor collective communication schedule on a logical multi-dimensional processor view with a partitioned memory address space (Sec. 2.2).

Listing 1: CNN loops

```cpp
for (b = 0; b < Nb; n++)
for (h = 0; h < Nh; h++)
for (w = 0; w < Nw; w++)
for (k = 0; k < Nk; k++)
for (c = 0; c < Nc; c++)
for (r = 0; r < Nr; r++)
for (s = 0; s <Ns; s++)
Out[n][k][w][h] += Ker[k][c][r][s] \ast \text{In}[n][c][w+r][h+s]
```

Listing 2: CNN with single-level tiling

```cpp
for (bt = 0; bt < Nb; bt += Tb)
for (ht = 0; ht < Nh; ht += Th)
for (wt = 0; wt < Nw; wt += Tw)
for (kt = 0; kt < Nk; kt += Tk)
for (ct = 0; ct < Nc; ct += Tc)
CNNTile(bt, ht, wt, kt, ct);
```

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2 BACKGROUND

Consider the CNN computation shown in Listing 1. Listing 2 shows a single-level tiled code for the computation, where five of the loops are tiled (excluding the stencil dimensions \( N_r \) and \( N_s \), which are usually small prime numbers like 3, 5, 7 and are not tiled). In prior work [9], it was shown that the volume of data movement for the sequential execution of the tiled CNN code on a system with a single-level memory hierarchy could be analytically modeled as a function of the tile sizes and fast-memory capacity \( M \) as:

\[
\begin{align*}
\text{cost} &= N_b N_c N_w N_h + N_k N_c N_r N_s N_w N_h N_b / (T_w T_h T_k) + \\
&= N_b N_c (\sigma_w T_w + N_r - 1)(\sigma_h N_h + N_s - 1)N_w N_h N_b / (T_w T_h T_k) + \\
&= (\sigma_w T_w + N_r - 1)(\sigma_h T_h + N_s - 1)T_c + T_w T_h T_k + \\
&= N_r N_i T_i T_c \leq M, T_i \leq N_i, i \in \{b, k, w, h, c\}
\end{align*}
\]

The five tile loops in Listing 1 are fully permutable, and for each permutation, an analytical cost expression can be derived [9]. However, many permutations have exactly the same cost expression. Specifically, it can be shown (under some conditions) that the permutation of the outer four tile loops does not change the cost [9]. Further, the three indexes \( b, h, w \) are equivalent with respect to the data reuse characteristics and can be treated as a composite index that ranges over the four tile loops. In the treatment below, we will use \( T_{bhw} \) to represent \( T_b T_h T_w \), and these tile loops will always be treated as a contiguous band.

2.1 Parallel CNN: Global Virtual Memory

First, we consider data-movement optimization for CNN for a parallel system with P processors, each with private local memory of capacity \( M \), and a shared virtual global memory. Each processor can perform copy-in or copy-out of blocks of tensors to/from the virtual global memory to local memory. All computations are performed on data present in local memory, interspersed with data movement of blocks of data between local memory and the virtual global memory.

Listing 3: Local loop schedule with \( c \) as the innermost tiling loop

for \( k_t = 0 : W_k / T_k \)
for \( b_t = 0 : W_b / T_b \)
for \( w_t = 0 : W_w / T_w \)
for \( h_t = 0 : W_h / T_h \)
for \( c_t = 0 : W_c / T_c \)
// load \( \text{In} \), Ker tile from global memory;
// when loading \( \text{In} \), also load the "halo"
for \( r = 0 : N_r \)
for \( s = 0 : N_s \)
for point loops \( k, b, w, h, c \)
Out[\( \{b_t b, k_t k, w_t w, h_t h\} \) +]
In[\( \{b_t b, c_t c, \sigma(w T_w w + r), s_k(h_t h + s) \) +]
\[\] // store (update) Out tile to global memory

The CNN iteration space of size \( N_k \times N_c \times N_r \times N_h \times N_s \times N_w \times N_t \) is partitioned into \( P \) equal individual work-partitions of size \( W_k \times W_b \times W_w \times W_h \times W_t \) per processor. The intersection of any pair of work-partitions is empty, and the union of all work-partitions covers the full iteration space. Each processor is responsible for executing the iteration-space points within its work-partition. But the available local memory may be insufficient to simultaneously hold all the data needed for executing its entire work-partition. Hence the work-partition is executed as a sequence of smaller work-partitions.

Further, the three indexes \( b, h, w \) are equivalent with respect to the data reuse characteristics and can be treated as a composite index that ranges over the four tile loops. In the treatment below, we will use \( T_{bhw} \) to represent \( T_b T_h T_w \), and these tile loops will always be treated as a contiguous band.

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for \( b_t = 0 : W_b / T_b \)
for \( w_t = 0 : W_w / T_w \)
for \( h_t = 0 : W_h / T_h \)
for \( c_t = 0 : W_c / T_c \)
// load \( \text{In} \), Ker tile from global memory;
// when loading \( \text{In} \), also load the "halo"
for \( r = 0 : N_r \)
for \( s = 0 : N_s \)
for point loops \( k, b, w, h, c \)
Out[\( \{b_t b, k_t k, w_t w, h_t h\} \) +]
In[\( \{b_t b, c_t c, \sigma(w T_w w + r), s_k(h_t h + s) \) +]
\[\] // store (update) Out tile to global memory

The CNN iteration space of size \( N_k \times N_c \times N_r \times N_h \times N_s \times N_w \times N_t \) is partitioned into \( P \) equal individual work-partitions of size \( W_k \times W_b \times W_w \times W_h \times W_t \) per processor. The intersection of any pair of work-partitions is empty, and the union of all work-partitions covers the full iteration space. Each processor is responsible for executing the iteration-space points within its work-partition. But the available local memory may be insufficient to simultaneously hold all the data needed for executing its entire work-partition. Hence the work-partition is executed as a sequence of smaller work-partitions.

Listing 3 shows one possible permutation for the tiled loops within a node; \( a : b \) denotes the integers from \( a \) to \( b - 1 \) inclusive.

The total data movement volume for this loop is given by Eq. 3.

\[
\text{cost} = W_k W_h W_w N_k N_c N_r N_t N_s N_w N_h N_b / (T_w T_h T_k) + \\
W_k W_t N_r T_h N_s N_w N_h N_b / (T_w T_h T_k) + \\
W_k W_c / (\sigma_w T_w + N_r - 1)(\sigma_h T_h + N_s - 1)T_c + T_w T_h T_k + \\
N_r N_i T_i T_c \leq M; 1 \leq T_i \leq N_i, i \in \{b, k, w, h, c\}; \quad \text{Equation 2}
\]

We proceed by formulating the following modified optimization problem that we can solve analytically, and use that solution to generate an efficient solution for Eq. 3. The main change from Eq. 3 to Eq. 4 is the simplification of the cost function and the memory capacity constraint by dropping the small \( N_r - 1 \) and \( N_s - 1 \) terms. Further, as discussed earlier, we replace \( T_b T_h T_w \) by a new variable \( T_{bhw} \) and \( W_k W_h W_w \) by a new variable \( W_{bhw} \). In addition, it is easy to see that an optimal solution would have \( T_c = 1 \), so we exclude this variable from Eq. 4. We denote the memory capacity in Eq. 4 by \( M_t \); the relation between \( M_t \) and the actual per-processor memory capacity will be established later.

\[
\text{cost}_{t_k} = W_k W_{bhw} N_k N_c N_{bhw} / p + N_r N_t T_{bhw} / T_{bhw} \quad \text{Equation 4}
\]

We first observe that any optimal solution to Eq. 4 will satisfy

\[
(W_k = T_k \quad \text{and} \quad W_{bhw} = T_{bhw}) \quad \text{or} \quad (W_c = N_c)
\]

We must have either that \( W_c = N_c \) or \( W_c < N_c \). Suppose \( W_c < N_c \) for some optimal solution. Consider the term \( W_k W_{bhw} \) in the function to be optimized in Eq. 4. Since \( W_c < N_c \) and \( W_k W_{bhw} = N_k N_c N_{bhw} \), an increase in \( W_c \) and a decrease in \( W_k \) or \( W_{bhw} \) could maintain this equality and could decrease the cost in Eq. 4, keeping all other variables the same. Thus, in an optimal solution with \( W_c < N_c \) it must be the case that \( T_k = W_k \) and \( T_{bhw} = W_{bhw} \).

The following analysis considers two cases, based on Eq. 5.

**Case 1:** \( W_c = N_c \)

The arithmetic-mean-geometric-mean inequality can be applied to
Table 1: Summary of optimal solutions for Eq. 4 for tile loop permutations with c as the innermost tiling loop.

| Condition | Cost |
|-----------|------|
| $N_b N_h b_w / P \geq M_L$ | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |
| $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and $N_b N_h b_w / P < M_L$ | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |
| $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and $N_b N_h b_w / P < M_L$ | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |

Table 2: Summary of optimal solutions for Eq. 4 considering all possible tile loop permutations.

| Condition | Cost |
|-----------|------|
| $N_b N_h b_w / P \geq M_L$ and $N_b N_h b_w / P \geq M_L$ | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |
| $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and $N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$ | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |
| $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and $(N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$) | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |
| $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and $(N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$ or $N_b N_h b_w / P < M_L$) | $N_b N_h b_w / P + \frac{N_b N_h b_w}{P} N_b N_h b_w$ |

With other processors only through explicit inter-processor communication operations.

The global memory model used in Sec. 2.1, the local memory capacity in each processor ($M$) only needs to be sufficient to hold the data-footprints (slices of accessed data in the three tensors) of a tile, with blocks of data being moved between local memory and the virtual global memory in between successive tiles. In a distributed-memory parallel system, in addition to holding the data-footprints of the currently executed tile, all elements of the three tensors must also be held in the local memory of one or more processors.

We first provide a high-level sketch of the construction of the distributed-memory parallel CNN algorithm. Given CNN problem parameters $N_b$, $N_h$, $N_c$, $N_k$, $N_k$, $N_s$, $N_p$, number of processors ($P$), and memory $M_P$ per processor: i) Determine the per-memory capacity $M_P$ needed to hold the tensors in a distributed manner to compute available memory for tiles, $M = M_P - M_p$; ii) Use the reduced capacity $M$ to solve the global-memory optimization problem discussed in Sec. 2.1 – the same tile schedule will be used by the processors in the distributed-memory system; iii) Determine parameters $P_b$, $P_k$, $P_s$, $P_w$ to create a logical multi-dimensional grid for the $P$ processors; iv) Generate the initial data distribution and the data communication schedule for the multi-dimensional processor grid.

**Parameters for Multi-dimensional Processor Grid:** The solution to the global-memory optimization problem in Sec. 2.1 provides values for tile sizes $T_i$ as a function of problem parameters and machine parameters. For the distributed-memory CNN algorithms, the $P$ processors are viewed as a logical multidimensional $P_b \times P_k \times P_s \times P_w \times P_k \times P_k$ grid, with $P_i = N_i / W_i$.

If the solution to the global-memory optimization problem addressed in Sec. 2.1 corresponds to Case 2, $P_i = N_i / W_i = N_k / T_k$, $P_b P_k P_s P_w = N_b N_h N_c (T_b T_w T_h)$, and $P_c = P / P_b P_k P_s P_w$.

For those solutions derived from Case 1, $P_i = 1$, $W_i = N_i$, $P_k = N_k / W_k$, $P_b P_w P_k = N_b N_h N_c (T_b T_w T_h)$, $W_k = \sqrt{N_b N_h N_c N_s / N_k}$, $W_b W_w W_h = \sqrt{N_b N_h N_c N_s / N_k}$.

The Case 1 solution is analogous to the 2D SUMMA [15] algorithm for distributed matrix-multiplication, and Case 2 corresponds to the 2D5 [14] and 3D [5] distributed matrix multiplication algorithms; the latter when $M_L \geq \left( \frac{N_b N_h b_w}{P} \right)^{1/3} (N_b N_h b_w)^{1/3}$ and the former otherwise.

**Initial Data Distribution:** For each tensor, one or more of the five loop indices $b, c, h, k, w$ are absent in the indexing expression: $k$ is absent in $In[b, c, \sigma w + r, \sigma h + s]$, $b, h, w$ do not appear in $Out[k, c, r, s]$, and $c$ is not used in $Out[b, k, w, h]$. Therefore, identical data slices of a tensor will be accessed by all processors along any missing loop index. For example, identical slices of $Out[k, c, r, s]$. 

2.2 Distributed CNN: Partitioned Memory

In this subsection, we show how the tiled solution from Sec. 2.1 can be used to construct an efficient algorithm for CNN for a distributed-memory parallel system with a fully partitioned memory: each processor has a local memory capacity $M_D$ and can communicate
will be accessed by processors that only differ in the processor-grid coordinates along \( b \) or \( h \).

Each processor \( P_{b,c,h,w} \) accesses a slice of \( Ker \), where the specific elements accessed by a processor depend on its indices \( c \) and \( k \), but not on \( b, h, w \). There are \( P_b \times P_k \) distinct slices of data, each with \( W_c \times W_k \times N_b \times N_k \) elements and accessed by \( P_b \times P_k \times P_w \) different processors. The initial distribution of data for \( Ker \) has each of these slices uniformly partitioned along \( c \) into smaller sub-slices of size \( \frac{W_c}{P_b \times P_k} \times W_k \times N_b \times N_k \), distributed over the \( P_b \times P_k \times P_w \) processors that need to access data in all the sub-slices. A similar initial distribution strategy is used for \( In \), where the data slice needed by a processor is partitioned among \( P_b \) processors. For \( Out \), if \( P_b > 1 \), replication is used instead of disjoint partitioning across the \( c \) dimension in the multi-dimensional processor grid, to avoid additional data movement compared to that required in the global-memory solution of Sec. 2.1.

**Collective Communication Schedule:** Each processor allocates buffers for storing the elements of \( In \) and \( Ker \) accessed by a tile. The sizes of buffers are \( T_b(\sigma_w T_w + N_r - 1) (\sigma_k T_k + N_b - 1) N_k N_C / P + N_b N_k N_C / P \) for \( In \) and \( T_k(\sigma_w T_w + N_r - 1) (\sigma_k T_k + N_b - 1) W_k W_C / (T_k T_h T_b) \) for \( Ker \). There is no need for allocation any additional memory for \( Out \) tile because space for the entire accessed data slice for the tiles is allocated in the initial data distribution. There is therefore also no need for any inter-processor communication for \( Out \) (until a reduction step at the very end). Execution proceeds as a sequence of \( W_c \) tiles with interspersed inter-processor communication between the tiles.

The communication for \( In \) is as follows. The \( W_c \) tiles are divided into \( P_k \) groups, each group containing \( W_c / P_k \) tiles. The first processor along the \( k \) dimension of the processor grid broadcasts the elements of \( In \) needed for the tiles in the first iteration group. After \( W_c / P_k \) steps, the next processor along the \( k \) dimension becomes the originator of data broadcasts for the next \( W_c / P_k \) steps, and so on. The communication schedule for \( Ker \) is analogous to \( In \), with the broadcast of data being performed along the \( b, w, h \) dimensions of the processor grid.

**Cost Analysis:** The communication cost of the above distributed CNN algorithm is as follows. Let \( cost \) be the initialization cost (initialization cost for \( In, Ker \) and reduction cost for \( Out \)). It is equal to the footprint of the initial data distribution. The communication cost, \( cost_C \), is equal to total volume of broadcast data for \( In \) and \( Ker \).

\[
\begin{align*}
\text{cost}_I &= \sigma_w W_k W_w W_h + (\sigma_w N_w + N_r - 1)(\sigma_k T_h + N_b - 1) N_k N_C / P + N_b N_k N_C / P \\
\text{cost}_C &= \sigma_k W_k W_C N_b W_k W_h W_b / (T_w T_h T_b) + \\
&\quad W_k W_C (\sigma_w T_w + N_r - 1)(\sigma_k T_h + N_b - 1) W_k W_C / (T_k T_h T_b)
\end{align*}
\]

(10)

The local memory \( M_D \) in each processor must hold the initial data layout for all three tensors, and the tile footprints for \( Ker \) and \( In \), giving the following local memory constraint expression:

\[
g_D = (\sigma_w T_w + N_r - 1)(\sigma_k T_h + N_b - 1) T_k T_c + N_b N_k T_c T_e + W_k W_k W_w W_h + N_b N_k N_C / P \\
+ (\sigma_w N_w + N_r - 1)(\sigma_k N_h + N_b - 1) N_k N_C / P \leq M_D
\]

(11)

Let \( cost \), \( cost_C \), and \( g \) be the cost and \( g \) stated in Equation (3). We can see that both \( cost_D - cost \) and \( g_D - g \) equal \( \frac{1}{2}(\text{size}(In) + \text{size}(Ker)) \), which is a constant. Thus, the data movement cost of the distributed CNN algorithm only differs from that of the global-memory solution Table 2 by a constant.

### 3 CONCLUSION

This paper presents a new methodology to synthesize efficient distributed-memory algorithms. The key insight driving this work is that a two-level tile optimization model can be used to synthesize efficient distributed-memory algorithms. The methodology was used to create new distributed algorithms for convolutional neural networks, analogous to the well-known 2D/2.5D/3D distributed matrix-multiplication algorithms.

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