A Back-End, CMOS Compatible Ferroelectric Field Effect Transistor for Synaptic Weights

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Motivation

The training of deep neural networks (DNNs) is very computationally intense. Each time a signal propagates from one layer to the next, a vector-matrix multiplication is required.

A memristor crossbar array is an energy efficient hardware solution. While applying a voltage to all inputs, the current at the outputs is the sum of all inputs (\(V_i\)) multiplied by the corresponding weights (\(G_{ji}\)). All outputs can be read at the same time.

Device Concept

Ferroelectric Field Effect Transistor (FeFET): Depending on the polarization direction of the ferroelectric gate dielectric (\(\text{HfZrO}_4\)), there is accumulation (low resistive state) or depletion (high resistive state) in the channel (\(\text{WO}_x\)).

Results

The channel resistance (\(R_{ds}\)) after the application of 5\(\mu\)s write pulses (\(V_{write,G}\)) of varying amplitudes. Each data point corresponds to a resistance measurement between S and D at \(V_{read,D} = 200\) mV.

Retention measurement for 1500s. \(V_{read,D} = 200\) mV was uninterruptedly applied while the current was measured every 5s to determine \(R_{ds}\). 18 states (>4bit) can clearly be differentiated.

25 potentiation (1V to 3.1V) and depression (-0.9V to -3.0V) cycles show stable operation with low cycle-to-cycle variation. Potentiation and depression show good symmetry. Writing to the high-impedance gate allows low writing energies (2.1 \(\times\) 10\(^{-17}\) J/\(\mu\)m\(^2\)).