Comprehensive Analysis of a High-Power Density Phase-Shift Full Bridge Converter Highlighting the Effects of the Parasitic Capacitances †

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Abstract: A phase-shift full bridge converter is analyzed in detail in continuous conduction mode for one switching cycle for both the leading and lagging legs of the primary bridge. The objective of the study is to determine how the stray capacitance of the transformer, and the capacitances of the diodes in the bridge rectifier affect the converter functionality. Starting from some experimental results, Laplace equivalent circuit models and describing equations are derived for each significant time interval during the switching cycle and are validated through simulations and experimental measurements. The resulting equations are of great interest in the high-power density domain because they can be used to design a clamping circuit for the output rectifier bridge accurately.

Keywords: phase-shift full bridge converter; stray capacitance; Laplace circuit models; parasitic elements

1. Introduction

The phase-shift full bridge converter (PSFB) uses parasitic circuits elements, such as capacitances of the semiconductor devices and leakage inductances of the power transformer to provide zero voltage switching (ZVS) without any other active components. During the dead time between switching the transistors of the same leg, the converter can achieve zero voltage ZVS using the energies stored in magnetic components (mainly the power transformer leakage and magnetizing inductance) and the output capacitances of the primary bridge switches. Dead time is usually calculated using a set of predefined conditions, which results in the loss of zero voltage switching condition (ZVS) at light loads [1]. Since the zero voltage switching determines the efficiency of the converter and considering that it depends on the dead time, the relationship between the available energies, the values of the magnetic components and the parasitic capacitances of the semiconductor devices can be determined by analyzing the equivalent circuit models during switching. The values of the magnetic components, the snubbers and the capacitances of the semiconductor devices can be chosen based on this analysis.

When a PSFB is designed for high output voltage, the effect of the stray capacitance of the power transformer together with the parasitic capacitance of the secondary rectifier bridge has a significant effect on its operation [2]. This type of converters are intensely used in many of industrial areas [3], for example: Battery chargers for plug-in-electric vehicles [4–6], photovoltaic (PV) power systems (charging batteries or boosting the PV voltage to higher levels) [4], fuel-cell stacks, wind turbines, DC microgrid applications, lighting, etc.

The PSFB topology is represented in Figure 1. As it can be seen, the converter has three modules: The full bridge inverter, the high frequency transformer, and the output rectifier and filter. The converter
has a simple topology which can be easily controlled using fixed frequency. Because the description and functional analysis of this type of converter are present in the literature [6,7], in this paper, the effect of the parasitic elements will be emphasized. The main advantages of this topology are: ZVS in a wide load range, simple control methods, low power density, and high efficiency [8].

![Phase-shift full-bridge converter](image)

**Figure 1.** Phase-shift full-bridge converter.

In most cases, high insulation requirements are needed between the primary and the secondary windings of the power transformer to satisfy the safety standards for this converter. This leads to large leakage inductance in primary and secondary sides. A large number of secondary turns required for high step-up and high voltage applications leads to an increased capacitance between the windings of the transformer, significantly deteriorating the performance of the converter [3,9]. The parallel capacitance of the secondary rectifier diodes adds to the stray capacitance of the transformer further increasing its effects. Another drawback of the converter is the dependency of the ZVS on the load conditions. The loss of ZVS causes not only a decrease in efficiency, but also results in high electromagnetic interference at light load. There are methods to increase the ZVS range by adapting the dead-time based on load condition [10,11]. Moreover, new control methods where used to increase the ZVS at light loads [12–15]. Modification of the power topology was proposed to extend the ZVS range in References [16–19]. By properly analyzing the switching behavior of the converter, the ZVS range can be extended without altering the control or the topology of the converter to some extent.

Many studies concentrate on the parasitic elements and how can they degrade the efficiency of the converter. None of these papers considers the stray capacitance of the transformer or the capacitance of the output rectifier. The parasitic elements of the high voltage transformer are analyzed in different papers, but only in predetermined conditions: For example, in Reference [3] only in discontinuous conduction mode (DCM) and for a PSFB converter with pure capacitive filter; in Reference [9] the effect of the transformer capacitance only on the leading leg from current drop perspective; in References [20,21] a discussion on voltage oscillations across secondary diodes in a PSFB converter, but not analyzing in every detail a complete switching interval.

The design of high voltage PSFB converter has many degrees of freedom which complicates the selection of the components [22]. Finding an optimized solution (highest power density, efficiency or lower cost) requires comprehensive analytical models and equations that account for the most harmful parasitic elements. This work concentrates on a detailed analysis of the PSFB converter that accounts parasitic influences, namely: Stray capacitance of the transformer secondary winding and the capacitances of the diodes in the bridge rectifier. The analysis is performed in continuous conduction mode for both the leading and lagging leg of the primary bridge for a complete switching cycle.

2. Motivation

Most articles nowadays start from method explanation and simulations followed by experimental results for validation. In this paper, a different approach is proposed. As presented in Figure 2,
one can see the differences between a simulation-based analysis and the waveforms obtained during experimental measurement. Starting from these differences, a mathematical analysis using Laplace equivalent models, together with Spice simulations for the different working time intervals are proposed for better understanding the influence of the parasitic capacitance on the phase shift converter [23].

The Laplace equivalent models emphasize the effects of the parasitic capacitance and provide the designer with an in-depth understanding of how to compensate them in order to provide a better design. The simulations were carried out to validate the theoretical analysis and provide a faster and more intuitive tool for the designers. A complete switching cycle of the converter was considered for the analysis. For an in-depth analysis, this cycle was divided into seven time intervals to better highlight the effect of the parasitic capacitance. For each time interval, Laplace equivalent models are provided in the paper followed by a simulation specific built for each situation. In the simulations, the component values used are the same as for the built experimental model. The results obtained through simulations are compared with the ones obtained during experiments. Comparing the numerical values, it can be seen that the mathematically equivalent model and simulations are validated. In some cases, the small inaccuracies that appear are due to other parasitic elements that were not taken into account intentionally to have a simple equivalent model that can be used with ease. As presented in the paper, the equations obtained can be used for instance as a basis for the design of an active snubber circuit that will increase the efficiency and ease the thermal enclosure design. Choosing the correct components through a minimum number of steps is every designer’s goal.

![Phase-shift waveforms obtained: (a) On simulation; (b) experimentally.](image)

The experimental model from which the analysis started was used to provide data to check the accuracy of the Laplace equivalent models and simulations.

The phase shift converter was designed for the following specifications: The input voltage of the converter reflected in the secondary is \( V_{in} = 250 \text{ V} \), and the output voltage is \( V_{out} = 173 \text{ V} \). The primary leakage inductance is \( L_{r,p} = 5 \mu\text{H} \), the transformer ratio is \( n = 0.6 \), and the output inductor is \( L_{out} = 280 \mu\text{H} \).

The secondary peak voltage and the oscillations caused by \( L_r = 14 \mu\text{H} \) inductance (the sum of the leakage inductances referred to the secondary that will be explained later) and \( C_s \) capacitance—total stray capacitance of the transformer and rectifier capacitances (will be demonstrated later) are presented in Figure 3.
As it can be seen from secondary rectified voltage, the frequency of oscillations is $f_r = 4.167 \text{ MHz}$. Thus, $C_s$ capacitance can be estimated as:

$$ C_s = \frac{1}{4\pi^2 f_r^2 L_r} = \frac{1}{4\pi^2 \cdot 4.167 \cdot 10^6 \text{ Hz} \cdot 14 \mu\text{H}} \approx 100 \text{ pF} $$

(1)

where $L_r = 14 \mu\text{H}$.

Also, the discharge time interval of $C_r$ (the switches equivalent output capacitance equal to 767 pF) can be estimated as:

$$ \Delta t = \frac{1}{\sqrt{L_r C_r}} \arcsin \left( \frac{V_m}{I_0 \cdot \sqrt{L_r / C_r}} \right) = \frac{1}{\sqrt{14 \mu\text{H} \cdot 767 \text{ pF}}} \arcsin \left( \frac{250 \text{ V}}{2.3A \cdot \sqrt{14 \mu\text{H} / 767 \text{ pF}}} \right) \approx 97 \text{ ns} $$

(2)

where $I_0 = 2.3 \text{ A}$ is the output current. Equation (2) will be later demonstrated in the article.

The $C_r$ capacitor is fully charged in about 97 ns as can be observed in Figure 4:

![Figure 3. Measured waveforms for the designed phase-shift full bridge converter (PSFB) converter.](image)

Figure 3. Measured waveforms for the designed phase-shift full bridge converter (PSFB) converter.

Although simulation tools can always be used for simulating the switching converters in a much easier way, the circuit parameters remain in non-closed form, and it is difficult to tell the impact of a certain design parameter on the results. Moreover, experiments often take time, and additional delay will be expected if changes in magnetic components are needed. On the other hand, a mathematical model can give very intuitive information, which can always help the designer to (1) fully understand the operation of the switching states; (2) reduce the number of iterations for optimization in experiments; (3) find worst case/corner case for testing; (4) analyze component tolerance impacts, etc.
3. The Model of the Converter

In Figure 5a, an equivalent electric circuit of a high frequency transformer is presented, with all the elements referred to the secondary side. \( R'_{w1} \) and \( R_{w2} \) are the resistances and \( L'_{lp} \) and \( L_{ls} \) are the leakage inductances of the primary and secondary windings, \( L_m \) is the magnetizing inductance of the secondary, \( C'_1 \) and \( C_2 \) are the self-capacitances of the primary and secondary windings, \( C_{12} \) the mutual capacitance between the windings and \( V'_1, V_2 \) are the voltages of the primary and secondary sides. For the analyzed converter, the primary and the secondary inductances of the transformer are small compared to the magnetizing inductance. The voltage drop across these inductances is small; thus, the stray parasitic capacitances can be modeled by a single capacitor, connected as in Figure 5b equal to: \( C_{sec} \approx C'_1 + C_2 \) with \( C_{12} \) neglected.

![Transformer models](image)

**Figure 5.** Transformer models: (a) Equivalent electric transformer model with all elements referred to the secondary side; (b) simplified model of the transformer with \( C_{12} \) neglected; (c) simplified model of the converter with \( L_r \) and \( C_{sec} \) introduced.

If the effects of the winding resistances and of the magnetizing inductance are neglected, then a simplified transformer model is obtained, Figure 5c, where \( L_r \) is the sum of the leakage inductances.

Due to design considerations, the transformer ratio is equal to 0.6, resulting in the equivalent circuit of the PSFB converter, Figure 6, where \( G_1, G_2, G_3 \) and \( G_4 \) are the gate drive signals, \( V_{cs} \) is the voltage on the stray capacitance, \( I_r \) is the current through the \( L_r \) inductance, and \( V_{rec} \) is the secondary rectified voltage. The rectifier capacitances are also included in the total stray capacitance of the transformer \( C_s = C_{sec} + C_{DIODES} \). When \( I_s \) flows through \( D_1, D_4 \) \( C_{DIODES} = C_{D2} + C_{D3} \) and vice-versa when \( D_2 \) and \( D_3 \) conduct.

![A simplified model of the PSFB converter](image)

**Figure 6.** A simplified model of the PSFB converter.
Whenever possible, the parasitic elements (leakage inductances of the transformer associated with semiconductor parasitic capacitances) can be used in an advantageous way to facilitate the resonant transition and to achieve ZVS. In Figure 1 the resonant inductor is depicted by $L_{r_p}$ that can be an external inductor added to the schematic but in this case, the leakage inductances of the transformer will be used as the resonant inductor, $L_r$, to achieve ZVS: $L_r = L_{lkp} + L_{lks}$. $C'_{o1}$, $C'_{o2}$, $C'_{o3}$, $C'_{o4}$ are the output capacitances of the switches and $I_r$ and $V_{inv}$ are values referred to the secondary.

4. Converter Operation

Figure 7 illustrates the operation waveforms of the converter.

![Figure 7. Qualitative operation waveforms of the converter.](image)

4.1. Operation during $[t_1-t_3]$.

In the first analysis, the influence of the capacitance $C_o$ is neglected. Before $t_1$, transistors $Q_1$ and $Q_3$ together with diode $D_1$ and $D_4$ are ON. In the same time, the output capacitor $C'_{o2}$ of the $Q_2$ transistor starts discharging. The output current $I_o$ flows through $D_1$, $D_4$, $D_3$ and $D_2$, so that the following relationships can be written.

\[
\begin{align*}
    i_{D1} &= i_{D4} \\
    i_{D2} &= i_{D3} \\
    i_{D1} + i_{D2} &= I_o
\end{align*}
\]  

(3)

During $t_1$-$t_2$, if there is enough energy stored in $L_r$, $C'_{o2}$ capacitor is completely discharged, and $C'_{o1}$ is charged to $V_{in}$. Thus, at $t_2$, the body diode of $Q_2$ turns ON, allowing ZVS turn ON for $Q_2$. Considering $C_r = C'_{o1} + C'_{o2}$ the equivalent output capacitance of $Q_1$ and $Q_2$ transistors and
neglecting the secondary parasitic capacitance \( C_s \), the Laplace equivalent circuit corresponding to this time interval is presented in Figure 8.

\[ I_r(s) \left( sL_r + \frac{1}{sC_r} \right) = L_r I_o \] (4)

If the angular frequency is \( \omega_r = \frac{1}{\sqrt{L_r C_r}} \) then the current through \( C_r \) is:

\[ I_r(s) = I_o \frac{s}{s^2 + \omega_r^2} \] (5)

Applying the Laplace inverse transform to (5) and shifting to \( t_1 \), results that \( C_r \) is discharged with the current:

\[ i_r(t) = I_o \cos(\omega_r(t - t_1)) \] (6)

The \( C_r \) capacitor voltage is:

\[ v_{cr}(t) = V_{in} - \frac{1}{C_r} \int_{t_1}^{t} I_0 \cos(\omega_r(t - t_1))dt = V_{in} - \frac{I_0}{\omega_r C_r} \sin(\omega_r(t - t_1)) \] (7)

From (7) results that the completely discharge time interval of \( C_r \) can be estimated as:

\[ \Delta t = \frac{1}{\omega_r} \arcsin \left( \frac{V_{in}}{I_o \sqrt{\frac{V_{in}}{C_r}}} \right) \] (8)

For the values used in the simulation presented in Figure 9: \( L_r = 14 \mu \text{H} \), \( V_{in} = 250 \text{ V} \), \( I_o = 2.3 \text{ A} \), using (8) \( \Delta t \) will be 97 ns. The same result for the time needed to discharge \( C_r \) is obtained in simulation, Figure 10. At \( t_1 \) all the diodes \( (D_1, D_2, D_3, D_4) \) will start to conduct immediately.

Figure 8. Laplace equivalent circuit corresponding to the discharge of \( C_r \) capacitor.

Figure 9. Spice equivalent schematic for the discharge of \( C_r \).
If one considers the influence of the $C_s$ secondary parasitic capacitance, which is assumed to be charged at $t_1$, the Laplace equivalent schematic of the converter is presented in Figure 11. It will be later demonstrated that $C_s$ is charged (for the worst case) at:

$$V_{cs}(0) = 2V_{out} \frac{L_r}{L_r + L_{out}}$$  \hspace{1cm} (9)$$

For example, if $L_r = 14 \mu H$ and $L_{out} = 280 \mu H$, then $V_{cs}(0) = 16.4 \text{ V}$. The equations describing the circuit from Figure 11 are:

$$\begin{align*}
I_r(s) + I_{cs}(s) &= \frac{I_0}{s} \\
\frac{V_{cs}}{s} - I_{cs}(s) \frac{1}{L_r} &= L_r I_0 - I_r(s) (s L_r + \frac{1}{s C_r})
\end{align*}$$  \hspace{1cm} (10)$$

After simple mathematical manipulations (10) becomes:

$$\frac{V_{cs}}{s} + \frac{I_0}{s C_r} = I_{cs}(s) \left( s L_r + \frac{1}{s C_1} \right)$$  \hspace{1cm} (11)$$

From (11), results that the expression of the current through the $C_s$ capacitor is:

$$I_{cs}(s) = \frac{V_{cs} C_1}{s^2 L_r C_1 + 1} + \frac{I_0 C_1}{s^2 C_1 (s^2 L_r C_1 + 1)} = \frac{V_{cs}}{s L_r / C_1} \frac{\omega_1}{s^2 + a_1^2} + \frac{I_0}{C_r L_r \omega_1^2} \left( 1 - \frac{s}{s^2 + a_1^2} \right)$$  \hspace{1cm} (12)$$

In (11) and (12), $C_1 = \frac{C_s C_r}{C_s + C_r}$ and $\omega_1 = \frac{1}{\sqrt{L_r C_1}}$.

Applying the Laplace inverse transform to (12) and shifting to $t_1$ results:

$$i_{cs}(t) = \frac{V_{cs}}{s L_r / C_1} \sin(\omega_1 (t - t_1)) + \frac{I_0 C_1}{C_r} \left[ 1 - \cos(\omega_1 (t - t_1)) \right]$$  \hspace{1cm} (13)$$

Figure 10. Spice simulation results for the discharge of Cr.

Figure 11. Laplace equivalent circuit corresponding to the discharge of Cr and Cs.
From (13) the voltage across the $C_s$ capacitor can be calculated as:

$$v_{cs}(t) = \frac{V_{cs}}{C_s + C_r} [C_s + C_r \cos \omega_1 (t - t_1)] - \frac{I_0}{C_s + C_r} [(t - t_1) - \frac{1}{\omega_1} \sin \omega_1 (t - t_1)]$$  \hspace{1cm} (14)

Solving the equation $v_{cs}(t) = 0$ V one gets: $\Delta t = 30$ ns.

The current through the resonant inductor is:

$$i_r(t) = I_o - i_{cs}(t - t_1)$$  \hspace{1cm} (15)

The capacitor $C_r$ will be discharged according to:

$$v_{cr}(t) = V_{in} - \frac{1}{C_r} \int_{t_1}^{t} i_r(t) dt$$  \hspace{1cm} (16)

$$v_{cr}(t) = V_{in} - \left[ \frac{I_0}{C_r} (1 - \frac{C_s}{C_r}) t + \frac{C_s}{C_r} \frac{1}{\omega_1} \sin \omega_1 (t - t_1) \right] + V_c \left( \frac{C_s}{C_r + C_s} \frac{1}{\omega_1} \sin \omega_1 (t - t_1) \right)$$  \hspace{1cm} (17)

After $\Delta t = 30$ ns the voltage on $C_r$ will be: $V_{cap} = 157$ V and $I_{r'} = 2.16$ A.

The Spice circuit is represented in Figure 12, and the simulation results are shown in Figure 13.

Figure 12. Spice equivalent schematic for $t_1$-$t_2$ interval.

Figure 13. Spice simulation results for $t_1$-$t_2$ interval.
As can be seen in Figure 13 the diodes will turn ON immediately after $V_{cs}$ reaches zero, starting from its initial value before $Q_1$ turns OFF. At this moment $t' = 30$ ns the voltage on the $C_r$ capacitor that is also discharging reaches the value of 157 V and the current through the $L_r$ inductor is 2.16 A. The $C_r$ capacitor needs in this case 97 ns to completely discharge from its initial value.

In Figure 14, a detailed set of waveforms is presented for the time interval corresponding to $[t_1 \rightarrow t_2]$. It can be observed that the values obtained with the mathematical and simulation model match closely the experimental measurements. $V_{cr}$ is the voltage measured on the primary of the transformer and corresponds to $V_{inv}$ from Figure 6, $V_{cs}$ is the voltage on the secondary, $V_{rc}$ is the rectified secondary voltage, and $I_{lr}$ is the output current in this case.

![Figure 14. Experimental results for $t_1$-$t_2$ interval.](image)

At $t'$ when $C_s$ is discharged, the Laplace equivalent circuit presented in Figure 15 can be used to compute the $C_r$ voltage.

$$V_{diff} = V_{in} - V_{cap}$$

$$i_r(t) = I_{rr} \cos(\omega_r(t - t')) - \frac{V_{diff}}{L_r} \sin(\omega_r(t - t'))$$

$$V_{Cr}(t) = V_{cap} - I_{rr} \sqrt{\frac{L_r}{C_r}} \sin(\omega_r(t - t')) + V_{diff}[1 - \cos(\omega_r(t - t'))]$$

where $V_{diff}$ is the difference between the input voltage and the initial voltage of $C_r$ at $t'$ and $I_{rr}$ is the current through $L_r$ at $t'$.

![Figure 15. Laplace equivalent circuit corresponding to $C_s$ discharged.](image)
The diodes $D_2$, $D_3$ will start to conduct after $t'$ when $C_s$ is completely discharged. At $t'' = 97$ ns when $V_{cs}(t'') = 0$ the resonant inductor current, $I_r$, is flowing through the body diode $D_{in2}$ of $Q_2$, decreasing with a slope equal to $V_{in}/L_r$. Now $Q_2$ can be switched ON. The current through $D_1$ is decreasing and through $D_3$ is increasing. At $t_3$, $D_1$ current is zero and $I_r = I_o$.

When $C_s$ is charged at a low voltage, its influence on the $C_r$ discharging time is negligible.

### 4.2. Operation during $[t_3-t_4]$ interval, immediately after $t_3$

At $t_3$, $D_1$ and $D_4$ diodes turn OFF, and the output current continues to flow through $D_3$ and $D_2$. For a short time after $t_3$ the current through $L_{out}$ can be considered constant, and this inductance is replaced by a constant current source.

The Laplace equivalent model corresponding to this time interval is presented in Figure 16.

**Figure 16.** Laplace equivalent circuit corresponding to $[t_3-t_4]$ time interval.

The equations describing the circuit from Figure 16 are:

\[
\begin{align*}
I_r(s) &= \frac{I_o}{s} + I_{cs}(s) \\
\frac{V_{in}}{s} - sL_rI_r(s) + L_rI_o &= \frac{1}{\sqrt{s}}I_{cs}(s)
\end{align*}
\]

After simple mathematical manipulation of (21) the expression of the $C_s$ current is:

\[
i_{cs}(t) = \frac{V_{in}}{\sqrt{L_r/C_s}} \sin(\omega(t - t_3))
\]

where $\omega = \frac{1}{\sqrt{L_rC_s}}$.

The voltage across the $C_s$ capacitor can be calculated as:

\[
v_{cs}(t) = \frac{1}{C_s} \int_{t_3}^{t} \frac{V_{in}}{\sqrt{L_r/C_s}} \sin(\omega(t - t_3))dt = V_{in}[1 - \cos(\omega(t - t_3))]
\]

As it can be deduced from (23), $V_{cs}$ voltage reaches its maximum value $V_{cs,max} = 2V_{in}$ after a time interval equal to $T/2 = \pi/\omega$. This equation is very useful for designing the output clamping circuit.

Spice simulation for the schematic in Figure 17 describing the converter immediately after $t_3$ is presented in Figure 18.
As it can be observed in Figure 18, immediately after $t_3$ the maximum voltage on the $C_s$ capacitor reaches the double input value, in this case, $V_{in} = 250\,\text{V}$. The value represents the voltage measured on the secondary side of the transformer.

In Figure 19 are highlighted the experimental results for the interval $t_3$-$t_4$ immediately after $t_3$. It can be observed that there is a difference between the simplified model used in the simulation and the experimental values. This difference is due to the fact that the simulation takes into account the worst-case scenario for the maximum possible $V_{cs}$ voltage (obtained for worst-case $R_1 = 0\,\Omega$).

For the experimental setup, if a secondary parasitic equivalent resistance $R_1 = 70\,\Omega$ is considered, the damping ratio of the secondary voltage is given by:

$$\xi = \frac{R_1}{2 \sqrt{\frac{L_r}{C_s}}} = \frac{70\,\Omega}{2 \sqrt{\frac{14\,\mu\text{H}}{100\,\text{pF}}}} \approx 0.095$$  \hspace{1cm} (24)

From (24) results that secondary peak voltage can be estimated with:

$$V_{c,\text{max}} = V_{in} \left(1 + e^{-\frac{\pi \xi}{\sqrt{1-\xi^2}}}\right) = 250\,\text{V} \left(1 + e^{-\frac{\pi \times 0.095}{\sqrt{1-0.095^2}}}\right) \approx 434\,\text{V}$$  \hspace{1cm} (25)
4.3. Operation during \([t_4-t_5]\]

At \(t_4\), \(Q_3\) turns off, and the energy transfer from primary to the output stops. The output capacitor \(C_{o3}\) of \(Q_3\) starts to charge, and the output capacitor of \(Q_4\) starts to discharge. If one considers \(C_r = C_{o3} + C'_{o4}\), then the equivalent schematic of the converter corresponding to this time interval is presented in Figure 20.

Since only \(D_1\) and \(D_4\) are on, results that \(C_r\) starts to be charged with an approximately constant current (the output current \(I_o\)), thus in general, this time interval is very narrow.

In this case, the voltage across the \(C_r\) capacitor is given by:

\[
v_{cr}(t) = \frac{1}{C_r} \int_{t_4}^{t} I_0 dt = \frac{I_0}{C_r} (t - t_4)
\]

\(\text{(26)}\)

\[\text{Figure 20. Equivalent circuit corresponding to } [t_4-t_5'] \text{ time interval.}\]

From Equation (26), results that the charging time interval of the \(C_r\) capacitor can be estimated with (27) supposing that during this time interval the capacitor \(C_s\) will remain charged at the approximately same voltage \(V_{in}\). A detailed analysis which takes into account the influence of \(C_s\) can be made, as in Section 4.1.

\[
t'_4 - t_4 = \frac{V_{in}C_r}{I_0}
\]

\(\text{(27)}\)

The equations describing the circuit in Figure 21 are:

\[
\begin{align*}
I_r(s) + I_{cs}(s) &= \frac{I_0}{s} \\
\frac{V_{in}}{s} - \frac{1}{sC_r} I_{cs}(s) &= L_tI_0 - sL_dI_r(s)
\end{align*}
\]

\(\text{(28)}\)
The equivalent circuit corresponding to this time interval is presented in Figure 22, supposing that \( C_r \) is already charged. During \([t_4'-t_5]\) time interval, as seen in Figure 23, the energy stored in \( C_s \) shall be evacuated through \( D_1 \) and \( D_4 \).

From (23) results that \( C_s \) current is given by:

\[
I_{cs}(s) = \frac{V_{in}}{\sqrt{L_r/C_s}} \frac{\omega}{s^2 + \omega^2}
\]

(29)

Applying the Laplace inverse transform to (29) and shifting to \( t_4' \), results that \( C_s \) is discharged by a sinusoidal current, as in (22). The equation of the voltage across the \( C_s \) capacitor becomes in this case:

\[
v_{cs}(t) = V_{in} - \frac{1}{C_s} \int_{t_4'}^{t} \frac{V_{in}}{\sqrt{L_r/C_s}} \sin(\omega(t-t_4')) dt = V_{in} \cos(\omega(t-t_4'))
\]

(30)

As supposed before, the \( C_r \) capacitor will start to charge according to Equation (26), while for the first part of this period of time the voltage on the \( C_s \) capacitor remains constant at the 250 V in this case. The energy stored in \( C_s \) shall be evacuated through the \( D_1 \) and \( D_4 \) diodes.

In Figure 24 are highlighted the experimental results for the interval \( t_4'-t_5 \). It can be observed that the results match closely the values obtained with the mathematical and simulation models.
4.4. Operation during $[t_5-t_7]$

From (30) results that at $t_5$ (after a time interval equal to $T/4 = \pi/2\omega$), the voltage across $C_s$ reaches zero, and the $i_{cs}$ current reaches its maximum value. After this time interval, due to the reverse voltage polarity on $C_s$, the energy stored in it shall be evacuated almost instantaneous through $D_2$ and $D_3$, which turn ON and keep the voltage on $C_s$ equal to zero. At $t_6$, $Q_4$ turns ON with ZVS, and the primary output reflected current continues to flow through the body diode $D_{in4}$ of $Q_4$. The $D_1$ and $D_4$ diodes are turned ON together with $D_3$ and $D_2$ until $t_7$, when the $L_r$ current reaches again the value of the output current reflected in the primary of the transformer. After $t_7$, the output current flows again only through $D_1$ and $D_4$. If one considers that in $[t_5-t_7]$ time interval the $L_r$ current is approximatively constant and the diode currents $i_{D1} = i_{D4}$ and $i_{D3} = i_{D2}$, then the equivalent schematic of the converter corresponding to this time interval is presented in Figure 25.

The equations describing the circuit in Figure 25 are:

$$\begin{align*}
  i_{D1} - i_{D2} &= I_r \\
  i_{D1} + i_{D2} &= i_o
\end{align*}$$

From (31) results that:

$$i_o - I_r = 2i_{D2}$$

(32)
Since this difference between the output current and the reflected primary current is given by the current drop through $C_s$ at $t_5$, results that:

$$\begin{align*}
I_{D1} &= I_o - I_{cs,\text{max}} \\
I_{D2} &= \frac{I_{cs,\text{max}}}{2} - \frac{V_{in}}{2\sqrt{L_s/C_s}}
\end{align*}$$

(33)

where $I_{D1}$ and $I_{D2}$ are the current values through $D_1$ and $D_2$ in $t_5$ and $I_{cs,\text{max}}$ is the maximum value of the $C_s$ current.

The diodes $D_2$ and $D_3$ are turning OFF at $t_7$, when the current through $L_r$ reaches the value of the current through $L_{out}$.

The equations describing the relation between the $L_r$ and $L_{out}$ currents are:

$$\begin{align*}
I_r &= I_o - I_{cs,\text{max}} \\
i_{t0}(t) &= I_o - \frac{V_{out}}{L_{out} + L_r} (t - t_5)
\end{align*}$$

(34)

Since the $L_r$ and $L_{out}$ currents are again equal at $t_7$, results that:

$$I_o - I_{cs,\text{max}} = I_o - \frac{V_{out}}{L_{out} + L_r} (t_7 - t_5)$$

(35)

From (35) results that $[t_5-t_7]$ time interval can be estimated as: 1.2 µs.

4.5. Operation during $[t_7-t_8]$  

At $t_7$, $D_2$ and $D_3$ diodes turn OFF, and $D_1$ and $D_4$ continue to stay ON until $t_8$, when $Q_2$ transistor turns OFF. The equivalent circuit from Figure 26 presents the Laplace model of the converter corresponding to $[t_7-t_8]$ time interval. In this case, the initial currents through $L_r$ and $L_{out}$ have no influence.

The voltage across the $C_s$ capacitor in $[t_7-t_8]$ time interval is:

$$V_{cs}(s) = V_{out} \frac{Z_p}{sZ_p + sL_{out}} = V_{out} \left( \frac{1}{sL_r + s^2L_{out}C_s} \right)$$

(36)
\[ V_{cs}(s) = \frac{V_{out}}{L_{out}C_s} s \left( s^2 + \frac{1}{L_{out}C_s + L_rC_s} \right) \]  

(37)

If \( Z_p = \frac{\frac{L_r}{sL_r}C_s}{sL_r + 1/sL_r} = \frac{\frac{L_r}{sL_r}}{1+1/L_rC_s} \) is the impedance of the parallel connection \( L_r - C_s \) and \( \omega_2 = \frac{1}{\sqrt{L_{out}C_s + L_rC_s}} \) then (37) becomes:

\[ V_{cs}(s) = \frac{V_{out}}{L_{out}C_s} s^2 \left( s^2 + \omega_2^2 \right) = \frac{V_{out}}{L_{out}C_s} \omega_2^2 \left( \frac{1}{s^2} - \frac{s}{s^2 + \omega_2^2} \right) \]  

(38)

Applying the Laplace inverse transform to (38), results that the voltage across the \( C_s \) capacitor in \([t_7-t_8]\) is:

\[ v_{cs}(t) = \frac{V_{out}L_r}{L_{out} + L_r} \left[ 1 - \cos \omega_2 (t - t_7) \right] \]  

(39)

Spice simulation for the schematic in Figure 27 describing the converter in \([t_7-t_8]\) interval is presented in Figure 28. As can be observed the \( C_s \) capacitor charges at the voltage deduced with Equation (9). So this is the worst-case values of \( V_{cs}(0) \) for this specific analysis.

![Figure 27. Spice equivalent schematic for t7-t8 interval.](image)

![Figure 28. Spice simulation results for Vcs and lLr immediately after t7.](image)

As it can be deduced from (39), \( v_{cs} \) voltage reaches the maximum value \( V_{cs,max} = 16.4 \) V after a time interval equal to \( T_2/2 = \pi/\omega_2 \):

\[ V_{cs,max} = \frac{2}{L_{out} + L_r} \]  

(40)

In Figure 29 can be observed that the voltage across the \( C_s \) capacitor in \([t_7-t_8]\) is \( V_{cs} = 16.4 \) V corresponding with the value obtained with Equation (40).
The analysis was performed in continuous conduction mode for both, leading and legging leg of the frequency transformer, with all the elements referred to the secondary side. The complete switching cycle considered for the analysis was divided into seven time intervals to better highlight the effect of the parasitic capacitance. A simplified Laplace equivalent circuit for each operation time interval was developed and the corresponding equations where derived. The values obtained through mathematical manipulation are compared with the ones obtained with the Spice simulation models created for each time interval. The simulation models validate the mathematical description on each time interval and provide an intuitive and easy to adapt method for analyzing a phase shift converter in detail.

Equations (9) and (23) can be used to design active snubbers. The effect of the stray capacitance can be observed in the experimental waveforms presented in Figure 29. Because of the short amount of time and small value that the \( V_{cs}(0) \) exhibits most of the time, its presence is ignored by designers resulting in flawed designs. The experimental waveforms were measured on the PSFB converter prototype. It can be observed that the experimental measurement prove that the mathematical model and the equivalent simulation circuits are valid and can be used for design optimizations.

5. Conclusions

This paper presents a detailed analysis of the PSFB converter that accounts for the stray capacitance of the transformer secondary winding and the capacitances of the diodes in the bridge rectifier. The analysis was performed in continuous conduction mode for both, leading and legging leg of the primary bridge and for a complete switching cycle, starting from an equivalent electric circuit of a high frequency transformer, with all the elements referred to the secondary side. The complete switching cycle considered for the analysis was divided into seven time intervals to better highlight the effect of the parasitic capacitance. A simplified Laplace equivalent circuit for each operation time interval was developed and the corresponding equations where derived. The values obtained through mathematical manipulation are compared with the ones obtained with the Spice simulation models created for each time interval. The simulation models validate the mathematical description on each time interval and provide an intuitive and easy to adapt method for analyzing a phase shift converter in detail.

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6. Discussion

The main objective of the paper is to highlight and better understand the effects of the parasitic capacitances on the PSFB. By using the equations and simulation models presented in Section 4 the design process of such a converter simplifies, and there is no need for implementing new complicated control techniques if the negative effects of the stray capacitance are taken into account. By determining the maximum voltage on the stray capacitance, an active clamping circuit can be designed. As highlighted in the Introduction section, such high power density converters are needed more and more in the automotive industry, due to the development of electric cars and off and on board charging stations. Using active snubbers in this equipment is necessary, due to high-efficiency requirements and space constraints that affect the heat dissipation needed for the passive snubbers approach. This type of analysis, presented in this paper, helps designers and scientist to better understand the effects that appear in high density power converters. If these effects are ignored it can
lead to a design with a very high number of iterations between the simulation stage and experimental measurements. Many times the redesign is the solution adopted.

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