FPGA-extended Modified Harvard Architecture

Philippos Papaphilippou
Imperial College London, UK
pp616@imperial.ac.uk

Myrtle Shah
ChipFlow Ltd, UK
gatecat@ds0.me

ABSTRACT

This paper introduces a computer architecture, where part of the instruction set architecture (ISA) is implemented on small highly-integrated field-programmable gate arrays (FPGAs). It has already been demonstrated that small FPGAs inside a general-purpose processor (CPU) can be used effectively to implement custom instructions and, in some cases, approach accelerator-level of performance. Our proposed architecture goes one step further to directly address some related challenges for high-end CPUs, where such highly-integrated FPGAs would have the highest impact, including access to the memory hierarchy with the highest bandwidth available. The main contribution is the introduction of the “FPGA-extended modified Harvard architecture” model to enable software-transparent context-switching between processes with a different distribution of instructions. The simulation-based evaluation of a dynamically reconfigurable core shows promising results for single and multi-processing, approaching the performance of an equivalent core with all enabled instructions, and better performance than when featuring a fixed subset of the supported instructions. Finally, the feasibility of adopting the proposed architecture in today’s CPUs is studied through the prototyping of fast-reconfigurable FPGAs and studying the miss behaviour of opcodes.

Keywords—computer architecture, reconfiguration, custom instructions, FPGA, memory hierarchy, ISA, extensions

1. INTRODUCTION

There has been enormous progress around traditional software on today’s CPUs. This has led to easier development through high-quality libraries and debug tools, as well as relatively mature programming models and verification routines. Additionally, a variety of software and hardware abstractions have enabled portability of code, such as with virtual memory and cache hierarchies, and enabled more effortless increase in performance, such as through instruction-level parallelism. However, general purpose processors leave a lot to be desired in terms of performance, hence the increase in use of computation offloading to specialised processors. These include graphics processing units (GPUs), field-programmable gate arrays (FPGAs) and even purpose-built silicon in the form of application-specific integrated circuits (ASICs).

One consideration in today’s hardware specialisation technologies is the fact that they are mostly based on the non-uniform memory-access model (NUMA). Large off-chip memories are found in the majority of today’s high-end FPGA offerings, resulting in power-hungry and expensive setups, as well as in limitations in programming models, and complicating deployment and data movement.

While promising techniques like wide Single-Instruction Multiple-Data (SIMD) instructions [23] in CPUs could be considered an attempt to close the gap between specialised and general purpose computing [11], this gap is wider than it has ever been. This is because of the increased need for highly customised architectures in trending workloads [37], whose functionality could not be efficiently expressed with a fixed general purpose ISA and microarchitecture.

The modified Harvard architecture is the most common computer architecture in today’s systems. It is similar to the Von Neumann architecture, in the sense that the higher-levels of the cache hierarchy share the same memory address space. The original Harvard architecture distinguished between an instruction address space and a data address space [41]. With the modified Harvard architecture this feature is reminiscent in the caches closer to the cores [20], which helps with modern micro-architectural features such as pipelining.

In this paper, we extend the modified Harvard architecture to introduce FPGA-based instruction implementations in general purpose systems. In contrast to current research, this goes beyond embedded or specialised processors, and introduces multi-processing for operating systems and finer-grain reconfiguration, as with standardised instruction extensions. A feasibility study shows promising performance for supporting reconfigurable extensions on-demand, especially when supporting fast FPGA reconfiguration.

The list of contributions goes as follows:

1. The “FPGA-extended modified Harvard Architecture”, a novel computer architecture to introduce FPGAs working as custom instructions, enabling context-switching and other advanced concepts for higher-end applications.

2. A comprehensive evaluation of fine-grain reconfiguration at the instruction-level in a benchmark suite. This is done in an exemplary environment where there is competition for two extensions, but no space for both.

3. Related insights such as with regards to multi-processing and the impact of the reconfiguration time and the operating system’s scheduler properties.

4. A feasibility study that elaborates on the readiness of current SoC technology to adopt the new architecture with optimisations for fast reconfiguration.

The paper first introduces the challenges for FPGA-based acceleration (section 2), and our proposed solution (section 3).
2. CHALLENGES

The research on FPGAs implementing custom instructions can be considered an attempt to overcome a series of challenges in current systems that use discrete FPGAs (2.1). This work addresses some of the challenges found in existing research on reconfigurable instructions (2.2).

2.1 Current CPUs and discrete FPGAs

One challenging design decision that relates to both hardware and software is the selection of instructions that would be more beneficial to include as part of the instruction set architecture (ISA). With a fixed ISA, vendors can select a subset of instructions, such as with the modularity of RISC-V [3], or design custom instructions for specialised applications. For general purpose computing it is difficult to predict what the most appropriate instructions will be. For instance, some applications may be ephemeral, as with some neural network models or cryptocurrencies, for which specialised hardware becomes obsolete faster.

Another challenge is hardware complexity. Supporting a high-number of instructions is expensive, but sometimes this has been unavoidable for widening the applicability of general purpose processors. For example, Intel’s AVX2 and AVX-512 include thousands of instructions [23], and RISC-V’s unratified vector extension hundreds [1]. The related implementation complexity, such as with AVX-512, is associated with a decrease in operating frequency and power efficiency, and area increase [12, 18]. Additionally, AVX-512 is suboptimal for certain workloads, where a serial code could surpass them in terms of performance and scalability [12]. Expanding the ISA can also harm the SoC scalability to many cores, which heavily relies on core miniaturisation and power efficiency.

When using FPGAs as accelerators, one of the most limiting bottlenecks to performance is the bandwidth to main memory [31]. For example, even with an Intel Xeon+FPGA prototype, although the FPGA is directly connected to the memory controller it only achieves 20 GB/s [7]. The memory hierarchy tends to always favour CPU performance, hence the presence of expensive off-chip memories in high-end FPGA boards. This heterogeneity is considered to impact FPGA development, as well as to increase the cost and deployment of FPGAs in the datacenter [32].

2.2 FPGAs implementing instructions

The basic limitation of the related work on FPGA-based instructions is their focus on embedded and/or heterogeneous systems, with no notion for multi-processing, context-switching and advanced micro-architectural features. The use of embedded FPGAs (eFPGAs) has many practical applications in embedded systems [5, 25], but there is currently no computer architecture to “hide” reconfiguration from traditional software.

One challenge in the existing methods of introducing eFPGAs as custom instructions is the need for manual intervention for reconfiguration. Although the recommended procedures to develop and load bitstreams can be well documented, deviating from conventional software development could be detrimental for achieving a wider adoption [5].

By initially focusing on highly-customised instructions and more complex accelerators in related research (section 7), there has been less opportunity for modern processors to gradually adopt small reconfigurable regions as part of their core. Custom instructions and accelerators are more complex to comment on, such as by introducing additional design decisions, and can quickly shift the focus to specialisation and optimisation.

3. SOLUTION

The proposed solution is the “FPGA-extended modified Harvard Architecture”, which unifies the address space for instructions, data, as well as for FPGA bitstreams. When compared to the traditional modified Harvard architecture, the proposed solution also adds a separate bitstream cache at level 1, to provide bitstreams for FPGA-instructions after an instruction opcode is ready. The idea is for a computing core that features reconfigurable slots for instructions, to be able to efficiently fetch instruction bitstreams transparently from the software. Figure 1 introduces the proposed computer architecture in high-level with respect to the memory hierarchy.

![Figure 1: FPGA-extended modified Harvard architecture](image)

Table 1 elaborates on the differences between common architectures with respect to the memory hierarchy, and after the introduction of FPGA-based accelerators. The modified Harvard architecture can be seen as a combination of the Von Neumann and the Harvard model, as it uses a shared address space (hence using the same datapath for the shared caches), but it uses a split L1 cache for instruction and data for easier memory performance. Today, the conventional use of FPGAs are based on heterogeneous systems with a host processor based mostly on the modified Harvard architecture (ignoring the multi-core aspect). In this case, the FPGA is used as a co-processor with secondary memories providing its bitstreams, usually manually. Since the bitstreams are not considered to be in the same address space, the mediums through which the bitstreams are arrive on the FPGA are seen
as a separate memory hierarchy to facilitate this comparison (e.g. through a network and then an EEPROM (electrically erasable programmable read-only memory)).

The memory performance notions here could be seen as effort metrics, as higher performance can be achieved at the expense of hardware and software complexity. One such example is for today’s high-end FPGAs in the “conventional heterogeneous” class that utilise an on-board memory in a non-uniform memory access (NUMA) manner. While it can provide high local bandwidth, the access to main memory is still significantly degraded when compared to the host processor’s. Thus, when applicable, specialised programming models are used to exploit the local memory [17].

**Bitstream cache.**

A separate cache specifically designed for FPGA bitstreams can increase the performance of the reconfigurable core. The first reason is that, similarly to today’s modified Harvard architecture, the L1 instruction and data caches are still separated and connected to a unified cache, allowing easier simultaneous memory accesses for pipelining the instructions. Since the instruction disambiguator unit waits for an instruction opcode to be ready, a bitstream fetch phase can be placed subsequently to the instruction decode pipeline stage in heavily-pipelined processors. Secondly, the bitstream cache is also separated to allow different dimensions or speeds than the rest of the caches, such as with wider blocks to facilitate the increased data width to carry bitstreams, as opposed to instructions (see section 6). Thus, separating the bitstream cache relates more to the implementation efficiency, as the aforementioned high-level functionality could be done without a separate bitstream cache (when seeing bitstream as data or instructions).

**Instruction disambiguator.**

This architecture assumes that the computing core features fast-programmable FPGAs that can be used to implement instructions. This can be achieved with a small cache-like structure, the instruction disambiguator, shown in figure 2. On every instruction decode there is a request to this unit to see if there is an instruction implementation for the requested instruction. It operates as a small fully-associative cache and uses opcodes (plus any additional fields for defining functions) as tags to determine the bitstream locations. On an opcode miss it requests the instruction bitstream from the bitstream cache, while on a hit it multiplexes the operands to the appropriate slot.

**Table 1: Comparison of the proposal to existing computer architectures**

| Computer Architecture | Von Neumann | Harvard | Modified Harvard | Heterogeneous (Modified Harvard) | FPGA-extended Modified Harvard |
|-----------------------|-------------|---------|------------------|----------------------------------|-------------------------------|
| L1 datapaths          | Shared for I/D | Separate for I, D | Separate for I, D | Separate for I, D, (B) | Separate for I, D, B |
| Address space/ L2+ datapaths | Shared for I/D | Separate for I, D | Shared between I/D | Shared for I, D | Shared between I/D |
| Memory performance   | Low          | High    | High             | High                             | High                          |

*Legend – I: instructions, D: data, B: bitstreams*

This enables the applications to be agnostic of the reconfiguration aspect. An operating system can provide the basic ISA extensions (or part of them) in the form of bitstream libraries, and the hardware shall be able to dynamically fetch the necessary bitstreams on demand. Sharing the same virtual or physical address space for the bitstreams provides the facility to keep bitstreams in software binaries, so that they can provide custom instruction extensions alongside their data segment for customisation and acceleration potential.

**4. METHODOLOGY**

As our proposal concerns a fundamental modification of the computer architecture and targets high-end hardened processors, the most accurate evaluation methodology would include fabrication. As this would be impractically expensive, the general philosophy of our methodology is to try to abstract and generalise the unexplored variable (such as by studying the worst case) indirectly-related to the main contribution, while evaluating new concepts in more depth.

**4.1 Simulated hardware**

The performance evaluation framework is based on an open-source FPGA-optimised RISC-V softcore [32], which is extended to facilitate our study on the system effects of our proposal.

The main addition is the instruction slot disambiguator. Its functionality here is to processes opcodes (and related fields) and add latency when there is an instruction slot miss. All required instructions actually pre-exist on the softcore. The instruction opcodes are first being resolved through the instruction cache, and the instruction slot disambiguator here
works as an L0 instruction cache that uses opcodes as tags and adds latency on opcode misses. The opcodes are encoded internally using a look-up table according to what subset of instructions we consider as part of the same slot. For example, it would make sense to share the main logic of integer addition with integer subtraction.

Essentially, this module is only used to provide “artificial” latency, emulating the performance overhead of the proposal as observed in software. The amount of added latency on slot misses is parameterisable to approach covering a wider range of possible reconfiguration arrangements. In this way, the system effects are studied without relying on a specific and currently-limiting FPGA reconfiguration architecture (see section 6.1).

The core specification was originally RV32IM [32], where “I” is the base 32-bit integer and “M” the integer multiplication and division extension [3]). This study extends it with the “F” extension for single-precision floating-point support. Another modification is the addition of the RISC-V “Zicsr” control and status register instructions [38]. This is done to enable access to certain control and status registers (CSRs) related to the use of a real operating system. Specifically, we add a subset of RISC-V’s CSRs (mstatus, mie, mcause, mepc and mtvec), which was the minimum subset that was required to support FreeRTOS by using machine-level privileges (under FreeRTOS v202112 and GCC 10.1.0). Timer interrupts are also now enabled through the addition of the machine-level memory-mapped registers mtime and mt imecmp, in order to support context switching.

Most of the “I” instructions introduce a single cycle of latency, while the “M” instructions occupy 4 non-blocking cycles of latency. The “F” extension is pipelined with a latency of 6 cycles, excluding the fused multiply-add instructions that yield a latency of 12 cycles.

The resulting codebase is synthesisable and also passed benchmark-based test cases on a Xilinx Zynq UltraScale+ FPGA, though we opted to use Verilog simulations instead. This is for convenience, as the resulting framework ran relatively fast in simulation. Additionally, the memory space required for the benchmark suite is less than this softcore’s cache, hence studying the interaction with a real DRAM was not considered of value here.

4.2 Software

The benchmark suite is Embench [33], providing a selection of benchmarks with different attributes of interest (such as compute or memory-intensive). The Embench benchmark suite was ported for use in our evaluation infrastructure, and each benchmark was made to run as a thread instead of a process. This required some additional modification, such as in the included beeb library that was originally supposed to streamline some common library functions with diverse implementations, but was not designed for multiple callers. Any local data are now passed as pointers into the beeb functions, such as for generating random numbers deterministically under a consistent seed, and for managing heap memory.

Originally, only one of the benchmarks (miner) used a single-precision floating point arithmetic. Thus, four more (wikisort, st, nbody and cubic) that used double-precision operations are modified to use single precision to facilitate the purposes of this study. This also involved appending the letter “f” to any calls of the math.h libraries sqrt, fabs, pow, cos, acos and atan. The pre-defined verification step is modified to comply with the appropriate values when using less precision by obtaining results from a modern laptop core (AMD Ryzen), hence the reported numerical values should not be used as a reference for other purposes. The benchmarks are compiled with the -O3, -ffast-math and -fno-schedule-insns flags.

![Figure 3: Unique instr. in Embench, “F” in green and “M” in blue shades. The remaining are the same as crc32.](image)

The distribution of unique instructions per benchmark after compiling with both “F” and “M” (RV32IMF) is visualised in figure 3. For every benchmark, the unique instruction count is found with the help of objdump. While the base and “M” instruction use is relatively consistent, the 5 floating-point benchmarks are found to differ more with regards to their selection of “F” instructions.

Finally, an operating system was needed to provide the multi-processing capability. The selected operating system is FreeRTOS [8], a real-time operating system. This provided a minimal framework allowing easier experimentation with the task scheduler. FreeRTOS can be seen as a multi-threading library [9]. Thus, a single binary is obtained, containing both FreeRTOS task scheduler and the benchmarks as threads. This is run as a bare-metal application by the adopted softcore to study the effects of context switching under our proposal.

1The latter flag is used to avoid an outlier for the benchmark nettle-sha256, where enabling the “F” extension doubles the runtime.
for multi-programming. The main modification to FreeRTOS was the porting context-switching routine to support the “F” extension in our platform.

### 4.3 Reconfigurable slot granularity

With respect to the size and complexity of the reconfigurable instructions, we explore three compartmentalisation scenarios, representing different logic granularities starting from the finest:

1. **One slot per instruction, 8 slots**: In this scenario, each reconfigurable slot fits exactly one instruction from “F” or “M”. This may be less representative for simple instructions, such as floating-point addition (fadd.s) and subtraction (fsub.s) that can share their adders, but it is included for the sake of completeness.

2. **One slot per instruction group, 4 slots**: This scenario groups instructions into single reconfigurable regions according to their logic similarity. There are 3 groups for the “M” extension (mul, mulh, mulhsu, mulhu, div, divu, rem, remu), and 7 groups for the “F” extension (fadd.s, fsub.s, fmul.s, fdiv.s, fsign.s, fsignx.s, fmin.s, fmax.s, flt.s, flt.s, fsgnj.s, fsgnjn.s, fsgnjx.s, fmin.s, fmax.s, fadd.s, fsub.s, fmin.s, fmax.s, fadd.s), totalling 10 groups.

3. **One slot per extension, 1 slot**: This scenario involves one slot and causes a slot reconfiguration on every use of an instruction of the other extension. For “M” and “F” this may not be representative, but can be generalised for applications competing for their own larger instruction accelerators.

This emulates an environment where the CPU has no space for implementing all extensions, and the workload exhibits competitiveness for a limited number of instruction slots.

### 4.4 Feasibility study

The evaluation of the feasibility (section 6) of the approach provides more isolated studies than the performance evaluation (section 5). This is because the goal is to provide examples and insights using current technologies and more demanding software that impacts SoC design. Thus, different frameworks are used in this section, though it also uses the findings of the performance evaluation to reach its conclusions.
Figure 5: Benchmark classification based on the speedups of RV32IM and RV32IF over RV32I

The performance of the class that is improved by both “F” and “M” is verified to be further improved when having both “F” and “M” in the specification. This is observed in the series of RV32IMF in figure 4. An exception is minver, whose RV32IF performance is very close to RV32IMF, indicating that its reliance on “M” can mostly be replaced by “F”.

5.2 Single-program

For the evaluation of the proposed architecture under single benchmarks, we select the later class from the classification of the previous section (“improved by both F and M”). This is done to focus on workloads where there is demand for both instruction extensions, before introducing multi-processing. Additionally, this section provides experiments for all reconfiguration granularity scenarios of section 4.3, and is also used to narrow down the well-performing configurations before introducing the effects of an operating system.

In this experiment with simulated reconfigurability, there are three indicative series for the bitstream miss latency from the instruction slot disambiguator. These are 10-cycle, a 50-cycle and a 250-cycle latencies representing both reconfiguration technologies that approach a latency closer to that of CPU instructions, and slower which could be achievable with more traditional partial reconfiguration techniques.

Figure 6 presents these results. The y-axes show the speedups/ slowdowns over when running with a fixed spec-

Figure 6: Approaching RV32IMF with reconfigurability for single benchmarks

ication with both “M” and “F” (RV32IMF). There is also the max(IM, IF) series, which represents the maximum performance between the fixed specifications RV32IM and RV32IF. This is done to see whether the latency overhead of the reconfigurable approach can still yield a competitive performance over the most appropriate fixed extension per benchmark.

As it can be seen from the results, the most important factor for performance appears to be the reconfiguration latency, at least here where there is frequent interchange between instructions of different extensions.

The behaviour between the selection of the reconfiguration granularity scenarios seem to be relatively similar with regards to the slowdowns when varying the reconfiguration latency. The worst scenario is the third (one slot per extension), with its 10-cycle average at 55% the speed of RV32IMF, being closer to the 250-cycle of the first scenario (one slot per instruction) at 52% than the first and second’s 10-cycle at over 90% of RV32IMF performance. This expected as an instruction miss on the disambiguator will cause the entire extension to be evicted for replacing it with the extension of the requested instruction.

The best performing scenario is the first, but this also relates to the number of slots. For example, if a benchmark only uses signed multiplication and not unsigned, the multiplication operation would still take exactly one slot in scenarios 1 and 2. Given that the scenario 2 is more representative (see section 4.3), the rest of the study only considers scenario 2 and variations, though such design choices would also relate to the logic complexity of individual instructions in such future systems.

One observation when selecting scenario 2 with a 50-cycle
Figure 7: Comparing the reconfigurable approach (with 2, 4 or 8 slots) to different subsets of RV32IMF in a multi-program environment, under different operating system scheduler timings. All series are sorted individually.

5.3 Multi-program

The effects of multi-processing are studied with the help of an operating system (FreeRTOS). A periodic interrupt is set by its task scheduler, responsible for context-switching. Each task is a benchmark, and the FreeRTOS scheduler enforces a round-robin priority between the tasks. A pair of benchmarks are run through two independent infinite loops, and once one of them finishes its predefined number of iterations, the operating system terminates.

Following the benchmark classification of section 5.1, the benchmark category that is not improved by “F” or “M” (“insensitive”) is not considered. The studied pairs are combinations between two of the five benchmarks that are improved by “F” and “M” (totalling \( \binom{5}{2} = 10 \)) and combinations between one from the latter category with one from the eight benchmarks that are only improved by “M” (totalling \( 5 \times 8 = 40 \)). The remaining combinations are omitted because they do not compete for slots, such as with pairs of benchmarks that are only improved by “M”, as all the reconfiguration scenarios allow the entire “M” to fit inside the slots, and “M” is a relatively small extension.

Figure 7 presents the results of this experiment under scenario 2 with a 50-cycle latency from the single-program experiments (“one slot per instruction group, 4 slots”), as well as with variations of it for a different number of slots (2 and 8). The latter variations are added to elaborate on the slot interaction with this multi-program case, as the competitiveness between the slots is increased. The y-axes are the average speedups for each of the paired benchmarks when compared to their corresponding runtimes with RV32IMF\(^3\). The left plots in figure 7 use binaries compiled for a 1000-cycle (1K) timer interrupt for context-switching, while the right plots present the results for a 20-fold increased timer interrupt delay. With the shorter 1000-cycle delay, all runtimes increase due to the additional instructions coming from the interrupt handler of the operating system. However, due to the different instruction distributions amongst the benchmarks, this also increases the instruction slot misses, hence the 20K-cycle versions improve the speedup of the reconfigurable approaches when compared to the same baseline. For

\(^3\)There are a few outliers (with wikisort) in the RV32IM series, obtaining a speedup > 1 over RV32IMF due to the compiler heuristics.
instance, the average speedup of 4-slot series improves from 0.62 to 0.71 (i.e. from 38% to 29% slowdown) for the top selection of pairs, and from 0.82 to 0.9 for the benchmark combinations on the bottom of the figure.

One observation when combining the benchmarks of the same class (figure 7 top) is that the reconfigurable approach remains at the similar levels of performance degradation as with the last section (single-program). For instance, the average speedup for the 4-slot with 50-cycle reconfiguration and a 20K-cycle timer is 0.71, while the last section’s corresponding average was also around 0.71.

From figure 7 (bottom right) we can see that the potential of reconfiguration is relatively higher when combining benchmarks with different extension preferences. The average speedup over RV/32IMF for the 2-slot, 4-slot and 8-slot approaches is 0.62, 0.9 and 0.94 respectively, under 20K-cycle interrupts.

The proposed reconfigurable approach is shown to be more well-rounded than fixed extensions. For example, RV/32IF performs significantly better than RV/32IM in the pairs figure 7 left, but this is reversed for the pairs of the right part. When considering all 50 of the aforementioned benchmark combinations for 20K cycle interrupts, the 4-slot version is 3.39x, 1.48x and 2.04x faster on average when compared to RV/32I, RV/32IM and RV/32IF respectively, at an average of 0.82x the performance of RV/32IMF. The reconfigurable approach also has relatively less variation between its performance with different benchmark combinations. Finally, fine-tuning the operating system’s scheduler parameters is deemed a necessary but relatively cheap additional step to take advantage of the acceleration potential of the proposed architecture.

6. FEASIBILITY

Up until this point, the paper refrained from elaborating on a specific architecture for the embedded FPGAs, as well as the movement of the bitstreams. This abstraction is done to enable discussions on the novel computer architecture through system effects. However, it is also important to comment on the readiness of current technologies to support such fast reconfiguration times in future SoCs.

6.1 Reconfiguration latency representativeness

The 50-cycle emulated latency used as an example in sections 5.2 and 5.3 yielded a rather desirable single-program and multi-program system performance behaviour. In order to demonstrate that future CPUs which feature FPGAs as functional units can be reprogrammed under a latency of this order of magnitude, we present an example fast-reconfigurable FPGA architecture and prototype it in simulation.

The modelled FPGA is based on a traditional FPGA fabric layout but directly exposes a wide configuration bus which can be loaded from a wide bitstream cache. In contrast, typical FPGA architectures such as the Xilinx UltraScale+ constrain the reconfiguration port to 32 bits wide [22].

The test designs for the FPGA were based on the RISC-V Bit Manipulation extension [2], including clmul (carry-less multiply) and bextdep (bit extract and deposition). This is a real-world example for a useful custom instruction with applications in cryptography (still in draft phase for RISC-V, but related instructions have already been introduced in Intel CPUs [24]).

A series of optimisations are applied to the architecture to minimise configuration array size (and hence cache size and configuration port width) and reconfiguration latency. The first optimisation relates to the removal of features less likely to be useful for this application, such as block RAM (BRAM) for storing large states (section 8 comments on states in instructions).

Another optimisation relates to the type of the look-up tables (LUTs), which are basic building blocks in FPGAs. 4-LUTs (i.e. with 4 inputs totalling 16 entries) are used rather than 6-LUTs. In this way the size of the configuration information is reduced; full instead of one-hot muxes is used for the routing; and the number of routing resources is generally minimised whilst keeping target designs routable. LUT permutation and route-throughs in place and route were used to partially compensate for the latter.

An architectural change required compared to a typical FPGA architecture is to keep the entire configuration data path equal to the number of bitlines, rather than narrowing to an 8-bit or 32-bit external port or memory mapped configuration interface. This can then be loaded at full rate, in the target number of cycles, directly from the bitstream cache.

FPGAs generally use static RAM (SRAM) cells to store the configuration bits; and a word/bit line architecture to configure them. Architectures typically have a similar number of word and bitlines to ease routing. However, this would generally lead to unacceptably high configuration latencies for this application. Reducing the configuration latency requires more bitlines and fewer wordlines - the number of wordlines being equal to the latency, all things being equal. A diagrammatic example of the implication of increasing wordlines to reduce latency, simplified to far fewer tiles and word/bitlines (only 4 configuration bits per tile shown, rather than a typical value of about 1000) than a real FPGA, is shown in figure 8.

Figure 8: Modification of SRAM-based FPGAs for a wide configuration

As physical implementation is not targeted at this stage, this prototype uses a chain of shift registers to store the configuration bits. A configuration word being shifted through the chain each configuration cycle (i.e. the chain is 50 deep and 1824 wide). This is done for the sake of simplicity but has not proven a bottleneck for the routability of the test case.
The FPGA is modelled inside nextpnr [34], using the viaduct plugin framework for architectures, with a Verilog simulation model to confirm that bitstreams can be loaded in the target latency and function correctly. There are two connections between the FPGA fabric and the CPU. A wide configuration bus based on the Pico Co-Processor Interface (PCPI) from PicoRV32 [40] is loaded through an L1 cache. Once the FPGA is configured, the fabric itself can also receive instruction operands and source register values; and returns a destination value after some cycles. The PCPI interface also enables the FPGA fabric to implement partial instruction decoding; so one bitstream could implement multiple related instructions.

![Figure 9: LUT type versus bitstream size and width](image)

The benefit of 4-LUTs in this context is shown with an experiment that determines the minimum configuration FPGA array size necessary to implement the bextdep benchmark. Note that a technique called fracturable LUTs could make the 6-LUT case more efficient by allowing multiple two smaller LUTs (with some shared inputs) to be placed onto one 6-LUT location [27]. Still, the tighter packing could have worsened routability, since the test exhibited competitiveness in its use of routing resources. However, this is beyond the scope of this simple framework that minimises the total number of LUT sites used in this test.

When configured for 1680 LUTs, the bitstreams are a total of 91 kbits, requiring a 1824-bit wide configuration port for 50-cycle reconfiguration latency. This is within the reasonable range of wide datapaths inside modern systems, and it could be reduced at the expense of latency. Even the 250-cycle latency showed benefits in some applications and would require only a 365-bit-wide port. See section 6.2 for a thorougher discussion on the cache organisation.

In practice, the architecture can also be extended with hard multiplier/DSP blocks to enable efficient acceleration of mathematical instructions. This would further reduce the number of configuration bits by avoiding the use of fabric resources for multiplies.

### 6.2 Bitstream cache dimensions

To better understand the bitstream cache requirements for high-end processors, a separate study is conducted on a commercial x86 platform with a higher instruction variety (such as with vector instructions). By using dynamic binary instrumentation (DBI), this section explores the spatial needs and temporal localities with respect to the bitstream usage by comparing it to the traditional instruction and memory usage.

This is done to ensure that an adequately-sized bitstream cache can fit alongside the other caches in a modern CPU, as well as to understand the overall cache organisation (including the number of levels) that would be most efficient.

In contrast, the evaluation on system performance (section 5) assumed that there are no misses in the L1 bitstream cache, but this related more directly to the RISC-V case with the modular extensions. In particular, the total number of bitstreams were considered to fit and pre-exist inside the bitstream cache, such as with the 10 instruction groups of the preferred scenario 2. By using an ideal bitstream cache of at least 10 slots, these would only be compulsory misses (only on first access), hence their dismissal in simulation for brevity. Still, the existence of a bitstream cache was assumed.

The study of cache requirements would normally involve measuring the cache working set by simulating caches of different sizes and levels and pinpointing the size where the miss rate declines sharply. However, could use assumptions relating to data and instructions, such as about the longevity of the working set (benefiting from multiple cache levels) and the access pattern (the notion of working set implies certain access distributions in space and time).

Through a custom Intel Pin [26] tool, on every dynamic instruction call, a routine updates a series of data structures for statistics on the opcodes, instruction pointers (IPs) and memory locations (where applicable). Each opcode is perceived as a separate bitstream. This represents the worst case to avoid specialisation in the observations, since it also includes control flow and data movement instructions, which are expected to be the most frequent [6, 13], as well as for similar instructions that could be grouped together (see section 4.3).

With regards to the memory and instruction addresses, a mask is applied to ignore the last 6 bits for a 64-byte-granularity in the cache blocks, which is commonly found in today’s x86 systems, including the target processor.

The data structures inside the Pin tool are mainly hash-sets that provide the number of unique opcodes, instruction and data blocks. On every n number of instructions, where n ∈ {2^6, 2^7, ..., 2^18}, the 3 corresponding sets are cleared and their cardinality is saved in lists (implemented as maps of _<cardinality, occurrence>_ pairs to conserve memory). This provides the distribution of compulsory miss cardinalities occurring in the specified periods of time (measured in instructions) for each of the opcode, instruction and memory cache blocks. For the instructions and data, the algorithm’s input would represent the stream observed right before the L1 instruction and L1 data caches. Though, the spatiotemporal locality scope of this experiment extends beyond the L1 caches. For the opcodes, since the bitstream disambiguator works as a L0 cache, this stream is considered to be observed from L0, when following the proposal specification.

The benchmark suite selection for the single-program experiment is the single-core part of Geekbench 5. Geekbench 5 runs a series of 21 compute-intensive benchmarks ranging

---

4AMD Ryzen 7 Pro 4750U, though other than the line size, as with other Pin tools the collected dataset is mostly microarchitecture-independent.
Figure 10: Compulsory misses cardinality for different time window sizes

Figure 11: Reuse behaviour in multi-programming

from encryption to machine learning one by one. Here, the same instance of the Intel Pin tool is used for the entirety of all Geekbench benchmarks.

These results are illustrated in figure 10. The x axes summarise the time period the hashsets are collecting information for, and are used to observe temporal locality. The y axes are the observed median cardinalities for each hashset, and represent the compulsory misses for each type of cache block (bitstream for opcode, instruction for IPs and data for data addresses). The shaded regions underneath the 3 series show the lower and upper quartiles of the cardinalities in each corresponding lists of hashsets. As can be seen, the opcode count starts from below 16 for the shorter time slices, while peaking at below 64 for the longer time slices.

Another observation is that the opcode series is "flatter" than the other curves, meaning that there is higher reuse of opcodes than instruction and memory blocks. It is also longer lasting. This could have been conjectured, but the relationship between the 3 types of reuse is a result of multiple factors. For instance, each instruction and data block already covers multiple locations (64-byte granularity), whose reuse also depends on the memory access pattern. From the opcode’s perspective, CISC ISAs like x86-64 include a rather high number, as with Intel Pin’s catalog of over 8000 entries.

The fact that the instruction and data series have a steeper upwards slope can also justify the need for multi-level cache hierarchies. This is because the cache size requirements are shown to grow gradually with time and a greater working set would be benefited from nearer caches of larger size. Of course this experiment does not discuss the amount of reuse such as through the distribution of accesses of the unique blocks, but the compulsory misses already represent the worst case for the space requirements.

After also comparing the behaviour from benchmarks in the processor category from the Phoronix Test Suite (not shown), the Geekbench behaviour was fairly typical especially with regards to the opcode behaviour. Some benchmarks exhibited more variety in the instruction and data reuse, such as with the botan encryption benchmark who accessed more instruction than data blocks, though the opcode behaviour was more consistent.

With respect to the multi-program behaviour, the same Pin tool (but with added thread safety mechanisms) is used on the adapted Embench suite for the FreeRTOS/RISC-V experiment of section 5.3. This time each benchmark is run as a thread using pthreads in Linux/x86_64 and is pinned down to the same core for oversubscription. The benchmark suite is compiled as a single binary, and with the -march=native flag to promote vectorisation. Although the benchmarks are synthetic, the idea of oversubscription here is to attempt increasing opcode demand, similar to the operating system’s frequent migration of hundreds of tasks in multi-core systems.

The results of the multi-program experiments are shown in figure 11, where the median compulsory misses are measured for different amounts of task oversubscription to a single core. The time window size is fixed at 32768 instructions. Superimposed to the scatter plot of medians are violin plots, which are used to visually provide more detailed distribution information than medians and percentiles. The data block behaviour was fairly similar to the data blocks in this instance, hence its omission for readability. As expected, there is higher reuse of opcodes than instructions among the different tasks when oversubscribed. For example, when all 22 tasks are run simultaneously, the median and maximum opcode miss count reaches 59 and 152 respectively, while the median and maximum for instructions are 119 and 672 respectively.

These numbers show that the bitstream cache is feasible with today’s technology on SoCs. Specifically, a 64-block bitstream cache is shown to be enough for relatively long periods of time in both the single-program and multi-program experiments. This totals 768 KB of SRAM when using 12 KB bitstreams, being inline with the example FPGA architecture of section 6.1. By observing recent processor trends that feature, for example, up to 256 MB L3 caches [35], the sub-MB size requirement is in the L2 territory. Additionally, a sub
2048-bit datapath that is demonstrated in section 6.1 is only needed between this cache and the instruction disambiguator, as the expected latency profile of the bitstream cache makes progressively-loaded bitstream blocks meaningful, even with 128/256-bit datapaths to L2. Although this study ignores conflict behaviour for generality, a 64-block cache is rather easy to feature high-amounts of associativity today, such as with the 8-way L1 caches [35]. The “flatter” curve of the opcode cardinality also indicates the possibility of benefiting from a flatter cache hierarchy than the conventional 3 or 4-level. Given the oversubscription experiment results and the read-only nature of the bitstreams from the FPGA’s view, future multicores could also benefit from sharing of the bitstream cache(s).

This conclusion is drawn also with the worst case approach in mind, such as by associating compulsory miss cardinality with the desirable cache size, and by not classifying opcodes into groups. Therefore, a fraction of the reported desirable bitstream cache would most likely still be beneficial in future high-end CPUs with FPGAs working as instructions.

7. RELATED WORK

The literature on FPGAs implementing CPU instructions could be considered rather thorough, and provided important insights that inspired this paper. Though, being based on a more practical approach and existing technologies, the related research inherited most of the challenges of section 2. The major difference of our approach to the related work is that it avoids specialisation and optimisation to propose a general purpose computer architecture. This enabled addressing advanced features found in modern computers, such multiprocessing, but in the context of reconfigurable instructions.

With respect to the acceleration of instructions, Soft-NEON [28] is an FPGA implementation of a custom vector extension for the Xilinx Zynq embedded platform that demonstrated a speedup of over 2.8 times for some custom kernels. It is mostly limited by the platform limitations related to the communication between the ARM cores and the FPGA. A relatively similar approach coupled a shared SIMD engine between multiple RISC-V cores [29]. This leveraged Xilinx’ partial reconfiguration to accelerate custom kernels on an embedded FPGA. The general focus is on the implementation and there are no insights on generalising the approach to the extent of our proposal.

There are also works focusing on embedded FPGA (eFPGA) fabrication. FABulous [25] is an open-source framework for integrating FPGAs into anASIC. One of its applications is for the implementation of eFPGAs, also for the purposes of extending hardened cores. A RISC-V SoC with eFPGAs is presented as a use case, which is extended as a separate study with FlexBex [16]. The custom instruction usage is limited to specialised kernels, and concepts like context-switching are not studied.

Earlier research also focused on using FPGAs as a functional unit. Garp [21] targets embedded processors without multi-processing support, but it introduces the idea of combining a bitstream alongside the process binary. It does not make FPGAs transparent, as it requires configuration instructions. DISC [39] is an earlier work that elaborates on reconfiguration in a similar context. Its instruction decoder is similar to the proposed instruction disambiguator in the sense that it uses a caching approach. It is not a general-purpose computer architecture, as the processor has a separate ISA from the host processor. On a similar note, Chimamera [42] provides a reconfigurable array to dynamically load FPGA-based instruction implementations. This is somewhat reminiscent of the proposed bitstream cache, but does not support context-switching and also focuses on custom instructions for software compiled with a specialised compiler. Later, architectures like CCA [14] and RISPP [10] aimed to improve the adaptability of embedded systems by providing a set of specialised functional units that can be dynamically selected at run-time. The latter does not involve FPGAs but it is similar in the reconfiguration granularity of instructions.

There are also softcores that enable easy modification with custom (fixed) instructions. For example, Simodense [32] is a RISC-V softcore that supports custom SIMD instructions of custom pipeline lengths. Although this framework is targeted for exploring FPGAs as instructions [30], it does not elaborate on system architecture. Applications run bare metal and assume FPGA configuration beforehand for the sake of instruction exploration. Such studies also use custom instructions which are relatively complex, whereas our focus includes simpler instructions, such as those found in RISC-V extensions [3] for also targeting CPU core miniaturisation.

8. FUTURE WORK

An interesting next step could be to introduce internal states in FPGA-based instructions. They are not necessary in the proposal, but they may be used for reaching more easily an accelerator-level of performance in CPUs. This is because “internalising” computation could be seen as one of main techniques FPGAs use to outperform CPUs in specific areas. Their existence would impact context-switching, programming models and hardware-based prediction mechanisms.

An alternative computer architecture could involve context-switching as a facility to swap the entire FPGA’s contents, which is similar to context-switching for partial reconfiguration [36]. Our solution prevents unnecessary reconfiguration of common logic. Using a customised context-switching routine to swap all reconfigurable units would be unnecessarily expensive for general purpose. However, if this is restricted to highly customised instructions it can still be meaningful to consider for managing internal states.

From the software’s perspective, should this architecture be adopted in production systems, it would be appropriate to standardise the definition of processes [21] to include instruction extension implementations (or dynamic linking) in their binaries.

The proof-of-concept FPGA architecture was optimised for low configuration latency. The operating frequency of small reconfigurable areas is an appropriate secondary optimisation parameter that does not seem prohibitive at the moment. This is because modern process nodes are reported to run small instruction-like FPGA designs in the GHz range [4, 19], and high-end processors already feature multiple-cycle instructions [23].

To further reduce the configuration latency, the FPGA
architecture could also be designed such that partial bitstream loads are supported. For instance, if an instruction only requires half of the FPGA fabric, then place-and-route and the bitstream could be constrained to half of the device.

9. CONCLUSIONS

The FPGA-extended modified Harvard architecture can be used to transparently fetch standardised ISA extensions or custom instructions through the computer’s memory hierarchy. The disambiguator unit works as an L0 cache for the instruction slots and requests and multiplexes the bitstreams and instructions to reconfigurable regions. The evaluation showed promising results, surpassing the performance of a core with a single fixed extension when the total reconfiguration latency is adequately low. The operating system in such computers is more likely to benefit from longer times between context-switches to compensate for the reconfiguration time. Finally, a low reconfiguration latency is deemed necessary for the efficiency of the proposal, and our feasibility study finds this to be possible by mainly using existing FPGA building blocks and a cache with appropriate dimensions for providing the bitstreams.

ACKNOWLEDGMENTS

The feedback of Anuj Vaishnav on an earlier version is gratefully acknowledged.

REFERENCES

[1] “RISC-V ‘V’ Vector Extension, Version 0.9,” 2020.
[2] “RISC-V ‘B’ Bitmanip Extension, Version 0.94-draft,” 2021.
[3] A. Waterman and K. Asanovic, “The RISC-V instruction set manual, volume I: Unprivileged ISA document, version 20191214-draft,” RISC-V Foundation, Tech. Rep., 2020.
[4] Achronix Semiconductor Corporation, “Speedcore architecture (accessed on 10/04/2022).” [Online]. Available: https://www.achronix.com/speedcore-architecture
[5] S. Z. Ahmed, “eFPGAs: Architectural explorations, system integration & a visionary industrial survey of programmable technologies,” Ph.D. dissertation, Université Montpellier II-Sciences et Techniques du Languedoc, 2011.
[6] A. Akshintala, B. Jain, C.-C. Tsai, M. Ferdman, and D. E. Porter, “X86-64 instruction usage among c/c++ applications,” in Proceedings of the 12th ACM International Conference on Systems and Storage, 2019, pp. 68–79.
[7] G. Alonso, Z. Istvan, K. Kara, M. Owaida, and D. Sidler, “doppiodb 1.0: Machine learning inside a relational engine.” IEEE Data Eng. Bull., vol. 42, no. 2, pp. 19–31, 2019.
[8] R. Barry, FreeRTOS reference manual: API functions and configuration options. Real Time Engineers Limited, 2009.
[9] R. Barry et al., “Freertos,” Internet, Oct, 2008.
[10] L. Bauke, M. Shafique, and J. Henkel, “Rispp: A run-time adaptive reconfigurable embedded processor,” in 2009 International Conference on Field Programmable Logic and Applications. IEEE, 2009, pp. 725–726.
[11] R. Bordawekar, U. Bondhugula, and R. Rao, “Can cpus match gpus on performance with productivity?: Experiences with optimizing a flop-intensive application on cpus and gpus.” IBM Research Report, RC25033, Tech. Rep., 2010.
[12] J. M. Cebrian, L. Natvig, and M. Jähre, “Scalability analysis of avx-512 extensions,” The Journal of supercomputing, vol. 76, no. 3, pp. 2082–2097, 2020.
[13] Y.-J. Chang, “Exploiting frequent opcode locality for power efficient instruction cache,” in Proceedings of the 18th ACM Great Lakes symposium on VLSI, 2008, pp. 399–402.
[14] N. Clark, J. Blome, M. Chu, S. Mahlke, S. Biles, and K. Flautner, “An architecture framework for transparent instruction set customization in embedded processors,” in 32nd International Symposium on Computer Architecture (ISCA’05). IEEE, 2005, pp. 272–283.
[15] I. corp, “Intel 64 and ia-32 architectures software developer’s manual volume 2: Instruction set reference,” 2021.
[16] N. Dao, A. Attwood, B. Healy, and D. Koch, “FlexBex: A RISC-V with a Reconfigurable Instruction Extension,” 12 2020.
[17] J. Fang, Y. T. Mulder, J. Hidders, J. Lee, and H. P. Høftstee, “In-memory database acceleration on FPGAs: a survey,” The VLDB Journal, vol. 29, no. 1, pp. 33–59, 2020.
[18] M. Gottschlag, T. Schmidt, and F. Bellosa, “Avx overhead profiling: How much does your fast code slow you down?” in Proceedings of the 11th ACM SIGOPS Asia-Pacific Workshop on Systems, ser. APSys ‘20. ACM, 2020, p. 59–66.
[19] D. Greenhill, R. Ho, D. Lewis, H. Schmit, K. H. Chan, A. Tong, S. Aissat, D. How, P. McElhenny, K. Duwel, J. Schulz, D. Faulkner, G. Iyer, G. Chen, H. K. Phoon, H. W. Lim, W.-Y. Koay, and T. Garibay, “3.3 a 14nm 1 ghz fpga with 2.5d transceiver integration,” in 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 54–55.
[20] J. H. Grosbach, J. M. Conner, and M. Catherwood, “Modified harvard architecture processor having program memory space mapped to data memory space,” Apr. 27 2004, US Patent 6,728,856.
[21] J. R. Hauser and J. Wawrzynek, “Garp: A mips processor with a reconfigurable coprocessor,” in Proceedings. The 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines Cat. No. 97TB100186). IEEE, 1997, pp. 12–21.
[22] X. Inc., “Vivado Design Suite User Guide, Partial Reconfiguration - UG909 (v2018.1),” 2018.
[23] Intel (R), “Intel intrinsics guide.” [Online]. Available: https://software.intel.com/sites/landingpage/IntrinsicsGuide/
[24] Intel (R), “Intel (r) carry-less multiplication instruction and its usage in iavx-512 extensions,” in Intel (R), “Intel (r) carry-less multiplication instruction and its usage in X86-64 instruction usage among c/c++ applications,” in Proceedings of the 11th ACM SIGOPS Asia-Pacific Workshop on Systems, ser. APSys ‘20. ACM, 2020, p. 59–66.
[25] D. Koch, N. Dao, B. Healy, and J. Yu, and A. Attwood, “Fabulous: an embedded fpga framework,” in The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2021, pp. 45–56.
[26] C.-K. Luk, R. Cohn, R. Muth, H. Pattil, A. Klauser, G. Lowney, S. Wallace, V. J. Reddi, and K. Hazelwood, “Pin: building customized program analysis tools with dynamic instrumentation,” ACM sigplan notices, vol. 40, no. 6, pp. 190–200, 2005.
[27] J. Luu, J. H. Anderson, and J. S. Rose, “Architecture description and packing for logic blocks with hierarchy, modes and complex interconnect,” in Proceedings of the 19th ACM/SIGDA international symposium on Field programmable gate arrays, 2011, pp. 227–236.
[28] J. R. G. Ordaz and D. Koch, “soft-NEON: A study on replacing the NEON engine of an ARM SoC with a reconfigurable fabric,” in 2016 IEEE 27th International Conference on Application-specific Systems, Architectures and Processors (ASAP). IEEE, 2016, pp. 229–230.
[29] Ordaz, Jose Raul Garcia and Koch, Dirk, “A Soft Dual-Processor System with a Partially Run-Time Reconfigurable Shared 128-Bit SIMD Engine,” in 2018 IEEE 29th International Conference on Application-specific Systems, Architectures and Processors (ASAP). IEEE, 2018, pp. 1–8.
[30] P. Papaphilippou, P. H. J. Kelly, and W. Luk, “Demonstrating custom SIMD instruction development for a RISC-V softcore,” in 2021 31st International Conference on Field-Programmable Logic and Applications (FPL), Aug 2021, pp. 139–139.
[31] P. Papaphilippou and W. Luk, “Accelerating database systems using FPGAs: A survey,” in 2020 28th International Conference on Field Programmable Logic and Applications (FPL). IEEE, 2018, pp. 125–130.
[32] P. Papaphilippou, K. Paul H. J., and W. Luk, “Simodense: a risc-v softcore optimised for exploring custom simd instructions,” in 2021
[33] D. Patterson, J. Bennett, P. Dabbelt, C. Garlati, G. Madhusudan, and T. Mudge, “Embench: A modern embedded benchmark suite,” 2020.

[34] D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist, and M. Milanovic, “Yosys+nextpnr: An open source framework from verilog to bitstream for commercial fpgas,” in 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2019.

[35] D. Suggs, M. Subramony, and D. Bouvier, “The amd “zen 2” processor,” IEEE Micro, vol. 40, no. 2, pp. 45–52, 2020.

[36] A. Vaishnav, K. D. Pham, J. Powell, and D. Koch, “Fos: A modular fpga operating system for dynamic workloads,” ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol. 13, no. 4, pp. 1–28, 2020.

[37] Y. E. Wang, G.-Y. Wei, and D. Brooks, “Benchmarking TPU, GPU, and CPU platforms for deep learning,” arXiv preprint arXiv:1907.10701, 2019.

[38] A. Waterman and K. Asanovic, “The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, v1. 12,” 2019.

[39] M. J. Wirthlin and B. L. Hutchings, “Disc: The dynamic instruction set computer,” in Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing, vol. 2607. SPIE, 1995, pp. 92–103.

[40] C. Wolf, “PicoRV32-a size-optimized RISC-V CPU,” 2019.

[41] I. Yasui and Y. Shimazu, “Microprocessor with harvard architecture,” Jul. 23 1991, US Patent 5,034,887.

[42] Z. A. Ye, A. Moshovos, S. Hauck, and P. Banerjee, “Chimaera: A high-performance architecture with a tightly-coupled configurable functional unit,” ACM SIGARCH computer architecture news, vol. 28, no. 2, pp. 225–235, 2000.