Building time-surfaces by exploiting the complex volatility of an ECRAM memristor

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Abstract—Memristors have emerged as a promising technology for efficient neuromorphic architectures owing to their ability to act as programmable synapses, combining processing and memory into a single device. Although they are most commonly used for static encoding of synaptic weights, recent work has begun to investigate the use of their dynamical properties, such as Short Term Plasticity (STP), to integrate events over time in event-based architectures. However, we are still far from completely understanding the range of possible behaviors and how they might be exploited in neuromorphic computation. This work focuses on a newly developed Li₂WO₃-based three-terminal memristor that exhibits tunable STP and a conductance response modeled by a double exponential decay. We derive a stochastic model of the device from experimental data and investigate how device stochasticity, STP, and the double exponential decay affect accuracy in a hierarchy of time-surfaces (HOTS) architecture. We found that the device’s stochasticity does not affect accuracy, that STP can reduce the effect of salt and pepper noise in signals from event-based sensors, and that the double exponential decay improves accuracy by integrating temporal information over multiple time scales. Our approach can be generalized to study other memristive devices to build a better understanding of how control over temporal dynamics can enable neuromorphic engineers to fine-tune devices and architectures to fit their problems at hand.

Index Terms—Memristor, analog computing, neuromorphic systems.

I. INTRODUCTION

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THE last decade has brought considerable progress in AI, mainly owing to the advent of Graphics Processing Units (GPUs) and other hardware accelerators. However, this progress has not been matched from the perspective of emulating general intelligence and cognition. Ideas such as deep multilayer learning and backpropagation have helped solve a particular class of well-defined problems but require high energy and vast amounts of labeled data [1], [2]. These requirements drastically limit on-board “intelligence” and reduce autonomy. Thus, essential functionalities such as continuous always-on learning with a reasonable power budget are still out of reach.

Neuromorphic engineering holds the promise of mitigating these restrictions [3], [4]. Recently, this field has reached a level of maturity that allows it to impact several other domains where autonomy and low power on-the-edge computation are crucial. One core principle is to remove the separation of memory and computation, typical of Von Neumann architectures, by taking inspiration from neurons and synapses and more closely integrating computation and memory.

Many researchers have taken an interest in memristive devices, given their ability to implement tunable nonvolatile weights similar to synaptic efficacy in biological synapses. Following this paradigm, memristors have been applied to many network-based computational approaches. Doygu et al. simulated memristor networks able to learn sequences of inputs [5]. Suri et al. used another simulated network of phase-changing memristors to learn MNIST letters [6]. Systems that perform STDP (Spike Time Dependent Plasticity) using RRAM (REsistive RAM) devices [7] or that implement recursive networks using PCM memristors have also been reported [8]. Vincent et al. simulated a network of STT-MRAM devices for car detection [9]. Networks of memristors have also been proposed to implement the k-means algorithm [10] and unsupervised learning [11]. In all of these examples, the synaptic devices modeled using memristors working in a “static” fashion, i.e., as a fixed scalar multiplier of spike events, before integration by the “neuron membrane”. This approach has been widely adopted because of its simplicity of implementation and mathematical tractability, as synaptic operations can be described by simple linear algebra.

In recent years, a different approach has surfaced. Several works have demonstrated the presence of transient conductance responses in memristive devices akin to short-term plasticity (STP) and Excitatory/Inhibitory Post Synaptic Potentials (EPSP/IPSP) [12]-[15]. These memristors with “volatile” properties are extremely promising for implementing neuromorphic networks that need physical devices capable of temporal computation [16]. In these devices, input events (i.e., voltage pulses) cause temporary changes in conductance that exponentially relax back to baseline, like EPSPs and IPSPs in biological synapses. Moreover, the conductance change is potentiated when multiple input events are close in time (STP). These short-term dynamics allow the modeling of temporal kernels and short-term plasticity without the need for additional circuitry. Electrochemical memristors exhibit both STP and EPSPs simultaneously [17], [18]. However, in memristors with oscillatory properties [19]-[21], STP is not present. Moreover, some devices can produce EPSPs with multiple exponential decays, making the range of possible dynamics extremely complex. We are still far from understanding the entire repertoire of short-term dynamics in volatile memristors, let alone being able to exploit them in real, practical scenarios. Many works utilizing the short-term dynamics of memristive devices have demonstrated only simple networks (or even single neurons) operating on limited examples [14]-[16], [22]-[25], or use memristor dynamics for different mimicking neuron operations such as adaptive thresholds.
To the best of our knowledge, the relationship between the different types of dynamics in representing temporal information from spiking data and recognition rates on real-world neuromorphic datasets has not been studied. Understanding this relationship will enable the design of custom neuromorphic systems that make full use of memristive dynamics for efficient computation.

This paper studies the effect of different memristive dynamics on recognition accuracy by complex networks on complex tasks by simulating a neuromorphic architecture based on a LiWES artificial synapse: a three-terminal electrochemical memristor with double exponential decays in the order of ten to hundred milliseconds (required by many neuromorphic datasets) and STP [24]. We build a model of the device response and use it to simulate a network based on the Hierarchy of Time Surfaces (HOTS) architecture [28] for pattern recognition. While these architectures tend to have lower accuracy than SNNs trained with backpropagation, the local unsupervised learning used for feature extraction is well suited for on-chip learning, especially in conjunction with memristive technologies [10].

We evaluate performance on the N-MNIST [29] and POKERDVS [30] datasets. First, we study whether inherent stochasticity in memristive dynamics could negatively impact accuracy. We compare the device model against an ideal noiseless memristor, finding no significant difference in the classification accuracy. Using information theoretic measures, we also study the effect of stochasticity on the mutual information of events propagated by the network and discuss a possible solution to reduce accuracy loss in architectures using dynamics in noisy memristors. Finally, we break down the model to see how different memristive dynamics (multiple-exponential decays and STP) can be used to improve accuracy and performance in HOTS-like neuromorphic architectures.

II. THE Li$_3$WO$_3$ ELECTROCHEMICAL MEMRISTOR

“Volatile” memristors enable efficient implementations of temporal computing, as they combine temporal dynamics and short-term plasticity in a single device. Among these, electrochemical memristors [31] have become good candidates thanks to their low power consumption, linear and symmetric response, low variability, and high reliability [18], [31]–[40]. We have previously proposed the use of a novel electrochemical memristor [24] based on Lithium Ions and Tungsten Oxide (Li$_3$WO$_3$), which has the advantages of low programming voltage (0.2 V), fast programming speed (500 ns), and high precision (1024 states corresponding to 1024 10ms 0.5V “write” pulses before reaching saturation), wide conductance range (≈ 1µs to ≈ 200µs), with a channel area of 400x200µm$^2$. These devices have been used to model synapses and to implement electrochemical random access memory (ECRAM) [41]. They are especially suitable for neuromorphic networks because they can model synaptic dynamics and short-term plasticity (STP) with time constants ranging from a few to hundreds of milliseconds. We focus on a version of Li$_3$WO$_3$ memristor that uses a self-gate design in which transitory effects dominate long-term effects [36].

This structure of the Li$_3$WO$_3$ memristor is illustrated in Fig. 1(a). Unlike conventional two-terminal memristors, the Li$_3$WO$_3$ electrochemical is composed of three terminals, the (S)ource, (D)rain and (G)ate. The memristor is built by deposition of tungsten oxide (WO$_3$) films on a LaALO$_3$ substrate. Lithium ions introduced via an electrolyte gel can flow between the gate and channel. When embedded into the tungsten oxide films, they act as short or long-term doping charges, changing the film conductance [24]. The conductance between the source and the drain terminal, $G_{DS}$, is considered to be the synaptic weight of the device.

![Fig. 1. The structure and operation of the physical Li$_3$WO$_3$ electrochemical synapse modelled in this paper. (a) The Li$_3$WO$_3$ electrochemical synapse is a three-terminal device with a (S)ource, (G)ate and (D)rain. The gate and channel between S and D are built by deposition of tungsten oxide (WO$_3$) films on a LaALO$_3$ substrate (green). The films are connected to gold terminals (yellow). Lithium (Li$^+$) and ClO$_4^-$ ions are introduced by applying a drop of electrolyte gel (blue) on top of the device. (b) The electrical behavior of the memristor in response to a square WRITE voltage pulse applied between (G) and (D) and a small DC READ voltage (0.1 V) applied between (S) and (D). (c) The electrochemical behavior of the memristor.](image-url)
field, which causes Li+ ions to accumulate at the channel/electrolyte interface and charge-balancing ClO4− ions to accumulate at the gate. Doping of the channel by the Li+ ions increases the channel conductance. During the relaxation phase, after the removal of the write pulse, the ions return to equilibrium and the channel conductance returns to its resting value. The double exponential decay response can be explained by the Kohlrausch-Williams-Watts (KWW) relaxation model \cite{[22], [33]}, which has also been found in other electrochemical devices \cite{[18]}.

Changing the material properties enables “programming” the exponential decays in the range of tens to hundreds of milliseconds, which is optimal for temporal integration of events for many real-world datasets \cite{[28], [44]}. Due to the high number of pulses required to reach saturation over, the high number of pulses required to reach saturation term plasticity (STP) similar to biological neurons. Moreover, the high number of pulses required to reach saturation (1024) make it more than capable to work on the proposed datasets, where the maximum number of events per pixel is 48, corresponding to a max of 48 “write” pulses per single synapse/device. Together, these properties make this device an excellent candidate for studying the computational benefits of memristors’ dynamics for neuromorphic time based learning applications.

A. Mathematical model of synaptic dynamics

Following \cite{[18], [24], [36], [42], [43]}, we develop a mathematical model to predict the electrical behavior of the Li+WO3 memristor by first modelling its response to a single square pulse, then combining the responses.

Given a spike train with spike times \(\{t_i\}\) indexed by \(i \in \{0, 1, 2, \ldots\}\), the conductance response is given by

\[
G(t) = \sum_i (G_{1,i}(t) + G_{2,i}(t)) + \eta(t)
\]

where \(G_{1,i}(t) + G_{2,i}(t)\) is the memristor’s response to all spikes up to and including the \(i\)th spike for times \(t \in (t_i, t_{i+1}]\), and \(\eta(t)\) is zero-mean Gaussian white noise with variance \(\sigma^2\).

To model the double exponential decay, we express the response as the sum of two components, \(G_{k,i}(t)\) for \(k \in \{1, 2\}\), each modelling a single exponential response.

We define the components \(G_{k,i}(t)\) recursively:

\[
G_{k,i}(t) = \begin{cases} 
L_{k,i}(t) & \text{for } t_i < t \leq \min(t_i + w, t_{i+1}) \\
E_{k,i}(t) & \text{for } t_i + w < t \leq t_{i+1} \\
0 & \text{otherwise}
\end{cases}
\]

where \(w > 0\) is the width of the write pulse. \(L_{k,i}(t)\) models the linear rise in conductance starting from \(G_{k,i-1}(t_i)\) to \(G_{k,i-1}(t_i) + A_{k,i}\), where \(A_{k,i}\) is the peak conductance change due to the \(i\)th write pulse.

\[
L_{k,i}(t) = G_{k,i-1}(t_i) + A_{k,i} \left( \frac{t - t_i}{w} \right)
\]

\[
E_{k,i}(t) = (G_{k,i-1}(t_i) + A_{k,i}) e^{-\left( \frac{t - t_i - w}{\tau_{k,i}} \right)}
\]

Fig. 2 shows our model for a given pulse width \(w\) at time \(t_i\).

We can see from (2), (3) and (4) that \(G_{k,i}(t)\) depends on the conductance at the start of the \(i\)th pulse, \(G_{k,i-1}(t_i)\). This models STP, where past pulses all contribute to the current device conductance. To model the hypothetical memristor without STP in section IV C, we remove \(G_{k,i}(t)\) from (3) and (4)

\[
L_{k,i}(t) = A_{k,i} \left( \frac{t - t_i}{w} \right)
\]

\[
E_{k,i}(t) = A_{k,i} e^{-\left( \frac{t - t_i - w}{\tau_{k,i}} \right)}
\]

so that every new pulse resets the peak conductance to \(A_{k,i}\), rewriting any conductance value from previous pulses.

As we are also interested in studying the effect of device stochasticity on computation, we consider two models: an ideal model and a stochastic model.

In the ideal model, the peak conductance changes and time constants are the same for all pulses, i.e., \(A_{k,i} = A_k\) and \(\tau_{k,i} = \tau_k\) for \(k \in \{1, 2\}\), where \(A_k\) and \(\tau_k\) are positive constants. The noise is zero (\(\eta(t) = 0\)).

In the stochastic model, the \(A_{k,i}\) and \(\tau_{k,i}\) are drawn from an independent and identically distributed discrete time (i.i.d.) random process in \(i\), where each sample is drawn from a Gaussian distribution,

\[
A_{k,i} \sim N(\bar{A}_k, \sigma^2_{A_k}).
\]

\[
\tau_{k,i} \sim N(\bar{\tau}_k, \sigma^2_{\tau_k}).
\]

where negative samples are rectified.

The dynamics of the LiWES can be tuned by changing the write pulse properties, such as pulse width and amplitude \cite{[24]}. To replicate the device behavior for a given pulse, we need to obtain the mean and standard deviation of the model parameters (\(A_1, A_2, \tau_1, \tau_2\)). We first compute the rest conductance by averaging the conductance before pulse onset and subtracting this from the data. We then combine (1) and (2) to compute the response, which we split into two parts:

\[
G_{\text{rise}}(t) = (A_1 + A_2) \left( \frac{t - t_0}{w} \right) \text{ for } t_0 < t \leq t_0 + w
\]

\[
G_{\text{decay}}(t) = A_1 e^{-\left( \frac{t - t_0 - w}{\tau_1} \right)} + A_2 e^{-\left( \frac{t - t_0 - w}{\tau_2} \right)} \text{ for } t_0 + w < t
\]

We fit the model parameters (\(A_1, A_2, \tau_1, \tau_2\)) using the least squares fit between the experimental data after the write pulse (\(t > t_0 + w\)) and \(G_{\text{decay}}(t)\) using the Gauss-Newton algorithm. We use the model and fitted parameters to predict the responses for \(t \leq t_0 + w\).

To find the parameters of the stochastic model, we repeated the model fit using data from multiple recordings of pulses with different pulse amplitudes (ranging from 1V to 4V) and durations (ranging from 200\(\mu\)s to 1 ms). Based on these fits, we calculated the distributions of the model parameters. We report the fitting results in Table I and Table II. The tables show the mean and standard deviations of the parameter estimates fitted over 20 recordings for the 200us 1V pulse and 5 recordings for the remaining conditions. The variance of the
noise $\sigma_\eta$ was set to the mean square error of the fit. For details, refer to the supplementary materials.

We can use equations (1)-(8) and the distributions specified in Tables I and II to simulate the response of any number of devices to any set of spike trains. Figure 3 compares the output of our stochastic model with the response of an actual device to the same spike train. Note that due to the stochasticity, we do not expect spike-to-spike matching of the responses. Rather, the statistics and timing of the responses will be similar.

III. MEMRISTOR IMPLEMENTATION OF HOT S

The Hierarchy of Event-Based Time-Surfaces (HOTS) architecture is a neuromorphic architecture for unsupervised pattern recognition [28]. HOTS networks are highly versatile and can be applied to the output of neuromorphic sensors for different modalities [28], [45]–[47]. Moreover, HOTS neurons are more mathematically tractable than other Spiking Neural Network (SNN) models. This feature makes it easier to isolate the effects of memristive dynamics on network behavior using the analysis we describe in the next section.

A HOTS network maps each input spike to an output spike from one of the neurons in the network. HOTS networks draw inspiration from clustering. Each neuron in a HOTS network represents a cluster corresponding to a pattern of events within a spatial window. The diversity of possible input patterns is reflected by the diversity of patterns represented by the neurons in the network. In order to represent event patterns as points to cluster, HOTS introduces the concept of the Time-Surface. Every time a neuron produces an event, it triggers the creation of a Time-Surface, an array representing the time history of events at that and neighboring neurons.

This section describes a model of a HOTS implementation that exploits the dynamics of Li$_2$WO$_3$ memristors to create the time surfaces. The process of creating time surfaces is shown in Fig. 4, where we assume input comes from an event-based vision sensor and the task is digit recognition. Input images (a) are captured by the event-based sensor (b), which emit trains of events at each pixel in response to brightness changes (c) [28].

Each event $i$ from an event-based vision sensor can be described by the tuple:

$$ev_i = (x_i, y_i, p_i, t_i)$$  \hspace{1cm} (11)

where $x_i$ and $y_i$ are the pixel positions, $p_i$ is the polarity (the direction of brightness change in the pixel), and $t_i$ is the timestamp.

In the original version of HOTS, every incoming event gives rise to an instantaneous rise exponential decay kernel with no memory. In our model, incoming events give rise to double exponential decays with STP. We assign a LiWES memristor to each spatial location and polarity $(x, y, p)$, and using the events at $(x, y, p)$ to generate WRITE signals to that memristor, which generate changes in its conductance $G_{x,y,p}(t)$ following the model described in Section II-A. For each event $ev_i$, we create a time surface by sampling the conductance at all memristors within a square spatial window of lateral size $l$ around $(x_i, y_i)$, i.e.

$$S_i(m, n, p) = G_{x_i+m,y_i+n,p}(t_i)$$  \hspace{1cm} (12)
for $m, n \in \{-l/2, \ldots, (l - 1)/2\}$ and for all polarities $p$, where the subscripts indicate the memristor’s location and polarity.

We use an unsupervised clustering method, such as the K-means algorithm, to cluster the time surfaces. The clusters capture recurring spatio-temporal features of the input data. Each input event generates an output event at the same location and time, but whose polarity is given by the closest cluster. Thus, the number of possible polarities of output events is equal to the number of clusters.

We can define a multiple layer architecture by defining each layer $k$ as a single iteration of this process. Its input events are

$$ev^k_i = (x^k_i, y^k_i, p^k_i, t^k_i)$$

Its output events are:

$$ev^{k+1}_i = (x^{k+1}_i, y^{k+1}_i, p^{k+1}_i, t^{k+1}_i)$$

where superscripts index the layer number, $x^{k+1}_i = x^k_i$, $y^{k+1}_i = y^k_i$ and $t^{k+1}_i = t^k_i$. The output events of one layer become the input to the next. However, to increase spatial integration from layer to layer, we often sub-sample the output events of one layer before inputting them to the next layer.

Fig. 4(g)-(m) shows an example of a two-layer architecture. In (g), we plot the most recent input events before a reference event $ev^1_i$. We sample the memristor conductances in the square neighborhood around $(x^1_i, y^1_i)$ (shown as the red square) to produce a Time-Surface $S^1_i$ (h), only one polarity shown. This Time-Surface gets assigned to a cluster of Layer 1 (i), producing a new output event $ev^2_i$ with a new polarity $p^2_p$ (j). Due to sub-sampling, time surfaces in layer 2 usually correspond to larger effective neighborhoods in layer 1. The entire process can be repeated, as shown in Fig. 4(k,l,m), until we achieve a desired amount of temporal and spatial integration.

Similarly to [28], we create a feature vector for each spike activity recording by building a histogram $H$ of the polarities of spikes from the last layer collected across all pixels and over the entire recording.

We classify the feature vector using a polynomial Support Vector Classifier (SVC). In our comparative experiments seeking to elucidating the effect of different facets of the memristor dynamics on the computed features, we used the simpler Euclidean distance approach proposed in the original HOTS paper [28]. For each label, we computed a template $H_{label}$ by averaging over all the histograms with that label in
the training set. To classify new digits, we performed template matching using the Euclidean distance measure.

IV. EXPERIMENTAL RESULTS

A. The effects of programmable integration constants on accuracy

Tables I and II show that different pulse settings (Voltage and duration) give rise to different decay time constants. The ability to tune integration constants is fundamental for neuromorphic applications, as spike rates vary between different applications. While these results do not enable us to model the full relationship between pulse settings and time constants, they do enable us to investigate whether different applications benefit from different time constants.

We tested the two-layer network shown in Fig. 4(g to m) on the N-MNIST [29] and POKERDVS [30] datasets. The subsampling factor was 7, which reduces the N-MNIST resolution from 28x28 in layer 1 to 4x4 in layer 2 and the POKERDVS resolution from 35x35 in layer 1 to 5x5 in layer 2. The Time-Surface lateral dimensions for N-MNIST results are \( l^1 = 7 \) and, \( l^2 = 3 \) respectively, for the first and second layer. The Time-Surface lateral dimensions for POKERDVS results are \( l^3 = 5 \) and \( l^4 = 7 \). The number of clusters for the N-MNIST results is \( N^{[1]} = 32 \) and \( N^{[2]} = 96 \). The POKERDVS network was smaller with only \( N^{[1]} = 8 \) and \( N^{[2]} = 64 \) clusters. To eliminate the effect of device stochasticity and enable comparison with other work on these datasets, which typically do not include device stochasticity, we used the ideal model described in Section II-A.

Since our implementation of HOTS uses K-means for learning the time surfaces, which requires relatively little data to train, we only use 10% of the training set for the N-MNIST results. Files were randomly selected at each run. However, our testing results are reported based on performance on the entire test set.

Table III compares the test-set classification accuracies on the two datasets for all the pulse settings listed in Tables I and II. These results were calculated over 5 runs on N-MNIST and 10 runs on POKERDVS. We classified with a polynomial support vector machine of order 3. We report results with additional classifiers in our supplementary materials.

Our results show that we obtained the best performance on the N-MNIST and POKERDVS datasets using different pulse parameters, which resulted in very different time constants. The best performance for N-MNIST were obtained for 1V 1ms-long pulses, which gave time constants \( \tau_1 = 10 \) ms and \( \tau_2 = 390 \) ms. The best performance for POKERDVS were obtained for 200\( \mu \)s-long pulses with amplitude either 1V (\( \tau_1 = 5 \) ms, \( \tau_2 = 92 \) ms) or 4V (\( \tau_1 = 11 \) ms, \( \tau_2 = 501 \) ms). These differences highlight the importance of the ability to tune time constants.

Our LiWES memristive HOTS network achieves state-of-the-art performance on N-MNIST (91.27%), exceeding that reported by Sironi et al. [48] and Iyer et al. [49], despite the use of only 10% of the training data.

B. The effects of stochastic dynamics on accuracy

To analyze the effects of stochastic dynamics on recognition rate on a neuromorphic architecture, we compared the performance of HOTS architectures on the N-MNIST dataset using the stochastic memristor model (the ‘Noisy’ network) and the ideal memristor model (the ‘Ideal’ network) defined in Section II-A.

Since the implementation of in-situ learning on the memristive chip was beyond the scope of this paper, we limited noise analysis to inference only. Calculation and clustering of time surfaces was performed using the Ideal network model only. The Noisy network and the Ideal network share the same sets of clusters, but in the case of the Noisy network, the Time-Surfaces generated by the test set were perturbed by the device stochasticity.

The computation time for this test was heavily dependent on the number of clusters and the number of files. For this reason, we set the number of clusters to \( N^{[1]} = 32 \) for layer 1 and \( N^{[2]} = 64 \) for layer 2. We tested only on a random selection of 10% of the test set every run, and averaged performance over 60 runs.

To ensure the generality of our results, we included results using both the Support Vector Classifier (SVC) and the Euclidean distance classifier (Eucl.). Thus, we considered four cases: Ideal SVC, Noisy SVC, Ideal Eucl. and Noisy Eucl. Each network was trained on the same training sets of N-MNIST data and tested on the same randomly chosen N-MNIST test sets. We also measured classification performance for both layers of the architecture.

The results in Table IV and Figure 5(a) show that while different classifiers result in different absolute accuracy, stochasticity in the memristor dynamics does not significantly affect the classification accuracy (\( t\)-test \( p > 0.05 \)). However, device stochasticity does influence both Time Surfaces and cluster assignment.

Fig. 5(b) compares Time Surfaces computed over the entire array (\( t = 28 \)) using the Ideal and Noisy models. Although the digit is still recognizable in the Noisy Time Surface, we can clearly see additional variation in the individual pixels.

As shown in Figs. 5(c) and (d), this variation leads to incorrect cluster (i.e., polarity) assignment of Time-Surfaces, a phenomenon we refer to as ‘dislocation’ (Fig. 5(e)). The mean percentage of events suffering from cluster dislocation in a single run was 10.58% in Layer 1 and 7.09% in Layer 2, suggesting that multiple layers might decrease the noise effect.

One possible explanation for the maintenance of high classification accuracy despite cluster dislocation is that by summarizing events across the entire recording, histogram-based classifiers are “averaging out” the effect of a relatively small number of cluster dislocations. If this were true, then we might expect classifiers integrating information over shorter time scales to be far more affected by dislocation error.

To determine whether this is not the case, we calculated the Mutual Information (MI) between events at different time scales and labels, using a method originally presented by Akolkar et al. [50]. In this method, we choose a layer \( k \), and sample a random event at that layer from our dataset \( ev^l_i \). We create a temporal window of length \( \delta \) centered on its timestamp.
Mutual information (MI) is a measure of the amount of information one random variable contains about another. In the context of neural networks, it can be used to quantify the amount of information that the spiking activity of a neuron carries about the stimulus. We can calculate the MI between two variables $X$ and $Y$ using the formula:

$$MI(X; Y) = \sum_{x \in X} \sum_{y \in Y} p(x, y) \log \frac{p(x, y)}{p(x)p(y)}$$

where $p(x, y)$ is the joint probability of $X$ and $Y$, and $p(x)$ and $p(y)$ are the marginal probabilities.

To calculate the MI in our experiments, we first computed the Time-Surfaces for the Ideal and Noisy memristor models. These surfaces represent the spiking activity of the neurons over time and across different layers. We then computed the MI between the probability of the stimulus $p$ and the probability of the polarity $P$. We also considered the MI between the probability of the stimulus $S$ and the probability of the stimulus $P(S)$. We repeated this process multiple times including all polarities $p_k$, averaging the result. This value tells us how well the spiking activity of the layer $k$ at timescale $\delta$ encodes the dataset labels. We include additional information on this method in our Supplementary materials.

By computing the MI at different timescales $\delta$, we can see how well spiking activity at different time scales encodes information about the stimulus labels. Since there is only one label for each recording in the N-MNIST and POKERDVS datasets, we expect the MI to decrease monotonically as the timescale $\delta$ decreases, since shorter timescales contain less information (fewer spikes).

We repeat this process multiple times including all polarities $p_k$, averaging the result. This value tells us how well the spiking activity of the layer $k$ at timescale $\delta$ encodes the dataset labels. We include additional information on this method in our Supplementary materials.

By comparing the MI computed for the Ideal and Noisy networks, we can see how cluster dislocation affects the MI. If it is true that classifiers integrating information over shorter timescales contain less information, then we expect the MI to decrease as the timescale $\delta$ decreases. We include additional information on this method in our Supplementary materials.

**Table III**

| Pulse settings | (200µs,1V) | (200µs,2V) | (200µs,3V) | (200µs,4V) | (500µs,1V) | (750µs,1V) | (1ms,1V) |
|----------------|------------|------------|------------|------------|------------|------------|----------|
| N-MNIST        | 90.90 ± 0.22 | 90.92 ± 0.24 | 91.15 ± 0.37 | 90.93 ± 0.21 | 90.09 ± 0.16 | 90.95 ± 0.19 | 91.27 ± 0.29 |
| POKERDVS       | **98.00 ± 3.31** | 96.50 ± 3.90 | 97.50 ± 4.03 | **98.00 ± 3.32** | 97.00 ± 3.32 | 96.50 ± 3.20 | 97.50 ± 4.03 |

**Table IV**

| Classification accuracy of the Ideal and Noisy Networks with Euclidean and SVC classifers |
|-----------------------------------------------|
| Ideal Eucl | One HOTS Layer 60.67% ± 2.11% | Two HOTS Layers 76.12% ± 1.98% |
| Noisy Eucl | 60.69% ± 2.33% | 76.66% ± 2.26% |
| Ideal SVC  | 84.54% ± 1.37% | 86.50% ± 1.33% |
| Noisy SVC  | 84.55% ± 1.33% | 86.76% ± 1.26% |

We then look across different recordings to calculate the probability of finding another event with the same polarity $p_i^k$ in the same temporal window. We can then calculate the MI between the probability of a response $R$ (equal to 1 if an event with polarity $p_i^k$ is present and 0 otherwise), $P(R)$, and the probability of the stimulus $S$ (the label of the input), $P(S)$. We repeat this process multiple times including all polarities $p_k$, averaging the result. This value tells us how well the spiking activity of the layer $k$ at timescale $\delta$ encodes the dataset labels. We include additional information on this method in our Supplementary materials.

By comparing the MI computed for the Ideal and Noisy networks, we can see how cluster dislocation affects the MI. If it is true that classifiers integrating information over shorter

Fig. 5. (a) Recognition rates of the Ideal and Noisy networks with the Support Vector and Euclidean Classifiers. (b) A qualitative comparison between Time-Surfaces computed over the entire input using the Ideal and Noisy memristor models. (c and d) The effect of Time-Surface perturbation on cluster (i.e., polarity) assignment in Layers 1 and 2. Blue dots indicate events where the Ideal and Noisy networks make the same cluster assignment. Otherwise, the Ideal (orange dots) and Noisy (green dots) assign events to different clusters. (e) We call this effect cluster dislocation. (f and g) The Mutual Information between the cluster response and the N-MNIST digit labels for Layers 1 and 2 at different Temporal Integration scales. (h) The Mutual Information Percentage Loss due to cluster dislocation. The effect of dislocation is small and constant across all timescales, except for a singularity when the temporal window is zero due to division by zero MI when computing the percentage. More importantly, cluster dislocation is equally likely to increase or decrease Mutual Information.
timescales are more affected by dislocation error, then we would expect the Noisy network’s MI to decrease faster than the Ideal network’s MI as delta decreases.

Figs. [5f-g] plot the MI for the Ideal and Noisy networks computed over ten runs using the N-MNIST dataset. As expected, the MI for both networks decreases as delta decreases. However, the two curves do not diverge as delta gets smaller, showing the introduction of cluster dislocation due to noise has little effect on the mutual information. We can show this more clearly using the Mutual Information Percentage Loss, defined by \( (MI_{\text{Ideal}} - MI_{\text{Noisy}})/MI_{\text{Ideal}} \). Fig. [5h] plots the Percentage Loss for each individual run. It remains largely constant across timescale, rarely exceeding 5% for the first layer and 2% for the second layer. In addition, the Mutual Information Percentage Loss is equally likely to be positive or negative [5h]. This suggests that rather than causing events to be mapped to less-informative clusters, cluster dislocation often results in events being mapped to equally, if not more, informative clusters.

The MI information loss might be considerably higher for different memristors or datasets. This could affect the accuracy of neuromorphic implementations. One possible solution suggested by this analysis is to exploit the monotonically increasing relationship between timescale and MI shown in Figs. [5f] and (g), which indicates that the lost information might be recovered by increasing the time window size. However, the window size will negatively impact latency.

C. Computational benefits of Memristive dynamics

In this section, we investigate whether the more complex dynamics of volatile LiWES memristors bring computational benefits compared to the simpler dynamics assumed in standard HOTS implementations.

We compare the classification accuracy of single-layer HOTS networks built with Ideal Memristor, a simulated Memristor without STP, and two traditional single-decay HOTS architectures. In order to simulate a memristor without STP, we use the ideal model with Eq. [5f], which causes the memristor response to reset to \( \overline{A_1} + A_2 \) at each new incoming event \( ev_i \) after the end of the write pulse of width \( w \) has been reached. Additionally, we set a single exponential decay model by setting \( k = 1 \), obtaining the original single decay response without STP used for HOTS [28]. Each network was tested with 30 runs of the N-MNIST dataset. Both the training set and test set were independently sampled for each run.

(Fig 6) shows the results. For brevity, we only show results with the Euclidean classifier. Suppl. Table 3 contains additional results. The Memristor model is significantly more accurate than the Memristor without STP and the two single decay HOTS models. Enabling STP results in the largest increase in accuracy.

Our results also suggest that the double exponential decay better integrates temporal information. Figure [7] shows the effects of STP and double-exponential decays on the time-surface representations. Fig. [7a] shows a full digit time-surface at a given time \( \tau_0 \) and a 11x11 Region-Of-Interest (ROI) with three distinct sub-regions. The ROIs are plotted in [7b], with the sub-regions showing the model response to 'Recent events’, 'Past events’ and 'Sensor noise’. The last region represents a portion of the frame where the digit is not present. Activity is only caused by the typical salt and pepper noise of the DVS [4].

Fig. [7c] shows the standard deviation of activity in the sub-regions, which is an indirect measure of the amount of information about recent, past, or noise events represented by the time surface. Exponential decay kernels de-emphasize activity that is too fast or slow compared to their decay time constants. This is evident when compare the standard deviation for recent events (light blue) in the HOTS Long Decay and for past events (dark blue) in the HOTS Short Decay.

In the original HOTS model [28], time surfaces were computed using single exponential decay kernels. Thus, each layer is sensitive to activity only at a single temporal scale. Integration across multiple scales was obtained using multiple layers with increasingly longer time constants. However, the LiWES memristor has double exponential decay response with both short and long time constants. This enables a single layer to integrate information across multiple time scales simultaneously. Thus, the standard deviations of activity for recent and past events are comparable. This is true for both the Memristor model and the Memristor without STP.

The standard deviation from the sensor noise region (in green) achieves its maximum for the HOTS Long Decay model and its minimum for the Memristor model. Longer delays cause the time surfaces to accumulate multiple random events, increasing the standard deviation. In contrast, STP reduces standard deviation by summing the effect of multiple spikes, suppressing the effect of random events. This is consistent with our finding that the Memristor w/STP has smaller standard deviation in the sensor noise region compared to the Memristor w/o STP. This effect might also account for our finding that performance of the network is insensitive to device stochasticity.

V. DISCUSSION

Currently, available neuromorphic processors are still in their infancy, as they aim to replicate biological neurons using silicon [51–54]. However, their application has been limited
due to several factors. First, our understanding of the brain is incomplete, lacking a comprehensive theory explaining its operations. Second, the different physical substrates of silicon and biological brains make it difficult to replicate the fundamental operation of temporal integration in the brain using neuromorphic architectures. Current solutions implement temporal integration digitally [55], [56] or through a combination of capacitors and transistors [57]. In contrast, this work utilizes an electrochemical memristor [24] with transitory conductance response to implement temporal integration on a single component, opening a path towards the development of compact and energy-efficient neuromorphic systems.

Advancements in technology offer a broader range of materials that could potentially facilitate the design of improved silicon-based brains. Architectures using this device challenge the conventional choices for abstraction level and partitioning in mixed-signal neuromorphic processors. These designs can employ more advanced computation building blocks and design rules. Determining the appropriate level of abstraction [58] remains an open question. The level of abstraction closely interacts with the physical substrate and the computational model design.

The commonly used level of abstraction, which closely resembles direct biological replication, models neural computation using coupled ordinary differential equations. The temporal dynamics of this model enable information integration over time, while the coupling across state variables models spatial information integration [59]. Analog continuous time VLSI circuits, such as those described by Mead [60], are commonly used to implement this level of abstraction. Although these circuits offer low power consumption, they suffer from drawbacks such as mismatch and limited programmability.

A related level of abstraction involves coupled difference equations and is commonly implemented using digital design methodologies in standard CMOS processes or FPGAs [51]–[54]. However, even with fully custom designs, these implementations fail to achieve the low power levels sought by neuromorphic engineers.

Hybrid substrates present an intriguing design space that can leverage the advantages of both analog and digital domains [61]. The most prevalent hybrid model utilizes analog circuits for computation and digital circuits for communication [62]–[64]. This approach recognizes that digital circuits operate much faster than the typical spike rate of neurons, enabling a single digital bus to carry signals from multiple neurons. Multi-chip Address Event Representation (AER) networks [65], [66] embody this level of abstraction, where computation within each chip utilizes analog continuous time circuits, while communication between circuits is digital and often asynchronous.

In this context, we advocate for a hybrid model that employs a different partitioning in the abstraction. Rather than dividing along the lines of function (computation vs. communication), we propose a partitioning based on dimension (time vs. space). We argue that analog implementation is optimal for temporal integration of signals, particularly spiking signals, while digital
technologies are better suited for spatial integration. Newly developed memristive technologies \cite{14, 15, 17, 25} provide an excellent physical substrate for temporal integration. In contrast, spatial integration, which requires signal communication across space, is best achieved using digital technologies.

The memristive network we study moves in the direction of the proposed partitioning. It exhibits space-time separability, as it integrates information over time, pixel by pixel, or more generally, neuron by neuron, followed by spatial integration across pixels or neurons. Space-time separability is a well-known principle in digital signal processing algorithms, offering significant implementation advantages \cite{67}.

However, not all neuromorphic algorithms exhibit space-time separability. For instance, not every set of coupled differential equations can be expressed as a space-time separable set of operations, with the majority being unable to do so.

Nevertheless, we argue that a large and compelling class of algorithms, operating at an abstract scale without relying on spiking neurons, specifically those utilizing time surfaces and hierarchies of time surfaces (HOTS) \cite{28, 48, 68}, naturally exhibit space-time separability as described earlier. These algorithms are ideally suited for implementation using a combination of memristive devices for temporal integration and digital spatial integration, particularly clustering and mapping to the nearest cluster centers. By combining HOTS with a novel three-terminal memristor (LiWES), we illustrate how such architectures can be employed for pattern recognition while remaining robust against non-idealities encountered in memristive devices, such as random mismatch and noise.

VI. Conclusion

Recent developments in semiconductor technology have led to the design and creation of a new class of devices called memristors. It has been predicted that memristors will be used in the near future as the atomic component of more advanced and complex systems, which can provide performance superior to conventional transistor-based hardware \cite{69}. In neuromorphic engineering, memristors are more commonly used as "static" synaptic weights for the spatial integration of signals. While the temporal dynamics of memristors are known in the literature, we still need to understand their computational properties better to be able to exploit them fully in practical scenarios.

In this work, we used a LiWES electrochemical memristor to test the effect of programmable time constants, double exponential decay and STP on the widely used MNIST and POKERDV5 datasets. We used single-pulse recordings to build a model of the device and then used it to simulate a HOTS network. The ability to program time constants is important, as different tasks generate spike activity with different temporal dynamics as evidenced by our results comparing the best pulse parameters for the MNIST and POKERDV5 datasets. In this work, we assumed that time constants for all memristors in the network had the same statistics, but moving forward, it may be interesting to investigate setting time constants layer by layer or even neuron by neuron. We showed that the intrinsic stochasticity of the device did not impact accuracy (VLB section). However, we also showed a relationship between latency and accuracy that could be used to offset accuracy loss by increasing integration time in devices with less precise temporal dynamics. This is especially important as it extends our considerations to memristors other than the one we tested, such as two-terminal memristors that also exhibit STP \cite{15, 25}.

One limitation of our results is that we could not include device mismatch in our simulation, as we have yet to realize a LiWES array, which would allow us to characterize this mismatch. However, we have modelled cycle-to-cycle variation, which also gives rise to mismatch in time-surfaces, albeit over time rather than space. Nonetheless, our results showing robustness to this type of mismatch suggest that our network may also be robust to spatial mismatch. This is a promising avenue for future work.

The last section (VLC) explored the computational properties of STP and the double exponential dynamics. Both STP and double exponential decay dynamics increased the accuracy of the network compared to the original HOTS network with single exponentials and no-STP. STP contributes to reducing "Noise" in the network. Multiple exponential dynamics allow temporal integration across a broader time scales. Since time surfaces are based on an exponential decay kernel, akin to biological EPSP/IPSPs, we expect our results to generalize to a wider class of models, such as integrate and fire neurons. These results are of particular importance as they highlight the practical use of less explored properties of this class of memristive devices and allow us to envision a future where memristors are used for temporal data processing and synaptic weight, eliminating the need for more complex analog or digital circuits.

Taken as a whole, our work provides strong evidence that the volatile properties of memristors can become a powerful tool for building a more specialized class of neuromorphic systems while reducing design complexity.

ACKNOWLEDGMENTS

We would like to thank Dr. Sio-Hoi Leng for his valuable comments and discussion during the manuscript preparation, and Richard Newcombe for supporting this work.

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