Lateral energy band profile modulation in tunnel field effect transistors based on gate structure engineering
Ning Cui, Renrong Liang, Jing Wang, and Jun Xu

Citation: AIP Advances 2, 022111 (2012); doi: 10.1063/1.4705398
View online: http://dx.doi.org/10.1063/1.4705398
View Table of Contents: http://scitation.aip.org/content/aip/journal/adva/2/2?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in
Study of tunneling transport in Si-based tunnel field-effect transistors with ON current enhancement utilizing isoelectronic trap
Appl. Phys. Lett. 106, 083501 (2015); 10.1063/1.4913610

A silicon nanocrystal tunnel field effect transistor
Appl. Phys. Lett. 104, 193505 (2014); 10.1063/1.4876765

Strained-Si/strained-Ge type-II staggered heterojunction gate-normal-tunneling field-effect transistor
Appl. Phys. Lett. 103, 093501 (2013); 10.1063/1.4819458

Silicon-based tunneling field-effect transistor with elevated germanium source formed on (110) silicon substrate
Appl. Phys. Lett. 98, 153502 (2011); 10.1063/1.3579242

Heteromaterial gate tunnel field effect transistor with lateral energy band profile modulation
Appl. Phys. Lett. 98, 142105 (2011); 10.1063/1.3574363
Lateral energy band profile modulation in tunnel field effect transistors based on gate structure engineering

Ning Cui, Renrong Liang, Jing Wang, and Jun Xu
Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, People’s Republic of China
(Received 27 February 2012; accepted 4 April 2012; published online 17 April 2012)

Choosing novel materials and structures is important for enhancing the on-state current in tunnel field-effect transistors (TFETs). In this paper, we reveal that the on-state performance of TFETs is mainly determined by the energy band profile of the channel. According to this interpretation, we present a new concept of energy band profile modulation (BPM) achieved with gate structure engineering. It is believed that this approach can be used to suppress the ambipolar effect. Based on this method, a Si TFET device with a symmetrical tri-material-gate (TMG) structure is proposed. Two-dimensional numerical simulations demonstrated that the special band profile in this device can boost on-state performance, and it also suppresses the off-state current induced by the ambipolar effect. These unique advantages are maintained over a wide range of gate lengths and supply voltages. The BPM concept can serve as a guideline for improving the performance of nanoscale TFET devices.

I. INTRODUCTION

As the feature sizes of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) scale down into the nanoscale regime, the devices face the challenge of short channel effects (SCEs), which increase power dissipation and degrade device performance.1 Numerous structures have been introduced to minimize SCEs, such as fully depleted silicon-on-insulators (SOIs),2 FinFETs,3 and nanowire devices.4 Nevertheless, the drift-diffusion mechanism of MOSFETs is a major obstacle that fundamentally limits supply voltage scaling and reduction of power consumption. Recently, tunnel field-effect transistors (TFETs) have received a lot of attention because they can provide a subthreshold swing (SS) lower than 60mV/dec at room temperature, and they can achieve a higher ratio between on- and off-state currents compared to MOSFET devices.5, 6 The structure of TFETs is a reverse-biased PN junction controlled by the gate, while the working principle is based on the band-to-band tunneling (BTBT) mechanism. Due to their inherent asymmetrical configuration, TFETs can work in on-, off-, and ambipolar-states depending on the polarity of the gate voltage.7

Many studies have compared the working principle, modeling, and electrical characteristics of TFETs to those of MOSFETs using both numerical simulations and experimental tests.8–10 However, some issues remain unresolved in TFET research. Previous investigations have focused on the development of special structures to boost the on-state current (Ion) of TFETs, such as source-channel heterojunctions,11, 12 ultra-thin body SOIs,13 and heavily doped tunnel junctions.14 However, these special structures require the use of certain key techniques, and these techniques are difficult to achieve using a standard CMOS fabrication process flow. Another concern about TFET devices is based on the implementation of narrow gap materials, e.g., germanium,7, 15 InGaAs,16 and

ajunxu@tsinghua.edu.cn

2158-3226/2012/2(2)/022111/16 2, 022111-1 © Author(s) 2012

All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. See: http://creativecommons.org/licenses/by/3.0/
Downloaded to IP: 198.91.36.79 On: Mon, 02 Mar 2015 10:45:27
graphene.\textsuperscript{17} The off-state current (I_{off}) of devices using these materials inevitably increases due to the ambipolar effect, which leads to an enlarged average SS and neutralizes the advantages of these devices. Therefore, we tried to find an effective solution that can increase I_{on} and reduce I_{off} and SS simultaneously to be compatible with the CMOS process.

In particular, the lateral energy band profile and the electric field contour can be tuned by the energy band profile modulation (BPM) effect, which manipulates the carrier tunneling probability and space distribution, thus improving device performance. In our previous work, a hetero-material-gate (HMG) structure was proposed to realize the BPM effect in the source-channel junction.\textsuperscript{18} It was shown that the HMG TFET had a higher I_{on} and a lower SS compared to the single-material-gate (SMG) TFET due to the BPM effect. Unfortunately, the ambipolar effect cannot be inhibited using the HMG configuration. Moreover, the ambipolar effect becomes even more pronounced when narrow gap materials are employed. To address this issue, a Si-based TFET design with a symmetrical tri-material-gate (TMG) structure was developed; the gate structure engineers the energy band profile at both the source and drain sides. The properties of the device were analyzed through numerical simulation. It was determined that the device performance of the TMG TFET was enhanced by the BPM effect.

II. DEVICE STRUCTURE AND SIMULATION

The simulations were performed with the 2D Sentaurus Device simulator\textsuperscript{19} using a dynamic nonlocal BTBT model. In contrast to local tunneling models, a nonlocal BTBT model describes a physical picture of the real space carrier transport through the barrier, and it dynamically takes account of the energy band profile along the entire tunneling path. Moreover, the electrons and holes are generated nonlocally at the end of the tunneling path, and the generation rate is obtained from nonlocal path integration. The dynamic nonlocal BTBT model provides a very complex BTBT probability expression, which is decided by both the potential profile and the electric field. Furthermore, the BTBT rate can be reduced to Kane and Keldysh models\textsuperscript{20} in the uniform electric field limit:

\[
G_{BTBT} = A \left( \frac{\xi}{\xi_0} \right)^P \exp \left( -\frac{B}{\xi} \right) \tag{1}
\]

where $\xi$ is the magnitude of the electric field, $\xi_0$ is 1V/cm, and $P = 2.5$ for the indirect tunneling process. Parameters A and B are fitting coefficients, and they were calibrated with experimental Zener diode characteristics, as reported by Fair and Wivell.\textsuperscript{21} Kane’s two-band dispersion relation was utilized due to silicon being an indirect bandgap material. A bandgap narrowing model and Fermi statistics were employed to take into account the effect of high doping concentration in the source and drain regions. The standard drift-diffusion carrier transport model and the Shockley-Read-Hall recombination model were also used. A fine mesh near the tunneling interface was built and carefully assembled.

To ensure fair comparisons, all the SMG, HMG, and TMG device structures described in this study are identical in terms of physical geometry and doping profile; the only difference among these devices is how the gate is engineered. The gate of the SMG TFET uses a single material, as shown in Fig. 1(a). The gate of the HMG TFET consists of two parts, and they have different work functions, as shown in Fig. 1(b). Fig. 1(c) shows our proposed device, which has a symmetrical TMG structure with the gate stack (L_{gate} = L_{S-gate} + L_{C-gate} + L_{D-gate}) being divided into three parts: the S-gate is close to the source region, the C-gate is above the center of the channel, and the D-gate is at the drain side. In the simulations, the materials of the S-gate, C-gate, and D-gate were designed to be Al, Cu, and Al, respectively, and their work functions were 4.1, 4.7, and 4.1 eV, respectively. It is worth mentioning that the work function difference can be precisely tuned by changing a variety of process parameters, such as the type of doping impurity, doping concentration,\textsuperscript{22} and germanium mole fraction.\textsuperscript{23} The thickness of the silicon film on the buried oxide was 30nm. 3nm-thick HfO$_2$ was used as a gate insulator, and its dielectric constant was 22. The following device doping levels were used: 10$^{20}$/cm$^3$ p-type for the source, 10$^{19}$/cm$^3$ n-type for the drain, and 10$^{17}$/cm$^3$ for the...
FIG. 1. Schematic cross-section of the (a) SMG TFET; (b) HMG TFET; and (c) TMG TFET. The gate of the TMG TFET consists of three parts: an S-gate close to the source region, a D-gate close to the drain region, and a C-gate above the center of the channel. The S-gate and D-gate are symmetrical and identical in terms of their material and shape.
lightly doped n-type channel. This type of asymmetrical doping profile is useful for suppressing the ambipolar effect.\textsuperscript{7}

A conceptual process flow was used to achieve the HMG structure based on conventional MOSFET technology, as illustrated in Fig. 2(a). One additional mask is needed for the fabrication of the S-gate, which requires a photolithography resolution that is equal to, or even higher than, that of the gate length. The S-gate can be formed using either an asymmetrical etch or lift-off techniques.\textsuperscript{24} Nevertheless, for TMG devices, the S-gate and the D-gate can be fabricated in one step by a self-aligned symmetrical spacer process, so the material and shape of the S-gate and the D-gate are almost identical, as shown in Fig. 2(b).

In our comparisons of the characteristics of TFET devices with different gate work functions, SS is defined as the average slope when the drain current increases from 0.1fA/mm to 1nA/mm. $V_{\text{turn-on}}$ and $V_{\text{turn-ambipolar}}$ correspond to the gate voltages in on- and ambipolar-states, respectively, when the drain current is equal to 0.1fA/mm. The ambipolar window, which is used to describe ambipolar behavior, is defined as $V_{\text{turn-on}} - V_{\text{turn-ambipolar}}$. $I_{\text{on}}$ is defined as the drain current when $V_{gs} - V_{\text{turn-on}} = 1$V. These definitions are used throughout this paper.
TABLE I. Parameters of the gate structures used in the simulations.

| Gate work function (eV) | LW TFET | HW TFET | HMG TFET | TMG TFET |
|-------------------------|---------|---------|----------|----------|
| Gate length, L_{gate} (nm) | 50      | 50      | 50       | 50       |
| Work function of S-gate, W_{FS-gate} (eV) | 4.1     | 4.1     | 4.1      | 4.1      |
| Length of S-gate, L_{S-gate} (nm) | 6       | 6       | 38       | 6        |
| Work function of C-gate, W_{FD-gate} (eV) | 4.7     | 4.7     | 4.7      | 4.7      |
| Length of C-gate, L_{C-gate} (nm) | 44      | 44      | 44       | 6        |

III. DEVICE PERFORMANCE

A. Transfer characteristics

Fig. 3(a) shows the comparison of the TMG TFET’s transfer characteristics with those of the HMG and SMG TFETs. The SMG TFET with a work function of 4.1eV is referred to as the LW TFET, and the SMG TFET with a work function of 4.7eV is referred to as the HW TFET. The gate structure parameters are summarized in Table I. It can be observed that the shapes of the transfer curves of the LW and HW TFETs are almost identical, except that V_{turn-on} is 0V for the LW TFET and 0.6V for the HW TFET, which is consistent with the difference in gate work function between these two devices. Due to the heterogeneous gate material, the curve of the HMG TFET follows the curve of the LW TFET in the on-state, and it follows the curve of the HW TFET in the off-state. The modulated band profile of the HMG TFET near the source region leads to a higher I_{on} and a reduced SS. The curve of the TMG TFET coincides with the curve of the HMG TFET in both on- and off-states, which indicates that the switching characteristic is not affected by the additional D-gate of the TMG TFET. Steep switching behavior requires the off- and on-state transition of the tunneling barrier width to be strongly dependent on the gate voltage. In the HMG and TMG TFETs, the tunneling distribution is controlled by the D-gate (C-gate in the TMG TFET) when the devices are in the off-state and by the S-gate when the devices are in the on-state. Fig. 3(b) quantitatively illustrates tunneling barrier width as a function of gate voltage (V_{gs} - V_{turn-on}) for the SMG and TMG TFETs. In the SMG TFET, the barrier width slowly decreases as V_{gs} increases. When the TMG TFET is in the off-state, the tunneling barrier width is larger than that of the SMG TFET because the energy band is pulled up by the C-gate. Once the E_c minimum near the source is below the E_T in the source region, tunneling occurs. In this situation, the barrier width of the TMG TFET suddenly decreases, which corresponds to its sharply ascending I_{ds}-V_{gs} curve. Thus, the BPM effect in the HMG and TMG TFETs significantly improves the switching behavior of the devices.

The most obvious difference between the transfer curves of the TMG and HMG TFETs concerns ambipolar behavior. The ambipolar behavior of TFET devices is related to their internal structure: when the valence band of the channel close to the drain side is above the conduction band of the drain region, tunneling can occur at the drain side. In this situation, the device is in the ambipolar-state. As shown in Fig. 3(a), the ambipolar window of the TMG TFET is 269mV, compared to 200mV for the HMG TFET. This difference can be explained by the fact that the ambipolar characteristic of the TMG TFET is improved mainly by the band profile close to the drain region, which is engineered by the additional D-gate. This hinders the occurrence of tunneling and provides a large ambipolar window and much reduced ambipolar current.

B. Output characteristics

Fig. 4 shows the typical output characteristics of the three devices and their second derivatives. The devices used in the simulations were identical to those shown in Fig. 1; the drain voltage varied from 0 to 1.5V and the gate voltage (V_{gs} - V_{turn-on}) was set at 1V. It can be observed that each output curve can be divided into three regions, i.e., exponential, linear, and saturated regions. The
FIG. 3. (a) Transfer characteristics of the LW, HW, HMG, and TMG TFETs. The curve of the TMG TFET coincides with that of the HMG TFET in the on-state, and the TMG TFET has a larger ambipolar window and much less ambipolar current due to the introduction of the D-gate; (b) Source-to-channel tunneling barrier width as a function of gate voltage in the SMG and TMG TFETs. The inserted figure displays the energy band of the TMG TFET in on- and off-states. The abrupt transition of the barrier width between the off- and on-states in the TMG TFET is induced by the local minimum in the conduction band close to the source side.

exponential region in the output behavior of the TFET devices can be explained by the large quantum capacitance of the accumulation channel in the on-state. In the presence of the surface charge layer, the response of the energy bands in the channel to the external gate voltage becomes very small, but the level at which the channel potential is pinned depends on the Fermi energy in the drain region. For small amounts of $V_{ds}$, the drain voltage is applied at the source-channel junction directly, thus resulting in the aforementioned exponential behavior. Furthermore, a certain minimum amount of drain voltage is required to turn the device on. Similar to the gate threshold voltage based on the transfer characteristics in MOSFETs, the drain threshold voltage $V_{td}$ in TFET devices is defined as the drain voltage for which the drain current dependence changes from exponential to linear, and $V_{td}$ can be extracted as the drain voltage where the second derivatives of the differential curves reach their maximum values. As shown in Fig. 4, the $V_{td}$ values of these three TFETs are almost
FIG. 4. Output characteristics of the SMG, HMG, and TMG TFETs and their second derivatives used for the extraction of the drain threshold voltage ($V_{td}$). The gate voltage ($V_{gs} - V_{turn-on}$) was set at 1V. Each output curve is comprised of exponential, linear, and saturated regions. $V_{td}$ is the drain voltage where the second derivatives of the differential curves reach their maximum values.

FIG. 5. Transfer characteristics of the HMG TFET. The work functions of the S-gate and the D-gate vary, but $\Delta WF$ is maintained at 0.4eV. These changes only result in a linear shift of the transfer curve.

identical. This suggests that output behavior is not affected by the BPM effect, although the drain currents of the HMG and TMG TFETs are greater than the drain current of the SMG TFET.

IV. DEVICE OPTIMIZATION

A. Effect of work function difference

In order to analyze the relationship of gate work function and device performance, HMG and TMG TFETs with different gate work functions were examined. Due to the basic principle of the BPM effect, device performance depends on the work function difference of the gate, rather than on specific work function values of each part of the gate. For example, the transfer curve of the HMG TFET with $WF_{S\text{-gate}} = 4.1eV$ and $WF_{D\text{-gate}} = 4.5eV$ is almost the same as that of the HMG TFET with $WF_{S\text{-gate}} = 4.3eV$ and $WF_{D\text{-gate}} = 4.7eV$; the only difference is their $V_{turn-on}$ values, as shown in Fig. 5. This is similar to the case of the HW and LW TFETs. Therefore, in our simulations, $WF_{S\text{-gate}}$ was set at 4.1eV, and $WF_{D\text{-gate}}$ ($WF_{C\text{-gate}}$ in the TMG TFET) varied. Work function difference ($\Delta WF$) is defined as $WF_{D\text{-gate}} - WF_{S\text{-gate}}$ in the HMG TFET and $WF_{C\text{-gate}} - WF_{S\text{-gate}}$ in the TMG TFET.

Fig. 6(a) shows different energy band profiles of the HMG TFET depending on $\Delta WF$ when $V_{gs} = 0.4V$, $V_{ds} = 1V$, and $L_{S\text{-gate}} = 6nm$. As $\Delta WF$ increases, the energy band in the middle of the channel is elevated, and the local minimum in $E_c$ at the source side becomes more significant. It is worth mentioning that the difference between the local minimum and maximum in $E_c$ of the
FIG. 6. Energy band profiles of the (a) HMG TFET; and (b) TMG TFET with ΔWF varying from 0.2 to 1.0eV, $V_{gs} = 0.4V$, and $V_{ds} = 1V$. As ΔWF increases, the local minimum in the conduction band at the source side becomes more significant. The energy band profile at the drain side of the TMG TFET is less steep than that of the HMG TFET.

Channel region is smaller than ΔWF. As shown in Fig. 3(b), these special band profiles are useful for improving the switching characteristic of the TFET devices. Furthermore, the BPM effect is more obvious when ΔWF increases. As shown in Fig. 7, when ΔWF varies from 0 to 0.4eV, the value of SS decreases significantly as $I_{on}$ increases; when ΔWF reaches 0.4eV, SS decreases slightly. Similar simulations were also carried out for the TMG TFET (Fig. 6(b)). The energy band profile nearly coincides with that of the HMG TFET in all situations, except that the energy band contour at the drain side becomes less steep. This indicates that the energy band profile at the source side is hardly affected by the additional D-gate in the TMG TFET, which is also consistent with its electrical properties. As shown in Fig. 7, the values of SS and $I_{on}$ of the TMG TFET are almost identical with those of the HMG TFET in all situations. This suggests that the D-gate does not affect on-state characteristics in TMG TFETs; details about device performance in off- and ambipolar-states will be presented in the next section.
FIG. 7. Subthreshold Swing (SS) and on-state current ($I_{on}$) of the HMG and TMG TFETs depending on the gate work function difference ($\Delta$WF). As $\Delta$WF increases, $I_{on}$ increases and SS decreases for both HMG and TMG TFETs.

### B. Effect of the length of the S-gate

To investigate the influence of gate configuration, HMG and TMG TFETs with different $L_{S\text{-}gate}$ values were examined. $L_{gate}$ was kept at 50nm and $\Delta$WF was set at 0.6eV. $L_{S\text{-}gate}$ in the HMG TFET varied from 0 to 50nm as $L_{D\text{-}gate}$ decreased from 50 to 0nm, and $L_{S\text{-}gate}$ ($L_{D\text{-}gate}$) in the TMG TFET varied from 0 to 25nm as $L_{C\text{-}gate}$ decreased from 50 to 0nm. The $I_{ds}$-$V_{gs}$ curves of the two devices are shown in Fig. 8. When $L_{S\text{-}gate}$ in the HMG TFET increases from 0 to 10nm, the transfer curves become more steep when the devices turn on, and $V_{\text{turn-on}}$ decreases because the channel region controlled by the S-gate is extended. Similar results can be also observed for the TMG TFET.

When $L_{S\text{-}gate} > 10$nm, the difference between these two devices is clear. As shown in Fig. 8, the $I_{off}$ current in the HMG TFET increases as $L_{S\text{-}gate}$ increases. However, for the TMG TFET, $I_{off}$ remains unchanged. The results illustrated in Fig. 9 are equally distinctive. In these simulations, the energy band profile was extracted when $V_{gs} = 0.4$V. As $L_{S\text{-}gate}$ in the HMG TFET increases, several phenomena concerning the energy band profile can be observed. First, when the local minimum in $E_c$ close to the source region is generated gradually, the switching behavior of the HMG TFET is improved by the BPM effect. Second, the local minimum in $E_c$ becomes more significant, which enlarges the overlap between $E_c$ in the source region and $E_c$ in the channel in the same $V_{gs}$. This means that the gate voltage required to turn the device on is reduced, and $V_{\text{turn-on}}$ decreases as $L_{S\text{-}gate}$ increases. On the other hand, the tunneling at the drain side is controlled by the D-gate, which is not affected by the increase in $L_{S\text{-}gate}$. Thus, $V_{\text{turn-ambipolar}}$ in the HMG TFET remains unchanged, and the difference between $V_{\text{turn-on}}$ and $V_{\text{turn-ambipolar}}$ is reduced. Once $V_{\text{turn-on}} = V_{\text{turn-ambipolar}}$, the tunneling can occur simultaneously at the source and drain sides, and the off-state of the HMG TFET disappears. A further increase in $L_{S\text{-}gate}$ results in $V_{\text{turn-on}} < V_{\text{turn-ambipolar}}$ and leads to an elevated $I_{off}$, as shown in Fig. 8(a).

In the TMG TFET, the work function of the D-gate is lower than that of the C-gate. The energy band close to the drain region is pulled down by the D-gate, and it becomes less steep as $L_{S\text{-}gate}$ increases. As shown in Fig. 9(b), the energy band profile of the TMG TFET nearly coincides with that of the HMG TFET in all situations except for that at the drain side. The special energy band contour suppresses the tunneling at the drain side and reduces $V_{\text{turn-ambipolar}}$ simultaneously. The quantitative relationship between the ambipolar window ($V_{\text{turn-on}}$-$V_{\text{turn-ambipolar}}$) and $L_{S\text{-}gate}$ is shown in Fig. 10. The value of the ambipolar window of the HMG TFET decreases continually as $L_{S\text{-}gate}$ increases. When $L_{S\text{-}gate}$ in the TMG TFET is smaller than 10nm, the value of the ambipolar window decreases as $L_{S\text{-}gate}$ increases, but it does so at a slower rate than in the HMG TFET because the D-gate is not large enough to thoroughly suppress the tunneling at the drain side. When $L_{S\text{-}gate} > 10$nm, the value of the ambipolar window stops decreasing and starts to rise. In the TMG TFET, $V_{\text{turn-on}}$ is always larger than $V_{\text{turn-ambipolar}}$. Thus, when $V_{\text{turn-ambipolar}} < V_{gs} < V_{\text{turn-on}}$, no tunneling occurs at either the source or the drain sides, which corresponds to the off-state of the TMG device. Therefore, the
FIG. 8. Transfer characteristics of the (a) HMG TFET; and (b) TMG TFET as a function of LS-gate at $V_{ds} = 1$V. When $L_{S-gate}$ is larger than 10nm, $I_{off}$ of the HMG TFET increases and that of the TMG TFET remains unchanged.

TMG TFET can suppress the ambipolar effect and provides a superior design window compared to the HMG TFET.

C. Design window of gate configuration

In the previous two sections, the influence of $L_{S-gate}$ and $\Delta WF$ on TFET devices were studied independently. To obtain an optimized design of the gate configuration in the HMG and TMG TFETs, the impacts of $L_{S-gate}$ and $\Delta WF$ on the design window were investigated together. In the simulations, $L_{S-gate}$ in the HMG TFET varied from 0 to 50nm, and in the TMG TFET, it varied from...
FIG. 9. Energy band profiles of the (a) HMG TFET; and (b) TMG TFET with $L_{S\text{-gate}}$ increasing from 2 to 30nm and $V_{gs} = 0.4V$, $V_{ds} = 1V$. The energy bands of the TMG TFET are pulled down by the D-gate, which suppresses the tunneling at the drain side and reduces $I_{off}$.

0 to 25nm; $L_{gate}$ was kept at 50nm. $\Delta WF$ varied from 0.3 to 0.8eV. As shown in Fig. 11(a), when $L_{S\text{-gate}}$ increases from 0 to 10nm, SS decreases significantly due to the BPM effect. Once $L_{S\text{-gate}}$ exceeds 10nm, SS in the HMG TFET increases and becomes saturated in the range of 20 to 40nm because of the aforementioned elevated $I_{off}$ due to the ambipolar effect. Similar phenomena can be observed when $\Delta WF$ is equal to 0.8eV; the only differences are the minimum and maximum values of SS and the corresponding value of $L_{S\text{-gate}}$. When $\Delta WF$ is equal to 0.3eV, $I_{off}$ of the HMG TFET remains $10^{-17}A/mm$ because the ambipolar window is not affected by $\Delta WF$ in this situation, as shown in Fig. 11(b). When $L_{S\text{-gate}}$ is larger than 15nm, the position corresponding to the local minimum $E_c$ is farther away from the source region (Fig. 9(a)); this means that the tunneling path increases and tunneling current decreases when the device turns on. Thus, the value of SS increases slowly when $L_{S\text{-gate}}$ varies from 15 to 50nm. Therefore, optimization of the HMG TFET involves a tradeoff between improved SS and a corresponding increased $I_{off}$ due to the ambipolar effect. In contrast, the
FIG. 10. Ambipolar window of the HMG and TMG TFETs depending on $L_{S\text{-gate}}$. As $L_{S\text{-gate}}$ increases, the ambipolar window of the HMG TFET decreases gradually, while that of the TMG TFET remains larger than 200mV.

value of $I_{\text{off}}$ of the TMG TFET remains almost unchanged for a wide range of $L_{S\text{-gate}}$ values and is not affected by $\Delta W_F$. Furthermore, the minimum value of $SS$ in the TMG TFET decreases in the same way as that of the HMG TFET, but the maximum value of $I_{\text{off}}$ remains unchanged if $\Delta W_F$ increases from 0.3 to 0.8eV. Thus, optimization of the TMG TFET involves choosing appropriate gate materials that have sufficient $\Delta W_F$. At the same time, the TMG TFET can provide a superior process tolerance of gate configuration compared to the HMG TFET.

D. Gate length scaling effects

To investigate whether the BPM effect was present when the feature size of the devices decreased, the performances of HMG and TMG TFETs with different gate lengths were also examined. In the simulations, $\Delta W_F$ was maintained at 0.6eV and the supply voltage was 1V. The devices of HMG and TMG TFETs represent SMG TFETs when $L_{S\text{-gate}}$ is equal to 0nm.

As the gate length of the TFET device decreases from 50 to 15nm, the direct tunneling from source to drain regions increases significantly and dominates the composition of the off-state current. Thus, $SS$ increases significantly, as shown in Fig. 12. When the gate length is shorter than 20nm, the curve of the HMG TFET is similar to that of the TMG TFET because the ambipolar current is much lower than the direct tunneling current. Furthermore, the $SS$ values of both HMG and TMG TFETs can be minimized when gate length reaches 15nm, even when the main leakage is not due to the ambipolar effect. The optimized value of $L_{S\text{-gate}}$ is maintained around 5nm when $L_{G\text{-gate}}$ varies from 50 to 15nm. Therefore, the optimized value of $L_{S\text{-gate}}$ is independent of $L_{G\text{-gate}}$; rather, it is largely determined by $\Delta W_F$. These results indicate that device performance of TFETs can be enhanced by the BPM effect regardless of the gate length.

To gain more insight into the scaling-down characteristics of TFET devices, the performances of the three TFETs at different levels of supply voltage were thoroughly investigated. In the simulations, $L_{S\text{-gate}}$ was set at 6nm and $\Delta W_F$ was kept at 0.6eV. Other parameters were set at their default values. As shown in Fig. 13, when the supply voltage is 1.5V, $I_{\text{on}}$ of the HMG TFET is about three times higher than that of the SMG TFET, but the HMG TFET has a high $I_{\text{off}}$ because of the ambipolar effect. The TMG TFET has the same $I_{\text{on}}$ as the HMG TFET, but its $I_{\text{off}}$ is smaller compared to that of the HMG TFET and is as large as that of the SMG TFET. These results confirm that $I_{\text{off}}$ induced by the ambipolar effect can be effectively suppressed by the TMG structure. On the other hand, when the supply voltage is 1V or 0.5V, $I_{\text{off}}$ is not decided by the ambipolar effect. $I_{\text{on}}$ and $I_{\text{off}}$ of both TMG and HMG TFETs are almost identical in these situations. Therefore, it can be speculated that the TMG TFET has superior current performance even at low supply voltage.

Note that an effective approach for boosting the device performance of MOSFETs is to enhance the carrier mobility. However, this method does not make much sense in TFET devices because the electrical characteristics are mainly determined by the space distribution of tunneling probability and...
FIG. 11. (a) SS and (b) $I_{\text{off}}$ of the HMG TFET (solid) and the TMG TFET (hollow) depending on the length of the S-gate. The work function difference ranges between 0.3eV (square), 0.6eV (triangle), and 0.8eV (circle). In the HMG TFET, the reason for the increased maximum value of SS is that $I_{\text{off}}$ is higher due to the ambipolar effect. However, this effect can be significantly suppressed by the additional D-gate in the TMG TFET.

the energy band profile. In many studies on TFETs, including examinations of hetero-source,$^{11,12}$ dual-material-gate,$^{27}$ and hetero-gate-dielectric$^{28}$ structures, the BPM effect was actually used to improve the properties of the devices, but it was not explained clearly how this was achieved. In our study, the BPM effect was achieved directly by introducing different gate configurations with lateral work function differences. Thus, the energy band contours can be easily tailored to improve the device characteristics of TFETs.

V. CONCLUSIONS

In this paper, a TFET with a symmetrical TMG structure was proposed. Three TFETs with different gate configurations were analyzed and compared in detail. The TMG TFET demonstrated excellent electrical performance. The enhanced on-state characteristic of the TMG TFET was due to the source-channel BPM effect, which led to an abrupt transition between the off- and on-states. In addition, the improved ambipolar-state performance was attributed to the drain-channel BPM
FIG. 12. SS versus Ls-gate for the (a) HMG TFET and (b) TMG TFET with Lgate varying from 15 to 50nm. The work function difference was set at 0.6eV. SS can be minimized even when Lgate decreases to 15nm for both HMG and TMG TFETs. The optimized value of Ls-gate is around 5nm regardless of the value of Lgate.

effect, which suppressed the ambipolar effect and resulted in a low off-state current. Conventional approaches for suppressing the ambipolar effect involve using an underlapped drain structure or an asymmetrical doping profile between the source and drain regions. The TMG structure was shown to be another effective way to provide a large channel-drain tunneling barrier, which inhibited the tunneling at the drain side in the ambipolar-state. Also, the optimization of gate materials and gate structures was conducted, and it was demonstrated that the TMG TFET had a better design window and a superior process tolerance compared to the HMG TFET. It can be concluded that the device performance of TFETs might be boosted by the BPM effect, which can be achieved directly by gate structure engineering.
FIG. 13. $I_{on}$ versus $I_{off}$ for the SMG, HMG, and TMG TFETs with different gate lengths and supply voltages. The length of the S-gate ($L_{S-gate}$) was set at 6nm and the work function difference ($\Delta WF$) was 0.6eV. At nearly every technology node, the TMG TFET has an increased $I_{on}$ and a reduced $I_{off}$ compared to the SMG and HMG TFETs.

ACKNOWLEDGMENT

This work was supported in part by the State Key Development Program for Basic Research of China (No. 2011CBA00602), and the National Natural Science Foundation of China (No. 60876076, 60820106001).

1. E. J. Nowak, “Maintaining the benefits of CMOS scaling when scaling bogs down,” IBM J. Res. Develop. 46, 169 (2002).
2. M. Bruel, “Silicon on insulator material technology,” Electron. Lett. 31, 1201 (1995).
3. D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, I. Bokor, and C. Hu, “FinFET—a self-aligned double-gate MOSFET scalable to 20 nm,” IEEE Trans. Electron Devices 47, 2320 (2000).
4. H. T. Ng, S. Han, T. Yamada, P. Nguyen, Y. Chen, and M. Meyyappan, “Single crystal nanowire vertical surround-gate field-effect transistor,” Nano Lett. 4, 1247 (2004).
5. M. R. William and A. J. A. Gehan, “Silicon surface tunnel transistor,” Appl. Phys. Lett. 67, 494 (1995).
6. Q. Zhang, W. Zhao, and A. Seabaugh, “Low-subthreshold-swing tunnel transistors,” IEEE Electron Device Lett. 27, 297 (2006).
7. T. Krishnamohan, D. Kim, S. Raghu, and K. Saraswat, “Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and <60mV/dec subthreshold slope,” in International Electron Device Meeting, Tech. Dig (IEDM08), (2008).
8. W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” IEEE Electron Device Lett. 28, 743 (2007).
9. J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, “Band-to-band tunneling in carbon nanotube field-effect transistors,” Phys. Rev. Lett. 93, 196805 (2004).
10. A. Seabaugh and Q. Zhang, “Low-voltage tunnel transistors for beyond CMOS logic,” Proc. IEEE 98, 2095 (2010).
11. G. Han, P. Guo, Y. Yang, C. Zhan, Q. Zhou, and Y.-C. Yeo, “Silicon-based tunneling field-effect transistor with elevated germanium source formed on (110) silicon substrate,” Appl. Phys. Lett. 98, 153502 (2011).
12. S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, “Ge-source tunnel field effect transistors with record high $I_{on}/I_{off}$,” in VLSI Symp. Tech. Dig. (2009).
13. A. Ford, C. Yeung, S. Chuang, H. Kim, E. Pas, S. Krishna, C. Hu, and A. Javey, “Ultrathin body InAs tunneling field-effect transistors on Si substrates,” Appl. Phys. Lett. 98, 113105 (2011).
14. R. Jiaveri, V. Nagavaran, and J. W. Doo, “Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor,” IEEE Trans. Electron Devices 58, 80 (2011).
15. D. Kazazis, P. Jannaty, A. Zaslavsky, C. Le Royer, C. Tabone, L. Clavelier, and S. Cristoloveanu, “Tunneling field-effect transistor with epitaxial junction in thin germanium-on-silicon,” Appl. Phys. Lett. 94, 263508 (2009).
16. H. Zhao, S. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, “$In_{x}Ga_{1−x}As$ tunneling field-effect transistors with an $I_{on}$ of 50 $\mu A/\mu m$ and a subthreshold swing of 86 mV/dec using $HfO_{2}$ gate oxide,” IEEE Electron Device Lett. 31, 1392 (2010).
17. Y. Yoon and S. Salahuddin, “Inverse temperature dependence of subthreshold slope in graphene nanoribbon tunneling transistors,” Appl. Phys. Lett. 96, 013510 (2010).
18. N. Cui, R. Liang, and J. Xu, “Heteromaterial gate tunnel field effect transistor with lateral energy band profile modulation,” Appl. Phys. Lett. 98, 142105 (2011).
19. Sentaurus User’s Manual, Synopsys, Inc. Mountain View, CA, 2010. v. 2010.03.
20. E. Kane, “Theory of tunneling,” J. Appl. Phys. 32, 83 (1960).
21. R. B. Fair and H. W. Wivel, “Zener and avalanche breakdown in As-implanted low-voltage Si $n-p$ junctions,” IEEE Trans. Electron Devices 23, 512 (1976).
22 M. Pawlak, A. Lauwers, T. Janssens, K. Anil, K. Opsomer, K. Maex, A. Vantomme, and J. Kittl, “Modulation of the workfunction of Ni fully silicided gates by doping: dielectric and silicide phase effects,” Electron Device Lett. 27, 99 (2006).
23 T.-J. King, J. Pfister, and K. C. Saraswat, “A variable-work-function polycrystalline-Si_{1-x}Ge_{x} gate material for submicrometer CMOS technologies,” IEEE Electron Device Lett. 12, 533 (1991).
24 X. Zhou, “Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFET’s) with gate-material engineering,” IEEE Trans. Electron Devices 47, 113 (2000).
25 C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, and S. Mantl, “Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors,” Solid State Electron. 53, 1126 (2009).
26 K. Boucart and A. Ionescu, “A new definition of threshold voltage,” Solid State Electron. 52, 1318 (2008).
27 S. Saurabh and M. J. Kumar, “Novel attributes of a dual material gate nanoscale tunnel field-effect transistor,” IEEE Trans. Electron Devices 58, 404 (2011).
28 W. Y. Choi and W. Lee, “Hetero-gate-dielectric tunneling field-effect transistors,” IEEE Trans. Electron Devices 57, 2317 (2010).
29 A. Verhulst, W. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” Appl. Phys. Lett. 91, 053102 (2007).