Abstract. The neuromorphic BrainScaleS-2 ASIC comprises mixed-signal neurons and synapse circuits as well as two versatile digital microprocessors. Primarily designed to emulate spiking neural networks, the system can also operate in a vector-matrix multiplication and accumulation mode for artificial neural networks. Analog multiplication is carried out in the synapse circuits, while the results are accumulated on the neurons’ membrane capacitors. Designed as an analog, in-memory computing device, it promises high energy efficiency. Fixed-pattern noise and trial-to-trial variations, however, require the implemented networks to cope with a certain level of perturbations. Further limitations are imposed by the digital resolution of the input values (5 bit), matrix weights (6 bit) and resulting neuron activations (8 bit). In this paper, we discuss BrainScaleS-2 as an analog inference accelerator and present calibration as well as optimization strategies, highlighting the advantages of training with hardware in the loop. Among other benchmarks, we classify the MNIST handwritten digits dataset using a two-dimensional convolution and two dense layers. We reach 98.0% test accuracy, closely matching the performance of the same network evaluated in software.

Keywords: Analog Accelerator · Neural Network Processor · Neuromorphic Hardware · Convolutional Neural Networks · Machine Learning · In-memory Computing · MNIST

1 Introduction

Artificial neural networks (ANN) find application in a wide variety of fields and problems. With networks growing in depth and complexity, the increase of computational cost becomes more and more significant [1]. In fact, execution time and power consumption often represent the crucial limiting factors in further scaling and in the application of ANNs [2].

A large fraction of the computational cost for neural network-based inference is spent on vector-matrix multiplications [3]. With their massive parallelization
of floating point calculations, GPUs already cut runtime significantly compared to CPUs. Computational complexity can often be cut by representing and processing data with reduced precision [4]. Specialized digital inference accelerators have been presented [5, 6] that offer further efficiency improvements over implementations on general-purpose hardware. Potentially even more efficient ASICs could be based on mixed-signal circuit designs by exploiting physical processes for computational purposes [7]. Drawbacks of such systems can include vulnerability to fixed-pattern and trial-to-trial variations, resulting in distorted network configurations and reduced reproducibility. Similar to digital solutions with reduced precision, networks have to cope with limited weight resolution, which can be as low as one bit [8].

In this work, we demonstrate BrainScaleS-2 [9] as an analog inference accelerator. We describe the hardware configuration and operating principle of analog vector-matrix multiplication on the ASIC and benchmark the system’s performance by training and classifying the MNIST dataset of handwritten digits [10]. We further discuss calibration and the benefits of training with hardware in the loop as strategies to counter chip-specific fixed-pattern variations [11, 12].

2 Methods

BrainScaleS-2 is a mixed-signal ASIC fabricated in a 65 nm CMOS process by TSMC that has originally been designed as an accelerator for biologically plausible spiking neural networks. It features analog circuits emulating neurons and synapses as well as digital periphery for communication, parameter storage, and realtime control. Recent additions to the system allow for in-memory computation of multiply-accumulate operations within the chip’s analog core, thereby making the system applicable for inference with artificial neural networks [9]. Matrix multiplication can also be combined with spiking operation, thus seam-
Fig. 2: **A**: Illustration of a multiply-accumulate operation. The vector value controls the length of the current pulses, the matrix weight their amplitude. The currents are integrated on the neuron’s membrane. **B**: The recorded membrane trace clearly shows the integration phase where the synaptic inputs are integrated, after which the result is digitized (dotted line). Afterwards, the voltage decays exponentially towards the resting potential.

A less integration of a partially spiking network is possible. The chip contains 512 analog neurons arranged in two blocks, each neuron receives input from 256 synapses. Thus, BrainScaleS-2 can be used to multiply a vector with 256 entries to a matrix comprising 512 columns. An architectural overview of the circuitry for processing vector-matrix multiplications on BrainScaleS-2 is depicted in fig. 1. Digitally encoded input vectors are injected from the left, converted to the analog domain and multiplied within the central synapse array. Each neuron accumulates values from its corresponding synapse column. The resulting vector of neuron activations is read out in parallel via a columnar analog-to-digital converter (CADC).

**Multiplication in analog synapse circuits.** Within the synapse array, the multiplication of an input value with the synaptic weight is modelled as the electrical charge $Q = I \cdot \Delta t$ emitted during a current pulse of variable length and amplitude. The current $I$ is determined by a 6 bit weight stored locally in each synapse. The time window $\Delta t$ during which that current is emitted is modulated by circuitry in the synapse drivers (triangles on the left in fig. 1). The value is set by the payload of input events, which is otherwise used to select a subset of synapses from a row. More specifically, we use 5 bit of this label to encode the pulse length $\Delta t$.

Each row of synapses can be connected to the afferent neurons with either positive or negative sign. To achieve signed weights, two rows of synapses can be combined to represent a single logical row. This configuration, however, reduces the number of available vector entries from 256 to 128. When using signed weights, the remaining input label bit is still available to differentiate two sets of synapses, therefore two different multiplications can be executed side by side.
Neurons integrate synaptic currents. Each neuron uses its membrane to accumulate the individual multiplication results from its respective synaptic column. They integrate the positive and negative charge contributions, as sketched in fig. 2A. Motivated by spiking operation, the input signals are low-pass filtered with finite time constant. To speed up integration and for reduction of synaptic input saturation, the minimum time constant of approximately 1\( \mu \text{s} \) was configured.

The neurons’ dynamics are based on a leaky integrator model commonly used for spiking networks [13]: A resistor continuously pulls the membrane voltage, which is physically represented across a capacitor, towards a resting potential. The resulting dynamics constitute a crucial part for the emulation of spiking networks. In contrast, they can lead to distortions in the accumulation of vector matrix multiplication results which do not contain implicit timing information. In order to stabilize the accumulated voltages and reduce the effect of noise, we configured a rather large but finite resistance. The leak resistance leads to an exponential decay of the integrated charge, which can be seen in fig. 2B.

Digitization of results. The membrane potentials are digitized in parallel for all 256 neurons connected to a synapse matrix, using the CADCs, and stored via the on-chip microprocessors. The resulting 8 bit values represent the neuron activations and are the result of the multiply-accumulate (MAC) operation.

By aligning the choice of the resting potential with the dynamic range of the ADC, two operating modes can be selected: In case the lower end of the ADC range coincides with the resting potential, negative activations are cut off. In this configuration, the neurons behave as hardware rectified linear units (ReLU).

In case the inputs a neuron receives exceed the size of the synapse matrix, the network can be partitioned into smaller matrices which are evaluated in a time multiplexed fashion [14]. Since the activation function needs to be applied after combining the individual results, negative activations must be representable. For this purpose, the resting potential can be chosen centered in the ADCs’ dynamic ranges.

2.1 Structure of a multiply-accumulate operation

To compile a MAC operation from the elements outlined above, the sequence shown in fig. 3 can be applied.
1. To begin with, the weight matrix is written to the synapses. Writing all \(256 \times 512\) values takes about 5 ms. Batched execution can minimize the amount of expensive reconfiguration.

2. A reset of the membrane potentials removes any previous state accumulated by the neurons. An immediate read of the voltages establishes a baseline activation to suppress low frequency noise. Resetting all neurons takes approximately 1 \(\mu\)s.

3. The vector inputs are sent sequentially to the chip. Between events, wait times of 8–200 ns are inserted. These mitigate saturation effects in the neurons’ synaptic inputs, which can occur in case multiple inputs of large amplitude are sent in a short period of time. To improve the signal-to-noise ratio, the activations on the membranes can be increased by incorporating resend of the input vectors within a single integration phase. Wait times as well as the number of resends must be optimized considering the neurons’ decay times, which limit the maximum integration time. Alternatively, the membrane capacitance can be reduced, yielding higher activations, but also shorter decay time constants. Skipping inputs of zero reduces the overall runtime, especially in conjunction with ReLU activation functions.

4. The activations are digitized after the accumulation of charges. Considering the finite time constant of the synaptic inputs, a waiting period of 2 \(\mu\)s is inserted for the membrane potential to settle. The ADC conversion takes 1.5 \(\mu\)s.

2.2 Calibration

Transistor-level mismatch in the manufacturing process of an ASIC leads to inhomogeneous electrical properties of the fabricated circuits. Due to the analog nature of BrainScaleS-2, the resulting fixed-pattern variations cause each neuron and synapse to behave differently when presented with similar input. Without calibration, networks sensitive to such perturbations can not perform up to their full potential on the analog substrate, as weights and activations would be distorted. BrainScaleS-2 therefore provides a substantial amount of digitally controlled parameters that allow equalization of all computational units through calibration.

The operating point of the neuron circuits is determined by a set of internal parameters and references. Some parameters are of technical nature and need to be calibrated to ensure correct operation. Others directly influence the circuit dynamics, e.g. the neurons’ time constants and resting potentials. Most importantly, the strength of the synaptic currents has to be equalized across neurons: It determines the increment of the membrane potential as a response to the synaptic stimulation. The response of all 512 neurons to constant stimuli is shown in the histograms of fig. 4A, separately for the calibrated and uncalibrated states. For both, positive and negative contributions, the synaptic strength has been calibrated to a precision of 7\%.

Calibration is also applied to the pulse generation circuits in the synapse drivers. The length of the current pulses encoding the 5 bit input values is subject
to row-wise random offsets. Calibration registers allow to strongly reduce these variations to 0.3 ns.

We developed a collection of optimization routines for BSS-2, which automate such calibration steps and allow to set the hardware up for matrix multiplication usage. The code is based on the Python API of Müller et al. [15] and may also be used for configuring the system for spiking neural networks.

2.3 Training with hardware in the loop

Remaining imperfections after calibration can still lead to a loss of performance when directly transferring trained network models to an analog computing substrate. In the context of spiking neural networks, it has been previously shown that integrating the analog hardware into the training loop can restore the original performance [11, 12]. For some parameters, such training in the loop can in fact replace explicit calibration [16]. For the analog matrix multiplication described in this manuscript, the gradients are calculated based on measured activations, only assuming linearity of the synaptic weights. A detailed description of the implementation and integration into PyTorch [17] is given by Spilger et al. [14].

3 Results

3.1 Characterization

We first evaluated the performance of BrainScaleS-2’s matrix multiplication mode by configuring a synthetic test matrix. In the left half, weights increased linearly from left to right, all synapses in column $i$ were set to weight $w = i - 63$. In the right half, each synapse was set to a random weight, drawn uniformly from -63 to 63. Multiple homogeneous vectors of different amplitude were used to characterize the linearity of both vector entries and matrix weights (fig. 4B).

For lower weights and inputs, the multiplication followed the expected linear behavior. For higher activations, saturation occurred, which is most clearly observable for the vector with entries of 15. However, we expect most real-world networks to use sparser matrices with more balanced excitatory and inhibitory weights than this test. In the right part of the matrix, the random weights resulted in activations close to zero. It is notable that per column this activation was either positive or negative, depending on the exact mean of the associated weights and scaling with the injected vectors’ values. This suggests that both, positive and negative inputs can be summed correctly and have been tuned to the same strength.

3.2 MNIST benchmark

The above measurements indicate that the analog substrate can indeed be used to perform MAC operations. To investigate its performance on a common benchmark, the MNIST [10] dataset is used. Spilger et al. [14] additionally trained and classified the Human Activity Recognition dataset on BrainScaleS-2.
Fig. 4: A: Histogram of amplitudes received on all neurons for equal inputs. After calibration (colored) the width of the distribution is decreased compared to the uncalibrated state (gray). B: Characterization of analog multiplication results, sweeping both matrix weights and vector entries. The left half of the synapse matrix was configured such that weights increased from a value of -63 in the leftmost column to +63 in the 127th column with an increment of one. Within each column, all weights were set to the same value. The right half was set to random weights for each synapse. We injected four constant input vectors, each consisting of 128 entries of 0, 3, 7 and 15. Error bars indicate the standard deviation within 30 runs.

Models We examined the performance of two different network models. Both relied on ReLU activation functions for the hidden layers and a softmax for the output layer. The two networks did not incorporate a bias. They were trained with the Adam optimizer [18] in TensorFlow [19] using 32 bit float weights.

The convolutional model was based on images zero-padded by one to 30×30 pixels. It consisted of a two-dimensional convolutional layer, a dense layer of 128 neurons and 10 label units. The convolution layer used 20 10×10 filters with a stride of 5×5.

The dense model consisted of two fully connected layers of 64 and ten neurons, respectively. Due to its small size, this model directly fits into the on-chip weight matrix and does not require reconfiguration.

Accuracy As a first step in transferring the models to BrainScaleS-2, we discretized the weights to 6 bit integers plus sign. Evaluating both networks in software showed only slight drops in performance (table 1).

When executing the convolutional network on BrainScaleS-2, the classification performance on held-out test data dropped to 92.1%, indicating a non-ideal calibration of and temporal noise in the analog circuits. After a continued train-
Table 1: MNIST classification accuracy in percent for two models in different conditions. The networks were trained in software using 32 bit float weights. Discretization to 6 bit integer weights plus sign had little impact on performance. Transferring the network to the chip lead to a loss of accuracy, which could be restored after training with hardware in the loop.

|                     | software | hardware |
|---------------------|----------|----------|
|                     | 32 bit   | 6 bit    |
|                     | float    | int      |
| convolutional model | 98.29%   | 98.10%   |
| dense model         | 97.43%   | 97.36%   |

|                     | only     | trained  |
|---------------------|----------|----------|
|                     | in the loop |         |
| convolutional model | 92.13%   | 98.01%   |
| dense model         | 92.46%   | 96.30%   |

Fig. 5: Confusion matrix of the dense network running MNIST. Left: Executed pre-trained model on hardware, no re-training. Right: Results after training one epoch with hardware in the loop. Note the logarithmic color bar in both plots.

ing with hardware in the loop, an accuracy of 98.0% could be restored, closely matching the results obtained in software. A similar behavior was observed for the smaller dense model, with 96.3% after training in the loop. Here, the discrepancy between software and hardware performance was more pronounced, we suspect that with the smaller number of synapses involved, the potential for correction is also lower as there is less redundancy. For the dense network, confusion matrices are shown in fig. 5. Classification works for all digits, no systematic misclassification is observable.

**Energy consumption** A bug in the current chip revision requires constant reconfiguration of the synapse matrix for each input vector. It yields a drastically increased runtime and energy consumption, far off the targeted performance for BrainScaleS-2. We expect the performance to increase by two to three orders of magnitude for the next chip revision.
Currently, when fully utilizing the resources on hardware, vectors of up to 256 entries can be multiplied with matrices of up to 512 columns. One of these vector-matrix multiplications takes 5 ms, and at a power consumption of approximately 0.3 W [12], takes 1.5 mJ. In signed mode, four multiplications involving only a subset of neurons can be executed simultaneously, all receiving independent full-size vector inputs. This is possible utilizing the synapse label bits and both synapse matrices on chip.

Assuming parallelized and batched execution, inference with the convolutional network takes 40 ms per image, resulting in an energy consumption of 12 mJ. The smaller dense network, again assuming parallel execution, requires 10 ms and therefore 3 mJ per image.

Calibration vs. learning It has previously been shown that, to a certain degree, learning can replace the need for explicit calibration [16]. To analyze such effects for the presented models, we started with a software-trained network and then detuned the calibration of the neurons’ leak conductance and synaptic input amplitudes by continuously transitioning between the calibrated and uncalibrated state. The latter resulted from taking the median of the respective parameter distribution across all neurons (fig. 4A). For multiple configurations on this spectrum, we then continued training with hardware in the loop for one epoch.

Fig. 6: MNIST accuracy when detuning the calibrated neuron parameters, shown for the dense network. Left: Accuracy before and after training one epoch with hardware in the loop. Results show the mean and standard deviation of 10 runs classifying the 10 000 test images with unchanged parameters. Right: Accuracy per batch during the one epoch of training. 200 images per batch, 300 batches per epoch. Colors indicate the state of calibration, corresponding to the left plot.
Within that single epoch, the network adapted to the changed parametrization of the substrate (fig. 6): Depending on the strength of decalibration, a strong loss of performance could be observed before re-training. After one epoch, a test accuracy of 96.07% was restored (decalibration factor: 1.0), representing only a slight drop down from 96.31% for the calibrated network.

In the uncalibrated state, synaptic input amplitudes differed by up to a factor of four. This can be interpreted as a reduction of the effective weight resolution from 6 bit to only 4 bit.

We replicated this reduction of resolution to 4 bit in software and observed a reduced accuracy of 96.99% compared to the original performance of 97.36%. Our results therefore coincide with the expectations.

4 Discussion

In this publication, we have shown that BrainScaleS-2 can be successfully used for vector-matrix multiplication, especially in the context of deep convolutional neural networks. We have presented a set of calibration mechanisms to set up the analog system and equalize fixed-pattern variations of the computational units. Improvements upon a pre-trained and directly transferred network could be reached through training with hardware in the loop, compensating for remaining imperfections. Since calibration data can be generated once and then be re-used for multiple networks, calibration can still prove valuable compared to task-specific training.

Compared to the same network evaluated in software, we reached state-of-the-art classification performance on the MNIST dataset. Shortcomings of the current hardware generation result in a reduced multiplication throughput and therefore far from optimal energy efficiency. The upcoming revision of the system addresses all the underlying issues and promises efficiencies and runtimes improved by a factor of 100–1000.

5 Contributions

J. Weis developed calibration routines, conducted the presented experiments and evaluations and wrote the initial manuscript. P. Spilger is the main developer of the software extensions providing support for BrainScaleS’ non-spiking operation mode. S. Billaudelle designed neuron and synapse driver circuits and contributed to commissioning of the chip. Y. Stradmann contributed to hardware design and commissioning and gave conceptual advice. A. Emmel contributed to experiment code. E. Müller is the lead developer and architect of the BrainScaleS-2 software stack. C. Mauch and O. Breitwieser contributed to the software architecture and implementation. A. Grübl was responsible for chip assembly and implemented the digital front- and backend. J. Ilmberger contributed to host-side communication infrastructure. V. Karasenko is the main developer of the FPGA firmware and developed the communication infrastructure between FPGA and
ASIC. M. Kleider contributed to FPGA firmware development as well as initial commissioning of the system. K. Schreiber designed and implemented the CADC and the physical ASIC test setup. J. Schemmel is the lead designer and architect of the BrainScaleS-2 neuromorphic system. All authors discussed and contributed to the manuscript.

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