A low-noise and fast transient response LDO design for high-speed SerDes

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Abstract: In order to deal with the special needs of high-speed digital-analog hybrid circuits for power supplies, this article has designed a LDO circuit specifically applied to high-speed SerDes. In the design process, a cross-coupled charge pump was used to increase the swing and reduce power supply noise, and to increase the gain and reduce the area overhead, the design of an asymmetric operational amplifier was introduced. At the same time, the use of the cascode structure is also conducive to the frequency stability of the loop and provides sufficient phase margin for the circuit. Through simulation verification, the low-frequency maximum internal noise of this LDO is only 0.96uV/sqrt(Hz), the transient response time when the load changes from low to high is 38ns, the transient response time from high to low is 84ns, the phase margin is 87.3deg, and the PSRR is 56.8dB.

1. Introduction

Low-dropout regulator (LDO) is the most commonly used power management circuit in integrated circuit systems, providing accurate, stable, and low-noise power supply voltages for high-performance digital circuits or digital-analog hybrid circuits [1]. For example, digital modules in high-performance circuit systems such as the high-speed SerDes interface usually have extremely high requirements for power supply, while LDOs have low power consumption, strong load capacity, low noise, and simple structure. These characteristics better meet the needs of high-performance circuit systems. Serializer-Deserializer(SerDes) is a physical interface that implements high-speed serial transmission protocols. SerDes is a digital-analog hybrid integrated circuit, which can be roughly divided into three parts according to large functional modules: transmitter, receiver, and clock circuit [2]. Both the PLL at the sending end and the CDR at the receiving end have the participation of high-speed clocks. In actual engineering applications, it is found that power fluctuations have the most significant impact on the clock-related structure and are most likely to cause system errors [3]. The LDO in the high-speed digital-analog hybrid circuit no longer blindly pursues high gain and high load capacity, but focuses...
more on the comprehensive requirements of circuit bandwidth, noise and transient response. Therefore, it is necessary to customize the design of a LDO circuit that matches the performance according to the actual working conditions of the high-speed module involved in the clock in the SerDes circuit. Starting from the basic principles of high-speed SerDes, this paper designs a LDO circuit based on the full study of the working characteristics of the high-speed clock module CDR at the receiving end to meet the circuit’s requirements to power supply for low noise, high speed and strong stability.

2. LDO circuit design

The basic structure of the linear regulator is shown in the figure below, which mainly includes: error amplifier, power tube, feedback network, bandgap reference circuit and auxiliary circuit.

![Figure 1. LDO circuit structure](image)

The operation principle of the LDO circuit is as follows: When the load current changes, because the output impedance is not infinite, the output voltage will fluctuate overshoot or undershoot, and the feedback voltage after the feedback network and the reference voltage will appear differential mode, and the operational amplifier will amplify. After this error, the voltage is output to the gate of the power transistor, and the load capacity of the power transistor is adjusted (or understood as adjusting the turn-on voltage of the power transistor) and the circuit returns to stability. The expression of the static operating point of the LDO is as follows (\(A_{\text{error amp}}\) is the error amplifier gain, \(A_{\text{power MOS}}\) is the power tube gain):

\[
V_{\text{out}} = V_{\text{ref}} \left( \frac{R_1 + 1}{R_2} \right) A_{\text{error amp}} \cdot A_{\text{power MOS}} + 1 = V_{\text{ref}} \left( \frac{R_1 + 1}{R_2 A_{\text{error amp}} \cdot A_{\text{power MOS}} + 1} \right)^{-1} \tag{1}
\]

2.1. Asymmetric operational amplifier

When designing the error amplifier, considering power consumption and area overhead, an asymmetric op amp design is adopted. As shown in Figure 2.21, the size of the transistor on the right is twice that of the transistor on the left. Assuming that the DC potentials of the gates of M1 and M2 are equal, the tail current source when symmetrical is \(I_{SS}\). It is important to note that in order to compare the difference between symmetrical design and asymmetrical design, the gain of the two circuits should be calculated under the condition of equal power consumption, so that the variables can be unified, and only the area of the circuit changes.
For this cascode folding op amp, \( V_{GS1} = V_{GS2} \), \( I_{D2} = 2I_{D1} = \frac{4}{3}I_{SS} \). According to the formula for calculating the on-resistance of the transistor and the formula for calculating the transconductance in the saturation region:

\[
\begin{align*}
    r_o &= (\lambda I_D)^{-1} \quad \text{and} \quad g_m = [2\mu_n C_{OX} \left( \frac{W}{L} \right) I_D]^{1/2}, \\

    r_{o,2W} &= \frac{3}{4} r_o \quad \text{and} \quad g_{m,2W} = \left( \frac{8}{3} \right)^{1/2} g_m,
\end{align*}
\]

the gain of the asymmetric op amp is calculated:

\[
\begin{align*}
    g_{m1} &= \left[ 2\mu_n C_{OX} \left( \frac{W_1}{L_1} \right) 2I_{SS}/3 \right]^{1/2}, \\
    g_{m2} &= \left[ 2\mu_n C_{OX} \left( \frac{2W_1}{L_1} \right) 4I_{SS}/3 \right]^{1/2}, \\
    A_v &= \left( \frac{8}{3} \right)^{1/2} g_{m2} \left( \left( \frac{8}{3} \right)^{1/2} (g_{m8} + g_{m8b}) \right) \frac{3}{4} g_{o8} \frac{3}{4} (r_{o4} || r_{o2}) || r_{o6}, \\
    |A_v| &\approx g_{m2} \left( \left( g_{m8} + g_{m8b} \right) r_{o8} \left( r_{o4} || r_{o2} \right) || r_{o6} \right),
\end{align*}
\]

The gain of the operational amplifier of the symmetrical structure is:

\[
    |A_v| \approx g_{m2} \left( \left( g_{m8} + g_{m8b} \right) r_{o8} \left( r_{o4} || r_{o2} \right) || r_{o6} \right),
\]

Approximately calculating the above formula can be obtained, in the case of the same power consumption of the circuit, the use of asymmetric design increases the circuit gain to a certain extent. Not only that, a larger size transistor can reduce the noise impact caused by mismatch [4], making the LDO more suitable for use in high-speed circuits.

### 2.2. Cross-coupled charge pump

When designing the operational amplifier, it is found that the use of a folded cascode operational amplifier structure combined with Miller capacitance compensation will be very beneficial to the stability of the loop. However, the cascode structure also brings many disadvantages while providing high output impedance. The most prominent problem is that the cascode structure limits the output swing of the second-stage common gate of the operational amplifier. To solve this problem, a charge pump structure is introduced here to generate a voltage source higher than the power supply voltage,
and to supply power to the second stage of the operational amplifier, which will help increase the output swing of the operational amplifier and suppress the power supply noise.

![Cross-coupled charge pump diagram]

**Figure 4. Cross-coupled charge pump**

Here we use the two-pole cross-coupled charge pump shown in Figure 2.17. The charge pump is controlled by a pair of non-overlapping clocks (clk_p and clk_m). The non-overlapping clocks have dead time, so that the through current can be effectively reduced during operation, and the voltage gain and power charging efficiency can be improved. The cross-coupled charge pump can output a voltage higher than the input voltage value for a full cycle, and the output voltage ripple of the cross-coupled charge pump is smaller than the power supply voltage[5].

When the second stage of the error amplifier is not powered by a charge pump, the gain expressions of the first and second stages are respectively $g_{m12}(r_{012}|r_{034})$ and $g_{m78}(r_{056}|r_{078})$, and the transconductance expressions of the M7 and M8 transistors are $g_{m78} = \left(2\mu_n C_{OX} W L I_D\right)^{1/2}$. Using the half-side equivalent circuit of the cascode op amp in Figure 2.18(b) to calculate the gain:

$$|A_v| \approx g_m\{(g_m + g_m b) r_{08}(r_{04}|r_{02})||r_{06}\}$$

(5)

After using the charge pump structure, because the output voltage of the charge pump is higher than the original power supply voltage, the current of the second stage of the error amplifier increases, the second stage transconductance increases, and the gain of the entire amplifier also increases. The output swing is:

$$|V_{max,range}| = 2[V_{dd, pump} - (V_{OD4} + V_{OD6} + V_{OD8})]$$

(6)

$V_{ODj}$ represents the overdrive voltage of the Mj tube. Compared with the amplifier without a charge pump structure, $V_{dd, pump} > V_{dd}$, ignoring the body effect, and when the overdrive voltage of the transistor remains unchanged, the swing of the output node increases. Not only that, due to the addition of the charge pump, the current of the second stage of the op amp will increase, the transconductance will also increase, and the gain and speed will be improved.
3. Performance simulation

3.1. PSRR and frequency response

Figure 2.23 is a Bode plot of the power supply rejection ratio, gain and phase of the LDO at a temperature of 25°C, a power supply voltage of 1.8V, and a process angle of πt. The system is simplified to a two-pole system. After the primary and secondary poles of the LDO loop are compensated, the other poles of the circuit are pushed to higher frequencies. The LDO loop has a gain of 46.3dB at low frequencies and a phase margin of 87.3deg to ensure that the loop is sufficiently stable. The power supply rejection ratio has a gain of 56.8dB at low frequencies. The inflection point of the power supply rejection ratio basically coincides with the main pole. The PSRR gains a minimum of 18.7dB when the frequency reaches 125MHz.

Figure 6. PSRR, gain and phase Bode plot

Figure 7. Line regulation under different loads

3.2. line regulation and load regulation

For the simulation of the line regulation, the power supply voltage variation range is ±10% of the standard voltage under the DC condition. The reference voltage is an ideal reference voltage of 0.31V, and the load changes from no load to full load, and the change curve of the LDO output voltage is
drawn. After calculation, the LDO circuit has a line regulation of 2.11mV/V at no load, and 1.46mV/V at full load.

The load regulation reflects the change of the output voltage when the load of the LDO circuit changes. Under the condition that other simulation conditions remain unchanged, set the LDO load to change from no load to full load, and draw the output voltage change curve. When the load current decreases from 3mA to close to 0mA (considering the leakage current of the load circuit, the current is slightly greater than 0mA under no-load conditions), the output voltage increases by about 0.86mV, and the calculated load regulation rate is 0.289mV/mA.

Figure 8. Load regulation

Figure 9. Noise density spectrum

3.3. Internal noise and transient response

Noise analysis is based on the linearization model of the circuit. In the simulation, the LDO circuit is regarded as a dual-port network with only one input and one output. During the simulation, the outputs of multiple uncorrelated noise sources are accumulated to obtain the power noise spectrum at the output. The output noise spectrum curve of the LDO circuit is as follows. The maximum noise at low frequencies is 9.62 uV/sqrt(Hz). At this time, the dominant noise is 1/f noise, while at high frequencies, the thermal noise of transistors and resistors is dominant.

Figure 10. Transient response curve
The transient response of the LDO is also another important indicator reflecting the performance of the LDO circuit in the project. This indicator is mainly used to measure the stability of the LDO circuit when the load changes rapidly. The simulation method used in this project is: within 1ns, the LDO load is switched from the no-load state to the full-load state (and from the full-load state to the no-load state), and the time required for the output voltage to recover to \( \pm 1\% \) of the rated value is calculated. This can reflect the stability of the LDO circuit during startup and shutdown to a certain extent, as well as the stability of the circuit when the load is switched rapidly during the working process. The simulation results are shown in Figure 2.13 below. The black curve is the size of the load current. The leakage current at no load is set to 10uA, and the load current at full load is 2.5mA. The load current is switched at 3us and 8us respectively, and a load switch of 2.5mA to 1mA is added at 6-7us to simulate the load switch when the LDO circuit is actually working normally. The switching time of each load current above is 1ns. The blue curve is the change of the output voltage. It can be observed that the amplitude of the output voltage fluctuation caused by the first and last switching is significantly larger than the two switchings in the middle due to the different amplitudes of the load current switching. The lower left and lower right curves are the waveform enlarged diagrams of the output voltage curve during the first and last switching. It took 38.4ns for the output voltage to recover after the first load switching, and 84.1ns for the output voltage to recover after the last load switching.

### Table 1. LDO performance

| Load current (mA) | PSRR (dB) | PSRR inflection point (KHz) | Phase margin (deg) | Load regulation (mV/mA) | Line regulation (mV/V) | Transient response time (ns) | Maximum low frequency noise (uV/\sqrt{Hz}) |
|------------------|----------|-----------------------------|-------------------|-------------------------|------------------------|-----------------------------|----------------------------------|
| 3.5              | -56.8    | 480                         | 87.3              | 0.29                    | 1.46                   | 38/84                       | 0.96                             |

### 4. Conclusion

This article designs an LDO applied to high-speed SerDes circuits. In order to cope with the special requirements of high-speed digital-analog hybrid circuits for low internal noise, high-speed transients, and high stability, a charge pump structure and asymmetric operational amplifier design methods are adopted. Through simulation verification, the LDO has fast load transient response, low internal noise and sufficient phase margin.

### References

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