A 10-bit 1.2GS/s 45mW time-Interleaved SAR ADC with background calibration

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Abstract: A 10-bit 1.2GS/s power efficient time-interleaved successive-approximation-register (SAR) analog-to-digital converter (ADC) is present in this paper. Substrate bias effect depression and output resistance stabilization techniques are provided to enhance the linearity of input buffer. Further, meta-stability restrained trigger comparator is used to enhance the ENOB (effective number of bits) of SAR ADC. Additionally, a digital background calibration technique is proposed to suppress the inter-channel gain, offset and timing skew mismatches. To demonstrate the proposed techniques, a design of time-interleaved SAR ADC is fabricated in 55-nm CMOS technology, consuming 45mW from 1.2V power supply with a SNDR of 50dB and SFDR of 60dB. The proposed ADC core occupies an active area of 0.84mm\textsuperscript{2}, and the corresponding FoM is 145 fJ/conversion-step with Nyquist rate.

Keywords: Analog-to-digital converter (ADC), Time-interleaved ADC, successive-approximation-register (SAR) ADC, Meta-stability restrained, High-linearity, Background calibration.

Classification: Analog integrated circuits

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1 Introduction

With the feature sizes of CMOS devices scaled down, medium resolution (8 to 10b) successive approximation register (SAR) analog-to-digital converters (ADCs) have been able to achieve sampling rates over 100MS/s with excellent power efficiency and small area. In the structure of time-interleaved, the effective conversion rate can be increased by N times with N channels. Because of the alternate sampling of every channel, input buffer is required to provide high linearity input signal to every channel in [1] and [2]. However, the feedback loop
decreases the speed of buffer in [1] and the complicated structure in [2] increases power consumption. Further, the performance of high-speed SAR ADC is restricted by meta-stability of high-speed dynamic comparator. Time-out detection is adopted [3] to prevent the error caused by meta-stability. But the occurred meta-stability possibly leads to conversion errors when the input is small. Tow comparators work alternately to prolong the compare time in [4] and meta-stability of comparators is depressed. However, the offset of comparators should be calibrated. Meta-stability immunity technique is provided in [5], the complicated logic in the signal path increases the delay of comparator when meta-stability does not occur. The performance of time-interleaved ADC is influenced by inter-channel non-ideal factors such as offset, gain error and timing skew mismatch. Thanks to their digital-friendly compatibility, SAR ADCs are superior in aspects of power efficiency and are highly scalable to an advanced CMOS technology, several calibration techniques are provided in [1] and [6]-[11] to correct the non-ideal errors produced by channel mismatches in time-interleaved SAR ADC (TI SAR ADC).

In this work, with voltage compensation methods for input buffer, a high-linearity input buffer with substrate bias effect depression and output resistance stabilization techniques is realized to increase the linearity of input signal. Moreover, a short delay meta-stability restrained technique is provided for high speed comparator to increase the speed of single channel. Finally, digital background calibration technique is provided to revise the errors of inter-channels.

2 System Architecture

The simplified architecture of proposed TI ADC is presented in Fig.1(a). The TI ADC mainly includes input buffer, clock generation block, eight identical 10-bit SAR ADCs in parallel and digital calibration block. For high-linearity input signal, an input buffer is used before the eight parallel SAR ADCs. The signal through the buffer is applied to the eight sub-ADC in parallel. We proposed a background calibration technique for sub-ADC mismatch calibration. The timing mismatches between sub-ADCs are corrected using a mixed-signal feedback. All calculations are performed in the digital domain and the actual timing correction is done in the analog domain by fine-tuning the edges of the sampling clocks Clki (i=0,1,…,6,7). The 150MHz sampling rate single channel binary SAR ADC is exhibited in Fig.1(b). For a single-channel high-speed SAR ADC, the performance of the structure is usually influenced by DAC settling, offset, capacitor mismatch and meta-stability of comparator. With the structure of constant common-mode switching scheme, the constant common-mode voltage will produce a small statistic offset for dynamic comparator and exhibit good common-mode rejection to suppress nonlinearity and better dynamic offset compared to monotonic switching scheme. The mismatch of capacitor could be satisfied with capacitance of 0.8fF by using MOM capacitor for SAR ADCs with 10b resolution or less. Assuming the positive and negative references are 1.2V and 0V, respectively, the LSB voltage of the SAR ADC is about 2.1mV for 10b resolution. It indicates that the meta-stability of comparator will occur if differential input signal is smaller.
than 1LSB and Vop and Von are the same voltage in digital domain. As a result, meta-stability restrained technique is provided to depress the meta-stability of comparator. The time diagram of TI ADC is given in Fig.1(c). Each channel operating at the overall sampling rate divided by eight with the duty cycle of about 11%. In this way, the same impedance is present at the input of every ADC for every sampling phase by non-overlap clocks. The interleaved system requires eight 150MHz clock phases, each having a duty cycle of about 11% so as to allow 0.73ns for sampling and 6ns for conversion in each sub-ADC channel.

3 Detail Design Implementation

3.1 High-linearity input buffer

A single-ended version of the input buffer is exhibited in Fig. 2 for simplicity, a differential structure is implemented. VIP and VIN are the input differential signals, VB is a bias voltage, R is a resistor, SW is the sample switch, C_P and C_S are
coupling and sampling capacitor, respectively. In Fig. 2, we provide two techniques to improve the linearity of the input buffer. Firstly, the substrate bias effect depression technique is produced by NMOS M3 and M4. The area of M3 and M4 are scaling down compared to M1 and M2 to save power consumption. The voltage of VP is the same with VOP, the source of M3 is connected to substrate of M1. It indicates that the substrate voltage of M1 follows its source voltage. As a result, the substrate bias effect is depressed and the total transconductance of M1 is more stable. Considering the voltage drop of source follower structure, M1, M2, M3 and M4 are 1.8V devices and power supply of the buffer is 1.8V. The area proportions of M1/M3 and M2/M4 are both set to 32/1. For the sake of increasing the output resistance of M2, the channel length of M2 should be increased. The W/L of M1 and M2 are 64µM/0.26µM and 128µM/0.7µM, respectively. Secondly, the output resistance of M2 is changeable because of the channel length modulation effect. We could note that the change of VIN is opposite to VIP, so the change of VG is opposite to the change of VOP. Thanks to the RC structure R and C_P, the current change of M2 influenced by VOP could be compensated by the change of VG. If we set proper parameters in the proposed buffer, the output resistance of M2 is more stable. Based on the simulation, the values of R and C_P are about 12Khom and 300fF, respectively. Consequently, a stable transconductance of M1 and a stable output resistance of M2 provide changeless output resistance for the proposed input buffer and the linearity of input buffer is improved. In this design, the common mode voltage and the input range of the input buffer are 1.2V and 0.7V, respectively.

The SFDR comparisons between proposed and conventional structure are exhibited in Fig. 3. In Fig. 3(a), the improvement of SFDR for proposed structure is about 5dB compared with conventional structure. In Fig. 3(b), without substrate bias effect depression and output resistance stabilization techniques, the deterioration of SFDR for conventional structure is more obvious compared to proposed structure. Especially, as the increasing of input Vp-p, the improvement of proposed compensation technique becomes more evident. In the condition of sampling frequency is 1.2GHz, input frequency is about 587MHz and input Vp-p is 0.7V, after Monte Carlo analysis of 200 times, the mean SFDR of sample and

![Fig. 2. The proposed input buffer](image-url)
hold circuit is 65.68dB with the change of process and mismatch in 60℃, the 3σ value is 0.45dB. In addition, the mean SFDRs are 62.3dB and 65.7dB in 125℃ and -40℃, the 3σ values are 0.78dB and 0.52dB, respectively.

3.2 Meta-stability restrained comparator

Meta-stability restrained high-speed comparator is introduced in Fig. 4, based on the high-speed and low-power dynamic comparator in [12], we proposed a meta-stability restrained technique. The proposed meta-stability restrained technique includes a rising edge logic delay block dly, D flip-flop (DFF), pull-down switch M11 and pull-up switch M12 outside the signal path compared to [5]. A rising edge logic delay block dly is added in the comparator, the output rising edge of dly Clk2d is the delay of Clk2. For the DFF, output port Q is reset to 0 when RST port is 0, otherwise, the output port Q is updated by D when CP is 1. The areas of M12 and M11 are designed carefully to ensure the similar parasitical capacitance in Tn and Tp, respectively. In addition, the offset provided by different parasitical capacitance of M12 and M11 is a linearity error. As a result, the dynamic characters of ADC are not influenced by the offset produced by different parasitical capacitances of M11 and M12.

Firstly, if meta-stability of comparator does not occur, the compare time of comparator is shorter than the delay of dly, the meta-stability restrained technique
is off, K1 and its opposite signal K1N keep 0 and 1, respectively. M12 and M11 are both off. If meta-stability of comparator occurs, it indicates that the compare time of comparator is longer than the delay of dly. Consequently, the meta-stability restrained technique is on, DFF is triggered by Clk2d, K1 and its opposite signal K1N are set to 1 and 0, respectively. M12 and M11 are both on, the weak balance of Tp and Tn are broken, Dp and Dn are set to 1 and 0 quickly. Hence, the meta-stability of the proposed comparator is eliminated. We should notice that the structure of meta-stability restrained is not on the path of signal and less delay is produced compared to [5]. Secondly, switches S1 and S1N are proposed to select the gate voltages of rest PMOS M6 and M9. In the reset phase, the voltages of Tp and Tn are both reset to VDD. In the compare phase, the input signals of comparator are also added to the gate of PMOS M6 and M9. Because of the different pull up speed of M6 and M9 in the compare phase, the different gate voltages of M6 and M9 increase the speed of positive feedback of the comparator. Consequently, the positive feedback of the proposed comparator is enhanced and the conversion speed of the comparator is increased. In order to increase the speed of comparator, the latching point in [12] is connected to the drain of input NMOS compared to [13]. Feedback technique is proposed in [12] to decrease the power consumption compared to [14]. Based on the structure in [12], we add another signal path from M6 and M9 to improve the compare speed in this design. The performance comparisons in terms of speed and power consumption are exhibited in Fig. 5(a) and Fig. 5(b), respectively. It can be seen that the proposed comparator

![Fig. 5. Performance comparisons. (a)ΔVin versus delay. (b)Vcm versus power](image)

![Fig. 6. Tp/Tn comparison without meta-stability (a) and with meta-stability (b)](image)
provides lower power consumption and shorter delay compared with previous structures.

The $T_p/T_n$ comparison without and with meta-stability are depicted in Fig. 6. In compare phase, if $T_p$ and $T_n$ become different voltages in digital domain before the delay of $dly$, DFF will not be triggered, it implies that comparator is working without meta-stability. Otherwise, if $T_p$ and $T_n$ keep the same voltage in digital domain after the delay of $dly$, that means comparator is working with meta-stability, DFF will be triggered and $M_{12}$ and $M_{11}$ are both on, $T_p/T_n$ will be pulled up or pulled down to 1 and 0 quickly.

3.3 Digital background calibration technique

Fig. 7 shows the block diagram of clock generation for the prototype. The interleaved system requires eight 150MHz clock phases, each having a duty cycle of about 11% so as to allow 610ps for sampling and 6.09ns for conversion in each sub-ADC channel. As shown in Fig.7, a differential clock buffer is used to match impedance and clock reshaping with no additional jitter issue. Then the 8 Divider block produce 8 no-overlap clock $Clk_{(0)}$ to $Clk_{(7)}$. To minimize the systematic mismatches in the clock path, an H-tree block is used to route clocks. The programmable delay block in Fig. 7 adjusts the output of H-tree routing by changing the capacitive load. Consequently, the timing of divided SAR clocks could correct the timing skew among the SAR ADCs. The calibration of offset and gain errors were realized by adding and multiplying correction parameters in digital domain that $x_i(n) = (1 + \Delta_{yo}) \cdot y_i(n) + \Delta_{yo}$, $y_i(n)$ is the direct output of sub-ADC channel. The correction parameters were updated after every N cycles of sub-ADC.

![Fig. 7. Block diagram of clock generation.](image)

The calibration of time skew is realized by adjust the delay of sub-ADC clock that inserted by a digitally controlled delay cell, which is proportion to the time skew correction parameter. As every time we update the correction parameters, the grades of the error loss function would be smaller than before, we also change the step $\mu_{\Delta o}$, $\mu_{\Delta g}$, $\mu_{\Delta t}$ dynamically during parameter updating, that after tens of iterations, it would be settle.

The offset, gain error and time skew mismatch of inter-channel are corrected after ADC begins to work. We could assume the input signal is wide-sense cyclostationary stationary (WSCS), thus, statistic blind estimation methods could
be used for error estimation by minimize the error loss function. The method to evaluate the offset errors between channels is the mean value of the output from each sub-ADC corresponds to the each offset errors. The offset error loss function could be approximately expressed as:

\[ E_{\text{offset}} = \sum_{i=1}^{7} \frac{1}{N} \sum_{n=0}^{N-1} (x_i(n) - x_0(n))^2 \]  

(1)

If we suppose no offset error is exist, the method for gain error evaluation is from the variance of output for every sub-ADC with respective gain errors. The gain error loss function could be approximately expressed as:

\[ E_{\text{gain}} = \sum_{i=1}^{7} \frac{1}{N} \sum_{n=0}^{N-1} (x_i(n)^2 - x_0(n)^2)^2 \]  

(2)

Because the loss function is convex, it provides more robust for numerical minimization. We could remove the offset and gain errors by solve the \( \min \{ E_{\text{offset}}, E_{\text{gain}} \} \).

We suppose the input signal is cyclostationary, if we define \( R(n,n') = E[x(n)x(n')] \), thus, \( R(n,n') = R(n+8,n'+8) \). Suppose offset and gain errors among sub-ADCs are eliminated, we could find that \( R(n,n') = R(n+k,n'+k) \), \( k = 1, \ldots, 7 \). For the system, the input signal is band limited to the Nyquist frequency, the correlation function \( R(t) \) is nearly monotonic near \( t=T \).

The time loss function can be defined as:

\[ E_{\Delta t} = \sum_{u,v} (R(u,u+1) - R(v,v+1))^2 \]  

(3)

We could get an evaluation of the parameters by minimizing the loss function, but it may be not convergence for the actual error value. In order to simplify the evaluation process and make it converge to the right value. We define:

\[ E_{\Delta t} = [e_{0,1}, e_{1,1}, e_{2,1}, e_{3,1}, e_{0,2}, e_{1,2}, e_{0,3}] \]  

(4)

\[ e_{i,j} = R(i,i+1) - R(8/2^{i-1} - i - 1, 8/2^{j-1} - i) \]  

(5)

We first minimize \( E_{\Delta t}(k) \), after the convergence, then started to minimize \( E_{\Delta t}(k + 1) \), \( E_{\Delta t} \) could be minimized step by step.

Adding and multiplying correction parameters in digital domain could eliminate offset and gain errors. A stochastic gradient minimization algorithm is used to update the correction parameters \( \Delta_o^k \) and \( \Delta_g^k \).

\[ \Delta_o^{k+1} = \Delta_o^k + \mu_{\Delta o} \cdot \frac{\nabla E_{\Delta o}}{\max |\nabla E_{\Delta o}|} \]  

(6)

\[ \Delta_g^{k+1} = \Delta_g^k + \mu_{\Delta g} \cdot \frac{\nabla E_{\Delta g}}{\max |\nabla E_{\Delta g}|} \]  

(7)
An analog method is used to realize low power consumption and low complexity. The time skew mismatch calibration parameter $\Delta_{\tau}^i$ is transformed through an encoder to control digitally controlled delay cell, the time skew mismatch among sub-channels could be eliminated. We could update the estimation parameters from the iteration below:

\begin{align*}
UP_{\Delta\tau}^i &= e^i_{\Delta\tau} \cdot \mu_{\Delta\tau} \cdot \text{sign}(E_{\Delta\tau}(8-i)), \quad i = 1, 2, 4 \\
UP_{\Delta\tau}^i &= e^i_{\Delta\tau} \cdot \mu_{\Delta\tau} \cdot \text{sign}(E_{\Delta\tau}(8-i)), \quad i = 3 \\
UP_{\Delta\tau}^i &= e^i_{\Delta\tau} \cdot \mu_{\Delta\tau} \cdot \text{sign}(E_{\Delta\tau}(8-i)) - UP_{\Delta\tau}(8-i), \quad i = 5, 6, 7 \\
\Delta_{\tau}^{k+1} &= \Delta_{\tau}^k + UP_{\Delta\tau}^k 
\end{align*}

Where $e^1_{\Delta\tau} = 1$ denote $E_{\Delta\tau}(8-i-1)$ has already minimized. Otherwise, $e^1_{\Delta\tau} = 0$.

4 Measurement Results and Discussions

Fig. 8. Die photo of the TI ADC

Fig. 9. Measured DNL and INL
The proposed SAR ADC is designed in 1P9M 55nm CMOS technology. The die micrograph of proposed SAR ADC is shown in Fig. 8. The core area is 1.4mm $\times$ 0.6mm and the area of the die is 2.5mm $\times$ 1.9mm. The measurements of differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 9. The peak DNL and INL are -0.77/+0.52 LSB and -1.2/+1.1 LSB. The measurement results with 15MHz input before and after calibration are shown in Fig. 10(a) and Fig. 10(b), respectively. Before calibration, the spurious free dynamic range (SFDR) is 65dB, the signal to noise and distortion ratio (SNDR) is about 48dB, which is limited by the 3rd-order harmonic, the spurs course by sampling timing skews (S1) and the spurs course by offsets of sub-ADCs (S2). After calibration, the SFDR is about 66dB and the SNDR is improved from 48dB to 54dB. It implies that the 3rd-order harmonic (H3) is nearly improved after calibration, thanks to the calibration of sampling timing skew and offset of sub-ADCs, the improvement of SNDR is obviously. Fig. 11 shows the measured spectrum with 587MHz input. The measurement results before and after calibration are shown in Fig. 11(a) and Fig. 11(b), respectively. Similar with Fig. 10, the 3rd-order harmonic (H3) with high input frequency is not sensitive to calibration. After calibration, H3 is worse than S1 or S2, the SFDR is decided by

![Fig. 10](image1.png)

**Fig. 10.** Measurement output spectrums with 15MHz input before calibration (a) and after calibration (b) with sampling rate 1.2GHz

![Fig. 11](image2.png)

**Fig. 11.** Measurement output spectrums with 587MHz input before calibration (a) and after calibration (b) with sampling rate 1.2GHz
the spurs S1 and S2 are optimized after calibration. With low frequency input, the performance of SAR ADC without calibration is undoubtedly affected by the mismatch of every sub-ADC. Because mismatches among sub-ADCs are more sensitive with the increase of input frequency, the ENOB is improved about 1.3 in Fig. 11. These results show that, with calibration, the ENOB of SAR ADC can increase at least 1b. The total power consumption is about 45mW at 1.2V power supply with operating frequency is about 1.2GHz, the power consumption for each sub-ADC is about 0.8mW, the input buffer consume about 2mW and 36.6mW for the digital calibration block. For every sub-ADC, The comparator and DAC occupy 46% and 28% power consumption, respectively. In addition, the SAR logic takes up 20% power consumption and the proportion of other analog part is about 6%.

The performance comparison with other related works is listed in Table I. The proposed SAR ADC achieves a small area of 0.84mm² with on-chip background calibration and a figure-of-merit of 145 fJ/conversion step with Nyquist rate.

| Reference | [6] | [10] | [11] | This work |
|-----------|-----|------|------|----------|
| Architecture | TI-SAR | TI-FLASH/SAR | TI-SAR | TI-SAR |
| Technology (nm) | 28 | 65 | 40 | 55 |
| Resolution | 10 | 10 | 9 | 10 |
| Supply (V) | 1 | 1 | 1 | 1.2 |
| Sampling rate (GS/s) | 5 | 1 | 1.6 | 1.2 |
| SNDR (dB) | 42 | 51.4 | 48 | 50 |
| SFDR (dB) | 54 | 63 | 62 | 60 |
| Power (mW) | 76 | 18.9 | 93 | 45 |
| FoM (fJ/conv) | 165 | 62.3 | 283 | 145 |
| Area (mm²) | 0.57 | 0.78 | 0.83 | 0.84 |

4 Conclusions

A 10-bit 1.2GS/s time-interleaved SAR ADC with high-linearity input buffer, comparator meta-stability restrained technique and on-chip background digital calibration is proposed. The TI-ADC gives a >50dB SNDR and achieves SFDR >60dB with Nyquist rate. As a result, the techniques proposed in the work increase the performance of high-speed time-interleaved SAR ADCs.

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