Reproducible Non-Volatile Multi-State Storage and Emulation of Synaptic Plasticity Based on a Copper-Nanoparticle-Embedded HfO$_x$/ZnO Bilayer with Ultralow-Switching Current and Ideal Data Retention

Shuai Chen $^{1,2}$, Hao Chen $^2$ and Yunfeng Lai $^{1,2, *}$

$^1$ Fujian Science & Technology Innovation Laboratory for Optoelectronic Information of China, Fuzhou 350108, China
$^2$ School of Physics and Information Engineering, Fuzhou University, Fuzhou 350108, China
$^*$ Correspondence: yunfeng.lai@fzu.edu.cn

Abstract: The multilevel properties of a memristor are significant for applications in non-volatile multi-state storage and electronic synapses. However, the reproducibility and stability of the intermediate resistance states are still challenging. A stacked HfO$_x$/ZnO bilayer embedded with copper nanoparticles was thus proposed to investigate its multilevel properties and to emulate synaptic plasticity. The proposed memristor operated at the microampere level, which was ascribed to the barrier at the HfO$_x$/ZnO interface suppressing the operational current. Compared with the stacked HfO$_x$/ZnO bilayer without nanoparticles, the proposed memristor had a larger ON/OFF resistance ratio ($\sim$330), smaller operational voltages (absolute value $<$ 3.5 V) and improved cycle-to-cycle reproducibility. The proposed memristor also exhibited four reproducible non-volatile resistance states, which were stable and well retained for at least $\sim$1 year at 85 $^\circ$C (or $\sim$10 years at 70 $^\circ$C), while for the HfO$_x$/ZnO bilayer without copper nanoparticles, the minimum retention time of its multiple resistance states was $\sim$9 days at 85 $^\circ$C (or $\sim$67 days at 70 $^\circ$C). Additionally, the proposed memristor was capable of implementing short-term and long-term synaptic plasticities.

Keywords: resistive switching; memristor; electronic synapse; oxides

1. Introduction

Memristors exhibiting multilevel resistive switching properties have attracted much attention from industries and academic communities due to their potential applications in non-volatile multi-state storage [1], reservoir computing [2], neuromorphic computing and in-memory computing [3,4]. The three-dimensional architecture of memristors has been considered as a hardware basis to fulfill the requirements of the aforementioned applications [5,6]. Embedded memristors might possess low power consumption and the so-called ON/OFF ratio of high-resistance states (HRS) to low resistance states (LRS) should be extended to accommodate as many storage states as possible. In addition, memristors should exhibit reproducible resistive switching behavior as a guarantee of reliable functionalities [7].

Several techniques have been attempted to control the dynamic evolution of resistance, which is helpful in achieving multi-state storage and simulating synaptic behavior [8]. Integrating multiple resistive switching mechanisms, such as ferroelectric [9], resistive and magnetic behaviors [10,11], into the same device seems to be an effective strategy. Through the modification of the device structure [12–14], the embedment of nanoparticles into the storage medium [15–18], the optimization of the electrical stimulus [19], element doping and interface modification [20,21], multi-state storage and synaptic plasticity could also be attained by precisely controlling the dynamic growth (or dissolution) of the conductive...
filaments (CFs) [22–26]. Stacked layers as a storage medium improve the stability and reliability of resistive switching to favor multi-state storage, but its lower ON/OFF resistance ratio is normally hard when accommodating many more intermediate resistance states. Doping metal nanoparticles into a storage medium facilitates the formation of CFs and usually extends the ON/OFF resistance ratio, but the relatively large operational current (~mA) does not serve its application in low-power neuromorphic computing [15,16,26,27]. Combining bilayers embedded with a nanostructure seems to be a feasible way to have a large ON/OFF resistance ratio as well as a low power consumption [28,29]. Niu Y combined an SiO$_2$ limiting layer with MoS$_2$ quantum dots (QDs) and inserted them into Al$_2$O$_3$/Pt. The SiO$_2$ as a limiting layer provided a small fracture area in Al$_2$O$_3$ for reducing the power consumption. The MoS$_2$ QDs positioned CFs to enhance the reproducibility. Sakellaropoulos D inserted Pt nanocrystals between the top electrode and the TiO$_2$−$x$/TiO$_2$−$y$ bilayer, in which the TiO$_2$−$y$ layer with a lower oxygen content acted as series resistance to limit the current and the Pt nanocrystals also positioned CFs. However, the reproducibility and stability of intermediate resistance states are still challenging [19,26,30] since their retention at high temperature needs further improvements. New approaches are still worth investigation. Hafnium oxide and zinc oxide are compatible with CMOS processing and exhibit excellent resistive switching properties [13,19,21]. Our previous work also indicates that the resistance of a HfO$_x$/ZnO bilayer was closely associated with the barrier on the Hf$_x$O/ZnO interface [31], which suggests the possibility of multilevel properties. Additionally, the HfO$_x$ RRAM doped with Cu presented a multilevel non-volatile storage capability [32], which further provides another clue for multilevel properties. In order to combine an interface barrier to suppress the current and a nanostructure to position conductive pathways, we therefore designed a HfO$_x$/ZnO double-layer embedded with copper nanoparticles and investigated its multi-state storage properties and conducted a simulation of its synaptic plasticity.

2. Materials and Methods

A corner-covered ITO/glass substrate was used with ~15 nm sputter-deposited ZnO thin films on the surface to fabricate a HfO$_x$/ZnO double-layer-based memristor. The ~15 nm HfO$_x$ thin films were then sputtered on the ZnO surface, followed by 10 s deposition of thin copper films. Subsequently, the samples were heated with rapid thermal processing at 550 °C for 20 s under a nitrogen atmosphere to form Cu nanoparticles. Finally, the upper ~15 nm HfO$_x$ thin films were deposited on the nanoparticles, followed by patterning a titanium electrode ($\Phi = 200 \mu$m) with a shadow mask to complete the device fabrication. Devices without nanoparticles were also prepared for comparison and marked as S0. Preparation parameters were determined according to our previous works and reference [31,33]. The morphologies of the thermal-processed HfO$_x$ thin films were observed by scanning electron microscopy (SEM) and an atomic force microscope (AFM) as shown in Figure 1. Cu nanoparticles with an average diameter of ~120 nm (Figure 1c) originated from the 10-second-deposited Cu thin films and the corresponding devices were marked as S120. The surface densities of the Cu nanoparticles were $\sim 2.88 \times 10^8$ cm$^{-2}$. Thermal processing drove the Cu thin film to cluster into ellipsoid-shaped nanoparticles with a height of ~30 nm as per the surface profile shown in Figure 1e. The switching properties of the devices were characterized using a semiconductor characterization system (4200-SCS; Keithley, Cleveland, OH, USA) with 0.5 V for reading. Electrical stimuli were applied to the top titanium electrodes with the ITO bottom electrodes grounded, as schematically shown in the inset of Figure 2a. To evaluate the capability of multi-state storage, the devices were set to be at several resistance states by controlling the amplitude of the electrical stimuli. The measurements were performed from room temperature to 200 °C to appraise the data retention and thermal stability of the storage states. The same semiconductor characterization system equipped with a pulse generator and oscilloscope was also used to study the synaptic behavior of the device with the bottom electrode as the post-synaptic location and the other as the pre-synaptic location.
appraise the data retention and thermal stability of the storage states. The same semiconductor characterization system equipped with a pulse generator and oscilloscope was also used to study the synaptic behavior of the device with the bottom electrode as the post-synaptic location and the other as the pre-synaptic location.

Figure 1. SEM images of HfO$_x$ thin films covered (a) without and (b) with copper nanoparticles; (c) diameter distribution of copper nanoparticles; (d) AFM image of the HfO$_x$ thin films covered by nanoparticles with (e) the surface profile along the yellow dotted line in (c).

Figure 2. (a) Current–voltage characteristics of the stacked layers with the inset of schematic diagram of device structure and measurement configuration; (b) ln(I)-V$^{0.5}$ and ln(I/V$^{0.5}$) fittings for the HRS and LRS of device S0; (c) ln(I/V$^2$)-1/V and log(I)-log(V) fittings for the HRS and LRS of device S120. The right inset is the ln(I)-V$^{0.5}$ fitting of the HRS at low electrical field, while the left inset is the LRS resistance vs. device area. (d) Conductance vs. 1/KT for the LRS device with Cu NPs.
3. Results and Discussion

3.1. Bistable Storage Properties

Figure 2a presents the current–voltage (I–V) characteristics of the devices. All the devices exhibited non-volatile bipolar resistive switching properties with operational currents less than 10 µA. The operational voltage decreased with the embedment of copper nanoparticles. To better understand the effects of the copper nanoparticles, the conduction mechanism of the devices was studied. Several physical models have been proposed to explain the conduction mechanisms of the devices. For the device S0 (Figure 2b), a good linear fitting of ln(I) versus $V^{0.5}$ suggested that a Schottky emission mechanism dominated its HRS conduction, while its LRS conduction was governed by the Poole–Frenkel emission theory due to the linear fitting of ln(I/V) versus $V^{0.5}$ [34,35]. The copper nanoparticles changed the conduction mechanisms of the devices (Figure 2c). For the HRS, the linear fitting of ln($I/V^2$)−$1/V$ under a high electric field and the linear fitting of ln(I) versus $V^{0.5}$ under a low electric field suggested that the HRS conduction of the device S120 changed from a Schottky-emission-dominated mechanism to a Fowler–Nordheim tunneling mechanism with the increase in the electric field. The LRS resistance did not show a clear trend with the device area (left inset of Figure 2c) and the linear log(I)−log(V) of its LRS indicated a filament-assisted Ohmic conduction [36]. We then applied the hopping model to the curve and plotted the dependence of the conductance vs. $1/KT$, as shown in Figure 2d, to further obtain insights into the Ohmic conduction. The activation energy for electronic migration ($E_e$) extracted from the curve was $\sim$0.24 eV, which agreed with the literature reports and suggested it was a charge-trap device [37]. Non-metallic oxygen vacancies ($V_{os}$) might be closely associated with the conduction. However, considering the high diffusion coefficient of Cu, the role of metallic copper could not be totally excluded from the conduction.

To further investigate the non-volatile bistable storage properties, the resistances of the HRS and LRS during 100 consecutive switching cycles were studied. As presented in Figure 3a, the HRS resistances of the device S0 gradually decreased during the switching cycles, though its resistances were greater than those of device S120 at the beginning. As for the LRS, the resistances of device S120 were much smaller than those of device S0. As a result, the ON/OFF resistance ratio increased with the addition of the copper nanoparticles from $\sim$20 to $\sim$330 to provide a much larger space to accommodate multiple storage states. To evaluate the reproducibility of the device resistance, the coefficient of variation (CV), defined as the ratio of the standard deviation to the mean, was utilized. The resistance CVs for the HRS and LRS decreases with the addition of the copper nanoparticles, as shown in Figure 3b, suggesting an improved resistance reproducibility with the embedment of copper nanoparticles. To count the operational voltages, the set voltage was defined as the voltage setting the operational current at half of the maximum, while the reset voltage was defined as the voltage dropping the operational current to half of the maximum. We then randomly selected 20 devices from each device category to count the operational voltages. As shown in Figure 3c,d, most of the set voltages and the reset voltages decreased with the embedment of copper nanoparticles with the counts matching a Gaussian distribution (fitting lines in Figure 3c,d). The narrower full-width at half of the maximum (FWHM) for device S120 further suggested the improved uniformity with the addition of copper nanoparticles.
The multilevel resistive switching properties of a memristor indicate several resistance states or conductance states that might be acquired by setting current-compliances ($I_c$) or voltage-compliances ($V_c$). If the conductance states represent synaptic weights, the simulations of synaptic behaviors by the device might be possible. If the resistance states are sustainable, non-volatile multi-state storage might be realized. Therefore, the multilevel resistive switching properties of the devices were then evaluated by setting gradually increasing values of $I_c$. As shown in Figure 4a, the device S0 completed its set process by three rounds with three increased values of $I_c$. We observed that the beginning of the $I$–$V$ curve of each round did not overlap the end of the $I$–$V$ curve of the last round, which indicated that the ending resistance of the last round was probably not stable. Three rounds were also required to complete the reset process with three increased values of $V_c$. Similarly, the $I$–$V$ curves of the successive rounds did not overlap during the reset process, suggesting the possibly instable resistance of the storage states. However, the embedment of copper nanoparticles brought some changes. The beginning of the $I$–$V$ curve of each round well overlapped the end of the $I$–$V$ curve of the last round during the set process and the reset process as shown in Figure 4b, which indicated that the ending resistance of each round might be reserved to favor multi-state storage. The easy identification of storage states is another important factor for multi-state storage, but the ON/OFF resistance ratio of device S0 was much smaller than that of device S120. The identification of multiple storage states in device S0 might not be easy as instable resistance states challenge the effective identification of states with a small ON/OFF resistance ratio (~20), so device S120 might thus be a better candidate for multi-state storage. Therefore, voltage stimuli were applied to device S120 in an initial HRS. Reproducible resistance switching to intermediate resistance states was observed in Figure 4c with acceptable resistance fluctuations, which allowed us to identify four repeatable storage states.

**Figure 3.** (a) The HRS and LRS resistances during 100 consecutive switching cycles with (b) their cumulative frequencies. Counts versus (c) reset voltage and (d) set voltage of devices.
According to which the embedment of Cu nanoparticles, the retention times of the resistance states at lower temperatures were well distinguished during measurement. The resistance of device S0 fluctuated more than that of device S120, and its level 0 and 1 could not be identified after $10^6$ s. To further appraise the sustainability of each resistance state, the accelerated retention test for resistance states under various temperatures was performed, which has been widely accepted to characterize the retention properties of RRAMs in a time-efficient manner. In this test, the retention failure time ($t_{\text{failure}}$) is measured as a function of temperature at elevated temperatures and then extrapolated to lower, nominal operating temperatures [38–40]. For the oxide-based RRAM in this work, the resistance evolution was closely associated with the migration of defects. Therefore, the retention failure process was dominated by Fick diffusion [40,41], which has an Arrhenius temperature dependence, i.e., $D \propto \exp(-E_a/k_B T)$, where $D$ is the diffusivity, $E_a$ is the Fick diffusion activation energy for the migration of defects (e.g., $V_{os}$ and Cu ions in this work), $k_B$ is the Boltzmann constant and $T$ is the temperature. As a result, the $t_{\text{failure}}$ is inversely proportional to $D$ and can be expressed as Arrhenius equation $t_{\text{failure}} \propto \exp(E_a/k_B T)$ [39,42,43]. The $t_{\text{failure}}$ at lower temperatures could be achieved using linear extrapolation from the data measured at high temperatures. In this work, the retention failure time was defined as the time for the abrupt change in resistance as shown in Figure 5c,d. Table 1 lists the retention failure times of resistance states under different temperatures, according to which the embedment of Cu nanoparticles extended the retention failure times of intermediate resistance states at higher temperatures. As shown in Figure 5e,f, we then plotted the mean retention failure time vs. the reciprocal temperature to conclude the data-retention abilities of all the resistance states by using the Arrhenius equation. The retention times of the resistance states at lower temperatures were thus available by the extraction results of the Arrhenius equation. All the resistance states of device S120 could be well kept for >10 years at 70 °C to satisfy practical applications. The HRS (level 0) and LRS (level 3) of device S0 could be kept for more than 600 years at 70 °C, but its intermediate resistance states (level 1 and level 2) could merely be retained for 67 days at 70 °C (or 9 days at 85 °C), which impedes its practical applications. To further analyze the effects of the nanoparticles for data retention, the value of $E_a$ of the storage states was calculated and is listed in Table 2. According to the literature [44,45], the activation energy of the oxygen vacancies in ZnO is ~1.8 eV. The activation energy of the oxygen vacancies in HfO$_2$ is 0.4–2.13 eV, which is closely associated with the composition, density and crystal structure of the material. The lower density inside the CFs could increase the confinement of the oxygen ion diffusion in the CF region and stabilize the CFs. The HRS (level 0) and LRS (level 3) of device S0 had much higher activation energies (1.92 eV and 1.90 eV) to stabilize defect status and sustain a rather long retention time. However, its intermediate resistance states (level 1 and level 2) had much lower activation energies (~1 eV). Compared with the HRS and LRS, the migration of defects
for the intermediate states might destroy the stability of conductive pathways, exhibiting poor retention. Device S120 was on the contrary; the activation energies of the HRS and LRS decreased to 1.65 eV and 1.43 eV, respectively. However, the activation energies of the intermediate states increased through the embedment of copper nanoparticles, which balanced the retention of all the resistance states to the meet basic requirements of practical applications.

![Figure 5.](image-url)

**Figure 5.** Room temperature data retention of four storage states for (a) device S0 and (b) S120; dependence of resistance on time at high temperatures for (c) devices S0 and (d) S120; temperature dependence of retention-failure-time fitting lines following the Arrhenius equations for (e) devices S0 and (f) S120.

**Table 1.** Retention failure times of resistance states.

| States      | Device S0 (s) | Device S120 (s) |
|-------------|---------------|-----------------|
|             | @160 °C | @180 °C | @200 °C | @160 °C | @180 °C | @200 °C |
| level 0     | 31,370  | 3280    | 440     | 26,340  | 3260    | 650     |
| level 1     | 4770    | 990     | 450     | 25,170  | 3000    | 820     |
| level 2     | 5720    | 1000    | 620     | 19,320  | 3380    | 750     |
| level 3     | 20,200  | 2400    | 310     | 15,240  | 2400    | 620     |
All the above improvements in non-volatile multi-state storage were attributed to the embedded copper nanoparticles and the stacked HfO$_x$/ZnO layers. A Schottky barrier at the HfO$_x$/ZnO interface suppressed operational current. Poole–Frankel conduction in the LRS of device S0 resulted in states with a much higher resistance. The embedded Cu nanoparticles significantly affected the whole process due to the electric field enhancement around the metallic nanoparticles [46]. As the embedded nanoparticles changed the LRS conduction mechanism to be CF-assisted Ohmic conduction with a much lower resistance, the ON/OFF resistance ratio of the device S120 was indeed broadened and possibly accommodated an increasing number of distinguishable resistance states. Meanwhile, the enhanced electric field surrounding the nanoparticle positions the CFs in the storage medium and secures the reproducibility of the resistance states, resulting in the reliable functionalities of multi-state storage. Furthermore, the activation energy reflected the difficulty in the migration of defects and was closely associated with the stability and retention of the resistance states. The embedded Cu nanoparticles serving as relays to construct conductive pathways shortened the spacing to build conductive pathways across the storage medium. The retention of the HRS (level 0) and LRS (level 3) degraded with the decreased values of $E_a$s of 1.65 eV and 1.43 eV, respectively. However, for the intermediate resistance states (level 1 and level 2), an increasing number of defects (e.g., V$_{os}$ and Cu ions) produced by the enhanced electric fields prevented the conductive pathways from being destroyed by the migration of a small number of defects. Considering the stacked HfO$_x$/ZnO structure favoring resistance stability at a high temperature [47], the localized conductive pathways should thus be strengthened with increased values of $E_a$s. The stability of the intermediate resistance states should be ensured as well to extend their retention. Consequently, reproducible non-volatile multi-state storage was obtained with desirable data retention. To highlight the merits of the HfO$_x$/ZnO bilayer embedded with Cu nanoparticles, we compared the multilevel properties in this work with the other literature reports as listed in Table 3. It is obvious that the proposed HfO$_x$/ZnO bilayer embedded with Cu nanoparticles had two advantages over the other reports. Firstly, four resistance states could be well reserved for ~1 year at 85°C (or ~10 years at 70°C) compared with the maximal retention of <10$^5$ s in the other work. Secondly, the maximal operational current in this work was 10 µA, which was far smaller than that in the other work.

### Table 2. Activation energies of storage states for devices S0 and S120.

| Device | Level 0 (eV) | Level 1 (eV) | Level 2 (eV) | Level 3 (eV) |
|--------|-------------|-------------|-------------|-------------|
| S0     | 1.92        | 1.05        | 1.07        | 1.90        |
| S120   | 1.65        | 1.53        | 1.44        | 1.43        |

### Table 3. Comparison of multilevel properties.

| Device Structure | $R_{OFF}/R_{ON}$ | Retention (s) | Maximal Current (mA) | Reference |
|------------------|------------------|--------------|----------------------|-----------|
| Ag/Ga$_2$O$_3$:PbS QDs/Pt | $10^6$ | $10^4$ at 85 °C for three states | 100 | [18] |
| TaN/HfO$_2$/Al$_2$O$_3$/HfO$_2$/ITO | $10^2$ | $10^4$ | 1 | [13] |
| Al/PMMA/ZnO QDs/PMMA/ZnO QDs/PMMA/FTO | $10^2$ | $5 \times 10^3$ | 20 | [15] |
| TaN/Co$_2$/Ti (1 nm)/Co$_2$/Pt | $>10^2$ | $10^4$ at 85 °C | 10 | [16] |
| Ag/IGZO/MnO/Pt | $10^6$ | $5 \times 10^3$ at 80 °C | 5 | [22] |
| Al/AlO$_x$/SnO$_x$/FTO | 20 | $5 \times 10^3$ | 20 | [25] |
| ITO/HfAlO/Pt NPs/HfAlO/ITO | $>10$ | $10^4$ | 3 | [27] |
| Cu/AlO$_x$/Al$_2$O$_3$/Pt | $10^5$ | $10^4$ | 10 | [30] |
| Ti/HfO$_x$/Cu NPs/HfO$_x$/ZnO/ITO | $>3 \times 10^2$ | ~1 year at 85 °C for 4 states | <0.01 | This work |
We should also note that the performance of a memristor is closely associated with the thickness of thin films that might change the conduction mechanism and affect performance. ZnO thin films with a suitable thickness strengthen the barrier on the HfO$_x$/ZnO interface with an ignorable resistance contribution [31]. If the ZnO thin films are very thin or even disappear, the ZnO might not be able to feed the HfO$_x$ films with enough oxygen ions. The HfO$_x$ films would be in a less-insulative state, and the switching current would increase with a degraded barrier. Additionally, the prototype device in this work provided a cue for non-volatile multi-state storage. However, the diameter of the devices was ~200 µm, which was huge. Devices of a smaller diameter and with smaller Cu nanoparticles might be necessary for practical integration. Furthermore, though the experimental data presented that device S120 had satisfactory electrical properties and a data retention of ~1 year at 85 °C for four states, the potential evolution of the electrical properties might be discussed as well because the migration of elements in the bilayer structure might have effects on the electrical properties. The diffusion of hafnium and zinc atoms would degrade or even eliminate the HfO$_x$/ZnO interface, causing the operational current to probably increase. Copper diffusion eventually leads to a Cu-doped storage medium, the multilevel properties might be reserved, and the device would have a large operational current [32]. Further investigations should be carried out to gain insight into the above issue.

3.3. Simulation of Synaptic Behaviors

The multilevel resistive switching properties of the devices favored the simulation of synaptic plasticity to serve neuromorphic computing. Considering the improved multilevel resistive switching properties caused by the embedment of copper nanoparticles, we therefore studied the synaptic plasticity of device S120 to evaluate its potential to be an electronic synapse. Typical excitatory postsynaptic currents (EPSC) are presented with electrical stimulation in Figure 6a. The second EPSC was much higher than the first one in mimicking paired-pulse facilitation (PPF) in a bio-synapse. According to the above discussion, the trapped charges affected the resistance of the memristor. When the second electrical stimulation was close to the first one, the trapped charges triggered by the first stimulation did not have enough time to escape completely. Eventually, the shorter interval time of the stimulation was, the higher the intensity of EPSC obtained, as shown in Figure 6b. As a significant property of electronic synapses, the tunable electrical conductance of the devices was studied and triggered by electrical stimuli, as schematically shown in the upper side of Figure 6c. A voltage of 0.5 V was applied for reading the conductance after each potentiation and depression stimulus. The tunable electrical conductance upon potentiation and depression pulses is shown in Figure 6c, suggesting the capability of implementing synaptic weight modulation in response to a potentiation or depression stimulus.

Short-term plasticity (STP) and long-term plasticity (LTP) are fundamental to memory in the human brain [48,49]. Electrical pulses with an amplitude ($V$) of 1.0 V or 2.0 V, a width ($W$) of 10 ms or 20 ms and repetition intervals ($T$) of 0.2 s or 1.0 s were applied to the memristors, as marked in the insets of Figure 7, to evaluate the capability of simulating synaptic plasticity. When input pulses were applied with the lower amplitude of 1.0 V, longer intervals of 1 s and a smaller width of 10 ms, the memristor failed to maintain the higher conductance state (~2.3 µS) and decreased with time back to its initial low conductance value, as shown in Figure 7a, suggesting behavior similar to the STP in a biological synapse. The memristor also presented a long-lived transition to the higher-conductance state with a higher amplitude of 2.0 V, a larger width of 20 ms or shorter intervals of 0.2 s as shown in Figure 7b–d, respectively, which implemented the LTP of a biological synapse as a permanent transition to higher-conductance states in response to the repeated application of input pulses.
Figure 6. Paired-pulse facilitation (PPF) implementations of the NP-embedded devices with tunable conductance to emulate potentiation (red) and depression (blue); (a) excitatory postsynaptic currents (EPSC) in red with their amplitudes of $I_1$ and $I_2$ stimulated by a pair of presynaptic voltage spikes (blue); (b) current change, defined as $(I_2 - I_1)/I_1 \times 100\%$, plotted as a function of pulse interval times; (c) gradual conductance modulation for the devices under pulse stimulation is shown on the top.

Figure 7. Implementation of transformation from STP to LTP for the NP-embedded devices with the insets of stimuli parameters; the transformation from (a) STP to LTP was realized through (b) increasing the stimuli amplitude, (c) extending the stimuli width, or (d) enlarging interval times between stimuli.

The synaptic weight in response to electrical stimuli was worth investigating as well. Figure 8 shows the dependence of conductance on the pulse width and pulse number, with the pulse amplitude and interval fixed at $\pm 3$ V and 1 ms, respectively. A larger pulse width induced a steeper change in conductance, showing a more digital resistive switching
feature. In comparison, a smaller pulse width usually leads to a slow shift in conductance, presenting a more analog switching behavior. When an increasing number of electrical pulses is applied to a memristor, the conductance gradually increases in the potentiation process and decreases in the depression process, approaching an eventually stable conductance state to avoid the uncontrolled growth of synaptic strength and excessive neural firing [49]. Additionally, the pulse frequency affects the conductance of the memristor as well. Figure 9 shows the dependence of current on the pulse number and frequency, with the pulse amplitude and width fixed at 1.5 V and 50 µs, respectively. Instead of the ignorable current change caused by lower frequency pulses, higher frequency (10–200 Hz) pulses resulted in a much larger current variation with an increasing number of pulses. Therefore, the conductance variation in response to pulse was determined by the parameters of the applied pulses. Stimuli with a high energy flux triggered a larger change in conductance.

![Figure 8. Conductance tunability upon pulse width during (a) potentiation and (b) depression for the NP-embedded devices.](image)

![Figure 9. Current tunability upon stimuli frequency for the NP-embedded devices.](image)

As one of the necessary activity-dependent plasticities required to implement important synaptic learning rules for neuromorphic computing [50,51], spike-timing-dependent plasticity (STDP) has been widely investigated for an asymmetric form of Hebbian learning induced by the tight temporal correlation between the pre- and post-synaptic spikes applied to synaptic neurons, as shown in Figure 10. STDP indicates the change in synaptic efficacy determined by the timing of the activity of pre- and post-synaptic neurons, which means the synaptic weight change ($\Delta w$) is a function of the temporal difference ($\Delta t$) between the pre- and post-synaptic spikes. Schematic diagrams of the pre- and post-synaptic spikes with the equivalent stimulus to the device are presented in the inset of Figure 10. As shown in Figure 10, the synaptic weight was enhanced when the pre-synaptic spike led to the postsynaptic spike ($\Delta t > 0$) with the occurrence of long-term potentiation, but it weakened when realizing long-term depression if $\Delta t < 0$. A larger $|\Delta t|$ produced a smaller $\Delta w$, suggesting a good agreement with the asymmetric Hebbian learning rule. The measurements
were performed five times for statistical purposes. Therefore, the STDP learning rule was implemented in the memristor. Small cycle-to-cycle variations in Δ\(w\) were another notable feature, which might be attributed to the embedded NPs sustaining the reproducibility and reliability of the resistive switching process.

![Figure 10. Implementation of the STDP learning rule for the NP-embedded devices. The synaptic weight change (Δ\(w\)) was tested as a function of the temporal difference (Δt) between the pre-spike (blue) and post-spike (red) that are schematically shown in the inset. Equivalent stimulus in black applied to the device is schematically shown in the inset with Δt = 20 ms. Δ\(w\) is defined as (\(w_2 - w_1\))/\(w_1\), where \(w_1\) and \(w_2\), respectively, represent synaptic weights before and after stimulus.](image)

The embedment of copper nanoparticles into the storage medium benefitted the simulation of synaptic plasticity. The copper nanoparticles acted as relays of conductive pathways and stabilized them to ensure the reproducibility of the synaptic weight changes in response to an electrical stimulus. Additionally, the copper nanoparticles enhanced the device sensitivity to electrical stimuli and the device responded to stimuli with a smaller step-size. For one thing, the copper nanoparticles produced many more intermediate states to symbolize the synaptic weight and favor higher accuracy neuromorphic computing to implement the STDP learning rule. For another, electrical stimuli with low energy flux could produce unsustainable conductive pathways for mimicking the STP and the stimuli with high energy flux resulted in LTP due to the sustainable conductive paths. The transformation from the STP to LTP was also mimicked by controlling the energy flux of stimuli.

4. Conclusions

\(\text{HfO}_2/\text{ZnO}\) bi-layer-based memristors with embedded copper nanoparticles were investigated. The embedment of Cu nanoparticles maintained the HRS conduction governed by a Schottky emission mechanism at a low electric field but changed the HRS conduction to cause it to be driven by a Fowler–Nordheim tunneling mechanism under a high electric field. The embedded Cu nanoparticles also changed the LRS conduction dominated by the Poole–Frenkel emission mechanism to be an Ohmic behavior associated with defect-assisted CFs. As a result, the copper nanoparticles acting as the relays of conductive pathways enhanced the localized electric fields to increase the stability and reproducibility of intermediate resistance states. The memristors thus operated at microampere levels with at least four reproducible non-volatile storage states, which could be retained for >10 years at 70 °C. Additionally, the copper-nanoparticle-embedded memristor was capable of implementing the short-term plasticity and long-term plasticity of a bio-synapse. The stacked \(\text{HfO}_2/\text{ZnO}\) bi-layer embedded with copper nanoparticles opens up a route to reproducible non-volatile multi-state storage as well as electronic synapses.

**Author Contributions:** Formal analysis, investigation and original draft preparation, S.C.; review and editing, H.C. and Y.L.; conceptualization, project administration and funding acquisition, Y.L. All authors have read and agreed to the published version of the manuscript.
Funding: This work was supported by the Natural Science Foundation of Fujian Province (Grant No. 2019J01218) and the Fujian Science & Technology Innovation Laboratory for Optoelectronic Information of China (Grant No. 2021ZR145).

Data Availability Statement: Data can be available upon request from the authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ding, G.; Zeng, K.; Zhou, K.; Li, Z.; Zhou, Y.; Zhai, Y.; Zhou, L.; Chen, X.; Han, S. Configurable Multi-State Non-Volatile Memory Behaviors in Ti3C2 Nanosheets. *Nanoscale* **2019**, *11*, 9. [CrossRef] [PubMed]

2. Moon, J.; Ma, W.; Shin, J.H.; Cai, F.; Du, C.; Lee, S.H.; Lu, W.D. Temporal Data Classification and Forecasting Using a Memristor-Based Reservoir Computing System. *Nat. Electron.* **2022**, *2*, 480–487. [CrossRef]

3. Yao, Z.; Osada, T.; Savel’ev, S.E.; Jiang, H.; Midya, R.; Lin, P.; Hu, M.; Ge, N.; Strachan, J.P.; Li, Z.; et al. Memristors with Diffusive Dynamics as Synaptic Emulators for Neuromorphic Computing. *Nat. Mater.* **2017**, *16*, 101–108. [CrossRef] [PubMed]

4. Pedretti, G.; Lelmini, D. In-Memory Computing with Resistive Memory Circuits: Status and Outlook. *Adv. Electron. Mater.* **2021**, *7*, 2000109. [CrossRef]

5. Luo, Q.; Cheng, Y.; Yang, J.G.; Cao, R.R.; Ma, H.L.; Yang, R.; Wei, W.; Zheng, Y.H.; Gong, T.C.; et al. A Highly CMOS Compatible Hafnia-Based Ferroelectric Diode. *Nat. Commun.* **2020**, *11*, 1391. [CrossRef]

6. Sivan, M.; Li, Y.D.; Veluri, H.; Zhao, Y.S.; Tang, B.S.; Wang, X.H.; Zamburg, E.; Leong, J.F.; Niu, J.X.; Chaudhary, U.; et al. All WSe2 1T1R Resistive RAM Cell for Future Monolithic 3D Embedded Memory Integration. *Nat. Commun.* **2019**, *10*, 12. [CrossRef]

7. Han, X.; Privat, A.; Holbert, K.E.; Seo, J.; Yu, S.; Barnaby, H.J. Total Ionizing Dose Effects on Multistate HfO2-Based RRAM Synaptic Array. *IEEE Trans. Nucl. Sci.* **2021**, *68*, 756–761. [CrossRef]

8. Shi, T.; Wang, R.; Wu, Z.; Sun, Y.; An, J.; Liu, Q. A Review of Resistive Switching Devices: Perforance Improvement, Characterization, and Applications. *Small Struct.* **2021**, *2*, 2000109. [CrossRef]

9. Lu, W.; Li, C.; Zheng, L.; Xiao, J.; Lin, W.; Li, Q.; Wang, X.; Huang, Z.; Zeng, S.; Han, K.; et al. Multi-Nonvolatile State Resistive Switching Arising from Ferroelectricity and Oxygen Vacancy Migration. *Adv. Mater.* **2017**, *29*, 1606165. [CrossRef]

10. Zhang, Y.; Cai, W.; Kang, W.; Yang, J.; Deng, E.; Zeng, Y.G.; Zhao, W.; Ravelosona, D. Demonstration of Multi-State Memory Device Combining Resistive and Magnetic Switching Behaviors. *IEEE Electron Dev. Lett.* **2018**, *39*, 684–687. [CrossRef]

11. Cao, Y.; Rushforth, A.W.; Sheng, Y.; Zheng, H.; Wang, K. Tuning a Binary Ferromagnet into a Multistate Synapse with Spin-Orbit-Torque-Induced Plasticity. *Adv. Funct. Mater.* **2019**, *29*, 1808104. [CrossRef]

12. Kim, Y.; Choi, H.; Park, H.S.; Kang, M.S.; Shin, K.Y.; Lee, S.S.; Park, J.H. Reliable Multistate Data Storage with Low Power Consumption by Selective Oxidation of Pyramid-Structured Resistive Memory. *ACS Appl. Mater. Interfaces* **2017**, *9*, 38643–38650. [CrossRef]

13. Mahata, C.; Kang, M.; Kim, S. Multi-Level Analog Resistive Switching Characteristics in Tri-Layer HfO2/Al2O3/HfO2 Based Memristor on ITO Electrode. *Nanomaterials* **2020**, *10*, 2069. [CrossRef] [PubMed]

14. Lee, H.; Beom, K.; Kim, M.; Kang, C.H.; Yoon, T. Nonvolatile Memory and Artificial Synaptic Characteristics in Thin-Film Transistors with Atomic Layer Deposited HfO2 Gate Insulator and ZnO Channel Layer. *Adv. Electron. Mater.* **2020**, *6*, 2000412. [CrossRef]

15. Wang, W.X.; Yang, L.; Yue, W.J.; Gao, S.; Zhang, C.W.; Chen, Z.X.; Chen, Y.H. Study on Multilevel Resistive Switching Behavior with Tunable ON/OFF Ratio Capability in Forming-Free ZnO QDs-Based RRAM. *IEEE Trans. Electron Dev.* **2020**, *67*, 4884–4890. [CrossRef]

16. Rana, A.M.; Ismail, M.; Akber, T.; Nadeem, M.Y.; Kim, S. Transition from Unipolar to Bipolar, Multilevel Switching, Abrupt and Gradual Reset Phenomena in a TaN/CoO/Ti/Pt Memory Devices. *Mater. Res. Bull.* **2019**, *117*, 41–47. [CrossRef]

17. Sun, C.; Lu, S.M.; Jin, F.; Mo, W.Q.; Song, J.L.; Dong, K.F. FePt Metallic Nanoparticle Dispersion-Induced Evolution of Resistive Switching Performance in SiO2-Based RRAM Devices. *J. Electron. Mater.* **2020**, *49*, 530–536. [CrossRef]

18. Yan, X.B.; Pei, Y.F.; Chen, H.W.; Zhao, J.H.; Zhou, Z.Y.; Wang, H.; Zhang, L.; Wang, J.; Li, X.Y.; Qin, C.; et al. Self-Assembled Networked PbS Distribution Quantum Dots for Resistive Switching and Artificial Synapse Performance Boost of Memristors. *Adv. Mater.* **2019**, *31*, 1805284. [CrossRef]

19. Giovinozzi, C.; Sandrini, J.; Shahraihi, E.; Celik, O.T.; Leblebici, Y.; Ricciardi, C. Analog Control of Retainable Resistance Multistates in HfO2 Resistive-Switching Random Access Memories (ReRAMs). *ACS Appl. Electron. Mater.* **2019**, *1*, 900–909. [CrossRef]

20. Sedghi, N.; Li, H.; Brunell, I.F.; Dawson, K.; Potter, R.J.; Guo, Y.; Gibbon, J.T.; Dhanak, V.R.; Zhang, W.D.; Zhang, J.F.; et al. The Role of Nitrogen Doping in ALD Ta2O5 and Its Influence on Multilevel Cell Switching in RRAM. *Appl. Phys. Lett.* **2017**, *110*, 102902. [CrossRef]

21. Lai, Y.F.; Xin, P.C.; Cheng, S.Y.; Yu, J.L.; Zheng, Q. Plasma Enhanced Multistate Storage Capability of Single ZnO Nanowire Based Memory. *Appl. Phys. Lett.* **2015**, *106*, 031603. [CrossRef]

22. Abbas, H.; Ali, A.; Jung, J.; Hu, Q.; Park, M.R.; Lee, H.H.; Yoon, T.S.; Kang, C.J. Reversible Transition of Volatile to Non-Volatile Resistive Switching and Compliance Current-Dependent Multistate Switching in IGZO/MnO RRAM Devices. *Appl. Phys. Lett.* **2019**, *114*, 093503. [CrossRef]
