Energy-Aware Multiple-Valued Current-Mode Sequential Circuits Using a Completion-Detection Scheme

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SUMMARY A multiple-valued current-mode (MVCM) circuit using current-flow control is proposed for a power-greedy sequential linear-array system. Whenever operation is completed in processing element (PE) at the present stage, every possible current source in the PE at the previous stage is cut off, which greatly reduces the wasted power dissipation due to steady current flows during standby states. The completion of the operation can be easily detected using “operation monitor” that observes input and output signals at latches, and that generates control signal immediately at the time completed. Since the wires of data and control signals are shared in the proposed MVCM circuit, no additional wires are required for current-flow control. In fact, it is demonstrated that the power consumption of the MVCM circuit using the proposed method is reduced to 53 percent in comparison with that without current-source control.

key words: multiple-valued logic, current-mode circuit, adaptive current control, many-core processor

1. Introduction

Vastly more powerful computers that deliver teraflop performance with the efficient capabilities are needed to handle tomorrow’s emerging applications. A many-core processor, which has lots of small cores, is a hopeful solution to realize these applications. However, in many-core processors, on-chip global interconnect links between cores are increased with the number of cores, and have significant effects on the overall system performance [1]–[3].

A promising approach to solving the wire complexity is the use of a multiple-valued current-mode (MVCM) circuit technique which allows each wire to deliver more information. In addition, low voltage-swing data transmission can be realized by using current-mode logic, which results in high-speed switching. It has been shown that the performance of various circuits, in particular arithmetic circuits, is improved by using the MVCM circuit technique [4]–[7]. However, it is not well considered how to reduce the wasted power dissipation due to steady current flows in the MVCM circuit.

In this paper, an MVCM circuit using a completion-detection scheme is proposed. Whenever operation is completed in processing element (PE) at the present stage, every
$I_{11}, I_{12}, \cdots, I_{1(L-1)}$ are applied to comparators which have different threshold current values $I_{T1}, I_{T2}, \cdots, I_{T(L-1)}$. In each comparator, the comparison of the amount of a duplicated current flow $I_{Tn}$ and a threshold current value $I_{Tn}$ is performed, and the comparison result is generated as a binary voltage signal $V_{Gn}$. Each voltage signal is stored into a flip-flop at once, and then applied to the output generator. The output generator recognizes the L-valued logic input value by $V_{Gn}$, and performs a certain L-valued logic operation. Finally, an L-valued current signal $I_0$ corresponding to $I_l$ is generated. By changing the L-valued logic operation implemented the output generator, an arbitrary L-valued function can be performed. In the same way, an arbitrary M-input N-output L-valued function can be performed by a processing element which is composed of M current mirrors, M(L-1) comparators, M(L-1) flip-flops, and N output generators.

To perform the threshold operation and the output-current generation, each of the comparators and the output generators contains current sources which continuously provide stable currents. That is, MVCM circuit inherently involves steady current flows which occur independent of an operation condition of the circuit. The current-based operation can be utilized to realize a high-performance circuit with low-voltage swing, however, it often becomes a major obstacle for broadening the application of MVCM circuits.

Figure 2 compares the power dissipation in binary CMOS circuits with that in MVCM circuits. In each clock cycle, a circuit operation can be divided into two phases: a transition phase where circuit elements are switched and current flows due to charge/discharge of load capacitance are occurred, and a completion phase where the charge/discharge of load capacitance are completed and the output of the circuit becomes constant. Binary CMOS circuits consume a large amount of power in the transition phase, while consume a little amount of power in the completion phase. In contrast, MVCM circuits consume a constant amount of power regardless of the operation phase due to the steady current flows in the circuit. Thus, if the MVCM circuit works in high operating frequency region where the circuit activity is relatively high, less power dissipation is required in comparison with a binary CMOS circuit. In low operating frequency region, on the other hand, the power dissipation of the MVCM circuit becomes larger than that of the binary CMOS circuit since the circuit activity is low and the amount of steady current flow dominates the total power dissipation. This severely restricts the application fields of MVCM circuits.

From this point of view, in the following section, we propose a low-power MVCM circuit which greatly reduces the wasted power dissipation due to steady current flows during standby states. The key idea is to detect the operation completion by monitoring the transition of internal signals, and greedily eliminate the wasted power consumption during the completion phase as shown in Fig. 3. An embedded internal-signal monitor circuit enables to detect the timing when the transition phase is finished, and eliminate the power consumption in the completion phase by cutting off the current paths. As a result, the power consumption of the MVCM circuit becomes lower than that of the CMOS circuit when the power consumption during the delay time for the current-flow control is relatively small. This makes it possible to extend the application field of MVCM circuits.

3. Design of an MVCM Circuit Using Completion-Detection Scheme

In this section, we explain the circuit implementation of a processing element based on an MVCM circuit using a current-flow control scheme, completion-detection scheme, and confirm its basic behavior. Then, we show the effectiveness of the proposed technique through the comparison of the power consumption in a binary CMOS circuit, a conventional MVCM circuit and the MVCM circuit using the completion-detection scheme.

Figure 4 shows a block diagram of the processing element based on an MVCM circuit with the completion-detection scheme, which consists of the conventional circuit
components and an additional component called “operation monitor (OM)”. The operation monitor detects whether the operation phase is transition phase or completion phase by monitoring internal signals $V_{Gn}$ and $V_{GMn}$, which are the output signals of the comparators and the master latches, and controls path switches to cut off the steady current flows depending on the operation phase.

When $V_{Gn}$ and $V_{GMn}$ have different logic values, the processing element is in the transition phase and steady current flows exist. On the other hand, when $V_{Gn}$ and $V_{GMn}$ have the same logic value, the output logic value of the comparator has been stored in the master latch and the operation phase has shifted to the completion phase. That is, the steady current paths to the processing element at the previous stage, path A, and in the processing element at the present stage, path B, can be cut off. Depending on the operation phase, the operation monitor generates an enable signal $V_{EN}$ and controls the current sources. $V_{EN}$ is given by

$$V_{EN} = \begin{cases} \text{LOW} & \text{if } V_{Gn} = V_{GMn}, \\ \text{HIGH} & \text{if } V_{Gn} \neq V_{GMn}. \end{cases} \quad (1)$$

The paths are cut off when $V_{EN}$ is “LOW”, and are turned on when $V_{EN}$ is “HIGH”. In this way, the use of the completion-detection scheme enables to eliminate wasted current flows of the processing element in the completion phase.

Figure 5(a) shows a block diagram of the operation monitor which consists of a delay element A, K-to-1 multiplexer, L-1 sets of a delay element B and an EXOR circuit, and an OR circuit. The delay element A, K-to-1 multiplexer, and AND circuit generate $V_{EO}$ which becomes “HIGH” from the timing when the clock signal rises to the timing when the transitions of $V_{Gn}$ start. The control signal of the K-to-1 multiplexer is generated in an external controller according to the kind of the operation and output distance. The L-1 sets of the delay element B and EXOR circuit detect the transition of $V_{Gn}$ through equality detections, and generate $V_{Mb}$ which become “HIGH” from the timing when the transition of $V_{Mb}$ happens to the timing when the transition of $V_{M(N-1)}$ or $V_{M(N+1)}$ happens. The OR circuit transforms $V_{EO}$ and $V_{Mb}$ into $V_{EN}$.

Figure 5(b), and (c) show operation flows of the operation monitors without the delay elements A and B, and with the delay elements A and B. In the operation monitor without the delay elements A and B, the timing when $V_{EO}$ becomes “HIGH” doesn’t exist and the timings when $V_{Mb}$ become “HIGH” don’t overlap one another. As a result, some parts of the timing when $V_{EN}$ should be “HIGH” become “LOW”. To solve this problem, the delay elements A and B whose delay times are adjusted to $T_A$ and $T_B$ are used. The use of the delay element A makes the timing when $V_{EO}$ becomes “HIGH” and the timings when $V_{Mb}$ become “HIGH” overlapped. The use of the delay element B makes the timings when $V_{Mb}$ become “HIGH” overlapped one another. As a result, the desired $V_{EN}$ is generated in the operation monitor.

Figure 6 summarizes basic components of the processing element. An output generator consists of NMOS pass-gate trees and current sources. In the current source, transistors $M_{P1}, M_{P2}, \ldots, M_{Pn}$ work as source degeneration resistances which relieve the effects caused by threshold-voltage variation and temperature variation [11]. As with the current source, transistors $M_{P1}, M_{P2}, \ldots, M_{Pn}$ in this current mirror work as not only switches to cut off current flows but also

![Figure 4](image1)

**Fig. 4** Block diagram of the processing element based on an MVCM circuit with the completion-detection scheme.

![Figure 5](image2)

**Fig. 5** Operation monitor: (a) block diagram, (b) operation flow without delay elements A and B, and (c) operation flow with delay elements A and B.
as source degeneration resistances. A comparator is implemented using a current source which generates a threshold current \( I_T \) and a CMOS-based inverter. Master and Slave latches are CMOS-based ones. In a master latch, there is an additional complementary pass gate whose input is \( V_{EN} \) to prevent the stored value from being changed during the completion phase.

Figure 7 summarizes a detailed operation flow of the processing element based on the MVCM circuitry using the completion-detection scheme. The operation is performed in the following steps:

1. A clock signal rises and an operation begins. \( V_{EN} \) turns to “HIGH” and \( I_f \) starts to flow.
2. The operation result of a processing element in the previous stage reaches the input of the master latch.
3. After the estimated delay time is elapsed, the operation monitor performs an equality detection between \( V_{GM} \) and \( V_{GMA} \).
4. The operation monitor detects the operation completion when \( V_{GMA} \) becomes the same logic value of \( V_{GM} \), which indicates that the operation result of a processing element in the previous stage is stored into the master latch, and \( V_{EN} \) turns to “LOW”.
5. \( I_f \) is cut off and the wasted current flows in the completion phase are eliminated.

In this way, in the MVCM circuitry using the completion-detection scheme, the current flows only exist from when the clock rises to when the operation completion is detected.

Figure 8 shows simulated waveforms of the processing element based on the MVCM circuitry using the completion-detection scheme. The waveform of \( V_{G1} \), \( V_{GMA} \), \( V_{EO} \), and \( V_{EN} \) show that the operation monitor works correctly. The waveform of \( I_f \) and \( V_{EN} \) show that \( I_f \) is correctly controlled with \( V_{EN} \) except that there are some glitches due to transition of the clock signal. Thus, it is confirmed that the wasted current flows in the processing element can be ac-
tually eliminated by using the completion-detection scheme.

To demonstrate the advantage of the MVCM circuit using the completion-detection scheme, we compared the power consumption of a 2-bit adder based on it with those based on the binary CMOS circuit and the conventional MVCM circuit. Since 4-valued representation can halve the operating frequency, the power consumptions of the 2-bit adders based on MVCM circuits are simulated at the operation frequency of 200 MHz and 500 MHz and that based on binary CMOS circuit are simulated at the operation frequency of 400 MHz and 1 GHz with HSPICE under a 90 nm CMOS technology.

Figure 9 indicates the unit current versus switching time characteristic of the 2-bit adder based on the MVCM circuit with completion-detection scheme. Note that the unit current represents the current value corresponding to one logic level. The delay time becomes smaller with the increase of unit current. We can confirm that the unit current should be set to larger than around 10 μA and 40 μA in case that the operation frequency is 200 MHz and 500 MHz, respectively. In this simulation, we set to 20 μA and 50 μA considering the variation of the unit current due to threshold-voltage and temperature variations.

Figure 10 shows a shmoo plot of the 2-bit adder based on the MVCM circuitry using the completion-detection scheme under threshold-voltage, temperature, and supply voltage variations. The range of temperature variation and supply voltage variation are from −25°C to 125°C and from 1.1 V to 1.3 V and are applied to the adder uniformly. The range of threshold-voltage variation is ±10% of the threshold voltage and is applied to each transistor randomly. The use of current sources and current mirrors with source-degeneration resistances as shown in Fig.6 prevents logic errors. In addition, proper configuration of the delay element B in the operation monitor prevents timing errors. As a result, the adder works correctly from −25°C to 75°C and from 1.1 V to 1.3 V under ±10% threshold-voltage variation.

Figure 11 indicates the wire length versus power consumption characteristics of the 2-bit adders based on the binary CMOS circuit, the conventional MVCM circuit, and the MVCM circuit using the completion-detection scheme at the operation frequency of 200 MHz and 500 MHz. Note that the equivalent circuit of a wire is given by a π-model in this evaluation. We can confirm that the longer the wire length becomes and the more the operating frequency decreases, the proposed MVCM circuit reduces the power consumption effectively. This is because the time ratio of the completion phase in each clock cycle is increased in the above condition, and the current dissipation caused by the steady current flows during the completion phase dominates the total power dissipation.

![Fig. 9](image1.png)  
Unit current vs. switching time of the 2-bit adder based on the MVCM circuitry using the completion-detection scheme.

![Fig. 10](image2.png)  
Shmoo plot of the 2-bit adder based on the MVCM circuitry using the completion-detection scheme under threshold-voltage, temperature, and supply voltage variations.

![Fig. 11](image3.png)  
Wire length vs. power consumption of the 2-bit adder based on the binary CMOS circuit, the conventional MVCM circuit, and the MVCM circuit using the completion-detection scheme: (a) at the operation frequency of 200 MHz, (b) at the operation frequency of 500 MHz.
In case that the operation frequency is 200 MHz, for example, the power consumption on the conventional MVCM circuit is smaller than that based on the binary CMOS circuit when the wire length is longer than 1500 μm. On the other hand, the power consumption of that based on the MVCM circuit using the completion-detection scheme is smaller than that based on the binary CMOS circuit when the wire length is longer than 10 μm. Similarly, in case that the operation frequency is 500 MHz, the conventional MVCM circuit is effective when the wire length is longer than 1750 μm, while the MVCM circuit with the completion-detection scheme is effective when it is longer than 250 μm. This result shows that the use of the completion-detection scheme enables to extend the range of the wire length where the MVCM circuit have advantage in power consumption over the binary CMOS circuit.

4. Evaluation Using an Application

In this section, we evaluate the performance of many-core processors based on the binary CMOS circuit, the conventional MVCM circuit, and the MVCM circuit with the completion-detection scheme by using two virtual operations.

As a typical example, we consider to apply the proposed technique to a fine-grained many-core processor which has broad range of wire length. Figure 12 shows the chip photograph of a matrix processor [12]. This processor has 32 sub-circuit blocks called “banks” each of which consists of 64 2-bit processing elements and 128 512-bit SRAMs. There are shorter wires which connect the processing elements and SRAMs in a bank locally and longer wires which connect distantly-positioned banks globally, and limited peer-to-peer data transmissions are performed during the operation. The wire length utilized for the data transfer varies from about 10 μm to 2000 μm depending on the operation. To enhance the performance of this kind of processors, it is important to increase the number of the embedded processing elements, which requires to reduce not only the wire complexity between the processing elements but also the power dissipation and the area of the processing elements.

Figure 13 shows a block diagram of 2-bit processing elements based on the binary CMOS and the MVCM circuit. Each processing element has two function units: a load-function unit, a processing-element-function unit, and flip-flops between them. The use of the MVCM circuit enables to implement compact arithmetic and logic units. Thus, the area of the processing-element-function unit based on the MVCM circuit is smaller than that based on the binary CMOS circuit. In addition, it also enables to reduce the number of the multiplexers to half in the load-function unit. As a result, in spite of the area overhead of the comparators, the area of the processing element based on the MVCM circuit is smaller than that based on the binary CMOS circuit [7]. The 2-bit processing element based on the MVCM circuit using the proposed scheme has about 10-percent area overhead in comparison with that based on the conventional MVCM circuit.

In this evaluation, we use two virtual operations, operation A and operation B, whose distributions of wire lengths utilized for the data transmission between the processing elements are different as shown in Fig. 14. Note that 0 μm wire occurs when a processing element outputs the operation result to itself. During the operation A, the utilization rate of shorter wires is higher than that of longer wires and the average wire length is 39 μm. On the other hand, during the operation B, the utilization rate of longer wires is higher than that of shorter wires and the average wire length is 669 μm. The difference of the distributions results in the difference of the power consumption.

Table 1 summarizes the evaluation result using the two virtual operations. In this evaluation, we assume:

- The power consumption of 16-banks 1024-processing-elements many-core processors are evaluated.
- The wire length between the banks and the processing elements are based on the chip layout of the matrix processor as shown in Fig. 15 without considering detour wiring.
- The number of wires between two processing elements limited to one.
- The equivalent circuit of a wire is given by a π-model.
- The power consumption of the processing elements are measured without considering those of the SRAMs.

During the operation A, the processing elements based on the MVCM circuit using the completion-detection scheme consume 10.2 mW and that based on the binary CMOS circuit consume 11.1 mW. That is, the power consumption of processing elements based on the MVCM circuit with the proposed scheme is 92 percent in comparison with that based on the binary CMOS circuit. On the other hand, during the operation B, the processing elements based on the MVCM circuit using the completion-detection scheme consume 18.6 mW and that based on the binary CMOS circuit consume 21.8 mW. That is, the power consumption of processing elements based on the MVCM circuit with the proposed scheme is 85 percent in comparison with that based on the binary CMOS circuit. From this result, it is confirmed that the MVCM circuit using the completion-detection scheme has advantage in the power consumption over the binary CMOS circuit, especially in the operation...
where long wires are often used. In case that the chip size becomes larger and more processing elements are embedded, the average wire length becomes longer. Thus, it is expected that the many-core processor based on the MVCM using the completion-detection scheme would have better advantage in power consumption over that based on the binary CMOS circuit.

5. Conclusion

An MVCM circuitry using a completion-detection scheme...
is proposed for a many-core processor. The use of a completion-detection scheme enables to eliminate the wasted power consumption due to steady current flows by detecting the timing when the operation is completed and cutting off the current flows. As a result, low-power processing element based on the MVCM circuit, where the wasted power consumption is greedily eliminated, can be implemented. In fact, it is demonstrated that the power consumption of a many-core processor based the proposed circuit during a typical operation is reduced to 53 percent and 85 percent in comparison with those based on a conventional MVCM circuit and a binary CMOS circuit, respectively.

In this paper, a new technique to finely cut off steady current flows during an active mode is proposed for MOS current-mode circuits. By combining the proposed technique with power gating techniques to reduce power consumption during a standby-mode, lower-power MOS current-mode circuits can be implemented.

As a future prospect, it is important to evaluate the many-core processor based on the MVCM circuitry using the completion-detection scheme where more processing elements are embedded. In addition, we will discuss typical applications of the MVCM circuitry with completion-detection scheme, for example FPGAs and implement them.

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