Study on Gate Circuit Multivibrator Based on FPGA

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Abstract. Gate circuit multivibrator is composed of logic gates and RC circuit. When the vibrator is designed based on FPGA, the pulse frequency measured using frequency meter in FPGA is much higher than theoretic analysis value. If this circuit is used as a pulse signal generator, mistakes will be made easily. In this paper, a gate circuit multivibrator based on FPGA is designed, and its vibrating frequency is measured using the FPGA itself. A frequency error is measured. The reason that causes this error is analyzed, and it is testified through simulation and real signal test. Pulse shaping through Schmitt trigger is an effective solution method. This study shows that clock pulse is very important to FPGA system.

1. Introduction
Gate circuit multivibrator is a kind of self-excited multivibrator composed of logic gates and RC (Resistor-Capacitor) circuit[1]. It is widely used because it is one of the simplest and most important pulse generating circuits in electronics. When we need an oscillation signal with a given frequency, the signal can be generated by a gate circuit multivibrator easily. The circuit can be designed through simulation, and the simulation result is close to theoretic analysis value. However, when the vibrator circuit is designed based on FPGA(Field Programmable Gate Array), the frequency measured via the FPGA itself is much higher than the theoretic analysis value or simulation result. Why does this difference arise and how to solve this problem? The experiment is designed and analyzed as follows.

2. Gate circuit multivibrator based on FPGA
There are many kinds of self-excited multivibrator circuits. A typical and simple one is asymmetric gate circuit multivibrator[2]. The principle of this vibrator is shown in Fig.1. The two NOT gates can be implemented based on FPGA.

Fig.1 Asymmetric gate circuit multivibrator based on FPGA
In this figure, a, b and c are defined as three I/O pins. They are described in VHDL as follows.

```vhdl
  a: in  STD_LOGIC;
  b: out STD_LOGIC;
  c: out STD_LOGIC;
```

The logic function in Fig.1 can be described as follows.

```vhdl
  b <= b_sig;
  c <= c_sig;
  b_sig <= not a;
  c_sig <= not b_sig;
```

A resistor R is connected between the pins a and b, and a capacitor C is connected between the pins a and c. Then a gate circuit multivibrator based on FPGA is designed. When the above program runs, oscillating pulses can be gotten at the point of “Output” in Fig.1.

3. Oscillation frequency measurement

3.1. Theoretic analysis

In Fig.1, the capacitor C is 0.1μF, and the resistor R is set as 3kΩ. A Digilent BASYS-2 Xilinx FPGA board is chosen in this experiment. The threshold voltage of the FPGA input is measured about 1.3V. The low level voltage and the high one are measured 0V and 3.3V respectively. We assume that the circuit operates under an ideal condition. That is to say, the low level voltage is always 0V, the high one is always 3.3V, and the gate circuit output impedance is 0 no matter its output is low or high level voltage. Under this ideal condition, the oscillation period is about \(2.2RC\). Therefore the frequency can be calculated about 1.5kHz. In fact, the circuit can not run under this ideal condition. The low level voltage or the high one of output will change with different load. The output impedance can not be 0. So the oscillation frequency of pulse generated in the real circuit is some different from the theoretic value under an ideal condition.

3.2. Experiment measurement

A frequency meter in FPGA is designed to measure the oscillation frequency of signal b_sig, c_sig or input a. The frequency that is measured by FPGA itself is about 52kHz. It is obviously much higher than theoretic value or simulation result. And at this moment, the frequency value fluctuates with a very wide range. Apparently, this measuring result is not right.

When the frequency of point “a” is measured with an oscilloscope directly, the result of frequency measured is shown in Fig.2.

![Fig.2 Frequency measured with oscilloscope directly](image)

In Fig.2, there are two different measured values of the frequency. The upper 52.63kHz is close to the result measured by FPGA frequency meter. It is much higher than the lower frequency 1.34179 kHz or theoretic analysis value. The frequency fluctuates with a very wide range too. The lower one is close to simulation value, and it is very stable. According to further analysis, the lower frequency is
just the frequency value under real circuit condition. The oscillation frequency of real circuit is about 1.34 kHz.

4. Reason analysis of wrong measured result
A same signal is measured, the two results are not same at all. Which one is right? What is the reason of wrong measured result?

4.1. Reason presumption
According to comparison of the two measurement methods, it is inferred that the reason which causes this difference is possibly from electronic noises. Influenced by all kinds of noises, some disturbing pulses may be generated. The FPGA frequency meter is very sensible to the edge of the pulse. Because the speed of FPGA is very high, this disturbing pulse will be counted. When the frequency is measured with oscilloscope directly, the high frequency disturbing pulse can be restrained because of bandwidth limited, so a right frequency value can be gotten.

4.2. Experiment analysis

4.2.1. FPGA threshold measurement
The transfer characteristic of NOT gate based on FPGA is measured. NOT gate function is described as follows. Here “a” is an input, “b” is an output.

\[
b <= \textit{not} \ a;
\]

The principle of measuring transfer characteristics of NOT gate in FPGA is shown as Fig.3.

Fig.3 Principle of measuring transfer characteristic
A DC voltage signal is input from “a”, and the output voltage of “b” is measured. The transfer characteristic of the NOT gate based on FPGA is shown in Tab.1.

| Vin /V | 0   | 0.5 | 1.0 | 1.1 | 1.1 | 1.2 | 1.3 | 1.3 | 2.0 | 3.0 |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Vout/V | 3.3 | 3.3 | 3.3 | 3.3 | 2.3 | 2.2 | 2.0 | 1.9 | 1.8 | 1.6 | 0   | 0   | 0   |

According to Tab.1, the transfer characteristic curve of NOT gate based on FPGA is shown as Fig.4. The curve shows that the threshold range of the NOT gate is small. When the input is near the threshold voltage, the state of the gate output is unstable extraordinarily. Especially, according to Fig.4, when the input voltage is from 1.30V to 1.35V, the output will change from 1.61V to 0. A very hairlike input change can cause state change of the output. At this time, the state of the next gate in Fig.1 will be changed too. So the gate state of FPGA will be disturbed by noises easily.
4.2.2. Influence analysis of noise disturbing via simulation

A ramp signal is assumed as the input of the NOT gate. In real circuit, this ramp signal contains noises. A higher frequency sine signal is simulated as a noise. So the total input signal composes of a net input ramp signal and a noise. The simulation circuit is shown as Fig.5. At this time, the output of the NOT gate is shown as Fig.6.

4.2.3. Testifying via FPGA experiment

A frequency meter is designed to measure the frequency of the pulse. The measurement principle is shown as Fig.7. The frequency of the input signal is set 1kHz, and the pulse is chosen sine-shaped, triangle-shaped, and rectangle-shaped signal respectively.
If the input signal is rectangle-shaped pulse, the measured frequency is the same as that of the input signal. But if the input pulse is sine-shaped or triangle-shaped one, the frequency is much higher than that of the input. The reason that causes this mistake is noise disturbing. The former presumption can be testified through this real experiment. In Fig. 1, the wave shape of point “a” is ramp, so disturbance is generated similarly.

4.3. Solution method

According to the above analysis, we can see that, FPGA clock system is sensible to the edge of the pulse. Ramp-edged signal will lead to disturbance easily. If ramp-edged signal are transferred to rectangle-shaped pulse, the disturbance will decrease. When clock input circuit is changed to Schmitt trigger, this disturbing can be decreased greatly[4-5].

Another solution way is synchronization. The error is mainly from electronic noises. If the vibrating signal is synchronized, the program can be described as follows.

```
process(clk)
begin
  if(falling_edge(clk)) then
    a_sig <= a;
  end if;
end process;
```

According to the above program, if “a_sig” is used as vibrating signal other than “a”, the disturbance can be restrained greatly, and the frequency or period value measured will be right.

5. Conclusion

Gate circuit multivibrator is widely used in generating a clock pulse signal because of its simpler structure and less components consumption than other circuits. A phenomenon of wrong frequency measurement of the gate circuit multivibrator based on FPGA is found. So this gate circuit multivibrator is not a reliable pulse source. The reason of causing the error is analyzed and testified. Much higher frequency disturbing pulses are generated because of noises. Clock pulse of digital system has a strict requirement. It ought to be with low noise and steep edge. Two methods are put forward to solve this problem. The analysis shows that more attentions should be paid to this problem.

References

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