Bias stress instability in multilayered MoTe$_2$ field effect transistors under DC and pulse-mode operation

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Introduction: In a recent past, transition metal dichalcogenides (TMDCs) have been actively employed towards next generation device research beyond Si technology owing to their thinness of two-dimensional nature, number of layers dependent sizable bandgaps, novel optical/mechanical properties, and others [1–4]. Among a variety of TMDCs, multilayered molybdenum ditelluride (m-MoTe$_2$) has been attractively considered as one of versatile candidates because of their low energy bandgap (~0.9 eV) properties, leading to preferable n (or p)-type switching, which is mandatory for the reconfigurable device operation [5]. Moreover, among a variety of applications, future display backplanes [6] and internet of things (IoT) sensors based on MoTe$_2$ field effect transistors (FETs) could be one of the envisioned promising candidates due to ease tunability toward n (or p)-type FETs, excellent gas sensitivity associated with large volume-to-surface ratio, and insensitivity to photoresponse under light illumination [7–9]. In this sense, significant research activities have been investigated towards the improvement of electrical properties and their feasibility confirmation on newly proposed applications, such as sensors and memory devices, and others [10, 11]. However, for realisation of the aforementioned application, aspects on device instability for m-MoTe$_2$ FETs during the electrical operation should be thoroughly investigated, but interestingly, such kind of research activities have been limitedly executed, as compared to one of the representative multilayered MoS$_2$ (m-MoS$_2$) FETs [12–14]. In particular, understanding of bias stress instability (BSI) behaviours under DC (or/and AC) mode operation and their comparison are highly demanding for the circuit level application because the better understanding on the origins of device instability in m-MoTe$_2$ FETs can secure the device reliability by either optimisation of material properties or development of novel operation scheme associated with duty cycle, amplitude, bias polarity, and others.

In this letter, we investigated BSI of m-MoTe$_2$ FETs after encapsulation with hydrophobic polymer (cyclic transparent optical polymer; CYTOP), which has been reported to have the effectiveness to secure external gas effects in air [15, 16]. Moreover, bias polarity, electric field, and device instability of m-MoTe$_2$, respectively. In this study, all protocols for the fabrication and encapsulation of m-MoTe$_2$ were adopted from the same method in the previous reports [9, 15].

Results and discussions: For evaluation of electrical performance of m-MoTe$_2$ FETs, transfer characteristics ($I_{DS}$–$V_{GS}$) at $V_{DS} = −0.1$ V and output characteristics ($I_{DS}$–$V_{DS}$) were measured. As shown in Figure 1c, transfer curves before (or after) CYTOP encapsulation show typically observed p-type behaviours. In addition, Figure 1d shows good saturation behaviours and Ohmic contact properties around a low drain bias regime which represents appropriate device operation. Detailed electrical properties of fabricated m-MoTe$_2$ FETs at $V_{DS} = −0.1$ V are summarised in Table 1. For the evaluation of electrical parameters, $V_{th}$ was calculated as the value of x-axis intercept of linear extrapolation of the $I_{DS} − V_{GS}$ curve at its maximum first derivative point [17] and $\mu_{fe}$ was

Here, bias stress instability on multilayered MoTe$_2$ field effect transistors (m-MoTe$_2$ FETs) with encapsulation of hydrophobic polymers (cyclic transparent optical polymer) is systematically investigated under DC and pulse mode operation. During DC mode stress, the threshold voltage shift ($\Delta V_{th}$) under positive bias stress is at least three times larger than that of negative stress due to high hole barrier (~0.57 eV), compared with electron barrier (~0.18 eV). However, $\Delta V_{th}$ in positive pulse mode stress is significantly reduced with decrease of a duty cycle, as compared with that of negative stress. With isolation from external gas ambient effects such as H$_2$O and O$_2$, shallow electron traps in multilayered MoTe$_2$ field effect transistors are identified as one of strong candidates to cause bias polarity dependency on $\Delta V_{th}$ in pulse mode. Moreover, recovery time for traps, involved during positive bias stress, is six times faster than that of negative stress, substantiating that shallow electron traps and their fast detrapping are one of key origins.

In practice, optimisation of pulse mode operation via bipolar switching can be potentially utilised for minimisation of device instability during the operation of multilayered MoTe$_2$ field effect transistors and their circuits.

Fig 1 (a) Trapping process of charge carriers in MoTe$_2$ channel. (b) Device structure of m-MoTe$_2$ FETs with CYTOP. (c) I–V curves of m-MoTe$_2$ FETs in a linear and a log scale. (d) Output curves of m-MoTe$_2$ FETs.
Table 1. Summary of electrical parameters for m-MoTe2 FETs with CYTOP encapsulation

| Parameter       | Value         |
|-----------------|---------------|
| $\mu_{\text{eff}}$ | 12.6 $\times$ 10$^4$ cm$^2$/V s |
| $L_{\text{eff}}/L_{\text{GR}}$ ratio | 2 |
| S.S (V/dec)     | 0.26          |
| $V_{\text{th}}$ (V) | 0.87        |
| $V_{\text{sys}}$ (V) | 0.3           |
| $R_{\text{C}}$ (Ω) | 7.9 $\times$ 10$^3$ |

Fig 2 (a) I–V curves under DC bias stress instability (BSI), (± 2 to ± 4 V). (b) Evolution of $V_{\text{th}}$ shift depending on both stress time and voltage extracted from maximum point of transconductance according to $\mu_{\text{eff}} = \frac{L_{\text{GR}}}{W C_{\text{GR}}} (W C_{\text{GR}})$, where $C_{\text{GR}}$ and $g_{\text{m}}$ are the gate capacitance per unit area and the transconductance, respectively. S.S was defined by relation of $S.S = \left(\frac{\partial \log g_{\text{m}}}{\partial V_{\text{GS}}}{\mid_{\text{max}}}\right)^{-1}$, $V_{\text{sys}}$ was extracted as the difference in $V_{\text{th}}$ between forwardly swept and reversely swept transfer characteristics, and contact resistance ($R_{\text{C}}$) was extracted by using Y-function method [18, 19]. Overall, with CYTOP encapsulation, decent electrical performance can be secured, which might be attributed to reduction of charge scattering associated with oxygen and OH$^-$ groups on the surface of MoTe2 surface in air [12, 16].

After evaluation of electrical properties, transfer characteristics and evolution of $\Delta V_{\text{th}}$ under various conditions of DC stress were measured to figure out $\Delta V_{\text{th}}$ behaviour depending on bias polarity (i.e. + or −), E-field strength (1–2 MV/cm), and effective stress time (1800 s). Figure 2a shows E-field strength effects on device instability from 1.0 to 2.0 MV/cm. As electric field strength was increased, $\Delta V_{\text{th}}$ increased accordingly. In addition, as shown in Figure 2b, the time dependence of $\Delta V_{\text{th}}$ for the positive bias stress (PBS) and negative bias stress (NBS) show excellent agreement with the stretched-exponential relationship, which is known to be involved in the charge trapping mechanism in various TFTs such a-Si [20] and a-IGZO TFTs [21]. The stretched-exponential equation of $\Delta V_{\text{th}}$ is defined as

$$\Delta V_{\text{th}}(t) = \Delta V_{\text{th0}} \left[1 - \exp \left(-t/\tau^\beta \right)\right],$$

where $\Delta V_{\text{th0}}$ is the $\Delta V_{\text{th}}$ at infinite time, $\tau = \tau_0 \exp(E_r/kT)$ denotes the characteristic trapping time of carriers where the thermal activation energy is given by $E_r = E_r \beta \exp(E_r/kT)$, $E_r$ is the average effective energy barrier that electrons in the MoTe2 need to overcome before they can enter the insulator, and $\tau_0$ is the thermal prefactor for emission over the barrier. The fact that $\Delta V_{\text{th}}$ is nicely fitted with Equation (1) can be attributed to the emission of trapped charge towards deep states in the bulk of MoTe2, for longer stress time ($\tau > \tau_0$). However, $\Delta V_{\text{th}}$ under positive stress is larger than negative stress in the same E-field strength range as shown in Figure 2b, implying that different electron and hole trapping behaviours are governed by bias polarity. To have a better understanding on bias polarity dependency, we have investigated device instability under pulse mode operation. Figure 3a shows an illustration to describe waveforms during DC and pulse mode operation. DC mode stress causes a continuous voltage stress, whereas pulse mode stress with an off period leads to a chance of detrapping for trapped charge carriers. With an independent DC and pulse stress, transfer characteristics and their $V_{\text{th}}$ shift were evaluated in Figure 3b,c. Under pulse mode stress with a duty cycle ranging from 0.1 to 0.7, $\Delta V_{\text{th}}$ was reduced, as compared to DC stress. Moreover, a duty cycle dependency on $\Delta V_{\text{th}}$ for both PBS and NBS is noticeably observed. Even though effective stress time is the same, lower duty cycle condition yields the larger off-period to detrap, leading to less $\Delta V_{\text{th}}$. Interestingly, as compared to NBS, $\Delta V_{\text{th}}$ of PBS is dramatically suppressed under pulse stress with any duty cycle. For the elucidation on the behind mechanism to cause duty cycle dependency, a normalised threshold voltage shift (i.e. $\Delta V_{\text{th}}$ (duty cycles)/$\Delta V_{\text{th}}$ (DC) (%)) is illustrated in Figure 3d. Compared to the gradual decrease in $\Delta V_{\text{th}}$ under NBS depending on duty cycles, the normalised $\Delta V_{\text{th}}$ behaviour under PBS shows sharp reduction by 20% under 0.7P duty cycle.

For further confirmation on key parameter of pulse stress, we extracted $\Delta V_{\text{th}}$ depending on frame time of pulse corresponding from 1 MHz to 1 Hz in Figure 4a. With a fixed bias stress voltage (2 MV/cm) for 900 s, $\Delta V_{\text{th}}$ under PBS shows clear frame time (pulse frequency) dependency for all range from 1 MHz to 1 Hz. On the other hand, NBS reveals insensitive shift behaviour according to frame time, as compared to that of PBS. These results suggest that electron trapping under PBS has fast recovery characteristics during off-period of the pulse. To understand the differences in bias polarity and frame time dependency on PBS and NBS, energy-band diagram models are suggested in Figure 4b. Under PBS, electrons can be trapped to interface traps or bulk traps in SiO2. However, for the case of NBS, hole trapping towards bulk trap in SiO2 is expected to be difficult, because barrier height between MoTe2 valence band and SiO2 defect band is larger (0.57 eV) than that of MoTe2 conduction and SiO2 defect band (0.18 eV) [22, 23], leading to less hole trapping. Thus, $\Delta V_{\text{th}}$ under DC stress is relatively strong in PBS, compared to NBS. In addition, the recovery characteristics after bias stress were examined to consider the detrapping process. As shown in Figure 4c, after PBS and NBS for 1800 s, immediate recovery monitoring was conducted without any bias stress. Figure 4d displays the recovery characteristics under PBS and NBS, respectively.
Fig 5 Threshold voltage shift for bipolar pulse stress. (a) Comparison of \( \Delta V_{th} \) under unipolar and bipolar stress. (b) Condition of bias polarity ratio to suppress \( \Delta V_{th} \).

normalised recovery characteristics for the absolute value of \( \Delta V_{th} \) in percentage scale, according to PBS and NBS. Thereafter, recovery time was extracted at the value of 63% of \( \Delta V_{th} \) (dotted grey line), which is according to the relationship of 1/e with the conventional meaning of time constant in engineering fields. PBS shows 150 s and NBS shows 900 s of recovery time constants. Furthermore, full recovery under PBS was shown after recovery for 3600 s, but not for NBS. Thus, compared to NBS, PBS has six times faster time constant in recovery and complete recovery was observed. These results indicate the time needed to detrapped trapped carriers during PBS, was much shorter than NBS. As a result, \( \Delta V_{th} \) was much suppressed under pulse mode operation in PBS, as compared with that of NBS.

For resolving device instability of undesirable \( V_{th} \) shift, bipolar pulse stress was introduced, from which trapping in one polarity of bias stress is relieved by the other polarity of bias stress as shown in inset of Figure 5b. \( \Delta V_{th} \) under positive and negative unipolar stress, their value of net summation, and bipolar stress (duty = 0.5P) are described in Figure 5a. Contrary to summated results of two kinds of unipolar stress, \( \Delta V_{th} \) under bipolar stress is perfectly suppressed. To confirm the duty cycle condition of bipolar stress (i.e. bias polarity ratio) for suppression of \( \Delta V_{th} \), device instability under various frame time was investigated. Interestingly, as shown in Figure 5b, duty cycle condition for perfect \( \Delta V_{th} \) suppression is different, according to a frame time. As frame time increase (i.e. frequency of pulse decrease), ratio of high level (+4) was reduced. This behaviour can be speculated from result of Figure 4a, where PBS shows clear frame time dependency for \( V_{th} \) shift. As a result, even for bipolar stress, PBS strongly affects for \( \Delta V_{th} \) than NBS as frame time decrease. Therefore, to have a balance, portion of high level (i.e. positive voltage) in bipolar pulse should be diminished for zero \( \Delta V_{th} \). Additionally, even with different bias voltage strength (i.e. \( \pm 4.5, +3 \) and \(-5 \) V), \( \Delta V_{th} \) could be successfully suppressed with optimised duty cycle depending on frame time. These results substantiate that bipolar stress mode could be effectively adopted, as compared with simple unipolar pulse stress with off-period for a practical application.

Conclusion: BSI in MoTe2 FETs was investigated under DC and pulse mode stress. After encapsulation of the MoTe2 FETs using CYTOP, charge trapping effects in air were intentionally decoupled with isolation of external effects related with oxygen (or/and moisture) as one of possible sources of the device instability. More severe \( \Delta V_{th} \) for DC PBS, as compared to DC NBS, is possibly attributed to different barrier heights between MoTe2 and SiO2 layer for conduction and valence band, which is experimentally substantiated by pulse frequency dependent test and time constant evaluation of recovery. Under pulse mode stress, PBS (or NBS) shows dramatic (or gradual) reduction of \( V_{th} \) shift. Furthermore, the frame time dependency on PBS in pulse mode was more clearly exhibited, compared with that of NBS. The BSI of MoTe2 FETs in pulse mode operation can be effectively controlled via bipolar stress with optimised duty cycle.

Acknowledgements: This work was supported by the Institute of Convergence Science and Technology Research Grant (2016-2333) of the Incheon National University.