Space Vector Modulation Method-based Common Mode Voltage Reduction for Active Impedance-Source T-Type Inverter

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ABSTRACT In recent years, many pulse width modulation techniques have been explored for three-level impedance-source inverters. Among them, a space vector modulation (SVM) technique using upper/lower shoot-through (UST/LST) insertion provides high voltage gain and satisfactory output voltage quality. This paper further introduces a new SVM control method to reduce the magnitude of common-mode voltage (CMV) without affecting the output voltage quality and voltage gain. With this approach, only small vectors with low magnitudes of CMV are adopted to synthesize an output voltage vector. The UST and LST states are also inserted to these small vectors to boost the DC-link voltage in high voltage gain and high modulation index. The comparison of CMVs between this strategy and other schemes is presented to demonstrate the effectiveness of the proposed method. The simulation and experiments are conducted to verify the accuracy of the theory.

INDEX TERMS Common-mode voltage reduction, quasi-switched boost inverter, three-level T-type inverter, space vector modulation.

I. INTRODUCTION
Conventional three-level T-type inverters (3L-T²I) have a simple structure and low conduction loss. They do not require many diodes or capacitors compared with other traditional configurations, such as three-level neutral-point-clamped inverters (3LNPCIs) or flying capacitor inverters. Because of these advantages, this topology provides superior low-voltage and medium-voltage applications, such as renewable energy systems or AC motor drives [1]–[3]. Nevertheless, this structure only provides a voltage buck capability, which is difficult to use in many applications requiring highly preferred AC output voltage from a low DC input power supply. To overcome this, two typical solutions were considered. The first one is to add a DC/DC boost converter to enhance the DC-link voltage before it is fed to the 3L-T²I [4]. The second is to use a low-frequency AC/AC transformer behind the inverter to achieve the desired AC output voltage. Furthermore, during operation, the conventional 3L-T²I does not accept the shoot-through (ST) state, which is generated when all switches in one or more phase legs are simultaneously opened [5]. This limitation can be resolved by applying a dead time for control signals before the switches are turned on. However, this approach can cause distortions at the output voltage [6].

Because of the foregoing problems, a Z-source inverter (ZSI) was introduced [7]. With one additional diode, two inductors, and two capacitors, the ZSI is known as a single-stage inverter with buck-boost capability and ST immunity. By placing the ZS network between the DC input source and two-level inverter, the ST state boosts the DC-link voltage without affecting output voltage and system reliability. However, this topology of an impedance-source network also has certain disadvantages, such as discontinuous input current or high voltage rating on capacitors [8], [9]. To overcome these limitations of the classical ZSI, quasi-ZSI (qZSI) was proposed. Although it uses the same number of inductors, capacitors, and diodes, the proposed structure creates a novel connection among these components [10]–
Due to the benefits of ZSI and qZSI, they have been validated by many applications, such as photovoltaic (PV) systems and grid connections [13]–[15]. To improve output voltage quality, the ZSI and qZSI are both integrated with a three-level inverter.

In [16], a novel connection between two identical ZS networks was investigated to provide a three-level voltage at the output of an intermediate network. This configuration used two isolated equal sources to feed two ZS networks. The 3LNPCI was installed after the ZS network to provide multilevel inverter characteristics. With the advantages of the connection reported in [16], a new combination involving only one ZS network with the 3LT²I was discussed in [17]. By applying split-DC input source feeding to the ZS network, this configuration provides three-level voltage to an output without requiring more ZS networks [16]. This topology can considerably reduce the required number of passive components without affecting the boost factor of the converter. As a result, size, cost, and control complexity are significantly improved. The 3LT²I was integrated with the qZS network in [9] and [18] not only to provide satisfactory output voltage quality but also to ensure that the benefits of qZS networks are derived. In this study, two identical qZS networks were connected in a cascade form to enhance the number of output voltage levels by merely utilizing one input source.

Although ZSI and qZSI afford advantages, both topologies also have disadvantages. They require numerous passive components (inductors or capacitors), they have a considerable inductor current ripple, and their boost factor and voltage gain are low. In [19], a qSB (quasi-switched boost) network was introduced to replace the ZS and qZS networks. Two diodes, one inductor, one capacitor, and one active switch comprise the qSB network. This type of intermediate network compared with the ZS and qZS networks reduces the required number of inductors and capacitors by one. The integration of this topology to the 3LNPCI was also proposed to enhance the number of output voltage levels [20]. This study used two identical qSB networks connected in a cascade form to generate three-level voltage output feeding to the 3LNPCI. In the new connection of the qSB network, one inductor was removed and feeding by a single DC source was introduced [21]–[23].

Common-mode voltage (CMV) is one of the critical problems of multilevel inverters. It causes leakage current, shaft voltage, bearing current, and electromagnetic interference [24], [25]. High leakage current through system ground causes system unreliability. The study in [26] has proposed a novel model predictive control for conventional 3LT²I to reduce the CMV and balance the neutral voltage. Two nearest vectors which have low CMV amplitude are used to produce reference vector. However, it is hard to apply this work to impedance-source network because the ST state is unable to be inserted in some region of space vector diagram. To reduce the CMV amplitude, the work in [27] used zero vector, medium vectors, and large vectors to generate the output voltage. This approach can reduce the CMV magnitude to twice of that in the conventional method. The method in [27] was also applied to qZSI in [9] and [28] to enhance the voltage gain of the inverter. In [9], an extra small vector with a low-magnitude CMV was used to balance the neutral voltage without affecting the CMV amplitude. However, the root mean square (RMS) value of CMV is slightly increased. In [9] and [28], the buck–boost capability is ensured by a full-ST state added to a zero vector. Nevertheless, the boost factor of these works is low. The work in [22] introduced an SVM method to eliminate the CMV using zero and medium vectors. Compared with [9] and [28], the study in [22] resulted in lower inductor current, higher voltage gain, and lower CMV. However, the output voltage quality of [22] is worse than those reported in [9] and [28]. Furthermore, the modulation index reported in [22] is limited and lower than those reported in [9] and [28]. The work in [23] enhanced the voltage gain, reduced the voltage stress on components, and provided a high output voltage quality compared with those in [9], [22], and [28]. However, the CMV magnitude is considerably larger than those reported in previous studies. In [23], the upper-ST (UST) and lower-ST (LST) states were applied to enhance the voltage gain. The study in [29] achieved the same voltage gain as that in [23] but with a lower CMV amplitude. However, the output voltage quality of the method in [29] was worse than that in [23].

To leverage the advantages of high voltage gain and satisfactory output voltage quality achieved in [23], this paper introduces a new pulse width modulation (PWM) technique based on an SVM to reduce the CMV magnitude. All vectors with high CMV magnitudes are removed from the space vector diagram, and those that produce low CMV are used to generate output voltage. In this scheme, small vectors are still used to insert UST and LST states. As a result, the output voltage quality is maintained compared with that in [23]. The remaining parts of this paper consist of five sections. Section II presents the inverter circuit and some operating states. The SVM method for reducing CMV is proposed in Section III. The overall comparison is discussed in Section IV. The PSIM simulation software and experiment prototype built in the laboratory were used to derive the simulation and experimental results presented in Section V. The summary is presented in Section VI.

II. INVERTER CIRCUIT

Fig. 1 presents the topology of 3L-qSB²I. In this figure, the conventional three-level T-type inverter is placed after the front-end active impedance-source network to ensure a three-level voltage output. In each leg, three-level voltage is ensured by four switches, \( S_{ij} \) \((j = 1, 2, 3, 4; x = a, b, c)\). State “\( P \)” denotes the value \(+V_{po}/2\) at the output pole voltage, \( V_{po} \), which is generated by activating switches \( S_{11} \) and \( S_{21} \). State “\( O \)” represents the value zero at the output pole voltage, which is ensured by turning on bi-directional switches \( S_{21} \).
S. When both switches, \( S_3 \) and \( S_4 \), are simultaneously triggered, the value of \(-V_{BP}/2\) is generated at the output. The DC-link voltage, \( V_{PN} \), at the input side of the T-type inverter circuit is generated by the qSB network, which consists of an inductor \( (L_b) \), two capacitors \( (C_P \) and \( C_N) \), two switches \( (S_P \) and \( S_N) \), and four diodes \( (D_1-D_4) \). The impedance-source network is fed by a single DC source, \( V_{dc} \), as shown in Fig. 1. By applying the front-end qSB circuit between the input voltage and inverter circuit, this topology can achieve ST immunity and buck–boost operation in a single-stage power conversion.

Similar to any single-stage inverters, this topology operates under two main modes: ST and non-ST (NST) modes (Fig. 2). As mentioned in [23], the ST mode consists of UST and LST modes, which are inserted to small vectors to enhance the boost factor and voltage gain of the inverter. In the UST mode, the inverter side can produce two states, “O” and “N,” which are ensured by capacitor \( C_N \). Capacitor \( C_P \) is disconnected from the main circuit, as shown in Fig. 2(e). Similarly, this \( C_P \) capacitor supports the inverter to produce states “P” and “O” under the LST mode, whereas capacitor \( C_N \) is disconnected from the power circuit. As shown in Figs. 2, (a)–(d), the NST mode consists of four sub-modes: NST modes 1–4, respectively. In particular, NST mode 3 is generated by triggering switches \( S_P \) and \( S_N \) of the impedance-source network, which stores energy to the inductor and enhances the boost factor. The on/off state of inverter switches is summarized in Table I.

### III. PROPOSED SVM SCHEME TO REDUCE CMV FOR 3LqSBT

The following equation yields the CMV:

\[
CMV = V_{GO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3}
\]

where \( V_{AO}, V_{BO}, \) and \( V_{CO} \) are the output pole voltages of the inverter side.

Based on (1), the CMV amplitude generated by each voltage vector of the inverter can be calculated, as summarized in Table II. According to the list, the largest CMV values are \( \pm V_{P2}/2 \), which are achieved by adopting zero vectors, [PPP] and [NNN]. The small vectors have four CMV values: \( \pm V_{P2}/6 \) and \( \pm V_{P0}/3 \). The large vectors also generated \( \pm V_{P2}/6 \). The medium vectors and zero vector, [OOO], have the zero CMV value.

In [23], all 12 small vectors are utilized to synthesize the output voltage vector; thus, the CMV is varied from \( +V_{P2}/3 \) to \(-V_{P2}/3\). Although the use of these small vectors enhances the boost factor and voltage gain by improving the ST duty ratio, it also increases the CMV.
In this study, small vectors with low CMV amplitudes ($\pm V_{po}/6$) are used with the zero vector ([0000]), medium vectors, and large vectors to reduce the CMV; this differs from that reported in [23]. Note that the use of these vectors does not limit the utilization of the ST duty ratio; thus, the advantage of high voltage gain of [23] is also leveraged in this work.

The space vector diagram of the proposed method is depicted in Fig. 3. In this figure, the space vector diagram is divided into six sectors (sectors I–VI). In each sector, four regions identify the sectors of the reference vector. Similar to the traditional SVM method, the reference vector is synthesized through three nearest vectors based on its location. The rest of this section presents details regarding vector selection, dwell time calculation, and ST insertion for the proposed SVM method.

A. DWELL-TIME CALCULATION AND SWITCHING SEQUENCE SELECTION

To analyze the proposed technique, the top of the reference vector is assumed to fall in region 2 of sector I, as highlighted in Fig. 3. As a result, three voltage vectors ($\bar{V}_{1}$, $\bar{V}_{2}$, and $\bar{V}_{7}$) are adopted to generate the output voltage vector, $\bar{V}_{ref}$. The following equation has been adopted:

$$\bar{V}_{ref} = \bar{V}_{1} \cdot t_{1} + \bar{V}_{2} \cdot t_{2} + \bar{V}_{7} \cdot t_{7},$$

where $\bar{V}_{ref}$: output voltage vector; $\bar{V}_{i}$: medium-voltage vector; $\bar{V}_{1}$, $\bar{V}_{2}$: small-voltage vectors; $T_{s}$: sampling period; and $t_{1}$, $t_{2}$, $t_{7}$: dwell times of $\bar{V}_{1}$, $\bar{V}_{2}$, and $\bar{V}_{7}$, respectively.

These voltage vectors are expressed by the following set of equations:

$$\bar{V}_{ref} = MV_{PN} / \sqrt{3}e^{j0},$$

$$\bar{V}_{1} = V_{PV} / \sqrt{3}e^{j0},$$

$$\bar{V}_{2} = V_{PV} / \sqrt{3}e^{j\pi/3},$$

$$\bar{V}_{7} = V_{PV} / \sqrt{3}e^{j\pi/2},$$

where $M$ is modulation index.

By substituting (3) to (2), the dwell times of these voltage vectors can be expressed as

$$t_{1} = T_{s} - 2MT_{s} \sin(\theta),$$

$$t_{2} = T_{s} - 2MT_{s} \sin(\pi/3 - \theta),$$

$$t_{7} = 2MT_{s} \sin(\theta + \pi/3) - T_{s}.$$  (4)

In conventional CMV reduction method for traditional voltage-source inverter, the switching sequence can be selected as [POO]-[PON]-[OON]. However, the unequal time durations of vectors [POO] and [OON] makes it hardly to insert UST/LST state. If try to use this conventional switching sequence, some disadvantages like worse inductor current profile, high amplitude of low frequency component of inductor current will appear. Thus, under the proposed method, the switching sequence for this region is selected as [PON]-[POO]-[OON]-[PON] and return, as shown in Fig. 4. The UST and LST states are inserted into N-type small [OON] and P-type small [POO] vectors, respectively. In both voltage vectors, phase B is also operated under state “O.” Thus, the insertion of UST and LST states into phase B is considered to reduce the number of commutations. The details of switching sequence and ST insertion are shown in Fig. 4. To leverage the advantages of the work in [23] in low inductor current ripple and high voltage gain, the switches ($S_{P}$ and $S_{N}$) of the impedance-source network are controlled and simultaneously turned on, as indicated by the yellow highlight in Fig. 4. Compared with the ST signal of the inverter side, this state is delayed by $T_{s}/4$. Both duty cycles of switches $S_{P}$ and $S_{N}$ are enhanced by coefficient $D_{0}$ to increase the boost factor.

The foregoing can similarly be applied to other regions and sections to calculate the dwell times and select the switching sequence. For example, consider sector I and region 4, shown in Fig. 3, three nearest vectors [POO], [PON], and [POO].
TABLE III
SWITCHING SEQUENCES OF PROPOSED SVM SCHEME

| Sector | Region | Switching sequence |
|--------|--------|--------------------|
| I      | 1      | [OOO]-[POO]-[PLO]-[DUN]-[OON]-[OON] and return |
|        | 2      | [PNN]-[POO]-[PLO]-[DUN]-[OON]-[OON] and return |
|        | 3      | [PNN]-[OPN]-[PLO]-[OON]-[OON]-[OON] and return |
|        | 4      | [PNN]-[OPN]-[PLO]-[DUN]-[OON]-[OON] and return |
| II     | 1      | [OOO]-[OPO]-[LOP]-[OON]-[OON]-[OON] and return |
|        | 2      | [OPN]-[OPO]-[LOP]-[OON]-[OON]-[OON] and return |
|        | 3      | [OPN]-[OPN]-[LOP]-[OON]-[OON]-[OON] and return |
|        | 4      | [PNN]-[OPN]-[LOP]-[OON]-[OON]-[OON] and return |
| III    | 1      | [OOO]-[OPO]-[OPN]-[NOO]-[NOO]-[NOO] and return |
|        | 2      | [NOP]-[OPO]-[OPN]-[NOO]-[NOO]-[NOO] and return |
|        | 3      | [NOP]-[OPN]-[OPP]-[NOO]-[NOO]-[NOO] and return |
|        | 4      | [PNN]-[OPP]-[OPP]-[NOO]-[NOO]-[NOO] and return |
| IV     | 1      | [OOO]-[OPP]-[OOP]-[OON]-[OON]-[OON] and return |
|        | 2      | [NOP]-[OPP]-[OOP]-[OON]-[OON]-[OON] and return |
|        | 3      | [NOP]-[OPN]-[OOP]-[OON]-[OON]-[OON] and return |
|        | 4      | [PNN]-[OPP]-[OOP]-[OON]-[OON]-[OON] and return |
| V      | 1      | [OOO]-[OOP]-[LOP]-[OUN]-[OON]-[OON] and return |
|        | 2      | [ONP]-[OOP]-[LOP]-[OUN]-[OON]-[OON] and return |
|        | 3      | [ONP]-[OPN]-[LOP]-[OUN]-[OON]-[OON] and return |
|        | 4      | [OPN]-[OPP]-[LOP]-[OUN]-[OON]-[OON] and return |
| VI     | 1      | [OOO]-[POO]-[POL]-[OUN]-[OON]-[OON] and return |
|        | 2      | [PNO]-[POO]-[POL]-[OUN]-[OON]-[OON] and return |
|        | 3      | [PNO]-[PPN]-[POL]-[POO]-[PNP]-[PNP] and return |
|        | 4      | [PNN]-[PPN]-[POL]-[POO]-[PNP]-[PNP] and return |

U: UST state, L: LST state.

D. STEADY-STATE ANALYSIS

The key waveform of the 3L-qSBT2I under proposed control method is shown in Fig. 5. It can be seen that the inductor voltage is kept at \( V_{dc} \) for both UST and LST states. Thus, the boost factor is not affected when the time intervals of UST and LST states are unequal. In steady-state, the average value of inductor voltage is zero. Thus, the capacitor voltages, \( V_{CP} \) and \( V_{CN} \), can be calculated using the following equation. Note that \( V_{CP} = V_{CN} \) the capacitor voltages are assumed as constant during operation.

\[
V_{CP} = V_{CN} = \frac{V_{dc}}{2} - 3D_{ST} - D_0, \tag{5}
\]

where \( V_{CP}, V_{CN} \) capacitor voltages of \( C_P \) and \( C_N \); \( V_{dc} \): DC input source of 3L-qSBT2I; \( D_{ST} \): ST duty ratio; and \( D_0 \): extra duty ratio of impedance-source network switches (\( S_P \) and \( S_N \)).

The following equation relates \( D_{ST} \) to \( D_0 \):

\[
D_{ST} \leq D_0 \leq 1 - D_{ST} \tag{6}
\]

The peak value of the output load voltage can be calculated through the modulation index (\( M \)) and DC-link voltage as follows:

\[
V_{x,peak} = \frac{2}{\sqrt{3}} \cdot \frac{M \cdot V_{PN}}{2} = \frac{2}{\sqrt{3}} \cdot \frac{MV_{dc}}{2 - 3D_{ST} - D_0}, \tag{7}
\]

where \( V_{x,peak} \): peak value of output voltage; \( M \): modulation index; and \( V_{PN} \): dC-link voltage.

Because the ST state is inserted to small vectors, \( D_{ST} \) can be calculated through \( M \) using the following equation [23]:

\[
\begin{align*}
M & \leq 1 \\
M + D_{ST} & \geq 1
\end{align*} \tag{8}
\]

C. NEUTRAL VOLTAGE BALANCED CONTROL

The neutral voltage imbalanced issue can be addressed by adjusting the extra duty ratio \( D_0 \) of switches \( S_P \) and \( S_N \) of impedance source network. In detail, the time interval of NST mode 1 and NST mode 2 shown in Figs. 2(a) and 2(b) are used to balance neutral voltage. As shown in Fig. 2(a), when NST mode 1 is adopted, the capacitor \( C_P \) is discharged, whereas capacitor \( C_N \) is charged. The result is that the \( C_P \) voltage is decreased while \( C_N \) voltage is increased. In NST mode 2, shown in Fig. 2(b), the \( C_P \) voltage is increased while \( C_N \) voltage is decreased. In general, the time intervals of these modes are equal which are determined by \( (D_0 - D_{ST})T_2/2 \). In order to balance neutral voltage, the time intervals of NST mode 1 and 2 are redefined as \( (D_1 - D_{ST})T_2/2 \) and \( (D_2 - D_{ST})T_2/2 \), respectively, where \( D_1 \) and \( D_2 \)
The overall implementation of the proposed SVM method is shown in Fig. 6. Firstly, three desired output voltages are transfer to $\alpha\beta$ axis to determine reference vector by using $abc/\alpha\beta$ transformation, as shown in Fig. 6. Based on location of reference vector, three nearest vectors are determined to control output voltages. Note that only vectors, which have low CMV shown in Fig. 2, are selected. Secondly, the dwell-times of candidate vectors are calculated by the same way shown in section III.A. Furthermore, the P-type or N-type small vector of candidate vectors helps to determine whether UST or LST state is selected. Thirdly, the switching sequence has been determined, which shown in Table III. The capacitor voltage balanced method is obtained by the extra duty ratios $D_1$ and $D_2$ of switches $S_F$ and $S_N$. The detail of this method is shown in section III.C and presented by block diagram in Fig. 6. All these steps are enough to implement the proposed SVM control strategy.

### IV. COMPARISON STUDY

The introduced PWM method has been considered for comparison with other single-stage topologies and methods. The overall comparison is summarized in Table IV. Among the works listed in the table, the proposed method and SVM method in [23] are superior in using the modulation index, $M$. With the same value of $M$, the maximum values of the ST duty ratio ($D_{ST}$) of the proposed method and the technique presented in [23] are found to be twice those of the other methods. This advantage supports the proposed method in improving the component voltage rating and output voltage quality, as detailed in [23] and [29]. The 3L-qZSI in [9] has the least boost factor and voltage gain leading to the generation of the high DC-link voltage, $V_{DC}$. For the 3L-qSBT-I topology, the method in [22] results in the smallest voltage gain (Table IV). This limit is explained by the utilization of only zero and medium vectors in the operation. The method in [29] yields the largest boost factor, but the work adopts a small modulation index [29]. Consequently,
the same voltage gain is achieved compared with that in [23], as demonstrated in [29].

As shown in Fig. 7(a), the THD value of the proposed method and method in [23] is the best. It can be explained that the used of small vectors helps to increase the quality and reduce the THD value of output voltage. In detail, the proposed SVM method with unipolar form of output line-to-line voltage compared with bipolar form of method in [22], produces high output voltage quality than [22], obviously. Moreover, the high voltage gain is applied for this method, it results in high modulation index utilization. This is also one of the reasons to explain for the high quality of output voltage. Although the method in [29] has the same voltage gain and modulation index, the use of zero vector to insert full-ST state results in high THD value of output voltage compared to the proposed method.

As summarized in Table IV, the method in [22] has the lowest CMV magnitude. However, the low voltage gain and the utilization limit of the modulation index are the two main drawbacks of this method. The method presented in [23] yields the largest CMV amplitude (from $V_{PN}/3$ to $+V_{PN}/3$) because all 12 small vectors are used. The methods in [9] and [29] and the proposed technique can reduce the peak CMV value to twice of that in [23] by removing the small vectors, which have large CMV values resulting from the switching sequence. The ratio between the CMV RMS to the input voltage is presented in Fig. 7(b). The figure indicates that the CMV produced by the proposed method is reduced compared with those generated by the methods in [9] and [23]. Although the CMV of the proposed method is larger than those of [22] and [29], the better output quality shown in Fig. 7(a) is among the main advantages of this method.

In summary, the main contribution of this study is the reduction in the CMV magnitude without affecting the voltage gain and modulation utilization compared with [23]. Moreover, the high output voltage quality is one of the important characteristics of this work.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The proposed SVM method is verified through simulation and experiments; the parameters used are listed in Table V. The simulation is implemented using PSIM software. The boost inductor value is 3 mH, and the two capacitors of the impedance-source network have a value of 2000 µF. The selected values for the three-phase low-pass filter values to generate approximately 1 kHz of cut-off frequency are 3 mH and 10 µF. The selected theoretical output load voltage is 110 V RMS/50 Hz. The three-phase 40-Ω resistive load is considered to test the proposed scheme in two cases (i.e., two input voltage values): 1) 200-V and 2) 100-V. To achieve 110 V RMS at the output load voltage, the set modulation index, $M$, and ST duty ratio, $D_{ST}$, are 0.92 and 0.16, respectively. Under the 200-V input voltage, 0.16 is the selected value for the extra coefficient, $D_{0}$; 0.84 is selected for $D_{0}$ when adopting the 100-V input voltage. The simulation results are shown in Figs. 8 and 9.

Fig. 8 shows the simulation results for the 200-V input voltage. In this case, the minimum voltage gain is obtained by setting 0.16 as the value for both coefficients, i.e., $D_{ST}$ and $D_{0}$. With the above values, the capacitor voltages are boosted to approximately 147-V, as shown in Fig. 8(a). The two capacitor voltage values are balanced. These capacitor voltage values result in the 294-V DC-link voltage, as presented in Fig. 8(a). Note that the DC-link voltage is a pulse wave and varies from 147-V to 294-V because the UST and LST states are used instead of the FST state. The top of the output line-to-line voltage, $V_{AB}$, is varied from 0 to the peak DC-link voltage value; its Fast Fourier Transform (FFT) spectrum is shown in Fig. 8(b). The peak value of the first-order harmonic is 269-V. The amplitude of high-frequency harmonic spectrum is mitigated by applying an LC (inductor–capacitor) filter, as shown in the FFT spectrum of the output current in Fig. 8(b). Thus, the output load current is a sinusoidal waveform whose peak value is 3.88-A. The THD values of $V_{AB}$ and $I_{A}$ are 32.29% and 0.345%.

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**TABLE V**  
SIMULATION AND EXPERIMENTAL PARAMETERS

| Components                  | Values                      |
|-----------------------------|----------------------------|
| DC input source $V_{dc}$    | 100 V ÷ 200 V              |
| Output voltage $V_{0,RMS}$  | 110 V RMS                  |
| Output frequency $f_{o}$    | 50 Hz                      |
| Switching frequency $f_{s}$ | 5 kHz                      |
| ST duty cycle $D_{ST}$      | 0.16                       |
| Extra coefficient $D_{0}$   | 0.16 ÷ 0.84                |
| Modulation index $M$        | 0.92                       |
| Boost inductor $L_{b}$      | 3 mH/20 A                  |
| Capacitors $C_{F} = C_{S}$  | 2000 µF/400 V              |
| LC filter $L_{F}$ and $C_{F}$ | 3 mH and 10 µF          |
| Resistor load $R$           | 40 Ω                       |

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**FIGURE 8.** Simulation results for proposed method under 200-V input source.
respectively. The average value of the current in inductor $L_B$ is 4.59 A, as shown in Fig. 8(a). Figure 8(c) shows the magnified waveforms of $I_{LB}$, $V_{SP}$, $V_{SN}$, and DC-link voltage $V_{PN}$. The voltage stresses of switches $S_P$ and $S_N$ are equal to the capacitor voltage. The inductor current frequency (20 kHz) is four times greater than the switching frequency.

Fig. 9 shows the simulation results for the 100-V input voltage. In this case, to achieve 110 V $V_{RMS}$ at the output load voltage, the maximum voltage gain is adopted. The extra coefficient, $D_0$, is set to 0.84 instead of 0.16. Two capacitor voltage values remain boosted at approximately 147 V from the 100-V input source, as illustrated in Fig. 9(a). The 294-V remains at the DC-link voltage and peak value of the output line-to-line voltage, $V_{AB}$. From the FFT spectrum of $V_{AB}$ and $I_A$, the calculated THD values of these waveforms remain as 32.29% and 0.374%, respectively. The average inductor current value is 9.2 A. The frequency of inductor current is also 20 kHz, as shown in Fig. 9(c).

The simulation result of neutral voltage balanced control are shown in Fig. 10. The unbalanced neutral-point voltage causes distortion at output line to line voltage, which results in high amplitude of low frequency components (100Hz and 200Hz) of $V_{AB}$. After applying the balanced control method, the different between two capacitor voltages is very small, which significantly reduces the magnitude of low frequency components of output line to line voltage.

The CMV comparison between the method in [23] and the proposed method is shown in Fig. 11. It can be seen that the boost characteristics of impedance-source network are the same for both method in [23] and the proposed SVM method, which is shown in DC-link voltage waveform, $V_{PN}$. The peak-value of $V_{PN}$ is 294V, and $V_{PN}$ waveform is varied from 147 V to 294 V because of adopting UST/LST insertion. The output line-to-line voltages, $V_{AB}$, have the same THD values which are 32.29% for both methods. Thus, it can conclude that the proposed method maintains the output voltage quality compared to [23]. Moreover, the peak-to-
peak value of CMV of proposed method is a half less than that of conventional method in [23]. The RMS values of CMV with the proposed method and strategy in [23] are 35.8 V_{\text{RMS}} and 46.4 V_{\text{RMS}}, respectively. The proposed method reduces 22.8% RMS of CMV compared to the method in [23]. The FFT spectrums of CMV are shown in Fig. 11. It can be seen that, with smaller RMS value of CMV, the proposed method can reduce the amplitude of high-frequency component of CMV compared to the work in [23], significantly. The investigation about CMV of method in [23] and the proposed method with variation of modulation index is shown in Fig. 12. It can be founded that the proposed method always has smaller RMS value of CMV compared to [23]. Both methods have max value of CMV at 0.5 of modulation index because the time interval of small vector is maximized in this case [9], [22], [28].

B. EXPERIMENTAL RESULTS
Experiments for validating the proposed SVM method have been conducted in a laboratory. The parameters are the same as those used in the simulation; both 100-V and 200-V input voltages are considered to test the inverter. The experimental results are presented in Figs. 13, 14 and 15.

Under the 200-V input source, the two capacitor voltages, $V_{CP}$ and $V_{CN}$, are boosted to 140 and 141 V, respectively, as shown in Fig. 13(a). The input current is continuous, and its
measured average value is 4.78 A. The peak value of DC-link voltage, $V_{\text{PN}}$, is the sum of the two capacitor voltage values, i.e., approximately 280 V, as shown in Fig. 13(b). In this figure, the $V_{\text{PN}}$ waveform varies from 140 to 280 V because the proposed method adopts the insertion of the UST and LST states. The output line-to-line voltage, $V_{\text{AB}}$, varies from $-V_{\text{PN}}$ to $+V_{\text{PN}}$, it has five voltage levels, as illustrated in Fig. 13(b). The output load current is a sinusoidal wave, and its RMS value is 2.59 A_RMS. The magnified waveforms of the inductor current, $i_{\text{LB}}$, the voltages values of switches $S_P$ and $S_N$, and the DC-link voltage are shown in Fig. 13(c). This figure indicates that the operating frequency of the inductor is four times larger than the switching frequency. The high operating frequency reduces the inductor current ripple compared with that yielded by the traditional PWM control method. In Fig. 13(c), the inductor current increases and decreases linearly. It increases in the UST/LST state when the DC-link voltage is half of its peak value. Moreover, when both switches (i.e., $S_P$ and $S_N$) are activated, the inductor also stores energy.

Under the 100-V DC input source, the extra duty ratio, $D_0$, increases to 0.84 to maintain the output voltage. In this case, the two capacitor voltages, $V_{\text{CP}}$ and $V_{\text{CN}}$, reach 126 and 128 V, respectively. The average inductor current value is 9.35 A, as shown in Fig. 14(a). The DC-link voltage can reach 254 V in the NST mode, as shown in Fig. 14(b). The peak value of the output line-to-line voltage is also 254 V. The RMS value of the output load current is 2.52 A_RMS. With the larger duty ratio, $D_0$, compared with that in case 1, the on periods of switches $S_P$ and $S_N$ also increase, as shown in Fig. 14(c).

The FFT spectrum of output load current $I_A$ and output line-to-line voltage $V_{\text{AB}}$ are presented in Fig. 15. Based on these spectrums the THD value of $V_{\text{AB}}$ can be calculated as 45.9%. The high frequency component of output voltage is mitigated by a LC filter, thus, the output load current is sinusoidal waveform, and its THD value is 2.15%.

The proposed method and that in [23] are implemented to prove the effectiveness of the proposed technique to achieve CMV reduction; the results are shown in Fig. 16. In this figure, the proposed method can reduce the peak CMV value by twice the CMV value of the conventional method without affecting the output line-to-line voltage. As a result, the quality of the output voltage is maintained. The RMS values of CMV of the proposed and conventional methods are 36.7 and 48.4 V_RMS, respectively. This shows that the proposed method can reduce the RMS voltage of CMV by 24.17% compared with the traditional control scheme.

VI. CONCLUSION

A new SVM control method is introduced for the 3L-qSBT3I to reduce the peak-to-peak CMV value. With this approach, the small vectors with small CMV values are used in addition to the zero, medium, and large vectors to generate the output voltage vector. The UST and LST vectors are utilized with traditional vectors to boost the DC-link voltage. Because the UST and LST vectors are added to the small vectors, the inverter achieves high voltage gain. Under the proposed SVM method, some results are obtained: 1) the high voltage gain is achieved with some benefits such as good inductor current profile and low component voltage rating, 2) output voltage quality is improved when compared to previous modulation methods, 3) the peak-to-peak value of CMV is reduced by twice of that in conventional SVM method, and 4) the magnitude of high frequency component of CMV is reduced, which reduces the negative impact on the system. The accuracy of the introduced method has been validated by simulation and experiment. The simulation and experimental results show that with the proposed SVM scheme, the peak CMV is reduced to half of that of the conventional method. The RMS value reduction of CMV under the proposed method is around 24.17%.

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