A wide-range and fast-locking all digital SARDLL for DVFS SoCs

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Abstract: A wide-range and fast-locking all digital successive approximation register-controlled delay-locked loop (SARDLL) is presented for dynamic voltage/frequency scaling (DVFS) system-on-chips (SoCs). The proposed SARDLL eliminates the harmonic lock problem and zero-delay trap problem by using the improved resettable digitally controlled delay line (DCDL) and shortens the lock time by adopting the 2-b successive-approximation-register (SAR) algorithm. The proposed 6-bit SARDLL is designed using the TSMC 65 nm CMOS low power cell library. The layout’s active area is 91 µm × 91 µm. The post-layout simulation results show that the proposed SARDLL can operate from 250 MHz to 2 GHz. Its lock time is constant 9 cycles of the input clock. The power consumption is estimated to be 0.72 mW at 1.2 V supply voltage and 2-GHz clock frequency.

Keywords: de-skew buffer, fast-locking, all digital delay-locked loop, SAR controller, harmonic lock, zero-delay trap, resettable digitally controlled delay line, system-on-chip, dynamic voltage/frequency scaling

Classification: Integrated circuits

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1 Introduction

With the rapid advances in complementary metal oxide semiconductor (CMOS) technologies, the complexity and operating frequency of the SoCs are increased dramatically, resulting in increasing demand for low power design methods. DVFS has been proved to be one of the most efficient techniques for realizing low power SoCs. For example, in a multicore SoC, a DVFS unit dynamically adjusts the supply voltage and the operating frequency of the processors according to the device’s mode of operation. Since the clock rate is changed, it will be important to resynchronize all subsystems as soon as possible after the DVFS unit adjusting the system clock [1]. Hence, a low-power, high-performance and fast de-skew circuit is required for clock synchronization in low power SoCs with DVFS method. Phase-locked loops (PLLs) and delay-locked loops (DLLs) are widely used in the SoCs to serve as the de-skew circuits. In general, DLLs are more attractive than PLLs in clock synchronization applications because of their unconditional stability and better jitter performance [2].

When DLLs are used as the de-skew circuits in DVFS systems, three problems are raised: first, the DLL should work in a wide operating frequency range. Second, the acquisition time, i.e., the lock time of the DLLs should be as short as possible [1, 3]. Third, the DLL should have no harmonic lock problem and zero-delay trap problem. Compared with analog and mixed-mode DLLs, the digital DLLs are suitable for DVFS SoCs, due to the fast response time, the compatibility for system integration and the insensitivity to the process, voltage, temperature (PVT) variations [1].

Among the digital DLL schemes, the SAR scheme seems to be a better choice in consideration of the lock time and the hardware complexity [4, 5, 6, 7]. However, in wide-range applications, the conventional SAR-based all digital DLL (ADDLL) may suffer from harmonic lock problem and zero-delay trap problem. These two problems have to be solved in designing the SAR-based ADDLL for DVFS SoCs [1, 5].

To satisfy the requirements of the DVFS SoCs, a novel all digital SARDLL scheme is proposed and implemented in a cell-based design flow in this paper. It uses improved resettable DCDLs to solve the harmonic lock problem and the zero-
delay trap problem [1, 7]. And the 2-b SAR scheme proposed in [8, 9], which determines two bits of the control word of the SAR controller at very step, is adopted to shorten the lock time.

This paper is organized as follows. Section 2 presents the proposed all digital SARDLL. Section 3 shows the post-layout simulation results of the proposed all digital SARDLL. Finally, some conclusions are summarized in Section 4.

2 System and circuits description

Fig. 1 depicts the block diagram of the proposed all digital SARDLL with 6-bit control word \(b[5:0]\). And an example timing diagram of the proposed all digital SARDLL is illustrated in Fig. 2. Three cycles of the input clock \(c_{\text{kin}}\) are grouped

Fig. 1. The block diagram of the proposed SARDLL.

Fig. 2. Example timing diagram of the proposed all digital SARDLL.

Fig. 1 depicts the block diagram of the proposed all digital SARDLL with 6-bit control word \(b[5:0]\). And an example timing diagram of the proposed all digital SARDLL is illustrated in Fig. 2. Three cycles of the input clock \(c_{\text{kin}}\) are grouped
as a period. Two bits from \( b[5:0] \) are determined in a three-cycle period. At very three-cycle period, the input clock \( \text{clkin} \) needs to be compared with 3 clock phases. Hence, the delay line is required to output 3 comparing clocks, \( \text{clk1}, \text{clk2}, \text{clk3} \), that are equally spaced in phase [9]. The timing controller shown in Fig. 3 is used to generate the required control signals. In the beginning, the \text{start} \text{signal initializes the system. The control word } b[5:0] \text{ and } d[1:0] \text{ of the 2-b SAR controller are initialized as “010000” and “00”, respectively. The delay of the DCDL1, DCDL2 and DCDL3 is all } 1/4D_{\text{max}} \text{, where } D_{\text{max}} \text{ is the maximum delay of the DCDL1. In the first cycle of the clkin, a short-pulse } \text{clk-edge} \text{ is generated and fed into the improved resettable DCDLs. At the same time, the } \text{sample-range} \text{ signal is set to high. If the } \text{clk-edge} \text{ does not show up at } \text{clkout or } \text{clk1} \text{ in the high } \text{sample-range} \text{ duration, the } \text{comp1}, \text{comp2} \text{ and } \text{comp3} \text{ of the samplers are kept logic low. In the second cycle, the } \text{rst_dcdl} \text{ signal is pulled up to reset the improved resettable DCDLs to ensure that no residual } \text{clk-edge} \text{ remains in the delay line. The } b[5:0] \text{ and } d[1:0] \text{ are also both adjusted to “000100” and “01” in this cycle, respectively. The delay of the DCDL1, DCDL2 and DCDL3 is all } 1/16D_{\text{max}} \text{. A short-pulse } \text{rstdff} \text{ signal is generated in the beginning of the third cycle to reset the samplers and the flip-flops in the timing controller such that the three-cycle period starts over again. In the fourth cycle, the second } \text{clk-edge} \text{ pulse is generated and fed into DCDLs. In the second high } \text{sample-range} \text{ duration, the } \text{clk-edge} \text{ shows up at } \text{clk1}, \text{ but does not show up at } \text{clk2} \text{ and } \text{clk3}. \text{ Thus, } \text{comp1} \text{ is changed to high, and } \text{comp2}, \text{comp3} \text{ are kept logic low. After the rising edge of the } \text{clksar}, \text{ which is the clock of the 2-b SAR controller, in the fifth cycle of the clkin, the } b[5:0] \text{ is locked to “000100”. The DCDLs are reset similarly in the fifth clkin cycle. Samplers and flip-flops of the timing controller are reset in the sixth clkin cycle to restart another three-cycle control loop. When all bits of } b[5:0] \text{ are determined, the } \text{stop} \text{ signal is set to logic high to switch the } \text{DCDL_in} \text{ signal from } \text{clk-edge} \text{ to } \text{clkin} \text{ such that the proposed all digital SARDLL works in the normal mode.}

![Fig. 3. Schematic of the timing controller.](image)

### 2.1 Resettable digitally controlled delay line

In essentially, the result causes harmonic lock is the residual input clock in the conventional DCDL when the delay of DCDL is longer than one cycle of the input clock [6]. So, an improved resettable DCDL scheme, which is sketched in Fig. 4, is
proposed based on [1] and [7] to clear the residual input clock in very three-cycle period. And then the harmonic lock problem and zero-delay trap problem are solved effectively [1]. Compared with the counterparts in [1] and [7], the improved resettable DCDL scheme whose delay cell is shown in the dash line in the Fig. 4 can increase the maximal operating frequency and reduce the hardware overhead. The $scode$ and $scode_{\text{bar}}$ are decoded from $b[5:0]$. When $scode$ is set to logic high, the $DCDL_{\text{in}}$ feeds into DCDL1 from the corresponding delay cell. All the delay cells are reset to logic low when the $\text{rst}_{\text{dcdl}}$ signal is pulled up to logic high.

![Fig. 4. The schematic of the improved resettable DCDL.](image)

### 2.2 Hardware implementation of the 2-b SAR controller

The conventional SAR controller in [4] determines one bit of the control word at every step. Therefore, the theoretic lock time is $N$ cycles of the input clock for the $N$-bit SAR controller. The 2-b SAR scheme determines two bits of the control word at every step to shorten the theoretic lock time to $N/2$ cycles of the input clock for the $N$-bit SAR controller at expense of added DCDLs.

![Fig. 5. (a) The 6-bit SAR circuit with 2-b SAR algorithm. (b) The internal structure of the SAR units and associated truth tables.](image)

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The hardware implementation of the 2-b SAR controller is depicted in Fig. 5(a). The SAR units are divided into even and odd units. The samplers in
Fig. 1 are simple D-type flip-flops (DFFs) that sample the \textit{sample range} by the three comparing clocks, \textit{clk1}, \textit{clk2} and \textit{clk3} and output \textit{comp1}, \textit{comp2} and \textit{comp3}, respectively. The \textit{comp} input for the odd SAR units is \textit{comp2}, while the \textit{comp} input of the even SAR units is \textit{even unit comp} which is given by

$$
\text{even unit comp} = \text{comp}_2 \cdot \text{comp}_3 + \overline{\text{comp}_2} \cdot \text{comp}_1
$$

(1)

The internal structure of the SAR units and associated truth tables are shown in the Fig. 5(b).

### 3 Simulation results

The proposed all digital SARDLL shown in Fig. 1 is designed using TSMC CMOS 65 nm LP technology. The layout active area is $91 \mu m \times 91 \mu m$. The HSIM® is chosen as the simulator to carry out the post-layout transistor level simulation at the conditions of typical corner, 25°C and 1.2 V power supply. The simulation results indicate that the operating frequency range is 250 MHz–2 GHz without harmonic-locking and zero-delay trap, the lock time is constant 9 cycles of the input clock \textit{clkin}, and the power dissipation is 0.72 mW@2 GHz. The simulation results are shown in Fig. 6(a), (b), (c) for 250 MHz, 1 GHz and 2 GHz of input clock \textit{clkin}, respectively.

Table I shows the comparison between this paper and the previous SAR-based ADDLLs. Where, $N$ is the size of the control word of the SAR controller. The proposed SAR ADDLL in this paper has the highest operating frequency, smallest hardware area, lowest power consumption.

| CMOS technology | [1] | [9] | [10] | This work |
|-----------------|-----|-----|------|-----------|
| Active area     | 0.09 mm$^2$ | 0.009 mm$^2$ | 0.02 m$^2$ | 0.0083 mm$^2$ |
| Maximal frequency | 1.2 GHz | 0.8 GHz | 1 GHz | 2 GHz |
| Power supply    | 1.8 V | 1.2 V | 1.2 V | 1.2 V |
| Power consumption | 16.2 mW@1.2 GHz | 0.89 mW@0.8 GHz | 3.6 mW@1 GHz | 0.72 mW@2 GHz |
| # of SAR bits   | 11 | 6 | 11 | 6 |
| Lock time       | 3*N | N | 4*N-2 | 3*N/2 |

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### 4 Conclusions

This paper presents a wide-range and fast-locking all-digital SARDLL without harmonic lock problem and zero-delay trap problem for DVFS SoCs. The proposed SARDLL can work from 250 MHz frequency to 2 GHz frequency. The lock time is constant 9 cycles of the input clock at all working frequency. All design units of the SARDLL are first described in Verilog HDL, and then mapped to silicon using the
TSMC 65 nm CMOS LP standard cell library. The cell-based digital IC design flow is demonstrated to design a SAR-based ADDLL successively. Therefore, a lot of man hours are saved in the design phase compared with the full-custom design flow.

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**Fig. 6.** (a) The frequency of the input clock is 250 MHz. (b) The frequency of the input clock is 1 GHz. (c) The frequency of the input clock is 2 GHz.