Evolution in Surface Morphology of Epitaxial Graphene Layers on SiC Induced by Controlled Structural Strain

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The evolution in the surface morphology of epitaxial graphene films and 6H-SiC(0001) substrates is studied by electron channeling contrast imaging. Whereas film thickness is determined by growth temperature only, increasing growth times at constant temperature affect both internal stress and film morphology. Annealing times in excess of 8-10 minutes lead to an increase in the mean square roughness of SiC step edges to which graphene films are pinned, resulting in compressively stressed films at room temperature. Shorter annealing times produce minimal changes in the morphology of the terrace edges and result in nearly stress-free films upon cooling to room temperature.

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The remarkable electronic properties of graphene have shown promise for use in high performance electronic devices [1]. However, large area fabrication processes for graphene devices have not yet been developed. Epitaxial graphene, which shares key electronic properties of free-standing graphene, has emerged as an attractive alternative to the layer-by-layer exfoliation process [2, 3, 4, 5, 6, 7], because of its potential for scalability and for integration with Si-based electronics. Epitaxial graphene layers were shown recently to display blueshifts in the frequencies of their optical phonons at room temperature [8, 9, 10], which are indicative of the presence of lattice strain in the epilayer. This strain is explained by the large difference in the thermal expansion coefficients of graphene and SiC which is nearly constant from the synthesis to room temperature [8, 9].

Strained heterostructures have received a significant amount of interest in the past because of the wide ranging implications of strain, from the ability to engineer bandgaps in silicon-based materials for electronic device fabrication [10] to the constraints it poses on the growth of defect-free heterostructures [11]. It is therefore of interest to investigate some of the consequences of the presence of strain on epitaxial graphene film properties and on epilayer quality. It is known that the amount of residual strain at room temperature in epitaxial graphene is tunable by adjusting the annealing time [8]. In this paper we investigate the evolution in the morphology of graphene domains pinned at SiC terrace edges with increased annealing time. An increase in the step edge mean square roughness is observed with annealing time. The evolution in step morphology is proposed as a mechanism for the relief of structural strain in the graphene epilayer, which is, in turn, controlled by the annealing time.

Graphene epilayers were produced by thermal annealing the Si-face of 6H-SiC single crystals with (0001) orientation (CREE Research, Inc.). 6H-SiC samples were first prepared ex vacuo by high temperature annealings in hydrogen atmosphere to obtain a regularly stepped surface, as described elsewhere [8]. The stepped surface is necessary to monitor the morphological evolution of epitaxial graphene as it grows off SiC terrace edges [12]. The resulting SiC surface was characterized by a sharp ($3 \times 3$) low-energy electron diffraction (LEED) pattern. Graphene layers were grown by annealing the SiC substrate in ultrahigh vacuum (UHV) for varied times (ranging from 1 to 30 minutes); subsequently, the substrate was cooled down to room temperature at the rate of $\leq 1$ Ks$^{-1}$. The same growth temperature $T_G = 1250 \pm 20$ C was used, in order to obtain the same number of graphene epilayers [2, 6]. The film thickness was measured after the annealing by monitoring the C:Si Auger electron spectroscopy (AES) ratio [6]. In all data presented here on the graphitized substrate, the C:Si ratio was $7 \pm 1$, corresponding to $1.0 \pm 0.2$ monolayer (ML). At room temperature, the resulting graphene layers possess a threefold symmetric LEED pattern superimposed on the $\{6\sqrt{3} \times 6\sqrt{3}\}R30^\circ$ pattern of the SiC surface reconstruction [2, 13]. Surface morphology was monitored with electron channeling contrast imaging (ECCI), through a low-voltage scanning electron microscope (NovelX My-SEM), operating at 1kV in topographic mode. The ability to directly image atomic terrace edges with ECCI has been demonstrated recently for crystalline SiC surfaces [14].

Figure 1(a) shows ECCI images of the SiC surface after the high temperature annealing in hydrogen ambient, but before the high temperature graphitization in UHV. Two sets of terrace edges are visible: major step bunches spaced about 1.1 $\mu$m, and subterraces spaced about 200 nm. The major terraces are 0.8 nm thick (measured by atomic force microscopy), corresponding to 3 SiC bilayer, in agreement with previous studies [12]. Terrace edges of the step bunches in the clean surface appear smooth and the subterraces can be clearly resolved. Scanning electron micrographs of 1 ML graphene grown in UHV for different annealing times at $T_G = 1250$ C are shown in Figs. 1(b)-(e). With increased annealing time, the major terrace edges become visibly rougher, while
the subterraces are much less clearly resolved. The edge roughening becomes increasingly more evident for longer annealing times. To quantify this effect, the mean square roughness of the step bunches as a function of annealing time was measured. Several terrace edges of an individual sample were traced using plot digitizing software at a sampling rate of about 17 nm/step (inset in Fig. 2). The trace was then fit against a 9th order polynomial, which provides the baseline fit $y_0(t)$. The resulting baseline was then used to extract the average mean square (MS) deviation from the baseline $y_0(t)$. The average MS deviation was found to be proportional to the edge length $L$. Thus, for each terrace edge, the average MS deviation was normalized by $L$. Finally, the edge roughness $R_{\text{edge}}$ was defined as the difference in the normalized MS deviation of any graphitized terrace edge with that of the initial ungraphitized surface (so that $R_{\text{edge}}$ for the initial surface is zero). The evolution in $R_{\text{edge}}$ with annealing time is shown in Fig. 2.

A sharp increase in step edge roughness occurs during the first 8-10 minutes of annealing, when $R_{\text{edge}}$ rises to about 15 nm$^2$/µm. For longer annealing times the edge roughness increases more gradually to a maximum of about 20 nm$^2$/µm. In addition to edge roughening, the SiC subterraces become increasingly rougher and finally appear to aggregate into large patches (Fig. 1(d)-(f)). It has been shown recently that graphene layers are formed by decomposition of the $\sqrt{3}$ terraces [12]. This process develops until much of the higher SiC step edge is consumed to form a graphene layer on the lower terrace. It is very likely that the variation in the terrace edge morphology observed here is related to the local dissolution of the SiC steps and the formation of graphene layers. However, such variation at constant growth temperature, does not appear to alter the surface coverage considerably (±0.2 ML, based on AES).

With increased annealing times, a similar trend of edge roughness is observed in the evolution in the 2D Raman line (Fig. 2), which indicates an increase in the strain of the graphene epilayer measured at room temperature. Uniform compressive strain in epitaxial graphene originates in the large difference between the coefficients of linear thermal expansion of SiC and graphene [8], and in the fact that graphene expands upon cooling [15], while SiC contracts. The difference $\Delta\alpha(T)$ in the coefficients of thermal expansion is nearly constant between room temperature (RT) and the graphene synthesis temperature, $T_G \approx 1250^\circ$C. A higher compressive stress at room temperature results from a lower stress film at the temperature of growth ($T_G$), while a nearly stress free film at room temperature indicates that the film existed under high tensile stress at $T_G$. Within experimental accuracy,
the strain measured at room temperature might well vanish for very short annealing times. In contrast, for long annealing times, assuming that the graphene layer is in mechanical equilibrium with the substrate at the temperature of growth, a compressive strain in the room temperature film of 0.8% is calculated, which is in agreement with recent measurements [8, 9]. This analysis suggests that mechanical equilibrium with the 6-$\sqrt{3}$ SiC substrate at $T_G$ is indeed achieved for annealing times longer than 10 minutes, while for shorter annealing times ($\sim$5 minutes or less), graphene is under high tensile strain at $T_G$.

The strain relaxation at $T_G$, implied by the Raman data, provides a likely explanation for the changes in morphology observed by ECCI. Accordingly, for long enough annealing time, tensile strain developed at $T_G$ is relieved by the break up of the pinned graphene layer on the SiC subterraces into a patchy film, as observed. These changes in morphology must be accompanied by roughening of the step edges to which graphene films are pinned. Such increase in roughness does not induce a significant change in surface coverage ($\pm 0.2$ ML). For shorter annealing times, surface relaxation does not take place, leaving the SiC terraces morphologically unchanged.

In summary, the evolution in the surface morphology of epitaxial graphene films and of the underlying (0001) 6H-SiC substrate was studied by ECCI and explained in terms of the changes in structural strain during the synthesis of epitaxial graphene. It is found that long annealing times produce layers in equilibrium at growth temperature (and thus under highly compressive strain at room temperature); stress relief at the growth temperature is obtained through the development of large step roughness (as high as 20 nm$^2$/µm) and film discontinuity. Shorter annealing times produce highly tensile films at growth temperature, resulting in almost stress-free films at room temperature as well as minimal change in surface morphology. Thus the ability to control strain in epitaxial graphene, by tuning of the annealing times, is tied with the ability to control the film morphology.

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