Implementation of Digital Lock-in Amplifier

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Abstract. The recovery of signal under the presence of noise is utmost essential for proper communication. The signals corrupted due to noise can be recovered using various techniques. However the weak signals are more prone to noise and hence they can be easily degraded due to noise. In such cases, a digital lock-in amplifier becomes an essential device for recovery of such weak signals. Keeping the cost, speed and other considerations, we will present the implementation of digital lock-in amplifier and how it recovers the weak signal under extreme noisy conditions.

1. Introduction

Optimum signal recovery under noisy environments is a very significant problem that the modern day research focuses upon. Traditional amplifier designs do not provide satisfactory results in a highly degraded noise scenarios as they give very low signal power levels. The prime reason behind it is that traditional amplifier designs do not single out the specific frequency component of our interest. Such amplifiers lead to scenarios where the noise levels are in millivolt range whereas the signal levels are in microvolt range and thus leading to poor signal-to-noise ratio.

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In the field of communication the signals gets degraded when they are allowed passed through the channel. The signals which are weak may not reach the receiver as the noisy channel conditions degrade the original signal upto extreme case. So a digital LIA can be used for the recovery of the weak signals at the receiver. LIA is also used for the null detection in AC bridge measurement systems\textsuperscript{3,4}. The lock-in amplifier implemented in a microcontroller based DSP is inexpensive, portable and customizable\textsuperscript{5}.

The implementation of digital LIA is feasible only when the frequency of the reference signal is in the range of a few kilohertz. In that case the analog signal can be converted into digital signal by using ADC and DSPs. To covert an analog signal into digital signal the sampling frequency must be at least twice the frequency of the input signal\textsuperscript{3}. However if frequency of the reference signal is in megahertz range then applying ADC and DSP on such signal may not be feasible due to the technical
Lock-in amplifiers are used to detect and measure very small AC signals all the way down to nanovolt range. It works on phase-sensitive detection to single out the components of the signal at a specific reference frequency and phase rejecting all other noise frequencies. Based on this, digital phase locked (DPLL) form the basis for providing an accurate tuning to the desired frequency and phase. The performance of the lock-in amplifiers is subject to parameters such as locking accuracy, speed of locking, noise immunity, sampling frequency, integration time for hardware integration, cost etc. [9]. Similar works has been reported in [10].

The background of LIA is explained in the second section. The literature review of LIA is reported in the third section. The proposed model of digital LIA is discussed in the next section. The experimental details are explained in the subsequent section. The result and discussion is reported in the next section followed by a suitable conclusion, acknowledgement and references.

2. Lock-in Amplifier

A lock-in amplifier is a device which can extract a signal of interest at a specific frequency from an output signal which contains significant noise levels at other frequencies. The main objective of the lock-in amplifier is to increase the signal-to-noise ratio of the system by synchronizing the output signal to the input signal at a specific frequency and by filtering the other frequencies which contains the noise [11]. The essential components of LIA are shown in Figure 1.

![Figure 1: Block diagram of a typical lock-in amplifier](image)

The lock-in amplifier consists of an input amplifier to amplify the input signal and its output is fed to BPF and then the output of the BPF is multiplied with a reference signal and then passed through the LPF to remove the high frequency components present in the signal thereby only the DC components are present at the output of the LPF. This output signal is the desired signal of interest.

3. Literature Review

Digital lock-in amplifier is widely used in the field of science and engineering. It can be used for the measurement of impedance by taking the advantage of the reduced noise enabled by the single frequency measurement [11]. The measurement of impedance can be useful for applications like semiconductor gas sensing inorganic molecules [13]. It is also used for the reduction of noise in the analysis of optical samples like infrared spectroscopy [14]. A high frequency digital LIA which works on the principle of random sampling is reported in [6]. An LIA is typically used in AC measurement system for null detection in order to measure the imbalance signal [3]. A novel digital lock in detection technique for measuring the amplitude and phase of the multiple AM signals has been reported in [15]. This detection technique requires a reference signal that is modulated at the same frequencies as their signal of interest while ignoring other frequencies [15]. The recovery of a weak signal based on the concept of zero-crossing algorithm which is implemented using digital phase locked loop is reported in [16][17].
4. Proposed Model

The block diagram of the proposed model is shown in Figure 2.

From the block diagram show in Figure 2, we have taken two reference signals one of which has the same phase as that of the experimental signal and the other reference signal is the 90° phase shift with respect to the input signal. The experimental signal taken to be sinusoidal cosine waveform is multiplied with the reference signal having same phase to produce the X component or the inphase component and then passed through the LPF. The experimental signal is multiplied with the 90° phase shifted reference signal to produce the Y component i.e. the quadrature phase component and then passed through the LPF.

The principle of digital LIA is explained in equations (1), (2) and (3).

\[ V_{\text{in}} = V_{\text{signal}} \cos (\omega_{\text{ref}} t + \theta_{\text{signal}}) \]  

where, \( V_{\text{in}} \) is the experimental signal

\( \omega_{\text{ref}} \) is the radian frequency of the experimental signal,

\( \theta_{\text{signal}} \) is the phase of the experimental signal

We have taken two reference signals as described by equations (2) and (3).

\[ V_{\text{ref} \cos} = V_{\text{ref}} \cos (\omega_{\text{ref}} t + \theta_{\text{ref}}) \]  

\[ V_{\text{ref} \sin} = V_{\text{ref}} \sin (\omega_{\text{ref}} t + \theta_{\text{ref}}) \]  

Multiplying equation (1) and (2) we get \( V_{\text{out} \cos} \) as described by equation (4)

\[ V_{\text{out} \cos} = \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \cos (\theta_{\text{signal}} - \theta_{\text{ref}}) + \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \cos (2\omega_{\text{ref}} + \theta_{\text{signal}} + \theta_{\text{ref}}) \]  

Multiplying equation (1) and (3) we get the \( V_{\text{out} \sin} \) as described by equation (5)

\[ V_{\text{out} \sin} = \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \sin (\omega_{\text{ref}} t + \theta_{\text{signal}} + \theta_{\text{ref}}) - \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \sin (\theta_{\text{signal}} - \theta_{\text{ref}}) \]  

Equation (4) and equation (5) are passed through the low pass filter in order to eliminate the high frequency component and hence we obtain only the inphase and quadrature phase component as described by equation (6) and (7).

\[ X = \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \cos (\theta_{\text{signal}} - \theta_{\text{ref}}) \]  

\[ Y = \frac{1}{2} V_{\text{signal}} V_{\text{ref}} \sin (\theta_{\text{signal}} - \theta_{\text{ref}}) \]  

The final amplitude of the lock-in amplifier is given by equation (8)

\[ A = 2 \times \sqrt{X^2 + Y^2} \]
The phase of the lock-in amplifier is given by equation (9)

\[ \text{Phase} = \tan^{-1} \frac{V}{x} \]  

(9)

5. Experimental Details

A heterodyne lock-in detection technique can be performed where there is a need for \( f_m \) to be larger than the possible values for \( f \) [15]. An experimental signal and two reference signals are created that has a time period of 0.1 seconds at a constant frequency of 5 KHz. In order to simulate the increase or decrease in the ADC sample frequency the amount of values per cycle for each signal matrix were increased or decreased which can be done while maintaining the correct frequency and same time period. The sampling frequency is set to be 70 KHz. A high sampling frequency is used so that the immunity of noise can be improved and the average error square can be reduced. The experimental signal is chosen to be a sinusoidal cosine waveform with a phase delay of \( \frac{\pi}{30} \) radian and amplitude of 30 mV. The first reference signal is a sinusoidal cosine waveform with a zero phase shift. The second reference signal is sinusoidal signal waveform. The amplitude of the two reference signals are 1V each. The experimental signal is multiplied element by element with the cosine reference signal and also with the sinusoidal reference signal. The output of the two multiplied signal requires filtering which can performed by using LPF. The LPF is designed by taking the mean of the two multiplied matrices thereby producing a single DC value for each of \( X \) and \( Y \) channel outputs. The \( X \) and \( Y \) channel outputs are then used to find the amplitude of the signal and the phase difference between the signal and the reference signal. After that the noise is added to the signal to test the lock-in amplifier noise rejection performance. The noise is added using `randn` function in MATLAB which produces a random number with a uniform Gaussian distribution. The length of the noise matrix should be same as that of the experimental signal matrix so that they can be added to the experimental signal. This random noise matrix is multiplied with a noise level multiplication factor which is in a range of increasing incremental values to simulate the level of noise increasing in the experiment. The range of the noise multiplication factor is in the range from 0.1 to 1000 with a step size of 100 linearly spaced over the range. This range is chosen because the performance of the lock-in amplifier is not known. The SNR of the signal is used for the determination of the level of immunity of noise at which the lock-in amplifier still produces an acceptable output. The SNR of the signal is calculated as the ration of signal power to the noise power. The amplitude of the lock-in amplifier is measured for the calculated SNR for the range of noise multiplication factors. As the amplitude of the signal would increase with increase in noise and so such output is not acceptable. So an acceptable threshold must be set so that the output must not be far above the input amplitude. A value of 2 percent above the input amplitude is considered as an acceptable output. If the output amplitude is below an SNR of -40 dB then it is discarded in this case. So the range of the noise multiplicative factor is then reduced from 0.1 to 100 in order to reduce the computational time. The error between the input and output is calculated by taking the difference between each element of input and output. This is done to monitor the output error as the noise is continuously increasing. This produces only one number for each level noise in the range. This value would change each time the program will run due to the different random noise. So a set of 1000 random noise is used. The sets of 1000 random noise samples are then averaged so that a more appropriate Gaussian distribution is achieved. These average random samples are then squared to obtain an average error square for each noise level. This average error square is the square of the average error between the input amplitude and output amplitude for the set of random variables. The multiplicative noise factor is then changed to a logarithmic scale as the average error square has been plotted in the logarithmic Y axis. In order to simulate the lock-in amplifier in microprocessor signal quantization is used to simulate a range of ADC bit resolutions. A range of 2 to 16 bit resolution is used. The quantization is performed on the experimental signal after the noise is added to it. The signal matrix is converted to a sixteen bit integer and then quantized to the required bit resolution. The signal is then converted back to double precision format. A plot of specific SNR values and their corresponding average error square value from the straight line approximation matrix is carried out in order to compare the different ADC resolutions.
6. Results and Discussion

In this section the results of the digital LIA are discussed.

An experimental cosine waveform is created having frequency of 5 KHz with a phase delay of $\frac{\pi}{10}$ radians. The amplitude of the experimental signal is 30 mV. The sampling frequency is 70 KHz. It is multiplied with a cosine reference signal without phase delay and has amplitude of 1V to produce a multiplicative output signal as shown in Figure 3.

![Figure 3: Experimental Cosine signal and Reference Cosine Signal and their multiplication.](image)

The experimental cosine waveform is multiplied with a sinusoidal reference signal and their plot is shown in Figure 4.

![Figure 4: Experimental Cosine Waveform and Sinusoidal reference signal and their multiplication.](image)
The output of the two multiplicative signals is then passed through the LPF. The LPF is designed as an averaging filter. The mean of the output of the first multiplicative signal is calculated to obtain a single DC value which is the inphase component and the mean of the second multiplicative signal is calculated to obtain a single DC value which is the quadrature phase component. The output amplitude of the signal and the phase is calculated using equation (8) and (9) respectively.

The error which occurred is then averaged and then squared to obtain the average error. The average error\(^2\) at calculated SNR at sampling frequency 70 KHz for 1000 sets of random samples with increase in bit resolution is given in Table 1.

| SNR     | Bit Resolution | Average Error |
|---------|----------------|---------------|
| -19.2474 | 2 bit          | 0.60777       |
| -23.4898 | 3 bit          | 0.48485       |
| -23.4898 | 4 bit          | 0.45437       |
| -23.4898 | 5 bit          | 0.44581       |
| -23.4898 | 6 bit          | 0.44493       |
| -24.0959 | 7 bit          | 0.44392       |
| -23.4898 | 8 bit          | 0.44283       |
| -24.0959 | 9 bit          | 0.44281       |
| -24.0959 | 10 bit         | 0.44280       |
| -24.0959 | 11 bit         | 0.44281       |
| -24.0959 | 12 bit         | 0.44280       |
| -24.0959 | 13 bit         | 0.44280       |
| -24.0959 | 14 bit         | 0.44279       |
| -24.0959 | 15 bit         | 0.44278       |
| -24.0959 | 16 bit         | 0.44276       |

From Table 1 we can conclude that the average error decreases with increase in bit resolution and then become constant at calculated SNR and at sampling frequency 70 KHz.

The results of the average error square in both logarithmic Y axis and linearly spaced scale, the quantization of the experimental signal and the output amplitude for 8 bit is shown in Figure 5.

From Figure 5, it can be seen that the average error square decreases with respect to increase in SNR in dB and finally becomes constant with further increase in SNR in dB. The average amplitude is valid at 2% error i.e. the output amplitude below SNR of -40 dB are discarded and only above SNR of above -40 dB is considered.

7. Conclusion
The digital LIA can be used for the recovery of extremely weak signal embedded in the background noise. The weak experimental signal is sampled at sampling frequency more than the Nyquists frequency and quantized. The experimental signal is converted into digital signal and an ADC bit resolution of 2 to 16 is considered. A sampling frequency of 70 KHz is considered. The average error square is calculated at calculated SNR and is seen that the average error square decreases with increase in ADC bit resolution from 2-8 bits and after that it becomes constant. Based on this 8 bit resolution can be used for the implementation of digital LIA. The output amplitude is plotted against SNR and an error of 2 percent above the input amplitude is considered as valid output.
Figure 5: Result of average error$^2$ for 8-bit resolution and the output amplitude at sampling frequency 70 KHz against SNR in dB.

8. Future Work

Hardware FPGA implementation of digital lock-in amplifier would be chosen as a basis for future work. Further the immunity of noise can be improved by about 3 dB and the average error square can be reduced by half by increasing the sampling frequency [15]. Also by increasing the integration time the noise immunity can be improve by about 10 dB [15].

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