Abstract—We present a design-technology tradeoff analysis in implementing machine-learning inference on the processing cores of a Non-Volatile Memory (NVM)-based many-core neuromorphic hardware. Through detailed circuit-level simulations for scaled process technology nodes, we show the negative impact of design scaling on read endurance of NVMs, which directly impacts their inference lifetime. At a finer granularity, the inference lifetime of a core depends on 1) the resistance state of synaptic weights programmed on the core (design) and 2) the voltage variation inside the core that is introduced by the parasitic components on current paths (technology). We show that such design and technology characteristics can be incorporated in a design flow to significantly improve the inference lifetime.

I. INTRODUCTION

Neuromorphic systems are integrated circuits designed to mimic the computations in a mammalian brain \cite{2}. They enable energy-efficient execution of Spiking Neural Networks (SNN) \cite{2} and therefore, these systems are suitable for implementing machine learning inference tasks for embedded Systems and Edge devices in Internet-of-Things (IoT). A neuromorphic system consists of processing cores that implement neurons and synapses. Multiple such cores are interconnected together using Segmented Bus \cite{3} or Network-on-Chip (NoC) \cite{4} to design a many-core neuromorphic hardware \cite{5}. Table I illustrates the neuron and synapse capacity of recent neuromorphic hardware cores.

| System          | # Neurons/core | # Synapses/core | # Cores/chip | # Chips/board |
|-----------------|----------------|-----------------|--------------|---------------|
| ODIN            | 256            | 64K             | 1            | 1             |
| µBrainDYNAPs    | 336            | 38K             | 1            | 4             |
| BrainScaleS     | 256            | 16K             | 1            | 352           |
| SpinNaker       | 512            | 128K            | 1            | 10            |
| Neurogrid       | 30K            | 2.8M            | 1            | 11            |
| Lilli           | 65K            | 8M              | 1            | 12            |
| TrueNorth       | 130K           | 130M            | 1            | 12            |
| # Neurons       | 256            | 65K             | 1            | 10            |
| # Synapses      | 336            | 1K              | 1            | 352           |
|                | 256            | 16K             | 1            | 10            |
|                | 512            | 128K            | 1            | 352           |
|                | 30K            | 2.8M            | 1            | 10            |
|                | 65K            | 8M              | 1            | 10            |
|                | 130K           | 130M            | 1            | 10            |
|                | 256            | 65K             | 1            | 10            |
|                | 336            | 1K              | 1            | 352           |

A neuromorphic core can be implemented using an analog crossbar where bitlines and wordlines are organized in a grid with memory cells connected at their crosspoints to store the synaptic weights \cite{14}–\cite{17}. Neuron circuits are implemented along bitlines and wordlines (see Figure 2). Recently, Non-Volatile Memory (NVM) technologies such as phase-change memory (PCM) and oxide-based resistive switching random access memory (OxRRAM) are used to implement the memory cells in a neuromorphic core due to their low power consumption, CMOS-compatible scaling, and multilevel analog operations \cite{18}. In an NVM-based neuromorphic inference hardware, the resistance state corresponding to the synaptic weights of an SNN are programmed on the NVM cells.

Unfortunately, NVMs suffer from reliability issues such as circuit aging, limited endurance, and read disturbance \cite{26}–\cite{29}. Many of these issues have been addressed recently in the context of neuromorphic computing \cite{30}–\cite{37}. In this work, we focus on the read disturbance issues of OxRRAM technology, where an OxRRAM cell’s resistance state may change after performing a certain number of read operations \cite{38}–\cite{40}. Therefore, when an OxRRAM-based neuromorphic hardware is used to implement an inference task, the trained synaptic weights programmed on the hardware may change after performing a few inference operations. To ensure expected results from an inference task, the trained weights need to be reprogrammed on to the hardware periodically. Reprogramming of synaptic weights to a neuromorphic hardware involves offlining the hardware and transferring the weights from the host to the hardware via a bandwidth-limited interconnect. This can significantly increase the overhead, and lower the availability and reliability of neuromorphic computing.

In this work, we present a design-technology tradeoff analysis in implementing machine-learning inference on many-core neuromorphic hardware. Through circuit-level simulations we show the negative impact of design scaling on read endurance of NVMs, which directly impacts their inference lifetime. We show that the inference lifetime of a crossbar depends on 1) the resistance state of synaptic weights programmed on the NVMs and 2) the voltage variation inside the crossbar that is introduced by the parasitic components on current paths. Such design and technology characteristics can be incorporated in a design flow to significantly improve the inference lifetime.

1NVMs are also used in classical von Neumann computing to mitigate the performance and energy bottleneck of DRAM \cite{19}–\cite{25}.
We briefly introduce Spiking Neural Network (SNN) and their implementation in hardware.

Spiking Neural Networks (SNNs) are the third generation of neural networks designed using spiking neurons and bio-inspired learning algorithms [2]. In an SNN, spikes injected from pre-synaptic neurons raise the membrane voltage of a post-synaptic neuron (middle sub-figure of Figure 1). When the membrane voltage crosses a threshold (\(V_{th}\)), the post-synaptic neuron emits spikes that propagate to other neurons (right sub-figure of Figure 1). SNNs implement some variants of Integrate and Fire (I&F) neurons with a spike duration ranging from 1 \(\mu s\) to several ms [41]–[43] (left sub-figure of Figure 1).

SNNs can implement many machine learning approaches [44]–[51]. In a supervised machine learning, an SNN is pre-trained with representative data. Machine-learning inference refers to feeding live data points to this trained SNN to generate the corresponding output. The quality of machine learning inference can be expressed in terms of accuracy [45], Mean Square Error (MSE) [44], Peak Signal-to-Noise Ratio (PSNR) [52], and Structural Similarity Index Measure (SSIM) [53]. For SNNs, these quality metrics are defined in terms of the inter-spike interval (ISI) [54]–[57].

\[
I S I = \frac{\sum_{i=2}^{K} (t_i - t_{i-1})}{(K - 1)}.
\]

A neuromorphic hardware platform is implemented as a tiled architecture, where tiles are interconnected via a time-multiplexed shared interconnect. Each tile consists of a neuromorphic processing core, which can implement neurons and synapses of a machine learning model. A common design practice is to use an analog crossbar to implement a core.

In a crossbar, pre-synaptic neuron circuits are placed on horizontal wires called wordlines, while post-synaptic neuron circuits are placed on vertical wires called bitlines. Memory cells are placed at the crosspoint of each wordline and bitline, and they implement the synaptic weights of an SNN. The left subfigure of Figure 2 illustrates an \(N \times N\) crossbar. The right subfigure illustrates the parasitic RC components on the current path from a pre-synaptic neuron to a post-synaptic neuron accessing the memory cell \((i, j)\) located at the crosspoint of \(i^{th}\) wordline and \(j^{th}\) bitline.

Overall, a neuromorphic hardware enables distributed and pipelined processing of SNN operations. Additionally, each crossbar in the hardware can implement a maximum of \(N\) pre-synaptic neurons per post-synaptic neuron. Therefore, system-softwarer frameworks such as NEUTRAMS [58], NeuroExplorer [59], Corelet [60], PACMAN [61], and LAVA [62] consist of 1) a compiler, which partitions an SNN model into clusters such that the neurons and synapses of each cluster can be mapped to a crossbar of the hardware, and 2) a run-time manager, which maps the clusters of an SNN to the cores of a many-core hardware. To this end, several mapping strategies have been proposed, including optimizing for energy [63]–[66], throughput [67]–[70], resource utilization [59], [58], [62], [71], [72], circuit aging [30]–[34], inference lifetime [39], and write endurance [35]–[37]. These mapping techniques all use some variant of the SNN-partitioning approach proposed in SpiNeMap [65].

Recently, dataflow models have been used to analyze performance of SNNs implemented on neuromorphic hardware, especially using Synchronous Dataflow Graphs (SDFGs) [73]. There are two strategies proposed in literature – the SDF-SNN [67] and its extended versions [68], [79], [80], which uses dataflow graphs to model an SNN, performing partitioning and mapping explorations with neurons and synapses directly, and the DFSynthesizer [69] and its extended version [71], which uses dataflow graphs to only model the clustered SNN, allowing mapping and scheduling of the clusters (a collection of neurons and synapses) to the PEs of a neuromorphic hardware.

Emerging non-volatile memory (NVM) technologies such as phase-change memory (PCM), oxide-based memory (OxRAM), spin-based magnetic memory (STT-MRAM), and Flash have recently been used for synaptic storage in crossbars. NVMs are non-volatile, have high CMOS compatibility, and can achieve high integration density. Each NVM device can implement both a single-bit and multi-bit synapse. Because of these properties, an NVM-based neuromorphic hardware typically consumes energy that is magnitudes lower than using SRAMs [81]–[83]. However, NVMs also introduce reliability issues [78]. Table II summarizes them for different NVMs.

We discuss one specific issue – limited read endurance for OxRAM-based neuromorphic hardware.
synaptic cells of a crossbar due to its demonstrated potential for low-power multi-level operation and high integration density [18]. An OxRRAM cell is composed of an insulating film sandwiched between conducting electrodes forming a metal-insulator-metal (MIM) structure (see Figure 3). Recently, filament-based metal-oxide OxRRAM implemented with transition-metal-oxides such as HfO$_2$, ZrO$_2$, and TiO$_2$ has received considerable attention due to their low-power and CMOS-compatible scaling.

Synaptic weights are represented as conductance of the insulating layer within each OxRRAM cell. To program an OxRRAM cell, elevated voltages are applied at the top and bottom electrodes, which re-arranges the atomic structure of the insulating layer. Figure 3 shows the High-Resistance State (HRS) and the Low-Resistance State (LRS) of an OxRRAM cell. An OxRRAM cell can also be programmed into intermediate low-resistance states, allowing its multilevel operations.

In OxRRAM technology, the transition from HRS state is governed by a sudden decrease of the conductive filament gap on application of a stress voltage during spike propagation [18]. This is illustrated in the left subfigure of Figure 4 where the vertical filament gap is shown to reduce by an amount $dg_{i,j}$ on application of stress voltage during spike propagation [38]. This causes the resistive state to change from HRS to LRS. The time for state transition in the $(i,j)^{th}$ OxRRAM cell is given by

$$t_{i,j}(LRS) = 10^{-14.7} V_{i,j} + 6.7 \text{sec}$$ (3)

and is related to the gap $g_{i,j}$, $a_0$ is the atomic hoping distance, and $\gamma_0$ is a fitting constant.

The transition from one of the LRS states is governed by the lateral filament growth [38]. This is illustrated in the right subfigure of Figure 4. The time for state transition in the $(i,j)^{th}$ RRAM cell is given by

$$t_{i,j}(HRS) = 10^{7.7} V_{i,j} + 6.7 \text{sec}$$ (4)

The computer memory industry has thus far been primarily driven by the cost-per-bit metric, which provides the maximum capacity for a given manufacturing cost. As shown in recent works [19–24], [84], manufacturing cost can be estimated from the area overhead. To estimate the cost-per-bit of a neuromorphic core, we investigate the internal architecture of a crossbar and find that a neuron circuit can be designed using 20 transistors and a capacitor [85], while an NVM cell is a 1T-1R arrangement with a transistor used as an access device for the cell. Within an $N \times N$ crossbar, there are $N$ pre-synaptic neurons, $N$ post-synaptic neurons, and $N^2$ synaptic cells. The total area of all the neurons and synapses of a crossbar is

$$\text{neuron area} = 2N(20T + 1C)$$ (5)

$$\text{synapse area} = N^2(1T + 1R)$$

where $T$ stands for transistor, $C$ for capacitor, and $R$ for NVM cell. The total synaptic cell capacity is $N^2$, with each NVM cell implementing 2-bit per synapse. The total number of bits (i.e., synaptic capacity) in the crossbar is

$$\text{total bits} = 2N^2$$ (6)
Therefore, the cost-per-bit of an \( N \times N \) crossbar is
\[
\text{cost-per-bit} = \frac{2N(20T + 1C) + N^2(1T + 1R)}{2N^2} \approx \frac{F^2(27 + 2N)}{N},
\] (7)
where the cost-per-bit is represented in terms of the crossbar dimension \( N \) and the feature size \( F \). Equation (7) provides a back-of-the-envelope calculation of cost-per-bit. Figure 5 plots the normalized cost-per-bit for four different process technology nodes, with the crossbar dimension ranging from 16 to 256. We observe that the cost-per-bit reduces with increase in the dimension of a crossbar, i.e., larger-sized crossbars can accommodate more bits for a given cost.

We now analyze the internal architecture of a crossbar. Figure 6a shows the current through the memory cells in a 128x128 crossbar. This current variation is due to the difference in the length of current paths from pre to post-synaptic neurons in the crossbar, where the length of a current path is measured in terms of the number of parasitic components on the path. These current values are obtained for a 65nm technology node and at 300K temperature corner. As can be clearly seen from the figure, current through memory cells on the top-right corner of the crossbar is lower than those at the bottom-left corner.

Figure 6b shows the endurance variation of a 128x128 crossbar at 45 nm node and at 30°C with each RRAM cell programmed to HRS state. The endurance variation is a direct result of the current variation in the crossbar.

Figure 7 shows the difference between currents on the shortest and the longest path for different crossbar sizes. The current difference increases with crossbar size because of the increase in the number of parasitic resistances on the longest current path, which results in larger voltage drops, lowering the current injected into its post-synaptic neuron. However, larger current variation causes larger endurance variation as illustrated in Figure 6b. Therefore, larger crossbar sizes lead to larger endurance variation.

System designers often make a tradeoff between cost-per-bit and endurance variation. Typically, crossbar sizes of \( 128 \times 128 \) and \( 256 \times 256 \) gives the best tradeoff.

V. DESIGN FLOW INCORPORATING DESIGN-TECHNOLOGY TRADEOFF

An optimized design flow is one, which takes into account the design and technology characteristics to place neurons and synapses to a crossbar such that those synapses that propagate more spikes are mapped to NVMs with higher read endurance. This is to increase the inference lifetime.

In our prior work [39], we show that such a design flow can significantly improve the inference lifetime. Figure 8 reports the inference lifetime for 10 applications for the proposed design flow normalized to SpiNeMap. We observe that through intelligent synapse mapping, the inference lifetime obtained using the proposed approach is on average 3.4x higher.

VI. CONCLUSION

A design-technology tradeoff analysis is performed to investigate inference lifetime of neuromorphic hardware that adopts NVM as synaptic storage. An essential observation of the analysis is that the read endurance of an NVM cell depends on its programmed synaptic weight (design) and the voltage exposed to the cell (technology). Our analysis also reveals that voltages exposed to NVM cells inside a crossbar vary due to the parasitic components on current paths, which leads to asymmetric read endurance across NVM cells in a crossbar.
From detailed circuit-level simulations, we show design scaling on read endurance of NVMs negatively impacts the inference lifetime of neuromorphic hardware. In addition, the design flow that considers asymmetry in read endurance can significantly improve the inference lifetime of neuromorphic hardware.

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