Design of Wideband Signal Decimation Based on Polyphase Filtering

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Abstract: In the wideband receiving system of radar, it is often necessary to process signals with high sampling rate and wide bandwidth. The sampling rate that the system can process is limited by the design structure of the whole system. Usually, the signal is processed by a polyphase filter bank composed of several low-order filters. The interpolation and decimation of signals are realized at the same time, which further reduces the sampling rate. However, the baseband signal data rate required by the signal processing system may not be obtained by integer decimation of the sampled signal. Therefore, a structure combining parallel polyphase interpolation filtering and parallel polyphase decimation filtering is designed to realize the decimation of \( L/M \) multiple of large bandwidth signals without improving the processing clock of the FPGA.

1. Introduction

With the continuous updating of radar, communication and electronic countermeasures technology, the bandwidth of digital waveform generation system is required to increase continuously. This has created a great challenge for ADC, DAC and DSP devices. The theory of polyphase filtering can effectively alleviate the restriction of digital signal processor on the wideband digital waveform. Its essence is to interpolate or decimate while the digital filtering is implemented [1–2]. In practical application, the sampling rate and carrier frequency of IF signal are not chosen at will by the digital IF receiver system, but the design of radio frequency (RF) transmitter and analogy receiver system should be considered comprehensively. The sampling rate is usually required to be converted to an \( L/M \) multiple of any rational number. The system consists of interpolation system of \( L \) multiple and decimation system of \( M \) multiple (where \( L \) and \( M \) is a prime integer). In this paper, an efficient algorithm structure based on polyphase filtering is applied to process the multichannel low-speed data stream which is after series-to-parallel conversion in order to complete the decimation of \( L/M \) multiple design of ultra-wideband signals.

2. Ultra-wideband digital reception

The decimation of \( L/M \) multiple is actually the resampling process of the baseband signal after the digital down conversion. The implementation of the algorithm must be based on the output data architecture of the ADC sampling chip and the implementation of the digital down conversion algorithm. Before discussing the decimation of \( L/M \) multiple, it is necessary to understand the processing of UWB digital IF receiver and digital down conversion [3], which is the basis of the decimation of \( L/M \) multiple algorithm in the engineering implementation of UWB digital IF receiver and digital down conversion. Unlike the receiving systems of low-speed narrow-band, even interpolating and decimating directly from single-channel will not exceed the clock processing power of FPGA. The data rate of parallel
branches of the UWB receiving and processing system is still high. The single-channel interpolating operation may cause the clock rate of FPGA to be too high, so the project cannot be realized. When the sampling rate is in the range of 1GHz to 3GHz, most ADC chips with low voltage differential signalling (LVDS) interface in the IF receiving system of UWB digital use two or four channels to output parallel digital signals, which reduces the data rate of each channel and can complete the subsequent digital down conversion algorithm.

2.1 Digital down conversion
The main function of digital down conversion is to lower the digital IF signal to the base band, and to provide the signal which is suitable for the subsequent digital signal processing. The basic model is shown in figure 1. Digital down conversion can be divided into the part of mixing and the part of decimation filtering [4].

![Figure 1. Basic model of digital down conversion](image)

Let the A/D sampling signal as follow:

\[ x(n) = A \cos(2\pi f_0 n / f_s + \phi) \]  

(1)

Where \( A \) is the amplitude of the signal; \( f_0 \) is the central frequency of the signal; \( n \) is the sampling serial number of the signal; \( f_s \) is the sampling frequency of the A/D conversion; \( \phi \) is the initial term of the signal.

The NCO generates two orthogonal local oscillators signals:

\[ I(n) = \cos(2\pi f_{LO} n / f_s) \]
\[ Q(n) = \sin(2\pi f_{LO} n / f_s) \]  

(2)

Where \( f_{LO} \) is the local frequency of NCO.

Then we get the in-phase component and the quadrature component of the mixing signal.

\[ y_i(n) = A\cos[2\pi(f_0 - f_{LO}) n / f_s + \phi] + \cos[2\pi(f_0 + f_{LO}) n / f_s + \phi] / 2 \]
\[ y_q(n) = A\{-\sin[2\pi(f_0 - f_{LO}) n / f_s + \phi] + \sin[2\pi(f_0 + f_{LO}) n / f_s + \phi] \} / 2 \]  

(3)

It can be seen from the formula (3) that the mixing signal includes not only the expected baseband signal, but also the high-frequency component. The baseband signal can be obtained by low-pass filtering after mixing the signals. In addition, in order to reduce the digital signal data rate and processing, the signal needs decimation processing. The function of the decimation filtering is to reduce the data flow rate of the signal, to reduce the computation and to filter out the high-frequency components of the signal.

2.2 Digital down conversion of parallel polyphase
For the digital IF receiving system with sampling rate above GHz, the parallel data bus architecture of ADC chip and the implementation of data deceleration pretreatment, the IF signal is usually converting to four or eight parallel low-speed signals. Digital mixing, digital low-pass filtering and decimation are also realized based on these parallel data. In a high-speed signal sampling system, to reduce the pressure
of digital mixing, the signal carrier frequency and sampling rate can usually be set to the relationship of \( f_c = (2n+1) f_s / 4(n=0, 1, 2, \cdots) \). This will make the digital local oscillator only has the values of 0 and ±1. In the process of digital mixing, only simple addition and subtraction operations are needed, and double decimation of parallel signals can be realized. Of course, limited to the overall design planning of radar system, even if the relationship between carrier frequency and sampling rate cannot be guaranteed, the mixing and decimation of the first stage can still be simplified by the way of secondary frequency conversion.

Let the system functions of the system to be:

\[
H(z) = \sum_{n=-\infty}^{\infty} h(n)z^{-n}
\]  

(4)

Because of \( n = rM + k(k=0, 1, \cdots, M-1) \), the system function \( H(z) \) is defined by the formula (4) as follow:

\[
H(z) = \sum_{k=0}^{M-1} \sum_{r=-\infty}^{\infty} h(rM + k)z^{-(rM+k)}
\]

\[
= \sum_{k=0}^{M-1} z^{-k} \sum_{r=-\infty}^{\infty} h(rM + k)z^{-rM}
\]  

(5)

The \( k \)-multiple component of \( H(z) \) is defined:

\[
E_k(z) = \sum_{r=-\infty}^{\infty} h(rM + k)z^{-r}(k=0, 1, \cdots, M-1)
\]  

(6)

Then the \( H(z) \) of formula (5) can be expressed as:

\[
H(z) = \sum_{k=0}^{M-1} z^{-k} E_k(z^{M})
\]  

(7)

We called formula (7) is the type I polyphase decomposition expression of \( H(z) \). If we make \( R_k(z) = E_{M-k+1}(z)(k=0, 1, \cdots, M-1) \), we get another expression of polyphase decomposition:

\[
H(z) = \sum_{k=0}^{M-1} z^{-(M-k)} R_k(z^{M})
\]  

(8)

We called formula (8) is the type II polyphase decomposition expression of \( H(z) \).

After digital down conversion through parallel polyphase filtering, the IF signal after N-channel deceleration is converted into N/2-channel baseband I/Q signal, and the data rate of each branch signal is \( f_s / N \).

3. Wideband decimation of L/M multiple

3.1 Conversion of L/M multiple of sampling rate

Based on the processing of UWB digital IF receiving system: high-speed ADC chip output in the form of multi-channel parallel data bus. High-speed digital IF signal pre-processing makes parallel data double, then digital mixing and double decimation. And finally, parallel polyphase filtering digital down conversion algorithm architecture makes the baseband signal of large bandwidth digital down conversion usually \( 2^k \)-path parallel branches. This baseband signal of \( 2^k \)-path parallel branches are the digital basis for wideband decimation of L/M multiple. In other words, UWB decimation of L/M multiple is not a simple interpolation or decimation of single-channel baseband signal, but a polyphase interpolation and polyphase decimation algorithm for baseband signal of multi-channel parallel.
Changing the sampling rate of sequence $x(n)$ to L/M multiple can be achieved by cascaded interpolation system of L multiple and decimation system of M multiple, as shown in Figure 2. It should be noted that interpolating (frequency compression) followed by decimating (frequency extension) is the best way to retain the spectrum components of the sequence. Because the mirror filter $h_m(l)$ and anti-aliasing filter $h_d(l)$ are directly cascaded. They work on the same sampling frequency of $Lf_s$. So they can be combined into an equivalent filter $h_l(l)$. The equivalent block diagram of the system converted by the sampling rate of rational L/M multiple is as shown in Figure 3. The temporal relationship between the output sequence $y(m)$ and the input sequence $x(n)$ is:

$$y(m) = w(Mm) = \sum_{r=-\infty}^{\infty} h(Mm - rL)$$  \hspace{1cm} (9)

![Figure 2. Schematic diagram for the sampling rate of rational L/M multiple conversion system](image)

When $h(n)$ is the unit pulse response of a FIR filter with length n, it can be implemented by using the structure of the algorithm shown in figure 4, where the FIR filter is a direct algorithm [5].

![Figure 3. Equivalent principle block diagram for the sampling rate of rational L/M multiple conversion system](image)

![Figure 4. Structure of direct FIR filter for the sampling rate of rational L/M multiple conversion system](image)

The direct-type FIR filter shown in figure 4 is clear in concept and simple in structure. However, all multiplication and addition operations of the filter are carried out at the highest sampling rate of the system. Because L-1 zeros sequences are inserted between adjacent sequences of the input sequence $x(n)$ during the zero-value interpolation. If the value of L is large, the signal values which enter the FIR filter is mostly zero. So, the result of multiplication is mostly zero, which means most multiplication is invalid. Moreover, the final decimation process makes only one out of every M output values of the FIR...
filter be decimated. The other M-1 filter output values are not useful, so the algorithm is inefficient in structure.

3.2 Polyphase decimation filtering
FIR filter algorithm structure of the decimation system of integer M multiple can be implemented by using the filter banks which composed of M short polyphase filters. As shown in figure 5, the FIR sub filter composed of the k -multiple component \( E_k(z) \) requires the multiplication of \( N_k \) times and the addition of \( N_k - 1 \) times. If the sample interval of \( x(n) \) is taken as units time, the multiplication number of the polyphase filter algorithm structure in M unit of time (to obtain a sequence value of output) are

\[
\sum_{k=0}^{M-1} N_k = N, \quad \text{and the total number of additions is } \sum_{k=0}^{M-1} (N_k - 1) + (M - 1) = N - 1.
\]

![Figure 5](image-url) Polyphase filter algorithm structure for the decimation system of integer M multiple

3.3 Polyphase interpolation filtering
If the interpolation filtering of integer L multiple is represented by \( \Pi \)-type polynomial decomposition, the polyphase filter structure of interpolation system is as shown in figure 6. In this structure, the operating frequency of \( R_k(z) \) is the same as the sampling frequency of the input sequence, so each multiplier has a unit time to complete the operation. The number of multiplications required by the system is

\[
\sum_{k=0}^{L-1} N_k = N, \quad \text{and the number of additions required is } \sum_{k=0}^{L-1} (N_k - 1) + (L - 1) = N - 1.
\]

![Figure 6](image-url) Polyphase filter algorithm structure for the interpolation system of integer L multiple
3.4 Algorithmic architecture

Efficient algorithm structure of polyphase filtering in the sampling rate of integer L/M multiple conversion system is based on the design by polyphase filtering of interpolation system and polyphase filtering of decimation system algorithm structure. The design idea is to make FIR filter operate at the lowest rate. For this, when $L > M$, $\frac{L}{M} f_s > f_s$, the direct FIR filter algorithm structure in figure 4 together with the previous interpolator $\uparrow L$ can be replaced by the polyphase filter algorithm structure for interpolation system of integer $L$ multiple in figure 6, and when $L < M$, $\frac{L}{M} f_s < f_s$, the direct FIR filter algorithm structure in figure 4 together with the back decimator $\downarrow M$ can be replaced by the polyphase filter algorithm structure for the decimation system of integer $M$ multiple in figure 5.

4. Simulation verification

In this paper, the simulation parameters are set as follows: the signal form is linear frequency modulation signal; the center frequency of the signal is 800MHz and the sampling frequency is 2400MHz; the signal bandwidth is 200 MHz; signal time width is 20 $\mu$s; the number of signal paths after serial-to-parallel conversion is four. The baseband data rate obtained by UWB digital receiving and processing after double decimation is 1200MHz, and the data rate output by the signal processing system is 800MHz. Therefore, it is necessary to carry out the decimation of L/M multiple operation when the interpolation multiple is two and the decimation multiple is three. Based on the output format of UWB digital down conversion parallel polyphase filtering, after the decimation of L/M multiple, the original baseband signal of 4-channel *300MHz is converted to baseband signal of 4-channel *200MHz.

Figure 7 is the time domain waveform and spectrum of the A/D sampled signal. After double decimation, the signal is output as baseband signal of 4-channel*300MHz. That is, the data rate of the single I or Q signal is 300MHz. Figure 8 is the time domain waveform and spectrum after parallel polyphase interpolation filtering. The original baseband signal is converted into parallel interpolation signal of (4*2)-channel*300 MHz by the parallel polyphase interpolation filtering of two multiple, and the processing clock of the FPGA is not changed. Figure 9 is the time domain waveform and spectrum after the decimation filtering of L/M multiple. Each interpolating branch is decimated by three multiple, and the parallel decimation signals of 8-channel *100 MHz are obtained, and finally the baseband signal of 4-channel *200 MHz by the decimation of L/M multiple is obtained.

From the simulation results, it can be seen that using the sampling rate conversion system of integer L/M multiple can complete the digital down conversion and deceleration processing of the sampled signal.
Figure 9. Time domain waveform and spectrum after the decimation filtering of L/M multiple.

Figure 10. Result after adding noise.

When the original signal is added with white Gaussian noise of 50dB, we can observe the time domain waveform and spectrum decimated after interpolating as shown in figure 10, and the effect still meets the requirement. That is to say, even if noise exists and after the processing of the decimation system of L/M multiple which combined with polyphase interpolation filtering and polyphase decimation filtering, the processing effect of the signal is not deteriorated. So, this method can be widely used in large bandwidth signal processing system.

5. Conclusion
Due to the limitation of high-speed ADC sampling and wideband digital down conversion algorithm architecture, the parallel polyphase interpolation filtering and parallel polyphase decimation filtering can reduce the number of multiplication and addition operations and improve the speed of signal processing. It realizes L/M multiple decimation of large bandwidth signal in wideband digital IF receiving system without raising hardware clock.

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