An Algorithm-Hardware Co-design Framework to Overcome Imperfections of Mixed-signal DNN Accelerators

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ABSTRACT
In recent years, processing in memory (PIM) based mixed-signal designs have been proposed as energy- and area-efficient solutions with ultra high throughput to accelerate DNN computations. However, PIM designs are sensitive to imperfections such as noise, weight and conductance variations that substantially degrade the PIM accuracy. To address this issue, we propose a novel algorithm-hardware co-design framework hereafter referred to as HybridAC that simultaneously avoids accuracy degradation due to imperfections, improves area utilization, and reduces data movement and energy dissipation. We derive a data movement-aware weight selection method that does not require retraining to preserve its original performance. It computes a fraction of the results with a small number of variation-sensitive weights using a robust digital accelerator, while the main computation is performed in analog PIM units. This is the first work that not only provides a variation-robust architecture, but also improves the area, power, and energy of the existing designs considerably. HybridAC is adapted to leverage the preceding weight selection method by reducing ADC precision, peripheral circuitry, and hybrid quantization to optimize the design. Our comprehensive experiments show that, even in the presence of variation as high as 50%, HybridAC can reduce the accuracy degradation from 60 - 90% (without protection) to 1 - 2% for different DNNs across diverse datasets. In addition to providing more robust computation, compared to the ISAAC (SRE), HybridAC improves the execution time, power, area, and energy efficiency by 26%-14%, 52%-40%, 28%-28%, 57%-45%, 43%-5×, and 81%-3.9×, respectively.

1. INTRODUCTION

In the recent years, processing in memory (PIM) and near memory (PNM) have been considered as fast, energy- and area-efficient solutions to build Deep Neural Network (DNN) accelerators. Among them, ReRAM-based mixed-signal DNN accelerators have absorbed a great deal of interest due to their high throughput and energy-efficiency [6, 7, 8]. For these mixed-signal DNN accelerators an unsuitable choice of the undesired accuracy drop [41]. These properties make these mixed-signal DNN accelerators an unsuitable choice for many existing applications.

Recently, several works have proposed solutions to make these accelerators more reliable [3, 9, 18, 19, 22, 30, 32, 37, 39, 40, 57]. The closest related work was done by Dash et al. [18, 19], where they present an algorithmic solution to increase reliability as shown in Figure 1. They present an approach that selects a fraction of important weights using a hessian-based solution and put them in digital units without considering its impact on the hardware cost. We call this approach IWS. Relying on this approach leads to a weight selection with a huge irregular sparsity. Supporting this type of sparsity needs not only considerable hardware overhead but also significant data movements that results in a design with high area, power, and low energy efficiency [6, 7, 8]. For instance, IWS suggests using expensive SIGMA [45] design as a centralized digital accelerator to perform sparse computation assigned to the digital cores. However, SIGMA exploits a configurable systolic array-based architecture with remarkable interconnection overheads. Most importantly, the same input data activation needs to be replicated in both analog and digital units to support correct computation of both sensitive and non-sensitive weights even if a very small portion of the data is located in digital cores, which leads to huge data movement and hence energy consumption (Figure 1). IWS also recommends writing weights of the next layers in the same ReRAM crossbars after the finishing the current layer. That means for each layer, even if the analog unit is finished earlier, it needs to wait for a long time until the slower digital unit has finished its computation. In addition, writing into the...
same ReRAMs per layer is time/energy consuming and has endurance issue [12, 23, 35]. Moreover, weights transferred from analog to digital units leave zeros in their original positions that leads to additional memory overhead. Those zeros suffer from variations as well.

In this work, we propose HybridAC, an algorithm-hardware co-design framework that not only addresses the aforementioned problems of the baselines [18, 19], but also provides more opportunities to optimize area, power and energy consumption of the PIM-based mixed-signal accelerators.

HybridAC proposes a novel data-movement-aware weight selection method that captures a fraction of critical weight channels along with their corresponding input channels (e.g., the weights channels that are sensitive to variation and significantly contribute to the final accuracy) per layer and performs their associated computations in the proposed digital accelerator (Figure 2).

The channels are mapped to the rows of crossbars in the mixed-signal designs. Since important weight channels are entirely selected to be placed in digital units, their corresponding rows in analog crossbar units are removed uniformly. This feature evenly reduces the aggregated partial sums over the bit lines. Hence, we are able to employ low precision ADCs that significantly reduce area and power consumption with a negligible accuracy loss [28, 49]. Moreover, channel-wise sensitive weight selection enables us to quantize the weights in the analog part with lower precision compared to the digital cores without any need to retraining/post-training while maintaining minimal loss in accuracy.

In summary, HybridAC brings the following contributions:

- Unlike IWS [18, 19], the proposed channel-wise weight selection method avoids replicating the input activation and significantly reduces data movement and energy consumption.

- In contrast with the previous works [30, 40], the proposed method doesn’t need any retraining. This is important as training is a costly procedure and it may not capture all kinds of variations that may occur during run-time operation.

- The proposed solution avoids adding extra zero weights in place of transferred weights, as the whole weight channel along with its corresponding input activation are transferred to the digital units. This reduces hardware overheads compared to the IWS solutions that select important weights without considering the hardware cost [18, 19].

- For the first time, we propose a novel hybrid quantization method for different input channels per layer by considering whether the weights are mapped to digital or analog cores, without requiring any fine-tuning.

- Due to transferring important weight channels to digital cores uniformly, HybridAC enables us to utilize smaller ADC and peripheral circuitry. In conjunction with hybrid quantization, HybridAC is able to further reduce the area, power, and energy consumption of analog part significantly, where a fraction of the saved area can be utilized to add a proposed digital accelerator that is robust against variation and protects the sensitive weights.

- Since HybridAC provides a design robust to the conductance variation, we are able to activate more word-lines of the analog crossbar at the same time without being worried about the accuracy degradation.

2. PROPOSED MECHANISM

2.1 Input Channel-wise weight Selection

To address the above mentioned problems, we propose HybridAC—an end-to-end hardware-software co-design framework—to overcome the inherent imperfection of the mixed-signal DNN accelerators that includes several innovations in both software and hardware perspectives (Figure 2).

Generally, the input to a CNN model is a 4D tensor ($B \times H \times W \times C$), where $B$, $H$, $W$, and $C$ represent the batch size, height, width, and the number of channels, respectively. Similarly, weight parameters consist of $K$ number of 3D kernel tensors of dimension ($R \times R \times C$), where $K$ is the number of output channels. $R$ and $C$ denotes height (and width), and depth of the kernel which is equal to the number of channels of the input activations. We propose an algorithm that extracts weights channel-wise that are sensitive to imperfections. We then map these weights in the digital units and the rest in analog units. Algorithm 1 and Figure 2 show the proposed solution. We take already trained network parameters as input, and generate a binary mask that assigns either 0 or 1 values to all the input channels of every kernels in the network, where 1 represents that channel needs to be protected. That means we need to map it to the digital accelerator to achieve the desired test accuracy. In order to compute this mask, we need to take into account the sensitivity of each parameter with respect to the variation. The sensitivity can be calculated using either the gradient [33, 34] or the Hessian [18, 19] of the parameters. Current research shows Hessian-based solutions reach superior accuracy in terms of estimating the robustness
or sensitivity of the parameters [18]. Following that, we calculate the weight sensitivities using the equation [1] as outlined in [18]:

\[ s = \sum_{i=1}^{n} (\lambda_i |q_i|^2) \cdot w^2 \]  

(1)

Where \( w \) is the parameter matrix and \( \lambda_i, q_i \) are the eigenvalue and the corresponding eigenvector of the Hessian of the parameter matrix with respect to the training objective, and \( n \) is the number of top-eigenpairs that are considered. After calculating the summation, we estimate \( s \) by taking the Hamdard product of the obtained sum and the weight matrix, \( w \). Next, in order to reduce the redundant data-movement and avoid input data repetition, instead of considering the sensitivity values of each parameter independently as suggested in previous works [18][19], we propose input channel-wise aggregated form. If \( P \) and \( Q \) are number of input channels found to be more and less sensitive to variation, respectively, where \( Q = C - P \), then we can say the number of parameters mapped to the digital and analog accelerators for this specific kernel will be \( W_i \in R^{R_xR_yP \times K} \), and \( W_a \in R^{R_xR_yQ \times K} \), respectively. The sensitivity of a particular input channel is calculated based on the aggregation of all the parameters sensitivity values along that dimension as equation [2] shows:

\[ s_i = \sum_{K} (\sum_{R} (\sum_{R} s)) \]  

(2)

Where \( s_i \) is the aggregated sensitivity values for the \( W \) kernel. The proposed algorithm computes \( s_i \) value for all channels of all existing layers of the given DNN and sorts them according to their magnitude. Initially, it starts its computation by assuming that all channels are mapped on the analog units. Then, it applies variation to all of the weights and computes the new accuracy, \( ACC_{calculated} \). If \( ACC_{calculated} \) is less than \( ACC_{desired} \), it selects the top channel of the sorted list of channel-wise sensitive values and puts it in the digital unit to be protected from the injected noise. We repeat this procedure iteratively until we reach the desired accuracy. The output of this procedure would distinguish the channels that need to be mapped to the analog and digital units and hence the corresponding channels of input data as shown in the left side of Figure 2.

Figure 2: Illustration of the proposed input channel-wise weight selection.

Compared to the individual weight selection [18][19], the proposed solution reduces extra data movement and avoid irregular and expensive sparsity. This method also abstains from inserting extra weights with zero values in the place of transferred weights because the entire weight channel is moved to the digital units. These improvements significantly contribute in reducing energy consumption and hardware overheads.

**Algorithm 1: Input Channel-wise Weight Selection**

**Result:** Analog and Digital mapping of the channels

**Input:** Trained weights, \( \lambda_i \) eigenvalues and \( v_i \) corresponding eigenvectors, \( ACC_{desired} \).

**Calculate** sensitivity of each parameter using:

\[ s_w = (\sum_{i=1}^{n} |\lambda_i| |q_i|^2) \cdot w^2;\]

\( SOL = [\ ];\)

for \( i < num\_layers \) do

for \( j < num\_channels \) do

\( SOL_{ij} = \) channel wise aggregation of sensitivity values;

\( SOL\_append(SOL_{ij})\)

end

end

\( SOL\_sort()\);

\( Digital\_channel = [\ ];\)

\( Analog\_channel = SOL;\)

Apply noise in Analog\_channel;

\( ACC_{calculated} = \) Inference(Digital\_channel, Analog\_channel);

while \( ACC_{calculated} < ACC_{desired} \) do

channel = Analog\_channel.pop();

Digital\_channel.push(channel);

Apply noise in Analog\_channel;

\( ACC_{calculated} = \) Inference(Digital\_channel, Analog\_channel);

end

**2.2 Hybrid Quantization**

Quantization is a well-known hardware-friendly solution to reduce computation efforts and increase energy efficiency. After the quantization, the original weights and/or activations are represented with lower precision as fixed-point or integer representation while the accuracy is preserved. If we represent the original floating-point tensor by \( x_f \), its quantized by \( x_q \), the zero-point by \( z_{p_z} \), the scaling factor by \( s_z \), and the
number of bits used for quantization by \( n \), we will have [65]:

\[
x_q = \text{round}(\frac{2^n - 1}{\max_f - \min_f} x_f)
\]

where \( \max_f \) and \( \min_f \) are the maximum and minimum of the floating-point values in the analog and digital accelerators, respectively.

As shown, the scaling factor is a parameter that depends on the desired bit-precision, \( n \), and the range of tensor values (\( \max - \min \)). In a typical CNN, each output feature map for a particular layer is generated by convolving the input feature maps with a number of filters.

\[
y = \sum_{m=0}^{M-1} w_m * x_m
\]

where \( M \) is the number of input channels for the kernel of that layer and \( * \) denotes convolution operation between input \( x_m \) and \( w_m \) as 2D tensors.

The linear quantization approximates the results as follows:

\[
y_q = \text{round}(\frac{y}{s_x s_w} \sum (x_q + z_{p_x})(w_q + z_{p_w}))
\]

where \( y, x, w \) represent the output activation, input activation, and weight respectively. The other parameters that are \( s, q, z \) represent the scaling factor, quantized output, and the zero-point quantization offset, respectively.

In HybridAC, the input channel with important weights are steered to digital cores while the rest of them are fed into analog ones. Since analog and digital cores do not share any weights, they can have a different number of quantization bits and different scaling factors. Although digital and analog cores do not share activations, we consider a similar quantization for all activations. This is because one tensor can be an input to multiple layers in some DNNs (e.g., DenseNet121). The partial results of the analog and the digital cores are only added once at the end for each layer:

\[
y = y_d + y_a = \sum_{d=0}^{D-1} w_d * x_d + \sum_{a=0}^{A-1} w_a * x_a
\]

where \( A \) and \( D \) represent the number of input channels computed inside analog and digital cores and \( D + A = M \) is total number of input channels. HybridAC quantizes the weights in analog with \( n_1 \) bits and weights in digital with \( n_2 \) bits, where \( n_2 > n_1 \) as important channels are processed in digital cores.

In order to add the analog and digital partial results, we need to have them in the same scaling factor. So, before adding them together, partial results are converted back to floating points, as follows:

\[
y_{fd} = \frac{s_y}{s_x s_w} \left( \sum_{d=0}^{D-1} (x_{q_d} + z_{p_x})(w'_{q_d} + z_{p_w}) \right)
\]

\[
y_{fa} = \frac{s_y}{s_x s_w} \left( \sum_{a=0}^{A-1} (x_{q_a} + z_{p_x})(w''_{q_a} + z_{p_w}) \right)
\]

where \( s_y, s_x, s_w \) are digital and analog scaling factors, \( w'_{q_d} \) and \( w''_{q_a} \) are digital and analog quantized weights, and \( z_{p_w} \) and \( z_{p_w} \) are zero points in digital and analog domains. Instead of rounding \( y_{fd} \) and \( y_{fa} \) and then summing them up, HybridAC first adds the floating-point values and then applies the rounding operation in order to reduce the quantization error. Note that converting from quantized value to floating-point happens in all typical DNNs in the return path before feeding the results into the next layer [13][29][49]. Here an extra floating-point addition is required compared to the linear quantization described in equation [5]. We also consider the area and power overhead of the quantization circuits in the estimated results.

We use FP16 data type for \( y_{fd} \) and \( y_{fa} \) as prior work shows that FP16 accumulator is enough to preserve the accuracy during inference [2]. Our simulation results show that if the weights in the analog and digital accelerators are 6-bit and 8-bit respectively, there would be negligible accuracy loss compared with the case that both of them are in 8-bit. The main advantage of the quantization is that it will reduce the number of required ReRAM cells theoretically by a factor of \( \frac{8}{6} = 1.33 \) that will lead to less resource consumption and computation efforts. To the best of our knowledge, this is the first work that proposes hybrid quantization for different input channels per layer depending upon where those channels are placed. The proposed method does not require any post-quantization fine-tuning, as it causes minimal accuracy degradation.

3. ARCHITECTURE BUILDING BLOCKS

3.1 Analog Accelerator Units

As the right side of Figure 2 shows the analog/digital units, called analog/digital tiles, are connected on an on-chip mesh fashion. Each analog tile is composed of several multiply-accumulate units (MACs), an eDRAM buffer to store input values, shift-and-add units that compute final results, output registers to store computed results, max-pooling and non-linearity activation units that are connected with a shared bus. MAC units include inverters, multiple crossbar subarrays, ADCs, and shift-and-add units. Existing architectures [16][39] either propose to activate many wordlines at the same time and use large ADCs (i.e., 8-bit) to achieve high throughput (which is not feasible in practice due to its undesired side-effects as we mentioned in Section 1), or they propose to use smaller ADCs at the cost of having lower accuracy [41], or even activating few number of wordlines, which leads to significantly reduced throughput [56][60]. In HybridAC, we are able to activate many wordlines at the same time while using smaller ADCs with small accuracy degradation.

In the proposed architecture, channels are mapped to the rows of crossbar arrays. Since important input channels are mapped to the digital units, those rows will not exist anymore in the analog units. On the other hand, ADCs are located per bitlines. Although only small portion of the weights are mapped to the digital accelerator, they play crucial roles in the final accuracy. Removing rows with important weights causes the value of accumulated current per column to be less sensitive to the variation. Our experimental studies show that if we use ADCs with a lower precision for the crossbars where none of the rows are removed, there would be considerable
accuracy drop. However, HybridAC allows us to use ADCs with lower resolution that enables exponential reduction in the area/power [43].

Since partial sum values over the bitlines are reduced, we are now able to employ smaller sample-and-hold and shift-and-add units. Moreover, when a channel is mapped to digital units, the associated rows are completely removed from analog crossbars. This feature prevents from having redundant zeros in the analog cores that existed in the prior works [18][19]. When a percentage of the weights are placed in digital accelerators, we need fewer crossbars holding the weights. Most importantly, since noise and variation have less impact on the remaining weights on the analog units, we can activate more wordlines holding the weights. This randomness averts from proposing any scheme that works for all world lines and bitlines uniformly (e.g., exploiting smaller ADCs and peripheral circuits, activating more wordlines).

### 3.2 Digital Accelerator Units

To have a better understanding of how the architecture of a digital unit at the high level looks like, we need to have an understanding of distribution of the selected weights mapped to the digital accelerator among assorted layers. Figure 3 illustrates these results for ResNet18 over CIFAR10 data set. We observe the deviation of important weights per layer in HybridAC is less than the IWS method [18][19]. As seen, for the first and the last layers, both individual and channel-wise weight selection methods map the significant portion of the weights of these layers on digital units. The reason is that these weights are usually more sensitive to noise. Interestingly, the number of weights in the first and last layers usually is not comparable to the other layers. For instance, for ResNet18 over CIFAR10, the number of parameters in the first and last layers are 1728 and 5120 respectively while for the seventeenth layer the number of parameters is 2359296. Even recent studies show that the last linear layers can be compressed significantly (e.g., 49× for VGG16) [25][26]. We observed that if we dedicate the first and the third last tiles to digital cores, it leads to a better performance and energy consumption.

Another feature of the proposed weight selection method is that the deviation among the percentage of protected weights per layer (except first and last layers that have dedicated tiles) in HybridAC is lesser than IWS method. For example, in the case of ResNet18, the standard deviation of percentage of protected weights per layer is 4.8× less than individual weight selection (1.37 vs 6.69). We observed the same trend for all the evaluated DNNs over different datasets. That means that the proposed approach provides more uniform weight selection distribution rather than the IWS [18][19]. This property simplifies the hardware of HybridAC and increases resource utilization.

Figure 4 demonstrates the building blocks of the digital accelerator. Unlike conventional accelerators like Eyeriss that put PEs one side and large buffer/memories on another side of the chip, we distribute tiny SRAMs throughout the chip besides computation units. The proposed architecture is inspired by WAX design [24]. In each tile, we employ a tuple of tiny SRAM, a MAC unit, and three registers including activation register, weight register, and partial sum register. In HybridAC, we utilize short interconnections, where it connects small SRAMs. These small SRAMs have been distributed among tiles and bring high data reuse of both weight and activation.

In HybridAC, we replace 54KB global SRAM buffer of Eyeriss [13] (considering 8-bit weights) or 6KB SRAM buffer of WAX [24] with 1KB buffer access (5.2× energy reduction). Like WAX architecture [24], we replace 12- and 24-entry register files and 224-byte scratchpad in Eyeriss with a single register access. Unlike WAX, these units are connected through a grid structure rather than H-tree. This brings the advantages of more bandwidth, less area, and better energy efficiency as demonstrated in the previous works [14][50]. Using H-tree makes the distance between these two neighbors as bad as \( \log(\text{chipwidth}) \). Although far tiles can communicate together thorough the grid structure, each tile usually needs to access each local SRAM or its neighbors (e.g., unlike WAX) or large, far-distant SRAMs (e.g., unlike Eyeriss-like designs). WAX architecture also needs additional muxing at each split point of its H-tree [46]. These hierarchical muxing is essential so that data from a neighboring sub-array is guided either to the other adjacent sub-array or to a central complex controller. This complex controller unit is eliminated in our proposed architecture.

Additionally, the number of required units is almost 20% of WAX because small portions of the weights are mapped to digital units.

The digital part of these tiles is located face to face to reduce wire length communication. Besides, unlike WAX, each SRAM has 1 row for activations, 24 rows for weights, and 7 rows for partial sums (6× size reduction).

### 3.3 Mapping Mechanism

The hierarchical structure of the HybridAC enables to reduce data movement between different sub-units, having fewer wordlines and bitlines, and having higher internal band-
We discuss more about the load balancing of HybridAC in Section 5.4.2.

4. SIMULATION SETUP

We evaluated five different DNNs, VGG16, ResNet18, ResNet34, Densenet121, and EfficientNetB3 over CIFAR10, CIFAR100, and ImageNet datasets. For all datasets, we compute five eigen pairs (values and vectors) as it has been demonstrated to deliver negligible accuracy drop [18,19]. Simulation are performed in a hardware setup consisting of Intel 10th gen core i7, 110 CPU and Nvidia GTX-1080Ti GPU.

We developed an in-house simulator to obtain the area, power, energy, and throughput of the HybridAC and evaluated baselines. Figure 6 shows the overall flow of the developed simulator. It uses PyTorch API to get the accuracy and weight distribution as the algorithm-side is implemented in PyTorch. The tool utilizes NVSIM [21], Cacti [5], and PIM primitives library [53] as backbone simulators to perform design space exploration and gets required inputs of the architectural simulator. For the architectural simulator, we modify MNSIM [64] to model the proposed hardware of analog units and also evaluated baselines. The tool is enriched with a digital simulator that mimics the proposed data flow.

Previous works [19,40] suggest that conductance variation of the individual devices in a PIM design can be modeled by a Gaussian distribution of noise with 0 mean and a standard deviation proportional to the stored parameter value. Eq. 9 shows the noise model considered in our work:

\[ \text{noise}_{\text{model},x} \sim \mathcal{N}(0, \sigma_w) \]

We consider \( \sigma = 50\% \) and \( \sigma = 10\% \) for the weights in analog and digital cores, respectively. We employ the VTEAM ReRAM model [36] and follow the methodology of ISAAC to model max-pooling, shift-and-add, ADC, and activation functions. The power and area of the shift-and-add, max-pool, and ReLU are taken from ISAAC [49] and PRIME [16].

We employ HyperTransport serial links the same as the one used by ISAAC [49] and DaDianNao [15].

To get the power and area of ADC, we use the most updated dataset [44]. To extract the area and power of the same ADC but with a lower resolution, we scale down the power and area of the memory, clock, and \( vref \) buffer linearly, and the capacitive DAC exponentially as explained in [48]. We choose this methodology to model peripheral circuitry and make a fair comparison at 32nm with state-of-the-art works. We also compare the results with the fully digital SIGMA [45]. We examine both offset subtraction-based designs [4,49,56], (i.e., HybridAC, HybAC) and differential cell-based designs [16,31,53] (i.e., HybridACDi, HybACDi) to show HybridAC mechanism is independent to the underlying architecture.

We implemented the RTL design of the proposed digital units and the baselines using Verilog-HDL that enables us to compute the power and area more accurately. We utilize Synopsys Design Compiler at 28nm, a Low Leakage library, and a clock frequency of 1GHz to synthesize the digital design.
To get SRAM results we utilize Synopsys memory compiler. We employ Innovus to conduct the layout for the digital part, where the extracted SRAM using memory compiler is used in the layout as a hard macro. The results are scaled up to 32nm. The extracted results are back annotated in the developed simulator to help us to get more accurate numbers.

5. RESULT

5.1 Accuracy vs Protected Weight Percentage

Table 1 illustrates the accuracy results of CIFAR10/100 dataset of the proposed approach and compare it with the IWS method [18,19]. We repeat the experiment 50 times and get the average of the results. The third column shows the accuracy when there is no variation. The fourth column shows the results when there are 50% and 10% variations for the weights placed in the analog accelerator. The “%Selected Weights” column shows the percentage of the weights that need to be placed in digital cores to reach the desirable accuracy, which is typically less than 1% of the original accuracy [7]. Plots demonstrate the results along with its trend over ImageNet dataset. The x axis shows the protected weight percentage and the y-axis shows the accuracy. For ImageNet, the accuracy without any protection mechanism is 7.25%, 17.13%, and 4.4% for ResNet18, ResNet34, and DenseNet121, respectively.

As the results illustrate, the amount of the weights that needs to be protected to reach the desired accuracy varies depending on the DNNs, dataset, number of layers, parameters, and most importantly weight distributions. In general, when the DNN and dataset become more complex, the amount of protected weight is increased. For example, the percentage of protected weight for ImageNet is more than CIFAR100 and for CIFAR100 is more than CIFAR10 for the same DNN. On the other hand, for the same dataset, in general, DenseNet121 needs the highest weight percentage to be protected among evaluated networks.

Compared with the IWS, the HybridAC pushes more weights to the digital units since it selects the whole channel rather than choosing the individual weights. Fortunately, this mechanism leads to a better load balancing and higher hardware utilization. We discuss this feature in Section 5.4.2.

5.2 ADC Resolution

In theory, the required bits for a full ADC resolution is computed using the equation [10,49].

$$\text{ADC}_{\text{bits}} = \begin{cases} v + w + \log(r), & \text{if } v > 1 \text{ & } w > 1 \\ v + w + \log(r) - 1, & \text{otherwise} \end{cases}$$ (10)

Where $v$ denotes number of bits per input, $w$ shows weight bits stored per ReRAM cell on the crossbar arrays, and $r$ represents activated wordlines per crossbar array [49]. For the evaluated architecture, we consider 2 bits per cell while 128 rows can be activated at the same time and the number of bits per input is 1. We employ the same encoding technique used in ISAAC to save 1-bit ADC. Accordingly, for the mentioned configuration, the required ADC resolution with zero accuracy loss assuming there is no source of variation is 8 bits.

Table 2 shows accuracy results when ADCs with different resolutions are used for HybridAC with bias and offset subtraction architecture (i.e., HybridAC), baseline (i.e., IWS [19]), and also differential cell architecture (i.e., HybACDi, IWSdi).

As the results illustrate, for 7-bit ADC, in the case of CIFAR10/100 the accuracy results of IWS is slightly higher than HybridAC because its original accuracy is higher. However, by reducing ADC resolution, the gains of the proposed solution become more apparent. For instance, in the worst case, 0.29%, 0.45%, and 0.66% accuracy drop happens for CIFAR10, CIFAR100, and Imagenet datasets, respectively. Nonetheless, using IWS method [19], the accuracy drops are 0.98%, 1.95%, and 3.87%, respectively, which, however comes at the cost of using higher bit-resolution (i.e. 8-bit) ADC.

In the proposed design, the channels are mapped to rows. Hence, by transferring a channel, the whole row values are moved to the digital accelerator. ADCs are defined per bitlines. Removing (a) row(s) will have an uniform impact on whole bitlines of a crossbar and hence ADC resolution. For IWS method [18,19], we are not able to have the same ADC for all bitlines. The reason is that important weights have a random distribution. As a result, the number of important weights may change dramatically by going from one bitline to another one. Furthermore, although only small portion of channels are transferred to the digital accelerator, they have a greater impact on the final accuracy. Removing these critical weights enables us to employ ADCs with smaller resolution and less area/power while having minimal accuracy drop.

In the last two columns, we assess more extreme situations where we use 4-bit ADCs and reach almost the same accuracy as 6-bit ADC but through different architecture. The reason is that, here, we examine differential cells [16,31,58] where two separated crossbars are used for matrices with positive and negative weights. Unlike bias and offset subtraction cells [4,49,50], this mapping does not add biases to the weights, and accordingly their corresponding conductance are reduced. This is helpful as in many DNNs, zero and low-value weights contribute significantly in distribution of weight values [27,62,63]. Accordingly, the conductance (weight) variation and parasitic voltage drop across the crossbar columns (rows) are decreased, that results in a higher accuracy. This fact shows that the proposed method is independent of the underlying architecture. It is noteworthy to mention that differential cell-based design have more hardware overhead and generally less throughput than offset-based designs.

Reducing ADC resolution is important as ADC contributes more than 30% of tile area and 50% of tile power in many architecture [49]. Having 7-bit ADC instead of 8-bit will save 7% area and 14% power of the tile. In the case of 6-bit ADC, the saving area and power of the tile would be 13% and 29%. By employing 6-bit ADC and pushing a percentage of weights to digital units as shown in the Table 1 and Figure 7 with the acceptable accuracy drop, the power/area saving is considerable. Obviously, by pushing more weights to digital accelerator, we can increase the accuracy at the cost of having lower throughput and performance.

5.3 Hybrid Quantization
Table 1: Comparing the impact of IWS and HybridAC approaches on accuracy over CIFAR10/100 datasets

| DataNet | DNN       | Original Accuracy with No Noise | Accuracy with PV Both | %Selected Weights | Accuracy IWS [18] | %Selected Weights HybridAC | Accuracy HybridAC |
|---------|-----------|---------------------------------|------------------------|-------------------|-------------------|-----------------------------|------------------|
| CIFAR10 | VGG16     | 92.01%                          | 27.53%                 | 3.00%             | 91.81%            | 10.00%                      | 91.89%           |
|         | ResNet18  | 94.76%                          | 25.66%                 | 4.00%             | 94.53%            | 10.00%                      | 94.26%           |
|         | ResNet34  | 93.93%                          | 55.01%                 | 6.00%             | 92.98%            | 9.00%                       | 92.94%           |
|         | DenseNet121 | 94.96%                        | 22.77%                 | 6.00%             | 94.32%            | 11.00%                      | 94.04%           |
|         | EfficientNetB3 | 95.22%                      | 23.88%                 | 5.00%             | 94.46%            | 10.00%                      | 94.36%           |
| CIFAR100| VGG16     | 69.29%                          | 13.2%                  | 4.00%             | 68.35%            | 12.00%                      | 68.30%           |
|         | ResNet18  | 74.07%                          | 13.86%                 | 8.00%             | 73.73%            | 13.00%                      | 73.71%           |
|         | ResNet34  | 74.78%                          | 24.28%                 | 8.00%             | 74.06%            | 14.00%                      | 74.00%           |
|         | DenseNet121 | 73.93%                        | 10.16%                 | 10.00%            | 73.12%            | 16.00%                      | 72.80%           |
|         | EfficientNetB3 | 82.35%                      | 13.20%                 | 8.00%             | 81.61%            | 14.00%                      | 81.50%           |

Table 4 demonstrates the impact of hybrid quantization along with various ADC resolutions on the final accuracy. The second column shows the impact of hybrid quantization where important weights in digital cores are 8-bit and less important weights placed in ReRAM crossbars are 6-bit. As seen in the best and the worst case scenarios, the accuracy drops by 0.09% (i.e., ResNet18/CIFAR10), and 0.53% (i.e., DenseNet121/ImageNet), respectively, compared to the situation where all weights are 8 bits. The last column shows the impact of hybrid quantization along with employing 6-bit ADC together. As shown, in the best case (ResNet18/CIFAR10) 0.30% and in the worst case (DenseNet121/ImageNet) 1.11% accuracy loss happens, compared to the situation when there is no smaller ADC and hybrid quantization.

As we mentioned in Section 2.2, mapping important channels in the digital and others in the analog units enables us to have the first work that proposes a mixed-precision quantization schemes for different input channels of a single layer without any need for retraining. Obviously, by employing post-quantization fine-tuning, we can even achieve smaller quantization bits [20][22].

5.4 Comparison with More Related Works

5.4.1 Power and Area

Table 5 shows the power and the area of different components of HybridAC and its comparison with ideal-ISAAC as a baseline architecture in details. Tables 6 and 7 summarize the numbers of Table 5 considering the required number of MCUs and Tiles in more coarse granularity. These tables also compare the power and area of HybridAC with assorted baselines. As we discussed in the Section 3.1, because of moving critical weights to the digital cores, HybridAC needs fewer crossbars, smaller peripheral circuitry such as eDRAM, ADC, and sample-and-hold logic. HybridAC needs bigger quantization circuitry as we explained in Section 2.2. However, it requires only 8 MCUs per tile, while other designs usually need 12 MCUs per tile. In addition the total number of required tiles reduces from 168 (in ISAAC) to 148. The bottom of the Table 5 provides the power and area of the digital accelerator of HybridAC.

As demonstrated, HybridAC provides 28% better area and 57% better power compared to ISAAC. For IWS [18][19], we consider two different approaches. In the first one (IWS-1), there is only 1 tile and the weights are written into crossbar cells after every layer is finished. Although this approach saves the area and power of the analog unit, the performance and the throughput will drop significantly. The reason is that writing the weights into ReRAM cells takes a considerable amount of time (e.g., 50ns unipolar and 200ns bipolar). Moreover, we need to write into a cell multiple times to make sure it has a correct value [54]. Using the same tile for writing the weights of all layers makes the endurance issue of ReRAM technology worse [43]. Besides, this method limits the parallelism to only one tile.

Accordingly, most of the existing works [16][18][49] will consider another approach where they write all (or most) weights once into the different crossbars in various tiles. IWS-2 follows this methodology. It impose weights overheads as they leave zeros in the crossbars in the place of the weight that are transferred to digital units. Those zeros (up to 22% in the case of DenseNet121/ImageNet) that randomly are distributed among other weights add up to 400 more crossbars to existing ones, which increase area, energy and execution time.

HybridAC improves the power and the area of the IWS-2 [19] by 65% and 2.1 × respectively. IWS-1 has a slightly better power (e.g., 1%) and worse area than HybridAC (47%) due to using costly SIGMA [45] that has high power and area.

As a digital accelerator, SIGMA exploits a configurable systolic based architecture with a lot of interconnection overheads. Consequently, SIGMA has a relatively lower area efficiency (i.e., 155 GOPS/mm²). In comparison with SIGMA, HybridAC provides 15% better area. HybridAC outclasses...
FORMS [60] by 44% (29%) in terms of power and area, while the improvement over SRE [56] are 45% (27%). Although digital accelerators show better power consumption, the area and power efficiency of the HybridAC outperforms the existing accelerators as Table 4 shows.

### 5.4.2 Comparison Summary: Area/Power Efficiency

Table 4 presents the area and power efficiency of HybridAC (e.g., using 6-bit ADC) and HybridACDi (using 4-bit ADC) and also assorted digital and analog accelerators. As seen, HybridAC and HybridACDi outperform all of them while they are more immune to variation. The efficiency of HybridAC comes from the novel design that utilizes smaller ADCs, hybrid quantization, fewer crossbars, and tiny but high throughput digital accelerator. The area- and power-efficiency of Ideal-ISAAC (e.g., it idealistically activates 128 wordlines)

Table 4: Peak area- and power-efficiency of different architectures normalized to Ideal-ISAAC.

| Architecture | $GOPS_{s \times mm^2}$ | $GOPS_{s \times mm^2}$ |
|--------------|------------------------|------------------------|
| Ideal-ISAAC  | 1                      | 1                      |
| PUMA         | 0.70                   | 0.79                   |
| SRE          | 0.19                   | 0.26                   |
| FORMS8(not pruned) | 0.54               | 0.61                   |
| FORMS16(not pruned) | 0.77               | 0.84                   |
| DaDianNao    | 0.13                   | 0.45                   |
| TPU          | 0.08                   | 0.48                   |
| WAX          | 0.33                   | 2.3                    |
| SIMBA        | 0.34-0.62              | 0.08-2.4               |
| IWS-1        | 0.13                   | 0.15                   |
| IWS-2        | 0.38                   | 0.41                   |
| HybridAC     | 1.43                   | 1.81                   |
| HybridACDi   | 1.75                   | 2.5                    |

Figure 8: Accuracy vs area-efficiency comparison for different architectures for ResNet18 inference on CIFAR10.

Table 3: Comparing impact of hybrid quantization on accuracy.

| DSet | DNN | 8-bit | 8-bit | 7-bit | 7-bit | 6-bit | 6-bit | 6-bit | 4-bit | 4-bit | 4-bit | 4-bit |
|------|-----|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|      |     | HYBAC | IWS   | HYBAC | IWS   | HYBAC | IWS   | HYBAC | IWS   | HYBAC | IWS   | HYBAC |
| VGG16| 91.69 | 91.57 | 91.46 | 91.45 | 91.15 | 91.39 | 91.05 |       |       |       |       |       |
| ResNet18 | 94.26 | 94.53 | 94.20 | 94.31 | 94.05 | 93.90 | 93.98 | 93.82 |       |       |       |       |
| C10 | 92.94 | 92.98 | 92.85 | 92.71 | 92.47 | 92.85 | 92.41 |       |       |       |       |       |
| DenseNet121 | 94.04 | 93.32 | 93.89 | 94.09 | 93.75 | 93.34 | 93.62 | 93.29 |       |       |       |       |
| EfficientNetB3 | 94.36 | 94.46 | 94.26 | 94.39 | 94.12 | 93.66 | 94.01 | 93.61 |       |       |       |       |
| VGG16 | 68.30 | 68.35 | 68.11 | 68.01 | 67.98 | 66.66 | 67.88 | 66.57 |       |       |       |       |
| ResNet18 | 73.51 | 73.73 | 73.40 | 73.43 | 73.23 | 72.17 | 73.17 | 72.09 |       |       |       |       |
| C10 | 73.99 | 74.06 | 73.85 | 73.85 | 73.69 | 72.54 | 73.52 | 72.48 |       |       |       |       |
| DenseNet121 | 81.30 | 81.61 | 81.37 | 81.42 | 81.25 | 81.08 | 81.13 | 80.95 |       |       |       |       |
| EfficientNetB3 | 89.21 | 91.29 | 89.99 | 90.75 | 86.65 | 87.08 | 86.50 | 86.95 |       |       |       |       |
| ResNet18 | 71.98 | 72.20 | 71.84 | 70.00 | 71.53 | 68.95 | 71.42 | 68.81 |       |       |       |       |
| DenseNet121 | 72.91 | 72.91 | 72.61 | 72.28 | 72.25 | 69.04 | 72.12 | 68.92 |       |       |       |       |

5.4.3 Execution Time and Energy Results

The results of execution time and energy of different DNNs using different methods over CIFAR100 dataset are demonstrated in Figures 9 and 10 where ideally assuming even ISAAC and SRE are immune to noise (ISO-accuracy). We mimic the behaviour and data flow of the evaluated architectures using our in-house simulator.

On average, the execution time of Ideal-ISAAC is 3.6× and 1.6× better than IWS-1 and IWS-2 [18, 19], respectively. Due to exploiting activation and weight sparsity, SRE [56] can outperforms ISAAC by 15×; however, by having weight and activation as 8-bit rather than 16-bit, the sparsity exploitation is reduced. In addition, SRE has substantial column/row
Table 5: Power and area of different components of HybridAC and its comparison with ISAAC table:

| Component          | Parameter       | Spec | Power(mW) | Area(mm²) | Spec | Power(mW) | Area(mm²) |
|--------------------|-----------------|------|-----------|-----------|------|-----------|-----------|
| cDRAM Buffer       | size            | 32KB | 11.2      | 0.041     | 64KB | 20.7      | 0.08      |
|                    | num-bank        | 2    | 40.8      | 0.232     | 2    | 40.8      | 0.232     |
|                    | Bus-width       | 256  |           |           | 256  |           |           |
| cDRAM to IMA Bus   | num-wire        | 384  | 7         | 0.09      | 384  | 7         | 0.09      |
| Router             |                 |      |           |           |      |           |           |
| Activation         | number          | 2    | 0.364     | 0.00042   | 2    | 0.364     | 0.00042   |
| S+A                | number          | 1    | 0.035     | 0.000042  | 1    | 0.035     | 0.000042  |
| Max-pool           | number          | 1    | 0.28      | 0.00016   | 1    | 0.28      | 0.00016   |
| Quantization Circuitry | number     | 1    | 0.0065    | 0.00098   | 1    | 0.0025    | 0.00040   |
| Output-Register    | Size            | 3KB  | 1.176     | 0.00224   | 3KB  | 1.176     | 0.00224   |
| ADC                | resolution      | 6-bit| 9.6       | 0.0062    | 8-bit| 16        | 0.0096    |
|                    | frequency       | 1.2GHz|          |           | 1.2GHz|           |           |
|                    | number          | 32   |           |           | 8    |           |           |
| Inverter (1-bit DAC) | resolution    | 1-bit| 4        | 0.00017   | 1-bit| 4        | 0.00017   |
|                    | number          | 8×128|          |           | 8×128|          |           |
| S&H                | number          | 8×128| 0.007    | 0.00003   | 8×128| 0.01     | 0.00004   |
| Crossbar Array     | number          | 8    | 2.4      | 0.00024   | 8    | 2.4      | 0.00024   |
|                    | size            | 128×128|       |           | 128×128|       |           |
|                    | bit/cell        | 2    |           |           | 2    |           |           |
| S+A                | number          | 4    | 0.2      | 0.000024  | 4    | 0.2      | 0.000024  |
| Local SRAM         | number          | 152  | 303.71   | 0.88      | ---  | ---      | ---       |
| MACs               | number          | 152  | 480.36   | 1.11      | ---  | ---      | ---       |
| Weight Register    | number          | 152  | 111.22   | 0.37      | ---  | ---      | ---       |
| Activation Register | number        | 152  | 150.26   | 0.42      | ---  | ---      | ---       |
| PSum Register      | number          | 152  | 95.23    | 0.39      | ---  | ---      | ---       |

Table 6: Comparison of total power and area of HybridAC with different baselines:

Table 7: Comparison of total power and area of HybridAC with different baselines: Continued table:

indexing overhead and relatively lower throughput as it activates only 16 rows. In HybridAC-10%, we assume up to 10% of weights can be transferred to digital cores. Hence, if a design needs more percentage of weight to be mapped to the digital cores, it needs to wait until the existing digital cores become available for the next computation.

As the plots show, due to load unbalancing issue, the results of HybridAC-10% are worse than ISAAC and SRE. Following our discussion in Section 5.4.2, by moving more weights to the digital cores (up to 16%), we can have a better load balancing that leads to improved timing and energy results. This amount best fits for the evaluated DNNs except DenseNet121 over ImageNet as the results in Table 1 and Figure 7 shows. That is why HybridAC-16% provides promising results. It improves the ISAAC timing by 26% and SRE by 14%. It is worth mentioning that having a perfect mapping and load-balancing for the mixed-signal designs is still an open challenge which is out of the scope of this work.

For power consumption, HybridAC consumes less power, has a shorter execution time. As we discussed in Section 3, since the digital and analog cores do not share any input activations –while in the IWS baselines the same input data of analog needs to be replicated in digital units even if very few weights are transferred to digital cores–, HybridAC-16% consumes less energy than the corresponding baselines. Since HybridAC-10% has longer execution time, its energy consumption is more than HybridAC-16% and SRE. In average, HybridAC-16% improves energy consumption over Ideal-
ISAAC, SRE, IWS-1, and IWS-2 by 52%, 40%, 8.9×, and 5.6×, respectively. Being faster and consuming less energy than the evaluated baselines leads to a better energy-delay product as well. It is noteworthy to mention that in practice, neither ISAAC, nor SRE are immune to weight variation and noise, which made them impractical for real-world applications.

Figure 9: Execution time of different DNNs using different architectures

Figure 10: Energy consumption of different DNNs using different architectures

5.4.4 Avoiding Accuracy Drop by Activating more Wordlines

As we discussed in Section 2, existing mixed-signal designs especially those that rely on bias and offset subtraction method cannot activate many wordlines at the same time. This problem can be mitigated if we can make the important weights immune against variations. Figure 11 shows our simulation study on different scenarios for ResNet18/CIFAR10 where we increase the $R - \text{ratio} = \frac{R_{on}}{R_{off}}$ and decrease conductance deviation ($\sigma$). The first plot (e.g., red one) considers $R - \text{ratio}$ of VTEAM model [36] and $\sigma = 50\%$ as a baseline ($R - \text{ratio} = R_0$). The second and third plots are for the situations when $R_{ratio} = 2R_0$, $\sigma = \sigma_b/2$ and $R_{ratio} = 3R_0$, $\sigma = \sigma_b/3$, respectively. The last one shows the behaviour of HybridAC. These figures show that the amount of the accuracy degradation is considerable in practice while HybridAC can reduce such an accuracy drop to less than 0.9%.

5.4.5 Accuracy Improvement Studies

Feinberg et al. propose an error correction scheme using AN-code to restore the accuracy loss [22]. AN codes rectify errors in linear functions and only consider the random telegraph noise. Moreover, it adds considerable hardware overheads, which makes it less scalable [30]. Prior works activate fewer wordlines and rely on ADC quantization to surpass the propagated errors [60,61]. However, this solution cannot completely resolve the issue. Besides, their methods show lower throughput and area/power efficiency. The method proposed by Liu [39] requires fine-tuning the network. This work replaces the final linear classification layer with a set of collaborative logistic classifiers to overcome the performance degradation, which needs retraining and add hardware overheads. In addition, modern image classifier architecture (e.g., SqueezeNet) does not incorporate any linear layer for making the final decision. Long et al. consider a Gaussian noise model and propose an algorithmic solution that needs retraining by incorporating the modeled noise [40]. Similarly, CxDNN utilizes a retraining method to recover accuracy loss due to the digital to analog conversion [30].

However, retraining-based approaches are less effective when models of variations assumed during retraining do not accurately match the variations experienced by the hardware during inference. In general, exact and comprehensive modeling of noise is a hard task that makes retraining-based methods less effective.

6. CONCLUSION

In HybridAC, for the first time, we propose a novel algorithm hardware framework that minimizes accuracy degradation, data movement, and energy consumption. We propose an input channel-wise weight selection method, where the important channels along with their corresponding input data are moved to a novel tiny digital accelerator. Our proposed method avoids input data replication and adding weight overheads. Besides, unlike the existing solutions, it does not require any retraining. In addition, it enables us to use a fewer number of crossbars, smaller peripheral circuitry, and ADCs with lower precision. The proposed solution also unlocks hybrid quantization where we have different quantization bits for different input channels per layer depending on where those channels are mapped to (i.e., analog or digital). We believe HybridAC gives an insight that having hybrid accelerator not only provides more immunity to noise and variations, but also promises a better area/power efficiency compared to the current mixed-signal accelerators.

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