A High Performance and Robust FIFO Synchronizer-Interface for Crossing Clock Domains in SFQ Logic

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Abstract—Digital single-flux quantum (SFQ) technology promises to meet the demands of ultra low power and high speed computing needed for future exascale supercomputing platforms. However, clocking SFQ logic circuits remains a challenge due to the presence of a large number of on-chip clock sinks, and hence, decomposing large designs into multiple independent clock domains similar to CMOS, have been proposed. However, such clock domains demand efficient synchronizing First-in-first-out (FIFO) buffers and robust interfaces to safely transfer data from one clock domain to another. In this brief, we propose such a FIFO synchronizer and clock-domain crossing interface for both uni and bi-directional data transfer without any significant degradation of the clock frequency. Our proposal scales to complex gate-level pipelined SFQ logic cores while demonstrating extremely low Bit Error Rate (BER) and is unaffected by noise, given current SFQ lithography feature sizes.

Index Terms—SFQ, crossing clock domain, interface, BER.

I. INTRODUCTION

As we face the fundamental limits of physical scaling dictated by Moore’s law, single flux quantum (SFQ) [1] has emerged as a promising beyond-CMOS logic technology, thanks to its switching energy per bit of $\sim 10^{-19} \text{ J}$ [2] and the potential to support clock frequencies up to 770 GHz [3]. Motivated by its’ promise, many researchers have successfully demonstrated cryogenic arithmetic logic units [4] and low-complexity microprocessors [5]–[7]. Recently, several energy-efficient variants of SFQ technologies have also been explored [8]–[11]. However, the potential of three orders of magnitude lower power consumption (in the case of non-resistive bias networks [8]) at an order of magnitude higher frequency [1], has still not been realized, primarily due to i) high process variations and non-idealities [1], [12], and ii) the lack of a three-terminal controllable switch element.

In particular, the gate-level pipelining and ultra-high clock frequencies associated with SFQ logic makes low-skew clock distribution extremely challenging [13]. As a result, a 1 THz device was forced to function at a disastrous 20 GHz frequency [14]. Previous work [15] addressed this clocking challenge by decomposing the SFQ design into several independently clocked blocks, i.e., into multiple clock domains, similar to how heterogeneous CMOS designs are managed. Moreover, increasing integration densities in SFQ logic [16] can drive SFO circuit designers to implement increasing numbers of on-chip clock domains. However, in the traditional design approach, circuitry within each clock domain is designed using a dedicated clock. Since these clock domains have no phase relationship, static timing constraints cannot be created to guarantee safe data transfer. Hence, the setup time of flip-flops (FFs) at the boundary of these domains may be violated. They can thus exhibit metastability [17] and high BER.

As timing constraints cannot be guaranteed between clock domains, safe/robust communication between them sometimes takes place either at a rate slower than the system clock (e.g. one transfer for every two cycles of the clock) or with some kind of mixed asynchronous design [17], [18]. While synchronizers for SFQ logic have been previously proposed [15], this paper is the first to propose a robust, high performance synchronizer that has flexible and robust read/write interfaces that support high-throughput bi-directional communication between asynchronous clock domains.

The remainder of the paper is organized as follows. Section II provides related background on SFQ, including descriptions of the SFQ crossing clock domains and First-in-first-out (FIFO) synchronizers, and identifies the key bottlenecks in previous synchronizer designs [15]. Section III presents two improvements over [15] and the associated interface for unidirectional communication. Section IV proposes a custom interface design to enable bi-directional communication between two clock domains. Section V performs JSIM [19] simulations to demonstrate the efficacy of the proposed synchronizer-interface. Finally some conclusions are given in Section VI.

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III. Uni-directional Communication

In this section, we present our proposed synchronizer and interface, illustrating uni-directional communication between two unrelated clock domains. Our FIFO is shown in Fig. 3(a).

A. Proposed Synchronizer

The first improvement in our proposed synchronizer over [15], [20] is that the newly proposed synchronizer accepts an additional enable signal from the write side notifying an intent to write data to the FIFO. Thus our proposed FIFO does not need to receive data every clock cycle, providing more flexibility to the designer. Moreover, this FIFO has a ready signal that is asserted when the FIFO has an empty pipeline stage in which it can accept new data. The cost of this flexibility, however, is that there is a two clock cycle delay between the enable and ready signal, and hence, we can write new data into the FIFO at most every other clock cycle.

In particular, after the ready and enable signals are asserted, the lower C-element produces a clock pulse that reads the new data into the FIFOs datapath and helps move this data forward through the FIFO with successive pulses on the read clock. The ready signal also sends out a pulse when the ~enable is active and the FIFO can still accept new data. The combination of these two distinct situations is implemented using the OR gate in the FIFO control path. Note that the enable and ~enable signals are mutually exclusive, and should arrive in the same clock cycle as new data is available.

Since all SFQ logic gates are clocked, the OR gate, followed by the DFF, function similar to a two-flop synchronizer.

Should the output of the synchronization OR gate become metastable, it still needs to propagate through the DFF next to it, before its value is used by the write side interface. The extra time provided by the additional synchronization DFF increases the probability that the metastable value will resolve, and is the second improvement in our design. The result is that the FIFO has low BER in the write side, as detailed in Section IV. On the read side, as proposed in [15], the data and valid signal might come out in different clock cycles if the valid signal arrives late, thereby corrupting the data transfer. Therefore, inspired by [15], [21], we employ two back-to-back DFFs to drive the read interface and make the probability of a late valid signal negligible.

Although the above description assumes noiseless synchronizers, a real system has noise and the resolution to 0 or 1 of a DFF synchronizer near its metastable point is a stochastic process. Fortunately, [22] proves that the presence of noise has almost no effect on the BER of a two-flop SFQ synchronizer due to metastability. Since our design involves two sequential clocked logic gates (OR and DFF), the same conclusion holds true in this design.

B. Interface

Upon reset, the write side of the FIFO interface assumes the FIFO is empty and that it can start operating by sending an enable signal to the FIFO. The output of the synchronizing DFF in the control path, along with the

*We show a 3-stage synchronizer, however, the optimal number of stages actually depends on throughput and burstiness constraints [20].
split write clock pulse, trigger the FIFO C-element $C_1$ and its split output produces the ready pulse, informing the write interface that it can accept new (enabled) data. Once consumed data propagates to the read side of the FIFO, a read clock pulse will produce a valid pulse, and the associated data can be read out. Unlike the write side, we can read out one data token every clock cycle, provided the read clock frequency abides by the timing constraints detailed in Sec IV-B. In principle, generic finite state machines (FSMs), as shown in Fig. 3(b), can manage the data transfer to/from our proposed FIFO protocol.

IV. BI-DIRECTIONAL COMMUNICATION

Whenever incoming or outgoing FIFO data is blocked, the interface logic must stall to avoid losing new data or overwriting old data, respectively. Stalling is typically implemented by gating the associated interface clock. However, the gate-level clocking nature of SFQ logic implies that the clock distribution networks (CDN) will have relatively high insertion delay which makes efficient clock gating difficult. To address these issues, we develop a custom circuit solution that can enable high throughput communication between clock domains. In particular, we propose a custom CDN and interface for our proposed FIFO that can support bi-communication between clock domains.

A. Design Details

Our design employs two FIFOs, and hence has two valid and ready signals, which together with the proposed interface, enable bi-directional data transfer. Each interface receives data from one FIFO and writes to the other. The valid signal generated by the first clock domain controls the data transfer to the FIFO clocked by the second clock domain. Once this second FIFO successfully receives a token from the interface, its’ ready port generates a pulse, which along with the valid pulse from the first clock domain controls the transfer of the next token between the interface and FIFO $1$. Note that this valid pulse will be generated when the other interface similarly communicates with FIFO $1$.

Our proposal is explained below in detail and illustrated in Fig. 4 where each NDRO is denoted as ND. We also note that logic gates that are connected in a local loop in the clock domain datapath, can be grouped and clocked together using one of the locally generated clocks. Note that the NDs and the DFFs in the control FSMs of both the datapaths are preset to logic ‘1’ assuming each pipeline stage holds valid data. Also, note that the clock, reset, and I/O pins are at the top, bottom, and either sides of the ND respectively in Fig. 4.

The steps involved in the bi-directional communication are described below and illustrated in Fig. 5.

1) When the first pulse of $CLK_1$ arrives, every ND will produce an output pulse, then the preset DFFs will each generate an output pulse that clocks their respective pipeline stages and, concurrently, reset their associated NDs. For example, the first ND will be reset by the pulse on the net labelled ‘e’. Also, note that this same sequence of actions happens in parallel in domain $CLK_2$.

2) When the second $CLK_1$ pulse arrives, only the leftmost ND directly connected to FIFO $1$ will produce an output pulse because the others have been reset in the previous cycle. The last DFF in the FSM control, denoted FSM$_1$ in Fig. 4, in addition to resetting the ND receiving the signal ‘5’ in its’
Fig. 5. Timing diagram of the dataflow for the proposed circuit shown in Fig. 4. The first two cases illustrate the read side of the FIFO with and without the presence of a valid pulse and second two cases illustrate the corresponding behavior on write side of FIFO. \( T_n, T_s, T_d, T_c \) and \( n \) represent the NDRO clock-to-Q delay, splitter delay, DFF clock-to-Q delay, C-element delay, and the bit-width of the data respectively.

### TABLE I

| Number of Stages | JJ-area of 32-bit previous FIFO [15] (\( \mu m^2 \)) | JJ-area of 32-bit proposed FIFO (\( \mu m^2 \)) | % Increase in JJ-area |
|------------------|-----------------------------------------------|-----------------------------------------------|-----------------------|
|                  | C-elements | DFFs | Splitters | Total | C-elements | DFFs | Splitters | OR gates | Total | Total |
| 3                | 7(1)       | 897.68(98) | 437.64(99) | 1335.32 | 14(2)       | 906.84(99) | 436(100) | 10.56 (1) | 1367.4 | 2.32 |
| 5                | 21(3)      | 1483.92(162) | 719.4(165) | 2223.32 | 28(4)       | 1493.08(163) | 723.76(166) | 10.56 (1) | 2255.4 | 1.39 |
| 10               | 56(8)      | 2549.32(322) | 1443.83(330) | 4444.32 | 63(9)       | 2558.68(323) | 1453.13(331) | 10.56 (1) | 4475.4 | 0.69 |

reset port, also sets the ND tied to signal ‘6’. The latter ND is clocked by \( CLK_1 \), and its’ output pulse is connected to the write port of FIFO, signaling it is ready to transfer data.

3) Note that until FIFO signals that it is ready to accept new data by sending out a ready pulse, the data in domain \( CLK_1 \) will remain stalled in the interface, even if FIFO tries to push more tokens into the pipeline. This is ensured by the reset operation of the ND by the signal ‘5’.

4) Once the ready pulse is produced, the last ND of in the top row of FSM will be set by signal ‘9’, while the ND below it will be reset by ‘8’. In the next cycle, the output pulse of the top ND will set the ND to its’ left by the signal ‘2’ and will permit any stalled \( CLK_1 \) token to enter FIFO.

5) This process continues until the ND receiving the first signal ‘c’ is set, which will eventually clock the read port of the FIFO. Concurrently, after the data enters FIFO, it will be transferred to the datapath stages of domain \( CLK_2 \).

The valid signal will drive the FIFO read port, repeating the above process.

### B. Timing Constraints

To ensure we can write data into the FIFO at least every other clock cycle, the clock period (both \( CLK_1 \) and \( CLK_2 \)) has to be larger than

\[
T_{cr} = T_n + 2T_s + T_d + T_{se}
\]

which is the critical path delay between the ND receiving the ready pulse and ND driving the write port (see Fig. 4), where \( T_n, T_s, T_d, \) and \( T_{se} \) denote the NDRO clock-to-Q delay, splitter delay, DFF clock-to-Q delay, and DFF setup time respectively. Hence, if \( F_{clk} \leq \frac{1}{T_{cr}} \), the FIFO operates correctly. The above expression evaluates to \( \sim 33 \) GHz in
SFQsee for 32-bit data. The clock frequency also needs to satisfy
\[ F_{clk} \leq \frac{1}{3T_s + T_d + T_{se}} \]  
(2)  
to ensure the data is transferred correctly to the read side with a valid pulse. The denominator in the right hand side of the above inequality is the critical path delay between the read port and the first DFF in the control path of the read side, which is \( \sim 40 \) GHz in SFQsee process. Note that both the above critical paths are independent of the datapath bit-width.

V. Simulation Setup & Results

To verify our proposed circuits, we designed our logic cell library in the MIT LL SFQsee process with Stewart McCumber parameter \( [1] \) equal to 2. The JJs used are superconductor-insulator-superconductor (SIS) Nb/AlOx-Al/Nb junctions, with critical current density of 100 \( \mu A/\mu m^2 \) and diameter of 700 nm. First, we evaluate our proposed synchronizer explained in Section III for a range of operating frequencies. We compute the BER of our synchronizer for data transfer between the two asynchronous clock domains as described in \( [15] \). The results, shown in Table II show that the proposed synchronizer leads to a BER of \( \sim 0.128 \times 10^{-15} \) in the write side at 30 GHz clock frequency, which may be sufficient for most applications. Note that the read side exhibits lower BER compared to the write side because it has a splitter between the two interfering DFFs. Moreover, the area overhead of our proposed design compared to the baseline is shown in Table III. Our proposed synchronizer incurs an average area overhead of 1.39\% compared to the previous design \( [15] \), for 5 stages.

In order to evaluate our proposal for bi-directional communication, we designed a 8-stage 32-bit wide circular shift register. We used two FIFOs to transfer the data from each set of four DFFs in the shift register as shown in Fig. 4. Our design not only provides extremely low BER mentioned above and satisfies the timing constraints described in Section IV.B.

VI. Conclusions

We present a FIFO synchronizer, compatible with the deep gate-level pipelining observed in SFQ, which can support bi-directional data transfer between two asynchronous clock domains. We further propose an associated robust interface which can handshake with our FIFO that supports high-frequency clocks. Our proposal demonstrates low BER and scales to large-scale SFQ designs with increased flexibility and negligible area overhead compared to previous designs.

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