A 54-GHz 23.3%-PAE CMOS Power Amplifier Using Dual-Gated Transistors

Lianming Li 1,2,a), Wenhao Zhong1, Xiaokang Niu1, Qin Chen1 and Xu Wu1, 2

Abstract A 54-GHz two-stage pseudo-differential common source power amplifier (PA) is implemented using dual-gated transistors (DGT). DGT structure is able to enhance both the linearity and back-off efficiency without consuming extra dc power. The nonlinear characteristics of the transistor can be compensated by adjusting the gate width and overdrive voltage of each transistor in the DGT. Besides, the dc power consumption of the DGT amplifier scales with the amplitude of the input signal, resulting in enhanced PAE at back-off. Fabricated in a 65-nm CMOS process, the measured small-signal gain of the 0.5×0.98 mm 2 PA is 17 dB at 52 GHz while consuming 24 mW from a 1-V supply. The maximum saturated output power is 10.5 dBm with a peak PAE of 23.3% measured at 54 GHz; the measured output power and PAE at 1-dB compression is 7.6 dBm and 17%, respectively.

Key words: power amplifier; back-off efficiency; dual-gated transistor

1. Introduction

With abundant spectrum advantage over sub-6GHz, mm-wave communication becomes a key enabler for 5G communication [1]. Recently, several licensed and unlicensed 5G mm-wave spectra (from 24 to 71GHz) have been selected by WRC-19, moving forward the 5G commercial deployment progress [2,3]. In particular, with IEEE 802.11ad and 802.11ay standards the unlicensed band around 60 GHz is attractive for high-speed WiFi and HD-video streaming. In China, to promote the mm-wave spectrum applications, 40-50 GHz band is also approved to be used for the mobile and fixed wireless access system. In this paper, by making use of the transistor with different threshold voltages, which is available in the commercial foundry process, dual-gated transistor techniques are adopted to improve the back-off efficiency [8]. However, these techniques require complex circuit structures and consume additional dc power. In [10], with a 55nm bulk CMOS, a 5.8GHz Doherty PA is realized with multi-gated transistor and second harmonic control techniques. Measurements show that the amplifier achieves 24.5% maximum PAE at 27.2 dBm saturated output power. In [11], to increase the amplifier linearity and efficiency, with advanced UTBB FD-SOI 28nm CMOS process, the segmented parallel transistors operate in different classes by tuning the transistor threshold voltage with its back gate terminal. Measurements show that the amplifier achieves 21% PAE at 1dB output compression power. In this paper, the design and implementation of a two-stage pseudo-
differential 54-GHz CMOS power amplifier are described in Section 3. Section 4 presents the measurement results, followed by the conclusion in Section 5.

2. Dual-gated Transistor Scheme

The structure of multi-gated transistors is shown in Figure 1(a) [12]. Gate width, overdrive voltage (i.e. $V_{GS}-V_{TH}$) of each transistor and the number of total transistors can all be adjusted. The overdrive voltage can be varied by changing gate-source voltage, $V_{GS}$. However, multiple transistors and separated gate and substrate metal lines will introduce extra devices and interconnect parasitic capacitances, which limit the output power and efficiency of the PA at mm-wave frequencies. Taking into the implementation complexity, the scheme proposed in this design is composed of two kinds of transistors and is called dual-gated transistors (DGT). All the four terminals of each transistor are connected together, as shown in Figure 1(b). Different overdrives are realized by using transistors with different $V_{TH}$ (i.e., low $V_{TH}$ and high $V_{TH}$). The gate width of each transistor is still able to be adjusted independently. Note that, from the circuit design perspective, the proposed dual-gated technique is more technology friendly, as typical commercial process supports transistors with different threshold voltages.

![Fig. 1. (a) Original multi-gated transistors, and (b) the proposed dual-gated transistors used in this design.](image)

2.1 Linearization of DGT

The drain current $i_{DS}$ of a common source MOSFET is expressed as

$$i_{DS} = I_{DC} + g_m v_{gs} + \frac{g_m'}{2} v_{gs}^2 + \frac{g_m''}{3} v_{gs}^3 + \cdots \quad (1)$$

where $g_m'$ and $g_m''$ are the first and the second derivatives of the MOSFET transconductance with respect to its gate-source voltage, respectively. Figure 2 shows the simulated $g_m''$ characteristics of low $V_{TH}$ and high $V_{TH}$ NMOS transistors. In this design, M1 is a low $V_{TH}$ (0.36V) transistor, while M2 is a high $V_{TH}$ (0.65V) transistor. As indicated in Figure 2 (curve “M1” and “M2”), the $g_m''$ of these transistors goes to the positive peak value at their sub-threshold regions, crosses zero near their threshold voltages, and shows negative peak value at the gate voltage which is slightly larger than their $V_{TH}$. To reduce dc power consumption without losing RF gain, the overdrive voltage of the NMOS transistor is usually set to about 0.25V. Unfortunately, for the low $V_{TH}$ and high $V_{TH}$ NMOS transistors, their $g_m''$ in this bias region has negative peak value, as shown in Figure 2. With the knowledge of trigonometry, we know that non-zero $g_m''$ will lead to PA’s gain nonlinearity and third order intermodulation (IMD3) distortion. Near-zero $g_m''$ is preferred to obtain high linearity.

![Fig. 2. The $g_m''$ of M1, M2 and DGT with respect to gate-source voltage](image)

The gate width and $V_{TH}$ of each transistor in DGT can be changed to obtain different kinds of curve shapes. In this design, the sizes of the low $V_{TH}$ and high $V_{TH}$ transistors are the same (48um/65nm). When their gate bias is set to around 0.6V, M1 works in class AB mode and is called the main transistor, while M2 works in class B mode and is called the auxiliary transistor. The negative $g_m''$ of the M1 is alleviated by the positive $g_m''$ of M2, as shown in Figure 2. In small-signal regime, the absolute value of $g_m''$ should be as small as possible, which can be easily understood according to (1). However, a relatively flat curve of $g_m''$ over a wide range is preferred in large-signal amplifiers, as shown in Figure 2 (curve “DGT”).

To illustrate the linearization effect of DGT, two groups of amplifiers are simulated. The conventional power amplifier employs only M1 and the overdrive voltage is about 0.25 V, which is a common situation in a typical mm-wave CMOS PA design. The other power amplifier adopts double gated transistors. The simulated dc power of DGT PA (16.2mW) is only 9.8% larger than Group1 (14.8mW), but the $P_{1db}$ (10.4dBm) is 4.2dB improved. Thus, we can conclude that the DGT method does have the ability to improve the power amplifiers’ linearity.

2.2 Back-Off Efficiency Enhancement of DGT

In large-signal regime, DGT is able to improve amplifiers’ back-off efficiency. The auxiliary transistor (M2) in DGT works in class B mode. When backing off from saturation, the dc power of M2 decreases accordingly, and thus the overall dc power will scale with the amplitude of input signal. Conventional mm-wave CMOS power amplifiers
work in class A or AB mode and their power consumption will not reduce obviously at back-off. In other words, power amplifiers using DGT structure can cut down extra power consumption and thus improve the efficiency at back-off. This mechanism is similar to reconfigurable sub-6GHz multi-mode power amplifiers where some PA-cells can be turned off with transformer and digital control switching PA techniques [13].

Note that DGT PAs have advantages over multi-mode PAs. The input and output impedances of DGT only vary slightly when the amplitude of the input signal changes. However, abrupt impedance variation may occur when multi-mode PAs’ operation mode alters. Besides, when operating in the low-power mode, gain compression may still exist if the remaining PA cells work near saturation and some output power may leakage to the “off” PA-cells because of their parasitic capacitances. Both issues are well avoided in DGT structures.

The simulated back-off efficiency of the same two groups of PAs as in sub-Section 2.1 is shown in Figure 3. The decline of curve “DGT” is slower and the corresponding PAE is higher at back-off. Besides, thanks to the effect of linearity improvement, the PAE of DGT is much larger than the conventional PA, which further proves that DGT does have the capability to improve back-off efficiency.

3. Circuit Design

A two-stage PA based on DGT techniques is shown in Figure 4. To simplify the schematic, DGT structures are represented by transistor symbols and labeled by DGT1, DGT2, DGT3 and DGT4, respectively. Both stages are realized using the neutralized common-source amplifier. With differential amplifier topology, the neutralization mitigates the intrinsic gate-drain capacitive feedback of each transistor and increases the power gain and reverse isolation with no penalty in power consumption [8]. Unconditional stability is obtained due to the nearly unilateral behavior of each stage, which simplifies the impedance matching. To reduce the chip area, transformers are intensively used in matching networks. Transformers can perform both differential to single ended conversion and impedance matching. Besides, in a multi-stage amplifier design, the center-taps of transformers can be used for dc biasing.

Figure 5 shows the stability factor $K_f$ and maximum power gain $G_{MAX}/MSG$ with respect to the neutralization capacitance value. The neutralization technique potentially degrades the common-mode stability as the feedback capacitance is increased from $2C_{GD}$ to $2(C_{GD}+C_C)$ for the common-mode signal [14]. To alleviate this effect, a transformer is used in all the three matching networks. As shown in Figure 6, the center tap of the primary or secondary winding of the transformer is either floating or connected to a high impedance. Thus, the common-mode current will be cancelled inside the transformer and the common-mode stability is then enhanced.

Apart from transformer, as shown in Figure 6, in this design by tuning the metal width and spacing, the optimal characteristic impedance of the differential transmission line is achieved, thereby realizing impedance matching between the transistor and transformer with optimized transmission line length and reducing the insertion loss. Transmission line can extend the distance between different components.
and thus alleviate the coupling between them. Besides, this transformer topology with transmission line will lead to wide band matching.

Fig. 6. Transformer topology with transmission line.

4. Measurement Results

The prototype two-stage pseudo-differential PA is fabricated in a 65-nm bulk CMOS process and the chip microphotograph is shown in Figure 7. All the transformers and transmission lines are realized with top metal to reduce the insertion loss. Inter-digitated MOM capacitors are employed to realize the neutralizing capacitors in each amplifier stage. Including pads, the prototype occupies a total chip area of $0.5 \times 0.98$ mm$^2$.

Fig. 7. Die photo of the two-stage power amplifier.

The PA consumes 24 mW from a 1-V supply. Figure 8 shows the measured S-parameters. An $S_{21}$ of 17.2 dB is achieved at 52 GHz. The -3-dB bandwidth is 4.8 GHz, from 51 to 55.8 GHz. The reverse isolation, $S_{12}$, of the PA is smaller than -25 dB from 40 to 67 GHz. The results prove the merits of applying neutralization to achieve stability, high gain and reverse isolation for mm-Wave operation.

Figure 9 shows the large-signal behavior of the PA with increased input power at 54 GHz. As indicated, a $P_{SAT}$ of 10.5 dBm is achieved, and the peak $PAE$ is 23%. The output power at 1-dB compression, $P_{1dB}$, is about 7.6dBm, and the corresponding $PAE_{1dB}$ is about 17%. Figure 10 gives the measured performance of the PA from 51 to 56 GHz in steps of 1 GHz. Across the 5-GHz range, the $PAE_{MAX}$ is more than 18%, while the corresponding output power is about 10 dBm.

From 53–56 GHz, the $P_{1dB}$ exceeds 6dBm with higher than 13% back-off $PAE$.

Fig. 8. S-parameters measurement results.

Fig. 9. Measured Gain, $P_{OUT}$, $PAE$ at 54GHz

Fig. 10. Measured $PAE_{MAX}$, $PAE_{1dB}$, $P_{SAT}$, $P_{1dB}$ across frequency

Table 1 compares the PA prototype to the state-of-the-art mm-wave PAs in 28 nm, 40nm, 55 nm, 65 nm and 90nm CMOS. Thanks to the DGT scheme, compared with the PA in 28-nm and 40nm CMOS, the proposed PA achieves very good gain and efficiency performance. Compared with other 65 nm CMOS PA, the proposed PA achieves the highest $PAE_{MAX}$ and $PAE_{1dB}$ at V-band. Besides, the PA realizes similar $P_{SAT}$ and larger $P_{1dB}$ while consuming almost half the dc power compared to [16], which shows the feasibility of linearity enhancement using dual-gated transistor topology.
Table 1. V-band CMOS PAs performance comparison

| Technology | Frequency [GHz] | Gain[dB] | DC power [mW] | PDC 1dB [dBm] | PDC 10dB [dBm] | PAE 1dB [%] | PAE 10dB [%] |
|------------|-----------------|----------|---------------|---------------|----------------|-------------|---------------|
| [11] 2G     | 60              | 13.4     | 108           | 16.9          | 16.2           | 21           | 23            |
| [12] 65     | 60              | 20.3     | 200           | 18.6          | 18.2           | 21.5         | 21.8          |
| [13] 65     | 60              | 30       | 65            | 10.6          | 9.6            | 18           | 17            |
| [14] 65     | 60              | 15.5     | 732           | 18.4          | 11.5           | 3.6          | 2             |
| [15] 65     | 60              | 19.2     | 460           | 17.3          | 15.1           | 11.1         | 8.5           |
| [16] 65     | 60              | 13.8     | 41.5          | 11.3          | 11.2           | 14.1         | 9.8           |
| [17] 65     | 60              | 17.3     | 362.6         | 16.8          | 15.3           | 14.5         | 10            |
| [18] 65     | 60              | 31       | 96            | 18            | 12.3           | 22.7         | 13.6          |
| [19] 65     | 60              | 10.6     | 143           | 14.8          | 11.8           | 7.3          | 4             |
| [20] 65     | 60              | 22.4     | 90            | 16.4          | 13.9           | 23           | 18.9          |
| [21] 65     | 60              | 9.5      | 800           | 22.8          | 19.5           | 15.9         | 9             |
| [22] 65     | 60              | 29.7     | 816           | 23.7          | 19.9           | 22.1         | 11.1          |
| [23] 65     | 60              | 20.4     | 126           | 24.3          | 19.4           | 21.1         | 12.2          |
| [24] 65     | 60              | 21.1     | 200           | 13.9          | 19.7           | 11.4         | 8             |
| [25] 65     | 50              | 13       | 106.8         | 13.3          | 12             | 16           | 13.9          |
| [26] 90     | 53              | 17.78    | 120           | 13.7          | 13.36          | 16.9         | 16.7          |
| [27] 65     | 62              | 13       | 11            | 10.1          | 10.1           | 33           | 31            |

5. Conclusions

A 54-GHz two-stage pseudo-differential common source CMOS power amplifier (PA) is implemented using dual-gated transistors (DGT). Simulation and measurement show that DGT structure is able to enhance both the linearity and back-off efficiency without consuming extra dc power. Neutralizing capacitors are cross-coupled in both common-source amplifiers to increase the power gain and reverse isolation. Transformers are implemented in matching networks for compact design. Fabricated in a 65nm CMOS process, the measured small-signal gain of the 0.5×0.98 mm² PA is 17 dB at 52 GHz while consuming 24 mW from a 1-V supply. The maximum saturated output power is 10.5 dBm with a peak PAE of 23.3% measured at 54 GHz. The output power at 1-dB compression is about 7.6 dBm and the corresponding PAE 1dB is about 17%.

Acknowledgments

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