Hardware-Conscious Optimization of the Quantum Toffoli Gate

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While quantum computing holds great potential in combinatorial optimization, electronic structure calculation, and number theory, the current era of quantum computing is limited by noisy hardware. Many quantum compilation approaches can mitigate the effects of imperfect hardware by optimizing quantum circuits for objectives such as critical path length. Few approaches consider quantum circuits in terms of the set of vendor-calibrated operations (i.e., native gates) available on target hardware. This manuscript expands the analytical and numerical approaches for optimizing quantum circuits at this abstraction level. We present a procedure for combining the strengths of analytical native gate-level optimization with numerical optimization. Although we focus on optimizing Toffoli gates on the IBMQ native gate set, the methods presented are generalizable to any gate and superconducting qubit architecture. Our optimized Toffoli gate implementation demonstrates an 18% reduction in infidelity compared with the canonical implementation as benchmarked on IBM Jakarta with quantum process tomography. Assuming the inclusion of multi-qubit cross-resonance (MCR) gates in the IBMQ native gate set, we produce Toffoli implementations with only six multi-qubit gates, a 25% reduction from the canonical eight multi-qubit implementations for linearly connected qubits.

CCS Concepts: • Hardware → Quantum computation; • Computer systems organization → Quantum computing;

Additional Key Words and Phrases: Toffoli gate, least-squares optimization, native gates, quantum compilation
1 INTRODUCTION

Over the past decade, quantum hardware has improved enough to physically realize quantum computers with tens of noisy qubits [3, 26, 39, 60]. Coupled with the creation of quantum software development kits such as IBM’s Qiskit [2] and Google’s Cirq [9], the current era of quantum computing has seen unprecedented researcher access to state-of-the-art quantum computers. With this broader access has come an accelerated demand for mitigating physical limitations that confine modern quantum circuit lengths to depths well under 100 multi-qubit gates. While several physics-based techniques for noise mitigation exist, such as dynamical decoupling [13, 59] and echoed gates [42, 46], much success has been found in developing quantum compilation strategies that yield circuits with smaller depths and fewer necessary operations.

A plethora of modern approaches to quantum compilation aim to decrease compiled circuit length and increase algorithm fidelity. While many of these approaches leverage classical compilation techniques such as temporal planners [57], list schedulers [27], and DAG circuit representations [30], physical limitations inherent in quantum computation have necessitated the fusion of these techniques with novel hardware-conscious methods that transcend traditional compiler theory. A particularly profitable class of these methods has tackled the problem of efficiently mapping quantum circuits to underlying qubit connectivity [14, 16, 30, 38, 49, 50, 52]. Another class of methods provides quantum compilers with accurate noise models of their target hardware in order to improve program success [34, 51].

The success of the preceding methods lends much support to taking a hardware-conscious approach to quantum algorithm optimization. Nevertheless, few current approaches consider optimization at the native gate level, a level of abstraction below that of standard quantum algorithm specification in which programs are described in terms of the quantum computer’s native gate set, namely, the set of operations explicitly calibrated by the hardware vendor. Previous work has explored the optimization of gates such as the SWAP gate [21] and ZZ interaction [19] at the native gate level, and only recently have researchers turned their attention to optimizing slightly longer operations such as the Toffoli gate at this level of abstraction [41].

The Toffoli gate is a fundamental three-qubit, multi-control operation that enacts a Pauli-X gate (the quantum equivalent of a classical NOT operation) on its target qubit provided that its two control qubits are in the $|1\rangle$ state [43, 55]. The Toffoli gate is used in many important quantum computing applications, including Shor’s algorithm [44], Grover’s algorithm [15, 22], Takahashi adders [48], and quantum error correction [11, 40]. Many of these applications enable some of the most exciting possibilities offered by quantum computing, underscoring the importance of the Toffoli gate.

Optimizing the Toffoli gate is crucial to improving quantum circuit compilation. For example, it has been shown that delayed hardware-aware decomposition of the Toffoli gate to the native gate set of target hardware substantially improves compilation results [14]. Furthermore, Amdahl’s law [24] suggests that small optimizations of the Toffoli gate can yield exponential fidelity improvements (and hence error reductions) for the many quantum algorithms that leverage it, making its native gate-level optimization worthwhile to explore.

In this article, we optimize the Toffoli gate for the IBMQ native gate set via a combination of existing and novel native gate-level optimization techniques. It is important to note that although...
we focus on the Toffoli gate, the methods developed in this article are readily generalizable to other quantum gates and circuits. The major contributions of this article are listed below:

- A novel native gate-level optimization technique termed “side-effect sandwiching” that significantly reduces quantum circuit critical path length;
- An optimized Toffoli gate for IBMQ machines with 18% lower infidelity than the current standard as benchmarked on IBMQ Jakarta;
- A method of parameterizing the set of all \( m \)-qubit quantum circuits with \( n \) multi-qubit operations with \( 3m(n + 1) \) real numbers;
- Numerical quantum circuit optimization methodology complementary to existing analytical native gate-level techniques.

This article is organized as follows: Section 2 contains background information on quantum computing and a review of existing native gate-level optimization techniques (also referred to as “a priori techniques”). Section 3 introduces side-effect sandwiching, which is a novel technique, and demonstrates that native gate-level optimization can be used to produce an optimal Toffoli gate for the IBMQ native gate set as characterized by quantum process tomography. Section 4 develops a methodology for the numerical discovery of novel quantum circuit implementations of a provided unitary matrix as well as how numerical techniques can aid analytical a priori techniques. Section 5 demonstrates the optimality of the Toffoli gate circuit presented in Section 3 by applying it to quantum compilation. Finally, we conclude and identify future research directions in Section 6.

2 BACKGROUND

In this section, we briefly introduce quantum circuits, quantum computer native gate sets, the multi-target cross-resonance gate, current Toffoli gate implementations for superconducting qubits, and some native gate-level optimization techniques. An exploration of the limitations of existing hardware and qubit connectivity is also provided. Moreover, notation specific to this article is introduced.

2.1 Qubits and Quantum Circuits

The most fundamental unit of quantum information is the qubit. The qubit is represented mathematically as a linear combination \( |\psi\rangle = \alpha|0\rangle + \beta|1\rangle \) of basis vectors \( |0\rangle \) and \( |1\rangle \), where \( \alpha, \beta \in \mathbb{C} \) and \( |\alpha|^2 + |\beta|^2 = 1 \). Note that this expression indicates that a qubit is not limited to existing in either the \( |0\rangle \) or \( |1\rangle \) state. Instead, it may also occupy a superposition of these two states. A single qubit state \( |\psi\rangle \) can be represented graphically as a point on the surface of a Bloch sphere.

Two qubits are said to be entangled if the state of the two-qubit system cannot be described as the tensor product of individual qubit states. Entangled states, while much more difficult to visualize and work with, are useful for a variety of applications including super-dense coding and state teleportation. This phenomenon, along with superposition, enables quantum computers to solve certain problems asymptotically faster than classical computers can.

In order to perform a certain computation on qubits, a series of quantum operations or gates performing this computation must be specified. Quantum circuits mirror classical digital logic circuits in that they are specified as a sequence of quantum gates to execute on some subset of available qubits. Quantum gates are represented algebraically by unitary matrices that describe how they map input quantum states to output quantum states and theoretically operate on any number of qubits. A quantum algorithm can be specified as a quantum circuit along with a procedure for interpreting the final quantum state resulting from the computation.

The lowest level of abstraction for specifying quantum circuits on superconducting qubits is the pulse schedule. Superconducting qubits are controlled with microwave pulses created by arbitrary
waveform generators. Each native gate in the native gate set of a quantum computer has an associated pulse schedule specifying the amplitude of the microwave pulse on a given qubit at any moment in time. In practice, the time axis is discretized. Pulse-level access to quantum computers gives the user more control over how operations are executed. In this article, we use pulse-level control in order to engineer new native gates and realize our native gate-level optimizations on modern quantum hardware.

2.2 Quantum Hardware Limitations

Similar to classical computers, quantum computers are limited by the way their computing model is physically implemented. Different quantum machines have different vendor-calibrated operations (i.e., native gates) available, which presents a challenge to developing quantum compilers. These constraints can sometimes be relaxed by pulse-engineering custom operations, effectively augmenting the native gate set of target hardware. This limitation is covered in Section 2.2.1. Different quantum computers also have different levels of qubit connectivity, which has a significant impact on the implementation of quantum circuits on quantum hardware; the majority of the length of NISQ-era circuits involve swapping information between qubits to satisfy hardware connectivity constraints. This constraint is covered in Section 2.2.2.

2.2.1 Native Gate Sets. Quantum algorithm design often proceeds in a relatively hardware-agnostic fashion, with quantum circuits built from a set of abstract, mathematically convenient gates that must be later transpiled to available vendor-calibrated operations and mapped onto the underlying qubit architecture of the device [10]. Consideration of the natural limitations of the underlying hardware during algorithm design yields several opportunities for optimization. The native gate set of a quantum computer is defined as the set of operations specifically calibrated by the hardware vendor to perform a targeted unitary operation. This set of operations is analogous to the instruction set in classical computing. Recent results in the quantum compiler community have indicated great opportunities in the optimization of quantum circuits at the native gate set-level [19]. In the case of IBMQ hardware, the native gate set consists of $\sqrt{X}$, $X$, the cross-resonance operator, and $R_z(\theta)$ for arbitrary $\theta$. The single-qubit gates $\sqrt{X}$ and $X$ enact $90^\circ$ and $180^\circ$ rotations of a qubit state about the $x$-axis of the Bloch sphere, while the $R_z(\theta)$ gate enacts a $\theta$ angle rotation of a qubit state about the $z$-axis of the Bloch sphere. The cross-resonance operator enables interaction between pairs of qubits and effectively performs a controlled-$R_x$ gate. When the rotation angle is calibrated to $\pi$, the cross-resonance effectively executes a CNOT gate (up to single-qubit gates). The cross-resonance operator is generally implemented as two half-cross-resonance pulses of opposite polarity so as to mitigate error. The details of this procedure are below the native gate set abstraction level; only the notion that there are two polarities for half-cross-resonance pulses is necessary for our discussion of native gate-level optimization.

Prior research indicates that augmenting native gate sets with pulse-level hardware control (such as OpenPulse for IBMQ hardware) leads to fidelity improvements in quantum gate implementations [21], including the Toffoli gate [41]. In this article, we consider augmenting the IBMQ native gate set to include the multi-target cross-resonance gate, which executes the equivalent of a cross-resonance gate between a target qubit and every target qubit. The single-target cross-resonance gate is normally implemented by driving its control qubit at the resonant frequency of its target qubit with an arbitrary waveform generator. The multi-target cross-resonance gate is implemented the same way, except that its control qubit is driven with the superposition of microwave pulses with resonant frequencies of each of its target qubits. The multi-target cross-resonance gate was chosen for two reasons. First, its operation is easily understood in terms of a familiar gate (i.e., the single-qubit cross-resonance gate), which makes analytical optimizations
Fig. 1. The connectivity graph of the IBMQ Yorktown qubit architecture (left) features two fully connected three-qubit subgraphs, while the IBMQ Jakarta qubit architecture (right) features only linearly connected three-qubit subgraphs.

more tractable. Second, it has already been demonstrated to asymptotically improve the length of several high-impact quantum algorithms [20].

2.2.2 Qubit Routing. When optimizing quantum algorithms for a target machine, the underlying qubit connectivity must be considered. Cross-resonance gates can be executed only on certain pairs of qubits in most superconducting qubit architectures. If a cross-resonance gate can be executed between two qubits, they are said to be “connected,” and a graph with qubits as nodes can be constructed that shows the qubit connectivity of a quantum computer. In this article, since we are optimizing a three-qubit gate, we focus on the connectivity of subgraphs of three nodes. We define a three-qubit subgraph as fully connected if every qubit in the subgraph is connected to every other qubit in the subgraph. We define a three-qubit subgraph as being linearly connected if the subgraph is connected and contains one qubit with degree two and two qubits with degree one. Figure 1 shows qubit connectivity graphs of two IBMQ systems; note that the left graph contains two fully connected three-qubit subgraphs, while the right graph contains only linearly connected three-qubit subgraphs.

Compiling quantum circuits to respect the underlying qubit connectivity of a target system is called the qubit routing problem, and it represents an important challenge in quantum compilation. The current method of solving the qubit routing problem is inserting SWAP operations that switch the quantum states represented by two connected qubits. If a cross-resonance gate is to be performed between two unconnected qubits, the states on these qubits can be swapped to adjacent qubits that can execute the operation. The importance of qubit routing is demonstrated by the effort that has been devoted to reducing the number of required SWAP operations to run algorithms on sparsely connected systems by the quantum compilation community. On most superconducting qubit systems (especially systems with over ten qubits), SWAP operations account for most of the compiled circuit and indicate the limitations of the underlying qubit connectivity.

Different connectivities have different strengths. On superconducting qubit architectures, operations run on fully connected qubit subgraphs require fewer SWAP operations in their implementations but are also more prone to crosstalk error. Linearly connected qubit subgraphs, on the other hand, require more SWAP operations but are also less prone to crosstalk error; in fact, quantum computer providers such as IBMQ are increasingly using less-connected architectures to improve qubit fidelity [35]. Therefore, in this article, we focus on developing optimizations for linearly connected qubits.

2.3 Notation

In this section, we introduce some notation. To denote the unitary of the Toffoli gate, we use the symbol $U_{CCX}$. To denote a 90° rotation around the x–axis of the Bloch sphere, we write $\sqrt{X}$. To denote a negative 90° rotation around the x-axis of the Bloch sphere, we write $R_z(180°)\sqrt{X}R_z(180°)$. 

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$R_z$ rotations are not physically executed and can be kept track of in software. Therefore, they are unimportant when measuring circuit parameters such as circuit length and total degrees of rotation. To emphasize this point, we denote $z$-axis rotations of various common angles with small arrows as shown in Table 1.

### 2.4 Existing Toffoli Gate Implementations

There are several existing implementations of the Toffoli gate for superconducting architectures. One of these is shown in Figure 2. We refer to this implementation [36] as the “canonical linear Toffoli gate” because it is among the oldest and most commonly used quantum circuits for implementing the Toffoli gate on linearly connected qubits. Previous work has explored optimizing the Toffoli gate at the pulse level [41], but the produced optimization introduces a side-effect SWAP gate on the control qubits, which may not always be desired.

### 2.5 Native Gate-Level Optimization

Although consideration of quantum circuits at the native gate level is a generally novel approach, a number of optimization techniques at this abstraction level have been explored in prior literature. We use the Superstaq platform [47] to apply three existing native gate-level optimization techniques to the Toffoli gate, initially developed to optimize the quantum SWAP gate [21]. Native gate-level optimization starts with a standard gate-level specification of a quantum circuit. The quantum circuit to be optimized is then translated into the native gate set of the target quantum hardware. Next, the following three techniques can be used to reduce circuit depth and active rotation.

#### 2.5.1 Cross-Gate Pulse Cancellation

Cross-gate pulse cancellation is a technique in which a sequence of native gates is compressed into a shorter sequence of native gates (including possibly the NO-OP identity); For example, if during optimization the native gate sequence $\sqrt{X}X\sqrt{X}$ is encountered (the $\sqrt{X}$ may itself be part of a preceding sequence of gates), it can be eliminated because it is equivalent to a $360^\circ$ (and $0^\circ$) rotation around the $x$-axis of the Bloch sphere. In this case, cross-gate pulse cancellation would save $360^\circ$ of active rotation and potentially result in circuit length reduction if one or more of the native gates were part of the critical path length of the quantum circuit.

#### 2.5.2 Cross-Resonance Commutation

Gates enacting rotations around the $x$-axis of the Bloch sphere commute. This fact becomes particularly relevant when considering the controlled $x$-rotation model of the cross-resonance operator. Figure 3 shows a conceptual model of the

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Table 1. Circuit Symbols (Bottom) for Representing the $R_z$ Rotation of Various Angles in Radians (Top)

| $\frac{\pi}{4}$ | $-\frac{\pi}{4}$ | $\frac{\pi}{2}$ | $-\frac{\pi}{2}$ | $\frac{3\pi}{4}$ | $-\frac{3\pi}{4}$ | $\pi$ | $-\pi$ |
|------------------|------------------|------------------|------------------|------------------|------------------|------|-------|
| $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ | $\uparrow\downarrow$ |

Fig. 2. Canonical implementation of a Toffoli gate designed for linear qubit architectures.
positive polarity cross-resonance operator. Note that half-CR pulses can be modeled as controlled \(X\) gates. This permits the movement of gates enacting \(x\)-axis Bloch sphere rotations on the target qubit through the cross-resonance operator. This often results in opportunities for active rotation and circuit length reduction via cross-gate pulse cancellation.

2.5.3 **Cross-Resonance Polarity Swap.** The cross-resonance operator has an associated polarity. Positive polarity cross-resonance operators are composed first of a positive half-CR pulse followed by an \(X\) gate on the control qubit and then a negative half-CR pulse. Negative polarity cross-resonance operators are the same except they first execute a negative half-CR pulse followed by an \(X\) gate and then a positive half-CR pulse. Implementing a negative polarity cross-resonance operator, however, introduces a side effect on the control qubit that must be counteracted with an \(X\) gate preceding the operation. This extra \(X\) gate can eliminate other gates or gate sequences via cross-gate pulse cancellation.

2.5.4 **Euler Decomposition.** Another technique that yielded considerable savings in angle rotation is decomposing the unitary of long single-qubit gate sequences into shorter, equivalent sequences. For example, CR gate commutation and cross-gate pulse cancellation often yield gate sequences featuring an \(R_z\) gate sandwiched between two \(R_x\) gates. Some of these gate sequences occur multiple times; in many cases, one can find an equivalent gate sequence with fewer \(\sqrt{X}\) and \(X\) gates and more degrees of \(R_z\) rotation. \(R_z\) gates do not represent physical rotations performed on IBMQ systems but are viewed instead as a change in the Pauli reference frame \[32\]. Therefore, \(R_z\) gates are better thought of as bookkeeping operations rather than physical processes. Therefore, this method effectively replaces physical quantum computer operations with “virtual” operations that do not need to be physically implemented. By reducing the number of physical operations required to perform a quantum circuit, fewer places exist for introducing errors.

3 **ANALYTICAL A PRIORI APPROACH**

In this section, we apply several native gate-level optimization techniques to the Toffoli gate implementation in Figure 2. We also present cross-resonance gate sandwiching, a novel technique that can significantly reduce the length of quantum circuits. All of these methods are termed “a priori” because they operate on an already existing quantum circuit.

3.1 **Cross-Resonance Sandwiching**

In addition to leveraging the prior native gate-level work covered in Section 2.5.1, we introduce cross-resonance gate sandwiching, a novel technique that yielded considerable savings in Toffoli gate implementation length. The cross-resonance operator is generally implemented in an echoed fashion that leaves room for a single-qubit gate to be applied to the target qubit at the same time as an \(X\) gate is applied to the control qubit. This observation is useful because CR gate commutation allows for \(\sqrt{X}\) and \(R_z(180^\circ)\sqrt{X}R_z(180^\circ)\) gates to be moved inside cross-resonance operators. In the context of computer architecture, this technique can be thought of as pipelining single-qubit operations. Although single-qubit operations are generally much faster than multi-qubit operations, repeated sandwiching of bottleneck single-qubit operations into multi-qubit operations adds up to significant time savings in certain cases. Examples and notations regarding this technique are
Fig. 4. (left) Definitions of sandwiched cross-resonance operations. The sign indicates the polarity of the cross-resonance operations, and the direction of the arrow represents whether a 90° or −90° side-effect rotation should be applied to the target qubit. (right) Pulse schedule of a sandwiched positive polarity cross-resonance gate enacting a $\sqrt{X}$ side-effect on its target qubit.

shown in Figure 4 (left). Figure 4 (right) shows the pulse schedule implementation of the cross-resonance operation with positive polarity and a $\sqrt{X}$ side-effect. This optimization is enabled only by pulse-level control of the hardware.

3.2 Results

The application of native gate-level optimization resulted in the Toffoli gate implementation in Figure 5. Please refer to Figure 4 (left) to interpret the quantum circuit diagram. Table 2 compares the canonical and optimized Toffoli gate implementations using three fidelity proxies. Fidelity proxies are circuit properties that are correlated with average circuit fidelity. Generally, the fidelity of a quantum circuit improves as the circuit length, total rotation, and the number of native gates decrease. Circuit length is the time taken to execute the critical path of a quantum circuit; total rotation is the total degrees of x-rotations required to implement all single-qubit gates in a quantum circuit. Prior work suggests that circuit length is most correlated with average circuit fidelity in the NISQ era [8]. We note that $R_z$ rotations are not counted in the number of native gates because they are not physically executed operations.

3.3 Benchmarking

To demonstrate the efficacy of the optimized Toffoli gate implementation in Figure 5, we benchmarked it on qubits 0, 1, and 3 of the IBMQ Jakarta quantum computer, using SuperstaQ [47] to produce the optimized Toffoli gate. While truth tables can verify the correctness of classical logic gates, benchmarking the performance of quantum gates presents novel challenges. Examining the truth table of a quantum gate over the computational basis states, for example, does not encapsulate its performance on states that are superpositions of these states. Superposition states represent a much larger portion of the Hilbert space on which a quantum gate operates, making it important to include them in any complete characterization of a quantum gate. One prominent benchmarking method used to characterize the accuracy of a quantum gate is quantum process tomography.

In quantum process tomography, many representative states are prepared and measured to reconstruct the true operation being performed. In Qiskit, each qubit of the operation to be benchmarked is prepared in one of the four Pauli-basis eigenstates and then measured in the X,
Table 2. Optimization Proxy Improvements of the Optimized Toffoli Gate for Linearly Connected Qubit Architectures

| Proxy                | Canonical | Optimized | Change  |
|----------------------|-----------|-----------|---------|
| Length (ns)          | 2694.1    | 2303.0    | −14.5%  |
| Total rotation (°)   | 3960°     | 2250°     | −43.2%  |
| Native gates         | 28        | 17        | −39.3%  |

Fig. 5. Final optimized Toffoli gate for linearly connected qubit architectures.

In order to establish the statistical significance of our optimizations, error bounds on average fidelities were also computed. The error bounds in the gate fidelities are obtained by a Monte Carlo method [7, 25, 37] assuming that the measured probabilities follow multinomial distributions. We randomly sample the single-shot probabilities 1,000 times to obtain the gate fidelity distribution. The error bounds are defined as 1.96 times of standard deviation or the 95% confidence level of a least-squares fit.

Figure 6 compares the average fidelity of our optimized Toffoli gate implementation with the average fidelities of the canonical linear Toffoli gate implementation (shown in Figure 2) and IBM Qiskit-optimized linear Toffoli gate implementation (compiled with optimization level 3 and transpilation seed 12345). We measured our optimized Toffoli gate, the canonical Toffoli gate, and the IBM Qiskit-compiled Toffoli gate average gate fidelities to be $0.864 \pm 0.00166$, $0.834 \pm 0.00153$, and $0.828 \pm 0.00166$, respectively. Therefore, our optimization results in an 18% reduction in infidelity compared with the canonical Toffoli gate.

4 NUMERICAL DISCOVERY APPROACH

The methods presented in Section 3 focused on the refinement of an already existing quantum circuit. In this section, we will focus on the discovery of novel quantum circuit structures for implementing a target unitary matrix using numerical optimization techniques. After an exploration of our mathematical methodology and its results for the Toffoli gate, we will discuss how the numerical quantum circuit discovery approach can be integrated with the a priori analytical methods presented in the preceding section.

4.1 Methods

We now turn our attention to developing numerical methods for quantum circuit discovery. First, we will present a technique for parameterizing the set of all quantum circuits containing $n$
multi-qubit gates. Then, we will present an objective function leveraging this parameterization which, when minimized, produces a quantum circuit implementing a specified unitary. Finally, we will describe how to use this objective function to computationally find quantum circuit implementations of unitary matrices in a parallel, massively scalable fashion. Although prior work has explored numerical optimization for quantum circuit synthesis [45], the novelty of this work lies in the objective function used. The objective function presented in this work allows for the combination of numerical circuit synthesis with a priori analytical methods.

4.1.1 Parameterizing Quantum Circuits. We first turn our attention to establishing a method of parameterizing the set of all quantum circuits. Note that any sequence of single-qubit operations can be expressed as the product of several unitary matrices, which itself is a unitary matrix. Any single-qubit operation can be expressed via a generic single-qubit rotation gate, denoted by $U$. The unitary matrix of the $U$ gate can be completely specified with three real numbers $\theta$, $\phi$, and $\lambda$ [36]. The $U$ gate is realized at the native gate level with the sequence $R_z(\phi)R_z(180^\circ)\sqrt{X}R_z(180^\circ)R_z(\theta)\sqrt{X}R_z(\lambda)$ on IBMQ hardware.

It follows that sequences of arbitrary single-qubit gates occurring between multi-qubit gates can be replaced by one layer of $U$ gates. Rearranging the quantum circuit in this manner results in $n+1$ layers of single-qubit gates interleaved with $n$ multi-qubit operations. Now, group every multi-qubit operation with the corresponding preceding layer of $U$ gates, and call this a block. Therefore, any circuit containing $n$ multi-qubit gates can be expressed by using $n$ blocks followed by a layer of $U$ gates. We use $B_0$ to denote the unitary matrix representing the first layer of $U$ gates. The blocks that can be used as building blocks are determined by the native gate set over which one optimizes. The unitary describing the action of the entire circuit equals $B_nB_{n-1}\ldots B_0$ (note that multiplied unitary matrices are applied to a quantum state from right to left).

Optimizing with linear qubit connectivity poses constraints on which block unitaries are allowed, reducing the optimization space. Note that multi-target cross-resonance (MCR) gates must all have the same control bit, for example, because allowing MCR gates with different control bits would require a fully connected qubit architecture. Let us label a set of three linearly connected qubits $q_0$, $q_1$, and $q_2$. We arbitrarily choose qubit $q_0$ to be the MCR control bit without loss of generality. This reduces our gate set to single-qubit gates, the MCR gate with $q_0$ as the control qubit, the CR gate between $q_0$ and $q_1$, and the CR gate between $q_0$ and $q_2$, because a CR gate between any other qubit pairs would violate the imposed connectivity constraint. Figure 7 illustrates the three blocks that can construct all possible quantum circuits containing $n$ multi-qubit operations over this gate set. This rigorous, parameterized approach to describing quantum circuits allows us to formulate our principal goal in the language of numerical optimization.
4.1.2 Objective Formulation. We can frame the problem of Toffoli optimization over a linear qubit architecture in the language of unconstrained nonlinear optimization. Consider an arbitrary \( n \)-layer quantum circuit parameterized via the method presented in Section 4.1.1. Let the \( U \) gate parameters in this circuit be organized into a vector in \( \mathbb{R}^{3n+3} \) as shown in Equation (2):

\[
\vec{\beta} = \begin{bmatrix} \theta_1 & \phi_1 & \lambda_1 & \cdots & \theta_{3n+3} & \phi_{3n+3} & \lambda_{3n+3} \end{bmatrix}^T
\]  

(2)

Let \( U(\vec{\beta}) = B_n B_{n-1} B_0 \) represent the final unitary matrix obtained from multiplying parameterized block unitary matrices as a function of \( \vec{\beta} \). We wish to solve the nonlinear least-squares problem detailed in Equation (3):

\[
\vec{\beta}^* = \arg\min_{\vec{\beta}} \| U_{CCX} - U(\vec{\beta}) \|_F^2
\]  

(3)

Note that the quantity minimized in Equation (3), by definition of the Frobenius norm, is the sum of squared residuals and is a measure of how close \( U(\vec{\beta}) \) is to implementing the Toffoli gate. While this objective alone is sufficient for Toffoli circuit discovery, it has limited applicability in that the parameter values produced by optimizing it can take on any real angle value. This makes it nearly impossible to apply analytical \( a \ priori \) methods (such as cross-gate pulse cancellation and active rotation virtualization) to numerically discovered Toffoli circuits. In order to make these techniques complementary, a more complex objective function penalizing certain parameter values and favoring others is required. Equation (4) presents a function that favors small parameter angle values that are multiples of \( \frac{\pi}{6} \), \( \frac{\pi}{4} \), and \( \frac{\pi}{3} \). Figure 8 graphically depicts \( f_1(\vec{\beta}) \) with parameters \( \alpha = 1 \) and \( \gamma = 0.001 \).

\[
f(\vec{\beta}) = \gamma \| \vec{\beta} \|_2^2 + \alpha \sum_{i=1}^{9n+9} \sin^2(6\vec{\beta}_i) \sin^2(4\vec{\beta}_i) \sin^4(2\vec{\beta}_i)
\]  

(4)

Combining Equation (3) and Equation (4) results in the objective function in Equation (5). Tuning parameters \( \alpha \) and \( \gamma \) scale the importance of small, ideal angles relative to accuracy.

\[
\vec{\beta}^* = \arg\min_{\vec{\beta}} \| U_{CCX} - U(\vec{\beta}) \|_F^2 + f(\vec{\beta})
\]  

(5)

This problem must be solved for every permutation of block types. Because there are three block choices per layer for a system with linear qubit connectivity, \( 3^\text{n} \) nonlinear least-squares problems must be solved to adequately search for Toffoli gate implementations with \( n \) multi-qubit operations. Since the shortest known implementation of the Toffoli gate over the gate set including single-qubit operations and the CR gate consists of eight CR gates, we need only search \( n = 1, 2, 3, \ldots, 7 \), since \( n \geq 8 \) would not generate more optimal linear Toffoli gate implementations.

For this numerical optimization problem, one must consider how close the unitary generated by a set of optimal parameters must be to the true unitary in order to be considered a Toffoli gate implementation. It is generally accepted that if the fidelity of a unitary with respect to some
target unitary is above 99.9% (or, equivalently, the infidelity of a unitary with respect to some target unitary is below 0.1%), then the unitary implements the target unitary [18]. Infidelity in this sense [28] is defined in Equation (6) where $\mu_1$ is infidelity, $U_{CCX}$ is the Toffoli gate unitary matrix, and $U(\vec{\beta})$ is the unitary matrix of a particular Toffoli gate implementation.

$$\mu_1 = 1 - \left| \frac{\text{Tr}(U_{CCX}^1 U(\vec{\beta}))}{8} \right|^2$$  \hspace{1cm} (6)

4.1.3 Minimizing the Objective Function. To find parameters that minimize the objective function in Equation (5), we used the Levenberg-Marquardt algorithm [33]. This algorithm was chosen because it is a standard method of solving unconstrained nonlinear optimization problems with several readily available software implementations. The Levenberg-Marquardt algorithm is a gradient-based algorithm that requires an initial guess from which to descend. Selection of the initial guess results in varying success, so several initial points per layered configuration must be tested. In practice, it was found that on the order of tens of points was sufficient.

Algorithm 1 describes the approach selected to search for $n$-layer Toffoli gate implementations. The computational complexity of this algorithm is $O(n^23^n)$ where $n$ is the number of circuit layers. Although this algorithm is exponential in nature, it is important to note the ease with which it can be parallelized. For example, a cluster of machines could each be assigned a specific multi-qubit circuit configuration to explore. If the machines have multiple cores, each core can be assigned a different initial parameter guess. The runtime of the ideal critical path length of this computation scales at rate $O(n^2)$. Although this algorithm can be computationally expensive, once novel implementations are discovered (e.g., via considerable computational effort), they can be easily stored and used by compilers on personal computers.

Additionally, if the desired underlying multi-qubit configuration of a circuit is already known, the algorithm can be run sequentially in polynomial time. Therefore, an additional application of this algorithm for larger circuits is reparameterizing them to enable analytical a priori optimizations.

4.2 Results
The algorithm presented in Section 4.1 was implemented in C++ [54] using the Google Ceres library [1] and parallelized with MPI. It was then used to run a computational search of $n$-layer
Algorithm 1: Searching for $n$-layer Toffoli implementation for a native gate set.

**Input:** List $o$ of multi-qubit native gates available on target hardware, integer $n \geq 1$ specifying the number of multi-qubit native gates that implementations should contain, integer $k \geq 1$ specifying the number of times to check each circuit configuration, and square residuals threshold $t$.

**Output:** Several parameter vectors $\{\vec{\beta}_i \in \mathbb{R}^{9n+9}\}$ and their corresponding quantum circuit structures implementing the Toffoli gate.

```
foreach $n$-length quantum circuit structure constructed from $o$ do
    for $i \leftarrow 1$ to $k$ do
        $\vec{\beta}_0 \leftarrow \vec{v} \in \mathbb{R}^{9n+9}$ where each entry in $\vec{v}$ is chosen from a uniform random distribution over the domain $[0, 2\pi)$;
        $\vec{\beta} \leftarrow$ result of running Levenberg-Marquardt starting from $\vec{\beta}_0$;
        if $\|U(\vec{\beta}) - U_{CCX}\|_F \leq t$ then
            Save quantum circuit structure and $\vec{\beta}$ to a file;
```

Toffoli gate implementations for $n = 1, 2, 3, \ldots, 7$ on a personal workstation (for $n = 1, 2, 3, 4$) and on the Argonne Bebop supercomputer (for $n = 5, 6, 7$). On the supercomputer, the program ran on 10 nodes. Each node solved all $3^n$ optimization problems on 36 cores using the Levenberg–Marquardt algorithm and a randomly generated starting point. For $n = 6$, the distributed algorithm ran for roughly half an hour. This implementation used an objective function agnostic to angle parameters (equivalent to setting $\alpha = \gamma = 0$ in Equation (5)) and discovered 38 six-layer quantum circuit structures and corresponding parameters capable of implementing the Toffoli gate.

One of these quantum circuit structures, shown in Figure 9 with angle parameters omitted for clarity, was then reparameterized by applying the SciPy Levenberg-Marquardt least squares optimizer [58] to the objective function in Equation (5) with $\alpha = 0.30$ and $\gamma = 10^{-8}$. The starting parameter vector provided to the least squares optimizer greatly affects the solution to which it will converge. By selecting several random starting parameter vectors and running the optimizer, it was found that this quantum circuit structure yielded several valid parameterizations with desirable angles (code and angle parameter values are available on GitHub [53]). Therefore, we propose numerical reparameterization of quantum circuit subsections as a tool for producing optimization opportunities.

4.3 Connection to Analytical Approach

It should be underscored that the numerical discovery approach and analytical \textit{a priori} approach are complementary. The numerical discovery approach can be used to find an initial implementation of a circuit or subcircuit, which can then be refined using analytical \textit{a priori} methods. This is best illustrated with an example. Consider the simple two-qubit circuit in Figure 10.

Notice that upon transpilation to native gates, there is no clearly applicable analytical \textit{a priori} method. Cross-gate pulse cancellation, for example, fails because $R_z$ gates used to implement the Hadamard and CNOT gates block physical $x$-rotation gates from canceling. It is in this situation.
that the numerical discovery method should be used. Notice this circuit is a two-qubit GHZ quantum circuit followed by a Hadamard gate and an X gate. If there exists a quantum circuit producing the two-qubit GHZ state that ends with a native gate sequence equivalent to a Hadamard gate on $q_0$ and an $X$ gate on $q_1$, then cross-gate pulse cancellation may be applied to entirely cancel the final two single-qubit gates in this circuit since both gates are their own inverses.

Such an implementation does in fact exist. It was discovered numerically using the methods developed in this section and led to the optimized circuit found in Figure 10. Note that this implementation requires only two layers of $\sqrt{X}$ gates and $540^\circ$ of active rotation. This compares favorably to the original quantum circuit, which contained five layers of $\sqrt{X}$ gates and $990^\circ$ degrees of active rotation.

This example clearly demonstrates the complementary nature of analytical a priori techniques such as cross-gate pulse cancellation and numerical quantum circuit discovery. The numerical discovery approach can be integrated into existing quantum compilers to provide otherwise unavailable optimization opportunities.

While the numerical discovery method is best suited for optimizing subcircuits with a small number of qubits, it can be easily generalized to an arbitrary number of qubits and multi-qubit gate set by determining the appropriate fundamental “layers” (see Figure 7). The applicability of these techniques to any native gate set and superconducting qubit architecture makes the numerical discovery approach broadly applicable to the quantum computing community.

5 APPLICATION TO QUANTUM COMPILATION

Quantum compilation is a highly non-trivial task that involves solving several problems, including qubit routing and decomposition to native gates. Traditionally, quantum compilation follows a two-pass approach in which input quantum circuits are first decomposed and then mapped onto physical qubits. Recently, however, a three-pass approach called “Orchestrated Trios” has been proposed [14]. In this approach, the compiler decomposes a quantum circuit while leaving Toffoli gates intact in its first pass. Next, the qubits acted on by Toffoli gates are routed (i.e., moved) in groups, or “trios” to accommodate the qubit architecture of the target device. Finally, all Toffoli gates are decomposed into either the standard 6-CNOT or 8-CNOT implementations, depending on trio connectivity.

The Toffoli gate optimization presented in Section 3 of this article was integrated into the third pass of the Orchestrated Trios compiler (referred to as the “PulseTrios” compiler). Toffoli gates were decomposed into the native gate-level quantum circuit in Figure 5. This resulted in significant quantum circuit length reductions. Table 3 shows the estimated probability of success of several quantum circuit benchmarks [4] and QAOA circuits for Maximum Independent Set [56] compiled with Qiskit, Trios, and PulseTrios.

The majority of these benchmarks have large depths and very low fidelities on current quantum hardware, making quantum process tomography infeasible to perform. Therefore, scaling system parameters such as gate error and decoherence time constants is a standard approach for estimating the probability of success of quantum circuits on near-term quantum devices. To illustrate the results of the optimized Toffoli gates on benchmark success rates, the IBMQ Mumbai device was
Table 3. Projected Success Probabilities of Several Quantum Circuit Benchmarks [4] when Compiled with Qiskit, Trios, and PulseTrios on Near-term Hardware

| Benchmark         | #Qubits | #Toffoli | #CNOT | #U3 | Qiskit   | Trios   | PulseTrios | Improvement |
|-------------------|---------|----------|-------|-----|----------|---------|------------|-------------|
| cnx_dirty [5]     | 18      | 16       | 0     | 0   | 66.0%    | 74.4%   | 78.1%      | 1.09x       |
| cnx_halfborrowed  | [17]    | 19       | 32    | 0   | 47.2%    | 56.9%   | 62.7%      | 1.15x       |
| cnx_logancilla    | [6]     | 19       | 17    | 0   | 64.4%    | 73.1%   | 77.0%      | 1.09x       |
| cnx_inplace [17]  | 4       | 54       | 46    | 33  | 29.6%    | 36.2%   | 42.6%      | 1.20x       |
| cuccaro_adder [12]| 20      | 18       | 46    | 18  | 55.7%    | 67.7%   | 71.5%      | 1.13x       |
| takahashi_adder   | [48]    | 20       | 18    | 44  | 56.0%    | 68.9%   | 72.7%      | 1.14x       |
| borrowedbit       | [17]    | 5        | 50    | 38  | 32.4%    | 39.4%   | 45.8%      | 1.19x       |
| grovers [22]      | 9       | 84       | 0     | 78  | 8.9%     | 22.3%   | 28.9%      | 1.80x       |
| QAOA_node6 [23, 56]| 6    | 4        | 32    | 56  | 81.5%    | 87.8%   | 88.9%      | 1.04x       |
| QAOA_node8 [23, 56]| 8    | 8        | 148   | 195 | 52.8%    | 73.3%   | 75.1%      | 1.19x       |

The geometric mean of the improvement of PulseTrios over Qiskit and Trios is shown in the final column.

chosen as the target device. We assume gate error rates to be 10x smaller than presently measured and decoherence time constants to be 10x larger than presently measured. Under these assumptions, the probability of quantum circuit success on a particular system can be estimated with Equation (7), where $F_i$ is the average fidelity of gates of type $i$, $n_i$ is the number of gates of type $i$ used, $\Delta$ is total circuit run time, $T_1$ is the system thermal relaxation time constant, and $T_2$ is the system dephasing time constant.

While PulseTrios shows an application of our purely analytical optimizations to quantum compilation, our combined analytical and numerical approach has been demonstrated by the QContext quantum compiler [31] on the IBMQ native gate set. QContext used the numerical discovery software presented in Section 4 to synthesize new implementations of the CNOT gate that yield cross-gate pulse cancellation opportunities. These cancellation opportunities resulted in QContext outperforming OrchestratedTrios, the state-of-the-art quantum compiler.

$$P_{success} = e^{-10\Delta/T_1-10\Delta/T_2} \prod_{i=1}^{N} \left(1 - \frac{1 - F_i}{10}\right)^{n_i}$$ (7)

6 CONCLUSION

Native gate-level analysis has opened a vast array of opportunities for optimization. In this article, we demonstrated that examining Toffoli gate implementations in the native gate set of target hardware (in this case, IBMQ machines) yields several opportunities for quantum circuit length reduction. This article presented cross-resonance gate sandwiching as a new analytical optimization technique that significantly reduces quantum circuit length. This technique was used in conjunction with existing techniques to produce a linear Toffoli gate implementation with 18% lower infidelity.

This article also contributed methodology for parameterizing quantum circuits with a finite set of real numbers and formulating quantum circuit length reduction as a nonlinear least-squares optimization problem that can be solved numerically in a distributed fashion. This technique was used to discover a Toffoli gate implementation with two fewer required multi-qubit gates than standard on a linearly connected qubit architecture with the IBMQ native gate set augmented with the multi-target cross-resonance gate. While this implementation was not able to be benchmarked with quantum process tomography, it merits further exploration and represents a direction for future research. In order to facilitate further exploration, the optimization code developed for this article will be made publicly available on GitHub.
Although optimizations were performed for the IBM system because (a) it is one of the most widely used quantum hardware platforms and (b) it is a leading system in terms of low-level access to pulse control and native gates, the principles expressed in our manuscript are applicable to other hardware platforms. For instance, the hidden inverse technique [61] has been used on trapped-ion systems; this technique is similar to the echo in cross-resonance gates and can be similarly optimized. In the same spirit, the leading two-qubit gate protocol on neutral atom systems [29] also involves an echoed sequence, which creates a polarity freedom that can be optimized.

Several avenues of future exploration exist for this topic. One direction is the continued development of context-aware compilers that leverage numerical resynthesis. Another direction is the application of the methodology presented in this paper to quantum gates and circuits besides the Toffoli gate. In terms of the native gate set augmentation aspect of this article, the multi-target cross-resonance gate represents only one of several promising gates that could augment the IBMQ native gate set architecture; several other native gate set augmentation candidates can be explored.

In summary, our work on optimizing the Toffoli gate supports the idea that examining quantum gates at a low level of abstraction yields a surprising number of opportunities for performance improvements. The primary contribution of this article is to encourage further exploration of quantum circuit optimization at the native gate set level of abstraction by concretely demonstrating the improvement of a frequently used quantum gate.

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