Abstract

Background: In Current VLSI circuits, e.g., Modules like accumulators, Arithmetic Logic Units (ALUs) are present generally in information line structure or discrete signal Processing chips. ABIST has a basic idea that is used by accumulators for built-in testing and its generated test patterns show the hardware overhead degradation and decreased circuit speed.

Method: In the present system this paper use a scheme which holds a generation of test patterns and is compared with previously proposed scheme. The test patterns created by accumulator proves that it takes input produced by a constant pattern holding an acceptable pseudorandom individuality, if a proper input pattern is selected. Weighed pseudorandom BIST schemes were utilized to bring down the vector number in BIST applications.

Findings: For the generation of test patterns, we use a group which has 0, 1 and 0.5 weights and this group is an impartial group and this use will lower the time needed for testing and also reduces power used. In the above work, digital circuits such as G27 Bench mark and SISO are, accumulator based BIST. Finally, the synthesis results of these circuits are compared with normal BIST. It was found that the circuit as low delay using accumulator based BIST.

Keywords: ABIST, ALU, BIST, CUT, Combinational Circuits

1. Introduction

Pseudo random Built-In Self-Test (BIST) generators are used for testing the merged circuits and systems. Accumulators driven by a standard value is used in the pseudorandom generator. Random patterns are generated by the circuit and it attains a greater fault coverage which helps to identify faults. Hence weighed pseudorandom with an input biasing of “0” or a “1” from 0.5 to some other value. A weighed random pattern generation with single weighedtask did not find faults completely. This paper use reasonable test patterns to identify most faults. If the propagation and activation requirement doesn't match, a large number of input combinations must be applied to the circuit so that entire faults are detected with lesser number of patterns, multiple weighed assignments have been suggested. Some deterministic test use derived weighed assignments because they have an ability to find maximum faults with minimum test patterns. Multiple weighed assignments with weights 0, 1, and 0.5 are reducing cost of implementation of hardware. In such a way some outputs from a generator remains stable (to either 0 or 1) and residual changes randomly (weight 0.5). The advantage of the system is that the hardware overhead is reduced effectively with minimal power consumption as some inputs remain same during specific test session. This was introduced for reducing the cost of implementation of hardware. In a similar manner a 3-weight random pattern generator based on scan chains also used for reducing the cost of implementation. Recently, patterns with 0, 1, and 0.5 scheme, provides an efficient compaction scheme. From the above analysis it is concluded that 3-weight pattern with 0, 1, and 0.5 is used generally as it reduces test time with decreased implementation cost. The present
VLSI circuits contain arithmetic modules. This gives rise to the arrival of arithmetic BIST (ABIST). ABIST uses accumulators for built-in testing which results in reduced hardware overhead with lower operating speed. The accumulator-based test pattern generation was compared to previous schemes. As a result of comparison, it was found that for the proper input selection, an accumulator with constant pattern holds an acceptable pseudorandom characteristic. Modules with harder faults may take additional test hardware by adding extra test patterns or by inserting test points. The accumulator weighed pattern generation scheme was proposed to overcome this problem. A test pattern with either of 0, 1, and 0.5 is generated thus reducing the test application time. The disadvantage of this scheme are 1) it can be used only when a ripple carry adder is used in the accumulator; 2) modification of accumulator is needed which may involve more cost with a change in the core data path and this is usually avoided in the present BIST schemes; and 3) the increased speed delay in adder is based on the normal operating speed. As per, a scheme for accumulator-based 3-weight generation is used for removing drawbacks of older system. More precisely: 1) the requirement of adder is not imposed; 2) the structure of adder remains same and so, 3) the speed for adder operation remains unaffected. The lateral scheme is compared to the schemes proposed in based on hardware overhead and the drawback is also found. The hardware complexity increases because of the usage of any type of adder in the generators. This disadvantage of hardware complexity can be overcome by replacing adder by XOR gate.

2. Weighed Pattern Generation OFAN Accumulator

This paper uses an example to explain the concept of a weighed pattern generation of an accumulator. Notify the checkgroup for the c17 ISCAS benchmark. Here this paper is in need to apply the 3-weighed pattern generation scheme on test group. So for this purpose this paper uses one of the schemes proposed in. By using this idea of weight assignment, separation of test group into two subgroups, G1 and G2 as follows: G1 = {T1, T4} and G2 = {T2, T3} takes place. The subgroups carry a weight assignment as denoted here W(G1) = {−, −, 1, −, 1}, and W(G2) = {−, −, 0, 1, 0}. Here a “_” denotes a weight assignment of 0.5, and “1” indicates the constantly driven input by the logic “1” value, and “0” indicates that the input is driven by the logic “0” value. For the first task, the inputs to I[2] and I[0] is a constant derived from “1”, while inputs I[4], I[3], I[1] are the pseudo randomly generated. Similarly, in the second weight assignment (subgroupG2), inputs I[2] and I[0] are constantly driven by “0”, input I[1] is driven by “1” and inputs I[4] and I[3] are pseudo randomly generated. These assignments of weight to the input test groups decides the configuration of accumulator for the below conditions viz., 1) an output to an accumulator may be a constant derived from “1” or “0” and 2) The carry output remains unchanged to “1” or “0”. The pseudorandom patterns are generated effectively in the accumulators’ output using the second condition given above.

3. Design Methodology

Figure 1 shows accumulator cell consists of a D flip-flop and Full Adder (FA) cell. This Figure 1 depicts an active high signals for group and regroup patterns. To attain this state any one of the three configurations from Figure 2 can be used.

A Accumulator cell drives the CUT inputs, when I[i] = 1. Thus this paper assume Group[i] = 1 and

Figure 1. Accumulator cell.

Figure 2. Configurations of accumulator cell.
Regroup\[i\] = 0 and hence I\[i\] = 1 and O\[i\] = 0. For an output 1, \(C_{in}\) is transferred automatically to \(C_{out}\). Next the CUT inputs when I\[i\] = "_" is depicted for its configuration. Here this paper get the values as shown Group\[i\] = 0 and Regroup\[i\] = 0. A value of either 1 or 0 is given to the D flip flop, which is the input of flip-flop register B, and this input value depends on the value of accumulator inputs. By next step, it place XOR gate in the place of adder. Further, the OR gate helps not to altering the resulting logic as that of XOR gate. This usage of two gates along with simple chips makes the circuit simple and the implementation becomes easy if IC chips contain one gate type per chip only.

This paper proposed a scheme of logic module, which affords the Group \([n-1:0]\) and Regroup \([n-1:0]\) signals that are driving the S and R inputs.

The 3-weight scan schemes and 3-weight pattern generation presented\(^5\) is compared with proposed scheme. The algorithms for test applications that are invented\(^10,13,14\) can be implemented by\(^16\) based on the number of test patterns. This paper doesn't impose any modification on the accumulator's adder in the proposed scheme. Therefore, data path timing characteristics are not affected.

This paper uses a scan chain which drives the output of a Linear Feedback Shift Register (LFSR) in the generation scheme of 3-weight pattern. Logic between scan chain and CUT inputs discussed in this study are to achieve the required output weight of 0, 0.5, or 1. A scan structure is used to implement the scheme. Here this paper also uses LFSR and scan counters. A 3-gate modules numbers are essential for each mandatory weighed input\(^17\). According to\(^17\), low-overhead 3-weight random BIST scheme, which is based on scan chains was compared to the parallel fixing BIST scheme. Decoding logic of hardware overhead is also calculated for ISCAS benchmarks that is presented in Table I.

4. Results

RTL Schematic of BIST generated Cadence RTL Compiler. Power and area are estimated. Figures 4 and 5 shows the output for RTL Schematic and Technology Schematic. Figure 6 shows the performance of delay.

The new defective models for MMOM covers a range of parametric defects to the multilevel applications. This proposed scheme of this study finds the faults by leveraging sneak-paths and tests the multiple memory elements and reduce the time by 2\%, using sneak-path as compared to previous tests. They created a BIST system which implements sneak-path testing.

Finally, the Figure 10 shows the comparison of power consumed by the chip, reduced in area and improvement in reduction of delay.
Design and Implementation of the Combinational Circuits Testing using Accumulator based BIST to Reduce Delay, Power Consumption and Area

This study tested the accumulator for generating the patterns based on weight and this can be used for generating patterns on weight and this is achieved without changing the adder shape. When comparing the proposed idea with the previously present techniques which results the overhead of hardware is reduced in the present system meanwhile the structure of accumulator is unaltered and because of this testing time is minimized for about 20%–95%. Scan based pattern generation have more hardware overhead when compared to our scheme. At last we conclude the hardware overhead is reduced in currently proposed system by comparing with the accumulator- based scheme proposed19. This system was mainly designed for maintaining proper speed and area. And we need to check our system using Project on Static Timing Analysis (STA) and System on chip verification (SOC) in order to debug and design layout.

5. Conclusion

6. References

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