PCM-trace: Scalable Synaptic Eligibility Traces with Resistivity Drift of Phase-Change Materials

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Abstract—Dedicated hardware implementations of spiking neural networks that combine the advantages of mixed-signal neuromorphic circuits with those of emerging memory technologies have the potential of enabling ultra-low power pervasive sensory processing. To endow these systems with additional flexibility and the ability to learn to solve specific tasks, it is important to develop appropriate on-chip learning mechanisms. Recently, a new class of three-factor spike-based learning rules have been proposed that can solve the temporal credit assignment problem and approximate the error back-propagation algorithm on complex tasks. However, the efficient implementation of these rules on hybrid CMOS/memristive architectures is still an open challenge. Here we present a new neuromorphic building block, called PCM-trace, which exploits the drift behavior of phase-change materials to implement long lasting eligibility traces, a critical ingredient of three-factor learning rules. We demonstrate how the proposed approach improves the area efficiency by $>10\times$ compared to existing solutions and demonstrates a technologically plausible learning algorithm supported by experimental data from device measurements.

I. INTRODUCTION

Neuromorphic engineering uses electronic analog circuit elements to implement compact and energy-efficient intelligent cognitive systems [1–4]. Leveraging substrate’s physics to emulate biophysical dynamics is a strong incentive toward ultra-low power and real-time implementations of neural networks using mixed-signal memristive event-based neuromorphic circuits [5–8]. The majority of these systems are currently deployed in edge-computing applications only in inference mode, in which the network parameters are fixed. However, learning in edge computing can have many advantages, as it enables adaptation to changing input statistics, reduced network congestion, and increased privacy. Indeed, there have been multiple efforts implementing Spike-Timing Dependent Plasticity (STDP)-variants and Hebbian learning using neuromorphic processors [9–11]. These methods control Long Term Depression (LTD) or Long Term Potentiation (LTP) by specific local features of pre- and post-synaptic activities. However, local learning rules themselves do not provide any guarantee that network performance will improve in multi-layer or recurrent networks. Local error-driven approaches, e.g., the Delta Rule, aim to solve this problem but fail to assign credit for neurons that are multiple synapses away from the network output [12, 13]. On the other hand, it has been recently shown that by using external third-factor neuromodulatory signals (e.g., reward or prediction error in reinforcement learning, teaching signal in supervised learning), this can be achieved in hierarchical networks [14, 15]. However, there needs to be a mechanism for synapses to remember their past activities for long periods of time, until the reward event or teacher signal is presented. In the brain, these signals are believed to be implemented by calcium ions, or CAMKII enzymes in the synaptic spine [16] and are called eligibility traces. In machine learning, algorithmic top-down analysis of the gradient descent demonstrated how local eligibility traces at synapses allow networks to reach performances comparable to error back-propagation algorithm on complex tasks [17–19]. Examples of neuromorphic platforms that implement these types of eligibility traces in spiking neural networks already exist [20–22]. However, learning in these platforms is only supported through the use of von-Neumann processors, either shared with the computation of network dynamics [21] or a dedicated core [20, 22]. Relying on numerical integration, these platforms do not leverage the physics of their computing substrate and are not free from the von-Neumann bottleneck problem [23, 24]. On the other hand, mixed-signal analog/digital neuromorphic circuits allow the use of in-memory computing that directly emulates the desired neural and synaptic dynamics using the physics of analog elements [25–27]. However, even though progress has been made in extending the duration of synaptic traces using advanced Fully-Depleted Silicon on Insulator (FDSOI) technologies [28], implementing tens-of-seconds-long time constants solely based on Complementary Metal-Oxide-Semiconductor (CMOS) is not scalable, as it requires the use of large capacitors. In this paper, we present a novel approach to exploit the drift behavior of Phase Change Memory (PCM) devices to intrinsically perform Eligibility Trace (ET) computation over behavioral timescales. We present the PCM-trace building block as a hybrid memristive-CMOS circuit solution that can lead to record-low area requirements per synapse. To the best of our knowledge, this is the first work that uses a memristive device not only to store the weight of synapses, but also to keep track of synaptic eligibility to interact with a third factor toward scalable next-generation on-chip learning.

II. ELIGIBILITY TRACES

The ET can be described as a decaying synaptic variable as in Eq. (1). The value of the ET at the synapse between pre-synaptic neuron $j$ and post-synaptic neuron $i$ can be controlled as a usually linear function, $f_j$, of the pre-synaptic activity $x_j$, and potentially non-linear function $g_i$ of the post-synaptic activity $x_i$ such that

$$e^{t+\Delta t}_{ij} = \alpha e^{t}_{ij} + \eta f_j(x_j^t)g_i(x_i^t), \quad (1)$$

where $\alpha$ is the learning rate, $\eta$ is the input gain, and $f_j(x_j^t)$ and $g_i(x_i^t)$ are the input and output functions, respectively. The ET is a critical ingredient of three-factor learning rules, as it enables adaptation to changing input statistics, until the reward event or teacher signal is presented. In the brain, these signals are believed to be implemented by calcium ions, or CAMKII enzymes in the synaptic spine and are called eligibility traces. In machine learning, algorithmic top-down analysis of the gradient descent demonstrated how local eligibility traces at synapses allow networks to reach performances comparable to error back-propagation algorithm on complex tasks. However, learning in these platforms is only supported through the use of von-Neumann processors, either shared with the computation of network dynamics or a dedicated core. Relying on numerical integration, these platforms do not leverage the physics of their computing substrate and are not free from the von-Neumann bottleneck problem. On the other hand, mixed-signal analog/digital neuromorphic circuits allow the use of in-memory computing that directly emulates the desired neural and synaptic dynamics using the physics of analog elements. However, even though progress has been made in extending the duration of synaptic traces using advanced Fully-Depleted Silicon on Insulator (FDSOI) technologies, implementing tens-of-seconds-long time constants solely based on Complementary Metal-Oxide-Semiconductor (CMOS) is not scalable, as it requires the use of large capacitors. In this paper, we present a novel approach to exploit the drift behavior of Phase Change Memory (PCM) devices to intrinsically perform Eligibility Trace (ET) computation over behavioral timescales. We present the PCM-trace building block as a hybrid memristive-CMOS circuit solution that can lead to record-low area requirements per synapse. To the best of our knowledge, this is the first work that uses a memristive device not only to store the weight of synapses, but also to keep track of synaptic eligibility to interact with a third factor toward scalable next-generation on-chip learning.
where $\eta$ is a constant and $\alpha = e^{-\Delta t/\tau_m}$ is the decay rate of ET. $
abla_t$ is decay time-constant up to tens of seconds in behavioural time-scales and $\Delta t$ is discrete time-step \textsuperscript{14}. The $e_{ij}$ acts as a temporal correlation detector between pre-synaptic $f_j(x_j)$ and post-synaptic $g_i(x_i)$ functions. The instantaneous correlation between $f_j$ and $g_i$ is defined as synaptic tagging, which is accumulated by $e_{ij}$ to keep track of past correlations. The $f$ and $g$ functions are determined by the chosen synaptic learning rule. For example, $f_j(x_j)$ is the low-pass filtered pre-synaptic events in e-prop and BDSP \textsuperscript{17}, \textsuperscript{29}, and $g_i(x_i)$ is a non-linear function of the post-synaptic state for e-prop and SuperSpike \textsuperscript{18}.

III. PCM MEASUREMENTS

Temporal evolution of electrical resistivity is a widely-observed phenomenon in PCM due to the rearrangements of atoms in the amorphous phase \textsuperscript{30}. This behavior is commonly referred to as structural relaxation or drift. To start the drift, a strong RESET pulse is applied to induce a crystalline to amorphous phase transition where the PCM is melted and quenched. The low-ordered and highly-stressed amorphous state then evolves to a more energetically favorable glass state within tens of seconds \textsuperscript{31}. At constant ambient temperature, the resistivity follows

$$R(t) = R(t_0) \left( \frac{t}{t_0} \right) ^{\nu} , \quad (2)$$

where $R(t_0)$ is the resistance measured at time $t_0$ and $\nu$ is the drift coefficient. It has been experimentally verified by many groups that Eq. (2) can successfully capture the drift dynamics \textsuperscript{31}−33, from microseconds to hours range \textsuperscript{34}.

We integrated Ge$_2$Sb$_2$Te$_5$-based PCM in state-of-the-art PCM heater-based devices fabricated in the Back-End-Of-Line (BEOL) based on 130 nm CMOS technology. The PCM thickness is 50 nm with the bottom size of 60 nm $\times$ 60 nm. Drift measurements were performed on three devices to monitor the temporal evolution of the resistance in the High-Resistive State (HRS) state, particularly confirming the model in Eq. (2). The test was conducted by first resetting all the cells by applying a RESET pulse to the heater, which has a width of 100 ns with 5 ns rising and falling times, and a peak voltage of 1.85 V. Then, an additional programming pulse is used to bring the devices to different initial conditions, corresponding

IV. PCM-TRACE

PCM-trace is a novel method to implement seconds-long ET on the synapse using the drift feature of PCM. By writing Eq. (2) as a difference equation of the conductance, we can show that the temporal evolution of the conductance has decay characteristics similar to Eq. (1) such that $G_{ij}^{t + \Delta t} = \left( \frac{t - \tau_p}{t - \tau_p + \Delta t} \right)^{\nu} G_{ij}^t$, where $G_{ij}^t = 1/R_{ij}^t$, and $\tau_p$ is the last programming time as drift re-initializes with every gradual SET \textsuperscript{35}, \textsuperscript{36}. The main difference is that the rate of change in PCM resistivity is a function of time; nevertheless, its time constant is comparable for behavioral time-scales as $\tau_{PCM} = \Delta t / \log((t/(t + \Delta t))^\nu)$ is on the order of tens of seconds \textsuperscript{37}. Therefore, the PCM-trace dynamics can emulate the ET of the synapse as follows:

$$G_{ij}^{t + \Delta t} = \left( \frac{t - \tau_p}{t - \tau_p + \Delta t} \right)^{\nu} G_{ij}^t + \eta f_j(x_j) g_i(x_i) \quad (3)$$

In the PCM-trace method (Eq. 3), the accumulating term on the ET is implemented by applying a gradual SET to the PCM device whenever the synapse is tagged. To maximize the number of accumulations a PCM device can handle without getting stuck in the Low-Resistive State (LRS) regime, some operational conditions need to be satisfied. We initialize the device to HRS by applying a strong RESET pulse, and wait for an initialization time $t_{init}$ of at least 250 ns for the device resistance to increase. If $t_{init}$ is too short, the device conductance would still be too high to be able to accumulate enough tags; and if it is too long, the decay will be weaker (see Eq. 2). Initialization time can be modulated to reach the desired drift speed depending on the material choice and the application. After the initialization time, whenever the synapse is tagged, a single gradual SET (with an amplitude of 100 $\mu$A and a pulse width of 100 ns with 5 ns rising and falling times) is applied. To make sure that the device stays in the HRS, a read-verify-set scheme can be used. Finally, the value of the ET can be measured after seconds by reading the conductance of the device (see Fig. 2).
A. Multi PCM-trace

The number of gradual SET pulses applied to a single PCM-trace device is limited, because each pulse partially increases the device conductivity and eventually move the device toward its LRS (< 2 MΩ), where the drift converges to a higher baseline level. This problem can be solved by storing the synaptic ET distributed across multiple PCM devices, as in Fig. 3. By successively routing the tags to multiple PCM devices, the number of gradual SET pulses to be applied per single device is significantly reduced. Fig. 4 demonstrates the increase of effective dynamic range (number of updates to ET without getting stuck in the LRS) using multiple PCM devices.

![Fig. 3: Multi PCM-trace concept. Each synapse has a weight and a PCM-trace block where multiple parallel PCM devices keep the ET of the synapse with their natural drift behavior. The postsynaptic neuron receives the sum of product of the pre-synaptic activity and the weight block. In parallel, the PCM-trace block calculates the ET as a function of pre- and post-synaptic activities (Eq. [3]), to be used in the weight update.](image)

![Fig. 4: Accumulating ET using multi-PCM configuration. Synapse receives 15 tags between 300 ms to 1300 ms which are routed to three different devices shown in the top three plots. The effective ET is calculated by applying a READ pulse to the parallel PCM devices. The initialization duration and synaptic activity period are shown with dashed lines in the bottom plot. The synaptic efficacy $W_{ij}$ is modified depending on the state of ET once the third-factor signal arrives.](image)

Fig. 5: PCM-trace-based neuromorphic architecture for three-factor learning. Only positive ET ($e_{ij}^+$) and $W_{ij}^+$ are shown.

V. CIRCUIT AND ARCHITECTURE

A. PCM-trace Architecture

An example in-memory event-based neuromorphic architecture is shown in Fig. 5 where the PCM-trace is employed to enable three-factor learning on behavioral time scales.

**Synapse**: Each synapse includes a weight block $W_{ij}$ in which two PCM devices are used in differential configuration to represent positive and negative weights $W_{ij}^+$ and $W_{ij}^-$. The effective synaptic weight is calculated as the difference of these two conductance values, i.e., $W_{ij} = W_{ij}^+ - W_{ij}^-$. Also, each synapse has a PCM-trace block $e_{ij}$ that keeps the ET. Inside the PCM-trace block, there are two PCM devices, keeping track of the positive and negative correlation between pre and post-synaptic neurons. On the onset of the pre-synaptic input spike, $PRE_{ij}$, (i) $W_{ij}$ is read, and the current is integrated by the post-synaptic neuron $i$; and (ii) Based on the $UP/DN$ signal from the learning block (LB), a gradual SET programming current is applied to positive/negative PCM-trace devices.

**Neuron with Learning Block (LB)**: The LB estimates the pre-post synaptic neuron correlation using the Spike Driven Synaptic Plasticity (SDSP) rule [39]. At the time of the pre-synaptic spike, the post-synaptic membrane variable is compared against a threshold, above (below) which an UP ($DN$) signal is generated representing the tag type. On the arrival of the third factor binary reward signal, $REW$, the state of the ETs devices is read by the $V_{PROG}$ block (Fig. 6b) which generates a gate voltage that modulates the current that programs the weight devices $W_{ij}$ (see Alg. 1).

B. Circuit simulation

Fig. 6 describes the block diagram of the LB implementing SDSP rule, which calculates the pre-post neurons’ correlation. The membrane variable (described here as a current $I_{mem}$ since circuits are in current-mode) is compared against a threshold value $I_{th}$ through a Bump circuit [38, 40]. The output of this block is digitized through a current comparator (in our design chosen as a Winner-Take-All (WT A) block [41]) and generates $UP/DN$ signals if the membrane variable is above/below the threshold $I_{th}$, and STOP, $SP$, if they are close within the dead zone of the bump circuit [40]. Fig. 6 presents the circuit schematic which reads the PCM-trace and generates $V_{PROG}$. To read the state of the device, a voltage
divider is formed between the PCM device and a pseudo resistor, highlighted in green. As the device resistance changes, the input voltage to the differential pair, highlighted in red, changes. This change is amplified by the gain of the diff. pair and the device current is normalized to its tail current giving rise to $I_{\text{PROG}}$ which develops $V_{\text{PROG}}$ through the diode-connected NMOS transistor. $V_{\text{PROG}}$ is connected to the gate of the transistor in series with the weight PCM (see Fig. 5). Fig. 7 plots $P_{\text{PRE}}$, $I_{\text{mem}}$, the output of the learning block at the time of the PRE, and the gradual SET pulse applied to the device. As shown, the $U$ signal is asserted when the membrane current is higher than the threshold indicated in red, which causes a gradual SET pulse with 100 $\mu$A to be applied across the PCM-trace device upon PRE events. Fig. 7 shows the generated $I_{\text{PROG}}$ as a function of the state of the ET device. The higher the ET device’s resistance, the less the accumulated correlation, thus the lower the programming current that should be applied to the weight device. The resistance on the x axis of the plot matches the measured resistance of PCM devices shown in Fig. 6.

VI. DISCUSSION AND CONCLUSION

Long-lasting ETs enable the construction of powerful learning mechanisms for solving complex tasks by bridging the synaptic and behavioral time-scales. In this paper, for the first time, we proposed to use the drift of PCM devices to implement ETs, and analyzed their feasibility for implementation in existing fabrication technologies.

The implementation of the three-factor learning rules with ETs per synapse requires complex memory structures for keeping track of the ET and the weight. Our proposed approach has clear advantages for scaling. Table I shows a comparison between our PCM synapse and a CMOS-only implementation in 22 nm FDSOI technology from [28].

PCM is among the most advanced emerging memory technology integrated into the neuromorphic domain [42]. Our approach of using PCM to store both the synaptic weight and the ET requires no additional nano-fabrication methods.

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Algorithm 1: Three-factor learning with PCM-trace

```plaintext
W_{ij}^+ = rand(); W_{ij}^- = rand();
RESET(e_{ij}^+); RESET(e_{ij}^-);

while $t < \text{taskDuration}$ do
    $I_{i,x} = 1 - (V_{i,th} - V_{i,mem})/V_{i,th}$;
    if @PRE and $t > t_{\text{init}}$ then
        # Eligibility trace accumulation
        forall $e_{ij}$ do
            if $I_{i,x} > I_{th}$ then
                GRADUAL_SET(e_{ij}^+);
            else if $I_{i,x} < I_{th}$ then
                GRADUAL_SET(e_{ij}^-);
        # Third-factor
        if Reward then
            forall $W_{ij}$ do
                $I_{ij,e^+}, I_{ij,e^-} = \text{READ}(e_{ij}^+, e_{ij}^-)$;
                $I_{\text{PROG}}^+ = I_{ij,e^+} * \text{scale Const};$
                $I_{\text{PROG}}^- = I_{ij,e^-} * \text{scale Const};$
                GRADUAL_SET(W_{ij}^+, I_{\text{PROG}}^+);
                GRADUAL_SET(W_{ij}^-, I_{\text{PROG}}^-);
```

TABLE I: Area comparison of ET implementation

|               | Area ($\mu m^2$) | $\tau$ (s) | Area/$\tau$ ($\mu m^2 \text{s}^{-1}$) |
|---------------|-----------------|------------|-----------------------------------|
| CMOS [28]     | 20 x 17         | 6          | 50.6                              |
| PCM [This work] | 12 x 12         | > 30       | < 4.8                             |

Fig. 6: (a) Learning block diagram generating UP/DN signals as a function of the correlation between pre and post-synaptic activity. (b) $V_{\text{PROG}}$ circuit reading from the ET device through the voltage divider (green) and generating $I_{\text{PROG}}$ through the diff. pair (red) to program the weight device.

Fig. 7: a) From the top: PRE events, POST membrane current ($I_{\text{mem}}$) and learning threshold ($I_{th}$). PRE events only when $I_{\text{mem}}$ is higher than $I_{th}$, and corresponding gradual SET current pulse applied to PCM-trace. b) Programming current to be applied to the weight PCM as a function of ET state.
