A high-precision and low-temperature-coefficient bandgap voltage reference is proposed in 0.11 μm CMOS process. A temperature piecewise compensation circuit is added to a traditional bandgap reference to decrease the temperature coefficient (TC). The digital trimming technology has been used to solve the deviation of TC and output voltage resulting from process corner and mismatch. Simulation result shows that the bandgap reference achieves TC of 2.18 ppm/°C from −40°C to 125°C. Bandgap reference output voltage is 1.2 V with the error of ±5 mV.

**Keywords:** bandgap voltage reference, temperature piecewise compensation, digital trimming, and temperature coefficient

**Classification:** Integrated circuits (memory, logic, analog, RF, sensor)

1. **Introduction**

Bandgap reference is a key component of analog, digital or mixed signal circuits such as analog to digital converters, digital to analog converters, low drop-out voltage regulators, phase-locked loops, and many other electronic devices [1, 2, 3, 4, 5, 6, 7]. Bandgap references provide voltage with a well-defined and stable insensitive to power supply voltage and temperature variation. The accuracy and stability of references play a significant role in the performance of the subsequent circuit [8, 9]. As a result many high-order temperature compensation techniques have been proposed to reduce the TC. The temperature-dependent resistor ratio compensation technique has been discussed in [10, 11, 12]. The curvature compensation effect of which is mainly determined by the ratio of two temperature coefficients resistors, which will drift dramatically according to the process corner and mismatch. Further discussion in [13, 14, 15, 16] adopts a temperature compensation mechanism that uses a gate-source voltage of the MOS transistor working in the sub-threshold region to compensate. However, the area of the sub-threshold MOS transistor is larger because of compensating. Therefore, the TC is greatly affected by the process. Elsewhere uses a nonlinear compensation term of $T \ln T$ method in [17]. The $T \ln T$ is generated by the voltage difference of two transistors working in different current states. But the structure of circuit is complex which needs more chip area and current consumption. However, the piecewise compensation technique [18, 19, 20, 21, 22, 23, 24] successfully eliminates non-linearity. And the compensation technique has been used in this paper.

The accuracy of the bandgap reference voltage is highly sensitive to the influence of several non-ideal characteristics introduced in the semiconductor manufacturing process, including device mismatch, absolute value deviation and package stress etc. Additionally, the length of all transistors will be shorter than the nominal length if over-etching occurs [25, 26]. The digital trimming technology has been used to resolve errors of output voltage and TC due to mismatch and process corners [27, 28, 29, 30].

In this paper, the piecewise compensation and digital trimming technology are combined in the design. Simulation result shows that the bandgap reference achieves high-precision and low-temperature-coefficient characteristics.

2. **Proposed design**

The traditional bandgap reference circuit is the first-order temperature compensated. It achieves the zero-temperature bandgap reference by the weighted sum of the emitter-base voltage $V_{BE}$ with a negative TC and the thermal voltage $V_T$ with a positive TC. But the traditional first-order bandgap reference can obtain low-temperature-coefficient in a defined temperature point not a higher temperature range, which does not meet the requirement of high-precision bandgap reference.

The proposed bandgap reference is shown in Fig. 1. When the traditional bandgap voltage shifts to a negative TC voltage, digital trimming technology can be used to adjust the TC. The positive TC current $M \cdot I_{PTAT}$ is produced by trim-
The positive TC voltage is used to compensate the circuit for obtaining a zero-temperature bandgap reference voltage. So the high-order temperature compensated bandgap reference voltage $V_{\text{REF}}$ is obtained.

The piecewise compensation current $I_{\text{NL1}} + I_{\text{NL2}}$ is to compensate high-order non-linearity. The output voltage can be adjusted by the reference current $I_{\text{REF}}$, when output voltage accuracy is impacted by the mismatch.

Fig. 2 indicates the positive TC voltage $V_{\text{trim}}$ is produced by the current $M \cdot I_{\text{PTAT}}$ flow through the resistor $R_3 + R_4$. The positive TC voltage is used to compensate the circuit for obtaining a zero-temperature bandgap reference voltage when the traditional bandgap reference voltage $V_{\text{REF}}$ has a negative TC. MOS transistors $M_1$, $M_2$ and $M_3$ have the same device parameter, the emitter area of $Q_2$ is $N$ times that of $Q_1$. The resistors $R_1 - R_4$ are made of the same material for offsetting the influence of the resistance temperature. Therefore, the output reference voltage $V_{\text{REF}}$ is shown in Eq. (1).

$$V_{\text{REF}} = V_{\text{BE3}} + \left[R_2 + (R_3 + R_4)(1 + M)\right] \frac{kT}{qR_1} \ln N$$

Eq. (1) indicates that the first-order bandgap reference can be obtained by optimizing resistors $R_1 - R_4$, parameter $N$ and parameter $M$.

The piecewise temperature compensation circuit technique of the proposed bandgap reference is achieved by adding a piecewise current in the low temperature and high temperature region to the first-order bandgap reference. The compensation current is obtained by subtracting the positive coefficient current and negative coefficient current.

Fig. 3 shows the temperature characteristic curve of high-order temperature compensated bandgap reference voltage $V_{\text{REF}}$ and the compensation voltage, $V_{\text{NL1}}$ and $V_{\text{NL2}}$. We determine the negative TC compensation current $I_{\text{NL1}}$ by taking the $I_{\text{CTAT}}$ current and subtracting the $I_{\text{PTAT}}$ current when the value $T$ is less than $T_1$. The voltage $V_{\text{NL1}}$ is produced by the current $I_{\text{NL1}}$ through the resistor $R_4$. The voltage $V_{\text{NL1}}$ is decreased linearly with increasing temperature, as shown in Fig. 3. No compensation measures are taken in the circuit when the value $T$ from $T_1$ to $T_2$. The positive TC compensation current $I_{\text{NL2}}$ is obtained by taking the $I_{\text{PTAT}}$ current and subtracting the $I_{\text{CTAT}}$ current when the value $T$ is greater than $T_2$. The voltage $V_{\text{NL2}}$ is produced by the current $I_{\text{NL2}}$ through the resistor $R_4$. The voltage $V_{\text{NL2}}$ is increased linearly with the increasing temperature, as shown in Fig. 3. The voltage $V_{\text{NL1}} + V_{\text{NL2}}$ can compensate the temperature high-order non-linearity of the first-order temperature compensated bandgap reference voltage. So the high-order temperature compensated bandgap reference voltage $V_{\text{REF}}$ is obtained.

According to the above analysis, the output reference voltage $V_{\text{REF}}$ of the proposed high-order curvature-compensated bandgap reference is shown in Eq. (2).

$$V_{\text{REF}} = V_{\text{BE3}} + \left[R_2 + (R_3 + R_4)(1 + M)\right] \frac{kT}{qR_1} \ln N + R_4(I_{\text{NL1}} + I_{\text{NL2}})$$

The proposed bandgap voltage reference circuit is shown in Fig. 4. The reference voltage source is composed of the $I_{\text{PTAT}}$ circuit, $I_{\text{CTAT}}$ circuit, low temperature compensation circuit, high temperature compensation circuit, TC trimming circuit, output voltage circuit trimming and $V_{\text{REF}}$ generator circuit.

$A_1$, $A_2$ and $A_3$ are high gain amplifiers. $M_1$, $M_2$ are the same with their aspect ratio. The emitter area of $Q_1$ is $N$ times of $Q_2$. The current $I_{\text{PTAT}}$ is generated by $Q_1$, $Q_2$, $M_1$, $M_2$, $R_1$ and $A_1$, as shown in Eq. (3).

$$I_{\text{PTAT}} = \frac{kT}{qR_1} \ln N$$

The $R_7 - R_9$ and $R_3$ are made of exactly the same material. Therefore, the voltage $V_{\text{PTAT}}$ is produced by the current $I_{\text{PTAT}}$ through the $R_7$, $R_8$ and $R_9$, as shown in Eq. (4).

$$V_{\text{PTAT}} = (R_7 + R_8 + R_9) \frac{kT}{qR_1} \ln N$$

Therefore $Q_2$, $M_3$, $A_2$, and $R_3$ generate current $I_{\text{CTAT}}$ is shown in Eq. (5).

$$I_{\text{CTAT}} = \frac{V_{\text{BE2}}}{R_2}$$

In the core circuit of the low temperature compensation, the width-length ratio of $M_6$ is $\beta_1$ times of $M_3$, the width-length ratio of $M_5$ is $\beta_2$ times of $M_1$, the width-length ratio of $M_8$ is $\beta_1$ times of $M_5$, and the width-length ratio of $M_9$ is $\beta_4$ times $M_8$. The voltage $V_{\text{NL1}}$ is produced by the compensation current $I_{\text{NL1}}$ through the $R_9$, as shown in Eq. (6).

$$V_{\text{NL1}} = \left\{ \begin{array}{ll} R_9 \beta_1 \left( \frac{V_{\text{BE2}}}{R_2} - \frac{kT}{qR_1} \ln N \right), & T \leq T_1 \\ 0, & T > T_1 \end{array} \right.$$

Eq. (6) indicates that $T$C of $V_{\text{NL1}}$ can be adjusted by optimizing the $\beta_1 - \beta_4$ parameters.
In the core circuit of high temperature compensation, the width-length ratio of M10 is $\beta_3$ times of M1, the width-length ratio of M13 is $\beta_6$ times of M1, the width-length ratio of M12 is $\beta_1$ times of M11, and the width-length ratio of M15 is $\beta_4$ times of M14. The voltage $V_{NL2}$ is produced by the compensation current $I_{NL2}$ through the $R_9$, as shown in Eq. (7).

$$V_{NL2} = \begin{cases} R_9\beta_8 \left( \beta_3\beta_7 \frac{kT}{qR_1} \ln N - \beta_6 \frac{V_{BE2}}{R_2} \right), & T \geq T_2 \\ 0, & T < T_2 \end{cases} \quad (7)$$

Eq. (7) indicates that the TC of $V_{NL2}$ can be adjusted by optimizing the $\beta_5$–$\beta_8$ parameters.

The TC of the reference voltage is improved by the TC trimming circuit. It can reduce the impact of non-systematic errors.

In the TC trimming circuit, the width-length ratio of M51–M56 is $\beta_9$ times of M1 respectively. Additionally, the current value $M \cdot I_{PTAT}$ of the trim network access circuit can be controlled by a 6-bit binary code S(0)–S(5). The transistors M51–M56 are turned on when the binary code is 0. The voltage $V_{trim}$ is produced by the trimming current $M \cdot I_{PTAT}$ flowing through the $R_8$ and $R_9$, as shown in Eq. (8).

$$V_{trim} = M I_{PTAT}(R_8 + R_9) = \frac{kT}{qR_1} \ln N \beta_9 \left( S(0) + S(1) + \cdots + S(5) \right) (R_8 + R_9) \quad (8)$$

In Eq. (8), $S(0)$–$S(5)$ are the logic NOT of the binary number S(0)–S(5).

The accuracy of output voltage accuracy is more severely affected by errors since the complexity of the bandgap reference circuit is increased. Therefore, a digital trimming circuit is needed to trim the output voltage.

In the output voltage trimming circuit, $V_{bg1}$ is the high-order bandgap reference voltage. M1, M20 are entirely the same, so the value of voltage $V_{bg1}$ is determined, as shown in Eq. (9).

The voltage of X1 is equal to the voltage of $V_{bg1}$ because of the amplifier circuit of a negative feedback loop and the high gain amplifiers $A_3$. The resulting reference current $I_{REF}$ is shown in the Eq. (10).

$$V_{bg1} = V_{BE3} + (R_3 + R_4 + R_5) \frac{kT}{qR_1} \ln N + R_5 \beta_4 \left( \beta_3\beta_7 \frac{V_{BE2}}{R_2} - \beta_2 \frac{kT}{qR_1} \ln N \right) + R_4 \beta_8 \left( \beta_3\beta_7 \frac{kT}{qR_1} \ln N - \beta_6 \frac{V_{BE2}}{R_2} \right) + \frac{kT}{qR_1} \ln N \beta_9 \left( S(0) + S(1) + \cdots + S(5) \right) (R_4 + R_5)$$

$$I_{REF} = \frac{V_{bg1}}{R_6} \quad (10)$$

In the output voltage trimming circuit, the width-length ratio of M515–M518 is $\beta_{10}$ times of M514, respectively. The current value $W \cdot I_{REF}$ of the trim network access circuit can be controlled by a 4-bit binary code W(0)–W(3). The M510–M522 can be controlled by binary code W(0)–W(3). The voltage $V_{CP}$ is produced by the reference compensation current $W \cdot I_{REF}$ through the $R_7$, $R_8$ and $R_9$, as shown in Eq. (11).

$$V_{CP} = W I_{REF}(R_7 + R_8 + R_9) = \frac{V_{bg1}}{R_6} \beta_{10} \left( W(0) + \cdots + W(3) \right) (R_7 + R_8 + R_9) \quad (11)$$

So Eq. (4), Eq. (6), Eq. (7), Eq. (8) and Eq. (11) show that the output voltage $V_{EFF}$ of the proposed bandgap reference voltage is shown in Eq. (12).

$$V_{REF} = V_{BE4} + V_{PTAT} + V_{NL1} + V_{NL2} + V_{trim} + V_{CP} \quad (12)$$

In summary, the temperature performance and accuracy of the proposed high-order bandgap reference can be effectively improved by adopting these techniques including piecewise temperature compensation and the digital trimming.

### 3. Experimental results

The proposed bandgap voltage reference circuit is designed

![Proposed circuit of the bandgap voltage reference](image-url)
with a 0.11 μm CMOS process. Fig. 5 shows the variation of $V_{\text{REF}}$ with temperature for different corners without trimming over a temperature range of $-40^\circ$C to $125^\circ$C. The TC are 2.33, 8.40, 10.37 and 7.98 ppm/$^\circ$C for the TT, SS, FF, SF and FS corners, respectively. Simulation results indicate that the bandgap reference voltage $V_{\text{REF}}$ without trimming does not achieve the output value of 1.2 V in different process corners. Furthermore, the TC is much higher in some corners. Therefore, the bandgap reference must be trimmed.

Fig. 6 shows the variation of $V_{\text{REF}}$ after trimming over a temperature range of $-40^\circ$C to $125^\circ$C. The proposed bandgap voltage reference $V_{\text{REF}}$ maximum value is 1.2022 V and the minimum value is 1.1998 V. Additionally, the TC of the bandgap reference have been improved dramatically after trimming. The TC are 2.18, 2.21, 2.66, 3.68 and 2.22 ppm/$^\circ$C for TT, SS, FF, SF and FS corners, respectively.

Fig. 7 shows the simulated temperature dependence of the proposed bandgap voltage reference at the TT corner over a temperature range of $-40^\circ$C to $125^\circ$C with a supply voltage of 2.2, 2.4, 2.6, 2.8, 3.0, 3.2, 3.3, 3.4 and 3.6 V, respectively. With a power supply of 3.0 V, the proposed bandgap voltage reference has a minimum TC of 2.11 ppm/$^\circ$C. The worst case of TC is 4.80 ppm/$^\circ$C while the supply voltage is 2.2 V.

Fig. 8 shows the $V_{\text{REF}}$ distribution obtained from 200 Monte Carlo analyses, with an average of 1.201 V and a standard deviation of 22.5935 mV. Fig. 9 shows the distribution of TC obtained by 200 Monte Carlo analyses with an average of 16.9337 ppm/$^\circ$C. The layout of the design is shown in Fig. 10 and the active area is approximately 0.1
Table 1 Performance summary and comparison

| Performance parameter | [13] | [22] | [28] | [31] | [32] | This work |
|-----------------------|------|------|------|------|------|-----------|
| Process (µm)          | 0.18 | 0.18 | 0.065| 0.13 | 0.18 | 0.11      |
| Supply Voltage (V)    | 1.2  | 1    | 0.8  | 2.5  | 1.2  | 3.3       |
| $V_{\text{REF}}$ (V)  | 0.766| 0.634| 0.428| 1.183| 0.586| 1.2       |
| Temp. Range (°C)      | 40   | -40  | -40  | -50  | -40  | -40       |
| TC (ppm/°C)           | 4.5  | 3.1  | 5.6  | 1.342| 0.58 | 2.18      |

mm².

Table I is a comparison of the performance of bandgap voltage reference mentioned in different works of literature. The literature [31] does not consider such non-ideal effect such as process corner and mismatch, which will deteriorate its performance when fabrication. Compared with the literature with resistor trimming [32], the digital trimming in this paper has the advantages of simplicity and lower cost. In addition, this paper achieves lower TC in the automotive temperature range of −40°C to 125°C.

4. Conclusion

A high-precision and low-temperature-coefficient bandgap voltage reference is proposed by adding the piecewise temperature compensation and the digital trimming in this paper. The proposed design circuit is based on a 0.11 µm CMOS process. The low TC is achieved with 2.18 ppm/°C from −40°C to 125°C, which can meet the requirement of automotive application. The proposed bandgap reference is 1.2 V, and error is not more than ±5 mV in the worst case simulation of process corners. Results show that the bandgap reference proposed by this paper is very suitable for high-precision circuit applications.

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