Scalable Hash Table for NUMA Systems

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Abstract
Hash tables are used in a plethora of applications, including database operations, DNA sequencing, string searching, and many more. As such, there are many parallelized hash tables targeting multicore, distributed, and accelerator-based systems. We present in this work a multi-GPU hash table implementation that can process keys at a throughput comparable to that of distributed hash tables. Distributed CPU hash tables have received significantly more attention than GPU-based hash tables. We show that a single node with multiple GPUs offers roughly the same performance as a 500–1,000-core CPU-based cluster. Our algorithm’s key component is our use of multiple sparse-graph data structures and binning techniques to build the hash table. As has been shown individually, these components can be written with massive parallelism that is amenable to GPU acceleration. Since we focus on an individual node, we also leverage communication primitives that are typically prohibitive in distributed environments. We show that our new multi-GPU algorithm shares many of the same features of the single GPU algorithm—thus we have efficient collision management capabilities and can deal with a large number of duplicates. We evaluate our algorithm on two multi-GPU compute nodes: 1) an NVIDIA DGX2 server with 16 GPUs and 2) an IBM Power 9 Processor with 6 NVIDIA GPUs. With 32-bit keys, our implementation processes 8B keys per second, comparable to some 500–1,000-core CPU-based clusters and 4× faster than prior single-GPU implementations.

1 Introduction
With applications including k-mer counting in biology [20], sparse matrix multiplication [3], graph triangle counting [21], and inner-join operations [7] [9] [17] [16], hash tables are among the most widely used data structures. Historically, hash tables have been deployed on an extensive set of architectures, from shared-memory with many-cores [6] [18], to massively multi-threaded systems [11], GPU accelerated [13] [15] [20] [21] [12] [2], and up to large scale systems distributed [8] [20] [10]. As accelerator-based computing grows, in particular GPU accelerators, the need for a single-node multiple-accelerator hash table continues to grow. For brevity and simplicity, we will use the term GPU in this paper in the context of our algorithm and use the term accelerator for only the broader-case where a GPU is not applicable.

Multi-GPU systems have advanced to the point they have as much memory as a many shared-memory systems with the benefit of the GPU’s higher throughput. CUDA’s support of unified memory means that having multiple GPUs within a given compute node increases memory size. In the case of an NVIDIA DGX-2 system, with 16 NVIDIA V100 GPUs, each with 32GB of memory, an individual node has 512GB of GPU memory. The IBM POWER9 AC922 system with 6 NVIDIA V100 GPUs can have up to 96GB of GPU memory. These GPU-based systems have an equal amount of memory found in many single-node CPU systems and have computational resources that distributed systems do not have. Specifically, the DGX-2 has NVIDIA’s NVSwitch interconnect, and the IBM Power 9 has NVLink 2nd Generation. These fast interconnects with the addition of unified memory turn these systems into high-speed shared memory systems (despite a resemblance to a distributed system). In this paper, we introduce a scalable hash table for single-node multi-GPU systems with performance comparable to that of 500–1,000-core distributed CPU systems.

While GPU-based implementations are gaining interest and often outperform shared-memory algorithms, GPU implementations are bottlenecked by memory. NVIDIA V100 GPUs, for instance, have 32 GB of high bandwidth memory (HBM2). An NVIDIA RTX8000 has 48GB of GDDR6 memory. Because of this limitation, multi-GPU implementations are necessary for GPU- implementations to process as much data as shared-memory implementations. Single-node multi-GPU hash tables have received some attention lately, such as cuDPP [13], StadiumHash [15], SlabHash [5], and WarpDrive [14]. However, out of all of these, only WarpDrive is multi-GPU. Also, none of those mentioned above, leverage the wealth of work in sparse-graph data structures or binning techniques. Our work is the first to use both sparse-graph structures and sophisticated binning for a multi-GPU hash table, and achieves higher throughput as a result.

Overall, in this paper, our contributions are the

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following.

- We introduce a single-node multi-GPU static hash table implementation with performance comparable to that of small distributed CPU-based clusters. Specifically, our implementation can process $2^{33}$ keys at a rate of 8B keys / second on a DGX-2 system. We accomplish this by extending an existing single-GPU hash table.

- We show that our new algorithm shares many of the key features that the single-GPU algorithm has. This includes a highly efficient collision management technique that copes with a large number of duplicates without a loss in performance.

- We introduce a multi-GPU static hash table implementation that can process 16× more keys than existing single-GPU hash tables. To this end, we leverage work in sparse-graph data structures and binning techniques not previously seen in distributed hash table work, to the best of our knowledge.

2 Background

A hash table maps every element in the input into an integer index using a hash function. These values are placed in the hash-table using a specific set of rules. These rules determine how the hash table behaves and are the primary differentiating factor between hash tables. For example, the hash table rules help determine how to deal with collisions—the case where the input has multiple instances of the same value. These rules are also part of the querying as they determine the correct search pattern within the hash table.

Hash functions map elements (that can be integers, floating points, strings, or complex data-types) to integers. The hash function is typically defined as follows, given an element $e \in A$ the hash of $e$ is:

$$\text{hash}(e) \in \{0, 1, 2, 3, \ldots, n/C\}$$

where $n$ is the number of input elements, and $C$ is known as the load factor. $n/C$ is the hash-range of the input. The underlying assumption of a good hash function is that the probability function of the output follows a good uniform distribution. In simple terms, given two different inputs $a$ and $b$, the likelihood of $\text{hash}(a) = \text{hash}(b)$ is very small. $C$ (a real number) is typically determined by the user with a trade-off between reducing the number of collisions at the cost of increasing the memory footprint.

For example, $C = 0.5$ increases the hash range to be $2 \cdot n$ and lowers chances of collision. In contrast, $C = 0.9$ results in a smaller hash range and an increased chance that two input hash values will collide.

In the remainder of the paper, we use the following terminology. A key, $e$ refers to an element that is pre-hash. A key can be part of the original input or part of the query set. A hashed-value refers to a key that has been hashed and will be denoted by $\text{hash}(e)$. Some hash tables store only the key inside the table while other tables can store a key-value pair. The “value” an extra piece of data associated with the key; for example, it can be the index in the original input array. This is common for “join” operations that require the index.

Collision Management Hash tables have different collision management techniques—with trade-offs from programmability, storage overhead, and computational complexity. In this subsection, we cover several of these in more detail. Many hash tables are an extension of two broad types of hash tables: separate chaining and open-addressing.

Separate Chaining Hash-tables based on the separate chaining collision approach, maintain a chain of keys hashed to a given hash value. Implementations typically use an array of linked lists such that each hash value has its own linked list (which are inherently sequential and limit scalability). Figure 1a depicts this with the long linked list at index 3. The lack of locality also means that memory accesses are random. Also, it doubles the memory footprint as we need to store both the keys and the next pointer in the list.

Open Addressing Many high-performance hash tables are open addressing based. One of the biggest attractions of implementing an open-addressed hash table is its simplicity and portability across architectures. The entire table is stored within a single memory allocation. Specifically, the hash-range is also the hash table size as each hash value can store a single key. If the desired hash value is already in use, then the following entries in the hash table are scanned until an empty entry is found. Open-addressing based methods fall short when the number of duplicates is high or when a large number of keys get hashed to the same hash value or vicinity. The cost of adding duplicate hash values grows at a quadratic rate with the number of duplicates. Figure 1b depicts this, as inserting any key that hashes to 2 requires traversing the keys with hash values 2 and 3.

Other Hash Tables Other collision management techniques include 2-choice hashing [1], and cuckoo hashing [22]t, and HashGraph [12].

Static vs. Dynamic Hash Tables On top of collision management techniques, hash tables can also be categorized as static or dynamic. In static hash tables, the entire set of input keys is specified upfront. After building the hash table with these input keys, users can look up the values in this set, but they cannot add any additional keys or remove existing ones. Dynamic hash tables contrast this by permitting insertions and deletions after building the hash table. In this work, we focus on static hash tables, though our methods can be extended to the dynamic case.

Parallel Hash Tables The need for fast and scalable hash tables in a plethora of applications has brought with it an abundance of parallel hash tables designed
for multi-threaded, massively multi-threaded, and distributed systems. Performance for these hash tables is typically given with a throughput metric such as the number of keys per second. Initially, many had worked on multicore CPU implementations of hash tables \([9, 18, 11]\). These implementations were designed for systems with a few hundred threads at most. These hash tables tend not to scale to larger thread counts due to the use of a large amount of memory per thread or dependent on having large private caches.

For instance, Maier et al. \([18]\) propose the “Folklore” CPU-based hash table, which can build a table with roughly 300 million keys per second. Balkesen et al. \([6]\) also developed a CPU-based hash table, one that can build a table at a rate of 450 million keys per second. Goodman et al. \([11]\) introduce CPU-based hashing strategies for the Cray XMT, which build at a table at roughly 250 million keys per second. All of these tables, however, do not provide the performance that distributed or accelerator-based implementation offers. Barthels et al. \([8]\) introduce two distributed inner-join algorithms, with the fastest running at roughly 48 billion keys per second on 4096 cores.

Hash-tables implementation for the GPU are very different than their CPU counterparts. Specifically, modern-day GPUs requires some 40k threads to keep the system fully utilized. This large thread count requires taking a very different approach as it is not possible to maintain a large amount of algorithmic state per thread. Another differentiating feature between CPUs and GPUs is that GPUs offer very efficient atomic operations.

For example, GPU based hash tables can build at a rate of over 1 billion keys per second on similar generation architectures. This includes the following hash tables: cuDPP \([13]\), StadiumHash \([15]\), SlabHash \([5]\), WarpDrive \([14]\), HashGraph \([12]\). Moreover, while all these hash tables are faster than CPU based hash tables, they each take a very different approach in building the hash table. cuDPP uses Cuckoo hashing \([19]\) to manage collisions. In the case of a collision, Cuckoo hashing will move the older value to a different place in the table (after rehashing) and store the new value in its place. Cuckoo is very useful when the input follows a uniform distribution, and there are few collisions. StadiumHash is also Cuckoo based and targets large tables that do not fit inside the physical memory of the system. WarpDrive is another recent GPU-based hash table that has both single GPU and multi-GPU implementations. The multi-GPU implementation used a multi-split to ensure good scalability. WarpDrive, unfortunately, does not permit duplicate keys in the input.

HashGraph by Green is a static hash table that uniquely treats hash tables as bipartite graphs \([12]\) where the two vertex sets are the keys and their corresponding hash values. With this problem formulation, Green shows an approach for building the hash table in a cache friendly manner. In contrast to open-addressing based tables, HashGraph avoids the extra work of finding an empty spot in the case of a collision. Altogether, HashGraph outperforms all the aforementioned GPU-based hash tables on a single GPU. Lastly, in contrast to many hash tables, HashGraph can cope with a huge number of collisions without losing performance – we too build off this feature an ensure that our multi-GPU algorithm can deal with a large number of duplicates.

3 Multi-GPU HashGraph

In this section, we introduce our new multi-GPU algorithm. Our new algorithm is based on the HashGraph formulation, as discussed by Green \([12]\). To fully understand our new multi-GPU algorithm, we cover the single-GPU version of HashGraph in the following subsections 3.1. After defining the terminology used by HashGraph, we will extend the single-GPU algorithm to multi-GPU in subsections. Our introduction of the single-GPU HashGraph is brief and covers the relevant details. We refer the reader to Green \([12]\) for additional details.

3.1 Single-GPU HashGraph

Green \([12]\) shows a new process for building a hash table by using a sparse graph data structure, namely compressed sparse row (CSR). The HashGraph formulation shows that building a hash table is similar to storing it in a sparse bipartite graph. In Figure 2 we show an example bipartite graph representation of keys and their hash values, along with the graph’s CSR representation.

In the following subsections, we explain how to build a single-GPU HashGraph, yet we prelude by stating that HashGraph’s uses an efficient collision management methodology. Rather than placing the element into the hash table in a single pass over the input data, HashGraph uses a sequence of parallel for loops to count the number of instances of hashed inputs into each hash value.
value. With the number of instances for each hash value, a varying size memory-bin is set aside for each hash value. This process of determining the bin sizes uses a prefix sum operation similar to the offset calculation required by a CSR representation. After the allocation process, it is possible to efficiently place elements into the hash table using an additional pass over the input. The amortized cost for adding each item into the hash table is $O(1)$ regardless of the number of duplicates. HashGraph offers excellent performance when the number of copies in the hash table is high.

Green [12] shows two algorithms for building HashGraph: 1) a naive algorithm that offers intuition and 2) a highly efficient algorithm that uses caching and binning to reduce the number of random memory accesses. In our multi-GPU HashGraph algorithm, we extend the formulation of the second single-GPU Hash graph algorithm. We chose this algorithm as the binning strategy offers a good starting point for scaling our hash table to multi-GPUs. We use a similar binning strategy, though, the purpose of our binning is different than the one used by Green [12].

Compressed-Sparse Row CSR is a well-known data structure used to represent sparse graphs and matrices. For the sake of completeness, we offer the following brief description of CSR. A CSR data structure typically consists of two arrays. The lengths of these arrays are respectively $n$ and $m$ (or $|V|$ and $|E|$). $n$ is the number of rows in the matrix or the number of vertices in the graph. $m$ denotes the number of NNZ (number of non-zero elements) in the matrix or the number of edges in the graph. The first array stores the number of nnz for each row. These lengths are stored in a monotonically increasing array - the offset array. The second array stores the actual nnz elements. Through the offset array, it is possible to get the starting and ending point for the nnz elements of a row. Figure 2 illustrates a CSR representation of an example bipartite graph. For discussing HashGraph, we will refer to the first array as offset and the second array as keys.

Building HashGraph At its core, building a HashGraph is just building both the offset (hash values) and keys arrays described above. These are the only two arrays in a CSR representation, so these are the only two arrays in HashGraph. The length of the offset array is the number of possible hash values, i.e. $N/C$, while the length of keys is the number of input keys to the hash table. In this formulation, each index in offset points to the first key in keys that hashes to that index. The last parallel for-loop in Algorithm 1 illustrates describes how values are finally placed in the keys array using the offset array. The atomic instruction ensures that there is no collision for that specific entry.

3.2 Efficient HashGraph with Bin Counting and its Application to Multi-GPU HashGraph In this subsection, we describe the second and more efficient HashGraph. Our multi-GPU HashGraph uses many concepts of this algorithm for preparing data for communication. Though we use them in a slightly different manner. The cost of random memory access is well-known for hash tables and has received significant attention. With Algorithm 1 accessing an array at index $H_A[i]$ is effectively a random access, as $H_A[i]$ can vary widely depending on the hash function.

The efficient algorithm for HashGraph, first reorganizes $H_A$ so hash values generally lie near similar hash values, and then builds the hash table. To do this in a cache-friendly manner, Green [12] first assigns each hash value to one of $B_L$ bins based on $H_A[i]/BinSize$ and then the hash values in order across all bins back into $H_A$. Here, $B_L$ is small enough to fit in the cache. All the phases of HashGraph use a single shared data-structure used by all threads. Using similar concepts, we extend this to multiple-GPUs.

3.3 Building Multi-GPU HashGraph At a high-level, multi-GPU HashGraph has a HashGraph per GPU for a subset of the hash values. Each GPU has an associated hash range, and that accelerator’s HashGraph only stores keys with hashes within that range. Ideally, we want the number of keys on each device to be roughly equal for proper load balancing and storage utilization,

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**Algorithm 1** Single-GPU HashGraph Build. Note $V = N/C$ [12]

1: parallel for $i = 0, \ldots, N − 1$
2: \hspace{1em} $H_A[i] = hash(A[i]) \mod V$
3: parallel for $i = 0, \ldots, V − 1$
4: \hspace{1em} $CounterArray[i] = 0$
5: parallel for $i = 0, \ldots, N − 1$
6: \hspace{1em} $AtomicAdd(CounterArray,H_A[i],1)$
7: \hspace{1em} $offset = PrefixSum(CounterArray)$
8: \hspace{1em} parallel for $i = 0, \ldots, V − 1$
9: \hspace{2em} $CounterArray[i] = 0$
10: \hspace{1em} parallel for $i = 0, \ldots, N − 1$
11: \hspace{2em} $pos = AtomicAdd(CounterArray,H_A[i],1)$
12: \hspace{1em} $keys[pos + offset][H_A[i]] = A[i]$
Algorithm 2 Multi-GPU HashGraph Build. Note $V = N_d/C$

1: parallel for $d = 0, \ldots, \text{DEVICES} - 1$ do \hspace{1cm} \triangleright \text{Phase 1 - Data Partitioning}
2: \hspace{1cm} parallel for $i = 0, \ldots, N_d - 1$ do
3: \hspace{2cm} $H_A[i] = \text{hash}(A[i]) \mod V$
4: \hspace{1cm} parallel for $i = 0, \ldots, N_d - 1$ do
5: \hspace{2cm} bin = $H_A[i] / \text{BinSize}$
6: \hspace{2cm} $\text{AtomicAdd}(\text{BinCounter}[bin, 1])$
7: \hspace{1cm} $\text{Reduce}(\text{BinCounter}, 0, \ldots, \text{DEVICES} - 1, 42H)$
8: \hspace{1cm} $\text{BinOffset} = \text{PrefixSum}(\text{BinCounter})$
9: \hspace{1cm} $\text{KeyCount} = \text{BinSize} / \text{DEVICES}$
10: \hspace{1cm} $\text{HighestHash} = \text{KeyCount} \times (d + 1)$
11: \hspace{1cm} $\text{HHId} = \text{BinSearch}(\text{BinOffset}, \text{HighestHash})$
12: \hspace{1cm} $\text{BinSplitId} + 1 = \text{HHId}$
13: \hspace{1cm} $\text{BCast}(\text{BinSplit}, 0, \ldots, \text{DEVICES} - 1, 23D)$
14: \hspace{1cm} $\triangleright \text{Barrier}$
15: \hspace{1cm} parallel for $i = 0, \ldots, N_d - 1$ do
16: \hspace{2cm} $\text{BinSplits} = \text{Search}(H_A[i], \text{BinSplitS})$
17: \hspace{2cm} $\text{AtomicAdd}(\text{BinCounter}[\text{BinSplits}, 1])$
18: \hspace{1cm} $\text{BinOffset} = \text{PrefixSum}(\text{BinCounter})$
19: \hspace{1cm} parallel for $i = 0, \ldots, \text{DEVICES} - 1$ do
20: \hspace{2cm} $\text{BinCounter}[i] = 0$
21: \hspace{1cm} $\text{FinalCounter}[d] = \text{BinCounter}[i]$
22: \hspace{1cm} $\text{FinalOffset} = \text{PrefixSum}(\text{FinalCounter})$
23: \hspace{1cm} $\triangleright \text{Barrier}$
24: \hspace{1cm} $\text{AllToAll}(\text{FinalKeys}, \text{BinCounter}, 23D)$
25: \hspace{1cm} $\triangleright \text{Phase 3 - Data Movement}$
26: \hspace{1cm} $\text{BuildHashGraph}(\text{FinalKeys})$
27: \hspace{1cm} $\triangleright \text{Phase 4 - HashGraph Creation}$
28: \hspace{1cm} $\text{PrintResult}()$
29: \hspace{1cm} $\triangleright \text{Print Result}$

Phase 1: Multi-GPU Data Partitioning. Our first goal is to partition the data across the multi-GPUs such that each GPU will be responsible for a near equal number of elements. To do this, we divide the hash range, $HR$, into $BINS_G$ sub-ranges. Each sub-range is a consecutive set of hash values and roughly covers $HR / BINS_G$ hash values. In most cases $HR = c \cdot N$, where $c$ is in $[0.5, 2]$. $BINS_G$ is a tunable parameter. Choosing a small number of bins will lead to the bins having a large number of elements and make the partitioning harder (assuming a uniform distribution). Selecting a large number of bins will increase the memory footprint (as discussed above). We have found that setting $BINS_G O(\sqrt{HR})$ does a good job in trading off the bin sizes, the number of elements in the bin, and the memory footprint.

After setting the value for $BINS_G$, each GPU creates an array of counters to count the number of instances per bin. In a first step, the counters’ values get set to zero. Then each input within a given is hashed, and
the counter for its respective bin is incremented. When this process has completed, each GPU has a distribution of values within the counters. This distribution is coarse grain and is for elements that fall into the same bin and not for the same hash-values. Also worth noting is that even if duplicates do exist, it is improbable that a single bin will be the target of all the duplicates. If it is the target of all the duplicates, then most traditional parallel and distributed hash tables will face the same type of challenges as our hash table; but ours is likely to perform better because of our collision management.

In the next phase, each GPU computes the prefix of the counters. An all-to-all (global) prefix sum operation across all GPUs follows the local prefix computation. With the global prefix sum array, we now have the distribution of values across the entire input. Recall that $BINS_G > DEVICES$. Our goal is to ensure that each GPU will receive roughly $\frac{N}{DEVICES}$ input keys. Thus, each rank, $r$, will compute two binary searches in the global prefix sum array: $r \cdot \frac{N}{DEVICES}$ and $(r + 1) \cdot \frac{N}{DEVICES}$. The entries found in the prefix sum array will enable defining the boundaries of the hash-ranges per rank.

**Phase 2: Data Reorganization Per GPU** With the sub-ranges each device will iterate over its data an additional time and count how many instances fall into each of the new sub-ranges (the number of sub-ranges is equal to the number of devices). Note that this phase also uses a prefix sum operation to create consecutive memory partitions for each device. These partitions will enable an efficient all-to-all communication phase where each device can share the relevant inputs with the remaining device—each device will send one message to all the other remaining devices. The prefix operation in this phase is an array of length $DEVICES$, and its overhead is relatively small compared to other parts of the computation. Each device will now reorganize the input into $DEVICES$ partitions. The values in the new partitions are not organized in any particular order. All we know about the values in the same partition is that these will be transferred to the same device for the hash graph creation.

**Phase 3: Distributing keys to correct devices** In this phase, the keys are sent to the device responsible for their specific hash-range. This is equivalent to an all-to-all communication step and can be easily done because we stored keys per device with CSR. When this has completed, each device will have all the input values that fall into the hash range under its responsibility.

**Phase 4: Instantiating HashGraph per device** After the all-to-all communication, each device has the correct set of keys per the device’s hash range. We can now instantiate a single-GPU HashGraph with these keys. Together, each HashGraph across all devices forms the distributed HashGraph.

**Querying Single-GPU HashGraph** HashGraph can be queried in the same manner as any other hash table. The uniqueness of the HashGraph data structure has brought with it a new querying process. The query-set is the second set of values such that for each entry in the query set, we want to know if that value exists in the first set. A typical assumption is that the first set has been placed in a hash table (if not, a hash table for the first set is constructed). Now, each value in the query set gets hashed, and the hash table gets scanned for that value.

We will first describe single-GPU HashGraph briefly, and then discuss how to extend this algorithm to the multi-GPU setting.

For a single-GPU HashGraph, querying the hash-graph is a simple two step process for querying. Build a HashGraph for the query set. Given two HashGraphs, we can perform list intersections between the corresponding lists of the two hash tables $HG_{1,i}$ with $HG_{2,i}$. Due to the simplicity of HashGraph, we know exactly which keys hash to a particular value $i$ by iterating from $keys[offset[i]]$ to $keys[offset[i] + 1]$. This is especially efficient as the number of random memory accesses is reduced, the is cache re-use, and only the relevant elements are scanned. Green [12] shows that this is especially efficient when there the average number of elements per list is greater than 4 (a reasonable number). HashGraph continues to outperform existing hash tables as the number of duplicates grows. Lastly, note that each set intersection is independent of other intersections as there is no overlap between the lists, so running all the intersections is embarrassingly parallel and straightforward.

**Querying Multi-GPU HashGraph** Querying multi-GPU HashGraphs is a natural extension of querying single-GPU HashGraphs. Similar to the single GPU algorithm, our multi-GPU querying algorithm consists of two steps: 1) build a multi-GPU HashGraph from the query keys and 2) run the intersections across all the GPUs.

It is crucial to note that both HashGraphs, input and query set, share the same hash range on each device. After building these HashGraphs, we simply run set intersections on each single-GPU HashGraph in the same way described in 3.3

### 3.4 Complexity Analysis

**Work Complexity** For this subsection, let $N$ be the average number of keys per device, and $P$ be the total number of devices. Note that the total number of processed keys is thus $NP$. The bottleneck of Algorithm 2 are lines 19 – 21 and 27 – 30, as these are for-loops that call a Search function. In our implementation, Search is a linear search across all processes and has $O(P)$ work. Since the outermost for-loop has $O(P)$ work, the inner for-loop has $O(N)$ work, and the Search function has $O(P)$ work, the overall work complexity is
4.1 Systems and Configuration In this subsection, we discuss the different systems we use to evaluate our implementation. We target NVIDIA V100 (Volta) GPUs for our implementation. We also focus on two general systems: The NVIDIA DGX2 and the IBM POWER9 AC922 system.

Volta GPUs The V100 is a Volta (micro-architecture) based GPU with 80 SMs and 64 SPs per SM, for a total of 5120 SPs (lightweight hardware threads). In practice, roughly 40K software threads are necessary for fully utilizing the GPU. The V100 has a total of 32GB of HBM2 memory and 6MB of shared-cache between the SMs. Each SM also has a configurable shared memory of 96KB. The V100 has two form factors: PCI-E and SXM. PCI-E is the default form factor found in most consumer GPUs. The SXM form factor is equivalent to placing a GPU on a board. The SXM form factor has multiple NVLink channels allowing GPUs to communicate with other multiple GPUs concurrently at a higher than PCI-E. The SXM form factor GPU is known for outperforming its PCI-E counterpart due to increased frequency and power consumption. The V100 in NVIDIA’s DGX-2 and IBM AC922 are slightly different. In the DGX-2 the NVIDIA V100 are the SXM3 form factors and have a peak power consumption of 350 watts. In the IBM AC922 the NVIDIA V100 are the SXM2 form factors and have a peak power consumption of 300 watts.

DGX-2 The NVIDIA DGX2 server is a single node server with sixteen V100 GPUs. The DGX2 server was the server to introduce NVSwitch. NVSwitch enables communication from each to GPU to all the remaining GPUs for a total of 300GB/s of bandwidth. Each GPU has six incoming and outgoing links at 25GB/s (each). Thus, a GPU can send and receive 150GB/s concurrently. The fully connected network also ensures that the latency between the varying communication paths is uniform in length. The true benefit of NVSwitch over existing interconnects is the fact the on-device bandwidth and off-device bandwidth are within an order of magnitude of each other. This ensures that the communication within a DGX-2 is fairly balanced. Ang et al. [?] give a detailed performance analysis of NVSwitch and NVLink. The DGX-2 also has a high-end CPU processor, an Intel Xeon Platinum 8168 processor with 48 cores and 96 threads. The DGX-2 used in our experiments has 1.5TB of DRAM memory.

IBM POWER9 AC922 The IBM AC922 is a single node server with two POWER9 22C CPUs and six V100 GPUs. Each of the V100s on the AC922 has 16GB of memory, in contrast to the GPUs on the DGX2 which have 32GB of memory. These devices are divided equally between two sockets for one CPU and three GPUs per socket. Within each socket, the three GPUs are connected to each other and to the CPU via NVLink 2.0, which has 100GB/s total bidirectional bandwidth between two devices. Between sockets, the AC922 uses IBM’s X-bus as its interconnect, with a 64GB/s bandwidth. The AC922 also uses two POWER9 processors (one per socket) for a 36 cores with 4-way SMT. The node also has 96GB of HBM2 memory and 512GB of DDR4 RAM.

4.2 Input Sizes and Key Distribution We focus on 32-bit keys in our implementation. Our input keys for each experiment fall in the range \(\{1, \ldots, 2^k\}\). The precise value of \(k\) depends on the experiment and is discussed in detail in Sec. 4.3. In all of our experiments, we use the Murmur hash function. Both single-GPU HashGraph and WarpDrive use Murmur hash.

4.3 Experiments Performed In this section, we outline each of the different experiments we run along with the frameworks we compare against. For each experiment, we evaluate our implementation based on throughput, i.e. keys/sec. This metric is the standard for evaluation in previous work [2][4][8]. Note that for almost all of our experiments, we choose \(C = 1\). That is, our table size is equal to the number of input keys. This is only false when we have over \(2^{32}\) input keys, as our table size is always 32-bit. In these cases, we have a table size of \(2^{31}\).

Weak Scaling We run weak scaling experiments to evaluate scalability, where we fix \(N_d\) and observe how throughput changes with device count. The value of \(N_d\) depends on the system. The V100s on the DGX2 have a greater memory capacity than the V100s on the AC922, allowing for larger experiments. Our strong scaling results showed similar performance to our weak scaling results, but are omitted for brevity.

Random vs. Sequential Keys Consistent with single-GPU HashGraph, we run experiments where our input keys are sequential. That is, for these experiments,
we build a hash table with the keys \(\{1, \ldots, 2^k\}\) for some \(k\). We also evaluate multi-GPU HashGraph on randomly generated key sets. In these experiments, we randomly sample with replacement \(2^k\) keys from the set \(\{1, \ldots, 2^k\}\).

**Build vs. Querying** We show scaling experiments for both building a multi-GPU HashGraph given an input array \(A\) along with querying a hash table with a query array. In each of our experiments, the number of query keys equals the number of inputs keys. Recall that querying a multi-GPU HashGraph, once the HashGraph of input keys is constructed, is two phases. First, we build a multi-GPU HashGraph from the query keys, followed by a series of list intersections.

**Duplicate Keys** We also evaluate multi-GPU HashGraph with duplicate keys. To that end, we vary the global hash range for our Murmur hash function while fixing the overall key count and GPU count. We adjust the hash range simply by adjusting \(V\), the value used in the modulus on line 4 in Alg. 2. When adjusting our hash range, the average number of occurrences for any key is simply the ratio of key count of length of the hash range.

### 5 Performance Analysis

#### 5.1 Weak Scaling

The results of our weak scaling performance experiments are depicted in Fig. 3. The build operations shows good scalability on both the DGX-2 and the AC922. On the DGX-2 the build operation starts at about 1.5B keys/sec and scales up to slightly over 6B keys/sec and 8B keys/sec, for 8 GPUs and 16 GPUs, respectively. That is an equivalent for a 4\(\times\) and 6\(\times\) speedup over one GPU using our algorithm. The single GPU HashGraph [12] is able to perform at roughly 2.3B keys/sec. The reduction in performance of our new algorithm in comparison to the single-GPU algorithm is due to the second round of binning which requires random memory accesses. Altogether, the overhead of moving from a single-node algorithm to multi-node algorithm is not considerably high and accounts for about 35%.

Lastly, our implementation uses CUDA’s unified managed memory. We chose managed memory over unmanaged memory to avoid the cost of memory allocations during the execution of our algorithm. In our benchmarking, we saw allocating memory during execution led to inconsistent throughput. In contrast, managed memory gave fairly consistent performance at the cost of some performance where the GPU’s runtime is responsible for fetching pages and moving them across devices. We include these runtime penalties in the times we report but note that these penalties account for some of the reduced speedups when going from 8 GPUs to 16 GPUs on the DGX-2.

**Phase Breakdown** Fig. 3 depicts the breakdown of the four key phases four building our hash-table. 1) **Partitioning** determines the hash range for each device (Phase 1 in Alg. 2) 2) **Pre-processing** reorganizes keys on each device into a CSR based on each key’s destination GPU (Phase 2 in Alg. 2) 3) **All-to-All** the all-to-all communication (Phase 3 in Alg. 2) 4) **Table Construction** builds the individual HashGraphs on each device (Phase 4 in Alg. 2). This is a weak scaling for 2\(^{29}\) and 2\(^{28}\) keys per GPU on DGX2 IBM, respectively.

For both servers, the relative cost of the communication increases with the number of GPUs. However, the cause of the increase is for different reasons. As the all-to-all communication has \(O(P^2)\) cost, going from 8 GPUs to 16 GPUs increases the number of messages by roughly 4\(\times\), while the average message decreases by 2\(\times\), the latency increases. NVIDIA’s DGX-2 has NVSwitch which enables direct communication between all the GPUs. In contrast, the IBM AC922 requires that GPUs connected to the different CPU processors transfer date over NVLink and across the CPUs. This greatly reduces the all-to-all communication and explains why at 4 GPUs the relative cost of the communication for the AC922 is higher. The increase from 4 GPUs to 6 GPUs on the AC922 is not that high as the bottleneck does not change. Lastly, we note that the cost of the preprocessing phase seems to grow with the number of GPUs. This seems to be an artifact of our implementation in how we place elements in bins. We plan on investigating other approaches for making this phase less expensive.

**State-of-the-Art Comparison** With our new algorithm, we see a build throughput of roughly 8B keys/sec on DGX2 and 5B keys/sec on the IBM AC922. Note that Barthels et. al [8] report having 10B keys/sec when using 1024 cores on their distributed inner-join algorithm. They also report an 8B keys/sec throughput with 512 cores, comparable to our throughput with Murmur hashing. In place of using a distributed cluster, multi-GPU HashGraph is able to achieve comparable throughput on a single DGX2 server. We can do so through a combination of 1) leveraging V100 accelerators on DGX2 with massive parallelism and 2) using communication primitives (e.g. all-to-all) that are typically prohibitively expensive for distributed settings, and 3) utilize NVIDIA’s NVSwitch for fast data transfers. Lastly, we note that we did not compare our algorithm to WarpDrive [14] as its multi-GPU is not available. The single-GPU version of HashGraph outperforms WarpDrive.

#### 5.2 Strong Scaling

Our strong scaling results exhibit the same performance trends as does our weak scaling, for the sake of brevity we do not show these duplicate plots. We do note that similar to weak scaling, we are able to test larger inputs on the NVIDIA DGX-2 due to the increased number of GPUs in comparison to the IBM AC922 and the difference in device memory between these two NVIDIA V100 GPUs.
store two HashGraphs, we could not build the same size building phase as it is one of two phases. As we need to then doing a large number of set intersections. Thus, consists of two phases, building a second HashGraph and our querying matches the performance of the single-GPU algorithm accounts for roughly 10% of the execution time and the rest of the time is spent on building the hash-table for the query set. While the overhead of the building might seem high, there is also some motivation there. If one can speedup the performance of the build,

5.3 Build Vs. Query Overall the performance of our querying matches the performance of the single-GPU algorithm [12]. Recall that our query algorithm consists of two phases, building a second HashGraph and then doing a large number of set intersections. Thus, we expect our query algorithm to be slower than the building phase as it is one of two phases. As we need to store two HashGraphs, we could not build the same size hash tables and limited ourselves to hash tables one scale smaller than those used in the build experiments. Similar to the single-GPU algorithm, the intersect phase of the algorithm accounts for roughly 10% of the execution time and the rest of the time is spent on building the hash-table for the query set. While the overhead of the building might seem high, there is also some motivation there. If one can speedup the performance of the build,
the querying will also be faster. While this is obviously desirable, our algorithm on a DGX-2 already performs as well as 512 core CPU system.

5.4 Duplicate Keys One of the nice features of HashGraph is its ability to deal with a large number of collisions created by duplicate keys within the input. Fig. 4 depicts the performance of our new multi-GPU hash-table as a function of the number of times that each key appears in the input. Moving on the x-axis from left to right the number of times that the key appears in the input increases. Note, the build rate is fairly consistent for all duplicate rates, as expected. The query plot has a bit more variation. It starts off with a fairly consistent throughput, until the number of duplicates is roughly $2^2 = 8\times$. From this point onwards, the throughput decreases at a steady rate. This is not surprising as due to duplicates, many lists will have $2^i$ duplicates. As our intersection operation counts the number of time each key appears in the input, we are required to iterate through the entire list. Thus, for each entry in the query set we need to do $2^i$ comparisons. Since the query set also has duplicates and its lists are now longer, the total time per intersection increases in a quadratic manner. Which explains the fast decay in throughput. On a positive note, this matches the trend of the single GPU. The single GPU version was over $100\times$ than other state-of-the-art hash-tables for similar duplicate rates.

6 Conclusions
In this paper, we presented a new algorithm for building a single-node hash table with performance comparable to distributed hash tables. We accomplished this by extending an earlier single-GPU hash table, HashGraph, to the multi-GPU setting. We enhanced single-GPU HashGraph in three ways. First, we extended a binning approach used in single-GPU HashGraph to effectively partition keys between GPUs. Second, used additional sparse-graph data structures to organize keys for proper communication. Lastly, we leveraged communication primitives that are typically prohibitive in distributed settings. We evaluate our algorithm’s performance on two different systems: an NVIDIA DGX-2 server with 16 GPUs, and an IBM AC922 with 6 GPUs. Our algorithm shows promising scalability. In particular, we show that our algorithm can scale to hundreds of thousands of cores available on 16 GPUs. We also showed that the various phases of our new algorithm are scalable and can be executed with hundreds of thousands of threads. Overall, we present a multi-GPU hash table can process $8B$ keys per second, comparable to some CPU-based distributed hash tables with 500 – 1,000 cores.

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