Evaluation of Residual Stress and Warpage of Device Embedded Substrates with Piezo-Resistive Sensor Silicon Chips

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Abstract
The residual stress and warpage of a device embedded substrate (DES) is evaluated using a Si chip including a piezo-resistive sensor. Two types of DESs are fabricated to investigate the effect of substrate structure on residual stress: a device mounted on the surface of a core substrate (core surface mounted type DES) and a device placed inside a through cavity of a core substrate (core cavity type DES). Both DESs have four conductor layers with two build-up ABF (Ajinomoto Build-up Film) layers. For the core cavity type DES, the effect of cavity clearance from 0.15 mm to 1 mm between the core wall and embedded chip is also investigated. The embedded devices are $9 \times 9 \, \text{mm}^2$ piezo-resistive sensor chips of 200 $\mu\text{m}$ in thickness, and the core is adjusted to the Si chip thickness. The residual stress induced from the fabrication process is obtained from measuring the resistance value of the piezo-resistive sensor before and after chip embedding. After measuring the residual stress, the warpage for each type of DES is observed using the shadow moiré interferometry method with the temperature changing from 25°C to 260°C. The relationship between the residual stress and warpage is discussed with respect to the substrate structure symmetry and balance.

Keywords: Device Embedded Substrate, Core Cavity Type, Residual Stress Evaluation, Piezo-resistive Sensor, Warpage

1. Introduction
Device embedded substrates have been attracting considerable industrial interest in the field of portable and wireless electronics because of the small form factor, low power consumption, good electrical performance, and short time-to-market.[1] At present, passive device embedded substrates are under mass production and active device embedded substrates are gradually becoming popular. Since the first active device-embedded substrate, the bumpless build-up layer (BBUL),[2, 3] was reported by Intel, various other types have been reported, including the integrated module board (IMB) by Helsinki University,[4] chip-in-polymer (CiP) by Fraunhofer IZM,[5, 6] the chip-in-substrate package (GiSP) by ITRI,[7] embedded active and passive chip-last (EMAP-CL) by the Georgia Institute of Technology,[8] and others. All these device-embedded substrates reported good signal performance and high reliability; however, challenges remain in their development, including low production yield from process difficulties as well as scaling to finer pitches. These reports placed devices either inside or on the substrate. In packages that bury devices inside the core substrate, like the BBUL, misalignment is the biggest obstacle to scaling down the pad pitch of the embedded active device. This alignment problem can be alleviated by increasing the pad size, but doing so prevents scaling down to a finer pitch. In packages that mount devices on the core substrate, aligning the via to the bond pad is easier, but some problems remain, such as the thinning of Si chips, leveling of epoxy resin without breaking chips, and substrate warpage.[7, 9]

In our previous paper,[10] we demonstrated the fabrication feasibility and reliability of the new core cavity type of device embedded substrate, where the device is embedded inside the through cavity in the core (EiCC). Compared with the core surface mounted type DES, EiCC can more easily produce a thinner device-embedded substrate,
giving EiCC-based devices better form factor and electrical performance than core surface mounted embedded substrates. Moreover, from the concept of EiCC, it is possible to obtain a balanced epoxy resin structure inside a substrate and consequently warpage problem can be solved.

The process induced residual stress is closely related to the warpage and reliability of IC packages and substrates. By evaluating the residual stress, it is possible to optimize the material and structure design of a package for good reliability and low warpage. The residual stress evaluation of IC packages has generally been conducted using finite element method (FEM) simulation,[11–13] nevertheless the FEM simulation is not correct enough to evaluate a large complicated structure exactly and is time-consuming. Consequently, several studies on real measurement of residual stress using a piezo-resistive sensor embedded Si chip have been reported.[14–16] The piezo-resistive behavior of Si has been studied extensively [17–20] and in a package system, the residual stress evaluation can be determined by measuring the change in resistance before and after the packaging process.

In this paper, the warpage issue of EiCC related to the residual stress will be discussed in detail. Using the piezo-resistive sensor embedded Si chips (STAC TEG-0101JY: WALTS Co., Ltd), we characterized the core cavity type DES in terms of the process residual stress, comparing this to the core surface mounted type DES. For the core cavity type DES, the effect of the cavity clearance between core wall and embedded chip on the residual stress was also investigated. The schematic cross sections of the two types of DESs for residual stress and warpage evaluation are shown in Fig. 1. From the stress measurements and cross-section observations, the relationship between the residual stress and the structure of DES will be investigated. In addition, the effect of material properties on the residual stress results will be discussed. Finally, after observing the warpage of each type of DES using the shadow moiré interferometry method, the mechanism of the warpage performance under the as-received state and the elevated temperature circumstance will be discussed in depth with the residual stress evaluation results.

### 2. Experimental Details

The fabrication process flows of two types of DES, that is, the core surface mounting type and the core cavity type, are shown in Fig. 2. For both types of DES, fabrication begins with a 200-μm-thick FR4 core (MCL-M-679FG, Hitachi Chemicals, Japan) of 510 × 407 mm². First, through holes (THs) for alignment were mechanically drilled. After drilling, the core substrates were desmeared using KMnO₄ alkali chemical etching, and the patterning of the core layer followed (layers 2 and 3). Using a router, through cavities (core cavity type only) were then drilled to make clearances of 150 μm, 300 μm, 500 μm and 1 mm on all four sides to prevent direct contact between the embedded device and core substrate. After the cavity machining, the core substrate was divided into four panels, each 250 × 190 mm, for post-processing. Every process panel had 24 pieces of DESs and each of them is 27 × 27 mm² size. Afterwards, the debris from machining were chemically removed and the Cu surface was roughened by chemical treatment.

After completing the core layer, the piezo-resistive sensor Si chip was mounted face-up on the core surface using non-conductive paste (EN-4900GC Hitachi Chemical) for the surface mounting type. For the core cavity type, after a temporary adhesive tape, which was a 25 μm thick polyimide film with a 6 μm adhesive layer (TRM 6250L, Nitto Denko, Japan), was laminated onto the top surface (layer 2) of the core, the Si chip was mounted face-down on it. The schematic image of the piezo-resistive sensor chip is shown in Fig. 3 together with the bump/pad structure of the chip. The Si chip was 9 × 9 mm² size and consisted of nine unit chips of 3 × 3 mm² size, where each chip had two piezo-resistive sensors formed in the x- and y-directions located in the chip center (red color) and a corner (blue...
color). The positions to be measured at the package level were identified from A to H and the other piezo-resistive sensors were omitted in Fig. 3. Each position of A to H has different distance from chip center and the residual stress variations as a function of the distance from chip center can be evaluated. The distances from chip center to several main positions are like as followings; A: 0.289 mm, B: 1.153 mm, E: 1.847 mm, C: 3.289 mm, and D: 4.153 mm.
The pad/bump structure of the chip was a 20 μm thick Cu bump with Φ100 μm formed on the 70 μm pad opening. The chips were carefully ground down to 200 μm thickness taking care not to induce electrostatic damage on the piezo-resistive sensors. The chips were mounted using a flip-chip bonder (MD3500, Toray Engineering, Japan) with a placement accuracy of ±5 μm. Before mounting, the resistance values of each piezo-resistive sensor of each chip were measured using the four point measurement method.

After mounting the chips, a two-layer structure of ABF (build-up resin: GX92K (10 μm) and filling resin: TH3L3 (50 μm)) was laminated. In the case of the core surface mounted type DES, both sides of the core were laminated simultaneously with a dielectric epoxy resin (Ajinomoto, ABF 60 μm). However, in the case of the core cavity type DES, the epoxy resin was sequentially laminated from one side (back, layer 3) of the substrate core. The ABF laminating was accomplished in two steps: vacuum laminating (resin filling without voids) and atmosphere pressing (surface leveling). The laminated substrate was then pre-cured at 120°C for 0.5 h in an atmosphere oven. The temporary adhesion tape was then peeled off, and the sample treated with oxygen plasma for 180 s to remove any remaining adhesive. To form a symmetric built-up resin structure, the plasma-treated side (layer 2) was laminated with the same epoxy structure as layer 3. After both sides of the core substrate were laminated, the epoxy resin was cured at 180°C for 1 h. For the core cavity type DES, both sides of the laminated core substrate showed good surface planarity without any dimples around the cavity clearance.

Laser via drilling was accomplished using a Hitachi Via Mechanics UV-CO₂ combined laser drilling machine. The UV laser (355 nm wavelength, 50 KHz YVO₄ laser) was used to obtain vias with a diameter of 50 μm (maximum size of the via) on 100 μm Cu UBM (under bump metallurgy). To drill the designed via diameters, the pulse power was manipulated by 4.7 W with a mask size of 1.45 mm. To prevent the target via size from increasing because of the heating effect, the laser drilling was performed using a cycling mode, that is, the 28 shots were implemented with 4 burst shots repeated for 7 cycles. Laser drilling often leaves undesirable byproducts known as smear. To remove smear from the bottom of the via and its surroundings, we used the conventional desmearing technique using a KMnO₄ alkali chemical solution.

After desmearing, we performed via filling and Cu trace patterning. This was a semi-additive process with the following steps: the Cu seed layer was grown to a target thickness of 1 μm for 45 min at 27°C using an ATS ADDCOPPER IW (OKUNO Chemical Industries, Japan) colloid including Pd/Sn catalysts. Patterns were formed using negative type dry film (DF) photoresist (RD1225, Hitachi chemicals, Japan) lamination and photolithogra-
phy. After that Cu electroplating for one hour with a DC current density of 1.5 A/dm² grew the 20-μm-thick plated Cu layer. The composition of the copper electroplating solution was 200 g/L CuSO₄ 5H₂O, 50 g/L H₂SO₄ and 50 mg/L HCl. The commercial additives TOP LUCINA α (OKUNO Chemical Industries, Japan) were also added to the plating solution. The DF resist lift-off and seed layer etching process then followed. A solder mask was then laminated using a film of solder resist (SR; PFR-800, AUS410 Taiyo Ink), and Ni/Au was electrolytically plated on the electrode pads.

Each completed substrate was separated into a test unit, and the resistance value of each piezo-resistive sensor was measured again. Figure 4 shows a schematic image of the first Cu wiring layer after DES completion. The resistance of each piezo-resistive sensor at package level was measured using four-point measurement method. The initial resistance value of the piezo-resistive sensor used in this study is around 25 kΩ and the resistance variation by residual stress is up to several hundreds Ω. The residual stress was calculated from the measured resistance value using the following equation:

$$\sigma_T = \frac{1}{S} \left[ \frac{R_{1T} - R_{0T}}{R_{0T}} + \beta_1 (T_1 - T_0) + \beta_2 (T_1^2 - T_0^2) \right], \quad (1)$$

where, $R_o$ is the initial resistance, i.e., resistance at the chip level, $R_I$ the resistance after embedded substrate completion, $S$ stress sensitivity, and $\sigma$ the stress in MPa unit. Because the resistance and sensitivity were very sensitive to the measurement environment, such as the temperature and light, the measurement was carried out in a dark room controlled at a constant temperature. The stress sensitivity at the temperature of 30°C ($T_0$) was assumed as -0.001399 (−) symbol is for p-type Si) based on the chip supplier’s calibration results. The stress value measured at different temperatures ($T_1$) was obtained by the following equation:

$$\sigma_T = \frac{1}{S} \left[ \frac{R_{1T} - R_{0T}}{R_{0T}} + \beta_1 (T_1 - T_0) + \beta_2 (T_1^2 - T_0^2) \right], \quad (2)$$

where, $\beta_1$ and $\beta_2$ are temperature dependent correction factors of a piezo-resistance and $\beta_1$ is 1.57E-3/°C and $\beta_2$ is -9.41E-8/°C².

After the stress measurement, the structural analysis at the center and sides of the Si chip was conducted through cross section observation. Finally, the warpage of each sample was investigated using shadow moiré interferometry with the temperature changing between the room temperature and the 260°C solder reflow temperature.

3. Results and Discussions

3.1 Residual stress evaluation

Figure 5 shows the measurement results for the residual stress in each type of device embedded substrate. As shown in Fig. 5, the core surface mounted type DES shows the high tensile stress (about 100 MPa) in the center and the stress magnitude decreases to around 20 MPa on moving outward from the chip center. Whereas, the core cavity type DES shows the small compressive stress between 10 MPa (at the chip center) and 30 MPa (at the chip edge). The large difference between the x- and y-directions was not observed for both types of DESs.

The process induced stress is well known as being
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occurred from the mismatch in the coefficient of thermal expansion (CTE) among the materials. The thermal loading, in this fabrication, was the result of the temperature difference between the plated Cu annealing temperature (180°C) and the room temperature of 25°C. The mismatches of CTE between the core and the ABF and/or the embedded Si chip and the ABF are considered the main reasons for the thermal stress. The representative material’s relevant properties are summarized in Table 1. For a core surface mounted type DES, the high tensile stress at the chip center area is explained easily by the lateral and vertical imbalance of the substrate structure. That is, the ABF thickness in the lateral direction is significantly different on the Si chip and on the core substrate surrounding it. Moreover, the structure in the vertical direction is different on the top and bottom of the Si chip. The ABF on the top of the chip was only 60 μm thick, whereas the bottom of the chip consisted of various materials, such as a 7 μm thick paste layer, a 200 μm core with two 18 μm Cu layers, and a 160 μm ABF layer. The thickness of each layer was established from the cross section as shown in Fig. 6(a). With the cooling from the Cu annealing temperature, shrinkage of the ABF on the bottom layer of the core was severe but on the upper layer of the core, because of the small quantity of ABF and Si chip stuck to the core, the shrinkage was restricted. This, consequently, induced

| Material          | Thermal expansion coefficient (α-CTE) | Young’s modulus (GPa) | Thickness (μm) | Glass transition temperature $T_g$ (°C) |
|-------------------|--------------------------------------|-----------------------|----------------|----------------------------------------|
| Si*               | 3                                    | 107                   | 200            | –                                      |
| Cu*               | 16.7                                 | 124                   | 18             | –                                      |
| FR4 core**        | X-Y < 120°C; 13-15                    | 25                    | 200            | 175 (TMA)                             |
| MCL-E-679FG       | Z < $T_g$; 22-33                      |                       |                |                                        |
| Hitachi Chemical  | Z > $T_g$; 140-170                    |                       |                |                                        |
| ABF**             | 21 < $T_g$                           | 7.9                   | 50             | 156 (TMA)                             |
| Ajinomoto fine Tech | 74 > $T_g$                         |                       |                |                                        |
| SR**              | 60                                   | 3.2                   | 25             | 105 (TMA)                             |
| PFR-800, AUS410   | 60                                   | 3.2                   | 25             | 105 (TMA)                             |
| Taiyo Ink         |                                      |                       |                |                                        |
| Non-conductive    | 57                                   | 0.73                  | 10             | 21 (TMA)                              |
| Paste**           |                                      |                       |                |                                        |
| EN-4900GC         |                                      |                       |                |                                        |
| Hitachi Chemical  |                                      |                       |                |                                        |

* The Electronic Packaging Handbook edited by Glenn R. Blackwell; CRC Press
** From company catalogs and technical reports

![Fig. 6 Cross-section images of the core surface mounted type (a) and core cavity type (b) device embedded substrate. The cross-section observation line is designated on Fig. 3.](image)
high tensile stress on the chip surface.

Whereas, for core cavity type DES, the totally different result was obtained because the balanced structure was obtained above and below the chip and the embedded chip was well placed in a parallel position to the core without directly contacting it as shown in Fig. 6(b). The small compressive stress seemed to be induced from the thermal shrinkage difference in ABF resin above and below the embedded Si chip. Considering the difference in the ABF thickness, because the top of the chip was thicker than the bottom, the ABF thermal shrinkage on the top was greater and resulted in the compressive stress on its surface. As explained in the experimental details section, because the epoxy resin was laminated side by side sequentially for the core cavity type DES, the former laminated ABF (backside of the chip) was more able to flow into the cavity clearance more and was thinner than the latter layer. Therefore, the decrease in thickness of the former laminated side was affected by the cavity clearance size, and induced the change in the residual stress in the Si chip. The effect of cavity clearance on the residual stress is shown in Fig. 7. When increasing the dimension of the clearance the residual stress in the chip increased gradually, especially in its center area. The thickness of ABF above and below the chip was obtained from cross-section observation using laser microscope and the results including the thickness difference (Δ) between above and below ABF are summarized in Table 2. As expected, the ABF under the chip became thinner with the increasing cavity clearance dimension. This can be avoided using the thicker ABF film on the former laminated side, but in this study we did not optimize it. Another possible mechanism for the compressive residual stress on the chip might be related to the different thermal histories of the ABF on the top and bottom of the chip. However, because the backside ABF undergoes more only the pre-curing time of 0.5 h at 120°C below

![Graph showing measured residual stresses of various cavity type device embedded substrates with cavity clearances of 0.15 mm, 0.3 mm, 0.5 mm, and 1 mm.](image)

### Table 2

| Type of DES            | Cavity clearance (mm) | ABF thickness (mm) |   |   |   |   |
|------------------------|-----------------------|--------------------|---|---|---|---|
|                        |                       | Left side          | Center | Right side |
|                        |                       | above | below | Δ   | above | below | Δ   | above | below | Δ   |
| Core Surface Mounted   | –                     | 58.0  | 160.0 | ±102.0 | 55.0  | 160.0 | ±105.0 | 60.0  | 160.0 | ±100.0 |
| Type                   | 0.15                  | 63.2  | 56.0  | ±7.2  | 66.0  | 58.4  | ±7.6  | 65.0  | 58.4  | ±6.6  |
|                        | 0.3                   | 72.0  | 46.0  | ±26.0 | 68.7  | 51.2  | ±17.5 | 70.0  | 46.4  | ±23.6 |
|                        | 0.5                   | 70.8  | 44.0  | ±26.8 | 68.0  | 50.8  | ±17.2 | 71.0  | 43.0  | ±28.0 |
|                        | 1.0                   | 72.8  | 38.5  | ±34.3 | 69.4  | 41.9  | ±27.5 | 75.6  | 38.5  | ±37.1 |

Fig. 7 Measured residual stresses of various cavity type device embedded substrates with cavity clearances of 0.15 mm, 0.3 mm, 0.5 mm, and 1 mm.
the $T_g$, the influence of different cure shrinkage might be ignored in this study. Therefore, the thermal shrinkage difference because of the difference in ABF thickness seemed to be dominant and consequently the chip was under the compressive stress on its surface.

For the core cavity type DES, another interesting result was that the stress increased when moving outside the chip in opposite to the surface mounting type. This seemed to be caused by the things that the embedded chip was placed parallel to the core and the cavity clearance was inserted between the core and the embedded chip. That is, being different to the core surface mounted type having large structural imbalance in the vertical direction, the core cavity type DES has the small ABF thickness difference in the direction. Moreover, in the lateral direction, it has three different areas such as ABF/core/ABF structure area, cavity clearance area, and ABF/Si chip/ABF structure area. Therefore, the stress can be higher at the chip edge area near to the ABF/core/ABF structure area which would deform more severely. However, this needs to be studied more to confirm.

So far, we have discussed how the residual stress in the DES can be minimized by realizing a balanced structure and placing the chip inside the core cavity in parallel. This controlled residual stress will decrease the warpage of the substrate, which we will discuss in detail in the next section.

### 3.2 Warpage evaluation

The substrate warpage is typically dependent on the properties of the dielectric materials such as Young’s modulus, CTE, and $T_g$, the layer thickness of each component, and the Cu coverage ratio of each layer. For the device embedded substrate, the warpage can be further affected by the embedded device’s mechanical properties and thickness. Figure 8 shows the warpage data obtained from the shadow moiré interferometry for the two types of device embedded substrates at room temperature before heat treatment. The measurement direction and surface area are shown in Fig. 9 and the chip area and outer wiring area are also designated in the figure. The maximum warpages (the term of “coplanarity” in 3D images) of the core cavity type DES varied from 46 $\mu$m up to 148 $\mu$m depending on the clearance width, and were much smaller than the 238 $\mu$m of the core surface mounted type DES. As shown in Fig. 8, concave contours were observed in contrast to the convex contours of the core surface mounted type DES. To explain the warpage results, we believe that the residual stress induced during fabrication process was the main factor of the substrate warpage which can be easily confirmed from the residual stress data shown in Figs. 5 and 7. That is, we can relate the residual stress curves and properties to the warpage contours and magnitudes. For the core surface mounted type DES, the considerable tensile stress highly concentrated on the embedded chip center area, and the small stress at the chip edge, made the substrate severely warp convexly. Whereas, for the core cavity type DESs, a small compressive stress was observed from 10 MPa at the center to 30 MPa at the chip edge and resulted in the small concave warpage in the chip area. The warpage in the chip area of the core cavity type DES increased with increasing cavity clearance width, similar to the residual stress increasing, as shown in Fig. 7. In the outer wiring area, the different warpage contour compared to the center area, and asymmetric warpage between two diagonal directions, were observed for clearances of 0.15 and 0.3 mm. However, the phenomena disappeared after heat treatment and cooling down back to 30°C as shown in Fig. 10. Figure 10 shows 3-D images of the warpages at the peak temperature of 260°C and at the returned temperature of 30°C. Therefore, these were possibly induced by the small mechanical force added during the fabrication process.

The variation in warpage with temperature was also investigated. Figure 11 shows the temperature dependent warpage variation of various DESs. The temperature increased from 30°C to 260°C (Pb-free reflowing temperature) and then back to 30°C. For the core surface mounted type DES, the warpage decreased with increasing temperature and at around 150°C changed from convex (Fig. 8(a)) to concave warpage (Fig. 10(a)). Because the temperature of 150°C was equal to $T_g$ of ABF as shown in Table 1, the transition seemed to be mainly dependent on ABF. With increasing temperature, ABF expanded gradually and then abruptly above $T_g$. Because ABF was much more on the back of the core, this induced compressive stress on the chip surface and made the substrate warp concavely. For the core cavity type DESs, the warpage showed quite complicated behavior with temperature as shown in Fig. 11. For some conditions, the warpage magnitude kept almost the same with increasing temperature and the transition from concave to convex was not observed. To explain this warpage behavior, first we consider the residual stress change from the ABF expansion with increasing temperature. In the case where the clearance was narrow enough, such as 0.15 and 0.3 mm clearance, the warpage behavior seemed to be decided mainly...
Fig. 8 Measured warpage of various device embedded substrates using shadow moiré interferometry before heat treatment. 3-D profiles and data along the two diagonal directions: (a) core surface mounted type DES, (b) core cavity type DES with 0.15 mm clearance, (c) core cavity type DES with 0.3 mm clearance, (d) core cavity type DES with 0.5 mm clearance, and (e) core cavity type DES with 1 mm clearance.
Fig. 9  Warpage measurement line and the measurement surface notification of shadow moiré interferometry.

Fig. 10  3-D warpage profiles of various device embedded substrates using shadow moiré interferometry at the temperature of 260°C and returned temperature of 30°C: (a) core surface mounted type DES, (b) core cavity type DES with 0.15 mm clearance, (c) core cavity type DES with 0.3 mm clearance, (d) core cavity type DES with 0.5 mm clearance, and (e) core cavity type DES with 1 mm clearance.
by the difference in the ABF expansion between the top and bottom of the embedded chip and/or core (ABF was thicker on the top side of the chip and core). However, with increasing clearance width, the increased distance to the core wall and the increased ABF volume in the cavity area seemed to affect the warpage temperature performance. For the possible mechanism of the unchanged concave contour up to the reflow temperature, we are considering a separate behavior between the chip area and the outer wiring area.[21] That is to say, although quite large amounts of stress or stress release seemed to be necessary to induce the warpage transition in the chip area, by increasing the cavity clearance width, the large stress induced in the outer wiring area had no influence up to the chip area. This was possibly because the ABF had quite a low Young’s modulus and ABF in the cavity clearance could absorb the deformation force. However, because the role of the ABF in the cavity clearance is still questionable and the warpage behavior in the wiring area cannot be discussed in enough detail in this study, the detailed discussion will remain for future study. Nevertheless, it was apparent that the residual stress can be controlled easily by obtaining a symmetric and balanced structure using a core cavity type design and the controlled residual stress can decrease the substrate warpage significantly. Additionally, to alleviate residual stress and warpage in an organic substrate the balanced structure in the substrate is more important than improving each material’s mechanical properties.

4. Conclusion

We demonstrated, using a piezo-resistive sensor embedded Si chip, that the core cavity type device embedded substrate has very small residual stress and good warpage performance. The residual stress in the embedded chip was mostly dependent on the balance of the ABF thickness above and below the embedded chip. The warpage properties of the as-received device embedded substrates could be explained by relating them to the residual stress evaluation. However, for the core cavity type DES, the temperature performance of the substrate warpage showed different behavior with increasing cavity clearance width. Because the measurement of the residual stress in the embedded chip region cannot explain the warpage performance in the full area of the package for a cavity clearance width of more than 0.5 mm, the effect and role of the cavity clearance on warpage should be investigated in more detail. Notwithstanding, it is apparent that the core cavity
type DES has the superiority to the core surface mounted type DES in regard to the residual stress and the warpage performance.

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