A Broadband GaAs High Power Millimeter Wave Amplifier with High Gain and Flatness

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Abstract: This paper presents a broadband millimeter-wave power amplifier with a combination of 2-way, each of which consist of a distributed amplifier and cascaded single-ended stages for high gain and output power. To the best of our knowledge, it is the first time that the two amplifiers based on a distributed stage and cascaded single-ended stages have been combined for high power. As a result, the saturated power is improved up to more than 20.5 dBm in the frequency band of 33-66 GHz. Meanwhile, by combining distributed amplifier and cascaded single-ended stages methods, the power amplifier has inherent advantages of high gain and wide bandwidth. Moreover, to improve the gain flatness, small resistor-capacitors in bias circuits are introduced in the cascaded single-ended stages amplifier structure, so the measured S21 is improved to 21.8±0.6 dB in the 38-67 GHz band. These results show that high gain with good flatness and power can be achieved using the proposed method.

Keywords: Millimeter-wave integrated circuits, broadband power amplifier

Classification: Microwave and millimeter wave devices, circuits, and systems

References

[1] K. Honjo: “Milestones of microwave and millimeter-wave technologies-Helical Progress in Device and Circuit,” IEICE Electron. Express 6 (2009) 673 (DOI: 10.1587/elex.6.673).

[2] Y. Ayasli, et al.: “A Monolithic GaAs 1-13 GHz Travelling-Wave Amplifier, IEEE Trans. on Electron Devices. ED-29 (1982) 1072
1 Introduction

The rapid development of millimeter wave gradually becomes the focus of research [1]. And there has been increasing interest in broadband power amplifier covering 38 GHz and 60 GHz. These bands are of interest for microwave engineers. Therefore, it is desirable to design a broadband power amplifier, with high output power, high gain and good flatness.

Several structures have been used to develop broadband amplifiers in the last few decades. One of the classic types is the conventional distributed amplifier (CDA) [2, 3] with multiple transistors in parallel between two transmission lines (TLs) as the input and output networks. The gate and drain impedance can be absorbed into the two TLs. The input voltage that appears at the gate of each transistor is amplified via the transconductance, producing the current that is added in the drain TL. CDA has the distinguishing advantage of bandwidth. However, it is difficult to increase the gain by adding stages, because multiple transistors are required at each stage. Since the development of the CDA, many modified circuit topologies have been developed. To use fewer transistors at each stage is one of them. Minis et al. [4] introduced the principle of a single-stage distributed amplifier (SSDA) for...
the first time. The rest transistors were removed rather than the last transistor. The only remaining transistor was matched between the two artificial TLs. The simulated results showed that over 6 dB gain in the 7-14 GHz band was achieved using one 800 μm FET [4]. Though the frequency band is a little narrower while it has a similar gain as CDA for the single stage, SSDA is more compact and easier to be cascaded to produce high gain, because each stage of SSDA requires only one transistor. As a result, Liang et al. [5] have improved the concept of the SSDA by transforming the structure into an n-stage cascaded single-stage distributed amplifier (n-stage CSSDA), constructed with n-stage SSDAs cascaded in series. The gain was improved up to ~20 dB in the 0-20 GHz band [5], compared with the ~9 dB gain of CDA. Other studies have also reported relatively high gain while using the same number of transistors as in the CDA [6, 7]. In 2003, Deng et al. [8] found that high gain and a broad band could be achieved simultaneously by combing the CDA and CSSDA (CDA-CSSDA). The CDA was used to extend the frequency band followed by CSSDA for the gain stages. In 2007, Virdee et al. [9] further revealed that the gain flatness could be improved by tuning the loss of the transistor in the CSSDA. This modified topology was called lossy CSSDA. However, the disadvantage of CSSDA is the difficulty to deliver high output power, because the associated dissipated power is increased due to the drain termination impedance in the final stage. Consequently, several improved structures that utilize a CDA as the last stage for higher power, namely, the CDA-CSSSDA-CDA and CSSDA-CDA, have been proposed. The output power could be improved to some degree using a multi-transistor CDA at the last stage. However, the improvement was still limited due to the inherent attenuation of the drain artificial TLs from the CDA. To further improve the output power, a distributed stage and two cascaded single-ended stages amplifiers, named CDA-Cascaded single-ended stages, has been developed [10]. The output matching network of the last stage utilized lossless matching to achieve a broadband output power instead of the drain termination impedance in the last stage of the CSSD. Therefore, the minimum saturation output power was improved up to 16 dBm, and a broadband frequency covering 18-71 GHz with a 22 dB gain was achieved. Unfortunately, the gain variation was approximately 8 dB, which would require additional compensation circuits in real applications. Moreover, the output power was relatively low. After this important report, litter improvement has been developed, since 2003.

In this work, a similar circuit topology [10] is adopted, and we focus on improvement of output power and gain flatness. As the state of the art, CDA-Cascaded single-ended stages and CDA-CSSDA circuits contain only a one-way structure. As a result, the output power is limited to 16 dBm. However, CDA- cascaded single-ended stages amplifier has the potential of further producing higher output power using the N-way combination method [11]. To the best of our knowledge, it is the first time that the two amplifiers based on a distributed stage and cascaded single-ended stages have been combined for high power. Saturated output powers of 22-23 dBm in the 34-61 GHz band and 20.5 dBm in the 61-66 GHz band are achieved. The second contribution worth noting is
that a method to improve the gain flatness is to increase transistor loss. We adopted small resistors-capacitors in the bias circuits, instead of Frequency-Dependent Lossy artificial lines [9]. The measured gain flatness is improved to 21.8±0.6 dB in the 38-67 GHz band. Upon the two proposed effective improvements, we feel this amplifier topology will become more useful compared with Ref. [10]. The brief history of the distributed amplifier and the detailed improvements are summarized in Fig.1.

2 Design of the amplifier

Fig.2 shows schematic diagram of two-way combined amplifier. Each way consists of 4 stages. The first stage utilizes three cells 2×23μm transistors as distributed amplifier. The 2nd, 3rd and 4th stage utilizes 4×30μm, 4×40μm and 4×58μm transistors respectively. The circuit is based on GaAs 0.1 μm pHEMT technology. The transition frequency f_T and maximum oscillation frequency f_{MAX} are 135 GHz and 200 GHz, respectively, for a 2×75 μm transistor.
2.1 Distributed Amplifier and Cascaded Single-End Stages

The gain of a distributed amplifier is restricted by the multiple transistors required at each stage. The CSSDA method presents a novel solution to achieve higher gain. The forward available gain $G_{av \, con}$ of the CDA and $G_{av \, cs}$ of the CSSDA can be expressed as in Eqn. (1-2) [7]. The gain of the CSSDA is an exponential function of the number of transistors. Therefore, the gain can be increased by adding stages.

$$G_{av \, con} = \frac{n^2 R_2 Z_{in} Z_{out}}{4}$$ (1)

$$G_{av \, cs} = \frac{2^{2n} R_1 Z_{in} Z_{out}}{4}$$ (2)

where $Z_{con}$ and $Z_{og}$ are the characteristic impedances of the gate and drain lines in CDA, respectively. And $n$ is the stage number, while $g_m$ is the transistors’ transconductance. In CSSDA, $Z_{int}$ is the internal characteristic impedance and $Z_{0xt}$ is the external characteristic impedance which represents the gate line characteristic impedance $Z_{og}$ of the first stage and the drain line characteristic impedance $Z_{od}$ of the last stage [7]. At each stage, the signal can be amplified and terminated by a properly matched load resistor. Therefore, a wide bandwidth and high gain characteristics can be obtained simultaneously. However, it is challenging to deliver high output power because of the drain termination impedance in the output networks.

As a result, a combination of distributed and two cascaded single-ended stages (CDA-Cascaded single-ended stages) without termination impedance in the output networks was presented [10]. The maximum output power was improved to 16 dBm.

To improve the output power, a new topology of a 2-way combination based on a CDA-Cascaded single-ended stage amplifier is presented in Fig. 2. Each path consists of 4 stages, which adopt a similar topological structure of the CDA-cascaded single-ended stages [10]. The first stage uses three cells (2×23 μm).
as a distributed amplifier for well-matched input and a 5-6 dB gain in the 30-70 GHz band. This CDA stage, which requires a larger gate width and three transistors, has an advantage for well-matched input. The 2nd, 3rd, and 4th stages use 4×30 μm, 4×40 μm and 4×58 μm transistors to achieve around 5 dB gain at each stage and a relatively large output power. These last 3 stages provide around 15-17 dB gain in total, almost three times as much as the 1st stage. And in the 2nd, 3rd and 4th stages, the transistor gate width of the later stage is larger than the former one for high output power consideration.

2.2 Gain Flatness
In the previous work [10], the gain was 22 dB in the 18-71 GHz band with an 8 dB gain fluctuation, which required additional compensation in real applications. The second improvement worth noting is that to improve the gain flatness by introducing small resistors-capacitors in the bias circuits. It has been proven that the gain can be tempered to have a flat response by introducing transistor loss and using series RC networks that form the artificial transmission lines [9]. In our work, smaller resistors (R1, R4 and R5 in the gate bias circuits and R2 and R3 in the drain bias circuits, as shown in Fig. 2) are used to improve the gain flatness instead of the loss artificial TLs [9]. As a result, the measured S21 is improved to 21.8 ± 0.6 dB in the 38-67 GHz band.

It has to be mentioned that both the mesa resistor and thin film resistor (TFR) are used in MMIC. The mesa resistor has a higher resistivity of 130 Ohm/Square than the TFR (50 Ohm/Square). However, the TFR has the advantage of being more accurate. Therefore, a larger resistance is often realized by the mesa resistor, such as typically RF-BLOCK and DC-FEED. TFRs are often used in RF chains as small and precise resistors. These resistors (R1-R5) are realized by TFR for RF matching and a gain compensator.

2.3 Output network of 4th transistor and combiner
The output network and the combiner are critical to the amplifier to obtain high power. The resistor in the output network of the CSSDA causes dissipation and limits the output power. An improved 2-way lossless matching network for output networks is proposed.

First, from the load-pull simulation, a series of transistor optimal load impedances $Z_{opt}$ of 30-70 GHz can be found accurately, as shown in Fig. 6. According to Steve Cripps’ load line theory, the equivalent circuit for load-pull impedance sets the resistor $R_{opt}=(V_{dc}-V_{th})/(I_{max}/2)$ and $C_{ds}$ in parallel, as shown in Eqn. (3). When $freq>1/(2\pi CR)$, as the frequency increases, the real and imaginary parts of $Z_{opt}$ decrease. It is consistent with the simulation results in the Smith chart, where $Z_{opt}$ decreases ($Z_{opt}=22.6+j\times14.7$ @ 30 GHz, $8+j\times6$ @ 70 GHz).

$$Z_{opt} = \frac{1}{R_{opt}} = \frac{R}{1+jωC} = \frac{1}{1+w^2C^2R^2} = \frac{1}{wCR} + \frac{1}{wCR}$$

Secondly, as shown in Fig. 3 (a) and (b), the 2-way output network and combiner structure (LOAD=50 Ω) can be split into two independent output networks.
(LOAD=100 Ω) in parallel, because the 2-way structure is operated in the even mode ideally. Due to symmetry, only half of the circuit requires analysis, as shown in Fig. 3 (c). This method can simplify the design of broadband output matching networks. As shown in Fig. 3 (c), port 1 and 100 Ω load are connected to the output network, and we can calculate $Z_{load}$ from the SP simulation.

![Fig. 3.](image)

(a) Two-way output network (b) the equivalent separated components (c) the simulation of the output network.

The different points in the network are shown in Fig. 4. The impedance transmission steps and frequency responses are shown in Fig. 5. The three TLs between points (2) and (3) are used to progressively decrease the 100-Ω impedance toward $Z_{opt}$. Two wide TLs (TL1 and TL2) between points (4) and (5) serve as small capacitors to adjust the impedance. The drain bias circuits between points (5) and (6) are equivalent to the parallel-L to neutralize the imaginary part of the impedance.

![Fig. 4](image)

The output network circuits

![Fig. 5](image)

Steps to transform the 50-Ω impedance to $Z_{opt}$ in 30-70 GHz. Every curve is marked at 30 GHz. The Smith chart is normalized to $Z_0=50$Ω.

Although two independent output network (LOAD=100 Ω) method can simplify
the design, the ignored coupling effects may influence the performance to some degree. As a result, the final 2-way layout that includes the complete circuits in Fig.2 should be validated using an electromagnetism (EM) simulation. As shown in Fig.6, the simulated $Z_{load}$ curve is similar to a circle with a small area, and the $Z_{opt}$ line calculated from Load Pull simulation runs across the $Z_{load}$ circle.

![Image](image_url)

**Fig. 6** Simulated impedance $Z_{load}$ of the output network with the power combiner and the optimal impedance $Z_{opt}$ from load pull simulation

It is worth noting that the $Z_{load}$ curve in Fig. 6 and the m6 curve in Fig. 5 are slightly different, and the one in Fig. 6 may be more accurate. This difference may be caused by the ignored coupling and parasitic effects, ignored by the m6 curve in Fig. 5. As a result, a final 2-way layout simulation that includes all the circuits in Fig. 2 is necessary. The layout may be retuned in several iterations to account for the coupling and parasitic effects. In the iterations, it is convenient to adjust the lengths of TL1 and TL2 to remedy these differences. As shown in Fig. 6, after removing TL1 and TL2, the $Z_{load}$ shows an obvious difference.

### 3 Simulated and measured results

A photograph of the amplifier is shown in Fig. 7. The size is 2.5 mm×2.2 mm. The amplifier is measured with a wafer measurement system on a Cascade probe station and a vector network analyzer (VNA) Keysight PNA-N5227A. The bias point is $V_g$=-0.25 V, $V_d$=4 V, and $I_d$=0.45 A.
Comparison between the simulated and measured small signal results are shown in Fig. 8. The small signal gain is 20-22.4 dB in the 36-68 GHz band and notably 21.2-22.4 dB in the 38-67 GHz band. Due to the limit of VNA (0.01-70 GHz), the highest measured frequency is only 70 GHz. The measured $S_{11}$ and $S_{22}$ is less than -10 dB above 38 GHz.

The comparison of the large signal results are shown in Fig. 9. The output P-1 dB power is greater than 19 dBm, and the output saturated power is greater than 20.5 dBm in the 33-66 GHz band. The simulated and measured results are mostly consistent except the measured frequency band becomes slightly narrower than the simulation. These differences might be caused by some tolerance effects, such as manufacture tolerance and transistor’s large signal model tolerance.

Fig. 7  Photograph of the broadband amplifier

Fig. 8  Simulated and measured small signal result: (a) S21 (b) S11 and S22
Table I compares the previous studies with the proposed design. These studies used approaches such as CDA [2], SSDA [4], CSSDA [5-7], CDA-CSSDA [8], lossy CSSDA [9], CDA-Cascaded single-ended stages [10], and N-way combinations [11]. High degrees of gain, flatness and output power are achieved simultaneously in our design.

| Ref. | Freq (GHz) | Gain (dB) | S11,S22 (dB) | Psat (dBm) | Feature |
|------|------------|-----------|--------------|------------|---------|
| [2]  | 1-13       | 9±1       | ≤-8          | -          | CDA, GaAs |
| [4]  | 7-14       | 5.5-6*    | ≤-12*        | -          | SSDA, 0.7μm GaAs |
| [5]  | 1-20       | 20±0.25*  | ≤-14*        | -          | CSSDA, HMIC |
| [6]  | 0.8-10.8   | 27±1      | ≤-10         | -          | CSSDA, HMIC |
| [7]  | 0.1-40     | 39±2      | ≤-10         | ≥15        | CSSDA, HMIC |
| [8]  | 2-10       | 22±2      | ≤-7          | ≥12.5      | CDA-CSSDA, 0.15μm GaAs |
| [9]  | 1-12       | 22±0.5    | ≤-10         | -          | Lossy-CSSDA, HMIC |
| [10] | 18-71      | 22±4      | ≤-5          | ≥16        | CDA-cascaded single-ended stages, 0.15μm GaAs |
| [11] | 50-70      | 15-17     | ≤-8          | ≥22        | 32 ways combination, 65 nm CMOS |
| This work | 36-66     | 21.2±1.2(36-68 G) | 21.8±0.6(36-67G) | ≤8 | 22-23(34-61G) | CDA-cascaded single-ended stages, 0.1μm GaAs |

* Only simulated results have been found.

4 Conclusion
A broadband high-power amplifier is presented using a two-way combination. Each way contains one stage distributed amplifier and three cascaded single-ended stages. The P-1dB power is greater than 19 dBm, and the output saturated power is greater than 20.5 dBm in the 33-66 GHz band. Small resistors are used in the bias circuits to improve the gain flatness. The small signal gains are 21.2±1.2 dB in the 36-68 GHz band and notably 21.8±0.6 dB in the 38-67 GHz band. These results show that high degrees of power, gain and flatness can be achieved by using the proposed method.