An algorithmic approach for minimizing test power in VLSI circuits

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Abstract: Testing is an approach to check the function of the circuit or device under the test after its fabrication. To test the device, test patterns are required. The test patterns can be generated with the help of EDA tool. Those patterns having huge number of unfilled bits. The unfilled bits need to be assigned with certain logical value. This paper proposed two new algorithms. First algorithm assigns the unfilled bits with effective logical value and second algorithm change the order of test set and both algorithms aims to reduce the test power. Investigation on benchmark circuits shows that, the results of proposed algorithms effectively reduces the test power.

1 Introduction

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions of transistors in order to get a single chip. The complexity of the circuit has been increased over years with the advancement of technology and testing of those circuits become complex and more important in order to prove the quality of product. The testing is done to check the functionality of the circuits after the verification process.

An IC may contain $2^n$ test patterns which is harder to generate test patterns and to check its quality when the value of $n$ increases. The time consumption for this testing will be very much higher. So when an IC chip is manufactured, its fault detection is a bit harder. This could make IC tests much easier and very much faster. Test pattern generator generates the test patterns. The generated test patterns are applied to devices or circuits that need to be tested. The output of the circuit for the given test set will be compared by the comparator. The comparator gets the stored response from memory and compares it with the output of CUT. If a match occurs for the entire test set then the respective CUT will be considered as PASS otherwise fail. The following figure -1 illustrates the basic testing process.
Due to the development of integrated circuits in the past few decades, the size of electronic components has been reduced, introducing complexity in testing those devices. During testing, unique test patterns stored in Automatic Test Equipment (ATE) are applied to the electronic device to evaluate its functionality. Nowadays, traditional techniques like ATE are becoming not suitable. Cost of ATE mainly depends on its memory size and its decoder complexity. The need of a minimum number of test sets is required to reduce the ATE memory and its cost. Minimal test sets also reduce the Test Application Time (TAT).

The cost of an electronic device or an IC indirectly depends on test cost. The test cost again depends on test power. The reason is during testing, test vectors stored in ATE are applied to the Circuit. These test vectors contain logic 0, logic 1, and unfilled bits. The unfilled bits may be assigned with either logic 0 or 1. If any test vectors that contain more successive logic 0s and 1s may increase the power dissipation. It is similar to switching on and off the light bulb continuously. The excessive heat that may damage the IC during its test. This affects the yield. So cost of the IC gets increased. The conclusion is test power is the major cause for test cost. So, the power dissipation during the test should be minimized.

2 Existing techniques

The test power is directly depending on logic value of unfilled bits because the unfilled bits occupy the major parts of the entire test set. Thus, it is important to fill the logic value for unfilled bits. Assigning proper values to the unfilled bits may reduce the power dissipation. There are numerous bit filling techniques existing. In Random bit filling, the unfilled bits are filled randomly with logical value of zeros and ones. But this technique increases the test power. Logic 0 filling technique and Logic 1 filling technique fills the ‘X’ bit with logical value zero and one respectively. The ‘X’ bit is filled with adjacent bit in adjacent filling technique. Column Bit Filling (CBF) is based on hamming distance between successive test vectors [1][2]. Based on hamming distance, test vectors are reordered and unfilled bits are filled column wise. Some code-based techniques also exist to reduce the test power. The proposed algorithm reducing the test power effectively compare to the above existing methods. The two categories of test power are maximum test power that exist during the test application and average of all test pattern power. Both maximum (peak) power and average power are calculated based on weighted transition metric.

2.1 Equations

The Weighted transition metric can be represented as follows.

\[ WTM = \sum_{i=1}^{n-1} (n - i) (t_{ij} \oplus t_{i,j+1}) \]  \hspace{1cm} [1]

Average power:

\[ P_{avg} = \frac{\sum_{j=1}^{N} \sum_{i=1}^{n-i} (i-0) (t_{ij} \oplus t_{i,j+1})}{N} \]  \hspace{1cm} [2]

**Figure 1.** Testing of an IC

Due to the development of integrated circuits in the past few decades, the size of electronic components has been reduced and introduced complexity in testing those electronic devices. During testing, unique test patterns stored in ATE are applied to the electronic device to evaluate its functionality. Nowadays, traditional techniques like ATE (Automatic Test Equipment) are becoming not suitable. Cost of ATE mainly depends on its memory size and its decoder complexity. The need of a minimum number of test sets is required to reduce the ATE memory and its cost. Minimal test sets also reduce the Test Application Time (TAT).

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Peak power:

\[
P_{\text{peak}} = \max_{j \in \{1, \ldots, N\}} \sum_{i=1}^{n-1} (n - i)(t_{i,j} \oplus t_{i,j+1})
\]  

\[3\]

\(N\) = Number of test vectors chosen for a particular circuit.
\(t_{i,j} , \ t_{i,j+1}\) are successive test bits of test vector.
\(n\) = total test bits in a single test vector.

3 Proposed algorithms

Algorithm-1

Test power is mainly depending on the position of unfilled bit also switching activity between successive test bits in the test vector. The proposed algorithm fills the unfilled test bit to a specific logic value based on the position. It combines the concept of 0 filling, 1 filling and adjacent filling based on the position of ‘X’ bit. The algorithm steps are follows.

Algorithm Steps:

Step1: If the unfilled bit ‘X’ is LSB: then filled with adjacent bit. If its MSB then filled with previous bit.
Step2: If previous bit of ‘X’ bit is zero and adjacent bit is one then fill it with previous bit.
Step 3: If previous and adjacent bit are same then fill it with previous bit.
Step 4: If ‘X’ bit occurs repeatedly then the length of ‘X’ bit is calculated and filled based on step 1 to 3

Algorithm-2

The proposed arithmetic approach is very simple and does not require and complex hardware to generate the test. This approach utilizes the existing test set and modify it effectively. It’s always wise to improve the test set instead of generating new test set. Mintest vectors are taken as reference and they are modified by using the arithmetic approaches. Hence by doing this, different test patterns will be obtained. The Mintest vectors of ISCAS benchmark has taken as reference vectors[6],[7],[8]. The don’t care bits are filled with logic 0 initially. Logic 1 may increase the test power. Then test patterns are reordered in effective way to perform arithmetic approach. Then arithmetic operations are performed with successive test patterns

4 Experimental Results

The proposed algorithm is applied for reducing the test power with single scan chain architecture. This algorithm is implemented using Python program. The ISCAS 89Benchmark circuits are taken as reference circuits to carry out the research.

| ISCAS’89 Circuits | No. of bits/Vector | Total bits | No of X bits |
|-------------------|--------------------|------------|--------------|
| S-9324            | 247/159            | 39273      | 28672        |
| S-13207           | 700/236            | 1,65,200   | 153877       |
| S-15850           | 611/126            | 76986      | 64329        |
| S-35932           | 1763/16            | 28208      | 9957         |
| S-38417           | 1664/19            | 1,64,736   | 112154       |
| S-38584           | 1464/136           | 1,99,104   | 163817       |

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 1 |
|------------------|-------------------|-----------|-----------|------------------|--------|----------------------|
| S-5378           | -                 | 10127     | 10309     | 12516            | 12822  | 11430                |
| S-9324           | 17494             | 12994     | 14471     | 20431            | 17169  | 14016                |
| S-13207          | 135607            | 101127    | 113980    | 100896           | 125392 | 94619                |
| S-15850          | 100228            | 81832     | 80453     | 99537            | 96452  | 70722                |
| S-35932          | 683765            | 505295    | 446608    | 572169           | 660096 | 437619               |
| S-38417          | 572618            | 531321    | 547921    | 583614           | -      | 480557               |
Table 3. Average power Reduction -Algorithm 1

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 1 |
|------------------|------------------|----------|----------|------------------|--------|----------------------|
| S-5378           | -                | 3336     | 3085     | 5851             | 10344  | 3469                 |
| S-9324           | 14630            | 5692     | 5870     | 14749            | 13492  | 4025                 |
| S-13207          | 122301           | 12416    | 16319    | 74854            | 103400 | 8028                 |
| S-15850          | 90899            | 20742    | 26503    | 102154           | 64275  | 13754                |
| S-35932          | 601840           | 172665   | 174770   | 337658           | 443030 | 118935               |
| S-38417          | 535875           | 136634   | 149640   | 610803           | -      | 86707                |

Table 4. Peak power Reduction- Algorithm 2-Xor

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|------------------|------------------|----------|----------|------------------|--------|----------------------|
| S-5378           | -                | 10127    | 10309    | 12516            | 12822  | 10223                |
| S-9324           | 17494            | 12994    | 14471    | 20431            | 17169  | 9772                 |
| S-13207          | 135607           | 101127   | 113980   | 100896           | 125392 | 121228               |
| S-15850          | 100228           | 81832    | 80453    | 99537            | 96452  | 87787                |
| S-35932          | 683765           | 505295   | 446608   | 572169           | 660096 | 537854               |
| S-38417          | 572618           | 531321   | 547921   | 583614           | -      | 190334               |

Table 5. Average power Reduction -Algorithm 2 -xor

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|------------------|------------------|----------|----------|------------------|--------|----------------------|
| S-5378           | -                | 3336     | 3085     | 5851             | 10344  | 3469                 |
| S-9324           | 14630            | 5692     | 5870     | 14749            | 13492  | 4025                 |
| S-13207          | 122301           | 12416    | 16319    | 74854            | 103400 | 8028                 |
| S-15850          | 90899            | 20742    | 26503    | 102154           | 64275  | 13754                |
| S-35932          | 601840           | 172665   | 174770   | 337658           | 443030 | 118935               |
| S-38417          | 535875           | 136634   | 149640   | 610803           | -      | 86707                |

Table 6. Peak power Reduction- Algorithm 2-or

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|------------------|------------------|----------|----------|------------------|--------|----------------------|
| S-5378           | -                | 10127    | 10309    | 12516            | 12822  | 10223                |
| S-9324           | 17494            | 12994    | 14471    | 20431            | 17169  | 9772                 |
| S-13207          | 135607           | 101127   | 113980   | 100896           | 125392 | 121228               |
| S-15850          | 100228           | 81832    | 80453    | 99537            | 96452  | 87787                |
| S-35932          | 683765           | 505295   | 446608   | 572169           | 660096 | 537854               |
| S-38417          | 572618           | 531321   | 547921   | 583614           | -      | 190334               |

Table 7. Average power Reduction -Algorithm 2 -or

| ISCAS’89 Circuit | ORIGINAL TEST SET | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|------------------|------------------|----------|----------|------------------|--------|----------------------|
| S-5378           | -                | 3336     | 3085     | 5851             | 10344  | 4419                 |
| S-9324           | 14630            | 5692     | 5870     | 14749            | 13492  | 4735                 |
Table 8. Peak power Reduction - Algorithm 2-and ISCAS’89 Circuit

| Circuit | ORIGINAL | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|---------|----------|-----------|-----------|-------------------|--------|----------------------|
| S-13207| 122301   | 12416     | 16319     | 74854             | 103400 | 16036                |
| S-15850| 90899    | 20742     | 26503     | 102154            | 64275  | 29099                |
| S-35932| 601840   | 172665    | 174770    | 337658            | 443030 | 239145               |
| S-38417| 535875   | 136634    | 149640    | 610803            | -      | 41646                |

Table 9. Average power Reduction -Algorithm 2-and ISCAS’89 Circuit

| Circuit | ORIGINAL | 0 FILLING | 1 FILLING | ADJACENT FILLING | CBF &DV | Proposed Algorithm 2 |
|---------|----------|-----------|-----------|-------------------|--------|----------------------|
| S-5378  | -        | 10127     | 10309     | 12516             | 12822  | 10322                |
| S-9324  | 17494    | 12994     | 14471     | 20431             | 17169  | 5060                 |
| S-13207 | 135607   | 101127    | 113980    | 100896            | 125392 | 90342                |
| S-15850 | 100228   | 81832     | 80453     | 99537             | 96452  | 49975                |
| S-35932 | 683765   | 505295    | 446608    | 572169            | 660096 | 327437               |
| S-38417 | 572618   | 531321    | 547921    | 583614            | -      | 44054                |

The following figure 2 figure gives the comparative analysis on both algorithms. The algorithm 1 uses the bit filling approach and second algorithm fills all unfilled bits with logic 0 and ordering the test vectors based on its binary weights. The peak power and average power are the major impact in testing[12][13][14]. Results of the figure indicate that Peak power and average power effectively reduced with algorithm 2 with And arithmetic approach.

![Peak Power Comparison](image)

**Figure 2.** Peak power comparisons of Proposed Algorithms
Columnwise Bit Stuffing with Difference Vector: A Better Scheme for Test Data Compression with Run Length Based Codes. In VLSI Design International Conference on (pp. 33-38). IEEE Computer Society.

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5 Conclusion:
The proposed X-filling algorithmic method reduces switching activity and thus reducing both peak test power and average test power. This algorithm improves the reduction of peak power 64%, 10%, 8% & 20% percentage over original test vectors, 0 filling, 1 filling and adjacent filling respectively. The reduction of average test power of the proposed algorithm is 91%, 33%, 37% and 79% over min-test vectors, zero filling, one filling and adjacent filling respectively. The second proposed algorithm indicates that the average of total peak power and mean power of benchmark circuits greatly reduced with binary And approach. Test data compression is used to reduce the size of test bits. Several compression techniques exist for test data compression [15]. The future work will be carried on data compression using arithmetic technique.

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