Parasitic consideration for differential capacitive sensor

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ABSTRACT
Parasitic integration for a single supply differential capacitive sensing technique is presented in this paper. In real capacitive sensor measurement, parasitic impedance exists in its measurement. This paper objective is to study the effect of capacitive and resistive parasitic to the capacitive sensor circuit. The differential capacitive sensor circuit derivation theory is elaborated first. Then, comparison is made using simulation. Test was carried out using frequency from 40 kHz up to 400 kHz. Result is presented and have shown good linearity of 0.99984 at 300 kHz, R-squared value. This capacitive sensor is expected to be used for energy harvesting application.

1. INTRODUCTION
In instrumentation and measurement research field, capacitive sensor measuring system easily provides efficient changes of parameter of interest into various range of capacitance conversion. Such advantage takes place without functionality loss compared to resistive and inductive sensors [1]. Capacitive sensor uses electric field to sense either conductive or non-conductive material, as long the material has surface area, its dielectric material and within the electric field distance [2]. The design of capacitive sensors can be categorized into several requirements. Such requirements are shown in works that require accuracy [3], resolution [4], noise immunity [5] and sensitivity [6].

Due to its low power consumption and its sensing element consumes no energy, capacitive transducer sensor could be a contribution factor for low power measurement. There have been great efforts on the readout circuit and several reported ways of conversion using capacitance sensing for sensor interface circuits. Before capacitance conversion takes place into other forms like frequency, phase or digital, it first converts into voltages and continue its conversion process into desired forms depending on the design and method used in the system.

Majority of previous work utilizing the differential capacitive sensing presented based on operational amplifiers [7-8]. This work is an extended version of work in [6] that will discuss on its parasitic consideration in real application. The supply used in this circuit is a single source that provide its power to the discrete components circuits, such as oscillator, operational amplifiers, voltage divider circuit and instrumentation amplifier. It was tested that using this method frequency 40 kHz up to 400 kHz are suitable to be used in the system. However, focus of this paper is on frequency at 300 kHz.
2. RESEARCH METHOD

One of the important considerations should be included in real circuit are parasitic capacitance and resistance associated at the capacitance sensor. This is usually caused by connecting wires and circuit construction. The total parasitic capacitance and resistances are often contributing to errors in measurement from the actual reading and may reduce the sensitivity level of the system if not properly managed.

2.1. Parasitic capacitance and resistance theory

In actual setting, based on work proposed in [6], there are also parasitic capacitance, $C_{p1}$ and $C_{p2}$ at capacitance sensor, $C_s$, which is located at one side of the $C_s$ electrode, parallel to the excitation sinusoidal source and parallel to the noninverting amplifier input, respectively. The third parasitic capacitor, $C_{p3}$, which is found at the offset capacitor parallel to the $C_s$ can be cancelled by nulling the capacitor or offset nulling through differential capacitance sensing, as confirmed in [5, 9-10]. These parasitic capacitance and resistances are shown in Figure 1. The proposed differential capacitive sensor is based on Figure 2 of [6] and [11]. This figure is not included in this paper due to avoid repetitive publication.

\[
\begin{align*}
\text{Figure 1. Half of the differential capacitance sensing circuit with parasitic} \\
\text{parasitic capacitance and resistance} & \quad \text{Z_sense} \\
& \quad \text{Z_feedback} \\
& \quad \text{V_{ref}} \\
& \quad \text{V_{out_A}} \\
\end{align*}
\]

\[
\begin{align*}
\text{Figure 2. Estimated bode plot of } V_{out_A}/V_{in} \text{ from the theory} \\
\end{align*}
\]

In this case, capacitive sensor, $C_s$ electrodes need to be properly shielded in order to give actual measurement and to avoid environment electromagnetic interference that would affect the behaviour of the circuit. However, in real situation stray capacitance always form between the shielding and the electrodes even in fully shielded condition.

Due to this, proper handling on the contributed parasitic resistance and capacitances should be taken into account. Theoretically, parasitic capacitance, $C_{p1}$ and $C_{p2}$, have virtually no effect on the current passing through $C_s$ when measurement is taken from the sensor capacitor, $C_s$. This is due to the low ohmic of the input voltage excitation signal at one side of the electrodes and $C_{p2}$ is negligible because of low impedance value at the input amplifier.

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The excitation voltage, \( V_{ex} \cos(2\pi f_{ex} t + \phi) \), with an amplitude voltage, \( V_{ext} \), excitation frequency, \( f_{ex} \), and \( \phi \) is the magnitude phase angle. \( Z_{ext} \) is an equivalent impedance at the sensor capacitance, \( C_s \), where the parasitic resistance, \( R_p \), and parasitic capacitance, \( C_{pB} \), are in parallel to the sensor. \( Z_{feedback} \) is the equivalent impedance at the sensing Opamp. Note that in this writing, the discussion only focus on one side of the differential Capacitance-to-Voltage Converter (CVC), since the other half behave the same as long as the components value is kept identical in symmetrical order. The transfer function derivation of circuit in Figure 1 are given in (1) to (3)

\[
Z_{sense} = R_A + Z_B = R_A + \frac{R_p}{j\omega R_p (C_s + C_p) + 1} + \frac{R_A + R_p}{j\omega R_p (C_s + C_p) + 1} 
\]

(1)

\[
Z_{feedback} = \frac{R_f}{1 + j\omega R_f C_f} 
\]

(2)

\[
V_{out,A} = \left(1 + \frac{Z_{feedback}}{Z_{sense}}\right) V_{ref} - \frac{Z_{feedback}}{Z_{sense}} V_{ext} 
\]

(3)

2.2. The proposed conditions exist in real situation

This transfer function is independent of parasitic resistors as long as it is within the passband frequencies. By substituting (1) and (2) into (3), the transfer function of \( V_{out,A} \) is extended from [12] as in the following:

\[
V_{out,A} = \begin{cases} 
1 + \frac{R_f}{R_A + R_p} \left\{ \frac{1 + j\omega R_p (C_s + C_p)}{1 + j\omega R_s (C_s + C_p)} \right\} V_{ref} \\
- \frac{R_f}{R_A + R_p} \left\{ \frac{1 + j\omega R_p (C_s + C_p)}{1 + j\omega R_s (C_s + C_p)} \right\} V_{ext} \\
= V_{ref} + \frac{R_f}{R_A + R_p} \left\{ \frac{1 + j\omega R_p (C_s + C_p)}{1 + j\omega R_s (C_s + C_p)} \right\} (V_{ref} - V_{ext}) 
\end{cases} 
\]

(4)

The target of CVC system is to have an independent and single source, i.e. from ambient energy, free from other additional sources, such as the battery. Due to the requirement, reference DC voltage source needs to be taken care of. Here, the value of the reference voltage, \( V_{ref} \), which to be supplied to the non-inverting Opamp input is obtained through voltage divider circuit supplied by the energy harvested source, \( V_s \). The reference voltage, \( V_{ref} \), is set at half of source voltage, \( V_s \), in order to gain a non-zero level output voltage at the end output voltage. This is due to the fact that any negative sides of sinusoidal wave will be cut out after rectification at the rectifier circuit (please refer to Figure 2 of [6]). Therefore, it is chosen to have the output voltage to be shifted at the half of \( V_s \), which is at the reference voltage, \( V_{ref} \).

As mentioned earlier, the supply voltage, \( V_s \), is obtained from ambient energy. Energy for \( V_{ref} \) is by choice is kept constant. However, because the source to this \( V_{ref} \) is supplied by supply voltage, \( V_s \), received from available ambient sources. It should worth to consider certain cases may happen, i.e. decreasing in supply voltage from intended voltage level. Further effect can be studied on (4) by simplifying the equation to (5) to study the inconsistent \( V_{ref} \) voltage value conditions that may exist in the circuit.

\[
V_{out,A} = (1 + A) V_{ref} - (A) V_{ext} 
\]

(5)
where

\[ A = \frac{R_f}{R_a + R_p} \left( \frac{1 + j \omega R_p (C_s + C_p)}{1 + j \omega R_f C_f} \right) \]  

(6)

It can be seen in (5) the output voltage includes \( V_{ref} \) and excitation voltage, \( V_{ext} \), in its output value, \( V_{out,A} \). The output voltage is categorised into several cases: (i) \( V_{ref} = 0 \) (ii) \( V_{ref} < V_{ext} \) (iii) \( V_{ref} = V_{ext} \) and (iv) \( V_{ref} > V_{ext} \) as supported in [13]. The transfer function equations are derived as in (3.13) to (3.16)

Case I: \( V_{ref} = 0 \)

\[ \frac{V_{out,A}}{V_{ext}} = -A \]  

(7)

Case II: \( V_{ref} < V_{ext} \) when \( V_{ref} = (1 - m)V_{ext} \) where \( 0 < m < 1 \)

\[ \frac{V_{out,A}}{V_{ext}} = (1 + A)(1 - m) - A \]  

(8)

Case III: \( V_{ref} = V_{ext} \)

\[ \frac{V_{out,A}}{V_{ext}} = 1 \]  

(9)

Case IV: \( V_{ref} > V_{ext} \) when \( V_{ref} = nV_{ext} \) where \( n > 1 \)

\[ \frac{V_{out,A}}{V_{ext}} = n + (n - 1)A \]  

(10)

where \( m \) and \( n \) is the multiplier numbers of excitation input voltage, \( V_{ext} \) equal to \( (1 - m)V_{ext} \) or \( nV_{ext} \).

As long the excitation frequency satisfies the condition of within the cutoff frequencies boundary conditions imposed by the parasitic resistances, the frequency of input voltage is independent to the CVC system. The cutoff frequencies are:

\[ f_{ext} \geq \frac{1}{j \omega R_f C_f} \]  

(11)

\[ f_{ext} \geq \frac{1}{j \omega R_p (C_s + C_p)} \]  

(12)

\[ f_{ext} \leq \frac{R_a + R_p}{j \omega R_a R_p (C_s + C_p)} \]  

(13)

Several conditions may exist to the output voltage, one of it is when \( V_{ref} = 0 \), the transfer function of

\[ \frac{V_{out,A}}{V_{ext}} = -A \], is further derived to obtain the estimated output voltage frequency range. This is shown in bode plot in Figure 2 where component values are as derived in (14)

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3. PARASITIC CAPACITANCE AND RESISTANCE INTEGRATION SIMULATION RESULTS

The simulation is done using OrCAD Capture Cadence 18.0 PSpice simulation. When $V_{ref}=0$, using components $C_f=C_r=C_x=5 \text{ pF}$ and $R_f=10 \text{ M}\Omega$, $C_x=8 \text{ pF}$ and parasitic resistance $R_A=20 \text{ M}\Omega$, and $R_P=2.2 \Omega$ parasitic capacitance, $C_P=5.6 \text{ pF}$. From Figure 2 and (14), expected corner frequencies from calculation in (11), (12), and (13), are 751 Hz, 3.18 kHz and 6.82 GHz, respectively as shown in the results of Figure 3. This shows a match simulation with the estimated theoretical drawing and values.

Further analysis of the overall transfer function for second condition when $V_{ref} < V_{ext}$ the transfer function is

$$
\left| \frac{V_{out,A}}{V_{ext}} \right| = (1 + A) \left( 1 - m \right) - A.
$$

Simulation result with integration of parasitic resistance and capacitance is shown in Figure 4. Expected corner frequencies from calculation in (11), (12), and (13), are 159, 588 Hz and 31.9 kHz using components $C_f=C_r=C_x=5 \text{ pF}$ and $R_f=1 \text{ M}\Omega$, $C_x=8 \text{ pF}$ and parasitic resistance $R_A=20 \text{ M}\Omega$, and $R_P=2.2 \Omega$ parasitic capacitance, $C_P=5.6 \text{ pF}$. 

![Figure 3. Simulated magnitude at opamp a output with parasitic](image)

\[
K \cdot \frac{f_1}{f_2 \cdot f_3} \cdot \frac{1 + \frac{s}{f_1}}{1 + \frac{s}{f_2}} \cdot \frac{1 + \frac{s}{f_3}}{1 + \frac{s}{f_4}}
\]  

(14)

where

\[
f_1 = R_f(C_x + C_p)
\]

\[
f_2 = R_f C_f
\]

\[
f_3 = \frac{R_A R_P}{R_A + R_P}(C_x + C_p)
\]

\[
K = - \frac{R_f}{R_A + R_P} \frac{R_f(C_x + C_p)}{R_f C_f \cdot \frac{R_A R_P}{R_A + R_P}(C_x + C_p)}
\]

(15)
3.1. Simulation of output voltage without parasitic integration

The linearity graph across frequencies obtained using $R_f=10\ M\Omega$, $R_d=100\ k\Omega$ and $C_d=0.1\ \mu F$, have shown wider detection range and high in sensitivity when run less than and equal to $f_{ext}=100\ kHz$. However, when frequency goes higher than 100 kHz, which is shown in Figure 5, less points of detection is observed, and the sensitivity is low.

By rules, the $f_{3dB}$ should be low than the cutoff frequency ($f_c=3.18\ kHz$). In this case has satisfied the condition when using $R_f=100\ k\Omega$ and $C_d=0.1\ \mu F$, the $f_{3dB}=15.9\ Hz$. Improvement on the number of detection points across certain capacitance range is increased by increasing the bandwidth of the low pass filter. This is by decreasing the $R_d$ value and $C_d$ value of the components. Figure 6 shows the simulation results using low $R_d$ and $C_d$ values of 10 kΩ and 0.01 $\mu F$ respectively, with $R_f=10\ M\Omega$. In this case, the cutoff frequency, $f_{3dB}=1.59\ kHz$, which satisfy the condition less than cutoff frequency $f_c=3.183\ kHz$. 

![Figure 4. Simulated magnitude transfer function at the output CVC circuit.](image)

![Figure 5. Effect of output voltage with $C_x$ variation for $R_d=100\ k\Omega$ and $C_d=0.1\ \mu F$ using $V_s=3.3\ V$ at 300 kHz](image)
The same trend is observed when frequency is increased, the detection capacitance is minimized. Compare to the previous results of Figure 5, the differential CVC output voltage is improved by more points were detected across wider capacitance range, using same capacitance change, ΔC=0.5 pF as seen in Figure 6. This method is suitable if high frequency of operation is targeted over the sensitivity, due to low sensitivity is observed at high frequency.

Improvement is made to the capacitance change, ΔC, so that wider capacitance range is been detected with low detection change at high frequency. This is done by using the Rf selection method. This method is considered relevant due to diode current value at higher frequency (i.e: 300 kHz) is becoming stable regardless of the change of the Rf value (refer to diode current of Figure 3 of [14] for Rf=10 kΩ and Cf=0.01 μF). Same principle applied to any components value at higher frequency, such as when Rf=10 kΩ and Cf=0.1 μF of Figure 2 of [14].

Figure 7 shows the linearity result using ΔC=0.1 pF change with Rf=10 kΩ and Cf=0.1 μF. Different Rf has been selected to overcome the sensitivity problems where Figure 7 is at Rf=200 kΩ at f_{ext}=300 kHz. These values must satisfy the condition > f_{3dB} range. In this case the frequencies are 3.183 kHz, 159 kHz and 106 kHz respectively, when f_{3dB}=159.13 Hz. At high frequency, high sensitivity of capacitive change of detection is achieved by reducing the value of the feedback resistor Rf.

3.2. Simulation with parasitic capacitance and resistance integration

In this test, parasitic capacitance and resistance involved in the real situation is mimicked as in the Zsense part of circuit in Figure 1 under parasitic capacitance and resistance region. This is done by using the component’s value tested earlier, Rf=10 MΩ, Cf=5 pF, Rd=10 kΩ, Cd=0.1 μF, V=3.3 V, Cr=5 pF, Cx=0.1-12

![Figure 6. Effect of output voltage with Cx variation for Rd=10 kΩ and Cd=0.01 μF using Vs=3.3 V at 300 kHz](image)

![Figure 7. Corrected capacitance change, ΔCx=0.1 pF with Rf=200 kΩ at f_{ext}=300 kHz](image)
pF, and by including the parasitic components, \( R_p = 2.2 \, \Omega \), \( R_f = 30 \, M\Omega \), \( C_{p3} = 0.05 \, pF \), \( C_{p1} = 0.56 \, pF \), \( C_{p2} = 0.56 \, pF \) for comparison purpose. Figure 8 shows the results using 300 kHz frequency. The 300 kHz frequency was chosen to test the possibilities and condition of the differential amplifier when running at frequency higher than 100 kHz.

![Figure 8](image)

**Figure 8. Corrected capacitance change, \( \Delta C_x = 0.1 \, pF \) with \( R_f = 200 \, k\Omega \) at \( f_{ext} = 300 \, kHz \)**

Table 1 shows the results with and without parasitic condition at 300 kHz excitation frequency. As predicted, the power consumption is higher with parasitic resistance and capacitance load. However, the output voltage range is higher with parasitic.

| Test                  | Detection range, \( C_x \) (pF) | Output Voltage (V) | \( P_{diss} \) (mW) | Sensitivity (mV/\( f \)F) | R-squared value |
|-----------------------|----------------------------------|--------------------|---------------------|---------------------------|-----------------|
| With Parasitic        | 1.0 – 6.0                        | 2.1075 – 2.4122    | 78.5                | 0.06094                   | 0.99984         |
| Without Parasitic     | 4.7 – 6.6                        | 1.6446 – 1.6869    | 3.83                | 0.02226                   | 0.99944         |

It is observed from the simulation result; power dissipation is increased when parasitic is included in the design. This is due to the high resistance involved across the capacitance detection sensor, \( C_s \) (i.e: \( R_p = 30 \, M\Omega \)). Therefore, more energy is needed for the operation. As a result, the DC output voltage range has also increased in the system. Proper measurement is required to obtain these stray resistances and capacitances value, but absolute values are impossible to be measured in real situation. Precaution is done to avoid unnecessary error and is according to the minimal value of \( pF \) range stated in [10], so that the parasitic value is not affected the \( C_s \) value. For example, when the parasitic across the \( C_s \) is chosen to be \( \frac{1}{100} \) of the \( C_s \), (i.e: \( C_{p3}=0.05 \, pF \)). Results have shown a wider detection range with increasing in sensitivity. In contra, power dissipation has also increased. These analyses and results were supported in [15].

### 4. CONCLUSION

In summary, this work has shown a proposed differential capacitive sensing with parasitic impedance. It is important to integrate the real situation into design consideration. Result has shown an increase of power dissipation to the system. A small increasing of 0.03868 mV/\( f \)F and 0.99984 were shown for sensitivity and R-squared values respectively at the output voltage, with parasitic components integration. The capacitance detection range is 1.0 – 6.0 pF. In future, a proposed solution can be done to improve points of detection of output voltage capacitance sensing across frequencies, by properly setting the values of component involved such as resistance and capacitance of the differential capacitive sensing.
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