Novel Tunnel-Contact-Controlled IGZO Thin-Film Transistors with High Tolerance to Geometrical Variability

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Thin insulating layers are used to modulate a depletion region at the source of a thin-film transistor. Bottom contact, staggered-electrode indium gallium zinc oxide transistors with a 3 nm Al2O3 layer between the semiconductor and Ni source/drain contacts, show behaviors typical of source-gated transistors (SGTs): low saturation voltage \( V_{D_{\text{SAT}}} \approx 3 \text{ V} \), change in \( V_{D_{\text{SAT}}} \) with a gate voltage of only 0.12 \( \text{V V}^{-1} \), and flat saturated output characteristics (small dependence of drain current on drain voltage). The transistors show high tolerance to geometry: the saturated current changes only 0.15x for 2–50 \( \mu \text{m} \) channels and 2x for 9–45 \( \mu \text{m} \) source-gate overlaps. A higher than expected (5x) increase in drain current for a 30 \( \text{K} \) change in temperature, similar to Schottky-contact SGTs, underlines a more complex device operation than previously theorized. Optimization for increasing intrinsic gain and reducing temperature effects is discussed. These devices complete the portfolio of contact-controlled transistors, comprising devices with Schottky contacts, bulk barrier, or heterojunctions, and now, tunneling insulating layers. The findings should also apply to nanowire transistors, leading to new low-power, robust design approaches as large-scale fabrication techniques with sub-nanometer control mature.

Rapid advances in high-rate large-area fabrication techniques\([1–4]\) are enabling new ways of realizing electronic devices. Along with a number of groups, we believe that revolutionary transistor design\([5–9]\) presents opportunities that are inaccessible to evolutionary developments, in terms of energy efficiency, gain, and large-area manufacturability. To this end, we propose thin-film transistors (TFTs) inspired by the principle of deliberately using blocking contacts. Significant application benefits, e.g. tolerance to manufacturing variability and superior gain at low drain–source voltages, can be derived using engineered potential barriers at the source of thin-film staggered-electrode transistors. Such structures, known as source-gated transistors (SGTs) have been proposed in numerous material systems\([10–15]\) and are an attractive alternative to conventional device structures due to their potential for ultralow power and robust operation\([16–19]\). As the current in these SGT structures is controlled by the source barrier region, the device operating speed is usually close to an order of magnitude lower than conventional transistors of identical geometry. If ionic oxide semiconductors are used as active layers, high performance can still be achieved due to the material’s intrinsic carrier mobility, which is more than an order higher than amorphous silicon\([20]\). Moreover, the SGT can be more aggressively scaled without deteriorating its electrical characteristics\([16,19]\).

The role of the barrier at the source is twofold: it induces saturation of drain current at low drain voltage\([11,21,22]\) and pins the potential at the edge of the source to a value dependent on gate voltage. Consequently, the injection of charge from the bulk of the source electrode is by processes which result in low activation energy\([21,23]\) and high intrinsic gain\([16,18,19,24]\). The barrier at the source of an SGT device is typically realized by a Schottky contact, but it is also possible to realize a similar effect by other means\([24–26]\).

Nanometer- and sub-nanometer-scale conducting or semiconducting layers, such as graphene\([40]\), CNT\([41]\) and TiSi\(_2\)\([29]\) have been used at the contacts of TFTs\([27–31]\) for gaining a better Ohmic behavior\([44]\) or tunneling behavior\([40,41]\). Likewise, nanometer-scale insulating layers also have been widely used as the gate insulators for deep sub-micrometer transistors and memory devices based on floating-gate principles\([32,33]\). Moreover, these insulting films have also been used as contact barriers against dopant diffusion to reduce short-channel effects of polysilicon TFTs\([34]\) and to allow depinning of the Fermi level at the metal–semiconductior interface for higher drain current\([32–41]\). The choice of insulator is responsible for the efficiency of charge transport across the contact\([43]\). Multiple insulating layers can be used to create a dipole which further contributes to barrier lowering, and similar techniques are applicable for organic devices\([33]\).

The application of a thin insulating film at the source contact in SGTs had been theorized over a decade ago. Such tunnel-contact devices are predicted to have smaller temperature
coefficient than Schottky-contact devices. In this communication, metal–insulator–semiconductor contacts whose properties would change from rectifying to Ohmic in the absence of the thin insulating interlayer will be referred to as tunnel contacts.) However, tunnel-contact SGTs have not been explored experimentally thus far. Combining indium gallium zinc oxide (IGZO), a leading amorphous oxide semiconductor, at the channel, with aluminum oxide (Al$_2$O$_3$) thin layers at the source and drain contacts, we report on the first tunnel-contact oxide SGTs that exhibit low-voltage saturation for energy efficiency, and tolerance to geometrical variations for robust operation in large-area circuits. To our knowledge, this is the first use of thin insulators at the contacts to deliberately induce an energy barrier leading to the effects described above. While the challenges of accurate large-area deposition of nanometer-scale films at a practical cost cannot be overlooked, large-area manufacturing techniques for such films are becoming increasingly viable allowing the integration of the proposed devices into conventional manufacturing flows.

Devices were fabricated in a top-gate, bottom-contact architecture using standard photolithography and were operated in a common-source configuration. Figure 1a shows the schematic cross-section including the two main features of SGTs: i) a thin barrier layer of Al$_2$O$_3$ deposited by atomic layer deposition (ALD) which acts as a barrier between the IGZO channel and Ni source/drain electrodes, and ii) the gate extending over the source electrode (source-gate overlap, S) in addition to covering the channel region as in the conventional TFTs. Figure 1b focuses on the region of interest at the source and illustrates the device’s equivalent circuit which will be discussed later. Figure 1c shows the typical device layout with large variation of source-gate overlap, S (1, 9, and 45 µm), and source–drain gap, L (2, 6.5, and 50 µm). The substrate photograph is also shown in Figure 1c. The width, W, of all devices was 110 µm. Several devices with S = 9 µm were tested to breakdown, and their microscopy images can be found in Figure S1 (Supporting Information).

Plots in Figure 2 confirm that the fabricated devices here operate, in the first order, as SGTs. Figure 2a,b shows that the drain current $I_D$ only doubles when S is increased fivefold. Next, as shown in Figure 2b,c, $I_D$ increases very little, only 0.15×, when L is increased 25×. These are consistent with the properties of SGTs that the device is controlled by the source region (S) and is less sensitive to L.[20,48,49] This is an advantage of conventional TFTs where the drain current is affected by the shorter channel and thus is susceptible to device-to-device fluctuations due to fabrication variability.[56,47] Moreover, Figure 2b,c shows that the devices with longer channel has a higher saturated current than those with shorter channel, which is the opposite of what is observed in a traditional TFT. This is attributed to the 2D potential distribution in the semiconductor owing to the staggered-electrode structure. This unusual effect has also been observed in other material systems.[45,48] The output characteristics in Figure 2a–c show low saturation voltage, $V_{DS, SAT}$, around 3 ± 1 V. It is noted that the $V_{DS, SAT}$ is similar for all S and L. The change in $V_{DS, SAT}$ with gate voltage extracted from these plots, 0.12 V V$^{-1}$, is also independent of S and L (see Figure 2d,e).

Moreover, Figure 2a–c shows very flat output curves indicating a low drain voltage dependence in saturation. Conversely, devices fabricated without the thin insulating layer show poor saturation (see Figure S2 in the Supporting Information).

Next, Figure 2g reveals a large negative threshold voltage, and in the off state, gate leakage becomes the dominant proportion of drain current, as a large potential difference, as high as 30–35 V is applied between the accumulation layer in the semiconductor and the gate electrode, across the <100 nm gate insulator. The depletion-mode, normally-on operation of the device indicates a channel conductivity much higher than the ideal. The deposited IGZO films have a carrier concentration $\approx 10^{19}$ cm$^{-3}$ with Hall mobility $\approx 10$ cm$^2$ V$^{-1}$ s$^{-1}$ and they have been previously incorporated as the active layer in bottom gate TFTs.[49] However, as shown in this work, these films become too conductive when used in top gate transistors. Several causes for this behavior are plausible, most likely related to the condition under which the semiconductor–insulator interface, critical to device behavior, forms. The ALD growth step for the Al$_2$O$_3$ gate insulator requires subjecting the already-deposited IGZO layer to vacuum as well as chemical precursors which may change the properties of the surface. Most notably, this may result in the formation of indium nanoparticles[50] and/or the adsorption of OH$^-$ at the surface of the semiconductor, with the net effect of increasing the conductivity of the IGZO layer at this interface. Inserting a barrier SiO$_2$ layer between IGZO and ALD Al$_2$O$_3$,[51] for instance, may improve the device operation. This initial study was not intended to optimize transistor characteristics, and transfer curves are secondary to the device operation in SGTs. Moreover, recent studies have shown that contact-controlled, source-gated transistors can be reliably made even with semimetals,[19] with the requirement that the active layer geometry and contact barriers are optimized; and that contact engineering can be reliably used to switch off devices with highly conductive semiconductor layers.[52] In the present case, this is evident when comparing transfer characteristics of devices with contact tunneling layers (Figure 2g) with those of devices with conventional, Ohmic metal–semiconductor contacts (Figure S2, Supporting Information): the presence of the contact barrier produces significantly larger current modulation as the device is turned off. Large negative gate voltages are still required to turn off the devices, and this has an adverse effect on the off-current, as the gate leakage is seen to sharply increase below $V_G = -25$ V. Transfer curves showing the impact of geometry, as well as an analysis of gate leakage current, are found in Figure S3 (Supporting Information). The gate leakage is largely unaffected by source area, yet the long channel device produces a noticeably larger leakage current than short channel transistors. This may be linked to the fact that in source-gated transistors, most of the applied drain–source voltage is dropped on the source depletion region, resulting in the channel being at a potential at close to $V_D$ over its whole length.[53] A longer channel effectively increases the area over which a large potential difference is seen across the gate insulator, augmenting gate leakage at high absolute values of $V_G$.

The device operation and the influence of the various equivalent components in different biasing conditions is exemplified by the qualitative band diagram and the schematic circuit diagram presented in Figure 3 and Figure 1b, respectively. Under
no applied bias, as shown in the horizontal and vertical cross section of device in the top left and bottom left panels, the thin insulating layer between the metallic electrodes and the semiconductor effectively create blocking contacts. Applying a positive gate bias and a small positive $V_D$ result in the band bending (top middle panel) and the flow of a small drain current, whose magnitude will be controlled by the applied drain bias and its distribution across the two contact barriers and semiconductor layer. As shown in Figure 1b, when a potential is applied across the source and drain tunnel barriers, $D_p$, an accumulation layer is formed at the semiconductor–gate insulator interfaces, with resistance, $R_{CH}$, in the gap between the source and the drain, with an incremental resistance (i.e., per unit length of the accumulation layer in the x direction), $r_{\text{ACC}}$. The drain current saturates at a drain voltage, $V_{D,\text{SAT}}$, which, for the tunnel-contact SGTs, can be defined as $(C_i/(C_i + C_T + C_S)) (V_C - V_T) + k$ where $C_i$, $C_S$, and $C_T$ are the capacitances for the gate insulator, the depleted semiconductor, and the tunnel layer, respectively, and $V_C - V_T$ is the effective applied gate voltage and $k$ is a material-dependent constant.

When the drain–source bias exceeds $V_{D,\text{SAT}}$, the semiconductor layer pinches off at the edge of the source closest to the drain (point A in Figure 1b)\cite{10,11,21} due to an expanding depletion region in an effectively reverse-biased source-barrier layer.
semiconductor junction. This condition is illustrated by the band bending at the interface of active layer and gate insulator in the bottom middle panel of Figure 3. It has been previously observed that the semiconductor can be fully depleted close to the source,[54,55] a phenomenon which allows for hot electron generation and transport at high effective mobility above the conduction band edge states to the drain.[56] Between point A and the edge of the source, the existence of a potential division across the capacitances $C_S$ and $C_T$, results in the majority of $V_{D_{SAT}}$ being dropped across the depleted semiconductor as

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**Figure 2.** a–c) Typical output characteristics for devices with barrier layer thickness $t_b = 3$ nm, demonstrating SGT behavior: low voltage saturation, flat saturated characteristics, minimal dependence of saturated current on $L$, dependence of drain current on source length $S$, and current crowding at low $V_D$ due to contact effects. d–f) The dependence of saturation voltage on gate voltage does not change significantly with geometry or temperature. g) Transfer curves show a negative threshold and gate leakage dominates transistor off current at high reverse gate voltage; h) transfer characteristics show moderate temperature dependence. i) Gate leakage depends weakly on temperature.
C_S << C_T, indicating a high-field operation. Since only a small proportion of V_D,SAT is dropped across the tunnel diode, we expect its I–V characteristics to control the current. Here, the current injected from the edge of the source into the depletion region dominates and this is conventionally defined in SGTs as mode I operation.[21]

In the bulk area of the source which is overlapped by the gate (Figure 1a), however, the insulator interface is accumulated due to the applied gate potential. This condition is illustrated by the band bending at the interface of the active layer and the gate insulator in the bottom right panel in Figure 3. This accumulation layer is essential for charge transport from the bulk of the source towards the drain through a distributed resistor network which accounts for the accumulation layer resistivity, r_ACC, semiconductor layer resistivity, r_SC, and diodes, D_T (Figure 1b).[11,19,21,33] Here, the current injected from the bulk of the source dominates and this is conventionally defined in SGTs as mode II operation[21]. Crucial for the operation of the device is a relatively low value of r_SC, which results in a significant proportion of the accumulation layer potential being applied to the thin barrier, making it able to sustain a large current density. However, Al2O3[57,58] and SiO2[59,60] films of 2–3 nm thickness can tolerate significantly higher current density than that observed for the present devices, for applied potentials in the range of a few volts. Thus, we conclude that in the bulk of the source, the tunnel layer is effectively transparent, and the current injected from the bulk of the source is controlled by the resistive network described in Figure 1b, which is dominated by the vertical resistance of the semiconductor layer pinned at voltage V_D,SAT at point A.

Having described the device operation, the performance of the fabricated devices is further examined for their SGT properties. For V_D < V_D,SAT, the semiconductor is not pinched off at point A, and the current injected from the source obeys the I–V characteristic of the source barrier, hence the s-shape of the output curves at low V_D (Figure 2a–c). To illustrate this behavior further, we plot families of output curves from three devices with different source lengths (1, 9, and 45 µm) in Figure 4a, on a semilogarithmic scale to account for the difference in drain current magnitude.

An exponential dependence is observed at low V_D, indicating turn-on of the contact barrier as the potential is increased. While somewhat detrimental to the speed of logic circuits, the sublinear output curves at low V_D is of no consequence in analog designs which typically operate in saturation. Of note in Figure 4a is also the independence of V_D,SAT on S for a given
This behavior is explained by the pinch-off mechanism which involves exclusively the edge of the source. Moreover, the $S = 1 \mu m$ device injects only in Mode I and the potential across the tunnel barrier is small, hence a low current is produced. In longer $S$ devices, Mode II injection with much higher current dominates, and a low contribution from the far side of the very long source due to the resulting resistive voltage drop results in minimal dependence of $I_D$ on $S$ [21,45,53] (see also Figure 1b).

As previously shown in Figure 2, the output curves show the typical ‘current crowding’ non-linear low-voltage behavior of forward-biased non-Ohmic contacts, which have been reported in numerous devices, e.g.[61] Interestingly, the diode-like characteristic observed at low $V_D$ shows a very small dependence on $V_C$. Figure 4b shows the sublinear $I$–$V$ characteristics at low $V_D$. Here we plot on the same graph the output ($I_D$ vs $V_D$, $V_C$ fixed), transfer ($I_D$ vs $V_C$, $V_D$ fixed), and diode ($I_D$ vs $V_C = V_D$) characteristics, where the fixed potential is 5 V, relative to the source. We can see that the diode characteristic follows the transfer curve at high voltage, and the output curve at low voltage, indicating that the low-voltage drain current is exclusively controlled by the applied drain bias and is independent of gate bias. This effect is seen in all the families of curves in Figure 2a–c, in which, before saturation, the plot follows the same envelope, linked to the capability of the source barrier to deliver current at a given bias.

To conclude the discussion relating to Figure 4b, we examine the diode curve obtained for the same device after being subjected to $V_D > 8$ V (dotted line). This high voltage leads to permanent failure of the barrier layer, at values consistent with measurements on MIM structures[62] (see Figure S4 in the Supporting Information). The result is a behavior closer to that of Ohmic contacts, and is attributed to dielectric breakdown at the edge of the source, removing the possibility of pinch-off at point A (Figure 1b). It is reasonable to assume that, given the relative sizes of source and drain contacts, a similar barrier layer failure occurs at the drain contact.

A characteristic of Schottky-barrier SGTs is their ability to produce large intrinsic gain, $A_V = \frac{g_{m}}{g_{o}}$ due to the very low $g_{o}$ which can be obtained with suitable device optimization, where $g_{m} = \frac{dI_D}{dV_C}$ is transconductance and $g_{o} = \frac{dI_D}{dV_D}$.
is output conductance. Intrinsic gain as high as ~85 for a-Si
Schottky-barrier SGTs[63] and over 1000 for polysilicon Schottky-
barrier SGTs[16] has been reported. Here, the intrinsic gain is a
modest ~20. This can be improved by reducing both the gate
insulator and semiconductor thicknesses, thereby increasing
$g_o$. $g_o$ is small but non-negligible in the operating range of $V_C$
(Figure 2a–c), although at very high gate bias, these transis-
tors show negative $g_o$ due to the 2D potential distribution in
the semiconductor.[48] It follows that, for a limited span of
$V_C$, a very low $g_o$ could be achieved. $g_o$ may be further improved by
field relief strategies, such as a source-metal overhang.[12,13]

For the present devices, we can calculate $γ ≡ C_s/(C_s + C_T + C_{Tiel})$

0.23 (V V$^{-1}$), which is much smaller than the value of unity
specific to conventional FETs, but significantly larger than the
measured $\text{d}V_{D, SAT}/\text{d}V_C = 0.12$ (Figure 2d–f).[16,63] In Schottky
barrier SGTs, the measured value is often larger than the cal-
culated value, especially when the pinch-off at point A is weak
due to either a low Schottky barrier height, or an inability to
easily deplete the semiconductor–insulator interface due to fab-
ication practicalities. In the case of tunnel-contact SGTs shown
here, the cause for the unusually low measured value is likely
to be linked to the turn-on characteristic of the source diode
and the resulting shape of the output characteristic. In practice,
the curves saturate not when the calculated $V_{D, SAT}$ is reached,
but rather at the bias condition at which the resistive network
in the source area of the semiconductor begins limiting the
current, as opposed to the source diode (Figure 1b). Designing
the devices with no tunnel layer at the drain contact and with
thinner source tunnel layer should diminish the s-shape of the
output curves and result in better agreement between measured
$\text{d}V_{D, SAT}/\text{d}V_C$ and theoretical ($γ$) values.

Devices with thinner, 2.5 nm barrier layers were also
fabricated, and the output characteristics are compared in
Figure 4c,d. For both barrier layer thicknesses, we see the
same behavior of the exponential current at low $V_D$, and its
independence of gate bias. The use of a thicker barrier layer
reduces the drain current only by half, indicating that direct
tunneling may not be the principal charge injection mecha-
nism. This is consistent with the model proposed in Figure 1b.

Table 1. Structural and electrical characteristics of source-gated transistors with different barrier types ($t_i$, insulator thickness; $t_s$, semiconductor thickness; $t_o$, tunnel insulator layer thickness; $\varepsilon_i$, insulator permittivity; $\varepsilon_s$, semiconductor permittivity; $S$, length of source contact overlapped by the gate; $\phi_{0B}$, effective zero-bias Schottky barrier height at the source contact; $t_p$, doped barrier layer thickness; $x_o$, extension of doped layer over the edge of the source contact into the source–drain gap; $N_o$, doping concentration in the doped barrier layer).

| Parameter | Tunnel-barrier SGT (TSGT) | Schottky-barrier SGT (SBST) | Bulk-barrier and heterostructure SGT (BUSGT) |
|-----------|--------------------------|----------------------------|-------------------------------------------|
| Barrier realized by | Thin insulating layer at source contact | Choice of source contact metal | Doping or heterostructure formation |
| Effective barrier height range | High | Low | High |
| Control over effective height of barrier | Difficult | Moderate | Moderate |
| Off-current | Low | Low | Low |
| On-current | Moderate | Low | High |
| Transconductance | Moderate | Low | High |
| Output conductance | Low (with field relief) | Very low (with field relief) | Potentially low (with field relief) |
| Temperature coefficient of drain current | Low | Moderate | Potentially low |
| Threshold tuning | Bulk semiconductor doping, gate work function | Bulk semiconductor doping, gate work function | Doped layer parameters, gate work function |
| Principal design parameters | $t_i$, $t_s$, $\varepsilon_i$, $\varepsilon_s$, $S$ | $t_i$, $t_s$, $\varepsilon_i$, $\varepsilon_s$, $S$, $\phi_{0B}$ | $t_i$, $t_s$, $\varepsilon_i$, $\varepsilon_s$, $x_o$, $S$, $N_o$ |

Figure 4e illustrates a comparatively high dependence on
temperature of the current injected across the 3 nm barrier for
the same low drain voltages (i.e., the current doubles for a 30 K
temperature increase), which is again inconsistent with direct
tunneling at the contact. These results suggest the presence
of an effective potential barrier at the contact that is reduced
by the applied bias (Figure 3). Likewise, the transfer curves in
Figure 2h show an approximately five-fold increase of drain
current upon a 30 K increase in temperature. The gate leakage
current less than doubles with a 30 K increase in temperature
(Figure 2i). This further supports our stated hypothesis that
barrier-layer tunneling is not the principal current control
mechanism in these devices, as it would result in a very low
temperature dependence. A space charge induced tunneling
model coupled with Ohmic transport in the semiconductor
would be a plausible explanation of the observed characteristics.

To put the characteristics of the proposed devices in context,
we refer to Table 1, which synthesizes the structural differences
and their impact on electrical behavior for contact-controlled
devices with: Schottky barriers[10] (traditional SGT), bulk or
heterostructure barriers,[25,26] and the proposed tunnel bar-
riers. Choosing the most suitable design will depend in equal
measure on the application and on the practicalities of fabrica-
tion (e.g., ability to produce reliable nanoscale contact barrier
layers on a large area for the tunnel devices, or solvent orthog-
nality for solution-processed heterojunction-barrier devices).
We highlight two important differences to conventional
(Ohmic-contact) TFTs: first, the temperature coefficient of drain
current can vary dramatically based on the choice of source bar-
rier and dominant injection mode; second, source area is an
important design parameter in all three types of devices.

In conclusion, contact-controlled IGZO SGTs were fabricated
and characterized. For the first time, pinch-off at the source was
induced by interposing a nanometer-scale Al$_2$O$_3$ layer between
the Ni source and drain contacts and the semiconductor.
These devices behave qualitatively as source-gated transistors,
with low saturation voltage, flat output characteristics, and
tolerance against geometrical variations affecting the current
flow. The behavior of the fabricated devices deviates from the
theory of Shannon and Balon,\textsuperscript{[24]} due to the significantly more complex, 2D injection and transport processes governing these devices, in contrast to a 1D tunnel diode: the current is not limited by the tunneling capability of the thin insulating layer at the contact, but by the electrostatics of the semiconductor layer in the source region, potentially with some assistance from the work function difference between the metal contact and the semiconductor.

As discussed above, optimizations of the channel layer and source contact area to maintain a constant potential at point A in Figure 1b would be expected to increase the gain.\textsuperscript{[11–13]} Maximizing this figure of merit improves energy efficiency and logic gate noise margin\textsuperscript{[13,18,19]} and may reduce analog circuit complexity.

The suitability of such devices for high-performance, high-throughput thin-film electronics is supported by recent advances thin layer deposition techniques with precise control over large areas, such as atomic layer deposition. The chosen material system has several advantages: carrier mobility is superior to a-Si with potentially higher switching speed; achieving a high-quality Al2O3 tunnel oxide/IGZO semiconductor interface is practical with current technologies; and the contact-controlled transistor on-current is robust against potential bias instability. Moreover, the potential replacement of the contact-controlled transistor on-current is robust against potential bias instability. The potential replacement of the semiconductor layer with an atomically thin material from the transition metal dichalcogenide family (WS2, MoS2, etc.) would be of great interest for next generation, highly efficient electronic devices. Finally, a similar device design may be used in nanowire transistors, where deliberate growth of insulating shells should lead to source-gated behavior, with large gain and tolerance to geometrical variations. We envisage this new architecture as a very promising opportunity for analog signal processing and biasing circuitry for low-power sensors made by low-cost and large-area fabrication.

**Experimental Section**

Fabrication: Top-gate, bottom-contact transistors were fabricated on Corning Eagle 2000 glass (see Figure 1) by contact photolithography. The source and drain bottom contacts were defined by lift-off using AZ5214E photoresist and 55 nm Ni deposited by electron beam evaporation (custom system, Univex) at a rate of $\approx 2 \ \text{Å} \text{s}^{-1}$. A significant amount of distortion (bowing) is noticed in the channel of devices with $L = 2 \ \text{μm}$. This is a result of the poor adhesion of the photoresist to the substrate in that area, with negligible effect on the operation of the present devices.

Next, using the mask for the active layer, the barrier layer and the semiconductor island were defined by photolithography, in a single lift-off step: following this definition, the barrier Al2O3 layer was deposited by atomic layer deposition using a Savannah 100 ALD (Cambridge NanoTech, Inc.) at 150 °C using trimethylaluminum and deionized water for 25 and 30 cycles producing barrier layer thicknesses of 2.5 and 3 nm, respectively. Ideally, the optimal device would have an Ohmic drain contact, but this was impractical to realize and test with the current device layout and process. The active layers (35 nm IGZO) were deposited using RF magnetron sputtering from an In2O3:Ga2O3:ZnO $(1:1:1)$ target in an argon atmosphere at a pressure of $7 \times 10^{-3} \ \text{mbar}$. Due to the comparatively high temperature experienced during the ALD process, the photoresist lift-off resulted in tearing of the edges of the defined patterns (Figure 1c), well outside the active device area, but with potential bearing on device-to-device drain current uniformity.

Al2O3 was deposited by ALD using the same deposition condition as the barrier layers (1000 ALD cycles), achieving a thickness of 98 nm and a refractive index of $1.62$ at $\lambda = 633 \ \text{nm}$ to serve as the gate insulator, and via holes were defined, then etched for $\approx 5 \ \text{min}$ in 80% H3PO4 at $\approx 70 ^\circ \text{C}$ in the contact pad area.

Finally, top gate contacts and access pads for source and drain, consisting of 10 nm Ti and 80 nm Au were deposited by the same e-beam lithography technique, and defined by photolithography.

Characterization: Device characterization was performed manually, in air, on a Wentworth semiconductor prober and using the Keysight B2902A precision SMU, connected to a PC via USB. Electrical connections were made through BNC cables. The drain was connected to Channel 1, the gate to Channel 2, and the source to Channel 1 ground. All measurements were performed with the source grounded, and all analyses and discussion imply common-source operation of the transistor. A heated chuck was used to set the substrate temperature.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

amorphous oxide semiconductors, IGZO, source-gated transistors, thin-film transistors, tunnel barriers

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