MuPix10: First Results from the Final Design

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Many years of research and development of High Voltage Monolithic Active Pixel Sensors (HVMAPS) have culminated in the final design for the Mu3e pixel sensor. MuPix10 is a fully monolithic sensor with an active pixel matrix size of $20 \times 20 \text{mm}^2$ produced in the 180 nm HV-CMOS process at TSI Semiconductors. The pixel size is $80 \times 80 \mu\text{m}$. Hits are read out using a column-drain architecture and sent over up to four serial links with up to $1.6 \text{Gbit s}^{-1}$ each. By means of DC/DC converters and exclusive usage of on-chip biasing, MuPix10 is fully operable with a minimal set of electrical connections. This is an integral requirement by the Mu3e experiment since it enables the construction of ultra-thin pixel modules with 1% of a radiation length per layer. First results from lab characterisation and testbeam campaigns are presented.

**KEYWORDS:** HV-CMOS, HVMAPS, particle tracking detectors, monolithic active pixel sensors

1. Introduction

The Mu3e experiment [1] is searching for the lepton flavor violating decay $\mu \rightarrow eee$ with an unprecedented sensitivity of $1 \times 10^{16}$ decays. To achieve the experimental goal, an ultra-thin pixel tracker with 1% of a radiation length per layer is being built, which handles rates up to $10^9$ muon decays per second.

The High Voltage Monolithic Active Pixel Sensor (HVMAPS) technology [2] was chosen to enable the construction of this detector. The combination of drift based charge collection and integrated readout on the same chip allows to build fast pixel detectors with an excellent fill-factor. Furthermore, the small active depletion region allows thinning of the sensors to 50 $\mu\text{m}$ thickness. Using commercially available processes, the MuPix chips [3–7] have been developed, culminating in the first large scale HVMAPS sensor.

With the technological challenges solved, the next step is the construction of pixel sensor modules. The MuPix10 [8] chip fulfils the specifications to build fully operational Mu3e tracker modules. This includes the final sensor size and a minimal chip interface. In the following, the requirements imposed by the module integration and their implementation on the MuPix10 are described. First results from testbeam measurements and the characterisation of key features are presented.
2. Mu3e Pixel Tracker Modules

![Schematic representation of a module, integrating four long ladders.](image)

![Layer stack of the HDI. PI=polymide, Al=aluminium.](image)

**Fig. 1.** CAD drawing of an Mu3e tracker module and the material stack of the HDI. [1]

The smallest mechanical unit of the Mu3e tracker [1] is the so-called ladder. It is formed by a High Density Interconnect (HDI) circuit, which provides the electrical connections and mechanical support for 6 MuPix sensors for the inner layers of the detector and up to 18 sensors for the outer layers. The HDIs are produced in a lithographic process by LTU Ltd. (Ukraine) [9], who offer a thin aluminium-polyimide technology which allows to use Single-point Tape Automated Bonding (SpTAB) [10] for the sensor-HDI interconnection. The material budget of the HDI sensor stack, including adhesives, sums to 1.15 % of a radiation length. This material stack has only two aluminium layers for the HDI as depicted in figure 1(b). These two layers provide power and the high-voltage bias, as well as control and data lines for the chip, which are realised as differential pairs.

The ladders are electrically divided into two halves and the MuPix sensors are read out from both ends. Every half ladder provides two differential buses which are used for clocking and the configuration of the sensors. The sensors are read out with 9 differential data lines to both ends at a bandwidth of 1.25 Gbit s⁻¹ per line, for the inner layers 3 per chip, in the outer layers 1 per chip. Power and ground are supplied globally, the sensors are connected in parallel. As the chips do not offer regulators for the 1.8 V nominal operating voltage, voltage gradients between sensors due to ohmic losses are avoided in the design of the power lines. For the outer layers up to 30 W have to be provided through this power grid, motivating a rigorous minimisation of the configuration and readout interface to allow for wider power traces.

3. The MuPix10 chip

In the design of MuPix10, all requirements imposed by the module framework have been implemented, leading to the first full-scale and module-ready MuPix prototype. The chip features two sets of aluminium bonding pads. One with a pad size of 200 × 100 µm² meeting the requirements of the HDI interface for SpTAB. The second, wedge bond pads of 90 × 150 µm² size, doubling the SpTAB pads and adding further signals, which help with the initial characterisation in the laboratory and offer alternative ways for the chip configuration and monitoring.

MuPix10 comprises a matrix of 256 × 250 pixels with a size of 80 × 80 µm², with a total active...
area of $20.48 \times 20.00 \text{ mm}^2$. The size of the die is $20.66 \times 23.14 \text{ mm}^2$, see figure 2. This includes the chip guard ring which is surrounded by an 11 $\mu$m seal ring to minimize dead space between chips on a ladder.

**Fig. 2.** The MuPix10 layout: Active matrix at the top and periphery at the bottom. The color change in the active matrix is a feature of the routing scheme, see section 4.5

![Diagram](image)

**Fig. 3.** A functional description of the MuPix architecture. From the in-pixel electronics with injection capability to the discriminator and readout infrastructure in the periphery. [1]

The architecture of MuPix10 follows the standard MuPix approach depicted in figure 3. The deep n-well contains a folded cascode amplifier with a PMOS input transistor and a source follower as line driver, implemented as floating logic. An additional supply voltage of nominally 1.2 V is required by the amplifier, which is not provided by the HDI. Therefore a voltage regulator is implemented to generate this additional voltage level from the 1.8 V supply, see section 4.2. The pixel line driver transmits the amplified signal via a point-to-point connection to the periphery to its digital partner-cell. This signal is AC-coupled to two parallel comparators which allow to apply different threshold schemes for hit detection and time sampling. Two timestamps are stored for each hit. The rising edge is sampled with 11 bit in 8 ns bins (TS1). A second, 5 bit, timestamp (TS2) is stored on the crossing
of the falling edge which allows to measure a Time-over-Threshold (ToT) by calculating the difference of the two timestamps. The sampling speed is adjustable to allow for a variable dynamic range. To ensure a correct measurement of the ToT and to maintain the level of chronology, a delay circuit is implemented which inhibits the readout of the hit after first registration for a constant time, see section 4.4. The chip is split into 3 sub-matrices with 84, 86 and 86 columns, respectively, which are read out in a column-drain fashion. The serialised and 8b10b encoded hit data is sent out over a differential link with a nominal bandwidth of 1.25 Gbit s$^{-1}$. There is one link per sub-matrix and an additional fourth multiplexed link which allows to send out data of all sub-matrices in a combined stream. Using the individual links a, theoretically, total rate of 90 MHit/s can be transmitted.

All control voltages are generated on chip, including the discriminator thresholds, making the chip operable with a minimal set of connections. To allow monitoring from outside, a programmable ADC can measure key voltages on the chip and send out the measured values via the data link to provide crucial information e.g. the threshold levels and the chip temperature.

4. First Results

In the following, preliminary results from the MuPix10 commissioning and tests of key features are presented.

![A MuPix10 chip mounted on a test PCB.](image1)

![MuPix10 hit map observed with the DESY electron beam.](image2)

**Fig. 4.** MuPix10.

4.1 Commissioning

MuPix10 has been successfully commissioned in the laboratory. It is fully configurable and works reliable with the nominal reference clock of 125 MHz, providing stable differential data links at 1.25 Gbit s$^{-1}$. At full readout speed problems with the data integrity have been observed. Therefore, it is currently throttled by a factor of 2. The breakdown of the deep n-well diode was measured to be around $-100$ V which exceeds the minimum requirement of $-60$ V. For a 200 $\Omega$ cm substrate this provides a depletion zone of $\approx 40 \mu m$, which means there is no inactive bulk material for 50 $\mu m$ thin chips. For testbeam use, a preliminary optimisation of the chip settings was performed, based on
knowledge from previous chip generations and qualitative investigations with radioactive sources ($^{90}$Sr and $^{55}$Fe). With these settings and all supply voltages provided externally, the power consumption of the chip is around 190 mW cm$^{-2}$, normalised to the active area. Figure 4 shows a MuPix10 hitmap obtained with a 3 GeV electron beam at DESY. With the large area, the core of the DESY beam is fully confined in the matrix. Based on the obtained data, the efficiency and time resolution is currently being studied.

4.2 VSSA Regulator

The architecture of the regulator is sketched in Figure 5(a). It is a linear series regulator which uses a differential amplifier to adjust the VSSA voltage level to a configurable reference value (vss_ref). As the regulator acts as a self-adjusting voltage divider, the current drawn by the 1.2 V network will dissipate additional heat in the regulating transistor leading to a power penalty. So far no detailed study of the regulator has been performed, however, an ad-hoc attempt to run the chip with a single supply voltage, was performed successfully. Figure 5(b) shows a scan of the regulator reference voltage. The VSSA level shows a linear behaviour with a range from 0 V to 1.4 V with the nominal working point of 1.2 V well covered. Further, the corresponding changes in the supply current are plotted. As the amplifier is the only circuit using the VSSA voltage, the change in current represents the turn-on of the amplifier. Only for voltage levels above 1 V the amplifier can be considered fully working. For the used settings, the total power consumption was measured to be 200 mW cm$^{-2}$ to 210 mW cm$^{-2}$ which corresponds approximately to a 10% power increase due to the regulator usage. With this, the Mu3e requirement of the sensor power consumption of $< 350$ mW cm$^{-2}$ is very well met.

![Functional sketch of the linear regulator](image1)

![VSSA voltage and supply current plotted for a scan of the regulator reference voltage (vss_ref)](image2)

(a) Functional sketch of the linear regulator.

(b) VSSA voltage and supply current plotted for a scan of the regulator reference voltage (vss_ref).

Fig. 5. The VSSA regulator.

4.3 Threshold Tuning

All pixels are connected to two comparators with globally applied thresholds. Due to process variations the threshold behaviour of the comparators will vary and are a source of non-uniformities. In the MuPix10, both comparators are equipped with a 3 bit DAC which allows to set individual thresholds to compensate the variations, the so-called trimming or tuning. Additionally, the pixels have a switch bit, which allows to mute pixels if they are uncontrollably noisy. This feature was tested and a tuning was performed successfully [11].
In this study all pixels have been stimulated with charge pulses corresponding to $3000 \, e^-$, using the injection infrastructure, see figure 3. A scan of the global threshold is performed and the amount of recognised injection pulses is measured. The resulting distribution is fitted with an s-curve function. The mean value extracted from this fit varies for different pixels. The RMS of the mean-distribution plotted in figure 6(b) is a measure of the threshold dispersion. With the application of individual threshold shifts, shown in figure 6(a), the differences of the mean values can be minimised, reducing the dispersion over all pixels.

![Graph](image1)

(a) Linear voltage steps achieved with the 3 bit tuning DAC.

(b) The threshold dispersion before (red) and after (blue) tuning for the full MuPix10 matrix with an equivalent signal of $3000 \, e^-$. 

**Fig. 6.** Results obtained with the threshold tuning method [11].

With this method the threshold dispersion was reduced from 11 mV to 4.8 mV or in electron equivalent from 240 e$^-$ to 75 e$^-$, see figure 6(b). The effect of the tuning on the efficiency still needs to be investigated in testbeam campaigns.

### 4.4 ToT-sampling

As shown with the MuPix8 chip [12, 13] the time resolution of the MuPix sensors can be significantly improved by correcting timewalk by using the ToT information. Although not necessarily required in Mu3e, the precise time information can help to ease tracking in the offline analysis. To provide correctly measured ToT values, while maintaining the data chronology and readout speed, the introduction of a new circuit is necessary.

![Diagram](image2)

(a) Inhibiting the pixel readout for a constant time, after hit recognition.

(b) The delay circuit logic. (The reset circuit is not shown.)

**Fig. 7.** Readout (RO) and timestamp sampling for different pulse lengths using a constant delay.
The solution chosen for MuPix10 is shown in figure 7(a). After the hit is registered, the readout of the hit is inhibited for a constant time. The delay is created by a new analogue delay circuit depicted in figure 7(b). The registered hit enables a current source which charges up a capacitor. The increasing voltage of the capacitor is measured by a discriminating element which switches when its threshold is crossed. This output enables the readout of the pixel cell. The strength of the current source is adjustable and thus the time delay.

Figure 8 shows three measured ToT distributions with different chosen delays. The peak in the end of the spectrum corresponds to the delay time. If the delay time lapsed, but the ToT of the pulse would be even longer, the expiring time of the delay is sampled instead. All pulses longer than the delay are contained in this peak. The dispersion of the peak is caused by variations of the delay time over the chip and is on an acceptable level for the usage in Mu3e. As long pulses correspond to a large signal amplitude, there is no need for a timewalk correction. Hence, the delay time can be reduced below the duration of the longest pulses without losing precision in the correction process.

Fig. 8. ToT spectra obtained for 3 different delay times controlled by the VPTimerDel DAC value.

This shows that the delay circuit is working as intended and the correct ToT sampling is secured. Detailed studies on the performance, sensor variations and possible position dependences of the circuit are under way.

4.5 Signal Line Crosstalk

Crosstalk in a MuPix chip was first observed with the MuPix7 prototype and could be fully attributed to the effect of signal line crosstalk. Other types of crosstalk have not been observed [4]. For MuPix-like chips, all pixels within one column have a point-to-point connection to the periphery which is routed within the same column. Neighbouring lines form a parallel plate capacitor, where the capacitance between those lines scales with the length they are adjacent. Via this parasitic capacitance the two lines are coupled and a signal pulse on one line creates a small crosstalk pulse in the neighbour. If it surpasses the comparator’s threshold, an additional hit is created. The larger the capacitance, the larger the crosstalk pulse. This effect was observed in the MuPix8 chip which featured increasing line lengths to more than 1.6 cm and with this increasing capacitive coupling [14]. For the longest lines of the MuPix8 the crosstalk pulse had approximately 17% of the amplitude of the initial pulse [12]. This gives rise to a 35% chance of crosstalk to both neighbouring lines, creating two additional hits which artificially increases the readout load. The MuPix8 only features 200 pixels within one column, while 50 more pixels are added for the Mupix10, thus further increasing the line length and therefore the crosstalk amplitude and as a consequence the amount of additional hits.
For the MuPix10 design, two metal layers were available for pixel routing. With the usage of the full column width and 125 lines per metal layer, the smallest distance between adjacent lines is the same as in MuPix8. Two strategies were applied in the MuPix10 design to reduce crosstalk as much as possible and make it easily distinguishable from "real" sensor phenomena such as charge sharing. For the latter, neighbouring pixels must not be routed on adjacent signal lines. By choosing an easily recognisable pattern, crosstalk can be identified and removed from the data. In case of one-sided crosstalk, the ToT information helps to identify the crosstalk hit, as the crosstalk pulses will be very short, while the initial signal is large. The second strategy aims to reduce crosstalk by minimising the length two different signal lines are routed in close proximity. With the two metal layers available, the scheme in figure 9(a) allows to limit the direct neighbour length to 1/4 of the maximal length. Following this simple picture and the extrapolation from the MuPix8 results, the new routing scheme reduces the crosstalk amplitude to 5% of the initial pulses amplitude. Therefore reducing the amount of additional hits by crosstalk.

In contrast to MuPix8, the signal line length is not increasing with the row position, but four discrete lengths are chosen to achieve a more uniform behaviour. Also, as a correlation between the total line capacitance and the pixel delays is expected [12]. Figure 9(b) shows the row address self-correlation of within one timestamp cycle. While charge-sharing will only create a broadening of the diagonal, due to the chosen routing pattern, the off-diagonal enhancements are fully attributed to crosstalk and can be easily identified. A first estimation by counting the crosstalk induced patterns and comparing them to the number of all clusters gives a total crosstalk probability of less then 1.5% for the MuPix10.

(a) The MuPix10 routing pattern with exemplary highlighted coupling capacities.

(b) Row address self correlation. Off diagonal elements are enhanced by lowering the displayed max-value.

Fig. 9. Implementation and effect of the crosstalk routing.
5. Summary and Conclusion

MuPix10 was commissioned successfully and works reliably. As it shows no obvious performance degradation considering efficiency and time resolution it is already used as reference layers in the MuPix-Telescope [14]. Key features, such as the new routing scheme, have been tested and perform as expected. It was shown that the chip can be powered with a single 1.8 V supply voltage, with 1.2 V generated by an on-chip regulator. This is an important milestone for the module readiness of the Mu3e pixel sensor. The next step is the production of a multi chip demonstrator.

Detailed studies of the presented features, the sensor efficiency and the time resolution are ongoing and will provide important input for the design of the MuPix11, which is going to be used for the module production. The design of MuPix11 will be very close to MuPix10 and only incorporates necessary fixes and possible performance improvements which are well reviewed and unlikely to cause a failure of the chip as a whole.

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