Design and Implementation of High-throughput PCIe with DMA Architecture between FPGA and PowerPC

Kun Cheng, Weiyue Liu, Qi Shen and Shengkai Liao,

Abstract—We designed and implemented a direct memory access (DMA) architecture of PCI-Express(PCIe) between Xilinx Field Programmable Gate Array(FPGA) and Freescale PowerPC. The DMA architecture based on FPGA is compatible with the Xilinx PCIe core while the DMA architecture based on POWERPC is compatible with VxBus of VxWorks. The solutions provide a high-performance and low-occupancy alternative to commercial. In order to maximize the PCIe throughput while minimizing the FPGA resources utilization, the DMA engine adopts a novel strategy where the DMA register list is stored both inside the FPGA during initialization phase and inside the central memory of the host CPU. The FPGA design package is complemented with simple register access to control the DMA engine by a VxWorks driver. The design is compatible with Xilinx FPGA Kintex Ultrascal Family, and operates with the Xilinx PCIe endpoint Generation 1 with lane configurations x8. A data throughput of more than 666 MBytes/sec is achieved with single PCIe Gen1 x8 lanes endpoint of this design. PowerPC and FPGA can send memory write request to each other.

Index Terms—PCIe, DMA, FPGA, PowerPC, VxWorks, Driver, VxBus

I. INTRODUCTION

For better observation, analysis and feedback, the data of scientific experiments such as Shanghai Synchrotron Radiation Facility(SSRF) and Shanghai Deep Ultra Violation Free Electric Laser(SDUV-FEL) need to be transmitted and processed online in real time [1]. Scientific systems contain data acquisition and processing subsystems, and the different subsystems will sustain Gigabyte per second data rates among them. Depending on the performance specifications of the particular application, FPGA with unique parallel processing and good timing control characteristics is usually used to acquire data from experiments, and PowerPC with powerful computational capacity is sometimes adopted as a host embedded system to process data on-line. However, the bottleneck between the subsystems usually lies in the data transmission link between FPGA and PowerPC. In our instrument, FPGA need to send data to PowerPC at the rate of no less than 500MBps. To solve such problem, we have developed PCI Express(PCIe) as data links.

PCIe is a widely used and reliable high speed data transmission protocol. Xilinx provides FPGA(XCKU040) with PCIe IP core(Gen3) [2]. Freescale provides PowerPC(MPC8641D) with PCIe integrated as a peripheral device [3]. WindRiver supplies VxWorks which contains a Board Support Package(BSP) to compatible with PowerPC. Both FPGA and PowerPC supply users with basic PCIe device. To achieve the highest data throughput while reducing the occupancy of PowerPC, DMA engine is needed to overcome the limitations introduced by the PowerPC scheduling of operating system(OS). [4], [5], [6] implement DMA architectures for PCIe core based on FPGA of Xilinx, however they always cost too much and these architecture usually are limited to a single FPGA device. To conquer these restrictions, we designed and implemented a high-performance and compact DMA engine architecture which is fully compatible with Xilinx FPGA Ultrascal family, together with a custom-designed VxWorks driver based on VxBus. This paper illustrates the DMA engine architecture in FPGA, the VxWorks driver in PowerPC and the handshaking sequence between FPGA and PowerPC. The different payload length transmission are discussed. In this paper, two development kit boards are adopted: KCU105 is for XCKU040(FPGA), and HPCN8641D is for MPC8641D(PowerPC).

II. SYSTEM OVERVIEW OF POINT-TO-POINT PCIe

PCIe is a layered protocol, containing a transaction layer, a data link layer, and a physical layer [7]. The structure of these layers for two different PCIe devices is illustrated in Figure 2. [8]. [7], [8].

The Data Link(DL) Layer is subdivided to include a media access control (MAC) sub layer. The Physical Layer is subdivided into logical and electrical sub layers. The Physical logical sub layer contains a physical coding sub layer (PCS). The PCIe IP core of Xilinx comprises the DL layer and Physical layer and it supplies user with interface which complies with the bus of AXI-4 [9] of transaction layer. It is convenient for users to consider only the transaction layer protocol(TLP) logic to finish PCIe transmission and Message Signaled Interrupts(MSI). The PCIe is a peripheral of the PowerPC and the BSP of the PowerPC contains a basic driver of PCIe, user will need to develop a compatible driver complied with VxBus for PCIe [10].
Three kinds of memory spaces lie in PCIe: Memory Space, Configuration Space and I/O space. We mainly develop PCIe with memory space in this paper. The configuration space contains the PCIe configuration registers, each PCIe device contains 6 base address registers (BAR 0-5), in this paper, only BAR0 is adopted and the memory size of BAR0 is configured as 2K bytes. The version of PCIe IP core is Gen3 in XCKU040 while Gen1 in MPC8641D. In order to match the FPGA and PowerPC, considering the PCIe is downward compatible, the PCIe IP core in FPGA is configured as Gen1.

PCIe Gen1 offers a data link operating at 2.5 Gbps each lane and uses 8B/10B encoding, thus the actual maximum throughput of each lane is 2 Gbps. Additional packet overhead is also included excluding the basic payloads as the structure illustrated in Figure 2.

We denote the maximum payload size with $P_l$, and the protocol header with $H_{pcie}$. $N$ is used as the number of lanes. The maximum theoretical throughput $V$ for PCIe Gen1 can be calculated with Equation 1.

$$V = \frac{P_l}{P_l + H_{pcie}} \cdot N \cdot 250MBps$$  

III. PCIE BASED ON FPGA

A. A High-Throughput DMA Architecture for PCIe Application

The DMA engine designed in this article adopts a stream mode in order to maximize the data throughput and minimize the FPGA resource utilization. The complete architecture of PCIe-DMA is shown in Figure 3.

FPGA is configured as the PCIe bus master to start memory write (MWR) and memory read (MRD) to PowerPC. The DMA uses TX engine to transmit data to host and RX engine to receive data from host. The PCIe core of XCKU040 offers an Advanced eXtensible Interface (AXI)-4. The width of AXI-4 interface is mainly configured as 128 bits. The AXI-4 contains four groups interface as following:

(1) Completer Request Interface (CRI): User application receives completers from host via this interface group.
(2) Completer Completion Interface (CCI): User application replies the requester from host and delivers each TLP on this interface.
(3) Requester Request Interface (RRI): User application delivers each TLP of requester as an AXI4-stream packet.
(4) Requester Completion Interface (RCI): Host replies user requester and delivers the TLP to FPGA via this interface.

User logic of TX engine is complied with RRI and CCI of PCIe Core in AXI4-Stream Slave mode, while the RX engine is complied with CRI and RCI. TX engine will send MWR and MRD TLP via RRI, then RX engine will receive requester completion information for MRD by RCI. Xilinx offers a basic PCIe communication example which implements MWR, MRD processing launched by host. We need to realize that MWR and MRD are launched by FPGA. The user clock in FPGA is configured as 125 MHz and the IP core is supplied with a reference clock 100 MHz from standard PCIe slot which is mounted on HPCN8641D.

B. Base Address Register

BAR0 in FPGA is implemented as a list of registers which are adopted as handshaking controlling. The width of each register is 32 bits according to the RISC width of PowerPC. The registers contains the following functions:

(1) Initialization flag.
(2) MWR and MRD start flag.
(3) MWR and MRD interrupt processing flag: It indicates that the PCIe in FPGA generates a MSI and is waiting for the PowerPC finishing processing the interrupt.
(4) MWR address, payload length and MWR times.
(5) MRD address, payload length and MRD times.
(6) DMA MWR and MRD performance flag: It is used to indicate the current throughput of PCIe.
C. TX Engine

A finite State Machine (FSM) diagram of the MWR DMA engine is shown in Figure 4 and is described below, together with the handshaking sequence with the VxWorks driver:

![FSM Diagram of MWR DMA-PCIe in FPGA](image)

Fig. 4. FSM of MWR DMA-PCIe in FPGA.

(1) Initialization phase (state 0): PowerPC set the register values including times of Memory Write (MWR), payload length and initial address in BAR0 space.

(2) After the initialization phase, the FSM waits in idle (state 0) for starting MWR (state 1).
   a) FPGA load the payload length and address to which it will send the data.
   b) FPGA check the MWR times and update the WR pointer with the last loaded address.

(3) If the FPGA has already prepared the data for once DMA-TX, then the FPGA start moving data from FPGA to PowerPC (state 2).

(4) After finishing MWR, FPGA generate a MSI (state 2).

(5) If MSI is sent to IP core, then FPGA will wait for the interrupt processed done signal from host (state 3).

(6) CPU deal with the MSI and return “interrupt done” to FPGA, then the FPGA return to idle (state 0).

We denote the DMA MWR payload length (DWORDs number) with \( P_{L_{mwr}} \) and DMA MWR times with \( N_{mwr} \). It will take one clock for FPGA to request once MWR, and the left clocks are valid data. The clock of user logic is 125MHz. Then the theoretical efficiency \( F_{mwr} \) and speed \( V_{mwr} \) of DMA is as Equation 2.

\[
F_{mwr} = \frac{P_{L_{mwr}}}{P_{L_{mwr}} + 1} \quad (2a)
\]

\[
V_{mwr} = \frac{P_{L_{mwr}} \times 4}{(P_{L_{mwr}} + 1) \times 8} \cdot GBps \quad (2b)
\]

Actually, we will count the real clock consumption as following: when \( mwr_{start} \) is valid, the counter will start to count, and when \( mwr_{done} \) which indicates the termination of DMA-MWR is valid, the counter stops count. Each clock denotes 8ns, so it takes 8 * counter value ns. We denote the data size with \( D_{mwr} \) bytes. The actual MWR speed will be calculated as Equation 3.

\[
V_{mwr,real} = \frac{D_{mwr}}{8 \times \text{counter value}} \cdot GBps \quad (3)
\]

D. RX Engine

A FSM diagram of the Memory Read (MRD) DMA engine is illustrated in Figure 5 and is described below, together with the handshaking sequence with the VxWorks driver:

![FSM Diagram of MRD DMA-PCIe in FPGA](image)

Fig. 5. FSM of MRD DMA-PCIe in FPGA.

(1) Initialization phase (state 0): PowerPC set the register values including times of MRD, payload length and initial address in BAR0 space.

(2) After the initialization phase, the PowerPC will prepare the data which will be moved from PowerPC to FPGA. Once the data has been ready, PowerPC will send a MRD command (state 0).

(3) If FPGA receives the MRD command, it will start the MRD (state 1).
   a) FPGA load the payload length and initial address.
   b) FPGA send a MRD TLP to PowerPC.

(4) FPGA will wait for the ack from host, update the RD pointer with the last loaded address and check whether it is the last transmission of a MRD.

(5) After FPGA receives all the data from PowerPC, it will generate a MSI (state 3) and wait for the MRD stop command from VxWorks (state 2).

(6) If MSI is sent to IP core, then FPGA will wait for the interrupt processed done signal from host (state 4).

(7) After FPGA receives the stop command, it returns to idle (state 0).

We denote the DMA MRD payload length (DWORDs number) with \( P_{L_{mrd}} \) and DMA MRD times with \( N_{mrd} \). It will take one clock for FPGA to request once MRD, and then the FPGA will receive the completion packet from PowerPC. The completion TLP contains one clock header for user logic to analyze and the left are valid payloads. The clock of user logic is 125MHz.

Then the theoretical efficiency \( F_{mrd} \) and speed \( V_{mrd} \) of DMA is as Equation 4.

\[
F_{mrd} = \frac{P_{L_{mrd}}}{P_{L_{mrd}} + 1} \quad (4a)
\]

\[
V_{mrd} = \frac{P_{L_{mrd}} \times 4}{(P_{L_{mrd}} + 1) \times 8} \cdot GBps \quad (4b)
\]
Actually, we will count the real clock consumption as following: when the TLP in RX is valid, the counter will start to count, and when \( mrd_{done} \) which indicates the termination of DMA-MRD is valid, the counter stops count. Each clock denotes 8ns, so it takes \( 8 \times \text{counter\_value} \) ns. We denote the data size with \( D_{mrd} \) bytes. The actual MRD speed will be calculated as:

\[
V_{mrd, real} = \frac{D_{mrd}}{8 \times \text{counter\_value}} \times \text{GBps}
\]

(5)

E. Interrupt Controller

It is convenient to generate an interrupt of MSI with Xilinx PCIe core by producing corresponding signals to the IP core, when the IP core feedback a sent signal, it means that the IP core has already successfully sent a MSI to PowerPC. Here, finishing both DMA-MWR and DMA-MRD will generate MSI, PowerPC will polling the MSI register which illustrates the current interrupt type in BAR0 space. The actual MSI timing diagram acquired by ILA is illustrated in Figure 6, and it is the same as in [2].

IV. PCIe Based on PowerPC

The BSP in VxWorks contains kernel, I/O system, file system and network support. WindRiver develop a brand new architecture which is called VxBus for driver development since VER 6.6. The relationship between VxBus and VxWorks is shown in Figure 7.

VxWorks maintains two linked lists: driver list and devices list. After power is on, the initialization will match the drivers and devices, if they are matched, then the matched driver and device will combine to be an instance. The instance is also connected to an instance list which can be called by user application. Generally, user needs to register the custom-designed driver to VxBus via \( \text{vxbDevRegister()} \) function. Then \( \text{pcieInstInit()} \), \( \text{pcieInstInit2()} \), and \( \text{pcieInstConnect()} \) will be called to initialize PCIe device. After that, \( \text{pcieDMAInit()} \) is defined as the interrupt service function and connected to the list of interrupt list.

The control registers that used as handshaking with FPGA is listed as head file in the driver. The registers is the same as registers in BAR0 of PCIe in FPGA. The buffers for TX and RX are both allocated for 2 Mbits. The driver also realizes MWR and MRD with payload length of double words(DWORD) to handshake with FPGA via PCIe.

The interrupt service routine(ISR) in this paper deals interrupt as following:

1. After initialization, the ISR will wait for coming of interrupt from MSI via PCIe.
2. If the interrupt is generated, ISR will first read the interrupt status register in FPGA and check whether it is MWR or MRD interrupt.
3. If it is DMA MWR done interrupt, PowerPC will move the data from the buffer in host to another address and process these data. After that, the PowerPC will send a MWR ISR done signal to FPGA. If the FPGA receives this ISR done signal, it will permit the next DMA MWR.
4. If it is DMA MRD done interrupt, PowerPC will prepare new data to the MRD buffer for the next time transmission and send an ISR done signal to FPGA. If the FPGA receives this ISR done signal, it will permit the next DMA MRD.

V. Test Result

The performance of the DMA engine has been measured using a Xilinx PCIe Gen1 core with different configurations. A KCU105 Kintex Ultrascale-PCIe board mounting on a HPCN8641D was used for the measurements with the Gen1 x8 lanes endpoints. The KCU105 contains a Xilinx XCKU040 device and HPCN8641D contains a Freescale MPC8641D device. The FPGA is plugged into the PCIe slot of the HPCN8641D. BSP is an original driver supplied by VxWorks and it is packaged as VxBus, user driver application is designed according to VxBus. The system architecture is shown in Figure 8.

The measurements don’t take into account the initialization phase: the driver is loaded by the OS and registers are written into FPGA BAR0. The memory addressing is a 32-bit. FPGA issue a MWR with a constant payload length of 16 bytes to PowerPC. There is one dummy clock beat between each MWR TLP. The measurements of this condition is issued in Figure 9.

We also issued a single MRD TLP from FPGA to PowerPC with different payload length. The result for receiving a single MRD completion TLP from PowerPC is shown in Figure 10.

The architecture of DMA-PCIe in this paper is lightweight. The resource requirements of this architecture are listed in Table 1.

### Table 1

| Resource  | Estimation | Available | Utilization |
|-----------|------------|-----------|-------------|
| LUT       | 6689       | 243420    | 2.76%       |
| LUTRAM    | 1174       | 112800    | 1.04%       |
| FF        | 11222      | 484800    | 2.31%       |
| BRAM      | 34.5       | 600       | 5.75%       |

VI. Conclusion

A high-throughput PCIe with DMA engine based on FPGA and PowerPC was described in this paper, the DMA engine is compatible with the Xilinx Kintex Ultrascale PCIe Gen1 Core and a special PCIe driver complied with VxBus is implemented in VxWorks 6.6 based on Freescale MPC8641D. We can easily apply this work in real-time data acquiring and processing system.

The DMA architecture has implemented a high-throughput more than 666 MBps. Because there is a long time between the FPGA issue MRD and PowerPC answer the MRD TLP, we can not realize a more efficient DMA-MRD this time. Generally, this design is satisfied with our data transmission target. However, We didn’t realize a MWR with payload more than 16 bytes this time, a more efficient DMA-MWR will be designed in future.
Fig. 6. MSI timing Diagram(AXI4-128) in FPGA.

Fig. 7. Diagram of VxBus in VxWorks[10].

Fig. 8. System Overview.

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