Calibration of Timing mismatch in TIADC Based on Monotonicity Detecting of Sampled Data

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Abstract In this paper, a calibration method aiming at the timing mismatch existing in the TIADC (Time-Interleaved Analog-to-Digital Converter) is proposed. Monotonicity detecting of the sampled data is employed to estimate the mismatch error, in which only additive operation is involved. Besides that, an improved Taylor expansion method is used to compensate the mismatch error. The processes of the estimation and the compensation are designed to constitute an adaptive loop, so that the calibration can be run in real-time. Compared with other approaches, this method consumes less hardware resources and has a good calibration result.

key words: monotonicity detecting, timing mismatch, sign judgment, Taylor expansion

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

High-speed ADCs are very important in communication systems such as broadband satellite receivers, cable TV tuners and Software Defined Radio. These have a high demand for high sampling rate, high resolution and low power consumption ADCs [1,2,3,4,5,6,7]. TIADC, consisting several parallel sub-channel ADCs which is clocked by sampling clocks with constant phase-shifting, can achieve ultra-high sampling rate [8]. Unfortunately, TIADC performance suffers from channel mismatches including offset, gain and timing mismatch due to process, voltage and temperature variations. These mismatches will significantly decrease SNR and SFDR of TIADC [9,10,11,12,13,14]. In particular, the timing mismatch plays the most critical role for it is becoming severer with the increasing input frequency and overshadows the effect of other

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mismatches for broadband input [15,16,17]. Timing mismatch in TIADC can be calibrated using analog or mixed-signal techniques [18,19,20], but the calibration precision is not high enough in analog domain, mainly affected by the process. All-digital calibration technique, by contrast, seems to be a more promising and more robust solution under various processes. Many techniques have been developed in digital domain for timing mismatch calibration. Most of these leading methods for error estimation are featured by using channel cross-correlation [21,22,23] or introducing reference channel [24,25,26], while most of the compensation methods are based on Taylor expansion [27,28,29] or filter [30]. Most of the calibration methods mentioned above use dividers, multipliers, and differentiators, which consumed high hardware and large power.

In this work, a calibration technique aiming at timing mismatch is proposed, with less hardware consumption and acceptable performance. The error estimation proposed here is realized simply by detecting the monotonicity of the data sampled by the sub-channels and the reference channel and then accumulating the difference as mismatch error. So there is no any multiplication or division needed. As to the error compensation, an improved Taylor compensation is proposed, with which the ideal value of sample point can be calculated from the actual values of sample point.

The rest of the paper is organized as follows. Section 2 introduces the basic idea of the estimation and compensation method. Section 3 presents the simulation results, which show that the proposed method works well with less hardware consumption. Conclusion are finally drawn in section 4.

2. The Proposed Calibration Technique

In this work, we focus on the timing mismatch calibration and suppose that the offset and gain mismatch are already corrected. Fig. 1 shows the overall block diagram of the TIADC with calibration algorithm, where the ADC_r is a reference ADC, and ADC_1, ADC_2, ..., ADC_M are the M sub-channel ADCs of the TIADC. A
band-limited analog signal \( x(t) \) is inputted to the reference channel ADC_r and M sub-channel ADCs at the same time. At the actually sampling time, the ideal sampling points of each channel cannot be acquired, so a reference channel is introduced and each sub-channel is calibrated respectively with the reference channel to cancel the timing mismatch. The sample-time interval of each sub-channel is \( T_s \), and the reference channel and each sub-channel sample the input signal in \((M+1)\) cycles. If \( M=4 \), the sample timing is shown in Fig. 2. The reference channel is aligned with the TIADC sub-channel in turn. The TIADC output value \( y[n] \) is sampled and held with \( 5T_s \) to discard the misalignment, and the clock cycle becomes synchronized with \( y_r \). In this case, if there is no timing mismatch error, the output value is the same as that of \( y_r \), otherwise it is different. At the same time, the error values are delayed by 0, \( 5T_s \), \( 10T_s \), and \( 15T_s \) respectively and sampled and held with \( 20T_s \) separately, and finally the error of each channel is separated. The calibration of the timing mismatch contains two steps: estimation and compensation, and the principle is as follows.

2.1 Timing Mismatch Estimation

Error estimation using derivative is a real-time and efficient algorithm that has been continuously explored [19,24]. The principle is shown in Fig. 3. The \( \hat{y}_n \) is the value of ideal sampling point in reference channel; \( y_{n-1} \), \( y_n \) and \( y_{n+1} \) are the value of the actual sampling points of the sub-ADC_n-1, the sub-ADC_n and sub-ADC_n+1 respectively. The \( e_n \) is the sampling error between \( \hat{y}_n \) and \( y_n \), and \( s_n \) represents the instantaneous derivative of \( y_n \). For the derivative-based Least Mean Square (LMS) calibration algorithm in [19], the timing mismatch can be estimated using the \( e_n \) and the \( s_n \) (or at least known in which direction the mismatch should be corrected [24]) as follows.

\[
\Delta_{n+1} = \Delta_n + \mu \times e_{error,n}
\]

where \( \mu \) is an iterative step size.

During the error estimating period, the contribution from the monotonically decreasing part is stuck to zero to reduce the power consumption. The block diagram of the estimation algorithm is shown in Fig. 4.

It has been proved that there would be convergence chaos for those calibration techniques whose iteration happen within the single ADC channel. In other words, when the frequency of the input signal exceeds the Nyquist band of the sub-ADC or the reference ADC, the sampled data may show a wrong monotonicity compared with the input signal, which is raised by frequency aliasing. In that case, the sign of the estimated error may be contrary to the actual one, which will result in a wrong iterative direction. For four-channel TIADC, the first Nyquist bandwidth of the reference channel is \([0, 1/10f_s]\), and the first Nyquist bandwidth of the sub-ADC
is [0, 1/8f_s]. Table 1 shows the changes of the sign, where the “+” indicates that the iterative direction comply with the actual situation and the “-” indicates that the iterative direction is contrary to it.

| f_s / f_s | ̇y_s | ̇y_s | e_s |
|---|---|---|---|
| [0,1/10] | + | + | + |
| [1/10,1/8] | - | + | - |
| [1/8,1/5] | - | - | + |
| [1/5,1/4] | + | - | - |
| [1/4,3/10] | + | + | + |
| [3/10,3/8] | - | - | - |
| [3/8,2/5] | - | - | + |
| [2/5,1/2] | + | - | - |

For this reason, an extra sign judgment module is introduced to decide the correct iterative direction, as shown in Fig. 5. It consists of two parts: the first part is used to determine the sign of the sub-channel output sign sub-ADC, and the other part is used to determine the sign of the reference channel output signADC_r. The sub-channel sign judgment is realized by multiplying y_Mux-D with y_D-Mux where y_Mux-D is the derivative of the MUX output of the TIAADC and y_D-Mux is the derivatives of the sub-ADCs after MUX [31]. In a similar way, the reference channel sign judgment is realized by multiplying r_sign and e_sign [24]. The adjacent sampled points that adopted here to calculate the derivative r_sign are all from the reference channel. Finally, these two sign outputs are multiplied to form the final result sign that corresponds to e_s in Table 1. The difference in Fig. 4 is multiplied by -1 if the sign is negative and multiplied by 1 if the sign is positive.

According to the formula above, higher order terms means higher compensation accuracy, but also means higher hardware complexity and power consumption. Facing this trade-off between accuracy and complexity, we propose to preserve the first three orders, then y_i can be represented as

\[ y_i = x_i (t + \Delta t_i) + \sum_{k=0}^{\infty} \frac{x_i^{(k)}(t)}{k!} ((t + \Delta t_i) - t)^k \]

(3)

where \( x_i(t), x_i'(t) \) and \( x_i^{(k)}(t) \) are respectively the first, second, and third order derivatives of the ideal sampled signal.

Since the ideal output \( x_i(t) \) of the i-th channel is unknown, \( y_i \) is actually used to take place of \( x_i(t) \). The compensated output can be written as

\[ \hat{y}_i = y_i - \Delta t_i y_i' - \frac{\Delta t_i^2 y_i''}{2!} - \frac{\Delta t_i^3 y_i^{(3)}}{3!} \]

(5)

\( y_i', y_i'' \) and \( y_i^{(3)} \) can be calculated according to formula (4) and then be substituted into formula (5), we get

\[ \hat{y}_i = x_i - \Delta t_i^2 x_i'' - \Delta t_i^3 x_i^{(3)} \]

(6)

The formula (6) shows that, is not what we want, only the first order error is eliminated, and the errors term \( O(\Delta t_i^2) \) and \( O(\Delta t_i^3) \) are still there. Ref. [28] proposed an effective method to eliminate the second and the third order errors, in which cascade structure is introduced to compensate the output step by step, as shown in Fig.6. The compensated output can be written as
where only the $O(\Delta t^4)$ item is left. In this compensation structure, more hardware resources are needed.

In this work, we propose an improved compensation method based on Taylor expansion in which the derivatives are evaluated at the point $t + \Delta t_i$. This improvement help to reduce the complexity while keep good compensation results.

In formula (3), the ideal data $x_i(t)$ is approximately replaced with the actually sampled data $y_i(t)$, which leads to only the first order error is eliminated. With Taylor expansion at $t + \Delta t_i$, the formula can be rewritten as

$$
\hat{y}_i = \sum_{i=0}^{\infty} \frac{x_i^{(k)}(t + \Delta t_i)}{k!} \left(t - (t + \Delta t_i)\right)^k
$$

(8)

where $y_i^{(k)}$ is the k-th order derivative of $y_i$.

Considering that is usually very small and $O(\Delta t^4)$ can be ignored, the formula (8) can be written as

$$
\hat{y}_i = y_i - \Delta t_i y_i^{(1)} + \frac{\Delta t_i^2}{2} \left(\Delta t_i y_i^{(2)} - \frac{\Delta t_i^3}{6} \left(\Delta t_i y_i^{(3)} + \frac{\Delta t_i^4}{24} \left(\Delta t_i y_i^{(4)}\right)\right)\right)
$$

(9)

$$
\hat{y}_i = x_i - \frac{\Delta t_i^4}{24} y_i^{(4)}
$$

According to the formula (9), the proposed compensation structure is shown in Fig. 7.

**Fig. 7.** The proposed compensation structure

For a 4-channel TIADC, the different hardware consumption of above three compensation methods based on Taylor expansion are shown in Table II. The proposed structure consumes the smallest hardware resource, which cost 24 adders, 16 multipliers and 12 differentiators. The comparison of calibration results is shown in Fig. 8. Compared with Ref. [27] and Ref. [28], the almost best ENOB can be obtain with the proposed structure, especially in higher frequency band.

**Table II. Comparison of hardware consumption**

| Ref.    | Adder | Multiplier | Differentiator |
|---------|-------|------------|----------------|
| [27]    | 24    | 28         | 24             |
| [28]    | 64    | 36         | 24             |
| This Work | 24    | 16         | 12             |

**Fig. 8.** Calibration results versus the input frequency

### 3. Simulation and results

A 12-b TIADC is modeled to verify the calibration algorithm at behavior level. Supposing that the normalized frequency $f_o/f_s=0.3972$ and timing errors $\Delta t]=[0.008, 0.006, 0.007, -0.008]T_s$, the spectrum diagram of the TIADC output are shown in Fig. 9 (a) and (b). Before calibration, the spurious spectrum is obvious, and the SNR of TIADC is 23.7dB; after calibration, the SNR are improved to 73.37dB (ENOB=11.87 bit). Fig. 10 shows that the SFDR and SNR can get a dramatic improvement well-distributed in the entire Nyquist band.
Fig. 9. Spectra before and after the calibration

(a) before calibration
ADC Output Spectrum, Fs=400.00MHz

SNR=73.37dB
ENOB=11.87bns

(b) after calibration

Fig. 10. SFDR&SNR before and after calibration at different input frequencies

Fig. 11 shows the output spectrum of two-tone signal. The spurs are suppressed greatly and the SFDR rises from 28.91dB to 69.24dB.

Clock jitters (3ps) are added in our further simulation, which show that clock jitters just slightly raise the noise floor, having little effect on the calibration effect [32]. The spectrum diagram is shown in Fig. 12.

4. Conclusion

In this work, a calibration technique for TIADC timing mismatch error is proposed according to the monotonicity principle. A reference channel are introduced to estimate the mismatch error and an improved compensation method are employed based on Taylor expansion. The pure-digital circuits of calibration are designed and verified on FPGA and the results show that the proposed method improves the SFDR and SNR well in the entire Nyquist band with less hardware consumption.

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