Semiconductor wafer defect classification using convolution neural network: a binary case

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Abstract. With the multitude of steps used in semiconductor industry, automation is being practiced extensively in its manufacturing processes to guarantee quality of manufactured chips and improvement in production. At front end of line, wafer are probed and defective chips are segregated. From this data wafer bin map are generated, these show defects on the surface of wafers. If analysis of wafer bin map is done manually, this may result in incorrect categorization of defects due to human error and lack of judgement. Thus, the rationale behind this research study is to determine the scope of vision-based methods for automatic classification of wafer defects. In view of this, a classifier which detects Type A and Type B defects in wafers is proposed. It involves a Convolution Neural Network (CNN) based binary classifier. 250 Images of each class of wafer bin map dataset, is used to conduct the study on five layer CNN architecture. The proposed setup gives the test accuracy of 97.7%.

1. Introduction

In a typical semiconductor processing sequence, there are over hundred process operations performed before the silicon wafers is converted to chips carrying electronic circuits [1]. The semiconductor process steps include processes such as polishing, etching, diffusion, oxidation and metallization. With the progress in semiconductor industry the number of surface defects are escalating due to reduction in size and increasing complexity [2]. These surface defects if inspected manually can consequently lead to incorrect classification of defects. There is a need to identify these defects at an early stage, so as to find the real cause of occurrence of these defects [3]. The pattern of defects can be classified and related to the issues in the particular fabrication process. Timely and proper addressing of these issues can further help the production and improvement in yield [4].

1.1 Computer vision based wafer defect detection

Computer vision is a field that aims to enable computers to interpret, recognize and process images in the same manner as human vision. Defect detection using computer vision techniques can be accomplished in following ways:

- Image processing methods adopt basic techniques, namely, enhancement and image restoration. Comparing the image under test with the standard image help in detecting defects.
AI-based approach need labelled dataset to develop algorithms for recognizing defect of a particular shape [5]. Furthermore, deep learning is replacing the conventional machine learning and is helping in real-time deployment of such systems.

The frequency of publications from year 2001 to 2020 is shown in Figure 1. Data clearly shows the significant rise in the paper published after 2018 which indicates the rise in research interest in this domain [6]. This graph is extracted from SCOPUS database for keyword “wafer defect classification” and filtered by selecting the articles published in engineering and computer science domain resulting in total 167 articles [7].

![Figure 1. Number of “wafer defect classification” documents published in past 20 years in SCOPUS database](image)

Recently, wafer defects classification using machine learning is being explored. The usual approach is to compute attributes from a wafer map and train a classifier based on these attributes. Contrarily, deep learning method that works directly on a bin map of wafer can be deployed [2]. The idea behind such an application is that it automatically collects defective images of the wafer surface and categorizes the collected images. According to the defect type, it quantifies the tendency of defect generation in the fabrication process [8].

2. Wafer Defects and Dataset Details

Defects on the wafer surface commonly occur due to fault in machinery, stains of chemical, material damages, errors due to manual handling of processes, and ambient settings. The faulty wafer maps illustrate a lot of distinctive patterns such as spot, repetitive shapes and clusters. To locate and visualize these defect patterns wafer map images are observed.

Wafer Bin Map (WBM) represents a particular positions of fault which can be analyzed for locating source of low yield in manufacturing [9]. Publically available real world WBM dataset, WM-811K [10], dataset provided by Multimedia Information Retrieval Lab, Department of Computer Science, National Taiwan University [11], and is created by Wu et al. in 2015 [12]. This dataset consists of total 811,459 WBMs among which, 172,950 are labelled and can be used in supervised learning. There are nine labels [13].
However, it can be noted that the distribution of each type of defect is imbalanced as shown in Figure 2. The most commonly occurring defect is Edge-Ring. In this research work, binary classification case is taken. Total 500 images of Random and Edge-Ring defect are classified as Type A and Type B defect, respectively as shown in Figure 3.

- **Type-A** defects appear haphazardly and no definite pattern is visible. The reason of occurrence of these defects is unknown and it is difficult to point out one specific cause of these defects [2].
- **Type-B** defects are systematic and repeatable. This type of defect has a definite pattern and the reason can usually be established by observing the defect pattern [2].

![Figure 2](image)

**Figure 2.** WM-811k dataset analysis

3. **Computer Vision Approach Wafer Defect Classification**

![Figure 4](image)

**Figure 4.** Computer vision approach for wafer defect classification
The methodology to implement computer vision approach for wafer defect classification is shown in Figure 4.

3.1 WBM Pre-processing
It is important to pre-process WBM array in order to apply computer vision techniques for classification. WBM defect pattern is converted to an image. All the bin maps are converted to equal size images of size 26x26.

3.2 Deep Learning Architecture Deployment
In deep learning approach, Convolution Neural Network (CNN) is utilized for image classification. These architectures can be designed from a scratch. To design CNN model for a specific application, early layers learn low-level features while the last layer performs classification on the basis of feature map. Table 1 lists the details of each layer of proposed CNN architecture.

![Figure 5. Details of proposed CNN Model](image)

**Figure 5. Details of proposed CNN Model**

CNN architecture includes:
- Convolution layer performs convolution of image with kernel to extract feature maps. Here five-layer CNN model is designed. It consists of convolution filters of sizes [3*3, 3*3, 5*5, 5*5, 7*7].
- ReLU is used to calculate activations of all convolved feature map.
- Max Pooling layers are utilized to reduce complexity of each CNN layer output.
- Optimizers_1 = “sgdm”; Optimizers_2 = “adam”; loss_function1 = “hinge”; loss_function2 = “squared_hinge”; classifier = binary support vector machine
- Total Trainable parameters: 1,15,969
- Accuracy is used as the performance metric here. It is the fraction of classes rightly classified to the overall number of input samples fed to the model during testing, training and validation resulting in Test accuracy, Train accuracy and Validation accuracy, respectively. Here, Test accuracy is considered for comparison of results

3.3 Defect Classification
In supervised learning the neural network learns in terms of value of weights and biases from the training dataset. The validation data provides neutral assessment of a model fit on the trained network. The validation dataset is required to fine-tune the hyper parameters. This dataset can also be used for an
unbiased evaluation of a trained model. At the output, a fully connected layer and classification layer predict the category of input image. Here binary SVM is used to classify the images on the basis of computed feature map.

3.4 Cause Analysis
The likely causes of each of defect can be related to a process variation. Center defects are caused due to fluctuation in power, liquid flow, or pressure. Local defect can result due to valve leakage, distortion in the pump. Random defect occur because of dirty pipes, showerhead, and scratch are the result of irregularity in robot handoffs. The cause of each defect is mentioned as follows:

- **Type-A** defect does not have a fixed pattern and this can be addressed by improving the constancy and precision of the system involved.
- **Type-B** defect can be caused by microscopic shifting of the mask during photolithography or disproportionate (over or under) etching process. Closed ring shapes usually reflect problem in etching or annealing process.

4. Results and Discussion

250 images of each class is considered and the experiment has been performed for 25 epochs, at 32 batch size, 0.01 learning rate and L2 regularization. For training the proposed network, accuracy is analyzed for the two optimizers selecting hinge loss function and squared hinge loss function at a time. Training is an iterative step until the desired accuracy is achieved. Once the network is trained to a satisfactory loss level, the network is tested on Test dataset. For evaluating the performance of computer vision approach for wafer defect classification the dataset is used as 70%, 15%, and 15% as train, test and validation set, respectively. Training and validation results for different combination of loss function and optimizer are shown in Figure 6 through Figure 9.

![Figure 6](image_url)  
*Figure 6.* Training and validation result for adaptive moment estimation optimizer and hinge loss function
Figure 7. Training and Validation Result for stochastic gradient descent with momentum optimizer and hinge loss function

Figure 8. Training and Validation Result for adaptive moment estimation optimizer and squared hinge loss function

Figure 9. Training and Validation Result for stochastic gradient descent with momentum optimizer and squared hinge loss function
Figure 10. Test accuracy of proposed CNN architecture for wafer defect classification

As shown in Figure 10, the maximum value of test accuracy is 97.7% for proposed five-layer CNN architecture.

5. Conclusion

In semiconductor fabrication steps, analysing the pattern of defect can help in finding the issue in the process. Addressing and correcting the problem may further help in improving the yield. It is critical to identify and classify these bin maps so that the actual cause for these defects can identified and corrected. In general, the engineers examine these wafer maps manually. In order to eliminate human inspection an automatic defect classification mechanism based on computer vision is proposed. In this paper, two classes of WM-811K are used to conduct the study using a five-layer CNN model. For the combination of “adam” optimizer and “squared hinge” loss function, the proposed model attained the maximum test accuracy.

In future, a multiclass CNN classifier will be designed to classify all the classes of wafer dataset. Also, the effect of variation of model hyper parameters for wafer defect classification will be analyzed in detail.

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