Pinch Off Plasma CVD Deposition Process and Material Technology for Nano-Device Air Gap/Spacer Formation

Son Nguyen, T. Haigh, K. Cheng, C. Penny, C. Park, J. Li, S. Mehta, T. Yamashita, L. Jiang, and D. Canaperi

1 IBM at Albany Nanotech, Albany, New York 12203, USA
2 GLOBALFOUNDRIES, Albany, New York 12203, USA

As integrated circuits for high performance CMOS devices scale down to \( \leq 10 \) nm dimension, further reductions in capacitance are vitally important for device performance. It is important to reduce capacitance in the FEOL and BEOL device structures while maintaining fabrication integration robustness. This paper presents an overview of material and process technology requirements for FEOL air spacer and BEOL air gap formation using a pinch off deposition approach. These approaches utilize established dielectric materials and processes such as Plasma CVD of SiN, SiCN, SiCOH, pSiCOH, in the formation of the air spacer/air gap. The selection of these dielectric materials and processes has a large impact in the void (gap) dimension and volume. The void dimension and volume in airgap/air spacer structures can be controlled with various dielectric deposition processes and materials to facilitate subsequent process fabrication steps, and ultimately to build a robust device with substantial capacitance reduction.

The air spacer (FEOL) and air gap (BEOL) structures require novel dielectrics of SiN, SiNO, SiCN, SiCOH, pSiCOH, for pinch off deposition to optimize the capacitance reduction while maintaining yield and reliability. Significant capacitance reduction with good reliability has been achieved with the pinch off deposition process approach on current 10 nm device structures as shown in Figure 1. For reference, the void dimension and volume in a typical air spacer/air gap structures can be controlled with various dielectric deposition processes and materials as in Figure 1: (a) Long and wide voids formation for optimal capacitance reduction, (b) Short and wide voids formation for improved process fabrication and integration, (c) Short and narrow voids formation for better sidewall protection and device reliability but with a smaller capacitance reduction. The overall void dimension and type of dielectric material are strongly related to the total device capacitance reduction and reliability. Significant capacitance reduction with good reliability has been achieved with the pinch off deposition process approach on current 10 nm device structures as shown in Figure 2 (a) Long and wide voids formation for optimal capacitance reduction.

The dielectrics of SiN, SiNO, SiCN, SiCOH, pSiCOH for pinch off deposition were deposited in a commercial high throughput production-worthy 13.6 MHz RF 300 mm Plasma Chemical Vapor Deposition process (PECVD) system at 350 C. The dielectrics were deposited using a combination of various silane (SiH4) or carbo silane or organosilicon precursors with other reactant gases such as Ammonia ((NH3), Nitrogen (N2), Oxygen (O2), or Nitrous Oxide (N2O) as described in previous publications. The advanced highly robust conformal SiN deposition was deposited by cyclic processing using Silane, Ammonia and Nitrogen. The SiCN dielectric was also deposited at 350 C using a combination of Trimethyl Silane (TMS) + Ammonia (NH3) and (optionally) with Hydrogen for robust SiCN film. For dense and porous SiCOH, liquid Octamethyl Orthosilicate (OMCTS) and Oxygen were used as precursors for the deposition at 350C or 230–280C and UV cure depending on the desired dielectric constant value and film’s porosity. Overall, the plasma CVD temperature and the subsequent UV treatment for porous SiCOH are maintained about or below 400 C for both Air Gap and Air Spacer pinch off dielectric deposition to ensure no/minimal detrimental impact on the nano CMOS devices. The plasma deposition conditions

\* Electrochemical Society Member.
\* E-mail: sonsn@us.ibm.com

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Figure 1. Scanning Transmission Electron Microscopy (STEM) of a typical 10 nm Finfet gate (dark): (a) Void (white areas in SEM pictures) dimension and volume in air spacer/air gap structures can be controlled with various dielectric deposition processes and materials: (a) Long and wide voids for optimal capacitance reduction. (b) Short and wide voids for improved process fabrication and integration. (c) Short and narrow voids for better sidewall protection and device’s reliability but smaller capacitance reduction.

Figure 2. Typical STEM of 2a) Front End of Line Air Spacer Formation in 10 nm FinFet (32 nm Pitch) Pinch off Deposition for elongated air spacer with robust sidewall protection dielectric to improve device’s reliability and 2b) Back End of Line 48 nm (see dimension bar) Pitch Air Gap Formation by Pinch of Deposition with optimal void’s volume and robust Cu diffusion dielectric for large capacitance reduction.

Figure 2a)- elongate voids in blue

Figure 2b)- triangle voids

Table I summarizes various plasma deposited dielectric films and their properties. These dielectric films have been developed and used by our laboratories and have appeared in many of our publications over the years. Since similar materials can be deposited under various conditions and have different properties, our reference publications is to prefer to specific process chemistry and tooling that use for this pinch off deposition processes. These dielectrics are also commonly used by the semiconductor fabrication industry over the years in our review papers including various References. Historically, both Silicon Nitride and Silicon Oxide dielectric films have been widely used for electronic devices fabrication. In recent years, carbon and porosity have been incorporated to these dielectrics to reduce the dielectric constant and to create new classes of lower dielectric constant SiCN and SiCOH films that are now widely used for nano electronic device fabrication. These dielectric films can also be used in the formation of air gap/air spacers for pinch off deposition. Table I shows several important dielectric properties, such as dielectric constant, conformality, porosity and carbon doping that have a strong impact on the pinch off deposition process. For the best optimal air gap/air spacer formation, a two-step deposition process is normally used. In this study, conformality defines as the ratio of side wall/planar surface film’s thickness over 1:1 aspect ratio structure as showed in Figure 4. In the first step, a thin robust conformal dielectric liner is deposited on the exposed top, sidewalls and bottom surface to

(rf power, pressure) and ratios of reactants were optimized to achieve good uniformity and optimal composition and bonding structure in the dielectric films. For barrier cap films such as SiN and SiNO, advanced cyclic multi-nanolayer deposition of the dielectric film was conducted with various surface treatments with Nitrogen and Nitrous Oxide plasma to achieve a high conformality as shown for SiN film in Figures 3 and 4. For highly conformal Cyclic multi nanolayer SiN or SiNO films, robust film sidewall protection can be achieved. Figure 3 shows the details of the cyclic plasma deposition processes for conformal SiN and SiNO films. STEM pictures in Figure 4 show the typical cyclic multi nanolayer SiN or SiNO dielectric of highly conformal (>75%) sidewall protection over gate structure and then flowing with a second poorer/low conformal low k dielectric to form the air spacer/airgap fabrication approach. In this cyclic process, the thin film (~2 nm) deposition followed by plasma treatment provides excellent step coverage sidewall and then the poorer conformality deposition is for the pinch off deposition. For plasma deposited dielectric materials, the cyclic deposition and plasma treatment process improved the dielectric film’s properties significantly. This first cyclic deposition/treatment step approach enables the change in the film’s composition at nano dimension level and to enhance deposited film’s sidewall conformality as indicated in our recent publications.

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protect the reactive surface (metal liner, metal gate, silicide . . . etc.) elements. The first step dielectrics are normally conformal SiCN or SiN. In the second step, a non-conformal dielectric is deposited to pinch off the gaps to form air gaps/air spacer. The second step dielectrics are normally low k SiCN or SiCOH film. The type of dielectric associated thickness and film properties used in the pinch off deposition will have significant impact on the gap formation, and the resultant FEOL (air spacer) and BEOL (air gap) device capacitance reduction and reliability. With these two-steps deposition, there is always a consistent robust thin dielectric deposited to protect the top/sidewall/bottom surface of the air spacer/air gap, to prevent unwanted oxidation and to ensure reliability. Scanning Electron Transmission Spectroscopy (STEM) and Electron Energy Loss Spectroscopy (EELS) techniques were used to examine the voids dimension by visual image and compositional detection. In next section, we will describe the fabrication, dimension and typical structures of both 10 nm Finfet Air Spacer and 48 nm Pitch Air Gap in Cu-ULK fabricated on many 300 mm wafers.

Air Spacer and Air Gap Device Fabrication, Results and Discussion

For air spacer fabrication, a 10 nm FinFET CMOS platform featuring contact gate pitch of 64nm, fin pitch of 42nm, replacement high-k/metal gate (RMG), and self-aligned contact (SAC) was used to develop an air spacer module that can be readily plugged into the standard CMOS flow. As depicted in Fig. 5a, the air spacer module is inserted in the FinFET flow after replacement high-k/metal gate (HK/MG) and source/drain trench silicide metallization (TS). Fig. 5b depicts the critical process steps for forming air spacers. The first step of air gap spacer formation is to remove a sacrificial gate caps and spacers after contact metallization. Reactive ion etching (RIE) process is used to remove the capping layer and spacer. It is required that not only gate metal but also contact metallization layer should not be eroded during the RIE process. The high aspect ratio structure (gate height/spacer thickness) in conjunction with high etch selectivity requirement for RIE pose a significant challenge for the removal of the layers. After forming the air gap, a two-step deposition process is used to form the air spacer. In the first step, a thin robust conformal dielectric liner is deposited on the exposed sidewalls of RMG and TS to protect the gate stack and TS metal. In the second step, a non-conformal dielectric is deposited to pinch off the gaps to form an air spacer. A planarization process is performed to remove dielectric above TS contact. The standard middle-of-line (MOL) process is resumed followed by back-end-of-line (BEOL) process to complete the transistor circuit fabrication. Figures 5c and 5d show a Scanning Transmission Micrograph of a fabricated 10 nm FinFET air spacer transistor and it associated graphical structures. It can be seen from Figure 5c that well shape-controlled air spacer structures can be fabricated with the steps in Figures 5a and 5b.

Since the air spacer dimensions are in nanometer scale, both STEM and EELS analysis techniques were used to detect, determine and measure the gaps such as between gate to source. Figure 6 shows both STEM image and EELS composition analysis of Air Gap X-section with 1nm conformal SiN and then 35 nm non-conformal pinch off deposition of SiCN dielectric. The STEM and EELS data confirm Air Spacer/Gap region dimensions. No or little Si/N/O signals as observed by STEM as voids.

The 10 nm Finfet device experimental data shown in Fig. 7 confirms the significant $C_{gs}$ (gate-to-source capacitance) reduction by

[Figure 3. Cyclic plasma deposition processes for conformal SiN/SiNO films using nanolayer deposition and plasma Nitrogen/Nitrous Oxide treatment.]

[Figure 4. Highly Conformal (>70%) robust multi-layer SiN/SiNO on side-wall for protection of the 32 nm gate structure (b) and then a second poorer/lower conformality (<45%) SiCOH pinch off deposition to form air gap/air spacer voids (void = white space).]
Table I. Various baseline and advanced dielectrics deposited by plasma CVD that can be used in liner and pinch off deposition. The detail properties of these films are in References 12–29.

| PECVD Film and ref. publications | Dielectric constant (k) | % Porosity (EP) | a/o % Carbon Doping (RBS) | Comment on conformality: defines as the ratio of side wall/planar surface film’s thickness over 1:1 aspect ratio structure as showed in Figure 4 |
|----------------------------------|------------------------|-----------------|---------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| SiO2 (Ref. 25,26)               | 4.0                    | 0               | 0                         | Baseline ILD, only ALD film is conformal. PECVD film is normally < 50% conformality                                             |
| SiCOH (Ref. 19)                 | 3-3.1 (insert carbon)   | ~1%             | ~11%                      | Low k ILD Dense SiCOH, < 40% conformality                                                                                     |
| SiCOH 2.7 (Ref. 27)             | 2.7                    | 7–8%            | 12–13%                    | Lightly porous SiCOH ILD, < 40% conformality                                                                                 |
| Porous SiCOH (Refs. 12,16)     | 2.3-2.4 (Porosity + C insertion) | ~20–38%       | 10–35% (varying C)        | Ultralow k pSiCOH ILD High C. K = 2.4 has ~30–33 a/o % C. < 40% conformality                                                  |
| SiNO (graded) (Refs. 20,21,23)  | 4.3-5.0                | 0               | 0                         | SiNO cap, conformality (>65%) like cyclic SiN                                                                               |
| Si3N4 (Refs. 23,24)            | 7                      | 0               | 0                         | Baseline PECVD Cap/ Passivation dielectric 40–50% conformality                                                              |
| (Silicon Nitride Cyclic) SiNx   | 6.8                    | 0               | 0                         | Multilayer (1–2 nm layer) conformal (>65%) silicon nitride                                                                  |
| SiCyNx – low H SiCN (Refs. 14,15,19,22) | 5.2–5.8              | 0               | ~8–22%                    | Robust Low H SiCNH < 40% conformality                                                                                         |
| C-Rich SiCNx (Refs. 28,29)     | 3.4–3.5                | 0–1%            | ~30%                      | Low k Cap top layer (4–8 a/o% N), <40% conformality                                                                        |

Figure 5. Process Flow to integrate air spacer in FinFET CMOS technology (A), key air spacer steps (B) including pinch off deposition step 4 (Reference 1), STEM of 10 nm Finfett air spacer structure with voids in white spaces (C) and associated graphic structure (D).
Figure 6. STEM and EELS composition analysis of Air Gap X-section with 1nm conformal SiN + 35 nm non-conformal pinch off SiCN dielectric. EELS confirm Air Gap Spacer region dimensions with No/Little Si/N/O signals as observed by STEM.

Figure 7. 10 nm Finfet device demonstration of 12% reduction of effective capacitance \(C_{\text{eff}}\) of ring oscillator (RO) by air spacer as compared with a reference low-k spacer \((k \sim 5.0)\). (Reference 1).

Figure 8. Normalized \(C_{\text{ov}}\) vs. spacer dielectric constant \((K)\). The partial air spacer results in \(\sim 21%\) \(C_{\text{ov}}\) reduction, equivalent to reducing the effective \(K\) value of a nominal FinFET from 5 to 3.2. (Reference 1).

air spacers. The split was done by varying the RIE etching pulldown amount of low-k spacer and thus air spacer depth. Clearly more spacer pulldown results in more air spacer and thus more \(C_{gs}\) reduction. The experimental data is in good agreement with TCAD simulation. The capacitance reduction is pronounced even when a very thin air layer is introduced in the spacer. Capacitance reduction of 50% can be achieved with 25% of air spacer. Capacitance reduction slows down with further increase in proportion of air portion. Therefore, a robust ultrathin dielectric like cyclic SiN or SiNO or SiCN liner to protect sidewall provides a good tradeoff between maximizing the benefit of air spacer while minimizing its reliability risk. TCAD simulation in Figure 8 confirms that our partial air spacer results in an equivalent \(K\) value of 3.2, significantly lower than any state-of-the-art low-k \((k \sim 5.0)\) spacer. Overall, partial air spacer (PAS) is a viable approach to introducing air spacer in FinFET, materializing the benefit of air spacer while minimizing its risks. In this approach, \(C_{gs}\) can be reduced by 15–25% and \(C_{\text{eff}}\) of Ring Oscillator by about 10–15%. With the two-step pinch off deposition approach, no significant degradation is found in 10 nm Finfet air spacer transistor reliability.

For BEOL air gap formation, the baseline BEOL structure involves dual damascene Cu wiring in porous SiCOH ultralow-k \((k = 2.4)\) dielectric at minimum wiring pitch of 48 nm. The Cu wires have a Co/dielectric bilayer cap for EM lifetime enhancement, as was previously developed. The BEOL airgap module utilizes relaxed lithography for airgap placement, while maintaining compatibility with the Co metal cap. The airgap integration module is depicted in
Fig 9. At these nm-scale dimensions, the Cu wire metal barrier and dielectric cap protection layers are highly critical for preventing any adverse interactions with the airgap processing. These layers are resistant to erosion, or chemical damage, and therefore protect the Cu wire itself. Any chemical attack must be avoided, as it can impact Cu wire resistance and reliability. The Co-Capping Cu process is followed by deposition of temporary hardmask and patterning stacks, and then lithographic patterning. Sequential dry and wet etch steps precisely etch back the interlayer dielectric in the desired locations. The hardmask stack is then completely removed, and an airgap robust protective dielectric barrier is deposited to seal the airgaps before the next low k (SiCOH 2.7 or pSiCOH 2.4 as in Table I) interlevel dielectric is deposited. For an optimal pinch off deposition process, either a single step robust SiCN dielectric deposition or a two-step conformal SiN/pinch off SiCN dielectric can be used to form the airgap. The single step pinched off deposition with robust dielectric is normally preferable due to the process simplicity and controlled cap thickness.

Figure 10 shows a typical structure of a 48 nm pitch Cu-ULK interconnect with SiCN dielectric pinch off deposition with a high and low plasma deposition pressures with the fabrication steps in Figure 9d. It can be seen from the Figure 10 images that the low pressure SiCN deposition process produced a better air gap with the pinch off below the Cu metal lines. This type of pinch off deposition with air gap below the Cu metal line is preferable for the subsequent fabrication steps. This is also enabling a larger process window for the air gap formation. Furthermore, this low-pressure SiCN film also provides additional advantage in k value reduction (\(~5\%\) k reduction) and subsequently will produce a slightly larger capacitance reduction in devices.

Figure 11 shows STEM cross sections comparing wafers running the “ungapped” baseline process to those running the full airgap process with both blocked regions and airgapped regions. The gapped sections show typical 48 nm pitch airgap depths and profiles. Optimization of the airgap patterning process has resulted in minimal erosion of the Cu lines, to maintain reliability and resistance while demonstrating marked capacitance reduction. An additional advantage of our process, shown in this figure, is that the dielectric cap thickness is identical in both the blocked-out and airgap regions. This eliminates topography and vertical capacitance impacts of 2-barrier solutions used by others. It should be noted that we observed no issue in either placement of airgap adjacent to vias or the gapped vs ungapped space using this pinch off deposition in conjunction with the use of selective CVD Cobalt hard mask with optimal wet clean.

With the optimized airgap process with a single step pinch off deposition, a capacitance reduction of approximately 20% relative to the baseline process using ULK (k = 2.4) dielectric was achieved with no line resistance increase, as seen in Fig. 12. This data shows total capacitance (interlevel plus intralevel) for a multilevel comb-comb capacitor with airgaps applied to the entire array at one metal level. Typical capacitance reductions can be tuned to 15–25%, depending on the airgap depth. A capacitance reduction of ~20% is achieved with no line resistance increase relative to the baseline ungapped process. Additionally, both TDDB and EM reliability are equivalent to ungapped controls. This is achieved through careful control of the Cu protection, pinch off deposition and wet clean processes. This demonstrates the feasibility of extending airgap technology from the fat-wire levels into the thin/fine wire levels, even at advanced technology nodes using pinch off deposition as one of the processing steps.

Figure 10. A typical example of 48 nm Pitch BEOL Cu-ULK air gap structures with SiCN pinch off deposition at low and high-pressure plasma CVD processes.

Figure 11. Typical cross section images of 48 nm Pitch Cu-ULK (a) baseline wafer without airgap processing and a wafer with airgap processing, showing regions where (b) airgaps are excluded and (c) airgaps are defined.
In summary, as it has been shown in Figures 1a,1b,1c and 2a,2b,6,10,11 that the pinch off deposition process with various dielectrics in Table I can be used to fabricated suitable voids of various shape and dimension. These two- step deposition process has been implemented into many 300 mm full functional test wafers with 10 nm FEOL Finfet air spacer and 48 nm pitch Cu-ULK BEOL structures. The air gap structures show a 20% capacitance reduction.

Conclusions
A pinch off deposition approach can be implemented to form voids suitable for capacitance reduction in nano device FEOL air spacer1 and BEOL air gap2 formation. These approaches utilize established dielectric materials and processes such as Plasma CVD of SiN, SiCN, SiCOH, pSiCOH, in the formation of the air spacer/air gap. The selection of these dielectric materials and processes has a large impact in the void (gap) dimension and volume. The void dimension and volume in airgap/air spacer structures can be controlled with various dielectric deposition processes and materials to facilitate subsequent process fabrication of robust devices with substantial capacitance reduction. Successful implementation of pinch off deposition in suitable process and integration approaches produces a significant capacitance reduction in both 10 nm FEOL Finfet air spacer and 48 nm pitch Cu-ULK BEOL structures. The capacitance reduction was obtained with improving device performance and without degradation in reliability.

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ORCID
Son Nguyen https://orcid.org/0000-0002-0501-7771

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