A Single Stage 1 Switched Capacitor 7S-7L using Different PWM Topologies for Harmonics Reduction

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Abstract. Design and analysis of single-stage 1 Switched Capacitor (SC) boost 7Switch 7-Level (7S-7L) inverter for attaining higher voltage levels with reduced switches count using various PWM techniques is presented. PD, POD, APOD, VF, and CO is different PWM techniques which used to control the switches in the SC circuit. The main objective of this analysis is to reduce the existing drawbacks as increased switches count, high % of Total Harmonic Distortion (THD), and typical PWM control method. Single-stage SC-based boost converter topology in Multi-Level Inverter (MLI) that resolves the existing problem. Single source, two capacitors, and the voltage gain ratio of 4 are attained from the presented topology without the transformer. Furthermore, comparisons are made between the existing parameters such as THD value, voltage levels, and proposed THD, voltage levels with different PWM techniques. SC-based 7L inverter is implemented, in order to compare the performance of proposed better than the existing 5-level MLI and 5-level SC-MLI inverter, and THD is compared with various PWM techniques and 0.9 modulation index. The performance of the proposed method is validated through the simulation results using MATLAB/Simulink.

Keywords: Multi-Level Inverter (MLI), PWM techniques, Switched Capacitor (SC), Total Harmonic Distortion (THD).

1. Introduction

In recent days’ solar power system is becoming well-known energy resources by reason of effortless installation, zero environmental pollution, and low continuance, no fuel cost whereas comparing to the wind, hydro, thermal and etc. The energy available from the solar is less at night and cloudy period. For that reason, front end or back end boost converter, and some special converters becomes essential to achieve high voltage but which leads to reduce the system efficiency and increase the circuit complexity. In this paper, 1 SC-based MLI using the LS-PWM technique is presented. It is validated through MATLAB/Simulink, and comparative analysis is accessed for proposed method with than existing as considered the component count, voltage gain, and %of THD value, controllers. The paper is organized as follow, analysis the survey of the MLI and its control methods are explained in section-2, in section-3 proposed topology and circuit description of SC-MLI, in section-4 modulation control, simulation results, performance and analysis of proposed method in LS-PWM techniques is in section 5, comparative [1] analysis of proposed and existing are presented in section-6, and the last section concludes this analysis.
2. Literature survey
Generally, Multi-Level Inverters (MLI) are familiar as the best results to improve the performance/execution of solar, wind, and other power electronics utilities in high or medium power applications [2-4]. The output of the MLI is stepped voltage waveform at the desired quality. Existing [4-6] have some advantages over the voltage source inverter, and it has some disadvantages like high switch count, low reliability, higher blocking voltage rating, and extra expenses for designing an immense filter, large capacitor banks required high power supply to attain desired output [7-8]. The developed structure of MLI is SC boost based multi-level inverter is overcome the above-mentioned issues. It reduces the count of the additional element, power supply, and gate driver, high voltage gain with reduced active and passive elements [9, 12]. Sine PWM is used widely, because of its simple operation and provides good results. LS-PWM is studied to establish and applied in that way, enlarging the conversion efficiency [14, 18, 23]. LS-PWM modulation and Carrier overlapping (CO) is used to produce the pulses to the switches in the SC boosting based multi-level inverter [19-22].

3. Proposed switched capacitor boosting 7-level inverter and circuit description
The MLI system consists of 7-level output voltage with a single SC-converter module, one DC source, fewer switches and two capacitors. Block representation of SC-MLI with RL load is shown in figure 1. Charging and discharging of capacitors are utilized to neglect the voltage balancing issues. The proposed boosting has the output of seven-level with reduced switch count. Single unit SC circuit consists of single DC source (Vdc), three switches (S1, S2, and S3) with two diodes (D1, D2), and two capacitors (C1, C2). 7L output voltage obtained from the single-phase inverter is 0, Vdc, 2Vdc, 3Vdc, -Vdc, -2Vdc, -3Vdc. It produces six bipolar (positive polarity & negative polarity) levels and zero state level across the load.

At initial analysis, capacitors are utilized for maintaining the output current (Io) and voltage (Vo) and also eliminates the voltage ripple across the load, input source (Vdc), avoids voltage balancing issues, and switches (S) are kept at ideal and depends on the switches in the switched capacitor boost converter.

![Figure 1. Block representation of SC-MLI](image)

1. Output states of proposed circuit
This paper focuses on the circuit topology of switched-capacitor boost MLI is represented in figure 2. The 7 states of SC-MLI are represented as 0Vdc to 3Vdc related to the positive half cycle, and 0Vdc to -3Vdc related to the negative half cycle.
Figure 2 Circuit diagram of 7L-7S SC-MLI

State 0Vdc
During the positive half cycle of 0Vdc state, SA is ON state. Remaining H-bridge inverter is OFF state. The diode in SB switch act as freewheeling. During the negative half cycle of 0Vdc state, SD is ON state. Remaining switches in H-bridge inverter is OFF state. The diode in SC switch act as freewheeling. Thus the DC bus voltage is zero

\[ V_{Bus} = 0 \]  

(1)

State Vdc& -Vdc
In positive mode, S3, SA, and SC are in ON state, DC bus voltage is equal to the input voltage which as capacitor (C2) by turning OFF of S1 and V input supplies power to the load and negative S3, SB, and SD is in ON state. Capacitor C1 is charged to the V input by turn ON of D2 and S3. Then the output voltage level is represented in the below,

\[ V_0 = \pm V_{dc} \]  

(2)

State 2Vdc & -2Vdc
In positive S1, SA, and SC are in ON state, when the capacitor voltage is greater than the input voltage the diode operates as reverse biased, and during the negative half cycle switches S1, SB, and SD are in ON state. Then the output voltage level is represented in the below,

\[ V_0 = \pm 2V_{dc} \]  

(3)

State 3Vdc & -3Vdc
In this the switches S1, S2, SA, and SC are in ON state. Capacitor (C2) is charged. At that time diode is reverse bias. Capacitor (C2) and input source supply the power to the load. The total DC bus voltage is equal to the output voltage, in negative switches S1, S2 SB, and SD are in ON state. The above-mentioned process is repeated in the negative cycle. Then the output voltage level is represented in the below,

\[ V_0 = V_{dc} + 2V_{dc} = \pm 3V_{dc} \]  

(4)

4. PWM strategy
Multicarrier PWM is used when the output voltage levels are 3 or more than three levels. It is generally classified into two methods, such as Phase Shifted (PS) pulse width modulation technique and level shifted (LS) PWM technique. In LS carrier signals are vertically shifted to each carrier signals.
Table 1. Switching States of Proposed 7L-7S SC-MLI

| Switches | Output (Vo) | 0 | VDC | 2VDC | 3VDC | 0 | -VDC | -2VDC | -3VDC | 0 |
|----------|-------------|---|-----|------|------|---|------|-------|-------|---|
| S1       | 0           | 0 | 1   | 1    | 0    | 0 | 1    | 1     | 1     | 0 |
| S2       | 0           | 0 | 0   | 1    | 0    | 0 | 1    | 1     | 0     | 0 |
| S3       | 1           | 1 | 0   | 0    | 1    | 1 | 0    | 0     | 1     | 0 |
| S4       | 1           | 1 | 1   | 1    | 0    | 0 | 0    | 0     | 0     | 0 |
| S5       | 0           | 0 | 0   | 0    | 1    | 1 | 1    | 1     | 1     | 1 |
| S6       | 0           | 0 | 1   | 1    | 0    | 0 | 0    | 0     | 0     | 0 |
| S7       | 0           | 0 | 0   | 0    | 1    | 1 | 1    | 1     | 1     | 1 |

It is used to generate a pulse to the switches. The performance of the multi-level carrier-based sinusoidal PWM with PD, POD, APOD, CO, and VF is applied for reducing the % of THD. In PD, all triangle signals are in phase. In POD, trapezoidal signals positive levels are out of phase with triangle signal by negative level at 1800. In APOD, all triangles are 1800 out of phase regarding its nearer triangle signal. In VF, frequency of the Carrier is varied properly, to balancing the switches. In CO, carriers with the same frequency and amplitude (Amp) are inclined such that the carriers are overlapping each other, overlapping distance between each Carrier is Amp/2.

For 7L, three high-frequency signals (Vdc to 3Vdc) of the same amplitude (Ts – triangular signal), the peak amplitude of the reference sinusoidal signal (Sref). Sref is compared with the triangular signal which generates pulses to turn ON semiconductor switches in SC-MLI. The modulation index of the proposed system is defined below equation (5). The pulse pattern of this proposed circuit is representing in figure 3.

\[ M = \frac{S_{\text{ref}}}{3 \times S_{\text{c}}} \]  

(5)

Sref - Peak amplitude of sinusoidal reference voltage
Sc - Amplitude of carrier signal (triangular signal)

Six triangular and one sine wave are used to attain the 7-levels at the output. A reference signal (sine wave) is continuously compared with each triangle signal (the carrier wave). Required pulse is produced when the reference signal is more than or lesser than the triangular signal. Pulse pattern of the 7L-7S inverter with the modulation index of M=0.9 is represented in figure 3.
5. Simulation Analysis

The design of the 7L-7S SC-MLI model has been developed by MATLAB/Simulink software platform. From the designed SC-MLI is shown in figure. 5, maximum 100Vdc is extracted in output 300V0 which a 7-level is attained. For the proposed system, a resistive-inductive load is used, and its specification is represented in table 2.

![Simulink Model of the Proposed System](image)

**Table 2. Simulink model specification**

| S. No | Parameter Name                        | Values       |
|-------|---------------------------------------|--------------|
| 1     | Source (Vdc)                          | 100V         |
| 2     | Capacitor (C1, C2)                    | 3000e-6      |
| 3     | Resistive-Inductive load              | 100Ω, 100mH  |
| 4     | Switching Frequency (Fs)              | 1000         |
| 5     | Modulation Index                      | 0.9          |
| 6     | Output voltage (V0)                   | 280V         |

Figure 6 is showing the 7level SC-MLI is 300V, and %THD value is 23.59% in 50Hz with RL load using PD-PWM technique.
In figure 7, 7 level SC-MLI is 300V and % THD value is 7.97% in 50Hz with RL load using POD-PWM technique. THD value of this method is less compared with PD-PWM.

Figure 8 shows the output voltage waveform of 7 level SC-MLI is 300V, and %THD value is 7.87% in 50Hz with RL load using APOD-PWM technique. THD value of this method is less compared with PD-PWM and POD-PWM.
Figure 8. APOD and %THD

Figure 9 represents 7-level SC-MLI is 300V, and %THD value is 15.60% in 50Hz with RL load using VF-PWM technique. THD value of this method is less compared with PD-PWM, POD-PWM, and APOD-PWM.

Figure 9. VF and %THD

Figure 10 shows the output voltage waveform of 7-level SC-MLI is 300V, and %THD value is 7.60% in 50Hz with RL load using CO-PWM technique. THD value of this method is less compared with PD-PWM, POD-PWM, APOD-PWM, and VF-PWM.

Figure 10. CO and %THD
6. Comparative Analysis
A comparison with various MLI is made for providing a fair decision about presented SC-MLI. For comparison, some of the existing 5L, 5L SC-MLI and proposed SC-MLI is proposed in this paper. Analyses are completed based on result levels (NL), number of MOSFET switches (NS), number capacitors (NCap), number of diodes (ND), input sources (NI), and output voltage boosting ratio. The common advantages of 7L-7S SC-MLI structure over the 5L multi-level inverter, existing 5L SC- multi-level inverter is evaluated in the table. 3

| S. No | PWM Techniques | %THD |
|-------|----------------|------|
| 1     | PD             | 23.59|
| 2     | POD            | 7.97 |
| 3     | APOD           | 7.87 |
| 4     | VF             | 15.60|
| 5     | CO             | 7.60 |

7. Conclusion
This study analyses a single stage single phase switched capacitor boost 7L-7S inverter for attaining high output voltage with a single DC source; the input voltage is boosted efficiently with levels. The proposed method reduces the switch count, reduces the maximum number of source required, and reduces the THD of the presented system using different PWM technique is analyzed. Parameter comparison made between the existing (5MLI, Existing SCMLI) and proposed, which provides a better decision about SC-MLI. The comparison provides the %THD value of various PWM techniques in SC-MLI. Results show that the SC-MLI using various PWM techniques and the CO-PWM provides the less %THD value is 4.83 than other methods are done using MATLAB/Simulink. Further reduction of THD values on the system is complex will be done in future.

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