Abstract—Deep learning has grown rapidly thanks to its state-of-the-art performance across a wide range of real-world applications. While neural networks have been trained using IEEE-754 binary32 arithmetic, the rapid growth of computational demands in deep learning has boosted interest in faster, low precision training. Mixed-precision training that combines IEEE-754 binary16 with IEEE-754 binary32 has been tried, and other 16-bit formats, for example Google’s bfloat16, have become popular.

In floating-point arithmetic there is a tradeoff between precision and representation range as the number of exponent bits changes; denormal numbers extend the representation range. This raises questions of how much exponent range is needed, of whether there is a format between binary16 (5 exponent bits) and bfloat16 (8 exponent bits) that works better than either of them, and whether or not denormals are necessary.

In the current paper we study the need for denormal numbers for mixed-precision training, and we propose a 1/6/9 format, i.e., 6-bit exponent and 9-bit explicit mantissa, that offers a better range-precision tradeoff. We show that 1/6/9 mixed-precision training is able to speed up training on hardware that incurs a performance slowdown on denormal operations or eliminates the need for denormal numbers altogether. And, for a number of fully connected and convolutional neural networks in computer vision and natural language processing, 1/6/9 achieves numerical parity to standard mixed-precision.

Index Terms—floating-point, deep learning, denormal numbers, neural network training

I. INTRODUCTION

Larger and more capable neural networks demand ever more computation to be trained. Industry has responded with specialized processors that can speed up machine arithmetic. Most deep learning training is done using GPUs and/or CPUs, which support IEEE-754 binary32 (single-precision) and (for GPUs) binary16 (half-precision).

Arithmetic and load/store instructions with 16-bit numbers can be significantly faster than arithmetic with longer 32-bit numbers. Since 32-bit is expensive for large workloads, industry and the research community have tried to use mixed-precision methods that perform some of the work in 16-bit and the rest in 32-bit. Training neural networks using 16-bit formats is challenging because the magnitudes and the range of magnitudes of the network tensors vary greatly from layer to layer, and can sometimes shift as training progresses.

In this effort, binary16 has not proved to be an unqualified success, mainly because its 5 exponent bits offer a narrow representation range of representable values, even when denormalized floating point numbers (or denormals — see a formal definition in Section III), which add three orders of magnitude to the representation range, are used. Therefore, different allocations of the 15 bits beyond the sign bit, to allow greater representation range, have been tried. Most notably, Google introduced the bfloat16 format, with 8 exponent bits, which until recently was only available on TPU clouds, but is now also included in Nvidia’s latest architecture, Ampere. Experiments have shown that both binary16 and bfloat16 can work, either out of the box or in conjunction with techniques like loss scaling that help control the range of values in software.

Our understanding of these issues needs to be deepened. To our knowledge, no study on the width of the range of values encountered during training has been performed and it has not been determined whether denormal numbers are necessary. To fill this gap, we study here the distribution of tensor elements during training on public models like ResNet and BERT. The data show that the representation range offered by binary16 is fully utilized, with a high percentage of the values falling in the denormal range. Unfortunately, on many machines performance suffers with every operation involving denormals, due to special encoding and handling of the range 1, 2. This raises the question of whether they are needed, or are encountered much less often, when more than 5 exponent bits are utilized. Indeed, bfloat16, with its large representation range, does not support and does not appear to require denormal numbers; but it loses an order of magnitude in numerical accuracy vis-a-vis binary16. Thus, we consider an alternative 1/6/9 format, i.e., one having 6 exponent bits and 9 explicit mantissa bits, both with the denormal range and without it. We demonstrate that this format dramatically decreases the frequency of denormals, which will improve performance on some machines.

In Section II we discuss 16-bit formats that have been previously used in neural network training. In Section III we recall basic notions of floating-point arithmetic and define the notations we use. Section IV presents our testing methodology and details the training settings for each tested network (Section IV-B). The results we gathered are detailed in Sections V and, finally, we conclude in Section VI.
II. RELATED WORK

There have been several 16-bit floating-point (FP) formats proposed for mixed-precision training of neural networks, including half-precision [3–5], Google’s bfloat16 [6, 7], IBM’s DLFloat [8] and Intel’s Flexpoint [9], each with dedicated configurations for the exponent and mantissa bits.

Mixed-precision training using half-precision was first explored by Baidu and Nvidia in [3]. Using half-precision for all training data reduces final accuracy, because the formats fail to cover a wide enough representation range, i.e., small values in half-precision might fall into the denormal range or even become zero. To mitigate this issue, the authors of [3] proposed a mixed-precision training scheme. Three techniques were introduced to maintain SOTA accuracy (comparable to single-precision):

- "master weights", i.e., a single-precision copy of the weights, is maintained in memory and updated with the products of the unscaled half-precision weight gradients and the learning rate. This ensures that small gradients for each minibatch are not discarded as rounding error during weight updates;
- during the forward and backward pass, matrix multiplications take half-precision inputs and compute reductions using single-precision addition (using FMACS instructions as described in Section III). For that activations and gradients are kept in half-precision, halving the required storage and bandwidth, while weights are downcasted on the fly;
- "loss scaling", which empirically rescales the loss before backpropagation in order to prevent small activation gradients that would otherwise underflow in half-precision.

Weight gradients must then be unscaled by the same amount before performing weight updates.

Loss scale factors were initially chosen on a model to model basis, empirically. Automated methods like dynamic loss scaling (DLS) [4, 5], and adaptive loss scale [10] were later developed. These methods allow for the scale to be computed according to the gradient distribution. Using the above techniques has become the standard workflow for many hardware is Google’s bfloat16 [6, 7]. The results presented in [6] reported only the convolutional layers in the forward pass being computed in bfloat16, leading to no accuracy loss on ResNet-50 [12] trained on ImageNet [13].

In subsequent work [7], Intel and Facebook studied the effectiveness of bfloat16 on convolutional and recurrent neural networks, as well as on generative adversarial networks and industrial recommendation systems. The experiments are based on simulations in which bfloat16 arithmetic is modeled by single-precision operations whose results are then rounded to values that are also representable in bfloat16. The results suggest that bfloat16 requires no denormal support and no loss scaling, and therefore, decreases complexity in the context of mixed-precision training. Recently, Nvidia also made it available in its latest architecture, Ampere [14].

IBM’s DLFloat [8] is a preliminary study of the 1/6/9 format that we also examine. DLFloat was tested on convolutional neural networks, LSTMs [15] and transformers [16] of small sizes, implying the potential for minimal or even no accuracy loss. The studied format did not support a denormal range. The authors briefly discuss the factors contributing to the hardware saving, without providing statistics on how they actually influence the training results.

Flexpoint [9] is a blocked floating-point format proposed by Intel. It is different from the previously mentioned formats by that it uses 16 bits for mantissa and shares a 5-bit exponent across each layer. Flexpoint was proposed together with an exponent management algorithm, called Autoflex, aiming to predict tensor exponents based on gathered statistics from previous iterations. The format allowed for un-normalized values to be stored, which invalidated the possibility of a denormal range. For this reason we are not going to study it further in this work.

For all these studies, single-precision training accuracy was achieved. But there is no mention of whether denormals, which significantly impact hardware area and compute speed, are encountered; neither is it tested whether or not they must be supported to achieve that accuracy.

III. FLOATING-POINT ARITHMETIC

Formally defined in Def.3.1, a floating-point (FP) number is most often used in computing as an approximation of a real number. Given a fixed bit width for representation, it offers a trade-off between representation range and numerical accuracy.

Definition 3.1: A real number $X$ is approximated in a machine by a nearby floating-point number:

$$x = M \cdot 2^{E-p+1},$$  \hspace{1cm} (1)

where,

- $E$ is the exponent, a signed integer $E_{\text{min}} \leq E \leq E_{\text{max}}$;
- $M \cdot 2^{-p+1}$ is the significand (sometimes improperly referred to as the mantissa), where $M$ is also a signed integer represented on $p$ bits.

From an engineering standpoint, the exponent is stored as an unsigned integer and offset from the actual value by the exponent bias. In the current work we only consider “vanilla” bias, i.e., equal range around 0, and for this reason we do not add a bias to our definition. For details on the implementation we refer the reader to the IEEE-754 standard [17].

To avoid representation redundancy the finite nonzero FP numbers are normalized. This is done by choosing the representation for which the exponent is minimum. However, this
results in an abrupt convergence towards zero. For this reason, the IEEE-754 standard \[17\] defined the denormal range, that allows for gradual underflow towards 0.

The two different types of representations are as follows:

- when the number is greater than or equal to \(2^{E_{\text{min}}}\) and its representation satisfies \(2^{p-1} \leq |M_x| \leq 2^p - 1\), we say that it is a \textit{normal} number;
- otherwise, one necessarily has \(E = E_{\text{min}},\) and the significand adjusted according to that, with \(|M_x| \leq 2^{p-1} - 1\); the corresponding FP number is called a \textit{subnormal / denormal} number.

From a numerical perspective, supporting denormal numbers offers a wider range of representation, which is desirable. However, traditional hardware implementation of denormals is generally slower, requiring more clock cycles. Moreover, a denormal number is represented with fewer significant bits and with a resulting loss of precision.

The normalized numbers are implemented using the implicit bit convention, in which a binary 1 is appended to the most significant bit (MSB) of the significand, yielding a \(p + 1\) precision. That bit is also called a hidden bit since it isn’t stored in the machine word. In such a system, some data (e.g. number 0) cannot be expressed as a normal or denormal number. For this reason, in order to achieve a “closed” FP system in which any operation is well specified, the standard allows for non-numeric data to be encoded as follows:

- \(E = 0\) and \(M = 0\) is reserved to representing \(\pm 0\);
- \(E = E_{\text{max}}\) and \(M = 0\) represents \(\pm \infty\);
- \(E = E_{\text{max}}\) and \(M \neq 0\) represents NaN (Not a Number).

Considering all the implementation details, a formal definition of a FP system is given in Def. 3.2. For more details on FP systems and their implementation we refer the reader to \[17\], \[18\].

\textit{Definition 3.2:} A floating-point number system is characterized by a quadruple:

\[ s/e/p/d, \tag{2} \]

where,

- \(s\) is the number of sign bits (1 in every case considered here);
- \(e\) the number of exponent bits;
- \(p\) the number of mantissa bits
- \(d\) is either the letter “\(d\)” or “\(n\)” depending on whether denormals are allowed or not.

\textbf{A. Mixed-precision training formats}

As noted in Section \[11\] the two 16-bit mixed-precision formats already used in the deep learning community are \textit{half}-precision (1/5/10/d) and \textit{bfloat16} (1/8/7/n). To these we add our 1/6/9 format. Following the notation introduced in Def. 3.2 we present the specific details in Table I and a representation range visualization in Fig. I

As observed in Fig. I 1/8/7/n offers a very wide representation range, the same as IEEE-754 single-precision.

| \(e\) | \(p\) | \(E_{\text{min}}\) | \(E_{\text{max}}\) | \(\text{min. denormal}\) |
|---|---|---|---|---|
| 1/5/10/d | 5 | 10 | -14 | 15 | \(\pm 2^{-24}\) |
| 1/6/9/d | 6 | 9 | -30 | 31 | \(\pm 2^{-39}\) |
| 1/8/7/n | 8 | 7 | -128 | 127 | — |

Thanks to its 8-bit exponent, its normal range is already wider than the full range, including denormals, of 1/5/10/d or 1/6/9/d, respectively. Also, it is public knowledge that Google TPU’s \[11\] implementation does not offer any support for denormal numbers, and their models are able to converge without issues. This implies that 1/8/7/n mixed-precision training of neural networks does not rely on denormals to achieve SOTA accuracy and for this reason we are not going to discuss this format in what follows.

In comparison, 1/5/10/d offers a much narrower representation range, with only 5 exponent bits. Although it has been adopted as the “standard” mixed-precision in the community, this is largely due to its availability as part of the IEEE-745 standard. As we will show in Section V its full range is being used during training, which may lead to execution slowdown, depending on the hardware platform. For this reason, in this work we introduce 1/6/9/d, which by extending the exponent range by one bit, is able to almost completely avoid denormal numbers.

\textbf{B. Mixed-precision instructions}

Neural network training relies heavily on matrix multiplication, which is performed using multiply and accumulate operations. The IEEE-754 standard only defines instructions on one numerical format at a time, i.e., the input and output variables are represented in the same FP system. In the context of mixed-precision, operations that allow for higher precision outputs have become available. The final result accuracy also depends on the number of rounding operations used, weather or not the instructions is fused. We introduce four possible instructions:

- \textbf{MAC:} \(a_{16} = \circ(a_{16} + \circ(x_{16} \cdot y_{16}))\);
- \textbf{MACS:} \(a_{32} = \circ(a_{32} + \circ(x_{16} \cdot y_{16}))\);
- \textbf{FMAC:} \(a_{16} = \circ(a_{16} + x_{16} \cdot y_{16})\);
- \textbf{FMACS:} \(a_{32} = \circ(a_{32} + x_{16} \cdot y_{16})\),

where, \(\circ\) represents any rounding operation performed and the subscript number gives the bit-width. In the following sections we will discuss the effects of FMAC and FMACS on denormal frequency.
is a state of the art transformer-based application, single consecutive FMAC instructions before adding it to a master accumulator, and resetting the product of half-precision vectors, returning a half-precision result, using this technique. We note here that the number not investigate whether or not it can be greater than 8 half-precision accumulations was empirically chosen; we did not round the products.

When defining a neural network model for our experiments, we insert roundfp operations at the inputs and outputs of every layer, forcing all activations and activation gradients to be cast to the modeled FP format. The weight updates computation is allowed. We bind this kernel to a custom PyTorch function roundfp(X, e, p, d) which performs rounding on both the forward and backward pass.

As a concrete example, when quantizing a torch.nn.Linear layer with input X, weight W and bias B, the forward pass is computed as:

\[ Y = R(R(R(W^T \cdot X)) + R(B)), \]

where \( R() \) is the roundfp function. Inside the matrix multiplication, \( W^T \cdot X \), FMAC or FMACS instructions are used.

Accumulating sums of products using FMAC operations leads to significant loss in final accuracy due to reduced accumulator precision [3]. For this reason, we only perform 8 consecutive FMAC instructions before adding it to a single-precision master accumulator, and resetting the 16-bit accumulator to 0. Algorithm 1 details a fast and accurate dot product of half-precision vectors, returning a half-precision result, using this technique. We note here that the number 8 of half-precision accumulations was empirically chosen; we did not investigate whether or not it can be greater than 8 without affecting accuracy. In what follows we will be using FMAC-8 to mean either this algorithm or a matrix multiplication or convolution in which such sums are accumulated in this manner.

**Algorithm 1** FMAC-8. Dot product of half-precision input vectors \( w \) and \( x \) with half-precision output using FMAC instructions. Superscript number represents the bit width of the variable, + denotes single-precision addition, and \( R() \) is the roundfp operation.

1: \( A^{(32)} = 0; a^{(16)} = 0 \)
2: for \( i \in [0, n) \) do
3: if \( i \mod 8 = 0 \) then
4: \( A^{(32)} = A^{(32)} + a^{(16)} \)
5: \( a^{(16)} = 0 \)
6: end if
7: \( a^{(16)} = \text{FMAC}(a^{(16)}, w_i, x_i) \)
8: end for
9: \( A^{(32)} = A^{(32)} + a^{(16)} \)
10: return \( R(A^{(32)}) \)

**B. Training details**

We evaluated the importance of denormal numbers to neural network training on four different models.

**ResNet** [12] is considered a classic convolutional neural network (CNN), primarily used for computer vision applications such as image classification and object detection. We trained two similar model depths, but using different datasets, with one significantly bigger than the other:

- ResNet20 on Cifar10 dataset [12], trained for 250 epochs with batch size 512 and an initial learning rate 0.1, decayed by 0.1 \times at epochs [100, 150, 200].
- ResNet18 on ImageNet dataset [13] with 1000 classes, trained for 90 epochs with batch size 256 and initial learning rate 0.1, decayed by 0.1 \times at epochs [30, 60, 80].

**BERT** [20] is a state of the art transformer-based [16] model for natural language processing (NLP). Its training consists of two stages, pre-training and fine-tuning. For our scope we focused only on pre-training, since it is the more computationally demanding part. We studied two variations of the model:
- BERT-Tiny [21], a shallow model with only two encoder layers;
- BERT-Base, one of the variants described in the original paper [20], with 12 encoder layers.

Training was done using the OpenWebText dataset for 900k steps with sequence length 128 and batch size 256. We used
a learning rate of $5e-5$ for BERT-Tiny and $1e-4$ for BERT-Base, respectively. The learning rate was scheduled to linearly ramp up at the beginning and then decay over the course of pre-training.

**LSTM** [15] is a long short-term memory network with 2 layers. Similar to the BERT model, we focused on a pretraining task. Training was done using the WikiText dataset with batch size 128 and learning rate $1e-3$, for a total of 10k steps.

**CVAE** [22] is a convolutional variational autoencoder model trained on a protein modeling task [23], using a private protein structure dataset. The model was trained for 3k steps with batch size of 512 and learning rate $1e-4$.

V. Results

Matrix multiplications, at the core of fully connected and convolution layers, account for over 90 percent of the arithmetic in neural network training. For this reason, we monitor tensor elements in fully connected layers and convolutions. During simulations we log the denormal fraction of each layer’s activations, weights, and activation gradients as they are computed and propagated through the network. From there we extract the highest denormal fraction observed across all of the tensors in the model. Most often, activation gradients have smallest magnitudes, since they become smaller with training. This problem is partially solved by dynamic loss scaling (DLS). In addition, denormals may occur during the forward pass of training, as we will show.

We used each of the 16-bit floating-point formats in two training scenarios:

- 16-bit mixed-precision training without dynamic loss scaling (w/o DLS), i.e., none of the tensors are scaled in order to better fit the representation range;
- mixed-precision training with dynamic loss scaling (w/ DLS) [4], which is a common practice in the community.

### A. Using FMAC-8 accumulation

In Table II we document the maximum denormal fraction observed over the entire length of training on hardware that only offers FMAC instructions. For this we applied our FMAC-8 algorithm (Algo. [1]). This fraction can be very high for 1/5/10/d-precision. With DLS enabled, that fraction is reduced, but for LSTM it is still high, notably 60% denormals in a single tensor at some point during training. This shows that denormals can be predominant in the forward pass as well, which is not scaled by the DLS technique. The situation is better with 1/6/9/d-precision. Without DLS there is strong reduction from the fractions seen with 1/5/9/d, but for LSTM the fraction remains high. Finally, the combination of 1/6/9/d-precision and DLS effectively solves the problem of slowdown due to the prevalence of denormals.

| Model       | maximum denormal ratio |
|-------------|------------------------|
|             | 1/5/10/d w/ DLS | 1/5/10/d w/ DLS |
| ResNet20    | 0.95           | 0.05             |
| BERT-Tiny   | 0.9            | 0.25             |
| LSTM        | 0.9            | 0.6              |
| CVAE        | 0.8            | 0.15             |

Fig. 2 shows tensorboard screenshots from our CVAE runs, that showcase different behaviour for different tensors. Taking a closer look at one of the convolution layers (Fig. 2(a)), we see that it is more than 80% denormal for 1/5/10/d training. Applying DLS reduces the fraction to 10%. During the same run, one of the deconvolution layers (showcased in Fig. 2(b)) does not exhibit the same reduction when using DLS, the denormal ratio being approximately the same for both 1/5/10/d runs (w/ and w/o DLS). For these particular layers, 1/6/9/d is able to fully represent the values using only its normal range.

### B. Using FMACS accumulation

Some specialized hardware architectures offer instructions such as FMACS, which allows for accumulation to happen in higher precision. Empirically, this avoids any denormal intermediate computation. This instruction can be found in Nvidia’s GPU architecture, based on TensorCores [24]. When testing this setting we were able to take advantage of GPU architecture and gained speed up, which allowed us to collect statistics on even bigger models like BERT-Base and ResNet18-ImageNet.

In Table III one can observe that using single precision additions in the matrix multiplies reduces the maximum denormal fraction for some networks, like BERT-Tiny. The reason likely is that the threshold for denormals is much lower in single precision. But for CVAE, the use of FMACS instructions doesn’t reduce denormals much, without DLS, and not at all with DLS. The data do suggest that when FMACS is used in conjunction with the 1/6/9/d format, the use of DLS is not needed to make the denormal fraction negligible or at least acceptable. (Note that we cannot compare the ResNet20 with the ResNet18 results, because the datasets used are different, with Imagenet being much larger.)

### C. Training with flushed formats

The data we have presented thus far show that using the 1/6/9/d format reduces the frequency of denormal values enough that it can speed up training on hardware that suffers
a slow-down whenever a denormal value is created. Guided
by the very low denormal ratios reported on 1/6/9/d with
DLS, we also trained using an s/e/p/n FP system (Def. 3.2),
in which denormals are flushed to 0, with no slow-down. The
question then is whether training speed or accuracy suffers.

The convergence results are detailed in Table IV All the
networks achieved SOTA accuracy using our proposed format,
1/6/9/n with DLS. The same cannot be stated about training
with 1/5/10/n, where we observed a significant decrease in
final model accuracy. Note also that the smallest tested
models, which are ResNet20, LSTM and CVAE, converge in
1/6/9/n without DLS.

Table III contains tensorboard screenshots for training BERT-
Tiny in mixed-precision with DLS vs. single-precision. For
reference we include the single-precision training curves,
despite that they are underlying and barely visible. The loss
curves in Fig 3(a) show that 1/5/10/n is the only run that
diverges after 200k training steps, while all others converge
as expected and achieve SOTA final accuracy. This can also
be observed on the Next Sentence Prediction (NSP) training
accuracy in Fig 3(b).

VI. Conclusions

We studied the occurrence of denormal numbers during
mixed-precision training of neural networks. We analyzed two
16-bit formats: 1/5/10/d, which is the same as the IEEE-754
half-precision and a novel 1/6/9/d format that has one more
exponent bit and one fewer significand bit.

Our data suggests that the 1/6/9 format suppress most
denormals because it significantly expands the representation
range of normalized numbers. This can speed up training on
many machines, those that slow down on any computation
involving denormals. Despite the loss of one bit in the signif-
cand, we observed no loss of training speed or final accuracy
compared with 1/5/10, or for that matter with single-precision
(1/8/23) training.

We observed other advantages. No re-tuning of hyperpa-
rameters like the batch size or learning rate was needed.

We saw that the 1/5/10/d format can achieve SOTA as
well, though 1/5/10/n cannot. We did not see any difference
in number of epochs to accuracy between 1/6/9 ("d") or "n") and 1/5/10/d. Thus, denormals are essential when using 1/5/10, even when DLS is employed (see Table 1V). And they occur frequently enough with 1/5/10 to be a performance problem on many platforms.

We found that with DLS, 1/6/9/n trains as accurately and as fast as single-precision, does not suffer a slowdown due to denormals. And that 1/6/9/d is fast and reliable with or without DLS in most cases. Furthermore, we saw that a limited amount of half-precision accumulation is allowable without changing these conclusions.

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