Binary Neural Networks as a general-purpose compute paradigm for on-device computer vision

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Abstract

For binary neural networks (BNNs) to become the mainstream on-device computer vision algorithm, they must achieve a superior speed-vs-accuracy tradeoff than 8-bit quantization and establish a similar degree of general applicability in vision tasks. To this end, we propose a BNN framework comprising 1) a minimalistic inference scheme for hardware-friendliness, 2) an over-parameterized training scheme for high accuracy, and 3) a simple procedure to adapt to different vision tasks. The resultant framework overtakes 8-bit quantization in the speed-vs-accuracy tradeoff for classification, detection, segmentation, super-resolution and matching: our BNNs not only retain the accuracy levels of their 8-bit baselines but also showcase 1.3-2.4× faster FPS on mobile CPUs. Similar conclusions can be drawn for prototypical systolic-array-based AI accelerators, where our BNNs promise 2.8-7× fewer execution cycles than 8-bit and 2.1-2.7× fewer cycles than alternative BNN designs. These results suggest that the time for large-scale BNN adoption could be upon us.

1. Introduction

Why aren’t binary neural networks (BNNs) mainstream? BNNs promise increased compute intensity and reduced memory / data movement requirements, both of which are paramount for deep learning workloads in resource-constrained settings such as wearables, mobile phones and drones. BNNs have also witnessed a significant accuracy boost \cite{21, 41} in ImageNet classification over the years since their inception in 2016 \cite{7}. Yet, despite the efficiency promise and the accuracy advancements, edge applications and deployment frameworks in industry \cite{11, 17, 19} predominantly prefer 8-bit or higher precision over BNNs. Some argues that this is in part still due to the lack of accuracy, as BNNs typically underperform floating-point models, with the exceptions of \cite{1, 25}. Nonetheless, we believe that the bottleneck to large-scale adoption lies instead in the speed-accuracy-tradeoff (SAT) and generality.

First, BNNs do not need to surpass 8-bit networks in accuracy alone; it may be sufficient to simply match 8-bit accuracy but with a more economical resource budget (e.g. latency). However, at the moment, accuracy is typically considered either in isolation or with metrics that are too coarse to reflect resource utilization on-device. A common competition is to “close the gap” between BNN and 8-bit networks without altering model architecture \cite{21, 32, 41}. While this endeavor removes the burden of architecture design for 8-to-1-bit adoption, it ignores the resource disparity between the two and puts BNNs at a natural disadvantage. As a result, the current state-of-the-art BNNs \cite{2, 23, 26, 49} still lag behind 8-bit in accuracy.

It is shown that BNNs with modified network structure could obtain sizeable improvement in the SAT \cite{1, 25, 26, 30}. Yet, most prior work relies on the number of binary operations (BOPS) as a proxy for inference latency, which is overly simplistic for practical applications. BOPS only accounts for the computation latency from convolutions. It ignores significant latency contributors, including memory access \cite{27}, non-linearities, and cross-precision conversions. In addition, without a plausible hardware design, it is difficult and potentially misleading to compare BNN operations with 8-bit operations. For example, the commonly-used conversion of 1 8-bit OP = 64 BOPS \cite{1, 25} is found overly-optimistic in actual hardware instantiations \cite{9, 42, 45}.

Lastly, another roadblock for industry-wide adoption is the lack of confidence in generality. Recent quantization techniques \cite{1, 2, 25} are iterated on ImageNet classification,
Figure 1. Speed-accuracy-tradeoff (SAT) and generality of BiNeal Networks. (a) Quantization-aware training with over-parameterization. Auxiliary parameters and operators (green, shaded boxes) are introduced to enlarge network capacity, enabling BiNeal net to match 8-bit accuracy (Sec. 3.1). (b) Simplified inference form. Once trained, the auxiliary parameters and operators can be absorbed into the original parameters, yielding a inference form with just binary convolution (Sec. 3.2). (c) BiNeal Net has a superior speed-vs-accuracy tradeoff in ImageNet classification than 8-bit and other binary networks. Latency measured using Bolt on Snapdragon 845 Cortex-A75@2.8GHz (Sec. 4.1). (d) Speedup of BiNeal networks over 8-bit on a variety of tasks at the similar accuracy or higher (Sec. 4.2). Accuracy deltas are shown on top the bars. “Bolt-X” is latency measured on CPU X core, “SA-Cycle” are cycles required by a prototypical AI accelerator.

putting in question their transferability to other tasks. In particular, classification is “lossy” in nature: it distills low-bandwidth categorical information from a high-bandwidth input image, discarding visual details in the process. Segmentation [20] and super-resolution [31], on the other hand, typically has higher resolution in the output than the input, and may not tolerate information-loss the same way, as shown in [18, 28, 40]. It therefore remains to be seen how binary methods and network architectures favoured by classification generalize to other tasks.

Driven by these observations, we focus on proving BNN’s superiority in SAT on actual hardware across vision applications. (1) We binarize a ResNet block by enlarging its channels and injecting auxiliary parameters. This modification expands network capacity and helps the BNN to match 8-bit accuracy. Since the enlarged channels are binarized, they are less memory-intensive than 8-bit networks at the original channel count. (2) During inference the BNN is transformed into a simple but mathematically equivalent inference form, where the auxiliary parameters are absorbed into the regular parameters. The bit-widths throughout the block are carefully balanced to both minimize cross-precision conversion and ensure sufficient representation capacity. The resultant block contains almost exclusively binary convolutions, with only one 4-bit addition in the end. No real-valued activation or nonlinearity is needed. The simplicity helps with reducing data movement and bandwidth, and leads to lower latency than other BNN designs and 8-bit networks using existing inference frameworks. It also enables convenient hardware acceleration, which we show using a cycle-calculation formula based on the standard systolic-array hardware design. (3) As the proposed BNN block is a replacement for the commonly-used ResNet blocks, it can be transferred to most computer vision tasks without hyperparameter-tuning (although tuning can still be applied if desired). We show that a straightforward transfer could deliver better SAT than current 8-bit networks.

Our main contributions are as follows:

- We propose a BNN structure, dubbed BiNeal networks (with Binary weights and No real-valued activations), a BNN that obtains state-of-the-art accuracy among other BNNs, while enjoys a simple and parsimonious inference form for on-device deployment.

- We are the first to validate the generality of BNNs. Without introducing additional hyperparameters, our BiNeal structure transfers to classification, detection, segmentation, super-resolution and matching, and outperforms 8-bit networks and BNN alternatives in the SAT for each individual task.

- We derive a metric to evaluate the inference speed of quantized networks in systolic-array based ASIC accelerators. The metric takes into account the latency incurred from by data movement. It simultaneously enjoys more reliability than BOPS, and more convenience than manufacturing actual hardware.
2. Related work

**Binary Neural Networks** BNNs are introduced by [7] where weights and activations are only +1 or −1. This field is popularized by earlier attempts such as XNOR [33], ABC-Net [23], and Bi-Real [26]. Recent work fall into two categories. One focuses on improving quantization algorithms based on the Bi-Real [26] structure, as exemplified by RBNN [21], ReCU [41], and IR-Net [32]. RBNN [21] introduces rotation matrices and angular biases to reduce the quantization loss, ReCU [41] introduces rectified clamp units to revive the "dead weights" for the purpose of reducing quantization error. Yet, these methods do not modify the downsampling operations in Bi-Real networks, which are conducted in floating-point and could incur large memory access.

The other category of methods modify the network structure, as in GroupNet [49], ReActNet [25], BinaryDenseNet [2], and MeliusNet [1]. The modifications enable BNNs to outperform 8-bit networks in accuracy: ReActNet surpasses ResNet18 accuracy [12], while MeliusNet overtakes MobileNet [13]. Nonetheless, it is unclear how the modified BNNs compare with 8-bit networks in on-device inference, as only model size and BOPS are considered for efficiency evaluation.

One notable exception is WRPN [30]. It not only matches full-precision accuracy by enlarging its network structure, but also provides hardware instantiations to showcase the efficiency win. We improve upon their work in three aspects: (i) higher accuracy with the BiNeal structure, (ii) a latency measurement formula that is more realistic than BOPS and does not require publishing ASIC design and synthesis for community adoption, (iii) generalization analysis on non-classification workloads.

**Application outside of classification** While the vast majority of modern BNN approaches report results in ImageNet classification, a few have also started experimenting on object detection and tracking [24, 36, 39, 43]. Yet, most attempts either report results on small-scaled datasets. The only exception is BiDet [39], which fails to bridge the gap with full-precision models on the standard COCO dataset.

**Single image super-resolution** has seen a recent surge in binarization efforts, but these efforts are still balancing between simplicity and accuracy. [40] introduces a simple strategy to replace regular convolutions with binary convolutions, but at the expense of noticeable performance degradation from full-precision. [28] only binarizes weights and [16] introduces scaling factors during inference, both of which sacrifices inference efficiency. BAM [40] and IBTM [18] obtain decent SAT with task-specific network modifications, which is not available for other tasks.

BNN applications on Segmentation have been limited. GroupNet [49] combines BNNs with a segmentation-specific modification to match floating-point performance in PASCAL VOC segmentation, yet its basic version still is underperforming in classification by a large margin, thus lacking generality.

**BNN Inference frameworks** There are multiple inference frameworks [4, 9, 14, 25, 42, 45, 46] that can export a trained BNN for on-device execution. Among them, BitStream [46] and BitFlow [14] are close-sourced; BMXNet [42]’s 1-bit inference speed is slower than floating-point.

There are several open-sourced BNN inference frameworks on ARM, such as daBNN [45], Larq [9], and Bolt. DaBNN proposed an upgraded bit-packing scheme and several speed-up and memory refinement strategies. Larq extends TensorFlow and TensorFlow Lite, and optimizes the implementations of binary operation at assembly level. PhoneBit [4] is a GPU-accelerated BNN inference engine for Android-based mobile devices. Bolt optimizes binary convolution using tilegemm, and it is the fastest binary inference framework on ARM so far. Limited by the scarcity in 1-bit hardware, these inference frameworks have to be shoehorned into existing 8-bit hardware, unable to utilize BNNs to their full potential. Vice versa, BNNs are not designed with these hardware in mind, which means that the architecture choices, such as channel counts, connectivity and operators, may not be aligned with hardware’s preference. As a result, speedups are often less impressive for whole networks on actual devices than for an individual convolution according to the theoretical estimates.

**Latency metric for BNNs** One way to fully exploit the compute and memory efficiency for BNNs is through specialized accelerators. A systolic array is an accelerator architecture design found in popular hardware, e.g. Google’s TPU, Tesla’s FSD [37], and MIT’s Eyeriss [6]. These designs so far are based on floating-point or 8-bit convolutions.

Various efforts have been made on binary accelerators. FINN [38] proposes a framework for binary neural networks inference on FPGA. ReBNN [10] focuses on reducing memory usage when training BNN. WRPN [30] synthesizes an ASIC for multiple precisions including binary. Reproducing latency measurements on specialized ASICs are often expensive, hence we seek to derive a cycle estimation formula based on common features in these designs, yielding a convenient and hardware-grounded latency metric.

3. BiNeal Network

BiNeal net is a combination of a quantization-aware training technique based on over-parameterization (Sec. 3.1), a simplified inference scheme (Sec. 3.2) and a block structure to replace ResNet (Sec. 3.3). We introduce each component below.

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1https://github.com/huawei-noah/bolt
2https://cloud.google.com/tpu/docs/system-architecture-tpu-vm
3.1. Quantization-aware Training with Over-Parameterization

We start with the prototypical convolution operation. During training, we introduce additional parameters and structures that are apparently redundant but conducive to training performance. Over-parametrization appears in XNOR++, ReActNet and many others, but we are the first to absorb the auxiliary parameters in the bias term for efficient on-device deployment. Other BNN approaches only consider computational costs of the convolution operation, and ignore other operations that may introduce extra memory access and impact latency. In a similar fashion as [8], the redundant parameterization can be absorbed into the conventional parameters during inference, at no cost to efficiency.

Let $W \in \mathbb{R}^{N \times C \times K \times K}$, $X \in \mathbb{R}^{B \times H \times W \times C}$ and $A = \text{Conv}(W, X)$ be the weight, input and output of the convolution, where $N, C, H, W, B, K$ are the output channel, input channel, height, width, batch size and kernel size (assumed square for simplicity).

3.1.1 Weight Over-Parameterization

Following DoReFa Net [47], we use floating-point weight $W_f$ for training, and approximately binarize them using $\text{Tanh}$ during the forward pass.

$$W_b = \text{Sign}(\text{Tanh}(\alpha \cdot W_f))$$
$$W_f \approx \lambda \cdot W_b$$

where $\alpha$ and $\lambda$ are auxiliary parameters. $\alpha$ can assume different shapes ($\in \mathbb{R}^N$, or $\mathbb{R}^{N \times C}$, or $\mathbb{R}^{N \times C \times K \times K}$) to adjust the desired degree of over-parameterization, and the magnitude of each $\alpha$ coefficient controls the degree of sharpness of the approximation to binarization. $\lambda \in \mathbb{R}^N$ is a per-output-channel scaling factor, introduced in XNOR [33], to compensate for the magnitude disparity between the unbounded weight $W_f$ and $W_b$ in $\{-1, 1\}$.

Prior work fixes $\alpha$ at 1 [47], and set $\lambda$ to minimize the L1 difference between $W_f$ and $W_b$. Neither is proven ideal for end-to-end performance. Instead, we unfreeze $\alpha$ and $\lambda$ as free parameters, and train them along with the weights.

3.1.2 Activation Over-Parameterization

Since both the approximated weight and the convolution operation are in floating-point, the output is real-valued and must be binarized before being fed to the next layer. Following [25, 26], we approximate the real-valued output $A_f$ using a binarized activation $A_b$ via a series of transformations:

$$A_b = \text{Sign}(\text{Htanh}(\tau A_f + b_0) + b_1))$$
$$A_f \approx \kappa \cdot A_b$$

where $\tau, b_0, b_1 \in \mathbb{R}^n$ and $\kappa \in \mathbb{R}$ are auxiliary parameters, Htanh is the hard-tanh function [26]. It clamps the input at $[-1, 1]$ during the forward pass, and uses sinusoids in the backward pass. PReLU [25] and Sign uses Straight-Through-Estimator to compute gradients.

At first sight the formulation above makes little sense, as 1) the transformations could be merged into an equivalent, per-channel thresholding operation, 2) the scale $\tau$ and biases $b_0$ are redundant given that $A_f$ is typically proceeded by a BatchNorm with its own learnable scale and bias. Nonetheless, as shown in [25], the over-parameterized formulation reshapes input distributions, which helps conditioning BNN training. Capitalizing on this phenomenon, we also assign scale and biases to the Sign function.

3.2. Parameter-fused Inference

The auxiliary parameters and non-linearities in training can be absorbed into a simple form during inference. Essentially, binarization only concerns with the relative value of two numbers, and disregards their magnitude. Exploiting this property, weight binarization in Eq. 1 is equivalent to:

$$W_b = \text{Sign}(\alpha) \cdot \text{Sign}(W_f)$$

Similarly, for each output channel $n$, the activation binarization in Eq. 2 is equivalent to:

$$A_b(n) = \text{Sign}(\tau(n)) \cdot \text{Sign}(A_f(n) - \theta(n))$$

where $\theta(n) \in \mathbb{R}$ is a threshold that depends on the $b_0(n), b_1(n)$ and $\tau(n)$ for channel $n$. This simplification

![Diagram](image-url)
owes to the fact that all transformations in Eq. 2 are monotonic given \(b_0(n), b_1(n)\) and \(\tau(n)\), thus one only needs to solve for the zero-point \(\theta(n)\) to determine the sign of \(A_k(n)\). The form and derivation can be found in (Appendix, A).

Finally, the convolutional output can be approximated by:

\[
\text{Conv}(W_f, A_f) \approx (\kappa \cdot \lambda)\text{Conv}(W_b, A_b)
\]  

(5)

3.2.1 BatchNorm Fusion

\((\kappa \cdot \lambda) \in R^N\) in Eq. 5 is a per-channel scaling factor that is carried into the next layer. Fortunately, they can be absorbed into the PReLU operation in the next layer, and thus do not need to be computed during inference. More generally, BatchNorms are also amenable to parameter-fusion. Let \(\gamma, \beta \in R^N\) be the BatchNorm scale and bias:

\[
\begin{align*}
\text{PReLU}(\tau \cdot \text{BN}(x) + b_0) + b_1 \\
= \text{PReLU}(\tau \cdot (\gamma \cdot x + \beta) + b_0) + b_1 \\
= \text{PReLU}((\tau \cdot \gamma) \cdot x + (\tau \cdot \beta + b_0)) + b_1
\end{align*}
\]

Then the PReLU parameters are collapsed the same way as described in Eq. 4.

To summarize, we take the over-parameterized form in Sec. 3.1 and simplify it by fusing the auxiliary parameters. The resultant inference form only involves bit-wise convolution and thresholding, as shown in Fig. 1.

3.3. Efficient Inference Block Design

After addressing binarization for a single convolution, we proceed to describe our strategy for binarizing a whole network. We design a binary block based on BasicBlock [12], the basic building block for ResNet-18 and one of the most versatile blocks found in backbone designs across vision tasks. Similar to Bi-Real blocks [26], our binary block serves as a drop-in replacement for BasicBlock with no additional hyperparameters.

Our design is illustrated in Fig. 2(c). Specifically: 1) Regular convolutions in the BasicBlock are replaced with binary convolutions described in Sec 3.2. The input and output channel counts are multiplied by a factor \(m\) \((m = 2\) in the experiments). 2) The skip connection is always equipped with a binary convolution, regardless of whether the layer downsamples or not. 3) Inputs into the elementwise-add are encoded in INT4. The sum is converted to 1-bit.

Compared to other BNN blocks such as Bi-Real, our block has the following properties. First, convolution inputs are all in 1-bit, eliminating the need for frequent precision conversion, and reducing the overall amount of data movement. Second, it does not contain PReLU, Sign or other nonlinearities. This eliminates the need for additional circuitry. Last, the skip connection is lightweight: both the additional convolution and the output are 1-bit, as opposed to being real-valued in Bi-Real.

The simplicity of our block design delivers tangible latency benefits compared to alternative designs. Yet, it is not conveniently reflected in conventional complexity metrics such as BOPS or model size. In the section below, we describe a 1-bit ASIC accelerator design based on the classical systolic array, and derive a formula to calculate the compute cycles required for different blocks.

3.4. 1-bit Systolic Array Design

We inherit a systolic array design in Fig. 3(a) for accelerating 8-bit convolution. It is prototypical to use a square array to ensure identical bandwidth for data-loads as well as writes without loss of generality. In turn, the input and output bandwidths (to and from SRAM) are typically identical. It is also common to store data in NHWC format (data arranged along each channel first).

To create a 1-bit systolic array, we replace the 8-bit PEs with 1-bit PEs. To utilize the full input bandwidth, we replace each 8-bit input with 8 1-bit input lines, essentially creating \(8 \times \) as many rows in the 1-bit design. As the array is square, the number of columns is also \(8 \times \). This translates to 64 \times more PEs, and a theoretical 64 \times speedup compared to 8-bit. PPA (performance or speed, power, and area) are the three key metrics for an ASIC. We use cycles as a proxy for speed of the ASIC, and derive a formula below for the total cycle count during inference of a given neural network. We also provides area and energy comparisons in (Appendix, B).

3.5. Cycle Metric

In practice, speedup is often subject to factors such as array utilization, data movement, as well as the non-convolution parts of the workload. Based on the systolic-array design, we derive a set of formulae that describes the number of cycles required to process a network.

We assume that the weights are not dynamically generated during inference. This means that they are known in advance and can be pre-arranged to the desired NHWC format without incurring latency.

A benefit of the systolic-array design is that in-place operations can be pipelined (no additional cycles required) as long as they do not alter bit-depth. For example, BatchNorm and scaling can be considered cycle-free. As a result, to compute the cycles for blocks in Fig. 2, one needs to consider convolution, bit-depth conversion, and elementwise-add. We briefly present their formulae below, and leave the derivations to the Appendix, C.

Let the array size be \(S \times S\). For example, \(S=128\) in Fig. 2(a). Denote \(M\) the input bandwidth (in bits per cycle), \(P\) the size of Psum memory (i.e. the number of partial sums that can be stored on-chip), and \(N, H, W, C\) represent...
3.5.1 Convolution

The cycle count for the computational portion in a convolution is given by:

$$T(*) = \left\lceil \frac{N}{S} \right\rceil \left\lceil \frac{WH}{P} \right\rceil S$$ (7)

When the input and output have identical bit-depth (e.g. 1-bit in and 1-bit out), the cycles for the entire convolution is given by:

$$T(\text{Conv}_{1\rightarrow1}) = WHK \left\lceil \frac{CK}{S} \right\rceil \left\lceil \frac{N}{S} \right\rceil + T(*)$$ (8)

When the output bit-depth $b$ is higher (e.g. 1-bit in and 8-bit out), the outgoing data will get congested. As input and output bandwidths are identical, higher output bit-depth translates to small number of results written per cycle. As a consequence, additional cycles, of number proportional to the output bit-depth $b$, are expensed in data movement:

$$T(\text{Conv}_{1\rightarrow b}) = WHK \left( \left\lceil \frac{CK}{S} \right\rceil - 1 + b \right) \left\lceil \frac{N}{S} \right\rceil + T(*)$$ (9)

3.5.2 Quantization and Sign

One may need to re-quantize an input if its bit-depth does not match that of the PE (e.g. converting an real-valued input to 1-bit in Bi-Reall). The cycle cost is essentially identical to the cost of reading the input feature map:

$$T(\text{read}) = WH \left\lceil \frac{C}{S} \right\rceil S/M$$ (10)

3.5.3 Elementwise Operations

The write portion of elementwise-sum can be pipelined and thus omitted in cycle calculations. The cycle count is given by those of reading the two inputs:

$$T(+) = 2T(\text{read})$$ (11)

So far, we have outlined all cycle calculations necessary for analysing blocks listed in Fig. 2. Please refer to the (Appendix. C for an extensive list and derivations.

3.5.4 Cycles for Common Network Blocks

We instantiate a typical systolic-array design using $S = 128$, $P = 1024$ and $M = 128$. We use this setup to compute the cycles for network blocks in Fig. 2 as well as full networks in the experiments.

The cycle counts for various block designs are shown in Tab. 1. BiNeal blocks are more amenable to acceleration despite having less BOPS with the other designs.

4. Experiments

Despite progress in quantized training for BNNs, there remains a discernible performance gap between BNNs and...
their floating-point (FP) counterparts. Similar to WRPN [30], BiNeal nets uniformly expand their constituent blocks by a channel multiplier. We compare BiNeal nets under various multiplier settings against FP, 8-bit and BNN models on ImageNet classification in Sec. 4.1. We examine the latency on mobile devices and cycle metrics, showing superior SAT with BiNeal net’s simple design. We then demonstrate BiNeal net’s general applicability on object detection, semantic segmentation, single-frame super-resolution and image matching in Sec.4.2.

### 4.1. SAT on Classification

We conduct classification experiments on ImageNet. Tab.2 displays the performance comparison among the proposed BiNeal nets, with ResNet-18 [12], [26] (floating-point (FP) and 8-bit) and popular BNNs, namely Bi-Real [26], ReActNet [25], MeliusNet [1], RBNN [21] and ReCU [41].

All models are tested on the Snapdragon 845 CPU (Cortex-A75@2.8GHz). For each method we choose the best inference engine. Overall, FP and 8-bit models prefer TFLite whereas 1-bit models are consistently faster on Bolt. We systematically vary the multiplier to sweep a SAT curve.

With a channel multiplier of \(m = 1.5\), our BiNeal net matches 8-bit ResNet-18 while achieving a \(1.9\times\) speedup on Bolt and a \(7.0\times\) speedup measured by cycle metric. Our method is also \(1.1\times / 2.7\times\) faster in latency / cycles than ReActNet-A, the most competitive BNN alternatives.

### 4.2. Generality

We proceed to demonstrate BiNeal net’s performance on common vision tasks. We deliberately avoid architecture specialization and choose one multiplier \(m = 2\) for all tasks. We use Cosine Annealing LR and WD=1E-5 for all tasks. While the performance per task may be further improved by structural and hyper-parameter tuning, the one-size-fits-all protocol seeks to establish a transferability baseline. This baseline not only helps with our generality assessment, but also mimics the practical setting of deploying models on novel tasks under time pressure.

As 8-bit typically achieves less or equal accuracy than FP networks, we chivalrously assume that 8-bit could achieve FP accuracy in our comparison. All below baseline models are considered as 8-bit and the latency is tested on Bolt with Snapdragon 845 Cortex-A75@2.8GHz. We describe the setup and results for each task below.

#### 4.2.1 Detection

Our detection experiment is conducted on COCO using the mmdetection [5] implementation. We choose two popular model architectures: the anchor-free centernet [48] and the anchor-based faster-rcnn [34] with fpn [22]. The backbone for both model are ResNet-18, which we replace with BNNs. This allows us to reuse the binary classification models mentioned in Sec. 4.1 as pre-trained backbone initializations. We keep all the settings the same with that from origin FP network.

The results are shown in Tab. 3. For Centernet we re-
port the mmdetection result [5] (which is higher than the original paper [48]). CenterNet-ours* refers to the model where both the backbone and head are binarized with the multiplier \( m = 2 \).

CenterNet with BiNeal backbones achieves comparable performance as the 8-bit model. Binarized CenterNet outperforms 8-bit model with \( 1.3 \times \) latency speedup. Binarized RCNN outperforms 8-bit model with \( 2.0 \times \) faster inference latency and \( 3.1 \times \) less cycles.

### 4.2.2 Segmentation

Our segmentation experiment is based on the CityScape [5] dataset, implemented with mmsegmentation [5]. Similar to detection, we binarize ResNet-18 backbones and pretrain them on ImageNet. We binarize FCN [31] using the proposed binary scheme and keep all the settings the same with that from original FP network.

Tab. 4 shows that our binarized model achieves comparable performance with the 8-bit model. Our binary model achieves \( 1.4 \times \) speedup on Bolt and \( 3.9 \times \) speedup on cycle metric.

|          | mIoU  | Bolt Latency (ms) | Cycle (G) |
|----------|-------|-------------------|-----------|
| FCN [5]  | 70.24 | 1230              | 81.16     |
| Ours     | 70.07 | 883.46            | 20.62     |

Table 4. Performance comparison of segmentation on cityscape. Bolt latency and cycle estimation are based on the input with \( 512 \times 1024 \times 3 \).

### 4.2.3 Super-resolution

For single-frame super-resolution, we embed BNNs in EDSR [20], which is one of the most iconic networks in the SR. The original network is extremely large, making channel expansion difficult. Instead, we binarize the smaller version of EDSR in the official release, which also matches the performance of the original. The smaller network differs in the following sense: (1) it uses 16 residual blocks instead of 32, (2) each block has 64 channels instead of 256, (3) we follow IBTM [18] and set the residual scale parameter to 1 instead of 0.1.

We leave the first and last layers of the network in 8-bit, and replace all the residual blocks by BiNeal blocks with \( m = 2 \). We follow the training settings of EDSR, except that we also follow [18] to normalize the input to 1 instead of 255.

We compare our method with previous SR networks, including EDSR [20] and EDSR-IBTM [18]. Tab. 5 shows that our proposed binary EDSR networks have equivalent PSNR and SSIM score compared with the full precision model, but achieve \( 2.4 \times \) lower latency and \( 2.8 \times \) less cycles.

### 4.2.4 Matching

For image matching, we applied our binary scheme to R2D2 [35]. We binarize most the network and leave the last two output layers intact. L2-Net consists mostly of convolutions. Every two consecutive convolutions could be regarded as a BasicBlock without skip connections. Therefore, we use four BiNeal blocks with \( m = 2 \) to replace eight floating-point convolution layers in L2-Net. We train the binary R2D2 model on Web image (W), Aachen day-time images (A) and Aachen optical flow pairs (F) and evaluate it on HPatches dataset. Mean Matching Accuracy (MMA) at an error threshold of 3px is the most popular accuracy metric for matching. Experimental results are shown in Tab. 7.

Our binary R2D2 model achieves better matching performance than the 8-bit model, at the same time achieves \( 2.1 \times \) speedup while inference using Bolt, and achieves \( 3.4 \times \) speedup evaluated by the cycle metric.

### 5. Conclusion

We identified SAT superiority and generality as the two missing links to BNN’s industrial success. Designed with inference efficiency in mind, our BNN managed to match 8-bit performance with greater frugality. This frugality was observed both in terms of direct latency measurements on mobile CPUs and theoretical cycle counts for prototypical AI accelerators. Moreover, the SAT advantage was observed across everyday vision workloads including classification, detection, segmentation, super-resolution and matching, delivering a consistent \( 1.3-2.4 \times \) speedup on ARM CPU. Cycle analysis reveals that the speedup could be \( 2.8-7.0 \times \) with a dedicated ASIC design. Importantly, our BNN framework adapts to these tasks without much need for hyperparameter-tuning. These results suggest that BNNs are general learners of computer vision tasks, and the opportune choice for replacing 8-bit as the default inference paradigm in resource-hungry scenarios.

### References

[1] Joseph Bethge, Christian Bartz, Haojin Yang, Ying Chen, and Christoph Meinel. Meliusnet: Can binary neural networks achieve mobilenet-level accuracy? arXiv preprint arXiv:2001.05936, 2020. 1, 3, 7

[2] Joseph Bethge, Haojin Yang, Marvin Bornstein, and Christoph Meinel. Binarydensenet: developing an architecture for binary neural networks. In Proceedings of the IEEE/CVF International Conference on Computer Vision Workshops, pages 0–0, 2019. 1, 3
| Method    | scale | Param   | Set5 PSNR/SSIM | Set14 PSNR/SSIM | B100 PSNR/SSIM | Urban100 PSNR/SSIM |
|-----------|-------|---------|----------------|-----------------|----------------|-------------------|
| EDSR      | x2    | 40.73M  | 38.19/0.960    | 33.95/0.918     | 32.35/0.902    | 32.97/0.936       |
| EDSR      | x2    | 1.370M  | 37.81/0.959    | 33.34/0.913     | 32.04/0.898    | 31.46/0.922       |
| EDSR      | x2    | 31.73M  | 37.80/0.960    | 33.38/0.916     | 32.04/0.898    | 31.49/0.922       |
| EDSR ours | x2    | 5.039M  | 38.85/0.959    | 33.36/0.914     | 32.06/0.898    | 31.46/0.923       |
| EDSR      | x3    | 40.73M  | 36.68/0.928    | 30.53/0.844     | 29.26/0.809    | 28.81/0.868       |
| EDSR      | x3    | 1.370M  | 34.24/0.924    | 30.23/0.836     | 29.03/0.802    | 27.83/0.844       |
| EDSR ours | x3    | 31.73M  | 34.10/0.924    | 30.11/0.838     | 28.93/0.801    | 27.49/0.839       |
| EDSR      | x3    | 5.039M  | 34.19/0.925    | 30.23/0.838     | 29.02/0.803    | 27.80/0.848       |
| EDSR      | x4    | 40.73M  | 32.48/0.894    | 28.82/0.781     | 27.72/0.736    | 26.65/0.805       |
| EDSR      | x4    | 1.370M  | 32.14/0.888    | 28.56/0.773     | 27.56/0.728    | 25.89/0.778       |
| EDSR ours | x4    | 31.73M  | 31.94/0.887    | 28.47/0.771     | 27.49/0.726    | 25.80/0.776       |
| EDSR      | x4    | 5.039M  | 31.94/0.887    | 28.47/0.771     | 27.49/0.726    | 25.80/0.776       |

Table 5. EDSR Result comparison. Models are evaluated on Set5 [3], Set14 [44], B100 [29], Urban [15].

| model     | Bolt Latency (ms) | Cycle (G) |
|-----------|-------------------|-----------|
| EDSR      | 9258.1            | 307.7     |
| Ours      | 3939.4            | 110.9     |

Table 6. Performance comparison of SR. Bolt latency and cycle estimation are based on the input with 192 × 192 × 3.

| model     | MMA@3 Bolt Latency (ms) | Cycle (G) |
|-----------|-------------------------|-----------|
| R2D2      | 0.686                   | 14942     |
| WRPN      | 0.645                   | 5973      |
| ours      | 0.692                   | 7262      |

Table 7. Performance comparison of MMA@3 on HPatches. Bolt latency and cycle estimation are based on the input with 598 × 796 × 3.

[3] Marco Bevilacqua, Aline Roumy, Christine Guillemot, and Marie Line Alberi-Morel. Low-complexity single-image super-resolution based on nonnegative neighbor embedding. 2012.

[4] Gang Chen, Shengyu He, Haitao Meng, and Kai Huang. Phonebit: efficient gpu-accelerated binary neural network inference engine for mobile phones. In 2020 Design, Automation & Test in Europe Conference & Exhibition (DATE), pages 786–791. IEEE, 2020.

[5] Kai Chen, Jiaqi Wang, Jiangmiao Pang, Yuhang Cao, Yu Xiong, Xiaoxiao Li, Zhiwei Sun, Wansen Feng, Ziwei Liu, Jiarui Xu, et al. Mmdetection: Open mmlab detection tool-box and benchmark. arXiv preprint arXiv:1906.07155, 2019.

[6] Yu-Hsin Chen, Tushar Krishna, Joel S Emer, and Vivienne Sze. Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks. IEEE journal of solid-state circuits, 52(1):127–138, 2016.

[7] Matthieu Courbariaux, Itay Hubara, Daniel Soudry, Ran El-Yaniv, and Yoshua Bengio. Binarized neural networks: Training deep neural networks with weights and activations constrained to+ 1 or-1. arXiv preprint arXiv:1602.02830, 2016.

[8] Xiaohan Ding, Xiangyu Zhang, Ningning Ma, Jungong Han, Guiguang Ding, and Jian Sun. Repvgg: Making vgg-style convnets great again. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 13733–13742, 2021.

[9] Lukas Geiger and Plumerai Team. Larq: An open-source library for training binarized neural networks. Journal of Open Source Software, 5(45):1746, 2020.

[10] Tianchan Guan, Peiye Liu, Xiaoyang Zeng, Martha Kim, and Mingoo Seok. Recursive binary neural network training model for efficient usage of on-chip memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(7):2593–2605, 2019.

[11] Philipp Gysel, Jon Pimentel, Mohammad Motamedi, and Soheil Ghiasi. Ristretto: A framework for empirical study of resource-efficient inference in convolutional neural networks. IEEE transactions on neural networks and learning systems, 29(11):5784–5789, 2018.

[12] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. Deep residual learning for image recognition. In Proceedings of the IEEE conference on computer vision and pattern recognition, pages 770–778, 2016.

[13] Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. Mobilenets: Efficient convolutional neural networks for mobile vision applications. arXiv preprint arXiv:1704.04861, 2017.

[14] Yuwei Hu, Jidong Zhai, Dinghua Li, Yifan Gong, Yuhao Zhu, Wei Liu, Lei Su, and Jiangming Jin. Bitflow: Exploiting vector parallelism for binary neural networks on cpu. In 2018 IEEE International Parallel and Distributed Processing Symposium (IPDPS), pages 244–253. IEEE, 2018.

[15] Jia-Bin Huang, Abhishek Singh, and Narendra Ahuja. Single image super-resolution from transformed self-exemplars. In
[16] Qiu Huang, Yuxin Zhang, Haoji Hu, Yongdong Zhu, and Zhifeng Zhao. Binarizing super-resolution networks by pixel-correlation knowledge distillation. In 2021 IEEE International Conference on Image Processing (ICIP), pages 1814–1818. IEEE, 2021.

[17] Benoit Jacob, Skirmantas Kligys, Bo Chen, Menglong Zhu, Matthew Tang, Andrew Howard, Hartwig Adam, and Dmitry Kalenichenko. Quantization and training of neural networks for efficient integer-arithmetic-only inference. In Proceedings of the IEEE conference on computer vision and pattern recognition, pages 2704–2713, 2018.

[18] Xinrui Jiang, Nannan Wang, Jingwei Xin, Keyu Li, Xi Yang, and Xinbo Gao. Training binary neural network without batch normalization for image super-resolution. In Proceedings of the AAAI Conference on Artificial Intelligence, volume 35, pages 1700–1707, 2021.

[19] Raghuraman Krishnamoorthi. Quantizing deep convolutional networks for efficient inference: A whitepaper. arXiv preprint arXiv:1806.03842, 2018.

[20] Bee Lim, Sanghyun Son, Heewon Kim, Seungjun Nah, and Kyoung Mu Lee. Enhanced deep residual networks for single image super-resolution. In Proceedings of the IEEE conference on computer vision and pattern recognition workshops, pages 136–144, 2017.

[21] Mingbao Lin, Rongrong Ji, Zihan Xu, Baochang Zhang, Yan Wang, Yongjian Wu, Feiyue Huang, and Chia-Wen Lin. Rotated binary neural network. arXiv preprint arXiv:2009.13053, 2020.

[22] Tsung-Yi Lin, Piotr Dollár, Ross Girshick, Kaiming He, Bharath Hariharan, and Serge Belongie. Feature pyramid networks for object detection. In Proceedings of the IEEE conference on computer vision and pattern recognition, pages 2117–2125, 2017.

[23] Xiaofan Lin, Cong Zhao, and Wei Pan. Towards accurate binary convolutional neural network. arXiv preprint arXiv:1711.11294, 2017.

[24] Chunlei Liu, Wenrui Ding, Xin Xia, Yuan Hu, Baochang Zhang, Jianzhuan Liu, Bohan Zhuang, and Guodong Guo. Rbcn: Rectified binary convolutional networks for enhancing the performance of 1-bit dcnn. arXiv preprint arXiv:1908.07749, 2019.

[25] Zechun Liu, Zhiqiang Shen, Marios Savvides, and Kwang-Ting Cheng. Reactnet: Towards precise binary neural network with generalized activation functions. In European Conference on Computer Vision, pages 143–159. Springer, 2020.

[26] Zechun Liu, Baoyuan Wu, Wenhao Luo, Xin Yang, Wei Liu, and Kwang-Ting Cheng. Bi-real net: Enhancing the performance of 1-bit cnns with improved representational capability and advanced training algorithm. In Proceedings of the European conference on computer vision (ECCV), pages 722–737, 2018.

[27] Ningning Ma, Xiangyu Zhang, Hai-Tao Zheng, and Jian Sun. Shufflenet v2: Practical guidelines for efficient cnn architecture design. In Proceedings of the European conference on computer vision (ECCV), pages 116–131, 2018.

[28] Yinglan Ma, Hongyu Xiong, Zhe Hu, and Lizhuang Ma. Efficient super resolution using binarized neural network. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition Workshops, pages 0–0, 2019.

[29] David Martin, Charless Fowlkes, Doron Tal, and Jitendra Malik. A database of human segmented natural images and its application to evaluating segmentation algorithms and measuring ecological statistics. In Proceedings Eighth IEEE International Conference on Computer Vision. ICCV 2001, volume 2, pages 416–423. IEEE, 2001.

[30] Asit Mishra, Eriko Nurvitadhi, Jeffrey J Cook, and Debbie Marr. Wrpn: Wide reduced-precision networks. arXiv preprint arXiv:1709.01134, 2017.

[31] Hyeonwoo Noh, Seunghoon Hong, and Bohyung Han. Learning deconvolution network for semantic segmentation. In Proceedings of the IEEE international conference on computer vision, pages 1520–1528, 2015.

[32] Haotong Qin, Ruihao Gong, Xianglong Liu, Mingzhu Shen, Ziran Wei, Fengwei Yu, and Jingkuan Song. Forward and backward information retention for accurate binary neural networks. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 2250–2259, 2020.

[33] Mohammad Rastegari, Vicente Ordonez, Joseph Redmon, and Ali Farhadi. Xnor-net: Imagenet classification using binary convolutional neural networks. In European conference on computer vision, pages 525–542. Springer, 2016.

[34] Shaoqing Ren, Kaiming He, Ross Girshick, and Jian Sun. Faster r-cnn: Towards real-time object detection with region proposal networks. Advances in neural information processing systems, 28:91–99, 2015.

[35] Jerome Revaud, Philippe Weinzaepfel, César De Souza, Noe Pion, Gabriela Csurka, Yohann Cabon, and Martin Humenberger. R2d2: repeatable and reliable detector and descriptor. arXiv preprint arXiv:1906.06195, 2019.

[36] Siyang Sun, Yingjie Yin, Xingang Wang, De Xu, Wenzhi Wu, and Qingyi Gu. Fast object detection based on binary deep convolution neural networks. CAAI transactions on intelligence technology, 3(4):191–197, 2018.

[37] Emil Talpes, Debjit Das Sarma, Ganesh Venkataramanan, Peter Bannon, Bill McGee, Benjamin Floering, Ankit Jalote, Christopher Hsiong, Sathil Arora, Atchuthy Gorti, et al. Compute solution for tesla’s full self-driving computer. IEEE Micro, 40(2):25–35, 2020.

[38] Yaman Umuroglu, Nicholas J Fraser, Giulio Gambardella, Michaela Blott, Philip Leong, Magnus Jahre, and Kees Vissers. Finn: A framework for fast, scalable binarized neural network inference. In Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 65–74, 2017.

[39] Ziwei Wang, Ziyi Wu, Jiwen Lu, and Jie Zhou. Bidet: An efficient binarized object detector. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 2049–2058, 2020.

[40] Jingwei Xin, Nannan Wang, Xinrui Jiang, Jie Li, Heng Huang, and Xinbo Gao. Binarized neural network for single
image super resolution. In European Conference on Computer Vision, pages 91–107. Springer, 2020. 2, 3

[41] Zihan Xu, Mingbao Lin, Jianzhuang Liu, Jie Chen, Ling Shao, Yue Gao, Yonghong Tian, and Rongrong Ji. Recu: Reviving the dead weights in binary neural networks. arXiv preprint arXiv:2103.12369, 2021. 1, 3, 7

[42] Haojin Yang, Martin Fritzscbe, Christian Bartz, and Christoph Meinel. Bmxnet: An open-source binary neural network implementation based on mxnet. In Proceedings of the 25th ACM international conference on Multimedia, pages 1209–1212, 2017. 1, 3

[43] Li Yang, Zhezhi He, and Deliang Fan. Binarized depthwise separable neural network for object tracking in fpga. In Proceedings of the 2019 on Great Lakes Symposium on VLSI, pages 347–350, 2019. 3

[44] Roman Zeyde, Michael Elad, and Matan Protter. On single image scale-up using sparse-representations. In International conference on curves and surfaces, pages 711–730. Springer, 2010. 9

[45] Jianhao Zhang, Yingwei Pan, Ting Yao, He Zhao, and Tao Mei. dabnn: A super fast inference framework for binary neural networks on arm devices. In Proceedings of the 27th ACM international conference on multimedia, pages 2272–2275, 2019. 1, 3

[46] Tianli Zhao, Xiangyu He, Jian Cheng, and Jing Hu. Bitstream: Efficient computing architecture for real-time low-power inference of binary neural networks on cpus. In Proceedings of the 26th ACM international conference on Multimedia, pages 1545–1552, 2018. 3

[47] Shuchang Zhou, Yuxin Wu, Zekun Ni, Xinyu Zhou, He Wen, and Yuheng Zou. Dorefa-net: Training low bitwidth convolutional neural networks with low bitwidth gradients. arXiv preprint arXiv:1606.06160, 2016. 4

[48] Xingyi Zhou, Dequan Wang, and Philipp Krähenbühl. Objects as points. arXiv preprint arXiv:1904.07850, 2019. 7, 8

[49] Bohan Zhuang, Chunhua Shen, Mingkui Tan, Lingqiao Liu, and Ian Reid. Structured binary neural networks for accurate image classification and semantic segmentation. In Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 413–422, 2019. 1, 3
Appendix A. Fusion of Auxiliary Parameters

As shown in Eq. 6, batchnorm can be absorbed into the PReLU operation in the next layer, so it is equivalent to Eq. 2. Now, we derive Eq. 4 below.

We define $x$ as:

$$x = \tau A_f + b_0$$

So Eq.6 can be defined as:

$$A_b = \text{Sign}(H\text{tanh}(\text{PReLU}(x) + b_1))$$

$$= \text{Sign}(\text{PReLU}(x) + b_1)$$

Let $\alpha$ as the parameter of PReLU, $\alpha > 0, \alpha \in R^N$, so PReLU can be defined as:

$$\text{PReLU}(x) = \begin{cases} 
\alpha x, & x \leq 0 \\
0, & x > 0
\end{cases}$$

We split Eq.13 in two parts.

Case 1: $b_1 \leq 0$

$$A_b = \text{Sign}(\text{PReLU}(x) + b_1)$$

$$= \text{Sign}(\alpha x + b_1)$$

$$= \begin{cases} 
-1, & x \leq -b_1/\alpha \\
1, & x > -b_1/\alpha
\end{cases}$$

Case 2: $b_1 > 0$

$$A_b = \text{Sign}(\text{PReLU}(x) + b_1)$$

$$= \text{Sign}(x + b_1)$$

$$= \begin{cases} 
-1, & x \leq -b_1 \\
1, & x > -b_1
\end{cases}$$

Considering Eq.12, Eq.15, Eq.16, we divide Eq. 2 into four cases. (We exclude the trivial scenario of $\tau = 0$)

Case 1: $\tau < 0$ and $b_1 \leq 0$

$$A_b = \begin{cases} 
1, & A_f < -b_1/\alpha \tau - b_0 \\
-1, & A_f \geq -b_1/\alpha \tau - b_0
\end{cases}$$

Case 2: $\tau < 0$ and $b_1 > 0$

$$A_b = \begin{cases} 
1, & A_f < -b_1/\tau - b_0 \\
-1, & A_f \geq -b_1/\tau - b_0
\end{cases}$$

Case 3: $\tau > 0$ and $b_1 \leq 0$

$$A_b = \begin{cases} 
1, & A_f > -b_1/\alpha \tau - b_0 \\
-1, & A_f \leq -b_1/\alpha \tau - b_0
\end{cases}$$

Case 4: $\tau > 0$ and $b_1 > 0$

$$A_b = \begin{cases} 
1, & A_f > -b_1/\tau - b_0 \\
-1, & A_f \leq -b_1/\tau - b_0
\end{cases}$$

We merge the cases above as:

$$A_b = \begin{cases} 
\text{Sign}(\tau)\text{Sign}(A_f + b_0 + b_1/\alpha \tau), & b_1 \leq 0 \\
\text{Sign}(\tau)\text{Sign}(A_f + b_0 + b_1/\tau), & b_1 > 0
\end{cases}$$

So, the $\theta(n)$ in Eq. 4 can be solved with:

$$\theta = \begin{cases} 
-b_1/\alpha \tau - b_0, & b_1 \leq 0 \\
-b_1/\tau - b_0, & b_1 > 0
\end{cases}$$

Appendix B. Area and Energy

For simplicity, we define 8-bit systolic array as $16B \times 16B$, and the corresponding 1-bit systolic array as $128B \times 128B$. Let the area of systolic array be $A$.

For 8-bit systolic array, there are a multiplier and a adder in each Process Element(PE). Under the design of TSMC 7nm, the area of the multiplier is about 23 $\mu m^2$, and the area of the adder is about 14 $\mu m^2$. Then, the total area of int-8 array can be approximately computed as: (Because there are slacks in chip placement, so the area sum here can only be a lower bound in a 2D chip floorplan. Same below)

$$A_8(pe) = (23 + 14) \times 16 \times 16 = 9472\mu m^2$$

Additionally, a partial sum memory ($Psum_{mem}$) is needed for each column of PE to store and compute partial sum cyclically, and get the sum finally. There are 16 $Psum_{mem}$ for $16B \times 16B$ array. Following the common setting of 8-bit arrays, the bit width of partial sum is 32, and the depth used to store the middle results of partial sum is 1024. Under the design of TSMC 7nm, the area is about 2300$\mu m^2$ for each $Psum_{mem}$ of 1024 $\times$ 32b. So, the total memory of $Psum_{mem}$ is:

$$A_8(Psum_{mem}) = 2300 \times 16 = 36800\mu m^2$$

The total memory of the 8-bit systolic array is:

$$A_8 = 9472 + 36800 = 46272\mu m^2$$

There are an XNOR gate for each PE, and a POPCOUNT unit for each column for sum in a binary systolic array. For simplicity, we define 8-bit systolic array as $16B \times 16B$, and the corresponding 1-bit systolic array as $128B \times 128B$. Let the area of systolic array be $A$.

For 8-bit systolic array, there are a multiplier and a adder in each Process Element(PE). Under the design of TSMC 7nm, the area of the multiplier is about 23 $\mu m^2$, and the area of the adder is about 14 $\mu m^2$. Then, the total area of int-8 array can be approximately computed as: (Because there are slacks in chip placement, so the area sum here can only be a lower bound in a 2D chip floorplan. Same below)

$$A_8(pe) = (23 + 14) \times 16 \times 16 = 9472\mu m^2$$

Additionally, a partial sum memory ($Psum_{mem}$) is needed for each column of PE to store and compute partial sum cyclically, and get the sum finally. There are 16 $Psum_{mem}$ for $16B \times 16B$ array. Following the common setting of 8-bit arrays, the bit width of partial sum is 32, and the depth used to store the middle results of partial sum is 1024. Under the design of TSMC 7nm, the area is about 2300$\mu m^2$ for each $Psum_{mem}$ of 1024 $\times$ 32b. So, the total memory of $Psum_{mem}$ is:

$$A_8(Psum_{mem}) = 2300 \times 16 = 36800\mu m^2$$

The total memory of the 8-bit systolic array is:

$$A_8 = 9472 + 36800 = 46272\mu m^2$$

There are an XNOR gate for each PE, and a POPCOUNT logit unit for each column for sum in a binary systolic array. Under the design of TSMC 7nm, the area of XNOR gate and POPCOUNT unit are 0.6 and 100 $\mu m^2$ respectively. So the total area of binary PE can be computed as:

$$A_{bin}(pe) = 0.6 \times 128 \times 128 + 100 \times 128 = 22631\mu m^2$$

Also, the bit width of partial sum is 16 in binary systolic array. and the area is about 1400$\mu m^2$ for each $Psum_{mem}$.
of $1024 \times 16b$. So, the total memory of $P_{sum_{mem}}$ in binary systolic array is:

$$A_{bnn}(P_{sum_{mem}}) = 1400 \times 128 = 179200 \mu m^2 \quad (27)$$

The area of array registers is small, and we ignore it. The total memory of the 8-bit systolic array is:

$$A_{bnn} = 22631 + 179200 = 201831 \mu m^2 \quad (28)$$

The ratios of $PEs$, $P_{sum_{mem}}$ and array area are 2.4, 4.87 and 4.36 respectively. Decreasing the bit width of partial sum is a good way to reduce the area of binary systolic arrays.

The main power consumption of network inference occurs in convolution layers, and the contribution to power consumption of $P_{sum_{mem}}$ is limited. The power consumption of convolution is proportional to the area of $PEs$. So, we can roughly estimate the power consumption of 1-bit systolic array is 2.5-4.36 times that of 8-bit, and much more close to 2.4 times.

**Appendix C. Convolution Cycle Formulae**

Follow the parameter definition in Sec. 3.5, we will derive the cycle counts for a convolution operation. For the computation of a convolution layer, the total cycles consist of loading instructions, MAC computation, and writing the results. When the output bit-depth is less or equal to the input bit-depth, the time for writing results can be absorbed via pipelines. Higher output bit-depth will lead to data blocking. The number of instructions required by a convolution layer, denoted by $I$, is proportional to the the size of aligned output feature map. The cost cycle of each cycle is equal to array size $S$. then,

$$I = \lceil \frac{N}{S} \rceil \lceil \frac{WH}{P} \rceil \quad (29)$$

which derives Eq. 7. When the input and output bit-depth are all 1-bit, the cycle count formula is described in Eq. 8. We define the number of cycles needed to write all the pixels in output feature map as $Round(R)$,

$$R = K\lceil \frac{CK}{S} \rceil \quad (30)$$

When the output bit-depth is larger than 1 in binary array, writing of the last round of feature map is congested, and the number of cycles is proportional to the output bit-depth $b$. So the cycles in this case is described in Eq. 9.