Uniting Control and Data Parallelism: Towards Scalable Memory-Driven Dynamic Graph Processing

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Abstract—Control parallelism and data parallelism is mostly reasoned and optimized as separate functions. Because of this, workloads that are irregular, fine-grain and dynamic such as dynamic graph processing become very hard to scale. An experimental research approach to computer architecture that synthesizes prior techniques of parallel computing along with new innovations is proposed in this paper. We establish the background and motivation of the research undertaking and provide a detailed description of the proposed computing system that is highly parallel non-von Neumann, memory-centric and memory-driven. We also present a message-driven (or even-driven) programming model called “diffusive computation” and provide insights into its properties using SSSP and Triangle Counting problems as examples.

Keywords—computer architecture, graph processing, processing in memory (PIM), non-von Neumann, high performance computing

I. INTRODUCTION

Within the context of computing systems and processing, the graph can have four embodiments as a manifest of the representation, processing, and computer system structure. These are: 1) Data Graph, 2) Program Graph, 3) Execution Graph, and 4) Architecture Graph. Detailed description is provided in Table I. For scalable graph processing, especially dynamic graph processing, these have been mostly treated and optimized as separate entities. We ask the questions: If we take an approach into unifying these, what will the requirements of such a system be? And what capabilities might it provide for dynamic fine-grain computations? This paper describes the background and a conceptual strategy establishing the foundational intellectual goals and exploratory approach of concepts, structures and methods conceived to aid in designing a proposed future class of, non-von Neumann, parallel computer systems called Continuum Computer Architecture [1] (CCA), which will enable scalable fine-grain computations associated with dynamic irregular graph processing for adaptive numeric algorithms (e.g., AMR) and AI problems (e.g., ML, NLP, and searching).

The domain of the work emphasizes the foundations of scalability for graphs that are physically distributed in a manner similar to conventional large-scale systems comprising rooms of rows of racks, each one of many nodes; but all within the same data and control name-space exporting a unified global abstraction for concurrent execution. This represents a potentially revolutionary departure from the more traditional hierarchical Communicating Sequential Processes (CSP) [2] model’s explicit partitioning, message-passing, and manual resource allocation. We believe that separate data and processes on ensembles of distinct standalone nodes must be retired and advanced to exporting a single system image. If successful, this research will deliver major progress in the fields of HPC, time-varying graph computation, and ML and AI. It will, further, provide guidelines for future research and development of a new generation of non-von Neumann parallel architectures to dramatically extend performance scale and reduce time to solution. AI and data analytics computational challenges at the end of Moore’s Law and within practical power limitations are projected to be enabled by establishing new machine-level data and control semantics and alternative architecture objective functions for optimization.

| Graph Type | Properties |
|------------|------------|
| Data graph | 1. Parallelism intrinsic in topology  
2. Static and dynamic  
3. Regular and irregular (neighbors having distinct degrees) |
| Program graph (BFS example) | 1. Dataflow graph.  
2. Programmer describing the algorithm.  
3. Compiler further changes/adapts it. |
| Execution graph (DAG) | 1. Variable with respect to each instance and dynamic due to runtime control.  
2. Time dependent. |
| Architecture graph (Dragonfly topology example) | 1. Network on chip.  
2. System area network topology. |
To that end, this paper highlights a strategy of five major interrelated concepts that in synergy will drive the proposed research while distinguishing it from prior, and sometimes stale art of conventional practices. The first and perhaps most profound among these is the semantic and operational unification of otherwise distributed architectural components for scalable graph processing systems. This is critical to fixing the major long-term barriers imposed by separation of physical processing nodes and differentiating control semantics of intra-node operation from that of global inter-node operation. The second strategic concept is on-the-fly discovery of lightweight parallelism intrinsic to the graph meta-data, principally its topology, that has little or no classical locality (e.g., temporal or spatial) but rather exhibits an alternative data relationship that might be referred to as “logical locality”. This is a creative innovation uniquely suited to highly scalable time-varying graph-based AI computations. The third strategic concept to be explored as part of this and driven in part by the first two concepts is the cross-cutting high-level abstraction of a parallel execution model required to tie together these other ideas within a unified framework. For comparison, over previous decades, have been commercial execution models of vector processing, SIMD, multiple threads, and CSP. An experimental parallel model transcends these with a more advanced control semantics that addresses the challenges imposed by the problem domain being pioneered. The fourth principal concept is again mutually in support of the others is that of message-driven computation which in early forms such as dataflow and RPC incorporated some limited attributes required but which for systems delivering unprecedented scalability and efficiency needs to reflect communication protocols for data movement, event synchronization, and action propagation for graphs. The final precept is “introspection”, the ability of a system to make on-the-fly decisions about its operation for enhanced performance. Introspection provides more information for guiding execution than merely that available by the programmer or compiler. Some application patterns can be launched with sufficient understanding that little or no benefit would be achieved through runtime control such as for dense linear algebra algorithms. But dynamic irregular graph problems exhibit unpredictable meta-data dependent access and control flow patterns demanding real-time supervision and resource management through advanced adaptive techniques. This last concept, while incorporated in some deployed systems using simplistic methods, are usually limited by processor utilization (throughput) goals. Modern enabling device technologies now are mostly impacted by memory bandwidth and latency sensitive methods. Future runtime introspective strategies need to be highly innovative in their handling of ultra-scale computing systems for AI and other application classes. The design of CCA will explore possible distributed control methods for such graph-based challenges to achieve measurable improvements for efficiency, scalability, time-to-solution, and energy consumption.

The remaining sections of this paper together expand on these interrelated strategies with extended discussions of the challenges being addressed, identified opportunities for dramatic improvements, and perceived innovations to achieve them. These sections are divided into: Section II: Conceptual Strategy, Section III: Prior Techniques Used For Synthesis, Section IV: Networking Infrastructure And Algorithms, Section V: Diffusive Programming Model, Section VI: Technical Approach and Section VI: Future work.

II. Conceptual Strategy

A. Strategy 1: Architectural Unification of Components that are in Synergy with the Scalable System

To have a unified architecture that is in synergy with the larger system design thereby allowing primitives, semantics, and the memory model to manifest at all system levels. It is a departure from contemporary node architectures that are designed for high degree of local uniform data-parallelism and a global non-uniform fractured (fragmented, partitioned) memory and namespace. To address this non-uniformity and attain scalable fine-grain parallelism, system design must not be limited to individual layers or sub-components but must go beyond and permeate throughout the larger system thereby creating equilibrium (a more homogenous system). This synergy must manifest in physically distributed but logically unified structures:

a) Global Namespace (memory model): Physical memory must be logically unified with the data contained in it. It is a shift from a segregated view of data that is contained logically within processes, which in turn reside within a physical memory space that is fractured into caches, NUMA domains and nodes. Instead, compute logic must be organized around memory thereby making a memory centric model. This physical memory layout must be homogenous and unified at the logical level by objects that not just represent data state but also the action state and the logical hierarchy as represented by the references between data objects (logical locality).

b) Communication model: The communication must be unified by creating a global and shared communication network that is built for large number of small messages thereby optimizing for latency. This will be a departure from staging data at various levels of hierarchies to optimize for bandwidth and enforcing different, and mostly static and synchronous, control flow mechanism. To attain high degrees of parallelism and hide latency the communication must be made transparent and captured though the asynchronous parallel programming semantics, discussed in Strategy 4.

c) Programming model: The programming model and syntactic interface needs to expose high degrees of parallelism that is intrinsic to the graph data-structure by exploiting the underlying parallelism offered by the hardware. Instead of hybrid forms of parallelism (e.g., MPI+OpenMP or GPUs) that are patched together to achieve throughput for coarse-grain computations, the programming model would benefit from enabling dynamically spawning asynchronous parallel computations from within the data. This can be achieved through a decentralized, asynchronous, and event-driven paradigm where the computation diffuses throughout a graph data-structure dynamically.
B. Strategy 2: Parallelism

Graphs do not have well-structured spatial locality patterns and therefore techniques such as data-parallelism do not inherently scale well. For the most part data-parallelism techniques are very static and regular; meaning that data that is being operated upon must not only be spatially contiguous but cannot change once the computation starts. This is also coupled with the fact that graph operations are not highly compute intensive and therefore control (or task) parallelism techniques (under fork-join and BSP) incur large overheads of synchronization and irregularities of execution. Data and Control parallelism must be unified for scalable graph processing.

Control-parallelism could work on meta-data of the irregular structure and expose inherent parallelism. This can be achieved by placing data (the graph structure) near computing capabilities that have the ability to spawn more computations. Such a setup will allow computations to asynchronously originate from within the graph vertex and diffuse throughout the larger graph. It is a departure from conventional data-parallelism where a central (“mother”) computation stages the operations and then uses some form of distributed (yet synchronized) control-parallelism to take the processing through its various stages.

C. Strategy 3: Execution Model to Expose Efficient and Scalable Inherent Parallelism

Properties that are critical to permit open-ended scalability of systems are: 1) global parallelism, 2) ability to express and execute dynamic computations, 3) exposure of large amount of fine-grain parallelism and 4) hiding latency.

These properties are driving needs for applications like graph-based problems that have irregular memory access patterns, low floating-point intensity, and high degrees of inherent parallelism. Therefore, it is important to have an execution model that is at its core not sequential and allows for very large amounts and diversity of global parallelism. Contemporary computing architectures are based on von-Neumann sequential machines connected together thereby creating what is called the Communicating Sequential Processes (CSP) execution model. Such machines may have high degrees of local parallelism but are globally sequential.

D. Strategy 4: Message-driven and Asynchronous System Model

Graph processing workloads being latency sensitive, low floating-point intensive, irregular and dynamic cannot be meaningfully optimized for bandwidth by techniques of message passing or “moving data to work”. The system model must optimize for large number of small messages, thereby optimizing for latency rather than bandwidth. Rather than sending data to where computation is to take place, the computation should be migrated (or initiated) where data resides. Such a message-driven approach coupled with asynchrony will perform computing operations near the data and, if needed, will dynamically launch new operations that will propagate through the graph structure. Such a computation can be called a “diffusive computation” being decentralized, asynchronous, dynamic and adaptive, not order constrained, and highly parallel. At its core a diffusive computation derives its benefits from the principle of “logical locality”.

E. Strategy 5: Introspection and Adaptive Management

The various aspects and functions of runtime systems that exist separately and independently between the programming language, accelerators, and communication libraries such as MPI must be shared and unified. The runtime system must be capable of administrating a global address as well as namespace and provide efficient placement, execution and migration of data and control objects. A range of runtime system software has been deployed throughout the many decades of HPC. Not all runtime systems address the same challenges or objective functions. Some augment operating systems to provide workflow management for job stream for resource scheduling at the job stream level. Here, runtime system is distinguished from OS or job stream oversight to the narrow focus within individual parallel application computations. For a given parallel application to be performed on a distributed hardware system, this runtime determines resource management and task scheduling from a combination of compile time information about the application and from information about the machine state and the application progress through introspective methods and control strategies. Most runtime system software developed over the last decade of this type emphasized ALU/FPU throughput and utilization. Whereas at the current state of enabling semiconductor technologies: memory capacity, access bandwidth, and latency are the precious resources for which to be optimized. This is particularly true for memory-intensive graph applications and new classes of memory-centric non von Neumann parallel architectures. Therefore, a deep understanding of the interoperability of architecture, compiler, and structures with runtime systems through co-design must be undertaken. Runtime effectiveness is sensitive to the additive overheads their implementation imposes. For this reason, architecture support for future runtime system design is a related imperative.

III. PRIOR TECHNIQUES AND THEIR SYNTHESIS

In this section we briefly touch upon past contributions, techniques and ideas that we believe have the potential to be synthesized to enable future scalable fine-grain and dynamic computational models and architectures. Typically, contemporary computing systems are broadly governed conceived under sequential processes computing model, where instructions are issued one at a time. Although there have been local optimizations for extracting parallelism such as superscalar architecture, pipelines, out-of-order execution, and branch prediction coupled with the CSP model for scaling but nevertheless there is an inherent lack of global parallelism. Functional and concurrent models provide unbounded parallelism and can be synthesized. Specially the properties of lambda calculus [3], actors model [4][5] and cellular automata [6]. For example, carrying in lambda calculus has the properties of:

1. Allowing the computation to progress while waiting on some arguments to be available.
2. Allowing the runtime context of the computation to be stored and potentially be migrated to some other part of the larger physical computing machine.

The above two properties are of interest to problems that arise out of the irregular, fine-grain and dynamic nature of graph processing and can be used to 1) increase throughput of the system by evaluating computations and not waiting on some dependencies and 2) migrate computations to improve load balance of the system and also hide latency by migrating computation to where the data resides.

The properties of the *actors model* include being history-sensitive (unlike dataflow functional systems) and being able to gracefully deal with dynamic topology, rather than static, thereby making it reconfigurable and extensible. From a structural and functional point of view, cellular automaton provides neighborhood state transforms and it can inspire future class of Processing In Memory (PIM) architectures. This can be used to further evaluate the placement, capacities and capability, and interaction of compute and memory logic.

Furthermore, PIM architectures not only provide an answer to the von Neumann bottleneck but also together with capabilities such as execution migration, of active messages [7], parcels and thread percolation [8], can explore more fine-grain parallelism and hide latencies. These along with the Dataflow architectures properties of exposing fine-grain parallelism through the program control graph [9] can provide a way towards unifying data parallelism with control parallelism.

Other important past works include high-level language computer architecture (HLLCA) [10] such as the Lisp machines [11], Intel iAPX, and knowledge-based systems like the NETL architecture [12]-[14]. These provide native support for garbage collection and application representation, to name a few. Such prior work and ideas can be used to unite the application, compiler, OS, and the architecture for runtime introspection and on-the-fly optimization that is a unique demand for dynamic and irregular applications like graph processing.

### IV. NETWORKING INFRASTRUCTURE AND ALGORITHMS

Fine-grain computations impose different kind of challenges on the networking infrastructure in order to provide scalability. These include the ability to:

1. Allow small size messages to be sent with low latency as blocking over communication and sending in bulk to maximize bandwidth will reduce the amount of parallelism exposed.
2. Allow large number of small messages the network must be able to sufficiently deal with resources waiting for contention.
3. Route a large number of small messages in a smaller number of hops.

Networks and topologies such as the Data Vortex and Kautz topology provide try to address the three requirements stated above. Data Vortex provides a low latency and contention free network [15] that is important for implementing message-driven fine-grain architectures and the Kautz topology provides the properties of small diameter needed to route messages in small number of hops. The data graphs themselves have diameters and the idea is to provide the architecture graph the capability to physically traverse the diameter in as little hops as possible (comparing the logical data graph diameter).

### V. DIFFUSIVE PROGRAMMING MODEL

The programming model must be capable of exposing massive fine-grain parallelism contained in the graph structure, and also be able to adapt the execution to the changes in the graph structure. Decentralized and asynchronous message-driven programming models [16] have the right properties and must be further studied and developed.

Here we explore what we called the “*diffusive computing model*”, where an asynchronous active massage is send from a memory locality to another memory locality (target). This active message can mutate the state of the target locality and can further create new messages (work) at the destination thereby creating a ripple effect. Since the computation progresses asynchronously and at the same time can reactivates a previous node in the execution graph, the consequence of this is that there is no predetermined computational dependency graph [17] or a one that is determined at runtime [18]. In asynchronous graph processing, there is no dependency graph or the Directed Acyclic Graph (DAG) of the execution. This is primarily because of arbitrary structure of the input graph with arbitrary weights, whereby the execution (program) relies on some arbitrary invariant to advance. Code Listing 1 shows such a program the Single Source Shortest Path (SSSP). This makes it difficult to know the amount of work that will be performed at runtime, since the execution can potentially take any path to the solution(s). There is another implicit problem with such computations called the Termination Detection Problem, which does not manifest in formulations in Bulk Synchronous Parallel (BSP) counterparts.

```plaintext
Code Listing 1: Asynchronous Diffusive SSSP

```diffuse(vertex v, int distance):
    if v.distance >= distance:
        v.distance = distance
        for u in v.neighbors:
            diffuse(u, v.distance + u.weight)

SSSP(vertex src):
    src.distance = 0
    for u in src.neighbors:
        diffuse(u, u.weight)
```

### A. Diffusive Computation

The steps and requirements of a *diffusive computation* for asynchronous graph processing are further described in detail below:

1. Each Vertex (in the graph) becomes active by calling a vertex function.
2. When active, a vertex can make neighboring vertices active by sending a message, i.e. the diffusion.
3. On receiving the message, a vertex can check some predicate (condition) on itself from the message data.
and decide whether to activate itself. This is where
relaxation and scheduling comes.

4. This diffusion message is asynchronous with fire-and-
forget semantics, which implies no DAG because there
could be cycles in the graph.

5. At some point when there is no work to do the vertex
deaactivates.

6. The whole diffusion computation finishes when there
is no vertex active and there is no message in transit.
Termination detection must be employed.

B. HPX-5 implementation of Diffusive SSSP

We implement asynchronous Single Source Shortest Path
(SSSP) using HPX-5. Code Listing 2 shows pseudocode for
SSSP HPX-5 implementation. We extensively used HPX’s
actions to perform vertex computations. This meant that very
large number of small messages were generated on the network.
For the purposes of termination detection we used Dijkstra–
Scholten algorithm [19], which creates an implicit spanning tree.
As computation comes to an end the tree naturally unfolds
and becomes empty, signifying termination. It comes at a cost of
extra acknowledgment message for each diffusion message.

```cpp
HPX_ACTION(sssp_vertex_func);
sssp_vertex_func_handler (hpx_addr_t vertex,
   hpx_addr_t Graph,
   hpx_addr termination_and_LCO,
   int incoming_distance_from_root) {
   hpx_lco_sema_p(v->vertex_local_mutex);
   // some part of termination detection logic might
   go here
   if(vertex.my_distance >
      incoming_distance_from_root ){
      //update
      vertex.my_distance = incoming_distance_from_root;
      //diffuse
      for-all u in neighbors {
         int new_distance = u.weight+vertex.my_distance;
         hpx_call(u, sssp_vertex_func, Graph,
            termination_and_LCO, new_distance);
         // some part of termination detection logic
         // might go here
      }
      // some part of termination detection logic
      // might go here: i.e ack back to the sender
      hpx_lco_sema_v(vertex.vertex_local_mutex,
         HPX_NULL);
   }
}
```

Code Listing 2: Simplified HPX-5 implementation of Diffusive SSSP

C. Experimental Method and Data-set Details

We report the time to solution and the number of actions
(dynamic work) done. Here action is the active message
generated at runtime. In an ideal run SSSP should traverse
a single edge just once, therefore we divide it with the number of
edges of the graph and report Actions Normalized.

We ran our HPX-SSSP code on Indiana University’s
Bigred2 system, where each node is 32 cores. We tested against
five different shapes of graphs based on varying degree
distribution and clustering coefficient. These include Erdos-
Renyi, Small-World, Scale-Free, Powerlaw-Clustered and
Graph500 and their degree distribution and clustering coefficient is depicted in Table II.

| Graph Type       | Degree Distribution | Clustering Coefficient |
|------------------|---------------------|------------------------|
| Erdos-Renyi      | ![Erdos-Renyi](image) | ![Erdos-Renyi](image) |
| Small-World      | ![Small-World](image) | ![Small-World](image) |
| Scale-Free       | ![Scale-Free](image) | ![Scale-Free](image) |
| Powerlaw-Clustered| ![Powerlaw-Clustered](image) | ![Powerlaw-Clustered](image) |

D. Performance Measurement Results

These experiments are designed not to beat the world record
but to act as a guide in our exploration of the programming
model and specially extracting out key features that effect the
runtime behavior. Contemporary computing systems are not
designed to efficiently process large number of small messages
and fine-grain computations as described by HPX actions. This
clogs the networking infrastructure and therefore we had to
perform the experiments on smaller size input graphs.

Figures 1, 2, 3, 4 and 5 show the time to solution and the
number of actions invoked as we scale to larger core counts. In
general, as we increase HPX processes the time to solution
decreases. This comes not only from the added parallelism but
also the dynamic nature of the computation. As we increase
HPX processes we increased number of LIFO queues (each
HPX process has its own LIFO queue) this in turn creates some
randomness, which helps in better scheduling.
Figure 2: Performance results of Erdos-Renyi input

Figure 3: Performance results of Powerlaw-Clustered

Figure 4: Performance results of Scale-Free

Figure 5: Performance results Small-World input

E. Some Recommendations

From this experience we found three main areas of improvement for HPX-5 that could lead to better performance and programmer productivity. These include:

1. Orchestrating predicate logic so that HPX scheduler gets access to it and schedule actions intelligently.

2. Providing termination detection logic with in HPX so that it makes code expression easy thereby not only increasing programmer productivity but also potentially increasing performance.

3. Providing read-write access labels for memory regions will eliminate programmer’s needs for explicitly locking the HPX process/thread on vertex object. This will increase programmer productivity and also expose new scheduling opportunities for HPX.

To this end we propose `hpx_diffuse` call. This captures the basics of diffusing computation that include the vertex function, the predicate that helps in scheduling and the termination detector.

```c
hpx_diffuse(vertex_id, vertex_func, arg_1, arg_2, ..., arg_n, terminator, predicate);
```

Code Listing 3: Diffuse primitive

- `vertex_id` the memory location at which the vertex exists: we send the parcel there
- `vertex_func` the active message that contains the vertex program (the diffusing computation)
- `arg_1` to `arg_n` any arguments to the `vertex_func`
- `terminator` is the object that knows whether this diffusion is finished
- `predicate` the invariant if false returns from the `vertex_func` without generating new work

Code Listing 4 shows the use of `hpx_diffuse` and how our previous HPX-5 SSSP implementation in Code Listing 2, could look like.

```c
HPX+ACTION(sssp_vertex_func);
sssp_vertex_func_handler (hpx_addr_t vertex, hpx_term terminator, hpx_addr_t Graph, int incoming_distance_from_root){
    //update
    vertex.my_distance = incoming_distance_from_root;

    //diffuse
    for-all u in neighbors {  
        int new_distance = u.weight + vertex.my_distance;
        hpx_predicate predicate = new Predicate(hpx_there > new_distance);
        hpx_diffuse(u, sssp_vertex_func, terminator, predicate, Graph, new_distance);
    } // for-all ends
} // vertex function ends
```

Code Listing 4: Asynchronous SSSP using the proposed HPX-5 `hpx_diffuse`

VI. TECHNICAL APPROACH

To achieve unbounded parallelism using an organization of memory centric structures that scales dynamic graph processing, we propose that the Continuum Computer Architecture (CCA) must be organized as an interconnection of homogenous global active memory cells that are decentralized (no single clock). These memory cells are hereafter referred to as Compute Cells (CCs), and shown in Figure 6, are capable of 1) data storage, 2) data manipulation and 3) data transmission to adjacent CCs.

An individual CC has limited capacity of data storage and other resources. Therefore, an arrangement of CCs tessellated for tight coupling and interconnected will work together to...
provide logical unification, unbounded data storage capacity and parallelism. Such an interconnect will be a mesh network, in its simplest form, as a consequence of the shape of tessellation. These shapes can include simple equilateral triangles (Figure 6), rectangles, hexagonal shapes and other forms. The actual number of CCs, their capacity and capabilities, and the mesh arrangement is a design objective to optimize for. This will be dependent on technology and application behavior.

Each CC can communicate with their neighboring CCs via the interface for the inter-compute cell communication channel as shown in the Figure 6.

![Figure 6: Triangular Tessellation of CCs: Each triangle (blue or orange) is a CC with the orange CC showing the internal structure. Different colors are used only to distinguish each cell; all CCs are identical.](image)

The execution model used in these CCs is based on the ParalleX model [20]. Each CC executes instructions asynchronously that are incident upon it in the form of “operons”, which is an implementation of a parcel and can be used for moving work/data using inter-cellular communication. If an action is performed locally, a “compute complex” is created within the CC; however, for a remote action, a parcel/operon is generated which is sent via the network that may generate a compute complex at the destination. Operons enable distributed control flow and dynamic resource management, featuring a split-phase transaction-based execution model [21][22].

A compute complex in this architecture is analogous to a thread in a conventional machine and a ParalleX process to a conventional process but internally highly parallel. One or more CCs may have one or more ParalleX process and further a ParalleX process may create one or more compute complexes. CCA is event-driven and exposes much of its parallelism at runtime rather than purely compile-time fork-join concurrency. At the heart of exposing and exploiting parallelism at the execution level for graphs and other structures is the fact that certain instructions spawn new compute complexes and are capable of execution, independently. Moreover, a compute complex is an abstract task instantiation, while it is hosted by a one or more physical CCs capable of performing it. Thus, since the machine is event-driven, it could have multiple instructions spawning multiple compute complexes and those newly created compute complexes may further spawn new child compute complexes which leads to the diffusive style of computation mentioned in the previous sections.

CCA being specialized in graph processing requires certain primitives that reduces conventional software overheads when processing both static and dynamic graphs. At the very fundamental level, a typical graph problem contains seven primitive operations – vertex add, vertex delete, vertex touch, edge add, edge delete, edge touch, and peek (reading the data of an adjacent vertex). These primitives when implemented directly in hardware (instruction set architecture) reduces overhead. Here, a peek operation does not have to be a primitive, however, having the ability of a vertex to see the data present in the neighboring vertex with hardware support reduces overhead dramatically especially in greedy algorithms like SSSP where the decision to touch a neighboring vertex depends on its value. Overheads are an important limiting factor in exposing and exploiting parallelism in general purpose computing and especially for graphs processing.

Global namespace as discussed in the previous section, plays a significant part in the execution model for this class of architecture. Computations involve variables; variables are first-class objects; they can be passed around from one compute-cell to another and can freely move across the system. Global namespace helps to identify these objects as they are not tied to a particular location as opposed to the conventional page-style memory addressing methodology where each variable is essentially tied to its memory location.

Global namespace is important as it is not only needed by the user defined variables, but also system created variables, messages, compute complexes, and all the objects that are created by both the system and the user. A name uniquely identifies the object and at the same time can locate an object across the system. Thus, the need of a “name server” arises. It will potentially be such an extensive tool that implementing it in software would make the name generation process very expensive and impractical. A hardware name server would provide a capability for the system that would be used to expose massive parallelism. A few characteristics are expected from a name given to an object by the nameserver. The name should uniquely identify the object across the system. It should also have the location embedded in it so that any compute-cell if needed could be able to derive its location. Since the objects are free to move across the system, any move should be able to change the translation of the fixed name of the object to the that of its new location.

Concurrent instruction issue is an important mechanism in a massively parallel architecture. Each CC or a locality (group of contiguous CC) can have multiple ParalleX processes. Each ParalleX process can have multiple compute complexes (threads). These mechanisms enable the system to issue multiple concurrent instructions. This mechanism since handled by hardware helps to reduce software overheads especially when issuing instructions like touching the outgoing edges of a vertex where all the outgoing edges can be traversed concurrently from a vertex. Here it is also important to make a distinction between concurrency and simultaneity. The concurrent instructions do not necessarily happen at the same time, they may or may not be time multiplexed and performed in any order.
Each CC executes an instruction based on an event either local or from a remote site. Typically, it would be an incident operon. An operon is a message that contains a specification of an action to be executed directed towards a specific first-class object in its resident CC. An operon, in addition to the action message, also contains a “continuation” field consisting of an action to be executed after completion of the intended instruction. Since all the fonts are identical in structure, and all the fonts work in a message-driven way; parsing an incoming Operon will be a frequent action executed by every font. The structure of an operon may evolve over the course of this research, but a skeleton of an operon would consist of an operon id, operon action specification, a continuation, and zero or more data values as operands. The operon id would be a sequence number as the messages could be sent or received out-of-order but they will be executed only when their precedent constraints are satisfied. The operon code may be either an explicit opcode or a “method” identifier that is an encoded form of an “action”. The continuation is an action to be performed after the action in the operon code has been completed. Actions can be of different types – (1) fetch, (2) read/write – context, data and metadata, (3) create/terminate ParalleX processes, (4) create/terminate compute complexes, (5) arithmetic operations, (6) graph operations/primitives, (7) move objects in physical space.

Managing parallelism in CCA is done asynchronously via the “Local Control Objects” (LCO). LCOs are abstract constructs that have two major sub-constructs viz. dataflow and futures and their variations. More simple conventional synchronization semantics are also supported for continuity with classical methods. For example, a mutex helps in providing mutual exclusion to a shared data structure in a distributed system to avoid race conditions. Unlike a mutex, which is a locking mechanism, a semaphore provides synchronization with the help of an interrupt- (or polling) based approach. It tells other processes that a particular process is done and is free to be used by others. It can be viewed as a generalized mutex. Futures, one of the most important synchronization mechanisms in the context of asynchronous distributed architecture is the primary area of focus for this research. Futures not only help manage parallelism but also help with managing asynchrony.

Futures is a construct used for synchronization between concurrent execution streams. It can be thought of as a transparent placeholder for a value. Once the value becomes available, the placeholder vanishes. This lets all the other operations continue and blocks only the operations that require the future’s value. For instance, if a future function is called with an argument X, in the language Racket’s notation, (future X), the future’s value. For instance, if a future function is called with an argument X, in the language Racket’s notation, (future X), where X is typically an expression, it immediately returns a future-variable (transparent placeholder or a proxy) for the value of the expression X. This future variable is also called an IOU which comes from “I owe you”, where X is a promise that will be eventually evaluated as it is owed by the function. At this point, the future variable or the IOU is said to be in an undetermined state. Once X is evaluated, the future variable gets the evaluated value, and its state gets updated to a “determined” state. A major advantage for overhead and starvation is that this still to be determined variable value can be manipulated in this indeterminate state within the evolving meta-data structure as long as its actual value is not directly required for the operations. Futures is a powerful construct to expose and exploit parallelism while dynamically adapting to asynchrony of execution and latency. Unlike other synchronization constructs like semaphores, it not only manages parallelism but is advanced to also manage the asynchrony. The conventional implementations of futures have been done entirely through software. This limits the use of futures and imposes high software overheads on the system. Every future instruction disassembles to multiple assembly instruction spanning multiple clock cycles, thus, limiting the use of futures construct to coarse granularity. If the futures can be implemented in hardware and has its own primitive operations, like creating the futures or changing the future state to determined, i.e., once the value of IOU is calculated, it would take only a couple of clock cycles for managing parallelism. This would significantly reduce the overheads in software implementations of futures and would lead to more effective use of futures.

A. Example Application Analysis on CCA (Triangle Counting)

The objective of triangle counting is to calculate the total number of triangles in a graph [23]. For instance, the total triangles in the graph (Figure 7) would be $3 - (1,2,6), (1,5,6), \text{and } (4,5,6)$.

![Figure 7: An undirected graph](image)

1) Parallel Algorithm

This algorithm assumes infinite computing resources. Every computing unit works with each wedge pair in parallel. It takes one hop to identify the wedge pair; in this case, it is $(v, v_x)$ and $(v, v_y)$. The 2nd hop is for checking if there exists an edge $E_{xy}$ between the vertices $v_x$ and $v_y$. Since the entire graph can do the above two steps in parallel and asynchronously, unlike bulk synchronous parallel execution model, the reduction operation which is counting the triangles does not have to wait for the above two steps. Most of the aggregation will overlap with computation. However, for the sake of speculating an upper bound, we assume that none of the reduction operation will overlap with counting the individual triangles. Thus,

\[
\text{Sequential Time} = (2 \text{ hops} \times \text{number of wedges}) + (1 \text{ hop} \times \text{number of triangles})
\] (1)
Parallel Time = [2 hops + (1 hop × number of triangles)]

Speedup = Sequential time ÷ Parallel Time

2) Triangle Counting on CCA

Each compute-cell (CC) stores its state and can communicate as well as observe the state of the neighboring compute-cells. Given enough resources, each CC needs 1 hop to identify the wedge pair simultaneously. The second hop involves finding the edge connecting the wedge. In the average-case scenario, since all the compute cells are asynchronous, unlike BSP, which has a limitation of global barriers, they start aggregation of counts as soon as they are done identifying if their respective wedge is a triangle. This computation overlap helps exploit the additional parallelism. However, at worst, if all the compute-cells start the aggregation step at the same time, they still exploit enough parallelism due to the sheer number of compute cells as shown in the table with almost a gain of 10x.

3) Preliminary Results

Table III illustrates early analytical and speculative analysis with an unoptimized parallel algorithm for the proposed memory-centric and event-driven computer on three different datasets viz. Twitter, WDC 2012, and Graph500. The number of triangles, wedges, and vertices are taken from [24]. Despite being an unoptimized parallel algorithm, we see a potential of gain in the order of 10. Figure 8, 9, and 10 compares the execution time in hops for sequential and parallel algorithms for these datasets.

| Dataset | Vertices | Triangles | Wedges | Seq Time | Parallel Time | Speedup |
|---------|----------|-----------|--------|----------|---------------|---------|
| Twitter | 4.16E+7  | 3.48E+10  | 1.478E+11 | 3.3E+11  | 3.4E+10       | 9.4     |
| WDC 2012| 3.56E+9  | 9.65E+12  | 1.226E+13 | 3.4E+13  | 9.6E+12       | 3.5     |
| G500    | 1.71E+10 | 5.05E+13  | 2.46E+14  | 5.4E+14  | 5.0E+13       | 10.7    |

Figure 8: Graph500 Dataset Triangle Counting Time in Hops

Figure 9: WDC 2012 Dataset Triangle Counting Time in Hops

Figure 10: Twitter Dataset Triangle Counting Time in Hops

VII. CONCLUSION AND FUTURE WORK

In this paper, we presented our work on an approach towards an experimental computer architecture called the Continuum Computer Architecture (CCA) that is non-von Neumann and message-driven for scalable dynamic graph processing. The central idea of CCA is to unite control and data parallelism using elements of PIM architectures and highly concurrent execution models like cellular automata coupled with message-driven computations and programming model. In the future this work will be extended and further validated by constructing a simulator of CCA using the Structural Simulation Toolkit (SST) [25] that will allow evaluation of the placement, capacities and capability, and interaction of compute and memory logic for applications ranging from graph benchmarks of traversal like BFS, SSSP and Triangle Counting to knowledge-base reasoning systems.

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