Design of universal logic gates using homo and hetero-junction double gate TFETs with pseudo-derived logic

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Abstract
This work explores homo- and heterojunction tunnel field-effect transistor (TFET)-based NAND and NOR logic circuits using 30 nm technology and compares their performance in terms of power consumption and propagation delay. By implementing homojunction TFET-based NAND and NOR logic circuits, it has been observed that NAND consumes less power than the NOR gate since current drawn by PTFET in the pull-up network of the NOR gate is higher. The delay of the homojunction TFET-based NOR logic gate is lower than that of the NAND gate due to its reduced internal capacitances. To meet the enhanced performance of both NAND and NOR logic circuits, shorted and independent double-gate heterojunction (GaSb-InAs) TFETs are designed and implemented. In order to reduce both power consumption and delay further, pseudo-derived logic is implemented in NAND and NOR logic circuits for the first time. Heterojunction TFET-based NAND with the pseudo-derived logic circuit shows a lower propagation delay of $10^3$ times and a reduction in power consumption by 0.75 times compared to the heterojunction NAND logic circuit. Heterojunction TFET-based NOR with pseudo-derived logic has the reduction in power consumption of $10^3$ times and lower propagation delay than the heterojunction NOR logic circuit.

1. Introduction

With the advancements in technology, scaling down of device dimensions is imminent to reduce power consumption and offer higher speeds of operation (Ratnesh et al., 2021)-(Dutta & Sarkar, 2019). The present metal-oxide-semiconductor field-effect transistor (MOSFET) technology becomes obsolete in lower scales of nanometre regime because of short channel effects (SCEs; Dutta et al., 2018)-(Talukdar et al., 2020). So, it is important to go for devices that can overcome SCEs and offer better performance in terms of power consumption and being capable of high-frequency operations. A tunnel field-effect transistor (TFET) is one such device famous for its steep subthreshold swing, lower threshold voltage and lower leakage current. Having a steep subthreshold swing (SS) proves to be useful in many low-power applications such as dynamic random-access memory (DRAM; Khatami & Banerjee, 2009). Also, the leakage current reduction leads to
the production of a higher \( \text{l}_{\text{ON}}/\text{l}_{\text{OFF}} \) ratio, which is of high significance in low power-integrated circuits. The band-band tunnelling (BTBT) mechanism in TFETs is one of the key factors responsible for the charge carriers to have high mobility and increased current density whilst crossing junction reducing chances of recombination, which usually occurs in MOSFET (Baraveli et al., 2014; Turkane & Kureshi, 2016; Villalon et al., 2014). The structure of TFET being like that of MOSFET can also make it easier for device fabrication to transition from MOSFET to TFET (Villalon et al., 2014). Although the transition is smoother in theory, still TFET technology has demerits such as low \( \text{l}_{\text{ON}} \) as the device depends on several factors like BTBT, effective mass of carriers, bandgap alignment dependance of the oxide thickness on the channel length and many factors (Anghel et al., 2011; Boucart & Mihai Ionescu, 2007; Duan et al., 2018; Khatami & Banerjee, 2009). However, such limitations can be removed with the current research with the usage of homojunction Si TFETs and usage of different materials and high-k dielectric oxides in heterojunction TFETs (Barboni et al., 2015; Dewan, 2020; Morris et al., 2014). Materials include binary and tertiary semiconductors, such as SiGe, InAs, GaSb and InGaAs, which can provide a higher rate of tunnelling by band bending at lower voltages. Although much research is being performed in realisation of TFETs, the simulations are still behind the experiments being performed. It is observed that not only the materials of the device but also the structural improvements are necessary for increasing the compatibility between simulation and experiments (Cem et al., 2017; Nirschl et al., 2004; Wei et al., 2017).

The basic structure of TFET is a p-i-n junction (p-type, intrinsic, n-type), in which the tunnelling of electrons in the intrinsic area (channel) is controlled by a gate terminal. As gate voltage is applied, BTBT occurs when the conduction band of the channel bends to the same level as the valence band of the p-region (Cheng et al., 2018)-(Boucart & Mihai Ionescu, 2007). Although the structure is like that of a MOSFET, the active transport regions of TFET need modelling in both electrostatics and carrier transport mechanisms. As mentioned as one of the SCEs, gate leakage current is an issue even in TFETs. The gate leakage disrupts the BTBT at the source-channel tunnelling junction, resulting in less control of the channel in single-gate TFETs demonstrated in previous studies (Garg & Saurabh, 2019)-(Sahoo and Dash, 2020; Wei et al., 2019). To address this issue and to provide better control of the channel, double-gate TFETs (DG TFETs) have been introduced (Salehi et al., 2013)-(Varghese et al., 2015; Zhang and Chan, 2016). To improve the rate of probability of tunnelling, a combinational dopant of gallium antimonide and indium arsenide (GaSb-InAs) is used (Kumar Asthana, 2015)-(Pown & Lakshmi, 2020)-(Sharma et al., 2014). The effective bandgap for tunnelling can be decreased even further by using this heterostructure with GaSb-InAs combination to give a non-overlapping bandgap (Lee et al., 2013; Li et al., 2017)-(Pown et al., 2020). One more convincing reason to select this combination is that the lattice constants are matched for the materials, which reduces chances of fault during fabrication stages of the device. Although there are analysis and comparison of different TFET technologies in the literature, required compact models at the device level and power optimisation techniques at circuit levels have not been together used for low-power applications. So, our aim in this work is to investigate the employment and efficiency of TFETs with the above-mentioned techniques and technologies into NAND and NOR gates, which are basic building blocks of any electronic digital circuit. With the continuous research in the nanoscale regime and TFET
technologies, limitations such as usage of high doping concentrations with placement of source and drain junctions came into existence. Since these junctions are susceptible to minor changes in electric potential, it is necessary to overcome this problem by removing the junctions with uniform doping across the TFET, leading to new configurations like Junctionless TFET (JLTFTET) and double-gate vertical TFETs (Ferhati et al., 2018)-(Bentrcia et al., 2020).

The key element of this work is to implement the NAND and NOR logic gates with lower power consumption and less propagation delay. In this article, Section 2 gives the device description and parameter space of the device. Section 3 provides the results and discussion where the implementation of NAND and NOR logic circuits using the homo- and heterojunction-based TFET is realised (Sentaurus Device User Guide, 2016). Finally, Section 4 provides the conclusion.

2. Device description and parameter space

All the device simulations are carried out using the TCAD simulator from Synopsys (Tripathy et al., 2020). Figure 1(a) shows the structure of homojunction-based Si TFET. The GaSb-InAs heterojunction TFET structure without and with doping/meshing is shown in Figure 1(b) and (c) respectively. Table 1 shows the parameter space for DG TFETs, which is used in the simulation. All simulations are performed at room temperature (300 K) with

![Figure 1. Simulated structure of DG TFET: (a) Si TFET, (b) GaSb-InAs TFET withou](image)

| Geometrical Parameters | Homojunction (Si) DG TFET | Heterojunction (GaSb-InAs) DG TFET |
|------------------------|---------------------------|-----------------------------------|
| Gate length (L_g)      | 30 nm                     | 30 nm                             |
| Channel thickness (T_ch) | 8 nm                     | 8 nm                              |
| Front and back gate oxide thickness (T_ox) | 1 nm                     | 1 nm                              |
| Source doping concentration | $1 \times 10^{20}$/cm$^3$  | $4 \times 10^{19}$/cm$^3$          |
| Drain doping concentration | $5 \times 10^{18}$/cm$^3$  | $2 \times 10^{17}$/cm$^3$          |
| Channel doping concentration | $1 \times 10^{17}$/cm$^3$  | $1 \times 10^{15}$/cm$^3$          |
various models included to account for transport and interaction mechanisms of carriers, all of which are preponderant to TFET structures. Doping dependence mobility, high and normal field effects on mobility and velocity saturation are used in the physics section of the simulator. Besides, the Fermi–Dirac statistics, Shockley-Read-Hall (SRH) recombination and the drive current method use the Hurkx model for tunnelling. Furthermore, the region interface of the source-channel junction has been considered as it remains the active region for the tunnelling of carriers. So, the tunnel current generated at this junction depends on tunnelling probability of the carriers and other parameters are explained from the Wentzel-Kramers-Brillouin (WKB) expression, which is given in Equation 1.

\[ T_{WKB} \approx \exp \left( \frac{4\lambda \sqrt{2m^*E_g^3}}{3qh(E_g + \delta)} \right) \]

where \( m^* \) is the effective carrier mass, \( E_g \) is the band gap, \( q \) is the electron charge, \( \lambda \) is the screening tunnelling length and describes the spatial extent of the transition region at the source-channel interface, \( \Delta \delta \) is the energy range over which the tunnelling can take place or the energetic difference between the conduction band in the source and the valence band in the channel and \( h \) is Planck's constant,

\[ \lambda = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}} \cdot \sqrt{t_{ox}t_{Si}} \]  

where \( t_{ox}, t_{Si} \) are the oxide and silicon-film thickness and dielectric constants, respectively.

The double-gate heterojunction TFET (DG-HTFET) used in this work operates in two modes, which are named shorted gate HTFET (SG-HTFET) and independent gate HTFET (IG-HTFET). In SG-HTFET, the two gates of the device are connected and driven by the same voltage. Although it improved \( I_{ON} \) of the device compared to homojunction TFET, there is a considerable increment in \( I_{OFF} \) as well. This reduced the overall \( I_{ON}/I_{OFF} \) ratio of the device. To reduce \( I_{OFF} \), instead of being simultaneously driven \( V_{g1} = V_{g2} = V_g \), two gates are driven independently \( V_{g1} \neq V_{g2} \).

The transfer characteristic of homo- and hetero-TFET devices is shown in Figure 2. In homojunction and SG-HTFET, single gate \( (V_g) \) of 1 V has been used to drive the drain current and is measured for a constant drain voltage of 1 V. In IG-HTFET, drain current is measured by keeping the constant voltage range of 1 V at \( V_{g2} \) and 1 V at drain, with the voltage \( V_{g1} \) varying from 0 to 1 V. From Figure 2, the transfer characteristic curve is almost identical for both homojunction and IG heterojunction TFETs for the same geometrical parameters. The \( I_{ON}/I_{OFF} \) ratio obtained for these devices is given in Table 2. The usage of IG-HTFET improved
the control over the channel, thus reducing $I_{OFF}$, which is evident from Table 2. The effect of interface traps, which degrade electrical behaviour of drain, has been considered using the two-stage negative bias temperature instability (NBTI) model in the TCAD physics section. Using the NBTI model, it is observed that the device threshold voltage is shifted and both $I_{OFF}$ and $I_{ON}$ are reduced. So, we can say that both cancel out each other in the case of power consumption. For example, the device with low threshold voltage with higher $I_{OFF}$ and $I_{ON}$ is the same as the device with high threshold voltage with lower $I_{OFF}$ and $I_{ON}$. The mentioned current values in Table 2 are after the introduction of interface traps (Abdi et al., 2011)- (Ghoggali & Djeffal, 2010).
The device model has been used to generate the circuit symbols using the Verilog-A models as discussed previously. Furthermore, the generated Verilog-A models are added into the library of devices in Cadence where they are used to construct NAND and NOR logic gates. To improve the accuracy of the conversion of the device into circuit level symbols, SPICE models will be considered in the future (Djeffal et al., 2007). The circuit symbol of homojunction NTFET and PTFET is shown in Figure 3(a), (b). The circuit symbol of SG heterojunction NTFET and PTFET is shown in Figure 4(a) and (b), respectively. The circuit symbol of IG heterojunction NTFET and PTFET is shown in Figure 4(c) and (d), respectively.

3. Results and discussion

In this section, the universal logic gates (NAND and NOR) are realised using both homo- and heterojunction-based TFETs. The power dissipation and propagation delay are extracted for both homo- and heterojunction TFETs, and a performance comparison is made. For average power consumption calculations, after construction of the circuit, the ADEL window is accessed to give stimulus to the circuit and transient analysis is chosen for analysis. Save all option is selected to save all pwr signals of the circuit. From the simulation waveform window, results browser is accessed to select the saved psf file for power. Option tran is selected from results browser, and the pwr signal is sent to the calculator to get the average of it.

For delay calculations, delay is the time required for a signal to rise 10% to 50% of the supply. From the simulation window, the calculator is accessed and delay is chosen in which threshold values of 0.08 V and 0.4 V are given as 10% and 50% of supply voltage 0.8 V and the obtained expression from the delay functional panel is evaluated in the calculator (Cadence Tutorial2: Schematic Entry & Digital Simulation, 0000). For the design of TFET, it is assumed that (i) PTFET has the same drain...
characteristics and but only inverted and (ii) the capacitance values of drain and source of both PTFET and NTFET are the same and as small as 0.2 ff. This makes their intrinsic gate delays the same and makes both equally strong to produce the same rise and fall times to avoid sizing of transistors. The SS of the simulated device is found to be 34 mV/decade for homojunction TFET and 56 mV/decade for heterojunction TFET, which explains the $I_{ON}/I_{OFF}$ ratio from Table 2. Also, since the barrier width in the heterojunction is lower than that in homojunction TFET, $I_{ON}$ and $I_{OFF}$ are high in heterojunction TFET, which explains the increase of SS from homojunction TFET to heterojunction TFET. However, the same devices when being used, heterojunction TFET gives better performance because of its double gate structure.

3.1. Homojunction TFET-based NAND and NOR logic circuits

This section provides the details of NAND and NOR realisation of homojunction Si-based TFET, and their corresponding timing diagrams are depicted.

A. Realisation of the NAND logic function

The realisation of the homojunction TFET-based NAND circuit, which uses 30 nm technology node, is shown in Figure 5(a). In the NAND logic circuit when both inputs are given as logic low, both PTFETs in the pull-up network gets turned on and in the pulldown network, both the NTFETs gets open circuited. So, the path is created from $V_{dd}$ to the output. When one of the inputs is low, one of the PTFET will get turned on and will pull the supply voltage to the output. Now, when both inputs are high, the pulldown network gets short-circuited and pull the output voltage to ground, and thereby, $V_{out}$ becomes logic low or zero. The timing diagram of homojunction TFET-based NAND is shown in Figure 5(b).

B. Realisation of the NOR logic function

The homojunction TFET-based NOR circuit is shown in Figure 6(a). When both inputs are logic high, PTFETs in the pull-up network are turned off and the NTFETs in the pulldown network get turned on. This results in the output getting pulled to logic zero. Now, when both the inputs are logic low, both PTFETs present in the pull-up network get turned on, thus resulting in the output getting logic high. When either of the input is logic high/one, the output is pulled down to logic zero/low, because one of the PTFETs present in the pull-up network gets open circuited. The timing diagram of homojunction TFET-based NOR is shown in Figure 6(b).

3.2. SG heterojunction TFET-based NAND and NOR logic circuits

This section provides the details of NAND and NOR realisation using SG heterojunction (GaSb-InAs)-based TFET, and its timing diagram is also plotted.
A. Realisation of the NAND logic function

The schematic of SG heterojunction TFET-based NAND is shown in Figure 7(a). The circuit consists of hetero-NTFET (HNTFET) in the pulldown network and hetero-PTFET (HPTFET) in the pullup network connected in series. When both input signals are given logic low, HPTFET gets turned on and forms a short-circuit path between supply $V_{dd}$ and output $V_{out}$. So the output signal gets logic high. When both inputs are logic high, HPTFET gets turned off and there is no path between supply voltage...
When either of the input signal is given logic low, that is either $V_{in1}$ or $V_{in2}$ is given logic low, the output signal goes logic high. The timing diagram is shown in Figure 7(b).
**B. Realisation of the NOR logic function**

The schematic of the SG heterojunction TFET-based NOR logic circuit is shown in Figure 8(a). Two HNTFETs are connected in parallel, and two inputs are given to each of them. HNTFET is connected in series to the parallel combination of HNTFETs to act as a resistor to limit the current into the circuit. When both inputs are given logic high, two HNTFETs get turned on and short the supply $V_{dd}$ to the ground, thereby producing logic low output. When both inputs are
given logic low, both HNTFETs get turned off and the supply $V_{dd}$ gets shorted to output, producing logic high output. When either of the input is high, one of the HNTFET gets turned on pulling down the output to logic zero. The timing diagram is shown in Figure 8(b).

3.3. IG Heterojunction TFET-based NAND and NOR logic circuits

In this section, the details of NAND and NOR realisation using IG heterojunction (GaSb-InAs) TFET are given along with their corresponding timing diagram.


Realisation of the NAND logic function

The schematic of IG heterojunction TFET-based NAND is shown in Figure 9(a). When one of the inputs of the gate is given as logic high, it establishes the channel and the other gate limits the leakage current by isolating the source and drain. In the operation of heterojunction NAND, the two gates of the PTFET are tied to each other and are given inputs $V_{in1}$ (input voltage 1) and $V_{in2}$ (input voltage 2) as shown in Figure 8(a). When both inputs are logic high, the output will be logic zero. Since the gates of the PTFET are connected to high potential, the device gets turned off, whilst the NTFET gets turned on forming a short circuit path between output and ground. When both the inputs are given logic low, the output will be logic high since the PTFET forms a short circuit path between supply $V_{dd}$ and output terminal $V_{out}$. The timing diagram is shown in Figure 9(b).

B. Realisation of the NOR logic function

The circuit diagram of the IG heterojunction TFET-based NOR gate is shown in Figure 10 (a). The HNTFET present between $V_{dd}$ and $V_{out}$ acts as a resistor. When both inputs are logic high, the HNTFET turns on and this leads output to logic low/zero. When both inputs are logic low, the HNTFET will turn off and create a short circuit path between $V_{out}$ and $V_{dd}$, which results in logic high output. When either of the inputs is high, the output will be logic low or logic low/zero as one of the HNTFET gets turned on and closes the path between the supply $V_{dd}$ and ground. The timing diagram of the IG heterojunction-based NOR logic function is shown in Figure 10(b).

3.4. IG Heterojunction TFET-based NAND and NOR logic circuits with Pseudo-derived logic

This section explores IG heterojunction TFET-based NAND and NOR logic circuits with Pseudo-derived logic. To reduce power consumption and delay, Pseudo-derived logic circuits are implemented for the first time. The inverter that uses a p-channel device in pull-up has its gate grounded. The n-channel transistor in the pull-down network is given the input signal. This usage of driving the n-channel transistor with the input in pull-down network is called Pseudo logic (Zhao et al., 2009). In CMOS technology, the Pseudo-NMOS logic is the provider of worst-case power consumption. But coming to the case of TFET technology, implementation of this Pseudo logic seems to be a promising logic in reducing the power consumption by making a change in its configuration. In this logic, the PMOS transistor is always turned on and it is in the linear region of operation. This means that as PMOS is always on, the resistance of drain-source would be very less and so the time constant RC is low, thus enhancing the speed of operation. The same has been applied to TFET-based NAND and NOR logic circuits. But this Pseudo logic has been modified in such a way that HPTFET is not permanently connected to the ground but connected to a pulsating signal, which controls the pull-down network. This makes HPTFET turned on only for the half cycle of the control signal.
A. Realisation of the NAND logic function

The schematic diagram of the NAND logic function with Pseudo-derived logic is shown in Figure 11(a). The HNTFETs in the pull-down network are connected in series, and a single HPTFET is connected to supply, which controls the NAND functionality. When both inputs are logic high, HNTFETs present in the pull-down network gets turned on, thus pulling the output to ground. When both inputs are logic low and the control signal is logic high, the path
between supply voltage $V_{dd}$ and output terminal $V_{out}$ gets closed and pulls $V_{out}$ to the level of $V_{dd}$. When either of the input is logic high or logic low, provided that the control signal is logic high, the output will be pulled down to the logic low value. In contrast to Pseudo logic, a control signal has been supplied to the PTFET in the pull-up network, which controls the functionality of the NAND logic gate. The timing diagram is shown in Figure 11(b).
The schematic diagram of the NOR logic function with Pseudo-derived logic is shown in Figure 12(a). The HNTFETs in the pull-down network are connected in parallel, and HPTFET is connected to the supply, which controls the NOR logic functionality. Whilst connecting the circuit with Pseudo-derived logic, the HPTFET has been given a pulse voltage (the pulse input given to the HPTFET in the pull-up network is considered as control signal ‘C’) such that it does not turn on during the whole operation of NOR logic. When the control signal is set logic low, HPTFET turns on and closes the circuit between supply $V_{dd}$ and ground. When both inputs are logic high, irrespective of the control signal (whether it is
logic low or logic high), both HNTFETs turn off and the output is pulled to ground. When both inputs are logic zero and the control signal is logic low, the output goes logic high. When either of the inputs is high, and the control signal is also high, the output gets grounded. The timing diagram is shown in Figure 12(b).

3.5. Performance Summary of Logic Gates

This section deals with the overall performance comparison of all the logic gates discussed so far. The performance metrics considered here are propagation delay and power consumption. The average power and the propagation delay are measured by performing

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**Figure 12.** (a) NOR realisation using IG hetero-junction TFET with Pseudo-derived logic. (b) Timing diagram of the IG heterojunction NOR gate with Pseudo-derived logic.
the transient analysis of logic gates, and the procedure to compute power and delay is explained in the Cadence manual (Power measurement with Cadence EDA, 0000). Table 3 gives the performance summary of both homo- and heterojunction-based NAND and NOR logic circuits.

Table 3. Performance summary of logic gates.

| Logic gates                                | Propagation Delay | Power Consumption |
|--------------------------------------------|-------------------|-------------------|
| NAND (homojunction TFET)                   | 25.23 ns          | 79.46 pW          |
| NAND (SG-HTFET)                            | 17.91 ps          | 1.04 pW           |
| NAND (IG-HTFET)                            | 43.53 ps          | 38.02 pW          |
| NAND with Pseudo-derived logic             | 95.51 ps          | 28.92 pW          |
| NOR (homojunction TFET)                    | 132.71 ps         | 3.01 nW           |
| NOR (SG-HTFET)                             | 57.42 ns          | 39.17 μW          |
| NOR (IG-HTFET)                             | 276.19 ps         | 79.63 nW          |
| NOR with Pseudo-derived logic              | 13.06 ps          | 65.31 pW          |

Figure 13. (a) Power consumption of logic gates. (b) Propagation delay of logic gates.
From the results shown in Table 3, the power consumption has been increased from the pW to µW range for SG-HTFET compared to homojunction TFET-based NAND gates. Similarly, for the NOR logic gate, power has been increased from the nW to µW range. This is due to the reduced $I_{on}/I_{off}$ of SG-HTFET, which is evident from Table 2. To improve the performance of these universal gates, IG heterojunction-based gates are implemented. Although the $I_{on}/I_{off}$ ratio of IG-HTFET is less compared to homojunction TFET, power consumption has been reduced considerably from µW to pW in IG-HTFET due to its reduced complexity with only 2 transistors for the NAND gate and 3 transistors for the NOR gate. Since the propagation delay of a transistor is inversely proportional to the total drain current, IG-HTFET shows lesser delay compared to both homojunction and SG-HTFET devices, which can be seen from Tables 2 and 3. With the application of pseudo-derived logic to IG heterojunction TFET-based NAND and NOR logic gates, delay has been reduced further.

In the implementation of homojunction TFET-based NAND and NOR circuits, NAND shows less power consumption than NOR since NAND consumes power only when both inputs are logic high. In the NOR circuit, except when both inputs are high, all other states consume power. In the implementation of SG heterojunction TFET, there is less delay with the increased power consumption. This is because of the substrate being absent in double-gate HTFET, which ultimately increases the power consumption.

With the implementation of IG heterojunction TFET, the two different biases applied to the gates offer better control of the channel by controlling the rate of probability of tunnelling and substrate leakage current. Due to bandgap energy being lower in GaSb (0.67 eV), it provides higher ON current at lower voltages. Due to the band offset being good in the GaSb-InAs heterojunction, it leads to faster transition and lower path delay in the circuit (Liu et al., 2012)-(Schmidt et al., 2014). Thus, IG HTFET gives less power consumption than SG HTFET.

Furthermore, the performance of HTFET-based NAND and NOR gates is improved by with Pseudo-derived logic. In contrast to the Pseudo logic, the HPTFET present in the pull-up network is not permanently grounded, instead a control signal was given such that the PTFET is not turned on during the whole time of operation of the circuit. This gives an improved efficiency of consuming power. When the control signal is given logic low, the supply $V_{dd}$ is connected directly connected to $V_{out}$, which produces logic high output.

Figure 13(a) and (b) shows the power consumption and propagation delay of homo- and hetero-junction TFET-based logic gates considered in this study. All power consumption values (in pW) and delay (in ps) values are given on the log scale.

4. Conclusion
In this study, homo- and heterojunction TFET-based universal gates are designed and their performance in terms of power consumption and propagation delay is explored. Homojunction TFET-based NAND and NOR logic circuits offer higher delay/lower power consumption and lower delay/high power consumption, respectively. This is because of the high band gap of homojunction TFET, which reduces probability of tunnelling. By using SG HTFET, the NAND logic function produced a considerable reduction in propagation delay, but increased power consumption compared to the homojunction-based NAND logic function. Using IG-HTFET, both power consumption and delay are reduced because of the two gates controlling the channel current independently. To reduce delay and power consumption
further, Pseudo-derived logic has been implemented for IG HTFET-based NAND and NOR logic circuits. In this Pseudo-derived logic circuit, HPTFET gets turned only for the half cycle of the input, reducing the power consumption. The heterojunction TFET-based NAND and NOR logic functions have retained their functionality till 0.28 Volts, which proves better control of the channel even at smaller voltages. Hence, it can be concluded that Pseudo-derived logic gates excel in performance in both delay and power consumption, and thus, it can be a potential candidate for ultra-low power applications.

Disclosure statement
No potential conflict of interest was reported by the author(s).

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