Flat-Combining-Based Persistent Data Structures for Non-Volatile Memory

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Abstract. Flat combining (FC) is a synchronization paradigm in which a single thread, holding a global lock, collects requests by multiple threads for accessing a concurrent data structure and applies their combined requests to it. Although FC is sequential, it significantly reduces synchronization overheads and cache invalidations and thus often provides better performance than that of lock-free implementations.

The recent emergence of non-volatile memory (NVM) technologies increases the interest in the development of persistent concurrent objects. These are objects that are able to recover from system failures and ensure consistency by retaining their state in NVM and fixing it, if required, upon recovery. Of particular interest are detectable objects that, in addition to ensuring consistency, allow recovery code to infer if a failed operation took effect before the crash and, if it did, obtain its response.

In this work, we present the first FC-based persistent object implementations. Specifically, we introduce a detectable FC-based implementation of a concurrent LIFO stack, a concurrent FIFO queue, and a double-ended queue. Our empirical evaluation establishes that due to flat combining, the novel implementations require a much smaller number of costly persistence instructions than competing algorithms and are therefore able to significantly outperform them.

1 Introduction

Byte-addressable non-volatile main memory (NVM) combines the performance benefits of conventional (volatile) DRAM-based main memory with the durability of secondary storage. The recent availability of NVM-based systems increased the interest in the development of persistent concurrent objects. These are objects that are able to recover from system failures (crashes) and ensure consistency by retaining their state in NVM and fixing it, if required, upon recovery. Of particular interest are detectable objects that, in addition to ensuring consistency, allow recovery code to infer if a failed operation took effect before the crash and, if it did, obtain its response.
The correctness condition for persistent objects that we use in this work is durable linearizability \cite{18}, which, simply stated, requires that linearizability \cite{16} be maintained in spite of crash-failures. Devising durably linearizable recoverable objects in general, and detectable ones in particular, is challenging. Although data stored in main memory will not be lost upon a system crash, with the currently available technology, caches and registers are volatile and their content is lost if the system fails before it is persisted (that is, written to NVM). Since operations on concurrent objects are, in general, not atomic, a system crash may occur in the midst of operations applied to the object and leave it in an inconsistent state that must be fixed upon recovery. Ensuring correctness is made even more complicated due to the fact that cache lines are not necessarily evicted in the order in which they were written by the program. Consequently, program stores may be persisted out of order. Persistence order can be guaranteed by explicitly invoking persistence instructions such as flushes and fences. However, these instructions are expensive and should be used as sparingly as possible.

A key approach for devising persistent concurrent objects is by using memory transactions. Persistent transactional memories (PTMs) (e.g. \cite{3,10,20,22,23,27,28}) are general-purpose implementations that support persistent memory transactions. A PTM implementation supports the execution of concurrent transactions by multiple threads while ensuring that the effect of each transaction is either persisted as a whole or has no effect. Although PTMs make the construction of persistent objects easier for programmers, they often incur significant performance overheads, largely because they have to maintain metadata for ensuring transactional semantics. Moreover, as we show in this work, they also incur extra persistence instructions in comparison with an optimized implementation of a specific concurrent object that is able to leverage object semantics. Another shortcoming of PTMs is that, to the best of our knowledge, none of them provides detectability. Unfortunately, for many key concurrent objects, optimized non-transactional detectable implementations still do not exist.

Flat combining (FC) \cite{14} is a coarse-grained lock-based synchronization technique, in which threads delegate their work to a single combiner thread, which combines operations by multiple threads in a manner that exploits the semantics of the implemented concurrent object and then jointly applies them. For example, several add operations on a counter can be replaced with a single add operation with the sum of their arguments. Informally, FC proceeds in combining phases, and in each phase, threads contend on a single global lock; the winner becomes the combiner for that phase, while the rest of the threads wait for their operation to be completed by the combiner. Despite being sequential, the reduced synchronization overhead and cache invalidations of FC more than offset the higher parallelism of alternative implementations. \cite{14} presented (non-persistent) FC-based implementations of stacks, queues and priority queues that outperform prior implementations of these objects that are either lock-based \cite{25,29} or nonblocking \cite{13,17,21,26}.

This work presents detectable flat combining (DFC), an approach for persistent objects that is based on FC, and applies it to derive detectable stacks,
queues and double-ended queues. We experimented in our DFC objects with the concept of elimination. In the case of a stack object, pairs of push and pop are combined by “eliminating” them: each pop operation in the pair return the item that is the argument of the push operation in the pair. Surplus push or pop operations are combined by atomically extending or truncating a linked-list stack representation. As shown by our experimental evaluation, when the combiner thread collects a large number of pairs that are suitable for elimination, performance is significantly improved.

Contributions.

– We present DFC stack, a flat-combining implementation of a persistent and detectable stack; it is the first non-transactional detectable persistent stack. To the best of our knowledge, DFC is the also the first flat-combining-based implementation of any persistent object.

– We experimentally evaluate the DFC stack on an Intel machine with NVM. We compare its performance with that of data structures implemented on top of the Romulus [10], OneFile [23] and Intel’s PMDK PTM [3]. The DFC stack outperforms all these implementations by a wide margin. Specifically, DFC leverages the stack semantics to significantly reduce the number of persistence instructions in comparison with the other algorithms.

– The key algorithmic ideas we use for making the FC technique persistent are generic. We apply DFC to derive detectable persistent queues and double-ended queues (deques). Experimental evaluation shows that DFC-based queues and deques provide good performance. The pseudo-code and evaluation of our DFC-based queue and deque are presented in the appendix.

2 System Model

We assume the shared cache model [18], in which the shared memory holds both non-volatile shared variables (residing in NVM) and volatile shared variables (residing in DRAM). The contents of the cache and processor registers are volatile: primitive operations are applied to volatile memory, since they are applied to variables residing in registers or in the cache. Writes to non-volatile variables are persisted to NVM using explicit flush instructions, or when a cache line is evicted. Under explicit epoch persistency [18], a write-back to persistent storage is triggered by a persistent write-back (pub) instruction. The thread may continue its execution after pub is issued. The order of pub instructions is not necessarily preserved. When ordering is required, a pfence instruction orders preceding pub instructions before all subsequent pub instructions. A psync instruction waits until all previous pub instructions complete the write back. For each memory location, persistent write-backs preserve program order.

We assume the Total Store Order (TSO) model, supported by the x86 and SPARC architectures, where writes become visible in program order. In addition, since in current architectures supporting NVM a pfence acts as both pfence and psync, our pseudocode uses pfence to indicate the execution of both.
At any point during the execution of an operation, a system-wide crash-failure (or simply a crash) may occur, which resets all volatile variables to their initial values, but preserves the values stored in the NVM. An operation’s response is lost if a crash occurs before it was persisted to a non-volatile variable.

Following a crash, the system resurrects all threads and lets them execute the Recover procedure, in order to recover the data-structure by fixing inconsistencies in it, if any. The system may crash again before resurrecting all threads. Thus, Recover may be invoked multiple times before it completes, because the system may undergo multiple crashes in the course of executing it.

DFC ensures durable linearizability [18], that is, linearizability is maintained despite crashes: once the system recovers after a crash-failure, the state of the data structure reflects a history containing all operations that completed before the crash and may also contain some operations that have not completed before the crash. This captures the idea that an operation must be linearized only once its effect is persisted to NVM. An implementation is detectable [6] if Recover also finishes p’s crashed operation (if there is one) and returns its response.

DFC provides starvation-freedom: If a thread invokes an operation Op, all active threads continue taking steps and the system does not crash, then eventually Op completes, either directly or by the completion of Recover.

3 The DFC Stack

In this section, we describe the DFC stack algorithm. As done in FC-based algorithms, each process announces its operation (in the DFC stack algorithm, this is either a Push or a Pop), by writing its operation code and arguments to its entry in an announcement array. Then, each process attempts to capture a global lock that protects a sequential data structure and become a combiner. Processes that fail to capture the lock (non-combiner processes) wait for the combiner to apply their operations, whereas the combiner proceeds to traverse the announcement array, collect announced operations, apply them to the data structure, and write operation responses to their corresponding announcement array entries. In our implementation, the stack is represented by a linked list.

In a plain-vanilla FC-based stack implementation, the combiner applies Push and Pop operations by simply adding or removing a list item from/to the head of the list. In our implementation, the combiner also employs (whenever possible) elimination [15], to pair concurrent Push and Pop operations. The combiner applies each such operations pair by setting the response of the Pop operation to be the input of the Push operation without having to access the linked list. The combiner needs to modify the linked list only if the numbers of Push and Pop operations that it collected differ. If there is a surplus of non paired-up Push operations, the combiner appends nodes containing their arguments to the head of the list; if there is a surplus of Pop operations, then the respective number of nodes is removed from the list (if they exist) and their values are written to the response fields of the respective announcement array; if the surplus of Pop
type Node {
    Integer param
    Node* next
}

Non-Volatile shared variables:
- Integer cEpoch, initially 0
- Node* top[2], initially both ⊥
- TAnnounce tAnn[N], all initially 0

Volatile shared variables:
- CAS variable cLock, initially 0
- CAS variable rLock, initially 0
- Integer pushList[N], popList[N], vColl[N], all initially 0

Fig. 1: DFC Stack: types and initialization

operations is larger than the length of the list, some POP operations return an empty response value. We now describe the algorithm in more detail.

Data types, shared variables and initialization values are presented in Figure 1. Variable cEpoch is a global epoch counter that counts the number of combining phases that have been performed so far (multiplied by 2, for reasons we explain soon). top is a two-entry array that stores two pointers, such that after each combining phase, in an alternating manner, one of them points to the head of the stack. The current epoch number, stored in cEpoch, is used in order to determine which of the top pointers is the up-to-date head of the linked list representing the stack. tAnn is the announcement array. It contains N entries, each of which stores an ann array consisting of two announcement structures. Each announcement structure has fields for storing the operation announcement, response, and a 2-bit variable valid, whose least-significant-bit (LSB) indicates which of the announcement structures is the active one, and whose most-significant-bit (MSB) is set only once the announcement is ready for the combiner to collect. For simplicity of presentation, we use LSB(valid) and MSB(valid) to access and set the respective bit of valid. cLock is the combiner lock. The rest of the variables presented in Figure 1 are described when they are first mentioned in the pseudocode description that follows.

Algorithm 1 (left) presents the pseudocode of the OP procedure, which implements both Push and Pop operations. At the beginning of each operation (lines 2-3), a thread t first creates a local copy opEpoch of the current cEpoch and checks if it is even. If it is not, t increments opEpoch to the next even number. Then, in lines 4-8, t announces its operation in the next available announcement structure (the one not currently pointed at by valid). It does so by writing the operation type and argument (the latter only in case of a PUSH), resetting the response value in val to a special value ⊥, and updating the structure’s epoch field. The following pwb and pfence instructions ensure that the values in the announcement structure are persisted before the valid field is modified to point to the updated announcement structure (line 10). This ensures that in case of a crash, valid does not point to the wrong announcement structure. Then, pwb and pfence instructions are executed again to ensure that valid is persisted, so that in case of a crash the recovery combiner will handle the correct announcement structure. After valid is persisted, t sets the MSB of valid in line 12 notifying the combiner that its announcement is ready to be combined.
The update of valid is done in this manner in order to deal with the following bad scenario. Suppose a non-combiner thread completes announcing its new operation and changes valid to point to it, but is yet to persist it. Now, a combiner collects the operation and applies it. In case of a crash, valid may point at the old announcement structure (since it was not persisted). Thus, the thread will not be able to tell whether its current operation was completed or not. An alternative solution to this issue is to have the combiner itself persist the valid field of any operation it collects. However, this would degrade the performance, since the combiner delays all other threads, and we opted not to do so. Note also that persistence instructions performed by the announcement code may be executed by different threads in parallel, so a fence instruction by one thread does not block the progress of other threads. In contrast, persistence instructions performed by the combiner delay all waiting non-combiner threads. As shown by our evaluation results, the adverse effect of these concurrent persistence instructions on the performance of DFC is smaller than that of the combiner’s persistence instructions.

After announcing its operation, a thread attempts to become the combiner by capturing the combiner lock cLock in the TakeLock procedure (line 13). We first describe the combiner code, and discuss the code performed by non-combiners later. The combiner returns from TakeLock without waiting and proceeds to combine all announced operations in line 17 by calling the Combine procedure (Algorithm 2). Only a single thread (the current combiner) may execute this procedure at any given time. Combine first calls Reduce in line
Algorithm 2 DFC Stack. Combine and Reduce procedures.

51: procedure Combine( )
52:     tIndex := -1
53:     while tIndex > 0 do
54:         cId := pushList[tIndex]
55:         vOp := vColl[cId]
56:         param := tAnn[cId].ann[vOp].param
57:         nNode := Allocate Node (param, head)
58:         tAnn[cId].ann[vOp].val := ACK
59:         pushList[i]
60:     end
61:     return
62: procedure Reduce( )
63:     for i = 1 to N do
64:         vOp := tAnn[i].valid
65:         if vOp) = 1 then
66:             tPush, tPop := -1
67:             for i = 1 to N do
68:                 vOp := vColl[i]
69:                 if head = 1 then
70:                     tAnn[cId].ann[vOp].val := EMPTY
71:                     tempHead := head
72:                     head := head.next
73:                     Deallocate Node(tempHead)
74:                 else
75:                     top((cEpoch/2 + 1)%2) := head
76:                     for i = 1 to N do
77:                         vOp := vColl[i]
78:                         if vOp >= ANN then
79:                             push(top((cEpoch/2 + 1)%2)), pfence()
value field of the paired PUSH operation, but the response of that PUSH operation might not have been updated before the crash, hence it might be coupled with a second POP operation after the crash, thus violating correctness. A similar problem may arise for operations that are applied by accessing the linked-list representing the stack. Consequently, in such cases, the recovery combiner must re-apply all operations and therefore needs to re-collect all the announcements of the crashed combining phase, regardless of their response values. In order to allow identifying operations that must be re-collected, each announcement structure stores the epoch in which it was collected by the combiner.

The combiner inserts operations into pop and push operation lists – to be latter combined and applied. Since there are at most \( N \) PUSH and POP operations, these lists are implemented using volatile arrays of size \( N \). We also use a volatile array \( vColl \) of size \( N \), indicating for each thread whether its operation has been collected and, if so, storing the index of the active announcement structure (line 94). If no operation was collected for a thread, the corresponding entry is set to \( \bot \) (line 102). In the loop of line 103 the combiner performs the actual reduction/elimination by eliminating couples of PUSH and POP operations, as long as none of the lists is exhausted, and updates their responses directly without accessing the linked list stack representation. This elimination reduces the number of \( pwb \) instructions, since accessing the stack requires additional \( pwb \)s, to persist the changes made to it. Finally, REDUCE returns the surplus push or pop operations. It does so by returning the number of surplus operations left. A positive number indicates surplus PUSH operations, while a negative number indicates surplus POP operations. This way, the combiner can later access these operations using the appropriate operations list.

COMBINE then applies the surplus operations, returned by REDUCE, to the stack. The while loop in line 55 deals with the case of surplus PUSH operations, and the while loop in line 69 deals with the case of surplus POP operations. For each PUSH operation, a new non-volatile node is allocated and added to the central stack, representing the actual operation. In addition, ACK is updated as the response value. Likewise, for each POP operation, a node is removed from the stack (if one exists), its key is used as the response value (line 73), and finally the node is de-allocated. After applying all operations to the stack, the next top entry – \((cEpoch/2 + 1)\)%2, is set to point to the new head of the stack. If there was no surplus, the new top entry equals the previous top entry. Finally, the combiner persists all modified variables, specifically, all the combined announcement structures (line 80) and the updated top entry, using \( pwb \) instructions for all these variables, followed by a single pfence instruction. After ensuring that the stack and all responses are in a consistent and persistent state, \( cEpoch \) is incremented twice and persisted once in between these two updates. Then, the combiner releases the combiner lock in line 85 and COMBINE returns. The operation of the combiner is guaranteed to have been completed, thus the thread returns its response in line 18.

\( cEpoch \) is incremented twice in order to deal with the following scenario. Consider a configuration in which the combiner increments \( cEpoch \) from \( v \) to
Suppose additionally that some thread \( t \) managed to observe the updated \( c\text{Epoch} \) before the crash. Thus, \( t \) observed a return value and can conclude that its operation was completed, therefore \( t \) may “safely” complete its operation and begin a new one. However, after the crash, the recovery function may observe the old \( c\text{Epoch} \) value \( v \) again, concluding that \( t \)’th operation was not performed. Moreover, this is indistinguishable from the case in which a crash occurred in the middle of the combining phase, before \( c\text{Epoch} \) was updated. However, in the first case it is not safe to re-execute \( t \)’th operation after recovery, since \( t \) may have started a new one, while in the second case \( t \)’s operation must be executed upon recovery, as it did not take effect. To solve this issue, we release non-combiner threads only when they observe that \( c\text{Epoch} \) was incremented twice (lines 21–22), thus ensuring that the announced operations were linearized properly and that the combiner successfully persisted \( v + 1 \) in line 53. In case of a crash, if the value of \( c\text{Epoch} \) is reverted back to an odd number \( v + 1 \), it is safe to consider the epoch phase \( v \) as completed, and simply fix \( c\text{Epoch} \) to \( v + 2 \). For this reason, we only persist \( c\text{Epoch} \) after updating it to \( v + 1 \), but not after updating it to \( v + 2 \).

We next describe what non-combiner threads do while waiting for their response. In line 21, a non-combiner busy-waits for the combiner to increase \( c\text{Epoch} \) by 2 (or more). If this condition is satisfied, it is guaranteed that all combined announcement structures received valid response values. Consequently, if the non-combiner thread finds a response value in line 47, it can safely return that value. Otherwise, if \( c\text{Epoch} \) was incremented but there is no response value, the thread has arrived late, that is, it has completed announcing its operation only after the combiner checked its announcement structure. In this case, \( \text{opEpoch} \) is incremented by two in line 48 in order to wait for the next combiner to collect the operation. The algorithm guarantees that this scenario can occur only once, since the next combiner will surely collect the thread’s announcement. Note that if a non-combiner announces an operation after the combiner increases the epoch counter but before it releases the lock, that thread might spin forever waiting for a combiner in line 21. Line 22 deals with this scenario, by attempting to capture the combiner lock again in case the lock is released and the epoch number was not incremented. To facilitate better understanding of the data structure used by DFC, we illustrate below two configurations reached in the course of its execution. In the first configuration, depicted by Figure 2a, the current epoch number is 10 but all announcement structures were last updated in previous combining phases. There is no active combiner in this configuration. Each thread is associated with a 2-bit entry in the \( \text{valid} \) array, whose LSB indexes a two-entry array of announcement structures (shown below the \( \text{valid} \) array). The LSB of the \( \text{valid} \) entry indicates which is the active announcement structure of the corresponding thread. The MSB of the \( \text{valid} \) entry indicates whether the announcement is complete (i.e. valid). A combiner should combine an announcement if it is active, the MSB of the corresponding \( \text{valid} \) entry is set, and the \( \text{val} \) field of the announcement was not yet set (i.e. it equals \( \bot \)). Announcement entries that are
colored in grey correspond to active announcements. The dotted announcement entry of $p_4$ is still not ready, as indicated by the MSB bit of the corresponding $valid$ entry. Consequently, it was not previously combined and thus its return value was not set yet. The two-entry array $top$ stores two pointers to the stack below. The current entry of $top$ is determined by the value $(cEpoch/2)\%2$, so the second cell, colored in grey, is the current entry of $top$ in this configuration.

Figure 2b depicts a second configuration, in which a combining phase is ongoing. The announcement structures of threads $p_1, p_2, p_4$ and $p_5$ were combined. Announcement structures colored in dark grey correspond to valid announcements that were combined in the current combining phase. In this configuration, the combiner, thread $p_4$, already updated the response values of the operations by $p_1, p_2, p_4$, but still did not update the response value of $p_5$’s operation. Here, the combiner eliminated the operations of $p_1$ and $p_2$ without accessing the stack, updated the epoch number and the response value of its own operation and added a corresponding node to the stack. As we described previously, if the system crashes in this configuration (before $cEpoch$ is incremented), all these operations must be combined and applied again.

The Recovery Procedure. In case of a crash, all threads execute the RECOVER procedure upon recovery (Algorithm 1(right)). If required, the recovery function recovers the shared stack by re-executing the last combining phase, thus completing all pending operations and updating their responses. Each thread first attempts to capture the recovery lock $rLock$ that protects the critical section of the recovery code. If the thread fails to capture the lock, it simply busy-waits until the lock is freed in line 42. If it succeeds, it becomes the recovery combiner. The recovery combiner increments the current epoch number to an even number (line 28), in case there was a crash after the first $cEpoch$ increment was persisted but before the second increment was persisted (lines 82-84). Note that it is safe to simply increment $cEpoch$ to the next even number, since, as was previously explained, if an odd value of $cEpoch$ was persisted, all operations from the previous epoch phase, $v$, were already linearized and persisted. In order to maintain the consistency and durability of $cEpoch$ for all future arriving threads, a $pwb$ and $pfence$ instructions are executed in line 30. The recovery combiner then fixes inconsistencies in the memory layout by performing garbage collection (line 31), as explained in Section 4 which describes memory management in our algorithm.

Then all announcement structures are traversed again. For each thread, the MSB of the $valid$ field is set in line 36. This allows the recovery combiner to later combine and apply the operation, if needed. The if statement in lines 37-38 is needed for operations that were applied during the last crashed combining phase for which response values were persisted before the crash. In this case, DFC needs to re-collect and re-apply these operations during the recovery. Note that the epoch number of operations that received a response value in the last combining phase was updated to the current epoch number in line 93. Since both the response field $val$ and the epoch number field $epoch$ reside in the same aligned cache line of 64 bytes, our machine’s architecture guarantees that they
are flushed together to the persistent memory. Consequently, if the response value was persisted before the crash, so was the epoch number. Thus, after the execution of line 38, all the announcement structures from the last combining phase have empty response values. We emphasize that even if this guarantee does not hold for other NVM-based machines, one could simply add a \texttt{pwb} instruction after the write to the \texttt{epoch} field in \texttt{Reduce}.

The recovery combiner proceeds by starting another combining phase in line 39. All operations from the last crashed combining phase will be collected and applied again in the \texttt{Reduce} function. We note that threads that did not manage to complete the announcement of their operations before the crash are not re-executed. Finally, the recovery combiner releases the lock in line 40 and returns its own response value (as do all other threads) in line 43.
Our DFC queue and deque algorithms are very similar to that of the DFC stack, except that we do not employ elimination in our queue implementation because this technique is more suitable for LIFO than for FIFO order. We provide the pseudo-codes of these implementations in Appendix A.

4 Memory Management

Several general Persistent Memory Management (PMM) schemes have been proposed in recent years. Makalu [7] is a PMM for NVM-based systems. A PMM was also designed and implemented as part of Atlas [8]. However, for efficiency reasons, many applications designed for NVM-based systems, and specifically PTMs, implement their own memory management schemes. For example, Romulus [10] and OneFile [23] pre-allocate all required memory before performing any transactions and maintain it during the execution with no extra calls to an external PMM. This allows the application to optimize memory management to fit its specific requirements, while avoiding any memory leakage in case of a crash.

Our implementation of DFC takes a similar approach and first allocates all required memory into a nodes pool of a user-defined size. During the execution of the algorithm, it utilizes this memory by synthetically allocating and deallocating the nodes of the actual data-structure (lines 60, 76). Before exiting, this memory is freed. Therefore it is insignificant to optimize the single allocation and deallocation from the NVM at the beginning and the end of the execution, respectively. We used libpmemobj-cpp for doing that.

DFC uses several fixed-size non-volatile variables: cEpoch, top and the announcement array tAnn, whose number of entries equals the number of threads that may access the data structure. The actual data-structure consists of nodes that represent the values that reside in the stack and which can be accessed via the top pointers. Node allocation is implemented by finding some free node from the pool that was allocated beforehand, followed by a declaration that the node is used using a flag bit. Similarly, deallocating a node is implemented by resetting the used flag of that node.

To track which nodes are free and which are used, we implemented a standard bit-map hierarchy. Assuming a 64-bit system, we use 64 words, in which each bit indicates whether the corresponding node is currently used or not, for a total of $64^2$ nodes. An additional word is used at the “root” of this shallow tree, indicating which of the lower-level words have at least a single free node. Each time a node is allocated or deallocated, the root word and the lower-level word corresponding to the node are accessed. This hierarchy can be easily extended to support more nodes by adding more levels, at the cost of a moderate increase in the time complexity of memory management routines.

In order to support persistence in the presence of system crashes, we use the following approach. During the Recover procedure, the recovery combiner executes a garbage collection (GC) cycle in line 31 before accessing the memory. Notice that this GC cycle is performed once by the combiner, in the absence
of concurrency, while all other threads are waiting for the combiner to release the lock. During the GC cycle, the combiner marks all nodes that are accessible from the active top entry as used, and all other nodes as free. As a result, there is no need to keep the bit-map tree persistent and so we store it in volatile memory. Clearly, the nodes themselves must be kept persistent. This GC mechanism achieves very lightweight memory management in normal operation at the cost of more expensive recovery. Since crashes are typically infrequent, this is a reasonable tradeoff.

5 Outline of correctness proof for DFC-Stack

**Linearizability.** Consider an execution of DFC. Denote the value of $cEpoch$ in the beginning of the latest combining phase as $e$. Assume process $p$ was the first process to win $cLock$ as the combiner in $cEpoch = e$. We next provide the linearization points for all threads that submitted an operation, in the following two cases: 1) $p$’s first $cEpoch$ modification in line 82 was not persisted to the NVM, 2) $p$’s first $cEpoch$ modification in line 82 was successfully persisted to the NVM, i.e. $cEpoch$ stores $e' > e$ in the persisted memory.

As long as the first case holds, no operation of any thread will be linearized. However when the second case holds, all threads that were collected in the current epoch number, i.e. threads for which the if statement in line 92 was evaluated as true for the combiner, are linearized immediately when the first change to $cEpoch$ is persisted to the NVM.

Note that the second case is possible if we assume that from some point in time, threads do not fail-stop, and therefore eventually there will be an epoch in which threads will be allowed to complete their execution before the system fails. Then, after some additional crash-free steps of the system, the epoch number will be incremented again and all collected threads will be able to retrieve their response values.

First all the collected combined operations are linearized, followed by all other collected operations, in an increasing order of their IDs - which is the order in which the combiner collects them in line 89. If a couple of push and pop operations were combined in REDUCE, then the pop operation will be linearized immediately after the push operation. Any other threads that finished submitting their jobs after the combiner concluded collecting the submitted operations of the current epoch, will not be linearized. These threads are considered as late arriving threads, and they are guaranteed to be collected and linearized in the next crash-free combining phase.

In case of a crash while the first case holds ($p$’s first $cEpoch$ modification was not persisted to the NVM), in RECOVER another process $q$ wins $cLock$ and becomes the recovery combiner. The same logic as above applies to this case - until case 2 is fulfilled, while substituting the recovery combiner thread $q$ with $p$.

Note that crashes while case 2 holds do not break linearizability, as operations from the last combining phase that were linearized just after the change to
cEpoch was persisted will not be collected again because their response value field will not be reset in line 38, and therefore will not be empty in line 92.

**Starvation-freedom for crash-free executions.** We assume for the progress condition, that starting from some point there are no more system failures or, at least, the system does not crash again until all threads complete their current operations. Otherwise, no progress can be established if the system crashes before threads complete their operations.

Consider the crash-free execution that begins from the point above. Note that as long as a thread submits an operation, after a finite number of steps (of the combiner, or the next combiner if this thread is late arriving), its operation is guaranteed to be applied, from similar arguments to FC [14]. It is left to notice that after a finite number of steps, (line 12) each thread finishes to submit its new operation.

### 6 Experimental Evaluation

In order to evaluate the performance of the DFC stack, we compared it to implementations using Romulus [10], OneFile [23] and libpmemobj-cpp (PMDK) [2]. Romulus is a lock-based PTM that uses flat combining for update transactions. It uses two copies of the memory, a main copy and a backup copy. Transactions are first performed and persisted to the main copy, and then are copied to the backup. In case of a crash, one of the copies is consistent, and is the one used upon recovery. OneFile is a wait-free PTM. It uses double-word-compare-and-swap (DCAS) instructions. Each update transaction is associated with a unique transaction identifier and all writes are done using a DCAS, writing the new value together with the identifier of the transaction that issues the write. PMDK is an open-source collection of libraries and tools to simplify managing and accessing persistent memory devices. It provides an undo-log based PTM. We note that none of these PTMs provides detectability.

**Experimental Setting and Benchmarks.** Our experiments were conducted using a machine equipped with two sockets of Intel Xeon Gold 5215 processors, each with a cache size of 13.75 MB. It contains a total of 20 physical and 40 logical cores and 4 256GB Intel Optane Persistent Memory Modules configured to the App Direct mode. The machine contains also 192 GB of RAM and runs on CentOS Linux with kernel version 5.8.7. All algorithms were implemented in C++ and compiled with g++ (version 9.1.0) with O2 optimizations. On Intel architectures [19], the `pwb` instruction is translated to `clwb`, `clflush` or `clflushopt` depending on what the machine at hand supports, where `clflushopt` is the most efficient option. In addition, the `pfence` and `psync` instructions are translated to `sfence`. Consequently, our code uses the `clflushopt` instruction and assumes that the execution of `sfence` ensures also the functionality of `psync`.

The first benchmark we used is the push-pop benchmark, in which we executed 1M couples of push and pop operations, that were distributed equally between the threads. In the second benchmark, called rand-op, each thread chooses
randomly and independently each of its operations to be either a push or a pop operation. In total, 2M operations are performed, distributed equally between the threads. We ran the benchmarks using a varying number of threads in order to test algorithms’ throughput and scalability. Each experiment was repeated 10 times and we report on median results.

**Analysis of Stack Experimental Results.** Figure 3a shows that DFC and ROMULUS outperform ONEFILE and PMDK by a wide margin for all concurrency levels except 1. DFC is outperformed by ROMULUS for up to 8 threads. However, DFC scales linearly from 4 to 16 threads and continues to scale up until concurrency levels of more than 30 threads. Specifically, with 16 threads, DFC outperforms
ROMULUS, ONEFILE and PMDK by factors of $\times 1.727$, $\times 16.542$, $\times 13.289$, respectively. It maintains and even slightly increases these factors for 40 threads, to $\times 2.053$, $\times 15.868$ and $\times 16.279$, respectively.

Figures 3c-3e present the average number of persistence instructions ($\text{pwb}$ and $\text{pfence}$ instructions, respectively) per operation performed by the algorithms across the concurrency range. It can be seen that algorithm performance is highly dependant on the number of persistence instructions executed by its operations. As the PMDK stack is significantly outperformed by all other algorithms in all concurrency levels, we do not analyze its performance in the evaluation that follows. ONEFILE assumes an x86 architecture in which a compare-and-swap (CAS) instruction acts as an implicit $\text{pfence}$ and therefore does not execute $\text{pfence}$ instructions explicitly. Consequently, we count the number of CAS instructions in ONEFILE as an estimate of the number of $\text{pfence}$ instructions it executes. For the DFC stack, we present two types of measurements: DFC in blue, and DFC-TOTAL in dashed blue. DFC-TOTAL refers to the total number of $\text{pwb}$ and $\text{pfence}$ instructions performed during the execution, while DFC excludes the persistence instructions that are performed during the announcement process (lines 9, 11), since those are performed by threads in parallel.

The parallel $\text{pwb}$ and $\text{pfence}$ instructions performed by any specific thread do not block the progress of other threads, and therefore penalize the performance of the DFC stack less than persistence instructions performed by a combiner thread. This statement is supported by the fact that the throughput of DFC outperforms that of ROMULUS, although the $\text{pfence}$ count of DFC-TOTAL is higher than that of ROMULUS, while the $\text{pfence}$ count of DFC is lower. Furthermore, we emphasize that although in general all $\text{pwb}$ instructions incur a similar cost, the execution time of a $\text{pfence}$ instruction may vary significantly. In fact, since $\text{pfence}$ instructions enforce the ordering and completion of all proceeding $\text{pwb}$ instructions, the execution time of each $\text{pfence}$ instruction highly depends on the number of $\text{pwb}$ instructions that precede it. Thus, the costs of the $\text{pfence}$ instructions of DFC (inside the COMBINE procedure) and ROMULUS are more dominant than the costs of the additional two parallel $\text{pfence}$ instructions that are only preceded by a small number of $\text{pwb}$ instructions.

The $\text{pwb}$ and $\text{pfence}$ graphs have a lot in common. For both, in the sequential case, ONEFILE starts with a small number of persistence instructions per operation compared to the other algorithms. However, for concurrency levels of 4 or more, it requires a larger number of persistency instructions. This explains the lack of scalability in the throughput of ONEFILE that is evident from Figure 3a. The persistency instruction counts of both DFC and ROMULUS start with a relatively steep descent as concurrency rises up to 16 threads and then stabilize. This explains the initial high throughput scalability ($\leq 16$ threads) which is then followed by a more moderate throughput increase (for $> 16$ threads) for both DFC and ROMULUS. This similarity is not surprising, considering the fact that both DFC and ROMULUS employ flat combining, and consequently, for high levels of concurrency they are both able to combine together larger

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\footnote{See [11] for a similar $\text{pwb}$ evaluation of queue implementations, including PMDK.}
numbers of operation and thus reduce the average per-operation number of persistency instructions. In addition, the ratios between the average number of pwb per operation between Romulus and Dfc-Total and between OneFile and Dfc-Total in concurrency level 40 (×2.51 and ×11.69, respectively) are quite close to those between the corresponding throughputs. Indeed, as we have described, the number of per-operation pwb instructions is an important indicator of an algorithm’s performance in NVM-based platforms.

The push-pop benchmark is favorable to the DFC stack because it allows to combine many operations by eliminating pairs of push and pop operations. In order to evaluate DFC on a more challenging workload, we use the rand-op benchmark. All algorithms except Dfc present no significant change in throughput in comparison to the push-pop benchmark. However, in this benchmark, Dfc’s performance drops significantly in comparison to the push-pop benchmark. Nevertheless, DFC stack outperforms all other algorithms also in this benchmark for concurrency levels higher than 8, albeit by a significantly lower margin. Figures 3e and 3f show that all algorithms maintain more-or-less the same average number of persistency instructions per operation on both benchmarks.

In order to better understand the performance drop in Dfc’s throughput in the rand-op benchmark, we also measured the average number of combining phases per operation in both. The results shown, a larger number of combining phases is performed by DFC in the rand-op benchmark. Consequently, a smaller number of operations is combined in each such phase on average, resulting in a smaller number of push and pop pairs that can be eliminated.

We remind the reader that Dfc is the only detectable stack implementation out of those we evaluated. In addition to providing higher throughput, the memory requirements of the DFC stack are roughly half of what is required by Romulus. This is because whereas Romulus uses two copies of all variables (including the main data structure, memory management data and required metadata), Dfc needs only a single copy of the stack and requires two copies of only the announcement structures and top pointers.

Figure 5 shows the effect of canceling pair operations in the stack algorithm. In both benchmarks, canceling improved the stack performance, however, the improvement is less significant in the rand-op benchmark, due to less cancelling.

The performance evaluation of our queue and deque implementations shows the same trends, and appears in Appendix A.

7 Discussion

This work presents the DFC stack—the first non-transactional persistent stack algorithm. The new algorithm provides detectability and higher throughput in comparison to PTM-based alternatives, especially so in workloads where many push and pop operation-pairs can be eliminated. It establishes that the usage of FC can leverage object-specific semantics so that the number of persistence instructions is significantly reduced. We have also shown how DFC can applied to obtain additional detectable objects—queues and doubly-ended queues.
Friedman et al. [13] introduced detectability and proposed a detectable queue implementation. Detectability was formalized by nesting-safe recoverable linearizability [4]. An alternative formalization named detectable sequential specification, recently proposed by Li and Golab [21], allows a thread to declare, per object operation, whether it requires detectability or not, by extending the object’s interface. There exist detectable implementations for read-write registers and compare-and-swap (CAS) [4–6]. Capsules [6] is a generic transformation making any implementation using read and CAS detectable, by replacing each primitive with its detectable counterpart. Persistent universal constructions [9, 11] imply a persistent version of any concurrent object, but none of them is detectable. Very recent work [12] presents detectable implementations of several objects, including a stack. Their algorithms employ combining as well, but, as they mention, there are some differences in technical implementation details. We have provided our previously-archived code to the authors and the performance evaluation they present shows higher throughput in comparison to our DFC stack for high concurrency levels, on a different machine than the one we used. We did not have access to their code, and therefore were not able to
fully explore the differences between the two implementations nor to evaluate the performance of their implementation on our machine.

Acknowledgments

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A DFC-based Queue and Deque

A.1 Code for DFC Queue and Deque

Based on the DFC stack shown before we implemented a DFC based queue and deque. These objects follows closely the DFC algorithm. both are represented by a linked list.

DFC Queue implement a FIFO queue that allows two operations - enqueue and dequeue. To perform them a thread first announce them. Then, it tries to capture the lock and become a combiner. If it succeeds, it proceeds to execute Combine; otherwise, it waits in LockTaken until its operation is applied by the combiner. Opposed to the Stack the DFC Queue don’t use a reduce procedure to cancel pairs of operations, The cases which allow the FIFO queue to perform cancels are limited reducing the benefits we saw in the case of the stack. Upon recovery from a crash, each resurrected thread executes the Recover procedure which remains without changes from the stack algorithm. The queue algorithm and data structures are further presented in figure 8 and algorithm 3.

DFC Deque an object supporting both FIFO and LIFO operations - pushFront, popFront allows to push and pop nodes from the front side of the list. pushRear, popRear allows to push and pop nodes from the rear side of the list. To perform them a thread first announce them. Then, it tries to capture the lock and become
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A combiner. If it succeeds, it proceeds to execute COMBINE; otherwise, it waits in LOCKTAKEN until its operation is applied by the combiner. The combiner first traverses an announcement array and eliminates pairs of PUSH and POP on the same side of the queue - for example pairs of PUSHFRONT and POPFRONT are canceled via the REDUCE procedure. Then, it commits the surplus announced push or pop operations.

Upon recovery from a crash, each resurrected thread executes the RECOVER procedure which remains without changes from the stack algorithm. The deque algorithm and data structures are further presented in figure 9 and algorithms 15.

A.2 DFC Queue and Deque experimental results

Experimental Setting and Benchmarks Our experiments were conducted using a machine equipped with two sockets of Intel Xeon Gold 5215 processors, with a cache size of 13.75 MB each. It contains a total of 20 physical and 40 logical cores and 4 256GB Intel Optane Persistent Memory Modules configured to the App Direct mode. The machine contains also 192 GB of RAM and runs on CentOS Linux with kernel version 5.8.7. All algorithms were implemented in C++ and compiled with g++ (version 9.1.0) with O2 optimizations. On Intel architectures [19], the pwb instruction is translated to clwb, clflush or clflushopt depending on what the machine at hand supports, where clflushopt is the most efficient option. In addition, the pfence and psync instructions are translated to sfence. Consequently, our code uses the clflushopt instruction and assumes that the execution of sfence ensures also the functionality of psync.

In the case of queue - The first benchmark we used is the enq-deq benchmark, in which we executed 1M couples of enq and deq operations, that were distributed equally between the threads. In the second benchmark, called rand-op, each thread chooses randomly and independently each of its operations to be either a enq or a deq operation. In total, 2M operations are performed, distributed equally between the threads. We ran the benchmarks using a varying number of threads in order to test algorithms’ throughput and scalability. Each experiment was repeated 10 times and we report on median results.

In the case of deque - The first benchmark we used is the pushf-pushr-popf-popr benchmark, in which we executed 1M couples of push and pop operations, that were distributed equally between the threads. The side in which the pair is executed front/rear is chosen randomly. In the second benchmark, called rand-op, each thread chooses randomly and independently each of its operations to be either a pushFront, popFront, pushRear or popRear operation. In total, 2M operations are performed, distributed equally between the threads. We ran the benchmarks using a varying number of threads in order to test algorithms’ throughput and scalability. Each experiment was repeated 10 times and we report on median results.

Queue Experimental Results Graphs are presented in Figure 6. As shown by Figure 6a and 6b, DFC and ROMULUS outperform OneFile and PMDK by a
Fig. 6: Queue Evaluation: Throughput for the enq-deq benchmark and rand-op benchmark.

(a) enq-deq throughput
(b) rand-op throughput

Fig. 7: Deque Evaluation: Throughput the push-pop benchmark and rand-op benchmark.

(a) pushf/r-popf/r throughput
(b) rand-op throughput

Wide margin for all concurrency levels. And DFC outperforms Romulus through all concurrency levels in the queue test.

Deque Experimental Results Graphs are presented in Figure 7. As shown by Figure 7a and 7b, DFC and Romulus outperform OneFile and PMDK by a wide margin for all concurrency levels.

A.3 Outline of correctness proof for DFC Queue and Deque

The same correctness proof arguments that were presented for the stack object in Appendix 5 can be applied for the queue and the deque objects, except for few small modifications, specifically in the 2nd case, in which the first eEpoch modification in lines 36 and 76 respectively was successfully persisted to the NVM. While in the stack all the collected operations (first the combined couples and then all others) were linearized in an increasing order of their IDs, in the queue first all the collected enqueue operations are linearized in an increased order of their IDs, followed by all the collected and ordered dequeue operations. In the deque, first all the collected combined operations on the head of the
queue are linearized in an increasing order, and then the collected combined operations on the tail are linearized in an increasing order. Finally all other collected operations on the head, followed by the collected operations on the tail are linearized in an increasing order.

```plaintext
type Node {
    Integer param
    Node* next
}

Type TAnnounce {
    2-bit variable valid
    Announce ann[2]
}

type Announce {
    Integer val
    Integer epoch
    Integer param
    {Enq, Deq} name
}

▷ Non-Volatile shared variables:
- Integer cEpoch, initially 0
- Node* top[2], initially both ⊥
- Node* bot[2], initially both ⊥
- TAnnounce tAnn[N], initially all fields are 0

▷ Volatile shared variables:
- CAS variable cLock, initially 0
- CAS variable rLock, initially 0
- Integer enqList[N], deqList[N], vColl[N], initially all 0

Fig. 8: DFC Queue: types and initialization
Algorithm 3 DFC Queue. Pseudocode for Combine and Collect procedures.

1: procedure Combine() 41: procedure Collect() 2: tEnq, tDeq := \textit{Collect}() 42: tEnq, tDeq := 1 3: head := top[(cEpoch/2)[2]] 43: for i = 1 to N do 4: tail := bot[(cEpoch/2)[2]] 44: vOp := tAnn[i].val 5: if tEnq > 0 then 45: MSB(vOp) = 1 and opVal = ∅ then 6: while tEnq > 0 do 46: tEnq −− 47: cId := enqList[tEnq] 8: cId := enqList[tEnq] 48: vOp := vColl[cId] 9: param := tAnn[cId].ann[vOp].param 49: nNode := \textit{Allocate Node} (param, tail) 10: nNode := \textit{Allocate Node} (param, tail) 11: tAnn[cId].ann[vOp].val := ACK 12: tAnn[cId].ann[vOp].val := ∅ 13: pwb(&nNode) 14: tail := nNode 15: if tDeq > 0 then 16: while tDeq > 0 do 17: tDeq −− 18: cId := deqList[tDeq] 19: vOp := vColl[cId] 20: if head = ∅ then 21: |tAnn[cId].ann[vOp].val := EMPTY 22: else 23: tAnn[cId].ann[vOp].val := 24: tempHead := head 25: head := head.next 26: Dealocate Node (tempHead) 27: if head = ⊥ then 28: tail = ⊥ 29: top[(cEpoch/2 + 1)[2]] := head 30: bot[(cEpoch/2 + 1)[2]] := tail 31: for i = 1 to N do 32: vOp := vColl[i] 33: if vOp ≠ ⊥ then pwb(&tAnn[i].ann[vOp]) 34: pwb(top[(cEpoch/2 + 1)[2]]); 35: pwb(bot[(cEpoch/2 + 1)[2]]); pfence() 36: cEpoch + + 37: pwb(&cEpoch); pfence() 38: cEpoch + + 39: cLock := 0 40: return
type Node {
    Integer param
    Node* next
    Node* prev
}

Type TAnnounce {
    2-bit variable valid
    Announce ann[2]
}

▷ Non-Volatile shared variables:
- Integer cEpoch, initially 0
- Node* top[2], initially both ⊥
- Node* bot[2], initially both ⊥
- TAnnounce tAnn[N], initially all fields are 0

▷ Volatile shared variables:
- CAS variable cLock, initially 0
- CAS variable rLock, initially 0
- Integer pushFrontList[N], popFrontList[N], vColl[N], initially all 0
- Integer pushRearList[N], popRearList[N], initially all 0

Fig. 9: DFC Deque: types and initialization
Algorithm 4 DFC Deque. Pseudocode for COMBINE procedure.

```
1: procedure COMBINE( )
2:   tIndexFront, tIndexRear := REDUCE()
3:   head := top[(cEpoch/2)%2]
4:   tail := bot[(cEpoch/2)%2]
5:   if tIndexFront < 0 then
6:     while tIndexFront > 0 do
7:       tIndexFront := −−
8:       cId := pushFrontList[tIndexFront]
9:       vOp := vColl[cId]
10:      param := tAnn[cId].ann[vOp].param
11:      nNode := ALLOCATE NODE (param)
12:      nNode.an.id := tAnn[cId].ann[vOp].val := ∅K
13: else if tail =⊥ then
14:     head := nNode
15: else if head := nNode
16:     tail := nNode
17: else
18:     tIndexRear := −−
19:     cId := popFrontList[tIndexRear]
20:     vOp := vColl[cId]
21:     if head =⊥ then
22:       tIndexRear := −−
23:       cId := popFrontList[tIndexRear]
24:       vOp := vColl[cId]
25:     if head =⊥ then
26:       tAnn[cId].ann[vOp].val := EMPTY
27: else
28:     tAnn[cId].ann[vOp].val := head.param
29:     tempHead := head
30:     head := head.next
31:     if head =⊥ then
32:       head.prev :=⊥
33:     else
34:       tail :=⊥
35:       DEALLOCATE NODE(tempHead)
36: if tIndexRear > 0 then
37:     while tIndexRear > 0 do
38:       tIndexRear := −−
39:       cId := pushRearList[tIndexRear]
40:       vOp := vColl[cId]
41:      param := tAnn[cId].ann[vOp].param
42:      nNode := ALLOCATE NODE (param)
43:      nNode.an.id := tAnn[cId].ann[vOp].val := ∅K
44: else if tail =⊥ then
45:     head := nNode
46:     tail := nNode
47: else
48:     nNode.prev := tail
49:     tail.next := nNode
50:     tail := nNode
51: else
52:     if tIndexRear < 0 then
53:     while tIndexRear > 0 do
54:       tIndexRear := −−
55:       cId := popRearList[tIndexRear]
56:       vOp := vColl[cId]
57:     if tail =⊥ then
58:       tAnn[cId].ann[vOp].val :=
59:       tail.param
60:     if tail prev =⊥ then
61:       head :=⊥
62:     else
63:       tail := tail.prev
64:     tail.next :=⊥
65:     DEALLOCATE NODE(tempHead)
66:     for i = 1 to N do
67:       vOp := vColl[i]
68:     if eOp =⊥ then p-node(kAn[i].ann[vOp])
69:     p-node(top(cEpoch/2 + 1)%2)
70:     p-node(top(cEpoch/2 + 1)%2); p-fence()
71: eEpoch +
72: p-node(kcEpoch); p-fence()
73: eEpoch +
74: eLock := 0
75: return
```
Algorithm 5 DFC Deque. Pseudocode for REDUCE procedure.

1: procedure REDUCE( ) 27: while tPushFront ≠ −1 and
2: tPushFront := −1 28: cPush := pushFrontList[tPushFront]
3: tPopFront := −1 29: cPop := popFrontList[tPopFront]
4: tIndexRear, tIndexFront := −1 30: vPush := vColl[cPush]
5: for i = 1 to N do 31: tAnn[cPush].ann[vPush].val := ⊥
6: vOp := tAnn[i].valid 32: vPop := vColl[cPop]
7: opVal := tAnn[i].ann[LSB(vOp)].val 33: tAnn[cPop].ann[vPop].val :=
8: if MSB(vOp) = 1 and opVal = ⊥ then 34: tAnn[cPush].ann[vPop].param
9: tAnn[i].ann[LSB(vOp)].epoch := 35: tPushFront :=
10: cEpoch 36: tPopFront := −
11: vColl[i] := LSB(vOp) 37: while tPushFront ≠ −1 and
12: if tAnn[i].ann[LSB(vOp)].name = 38: tPopFront ≠ −1 do
13: PushFront then 39: cPush := pushRearList[tPushRear]
14: tPushFront := i + 40: cPop := popRearList[tPopRear]
15: pushFrontList[tPushFront] := i 41: vPush := vColl[cPush]
16: tPushFront := + 42: cPop := pushFrontList[tPopFront]
17: pushRearList[tPushRear] := i 43: vPop := vColl[cPop]
18: else 44: tAnn[cPop].ann[vPop].val :=
19: if tAnn[i].ann[LSB(vOp)].name = 45: tAnn[cPush].ann[vPop].param
20: PushRear then 46: tIndexFront = tPushFront + 1
21: tPopRear := + 47: if tPopFront ≠ −1 then
22: popRearList[tPopRear] := i 48: tIndexFront = −1 * (tPopFront + 1)
23: else 49: if tPushRear ≠ −1 then
24: tPopFront := + 50: tIndexRear = tPushRear + 1
25: popFrontList[tPopFront] := i 51: if tPopRear ≠ −1 then
26: vColl[i] := ⊥ 52: tIndexRear = −1 * (tPopFront + 1)
53: return tIndexRear, tIndexFront