Performance Optimizations of Recursive Electronic Structure Solvers Targeting Multi-Core Architectures
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Abstract

1 Abstract

As we rapidly approach the frontiers of ultra large computing resources, software optimization is becoming of paramount interest to scientific application developers interested in efficiently leveraging all available on-Node computing capabilities and thereby improving a requisite science per watt metric. The scientific application of interest here is the Basic Math Library (BML) that provides a singular interface for linear algebra operation frequently used in the Quantum Molecular Dynamics (QMD) community. The provisioning of a singular interface indicates the presence of an abstraction layer which in-turn suggests commonalities in the code-base and therefore any optimization or tuning introduced in the core of code-base has the ability to positively affect the performance of the aforementioned library as a whole. With that in mind, we proceed with this investigation by performing a survey of the entirety of the BML code-base, and extract, in form of micro-kernels, common snippets of code. Since the data structure of the core BML code-base is well established we pursue less invasive optimization strategies, that is, we focus our effort on optimizing at the thread level as opposed to modifying the data-structures for performance at the Single Instruction Multiple
Data (SIMD) scale. We incorporate several active and passive directives/pragmas that aid to inform the compiler on nature of the data-structures and algorithms. Following that, we introduce several optimization strategies into these micro-kernels including 1.) Strength Reduction 2.) Memory Alignment for large arrays 3.) Non Uniform Memory Access (NUMA) aware allocations to enforce data locality and 4.) appropriate thread affinity and bindings to enhance the overall multi-threaded performance. After introducing these optimizations, we benchmark the micro-kernels and compare the run-time before and after optimization for several target architectures. Finally we use the results as a guide to propagating the optimization strategies into the BML code-base. As a demonstration, herein, we test the efficacy of these optimization strategies by comparing the benchmark and optimized versions of the code using a 1.) matrix-matrix multiplication using the ELLPACK format and 2.) a full simulation using ExaSP2, a proxy application for linear scaling electronic structure calculations. The results of the optimization are promising and in agreement with findings in literature.

**Keywords** MULTI-THREADED OPTIMIZATIONS · STRENGTH REDUCTION · MEMORY ALIGNMENT · NON UNIFORM MEMORY ACCESS · DATA LOCALITY · THREAD AFFINITY AND BINDINGS · MULTI-THREADED PERFORMANCE

2 Introduction

3 Introduction

The optimization of electronic structure codes requires different efforts including the improvement of solvers, and the adaptation of basic operations to novel computer architectures. With the advent of the exascale computing architectures, the aforementioned adaptation requires thorough modifications in order to maximize the use of the computational capacity \[12\]. Furthermore, in the specific case of electronic structure calculations, different chemical systems require specific solver as well as specific architecture adaptation, and generally, what is beneficial for some systems will not necessarily be for others. QMD technique requires solving for the electronic structure of the physical system to advance the positions of the atoms at each simulation time-step. Solving for the electronic structure is generally a task that involves a high computational cost due to the fact that the number of arithmetic operations scale with the cube of the number of atoms. In order to alleviate this computational cost, various \(O(N)\) complexity algorithms have been proposed \[3\]-\[4\]. These algorithms typically approximate the solution with an error that can be controlled by means of an adjustable parameter. They are typically iterative, and require linear algebra operations in each iteration \[5\]-\[6\]. For optimal performance however, these linear scaling codes have to be optimized at both the vector and thread level.

Optimizing data structure for improved parallelism is challenging and can be somewhat disruptive, therefore, we focus on optimizing at the thread level. One of the primary purposes of multi-core computer technology is latency hiding. However, at the cost of latency hiding is the inherent programmability challenges needed to be circumvented in order to achieve high performance gains in software applications, measured in terms of improvements in floating point operations (FLOPS) or run-time. Therefore, herein, we attempt to optimize the Basic Matrix Library (BML) software for performance gains in terms of run-time. BML is a collection of matrix data formats (for dense and sparse) and basic matrix operations designed to help electronic structures codes run efficiently on various platforms \[7\]-\[8\]-\[9\]. We focus on several strategies namely (i) Strength Reduction (SR), (ii) memory alignment (MA) to prevent cache contention, (iii) memory initialization with an understanding of first touch (FT) policy on Linux system, and (iv) thread affinity and binding (A&B) optimizations that works in conjunction with all the aforementioned techniques for optimal performance.

The rest of this manuscript is organized in the format delineated below. Section 4 expands on the optimizations techniques implemented in the BML \[9\] software. It is preceded by section 4.1 where we brief on the overall approach taken to optimizing the BML \[9\] software. This is followed by section 4.2 which discusses the target computer architectures used for evaluating the performance of the BML \[9\] code-base before and after optimization. sections 4.3 to 4.6 discusses and demonstrates in detail the optimization techniques introduced into the BML \[9\] software namely Strength Reduction (SR) \[10\]-\[18\], NUMA aware allocations to enforce data locality \[12\]-\[19\]-\[22\], Memory Alignment (MA) \[23\]-\[30\] for large arrays and appropriate thread affinity
and bindings (AB) \cite{31,35} to enhance multi-threaded performance, respectively. Sections 4.3 to 4.6 is also accompanied by sample implementation of in form of code snippets demonstrating the implementation of the aforementioned optimizations techniques. It also shows individual results of performance improvements. Section 5.2 combines all the aforementioned optimization techniques and introduces them into the BML software \cite{9}. Following that we generate several pseudo system matrices representing metals, semi conductors and soft matter ranging in size from 1000 to 32000 and evaluate the efficacy of these optimizations by measuring the performance differences of BML’s EllPACK matrix-matrix multiply algorithm before and after tuning \cite{9}. Section 5.3 evaluates the performance of ExaSP2, a proxy application for performing QMD calculations that relies on the BML \cite{9} software for its linear algebra computations. System matrices representing semi conductors and soft matter of size 32000 are evaluated for performance. Section 6 contains a discussion summary of the findings herein.

4 Methodology

4.1 Brief

Performance optimization of a large code-base can be a daunting task therefore, herein we introduce carefully designed subroutines, henceforth referred to as micro-kernels, that are representative of the methods in the un-optimized BML \cite{9} software. For the ease of evaluating the effects of the optimizing techniques introduced herein, we design the micro-kernels such that complex code behaviour e.g. cache trashing, branching and non-unit stride access are avoided though present in BML’s \cite{9} ELLPACK subroutine. At a latter time, we plan to address the effects of such complex behaviour as they impede on overall performance. We proceed by optimizing this micro-kernels in a step by step manner while being mindful of the compile time difference that may be introduced while building and linking the actual BML software \cite{9}. The target algorithm is memory bandwidth bound as it is a sparse matrix-matrix multiply algorithm with the ratio of FLOP to byte of data (n) requested from memory of O(n < 3).

4.2 Target Architecture:

The target multi-core platform experimented with herein are recent releases of Intel architectures namely Intel’s Sky-lake Gold, Sky-lake Platinum, Cascade Lake with and without support for Intel’s Optane™ DC persistent memory. Table 1 contains the specification details of the aforementioned architectures.

| Features                  | Skylake-Gold | Skylake-Platinum | Cascade Lake | Cascade Lake w/ Optane |
|---------------------------|--------------|------------------|--------------|------------------------|
| Model Number              | 6152         | 8176             | 6254         | 8260                   |
| Launch Date               | Q3’17        | Q3’17            | Q2’19        | Q2’19                  |
| Cores                     | 22           | 28               | 18           | 24                     |
| Threads Per Core          | 2            | 2                | 2            | 2                      |
| Base Frequency(GHz)       | 2.10         | 2.10             | 3.10         | 2.40                   |
| Turbo Frequency(GHz)      | 3.70         | 3.80             | 4.10         | 3.90                   |
| Cache L3(MB)              | 30.25        | 38.50            | 24.75        | 35.75                  |
| HBM (MB)                  | No           | No               | No           | No                     |
| TDP (W)                   | 140          | 165              | 200          | 165                    |

Table 1: Hardware specification for Intel architectures (Ark Intel).

4.3 Micro-Kernel Performance Evaluation - Strength Reduction:

Strength Reduction \cite{10,18}, is an optimization procedure, driven either via human intervention or software compiler, where by high latency (costly) operations are substituted with their lower latency (cheaper) counterpart while maintaining mathematical correctness. SR or approach approximate strength reduction (ASR) techniques can vary from very simple \cite{12,13} to more complex and involving substitutions \cite{10,11,14,18}. The need for SR tuning in the BML \cite{9} software, though not prevalent, is a low hanging fruit therefore we evaluate the performance difference between atypical occurrences of in-loop division with multiplications. Listing 1 is a code snippet of the micro-kernel atypical of the occurrences in the BML software \cite{9}. Listing 2
```c
#pragma omp parallel for simd
#pragma vector aligned
for(i=0; i < A->N; i++)
{
  A->index[i] = i
  A->nnn[i] += i
  A->value[i] = 16.0/RAND_MAX;
}
```

**Figure 1:** Micro-kernel without strength reduction representative of the subroutines in BML [9] before tuning.

```c
double INV_RAND_MAX = 1.0/RAND_MAX;
#pragma omp parallel for simd
#pragma vector aligned
for(i=0; i < A->N; i++)
{
  A->index[i] = i
  A->nnn[i] += i
  A->value[i] = 16.0 * INV_RAND_MAX;
}
```

**Figure 2:** Micro-kernel with strength reduction applied.

is a SR substitutions where we replace divisions within a loop with a single multiplication. Figure 3 is a run-time comparison of the benchmark (BHMK) vs. optimized (TUNED) micro-kernels for multiple dual socket Intel architectures using Intel 17 compiler. The performance of the optimized (TUNED) micro-kernel is approximately 2X across multiple thread sizes and varying architectures.

### 4.4 Micro-Kernel Performance Evaluation - NUMA Aware Data

Data locality in the BML [9] software is tuned for by ensuring that 1.) malloc-ed memory is initialized in a parallel region with the “First Touch” policy in mind and 2.) the affinity and binding settings for the initialization and computation loops for data used in multi-threaded regions are specified carefully such that computational data remains NUMA local. The “First Touch” policy with respect to memory allocation and memory page assignment on Linux systems, is associated with the physical location of memory (NUMA domain) at the point in which the actual memory addresses get modified (initialization). At the point of modification, the memory pages get assigned and further associated with that specific NUMA domain. Therefore, the First Touch policy determines memory page ownership [23]. Consideration for NUMA in order to avoid needless data movement (data locality) can be implemented to cater to different levels of parallelism which may include the SIMD, Thread and Node level. Several researchers [12, 19–22] have shown that the aforementioned approach improves the overall performance of computational algorithms by avoiding needless data movement. Prior to optimization for data locality, atypical linear algebra operations performed using the BML API required three steps namely 1.) memory allocation and initialization followed by 2.) the linear algebra calculation of interest and 3.) Memory de-allocation. The memory allocation and initialization step above is typically achieved in BML via two calls, one to `malloc()` and the other to `memset()`. This is also achieved via a single call to `calloc()`. The second step involving the Linear algebra operation of interest, e.g. a Matrix-Matrix multiply calculation, is typically comprised of a multi-threaded loop in a parallel region written using the OpenMP paradigm. With the First Touch policy in mind, step one and two are in conflict given that they are performed in a serial and parallel region, respectively. The first step is a serial operation with an associated performance penalty as the memory pages become associated with the specific NUMA domain they were first touched. Listing 4 is a code snippet of the micro-kernel atypical of the occurrences in the BML software. Listing 5 is a NUMA aware data initialization that ensures data locality in the computational loop by first touching data in a parallel region (lines 7-10) a opposed to (listing 4 lines 7-9) using `memset()` to initially modify malloc-ed data. Figure 13 is a pictorial illustration of a simplified modern multi-core computer showing computational cores and memories (RAM) associated with two NUMA domains. NUMA domain zero (core:0 and Memory:0) and one (core:1 and Memory:1) have an associate compute core and memory colored in blue and red respectively. To minimizes obscurity, we simplified the
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Figure 3: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) micro-kernel for SR for Cascade Lake (Top-Left), Sky-Lake Gold (Top-Right), Sky-Lake Platinum (Bottom-Left) and Cascade Lake with Intel Optane Technology (Bottom-Right).

physical description of each NUMA domain (0 and 1) and further assume that each core is actually multiple cores each with multiple levels of associated cache hierarchy and bandwidth infrastructure. The blue banks of memory located on NUMA:0 (red) represent data initialized on Memory:0 that potentially get moved to NUMA:1 (blue) during computation. This movement leads to additional performance penalty (higher latency) when performing computation on non-local data. This needles computational expense may also lead to cross NUMA domain cache conflict. Figure 7 shows a snap-shot of the preferred association of data and computational core in a compute loop. A completely disjoint subset of data associated with distinct NUMA domains is ideal, though in practice may require careful software design. Figure 8 is run-time comparison of the benchmark (BHMK) vs. optimized (TUNED) micro-kernels for multiple dual socket Intel architectures using Intel 17 compiler. The performance of the optimized (TUNED) micro-kernel is at best 3X for high thread counts and 2X on average on all architectures. In conjunction with NUMA aware allocations is the careful specification of thread affinity and binding to ensure thread placement is consistent with data location, in addition, the specified number of threads per core is consistent with the arithmetic intensity of the application under consideration, and finally that threads migration is avoided. Others authors [37–42] have demonstrated the challenges associated with non-locality of data and have proposed several solutions.

4.5 Micro-Kernel Performance Evaluation - Memory Alignment:

The application of memory alignment, as demonstrated by [23–30], is primarily for the purpose of preventing cache contention on multi-core computer hardware. Cache contention on multi-core hardware occurs when multiple hardware threads attempt to use the same line of cache. Figure 9 is an illustration of a simplified modern multi-core computer architecture containing four cores and showing two cache lines belonging to

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1 // Data Allocation
2 A->nnz = (int *) malloc(sizeof(int) *N);
3 A->index = (int *) malloc(sizeof(int) *N*M);
4 A->value = (double *) malloc(sizeof(double)*N*M);

6 // Non-NUMA Aware: Initialization
7 memset(A->nnz, 0, A->N*sizeof(int));
8 memset(A->index, 0, A->N*A->M*sizeof(int));
9 memset(A->value, 0.0, A->N*A->M*sizeof(double));

11 // Computational Loop
12 #pragma omp parallel for simd
13 #pragma vector aligned
14 for(i=0; i < A->N; i++)
15 compute(A);

Figure 4: Micro-kernel without consideration for data locality representative of the subroutines in BML [9] before tuning.

1 // Data Allocation
2 A->nnz = (int *) malloc(sizeof(int) *N);
3 A->index = (int *) malloc(sizeof(int) *N*M);
4 A->value = (double *) malloc(sizeof(double)*N*M);

6 // NUMA Aware: Initialization:
7 #pragma omp parallel for simd
8 #pragma vector aligned
9 for(i=0; i < A->N*A->M; i++)
10 initialize(A);

12 // Computational Loop
13 #pragma omp parallel for simd
14 #pragma vector aligned
15 for(i=0; i < A->N; i++)
16 compute(A);

Figure 5: Micro-kernel with consideration for data locality representative of the subroutines in BML [9] after tuning.

core:2 (purple) and core:3 (blue). Listing 10 is a code snippet of the micro-kernel atypical of the occurrences of memory allocation in the BML software. Listing 11 is a code snippet of the micro-kernel reflecting memory alignment that ensures minimal cache contention in the computational loop. Listing 11 shows aligned memory allocations using Intel compiler [23] (lines 2-4), hinting the compiler (lines 11-13) and a complementary aligned memory de-allocation (lines 18-20). A similar API that allows for aligned memory allocation is available with the GCC compiler [43]. Figure 12 is comparison of the run-time of the benchmark (BHMK) vs. optimized (TUNED) micro-kernels for multiple dual socket Intel architectures using Intel 17 compiler. The performance of the optimized (TUNED) micro-kernel is at best 11X for high thread counts and 5X on average across all architectures.

4.6 Micro-Kernel Performance Evaluation - Thread Binding and Affinity:

The purpose of rectifying the previously utilized thread binding and affinity settings used while performing linear algebra computations in BML [9] is to ensure that sub-optimal hardware utilization is prevented. Two known issues that degrade performance when using multi-core computers are 1.) thread migration and 2.) the utilization of non-equivalent threads during simulation. Thread migration is a process whereby operational threads migrate or move from core to core during simulations. This behaviour affects the repeatably during performance testing or bench-marking. Non-equivalent thread utilization is a scenario whereby operational threads do not have the same associated resources (L1, L2 or L3/LLC cache). This also
Figure 6: Illustration of modern multi-core architectures with multiple NUMA domains. Showing the effect of programming without considerations for “First Touch” policies on Linux systems. During simulation data present on NUMA:0 is fetched from NUMA:1.

Table 2: Best practice guidelines for configuring the affinity and binding setting depending on predominant arithmetic intensity using Intel’s [31–34] and OpenMP’s [31,32] API.

| Intel’s API: | OpenMP’s API: |
|--------------|---------------|
| **Arithmetic-Intensity** | **Compute Bound** |
| | All HW Threads |
| | “compact” |
| **Memory Bound** | All HW Threads |
| | “scatter” |
| **Migration Control**: set KMP_AFFINITY & KMP_HW_SUBSET | **Migration Control**: set OMP_PROC_BIND=true, OMP_NUM_THREADS & OMP_PLACES=cores |

affects repeatably during performance testing or bench-marking. It occurs as a result of a lack of specificity in the environment variables that control the binding and affinity of thread to hardware core(s) and/or socket(s). Preventing thread migration and appropriately specifying the correct thread binding and affinity using Intel’s API [31–34], requires setting two environment variables namely KMP_AFFINITY and KMP_HW_SUBSET. KMP_AFFINITY controls the thread placement which is highly dependent on the predominant arithmetic intensity (AI) of the application. Figure 13 is a pictorial representation of a thread placement specified as “scatter”. In addition, setting both environment variable prevent thread migration. KMP_HW_SUBSET determines the number of active threads and is set in the following format \(<#1>s, #2t, #3c\). c,t,s stand for cores per socket, threads per core, and number of active sockets, respectively. As an example, for a dual socket hardware with twenty-four cores and two hardware threads per core, KMP_HW_SUBSET set to 1t, 2s, 24c implies that forty-eight threads are operational on that node at one thread per core. Similarly, 2s, 2t, 24c implies that forty-eight threads are operational on each socket with a total of ninety-six total threads (two threads per core). Table 2 shows the best practice guidelines for configuring the affinity and binding of an application depending on the procedure with the dominant AI using Intel and OpenMP API.
Figure 7: Illustration of modern multi-core architectures with multiple NUMA domains. Showing the effect of programming with considerations for “First Touch” policies on Linux systems. During simulation data present on NUMA:0 is fetched from NUMA:0 and vice-versa.

5 Results

5.1 Brief

In order to demonstrate the viability of the aforementioned optimizations we proceed following the three steps delineated below. First, we generate chemically relevant system matrices following the techniques discussed in section 5.2 representing Metals, Semi Conductors and Soft Matter. Second, we evaluate the performance of BML ELLPACK matrix-matrix multiply algorithm for each system. Third, in order to demonstrate the viability of the aforementioned optimizations in a full simulation, we use ExaSP2, a spectral projection proxy application [44] for carrying out QMD computations. Following that, we establish a benchmark run-time for ExaSP2 to determine signature of the SP2-Basic algorithm which will inform on the condition in which the best performance gains in run-time is achieved. After establishing the representative/dominant AI, we compare the performance of the BHMK to that of the TUNED for those specific cases.

5.2 On the Generation of Model Hamiltonian System Matrices

Chemically relevant system matrices typically fall under the following categories namely 1.) Metals, 2.) Semi Conductors or 3.) Soft Matter. Figure 14 is a schematic representation of the model Hamiltonian matrices. These model systems are constructed by coupling arrays of two-level systems with A and B as atomic type of orbitals. Given that, A and B orbitals have onsite energies $\epsilon_A$ and $\epsilon_B$, respectively. A coupling between the same type of orbital, that is, comprising of only A type or B type, is given by either $\delta_{A,A}$ or $\delta_{B,B}$. Similarly, a coupling of elements between different orbitals, that is A and B, is given by $\delta_{A,B}$. All couplings between orbitals are modulated by an exponential dumping factor computed as $\exp(k|j - i|)$, where $k$ is the decaying constant, and $i$ and $j$ are the positions of both orbitals. All the couplings and onsite energies are in units of electron Volts(eV). We also introduced a randomization parameter that adds noise to couplings and onsite energies. This noise is introduced as param$(1 + r \times \text{RAND})$, where RAND is a random number chosen between -1 and 1 and param represents any of the coupling or onsite energies involved. A module that enables the generation of these Hamiltonian system matrix has been recently added to the PROGRESS [45] library. Figure 15 is a plot of the total DOS computed out of different model Hamiltonian matrices. The Fermi Level of the system is set to be 0.0 eV. System matrices representing Metals were generated by setting:

$$\delta_{A,A} = -1.0, \quad \delta_{B,B} = -1, \quad k = -0.01,$$
and the rest of the parameters to 0.0, resulting in a sparsity of 0.98%. For system matrices representing Semi Conductors, the parameters set to:

$$\delta_{B_iB_j} = -1.0, \quad \delta_{AB} = -2.0, \quad k = -0.01,$$

and the rest of the parameters to 0.0, resulting in a sparsity of 94% sparse. Soft Matter systems matrices were generated by setting:

$$\delta_{B_iB_j} = -1.0, \quad \delta_{AB} = -1.0, \quad \epsilon_A = -10.0, \quad k = -0.1, \quad r = 1.0,$$

resulting in a sparsity of 82% sparse. Figure 16 is a matrix plot using the BML Ellpack format for Metals, Semi Conductors and Soft Matter.

5.3 Performance Evaluation using System Matrices

Figure 16 is a matrix plot of three systems namely metals, semi conductors and soft matter. It serves as a visual representation of the density of each system: with metal being the most dense. Figure 17, 18 and 19 show the performance of the benchmark (BHMK) vs. optimized (TUNED) BML matrix-matrix multiply algorithm using the ELLPACK format for the aforementioned systems on four different architectures. Matrix-matrix multiplications with metals (Figure 17), shows a 15% to 30% improvement on average in the optimized version of the BML library for larger matrix sizes on every architecture. Semi conductors (Figure 18), show excellent improvement in the optimized code for all matrix sizes experimented with. On average, the 32k matrices are improved by over 100 folds. Figure 19 (soft matter systems) shows similar improvements to that semi conductors. On average, the 32k matrices are improved by over 50 folds across all architectures.
Figure 9: An Illustration of the need for memory alignment on multi-core architectures. Showing contention between core:2 and core:3.

```c
// Allocating unaligned memory:
A->nnz = (int *) malloc(sizeof(int)*N);
A->index = (int *) malloc(sizeof(int)*N*M);
A->value = (double *) malloc(sizeof(double)*N*M);

// Computational loop:
#pragma omp parallel for
for(i=0; i < A->N; i++)
compute(A);

// De-allocation of unaligned memory:
free(A->nnz);
free(A->index);
free(A->value);
```

Figure 10: Memory allocation in BML software.

```c
// Allocating aligned memory:
A->nnz = (int *) _mm_malloc(sizeof(int)*A->N,64);
A->index = (int *) _mm_malloc(sizeof(int)*A->N*A->M,64);
A->value = (double *) _mm_malloc(sizeof(double)*A->N*A->M,64);

// Computational loop:
#pragma omp parallel for simd
#pragma vector aligned
for(i=0; i < A->N; i++)
{
    __assume_aligned(A->nnz,64);
    __assume_aligned(A->index,64);
    __assume_aligned(A->value,64);
    compute(A);
}

// De-allocation of aligned memory:
_mm_free(A->nnz);
_mm_free(A->index);
_mm_free(A->value);
```

Figure 11: Memory allocation with memory alignment in BML software.
5.4 Performance Evaluation using an ExaSP2 Application:

The procedures that make up the SP2-Basic algorithm can be decomposed into two types namely the initialization and SP2 calculation step. The initialization step involves reading in the Hamiltonian (Read Hamiltonian) matrix and other miscellaneous initialization sub-steps (Init. Misc.). The SP2 calculation step involves a matrix-matrix multiplication (SP2 Loop X2) and a matrix norm (SP2 Loop Norm) calculation. All other steps within the SP2 calculation are categories under (SP2 Loop Misc.). For this exercise, only Semi Conductor and Soft Matter where experimented with as they are appropriate for an SP2 calculation. The ELLPACK matrix format and corresponding algorithms were used to represent both systems. In addition, since the overall performance of each system has shown repeat-ability across all four architectures, only Intel Cascade Lake and Skylake Platinum were used here. Figure 20, 21, 22 and 23 is a comparison of the benchmark (BHMK) vs. optimized (TUNED) ExaSP2 for both systems. On Intel Cascade Lake (figure 20 and 21), both systems show an improvement in run-time by over four folds (4x) while other subroutines vary from four (4x) to twelve (12x) folds.

6 Conclusions

We evaluated the viability of several optimization strategies namely 1.) Strength Reduction 2.) Memory Alignment 3.) NUMA aware allocations and all incorporation with the appropriate thread affinity and binding. Initially, we tested the viability of these performance tuning techniques in micro-kernels by comparing the run-time before and after optimization for several target architectures. For SR optimizations, the optimized
Figure 13: An illustration of a modern dual socket multi-core architecture. Showing a coordination of memory initialization with thread binding and affinity with considerations for “First Touch” policies on Linux systems.

Figure 14: Two-level system model Hamiltonian used to generate representative Hamiltonian matrices for bench-marking purposes. The model has the following parameters: Four coupling parameters, four onsite energies, a decaying exponential parameter, and a randomization factor.
Figure 15: Total DOS computed out of different model Hamiltonian matrices. The Fermi Level of the system is set to be 0.0 eV. a) Metals can be generated by setting $\delta_{A_iA_j} = -1.0$, $\delta_{B_iB_j} = -1$, $k = -0.01$, and the rest of the parameters to 0.0. Matrices of this type are about 0.98% sparse. b) Semiconductors can be generated by setting $\delta_{B_iB_j} = -1.0$ and $\delta_{AB} = -2.0$, $k = -0.01$ and the rest of the parameters to 0.0. Matrices of this type are about 94% sparse. c) Soft matter systems can be generated by setting $\delta_{B_iB_j} = -1.0$ and $\delta_{AB} = -1.0$, $\epsilon_A = -10.0$, $k = -0.1$ and $r = 1.0$. Matrices of this type are about 82% sparse.

Figure 16: Matrix plot of Metals (Top Left), Semi Conductors (Top Right) and Soft Matter (Bottom) generated using the techniques discussed.
Figure 17: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) BML ELLPACK matrix-matrix multiply for Metals computed on Cascade Lake (Top-Left), Sky-Lake Gold (Top-Right), Sky-Lake Platinum (Bottom-Left) and Cascade Lake with Intel Optane Technology (Bottom-Right).

micro-kernel showed approximately 2X across multiple thread sizes and varying architectures. For NUMA aware data initialization that ensures data locality, the performance of the optimized micro-kernel is at best 3X for high thread counts and 2X on average on all architectures. Memory alignment optimizations, the optimized micro-kernel is at best 11X for high thread counts and 5X on average across all architectures. The optimizations were used in conjunction with an appropriate thread binding and affinity settings such that, two well known issues that degrade performance when using multi-core computers are avoided.

We followed this up by generating chemically relevant system matrices representing Metals, Semi Conductors and Soft Matter evaluate the performance of BML ELLPACK matrix-matrix multiply algorithm for each system. The matrix-matrix multiplications with metals showed a 15% to 30% improvement on average in the optimized version of the BML library for larger matrix sizes on every architecture. Semi conductors, showed an excellent improvement in the optimized code for all matrix sizes experimented with. On average, the 32k matrices were improved by over 100 folds. Soft matter systems showed similar improvements to that semi conductors where on average, the 32k matrices are improved by over 50 folds across all architectures. Finally, we evaluated the performance of these optimizations using a QMD proxy application, where the ELLPACK matrix format and corresponding algorithms were used to represent both Soft Matter and Semiconductors. Both systems on Intel Cascade Lake and Skylake Platinum showed an improvement in run-time by over four folds (4x). Other relevant subroutines within ExaSP2 showed improvements varying from four (4x) to twelve (12x) folds.
Figure 18: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) BML EllPACK matrix-matrix multiply for Semi Conductor computed on Cascade Lake (Top-Left), Sky-Lake Gold (Top-Right), Sky-Lake Platinum (Bottom-Left) and Cascade Lake with Intel Optane Technology (Bottom-Right).
Figure 19: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) BML EllPACK matrix-matrix multiply for Soft Matter computed on Cascade Lake (Top-Left), Sky-Lake Gold (Top-Right), Sky-Lake Platinum (Bottom-Left) and Cascade Lake with Intel Optane Technology (Bottom-Right).

Figure 20: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) ExaSP2 for Semi Conductor simulated on Intel’s Cascade Lake. Showing run-time of individual subroutines.
Figure 21: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) ExaSP2 for Soft Matter simulated on Intel’s Cascade Lake. Showing run-time of individual subroutines.

Figure 22: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) ExaSP2 for Semi Conductor simulated on Intel’s Skylake Platinum. Showing run-time of individual subroutines.
Figure 23: Performance in run-time for the benchmark (BHMK) vs. optimized (TUNED) ExaSP2 for Soft Matter simulated on Intel’s Skylake Platinum. Showing run-time of individual subroutines.
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