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PV Based Sliding Mode Controller for Voltage Regulation in Positive Output Elementary Parallel Connected Boost Converter

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Abstract

The necessity of higher current and providing a back-up when one unit fails, demands the parallel operation of dc-dc converters. One of the problems of the parallel operating power converters is to regulate the output voltage and equalize the output currents of modules. This paper provides the design of PV based sliding mode controller (SMC) for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviors are studied for the designed SMC for disturbances viz. line voltage variations of converters, load variation and other circuit components changes. The performance evaluation is done in hardware and MATLAB-Simulink tool, finally the results are compared with conventional proportional-integral (PI) controller.

Keywords
Parallel Connected Boost Converter, PV, Sliding Mode Controller, PI Controller, Voltage Regulation

1. Introduction

Solar power is a renewable energy source that may replace fossil fuel dependent energy sources. However, for that to happen, solar power cost per kilowatt-hour has to be competitive with fossil fuel energy sources. Currently, solar panels are not very efficient; it has 12% - 20% efficiency to convert sunlight to electrical power. The efficiency can drop further due to other factors such as solar panel temperature and load conditions. In order

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to maximize the power derived from the solar panel, it is important to operate the panel at its optimal power point. To achieve this, a type of charge controller called a Maximum Power Point Tracker should be designed and implemented.

The MATLAB/PSPICE model of the PV module is developed [1]-[4] to study the effect of temperature and insolation on the performance of the PV module. MATLAB-based modelling and simulation scheme which is suitable for studying the I-V and P-V characteristics of a PV array under a non-uniform insolation due to partial shading [5] is proposed. The mathematical model of solar PV module is useful for the computer simulation. The power electronics interface is connected between a solar panel and a load or battery bus, is a pulse width modulated (PWM) DC-DC converter or their derived circuits is used to extract maximum power from solar PV panel [6]. The main drawback of PV systems is that the output voltage of PV panels is highly dependents on solar irradiance and ambient temperature. Therefore PV panels outputs are cannot connect directly to the load. To improve this, a DC-DC boost converter is required to interface between PV panels and loads [7]. The boost converter is fixing the output voltage of the PV system. Converter receives the variable input voltage which is the output of PV panels and gives up constant output voltage.

DC-DC step-up converters are widely used in computer hardware and industrial applications, such as computer peripheral power supplies, car auxiliary power supplies, servo-motors drives, and medical equipment [8][9]. In recent years, the DC-DC conversion technique has been greatly developed. The main objective is to reach a high efficiency, high power density and cheap topology in a simple structure. Generally, in power supply applications, DC-DC converter modules are operated in parallel due to the reasons like higher power demand, improving the power system reliability and the operational redundancy (N+1 redundancy—N is the number of units needed to power the load, plus 1 as the back-up) [10]. There is also a trend in manufacturing the standard power converter modules which can be connected in parallel to cover a wide power range. This significantly reduces the costs of development and existing systems can be extended easily. The parallel operation offers the advantages such as expandability of output power, reliability and ease of maintenance. The main challenges in the parallel operations are output voltage regulation and load current sharing at different disturbances.

The average generalized PI output feedback regulator as a steer for defining the switched implementation of the average sliding mode features through a sigma-delta modulation strategy has been addressed [11]. The control loop of a parallel connection of two non-identical paralleled positive output elementary super lift Luo converters using the SMC theory for current distribution control in continuous conduction mode [12]. A droop method has been proposed for the converter parallel operation, which adaptively controls the reference voltage of each module. The scheme improves the output voltage regulation and the current sharing of the conventional droop method [13]. A robust controller for parallel dc-dc buck converters has been coined by combining the concepts of integral-variable-structure and multiple-sliding-surface control [6]. Grid connected solar PV system with SEPIC converter compared with parallel boost converter based MPPT [14]. Nonlinear back-stepping adaptive controller has been proposed for the design of parallel DC-DC buck converters with uncertainties of load and power disturbance. The relationship between the control elements and circuit parameters has been determined by simulation analysis. The relationship between current sharing difference and circulating current for two parallel connected dc-dc converters has been investigated [15]. Although there may exist a trade-off between current sharing difference and voltage regulation, the proposed droop index algorithm gives better performance and low voltage regulation. The detailed analysis and design procedure are explained for two dc-dc boost converters connected in parallel. The effectiveness of proposed method is verified using MATLAB simulation.

The uncertainties in the source, load and other circuit parameters make the parallel operation of DC-DC converters challenging. This paper provides the design of sliding mode controller (SMC) for parallel operated DC-DC boost converter. The output voltage regulation and load sharing behaviors are studied for the designed SMC for disturbances viz. line voltage variations of converters, load variation and other circuit components’ changes. The performance of the developed controller in parallel boost converter is validated at the different working conditions through the simulation in the comparison with PI controller.

2. Matlab Model of L1235-37W Solar PV Module

A solar cell is the building block of a solar panel. A photovoltaic module is formed by connecting many solar cells in series and parallel. Considering only a single solar cell; it can be modelled by utilizing a current source, a diode and two resistors. This model is known as a single diode model of solar cell. Two diode models are also
available but only single diode model is considered here [1] [3] [4] [16]-[18]. The equivalent circuit of PV module is shown in Figure 1.

From Figure 1, the current equation is given by

\[ I_{sc} = I_D + I_{pv} + \left( \frac{V_D}{R_p} \right) \]

\[ V_{pv} = V_D - \left( I_{pv} * R_p \right) \]

(1)
(2)

where diode current is,

\[ I_d = I_s + \left( e^{\frac{V_D}{nT}} - 1 \right) \]

The load current is given by

\[ I = I_{sc} - I_{pv} \left( \exp \left( \frac{q(V_{pv} + RI)}{NK} \right) - 1 \right) - \frac{V_{pv} + RI}{R_p} \]

(3)

In this equation \( I_{pv} \) denotes the photo voltaic current, \( I_{sc} \) is the diode reverse saturation current, \( q \) is the electron charge, \( V_{pv} \) is the diode across the voltage, \( K \) is the Boltzmann’s constant, \( T \) is the temperature of the junction, \( N \) is the diode identity factor, \( R \) and \( R_p \) are the series and shunt resistors of the solar cell. The complete physics behaviour of the PV cell is in relation with \( I_{sc}, I_{pv}, R \) and \( R_p \) from one hand and with two environmental parameters as the temperature and solar radiation from the other hand. The model is developed in MaLab/simulink based on the above equations. For a given radiation, temperature, \( R \) and \( R_p \), the I-V and P-V curves are generated [19]. Based on the electrical Equations ((1) and (2)), the solar PV module is modelled in MATLAB shown in Figure 2. Which is used to enhance the understanding and predict the V-I characteristics and to analyze the effect of temperature and irradiation variation. If irradiance increases, the fluctuation of the open-circuit voltage is very small. But the short circuit current has sharp fluctuations with respect to irradiance. However, for a rising operating temperature, the open-circuit voltage is decreased in a Non-linear fashion [4].

The V-I characteristics are validated experimentally in the L1235-37Wp solar module shown in Figure 3. Table 1 shows the technical specifications of L 235-37W solar module under test. Figure 4 shows the V-I characteristics is based on the experimental results under irradiation (G) = 1000 W/m², temperature = 25°C.

The PV model was simulated in Matlab/Simulink. The above model includes two subsystems: one that calculates the PV cell photocurrent which depends on the radiation and the temperature according to Equation (3) [20].
Table 1. Specifications of L1235-37W single solar PV panel.

| Specification             | Value          |
|---------------------------|----------------|
| Short circuit current (I_{sc}) | 2.5 A         |
| Voltage at MPP (V_{mpp})   | 16.4 V         |
| Current at MPP (I_{mpp})   | 2.25 A         |
| Open circuit voltage (V_{oc}) | 21 V       |
| Length                    | 645 mm         |
| Width                     | 530 mm         |
| Depth                     | 34 mm          |
| Weight                    | 4 kg           |
| Maximum power (P_{max})   | 37 W           |

3. Principle of Operation and SMC

Variable structure control (VSC) with sliding mode, or sliding-mode control (SMC), is one of the effective non-linear robust control approaches since it provides system dynamics with an invariance property to uncertainties once the system dynamics are controlled in the sliding mode [21]. For the non-linear system like positive output

\[ I_{ph} = \left[ I_{sc} + K_i (T - 298) \right] \frac{\beta}{1000} \]  (4)

where \( K_i = 0.0017 \ \text{A/}^\circ\text{C} \) is the cell’s short circuit current temperature coefficient and \( \beta \) is the solar radiation (W/m²).
elementary cascade boost converter, the sliding mode controller is a more suitable approach. Sliding mode control has been presented as a good alternative to the control of switching power converters [22] [23]. The main advantage over the classical control schemes is its insusceptibility to plant parameter variations that leads to invariant dynamics and steady-state response in the ideal case. In this paper, a sliding mode controller for the positive output elementary cascade boost converter is proposed.

3.1. System Description

The Positive Output Elementary Parallel Connected Boost Converter (POEPCBC) is shown in Figure 5. It includes dc supply voltage $V_{in}$, capacitor $C$, input inductor $L$, power switch (n-channel) $S$, freewheeling diode $D$, load resistance $R$. The principle of the sliding mode controller is to make the capacitor voltage $V_C$ follows as faithfully as possible a capacitor voltage reference.

In the description of the converter operation, it is assumed that all the components are ideal and that the proposed converter operates in a continuous conduction mode. Figure 6 shows equivalent circuit while Figure 7 and Figure 8 represent two topological modes for a one cycle period of operation. When the switch $S$ is closed in Figure 7, inductor current $i_L$ rises quite linearly, diode current $D$ is reverse polarized, and capacitor $C$ supplies the energy to output stage. Once the switch $S$ is open in Figure 8, inductor current $i_L$ is forced to flow through the diode $D$, capacitor $C$ and load. The current $i_L$ decrease while capacitor is recharged.

The ripple inductor current is

$$\Delta i_L = \frac{V_{in}}{L} dT = \frac{V_{in} - V_D}{L} (1 - d) T$$

Voltage transfer gain

$$G = \frac{V_C}{V_{in}} = \frac{1}{1 - d}$$

$$C = \frac{V_C}{V_{in}} = \frac{1}{1 - d}$$

Figure 5. The positive output elementary parallel connected boost converter controlled by sliding mode.
3.2. Sliding Mode Controller

When good transient response of the output voltage is needed, a sliding surface equation in the state space, expressed by a linear combination of state-variable errors $e_i$ (defined by difference to the references variables), can be given by
\[ S = (i_L, V_C) = K_1 \varepsilon_1 + K_2 \varepsilon_2 \]  
\[ (10) \]

where coefficients \( K_1 \) and \( K_2 \) are proper gains, \( \varepsilon_1 \) is the feedback current error and \( \varepsilon_2 \) is the feedback voltage error, or

\[ \varepsilon_1 = i_L - i_{L_{\text{ref}}} \]  
\[ (11) \]

\[ \varepsilon_2 = V_C - V_{C_{\text{ref}}} \]  
\[ (12) \]

By substituting (7) and (8) in (6), one obtains

\[ S = (i_L, V_C) = K_1 (i_L - i_{L_{\text{ref}}}) + K_2 (V_C - V_{C_{\text{ref}}}) \]  
\[ (13) \]

The signal \( S(i_L, V_C) \), obtained by the implementation of (13) and applied to a simple circuit (hysteresis comparator), can generate the pulses to supply the power semiconductor drives. The resulting control scheme is shown in Figure 9. Status of the switch \( \gamma \) is controlled by hysteresis block \( H \), which maintains the variables \( S(i_L, V_C) \) near zero. The system response is determined by the circuit parameters and coefficients \( K_1 \) and \( K_2 \). With a proper selection of these coefficients in any operating condition, high control robustness, stability, and fast response can be achieved.

In theory, the sliding mode control requires sensing of all state variables and generation of suitable references for each of them. However, the inductor current reference is difficult to evaluate since it generally depends on load power demand supply voltage, and load voltage. To overcome this problem, in implementation the state variable error for the inductor current \( (i_L - i_{L_{\text{ref}}}) \) can be obtained from feedback variable \( i_L \) by means of a high-pass filter in the assumption that their low-frequency component is automatically adapted to actual converter operation. Thus, only the high-frequency component of this variable is needed for the control. This high pass filter increases the system order and can heavily alter the converter dynamics. In order to avoid this problem, the cut-off frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple at the switching frequency, but high enough to allow a fast converter response.

![Figure 9. Sliding mode controller scheme.](image-url)
4. Design Calculation

In the design of the controller, Ideal power switches; Power supply free of dc ripple and converter operating at high-switching frequency are assumed. The controller design describe the selection of controller parameters, switching frequency, duty cycle, inductor current, voltage capacitor [23]. The main purpose of this section is to use to calculate the proposed converter components value, controller parameters and simulation studies. The validation of the system performance is done for three regions viz. line variation, load variation and components variations. Simulations have been performed on the POEPCBC circuit with parameters listed in Table 2.

The performance of proposed method is evaluated using Matlab/Simulink. The signal $S(i_L, V_C)$, obtained by the simulation implementation of (13) and applied to a simple circuit (hysteresis comparator), can generate the pulses to supply the power semiconductor drives. Status of the switch $\gamma$ is controlled by hysteresis block $H$, which maintains the variables $S(i_L, V_C)$ near zero.

5. Design of PI Controller

A PI controller is chosen for providing the better output voltage regulation in POEPCBC. The DC output voltage is sensed and compared with reference output voltage and error signal is obtained. This error signal is processed by the PI controller to maintain the output voltage constant. The PI parameters, Proportional gain ($K_p$) and Integral times ($T_i$) are obtained by using Zeigler-Nichols tuning method. The Transfer Function (TF) model of equation is obtained from the state space average model of the following equation using MATLAB. Then

$$\text{TF} = \frac{-7.958e^{-12}s^2 + 1.667e^8s + 1.389e^{15}}{s^3 + 666.7s^2 + 8.333e^9}$$

(14)

For simplifying the design aspect, the term $-7.958e^{-12}s^2$ in the numerator of the TF model is very small and hence it can be neglected. Therefore, the new TF becomes

$$\text{TF} = \frac{1.667e^8s + 1.389e^{15}}{s^3 + 666.7s^2 + 8.333e^9}$$

(15)

The characteristic equation with proportional control is expressed by

$$s^3 + 666.7s^2 + s\left(8.333e^7 + K*1.667e^8\right) + K*1.389e^{12} = 0$$

(16)

The Routh-array of above equation is

- $s_3$: $1\left(8.333e^7 + K*1.667e^8\right)$
- $s_2$: $666.7\left(K*1.389e^{12}\right)$
- $s_1$: $-8.333e^7 + 2247116569\left(K\right)$
- $s_0$: $K*1.389e^{12}$

### Table 2. Parameters of chosen POEPCBC.

| Parameters Name           | Value   |
|---------------------------|---------|
| Input Voltage ($V_{in}$)  | 12 V    |
| Output Voltage ($V_o = V_C$) | 36 V    |
| Inductor ($L$)            | 100 μH  |
| Capacitor ($C$)           | 30 μF   |
| Nominal Switching Frequency ($F_s$) | 100 kHz |
| Determination the Ratio $K_o/L$ | 7453    |
| Determination the Ratio $K_o/C$     | 248,433 |
| Co-efficient $K_1$        | 0.745   |
| Co-efficient $K_2$        | 7.45    |
| Load Resistance ($R$)     | 50 Ω    |
| Output Power ($P_o$)      | 25.92 W |
| Input Power ($P_i$)       | 27.684 W|
| Input Current ($I_o$)     | 2.307 A |
| Efficiency $\eta$         | 93.62%  |
from this Routh-array technique, the range of $K$ for stability is $\left( -8.333e^{-7} + 2247116969\times K \right) > 0$, $K > 0.037$. $0 < K < 0.037$ So, the ultimate critical gain $K_{cr} = 0.037$ and their corresponding $\omega_n = 210447$ rad/sec and $P_{cr} = 2\times{\pi}\omega_n = 2.9856e^{-3}$. After turning the controller using this method, the POEPCBC is providing a sustained oscillation with ultimate gain for stability and can be found by $K_{cr} = 0.02$ and their corresponding ultimate period $P_{cr} = 0.0012$ s. Using this method the value of $K_p = K_{cr}/2 = 0.01205$ and integral time $T_i = P_{cr}/0.2 = 0.0133$ s are determined [24].

6. Simulation Results and Discussions

The main purpose of this section is to discuss the simulation studies of the POEPCBC with SMC. Here the PI controller is used for comparison with the designed controller. The validation of the system performance is done for different conditions viz. the start-up transient, line variation, steady state and component variations. Simulations are performed on the POEPCBC circuits with the specifications are listed in Table 2.

Figure 10 and Figure 11 show the average output currents and the gate pulse of paralleled modules without a controller for different input voltages ($V_{in1} = 12$ V and $V_{in2} = 15$ V). It can be seen that the current share of the modules are unequal. Table 3 lists the simulated results of the average output current/voltage for each of the modules and the POEPCBC without controllers for various input voltages and load resistances. From Table 3, it can be clearly seen that the output voltage regulation and the output current distributions of each of the modules and the POEPCBC are unequal.

![Figure 10](image1.png)  
**Figure 10.** Average output currents without a controller.

![Figure 11](image2.png)  
**Figure 11.** Gate pulse of paralleled modules without a controller.
6.1. Start-Up Transients

Figure 12 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9 V, 12 V and 15 V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.008 s for $V_{in} = 15$ V whereas for 12 V and 9 V there are negligible overshoots and a settling time of 0.01 s and 0.012 s for designed SMC, respectively. Figure 13 shows the dynamic behavior at start-up for the output voltage of paralleled module-1 for different input voltages viz. 9 V, 12 V and 15 V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.022 s for $V_{in} = 15$ V whereas for 12 V and 9 V there are negligible overshoots and a settling time of 0.025 s and 0.028 s respectively. Figure 14 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different input voltages viz. 9 V, 12 V and 15 V. It can be seen that the output voltage of the paralleled module-2 has a little overshoot and a settling time of 0.022 s for $V_{in} = 15$ V whereas for 12 V and 9 V there are negligible overshoots and a settling time of 0.025 s and 0.028 s respectively. The overshoot behavior imitates the conclusions of the previous cases. Figure 15 shows the dynamic behavior at start-up for the average output current of paralleled modules.

Figure 16 shows the dynamic behavior at start-up for the output voltage of paralleled modules for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output voltage of the paralleled modules has a slight overshoot and settling time of 0.012 s for $R = 60$ Ω, whereas the output voltage of the paralleled modules for $R = 50$ Ω and $R = 40$ Ω has a negligible overshoot and settling times of 0.013 s and 0.014 s with the designed SMC. Figure 17 shows the dynamic behavior at start-up for the average output current of paralleled module-1 for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output voltage of the paralleled module-1 for $R = 40$ Ω, $R = 50$ Ω and $R = 60$ Ω has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s with the designed controller.

Figure 18 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output current of the module-2 for

| Change in $V_{in}$ & $V_{sd}$ (V) | $V_{in}$ (V) | $V_{sd}$ (V) | $V_{o}$ (V) | $I_{1}$ (A) | $I_{2}$ (A) | $I_{O}$ (A) |
|----------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 9 V - 12 V                       | 33.92       | 33.92       | 33.92       | 0.040       | 0.645       | 0.685       |
| 12 V - 15 V                     | 47.04       | 47.04       | 47.04       | 0.063       | 0.802       | 0.865       |

| Resistance (Ω) | $V_{o}$ (V) | $V_{sd}$ (V) | $V_{o}$ (V) | $I_{1}$ (A) | $I_{2}$ (A) | $I_{O}$ (A) |
|----------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 40 Ω           | 34.42       | 34.42       | 34.42       | 2.414       | 1.041       | 3.455       |
| 50 Ω           | 36.85       | 36.85       | 36.85       | 0.308       | 0.428       | 0.736       |
| 60 Ω           | 36.92       | 36.92       | 36.92       | 0.315       | 0.300       | 0.615       |

Table 3. Performance of POEPCBC without controllers.
Figure 13. Response at start-up for average output current of POEPCBC 1.

Figure 14. Response at start-up for average output current of POEPCBC 2.

Figure 15. Response at start-up for average output current of POEPCBC.
Figure 16. Response at start-up for output voltage of paralleled modules.

Figure 17. Response at start-up for average output current of POEPCBC 1.

Figure 18. Response at start-up for average output current of POEPCBC 2.
$R = 40 \, \Omega$, $R = 50 \, \Omega$ and $R = 60 \, \Omega$ has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s with the designed SMC. Figure 19 shows the dynamic behavior at start-up for the average output current of paralleled module-2 for different load resistances like 40 $\Omega$, 50 $\Omega$ and 60 $\Omega$. It can be seen that the output current of the modules for $R = 40 \, \Omega$, $R = 50 \, \Omega$ and $R = 60 \, \Omega$ has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s with the designed SMC.

Table 4 lists the simulated results of the average output current and voltage of each of the modules and the POEPCBC with controllers for various input voltage and load resistances in the start-up region. From Table 4, it can be seen that the voltage regulation and the current distributions of each of the modules and the POEPCBC using the designed SMC show excellent performance in comparison with a conventional PI controller.

### 6.2. Line Variations

Figure 20 shows the response of the average output voltage of paralleled modules using both a PI controller and SMC for an input voltage step change from 12 V to 15 V (+30% line variations) at time $t = 0.1$ s. It can be seen that the output voltage of the paralleled modules using SMC has a maximum overshoot of 3.8 V and a settling time of 0.01 s, while the output voltage of the paralleled modules using a PI controller has a severely affected overshoot of 12 V and a long settling time of 0.02 s respectively. Figure 21 shows the response of the average output voltage of the SMC with paralleled modules using both a PI controller and SMC for an input voltage step change from 12 V to 9 V (−30% line variations) at time $t = 0.1$ s. It can be seen that the output voltage of the paralleled modules using the SMC has a maximum overshoot of 4 V and a settling time of 0.01 s, while the output

### Table 4. Voltage/Current profiles of POEPCBC for input voltages/load resistances with nominal input voltage/load in start-up region

| Line Variation 9 V - 15 V (Start-up Region) | Voltage Profile | SMC |
|-----------------------------------|----------------|-----|
|                                   | $V_o$ (V)      | $V_o$ (V) |
|                                   | PI Controller  | SMC  |
| $V_o$ (V)                         | 36.05          | 36.05 |
| $V_o$ (V)                         | 36.05          | 36.05 |
| $V_o$ (V)                         | 36.05          | 36.05 |
| $V_o$ (V)                         | 36             | 36    |
| $V_o$ (V)                         | 36             | 36    |
| $V_o$ (V)                         | 36             | 36    |

| Load Variation 40 $\Omega$ - 60 $\Omega$ (Start-up Region) | Current Profile | SMC |
|-------------------------------------------------------------|----------------|-----|
|                                                             | $I_1$ (A)      | $I_2$ (A) |
| $40 \, \Omega$                                              | 0.441          | 0.441   |
| $50 \, \Omega$                                              | 0.358          | 0.358   |
| $60 \, \Omega$                                              | 0.291          | 0.291   |
voltage of the paralleled modules using a PI controller has a maximum overshoot of 10 V and a long settling time of 0.02 s respectively.

6.3. Load Variations

Figure 22 shows the response of the output voltage of paralleled modules using both a PI controller and SMC for load step change from 50 Ω to 60 Ω (+20% load variations) at time = 0.1 s. Here the output voltage of the paralleled modules using SMC has a small overshoot of 1.8 V with a settling time of 0.01 s, while the output voltage of the paralleled modules using PI controller has a severely affected overshoot of 16 V and a settling time of 0.02 s respectively. Figure 23 shows the response of the output voltage of paralleled modules using both a PI controller and SMC for load step change from 50 Ω to 40 Ω (−20% load variations) at time = 0.1 s.

6.4. Steady State Regions

Figure 24 shows the instantaneous output voltage and the inductor current of paralleled modules in the steady state using SMC. It is evident from this figure that the output voltage ripple is very small, about 0.03 V and the peak to peak inductor ripple current is 0.32 A for an average switching frequency that is 100 kHz closer to the
Figure 22. Response of output voltage of paralleled modules (50 Ω and 60 Ω).

Figure 23. Response of output voltage of paralleled modules (50 Ω and 40 Ω).

Figure 24. Inductor current $i_L$ and output voltage in steady state region using SMC.
theoretical designed. Figure 25 shows the instantaneous output voltage of paralleled modules in the steady state using PI controller. It is evident from the figure that the output voltage ripple is little high about 0.025 V.

6.5. Circuit Components Variations

Figure 26 and Figure 27 represent the response of the output voltage and current of paralleled modules using both SMC and a PI controller for the variation of inductor L from 100 μH to 500 μH. It can be seen that the change does not influence the paralleled converters behavior due to the proficient design of the designed controller in comparison with a conventional PI controller.

An interesting result is illustrated in above Figure 28 and Figure 29. It shows the response of the output voltage and the current of the paralleled modules with both a PI controller and the proposed controller scheme for a variation in the capacitors values from 30 μF to 100 μF. It can be seen that the SMC is very successful in suppressing the effect of the capacitive variation except that a negligible output voltage ripple with a quick settling time and a proper current distribution in comparison with a conventional PI controller. In summary from Figure 28 and Figure 29, it is obviously specified that the simulated graphs of developed SMC has excellent performance of POEPCBC in comparison with a conventional PI controller during circuit component variation.
Figure 27. Performance of POEPCBC output current (100 μH to 500 μH).

Figure 28. Performance of POEPCBC output voltage (30 μF to 100 μF).

Figure 29. Performance of POEPCBC output current (30 μF to 100 μF).
7. Discussions on Experimental Results

The main purpose of this section is to discuss the experimental results of POEPCBC with the designed SMC. The verification of the model performance is completed for different conditions. The laboratory prototype model is performed on POEPCBC circuits with the same specification as the simulations.

The parameters are as follows:

- Q: IRFN 540 (MOSFET)
- D: FR306 (Diodes)
- C: 30 μF/100V (Electrolytic and plain polyester type)
- L: 100 μH/5A (Ferrite Core)

The parameters of the controller coefficients are: $K_1 = 0.667$, $K_2 = 0.217$ and $\delta = 0.5$ as calculated in the previous section. The designed SMC is implemented in an analog platform and its operation is as follows; the inductor current and the capacitor voltages $V_{c1}$ and $V_{c2}$ of the POEPCBC are sensed by using an LA 25-NP current sensor, resistances, capacitors and LM324 operational amplifiers, which are then compared with reference signals by using an LM324 operational amplifier that gives error signals. The inductor current error signal is further processed through a HPF (20 kHz) for the purpose of filtering out the low frequency component of the converter as the controller allows only high frequency signals. The output of the entire designed controller signals are summed and compared using an LM311 to generate the PWM. First time gate drive control signal of the generated gate signal is passed through the opt-isolator (MCT 2E) and the driver circuit (transistors SK100, 2N2222 and the resistance arrangement) and then to the MOSFET. In MOSFET there is an internal capacitor in the gate terminal. Therefore, the transistors (2N2222 and SK100) are used as a quick charging and discharging capacitor and also for amplification. The output of the driver is directly connected to the gate of the MOSFET (IRFN 540) through the resistance. Using SMC, the switching frequency of the gate pulse is varied to regulate the output current and the voltage and also to improve the dynamic performance of the POEPCBC.

7.1. Start-Up Region

Figure 30 shows the dynamic behavior in the start-up for output voltage in POEPCBC for different input voltages viz. 9 V, 12 V and 15 V. It can be seen that output voltage of POEPCBC has a little overshoot and settling time of 0.005 s for $V_{in} = 15$ V, where for 12 V and 9 V there are negligible overshoots and settling time of 0.007 s and 0.01 s for the designed SMC respectively. Figure 31 shows the dynamic behavior in the start-up for output voltage of POEPCBC for different load resistances like 40 Ω, 50 Ω and 60 Ω. It is seen that output voltage of POEPCBC has a slight overshoot and settling time of 0.005 s for $R = 60$ Ω, $R = 50$ Ω and $R = 40$ Ω, the output voltage has negligible overshoot and settling times of 0.007 s and 0.01 s in start-up with designed SMC respectively.

Figure 32 and Figure 33 shows the dynamic behavior at start-up for the average output currents of modules-1 and modules-2 for $V_{in1} = 12$ V and $V_{in2} = 15$ V. It can be seen that the output current of modules-1 and modules-2 for $V_{in1} = 12$ V and $V_{in2} = 15$ V has an equal current distribution.

7.2. Line Variations

Figure 34 shows the simulation response of average output voltage of POEPCBC using SMC for input change from 12 V to 15 V (+30% line variations) at time = 0.11 s and 0.05 s from these figures, it is clearly found that both the simulated and experimental response of output voltage of the POEPCBC using SMC has maximum overshoot of 2.5 V and settling time of 0.025 s. Figure 35 shows the experimental response of the average output voltage of the POEPCBC using SMC for and input voltage step change from 12 V to 15 V (+30% line variations) at time = 0.02 s. From these figures, it is clearly found from the experimental response that the output voltage of the POEPCBC using SMC has a maximum overshoot of 2.5 V and a settling time of 0.02 s.

Figure 36 shows the simulation response of average output voltage of POEPCBC using SMC for input change from 12 V to 9 V (−30% line variations) at time = 0.11 s and 0.05 s. From these figures, it is clearly found that both the simulated and experimental response of output voltage of the POEPCBC using SMC has maximum overshoot of 2.3 V and settling time of 0.02 s. Figure 37 shows the experimental response of the average output voltage of the POEPCBC using SMC for an input voltage step change from 12 V to 9 V (−30% line variations) at Time = 0.02 s. It can be seen from the experimental response that the output voltage of the POEPCBC using SMC has a maximum overshoot of 2.3 V and a settling time of 0.02 s.
Figure 30. Start-up response of average output voltage of POEPCBC ($R = 50 \Omega$).

Figure 31. Start-up response of average output voltage of POEPCBC ($V_{in} = 12 \text{ V}$).

Figure 32. Start-up response of various input voltage ($V_{in1} = 12 \text{ V}$ and $V_{in2} = 15 \text{ V}$) and average output current of POEPCBC 1 [Ch1: 500 mA/Div-load current].
Figure 33. Start-up response of various input voltage ($V_{in1} = 12$ V and $V_{in2} = 15$ V) and average output current of POEPCBC 2 [Ch1:500 mA/Div-load current].

Figure 34. Output voltage of POEPCBC (12 V to 15 V).

Figure 35. Output voltage of POEPCBC for input step change from 12 V to 15 V at time 0.05 s with $R = 50$ $\Omega$ [Ch1:5V/Div-output voltage and Ch2:5V/Div-input voltage].
7.3. Load Variations

Figure 38 shows the simulated response of output voltage of POEPCBC using SMC for load change 50 Ω to 60 Ω (+20% load variations) at time = 0.05 s. It could be seen that both simulation and the experimental results of output voltage of POEPCBC using SMC has a small overshoot of 1 V with quick settling time of 0.015 s.

Figure 39 shows the experimental response of the output voltage of the POEPCBC using SMC for a load step change from 50 Ω to 60 Ω (+20% load variations) at time = 0.05 s. It can be seen from the experimental results that the output voltage of the POEPCBC using SMC has a small overshoot of 2 V with a quick setting time of 0.01 s.

Figure 40 shows the simulated response of output voltage of POEPCBC using SMC for load change 50 Ω to 40 Ω (+20% load variations) at time = 0.05 s. It could be seen that both simulation and the experimental results of output voltage of POEPCBC using SMC has a small overshoot of 0.5 V with quick settling time of 0.02 s. From Figure 38 and Figure 40, it is clear that the experimental results exhibit close agreement with simulation results under load variation with the designer controller.

Figure 41 shows the experimental response of the output voltage of POEPCBC using SMC for a load step change 50 Ω to 40 Ω (−20% load variations) at time = 0.05 s. It can be seen from the experimental results that the output voltage of the POEPCBC using SMC has a small overshoot of 2 V with a quick setting time of 0.01 s.
Figure 38. Output voltage of POEPCBC (50 Ω to 60 Ω).

Figure 39. Output voltage of POEPCBC when load value takes a step changes from 50 Ω to 60 Ω at time 0.05 s with $V_{in}=12$ V [Ch 1:5V/Div-output voltage and Ch2:500 mA/Div-load current].

Figure 40. Output voltage of POEPCBC (50 Ω to 40 Ω).
Table 5 shows the experimental and simulated results of the average output current and voltage of each of the modules and the POEPCBC with the developed controllers for various input voltages and load resistances in the start-up region. From Table 5, it is clearly found that the voltage that the voltage regulation and the current distributions of each of the modules and the POEPCBC using the designed SMC show excellent performance with a clearance of 2%.

### 7.4 Steady Stage Regions

Figure 42 shows the simulation instantaneous output and the inductor current of POEPCBC in the steady state region using developed controller. It is evident from the figure that the output voltage ripple is very small about 0.18V/0.03V and peak to peak inductor ripple current is 0.42A/0.32A for the average switching frequency of 100kHz closer to theoretical value listed in Table 2. Figure 43 shows the experimental instantaneous output voltage and inductor current of the paralleled modules in the steady state region using the SMC. It is marked from the figure that the load voltage ripple is very low about 0.45 V, and that the peak to peak inductor ripple current is 0.4 A for an average switching frequency of 100 kHz and is closer to the theoretical designed value listed in Table 2. In summary, from this it is clearly signified that the experimental results of the POEPCBC using the designed SMC match the simulated results with a tolerance of 2%. The proposed SMC performed well in all of the working conditions of the POEPCBC.
8. Conclusion

This paper has successfully demonstrated the design and suitability of the sliding mode controlled based positive output elementary parallel connected boost converter. The simulation based performance analysis of a sliding mode controlled positive output elementary parallel connected boost converter circuit has been presented along with its state averaged model. The proposed control scheme has proved to be robust and its triumph has been validated with load and line regulations and also with circuit components variations. Therefore, the system achieves a robust output voltage against load disturbances and input voltage variations to guarantee the output voltage to feed the load without instability. The approach thus has several advantages for it credits: stability even for large supply, load variations, and circuit components variations, robustness, good dynamic behavior and simple implementation. The proposed configuration, thus claims its use in applications such as computer peripheral equipment and industrial applications, especially for high output voltage projects.

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G. Jiji et al.

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