Novel 5T1C pixel circuit for high-ppi AMOLED displays with n-channel LTPS TFTs

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ABSTRACT
This paper proposes a novel 5T1C pixel circuit to compensate for the threshold voltage variation of n-channel LTPS TFTs for high-ppi AMOLEDs. SmartSpice simulation is used to evaluate the compensation capability of the proposed pixel circuit, and layout is performed to check the pixel density in 1 inch. The simulation results show that the proposed pixel circuit can compensate for the threshold voltage variation of n-channel poly-Si TFTs, and the layout confirms that the proposed pixel circuit can be integrated into up to 564-ppi AMOLED displays.

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1. Introduction
The active-matrix organic light-emitting diode (AMOLED) display has been the most popular display of late for smartphone applications due to its high flexibility, fast response time, wide viewing angle, low power consumption, and low thickness. Although AMOLED displays for smartphones are mass-produced, AMOLED displays have several issues, such as luminance non-uniformity, IR droop on the supply line, short lifetime, and the screen burn-in [1–3].

A typical AMOLED pixel circuit consists of a driving transistor, several switching transistors, and one or two capacitors using low-temperature polysilicon (LTPS) thin-film transistors (TFTs), which have higher mobility than amorphous silicon (a-Si) TFTs. The luminance non-uniformity of the AMOLED display, however, is induced by the non-uniformity in the electrical characteristics of the driving TFTs because the luminance of the pixels is sensitive to the electrical characteristics of driving TFTs with the conventional pixel structure consisting of two transistors and one capacitor [3,4]. The variations of the LTPS TFT characteristics usually originate from the beam energy fluctuation of the excimer laser used for the crystallization of the a-Si. This luminance non-uniformity problem has been alleviated by internal or external compensation [4,5]. In general, AMOLED displays for smartphones are more suitable for internal compensation than for external compensation.

The internal compensation method can be classified into the current programming scheme or the voltage programing scheme [4]. The current programing scheme can compensate for the change in both the threshold voltage and mobility of a driving TFT. There are problems, however, of long programing times caused by the parasitic capacitance and resistance of the data line at low luminance levels and the larger size of the D-IC for the current programing AMOLED compared to the D-IC for the voltage programing AMOLED [3,6]. Therefore, the voltage programing scheme is considered more suitable for small AMOLED display panels.

The AMOLED pixel circuit with LTPS backplane technologies can be implemented as an n- or p-channel pixel circuit. Although p-channel pixel circuits are more widely used than n-channel pixel circuits, the n-channel pixel can be extended to the amorphous-oxide TFT backplane, which has only an n-channel device. Therefore, this paper proposes a new voltage programing AMOLED pixel circuit, which can compensate for the threshold voltage variation of n-channel poly-Si TFTs, for high-ppi AMOLED displays.

2. Proposed pixel circuit
Figure 1 shows the proposed pixel circuit and its timing diagram. The proposed 5T1C pixel circuit is composed of one driving TFT (T3), four switching TFTs (T1, T2a, T2b, T4, and T5), and one capacitor (Cst). To reduce the voltage fluctuation of node ‘A’ due to the leakage current of the LTPS TFTs, the switching TFT between node A and the source terminal of T1 is implemented as
Figure 1. (a) Schematic and (b) timing diagram of the proposed 5T1C pixel circuit.

Figure 2. Operation of the (a) initialization, (b) threshold sensing and data programming, and (c) emission for the proposed 5T2C pixel circuit.
(3) Threshold sensing and data programing period: Only G(N) maintains a high state, so that T2a, T2b, and T4 are turned ON and a data voltage is supplied to the source terminal of T3 through T4, as shown in Figure 2(b). As the gate and drain voltages of T3 are higher than \( V_{\text{data}} + V_{\text{th,T3}} \), the current flows through T3. The current that flows through T3 decreases the potential of T3’s gate node, and T3’s \( V_{GS} \) approaches the threshold voltage of T3 at the end of this period. Finally, the gate voltage of T3 becomes \( V_{\text{data}} + V_{\text{th,T3}} \).

Table 1. Device parameters and driving voltages for the proposed pixel circuit.

| Parameter Value | Parameter Value |
|-----------------|-----------------|
| \((W/L)T1 [\mu m/\mu m]\) | \((W/L)T2a,T2b [\mu m/\mu m]\) | \((W/L)T3 [\mu m/\mu m]\) | \((W/L)T4 [\mu m/\mu m]\) | \((W/L)T5 [\mu m/\mu m]\) | \(C_{\text{st}} [\text{fF}]\) | \(G(N) [\text{V}]\) | \(EM(N-1) [\text{V}]\) | \(EM(n) [\text{V}]\) | \(VDD [\text{V}]\) |
| 3/3 | 3/3 | 3/15 | 3/3 | 3/3 | 40 | 0 \(\sim\) 15V | 0 \(\sim\) 15V | 0 \(\sim\) 15V | 11V |

(4) Holding period: EM(N) and G(N) are kept at a low state in this period so that node A is floating and the stored charges of \( C_{\text{st}} \) are held.

(5) Emission period: EM(N-1) and EM(N) set the current path from \( V_{\text{DD}} \) to \( V_{\text{SS}} \) via the OLED and T3, so that OLED emits light, as shown in Figure 2(c). The gate voltage of T3 remains \( V_{\text{data}} + V_{\text{th,T3}} \), which is stored in the storage capacitor \( (C_{\text{st}}) \), as shown in Figure 2(c). As the threshold voltage of the driving TFT is included in the gate voltage of T3, and as T3 operates as a source follower, the OLED current becomes less sensitive to the threshold voltage variations of the driving TFT than the conventional 2T1C pixel structure [8].

3. Simulation results

To verify the compensation performance of the proposed pixel circuit, the proposed circuit was simulated with

![Figure 3](image)

Figure 3. Simulated waveforms of the (a) voltage of node A and the (b) OLED current of the proposed pixel circuit.

![Figure 4](image)

Figure 4. OLED current as a function of the data voltage for (a) the conventional 2T1C pixel circuit and (b) the proposed 5T1C pixel circuit.
Table 2. Layout design rule of the n-channel LTPS TFT process.

| Description                        | Value       |
|------------------------------------|-------------|
| Minimum width of active            | 2.0 μm      |
| Minimum space between two actives  | 2.0 μm      |
| Minimum width of gate              | 2.5 μm      |
| Minimum space between two gates    | 2.0 μm      |
| Minimum width of M1                | 2.5 μm      |
| Minimum space between two M1s      | 2.5 μm      |
| Minimum width of S/D               | 2 μm        |
| Minimum size of CNT                | 2 μm x 2 μm |
| Minimum space between two S/Ds     | 2 μm        |
| Minimum extension of active from CNT| 1 μm       |
| Minimum extension of gate from CNT | 1 μm       |
| Minimum extension of M1 from CNT   | 1.5 μm      |
| Minimum extension of S/D from CNT  | 1.25 μm     |
| Minimum size of Via                | 3 μm x 4 μm |
| Minimum extension of S/D from Via  | 1 μm        |
| Space between n+ active and gate   | 1 μm        |

Smartspice (level = 36). Table 1 lists the driving voltages of the control signals and power, and the device parameters of the proposed 5T1C pixel circuit. The OLED is modeled by a diode-connected TFT with a capacitor.

Figure 3 shows the transient waveforms of the voltage of node A and the OLED current with \( V_{\text{data}} = 4.6 \) V when the threshold voltage of T3 is set to 2.0, 2.5, and 3.0 V. The frame frequency is 60 Hz, the resolution is Quad HD \((2560 \times 1440)\), and the gate ON time is 6.5 μs. The voltage of node A changes drastically at the control signal edges due to the capacitive coupling between the parasitic capacitance of the switching TFT and \( C_{\text{st}} \). In the initialization period, it can be confirmed that the voltage of node A increases to more than \( V_{\text{data}} + V_{\text{th}} \). In the threshold sensing and data programing period, the voltage of node A is modulated according to the threshold voltage of the OLED driving TFT (T3) when 4.6 V is applied to the pixel. Lastly, the gate voltage of T3 becomes \( V_{\text{data}} + V_{\text{th,T3}} \) and is stored in \( C_{\text{st}} \). In the emission period, the variation of the OLED current is very small, between 65 and 75 nA, despite the threshold voltage variation of the TFTs.

Figure 4 shows the OLED currents for the proposed pixel circuit and the conventional 2T1C pixel circuit. It can be seen that the OLED current is well compensated in the proposed circuit with regard to the data voltage for a 2–3 V threshold voltage shift. Therefore, the proposed pixel circuit has better immunity to the threshold voltage variation of the driving TFT compared to the conventional 2T1C pixel structure.
To investigate the compensation performance of the threshold voltage variation of the proposed pixel circuit, the range of the threshold voltage was set at 2–3 V. Figure 5 shows the relative current error rate as a function of $I_{\text{OLED}}$ at $V_{\text{th}} = 2.5$ V for different threshold values in the proposed pixel circuit. The maximum error rate of the OLED current at $I_{\text{OLED}} = 20$ nA is 14.11%, that at $I_{\text{OLED}} = 30$ nA is 11.75%, and that at $I_{\text{OLED}} = 40$ nA is 10.30%. Obviously, OLED is almost independent on the threshold voltage variation of TFTs, so the proposed pixel circuit can compensate well for the threshold voltage variation of TFTs.

4. Layout of the pixel circuit

The layout of the proposed pixel circuit is performed using the top-gate coplanar n-type LTPS TFT structure for the 5.2-inch QHD display with a pentile technology of 2 subpixels per pixel. The subpixel size is set to $22.5 \times 45 \mu m$, and for the device parameters of the proposed pixel circuit, those in Table 1 are used. The layout design rules of thin films are summarized in Table 2, and M1 is a metal layer and is located between the gate and S/D layers. $C_{\text{st}}$ is formed by the metal–insulator-metal (MIM) capacitor and by using the gate and M1 layers. The CNT defines the contacts from S/D to active, gate, and M1, and the Via hole connects S/D and the anode electrode. Figure 6 shows the layout of the proposed pixel circuit, in which the anode layer is omitted, and verifies that the proposed pixel circuit can be integrated up to 564 ppi.

5. Conclusion

In this paper, a novel organic light-emitting diode (OLED) pixel circuit is proposed to compensate for the threshold voltage variation of n-channel low-temperature polysilicon thin-film transistors (LTPS TFTs) for high-ppi active-matrix OLEDs (AMOLEDs). The proposed 5T1C OLED pixel circuit consists of four switching TFTs, one OLED driving TFT, and one capacitor. One frame time of the proposed pixel circuit is divided into the no-emission period, initialization period, threshold voltage sensing and data programing period, data holding period, and emission period. The SmartSpice simulation results show that the maximum error rate of the OLED current at $I_{\text{OLED}} = 20$ nA is 14.11%, that at $I_{\text{OLED}} = 30$ nA is 11.75%, and that at $I_{\text{OLED}} = 40$ nA is 10.30% when the threshold voltage of the driving TFT varies from 2 to 3 V. The layout of the subpixel indicates that the proposed pixel circuit can be integrated up to 564 ppi using the pentile technology with 2 subpixels per pixel. Thus, the proposed 5T1C pixel circuit can achieve a uniform OLED current with high immunity to the threshold voltage variation of the n-channel LTPS TFT and high-ppi AMOLED displays.

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