Forming small junctions with reduced defectiveness

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Abstract. This paper is dedicated to studying possibilities of forming small junctions with reduced defectiveness. As horizontal dimensions of devices in VLSIs diminishes, the task of reducing their vertical dimension becomes more pressing [1, 2]. Due to that, the task of producing small p+n junctions for CMOS structures by means of boron implantation becomes ever more important; the projected path of boron ions is significantly longer than those of n-type conductivity dopants. Using ion implantation for this purpose at low energy is not a good idea, as the depth of junction is largely determined by channeling effects in monocrystalline substrates. Ion implantation in substrate covered with amorphous films of SiO2 or Si3N4 does not remove the phenomenon of channeling completely. Nitrogen and oxygen atoms being trapped in the substrate from the amorphous films may result in degradation of characteristics of produced devices. Besides the channeling effects, the processes of dopant redistribution during annealing may also significantly affect the depth of the junctions.

1. Introduction

As horizontal dimensions of devices in VLSIs diminish, the task of reducing their vertical dimensions becomes more pressing [1, 2]. Due to that, the task of producing small p+n junctions for CMOS structures by means of boron implantation becomes ever more important; the projected path of boron ions is significantly longer than those of n-type conductivity dopants. Using ion implantation for this purpose at low energy is not a good idea, as the depth of junction is largely determined by channeling effects in monocrystalline substrates [3]. Ion implantation in substrate covered with amorphous films of SiO2 or Si3N4 is performed with the aim of reduce the influence of channeling [4, 5] However, it does not prevent the phenomenon of channeling completely. Moreover, nitrogen and oxygen atoms being trapped in the substrate from the amorphous films may result in degradation of characteristics of produced instruments. Besides the channeling effects, the processes of dopant redistribution during annealing may also significantly affect the depth of the junctions, the the diffusion factor of boron in silicon is large enough.

That is why ion implantation into amorphous layers of Si (α-Si) with subsequent epitaxial recrystallization of implanted amorphous layers is a promising direction of research [6, 7]. In this case, there are no channeling effects and the temperature of the epitaxial recrystallization is low enough to prevent significant dopant redistribution. There are several variants of the implantation process that include implantation of BF2+ ions, implantation of boron ions into a substrate surface previously amorphized by implantation of silicon or inert gas ions, implantation of boron ions into a substrate covered with a precipitated amorphous layer of α-Si. This work considers the formative conditions for small p+n junctions by means of implanting boron ions into α-Si layers

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with subsequent low-temperature thermal or electron beam annealing.

2. Experiment
Substrates Si(100) with specific resistivity of 10 Ohm-cm were used. Precipitation of α-Si layers onto the substrates were performed at a temperature of 30°C in 10⁻⁶ Pa vacuum at a precipitation rate of 0.5 nm/s. Implantation of silicon ions into the substrates were done with energy of 100 keV at a dosage of (1-2)×10¹⁵ cm⁻².

Boron ions were implanted at energy of 35 keV at a dosage of 10¹⁵ cm⁻² in a direction deviated by 7° from the normal to the surface of the substrate in order to minimize channeling effects. In order to obtain p-n junction in both amorphous layer and monocrystalline substrate, the thickness of the α-Si layers was changed by means of varying its precipitation time, or by means of reducing the energy of the implanted Si ions.

So, the formative depth of a p-n junction at the conditions of boron implantation is 205 nm and in the specimens where the thickness of the α-Si layer amounted to 300 nm, the junction was located inside the α-Si layer, while in those specimens where the α-Si layer was 150-nm-thick, the junctions was located in the monocrystalline substrate. Specimens were annealed at a temperature of 650°C for 30 minutes or at a temperature of 900°C during the same time but in nitrogen atmosphere. Electron beam annealing was conducted at an accelerating voltage of 30 kV, beam current was 80-100 µA. Substrate temperature was 300°C. In addition, before the electron beam annealing, the specimens were annealed at 650°C to prevent polycrystalline growth of amorphized layers. Distribution profiles of carrier concentration and mobility were determined with Hall effect and measurements of surface resistance with layer-by-layer removal of surface layers by means of anodic oxidation. Control over distribution of implanted boron ions was performed by the method of secondary ion mass spectrometry.

In order to optimize the annealing conditions, changes in electric activity of implanted boron depending on the power of electron beam were studied. The activity was determined as a ratio of the surface concentration of N₁eff carriers to the total dose of implantation N₄. Figure 1 shows the results for the specimens with implanted boron ions. As it may be seen, electric activity linearly increases with temperature.

![Figure 1. Electric activity and mobility as functions of temperature](image)

During the studies, no significant difference between electron beam and thermal annealing was found, as well as between a single-stage and two-stage annealing with respect of changes in mobility and electric activity in the samples. Thus, the temperature of the electron beam annealing was maintained at 1150°C, providing full activity and lack of defects.

Studying distribution profiles of boron ion implantation has shown that the tail of the distribution profile for monocrystalline substrates is 130 nm deeper that in the specimens with amorphized surface layer. Besides, carrier concentration in α-Si was up to 25% higher than the atomic concentration.

Figure 2 shows distribution profiles for boron concentration in specimens with the thickness of α-Si precipitated layer of 300 (1) and 150 (2) nm after annealing at 650°C for 30 minutes. It is evident that the depth of ion penetration by means of channeling is significantly reduced with increased thickness of amorphized layers.
Figure 2. Distribution profiles for boron concentration with various thicknesses of α-Si precipitated layer: 1 - 300 nm, 2 - 150 nm, 3 - without α-Si

Electric characteristics of the boron-implanted α-Si layers were studied with current-voltage curves of the testing diode structures. Figure 3 shows dependences of reverse currents in p-n junctions. It is evident that the current in such specimens is higher in comparison with the standard specimens without a α-Si (1) film.

Figure 3. Dependences of reverse currents in p-n junctions: 1 - without α-Si, 2 - α-Si (150 nm), 3 - α-Si (300 nm)

Deterioration of current-voltage curves of the studied junctions is linked to formation of structural defects during solid phase recrystallization [8]. Rutherford backscattering was used to establish that the defects are mainly located in a partially misoriented area between the α-Si and the substrate. Besides, the quality of recrystallized layers is worse than that of the initial monocrystal. In order to anneal the defective structures, temperatures above 900°C are needed. High-temperature annealing facilitates thermal diffusion of the implanted dopant and is unacceptable in formation of small junctions.

Unlike in previous specimens, Rutherford backscattering does not find crystalline defects in precipitated α-Si films, however, transmission electronic microscopy finds a small number of dislocation loops at a α-Si/Si boundary, which later remain in the recrystallized layer.

In specimens where the α-Si layer thickness is larger than the junction depth, the initial α-Si/Si boundary is located in the depletion region. That is why defects existing at this boundary act as generation and recombination centers, resulting in high values of current. For specimens where the α-Si layer is significantly thinner, the
defects do not get into the depletion region, thus, quality of such junctions is significantly higher. For specimens where after ion implantation of silicon there is a high density of residual defects in the depleted layer, the depth of the junction is somewhat above the amorphization boundary. Thus, in order to obtain small-scale junctions with good electric characteristics, it is advantageous to implant boron ions into substrates with precipitated α-Si films in such a way that the energy of the ions is sufficient to form junctions beyond the boundary of α-Si

Influence of the two-stage annealing onto characteristics of the junctions may be described in the following way. Boron atoms in the monocrystalline silicon substrate, which are insufficiently activated with low-temperature thermal annealing are very efficiently activated by means of the subsequent electron beam annealing. Junction location migrates deeper through the monocrystalline silicon substrate by means of additional activation of boron atoms. As a result, the depleted layer is no longer reaching the α-Si/Si boundary, even when the reversed bias is large.

Thus, precipitated films and self-implanted layers of α-Si provide formation of small p-n junctions, however, structural defects at the α-Si/Si boundary that are not removable with low-temperature thermal or electron beam annealing lead to a significant increase in reverse currents in such junctions if the depleted layer crosses this boundary. That is why p-n junctions with good electric characteristics are obtained as a result of implanting boron ions into precipitated layers of α-Si on the surface of monocrystalline substrate, with the thickness of the layer not exceeding the depth of a p-n junction. In case of α-Si layers, that are amorphized with silicon implantation, the junction shall be formed deeper than a partially misoriented zone between the α-Si and the monocrystalline substrate. A two-stage annealing consisting of a low-temperature thermal annealing with subsequent electron beam annealing efficiently reduces the shunt current to reverse biased p-n junctions formed in the monocrystalline silicon substrate below the α-Si/Si boundary.

When activating the alloying admixture during the solid phase epitaxial growth, there remains a zone of dislocation loops near the boundary between the amorphous and crystalline phases, induced by residual disturbances in the final part of the path of an ion used for amorphization. A complete removal of ion implantation-induced defects after alloying admixture activation is a serious problem in creating junctions with a small value of shunt current. The second problem in the small junction technology is a high surface resistance due to limited solubility of the alloying dopant in silicon. In order to reduce the resistance, precipitation of a metal silicide with good conductivity at the junction area is used. It is known that interaction of a high-melting metal with silicon results in excessive vacancies. For many high-melting metals, the main diffusing particles during formation of their silicides are Si atoms, moving though the silicide layer leaving behind vacancies in the substrate. These vacancies may recombine at dislocations in the end of the ion path, dissolving them in the silicon substrate. We also created small junctions using silicon substrates pre-amorphized with germanium. After activation of alloying admixture by means of solid phase epitaxial growth near the initial boundary between the amorphous and crystalline phases, there is a zone of dislocation loops, induced by residual distortions in the end of path of the Ge+ ions. A complete annihilation of interstitial defects in small p+n junctions induced by germanium implantation takes place during the silicide formation.

We studied the influence of interactions between a metal and silicon onto reduction of the residual defects. As substrates, silicon plates were used with an orientation of (100), p-type conductivity with a specific resistivity of 10 Ohm-cm and n-type conductivity with a specific resistivity of 7.5 Ohm-cm. In small junctions, p+ and n+ layers were created after amorphization with Ge+ ions by ion implantation of B+ and As+, respectively. Energy (80 keV) and dosage (10^15 cm^-2) of the Ge+ ions were selected in order to amorphize the whole area of B+ implantation (and thus prevent channeling) and to keep extensive defects that appear in the end of the ion path at a boundary between the amorphous and crystalline phases inside the strongly alloyed layer and farther away from the depleted zone. Boron implantation for formation of p+ areas was performed at the energy of 10 keV and dosage of 10^15 cm^-2, while implantation of As+ for formation of n+ areas was performed at the energy of 50 keV and dosage of 5×10^15 cm^-2. Following the implantation, the specimens were annealed in a two-stage process in argon atmosphere at a temperature of 550°C during 30 minutes for solid phase epitaxial growth with subsequent fast thermal annealing at 1050°C for 10 seconds to activate the alloying dopant.

The depth of the junction measured with secondary ion mass spectrometry amounted to 180 nm for the p+ layer and 160 nm for the n+ layer at a concentration of charge carriers in the initial substrate at about 10^16 cm^-3. The silicide was formed either by regular two-stage annealing process after the junction was formed, or in a parallel process, where the reaction between a metal and silicon undergoes in parallel with annealing of the junction. Silicide formation starts with precipitation of titanium layer with a thickness of 30 nm, after which the specimen undergoes quick thermal treatment at 600-650°C for 10 seconds to facilitate mutual diffusion of the metal and silicon, with subsequent quick thermal annealing for 10 seconds, but this time at a temperature of 800-850°C. Both processes of quick thermal treatment are performed under inert atmosphere of argon or nitrogen. In the parallel process of silicide formation, a layer of Ti film with a thickness of 30 nm was precipitated directly after creating a junction by means of ion implantation. After that, the specimen underwent a quick thermal
treatment at 600-800°C in argon or nitrogen for 10 seconds, with a subsequent second quick thermal treatment at 1000-1100°C in argon during 10 seconds. The second annealing is performed in order to activate and transform titanium silicide to a low-resistance disilicide form.

Surface resistance of titanium silicide formed at p+ and n+ layers was studied in the context of the silicide formation temperature. In the low-temperature zone (below 600°C), the surface resistance of the silicide is a measure of silicide-forming reaction: the lower the layer resistance, the more silicide is formed. At a temperature of 600-800°C, the surface resistance abruptly drops, which corresponds to an abrupt change in the amount of silicide formed. There is a difference between the silicides formed at p+ and n+ layers. Surface resistance of the silicides at p+ and n+ is being saturated similarly, up to 2-3 Ohm/□, for silicides grown at a temperature above 850°C; the surface resistance of silicides on n+ layers is higher than that on p+ layers for the silicides at a temperature of 550-700°C. Thus, at lower temperatures, the amount of silicides being formed on a n+ layer is lower than on the p+ layer; this difference is confirmed by analysis of electronic micrography.

Annihilation of defects on the p+ layer of junction was studied with a transmission electron microscope on structures of a p-channel MOS transistor formed by a sequence of abovementioned processes before precipitation of Ti. Following the implantation of Ge+, an amorphous surface layer is formed; subsequent annealing for activation of the alloying dopant results in recrystallization of the amorphous layer, but leaves behind some defects like implantation dislocations somewhat below the initial boundary between the amorphous and crystalline phases [9]. Defects induced by the ion implantation are evident at a layer at a depth of about 120 nm below the silicon surface. The surface resistance of silicide layers formed at temperatures of 600, 800 and 1000°C is 14.1; 4.2 and 2.8 Ohm/□, respectively. The number and dimensions of the implantation defects decrease with reduction of the surface resistance of the silicide. Reduction of defects in the end of the ion path seems to be caused by injection of vacancies [10].

3. Conclusion

Reduction in implantation defects correlates with the amount of metal participating in a reaction with silicon or with the size of the silicide formed. The more silicide formed, the more atoms leave the substrate to a metal-linked state and thus, more vacancies are injected. A complete prevention of implantation defects requires the number of injected vacancies to be higher than the total concentration of interstitial atoms in the silicon substrate and defects. The total prevention of implantation defects is observed for a silicide with a surface resistance of under 3 ohm/□, corresponding to formation of TiSi2 film with a thickness of 60 nm. The total prevention of defects in the end of the ion path was observed also in silicides formed on p+ layers in the two-stage process at a temperature of 650-850°C in the argon atmosphere, where the layer resistance was 2.0 ohm/□. Formation of silicides depends on changes in surrounding atmosphere. It is known that annealing in nitrogen results in formation of titanium-enriched layer of TiON at the surfaces and a lower amount of silicide than annealing in argon. For the same two-stage process at a temperature of 650-850°C with the first annealing at 650°C, but in the nitrogen atmosphere, the surface resistance of specimens increased to 4.1 ohm/□, while defects in the end of the ion path were not completely annihilated. Implantation defect concentration in the n+ layer is much higher than in the p+ layer, as the n+ layer is heavily doped with As+ ions at a dose of 5 × 10¹⁵ cm⁻². A higher local concentration of interstitial atoms in the n+ layer also requires a higher number of vacancies being injected during the silicide formation. As less silicide is formed in the n+ layer of the junction, there are fewer vacancies formed than in the case of the p+ layer.

When silicide is formed in a process parallel to junction formation, when the metal chemically interacts with a previously amorphized silicon surface, simultaneously with the recrystallization process, the number of vacancies produced in formation of silicide shall be much higher in comparison with sequential processes of junction formation and silicide formation for the same thickness of the silicide layer. Surface resistance of titanium silicide formed first at 800°C for 10 seconds with subsequent thermal treatment at 1050°C for 10 seconds amounts to 2.5 ohm/□.

Reduction in defects during the silicide formation was also evaluated by comparing channeling current in junctions with a titanium silicide film and without such film. For junctions without the silicide film, surface-leakage current distribution is very dense with an average value of about 10 nA. For junctions with the silicide film, distribution of the surface leakage current is up to 1 nA. The average surface resistance of the junctions with silicide in the cases under consideration was 3.5 ohm/□.

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