CQC: A Crosstalk-Aware Quantum Program Compilation Framework

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Abstract
Near-term quantum systems are noisy. Crosstalk noise has been identified as one of the major sources of noises in superconducting Noisy Intermediate-Scale Quantum (NISQ) devices. Crosstalk arises from the concurrent execution of two-qubit gates, such as \( \text{CX} \), on nearby qubits. It may significantly increase the error rate of gates compared to running them individually. Crosstalk can be mitigated through scheduling or hardware tuning. Prior studies, however, handle crosstalk at a very late stage in the compilation, typically after hardware mapping is done. It might miss great opportunities of optimizing algorithm logic, routing, and crosstalk at the same time. In this paper, we push the envelope by considering all these factors simultaneously at the very early compilation stage. We propose a crosstalk-aware quantum program compilation framework called CQC that can enhance crosstalk-mitigation while achieving satisfactory circuit depth. Moreover, we identify opportunities for translation from intermediate representation to circuit for application-specific crosstalk mitigation, for instance, the \( \text{CX} \) ladder construction in variational quantum eigensolvers (VQE). Evaluations through simulation and on real IBM-Q devices show that our framework can significantly reduce the error rate by up to 60%, with only \( \sim 60\% \) circuit depth compared to state-of-the-art gate scheduling approaches. In particular for VQE, we demonstrate 49% circuit depth reduction with 9.6% fidelity improvement over prior art on the H4 molecule using IBMQ Guadalupe. Our CQC framework will be released on GitHub.

1. Introduction
Quantum computing are known to solve certain classically intractable problems across various domains such as cybersecurity [24], chemistry [16, 7], complex manufacturing [13], and artificial intelligence [9, 37]. IBM, Google, and Rigetti among others have delivered superconducting quantum devices with dozens of qubits through the cloud. Particularly, it is expected that IBM will deliver thousand-qubit devices soon [11], bringing quantum computing closer to technical reality.

Today’s superconducting NISQ systems are prone to various types of errors: decoherence error [31], readout error [23], gate error [12], and crosstalk error. In particular, the crosstalk error is reported to have significant impact, which could be 10x worse than other errors [30, 14]. Crosstalk error arises from unwanted coupling between concurrent qubit operations under similar frequency [30]. Two gates that are on physically nearby qubits are prone to crosstalk. Running two gates that have crosstalk will lead to higher error rate for each gate than when running each of the two gates independently. In summary, the three contributing factors to superconducting crosstalk are the following: (a) spatial closeness; (b) temporal closeness, and (c) similar operating frequency.

Recent studies have aimed to mitigate crosstalk from hardware perspective and software perspective. From hardware perspective, certain hardware devices [6, 5] allow dynamic frequency tuning. Hence it can be leveraged to break one of the conditions for crosstalk [8, 17]. However, it requires the hardware to have such capability. Different vendors use different technology. Not all support tunable frequency. For instance, most available quantum machines by IBM are implemented using fixed-frequency transmons.

From software perspective, it mitigates crosstalk at compile-time, runtime, and pulse level. It does not require hardware modification. Our work belongs to this category. Murali et al. [25] alleviate crosstalk at gate scheduling level, by delaying one of the two interfering gates to a later time. Delaying gates may lead to larger depth and potentially larger decoherence error. They rely on an SMT solver to find a tradeoff between crosstalk and depth. Xie et al. [39] suppresses ZZ crosstalk using a co-design approach. It takes crosstalk into consideration during pulse generation stage. It leverages pulse scheduling and topology partitioning together to suppress ZZ-crosstalk for the whole circuit.

Compared with prior software approaches [25, 39], our approach is unique in that we take an up-the-stack approach. Rather than waiting until scheduling and pulse phase, we discover that crosstalk can already be mitigated as early as the

Figure 1: Our quantum program compilation workflow.
hardware mapping and IR-to-circuit phase. To better illustrate this idea, an end-to-end quantum compiler includes the following phases: (1) Converting a high-level program specification into intermediate representation (IR), (2) converting IR into a logical circuit [22], (3) hardware mapping [21, 40, 33] from logical circuit to physical circuit, (4) gate scheduling of the physical circuit, and (5) converting gates to pulses and performing pulse scheduling/optimization [39]. The entire workflow converts a high level program specification into control pulses that can be recognized by the low-level hardware.

Existing software approaches [25, 39] have optimized crosstalk at the phases of gate scheduling and pulse generation/scheduling. Our major finding of this paper is that opportunities exist up the stack of the compiler flow for mitigating crosstalk. Postponing until the gate scheduling and pulse generation phases may miss these opportunities.

These opportunities for mitigating crosstalk emerge in two scenarios. First, it is the hardware mapping stage, where SWAP gates are inserted to overcome the topology connectivity constraint. At this stage, a crosstalk-oblivious strategy might lead to a less desired circuit regardless how efficient the scheduling stage is. We show an example that at hardware mapping level, we can properly choose a right SWAP insertion strategy such that crosstalk can be completely mitigated without having to delay gates at scheduling stage, in Fig. 2.

Second, the opportunities arise at the application level. An important class of applications in quantum computing named variational quantum algorithms (VQA) [29, 22] allow circuits to be synthesized in a flexible way from IR: (a) the order of certain gate(s) can be flexibly determined, and (b) even which gates to be synthesized is flexibly determined as long as a tree-Construction constraint is met.

As a matter of fact, VQA happen to be one of the very few applications that can demonstrate quantum advantage using near-term quantum devices [3, 2]. We show two motivating examples for application-specific optimization. In the first example we show a circuit where by exploiting the flexibility of the order of gates, we suppress the crosstalk without affecting the depth. It is in Fig. 3. In the next example, we show how different circuit synthesis with respect to a tree-based constraint can help yield less crosstalk, in Fig. 4.

To exploit these unique opportunities, we introduce a crosstalk-aware quantum program compilation framework, as shown in Fig. 1. The difference between our crosstalk-mitigation compiler and prior work is highlighted in Fig. 1. Compared with the existing framework that perform crosstalk-oblivious [22] IR-to-circuit optimization and hardware mapping, we perform a cross-stack joint crosstalk-aware optimization. The application-specific component is dedicated to VQA applications. For general applications, crosstalk mitigation mainly happens at the hardware mapping and gate scheduling phases. For VQA applications, crosstalk mitigation happens as early as in the circuit construction phase.

As far as we know, our framework is the first to take an up-

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Figure 2: Crosstalk mitigated at the hardware mapping level: (a) The hardware coupling graph. Crosstalk exists between every pair of adjacent links. For instance, \( Q_0 \), \( Q_1 \) and \( Q_4 \), \( Q_5 \); \( Q_1 \), \( Q_2 \) and \( Q_3 \), \( Q_4 \), which implies a significantly higher error rate if two double-qubit gates are executed simultaneously than individually on these pairs. (b) The baseline approach that chooses a SWAP insertion strategy with minimal depth, but introduced high crosstalk [21]. Then a gate must be delayed to avoid crosstalk if two double-qubit gates are executed simultaneously than individually on these pairs. (c) Our Approach. (d) Our SWAP-insertion approach that that attains the maximum parallelism too but without any crosstalk. Our depth is 2. Note that if we assume a SWAP takes 3 CX. Our depth is 4, while the baseline’s depth is 7.

Figure 3: QAOA: Exploiting the flexibility in gate ordering. QAOA is a type of VQA algorithm. The controlled-Rz gate can commute without affecting the outcome. We use the same hardware coupling as in Fig. 2 (a). Now (b) shows the original ordering of gates. (c) Executing according to the original order causes crosstalk. (d) A different order (switching \( R_z(q_3,q_4) \) leads to no crosstalk, same depth.
Figure 4: VQE Example: Exploiting the flexibility in gate synthesis. In this example, we focus on Hamiltonian simulation. (a) Shows the Pauli-string to be simulated. For all non-identical operators (on qubit 0, 1, 3, and 4), a circuit synthesizer must construct a directed tree where a node can follow links (implemented as CNOT gates) to the root. The execution order is also specified by the directions in the tree edges. (b) shows a synthesized tree (and corresponding circuit) that high crosstalk exists if a depth of 3 must be achieved. (c) shows an optimal way to synthesize the circuit with optimal depth is achieved without any crosstalk. Note that the other half of a synthesized circuit is omitted here since they are symmetric.

2. Background

2.1. Circuit Error Model and Crosstalk

1) Single-qubit gates and decoherence error: In superconducting transmose systems, single-qubit gates are implemented by driving the target qubit through microwave in the pulse level [4]. For example, RX and RY rotations can be implemented by sending microwave voltage signals. However, due to imperfect implementation, all these gates can incur single-qubit error. Besides, qubit state can decay in two ways: i) T1 relaxation (i.e., spontaneous loss of energy leading to decay from excited state |1⟩ to ground state |0⟩), and ii) T2 dephasing (i.e., loss of relative quantum phase between |0⟩ and |1⟩). We can model the two decays using the following equation:

\[ q(t) = (1 - e^{-t/T1})(1 - e^{-t/T2}) \]

where \( t \) is qubit life-time; T1 and T2 are constants characterizing the speed of the decays, for a qubit \( q \).

2) Two-qubit gates error and cross-talk error: two-qubit gates play a critical role in quantum computing, as they enforce entanglement between two qubits. Commonly used two-qubit gates include CX (also known as CNOT), CZ and SWAP. Two-qubit gate also has errors and tend to have higher error rate than single-qubit gates.

On top of the individual two-qubit gate error, crosstalk exists when two (pairs of) qubits are accidentally turned on (or close to) resonance, using very close interaction frequencies. Crosstalk exists for all superconducting NISQ machines. Previous study by Murali et al. [25] shows that crosstalk can degrade the error rate of a two-qubit gate by as much as 10x. Moreover, there is a variability of crosstalk error in the architecture. That is, some pairs of gates are more prone to crosstalk errors while others are less affected by the interference [25].

2.2. Quantum Program Compilation Process

From a high-level quantum program to control pulses ready for execution on quantum hardware, there are several stages.
Firstly, the high-level program is translated into a quantum intermediate representation (IR). Next the IR should be further converted to a logical circuit. Depending on the application, the logical circuit may be flexibly [22] synthesized or there is only one way to synthesize a logical circuit, in most cases.

A logical circuit needs to be converted into a physical circuit. When applying a two-qubit gate, two participating qubits need to be physically connected. SWAP operations are inserted to move logical qubits to prepare for double-qubit execution. The hardware mapping stage addresses the SWAP insertion problem. Crosstalk mitigation is typically omitted in the hardware mapping stage in previous studies, as shown in Fig. 1.

After the hardware mapping process, it comes to the gate scheduling process. The crosstalk-adaptive schedule by Murali et al. [25] chooses to delay the gates that have crosstalk if necessary. Delaying is implemented by barriers inserted to the circuit, as shown in our example in Fig. 2 (b).

Our work considers joint optimization of crosstalk through a cross-stack approach, covering IR-to-circuit, hardware mapping, and scheduling stages.

### 2.3. Application-specific Optimization

We focus on VQA for application-specific optimization. Unlike other generic quantum circuit, VQA application gives us the flexibility to synthesize or transform the quantum circuit. In the IR level specification of VQA applications [22], each program be expressed as a sequence of Pauli strings, where gates must be performed on qubits that have non-identify operator. An example is in Fig. 4 (a).

We discuss two categories of VQA applications. One special type of VQA application is the 2-local simulation/optimization applications, such as the Ising model ?? and the QAOA-Maxcut problem. Each Pauli-string in a 2-local VQE application only contains two non-identity operators. This type of quantum application is quite common. In this particular class of applications, the gates do not impose any dependence among themselves [19, 3, 2]. They can run (commute) in any order, without affecting the outcome of the circuit (in the perfect hardware case). An example is in Fig. 3.

The other type of VQE application is n-local, meaning local interaction between n qubits. A Pauli-string may contain more than two non-identity operators. The circuit can be constructed in any form as long as the n involved qubits are connected using CX gates while the formed graph must be a directed tree. There has to be a root. And that every qubit is able to interact with the root through the directed edges in the tree. The execution dependence order is also enforced by the tree. The gates must be executed from the leaves to the root (as if climbing a ladder in the tree) [22]. An example of two different trees for one Pauli-string is shown in Fig. 4.

Li et al. [22] considers such flexibility when performing hardware mapping to minimize depth and gate count. Our framework is the first that exploits such flexibility in circuit synthesis for improving the fidelity and mitigating crosstalk.

![Figure 5: CQC's detailed workflow](figure5.png)

**Algorithm 1:** Compile circuit given a crosstalk allowance xa

```plaintext
1 Function compile_circuit (C, h, arch-X, xa):
   2 // C is input circuit or IR, h is hardware coupling graph, arch-X is crosstalk profile, and xa is crosstalk allowance
   3 while |Unscheduled_gate| > 0 do
   4     V, E = {}, {};
   5     CSG = {V, E};
   6     Cgates = getExecutable(Unsched_gate, xa, h);
   7     SWAPs = getUsefulSWAP(Unsched_gate, h);
   8     V.add(Cgates, SWAPs);
   9     depEdges = getConflict(Cgates, SWAPs);
  10     crosstalkEdges = getXtalk(h, arch-X, xa);
  11     E.add(depEdges, crosstalkEdges);
  12     top_k_sets = graph_coloring(CSG);
  13     gs = top_k_sets.select();
  14     Unsched_gate.update(C, gs);
  15     Qubitmapping.update();
  16 end
```

### 3. Overview of CQC

In this section, we introduce our crosstalk-aware compilation framework. We first define the input and output of our compiler framework, then demonstrate the major components in our framework.

#### 3.1. Input and Output

Our compiler framework CQC either takes a logical circuit (where there is only one way to synthesize the circuit from IR) or an IR as input. It also takes the hardware coupling graph as well as the crosstalk information as input. The crosstalk parameters can be profiled or provided by the vendor. Since we do not focus on the profiling, we adopt previous approach for profiling if necessary [25]. With the consideration of physical connectivity constraint, crosstalk, and qubit decoherence effect, our framework aims to produce a compiled circuit with
maximal fidelity.

3.2. Overall Design

Our ultimate goal is to compile the given circuit with maximal fidelity. Ideally, the compiled circuit has minimal circuit depth and zero crosstalk. However, it may not be possible to have both at the same time. Increasing the allowance of crosstalk, depth of compiled circuit decreases and the decoherence error decreases. Zero crosstalk allowance would make the circuit depth large which would impair the fidelity. With a reasonable tolerance of crosstalk, we may find the balance between circuit depth and crosstalk and achieve the maximal fidelity.

We first determine the range of crosstalk allowance. Next we choose the circuit version with the maximum fidelity in this range.

Maximum crosstalk allowance \( X_{\text{Max}} \). We need to set the maximum crosstalk allowance. With all crosstalk allowed, we compile the input circuit to achieve maximal parallelism and minimal circuit depth. Then we calculate the amount of crosstalk in this compiled circuit and set this as our maximum crosstalk allowance \( X_{\text{Max}} \). The crosstalk could not be worse than that for this version.

Minimum crosstalk allowance \( X_{\text{Min}} \). We set \( X_{\text{Min}} = 0 \).

How to determine the best allowance \( X \). We use binary search to find the best crosstalk allowance in the range \( (X_{\text{Min}}, X_{\text{Max}}) \). The criteria is the fidelity of generated circuit.

Given the crosstalk allowance range \( X \in [X_{\text{Min}}, X_{\text{Max}}] \), we set the initial allowance equal to \( X = (X_{\text{Min}} + X_{\text{Max}})/2 \). Then we compile circuit with crosstalk allowance \( X \) and \( X+1 \) (or \( X \) and \( X-1 \)). We obtain the fidelity of two compiled circuits by calculating the estimated Success Probability (ESP) \(^{[28]}\) considering both decoherence error and crosstalk errors. \(^{1}\)

Then we reset \( X_{\text{Max}} = X \) if \( X+1 \)’s corresponding circuit has worse fidelity, else \( X_{\text{Min}} = X \). Repeating this process until we find the best crosstalk allowance. Once we find the best crosstalk allowance, we also found the circuit with the maximum fidelity. The whole process is shown in Fig. 5 (left side).

3.3. Compile with Respect to A Given Crosstalk Allowance

Now, Let’s discuss how to compile a given circuit with fixed crosstalk allowance and crosstalk parameter. The whole process is shown in right component in Fig. 5 (right side). To compile the input circuit, we go through the circuit and save all un-executed gates in a list \( \text{Unsched list} \) (in Algorithm 1).

We also construct a graph called candidate set graph (CSG) where each node is a gate that can be scheduled at the current time step, where CSG = \( \{V, E\} \).

\( V \) consists of two types of gates. One type is the original gates in the circuit that are executable, satisfying both dependence constraints and hardware coupling constraints. The other type is SWAP gates. They consist of the SWAP gates that can help non-executable (dependence resolved) gates over come the physical constraint. We only focus on the SWAPs that can help reduce the distance by 1 for any pair of qubits in an un-executable CX.

If two vertices \( v_i \) and \( v_j \) share a qubit or there is a crosstalk (that is not in crosstalk allowance) between them, we add an edge \((v_i, v_j)\) into set \( E \).

The Chromatic Method We apply a chromatic method for determining which gates to run and which SWAPs to insert. The idea is that if two gates share a qubit (they conflict), they cannot run simultaneously; If two gates have crosstalk and the crosstalk is not in allowance, they cannot run simultaneously. The coloring method ensures that any two vertices that are adjacent cannot be given the same color, corresponding to the aforementioned constraints. An example on how our compiler automatically found the solution in the motivating example (Fig. 2) is shown in Fig. 6.

After coloring, all gates corresponding to a specific color can run at the same time. We pick a gate set that correspond
to a color with certain criteria such as Cgate count, criticality of selected gates, the usage of crosstalk allowance, and etc (details discussed in Section 4 and Section 5).

We run the selected gate set, update Unshed gate and mapping. This process will be repeated until there is no gate in unscheduled circuit. The algorithm is described in Alg. 1.

**Application-specific Optimization** The overall framework in Fig. 5 and Algorithm 1 work for both general applications and VQA. The differences, however, are in the implementation of the component for generating a compiled circuit given a crosstalk allowance (named Compile circuit(C, arch-X, xa) component). In particular, it is in the “Candidate gate graph construction (CSG)” and the “Getting a gate set” components. We describe them for general applications and VQE in details in the next two sections.

4. Compiling for Generic Applications

For generic applications, there is typically one way to generate a logical circuit from the IR. Hence the order and the gates are pre-determined before compilation.

4.1. Construct CSG For Generic Application

4.1.1. Determining the Vertices of CSG We describe how to construct candidate set graph (CSG) for generic applications. The outline is in Fig. 7.

A vertex in CSG corresponds to a gate. There are two types of vertices in CSG, the original gates in the circuit, which we name as circuit gate (Cgate), and SWAP gates that are to be inserted to the circuit.

**Circuit gate vertex** Generic circuit imposes dependences between gates. The circuit gates that have their dependence resolved, i.e., their predecessors have been executed, and satisfied the coupling constraints, i.e., the two qubits that participate in the gate are placed in adjacent physical qubits, are considered as gate vertices in CSG.

**SWAP gate vertex** We choose the SWAP gates that can help the circuit gates which have their dependency but not coupling constraints resolved. We choose the SWAP gates that can reduce the distance by one for any pair of such qubits.

See an example of Cgate and SWAP vertices in Fig. 6 (b).

**In-progress SWAP** It is note worthy that the execution time of SWAP gate may be decomposed into three CX gates (in some architectures). Hence its latency is different from the CX gate or other two-qubit gates.

It is possible that as the hardware mapper process the next set of gates in the frontier (dependence-resolved gates) in the iterative process (in Alg. 1), the SWAP gates from the last iteration(s) are still in progress. Those SWAP cannot be interrupted and should not let their qubits be used by any other new SWAPs. So those in-progress SWAP gates would be added as SWAP gate vertices to CSG as well.

4.1.2. Determining the Edges of CSG There are two types of edges in the CSG. One type is induced from the gates that share qubits, for instance, different candidate SWAPs. The other type is induced from the crosstalk constraint.

**Shared-qubit induced edges** If two gates(vertices) share a qubit, we add an edge connecting these two vertices.

**Crosstalk edge** If there exist a crosstalk between two gates, we add an edge connecting these two gate vertices in the CSG. In the case of crosstalk allowance, not all crosstalk edges will be included in the final CSG, depending on how much crosstalk is allowed at the current iteration. We first sort all these crosstalk edges according to their crosstalk errors in the ascending order. Then we remove a corresponding number of crosstalk edges that have least crosstalk errors. The number of edges we remove is based on how much crosstalk allowance is left at this current iteration. The crosstalk allowance is updated iteration by iteration.

See an example in Fig. 6 (c) for edges in CSG.

4.2. Gate set generation by graph coloring

To perform graph coloring, we use the Welsh Powell algorithm [36]. It sorts all the vertices by degree and color the highest degree first. It is an efficient greedy algorithm that work for large number of vertices. We slightly modified it to accommodate the case of in-progress SWAPs. If a SWAP gate is decomposed into three CX gates, we do not want to interrupt these in-progress swaps. We first give these in-progress SWAP gates the same color, then we follow the same steps as that in Welsh Powell.

4.3. Gate Set Ranking

After coloring, we must select a proper color which corresponds to a particular gate set to be executed. We can select the color that corresponds to the largest number of gates. However, to maximize fidelity and minimize depth, we must consider the following three factors:

- Circuit gate count.
- Gate criticality.
- Consecutive SWAPs making progress.
• Crosstalk allowance.

For circuit gates count, a color might correspond to a large gate set. But some of them might be just SWAP gates. We need to have a good balance between the number of SWAP gates and circuit gates to make sure the circuit makes progress.

For gate criticality, in each color set, some gates are in the critical path of the circuit while some others are not. Delaying the execution of those critical gates would increase the circuit depth and result in higher decoherence rate. So the more gates in a color set involving the critical path gate, the higher ranking the color has.

For the SWAP gates, since we only determine the concurrent SWAP at one layer at one time. If not properly designed, a SWAP gate that is inserted in the last iteration could be counteracted by another SWAP in the current iteration. This is harmful and prevents the circuit from making progress.

With these considerations, our color set ranking is designed as follows. First, we pick top-k colors with largest gate count. Then we rank these k sets with respect to the number of Cgates. Next we pick the one containing more SWAP gate(s) which help a CX gate already helped in the last iteration, but has not been executed due to coupling constraint. By doing this, the circuit can continue to make progress. We also use crosstalk allowance as a tie breaker at this stage. If both gate sets are ranked the same, we choose the one that uses less crosstalk allowance.

5. Compiling for VQA Applications

5.1. Two Categories of VQA

We categorize VQA into two types. One type encodes 2-local qubit interaction in each Pauli-string. Different Pauli-strings can commute. Each Pauli-string corresponds to one two-qubit gate. Hence the two-qubit gates can commute. This is a fairly common type of VQA application. Examples are quantum approximate optimization algorithm (QAOA), Ising model, and Heisenburg model, [19].

The second type is N-local qubit interaction (N>2), where in each Pauli-string block, more than 2 qubits interact through a tree-like structure. In this case, the flexibility in circuit (tree) synthesis can be exploited for crosstalk mitigation.

5.2. 2-local Case

We still use the overall framework described in Section 16. We in particular discuss the candidate set graph (CSG) construction (in Fig. 8). There is no pre-determined partial order between gates. As the two-qubit gates all commute, the vertex sets need to be constructed in a different way compared with the generic applications.

Circuit gate vertex: Unlike the generic circuit, in the 2-local VQA case, the circuit gate vertex set of CSG consists of coupling-compliant and dependency-resolved gates. We look at the whole circuit and add all the coupling-compliant gates into the vertex set of CSG.

SWAP gate vertex: The vertex set of CSG also contains SWAP gates that will help the coupling in-compliant gate. Similarly those SWAP gates reduce the distance between two qubits corresponding to the coupling in-compliant gates by one. In-progress SWAP gates are also included in the vertex set of CSG.

The edge set: The edge set is determined in the same way as that for the generic application.

2-local case compilation: Once the coloring graph constructed, we apply the graph coloring algorithm to schedule gates at the current layer as discusses in section[??]. This process is repeated until all gates are scheduled.

5.3. N-local Cases (N>2)

5.3.1. Overview N-local VQA provides even more flexibility. It allows flexibly synthesis of a circuit. Instead of decoupling the logical circuit synthesis step from the other components of crosstalk mitigation, we determine the synthesized circuit on the fly together with hardware mapping. The guidance for synthesizing a circuit with respect to a Pauli-string is that two-qubit gates must be applied to the qubits in the non-identity operator in Pauli-string representation. For instance, for the
We apply the MST method to a different graph – the qubit weight. For instance, in Fig. 10 (c), the minimal spanning tree without any cycle, and in the meantime, have smallest total where the logical qubits are mapped to. Certain edges in the weight of the edges in the clique are different.

The non-executable gate set

- The Cgates set
- Candidate SWAP gates set contains SWAP gates that reduce the shortest distance between every two qubits for each gate in the non-executable gates set.

A subtlety here is that for the non-executable gate set, it is not the entire set of edges in the MST with weight > 1. Because we must follow the order of executing gates (as if edges in a tree) from a leave to the root, the edges in the middle of the MST (edges with degree of both nodes >= 2) are unlikely to be executed first anyway. Hence, we only choose the edges in MST which connects one end node (degree of 1).

An example of these three sets are shown in Fig. 10 (d). All gates in the Cgates set, and the SWAP set are added to the vertex set of CSG. In addition, those in-progress SWAP gates are included in CSG like in generic applications.

5.3.3. The edge set of CSG

The edges of CSG for N-local VQE are determined the same as that for the generic application. Fig.10(e) shows the CSG graph.

5.3.4. Workflow Modification for the N-local Case

The handling of the N-local case is a bit different since we need to determine which gates to synthesize at every step, and we have to ensure that we eventually synthesize a tree and that tree-induced circuit is efficient. Hence, we make a slight modification to the workflow as follows.

After the CSG constructed, we apply graph coloring approach in the same way as generic application compilation.

An example for the colored graph is shown in Fig. 10(e) where the gray vertex set is larger than other colored vertex set. Therefore we choose to schedule Cgate(0, 1) and SWAP(4, 6). Then we update the corresponding mapping since a SWAP gate is applied, as shown in Fig. 10(g).

Now we describe the changes to the workflow here.

Gate execution. Despite the fact that we have determined which Cgate to synthesize given the MST, we haven’t determined the the control and target qubits in each selected Cgate. It is important, since the control-target relationship determines the direction of edges in the formed tree. Either direction is okay, as long as eventually we form a tree for a node to find a path all the way to the root. But it might add SWAP cost, if the direction is set up in a un-desired way.

In order to reduce such SWAP cost, we find the graph center of MST. We let the qubit closer to the center be the target qubit and the other qubit be the control qubit. For instance, in our example Fig. 10 (f), we let Cgate(q0, q1) take q0 as control qubit and q1 as target qubit.

Qubit Deleting. After the direction is determined, we re-move the control qubit from the consideration for a future iteration since every time we remove a leaf node and there is no other qubit that points to it. Then we handle the rest of the qubits. For example, in the second iteration of Fig. 10(h), the qubit graph does not contain qubit q0 anymore.

Therefore in the workflow, we need to perform control-target direction determination and qubit deletion after a gate set is selected. It is worth mentioning that at each iteration of
the major workflow component Compile_circuit in Fig. 5, we repeat the same process of qubit graph construction, MST search, and so on. The MST helps us determine a part of the gates that can be executed at one iteration, but it does not mean the tree determined by MST is the final tree. Our example happens to show that MST gives the final synthesized circuit tree, but it is not necessarily the case. The qubit mapping changes over time, and the best circuit tree may change from iteration to iteration too. That’s why we perform circuit synthesis on the fly.

Our example shows a complete process for solving the motivation example circuit in Fig. 4 in Fig. 10. The last few steps (h) to (l) show how the rest of the circuit is handled.

6. Evaluation

In this section, we evaluate CQC by comparing it with the state-of-the-art. First we introduce our experiment setup including the backend, metric, and baselines. Then we show the fidelity and performance (depth) of CQC compared with prior approaches. We perform experiments on both real machine and simulator. For any benchmark with less than 20 qubits, we run it on real machine. Beyond 20 qubits, we run it using simulation. Both generic applications and VQA applications are included for evaluation.

6.1. Experiment setup

Backend All real-machine experiments are performed on the machine, IBMQ 27-Qubit IBM-Geneva.

For the experiments of large benchmarks with more than 20 qubits, we use the IBM Washington simulator. IBM Washington is the largest near-term 127-qubit architecture. The classical backend machine for simulation has Intel Xeon CPU E5-1607 with 4 cores at 3 GHz.

Since IBM Qiskit simulator does not automatically take crosstalk error into account, we modified it to reflect the crosstalk errors between different links of qubits. Although the IBM Washington simulator can support up to 127 qubits, due to the classical backend machine’s memory and speed limit, we only simulate the benchmarks for qubit number up to 30 qubits and gate number up to 50000.

Metric We use two metric: total variant distance (TVD) [27, 18] and depth. TVD measures the fidelity of the generated circuit. The minimum distance TVD of 0 is achieved when the compiled circuit runs with zero error. The lower the TVD is, the more promising the compiled circuit is. Depth measures the performance of the compiled circuit, that is, how long it takes to run. For depth, we assume each gate takes a unit of time and a SWAP gate consists of three CX gates. Note that the depth not only contributes to the performance, but also the decoherence error. A smaller depth circuit tends to have smaller decoherence errors. Therefore, if other error rates are the same, the smaller the depth is, the better.

Benchmarks The benchmarks used for evaluation are selected from RevLib [38], IBM Qiskit [1], QASMBenche [20], and ScaffCC [15]. We show the qubit and gate number in Table 1.

There are three types of benchmarks. The first type is the generic benchmark. The second type is for 2-local VQA application. We use QAOA [10] for the 2-local VQA benchmark. For QAOA we choose different input-problem graphs ranging from 5 vertices to 30 vertices. The gate number is the same as the edge number in the problem graph. We show the gate number in Table 1 as well.

The third type is N-local VQA, for which we choose Hamiltonian simulation. These are variational quantum eigensolvers (VQE) generated using Pyscf [34]. We choose four different molecules (H2, Li-H, Li-Li, H4) with different basis (sto3g, mingo) to generate Hamiltonian functions. There are six benchmarks in this category.

Baseline For generic applications and QAOA, we use the best-known approach called Xtalk [25] as our baseline. Xtalk optimizes crosstalk at scheduling level. It uses SMT solver to determine where and if barriers should be added to delay the execution. For hardware mapping, we use Sabre [21] which is an efficient mapper integrated in Qiskit. We name this baseline as “Xtalk”.

For VQE applications, we use Paulihedral [22] as our baseline, which is the state-of-art approach to synthesize circuits from Pauli-string specifications.

6.2. Experiment result

We show the overall experiment results in Table 1. We have improvements in fidelity compared with prior work, ranging from 5% to 23%, and depth improvement from 7% to 39%.

Generic applications We first show the TVD results for generic applications in Fig. 11. We have consistently better TVD compared with that generated by Xtalk. On average we improved TVD by 5% and at maximum by 15% for benchmarks like QFT where there are more gates.

From depths in Table 1, we can see further improvement, where we reduce the depth by up to 39% for the 4GT11 benchmark. It is mainly because instead of only adding a barrier for crosstalk mitigation, we exploit the hardware mapping opportunities.

Moreover, it is worth mentioning that the SMT solver may not be able to run large-scale circuit. For example, for the QFT20 benchmark, it can not return a result within a reasonable amount of time, for instance, 1 hour, while our method can compile the QFT20 circuit and generate a reasonable compiled circuit.

We show a comparison of compilation time in Fig. 14. Our compiler takes 1% of the prior work’s compilation time in most cases. The scalability of the compiler is also important, especially current quantum machines are expected to scale beyond 1,000 qubits in a couple of years.
Variational Quantum Algorithms  We show TVD results for QAOA in Fig. 12, and for VQE in Fig. 13. For QAOA, we have the TVD improvement ranging from 10% to 15%. Since Xtalk failed to compile for the 25-qubit and 30-qubit case due to the compilation time overhead, we do not have TVD result for Xtalk in these two cases.

For VQE, we find even more TVD and depth improvement compared with the state-of-the-art. It is because for VQE, we have more optimization opportunities at circuit synthesis stage.

For VQE, we have TVD improvement ranging from 15% to 23%. And we can also find that CQC takes 60% depth compared with Paulihedral in some benchmarks and 69% on average depth.

From the results, we can see that the compiled quantum circuit’s fidelity (calculated as 1-TVD) drops below 30% when
### Table 1: Overview of Experimental Results

| Benchmark | Qubits | QAOA | CQCC | Xtalk/Pauli-hedral |
|-----------|--------|------|------|-------------------|
| H2        | 4      | 15   | 40   | 0.19              |
| H2-minao  | 4      | 25   | 72   | 0.23              |
| H4        | 8      | 316  | 390  | 0.36              |
| H4-minao  | 8      | 362  | 1381 | 0.65              |
| Li-H      | 12     | 631  | 3117 | 0.72              |
| Li2       | 16     | 2980 | 19850| 0.89              |

we have QAOA with 30 vertices and 150 edges, or Li2 with 26 qubit and 2980 Pauli strings. However, Paulihedral’s fidelity drops to 5%. That means our work outperforms the state-of-the-art by improving fidelity by 6X.

### 7. Related work

A vast body of prior work exists on physical and software have been proposed to mitigate the crosstalk problem. There are mainly two categories of studies which focus on different parts: 1) Physical level mitigation: connectivity reduction [8] or frequency tuning [8]; 2) The other study focus on the software level which is to delay gates [25] or to perform pulse-level optimization [39]. The first category focuses on physical level which has strict physical requirements, the methods might not suit all the machines. For example some machine architecture have been decided and there are some extra costs when tune the frequency of the qubits [35]. The second category is at the software level, although delaying gate seems promising to reduce the crosstalk-error [25], it might increase the decoherence error [32] due to longer execution depths.

However, all prior work takes it for granted that existing hardware mapping methods [26, 21] or circuit synthesis methods are good enough without considering crosstalk mitigation. So they are doing the crosstalk mitigation all after the mapping and inserting swaps process. However, far too little attention has been paid to take the crosstalk-error into consideration for all mapping and inserting swap methods, which leaves a new work for a new crosstalk-aware mapping strategy which take crosstalk into consideration when they map the logical qubits to physical qubits and inserting swaps. Although a lot of work exists for mapping logical qubit to physical qubit and inserting swaps, like (Sabre [21], the one by Zulhner et al. [40]). These methods are considering minimizing the decoherence error by decreasing the number of inserting swaps instead of considering crosstalk. So we are first to build a new crosstalk-aware mapping framework which minimize the crosstalk error in the mapping process and circuit synthesis stage, which can have a significant advantage compared to the prior work since a good mapping process or synthesized circuit can already mitigate or completely remove the crosstalk errors which can eventually decrease the depths and decoherence error.

To the best of our knowledge, this is the first work to build a crosstalk-aware mapping method which consider the crosstalk error and have a better performance(error rate/deptches) compared to prior work. It first considers mitigating crosstalk error together with schedule gates/inserting swaps and mapping. Also our work first use commutative to schedule gates to avoid crosstalk error without any extra cost.

### 8. Conclusion

Crosstalk remains one of the major contributing factors for the high error rate of contemporary superconducting NISQ devices. Existing studies consider crosstalk at the scheduling stage or pulse generation stage compilation, leading to suboptimal performance and/or fidelity. This paper presents the first crosstalk-aware quantum program compilation framework CQCC that comprehensively addresses circuit synthesis, qubit routing, and crosstalk effect altogether during the compilation. Evaluations on real NISQ machines demonstrate up to 23% error rate reduction with 60% circuit depth compared to state-of-the-art approaches.

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