A high-precision time-to-digital converter applied to CDC

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Abstract—This paper presents a high-precision CMOS time-to-digital converter (TDC) applied to a capacitance-to-digital converter (CDC). The time-to-digital converter in the capacitance-to-digital converter is used to measure the time interval between the charging time of the capacitor under test and the charging time of the internal reference capacitor. The time resolution of the TDC directly determines the capacitance resolution of the CDC. In order to improve the measurement resolution of TDC, a TDC structure based on phase-locked loop (PLL) is proposed. This paper first gives a capacitance-to-digital converter scheme, and then introduces the time-to-digital converter used in the scheme. The frequency multiplication technology of the phase-locked loop optimizes the integral nonlinearity (INL) of the interpolator and greatly improves the interpolation of the interpolation ratio. The TDC was realized in a 0.13-μm CMOS process, and the measurable time interval is 21.14μs. When the external reference clock is 200MHz, the resolution is 40.3ps and only 31 delay units are needed.

1. INTRODUCTION

With the widespread application of the Internet of Things (IoT) technology, such as implantable biomedical systems [1] and automatic environmental monitoring facilities [2], various sensing circuits and very low power consumption are required. Capacitive sensors are very suitable for such applications because they only consume dynamic power and can measure a variety of physical factors [3]. Capacitance-to-Digital Converter (CDC) is an indispensable part of capacitive sensing circuit, which realizes the conversion of capacitance value to digital quantity. For high-performance capacitance-to-digital converters, resolution and precision are two very important parameters. There are many ways to implement CDC. Here we introduce a TDC-based CDC solution.
Figure 1 shows the overall schematic diagram of the TDC-based CDC scheme. The basic idea is to first use the known cancellation capacitance CB to cancel the unknown parasitic capacitance CP, and then convert the variation of the capacitance CX to be measured into a time difference, and then convert the time difference into a number through the TDC module. The system is divided into two states, current self-calibration state and measurement state. When the two charging times are equal, it means that the parasitic capacitance CP has been cancelled out, and the VCX and VCP in Figure 1 arrived at the same moment. The system can now enter the measurement state.

The IREF in Figure 1 is the reference current, which is usually generated by the output voltage VR of the band gap reference source and the ideal resistance outside the chip. Generally, the proportional relationship K2 between ICB and IREF is fixed, and the proportional relationship K1 between ICX and IREF is controlled by controlling the DAC. When the switch K is not turned on, the charging time of the left and right channels is equal, which can be expressed as (1):

$$T_{eq} = \frac{VR \times CP}{K1 \times IREF} = \frac{VR \times CB}{K2 \times IREF} = T_{eq}$$ (1)

In general, VR in (1) is generated by a bandgap reference voltage source and a reference current IREF is generated at the same time, so the proportional relationship between VR and IREF, RB, is fixed. Then (1) can be simplified to (2):

$$T_{eq} = \frac{RB \times CP}{K1} = \frac{RB \times CB}{K2} = T_{eq}$$ (2)

When the switch is turned on, the capacitor CX to be measured is connected to the left charging circuit, and the total capacitance value of the left circuit changes, and there must be a time difference between the arrival time of VCX and VCP. Refer to (2), the time difference can be expressed as (3):

$$\Delta T = \frac{RB \times CX}{K1}$$ (3)

The corresponding quantitative data is (4):

$$\Delta N = \frac{1}{K1} \times \frac{RB \times CX}{TCK}$$ (4)
TCK in (4) is the reference clock of the TDC circuit. In the general TDC scheme, the quantization of the time interval is achieved by calculating the number of full cycles of the reference clock in the time interval. To improve the resolution, a very high clock frequency is required, and the power dissipation is greatly increased. This is what we don’t want to see. This article introduces a TDC structure based on a phase-locked loop. Through frequency multiplication technology and interpolator, under the premise of a lower reference clock, the resolution of TDC is greatly improved.

Time-to-Digital Converter (TDC) has been widely used in nuclear physics and high-energy physics experiments and the fields related to time measurement [4], such as communication, spectrum analysis, pulse laser flight time measurement and capacitance detection circuit. Compared with other forms of time interval measurement technology, TDC has higher performance and silicon utilization.

The time interval between time boundary signals (start/stop) can be obtained by calculating the number of cycles of the reference clock in the time interval. At the same time, by interpolating the reference clock period, the measurement resolution can be effectively improved, making it possible to use a low-frequency reference clock, thereby reducing power dissipation.

High-precision TDC measurement methods are carried out with counters and interpolators. For high-precision time interval measurement, there are many interpolator structures, which can be roughly divided into linear interpolators and ring interpolators. At present, good results have been achieved based on the ring interpolation structure. The ring structure allows a clock signal to be repeatedly transmitted in the loop, which greatly reduces the number of delay units. Using this feature, the time interval to be measured can be expanded as needed without increasing the length of the TDC. Therefore, compared with linear TDC, ring TDC meets higher requirements with lower complexity and cost.

2. Interpolation technology based on phase locked loop

2.1. Operation and realization principle

The precise reference clock period can be divided into multiple shorter time lengths using the multi-phase output function of the phase-locked loop. The time boundary signal arrives at any time within the reference clock period, and the phase state of the phase-locked loop at this moment is recorded. Compared with using the full cycles of the reference clock to calculate the time interval, this method can greatly improve the resolution.

![PLL Interpolator](image)

The time interval measurement scheme based on the phase-locked loop is implemented by a counter and an interpolator acted by the phase-locked loop. The phase-locked loop in Figure 2 divides a reference clock period $\tau_{ref}$ into 10 time segments, The length of each segment is $\tau_1$. When the time boundary signal arrives, the phase state of the phase-locked loop is recorded, and the counter counts the number of full cycles of the reference clock in the time interval. The time interval between the time boundary signals (start and stop) is represented by the counter result $T_{CONT}$ and the interpolation result, such as (5):

$$T = T_{CONT} \times \tau_{ref} + \left(P_{stop} - P_{start}\right) \times \tau_1$$  \hspace{1cm} (5)
The TDC structure introduced in the article is shown in Figure 3. The ring oscillator in the phase-locked loop is composed of 31 delay elements, which can generate 62 phases, which greatly improves the interpolation ratio and resolution. Frequency multiplication technology makes it possible for the system to work on a low-frequency reference clock. The 31-bit register can instantly record the phase status when the time boundary signal comes, and at the same time obtain the phase difference in the 6-bit register. The 13-bit counter is enabled by the start signal and stopped by the stop signal. The delay time of the delay elements is usually adjustable, and the required delay can be provided according to different working conditions.

2.2. The frequency multiplication technology of PLL
In a traditional phase-locked loop, in order to achieve a higher resolution, a higher system frequency is usually required, which causes a larger power dissipation. After dividing the output frequency of the ring oscillator by N and connecting it to the input of the phase detector, the divided frequency is synchronized with the reference frequency. This operation makes the frequency of the ring oscillator reach the effect of N multiplication. The power dissipation is reduced, and the number of delay units in the oscillator is reduced to the original 1/N, which greatly weakens the influence of integral nonlinearity on measurement accuracy. This method of frequency multiplication is also often used in delay-locked loops, which manifests as frequency multiplication DLL or cyclic DLL, especially used in clock multiplication circuits [7]-[9].

2.3. Delay elements
The delay time of the delay element in the voltage-controlled oscillator is regulated by the voltage. The structure is shown in Figure 4, which consists of two parallel-connected delay adjustable inverter and two smaller inverters [10]. In order to match the delay, the structure of all elements is the same. The differential structure has many advantages, such as improving resolution and reducing noise [11].
3. Interpolation accuracy
The interpolation accuracy of TDC is usually determined by the quantization error and the nonlinearity of the interpolation circuit. When the time boundary signal is at different positions of the interpolator, these non-ideal factors are different, which leads to the error between the measurement result and the ideal value.

The CDC scheme introduced in the article charges and discharges the capacitor periodically, which means that the time boundary signal of the TDC is generated repeatedly, which allows multiple measurements at the same time interval. The standard deviation of the measurement results can represent the accuracy of the interpolation circuit, and the absolute length of the time interval will also affect the accuracy. For the stability of accuracy, it is analyzed by doing root-mean-square around the theoretical value. The accuracy of a single signal is usually expressed by σ. Among the factors that affect the accuracy of a single signal, integral nonlinearity and quantization error are usually dominant.

3.1. Quantization Noise
For time interval measurement systems like TDC, the quantization noise is usually caused by resolution. No matter how to improve the resolution, the LSB is still a finite value, and the time boundary signal will reach the TDC at any time within the clock cycle, so the quantization noise appears as an uncertainty value of up to ±1LSB in a single measurement result.

If the time interval T is regarded as a multiple of the clock period T0, it can be expressed as (6):

\[ T = T_0 \times (Q + F) \quad (6) \]

In (6), Q is an integer multiple of T0, and F is a fractional multiple of T0 (0≤F≤1). For accuracy σ, it is usually affected by the fractional part F, and the function relationship can be approximated to (7)

\[ \sigma = T_0 \sqrt{F(1-F)} \quad (7) \]

In a period of T0, integrating the change of σ² will get the root mean square value T0/√6.

3.2. Integral nonlinearity of interpolator
In the IC manufacturing process, the parameters are often uneven, the layout is diverse, and system interference will also cause some noise. These factors will cause the static difference in the delay time of the delay element, which is expressed as differential nonlinearity in the system. When passed through the interpolator, differential nonlinearity will accumulate as integral nonlinearity (INL). After the PLL is stable, the output frequency is matched to the reference frequency, and the INL starts to accumulate from the beginning of the PLL operation. The maximum value of INL error generally appears at the midpoint of the interpolator. The integral nonlinearity is related to the difference of the individual delay time and the length of the interpolator. Through the unified structure of all delay units and a reasonable layout, the difference in delay time can be effectively reduced. Shortening the length of the interpolator can reduce the INL error on the one hand, but on the other hand, it reduces the resolution. Therefore, it is not enough to shorten the length of the interpolator. It also requires the frequency multiplication technology of PLL introduced above. It can effectively reduce the INL error without affecting the resolution. Figure 5 and Figure 6 show the differential nonlinearity and integral nonlinearity of the interpolator.
3.3. Time resolution
After the PLL is stable, in order to match the reference frequency, the charge pump generates a corresponding control voltage \( V_{\text{ctrl}} \) to control the VCO. Figure 7 shows the corresponding output frequency of the VCO under different control voltages \( V_{\text{ctrl}} \). It can be seen from Figure 7 that when the system reference frequency is 200MHz, the output frequency \( f_{\text{out}} \) of the interpolator is 400MHz through the frequency multiplication technology of PLL, which can provide a resolution of 40.3ps.

When the resolution is 40.3ps, by averaging 50 measurement results, the corresponding relationship between different time intervals and TDC output data is obtained, as shown in Figure 8. Figure 8 tested every 10ps in the time interval from 0 to 12ns, and the corresponding TDC output data showed good linearity.
Figure 8. Linear relationship between different time intervals and TDC output data
The stability of the resolution is worthy of further testing. Here, in the maximum time interval of 12ns, 300 sets of output data have been recorded, and the resolution of each set of data has been counted. As shown in Figure 9, the average resolution is 40.25ps.

Figure 9. TDC Resolution

3.4. Random noise
When the PLL starts to work, random noise will show up. The external reference signal has phase noise, which will affect the delay time of the delay element, thereby affecting the frequency of the output signal of the interpolator. Random noise is caused by the random jitter of the reference signal, which is inevitable, but it can be averaged after multiple tests at the same time interval, which can effectively reduce the random noise.

Table 1. Summary of TDC parameters and performance

| Power supply voltage | 1.2V       |
|----------------------|------------|
| Process              | 0.13μm CMOS|
| Frequency reference  | 200MHz     |
| Internal virtual frequency | 400MHz |
Some parameters and performance of TDC are given in Table 1.

### Table 1

| Parameter                          | Value       |
|------------------------------------|-------------|
| Number of delay elements           | 31          |
| Maximum INL for $t_0=40.3$ps       | ±50ps       |
| TDC resolution                     | 40.3ps      |

4. Conclusion

A time-to-digital converter applied to CDC realized by 0.13μm CMOS process. The resolution is 40.3ps, and the measurement range is 21.14μs. The circuit uses an external reference frequency of 200MHz and only uses 31 effective delay elements.

Various methods are used to obtain high interpolation ratio and low nonlinearity. One of them is the use of a ring oscillator structure, which effectively expands the interpolation ratio to twice the linear structure. Frequency multiplication technology of PLL reduces the number of delay element, thereby reducing the size and non-linearity of the TDC, and at the same time making a low reference frequency possible, effectively reducing power dissipation. The advanced delay element structure adopts a differential structure to improve the resolution while reducing noise.

Through the test, the scheme has lower nonlinear error and higher accuracy. It is very suitable for application under the CDC scheme, and has a higher effect on improving the resolution of CDC measurement.

Acknowledgements

This work has been strongly supported by Shenyang University of Technology.

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