GPU Based Parallel Ising Computing for Combinatorial Optimization Problems in VLSI Physical Design

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Abstract—In VLSI physical design, many algorithms require the solution of difficult combinatorial optimization problems such as max/min-cut, max-flow problems etc. Due to the vast number of elements typically found in this problem domain, these problems are computationally intractable leading to the use of approximate solutions. In this work, we explore the Ising spin glass model as a solution methodology for hard combinatorial optimization problems using the general purpose GPU (GPGPU). The Ising model is a mathematical model of ferromagnetism in statistical mechanics. Ising computing finds a minimum energy state for the Ising model which essentially corresponds to the expected optimal solution of the original problem. Ising computing is one of the proposed applications for quantum annealing computing and many combinatorial optimization problems can be mapped into the Ising model. In our work, we focus on the max-cut problem as it is relevant to many VLSI physical design problems. Our method is motivated by the observation that Ising computing by the annealing process is very amenable to fine-grain GPU based parallel computing. We will illustrate how the natural randomness of GPU thread scheduling can be exploited during the annealing process to create random update patterns and allow better GPU resource utilization. Furthermore, the proposed GPU-based Ising computing can handle any general Ising graph with arbitrary connections, which was shown to be difficult for existing FPGA and other hardware based implementation methods. Numerical results show that the proposed GPU Ising max-cut solver can deliver more than 2000X speedup over the CPU version of the algorithm on some large examples, which shows huge performance improvement potential for addressing many hard optimization algorithms for practical VLSI physical design.

I. INTRODUCTION

There are many hard combinatorial optimization problems such as max-flow, max-cut, graph partitioning, satisfiability, and tree based problems, which are important for many scientific and engineering applications. With respect to VLSI physical designs, these problems translate to finding optimal solutions for cell placement, wire routing, logic minimization, via minimization, and many others. The vast complexity of modern integrated circuits (ICs), some having millions or even billions of integrated devices, means that these problems are almost always computationally intractable and require heuristic and analytical methods to find approximate solutions. It is well-known that traditional von Neumann based computing can not deterministically find polynomial time solutions to these hard problems [1].

To mitigate this problem, a new computing paradigm utilizing the Ising spin glass model or Ising model has been proposed [2]. The Ising model is a mathematical model describing interactions between magnetic spins in a 2D lattice [3]. The model consists of spins, each spin will take one of two values \{+1,-1\} (to present up and down states of a spin along a preferred axis) and spins are generally arranged in a 2D lattice. The spin’s value is determined so that its energy is minimized based on interactions with its neighbor spins. Such local spin updates will lead to the expected optimized solution, which is typically presented as the ground state (globally lowest energy configuration) of the Ising model. It was shown that many computationally intractable problems (such as those in class NP complete or NP hard) can be converted into Ising models [4]. Some natural processes, such as quantum annealing process, were proposed as an effective way for finding such a ground state [5], [6]. D-Wave [7] is one such quantum annealing process solver based on the Ising model and it shows $10^8$ speedup over simulated annealing on the weak-string cluster pair problem [8]. However, existing quantum annealing requires close to absolute zero temperature operating on superconductive devices, which are very complicated and expensive.

While Quantum computing has yet to reach maturity, there exists a number of other hardware-based annealing solutions which have been proposed to exploit the highly parallel nature of the annealing process in the Ising model. In [9], a novel CMOS based annealing solver was proposed in which a SRAM cell is used to represent each spin and thermal annealing process was emulated to find the ground state. In [10], [11], the FPGA-based Ising computing solver has been proposed to implement the simulated annealing process. However, those hardware based Ising model annealing solvers suffer several problems. First, the Ising model for many practical problems can lead to very large connections among Ising spins or cells. Furthermore, embedding those connections into the fixed 2-dimensional fixed degree spin arrays in VLSI chips is a not trivial problem and requires mitigation techniques such as cell cloning and splitting as proposed in [10], [11].

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Second, ASIC implementations are not flexible and can only handle a specific problem and FPGA implementations require architectural redesign for different problems. Third, one has to design hardware for the random number generator for each spin cell and simulate the temperature changes, which has significant chip area costs which resulting in scalability degradation.

Based on the above observations and the highly parallel nature of the Ising model, in this work, we explore the General Purpose Graphics Processing Unit (GPGPU or more simply GPU) as the Ising model annealing computing platform. The GPU is a general computing platform, which can provide much more flexibility over VLSI hardware based annealing solutions as a GPGPU can be programmed in a more general way, enabling it to handle any problem that can be mapped to the Ising model. That is, it is not restricted by the topology or complex connections that some problems may have. At the same time, it provides massive parallelisms compared to existing CPUs. The GPU is an architecture that utilizes large amounts of compute cores to achieve high throughput performance. This allows for very good performance when computing algorithms that are amenable to parallel computation while also having very large data sets which can occupy the computational resources of the GPGPU [12], [13]. The problem sizes in the physical design domain can easily accomplish this and heuristic methods can solve the Ising model in a parallel manner which makes the GPU ideal for this application. We remark that extensive work for Ising computing on GPGPUs have been proposed already [14]–[16], however; they still focus on Physics problems which assume a nearest neighbor model only. This model, is highly amenable to the GPU computing as it is easily load balanced across threads but is not general enough to handle problems such as max-cut. Furthermore, many GPU based methods use a checkerboard update scheme, but this is still only practical for the nearest neighbor model without using complicated graph embedding.

In this paper we propose a GPGPU-based Ising model solver, using a modified simulated annealing heuristic, that can handle any general problem. We focus on the max-cut problem as it is relevant to many VLSI physical design problems. We show that Ising computing by the simulated annealing process is very amenable to fine-grain GPU based parallel computing. We further propose an update method that utilizes the GPGPU scheduler to achieve a random update pattern. This allows us to maximize thread utilization while also avoiding sequential and deterministic update patterns for a more natural annealing process. Furthermore, new GPU-based Ising computing algorithm can handle any general Ising graph with generally connected spins, which was shown to be difficult for FPGA and other hardware based implementation methods. Our numerical results show that the proposed GPU Ising solver for max-cut problem can deliver more than 2000X speedup over the CPU version of the algorithm on some large examples, which shows huge potential for performance improvement for solving many practical VLSI physical design hard optimization algorithms.

II. ISING MODEL AND ISING COMPUTING

A. Ising model overview

The Ising model consists of a set of spins interconnected with each other by a weighted edge. For the general Ising model, these connections of the spins can take any topology. One of the connection topologies is the 2D lattice, referred to as the nearest neighbor model, shown in Fig. 1 which describes the ferromagnetic interactions between so-called spin glasses. Many computationally intractable problems can be mapped to this Ising model. It was shown that finding the ground state in 2D lattice Ising model using is an NP-hard problem [17]. However, it has certain characteristics that make it more amenable to the annealing process as each update results in energy minimization and spin glass updates can be performed in a highly parallel manner.

![Fig. 1: The 2D nearest neighbor Ising model.](image)

Specifically, each spin $\sigma_i$, has two discrete spin values $\sigma_i \in \{-1, 1\}$ and some interaction with adjacent spins in the form of a weighted edge. Then the local energy or Hamiltonian of the spin is described by (1):

$$H_i(\sigma_i) = \sum_j J_{i,j} \sigma_i \sigma_j - h_i \sigma_i$$  \hspace{1cm} (1)

In this equation, $J_{i,j}$ is the interaction weight between $\sigma_i$ and $\sigma_j$, and $h_i$ is a bias or external force acting on $\sigma_i$. By find the minimum value of $H_i(\sigma_i)$, we can determine the local spin value $\sigma_i$. Specifically (1) can be written as

$$H_i(\sigma_i) = \left( \sum_j J_{i,j} \sigma_j - h_i \right) \sigma_i = -S \sigma_i$$  \hspace{1cm} (2)

From (2), we can see that $\sigma_i$ can be determined just from the sign of the $S$ value. If $S > 0$, $\sigma_i = -1$, otherwise, $\sigma = -1$. If $S = 0$, it can take any value of $-1, 1$. We note that such update for obtaining the minimum value of $H_i(\sigma_i)$ only depends on its neighbors. As a result, all the spin updates can be done independently and thus in parallel.

Then the global energy of the whole Ising model is given by the following (3), where $\langle i,j \rangle$ indicates the combination of all spin interactions.

$$H = \sum_{\langle i,j \rangle} J_{i,j} \sigma_i \sigma_j - \sum_i h_i \sigma_i$$  \hspace{1cm} (3)
As mentioned before, finding the minimum energy state of Ising model problem is an NP-hard problem. For this reason, it is practical to use heuristic methods, or analytical methods, to find approximate solutions close to the minimal energy state. Previous methods have focuses on solving the nearest neighbor Ising model [9]–[11]. However, this model has the drawback of not being able to handle any general problem which may have arbitrary and complex connections. Therefore, in this work, we assume that a spin glass’s connections, or edges, are able to connect to any other spin glass in the model, an example of which is shown in Fig. 2. Using this more general model removes the nearest neighbor restriction on the Ising model and allows us to handle more complex problems.

![Fig. 2: An example of a generally connected Ising model.](image)

B. Annealing method for Ising model solution

A classical and well known heuristic for combinatorial optimization is Simulated Annealing (SA). This heuristic mimics the behavior of thermal annealing, found in metallurgy. Essentially, it works by setting the environment to a high "temperature", giving the model high energy and allowing for higher probability of changing states, and then gradually decreases the temperature as the simulation runs. More precisely put, it iteratively calculates and evaluates neighbor states of a model and probabilistically determines whether to keep the new state or reject it based on the Metropolis algorithm and decreasing "temperature" which helps it avoid local minima which are depicted in Fig. 3.

While classical SA could be used to find the Ising model ground state, we use a modified annealing method that better exploits the Ising model while also being more amenable to parallel implementation. Furthermore, unlike the classical SA method, where each step requires the computation of a neighbor state which may or may not decrease the energy, every spin update in the Ising model will reduce the local energy of the spin. Because of this, there is no reason to utilize the Metropolis criteria to accept or reject states which do not minimize the model’s energy.

In algorithm 1, \( M \) is the maximum number of sweeps, \( N \) is the number of glasses to randomly flip, and \( S \) is the set of all spin glasses. Once the spin glasses are initialized, all spin glasses are updated iteratively to propagate the interactions between each glass (which we’ll call a “sweep”). After each sweep is finished, \( N \) glasses are randomly flipped and \( N \) is decreased according to an annealing schedule. After this, the process is repeated for \( M \) sweeps or until convergence is achieved.

Following this process, the local energy of each spin glass, and thus the global energy of the model, is gradually decreased. Furthermore, we avoid the local minima by introducing energy to the model by using random flips which slowly decrease over time.

III. Problem Description

The Ising model and the method introduced in this paper can be applied to many NP class problems, however, we use the max-cut problem as a practical example. The max-cut problem, in practice, can help find solutions to several EDA and VLSI design problems. For example, the general via minimization problem, the act of assigning wire segments to layers of metallization such that the number of vias is minimized, can be modeled as a max-cut problem [18], [19].

The max-cut problem is defined as partitioning a graph into two subsets \( S \) and \( S' \) such that the weighted edges between the vertices of one subset and the other subset are maximized. This is mathematically formulated by assuming a graph \( G = (V, E) \) has a variable \( x_i \) assigned to each vertex:
\[
max \frac{1}{2} \sum_{i,j \in V, i < j} w_{i,j} (1 - x_i x_j) \\
\text{s.t. } x_i \in \{1, -1\}
\]  

(4)

In this equation, \(V\) is the set of vertices in the graph \(G\), \(w_{i,j}\) is the edge weights in \(E\) between the \(i\)th and \(j\)th elements in \(V\), and \(x_i\) is an indication of which subset the vertex belongs in and can take the values \(\{-1, 1\}\).

Intuitively, looking at the Ising spin glass problem in (3), we can see how the max-cut problem should map to the Ising model by associating the spin of a spin glass \(\sigma_i\) with a subset of the graph in the max-cut problem. That is, we can say that if a spin is 1 then the glass is in \(S\) and if a spin is \(-1\) then the glass is in \(\bar{S}\), which is analogous to \(x_i\). Furthermore, the weights between vertices \(w_{i,j}\) is the same as the interaction weights between spin glasses \(J_{i,j}\) and, in this case, there is no bias or external force so the \(h\) term in the Ising model is simply zero. The global energy minimization of the Ising model for the Max-cut problem is shown below in (5).

\[
H = - \sum_{(i,j)} J_{i,j} \sigma_i \sigma_j
\]

(5)

Once mapped to the Ising model, the max-cut problem can then be solved by finding the ground state of the model using the methods proposed in this paper. While there are other ways to solve this problem, the method we propose is highly amenable to parallel computation and large problem sets have great performance when implemented on the GPU, thus, giving our method an advantage in scalability.

IV. GPU IMPLEMENTATION

A. GPU Architecture

The general purpose GPU is an architecture designed for highly parallel workloads which is leveraged by Nvidia’s CUDA, Compute Unified Device Architecture, programming model [12]. The Nvidia GPU architecture is comprised of several Symmetric Multiprocessors (SMs), each containing a number of “CUDA” cores, and a very large amount of DRAM global memory [13]. The Kepler architecture based Tesla K40c GPU, for example, has 15 SMs for a total of 3072 CUDA cores (192 cores per SM), and 12GB DRAM global memory. Additionally, each SM has additionally special function units, shared memory, and cache.

The CUDA programming model, shown in Fig. 4, extends the C language adding support for thread and memory allocation and also the essential functions for driving the GPU [20]. The model makes a distinction between the host and device or the CPU and GPU respectively. The model uses an offloading methodology in which the host can launch a device kernel (the actual GPU program) and also prepare the device for the coming computation, e.g., the host will create the thread organization, allocate memory, and copy data to the device. In practice, a programmer must call many threads which will be used to execute the GPU kernel. Thread organization is therefore extremely important in GPU programming. Threads are organized into blocks which are organized into grids. Each block of threads also has its own shared memory which is accessible to all the threads in that block. Additionally, the threads in the block can also access a global memory on the GPU which is available to all threads across all blocks.

The GPU fundamentally focuses on throughput over speed. This throughput is achieved through the massive compute resources able to be run in parallel. Because of this, it is important to realize that the GPU is not meant for small data sets or extremely complicated operations that may be better suited for a powerful CPU. Instead, the GPU is meant to execute relatively simple instructions on massive data in parallel that can occupy the GPU resources for an extended period of time.

B. Ising model implementation

The GPU, while lacking the massive scaling of a quantum computer, has much larger scaling capabilities than CPUs, allowing it to handle very large problem sizes. Indeed, smaller problems that are unable to fully utilize the GPU resources may achieve worse performance than a CPU.

In order to ensure the best utilization of GPU resources, it is necessary to devise a spin glass update scheme more amenable to parallel computation. Algorithm 1 relies on sequential updates to propagate the interactions between the spin glasses. However, this would be highly inefficient on the GPU as it would mean each thread would have to wait for previous threads to update.

In previous works that have addressed the nearest neighbor Ising model, a checkerboard update scheme is implemented which allows for many spin glasses to be updated in parallel [16]. While the spin glass updates are independent of their neighbors, they are not truly independent since the update pattern is deterministic and can introduce autocorrelation between spin updates but this autocorrelation generally does not affect the global balance of the model [16]. For the problem

![Fig. 4: The Nvidia CUDA programming model showing the Host (CPU) and Device (GPU) and the relation between threads, blocks, and grids.](image-url)
addressed in this work, however; interactions are not confined to nearest neighbors nor are they restricted to regular patterns. This results in very complex interactions in which spins can be dependent on many other spins across the entire model. Consequently, a different update scheme must be developed for such a general solver.

To address the above mentioned issues, we modify the original algorithm in algorithm 1. Firstly, we assign each thread to a single spin glass, and make it responsible for updating that glass. One may notice that since each spin glass may have a different number of neighbors, then the threads will not be perfectly load balanced. However, the alternative is to use graph minor embedding, another NP-hard problem [21], to create clone nodes such that every thread will have an equal number of updates [10]. However, this means that we need to have the GPU do some intensive pre-processing on the model, and it also means that after each update sweep, a reduction must be performed on each spin glass’s clones so that the true spin value can be determined. For these reasons, it is much better to allow for some load imbalance and suffer some computational penalty on the GPU, instead of increasing the complexity of the algorithm. Furthermore, we do not synchronize our thread updates. In practice, this means that threads will update their assigned spin glass as soon as they are scheduled and will use whatever spin status their respective neighbors have at the time of data access. Therefore, there is no guarantee that a spin’s neighbors will have been updated during a particular sweep. This naturally propagates the updates of each spin glass in a non-deterministic pattern which reduces autocorrelation of the local energy of each spin and enable fines grain computation.

Another major change to the algorithm is the implementation of the random flips. Instead of randomly selecting a number of spin glasses to be flipped at the end of an update sweep, we let each thread decide if it should flip or not. A global variable, visible to all threads, gives the flip probability in the form of a floating point number between 0.0 and 1.0. Each thread then grabs a random number between 0.0 and 1.0, generated by the CUDA cuRAND library for efficient random number generation, and flips if the number is below the global flip probability. The cuRAND library allows us to generate sequences of random numbers at the very beginning of the program and stores these sequences in global memory. This adds a one time computation cost but is very small as the GPU utilizes its massive compute resources to generate these numbers. Furthermore, because we only need to generate these numbers once, our threads are able to simply read a memory address which returns a random number that is independent of all other threads, so the thread level random number generation is extremely efficient during the annealing process. Again, this allows us to avoid synchronization since each thread is responsible for its own flipping and can decide to flip or not as soon as it finishes its update without waiting for other threads which may still be updating. Consequently, a thread may not only update using an already updated neighbor, it may actually update using a neighbor that has been randomly flipped also. The flip probability is then reduced as update sweeps are completed.

In algorithm 2, the parallel simulated annealing solver for the Ising model is presented. While mostly similar to the algorithm 1, there are some differences. We replace the number of random flips input with a variable \( F_p \), which represents the flip probability mentioned above. Next, we have each thread grab a random number, from the cuRAND pre-generated random number sequence, between 0.0 and 1.0 and compare this to \( F_p \). If it is less, then the thread will flip the spin value. While these changes are subtle, the effect is large as it allows the parallel computation of an entire update sweep.

### V. Experimental Results

In this section, we present the experimental results showing both the accuracy and speed of our parallel GPU-based Ising model solver for the max-cut problem. The CPU-based solution is done using a Linux server with 2 Xeon processors, each having 8 cores (2 threads per core) and a total of 32 threads, and 72 GB of memory. On the same server, we also implement the GPU-based solver using the Nvidia Tesla K40c GPU which has 3072 CUDA cores and 12 GB of memory. Test problems from the G-set benchmark [22] are used for testing as well as some custom made problems to show very large cases. The problems’ edge counts are used to represent their size as the size of each problem is dominated by the number of edges.

#### A. Accuracy study

To test the accuracy of the method presented in this paper, we compare the max-cut value our method generates with that of the best known solution in the G-set benchmark.

For the results in Table I, average cut values were obtained by running the GPU solver several times. From the table, we can see that the GPU consistently performs well with almost all results above 90%. We also note that in practice, the best result could be picked form a number of simulations and some simulation parameters could be tuned to achieve better results, e.g., annealing schedule and initial flip probability. However, we present average results of a parameter configuration we found to be consistent across many graphs.

In Fig. 5 the region of convergence is shown for the proposed method and was obtained by running the solver several times for a particular problem. The red line shows the lowest observed accuracy while the green line shows the highest observed accuracy. One example run is also included to show the overall behavior of the convergence. Unlike classic

### Algorithm 2 GPU Simulated Annealing method for Ising model

| Algorithm 1 | GPU Simulated Annealing method for Ising model |
|-------------|--------------------------------------------------|
| input: \((F_p, S)\) | initialize ALL \(\sigma_i\) in \(S\) |
| while \(F_p > 0\) do | |
| for all \(\sigma_i \in S\) in parallel do | |
| \(\sigma_i \leftarrow \text{argmin}(H(\sigma_i))\) | |
| flip \(\sigma_i\) with probability \(F_p\) | |
| end for | |
| reduce \(F_p\) | |
| end while | |
TABLE I: Accuracy comparison of the GPU max-cut value against the best known cut values for the G-set benchmark.

| Graph | Best known cut | GPU Ising cut (%accuracy) |
|-------|----------------|---------------------------|
| G13   | 580            | 522(90.0%)                |
| G34   | 1372           | 1191(86.8%)               |
| G19   | 903            | 844(93.5%)                |
| G21   | 931            | 880(94.6%)                |
| G20   | 941            | 880(93.6%)                |
| G18   | 968            | 938(94.9%)                |
| G51   | 3846           | 3754(97.6%)               |
| G53   | 3846           | 3756(97.7%)               |
| G54   | 3846           | 3756(97.7%)               |
| G50   | 5880           | 5803(98.7%)               |
| G47   | 6656           | 6619(99.4%)               |
| G40   | 2387           | 2267(94.7%)               |
| G39   | 2395           | 2269(94.7%)               |
| G42   | 2469           | 2325(94.2%)               |
| G41   | 2398           | 2284(95.2%)               |
| G9    | 2048           | 2004(97.9%)               |
| G31   | 3288           | 3227(98.2%)               |

Fig. 5: Convergence region of the GPU-based annealing for the Ising model on the G-set G47 problem.

SA, the solver does not converge to a single state but rather it continues to have minor variations in energy as the solver progresses. This is because of the utilization of the GPU scheduler as the random update pattern which means there is always some extra energy being added to the model, even when the number of random flips is small or zero.

B. Performance study

The speed of our method is judged by measuring how long it takes to perform a number of update sweeps on various sized models. We run both the proposed GPU-based method and the sequential CPU implementation of the algorithm for 1000 sweeps and compare the computation time. Because the GPU performs best when its resources are fully utilized, and because it is not optimized for small workloads, we expect to see performance improve as the problem size increases. We also should not expect a large speed-up over a CPU version for smaller problems.

In table II, the time (in seconds) to complete 1000 simulation sweeps is shown for the CPU and GPU for various G-set problems of increasing edge counts. Furthermore, we include several very large custom made and randomly generated non-torus graphs in the table to show the scalability of the proposed method against the CPU-based solution. It should be noted that accuracy results are not included for the custom graphs as there is no data for best known or optimal cut values.

| Graph | # edges | torus | CPU  | GPU  | speed up |
|-------|---------|-------|------|------|----------|
| G13   | 1600    | yes   | 0.17 | 0.11 | 1.5      |
| G34   | 4000    | yes   | 0.29 | 0.11 | 2.6      |
| G19   | 4661    | no    | 0.39 | 0.17 | 2.3      |
| G21   | 4667    | no    | 0.39 | 0.17 | 2.3      |
| G20   | 4672    | no    | 0.39 | 0.15 | 2.6      |
| G18   | 4694    | no    | 0.41 | 0.18 | 2.3      |
| G51   | 5909    | no    | 0.41 | 0.19 | 2.1      |
| G53   | 5914    | no    | 0.41 | 0.20 | 2.0      |
| G54   | 5916    | no    | 0.41 | 0.20 | 2.0      |
| G50   | 6000    | yes   | 0.49 | 0.15 | 3.2      |
| G47   | 9990    | no    | 0.64 | 0.15 | 4.3      |
| G70   | 9999    | no    | 5.34 | 0.34 | 15.7     |
| G57   | 10000   | yes   | 1.44 | 0.15 | 9.3      |
| G40   | 11748   | no    | 4.36 | 0.21 | 20.9     |
| G66   | 18000   | yes   | 4.19 | 0.16 | 27.0     |
| G9    | 19176   | no    | 1.27 | 0.17 | 7.6      |
| G31   | 19990   | no    | 1.16 | 0.16 | 7.4      |
| G57   | 20000   | yes   | 5.06 | 0.16 | 32.5     |
| G77   | 28000   | yes   | 9.64 | 0.16 | 61.8     |
| G59   | 29570   | no    | 4.07 | 0.34 | 11.9     |
| G81   | 40000   | yes   | 19.89| 0.16 | 125.6    |
| G64   | 41459   | no    | 7.97 | 0.39 | 20.6     |
| C1    | 100E3   | no    | 26.63| 0.18 | 147.9    |
| C2    | 250E3   | no    | 59.81| 0.38 | 157.39   |
| C3    | 500E3   | no    | 121.5| 0.61 | 199.5    |
| C4    | 750E3   | no    | 179.87| 0.91 | 197.65   |
| C5    | 1E6     | no    | 234.86| 1.18 | 198.69   |
| C6    | 5E6     | no    | 15638.95| 7.11 | 2200.81  |
| C7    | 7E6     | no    | 20520.72| 9.99 | 2254.74  |

TABLE II: Performance results comparing GPU performance against CPU performance for the G-set benchmark (G prefix) problems and large custom problems (C prefix).
seen as the CPU struggles to handle such large problems while the GPU is able to finish them quite quickly and even achieve over 2000X speedup for the largest problems.

For the most part, as the problem size increased, so did the GPU speed-up. However, we note that there were some graphs which the CPU performed noticeably better than expected and the GPU performed somewhat worse. After further inspection we identified that the solvers had interesting performance depending on the graph structure which prompted further investigation.

We immediately noticed that the performance of both the GPU and CPU was dependent on whether or not the graph was a 2D torus structure. As seen in Fig. 8, the speedup (GPU solver time over CPU solver time) is separated by the graph type, green for a torus and red for a non-torus. By examining this figure, we see that the speedup of the torus structure, which is highly regular, steadily increases as the problem size increases. However, the non-torus structure, while still showing speedup, is more sporadic but generally shows an increase in speedup as the problem size increases.

We further investigate the individual performance of the CPU and GPU by plotting their speed results individually and also separating these results by graph type in Fig. 9 and Fig. 10 respectively. From these graphs we can make a few observations. Firstly, the overall performance of the GPU versus the CPU is dominated by the CPU as the CPU results in Fig. 2 almost exactly follows the overall speedup results. Furthermore, by comparing the two graphs, we see that the CPU performance increases on the non-torus structures while the GPU handles the torus structures very nicely. This can be explained by the regularity of the torus structure which means that the threads in the GPU will be evenly load balanced. The GPU results show that the performance on the torus structures is highly efficient with almost no noticeable change in computation time between the graph with 6000 edges and the graph with over 40000 edges. However, the complexity of the connections in the non-torus graphs hurts the performance of the GPU due to the irregularity of loads on the threads. However, we also note that the effect of the non-torus structure on the GPU is relatively small compared to the effect it has on the CPU.

VI. CONCLUSION

In this work, we have proposed the Ising spin model based computing to solve the max-cut combinatorial optimization problem, which is widely used method for VLSI physical design, on the general purpose GPU (GPGPU). Our new algorithm is based on the observation that Ising computing by the simulated annealing process is very amenable to fine-grain GPU based parallel computing. GPU-based Ising computing provides clear advantage as a general solver over existing hardware-based Ising computing methods that utilize
integrated circuits and FPGAs. We further illustrate how the natural randomness of GPU thread scheduling can be exploited during the annealing process to improve GPU resource utilization. We also showed that GPU-based computing can handle any general Ising graph with arbitrary connections, which was shown to be difficult for FPGA and other hardware based implementation methods. Numerical results show that the proposed GPU Ising max-cut solver can deliver over 2000X speedup over the CPU version of the algorithms over some large examples, which renders this method very appealing for many practical VLSI physical design problems.

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