CoDR: Computation and Data Reuse Aware CNN Accelerator

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Abstract—Computation and Data Reuse is critical for the resource-limited Convolutional Neural Network (CNN) accelerators. This paper presents Universal Computation Reuse to exploit weight sparsity, repetition, and similarity simultaneously in a convolutional layer. Moreover, CoDR decreases the cost of weight memory access by proposing a customized Run-Length Encoding scheme and the number of memory accesses to the intermediate results by introducing an input and output stationary dataflow. Compared to two recent compressed CNN accelerators [5] [1] with the same area of 2.85 mm², CoDR decreases SRAM access by 5.08× and 7.99×, and consumes 3.76× and 6.84× less energy.

Index Terms—CNN acceleration, computation reuse, data reuse, Run-Length Encoding

I. INTRODUCTION

With the increasing complexity of the neural networks, the network model becomes even "deeper," improving the accuracy progressively at the cost of more computation resources and memory space, which requires high-performance processors and high-bandwidth memory systems. As a result, various Convolutional Neural Network (CNN) accelerators are proposed mainly to address two obstacles: (a) convolutional computation throughput, and (b) on-chip data usage efficiency.

To increase the computation throughput, specialized CNN dataflows exploit the characteristics of the network models, such as weight sparsity [1], [5], weight repetition [5], [10], and weight similarity [9]. Fig. 1 illustrates these optimizations in the simple multiplication model of a fully-connected layer. To achieve high efficiency in data transfer (off-chip memory access), previous works [1], [3], [5] show that dataflow of CNNs can be pruned, quantized or compressed. Moreover, CNN accelerators exploit the locality in the off-chip data access by caching the recently-used data. To utilize the on-chip data, various CNN dataflows are proposed: Input Stationary [1], Output Stationary [3], [11], and Weight Stationary [2], [6], in which input features, output features, and weights are kept stationary in the processing element.

In this paper, we study three complementary computation reuse techniques proposed in [1], [5], [9]. CoDR presents a novel CNN dataflow that employs scalar-matrix multiplication (Fig. 3b) to pave the way for the Universal Computation Reuse (Fig. 1) that exploits weight sparsity, repetition, and similarity simultaneously in the convolutional layers. Next, we design a novel Run-Length Encoding (RLE) scheme customized for the data values required data for the Universal Computation Reuse. Finally, we observe that specialized CNN dataflows must make use of the accelerator characteristics; since the weights are compressed, access to the on-chip weights is less costly than the access to the input and output features. Thus, we design the loop ordering of the CoDR dataflow to reduce the number of costly accesses to the input and output features.

Compared to Sparse CNN (SCNN) [1] and Unique Weight CNN (UCNN) [5] accelerators, CoDR: (a) improves weight compression by 1.69× and 2.80× due to the RLE customization, (b) reduces SRAM accesses by 7.99× and 5.08× because of the dataflow loop ordering, and (c) achieves energy savings by 6.84× and 3.76× thanks to the universal computation reuse. The contributions of this paper are as follows:

- We introduce Universal Computation Reuse that exploits weight sparsity, repetition, and similarity by adapting scalar-matrix multiplication for the convolutional layers.
- We customize RLE scheme to encode each type of weight data required for the Universal Computation Reuse.
- We present a CNN dataflow optimized for minimum on-chip memory accesses. CoDR dataflow leverages the low per-access cost of weight memory access to reduce the total number of accesses to the input and output features by keeping them stationary in the processing elements.
- We implement CoDR architecture using a 45nm technology and compare it with two similar works: SCNN [1] and

Fig. 1. Dataflow comparison of SCNN [1], UCNN [5], CORN [10]. ΔNN [9], and CoDR. Densify and Unify eliminate ineffectual and repetitive weights, respectively. Differential adds differential computation to exploit prior results.
CoDR

\begin{equation}
\Delta = \Delta_0 = 0
\end{equation}

\begin{equation}
\Delta > 3 \quad \Delta = 3 \quad \Delta = 2 \quad \Delta = 1 \quad \Delta = 0 \quad w = 0
\end{equation}

UCNN [5], which exploit weight sparsity and repetition.

The rest of the paper is organized as follows: Section II describes three complementary computation reuse optimizations. Section III explains data reuse techniques in the CoDR dataflow. Section IV presents CoDR architecture and Section V compares CoDR with two compressed CNN accelerators.

II. Computation Reuse

Fig. 1 explains three complementary techniques of computation reuse used in the state-of-the-art neural network accelerators and introduces universal computation reuse that employs all three methods simultaneously. These techniques are applied on the multiplication model of a fully-connected layer (Fig. 1b) in which an input feature \( (i_1) \) is multiplied by a vector of weights whose results are routed to the output accumulators. Since these modifications lead to irregularity of computation, CNN accelerators use extra data to store output indexes. Section III explains how CoDR maps the dataflow of the convolutional layers to this multiplication model.

A. Weight Sparsity

Fig. 2 shows that the sparsity \((W=0)\) of the 8-bit weight values of three contemporary CNN models can reach to 94% in the VGG16 model \([13]\). Weight sparsity leads to ineffectual computation (red color in Fig. 1) that can be eliminated by Densification. Fig. 1b shows that SCNN [11] exploits weight sparsity by removing zero terms from the on-chip data.

B. Weight Repetition

While deep neural network inference requires millions of the weights (130 million weights in VGG16 [13]), number of unique weights is bounded by the data bit-length (256 unique weights for the 8-bit fixed-point numbers). This results in the computation redundancy (unique colors in Fig. 1). Fig. 2 shows that redundant computation on the non-zero weights \((\Delta=0)\) can even reach to 39% in the 8-bit GoogleNet [14] weights. Consequently, various CNN accelerators exploit the computation redundancy by the means of Unification; instead of multiplying all weights by the input feature, Fig. 1b shows that CORN [10] routes redundant computations through a programmable crossbar to the next-stage accumulation buffer to bypass the repeated computation. Fig. 1b presents UCNN [5] that factorizes out the same weights in the dot product as an activation group, which includes the coordinates of the input features that are multiplied by the same weight. UCNN also exploits weight sparsity by eliminating the activation groups related to the zero weights. As a result of Unification, number of multiplications is reduced to the number of unique weights.

C. Differential Computation

Fig. 2 shows that the portion of zero and redundant weights drop significantly to 0.5% and 9.0% in the 16-bit fixed-point weights, which makes the Densification and Unification techniques useless. As an alternative, Differential computation operates on the differences of the similar weights rather than the absolute operands by reusing the previous results. Fig. 1b shows that \(\Delta_{NN} [9]\) computes the difference between successive sorted weights \((\Delta)\), and multiplies the \(\Delta_s\) instead of the absolute weights. Equation (1) shows how this accelerator exploits differential computation in the CNN inference.

\begin{equation}
w_{m+1} \times i = (w_{m+1} - w_m) \times i + w_m \times i = \Delta_m \times i + w_m \times i
\end{equation}

Fig. 2 shows that using Differential Computation enables the CNN accelerator to extend the computation reuse to the small \(\Delta\) values and compensates the lack of weight sparsity and weight repetition in the 16-bit data. However, \(\Delta_{NN} [9]\) is unaware of weight sparsity \((W=0)\) and repetition \((\Delta=0)\).

D. Universal Computation Reuse

While computation reuse techniques are employed individually in different works, we observed that they are complementary to each other. Thus, we introduce universal computation reuse that employs Densification, Unification, and Differential Computation simultaneously to exploit \(W=0, \Delta=0,\) and small \(\Delta\) values. The following steps that implement universal computation reuse impose no overhead on the chip as they are executed offline once per each neural network model.

(i) We break a convolutional layer into the tiles of \(T_N\) input and \(T_M\) output channels that are processed at the same time by a processing unit of the CoDR accelerator. (ii) Tiles of weight and bias terms are quantized into the 8-bit fixed-point numbers. (iii) We collect the weights related to a single input channel inside the tiles, and produce \(T_N\) weight vectors, each contains the weights of \(T_M\) weight kernel for a unique input channel. (iv) We sort, densify, and unify the weights (Fig. 1e, g, and h). (v) \(\Delta\) values of the non-zero unique weights and their corresponding indexes are computed and sent to the RLE encoders (Section III-C) for the data reuse techniques.

III. Data Reuse

Data transfer in neural network accelerators costs more than computation. According to our evaluations, UCNN [5]
A. Scalar-Matrix Multiplication in CoDR Dataflow

Convolutional layers have a 4-dimensional (4D) weight that consists of 3D weight filters for M output channels, each of which contains \( R_K \times C_K \) weight kernels for \( N \) input channels. Output features can be produced by applying an activation function on each of the following operations results:

**3D convolutions.** Fig. 3 shows how the features of the first output channel are computed by a 3D convolution of the weight filter and the input features. A single output feature is computed by 2D dot product operations, each of which includes pairwise multiplication of a weight kernel by a window of the input features, followed by accumulating the partial products. 2D dot product results (14 and 7) are then accumulated across input channels to produce the result of the 3D convolution (21). The input feature window moves by stride cells to compute the next output feature.

**Scalar-matrix Multiplication.** Another CNN dataflow proposed by [8] is shown in Fig. 3b. Shaded regions of the input features present the cells involved in the dot product operations between the non-zero weights of the second weight filter (2 and 3) and the input features. Each weight (scalar) is multiplied by its corresponding region of the input features (matrix). Then, partial results of a weight filter (dotted matrices) are accumulated to produce the final results.

CoDR dataflow employs the scalar-matrix multiplication model since it breaks the dependency between the individual weight terms and enables us to linearize the weight kernels

![Fig. 3. A convolutional layer with N=2 input channels (blue and red cells), M=2 output channels (green and purple numbers), input feature size of \( R_1=C_1=4 \), kernel size of \( R_K=C_K=2 \) and output feature size of \( R_O=C_O=3 \). (a) Convolutional inference uses 3D convolution operations illustrated for the first output channel. (b) Instead, CoDR employs scalar-matrix multiplication for CNN inference as shown for the second output channel. (c) Linearized weight vectors of the first (blue) and second (red) input channels.](image)

SCNN [1] spend 64% and 76% of the total energy for data transfer. We show the CoDR data reuse scheme below.

B. On-Chip Data Reuse (Dataflow Loop Ordering)

We observe that a CNN dataflow must emphasize on the features in which the accelerator outperforms. As CoDR employs novel RLE schemes to compress the weights (Section III-C), accesses to the weight terms (on average 1.69 bits/weight) are less costly than access to the input or output features (8 bit/feature). CoDR reduces the number of on-chip accesses to the input and output features by using an input and output stationary dataflow whose loop ordering is illustrated in Fig. 5. (a), (b), (c), and (d) show that CoDR accesses output features only once and (e) and (f) show that input features are fetched \( T_{PU} \times T_{AR} \) times in which \( T_{PU} \) is the number of processing units. In contrast, UCNN [5] and SCNN [1] increase the number of costly accesses to the input and output features.

C. Run-Length Encoding

Due to the irregularity of computation arising from employing the universal computation reuse (Fig. 1), CoDR stores three data structures to obtain the computation order: (a) \( \Delta \) values between the non-zero unique weights. (b) Output indexes related to each unique weight repetition. (c) And the count of unique weight repetitions. CoDR customizes RLE schemes for the characteristics of each data type. Additionally, the RLE process of each data structures is independent; RLE Encoder iterates on the encoding parameter of each data structure, finds the specific parameters with which it encodes them in the least memory space, and stores the encoding parameters along with the compressed values to the off-chip memory. The per-structure and per-layer customization improves the compression rate and DRAM access efficiency. Fig. 4 shows the encoding process of the example in Fig. 1.
Fig. 5. (a) High-level CoDR architecture includes Weight, Input, and Output SRAM modules, Input Register File (RF), and Processing Units (PU). Circled numbers show the loop ordering of the CoDR dataflow. (b) PU architecture consists of $T_M$ Multiplier Processing Elements (MPE), $T_M$ Accumulator Processing Units (APE), and an Interconnection Network. (c) MPE decodes compressed weight structures, multiplies scalar weights by the input feature matrices, selects the results based on the index, and sends them to the corresponding APE, which accumulates and post-processes the partial results.

Fig. 2 shows that Δ values are smaller in the 8-bit raw data since the resolution is less than the 16-bit weight terms and weights are highly repeated. RLE Encoder exploits the small Δ values by encoding them in narrower numbers, e.g., 2 bits. When a Δ does not fit into this bit-length, it is encoded as a full-precision value, i.e., 8 bits. A single bit (shaded bits in Fig. 4) is appended to each Δ value to distinguish between the low-precision and high-precision values. A longer low-precision bit-length results in more weights encoded in the low-precision values, yet, each requires more memory space.

**Unique Weight Repetition.** The possible repetition count for unique weights ranges from 1 to $T_M \times R_K \times C_K$. RLE Encoder encodes them in numbers with a specific bit-length. When the repetition count of a unique weight overflows, a dummy unique weight with $Δ = 0$ is inserted to the unique weight data structure to track the overflowed portion of the repetition count. A long bit-length decreases the overflows, but it wastes the memory space for the small repetitions.

**Indexes.** CoDR employs the same RLE scheme as the unique weight Δs with one difference: Having computed the Δ values between subsequent indexes, RLE Encoder uses absolute indexes when the Δ value is either negative or does not fit into the low-precision bit-length.

### IV. CoDR Architecture

#### A. High-level Architecture

Figure 3h illustrates CoDR architecture that contains 3 SRAM cells for input features, weights, output features, and $T_{PU}$ (=4) Processing Units (PUs). Since all PUs work on the same region of the input/output features, an input register file (RF) shared between all PUs caches input features. A PU calculates $T_M$ tiles of $T_{RO} \times T_{CO}$ output features in an Iteration, which is executed in multiple Cycles. In each Cycle, $T_N$ tiles of $T_{RI} \times T_{CI}$ input features are processed.

#### B. Processing Unit Architecture

A processing unit contains $T_N$ Multiplier Processing Elements (MPE), $T_M$ Accumulator Processing Elements (APE), and an interconnection network that connects the MPEs to APEs (Fig. 3). In each Iteration, APE accumulates the partial results of a single output channel; a MPE is assigned with an input channel in a Cycle; the $i^{th}$ layer of the input features inside the Input RF is broadcasted to the $i^{th}$ MPE of all PUs.

#### C. MPE and APE Architecture

Fig. 3j shows that a Weight RF gradually loads the compressed Repetition Counts, Unique Weight Δs, and Indexes from the Weight SRAM. These data structures are then decoded by the Weight Decoder module. A differential Scalar-Matrix Multiplier (MLP Array) multiplies each unique weight (scalar) by a tile of input features from the Input RF (matrix).

### D. Computation and Data Reuse Support

Universal computation reuse is employed in the CoDR architecture: (i) By eliminating zero weights from the off-chip data, CoDR implicitly exploits weight sparsity. (ii) To make use of weight repetition, Weight RF broadcasts a unique weight to the MLP Array where it is multiplied by all of the input features. In the subsequent clock cycles, an index related to each repetition of the unique weight is fetched for the Selector to choose a $T_{RO} \times T_{CO}$ window of the multiplication results and send them to the corresponding APE. (iii) Differential computation is employed by adding a Matrix-Matrix Accumulator inside the MLP Array to add the Δ multiplication results to the prior accumulated results. Data reuse is also used by (i) keeping the input features stationary in the Input RF (MPE) and output features in the Output RF (APE). (ii) Loop ordering (circled numbers) accesses output features only once (fully output stationary) and input features only $T_M \times T_{PU}$ times (semi input stationary). (iii) Weights are all compressed and decoded by the Weight Decoder.

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**TABLE I**

| Parameter | CoDR | UCNN | SCNN |
|-----------|------|------|------|
| $T_{PU}$  | 8    | 48   | 21   |
| $T_M$, $T_N$ | 4, 4 | 1, 4 | 2, 1 |
| $T_{RO}$, $T_{CO}$ | 8, 8 | 1, 8 | 1, 1 |
| $T_{RI}$, $T_{CI}$ | 20, 20 | 1, 12 | 1, 1 |
| $\times$ per PU | 64 | 8 | 16 |
weight densities and repetitions. The middle group shows the original density and repetition while they drop towards the right-side and left-side groups.

V. EVALUATION

A. Benchmarks and Analysis Tools

We compare CoDR with two recent compressed CNN accelerators: SCNN [1] and UCNN [5] that exploit weight sparsity and repetition, respectively. We implement all designs in Verilog and synthesize them using Synopsys Design Compiler with a 45 nm technology. Table 1 presents the configuration of the three architectures. We assign the number of processing units \( (T_{PU}) \) to equalize the overall area of each design. We employ 250 kB of input and output SRAM cells and 200 kB of weight SRAM such that they accommodate all data required for an Iteration. Consequently, overall area of each architecture is 2.85 mm\(^2\). We evaluate the number of memory accesses in each design by cycle-accurate simulation. SRAM cells are modeled using CACTI [12] and DRAM access energy consumption is considered 160 pJ/B [5]. We quantize AlexNet [7], VGG16 [13], and GoogleNet [14] weights into the 8-bit fixed-point terms. We evaluate four weight densities (denoted as \( D \)) by randomly eliminating the non-zero weights and study different numbers of unique weights (denoted as \( U \)) by making the \( 8 - \log_2(U) \) least significant bits of weights zero.

B. Weight Compression Analysis

Fig. 6 shows the compression rate across three CNN models with different weight densities and repetitions. SCNN does not compress the non-zero weights and stores the number of zero values between two subsequent non-zero weights in 4 bits [1]. UCNN employs RLE to compress the weights and indexes [5], yet, it uses bit-length of 5 for all layers. CoDR chooses the optimal parameter with which it encodes weights and indexes into the minimal memory space. UCNN additionally appends 1 bit to each index to indicate the transition to a new unique weight [5]. CoDR prevents this 1-bit overhead by encoding the repetition counts in numbers with a specific bit-length. This improves the compression for the highly-repeated weights. As a result, CoDR compresses the weights by 1.69\( \times \) and 2.80\( \times \) more than UCNN and SCNN.

We observe that weight sparsity (right groups) and weight repetition (left groups) have different effects on the weight data values. Since all designs eliminate zero weights and their corresponding indexes form the off-chip memory, sparsity results in longer distance between subsequent non-zero weights and their indexes, and smaller number of unique weight repetitions. Thus, customized RLE encoder chooses longer bit-lengths for weights and indexes, shorter bit-length for the repetition counts, and improves compression rate by 1.61\( \times \) and 4.75\( \times \) compared to UCNN and SCNN. On the other hand, limiting number of unique weights increases the weight repetition. Consequently, weight and index \( \Delta \) values are smaller, and unique weights repeat more; customized RLE encoder employs shorter bit-lengths for weights and indexes and longer bit-lengths for the repetition counts. Consequently, CoDR compression rate is 1.87\( \times \) and 4.52\( \times \) higher than UCNN and SCNN in these groups.

C. SRAM Access Analysis

Besides weight compression rate, dataflow substantially affects SRAM access as it determines the trade-offs in how PUs access each type of data. Since all designs compress weight terms, an access to the weight SRAM costs 20.61\( \times \) (CoDR), 12.17\( \times \) (UCNN), and 4.34\( \times \) (SCNN) less than an access to the input or output features. As a result, a weight-compressed CNN dataflow should decrease the number of costly accesses to the input and output features by keeping them stationary in PEs. Thus, CoDR dataflow increases the number of weight accesses to maximize input and output feature reuse (50% of the CoDR SRAM bandwidth is spent on the weights). On the other hand, UCNN and SCNN increase the number of input feature accesses by 20.4\( \times \) and 21.3\( \times \). Moreover, UCNN accesses each output feature 72.1 times, and spends only 1.40% of the total SRAM bandwidth for the weight access. Having considered increased costly accesses to the input and output features by UCNN and SCNN, CoDR dataflow reduces SRAM accesses by 5.08\( \times \) and 7.99\( \times \).

D. Energy Consumption Analysis

Fig. 8 illustrates the effect of weight density and repetition on the energy consumption. CoDR consumes on average 3.76\( \times \) and 6.84\( \times \) less energy relative to UCNN and SCNN. DRAM, SRAM, and Register File Access. Since the intermediate results are kept on-chip, input and output feature access consumes less than 15% of total DRAM access energy in all designs. Thus, DRAM and SRAM energy footprints.
follow the same characteristics of Fig. [5] and [7] DRAM is the most energy-hungry part of the SCNN design (37%) due to the low compression rate while it consumes 18% and 6% of the CoDR and UCNN energy. UCNN and SCNN SRAM energy consumption does not change with weight sparsity and repetition, since 98.6% and 86.4% of total SRAM bandwidth is used by the input and output feature access. However, 50% of the CoDR’s SRAM energy is consumed by the weight access that drops by 16% and 8% in the right and left groups. Register file energy consumption includes the input, weight, and output RF access that is on average 342, 3880, and 2861 µJ in CoDR, UCNN, and SCNN, respectively.

ALU and Crossbar. ALU consumes a significant portion of CoDR energy (42% on average) as DRAM and SRAM accesses are minimized with the RLE compression and CoDR dataflow. ALU energy consumption of all designs decreases by around 25% in the right groups with the density degradation. CoDR and UCNN also exploit weight repetition in the groups with the limited number of unique weights. Thus, ALU energy consumption drops substantially by 52% and 48% when limiting the number of unique weights to 16. In short, ALU in CoDR consumes 1.32× and 3.80× less energy than UCNN and SCNN due to the universal computation reuse. Finally, crossbar is the least energy-hungry module in both CoDR and UCNN designs as it consumes 4.7% and 2.3% of total energy.

VI. CONCLUSION

In this work, we study three complementary computation reuse optimizations for the CNN accelerators and introduce Universal Computation Reuse that exploits weight sparsity, repetition, and similarity simultaneously. We propose a dataflow that employs scalar-matrix multiplication to apply Universal Computation Reuse to the convolutional layers. CoDR dataflow makes use of data reuse to minimize the on-chip memory access. We reduce the cost of each weight memory access by customizing run-length encoding based on the weight values. The loop ordering of the CoDR dataflow also reduces the total number of accesses to the input and output features by keeping them stationary in the processing elements. Our evaluation over three CNNs with different weight densities and repetitions shows that compared to two recent compressed CNN accelerators with the equivalent area of 2.85 mm², CoDR requires 1.69× and 2.80× less DRAM access, reduces SRAM access by 5.08× and 7.99×, and consumes 3.76× and 6.84× less energy.

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