Realization of a High Mobility Dual-gated Graphene Field Effect Transistor with Al$_2$O$_3$ Dielectric

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We fabricate and characterize dual-gated graphene field-effect transistors (FETs) using Al$_2$O$_3$ as top-gate dielectric. We use a thin Al film as a nucleation layer to enable the atomic layer deposition of Al$_2$O$_3$. Our devices show mobility values of over 8,000 cm$^2$/Vs at room temperature, a finding which indicates that the top-gate stack does not significantly increase the carrier scattering, and consequently degrade the device characteristics. We propose a device model to fit the experimental data using a single mobility value.

Graphene, a mono- to few-layers of $sp^2$ bonded carbon in a honeycomb lattice, has been studied intensively since its discovery in 2004$^1$ due to its unique electron physics, as well as possible applications to electronic devices. Graphene’s high intrinsic carrier mobility (over 200,000 cm$^2$/Vs at low temperature for suspended samples$^2$), combined with its mechanical and thermodynamic stability$^3$, makes it a promising material for nano-electronic devices.

The fabrication of graphene-based field-effect transistors requires a uniform gate dielectric deposition technique on graphene, with high dielectric constant ($\kappa$) and reduced interface states density. It is well known that the existence of a mechanically and chemically stable native oxide for silicon, SiO$_2$, has been key to the success of silicon-based microelectronics. Highly insulating SiO$_2$ grows on Si by thermal oxidation$^4$, and the interface between Si and SiO$_2$ has almost close-to-ideal properties. Atomic layer deposition (ALD) is a well developed technique used for growing high-$\kappa$ gate dielectric layers, thanks to its precise control over the film thickness and uniformity. However, the direct deposition of high-$\kappa$ dielectric materials, such as Al$_2$O$_3$ and HfO$_2$, on graphene using H$_2$O-based ALD is not possible because of the hydrophobic nature of graphene basal plane. Given that a perfect graphite surface is chemically inert$^5$, attempts to grow ALD Al$_2$O$_3$ layer on a clean HOPG (highly oriented pyrolytic graphite) surface lead to a selective growth at the steps between graphite layers, where the broken carbon bonds along the terraces serve as 1D nucleation center for the initial ALD process. Therefore, the deposition of high-$\kappa$ dielectric materials on graphene has been relatively limited so far.

Previous studies have used surface treatments of the graphene surface in order to allow ALD growth. Examples include NO$_2$ functionalization$^{10}$, O$_3$ functionalization$^7$, and PTCA (perylenetetracarboxylic acid) coating$^{11}$, or simply nucleating the dielectric growth from impurities on graphene without prior cleaning.$^{12}$ The carrier mobility on top-gated graphene devices with Al$_2$O$_3$ dielectric deposited using NO$_2$ functionalization was 7,000 cm$^2$/Vs at 4.2K.$^{10}$ On the other hand, Lemme et al. showed a significant degradation of graphene carrier mobility with more than an 85% decrease for both electrons and holes when an evaporated SiO$_2$ layer was used as a top-gate dielectric.$^{13}$ Here we report the realization of a top-gated graphene field-effect transistor with a high-$\kappa$ dielectric layer grown by ALD, and with minimal carrier mobility degradation with respect to a graphene layer without a top dielectric. In order to deposit the Al$_2$O$_3$ dielectric, we introduce a thin nucleation layer of oxidized Al between the graphene layer and the dielectric. The electrical characteristics of top-gated field-effect transistors fabricated using this technique, indicate that a high, above 8,000 cm$^2$/Vs, carrier mobility at room temperature after top-gate processing. We develop a simple device model including the effect of quantum capacitance, which agrees well with the observed transport characteristics, and provides the extracted value of mobility, initial charge density, and contact resistance of devices.
The transport characteristics of the device are measured at room temperature in a vacuum probe station. The top-gate electrode and the Si substrate are used as a local gate and global back-gate, respectively, and control the carrier concentration and polarity in the graphene layer. Fig. 2 shows the total device resistance ($R_{\text{total}}$) as a function of top-gate voltage measured at different back-gate bias from -40V to 40V, and at a drain bias of $V'_d = 0.1V$. Without an applied back-gate bias ($V_{BG} = 0V$) the sample resistance reaches a maximum (Dirac point) at $V_{VBG,Dirac} = 0.08V$. This observation indicates that there is little unintentional doping of the graphene sample after the top-gate stack deposition. As $|V_{BG}-V_{Dirac,TG}|$ increases, the electron or hole concentration in the graphene channel increases and $R_{\text{total}}$ decreases, resulting in a $\Lambda$-shape traces. The top-gate hysteresis is smaller than 0.05V, and the leakage current through the $Al_2O_3$ top-gate dielectric is less than 0.75 $pA/\mu m^2$. These observations indicate a high dielectric quality and a low ($<9.4 \times 10^{10} cm^{-2}$) interface state density.

Figure 2 data show $R_{\text{total}}$ vs. $V_{TG}$ measured at different $V_{BG}$ values. An applied $V_{BG}$ bias changes the position of the Dirac point, and also shifts vertically the measured resistance values. The change of the Dirac point position can be explained as follows: a positive (negative) $V_{BG}$ bias induce a finite concentration of electrons (holes) in the active area, proportional to the back-gate capacitance ($C_{BG}$). In order to restore the device to the Dirac point, where the carrier concentration is minimum, a negative (positive) applied $V_{TG}$ is required. The vertical shift is caused by the resistance change in the un-top-gated regions of the graphene flake. The position of the minimum conductivity points in terms of $V_{TG}$ and $V_{BG}$ is shown in the inset of Fig 2. The slope represents the ratio between the top-gate and back-gate capacitances, $C_{TG}/C_{BG} = 28$. Using the back-gate capacitance value of $C_{BG} = 11nF/cm^2$, the top-gate capacitance is estimated to be $C_{TG} = 306nF/cm^2$, corresponding to a relative dielectric constant of 6.4 for the $Al_2O_3$ film.

We now present a model for the device characteristics of Fig. 2. The carrier concentrations (electrons or holes) in the graphene channel regions, $n_{\text{total}}$, can be approximated by

$$n_{\text{total}} = \sqrt{n_0^2 + n(V_{TG})^2}$$

where $n_0$ represents the density of carriers at the minimum conductivity, Dirac point. The residual carrier concentration $n_{BG}$, which for an ideal, disorder-free graphene layer should be zero, is generated by charged impurities located either in the dielectric or at the graphene/dielectric interface. $n(V_{TG})$ represents the carrier concentration induced by the top-gate bias away from the Dirac point, $V_{TG} = V_{TG,Dirac}$. The expression for $n(V_{TG})$ is obtained from the following equation relating $V_{TG}$, $C_{ox}$ and the quantum capacitance of the two-dimensional electrons in the graphene channel.

$$V_{TG} - V_{TG,Dirac} = C_{ox} \frac{e}{n} \frac{n_{BG} \pi n}{e}$$

The total device resistance, $R_{\text{total}}$ is given by
In Eq. (1) we show the measured (lines). The inset shows the extracted contact resistance, $R_{\text{contact}}$ vs. values (symbols) along with modeling results for each dataset.

By fitting this model to the measured data of Fig. 2, we can extract the relevant parameters, $n_0$, $\mu$, and $R_{\text{contact}}$. In Fig. 3 we show the measured $R_{\text{total}}$ vs. $V_{\text{TG}}$ (symbols), along with the model of Eq. (1) (solid lines). The modeling results agree well with the experimental data. Indeed, the data set of Fig. 3 can be fitted with a single value of the mobility $\mu=8,600 \text{ cm}^2/\text{V} \cdot \text{s}$, and with different contact resistance which depend on the applied $V_{\text{BG}}$ (Fig. 3 inset).

![Graph showing $R_{\text{total}}$ vs. $V_{\text{TG}}$ at selected $V_{\text{BG}}$ values (symbols) along with modeling results for each dataset. The inset shows the extracted contact resistance, $R_{\text{contact}}$ vs. $V_{\text{BG}}$.](image)

We now discuss the extracted $\mu$ and $n_0$ values in our device in comparison with existing theoretical studies on graphene transport. Adam et al.\textsuperscript{20} studied graphene transport in the diffusive limit using the Boltzmann transport formalism, and calculated $\mu$ and $n_0$ as a function of a single parameter, the impurity concentration ($n_{\text{imp}}$) at the graphene/dielectric interface\textsuperscript{21}: $\mu \approx 3\hbar/(h \cdot n_{\text{imp}})$, and $n_0 \approx 0.2 \times n_{\text{imp}}$. According to Adam et al.’s model, the extracted mobility value in our device, $\mu=8,600 \text{ cm}^2/\text{V} \cdot \text{s}$, corresponds to an impurity concentration $n_{\text{imp}} \approx 1.0 \times 10^{12} \text{ cm}^{-2}$, which in turn would result in a residual carrier concentration $n_0 \approx 1.9 \times 10^{11} \text{ cm}^{-2}$, in good agreement with our experimental data. Lastly we discuss the temperature dependence of the transport data in our device. From 300K down to 77K the carrier mobility is rather insensitive to temperature, showing a modest ~10% increase. This observation suggests that phonon scattering is relatively small, and that the mobility is primarily determined by fixed impurity scattering\textsuperscript{22}.

In summary, we fabricated a top-gated monolayer graphene device and successfully deposited an Al$_2$O$_3$ gate dielectric on its surface by ALD. The device characteristics are investigated in the dual-gate operation mode. Our data show that the overlaying Al$_2$O$_3$ layer does not substantially degrade the electrical properties of the graphene device. Our model, including quantum capacitance of graphene, agrees very well with our experimental results, and extracted mobility values are above $8,000 \text{ cm}^2/\text{V} \cdot \text{s}$ at room temperature. These results are very promising both for high speed FETs, and also to enable novel device designs in graphene.

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