Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures

BISHNU PATRA (Student Member, IEEE), MOHAMMADREZA MEHRPOO (Student Member, IEEE), ANDREA RUFFINO (Student Member, IEEE), FABIO SEBASTIANO (Senior Member, IEEE), EDOARDO CHARBON (Fellow, IEEE), AND MASOUD BABAIE (Member, IEEE)

1 Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands
2 Broadcom Netherlands B.V., 3981 AJ Bunnik, The Netherlands
3 Institute of Microengineering, Faculty of Engineering, École Polytechnique Fédérale de Lausanne, 2002 Neuchâtel, Switzerland

CORRESPONDING AUTHOR: B. PATRA (e-mail: b.p.patra@tudelft.nl)

This work was supported by Intel Corporation. (M. Mehrpoo and A. Ruffino contributed equally to this work.)

ABSTRACT This paper presents the characterization and modeling of microwave passive components in TSMC 40-nm bulk CMOS, including metal-oxide-metal (MoM) capacitors, transformers, and resonators, at deep cryogenic temperatures (4.2 K). To extract the parameters of the passive components, the pad parasitics were de-embedded from the test structures using an open fixture. The variations in capacitance, inductance and quality factor are explained in relation to the temperature dependence of the physical parameters, and the resulting insights on the modeling of passives at cryogenic temperatures are provided. Modeling the characteristics of on-chip passive components, presented for the first time down to 4.2 K, is essential in designing cryogenic CMOS radio-frequency integrated circuits, a promising candidate to build the electronic interface for scalable quantum computers.

INDEX TERMS Cryo-CMOS, quantum computing, cryogenic, capacitor, inductor, transformer, resonator, quality factor.

I. INTRODUCTION
Solid-state circuits operating at cryogenic temperatures have been used for several applications. In quantum computing applications, as the number of qubits starts growing [1], it becomes infeasible to fit the cables between cryogenic quantum bits (qubits) and room-temperature control electronics into a standard cryogenic refrigerator. Thus, we advocate the integration of qubits and control electronics inside the refrigerator [2]. Complementary Metal Oxide Semiconductor (CMOS) circuits operating at cryogenic temperatures (Cryo-CMOS) have been proposed for the implementation of a scalable control and readout interface of cryogenic quantum processors [3], [4].

In deep-space applications, the telemetry link capacity is limited by the signal-to-noise ratio (SNR, i.e., $\sim -30$ dB) of the current radio-frequency downlink circuits. To obtain higher SNR, an optical link can be implemented as large arrays of superconducting nanowire single-photon detectors (SNSPDs) at 1 K, all operating in parallel. The interface and readout of such arrays using room temperature electronics are impractical due to heat load and SNR degradation caused by attenuation of the cables. Moreover, the stringent low noise temperature requirements for the readout could only be achieved by operating at cryogenic temperatures [5].

In space applications, since the circuits have to operate at temperatures far beyond the military range, circuit designs also have to be optimized for cryogenic operation [6]. Besides that, cryo-CMOS technology has also been used in the past to fabricate cryogenic low noise amplifiers (LNAs) for high sensitivity receivers [3], [7] and cryogenic LC oscillators for electron spin resonance detectors [8].

The design of solid-state electronics at cryogenic temperatures has triggered the need for characterization of active...
and passive components as required to reliably predict the performance of cryogenic radio-frequency integrated circuits (RFIC) [9]. To some extent, this has been pursued by the scientific community in the case of active devices, which is evident from papers that show DC characterization [10], [11], RF and noise characterization [12], device mismatch [13], [14] of bulk CMOS, as well as DC characterization [15], [16], small-signal and noise characterization [17] of SOI CMOS devices in different technology nodes. In the case of passive devices, cryogenic characterization of off-chip discrete commercial off-the-shelf capacitors and resistors [18], [19] proved that the capacitance/resistance can change drastically at those temperatures depending on the material, thus affecting circuit performance. In the case of on-chip passive devices, prior work is limited to the measurement of capacitor and resistor values [20], [21]. Consequently, there is a lack of cryogenic models for on-chip inductive/capacitive components predicting their behavior, variation and quality factor. In this paper, for the first time, we have modeled the characteristics of on-chip passive components in bulk CMOS at cryogenic temperatures, which would complement active device models for accurate prediction of the behavior of RFICs at cryogenic temperatures.

Section II presents the test structures and measurement setup. Section III elaborates on the measurement and modeling of metal-oxide-metal (MoM) capacitors. The characterization, lumped-component based modeling and electromagnetic (EM) simulation of a transformer are presented in Section IV. Section V emphasizes the impact of the developed cryogenic models on RFICs, followed by a conclusion in Section VI.

II. TEST STRUCTURES AND MEASUREMENT SETUP
Several test structures were fabricated in the 1P7M-4X1Z1U TSMC 40-nm bulk CMOS with an ultra-thick metal layer to characterize passive components both at 300 K, and 4 K, comprehensively. A high-density rotative MoM capacitor with a poly shield was chosen from the library provided by the foundry. For the inductance and metal resistance characterization, a transformer with high-inductance multi-turn windings was designed to be less sensitive towards calibration errors. Finally, a resonator was also fabricated to validate the cryogenic model of the transformer and capacitor. The substrate was left floating for all the test structures.

The measurements were done using ground-signal-ground (GSG) probes in a 40 GHz Lakeshore CPX cryogenic probe station with R&S ZNB40 vector network analyzer (VNA) (see Fig. 1 (a)). To ensure proper thermalization, the dies were mounted with conductive glue on a copper plate (CP), which was securely taped to the sample holder (see Fig. 1 (b)).

The thermal conductivity of the chip substrate at temperatures below 20 K is comparable to that at 300 K [22], while thermal conductivity of copper remains the same or improves depending on its purity at 4 K [23], suggesting a good thermal link between the sample holder and device under test (DUT). Since all the measured test structures were passive components and the measurements were done by applying small AC signals, the self-heating should be negligible. During the measurement, it was ensured that the temperature sensor mounted on the sample holder was at 4.2 K. Consequently, although the die temperature was not measured directly, considering the large area under the DUT, no static power dissipation and large copper mass below the dies, it can be concluded that the DUT was at 4.2 K. Moreover, the probes were thermally anchored with thick copper wires to the 4 K stage of the probe station.

1. Boron-doped silicon layers.
Due to the variation in the GSG probe electrical characteristics over temperature, short-open-load-through (SOLT) calibrations were done right before the measurement using a Picoprobe calibration substrate (CS-5) at the measurement temperature. Although the load standards in the CS-5 are accurately trimmed to their 50 $\Omega$ stated value at room temperature, their absolute value at cryogenic temperature is not specified, and therefore, it was measured by injecting a DC signal. The resistance of the short fixture was measured and it was subtracted from the measurement of the load, so as to remove the effect of cable and GSG probe and to yield the absolute resistance of the load fixture. At 300 K, the measured load was 50.55 $\Omega$, while at 4.2 K, its value was 49.91 $\Omega$, showing a negligible (∼1 %) change. The measured value of the load was then used as part of the cal kit file for VNA calibration.

For probing, all the components were connected to a 100 $\mu$m GSG pad without electrostatic discharge (ESD) protection diodes to minimize parasitic capacitance (see chip micrographs in Fig. 3 (c), 4, and 8 (b)). The two ground pads in the GSG structure are shorted to each other at metal-1 (M1) level after using vias from AlCu pad (AP) layer to M1 layer, thus creating the signal-to-ground parasitic capacitance of 60 fF. Finally, the pad parasitics were de-embedded from the measurement results of the test structures by using the open standard [24].

### III. MOM CAPACITOR

A high-density rotative MoM capacitor with a poly shield was taped-out using stacked inter-digitated metal fingers in layers 1 to 5 with a finger width of 100 nm and a spacing of 90 nm. To increase the capacitance to a measurable value and in order not to be dominated by the parasitics of pads, 10 such capacitors were connected in parallel, with 6 horizontal and 38 vertical fingers. This provides a capacitance of 202 fF for an area of 150 $\mu$m$^2$ (7.97 $\mu$m $\times$ 1.89 $\mu$m $\times$ 10). The pitch for landing the probes is 100 $\mu$m and the estimated capacitive coupling between the probe tips based on 3D EM simulation is ∼0.2 fF.

The MoM capacitor can be modeled by a frequency-independent $\pi$-network [25], as shown in Fig. 2, where $C_{\text{MoM}}$ is the actual capacitance due to the interdigitated metal fingers across an extra low-k inter-metal dielectric [26], and $C_{\text{par}}$ represents the parasitic capacitance between terminals and ground plane (poly shield). $R_{\text{se}}$ and $L_{\text{se}}$ represent the equivalent series resistance and inductance, respectively, of the traces and vias from the pad to the device terminals. Since, an open test fixture was used for de-embedding, $R_{\text{se}}$ and $L_{\text{se}}$ must be included in the model. The effect of $R_{\text{se}}$ is negligible, since the top metal layer was used for interconnection to the pad. However, $L_{\text{se}}$ affects the self-resonance frequency (SRF) of the structure. The frequency-dependent losses are modeled using $R_f$ and $L_f$, which constitute both metal (skin effect) and dielectric loss. $L_f$ is not a physical parameter, but a fitting parameter, used to model the frequency-dependent loss. The quality factor of the capacitor above 10 MHz is limited by the series resistance [27], and hence, the leakage resistance (modeled as a very high resistance across the capacitor terminals at DC) due to the interface traps [28] is ignored in the model. The parameters in the model can be extracted using Y-parameters.

Figure 3 (a) shows the measured $\text{Im}(-Y_{12})/\omega$ ($\omega$ is the angular frequency), from which the $C_{\text{MoM}}$ can be extracted at the lowest measured frequency (i.e., 100 MHz), where the effect of parasitic inductance is negligible [29]. The capacitance incurs a slight change at 4 K compared to room temperature (RT) due to variation in the dielectric constant, as the thermal contraction of metals is negligible [23]. Based on several measurements, the precision error in $C_{\text{MoM}}$ value was obtained to be less than 1 % (i.e., ∼0.5 fF variation in 200 fF).
For the quality factor measurement, the uncertainty increases when the desired real impedance is negligible compared to the VNA reference impedance of 50 Ω [30]. Hence, at frequencies below 5 GHz (where the quality factor tends towards infinity), the error in the determination of the equivalent series resistance and capacitor’s quality factor \((|\text{Im}(-Y_{12})|/|\text{Re}(-Y_{12})|)\) would be significant and is excluded from Fig. 3 (b). Due to the reduction of dielectric and metal loss at lower temperatures, there is a boost in the quality factor at frequencies below 10 GHz. However, the dielectric loss does not improve over temperature above a certain frequency. This is also in line with the measurement results of capacitors in the military temperature range in a similar technology, as presented in [27]. Consequently, a negligible quality factor improvement is observed above 15 GHz, as can be gathered from Fig. 3 (b). Table 1 concludes the discussion on MoM capacitors and summarizes the change of the model parameters over temperature.

**IV. TRANSFORMER**

A multi-turn transformer featuring a two-turn primary winding with 190 µm diameter and 8 µm trace width and a two-turn secondary coil with 130 µm diameter and 7 µm trace width, as illustrated in Fig. 4, was designed using the ultra-thick metal layer. Shielding of the transformer was prevented due to a highly resistive substrate at 4 K, thereby not having the need to reduce the tangential electric field losses in low-resistive substrates [31]. An open test fixture was used to de-embed the pad parasitics, which is sufficient for a transformer since the DUT plane is at the GSG pads.
The dotted lines in Fig. 5 show the extracted parameters of the transformer versus frequency based on the S-parameter measurement at both RT and 4 K. At first glance, it can be observed that there is a slight reduction in transformer inductance, an increase in coupling factor and a substantial improvement in the quality factor of the transformer windings at 4 K compared to RT. To gain more insight and to track the changes in various parameters over temperature, a lumped-element model is presented in Section IV-A. Based on the developed model, some modifications in the physical parameters of the metal stack provided by the foundry are suggested in Section IV-B. The measurement results are also replicated by using EM simulation.

### A. LUMPED ELEMENT MODEL

The transformer can be modeled using the well-known frequency-independent lumped model for on-chip spiral inductors [32], as depicted in Fig. 6, where \( L_p \) and \( L_s \) represent the inductance, \( R_p \) and \( R_s \) describe the DC ohmic loss, of the primary and secondary windings, respectively. \( k_m \) represents the coupling factor of the transformer. \( C_{ov} \) models the interwinding capacitance, \( C_{ox} \) denotes the oxide capacitance, while \( C_p \) represents the capacitance due to metal lines running in parallel in the multi-turn primary winding. \( C_{sub} \) and \( R_{sub} \) model the substrate capacitance and resistance, respectively. \( R_{skin} \) and \( L_{skin} \) model the frequency-dependent losses (skin effect) in the transformer windings.

\( R_p \) (extracted from \( Re[Z_{11}] \) shown in Fig. 5 (a), (d) at 1 GHz where the skin effect is negligible) is \( \sim 5 \times \) lower at 4 K compared to RT, due to the increase in copper conductivity [23]. Note that the resistivity of copper does not reduce proportionally with temperature until 4 K but it saturates at certain temperatures, due to impurities and crystallographic defects in the metal layers [9]. At higher frequencies, the skin effect dominates and the loss becomes proportional to \( 1/\sigma_{cu}\delta \), in which the skin depth \( \delta = \sqrt{\frac{2}{\mu \sigma_{cu} \omega}} \), where \( \mu \) and \( \sigma_{cu} \) represent the magnetic permeability and conductivity of copper respectively. Since the conductivity increases by \( 5 \times \), skin depth and thus the inductor loss at higher frequencies decreases by \( \sim \sqrt{5} \) [33], as confirmed by Fig. 5 (a) for frequencies above 10 GHz.

The inductance associated with a loop has two components; internal \( (L_{int}) \) and external \( (L_{ext}) \) inductance [34]. \( L_{ext} \) dominates the total inductance and is dictated by the currents flowing on the surface of the conductor. Its value is determined by the phase velocity and characteristic impedance of the inductor trace and hence, is a strong function of the coil dimension. \( L_{int} \), the non-dominant component, is associated with the internal current of the inductor and can be calculated by

\[
L_{int} = \frac{R_{ac}}{\omega} = \frac{l}{2W} \sqrt{\frac{\mu}{\sigma_{cu} \rho_f}}
\]

where \( R_{ac} \) is the ac resistance, \( f \) is frequency, \( l \) and \( W \) are the length and width of the trace, respectively [34]. Intuitively, an increase in conductivity would reduce the skin depth and force the current to flow in the boundary of the conductor. Consequently, the current flowing in the conductor interior reduces, decreasing \( L_{int} \), and thus, the total inductance. This
Table 2: Lumped-element model parameters of transformer at RT and 4 K.

| Parameter | Units | RT | 4 K |
|-----------|-------|----|-----|
| \( L_p \) | pH    | 691 | 650 |
| \( R_p \) | Ω     | 0.95 | 0.22 |
| \( R_{\text{skin}} \) | Ω    | 1.2 | 0.53 |
| \( L_{\text{skin}} \) | pH   | 48  | 48  |
| \( C_p \) | fF   | 18  | 19  |
| \( C_{\text{ox}} \) | fF   | 50  | 52  |
| \( C_{\text{sub}} \) | fF   | 19  | 22  |
| \( R_{\text{sub}} \) | kΩ   | 1.24 | 1000 |
| \( R_{\text{se}} \) | kΩ   | 2   | 2000 |
| \( C_{\text{ov}} \) | fF   | 4.5 | 4   |
| \( k_m \) | -    | 0.367 | 0.39 |

phenomenon is also observed in our measurement results; the 5× increase in conductivity led to a ~5% reduction in inductance (extracted from \( \text{Im}[Z_{11}] \) at the lowest measured frequency), as shown in Fig. 5 (b), and (e).

Figure 5 (c) reveals that the peak quality factor of the primary winding of the transformer (extracted from \( \text{Im}[Z_{11}]/\text{Re}[Z_{11}] \)) increases by 2.7× from RT to 4 K. The improvement is partially contributed (1.6× as verified from EM simulation in Section IV-B) by the increase in conductivity and partly due to the reduction of tangential electric field losses in the silicon substrate, as it becomes highly resistive due to dopant freeze-out.

Figure 5 (f) shows the measured \( k_m \), calculated as \( k_m = \text{Im}[Z_{21}]/\sqrt{\text{Im}[Z_{11}] \cdot \text{Im}[Z_{22}]} \), at both RT and 4 K. The coupling factor is mainly set by the physical dimensions of the transformer, which barely change over temperature (i.e., <1% as shown in [23]). Since the magnetic coupling is not temperature dependent, the slight increase in the coupling factor at 4 K is due to the change in capacitive coupling.

Table 2 summarizes the values of model parameters at RT and 4 K. \( R_{\text{sub}} \) and substrate coupling resistance (\( R_{\text{se}} \)) increases by 3 orders of magnitude at 4 K mainly due to substrate freeze out [35]. For low resistive substrates, the capacitance from the windings to the ground plane is dominated by \( C_{\text{ox}} \) [36], [37], while for highly resistive substrates, the effective capacitance is lowered by \( C_{\text{sub}} \) in series with \( C_{\text{ox}} \), resulting in a slight increase in the frequency where peak quality factor occurs. The self-resonance frequency of the transformer increases by 5%, due to the decrease in both inductance and effective parasitic capacitance to ground.

B. EM MODEL

Besides using lumped-element models of integrated passives, it is convenient for circuit designers to perform EM simulations to generate S-parameters of inductors/transformers and use them for circuit design. For this reason, and to extend the scope of this work towards the design of cryogenic custom integrated passive networks (e.g., hybrid coupler, power splitter, etc.), the metal stack provided by the foundry was modified to enable EM simulations, predicting cryogenic operation.

Based on the performed measurements, the following material properties have been modified in the foundry metal stack: the conductivity of metal-7 (M7) layer was increased 5×, to reproduce the copper conductivity increase, while the substrate resistivity was increased 1000×, to reproduce the effect of carrier freeze-out. The obtained modified metal stack was used to perform EM simulations in Keysight ADS®/Momentum®, with an infinite conductive plane beneath the substrate as the current return path, while the simulator temperature was kept at 300 K. The obtained results could accurately predict the performance of the transformer at 4 K, as can be gathered from Fig. 7 (a)-7 (f). The measured quality factor of the windings was slightly different from the simulation results at 4 K. This is attributed to the exclusion of metal fill in EM simulations, which is required to satisfy the density rules [38].

2. As can be gathered from Fig. 5 (b), the transformer SRF is at 21 GHz. Hence, Fig. 5 (a), Fig. 5 (c), Fig. 5 (f) have been plotted up to 21 GHz. To keep the visibility, the zoomed in version of \( \text{Im}[Z_{11}]/\omega \) and \( \text{Re}[Z_{11}] \) are shown up to 10 GHz.
V. IMPACT ON RFICS

To validate the developed models and combine the use of modified EM simulation for inductors/transformers, with the cryogenic lumped-element model of capacitors, a custom transformer-based resonator (matching network), shown in Fig. 8, was designed. The tank is also used to analyze the impact of the cryogenic operation of passive components on the performance of RFIC blocks like oscillators [39], power amplifiers (PAs) [40], and wideband LNAs [41]. The application of the transformer-based resonator in such circuits is shown in Fig. 9.

The custom transformer was realized by an interwinding multturn spiral inductor in the ultra-thick metal-7 layer with metal-6 underpass and AlCu pad (AP) overpass, while capacitors were implemented as design kit rotative MoM capacitors. The resonator parameters are $L_p = 1.25 \, \text{nH}$, $L_s = 1.07 \, \text{nH}$, $k_m = 0.72$, $C_p = 340 \, \text{fF}$, and $C_s = 385 \, \text{fF}$. Its performance at 4 K was estimated by combining EM simulation of the developed cryogenic metal stack for the spiral transformer and the modified cryogenic model for the capacitors, through layout abutment. The simulation results are compared with the measurement results in Fig. 10.

Figure 10 (a) shows the input impedance of the resonator with Port-2 open ($|Z_{in}|$), which is inversely proportional to the power consumption of a transformer-based oscillator [39]. There is an increase in the impedance peak of the resonator, from RT to 4 K, due to the overall increase in quality factor, which is well predicted by the cryogenic models. Thanks to this improvement, one can obtain the same output voltage swing for smaller current consumption, thus improving the oscillator’s power efficiency. The reduction in inductance and the effective parasitic capacitance causes the first resonance to shift towards higher frequencies by 8 %. The ratio of the resonant frequencies (i.e., the frequency separation between the impedance peaks in $Re(Z_{in})$) merely depends on the coupling factor ($k_m$), which increases by 8 % as predicted by the model.

Figure 10 (b) shows the trans-impedance $Z_{21}$ of a matching network, where the tank in Fig. 9 (b) is terminated with a 50 Ω load resistance. This parameter is widely used in calculating the output transfer function when designing wideband PAs [40]. It can be observed that there is a substantial increase in the $Z_{21}$ at 4 K compared to RT, especially at higher frequencies. Moreover, there is a slight increase in bandwidth due to the increase in $k_m$ and an overall shift of the poles of the transfer function towards higher frequencies, due to the decrease in inductance of the windings. Such improvements can be exploited to deliver larger output power for the same current, and over a larger bandwidth at 4 K with respect to RT. So, this is a considerable advantage for PA design at cryogenic temperatures.

Figure 10 (c) shows the measured $S_{21}$ of the tank, which is required to predict the insertion loss (IL) of input/output or inter-stage matching networks in LNAs/PAs. At cryogenic temperatures, the $S_{21}$ improves, consequently reducing the insertion loss. Note that, for an LNA, the insertion loss of the input matching network directly adds to the overall noise figure. Therefore, such an improvement represents a clear advantage in designing multi-stage LNAs with large bandwidth operating at cryogenic temperatures. As can be gathered from Fig. 10, the developed models can fairly predict the cryogenic performance of the passive network in such circuits.

Such models have also been employed to design more complex circuits, such as a cryogenic CMOS circulator [42], based on LC first- and second-order all-pass filters, and a parametric CMOS LNA [43], with transformer-based passive amplification. The developed models were used to predict the performance of such circuits at 4 K, leading to more optimized designs and gaining more insights about the cryogenic operation of the circuits.

VI. CONCLUSION

Passive components at cryogenic temperatures show in general higher quality factor ($\sim 2 \times$) due to higher metal conductivity and lower loss in the substrate. However, the value of inductive and capacitive on-chip components slightly changes ($\sim 5\%$) from RT to 4 K. These variations can be replicated in an EM simulation by manipulating the resistivity of metals and substrate. As a result, RFIC designers can predict the performance of cryogenic passive devices both by using EM simulation and/or by scaling the presented
lumped model parameters. This enables, in combination with active device models, the reliable design of cryogenic RFICs needed for future large-scale quantum computers.

**ACKNOWLEDGMENT**
The authors would like to acknowledge Carmine de Martino and Prof. Marco Spirito for technical discussions.

**REFERENCES**

[1] F. Arute et al., “Quantum supremacy using a programmable superconducting processor,” *Nature*, vol. 574, no. 7779, pp. 505–510, 2019.

[2] L. Vanderven et al., “Interfacing spin qubits in quantum dots and donors–host, dense, and coherent,” *NPJ Quantum Inf.*, vol. 3, no. 1, p. 34, 2017.

[3] B. Patra et al., “Cryogenic CMOS circuits and systems for quantum computing applications,” *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[4] J. C. Bardin et al., “29.1 A 28nm Bulk-CMOS 4-to-8GHz <2mW cryogenic pulse modulator for scalable quantum computing,” in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, Feb. 2019, pp. 456–458.

[5] J. C. Bardin et al., “A high-speed cryogenic SiGe channel combiner IC for large photon-starved SNSPD arrays,” in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Sep. 2013, pp. 215–218.

[6] A. Çalı̇ğer and M. B. Yelten, “Design of cryogenic LNAs for high linearity in space applications,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4619–4627, Dec. 2019.

[7] S. Montazeri, W. Wong, A. H. Coskun, and J. C. Bardin, “Ultra-low-power cryogenic SiGe low-noise amplifiers: Theory and demonstration,” *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 178–187, Jan. 2016.

[8] G. Gualco et al., “Cryogenic single-chip electron spin resonance detector,” *J. Magnetic Resonance*, vol. 247, pp. 96–103, Oct. 2014.

[9] M. Mehrpoor et al., “Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2019, pp. 1–5.

[10] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiani, “Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures,” *IEEE J. Electron Devices Soc.*, vol. 6, no. 1, pp. 996–1006, Apr. 2018.

[11] A. Beckers et al., “Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing,” in *Proc. 47th Eur. Solid State Device Res. Conf. (ESSDERC)*, Sep. 2017, pp. 62–65.

[12] A. Siligaris et al., “High-frequency and noise performances of 65-nm MOSFET at liquid nitrogen temperature,” *IEEE Trans. Electron Devices*, vol. 53, no. 8, pp. 1902–1908, Aug. 2006.

[13] N. C. Dao, A. E. Kass, C. T. Jin, and P. H. W. Leong, “Impact of series donors–hot, dense, and coherent,” *Nature*, vol. 574, no. 7779, pp. 505–510, May 2018.

[14] H. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, “Thermal conduction in doped single-crystal silicon films,” *J. Appl. Phys.*, vol. 91, no. 8, pp. 5079–5088, 2002.

[15] P. Duthil, “Material properties at low temperature,” *CERN, Meyrin, Switzerland*, Rep. CERN-2014-005, Jan. 2015, pp. 77–95.

[16] M. Babaie and R. B. Staszewski, “A class-F CMOS oscillator,” *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 12, pp. 4141–4148, Dec. 2006.

[17] F.-W. Tsai, K.-C. Wang, K.-C. Lin, C.-L. Lin, and S.-M. Jeng, “Extreme low-K dielectric film scheme for advanced interconnects,” U.S. Patent 7,626,245, Dec. 2009.

[18] P. Riess and P. Baumgartner, “Temperature dependent dielectric absorption of MIM capacitors: RF characterization and modeling,” in *Proc. Eur. Solid State Device Res. Conf.*, Sep. 2006, pp. 459–462.

[19] V. F. Tseng and H. Xie, “Increased multilayer fabrication and RF characterization of a high-density stacked MIM capacitor based on selective etching,” *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2302–2308, Jul. 2014.

[20] H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee, “Fractal capacitors,” *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2035–2041, Dec. 1998.

[21] P. Rezasto, F. Morin, M. Spirito, and L. Galatro, “The HF–VNA, an interferometric approach for the accurate measurement of extreme impedances,” in *Proc. IEEE 93rd ARFTG Microw. Meas. Conf. (ARFTG)*, 2019, pp. 1–6.

[22] T. S. D. Cheung and J. R. Long, “Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.

[23] C. P. Yue and S. S. Wong, “Physical modeling of spiral inductors on silicon,” *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, Mar. 2000.

[24] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*, Hoboken, NJ, USA: Wiley, 2011.

[25] H. Homulle, “Cryogenic electronics for the read-out of quantum processors,” Ph.D. dissertation, Inst. Repository, Delft Univ. Technol., Delft, The Netherlands, 2019.

[26] D. Eggert et al., “A SOI-RF-CMOS technology on high resistivity SIMOX substrates for microwave applications to 5 GHz,” *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1981–1989, Nov. 1997.

[27] R. A. Johnson et al., “Comparison of microwave inductors fabricated on silicon-on-sapphire and bulk silicon,” *IEEE Microw. Guided Wave Lett.*, vol. 6, no. 9, pp. 323–325, Sep. 1996.

[28] C. Detcheverry et al., “The effect of copper design rules on inductor performance,” in *Proc. 33rd Conf. Eur. Solid State Device Res. (ESSDERC)*, Sep. 2003, pp. 107–110.

[29] M. Babaie and R. B. Staszewski, “A class-F CMOS oscillator,” *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[30] M. Vigilante and P. Reynaert, “On the design of wideband transformer-based fourth order matching networks for E-band receivers in 28-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017.
[42] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, “A 6.5-GHz cryogenic all-pass filter circulator in 40-nm CMOS for quantum computing applications,” in Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC), Jun. 2019, pp. 107–110.

[43] M. Mehrpoo, F. Sebastiano, E. Charbon, and M. Babaie, “A cryogenic CMOS parametric amplifier,” IEEE Solid-State Circuits Lett., vol. 3, no. 1, pp. 5–8, Oct. 2019.

BISHNU PATRA (Student Member, IEEE) received the M.Sc. degree in electrical engineering (microelectronics) from the Delft University of Technology, The Netherlands, in 2016, where he is currently pursuing the Ph.D. degree, focusing on cryogenic RF Integrated circuits for quantum computing applications.

From 2013 to 2014, he was a B.Sc. Researcher with the ELCA Department, Delft University of Technology. He worked as an RF and Mixed Signal IC Design Intern with Intel Lab., Hillsboro, OR, USA, from 2017 to 2018. His current research interests include RF transmitters for qubit control, CMOS frequency synthesizers, and design and modeling of microwave passive components at cryogenic temperatures. He was a recipient of the 2014 M.Sc. Faculty Scholarship by the Microelectronics Research Department, Delft University of Technology and the IEEE SSCS Predoctoral Achievement Award (2019–2020).

MOHAMMADREZA MEHRPOO (Student Member, IEEE) received the B.Sc. degree in electrical engineering from Tehran University, Tehran, Iran, in 2010, and the M.Sc. degree (cum laude) in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2012, where he is currently pursuing the Ph.D. degree.

He was an RF System and Circuit Architect with Catena Microelectronics, Delft, where he was involved in low-power CMOS circuits and systems for the IoT applications from 2012 to 2015. He has joined Broadcom, Bunnik, The Netherlands, as a Senior Research and Development IC Design Engineer. His current research interests include high-speed data converters and radio frequency integrated circuit transceivers in CMOS for wireless and wire line communication.

Mr. Mehrpoo was a recipient of the Top Talent Fellowship from the Delft University of Technology, the Project Fellowship from Mediatek, Taiwan, in 2010, and the IEEE Radio Frequency Integrated Circuits Symposium Best Student Paper Award (First Prize) in 2017.

ANDREA RUFFINO (Student Member, IEEE) was born in Torino, Italy, in 1991. He received the B.Sc. degree (cum laude) in engineering physics from Politecnico di Torino, Torino, Italy, in 2013, and the triple joint M.Sc. degree (cum laude) in micro and nanotechnologies for integrated systems from Politecnico di Torino, Institut National Polytechnique de Grenoble, Grenoble, France, and École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, in 2015, where he is currently pursuing the Ph.D. degree in cryogenic CMOS electronics for spin and superconducting qubits.

From 2015 to 2016, he was with Hypes, Inc., Elmsford, USA, where he was involved in designing super conducting readout circuits in RSFQ technology for superconducting nanowire detectors. His current research interests include analog and RF integrated circuit design, cryogenic CMOS electronics for quantum computing applications, superconducting electronics, and sensors.

FABIO SEBASTIANO (Senior Member, IEEE) received the B.Sc. (cum laude) and M.Sc. (cum laude) degrees in electrical engineering from the University of Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (cum laude) from the Sant’Anna School of Advanced Studies, Pisa, Italy, in 2006, and the Ph.D. degree from the Delft University of Technology, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, deep-submicron temperature sensors and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Associate Professor. He has authored or coauthored one book, 11 patents, and over 60 technical publications. His main research interests are cryogenic electronics for quantum computing, quantum computing, sensor read-outs, and fully integrated frequency references.

Dr. Sebastiano is on the technical program committee of the IEEE RFIC Symposium and he is currently serving as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He was co-recipient of the 2008 ISCAS Best Student Paper Award and the 2017 DATE Best IP Award. He is a Distinguished Lecturer of the IEEE Solid-State Circuit Society.

EDOARDO CHARBON (Fellow, IEEE) received the Diploma degree in electrical engineering and EECs from ETH Zürich in 1988, the M.S. degree in electrical engineering and EECs from the University of California at San Diego in 1991, and the Ph.D. degree in electrical engineering and EECs from the University of California at Berkeley in 1995. He has consulted with numerous organizations, including Bosch, X-Fabs, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the Company’s initiative on information hiding for intellectual property protection. In 2000, he joined Canesta, Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002, he has been a Member of the Faculty of EPFL, where he is a Full Professor since 2015. From 2008 to 2016, he was with the Delft University of Technology, as the Chair of VLSI design. He has authored or coauthored over 350 papers and two books, and he holds 21 patents. His interests span from 3-D vision, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits, and systems for quantum computing. He is a Distinguished Visiting Scholar of the W. M. Keck Institute for Space, Caltech, a fellow of the Kavli Institute of Nanoscience Delft.

MASOUD BABAIE (Member, IEEE) received the Ph.D. degree (cum laude) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016. In 2006, he joined the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From 2009 to 2011, he was the CTO of Kavoshcom Research and Development Group. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently a tenured Assistant Professor. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications, and cryogenic electronics for quantum computation.

Dr. Babaie was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, and the 2019 IEEE ISSCC Best Demo Award. In 2019, he received the Veni award from the Netherlands Organization for Scientific Research (NWO). He has been a Committee Member of the Student Research Preview of the IEEE International Solid-State Circuits Conference since 2017. He is currently serving on the Technical Program Committee of the IEEE European Solid-State Circuits Conference.