Memory characteristics of capacitors with poly-GaAs floating gates

I.P. Roh, N.S. Kang, S.H. Shin, Y.T. Oh, K.B. Kim, J.D. Song and Y.H. Song

The memory characteristics of a capacitor with polycrystalline gallium arsenide (poly-GaAs) as a floating gate material have been evaluated, and compared with a capacitor using poly-silicon (poly-Si). The poly-GaAs film with thickness of 100 nm was successfully grown on silicon at 250°C, using an arsenide beam flux, in a molecular beam epitaxy chamber. Based on the optical and electrical evaluation, this film appeared to have obvious poly-GaAs. Here, the measured memory window by comparing it to a conventional device with a poly-Si floating gate, which showed it to have approximately twice the value of the poly-Si. Based on these results, poly-GaAs floating material can be considered to be a candidate for a wider memory window in scaled two-dimensional flash memory.

Introduction: Recently, two-dimensional NAND flash memory has been scaled-down beyond 20 nm technology, but it still faces several scaling issues. Among them, a narrowing memory window for the scaled cell is a very serious issue for multi-bit operation. The memory window is dependent on the trap density of the floating gate material, coupling ratio, and interference due to the neighbouring cell etc. [1-6]. Up until now, structural investigations into the coupling ratio and interference issue have been performed to sustain the memory window in the scaled NAND flash memory. However, the studies into the floating gate material have not yet been reported, in view of the memory window. Poly-silicon (poly-Si) material has been used as a floating gate in NAND flash memory due to its superior characteristics such as scalability, process feasibility, and thermal stability [7, 8].

In this letter, we study the improvement of the memory window via the application of polycrystalline gallium arsenide (poly-GaAs), instead of poly-Si, as a floating gate material for the first time. It is known that GaAs provides very good electrical isolation between the devices and circuits, and is a semi-insulating (SI) material. In addition, Si-GaAs has significant traps, with its major trap level being the EL2 level of 10^{12}–10^{13} cm^{-3} [9]. The interface between the SiO2 and GaAs has a significant lattice mismatch, which gives a larger interface trap state density of 6 × 10^{18}–10^{19} cm^{-2} eV^{-1} [10], while it is ~10^{12} cm^{-2} eV^{-1} between the silicon and SiO2 [10]. Based on the expectation of higher trap densities in the bulk and interface for GaAs material, the memory window of the capacitor pattern with a GaAs floating gate was compared to one with a poly-Si floating gate, confirming the possibility of a candidate material in sub-20 nm NAND flash memory.

Fabrication: A P-type Si (100) wafer was prepared by pre-cleaning; then, thermal dry oxidation with a 10 nm thickness was performed at 900°C. A polycrystalline GaAs layer was grown on cleaned sample using a Riber Compact 21E solid source molecular beam epitaxy (MBE) system. To obtain high quality GaAs layer, the main chamber was kept in an ultra-high vacuum at 3 × 10^{−10} Torr. The sample was loaded into the main chamber; then, a floating layer of 0.1 μm was grown oxide under the conditions of 1.82 A/s, at 250°C, with an operation vacuum level of (3 × 10^{−4} Torr) and a (1 × 10^{−5} Torr) arsenic source flux. The SiO2, as block oxide on the grown sample, was deposited using low pressure chemical vapour deposition (LPCVD). The gate material, using titanium (50 nm) as a barrier layer and platinum (100 nm) was deposited by electron beam evaporation. For the reference, a capacitor with poly-Si was fabricated under the same geometric conditions.

Device characteristics and discussion: To confirm the crystallinity of the GaAs, the fast Fourier transform (FFT) method was used in a high magnification transmission electron microscopy (TEM) image at a scale bar of 10 nm. Fig. 1 shows the FFT pattern with grain boundary, which demonstrate the polycrystalline growth on the SiO2. The Hall measurement at 300 K typically shows an electron mobility of 2400 cm²/Vs, which is higher than that of Si. Based on these results, it was confirmed that the poly-GaAs was grown successfully.

Fig. 2 shows a low magnification TEM cross-sectional image of the capacitor with floating poly-GaAs, and the multi-layers consisting of a metal gate (platinum: 100 nm, titanium: 50 nm), block oxide (50 nm), tunnel oxide (10 nm), and silicon substrate. The aerial of the top electrode is 500 × 500 μm².

Fig. 3a shows the C–V characteristics of those cells whose floating gates consist of poly-GaAs and poly-Si; the C–V measurement was conducted using an Agilent/HP 8110A Pulse generator. The inset shows the saturation of the memory window, and while one poly-Si is saturated to 3 V at a sweep bias of 14 V, one poly-GaAs shows 5.5 V at a bias of 22 V.

Fig. 3b shows the 10 nm C–V characteristics of both poly-GaAs and poly-Si flash cell. The inset shows the C–V characteristic with a flat band voltage (VFB) with applying sweep voltage from −24 to 24 V. Fig. 3b shows the average value of memory window with 40 cell samples.
At the same voltage from −24 to 24 V, the poly-Si is 3.2 V and poly-GaAs is 5.6 V. Based on these results, we confirmed that the window margin of the poly-GaAs has a value 1.8 times larger than that of the poly-Si. Fig. 3b shows the average value of the memory window after measuring 40 cell samples with a sweep voltage ranging from −24 to 24 V. We confirmed that more than 60% of the measured cells have poly-Si at 3 V and poly-GaAs at 5.5 V. However, the memory window is small because the gate coupling is very low due to thick block oxide (50 nm). We need further investigation for a capacitor with nominal coupling ratio (> 0.5) by an application of thinner block oxide or oxide/nitride oxide/film.

Conclusion: In this Letter, poly-GaAs has been proposed as a floating gate material instead of poly-Si. It is expected to improve the memory window with a large trap density between the poly-GaAs and SiO2. We have demonstrated that the proposed cells show sufficient memory window of 5.6 V at a sweep voltage ranging from −24 to 24 V. This result reflects a 1.8 times larger window margin than that of the poly-Si under the same geometric conditions. Therefore, it is expected that this will be a good candidate material for wider memory window in sub-20 nm NAND flash memory.

Acknowledgments: This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning (NRF-2015R1A2A2A01007289). The authors in KIST acknowledge the partial support from the KIST institutional program.

© The Institution of Engineering and Technology 2016

Submitted: 17 December 2015 E-first: 28 April 2016 doi: 10.1049/el.2015.3823

One or more of the Figures in this Letter are available in colour online.

I.P. Roh, N.S. Kang, S.H. Shin, Y.T. Oh, K.B. Kim and Y.H. Song (Department of Electronics and Communications Engineering, Hanyang University, Seoul, Republic of Korea)

✉ E-mail: yhsong2008@hanyang.ac.kr

J.D. Song (Center for Opto-Electronic Materials and Devices, Korea Institute of Science and Technology, Seoul 136-791, Republic of Korea)

References
1 Goda, A., and Parat, K.: ‘Scaling directions for 2D and 3D NAND cells’. IEEE Int. Electron Devices Meeting, San Francisco, CA, USA, December 2012, pp. 2.1.1–2.1.4, doi: 10.1109/IEDM.2012.6478961
2 Kim, K.: ‘Future memory technology: challenges and opportunities’, VLSI-TSA, April 2008, pp. 5–9, doi: 10.1109/VTSA.2008.4530774
3 Kim, Y.S., Lee, D.J., Lee, C.K., Choi, H.K., Kim, S.S., Song, J.H., Song, D.H., Choi, J.H., Suh, K.D., and Chung, C.: ‘New scaling limitation of the floating gate cell in NAND flash memory’. IEEE Int. Reliability Physics Symp. (IRPS), Anaheim, CA, USA, May 2010, pp. 599–603, doi: 10.1109/IRPS.2010.5488765
4 Seo, S., Kim, H., Park, S., Lee, S., Antome, S., and Hong, S.: ‘Novel negative Vt shift program disturb phenomena in 2X−3X nm NAND flash memory cells’. IEEE Int. Reliability Physics Symp. (IRPS), Monterey, CA, USA, April 2011, pp. 6B.2.1–6B.2.4, doi: 10.1109/IRPS.2011.5784548
5 Lee, S.: ‘Scaling challenges in NAND flash device toward 10 nm technology’. IEEE Int. Memory Workshop (IMW), Milan, Italy, May 2012, pp. 1–4, doi: 10.1109/IMW.2012.6213636
6 Bez, R., Camerlenchi, E., Modelli, A., and Visconti, A.: ‘Introduction to flash memory’, Proceedings of the IEEE, 2003, 91, pp. 489–502, doi: 10.1109/JPROC.2003.811702
7 Kim, T.K., Chang, S., and Choi, J.H.: ‘Floating gate technology for high performance 8-level 3-bit NAND flash memory’, Solid-State Electron., 2009, 53, pp. 792–797, doi: 10.1016/j.sse.2009.03.019
8 Kamigaichi, T., Arai, F., Nisuta, H., et al.: ‘Floating gate super multi-level NAND flash memory technology for 30 nm and beyond’. IEEE Electron Devices Meeting, San Francisco, CA, USA, 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796825
9 McGregor, D.S., Rojeski, R.A., Knoll, G.F., Terry, F.L. Jr, East, J., and Eisen, Y.: ‘Evidence for field enhanced electron capture by EL2 centers in semi-insulating GaAs and the effect on GaAs radiation detectors’, J. Appl. Phys., 1994, 75, pp. 7910–7915, doi: 10.1063/1.356577
10 Helms, C.R., and Deal, B.E.: ‘The physics and chemistry of SiO2 and the Si-SiO2 interface 2’ (Plenum Press, New York, 1993, 1st edn.)

ELECTRONICS LETTERS 26th May 2016 Vol. 52 No. 11 pp. 963–965