Dendritic-Inspired Processing Enables Bio-Plausible STDP in Compound Binary Synapses

Xinyu Wu, Student Member, IEEE and Vishal Saxena, Member, IEEE

Abstract — Brain-inspired learning mechanisms, e.g. spike timing dependent plasticity (STDP), enable agile and fast on-the-fly adaptation capability in a spiking neural network. When incorporating emerging nanoscale resistive non-volatile memory (NVM) devices, with ultra-low power consumption and high-density integration capability, a spiking neural network hardware would result in several orders of magnitude reduction in energy consumption at a very small form factor and potentially herald autonomous learning machines. However, actual memory devices have shown to be intrinsically binary with stochastic switching, and thus impede the realization of ideal STDP with continuous analog values. In this work, a dendritic-inspired processing architecture is proposed in addition to novel CMOS neuron circuits. The utilization of spike attenuations and delays transforms the traditionally undesired stochastic behavior of binary NVMs into a useful leverage that enables biologically-plausible STDP learning. As a result, this work paves a pathway to adopt practical binary emerging NVM devices in brain-inspired neuromorphic computing.

Index Terms— Brain-Inspired Computing, Crossbar, Neuromorphic Computing, Machine Learning, Memristor, Emerging Non-Volatile Memory, RRAM, Silicon Neuron, Spike-Timing Dependent Plasticity (STDP), Spiking Neural Network.

I. INTRODUCTION

Brain-inspired neuromorphic computing has been attracting a lot of interest recently; deep neural networks and deep learning are quickly shaping modern computing industry and human society with their outstanding performance in imaging pattern recognition, speech recognition, natural language processing, and autonomous driving and flight. However, while running on modern CPU, GPU or FPGA platforms enabled by the most advanced complementary metal-oxide semiconductor (CMOS) technologies, these computing machines are very power hungry and still require several orders of magnitudes higher energy compared to their biological analogs, as well as need specialized programming. Recently, brain-inspired neuromorphic hardware have demonstrated impressive ultra-low power performance in implementing convolutional neural networks [1] by leveraging massive parallelism and event-driven spiking neural processing techniques. However, it cannot adjust the synaptic weights while in operation; moreover, in view of the foreseeable physical limitations, CMOS based brain-inspired computing integrated circuits (ICs) will not amenable to accommodate a neural network comparable to the level of human cortex in terms of synaptic density and power consumption.

In the past decade, the discovery of spike-timing-dependent-plasticity (STDP) mechanisms and the emergence of nanoscale non-volatile memory (NVM) devices have opened a new avenue towards the realization of brain-inspired computing. Prior research suggests that STDP can be used to train spiking neural networks (SNNs) with resistive random-access memory (RRAM) synapses in-situ, without trading-off their parallelism [2], [3]. Further, these devices have shown low-energy consumption to change their states and very compact layout footprint [4]–[9]. Hybrid CMOS-RRAM analog very-large-scale integrated (VLSI) circuits have been proposed [10], [11] [20, 21] to achieve dense integration of CMOS neurons and emerging devices for neuromorphic system-on-a-chip (NeuSoC). Fig.1a illustrates a NeuSoC architecture where a three layer fully-connected spiking neural network is envisioned. Here, the input layer encodes the real-valued inputs into spatiotemporal spike patterns, and the subsequent layers process these inputs using STDP-based unsupervised or semi-supervised learning [12]–[18]. The neurons in each of the layers are connected to the higher layers using synapses that hold the ‘weights’ of the SNN. As shown in Fig.1b, an NVM crossbar array is used to form synaptic connections between the two layers of neurons. The spiking neurons in the second and higher layers implement competitive learning using a winner-take-all shared bus mechanism where the neuron that spikes first for an input pattern, inhibits the rest of the neurons in the same layer [37]. Using a combination of STDP and WTA-based learning rules, the synapses are locally updated through the interaction of pre- and post-synaptic neuron spikes (Fig.1c) that results in network learning in the form of the fine-grained weight (or conductance) adaptation in the synapses. The presented

Xinyu Wu and Vishal Saxena are with the Electrical and Computer Engineering Department, University of Idaho, Moscow, ID 83844, USA (email: vsaxena@uidaho.edu)
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Fig. 1. Envisioned Neuromorphic SoC architecture: (a) A fully-connected spiking neural network showing input, hidden and output layers comprised of spiking neurons, with synaptic connections shown for one neuron in the hidden and output layers; (b) A section of the neural network architecture implemented using RRAM crossbar memory array and column/rows of mixed-signal CMOS neurons with winner-take-all (WTA) bus architecture for competitive learning; (c) A single multi-bit synapse between the input (pre-synaptic) and output (post-synaptic) neurons that adjusts its weight using STDP; (d) The architecture leverages 2D arrays and peripheral circuits used in memory technology to achieve high-density spiking neural network hardware motifs.

The architecture is very similar to existing memory architectures, where the devices are arranged in a dense two-dimensional array with the input and output neurons forming the peripheral circuitry, laid out at a matching pitch with the memory array (see Fig. 1d). This layout forms a repeatable motif which can be scaled to deeper SNN architectures. Thus, such a NeuSoC architecture can achieve highest area density aided by nanoscale NVM devices and compact mixed-signal neurons. Extension to larger 3D IC architectures using thru-silicon-via (TSVs) provides a natural pathway for further scaling to very high integration density and network complexity without resorting to the overhead incurred by asynchronous communication protocols such as the address-event-representation (AER).

Ideally, non-volatile analog-like weights are required for effective STDP learning. However, majority of practical small-sized RRAM devices exhibit abrupt switching behavior, which consequently limits the stable synaptic resolution to 1-bit (or binary, bistable). Furthermore, their switching probability and switching times typically depend upon the voltage applied across the device, as well as the duration of the voltage pulse [19]–[24]. To circumvent the binary resolution of devices, compound memristive synapse with multiple bistable devices in parallel was recently proposed to emulate analog weights on average [23], [25], [26]. However, we will show that this compound synapse only yields a simple linear STDP learning function.

This work proposes a new concept where dendritic-inspired processing is added to the compound synapse, along with necessary modifications to the CMOS neuron circuit. This architecture introduces two additional set of parameters to the spike waveforms: amplitude modulation and additional temporal delays. They, in turn, enable nonlinear STDP learning functions, e.g. exponentially shaped window that appears in biological neural electrophysiology, and has been found critical for guaranteeing computing stability and efficiency in theoretical analyses [27]–[29]. Therefore, this is an important step towards integrating practical binary NVM devices, employed in stochastic operating regime, to realize synapses with multi-bit resolution; a breakthrough can lead to practical realization of large-scale spiking neural networks on a chip. Leveraging the bistable probabilistic switching, we specifically demonstrate in this work that the proposed compound synapse with dendritic-inspired processing can realize multi-bit resolution plasticity in synapses with complex non-linear STDP learning functions, including the highly desired exponential one needed for spike-based learning [29]. Therefore, inclusion of even simple dendritic behavior unlocks the computing effectiveness of STDP without any limitations of realistic synaptic device behavior. The novelty of this work is that it combines bistable RRAM devices, that are inherently stochastic, to be used in parallel with simple dendrites with simple circuit structures implementing delay and/or attenuation in event-driven CMOS neurons, to realize higher resolution weights. Simulation results have shown that a STDP learning behavior similar to biological plasticity can be recreated with the proposed concept.

The rest of this article is organized as follows: Section II reviews the STDP learning and its realization in emerging NVM devices; Section III introduces the proposed dendritic-inspired processing architecture and the respective circuitry; Section IV presents the experimental setup and results; finally, Section V estimates the energy-efficiency of the architecture, discusses current limitations, and presents future investigations.

II. STDP LEARNING AND EMERGING NVM DEVICES

Spike-timing dependent plasticity (STDP) is a mechanism that uses the relative timing of spikes between pre- and post-synaptic neurons to modulate synaptic strength. It was first formulated in spiking neural network simulations without considering it as a biologically plausible mechanism [30]; while observed in in vivo experiments of cortical pyramidal cells [31] and many other neuroscience experiments conducted later [31]–[36]. The well-known pair-wise STDP states that the strength of synapse connection is modulated according to the relative timing of the pre- and post-synaptic neuron firing. As illustrated in Fig. 2A, a spike pair with the pre-synaptic spike arrives before the post-synaptic spike results in increasing the synaptic strength (or potentiation); a pre-synaptic spike after a post-synaptic spike results in decreasing the synaptic strength (or
Changes in the synaptic strength $\Delta w$, plotted as a function of the relative arrival timing, $\Delta t$, of the post-synaptic spike with respect to the pre-synaptic spike is called the STDP function or learning window. A typical STDP function, $\Delta w$, is a double-exponential function

$$
\Delta w = \begin{cases} 
A_+ e^{-\Delta t/\tau_+}, & \text{for } \Delta t > 0 \\
A_- e^{\Delta t/\tau_-}, & \text{for } \Delta t < 0
\end{cases}
$$

(1)

where $A_+$, $A_-$, $\tau_+$, and $\tau_-$ are the parameters that control the shape of the curve. Further experiments have shown that the relative voltage of the pre- and post-synaptic spike pair is more fundamental than the spike timing [35], [37]. Theoretical studies have revealed that STDP learning rule enables unsupervised local learning in spiking neural networks by realizing Bayesian expectation-maximization algorithm [29], and hidden Markov models [38]. Moreover, a nonlinear STDP learning function, e.g., exponentially shaped window that appears in biological neural systems, is critical for guaranteeing computing stability and efficiency [27]–[29].

As mentioned earlier, emerging NVM devices are being considered as an enabler of realizing large-scale neuromorphic hardware. Emerging NVMs, including phase change memory (PCM), resistive random-access memory (RRAM) and spin-torque-transfer random-access memory (STT-RAM), have been demonstrated to realize STDP-like switching characteristics [4], [5], [7]–[9], [39]–[43]; while enabling highly desired advantage of small silicon area of $4F^2$ ($F$ is the feature size of the semiconductor fabrication process) [44], ultra-energy-efficient operation of sub-pico-Joule per switching event, CMOS compatibility, and dense crossbar (or crosspoint) arrays and 3D integration.

Specially, RRAM devices behave like the biological synapses in several aspects. Besides having their conductance to be equivalent to the synaptic strength (or weight) and that the conductance can be modulated by voltage pulses, RRAMs realize STDP directly with identical pair-wise spikes. As illustrated in Fig. 2B, the net potential $V_{\text{net}}$ created by a pre-synaptic spike and a late arriving post-synaptic spike, with $\Delta t > 0$, produces an over-threshold ($V_{\text{th}+}$) portion $V_{\text{eff}}$, and then, causes an increase in conductance in a typical bipolar RRAM. The intrinsic stochastic switching of a typical bipolar RRAM shows the change $\Delta w$ of which the over-threshold portion ($V_{\text{th}+}$) may cause the RRAM resistance to switch. (C) Abrupt switching and stochastic switching of a typical RRAM device, adapted from [46].
neural network computing, and a simulation demonstrated that a 4-bit compound synapse (16 memristors in parallel) is able to achieve a comparable accuracy on a 2-layer fully-connected neural network with MNIST handwritten digits dataset. At the same time, a simulation work in [26] also suggested it is possible to create biological plausible STDP learning window using a compound binary synapse. However, no circuit implementation or practical method to control the shape of the learning window was provided.

Thus, in order to unlock the STDP-based learning in SNN hardware, a solution to enable non-linear, especially exponential, STDP learning function with binary RRAMs is highly desired and investigated in this work.

III. DENDRITIC PROCESSING ARCHITECTURE AND CIRCUITS

The role of active dendrites in neural cells in the computing ability has been studied in [48] where it was shown that nonlinear dendritic processing enhances the ability to learn patterns with low resolution synapses. Recent work in neuromorphic computing in [49], [50] implemented a reservoir readout layer that used the dendritic concept provided in [48] to improve the classification performance. Here, nonlinear dendritic processing circuits were used to achieve learning with analog synapses (realized using CMOS transistors) with binary long-term storage. However, to the best of our knowledge, dendritic-inspired processing with nanoscale NVMs, and the associated spike waveform engineering, have not been explored prior to our work.

To leverage RRAM in the compound synapse with non-linear spike-timing-dependent switching probability, a dendritic-inspired processing stage is applied to the pre-synaptic neuron output as shown in Fig. 3A. Here, a single-layer neural network is implemented using the crossbar architecture with a RRAM devices as electrical synapses; synapses interconnect pre- and post-synaptic neurons at each crosspoint. In this configuration, we don’t use the nonlinearity of active dendrites as in [48-50], but instead introduce simple circuit modifications such as delay and spike amplitude variations, hence terming it as “dendritic-inspired” processing. The novelty of this work is that it combines bistable (or binary) RRAM devices that are inherently stochastic, to be used in parallel with simple dendrites with varying delay and/or attenuation to realize higher resolution nonlinear STDP learning. Also, the use of dendrites with nanoscale NVM devices is a natural fit as it doesn’t incur area penalty as several rows/columns of memory devices can be laid out on the pitch of the CMOS neurons. Also, separating the attenuating buffers for each dendrite helps reduce the resistive loading, and thus the current drive needed to drive the load by the neuron.

The presented neuron in Fig. 3A is adapted from our previous experimental demonstration of RRAM-compatible spiking neuron integrated circuits [10], [11], [45]. Here in contrast to Fig. 1b, the original spike waveform from the pre-synaptic neuron runs through multiple dendritic branches before reaching the binary synaptic devices, and the spike amplitudes are reduced in these branches depending on their attenuation. Since the synaptic devices’ switching depends on the voltage and pulse duration applied across their two terminals, these post-dendritic spike waveforms produce several different voltage amplitudes and cause the respective synaptic devices to switch with different probabilities (assuming same pulse duration for each device). The greater the post-dendritic spike amplitude, the higher probability of switching; the lower the post-dendritic spike amplitude, the lesser probability of switching.

From statistical standpoint, the average conductance of the compound synapse \( G_{cs} \) with \( n \) binary RRAM devices in parallel under a given voltage \( V_i \) can be written in a mathematical expression as

\[
G_{cs}(V) = \sum_{i=1}^{n} p_i(V_i) \frac{1}{R_{ON,i}} + \sum_{i=1}^{n} (1 - p_i(V_i)) \frac{1}{R_{OFF,i}},
\]

where \( p_i \) is the SET switching probability of the \( i^{th} \) device, and...
\( R_{\text{ON}} \) and \( R_{\text{OFF}} \) are the RRAM resistances in the ON and OFF states respectively. Generally, \( R_{\text{OFF}} \) is greater than \( R_{\text{ON}} \) by several orders of magnitude [51], and thus, can be neglected in overall conductance. Furthermore, assuming \( R_{\text{ON}} \) of all devices are the same*, a simplified expression for Eq. (1) is

\[
\bar{u}_{\text{cm}}(V) = \frac{1}{R_{\text{ON}}} \sum_{i=1}^{n} p_i(V_i). \tag{2}
\]

Noting that the devices are operated in probabilistic switching regime, and each device switches differently with respect to the time difference between the pre- and post-spikes (\( \Delta t \))

\[
V_i = f(\Delta t), \tag{3}
\]

Thus, the combined effect of parallel RRAMs could approximate a nonlinear function if \( p_i \) and \( V_i \) are not linear functions at the same time. Therefore, the proposed dendritic processing provides additional degrees of freedom to manage the amplitudes and relative timing of spikes. With appropriate design, the proposed concept able to approach biology-like exponential functions (see an example in the Appendix).

In terms of circuit realization, each dendritic branch is implemented by adding an attenuator to the CMOS soma output using compact circuitry as shown in Fig. 3B. Some of the several possible realizations can be a resistor, or diode-connected MOSFET, ladder followed by source follower buffers, or parallel buffers with varying attenuations. In detail, noting the spike waveform generated by the spike generator as \( V_s^a \) and \( V_s^b \), dendritic processing generates \( n \) post-dendritic spikes

\[
\begin{align*}
  V_{p_{di}}^+ &= \alpha_i V_{a}^+, & \text{while } i = 1,2,\ldots,n \\
  V_{p_{di}}^- &= \alpha_i V_{a}^-,
\end{align*}
\]

where \( V_{p_{di}}^+ \) and \( V_{p_{di}}^- \) is the positive and negative amplitudes of the \( i \)th post-dendritic spike, and \( \alpha_i \) is the attenuation factor of the \( i \)th dendritic branch.

Besides the amplitude attenuation, time delays could be also introduced into the dendritic processing. Noting the spike waveform generated by the spike generator as \( V_s \), then the dendritic processing generates \( n \) post-dendritic spikes

\[
V_{p_{di}} = V_s(t + \Delta t), \quad \text{while } i = 1,2,\ldots,n \tag{5}
\]

where \( \Delta t \) is the delay of the \( i \)th dendritic branch.

The CMOS soma can be implemented as an integrate-and-fire circuit with a winner-takes-all (WTA) mechanism in an event-driven triple-mode architecture based on a single opamp, as previously presented by us in [10], [11], [45]. In the integration-mode configuration, the CMOS soma is designed to provide a constant voltage at the neuron’s current summing input, and allows reliable and linear spatio-temporal spike integration by charging membrane capacitor, with the inflowing currents flowing through the passive resistive synaptic devices. In the firing-mode configuration, the CMOS soma generates STDP-compatible spike and drives the spikes propagating in both forward as well as backward directions with high energy-efficiency. In the discharge-mode, this soma circuitry supports local learning with several neurons organized in a group and becomes selective to input patterns through competition and lateral inhibition with a shared WTA bus [10].

It is worthwhile to note that dendritic attenuation and delay are natural phenomenon and intrinsic properties of biological neurons. A biological dendritic tree has much higher resistance than metal interconnection in semiconductor chips, then, yield a larger attenuation to the spike amplitude. For examples, in a biophysical simulation, the synaptic potential close to the center of soma is 13 mV whereas the potential is approximately 0.014 mV at the end of the dendritic tree which is a more than 900-fold attenuation [52]; while the simulation in this work will use attenuation factors less than 2-fold.

IV. EXPERIMENTS

A. Setup

The stochastic switching of the RRAM synapse is modeled by the cumulative probability of a normal distribution as experimentally demonstrated in [53]

\[
p(V) = \int_{0}^{V} \frac{1}{\sqrt{2\pi}\sigma^2} e^{-\frac{(x-V_{\text{th}})^2}{2\sigma^2}} \, dx, \tag{6}
\]

where \( p(V) \) is the SET or RESET switching probability under net potential \( V \) applied across the two terminals of the RRAM;
V_th is the mean of threshold voltage, and σ is the standard deviation of the distribution. Here, for demonstration purpose we choose V_th^+ = 1V and V_th^- = -1V for the positive and negative thresholds respectively, with σ = 0.1.

During simulation, the timescale and change in conductance were normalized for convenience. A simulation step of 0.01 was used, and the delay of circuits were ignored except the delay implemented in dendritic processing unit as described earlier. A total of 10,000 epochs were performed to generate stochastic data for each simulation.

The whole neural circuit with dendritic neurons and synapses was modeled and simulated with Python 2.7 in Linux Mint 18 environment and on an Intel Core-i5 6600 quad-core CPU running at 3.5GHz. Each simulation took approximately 7.5 seconds.

### B. Stochastic STDP with Exponential Learning Function

In the first simulation, a circuit hardware-friendly spike waveform [2], [10] as shown in Fig. 4A is selected. This half-rectangular-half-triangular (HRHT) spike waveform has a constant positive shape and a linearly rising negative tail, and has been demonstrated on a CMOS neuron chip by the authors [11]. The positive tail of the spike has 0.9V amplitude and spans 1 time unit; the negative tail has a peak amplitude of 0.4V and spans 5 time units.

Without dendritic processing, a pair of spike was applied to a compound synapse with 16 RRAM devices in parallel. In this scenario, the attenuating factors α_i = 1, or simply, the terminals of these devices are connected to one node. The simulation results for stochastic STDP learning is shown in Fig. 4B. Here, each dot represents the state of conductance of the compound synapse, and the LRS variation of RRAMs is modelled as a normal distributed random variable with standard deviation of 0.1. By connecting 16 binary devices in parallel, this simple compound synapse achieves 4-bit weight resolution through STDP leaning, however, the learning curves are linear, i.e. have a linear best fit, due to the same switching probability for all the devices in parallel.

With dendritic processing applied to the pre-synaptic spike, the attenuating factors α_i of the dendritic attenuators were set to values linearly spanning from 0.6 to 1, and produced 16 positive and 16 negative levels as shown in Fig. 4C; while the postsynaptic spike remained a single waveform same to the one shown in Fig. 4A. The simulation result is shown in Fig. 4D, and it can be discerned that the STDP learning windows is significantly different from the previous one in Fig. 4B. Interestingly on the left-hand panel, the conductance change shows a non-linear relationship to the relative time Δt, and an exponential curve fits well to it. Another significant difference between the two schemes is that the flat plateau in Fig. 4B for Δt in the range of -1 to 0 almost disappeared, while the plateau region narrowed down in the right-hand panel with Δt close to 0. Since the maximum net potential over the RRAM devices is same when only a portion of the pre-synaptic spike’s tail positive head overlaps with the post-synaptic spike’s negative tail, the switching probabilities of the parallel devices are also the same and equal to 1 in this design. Ideally, this plateau can be eliminated by using a very narrow positive tail for the spike waveform which corresponds to faster switching characteristics for the RRAM device.

Fig.5 provides a closer look to the impact of dendritic processing on the overall STDP learning. Fig. 5A shows the effective potential V_eff over parallel devices versus the relative arrival times of post- and pre-synaptic spikes. Here, 16 voltage levels are created over V_th^+ and V_th^- for Δt >0 and Δt < 0 respectively. As a result, they produce 16 levels of conductance change as shown in Fig. 5B. In this plot, each dot represents a non-zero probability of conductance change without taking the values of probability into consideration and by ignoring LRS variations.

Fig. 5C plots the individual switching probability of the 16 devices versus Δt. With the attenuated amplitudes in the dendrites, the switching probabilities of these 16 devices decreased and entered into non-switching status (0 switching probability) successively in the left-hand panel. As shown in the Appendix, the successive shifting of switching probability from non-zero to zero introduces a quadratic term in the compound synapse, and thus produces the approximated exponential curve. One can also find that the RRAMs’ switching probability curves are dense in the left-hand panel, due to the smaller amplitude of the spike’s negative tail than its positive head. Dense probability curves yield narrow span of their combined
distribution, and are easier to saturate, especially when the positive head of pre-spike partially overlaps with the post-spike and creates a smaller change to the net potential with respect to Δt. In this simulation, almost a half of the RRAM devices were saturated when Δt is in the range of 0 to 1.

Another view is shown in Fig. 5D, which depicts the probability of the compound synapse to occupy each of the normalized conductance states. It shows that the state-wise probability curves are spaced with exponential increments in time.

The HRHT spike waveform used in this simulation is very easy to realize in CMOS circuits and produces a single exponential curve in the STDP learning function. However, in the other positive half, the curve fit follows a straight line with a linear decrease for most of the time; while has a small exponential decreasing tail at the far end. Consequently, other waveform shapes were explored to realize a biology-like double-exponential STDP.

C. Other Stochastic STDP Learning Functions

Several other spike waveform shapes were also simulated and the results are illustrated in Fig. 6. In this figure, the spike waveforms with dendritic processing are shown in the first row while waveforms without dendritic processing will correspond to the ones with largest peak-to-peak swing. The respective STDP learning functions without dendritic processing are shown in the second row, and the corresponding STDP learning functions with dendritic processing are shown in the third row.

A widely employed simple rectangular spike produces a rectangular STDP learning widow with dendritic processing, as shown in Fig. 6A. It is easy to observe that the switching probability of the RRAM devices remains unchanged in the learning window because the amplitude of the spike waveform is independent of the relative timing. Hence, there isn’t a quadratic term which can be introduced into the design.
Double sawtooth and double exponential spike waveforms were simulated and the results are shown in Fig. 6B and 6C. Similar to the waveform of Fig. 4C, dendritic processing introduced nonlinearity into the STDP learning window. Due to the sharp curves in the spike waveforms, both of them produced curves of STDP learning functions that eliminated the plateau and approximated to a double-exponential function as shown in Fig. 2A and formulated in Eq. (1).

A biologically plausible spike was also simulated and shown in Fig. 6D. Dendritic processing introduced nonlinearity into the STDP learning window for this waveform as well; whereas conductance changes are also found around the $\Delta t = 0$ region due to the smooth change of the positive and negative tails in this waveform.

In the case of a STDP learning function where a double-exponential curve is desired for a VLSI implementation, the sawtooth waveform is a good choice because it is easier to realize in circuits compared to the exponential or the biological-plausible spike waveforms.

**D. Incorporating with Dendritic Delay**

Propagation delay is another parameter which can be implemented into the dendritic processing architecture. To find the impact of the dendritic delay, a 0.3 time-unit delay was used in this simulation which accounts for 5% of the 6 time-unit total waveform span.

As shown in Fig. 7, HRHT, double sawtooth, double exponential and biological plausible spike waveforms were applied. With time delays, all of them produce conductance change probability around $\Delta t=0$, as few dots that can be seen at the two sides of $y$-axis, and a wider distribution of dots towards $y$-axis. Time delays also reduce the probability of large conductance change due to the shift in the pairwise spike peaks (this problem can be resolved by choosing appropriate waveform amplitudes or attenuation factors). Interestingly, the double-exponential spike waveform created a STDP learning function very similar to the in vivo measured biological STDP seen in Fig. 2A. This waveform with dendritic delays can be used to realize an STDP response that is highly faithful to the biological measurements.

**V. DISCUSSION**

**A. Energy Efficiency**

The primary motivation of exploring memristive (or RRAM-based) spiking neural network is the potential energy efficiency saving comparing to conventional computing paradigms. This goal could be achieved from two aspects: the event-driven asynchronous architecture of SNN, and the ultra-low-power memory devices. In an SNN, the spike shape parameters and the ON state resistance $R_{ON}$ of the memristive devices ($R_{OFF}$ is generally several orders of magnitude greater than $R_{ON}$, and thus can be neglected) contribute to the energy computation of one spike event; while the total energy consumption is also decided by the percentage of RRAM devices in ON state, spike activity, and the power consumption in the neurons.

Taking the HRHT waveform with tall and thin positive rectangular head and a short and fat negative triangular tail as example, the pulse shape is defined as:

$$V_{spk}(\Delta t) = \begin{cases} 
A_+ & \text{while } \tau_- < \Delta t < 0 \\
-A_- \left(1 - \frac{\Delta t}{\tau_+}\right) & \text{while } 0 < \Delta t < \tau_+,
\end{cases}$$

(8)

where $A = A_+ + A_-$ is the peak-to-peak amplitude of the waveform, and $\tau_-$ and $\tau_+$ are the positive and negative tail duration respectively. Then, energy consumption of one spike over a memristor device with ON resistance $R_{ON}$ is given by
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\[ E_{spk} = \frac{A_{\alpha}^2}{R_{ON}} \tau + \int_0^{\tau} \left[ -A_{\alpha} \left( 1 - \frac{t}{\tau} \right) \right]^2 dt, \tag{9} \]

and the total SNN energy consumption for one event can be formulated as

\[ E_{SNN} = \eta_{act} \eta_{ON} s E_{spk} + n P_{neuron} \tau, \tag{9} \]

where \( \eta_{act} \) is neuron activity ratio, \( \eta_{ON} \) is ON-state RRAM ratio in the SNN, \( s \) is the number of synaptic connections, \( n \) is the number of neurons, \( P_{neuron} \) is neuron power and \( \tau = r + r \) is the spike duration.

For instance, the well-known AlexNet convolutional neural network for deep learning is built with 61 million synaptic connections and 640 thousand neurons. With a conservative estimation based on the spiking neuron chip realization in [11] and 4-bit compound binary synapse, the energy consumption for processing of one image is 62 \( \mu \)J, as shown in Table 1. By comparing with the today’s most advanced GPU Nvidia P4 for deep learning [54], it could provide a better energy-efficiency of 94-fold. Noting a great room for improvement in the CMOS design in [11], high-LRS memristor devices (>10MΩ) and fast STDP (<50 ns) have been demonstrated, and penitential low neuron activity ratio, a 11 thousand-fold energy efficiency improvement could be a reasonable target for a SNN on a hybrid CMOS-RRAM chip.

Table 1. Energy Efficiency Estimation of Memristor Based SNN

| Spike Duration | Conservative | Medium | Aggressive |
|----------------|--------------|--------|-----------|
| \( \tau \)     | 500 ns       | 50 ns  | 5 ns      |
| \( \tau^* \)    | 2500 ns      | 250 ns | 5 ns      |
| Spike Amplitude | \( A^* \)    | 300 mV | 300 mV    | 300 mV |
| ON State Resistance | \( R_{ON} \) | 1 MΩ   | 10 MΩ    | 10 MΩ |
| Single Spike Energy | \( E_{spk} \) | 45 fJ  | 0.45 fJ  | 0.045 fJ |
| Neuron Baseline Energy | \( E_{neuron} \) | 70 pJ  | 700 pJ   | 35 nJ  |
| Neuron Act Ratio | \( \eta_{act} \) | 0.8    | 0.5      | 0.1    |
| On State RRAM Ratio | \( \eta_{ON} \) | 0.5    | 0.5      | 0.5    |
| Single Event Energy | \( E_{SNN} \) | 62 \( \mu \)J | 560 nJ | 25 nJ |
| Images / Sec / Watt | - | 16 k | 1.5 M | 41 M |
| Acceleration Ratio to GPU [54] | - | \( \times 94 \) | \( \times 11 k \) | \( \times 240 k \) |

For an aggressive estimation, the power consumption of neuron and \( R_{ON} \) are kept unchanged by considering steep slowdown in CMOS process evolution, and the signal-to-noise ratio (SNR) being fundamentally limited by the thermal noise [55]. However, a faster spike duration and much sparse neuron activity could be possible. With nano-second scale spike duration and 0.1 neuron activity, we could expect an energy-efficiency improvement of 240 thousand-fold.

**B. Limitations and Future Work**

This work proposes a dendritic processing architecture that provides a potential solution for implementing biologically plausible STDP and its realization using CMOS neuron circuits with stochastic binary RRAM devices.

Although the mathematical analysis of HRHT waveform proves that dendritic attenuation introduces a second order approximation of the exponential function, it was performed in terms of average conductance instead of the maximum probability. In this work, simulations were used to demonstrate that the produced STDP learning functions closely mimic the measured biological STDP. In order to provide analytical guidance for the spike waveform design, precise mathematical analysis in terms of probability of each conductance state is required to establish the relationship between the maximum probability and the relative timing, \( \Delta t \), and this could be a future theoretical work.

Besides the variations in the LRS, the noise in the waveform amplitude is also a practical parameter to be considered. Amplitude noise has impact on the switching of RRAM devices. It can shift device switching probabilities; cause switching probability to saturate at the higher end, and turn off the switching at the lower end. As a result, the amplitude noise can create undesired conductance change states or skip conductance states. Our simulations show that a normal distributed amplitude noise with standard deviation more than 0.05 significantly distorted the STDP learning window; and a noise with standard deviation less than 0.02 created a few additional conductance states while retaining shaped similar to the ideal STDP learning windows.

Finally, there have been a few theoretical studies on the impact of STDP learning function to learning in very simple neural networks [38], [56]. However, detailed study hasn’t been performed for a neural network of practical size, e.g. a multi-layer perceptron. It would be very interesting to understand the impact of STDP function to the overall network learning performance, including the stability, learning speed or convergence time, the resulting classification accuracy, and these metrics’ sensitivity to the variations in the STDP function. In a further step, when STDP is applied to state-of-the-art networks, like deep convolutional neural networks and recurrent neural networks, the impact of STDP function remains completely unknown and will form the bulk of our future study.

**VI. CONCLUSION**

The proposed compound synapse with dendritic processing realizes biologically plausible exponential STDP learning, while using practically feasible bistable nonvolatile memory devices with probabilistic switching. This can potentially create a breakthrough in ultra-low-power and significantly compact machine learning hardware for large-scale spiking neural networks that require synaptic plasticity with multibit resolution; a bottleneck in taking the next leap with the practical RRAM or memristive devices. Immediate applications will include practical realization of spike-based deep neural networks in a compact chip-scale form factor, with orders of magnitude reduction in energy consumption compared to GPUs and digital ASICs. Architectural exploration using the proposed compound probabilistic synapses can help benchmark the expected behavior from the emerging RRAM devices; nanoscale RRAM devices with large resistances will help realize lower power consumption.
APPENDIX: AN APPROACH TO EXPONENTIAL STDP CURVE

A. Approximation of Exponential Function

The exponential function can be expressed using Taylor expansion as

$$e^{-x} = \sum_{n=0}^{\infty} \frac{(-x)^n}{n!} e^{-x} \approx 1 - x + \frac{1}{2} x^2,$$  \hspace{1cm} (7)

when \( x \) is sufficiently small.

B. Model of Stochastic Switching

For an RRAM device with linear stochastic switching characteristics as shown in Fig.2, it is described by the equation

$$p(V) = \begin{cases} 1 & V \geq \frac{1}{\alpha} + V_{th} \\ \gamma(V - V_{th}) & V_{th} < V < \gamma^{-1} + V_{th}, \\ 0 & V \leq V_{th} \end{cases}$$ \hspace{1cm} (10)

where \( p \) the switching probability, \( V \) is the voltage across the device, \( V_{th} \) is the minimum threshold voltage, and \( \gamma \) is a constant which represents the slope of the switching function.

C. Model of Dendritic Processed Spike

Several spike shapes have been studied for STDP learning while they possess different levels of biological mimicry and hardware realization complexity. Here, the HRHT waveform with tall and thin positive rectangular head and a short and flat negative triangular tail is selected as Formulated in Eq. 9. This spike shape is widely used in widely used in simulation and CMOS neuromorphic implementations, while at the same time it is convenient for mathematical analysis.

When the proposed dendritic processing is applied to the pre-spike, the net potential \( V_i \) created by the \( i \)th pre-spike and the post-spike is

$$V_i(\Delta t) = (A_i - i\Delta V) + A \left(1 - \frac{\Delta t}{\tau_s}\right)$$ \hspace{1cm} (11)

$$= A - i\Delta V - \beta \Delta t,$$ \hspace{1cm} (12)

where \( A = A_i + A \) is the peak-to-peak amplitude of the waveform, \( \Delta V \) is the step of amplitude change, and \( \beta = A / \tau_s \).

D. Average Conductance

The value of greatest interest in this analysis is the maximum likelihood value of the conductance versus relative time difference, \( \Delta t \). However, it is very difficult to derive the analytic results for a general case. As an alternative, the average conductance is assumed as a reasonable approximation without providing explicit proof in this work.

To derive the relationship between average conductance \( \bar{g}_{cs} \) and relative timing \( \Delta t \), by substituting Eq. (9) and (10) into Eq. (2), we have

$$\bar{g}_{cs}(V) = \frac{1}{R_{on}} \sum_{i=0}^{n} \gamma(A - i\Delta V - \beta \Delta t - V_{th}).$$ \hspace{1cm} (13)

where all the waveforms have their switching probability less than one, and \( k \) is the index of the waveforms that have a smallest non-zero switching probability and is a linear function of \( \Delta t \)

$$k(\Delta t) = a_1 + b_1 \Delta t,$$ \hspace{1cm} (14)

Here \( a_i \) and \( b_i \) can be solved from Eq. (10) and Eq. (11)

$$a_i = \frac{1}{\Delta V}(A - V_{th}),$$ \hspace{1cm} (15)

$$b_i = \frac{\beta}{\Delta V}.$$ \hspace{1cm} (16)

Normalizing \( 1/R_{on} \) to a value of one for convenience and rearranging Eq. (13) we obtain

$$\bar{g}_{cs}(\Delta t) = (n - k)[\gamma(A - V_{th}) - \beta \gamma \Delta t] - \gamma \Delta V \sum_{i=k}^{n} i.$$ \hspace{1cm} (17)

In Eq. (17), the last term can be expressed as

$$\sum_{i=k}^{n} i = \frac{n(n + 1)}{2} - \frac{k(k + 1)}{2}.$$ \hspace{1cm} (18)

Substituting Eq. (15) and (16) into Eq. (17) and allocating the terms according to the order of \( \Delta t \), we get

$$\bar{g}_{cs}(\Delta t) = a - b \Delta t + c \Delta t^2,$$ \hspace{1cm} (19)

where the constant \( a \) is given by

$$a = \gamma(A - V_{th})(n - a_1) - \gamma \Delta V \frac{n(n + 1) - a_1(a_1 + 1)}{2}.$$ \hspace{1cm} (20)

The factor \( b \) of the first-order term is expressed as

$$b = b_1 \gamma \left[ \frac{1}{2} \Delta V (a_1 + 1) - \beta \right].$$ \hspace{1cm} (21)

By substituting \( a_1, b_1 \) and \( \beta \) into above equation, it is not difficult to find \( b > 0 \) as \( \tau_s > 2 \) and \( A > V_{th} \). The factor \( c \) of the second order term is

$$c = b_1 (\beta \gamma + b_1).$$ \hspace{1cm} (22)

As \( b_1, \beta \) and \( \gamma \) are all positive numbers, \( c \) is a positive number as well. Thus, it has been shown that the average conductance of STDP learning window with dendritic processed HRHT waveforms is a second-order approximation of the exponential learning function.

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