Bridging the Band Gap: What Device Physicists Need to Know About Machine Learning

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Abstract—This article surveys the landscape of semiconductor materials and devices research for the acceleration of machine learning (ML) algorithms. We observe a disconnect between the semiconductor and device physics and engineering communities, and the digital logic and computer hardware architecture communities. The article first provides an overview of the principles of computational complexity and fundamental physical limits to computing and their relation to physical systems. The article then provides an introduction to ML by presenting three key components of ML systems: representation, evaluation, and optimisation. The article then discusses and provides examples of the application of emerging technologies from the semiconductor and device physics domains as solutions to computational problems, alongside a brief overview of emerging materials and devices for computing applications. The article then reviews the landscape of ML accelerators, comparing fixed-function and reprogrammable digital logic with novel devices such as memristors, resistive memories, magnetic memories, and probabilistic bits. We observe broadly lower performance of ML accelerators based on novel devices and materials when compared to those based on digital complimentary metal-oxide-semiconductor (CMOS) technology, particularly in the MNIST optical character recognition task, a common ML benchmark, and also highlight the lack of a trend of progress in approaches based on novel materials and devices. Lastly, the article proposes figures of merit for meaningful evaluation and comparison of different ML implementations in the hope of fostering a dialogue between the materials science, device physics, digital logic, and computer architecture communities by providing a common frame of reference for their work.

I. INTRODUCTION

From the employment of graphical methods by ancient Babylonian astronomers to calculate Jupiter’s position in the sky [130], to the Antikythera mechanism, used by ancient Greek navigators to track the paths of celestial bodies [52], humans have been doing computations for millennia. Computers are now an integral part of daily life, with applications from healthcare to construction, transport to fitness, agriculture to science. In the tradition of naming historical periods after dominant materials in tools, some claim that we are living in the silicon age [24,157]. Silicon is the dominant material used in contemporary computing devices. The success of silicon and in particular, metal-oxide-semiconductor field-effect-transistors (MOSFETs), has been described and explained many times and in great detail, but to briefly summarise:

1) Stable Oxide Formation: Silicon forms a stable oxide layer which serves as a good semiconductor-insulator interface.
2) Abundance: Silicon is the second most abundant element in the earth’s crust, after oxygen, making up 28.2% of its mass [144].
3) Miniaturisation and Mass Production: MOSFETs are the first transistor which could be miniaturised and mass-produced [121].
4) Power Efficiency: Complimentary metal-oxide-semiconductor (CMOS) eliminates the always-on power draw of n- or pMOS by combining both into a single device which only consumes power when the device switches.

However, physical constraints and new application classes are demonstrating the limitations of conventional computing methods. The growing prevalence of machine learning (ML) and big data, alongside the diminishing returns and increasing difficulty of CMOS scaling has triggered a search for alternative and complimentary approaches to computation. ML training compute demands have doubled roughly every 3.4 months since 2012 [8], significantly faster than the roughly two year doubling time of integrated circuit transistor counts described by Moore’s Law [120]. Despite a large research focus, very few of these new technologies have seen adoption in mainstream computing systems. This article examines and addresses the varied reasons for this, with a focus on ML hardware.

A. Definitions

We provide the following definitions of common terms which will be used in this article.

1) Algorithm: a sequence of operations used to perform a computation, independent of implementation.
2) Computer Architecture: an abstract description of a computer, such as an instruction set architecture (ISA), which defines functionality but not the physical implementation. See Section [III] for a more thorough explanation.
3) Computer Device: an individual device used to represent data for computation, e.g., a transistor, or a resistive random-access memory (ReRAM).
4) Software: An implementation of an algorithm or algorithms generally intended to be executed on reprogrammable digital CMOS hardware (e.g., a microprocessor).
5) Neuromorphic System: a hardware device or circuit which mimics the behaviour of biological neural systems. See our discussion in Section [VI-A] for a more detailed exploration of the term.
6) Fixed-Function Digital Hardware: a device or circuit which processes data using digital logic in a fixed manner. For example, an H.264 decoder is an application-specific integrated circuit (ASIC) designed to decode video streams encoded in a common format.
7) Programmable Architectures: a piece of hardware that can be reprogrammed for arbitrary functionality, such as a microprocessor. Such a system reuses the same logic elements for different applications.
8) Hardware Microarchitecture: the physical specification of an ISA, defining ALUs, buses, registers, etc.
For continued development of computer technology, significant and meaningful advances in computation must be made on two main fronts: computational devices and computer architectures. However, the disconnect between the devices and computing communities may pose a greater hurdle to progress than technological challenges. Although it will be necessary to examine the state of the art in the research areas we discuss in this article, we do not intend this article to be a literature survey of existing technologies to arrive at a given implementation, in essence, a top-down approach, followed by device fabrication, and then integration of devices into a larger circuit. This results in a bottom-up approach, or, in practice, a solution looking for a problem. By examining the key considerations described by Norrie [124], we begin to see what considerations computer architects make when searching for a suitable solution. Norrie et al. divide tasks into two groups: those which need to be done well, and those which can be done to a working level. The first group, tasks which must be done well, consist of the following:

1) Build Quickly: Fast design and fabrication of hardware, e.g., using readily-available components and ‘good-enough’ designs;
2) Achieve High Performance: High-bandwidth buses and memory, systolic array structure for high computation density, use of the bfloat16 format, instruction-level parallelism;
3) Scale Efficiently: Ability to add multiple processors to cope with increasingly-complex problems and datasets;
4) Easily Adapt to New Workloads: bfloat16 is easy for ML software to use, chip developed alongside compiler team to ensure programmability, the terminology of linear algebra used due to its generality;
5) Cost Effective: The systolic array structure allows high density without demanding a large chip area, bfloat16 reduces hardware and energy costs, dual-core design, compiler-controlled memory hierarchy.

Considering novel devices as solutions to computational problems is a key motivation of this article and provides a way to judge the most effective application of novel materials and devices to acceleration of ML computations, thus facilitating their consideration by computer architects. Table I gives some examples of existing uses of hardware as solutions to computational problems, grouping devices as potential solutions to computational problems. For example, artificial neural network (ANN) inference as a computational problem is simply matrix-vector multiplication (MVM), with ReRAM crossbars being a potential solution.
II. COMPUTATIONAL COMPLEXITY, THERMODYNAMICS AND FUNDAMENTAL LIMITS

A. Computational Complexity

Every computer algorithm, from the simple addition of two numbers to the Fourier transform, requires a certain amount of time and resources to run. This complexity is an important consideration in any computing system as it has implications for the efficiency and scalability of an algorithm’s implementation. Complexity is generally evaluated in two main ways: time and space \[9, 60, 134].

- Time complexity is the number of steps for some target computational model that an algorithm takes to run and is implementation independent.
- Space complexity describes the memory cost of an algorithm. A given program requires temporary space during the execution of an algorithm (auxiliary space) and memory to store the input variable (input space). The total space complexity is the sum of these: Space Complexity = Auxiliary Space + Input Space.

B. Big-O Notation

Big-O notation is a way of describing algorithmic complexity as a function of input size according to the growth of time and space requirements. Formally, big-O notation describes the asymptotic upper bound of the function’s complexity to within a constant factor \[38\].

Determining the complexity of a function is relatively simple: one simply selects the fastest growing term, ignoring constant terms. For example, if a function \( f(x) \) is defined as \( f(x) = ax + b \), where \( a \) and \( b \) are constants and \( n \) is the input, \( a \) and \( b \) can be ignored as they become small compared to \( n \), when \( n \) tends towards infinity. The big-O complexity of the function is thus \( O(n) \). The addition of numbers is an example of an algorithm with complexity \( O(n) \). Now consider another function, \( g(x) \), defined as \( g(x) = an^2 + bn + c \). This is a simple quadratic equation. By inspection, it is clear that, as \( n \) tends to infinity, the \( n^2 \) term will grow larger more quickly than the \( n \) term and so the big-O complexity of this function will be \( O(n^2) \). Traditional ‘long multiplication’ has complexity \( O(n^2) \), however algorithms have been developed which reduce the time complexity of multiplication to \( O(n \log(n)) \) \[24\].

Though the actual time and resources required by an algorithm are dependent on the system running it, algorithmic complexity is always an important consideration. Consider two sorting algorithms: bubble sort, with average-case complexity \( O(n^2) \) and merge sort, with average-case complexity \( O(n \log(n)) \). If one wishes to sort an array containing a million numbers, using both algorithms, with the bubble sort running on a computer that can complete a hundred million operations per second and the merge sort running on a slower computer which can only complete one million operations per second, then the time taken for the bubble sort is:

\[
\frac{(10^6)^2}{10^8} = 10,000s,
\]

whereas the slower computer, using merge sort, takes:

\[
\frac{(10^6) \log(10^6)}{10^8} = 6s.
\]

Even though the first computer is a hundred times faster, it performs the same operation significantly slower. This illustrates the importance of algorithmic complexity in a computing system. A fast algorithm on a slow implementation will perform better than a slow algorithm on a fast implementation. This observation is important regardless of whether the one or both of the implementations of the algorithm are achieved using a programmable processor, fixed-function digital hardware such as a digital ASIC or analog domain computation. Figure 2 shows the time complexity growth of different big-O complexities with problem size.

C. Precision in Computing

In digital computing, the number of bits used to represent a number gives the precision of that number. Greater precision is
generally a desirable goal. Modern ML implementations in fixed-function hardware typically make use of the `bfloat16` format\cite{124}, as it allows for fast conversion to 32 bit floating point formats whilst reducing storage requirements and computation time for ML algorithms. The reduced size allows for a sufficient level of accuracy to be retained whilst reducing the input size. For a 7 nm process, Norrie et al. estimate a 1.5× reduction in energy consumption for the `bfloat16` format compared to a conventional IEEE 16-bit float format.

However, more bits cost time, resources and energy. These constraints have led to a renewed interest in computation, which, in theory, can offer infinite precision, as one does computation using continuous rather than discrete signals. In Section V we discuss how analog approaches can offer significant savings in terms of resources and energy requirements.

To readout or otherwise interact with the data one is computing involves measuring a signal. Thus we see that a truly analog computation is not possible, as measurement is a discrete process; an truly analog signal would require infinite precision. Analog systems are more sensitive to noise and offset than digital systems. As digital circuits rely on some discrete, reference state, the continuous nature of analog circuits means these cannot exist in analog systems\cite{151}. As computations become increasingly complex, the associated noise accumulation becomes a dominant and limiting factor in the precision. Compensating circuitry can of course be added to attenuate the noise, however this adds additional resources and energy costs to the system which may eventually eliminate any advantages in energy and space efficiency afforded by an analog system.

D. Physical Limits of Computation

As well as mathematical constraints on computation, there also exist physical limits. Computation is ultimately a physical action and so obeys the laws of physics. One obvious limit is the speed of light and the resulting impossibility of faster-than-light communication. An exception that may be raised here is quantum entanglement, which may eventually eliminate any advantages in energy and space requirements.

| Temperature (°C) | Energy (zJ) |
|-----------------|-------------|
| 24              | 24          |
| 25              | 25          |
| 26              | 26          |
| 27              | 27          |
| 28              | 28          |
| 29              | 29          |
| 30              | 30          |
| 31              | 31          |
| 32              | 32          |

Fig. 3. A plot of the classical Landauer limit as a function of temperature.

1) The Classical Landauer Limit: The Landauer limit asserts that there is a minimum energy requirement, $E_0$, for erasing a single bit of information\cite{100}. This is given by

$$E_0 = k_B T \ln(2), \quad (1)$$

where $k_B$ is Boltzmann’s constant and $T$ is the temperature. Assuming room temperature operation ($T = 293$ K), the minimum energy required to erase a single bit of information is $0.0175$ eV or $2.8 \times 10^{-21}$ J. Figure 3 shows the Landauer limit as a plot of energy against temperature. Berut et al. experimentally verified the classical Landauer limit in 2012\cite{15} and Yan et al. demonstrated a quantum Landauer limit in 2018\cite{183}.

Here, $\Delta$ is a factor, $p_0(M)$, which gives the density of the discrete probability distribution, $p(x)$, that represents the spin degree(s) of freedom, i.e., the minimum quantum of the configuration volume of a physical system. $S$ is the Shannon entropy, $k_B$ is the Boltzmann constant, $\hbar$ is Planck’s constant, and $s_{\text{class}}$ is the electron spin in the classical limit of the quantum Heisenberg model. $N_L$ is the integer (int) number of spins, given by:

$$N_L = \text{int} \left( \frac{8\pi L}{\hbar} \right), \quad (3)$$

where $L$ is the angular momentum of the system. This allows for the number of bits, $n$, which characterise the system, to be determined from $n = \log_2(N_L)$. For the Heisenberg model, one can assume that $s_{\text{class}} = 1$, which reduces the expression to $\ln(\frac{2\pi}{\hbar})$.

Landauer derived the original limit in the nascent days of statistical thermodynamics, applying it only to equilibrium, non-reversible digital systems, i.e., a Boolean logic gate. For conventional computing, this makes it a useful guideline. More recent work on the link between logical and thermodynamic reversibility has shown that the thermodynamically reversible erasure of a bit is not forbidden by the laws of physics\cite{146}, however irreversibility may be an inherent aspect of a computation.

E. Case Study: Optical Neural Networks Below the Landauer Limit

We have seen that there exists a fundamental, thermodynamic limit on information processing, namely the erasure of a single bit. Hamerly et al.\cite{66} detailed an optical neural network which, theoretically, had a lower bound on a single multiply-accumulate (MAC) operation below the classical Landauer limit.
The authors describe the scenario of a MAC operation using 32-bit numbers. This would require on the order of $10^7$ binary logic gates, which are subject to the original Landauer limit as they are digital and irreversible. This has a corresponding lower bound energy per MAC operation ($E_{MAC}$) of $E_{MAC} \geq 3 \text{ J}$. In contrast, they claim a theoretical lower bound of $50 \text{ zJ/MAC}$ for their method, limited by shot noise in their photodetectors, with a range of $50 \text{ zJ/MAC}$ to $5 \text{ aJ/MAC}$. The authors note the consideration of the electrical energy required to generate weights for the network, estimating a minimum of $1 \text{ fJ/MAC}$, but also state that existing technology should permit sub-fJ/MAC operation.

How then does the authors’ system bypass this limit? The first way is the nature of the processing. It is analog and so will be subject to a different limit than the classical limit. Using Equation (8), we can estimate an analog limit. Continuing with the $n = 32$ bit example, $N_L = 2^{32}$. The authors use a detector with one million pixels (i.e., a $1000 \times 1000$ pixel sensor), where each pixel is $20 \mu \text{m} \times 20 \mu \text{m}$, but confine the active area to a $5 \mu \text{m} \times 5 \mu \text{m}$ space. Analog signals become discretised at the point of measurement and so we will consider the detector as the computing medium here. Let us assume the thickness of each pixel is $100 \text{ nm}$ and that the average diameter of each atom is $0.3 \text{ Å}$. $\Delta$ is in terms of atoms and so each dimension of the pixel is divided by the atom diameter to gain the value in terms of atoms. To calculate the energy, we rearrange Equation (8) and multiply by temperature, $T$:

$$E = TS = \frac{k_B N T}{\Delta} \ln \left( \frac{8\pi \sigma_{\text{class}}}{h} \right).$$

Assuming room temperature operation, the per-pixel energy requirement ($E$) of about $6 \times 10^{-25} \text{ J}$ and a total of $6 \times 10^{-25} \text{ J}$ for all one million pixels, which falls within the ballpark of the authors’ claims. We have made a number of assumptions based on the available information so our calculations likely deviate from the true numbers. For comparison, Yan et al. give a quantum Landauer limit of $1.7 \times 10^{-25} \text{ J}$ at $48.5 \mu \text{K}$ and so Hamerly et al.’s lower bound does not appear to violate any of these limits.

The other aspect of Hamerly et al.’s work that exempts it from the classical Landauer limit is the fundamental operation is reversible. The dot product computation is computed by the homodyne detector using a polarisation identity which uses optical interference, a reversible process, to convert the signals representing the vectors into the correct form. Here then we have a good example of how, by harnessing specific properties of a material or medium, one can make significant improvements in computational speed and efficiency.

**F. Case Study: Memcomputing**

Complexity is an essential consideration when it comes to computing approaches, but it is often overlooked by the devices community. A good example of this is the paradigm of memcomputing. Amongst the devices community, it appears to be an elegant and promising solution to the von Neumann bottleneck, which is framed as a problem of moving data. The underlying premise is that, rather than moving data between a processor and a memory element, the processing and memory elements are combined into a single unit and so processing is done in-memory [45].

This begs the question: why has the paradigm been met with such a lukewarm reception by computer architectures researchers? One claim in particular, that it is possible to efficiently solve $NP$-complete problems in polynomial time using memcomputing [168], has, understandably, led to doubt by the architectures community. This is, in practise, a claim to answer one of the major unsolved problems in computer science, the $P$ vs $NP$ problem [37]. A simple formulation of the problem is as follows: can a problem whose solution can be verified quickly also be solved quickly? In other words, can a problem whose solution can be verified in polynomial time also be (efficiently) solved in polynomial time? The general consensus amongst the architectures community is the $P \neq NP$, whereas the claim of memcomputing implies that $P = NP$. Such a discovery would have a significant impact across a multitude of fields.

Traversa et al. [168] present a memprocessor consisting of four fundamental computing elements: a differentiator, four voltage multipliers, a summing amplifier and a difference amplifier. The memprocessor encodes information in the frequencies of the collective state of signals in the machine, i.e., the measured signal is the sum of the encoding frequencies. The system does readout by taking the Fourier transform of the signal. For a demonstration of an $NP$-hard problem, they use a version of the Subset-sum problem. The full subset-sum problem asks the following question: for a set of $N$ integers, $k$, is there a subset, $s$ which sums to a particular number, $P$? A common formulation of this has $P$ as zero and $s$ as a non-empty subset, i.e., if $k = \{-2, 4, -7, 9, 10\}$, then we can see that there exists a subset $s = \{-2, -7, 9\}$ which will sum to zero. As the power set, i.e., the set of all subsets contains $2^N$ subsets, then it is clear that the problem size grows exponentially with the input size. Indeed, algorithms to solve this problem have exponential time complexity, with the naive solution having complexity $O(2^N)$ and better approaches having complexity $O(2^N \frac{1}{N})$.

Traversa et al. generate waves at frequencies that encode all possible subsets of $k$ and measure the output signal to see if a frequency corresponding to $P$ exists. As the number of subsets grows exponentially with input size, then, despite anything else, exponentially many frequencies will be required to encode all possible subsets. This measurement therefore will therefore take an exponential amount of time. If each measurement takes the same amount of time, an exponentially increasing number of measurements will take exponentially increasing time.

The authors also remark that “all frequencies involved in the collective state... are dampened by the factor $2^{-N\omega}$, in order to place a bound on the energy consumption of the system. This also presents a fundamental limit of the scalability of the system, beyond the obvious issue of exponential growth when taking into account the Landauer limit. From the authors’ work, we see that energy is related to the fundamental frequency, $f_0$ by $E \leq \frac{1}{f_0}$, i.e., the energy for a computation is proportional to the energy in the collective state in a single period. Frequency is related to wavelength $\lambda$ by the well-known relation $f = \frac{c_0}{\lambda}$, where $c_0$ is the speed of light. We can establish the smallest fundamental frequency by setting the Planck length as the shortest possible wavelength. From this, we can get the following expression for the maximum energy of the collected state (the sum of frequencies):

$$E \leq \frac{\lambda}{c_0}.$$ 

As we know that the attenuation is by a factor of $2^{-N}$, we have an expression for the maximum energy of the collected state $E$ and a thermodynamic limit on the energy for processing a bit of information, $E_0$, we can combine these into an expression to find the maximum input size:
\[ 2^{-N} E \geq E_0. \]

Rearranging for \( N \):

\[ N \leq \log_2 \left( \frac{\lambda}{c_0 E_0} \right). \]

From this, we can finally establish a maximum value of \( N \) based on fundamental physical constants, which turns out to be about \( N \leq 76 \). Again, this is proportional to the energy in the collective state.

This does not dismiss the work on memcomputing, because the authors do indeed demonstrate a speedup and improvement over existing methods for the problem, verifying this in more recent simulations [140], albeit for approximations rather than true solutions. The issue is the exponential factor. Though the memprocessor solves a particular problem in a reasonable time, higher calculation precision requires exponentially greater measurement precision, meaning there is a trade-off between these, and scalability becomes a limiting factor.

**G. The Unavoidability of Computational Complexity**

We have seen that memcomputing is still subject to the same constraints of computational complexity as any other architecture. Are there other architectures that might escape this, such as quantum computing, which can try every solution to a problem at once? The answer, unfortunately, is no. Despite their speed and special properties, quantum computers are still subject to the same constraints of computational complexity. On a basic level, this is because quantum mechanics can, to the best of our understanding, describe all physical phenomena. This means that any problem solvable by a classical computer can also be solved by a quantum computer and vice-versa.

Aaronson [4] addresses the issue of exponentially growing resources, evaluates various proposals for solving NP-complete problems in polynomial time under known physics, and suggests that efficient solutions to NP-complete problems are unlikely and that such attempts are akin to attempts at constructing perpetual motion machines. This is a powerful guiding principle in development of computing devices, as, like the various forms of the Landauer principle, it helps place constraints on possible devices and computations.

The scalability consideration also suggests a limit of what researchers in the field should concern themselves with; a solution to the \( P \) vs \( NP \) problem is the domain of theoretical computer science and mathematics. Attempting a proof via demonstration is akin to demonstrating infinity by writing out all its digits.

One final point worth reiterating is the nature of exponential growth. A common argument is that smaller devices and increased integration density will offset the problems of exponential growth in the number of devices required by an approach, yet this does not hold up to scrutiny. Consider some hypothetical computing device of dimensions \( 1 \times 1 \times 1 \) nm that can perform any desirable computation on a single bit of information. Say an arbitrary number of these are integrated together into an array on a single die. Now say we wish to implement an algorithm of circuit complexity \( O(2^N) \) in hardware on this system. If we start with some operation involving two 4-bit numbers, then the system would require \( 2^4 = 16 \) devices to function, giving a total lateral area of \( 16 \) nm\(^2\). If we then jump to a typical binary, single-bit floating point representation, i.e., 32-bits, this requires \( 2^{32} = 4,294,967,296 \) devices, giving a lateral area of about \( 4 \times 10^5 \) nm\(^2\) for two numbers. If we wished to use such a system for a cryptographic computation, using a standard 128-bit encryption, this would require \( 3.4 \times 10^{38} \) devices, corresponding to a lateral area of \( 3.4 \times 10^{29} \) m\(^2\). For comparison, the average surface area of the sun is about \( 6.1 \times 10^{18} \) m\(^2\). Even if these devices were integrated in three dimensions, the total volume would be at least \( 3.4 \times 10^{11} \) m\(^3\), which is about a third of the volume of Mars’ moon, Deimos (volume \( \approx 10^{10} \)).

**III. A QUESTION OF ARCHITECTURES**

In its simplest definition, an algorithm is a sequence of operations to perform a computation or calculation, independent of implementation. A computer program is an implementation of an algorithm. Likewise, a hardware accelerator, such as a ReRAM crossbar for matrix-vector multiplication (MVM), is also an implementation of an algorithm.

Architectures is also a nuanced term. In computing, there are two main things which the word architecture refers to. The first is an instruction set architecture (ISA), which is the abstract model of a computer and is what the term computer architecture is typically used to refer to. An ISA describes the data types, registers, I/O model and fundamental features of a computer. The two main classes of ISA are Complex and Reduced Instruction Set Computer (CISC and RISC) architectures. The Intel x86 family is an example of a CISC architecture and the ARM family is an example of a RISC architecture.

Like an algorithm, an ISA can be implemented in different ways. For example, though AMD and Intel might both build CPUs with an x86 ISA, the physical implementations will be very different. This is an example of the other use of the term architecture that commonly arises in discussions of computer systems, referring here to a microarchitecture, which is the set of processor design techniques used in a given piece of hardware, i.e., the hardware layout.

Most modern computers are based on either the von Neumann architecture (also known as the Princeton architecture, Figure 4) of the Harvard architecture (Figure 5). The former was developed by von Neumann in 1944 [172], itself inspired by the universal computing machine described by Turing in 1936 [170].

![Fig. 4. Schematic of a von Neumann computer.](image)

However, the von Neumann architecture has a fundamental design limitation which hinders performance, the von Neumann bottleneck, which arises from the shared bus used by the program and data memory. This limits the throughput between the CPU and the memory, as only program or data memory can be accessed at a given time and so the CPU must wait for data to be moved to and from memory to process it. No matter how much CPU speed and memory size increase, the limited throughput means that there will always be a significant restriction on data processing rates.

The Harvard architecture does not use a shared memory and program bus and so is not subject to the associated bottleneck. Though this avoids the von Neumann bottleneck, it also means that the data and
program memory in a Harvard computer occupy different address spaces. Here, a memory address does not identify a storage location and so the memory space that the address belongs to, whether data or program, must also be known. This gives von Neumann computers an advantage in the sense that data and program memory can be treated in the same way. For example, data can be read and then executed as code, whereas a Harvard machine requires additional processing.

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Fig. 5. Schematic of the Harvard architecture.
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The Harvard architecture is commonly used in digital signal processors [165] as well as a number of microprocessors including the ARM Cortex M3 [156] and PIC microcontrollers [179]. Many modern general computers use a modified Harvard architecture, which is similar to the von Neumann architecture in that there are separate CPU caches for data and instructions which share a single address space. This is the split-cache architecture of most modern CPUs.

An architecture can have multiple implementations. Many research articles which propose and demonstrate novel devices make reference in some form to the limitations of contemporary computer architectures, before going on to describe the implementation of a particular algorithm, e.g., a MVM accelerator/dot-product engine using a novel device. This comparison of an abstract computer architecture to an algorithm implementation is thus meaningless. Consider again the von Neumann architecture. One of the components of this is the ALU. This is a digital circuit which performs arithmetic and bitwise operations on integer binary numbers, i.e., a circuit which implements algorithms (binary addition, multiplication, division etc.). Likewise, a circuit which implements a MVM operation is simply that. It is not a computer architecture in and of itself, but may be used in the hardware microarchitecture.

IV. BRIEF OVERVIEW OF MACHINE LEARNING

Machine learning is a field which has, in recent years, become simultaneously a technological revolution, a household term, a source of moral and philosophical consternation, and a scientific endeavour. Despite its long history, with the term machine learning being coined in 1959 [47], it is only relatively recently that ML has entered mainstream awareness. ML has quickly become a dominant technology, seeing applications in almost all areas of computing, from computer vision [2] to medicine [3] and law [163].

At a fundamental level, ML is where a program is able to make predictions from a pre-existing dataset. In strictly mathematical terms, a dataset with one or more features (variables) has an associated output. ML is the attempt to discover the mathematical function that depends on these features and most accurately predicts the output, though ML is a broad term which encompasses a wide range of approaches and models. Domingos [47], suggests that all learning algorithms have three principal components: representation, evaluation, and optimisation. Commonly-used terms, such as “machine learning techniques” typically refer to a given representation, e.g., neural networks, independent of the evaluation function or optimisation methods.

A. Representation

Domingos [47] gives six classes of representation for machine learning methods: instances (K-nearest neighbour, support vector machines), Hyperplanes (naïve Bayes, logistic regression), Decision Trees, Sets of Rules (Propositional rules, logic programs), Neural Networks and Graphical Models (Bayesian networks, conditional random fields).

1) Neural Networks: ANNs are the most ubiquitous ML approach and are modelled on biological neurons. The simplest types of neural network are a type of feedforward neural network known as single-layer perceptrons. These consist of an input layer and a single output neuron, corresponding to a binary output. More complicated ANNs will have one or more hidden layers and an output layer. During training, each input will fire and activate a neuron in the next layer and different inputs will fire with different intensities (weights). Figure 6 (a) illustrates a simple ANN with a set of inputs \( (x_1, x_2, x_3, \ldots, x_j) \) and corresponding weights \( (w_1, w_2, w_3, \ldots, w_j) \), a transfer function \( \sum \), an activation function \( \Phi \) and a threshold \( \theta \).

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Fig. 6. (a) Schematic of a simple single-layer perceptron ANN; (b) Schematic of a simple, single-layer spiking neural network
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The error is calculated using a cost function such that \( E = L(t, y) \). A commonly-used function is the squared error, \( (t - y)^2 \), where \( t \) is the true value and \( y = \sum w_i x_i \). In each training cycle, the weights of the connections between neurons in each layer are adjusted until the weights giving the most accurate classification of the test sets are determined. Optimal weights are found by making use of the cost function, which measures the discrepancy between the neural network’s classification and the actual result. This
updated by weights is the most vital aspect of training and is known as **backpropagation**.

Feedforward networks can be extended beyond the simple single-layer perceptron example, and most state-of-the-art feedforward networks involve multiple layers between the input and output. Hence, they are described as **deep** neural networks (DNNs). Depending on the application, different varieties of DNN are used. Recurrent neural networks (RNNs) are common for applications with sequential data, such as speech recognition, whereas convolutional neural networks (CNNs) are the predominant approach for tasks such as computer vision, natural language processing and image classification.

Spiking neural networks (SNNs) differ from feedforward networks in that each neuron only fires once a specific threshold value is reached, thus SNNs more closely resemble biological NNs than feedforward networks. Figure 3(b) The threshold for a neuron firing is commonly referred to as the **membrane potential**, after the property in biological cells. These have an inbuilt time dependence, with input taking the form of a spike train rather than an instantaneous value. This means that, in a given epoch (training cycle), not all neurons will activate, and that a given neuron requires a certain time to activate, i.e., when a sufficient number of spikes have been input within a given time.

2) **Instances:** k-nearest neighbours (k-NN) is a method used for both classification and regression. In the former case, the algorithm output is the class to which the object being tested belongs to. In the latter, the output is the property value of the object of interest. A k-NN algorithm classifies an object by measuring the distance between a datapoint of interest and neighbouring datapoints with the final classification of the datapoint determined by the class of the k nearest neighbours, where k is a small, positive integer value.

Support Vector Machines (SVMs) are ML models which are used to find and construct hyperplanes. A hyperplane is defined geometrically as a space with one less dimension than the ambient space. For example, a hyperplane would be a 2D plane in 3D space. In the case of ML, these act as boundaries between classes of datapoints. Datapoints that fall on one side of a boundary can therefore be considered as belonging to one class, whereas those that fall on another side belong to a different class. A support vector is a datapoint which is close to the hyperplane and helps influence the hyperplane’s position and direction. These support vectors can be used to find the margin of a classifier, which is the distance from a datapoint to a decision boundary. Ideally, this will be large.

3) **Hyperplanes:** For SVMs to be able to draw the boundaries between classes of data, algorithms which classify the data to begin with are needed. Naïve Bayes methods, such as Gaussian or Multinomial Naïve Bayes classifiers, are an example of these. Naïve Bayes refers to a family of classifiers which use Bayes theorem, given as follows:

\[
P(B|E) = \frac{P(E|B)P(B)}{P(E)}. \tag{4}
\]

Here, **B** and **E** are two independent random variables. For the example here, **B** is a belief and **E** is a piece of evidence. Bayes’ theorem states that the probability a belief is true, given a new piece of evidence, is equal to the probability that evidence is true given that the belief is true, multiplied by the probability that the belief is true, regardless of the new evidence, all divided by the probability that the evidence is true regardless of whether the belief is true. Naïve Bayes algorithms are so-called because they assume a strong independence between features in a dataset.

4) **Decision Trees:** Decision tree (DT) learning is a predictive model approach which uses decision trees to draw conclusions about the value of some item, based on observations about the item. A DT represents observations the branches of the DT and the conclusions in the leaves. DTs where the variables have discrete values are known as classification trees, whereas those where the variables are continuous are known as regression trees.

5) **Graphical Models:** Bayesian inference is another approach based on Bayes’ theorem. Bayesian networks can be considered probabilistic computers, as they compute probabilities as opposed to specific numbers or values.

Conditional Random Fields (CRFs) are a method which differ from classifiers such as Naïve Bayes or k-NN in that CRFs consider context, whereas the others do not. Random fields themselves are a function that takes on a random value at a given point in the input space, which is often multi-dimensional. A given CRF models the conditional probability distribution of a graph whose nodes form two disjoint sets, one of the observed variables and one of the output variables.

### B. The Curse of Dimensionality

Real-world datasets are often very large, with many variables, which gives rise to the ‘curse of dimensionality’, coined by Bellman in 1961 [12]. This refers to the phenomena arising from analysis and organisation of high-dimensional datasets, namely the tendency for algorithms working well in lower dimensions to become far more complex as the dimensionality increases. For ML, this is a significant issue, as data becomes sparser and meaningful groupings or methods that rely on statistical significance break down, something which Domingos [42] addresses.

C. **Machine Learning Benchmarks**

With a range of ML approaches being actively researched, it is vital that some common frame of reference or benchmark exists which allows for different methods to be evaluated against one another in a meaningful way. Here we present a brief overview of some popular ones.

1) **MNIST:** The most common benchmark, which serves as the ML analogue of “Hello World” in traditional computer programming, is the MNIST dataset. This is an optical character recognition (OCR) task using a database consisting of 60,000 training examples and 10,000 test examples of handwritten digits, where each example is a 28×28 pixel greyscale image. The current top five verified algorithms for MNIST have accuracies of around 99.79 % or greater [143], whereas accuracies closer to 90 % are often reported for experimental devices such as P-bits [131] or ReRAMs [71]. Such accuracies are significantly lower than those of MNIST software approaches from as far back as 1998 [102].

2) **UCI Databases:** Another popular and comprehensive suite of benchmarks are the 559 (at the time of writing) datasets provided by researchers at the University of California, Irvine [48]. These datasets cover a broad range of fields and data types (e.g., text, images, numerical), from healthcare (e.g., arrhythmia, lung cancer, thyroid disease), botany (types of iris plant, types of soybean), finance (credit approval, stock exchanges), and many others. As ML algorithms are typically tailored to the data from which one wishes to learn, these datasets offer an excellent resource for researchers wishing to test their algorithms.

3) **ImageNet:** ImageNet is another popular benchmark, consisting of over 14 million images and focuses on image classification [43]. Unlike MNIST, which covers just handwritten characters, ImageNet includes datasets of fungi, flora, fauna, geological formations, people, and miscellaneous objects such as food items.
V. Novel Devices as Alternatives to Digital Silicon Electronics

A. Limitations of Digital CMOS

The key driver in increasing computer performance over the past several decades is the miniaturisation of computing devices. Moore’s law, which described the apparent doubling in the transistor count of integrated circuits (ICs) every eighteen months [120], became a guiding principle in the development of semiconductor roadmaps. Another law which guided the development of semiconductor devices, and CPUs in particular, for around thirty years is Dennard scaling [44]. Dennard et al.’s article describes scaling relationships in MOSFETs, providing a framework within which device designers can scale various parameters to improve device performance. The key result of the article is constant field scaling, which describes the relationship between the supply voltage \((V_{dd})\) and dynamic switching power \((P_{dyn})\) via the relation \(P_{dyn} \propto CV_{dd}^2\), where \(C\) is the gate capacitance.

In 2006, the Dennard scaling era drew to a close and the clock speeds of CPU cores began to saturate as limits of power density were reached. This led to the introduction of multi-core CPUs, in which parallel processing threads are used. This tendency towards parallelisation has helped maintain Moore’s law for CPUs by increasing the number or processing cores on a single CPU die, as opposed to simply increasing the number of transistors in a single processing core. Figure 7 illustrates these scaling laws over time, based on data we collected of both commercial and research devices [171]. Figure 7(c) shows the growth in time of CPU clock speeds and (a) shows the number of CPU cores as a function of time. The causes of this are primarily material; in the case of Dennard scaling, CMOS dynamic (i.e., switching) power consumption is proportional to the frequency and so reducing the size of transistors allows for faster switching. However, as devices reach a certain scale, typically below 45 nm, it is no longer the switching which is the main source of power consumption, but leakage current [59]. Figure 7(b) shows the slowing of Moore’s law since around 2010.

Keyes [86] highlights the successes of CMOS and outlines the general features that a digital computing device must have. These are:

1) Gain: High gain in each component reduces issues arising from inter-device variation. As environmental and manufacturing variations can influence device performance, signal degradation is prevented by using reference signal levels throughout a system. Signal levels are restored to this reference at each step.

2) Input/Output Isolation: Inputs and outputs must be isolated from one-another to ensure calculations are carried out in a predetermined manner. This means the output of a device must have no impact on the input, otherwise the state of the inputs may change and influence the output in an uncontrolled manner.

3) Comparable On/Off Switching Times: The switching time between on and off states must be comparable. If this is not the case, a separate reset operation is needed, adding both time and material costs.

4) Inversion: A computer device must be able to convert a one to a zero and vice-versa.

We have focused so far on CPUs, however Moore’s Law and Dennard Scaling also apply to other technologies, including reprogrammable hardware such as field-programmable gate arrays (FPGAs), and memory such as DRAM, SRAM and Flash. The two main forms of volatile memory are SRAM and DRAM, whereas Flash memory is non-volatile. An SRAM cell typically consists of six transistors, and is typically used for the cache on a CPU, meaning it has generally scaled with CPU process nodes. However, DRAM, which requires a capacitor and a transistor, and is typically used on separate chips (e.g., the main memory in a computer). DRAM is slower but cheaper than SRAM, however has further scaling is becoming increasingly difficult, owing to the difficulties in scaling down capacitors [138]. As we discuss in Section VI, researchers have demonstrated ML accelerators using both DRAM and SRAM. Flash memory, which consists of a floating gate transistor, has successfully experienced 3D integration [156], however the read/write times for it are slow, making them unsuitable for use as anything other than storage devices, as per Keyes’ criteria, as well as the requirement for block-by-block erasure, as opposed to specific updating of individual bits. However, there has been some recent work in this area [95] [105], and novel approaches may render this a feasible method.

Traditional semiconductor roadmaps predominantly rely on the continuation of scaling laws, and thus a key focus of devices and materials research is focused on replacements to conventional silicon and digital CMOS. However, many novel technologies fail to compete with digital CMOS on matters of energy, speed, scalability and price, but this does not make them non-starters for computing applications! Sarapeshkar [151] highlights the stark difference between computational approaches, discussing the addition of two, parallel eight bit numbers which, in the analogue domain requires only a single wire, using Kirchoff’s current law. However, in the digital domain, around 240 transistors are required for a CMOS circuit. In the case of multiplication, between four and eight transistors are required for an analogue approach, whereas digital computation demands as many as 3000 transistors. It is clear that fundamentally different approaches and devices have the potential to offer significant improvements in the efficiency and resource requirements of certain computations. In practise, this is likely to mean technologies complementary to the CPU plus memory architecture of conventional computers.
B. Case Study: Generating Non-Uniform Random Variates with GFETs

Keyes’ observations about what constitutes a good computer device would suggest that some experimental devices are inherently unsuitable for computation. One such device is the graphene field-effect transistor (GFET). First reported in 2007, by Lemme et al. in 2007 [106], graphene FETs (GFETs) have a channel made of single- or multi-layer graphene, rather than a semiconducting material such as silicon or germanium. Due to their high mobilities [27] and fast switching speeds [123], GFETs attracted significant interest from researchers. However, the lack of a band gap which gives rise to these properties also means that GFETs have low on- to off-current ratios, making them unsuitable for digital logic applications [86].

However, this does not preclude the use of GFETs for alternative computing applications. Our own work provides an example of this [172], Figure 5 provides an illustrated overview of the process. As a computational problem, we investigate sampling from non-uniform random variates. This is a computational problem which arises in ML applications such as Bayesian inference, which requires the computation of marginal probabilities. This involves integrating a many-dimensional probability distribution, which rarely has an analytic form. Sampling from the distribution is therefore necessary. Typically, this sampling is done using Markov Chain Monte Carlo (MCMC) methods, based on the Metropolis-Hastings algorithm [68] or approaches which build on it [64] [112]. Other methods include Gibbs sampling [58] and the Hamiltonian Hybrid Monte Carlo method [49]. These algorithms are computationally inefficient and expensive, meaning there is significant scope for improvement.

Generally, algorithms for sampling non-uniform random variates are implemented using reprogrammable digital hardware, i.e., a programming language running on a CPU. In our approach, we use an array of selectively-biased GFETs to approximate a lognormal probability distribution, and predict a $\approx 2 \times$ speedup compared to MATLAB, with the sample rate limited by the speed of the analog-to-digital converter (ADC). Although our initial approach produced less accurate samples than MATLAB, we demonstrate comparable levels of accuracy to MATLAB non-uniform random number generation using as few as 16 GFETs, as well as application to arbitrary probability distributions in subsequent simulations (yet to be published), by using GFET transfer characteristics as orthonormal basis functions. Being significantly faster and requiring far fewer devices than an all-digital approach, we see how, by mapping a computational problem to novel devices and materials, one can provide significant improvements over existing approaches. External circuitry is required, e.g., to calculate bias voltages, as well as ADCs to read the generated sample, however biases only need to be determined once for a given approximation. Furthermore, we also demonstrate a robustness to inter-device variation, meaning the requirement for so few devices also means that the challenge of scalability, i.e., being able to produce consistent devices at scale, becomes a non-issue.

C. Experimental Devices

1) Non-Silicon Transistors: Silicon, germanium, and III-V compounds such as GaAs, InGaAs are the dominant materials used in commercial transistors, however there is a large research focus into the use of alternative materials as transistors. Carbon nanotubes (CNTs), which, depending on how they are rolled, can be semiconducting or metallic are one such material, and have been the subject of an intensive research effort as FETs [141], as well as having demonstrated application in ML hardware [91].

The discovery of the electric field effect in graphene triggered an interest in atomically-thin materials, due to their inherent suppression of short-channel effects as a result of their thickness. In addition, their scalability, unique properties and potential for new phenomena arising from selective stacking of materials have also made their study attractive to device researchers. FETs have been demonstrated using a range of 2D materials, including 2D semiconductors such as MoS$_2$ [150] and WS$_2$ [41].

Ferroelectric FETs (FeFETs) consist of a ferroelectric material such as BaTiO$_3$ placed between the gate electrode and the source-drain section of the device. MOSFETs are subject to a fundamental limit to the supply voltage, and thus power consumption required to switch at a given temperature, known as the Boltzmann Tyranny [7]. This related to the steepness of the subthreshold region of a device’s IV characteristics and is capped at around 60mV/decade at room temperature. A key attraction of these devices is their subthreshold swing which can be below the 60mV/decade limit [189].

2) Nonvolatile Memories: Motivated by the problem of the von Neumann Bottleneck, a significant amount of devices research explores the use of novel memory technologies for in-memory computation, in effect, attempting to solve a computer architectures problem using novel devices. However, such novel devices often end up being viewed as less-competitive alternatives to existing (digital CMOS) memory technologies. As we describe in Figure 1, mapping computational problems to these devices has the potential for a greater research impact.

The majority of novel memory devices fall under the umbrella of a class of memory called non-volatile (random access) memory (NVM), i.e., (random access) memories which retain their state in the absence of a power supply. Table II shows a comparison of the performance of different novel memory technologies. To this end, we provide a brief overview of novel memory technologies. Chen published a comprehensive review in 2016 [25].

| Memory Technology | Switching Speed | Cycle Endurance | Write Voltage |
|-------------------|-----------------|-----------------|---------------|
| STTMRAM           | $< 10$ ns       | $> 10^{12}$     | $< 1$ V       |
| ReRAM             | $> 20$ ns       | $10^{-1} 10^{9}$ | -0.5-5 V      |
| PCM               | $< 100$ ns      | $> 10^9$        | $< 3$ V       |
| FeRAM             | $> 20$ ns       | $10^{-2} 10^9$  | $\approx 5$ V |

Among the most widely explored technologies for next-generation computing are ReRAMs. This expression is often used interchangeably with the term memristor, however memristors often refer to a specific type of device. First theorised by Leon Chua in 1971 [32], the memristor was predicted to be a missing circuit element which relates electrical charge and magnetic flux linkage. Since the first experimental realisation in 2008 [162], memristors have regularly been touted as a revolutionary device for novel forms of computing and have been the subject of intensive research. Chua updated the definition of a memristor in 2014 to include any device with a pinched hysteresis loop [33] (Figure 9). In this article, we use ReRAM as the general term, and memristor for specific examples.

Resistive switching mechanisms in ReRAMs are broadly divided into body-effect and interface-effects [65]. Body-effect switching involves a change in the active layer due to different biases, such as the formation of conductive metal filaments (CFs) in the oxide or insulating layer, charge trapping, charge transfer and changes in
Fig. 8. Overview of the development process for the GFET-based non-uniform random variate generator in [172], showing the combination of materials and device selection as well as a mapping of a computational problem to an experimental device.

Fig. 9. Example of the pinched hysteresis loop which Chua defines as the characteristic property of a memristor [33].

the carrier concentration. Conductive Bridge RAM (CBRAM) is a common example, with CF formation and rupturing being the source of the high and low resistance states (HRS & LRS). CBRAM generally requires an initial electroforming process, in which a large voltage is applied to induce a breakdown in the oxide layer that allows for the subsequent formation of CFs. The voltage required to set and reset following this step is typically much lower. However, these CFs are a large source of inter-device variation, as the path and number of filaments that form in a device is difficult, if not impossible, to control. Body-effect ReRAMs also incorporate valence change RAM (VCRAM), where switching is the result of a valence change in the oxide layer, due to oxygen atom migration, leading to conductive path formation and dissipation. Switching in interface-effect ReRAMs is derived from effects at the interface of the active layer and the electrodes, such as Schottky barrier formation, a change in the profile of the potential barrier at the interface or a phase transition at the interface [65]. The active layers in such devices typically consist of transition-metal oxides such as HfO2 [167]. A key advantage of many of these devices is their compatibility with the CMOS process, however non-CMOS devices, such as those based on polymers also exist [28].

Phase-change memories (PCMs) are a form of NVM which rely on the phase transition of a given material or materials to change the electronic properties, typically as a result of Joule heating due to an applied current [54]. Generally, this involves a transition between a crystalline and an amorphous phase, with the former generally representing a low resistance state and the latter a high resistance state [25].

Magnetic or magnetoresistive random-access memories (MRAMs) are a form of NVM in which data is stored in magnetic domains; they use electron spin, rather than charge, to store data. The most common form of this is the magnetic tunnel junction (MTJ), a mature technology which is used most widely in computer hard drive read heads [191]. Traditional MTJs consist of two magnetic layers separated by a non-magnetic or insulating material. The state of the devices is read by measuring their electrical resistance: when the two magnetic layers are magnetised in the same direction, the tunnel current between them is greater and so they are considered to be in a low resistance state. When they are magnetised in opposite directions, the tunnel current is much smaller and so they are considered to be in a high resistance state.

The state of an MTJ is traditionally set by the application of a magnetic field induced by the current in a write line in the device. A
more recent form of MRAM is known as spin-transfer torque MRAM (STT-MRAM). This is a MTJ where spin-polarised electrons are used to directly influence the nature of the magnetic domains. If the electrons flowing into a layer change their spin, this induces a torque which is transferred to the nearby layer, reducing the current required to write to the cells.

FeFETs also have utility as NVMs, as the ferroelectric layer retains a permanent polarisation in the absence of a current, meaning the device retains its state. Ferroelectric materials are also used for ferroelectric RAMs (FeRAMs), possesses a similar structure to a DRAM cell, replacing the dielectric layer of the DRAM capacitor with a ferroelectric layer [130]. These differ slightly from FeFETs in that the transistor need not be ferroelectric.

D. Memory Devices as Solutions to Computational Problems

1) Case Study: Probabilistic Bits: Though researchers have posited MRAMs as a potential ‘universal memory’ [6], they also have been proposed for computational applications. One such application is probabilistic bits (P-bits). First proposed by Palem in 2003 [133], P-bits are a computational primitive analogous to bits in Boolean logic, or qubits in quantum computing. Unlike bits, which are either 1 or 0 at a given moment, or qubits, which exist in a superposition of states, where they are both 1 and 0, P-bits rapidly flip between 1 and 0 and so have a probability of being 1 or 0 at a given moment, making them a hardware implementation of a Bernoulli random variable. This property allows for them to be used to do computations directly on probabilities.

Khasanvis et al. constructed an array of P-bits based on strained-MTJs (S-MTJs) to implement a Bayesian network [88]. Compared to a digital CMOS implementation of the same Bayesian network using a 45 nm process, Khasanvis et al. claim area reductions up to 127×, a 214× power reduction and a 70× lower latency, based on HSPICE simulations comparing S-MTJ based circuits to 5-bit digital CMOS multipliers. However, the precision must also be considered. The 5-bit digital CMOS circuits simulated in the work have a precision of 1/16, whereas the S-MTJ circuits have a precision of 1/10. Component spacing is also an important consideration: Khasanvis et al. calculate a minimum rectangular area of 0.25 µm² to avoid magnetic interactions between devices. Modern digital CMOS devices can be below 10 nm and so have much higher possible integration densities.

Camsari et al. present the example of a genetic circuit, used to find the genetic correlation between two siblings (i.e., how related they are). SPICE simulations in which each of the family members are represented by a P-bit device and the correlation is found by using an XNOR gate, along with an RC circuit, to find the time average of the circuit output. Their circuit gave an output of around 0.5, which agrees with Bayes’ rule [22]. This is, in effect, a directed graph, which typically requires nodes to be sequentially updated from parent to child, whereas the simulations suggest good asynchronous operation. However, the authors do remark that further work is required to determine whether the behaviour generalises to larger networks.

The key difference between P-bits and MRAMs is that P-bits make use of a typically undesirable property of MTJs: instability. The magnetic materials used in MTJs exhibit a phenomenon that arises in ferro- and ferri-magnetic nanoparticles: superparamagnetism. This is where, under the influence of temperature, the magnetisation of the magnet randomly flips direction. The time period of this flip, τN, also known as the Néel relaxation time, is given by the Néel-Arrhenius equation:

\[ \tau_N = \tau_0 \exp \left( \frac{E_b}{k_B T} \right), \]

where \( E_b \) is the energy barrier level of the magnet, given by the product of the material’s magnetic anisotropy energy and its volume, \( k_B \) is Boltzmann’s constant and \( T \) is the temperature. \( \tau_0 \) is a constant with a value on the order of pico- to nano-seconds. A zero-barrier magnet, where \( E_b < k_B T \) would be ideal here, as the time period for a flip would be less than 1 ns [22].

This also illustrates well the intersection of devices, materials and computational research. As P-Bits offer a fundamentally different way to do computations by physically representing probabilities, they map computational problems such as Bayesian networks directly to hardware, which is of interest to both computing and devices researchers. However, as their performance is directly tied to materials properties, the ‘materials discovery’ aspect links directly to the computational problem. 2D materials offer particularly interesting opportunities for P-Bits as they are predicted to have very low magnetic anisotropy energies. The barrier of monolayer CrI$_3$ has been measured to be as low as 0.66 meV and is variable with the addition or removal of electrons. A barrier of 0.66 meV, using Equation 5 corresponds to a \( \tau_N \) of about 1 ns. Another candidate material, strained Fe-doped MoS$_2$, has a barrier of about 1.3 meV [22], corresponding to a \( \tau_N \) of 1.06 ns, which decreases with the addition of strain. For comparison, P-bit approaches using bulk materials from Borders et al. give best-case retention times of a few ms [18], and Mizrahi et al.’s simulations give a natural rate of 518 Hz, or 1.93 ms [19]. Pleeggi et al. report times on the order of a few ns using strained-MTJs [17] [16] [131], however these require an additional piezoelectric layer, adding material and space costs.

Camsari et al. do note that magnetic materials are not the only approach to implementing P-bits, proposing a general description of a P-bit as any three-terminal tunable random number generator [22]. The majority of prior implementations of P-bits make use of MTJs, with each P-bit having a structure very similar to cells used for MRAMs, consisting of a transistor with an MTJ cell connected to one of the legs. The input to the device, i.e., the gate, which tunes the device, effectively biases the stochastic output. Johnson-Nyquist noise, as observed in a resistor, is not useful here as it cannot be biased.

2) Case Study: Nonvolatile Memories for ANN Inference: A third example of mapping a computational problem to novel devices is the commonly described use of NVMs in crossbar arrays (Figure 19) to implement MVM operations. These use Ohm’s law and Kirchhoff’s laws, where the sum of currents from each device gives a final output current. The value of the output current corresponds to a particular signal strength. The major attraction of this approach for computer architects is that it significantly reduces the complexity of the MVM operation. Conventionally, given two vectors, \( x \) and \( y \), of the same size, \( n \), their dot product is \( \sum x \cdot y \). If each addition takes one clock cycle, then the complexity of the operation is \( O(n^2) \), i.e., quadratic time. Using the crossbar approach, the entire operation is completed in a single cycle, with complexity \( O(1) \) [22], i.e., constant time.

NVM implementations do face a number of challenges, however. Inherent inter-device variation can become an issue, leading to unpredictable behaviour. In large arrays, parasitic wire resistance is intensified and restricts the performance of devices. In the case of MVM, this means the precision of the weighted sum is reduced. Li et al. suggest solutions for overcoming issues with inter-device variability and parasitic wire resistance [110], stating that variability can be reduced by scaling down devices and wire resistance reduced by 3D integration. Another issue which still persists and is perhaps one of the key hindrances to the scalability of both 2D and 3D memristive circuits is that of sneak path currents [154]. Suppression of these requires a selector device with a highly nonlinear current-
1.4 billion dot-product operations can be completed per second. For a 16 CUDA cores operating at 1402 MHz [125], meaning that roughly values [169].

ReRAM implementation of the best-case cycle endurance, operating a simple 4x4 dot-product operation. The Nvidia GeForce 210 features one clock cycle per dot-product operation, as does a GPU [1]. Consider often used for ANN acceleration. A ReRAM-based approach requires endurance is still an important factor. A direct comparison to a CPU would not function well here. These circuits are not i.e.,

demonstrated a switching endurance on the order of $10^9$ cycles, about three orders of magnitude [57] compared to a layer in the CNN. However, Garbin et al.’s work on memristor-based device variation. Lin et al. recently demonstrated a 3D memristor circuit, consisting of eight monolithically-integrated layers of devices for inference using a CNN [111], in which each device layer represents a layer in the CNN. However, Garbin et al.’s work on memristor-based CNNs demonstrated the requirement for a much higher number of switching cycles, about three orders of magnitude [57] compared to fully-connected approaches, due to the reduced parallelism. Cycle endurance has been a key issue with memristive devices. Yang et al. demonstrated a switching endurance on the order of $10^{10}$ cycles in TaO$_x$-based devices, however many implementations exhibit much lower endurance.

Modern CPUs operate at switching speeds on the order of GHz, i.e., $10^9$ cycles per second and so even the best of the memristive approaches would not function well here. These circuits are not expected to operate at the same sorts of frequencies, however the endurance is still an important factor. A direct comparison to a CPU is unfair here and so a GPU is worth instead considering, as these are often used for ANN acceleration. A ReRAM-based approach requires one clock cycle per dot-product operation, as does a GPU [11]. Consider a simple 4x4 dot-product operation. The Nvidia GeForce 210 features 16 CUDA cores operating at 1402 MHz [125], meaning that roughly 1.4 billion dot-product operations can be completed per second. For a ReRAM implementation of the best-case cycle endurance, operating at a comparable speed, the devices would degrade shortly after one second. Top-end GPUs from Nvidia feature as many as 4608 CUDA cores, as well as Tensor Cores [126], which also offer accelerated performance for ML applications, meaning there is a large disparity between ReRAM and GPU performance. However, parallelised MVM hardware simply transfers the complexity, requiring $O(n^2)$ devices or cores, instead of $O(n^3)$ time. As a ReRAM approach requires only one device compared to an entire core in a GPU, ReRAMs offer a significantly more space-efficient solution.

A final consideration is that not all novel devices are likely to perform equally. For example, certain transistor materials and structures are better-suited to some applications than others; an amplifier circuit design to operate at radio frequencies would perform poorly if one used a transistor designed for audio applications, despite the fundamental circuit structure being the same. Likewise, certain ReRAMs (crossbars) made from a given combination of materials may be more suited to some applications than others. This is another example of how determining one’s computational problem first can lead to more impactful research. Flexible or disposable electronics, for example, may not require the endurance of conventional applications, or CMOS processes may be prohibitively expensive or unsuitable for such applications, and so NVMs such as those based on polymers [28] would be useful here.

VI. MACHINE LEARNING ACCELERATORS

Limitations in the performance of ML using conventional CPUs has resulted in the investigation of hardware accelerators, variously referred to by terms including ‘hardware neural networks’ or ‘intelligence processing units’. Often, such approaches are described as neuromorphic, as their design is influenced in part by biological systems. These come in a number of varieties, as the hardware requirements depend on the ML approach being implemented. It is worth making a distinction here about the precise aspect of ML that is being accelerated. By definition, ML involves a learning process (training) and is used to make predictions (inference). Thus, accelerators tend to focus either on training or inference.

A. Neuromorphic Systems

Neuromorphic computing systems are computing architectures which draw inspiration from the structure and physical operation of biological neural architectures. Architectures for neuromorphic computing range from all-digital implementations [116], [153], [53], [118] to mixed analog-digital implementations which emulate the dynamics of biological neural systems using the dynamics of man-made structures such as analog electrical circuits or phase-change materials [159], [39], [40], [24], [122], [139], [182], [14]. The models of neural circuits that neuromorphic computing systems emulate range from simple spiking neural networks to sophisticated models of the ion transport in biological neurons, captured in millions of differential equation instances. The applications of these neuromorphic systems demonstrated in the research literature range from digit recognition, speaker recognition and sequence prediction [50], to the modelling of mammalian olfactory pathways [23].

However, the term ‘neuromorphic’ is not well-defined. For example, a hardware realisation of a DNN using e.g., logic gates to perform MVM might be referred to as a neuroorphic system, despite possessing no real resemblance to a brain. On the other hand, a system with artificial neurons and synapses might also be referred to as neuroorphic. Another issue with discussions of neuromorphic systems is that the current understanding of the brain and animal nervous systems is relatively limited. Thus, in essence researchers are potentially designing systems which do not accurately mimic
biological processes, which may lead to unforeseen or faulty behaviour. Much of the modern devices literature relies on the neural network model of McCulloch and Pitts [114], and the Hodgkin-Huxley model of spiking neurons [70]. Although these have proven successful for neural networks, these are outdated models of neurons, and there are more accurate and up-to-date models, such as the Galves-Löcherbach stochastic model [53]. Conversely, there may also be unforeseen advantages to such approaches, however there is a large amount of uncertainty, which limits their usefulness in applications beyond research. This, alongside the loose definition of term neuromorphic therefore limits its usefulness in technical discussions, and so we avoid using it.

B. Feedforward ANN Accelerators

1) Digital CMOS: The reliability and ease of fabrication using CMOS processes makes them a natural option for use in ML architectures, as such an approach would allow easy and fast integration with existing computer hardware. Many CMOS approaches take the form of ASICs or FPGAs [128] [135] [137] [31] [104] [189] and a number of commercial options already exist [75] [62].

2) Nonvolatile Memories: ReRAM ML accelerators are commonly implemented using a crossbar array, with rows and columns corresponding to a bit or word line. This structure generally acts as the fully-connected layer in an ANN. Operation depends on whether the circuit is being used for training or inference. For training, the resistance of each ReRAM corresponds to the weight of a neuron in the ANN layer and the resistance values are trained either in- or ex-situ. In the former, the best resistance values for each device are determined by adjusting the circuit itself until the error rate is minimised. In the latter case, the optimum resistance values are determined outside of the circuit, e.g., through simulation, and the final values are programmed in before the circuit is used.

ReRAM crossbars are typically implemented as a single component connected to external off-the-rack circuitry, such as selectors, sense amplifiers, digital-to-analogue (DAC) and analogue-to-digital (ADC) converters. This external circuitry can become a limiting factor in the gains made by the ReRAM approach. If the external circuitry requires a significant amount of real estate or power consumption, then the performance gains of ReRAM crossbars may be significantly attenuated.

The inherent inter-device variation can also become an issue in ReRAM approaches. In large arrays, parasitic wire resistance is intensified and restricts the performance of devices. In the case of a MVM, this means the precision of the weighted sum is reduced. Li et al. suggest solutions for overcoming issues with inter-device variability and parasitic wire resistance [110], stating that variability can be reduced by scaling down devices and wire resistance reduced by 3D integration. Another issue which still persists and is perhaps one of the key hindrances to the scalability of both 2D and 3D ReRAM circuits is that of sneak path currents [154]. Suppression of these requires a selector device with a highly nonlinear current-voltage characteristic connected in series with the ReRAM. This is compounded by the fact that the large nonlinearity results in nonlinear amplification of noise and thus Ohm’s law, on which the crossbar MVM operation depends, no longer applies.

3) Other Feedforward ANN Technologies: Though CMOS and ReRAM implementations are the most common approach to implementing feedforward ANNs, they are not the only approach. Neurotransistors have also been explored. These utilise a ReRAM integrated with a transistor gate, which mimics the ‘integrate-and-fire’ behaviour of biological neurons [178] [11].

![Fig. 11. Schematic of the Hodgkin-Huxley model of a neuron [70].](image)

**Fig. 11.** Schematic of the Hodgkin-Huxley model of a neuron [70]. $C_m$ is a capacitance representing a lipid bilayer, $g_n$ is a nonlinear voltage source representing a voltage-gated ion channel (dependent on both voltage and time), $g_L$ is a linear voltage source representing the leak channels, $I_p$ is a current source representing ion pumps and the electrochemical gradients are represented by the voltage sources $E_n$ and $E_L$.

Optical implementations of matrix multiplication were demonstrated at least as early as 1970 [69] and a large body of the work on optical computing focuses on parallel computing and particularly matrix multiplication, making it of obvious interest for ML applications. However, optical/photonic implementations of neural networks specifically also exist. Hamerly et al. demonstrated an all-optical neural network which offered very low-energy operation for MVM operations and gigahertz speeds, as well as $≤ 1\%$ error rates on MNIST [69].

We would also be remiss not to discuss Reservoir Computing, a computational framework based on recurrent neural networks (RNNs) [166]. RNNs are a type of ANN which have a temporal sequence, and are used for tasks such as natural language processing (NLP) [108]. RNNs use previous outputs as inputs, i.e., the activation at a given time is a function of the activation at a previous time.

A reservoir computer (RC) builds upon several RNN models and so is also suited for temporal data processing. The reservoir part of a RC is treated as a black box, but has two requirements: it must be made up of individual nonlinear units and be able to store information [169]. A RC uses the reservoir to map inputs into a higher dimensional computing space, and then conducts pattern analysis in a readout section. Unlike other ANN approaches, a reservoir computer does not train the weights of the input or reservoir sections, only the readout part. This theoretically means a simplified and faster training process, as simple training algorithms, such as linear regression, can be used, with a focus on reduced computational cost compared to alternate approaches [166]. As with accelerators for other ML approaches, RCs have been realised using different devices and materials, including a photonics-based approach [101], or even a literal reservoir in the form of a water tank [51]. For a comprehensive review, see Tanaka et al. [166].

C. Spiking Neural Network Accelerators

1) Artificial Synapses: As discussed in Section [IV-A1], SNNs more closely resemble biological systems than feedforward ANNs. The spike train discussed serves as the integrate-and-fire mechanism, whereby the inputs to a neuron are summed until some threshold is reached, after which they fire. A common model, the Hodgkin-Huxley model, describes the activation level of a neuron with sets of differential equations with tens of parameters, which are difficult to compute [70]. Figure [1] shows a schematic of the model.
‘Leaky’ models are preferable, as these are less difficult to compute. A simple example of such a leaky neuron would be a leaky capacitor which sums the currents from input synapses and whose leakage current brings the neuron to a rest state. Alternatives using existing devices, such as Schmitt triggers [52], also exist.

Artificial synapses are themselves an area of active research, with many articles published demonstrating synapse-like performance for a range of devices and materials. A comprehensive review of nanoelectronic materials for use as artificial synapses was recently published by Sangwan and Hershman [148].

2) ReRAM as Artificial Synapses vs ReRAM as Feedforward Accelerators: ReRAM are often discussed in two main applications for ML approaches: as artificial synapses and as computational devices for accelerating feedforward ANNs. This can potentially lead to confusion in terminology. Often people may refer to the nodes in an ANN as neurons. As this borrows from neuroscience terminology, it can be easy to conflate and associate research into ANN accelerators as being aligned with artificial synapses, where this is not always the case. Section [V] presented the basic operation of a ReRAM: the resistance is dependent on the current that has previously flowed through it, an integral with respect to time. This can be seen as analogous to the operation of a biological neuron, whose leakage current may accumulate over time until the activation potential (i.e., threshold) is reached. When this threshold is reached, the neuron fires. This uses the properties of ReRAM in a different way to a crossbar MVM accelerator, where the state of the ReRAM represents a stored weight or value.

3) Digital CMOS SNN Accelerators: There is also a large body of research into hardware implementations of SNNs. Perhaps the best-publicised of these implementations is IBM’s TrueNorth, a hardware SNN implemented using 5.4 billion transistors and fabricated on a Samsung 28 nm CMOS process [117]. TrueNorth has a claimed power consumption of about 65 mW for multi-object detection and classification with 240×400 pixel 30 frames-per-second video input. However, their claimed classification precision of 0.85 on the test set of the DARPA Neovision2 Tower dataset was for 1920×1088 pixel images, making comparisons between the reported power consumption and the associated accuracy difficult to establish. In terms of power density, TrueNorth also reports a power density of 20 mW cm⁻², compared to 50-100 W cm⁻² for CPUs. For example, SpiNNaker (Spiking Neural Network Architecture), a massively parallel manycore architecture and part of the Human Brain Project, currently consists of 57,600 ARM9 18-core processors, corresponding to a total of 1,036,800 cores [5]. The TrueNorth team compare their platform to SpiNNaker, reporting 769× less energy consumption and 11.4× less silicon area, however these comparisons are not like-for-like: SpiNNaker cores are fabricated on a 130 nm process and different benchmarking suites are used.

It is important to draw a distinction between systems such as SpiNNaker, TrueNorth and ASIC approaches such as Google’s TPUs [61]. Although all are based on CMOS processes, their constructions and purposes are different. SpiNNaker aims to simulate the human brain, whereas TrueNorth has dedicated CMOS neurons and synapses, which do computation inspired by the way the brain works. ASIC approaches such as TPUs are simply hardware implementations of ANNs, e.g., to accelerate matrix multiplication.

D. Acceleration of other ML Approaches

As discussed in Section [V], there are a plethora of ML approaches beyond ANNs. Many of these are less-explored than ANNs however, so the body of work on hardware acceleration of them is also correspondingly smaller.

1) Support Vector Machines: Many hardware implementations of SVMs appear to be based on FPGAs [65, 98, 77, 190, 176], though most non-FPGA approaches still utilise CMOS technology. Genov and Cauwenberghs demonstrated a silicon-based ‘kerneltion’ SVM processor, which is a mixed-signal system consisting of an array of charge-injection devices combined with DRAM [59]. Kang and Shibata demonstrated a Gaussian-kernel based SVM using 180 nm CMOS technology [83] with a reported power consumption of around 220 µW. Takagi et al. reported a sub-100 mW SVM accelerator using a 65 nm CMOS process to implement a Histogram of Oriented Gradients algorithm [164] and Jeon et al. fabricated an accelerator for facial recognition using 5-transistor memory cells fabricated on a 40 nm CMOS process, with a reported power consumption of 23 mW [80].

2) Decision Trees: Hardware implementations of DTs are suggested to offer significant savings in power and improvements in throughput; de Franca et al. demonstrated a hardware DT classifier for dealing with network attacks with a reported 15× throughput compared to a software approach written in C++ which also had an energy consumption of 0.03% of the corresponding software implementation [42]. As with SVMs and indeed most ML accelerators, initial work on DT hardware accelerators utilised FPGAs. Struhalik proposed architectures suitable for implementation in both FPGAs and ASICs [161]. The hardware approaches proposed offered speedups between 8.58× and 1790.4× that of comparable software approaches whilst also offering reductions in the hardware resources required.

Saqib et al. proposed a pipelined accelerator for DT inference, testing it on the Iris and Contact Lenses databases and achieving accuracies of 98% and 83.3% respectively [139].

In-memory approaches have also attracted interest. Kim et al. proposed a DT accelerator design using memristors [93] for image-recognition applications. Their design was simulated for a 45 nm CMOS process and evaluated using several benchmarks, including MNIST, where it achieved an accuracy of 97.5%.

Kang et al. used a bespoke 6-transistor SRAM-based IC fabricated on a 65 nm CMOS process to implement a Random Forest DT accelerator [84].

More recently, Goswami et al. demonstrated a ‘molecular memristor’ for hardware implementation of a decision tree [53]. As well as demonstrating ML acceleration using a novel device, this work also uses materials properties to implement logic functions, with the different redox states of a given device representing different logic functions.

E. Hardware vs Software

It is worthwhile now to return to the thesis of this article, the disconnect between the materials devices communities on one hand, and the computer science and computer hardware architectures communities on the other. As discussed in Section [V], a number of benchmarks exist for evaluating the performance of ML systems. A comparison between the performance of new circuits implemented using newly-proposed materials and devices versus circuits based on silicon (often CMOS) and digital logic is a good way to address this gap, as metrics of success vary between the disciplines.

As we have already noted, neural networks implemented using novel materials and devices often perform significantly worse than their digital and silicon CMOS counterparts. Figure [12] shows the accuracies of several digital and silicon CMOS-based and approaches based on novel materials and devices against a given year. Table [III] and [IV]
show the corresponding specifications of each system. Again, these are intended as representative rather than exhaustive comparisons.

Fig. 12. Scatter plot showing the reported accuracies on the MNIST dataset of several technologies currently being researched.

The low accuracy of approaches based on novel materials and devices when compared to approaches based on digital silicon- and CMOS-based hardware, including software-programmable processors and GPUs, or fixed-function ASICs and other accelerators, is immediately obvious. The accuracies of ASIC approaches seem to lag algorithmic approaches by about ten years, despite ASIC being a mature technology. The ASIC and programmable hardware approaches both show a trend of progress, i.e., they become more accurate over time, however this does not seem to be as true for approaches based on ReRAMs or other experimental materials and devices, where time does not seem to correlate with improved accuracy. As the ‘other’ approaches are not a unified technology, but rather a range of different implementations, this can be forgiven, as a comparison would not make sense. These are included instead to indicate the accuracies reported for approaches outside the most popular ones. For memristors, a ten-year lag might be understandable, given the relative youth of the technology compared to CMOS or software (memristors were first experimentally realised in 2008 [162], ten years after the MNIST dataset was released [102]), however there is a lack of a clear trend in increasing accuracy over time.

Several authors have remarked on the scarcity of full-scale physical realisations of complete systems, and expressed the importance of experimental demonstrations of these [71] [107]. We suggest a parallel research path at each level of abstraction will have significant impact. Further materials research will help identify the best materials combinations for different applications. For example, 2D materials exhibit resistive switching mechanisms that do not exist in conventional bulk materials. Engineering of these properties may allow for greater control of switching, and thus more reliable and durable devices. Li et al. [109] recently demonstrated GRM-based ReRAMs using layers of PdSe₂, where resistive switching emerges due to grain boundary formation resulting from local phase transitions induced by electron beam irradiation. This control of grain boundaries allows for guided filament formation, allowing greater control than the stochastic filament formation typically observed in conventional materials.

Alongside this, progress towards full-scale physical realisations will aid in overcoming the engineering challenges that frequently emerge with producing novel devices at scale, as well as offering more tangible evidence for the impact and advantages of a given approach. Lastly, suitable application of novel devices can allow for more immediate application of novel technologies. For example, some approaches may eliminate the need for large numbers or high-endurance devices, as we discuss in Section VII.

The perceptions of accuracy in each community are also worth highlighting. It is not uncommon in devices research articles to see claims that accuracies of 90 % are comparable to a simulated hardware approach accuracy of 94 %, for example. Initially, this might appear relatively close, however, when the difference between best and the tenth best digital approaches have a difference of only 0.09 %, a 4.4 % difference is almost 50 × larger. Of course, the raw numbers do not tell the entire story. The leading digital approaches have millions of parameters; the top algorithm at the time of writing has 1,514,187 trainable parameters [21]. In comparison, many implementations based on novel materials and devices have only hundreds or thousands and so, understandably, do not perform as well. This makes it clear that a better metric is required, which we discuss in Section VII.

F. Materials, Devices, Architectures, and Algorithms

The overview of computing devices, algorithms, complexity and architectures we have presented, alongside comparisons of ML algorithm implementations in digital silicon- and CMOS-based hardware, as well as those based on novel materials and devices, brings us to a key thesis of this work. Many research articles published in the devices literature refer to phenomena such as the ‘decline’ of CMOS and indeed appear to treat CMOS circuits as synonymous with digital circuits. This is not the case, however. Many novel devices, including ReRAMs, are fabricated using CMOS processes, and some of the best-performing hardware implementations of ML algorithms, such as IBM’s TrueNorth [117], use CMOS processes. It is clear then that CMOS technology is not the limiting factor here, but the architecture. Architectures are thus equally as important as the fundamental technology, be it CMOS or some alternative. Despite being published in 1985, Keyes’ observations [86] about the successes of CMOS remain true and CMOS remains the most successful technology for computing devices, regardless of the high-level computer architecture. Simply recreating CMOS devices using novel materials, whilst maintaining the same fundamental way of doing computation has limited impact, as few match or better CMOS in the criteria outlined by Keyes. It is too early to say whether, under alternative computing paradigms, CMOS technology will remain dominant and so it remains worthwhile to investigate alternative technologies. A hybrid approach, where new materials and devices are integrated into CMOS processes is one possible avenue. Alternatively, technologies such as P-bits, as discussed in Section VII, where the fundamental nature of the computation relies on completely different device and material properties, mean it is likely that CMOS will not be the best technology for all applications.

VII. Outlook for Devices Research

A. Computational Complexity of Neural Networks

Livni et al. addressed the complexity of training neural networks [113]. The authors remark that successful learning with neural networks is computationally hard (i.e., is difficult to solve efficiently in polynomial time) in the worst-case, however, several tricks exist which allow for improvement in the efficiency of successful training.
The first and perhaps most relevant of these tricks to device physicists is to consider the activation function. Activation functions are a key part of ANNs, determining the threshold at which a neuron fires. Table V shows the most commonly used. Here we can see that different functions have different complexities and thus will have an influence on the overall efficiency of the network. However, a hardware implementation of these may offer significant advantages: if the transfer characteristic of a given device operates in a single clock cycle, then any of the activation functions will be reduced to a complexity of O(1).

Table V.

The Year of the Work and Their Reported MNIST Accuracy.

| Year | ANN Type | RAM Material | Algorithm | Accuracy Rate |
|------|----------|--------------|-----------|---------------|
| 2014 | CNN      | HBM          | CNN       | 99.65%        |
| 2013 | CNN      | PCM          | CNN       | 99.58%        |
| 2012 | CNN      | PCM          | CNN       | 99.75%        |
| 2011 | CNN      | PCM          | CNN       | 99.37%        |
| 2010 | CNN      | PCM          | CNN       | 99.03%        |
| 2009 | CNN      | PCM          | CNN       | 98.74%        |
| 2008 | CNN      | PCM          | CNN       | 98.50%        |
| 2007 | CNN      | PCM          | CNN       | 98.20%        |
| 2006 | CNN      | PCM          | CNN       | 97.90%        |
| 2005 | CNN      | PCM          | CNN       | 97.60%        |
| 2004 | CNN      | PCM          | CNN       | 97.30%        |
| 2003 | CNN      | PCM          | CNN       | 97.00%        |
| 2002 | CNN      | PCM          | CNN       | 96.70%        |
| 2001 | CNN      | PCM          | CNN       | 96.40%        |
| 2000 | CNN      | PCM          | CNN       | 96.10%        |
| 1999 | CNN      | PCM          | CNN       | 95.80%        |
| 1998 | CNN      | PCM          | CNN       | 95.50%        |

For a few thousand devices, the comparison becomes unfair. Thus we suggest that it is better to evaluate systems as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes, where the relations between outputs are useless as black boxes.
• Power Draw: the average power consumed by the system;
• Recognition Rate: the prediction accuracy of the system (i.e., the number of correct predictions divided by the total number of examples);
• Runtime: the time taken to make a prediction.

Based on these, we propose the following figures of merit for ML accelerator approaches.

1) Joules Per Recognition: As discussed already, many of the best-performing digital logic approaches for MNIST utilise over a million different parameters and many layers. This corresponds to a high cost in both time, resources, and energy consumption. By comparison, approaches based on novel materials and devices, such as ReRAM crossbars, use significantly fewer resources, however have lower recognition rates. Ideally, the higher the recognition rate the better, but the time and power costs can offset the advantages of accuracy: a facial recognition algorithm that only unlocks a mobile phone only when it is 99.98% certain the right face has been scanned is not much good if the algorithm takes several minutes and depletes the battery. On the other hand, an ML algorithm used for medical diagnosis must be as accurate as possible in order to minimise false positives or false negatives, although if it takes several weeks to run, this may also be a problem. Joules per Recognition (JPR) is thus a good performance metric for a system, as it accounts for energy consumption, time and accuracy:

\[
JPR = \frac{\text{Power} \times \text{Time}}{\text{Recognition Rate}}. \tag{6}
\]

2) Devices Per Recognition: Energy consumption alone does not tell the whole picture however: if one requires significantly more devices to run an algorithm with equivalent accuracy and in the same time, but with reduced power consumption, then the runtime power savings may be offset or negated by the physical space required by the system and, more generally, by manufacturing costs and energy requirements. Thus, Devices per Recognition (DPR) is a useful metric, as it evaluates the accuracy of the system against the number or physical devices required to implement it:

\[
DPR = \frac{\text{Device Count}}{\text{Recognition Rate}}. \tag{7}
\]

This metric is also useful as it helps quantify the device needed for a given task; a given novel device will not be a good candidate for computing tasks if the number of devices needed to solve realistic problem sizes is significantly large. Likewise, if a solution to a computational problem using some novel device requires only tens of devices, with comparable performance to a computer program running on reprogrammable digital CMOS hardware, using millions of transistors, then the novel solution would be a clear leader in this case.

3) Dot-Product Operations Per Second: The final figure of merit we propose is dot-product operations per second (DPOPS):

\[
\text{DPOPS} = \frac{\text{Dot-Product Operations}}{\text{Time}}. \tag{8}
\]

This is analogous to floating point operations per second, a common metric for computer performance. DPOPS describes the throughput of an accelerator in terms of speed and MVM size. Each crosspoint in a given circuit corresponds to a single weight, and so the number of operations in a single cycle would be equivalent to the number of crosspoints. The limiting factors here are thus crossbar size and also the time taken for a crossbar read and write operation; devices which are slow to program will limit the sequential speed of the system.

4) Optimisation of System Parameters: The desirable or acceptable performance of a system is ultimately application-specific and so it is likely that a balancing of various parameters will be necessary for each individual system design. Multi-objective or Pareto optimisation with our proposed figures of merit would provide a useful framework with which to determine the ideal balance of different parameters in a given implementation.

C. Other Proposals to Facilitate Evaluation and Comparison Between Domains

For reasons we discuss in Section\[11\] fixed-function hardware such as Google’s TPU have begun to use the IEEE bfloat16 format, and so we propose that this be a common standard of precision used for ML systems.

A final suggestion we propose is the standardised reporting of the computational cost in devices papers, e.g., as a dedicated section. Not only will this help researchers consider the scalability and viability of their own research, but it will help readers and those who build upon their work to better direct subsequent investigations. In the textbook, Introduction to Algorithms, the authors discuss ‘algorithms as a technology’ [38] and this is an important consideration. Returning to the example of ReRAM-based MVM operations, we can see that changing the architecture reduces the time complexity of the operation, but, more importantly, this does not smuggle the complexity elsewhere: the resource complexity grows linearly with input size.

For ML approaches, whether based on digital logic implemented in CMOS, or based on digital- or analog-domain computation using novel materials and devices, the understanding that any ML algorithm has three components makes this easy to calculate, as the complexity of the system or algorithm will be whichever term in the Learning = Representation + Evaluation + Optimisation equation grows the fastest.

D. Machine Learning Computational Problems and Hardware Solutions

In light of the end of Dennard scaling around 2006, researchers at UC Berkeley [10] from a variety of fields met to discuss and make predictions for the transition towards parallel computing. They described thirteen ‘dwarfs’, which are algorithmic methods that describe patterns of data communication and computation. The classification also accounts for ML applications, and Table VI lists the thirteen dwarfs and their corresponding applications in ML.

Not all the dwarfs are applicable to ML, and there is some overlap in applications, e.g., Dense and Sparse Linear Algebra both have utility for SVMs, PCA and ICA. These dwarfs pose an additional interesting consideration; conventional wisdom suggests that increased parallelisation can improve computation efficiency. However, as we have seen with the von Neumann bottleneck, one must also consider the movement of data itself, as well as the difficulty of a given computation.

Fundamentally, most ML applications are simply collections of more general computational problems. The properties of novel devices and materials may thus have the potential to perform these computations in different and more efficient ways than existing algorithms. If we consider the fundamental ML computations in isolation, ignoring the minutiae of a given ML application, we may see that novel devices have wider potential applications than implementing a given ML approach. For example, if we consider the fact that ReRAM crossbars implement MVM, rather than a neural network, we see that they also have utility as linear algebra accelerators, giving them use in applications described by the first two of the Berkeley


Many review articles in the devices literature discuss emerging technologies and their principles of operation, providing a comprehensive overview of the field, but many ultimately end with the message that useful implementations are far-distant due to engineering challenges and issues with scalability when compared to current CMOS devices. We instead suggest that emerging technologies may be better applied and commercialised if researchers shift their focus from the direct mapping of computational problems to the unique properties of new devices to achieve better performance in a given application than conventional digital CMOS devices using the above figures of merit.

VIII. SUMMARY AND CONCLUSIONS

In the past decade, ML has become an important and widely used tool across a range of disciplines and fields. However, the fundamentally different nature of ML computations when compared to traditional computer programs has shown limitations with mainstream computing methods for these approaches. This has resulted in the development of a variety of proposals for novel materials, devices, and architectures. Despite the technical ingenuity, skilled manipulation of device and material properties and new physics that many of these experimental devices and approaches have demonstrated, the transfer from lab to fab and the adoption of these devices by computer architects is minimal at best. In this work, we have evaluated a variety of proposed new forms of computation and sought to explain this disconnect. Firstly, we provide an overview of the fundamental concepts of computational complexity and physical limitations of computing. We then provide a tutorial overview of ML, with a focus on representation. Next, we discuss the use of novel materials and devices as solutions to computational problems, alongside a brief overview of candidate technologies. Following this, we provide a survey of different approaches to ML accelerators, and compare the performance of different approaches. Our key findings are (1): ANNs based on novel materials and devices significantly lag ANNs based on digital CMOS hardware (both fixed-function accelerator ASICs and programmable microprocessors, GPUs and FPGAs) in MNIST, a popular ML benchmark; (2): NVM implementations of ANNs, despite having been explored for the best part of a decade, have demonstrated no real trend of progress and (3): many proposed ML accelerators using experimental devices lack a physical realisation, relying on simulations of a system based on the performance of a few successfully fabricated devices. Though the problem of fabricating at scale is important to solve, suitable application of emerging technologies as solutions to computational problems, rather than as direct replacements for digital CMOS devices may circumvent this, as certain applications may not require high endurance or large numbers of devices. The first point in particular, the lag in performance, appears to be the result of differing conceptions of success between the materials, devices, and architectures communities. Finally, we propose several figures of merit and other suggestions that we hope will help unify the materials, devices, and architectures communities in the domain of ML research, enabling valid comparisons between approaches in both communities and fostering a dialogue to facilitate more impactful research.

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