An ultra-high ramp rate arbitrary waveform generator for communication and radar applications

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Abstract: Currently, the frequency ramp rate of most commercial direct digital synthesizer (DDS) chips is not more than several hundred MHz. In some communication or radar applications, the frequency ramp rate must reach several GHz. In order to greatly increase the frequency ramp rate, this paper proposes a full-custom multi-core & single-channel DDS (MCSC-DDS). This MCSC-DDS consists of some DDS sub-cores which are implemented in a field programmable gate array (FPGA) and a high speed digital analog converter (DAC) whose sampling frequency achieves several GHz. In FPGA, these DDS sub-cores operate in parallel to equivalent achieve ultra-high frequency ramp rate which is equal to the sampling frequency of the DAC. As an example, a compact and portable MCSC-DDS whose frequency ramp rate achieves 2.5 GHz is presented. It is mainly made up of a Virtex-5 FPGA and an AD9739. The measured chirp waveform has a maximum 2.5 GHz frequency ramp rate which demonstrates the efficiency of the MCSC-DDS.

Keywords: direct digital synthesizer (DDS), frequency synthesizer, arbitrary waveform generator, multi-core & single-channel DDS, radar source, ramp rate

Classification: Electron devices, circuits, and systems

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1 Introduction

By now, commercial DDS chips are widely used in radar and communication fields. The ramp nonlinearity of chirp waveform or linear frequency modulation continuous wave (LFMCW) generated by DDS is significantly determined by the minimum frequency ramp step size and frequency ramp rate. Fig. 1 shows the definition of ramp nonlinearity [1], frequency ramp step size and frequency ramp rate [2]. From Fig. 1, we can see that the frequency ramp step size is $\Delta f$, the time interval between steps is $\Delta t$, the ramp time is $\tau$, the frequency ramp rate is $f_r = 1/\Delta t$, the output bandwidth is $B$ and the ramp nonlinearity is $\eta = \Delta f/B$.

Because the minimum ramp step size of most commercial DDS chips is too small to take in to consideration, the frequency ramp rate is the key parameter to be considered. For example, the DDS chip AD9914 [2] has a minimum ramp step size of 0.81 Hz which is very small and a maximum frequency ramp rate of 145 MHz which is not very high. In some radar applications, such as LFMCW radar [3], the range resolution is significantly determined by the linearity of LFMCW. In order to achieve high range resolution, an ultra-high ramp rate DDS whose frequency ramp rate can reach several GHz is required. So the most commercial DDS chips, such as AD9914, may not meet the requirement. This is true in some communication applications as well. One way to solve this problem is to use a high speed DDS chip [4, 5, 6]. Though these DDS chips have very high sampling frequency, the frequency resolution is too low or the chip is not commercial. Some of them cannot sweep frequency.

This paper proposes a flexible, full-custom and easy implementable ultra-high ramp rate MCSC-DDS for communication and radar applications. Our MCSC-DDS is constructed by using commercial off-the-shelf components. Generally, the frequency ramp rate of most commercial DDS chips is far smaller than the sampling frequency, such as AD9914 whose sampling frequency is 3.5 GHz and the frequency ramp rate is only 145 MHz [2]. However, the frequency ramp rate of our MCSC-DDS is equal to the sampling frequency of DAC. Our MCSC-DDS is
made up of a group of low-speed DDS sub-cores and a high-speed DAC. All the DDS sub-cores are implemented in a FPGA and they are RAM-based. The exact number of DDS sub-cores is configurable and determined by the combination of FPGA and DAC. These low-speed DDS sub-cores operate in parallel to achieve a high-speed DDS. Compared with commercial DDS chips, our MCSC-DDS is capable of generating arbitrary waveforms and providing various potential applications in other fields.

2 The basic principle of the MCSC-DDS

Some rough and simple MCSC-DDS architectures have been presented in some papers, such as [7, 8, 9]. But the theory behind them is not presented. So, let us briefly deduce the basic principle of MCSC-DDS. Consider a sampled discrete-time sine wave:

\[ s(n) = a \sin(2\pi f_0 n T_s + \alpha) \]  

where \( T_s \) is the sampling interval, \( a \) is the amplitude, \( \alpha \) is the output phase and \( f_0 \) is the output frequency. Rewrite Eq. (1) in the form of series summation yields

\[ s(n) = a \sum_{m=-\infty}^{\infty} \delta(m - n) \sin(2\pi f_0 m T_s + \alpha) \]  

where \( \delta(n) \) is Dirac function and

\[ \delta(n) = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0 \end{cases} \]  

Decimate Eq. (2) by \( D \), and then Eq. (2) can be divided into \( D \) subgroups

\[ s(n) = a \sum_{m=-\infty}^{\infty} \delta[(Dm + 0) - n] \sin[2\pi f_0 T_s \cdot (Dm + 0) + \alpha] \]

\[ + a \sum_{m=-\infty}^{\infty} \delta[(Dm + 1) - n] \sin[2\pi f_0 T_s \cdot (Dm + 1) + \alpha] \]

\[ + \cdots \]

\[ + a \sum_{m=-\infty}^{\infty} \delta[(Dm + D - 1) - n] \sin[2\pi f_0 T_s \cdot (Dm + D - 1) + \alpha] \]  

Set

\[ s_i(n) = a \sum_{m=-\infty}^{\infty} \delta[(Dm + i) - n] \sin[2\pi f_0 T_s \cdot Dm + 2\pi f_0 T_s \cdot i + \alpha] \]  

where \( i \) is from 0 to \( D - 1 \). Substituting Eq. (5) into Eq. (4) yields

\[ s(n) = a \sum_{i=0}^{D-1} s_i(n) \]

\[ = a \sum_{i=0}^{D-1} \sum_{m=-\infty}^{\infty} \delta(Dm + i - n) \sin[2\pi f_0 T_s \cdot Dm + 2\pi f_0 T_s \cdot i + \alpha] \]  

According to the well-known DDS theory, for a DDS who has an N-bit phase accumulator, the output frequency satisfies
\[ f_0 = \frac{K}{2^N T_s} = \frac{K}{2^N} f_s \]  

where \( K \) is the frequency tuning word of DDS. Substituting Eq. (7) into Eq. (6) and collect terms produce

\[ s(n) = \sum_{i=0}^{D-1} s_i(n) = a \sum_{i=0}^{D-1} \sum_{m=-\infty}^{+\infty} \delta[(Dm + i) - n] \sin \left[ \frac{2\pi}{2^N} (DKm + iK + \phi) \right] \]

where \( \phi = 2^N a/2\pi \). Eq. (8) represents the basic principle of MCSC-DDS.

In Eq. (8), for each subgroup \( s_i(n) \), the sampling frequency is reduced to \( f_s/D \), so it can be implemented by a low-speed DDS sub-core which operates at \( f_s/D \). Because there are \( D \) subgroups in Eq. (8), we need \( D \) DDS sub-cores to implement Eq. (8). The exact value of \( D \) is determined by the combination of FPGA and DAC. In general, \( D \) is relatively small when we use a high-speed FPGA. On the other hand, \( D \) is relatively large when we use a high-speed DAC. For DDS sub-core \( i \), the core frequency tuning word is \( DK \), the phase control word is \( \phi \), the amplitude is \( a \) and the phase offset is \( iK \). A prototyping MCSC-DDS is designed according to Eq. (8). The block diagram is shown in Fig. 2. In Fig. 2, the MCSC-DDS is RAM-based. The output waveform is determined by the data stored in RAM and the corresponding parameters in Eq. (8). So this MCSC-DDS is capable of generating arbitrary waveforms. In general, a quarter period of sine wave is stored in the RAM, and for all DDS sub-cores, the RAM is the same. All the DDS sub-cores operate in parallel in FPGA. The output of each DDS sub-core is delivered to DAC through a high speed Multiplexer in sequence at \( f_s \). Generally, the Multiplexer is embedded in the DAC chip.

### 3 The principle of the ultra-high ramp rate MCSC-DDS

The basic MCSC-DDS mentioned above cannot sweep frequency. In order to sweep frequency at a very high speed, a more complex MCSC-DDS must be
designed to meet the high requirement in some communication or radar applications. The design procedure is shown below.

The sampled discrete-time linear frequency modulation (LFM) signal whose bandwidth is $B$ and pulse width is $\tau$ is written as

$$s(n) = a \sin \left( 2\pi \left( f_0 + \frac{1}{2} \mu n T_s \right) n T_s + \alpha \right) \tag{9}$$

where $\mu = \pm B/\tau$ is the signed LFM coefficient. Rewrite Eq. (9) in form of Eq. (6) produces

$$s(n) = \sum_{i=0}^{D-1} s_i(n)$$

$$= a \sum_{i=0}^{D-1} \sum_{m=-\infty}^{+\infty} \delta[(Dm + i) - n] \sin \left\{ 2\pi \left[ f_0 + \frac{1}{2} \mu(Dm + i) T_s \right] (Dm + i) T_s + \alpha \right\}$$

$$= a \sum_{i=0}^{D-1} \sum_{m=-\infty}^{+\infty} \delta[(Dm + i) - n] \sin \left[ 2\pi \left( f_0 + \frac{1}{2} \mu T_s \cdot Dm + \frac{1}{2} \mu T_s \cdot i \right) (Dm + i) T_s + \alpha \right]$$

$$= a \sum_{i=0}^{D-1} \sum_{m=-\infty}^{+\infty} \delta[(Dm + i - n) \sin[2\pi F(m, i) T_s \cdot Dm + 2\pi F(m, i) T_s \cdot i + \alpha] \tag{10}$$

where

$$F(m, i) = f_0 + \frac{1}{2} \mu T_s \cdot Dm + \frac{1}{2} \mu T_s \cdot i \quad \tag{11}$$

According to Eq. (7), set $f_0 = K_0 f_s / 2^N, \alpha = 2\pi \phi / 2^N$ and $\mu T_s = K_s f_s / 2^N$, where $K_s$ is the signed ramp step size of the DDS, $\phi$ is the initial phase control word and $K_0$ is the start frequency tuning word of the DDS. Hence, one can rewrite Eq. (11) as

$$F(m, i) = \frac{K_0 + \frac{1}{2} Dm K_s + \frac{1}{2} iK_s}{2^N} f_s = \frac{K(m, i)}{2^N} f_s \quad \tag{12}$$

where

$$K(m, i) = K_0 + \frac{1}{2} Dm K_s + \frac{1}{2} iK_s \quad \tag{13}$$

Eq. (13) represents the frequency ramp rule of DDS sub-core $i$. There are three terms in Eq. (13). The middle term $\frac{1}{2} Dm K_s$ varies linearly versus time series $m$, so it can be implemented by using an accumulator. It is named as frequency accumulator. According to Eq. (13), a digital frequency ramp block corresponding to DDS sub-core $i$ is designed. The prototyping architecture is shown in Fig. 3. From Fig. 3, we can see that the adder has an add/subtract control input. When $K_s$ is negative, the adder must be configured as a subtractor. In this case, the output of the ramp block is $K(m, i) = K_0 - \frac{1}{2} Dm|K_s| - \frac{1}{2} i|K_s|$ and the output frequency of the MCSC-DDS is ramping down. On the other hand, when $K_s$ is positive, the output of the ramp block is $K(m, i) = K_0 + \frac{1}{2} Dm K_s + \frac{1}{2} iK_s$ and the output frequency is ramping up.

Substituting Eq. (13) and Eq. (12) into Eq. (10) yields
Eq. (14) is the principle of ultra-high ramp rate MCSC-DDS. Because Eq. (14) is equal to Eq. (9), the frequency ramp rate of the output waveform is equal to the sampling frequency $f_s$. For each DDS sub-core, the frequency ramp rate is $f_s/D$. This feature allows the MCSC-DDS to accommodate applications with wideband modulation requirements.

Compare Eq. (14) with Eq. (8), we can see that their forms are uniform. The differences between them are that in Eq. (8) the frequency tuning word $K$ is time-independent, while in Eq. (14) the corresponding one $K(m, i)$ varies linearly versus time. As a result, in Eq. (8), the phase term $DKm$ will vary linearly versus time and it can be implemented by using a phase accumulator. On the other hand, in Eq. (14), the phase term $DK(m, i)m$ is a quadratic equation of the time series $m$, so it cannot be implemented by a traditional phase accumulator. Instead, a quadratic phase generation block is created to produce the quadratic phase. The architecture of the quadratic phase generation block corresponding to DDS sub-core $i$ is plotted in Fig. 4. As seen from Fig. 4, the quantity $K(m, i)$ is from the corresponding digital frequency ramp block shown in Fig. 3, and the quadratic phase generation block includes two sub-blocks. They are a time accumulator and a multiplier, respectively. The term time accumulator is first used in DDS design. Its input is a constant value of 1 which corresponds to the sampling interval $D/f_s$. Its output is the time series $m$ in Eq. (14). For all DDS-sub cores, the value of $m$ is equal. The multiplier multiplies the time series $m$ by the sub-core frequency tuning word $DK(m, i)$ and makes the quadratic phase term $DK(m, i)m$.

In practice, in FPGA, the time series $m$ is a non-negative variable. Suppose that the pulse width or the positive/negative ramp time is $\tau$, then $m$ is from 0 to $M - 1$, where $M$ is defined as
\[ M = \lfloor rf_s/D \rfloor \]  \hspace{1cm} (15)

For an N-bit time accumulator, its output range is from 0 to \( 2^N - 1 \). Generally, the maximum value of \( M \) satisfies the following inequality

\[ M < 2^N - 1 \]  \hspace{1cm} (16)

For example, set \( f_s = 2.5 \text{GHz} \), \( D = 16 \) and \( N = 32 \). According to Eq. (15) and Eq. (16), the maximum pulse with or ramp time is about 27 seconds. This value is huge for radar applications and nearly no radar system employ such a value. When the MCSC-DDS finishes one ramp and starts another ramp, the time accumulator must be firstly reset and then the value of \( m \) is from 0 to \( M-1 \) again.

According to Eq. (14), Fig. 2, Fig. 3 and Fig. 4, a prototyping ultra-high ramp rate DDS is designed. Its detailed architecture is depicted in Fig. 5. Compare Fig. 5 with Fig. 2, we can see that the phase accumulator in Fig. 2 is replaced by the quadratic phase generation block and the time-independent parameter \( K \) in Fig. 2 is replaced by the digital frequency ramp block. The other blocks keep the same. For each DDS sub-core, the frequency ramp rate is \( f_s/D \), the \( D \) DDS sub-cores operate in parallel to achieve the ultra-high frequency ramp rate. The advantage is that we can use relatively low speed devices to implement digital signal processing and use high speed devices to output waveforms. By controlling the corresponding parameters, such as the ramp step size \( K_s \), the upper limit value of the time series \( m \), this MCSC-DDS can generate arbitrary chirp waveforms whose frequency ramp rate is equal to the sampling frequency.

\[ \text{Fig. 5. The detailed architecture of the ultra-high ramp rate MCSC-DDS.} \]

4 A practical MCSC-DDS design and measured results

A practical MCSC-DDS which is composed of commercial off-the-shelf components is presented. Its block diagram is shown in Fig. 6. The FPGA is Virtex-5 and the DAC is AD9739. In FPGA, there are 16 parallel DDS sub-cores. The maximum
The sampling frequency of AD9739 is 2.5 GHz [10], so the maximum frequency ramp rate is 2.5 GHz and the sampling frequency of each DDS sub-core is 156.25 MHz. For each DDS sub-core, there is a 32-bit time accumulator and a 32-bit frequency accumulator. But the bits number is not limited to 32. Some other values, such as 48 or 64, are suitable depending on practical requirements. So the frequency resolution is user-defined. In fact, all the parameters mentioned are user-defined. The same data, a quarter period of sine wave, are stored in each RAM. In order to obtain the best results, the sampling frequency is 2.5 GHz. The sampling wave-master is LeCroy 8400A and the spectrum analyzer is ADVANTEST R3273. The output of MCSC-DDS is directly connected to the wave-master. There is no analog filter between MCSC-DDS and wave-master. This MCSC-DDS is capable of generating arbitrary LFM waveforms by controlling the corresponding parameters, such as $K_s$ and $K_0$. For observation convenience, the frequency ramp range is from 100 MHz to 900 MHz, the number of frequency ramp steps is 256 and the output pulse width is 102.4 ns. So the frequency ramp step size is 3.125 MHz and the time series $m$ is from 0 to 15 according to Eq. (15).

For comparison convenience, a simulated LFM waveform with the same parameters is generated in MATLAB simulation environment. The measured results are shown in Fig. 6 and Fig. 7, the simulated results are plotted in Fig. 8. The output spectrum of the LFM waveform is shown in Fig. 6. As seen from Fig. 7, the upper grid shows the generated LFM waveform. In the upper grid we can see that the amplitude of lower frequency components is larger than that of upper frequency components. This is determined by the sinc roll-off inherent at the DAC output [10]. In the upper grid of Fig. 8, a simulated LFM waveform is plotted. The lower grid of Fig. 8 shows the zoomed waveform. In both zoomed grids, the horizontal time axis is 400 ps per divider. From Fig. 8, in the lower grid, it is obvious that the frequency changes every 400 ps. Because each turning point represents one frequency component. The reason the zoomed waveform is like triangular shape is that the sampling frequency of DAC is not very high compared with these frequency components. On the other hand, we can clearly see that the waveform corresponding to the lower frequency components is like sinusoidal shape. This is because the sampling frequency of DAC is very high compared with these frequency components. Compare Fig. 7 with Fig. 8, we can see that the waveforms are in agreement. So we can conclude that the output frequency of MCSC-DDS.
changes every 400 ps. In other words, the frequency ramp rate is 2.5 GHz. From [2], we can find out that the frequency ramp rate of AD9914 is 145 MHz, so the frequency ramp rate of MCSC-DDS is about 17 times that of AD9914. If AD9914 generates the same LFM waveform, the ramp step size is 53.13 MHz. According to [1], the ramp nonlinearity $\eta$ of DDS is defined as $\eta = \Delta f / B$, where $\Delta f$ is the ramp step size and $B$ is the output bandwidth. So in the case of Fig. 7, the ramp nonlinearity of AD9914 corresponding to the bandwidth is $53.13 / 800 = 6.64\%$, while in the case of MCSC-DDS the ramp nonlinearity is only $3.125 / 800 = 0.39\%$.

5 Conclusion

This paper presents a flexible and easy implementable MCSC-DDS. The parameters, such as the number of DDS sub-cores, frequency resolution and frequency ramp step size, are all user-defined. The significant feature is that the frequency ramp rate is equal to the sampling frequency of DAC, while most commercial DDS chips do not have such high frequency ramp rate. According to the deduced principle of MCSC-DDS, a practical MCSC-DDS whose frequency ramp rate achieves 2.5 GHz is produced. This MCSC-DDS is capable of generating arbitrary LFM waveforms and other waveforms. An example of a LFM waveform whose bandwidth is 800 MHz, pulse width is 102.4 ns and frequency ramp rate is 2.5 GHz is generated to demonstrate the performance of the MCSC-DDS.
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