Understanding Memory Modules on Learning Simple Algorithms

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Abstract

Recent work has shown that memory modules are crucial for the generalization ability of neural networks on learning simple algorithms. However, we still have little understanding of the working mechanism of memory modules. To alleviate this problem, we apply a two-step analysis pipeline consisting of first inferring hypothesis about what strategy the model has learned according to visualization and then verify it by a novel proposed qualitative analysis method based on dimension reduction. Using this method, we have analyzed two popular memory-augmented neural networks, neural Turing machine and stack-augmented neural network on two simple algorithm tasks including reversing a random sequence and evaluation of arithmetic expressions. Results have shown that on the former task both models can learn to generalize and on the latter task only the stack-augmented model can do so. We show that different strategies are learned by the models, in which specific categories of input are monitored and different policies are made based on that to change the memory.

1 Introduction

The generalization ability of neural networks is the most important criterion to determine whether they are powerful or not. Recent work on memory-augmented neural networks (MANN) has shown promising results about generalizing perfectly on simple-algorithm tasks \cite{grefenstette2015, joulin2015, graves2016, rae2016, gulcehre2016}. However, understanding the working mechanism of memory modules has not been well studied. Existing work has stopped at conjecturing the underlying learned strategies based on shallow, single-case visualization without any further verification. This raises concern of the lack of interpretability and hinders us from designing better memory modules. Currently, there are two main difficulties for interpreting the black-box memory-modules.

Firstly, the diversity among the different MANNs makes it hard to isolate the functions of memory-modules. Consequently, we cannot focus on the decisive parts of the models, as the different designs make the comparison work hard to carry out. Secondly, to interpret MANNs is challenging. Although interpretation methods for RNN models are well studied, little attention has been paid on that for MANNs.

To solve the above problems, we formalize a unified framework for MANNs with different implementations of memory modules, which makes comparison among different memory modules feasible. Then, we propose a novel qualitative analysis method based on dimension reduction for interpreting memory cells by verifying hypotheses. We implement neural Turing machine and stack-augmented neural network under the unified framework and carry out detailed analysis on two algorithm tasks consisting of reversing a random sequence and evaluating arithmetic expressions to show the effectiveness of our proposed analysis method.

The experiment and analysis have shown that the external memory can compensate for the need for storing intermediate results to travel along the dependency path. Specifically, neural Turing machine generalizes well on mirror task, and stack-augmented neural network generalizes well on reversing a random sequence and evaluation of arithmetic expressions. To summarize, our main contributions are as follows:

\begin{itemize}
  \item We generalize different MANNs with a unified framework, which ensures the fairness of comparing different memory mechanisms.
  \item We propose a novel analysis method for memory cells. By applying our analysis method, we infer and verify the hypotheses about what strategy has been learned by the model that can generalize well.
\end{itemize}

2 Our unified MANN framework

In order to compare different types of memory modules, we propose a unified framework for MANNs by fixing the controller and memory access interface. By abstracting the processing components used in stack augmented neural network \cite{joulin2015, yogatama2018} and neural Turing machines \cite{graves2014}, the framework shown in Figure 1 contains an LSTM controller, a memory module at time $t$ with $N$ cells represented as $M_t = [m_0, m_1, \ldots, m_{N-1}]^T \in \mathbb{R}^{N \times d}$ equipped with a specific read-write method, such as push and pop actions of the stack memory extension.

The input $i_t$ at time step $t$ to the controller is a combination of the system input $x_t$ at time step $t$ and readout $r_{t-1}$ at the
Last time step. Formally,\[ h_t = f_i(x_t, r_{t-1}). \] (1)

where \( f_i \) is a learnable function and we here take it simply to be a concatenation operation. The state of the LSTM controller is represented as \( h_t \), updated by the standard LSTM model:\[ h_t = \text{LSTM}(i_t, h_{t-1}). \] (2)

The controller output \( o_t^{(c)} = h_t \) and the input \( x_t \) are then inputted to the write module and the read module, indicating how to interact with the memory. Finally, the readout \( r_t \) is combined with the controller output \( o_t^{(c)} \) to form the system output \( o_t \) at time step \( t \):
\[ o_t = f_o(o_t^{(c)}, r_t), \] (3)

where \( f_o \) is also a concatenation function.

In this paper, we experiment with two typical MANNs whose external memories are a stack memory and a tape memory respectively. To implement the two models under our proposed framework, we only need to specify the detailed read and write methods, which are shown in Section 2.1 and 2.2 respectively. As a special case, an LSTM model is an instance of the framework without memory\(^1\).

2.1 Stack memory

We adopt the stack-augmented neural network (SANN) proposed in Yogatama et al. [2018]. The readout at each time step is just the top of the stack:
\[ r_t = M_t[0]. \] (4)

For each write step, there are \( 2K + 2 \) possible actions \( a_t \)'s to choose:
- **PUSH\(_k\)**: Push the transformed current controller state \( f_s(h_t) \) onto the stack after \( k \) (\( k = 0, 1, 2, \cdots, K \)) pops.
- **STAY\(_k\)**: Keep the stack unchanged after \( k \) (\( k = 0, 1, 2, \cdots, K \)) pops.

Where \( f_s \) is a learnable function and is implemented as a linear transformation.

In order to ensure the model differentiable, the write step for the stack is formalized as the expectation of the memory after one of the \( 2K + 2 \) specific actions \( a_t \):
\[ M := \sum_i p(a_i|M) \cdot M_{a_i}, \] (5)

where the \( M_{a_i} \) is the memory after the action \( a_i \) is adopted, and the probabilities of the write actions \( a = [a_0, a_1, \cdots, a_{2K+1}]^T \) is computed using the current memory \( M_t \) and the system input \( x_t \):
\[ p(a|M, x_t) = \text{softmax}(W_{aM}\text{Conv1d}(M_t) + W_{ax}x_t + b_a), \] (6)

where the \text{Conv1d} is a two-channel 1-D convolutional operation with a size-2 kernel over the \( N \) memory cells.

2.2 Tape memory

As the memory in a standard Turing machine is called a tape, we here name the class of neural Turing machines by TANNs, i.e. tape augmented neural networks. The tape memory module is adopted as mentioned in Graves et al. [2014], with random access read-write steps totally controlled by the controller.

Both the read and write actions contain two preparation steps before the actual interaction with the memory: 1) an analysis step to the controller state and 2) an addressing step. The detailed formulas of these two steps are omitted here. After the addresses to read and write are determined, the readout is the expectation of the memory cells over distribution \( w^r \):
\[ r_t = \sum_{i=0}^{N-1} w^r_i [i|M_t], \] (7)

where \([i]\) means to index the \( i \)th row of the vector or matrix. And the write step:
\[ M_t = M_{t-1} \odot (1 - w^w e_t^T) + w^w a_t^T, \] (8)

which is combining the influence of erase vector \( e_t \) and add vector \( a_t \) on the memory \( M_{t-1} \) over the distribution \( w^w \).

3 Experiment

In the experiment, we want to figure out which kind of and how memory module helps generalize on two algorithm tasks including reversing a random sequence (called mirror task) and evaluating arithmetic expressions (called \textit{M10AE} task). Simple RNN (SimpRNN) and LSTM are adopted as two baseline models, which represent neural networks without external memory modules.

| task       | input     | output                        | measure |
|------------|-----------|-------------------------------|---------|
| mirror     | \( x_1x_2 \cdots x_{L} \) | \( x_Lx_{L-1} \cdots x_1 \) | input length |
| \textit{M10AE} | \( 8 + 6 \div 3 \div 2 - 4 \) | 4 | \#LPO |

Table 1: Task examples. The \( x_i \) represents the \( i \)th random binary vector. \#LPO is short for number of low-priority operators. Note that for \textit{M10AE} the \( \div \) represents a modulo operator and each intermediate result is followed by a modulo-10 operation. For an instance, the evaluation procedure of the example in the table can be done in 4 steps: i. \( (6 + 3) \% 10 = 8 \), ii. \( (8 \% 2) \% 10 = 0 \), iii. \( (8 + 0) \% 10 = 8 \), iv. \( (8 - 4) \% 10 = 4 \).

\(^1\)The LSTM model contains internal memory actually. The term memory mentioned in this paper all refers to external memory, if without specific explanation.

\(^2\)Although the policy is parameterized in a recursive formula in the original paper, we find this simple setting is powerful enough.
3.1 Experimental settings

For mirror task, the input is a sequence of binary vectors whose size is 9. During encoding (input) stage, the inputs are randomly sampled from Bernoulli distribution with \( p = 0.5 \) and the inputs are zero vector during decoding (output) stage. This setting is similar to that of copy task in Graves et al. [2014]. Both the number \( N \) of and size \( M \) of memory cells are 20. The controller dimension is 100. For M10AE task, the input embeddings \( x_t \)’s are trainable parameters from random initialization. The input embedding dimension 100. The dimension of a memory cell and a controller state is set to be equal to the input embedding dimension. The number of memory cells is chosen from \([5, 10, 20]\). We adopt training using Adam algorithm with batch size chosen from \([32, 64, 128, 256]\) and the learning rate chosen from \([0.001, 0.0001]\). The hyper-parameters are tuned on a development set.

3.2 Mirror

First, we are interested in exploring whether SANN and TANN are able to learn to output the input sequence in a reverse order, which we call mirror task. An example of this task is shown in the first row of Table 1. We append a delimiter at the end of the input to tell the model when to output, and it is noted as (EOS). We adopt the length of input sequence as the difficulty measure of each sample.

**Result**

The maximum length of input sequence is 5 during the training stage, and the maximum length is extended to 10 when testing. Here we view a prediction as correct only if the whole output sequence is the same as that of the input. The result is shown in Figure 2. We can find that both SANN and TANN can generalize beyond input length of training samples. Figure 2b shows that SANN converges faster than TANN, which corresponds with the intuition that stack memory is more suitable for this task.

![Figure 2](image1.png)

Figure 2: (a) Test performance along with different input length for mirror task. Black dash line indicates the maximum length of input sequence during the training stage. (b) Learning curves for each model on mirror task in the training stage, whose y-axis indicates the performance on the training set.

**Analysis**

Since TANN and SANN can generalize greatly, we here analyze both of them to investigate what strategy they have induced. In order to gain a general averaged insight into what mechanism underlying these two models on mirror task, we generate 500 samples with the same length, whose each input binary vector is restricted in the binary format of \( 1, 2, \cdots, 9 \).

These numbers can be viewed as the labels of the samples, which helps index the input vectors. And all the analysis for mirror task is based on the 500 samples.

![Figure 3](image2.png)

**Figure 3**: Averaged visualization about (a and c) controller gate and (b and d) read-write policy for TANN and SANN on mirror task. Note that all the plots are derived from being averaging over 500 random samples. The x-axis shows each time step represented by input \( x_t \) or output \( y_t \). The (EOS) represent the input delimiter.

We first are interested in investigating how the controller gates change on mirror task. Specifically, we plot in Figure 3a and 3c the averaged saturation ratio [Karpathy et al., 2015] of the input gates and forget gates of the controller along with each input. Here a gate is defined right-saturated if its value is larger than 0.9 and defined left-saturated if its value is less than 0.1. Comparing these two figures, we can find that both TANN and SANN are sensitive of the delimiter in terms of each controller gates, after which dramatic changes of saturation rate appear. The change of controller gates of TANN seem more complicated than that of SANN, which indicates it is much easier to control a stack memory to finish the mirror task than a tape memory. The early convergence of SANN on mirror task can also support this idea.

We then visualize the read-write and push-pop policies for TANN and SANN respectively. For read-write policy of TANN, we average the expected address over the 500 samples. The expected address \( p_t \) for read and write operations at time step \( t \) can be calculated as:

\[
p_t = \sum_{i=0}^{N-1} w_t[i] \cdot i, \tag{9}
\]

where the \( w_t \) is either \( w^r_t \) or \( w^w_t \) to get the expected address for read or write. For SANN, the push probability is just the probability sum mass of all type of push actions:

\[
P(PUSH|M_t) = \sum_{k=0}^{K-1} P(PUSH_k|M_t), \tag{10}
\]

and the expected number of times to pop (noted as \( n_{pop} \)) at time step \( t \) can be calculated as:

\[
n_{pop} = \sum_{k=0}^{K-1} P(POP_k|M_t) \cdot k. \tag{11}
\]
The result is shown in Figure 3b and 3d. We can find that both for TANN and SANN the policies for encoding (solid red lines) and decoding (solid blue lines) information are opposite to each other, indicating reversing in their own ways.

Based on these findings above, we make hypothesis about what strategy learned by TANN by the following pseudocode:

**input:** sequence of binary vectors \( s = x_1, x_2, \ldots, x_L \)

**output:** the reverse of the input sequence

1. \( M \in \mathbb{R}^{N \times M} \) \( \triangleright \) initialize the memory randomly
2. \( w^w \leftarrow 17 \) \( \triangleright \) initialize the writing-to-address
3. for each input \( x_i \) in \( s \) \( \triangleright \) encoding stage
   4. if \( x_i \) is a delimiter then \( \triangleright \) the end of the input
      5. \( w^r \leftarrow (17 + L - 1) \% N \) \( \triangleright \) initialize the reading-from-address
   6. else
      7. \( M[w^w] \leftarrow x_i \) \( \triangleright \) write to store \( x_i \)
      8. \( w^w \leftarrow (w^w + 1) \% N \) \( \triangleright \) point to the next cell
   9. end if
10. end for
11. for \( i \) in 1, 2, ..., \( L \) \( \triangleright \) decoding stage
12. output \( M[w^r] \) \( \triangleright \) read and output
13. \( w^r \leftarrow (w^r - 1) \% N \) \( \triangleright \) point to the next cell
14. end for

And the hypothesis strategy for SANN on mirror task is:

**input:** sequence of binary vectors \( s = x_1, x_2, \ldots, x_L \)

**output:** the reverse of the input sequence

1. empty the stack \( S \)
2. for each input \( x_i \) in \( s \) \( \triangleright \) encoding stage
   3. if \( x_i \) is not a delimiter then \( \triangleright \) store information
      4. push the \( x_i \) to \( S \)
   5. end if
6. end for
7. for \( i \) in 1, 2, ..., \( L \) \( \triangleright \) decoding stage
8. output the top of \( S \) \( \triangleright \) read and output
9. pop the top of \( S \)
10. end for

The next goal is to verify these hypotheses above. To this end, we evaluate the hypothesis information encoded in each memory cell by our proposed qualitative verification method. This method is based on the assumption that if the intermediate results are the same in a certain step of the hypothesized strategy, then their distributed representations in the memory should be similar as well. In detail, this includes 4 steps:

1. Collecting the memory cells \( m_{(1)}^i, m_{(2)}^i, \ldots, m_{(l)}^i \) at the same position in the memory at the same time step.
2. Labelling the memory cells with the corresponding results \( \tilde{y}_1^{(1)}, \tilde{y}_1^{(2)}, \ldots, \tilde{y}_1^{(l)} \) derived from the candidate strategy to get pairs \( \{m_{(i)}^{(j)}, \tilde{y}_1^{(i)}\}_{i=1}^l \).
3. Using t-SNE [Maaten and Hinton, 2008] to visualize the labelled memory cell vectors.
4. If there appear the clear labelled clusters, then the candidate strategy is reasonable.

The examples are shown in Figure 4. The compact labelled clusters in Figure 4a, 4b (for TANN) and Figure 4d, 4e (for SANN) support the hypothesis semantics shown in the captions of each subfigure. We also include negative examples in Figure 4c and 4f to exemplify when the evaluation result shows the hypothesis is not reasonable. Since the input sequence are randomly sampled, labelling guided by a wrong hypothesis can not cover all the samples and this mismatch will also show up in the visualization as chaotic labels.

![Figure 4](image-url)

Figure 4: Six examples of qualitative evaluation result of hypothesis information encoded in memory cells of TANN (a, b and c) and SANN (d, e and f). The parts before the semicolon in the captions are the time step and the memory cell address, noted in the form of \( \langle \text{time step}, \langle \text{cell address} \rangle \rangle \). And after the semicolon is the hypothesis semantics of the memory cells, represented as certain position of the input sequence.

### 3.3 M10AE

After analysis on mirror tasks, we are then interested in extending the interpretation procedure to the harder case. We propose a new simple algorithm task named *modulo-10 arithmetic expressions, M10AE*, in which each input sequence is in the form of an arithmetic expression without parentheses and the output is the evaluation result of it. In order to make the task tractable to analyze while preserving the recursive nature inside it, we add the following constraints:

- Each numeral is limited in 1, 2, ..., 9.
- The / represent a modulo operator.
- Each intermediate result is modulo by 10.
- The * / have higher priority than + and -.

An example is shown in the second row of Table 1. Based on the constraints, the evaluation results can only range in integers from 0 to 9, and thus we formalize the task as a 10-class classification. Since the computation procedure interrupts when encountering low-priority operators and thus larger number of low-priority operators (#LPO) means larger memory burden, we take #LPO to be the difficulty measure for M10AE.

Recently, Hupkes et al. [2018] and Jacob et al. [2018] have proposed two similar tasks. However, they formalize the task as either a regression problem or a two-digit sequence prediction problem, without consideration of the intermediate re-
sults. These settings are poor at restricting the space of intermediate results, whose distribution is much sparser, and this hinders us from verifying a candidate strategy empirically. By contrast, in M10AE, the result is given as a classification label, and both the intermediate results and the final results range in integers from 0 to 9 due to modulo-10 design. This leads to abundant samples for each intermediate category.

Result

80 and 20 thousand examples are generated for training and validation, respectively. The maximum #LPO is 14 for training and 20 for validation. The results are shown in Figure 5. Overall, the performance of all the models except SANN drops quickly with the increase of #LPO. Figure 5a indicates the SANN has learned to generalize on this task. In addition, the models with an external memory are better than the ones without any external memory (i.e. LSTM and SimpRNN). By contrast, the baseline model simpRNN performs extremely bad, indicating that the internal memory of LSTM is crucial for this task. As shown in Figure 5b, all the models converge slowly, which indicates the complexity of the task.

![a. test performance](image1)

![b. learning curves](image2)

Figure 5: (a) Test performance along with different input length for M10AE task. Black dash line indicates the maximum #LPO of input sequence during the training stage. (b) Learning curves for each model on M10AE task in the training stage.

Analysis

As the SANN seems to induce a stable strategy, we then analyze it. We generate 500 samples with the same structure to get general averaged patterns. And the analysis is all based on these 500 examples. These examples are noted as \( \langle N_0 \rangle \langle L_0 \rangle \langle N_1 \rangle \langle H_1 \rangle \langle N_2 \rangle \langle H_2 \rangle \langle N_3 \rangle \langle L_1 \rangle \langle N_4 \rangle \), where \( \langle N_i \rangle \) represents the ith numeral, \( \langle L_i \rangle \) represents the ith low-priority operator (i.e. + or -, ) and \( \langle H_i \rangle \) represents the ith high-priority operator (i.e. * or /). One samples is \( 8+6*5/2-4 \). Other samples generated by substituting the operators and numbers at the same position into the other symbols from the same category, e.g., * to /, + to -, 1 to 2, and etc..

In the same way with Section 3.2, we first visualize the controller gates and the read-write policy of SANN. The results are shown in Figure 6. As shown in Figure 6a, The controller gates peak at the time steps when the low-priority operators (i.e. \( \langle L_0 \rangle \) and \( \langle L_1 \rangle \) in Figure 6a) appear, which indicates the controller of SANN track specific categories of symbols as the controllers do in mirror task. As shown in Figure 6, the push/pop actions are adopted regularly with respect to local structures: 1) every time the lower-priority operator (+, -) comes, the push probability goes to zero and the expectation of pop times rise up sharply to around 3; and 2) when dealing with high-priority operations (*, /), the push/pop lines go up/down with each numeral input relatively more gently.

![a. controller gate](image3)

![b. push-pop policy](image4)

Figure 6: Averaged visualization about (a) controller gate and (b) push-pop policy for SANN on M10AE task. The x-axis shows each time step represented by categories of input symbol.

However it is still hard to make a hypothesis about what SANN has learned, and we then visualize the averaged memory at each time step to get further clues shown in Figure 7. The pattern is highly regular: the stack pops all its stored items when it comes to the end of a term (i.e. \( \langle N_0 \rangle \) and \( \langle N_1 \rangle \langle H_0 \rangle \langle N_2 \rangle \langle H_1 \rangle \langle N_3 \rangle \) here), which is consistent with Figure 6b; during processing each term, the stack pushes every time it sees a high-priority operator.

![input symbols along time](image5)

Figure 7: Averaged visualization about memory cells along with input sequence. Each memory cell vector is truncated from 100-D to its first 3 dimensions. Darker blue represents higher weight. Blue dashed boxes show the possible number of cells at each time step. Red solid boxes show possible information flow.

A hypothesis about what strategy SANN has induced is shown below:

**input:** arithmetic expression \( e = x_0, x_1, \cdots, x_L \)

**output:** the evaluation result of \( e \)

1. \( S \leftarrow [0,0,\cdots,0]^T \in \mathbb{R}_N \) \( \triangleright \) stack
2. \( l_0, l_1 \leftarrow 0 \) \( \triangleright \) low/high-priority results
3. \( l'_0 \leftarrow 0 \) \( \triangleright \) temporary low-priority result
4. \( p_0, p_1 \leftarrow \text{null} \) \( \triangleright \) low/high-priority operators
5. for each input \( x_i \) in \( e \) do
6. if \( x_i \in \{+,\} \) then \( \triangleright \) for low-priority operators
7. \( p_0 \leftarrow x_i \) \( \triangleright \) save the operator
8. pop till empty
9. else if \( x_i \in \{*,/\} \) then \( \triangleright \) for high-priority operators
10. \( l_0 \leftarrow l'_0 + \) \( \triangleright \) adopt the candidate result
11. push \( (l_1, x_i) \) \( \triangleright \) push the combination
12. else \( \triangleright \) for numerals
13. \( l_1, p_1 \leftarrow S[0] \) \( \triangleright \) read the combination pushed
14. \( l_1 \leftarrow \text{eval}(p_1, l_1, x_i) \) \( \triangleright \) high-priority operation
15. \( l'_0 \leftarrow l_0 \) \( \triangleright \) save the candidate result
16. \( l_0 \leftarrow \text{eval}(p_0, l_0, l_1) \) \( \triangleright \) low-priority operation
17. pop till empty
18: \text{push } l_0 \quad \triangleright \text{ push the whole result so far}
19: \text{end if}
20: \text{end for}
21: \text{return } l_0

where \text{eval}(f, a_0, a_1)\footnote{As a special case, if the stack is empty or } f \text{ is null, the second argument of this function will be returned.}

There are two kinds of storage in this hypothesis, in-controller storage \(l_0, l_0', l_1, p_0, p_1\) and in-memory storage \(S\). An example is shown in Figure 8, where the boxes and arrows in purple (an evaluation step, e.g. \(6*3/2-4\) at time step 4) and red (a combination-pushing step, e.g. push the combination of 6 and \(*\) at time step 3) directing the information flow indicates a recursive strategy.

As a special case, if the stack is empty or \(f\) is null, the second argument of this function will be returned.

Figure 8: Applying the hypothesized strategy to the example \(8+6*3/2-4\). The value of all the variables is displayed at each time step below the expression.

As in Section 3.2, we then verified the hypothesis by our proposed analysis method. The result is shown Figure 9, where the clear clusters (in Figure 9a and 9b) indicate the hypothesis is reasonable. A negative example is also included in Figure 9c for illustration about an unreasonable hypothesis.

Figure 9: Visualization for verifying what the memory cell vectors represent. The parts before the semicolon in the captions are the time step and the memory cell address, noted in the form of \((\text{time step}), (\text{cell address})\). And after the semicolon is the hypothesis semantics of the cell vectors, represented as specific parts of \((N_0)\langle L_0\rangle (N_1)\langle H_0\rangle (N_2)\langle H_1\rangle (N_3)\langle L_1\rangle (N_i)\).

4 Related Work

The related work can be divided into two categories, memory-augmented neural networks and visualization methods.

4.1 Memory Augmented Neural Network

The first MANN model is NTM, neural Turing machine [Graves et al., 2014], which is proposed to assign logical control flow over external memory to RNNs. These types of models are associated with the automaton theory. The MANNs can be viewed as RNNs with only internal memory augmented with different types of data structures, as a simple DFA is to form complex automaton like PDA, LBA and Turing machine. Thus some work focus on various memory types from different prior bias for specific tasks. For example, an RNN can learn to generalize on context-free grammars augmented with stacks [Joulin and Mikolov, 2015; Grefenstette et al., 2015], learn to model shortest syntactic dependency with a gated memory [Gulcehre et al., 2017] and learn to solve shortest-path tasks with a more general tape memory [Graves et al., 2016]. Some work is dedicated to overcoming the defects of these models, especially for NTMs, such as separating each memory cell into content and address vectors [Gulcehre et al., 2016], introducing memory allocation and de-allocation protocols [Graves et al., 2016; Munkhdalai and Yu, 2017], speeding up the addressing mechanism [Rae et al., 2016] and adding adaptive computational design [Yogatama et al., 2018].

4.2 Understanding Recurrent Networks

Understanding the RNNs and their variants is enjoying renewed interest, as a result of successful applications in a wide range of machine learning problems on sequential data. For one thing, many work focus on what the RNNs remember in their hidden states. Some visualize the dynamics of the LSTM gates in terms of absolute value and saturation rates that keep track of the structure hints [Karpathy et al., 2015; Ghaeini et al., 2018]. And some plot t-SNE visualization for clause representations and derivative saliency maps to understand the polarity changes in sentiment analysis [Li et al., 2016a]. There are also researches trying training multiple decoders to predict the history inputs for checking what and how much information is stored [Koppula et al., 2018]. And in Verwimp et al. [2018], the gradient matrix of the states with respect to the input embeddings is decomposed with SVD to find the principal direction in the input space. For another, which part of the input has a key effect on the model decisions is also a popular topic. Many works view this problem as searching the minimum set of word vectors or their dimensions to flip the models’ decision [Li et al., 2016b; Westhuizen and Lasenby, 2018]; and there is other work computing different relevance measures between inputs and outputs to explore the contribution of the words [Arras et al., 2017; Ding et al., 2017; van der Westhuizen and Lasenby, 2017].

5 Conclusion

In this paper, we analyze strategies learned by memory augmented neural networks on task of reversing random sequence and evaluation of arithmetic expressions. By visualizing the controller gates and read-write policy for the memory, we find both models can summarize the input symbols into categories and dynamically change the policy according to these categories. We make hypothesis about what strategy is induced by the models, and verifying them by our proposed novel qualitative analysis method. One can mimic the analysis pipeline for other settings and thus this work helps inspire more researches on the strategy interpretation for MANNs.
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