A 5291-ppi organic light-emitting diode display using field-effect transistors including a c-axis aligned crystalline oxide semiconductor

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Abstract
C-axis-aligned crystalline-oxide semiconductor field-effect transistor (CAAC-OS FET) can be scaled down to a width and a length of 60 nm. We fabricated an organic light-emitting diode (OLED) display with more than 5000 ppi, which is required in virtual reality (VR) display applications, using CAAC-OS FETs as the backplane.

KEYWORDS
high resolution, IGZO, micro display, OLED, VR

1 | INTRODUCTION

Virtual reality (VR) as a technology has recently become a popular topic of research, especially in the development of more realistic VR worlds requiring the fabrication of displays with higher resolutions. For example, head-mounted displays (HMD) necessitate the use of more than 5000 pixels per inch (ppi) to prevent users from noticing the pixels at short distances. Although recently developed small, medium, and large displays utilize field-effect transistors (FET) the size of a few micrometers, the fabrication of high-resolution displays (greater than 5000 ppi) would require the use of FETs smaller than a micrometer within the pixels. However, scaled-down FETs may negatively affect the display performance due to phenomena such as the existence of a short-channel effect.

Oxide semiconductors (OS) have recently been widely employed as an alternative to low-temperature polycrystalline silicon and hydrogenated amorphous silicon backplanes owing to their advantage of not requiring a laser crystallization process. In 1985, Kimizuka et al performed the first synthesis for a notable example of OS called indium gallium zinc oxide (IGZO), which paved the way for a wider field research. Table 1 illustrates the crystallinity classification of the IGZO material. Yamazaki et al proposed a crystalline oxide semiconductor named c-axis aligned crystalline IGZO (CAAC-IGZO), which Kimizuka described as neither crystal nor amorphous but “an intermediate state” between the two states. Here, crystallinity in the intermediate state is defined as crystalline where nanocrystal (nc) IGZO and others are also classified. Additionally, FETs that employ the crystalline IGZO in their active layer exhibit favorable characteristics. For example, in contrast to Si-FETs, FETs with a CAAC-IGZO active layer have an extremely low off-state current and a high on-off ratio and are less likely to suffer...
from the short-channel effect. Thus, CAAC-IGZO also exhibits an advantage in terms of scaling.\textsuperscript{22}

In this paper, we propose a high-resolution organic light-emitting diode (OLED) display with more than 5000 ppi that utilizes a c-axis-aligned crystalline-oxide semiconductor field-effect transistor (CAAC-OS FET) backplane.

2 | MOTIVATION FOR DISPLAYS WITH 5000-PPPI PIXEL DENSITY

In one type of VR applications, users wear an HMD, and images are projected through a display mounted on the headset; hence, wearable displays in the form of goggles and glasses are being developed as HMDs. If lenses are not used, then the distance between the HMD display and the eyes of the person wearing the headset is between 12 and 40 mm. According to the calculation completed by Clark,\textsuperscript{23} the visual acuity of a human eye is 0.59 arcmin per line pair. Based on this visual acuity and the assumption of a 30-mm distance between the eyes and the display, headset wearers would not be able to notice each pixel in front of their eyes if the pixel pitch is approximately equal to 5.15 $\mu$m, corresponding to approximately 5000 ppi. Therefore, the projection of realistic VR images in an HMD would be enabled by the incorporation of a high-resolution display with more than 5000 ppi.

3 | PROPERTIES OF CAAC-OS FET

Smartphone displays use a resolution between 400 and 500 ppi, less than the VR display requirement of more than 5000 ppi. In other words, the size of each subpixel of a realistic VR display would be approximately 3 $\mu$m, where transistors used in devices similar to smartphones are too large and unsuitable for the purpose. Moreover, the amount of electric current that flows in each pixel of OLED displays is proportional to the pixel size, implying that the amount of electric current that flows through the device would be smaller. Consequently, backplanes for displays with more than 5000 ppi would require the following properties: (a) transistors with short length and (b) current capability suitable to control an OLED device.

We considered these factors in adopting CAAC-OS FETs for the backplane of our high-resolution display prototype.

Figure 1A shows a perspective view of the CAAC-OS FET. The CAAC-OS FET had a three-gate structure that improves electric-field control of the gate surrounding the channel. Figure 1B indicates that the CAAC-OS FET exhibited favorable $I_d$–$V_g$ characteristics for width ($W$) and length ($L$) of 60 nm ($W/L = 60$ nm/60 nm). Figure 1C shows the FET’s gate breakdown voltage. Note that gate leakage was virtually negligible up to 10 V.

The current capabilities and current saturation of high-resolution OLED displays need to be considered when small driving FETs are utilized. Figure 2A,B shows the $I_d$–$V_g$ and $I_d$–$V_d$ characteristics, respectively, of a CAAC-OS FET with $W/L = 60$ nm/200 nm. The pixels of our high-resolution OLED display prototype employed driving FETs of $W/L = 60$ nm/200 nm with an operating range of $V_g$ less than 1.0 V when displaying images. Specifically, in Figure 2B, CAAC-OS FETs exhibited favorable saturation characteristics even at short lengths and ample amount of current flow for control of the OLED devices. This confirms that CAAC-OS FETs are suitable for backplanes of high-resolution OLED displays.

Additionally, CAAC-OS FETs have the advantage of exhibiting an extremely low off-state current, making them suitable for display applications. Figure 2A indicates that even when the channel length of the

\begin{table}
\centering
\begin{tabular}{|c|c|c|}
\hline
Amorphous \textsuperscript{[19, 20]} & Crystalline & Crystal \textsuperscript{[5, 8, 18]} \\
\hline
completely amorphous & \textbullet CAAC \textsuperscript{[14]} & \textbullet single crystal \\
& \textbullet nc \textsuperscript{[15, 16]} & \textbullet poly crystal \\
& \textbullet CAC \textsuperscript{[17]} & excluding single crystal and poly crystal \\
\hline
\end{tabular}
\caption{Classification of crystallinity of IGZO\textsuperscript{11–20}}
\end{table}
CAAC-OS FET employed as a driving FET is scaled-down to 200 nm, the off-state current remained lower than $1 \times 10^{-12}$ A, which is below the measurement limit. Therefore, when the display shows black, the amount of electric current that flows would be extremely small, leading to a low-power consumption.

4 | PANEL STRUCTURE

Figure 3A shows the configuration of our display prototype, which has a resolution of 1280 $\times$ 720 pixels. The scan drivers surrounding the pixels consist of n-type OS-FETs, formed in the same layer and the same process as the pixels’ selection and driving FETs. Thus, the formation of all these components does not result in an increased number of process steps. The scan drivers are positioned at both sides of the pixel array.
with the gate lines connected to the scan drivers on the left side and the right side alternately, as shown in Figure 3B.

5 | CIRCUIT CONFIGURATION AND OPERATION

Figure 4A,B displays a block diagram and a timing chart, respectively, of a scan driver, whereas Figure 5 shows one of the shift registers (SRs) composing our proposed scan driver. A gate start pulse (GSP) was input into the first-stage SR, which, with a four-layer GCLK and GPWC, generated a shift pulse at GSROUT and a gate signal at GOUT, for the next-stage SR. Accordingly, the scan driver in Figure 4A corresponded to the scan driver (L) in Figure 3B. The GOUT of each SR were gate signals to rows 0, 2, 4, 6, ..., and 2N-2.

The shift pulse and the gate signal were generated and output by GOUT and GSROUT (Figure 5), respectively, in the following manner.

First, a GRES signal initialized the voltage of node O1 to GVSS and that of node O2 to GVDD-Vth (Vth corresponds to the threshold voltage of the OS FET). At this point, GOUT and GSROUT were both fixed at GVSS.

Next, the shift pulse of GSROUT was input to LIN, changing the voltage of node O1 to GVDD-Vth and that of node O2 to GVSS. The voltage of node O1, GVDD-Vth, was input to node OA via M6 and to node OB via M9, thus allowing M7 and M10 to be turned on. Node O2 was connected to and subsequently shuts the gates of M8 and M11.

With M7 and M10 turned on, the voltages of GOUT and GSROUT increased when CLK1 and PWC1 were
changed from LOW to HIGH. With this, bootstrap capacitors C2 and C3 increased the gate voltages of M7 and M10 from GVDD-$V_{th}$. Thus, GOUT and GSROUT output the shift pulse and the gate signal, respectively, without a drop in the $V_{th}$. In this case, M6 and M9 contributed to the efficient increase of the gate voltages of M7 and M10.

**FIGURE 4** (A) Block diagram and (B) timing chart of the scan driver

6 | PIXEL STRUCTURE

Figure 6A shows a subpixel circuit diagram of our display prototype using an OLED device. Each pixel was configured at 2Tr1C. In all the subpixels, the selection FET, M1, was an OS-FET with $W/L = 60\text{nm}/60\text{nm}$, whereas the
driving FET, M2, was an OS-FET with \( W/L = 200 \text{ nm}/60 \text{ nm} \). The symbol C1 represents a storage capacitor.

Figure 6B describes that at a display prototype of a high-pixel density, the pixels were arranged in a zigzag pattern similar to that in Shiokawa et al.\textsuperscript{24} The subpixel pitch was equal to 2.4 \( \mu \text{m} \) horizontally and 3.2 \( \mu \text{m} \) vertically, and all pixels that emit red, green, and blue (R, G, and B) light of the display prototype were configured for them to have the same pixel pitch.

Theoretically, human vision is limited to 60 cycles per degree. Thus, if more than 60 light-dark cycles occur at a viewing angle of 1°, humans would not distinguish light and dark but would instead perceive an intermediate color.

For best quality, smartphones should be viewed from a distance of approximately 30 cm. At this position, the estimated distinguishable resolution would then be approximately equal to 500 ppi, along with a visual acuity of 60 cycles per degree.

Moreover, a person would not be able to distinguish between zigzag and stripe arrangements in such a display resolution, as it is theoretically impossible for the human eye to distinguish each pixel at a pixel density surpassing 5000 ppi.

Moreover, a zigzag arrangement allows the pixels to form a square at 2 \( \times \) 2 pixels (approximately 2500 ppi) and would virtually bear no effect on visibility.

7 | OLED DEVICE

Figure 7 presents the structure of the OLED display prototype, which employed a white OLED as the light-emitting device. Here, the acronyms TFE, EIL, ETL, HIL, and HTL denote the thin film encapsulation layer, the electron injection layer, the electron transport layer, the hole injection layer, and the hole transport layer,
respectively. The OLED display prototype adopted a microcavity structure, had a narrow luminance spectrum, and was colored by a color filter (CF) formed over the white OLED device.

8 | SPECIFICATIONS AND DISPLAY IMAGE

Table 2 reveals the specifications of the display prototype, which achieved a pixel density of 5291 ppi by using CAAC-OS FETs within the size range 60 to 200 nm and through scaling down of the subpixel pitch to 2.4 μm × 3.2 μm. The display prototype was designed with a frame frequency of 120 Hz for VR use.

In Figure 8, the triangle with a white circle on each tip represents the color gamut of the display prototype, whose NTSC ratio was 74.4%. This ratio is expected to increase after future optimization of the fabrication conditions of the color filters.

Figure 9A shows an actual photograph of the display prototype, with the 6.14 × 3.16 mm display region at the center and the scan drivers on its left and right sides. Figure 9B shows the image displayed in this small display region and indicates that the 5291-ppi high-resolution display prototype with pixels and scan drivers that utilize CAAC-OS FETs with the sizes W/L = 60 nm/60 nm and W/L = 60 nm/200 nm has successfully displayed an image with good quality. The screen door effect could not be observed with the

![FIGURE 6](image6.png)  
(A) Subpixel circuit diagram and (B) arrangement of pixels

![FIGURE 7](image7.png)  
Structure of OLED device. OLED, organic light-emitting diode

![TABLE 2](image2.png)  
Display specifications

| Specifications          |          |
|------------------------|----------|
| Screen diagonal        | 0.28 in  |
| Resolution             | 1280 × 720 |
| Subpixel pitch         | 2.4 μm × 3.2 μm |
| Pixel density          | 5291 ppi |
| Frame frequency        | 120 Hz   |
| Aperture ratio         | 31.3%    |
| Coloring method        | White OLED + color filter |
| Emission type          | Top emission |
| Source driver          | External |
| Scan driver            | Integrated |
naked eye or even after zooming in 10 times with a magnifying lens.

9 | CONCLUSION

We fabricated a high-resolution OLED display prototype with 5291 ppi using CAAC-OS FETs as the backplane. Results validated that CAAC-OS FETs can be scaled down and that they are capable of controlling the electric current necessary for the small pixels in a display with a pixel density of more than 5000 ppi. As the current demand entails the fabrication of 3-inch displays in VR applications, our next challenge is focused on the enlargement of the screen size.

FIGURE 9 (A) Photo of the display prototype and (B) image displayed on the display prototype

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