The Memorism Processor: Towards a Memory-Based Artificially Intelligence Complementing the von Neumann Architecture

Katsumi Inoue * and Cong-Kha Pham **

Abstract: Central processing unit (CPU) and graphics processing unit (GPU) are weak ("weak" means inefficiency) at detecting information represented by search, reference and recognition for reason of computer architecture. The memorism processor is a memory base processor which complements CPU’s weak point. The two memorism processors called set operating processors (SOP) and database processors (DBP) are the device technology that covers the processing that CPUs and GPUs are not good at. Their profitability in various information processing including rapidity and energy saving performance has been proved and therefore there are great expectations for them as a device technology in the post-Moore era. In addition to the conventional SOPs and DBPs, we have developed cross operating processors (XOP), which are excellent at combination/comparison operation and therefore we have applied for a patent of it. These three memorism processors are expected to play a great role in the evolution of the artificial intelligence. This paper is contributed as continuation of [K. Inoue, M. Odaka and C.-K. Pham: Memorism Processor which complements weak point of von Neumann processor, Proc. SII2016, pp. 267–270, 2016], and the authors propose computation that is more suitable for the artificial intelligence era.

Key Words : CPU, function-memory, non-von Neumann computer, IoT, AI.

1. Present Situations and Problems of AI

In recent years expectations and interests in artificial intelligence (AI) have been rising as never before. This is because big data have come to be used via internet easily, computing power such as central processing unit (CPU) or graphics processing unit (GPU) has been improved, and the capacity of memories and storage has been expanded.

The applicable field of AI is extremely extensive and a number of methods based on it exist in addition. The application fields of AI are extremely wide and there are numerous methods, however the two major trends of AI are deep learning which evolved neural networks and natural language processing [1]. Deep learning imitates the function of the brain by arithmetic operation, especially the high-speed arithmetic operation power such as GPU is the driving force of development. The idea of a neural network as deep learning originates the arithmetic calculation which was the maximum value of the person thinks. Scientists of AI call arithmetic calculation as the function of the brain ("arithmetization of thinking") by many mathematicians.

As a matter of course, the human brain does not perform arithmetic calculation when the person thinks. Scientists of AI in those days (1950’s) only replaced the human thought with the arithmetic calculation which was the maximum value of the computers for convenience. This idea deserves to be called calculus. Although many achievements such as recognition of images and sounds are provided by deep learning, many needs of users for current deep learning are to make learning methods easy, shorten learning time, and further reduce the size and power consumption of the system. If there is another method to mimic highly and efficiently the human brain that does not stick to arithmetic calculation, it will be one of the next important AI technology. Set operating processor (SOP) is a technology invented in view of the above problem [2]–[12].

On the other hand, the natural language processing that is represented by Watson of IBM constructs knowledge processing equivalent to the functions of a brain based on the database called the knowledge representation, and therefore its measures are in contradiction to neural networks. The natural language processing is applied to the field where data encoding is possible and the construction of the knowledge representation database is its greatest characteristic. The knowledge representation arranges the database that extracts various data such as words, the appearance frequency of words, the correlation between words, the order of their appearances, and their categories from big data, and performs processing that is equal to the functions of a human brain artificially using this large-scale database. The capacity of memories and storage has been expanded and their costs have been lowered.

This is the motive power of the natural language processing development, while on the other hand the equipment would upsize and complicate unless it becomes easy to store knowledge representation and to extract the stored data. Furthermore, it would take enormous time for designing and tuning as a result. Therefore, even if there is an excellent idea, we fail to realize it with high probability in the AI field. Database processor (DBP) is a technology invented in view of the above problem [13]–[15]. In order to examine the problems in AI, it is necessary to look back on the history and the architecture of the current computer.

2. The von Neumann-Type Computer

The computers (von Neumann computer) routinely used nowadays were developed 70 years ago so as to realize a high-
level and high-speed arithmetic operation such as calculation of trajectory of artillery. It was extremely epoch-making equipment in the era when there were only analog-type calculators such as abacuses and slide rules. The architecture of a CPU, which is the core of a von Neumann computer, is a step-by-step sequential processing, and therefore its versatility is high and it can be applied to various information processing other than arithmetic operations. Therefore, it is used in various fields, and the information processing performed by a CPU varies from OS processing, data processing and IO processing to processing with information detection such as search, reference, recognition and so on.

However, the miniaturization technology that has greatly contributed to realizing of today’s IT society is reaching its end and reconstruction of computers and rebooting computing have come to be expected. Fortunately, various effects of the memristor processor have been proved nowadays and it is necessary to review and rebuild the past IT technique in which all information processing is left to CPUs regardless of whether these CPUs are good at such processing or not.

3. What is Required for a New Computer

Even if the limit of the miniaturization technology is reaching its limit, almost all users' needs for speeding-up, even higher performance and higher accuracy, cost reduction and power saving will be pursued for eternity. The contemporary theme on reaching the fourth industrial revolution is the needs of AI including edge computing and deep learning of the internet of things (IoT).

The intellectual processing such as recognition is the processing that current computers are weakest at, and a new type of computer is demanded whose techniques are not only improved versions of conventional von Neumann computers. However, computers that take a lot of time to practical use or computers that are completely different from the concepts so far will abandon all the existing technology assets. And hence, current infrastructures such as application technologies can not follow up such computers. Technology that instantaneously keeps up with the above demand without changing the concept of the current von Neumann type computer, which can be used immediately and achieves remarkable effects is the most realistic one.

3.1 Outline of Information Detection by Memory and CPU

Figure 1 shows the configuration of a general memory. For example, the address is 1 M (1 million) or 1 G (billion) while the data width n is 32 bit or 64 bit, which is a very vertical long configuration.

When a CPU fully scans the memory of such a structure, n times of accesses are required. Therefore, even in the case that the fastest CPU and the fastest memory module (DDR4 PC4-34100 DIMM) are combined, the limit of the information detection performance would be the transfer rate of 34.1 GB/s as full scan performance (≈ information detection of 1 unit).

A human brain finds out appropriate information from barrage of information that is supposed to be around 1 PB (10^15 Byte) with the energy of only around 20 W in around several 10 ms so as to maintain our life activity. In the case of carrying out data of 1 PB with one set of CPUs and memory modules, it would take more than 1 PB/34.1 GB/s ≈ 30,000 s ≈ 8 h. Even in the case of a distributed processing with the K computer, which consumes electric power of 12 MW with more than 80,000 of CPUs in parallel, it would require as long as 0.37 s. Even except such an extreme case, repeated computation and information detection that is concentrated in a short time are severe for a von Neumann computer.

In order to alleviate the fate of the von Neumann type computer as described above, we must rely on utilization technology. Information retrieval algorithms and metadata such as indices for databases and Fourier transformations for image processing have been used for a long time. However, information search algorithms and meta data have five issues as follows:

- Firstly, in order to find out target information from a large quantity of memory data effectively, there are no other ways but to ask experts with various knowledge and experience to build software making full use of complicated and difficult algorithms and meta data.
- Secondly, it is necessary to create meta data based on basic data, which means that processing time needs to be secured for it. Therefore, it is difficult to achieve real time performance and quick response.
- Thirdly, memory space for meta data is larger than that for basic data by a few times in case of a transposed index of full text search. Such cases are never few.
- Fourthly, it is necessary to update (maintain) the meta data every time the basic data are changed, revised or added. Further, even partial change in basic data requires extensive maintenance for the meta data. Therefore, load (power loss) on a CPU such as the background processing and night batch processing during night are not outstanding but extremely large.
- Fifthly, in the case of consuming too much meta data such as the index related to the above, the performance of the system extremely deteriorates and therefore tuning work is required to acquire an optimum state. These problems need be solved.

The above means that complicate and time-consuming procedure is required at the time of writing data in a memory and
operational units are arranged on the bottom of the address di-
pact and super parallel GAPs comprised of 1 bit logic (Boolean) this memory base processor, as shown in the figure, ultracom-
processors (DBP), which are excellent at the search and refer-
4.1 Outline of DBP
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The memorism processor is based on this idea. A group of array processors (GAP) that enable super parallel (collectively) processing of memories and data are integrated in one chip and perform batch data processing (process in a lump) without processing data one by one.

The memorism processor is based on this idea. A group of array processors (GAP) that enable super parallel (collectively) processing of memories and data are integrated in one chip, and processing of the high-level information detection (search, reference and recognition) is realized in a self-contained manner in one chip. The memorism processor reduces processing time of the CPU and the electric power consumed for information detection such as search, reference and recognition, which is the heaviest load among the processing performed by a CPU.

4. Database Processor (DBP)
4.1 Outline of DBP

Figure 2 shows outline of the configuration of the database processors (DBP), which are excellent at the search and refer-
ence of accumulated data such as data table or record data. In this memory base processor, as shown in the figure, ultracom-
and super parallel GAPs comprised of 1 bit logic (Boolean) operational units are arranged on the bottom of the address di-
rection of the memory cell for memorizing database information.

In other words, these \( n \) GAPs correspond to \( n \) pairs of cas-
caded memory cell groups on a one-to-one basis, and the cas-
caded memory cell groups are the field data of one set of record data. The data width \( n \) of a general memory is 64 bit while the data width of DBP vary from tens of thousands to millions of bits per chip, which is considerably wider than that of a gen-
eral memory and raises the parallelism of GAPs as a result. Its technical details are described in the reference [13]–[15].

The high-level and very-high-speed information retrieval such as perfect matching, comparison data and data counting is re-
alyzed by assigning (reading) the memory data of the selected address in super parallel in GAPs and repeating logical product (AND), logical sum (OR), logical negation (NOT) and exclu-
sive logical operation (XOR) of 1 bit in each record-parallel for predetermined number of times.

4.2 The Possibility of ASIC Implementations of DBP
We have conducted fundamental researches on various types of SOPs and DBPs by GAP processings from various points of views such as speed-up of information detection or electric power for information processings. For future application specific integrated circuits (ASIC), it is necessary to study in detail on optimum operation clock, power consumption and appro-
input-output configuration. Based on the past research results, performance expected by applying ASICs to DBPs is summarized in Table 1.

The possibility of ASIC implementations for DBP ①∼③ is shown in Table 1. A low power type CPU is sufficient for the CPU for reading the results obtained by giving operation condi-
tions to these four types of DBPs. The implementation ④, field programmable gate arrays (FPGA) are configuration ex-
amples of DBPs that have been put into practical uses. In the case of FPGAs, it is difficult to use large-scale memories or a large quantity of GAPs due to the limitation of logic resource of the FPGAs. ALTERA Arria V (average power consumption of around 10 W) with data volume of 32 Krecord×512 bit is used and 32 K pieces of GAP are implemented, which realizes ad-
ress selection and operation in GAPs shown in Fig. 2 in 10 ns. Therefore, full scanning of field data of 512 bit is achieved in 5 \( \mu \)s. The speed of current information processings is improved abundantly as shown in the above example of a supercomputer.

Further, if the index has been used, the search will be faster but will cause other adverse effects. Therefore, performance values that represent the ability of the memorism processor objec-
tively is needed. The authors focus on the fact that the ability for information detection with the current CPUs and memories reaches its limit in data transmission rate of the memories. The values obtained by dividing the total data capacity of this mem-
ism processor DBP by the time of full scan (processing all field bits) is defined as the information detection capability, and these values are compared with the values of conventional tech-
nologies.

Based on the above definition, 2 MB of data can be fully scanned in 5 \( \mu \)s by the FPGA implementation. Therefore, the information detection capacity per chip reaches 400 GB/s. The transfer ability of the fastest memory module is 34.1 GB/s, and even a CPU with thermal design power (TDP) (maximum electric power) of more than 100 W would not be able to achieve the above ability of 400 GB/s. Considering that the power con-
sumption of the FPGA is about 10 W, we see that the per-
formance of the same power consumption is 400 GB/s-chip W, which is phenomenal information detection capability. Al-
though this DBP by FPGAs is small capacity, it has very-
high-speed information detection capacity. Therefore, its utility value is high as a tool to monitor sensor data that require real-
time performance and as the index of data or big data which are accessed intensively in unit time.

② is the estimated implementation of DBPs using the static
random access memory (SRAM) with the field data extended to 1 Kbit in consideration of its versatility. Therefore, very-high-speed information detection is realized by using this type of DBPs in large quantities. ② is the estimated implementation of DBPs using the dynamic random access memory (DRAM). The feature of DRAMs is that its capacity can be improved more than SRAMs, and the newest synchronous dynamic random access memory (SDRAM) has realized random access of approximately 10 ns. The information detection capacity per chip reaches 100 TB/s by incorporating GAPs for DBPs into 1 GB/chip, showing overwhelming superiority to conventional information processing with CPUs and memories. If this performance can be guaranteed, information processing is achieved only by basic data without using the index that has various problems as before, and further speed-up can be expected by using the index. It should be noted that in the case of consisting DBPs with the nonvolatile memory (storage) such as NAND (SSD) memory of (independent of memory capacity) the time required for full scanning 1 Kbit field of 1 TB would be 10 ms. Since the detection time is constant even if full scan is performed using this DBP in large amount, the characteristic of this technology becomes remarkable as the data size is larger. In the case that 1,000 pieces of this SSD are used in parallel, a large-capacity memory of approximately 100 TB would be required for full scanning 1 Kbit field of 1 TB would be 10 ms. Since the detection time is constant even if full scan is performed using this DBP in large amount, the characteristic of this technology becomes remarkable as the data size is larger. In the case that 1,000 pieces of this SSD are used in parallel, a large-capacity memory of 1 PB that corresponds to the human brain is created, and its full scanning time is 10 ms in addition. SSDs are nonvolatile memories and their power consumption at the time of operation is low. Therefore, the integration degree as a device has been improved, which enables downsizing.

As mentioned in subsection 3.1, in the case of using current CPUs or GPUs for data searching, it is necessary to update (maintain) the meta data every time the basic data are changed, revised or added. Further, even partial change in basic data requires extensive maintenance for the meta data. By using the proposed DBPs, the index and maintenance are unnecessary, and persons other than specialists of database are enabled to process information similar to inspiration of a human brain. In this way, the intellectual information processing, which has been difficult to realize so far, is greatly improved.

5. Set Operating Processor (SOP)

5.1 Outline of SOP

The origin of the intelligent information processing is pattern recognition. However, the evolution of the pattern recognition technology is extremely slow. The major cause is that there has not been a definition for information processing of “pattern” until now, we presume. Figure 3 shows the definition of “pattern” for the two-dimensional pattern. The positions of the data for the pattern concerned can be designated as a relative position and therefore the definitions for the pattern are obtained by designating both the positions and the values of the data at the same time. The above-mentioned definition is common for all of the one-dimensional patterns such as character string, two-dimensional patterns such as graphics, three-dimensional patterns such as solid objects and N-dimensional patterns.

As indicated by the definition of the above patterns, the pattern matching can be realized by parallel computation of three factors of the data value, the position of the data, and the operator independently for each pixel. GAPs can be realized by a data magnitude comparator for a data value and address (pixel) swap circuit with, for example, a two-dimensional shift register for data position.

Details of the technique of set operating processors (SOP) based on the above-mentioned definition of pattern are described in reference [3]–[12]. Figure 4 shows a structure of the SOPs which are optimized for processing of stream data including recognition of graphics and character. This example is the 2D-SOP that realizes the recognition of two-dimensional array image data and feature extraction of images. For instance, a video graphics array (VGA) image would consist of 640 pixels in X-axis and 480 pixels in Y-axis. The GAPs within the SOP, which realize the pattern match of image pixel data of Y-X or the detection of edge/area at a pixel level, and memory cells to
memorize pixel information are integrated in one chip. Feature extraction such as a complicated pattern match that takes over 10 s for configuration of general CPUs and memories (pattern match based on ambiguous conditions) is achieved in approximately 5 µs by the proposed 2D-SOP, and therefore it is suited for recognition and detection of stream data. It is possible to utilize SOPs for GAP configurations appropriate to the number of dimensions of the array data such as the 1D-SOP for full text search of text data or the 3D-SOP for analysis of three-dimensional configurations.

5.2 The Possibility of ASIC Implementations of SOP

SOPs realize recognition, reference and matching processing, which require intellectual ambiguity most among the detection of various information and can hardly be performed in real time, at an extremely high speed with extremely low power consumption. The authors have verified various SOPs from one dimension to three dimensions in FPGAs. Since the circuit scale of GAPS is larger than that of DBP, it is difficult to implement a practical level SOP in FPGAs. However, a high-performance SOP can be realized in a practical level by ASICs.

The SOP address swap circuit can transfer the information of the address (pixel) of the entire address (pixel) space not only to the neighborhood but also to an arbitrary address (pixel), so it is equivalent to a hardware implementation of the cellular automaton. It is also possible to realize a high speed and high function automaton by using the function of the SOP address swap circuit. Moreover, it can be applied to the normally off type sensing technology by using silicon-on-thin-buried oxide (SOTB), which is an ultra low power LSI technology.

Required information is extracted directly from given stream data without complicated processing for sensor data and various stream system data. SOPs themselves are intellectual processing such as inspiration of the human brain. Of course SOPs can be used in real time, and the extracted characteristic data can be accumulated and utilized as the database. Collaborating the DBP that detects the accumulation system data at high-speed, and the SOP, makes it possible to develop an extensive database in which images, sounds, text data, etc. are integrated. Also, it is expected to advance the natural language processing, then the intellectual information processing is considerably evolved, and realization of information processings that are close to human being can be expected.

6. Cross Operating Processor (XOP)

6.1 Outline of XOP

Figure 5 shows outline of the structure of the cross operating processor (XOP) which realizes combination comparison operation in super parallel. In this structure, n and m pieces of data are memorized in the X and Y directions, respectively. Comparison operation of the memorized data of X and Y axes is performed in a fully parallel manner \((m \times n)\) in GAPS, and the coordinate to which the results of the comparison operation correspond is output.

6.2 The Possibility of ASIC Implementations of XOP

The current semiconductor technology enables to integrate more than 10 billion transistors in one chip. Examining the structure of memory and computing unit (GAP) from the above-mentioned point of view, the GAP structure can be changed from \(m \times n\) to \(4\times 4\ K = 16\ M\ pieces\). The above result suggests that in the case of comparison operation at 1 ns clock per bit for comparison between 64 bit data, matching of the data for the entire XY space can be performed in 64 ns. The computing unit (AP) of 64 ns/16 M pieces performs comparison operation in 64 ns and therefore it is equivalent to operation of \(4\times 10^{14}\) s \((4\ fs)\) by one computing unit (AP). Considering that the operation performance of the fastest CPU is around 4 T times/second \((4\times 10^{12}\) time/s) at the moment, extremely high-speed combination comparison operation is enabled. Although the use of data rewriting accompanies data writing and overhead of the comparison result output process, the optimized XOP enables combination comparison operation between 1 M data in 4 ms. The data combination comparison operation that the XOP solves can be applied to various combination comparison operation such as statistical analyses on correlations between data and frequency of data appearance, filtering of data and usage as a discriminator. In particular, combination and mining processing of big data and discriminator are expected to be applied to various AI recognition technology.

7. Shortcut to AI Evolution

Various characteristics of structure and information processing of DBPs, SOPs and XOPs have been described above. With the proposed memorism processors, data are collected, processed and accumulated data are being used. That means we have proposed the computing technique that emphasizes the uti-
The CPU and GPU of the von Neumann computer are adopting arithmetic logical unit (ALU) and floating point unit (FPU) for arithmetic operations which are high cost operator and consume much power. The processing ratio of the CPU’s weak processing, which means inefficient processing of the whole information processing, might be equal to or greater than the processing ratio of the CPU’s strong processing, which means efficient processing is necessary.

Therefore, light work that does not include arithmetic operations such as data retrieval, collation, recognition, etc. is useless when using a CPU or GPU, and power performance can be greatly improved by leaving it to the memorism processor. And also to do separately processing good job of CPU, GPU and good job of SOP, DBP, XOP each other is the easiest way for all of information processing.

Today’s memories of computers have extremely large capacity and operate at high-speed (high efficiency), and in addition to calculism that focuses on calculation by conventional CPUs and GPUs, positive utilization of the memorism processors which attach great importance to inflection of data would be the most effective and natural idea as a shortcut to the essential AI evolution.

The followings are the advantages obtained by the use of the memorism processors, which enable self-contained information processing for AI.

1. Since the data structure can be simplified and power saving can be achieved, the system becomes compact and power saving. For a peculiar AI, cut-and-try and optimized tuning can be applied.
2. Extract characteristics of data from big data at ultra-fast speed.
3. Extracted data are easily stored or drawn.
4. The major problems on pattern recognition, which is the base of the recognition technology, are those regarding matching and classification, and the memorism processors are capable of processing both of the above fast.
5. The current learning problem of AI systems is reduced by combining SOPs, DBPs and XOPs.
6. Since the preprocess such as index is unnecessary, the performance of the system such as throughput speed can be predicted beforehand.
7. Every memorism processor is executed by the control software for driving the internal single instruction multiple data (SIMD) type operator GAP. The memorism processors can be used by this control software as standard equipment immediately.

8. Conclusion

Table 2 shows an example of application to a representative AI of the memorism processor. As shown in Figs. 2, 4 and 5, each of the SOP, DBP and XOP has the function that is to be called “new AI”. The processing that is hard to be realized in the conventional information processing becomes possible by combining these processors. In particular, as shown in Fig. 5, it is possible to improve the efficiency of machine learning and realize a system that takes advantage of each other by making cooperative learning by combining memorism processors good at connectionism and pattern matching.

Moreover, as shown in Table 2, when the memorism processor is combined with the natural language processing, the efficiency of extracting knowledge representation data is increased, and the extracted data is freely storing or reading without pre-processing or post-processing can be realized. As above, the computing which complements weak points of the von Neumann computers by the memorism that focuses on the utilization of data deserves to be called “novel von Neumann computer” and it is expected to contribute greatly to the evolution of AI.

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