Improved Circuit Design of Analog Joint Source Channel Coding for Low-power and Low-complexity Wireless Sensors

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Abstract—To enable low-power and low-complexity wireless monitoring, an improved circuit design of Analog Joint Source Channel Coding (AJSCC) is proposed for wireless sensor nodes. This innovative design is based on Analog Divider Blocks (ADB) with tunable spacing between AJSCC levels. The ADB controls the switching between two types of Voltage Controlled Voltage Sources (VCVS). LTSpice simulations were performed to evaluate the performance of the circuit, and the power consumption and circuit complexity of this new ADB-based design were compared with our previous parallel-VCVS design. It is found that this improved circuit design based on ADB outperforms the design based on parallel VCVS for a large number of AJSCC levels (≥16), both in terms of power consumption as well as circuit complexity, thus enabling persistent and higher temporal/spatial resolution environmental sensing.

Keywords—Power Efficiency, Analog Compression, Circuit Complexity, Signal Multiplexing, Environmental Monitoring.

I. INTRODUCTION

Motivation and Background: High temporal/spatial resolution environmental monitoring applications involve deploying a large number of power-efficient and low-complexity/low-cost wireless sensors [1], [2]. Some application scenarios include low-cost, high-confidence monitoring of urban infrastructure [3], intelligent transportation systems [4], wireless health monitoring [5], datacenter monitoring [6], ocean environment monitoring [7]. For such applications, we observe that: i) sensors need to be deployed in a wide area and with high density, hence a large number of disposable low-cost sensors are needed; ii) nearby sensors are clustered and transmit wireless signals to a cluster-head node in separate and multiplexed channels; iii) sensors are expected to be powered by battery or even self-powered and should work for extended periods of time. All these requirements demand low-power, low-cost/complexity designs of the sensor nodes.

State of the Art: Current research efforts to reduce the power consumption of wireless sensors include: i) reducing the power of radio Radio Frequency (RF) components as well as the power of radio transmission; ii) adopting new materials to reduce the power needs of sensing components; iii) adopting energy-harvesting power supplies. To reduce the radio power, a wake-up radio-receiver approach is proposed to save radio power [8]. A transmission adaptive power-control approach is proposed based on wireless link-quality measurement for wireless monitoring sensors [9]. An event-driven approach is described to reduce the power consumption for large-scale wireless monitoring [10]. To reduce the power consumption at the sensing components, a new type of carbon nanotube is proposed for low-power gas sensing [11]. Power circuits for energy harvesting wireless sensors are also proposed [12]. These existing research works address reducing power consumption for digital circuits. The advantage of such digital architecture is that functionalities such as digital data compression, channel coding, and digital modulation (as well as various types of signal processing) can be done in a digital processing chipset. However, the drawback is that Analog-to-Digital-Converter (ADC), Digital-to-Analog Converter (DAC), and digital chipsets are needed, all of which are power-demanding components, resulting in high circuit complexity and high cost. A digital architecture, therefore, tends to yield powerful yet non-disposable and non-persistent wireless sensing motes.

Power Consumption: Digital wireless sensing motes with their microprocessors consume much higher power than our proposed analog circuit. The active microprocessor power consumptions for these sensors (as in [2]) are: 1.1 mW for WSN340, 2.4 mW for Mantaro CoSeN, 6 mW for Telos RevB, and 26.4 mW for MICA2. For our proposed ADB design with 64 AJSCC levels, assuming nano fabrication technology of the analog components, the consumption is found to be 90 µW excluding the RF module, which suggests that the sensor can also be powered without a battery via energy harvesting techniques using solar cell, vibration (piezo electricity), etc. In contrast, the power consumptions of the microprocessor-based digital sensors are at least two orders of magnitude higher than our ADB-based AJSCC circuit design.

Our Approach: To overcome these limitations, we propose new baseband signal compression and processing in all-analog components to replace the ADC, digital chipset, and DAC, therefore achieving power-consumption reduction at the baseband components. This approach does all the processing in the analog domain (without the need for ADC, DAC and digital chipsets), and thus greatly reduces power consumption as well as circuit complexity compared with a digital-based sensor design. In addition, our structure retains some of the key functionalities of the digital system such as signal compression and multiplexing, thus allowing power-efficient transmission of the sensed signals from a large number of all-analog sensors. In particular, the signal-compression functionality is realized...
with innovative circuit designs that realize rectangular-type Analog Joint Source Channel Coding (AJSCC), which is the source compression method proposed by Shannon in his 1949 seminal paper \[13\]. To the authors’ best knowledge, ours is the first all-analog circuit realization of AJSCC, which replaces the digital processing components with a complete analog structure, resulting in low circuit complexity and low power consumption. In this article, we present two analog designs of the rectangular-type AJSCC circuit: i) Design 1—circuit realized by parallel Voltage Controlled Voltage Source (VCVS), which is our previous work \[1\]; ii) Design 2—circuit realized by Analog Divider Blocks (ADB), an improvement over Design 1 in terms of power and cost, which are critical requirements in high-density persistent wireless monitoring solutions. In this work, we are focusing on designing low-power and low-cost encoding circuits (based on rectangular Shannon Mapping) for transmission only. We assume the receiver/cluster head is a resource-rich mote with digital processing units and, as such, the decoding does not need to employ all-analog low-power circuits. Finally, even though we illustrate our design with temperature and humidity signals, it is generalizable to any two analog signals as our design does not pose any restriction on the type of signals as long as they are analog in nature.

Choice of Rectangular-type AJSCC: This choice is motivated by the circuit realization advantage of the rectangular-type AJSCC over the alternate spiral type. Due to the spiral-type’s unique structure, which is very difficult to fit into any of the existing analog circuits, its realizations are based on digital circuits. Specifically, the challenge in designing an all-analog spiral-type AJSCC circuit is to find an analog circuit that can realize the space-filling property of a spiral curve. The inputs of the circuit are two analog signals, and the output should be only one analog signal representing the accumulated length of the curve from the origin to the mapped point in such a way that, at the receiver, the two analog signals can be mapped back by the curve. As this is still an open-research analog design challenge, in this article we focus on the analog circuit realization of rectangular-type mapping.

Sensor Multiplexing: The sensor nodes in the cluster are multiplexed by frequency division multiplexing, i.e., each node occupies a specific frequency band. The nodes are identified by the frequency band assigned at the initial design of the sensing system. Note that there are no digital packets and no digital synchronization designed in the system. The signals from the sensor nodes can be sent periodically with a null period to save transmission power. The receiver/cluster head samples the analog signal and recovers the compressed sensor signal at the frequency band assigned. The reason that the system does not need synchronization is that any sampled signal at a particular time instance contains the two compressed signals at that time instance, and the decoding process is the reverse mapping on the AJSCC curve. sensor multiplexing schemes are also being proposed by us based on frequency position modulation \[14\].

Our Contributions: They can be summarized as follows.

- We propose an improved AJSCC circuit design by Analog Divider Blocks with tunable AJSCC-level spacing;
- We verify the functions of the proposal with LTSpice simulations, and estimate its power consumption;

\[
\begin{align*}
&V_{H0} \\
&0.05 \\
&0.0 \\
&0.75 \\
&0.45 \\
&0.3 \\
&0.15 \\
&0.0 \\
&\sigma V_R \\
&V_{T0}
\end{align*}
\]

Fig. 1: Shannon’s Rectangular Mapping \[13\]. The sensed point is mapped to the point closest on the rectangular curve, and the curve accumulated length from the origin to the mapped point (in bold) is transmitted instead of the two values identifying the 2D sensed point. Here the numbers are the voltages used in our Spice simulations.

- We compare the proposal with previous design to show the lower power and circuit complexity advantages of the improved circuit.

Outline: In Sect. \[II\] we present the principle of rectangular-type AJSCC and its existing circuit realizations. In Sect. \[III\] we review the parallel-VCVS-based Design 1. In Sect. \[IV\] we introduce Design 2, which is based on Analog Divider Blocks, as an improvement over Design 1. Finally, in Sect. \[V\] we draw the conclusions and discuss future directions.

II. AJSCC AND EXISTING CIRCUIT REALIZATIONS

Analog Joint Source Channel Coding (AJSCC) \[15\] can compress two or more sensor signals into one with controlled distortion while also being robust against wireless channel impairments. AJSCC adopts Shannon mapping as its encoding method \[16\]. Such mapping, in which the design of rectangular (parallel) lines can be used for 2:1 compression (Fig. \[1\]), was first introduced by Shannon in his seminal 1949 paper \[13\]. Later work has extended this mapping to a spiral type as well as to N:1 mapping \[17\]. AJSCC achieves optimal performance in rate-distortion ratio, whereas to achieve such optimality using separate source and channel coding complex encoding/decoding and long block-length codes would be required, causing delays and energy inefficiencies. Shannon mapping has the two-fold property of (1) compressing the sources (by means of N:1 mapping) and (2) being robust to wireless channel distortions as the noise only introduces errors along the parallel lines (or the spiral curve).

AJSCC requires simple compression and coding at the transmitter, and low-complexity decoding at the receiver. In rectangular-type mapping, to compress the source signals (“sensing source point”), say Humidity and Temperature voltages \(V_{H}, V_{T}\), the point on the space-filling curve with minimum Euclidean distance from the source point is chosen (“AJSCC mapped point”), as illustrated in Fig. \[1\] via a simple
We had proposed a circuit realization with parallel VCVS in [1]. Here, we review the key design concepts of this parallel-VCVS design so as to prepare the reader for the new and improved AJSCC circuit design, Design 2, in the next section.

**Design Overview:** Our original analog circuit is depicted in Fig. 2. In our all-analog implementation by parallel VCVS, odd-level voltages are generated using Type-1 Voltage Controlled Voltage Sources (VCVS), whereas even-level voltages are generated using Type-2 VCVS. \( V_H \) and \( V_T \) are the humidity and temperature variable voltages, and \( V_{H0} \) and \( V_{T0} \) are the humidity and temperature variable voltages after range adjustment (i.e., offset removal). \( \Delta_H \) is the spacing between the levels and \( V_R \) is the voltage of one parallel line in the mapping curve, which is a constant voltage value. As such, it is chosen to be proportional to the maximum value of \( V_{T0} \) and vice-versa, as shown in Fig. 1.

The VCVS accepts voltages \( V_{T0} \) and \( V_{H0} \) as inputs, and outputs a voltage that is a function of the input voltage. By observing the rectangular-mapping curve (see Fig. 1), there are two types of output increments. In the first (which we call Type 1), the output \( V_O \) increases linearly with increasing \( V_{T0} \), i.e., \( V_{O,Type1} \propto V_T \). This happens when we traverse the curve from left to right on odd-numbered lines to reach the mapped point. In the second (Type 2), the output decreases linearly with increasing \( V_T \), i.e., \( V_{O,Type2} = V_R - V_{O,Type1} \), which corresponds to traversing the curve from right to left on even-numbered lines to reach the mapped point. We realize these two types of outputs using two types of VCVS, where the overall mapping output is the voltage summation of the activated VCVS blocks, which represents the accumulated length of the curve from the origin to the mapped point. Note that \( V_{H0} \) controls which VCVS levels/lines are activated, while \( V_{T0} \) controls the VCVS output. A stack of analog switches is used to implement the former and also to control the output of all levels. The number of switches is determined by the mapping resolution sought \( (\Delta_H) \).

Each parallel line is defined as a level and is numbered from the bottom upward. The first and second levels are combined to be defined as the first stage. The second stage will include the third and fourth levels and so on. The first stage is shown in Fig. 2 where the output of each level is controlled by the corresponding analog switch. Each switch has three inputs: \( V_H + \Delta_H, GND \), and the output of either a Type-1 or Type-2 VCVS. Odd- or even-numbered switches are connected to Type-1 or Type-2 outputs, respectively. Note that the number of activated switches and the activation voltage of each switch are determined by considering both \( V_{H0} \) and the chosen resolution \( \Delta_H \). The switching logic is explained as follows: each switch is activated only if \( V_H \) is greater than a certain value based on the switch’s level in the stack. If not activated, the output of the switch is connected to \( GND \); if activated, the output is equal to the VCVS output within a certain range \( (\Delta_H) \) of \( V_{H0} \) above the activation voltage. Once \( V_{H0} \) exceeds this range, the switch outputs its saturation voltage of \( V_H + \Delta_H \). Even though \( \Delta_H \) is used to calculate the length of the curve from the origin to the mapped point, it does not provide any additional information. Hence the saturation voltage can just be \( V_R \), instead of \( V_R + \Delta_H \). Since neglecting this part of the length of the curve (i.e., \( \Delta_H \)) will not affect the accuracy of the decoded signal and can simplify the mapping, in both simulation and hardware implementation of Design 1 this \( \Delta_H \) gap has been neglected.

The AJSCC mapping circuit has been simulated in LTSpice using manufacturer-provided Spice models to capture real performance; Figure 3a shows the output of the second level over its entire mappable range of \( V_T \) and \( V_H \). It can be seen that the output is almost zero when \( V_H \) is below 1.25 V and that, when \( 1.25 < V_H \leq 1.55 \), Type 1 mainly drives the output (with zero contribution from Type 2); conversely, when \( 1.55 < V_H \leq 1.85 \), Type 2 mainly drives the output (with \( V_R \) contribution from Type 1); finally, when \( V_H > 1.85 \), the output is \( 2V_R \) (i.e., \( V_R \) from each VCVS). The detailed information on the LTSpice simulation results can be found in [1].
**SDR vs. CSNR Results:** The proposed system has been implemented in a prototype composed of multiple sensor nodes and one cluster head node. The sensor nodes are multiplexed by frequency multiplexing on adjacent and separated channels. The two sensing signals are first compressed by the AJSCC circuit, then modulated using frequency modulation by a Radio Frequency Integrated Circuit (RFIC), then sent to the antenna, all realized on a PCB. At the receiver, the signal is digitally sampled, and then frequency-demodulated and AJSCC-decoded to recover the original signals. Figure 3 compares the Signal-to-Distortion Ratio versus Channel Signal-to-Noise Ratio (SDR-vs-CSNR) performance of one, two, and three analog sensors communicating to a digital cluster head using different channels showing the effect of receiver diversity. We clearly observe that the three-sensor case has better performance than the two-sensor case, which in turn is far better than the single-sensor case thanks to channel diversity at the receiver. For further details, interested readers can refer to [2].

**Optimum Number of AJSCC Levels:** We note an interesting tradeoff on the number of AJSCC levels used. With increasing number of levels, $n$, the Mean Square Error (MSE) of $V_H$ drops as the spacing between the lines ($\Delta_H$) reduces. However, since the total encoded voltage cannot be arbitrarily high (as it is limited by the supply voltage), the voltage representing $V_T$ will be smaller, which will increase the MSE for $V_T$. On the other hand, with decreasing $n$, the quantization error in $V_H$ increases, leading to high MSE for $V_H$. We have thoroughly studied this tradeoff via MATLAB simulations and found an optimal $n = 73$, as in Fig. 3c (for further details refer to Sect. III-C of [2]). We note that the optimum number of levels (for minimum MSE) is a large number (around 73), which is difficult to implement using Design 1 (in terms of both power and cost). We observe from Fig. 3c that in increasing from 11 levels (as in Design 1) to 64 levels (feasible with Design 2), the signal recovery MSE is reduced dramatically by an order of magnitude for the three SNR values evaluated. This presents compelling motivation to develop Design 2, which can support a large number of levels and achieve optimality.

**IV. IMPROVED DESIGN WITH MULTISTAGE ANALOG DIVIDER BLOCK (DESIGN 2)**

The circuit in our previous work grows linearly in complexity with the number of levels, $n$ (but exponentially with the number of components used), which is not desirable for low-power sensing at a large number of levels. Thus, developing a method with better than $O(n)$ linear complexity would lower power consumption for large $n$. Hence, in Design 2, we aim...
at achieving $O(\ln(n))$ complexity (or linear in the number of components used). In the following content, we firstly describe the design methodology of Design 2; then present the circuit design and LTSpice simulation results. The power consumption of Design 2 is elaborated and, finally, power and cost comparisons with Design 1 are presented.

**Design Methodology:** In this improved second design, we propose to shift the parallel lines in Fig. 1 upward by half $\Delta_H$, as shown in Fig. 4 for the implementation of the proposed design. The new mapping offsets all of the levels by $V_{H0} = \Delta H$ and removes the highest level. This mapping makes the circuit more efficient as it removes the asymmetry in the first level (i.e., the mapping range from $V_H = -0.15$ to 0 V is not available in the example shown in Fig. 1 unlike other levels, as we consider only positive sensor values). With this background, the improved circuit to realize the AJSCC mapping with arbitrary $\Delta_H$ is shown in Fig. 5. The input voltage $V_H$ is firstly divided by a tunable voltage of $\Delta_H$ — the desired spacing between the ASJCC levels. The voltage divider outputs the integer part of the division, and this integer is input to two blocks, the first is the Odd/Even block and the second is the Analog Multiplier block, where the former will determine if the input integer is odd or even, whereas the latter will multiply the integer with voltage $V_T$. The Analog division and Odd/Even block are combinedly realized using multistage Analog Divider Block (ADB), as explained below.

**Circuit Implementation:** In the following multi-stage ADB circuit, the term “stage” refers to an analog divider block, and parameter $k$ denotes the number of such stages. (Note that usage of “stage” here is different than in Design 1.) A circuit with $k$ stages results in $n = 2^k$ levels, and Fig. 6 shows the proposed circuit for $k = 4$, corresponding to 16 levels. This design uses VCVS output to generate each level as in the previous circuit, but differs in how a sensed point is mapped to a particular level and as well as on what VCVS type is chosen for that level. Instead of using comparators between every individual level, the proposed circuit identifies the appropriate level number by dividing $V_H$ by $\Delta_H$ using the multi-stage ADB. The resulting quotient is input in bits and the smallest bit is used to determine whether to use Type-1 or Type-2 VCVS. The quotient bits are converted back to
voltage using comparators and a summing amplifier. Note that this is done solely in the analog domain, without the use of any power-hungry ADCs. The circuit can be configured to have any number of stages, $k$, depending on the resolution requirements of the application. In the rectangular mapping used for this circuit, each subsequent level uses the opposite VCVS from the previous level. The result is that all odd-numbered levels use the Type-1 VCVS while even-numbered levels use the Type-2 VCVS. Thus, the problem of selecting which VCVS to use reduces to determining if the level is odd or even, removing the need to have the linear cascade design as in Design 1.

A simple way to determine parity is to use the modulo operation. For example, to determine if an integer $M$ is even or odd, $M$ mod 2 results in either 0 if $M$ is even, or 1 if $M$ is odd. If $M$ is a real number instead of an integer, it cannot directly be classified as even or odd. However, the parity of $\lfloor M \rfloor$ can still be found from $M$ mod 2, whose result will be a real number ranging in $[0, 2)$. If the result is within the range $[0, 1)$, then $\lfloor M \rfloor$ is even; if it is within $[1, 2)$, $\lfloor M \rfloor$ is odd. To apply this concept to the circuit, we calculate $V_{in}$ mod by $\Delta_H$. If the result of this expression falls within the range $[0, \frac{\Delta_H}{2})$, then it belongs to an odd level, whereas if it is within $[\frac{\Delta_H}{2}, \Delta_H)$ it belongs to an even level. One way to perform the modulo operation in analog is to use a multi-stage analog divider [21]. The analog divider can find modulo of one voltage by a second voltage within a predefined range. Figure 7a shows one stage of the analog divider, which performs $V_{in}$ mod $V_{REF}$ where the input voltage, $V_{in}$ falls within $[-V_{REF}, V_{REF}]$ and $V_{REF}$ is a reference voltage in the modulo circuit which is chosen to determine both the modulo divisor and the input voltage range. Figure 7b shows this stage implemented in LTSpice. Cascading $k$ such stages yields $V_{in}$ modulo by $\frac{V_{REF}}{2^k}$, with the same input range $[-V_{REF}, V_{REF}]$, and $\Delta_H = \frac{V_{REF}}{2^k}$. In this design, to create the discontinuity around the $y$-axis, a comparator checks the input voltage and outputs an offset of $V_{REF}$ if the input is negative. This offset is added to the input voltage at a summing amplifier, which also adds another offset of $-\frac{\Delta_H}{2}$ to center the output about the $x$-axis. This is useful since the operating region of the Op Amp used in the summing amplifier is also centered around the $x$-axis. The sum is multiplied by 2 to get the final output, called the residue of the stage. Eq. (1) shows the output $V_o$ of the stage,

$$V_o = \begin{cases} 2 \times \left( V_{in} - \frac{V_{REF}}{2^k} + V_{REF} \right) & V_{in} < 0, \\ 2 \times \left( V_{in} - \frac{V_{REF}}{2^k} \right) & V_{in} \geq 0. \end{cases} \tag{1}$$

A cascade of analog divider stages can generate the binary equivalent of the quotient, as shown in Fig. 7c. If the output voltage for a stage is positive, this represents a 1 bit; whereas, if the output voltage is negative, it represents a 0 bit. The comparators are used to check whether the previous output is positive or negative by outputting low if it is a 1 bit and high if it is a 0 bit. Cascading $k$ stages gives a string of $k$ bits, with the most significant bit at the first stage in the cascade and the least significant bit at the final stage. The value of this binary code corresponds to the mapped level in the rectangular mapping. Cascading $k$ stages results in up to $2^k$ levels, with $\Delta_H = \frac{V_{REF}}{2^k}$, Table I shows how the number of levels and $\Delta_H$ scale with $k$. For each $k$ (i.e., corresponding hardware), it shows the minimum and maximum values of levels, $V_{REF}$, and $\Delta_H$ supported by the circuit. As the table shows, adding levels increases the complexity by log$_2(k)$, which is better than $k$ of the previous circuit. Note that the number of stages cannot be modified after circuit fabrication.

After the analog divider, there are a few steps before calculating the final quotient voltage. First, the bits need to be converted into a voltage representing the number of levels. To do this, the circuit uses comparators to act as switches to convert each bit to a voltage of either $V_R$ or ground. Then, a summing amplifier (with gains corresponding to the respective powers of 2) calculates the total voltage. Now, we need to add

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**TABLE I: $V_{REF}$, $\Delta_H$, and $V_R$ for up to $k = 8$ analog divider stages; all voltages are in Volts.**

| $k$ | Max $n$ | Min $V_{REF}$ | Min $\Delta_H$ | Min $n$ | Max $V_{REF}$ | Max $\Delta_H$ | $V_R$ |
|-----|---------|---------------|----------------|---------|---------------|----------------|-------|
| 1   | 2       | 6             | 3              | -       | -             | -              | 2.5   |
| 2   | 4       | 4             | 1              | 4       | 4             | 1              | 1.25  |
| 3   | 16      | 3.429         | 0.429          | 6       | 4.8           | 0.6            | 0.625 |
| 4   | 16      | 3.2           | 0.2            | 11      | 4.8           | 0.1            | 0.3125|
| 5   | 32      | 0.979         | 0.097          | 21      | 4.8           | 0.15           | 0.1563|
| 6   | 64      | 0.048         | 0.048          | 40      | 4.923         | 0.077          | 0.0781|
| 7   | 128     | 0.024         | 0.024          | 78      | 4.987         | 0.039          | 0.0391|
| 8   | 256     | 0.012         | 0.012          | 155     | 4.987         | 0.019          | 0.0195|

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this voltage to one of the VCVS voltages. Both Type-1 and Type-2 VCVS have a comparator at their outputs. If the last bit of the analog divider is 0 (i.e., quotient is even), then Type-1 VCVS voltage is added and vice-versa. Although the number of stages cannot be adjusted, $\Delta H$ (and, thus, the number of levels) can be altered through changing $V_{REF}$. $V_{REF}$ has a minimum of 3 V since the input $V_{H0}$ reaches up to 3 V and a maximum of 4.5 V due to saturation at the Op Amp. This allows increasing $\Delta H$ up to 50% from the minimum, which is a decrease in levels up to 33%. If the number of levels is decreased, $V_R$ can be increased if desired to keep $V_R \times 2^k$ approximately $V_{DD}$, although it is not required. To make $V_R$ adjustable, however, we need to calculate $V_R = \frac{V_{DD}}{2^k}$, which will require three more Op Amps. To save on power consumption, the proposed circuit keeps $V_R$ constant.

**LTSpice Simulation:** Fig. 8a shows LTSpice simulation output of the circuit’s output voltage (AJSCC encoded voltage) for all possible values of $V_H$ while fixing $V_T$ at 2.5 V so that the mapped point will always be at the center of each level. This plot is generated using $LTC1047$ for the Op Amps and $LTC1441$ for the Comparators instead of $LM324$ and $LP2901$, the respective components used in Design 1. These parts are chosen to ensure that the output voltage does not saturate before reaching $V_{DD}$. The figure shows all the 16 levels possible with $k = 4$ and matches the expectations of the circuit. The simulation for one stage of ADB is shown in Fig. 8b. Here, $V_{in}$ and $V_{out}$ are shown to be consistent with Fig. 7. Fig. 8b also shows $V_{comp}$, the bit output from the stage’s comparator. $V_{comp}$ represents the modulo quotient of the stage. Note that $V_{comp}$ is high when $V_{in}$ is negative and vice-versa. $V_{out}$ and $V_{comp}$ are both very linear which is important to ensure that circuit calculates the correct level. All other parts of the circuit are (nearly) linear with respect to the input voltages, $V_{H0}$, $V_T0$, largely due to the use of Op Amps.

**Power Consumption:** Fig. 8c shows the simulated power consumption for different numbers of levels of the ADB circuit with $V_{REF} = 3$ V and $V_{DD} = 5$ V. The circuit here used the same Op Amp $LM324$ and Comparator $LP2901$ as in the parallel VCVS circuit for comparison purposes. At $k = 4$ stages/16 levels, the ADB circuit requires 21.66 mW, whereas the parallel VCVS circuit requires 22.72 mW, which is nearly the same power. For fewer levels, the parallel VCVS circuit is more efficient in power used per level. For the case of designs with $\geq 16$ levels, the ADB-based design is much more (exponentially) power efficient than the parallel VCVS design (see Fig. 8c), e.g., for 128 levels, the power consumption per level of the ADB design is 0.252 mW, whereas that of parallel VCVS design is 1.215 mW which is 5× more. Table II shows the percentages of power consumption of a 16-level ADB circuit broken down by subcircuits as labeled in Fig. 6. The ADB subcircuit is the most power consuming block, while the bits to voltage converter is the second most. The analog divider is the only subcircuit to significantly increase in power as more stages are added, while the power consumption of the remaining subcircuits remains virtually constant. Hence, in future designs, the ADB subcircuit needs to be made more power efficient. It is worth noting that more power-efficient COTS components can be used to further lower the power consumption. Figure 8c also shows (as “Efficient ADB”) the power consumption after swapping the Op Amps and Comparators to more power-efficient ones. Here, $LTC1047$ is used for the Op Amp and $LTC1441$ is used for the Comparator. With these efficient components, the ADB circuit consumes 4.8 mW for 16 levels.

**Cost/Component/Complexity Comparison:** In order to compare the cost of fabrication/complexity of circuit, the number of components are compared in both designs, as shown in Table III. For the ADB-based design, the number of Op Amps, high power Comparators, low power Comparators, and the Resistors are counted. For the parallel-VCVS design, the

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**Fig. 8:** (a) AJSCC encoded output of 16-level analog divider circuit with varying $V_H$ and $V_T = 2.5$ V and $V_{REF} = 3$ V; (b) Output of one-stage analog divider circuit with $V_{in}$ ranging from $-3$ to $3$ V, with $V_{REF} = 3$ V; (c) Power (blue, left y-axis) and Power-per-level (red, right y-axis) consumed by the ADB design, parallel VCVS design, and ADB design with power efficient COTS components.

**TABLE II:** Power consumption in each module of circuit with non-power efficient components, $k = 4$; all values are in mW.

| Subcircuit                          | Power [mW] | % of Total |
|-------------------------------------|------------|------------|
| Analog divider                      | 14.710     | 67.93%     |
| $V_T$ Offset                        | 0.835      | 3.95%      |
| VCVS Type 1                         | 0.963      | 4.45%      |
| VCVS Type Selector                  | 0.002      | 0.01%      |
| Bits to Voltage Converter           | 3.396      | 15.68%     |
| Final Adder                         | 0.834      | 3.85%      |
| $V_H$ Buffer                        | 0.307      | 1.44%      |
| Total Circuit                       | 21.660     | 100%       |
number of Op Amps, Comparators, Multiplexers, and Resistors are counted. From Table III, we can observe that, with the increasing number of stages, the number of components grows linearly for the ADB-based design with respect to \( k \), the logarithmic value of number of stages. In contrast, the number of components grows exponentially for the parallel-VCCS design with respect to \( k \). This is the case for all of the components. For example, by comparing 32 vs. 64 vs. 128 levels, it can be observed that, for the ADB-based design, the number of Comparators and Resistors increases linearly for each step; however, for parallel VCCS-based design, the number of Comparators, Multiplexers, and Resistors doubles for each step. This observation indicates that the analog-divider-based design has much lower circuit complexity and hence cost than parallel-VCCS based design.

**Nanometer Design Power Consumption:** An estimate of the power consumption of our circuit when it is fabricated using the latest nanometer Silicon technology can be made as follows (for the sake of illustration, we will consider 64 levels; a similar analysis can be done for other number of levels too). Based on Table III, our ADB-based circuit in total has 11 Op Amps, 14 Comparators and 65 Resistors, where Op Amps are clearly the major contributors to the overall power consumption. Using the same nano-designs we considered for these components in [1] (8 \( \mu W \) for Op Amp and 12.7 \( nW \) for comparator), the power consumption of the circuit (\( k = 6 \)) can be estimated as 90 \( \mu W \). In contrast, for Design 1 with 11 levels, the estimated power consumption is 130 \( \mu W \).

### V. Conclusions

A low-power and low-complexity/cost all-analog circuit is proposed for the realization of rectangular Analog Joint Source Channel Coding (AJSCC) mapping. The design, which allows tunable spacing between AJSCC levels, is based on Analog Divider Blocks (ADB) and enables inexpensive realizations of wireless sensor nodes for real-time, high temporal/spatial resolution persistent monitoring of urban infrastructure, transportation systems, and precision agriculture, just to name a few applications. Compared with our previous design using parallel Voltage Controlled Voltage Source (VCVS), this new design based on ADB has a much lower circuit complexity.

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