An interleaved ZVS ultra-large gain converter for sustainable energy systems applications

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Abstract
This paper proposes an interleaved zero-voltage switching (ZVS) ultra-large gain converter. By implementing coupled-inductor (CI) and built-in transformer (BIT) together with a switched capacitor (SC) voltage multiplier cell (VMC), a higher degree of flexibility is achieved for improvement of step-up voltage gain in comparison with those in which only one of these magnetic devices is utilised. Furthermore, the imposed voltage across the semiconductors is reduced by adjusting the turns ratio of the implemented CI and BIT. To further improve the efficiency, semiconductor devices with low ON-state resistance can be used. Moreover, to ensure ZVS turn-on, active clamp circuits are located in parallel with the main MOSFETs, which realize ZVS for all MOSFETs during an entire switching cycle. Minimizing the input current ripple as well as attenuating the reverse recovery problem of the diodes are the other advantages of this converter. Therefore, the proposed converter is a suitable candidate for those applications requiring high step-up gain and high conversion efficiency, such as renewable energy systems. To validate the performance of the proposed converter, a 600 W prototype with 22–380 V voltage conversion is designed, fabricated, and tested. Experimental results confirm that the proposed converter outperforms the previously presented ones in terms of the voltage gain and efficiency.

1 | INTRODUCTION

Renewable energy sources such as photovoltaic (PV) and fuel cell (FC) stack systems have become the most popular types of electricity generation worldwide. However, the output voltage of PV panels and FC stacks is relatively less than the amount required to power local loads and electrical utility. Typically, when a large duty ratio is applied to obtain the high output voltage for DC-DC boost converters, yields such problems as supremely narrow turn-off interval, high peak current, in addition to considerable conduction and switching losses [1].

Switched capacitor (SC) and switched inductor (SI) voltage multiplier cells (VMCs) are well known circuit to extend voltage gain [2–6]. The proposed converter in [4] successfully integrates the SC cells in to a voltage lift circuit to improve voltage gain. However, in the generalized structures, the voltage and current rating of the utilized components in each cell differs with the other cells which makes the design relatively complex. This issue has been discussed and solved in [5] by utilizing of Cock-Croft Walton VMCs. To achieve high voltage gains, the number of VMCs should be increased which increases cost, complexity and current spikes as well. A fourth-order simple common source-load ground structures to increase the operability and power density, low components stress and no sudden changings on capacitors voltage to prevent the instantaneous overcurrent phenomenon has been proposed in [7]. In this case the introduced buck-boost converter achieves high step-up conversion ratio in boost mode. However, due to cascaded power processing stages and utilizing of two power switches, the conversion efficiency is deteriorated. Quadratic converters [8, 9] converters can achieve higher voltage gains at lower duty cycles whereas the input current ripple is low. Although, the voltage step-up ratio is enhanced in these converters; however, the common source-load ground is lost in [8] and due to utilization of the diodes at high current side, the conduction losses is increased. A single-switch high step-up Zeta converter has been introduced in [10]...
based on the combination of basic Zeta converter and corresponding coat circuit. By implementing of the coat circuit, not only higher voltage gain is achieved, but also the voltage stress across the semiconductors is decreased. However, the main disadvantages of the zeta based step-up converters is the pulsating input current arising from the series connection of the power switch with the input power source. The Z-source converter utilizes a network of diode-capacitor-inductor between the input power source and the main switch [11, 12]. The voltage gain is improved at the expense of limiting the duty cycle. Moreover, in the Z-source converter just like the quadratic ones, the conversion efficiency is deteriorated by implementing of the diodes at high current side.

Although, the transformer-less converters of [2–12] are low cost and easy to implement; however, the only freedom to extend the voltage gain is the duty cycle. Moreover, high transient current and high current spikes are imposed across the active and passive components which leads to considerable conduction losses. Coupled inductors (CIs) are other potential approaches to achieve high step-up voltage gain in the boost converter [13, 14] and also in buck-boost converter in step-up mode [15]. The turns ratio is increased to increase voltage gain without a large duty cycle and the voltage stress across MOSFETs is decreased, as well. In such types of step-up converters passive clamp technique is utilized to recycle the energy of the leakage inductance of the CI and to suppress the high voltage spikes. Meanwhile, the leakage inductances of the CIs, provide zero current switching (ZCS) turn-on for MOSFETs and control the falling current rate of the diodes and the reverse recovery problem is alleviated. This concept is applied to the quadratic [16] and Z-source [17] converters to extend voltage gain. However, the main disadvantages of these types of converters mentioned earlier still exist. To reach higher step-up voltage gain along with lower transient current, CIs are typically implemented with SCs circuits [18–20].

To decrease the current stress of the main switches some researches have proposed multiple switches converters with switched-inductors [21, 22] and switched-coupled inductors [23, 24]. The switches are turned ON and OFF simultaneously to charge the magnetic devices. Although the current stress of the MOSFETs is decreased in these schemes; however, implementation of two gate drive circuits increases the total cost and the main problems of the single switch converters such as high input current ripple and low conversion efficiency at high output power levels still exists.

The input current ripple of single-phase boost converters is rather large, which reduces the service life of PV panels as well as the input electrolytic capacitor. To share the input current in each phase and minimizing the input current ripple, interleaved boost converters (CIBCs) have been introduced, where low step-up voltage gain remains as their common problem. The interleaved converters not only promise the low input current but also it offers higher conversion efficiency at higher output powers due to thermal losses distribution. There are many interleaved approaches that have been developed SI and SC VMCs to rectify this problem and achieve high step-up voltage gain [25–29]. The introduced converter in [25] utilizes active SI and SC to increase the voltage gain. The MOSFETs are switched ON and OFF, simultaneously. However, the input current is pulsating and the common source-load ground is lost which arises safety problems and passing of PV leakage current through the circuit. The two-phase [26, 27] and three-phase [28, 29] SC based interleaved converters achieve high voltage gain while maintaining the low input current ripple and common source-load ground.

Three winding CIs along with VMCs are utilized in [30–32] to extend the voltage gain. The primary windings of the CIs act as the input filter inductor in CIBC. The secondary is inserted at the same phase as well as the primary winding. To enhance the voltage gain and current sharing performance, the third winding is inserted at the other phase. To handle higher amount of power with maintaining the efficiency at high levels, a modular CI assisted converter has been proposed in [33]. However, the input current is not shared equally between the phases of an individual module. To further extend the voltage gain, the secondary windings of the CIs are inserted in series to each other in a voltage doubler which its output is connected directly to the output stacked capacitors [34]. Two sets of VMCs are implemented in [35] to obtain high voltage gain in which one of them is mixed with the secondary windings of the CIs. Unfortunately, the input current is not shared between the two phases equally that is a common disadvantage of the introduced converters in [36]. By implementing of CIs and voltage quadrupler, the converter of [37] achieves high voltage gain at the expense of losing common source-load ground. An interleaved input-parallel and output series converter with high voltage gain is introduced in [38]. However, too many components are needed to extend the voltage gain. The converters of [39, 40] share a common CI based VMC between the two interleaved phases and utilizes a voltage lift circuit. In this case high voltage gain is achieved with low number of components and also the input current is shared equally between the phases. The introduced converter in [41] obtains high step-up voltage gain by using two CIs and two VMCs. This topology utilizes the interleaved boost converter in the input side, and the input current is shared with low ripple. On the other hand, a VMC with the secondary windings of the coupled inductors is employed in the output side to achieve the interleaved energy storage. Hybrid series-parallel connection of the VMCs has been introduced in [42, 43] to improve voltage gain. However, the common source-load ground is lost in these types of converters.

Built-in transformer (BIT) can be implemented to extend the voltage conversion ratio [44, 45]. Due to the zero-average current through the primary winding of the BIT, the RMS current is considerably decreased which enables the designer to utilize cores with lower sizes. Moreover, the core saturation is inherently avoided even with in the small cores.

To further increase the voltage gain, the CI and BIT are simultaneously implemented in the converters of [46–48]. In such a case, an extra degree of freedom is obtained for voltage boosting in comparison with those that utilizes one of these magnetic devices. The turns ratio of the CI and BIT together decrease the voltage stress across the MOSFETs, Hence, low voltage rated devices with low cost and low ON-state resistance
can be selected that decreases the conduction losses, considerably.

Although the ZCS turn-ON is provided for MOSFETs through the leakage inductances of CI and/or BIT; however, this can not minimize the turn-ON losses. At higher switching frequency in which the size of the components is considerably decreased, the zero voltage switching (ZVS) is a promising solution to reduce the switching losses [49–60] that can be achieved by an active clam rather than passive clamp in [30–48]. The active clamp scheme is introduced to satisfy ZVS performance for the main and auxiliary MOSFETs in an interleaved transformerless converter with Dickson VMCs [49]. Here, to provide the required resonance to discharge the parasitic capacitors of the MOSFET, auxiliary inductors are embedded within the SC VMCs. However, additional cores are needed and also too many components should be implemented to increase voltage gain. In the contrary, the leakage inductances of CI or BIT in the converters of [50–60] acts the role of that auxiliary inductors in [49]. Generally, the active clamp consists of a clamp capacitor and an auxiliary MOSFET that is simply connected across the main switch [50–55, 59, 60]. An active clamp cell consisting of a CI, an auxiliary MOSFET, four diodes and one capacitor is introduced to the converter of [30] to achieve soft switching performance for the main switches in whole switching transition [56]. It is seen that in the proposed concept, the voltage gain is considerably increased even with a lower winding for BIT. Moreover, ZVS performance is achieved for the MOSFETs through whole switching transition. Altogether, through the extensive analysis and conducted performance comparison later in the paper, it is proved that the proposed converter has the following advantages:

- Ultra-large voltage gain is provided.
- Low voltage stress across the MOSFETs and diodes.
- ZVS performance of the MOSFETs is realized through whole switching transition.
- Reverse recovery problems of the diodes are alleviated.
- High efficiency is achieved following to the abovementioned merits.

2 | PROPOSED CONVERTER AND OPERATING PRINCIPLE

The circuit schematic of the proposed high step-up voltage gain converter consisting of two sets of CIs, a BIT and a SC VMC is illustrated in Figure 2. To provide ZVS operation, two sets of active clamps are employed as well. The reflected leakage inductances of the CIs from the secondary to the primary side are symbolized by $L_{l,k1}$ and $L_{l,k2}$. The magnetizing inductances of the CIs are represented by $L_{m1}$ and $L_{m2}$. The overall reflected leakage inductance of the BIT is denoted by $L_{L,BIT}$. $S_1$ and $S_2$ are the main MOSFETs; $S_{c1}$ and $S_{c2}$ are the active clamp MOSFETs;
Figure 3 Key waveforms of the proposed converter

$C_{cl}$ and $C_{c2}$ are the clamp capacitors; $C_{s1}$ and $C_{s2}$ are the parallel capacitors; $C_{m1}$ and $C_{m2}$ are the multiplier capacitors; $C_{o1}$, $C_{o2}$, and $C_{o3}$ are the output capacitors; $D_{r1}$ and $D_{r2}$ demonstrate the regenerative diodes; $D_{f1}$ and $D_{f2}$ are the output diodes for forward-flyback operation and $R_{out}$ represents the load resistance. The turns ratio of the CI1s is given by $n = n_{s1}/n_{p1} = n_{s2}/n_{p2}$ and turns ratio of the BIT is defined as $N = N_s/N_p$.

The main waveforms of proposed converter are plotted in Figure 3. There are eighteen basic operation stages during one switching mode. As the configuration of the proposed converter is symmetric, only nine modes are analysed in detail and the corresponding equivalent circuits of each switching interval are indicated in Figures 4 and 5. Although, because of limitations on the number of figures, the mode IX figure not drawn.

Mode I $[t_0, t_1]$ (Figure 4(a)): During this time interval, just the MOSFETs $S_1$ and $S_2$ are in ON state. The magnetizing

Figure 4 Operational modes of the proposed converter during half switching cycle, (a) Mode I $[t_0, t_1]$, (b) Mode II $[t_1, t_2]$, (c) Mode III $[t_2, t_3]$, and (d) Mode IV $[t_3, t_4]$
inductances of the coupled-inductors $L_{m1}$ and $L_{m2}$ are directly proportional to the input voltage and are changed by it linearly. The output load is supplied through the capacitors $C_{o1}$, $C_{o2}$, and $C_{o3}$. The current passing through the leakage inductances $L_{L,k1}$ and $L_{L,k2}$ is given by:

$$i_{L,k1}(t) = i_{L,k1}(t_0) + \frac{V_{in}}{L_{L,k1} + L_{m1}}(t - t_0)$$

$$i_{L,k2}(t) = i_{L,k2}(t_0) + \frac{V_{in}}{L_{L,k2} + L_{m2}}(t - t_0)$$

Mode II $[t_1, t_2]$ (Figure 4(b)): At time $t_1$, thanks to the parallel capacitor $C_{s1}$, the MOSFET $S_1$ is turned OFF with ZVS and the current of the magnetizing inductance $L_{m1}$ flows through $C_{s1}$. The drain-source voltage of $S_1$ can be written as:

$$V_{DS1}(t) = V_{Cs1}(t) = i_{Lm1}(t_1)C_{s1}(t - t_1)$$

Mode III $[t_2, t_3]$ (Figure 4(c)): At time $t_2$, the voltage across the capacitor $C_{s1}$ reaches the value on the clamp capacitor $C_{c1}$ and turns the anti-parallel diode of $S_1$ ON. Since the capacitor $C_{s1}$ is much smaller than $C_{c1}$, the current passing through the magnetizing inductance $L_{m1}$ flows through $C_{c1}$. As a result, the voltage stress across the MOSFET $S_1$ is successfully clamped to the $C_{c1}$ voltage:

$$V_{DS1}(t) = V_{c1}(t) = \frac{i_{Lm1}(t_2)}{C_{c1}}(t - t_2)$$

Mode IV $[t_3, t_4]$ (Figure 4(d)): At time $t_3$, $V_{DS1}$ reaches the point that makes $D_{b1}$, $D_{b2}$ and $D_{f1}$ start conducting. By ignoring the voltage across $L_{L,k1}$, $L_{L,k2}$, $L_{L,kb}$ the applied voltage across the primary winding of the BIT is equal to the sum of $V_{c1}$ and the voltage of the secondary side of the CI's. The primary side of BIT charges $C_{m2}$ via $D_{b2}$. The output capacitor voltage $V_{c2}$ is equal to the sum of the $V_{wm1}$, the primary voltage of BIT ($V_{np}$), and the secondary voltage of the CI ($V_{ns1}$). Finally, the output voltage $V_{os1}$ is equal to the sum of the all output capacitors voltages. The stored energy in $L_{m1}$ and $C_{m1}$ is transferred to $C_{f1}$ and $R_{out}$ through $D_{b1}$. The voltage of the secondary side of BIT charges $C_{c3}$ by means of diode $D_{f1}$. The current passing through $S_2$ in this time interval is expressed as:

$$i_{S2}(t) = i_{L,k2}(t) + N_i D_{f1}(t) + i_{D2}(t)$$

Mode V $[t_4, t_5]$ (Figure 5(a)): At time $t_4$, turn-ON gate pulse is applied to $S_1$. Thanks to the antiparallel diode, this MOSFET is turned ON with ZVS.

Mode VI $[t_5, t_6]$ (Figure 5(b)): At time $t_5$, the parallel capacitors $C_{ci}$ and $C_{c1}$ make $S_1$ turned-OFF with ZVS. A resonant circuit is created consisting of $L_{L,kb}$, $L_{L,k1}$, $L_{L,k2}$, $C_{ci}$, $C_{m1}$, and $C_{m2}$. The capacitor $C_{ci}$ begins to be discharged until its voltage reaches to zero at $t_6$.  

![FIGURE 5](image-url) Rest of operational modes of the proposed converter during half switching cycle, (a) Mode V $[t_4, t_5]$, and (b) Mode VI $[t_5, t_6]$, (c) Mode VII $[t_6, t_7]$, (d) Mode VIII $[t_7, t_8]$
Mode VII \([t_6, t_7]\) (Figure 5(c)): At time \(t_6\), the voltage across \(C_{bf}\) reaches to zero. Then, the anti-parallel diode of the main switch \(S_7\) is turned ON. The current falling rates of the diodes \(D_{r2}, D_{b1}\) and \(D_{b2}\) are controlled by the leakage inductances of the magnetic devices. The following equations are held during this time interval:

\[
i_{L,k1} = i_{L,k1}(t_0) + \frac{V_{Ca1} - V_{Ca1} + NV_{in}}{nL_{t,k1}} (t - t_0)
\]

\[
Ni_{D2} = i_{L,kb}(t_0) - \frac{V_{Ca3}}{NIL_{t,kb}} (t - t_0)
\]

\[
\frac{di_{D2}}{dt} = \frac{V_{Ca3} - 2V_{Ca3} + V_{in} + V_{Ca3}}{n^2L_{t,k}}
\]

Mode VIII \([t_7, t_8]\) (Figure 5(d)): At time \(t_7\), the turn-OFF gate pulse is applied to the MOSFET \(S_7\). The antiparallel diode makes \(S_7\) turned-OFF with ZVS. The current passing through \(L_{t,kb}\) reduces and \(D_{b1}\) and \(D_{b2}\) currents linearly decreases to zero. At \(t_8\), the diodes \(D_{r2}\) and \(D_{b1}\) currents reach to zero. At the end of this time interval, \(D_{r2}\) and \(D_{b1}\) are turned OFF with ZCS and their reverse recovery problem is attenuated.

\[
\frac{di_{D1}}{dt} = \frac{V_{Ca3}}{NIL_{t,kb}}
\]

Mode IX \([t_8, t_9]\): At time \(t_8\), the diodes \(D_{r2}\) and \(D_{b2}\) turned OFF with ZCS. During this time interval, the current flowing through \(L_{t,kb}\) continues to decrease to zero. At \(t_9\), the diode \(D_{b2}\) is turned OFF. As mentioned earlier, because of limitations on the number of subfigures, the figure of this mode is not shown.

As mentioned earlier, because of the symmetrical configuration of the proposed converter, there are similar operating modes for the remaining switching cycles.

3 | STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

As the configuration of the proposed converter is symmetric, it is sensible to assume \(L_{c1} = L_{v11} = L_{v12}, C_{c} = C_{v1} = C_{v2},\) and \(C_{c} = C_{v1} = C_{v2}.\) The leakage inductances of BIT and CI are regarded zero. In addition, the capacitors are large enough, so their voltage is considered to be constant during one switching cycle.

### 3.1 Step-up voltage gain

By applying the voltage-second law to the magnetizing inductance \(L_{cm}\), the voltages across the clamp capacitors can be obtained as:

\[ V_{Co} = V_{Ca1} = V_{Ca2} = \frac{V_{in}}{1 - D} \quad (11) \]

According to the equivalent circuit of Mode V (see Figure 4(d)), the voltage across \(C_{fr}\) can be expressed as \(12\). Also, the secondary voltages of CIs \((V_{fr1}\) and \(V_{fr2}\)) are as Equations \((13)\) and \((14)\).

\[ V_{fr2} = nV_{in} \quad (14) \]

The voltages of the output capacitors can be represented as:

\[ V_{Co1} = V_{fr2} = (1 + n)V_{fr} = \frac{1 + n}{1 - D} V_{in} \quad (15) \]

According to Equations \((11)-(14)\), the voltage across the multiplier capacitors is as follows:

\[ V_{fr1} = V_{fr2} = V_{fr} = 2(1 + n)V_{fr} = \frac{2(1 + n)}{1 - D} V_{fr} \quad (16) \]

\[ V_{fr2} = (1 + n)V_{fr} = \frac{N(1 + n)}{1 - D} V_{fr} \quad (17) \]

According to Equations \((15)-(17)\), the output voltage can be obtained as:

\[ V_{out} = V_{fr1} + V_{fr2} + V_{fr3} = \left( \frac{2N + 2n + 2n + 2 + n}{1 - D} \right) V_{in} \]

Finally, the step-up voltage gain can be calculated as:

\[ M = \frac{V_{out}}{V_{in}} = \frac{2N(1 + n) + n(1 + D) + 2}{1 - D} \quad (19) \]

As can be seen from Equation \((19)\), the step-up voltage gain \(M\) can be controlled by duty cycle and turns ratio of the CIs and BIT, and a high step-up voltage gain can be achieved without large duty cycles.

Based on the performance analysis presented in section II, the leakage inductance of the magnetic devices impacts the step-up voltage gain \(M\). By considering this impact, the output voltage gain can be extracted as follows:

\[ M = \frac{2N(1 + n) + n(1 + D) + 2}{1 - D} \times \frac{1}{1 + \frac{2Q_s(2N^2 + 12N - 5)}{2(1 - D)^3} + \frac{4N^2Q_s}{(1 - D)^3}} \quad (20) \]
where $Q_i = I_L f_s / R_{on}$ and $Q_b = I_L f_s / R_{out}$.

It is obvious that the step-up voltage gain $M$ is affected by the leakage inductances, $R_{out}$, the switching frequency $f_s$ as well as the duty cycle $D$ and the turn ratios of CIs and BIT. Hence, to reduce the leakage inductances, Equation (20) results in Equation (19).

### 3.2 Voltage and current stress

The voltage stress of $S_1$, $S_2$, $S_D$, and $S_{D2}$ is equal to the voltage across $C_{cl}$ and $C_{c2}$ as follows:

$$V_S = V_{Sc} = V_{Cc} = \frac{V_{in}}{1 - D} = \frac{2N(n + 1) + n(1 + D) + 2}{V_{out}}$$  \hspace{1cm} (21)

From Equation (21), the voltage stress is inversely proportional to the turn ratios of the magnetic devices. Hence, to reduce conduction losses and cost, low-voltage-rated switching devices with low ON-state resistances can be adopted. The following equations for the voltage stresses of the diodes are provided:

$$V_{Dr} = \frac{2(n + 1)}{1 - D} V_{in} = \frac{2(n + 1)}{2N(n + 1) + n(1 + D) + 2} V_{out}$$  \hspace{1cm} (22)

$$V_{Db} = \frac{n + 2}{1 - D} V_{in} = \frac{n + 2}{2N(n + 1) + n(1 + D) + 2} V_{out}$$  \hspace{1cm} (23)

$$V_{Df} = \frac{2N(n + 1)}{1 - D} V_{in} = \frac{2N(n + 1)}{2N(n + 1) + n(1 + D) + 2} V_{out}$$  \hspace{1cm} (24)

The root mean square (RMS) value of the currents through switching devices are obtained as:

$$I_{RMS,S} = I_{in} \sqrt{\frac{2(1 + n)(1 + 2N)}{M} + \frac{4(1 + n)^2(1 + 2N)^2}{3M^2(1 - D)}}$$  \hspace{1cm} (25)

$$I_{RMS,S'} = I_{in} \sqrt{\frac{(1 - D)}{2\sqrt{3}}}$$  \hspace{1cm} (26)

$$I_{RMS,Dr} = I_{RMS,Db} = I_{out} \sqrt{\frac{1}{3(1 - D)}}$$  \hspace{1cm} (27)

$$I_{RMS,Df} = 2I_{out} \sqrt{\frac{1}{3(1 - D)}}$$  \hspace{1cm} (28)

### 3.3 Conduction losses analysis

To calculate the mathematical conversion efficiency of the proposed converter and to survey the impact of the component’s parasitic specifications on the step-up voltage gain, the leakage inductance of the CIs and BIT as well as the parallel capacitors of the MOSFETs are supposed to be zero. Subsequently, the active clamp circuits are removed $[51, 52]$. The simplified circuit schematic is depicted in Figure 6. Because of the removing the active clamp circuits, there are only four basic operation stages during a switching cycle.

When the MOSFETs $S_1$ and $S_2$ are in ON state, the voltage on $I_{out}$ is given by:

$$V_{Lm2} = V_{in} - \frac{I_{in}}{2}(R_L + R_{DS})$$  \hspace{1cm} (29)

When $S_2$ is ON and $S_1$ is OFF, the following equations are obtained:

$$V_{Lm2} = V_{in} - \frac{I_{in}}{2}(R_L + R_{DS})$$

$$- (nR_{L1} + nR_{DS} + nR_{L2}) \frac{2N + 2N + n(1 + D) + 1}{2(1 + n)(1 - D)} I_{out}$$  \hspace{1cm} (30)

$$V_{np-BIT} = V_{in} + (1 - n) V_{Lm1} + n V_{Lm2} - (R_{L1} + R_{DS}) I_{in}$$

$$+ (nR_{L1} - R_{L2}) \frac{2N + 2N + n(1 + D) + 2}{2(1 + n)(1 - D)} I_{out}$$

$$- (R_{DS} + nR_{DS} + R_{L2}) \frac{I_{in}}{2(1 - D)}$$

$$- (R_{L1} - nR_{L1}) \frac{2N + 2N + nD - n}{2(1 + n)(1 - D)} I_{out}$$  \hspace{1cm} (31)

$$V_{Cov} = -V_D - R_D \frac{I_{out}}{2(1 - D)} + R_{L1} \frac{2N + 2N + nD - n}{2(1 + n)(1 - D)} I_{out}$$

$$+ V_{np-BIT}$$  \hspace{1cm} (32)
By applying volt-sec law to \( I_{\text{out}} \) and considering the symmetry of the converter, we have:

\[
V_{L_{\text{le}2}}^{\text{III}} (2D - 1) + V_{L_{\text{le}2}}^{\text{II}} (1 - D) = V_{L_{\text{le}2}}^{\text{IV}} (1 - D)
\]

\[
V_{L_{\text{le}2}}^{\text{IV}} = V_{L_{\text{le}2}}^{\text{II}}
\]

\[
I_{\text{in}} = \left( \frac{2Nn + 2N + nD + n + 2}{1 - D} \right) \frac{V_{\text{out}}}{R_{\text{out}}}
\]

When \( S_1 \) is ON and \( S_2 \) is OFF, the following equations are obtained:

\[
V_{L_{\text{le}1}}^{\text{II}} = \frac{D}{1 - D} V_{\text{in}} - (2D - 1)(R_L + R_{DS}) \frac{I_{\text{in}}}{2(1 - D)}
\]

\[
- (R_{L1} + R_{DS}) \frac{I_{\text{in}}}{2}
\]

\[
- (nR_{L1} + R_{DS} + nR_{DS}) \frac{2NH + 2N + nD + 1}{2(1 + n)(1 - D)} I_{\text{out}}
\]

The voltage across the output capacitors can be calculated as:

\[
V_{Cd1} = (R_{L1} + R_{DS}) \frac{2NH + 2N + nD + 1}{2(1 + n)(1 - D)} I_{\text{out}} + R_D \frac{I_{\text{out}}}{2(1 - D)}
\]

\[
-R_D \frac{I_{\text{in}}}{2} - V_D = V_{Cd1} = V_{Np-BIF} - nV_{L_{\text{le}2}}^{\text{II}}
\]

\[
V_{Cd2} = nV_{Np-BIF} - V_D
\]

Finally, from Equations (29)–(38), the converter efficiency as well as the voltage gain can be calculated as:

\[
\eta = 1 - \frac{4(1 - D) V_D}{(2Nn + 2N + nD + 2) V_{\text{in}}}
\]

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = 1 + \frac{2N + 2N + nD + 2}{2(1 - D) R_c} - \frac{A1}{B}
\]

where

\[
A1 = \left[ (4Nn + 4N + 3n + 4)(2Nn + 2N + n + 2 + nD) + (4Nn + 2N + 3n + 3) \left( \frac{2N + 2N + nD + 1}{1 + n} \right) \right] n
\]

\[
- (2N + 2) \left( \frac{2N + 2N + n + nD + 2}{1 + n} \right) n R_{L1}
\]

For the following power specifications (equal to those for experimental verification), the mathematical conversion efficiency \( \eta \) and the step-up voltage gain \( M \) of the proposed converter are illustrated in Figure 7. As can be seen, the conversion efficiency \( \eta \) and the step-up voltage gain \( M \) are influenced by the parasitic components and are also reduced by growing the winding resistances of the magnetic devices.

\[
A_2 = \left[ (4Nn + 4N + 3n + 4)(2Nn + 2N + n + 2 + nD) + (2N + 2N + nD + 1) \right] R_{DS}
\]

\[
A_3 = \left[ (2N + 1)(2Nn + 2N + nD + 1) + (2N + 2)(2Nn + 2N + n + nD + 2) \right] R_{L1}
\]

\[
B = (2N + 2N + 2 + 2(2D - 1)(2Nn + 2N + n + 2 + nD)) \times (R_{L1} + R_{DS})
\]

\[
V_{\text{in}} = 22 \text{ V}; n = N_1 = 1; P_{\text{out}} = 600 \text{ W}; R_{DS} = 4.5 \text{ m\Omega};
\]

\[
R_{Df} = R_{DF} = 10 \text{ m\Omega}; \ V_{FDf} = V_{FDr} = 1.2 \text{ V};
\]

### 3.4 Soft-switching performance

ZVS turn-OFF for the main switches is fulfilled thanks to their parallel capacitors. For the clamp switches, ZVS turn-ON is realised naturally once their anti-parallel diodes are in ON state. To achieve ZVS turn-ON operating condition for the main switches (when the clamp switches are in OFF state), the stored energy in the leakage inductances must be higher than that in the parallel capacitors of the main switches, which yields the
following restriction:

\[ I_{L,m1} \geq \frac{C_{m} V_{m}^2}{n^2 (2N + 2)^2 L_{ad}} \]  \hspace{1cm} (41)

To ensure ZCS turn-OFF for all diodes, the current falling rates of the diodes (as Equations (8)–(10)) must be controlled by using the leakage inductances of the BIT and the CIs.

4 | DESIGN EXAMPLE

4.1 | Coupled-inductors and built-in transformer

The design procedure for the circuit components is conducted by using the experimental specifications as 22 V input voltage to 380 V output voltage and 61% nominal duty cycle. \( L_{m1} \) and \( L_{m2} \) are designed to assure operating in continuous current mode (CCM) at 10% of full load:

\[ L_{m1} = L_{m2} = L_m \]

\[ \geq \left[ \frac{10D_{\text{min}} (1 - D_{\text{min}})^2 R_v}{(2N + 2 + n + nD + 2)^2 f_s} \right] \]  \hspace{1cm} (42)

By considering \( D_{\text{min}} = 0.5 \), \( L_{mB} = 53.3 \) \( \mu \)H and having \( L_{m1}, n_1 \) is computed as:

\[ n_1 = \frac{L_{m1}}{L_{m,\text{Max}}} \]  \hspace{1cm} (43)

where \( I_{L,m,\text{Max}} \) denotes the maximum value of the current through magnetizing inductance and is \( \approx (I_{m}/2) + (DV_{\text{in}}/2L_{mfs}) \). \( B_{\text{Max}} \) represents the maximum amount of the magnetic flux density and \( A_C \) is the core cross-sectional area of the coupled-inductors.

For the proposed converter with 97% conversion efficiency at full load condition, \( I_{L,m,\text{Max}} = 17.3 \text{ A} \) is obtained. Also, EE55 core is selected with equivalent area of the magnetic core equal to \( A_e = 354 \text{ mm}^2 \) and the maximum flux density of 320 mT. Considering 200 mT variation in flux density, \( n_p = n_r = 13.02 \) is obtained (using Equation (44)), which is rounded to 13 turns when fabricating a CI with \( L_m = 57 \text{ uH} \) and \( L_{L,k} = 1.2 \text{ uH} \). From Equation (41), it can be inferred that the proposed converter provides ZVS performance at 12% of load.

When switch \( S_1 \) is ON and switch \( S_2 \) is OFF, the voltage applied to the primary winding of the BIT is obtained as:

\[ V_{P,\text{Built-In Transformer}} = \frac{1 + n}{1 - D} V_{\text{in}} = N_p \frac{(1 + n) \Delta B_p A_{pB}}{(1 - D) T_p} \]  \hspace{1cm} (44)

where \( A_{pB} \) denotes the equivalent area of the magnetic core and \( \Delta B_p \) represents the variations in the magnetic flux density of the BIT. Selecting EE55 ferrite core yields \( N_p = N_r = 12.42 \) that is rounded to 13 turns for the same reason as that for CIs. The measured value for the magnetizing and leakage inductances of the BIT are about 790 and 2.5 \( \mu \)H, respectively.

4.2 | Semiconductors

From Equation (21), the voltage stress across the power MOSFETs are calculated 56.7 V. Therefore, IRF4110/PBF (100 V, 4.5 m\( \Omega \)) is selected for the power MOSFETs. From Equations (22)–(24), \( V_{D1} = V_{Df} = 199.7 \text{ V} \) and \( V_{Dh} = 147.5 \text{ V} \). Hence, MUR840 is chosen for diodes.

4.3 | Clamp and voltage multiplier capacitors

The capacitors are designed by taking into account the voltage ripple on them. So, the value of the capacitors can be calculated by:

\[ C_m \geq \frac{P_{\text{out}}}{2V_{\text{out}} \Delta V_{C_m} f_s} \]  \hspace{1cm} (45)

\[ C_c \geq \frac{(2N + n + nD + 2)P_{\text{out}}}{4V_{\text{FS}} \Delta V_{C_c} f_s} \]  \hspace{1cm} (46)

where \( \Delta V_{C_m} \) and \( \Delta V_{C_c} \) are the voltage ripple on the \( C_m \) and \( C_c \), respectively. \( V_{C_m} = 56.7 \text{ V} \) and \( V_{C_m} = 100 \text{ V} \) are obtained from Equations (11) and (15), respectively. By restricting the voltage ripple across \( C_m \) and \( C_c \) to the 1% and 5% of their steady-state values, respectively, their values are extracted as \( C_m = 7.89 \text{ \mu F} \) and \( C_c = 10 \text{ \mu F} \). Hence, 10 \( \mu \text{F} \) value is chosen for multiplier and clamp capacitors.

4.4 | Performance comparison

In order to probe the advantages of the proposed converter, a performance comparison between the proposed converter and the converters presented in [34, 38, 42–44, 48–53, 55, 56, 58], and [59] is carried out and the results are provided in Table 1, where the voltage across the diodes in the table is the maximum voltage values of the them. Figure 8 illustrate the comparison results of voltage gain and the voltage stress across the switches and diodes. As can be seen in Figure 8(a), the higher step-up voltage gain belongs to the proposed converter. Moreover, according to Figure 8(b) the voltage stress across the MOSFETs in the proposed converter is the lowest from all. In such a case, devices with low ON-state resistance can be adopted to decrease conduction losses and cost. It is seen from Figure 8(c) that the voltage stress across the diodes in the proposed converter is much lower than the output voltage which is due to using forward-flyback topology and adjusting the turns ratio. Also, ZVS operating condition for all the switches in the proposed converter and the converters presented in [49–53, 55, 56, 58, 59] is realized, whereas this feature is not fulfilled for the converters in [34, 38, 42–44, 48].
TABLE 1  Performance comparison between the interleaved high step-up converters

| Topology      | Voltagen-step-up technique | Voltagegain | $V_{Df}$ | $V_{D,\text{max}}$ | No. of components | Switch | Diode | Cap. | Core | Total | Soft switching | Cost($) |
|---------------|-----------------------------|-------------|----------|--------------------|-------------------|--------|-------|------|------|-------|----------------|--------|
| Ref. [34] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{(n+1)}{2(1+n)}$ | 2 | 6 | 5 | 2 | 15 | ZCS with $I_{Lh}$ | 28.32 |
| Ref. [38] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{(n+1)}{2(1+n)}$ | 2 | 9 | 7 | 2 | 20 | ZCS with $I_{Lh}$ | 30.25 |
| Ref. [42] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{(n+1)}{2(1+n)}$ | 2 | 6 | 6 | 2 | 16 | ZCS with $I_{Lh}$ | 25.2 |
| Ref. [43] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{(n+1)}{2(1+n)}$ | 2 | 6 | 6 | 2 | 16 | ZCS with $I_{Lh}$ | 33.34 |
| Ref. [44] B±4-VMC | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | 2 | 6 | 5 | 3 | 16 | ZCS with $I_{Lh}$ | 28.4 |
| Ref. [48] B±4-CI + VMC | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | 2 | 8 | 7 | 3 | 20 | ZCS with $I_{Lh}$ | 31.35 |
| Ref. [49] Inductor + VMC | $\frac{1}{2}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | 4 | 7 | 9 | 6 | 26 | ZVS | 36.17 |
| Ref. [50] C±4-VMC | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | 4 | 4 | 5 | 2 | 15 | ZVS | 33.48 |
| Ref. [51] B±4-VMC | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | 4 | 2 | 3 | 3 | 12 | ZVS | 32.44 |
| Ref. [52] B±4-VMC | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | $\frac{1}{2(1+2)+1}$ | 4 | 4 | 5 | 3 | 16 | ZVS | 34.18 |
| Ref. [53] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | 4 | 2 | 4 | 2 | 12 | ZVS | 31.04 |
| Ref. [55] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | 4 | 6 | 9 | 4 | 23 | ZVS | 39.1 |
| Ref. [56] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | 3 | 10 | 6 | 3 | 22 | ZVS | 38.1 |
| Ref. [58] B±4-VMC | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | 4 | 2 | 4 | 3 | 13 | ZVS | 31.95 |
| Ref. [59] C±4-VMC | $\frac{2(1+n)}{1-D}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | $\frac{1}{2(1+n)}$ | 4 | 4 | 5 | 2 | 15 | ZVS | 31.84 |
| Proposed B±4-CI + VMC | $\frac{2(1+n)}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | $\frac{1}{2(N+1)+1}$ | 4 | 6 | 6 | 3 | 19 | ZVS | 35.82 |

Total number of the components is a deterministic factor for the volume of the converter at a given switching frequency. It is seen from Table 1 that the proposed converter utilizes 19 total number of components which is lower in comparison with the converters of [38, 48, 49, 55, 56]. Therefore, it is estimated that the proposed converter has a smaller volume in comparison with the mentioned competitors. Although the proposed converter implements higher number of components with a larger fabricated volume than [42–44, 50–53, 58, 59]; however, it achieves the highest voltage gain and the lowest voltage stress across MOSFETs which covers its higher components. In order to compare the cost of the proposed topology with other converters, the same parameters ($V_{in} = 22$ V, $V_{out} = 380$ V, $P_{out} = 600$ W, $N = n = 1$) and similar series of the elements are considered for all converters. Depending on the voltage stress of the MOSFETs, IRFB4110, IRFB4127, and IRFB4137 are selected for MOSFETs with voltage stress of less than 100, 200, and 300 V, respectively. In addition, MUR840, MUR860, and MUR880 are selected for diodes with voltage stress of less than 400, 600, and 800 V, respectively. EE55 core for CI and BIT, and torpid core for simple inductor are selected. Also, capacitors are categorized based on their operating voltage of less than to 200, 250, 400, and 450 V, respectively. It should be mentioned that PCB and control circuit are not considered in the price and semiconductor and capacitor prices are obtained from mouser.com website and magnetic core are obtained from local sellers. As can be seen, although the price of the proposed converter is almost higher than the other topologies except [49, 55, 56], the advantages of the proposed converter are greatly improved related to other converters.

According to Figure 8(a), the converters of [48, 58], and [59] have the highest voltage gain after the proposed converter. Therefore, they are selected to conduct a comparison in the terms of the RMS current through the main MOSFETs and the diodes which is shown in Table 2. The result of the comparison is shown in Figure 9. It is seen that at a given voltage gain the proposed converter and [58] have a lower RMS current through the MOSFETs in comparison with [59]. Moreover, the proposed converter and [48] have a lower RMS current trough the diodes.

5 | EXPERIMENTAL VERIFICATION

To probe the advantage of the proposed converter, a 22–380 V prototype with 600 W output power is built in the laboratory with the components’ specifications of Table 3. The nominal duty cycle is around 61%.

Figure 10(a) shows the experimental results of the output voltage and current. It is seen that the output voltage is about 380 V and the output power is about 1.58 A which provides 600 W output power. Figure 10(b–d) depicts the
TABLE 2 Comparison of the RMS currents passing through the semiconductors

| Converters | Main switches | Diodes |
|------------|---------------|--------|
| Ref. [48]  | $I_{out} \sqrt{\frac{1+4(N+1)n}{1+D}} \left(D-1\right) + \frac{\left(N+4n+3\right)^2}{1+D}$ | $I_{out} \sqrt{\frac{1}{1-D}}$ |
| Ref. [58]  | $I_{out} \sqrt{\frac{DM^2}{4} + \frac{4(N+1)^2}{N+1-D} + \frac{M}{N+1}}$ | $2I_{out} \sqrt{\frac{1}{3(1-D)}}$ |
| Ref. [59]  | $I_{out} \sqrt{\frac{2(2n+1)M}{1-D}} \left(\frac{2n+1}{3} - \frac{n}{3} \right)$ | $2I_{out} \sqrt{\frac{1}{3(1-D)}}$ |
| Proposed   | $I_{out} \sqrt{\frac{2}{D} + \frac{2(4+6n+4N^2+4n^2)}{M} + \frac{4(3+n)^2(4+2N^2)}{3M^2(1+D)}}$ | $2I_{out} \sqrt{\frac{1}{3(1-D)}}$ |

The experimental results of the voltages of the capacitors in the proposed converter. The measured values are about $V_{Co1} = 190 \, \text{V}$, $V_{Co2} = 95 \, \text{V}$, $V_{Cm1} = 100 \, \text{V}$ and $V_{CC1} = V_{CC2} = 58 \, \text{V}$. The experimental results match the steady-state analysis, as well.

Figure 11(a) shows the experimental results of the input current, and the currents through the leakage inductances of the CL. The average value of the input current is about 28.3 A. One can see that 622 W power is drawn from the input power source and the conversion efficiency is about 96.4%. The input current ripple is about 5 A which is 17.6% of input current ripple. Moreover, a good current sharing performance is concluded form

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FIGURE 8 Performance comparison, (a) voltage gain, (b) normalized voltage stress across switches, (c) normalized voltage stress across diodes

FIGURE 9 Comparison of normalized RMS currents passing through the semiconductors

$\bar{i}_{Lk1}$ and $\bar{i}_{Lk2}$. Figure 11(b) shows the experimental result of the current through the leakage inductance of the BIT.

Figure 12 shows the experimental results of the drain-source voltage and the current of the main and clamp MOSFETs. The voltage stress across the MOSFETs is clamped to nearly 60 V
FIGURE 10  The experimental results of the, (a) output voltage and output current, (b) voltages of capacitors $C_{o1}$ and $C_{o2}$, (c) voltages of capacitors $C_{c1}$ and $C_{c2}$, (d) voltage of capacitor $C_{m1}$.

FIGURE 11  The experimental results of the, (a) input current, and the currents through the leakage inductances of the CI. (b) the current through the leakage inductance of the BIT.

FIGURE 12  The experimental results of the drain-source voltage and the current of the main and clamp MOSFETs.

which is about 15% of the high output voltage and utilization of low voltage rated devices is facilitated. Moreover, ZVS Performance is realized for the MOSFETs through whole switching period.

Figure 13 shows the experimental results of the voltage stress and current of the diodes. It is clear that the voltage stresses of the diodes are lower than the high output voltage (nearly $V_{out}/2$). In such a case, low forward voltage diodes can be implemented which decreases the associated losses and improves the circuit performance. Furthermore, all diodes are turned OFF with ZCS performance and the reverse recovery problems is alleviated.

The dynamic performance of the proposed converter is given in Figure 14. From Figure 14(a), it is clear that the output voltage is well regulated at 380 V when the output power is changed between half load and full load. According to Figure 14(b), the voltage stabilization is also achieved sufficiently while the input voltage is fluctuated between 17, 22, and 27 V.

Figure 15(a) shows the measured conversion efficiency of the proposed converter along with its theoretical values. The

### TABLE 3  Components specifications of the proposed converter

| Components | Parameters |
|------------|------------|
| Output power ($P_{out}$) | 600 W |
| Input-output voltages ($V_{in} - V_{out}$) | 22 – 380 V |
| Switching frequency ($f_s$) | 100 kHz |
| Power MOSFETs ($S_1, S_2, S_{C1}, S_{C2}$) | IRF4410BF (100 V, 4.5 mΩ) |
| Diodes ($D_{s1}, D_{s2}, D_{o1}, D_{o2}, D_{j1}, D_{j2}$) | MUR840 |
| Capacitor ($C_{C1}, C_{C2}, C_{o1}, C_{o2}$) | 10 μF (Film Capacitors) |
| Capacitor ($C_{c1}, C_{c2}, C_{c3}$) | 220 μF (Electrolytic Capacitors) |
| Parallel capacitors ($C_{s1}, C_{s2}$) | 3.5 nF |
| Coupled inductors | EPCOSB66344 (Ferrite Core EE55) |
| Built-in transformer | $N = 1, I_{win} = 800$ A, $L_{lkb} = 2.5$ μH |

n = 1, $I_{win} = 800$ A, $L_{lkb} = 2.5$ μH
full load efficiency is about 96.4% and the highest efficiency is 96.8% achieved at 500 W output power. At lower loads, the core losses and skin effect, decrease the experimental efficiency in comparison with the theoretical one. However, by increasing of the load the, effect of these losses decreases and the efficiencies match each other. Figure 15(b) illustrates the full load loss breakdown of the proposed topology in which the detailed losses of the components is given in Table 4. As can be seen, the diode, CI and BIT losses are the predominant power losses in the proposed topology. So, the better graded wires for CI and BIT and using diodes with lower forward voltage improves the conversion efficiency and circuit performance. Total power losses is 16.67 W and the calculated efficiency is about 97.3% which is close to the measured value. Table 5 shows the efficiency comparison between the proposed converter and its competitors in discussed in Table 1. The major factors that affect the conversion efficiency are switching frequency, input/output voltage and output power. At fixed output power, lower input voltage causes higher input current to be drawn from the input side which consequently decreases the conversion efficiency. It is seen that the proposed converter with 100 kHz switching frequency, 22 V/380 V voltage conversion and 600 W output power has a higher conversion efficiency in comparison with the converters of [38, 42–44, 50–53, 37]. Although the converters of [34, 48, 49, 55, 58, 59] have higher conversion efficiencies; however, their input voltage and/or switching frequency are considerably higher and lower, respectively.

6 | CONCLUSION

An interleaved high step-up converter with ZVS performance has been introduced in this paper. By inserting the secondary windings of the CIs between the clamp circuits and the primary
TABLE 4  Loss distributions of the proposed converter

| Components                      | Power loss relations                                                                 | Loss value       |
|---------------------------------|--------------------------------------------------------------------------------------|------------------|
| Main switches                   | $2(R_{DS} \times I_{RMS,S}^2)$                                                      | $2 \times 1.37$ W|
| Clamp switches                  | $2(R_{DS} \times I_{RMS,C}^2)$                                                      | $2 \times 0.12$ W|
| Flyback diodes + Forward diodes + Output diodes | $2(V_{DS} \times I_{RMS,Ds} + R_{DS} \times I_{RMS,Ds}^2)$                    | $2 \times 1.97$ W + $2 \times 0.97$ W |
| Flyback diodes + Forward diodes + Output diodes | $2(V_{DS} \times I_{RMS,Ds} + R_{DS} \times I_{RMS,Ds}^2)$ | $2 \times 0.97$ W |
| CI wires + BIT wires            | $2(R_{CI_{Pr}i} \times I_{RMS,CI_{Pr}i}^2 + R_{CI_{Sec}} \times I_{RMS,CI_{Sec}}^2)$ | $4.27$ W + $0.19$ W |
| Capacitors                      | $ESR \times I_{RMS,Cap}^2$                                                          | $1.42$ W         |

TABLE 5  Efficiency comparison of the proposed converter

| Topology | Switching Frequency (KHz) | Input Voltage (V) | Output Voltage (V) | Output Power (W) | Efficiency (%) |
|----------|---------------------------|-------------------|--------------------|------------------|----------------|
| Ref. [34]| 40                        | 40                | 380                | 600              | 96.6           |
| Ref. [38]| 50                        | 7                 | 170                | 120              | 89             |
| Ref. [42]| 40                        | 20                | 400                | 400              | 94             |
| Ref. [43]| 40                        | 50                | 400                | 400              | 96             |
| Ref. [44]| 100                       | 40                | 380                | 600              | 96.2           |
| Ref. [48]| 20                        | 45                | 675                | 600              | 97.6           |
| Ref. [49]| 100                       | 40                | 400                | 600              | 97.7           |
| Ref. [50]| 50                        | 48                | 380                | 600              | 93             |
| Ref. [51]| 50                        | 48                | 380                | 600              | 94.5           |
| Ref. [52]| 100                       | 40                | 380                | 600              | 96.2           |
| Ref. [53]| 50                        | 12                | 120                | 500              | 91.2           |
| Ref. [55]| 50                        | 30                | 270                | 600              | 97.2           |
| Ref. [56]| 50                        | 24                | 380                | 300              | 92.5           |
| Ref. [58]| 40                        | 35                | 500                | 600              | 97.2           |
| Ref. [59]| 100                       | 40                | 600                | 600              | 97.1           |
| Proposed| 100                       | 22                | 400                | 600              | 96.4           |

winding of the BIT, high voltage gain and reduced voltage stress across the switching devices is achieved. Therefore, working at high duty cycles to achieve high voltage gain is avoided and the low voltage rated switching devices can be implemented. Moreover, all of the MOSFETs are operated with ZVS performance through whole switching cycle and the switching losses is minimized, effectively. Furthermore, the input current ripple is decreased thank to interleaving effect and the ZCS turn-OFF of the diodes is realized due to the presence of the leakage inductances. Finally, to examine the effectiveness of the proposed converter, the performance operation was validated via experimental results of a 22–380 V laboratory prototype with 600 W output power. The full load efficiency was about 96.4% and the highest efficiency was 96.8% achieved at 500 W output power. It is concluded that the proposed high efficiency converter can be regarded as a suitable solution for high step-up and high current applications such as renewable energy systems.

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