P²M-DeTrack: Processing-in-Pixel-in-Memory for Energy-efficient and Real-Time Multi-Object Detection and Tracking

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Abstract—Today’s high resolution, high frame rate cameras in autonomous vehicles generate a large volume of data that needs to be transferred and processed by a downstream processor or machine learning (ML) accelerator to enable intelligent computing tasks, such as multi-object detection and tracking. The massive amount of data transfer incurs significant energy, latency, and bandwidth bottlenecks, which hinders real-time processing. To mitigate this problem, we propose an algorithm-hardware co-design framework called Processing-in-Pixel-in-Memory-based object Detection and Tracking (P²M-DeTrack). P²M-DeTrack is based on a custom faster R-CNN-based model that is distributed partly inside the pixel array (front-end) and partly in a separate FPGA/ASIC (back-end). The proposed front-end in-pixel processing-down-samples the input feature maps significantly with judiciously optimized strided convolution and pooling. Compared to a conventional baseline design that transfers frames of RGB pixels to the back-end, the resulting P²M-DeTrack designs reduce the data bandwidth between sensor and back-end by up to 24×. The designs also reduce the sensor and total energy (obtained from in-house circuit simulations at Globalfoundries 22nm technology node) per frame by 5.7× and 1.14× respectively. Lastly, they reduce the sensing and total frame latency by an estimated 1.7× and 3× respectively. We evaluate our approach on the multi-object object detection (tracking) task of the large-scale BDD100k dataset and observe only a 5% reduction in the mean average precision (0.8% reduction in the identification F1 score) compared to the state-of-the-art.

Index Terms—autonomous vehicles, detection, tracking, processing-in-pixel-in-memory, faster R-CNN

I. INTRODUCTION & RELATED WORK

Artificial intelligence (AI)-enabled video processing presents a challenging problem because the high resolution, high dynamic range, and high frame rates of image sensors generate large amounts of data that must be processed in real-time [14], [28]. In particular, the data transmission between the image sensor and the off-chip processing unit leads to significant latency, energy, and bandwidth bottlenecks. This problem is further exacerbated in an autonomous driving scenario, where there are a plethora of other sensors, such as radars and inertial measurement units (IMUs), that also need to transmit data for intelligence processing, including perception and localization [30].

To mitigate this problem, prior works have proposed massively parallel in-memory [6], [18], in-sensor [5], [19], and in-pixel computing [2], [3], [7], [12], [13], [20], that aims to desegregate sensing, memory, and computation. Some in-sensor computing works implement analog computing in peripheral circuits for mapping AI algorithms [5], [19] but rely on serial kernel access that incurs significant energy and throughput bottlenecks. On the other hand, in-pixel computing approaches based on emerging technologies [2], [20] promise excellent energy and throughput improvements but are not compatible with the foundry-manufacturing of modern CMOS image sensor (CIS) platforms and hence are difficult to scale. Other solutions that are based on CMOS technology [3], [12], [13] have been limited to toy workloads, such as digit recognition, because they lack the support of multi-channel in-pixel convolutions.

More recently, an in-situ processing-in-pixel-in-memory (P²M) framework has been proposed [7] in which the pixel array implements several deep learning operations, including multi-bit, multi-channel convolution, batch normalization (BN), and ReLU operations. However, this work proposed using non-overlapping strides in the convolutional layer that can lead to a significant drop in accuracy for more complex vision tasks, such as object detection and tracking. In particular, these complex tasks often involve large kernel sizes operating over high-resolution images for which overlapping strides are necessary to avoid missing critical spatial features. In fact, most of the prior works, including [7], have been focused on datasets, such as CIFAR-10 [27], hyperspectral image recognition [8] and TinyML applications [26], which have input images with a significantly lower resolution compared to those in large-scale object detection benchmarks, such as BDD100k [32], and do not represent images captured by the existing high resolution (≥1M Pixel) image sensors.

To the best of our knowledge, this work is the first to show the feasibility of scaling analog processing-in-pixel paradigms, specifically the P²M paradigm, to large-scale complex com-
puter vision applications like real-time multi-object detection and tracking featuring manufacturing-friendly hardware platform. As compared to prior work on P²M [7], the presented P²M-DeTrack proposal features 1) support for overlapping strides, 2) novel P²M-DeTrack parallelism using column-parallel ADCs, and 3) tightly-intertwined algorithm-hardware co-design for real-time complex vision task involving multi-object detection and tracking. Specifically, as illustrated in Fig. 1, our approach termed P²M-DeTrack enables the support for overlapping strides, by inclusion of additional weight transistors $W_i$ inside the pixel, such that weights transistors cater to individual stride in a specific channel as well as multiple channels in the output feature map. This in turn improves task accuracy and max/average pooling that jointly yields up to $24 \times$ bandwidth reduction between the image sensor and back-end processing unit. Further, we show how proposed novel parallelism exploiting column parallel ADCs mitigate the large latency induced by overlapping strides, thereby meeting the high frames per second (FPS) needed for real-time detection and tracking. Finally, we present and evaluate P²M-compatible faster R-CNN-based detection [25] and tracking [23] models obtained via extensive algorithm-hardware co-design. We choose BDD100K [32] to validate our approach because it incorporates geographic, environmental, and weather diversity as well as intentional occlusions, and is the most comprehensive open-source dataset for large-scale object detection and tracking geared towards autonomous driving. Our resulting models obtain significant reductions in communication bandwidth, total latency, and energy consumption with negligible drop in detection and tracking accuracies.

II. PRELIMINARIES

A. P²M: Processing-in-Pixel-in-Memory Paradigm

The P²M framework proposed in [7] implements multi-bit, multi-channel, non-overlapping strided convolution using memory (weight)-embedded pixels. The weights are represented by the transistor widths [31], which modulates the pixel outputs, and the BN and ReLU operations are implemented in the periphery of the pixel array using available on-chip column parallel ADCs in CMOS image sensors. Although the width-encoded weights are fixed during manufacturing, this lack of programmability may be more than an acceptable penalty because the first few layers of any computer vision (CV) model extract high level features that can be common across various vision datasets. Moreover, we can also reconfigure the weights by mapping them to emerging resistive non-volatile memory elements embedded within individual pixels [7]. P²M leverages the existing on-chip correlated double sampling (CDS) circuit in commercial cameras to accumulate both negative and positive weights that are needed to train accurate CV models. Note that the CDS circuit also helps implement the subsequent ReLU operation. Interested readers are referred to [7] for more details of the P²M circuit implementation.

B. Object Detection & Tracking

QDTrack is a tracking by detection method [23] that uses a two stage detector such as faster R-CNN [25] to associate region proposals in temporal neighborhood using contrastive loss. This helps to associate identical objects in the same representation space while pushing dissimilar objects apart. QDTrack creates a per frame representation for each object detected which is then used in nearest neighbor search to do
association between frames. In this work, we adopt the state-of-the-art (SOTA) QDTrack method with the faster R-CNN architecture for detection to validate our approach.

III. PROPOSED METHODOLOGY

In this section, we first present our algorithm-hardware co-design framework that enables the support for non-overlapping strides and pooling layers which improves task accuracy. Our framework also enables real-time detection and tracking by exploiting column parallel ADCs for improved analog processing throughput. Lastly, we analytically derive the bandwidth reduction (which leads to energy and latency savings) obtained by P²M-DeTrack.

A. Algorithm-Hardware Co-Design

Strided Convolution: In order to implement the strided convolution needed by object detection models, we propose to embed each pixel with different sets of weight transistors, depending on the value of the stride. In particular, as illustrated in Eq. 1, the maximum number of required transistors ($N_t$) per pixel is calculated as

$$N_t = \left\lceil \frac{K}{S} \right\rceil^2 \ast C_o$$  \hspace{1cm} (1)

where $K$, $S$, and $C_o$ are the kernel size, stride, and the number of output channels of the in-pixel layer. Notice that a lower stride value improves detection and tracking accuracy but incurs more transistors and higher required data transmission bandwidth between the sensor and back-end processing unit.

Pooling: The pooling layer in a CNN backbone reduces both the spatial dimensions of a feature map. In order to increase bandwidth reduction, we propose to implement the first pooling layer, following the convolutional, BN, and ReLU layers, inside the P²M chip. To achieve this, we buffer the outputs of the counter (of a single-slope ADC) used to implement the ReLU [7], and perform an ‘average’ or ‘max’ operation by digital logic in the periphery of the pixel array, as illustrated in Fig. 1. Consequently, we can map all the computational aspects of modern CNN layers inside the sensor chip through P²M analog computing.

$P²M$-DeTrack Parallelism: Enabling P²M-DeTrack computations inside the pixel array opens up a new opportunity to improve in-pixel parallelism for a given channel. Consider Fig. 2 that shows a pixel array of size $5 \times 5$ and $2 \times 2$ kernel with a stride of 1. Operating on Row-1 and Row-2 across two cycles (Fig. 2(a) and Fig. 2(b)), all the output activations corresponding to the horizontal striding can be generated. Note, for each kernel one ADC in the periphery, represented with same color coding as the corresponding kernel, is activated to convert the analog convolution operation into digital activations. More generally, this implies for each kernel of size $K \times K$ only one among $K$-ADCs is being utilized, leaving $(K-1)$ ADCs idle (not used) per $K$ columns. Fig. 2 presents a method to exploit such idle ADCs to improve processing parallelism. Specifically, for each column, $K$ kernels can be activated, simultaneously. $K$ ADCs on $K$ columns would be used to convert the analog convolution output to digital activation. Assuming a stride of $S$, $\left\lfloor \frac{K}{S} \right\rfloor$ clock cycles are required to process each row, where $\lceil \cdot \rceil$ denotes the ceiling function. On the other hand, using $K$ ADCs in parallel for each kernel, implies that only $\left\lceil \frac{H}{K} \right\rceil$ cycles are required to process each column, where $H$ is the height of the input activation map (which equals the height of the input activation map divided by $S$). Consequently, the number of clock cycles required to yield the complete digital output activation map for a given channel is

$$N_c = \left\lceil \frac{H}{K} \right\rceil \ast \left\lceil \frac{K}{S} \right\rceil$$  \hspace{1cm} (2)

In this way, P²M-DeTrack enables row and column parallelism, transforming the pixel array into multiple analog parallel processing blocks.

Discussion: The parallelism in P²M-DeTrack within a channel is limited by the amount of overlapping of the kernels. More precisely, it takes $\left\lceil \frac{K}{S} \right\rceil$ cycles to execute each pixel row. In addition, the different channels must be executed on the pixel array sequentially. Moreover, the number of required weight transistors per pixel is dependent on the kernel size, stride, and number of channels which is limited by area and technology constraints [7]. These constraints motivate a circuit-algorithm co-design that minimizes the number of channels and maximizes the stride $S$ subject to FPS requirements and achieving close to state-of-the-art (SOTA) accuracy. Finally, to achieve these accuracy goals, we must consider the non-linearities of the analog circuitry in the training process [7]. In particular, we focus on maximizing the mean average precision (mAP) corresponding to an intersection of union (IoU) averaged uniformly from 0.5 to 0.95 with a step size of 0.05, and mean identification F1 score (IDF1) [23] for object detection and tracking, respectively.

B. Bandwidth Reduction

To quantify the bandwidth reduction (BR) by the P²M-implemented layers, let the number of elements in the RGB input image be $I$ and in the output activation map after the pooling layer be $O$. Then, $BR$ can be estimated as

$$BR = \left( \frac{0}{I} \right) \left( \frac{4}{3} \right) \left( \frac{12}{N_o} \right)$$  \hspace{1cm} (3)

Here, the factor $\left( \frac{4}{3} \right)$ denotes the demosaicing operation [1], which converts the Bayer’s pattern of RGGB pixels to RGB
pixels by either ignoring the additional green pixel or designing the circuit to effectively take the average of the photodiode currents coming from the green pixels. The factor $\frac{12}{N_b}$ denotes the ratio of the bit-precision between the image pixels captured by the sensor (pixels typically have a bit-depth of 12 [22]) and the quantized output of the first convolutional layer denoted as $N_b$. Let us now substitute

$$O = \left(\frac{(i-K+2+2S')}{S} + 1\right)^2 - K + 2 + D D' + 1 \right)^2 = C_o, \quad I = i_2 \ast 3$$

into Eq. 3, where $i$ denotes the spatial dimension of the input image and $C_o$ denotes the number of output channels of the first convolutional layer. While $K$, $D$, $S$ denote the kernel size, padding and stride of the in-pixel convolutional layers, respectively, similar notations with the prime superscript $'$ denote the same hyperparameters of the pooling layer. We report the BR obtained by some of these hyperparameter combinations (selected based on the design space exploration approach discussed above) in Table I.

### IV. Simulation Results

In this section, we first introduce the implementation details and present our detection and tracking results on the BDD100K dataset. We then provide the energy consumption and FPS improvements obtained by our approach.

#### A. Experimental Setup

We evaluate P$^2$M-DeTrack on BDD100K detection and tracking datasets with 12 and 10 object categories, respectively. While the detection set includes 70,000 images for training, and 10,000 images for validation, the tracking dataset includes 1,400 videos (278K images) for training and 200 videos (40K images). All these images have a resolution of 1.06M Pixel. Note that we report results on the validation dataset. The images in the tracking set are annotated per pixel area is expected because of the dense metal-pitch (MP) and contacted poly-pitch (CPP) [11] of advanced technology nodes and the relatively large sizes of underlying pixel arrays.

In addition, to improve the accuracy of downsampled output feature maps of the sensor, the feature maps are upsampled in the back-end processing unit, as shown in Fig. 1. In particular, the spatial dimension at the input of the back-end is chosen to be no less than $(\frac{1}{4})^{th}$ of the image dimension. In general, the data generated from sensor has to be transferred through costly wired or wireless channels, which could form the key energy bottleneck for the overall system, particularly if the physical distance between the front- and back-end is large.

#### B. Detection Results

We developed multiple detection and tracking models with different strides in the convolutional and pooling layers (see Table I) as shown in Table II. The evaluated models in Table I yield mAPs for IoU=0.5:0.95 within 1% of the baseline model, as detailed in Table II. We also ablate over the number of channels and strides in Fig. 3 to understand the limits of bandwidth reduction. The figure shows that the mAP drops beyond 1% as we decrease the number of channels below 16. A similar significant accuracy drop is observed for strides beyond 1% as we decrease the number of channels below 16. A similar significant accuracy drop is observed for strides beyond 1%

### Table I

| Convolutional stride ($S$) | Pooling stride ($S'$) | ReLU output bit-width ($N_b$) | Transistors/pixel ($N_t$) | Bandwidth Reduction (BR) |
|---------------------------|----------------------|-------------------------------|---------------------------|--------------------------|
| 2                         | 2                    | 8                            | 256                       | 6                        |
| 4                         | 2                    | 8                            | 64                        | 24                       |
| 6                         | -                    | 8                            | 64                        | 13.5                     |

For a fair comparison, all results are produced using the MMDetection framework [4] and the standard COCO-style evaluation protocol. In addition, we use ImageNet-pretrained ResNet-50 as the backbone to all our models and fine-tune the learning rate schedules of each model to obtain the best detection mAP. All our proposed models process the first four layers (convolutional+BN+ReLU+pooling) inside the sensors and the remaining layers in the back-end, while the baseline models process the entire neural network in the back-end.

### Table II

| Model            | $S$ | $S'$ | mAP (%) (IoU=0.5) | mAP (%) (IoU=0.75) | mAP (%) (IoU=0.5-0.95) |
|------------------|-----|------|------------------|-------------------|------------------------|
| Faster R-CNN     | Max | 2    | 57.5             | 33.2              | 33.7                   |
| P$^2$M-DeTrack 6 | Max | 2    | 56.5             | 29.2              | 33.2                   |
| P$^2$M-DeTrack 6 | Avg | 2    | 55.5             | 31.7              | 32.3                   |
| P$^2$M-DeTrack A | Avg | 2    | 53.5             | 30.3              | 31.1                   |

1We observe that dropping every other frame does not lead to any degradation in the tracking IDF1 score for the BDD100K dataset.

2Note that fewer pixels need 64 weight transistors for a stride of 6 than for a stride of 4.
Fig. 3. Comparison of object detection mAP for various stride and channel counts of the in-pixel convolutional layer.

![Comparison of object detection mAP](image)

**TABLE III**

| Model         | 1s | mapOTA mm | mIDF1 | FN | FP | ID SW | mAP |
|---------------|----|------------|-------|----|----|-------|-----|
| QDTrack       | 1  | 36.6       | 50.8  | 63.5 | 71.5 | 108614 | 46621 |
| P^2-M-DeTrack | 2  | 34.0       | 49.7  | 62.4 | 70.7 | 119256 | 41466 |
| P^2-M-DeTrack | 6  | 34.2       | 49.1  | 61.8 | 70.3 | 122691 | 40480 |

**MULTI-OBJECT TRACKING (MOT) METRICS OF THE BASELINE FASTER R-CNN-BASED QDTRACK AND P^2-M-DETRACK MODELS FOR DIFFERENT IN-PIXEL CONVOLUTIONAL AND POOLING STRIDES.**

above 6. Note that we also increase the kernel size (i.e., make the kernel size equal to stride) to support strides of 8 and 12.

**D. Tracking Results**

The detailed breakdown of our tracking results on the BDD100K multi-object tracking (MOT) validation set are shown in Table III. Our P^2-M-DeTrack models achieve 49.7% mIDF1 (stride 2, pool 2) and 49.1% mIDF1 (stride 6, pool 2, followed by upsampling), both of which are comparable to the SOTA 50.8% mIDF1 obtained by QDTrack [23].

**E. Reduction in Energy Consumption**

As described in [7], the total energy consumption for both P^2-M-DeTrack and conventional baseline models can be partitioned into three major components, sensor ($E_{sens}$), sensor-to-SoC communication ($E_{com}$), and SoC energy ($E_{soc}$) as captured in Eq. 4. Note that $E_{sens}$ is the sum of the pixel array energy and the ADC energy; both are obtained from circuit simulations using commercial Globalfoundries 22nm FD-SOI technology node. $E_{com}$ is computed from $e_{com}$ as shown in Eq. (4), and its value shown in Table IV is obtained from [15]. On the other hand, $E_{soc}$ is primarily dominated by multiply-and-add (MAdd) energy of the models used for detection ($E_{mac}$).

\[
E_{tot} \approx (e_{pix} + e_{adc}) \cdot N_{pix} + e_{com} \cdot N_{pix} + e_{mac} \cdot N_{mac}
\]

Fig. 4 shows the normalized energy comparison between P^2-M-DeTrack and baseline detection models. In particular, the in-pixel architecture is estimated to reduce the sensing energy by up to $5.7 \times$ with a total energy improvement of $1.14 \times$. Note, in Eq. 4, $N_{pix}$ and $N_{mac}$ corresponds to the total number of pixels needed to be processed in-in pixel and total MAC operations [16] for the back-end model, respectively. We note that the dominating back-end can be often over-parameterized and thus various off-the-shelf model compression [17], [24] can be deployed to further reduce the back-end computation cost. This, in turn, can further reduce the total energy.

**F. Reduction in Delay**

The delay associated with the detection pipeline can be partitioned into four components, sensing delay ($\tau_{sens}$), ADC delay ($\tau_{adc}$), communication delay ($\tau_{com}$), and backend delay ($\tau_{back}$) as shown below

\[
\tau_{delay} \approx \tau_{sens} + \tau_{adc} + \tau_{com} + \tau_{back}
\]

We use the per-pixel communication delay from [9] to estimate the delay required to send the output activation maps from sensor to SoC ($\tau_{com}$). While $\tau_{sens}$ is primarily governed by the sensor read delay, $\tau_{adc}$ is associated with the total number of ADC clock cycles required to generate the first layer output activation map, dictated by our P^2-M-DeTrack parallelism approach discussed in Section III-A. Note that both of these values are computed from our circuit simulations.

$\tau_{back}$ was computed by the Xilinx FINN-based [29] FPGA simulation framework targeting the Xilinx Alveo U250 platform with a maximum clock frequency of 300 MHz, which was modified to include the QSFP+ high-speed transceiver for streaming purposes. Our framework utilizes High-Level Synthesis (HLS) to translate the developed PyTorch model into a synthesizable RTL to generate a bitstream for the target Alveo U250 device. The HLS flow evaluates the network layers, splits each layer into submodules, and applies transformations to aid in the HLS conversion process. These transforms are intended to optimize the HLS process by enabling FPGA-friendly quantization, pipeline the FIFO insertions, and implementations for efficient memory (BRAM, URAM and LUTRAM) and processing (DSP) for all layers. The resulting model is stitched back together in RTL submodules and run through synthesis, place-and-route, leading to the final bitstream generation. This process allows for refining individual modules and stages with HLS and analyzing latency and resource utilization for the system bottlenecks.

The resulting inference latency through the system implementing only the CNN backbone is 15.5 ms. The resource utilization is 60% LUTs, 30% Flip-Flops, 13% DSPs, 60% BRAMs, 10% LUTRAMs and 2% URAMs. The power utilization is 70W based on default switching models as reported by the Xilinx Vivado tools. Augmenting the baseline ResNet-50 model to our proposed custom network with the first convolutional, BN, ReLU, and pooling layers removed, results in a 1.15x improvement in latency, down to 13.5 ms. As shown in Fig. 4, the total delay improvement for in-pixel architecture is

| Notation | Description                  | Value       |
|----------|------------------------------|-------------|
| $e_{pix}$ | Sensing energy/#pixel        | 148 pJ (P^2-M) |
| $e_{adc}$ | ADC energy/#pixel            | 312 pJ (baseline) |
| $e_{com}$ | SoC comm. energy/#pixel      | 900 pJ (P^2-M) |
| $e_{mac}$ | MAdd energy in 22nm technology | 1.588 pJ (baseline) |
estimated to be up to \(\sim 3 \times\). In particular, the proposed P²M-DeTrack model can yield an improved \(~17\) FPS compared to the baseline’s \(~9.6\) FPS, which may be acceptable for real-time detection and tracking in an autonomous driving scenario.

Note that the FPS can be further improved by using faster pixels or by designing and leveraging more than one ADC per column. For example, using 2 ADCs per column can double the FPS at the cost of only modest increase in area.

V. CONCLUSIONS AND DISCUSSIONS

This work proposes P²M-DeTrack, a processing-in-pixel-in-memory-based algorithm-hardware co-design framework that can reduce the EDP cost of a complex object detection and tracking pipeline by up to \(3.42\times (3 \times\) reduction in latency for a \(14\%\) reduction in energy) compared to existing in-sensor processing approaches. Our hardware modifications can be readily integrated into the foundry-manufacturable CMOS image sensor platforms, and our hardware-inspired algorithmic modifications are shown to yield negligible performance drop in multi-object detection and tracking.

It is important to note that the energy metric presented in this work is based on the assumption that the front-end and back-end chips are closely located on the same printed-circuit board [15]. In general, the front-end and back-end sensors could be separated by large distances, necessitating long energy-expensive wired or wireless data transfer (which is common for the case of sensor-fusion and swarm intelligence applications). In such cases the overall energy improvement would approach the bandwidth reduction (up to \(24\times\)) obtained from the proposed P²M-DeTrack scheme.

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