Current Sharing Analysis for Novel Paralleled CLLLC Converters

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This work was supported in part by the NSFC Project of China under Grant 61963030, and in part by the NSF Project of Jiangxi, China, under Grant S2019QNZD2B0113.

ABSTRACT In the field of high-capacity bidirectional converters, paralleled LLC converters are usually used to increase the output power and system power density. However, because of the production tolerances the parameters of the resonant components for each paralleled unit may not be completely identical. The gain characteristic of the LLC resonant converter is sensitive to the parameters of the resonant components. For the paralleled converters, because voltage gains can be slightly different from each other for a same input, system output current may be poorly shared among the parallel units. In this paper, novel paralleled CLLLC converters are proposed. For the proposed converters, the load current sharing performance is not sensitive to component parameter differences or derivations. Equal load sharing can be realized easily. And no additional components or controllers are needed. The gain characteristics are analyzed and they are similar with that of a single CLLLC resonant converter. The mathematical model of the paralleled converters is deduced based on fundamental harmonic approximation (FHA) method. And the load current sharing errors for the conventional and proposed paralleled CLLLC converters are compared or analyzed by introducing variables such as the load current sharing coefficient. It is shown that for the same set of component parameters, when the conventional paralleled converters are used most of the load may be supported by a single converter while the output power of another one is small. On the other hand, for the cases of parameter derivations, the current sharing performance of the novel proposed paralleled converters is obviously much better. And finally the effectiveness of current sharing for the proposed paralleled CLLLC converters is verified by simulations and experiments.

INDEX TERMS Current sharing, paralleled CLLLC converters, component parameter derivation, equivalent circuit.

I. INTRODUCTION
Since the isolated dc-dc converter has the advantages of electric isolation and high power density, it is widely used in many power applications such as battery charger, automobiles and so on [1]–[3]. In recent years, LLC resonant converter has been proposed to improve power conversion efficiency since the converter can naturally achieve zero voltage switching (ZVS) for the primary side and zero current switching (ZCS) for the secondary side [4]–[6]. By replacing diodes in the secondary side with MOSFETs, bidirectional power conversion can be realized [7], [8]. In order to increase system output power, converters are usually parallel connected [9], [10]. However, due to the tolerances in the production process, the parameters of each unit cannot be identical [11], [12]. This may cause unequal current sharing, and sometimes it may ruin the system since some units may be overloaded. Therefore equal current sharing is essential for the paralleled LLC resonant converters. In this paper, novel paralleled converters are proposed which can realize equal load current sharing.

Some technologies have been developed for current sharing. There are mainly two categories. One is the active method. This method is to adjust switching frequencies or resonant parameters by detecting the current of each unit to realize satisfying current sharing [13]–[15]. For instance, in [14] a new control strategy is proposed for paralleled interleaved SCC-LLC converters, and satisfying load current sharing performance can be achieved. On the other hand, the active methods should use the current sampling circuits for every unit. These circuits make the whole system unreliable. It also costs more. The other category is the passive current sharing
method which is to achieve equal current sharing by using passive components [16], [17]. In [18], [19] converters with series input capacitors are presented. These converters own good current sharing characteristics, while the input of each unit is only \(1/n\) of the input voltage of the whole system and \(n\) is the unit number. But for the case of parallel connection, load current sharing may be poorer. In [20] Y-connected three interleaved and paralleled LLC resonant converters are presented and the load current is well shared. However, when the number of parallel units is more than three, the current sharing performance may deteriorate. In [21] paralleled LLC resonant converters are presented with a common resonant inductor or capacitor. Good current sharing performances can be achieved. However, a common inductor increases the system design complexity and also further research may be needed in regard with the gain characteristics of the system.

On the other hand, the converters discussed above can only realize single-direction energy conversion. For many application cases, energy may be transferred back to the input side batteries or capacitors. But the soft switching and gain characteristics cannot be guaranteed during reverse operation mode. A CLLLC type resonant converter with a series LC branch in the secondary side has been proposed to solve these problems [22], [23]. Because of its symmetrical construction, it can naturally realize ZVS and ZCS soft switching for forward or reverse modes. But as mentioned above, for high-capacity applications the capacity of a single CLLLC resonant converter is limited. As shown in Fig. 1, paralleling the power modules is often used to increase system capacity. To cope with the load current sharing problem mentioned above, in this paper a novel paralleled bidirectional CLLLC converter is proposed. It is shown that equal load current sharing can be realized for the proposed paralleled CLLLC converters. But for the traditional paralleled converters, the current sharing performance is much poorer. The main contributions of this paper are as follows.

a. No additional components are needed. By connecting CLLLC converters as in Fig. 1, load current can be shared equally among the parallel units, even the component parameters of the converters are different from each other. On the other hand, when CLLLC converters are connected in the conventional way as in Fig. 6, equal load sharing cannot be guaranteed and as the result some units may be overloaded.

b. The mathematic models for the proposed paralleled converters and the conventional one are deduced and analyzed. The 3-D gain surface for the new converters is obtained which is beneficial for system design. And it is proved that the gain properties of the proposed paralleled CLLLC converters are similar with those of a single converter. By introducing variables, i.e., the load sharing coefficient \(\lambda\) and current sharing error, the load current sharing error curves are illustrated indicating the effectiveness of the proposed paralleled converters.

The rest of this paper is organized as follows: in section II, the gain characteristic of the proposed converters is obtained, and the current sharing performance is analyzed based on fundamental harmonic approximation (FHA) method. In section III, by introducing variables such as load current sharing error, the current sharing performances for the proposed and conventional paralleled converters are analyzed. In order to verify the effectiveness of the proposed paralleled converters, the simulation and experiment results are presented in section IV and V respectively. Conclusions are offered in section VI.

![FIGURE 1. The proposed paralleled CLLLC resonant converter.](image1)

![FIGURE 2. The proposed paralleled CLLLC converters and its switch gate drive signals, (a) the circuit of the proposed paralleled CLLLC converters, (b) the gate drive signals.](image2)
According to (1)-(4), the transfer function of $V_{in}(s)$ to $V_{out}(s)$ can be derived as in (5), shown at the bottom of the page, where $R_{ac} = \left(8\eta^2/\pi^2\right)R_{load}$. Let $s = j\omega$, $L_m = gL_r$, $\omega_r = 1/\sqrt{L_rC_r}$, the normalized angular frequency and quality factor are listed in (6):

\[
\begin{align*}
\omega_n &= \frac{\omega_0}{\omega_r} \\
Q &= \sqrt{L_r/C_r} / R_{ac}
\end{align*}
\]  

(6)

According to (5) and (6), the gain $G$ of the proposed paralleled converters in Fig. 2 (a) can be derived in (7):

\[
G = \left| \frac{V_{out}(s)}{V_{in}(s)} \right| = \left| x_n X + jY \right| 
\]

(7)

where

\[
\begin{align*}
x_n &= g(1 + b)^2 \left(2acg + a^2 + 2cg + c \right) \\
X &= x_{dR1} + x_{dR2} \frac{1}{\omega_0^2} \\
Y &= Q \left( x_{dL1}\omega_n + x_{dL2} \frac{1}{\omega_n} + x_{dL3} \frac{1}{\omega_0^2} \right) \\
x_{dR1} &= (1 + b)^2 \left(2acg^2 + a^2g + 2cg + c \right) \\
x_{dR2} &= -2g(c + 1)(ab + a + b) - (b + 1)(a + 1)^2 \\
x_{dL1} &= a(1 + b)^2(2cg + 1)(2g + 1) \\
x_{dL2} &= -2(1 + b)cg(2ga + 2g + 2a + 1) \\
x_{dL3} &= (1 + a)(a + cg + g + 1)
\end{align*}
\]

(8)

FIGURE 4. The simplified circuits of the proposed paralleled CLLLC converters.

to analyze the gain for the forward mode. Fig. 3 shows the FHA equivalent circuit of the proposed paralleled converters. Since it is not easy to evaluate $V_{out}(s)$ according to Fig. 3, $\Delta - Y$ transformation is used here to simplify the circuit and the resulted circuit is shown in Fig. 4. The related equivalent impedances can be derived in the following equations (1)-(4):

\[
\begin{align*}
Z_{10}(s) &= \frac{s(2L_m + L_r)}{L_m} \\
Z_{12}(s) &= \frac{s(2L_m + L_r)}{L_m} \\
Z_{21}(s) &= \frac{s(2L_m + aL_r)}{L_m} \\
Z_{22}(s) &= \frac{s(2L_m + aL_r)}{cL_m} \\
Z_{23}(s) &= \frac{s(2L_m + aL_r)}{L_m} \\
Z_1(s) &= Z_{11}(s)/Z_{22}(s) \\
Z_2(s) &= Z_{12}(s)/Z_{22}(s) \\
Z_3(s) &= Z_{13}(s)/Z_{22}(s)
\end{align*}
\]

(1)

\[
\begin{align*}
Z_1^*(s) &= \frac{Z_1(s) \cdot Z_2(s)}{Z_1(s) + Z_2(s) + Z_3(s)} \\
Z_2^*(s) &= \frac{Z_1(s) \cdot Z_2(s)}{Z_1(s) + Z_2(s) + Z_3(s)} \\
Z_3^*(s) &= \frac{Z_1(s) \cdot Z_2(s)}{Z_1(s) + Z_2(s) + Z_3(s)}
\end{align*}
\]

(2)

\[
\begin{align*}
V_{out}(s) &= \frac{Z_1^*(s) \cdot Z_2^*(s) \cdot Z_3^*(s) \cdot R_{ac} \cdot V_{in}(s)}{Z_1^*(s) \cdot Z_2^*(s) + R_{ac} + \frac{1}{(1+\theta)\omega_0^2} + Z_3^*(s) + Z_3^*(s) + R_{ac} + \frac{1}{(1+\theta)\omega_0^2}}
\end{align*}
\]

(5)
load is larger and its gain curve surface becomes flatter even the switching frequency is low. The gain is decreasing for heavy load. For the proposed paralleled CLLLC converters, properties of the gain curve are similar to that of a single CLLLC resonant converter.

For the proposed converter, the design process of the resonant inductor, capacitor, transformer and other parameters is the same as the traditional CLLLC converters. And can be referred in [22], [23] and other literatures. In this paper it is omitted for the sake of brevity.

III. CURRENT SHARING ANALYSIS

Because of the symmetrical structure of the proposed bidirectional converters, we just need to analyze the current sharing for the forward mode. For the two paralleled converters, the load sharing coefficient \( \lambda \) is defined as in (9):

\[
\lambda = \frac{P_{o1}}{P_{o1} + P_{o2}} = \frac{P_{o1}}{P_{o}}
\]

where \( P_{o1}, P_{o2} \) are the output power of paralleled unit 1 and 2, and \( P_{o} \) is the total output power.

The load sharing coefficient \( \lambda \) is valid in \([0, 1] \). \( \lambda = 0 \) or \( \lambda = 1 \) mean one of the parallel units support all the load and the other one provides none. When \( \lambda \) equals 0.5, it means that the two parallel converters share the load equally.

A. CURRENT SHARING ANALYSIS FOR THE CONVENTIONAL PARALLELED CLLLC CONVERTERS

In Fig. 6, two conventional CLLLC converters are parallel connected. The gate drive signals are as same as those of the proposed converters as in Fig. 2(b). In a switching period, the average value of \( i_{o1} \) and \( i_{o2} \) can be obtained as in equation (10):

\[
\begin{align*}
    i_{o1} &= \frac{2}{T_s} \int_{t_1}^{t_2} i_{o1} dt = \frac{P_{o1}}{V_o} \quad \text{(10)} \\
    i_{o2} &= \frac{2}{T_s} \int_{t_1}^{t_2} i_{o2} dt = \frac{P_{o2}}{V_o}
\end{align*}
\]

where \( T_s \) is the switching period, \( V_o \) is the dc output voltage as in Fig. 6, \( i_{o1} \) is the average value of output current \( i_{o1} \), \( i_{o2} \) is the average value of \( i_{o2} \). The equivalent load of each unit can be described in (11):

\[
\begin{align*}
    R_{load1} &= \frac{V_o^2}{P_{o1}} = \frac{V_o^2}{\lambda P_o} \\
    R_{load2} &= \frac{V_o^2}{P_{o2}} = \frac{V_o^2}{(1-\lambda) P_o}
\end{align*}
\]

where \( R_{load1} \) is the equivalent load of unit 1, \( R_{load2} \) is the equivalent load of unit 2. And \( R_{load} \) can be expressed as (12):

\[
R_{load} = \frac{V_o^2}{P_o}
\]

According to (11) and (12), \( R_{load1} \) and \( R_{load2} \) can be further expressed as (13):

\[
\begin{align*}
    R_{load1} &= \frac{R_{load}}{\lambda} \\
    R_{load2} &= \frac{R_{load}}{1-\lambda}
\end{align*}
\]

Then the decoupled FHA equivalent circuits of the conventional paralleled CLLLC converters can be obtained as in Fig. 7. \( R_{ac1} \) and \( R_{ac2} \) are the decoupled ac equivalent resistors and they can be calculated as (14):

\[
\begin{align*}
    R_{ac1} &= \frac{\pi^2 R_{load1}}{8} \\
    R_{ac2} &= \frac{\pi^2 R_{load2}}{8}
\end{align*}
\]

The Thevenin equivalent circuits are shown in Fig. 8. \( Z_1 \) and \( Z_2 \) are the equivalent impedances of unit 2 and unit 2. And \( V_{ac1}, V_{ac2} \) are the equivalent input voltages. \( V_{oc1}, V_{oc2}, Z_1 \) and \( Z_2 \) can be expressed as in (15)-(18):

\[
\begin{align*}
    V_{oc1} &= \frac{Z_m1}{Z_m1 + Z_{11}} V_{in} \\
    Z_1 &= \frac{Z_m1Z_{11}}{Z_m1 + Z_{11} + Z_{12}} \\
    V_{oc2} &= \frac{Z_m2}{Z_m2 + Z_{21}} V_{in} \\
    Z_2 &= \frac{Z_m2Z_{21}}{Z_m2 + Z_{21} + Z_{22}}
\end{align*}
\]

where

\[
\begin{align*}
    Z_{11} &= j\omega L_{Lr} + \frac{1}{j\omega C_r} \\
    Z_{m1} &= j\omega L_m
\end{align*}
\]
Then the output voltages of the decoupled circuits for the conventional paralleled CLLLC converters, i.e., $V_{\text{out}1}$ and $V_{\text{out}2}$, can be derived as (21):

$$
\begin{align*}
V_{\text{out}1} &= \frac{n^2 R_{\text{ac}1}}{Z_1} V_{\text{oc}1} + \frac{n^2 R_{\text{ac}1}}{Z_2} V_{\text{oc}2} \\
V_{\text{out}2} &= \frac{n^2 R_{\text{ac}2}}{Z_1} V_{\text{oc}1} + \frac{n^2 R_{\text{ac}2}}{Z_2} V_{\text{oc}2}
\end{align*}
$$

(21)

According to (9), (10), then $\lambda$ also can be expressed as in (22):

$$
\lambda = \frac{I_{o1}}{I_{o1} + I_{o2}}
$$

(22)

In order to evaluate the current sharing performance of the converters, the load current sharing error $\delta_o$ is defined as in (23):

$$
\delta_o = \frac{|I_{o1} - I_{o2}|}{I_{o1} + I_{o2}} = \text{abs}(1 - 2\lambda)
$$

(23)

Since $\omega_s = 2\pi f_s$, $R_{\text{ac}} = \sqrt{L_r/C_r}$, $R_{\text{ac}1} = R_{\text{ac}}/\lambda$ and $R_{\text{ac}2} = R_{\text{ac}}/(1 - \lambda)$, the output voltages $V_{\text{out}1}$ and $V_{\text{out}2}$ can be determined by $f_s$, $Q$ and $\lambda$. Because the output of each unit has been connected together, the amplitude of the reflected output voltages of both units should be the same [21]. It means that the absolute values of the ac equivalent output voltages of both units are equal. Let $|V_{\text{out}1}| = |V_{\text{out}2}|$ directly, a quadratic equation about $\lambda$ can be obtained as in (24):

$$
\sqrt{\frac{V_{\text{oc}1}^2 Z_1^2}{Z_2^2} (1 - \lambda)^2 + \frac{V_{\text{oc}1}^2 n^4 R_{\text{ac}}^2}{Z_2^2}} = \sqrt{\frac{V_{\text{oc}2}^2 Z_1^2 \lambda^2}{Z_2^2} + \frac{V_{\text{oc}2}^2 n^4 R_{\text{ac}}^2}{Z_2^2}}
$$

(24)

However, for some switching frequencies and values of $Q$, the quadratic equation (24) may have no solution. In Fig. 9 are the curves of $|V_{\text{out}1}|$ and $|V_{\text{out}2}|$ versus $\lambda$ with fixed $f_s$ and $Q$. If the curves $|V_{\text{out}1}|$, $|V_{\text{out}2}|$ intersect at point $P$, the corresponding $\lambda_p$ is the solution of equation (24). Otherwise, there are two cases: (1) $|V_{\text{out}1}| > |V_{\text{out}2}|$: $\lambda$ is equal to 1 which means that the whole load is supplied by unit 1; (2) $|V_{\text{out}1}| < |V_{\text{out}2}|$: in this case $\lambda$ becomes 0 and the whole load is supplied by unit 2.

Define $L_r$, $C_r$, $L_m$ as the resonant inductor, resonant capacitor and magnetizing inductor of unit 1. And the parameters of unit 2 are $aL_r/bC_r/cL_m$, where $a/b/c$ reflects the production tolerance by 5%.
According to equation (23), the current sharing errors of the conventional paralleled converters can be depicted as in Fig. 10. Case 1 is shown in Fig. 10(a) where \( a=1, b=1, c=1 \); case 2 is shown in Fig. 10(b) where \( a=1, b=1.05, c=1 \); case 3 is shown in Fig. 10(c) where \( a=1, b=1, c=1.05 \); case 4 is shown in Fig. 10(d) where \( a=1.05, b=1.05, c=1.05 \).

It can be seen from Fig. 10(a)–(d) that when the switching frequency \( f_s \) is smaller or larger than the resonant frequency \( f_r \), the current sharing errors decrease as \( Q \) increases. When the switching frequency is near \( f_r \), no matter how \( \lambda \) becomes, \( |V_{out1}| \) and \( |V_{out2}| \) are slightly affected. Then for Fig. 9, when \( f_s \) is close to \( f_r \), \( \lambda_p \) will be far away from 0.5. Or the two curves may not intersect at all. It means that system load is not equally shared.

For case 3, since \( a=1, b=1, \) and \( c=1.05 \), the resonant frequencies of both units are the same. Therefore when the switching frequency is equal to \( f_r \), no matter how the load changes, the AC equivalent output voltages of unit 1 and unit 2 are equal. Then the load current sharing coefficient \( \lambda \) is 0.5. And the current sharing error \( \delta_o \) for case 3 is 0 when \( f_s = f_r \) as in Fig. 10(c).

From the analyses above, when \( f_s \) is much higher or lower than \( f_r \), \( \delta_o \) may become smaller. However, for the CLLLC resonant converters, when the switching frequency is too low the voltage gain becomes very high. And the output current ripple is large. When the switching frequency is high, the gain of the CLLLC converter is low and ZCS cannot be realized for the secondary side.

**B. CURRENT SHARING ANALYSIS FOR THE PROPOSED PARALLELED CLLLC CONVERTERS**

The analysis of the proposed paralleled CLLLC converters is similar to that for the conventional converters. The gate drive signals of the proposed converters are shown in Fig. 2(b). The paths for \( i_{o1}/i_{o2} \) intervals \([t_1, t_2]/[t_3, t_4]\) are different. And they are shown in Fig. 11 and Fig. 12. The commutation state of \([t_1, t_2]\) is defined as mode 1 and the commutation state of \([t_3, t_4]\) is defined as mode 2.

**FIGURE 11. The commutation stage of mode 1 during \([t_1, t_2]\).**

For mode 1, the decoupled FHA equivalent circuit can be obtained as in Fig. 13. Its Thevenin equivalent circuit is shown in Fig. 14. The equivalent impedances \( Z_{pro11}, Z_{pro21} \) and equivalent voltages \( V_{pro, oc11}, V_{pro, oc21} \) of the two units can be obtained as in (25)–(28):

\[
V_{pro, oc11} = \frac{L_m}{L_m + L_r} (V_{in} - V_{cr1}) \tag{25}
\]

\[
Z_{pro11} = \frac{j\omega_a L_m L_r}{L_m + L_r} + j\omega a^2 L_r \tag{26}
\]

\[
V_{pro, oc21} = \frac{c_{lm}}{c_{lm} + a_L} (V_{in} - V_{cr1}) \tag{27}
\]

\[
Z_{pro21} = \frac{j\omega a c_L L_m L_r}{c_{lm} + a_L} + j\omega a^2L_r \tag{28}
\]

Equation (29) can be derived by Kirchhoff Laws. And \( I_1, I_2 \) in Fig. 14 can be obtained as (30). Then the equivalent output voltages \( V_{pro, ou11} \) and \( V_{pro, ou21} \) of mode 1 can be obtained as (31):

\[
\begin{align*}
\{V_{pro, oc1} &= a_{11} I_1 + a_{12} I_2 \\
V_{pro, oc2} &= a_{21} I_1 + a_{22} I_2 \\
I_1 &= \frac{a_{22} V_{pro, oc1} - a_{12} V_{pro, oc2}}{a_{22} a_{11} - a_{12} a_{21}} \\
I_2 &= \frac{a_{21} V_{pro, oc1} - a_{11} V_{pro, oc2}}{a_{12} a_{21} - a_{11} a_{22}}
\end{align*}
\tag{30}
\]
Similarly the equivalent decoupled circuit for mode 2 is shown in Fig. 15. The related Thevenin equivalent circuit is shown in Fig. 16.

For mode 2, the equivalent output voltages, i.e., \( V_{\text{pro, out1}} \) and \( V_{\text{pro, out22}} \), can be obtained as follows:

\[
Z_{\text{pro}} = \left( n^2 R_{\text{ac1}} + \frac{1}{j \omega C_r} \right) / \left( n^2 R_{\text{ac2}} + \frac{1}{j \omega b C_r} \right) \tag{34}
\]

For comparison the electric component parameters in Table 1 are used. According to (37), the curves of current sharing error of the proposed CLLLC converters can be obtained as in Fig. 17. Case1 is shown in Fig. 17(a) where \( a=1.05, b=1, c=1 \); case2 is shown in Fig. 17(b) where \( a=1, b=1.05, c=1 \); case3 is shown in Fig. 17(c) where \( a=1, b=1, c=1.05 \); case4 is shown in Fig. 17(d) where \( a=1.05, b=1, c=1.05 \). From Fig. 17 (a) and (c), it can be seen that when the switching frequency increases, the current sharing error decreases. And for the same switching frequency, the load current sharing error \( \delta_{\text{pro}} \) decreases with increasing \( Q \). Fig. 17(b) shows the current sharing errors of case2. The resonant inductors and the magnetizing inductors of both units are the same. Hence, for mode 1, the secondary side capacitors of unit 1 and unit 2 are paralleled. The difference between the resonant capacitors does not affect the load current sharing error. Then \( \lambda_{\text{pro1}} \) becomes 0.5. As stated above, \( \lambda_{\text{pro2}} \) is equal to \( b/(1+b) \) which is a constant. Therefore the load current sharing error \( \delta_{\text{pro}} \) of the proposed converters can be obtained as 0.0122. Fig. 18(d) shows the current sharing error of the proposed converters.

| Table 1. Simulation parameters. |
|--------------------------------|
| Transformer Ratio | 1.056:1 |
| Output Capacitor | 880\mu F |
| Resonant Capacitor (\( C_r \)) | 209\mu F (unit1) |
| Resonant Inductor (\( L_r \)) | 220\mu H (unit1) |
| Magnetizing Inductor (\( L_m \)) | 11.4\mu H (unit1) |
| Load \( R_{\text{out}} \) | 12\mu H (unit2) |
| Output Voltage | 250\Omega/35\Omega |

\[
V_{\text{AB}} = V_{\text{pro, out12}} \left( \frac{Z_{\text{pro22}}/Z_{\text{pro}}}{Z_{\text{pro12}}/Z_{\text{pro}}} + Z_{\text{pro12}} \right)
+ V_{\text{pro, out22}} \left( \frac{Z_{\text{pro12}}/Z_{\text{pro}}} {Z_{\text{pro12}}/Z_{\text{pro}}} + Z_{\text{pro22}} \right)
\tag{35}
\]

\[
V_{\text{pro, out12}} = V_{\text{AB}} \left( R_{\text{ac1}} + \frac{1}{j \omega C_r} \right)
R_{\text{ac2}} + \frac{1}{j \omega b C_r}
\tag{36}
\]
errors of case 4. In mode 1, according to equations (25) to (32), \( V_{\text{pro},\text{oc}11} \) and \( V_{\text{pro},\text{oc}21} \) are equal and \( |Z_{\text{pro}21}/Z_{\text{pro}21}| \) is a constant. For this case, the load sharing coefficient \( \lambda_{\text{pro}1} \) is a constant value 0.5122 and the current sharing error \( \delta_{\text{pro}} \) is 0.0243.

Comparing with Fig. 10, the load current sharing error of the proposed converters decreases when the switching frequency increases. From Fig. 17 (a) and (b), it can be seen that when \( Q \) is 0.1 or the load is light, the current sharing error \( \delta_{\text{pro}} \) is larger. When \( Q \) is larger than 0.3, for the 4 cases the current sharing error \( \delta_{\text{pro}} \) becomes very small and smooth for the entire switching frequency range. In order to further illustrate the effectiveness of the proposed paralleled CLLLC converters, another set of randomly chosen parameters are used (Case 5), i.e., \( a=0.98; b=1.02; c=1.05 \). And the load current sharing error curves are shown in Fig. 18. It can be seen that the current sharing performance is similar to those discussed above. It further illustrates that the proposed converters can effectively solve the problem of poor current sharing near the resonant frequency. And the paralleled converters can realize PFM frequency modulation control while ensuring good current sharing performance.

**IV. SIMULATIONS**

In this section we test the effectiveness of the proposed paralleled converters by PLECS software. Table 1 shows the simulation parameters. Simulations have been conducted for the converters in Fig. 2 and Fig. 6 with the output loads being 25Ω and 35Ω.

Fig. 19 and 20 are the waveforms for the conventional paralleled converters. Fig. 19(a) and Fig. 20(a) are the results when \( R_{\text{load}} \) is 25Ω or 35Ω for the forward operation mode. It can be seen that the resonant current \( i_{r2} \) of unit 2 is almost identical to the magnetizing current. That means unit 2 is working nearly with no output power. And system load is mainly supplied by unit 1. The waveforms of the conventional converters for the reverse operation mode are shown in Fig. 19(b) and Fig. 20(b). Similarly, for the reverse operation mode, the output current \( i_{o2} \) of unit 2 is almost zero.
FIGURE 19. Simulation waveforms of the conventional paralleled CLLLC converters when $R_{\text{load}} = 25\Omega$: (a) Forward operation mode; (b) Reverse operation.

Unit 1 supplies the entire load. In practical applications, this may ruin the system.

Fig. 21 and Fig. 22 are the simulation waveforms of the proposed paralleled CLLLC converters. In Fig. 21(a) and Fig. 22(a) are the waveforms for forward operation mode when $R_{\text{load}}$ is 25\Omega or 35\Omega. It can be seen from the results that the resonant currents and the output currents of both units are almost equal. Unit 1 and 2 share the load well. The reverse operation waveforms are shown in Fig. 21 (b) and Fig. 22 (b). Likewise, the proposed converters can achieve equal current sharing too. Comparing with the simulation results in Fig. 19 and 20, the current sharing performance has been greatly improved.

FIGURE 20. Simulation waveforms of the conventional paralleled CLLLC converters when $R_{\text{load}} = 35\Omega$: (a) Forward operation mode; (b) Reverse operation.

V. EXPERIMENTS

In Fig. 23 a 2kW experiment platform has been set up to test the effectiveness of the proposed paralleled CLLLC resonant converters. Table 2 shows the parameters of main components.

A. FORWARD OPERATION MODE

In Fig. 24 and Fig. 25 are the experiment results of the conventional paralleled converters for forward operation mode with different loads. It can be seen that for $R_{\text{load}}$ being 25\Omega or 35\Omega, unit 1 does not supply power for the load and all the output power is supported by unit 2. According to the experiment waveforms, when $R_{\text{load}} = 25\Omega$, the average $i_{o1}$ is 32mA. The average $i_{o2}$ is 7.69A and the current sharing error $\delta_o$ is 0.9917. Similarly when $R_{\text{load}} = 35\Omega$, the current sharing error is 0.9957.
In Fig. 26 and Fig. 27 are the experiment waveforms of the proposed paralleled converters for forward operation mode with different loads. It can be obviously seen that the proposed converters can achieve much better current sharing. The output power can be shared by unit 1 and unit 2 equally.

According to the experiment results, when $R_{\text{load}} = 25\Omega$, the average $i_{o1}$ is 3.8954A. The average $i_{o2}$ is 3.8694A and the current sharing error $\delta_{\text{pro}}$ is 0.0014. When $R_{\text{load}} = 35\Omega$, the average $i_{o1}$ is 2.7590A. The average $i_{o2}$ is 2.8475A and
the current sharing error $\delta_{\text{pro}}$ is 0.015. In Table 3 are the experiment data of the current sharing errors of the two kinds of paralleled converters for forward operation mode with different loads.

B. REVERSE OPERATION MODE

In Fig. 28 and Fig. 29 are the experiment results of the conventional paralleled converters for reverse operation mode with different loads. When $R_{\text{load}}$ is 25$\Omega$, the average $i_{\text{o1}}$ is 15mA. The average $i_{\text{o2}}$ is 7.8821A and the current sharing error $\delta_{o}$ is 0.9962. Similarly when $R_{\text{load}} = 35\Omega$, the current sharing error is 0.9919.

In Fig. 30 and Fig. 31 are the experiment waveforms of the proposed paralleled converters for reverse operation mode with different loads. Whether $R_{\text{load}}$ is 25$\Omega$ or 35$\Omega$, the proposed converters can achieve much better current sharing as
well. When $R_{\text{load}} = 25\Omega$, the average $i_{o1}$ is 3.9214A. The average $i_{o2}$ is 3.9194A and $\delta_{\text{pro}}$ is 0.00026. Likewise when $R_{\text{load}} = 35\Omega$, the average $i_{o1}$ is 2.8272A. The average $i_{o2}$ is 2.8185A and $\delta_{\text{pro}}$ is 0.0015. Table 4 shows the experiment data for the reverse operation mode.

According to the simulation and experiment results, the conventional paralleled CLLLC converters poorly share the load and this may deteriorate system’s reliability. The proposed paralleled converters solve this problem and no matter how the load changes, good current sharing performance can be achieved.

Fig. 32 shows the efficiency of the proposed paralleled CLLLC converters. For forward or reverse operation modes, the proposed converters can achieve high efficiency. In practical applications, this topology can be used to increase output power and improve the reliability of the system.
TABLE 3. Current sharing errors for the two kinds of paralleled CLLLC converters for forward operation mode.

| Output power |  |  |
|--------------|--------------|--------------|
|              | $\delta_c$ for conventional paralleled converters | $\delta_c$ for proposed paralleled converters |
| 627W         | 1            | 0.0916       |
| 800W         | 1            | 0.0326       |
| 1143W        | 0.9957       | 0.015        |
| 1369W        | 0.9924       | 0.0081       |
| 1600W        | 0.9917       | 0.0014       |

TABLE 4. Current sharing errors for the two kinds of paralleled CLLLC converters for reverse operation mode.

| Output power |  |  |
|--------------|--------------|--------------|
|              | $\delta_{pm}$ for conventional paralleled converters | $\delta_{pm}$ for proposed paralleled converters |
| 627W         | 1            | 0.0316       |
| 800W         | 0.9986       | 0.0126       |
| 1143W        | 0.9957       | 0.0015       |
| 1369W        | 0.9924       | 0.0011       |
| 1600W        | 0.9917       | 0.00026      |

FIGURE 32. The efficiency of the proposed paralleled CLLLC converters.

VI. CONCLUSION

In this paper novel paralleled CLLLC converters are proposed. By the converters, system load can be easily and equally shared among the parallel units. And this is important to improve system capacity and power density. Through the analyses, simulations and experiments above, the following conclusions can be obtained.

a. In practical implications, component parameter derivations is inevitable and it can cause poor load current sharing for conventional paralleled CLLLC converters. Because of the satisfying equal current sharing performance, the proposed paralleled converters can be widely adopted for parallel DC energy conversion.

b. Through comprehensive modeling, analyses, simulations and experiments, the effectiveness of the proposed paralleled CLLLC converters has been verified. For other LLC types of DC/DC converters, similar technology routines can be adopted for parallel operations.

c. Since no more components are used and no complicated controllers are needed, it is simple for the utilization of the proposed paralleled converters. Because its symmetrical structure and simple connections between paralleled units, it is beneficial for modularization production. By advanced design of transformers integrated with resonant inductors, the power density can be further improved.

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