Analytical Inverter Delay Modeling Using Matlab’s Curve Fitting Toolbox

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Abstract—This paper presents a new analytical propagation delay model for deep submicron CMOS inverters. The model is inspired by the key observation that the inverter delay is a complicated function of several process parameters as well as load capacitance. These relationships are considered by fitting functions for each parameter derived from the Curve Fitting Toolbox in Matlab. Compared to SPICE simulations based on the BSIM4 transistor model, the analytical delay model shows very good accuracy with an average error less than 2% over a wide range of process parameters and output loads. Hence, the proposed model can be efficiently used for different technology nodes as well as statistical gate delay characterisation.

Index Terms—CMOS inverter, process parameters, gate-delay, curve fitting

I. INTRODUCTION

In CMOS digital design accurate timing characterisation of logic gates and digital circuits is essential. For static timing analysis (STA) it is common practice that two dimensional lookup-tables are used for describing the delay of cells dependent from slope and load capacitance. Building such tables however is computationally quite expensive as lots of SPICE simulations are necessary. Therefore the development of accurate analytical timing models has been the subject of much research in the past. As the CMOS inverter is an essential element in digital IC design analytical inverter delay models are of particular interest. Early models are based on the Shockley model for MOSFETS [1], [2] which turn to be inaccurate in 90nm technologies and beyond. Later on Sakurai and Newton proposed an empirical compact MOSFET model known as Alpha-Power Law Model [4], [5] which considers velocity saturation through parameter $\alpha$ (between 1 and 2). In the past several analytical delay formulas partly based on the Alpha-Power Low Model were introduced in [6], [8], [9] but there is still a lack in precise delay estimation. This is due to the complicated dependence of load capacitance, input slope, I/O coupling capacitance, short circuit current, velocity saturation, channel length modulation and drain-induced barrier lowering (DIBL) on delay. In [7] the most promising approach for an analytical inverter delay model is presented which takes into account all mentioned physical effects. However for the drain current empirical parameters $K_{in}$ and $K_{sat}$ are used. So the influence of process parameters like oxide thickness $t_{ox}$ or electron mobility $\mu$ on $K_{in}$ and $K_{sat}$ is hidden. Furthermore process parameters tend to vary (see Table I) within one technology node, so $K_{in}$ and $K_{sat}$ cannot be treated as constants. This will lead to misleading results.

| Year | $L$ (nm) | $t_{ox}$ (nm) | $V_{th}$ (V) |
|------|----------|---------------|--------------|
| 2001 | 180      | 4.5-5.5       | 0.39-0.43    |
| 2003 | 130      | 3.5-4.0       | 0.35-0.40    |
| 2004 | 90       | 1.6-3.0       | 0.25-0.40    |
| 2007 | 65       | 1.5-2.0       | 0.20-0.35    |
| 2009 | 45       | 1.0-1.4       | 0.20-0.35    |

TABLE I

Our proposed method provides a compact analytical inverter delay model dependent from process parameters and load capacitance. In a first step we model the drain saturation current $I_{DnSat}$ (this current is sufficient for fast input ramps which will be the focus in this paper) as a function of process parameters. Then the effect of load capacitance on delay is investigated. By using the Curve Fitting Toolbox of Matlab [11] then we derive an analytical formula for the inverter delay dependent from $I_{DnSat}$ and load.

The rest of the paper is organized as follows. In the next Section we review the technical background of inverter delay modeling. In Section III we demonstrate the procedure for obtaining an analytical saturation drain current followed by our analytical inverter delay model in Section IV. The experimental results are presented in Section V and finally we conclude in Section VI.

II. PRELIMINARIES

A. Theoretic Basics of Delay Modeling

The average propagation delay $t_d$ of a CMOS inverter driving a load capacitance $C_L$ (Figure 1) is calculated by:

$$ t_d = \frac{t_{pHL} + t_{pLH}}{2} \quad (1) $$

where both components $t_{pHL}$ and $t_{pLH}$ are computed by $t_{out50} - t_{in50}$ [15]. $t_{out50}$ refers to the time at which the output voltage level reaches half of $V_{DD}$. When applying a rising input ramp the load capacitance is discharged by the drain current $I_{Dn}$ as shown in Figure 1

The solution of the differential equation

$$ C_L \cdot \frac{dV_{out}}{dt} = I_{Dn} \quad (2) $$
yields the fall-delay $t_{pHL}$.

Under the assumption of a sufficient fast rising input ramp we can approximate $I_{Dn}$ with the drain saturation current $I_{DnSat}$. Then we have [9]

$$t_{pHL} = \frac{C_L \cdot V_{DD}}{2 \cdot I_{DnSat}} \quad (3)$$

$I_{DnSat}$ is given according to [8]

$$I_{DnSat} = \frac{1}{2} \cdot \mu \cdot \epsilon_r \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^\alpha \cdot (1 + \lambda V_{DS}) \quad (4)$$

with $\mu$ as the electron mobility, $t_{ox}$ as the oxide thickness and $V_{th}$ as the threshold-voltage, $W$ is the channel-width, $L$ the channel-length, $\lambda$ the channel-length modulation factor and $\alpha$ the velocity saturation index. These parameters refer to the nMOS transistor. $V_{DS}, V_{GS}$ are the drain-source and gate-source voltage.

For deriving $t_{pLH}$ when applying a falling input ramp $C_L$ will be charged by $I_{Dp}$ of the pMOS transistor. Therefore the pMOS transistor parameters are needed. In the following we want to focus on $t_{pHL}$ but our method is also applicable for $t_{pLH}$.

B. Determination of Drain Current: Mismatch between analytical model and SPICE simulation

An accurate drain current model is crucial for an exact gate delay. A comparison between the analytical drain saturation current in eq.(4) and SPICE simulation is quite difficult due to the highly complex relationships between model parameters for SPICE and physical parameters used in eq.(4) [12].

Feeding the SPICE simulator with the model parameters as in Table II-B we get the following $I_{Dn} - V_{DS}$ characteristics of the nMOS transistor for different widths (see Figure 2). As for the gate delay computation with fast input ramps only the saturation drain current $I_{DnSat}$ is important we take $I_{DnSat}$ for $V_{GS} = V_{DS} = V_{DD} = 1.2V$ from these curves and compare them to the analytical $I_{DnSat}$. From Figure 3 we can conclude:

- The different nature of physical parameters (used in eq.(4)) and the model parameters for SPICE cannot be neglected. The model parameters, such as $U0$ or $VTH0$ must be converted to effective parameters like $\mu$ and $V_{th}$ in order to use the analytical model. Such complicated equations as described in the BSIM4 manual [12] with more than 200 model parameters may lead to an impractical delay model.
- The dependency of $I_{DnSat}$ from parameters is quite more difficult as stated in eq.(4). For example there is no real linear dependency from the channel width $W$ as seen in the right part of Figure 3. This is also for other parameters.

![Figure 1](image1.png)

**Fig. 1.** CMOS-inverter with load $C_L$ which is discharged through nMOS transistor for a rising input ramp

![Figure 2](image2.png)

**Fig. 2.** $I_{Dn} - V_{DS}$ characteristics of nMOS transistor dependent from transistor width $W$

![Figure 3](image3.png)

**Fig. 3.** $I_{DnSat}$ with SPICE and eq.(4) (left), dependency of $I_{DnSat}$ on channel width $W$ (right)

| Parameter | for eq.(4) (physical parameter) | for SPICE (model parameter) | value |
|-----------|---------------------------------|-----------------------------|-------|
| mobility  | $\mu$                           | $U_0$                       | 550 cm$^2$/V s |
| threshold-voltage | $V_{th}$               | $V_{TH0}$                    | 0.4V   |
| oxide thickness | $t_{ox}$            | $TOXE$                       | 3.0 nm |
| channel-length | $L_{eff}$         | $L$                          | 90 nm  |

**TABLE II**

**MODEL PARAMETERS FOR SPICE AND PROCESS PARAMETERS**
Many papers use the transconductance parameter $K$ empirical achieved by SPICE simulation (e.g. [7]) for their analytical models. Though a reasonable accuracy is reached the dependency of $K$ from process/model parameters is lost. To overcome this problem in the following Section we suggest a fitting-based approach to get an analytical expression for $I_{DnSat}$, which preserves the dependency on process/model parameters.

III. ANALYTICAL DRAIN SATURATION CURRENT

Starting with a specific technology node the following steps yield the desired analytical drain current equation.

1. Generate a reference saturation drain current $I_{DnSat-R}$ through SPICE simulation with reference values for the parameters $TOXE$, $VTH0$, $U0$, $L$ and $W$.
2. Specify an interval for each parameter by using Table I or the Predictive Technology Model PTM [10]. Subdivide each interval in equal steps, e.g. $L$ becomes a list $(L_1, L_2, ..., L_n)$ consisting of $n$ different channel-lengths.
3. Generate a list of saturation drain currents for all values within the list for one parameter through SPICE simulation. All other parameters are set to their reference values. Referring to $L$ we get $n$ currents, denoted as $I_{DnSat-L}$.
4. Start the Curve Fitting-Toolbox from Matlab with the following inputs:
   - $x$-data = ratio between varied parameter and reference parameter, e.g. $L/L_R$.
   - $y$-data = ratio between simulated drain saturation current and $I_{DnSat-R}$, e.g. $I_{DnSat-L}/I_{DnSat-R}$

   Choose an appropriate fitting function for the investigated parameter, e.g. a quadratic fitting function $y_1$ is used for $L$ which is illustrated in Figure 4.
5. Repeat the steps 3 and 4 for all other parameters. From the toolbox we get the fitting functions denoted as $y_2$, $y_3$, $y_4$, $y_5$.
6. The formula for the analytical drain saturation current is given as:

$$I_{DnSat-A} = y_1 \cdot y_2 \cdot y_3 \cdot y_4 \cdot y_5 \cdot I_{DnSat-R} \quad (5)$$

IV. ANALYTICAL INVERTER DELAY

Now for computing the delay $t_{pHL}$ as described in Section II we take the load capacitance $C_L$ into account. However using the simple eq.(3) is problematic since $I_{DnSat}$ is not really constant for the timing interval of discharging the load. This is illustrated in Figure 5.

In order to work with our analytical drain saturation current formula eq.(5), the following procedure is suggested.

- Simulate the delay $t_{pHL}$ with SPICE for the parameter constellations as in Section III and different loads $C_L$.
- Compute $I_{DnSat-A}$ using eq.(5) with these parameter constellations.
- Start the Curve Fitting-Toolbox from Matlab with the following inputs:
  - $x$-data = $I_{DnSat-A}$
  - $y$-data = loads $C_L$
  - $z$-data = $t_{pHL}$ values after SPICE simulation

   This means $t_{pHL}$ is a two-dimensional plane dependent from drain current and load capacitance as illustrated in Figure 6. By choosing an appropriate fitting function we get the desired analytical model denoted as $t_{pHL-A}$.

Note: A visual examination of a fitted curve/plane which is displayed in the Curve Fitting App of Matlab should always be the first step in the evaluation of the fitting quality. Beyond the toolbox generates a Goodness-of-Fit Output, which provides goodness-of-fit statistics like the sum of squares due to error (SSE) or the root mean square error (RMSE) [11], [14].
| Test No. | L (nm) | W (µm) | TOX E (nm) | VTH0 (V) | U0 (cm²/V²) | Simulated Delay (ps) | Analytical Delay (ps) | Maximum Error (%) | Average Error (%) |
|---------|-------|--------|-----------|----------|------------|----------------------|-----------------------|-------------------|------------------|
| 1       | 80.8  | 2.8    | 1.78      | 0.27     | 538        | (13.4, 21.9, 38.1, 51.8, 73.4) | (14.1, 22.5, 38.1, 51.9, 72.4) | 5.0              | 1.8              |
| 2       | 80.8  | 2.8    | 2.40      | 0.37     | 540        | (18.6, 32.0, 57.4, 80.0, 114.4) | (17.9, 31.1, 55.9, 77.5, 111.3) | 3.9              | 3.1              |
| 3       | 80.8  | 1.34   | 1.78      | 0.27     | 542        | (19.5, 37.4, 71.2, 100.6, 146.4) | (20.0, 37.8, 71.3, 100.1, 145.4) | 2.5              | 1.0              |
| 4       | 80.8  | 4.65   | 1.78      | 0.27     | 538        | (11.1, 16.1, 25.8, 34.3, 47.0) | (11.1, 16.1, 25.7, 33.8, 46.6) | 1.5              | 0.6              |
| 5       | 85.3  | 2.8    | 1.78      | 0.33     | 542        | (15.1, 24.1, 42.3, 58.0, 82.2) | (15.1, 25.4, 43.1, 59.1, 82.8) | 5.1              | 2.0              |
| 6       | 85.3  | 1.34   | 1.62      | 0.37     | 542        | (22.7, 43.0, 80.8, 114.0, 165.5) | (22.8, 44.0, 83.9, 117.5, 170.5) | 3.7              | 2.5              |
| 7       | 87.8  | 2.8    | 1.78      | 0.37     | 540        | (15.9, 26.3, 46.2, 63.3, 89.9) | (15.6, 26.3, 46.1, 63.4, 89.9) | 1.9              | 0.4              |
| 8       | 87.8  | 1.34   | 1.78      | 0.27     | 538        | (20.2, 38.6, 73.2, 103.5, 150.2) | (21.3, 39.7, 74.9, 107.0, 153.0) | 4.3              | 2.8              |
| 9       | 87.8  | 4.65   | 2.26      | 0.37     | 542        | (14.4, 22.5, 37.0, 49.9, 69.6) | (13.8, 21.2, 35.9, 48.5, 68.2) | 6.1              | 4.0              |
| 10      | 89.3  | 2.8    | 2.07      | 0.30     | 538        | (15.5, 26.1, 45.6, 62.7, 89.4) | (15.6, 26.2, 45.9, 63.0, 89.6) | 0.7              | 0.5              |

**TABLE III**
**Comparison between SPICE inverter delay and analytical delay model for different process/model parameters and load capacitances**

![Image](image.png)

**Fig. 6.** Piecewise linear interpolating function $t_{pHL - A}$ which fits $t_{pHL}$ dependent from $I_{DnSat - A}$ and $C_L$, $L = 90nm$ technology node

**Fig. 7.** Comparison between simulated and analytical drain saturation currents $I_{DnSat - A}$

V. EXPERIMENTAL RESULTS

A. Validation of drain current model

We start with specifying a list of values (valid for a 90nm technology node) for each parameter as described in Section III: $L = (90, 88, 86, 84, 82)\, nm$, $W = (1, 2, 3, 4, 5)\, \mu m$, $TOXE = (3, 2.5, 2, 1.6)\, nm$, $VTH0 = (0.4, 0.35, 0.3, 0.25)\, V$ and $U0 = (550, 540, 530, 520)\, \text{cm}^2/\text{V}^2$. Then 22 SPICE simulations are needed to get the drain saturation currents. Together with one additional simulation for the reference drain current $I_{DnSat - R}$ (using the reference values for the parameters according to Table II-B) Matlab's Curve Fitting Toolbox can be fed. It turns out that for each parameter a second order polynomial is an appropriate fit with a RMSE below 0.01% in any case. Computing $I_{DnSat - A}$ with eq.(5) with all possible combinations of the parameter values listed above leads to 1600 different values. Randomly we choose a subset of 25 testcases. Figure 7 illustrates the quite good accordance of simulated and calculated saturation drain currents. The maximum error is smaller than 7%, the average error is 3.0%.

B. Validation of inverter delay model

First we take the parameter settings for the mentioned 25 testcases and obtain 5 inverter delays $t_{pHL}$ due to $C_L = (10, 20, 50, 100, 200)\, fF$ for each testcase by SPICE. Together with the values of $I_{DnSat - A}$ for these testcases, Matlab's Curve Fitting Toolbox generates a piecewise linear interpolate fit $t_{pHL - A}$ with 125 coefficients. Then we randomly generate 5 values for each parameter with the Matlab routine rand, e.g.: $I_{var} = (90nm - 10nm) \cdot \text{rand}(5, 1) + 80nm$. All values are within the lists as specified in Section V.A. Also we use 5 different load capacitances in the interval $[10, 200]\, fF$, namely $(13, 37, 83, 123, 185)\, fF$.

For each parameter combination and load capacitance we compute the analytical inverter delay using the fitting function $t_{pHL - A}$. Overall we get $5^6 = 15625$ values. In order to avoid simulating each case with SPICE, we choose 10 different parameter combinations. For each combination SPICE reports the delay for all five load capacitances. In Table III it is illustrated that the maximum error between SPICE and analytical model is about 6%. The average error for all cases is less than 2%.
C. Comparison to other analytical models

Finally we want to evaluate the quality of recently published inverter delay equations. As reference we use the simulated SPICE delays for testcase No.1 and the loads \( C_L \) as above. Both the Sakurai-Newton (SN) delay metric and the Taur-Ning (TN) delay metric from \([8]\) underestimate the delay compared to SPICE. This underestimation becomes smaller with increasing loads. The delay \( T_{pHL} \) from eq.(6) in \([13]\) also underestimates the inverter delay, however the underestimation becomes smaller with decreasing loads. This is illustrated in Figure 8. One can argue that in all cases this enormous discrepancy is caused by the mismatch of model and process parameters. But on the other hand a simple additional fitting factor would not solve the problem due to its dependency on \( C_L \).

![Fig. 8. Comparison of delay metrics from [8], [13] and SPICE simulation](image)

VI. CONCLUSION

In this paper we propose a novel analytical CMOS inverter delay model. The main advantage of this approach compared to previous related work is the more detailed study of the drain current especially the transconductance parameter dependent from process parameters. The model generation is both simple because of curve fitting and - apart from some necessary SPICE simulations - computationally inexpensive. Furthermore our method is applicable to any technology node. Experimental results for a wide range of different parameter values and load capacitances have shown that the worst case error is smaller than 7%. It is expected that our model is suitable to consider process variations in future technologies.

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