PolyMPCNet: Towards ReLU-free Neural Architecture Search in Two-party Computation Based Private Inference

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ABSTRACT

The rapid growth and deployment of deep learning (DL) has witnessed emerging privacy and security concerns. To mitigate these issues, secure multi-party computation (MPC) has been discussed, to enable the privacy-preserving DL computation. In practice, they often come at very high computation and communication overhead, and potentially prohibit their popularity in large scale systems. Two orthogonal research trends have attracted enormous interests in addressing the energy efficiency in secure deep learning, i.e., overhead reduction of MPC comparison protocol, and hardware acceleration. However, they either achieve a low reduction ratio and suffer from high latency due to limited computation and communication saving, or are power-hungry as existing works mainly focus on general computing platforms such as CPUs and GPUs.

In this work, as the first attempt, we develop a systematic framework, PolyMPCNet, of joint overhead reduction of MPC comparison protocol and hardware acceleration, by integrating hardware latency of the cryptographic building block into the DNN loss function to achieve high energy efficiency, accuracy, and security guarantee. Instead of heuristically checking the model sensitivity after a DNN is well-trained (through deleting or dropping some non-polynomial operators), our key design principle is to \textit{enforce} exactly what is assumed in the DNN design—training a DNN that is both hardware efficient and secure, while escaping the local minima and saddle points and maintaining high accuracy. More specifically, we propose a \textit{straight through polynomial activation initialization} method for cryptographic hardware friendly trainable polynomial activation function to replace the expensive 2P-ReLU operator. We develop a cryptographic hardware scheduler and the corresponding performance model for Field Programmable Gate Arrays (FPGA) platform.

KEYWORDS

Multi Party Computation, Neural Architecture Search, Model Compression, FPGA

1 INTRODUCTION

The large deep neural network (DNN) model size causes great computational cost and memory footprint overhead. A Google study has shown that one of the most successful pre-training language models, GPT-3 (175 billion parameters), consumed 1,287 MWh of electricity during training and produced 552 tons of carbon emissions, the equivalent of a car 120 years of emissions [1]. Various model compression techniques [2–9] have been developed to reduce the DNN model size.

On the other hand, machine learning system has been facing various security concerns. For example, recent research [10–12] shows that the publicly shared gradients in the training process of Machine-Learning-As-A-Service (MLaaS) can reveal private training data to a third party. Privacy-preserving machine learning (PPML) has emerged to protect sensitive data with strong security guarantees in DNNs. As one representative technique, secure multi-party computation (MPC) allows more than one user to conduct collaborative computing without revealing individual data to each other, as shown in Fig. 1 [13, 14]. However, they often come at very high computation and communication overhead in practice. Adding additional cryptographic operations could potentially prohibit the popularity and the adoption of large-scale edge devices such as mobile or IoT.

To achieve high performance, scalability, and energy efficiency for secure deep learning systems, two orthogonal research trends have attracted enormous interests. The first trend is the \textit{MPC comparison protocol overhead reduction} by using model compression [15–19] and polynomial approximation [20–22]. Reinforcement learning based neural architecture search (NAS) has also been introduced to reduce such overhead, e.g., CryptoNAS [18]. However, the reduction of non-polynomial operators (e.g., ReLU or maxpool) in these works leads to a severe accuracy drop. To maintain accuracy, a low reduction ratio needs to be used. As a result, these works suffer from high latency due to limited computation and communication saving.

The energy efficiency challenge of secure DNN models motivates the second trend: \textit{hardware acceleration}. Prior arts mainly focus on CPU (e.g., CryptTFlow [23], MP-SPDZ [24], GAZELLE [25]) and GPU.

Figure 1: Secure multi-party computation (MPC) guarantees.
(e.g., CryptGPU [26]) implementations. CryptGPU could provide up to 150× faster than CPU-based designs. However, these works are power-hungry. For example, our observation shows that, CryptGPU [26] requires 700W power and over 2.7GB communication size to run the MPC-based VGG16 network.

In this work, as the first attempt, we develop a systematic framework of joint overhead reduction of MPC comparison protocol and hardware acceleration, by integrating hardware latency of the cryptographic building block into the DNN loss function to achieve high energy efficiency, accuracy, and security guarantee. Instead of heuristically checking the model sensitivity (deleting or dropping some non-polynomial layers or operators and observing accuracy) after a DNN is well-trained, our key design principle is to enforce exactly what is assumed in the DNN design—training a DNN that is both hardware efficient and secure, while maintaining high accuracy. On hardware platforms, FPGAs [27–29] lend themselves as the top choice since strike an effective balance between high hardware performance, parallelism degree, and fast development round. We summarize our contributions as follows:

1. We propose a straight through polynomial activation initialization method for cryptographic hardware friendly trainable polynomial activation function to replace the expensive 2P-ReLU operators.

2. Cryptographic hardware scheduler and the corresponding performance model are developed for FPGA platform. The latency loop up table can be constructed based on such model.

3. We start with the DNN optimization stage, and integrate latency of the cryptographic building block into the DNN loss function to facilitate escaping the local minima and saddle points, therefore achieving high accuracy.

4. We propose a differentiable cryptographic hardware-aware micro-architecture search framework to select the proper polynomial or non-polynomial activation based on given constraint.

5. To the best of our knowledge, we are the first attempt to report large scale ImageNet performance for cryptographic NN with polynomial activation. Experiment shows that we are able to achieve all polynomial replacement with 0.78% top-1 accuracy improvement for PolyMPCNet-A model (ResNet18 as baseline) on ImageNet dataset, and even higher top-1 accuracy for PolyMPCNet-B model with partial polynomial replacement.

2 BACKGROUND AND RELATED WORKS

2.1 Secure Multi-party Computation in DNN

2.1.1 Hardware Acceleration of Secure DNNs. Secure MPC, a cryptographic technique, is used to allow multiple parties to jointly and securely perform a function while keeping each party’s inputs private. MPC is capable of providing security guarantees as robust as those achievable by trusted third parties [30]. Researchers have been using MPC to build secure, privacy-preserving DNN frameworks. The state-of-the-art secure DNNs using MPC are mainly implemented on CPUs. For instance, CryptTensorFlow [23] converts TensorFlow inference code [31] into MPC protocols at the push of a button using Intel SGX. MP-SPDZ [24] primarily targets at the compiler level, i.e., compile the high-level secret protocol code (bytecode) into virtual machine. CryptTensorFlow2 [32] further improves CryptTensorFlow by using Athos, an end-to-end compiler, to convert TensorFlow to MPC protocols. GAZELLE [25] uses a combination of homomorphic encryption (HE) and traditional two-party computation techniques (such as garbled circuits) on Intel Xeon E5-2666 CPU with 7.5GB memory and demonstrates three orders of magnitude faster inference time, compared with fully homomorphic approaches such as CryptoNets [33].

Recently, a DNN system built on graphics processing unit (GPU) using MPC, titled CryptGPU [26], has been discussed. CryptGPU embeds cryptographic operations over secret-shared values into the floating-point operations for CUDA kernels. It achieves up to 150× speedups over CPU-based solutions. As the first effort towards building an end-to-end MPC-DNN framework on FPGAs, we thoroughly investigate secret sharing MPC for FPGA-DNN acceleration.

2.1.2 Overhead Reduction of MPC Comparison Protocol. Existing MPC comparison protocol overhead reduction fall into two categories: model compression [15–19] and polynomial approximation [20–22]. TAPAS [16], XONN [17], and Soteria [15] focus on Binary Neural Network (BNN) for cryptographic inference, however, the reduction of non-polynomial operators (e.g., ReLU or maxpool) leads to a severe accuracy drop. To maintain accuracy, a low reduction ratio needs to be used, as a result, these works suffer from high latency due to limited computational cost saving.

CryptoNAS [18] utilizes reinforcement learning (RL) based micro-architecture search framework [34] to improve the parameter to ReLU ratio and find the near-optimal structure. However, the performance of CryptoNAS is limited as it is featureless search target. The method is also not scalable due to the long training time incurred by RL-based search framework. Delphi [20] and SAFENet [22] propose to replace ReLU operation with polynomial activation. However, the reduction of ReLU operations leads to a severe accuracy drop in their implementation.

2.2 Threat Model

2PC setup. We consider a similar scheme involving two semi-honest in a MLaaS applications [35, 36]. In this scheme, the two servers receive the confidential inputs that are secretly outsourced from the client and invoke a two party secure computing protocol to securely evaluate the function within the given inputs. The 2PC protocol ensures that intermediate information and computation results are not exposed to the servers during the evaluation process. Notably, this server-aided secure computation setup could also be used for an arbitrary number of clients, providing their confidential inputs for general multi-party applications [35].

Threat model. We assume that an admissible adversary [37] who can compromise up to one server at a time to launch attacks, which captures the non-colluding server assumption. Furthermore, we focus on a semi-honest security model [38–41] where the adversary is “honest but curious”, which does not deviate from the protocol specification but can do arbitrary side calculations that try to violate the security of the system. Although this is not the strongest assumption, this model makes sense in the context of many real-world applications, as simply starting a secure computing instance already requires a substantial degree of trust between all parties.
3 CRYPTOGRAPHIC BUILDING BLOCKS

3.1 Secret Sharing

As the most critical manner in multi-party computation, secret sharing rules the communication between parties by still keeping one’s information secure without risk of reasoning by other parties. Specifically, in this work, we apply the scenario that inputs and intermediate data in DNN are separated in two parts for individual computation and shared between two parties for the result derivation or further computations.

Definition 3.1 ((n, t)-secret sharing). Given ring $\mathbb{Z}_m$ as an integer space, such that $m$ is a prime number, the $(n, t)$-secret sharing ($t$-out-of-$n$) over $\mathbb{Z}_m$ represents a manner that splits a secret value $x \in \mathbb{Z}_m$ among $n$ parties. The security property ensures that any $s$ out of $n$ parties can recover $x$ if and only if $s \geq t$. Otherwise, the secret value $x$ cannot be recovered with less than $t$ parties.

This definition interprets the secret sharing in MPC that one secret value is decomposed as multiple parts and can be regenerated from these parts, noting that all the values should be in the ring space $\mathbb{Z}_m$. Since we investigate the two-party DNN inference, the implementation is formulated as $(2, 2)$-secret sharing, meaning that the secret value $x$ is converted to two shares and will never be recovered unless both shares are obtained. As a symbolic representation, for a secret value $x \in \mathbb{Z}_m$, $[x] = (x_0, x_1)$ denotes the two secret shares, where $x_0, i \in [0, 1]$, is the share distributed to server $i$ on FPGA. The share generation and the share recovering of secret share adopted in our work are shown below:

- Share Generation $\text{shr}(x)$: Given $x \in \mathbb{Z}_m$, a random value $r$ in $\mathbb{Z}_m$ is sampled, and shares are generated as $[x] \leftarrow (r, x - r)$.
- Share Recovering $\text{rec}([x])$: Given shares $[x] \leftarrow (x_0, x_1)$, it computes $x \leftarrow x_0 + x_1$ as the recovered $x$.

To eliminate the redundancy, we get rid of the notation of ring calculation on $\mathbb{Z}_m$ (i.e., mod $m$) in all exhibited equations, except for explicit identifying.

3.2 Polynomial OPR. Over Secret-Shared Data

DNN are mainly composed of multiplication and addition operator (OPR) on tensors. These operations contain but not limited to matrix/vector addition and scaling, Hadamard product, matrix/vector multiplication, and convolution. We denote matrices as $[X]$ and $[Y]$ as two secret-shared data. For the addition and scaling, the secret sharing is supposed to keep the result also following the sharing manner, as shown in Eq. 1, where $Z$ is the bias on results.

$$\begin{align*}
\left[aX + bY + Z\right] & \leftarrow (aX_0 + bY_0 + Z, aX_1 + bY_1 + Z) \\
\end{align*}$$

On the other hand, we expect the matrix multiplicative operations as Eq. 2 in the secret-sharing pattern.

$$\begin{align*}
[R] & \leftarrow [X] \otimes [Y] \\
\end{align*}$$

where $\otimes$ is a general multiplication, such as Hadamard product, matrix multiplication, and convolution. Unlike the addition and scaling, multiplication needs careful design to guarantee the result recoverable. Typically, homomorphic encryption [42] and oblivious transfer (OT) [43] are two effective approaches, while OT is selected in this work to generate shares [35].

To make the multiplicative computation secure, an extra pre-computed matrix $Z$ should be generated as $[Z] = \begin{bmatrix} A \otimes B \end{bmatrix}$, where $A$ and $B$ are randomly initialized. Specifically, their secret shares are denoted as $[Z] = (Z_0, Z_1)$, $[A] = (A_0, A_1)$, and $[B] = (B_0, B_1)$. Noting that $[Z]$, $[A]$, and $[B]$ must have the same shape as $[X]$, $[X]$, and $[Y]$, respectively, to align the matrix multiplication. Later, two matrices are derived from given shares: $E_S = X_0 - A_0$, and $F_S = Y_0 - B_0$, in each party end separately. Then, the intermediate shares are jointly recovered as $E \leftarrow \text{rec}([E])$ and $F \leftarrow \text{rec}([F])$. Finally, each party, i.e, server $S_i$, will calculate the secret-shared result $R_{S_i}$ locally:

$$R_{S_i} = - i \cdot E \otimes F + A_{S_i} \otimes F + E \otimes B_{S_i} + Z_{S_i} \quad (3)$$

Consequently, each server gets its own secure result $R_{S_i}$ from the initial inputs $X_{S_i}$ and $Y_{S_i}$, i.e., $\text{rec}([R]) = R_{S_0} + R_{S_1} = [X] \otimes [Y]$.  

3.3 Non-Polynomial Operator Modules

Except for the intensive polynomial operations, there is other non-polynomial process existing in the two-party neural network (2PC-NN) inference, such as the oblivious transfer as the communication during secret sharing and the comparison module for the non-polynomial operations, e.g., ReLU and MaxPool.

3.3.1 Oblivious Transfer (OT). OT is a protocol that allows one party send one of the potentially many messages to a receiver while retaining oblivious on which message is transferred. This approach is the backbone of our 2PC-NN framework. To give a more perceptual understanding, we assume a scenario of NN inference, such as the oblivious transfer as the communication going on FPGA. The share generation and the secret recovering of secret shared adopted in our work are shown below:

$$R_{S_i} = - i \cdot E \otimes F + A_{S_i} \otimes F + E \otimes B_{S_i} + Z_{S_i} \quad (3)$$

Consequently, each server gets its own secure result $R_{S_i}$ from the initial inputs $X_{S_i}$ and $Y_{S_i}$, i.e., $\text{rec}([R]) = R_{S_0} + R_{S_1} = [X] \otimes [Y]$.

3.3.2 Secure 2PC Comparison. The 2PC comparison, a.k.a. millionaires protocol, is committed to determine whose value held by two parties is larger, without disclosing the exact value to each other. Work [45] has proposed a practical strategy for 2PC comparison protocol, which is adopted in this work as the primitive for non-polynomial operations. Assuming the values held by party $S_0$ and $S_1$ are $x, y \in \mathbb{Z}_m$, where $x$ and $y$ are $t$-bit integers, the comparison result will be $1 (x < y)$, $2 (x = y)$, or $3 (x > y)$ by keeping the values themselves unrevealed. Since $x$ and $y$ can be represented in $t$ bits, their values can be parsed as binary sequences, $x \leftarrow x_{t-1}|x_{t-2}|...|x_0$ and $y \leftarrow y_{t-1}|y_{t-2}|...|y_0$ respectively, i.e., $x, y \in [0, 1]^t$. We further split the value sequence evenly by $\ell$ parts, so that each part has $(\ell/\ell)$ bits. For example, our later mentioned case divides the 32-bit value to 16 parts, with 2 bits for each part. The comparison follows the $(1, 2)$-OT rule. It starts by server $S_1$ encoding the parts of $y$ as a key list, which is transferred to server $S_0$. Then, $S_0$ will generate the encrypted comparison message regarding the key list such that $S_1$ can retrieve the message. By decrypting it, $S_1$ gets the comparison results for these parts correspondingly on $x_0$ and $y_0, u \in [1..U]$. After $S_1$ obtains the comparison sequence of value parts, it will check the results from the most left part until determines the final comparison result, as shown in Figure 3. The comparison result will also be shared with $S_0$. 
Here we demonstrate a toy case of the 2PC comparison which splits the INT4 values as two parts, i.e., \( x, y \in \{0, 1\}^4 \) and \( U = 2 \). Note that for simplicity in this example, we only illustrate the detail of the comparison sequence generation while omitting the processing of OT. For server \( S_0 \), it will split \( x \) as two parts \( M_0(x, 0) = x_3 || x_2 \) and \( M_0(x, 1) = x_1 || x_0 \). Since two bits only have four possibilities, \( pm = \{00, 01, 10, 11\} \), there will be four results after making the \( u \)-th part compare with \( pm \), where \( u \in \{0, 1\} \) in this example, and each comparison result follows:

\[
M_0(x, u, l) = \begin{cases} 
1, & M_0(x, u) < pm \\
2, & M_0(x, u) = pm \\
3, & M_0(x, u) > pm 
\end{cases}
\]  (4)

Here \( l \) indicates the index for the \( pm \), which is also referred as a mapping index for an injective function \( b2d(\cdot) \). Assuming \( S_0 \) has received the key \( R \) containing value information from \( S_1 \), it will then generate encrypted messages combining the comparison results, i.e., Table 1, with the key \( R \). The encrypted messages will then be transmitted to \( S_1 \) for further process. Due to the \((1,2)\)-OT protection, \( S_1 \) can only decrypt the interested messages. For example, if \( S_1 \) interests index 2 and 1 for the part 0 and 1, then only the comparison message \( M_0(x, 0, 1) \) and \( M_0(x, 1, 0) \) will be revealed while other messages keep unrevealed, so that the value \( x \) itself cannot be recovered due to the incomplete comparison matrix received by \( S_1 \).

Choosing the shape of comparison matrix. With the fact that there are many ways to evenly split a multi-bit value into parts and all of them can achieve the privacy and security requirements (except for 1-bit parts), it is still worthwhile to discuss the cut basis. We assume a \( t \)-bit value which can be evenly split to \( U \) parts, meaning that the comparison matrix size is \( 2^t/\log U \). We assume the dishonest scenario that \( S_0 \) wants to know which indices \( S_1 \) are in interested in and \( S_1 \) wants to know the value \( S_0 \) is holding. From the \( S_0 \) perspective, it needs to correctly guess the index for each column in the comparison matrix, whose guessing space is \( (2^t/\log U)U = 2^t \); on the other hand, only when all the parts return an “equal” message, i.e., \( x = y \), can \( S_1 \) surely determine the value \( x \) held by \( S_0 \), whose possibility is \( 1/2^t \). Hence, the security of 2PC comparison is not significantly related to the way to split the values. If considering the encryption and communication complexity, the comparison matrix has \( 2^t/\log U \cdot U \) elements. By optimizing the efficiency on the inference, we are trying to minimize the number of elements in the comparison matrix:

\[
\min_U 2^t/\log U \cdot U \tag{5}
\]

The optimal solution is \( U = 0.693t \), meaning that each part has \( t/\log U \) 2 bits. Hence, in our work, we adopt the split strategy that each part has two bits to divide multi-bit values.

### 4 THE CRYPTOGRAPHIC HARDWARE ACCELERATOR SEARCH FRAMEWORK

In this section, we review the computation and communication pattern of main cryptographic building blocks for DNN, and provide analytical models for FPGA implementations of DNN operators. With the help of analytical models, we develop a differentiable algorithmic-hardware co-search framework to select the best model architecture under different constraints. The proposed design could be migrated to other platforms, such as mobile and cloud platforms.

Note that here the possibility is not accurate, since we ignore some special cases for simplicity of qualitative analysis, e.g., with the knowledge that \( x_u < y_u \) and \( y_u = 1 \), \( S_1 \) still can determine the \( x_u \) as 0. This exception is also the cause of the vulnerability of 1-bit parts.
4.1 Problem Formulation and Overview

In order to find a balance in the latency (polynomial replacement) and model accuracy trade-off, a neural architecture search method is desired. For example, in a VGG-16 network for image classification, there are 20 non-polynomial layers: 5 MaxPool layers and 15 ReLU layers. The replacement of non-polynomial layers with polynomial layers for VGG-16 incurs a $2^{20}$ search space and the search space grows exponentially with the number of non-polynomial layers. Thus the brute-force search is not feasible for the proposed search.

The proposed micro-architecture search framework is given in Fig. 2, we firstly provide the framework with backbone architecture such as ResNet-18 and MobileNet-v3, and the latency constraint. Then we generate gated micro-architecture weighted by trainable parameter. The gated operators are used to select between polynomial operation and non-polynomial operation. Other than gated operators, the computation intensive parts such as Conv2D (a convolution operation on the 2D matrix) and FC (fully-connected) layers are shared in the architecture to reduce the training overhead. The latency modeling of operators will be given in future works. The detailed loss function design and parameter update of gated operator will be given in Sec. 4.2. With the proposed micro-architecture search framework, we are able to obtain a NN architecture with a finer combination of polynomial and non-polynomial architecture.

We use a hardware friendly trainable second order polynomial activation function for our framework, shown in Eq. 6, where $w_1$, $w_2$ and $b$ are all trainable parameters. We propose straight through polynomial activation initialization (STPAI) method to set the $w_1$ and $b$ to be small enough and $w_2$ to be near to 1 in Eq. 6 at the start of training process. Experiment shows that our method converges to a better local optima than SAFENet [22] and avoids gradient explosion due to the second order polynomial term. During inference, we use equivalent form Eq. 7 of the proposed activation and incorporate $w_1'$ and $b_1'$ into the convolution or fully connected layers’ parameters. Thus, the proposed activation only requires only single square operation during the inference process. The square operation follows same computation steps with secret-share matrix Hadamard product.

$$\delta(x) = w_1 x^2 + w_2 x + b$$

$$\delta(x) = (w_1' x + b_1')^2 + b_2' = x^2 + b'_2$$

Layer-wise second order polynomial activation functions preserve the convexity of single layer neural network [46]. Higher order polynomial activation function or channel-wise fine-grained polynomial replacement proposed in SAFENet [22] may destruct the convexity of neural network and leads to a deteriorated performance. As listed in the experiment, layer-wise second order polynomial activation function can already achieve an excellent performance so no higher order polynomial function is needed.

To further enhance the model performance, we adopt transfer learning method [47] for general weights initialization and straight through polynomial activation initialization for polynomial weights. After the appropriate model architecture is found from NAS framework, we load the pre-trained weight parameters for the backbone model and task to target model architecture. Experiment shows that the transfer learning with proposed polynomial activation initialization methods can effectively avoid the gradient explosion problem and achieve a high model accuracy.

4.2 Differentiable NAS Algorithm

Early work [48, 49] focus on using RL for NAS. The RL based method effectively explores the search space but still requires a significant amount of search overhead such as GPU hours and energy. Hardware-aware NAS have also been investigated [50–54]. In this work, we incorporate latency constraint into the target loss function of the DARTS framework, and develop a differentiable cryptographic hardware-aware micro-architecture search framework. We firstly determine a backbone model for NAS, and introduce gated operators $OP_l(x)$ which parametrizes the candidate operators $OP_{l,j}(x)$ selection with a trainable weight $a_{l,j}$ (Eq. 8). For example, a gated pooling operator consists of MaxPool and AvgPool operators and 2 trainable parameters for pooling selection. The latency of the operators could be determined based on explicit hardware modeling. A parameterized latency constraint is given in Eq. 9, where the latency of gated operators is weighted by $\theta_{l,j}$. As shown in Eq. 10, we incorporate the latency constraint into the loss function and penalize the latency $Lat(\alpha)$ by tunable parameter $\lambda$.

$$\theta_{l,j} = \frac{\exp(a_{l,j})}{\sum_{k=1}^{m} \exp(a_{l,k})}, \quad OP_l(x) = \sum_{k=1}^{m} \theta_{l,k}OP_{l,k}(x)$$

$$Lat(\alpha) = \sum_{l=1}^{n} \sum_{j=1}^{m} \theta_{l,j}Lat(OP_{l,j})$$

$$\xi(\omega, \alpha) = \epsilon \frac{\delta \xi}{\delta \omega}(\omega, \alpha) + \lambda \frac{\delta \xi}{\delta \alpha}(\omega, \alpha)$$

The optimization objective of our design is shown in Eq. 11, we aim to minimize the validation loss $\xi_{val}(\omega', \alpha)$ with regard to architecture parameter $\alpha$. The optimal weight $\omega'$ is obtained through minimize the training loss. The second order approximation of the optimal weight is given in Eq. 12, the approximation is based on current weight parameter and its’ gradient. The virtual learning rate $\xi$ can be set equal to that of weight optimizer. Eq. 13 gives the approximate $\alpha$ gradient using chain rule, the second term of $\alpha$ gradient can be further approximated using small turbulence $\epsilon$ with Eq. 14 and Eq. 15.

$$\arg\min_{\alpha} \xi_{val}(\omega', \alpha), \text{s.t. } \omega^* = \arg\min_{\omega} \xi_{trn}(\omega, \alpha)$$

$$\omega^* = \omega' - \xi \frac{\delta \xi_{trn}(\omega, \alpha)}{\delta \omega}$$

$$\delta \xi_{val}(\omega', \alpha) / \delta \alpha - \xi \frac{\delta \xi_{trn}(\omega, \alpha) / \delta \omega}{\delta \omega} = \delta \xi_{trn}(\omega^*, \alpha) - \delta \xi_{trn}(\omega, \alpha) / (2\epsilon \delta \alpha)$$

With the help of analytical modeling of optimization objective, we are able to derive the differentiable polynomial architecture search framework in Algo. 1. The input of search framework includes backbone model $M_b$, dataset $D$, latency loop up table $Lat(OP)$, and hardware resource $H$. The algorithm returns a searched polynomial model $M_p$. The algorithm iteratively trains the architecture parameter $\alpha$ and weight $\omega$ parameter till the convergence. Each $\alpha$ update requires 4 forward paths and 5 backward paths according to Eq. 11 to Eq. 15. And each $\omega$ update needs 1 forward paths and 1 backward paths. After the convergence of training
loop, the algorithm returns a deterministic model architecture by applying Eq. 16. The returned architecture is then used for end to end Cryptographic NN inference evaluation.

\[
OP_1(x) = OP_{k^*}(x), \ s.t. \ k^* = \text{argmax}_k \ \theta_{lk}
\]

(16)

Algorithm 1: Differentiable Polynomial Architecture Search.

Require: \(M_p\): backbone model; \(D\): a specific dataset

\(Lat(O):\) latency loop up table; \(H\): hardware resource

Ensure: Search polynomial model \(M_p\)

1. \(\text{while not converged} \ do\)
2. Sample minibatch \(x_{trn}\) and \(x_{val}\) from \(trn\) and \(val\) dataset
3. // Update architecture parameter \(\alpha\):
4. Forward path to compute \(\xi_{trn}(\omega, \alpha)\) based on \(x_{trn}\)
5. Backward path to compute \(\delta:\alpha = \delta_{k\omega}(\omega, \alpha)\)
6. Virtual step to compute \(\omega' = \omega - \xi \delta_{\omega}\)
7. Forward path to compute \(\xi_{val}(\omega', \alpha)\) based on \(x_{val}\)
8. Backward path to compute \(\delta:\alpha' = \delta_{k\omega}(\omega', \alpha)\)
9. Backward path to compute \(\delta:\alpha'' = \delta_{k\omega}(\omega', \alpha')\)
10. Virtual steps to compute \(\omega'' = \omega + \xi \delta_{\omega}\)
11. Two forward path to compute \(\xi_{trn}(\omega'', \alpha)\)
12. Two backward path to compute \(\delta:\alpha'' = \delta_{k\omega}(\omega'', \alpha)\)
13. Compute hessian \(\delta:\alpha'' = \frac{\partial^2 \xi_{trn}(\omega'', \alpha)}{\partial \alpha''}\)
14. Compute final architecture parameter gradient \(\delta:\alpha = \delta:\alpha'' - \xi \delta:\alpha''\)
15. Update architecture parameter using \(\delta:\alpha\) with Adam optimizer
16. // Update weight parameter \(\alpha\):
17. Forward path to compute \(\xi_{trn}(\omega, \alpha)\) based on \(x_{trn}\)
18. Backward path to compute \(\delta:\alpha = \delta_{\omega}(\omega, \alpha)\)
19. Update architecture parameter using \(\delta:\alpha\) with SGD optimizer
20. \(\text{end while}\)

Obtain architecture by \(OP_1(x) = OP_{k^*}(x), \ s.t. \ k^* = \text{argmax}_k \ \theta_{lk}\)

5 EVALUATION

Hardware setup. Our experiment platform is based on two ZCU104 MPSoCs, both are connected to a router with \(R_{max} = 1000\text{Mb/s}\) though LAN. The load/store bus width is 128-bit and our data is 32-bit, thus, we have \(PP = 4\) and implements on \(f_{req} = 200\text{MHz}\).

Datasets and Backbone Models. We evaluate PolyMPCNet on two public dataset: CIFAR-10 and ImageNet for image classification tasks. CIFAR-10 dataset [55] consists of colored images under size 32 \times 32. It is classified into 10 classes with 60,000 images in total: 50,000 images forms training set and 10,000 forms validation set. ImageNet benchmark [56] consists of RGB images under size 224 \times 224. It has 1000 categories and consists of 1.2 million colored images as training set and 50,000 images as validation set.

Systems Setup. All polynomial architecture search experiments are conducted on Ubuntu 18.04 and Nvidia Quadro RTX 6000 GPU with 24 GB GPU memory. All of the baseline models we used from are implemented with PyTorch v1.8.1 and Python 3.9.7. All the pretrained weight for CIFAR-10 are from [57], and for ImageNet are from Pytorch Hub2. The cryptographic DNN inference experiment is conducted on FPGA-based accelerator for 2PC DNN setup. Two ZCU104 boards are used for server 0 and server 1, which are equipped with XCZU7EV MPSoC for PS-PL system. Two boards are connected to a router with Ethernet LAN setup. The FPGA accelerators are optimized with coarse-grained and fine-grained pipeline structure.

5.1 Algorithm \(\Leftrightarrow\) Hardware Evaluation

Our hardware-aware polynomial architecture search experiment was conducted on CIFAR-10 training dataset. A new training 

validation dataset is randomly sampled from the CIFAR-10 training dataset with 50%-50% split ratio. The new training dataset is used to update the weight parameter of PAS models, and the new validation dataset is used to update the architecture parameter of PAS models.

The latency is modeled through FPGA hardware modeling, and the \(\lambda\) for latency constraint in loss function (Eq. 10) is tuned to generate architectures with different latency-accuracy trade-off. Prior search starts, the major model parameters are randomly initialized and the polynomial activation function is initialized through STPAI method. We use VGG-16 [58], ResNet-18, ResNet-34 [59], and MobileNetV2 [60] as backbone model to evaluate our micro-architecture search performance.

Figure 4: Architecture search accuracy on validation dataset

Fig. 4 shows the accuracy research of our search algorithm with 4 backbone models. With the increase of latency penalty, the searched structure’s accuracy decreases since more polynomial structure is used in the model. After the proper model structure is found during architecture search process, the transfer learning with STPAI is conducted to evaluate the finetuned model accuracy.

The finetuned model accuracy and the searched layer replacement policy can be found in Tab. 2. The baseline model with original setting and all-polynomial operation based model are also included in the table for comparison. Generally, a higher polynomial replacement ratio leads to a lower accuracy. The VGG16 model is the most vulnerable model in the study, while the complete polynomial replacement leads to a 3.2% accuracy degradation. On the other side, ResNet18 and ResNet34 are very robust to full polynomial replacement and there are only 0.33% and 0.26% accuracy drop. MobileNetV2’s is in between the performance of VGG and ResNet, in which a full polynomial replacement leads to 1.27% degradation.

A further accuracy-ReLU count analysis is conducted and compared with SOTA works with ReLU reduction: DeepReDuce [19], DELPHI [20], and CryptoNAS [18]. As shown in Fig. 5, We generate the pareto frontier with best accuracy-ReLU count trade-off from...
Table 2: Finetuned model Top-1 accuracy on CIFAR-10.

|         | VGG16 | Pooling | Act. func | ResNet18 | Pooling | Act. func | ResNet34 |
|---------|-------|---------|-----------|----------|---------|-----------|----------|
|         |       |         |           |          |         |           |          |
|         | ACC (%) | Max | Avg | ReLU | X^2 | ACC (%) | Max | Avg | ReLU | X^2 | ACC (%) | Max | Avg | ReLU | X^2 |
| Le-17 | 93.5 | 6 | 5 | 15 | 0 | 93.2 | 1 | 1 | 17 | 0 | 93.4 | 1 | 1 | 17 | 0 |
| Le-16 | 92.6 | 2 | 3 | 12 | 3 | 93.4 | 1 | 1 | 12 | 5 | 93.6 | 1 | 1 | 12 | 5 |
| Le-15 | 91.9 | 4 | 5 | 10 | 5 | 93.8 | 1 | 1 | 9 | 8 |
| Le-14 | 90.3 | 3 | 4 | 11 | 2 | 93.8 | 1 | 1 | 6 | 11 |
| Le-13 | 90.9 | 3 | 3 | 12 | 2 | 93.9 | 0 | 2 | 2 | 13 |
| Le-12 | 90.2 | 3 | 5 | 0 | 15 | 93.9 | 2 | 0 | 17 |

|         | MobileNetV2 | Pooling | Act. func | ResNet18 | Pooling | Act. func | ResNet34 |
|---------|-------------|---------|-----------|----------|---------|-----------|----------|
|         |             |         |           |          |         |           |          |
|         | ACC (%) | Max | Avg | ReLU | X^2 | ACC (%) | Max | Avg | ReLU | X^2 | ACC (%) | Max | Avg | ReLU | X^2 |
| Le-17 | 94.0 | 6 | 0 | 23 | 12 | 93.8 | 1 | 1 | 25 | 8 |
| Le-16 | 93.9 | 6 | 0 | 17 | 18 | 93.8 | 0 | 2 | 14 | 19 |
| Le-15 | 93.8 | 2 | 14 | 21 | 5 | 93.3 | 0 | 2 | 6 | 27 |
| Le-14 | 93.4 | 0 | 1 | 34 | 2 | 93.7 | 0 | 2 | 30 |
| Le-13 | 92.9 | 0 | 0 | 35 | 1 | 93.5 | 0 | 2 | 53 |

Table 3: PolyMPCNet evaluation & cross-work comparison with CryptGPU [26] and CryptFLOW [23]

|                     | CIFAR-10 dataset |                     | ImageNet dataset |                     |
|---------------------|-------------------|---------------------|-------------------|---------------------|
|                     | Top 1 (%) | Lat. (s) | Comm. (GB) | EFF (1/(s*kW)) | Top 5 (%) | Lat. (s) | Comm. (GB) | EFF (1/(s*kW)) |
| PolyMPCNet-A | 93.97 | 3.1 | 0.0124 | 20.2 | 89.99 | 4.4 | 0.0179 | 14.2 |
| PolyMPCNet-B | 92.95 | 2.4 | 0.039 | 13.4 | 76.79 | 19.4 | 0.0479 | 9.2 |
| PolyMPCNet-C | 92.62 | 11.0 | 0.0117 | 5.7 | 71.26 | 13.4 | 0.0484 | 4.7 |
| CryptGPU/ResNet18 | \ | \ | \ | \ | 78 | 92 | 9.31 | 3.08 |
| CryptFLOW/ResNet18 | \ | \ | \ | \ | 76.45 | 91.25 | 25.9 | 6.9 |

Figure 5: Accuracy-ReLU count trade-off on CIFAR-10.

Figure 6: ReLU reduction comparison on CIFAR-10.

Our architecture search result. We name the selected models as PolyMPCNet, and compare it with other works. The accuracy-ReLU count comparison is show in Fig. 6. Our work achieves a much higher ReLU replacement ratio than existing works with only subtle accuracy degradation.

Based on CIFAR-10 dataset evaluation, we pick up 3 searched PolyMPCNet model variants (PolyMPCNet-A, PolyMPCNet-B, and PolyMPCNet-C) for CIFAR-10 & ImageNet dataset accuracy & latency evaluation. PolyMPCNet-A and PolyMPCNet-B share the same backbone model as ResNet-18 but with a different activation layer architecture. PolyMPCNet-A has only polynomial operators and PolyMPCNet-B has 1 2PC-MaxPool layers and 11 2PC-ReLU layers. PolyMPCNet-C is derived from MobileNetV2 with all polynomial layers. Note that the baseline top-1 accuracy of ResNet-18 on CIFAR-10 and ImageNet are 93.7% and 69.7%, and the baseline top-1 accuracy of MobileNetV2 on CIFAR-10 and ImageNet are 94.09% and 71.88%. We further transform the float point number in PolyMPCNet to 32-bit fixed point number for secure protocol implementation.

The PolyMPCNet variant evaluation result and cross-work comparison with SOTA CryptGPU [26] and CryptFLOW [23] implementation can be found in Tab. 3. We observe 0.78% and 1.03% top-1 accuracy increase for our PolyMPCNet-A and PolyMPCNet-B compared to baseline ResNet18 performance on ImageNet. And we achieve only 0.13% accuracy drop for our PolyMPCNet-C compared to baseline MobileNetV2 performance on ImageNet. Even with the ZCU 104 edge devices setting, we are able to achieve a comparable secure inference latency as SOTA works implemented on the large-scale server system. Meanwhile, our PolyMPCNet-A achieves more than 90× more energy efficiency than CryptGPU. With the polynomial activation layers, the proposed PolyMPCNet-A is able to achieve 156× communication volume reduction than SOTA CryptGPU work. PolyMPCNet is more shallow than the ResNet50 implemented in CryptGPU and CryptFLOW, so our accuracy is reasonably lower than their works.

6 CONCLUSION

In this work, as the first attempt, we develop a systematic framework, PolyMPCNet, of joint overhead reduction of MPC comparison protocol and hardware acceleration, by integrating hardware latency of the cryptographic building block into the DNN loss function design to achieve high energy efficiency, accuracy, and security guarantee. We propose a straight through polynomial activation initialization method for cryptographic hardware friendly trainable polynomial activation function to replace the expensive 2P-ReLU operator. We develop a cryptographic hardware scheduler and the corresponding performance model for FPGA platform, the latency loop up table can be constructed based on such model. We start with the DNN optimization stage, and integrate latency of the cryptographic building block into the DNN loss function to facilitate escaping the local minima and saddle points, therefore achieving high accuracy. Then we propose a differentiable cryptographic hardware-aware micro-architecture search framework to select the proper polynomial or non-polynomial activation based on given constraint. On hardware platforms, Our proposed 2PC-aware polynomial architecture search framework models the latency of each 2PC operator on the FPGA platform and evaluate the trade-off between latency and accuracy of 2PC-NN. Experiments show that we are able to achieve all polynomial replacement with 0.78% top-1 accuracy improvement for PolyMPCNet-A model (ResNet18 as
baseline) on ImageNet dataset, and an even higher top-1 accuracy for PolyMPCNet-B model with partial polynomial replacement.

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