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Development of GEM trigger electronics for the J-PARC E16 experiment

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Abstract. At the J-PARC E16 experiment[1], we measure mass spectra of vector mesons in nuclei from the $e^+e^-$ decay channel with high precision and high statistics. We have developed the trigger system consisting of newly developed ASD ASICs which can extract signals from the GEM foil used as a cathode plane of the induction gap in a GEM chamber and digital electronics using FPGAs which processes binary signals from the ASIC.

1. Introduction
The purpose of the J-PARC E16 experiment is to investigate an origin of hadron mass and the chiral symmetry restoration in nuclear matter. In the experiment, we measure mass spectra of vector mesons in nuclei from the $e^+e^-$ decay channel with high precision and high statistics. Shown in Fig. 1, a spectrometer of the experiment is developed and, GEM Trackers (GTR), which are composed of three layers of tracking planes in a magnetic field, are used to measure momenta of the decay electrons in high counting-rate environment. Hadron Blind Detectors (HBD), which are gas Cerenkov counters using GEM, and Lead Glass Calorimeters (LG) are placed outside the GTR to identify electrons. Efficient trigger system selecting events of $e^+e^-$ decays from huge background events must be constructed in order to reduce the trigger rate to 1-2 kHz that our data acquisition system can cope with.

2. E16 trigger system
The design of the E16 trigger system is shown in Fig. 2. The $e^+e^-$ event trigger consists of three-fold coincidence of signals from the most outside GTR, HBD and LG. The number of channels for the trigger of GTR, HBD and LG is approximately 620, 940, and 1000, respectively. The trigger signals of $300 \times 300$ mm$^2$ GTR and HBD are picked up from a cathode plane of an induction gap of GEM chambers, namely, the last GEM foil in the stack, by Amplifier-Shaper-Discriminator (ASD) ASICs. The binary signals from the ASD preamp boards are converted to the timing information on the Trigger Merger board (TRG-MRG). The merged information of hit channels and timing on the TRG-MRG is sent to a global trigger decision module using a
0◦ ∼ ±12◦ both vertically and horizontally to avoid beam halo. Schematic view of the geometrical acceptances are shown in Fig. 11.

Figure 1. Schematic view of the proposed new spectrometer (plan view/beam view). Green and red area represents pole piece and coil, respectively.

The list of detectors is shown in Table 1. The spectrometer has a large magnet and detectors. We will use the same magnet used by E325. The tracking device consists of 3 layers of GEM trackers and outside tracker. Particle momentum is mainly determined by Gas Electron Multiplier (GEM) trackers. The GEM tracker is originally developed for the COMPASS experiment[21] for high rate counting and is also used at RCNP[22]. The outside tracker

Figure 1. Schematic view of the spectrometer

high-speed optical link. We utilize two modules for the trigger decision, and generation of global trigger and clock distribution, Universal Trigger Board (UT3) and Front-end Timing Switch (FTSW), which are developed for Level-1 trigger system of the Belle-II experiment[2].

Details of the trigger electronics which consists of analog and digital signal processings are described in a following section.

3. Trigger electronics

The trigger electronics of the GEM chambers consists of analog and digital signal processing units as preamp boards for the detectors and digital signal processing units having the TRG-MRG which receives digital signals from the preamp cards and sends hit information to the global trigger decision module, UT3 and the FTSW.
3.1. Analog signal processing

We developed new Amplifier-Shaper-Discriminator (ASD) ASICs which can deal with large detector capacitance originating from GEM and have a short shaping time to handle the high rate counting. A photograph of the ASD ASIC chip is shown in Fig.3. The first idea to extract the trigger signal from these GEM detectors, such as GTR and HBD, is utilizing signals of strips or pads on the anode readout plane which are originally used for tracking or electron identification. However, this idea requires R&D of complex front-end circuits and a large number of channels for the fast signal outputs. In order to avoid these problems, trigger signals are picked up from a cathode plane of an induction gap of these GEM chambers, namely, the last GEM foil in the stack. Considering using signals from the GEM foil, it is difficult to cope with large capacitance of the order of nF by using normal preamps.

The trigger electronics for GTR need to cope with the large detector capacitance of approximately 2 nF, a fast shaping time, and a good signal-to-noise ratio for the minimum input charge of 10 fC. The cathode plane of a GEM foil of the most outside GTR, whose size is $300 \times 300$ mm$^2$, has detector capacitance of about 50 nF. The GEM foil is divided into 24 segments in order to reduce the capacitance to about 2 nF and also a counting rate in each segment. These segments can be used for roughly track charged particles. The rough tracking has an important role of decreasing a background of electrons which do not come from targets. In the forward region of the spectrometer, the maximum hit rate of each segment is expected to be 1-2 MHz. Thus, we set the shaping time to 25 ns corresponding to a pulse width of about 200 ns. The electric circuit of the ASIC was designed to suppress Equivalent Noise Charge (ENC) under $2 \times 10^4$ for the input detector capacitance of 2 nF. The ASD ASIC chip satisfying the above requirements has been developed by our group in cooperation with the Open-It[3] project. The ASIC has a digital section containing an 8-bit register for control of a comparator on-off, a polarity of the comparator and an adjustment of each comparator threshold. A channel-by-channel fluctuation of the threshold can be compensated by the adjustment using a 4-bit internal DAC. The ASIC for the GTR is modified and used as the electronics for the trigger of the HBD.

A prototype of a preamp board with the ASIC chips was produced as shown in Fig.4. Size of the board should be enough small to be installed in small spaces of GTR modules. One of functions of the preamp board is to convert discriminated digital outputs of the ASIC to parallel LVDS signals which are sent to the TRG-MRG. Also, the board is required to receive slow control signals from the TRG-MRG to activate and control digital functions of the ASIC. We confirmed that the cathode signals from the GEM foil of GTR can be extracted using the

![Figure 3. A photograph of the ASD ASIC chip.](image1)

![Figure 4. A photograph of the ASD preamp board.](image2)
preamp board.

3.2. Digital signal processing

Digital signals from the ASD preamp board are handled by the TRG-MRG. The TRG-MRG consists of a carrier card and two mezzanine cards as shown in Fig. 5. The TRG-MRG carrier card has a Xilinx Kintex-7 FPGA, two FMC slots, eight SFP+ transceiver slots and the trigger-clock interfaces. The board is a 9U form factor without a back plane. The TRG-MRG mezzanine card has 96 channel LVDS receivers per card and the slow control interface for the ASD preamp boards.

Firmware of the TRG-MRG has been developed for pre-processing and serializing the trigger signals from GTR, HBD and LG. The LVDS signals from the ASD preamp boards are converted to timing information with better than 10 ns resolution on the TRG-MRG board as shown in Fig. 6. Time stamps of the ASD hits are determined by the global clock of 125 MHz. A difference of a cable delay is compensated by delay buffers on the FPGA. Timing information is packed in a data frame with a fixed length of about 250 bits. The data frame contains up to 8 hits, and additional information such as the data source ID, number of hits and error flags. The data frame is 64b66b encoded and sent to the UT3 module every 64 ns using Xilinx Aurora 64b66b protocol. Test of the TRG-MRG is on going. The UT3 module is a triple-slot wide 6U VME module with a Xilinx Virtex-6 HXT FPGA and 64 multi-gigabit transceivers. The UT3 module gathers trigger signals from 2548 trigger segments and generates a Level-1 event trigger using a coincidence matrix of GTR × HBD × LG. The event trigger is broadcasted via the FTSW as a serialized and encoded data.

4. Summary

An ASD ASIC for the trigger using signals from the cathode plane of a GEM foil was developed. A preamp card with the ASICs was developed. We confirmed that the ASIC satisfies the requirements and the cathode signal from GTR can be extracted using the preamp card.

In order to handle digital signals from the ASIC, we developed the TRG-MRG which converts the LVDS signals to information of hit channels and timing and sends the information to the...
UT3 using Xilinx Aurora 64b66b protocol. Firmware of the TRG-MRG has been developed and test is on going.

[1] http://j-parc.jp/researcher/Hadron/en/pac_0606/pdf/p16-Yokkaichi_2.pdf
[2] Iwasaki Y et al 2011 Level 1 Trigger System for the Belle II Experiment, *Nuclear Science, IEEE Transactions* **58**, 4, 1807-1815. doi: 10.1109/TNS.2011.2119329
[3] http://openit.kek.jp/