Design and performance of MPPC-array readout system for the WAGASCI neutrino detector

Kohei Matsushita\textsuperscript{1} on behalf of the WAGASCI collaboration

\textsuperscript{1}University of Tokyo, 7-3-1 Hongo, Bunkyo, Tokyo 113-0033, Japan

E-mail: kohei@hep.phys.s.u-tokyo.ac.jp

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We have developed a readout system for the WAGASCI neutrino detector at J-PARC. A WAGASCI module uses 1280 MPPC channels to detect light from scintillators via wavelength shifting fibers. The frontend electronics is based on Silicon PM Integrated Read-Out Chip (SPIROC), which has large dynamic range, low noise, low power consumption, high precision and large number of readout channels. The data taking began in October 2017. All of the MPPC gains were stable within $\pm10\%$ for about four months of operation. After the first commissioning, the timing resolution was improved by an update of firmware.

KEYWORDS: neutrino detector, readout electronics

1. The WAGASCI detector

In order to reduce the uncertainties in the T2K long baseline neutrino oscillation experiment, we developed a new neutrino detector named WAGASCI [1]. The purpose of the WAGASCI detector is to improve the understanding of the neutrino interaction by measuring the charged-current neutrino cross section ratio between water and hydrocarbon with a large phase space. A schematic view of the WAGASCI detector is shown in Fig. 1.

A WAGASCI module is composed of 1280 plastic scintillator bars which make a three-
dimensional grid structure with gaps filled by water (Fig. 2) which serves as the neutrino interaction target. The WAGASCI module is designed to have 4 \( \pi \) angular acceptance for charged particles. Thin plastic scintillator bars, the thickness of which is 3mm, are used to reduce the mass ratio of scintillator bar to water because neutrino interactions in the scintillator bars are a background for the cross section measurement on water. The mass ratio of the scintillator bars to water is 1:4. The light from scintillators is read out by MPPCs via wave length shifting fibers. The WAGASCI detector is installed and operated at J-PARC neutrino monitor hall, Tokai, Ibaraki, Japan.

### 2. MPPC-array readout system

In a WAGASCI module, forty 32-channel arrayed MPPCs (Fig. 5) for a total number of 1280 channels are used. In order to read out signals from MPPC arrays, a dedicated readout system [2] was designed by LLR, Ecole Polytechnique based on a system developed for the ILC calorimeter [3]. The system is based on Silicon PM Integrated Read-Out Chip (SPIROC, Fig. 3) [4], version SPIROC2D, which can control and readout 36 MPPC channels. The bias voltage of each MPPC can be individually adjusted. The charge is measured with a range of one to 2,000 photoelectrons, and time information is recorded with 100 ps step.

A front-end electronics board, Active Sensor Unit (ASU), is designed to control a 32-channel arrayed MPPC. Signals readout from ASU are processed through an interface board (IF) and a detector interface (DIF) which controls SPIROC chips. Giga data concentrator card (GDCC) communicates with DAQ PC and the output data from DIF are sent to DAQ PC via GDCC. The whole system is synchronized to a 50MHz clock by Clock Control Card (CCC). The electronics readout scheme is shown in Fig. 4.

![SPIROC on the ASU board.](image)

**Fig. 3.** SPIROC on the ASU board. All ASU boards we need were manufactured and installed to the WAGASCI detector. We operate the detector with these ASU boards.

The readout system is synchronized to the neutrino beam timing using two timing signals, *pre-beam trigger* and *beam trigger*. The pre-beam trigger signal arrives 100 ms before the arrival of the beam trigger signal and the beam trigger signal arrives about 30 \( \mu s \) before the neutrino beam. With receipt of those signals, CCC sends DIF a digital signal to open an acquisition gate for the neutrino beam data. After the acquisition gate for the neutrino beam is closed, periodic acquisition gate is opened to accumulate data for monitoring the detector stability. Fig. 7 shows a schematic timing chart for the timing synchronization.
3. Performance

We have confirmed the performance of readout system during the data taking with neutrino beam, from October 22nd, 2017 to May 24th, 2018. A couple of examples of measured performances are given below.

3.1 Gain stability

Performance of MPPC is sensitive to temperature and bias voltage. The gain of MPPC is a sensitive probe to monitor the stability of MPPC performance. A DAC is implemented in SPIROC to adjust bias voltage of individual MPPC, so that the performance can be kept stable. Fig. 6 shows the gain history from October 22nd, 2017 to May 24th, 2018. All of the channels are stable within $\pm 10\%$ over the whole period.

3.2 Timing resolution

In the neutrino beam run, it was found that the timing resolution was much worse than expected. In order to improve the timing resolution, we have improved the DIF firmware in 2018. DIF, just after receiving a beam trigger signal from CCC, generates an acquisition gate which is synchronized with the internal 580ns-period clock. With the old firmware, because
the DIF internal clock was not reset on each acquisition, a random jitter between the beam trigger signal and the start of acquisition gate existed. In the updated firmware, the DIF internal clock is reset every time DIF receives the beam trigger signal from CCC and the random jitter is removed. Fig. 9 shows the results of timing measurement using LED light with old and new firmware. The timing resolution has been improved from about 900 ns to about 40 ns, so that the timing resolution becomes sufficient to distinguish the different bunches of the neutrino beam. The updated firmware will be applied in the next physics run. Further improvement is being investigated, which might allow determining the direction of scattering particles using the hit time information.

4. Summary

We have developed a MPPC-array readout system based on the SPIROC frontend ASIC for the WAGASCI neutrino detector. The detector has been built, commissioned and tested with neutrino beam. The electronics system successfully worked to read out 1280 MPPCs and the basic performance was verified to be consistent with expectations.

References

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