Analog Multipliers-Based Double Output Voltage Phase Detector for Low-Frequency Demodulation of Frequency Modulated Signals

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ABSTRACT This work deals with the design of a simple double output voltage phase detector, using a specific type of analog multiplier, and its application in a frequency demodulator. The design of active parts was performed in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm 1.8 V CMOS technology. The intention is devoted to design the circuitry in such a way to avoid low-frequency signal processing with large values of capacities that are not available in case of on-chip implementation. The idea consists in the processing of significantly faster signal (tens of kHz) carrying modulated low frequency information. Then the coupling capacity may have significantly smaller value. The operation of the demodulator was tested for carrier frequency 50 kHz and for modulation signal with frequency of 10 Hz and 500 Hz. Differences of these frequencies approximately determine the values of capacitors required for AC coupling. Simulations (Cadence Spectre simulator) as well as experimental measurement, using fabricated ASIC prototypes, are provided to verify the proposed circuits in both the time and frequency domain.

INDEX TERMS All-pass filter, CMOS multiplier, electronic adjustment, frequency demodulation, phase detector, phase shifter.

I. INTRODUCTION
A. MOTIVATION OF THE DESIGN
The on-chip signal processing is significantly limited for low-frequency signals because of the values of available capacitors (units of pF in modern CMOS processes per capacitor, tens of pF when connected in parallel but a large silicon area is occupied) [1]. It also omits low-frequency signals from the processing in these devices when AC coupling between internal stages or cells (functional blocks respectively) is required. However, applications operating with very low frequencies receive increasing attention (see for example integrated filters for the field of Hz and sub-Hz bands [2], [3]) because low-frequency responses are typical in sensing of nonelectrical quantities (for instance low-frequency vibrations and seismic activities [4]–[6]). It is necessary to use AC coupling in complex processing systems because of many reasons (e.g. separation of DC component, different DC operating points and principles of partial blocks). Values of coupling capacitors can easily overcome tens-hundreds of nF or even units of µF for low cut-off frequency $f_{-3dB}$ hundreds of Hz and below. Therefore, it is important to find a way how to avoid the necessity of such large values unpractical in case of on-chip systems. Fortunately, majority of designs in the field of analog signal processing has no requirements on power propagation through the system. Therefore, small voltage and current levels can be processed by active elements and functional blocks operating linearly with levels of low hundreds of mV and tens of µA. Synthetic capacitance multipliers [7] offer some possibility to the design an equivalent capacitor of higher value from the active circuit and capacitor with low value. However, their...
application in floating form requires extensive circuitry very often [8] and, therefore, is not very useful for these cases.

The idea presented in this work is to explore processing of low-frequency signals transposed from base-band slowly changing signals (e.g. from biosensors or sensors of non-electrical quantities) by modulation techniques known from radio communication technologies [9] to higher frequency bands. Low-frequency signal in hundreds of Hz or lower can be represented by readouts working with biological signals. Transposition of such a baseband signal to 10 or 100 times higher frequency band brings significant advantages. It can be distributed/propagated by the processing chain integrated on an IC. The coupling capacitors could have 10, 100 or 1000 times smaller value. Therefore, the total silicon area and also the final expenses can be significantly reduced. Moreover, in the case of the transmission of a modulated signal, common amplitude distortions and additive noise can be suppressed. Figure 1 shows the principal block scheme using frequency modulation (FM) and demodulation procedure. Of course, the demodulation process supposes as it is also shown here the presence of large values of capacitors for integration procedure. Fortunately, these elements are placed at the end of the processing sequence and they are external parts. In this paper, we focus on the end-processing of the signal, more precisely on the verification of demodulation stage). The design of the block, indicated by the red color, is the main goal of this work. The FM modulator can be any voltage-controlled oscillator (VCO) and particular solution is off the interest of this paper.

Our work has the following goals:

a) simplicity,
b) differential output (2x higher voltage level if necessary),
c) simple electronic adjustability of phase shifter and frequency demodulator (by DC driving voltage),
d) single-parameter simultaneous adjustment of zero/pole frequency of the phase shifter,
e) all grounded passive elements and,
f) high-impedance inputs.

This work is divided into the following sections: Section 1 presents the motivation of this work and deals with state-of-the-art features of modern CMOS multipliers (MLTs) and phase shifters as well as overview of phase detectors in various demodulating applications. Section 2 introduces the used active device (CMOS implementation of multiplier circuit). Operation of the proposed double output voltage phase detector is derived in Section 3. Section 4 completes the application example of the detector in a simple frequency demodulator. Verification of the features of the partial blocks as well as the complete demodulator is given in Section 5. Section 6 concludes this work.

B. BRIEF STATE-OF-THE-ART OF BUILDING ELEMENTS

Our design uses several building parts (phase detector and phase shifter) based on analog CMOS multiplier, fabricated lately in CMOS process. Comparison of these blocks and elements with state of the art is presented in the following sections.

1) CMOS MULTIPLIER

The analog multiplier represents the key part of our design. The basic principle of the multiplier can be studied in [10] and [11]. Many other solutions have been presented in recent literature. Table 1 represents a comparison of recent CMOS multipliers operating in various regimes (saturation, triode) and performing product of input currents or input voltages, having various input/output ranges, bandwidths, etc. Particular features always depend on the specific purpose of these designs.

The analysis of the features of solutions [12]–[46], presented in Table 1, gives the following conclusions:

a) many circuits are not directly suitable for voltage-mode and mixed mode applications because they have insufficiently low impedance of current input terminals [12]–[17], [19]–[24], [27], [28], [32], [35]–[37], [40], [41], [43]–[45],
b) voltage input terminals are available in limited number of cases [18], [26], [29]–[31], [33], [34], [38], [39], [42], [46],
c) many circuits process only very low-level signals (dynamical limitation) unsuitable for many purposes (especially [13], [17], [23], [38]), in other words only [31] and [46] are acceptable for our purposes but another features are not fulfilled or significant enhancement is required,
TABLE 1. Comparison of CMOS topologies of multipliers available in literature.

| Reference | Type of CMOS process | Supply voltage | Input-output resistance | d) all solutions in Table 1 have only one single output and, e) the value of output resistance is not known as well as information about its variability when the input levels of the multiplier are changed or DC voltage is connected to selected pair of input terminals in order to operate as operational transconductance amplifier (independence on driving process [47]). On the other hand, numerous compared circuits have larger bandwidth, lower power consumption or smaller chip area. However, these features are not the key parameters for our application. There is always a trade-off between these parameters. Moreover, high-frequency behavior of several of mentioned solutions brings some questions because no information about bonding and load effects (load capacity) is given. Unfortunately, in many cases, only PSpice-based simulations were provided. In addition, different processes and supply voltage limit reproducibility (adopter) of known concepts in different CMOS technologies (at least with identical features). Therefore, substantial reasons for design of own MLT cell exist. The multiplier suitable for our application should fulfill the following specification: a) large input voltage range (at least ±200 mV), b) large output current range (at least ±200 µA), two pairs of differential input voltage (high-impedance) terminals, two complementary current output (high-impedance) terminals, c) constant output small-signal resistance (~100 kΩ) for variable input voltage (independent on driving process), d) bandwidth wider than 40 MHz (load capacity 10-15 pF) and e) power consumption below 10 mW. All these aspects were not fulfilled simultaneously by known topologies presented in recent literature as can be seen in Table 1. The complete topology and details about the design of CMOS multiplier used in this work are available in [47].

Table 1 indicates many interesting MLT concepts having only two input terminals (two single-ended voltages). Unfortunately, two single-ended input voltages cannot be used in the system presented in our paper. We require construction of an operational transconductance amplifier based on MLT for further parts of the system and there are used fully differential inputs. Therefore, four input terminals (two differential input voltages) are expected from MLT. Lack of two symmetrical outputs of the other MLTs also does not allow construction of double voltage output phase detector (detection of doubled output levels). Simple extension of the particular CMOS topology to second current output is not always easy task because additional current mirrors and current inverters cause significant drop of bandwidth due to increased C_{GS}
TABLE 2. Brief comparison of relevant electronically adjustable first-order OTA-based phase shifters (all-pass filters).

| Reference | Number of active elements (type) | Grounded capacitor | Zero/pole frequency adjustable simultaneously by single parameter | OTA designed in technology | Electronic adjustment by | Dependence of transconductance (zero/pole frequency) on driving force | Matching of two or more parameters in design not required | Matching of parameters in design not required | High input impedance | Linear processing of levels at least hundreds of mV |
|-----------|---------------------------------|--------------------|---------------------------------------------------------------|----------------------------|------------------------|---------------------------------------------------------------|-----------------------------------------------|-----------------------------------------------|-------------------------------|---------------------------------------------|
| [48]      | 2                               | No                 | No                                                            | Yes                        | linear                 | No                                                            | No                                    | No                             | N/A                           | No                           |
| [50]      | 1                               | No                 | Yes                                                           | Yes                        | linear                 | Yes                                                            | No                                    | No                             | N/A                           | No                           |
| [51]      | 3                               | Yes                | No                                                            | No                         | CMOS                   | nonlinear                                                      | No                                    | No                             | Yes                           | No                           |
| [52]      | 3                               | No                 | No                                                            | Yes                        | CMOS                   | linear                                                         | No                                    | No                             | No                            | No (60 mV<sub>pp</sub>) |
| [53]      | 2                               | Yes                | No                                                            | Yes                        | CMOS                   | nonlinear                                                      | No                                    | No                             | No                            | N/A                           |
| [54]      | 2                               | Yes                | No                                                            | No                         | NA                     | linear                                                         | No                                    | No                             | No                            | N/A                           |
| [55]      | 2                               | No                 | No                                                            | Yes                        | NA                     | linear                                                         | No                                    | No                             | No                            | N/A                           |
| [56]      | 2                               | Yes                | Yes                                                           | Yes                        | both                   | linear                                                         | Yes                                   | No                             | No                            | No (50 mV<sub>pp</sub>) |

Fig. 5 2 (C, R) Yes Yes CMOS DC voltage (no bias) linear Yes No Yes Yes

N/A – information not available, not verified, solved, tested

capacities in internal topology. We can see that only two other solutions [33], [46] (from several tens of examples) fulfill partially requirements of our application but substantial reasons, why they cannot be used, remain.

2) PHASE SHIFTER

In our system, the phase shifter is an important part of the design. The used CMOS multiplier can be applied as a simple differential input differential output operational transconductance amplifier (OTA) [48]. We provided a survey (summarized in Table 2) of solutions using OTAs applied (only OTAs are accepted as suitable active devices) in first-order all-pass filters (phase shifters) [49] and revealed the following conclusions:

a) the zero/pole frequency cannot be adjusted simultaneously (as requested typically) by a single parameter in all cases (matching condition is required in each case except [50], [56]),

b) solution [50], where the electronic adjustment is possible by single parameter, requires two floating capacitors (matched design) and does not possess high-impedance input (useful when exposition of the signal at input node to the frequency dependent load is an issue),

c) linear voltage electronic tuning is not available in case of CMOS-based OTA solutions [51], [53], [54], [56],

d) there are solutions without grounded capacitor unsuitable for on-chip integration [48], [50], [52], [54],

e) available range of linear processing of signal levels in all-pass structures is not often reported or with quite low range, if tested [52], [56] (correct signal processing of our system requires operation in hundreds of mV) and

f) some matching condition is required for correct operation of all solutions presented in Table 2 (including our case) but the adjustment of zero/pole frequency has no influence on matching condition in our case (filter features) that is fixed during the adjustment.

Other solutions in Table 2 expect simultaneous driving of two [48], [53]–[55] or more transconductances and matching condition fulfillment simultaneously [51], [52] for correct operation. Our design supposes single parameter linear zero/pole electronic frequency adjustment, high-input impedance, grounded capacitor and linear dependency of transconductance on driving parameter (DC voltage).

Topologically similar OTA-based solution of the phase shifter, can be obtained from general multifunctional concept presented by Jaikla et. al [56]. Unfortunately, linear adjustment of zero/pole frequency by DC voltage is not available and dependence of zero/pole frequency on driving parameter (bias current) is not studied. The design in [56] can be considered as a useful alternative of used phase shifter. However, some features (linearity, limited signal levels of processed voltage, absence of linear DC voltage driving not influencing bias conditions, i.e. output resistance of OTA independent on bias current/voltage and not affecting performance of applications) of solution from [56] do not allow immediate employment in our system.

Many further solutions of active phase shifters (all-pass filters) exists in literature using various active elements suitable for the design of these filtering and phase shifting applications [49] (current conveyors, current feedback operational amplifiers, current amplifiers, advanced types connecting several basic parts, etc.). Unfortunately, some of their features can be insufficient for our concepts (input resistance, electronic adjustability, nonlinearity of dependences and...
transfer responses). Therefore, Table 2 includes OTA-based phase shifters.

3) PHASE DETECTOR AND APPLICATION IN THE FREQUENCY DEMODULATOR

Phase detectors are important parts of modulation and demodulation schemes in modern communication systems [9]. Their features can be also beneficially utilized in the key parts of phase locked loops (PLL) [9] that create important blocks of many classical analog as well as modern digital modulation schemes [9], [57]. Dominant part of solutions of phase detectors belongs to the digital field (implementation by logical functions OR, NOR) [58]. Numerous implementations of modulator and demodulator are fully digital [59]. However, these systems address high-frequency behavior (very high-power consumption, high-speed platform, etc.). Standard analog examples of radio transceivers can be found in [60] and [61]. Their similarity to our work consists in the application of standard analog multiplier for phase detection. Other parts of concepts are more sophisticated due to different requirements (modulation/demodulation of in-phase and quadrature branch for digital modulation schemes). Standard receiver using FM demodulation can be found for example in [62]. Operation of phase detector and the complete FM demodulator is principally very similar to our case. However, the phase shifter in [62] is not employing a pure all-pass filter (only resonant RLC circuit is sufficient due to high-frequency application and large ratio of center frequency to operational bandwidth of the demodulator). Unfortunately, such a concept cannot be used in low-frequency applications (presence of coils of inappropriate features for low-frequency bands) beneficially. The proposed solution targets on low-frequency band (tens of kHz) and processing of baseband signals (hundreds of Hz). Table 3 compares the proposed design of phase detector for demodulation of a low-frequency signal and its application with several recently reported solutions.

The applications target on RF systems and receivers for the domain of GHz and MHz [57], [62]–[65], but also on low frequency systems for various purposes [58], [66]. However, for wireless transfer of signal in most cases. Therefore, the low-frequency field is not typical for similar approaches as discussed in this paper. Numerous phase detectors serve for construction of PLL [58], [63]–[65] or directly for demodulation in different digital modulation schemes [57], [63]. Only several cases represent the standard application in FM radio receiver [61], [62].

The main differences between the proposed and previous concepts are in utilization of linear multiplier, used in work [66], (linear in a specific range of input voltages), that is not always required and also in the type of the filter (active tunable all-pass solution). This feature allows a simple modification of the parameters of the demodulator. Different modulated carrier (middle) input frequency can be set without necessity of voltage controlled oscillator as in case of PLL. All-pass filter seems to be also more beneficial than employment of a simple RLC resonator that must be redesigned (different values of elements) when carrier frequency is changed. Significant benefit also yields from availability of double-output voltage level of phase detector. Low-voltage CMOS technologies have drawback of small processed voltages (several tens of mV) very often. It presents issue for signal-to-noise ratio, available ranges of adjustabilities, and obtaining sufficient level for further processing by analog-to-digital converter, etc. We can see that also complexity of demodulators can be higher [61]–[65] than in the presented case, especially in cases of phase locked loop – PLL (VCO necessary).

C. SUMMARIZATION OF CONTRIBUTION AND NOVELTY OF PRESENTED DESIGN

Contribution and novelty of the proposed building parts and whole application, regarding detailed tabular comparisons, can be summarized in the following paragraphs.

1) BUILDING PARTS

The most important practically useful features of the used multiplier among other works (see Table 1) are: a) four inputs (two differential pairs of voltages) and two current outputs (a pair of fully symmetrical output currents), 2) differential output has benefits for low-voltage application (doubled level of signals), 3) sufficiently high value of output resistance independent on input voltage levels (not reported in other works), 4) sufficient levels (linearly processed) of input voltages and output currents simultaneously (in most cases, previous works indicated only fulfilment of this condition at the input or output).

The most important contributions of the presented simple phase shifter with respect to other works (in Table 2) are: 1) single parameter electronic tunability without matching condition (for tuning) and without influence on biasing conditions (input/output resistance, linearity, etc.) of the used active device – no bias current adjustment used as typical in standard concepts of OTAs, 2) high input impedance, 3) grounded passive elements, 4) quite high levels of processed signals (better dynamics and linearity) in comparison to concepts (using standard OTAs) having the most similar features or topologies [56].

2) DESIGNED APPLICATION EXAMPLE (FREQUENCY DEMODULATOR USING PHASE DETECTOR AND PHASE SHIFTER)

Based on Table 3, the phase detector applied in frequency demodulator (complete system) has the following significant novelty and advantages: 1) simple solution for frequency demodulation without requirement of more complex PLL method, 2) low complexity of phase detector (multiplier and passive RC load) – some solutions require complex low-pass filter [58], 3) electronically tunable phase-shifter (i.e. modulated carrier wave, can be easily modified in frequency in comparison to standard passive solutions in other works) 4) no requirement of precise voltage
controlled oscillator (VCO) in comparison with PLL concepts [63]–[65]. Frequency modulation/demodulation is standardly used for RF wireless communication systems (examples are [57], [61]–[65]) but purpose of this methodology in our work is different.

Our work shows employment of modulation technique for transpositions of signals in wired environment without necessity of wireless transport of information (wire connection always exists). The method, in comparison to others, does not use mixer (and local oscillator) and it never uses constant inter-frequency wave for demodulation as typical for superheterodynes. It targets on transposition of very slow signals to higher frequencies for their better propagation by the system without coupling capacity issues (typically on IC – large values in nF are not feasible). To the best of authors’ knowledge, similar purpose of frequency modulation/demodulation was not elaborated in the past.

### II. SHORT DESCRIPTION OF ANALOG CMOS MULTIPLIER

Recently, we have developed a compact topology of CMOS multiplier in 0.18 μm 1.8 V Taiwan Semiconductor Manufacturing Company (TSMC) CMOS process [67]. The device, as it is shown in Fig. 2 (including internal topology, note that ESD precautions are not shown for simplicity), performs multiplication of two input differential voltages and provides their product in a form of two complementary (inverting and noninverting terminal) output currents. The developed Application Specific Integrated Circuit (ASIC) includes five identical MLT cells, bias current distribution and voltage follower/inverter (not used application specific integrated circuit in the system presented in this paper). Figure 2 shows top layout (1610 × 1610 μm) of the IC as well as detail of MLT cell layout (345 × 129 μm). Other details about the device have been presented in [47]. The operation of the device as a multiplier has the following form:

\[ i_z = -i_z = (v_{X1} - v_{X2}) \cdot (v_{Y1} - v_{Y2}) \cdot k, \]

where the transconductance constant \( k \) varies (confirmed difference of real experiment vs simulation expected from corner analysis) from 1.3 to 1.8 mA/V². The multiplier (see Fig. 2) can be easily rearranged (see Fig. 3) to operate as a transconductance amplifier having electronically adjustable transconductance \( g_m \) (by \( V_{set \_gm} \)– DC voltage).

### III. DOUBLE OUTPUT VOLTAGE PHASE DETECTOR

The phase detector represents a device generating a DC voltage based on the phase difference of two input signals. The basic concept that is shown in Fig. 4 employs multiplier from Fig. 2. Its structure is supplemented by loads (parallel \( R_l, C_l \) impedance to both complementary outputs). Differential output voltage has two-times larger output level than a single-output device in comparison with standard multipliers having a single voltage output.

The principle of the operation of phase detector is very simple. We have two signals of the same frequency \( \omega = 2 \cdot \pi \cdot f \) and two generally different amplitudes \( V_{m1} \) and \( V_{m2} \) available at the inputs of phase detector:

\[ v_{in1}(t) = V_{m1} \sin(\omega t), \]

\[ v_{in2}(t) = V_{m2} \sin(\omega t + \phi). \]
FIGURE 2. Description of the device (special CMOS multiplier): a) ideal principle, b) schematic symbol used in schemes, c) complete CMOS topology, d) top layout of developed ASIC and single MLT cell layout.
In comparison to $v_{in1}(t)$, signal $v_{in2}(t)$ is phase shifted by $\varphi$. The multiplication of both signals leads into expected result (expressed for single output $V_{out+}$):

$$i_{out+}(t) = V_{in1}V_{in2}\sin(\omega t) \cdot \sin(\omega t + \varphi) \cdot k.$$  
(4)

Equation (4) can be rearranged and modified by trigonometric rules, which gives:

$$i_{out+}(t) = \frac{V_{in1}V_{in2}}{2}(\cos(\varphi) - \cos(2\omega t - \varphi)) \cdot k.$$  
(5)

An appropriate load connected to the output terminal of the multiplier creates an output voltage. A simple resistor modifies previous equation into the following form:

$$v_{out+}(t) = \frac{V_{in1}V_{in2}}{2}(\cos(\varphi) - \cos(2\omega t - \varphi)) \cdot k \cdot R_L.$$  
(6)

However, there is still a time and frequency dependent component. This dependence can be removed when an RC load is used at the output terminal of multiplier. The resistor transforms the output current into the output voltage and the capacitor eliminates the time and frequency dependence (i.e. it provides integration of the fast changes).

The time constant of the RC must be significantly larger than changes in the input signal (condition: $\tau = R_LC_L \gg 1/\omega_{in}$). After that, the time and frequency dependent part can be removed from (6), as well as $C_L$ is not included in the resulting equation. As a result, equation (6) is reduced (in steady state) into the equation where both output polarities are available (multiplier has two complementary current output terminals):

$$V_{out_{\pm}, max}(\tau \ll t) \cong \pm \frac{V_{in1}V_{in2}}{2} \cdot k \cdot R_L \cdot \cos(\varphi[rad]).$$

It can be seen, that phase difference of waves directly determines output “DC” (or low-frequency) voltage. Form (7) expects steady state of the output response. However, time required for stabilization of the output voltage can be from high units of ms up to low tens of ms for components used in our cases. It depends on exponential increase across the load (valid between $V_{out_{+}} = 0$ V and $V_{out_{+}} = V_{out_{max}}$):

$$V_{out\pm}(\frac{1}{f_{in}} \ll t) \cong \pm \frac{V_{in1}V_{in2}}{2} \cdot k \cdot R_L \cdot \cos(\varphi[deg] \cdot \frac{\pi}{180}) \cdot \left[1 - \exp\left(-\frac{t}{R_L C_L}\right)\right].$$  
(8)

When both input amplitudes are identical $V_{m1} = V_{m2} = V_{m1,2}$, then the steady state of the output voltage of phase detector slightly changes (7):

$$V_{out_{\pm}, max}(\tau \ll t) \cong \pm \frac{V_{m1,2}^2}{2} \cdot k \cdot R_L \cdot \cos(\varphi[deg] \cdot \frac{\pi}{180}).$$  
(9)

### IV. APPLICATION EXAMPLE – FREQUENCY DEMODULATION

As discussed in introductory part of this paper, transposition of slowly changing signals to higher frequencies can be very useful for decreasing of large values of coupling capacitors requiring unreasonable big silicon area. The construction of frequency demodulator requires cooperation of two building blocks: phase detector and phase shifter. In circuit theory, the phase shifter is often referred to as all-pass filter.

The presented application uses an electronically adjustable type of the phase shifter that allows simple control of the frequency considered as carrier in case of demodulation. Figure 5 shows block scheme and also complete circuitry of frequency demodulator utilizing the double output voltage phase detector and phase shifter. Multiplication of the input signal and phase-shifted version of the same wave is supposed, i.e. product of $v_{in}(t)$ (i.e. $v_{in1}(t)$) having “carrier” $f_c$ frequency influenced by current frequency change $\Delta f$ and phase-shifted version of the same wave $v_{in2}(t)$. The phase shifter has the following transfer response:

$$K_{AP}(S) = \frac{V_{out2}(S)}{V_{in1}(S)} = -g_{m2}R_1 \left(\frac{sC_1 - g_{m1}}{sC_1 + g_{m1}g_{m2}R_1}\right)_{g_{m2} = 1/R_1} = \frac{sC_1 - g_{m1}}{sC_1 - g_{m1}}.$$  
(10)

where the zero and pole frequency ($f_{z/p} = g_{m1}/(2\pi \cdot C_1)$) can be adjusted simultaneously by parameter $g_{m1}$. Single parameter adjustability is advantageous feature of this solution.

Matching condition $g_{m2} = 1/R_1$ can be easily fulfilled and then it does not influence adjustability and the response. Equation (10) changes to:

$$K_{AP}(S) = 1 \cdot \exp\left[-2tan^{-1}\frac{(\omega C_1/\delta m_1)}{j}\right].$$  
(11)
Argument (phase) frequency response can be derived from (11) as:

$$\varphi_{AP} = -2\tan^{-1}\left(\frac{\omega C_1}{g_{m1}}\right).$$  \hspace{1cm} (12)

Formulas (9) and (12) allow us to find relation between value of phase shift at specific frequency ($f_{FM} = f_{vin1} = f_c \pm \Delta f$) and output voltage of the demodulator in form:

$$V_{out_{max}} \approx \left(\frac{V_{m1.2}}{2}\right) \cdot k \cdot R_L \cdot \cos\left[-2\tan^{-1}\left(\frac{2\pi(f_c \pm \Delta f)C_1}{g_{m1}}\right)\right].$$  \hspace{1cm} (13)

Supposing equality of $f_{Z/P} = f_c$ and definition of $f_{Z/P} = g_{m1}/(2\pi \cdot C_1)$, (13) can be modified as:

$$V_{out_{max}} \approx \left(\frac{V_{m1.2}}{2}\right) \cdot k \cdot R_L \cdot \cos\left[-2\tan^{-1}\left(\frac{f_c \pm \Delta f}{f_c}\right)\right].$$  \hspace{1cm} (14)

The operation of the demodulator can be explained as follows. When the input frequency $f_c \pm \Delta f$ ($\Delta f \to 0$ Hz) and the zero/pole frequency $f_{Z/P}$ (frequency where phase shift of the shifter reaches $90^\circ$) of the phase shifter are the same, the phase detector produces steady state voltage $V_{out_{\pm}}$ near to 0 V. When the input frequency $f_c \pm \Delta f$ varies below the zero/pole frequency ($f_c - \Delta f < f_{Z/P}$) set by the phase shifter (fixed tuning for carrier frequency), then phase shift of $v_{in2}$ changes for incoming frequency (negative value of
the output \( V_{\text{out}+} \), positive value of the output \( V_{\text{out}–} \) and vice versa for input frequency above zero/pole frequency of the phase shifter \((f_C - \Delta f > f_{Z/P})\).

V. EXPERIMENTAL VERIFICATION

Functionality of the proposed concept was verified experimentally. For the measurement, we employed Keysight DSOX-3024T oscilloscope and development breadboard with a fabricated IC device (including multipliers) and external passive elements. The obtained results from real laboratory experiments are compared with Cadence Virtuoso (0.18 \( \mu \text{m} \) TSMC process design kit) simulations as well as with theory. Supply voltage \( \pm 0.9 \) V (1.8 V) has been applied. The quiescent power consumption reaches 17 mW. The phase detector (multiplier) has power consumption of 5.7 mW as well as each MLT cell used in the design (5.68 mW for MLT\( _3 \), 5.66 mW for MLT\( _1 \) and 5.65 mW for MLT\( _2 \)).

The design of the MLT respects universal application purpose (up to several MHz). Therefore, power consumption is not optimized for extremely low-power (microwatts) applications limited to several units-tens of kHz of bandwidth. As already noted in the introductory part and [47], this device supposes operation with bandwidth wider than 40 MHz (between 40 and almost 90 MHz) to the 10-15 pF capacitive load with linear input dynamics between \( \pm 200 \) mV.

The obtained levels of power dissipations (units of mW per cell) are typical for presented features and performances of the device in particular CMOS process. Future applications of the MLT expect operations in MHz bands but high tens of kHz (around 50 kHz) are sufficient for the system presented in this paper. Therefore, the design of the system (the main purpose in frequency transpositions of slow signals in order to decrease the values of coupling capacitors) can be also further optimized from the power dissipation aspect.
FIGURE 9. Test of the FM demodulator on phase shift variation between \( v_{\text{in}1}(t) \) and \( v_{\text{in}2}(t) \) by the phase shifter \((f_Z/P)\) in system at constant carrier frequency \( (f_C = 50 \text{ kHz}) \): a) impact of current adjustment of the filter at phase shift \( \phi_{\text{AP}} \) at 50 kHz, b) dependence of generated DC output voltage of the phase detector on variable phase shift generated by phase shifter for \( f_C = 50 \text{ kHz} \).

A. REAL BEHAVIOR OF THE PHASE DETECTOR

The comparison of ideal, simulated and measured operation of the double output voltage phase detector is shown in Fig. 6. The difference of nominal and tested transconductance constants (1.8 vs 1.3 mA/V²) belongs to the expected and acceptable variation of ±30% from corner-temperature analysis. The phase shift (generated by independent signal source) varies between 0° and 180° (input amplitudes \( V_{\text{m1}} = V_{\text{m2}} = V_{\text{m}} = 200 \text{ mV} \) at \( f_{\text{in}} = 50 \text{ kHz} \), \( R_L = 10 \text{ k\$} \) and \( C_L = 220 \text{ nF} \)) that results into theoretical (valid for \( k = 1.8 \text{ mA/V}^2 \)) DC component value from −360 mV up to 360 mV. Simulation provides range from −340 mV up to 320 mV. The calculated results, using \( k = 1.3 \text{ mA/V}^2 \) indicate voltage range from −260 mV up to 260 mV whereas experimental test yields range between −275 mV and 240 mV. It corresponds to good accuracy of equation (9) derived for DC output voltage dependence on phase shift of input voltages. The time domain examples of \( V_{\text{out}+} \) for phase shifts 22°, 91° and 135° are given in Fig. 7. Note that further tests in this paper suppose the same setting of \( g_{\text{m}} \)'s in simulations and experimental measurements (slightly different \( V_{\text{set},g_{\text{m}}} \) is necessary due to deviation of fabricated sample and nominal simulation run).

FIGURE 10. Response of the demodulator on input (carrier) frequency \( f_C \pm \Delta f \) variation: a) dependence of actual phase shift between \( v_{\text{in}1}(t) \) and \( v_{\text{in}2}(t) \) on input frequency \((f_Z/P = 50 \text{ kHz})\), b) dependence of output voltages of the demodulator in input frequency (i.e. frequency deviation), c) dependence of differential output voltage on input frequency.

B. PHASE SHIFTER

The frequency responses (tuning example) of the phase shifter in one decade are plotted in Fig. 8. The phase shifter (all-pass filter) uses the following components: \( C_1 = 1 \text{ nF}, R_1 = 2 \text{ k\$} \) and \( g_{\text{m}2} = 500 \text{ \mu}\$ \) \((V_{\text{set},g_{\text{m}2}} = 0.38 \text{ V})\). Note that real (valid in experiments) \( V_{\text{set},g_{\text{m}}} \) values are always
The transconductance $g_{m1}$ was adjusted from 50 $\mu$S ($V_{\text{set}_{g_{m1}}} = 0.038$ V) up to 500 $\mu$S ($V_{\text{set}_{g_{m1}}} = 0.38$ V). Such variation of $g_{m}$ values represents typical available operational range of the designed multiplier (OTA) [47]. It yields $f_{Z/P}$ values between 9 kHz and 79 kHz that is near to theory: 7.95 kHz → 79.5 kHz. This setting was intentionally selected due to $f_C = 50$ kHz.

**C. FREQUENCY DEMODULATOR**

Our specification on frequency demodulator supposes carrier frequency of 50 kHz. Therefore, the zero/pole frequency of the phase shifter ($f_{Z/P}$) must be set on the same value. It results into $g_{m1} = 0.314$ $\mu$S ($V_{\text{set}_{g_{m1}}} = 0.24$ V) whereas the rest of parameters remains as stated above. The analysis of the FM demodulator (presented in Fig. 5) covers the complete topology including the proposed and designed phase shifter.

This arrangement provides response for phase shift variation approximately between $\psi_{AP} = 37^\circ$ and $160^\circ$ at $f_C = 50$ kHz as it is shown in Fig. 9. Frequency $f_{Z/P}$ was tuned in order to emulate the change of the phase difference between input signals. Such a test of the FM demodulator covers intentional phase shift variation between $v_{\text{in1}}(t)$ and $v_{\text{in2}}(t)$ by the phase shifter ($f_{Z/P}$) in the system at constant carrier frequency 50 kHz. Figure 9 shows the impact of
Application of the phase detector and phase shifter expects variation of frequency with some frequency deviation $\pm \Delta f$ around $f_C$ (or considered also as variation of input/carrier frequency $f_C$ itself in some range, i.e. narrow-band or wide-band modulation) [9]. The concept was tested with $f_C$ variable from 10 kHz up to 100 kHz (while $f_{Z/P}$ of the phase shifter still set to 50 kHz), i.e. $f_{FM} = f_{in} = f_C \pm \Delta f$, where $\Delta f = 5$ kHz $\rightarrow$ 40 kHz. The frequency deviation $\Delta f$ is determined by the maximum peak-to-peak value of modulation signal [9], [62]. As it is shown in Fig. 10, this variability of carrier frequency (input frequency of the demodulator) causes phase difference between $v_{in1}(t)$ and $v_{in2}(t)$.

Figure 11 captures the block diagram of test setup proposed to verify the experiment in the time domain (with real frequency modulated signal). All experimental tests were performed by Keysight DSOX-3024T oscilloscope allowing time domain and spectral analysis as well as frequency response analysis (phase shifter). The generator of the oscilloscope also generated sine-wave testing patterns (low-frequency modulation signal 500 Hz) for internal modulator and output modulated waveform. Unfortunately, oscilloscope itself is not showing modulation (low-frequency) signal. Therefore, external generator SDG6022X has been used for tests where modulation signal shape is required to be visible for comparison with reproduced one (demodulated waveform). In this case, switches (shown in Fig. 11) are commutated as indicated by arrows. Then, the internal generator of the oscilloscope produces a complex modulation signal (low-frequency 10 Hz of basic tone in this case) that is also monitored at channel 1 (CH1) and SDG6022X is responsible for modulation procedure and produces carrier wave (monitored at CH2). The demodulated waveform is observed at CH3 and CH4 (single ended) and mathematical function creates their difference.

The experiment was set as follows: carrier signal $V_C = 200$ mV, $f_C = 50$ kHz, $\Delta f = 30$ kHz (wideband modulation) and modulation signal $f_{FM} = 500$ Hz (then, $f_{in} = f_C \pm \Delta f = 50$ kHz $\pm$ 30 kHz). Modification of $C_L$ (in this case 100 nF) offers possibility to influence the quality of demodulation. Correct setting of time constant $\tau = R_L C_L$ allows to follow the modulation wave precisely without leakage of carrier wave but too fast changes of modulation signal $v_M(t)$ (when $\tau > 1/f_M$) can be also attenuated and not restored correctly from $v_{FM}(t)$. The measured results are plotted in Fig. 12. The example of time domain waveforms illustrates the effects of frequency modulation in the modulated carrier wave and...
also results of demodulation. The spectral analysis of the output wave is given for $V_{\text{out}+}$ as well as differential value $V_{\text{out\_diff}}$. Figure 13 shows situation for frequency deviation for $\Delta f = 2$ kHz. The rest of parameters remain unchanged. In this case, we can see that the demodulated signal has lower level than for large $\Delta f$ because narrower frequency deviation generates lower demodulated amplitude as expected. Results sufficiently confirm correct operationability of the demodulator for low-frequency modulation signals $V_M(t)$.

The occupied bandwidth of the FM modulated signal is defined by Carson relation \[9\] as $CBR = 2 \cdot (\Delta f + f_M) = 2(2 \text{ kHz} + 500 \text{ Hz}) = 5 \text{ kHz} (50 \text{ kHz} \pm 2.5 \text{ kHz})$. The frequency $f_0 = 47$ kHz ($\approx 50$ kHz $\pm 2.5$ kHz) of limited bandwidth (see Fig. 13) and resistance levels ($R_{\text{node}}$) about 50$\rightarrow$500 k$\Omega$ (high-impedance nodes) means that the coupling capacity for low-cut off frequency (-3 dB) of high-pass AC coupling ($f_d = 1/(2 \cdot \pi \cdot C_V \cdot R_{\text{node}})$) reaches approximately 70$\rightarrow$7 pF. These values are somehow feasible (with some limitations) on chip (parallel combinations of maximal metal-insulator-metal capacitors in the worst case for example). The value $f_M = 500$ Hz means $C_V \approx 0.7 \text{ nF}$. Lower frequencies (tens of Hz and lower) require significantly larger values of $C_V$ (hundreds of nF, µF).

Example of demodulation of more complex and slow signals than sine wave (electrocardiogram and sinc available in generator functions were selected) is given in Fig. 14 for $V_C = 200$ mV, $f_C = 50$ kHz, $\Delta f = 20$ kHz, and parameters of modulation signal $V_M = 2.5$ V, $f_M = 10$ Hz. The generator Siglent SDG6022X, allowing external input of modulation signal, was used for these tests. We can see that the shapes of the input waveforms are sufficiently restored at the output of the demodulator (differential output used $V_{\text{out\_diff}} = V_{\text{out}+} - V_{\text{out}-}$). The output signal of the demodulator is attenuated about 30 dB in comparison to the modulation signal. However, the sensitivity can be improved by modification of values of load resistances of the double output voltage phase detector and also by selection of the all-pass filter (phase shifter) of 2nd order having variable quality factor (slope of argument characteristic can be modified in order to obtain increased sensitivity).

Results shown in Fig. 14 require coupling capacitors for the lowest frequency 10 Hz approximately between 320 and 32 nF (nodal resistance 50$\rightarrow$500 k$\Omega$). So, we need value equal to 320 nF in the worst case. When our approach is used, value up to 70 pF (worst case) is sufficient on IC when the presented technique (transposition of baseband, basic tone 10 Hz, signal to the band around 50 kHz) is used. Design of capacities in tens of pF is available in many processes. However, the carrier frequency can be even readjusted easily to higher values and then lower values of coupling capacitors are required. In general, the proposed technique and limits of our specific system (as it is now presented) offer reduction of coupling capacities from hundreds of nF to tens of pF. The effect of capacity decrease approximately depends on distance of baseband tone and carrier frequency. The testing coupling capacity $C_V = 68 \text{ pF}$ together with $R_{\text{node}} = 100 \text{ k}\Omega$

\[f_C > 25 \text{ kHz}\] is sufficient) is placed in front of demodulator as shown in Fig. 11. The value of $>150$ nF (not feasible on IC) would be required without implementation of the proposed technique for baseband tone 10 Hz at this place.

The information about dynamic power consumption of the demodulator is graphically shown in Fig. 15 for all three
MLT cells forming the proposed demodulator measured in test setup (see Fig. 11).

VI. CONCLUSION

This work proved that simple building blocks can be useful for applications in signal processing and communication subsystems. Moreover, whole designed system can be integrated on one chip thanks to fabricated multipliers offering simple solution of a double output voltage phase detector (nonlinear operation) and phase shifter (linear system) for utilization in frequency demodulator as a final example of application of these parts.

The proposed phase detector is able to generate a DC (or slowly varying - if the time constant is modified for demodulation purposes) output voltage in a range ±250 mV (500 mV in differential view) approximately, when the input phase difference \( \phi \) (between \( \varphi_1(t) \) and \( \varphi_2(t) \)) varies between 0° and 180° (tested at an input frequency of 50 kHz). Adjustability range of the phase shifter \((\varphi_{AP})\) itself (by transconductance \(g_{m1}\)) offers also similarly wide change of the output voltage of the detector at a single frequency. Nevertheless, the available phase shift range generated by the phase shifter itself is smaller (from 37° up to 160°) when \(g_{m1}\) is varied from 70 μS up to 870 μS. Operation of the detector with phase shifter produces similar output voltage range (±250 mV) for variation of input frequency of the demodulator tested between 10 kHz and 100 kHz. Cadence simulations show similar results as the outputs of experimental measurements, only a slightly different transconductance constant (simulation vs experiment) must be taken into account.

Verification of the application by frequency-modulated waveform confirms the expected behavior for wideband and narrowband character of frequency deviation using low-frequency modulation wave frequencies in hundreds of Hz (500 Hz and 10 Hz tested in experiments). All these features are available without more complex (topologically) PLL systems standardly used for demodulation [9]. Current design specifications of our system for purpose of coupling capacity (value) offer reduction of values from hundreds of nF down to tens of pF.

Usefulness of these systems can be found in processing low-frequency signals (vibrations) [4]–[6] or in modern methods of measurements [68]. In cooperation with modulation system, the proposed concept may help with issues of high coupling capacity values in specific cases.

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