We introduce the Coarse-Grain Out-of-Order (CG-OoO) general purpose processor designed to achieve close to In-Order processor energy while maintaining Out-of-Order (OoO) performance. CG-OoO is an energy-performance proportional general purpose architecture that scales according to the program load. Block-level code processing is at the heart of this architecture; CG-OoO speculates, fetches, schedules, and commits code at block-level granularity. It eliminates unnecessary accesses to energy consuming tables, and turns large tables into smaller and distributed tables that are cheaper to access. CG-OoO leverages compiler-level code optimizations to deliver efficient static code, and exploits dynamic instruction-level parallelism and block-level parallelism. CG-OoO introduces Skipahead issue, a complexity effective, limited out-of-order instruction scheduling model. Through the energy efficiency techniques applied to the compiler and processor pipeline stages, CG-OoO closes 64% of the average energy gap between the In-Order and Out-of-Order baseline processors at the performance of the OoO baseline. This makes CG-OoO 1.9× more efficient than the OoO on the energy-delay product inverse metric.

1. INTRODUCTION

This paper revisits the Out-of-Order (OoO) execution model and devises an alternative model that achieves the performance of the OoO at over 50% lower energy cost. Czechowski et al. 2 discusses the energy efficiency techniques used in the recent generations of the Intel CPU architectures (e.g. Core i7, Haswell) including Micro-op cache, Loop cache, and Single Instruction Multiple Data (SIMD) instruction set architecture (ISA). This paper questions the inherent energy efficiency attributes of the OoO execution model and provides a solution that is over 50% more energy efficient than the baseline OoO. The energy efficiency techniques discussed in 2 can also be applied to the CG-OoO model to make it even more energy efficient.

Despite the significant achievements in improving energy and performance properties of the OoO processor in the recent years 2, studies show the energy and performance attributes of the OoO execution model remain superlinearly proportional 3,4. Studies indicate control speculation and dynamic scheduling technique amount to 88% and 10% of the OoO superior performance compared to the In-Order (InO) processor 5. Scheduling and speculation in OoO is performed at instruction granularity regardless of the instruction type even though they are mainly effective during unpredictable dynamic events (e.g. unpredictable cache misses) 4. Furthermore, our studies show speculation and dynamic scheduling amount to 67% and 51% of the OoO excess energy compared to the InO processor. These observations suggest any general purpose processor architecture that aims to maintain the superior performance of OoO while closing the energy efficiency gap between InO and OoO ought to implement architectural solutions in which low energy program speculation and dynamic scheduling are central.

Our study provide four high level observations. First, OoO excess energy is well distributed across all pipeline stages. Thus, an energy efficient architecture should reduce energy of each stage. Second, OoO execution model imposes tight functional dependencies between stages requiring a solution to enable energy efficiency across all stages. Third, as mentioned by others, complexity effective micro-architectures such as ILDP 6 and Palachara, et al. 7 enable simpler hardware, such as local and global register files that improve energy efficiency. A block-level execution model, like CG-OoO, enables energy efficiency by simplifying complex, energy consuming modules throughout the pipeline stages. Fourth, since dynamic scheduling and speculation techniques mainly benefit unpredictable dynamic events, they should be applied to instructions selectively. Unpredictable events are hard to detect and design for; however, we show a hierarchy of scheduling techniques can adjust the processing energy according to the program runtime state.

CG-OoO contributes a hierarchy of scheduling

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1 Not to be confused with energy-proportional designs 1. Energy-performance proportional scaling refers to linear change in energy as the processor configuration allows higher peak performance (Figure 26).
techniques centered around clustering instructions; static instruction scheduling organizes instructions at basic-block level granularity to reduce stalls. The CG-OoO dynamic block scheduler dispatches multiple code blocks concurrently. Blocks issues instructions in-order when possible. In case of an unpredictable stall, each block allows limited out-of-order instruction issue using a complexity effective structure named Skipahead. Skipahead accomplishes this by performing dynamic dependency checking between a very small collection of instructions at the head of each code block. Section 4.4.1 discusses the Skipahead micro-architecture.

CG-OoO contributes a complexity effective block-level control speculation model that saves speculation energy throughout the entire pipeline by allowing block-level control speculation, fetch, register renaming bypass, dispatch, and commit. Several front-end architectures have shown block-level speculation can be done with high accuracy and low energy cost [8, 9, 10]. CG-OoO uses a distributed register file hierarchy to allow static allocation of block-level, short-living registers, and dynamic allocation of long-living registers.

The rest of this paper is organized as follows. Section 2 presents the related work, Section 3 describes the CG-OoO execution model, Section 4 discusses the processor architecture, Section 5 presents the evaluation methodology, Section 6 provides the evaluation results, and Section 7 concludes the paper.

2. OVERVIEW & RELATED WORK

CG-OoO aims to design an energy efficient, high-performance, single-threaded, processor through targeting a design point where the complexity is nearly as simple as an in-order and instruction-level parallelism (ILP) is paramount. Table 1 compares several high-level design features of the CG-OoO architecture compared to the previous literature.

| Design Feature | CG-OoO | Braid | WiDGET | TRIPS [12, 15] | Multiscalar | CE | TP | MorphCore | BOLT | iCFP | ILDP | WaveScalar |
|----------------|--------|-------|--------|----------------|-------------|----|----|-----------|------|------|------|-------------|
| Distributed instruction window | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Energy Modeling | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Complexity Effective Design | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Static & Dynamic Scheduling | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Energy Modeling | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Block-level Out-of-Order Scheduling | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Register File Hierarchy | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Table 1: Eight high-level design features of the CG-OoO architecture compared to the previous literature.

Multiscalar [14] evaluates a multi-processing unit capable of steering coarse grain code segments, often larger than a basic-block, to its processing units. It replicates register context for each computation unit, increasing the data communication across its register files. TRIPS and EDGE [12, 20] are high-performance, grid-processing architectures that uses static instruction scheduling in space and dynamic scheduling in time. It uses Hyperblocks [21] to map instructions to the grid of processors. Hyperblocks use branch prediction to group basic-blocks that are connected together through weakly biased branches. To construct Hyperblocks, the TRIPS compiler uses program profiling. While effective for improving instruction parallelism, Hyperblocks lead to energy inefficient mis-speculation recovery events. Palachara, et al. [7] supports a distributed instruction window model that simplifies the wake-up logic, issue window, and the forwarding logic. In this paper, instruction scheduling and steering is done at instruction granularity. Trace Processors [15] is an instruction flow design based on dynamic code trace processing. The register file hierarchy in this work consists of several local register files and a global register file. ILDP [6] is
a distributed processing architecture that consists of a hierarchical register file built for communicating short-lived registers locally and long-lived registers globally. ILDP uses profiling and in-order scheduling from each processing unit. In contrast to all of these proposals, the CG-OoO compiler does not use program profiling (col. 5), and avoids static control prediction by clustering instructions at basic-block granularity. CG-OoO uses local and segmented global registers to reduce data movement and SRAM storage energy.

iCFP [13] addresses the head-of-queue blocking problem in the InO processor by building an execution model that, on every cache miss, checkpoints the program context, steers miss-dependent instructions to a side buffer enabling miss-independent instructions to make forward progress. CFP [22] addresses the same problem in an OoO processor. Similarly, BOLT [17], Flea Flicker [23], and Runahead Execution [24] are high ILP, high MLP latency-tolerant architecture designs for energy efficient out-of-order execution. All these architectures follow the runahead execution model. BOLT uses a slice buffer that utilizes minimal hardware resources. CG-OoO solves the head-of-queue scheduling problem through a hierarchy of energy efficient solutions including the Skipahead (Section 3.4.1) scheduler (col. 8).

WaveScalar [19] and SEED [25] are out-of-order data-flow architectures. The former focuses on solving the problem of long wire delays by bringing computation close to data. The latter is a complexity effective design that groups data-dependent instructions dynamically and manages control-flow using switch instructions. MorphCore [16] is an InO, OoO hybrid architecture designed to enable single-threaded energy efficiency. It utilizes either core depending on the program state and resource requirements. It uses dynamic instruction scheduling to execute and commit instructions. In contrast to the above, CG-OoO is a single-threaded, block-level, energy efficient design that addresses the long wire delays problem through clustering execution units, register files and instruction queues close to one another. CG-OoO is end-to-end coarse-grain, and code blocks do not need additional instructions to manage control flow.

3. CG-OOO ARCHITECTURE

The goal of the CG-OoO processor is to reach near the energy of the InO while maintaining the performance level of OoO. This section introduces the CG-OoO as a block-level execution model that leverages a hierarchy of solutions (software and hardware) to save energy. Section 3.3 provides an execution flow example.

CG-OoO consists of multiple instruction queues, called Block Windows (BW), each holding a dynamic basic-block and issuing instructions concurrently. BW’s share execution units (EU) to issue instructions (Figure 1). Several BW’s and EU’s are grouped to form execution clusters. CG-OoO uses compiler support to group and statically schedule instructions.

3.1 Hierarchical Design

3.1.1 Hierarchical Architecture

CG-OoO groups instructions into code-blocks that are fetched, dispatched, and committed together. At runtime, each dynamic block is processed from a dedicated BW. To manage data communication energy, BW and EU’s are grouped together to form clusters. Figure 1 shows CG-OoO clusters highlighted; thin wires, in blue, enable data forwarding between EU’s. Microarchitecture clustering provides proportional energy-performance scaling based on program load demands. Scalable architectures are previously studied by [5][20][24]. CG-OoO extends this concept to energy efficient, block-level execution.

3.1.2 Hierarchical Instruction Scheduling

We use static instruction list scheduling on each basic-block to improve performance and energy (a) by optimizing the schedule of predictable instructions along the critical path, (b) by improving MLP via hoisting memory operations to the top of basic-blocks, and (c) by minimizing wasted computation due to memory mis-speculation (Section 3.2.2). The compiler assumes L1-cache latency for memory operations.

BW’s in each cluster schedule instructions concurrently to hide each other’s head-of-queue stalls. We call this scheduling model block level parallelism (BLP). Furthermore, each BW supports a complexity effective, limited out-of-order instruction issue model (Section 3.1.1) to address unpredictable cases where coarse-grain scheduling cannot provide enough MLP. These techniques combined help save energy by limiting the processor scheduling granularity to the program runtime needs (Section 3.2.2 shows an example).

3.1.3 Hierarchical Register Files

The CG-OoO register file hierarchy consists of: Global Register File (GRF), and Local Register File (LRF). The GRF provides a small set of architecturally visible registers that are dynamically managed while LRF is statically managed, small, and energy efficient. The GRF is used for data communication across BW’s while LRF is used for data communication within each BW. Each BW has its dedicated LRF. As shown in Section 3.2.2, 30% of data communication (register→register and register+memory) is done through LRF’s. To further save energy, the GRF
3.2 Block-level Speculation

CG-OoO supports energy efficient, block-level speculation by using only one BPU lookup per code block. The compiler generates an instruction named head to specify the start of a new code block, (b) access the BPU to predict the next code block, (c) trigger the Block Allocation unit to allocate a new BW and steer upcoming instructions to it (Figure 1). head is often ahead of its branch by at least one cycle making the probability of front-end stall due to delayed branch prediction low.

Figure 2 shows the head instruction fields: (a) opcode, (b) control instruction presence bit, (c) block size, (d) control instruction least significant address bits. The example code in Figure 3 shows head has HasCtrl=1'b1 indicating a control operation ends the basic-block. If HasCtrl=1'b0, BPU lookup is disabled to save energy. In Figure 3, local and global operands are identified by r and g prefixes respectively.

3.2.1 Squash Model

CG-OoO supports block-level speculative control and memory squash. Upon control mis-prediction, the front-end stalls fetching new instructions, all code blocks younger than the mis-specified control operation are flushed, and the remaining code blocks are retired. The data produced by wrong-path blocks are automatically discarded as such blocks never retire. Once the BROB is empty, the processor state is non-speculative, and it can resume normal execution.

3.3 CG-OoO Program Execution Flow

This section illustrates CG-OoO architecture with a code example. To better understand the execution flow, Figure 4 shows the CG-OoO processor pipeline. The highlighted stages differ the traditional OoO. Control speculation, dispatch, commit are at block granularity, and rename is only used for global operands. Section 4 discusses how each stage saves energy.

Figure 5 illustrates a two-wide superscalar CG-OoO. The instruction scheduler issues one instruction per BW per cycle to the two EU’s. The code in BW’s are two consecutive iterations of the abovementioned do-while loop. Figure 6 shows the cycle-by-cycle flow of instructions through the CG-OoO pipeline. Instructions in iterations 1 and 2 are green and red respectively. It also shows the contents of BW0, BW1, and the Block Re-Order Buffer (BROB). Here, lw is a 4-cycle operation, and all others 1-cycle.

In cycle 1, {head.1, add.1} instructions are fetched from the instruction cache. In cycle 2, the immediate field of head.1 is forwarded to the BPU. In cycle 3, head.1 speculates the next code block before the control operation, bne.1, is fetched; furthermore, the Block Allocator assigns BW0 to the instructions following head.1, and BROB reserves an entry for head.1 to stores the runtime status of its instructions. In cycle 4, BW0 receives its first instruction. In cycle 5, add.1 is issued while more instructions join BW0. In cycle 10, the last instruction of iteration 1 leaves BW0. In cycles 11, BW0 is available to hold new code blocks. In cycle 13, head.1 is retired as all its instructions complete execution; at this point, all data generated by the block operations will be marked non-speculative.

4. CG-OoO MICRO-ARCHITECTURE

This sections presents the CG-OoO pipeline micro-architecture details and highlights their energy saving attributes. These stages save energy by utilizing several complexity effective techniques through (a) the use of small tables, (b) reduced number of table accesses, and (c) hardware-software hybrid instruction scheduling.

4.1 Branch Prediction

Figure 7 shows the micro-architectural details of the branch prediction stage in the CG-OoO processor; it consists of the Branch Predictor (BP) 29, Branch Target Buffer (BTB), Return Address Stack (RAS), and Next Block-PC. Equation 1 shows the Next Block-PC computation relationship.

\[ PC_{next} = PC_{head} + \text{fall-through-block-offset} \] (1)

The fall-through-block-offset is the immediate field of the head instruction shown in Figure 2. In the CG-OoO model, only head PC’s access the BPU. Upon lookup, a head PC is used to predict the next head PC. Speculated PC’s are pushed into a FIFO queue, named Block PC Buffer, dedicated to communicate block addresses to Fetch (Figure 6).
Once completed, each control operation verifies the next-block prediction correctness and updates the corresponding BPU entry(ies) accordingly. Since the BPU is indexed by head PC's, control operations access their corresponding BPU entry(ies) by computing their head PC using Equation 2.

\[ PC_{\text{head}} = PC_{\text{control-op}} - \text{code-block-offest} \quad (2) \]

4.2 Fetch Stage

Figure 7a illustrates a control flow graph with five basic-blocks. Each block is marked with its head identifier, \( h \), at the top, and its control operation identifier (if any), \( c \), at the bottom. Figure 7b illustrates the mapping of these basic-blocks to the instruction cache where each box represents an instruction and each set of adjacent boxes with the same color represent a fetch group. Entries marked I represent non-control, non-head operations in each basic-block in Figure 7b. As shown in Figure 7b, an arbitrary number of head's may exist in a fetch group. Fetch and BPU handle all cases.

The Block PC Buffer holds either a next-PC address or a 64-bit address of the next code block to fetch from the cache, and the latter is a hint that next-PC is unknown. An unknown PC happens when a head operation, \( hh \), is predicted not-taken and \( hh \) itself is not yet fetched. Recall, the predictor needs to have the fall-through block offset of \( hh \) to predict the next block. In such cases, Fetch assumes the fall-through block is adjacent to the \( hh \) block in memory; so, it continues fetching the next block while the fall-through block address for \( hh \) is computed.

This section assumes no fetch-alignment [32].

4.3 Decode & Register Rename Stages

The Decode micro-architecture follows that of the conventional OoO except for its additional functionality to identify global and local register operands by appending a 1-bit flag, named Register Rename Flag (RRF), next to each register identifier. If an instruction holds a global operand, it accesses the register rename (RR) tables for its physical register identifier; otherwise, it would skip RR lookup (Figure 6). Skipping the register rename stage reduces the renaming lookup energy by 30% on average. This saving is realized due to our block-level execution model. Our RR evaluations use the Merged Rename and Architectural Register File model discussed in [33, 34, 35].

4.4 Issue Stage

Before discussing the CG-OoO issue model, let us visit the Block Window micro-architectural shown in Figure 5. It consists of an Instruction Queue (IQ), a Head Buffer (HB), a dedicated LRF, a GRF segment, and a number of EU's. IQ is a FIFO that holds code block instructions. HB is a small buffer that holds instructions waiting to be issued by the Instruction Scheduler in a content accessible memory (CAM) array. HB pulls instructions from the IQ and waits for their operands to become ready for issue. The CG-OoO issue model allows register file accesses only to operations in the HB thereby (a) avoiding the OoO post-issue register file read cycle, and (b) saving the pre-issue large data storage overhead [34] by only storing operands in HB's. Because the number of operations in all HB's is a fraction of all in-flight instructions, this model is as fast as the OoO pre-issue model, and more energy efficient than both models.

4.4.1 Skipahead Instruction Scheduler

The Skipahead model allows limited out-of-order issue of operations. The term limited means out-of-order
The Skipahead model improves the CG-OoO performance by 41% (Section 6.1) while enabling a selection and wakeup model no more energy hungry than an in-order issue model. The wakeup unit presents three sources of energy efficiency. (a) In each BW, the wakeup unit uses a small HB storage space to hold operand data. In contrast to OoO, operations in the Instruction Queue are not included in the wakeup process. (b) The wakeup unit searches small CAM tables for source operands. For instance, in a CG-OoO processor with 8 BW’s, each with 3 HB entries, the wakeup unit accesses 48 CAM source operand entries. The OoO baseline assumes 128, 24, 37 in-flight operations in Instruction Window to search for ready operands. (c) Local write operands wakeup source operands associated with their own BW only.

4.5 Memory Stage

The CG-OoO Memory stage consists of a load-store-unit (LSU) that operates at instruction granularity. A squash is triggered when a sw conflicts with a younger lw at which point the block holding the lw is flushed; this means useful instructions older than lw are also squashed. For instance, in Figure 9 if operation 2 were to trigger a memory mis-speculation event, the entire block, including operation 1, would be squashed. Flushing useful operations is called wasted squash which the compiler reduces by hoisting memory operations toward the top of basic-blocks. Efficient memory speculation models such as NoSQ [38] can further improve processor energy efficiency by replacing associative LSU lookups with indexed lookups. Evaluating the energy impact of such designs is outside of the scope of this work.

4.6 Write Back & Commit Stage

Figure 10 shows the contents of a BROB entry; it holds the block sequence number, block size, and block instruction issue is restricted to only the HB instructions, a subset of all code block instructions. When a HB instruction, Ins, becomes ready prior to HB instruction(s) ahead of it, if Ins does not create a true or false dependency with older instructions, it may be issued out-of-order. Figure 8 shows the complexity effective XOR logic used for dependency checking.

For example, assuming a three-entry HB, in Figure 9 instructions are issued as \{1, 3\} followed by \{2, 4\}. Before issuing 3, its operands are dependency checked against those of 2.

The Skipahead model improves the CG-OoO performance by 41% (Section 6.1) while enabling a selection and wakeup model no more energy hungry than an in-order issue model. The wakeup unit presents three sources of energy efficiency. (a) In each BW, the wakeup unit uses a small HB storage space to hold operand data. In contrast to OoO, operations in the Instruction Queue are not included in the wakeup process. (b) The wakeup unit searches small CAM tables for source operands. For instance, in a CG-OoO processor with 8 BW’s, each with 3 HB entries, the wakeup unit accesses 48 CAM source operand entries. The OoO baseline assumes 128, 24, 37 in-flight operations in Instruction Window to search for ready operands. (c) Local write operands wakeup source operands associated with their own BW only.

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4.6 Write Back & Commit Stage

Figure 10 shows the contents of a BROB entry; it holds the block sequence number, block size, and block

global write (GW) register operand identifiers. BlkSize is initialized by the corresponding head operation. The GW fields are updated by instructions with global write registers as they are steered from the Register Rename stage to their BW. The compiler controls the number of global write operands per code block.

4.6.1 Write-Back Stage

Once an instruction completes, it writes its results into either a designated register file entry (global or local) or into the store queue. In Figure 10 BlkSize is decremented upon each instruction complete; once its value is zero, the corresponding block is completed.

4.6.2 Commit Stage

A block is committed when it is completed and is at the head of the BROB. During commit, all global registers modified by the block are marked Architectural using the GW fields in BROB. Upon commit, sw operations in the committing code block retire; in doing so, the Store-Queue “commit” pointer moves to the youngest sw belonging to the committing block. This sw is found via searching for the youngest store operation whose Block SN matches that of the committing block. Note, our LSU holds a Block SN column.

Checkpoint-based processors [39, 40, 41] propose a general concept applicable to many architectures (e.g. iCFP [18]). While outside of the scope of this work, coarse-grain checkpoint-based processing is promising for extending the energy efficiency of CG-OoO.

4.7 Squash Handling

CG-OoO handles squash events through the following steps: (a) the MPU history queue and Block Processor flush the content corresponding to wrong-path blocks. The code block PC resets to the start of the right path; in case of a control mis-speculation, the right path is the opposite side of the control operation, and in case of a memory mis-speculation, it is the start of the same code block. (b) All BW’s holding code blocks younger than the mis-speculated operation flush their IQ, Head Buffer, and mark LRF registers invalid. (c) LSU flushes operations corresponding to the code block younger than the mis-speculated operation by comparing the mis-speculated Block SN against that of memory operations. (d) BROB flushes code block entries younger than the mis-speculated operation. The remaining blocks complete execution and commit.

5. METHODOLOGY

The evaluation setup consists of an in-house compiler, simulator and energy model. The compiler performs Lo-
**Table 2: System parameters for each individual core**

| Parameter                        | CG-OoO Processor | OoO Processor | InO Processor |
|----------------------------------|------------------|---------------|---------------|
| Pipeline Depth                   | 13 cycles        | 12 cycles     | 13 cycles     |
| Instruction Queue                | 128 entries, RAM/CAM | 256 entries (64bit) | 64 entries, CAM |
| Register File                    | 1-8 wide         | 1-8 wide      | 1-8 wide      |
| Re-Order Buffer                  | 160 entries      |               |               |
| Instruction Queue / BW           | 10 entries, FIFO | 2-5 entries, RAM/CAM | 16 entries    |
| Head Buffer / BW                 | 1-8 wide         | 1-8 wide      |               |
| Execution Unit / BW              | 1-8 wide         |               |               |
| Number of BW's                   | 3-18             | 3-18          | 3-18          |
| Instruction Queue / BW           | 10 entries, FIFO | 2-5 entries, RAM/CAM | 16 entries    |

**5.1 Energy Model**

Our energy model produces per-access energy numbers for the simulator to use to compute the total energy of each hardware unit. This model extends the energy model in [43] to support tables, caches, wires, stage registers, and execution unit energies and areas. It estimates per-access dynamic energy and per-cycle static energy consumption. The simulator computes the total dynamic energy by incrementing per-access energy of each unit. It computes the total static energy by multiplying the number of simulation cycles by the per-cycle leakage energy of each unit. Other logical blocks in the processor (e.g., control modules) are assumed to have similar energy costs for the baseline OoO and the CG-OoO, and to have secondary effect on the overall energy difference.

RAM tables are modeled as standard SRAM units accessed through decoder and read through sense amplifiers. Static and dynamic energy are generated using SPICE. Then, additional steps including area estimation, energy scaling for different port configurations and cache structures are done. Similarly, CAM tables are designed as standard SRAM units accessed through a driver input module and read through sense amplifiers. To evaluate the energy and area of pipeline stage registers, 6-NAND gate positive edge-triggered flip-flops (FF) are simulated in SPICE.

Different 64-bit execution units including the add, multiply, divide units for arithmetic and floating-point operations are developed in Verilog and simulated in the Design Compiler [4]. The Design Compiler provides per-operation energy numbers for each unit.

**6. EVALUATION**

CG-OoO achieves the performance of OoO at 48% of its total energy cost on SPEC Int 2006 benchmarks [46]. This section quantifies the performance and energy benefits of the CG-OoO processor and the pipeline stages that contribute to its superior energy profile.

**6.1 CG-OoO Performance Analysis**

Figure 11a uses a 4-wide OoO superscalar processor as the baseline for illustrating the relative performance of a 4-wide InO processor with a CG-OoO processor (4-wide front-end and 4 EU’s arranged as a single cluster). In this case, the CG-OoO harmonic mean performance is 7% lower than the OoO baseline. Performance results are measured in terms of instructions per cycle (IPC). In Figure 11b, the same 4-wide InO and OoO configurations are compared against a CG-OoO model with a 4-wide front-end and 12 EU’s spread across 3 clusters. In this configuration, the CG-OoO ILP reaches that of the OoO. As can be observed for Hmmer, Bzip2, and Libquantum benchmarks, the higher availability of computation resources allows exploiting higher ILP.

The first source of performance gain is static block-level list scheduling. Figure 12 shows the effect of static scheduling on performance. On average, static scheduling increases the CG-OoO performance by 14%. In case of Hmmer, 19% more MLP is observed with the origin
This feature leverage the Head Buffer tables. Figure 13 shows the performance gain obtained via varying the number of HB entries. Without Skipahead, 17% of the gap between OoO and InO is closed. Skiphead 2 refers to a HB with two entries; Skiphead 2 closes an additional 67% of the performance gap between InO and OoO. Skiphead 4 (i.e. 4-entry HB) closes the rest of the performance gap. No significant performance difference is observed for larger HB sizes. All CG-OoO results use the statically list scheduled code.

Figure 14 shows the CG-OoO performance as the processor front-end width varies from 1 to 8. Comparing the harmonic mean results for the OoO and CG-OoO shows the CG-OoO processor is superior on narrower designs. A wider front-end delivers more dynamic operations to the back-end. Because the OoO model has access to all in-flight operations, it can exploit a larger effective instruction window. Despite the larger number of in-flight operations, the CG-OoO model maintains a limited view to the in-flight operations making an 8-wide CG-OoO machine not much superior to its 4-wide counterpart.

### 6.2 CG-OoO Energy Analysis

In this section, the source of energy saving within each stage is discussed. Overall, CG-OoO shows an average 48% energy reduction across all benchmarks. Energy results are measured in terms of energy per cycle (EPC). Figure 15a shows the total energy level for the CG-OoO, OoO, and InO processors; Figure 15b shows the harmonic mean energy breakdown for different pipeline stages: all benchmarks follow a similar energy breakdown trend as the harmonic mean. This figure shows the main energy savings are in the Branch Prediction, Register Rename, Issue, Register File access, and Commit stages. Figure 15c shows 61% average energy saving for the CG-OoO compared to OoO.
baseline with similar performance. Since the main contribution of this paper is an energy efficient processor core, Figure 15 excludes cache and memory energy.

Figure 16 shows the inverse of energy-delay (ED) product indicating the favorable energy-delay characteristics of the CG-OoO over OoO for all benchmarks, even those that fall short of the OoO performance such as Sjeng and Gobmk. The CG-OoO is 1.9× more efficient than the OoO on average.

Figure 17 shows the static and dynamic energy breakdown for different benchmarks relative to the OoO baseline. On average, the leakage energy is smaller than 4% of the total energy.

6.2.1 Block Level Branch Prediction

Block-level branch prediction is primarily focused on saving energy by accessing the branch prediction unit at block granularity rather than fetch-group granularity. Figure 18 shows the average block sizes for SPEC Int 2006 benchmarks. For a benchmark application with average block size of eight running on a 4-wide processor, this translates to roughly 2× reduction in the number of accesses to the BPU tables. Figure 19 shows the relative energy-per-cycle for the CG-OoO model compared to the OoO baseline. On average, Block Level BP

![Figure 16: The CG-OoO inverse of energy-delay product normalized to OoO.](image1)

![Figure 17: Static and dynamic EPC normalized to OoO.](image2)

![Figure 18: Average code block size of SPEC Int 2006 benchmarks.](image3)
The register file (RF) used in both OoO and CG-OoO is 256 entries. While the use of local registers enables the use of a smaller global register file in CG-OoO without noticeable reduction in performance, our experiments use equal global register file sizes for fair energy and performance modeling between CG-OoO and OoO.

To reduce the access energy overhead of a unified register file and to increase the aggregate number of ports in the CG-OoO, this processor model breaks the global register file (GRF) into multiple segments. Each segment is placed next to a BW. The access energy to each register file segment is divided by the number of segments relative to the OoO unified register file access energy. Figure 20 also shows the contribution of the global register file energy compared to the OoO baseline; it shows an average 68% reduction in the global register file energy consumption due to register file segmentation. Notice GRF segmentation is not commonly used in OoO architectures; some ARM architectures bank the register file for various purposes such as better thread context switching support. Figure 22 shows the effect of register file segmentation on energy. It shows the case of a unified GRF, one GRF segment per cluster (for a 3-cluster CG-OoO), and one GRF segment per BW. As the number of register segments increases, energy consumption decreases linearly.

Placing a GRF segment next to each BW is energy saving when operations read/write global operands from/to the closest segment. Our register renaming algorithm reduces data communication over wires by allocating an available physical register from the GRF segment nearest to the BW of the renamed instruction.

### 6.2.3 Instruction Scheduling

The CG-OoO processor introduces the Skipahead issue model. In OoO and CG-OoO, in-flight instructions are maintained in queues that are partly RAM and partly CAM tables. For the InO model, instructions are held in a small FIFO buffer. Figure 23 shows the energy breakdown of the dynamic scheduling hardware; it shows the majority of the OoO scheduling energy (75%) is in reading and writing instructions from the RAM table. Another 20% of the OoO energy is in CAM table accesses. The “Rest” of the energy is consumed in stage registers and the interconnects used for instruction wake up and select. This figure also indicates 90% average reduction in the CG-OoO RAM table energy (relative to OoO RAM energy) which is due to accessing smaller SRAM tables, and 95% average reduction in the CAM table energy which is due to using 2 to 4-entry Head Buffers (HB) instead of the 128-entry CAM tables used in the baseline OoO instruction queue. The “Rest” average energy is increased by 40% due to the more pipeline registers at the issue stage. Overall, the CG-OoO issue stage is 84% more efficient than OoO.

### 6.2.4 Block Re-Order Buffer

The CG-OoO processor maintains program order at block-level granularity. This makes read-write accesses
to the BROB substantially smaller than that of OoO ROB. Block write operations are done after decoding each head and block reads are done at the commit stage. Instructions access BROB to notify the corresponding block entry of their completion. In addition, since the BROB is designed to maintain program order at block granularity, it is provisioned to have 16 entries rather than 160 entries used for OoO. The 10× reduction in the re-order buffer size makes all read-write operations 10× less energy consuming. Figure 24 shows 76% average energy saving for CG-OoO.

![Figure 24: The commit EPC normalized to OoO.](image)

## 6.3 Clustering and Scaling Analysis

The CG-OoO architecture focuses on reducing processor energy through designing a complexity-effective architecture; to remain competitive with the OoO performance, this architecture supports a larger number of execution units (EU). To do so, the CG-OoO model must employ a design strategy that is more scalable than the OoO. A cluster consists of a number of BW’s sharing a number of EU’s. To illustrate the effect of different clustering configurations, the experimental results in this section assume three clusters.

![Figure 25: Normalized Performance & Energy for different clustering configurations. All configurations assume a 3-cluster CG-OoO model; the total number of BW’s and EU’s is calculated through multiplying the above numbers by 3. Here, performance is measured as the harmonic mean of the IPC and the energy is measured as the harmonic mean of the EPC over all the SPEC Int 2006 benchmarks.](image)

![Figure 26: The energy versus performance plot showing different CG-OoO configurations normalized to the OoO. The CG-OoO core configurations illustrate the energy-performance proportionality attribute of the CG-OoO. Performance is measured as the harmonic mean of the IPC and energy is measured as the harmonic mean of the EPC over the SPEC Int 2006 benchmarks.](image)

**Figure 26** shows the energy-performance characteristics of the CG-OoO model plotting all the cluster configurations presented above. The lowest energy-performance point in the plot refers to the 1 BW, 1 EU per cluster configuration and the highest energy-performance point refers to the 6 BW, 8 EU per cluster configuration. This figure suggests as the

7. CONCLUSION

The CG-OoO leverages a distributed micro-architecture capable of issuing instructions from multiple code blocks concurrently. The key enablers of energy efficiency in the CG-OoO are (a) its end-to-end complexity effective design, and (b) its effective use of compiler assistance in doing code clustering and generating efficient static code schedules. Despite the reliance of the CG-OoO architecture in providing energy efficiency static code, it requires no profiling. This architecture is an energy-proportional design capable of scaling its hardware resources to larger or smaller computation units according to the workload demands of programs at runtime. The CG-OoO supports an out-of-order issue model at block granularity and a limited out-of-order issue model at instruction granularity (i.e. within block). It leverages a hierarchical register file model designed for energy efficient data transfer. Unlike most previous studies, this work performs a detailed processor energy modeling analysis. CG-OoO reaches the performance of the out-of-order execution model with over 50% energy saving.
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