Physical Modeling the Impact of Self-Heating on Hot-Carrier Degradation in pNWFETs

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Abstract—We develop and validate a physics-based modeling framework for coupled hot-carrier degradation (HCD) and self-heating (SH). Within this framework, we obtain the lattice temperature distribution throughout the device by solving the lattice heat flow equation coupled with the drift-diffusion approach. Then, the evaluated temperature spatial profile in the transistor is taken into account while solving the Boltzmann transport equation for carriers to obtain the carrier energy distribution functions, which are needed to compute the rates of the single- and multiple-carrier mechanisms of bond dissociation. The effect of SH on HCD is threefold: (i) it results in a significant distortion of the carrier distribution function, (ii) device heating decreases vibrational lifetime of the Si-H bond, thereby suppressing the multiple-carrier mechanism, and (iii) the rate of thermal bond-breakage becomes higher due to SH. The model is capable of accurately reproducing relative changes in the saturation drain current with stress time measured in p-channel nanowire field-effect transistors subjected to SH during different stress conditions. We show that neglecting SH leads to substantial underestimation of HCD.

Index Terms—Hot-carrier degradation, self-heating, transport, interface states, NWFET, modeling

I. INTRODUCTION

Hot-carrier degradation (HCD) accelerated by self-heating (SH) was highlighted to be the most detrimental reliability concern in modern ultra-scaled field-effect transistors (FETs) with confined architectures, such as nanowire (NW) and FinFETs\textsuperscript{[1–3]}. This is because in modern FETs device dimensions reduce faster than the operating and stress voltages, thereby resulting in high electric fields. On top of this, channel lengths in scaled devices are comparable to (or even shorter than) the mean free path of carriers and therefore electrons/holes dissipate much less energy due to scattering events. These factors lead to substantial acceleration of carriers even in decanometer transistors and hence to prominent hot-carrier degradation. As for the intimately related phenomenon of bias temperature instability (BTI), it was reported to be less destructive in ultra-scaled transistors than HCD\textsuperscript{[1]}. Moreover, special measures how to control and alleviate BTI were recently proposed and validated\textsuperscript{[4, 5]}. These techniques are based on shifting the defect band towards the energy range inaccessible for the carriers by tuning the work-function and introducing dipoles between SiO\textsubscript{2} and high-\textit{k} layers. However, comparable approaches to mitigating HCD were not elaborated so far and thus better understanding of the physical mechanisms responsible for HCD should help us develop such approaches.

In confined structures, such as FinFETs and NWFETs, narrow channels are surrounded by dielectric layers with a low thermal conductivity and therefore heat dissipation in these channels is hindered. As a consequence, local lattice temperature in a nanowire/fin channel can be substantially higher than ambient temperature. This effect is called “self-heating”\textsuperscript{[6]}. On the other hand, it is widely acknowledged that in short-channel MOSFETs HCD becomes stronger at elevated temperatures\textsuperscript{[7–10]}, as opposed to long-channel transistors where HCD is weaker if a device is heated\textsuperscript{[11–13]}. Therefore, self-heating enhances hot-carrier degradation and an accurate predictive model for HCD should consider the impact of SH on this detrimental phenomenon.

Although there are a number of carefully validated physical models\textsuperscript{[10, 14–18]} for HCD as well as physics-based simulation approaches to SH\textsuperscript{[6, 19, 20]}, they have not been combined within a single simulation framework. To the best of our knowledge, the attempts to model the impact of SH on HCD published so far are empirical and phenomenological\textsuperscript{[21–24]}. However, HCD itself is a very intricate effect, which stems from rupture of Si-H bonds at the Si/SiO\textsubscript{2} interface induced by hot and cold carriers via single- and multiple-carrier (SC- and MC-) mechanisms of bond dissociation\textsuperscript{[14, 25–28]}. Understanding the fashion of how SH impacts the rates of these mechanisms is a non-trivial task, which is, however, of high importance because switching from harsh stress regimes to the operating conditions is accompanied by reduction of the relative role of the SC-mechanism\textsuperscript{[10]}. As a result, a predictive model for HCD should accurately capture this trend, which is made even more complex by SH. Since empirical/phenomenological models are not capable of reproducing this behavior, one needs to thoroughly describe the physical picture behind HCD accelerated by SH.

To bridge the gap between models for HCD and SH we extend our hot-carrier degradation simulation framework and model carrier transport, the bond-breakage rates, and degradation of transistor characteristics considering non-uniform temperature distributions due to SH. To validate the model we use hot-carrier degradation data acquired in p-channel NWFETs.

II. DEVICES AND EXPERIMENT

We employed p-channel gate-all-around NWFETs on Si. Each of these devices is designed up of 44 (22×2) stacked parallel NWs with a diameter of 9 nm and a gate length of 100 nm; the devices are sketched in Fig. 1. The high-\textit{k} gate stack contains SiO\textsubscript{2} and HfO\textsubscript{2} layers with thicknesses of...
0.7 and 2.1 nm, respectively. More details of the fabrication process and device architecture can be found in [29].

The NWFETs were subjected to hot-carrier stress at three different combinations of voltages: \( V_{gs} = -1.3 \, V, V_{ds} = -1.6 \, V \); \( V_{gs} = -1.3 \, V, V_{ds} = -1.9 \, V \) and \( V_{gs} = -1.3 \, V, V_{ds} = -2.2 \, V \). Stresses were applied for \( \sim 500 \, ks \) at ambient temperature of 298 K. To assess HCD we recorded relative changes of the saturation drain current \( \Delta I_{d,sat} \) as a function of stress time \( t \) and summarized them in Fig. 2. Note that \( I_{d,sat} \) corresponds to \( V_{gs} = V_{ds} = V_{dd} (V_{dd} = 0.9 \, V \) is the operating voltage).

During measurements, special attention was paid to ensure that the degradation is driven by HCD and BTI does not make a significant contribution. For this, we checked whether the degradation has a recoverable component and found that recovery can be neglected; this proofs that BTI, which is mainly due to trapping of carriers by oxide traps, can be indeed disregarded. Moreover, we stressed in a regime with relatively high drain voltage of \( V_{ds} > 1.0 \, V \) in combination with room ambient temperature \( T = 298 \, K \) to further weaken possible contributions of BTI. In this regime the degradation is dominated by a superposition of SC- and MC-mechanisms of Si-H bond dissociation [10, 30]. More details of our measurements are given in [31].

III. THE MODELING FRAMEWORK

We extend our model for hot-carrier degradation (sketched in Fig. 3), which was validated against HCD data measured across a wide class of transistors [30, 32–34], in the manner as to incorporate a non-uniform distribution of lattice temperature \( T \) resulting from SH. Note that in our recent publication [35] the model was demonstrated to reproduce HCD in the same pNWFETs but the impact of SH was not addressed.

Within this model, HCD is assumed to be driven by dissociation of Si-H bonds at the Si/SiO\(_2\) interface. Bond rupture can be induced by a solitary highly energetical carrier which energy higher than the bond-breakage energy (\( E_a \sim 2.6 \, eV \) [36]). This mechanism is called “single-carrier mechanism” (Fig. 4). If \( V_{ds} < E_a/|e| \) (\( e \) is the electron charge) the concentration of these energetical carriers is low and the SC-mechanism has a negligible rate. However, HCD can still be strong even in ultra-scaled devices because in this case bond rupture is driven by the MC-process, which is based on the multiple vibrational excitation of the bond [14, 25, 26, 37], see Fig. 4. The SC- and MC-mechanisms are two alternative pathways of the same reaction converting the defect precursors (Si-H bonds) into the electrically active defects (P\(_n\)-centers) and these processes are coupled. Moreover, in ultra-scaled MOSFETs with stress drain voltages in the range of 1.2-2.0 V the most probable scenario of bond dissociation is related to initial pre-heating the bond via inducing its vibrational modes by cold carriers, followed by its rupture by a single hot carrier [15, 38]; this scenario is sketched in Fig. 4, right panel. Within this picture, the potential barrier separating an excited (but still bonded) level is reduced as compared to the bonding energy \( E_a \) by the energetical position of this level. Therefore, the probability that the carrier ensemble contains particles possessing this energy or higher can be substantially high.

To calculate the rates of SC- and MC-mechanisms one needs to know how the carriers are distributed over energy; this infor-
A schematic representation of our model for HCD. The previous given stress time step in the drain current, i.e. at each times step models are not so critical because we consider relative changes reducing the carrier mobility. Both aspects are captured in MINIMOS-NT. At this stage, possible errors in calculations perturb the electrostatic potential and scatter carriers, thereby the effect of charged interface states is twofold, i.e., they implemented in MINIMOS-NT. Therefore, we solve the coupled drift-diffusion and lattice heat flow equations only once, obtain the temperature distribution, and compute the carrier DFs based on this distribution.

Another important ingredient taken into account in the extended model is the temperature dependency of the lifetime of the stretching vibrational mode of the Si-H bond. Note the Si-H bond has stretching and bending vibrational modes but bond rupture occurs via the stretching mode, as it was discussed in sufficient detail in [10,46]. Andrianov et al. [47, 48] have shown that vibrational lifetime is a decaying function of $T$, i.e. at higher $T$ an excited Si-H bond returns faster to the ground state and this reduces the MC-process rate [14, 25, 38]. In one of our publications [10] we discussed in sufficient detail that the dependence of vibrational lifetime on $T$ is an important factor, which should be considered while modeling HCD and its temperature behavior.

Dissociation of a Si-H bond can occur from excited bonded states by a superposition of (i) the contribution given by carriers which deliver a portion of energy higher than the potential barrier separating this bonded state and the transport mode and (ii) thermal activation over this potential barrier (see Fig. 4). In this case the bond-breakage rate is evaluated as

$$R_{SC,i} = \omega_{\text{th}} \exp \left[ -\frac{E_a - E_i}{k_B T} \right] + I_{SC,i},$$  

where $\omega_{\text{th}}$ being the attempt frequency for thermal activation, $i$, $E_i$ the index of the excited level and its energetical position, and $k_B$ the Boltzmann constant; a more detailed description is provided in [30, 38]. In (1) the first term corresponds to thermal breakage of the bond, while the second term represents the SC-process rate from an excited level $i$. On can see that the first term is a rapidly increasing function of $T$.

The rate $I_{SC,i}$ is calculated as

$$I_{SC,i}(E_a) = \int f(E) g(E) \sigma_0 (\varepsilon - E_a + E_i) \rho_{\text{a}}(\varepsilon) \nu(E) dE,$$

with $f(E)$, $g(E)$, $\sigma_0(\varepsilon)$, and $\nu(E)$ being respectively the occupation number as a function of energy $E$, the density-
It is noteworthy that changes in the carrier DF (the product \( f(E)g(E) \)) - due, for example, to SH - can result in substantial changes in the bond-breakage rate \( I_{\text{SC},i} \). In the extended model, the interplay between all the aforementioned components is considered.

### IV. RESULTS AND DISCUSSION

Fig. 5 summarizes temperature distributions evaluated for three stress conditions; these distributions are shown for the channel and source/drain extensions. First of all, one can see that lattice temperature can be substantially higher than ambient temperature and this effect becomes more pronounced at higher drain voltages. (Let us remind that the gate voltage is fixed and equal to \(-1.3 \text{ V}\)). This is because at higher values of \( V_{\text{ds}} \) and a fixed \( V_{\text{gs}} \) the density of power dissipated in the transistor channel is higher, thereby making the effect of self-heating stronger. Another important feature pronounced in Fig. 5 is that lattice temperature peaks in the drain end of the channel and this trend is similar to one of the main peculiarities of HCD, i.e. its strong localization near the drain. In both cases of SH and HCD the carriers need to travel some distance in the transistor until they are accelerated to energies high enough to substantially heat the devices or trigger a bond-breakage event. For the sake of better visibility, we made one dimensional cuts of temperature distributions (Fig. 5) at the Si/\( \text{SiO}_2 \) interface and obtained temperature dependencies vs. the coordinate \( z \) in the source-drain direction, which are shown in Fig. 6 for all stress conditions. Note that as the channel has a cylindrical symmetry, these one-dimensional temperature profiles are the same for different values of the coordinates \( x \) and \( y \) in the plane perpendicular to the source-drain direction. Fig. 6 shows exactly the same trends as Fig. 5: the temperature peak becomes higher at higher \( V_{\text{ds}} \) and is situated near the drain.

Fig. 7 shows a series of hole DFs computed with and without the impact of distributed temperature for \( V_{\text{gs}} = -1.3 \text{ V} \) and \( V_{\text{ds}} = -1.6 \text{ V} \) and plotted for \( z = 50 \text{ nm} \) (exactly in the middle of the device), \( z = 75 \text{ nm} \), and \( z = 100 \text{ nm} \) (the drain end of the channel). Let us note that the hole DFs are substantially shifted from equilibrium, i.e., they are visibly non-Maxwellian. Nevertheless, the Maxwellian tail can be seen at higher energies. However, when we proceed closer to the drain (where carriers are hotter than in the center of the NWFET) this tail shifts to even higher energies and in general the DFs transform become more non-Maxwellian.

Another important peculiarity is that DFs obtained considering the impact of SH are shifted towards higher energies with respect to those computed neglecting SH. Based on this trend, one can conclude that the SC-process induced portion of the damage should have a higher rate due to SH (as can be seen from formula (2)) and therefore HCD in general is enhanced by SH. At a first glance, the reported behavior of the hole DFs seems counterintuitive because the scattering mechanisms – which suppress the high energetical fraction of the carrier ensemble – become more efficient at elevated temperatures, thereby weakening HCD. However, the segment where the DF values increase with energy (for instance, for the drain DFs this increase corresponds to the energy range of [0-0.7] eV) is due to the interactions of carriers with phonons. Due to the temperature activation of this process the aforementioned segment becomes wider if SH is considered, thereby leading to the shift of the high-energetical tails of the DFs. This effect is consistent with the scenario reported by Abramo et al. [49], in which carriers can gain energy from phonons if the number of adsorbed phonons exceeds the number of emitted ones and these interactions can be responsible for enhancement of HCD in sub-0.1 \( \mu \text{m} \) transistors.

From Fig. 2 one can see that \( \Delta I_{\text{d,sat}}(l) \) traces simulated without the impact of SH on HCD are lower compared to those obtained considering this impact. The difference in the \( \Delta I_{\text{d,sat}} \) changes is especially pronounced at short stress times. Such an observation appears consistent with our previous findings that short-term HCD is determined by the near-drain portion of the damage induced by the single-carrier process (accelerated by the multiple-carrier mechanism though) [32, 33]. Our current modeling results suggest that SH makes the most prominent impact on the single-carrier process accelerated by the vibrational excitation of the bond induced by cold carriers, see Fig. 4 and Eqs. (1) and (2), and therefore the impact of SH on \( \Delta I_{\text{d,sat}} \) changes are most prominent for short stress times. Nevertheless, one can see that neglecting SH results in substantial HCD underestimation also at longer stresses. It is noteworthy, however, that larger values of \( \Delta I_{\text{d,sat}} \) obtained when SH is taken into account stem not exclusively from the behavior of hole DFs but also from the \( T \) dependence of the SiH bond vibrational lifetime and thermal contribution to bond rupture, as discussed in Section III. Finally, one can see that the model can cover the degradation traces with good accuracy.
Fig. 5. Lattice temperature distributions computed with the device simulator MINIMOS-NT for three combinations of stress voltages. SH results in severe temperature non-uniformity. The sketch shows the nanowire channel as well as the source and drain channel extensions; the source is situated in the left side of the device. The data are obtained for $V_{gs} = -1.3\ V$, $V_{ds} = -1.6\ V$ (upper panel), $V_{gs} = -1.3\ V$, $V_{ds} = -1.9\ V$ (central panel), and $V_{gs} = -1.3\ V$, $V_{ds} = -2.2\ V$ (lower panel).

V. CONCLUSIONS

We presented and validated a framework for modeling coupled self-heating and hot-carrier degradation; this framework is physics-based. The impact of SH on HCD is a superposition of features of carrier transport at distributed temperature, the temperature dependency of the vibrational lifetime of the bond, and the thermal contribution to bond dissociation. To obtain lattice temperature changes due to SH we solved coupled drift-diffusion and heat flow equations. The impact of non-uniformly distributed temperature on carrier transport was shown to shift carrier energy distribution functions towards higher energies. Our extended framework is capable of representing experimental degradation traces acquired in pNWFETs with good accuracy and shows that neglecting SH results in substantial underestimation of HCD.

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