IoT Systems with Low-Power SRAM Memory Architecture

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ABSTRACT

A quantitative and yield analysis was made and tested on a single-bit cache memory design using a range of resistor values and various sense amplifier types, such as the voltage mode differential sense amplifier (VMDSA). In a single-bit cache memory design, the voltage mode differential sense amplifier uses the least power. The low power consumption and long access times of this SRAM will be very advantageous for the Internet of Things (IoT).

Keywords: Write Driver Circuit (WDC); Sense Amplifier (SA); Voltage Mode Differential Sense Amplifier (VMDSA); Single Bit SRAM VMSA Architecture (SBSVMA); Static Random Access Memory Cell (SRAMC).

1.0 Introduction

A typical Internet of Things (IoT) sensor is made up of microcontrollers, wireless computers (Bluetooth, Wi-Fi, and LoRa), and a random-access memory cell (RAM) (SRAMC). SPI and I2C are two serial bus standards that enable communication between electrical devices. Sensor nodes use these protocols because of their low power consumption and slow data transmission and reception. The IoT node’s MCU is in charge of all crucial operations. Data transmission between devices is the responsibility of this section. To the nearest gateway possible, data from sensors and wireless directives for system management should be transferred. Digital temperature and humidity readings are sent over the SPI/I2C serial interface. The local data is stored in SRAM in the absence of a gateway. This method creates and stores all of the necessary signals in place of the SRAM’s internal clock. The circuit can therefore be scaled up or down depending on the application’s requirements and is easy to understand [1, 2]. SPI signals were the main source of control signals up until recently.

Embedded storage is widely employed for developing systems on chips (SOCs). The International Technical Roadmap for Semiconductors predicts that by 2025, memory will make up around 90% of SOCs. Memory is a critical component of many technologies, including computers with microprocessors. The digits 0 and 1 are used to store information and data. Memory is needed to run programs and keep data. Digital systems must be able to store data both permanently and temporarily to do this [3-5].

Nowadays, a growing number of people rely on portable technology. Some examples of low-power devices are medical devices, wireless communication systems, and portable media players. For chip designers to integrate more memory and logical circuits onto a single chip, numerous attempts have been made to develop low-power circuitry.

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According to scientists, the creation of unique logical and memory circuits is anticipated to be made possible by a new chip manufacturing technology. As a result, numerous new CPUs and memory architectures were made possible. There have also been investigations into static memory [6–8]. Yes, as the SOC circuit is the most important part. Due to their high leakage rates and high transistor counts, these circuits have come to be known as "high-density circuits." Energy use decreased as a result. There will be a decline in the data’s consistency, nevertheless. Static memory is more prevalent in portable devices with DRAM memory than SRAM memory because DRAM memory has to work more to maintain data constant [9 -11]. Access times to static and dynamic memory are essentially equal.

2.0 Single-Bit Memory Architecture

The single-bit cache memory architecture shown in Figure 2 comprises WDC, SRAMC, and VMSA. I’ll break it up into three sections to make things simpler. Two pins on the WDC, WE and Bit, are connected.

Data is output using the WDC’s BL and BLBAR output pins. The three input pins of the SRAMC are WL, V1, and V2. The VMSA has five input pins: SAEN, PCH, BL, BLBAR, and Ysel.
2.1 Write driver circuit

This framework makes use of the write driver schematic displayed in Figure 3. One of the goals of WDC is to reduce the high pre-load of the bit line to a level below the writing margin of the SRAMC. "WE=1" instructs how much voltage to apply to a bit line to obtain the required value from the WDC Access transistors to send data to a particular memory cell (write enable pulled high). To avoid bit line hiccups, the WDC output has a buffer circuit in front of it. Only when a specific value of the bit cell is present can the WDC be accessed. To write the required Bit, the circuit charges and empties the memory cell’s bit lines [12-14].

![Figure 3: Write Driver Circuit Schematic](image)

2.2 Conventional SRAM

Figure 4 depicts the 6T SRAMC schematically. SRAMCs are "static RAM cells" when data is kept for a long time. The SRAMC comprises six transistors: two CMOS inverters, two NM8/9 access transistors, and four cross-connected PMOS transistors (PM6, PM7, NM6, and NM7). The SRAMC and transistors in each Bit work together to produce cross-coupled inverters. [15, 16] There are only two conceivable states for the cell: 0 or 1.

![Figure 4: SRAM Cell Schematic](image)

2.3 VMSA

Every part needed for differential sensing is included in the MOS differential voltage sense amplifier circuit. A differential amplifier can treat small signals as if they were single-ended. To
increase the difference between two signals and enhance their difference, a differential amplifier must be able to filter out common noise [17,18].

VMSA is not appropriate for use in memory because they operate slowly, draw a lot of power, and have a sizable offset. The basic differential voltage mode sensing amplifier is shown in Figure 5. This group comprises three NMOS transistors (NM8-NM10) and seven PMOS transistors (PM8-PM14). This circuit operates effectively by utilizing the slight difference between the bit lines and the output nodes [19,20].

**Figure 5: Schematic of VMSA**

![Schematic of VMSA](image)

3.0 Analysis of Result

The outputs of the circuits have been shown and described in this section. To ascertain how R affects how much power a circuit uses, the amount of power utilized by the cache memory is tracked and compared to changes in R’s value.

**Figure 6: Output Waveform of WDC**

![Output Waveform of WDC](image)
In Figure 6, several WDC waveforms are displayed. When they are both VDD, WE are 0V, BL is 0V, and BLBAR is VDD. In this case, the Bit is 0V. The voltages in WL, BL, and BLBAR are all zero volts. Therefore, the Bit is equal to VDD. In this scenario, Bit is set to VDD, and WE, BL, and BLBAR are set to 0.

Figure 7 shows how to write and store data using the SRAM cell. A sensing amplifier has a pull-up and pull-down transistor for storing and retrieving data.

**Figure 7: Output Waveform of SRAM Cell**

![Output Waveform of SRAM Cell](image)

When both SAEN and WL are at their greatest values, as seen in Figure 8, the VMSA measurement is shown. This sensing amplifier can read only the bit lines of SRAM cells. Then, bit lines transmit data to V3 and V4, respectively.

**Figure 8: Output Waveform of VMSA**

![Output Waveform of VMSA](image)

According to Table 1, power consumption falls as resistance rises. A circuit’s size, speed, or usefulness are unaffected by the amount of resistance obstructing current flow.

**Table 1: Different Parameters of SBSVMA**

| Parameters | Power Consumption | No. of Transistors | Sensing Delay |
|------------|-------------------|--------------------|---------------|
| R=42.3Ω   | 20.05 μW          | 32                 | 21.22μs       |
| R=42.3KΩ  | 9.50μW            | 32                 | 21.22μs       |
4.0 Conclusion

Cache memory for single bits was provided by several sense amplifiers, including voltage differential sense amplifiers. Researchers investigated several resistors’ power usage, sensing time, and transistor count. In a single-bit cache memory design, the voltage mode differential sense amplifier uses the least power.

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