Research on Silicon Wafer Manufacturing Process and Physical Properties Testing Using High-Purity Polysilicon

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Abstract. The shape of a bare wafer is round, so it is called a wafer or a silicon wafer. It is the basis for the production of silicon semiconductor integrated circuits. The silicon wafer is cut from a large piece of semiconductor material silicon ingot. The high-purity polysilicon (its purity is up to 99.999999999%) is into a large single crystal, given the correct orientation and an appropriate amount of N-type or P-type doping, a silicon ingot is obtained through five-step crystal growth. Wafers (wafers) are then made from silicon ingots by more than eight processes. This paper investigates the single crystal silicon growth and wafer preparation process technology, and finally discusses the evolution of wafer size growth and changes in the development of the semiconductor industry chain.

Keywords: CZ method; wafer preparation technology; wafer inspection; wafer size evolution.

1. Quartz sand to semiconductor-grade-silicon, SGS
The first stage of silicon wafer preparation is the selection and purification of quartz sand raw materials [1]. Quartz sand is a quartz particle produced by crushing quartz stone as shown in Figure 1. Quartz sand is a hard, wear-resistant, chemically stable silicate mineral, its main mineral composition is SiO2, its colour is milky white, or colourless and translucent, its hardness is 7, its density is 2.65, its chemical, thermal and mechanical properties have obvious anisotropy, insoluble in acid, slightly soluble in KOH solution, melting point 1750°C.

Figure 1. Quartz sand (coarse and fine).
The preparation of high purity silicon begins with the production of industrial silicon (crude silicon) from silica (SiO$_2$), which is then made into high purity polycrystalline silicon and finally manufactured with silicon monocrystals, a semiconductor material. From ore to SGS, the process of its production process is: crushed crude silicon is treated with hydrochloric acid, aqua regia and (HF + H$_2$SO$_4$) mixed acid in turn, and finally washed with distilled water to neutral and dried to obtain industrial crude silicon with a content of 99.9%. The current method of preparing high purity silanes by pyrolysis is a promising method for preparing high purity silicon. Such silicon has a purity of 99.9999999%. SGS is one of the purest substances on earth; it is a polycrystalline or polycrystalline silicon crystal structure, as shown in Figure 2.

![Illustration of the ortho-tetrahedral structure of silicon](image)

**Figure 2.** Illustration of the ortho-tetrahedral structure of silicon

2. **SGS from monocrystalline silicon growth into silicon ingots**

The conversion of a polycrystalline block into a large single crystal, given the correct orientation and the right amount of N-type or P-type doping, is called crystal growth. The common process for the growth of monocrystalline silicon rods is the Czochralski method (CZ method). This is the mainstream technology for growing single crystalline silicon. The CZ method is characterized by aggregation in a straight thermal system with graphite resistance heating, melting the polysilicon contained in a high purity quartz crucible, then inserting the crystal seed into the surface of the melt for fusion, turning the crystal seed at the same time and then reversing the crucible, the crystal seed is slowly lifted upwards, after crystal attraction, amplification, shoulder turning, isometric growth, finishing and other processes, a silicon single crystal is grown.

The basic principle of the CZ method is that a crucible made of fused silica is filled with polycrystals in a vacuumable chamber, which is refilled with a protective atmosphere and heated to around 1500°C. A chemically etched crystal seed (about 0.5cm in diameter and 10cm long) is then lowered into contact with the polycrystalline melt. The crystal seed must be strictly oriented, as it is a replica, and a rotating and lifting crystal seed rod is located above the crucible, with a collet at the lower end of the rod to hold the crystal seed on which the large, bulleted crystals will be grown. The ingots can be over 300 mm in diameter and 1-2 m in length.

After the raw material has been melted by the heater, the seed crystals are placed into the melt and the suitable temperature is controlled to reach the saturation temperature. While rotating and lifting, the silicon in the crucible is heated by the single crystal furnace and the silicon becomes molten; the seed crystals come into contact with the surface of the melt and rotate in the opposite direction to the rotation of the crucible. As the seed crystals leave the melt during the direct pulling process, the liquid on the melt is raised due to surface tension and as the seed crystals are pulled out of the melt, single crystals with the same crystal orientation as the seed crystals are grown and the required silicon single crystals are obtained, as shown in Figure 3.
Single crystal silicon growth process by CZ method\textsuperscript{3}, as shown in Figure 4.

(1) Crystal seed welding; (2) Seeding and necking; (3) Shoulder placement; (4) Equal diameter growth; (5) Crystal collection.

CZ method process operation flow: preparation $\rightarrow$ opening $\rightarrow$ growth $\rightarrow$ stopping.

Note: n-type and p-type doping should be carried out in the silicon melt; it is divided into very light doping; light doping; moderate doping; and heavy doping. When silicon is doped with one part per million of phosphorus or arsenic, the electrical conductivity is enhanced by a factor of 1.25 million. SGS grows through single crystal silicon and becomes a silicon ingot (or silicon rod) with a purity of up to 99.999999999%, as shown in Figure 5.

3. The production process from silicon ingot to wafer

From the silicon ingot to the wafer, the preparation process is as follows.

(1) Silicon rod shaping. Shaping process: remove both ends; radial grinding; silicon wafer positioning edge or positioning groove.
(2) Crystal orientation. Methods of crystal orientation include the optical image orientation method, etc.

(3) Crystal surface marking. A. Main reference surface (main positioning surface, main mark surface) for silicon wafer positioning edge marking; to identify the scribing direction; as a reference surface for silicon wafer (ingot) mechanical processing positioning and wafer mounting contact position, can reduce silicon wafer loss. B. Secondary reference surface (secondary positioning surface, secondary mark surface); to identify the crystal direction and conductive type. C. Positioning slots are used instead of positioning edges for wafers 200 mm diameter and above, as shown in Figure 6, Figure 7 and Figure 8.

Figure 6. Positioning edge marking for wafers over 200 mm.

Figure 7. Primary and secondary positioning surfaces of small diameter wafers.
(4) Sliced. It is wafer dicing. After the finished product is formed, the wafer must be diced before it can be used in chip manufacturing. The bare wafers cut from silicon crystal pillars have good luster, like a mirror, as shown in Figure 9.

(5) Grinding and chamfering. The grinding of the wafer will make the thickness of each wafer consistently so that the thickness of each silicon wafer uniform in all places, and improve the flatness. The abrasives for the grinding piece are required to be harder than the silicon wafer hardness.

(6) Polishing. There is a thin layer of surface defects on the surface of the wafer after the completion of the ordinary grinding of the wafer. The polishing used is mechanical plus chemical method, called chemical-mechanical polishing (CMP). After the polishing process, the surface of the silicon wafer truly reaches an ideal surface that is highly flat and smooth as a mirror, as shown in Figure 10 and Figure 11.
(7) Wafer marking. In the manufacturing process, wafers must be distinguished to maintain accurate traceability and prevent misoperation, and use barcode or digital matrix of laser-engraved numbers to distinguish them.

(8) Wafer inspection. The technical indicators of silicon wafer inspection include: dimensions (diameter, thickness), crystal orientation, resistivity, flatness, defect density and finally the generation and inspection of epitaxial layers.

One of the main wafer inspections is Wafer surface inspection. (General Surface Defects and Stains)

A. General surface defects and dirt inspection (Automatic detection of stains on the wafer surface and defect classification of surface quality).

B. Thickness variation & resistance measurement (TTV & Rs Measurement).

Figure 11. An almost perfect wafer surface.

Figure 12. The uneven thickness surface of the wafer.
The second main test is: silicon wafer defect detection; there are often three kinds of detection: point defects caused by stress which caused by impurity atoms squeezing the crystal structure in the crystal; dislocations caused by a group of cells in a single crystal in the wrong position; crystal slippage produced by the crystal plane and crystal layer defects caused by the growth of two different directions at the same interface, as shown in Figure 12.

4. Evolution of wafer size
The semiconductor chip industry is the foundation of the integrated circuit technology and application industry; the semiconductor chip industry chain has complex processes and procedures, and wafer manufacturing and processing are in the midstream of the semiconductor chip industry chain.

The development of high-density and large-size chips requires larger diameter wafers due to the extended demands of the semiconductor chip industry chain. Driven by Moore's Law, chip wafer sizes grew from 6 inches to 8 inches and finally to 12 inches (see table below). From 1960 to the early part of the 21st century, it has shifted to 300mm (12-inch) diameter wafers, and now it is shifting to the 450mm (18-inch) field. The larger the wafer area, the more chips can be produced, which not only reduces the cost but also increases the probability of goodness [5]. It is still the age of 12-inch wafers. Although 18-inch wafers are a certain direction for the semiconductor industry to drive, the technical hurdles are higher than expected and there are currently very few semiconductor fabs in the world capable of entering the 18-inch wafer era, as shown in Table 1.

| Wafer size      | Wafer thickness | Year of manufacturing | Weight/piece | 100mm² (die per wafer) |
|-----------------|-----------------|-----------------------|--------------|------------------------|
| 1-inch (25mm)   | 275 μm          | 1960                  | 10           | 56                     |
| 2-inches (51mm) | 375 μm          | 1972                  |              |                        |
| 3-inches (76mm) | 525 μm          | 1976                  | 10           | 56                     |
| 4-inches (100mm) | 625 μm          | 1981                  |              |                        |
| 4.9-inches (125mm) | 675 μm          | 1983                  | 10           | 56                     |
| 5-inches (150mm) | 725 μm          | 1992                  | 53           | 269                    |
| 6-inches (usually) | 775 μm          | 2002                  | 125          | 640                    |
| 7-inches (usually) | 925 μm          | future                |              |                        |
| 8-inches (usually) | 1000 mm²       | future                |              |                        |

5. Conclusions
The semiconductor chip industry chain and wafer size growth are driving each other's development. Under the influence of Moore's Law, wafer diameters are constantly moving towards 18 inches (450 mm).

However, in the process of developing large-size silicon wafers, our technical difficulty lies in the fact that the consistency and pollution of crystal structure and electrical properties during crystal growth are challenges. There are also issues in wafer preparation, flatness, diameter control, and crystal integrity.
Larger diameter wafers require more robust process equipment. A 450mm wafer has a mass of about 800kg and a length of 210cm. Growing and preparing 450mm wafers are equally challenging. Higher process specifications demand and challenge go hand in hand. The manufacture of larger diameter wafers is the key and the driving force behind the continuous progress in chip manufacturing.

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