22–27 GHz 11 dB inductive feedback cascode amplifier with 12 picoseconds group delay variation

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Abstract: This paper uses the transmission line to implement the inductive feedback cascode amplifier to achieve 16.9% group delay variation from 22 GHz to 27 GHz. The transfer function of the second-order all-pass network, derived from the two-port Y-parameter, is applied to synthesize the group delay. A prototype, fabricated in the 0.13 µm CMOS technology, is characterized through the on-wafer testing. The measurements show a power consumption of 12 mW from 1.2 V, an amplifier gain of 11 ± 0.4 dB, a noise figure (NF) of 5.1 ± 0.4 dB and a group delay of 71 picoseconds (ps) with a variation of ±6 ps from 22 GHz to 27 GHz. From 21 GHz to 27 GHz, the measured input 1-dB compression point (IP\(_{1dB}\)) and the input third-order intercept point (IIP3) are higher than −9.2 dBm and +4.2 dBm, respectively.

Keywords: CMOS, all-pass, cascode amplifier, group delay, linearity

Classification: Integrated circuits

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1 Introduction

Wideband systems need the radio frequency (RF) front-end amplifier to achieve the signal amplification with a small group delay variation and contribute little noise in the broadband frequencies [1, 2, 3]. Fig. 1 shows the statistic of the reported monolithic amplifiers with the multiple feedbacks to minimize the group delay variation. The SiGe prototype in [4] used the capacitive, the inductive, and the resistive feedbacks to implement the four-stage common-emitter (CE) amplifier, demonstrating a group delay of 128 ps with $\pm 28$ ps variation from 3 GHz to 10 GHz. The CMOS prototypes in [6, 7] designed the amplifiers with the resistive feedback and the RLC-branch to accomplish the group delay of 75 and 86 ps with the variations of $\pm 16.7$ and $\pm 22$ ps from 3.1 GHz to 10.6 GHz, respectively.

![Fig. 1. Statistic of the wideband monolithic feedback amplifiers.](image)

All the reported amplifiers have the resistors in the feedback loops [4, 5, 6, 7, 8, 9]. The feedback resistor in the first stage [7] makes higher noise figure than the resistor in the third and fourth stages [8]. The resistive feedback architecture, achieving lower gain per amplifier stage, needs to cascade the multiple stages to produce the sufficient amplifier gain [4, 8, 9]. Additionally as shown in Fig. 1, all
the resistive feedback amplifiers have a group delay variation higher than 20%. To reduce the group delay variation and improve the product of gain and bandwidth per stage, this paper uses two TLs to realize two inductive feedbacks in the single-stage cascode amplifier to achieve a group delay variation of ±6 ps and a gain of 11 dB from 22 GHz to 27 GHz. Fig. 2 shows that the proposed amplifier achieves the highest gain-bandwidth product per stage with the lowest group delay variation, revealing high potential on wideband amplifier implementation. In Section 2, the transfer function of the proposed amplifier, derived from the Y-parameters, is applied to design the feedback loop for synthesizing the group delay. A K-band CMOS prototype is designed based on the proposed architecture. Section 3 reports the theoretical and the measured results of the prototype to confirm the feasibility of the proposed design methodology. Both simulations and measurements show that the amplifier gain is 11 ± 0.4 dB from 22 GHz to 27 GHz. The measured maximum and minimum group delays are 65 and 77 ps, indicating ±6 ps variation. The measured NF is lower than 5.5 dB from 22 GHz to 27 GHz. From 21 to 27 GHz, the measured IP1dB and IIP3 are higher than −9.2 and +4.2 dBm between 21 GHz and 27 GHz, respectively. Section 4 concludes the paper.

2 Cascode amplifier with dual inductive feedbacks

Fig. 2(a) shows the schematic of the proposed cascode amplifier. The TLs of $T_1$ and $T_5$ form two individual inductive feedback loops in the common source (CS) and the common gate (CG) stages, respectively. $C_{B1}$ and $C_{B2}$ are the DC-block capacitors to isolate the DC signals in the feedback loops. Comparing to the reported prototypes, the proposed amplifier has two major differences. First, the proposed inductive feedback, eliminating the additional resistor shown in Fig. 7 of [4], only use the TL to realize the feedback loop. Second, the proposed design, removing the resistor at the output of the amplifier in [4, 5, 6, 7], uses only TL of $T_4$ for the output matching. TL of $T_2$ performs the complex impedance matching between the CS and CG amplifiers. TL of $T_3$ and $R_{b1}$ creates the inductive peaking to boost the amplifier gain. $R_{b2}$ is used to isolate the input signal from the biasing voltage on the gate terminal of $M_1$. To derive the transfer function of the proposed
amplifier, the hybrid-π model shown in Fig. 2(b) is applied to calculate the equivalent Y-parameter represented by

$$Y \cong \begin{bmatrix} \frac{s \cdot (C_{gs} + C_{gd}) + Y_f}{g_m - s \cdot C_{gd} - Y_f} & -s \cdot C_{gd} - Y_f \\ s \cdot (C_{gs} + C_{gd}) + Y_f & \frac{s \cdot (C_{gd} + C_{ds}) + Y_f}{s \cdot (C_{gs} + C_{gd}) + Y_f} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}, \quad (1)$$

where $Y_f$ is the equivalent admittance of the TL of $T_1$ connected with the capacitor of $C_{B1}$. $C_{B1}$ has a capacitance higher than 0.72 pF, and can be neglected during the calculation. Thus, $Y_f$ can be simplified by

$$Y_f \cong \frac{1}{s \cdot (Z_0 \cdot l/v_g)} = \frac{1}{s \cdot L_{eff}}, \quad (2)$$

where $L_{eff}$ represents the effective inductance of the feedback loop in the CS amplifier. $v_g$ is the wave velocity in TL of $T_1$. The transfer function of the CS amplifier, equal to the ratio of the output voltage to the input voltage, can be represented by

$$H = \frac{v_{out}}{v_i} = -\frac{y_{21}}{y_{22} + Y_L} \cdot \frac{1}{1 + Y_{in1} \cdot Z_S}, \quad (3)$$

where $y_{21}, y_{22}$ are the parameters in (1). $Y_L$ represents the input admittance of the CG amplifier at the reference plane in Fig. 2(a). $Z_S$ is the equivalent impedance of the $R_S$ connected with $C_1$. As shown in Fig. 2(a), $Y_{in1}$ can be expressed by (4).

$$Y_{in1} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}. \quad (4)$$

Assuming $|Y_L| \ll |y_{12}y_{21}Z_S|$, and substituting (4) into (3), (3) can be in the form of a second-order all-pass function, represented by

$$H \cong \frac{s^2 \cdot C_{gd}L_{eff} - s \cdot g_mL_{eff} + 1}{s^2 \cdot C_{gd}L_{eff} + s \cdot g_mL_{eff} + 1}. \quad (5)$$

The group delay of the all-pass function in (5) can be expressed by

$$GD(\omega) \cong 2 \frac{\omega_n}{Q} \frac{\omega_n^2 + \omega^2}{(\omega_n^2 - \omega^2)^2 + \frac{\omega_n^2 \omega^2}{Q^2}} \quad (6)$$

where $\omega_n$ and $Q$ are equal to (7), and (8), respectively.

$$\omega_n^2 = \frac{1}{C_{gd}L_{eff}} \quad (7)$$

$$Q = \frac{1}{g_m} \sqrt{\frac{C_{gd}}{L_{eff}}} \quad (8)$$

(7), and (8) reveal that the transistor’s parameters, $g_m$ and $C_{gd}$, affect the group delay of the amplifier. $L_{eff}$ can provide more degree of freedom for the group delay syntheses. To validate the feasibilities of (7) and (8), the proposed amplifier in Fig. 2(a) is analyzed by using ADS2012™. The characteristic impedance of the $T_1$ and $T_5$, are designed as 66 Ω. The electrical length of $T_1$, and $T_5$ are defined by $\theta_{T_1}$, and $\theta_{T_5}$. Fig. 3 shows the simulated group delays of the proposed amplifier with different $\theta_{T_1}$ and $\theta_{T_5}$. $T_5$ is designed with a length of 56-degree at 24 GHz to sustain the assumption on $|Y_L|$ much smaller than $|y_{12}y_{21}Z_S|$. As show in Fig. 3(a), by
changing $\theta_{T_1}$ from 36° to 86-degree, the group delay variation has a minimum value of 7 ps from 22 GHz to 27 GHz, corresponding to 56-degree of $\theta_{T_1}$ at 24 GHz. Additionally, the group delay is also analyzed with different $\theta_{T_5}$. The curves in Fig. 3(b) show that the group delay variation is less than 10 ps from 22 GHz to 27 GHz when $\theta_{T_5}$ is more than 56-degree at 24 GHz. When $|Y_{21}|$ is much smaller than $|Y_{12}||Y_{21}|Z_5$, the CG amplifier has a little effect on the group delay variation. The simulated group delay without the feedbacks, as shown in Fig. 3, is about three times of the variation higher than the proposed designs. The comparisons theoretically confirm that the proposed inductive feedback loops can effectively minimize the group delay variations.

3 K-band CMOS prototype

A K-band amplifier design is fabricated in the 1P8M CMOS 0.13 µm foundry. Fig. 4(a) shows that the prototype is in a chip area of 320 µm $\times$ 380 µm excluding testing pads. All the TLs in Fig. 2(a) are realized by the on-chip complementary-conducting-strip TL (CCS-TL) [10]. Fig. 4(b) shows the comparison between the measured and simulated two-port scattering parameters. The difference between the simulated gain and the measured gain is less than 2 dB from 21 to 27 GHz. In Fig. 5(a), the measured group delay variation is $71 \pm 6$ ps from 22 to 27 GHz. In
Fig. 5(b), the measured minimum and maximum NFs are 4.7 and 5.5 dB at 24 and 27 GHz, respectively. Fig. 6 summarizes the measured linearity and the stability of the prototype. In Fig. 6(a), the IP1dB and IIP3 are higher than −9.2 and +4.2 dBm between 21 GHz and 27 GHz, respectively. In the Fig. 6(b), the K-factor, μ, and μ′ of the proposed amplifier, extracted from the measured two-port scattering parameters shown in Fig. 4(b) with the formulas in the chapter three of the textbook [11], and [12], are greater than one from 21 GHz to 27 GHz, confirming the amplifier in stable.

Fig. 5. Measured and simulated: (a) the group delays and (b) the noise figures of the prototype in Fig. 4(a).

Fig. 6. Measured linearity and stability of the prototype in Fig. 4: (a) IP1dB and IIP3, (b) Stability factors.

4 Conclusion

The cascode amplifier with the TL feedbacks is proposed to demonstrate the amplifier implementation with low group delay variation. The simulations validate that the derived second-order all-pass function can be applied to synthesize the group delay. A CMOS prototype is experimentally validated to prove the feasibility of the proposed architecture on minimizing the group delay variation without scarifying the gain and bandwidth of the amplifier.

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