Thermal Effect on Dynamic $R_{\text{on}}$ Degradation of p-GaN AlGaN/GaN HEMTs on SiC Substrates

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Abstract In this work, the thermal effect in the dynamic on-resistance ($R_{\text{on}}$) degradation of normally-off p-GaN AlGaN/GaN HEMTs on SiC substrates has been analyzed using pulse-mode voltage stress. Compare to the significant degradation characteristics of GaN-on-Si HEMTs, a suppressed dynamic $R_{\text{on}}$ degradation is achieved in GaN-on-SiC due to higher thermal boundary conduction with less ionized acceptor-like buffer traps. Different electrical characteristics have been discussed to reveal the traps mechanisms related to thermal effect. Finally, two-dimension device simulation has been carried out to probe the physical insight into the thermal effect on the dynamic $R_{\text{on}}$ degradation.

key words: Buffer-traps; Dynamic $R_{\text{on}}$ degradation; AlGaN/GaN HEMTs; Pulse-mode Stress; Substrate; Temperature

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

In recent years, the properties of wide-bandgap (WBG) materials, especially Gallium Nitride (GaN), have gained a lot of attention for high-power, high-frequency, and high-temperature application in the power and microwave range, because of large bandgap, high breakdown electric field, and high mobility two-dimension electron gas (2DEG) [1-5]. A p-type doped GaN layer is covered locally under the gate in order to achieve enough high threshold voltage with a low specific on-resistance [6-10]. However, the capabilities of a full integrated GaN power electronics are still limited by several reliability issues when GaN HEMTs are operated between kHz to MHz switching frequencies [11-16].

On the one hand, several trapping mechanisms responsible for dynamic $R_{\text{on}}$ degradation have been investigated, relating to surface hot electron injection and buffer traps mechanisms [12, 14]. These traps can be generated in a variety of ways, starting from the epitaxy with lattice defects like vacancies, dislocations, or impurities. On the other hand, the high-temperature resistance of GaN materials determines that AlGaN/GaN HEMTs are often used in high-temperature environments [17-19]. Therefore, it is necessary to study the reliability of devices during high-temperature operation. Particularly, there are two different substrates existing in nowadays GaN HEMTs. GaN-on-Si HEMTs, which are mainly applied in commercial microwave applications, show the advantages with a perfect material match between GaN and SiC substrate and a higher efficiency compare to that of GaN-on-Si HEMTs. However, more discussion about the reliability characteristics of GaN-on-SiC HEMTs is needed under harsh environments.

In this paper, we systematically investigate the impact of temperature on dynamic $R_{\text{on}}$ degradation for the GaN HEMTs on SiC substrate. The insight of buffer traps mechanisms related to temperature and electrical parameters has been discussed experimentally. The numerical simulations accounting for different temperatures are carried out to prove the physical insight into dynamic $R_{\text{on}}$ degradation due to trap interaction with pulse-mode stress.

2. Devices and Stress Methods

Devices examined in this work are normally-off AlGaN/GaN stack structures on a Silicon Carbide substrate fabricated based on standard process. The schematic of the fabricated GaN-on-SiC cross-section is shown in Fig. 1. And The basic parameter of fabricated GaN-on-SiC HEMTs is listed in Table 1.

![Fig. 1. The schematic of normally-off GaN-on-SiC HEMTs with $L_{\text{gs}}/L_{\text{g}}/L_{\text{gd}} = 1/1/2\mu m$ and $100\mu m$ gate width.](Image)

Table 1 Measured Devices Parameter.

| Devices | Substrate | BV  | $V_{th}$ | $R_{\text{on}}$ |
|---------|-----------|-----|----------|----------------|
| Devices as Fig. 1. | SiC | 154V | 1.6V | 42 mΩ |
In order to mimic the power converter circuit operation environment, the pulse-mode stress measurement has been adopted to evaluate the dynamic $R_{on}$ degradation. Fig. 2 shows the waveforms of an on-the-fly pulse-mode voltage stress measurement [20]. Both drain voltage and gate voltage waveforms were biased by using the two ultra-fast pulse I-V PMU modules with a Keithley 4200A Semiconductor Characterization System. A temperature control chuck is mounted in the probe station to bias the devices with different temperatures.

3. Experimental Results

In view of power electronics circuits, such as Boost converter and Buck converter, the GaN HEMTs are subjected to pulse stress from the off-state to on-state which is similar to our experimental conditions discussed early. In our experiments, the dynamic $R_{on}$ is extracted during each cycle of pulse-mode stress with the temperature range from 300K to 450K. And in order to reveal the relationship between buffer trap mechanisms and thermal effects, the dynamic resistance degradation is analyzed as a function of off-state drain voltage, and on-stage gate voltage.

The dynamic $R_{on}$ degradation of GaN-on-SiC HEMTs under different ambient temperature is shown in Fig. 3. It can be seen instinctively from Fig. 3 that, the dynamic $R_{on}$ degradation of GaN-on-SiC HEMTs continuously increased with the increasing pulse-mode stress time. And with the increased temperature from 300K to 450K, the peak dynamic $R_{on}$ degradation at 3100s stress time increased from 1.19% to 9.98%, which suggests the dynamic $R_{on}$ has a strong dependence on the temperature. Compare to the dynamic $R_{on}$ degradation as reference [16], a released dynamic $R_{on}$ characteristic is shown in GaN-on-SiC HEMTs under high temperature operation. The main reason was less acceptor-like buffer traps were ionized with higher temperature distribution in GaN-on-SiC HEMTs.

According to previous research results, the dynamic $R_{on}$ degradation is believed originates from the ionized acceptor-like buffer traps, which is temperature-dependent. And as the SiC has higher thermal conduction compare to Si, the GaN buffer layer in the GaN-on-SiC HEMTs will suffer lower temperatures under the same operating conditions [22]. The lower temperature in GaN buffer will trigger less ionized acceptor-like traps, where the hole-emission from the ionized acceptor-like traps will deplete the 2DEG with decreased dynamic $R_{on}$ degradation in GaN-on-SiC HEMTs [12].

In order to further investigate the traps mechanisms related to surface and buffer traps, different electrical parameters in the pulse-mode stress are discussed. Off-state drain voltage stress plays an important role in the degradation of dynamic on-resistance subjected to DC stress [10]. In this work, the relationship between dynamic resistance degradation and $V_{DTH}$ of GaN-on-SiC are illustrated. The GaN HEMTs under test were stressed for different off-state drain voltages and on-state gate voltages. According to the safe operation area (SOA) [23] of 60V GaN HEMTs, the stress level between 10V and 50 V is sufficient enough. The normalized dynamic $R_{on}$ degradation of GaN-on-SiC HEMTs is from 1.77% to 9.59% with an increased off-state drain voltage to 50V after 3100 seconds of pulse-mode stress at $T$=400K (see Fig. 4 for detail). The increased degradation characteristics in both devices indicate the off-state drain voltage plays an important role in the dynamic $R_{on}$ degradation. The presence of a Carbon-related acceptor-like traps with the GaN buffer layer will emit holes to deplete the 2DEG with increased dynamic $R_{on}$ degradation.

In the power switch applications, one of the most important circuits is the gate driver. For different applications, the gate driver current varies significantly [24]. This leads us to examine the gate voltage effect on the dynamic $R_{on}$ degradation. In our experiments, the on-state

![Fig. 2. On-the-fly measurement stress conditions.](image1)

![Fig. 3. The dynamic $R_{on}$ degradation under the different temperature of GaN-on-SiC HEMTs. The device was stressed under $V_{DTH}$ = 40V, $V_{GSH}$ = 1V, $V_{GSL}$ = 6V, and $V_{DOL}$ = 0V with a pulse width of 3.1µs and duty cycle of 67% after 3100s of pulse stress.](image2)

![Fig. 4. The dynamic $R_{on}$ degradation under different off-state drain voltage at $T$ = 400K of GaN-on-SiC HEMTs. The device was stressed under $V_{DOL}$ = 1V, $V_{DOL}$ = 6V, and $V_{DOL}$ = 0V with a pulse width of 3.1µs and duty cycle of 67% after 3100s of pulse stress.](image3)
The normalized dynamic $R_{on}$ in GaN-on-SiC HEMTs is degraded from 1.85% to 4.95% when $V_{GH}$ is increased from 2 V to 8 V during pulse stress at $T=400K$. Compare to the significant impact on dynamic $R_{on}$ degradation from off-state drain voltage, the increased amplify from the increased on-state gate voltage is much less. As previously studied [12], the surface traps ionized from on-state gate voltage play an important role in the dynamic $R_{on}$ degradation. The results also imply the trap mechanisms induced by the on-state gate voltage is self-heating dependent. Based on the above experimental data, the dynamic $R_{on}$ in normally-off GaN HEMTs at a high temperature can be caused by temperature-variations of Fermi levels due to the increase in intrinsic carrier concentration, ionization of deeper defect energy levels in the p-GaN layer (residual donors) and surface donor-like traps.

4. Sentaurus Device Simulation Results

The Sentaurus two-dimension (2D) simulation is used to probe the physical insight into the trap mechanism relating to observed dynamic resistance degradation from the experiment. The AlGaN/GaN HEMTs on SiC substrate shown in Figure 1 are examined in simulation. The source and drain contacts are implemented using heavily doped GaN to form ohmic contacts. High-field mobility saturation model and inverse piezoelectric effect are adjusted to improve the simulation accuracy and consistent with the real situation. The polarization scale parameter with 0.29 has been applied to be consistent with the measured experimental data [12]. Shockley-Read-Hall and Fermi-Dirac statistics are enabled to simulate the trapping and detrapping mechanisms under different voltage stresses [26]. The self-heating effect including the lattice temperature model and electron/hole thermal model is enabled to monitor possible hole/electron emission processes [27]. The buffer layer is set as a low mole-fraction AlGaN to mimic graded buffer layers in fabrication. In the device simulation, Gaussian distribution with the peak density of $10^{19} \text{ cm}^{-3}$ shallow compensating donors in the Carbon-doping buffer layer is implemented [28]. As shown in [29], trapping phenomena in the Carbon-doped buffer layer can be reproduced by adopting deep-level acceptor-like traps with a concentration almost two orders of magnitude lower than that at the nominal Carbon doping level. Therefore, low-density deep-level ($E_C - 0.9 \text{ eV}$) acceptor-like traps ($10^{15} \text{ cm}^{-3}$) with deeper-level capture cross-section area of $10^{-15} \text{ cm}^2$ are applied to the buffer layer. In order to verify the trap effect, the mixed-mode transient simulation with different pulse voltage stresses is simulated. The key parameters used in the 2D simulation are listed in Table II. units for each quantity in an equation.

The lattice temperature of GaN-on-SiC HEMTs under different ambient is first simulated as shown in Fig. 6. With the increased ambient temperature, the higher peak lattice temperate is observed at the gate contact edge close to the drain side in GaN-on-SiC HEMTs. And the high lattice temperature region will extend to the buffer layer with the increased ambient temperature, which is related to ionization of acceptor-like buffer traps. The results verify that the increase in intrinsic carrier concentration and ionization of acceptor-like traps play an important role in severe dynamic $R_{on}$ degradation at high temperatures.
observed dynamic Ron degradation in experiment early, with respect to an increase in temperature are consistent with in GaN-SiC HEMTs. This simulated buffer traps movement of the hole emission from the acceptor-like traps is increased the increased ambient temperature, meaning that the density the dominant role in the dynamic Ron degradation, are highly directly observed by the experiment early.

The electron density as a function of temperature under pulse-mode stress successfully reflects the self-heating effect with the higher thermal conduction substrate material. Finally, trap physical mechanisms, like lattice temperature, ionization acceptor-like traps, and electron density under different temperatures, have been demonstrated by TCAD mixed-mode device simulation.

Fig. 7. The simulated trap occupation distribution (b) GaN-on-SiC HEMTs under different ambient temperatures. The device was simulated under V_{DH} = 40V, V_{DL} = 1V, V_{GH} = 6V, and V_{GL} = 0V with a pulse width of 3.1µs and duty cycle of 67%.

Fig. 8. The simulated electron density distribution GaN-on-SiC HEMTs under different ambient temperatures. The device was simulated under V_{DH} = 40V, V_{DL} = 1V, V_{GH} = 6V, and V_{GL} = 0V with a pulse width of 3.1µs and duty cycle of 67%.

Using the above-mentioned physical models in device simulation, the simulated acceptor-like trap occupation densities in the buffer layer after 3100s of voltage stress versus different ambient temperature are shown in Fig. 7. All the simulations are subjected to pulse-mode stress with a pulse width of 3.1µs. The trap occupation refers to the ionization rate which indicates the hole emission process from the acceptor-like traps. It can be seen in Fig. 7 that the region of the acceptor-like trap occupation is extending with the increased ambient temperature, meaning that the density of the hole emission from the acceptor-like traps is increased in GaN-SiC HEMTs. This simulated buffer traps movement with respect to an increase in temperature are consistent with observed dynamic Ron degradation in experiment early, which also demonstrate the acceptor-like traps is dependent on the self-heating as they have similar distribution area.

To examine the simulation results further, the electron density of the 2DEG under temperature in pulse-mode stress is analyzed in Fig. 8. Since the trap emission model [30] may not be accurate enough, we add measured interface trap distributions at the GaN cap/Nitride interface to mimic the current degradation subjected to different pulse-mode stress conditions based on the [12]. Although the decreased electron density is observed with the increased ambient temperature, the higher electron density is extracted in GaN-on-SiC HEMTs. The electron density as a function of temperature under pulse-mode stress successfully reflects the trap effect directly observed by the experiment early.

5. Conclusion

A detailed analysis of the correlation between thermal effect and dynamic Ron degradation in AlGaN/GaN HEMTs on SiC substrate has been studied by using pulse-mode stress and TCAD simulation. The acceptor-like traps, which play the dominant role in the dynamic Ron degradation, are highly dependent on the temperature. And robustness reliability characteristics with relaxed dynamic Ron degradation are observed in GaN-on-SiC HEMTs by suppressing the self-heating effect with the higher thermal conduction substrate material. Finally, trap physical mechanisms, like lattice temperature, ionization acceptor-like traps, and electron density under different temperatures, have been demonstrated by TCAD mixed-mode device simulation.

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