Comparative performance analysis based short channel effects for TG Nano FinFETs

Zohmingmawia Renthlei, Rudra Sankar Dhar* and Swagat Nanda

Department of Electronics and Communication Engineering, National Institute of Technology Mizo, Aizawl, Mizoram, 796012, India

E-mail :* rdhar@uwaterloo.ca

Abstract: The scaling down of CMOS technology has been carried out successfully following the Moore’s law for the last five decades. One of the main challenges for a nano scaled device are the Short Channel Effects (SCEs). It has begun to reach the limit of Silicon material; hence high-k dielectric materials are introduced to challenge the SCEs. Particularly HfO2 is used for this study. The high k dielectric material has been compared with the well-known SiO2 in a 3D SOI Tri-Gate (TG) FinFET device which is modelled and simulated in SILVACO TCAD tools. TG SOI FinFETs having 22nm, 14nm and 10 nm channel lengths are developed. Since the device are in nano regime, short channel device parameters such as threshold voltage, subthreshold swing (SS), Ion current, Ioff current, Ion/Ioff ratio and DIBL are analysed for the two materials developed in TG SOI FinFET. The comparison shows that high k dielectric materials shows better results in reducing current leakage and drain induced barrier leakage than that of SiO2.

Keywords: TG SOI FinFET, SCEs, High k dielectric materials, SILVACO.

1. INTRODUCTION

The efficient miniaturization of a transistor has been one of the most important topics to integrate a greater number of electrical components in a single chip. The MOSFET, being one of the most iconic devices for the past few decades, has started to reach its limit when it comes to nano-regime. The drastic scaling of MOSFET device has been made possible until recently when the device dimensions has reached below 100nm. These devices are called nanotechnology devices [1]. Such devices require new materials or new designs to cope up with the Moore’s law. The channel length when reduced beyond sub-32nm, the MOSFET performance shows degradation in low power application due to SCEs such as degradation of subthreshold swing, Gate Induced Drain Leakage (GIDL), punch-through and Drain induced barrier lowering (DIBL) [2]. Researchers around the world have been trying different ways to enhance the performance of MOSFETs in nanoscale. Most of their technique includes reduction in gate oxide thickness, increasing the doping concentration, indulging high-k dielectric materials, introducing dual material gate, pocket implantation, lateral channel engineering, Silicon-on-Insulator (SOI) and strained silicon technology [3-5].

To integrate as many components as possible in a microprocessor chip, a system called Silicon on insulator (SOI) has been used which enable more speed, better current drive and reduction in power consumption in the circuit while scaling down the device.
Since the conventional MOSFET has come to the limit in nano regime, there is a need to develop a new design of a transistor. Among the different variety of device structure that are developed, a multigate device has been one of the best. FinFET has been one of the most promising technology to carry out future nanoscale CMOS technology. Among the multigate FinFETs that are developed, Tri-gate (TG) FinFET are very promising because a greater number of gates has better control of the gate current. The analytical study of FinFET is a current topic of research in big companies like TSMC, Samsung and Intel aiming to create the most efficient microprocessors.

Apart from the design model of the device, for an efficient control of the short channel effects, the relation between the channel length and the thickness of the insulator must be kept at minimum state [6]. But reducing the thickness of the insulator increases the gate leakage current. For SiO₂, when the thickness reaches down to 2 nm, there is a sudden rise in the gate leakage current [7] which is least desirable. Because of this reason, the use of High-k materials has been introduced since it has thicker insulator for the same control of the gate current which results in reducing the current leakage [8]. The high k dielectric material increases the ON current and the gate capacitance without interfering the leakage effects [9]. Furthermore, the choice of the high k dielectric material has been specified. HfO₂ is the considered the most favourable high k dielectric material for gate oxide as it shows the best results while encountering short channel effects like DIBL, Subthreshold swings, leakage current and Ion/Ioff ratio [10].

Based on the specification described from the above statements, the characteristics of SiO₂ and HfO₂ are compared using SILVACO TCAD tools based on the same TG SOI FinFET device considering a promising device for future nano regime semiconductor device.

2. DEVICE STRUCTURE

In this work, the TG SOI FinFET structure using two different gate oxides have been simulated whose parameters are provided in table 1. The modelling of the device is done using SILVACO Atlas simulator and the simulation is carried out using SILVACO TCAD tools. The model used for simulation includes Shockley-Read-Hall (SRH) model, Lombardi CVT model, Auger model and Band gap narrowing model. The 3–D schematic of the simulated SOI FinFET is shown in figure 1.
Two different materials are used as gate oxide. The electrical characteristics of the two materials are compared between SiO$_2$ and HfO$_2$ and their gate oxide thickness are considered for the same Equivalent Oxide Thickness (EOT) which can be expressed as (1) [11]

$$EOT = T_{high} \cdot \frac{\varepsilon_{SiO_2}}{k_{high}} - T_{low} \cdot \frac{\varepsilon_{HfO_2}}{k_{low}}$$ (1)

where $\varepsilon$ stands for dielectric constant and $T$ stands for thickness of the material used. The different parameters of the considered is given in table 1.

| Notation | Description                  | Dimension                  |
|----------|------------------------------|----------------------------|
| L$_D$, L$_S$ | Length of Drain and source   | 11nm                       |
| L$_G$    | Length of channel            | 22nm, 14nm and 10nm        |
| T$_{ox}$ | Thickness of oxide           | 1nm                        |
| T$_{fin}$ | Thickness of Fin             | 10nm                       |
| H$_{fin}$ | Height of Fin                | 10nm                       |
| T$_{box}$ | Thickness of Buried oxide    | 50nm                       |
| T$_{sub}$ | Thickness of silicon substrate| 30nm                      |
| N$_a$    | Doping of channel            | $10^{15}$ cm$^{-3}$        |
| N$_d$    | Doping of Drain/Source       | $10^{18}$ cm$^{-3}$        |

Different TG FinFETs are simulated with two different gate oxide namely SiO$_2$ ($k=3.9$) and HfO$_2$ ($k=25$) having EOT of 1nm. The channel lengths are varied between 22 nm, 14 nm and 10 nm for both the gate oxides. The silicon is grown on top of buried oxide having thickness of 50 nm and substrate having 30 nm thickness. The length of the source as well as drain are kept at 11 nm in all the simulated devices. The length and the width of the fin of the FinFET is also fixed at 10 nm for all the simulated device. The doping concentration of the channel region is taken to be $10^{15}$ cm$^{-3}$ and the source and drain are doped at $10^{18}$ cm$^{-3}$.

3. RESULTS AND DISCUSSIONS.

The simulation and the modelling of the 3D TG FinFET has been done using Silvaco TCAD tools for two different gate oxides. The simulation is first done using SiO$_2$ as the gate oxide material for different gate lengths. In the second part, SiO$_2$ is replaced with HfO$_2$ and simulated with different gate lengths. The two characteristics are then compared taking an EOT of 1nm on the same TG FinFET design parameters [11]. The I$_D$–V$_{GS}$ characteristics in the linear scale has been plotted in figure 2, and the characteristics in the logarithmic scale for the same TG FinFET structure is depicted in figure 3 with different channel lengths. The gate voltage is varied from 0 to 1 V taking 10 mV step for each drain-source voltage. The threshold voltages of the device using SiO$_2$ as gate oxide is 0.24 V, 0.23 V and 0.22 V and 0.30 V, 0.29 V and 0.28 V for the device using HfO$_2$ as gate oxide for 22 nm, 14 nm and 10 nm gate length respectively at V$_{DS}$ = 0.1V which is compared in figure 4. This shows that as we keep on scaling down the channel length, the threshold voltage also reduces. Comparison of the two devices also depicts higher threshold voltage using HfO$_2$. 


The max current or the on current can be determined from the linear scale plot of the $I_D-V_{GS}$ characteristics. The on current, $I_{on}$, for all the simulated devices are found to vary slightly around 1.5 $\mu A/\mu m$ at $V_{GS} = 0.1V$ as shown in figure 5. As the gate voltage increases, there is a sudden rise in the on current because of the rise in drain voltage.
The logarithmic scale of $I_D$–$V_{GS}$ characteristics presents an excellent analysis of the leakage currents, subthreshold swing (SS) and DIBL of the simulated devices. When the channel length shrinks, the capacitance between the channel and the source/drain changes because of the potential given on the channel. The $I_{off}$ current can be calculated using (2) [12]:

$$I_{off}(nA) = \frac{100W}{L} 10^{-\frac{V_{th}}{SS}}$$

(2)

where $L$ and $W$ are the length and width of the device channel respectively and SS and $V_{th}$ are the subthreshold swing and threshold voltage respectively. The comparison graph of the leakage current has been plotted in figure 6. For 22 nm gate length, the device with gate dielectric as SiO$_2$ shows an $I_{off}$ current of 2.91 pA/µm whereas the device with gate dielectric as HfO$_2$ shows an $I_{off}$ current of 0.32 pA/µm only. Similarly, for 14 nm and 10 nm devices also, the leakage currents are 8.92 pA/µm and 29.76 pA/µm for the FinFET with SiO$_2$ gate dielectric and 1.11 and 4.1 pA/µm for HfO$_2$ gate dielectric.

![Figure 6. Variation of Off Current, $I_{off}$, of the devices using SiO$_2$ and HfO$_2$ as gate dielectric material.](image)

Now that the values of $I_{on}$ and $I_{off}$ have been determined, the comparison of $I_{on}/I_{off}$ current ratio has been plotted in figure 7. Although the $I_{on}$ values are similar for all the devices, there is a big variation in the $I_{off}$ currents in pico-amperes which gives peculiar variation in the $I_{on}/I_{off}$ current ratio. The $I_{on}/I_{off}$ current ratios are approximately 9, 8 and 7 times more for HfO$_2$ devices than SiO$_2$ devices for 22 nm, 14 nm and 10 nm gate length FinFETs respectively which interprets that devices with HfO$_2$ as gate dielectric materials provide better switching thereby decreasing short channel effects.

But in this work, as the channel length decreases, the ratio also decreases which reduce the switching capability of the transistors. As the channel length decreases, the $I_{off}$ increases almost exponentially which leads to decrease in $I_{on}/I_{off}$ current ratio. But comparatively, HfO$_2$ has higher ratio and shows promising results which means that HfO$_2$ has lesser gate leakage between the two which is desirable for a transistor. This is due to the fact that the subthreshold leakage of SiO$_2$ is larger than that of HfO$_2$. 

Figure 7. Comparison of $I_{on}/I_{off}$ ratios of the devices using SiO$_2$ and HfO$_2$ as gate dielectric material.

The subthreshold swing is one of the major factors responsible for the calculation of leakage current. As the device channel length is decreased, the SS also increases. The calculation of the subthreshold swing can be expressed as [13]:

$$SS \left( \frac{mV}{\text{decade}} \right) = \frac{dV_{gs}}{d(\log_{10}I_{DS})}$$  

where $dV_{gs}$ is the change in gate voltage and $d(\log_{10}I_{DS})$ is the change in the drain current taken in logarithmic scale.

The SS of the devices with HfO$_2$ as the gate dielectric material are only marginally greater than their counterparts with SiO$_2$ as the gate dielectric material for 22 nm, 14 nm and 10 nm channel length devices as depicted in figure 8.

Figure 8. Subthreshold Swing of the devices using SiO$_2$ and HfO$_2$ as gate dielectric material.

The output characteristics is plotted in figure 9 where the drain characteristics has been analysed at a given gate voltage for the same TG FinFETs with the two gate oxides. Figure 9 shows the $I_D$–$V_{GS}$ characteristics of the TG FinFET with different gate oxides material varying their channel length. The gate to source voltage is constant at 0.5V. It is observed that the saturation region is obtained rapidly for all the devices. The saturation current is obtained at a lower current for HfO$_2$ in comparison with SiO$_2$ which shows that there is an enhancement in the device.
Figure 9. $I_D-V_{DS}$ characteristics of the TG FinFET using SiO$_2$ and HfO$_2$ as gate dielectric material.

Another important aspect that can be considered for the comparison of the TG FinFET simulated for all respect materials and varied gate length is DIBL. It is one of the short channel effects which is defined as the ratio of the variation in threshold voltages when the drain voltage changes from a low value to a high value, given in the relation:

$$\text{DIBL (mV/V)} = \frac{\Delta V_{th}}{\Delta V_{DS}}$$

(4)

where $\Delta V_{th}$ is the variation in the threshold voltage and $\Delta V_{DS}$ is the change in the drain to source voltage.

Figure 10. Comparison of DIBL of the devices using SiO$_2$ and HfO$_2$ as gate dielectric material

The DIBL comparison has been plotted in figure 10 where HfO$_2$ shows better result except for the 22nm device. As the channel length decreases, due to short channel effects, the leakage of the device increases. SiO$_2$ has greater leakage than that of HfO$_2$.

4. CONCLUSIONS

A Triple Gate SOI FinFET with three varied channel lengths has been developed and simulated using Silvaco TCAD tools. High k dielectric material HfO$_2$ is compared with SiO$_2$ which are used as gate
oxide in all the devices. The thickness of the gate oxide is kept EOT of 1 nm of SiO₂. Different parameters of SCEs are analytically observed and compared for different channel length devices. As the device was scaled down, the short channel effects degraded. The I_D–V_GS and I_D–V_DS are plotted from which the threshold voltage V_th, I_off current, I_on current and I_on/I_off current ratio are compared for the two dielectric materials in which improvements are observed for HfO₂ dielectric material. Similarly, subthreshold swing and DIBL also shows improvement in HfO₂ dielectric material. So, we can conclude that HfO₂ is the better dielectric material for the future nanoscale TG SOI FinFET technology even beyond 14nm devices.

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