CAPACITOR BALANCING FOR MMCC-SSBC TOPOLOGY WITH NEGATIVE SEQUENCE CURRENT INJECTION METHOD

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Abstract

This paper investigates the negative sequence current injection method for balancing the capacitor voltage in cascaded H-bridge D-STATCOM (MMCC-SSBC). Though the cascaded H-bridge D-STATCOM has the advantage of having less number of circuit components compared to Diode clamped and flying capacitor clamped D-STATCOM but the capacitor voltage balancing between the phase clusters is a main issue. Considering this problem the negative sequence current injection method is investigated under normal working condition of D-STATCOM as well as under large unbalance in the supply voltage. The performance of this technique is investigated by using MATLAB-SIMULINK modeling.

Keywords: D-STATCOM, Capacitor balancing, Multi-level converter, Cascaded H-bridge multilevel converter.

I. Introduction

The cascaded H-bridge multilevel converter consists of series connected H-bridge cells, here a 7 level H-bridge D-STATCOM is considered with H-bridge cell is having an isolated DC capacitor. Even though it is not an active source but voltage balancing of DC capacitor in individual H-bridge and total DC cluster is needed for the following reasons

1. For protection of semi-conductor switches from high voltage in case of faults or may be of large unbalance in source voltage.
2. For providing adequate compensation currents for unbalanced loads.

Several methods of capacitor voltage balancing techniques are exist in literature[VI][VII][XI][IV][XV]. The practical implementation of a 154 KV, 50 MVAR of 21 level cascaded multilevel converter [I] have used the selective swamping algorithm for voltage equalization of DC capacitors. One of the method proposed can independently control the active power flow between the individual DC and for the phase cluster but unbalance in the power system voltage is not taken into consideration. The average power balancing APB proposed[XIII] can control both the reactive power compensation and DC capacitor voltage balancing even under voltage sags. The capacitor voltage balancing method by negative sequence current injection is proposed[XII] for hybrid cascaded H-bridge topology and the performance is...
investigated under asymmetrical faults. The drawback of selective swamping algorithm is the need of look up table, whereas the average power balancing scheme needs one cycle for calculation of average power.

In order to design the control strategy for power electronic based systems the instantaneous values are to be considered for making the decision. Here the instantaneous value of source voltage and load currents are taken into consideration for designing the control strategy i.e negative sequence current injection method[VI] and the control strategy is modified as current control strategy with the help of synchronous frame theory[VIII]. For the designed control strategy performance is investigated for unbalanced nonlinear load and also under large unbalance in the source voltage.

II. Circuit configuration and control strategy

The advantage of multilevel is to eliminate the bulky line frequency transformers. The Cascaded H -bridge D-STATCOM circuit configuration is shown in Fig 1 was proposed in [II] and renamed under modular multilevel converter (MMCC) family as a single star -bridge cells (SSBC) [III]. In each H -bridge and for every leg the switches are triggered complementarily such that the three possible outputs obtained are + V dc, 0, - V dc (for the capacitor reference voltage V dc ) leading to Two nonzero voltages and one Zero voltage. If capacitor voltages are the same (V dc) in three H-bridges in a particular phase, then the output of each phase can assume seven levels (six non- zero voltages and one zero voltage). Total 64 possible switch combinations and the corresponding voltage levels are shown in table 1. From Fig 1 the voltage \( v_{xn} \) can be found out from eq.(1)

\[
v_{xn} = v_{a1} + v_{a2} + v_{a3} \]

\[
v_{xn} = [(s_{1a} - s_{3a}) + (s_{2a} - s_{3a}) + (s_{3a} - s_{3a})]v_{dc}
\]

(1)

For the switch combination (S_{1a}, S_{3a}, S_{2a}, S_{3a}, S_{3a}, S_{3a})=(1,0,1,0,1,0) the voltage \( v_{xn} \) can be find from eq.(1) is 3V dc.

Table 1 Switch combinations and its corresponding voltage levels

| Switch combinations \((S_{1a}, S_{3a}, S_{2a}, S_{3a}, S_{3a}, S_{3a})\) | No of combinations | Voltage\((v_{xn})/\) Level |
|---|---|---|
| (1,0,1,0,1,0) | 1 | 3V dc |
| (0,1,0,1,0,1) | 1 | -3V dc |
| (0,0,1,0,1,0)(1,0,0,0,1,0)(1,0,1,0,0,0)(1,0,1,0,1,1)(1,0,1,1,0,1) | 6 | 2V dc |
| (0,0,0,1,0,1)(0,1,0,0,1,0)(0,1,0,1,0,0)(0,1,0,1,1,1)(0,1,1,0,1,1) | 6 | -2V dc |
| (0,0,0,0,1,0)(0,0,1,0,1,0)(0,0,1,0,1,1)(0,0,1,1,0,0)(0,1,1,0,1,0) | 15 | V dc |

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\begin{align*}
(1,1,0,0,0) & (1,1,0,1,1) & (1,1,1,1,1) \\
(0,0,0,0,1) & (0,0,0,1,0) & (0,0,1,1,1) \\
(0,1,0,1,0) & (0,1,0,0,0) & (0,1,1,0,1) \\
(1,0,0,0,1) & (1,0,0,1,1) & (1,1,1,0,1) \\
(1,1,0,1,0) & (1,1,1,1,1) & (1,1,1,1,1) \\
(0,0,0,0,0) & (0,0,0,1,1) & (0,0,1,1,0) \\
(0,1,0,1,1) & (0,1,0,0,0) & (0,1,1,1,0) \\
(1,0,0,1,1) & (1,0,0,0,0) & (1,1,1,0,1) \\
(1,1,0,1,0) & (1,1,1,1,1) & (1,1,1,1,1) \\
15 & -V_{dc} & \\
20 & 0 & \\
\end{align*}

Fig 1 Cascaded H-bridge (MMCC-SSBC)
Two triangular carrier waves are required for each H-bridge in order to implement the level shifted PWM (LSPWM). Fig 2 consists of level shifted carries which are in phase with each other and a modulating signal taken as sine waves of peak value $v_m$ to show as to how gating pulses are generated. The uppermost and lowermost carrier pair in Fig 2 i.e $c_{r1+}$ & $c_{r1-}$ are used to generate gating pulses for switches $S_{11a}$ and $S_{13a}$ of H1a. The innermost carrier pair $c_{r3+}$ & $c_{r3-}$ generate the gating signals for $S_{31a}$ and $S_{33a}$ of H3a. The remaining carrier pair $c_{r2+}$ and $c_{r2-}$ are for $S_{21a}$ and $S_{23a}$ in H2a. For the carriers above the zero reference ($c_{r1+}$, $c_{r2+}$, and $c_{r3+}$), the switches $S_{11a}$, $S_{21a}$, and $S_{31a}$ are turned on when the modulating signal $v_m$ is higher than the corresponding carriers. For the carriers below the zero reference ($c_{r1-}$, $c_{r2-}$, and $c_{r3-}$), $S_{13a}$, $S_{23a}$, and $S_{33a}$ are switched on when the modulating signal $v_m$ is lower than the carrier waves. For lower switches in each leg of all the H-bridges are driven by a gating pulse which is complementary of upper switch gating pulse.

![Carrier &modulating signals](image)

**Fig 2 Level shifted carrier modulation (LSPWM)**

$$v_{dc_{ref}} = k \frac{V_{sa}}{N}$$

(2)

To control this capacitor voltage its sensed value is compared with the reference value as given in eq.(2). The DC capacitance and filter inductance are designed from [VIII][X][XIV].

Each phase is fed by a DC link voltage obtained from cluster of three capacitors. When D-STATCOM is injecting unbalanced currents, not only does the voltage of each capacitor vary from other but the voltage of each cluster also differs from other. A DC cluster balancing technique is used to balance the DC voltage in all the phases. The individual DC capacitor voltage unbalance is caused by uneven conduction of switching devices, which depends on the type of PWM technique used. Here a level shifted PWM technique is preferred which give rise to unequal
conduction of switches over to the rotation of carrier PWM in which all the switches of a H-bridge are conducted uniformly.

B. Reference current generator:

The main criteria is to compensate for harmonic and reactive power required by the unbalanced non-linear load. In this reference current generation, load currents are converted into d-q synchronous frame with the help of three phase locked loop. The nature of these currents will have oscillating and average component. The oscillating component is due to harmonics and the average component in d-axis current represents active power and that in q-axis current represents reactive power. The low pass filters are used to separate these components. The entire quadrature axis load current should be nullified. The resultant reference current generator is shown in Fig 3.

So the reference compensation currents for D-STATCOM on d-q synchronous frame are given by eq.(3)-(4).

\[ i_{cd}^* = -(i_d + i_{loss} + i_{nd}) \]  
\[ i_{cq}^* = -(i_q + i_{nq}) \]  

These currents are then converted back into abc quantities by using inverse transformation to obtained reference currents of D-STATCOM. A PWM current controller then forces actual currents to follow these reference currents.

Fig 3 Control strategy of D-STATCOM with negative sequence current injection method
C. Capacitor voltage balancing: The capacitor voltage balancing is crucial in order to provide the adequate compensation. The capacitor voltage balancing is divided into two categories individual capacitor voltage balancing and a cluster voltage balancing. The individual capacitor voltage balancing is sufficient for absorbing the balanced harmonics and reactive power of a non-linear load whereas the cluster voltage balancing is required in case of compensation for unbalanced non-linear load or unbalanced source.

Ci. Individual DC capacitor voltage balance: The technique used for individual DC capacitor voltage balancing is shown in Fig 4. The individual error between the reference capacitor voltage and the actual capacitor voltage (filtered by a low pass filter) after being passed to a PI controllers is summed up to obtain $i_{loss}$ for each phase. The $i_{loss}$ components of all phases are added to get $i_{loss}$, which is then added to d axis current $i_d$ shown in Fig 3.

C.ii. DC capacitor cluster voltage balance: During compensation of unbalanced loads, a negative sequence current is injected by D-STATCOM. If the DC cluster voltages are not the same, the compensation capability of phases will be lowered. Therefore to ensure availability of compensation at all times, the DC cluster voltage in all the phases should be maintained constant. The negative sequence current injection method to balance the cluster voltages is shown in Fig 3. The negative sequence current which is to be injected are taken in proportion to the dc cluster voltages. These equations are represented in eq(5)-(7) below.

$$i_{a} = K(v_{a} \alpha(\theta) + v_{c} \alpha(\theta + 2\pi/3) + v_{c} \alpha(\theta - 2\pi/3))$$

$$i_{b} = K(v_{a} \alpha(\theta + 2\pi/3) + v_{c} \alpha(\theta - 2\pi/3) + v_{c} \alpha(\theta))$$

$$i_{c} = K(v_{a} \alpha(\theta - 2\pi/3) + v_{c} \alpha(\theta) + v_{c} \alpha(\theta + 2\pi/3))$$

Where the dc cluster voltage for phase-a can be found from eq.(8)
Similarly other cluster voltages can be found for $v_{cb}$ and $v_{cc}$. These equations from (5) - (7) when represented in dq frame are given by eq.(9).

\[
\begin{align*}
\frac{\dot{i}_{ad}}{\dot{i}_{dq}} &= \begin{pmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{pmatrix} \begin{pmatrix} v_{ca} \frac{(v_{cb} + v_{cc})}{2} \\ v_{cb} - v_{cb} \end{pmatrix} \\
&= K \begin{pmatrix} \sqrt{3}(v_{ca} - v_{cb})/2 \\
\end{pmatrix}
\end{align*}
\]

These $i_{ad}^*, i_{dq}^*$ contribute to correction when there is a deviation in DC cluster voltage and this information is processed in the control strategy of D-STATCOM shown in Fig 3.

**D. PWM current controller:** The PWM current controller can be implemented for particular a-phase is shown Fig 5. The error which is generated by subtracting the actual currents from reference currents is passed to a PI controller to give a modulating signal for a-phase. This modulating signal and the level shifted carriers are then used to generate the gating pulses for H-bridges as described in [XII]. Similarly, gating pulses for other phases are also generated.

**E. Design of components in D-STATCOM:**

The circuit diagram of D-STATCOM is shown in Fig 1. The values of coupling inductance and capacitance play an important role in the transient response of the system and for maintaining the instantaneous energy requirement of the system [I, VII, IX]-[XIV].

**DC capacitor for each H-bridge:** The design of dc capacitor is based on principle of conservation of energy. Whenever there is change in the load the voltage of the capacitor will fall or raise corresponding to increase and decrease of the load respectively. The instantaneous energy stored by the capacitor given by eq.(10)
Whenever there is change in the load during this transient period the change in the capacitor energy [XIII]is given by eq.(11)

\[ \frac{1}{2} C_{dc} [V_{dc}^2 (\text{ref}) - V_{dc}^2 (\text{act})] = 3V(xI)t \]  

(11)

Considering 1 MVA 6.6 KV system with capacitor reference voltage as 2300 V and allowing 4 % ripple in capacitor voltage, overloading factor \( x = 1.2 \), \( t = 300 \mu\text{sec} \), the capacitance value is found from the above equation (11). The nearest available value is 1600 \( \mu F \).

Coupling Inductor (\( L_c \)): The selection of the coupling inductor depends on the current ripple and transient response [XIII]. The value of \( L_c \) is calculated by eq.(12)  

\[ L_c = \frac{\sqrt{3} m V_{dc}}{12 f s i_{cr(p-p)}} \]  

(12)

Considering 5 % current ripple, switching frequency 1 kHz, modulation index \((m) = 1\), dc cluster voltage=6900V. So coupling inductor value \( L_c \) is found as 6mH.

| Table 2: System parameters used for simulation |
|-----------------------------------------------|
| Source voltage | 6.6 KV(L-L) |
| Internal impedance of source\((Zs)\) | \( L_s = 0.1 \, \text{mH} \) |
| DC capacitance | 1600 \( \mu F \) |
| Filter inductance | 6mH |
| DC reference voltage for each H-bridge | 2300 V |
| Controlled rectifier load (RL load) | \( \alpha = 30^\circ\) \( R = 300\Omega\), \( L = 500 \, \text{mH} \) |
| Switching frequency, sampling time | 1KHz, 20 \( \mu\text{sec} \) |
| Cluster voltage gain\((k_c)\) | 0.13 |
| Individual dc voltage capacitor balancing\((k_p)\) &\((k_i)\) | 0.12 & 0.19 |
| Current controller proportional gain \((k_{pc})\) & integral gain \((k_{ic})\) | 25 & 50 |

### III. Results and discussion

The modified control strategy is modeled in MATLAB Simulink environment and this strategy is verified under different conditions. The parameters used for simulation are shown in Table 2.
(a) Performance of D-STATCOM with balanced Non-linear load (Controlled rectifier with RL load at $\alpha = 30^0$)

Initially, the system is operating at $i_L = 32$ A, at $t=0.2$ sec an additional load is applied i.e $i_L = 87$ A, which is then removed at $t=0.3$ sec. The source voltage, source current, load current, injected compensating current and dc capacitor voltages are shown in Fig 6(a) and Fig 6(b). During transient period of change in load the dc capacitor voltages are disturbed by 70V, which are then restored back in 0.01sec. It is also observed from the source current waveform that the D-STATCOM is providing the reactive power and eliminating the harmonics such that source current is sinusoidal. Here, the source is providing the active power required by the load. For this particular case the individual dc capacitor voltage balancing method is sufficient for balancing the capacitor voltages.

Fig 6(a) Performance of D-STATCOM under perturbation of balanced change in Non-linear load

Fig 6(b) Variation of Capacitor voltages under perturbation of balanced change in Non-linear load

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(b) Performance of D-STATCOM with unbalanced Non-linear load (Controlled rectifier with RL load at $\alpha = 30^\circ$)

Figure 7 Performance of D-STATCOM under unbalanced Non-linear load

The unbalanced nonlinear is created by opening any one phase of the load connected to the 3 phase 3 wire system. The source voltage, source current, load current, injected compensating current and dc capacitor voltages are observed as shown in Fig 7 at $t=0.24$ sec one of the phase of the load is open and again it is connected at $t=0.34$ sec. During this period the load current is unbalanced, D-STATCOM gives an unbalanced currents such that the source currents are balanced. The individual dc capacitor voltages $V_{cja}, V_{cjb}, V_{cjc}$ where $j=1,2,3$ of all of all the 3 phases are perfectly balanced as observed in Fig 7. The individual dc capacitor voltages are balanced in all the phases so that the cluster voltages are also balanced with the negative sequence current injection method.

(c) Performance of D-STATCOM under unbalanced supply and unbalanced Non-linear load (Controlled rectifier with RL load at $\alpha = 30^\circ$)

Fig 8 Performance of D-STATCOM under unbalanced supply voltages
The unbalanced supply voltage is created from t=0.5 sec to t=0.7 sec and at t= 0.62 sec one of the phase of the load is disconnected and again it is restored at t=0.65 sec. The source voltage, source current, load current, injected compensating current and dc capacitor voltages are observed as shown in Fig 8. During the period of unbalanced source and unbalanced load the individual dc capacitor voltages are restored to its reference values by proper working of the negative sequence current injection algorithm.

IV. Conclusion

The current controlled negative sequence current injection scheme for capacitor balancing in single star -bridge cell (MMCC-SSBC) is investigated for unbalanced nonlinear load and under unbalanced supply voltage. This control scheme is modeled by using MATLAB-SIMULINK and the simulation results show the effectiveness for balancing the capacitor voltages in cascaded H -bridge (MMCC-SSBC) for both balanced and unbalanced supply. The same control scheme is shown to work effectively for unbalanced nonlinear loads also.

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