Polymer waveguides for electro-optical integration in data centers and high-performance computers

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Abstract: To satisfy the intra- and inter-system bandwidth requirements of future data centers and high-performance computers, low-cost low-power high-throughput optical interconnects will become a key enabling technology. To tightly integrate optics with the computing hardware, particularly in the context of CMOS-compatible silicon photonics, optical printed circuit boards using polymer waveguides are considered as a formidable platform. IBM Research has already demonstrated the essential silicon photonics and interconnection building blocks. A remaining challenge is electro-optical packaging, i.e., the connection of the silicon photonics chips with the system. In this paper, we present a new single-mode polymer waveguide technology and a scalable method for building the optical interface between silicon photonics chips and single-mode polymer waveguides.

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OCIS codes: (130.0130) Integrated optics; (130.5460) Polymer waveguides.

References and links

1. statista, The Statistics Portal (2014), “Global data center IP traffic from 2012 to 2017, by data center type,” http://www.statista.com/statistics/227268/global-data-center-ip-traffic-growth-by-data-center-type.
2. TOP500 supercomputer list of June 2014, http://top500.org/static/lists/2014/06/TOP500_201406_Posters.png.
3. M. A. Taubenblatt, “Optical interconnects for high-performance computing,” J. Lightwave Technol. 30(4), 448–457 (2012).
4. P. W. Coteus, J. U. Knickerbocker, C. H. Lam, and Y. A. Vlasov, “Technologies for exascale systems,” IBM J. Res. Develop. 55(5), 141–1412 (2011).
5. D. A. B. Miller, “Physical reasons for optical interconnection,” Int. J. Optoelectron. 11(3), 155–168 (1997).
6. B. J. Offrein, C. Berger, R. Beyeler, R. Dangel, L. Dellmann, F. Horst, T. Lamprecht, N. Meier, R. Budd, F. Libsch, and J. Kash, “Parallel optical interconnects in printed circuit boards,” Proc. SPIE 5990, 59900E (2005).
7. T. Lamprecht, F. Horst, R. Dangel, R. Beyeler, N. Meier, L. Dellmann, M. Gmür, C. Berger, and B. J. Offrein, “Passive alignment of optical elements in a printed circuit board,” in Proceedings of 36th Electronic Components and Technology Conference, pp. 761–767 (2006).
8. D. Dangel, C. Berger, R. Beyeler, L. Dellmann, M. Gmür, R. Hamelin, F. Horst, T. Lamprecht, T. Morf, S. Oggioni, M. Sprefico, R. Stevens, and B. J. Offrein, “Polymer-waveguide-based board-level optical interconnect technology for datacom applications,” IEEE Trans. Adv. Packag. 31(4), 759–767 (2008).
9. F. E. Doany, C. L. Schow, C. W. Baks, D. M. Kuchta, P. Pepeljugoski, L. Schafer, R. Budd, F. Libsch, R. Dangel, F. Horst, B. J. Offrein, and J. A. Kash, “160 Gb/s bidirectional polymer-waveguide based board-level optical interconnects using CMOS-based transceivers,” IEEE Trans. Adv. Packag. 32(2), 345–359 (2009).
10. D. Jubin, R. Dangel, N. Meier, F. Horst, T. Lamprecht, J. Weiss, R. Beyeler, B. J. Offrein, M. Halter, R. Stieger, and F. Betschon, “Polymer waveguide based multi-layer optical connector,” Proc. SPIE 7607, 76070K (2010).
11. R. Dangel, F. Horst, D. Jubin, N. Meier, J. Weiss, B. J. Offrein, B. W. Swatowski, C. M. Amb, D. J. DeShazer, and W. K. Weidner, “Development of versatile polymer waveguide flex technology for use in optical interconnects,” J. Lightwave Technol. 31(24), 3915–3926 (2013).
12. M. Fields, “Applications and commercialization of board mounted parallel optics,” presented at Market Focus at ECOC 2013 Exhibition, http://www.ecocexhibition.com/sites/default/files/files/ECOC 2013 Market Focus Avago FIELDS FINAL.pdf.
13. S. Assefa, S. Shank, W. M. J. Green, M. Khater, E. Kiewra, C. Reinholm, S. Kamlapurkar, A. Rylyakov, C. Schow, F. Horst, H. Pan, T. Topuria, P. Rice, D. M. Gill, J. Rosenberg, T. Barwicz, M. Yang, J. Proesel, J. Hofrichter, B. J. Offrein, X. Gu, W. Haensch, J. Ellis-Monaghan, and Y. A. Vlasov, “A 90nm CMOS integrated
nano-photonics technology for 25Gbps WDM optical communications applications,” in IEEE Electron Devices Meeting (IEDM), pp. 33.8.1 - 33.8.3 (2012).
14. F. Horst, W. M. J. Green, B. J. Offrein, and Y. A. Vlasov, “Silicon-on-insulator Echelle grating WDM demultiplexers with two stigmatic points,” IEEE Photon. Technol. Lett. 21(23), 1743–1745 (2009).
15. F. Horst, W. M. J. Green, S. Assefa, S. M. Shank, Y. A. Vlasov, and B. J. Offrein, “Cascaded Mach-Zehnder wavelength filters in silicon photonics for low loss and flat pass-band WDM (de-)multiplexing,” Opt. Express 21(10), 11652–11658 (2013).
16. D. Taillaert, P. Bienstman, and R. Baets, “Compact efficient broadband grating coupler for silicon-on-insulator waveguides,” Opt. Lett. 29(23), 2749–2751 (2004).
17. G. Roelkens, D. Van Thourhout, and R. Baets, “High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay,” Opt. Express 14(24), 11622–11630 (2006).
18. K. Shiraishi, H. Yoda, A. Oshihama, H. Ikedo, and C. S. Tsai, “A silicon-based spot-size converter between single-mode fibers and Si-wire waveguides using cascaded tapers,” Appl. Phys. Lett. 91(14), 141120 (2007).
19. Y. Liu, Y. Li, Z. Fan, B. Xing, Y. Yu, and J. Yu, “Fabrication and optical optimization of spot-size converters with strong cladding layers,” J. Opt. A, Pure Appl. Opt. 11(8), 085002 (2009).
20. A. Yariv, Quantum Electronics, Third Edition (Wiley, 1989), Chap. 22.
21. A. W. Snyder and J. D. Love, Optical Waveguide Theory (Chapman & Hall, 1983), Chaps. 19, 28.
22. I. M. Soganci, A. La Porta, and B. J. Offrein, “Flip-chip optical couplers with scalable I/O count for silicon photonics,” Opt. Express 21(13), 16075–16085 (2013).

1. Introduction

1.1 Performance development of data centers and high performance computers

Worldwide, the internet data traffic growths tremendously, which implies steadily increasing performance requirements on the data centers [1]. New applications in Cloud computing, as projected in Fig. 1, Big Data, and Social Media will aggravate the issue of data-center performance even more. A similar trend is also observed for high-performance computers (HPC). For example, the performance of the most powerful supercomputers of the TOP500 list [2] has increased by a factor of 10 every four years over the past 20 years, as illustrated in Fig. 2. Following this trend, the industry is expected to provide first exaflop supercomputers in 2020 with a 30 times higher performance than today’s No. 1 supercomputer, which provides 33.9 petaflops/s.

Fig. 1. Global data-center IP traffic development from 2012 to 2017 (split by data-center type) [1].

Fig. 2. “Top500 list” showing performance development of the 500 most powerful supercomputers from 1993 to 2017 [2].

To meet the projected performance requirements of future data centers and HPCs [3,4], the communication bandwidth needs to scale accordingly at all levels of the system, i.e.,
exponentially. Consequently, there is a strong need for high-bandwidth, high-speed interconnects between racks, on backplanes, daughter-cards, carriers, and finally on the chip level. Optical link technology offers fundamental advantages in scaling, bandwidth, density, and power efficiency compared with established electrical interconnects [5]. In today’s computer systems, mainly multi-mode (MM) optical link technology at a wavelength of 850 nm is applied. For increasing the bandwidth × length product of optical interconnects in future systems, single-mode (SM) technology is attracting increasing attention. This is further sustained by the emergence of silicon (Si) photonics. To meet system-cost and power constraints, a high level of integration will be required, which in our view can be achieved with the following two technologies:

(I) CMOS-based Si photonics using Si-On-Insulator (SOI) waveguides.

(II) Optical Printed Circuit Board (PCB) technology using optical polymer waveguides.

Si photonics is an emerging integrated-optics technology platform based on an SOI structure, in which a wide variety of optical and electro-optical functions can be densely integrated. Optical PCB technology is an extension of established electrical PCB technology with optical signal distribution capability.

1.2 Optical PCBs and Si photonics as key technologies

We have already reported in detail on the realization of our optical PCB technology using siloxane-based low-loss multi-mode waveguides for 850-nm-wavelength applications [6–11]. Various passive and active optical interconnect demonstrators have been built that use MM waveguides in or on top of mechanically rigid, Figs. 3(a) and 3(b), as well as flexible, Fig. 3(c), optical PCBs. In this paper, we therefore focus on Si photonics and possible packaging approaches. We will briefly present IBM’s 90-nm CMOS-based Si photonics technology and report on our newly developed single-mode (SM) polymer waveguide technology for wavelengths of 1310 and 1550 nm. In particular, we will highlight “adiabatic optical coupling” as a low-cost photonic coupling approach with relaxed alignment tolerance and scalability to very high I/O (Input/Output) counts.

![Image](https://via.placeholder.com/150)

**Fig. 3.** (a) Optical transmitter card of a 12 × 10 Gbit/s optical-link demonstrator containing 12 embedded multi-mode polymer waveguides [8]. (b) High-speed and low-power link demonstrator TERABUS (funded by Darpa) with 2 “Optochips” linked by 32 on-board high-density polymer waveguides (with 62.5 μm pitch) [9]. (c) Optical backplane of 192 channels with complex channel shuffling based on 8 stacked polymer waveguide flexes (after connectorization) [10].

2. Photonics integration

The cost-effective and power-efficient optical interconnects needed require the availability of low-cost and low-power transceivers. Most commercially available optical transceivers, such
as used e.g., in active optical cables (AOCs), are built from discrete components (lasers, modulators, photodetectors, amplifiers) in sequential fabrication processes and then assembled into standardized-form-factor housings (e.g., SFP, SFP+, QSFP). One example in which this technology was extensively used, is IBM’s former No. 1 supercomputer ROADRUNNER, introduced in 2008, which was the first petaflop system. In ROADRUNNER, photonics was used exclusively at the card edge, see Fig. 4(a). Three years later, IBM launched the POWER 775 supercomputer. In the POWER 775 system, photonics was brought onto the board. For the first time in a system of that scale, the optical transceivers were assembled into the ASIC (Application-Specific Integrated Circuit) package. On each carrier substrate, 56 optical transceiver modules (Avago MicroPOD [12]) were assembled and connected to the board edge by MM optical-fiber ribbons, see Fig. 4(b). In the largest POWER 775 system, about one million fibers were required. From an assembly, routing, and cost perspective, this huge number of discrete photonic components is a challenge. In electrical systems, discrete components and electrical wires have been replaced by integrated circuits and PCB technology. We believe that optical technologies will have to follow a similar path. An additional challenge is to maintain compatibility with existing electrical manufacturing and assembly technologies, i.e., to establish a unified electro-optical assembly and integration platform.

Established approaches for integrating optical interconnects in server systems rely on the assembly of the electro-optical components in a transceiver housing, which is then attached to the system. Examples of such packaging techniques are the card-edge assembly of active optical cables and the board-level integration of embedded optical transceivers. To massively improve the density of the interconnects in order to minimize the assembly overhead and related costs, we investigate a radically different approach in which the Si photonics chip is integrated directly on the carrier substrate, together with the ASIC chip, as shown in Fig. 4(c).

![Fig. 4. Photonics integration: (a) In 2008: IBM’s former No. 1 supercomputer ROADRUNNER with optics (AOCs) at the board edge only. (b) In 2011: IBM’s HPC system POWER 775 with many optical transceivers assembled on carriers and a huge number of fibers connected with the board edge. (c) Current research: optical polymer waveguides connecting Si photonics chips assembled on carriers with the carrier edge, other carriers, and board edge.](image-url)
Polymer waveguides are envisioned to distribute the optical signals, similar to the role played by copper traces and vias in established high-density electrical laminates. Furthermore, they form the interface between the Si photonics chip and the fiber cable. This approach has several advantages:

a) Direct soldering of Si photonics chips reduces the overall assembly effort.

b) Higher bandwidth density because of smaller footprint (no housing).

c) Improved electrical signaling due to shorter electrical interconnects with fewer interfaces.

d) Additional functionalities available in integrated Si photonics, such as wavelength division multiplexing (WDM).

For our current research approach on the carrier level, as illustrated in Figs. 4(c) and 5, we are aiming at $\geq 1$ Tbit/s off-carrier optical communication. To achieve this, a very high optical-channel count and channel density will be required. Currently, we consider a wavelength-transparent in-plane coupling as a viable option, in contrast to, e.g., the wavelength-dependent out-of-plane grating couplers. Adiabatic optical coupling to SM polymer waveguides can provide the large operating-wavelength window needed as well as parallel coupling between a large number of SOI and polymer waveguides. Additional advantages are rather relaxed alignment and manufacturing tolerances, as will be described below.

![Fig. 5. Schematic illustrating current research work, i.e., the use of SM polymer waveguides to connect Si photonics chips with the system.](image)

3. Silicon photonics technology

The prospects of Si photonics of providing a low-cost high-throughput platform for the integration of optics into the electronics ecosystem, motivate researchers in academia and industry around the world to investigate the field. Si photonics builds on the infrastructure established for CMOS (Complimentary Metal-Oxide Semiconductor) technology to realize integrated-optical functions in SOI technology. In IBM’s Si photonics technology, optical and CMOS-based electrical building blocks are combined in one platform. These building blocks are modulators, detectors, WDM multiplexers and demultiplexers, as well as drivers and amplifiers. Figure 6 schematically shows the functions combined in an integrated transmitter and receiver chip.
The low-cost expectations of Si photonics are mainly attributed to its compatibility with the manufacturing technologies of CMOS devices, which have been performance- and cost-optimized over decades. IBM has been researching Si photonics devices for more than ten years. An entire set of Si photonics building blocks was demonstrated, including electro-optical modulators [13], waveguide-integrated germanium photo-detectors [13], WDM (de)multiplexers, based e.g., on optical echelle gratings [14] or cascaded Mach–Zehnder filters [15], see Fig. 7.

The system-level integration of this technology will be based on transceiver packages incorporating the Si photonics chips and all other building blocks required. However, to integrate the Si photonics-based building blocks into the system, one important technological challenge remains: the optical connection from the Si photonics chips to the rest of the computer system. For Si-photonics-based devices with low channel count, the coupling is typically made by waveguide diffraction gratings [16,17] or on-chip spot-size converters [18,19].
4. Large-area-capable single-mode polymer waveguide technology

4.1 From MM to SM polymer waveguides

Recently, we established a single-mode polymer waveguide technology for $\lambda = 1310$ and 1550 nm wavelength. This technology extends our existing low-loss multi-mode polymer waveguide technology developed for 850 nm using siloxane-based polymers from Dow Corning Corporation (DCC). For SM applications, DCC reformulated the core and cladding polymer to enable low absorption at 1310 and 1550 nm. Furthermore, the core-cladding index contrast was lowered from $\Delta n \approx 0.02$ to 0.005 – 0.008 for SM operation of square-shaped waveguides of 6 – 8 $\mu$m width and height. The critical waveguide processing steps, the doctor-blading for polymer-layer deposition and the UV-laser direct-writing, or alternatively the mask-lithography patterning, can be applied for both the MM and the SM system. The doctor-blading and the laser-writing processes are scalable to large-panel-size fabrication. In our lab, we realize SM waveguide structures on panels of up to 450 × 300 mm$^2$ in size. Figure 8 schematically shows the fabrication process with UV-induced polymerization/patterning, solvent-based wet-chemical development, and a single curing bake at the end of the processing. All in all, a very straightforward process, requiring a short overall processing time of less than 90 min. In Table 1, some of the key properties of our new SM polymer waveguides are listed for comparison with the MM polymer waveguides and the SOI waveguides on Si photonics chips.

Table 1. Comparison between MM polymer, SM polymer, and SOI waveguides (WGs)

| Properties | MM polymer WGs | SM polymer WGs | SOI waveguides |
|------------|----------------|----------------|---------------|
| WG dimensions [width × height] | 35–50 $\mu$m × 35–50 $\mu$m | 6–8 $\mu$m × 6–8 $\mu$m | 300–500 nm × 140–250 nm |
| Operation wavelength | 850 nm | 1.31 and 1.55 $\mu$m | 1.31 and 1.55 $\mu$m |
| Typical propagation loss | 0.05 dB/cm @ 850 nm | 0.5 dB/cm @ 1.31 $\mu$m | 3 dB/cm @ 1.31 $\mu$m |
| Butt-coupling typically to $(N/A = $ numerical aperture) | MM graded-index fiber with $N/A = 0.22$ | SM step-index fiber with $N/A = 0.14$ | |
| Typical x/y-coupling tolerance | 3–5 $\mu$m | 1 $\mu$m | |
To ensure SM waveguide behavior and to achieve a reproducible coupling efficiency to standard SM fibers, we have to control the waveguide core thickness within ± 0.5 μm. For that purpose, our system consists of an ultra-planar vacuum chuck, Fig. 9, with ± 1 μm planarity over the entire area of 500 × 375 mm² and an ultra-planar doctor-blade, Fig. 10(a), with a planarity of better than ± 0.5 μm over the entire span of about 300 mm. Polymer deposition by means of doctor-blading is illustrated in Fig. 10(b). Furthermore, we use PCB-compatible substrates with an overall thickness uniformity of ± 1 μm. There are commercially available PCB substrates (e.g., DuPont KAPTON flexible polyimide films) that fulfill this requirement. The vacuum chuck features 20 × 30 = 600 tiny vacuum holes regularly distributed over the chuck top surface. This is necessary to keep the substrates completely flat throughout the entire waveguide fabrication process.

![Ultra-planar vacuum chuck with 600 tiny vacuum holes and an overall planarity of ± 1 μm to achieve ± 0.5 μm polymer layer thickness control.](image)

Fig. 9. Ultra-planar vacuum chuck with 600 tiny vacuum holes and an overall planarity of ± 1 μm to achieve ± 0.5 μm polymer layer thickness control.

![Schematical side-view of doctor-blading process used for polymer-layer deposition on PCB-compatible substrates](image)

4.2 Experimental results

By applying the process discussed above, we demonstrated SM polymer waveguides on rigid Si and glass wafers of up to 8” diameter and on flexible substrates up to a panel size of ≈ 450 × 300 mm². Figure 11(a) shows a completed waveguide flex panel, which carries numerous samples. Each sample, one is depicted in Fig. 11(b), consists of an array of 12 straight, 7-μm-wide SM waveguides, which are spaced 50 μm apart and have the top cladding locally removed, see Fig. 11(c). These waveguide samples were used to investigate the adiabatic optical coupling approach, which is described in detail in Section 5.
Because the new SM polymer waveguide technology is strongly based on our existing MM polymer waveguide technology, many processing challenges have already been solved. The excellent properties established in the MM material could be maintained. Polymer adhesion to the substrate is very good and the curling of the structure due to CTE (Coefficient of Thermal Expansion) mismatch could be tackled and mitigated in an early stage of the SM waveguide development. This is illustrated in Fig. 12(a), where two wafer-size SM waveguide patterns (120 × 120 mm²) were realized on a panel-size transparent flexible substrate. The two SM waveguide flexes exhibit virtually no CTE-induced curling both before and after a thermal treatment of 1 h at 200°C, see Figs. 12(b) and 12(c). Flatness of the waveguide samples is important for their use in various packaging applications (e.g., in adiabatic optical coupling).

5. Adiabatic optical coupling between Si photonics chips and SM polymer waveguides

5.1 Principle of adiabatic optical coupling

To exploit the potential of Si photonics, as described in Section 3, we investigate adiabatic optical coupling as means to connect the Si photonics chips with the system and a fiber array. The physics behind this is based on the adiabatic transformation of the optical mode of an SOI waveguide to that of a SM polymer waveguide and on the reduction of the SOI waveguide width.
The cores of the SOI and polymer waveguides are brought into either physical contact or very close proximity to each other. Upon gradually tapering the SOI waveguide, the supermodes (i.e., eigenmodes of the coupled-waveguide system) evolve adiabatically along the coupler [20,21]. Figure 13 depicts the positioning of the tapered SOI waveguide core on the SM polymer waveguide core.

In Fig. 14, the simulation results for $\lambda = 1550$ nm depict the coupling mechanism based on mode transformation: At the input of the taper, Fig. 14(a), the supermode of the coupled SOI/polymer waveguide system is completely confined in the SOI core. At the taper center, Fig. 14(b), the supermode extends over both waveguide cores. And at the output of the taper, Fig. 14(c), the supermode is completely confined in the SM polymer waveguide core. Because of reciprocity, this coupling method is bi-directional, i.e., allows optical coupling from SOI to polymer waveguides and vice versa. Additional simulations and experimental results (see Section 5.2) showed that this approach is tolerant in terms of lateral positioning errors and in terms of process variations in waveguide dimensions, refractive indices, and wavelength. In contrast to directional coupling, adiabatic optical coupling does not require phase-matching between SOI and polymer waveguide mode, and their effective refractive indices are different.

The big advantage of adiabatic optical coupling, from an assembly and cost perspective, is the scalability to a large number of SOI waveguides and polymer waveguides that can be connected simultaneously in a single bonding step. Moreover, assuming that the polymer waveguides are deposited on a dedicated interposer or carrier with suitable electrical contact pads, the optical coupling as well as many electrical contacts can be established in a single flip-chip bonding step, as illustrated in Fig. 13.
5.2 Experimental proof of concept

In a recent paper [22], we reported in detail on the design, fabrication, and experimental proof of concept of multi-channel adiabatic optical couplers for Si photonics chips which were flip-chip-bonded onto SM polymer waveguides. The corresponding experimental layout, results, and findings are summarized below.

Figure 15(a) depicts the experimental layout used for the proof of concept: light initially propagating in a SM polymer waveguide is coupled adiabatically to an SOI waveguide, which transports the signal through an S-bend to the adjacent polymer waveguide channel. The second adiabatic coupler transfers the signal from the SOI waveguide to the second polymer waveguide. To realize this waveguide configuration experimentally, a Si photonics chip with S-bent SOI waveguides was flip-chip-bonded to an array of straight SM polymer waveguides whose top cladding had been removed. Figure 15(b) shows a top-view photograph of the assembly prior to application of an optically transparent epoxy-underfill material. This underfill material provides mechanical stability and acts as the required upper cladding for the SOI and polymer test waveguides. In Fig. 16, the schematic and the micrograph show the cross-section of a completed adiabatic optical coupler.

Fig. 14. Theoretical simulation results for adiabatic optical coupling at $\lambda = 1550$ nm: (a) light is completely confined in SOI waveguide, (b) light is confined in both waveguides, and (c) light is completely confined in SM polymer waveguide.

Fig. 15. (a) Schematic of SOI and SM polymer waveguide layout to prove the concept of adiabatic optical coupling. To characterize the coupler performance, the optical transmission of the input-to-cross, input-to-bar, and reference path had to be measured. (b) Microscopical top-view of Si photonics chip flip-chip-bonded onto an array of un-cladded SM polymer waveguides.
The SOI chip was flip-chip bonded onto the polymer waveguides by thermocompression bonding. A flip-chip bonder (FC 150 by Smart Equipment Technology) was used for this
purpose. Our tool is configured for manual use. However, the FC 150 can be upgraded for automated alignment enabling production capabilities. The silicon and polymer waveguide samples were parallelized and aligned to each other visually. This approach is limited by the placement accuracy (± 1 µm) and the vision system resolution (0.42 µm/pixel) of the flip-chip bonder.

The adiabatic coupling measurements presented in Fig. 18 were performed with an adiabatic optical coupler, as shown in Fig. 16, with a non-linear taper consisting of three segments with different tapering angles. For each input port, the transmission was measured at the corresponding bar and cross port. To extract the optical loss of one adiabatic coupling structure, we also measured the transmission loss through a reference SM polymer waveguide that is separated physically from any SOI waveguide. The experimental results show a coupling loss of 0.8 – 1.1 dB for TE polarization and of 0.8 – 1.3 dB for TM polarization for wavelengths $\lambda = 1530$ nm, 1550 nm, and 1570 nm, according Figs. 18(a)-18(c). At 1550 nm, the extra loss caused by a lateral misalignment of $\Delta x = \pm 2$ µm, as depicted in Fig. 17, is less than 0.6 dB for TE polarization and 0.3 dB for TM polarization. This clearly highlights the relaxed alignment accuracy requirements compared with those of direct butt-coupling.

![Fig. 18. Loss per coupler versus lateral offset between SOI and polymer waveguides at the wavelength $\lambda$ of (a) 1530 nm, (b) 1550 nm, and (c) 1570 nm and for the two polarizations TE and TM.](image)

To facilitate the interpretation of the measurement data for the three wavelength $\lambda = 1530$ nm, 1550 nm, and 1570 nm, Table 2 lists the lowest coupling losses and the highest losses induced by a lateral misalignment within an offset range of ± 2 µm.
Table 2. Lowest coupling losses and highest losses induced by SOI waveguide to polymer waveguide misalignment within an offset range of ± 2 µm

| Wavelength (nm) | Lowest TE loss (dB) | Lowest TM loss (dB) | Highest TE loss within ± 2 µm offset range (dB) | Highest TM loss within ± 2 µm offset range (dB) |
|-----------------|---------------------|---------------------|-----------------------------------------------|-----------------------------------------------|
| 1530 nm         | 1.0                 | 1.3                 | 0.9                                           | 0.7                                           |
| 1550 nm         | 1.2                 | 1.2                 | 0.6                                           | 0.3                                           |
| 1570 nm         | 0.8                 | 0.8                 | 0.6                                           | 0.3                                           |

One interesting application for adiabatic optical coupling is in processor packaging. Because processors dissipate a lot of power, optical interfaces in that environment are exposed to substantial temperature variations during operation. For this purpose, we investigated the sample of Fig. 16 at different temperatures, but could not find any significant coupling-loss dependencies up to 70°C, as can be seen in Fig. 19. This low temperature sensitivity can be explained by the fact that adiabatic optical coupling does not rely on resonant operating conditions, which are known to be more susceptible to temperature variations. A temperature increase leads to a change of the refractive indices of the materials, but the adiabatic coupler continues to function as long as the polymer waveguide has a higher refractive index than the buried oxide.

![Normalized loss per coupler as a function of temperature](image)

Fig. 19. Normalized loss per coupler as a function of temperature. The data corresponds to wavelength $\lambda = 1550$ nm and TM polarization.

5.3 Application area of adiabatic optical coupling and SM polymer waveguides

With the currently achieved propagation losses of our SM polymer waveguides of about 1 dB/cm for $\lambda = 1.55$ µm and 0.5 dB/cm for $\lambda = 1.31$ µm, according Table 1, on-carrier polymer waveguide interconnects with cm-lengths are feasible. For longer off-carrier links, fiber-based solutions with lower propagation losses are envisioned. In the future however, by reducing further the intrinsic polymer material losses towards 0.1 dB/cm, SM polymer waveguides will be suitable also for board-level applications.

6. Conclusion

In this paper, we summarized IBM’s research results of two optical technologies, which we consider as key for the dense system integration required to satisfy the intra- and inter-system bandwidth demands of future data centers and HPCs. In both fields, the CMOS-based Si photonics using SOI waveguides and the optical PCB technology using polymer waveguides, an entire set of building blocks has been demonstrated. We also presented our newly developed SM polymer waveguide technology for 1310 and 1550 nm wavelength, which helps tackle an important remaining issue, the interfacing of the Si photonics chips to the system. SM polymer waveguides samples on both rigid and flexible PCB-compatible substrates were realized in a panel-size fabrication process, which is an extension of our established MM polymer waveguide process developed for optical PCBs. Our SM polymer...
waveguides proved to be a suitable optical platform for adiabatic optical coupling with Si photonics waveguides. Low-loss adiabatic optical coupling with a relaxed lateral alignment tolerance of ± 2 μm between SM polymer and SOI waveguide arrays could be demonstrated. Theoretical and experimental work to further improve the coupling efficiency and to demonstrate the potential of this approach in terms of high-channel count is ongoing.

Acknowledgments

The authors would like to thank M. Taubenblatt, C. Schow, F. Doany, C. Baks, R. Budd, F. Libsch, S. Assefa, W. Green, J. Rosenberg, W. Haensch, T. Barwicz, S. Nakagawa, Y. Taira and many others at IBM for their technical work and insights contributing to and underlying the content of this paper. Furthermore, we would like to thank Dow Corning Corporation (Midland, MI, USA) for developing and tailoring the optical polymers. This work was partially supported by the European Union Seventh Framework projects FIREFLY, RAPIDO, and CARRICOOL.