Design of Synaptic Neuronal Circuit Based on Memristors

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Abstract: To solve the problems of poor learning efficiency and low accuracy caused by the single fixed synaptic weight in the traditional artificial neural network. On the foundation of the improved memristor model, this paper designs a synaptic neuronal circuit based on the natural memory characteristics of the memristor. This synapse is composed of six memristors. The resistance of the memristor is changed by adding a periodic square wave to update the synaptic weight. This circuit can realize signed synaptic weighting, which has certain linear characteristics. Finally, two synaptic weight update methods are proposed based on this circuit, and the validity of the design is verified through Spice simulation experiments.

1. Introduction

The memristor [1] is considered to be the best device for designing synaptic circuits due to its non-volatility, memory, nanometer size, and high integration. In recent years, scholars have studied more and more synaptic circuits. Literature [2] proposed a synaptic circuit composed of a single memristor, which can simulate the relative plasticity of synapses, but the controllability is poor. It can achieve "positive" synaptic weights. The synaptic circuit proposed in [3] consists of two memristors, but it can only achieve "positive" synaptic weights, which has limitations. Literature [4] introduced a transistor as a switch to realize the linear operation of the synaptic weights, which improved the accuracy of the weights, but the linearity characteristics were poor. Literature [5] proposed a synaptic circuit composed of four memristors, which can realize the "negative", "zero", and "positive" of the synaptic weights, but the weight processing process still does not have linear characteristics and is accurate Degree is low. Literature [6] is composed of two memristors and two resistors, which can realize the "negative", "zero", and "positive" of the weight, but it increases the power consumption and the circuit size, and the weight processing process is not continuous. Affect the speed of neural network training. Based on the above, this paper proposes a synaptic circuit composed of six memristors and proposes two-weight processing methods, which not only realizes the "negative", "zero", and "positive" of the synaptic weight but also has a good Circuit compatibility and linearity characteristics.

2 Memristor model

2.1 Proposal of the memristor

As shown in Figure 1, the existing basic components have always lacked a component that can express the relationship between the charge and magnetic flux of the charge memristor. In 1971, Chua defined the relationship between the two based on the completeness principle of circuit theory [7]. The defined
circuit element [8] is called a memristor.

![Diagram of four basic elements: resistance, capacitance, inductance, and memristor](image)

According to the literature [9], the resistance of the HP memristor is:

\[ M(t) = R_L \cdot x(t) + R_H [1 - x(t)] \quad (1) \]

\[ x(t) = \frac{w(t)}{D} \in [0,1] \quad (2) \]

\( x \) represents the internal state of the memristor, which is the ratio of the doping thickness (\( w \)) to the film thickness (\( D \)). \( R_L \) and \( R_H \) are the minimum memristive value and the maximum memristive value of the memristor, respectively. The state equation corresponding to the state is:

\[ \frac{dx}{dt} = k_i(t) \quad (3) \]

\[ k = \frac{u_v R_L}{D^2} \quad (4) \]

\( u_v \) represents the average mobility of ions, \( i \) represents the current flowing through the memristor, and \( k \) is the ratio of the changing speed of the state variable to the current flowing through the memristor[10].

### 2.2 Threshold Memristor Modeling

To better simulate the nonlinear migration phenomenon of ions inside the memristor, equation (3) can be improved as:

\[ \frac{dx}{dt} = k_i(t) \cdot f(x) \quad (5) \]

\( f(x) \) is the window function, and \( joglekar \) functions are used in this article:

\[ f(x) = 1 - (2x - 1)^{2p} \quad (6) \]

The above model has a simple structure and is easy to implement, but it does not have threshold characteristics. Based on this, it is necessary to add a threshold function to this model as follows:

\[ g(x) = \begin{cases} 0, & v \leq v_T \\ 1, & v > v_T \end{cases} \quad (7) \]

So the state equation can be further rewritten as:

\[ \frac{dx}{dt} = k_i(t) \cdot f(x) \cdot g(x) \quad (8) \]

When the input voltage is greater than the memristor threshold, the memristor resistance changes. The resistance of the memristors do not change if it does not reach the memristor threshold voltage. The memristors used below are all of this model.
3 Synapse circuit design

Figure 2 shows the specific neuron circuit. All synaptic circuits share an active load. During the operation of the circuit, the output voltage of each synaptic circuit is converted into a corresponding current signal by a differential amplifier and finally converted by a load circuit. For the corresponding voltage signal output.

The synapse circuit consists of six memristors. When a forward or reverse voltage is applied to the input, the resistance of the memristor increases or decreases depending on its polarity. Each circuit contains three memristors. When a strong forward voltage is applied, the resistance of the forward-biased memristor becomes smaller, the voltage at point A increases, and the resistance of the reverse-biased memristor increases, and the voltage at point B decreases.

The memristor components of this synapse circuit are \( M_1, M_2, M_3, M_4, M_5, M_6 \). Define the input voltage as \( v_{in} \), then the voltage at point A is:

\[
v_A = \frac{M_2 + M_3}{M_1 + M_2 + M_3} v_{in} \tag{9}
\]

The voltage at point B is:

\[
v_B = \frac{M_5 + M_6}{M_4 + M_5 + M_6} v_{in} \tag{10}
\]

The voltage difference between point A and point B is (9)-(10), which can be obtained:

\[
v_A - v_B = \frac{M_2 + M_3}{M_1 + M_2 + M_3} v_{in} - \frac{M_5 + M_6}{M_4 + M_5 + M_6} v_{in} \tag{11}
\]

And because the memristors \( M_2 \) and \( M_3 \) are connected in reverse series, and the total resistance is \( M(t) \), we can get:

\[
M(t) = M_2(t) + M_3(t) \tag{12}
\]

Select memristor \( M_2, M_3, M_5, M_6 \) as the same type of memristor, which can be obtained by formula (1), the initial values of \( M_2 \) and \( M_3 \) at zero time:

\[
M_2(0) = R_L \cdot x(0) + R_H [1 - x(0)] \tag{13}
\]

\[
M_3(0) = R_H \cdot x(0) + R_L [1 - x(0)] \tag{14}
\]

\( x(0) \) is the state of the memristor at zero time, the resistance value of \( M_2, M_3 \) can be written as:

\[
M_2(t) = R_L \cdot [x(t) + x(0)] + R_H [1 - x(t) - x(0)] \tag{15}
\]

\[
M_3(t) = R_H \cdot [x(t) + x(0)] + R_L [1 - x(t) - x(0)] \tag{16}
\]

Substituting formulas (15) and (16) into (12), we can get:

\[
M(t) = M_2(0) + M_3(0) \tag{17}
\]

From (17), the memristor is connected in reverse series, the total resistance value is the initial value and the sum of the resistance values is a constant, denoted as \( M \), and then into equation (11):

\[
v_A - v_B = \frac{M}{M_1 + M} v_{in} - \frac{M}{M_4 + M} v_{in} = \left( \frac{M_4 - M_3}{M_1 + M_2 + M_3} \right) v_{in} \tag{18}
\]

Formula (18) can be expressed as:

\[
v_A - v_B = k v_{in} \tag{19}
\]

The changing trend of synapse weight \( k \) is:
\[
\begin{aligned}
&k > 0, M_4 > M_1 \\
&k = 0, M_4 = M_1 \\
&k < 0, M_4 < M_1
\end{aligned}
\]  

(20)

4 Experimental results and analysis

4.1 HP Memristor with Threshold

Figure 3 Simulation diagram of threshold memristor characteristics

Set the memristor threshold voltage to 0.5V, Figure 3 shows the V-I curve of the memristor when the input voltage is a sin function.

4.2 Update of Synaptic Circuit Weights

4.2.1 Forward voltage updates synaptic weights

Figure 4. Forward voltage updates synaptic weights

Define parameters \( R_L = 100\Omega \), \( R_H = 15k\Omega \), \( D = 10nm \), \( u_y = 10^{-14} m^2s^{-1}v^{-1} \), \( P = 1 \), \( v_T = 0.5V \), \( M_1(0) = 14k\Omega \), \( M_4(0) = 1k\Omega \). Other memristor resistance values are 1kΩ.

As shown in Figure 4, input a two-second periodic voltage, and the synapse weight changes. Based on the different initial resistance settings of the memristors \( M_1 \) and \( M_4 \), the synaptic weights can be updated and maintained only with the forward voltage, which greatly improves the learning efficiency of the neural network.

4.2.2 Bidirectional voltage update synaptic weight

Define parameters \( R_L = 100\Omega \), \( R_H = 15k\Omega \), \( D = 10nm \), \( u_y = 10^{-14} m^2s^{-1}v^{-1} \), \( P = 1 \), \( v_T = 0.5V \), \( M_1(0) = 8k\Omega \), \( M_4(0) = 8k\Omega \). Other memristor resistance values are 3kΩ.

As shown in Figure 5, input the forward and reverse voltages for 1.5 seconds respectively, and the changes in the synaptic weight. Based on the same initial resistance settings of the memristors \( M_1 \) and \( M_4 \). To realize the update of synaptic weight. The continuity of the input voltage can be achieved through an external circuit, and the synapse weight has a linear characteristic.
Figure 5. Bidirectional voltage update synaptic weight

From the above simulation results, it can be seen that the above two methods can realize the update of synapse weights, and the methods are stable, indicating that this synapse is beneficial to the smooth progress of the neural network and the test. It should be noted that the operation and operation of the entire neural network circuit are based on impulse signals. This is mainly because of the stability and ease of implementation of the pulse signal. At the same time, the memristive synaptic circuit is easier to control the weight under the pulse signal, such as the change time of the memristor resistance value, the change time of the synapse weight, so Need a duty cycle and so on, further thinking, within the range of the pulse period, the power consumption of the circuit can be better reduced, to avoid the waste of energy.

5. Conclusions
This paper proposes a synaptic neuron circuit. Both of the two synaptic weight adjustment methods used can achieve signed synaptic weights, which can maintain a certain linear characteristic in the process, and the synaptic weights are stable and controllable. The synapse circuit is only composed of memristors. Compared with the traditional neuron circuit, the circuit compatibility is higher and the synapse weight can be stored in time. The effectiveness of this synaptic neuron circuit function is verified by Spice simulation experiments. Therefore, this design is of great significance to the research of neural network circuits and has a certain reference value.

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