A 2D analytical cylindrical gate tunnel FET (CG-TFET) model: impact of shortest tunneling distance

S Dash and G P Mishra

1 Deparment of Electronics and Communication Engineering, Institute of Technical Education and Research, Siksha ‘O’ Anusandhan University, Khandagiri, Bhubaneswar, India
2 Device Simulation Lab, Department of Electronics and Instrumentation Engineering, Institute of Technical Education and Research, Siksha ‘O’ Anusandhan University, Khandagiri, Bhubaneswar, India

E-mail: gurumishra@soauniversity.ac.in

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Abstract

A 2D analytical tunnel field-effect transistor (FET) potential model with cylindrical gate (CG-TFET) based on the solution of Laplace’s equation is proposed. The band-to-band tunneling (BTBT) current is derived by the help of lateral electric field and the shortest tunneling distance. However, the analysis is extended to obtain the subthreshold swing (SS) and transfer characteristics of the device. The dependency of drain current, SS and transconductance on gate voltage and shortest tunneling distance is discussed. Also, the effect of scaling the gate oxide thickness and the cylindrical body diameter on the electrical parameters of the device is analyzed.

Keywords: TFET, cylindrical gate, BTB tunneling, drain current, subthreshold swing

Classification numbers: 2.00, 2.07, 3.00, 3.02, 4.00, 4.12, 6.01

1. Introduction

As conventional metal oxide semiconductor field-effect transistors (MOSFETs) are downscaled to the sub-nanometre region, the close proximity between source and drain reduces the controlling capability of the gate over the channel. This leads to several problems, such as high subthreshold swing (SS), high leakage current in the OFF state (I\text{OFF}), a complex supply voltage reduction, and other short channel effects (SCEs) like threshold voltage roll-off and increased substrate bias effect [1–4]. Many researchers have adapted multigate silicon on insulator (SOI) technology, which is the potential candidate to replace bulk MOS [5–8]. However, cylindrical gate all-around MOS (GAA-MOS) provides better electrostatic control of the channel; reduces SCEs, floating body effect, and corner effects, and has better scaling option compared to trigate, double-gate and single-gate structures [9–11]. But the key challenge of GAA-MOS technology is to improve the parameters like SS and leakage current, as they lead to higher power consumption and sluggish switching characteristics [12, 13]. The SS of GAA-MOS is limited to 60 mV/decade at room temperature due to the thermionic emission of the MOS structure. The high SS of the GAA-MOSFET results in an increase in a significant amount of OFF-state current leaking in the subthreshold region, which makes the device unsuitable for low power and steeper switching applications.

Tunnel FET (TFET) is the potential solution for low power application, as it has the capability to overcome the SS limit. The carrier movement of TFET mostly depends on the nonlocal band-to-band tunnelling (BTBT) phenomena. However, TFETs can be used in faster switching applications with properly supplied voltage scaling, and the device characteristic does not depend on the temperature variation, unlike MOS [14–16]. TFET results low \text{I\text{OFF}} due to the reduced electric field at the tunnel junction in the OFF state. Therefore in recent times, many researchers have taken an interest in developing the TFET model to study the device physics for further improvement and scaling [17–19]. A number of models have been designed to compute the channel potential and tunneling current of TFET by assuming geometric tunneling paths [20, 21]. Also, a number of 2D single-gate and...
double-gate TFET models have been reported recently, which show the calculation of the tunneling current using the generation rate of the carrier over tunneling volume [22–26].

In this paper a p-channel cylindrical gate TFET (CG-TFET) analytical model is developed that predicts the tunneling current through a minimum tunneling path in a lateral direction. The minimum tunneling distance plays a key role for the estimation of the other electrical parameters, such as SS, ON current and transconductance. The potential distribution and electric field have also been derived for the developed model. The electrical parameters are computed by varying the Si pillar diameter from 4 to 10 nm and scaling the gate oxide thickness from 4 to 2 nm for a channel length of 50 nm.

2. Analytical model

2.1. Device structure

The TFET is a p-i-n diode operating in a reverse bias condition. The structural schematic diagram of the p-channel CG-TFET is shown in Figure 1. The source and drain regions of the CG-TFET model are heavily doped by pentavalent impurity and trivalent impurity, respectively. However, the channel region of the device is made up of intrinsic material. For the present model, the channel is assumed to be very lightly doped of the order of \(10^{15}\). The potential distribution along the channel can be estimated by solving two-dimensional Poisson’s equation under parabolic approximation [10].

The 2D Poisson’s equation in the cylindrical coordinate is expressed as

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi(r, z)}{\partial r} \right) + \frac{\partial^2 \phi(r, z)}{\partial z^2} = \frac{qN_c}{\varepsilon_{si}},
\]

(1)

where \(N_c\) is the doping concentration of the thin silicon cylindrical body, \(\phi(r, z)\) is the electrostatic potential distribution in the intrinsic channel, \(\varepsilon_{si}\) is the dielectric permittivity of silicon and \(q\) is the elementary charge. As the device body is very lightly doped (order of \(~10^{15}\)), the effect of \(N_c\) upon the solution of equation (1) is negligible. So equation (1) takes the form of a 2D Laplace equation as

\[
\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \phi(r, z)}{\partial r} \right) + \frac{\partial^2 \phi(r, z)}{\partial z^2} = 0.
\]

(2)

The potential distribution along the channel is approximately defined as a parabolic equation with the boundary conditions of GAA-MOSFET [12]

\[
\phi(r, z) = a_0(z) + ra_1(z) + r^2a_2(z).
\]

(3)

The boundary conditions are essential to predict the coefficients \(a_0, a_1, a_2\) of the 2nd order polynomial and are finally able to find the solution of the 2D Laplace equation given by equation (2). The required boundary conditions in the intrinsic channel region are approximated as [10].

1. The potential at the center of the cylinder structure varies w.r.t. \(z\) only

\[
\phi(r, z)|_{r=0} = \phi(z) = a_0(z).
\]

(4)

2. The electric field at the center of the thin silicon body is minimal and has a negligible effect on the potential distribution in the channel

\[
E(r, z)|_{r=0} = 0 = a_1(z).
\]

(5)

3. The electric field at the gate oxide–channel interface is maximal and is represented as

\[
E(r, z)|_{r=\frac{r_s}{2}} = \frac{\partial \phi(r, z)}{dr}|_{r=\frac{r_s}{2}} = \frac{C_{ox}(\phi_{GS} - \phi_{FB})}{\varepsilon_{si}} = \frac{t_{si}a_2(z)}{r_s},
\]

(6)

where

\[
\phi(r, z)|_{r=\frac{r_s}{2}} = \phi(z),
\]

\[
\phi_{GS} = V_{GS} - V_{FB},
\]

\[
C_{ox} = \frac{2\varepsilon_{ox}}{t_s \ln \left( 1 + \frac{2t_{ox}}{t_s} \right)}.
\]

Here \(t_{si}\) is the diameter of the cylindrical channel, \(C_{ox}\) is the oxide capacitance, \(t_{ox}\) is the thickness of the SiO\(_2\) layer, \(\varepsilon_{ox}\) is the permittivity of the oxide layer, \(V_{GS}\) is the gate-to-source voltage and \(V_{FB}\) is the flat-band voltage.
Using the boundary conditions in equation (3), we get
\[ \varphi(r, z) = q_1(z) + r^2 \frac{C_{ox}(\varphi_{GS} - q_1(z))}{\epsilon_{si}t_{si}}. \]  
(7)

Equation (2) can be solved for the center of the cylindrical body \( r = 0 \). Substituting equation (7) in (2) and setting \( r = 0 \), we obtain the following one-dimensional (1D) differential equation
\[ \frac{\partial^2 \varphi(z)}{\partial z^2} + \frac{4(\varphi_{GS} - q_1(z))C_{ox}}{\epsilon_{si}t_{si}} = 0. \]  
(8)

The surface potential \( q_1(z) \) is related to the center potential \( q_1(z) \) as [13]
\[ q_1(z) = (H + 1)q_S(z) - H\varphi_{GS}, \]  
(9)

where
\[ H = \frac{\epsilon_{ox}t_{ox}}{4\epsilon_{si}t_{si}}, \quad t_{ox} = \frac{t_{si}}{2} \ln \left(1 + \frac{2t_{ox}}{t_{si}}\right). \]

Differentiating the previous equation
\[ \frac{\partial^2 \varphi(z)}{\partial z^2} = \frac{\partial^2 q_1(z)}{\partial z^2}, \]  
(10)

now equation (8) becomes
\[ \frac{\partial^2 q_1(z)}{\partial z^2} + \frac{4(\varphi_{GS} - q_1(z))C_{ox}}{\epsilon_{si}t_{si}} = 0, \]  
(11)
\[ \frac{\partial^2 q_1(z)}{\partial z^2} + \frac{\varphi_{GS} - q_1}{\lambda_c^2} = 0, \]  
(12)

where \( \lambda_c \) is known as the characteristic length of the cylindrical gate and is mathematically defined as
\[ \lambda_c = \sqrt{\frac{t_{si}^2}{8C_{ox}}} \ln \left(1 + \frac{2t_{ox}}{t_{si}}\right). \]  
(13)

2.2. Surface potential distribution
The differential equation (12) can be solved by using an auxiliary equation to obtain the surface potential of the cylindrical channel as
\[ q_1(z) = c_1 e^{kz} + c_2 e^{-kz} - \varphi_d, \]  
(14)

where \( \varphi_d = -\varphi_{GS} \) and \( k = 1/\lambda_c \).

For the previous expression the coefficients \( c_1 \) and \( c_2 \) can be calculated by using the boundary conditions at the source and drain ends. The surface potential at the source end \( z = 0 \) is defined as the built-in potential, which is the amount of band bending of valence band and conduction band at the source-channel interface for \( \varphi_{GS} = 0 \). Similarly, the potential at the channel-drain interface \( z = z_{max} = L \) is the sum of the built-in potential \( \varphi_{bi} \) and drain voltage \( \varphi_{DS} \), as the channel is inverted at the drain end.

The necessary sufficient boundary conditions are [18]
\[ q_1(z) \bigg|_{z=0} = \varphi_{bi}, \]  
\[ q_1(z) \bigg|_{z=z_{max}=L} = \varphi_{bi} + \varphi_{DS}. \]  
(15)

Equating equation (14) using the previous boundary conditions
\[ c_1 = \frac{1}{2} \sinh(kL) \left[ \varphi_{bi}(1 - e^{-kL}) \right. \]  
\[ \left. + \varphi_d(1 - e^{kL}) + \varphi_{DS} \right], \]  
(16)
\[ c_2 = -\frac{1}{2} \sinh(kL) \left[ \varphi_{bi}(1 - e^{kL}) \right. \]  
\[ \left. + \varphi_d(1 - e^{-kL}) + \varphi_{DS} \right]. \]  
(17)

2.3. Electric field analysis
The electric field of the channel can be derived by differentiating electrostatic potential distribution \( \varphi \) with respect to \( r \) and \( z \),
\[ E_r(r, z) = -\frac{\partial \varphi(r, z)}{\partial r} = -2r\varphi_z(z) \]  
\[ = -2r(\varphi_{GS} - q_1)C_{ox} / t_{si}\epsilon_{si}, \]  
(18)
\[ E_z(r, z) = -\frac{\partial \varphi(r, z)}{\partial z} \]  
\[ = -\frac{\partial q_1}{\partial z} \]  
\[ = -c_1k e^{kz} + c_2ke^{-kz}. \]  
(19)

However, for a TFET model, the tunneling process is dominant in the lateral \( z \)-direction compared to the radial direction [27]. So the lateral electric field along the length of the channel is considered in the next section to calculate the tunneling current.

2.4. Tunneling phenomena
The tunneling of the charge carrier at the source end starts only when the conduction band of the source gets aligned with the valence band of the intrinsic channel region. The shortest tunneling distance \( (L_{tunn}) \) is the lateral distance between the source-channel interface \( (z=0) \) and the point in the channel where the surface potential changes by an amount of unit bandgap energy per elementary charge \( (E_g/q) \). However, the shortest tunneling distance plays a crucial role in finding the amplitude of the tunneling current in the device.

The gate voltage has a significant effect on the tunneling phenomena as shown in figure 2. At low gate voltage, there is a small amount of band bending of the valence band and conduction band. So the current is negligible due to the
The absence of BTBT of the charge carrier. For a critical value of the gate voltage known as the threshold voltage \((V_{th})\), the conduction band of the source and the valence band of the channel are in line to each other. For \(V_{GS} > V_{th}\), the tunneling probability increases, which improves the BTBT current in the channel. The BTBT drain current increases exponentially due to the improvement in tunneling volume as depicted by the area under the solid lines in figure 2(b).

\[ L_{tunn} = \frac{1}{k} \ln \left( \frac{A - \sqrt{A^2 - 4c_1c_2}}{2c_1} \right), \quad \text{(23)} \]

where \(L_{tunn}\) is the shortest tunneling distance.

Table 1. Subthreshold slope for CG-TFET in subthreshold region.

| Drain voltage (V) | Gate oxide thickness (nm) | Si pillar diameter (nm) | Subthreshold slope (mV/decade) |
|-------------------|---------------------------|-------------------------|-------------------------------|
| –1                | 2                         | 10                      | 27                            |
| –1                | 3                         | 10                      | 44                            |
| –1                | 4                         | 10                      | 56                            |
| –1                | 4                         | 8                       | 46                            |
| –1                | 4                         | 6                       | 38                            |

The corresponding potential values for \(z = 0\) and \(z = L_{tunn}\) are obtained from the defined boundary conditions

\[ \varphi_{sc0} \left( z \right) \big|_{z=0} = \varphi_{0}(0) = V_{bi}. \quad \text{(21)} \]

\[ \varphi_{sc} \left( z \right) \big|_{z=L_{tunn}} = \varphi \left( L_{tunn} \right) + \frac{E_{f}}{q} \left( c_1 e^{L_{tunn}} + c_2 e^{-L_{tunn}} - \varphi_{di} - \frac{E_{f}}{q} \right), \quad \text{(22)} \]

where \(\varphi_{sc0} (z)\) and \(\varphi_{sc} (z)\) are the conduction potential of the source and valence potential of the channel.

The value of the shortest tunneling distance can be obtained from the critical threshold condition as

\[ L_{tunn} = \frac{1}{k} \ln \left( \frac{A - \sqrt{A^2 - 4c_1c_2}}{2c_1} \right), \quad \text{(23)} \]

where \(A\) is the device-dependent constant and expressed as

\[ A = \varphi_{di} - \frac{E_{f}}{q} + V_{bi}. \]

However, the shortest tunneling distance can be reduced by using low bandgap material and increasing the gate potential \((V_{GS})\), which increases the tunneling volume in the channel region. The higher the tunneling volume, the greater the ON current of the device. For a constant gate voltage, the tunneling volume is not affected by drain voltage.

2.5. Drain current analysis

The drain current of the proposed model is calculated analytically by Kane’s model, which uses a nonlocal BTBT approach. However, Kane’s model [28] is used to find the rate of generation of carrier \((G_{tunn})\) tunneling from source to drain along the channel as:

\[ G_{tunn} = A_{kane} \left( E_{avg} \right)^{\theta} e^{-\left( \frac{E_{gap}}{kT} \right)}, \quad \text{(24)} \]
where \( A_{kane} \) and \( B_{kane} \) are tunneling-dependent parameters and the default values of \( A_{kane} = 4 \times 10^{15} \text{m}^{-1/2} \text{V}^{-5/2} \) and \( B_{kane} = 1.9 \times 10^8 \text{V}^{-1} \) [29]. \( \beta \) is the material-dependent parameter and its value depends on the type of tunneling, i.e., 2.5 for the indirect tunneling and 2 for direct tunneling [29]. However, in the present analysis the value of \( \beta \) is considered as 2. \( E_{\text{avg}} \) is the average electric field over the tunneling volume and is expressed as

\[
E_{\text{avg}} = \frac{E_g}{qL_{\text{path}}},
\]

where \( L_{\text{path}} \) is the length of the BTBT tunneling path, which varies over the tunneling volume in the \( z \)-direction. From figure 2, the \( L_{\text{path}} \) is described as the path between two lateral points \( z_1 = L_{\text{tunn}} \) and \( z_2 \).
Now the drain current can be computed with the help of the BTBT generation rate

\[
I_D = \int G_{\text{BTBT}} \, dv
\]

\[
= q \int_0^{z_1} \int_{z_1}^{z_2} A_{kane} E_z (E_{\text{avg}})^{\beta-1} e^{-\left(\frac{B_{kane}}{E_{\text{avg}}}\right)} \, dz \, dr.
\]

Substituting the value of the lateral electric field and the average tunneling field from equations (19) and (25)

\[
I_D = \frac{q t_{sl} E_D^{\beta-1} A_{kane}}{q^{\beta-1}} \left[ \int_{z_1}^{z_2} -c_1 k \left(\frac{k B_{kane}}{E_{\text{avg}}}\right)^{\beta-1} \, dz \right]
\]

Figure 7. $I_D$-$V_{GS}$ characteristics for the proposed p-channel CG-TFET. The drain current is plotted on (a) linear scale and (b) logarithmic scale.

Figure 8. $I_D$-$V_{DS}$ characteristics for p-channel CG-TFET. The drain current is plotted on (a) linear scale and (b) logarithmic scale.

Figure 9. Impact of gate oxide scaling on drain current $I_D$ versus $V_{GS}$ (a) and versus $L_{\text{tunn}}$ (b).
Here, the tunneling of the charge carrier takes place between two lateral points \( z_1 = L_{tunnel} \) and \( z_2 \). Between the two boundaries along the \( z \)-direction, the effect of the polynomial term \( (z^{\beta-1}) \) is negligible as compared to the exponential term \( e^{-qB_{tunnel}z/E_g} \). So the drain current is obtained by integrating equation (27) over the tunneling interval and neglecting the polynomial term; thus, we get

\[
I_D = \frac{q|\Delta z|E_g A_{lane}}{q} \left[ \left\{ -\frac{e^{kz}}{k} \right\} \left( P_{z_2} - P_{z_1} \right) \right. \\
- \left. \left( \frac{c_2 k}{k + qB_{tunnel}E_g} \right) \left( Q_{z_2} - Q_{z_1} \right) \right] 
\]

where \( P_z \) and \( Q_z \) are expressed as

\[
P_z = e^{\left( \frac{qB_{tunnel}E_g}{k} \right) z}, \quad Q_z = e^{\left( \frac{qB_{tunnel}E_g}{k} \right) z}.
\]

As \( z_2 > z_1 \), it is noted that the exponential coefficient \( P_{z_2} \ll P_{z_1} \) and \( Q_{z_2} \ll Q_{z_1} \). In the present model, the current

Figure 10. Impact of cylinder diameter scaling on drain current \( I_D \) versus \( V_{GS} \) (a) and versus \( L_{tunnel} \) (b).

Figure 11. Variation of sub-threshold slope with gate voltage in sub-threshold region.

\[
I_D = \frac{q|\Delta z|E_g A_{lane}}{q} \left[ \left\{ -\frac{e^{kz}}{k} \right\} \left( P_{z_2} - P_{z_1} \right) \right. \\
- \left. \left( \frac{c_2 k}{k + qB_{tunnel}E_g} \right) \left( Q_{z_2} - Q_{z_1} \right) \right] 
\]

where \( P_z \) and \( Q_z \) are expressed as

\[
P_z = e^{\left( \frac{qB_{tunnel}E_g}{k} \right) z}, \quad Q_z = e^{\left( \frac{qB_{tunnel}E_g}{k} \right) z}.
\]

As \( z_2 > z_1 \), it is noted that the exponential coefficient \( P_{z_2} \ll P_{z_1} \) and \( Q_{z_2} \ll Q_{z_1} \). In the present model, the current

Figure 12. Variation of transconductance as a function of gate voltage for different gate oxide thicknesses in CG-TFET (a) linear scale and (b) logarithmic scale.
analysis is carried out by neglecting the minimal effects of \( P_z \) and \( Q_z \) and instead using the shortest tunneling distance \( z_1 = L_{tunn} \).

\[
I_D = I_0 \left[ P_{z1} \left( \frac{c_1 k}{k + \frac{q B_{kane}}{E_g}} \right) + Q_{z1} \left( \frac{c_2 k}{k + \frac{q B_{kane}}{E_g}} \right) \right],
\]

where \( I_0 \) is the dc current that only depends on constant parameters and is defined as

\[
I_0 = \frac{q v_A E_g A_{kane}}{q}.
\]

2.6. Subthreshold swing (SS)

SS is a feature of a MOSFET’s current–voltage characteristic in the sub-threshold region \( (V_{GS} < V_{th}) \) and is defined as the slope of logarithmic drain current w.r.t. gate voltage at a constant drain voltage. The inverse of this slope is usually referred to as SS in mV/decade

\[
SS = \frac{\partial V_{GS}}{\partial (\log I_D)} = \left( \frac{\partial (\log I_D)}{\partial V_{GS}} \right)^{-1}.
\]

The optimum value of the SS of a conventional MOSFET is 60 mV/decade at room temperature (300 K). It is always desirable to have a small SS, as it improves the \( \frac{I_{on}}{I_{off}} \) ratio by reducing the leakage of the OFF state current. Also the low SS or steep subthreshold slope of a device indicates the faster switching behavior, i.e., faster transition between OFF state and ON state. SS can be computed by substituting the value of \( I_D \) in equation (32)

\[
SS = \left( \frac{\partial (\log I_D)}{\partial V_{GS}} \right)^{-1} = \left( \frac{\partial}{\partial V_{GS}} \left[ \frac{c_1 k h P_z}{k - \frac{q B_{kane}}{E_g}} \right] \right)^{-1} + \left( \frac{c_2 k I_0 Q_z}{k + \frac{q B_{kane}}{E_g}} \right)^{-1},
\]

where

\[
Y_1 = \frac{I_0 k P_z}{k - \frac{q B_{kane}}{E_g}}, \quad Y_2 = \frac{I_0 k Q_z}{k + \frac{q B_{kane}}{E_g}}.
\]

It is noted that the model offers an SS of 26∼40 mV/decade compared to the GAA-MOS limit of 60 mV/decade over a wide range of gate voltages, as shown in table 1. This leads to a reasonable amount of improvement in \( \frac{I_{on}}{I_{off}} \).

2.7. Transconductance

Transconductance \( (g_m) \) is the transfer characteristics of the device and is calculated by differentiating equation (30) w.r.t. \( V_{GS} \) at constant \( V_{DS} \).

\[
g_m = \frac{\partial I_D}{\partial V_{GS}} \Bigg|_{V_{DS} = {\text{const}}} = \frac{-Y_1 (1 - e^{-kL}) + Y_2 (1 - e^{kL})}{2 \sinh(kL)}.
\]
transconductance of CG-TFET as depicted in figures 12 and 13.

3. Results and discussion

Figure 3 illustrates the surface potential profile in the cylindrical p-TFET for different gate voltages. The potential is pinned to $V_{bi}$ and $V_{th} = V_{DS}$ at the source and drain end as per the boundary conditions defined in equation (15). As the gate voltage increases for constant drain voltage, the potential in the intrinsic channel region improves. However, we get a constant surface potential at the middle of the channel. This is due to the saturating effect of gate control over the channel. Also the variation of surface potential near the tunneling junction is less because the charge carriers vary less. The slope of the potential distribution decreases along the channel from source to drain end.

Figure 4 shows the behavior of lateral and radial electric fields for different gate voltages for a 50 nm channel. It is clearly seen from the figure that the electric field varies nonlinearly at the source and drain ends. The variation of the field arises at the source-channel interface because of the tunneling phenomena, and the same results at the drain interface are due to the influence of the drain potential. The constant potential in the middle of the cylindrical body gives rise to a constant electric field in both directions. The radial and lateral field reaches zero at the middle of the channel due to zero slope potential.

The shortest tunneling distance as a function of gate and drain voltage is shown in figure 5. As the gate voltage increases beyond the threshold level, the tunneling of charge carriers from source to channel improves. Thus, $L_{tunn}$ is achieved at a very small lateral distance from the source end as depicted in figure 5. But $L_{tunn}$ does not change significantly due to variation of the drain voltage (figure 5(b)). However, the drain output voltage plays an important role in deciding the tunneling volume. For higher $V_{GS}$, small $L_{tunn}$ is achieved, which increases the tunneling volume based on drain voltage.

As the gate voltage increases beyond the threshold, $L_{tunn}$ reduces for a fixed gate oxide thickness and cylindrical body diameter. However, as the gate oxide thickness ($t_{ox}$) is scaled from 4 to 2 nm for radii 5 nm, the tunneling is achieved faster due to reduction of $L_{tunn}$ as depicted in figure 6(a), which improves the device performance by increasing BTBT current. So at low gate oxide thickness, the gate has a greater impact on the channel and threshold achieved at a low $V_{GS}$, enabling flow of charge carriers. Similarly, figure 6(b) shows the variation of $L_{tunn}$ versus $V_{GS}$ for different Si body diameters. When the radius of the cylindrical body goes on reducing for constant $t_{ox}$, the effect of the gate over the cylindrical body is dominant compared to the drain and thereby reduces $L_{tunn}$ marginally. However, it is clearly evident from figure 6 that the effect of $t_{ox}$ scaling has a greater impact compared to Si pillar diameter scaling on TFET ON current performance.

Figures 7 and 8 show the graph of $I_{D}-V_{GS}$ and $I_{D}-V_{DS}$ characteristics for CG-TFET. Here it is observed that the tunnel drain current improves exponentially at the ON condition ($V_{GS}>V_{th}$) due to the dominant tunneling process. Figure 7(b) displays the logarithmic ON current that helps to find the OFF current and SS in the sub-threshold region ($V_{GS}<V_{th}$). Table 1 displays the measured SS in the sub-threshold region for different $t_{ox}$ and $t_{si}$. However, at higher gate voltages, the tunneling volume gradually saturates and leads to the saturating drain current.

Figure 9 displays the effect of gate oxide thickness on the drain current analysis of the model. It is clearly seen that for small gate oxide thickness, the tunneling current is higher as depicted in figure 9(a). This is due to the small value of the minimum tunneling distance that leads to a large tunneling volume and maximum ON current. For a constant value of gate oxide thickness, the tunneling current increases sharply with small $L_{tunn}$ as in figure 9(b). However, as the oxide thickness is scaled from 4 nm to 2 nm, the minimum tunneling distance ($L_{tunn}$) is achieved early, at a 3 nm distance from the source end, which improves the non-local BTBT tunneling of charge carriers.

The effect of cylindrical body thickness on drain current analysis of the model w.r.t. gate voltage and shortest tunneling distance, respectively, is depicted in figure 10. The BTBT tunneling takes place faster for small radii and conversely improves the tunneling current. But in the sub-threshold region ($V_{GS}<V_{th}$), the effect of the variation of the cylindrical body diameter is insignificant on drain current due to the absence of BTBT tunneling of carriers. However, the present TFET model produces a steep SS in the range of 27–56 mV/decade as presented in table 1. SS can also be calculated for different gate voltages in the sub-threshold region as shown in figure 11.

Figure 12 shows the transconductance as a function of gate voltage at a constant drain voltage of $-1$ V. It is clearly evident from figure 12(a) that for a particular value of oxide thickness, the transconductance improves above the threshold value of the gate bias. This is due to the fact that for $V_{GS}>V_{th}$, the increased tunneling current saturates the mobile charge carriers and decreases the resistance and results in an increment of transconductance beyond the threshold voltage. Figure 12(b) shows the logarithmic values of transconductance for different gate oxide thickness. However, the transconductance improves further by reducing the gate oxide thickness due to low resistance and small tunneling distance. Further, figure 13(a) displays the relationship between transconductance and $L_{tunn}$, which concludes that 2 nm oxide thickness produces high transconductance compared to 4 nm, as $L_{tunn}$ is achieved earlier.

The relationship between transconductance and $L_{tunn}$ for different diameters of the cylindrical body is plotted in figure 13(b). The transconductance of the device enhances with the reduction of the cylinder radii, as the tunneling current increases for a large tunneling volume.

CG-TFET produces low SS (SS < 60 mV/decade), better gate oxide thickness scalability and cylindrical body diameter scalability. Therefore, this model can be a potential candidate for ultra-low-power CMOS applications in the near future.
4. Conclusion

In this paper, an accurate, physics-based model for p-channel CG-TFET is developed. The tunneling current in the proposed device is derived using a generalized Kane’s model and expressed as a function of gate voltage. The drain current shows the impact of shortest tunneling distance, gate oxide thickness and cylindrical body diameter. Also, the improved SS that resulted for the present model (27~56 mV/decade) allows the device to be a promising candidate for low-power and high-speed applications.

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