Wire Recycling for Quantum Circuit Optimization

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Quantum information processing is expressed using quantum bits (qubits) and quantum gates which are arranged in the terms of quantum circuits. Here, each qubit is associated to a quantum circuit wire which is used to conduct the desired operations. Most of the existing quantum circuits allocate a single quantum circuit wire for each qubit and, hence, introduce a significant overhead. In fact, qubits are usually not needed during the entire computation but only between their initialization and measurement. Before and after that, corresponding wires may be used by other qubits. In this work, we propose a solution which exploits this fact in order to optimize the design of quantum circuits with respect to the required wires. To this end, we introduce a representation of the lifetimes of all qubits which is used to analyze the respective need for wires. Based on this analysis, a method is proposed which “recycles” the available wires and, by this, reduces the size of the resulting circuit. Numerical tests based on established reversible and fault-tolerant quantum circuits confirm that the proposed solution reduces the amount of wires by more than 90% compared to unoptimized quantum circuits. Source code is available at [http://github.com/alexandrupaler/wirerecycle](http://github.com/alexandrupaler/wirerecycle).

I. INTRODUCTION

Quantum computing [1] is an emerging technology that is recently receiving significant attention due to its ability to solve several classes of problems which are computationally inefficient on standard classical computers. Current applications of quantum computing range from integer factorization, unstructured search [2] and quantum chemistry [3].

Corresponding solutions are theoretically described in terms of quantum algorithms which, in turn, are realized as quantum circuits. In contrast to classical circuits, a quantum circuit works with so-called qubits that cannot only assume the values 1 and 0, but also their superposition. Here, operations to be conducted are represented in terms of quantum gates. Electronic Design Automation in this domain deals with questions how to synthesize, optimize, and verify corresponding quantum circuits [4].

Current efforts are mainly motivated by the conclusion that practical quantum circuits need to incorporate a large amount of error-correction techniques because the quantum hardware is highly susceptible to environmental noise [5]. Practical computations necessitate a high amount of hardware resources, which could be lowered by optimizing quantum circuits [6, 7]. Accordingly, existing quantum circuit optimization methods focus on either reducing the number of qubits or the number of particular gates, or both [8].

However, this view ignores the fact that, eventually, quantum circuits are synthesized so that each single qubit is associated to a quantum circuit wire. While the qubit is a representation of quantum information, quantum circuit wires represent the structural property of a circuit. More precisely, in order to realize a quantum algorithm, a quantum circuit wire is instantiated for each qubit and represents the passage of time. Then, the operations to be conducted on this qubit are realized in terms of quantum gates applied to the respective wire. Because of the one-to-one mapping between qubits and wires, the quantum circuit terminology often accepts both terms as being equivalent terms.

But this perspective and the existing design scheme frequently lead to quantum circuits of considerable size with respect to the needed quantum circuit wires. In fact, qubits are usually not needed during the entire computation of an algorithm, but only during their lifetime, i.e. between their initialization and measurement. Before and after that, the quantum circuit wire may be used by other qubits. But, thus far, existing design solutions do not exploit this fact and create a dedicated quantum circuit wire for each qubit – obviously leading to a significant overhead.

In this work, we propose to “decouple” the terms qubit and quantum circuit wire and exploit the potential of recycling wires in the design of quantum circuits. To this end, a method is proposed which associates multiple qubits to the same wire, so that individual qubit lifetimes do not overlap in time. While recycling-methods have already been proposed before in [9] (specific quantum algorithm perspective) and in [10] (specific quantum computing architecture perspective), this work exploits recycling for the design of arbitrary quantum circuits. Similar work from Parent, Roetteler and Svore [11], known as REVS, also examines resource recycling that can be integrated with quantum compilers such as LIQi[1].

The proposed methods clearly show that quantum circuit optimization should focus on the number of wires instead of the number of qubits. In fact, wire recycling as proposed in this work generates a quantum circuit
with the same number of qubits but with less wires and, hence, with a substantially lower hardware requirement. In the best case, the amount of quantum circuit wires can be reduced by more than 90%. The reduction is proportional to the amount of resources required to implement fault-tolerant quantum circuits, where error correction techniques are heavily used.

The paper is organized as follows: Sec. II will briefly introduce the formalism of quantum circuits. The idea of wire recycling is introduced and illustrated in Sec. III while Sec. IV provides a detailed description of the proposed optimization method. Conclusion and future work are discussed in Sec. VII after having analyzed the performance of the method using relevant reversible and quantum circuits in Sec. V.

II. BACKGROUND

Quantum computations are reversible by definition, meaning that the inputs can be computed from the outputs by applying the circuit backwards. This is possible because (1) quantum circuit gates have an equal number of inputs and outputs and (2) gates implement a specific type of operation. Classical circuits can be made reversible by using gates implementing bijective Boolean functions, and thus having an equal number of inputs and outputs as well. Classical reversible circuits do not have the computational power of their quantum counterparts, but are described using the same circuit formalism and often serve as initial blueprint.

In the following we consider reversible circuits being a subtype of quantum circuits.

A. Initializations, Gates and Measurements

A quantum circuit is executed by applying a time ordered set of gates, which are generally written from left to right. A time axis running left-to-right can be linked to any quantum circuit, so that each circuit operation can be identified at a certain point in time. Inputs are on the left and outputs on the right. Fig. 1 illustrates corresponding examples. A quantum circuit implements three types of operations: 1) qubit initialization; 2) quantum gates which operate on qubits; 3) qubit measurement. The state of a qubit $q$ is represented as the vector $|q⟩ = α_0|0⟩ + α_1|1⟩$, where $α_0$ and $α_1$ are complex numbers (called amplitudes) that satisfy $|α_0|^2 + |α_1|^2 = 1$. The vectors $|0⟩$ and $|1⟩$ are states analogue to the classical bits 0 and 1, but a qubit can be in a superposition of these two states, where it is both 0 and 1 (e.g. when $α_0 ≠ 0$ and $α_1 ≠ 0$).

Definition 1 A quantum circuit is a sequence of operations applied to a set of qubits.

Qubits are initialized before any gates can be applied. Commonly used initial states, particularly in the context of error corrected quantum computation are $|0⟩$, $|1⟩$, $|+⟩ = \frac{1}{\sqrt{2}}(|0⟩ + |1⟩)$, $|Y⟩ = \frac{1}{\sqrt{2}}(|0⟩ + i|1⟩)$ and $|A⟩ = \frac{1}{\sqrt{2}}(|0⟩ + e^{iπ/4}|1⟩)$.

Quantum gates manipulate the state of qubits, but in contrast to classical gates, quantum gates always have an equal number of inputs and outputs. As a result, quantum gates can operate on single or multiple qubits. Multi-qubit gates are of two types: controlled and uncontrolled. Assuming an $m$-qubit gate named $G$ is applied on the qubit set $Q = \{q_0, \ldots, q_m\}$. If $G$ would be controlled then the function $O_c$ is applied to the qubit subset $C \subset Q$ (target qubits) depending on the state of the qubit subset $C \subseteq Q$, $C \cap T = \emptyset$, $C \cup T = Q$ (control qubits). If $G$ is uncontrolled, then the function $O_u$ would be applied to all $Q$. The controlled NOT (CNOT) operation between two qubits $Q = \{c, t\}$, where $C = \{c\}$ and $T = \{t\}$, will perform the NOT operation to $T$ only if the state of the qubits in $C$ is $|1⟩$, thus $\text{cnot}(c, t) = (c, t \oplus c)$, where $\oplus$ is the Boolean XOR function.

Qubit measurement is the quantum counterpart of reading the value of a classical bit. The standard measurement in quantum computation, referred to as a Z-basis measurement, measures if the qubit is in the $|0⟩$ or $|1⟩$ state, collapsing any superposition inconsistent with the measurement result. Another type of measurement is an X-basis measurement, which measures if the qubit is in the $|+⟩ = \frac{1}{\sqrt{2}}(|0⟩ + |1⟩)$ state.

Quantum gates are chosen from an universal gate set sufficient for approximating any quantum computation with arbitrary precision. The set of all single qubit quantum gates together with CNOT forms an universal gate set. Classical reversible circuits are generally specified using the Toffoli gate, which is a 3-qubit gate applying the NOT operation on the target $t$ if both control qubits $c_1, c_2$ are $|1⟩$. From a Boolean perspective the Toffoli gate implements the function $\text{toffoli}(c_1, c_2, t) = (c_1, c_2, t \oplus c_1c_2)$. However, the Toffoli gate is not quantum computing universal but only classically universal (can be used to implement NAND).

B. Ancilla Qubits

Quantum circuit qubits can be classified into I/O-qubits and ancillae qubits. The total number of qubits of a circuit is the sum between the number of I/O- and an-
cillae qubits. If a circuit would be abstracted as a black box, the I/O-qubits are the interface to the box (inputs and outputs) and the ancillae are internal to the box. Circuit inputs and outputs are configurable with respect to the states used for qubit initialization and qubit measurement (e.g. can be $|0\rangle$, $|1\rangle$ or $|+\rangle$), whereas ancillae are initialized and measured into specific states (e.g. always $|A\rangle$). Ancillae are used as temporary workbenches [13] or for increasing the fault-tolerance of the implemented computation [13].

**Definition 2** An input ancilla is a qubit always initialized in the same state, irrespective if its measurement is configurable or not. An output ancilla is a qubit always measured in the same state, irrespective if its initialization is configurable or not.

C. Circuit Wires and Qubit Lifetime

The temporal ordering of operations introduced by a quantum circuit determines the lifetime of a qubit.

**Definition 3** The lifetime of a qubit is spanned between its initialization and measurement points in time.

The lifetime consists of three stages: a passive, an active and another passive stage. The length (along the time axis linked to the circuit) of a quantum circuit wire is the abstraction of a qubit’s lifetime.

The active stage is the relevant one in a qubit’s lifetime and exists between the first and the last gate affecting the qubit. The first passive stage exists between the qubit’s initialization and the first gate, while the second passive stage exists between the last gate and the qubit’s measurement.

### III. WIRE RECYCLING

In this work, we propose to recycle quantum circuit wires in order reduce the overhead of quantum circuits. The main idea is to compute the temporal ordering of all the relevant qubit lifetimes and, afterwards, arrange them in a fashion so that the corresponding quantum circuits wires are used and re-used (recycled) as best as possible.

Note thereby that wire recycling can be applied to ancillae qubits only (only these will be marked with the measurement symbol \(\parallel\)), since the lifetime of I/O-qubits is spanned along the entire time axis. The general idea is illustrated by means of the following example:

**Example 1** Fig. 2 shows a quantum circuit with eight operations: three qubit initializations (two ancilla, one I/O-qubit), two CNOTs and three qubit measurements (two ancilla, one I/O-qubit with unmarked measurement). The first CNOT gate applied on the qubits \(|q_0\rangle\) and \(|q_1\rangle\) is applied before the CNOT affecting \(|q_1\rangle\) and \(|q_2\rangle\), while each of the qubits needs to be firstly initialized and finally measured. The lifetime of qubit \(q_0\) starts at the beginning of the first quantum circuit wire, includes the application of the first CNOT where the wire is acting as control and ends at the rightmost wire end point. The lifetime of qubit \(q_1\) starts at the beginning of the second wire, includes the application of the first CNOT and the application of the second CNOT. Its lifetime ends at the rightmost end point of the second wire. Hence, the lifetime of the third qubit \(|a_2\rangle\) does not overlap with the lifetime of the first qubit \(|a_0\rangle\) and one quantum circuit wire can be recycled. This yields the quantum circuit as shown in Fig. 2.

![Fig. 2](image)

**FIG. 2** Wire recycling correctness by example: a) a quantum circuit with three wires including two ancillae \(a_0\) and \(a_2\) and one I/O-qubit \(q_1\); b) computation is left unchanged, but the \(a_2\) ancilla is initialized after the first CNOT is performed; c) the equivalent computation, but requiring only two wires because both ancillae share the topmost wire. The lifetime of the third qubit \(|a_2\rangle\) does not overlap with the lifetime of the first qubit \(|a_0\rangle\).

### IV. METHOD

In order to introduce wire recycling an equivalent representation of arbitrary quantum circuits is introduced in the form of graphs expressing the temporal relation between circuit operations. The structural analysis of the graphs will be used afterwards to devise two recycling heuristics.

A. Causal Graph

The temporal ordering of quantum circuit operations can be modeled using the \(\to\) operator by writing \(g_1 \to g_2\) if gate \(g_1\) needs to be executed before gate \(g_2\). The situation exists if the gate \(g_2\) takes as input one of the outputs of \(g_1\). Therefore, any qubit initialization will precede a gate, and, for example, we can write input1 \(\to\) g3, if the gate \(g_3\) is applied on the freshly initialized qubit existing at the circuit’s input named input1. For this reason, qubit measurements will not precede any operation, but will always have their own predecessors. For example, \(g_4 \to\) output2 indicates that the output qubit of gate \(g_4\) existing on the circuit’s output named output2 is measured. The \(\to\) operator is transitive, because if \(a \to b\) and \(b \to c\), then \(a \to c\).

All the temporal relations between quantum circuit operations modeled using the \(\to\) operator can be abstracted
by causal graphs. A quantum circuit is represented by a graph, where each node has two associated attributes: 1) type (an operation identifier), and 2) wires (the set of wires linked to the qubits operated by the gate). A temporal ordering between two circuit operations is established if one of the operations is based on the output of the other. Thus, if two operations are applied to the same qubit, an edge or a chain of edges will exist between the corresponding operation nodes. Each path in a causal graph represents a chain of circuit operation precedences.

**Definition 4** A quantum circuit causal graph is a directed acyclic graph where each circuit operation (initialization, gate, measurement) is abstracted by a node, and edge directions indicate the relative temporal ordering of the circuit operations.

**Observation 1** A graph edge is abstracting a quantum circuit wire segment existing between the circuit operations represented by the adjacent graph nodes.

An initial causal graph does not contain any direct edges between output and input nodes: there is no precedence established between qubit initializations and measurements of different qubits. Thus, initially, the precedence of qubit lifetimes is not known.

**Example 2** In Fig. 3, the lifetime of $|a_0\rangle$ (top most qubit in Fig. 3a) is represented by the subgraph having input0 as root and output0 as leaf. The lifetime of $|a_2\rangle$ is the subgraph having input2 as root and output2 as leaf. It can be concluded that the lifetime of $|a_0\rangle$ can precede the lifetime of $|a_2\rangle$, so that the qubits can share the top most wire (Fig. 3).

### B. Recycling Algorithm

A circuit’s causal graph contains all the information necessary for wire recycling where an input graph having each qubit on a distinct wire is gradually transformed to an output graph having multiple qubits on the same wire. We propose two optimization heuristics for the transformation of graphs. Both heuristics are applications of the same transformation rule, which is the result of an observation about the graphs’ structure.

#### 1. Relation Between Input and Output Nodes

There are situations when a qubit is measured before another qubit is initialized, and this can be modeled by a supplemental graph edge connecting the corresponding qubit’s output node to the other qubit’s input node. When adding such an edge it has to be guaranteed that the two nodes are not elements of a direct path. Otherwise, two equivalent problems arise: 1) the graph contains a cycle which is not allowed because causal graphs are acyclic; 2) although the initialization takes place before the measurement, the edge indicates that the measurement precedes the initialization, which is impossible.

**Observation 2** A direct edge can be drawn between an output and an input node, if no direct path starts at the input and ends at the output node.

Observation 2 is the basis of the causal graph transformation rule (Fig. 4, where an edge is added between an output allowed to precede an input (Fig. 4). If the input and the output nodes referenced distinct wires (e.g. $w_1$ and $w_2$), the input graph can be transformed (Fig. 4), so that both the gates address the same wire, e.g. $w$: 1) gate $g_1$ is executed; 2) its output is measured on wire $w$ (node output), 3) a new qubit is initialized on wire $w$ (node input), 4) gate $g_2$ is executed. The result is that $w_1$ and $w_2$ are treated as segments of $w$ which abstracts the lifetime of two distinct qubits: the one measured after $g_1$, and the one initialized before $g_2$. The passive stages of $w_1$ and $w_2$ were shortened without influencing the computation, the wires do not overlap in time and are arranged so that $w_1 \rightarrow w_2$.

#### 2. Main algorithmic routine

The central aspect of wire recycling is to determine which qubit measurements are potential candidates to precede qubit initializations. In Alg. 1 an unoptimized circuit is used to generate a causal graph $\text{cg}$ and to infer the nodes corresponding to the input ancillae set ($\text{IA}$) and the output ancillae set ($\text{OA}$). It is necessary to know how many ancilla output nodes succeed each ancilla input node ($n_a$), because in the light of Observation 2, only outputs preceding inputs can be connected by edges.
The highest chances of successfully applying the graph transformation rule is for those ancilla inputs used at the latest points in time. Such inputs reach the least outputs and, thus, a maximal number of outputs precedes them. Therefore, for each ancilla input the maximum number of preceding outputs \(|OA| - n_a\) is computed.

The order in which input nodes are connected to outputs nodes is dictated by a priority queue data structure where input nodes are sorted based on the corresponding value of \(|OA| - n_a\). For each found output node, the input and all the graph nodes following it will use the same wire as the output.

Because each causal graph node knows the wire(s) it operates on, the notation \(a.wire\) is to be interpreted as the wire label of node \(a\). In the main algorithmic routine of Alg. 1, after an input node \(a\) is connected to an output node \(o\), the wire label of node \(a\) is replaced by the wire label of node \(o\), because \(a\) will operate on the wire of \(o\).

Finally, after transforming \(cg\) by each transformation rule, the queue \(Q\) is recomputed to reflect the new graph structure.

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**Algorithm 1 Qubit Recycling Algorithm**

**Require:** Input circuit \(circ\)
- \(cg\) = causal graph of \(circ\)
- \(IA\) = the set of all ancilla input nodes in \(cg\)
- \(OA\) = the set of all ancilla output nodes in \(cg\)
- \(N = \{ n_a | a \in IA, n_a \text{ the number of nodes } o \in OA \text{ preceded by } a \}\)
- \(Q = \text{queue constructed from } IA \text{ with elements sorted by priority } |OA| - n_a\)

**while** \(Q\) not empty **do**
- \(a = \text{Read and remove topmost input node from queue } Q\)
- \(o = \text{Result of searching for a preceding output node}\)
  - **if** Found \(o \in OA\) **then**
    - Draw edge between \(o\) and \(a\)
    - Replace at successors of \(a\): \(a.wire\) with \(o.wire\)
  - **end if**
  - Update \(Q\) to reflect the new structure of \(cg\)
**end while**

This work proposes two search heuristics for computing the output node preceding an input node. As previously mentioned, quantum circuit optimization follows circuit synthesis. After synthesis the wires in a circuit diagram can be considered either being ordered or unordered. The first situation is the result of most synthesis methods, as explained in the subsequent example and section. The second situation exists when circuits are further optimized for specific quantum computer architectures (e.g. using nearest neighbor interactions [15]).

**Example 3** Consider the recycling presented in Fig. 4

The wires in Fig. 4a are ordered if their labels are considered integers determining their position from the top to the bottom. The wires are unordered if their labels are considered simple strings, implying that the way the circuit was drawn is one of the many possibilities of how its wires can be arranged vertically.

3. **M1: Recycling Ordered Wires**

The majority of the synthesis methods introduce ancilla qubits. For a gate sequence \(GS\), with gates \(g_1\) and \(g_2 \in GS\), \(g_1 \rightarrow g_2\) if gate \(g_1\) will be executed before \(g_2\). Gates are processed during synthesis according to their ordering from \(GS\) (\(g_1\) before \(g_2\)), and ancillae are introduced, if necessary, in the same order (the ancilla needed for \(g_1\) is inserted before the ancilla required by the synthesized \(g_2\)).

The position where ancillae are introduced into the circuit, e.g. top down numbering of wires in circuit diagram, can be used as an indicator of which wires to recycle. For the same gates, where \(g_1 \rightarrow g_2\), having gate \(g_1\) operate on the wire numbered \(w\) and \(g_2\) on the one numbered \(w + 1\), let us assume that the synthesis of \(g_1\) needs to introduce an ancilla. After its introduction, the ancilla will be numbered \(w + 1\), and \(g_2\) will operate on the wire numbered \(w + 2\). Effectively, the number of wires is increased by one, the ancilla’s position is right next to the initial wire of \(g_1\), and all the wires of the gates succeeding \(g_1\), e.g. \(g_2\), are shifted by one position. Therefore, the vertical position of such ancillae relative to the neighboring wires can be used as an indicator of the starting time point of the corresponding qubit’s active stage.

This implies that, there exists an ordering between the wires of a synthesized circuit: ancillae are positioned next to the wires representing the specified gates. This observation can be translated to the causal graphs abstracting circuit diagrams: wire ordering is an indicator of the closest output node in time which precedes a currently investigated input node. The first search heuristic is to simply search for the minimum of \(o.wire - a.wire\), for the output ancilla \(o \in OA\) and the input ancilla \(a \in IA\) where \(o \rightarrow a\).

4. **M2: Recycling Unordered Wires**

The previous ordering of wires is not always guaranteed, because a synthesized circuit could have been optimized after synthesis in ways which affected the ordering of wires. As a consequence, wires should not always be assumed ordered.

An unknown wire ordering increases the complexity of the preceding output node search. The heuristic proposed in this section allows edges to be traversed backwards (Alg. 2). Although, causal graphs are directed, some of the edges will need to be traversed backwards due to the structure of the transformation rule (Fig. 3, 4): before recycling there is no direct path connecting the affected input and output nodes. Thus, in order to connect two arbitrary nodes which satisfy the transformation rule, a graph search has to be performed, where at least one edge has to be traversed backwards.

An aspect not mentioned previously is that, without loss of correctness, the edges in the transformation rule from Fig. 4 represent not only a single graph edge but...
chains of directed edges. Therefore, the output node search is allowed to traverse multiple edges in their specified (forward) direction or backwards. The number of edges traversed backwards ($nr$) is an indication of how much earlier on the circuit’s time axis the currently investigated node exists relative to the input node. The selection criteria chosen in Alg. 2 is to consider the ancilla output node assumed to be closest in time to the input node: forward traversals are preferred to backward traversals. Overall, the shortest path with the lowest $nr$ between an input and and output node is chosen as a solution.

**Algorithm 2.** Search Preceding Output in a Quantum Circuit with Unordered Wires

**Require:** Causal graph $cg$; Input node $input$; Current node $current$; Number of edges traversed backwards $nr$

Return $current$ if $current \in OA$ and $nr \not= 0$

for all node $\in cg$, $current \rightarrow node$
do 
  return Alg. 2 with parameters $cg$, $input$, $node$, $nr$
end for

for all node $\in cg$, $node \rightarrow current$
do 
  return Alg. 2 with parameters $cg$, $input$, $node$, $nr + 1$
end for

**V. RESULTS**

Wire recycling was prototypically implemented and applied to quantum as well as reversible circuits defined over arbitrary gate sets. This is possible because the graph nodes represent operations which are independent of the implemented computation. The applicability of the proposed method is investigated using reversible circuits and quantum circuits consisting entirely of qubit initializations, CNOTs and qubit measurements (ICM circuits) [16]. The source code is available at [http://github.com/alexandrupaler/wirerecycle](http://github.com/alexandrupaler/wirerecycle).

**A. Reversible Circuits**

The entire set of RevLib [17] circuits was downloaded and wire recycling was applied to each circuit using the methods M1 and M2. The results are reported in Table I. The columns $\%M1$ and $\%M2$ are computed as the ratios $\frac{M1}{Qubits}$ respectively $\frac{M2}{Qubits}$. It can be noticed that the highest optimization rate is about 80% for M1, and that in general M1 performs better than M2. This can be explained by the fact that M1 uses the knowledge about how synthesis methods work: there is a very high probability that ancillae are introduced in an ordered fashion, which greatly benefits M1. The large reduction range (0% ... 80%) illustrates that the best optimizations are...
TABLE I: Reversible circuit optimization results (heuristics M1 and M2) and percentage of recycled wires (%M1 and %M2).

| Circuit | Qubits | Ancilla | M1 | M2 | %M1 | %M2 |
|---------|--------|---------|----|----|-----|-----|
| pdc_207 | 619    | 603     | 00 | 01 | 4  | 5  |
| sqa_115 | 489    | 473     | 01 | 02 | 75 | 76 |
| sys_126 | 299    | 233     | 01 | 02 | 65 | 66 |
| e64-had_295 | 195 | 130     | 01 | 02 | 56 | 57 |
| sys_159 | 206    | 198     | 01 | 02 | 52 | 53 |
| sys_204 | 170    | 161     | 01 | 02 | 52 | 53 |
| sys_247 | 203    | 171     | 01 | 02 | 36 | 37 |
| add_284 | 193    | 164     | 01 | 02 | 33 | 34 |
| mod_228 | 196    | 169     | 01 | 02 | 33 | 34 |
| sys_281 | 112    | 104     | 01 | 02 | 52 | 53 |
| sys_291 | 87     | 82      | 01 | 02 | 51 | 52 |
| add_322 | 97     | 32      | 01 | 02 | 32 | 33 |
| add_183 | 97     | 32      | 01 | 02 | 32 | 33 |
| sys_282 | 73     | 66      | 01 | 02 | 41 | 42 |
| cyclo_190 | 39   | 27      | 01 | 02 | 51 | 52 |
| mod_301 | 46     | 40      | 01 | 02 | 43 | 44 |
| rda_314 | 34     | 26      | 01 | 02 | 59 | 60 |
| mod_298 | 45     | 30      | 01 | 02 | 42 | 43 |
| add_174 | 49     | 16      | 01 | 02 | 31 | 32 |
| add_2475 | 49   | 16      | 01 | 02 | 31 | 32 |
| sym_217 | 27     | 18      | 01 | 02 | 56 | 57 |
| mod_adder_206 | 32 | 26   | 01 | 02 | 41 | 42 |
| rda_212 | 25     | 18      | 01 | 02 | 52 | 53 |
| phu_12_mod_192_308 | 25 | 12 | 01 | 02 | 50 | 51 |
| phu_6_mod_192_110 | 25 | 12 | 01 | 02 | 50 | 51 |
| mod_200 | 28     | 23      | 01 | 02 | 32 | 33 |
| mod_406_209 | 23 | 11 | 01 | 02 | 39 | 40 |
| cm_163_a_213 | 29 | 13 | 01 | 02 | 31 | 32 |
| add_172 | 25     | 8       | 01 | 02 | 28 | 29 |
| ham_299 | 21     | 14      | 01 | 02 | 33 | 34 |
| cu_219 | 25     | 11      | 01 | 02 | 24 | 25 |
| rda_142 | 15     | 7       | 01 | 02 | 40 | 41 |
| rda_143 | 15     | 7       | 01 | 02 | 40 | 41 |
| abs_198 | 20     | 8       | 01 | 02 | 25 | 26 |
| sk_27_225 | 18     | 9       | 01 | 02 | 28 | 29 |
| sym_216 | 14     | 8       | 01 | 02 | 36 | 37 |
| rda_111 | 13     | 8       | 01 | 02 | 28 | 29 |
| sk_7_224 | 21     | 11      | 01 | 02 | 14 | 15 |
| mini_div_206 | 10 | 6    | 01 | 02 | 30 | 31 |
| pcell_248 | 21 | 5      | 01 | 02 | 14 | 15 |
| eq_267 | 17     | 7       | 01 | 02 | 18 | 19 |
| sys_6_v_111 | 10 | 4    | 01 | 02 | 30 | 31 |

TABLE II: Quantum adder circuit optimization results and percentage of recycled wires (%M1 and %M2).

| Circuit | Qubits | Ancilla | M1 | M2 | %M1 | %M2 |
|---------|--------|---------|----|----|-----|-----|
| Cuccaro_4 | 304    | 295     | 25 | 26 | 51 | 51 |
| Cuccaro_5 | 390    | 379     | 35 | 36 | 51 | 52 |
| Cuccaro_6 | 476    | 463     | 38 | 39 | 52 | 53 |
| Cuccaro_7 | 562    | 547     | 50 | 51 | 52 | 53 |
| Cuccaro_8 | 648    | 631     | 51 | 52 | 53 | 54 |
| Cuccaro_9 | 734    | 715     | 52 | 53 | 54 | 55 |
| Cuccaro_10 | 820   | 799     | 66 | 67 | 58 | 59 |
| Cuccaro_11 | 906    | 883     | 72 | 73 | 54 | 55 |
| Cuccaro_12 | 992    | 967     | 78 | 79 | 56 | 57 |
| Cuccaro_13 | 1078   | 1051    | 84 | 85 | 58 | 59 |
| Cuccaro_14 | 1164   | 1135    | 90 | 91 | 58 | 59 |
| Cuccaro_15 | 1250   | 1219    | 106 | 107 | 59 | 60 |
| Cuccaro_16 | 1336   | 1303    | 108 | 109 | 60 | 61 |
| Cuccaro_17 | 1422   | 1387    | 116 | 117 | 62 | 63 |
| Cuccaro_18 | 1508   | 1471    | 120 | 121 | 63 | 64 |
| Cuccaro_19 | 1594   | 1555    | 127 | 128 | 65 | 66 |
| Cuccaro_20 | 1680   | 1639    | 157 | 158 | 67 | 68 |

achieved for circuits having qubits with short lifetimes and interacted by few gates.

B. ICM Circuits

Wire recycling was evaluated on fault-tolerant implementations of the quantum adder circuits presented in [13]. The fault-tolerant form was obtained after transforming the circuits using the method from [16]. Fault-tolerant quantum circuits include only qubit (I)nitializations, (C)NOT gates and qubit (M)easurements. ICM circuits use only CNOT gates, because the necessary single qubit gates are implemented by teleportation mechanisms [1, 16] with ancilla qubits initialized in $|0\rangle$, $|+\rangle$, $|Y\rangle$ or $|A\rangle$. Qubits can be measured in the $X,Z$ basis [16].

The results reported in Table II show that in general M1 performs better than M2. At the same time, more than 90% wire reduction obtained for all the circuits shows that fault-tolerant circuit synthesis introduces a vast amount of ancillae with very short active stages.
VI. CONCLUSION

This work introduced quantum circuit wire recycling as a method for quantum circuit optimization. To this end causal graphs were introduced as an equivalent description of a quantum circuit and a recycling method was formulated using two heuristics applied to causal graphs. The method was implemented and its performance was evaluated on circuits from the RevLib circuit library and fault-tolerant implementations of quantum adder circuits. Optimization rates of more than 90% showcase the potential of wire recycling to reduce the quantum hardware requirements. Future work will analyze the complexity of the method, the temporal overhead introduced by recycling, and ways to optimize it using classic data flow graph algorithms.

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