Microwave Engineering for Semiconductor Quantum Dots in a cQED Architecture

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We develop an engineered microwave environment for coupling high $Q$ superconducting resonators to quantum dots using a multilayer fabrication stack for the dot control wiring. Analytic and numerical models are presented to understand how parasitic capacitive coupling to the dot bias leads can result in microwave energy leakage and low resonator quality factors. We show that by controlling the characteristic impedance of the dot bias wiring, on-chip quality factors of 8140 can be attained without the addition of explicit filtering. Using this approach we demonstrate single electron occupation in double and triple dots detected via dipole or quadrupole coupling to a superconducting resonator. Additionally, by using multilayer fabrication we are able to improve ground plane integrity and keep microwave crosstalk below -20 dB out to 18 GHz while maintaining high wire density which will be necessary for future circuit quantum electrodynamics (cQED) quantum dot processors.

Gate defined quantum dots are a nascent platform for quantum computing in which electron charge and spin states are used to define the quantum bit. In silicon and Si/SiGe heterostructures, recent work has shown it is possible to fabricate single, two, and four qubit systems with control fidelities at or approaching the $10^{-2}$ level requisite for error correction. For most quantum dot circuits, the control wiring scheme consists of an electron beam (e-beam) defined gate electrode structure with a rapid fan out into pads that are connected by aluminum or gold wire bonds to a printed circuit board (PCB) with typical die sizes of only a few millimeters. While this keeps the fabrication complexity to a minimum, it results in a minimally controlled microwave environment for the device and any readout circuitry. Near term quantum computing efforts with quantum dots face significant quantum systems engineering challenges balancing the needs for high fidelity readout, coupling, and control.

In this letter, we demonstrate a wiring scheme for quantum dot devices in a cQED architecture. This approach allows for high-density, low crosstalk wiring with controlled RF leakage characteristics, paving the way for larger quantum dot processors utilizing cQED techniques. A simple and intuitive circuit model for cavity leakage from external leads reveals that minimization of the impedance of the environment at the cavity frequency ameliorates photon leakage out the gate leads, which otherwise present an undesired load on the cavity. We implement this method with a microstrip wiring scheme that achieves a low characteristic lead impedance of $Z_{g} \approx 10 \Omega$, and demonstrate resonators with quality factors as high as 8140 (design $Q_L = 10^3$) while connected to the quantum dot gate stack.

For these experiments, we fabricate cavity-coupled pairs of quantum dot structures on an undoped Si/SiGe heterostructure using an overlapping aluminum gate stack. The two dimensional electron gas (2DEG) is formed in a 9 nm thick strained silicon layer either 20 or 30 nm below the surface. To avoid accumulation of 2DEG under the resonator, we remove the heterostructure everywhere except for two

![Image](image-url)

FIG. 1. (a) Dark field optical micrograph of a device using microstrips for the quantum dot leads (lower half of die). (b) A simplified circuit model for the device. The cavity (purple) is a half-wave superconducting microwave resonator with a quarter-wave impedance transformer with shunt capacitance (orange) connected to its voltage node. Transmission lines with characteristic impedance $Z_g$ (teal) are used to supply bias voltages to tune the dots. (c) Scanning electron microscope image of a typical triple dot device. The center dot plunger pin is galvanically tied to the resonator allowing for microwave detection of both double and triple quantum dots. Inset: a schematic cross section along the active region of the device. (d) Cavity phase detection of a double quantum dot stability diagram in the single-electron regime under P2 and P3. A linear background was subtracted from the raw data for clarity. Inset: Cavity detection of a triple dot stability diagram in the single-electron regime.
is shown in Fig. 1(a). To understand the control environment of the 
device, Fig. 1(b) provides a simplified circuit diagram illustrating 
the key components on-chip microwave engineering. Additional 
wires and parasitic cross capacitances are not drawn for simplicity. 
We confine the 2DEG into quantum dots using three layers of overlapping 
metal gates patterned with e-beam lithography (Fig. 1(c)) and deposited by 
e-beam evaporation. High yield electrical isolation between 
gate layers is achieved by cleaning and oxidizing the aluminum 
after lift-off of each layer with a 250 W downstream oxygen plasma ash 
for 10 minutes.

Measurements of these samples are performed by wire bonding each device in a hybrid PCB-metal box enclosure designed to raise unwanted chip-mode frequencies to >20 GHz by creating a milled pocket below most of the 6.15 x 6.15 mm die. The packaged sample is cooled in a dilution refrigerator with base a temperature of $T_{\text{base}} = 25$ mK and typical electron temperatures between 80-100 mK determined by fitting to a thermally broadened conductance peak. Charge detection is achieved by measuring the charge-carrier interaction during electron tunneling events. These interactions are formed by connecting a gate (in our case P2 in Fig. 1(c)) to an aluminum or niobium microwave $\lambda/2$ resonator. Zero point fluctuations in the electric potential of the LC oscillator couple to the dipolar (quadrupolar) detuning degree of freedom ($\epsilon$) for the charge in the double (triple) dot system, allowing for detection of the quantum capacitance $C_Q \approx \frac{d^2 E_{\text{dc}}}{d\epsilon^2}$. By probing the cavity with a microwave tone at the bare cavity frequency ($f_c$) and recording the transmitted amplitude and phase as a function of plunger gate voltage, damping and phase shifts of the probe are observed during electron tunneling events. These interactions are formed by connecting a gate (in our case P2 in Fig. 1(c)) to an aluminum or niobium microwave $\lambda/2$ resonator. Zero point fluctuations in the electric potential of the LC oscillator couple to the dipolar (quadrupolar) detuning degree of freedom ($\epsilon$) for the charge in the double (triple) dot system, allowing for detection of the quantum capacitance $C_Q \approx \frac{d^2 E_{\text{dc}}}{d\epsilon^2}$. By probing the cavity with a microwave tone at the bare cavity frequency ($f_c$) and recording the transmitted amplitude and phase as a function of plunger gate voltage, damping and phase shifts of the probe are observed during electron tunneling events.

In order to maintain a high cavity quality factor we engineer the microwave environment to minimize photon leakage out the 25 bias leads of the two triple dot gate structures. This engineering amounts to maximizing the reflection coefficient of the microwave energy out any lead other than the readout port by making the other leads look high or low impedance to ground. A unique requirement for cQED experiments with dots is DC voltage biasing of the center pin of the coplanar waveguide (CPW) resonator in order to accumulate a quantum dot under P2. Test devices with DC taps at the center of the waveguide had quality factors less than 10$^3$, which was much lower than the explicit coupling defined by $C_{\text{in}}$ and $C_{\text{out}}$. We eliminate leakage out this lead by turning the tap into a $\lambda/4$-length CPW. The end of the $\lambda/4$ CPW is shunted with a load impedance $Z_L$ in the form of a large parallel plate capacitor using an SiO$_2$ dielectric. The input impedance for a $\lambda/4$ segment of transmission line terminated by a load $Z_L$ is given by

$$ Z_{\text{in}} = Z_0 + \frac{Z_0 \tan(\beta \ell)}{Z_0 + i Z_0 \tan(\beta \ell)} = \frac{Z_0^2}{Z_L}, $$

where $\beta = 2\pi/\lambda$ is the propagation constant of the transmission line, and $\ell$ is its physical length. By making the shunt capacitance large ($C_{\text{shunt}} \approx 100$ pF), we achieve $Z_{\text{in}} \approx 10$ kΩ. In combination with tapping at the voltage node, this effective impedance leads to minimal leakage out the DC bias tap at the resonance frequency. Using this DC bias, devices without the overlapping aluminum gates achieved loaded quality factors as high as 4x10$^4$, well beyond the limit imposed by parasitic loading from the quantum dot circuit. We note that the quadratic dependence of $Z_{\text{in}}$ on $Z_0$ provides a way to further increase the quarter-wave tap input impedance through use of large $Z_0$ CPW.

The use of the overlapping gate stack poses a unique challenge for RF readout schemes, because of the large parasitic capacitances $C_p$ (order 1 fF) between the gate electrodes in the region where the dots are formed. These parasitic capacitances are the same order of magnitude as the capacitance used to purposefully couple photons into the readout port ($C_{\text{out}} \approx 5.5$ fF for a quality factor of 10$^4$ at 7.25 GHz) and therefore result in substantial microwave leakage out the leads. To analyze this leakage we first use a lumped element circuit model for loading of an LCR oscillator to a transmission line environment with characteristic impedance $Z_0$ and parasitic capacitance $C_p$.

In the Norton equivalent circuit the gate impedance transforms to an additional parallel resistance

$$ Z_g' = Z_g \left( 1 + \frac{1}{\omega^2 C_p Z_g^2} \right). $$(2)

By computing the new total load resistance $R_{\text{tot}} = R_{\text{r}} || Z_g'$, we find the effective quality factor $Q_{\text{eff}} = \frac{\omega L C R_{\text{r}}}{C_p}$. In terms of the impedance of the parasitic capacitor $Z_p$, gate impedance $Z_g$, and effective internal resistance $R_e$ we find:

$$ \frac{Q_{\text{eff}}}{Q_i} = \frac{Z_p^2 + Z_g^2}{Z_p^2 + Z_g^2 \left( 1 + \frac{R_e}{Z_g} \right)}, $$

revealing there are in principle two ways for reducing the effect of unwanted loading: minimize the parasitic capacitance
(maximizing $Z_\mathrm{g}$) or alter the gate impedance $Z_\mathrm{g}$ to minimize the effect of the $R_\ell/Z_\mathrm{g}$ term in the denominator of Eq. (3). Notably, it is easier to reach the limit of $Z_\mathrm{g} \ll R_\ell$ than $Z_\mathrm{g} \gg R_\ell$, as $R_\ell \gtrsim 10 \, \text{M}\Omega$ for typical superconducting resonators. Figure 2(b) shows a contour plot of Eq. (3) in the low $Z_\mathrm{g}$ regime. For our experiments, the characteristic cavity impedance is $Z_\mathrm{g} = 50 \, \Omega$, but the core result holds for higher impedance cavities as well and is captured by the definition of $R_\ell$.

![Diagram](image)

**FIG. 2.** (a) Lumped element model for an LCR oscillator coupled to a parasitic lead and its Norton equivalent circuit. (b) A contour plot of $Q_{\text{eff}}/Q$, as a function of gate impedance and parasitic capacitance assuming $Q_t = 10^5$. (c) A schematic of a microstrip line consisting of a substrate ($\epsilon_r$), ground plane, pad dielectric ($\epsilon_r'$) of thickness $h$, and strip of width $W$. Adjacent is an optical image of a mesa structure with microstrip leads on a 7 $\mu$m pitch (scale = 50 $\mu$m). Below: the microwave crosstalk between numberer microstrips connected to the set of gates used for biasing (P1:B2:S2:B3:P3) indicating -20 dB crosstalk between leads at frequencies above 5 GHz for a 7 $\mu$m pitch. Below 3 GHz, crosstalk is dominated by proximity of bond pads rather than proximity of the microstrips. Ripple features in the crosstalk are due to the finite lengths of the microstrips and their mismatch to the 50 $\Omega$ coaxial cables. (d) Example resonator transmission spectra from two devices with $Q_t \approx 4888$ and $Q_t \approx 8140$.

Since reducing the parasitic capacitance in the overlapping gate stack is intrinsically difficult, we opt to control the gate impedance $Z_\mathrm{g}$. Previous efforts to improve cavity quality factors involve the use of RF choke inductors or LC low pass filters, which have either high or low impedance at the cavity frequency, suppressing leakage. In both cases, the leads acquire a frequency dependent filter function which substantially limits the control bandwidth. To eliminate this potentially undesired feature, we choose to reduce the characteristic impedance of the transmission line on-chip using a microstrip geometry. The design and implementation of microstrip wiring is illustrated in Fig. 2(c). The wires are fabricated in a multilayer fabrication process that has three essential steps: deposition of the base layer ground plane, growth of an insulating dielectric layer, and deposition of the microstrip counter electrode.

To obtain the desired low impedance, we fabricate microstrips with a width $W = 3 \, \mu$m and an SiO$_2$ thickness $h = 0.2 \, \mu$m yielding the limit where the parameter $\alpha = W/h \gg 1$. The impedance of the microstrip in this limit can be calculated using conformal mapping and is given by

$$Z_\mathrm{g} \approx \frac{1}{\alpha + 1.393 + 0.667 \log(\alpha + 1.444) \sqrt{\frac{\mu_0}{\epsilon_0 \epsilon_r}}}$$

with an effective permittivity:

$$\epsilon_r \approx \epsilon_{r2} + \frac{1}{2} + \frac{\epsilon_{r2} - 1}{2 \sqrt{1 + 12/\alpha}}.$$  

For our parameters, we find $Z_\mathrm{g} \approx 10 \, \Omega$ which compares favorably to LC low pass filters in the literature that have an input impedance of $Z_{in} \approx 20 \, \Omega$, while retaining the flexibility of a flat frequency response. The low impedance leads come at the cost of an insertion loss of approximately 3.5 $\text{dB}$ due to mismatch between the $Z_0 = 50 \, \Omega$ coaxial cabling and the $Z_\mathrm{g} = 10 \, \Omega$ microstrip. This effect could be mitigated by an impedance matching element such as a Klopfenstein taper. The multilayer stack also provides a means for improved and reliable microwave performance in increasingly complex processors through additional on-chip crossovers. These structures serve as low inductance connections between ground planes on-chip, thereby suppressing spurious slot line modes more efficiently than with traditional aluminum wire bond stitching. Furthermore, aluminum wire bond stitching suffers from the low critical field of aluminum ($H_c \approx 10 \, \text{mT}$), which can damage the cavity upon application of an external magnetic field. Since both the crossover and base ground plane metal can be made of field tolerant superconductors such as niobium, they are useful for preserving circuit performance in cavity-spin coupling experiments. Lastly, in Fig. 2(c) we demonstrate that this microstrip wiring scheme maintains less than -20 $\text{dB}$ crosstalk between adjacent leads over a broad frequency range with a 7 $\mu$m wire pitch for approximately 1 mm, which could be important for minimizing off-resonant driving observed in recent resonant two-qubit gate experiments.

Using these design principles, we fabricated and measured over twenty cavity coupled quantum dot structures and found a total spread in resonance quality factors between 2600-8140 (example spectra shown in Fig. 4(d)). We attribute the spread in quality factor to variation in parasitic capacitance and finite length effects for the low impedance microstrips (discussed below). We note that in addition to the spread in quality factors for identical resonator designs (with lithographic variation of order 0.2 $\mu$m), the fundamental resonance frequencies show a large spread of approximately $\pm 100 \, \text{MHz}$. Using the measured frequency, length of the waveguide, and conformal mapping, we estimate the capacitance of the CPW structure, we back out a mean substrate permittivity to be $\epsilon_r \approx 14.2$. Using linear interpolation, we estimate the permittivity of the SiGe alloy to be $\epsilon_r(x) \approx \epsilon_r^0 (1-x) + \epsilon_r^\text{Ge} x \approx 13$ where $x = 0.3$. The origin of the apparent deviation is unknown at this time. Variation in the observed resonance frequencies could be explained by variation in the relative dielectric constant of the SiGe alloy by $\pm 0.3$, possibly caused by fabrication processing or growth variation across the wafer.
FIG. 3. (a) Circuit schematic for the SPICE simulations of loading from an impedance-mismatched lead (red) of variable length to a 50 Ω frequency environment. The resonator (blue) with explicit external loading from the drive and readout circuity (green) has a design $Q = 10^5$ and frequency $f_0 = 7.25$ GHz. (b) A contour plot of $Q_{eff}/Q_L$ for a 1 mm long leakage path as a function of its characteristic impedance and parasitic capacitance. (c) Color plot of $Q_{eff}/Q_L$ as a function of the leakage path length and impedance ($Z_g$). Inset: the reflection coefficient of a 50 Ω terminated transmission line computed using Eq. (1). (d) Line cuts from (c) for different $Z_g$ showing the impact on the $Q_{eff}/Q_L$ as a function of the lead length. Inset: the nominal voltage profiles for the quarter-wave (green) and half wave (red) lengths of transmission line. (e) Color plot of the $Q_{eff}/Q_L$ as a function of leakage path length and parasitic capacitance. (f) Line cuts from (e) for different $C_p$ as a function of lead length. In both (d) and (f) flattening in $Q_{eff}/Q_L$ is the result of the leakage becoming less than the design $Q_L = 10^5$.

Although Eq. 3 is corrected for coupling to an infinitely long transmission line with impedance $Z_g$, in practice the low impedance leads on-chip are only a few millimeters long and are wire bonded to a 50 Ω environment. To elucidate the impact of the finite length of on-chip low impedance leads, we use "Simulation Program with Integrated Circuit Emphasis" (SPICE) to calculate the resonator line width under various conditions. Figure 3(a) shows the circuit schematic used to understand the consequences of using finite transmission lines of length $L$. Similar to the lumped element case, lowering $Z_g$ and $C_p$ results in suppression of leakage. For a $L = 1$ mm microstrip, the contour plot of the leakage path impedance in Fig. 3(b) is qualitatively similar to that in Fig. 2(b), but the roll-off is stronger as a function of $Z_g$.

In Fig. 3(c,d) we compute $Q_{eff}/Q_L$ as a function of $Z_g$ and leakage path (gate) length. When the gate length is a quarter wavelength of the resonance frequency, no voltage drop occurs across the 50 Ω environment at the end of the lead, effectively eliminating loss out the lead. Conversely, when the lead is exactly $\lambda/2$ in length, the voltage drop across the 50 Ω environment is maximal, resulting in loss to the environment equivalent to using no leakage suppression scheme at all. As shown in Fig. 3(c,d), if $Z_g$ is low, the range of gate lead lengths that suppress leakage becomes very wide, with only lengths very close to $\lambda/2$ displaying any significant degradation in $Q_{eff}$. Figure 3(e,f) shows that analogous results hold for $Q_{eff}$ as a function of $C_p$. The inset to Fig. 3(c) shows the reflection coefficient of a 50 Ω terminated transmission line calculated using Eq. (1). The result is very similar to the SPICE calculation in the main panel, and thus the simple analytic form provides good intuition for the finite length effects in maintaining a high $Q$.

In conclusion, we demonstrated a high-density, low-crosstalk, low impedance wiring scheme for quantum dots in a cQED framework. Using a simple circuit model we designed a filterless low impedance wiring strategy for minimal microwave leakage achieving quality factors as high as 8140. We showed how this approach remains robust even in the presence of finite length effects of the low impedance leads. For devices with functional quantum dots, measurement of the charge configuration down to zero electrons in both double and triple dots is achieved, paving the way towards study of spin-photon coupling of exchange-based qubits in Si/SiGe.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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