Analyzing and Measuring the Performance of Memristive Integrating Amplifiers
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Abstract—Recording reliably extracellular neural activities is an essential prerequisite for the development of bioelectronics and neuroprosthetic applications. Recently, a fully differential, 2-stage, integrating pre-amplifier was proposed for amplifying and then digitising neural signals. The amplifier featured a finely tuneable offset that was used as a variable threshold detector. Given that the amplifier is integrating, the DC operating point keeps changing during integration, rendering traditional analysis (AC/DC) unsuitable. In this work, we analyse the operation of this circuit and propose alternative definitions for validating the key performance metrics, including: gain, bandwidth, offset tuning range and offset sensitivity with respect to the memory states of the employed memristors. The amplification process is analysed largely through investigating the transient behaviour during the integration phase. This benchmarking approach is finally leveraged for providing useful insights and design trade-offs of the memristor-based integrating amplifier.

Index Terms—neural spike detection, threshold detection, hybrid CMOS/memristor circuit, integrating amplifier, high sensitivity

I. INTRODUCTION
RECORDING neural signals using implantable microsystems is essential to the development of diagnostic and therapeutic solutions [1]. Brain Machine Interfaces (BMIs) [2] and neuroscience research [3]. The implantable device typically contains electrodes as well as front-end and back-end module, where raw neural signals collected from electrodes will be fed into the other two modules for further processing [4]. After processing, analogue neuronal trains [5] or digital format [6] will be transmitted to external devices wirelessly. With digital output, a neural spike (Action Potential, AP) detection algorithm which comprises threshold detection and digitisation can be applied in back-end stage typically [7]. For an implantable device, this is required to have low power/heat dissipation (< 80 mW/cm²) in order to avoid damaging surrounding tissue [8]. The low power dissipation contributes to high integration density. Furthermore, both dc offset [9] and minute extracellular neural activity signals (in the order of 10s-100s of µV) picked up by electrodes will be fed into front-end devices for amplification and filtering [10]. In summary, the implantable front-end module needs to have low-power dissipation, low-noise and also to reject dc offset and other noise interference.

To achieve low power consumption, a number of multi-channel neural recording architectures has been proposed [11]. It is clear that the energy consumed in the analogue multiplexer before ADC can be reduced to improve power efficiency. From the system level point of view, Serb et al. [14] propose to perform spike detection and digitisation directly on the neural signal from electrodes in order to save power from processing local field potentials (LFP) which will be discarded. Preamplifiers are critical for boosting the extremely weak input signals to levels where they can be further processed and so they act as the first stage in any neural recording processing (a result of the Friis formula) [15]. Alternatively, the operational transconductance amplifier-capacitor (OTA-C) structure is suitable for bio-electronic devices as the low-pass filter for neural signals [16]. The objective of combining an OTA with load capacitor is to integrate signals instead of simply amplifying them in continuous mode in order to boost effective gain. A different technique has been proposed to compensate the DC offset of the electrode-tissue interface [17] [18] [19]. The Harrison topology is capable of rejecting large dc offset, operates in continuous mode and is the current standard in the field [20]. It is possible to conduct threshold detection directly on the signals in Harrison amplifier. [14].

With the characteristic of analogue modulation of their resistive state, memristive devices can be utilised in CMOS circuit as trimming component [21]. Such an integrating pre-amplifier enhanced with offset tuning for ultra-fine threshold detection was proposed [14]. In this work, memristive devices were utilised as non-volatile resistive loads [22] to trim the offset voltage with high precision.

The architecture and preliminary analysis presented in [14] demonstrated the general operating principle of what we may describe as a "memristive integrating amplifier". In this work we add detail on the operation of this type of amplifier as well as investigate how important parameters such as clocking and differential/common input voltage affect performance. One of the challenges identified in doing this is defining important performance (e.g. gain, bandwidth, CMRR and etc.) in a manner suitable to the operation of integrating amplifiers. We provide such metrics that suit the particular implementation of the memristive integrating pre-amplifier. The mathematical descriptions of the resulting metrics and insight obtained from examining the behaviour of transistors during the key integration phase of the amplifier illuminate various trade-offs that characterise the design. This work has been done using commercially available 0.18µm CMOS technology with 1.8V supply voltage across all the experiments.

The paper is organised as follows: A brief overview of the pre-amplifier and its operation, followed by the re-definition of its key performance metrics is presented in section [11].
Simulation set-up, analysis and results are shown in section III. A discussion of design trade-offs and other points of interest pertaining to the amplifier design is in section IV. Finally, section V summarises and concludes the paper.

II. FUNDAMENTAL OPERATION AND ANALYSIS

A. Amplifier design overview

The architecture studied is a modified/simplified version of the original design proposed in [14]; it is shown in Fig. 1. It consists of three main sections: I) a fully differential core amplifier (effectively a single-stage analogue amplifier acting as the 1st stage of the design), II) a dynamic latched comparator (DLC) amplifying and quantising the output state of the core amp and III) a current bias unit powering the system’s core. The overall system operates as a threshold detection circuit which compares two minute input signals and ultimately outputs a binary flag, as shown in Fig. 2.

Each threshold detection operation is carried out in four phases that we label as: (i) reset, (ii) integrating, (iii) digitisation and (iv) off. These are illustrated in Fig. 3. They remain unchanged from the original work and act as follows:

In the reset phase (i) the core amplifier is on (clk_ana, clk_rst: high, clk, clk_anabar: low) and the load capacitors are discharged ($V_{mida/b} = 0$), so that voltage/current in core amplifier is initialised and cleared before integration commences in the next phase.

In the integrating phase (ii) (clk_ana: high, clk_anabar, clk_rst, clk: low) the reset transistors (M8&M9) are switched off and the currents flowing through the branches of the core amplifier drain into the load capacitors. From a ‘large signal’ perspective, $V_{mida}$ and $V_{midb}$ continuously increase during integration. In terms of ‘small signal’, $\Delta V_{mida-midb}$ increases with time and normal operation is maintained so long as the cascode transistors M6&M7 remain in the saturation region. The voltage difference between nodes $mida$ and $midb$ is impacted by the charging speed/current and integration time. Memristors R1&R2 work as trimming devices and tune the offset of the core with very high sensitivity ($1\mu V/k\Omega$ shown in the original paper). At the end of this phase, $V_{mida/b}$ should be high enough to successfully trigger the DLC and $\Delta V_{mida-midb}$ should be as large as possible for maximising gain.

In the digitisation phase (iii) (clk_ana, clk: high, clk_anabar, clk_rst: low) clk goes high, triggering the DLC to perform the conversion of $V_{mida/b}$ into the final digital outputs. By convention we take the output from the branch where output ‘1’ represents a spike while ‘0’ represents the absence of a spike. Shortly after the decision is committed by the DLC, the core amplifier is turned off as the system re-enters the off phase.

Finally, in the off phase (iv) (clk: high, clk_ana, clk_anabar, clk_rst: low), the tail current is cut off by setting clk_ana to zero. The pre-amplifier is turned off and stops recording neural signals. clk_anabar is also deactivated (goes to high) thus preventing the accumulated charge across the large gate capacitances of M4&M6 from draining away.

B. Differences vs. the original design

The design under study has been simplified vis-a-vis the original from [14] as follows: First a fixed clocking scheme was adopted. The previous design featured an asynchronous clock generation circuit embedded in each channel. When it determined that the result would be available on nodes $mida/midb$ it triggered, on-demand, the clocks. However, it has been observed that the integration results for the very small differential input signals of interest always become available at fixed intervals; therefore, an on-demand triggering system is not required here. Second, the sizes of the input transistor pair were decreased. In [14], huge transistors were introduced as input pair to reduce noise. However, the associated large parasitic capacitances together with the $\mu A$ tail currents result in a low transit frequency ($f_T$). Therefore, in consideration of speed and power consumption the sizes of input transistors have been decreased.

C. Key performance metrics

The main performance indicators for the core amplifier include: gain, bandwidth, offset tuning range and sensitivity on memristor resistance, noise performance, input range, common-mode rejection ratio (CMRR) and power consumption. All these metrics (with the exception of power) mostly depend on the integrating phase, when amplification is conducted. In this stage the cascode transistors are in saturation...
mode. As $V_{\text{mida/b}}$ keep increasing throughout the integration phase, there is no set DC operating point. nonetheless, because this is an extremely small signal amplifier, the current flowing through each branch is under normal circumstances approximately the same and constant. This allows for analysis similar in spirit to regular small-signal analysis by using transient simulations for obtaining the relevant data. Standard DC operating point and AC analysis cannot be applied here directly. It is perhaps more appropriate to think of $V_{\text{mida/b}}$ as ‘large signal’ in the $mV$-range and $\Delta V_{\text{mid}} = V_{\text{mida}} - V_{\text{midb}}$ as ‘small signal’ in the $\mu V$-range.

1) Gain: The gain is defined, as usual, as the ratio of the output signal amplitude over the input signal amplitude, $\delta V_{\text{out}} / \delta V_{\text{in}}$. For the core amplifier this translates into $\delta V_{\text{mid}} / \delta V_{\text{in}}$, where $\delta V_{\text{mid}}$ is taken at the end of the integration phase and $\delta V_{\text{in}}$ is considered constant for the purposes of this analysis.
that depends only on engineering parameters. We begin by observing that:

$$\Delta V_{\text{mid}} = \Delta Q/C$$

(5)

where $\Delta Q$ is the total charge accumulated on each node (mida/b) as a result of the tail current. This can, however, be easily expressed as:

$$\Delta Q \approx i_{\text{tail}/2} \cdot \tau$$

(6)

where $i_{\text{tail}/2}$ is the half-tail current of the amplifier core. This allows us to express $\tau$ as follows:

$$\tau = \Delta V_{\text{mid}} \cdot C / i_{\text{tail}/2}$$

(7)

where we replaced the approximation symbol with an equality for clarity, since the deviation is expected to be sufficiently small under normal operation.

Now we can substitute Eq (7) into Eq (4) and obtain gain as:

$$G = \frac{g_m \cdot \Delta V_{\text{mid}}}{i_{\text{tail}/2}}$$

(8)

which further simplifies to:

$$G = TE \cdot \Delta V_{\text{mid}}$$

(9)

where $TE$ is the transconductor efficiency factor of the input diff pair transistors. In other words the differential gain of the pre-amplifier core only depends on the $TE$ and the voltage range over which we are integrating. Integration time and tail current can be freely traded off, in principle (but consider noise, etc.). Note that $\Delta V_{\text{mid}}$ represents voltage difference during the integration phase, while $\delta V_{\text{mid}}$ is the output that captured at the end of integration.

2) Bandwidth: In an integrating amplifier, such as the one studied here, the notion of bandwidth is somewhat different than in continuous mode systems because the output is not a continuous waveform whose Fourier component at some frequency can be compared in magnitude to an input stimulus. Instead, our amplifier output is a continuous waveform whose Fourier component at some frequency can be compared in magnitude to an input stimulus. Throughout our analysis we make the following approximation: the amplifier is integrating linearly throughout its integration voltage range $\Delta V_{\text{mid}}$. The input differential signals of interest are so small that linear approximations can be assumed to hold throughout the whole system (eqs. (1) and (6)). In practice, there will be some additional distortion due to the changing $V_{ds}$ experienced by the cascode transistors, but we currently ignore this effect in our analysis.

3) Tuning Sensitivity and range: The memristive devices applied in the current branches regulate the charging speed to load capacitors by modulating the effective output resistance of the core amplifier as seen by the capacitive load. To see the mechanics of this action we refer to the schematic in Fig. 1 and the standard equation for the impedance of a drain-degenerated MOSFET, looking into the source. When this is applied to the source of M6 we obtain:

$$Z_{s6} \approx \frac{1}{g_{m6}} \left(1 + \frac{R_1}{R_{o6}}\right)$$

(12)

where $Z_{s6}$ is the impedance looking into the source of M6, $g_{m6}$ is the differential transconductance of M6, and $R_{o6}$ the output resistance of M6.

Extending this principle to calculate the impedance of M4, as drain-degenerated by the M6-R1 cascade we obtain:

$$Z_{s4} \approx \frac{1}{g_{m4}} \left(1 + \frac{Z_{s6}}{R_{o4}}\right)$$

(13)

which eventually unfolds to:

Fig. 4 illustrates the evolution of $\lambda$ with $f$: the frequency of the sinusoid in units of $\pi$. We many now define the effective bandwidth of the amplifier as the frequency above which $\lambda(f)$ is always below a certain value $p$. An indicative measure of bandwidth may be given by $p = 20\%$. For an integration period of $1 \mu s$ this yields around $1.5 MHz$ bandwidth. Naturally, $p$ can be set to another suitably chosen value to yield different appropriate bandwidth figures. This metric holds only so long as the resulting frequency is much lower than all other RCs in the amplifier core, and thus we have no additional attenuation. It is worth noting that the most typical neural signals of interest, action potentials (spikes), last in the order of $\mu s$. This implies that the even spike features of the order of $100s$ of $\mu s$ will be integrated without any significant attenuation.
\[ Z_{s4} = \frac{1}{g_{m4}} + \frac{1}{g_{m6}g_{m4}R_{o4}} + \frac{R_1}{g_{m6}R_6g_{m4}R_{o4}} \]  

A similar expression also applies for the right current branch.

Setting \( A = \frac{1}{g_{m4}} + \frac{1}{g_{m6}g_{m4}R_{o4}} \) and \( B = \frac{1}{g_{m6}R_6g_{m4}R_{o4}} \) we can express the impedances seen by M3 looking into each current branch as:

\[ Z_l \approx A + BR_1 \]
\[ Z_r \approx A + BR_2 \]

where \( Z_l = Z_{s4} \) is the left current branch impedance and \( Z_r \) is the right branch impedance.

Next, examining the distribution of tail current across the branches we obtain an expression for the left branch current \( i_l \) as follows:

\[ i_l \approx i_T \frac{A + BR_2}{2A + B(R_1 + R_2)} \]  

where \( i_T = i_3 \) is the tail current. Given that \( B \ll 1 \) (as it is the product of two maximum FET amplifier gains), \( i_l \) can be further approximated as follows:

\[ i_l \approx i_T \frac{1}{2} \left( 1 - \frac{B}{2A} (R_1 - R_2) \right) \]  

Similarly for the right branch current \( i_r \):

\[ i_r \approx i_T \frac{1}{2} \left( 1 + \frac{B}{2A} (R_1 - R_2) \right) \]

This yields a total current imbalance of:

\[ i_l - i_r \approx \Delta i = -i_T \frac{B}{2A} (R_1 - R_2) \]

which if divided by the common transconductance of the input differential pair transistors yields the required voltage offset to rebalance the branches as a function of the difference in RRAM resistive states:

\[ V_{os} \approx V_{ina} - V_{inb} = \frac{\Delta i}{g_{m4,5}} \]

which when fully unfolded yields:

\[ V_{os} \approx -\frac{(R_1 - R_2)i_T}{2R_{o,cas}g_{m,ina}(1 + g_{m,cas}R_{o,ina})} \]  

where we have renamed our variables to explicitly stress the common values of output impedances and differential transconductances of the input differential pair and cascode transistors. (\( R_{o,cas} \) is output impedance of cascode transistor, \( g_{m,ina} \) = diff. transconductance of the input diff pair).

This result relies on the standard small-signal assumptions that the various \( g_{m,s} \) and \( R_{o,s} \) remain constant, all transistors involved remain saturated (either over or below threshold) and crucially, it makes no other assumptions on the voltage present at the load capacitors. So long as: a) the \( g_{m,s} \) of all transistors remain mostly unchanged and b) the change in load capacitor voltage does not affect the absolute difference in RRAM resistive states seen by the system, the transistors charge uniformly under balanced conditions \( (V_{in} = V_{os}) \). Whilst condition (a) can be reasonably approximated as true in saturation, condition (b) is not generally true because of the non-linearity in the \( I-V \) of the RRAM devices \[ [23] \]. Analysis of this phenomenon is outside the scope of the paper as it is RRAM technology-specific, but in general if the absolute resistive state difference changes as the integration process progresses, we obtain offset voltage drift that may potentially affect operation when a fixed, non-zero offset is specifically required (e.g. for threshold detection with the offset acting as threshold).

Overall, Eq. 22 shows that in small-signal conditions the offset voltage of the core amplifier is proportional to the difference in RRAM resistive states divided by the maximum transistor gains of the input diff pair and cascode transistors. This division explains the extreme fineness of tuning achievable.

The tuning range can in principle be extended under the rule of Eq. 22 for as long as the underlying assumptions hold. We note two important limiting conditions: 1) If the imbalance in currents becomes large, eventually the assumption of equal \( g_{m,s} \) on both current branches collapses. Exactly when this occurs depends on the tightness of the specifications. 2) If the voltage dropped across the larger of the pair \( R_{1,2} \) becomes comparable to the capacitor voltage range through which the amplifier can integrate while maintaining transistor saturation (normal operation), eventually the amplifier will run out of integration voltage headroom. Thus, introducing a headroom vs. maximum tuning range headroom (so long as condition (2) remains the dominant limit).

4) Input-Referred Noise: The amplifier’s core noise is dominated by the input differential pair. The reasons are the same as in continuous mode amplifiers such as the Harrison \[ [20] \]: the input pair provides substantial gain through its \( g_{m,s} \) and thus mitigates the input-referred contributions from downstream elements (primarily the cascode transistors and the RRAM devices).

The standard MOSFET input referred-noise model containing both thermal and flicker noise is given by the following expression for spectral density \[ [24] \]:

\[ \overline{V_{in}^2}(f) = 4kT \gamma \frac{1}{g_{m}} + \frac{K}{C_{ox}WL} \]  

where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature, \( \gamma = \frac{2}{3} \) for long-channel transistors and higher for shorter channel devices, \( K \) a typically empirically determined factor scaling \( 1/f \) noise, \( C_{ox} \) the gate capacitance, \( W,L \) the transistor sizes and \( f \) denotes (linear) frequency.

In our amplifier the noise from each transistor in the input differential pair from Eq. 22 propagates to the output via the gain \( G \) from Eq. 8 and is then moderated by the attenuation factor \( \lambda \) from Eq. 11. Moreover, bearing in mind that the amplifier’s output is the difference \( V_{mid} \) and that it is operating in a ‘nearly balanced’ regime, the total noise spectral density equation at the outputs becomes:

\[ \overline{V_{out,total}^2}(f) = 2 \cdot \overline{V_{in}^2}(f) \cdot G^2 \cdot \lambda^2(f) \]  


where we substitute all $\omega$s with $f$ for simplicity and have assumed that both branches contribute equally to noise.

We note the following: First, the application of $\lambda(f)$ turns white noise into $1/f$ (more accurately $1/af$) and $1/f^2$ noise into $1/f^2$, as is typical of single-pole low-pass filters. Second, if we desire short integration periods, noise modulation effect by $\lambda(f)$ may become too weak to make any practical difference because of the $a \ll 1$ factor.

Finally, input-referring Eq. 23 and the contributions of $\lambda(f)$ (which can be ignored in this case), we obtain the following noise profile:

$$V_{in,\text{total}}^2 = 2 \cdot \lambda^2(f) \left( \frac{8kT_0}{3g_{m}} + \frac{K}{C_{ox}WLf} \right)$$  \hspace{1cm} (25)

where the $g_{m}$, $W$ and $L$ factors are the same (at least approximately) for both transistors in the input diff pair.

5) Input Range: Under normal operation, the input differential pair transistors M4,5 must be in subthreshold saturation. This implies two operating conditions: (1) A minimum drain-source voltage $|V_{ds,\text{min}}| = m \cdot V_T$, where $V_T$ is the thermal voltage and good rule of thumb for ensuring subthreshold saturation is $3 \leq m \leq 4$ (here we will use $m = 4$) \hspace{1cm} (25).

2) We need an appropriate gate-source voltage $|V_{gs,4}| < |V_{th}|$ that allows the transistor to pass $\approx i_{\text{tail}}/2$ in subthreshold saturation. This is treated as approximately constant in this analysis.

Therefore the common mode voltage $V_{CM}$ is bounded: The top boundary is simply:

$$V_{DD} - |V_{ds,\text{sat},3}| - |V_{gs,4}| \geq V_{CM}$$ \hspace{1cm} (26)

where $V_{ds,\text{sat},x}$ is the drain-source saturation voltage of transistor $x$. Exceeding the boundary causes M3 to triode and simultaneously encroaches on $V_{gs,4}$, progressively shutting the amplifier down.

The bottom boundary hinges on maintaining the input differential pair in subthreshold saturation ($|V_{ds,4}| \geq |V_{ds,\text{min},4}|$):

$$|V_{ds,4}| \approx (V_{CM} + |V_{gs,4}|) - (V_{anabar,\text{low}} + |V_{gs,6}|) \geq 4 \cdot V_T$$ \hspace{1cm} (27)

where $V_{gs,6}$ is the gate-source voltage allowing the cascode transistor to pass $\approx i_{\text{tail}}/2$. This is also treated as approximately constant in this analysis. The 2nd term is recognised as $V_{\text{drain}_a}$ under normal operation and node voltage $V_{\text{drain}_a}$ can be seen in the schematic of Fig. [1]. This unfolds to:

$$V_{CM} \geq V_{anabar,\text{low}} + |V_{gs,6}| - |V_{gs,4}| + 4 \cdot V_T$$ \hspace{1cm} (28)

Here, the cascode transistor M6 enforces a specific and relatively fixed value of $V_{\text{drain}_a}$ under the control of $V_{anabar,\text{low}}$ (similarly for M7 and $V_{\text{drain}_a}$). Combining Eqs. 26 and 28 we can find the approximate value of $V_{anabar,\text{low}}$ above which the input differential pair runs out of common mode range:

$$V_{anabar,\text{low}} = V_{DD} - |V_{ds,\text{sat},3}| - 4 \cdot V_T - |V_{gs,6}|$$ \hspace{1cm} (29)

From here we can see the trade-off between common mode and integration voltage ranges (directly connected to gain). If the input stage of the amplifier is AC-coupled, the required $V_{CM}$ range may become very small.

6) CMRR and CMGD: In continuous mode amplifiers CMRR (common more rejection ratio) is defined as the ratio of the differential gain vs. the common mode gain. In our case this is given by:

$$\text{CMRR} = \frac{A_{dm}}{A_{cm}} = \frac{dG}{dA_{cm}}$$ \hspace{1cm} (30)

where $A_{dm}, A_{cm}$ are the differential and common mode gains respectively.

In a perfectly balanced amplifier (nominal design) this will be zero at first order, so it would be perhaps more informative to measure this directly in silico.

There is a slightly different effect which will impact our integrating amp and can be analysed easily: Gain distortion vs. common mode voltage $V_{CM}$:

We define this ‘common mode gain distortion’ as:

$$\text{CMGD} = \frac{dG}{dV_{CM}}$$ \hspace{1cm} (31)

Taking Eq. 30 and substituting $g_m = i_{\text{tail}}/2$ we obtain:

$$G = \frac{\Delta V_{\text{mid}}}{V_{gs,4}}$$ \hspace{1cm} (32)

We can now unfold the derivative $\frac{dG}{dV_{CM}}$ as follows:

$$\frac{dG}{dV_{CM}} = \frac{\Delta V_{\text{mid}}}{V_{gs,4}} \cdot \frac{dV_{gs}}{dV_g} = -\frac{\Delta V_{\text{mid}}}{V_{gs,4}^2} \cdot \frac{dV_{gs}}{dV_g}$$ \hspace{1cm} (33)

where $\frac{dV_g}{dV_g} \approx 1$ due to the high impedance of M3.

We note that this value could easily be as low as 1 (e.g. consider the case of $\Delta V_{\text{mid}} = 0.5V$ and $V_{gs} = 0.7V$). This means that for every Volt of change in $V_{CM}$ the gain deviates by a unit (e.g. $G = 25$ at $V_{CM} = xV$ means $G = 26$ at $V_{CM} = (x-1)V$). Nevertheless, for indicative values of $G = 25$ and $V_{CM}$ fluctuations in the low 100s of mV we obtain gain deviations/errors in the order of 1%.

III. PERFORMANCE MEASUREMENTS AND RESULTS

In this section, the suitably defined performance parameters from the previous section will be assessed for an example design in simulation. We split the results into two groups for convenience: differential mode and common mode effects. Under differential mode-related effects we examine the differential gain, bandwidth, and tunable range/sensitivity of offset vs. RRAM device resistive state. Under ‘Common mode-related effects’ we include input range (largely determine by the common mode by assumption) and CMRR/CMGD. Finally, power consumption is discussed on its own at the end.
A. Differential Mode Effects

1) Gain: For the purposes of amplifier gain analysis, we have run multiple, single data-point amplification transients sweeping a range of input differential voltages centred around zero. These simulations are under nominal conditions for this study: no added noise, mismatch or process variation was included.

There are two main experiments: First we set an integration phase run where \( \delta V_{in} \neq 0 \) and the \( \text{clk} \) signal does not interrupt the integration process, but rather lets it run its course until both \( V_{mid,a/b} \) saturate. Thus, the important features of the resulting waveform (e.g. position of peaks) are revealed. A key question we seek to answer here is whether there is an optimum time to stop the amplification in order to reliably obtain maximum gain, and if so when that occurs. The second experiment uses a fixed clock allowing us to explore the gain linearity for fixed integration period: we run multiple simulation runs with \( \delta V_{in} \) swept from \(-100\mu V\) to \(100\mu V\) with integration period \( \tau = 150\text{ns} \). The key question here is whether the amplifier has a usable linear range centred around the 0V differential input and if so, how wide it is.

The first experiment is illustrated in Fig. 5(a). We observe that for all test inputs \( \delta V_{in} \in \{-100, -50, -5, 5, 50, 100\} \mu V \) \( \Delta V_{mid} \) increases linearly to a global peak at \( \approx 170\text{ns} \) into the integration phase and then gradually decreases to zero, at which point both \( V_{mid,a/b} \) have saturated and any potential difference they had is erased. The peak occurs because as we keep integrating, the voltage at \( mida/b \) nodes eventually increases to the point where the cascode transistors enter the triode mode. This causes the rate of voltage accumulation on whichever \( V_{mid} \) node is highest to slow first, allowing the other node to catch up (and leading to the post-peak drop in \( \Delta V_{mid} \)). At this point we are past maximum gain and continuing the integration eventually equalises the \( V_{mid,b} \).

Next, we note that the peak gain time is nearly perfectly aligned for all input samples; the maximum peak time difference is only 1ps. The high quality of alignment arises because the time at which the \( V_{mid} \) voltages start trioding the cascode transistors is determined primarily by the tail current and not the differential currents. The small discrepancy is explained by the fact that the peak gain time is technically determined by the time at which the first of \( V_{mid,a/b} \) reaches the point where it triodes its cascode transistor. This has two key engineering implications: 1) It allows us to set a universally optimal DLC triggering time. 2) It states that the optimal trigger time is bounded by the trioding time obtained for \( V_{mid,a} = \min \) and \( V_{mid,b} = \max \) (or vice versa), in which case we have the fastest trioding corner.

The results from the 2nd experiment are shown in Fig. 5(b). The differential output voltages \( \delta V_{mid} \) for \( \tau = 150\text{ns} \) are plotted versus input differential voltage \( \delta V_{in} \). We notice excellent gain linearity arising again from the extremely small effect that the differential voltages have on the behaviour of the voltages at \( V_{mid,a/b} \). For this experiment the differential input voltage was swept on the basis of a fixed input \( V_{mid} = 1.1V \) and a swept input \( V_{in} \in [1.1V - 100\mu V, 1.1V + 100\mu V] \). Results were linearly fitted yielding a gain of \( G = 25V/V \) (28dB) with excellent linearity throughout the range (MSE = 0.0011).

2) Bandwidth: We operated our amplifier with an integration period of 150ns as shown in Fig. 3 and ran a collection of transient analyses for fixed amplitude pure tone signal inputs. The tone frequencies ranged from 1Hz to 27MHz (covers around four cycles of window) and for each frequency the phases where stepped in increments of 10°. Additionally we also carried out a DC run (\( \delta V_{in} = 100\mu V \)). For each simulation run we looked at the amplifier output \( \delta V_{mid} \) after 150ns of integration. The outcome was a plot of maximum \( |\delta V_{mid}| \) as a function of frequency, as illustrated in Fig. 6 (normalised to \( |\delta V_{mid}| \) at DC). The resulting curve is closely bounded by the envelope calculated by Eq. 1 indicating no surprises. To keep \( \lambda > 20\% \), the bandwidth achieves four fifths cycles/window period in Fig. 6 that yields 5.4MHz bandwidth.
We note that if we assume that the highest frequency spectral component of interest in a neural spike lies at 10kHz, the maximum attenuation of this particular design is around 0.08%. Therefore we can reliably sample spiking waveforms with this design.

3) Tuneable Range and Tuning Sensitivity: To obtain the tuneable range and sensitivity of implanted memristive devices, multiple transient simulations such as those seen in Fig.2 can be repeated while sweeping both RRAM device resistive states (R1 and R2). By tracking at what difference \( \Delta V_{in} \) the outputs flip value we can obtain an estimate for the offset. The quality of the estimate is calculated as follows: if at cycle \( n \) we had \( V_{outa} = 0 \) and at cycle \( n + 1 \) we obtained \( V_{outa} = 1 \), it means that somewhere between \( \delta V_{in} \) and \( \delta V_{in}(n+1) \) we crossed the amplifier’s offset voltage. The tracking will be applied in both ascending and descending phase, after which offset voltage will be averaged. Assuming that the amplifier always makes a decision at approximately the same relative time in each cycle (in our case always at 150ns into the integration phase), the duration of this interval is fixed and given by the total swept range over the number of sampling cycles. In our case, we run 200 cycles (10μs/cycle for a total duration of 2ms) and sweep the input across a range of 400μV (200μV ascending and 200μV descending).

Table II shows the offset voltage as a function of \( R1, R2 \). From there we observe: 1) The overall trimming range for this particular design is \( \approx 235μV \). 2) The maximum induced offset occurs, as expected, at the maximum, \( R1, R2 \) imbalance corners. 3) The offset sensitivity is close to 1μV/kΩ for any combination of \( R1, R2 \). 4) The table is almost symmetric (as expected). The slight asymmetry indicates that the common mode voltage influences the offset voltage. This effect will be the subject of a dedicated study. Finally, the quoted offsets were checked and are the same both on the upward and the downward slopes, indicating no history-dependence.

### Table II

| R1 [kΩ] | R2 [kΩ] | 10kΩ | 100kΩ | 1000kΩ | 130kΩ |
|---------|---------|------|-------|--------|-------|
| 10kΩ    | 0       | 35   | 60    | 90     | 120   |
| 40kΩ    | -35     | 0    | 25    | 55     | 95    |
| 100kΩ   | -25     | 0    | 25    | 55     | 95    |
| 130kΩ   | -85     | -50  | -25   | 0      | 30    |

4) Input-Referred Noise: To estimate the noise behaviour we employ the following trick: we take the core of the basic circuit shown in Fig.1 balance the inputs and add a pair of ideal, noiseless resistors that sink the baseline value of \( t_{tail}/2 \) for some suitably chosen equilibrium voltage \( V_{mid}=V_{equil} \) within the amplifier's integrating range. This is shown in Fig.7(a) (note that we have removed M17&M18 for simplicity - they only increment node capacitance by a small fraction). Then, we need to run our noise analysis and apply the sinc moderation (Eq.11) in order to obtain our final results.

Before we begin, we need to make some key observations/assumptions: 1) At DC equilibrium, what is left on \( V_{mid} \) after removing the baseline tail currents is fluctuations due to noise; there is no other possible source of fluctuation. 2) Any distortions introduced by the finite impedance of the compensation resistors is negligible due to the minute input signals at play. 3) Input-referred output noise levels are expected to be comparable throughout the entire integration range given that most of the noise is generated by the input differential pair. Additionally, running the noise test at half-gain is compensation against underestimating the noise generated by other sources (most notably the cascode pair). Now we can run our noise analysis.

For baseline compensation resistances \( R_{comp} = 330kΩ \), we get \( V_{equil} \approx 0.5V \) and a noise spectrum (with and without sinc moderation) as shown in Fig.7(b). Across a \( 0.05Hz – 50MHz \) bandwidth we obtain a root-mean square (RMS) voltage noise level of \( \approx 350μV \) unmoderated, dropping to \( 34μV \) moderated. This represents a saving of \( \approx 90\% \). We also observe a 1/f corner frequency around 250Hz. We have tested that expanding the included noise bandwidth both to the left and to the right does not change the above figures significantly. The present analysis excludes noise contributions from the RRAM devices.

The overall result suggests that for neural probing, the noise levels obtained for this design may still be slightly too high, especially if we include additional noise from the RRAM devices. In this case switching to longer integration periods would help.
B. Common Mode Effects

1) Input and Range: In order to experimentally demonstrate the input range of the amplifier we performed a series of experiments querying different potential range limitation factors in practice. First, we checked the behaviour of the system at different stages as a function of common mode voltage by running a series of integration cycles whilst sweeping $V_{CM}$ from $0V$ to $VDD$ in steps of $50\mu V$. At each run the differential input was $50\mu V$ and the outputs were registered after integrating for $150ns$. Results were registered at: i) $V_{midb}$, ii) $\delta V_{mid}$ and iii) the overall system output after the DLC. Results are shown in Fig. 8. Note: in order to check for possible input signal history-dependence during these tests, each test integration cycle was preceded by three integration cycles ran with $V_{CM} = 1.8V$. We have sample-tested a few runs with initial $V_{CM}$ between $0.1V$ and $1.8V$ and confirm that the history-dependence effect is negligible.

From the results in Fig. 8 we can draw three key conclusions: 1) The DLC successfully triggers for $V_{CM}$ between approx. $0.5V$ and $1.4V$. This means that $V_{midb}$ is sufficiently high for the DLC to settle to an output within $50ns$ of it triggering (which occurs when clk goes high). 2) In this case the DLC provides the correct answer so long as it triggers, but this might change towards the edges of the range once we take noise into account. 3) The actual analogue gain of the amplifier remains close to maximum ($\approx 28dB$) within a narrower region: approx.$[0.9, 1.3]V$. We would recommend that maximum gain area is taken as the effective $V_{CM}$ range in order to maximise the chances of correctly capturing small differential inputs under noisy conditions. Nevertheless, this shows that by de-rating the specification of the amplifier to higher $\delta V_{mid}$ we can extend its effective input range.

In order to visualise the effects leading to loss of gain outside the region $V_{CM} \in [0.9, 1.3]V$ we ran some unrestricted integration tests as shown in Fig. 5 for different values of $V_{CM}$. The results are shown in Fig. 9, where we observe that for $V_{CM}$ between $1.0V$ and $1.3V$ the integration traces follow each other very closely, with traces at $0.9V$ and $1.4V$ beginning to show more substantial deviations. We note how excessively low $V_{CM}$ shortens the peak without shifting (a result of desaturating the input differential pair but not changing the integration range) whilst excessively high $V_{CM}$ shifts the peak without changing its magnitude.

2) CMRR and CMGD: For evaluating the CMRR we set the differential input to $0V$ and swept $V_{CM}$ between $[0.9, 1.4]V$. Since we deliberately don’t account for process variations and mismatch in this work, we obtain the expected common mode gain of 0.

For CMGD, we run a series of integration runs with fixed differential input voltage ($50\mu V$) and sweep $V_{CM}$ in steps of $10\mu V$ and plot the gain as illustrated in Fig. 10(a). The highlighted region where the gain maximises is then resampled at $5\mu V$ step and for each consecutive pair of data points we calculate the derivative. As per Eq 33 this yields our CMGD. Converting approximately we obtain $CMGD \geq 20dB$ for $V_{CM} \in [0.99V, 1.14V]$. To exemplify this effect, a $0.15V$ change in common mode voltage $\Delta V_{CM}$ causes less than $1.5\%$ change in the output of the amplifier core ($\frac{dG}{dV_{CM}} \Delta V_{CM}$).

C. Power Consumption

The power consumption has to be assessed for all operating phases of the pre-amplifier. The most power-hungry phase is the reset phase since it is the only one where a DC path exists between the power supplies. For this reason the reset phase should be kept as short as possible. However, it is also during the reset phase that the core amplifier reaches steady state at all nodes so that the integrating phase can then commence without any history-dependence, i.e. influence from or ‘memory of’ its previous inputs. Finding the optimal reset phase duration is a key optimisation task for this design. Next, the cost associated with the integration and digitisation phases can be split into two main components: First, the integration cost is equal to charging the core amplifier’s capacitors from GND to their equilibrium level, where the integration self-terminates ($\approx 1.26V$ in our case - note how this integration cost currently spans both integration and digitisation phases because we do not stop the integration once we trigger the DLCs). Second, the comparison cost is equal to the energy...
needed to operate the DLC. Finally, during the ‘off’ phase power dissipation is mainly down to leakages.

Through one detection cycle (350ns), the average energy consumption is 1.927pJ, of which 663fJ during the reset phase, 814fJ during the integration phase and 450fJ during digitalisation. This yields a power rating of 5.5μW for continuous operation (no off phase), of which the core amplifier accounts for 5μW. If we operate the amplifier at typical biointerface sampling rates of ≈ 20kHz, power dissipation becomes 38.5mW (assuming practically zero ‘off’ mode dissipation).

For a more complete, multiple channel pre-amplifier, additional power will be dissipated by 1) the current reference generation unit (III in Fig.1, 2) the control system, including clk_ana, clk_anabar, clk_rst and clk generators. Both of the above would be shared across multiple channels, yielding a certain degree of amortisation.

IV. DISCUSSION

From the analysis and simulation of the integrating amplifier we highlight some key conclusions:

First, the performance improvement of the integrating amplifier over more traditional e.g. Harrison designs relies on the integration process, which enhances the gain and decreases the effective bandwidth (helping reduce noise in the process). To visualise this let us consider an integrating amplifier using the same tail current as a standard OTA first stage. During integration the power dissipation is effectively the same, but the gain and bandwidth are different. In this sense the design represents a trade-off between gain and bandwidth without changing power dissipation or using feedback.

Next, we note that there is a natural trade-off between tail current and integration time while keeping the overall energy dissipation approximately constant. This is the result of the fixed duration of the reset phase (just enough to clear any residual charge at the $V_{mid}$ nodes) and the fact that energy consumption during the integration phase only depends on the size of the load caps and the voltage change across them during that phase. Thus, in principle we can design for a wide range of required sampling rates or bandwidths for the same energy budget.

The trade is not completely free: Changing the tail current affects gain, bandwidth and noise performance, by altering the $g_{mS}$ of all transistors involved and the integration period. Furthermore, if using real RRAM devices with non-linear IV curves, changing the tail current also changes the static resistance of the RRAM devices. Together with changes in transistor $g_{mS}$ this means that the tunability range is also affected since it depends on the impedance balance between RRAM and transistors. Thus, whilst the integrating amplifier clearly offers a lot of design flexibility, the precise design trade-off space is also not trivial, much like it is for OpAmps. This is an important subject meriting its own dedicated study.

The last design decision to highlight concerns the size of the load capacitors $C$. The gain analysis in section II shows that $C$ doesn’t affect the gain, but it does affect the integration period and therefore can be used to adjust the bandwidth, if for some reason that cannot be achieved by tweaking the tail current. Effectively it is a design parameter that trades away energy for design flexibility.

In terms of operation, we note the importance of ensuring that the integrating amplifier is cleared properly in preparation for each integrating phase in order to avoid history-dependence of the output. This means that all node voltages should be equalised across the left and right branches prior to the commencement of the sensitive integration phase. In the current design this is achieved by forcefully flushing the system during the reset phase, but more energy-efficient approaches are under development as the rest phase represents a substantial fraction of the energy budget.

Finally, we compare our amplifier’s performance with a few standard designs as shown in Table III. We observe a slightly reduced gain and increased noise levels traded against power dissipation as a result of our design decisions so far. Importantly, for relatively low precision operations such as threshold detection of neuronal spikes a 10-fold increase in noise may be an acceptable price for a 100-fold reduction in power dissipation. We also note that the present design is not completely optimised, with an increase in integration time as a very promising avenue of investigation for decreasing noise levels within the same power envelope.

| Table III | PERFORMANCE AND COMPARISON OF THE PROPOSED AMPLIFIER, IRN: INPUT-REFERRED NOISE |
|-----------|-------------------------------|
| Work | [20] | [26] | [27] | This work |
| Tech. ($\mu$m) | 1.5 | 0.18 | 0.18 | 0.18 |
| Power (W) | 40μ | 3.2μ | 1.5μ | 38.5m@20kHz |
| BW (Hz) | 7.5k | 8.1k | 10k | 8.4M |
| IRN @freq. ($\mu$Vrms) | 2.1 | 2.14 | 3.4 | 34 |

Note: Table III shows the performance and comparison of the proposed amplifier with other designs. IRN stands for Input-Referenced Noise.
V. CONCLUSION

In this work we have performed a theoretical analysis of the core functionality of memristive integrating amplifiers and used industrial CAD-level simulations to provide a specific example for an integrating amplifier design targeting electrophysiological applications. Throughout our analysis we have concluded that the performance enhancement over traditional, continuous mode amplifiers can be most intuitively understood as a gain boosting effect arising from the integration process and showed how this process erodes the amplifier’s effective bandwidth (which is desirable for electrophysiology applications). Moreover, we have explained how standard metrics of amplifier performance such as gain and input common mode range, but also new metrics such as offset voltage tunability range can be described by governing equations for use by designers. Finally, we implemented an exemplar design in commercially available 180nm CMOS and demonstrated typical values for all studied performance parameters that can be expected from a 0.18μm node technology. These included gain of 25V/V, offset tuning range of 235µV, input-referred noise of 34µVRms and power dissipation of 38.5nW at 20Hz sampling rate. These are competitive vs current literature for an not fully optimised design.

This work is a stepping stone towards de-risking and documenting the RRAM-based integrating amplifier. We believe that the trade-off induced by the integration process in combination with the offset trimming enabled by RRAM has the potential to add a powerful circuit topology to the arsenal of the analogue designer.

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