A 30 MHz–3 GHz watt-level stacked-FET linear power amplifier

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Abstract In this letter, we present a 30 MHz–3 GHz ultra-broadband GaAs stacked power amplifier (PA) fabricated in 0.15 µm pHEMT process for many applications. The implemented PA obtains 18.9 dB gain by using novel input matching networks, and better than 10 dB input and output return loss. The large-signal measurements show that the output power is 30.5 dBm at 12 dBm input power, with a peak PAE of 30% at 400 MHz. For multi-standard system usage, the broadband PA also shows good linearity when tested with two tones and long-term evolution (LTE) signal.

Keywords: GaAs pHEMT, ultra-broadband, stacked power amplifier
Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

The RF transmitter is experiencing the rapid evolution, so that more concerns have been put on the bandwidth of PAs [1, 2]. The transmitters in Wireless communication and electronic warfare (EW) often operate in different standards that contain various frequency bands. The 30 MHz–3 GHz containing very-high frequency (VHF) band and ultra-high frequency (UHF) band is applied in many commercial and military situations, so the broadband PAs over this bandwidth are needed to substitute narrowband PAs.

It is difficult for a PA to improve the bandwidth, output power, efficiency and linearity simultaneously, especially for the multi-octave PA. There are several possible broadband PA structures. The distributed amplifier has a good bandwidth performance because its gain is independent on the frequency, but it has low output power and efficiency [3, 4, 5]. The resistive feedback is easy to design, with the disadvantage of high power loss [6]. Harmonic-tuned amplifiers operating in high-efficiency switch-mode rely deeply on complex harmonic impedance match, resulting in a limited bandwidth [7, 8].

Stacked configuration is another important method for broadband PAs [9, 10, 11]. With several same transistors stacked in the PA, the bandwidth and output power are enhanced. Furthermore, the output impedance also increases in broad frequency range, which makes better return loss possible. Although stacked PA can be fabricated by different materials [12, 13, 14, 15], GaAs is the most mature process for mid-power PA with good linearity [16, 17, 18, 19, 20].

During recent years, stacked structure is widely researched in high frequency [21, 22, 23, 24, 25, 26, 27, 28, 29], but seldom referring to low frequency. Moreover, most reports put little attention on linear performance in broadband circuit design, which is critical in RF communication system.

Thus, an ultra-broadband PA designed in 0.15 µm GaAs pHEMT process was proposed, covering lower frequencies from 30 MHz to 3 GHz. It employs a novel input matching network to flatten gain and improve S11 and a power combiner to match the fundamental and second harmonic impedances. The PA was tested with single-tone, two-tone and LTE signals to show a good linearity. The measurement results demonstrate an outstanding overall performance of bandwidth, flatness, output power and linearity.

2. Circuit design

Fig. 1 shows a schematic of the parallel-combined power cells. It is highly symmetrical and half schematic is plotted. Each single part includes three stacked transistors with the same size of 16 × 150 µm. The gate capacitors C₁ and C₂ are used for adjusting the internal impedance match so that the power from each device can be delivered from bottom to top with low reflection loss [23]. The shunt resistors R₁, R₂ and R₃ that are connected to the gates serve as the DC biasing network, while R₄ and R₇ between gate feeds and drain feeds are isolation resistors to prevent odd-mode oscillations.
The transistor gain normally has a 6 dB roll-off for each octave, so it is quite difficult to equalize the gain for an ultra-broadband PA. A novel structure of the Parallel Resistor and the Microstrip line (PRM) was proposed in a dashed rectangle in Fig. 1 to improve the gain flatness. The microstrip line’s electrical length is the quarter wavelength at 18.2 GHz. The quarter-wave short circuited stub is a narrowband network, which is known as the RF choke that can provide a bias point; however, here the similar PRM’s narrowband performance is designed to match the circuit gain feature. In Fig. 2a, the PRM insertion loss in blue line, simulated by directly paralleling it between two terminals, increases with frequency declining. With the two PRMs’ help, the circuit gain in black line drops to different extent that dependent on frequency, resulting in a flat gain showed by the red line. The compensation is proper below 0.5 GHz while unflat above 2 GHz because of high-frequency parasitic effect forming choke to prevent power leak. On the other hand, the series resistor in PRM also helps the input return loss S11 move along the constant conductance circle and transforms the input impedance to 50 ohms nearby, especially for the low-end frequency that is difficult to adjust by microstrip line. Fig. 2b shows the input impedance with and without PRMs part.

Fig. 2. (a) Simulated small signal gain compensation and (b) simulated input impedance with (red line) and without (blue line) PRMs.

Due to resistive losses in the transistor and phase misalignment of the drain voltage, the effect of improving the combined power through stacking transistor is limited [22]. So the parallel combiner is used to achieve a higher output power. In addition, the combiner works as an impedance transformer. In Fig. 3, the load-pull simulation results show a series of optimized load impedances for fundamental (ZL_opt) and high PAE area for second harmonic (ZL_2nd harmonic). For the proposed multi-octave broadband PA, the second harmonics of the low-end frequencies, such as 30 MHz–1.5 GHz, will occur in the passband. To avoid having impacts on fundamentals, the second harmonic is decided from 3.1 GHz–6 GHz. The 0.03 GHz–6 GHz load impedance curve in Fig. 3 represents for the simulated input impedance of the output matching network in Fig. 4. The typical frequency points are marked with the same legend colors. The load impedance is close to the optimized fundamental impedance circles and get into high PAE area for second harmonic matching, especially well matched in 0.1 GHz–2 GHz for fundamental and 4 GHz–6 GHz for second harmonic. Considering the costly chip price and large network area, the output matching network is fabricated off the chip using printed circuit board (PCB).

Fig. 3. Simulated input impedance of the combiner and the circled optimized fundamental and second impedance.

Fig. 4. Off-chip output matching network

3. Experiment result

An integrated chip was fabricated using 0.15 μm GaAs pHEMT process of WIN Semiconductors. Fig. 5a shows the die micrograph of the PA. The size of the chip including pads is 1.930 × 1.780 mm². The chip is wire-bonded to a 30 mils Rogers 4350B PCB to connect the biased network and output matching network, which is shown in Fig. 5b. In biased network, the conical inductors block the RF signal over the whole bandwidth and the bypass capacitors can couple ripple resulting from the DC signal. The PA was biased at Vgs = 0.5 V and Vds = 12 V, working at class AB.

The S-parameter and power performance of the broadband PA has been measured with small-signal and large-signal excitation. As shown in Fig. 6, the proposed PA is unconditional stable due to Rollett factor K larger than 6.7 and achieves an 18.9 dB gain with a fluctuation inside 0.9 dB from 30 MHz–3 GHz. In addition, the PA achieves a good input and output return loss that is better than 10 dB for most frequencies. The simulated results agree well with the measured results. The power performance was measured by a continuous-wave (CW) signal. The Fig. 7 illustrates the simulated and measured output power (Pout) and power added efficiency (PAE) at 12 dBm constant input power. The black drop lines indicate the degree of power compression. The output power is 30.5 dBm ± 1.2 dB. The power compression degree is moderate, merely exceeding 3 dB beyond 2.7 GHz. The peak PAE is 30% at 400 MHz and drops to 21% at 3 GHz. This broadband amplifier can
be applied in many fields, such as land mobile radio service (LMRS), Global System for Mobile Communications (GSM), Universal Mobile Telecommunications System (UMTS), and Long Term Evolution (LTE).

Because signals represented by discrete spectra can no longer fully predict the system’s performance when considering the current complex modulation techniques and baseband algorithms, the linearity was tested by two tones with 1 MHz spacing and 20 MHz LTE signals with 7 dB PAPR. Fig. 8 shows the third-order intermodulated products (IMD3) as a function of the output power at 100 MHz, 1 GHz and 2.1 GHz, which is below $-30$ dBc when output power is 26 dBm.

Besides, the adjacent channel leakage radio (ACLR) is defined by upper x axis and right y axis and represented by black line. The measurement data shows ACLR is below $-30$ dBc in most frequencies at an average of 23 dBm output power without applying predistortion.

Table I compares the performance of recently reported GaAs pHEMT broadband PAs. The results of FOM (figure of merit) exhibit that the proposed PA achieves the best performance.

### 4. Conclusion

In this letter, a 30 MHz–3 GHz stacked broadband PA is presented, which is fabricated in 0.15 μm GaAs process. A novel input match method to improve the flatness and input return loss has been proposed. The output matching network is designed by harmonic load pull to achieve optimal power and PAE performance. The results indicate that the proposed PA design has state-of-the-art performance. This ultra-broadband medium power amplifier is a good choice for multi-standard system.

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### References

[1] D. Chen, et al.: “A package-level wideband driver amplifier with 134% fractional bandwidth,” IEICE Electron. Express 15 (2018) 20180179 (DOI: 10.1587/exlex.15.20180179).
[2] J. Li, et al.: “Multiband and multimode concurrent PA with novel intermodulation tuning network for linearity improvement,” IEEE Microw. Wireless Compon. Lett. 28 (2018) 248 (DOI: 10.1109/LMWC.2018.2794819).

[3] H.-F. Wu, et al.: “A compact ultrabroadband stacked traveling-wave GaN on Si power amplifier,” IEEE Trans. Microw. Theory Techn. 66 (2018) 3306 (DOI: 10.1109/TMTT.2018.2828434).

[4] X. Zhou, et al.: “1-W, highly efficient, ultra-broadband non-uniformly distributed power amplifier in GaN,” IEEE Microw. Wireless Compon. Lett. 23 (2013) 208 (DOI: 10.1109/LMWC.2013.2250270).

[5] K. W. Kobayashi, et al.: “A novel 100MHz–45GHz input-termination-less distributed amplifier design with low-frequency low-noise and high linearity implemented with a 6 inch 0.15μm GaN-SiC wafer process technology,” IEEE J. Solid-State Circuits 51 (2016) 2017 (DOI: 10.1109/JSSC.2016.2558488).

[6] S. Hu, et al.: “A 0.2–6GHz linearized Darlington-cascade broadband power amplifier,” IEICE Electron. Express 15 (2018) 20180298 (DOI: 10.1587/elecom.15.20180298).

[7] P. Jia, et al.: “A 0.25–1.25-GHz high-efficiency power amplifier with computer-aided design based on optimized impedance solution continuum,” IEEE Microw. Wireless Compon. Lett. 28 (2018) 443 (DOI: 10.1109/LMWC.2018.2814483).

[8] A. A. Nawaz, et al.: “Harmonic tuning of stacked SiGe power amplifiers using active load pull,” IEEE Microw. Wireless Compon. Lett. 28 (2018) 245 (DOI: 10.1109/LMWC.2018.2801027).

[9] Y. Park, et al.: “X-to-K band broadband watt-level power amplifier using stacked-FET-UNIT cells,” IEEE Radio Freq. Integr. Circuits Symp. (2011) 1 (DOI: 10.1109/RFCIC.2011.5940620).

[10] D. Fritsche, et al.: “Analysis and design of a stacked power amplifier with very high bandwidth,” IEEE Trans. Microw. Theory Techn. 60 (2012) 3223 (DOI: 10.1109/TMTT.2012.2209439).

[11] H. F. Wu, et al.: “Analysis and design of an ultrabroadband stacked power amplifier in CMOS technology,” IEEE Trans. Circuits Syst. II, Exp. Briefs 63 (2016) 49 (DOI: 10.1109/TCSII.2015.2504926).

[12] D. P. Nguyen, et al.: “A 1.5–88GHz 19.5 dBm output power triple stacked HBT InP distributed amplifier,” IEEE MTT-S Int. Microw. Symp. Dig. (2017) 20 (DOI: 10.1109/MWSYM.2017.8059080).

[13] M. M. Tarar, et al.: “Efficient 2–16GHz flat-gain stacked distributed power amplifier in 0.13μm CMOS using uniform distributed topology,” IEEE MTT-S Int. Microw. Symp. Dig. (2017) 27 (DOI: 10.1109/MWSYM.2017.8059102).

[14] S. Porpnromlikit, et al.: “A watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS,” IEEE Trans. Microw. Theory Techn. 58 (2010) 57 (DOI: 10.1109/TMTT.2009.2036323).

[15] J. J. Yan, et al.: “Design of a 4-W envelope tracking power amplifier with more than one octave carrier bandwidth,” IEEE J. Solid-State Circuits 47 (2012) 2298 (DOI: 10.1109/JSSC.2012.2204927).

[16] M. Meighdadi and A. Medi: “Design of 6–18GHz high-power amplifier in GaAs pHEMT technology,” IEEE Trans. Microw. Theory Techn. 65 (2017) 2353 (DOI: 10.1109/TMTT.2017.2680431).

[17] S. Li, et al.: “A broadband high efficiency monolithic power amplifier with GaAs HBT,” IEICE Electron. Express 15 (2018) 20180245 (DOI: 10.1587/elecom.15.20180245).

[18] Y. H. Chow and T. Chong: “A high performance 2.4 GHz linear power amplifier in enhancement-mode GaAs pHEMT technology,” 34th European Microwave Conference (2004) 5 (DOI: 10.1109/EUMC.2004.183922).

[19] H. Zhang, et al.: “A novel tunable broadband power amplifier module operating from 0.8GHz to 2.0GHz,” IEEE MTT-S Int. Microw. Symp. Dig. (2005) 661 (DOI: 10.1109/MWSYM.2005.1516692).

[20] X. Ding and L. Zhang: “A high-efficiency GaAs MMIC power amplifier for multi-standard system,” IEEE Microw. Wireless Compon. Lett. 26 (2016) 55 (DOI: 10.1109/LMWC.2015.2505615).

[21] A. Agah, et al.: “Multi-drive stacked-FET power amplifiers at 90GHz in 45nm SOI CMOS,” IEEE J. Solid-State Circuits 49 (2014) 1148 (DOI: 10.1109/JSSC.2014.230892).

[22] H.-T. Dabag, et al.: “Analysis and design of stacked-FET millimeter-wave power amplifiers,” IEEE Trans. Microw. Theory Techn. 61 (2013) 1543 (DOI: 10.1109/TMTT.2013.2247698).

[23] Y. Kim and Y. Kwon: “Analysis and design of millimeter-wave power amplifier using stacked-FET structure,” IEEE Trans. Microw. Theory Techn. 63 (2015) 691 (DOI: 10.1109/TMTT.2014.2387846).

[24] J. Kim, et al.: “Q-band and W-band power amplifiers in 45-nm CMOS SOI,” IEEE Trans. Microw. Theory Techn. 60 (2012) 1870 (DOI: 10.1109/TMTT.2012.2193593).

[25] Y. Jin, et al.: “A bandwidth millimeter-wave power amplifier with 20 dB linear power gain and +8 dBm maximum saturated output power,” IEEE J. Solid-State Circuits 43 (2008) 1553 (DOI: 10.1109/JSSC.2008.922385).

[26] A. Agah, et al.: “A 34% PAE, 18.6 dBm 42–45 GHz stacked power amplifier in 45nm SOI CMOS,” IEEE Radio Freq. Integr. Circuits Symp. (2012) 57 (DOI: 10.1109/RFCIC.2012.6242231).

[27] F. Thorne, et al.: “Broadband high-power W-band amplifier MMICs based on stacked-HEMT unit cells,” IEEE Trans. Microw. Theory Techn. 66 (2018) 1312 (DOI: 10.1109/TMTT.2017.2772809).

[28] D. P. Nguyen, et al.: “A 28-GHz symmetrical Doherty power amplifier using stacked-FET cells,” IEEE Trans. Microw. Theory Techn. 66 (2018) 2628 (DOI: 10.1109/TMTT.2018.2816024).

[29] P. M. Asbeck, et al.: “Power amplifiers for mm-wave 5G applications: Technology comparisons and CMOS-SOI demonstration circuits,” IEEE Trans. Microw. Theory Techn. (2019) 1 (DOI: 10.1109/TMTT.2019.2896047).

[30] C.-Y. Chiang, et al.: “Monolithic wideband linear power amplifier with 45% power bandwidth using pseudomorphic high-electron-mobility transistors for long-term evolution application,” Jpn. J. Appl. Phys. 53 (2014) 110311 (DOI: 10.7567/JAP.53.110311).

[31] M. Sayginer and M. Yazigi: “A systematic design of 1.5–9GHz high power-high efficiency two-stage GaAs PHEMT power amplifier,” Int. J. RF Microw. Comp.-Aided Eng. 24 (2014) 615 (DOI: 10.1002/mnew.20806).

[32] K. Fujii: “A DC to 22GHz, 2W high power distributed amplifier using stacked FET topology with gate periphery tapering,” IEEE Radio Freq. Integr. Circuits Symp. (2016) 270 (DOI: 10.1109/RFCIC.2016.7508303).