Real-Time Betatron Tune Correction with the Precise Measurement of Magnet Current

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Abstract—The betatron tune, which is defined as the number of transverse oscillations in one turn of a ring accelerator, is one of the most important parameters. An undesired betatron tune increases the amplitude of the transverse oscillation so that many particles are lost from the ring sooner than designed. Since a betatron tune is controlled by the magnetic fields in the ring, the ripple of the magnet current directly displaces the betatron tune from its designated value. We have developed a system that corrects the betatron tune displacement using the measured magnet current at the J-PARC (Japan Proton Accelerator Research Complex) Main Ring. We adopted Field Programmable Gated Arrays (FPGA) to convert from the measured magnet current to the betatron tune in real time. Using the system, we have decreased the fluctuation of the betatron tune $\sigma_{\nu}$ from $5.2 \times 10^{-4}$ to $3.3 \times 10^{-4}$ at the frequencies less than 250 Hz.

Index Terms—Proton synchrotron, Betatron tune, Optics correction, Field Programmable Grated Array, System-on-chip, Electromagnet, Current regulator

I. INTRODUCTION

Articles in an accelerator generally oscillate in directions perpendicular to the beam. This transverse oscillation is called the betatron oscillation[1]. The betatron oscillation is usually considered in two independent directions which are the horizontal and vertical directions. In this paper, the horizontal and vertical directions are indicated by $x$ and $y$, respectively. The transverse position of a particle in an accelerator is described as

$$\begin{align*}
x, y = \sqrt{\beta_{x,y}(s)s}e_{x,y}\cos[\phi_{x,y}(s) + \phi_{0,x,y}] 
(1)
\end{align*}$$

where $s$ is the distance along the reference orbit, $\phi_{x,y}(s)$ is the phase function, $e_{x,y}$ and $\phi_{0,x,y}$ are constants, and $\beta_{x,y}(s)$ is referred to as the betatron amplitude function. For a circular accelerator, the number of the oscillation in one turn is called the betatron tune, which is usually indicated by $\nu_{x,y}$. The betatron tune $\nu_{x,y}$ is written as

$$\nu_{x,y} = \frac{1}{2\pi} \int_C \phi_{x,y}(s)ds
(2)$$

, where the $C$ indicates the line integral along the ring. The design and control of the betatron tune is one of the most important tasks for ring accelerator operation. Inappropriate betatron tunes, which satisfy the resonance condition described as

$$ln\nu_x + m\nu_y = n, (l, m, n : integer)
(3)$$

may excite amplitude growth of the transverse oscillation which causes beam losses.

In general accelerator tunnels, many magnets including dipole (bending), quadrupole and sextupole are located along the ring. These magnets are in charge of controlling the parameters of the betatron oscillation. Many of these magnets are electromagnets that consists of magnetic materials and coils. Since the magnetic field of an electrode-magnet is controlled by the current through the coil, the precise current regulator is the key to the stable operation[2]. However, the magnet current regulators can not be always optimized for precise regulation since accelerator facilities are usually multi-purpose. For instance, the J-PARC Main Ring (MR)[3] provides proton beams to experiments via two different extraction modes. One is called “the fact extraction” (FX), which is used for the neutrino production. Since the neutrino production requires many primary protons, the beam is accelerated as fast as possible, and immediately extracted in the FX mode. To ramp the magnets faster, high voltage current regulators is mandatory. The other is called “the slow extraction” (SX), which is used for the hadron and nuclear experiments. In these experiments, temporal uniformity of the extracted beam intensity is required so that the number of charged particles that come to their detectors can be limited within their data acquisition performance. In the J-PARC MR, the temporal uniformity is achieved by controlling the betatron tune to slowly approach the resonance condition. This operation is apparently related to precise current regulation. However, high-voltage current regulators generally involves large and slow semiconductor switches, which prevent precise current regulation. In the J-PARC MR, the 4000 V 2000 A transistors are used at 450 Hz to drive the main magnets.

For more precise control of the betatron tune with the high voltage current regulators, we have developed a system that
corrects the betatron tune displacement using the measured magnet current. The schematic overview is shown in Figure 1.

In the system, the betatron tune is predicted by the measured magnet current in real time. The predicted betatron tune is used to drive the correction quadrupole magnet. For the real-time conversion from the magnet current to the betatron tune, FPGAs are adopted. The reason why the system must have real-time feature is that the magnet current ripples are generally not predictable since the regulators are affected by the fluctuation of the main AC grid voltage and frequency. The advantage of using the measured magnet current is non-destructive measurement for the beams. The magnet current is continuously measured for the feedback control of the regulators. Hence, the magnet current is always available as long as the regulators are under operation. On the other hand, the direct measurement of the betatron tune generally involves the excitation of transverse oscillations, which causes additional beam losses.

The paper is organized as follows. In Section II we will describe the experimental setup of our developed system including the details of the hardware. In Section III the betatron tune predicted by the system will be compared with the direct measurement. The result of the tune correction with the system will be shown in Section IV. Finally, we will summarize this paper in Section V.

II. EXPERIMENTAL SETUP

A. Overview

![The overview of the experimental setup is shown in Figure 2. The J-PARC MR uses 96 bending magnets and 216 quadrupole magnets. Six current regulators are used for all bending magnets while 11 for quadrupole magnets. All the 6 regulators for the bends and only the largest 2 regulators for the quadrupoles make dominant contribution to the betatron tune. This is the reason why we choose the 8 current regulators for the system. The current regulators of the main magnets are located in three different buildings (D1, D2 and D3), which are approximately 1 kilo-meters apart from each other. On the other hand, only one current regulator of the corrector is located at the one of them (D2). Therefore, the measured current of each regulator must be sent to the building where the corrector is located. For this purpose, we use existing optical fibers between the buildings. The fiber length is approximately 600 meters. Since there is no fiber between the D2 and D1, the signals from the D1 must go through the D3 before reaching the corrector located at the D2. The maximum delay caused by the data transfer between the buildings is approximately 6 μs, which is ignorable in comparison with the timescale of ΔI. The frequency-domain ΔI of the current regulator for the bends is shown in Figure 3. The dominant components are concentrated at the frequencies less than 100 Hz.]

![The FFT of the current deviation of the bending magnet power supply in the J-PARC MR.](image)

Each current regulator has analog monitor ports including the measured output current I_{out} and the current deviation. The current deviation is defined as ΔI = I_{ref} - I_{out} where the I_{ref} is the reference current. The I_{out} and ΔI are converted to digitized optical signals using the analog-to-digital converter board (AD board) located at each current regulator. The details of the AD board will be described in Section II-B. The FPGA board located at each building collects the I_{out} and ΔI signals from each AD board, and sends them to another building. At the final FPGA board at the D2, All ΔI signals are collected and converted to the betatron tune displacement, which is sent to the corrector. This is how we correct the betatron tune using the measured magnet currents. The hardware description of the FPGA board will be in Section II-C. Apart from the ΔI for the correction, the collected I_{out} and ΔI signals are sent to the upper network system via the Ethernet port of the FPGA board. These are used as the on-line monitors of the current regulators. The way to send the collected signals to the upper system will be described in Section II-D.

B. AD board

The conceptual block diagram and picture of the AD board are shown in Figure 4 and Figure 5, respectively. The 8-channels 16-bit analog-to-digital converter (Texas Instruments ADS8568) is adopted for the AD converter IC. The sampling frequency is set to 10 kHz in the system. The digital inputs for the control and digitized data output are all optical. Although the AD converter IC itself provides both serial and parallel digital outputs, the board only provides the serial digital output. The multiple boards can forms into “Daisy Chain” so that an additional board can be easily included in the
existing system by connecting the new board to the tail of the system. The upper four optical ports in Figure 4 are for the communication to the master. The AD conversion is triggered by the “Conversion Start” signal. It takes approximately 1.7 $\mu$s until the completion. After the AD conversion, the digitized data are transferred to the master via the “Data Out” port when the “Chip Select” port is asserted. The data transfer starts with the most significant bit of the first channel. The data is updated to the next bit in synchronization with the 20 MHz clock on the “Clock” port. Not only the data from the other channels but also from the other slave boards are also transferred through the “Data Out” port. The lower four optical ports in the figure are for the communication to the slave AD boards. The “Conversion Start”, “Clock” and “Chip Select” signals are sent to the slave boards using the first three ports out of the lower four. The digitized data of the slave boards are received via the “Data In” port.

Fig. 6: Conceptual block diagram of the developed FPGA board.

C. Hardware Design of the FPGA board

Fig. 7: Picture of the developed board.

Fig. 4: Conceptual block diagram of the developed AD board.

Fig. 5: Picture of the AD board.

The conceptual block diagram and picture of the developed board are shown in Figure 6 and Figure 7, respectively. We have adopted a System-on-Chip (SoC) FPGA for the intelligent component of the board. A single SoC FPGA chip, a processor, memory controllers and peripherals are integrated with the FPGA block. Hereinafter, these are collectively referred as to “micro-controller block” against the FPGA block. The details of the chosen SoC FPGA will be described in Section II-C0a. General purpose digital IO ports and 4-channel analog outputs are available in the board. The specific configuration of the SoC FPGA is loaded from a SD card or NOR flash memory. A single gigabit ethernet port is also available so that we can communicate with the board via a network. This FPGA board was originally developed as the multi-purpose intelligent I/O board for the J-PARC MR. The other applications are described in [4].

a) SoC FPGA: We have chosen a device from Altera Cyclone V SX Soc families. The device name is 5CSXC6. The FPGA block includes 41509 active logic modules, 5570 Kb internal memory, 112 variable-precision DSP blocks, 288 user I/Os. The micro-controller block includes dual processor cores (ARM Cortex-A9 MPCore), a hardened memory controller. The FPGA block is for functions specific to accelerator components. This block is very suitable especially for real-time applications such as power supply control, beam position feedback, low-level RF control and so on. This is because the functions in the FPGA block are configured as hardened circuits and the timing properties such as throughput and latency are exactly determined. An Linux operating system (OS) is executed in the micro-controller, which can internally communicate with the FPGA block. The DDR (Double Data Rate) 3 memory devices attached to the micro-controller block are used for the OS expansion. We execute one user program in the OS. The program can start and stop the operation of the functions implemented in FPGA block. In addition, it plays a role in changing the parameters of the functions. This gives us flexibility for designing circuits in the FPGA block with
variable parameters and states. The program also monitors the parameters and states. Some of the parameters and states are required for other accelerator components and must be remotely changed. To carry out these tasks, the program also works as a network socket server so that we can access the board from the outside through an Ethernet port.

b) User Memory Device: We have adopted 1GB DDR3 as a user memory device. This large memory storage is very useful especially for accelerators with relatively longer repetition periods. In those accelerators, the states of many accelerator components must vary with the proceeding of beam acceleration. For example, we must vary the currents for main magnets corresponding to the particle momentum. Therefore, we need to store not single value but a table of the reference current values. In additions, we usually need to apply some corrections to the accelerator components and the correction values may also be tables.

D. Firmware Design of the FPGA

Figure 8 shows the block diagram of the firmware on the SoC FPGA. This firmware corresponds to the final FPGA board located at the D2 building. There are two main data ($I_{out}$, $\Delta I$) streams in the firmware. One is for the conversion from the $\Delta I$ signals to the betatron tune displacement. This corresponds to the left part of Figure 8. The betatron tune displacement can be calculated as the linear combination of the $\Delta I$ signals ($\nu\Delta I = \sum_{i=1}^{n} \alpha_i \Delta I_i$). The coefficients $\alpha_i$, which are determined by the optics models of the J-PARC MR, are stored in the internal memory. After the conversion, the calculated tune displacement is sent to the corrector. The other stream is for the on-line monitoring. This is described in the right part of the figure. The received $\Delta I$ and $I_{out}$ are temporally stored in the DDR3 connected to the FPGA block. Once the data for one accelerator cycle (2.48 - 5.2 sec) are stored, they are transfered into the DDR3 connected to the micro-controller block with the DMA (Direct Memory Access) control. The network program running in the micro-controller block sends the transfered data to the upper system via the Ethernet port. The communication between the FPGA and micro-controller blocks can be done via a standard interface which is called “Intel Avalon Interface”.

III. COMPARISON WITH THE DIRECT MEASUREMENT

For the direct measurement of the betatron tune, we measure the frequency of the transverse oscillation excited by the stripline kickers [5]. This measurement is destructive and cannot be done for the user operation. Therefore, it is important to compare the predicted tune with the direct measurement during the beam study time. Figure 9 shows the comparison between the direct measurement and the prediction. Figure 9a shows the direct measurement while Figure 9b shows the prediction using the system. The corrector was turned off for this comparison. The tendencies of the time variation are roughly same although there are some discrepancies between them. There are possible reasons for the discrepancies. One possibility is the precision of the direct measurement. The transverse excitation at some time windows is not enough so that the betatron sideband can be hardly found. Another reason is that the prediction is not done by the all magnet current regulators as mentioned in Section II-A.

IV. BETATRON TUNE CORRECTION

To examine the effect of the system, we measured the betatron tune three times in the SX mode with the corrector turned on. For the comparison, the betatron tune without the corrector turned off is also measured. The upper three plots in Figure 10 show the measured betatron tunes with the corrector turned off while the lower three with turned on. The interval between the measured points is 2 ms. Hence, these plots are sensitive to the frequencies below 250 Hz which cover the dominant frequencies of the $\Delta I$ ($\leq$ 100 Hz). In the actual user operation, the beams are controlled to the resonance condition and slowly extracted during these measurement periods. Therefore, the fluctuation of the measured betatron tune in these plots must be smaller with the system. To check this more clearly, we also show the projection of these plots (histograms) in Figure 11 and performed the Gaussian fitting to these histograms. The upper three histograms correspond to the measurements with the corrector turned off while the lower three with turned off. The standard deviations of the fitted Gaussian are shown in Table I. The system reduces the fluctuation by approximately 43%.

| Shot 1     | Shot 2     | Shot 3     | Average   |
|------------|------------|------------|-----------|
| Corrector Off | 5.5 x 10^-4 | 4.6 x 10^-4 | 5.6 x 10^-4 | 5.2 x 10^-4 |
| Corrector On  | 3.4 x 10^-4 | 3.2 x 10^-4 | 3.2 x 10^-4 | 3.3 x 10^-4 |

V. CONCLUSION

The betatron tune, which is defined as the number of transverse oscillations in one turn of a ring accelerator, is one of the most important parameters. An undesired betatron tune increases the amplitude of the transverse oscillation so that many particles are lost from the ring sooner than designed. Since a betatron tune is controlled by the magnetic fields in the ring, the ripple of the magnet current directly displaces the betatron tune from its designated value.

We have developed a system that corrects the betatron tune displacement using the measured magnet current at the J-PARC MR. We adopted Field Programmable Gated Arrays (FPGA) to convert from the measured magnet current to the betatron tune in real time. The $\Delta I$ signals from the 8 magnet current regulators are used to calculate the betatron tune displacement. We have only one corrector magnet while these 8 regulators are located in different three buildings. Hence, the digitized $\Delta I$ signals at each regulator are sent to the building where the corrector is located through the optical fibers. We performed the direct measurement of the betatron tune with the system. The measurement shows that the system can decrease the fluctuation of the betatron tune $\sigma_\nu$ from 5.2 x 10^-4 to 3.3 x 10^-4 at the frequencies less than 250 Hz.
Fig. 8: Conceptual block diagram of the developed firmware on the SoC FPGA.

(a) The direct measurement of the betatron tune.

(b) The betatron tune prediction, which is calculated with the system (in real time)

Fig. 9: The comparison between the direct measurement and the prediction

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REFERENCES

[1] A.W. Chao et al., Eds., Handbook of Accelerator Physics and Engineering. World Scientific, 2012.
[2] Y. Kurimoto, Y. Morita, S. Nakamura, and T. Shimogawa, “Precise current control in accelerator magnets with a digital feedback system,” IEEE Transactions on nuclear science, vol. 61, no. 1, pp. 546–552, 2014.
[3] T. Koseki et al., “Beam commissioning and operation of the J-PARC main ring synchrotron,” Progress of Theoretical and Experimental Physics, vol. 2012, no. 1, p. 02B004, 2012. [Online]. Available: http://dx.doi.org/10.1093/ptep/pts071
[4] Y. Kurimoto and K. Nakamura, “Development and applications of a multi-purpose digital controller with a System-on-Chip FPGA for accelerators,” Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 840, no. 21, pp. 160–167, 2016.
[5] T. Toyama et al., “Beam Diagnostics at the First Beam Commissioning of the J-PARC MR,” in Particle accelerator. Proceedings, 23rd Conference, PAC’09, Vancouver, Canada, May 4-8, 2009, 2010, p. WE4GRc01. [Online]. Available: http://accelconf.web.cern.ch/AccelConf/PAC2009/papers/we4grc01.pdf
Fig. 10: The measured betatron tunes as a function of time. The upper three plots correspond to the measurements without the system while the lower three with the system.

Fig. 11: The histograms of the measured betatron tunes. The upper three plots correspond to the measurements without the system while the lower three with the system.