Extensive Analysis on the Effects of Post-Deposition Annealing for ALD-Deposited Al₂O₃ on an n-Type Silicon Substrate

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Abstract: In this study, an investigation was performed on the properties of atomic-layer-deposited aluminum oxide (Al₂O₃) on an n-type silicon (n-Si) substrate based on the effect of post-deposition heat treatment, which was speckled according to ambient temperature and treatment applied time. Based on these dealings, a series of distinctions for extracted capacitance and dielectric constant, hysteresis was performed on annealed and nonannealed samples. The interface and border trap responses, including stress behavior after an application of constant voltage for a specific time and surface morphology by X-ray diffraction (XRD) technique, were also analyzed between the two above-mentioned sample types. Based on observation, the annealed samples showed superior performance in every aspect compared with the nonannealed ones. Some unusual behaviors after high annealing temperature were found, and the explanation is the ion diffusion from oxide layer towards the semiconductor. Since a constant voltage stress was not widely used on the metal–oxide–semiconductor capacitor (MOSCAP), this analysis was determined to reveal a new dimension of post-deposition annealing condition for the Al/Al₂O₃/n-Si gate stack.

Keywords: Al₂O₃; ALD; constant voltage stress; diffusion; MOSCAP; PDA

1. Introduction

A large band gap and an exalted barrier height between the dielectric and Si has essential chemical, along with the thermal steadiness of the conventional dielectric material silicon dioxide (SiO₂), on silicon (Si) wafers [1–3]. However, the applicable SiO₂ layer thickness (which functions as the insulating layer) reaches its maximum owing to the miniaturization of metal–oxide–semiconductor field-effect transistors (MOSFETs). Because of direct tunneling through the SiO₂ film, low-power application devices mostly agonize from high leakage currents [4]. Nevertheless, the leakage current and equivalent oxide thickness (EOT), which are associated with the speed of the transistor, can be decreased with a denser oxide layer with a high dielectric constant (k). Among the different deposition techniques, such as physical vapor deposition, chemical vapor deposition (CVD), and atomic layer deposition (ALD) for high-k oxides, ALD [5–9] is considered the most promising technique for studying the microelectronic and nanotechnological characteristics of samples. Being a subtype of CVD, in ALD, at the same time in the deposition chamber, the precursors and oxidants are not only present but also introduced in a chronological and noncongruent way. The continuous purge gas flow eradicates residual precursors and reactant species between the precursor and oxidant inoculations. The combination of the precursor/oxidant pulses and purge gas flow is acknowledged as a half cycle; the film is deposited through this self-saturating half cycle because the reactions stop once all reactive components on the Si surface are devoured. Throughout this process, the reactions are eradicated by themselves [9]. Therefore, deposition occurs in a cyclic order in ALD, whereas it happens on a time basis in CVD [5]. The thickness of the deposited film can be accustomed to the number of deposition cycles. Thus, the self-saturating nature and cyclic deposition deliver amenable, disciplined, uniform, high-quality, condensed, and
pinhole-free thin films with thickness errors of less than 1%; the film growth is autonomous of the precursor and oxidant flux \([7,10]\). The different deposition procedures (including ALD) are comprehensively compared in \([9]\). \(\text{Al}_2\text{O}_3\), which is one of the studied high-\(k\) oxides, is considered to be one of the most auspicious substitutions for \(\text{SiO}_2\) because of its simple ALD manufacturing process \([11]\). \(\text{Al}_2\text{O}_3\) has a higher bandgap (approximately 8.8 eV) and band orientation analogous to \(\text{SiO}_2\), good thermal steadiness, and concentrated oxygen and ionic carriage, with a reasonable dielectric constant (\(k = 6–9\)) \([12,13]\).

Post-metal annealing (PMA) and post-deposition annealing (PDA) are two methods of rapid thermal annealing (RTA) used to observe the features of MOSCAPs. This observation can be conducted at different temperatures for different durations in an ambient gas environment. For the \(\text{Al}_2\text{O}_3\) MOSCAP, numerous research studies have been conducted on PMA characteristics \([14–16]\). In PMA, after the fabrication of the oxide layer and metal layer on the semiconductor, the MOSCAP is annealed at a specific temperature for a definite time in a suitable ambient gas condition. In PDA, the MOSCAP is annealed after the fabrication of the oxide layer and before the deposition of the metal layer. Researchers have discovered that a slowly increasing PMA temperature makes the capacitance value reduced and the leakage current enlarged. These outcomes signpost that PMA with aluminum electrodes is substantially subtle to the annealing condition compared with PDA \([17]\). Additionally, PMA ought to have higher value of equivalent oxide thickness (EOT) and interface state density as compared with PDA. Besides, there is no frequency dependence in the case of PDA found in the weak inversion region of capacitance–voltage (C–V) curves of PMA-annealed samples \([17]\). According to \([18,19]\), PDA can affect the capacitance, hysteresis, dielectric constant, and morphological structure, but constant voltage stress, interface, and border trap characterizations are not clearly stated in those articles. The shift in the threshold voltage after constant voltage stress should generally differ from MOSCAP to MOSCAP based on the annealing conditions (e.g., duration, temperature, and ambient gas environment). In this paper, all these attributes, along with the constant voltage stress for the Al/\(\text{Al}_2\text{O}_3\)/n-Si MOSCAP regarding PDA, are discussed.

The flat-band voltage, \(V_{FB}\) (which is the gate voltage at which the energy bands in the semiconductor substrate remain horizontal with respect to the semiconductor–dielectric interface and at which the surface potential of the semiconductor substrate is zero), is one of the most critical parameters of a metal–oxide–semiconductor (MOS) structure. The importance of this parameter is attributable to the fact that it is a critical feature of the threshold voltage, \(V_T\), of the MOS transistor and its diverse uses for other characteristics of MOS structures \([20]\). The shift of the flat-band voltage in the positive direction in the C–V curve is a prominent problem of \(\text{Al}_2\text{O}_3\) films. The positive shift is due to negative charge traps in the oxide layer induced by Al diffusion from the \(\text{Al}_2\text{O}_3\) layer to the Si substrate \([21,22]\). When the annealing temperature increases, the diffusion rate increases. In addition, because neither optical nor electrical impulses are applied, free charges must be created by the trapping or detrapping defects inside the dielectric; the energy required to trigger this mechanism can only be provided by temperature (i.e., phonons). The bulky shift of the flat-band voltage upsurges the Coulomb scattering between carriers and trap charges. This causes the catastrophic reduction of the conductance of the carrier. Researchers have stated that the variations in the chemical states and atomic structures of films are strongly linked to these phenomena \([21–24]\). Because \(\text{Al}^{3+}\) diffuses into the Si substrate, the density of positive ions (holes) in the semiconductor increases, which attracts more negative charges (electrons). Thus, n-type Si, which usually functions as the donor, starts to function as the acceptor. Moreover, as the atomic radius of Al (143 pm) is larger than that of Si (118 pm) \([25]\), diffusion is accompanied by some scattering events in usual Si atomic structures. These phenomena may change the attributes of samples that have been annealed at high temperature and are subjected to constant voltage stress.

Constant voltage stress measurements are conducted to determine how a MOSCAP device reacts when a gate bias is applied for a specific duration; in these measurements, unusual properties such as strain instead of stress can occur after certain PDA conditions. In
this study, some other hallmarks of MOSCAP characterization, such as interface trap density (D_it) and border trap (N_bt), are extracted. To determine the D_it of dielectric/semiconductor (SiO_2/Si) interfaces of MOSCAP structures, researchers developed different approaches in the 1960s [26]. High interface trap densities are the reason for unproductive Fermi level response. In addition, they can cause Fermi level pinning, thereby preventing the successful control of charge carriers in the channel and the comprehension of MOSFETs with good subthreshold slopes and high drive currents, although Si possesses high-quality native oxides with good stability, low leakage, and high breakdown fields. To extract the D_it, the conductance method was used in this study, as recommended in [26].

Owing to the time constant difference between both forms of traps and the border trap density estimate from the C–V hysteresis, which exhibits full re-emission of captured charges during the reverse C–V sweep, the traditional interface trap model does not explain the existence of border trap phenomena. Their existence must be proved based on the dispersion of accumulated frequencies [13,27]. Many researchers have investigated border trap reduction caused by annealing; nevertheless, the annealing environment and its effects have not been studied thoroughly [28,29]. A robust method for border trap extraction is presented in [29–32]; the same strategy was used in this study.

2. Methods and Materials

The Al_2O_3 thin film was deposited with a thermal ALD system. The deposition temperature was 250 °C, and an n-type Si (100) substrate (Sehyoung Wafer Co. Ltd., Seoul, Korea) with 1–100 Ω cm resistivity and try-methyl aluminum (TMA) as the precursor for Al_2O_3 were used. The Chemical Abstracts Service number of TMA is 75-24-1; it has 99.99% purity according to UP Chemical Co., Ltd. (Pyeongtaek, Korea). H_2O was used as the oxidizing agent, and argon was the carrier and purge gas. The ALD system consisting of an allocation system with four sets of precursor canisters conducted the thermal ALD process (“Atomic Classic”, CN1, Hwaseong, Korea) at a maximal deposition temperature of 450 °C. The TMA precursor was kept at room temperature. The carrier and purge gas flow rates for Al_2O_3 deposition were 0.3 L/min. Moreover, the pulse time was 0.1 s, and the purge time was 20 s. The oxidant (H_2O) pulse and purge times were 0.1 s and 60 s, respectively. The Al_2O_3 layer was deposited with 100 cycles. Before deposition, the substrate was processed with a standard precleaning method with acetone, isopropyl alcohol, and deionized water. Subsequently, the substrate was dried in a N_2 environment for the prevention of watermark formation on the surface. Eight samples were prepared for oxide layer deposition. The deposition started with pre-argon purging, 100 cycles of Al_2O_3 deposition as the second step, and post-argon purging as the third step. The thicknesses of the ALD-deposited films were measured with ellipsometry at an incident angle of 70°. Because all eight samples had been simultaneously covered with Al_2O_3, their oxide thicknesses were approximately identical. The average calculated growth per cycle (GPC) was 1.14 Å. For the PDA process of the substrates, the Nextron TM rapid thermal processing system RTP-1200 and Atovac flow and pressure controller GMC1200 were used. The RTA time and temperature were as follows: 300 °C–2 min, 300 °C–5 min, 300 °C–10 min, 400 °C–2 min, 400 °C–5 min, 500 °C–2 min, and 500 °C–5 min; the resulting characteristics were compared with those of as-grown substrates that were not treated with PDA. Instead, they were preannealed at 100 °C for 1 min. To prepare MOSCAP devices, an approximately 150 nm thick Al metal layer was deposited with a thermal evaporator (Korean vacuum thermal evaporator system, KVT-438) on the dielectric to create front electrodes with different areas with a shadow mask: 200, 300, and 400 µm^2. The same metal layers were deposited without masks as back contacts. The electrical characterization (e.g., the C–V and constant voltage stress measurements) and interface and border trap extractions were performed with a probe station (MSTech 5500), semiconductor device analyzer (Keysight B1500A), waveform generator/fast measurement unit (Keysight B1530A), precision LCR meter (Agilent 4284A), and low-leakage switch mainframe (HP E5250AX-Ray diffraction (XRD) was measured by
an X-ray diffractometer (Rigaku Ultima 4) where, Cu Kα radiation (40 kV, λ = 1.54 Å) was used for measuring. Various conditions for preparing the MOSCAPs are shown in Table 1.

Table 1. Conditions of parameters used for MOSCAP fabrication.

| Sample       | Oxide    | ALD RTA Thermal Evaporator | Metal Layer |
|--------------|----------|---------------------------|-------------|
|              | Cycle    | Temperature | Gas | Temperature | Time (min) |                 |
| As-grown     | 100      | 250         | Ar  | -           | -         |                 |
| 300 °C–2 min | 100      | 250         | Ar  | 300 °C      | 2         | Al              |
| 300 °C–5 min | 100      | 250         | Ar  | 300 °C      | 5         |
| 300 °C–10 min| 100      | 250         | Ar  | 300 °C      | 10        |
| 400 °C–2 min | 100      | 250         | Ar  | 400 °C      | 2         |
| 400 °C–5 min | 100      | 250         | Ar  | 400 °C      | 5         |
| 500 °C–2 min | 100      | 250         | Ar  | 500 °C      | 2         |
| 500 °C–5 min | 100      | 250         | Ar  | 500 °C      | 5         |

3. Results and Discussion

Figure 1 demonstrates the C–V characteristics of the Al₂O₃ MOS capacitors (PDA) annealed at different temperatures for different times at 1 MHz. The colored curves represent the capacitance values of the MOSCAPs. The MOSCAP annealed at 300 °C for 5 min has the highest capacitance, and the 500 °C–5 min sample has the lowest. The as-grown and other samples have similar values except sample 400 °C–5 min; its capacitance value is lower than that of 300 °C–5 min and higher than those of the others. The C–V curves of the samples are fluctuating towards the right side as PDA time and temperature extend. The curves of the as-grown to 400 °C–5 min samples are close; however, those of the samples annealed at 500 °C shift abundantly. When a C–V curve is shifting towards the positive side, that means the threshold voltage, as well as the flat-band voltage (V_{FB}), is also increasing.

Figure 2a shows the V_{FB} value of each sample; it gradually increases with increasing PDA time and temperature. The V_{FB} values of the samples were calculated with the inflection point method using a second derivative of the C–V curve. The point of intersection of the second derivative of the C–V curve with the Vg-axis is zero, which is called the inflection point, as well as the value of flat-band voltage [33]. Most researchers have stated that V_{FB} shifts owing to ion diffusion at the annealing temperature [21–24]; this results in an additional aluminum silicate layer at the interface of the Si substrate and oxide layer, as presented by the X-ray diffraction (XRD) data in Figure 2b (each sample exhibits peaks at 82.5°) [34]. For the XRD measurements, the annealing time was set to 5 min, and the temperatures were 300, 400, and 500 °C. We measured 2θ from 30° to 90°, but significant difference in the peak analysis, in terms of annealing, was not found except in 2θ = 82.5°. From the literature [34–36], we found that this value of 2θ indicates the presence of aluminum silicate. That is why we narrowed down the whole XRD waveform into around 80 degree. The peak variations among the four samples indicate that the increasing temperature promotes diffusion in the interfacial layer. The peak of the sample annealed at 500 °C is much higher than those of the others; this confirms greater diffusion at 500 °C. In the n-Si samples, the shift of V_{FB} to the right means that Al³⁺ ions from the Al₂O₃ layer diffuse toward the Si substrate.
Figure 1. Capacitance–voltage curves comparison at 1 MHz.

Figure 2. (a) Flat-band voltage comparison by inflection point method; (b) XRD peak value indicating aluminum silicate presence.

Figure 3a compares the dielectric constants of the samples. The 300 °C–5 min sample has the highest dielectric constant because the constant depends on the capacitance value. The dielectric constant is calculated as follows [26]:

$$\varepsilon_{high-k} = \frac{C_{max} \times T_{ox}}{\varepsilon_0}$$

Figure 3b presents the hysteresis results. Accordingly, the 300 °C–5 min sample has the lowest hysteresis. In general, the Al$_2$O$_3$ hysteresis is inversely proportional to the PDA time and temperature. However, above certain temperature and time thresholds, the hysteresis increases; this increase is still lower than that of the as-grown sample (which has no PDA-annealed MOSCAP). The highest capacitance and hysteresis were measured in several devices in each of the MOSCAPs to be sure about the trend. All test and average calculation results and the calculated standard deviation of the seven samples are listed in Tables 2 and 3. The standard deviation indicates how disperse the data are in relation to the average value. For example, in Table 2, the standard deviation values indicate that the 300 °C–5 min sample has the lowest scattering in terms of hysteresis.
(a) (b) Figure 3. (a) Average dielectric constants; (b) comparison of average hysteresis.

Table 2. Highest capacitance values of tested devices.

|            | As-Grown | 300 °C–2 min | 300 °C–5 min | 300 °C–10 min | 400 °C–2 min | 400 °C–5 min | 500 °C–2 min | 500 °C–5 min |
|------------|----------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Test 1     | 0.46     | 0.47         | 0.54         | 0.43         | 0.42         | 0.47         | 0.45         | 0.48         |
| Test 2     | 0.38     | 0.52         | 0.53         | 0.45         | 0.45         | 0.47         | 0.53         | 0.52         |
| Test 3     | 0.375    | 0.34         | 0.53         | 0.43         | 0.42         | 0.51         | 0.50         | 0.43         |
| Test 4     | 0.48     | 0.46         | 0.53         | 0.38         | 0.51         | 0.50         | 0.43         | 0.29         |
| Test 5     | 0.475    | 0.4          | 0.53         | 0.46         | 0.43         | 0.46         | 0.54         | 0.52         |
| Test 6     | 0.375    | 0.35         | 0.56         | 0.4          | 0.4          | 0.44         | 0.48         | 0.27         |
| Test 7     | 0.45     | 0.45         | 0.475        | 0.48         | 0.5          | 0.52         | 0.475        | 0.425        |
| Avg        | 0.43     | 0.43         | 0.53         | 0.43         | 0.45         | 0.48         | 0.49         | 0.42         |
| STD        | 0.05     | 0.07         | 0.03         | 0.03         | 0.04         | 0.03         | 0.04         | 0.1          |

Table 3. Hysteresis data of tested devices.

|            | As-Grown | 300 °C–2 min | 300 °C–5 min | 300 °C–10 min | 400 °C–2 min | 400 °C–5 min | 500 °C–2 min | 500 °C–5 min |
|------------|----------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Test 1     | 30.0     | 13.6         | 10.9         | 17.6         | 42.0         | 33.4         | 9.0          | 13.2         |
| Test 2     | 55.5     | 31.3         | 2.2          | 40.7         | 56.6         | 38.2         | 14.6         | 22.2         |
| Test 3     | 55.6     | 36.8         | 8.2          | 34.1         | 32.1         | 36.5         | 26.5         | 76.2         |
| Test 4     | 53.7     | 6.1          | 2.4          | 54.3         | 28.1         | 28.7         | 2.5          | 9.4          |
| Test 5     | 52.6     | 62.9         | 1.9          | 65.0         | 23.5         | 27.0         | 33.7         | 15.7         |
| Test 6     | 51.1     | 36.8         | 0.4          | 33.5         | 49.0         | 44.5         | 3.9          | 10.4         |
| Test 7     | 34.3     | 70.7         | 10.4         | 27.2         | 34.0         | 22.3         | 24.1         | 61.8         |
| Avg        | 47.5     | 36.9         | 5.2          | 38.6         | 37.9         | 35.8         | 16.3         | 29.8         |
| STD        | 10.7     | 23.6         | 4.5          | 16.1         | 11.8         | 12.2         | 12.0         | 27.4         |

Figure 4a exemplifies the interface trap density ($D_{it}$) of the samples and as-grown sample under different treatment conditions; the trap density was calculated with the conductance method by considering the series resistance correction with the following equation:

$$D_{it} = \frac{2.5}{Aq} \times \left( \frac{G_p}{\omega} \right)_{\max}$$

(2)

where A is the area of the measured device, q the electron charge, $G_p$ the parallel conductance, and $\omega$ the angular frequency. [26] The $D_{it}$ values of the as-grown, 300 °C–2 min, 300 °C–5 min, 300 °C–10 min, 400 °C–2 min, 400 °C–5 min, 500 °C–2 min, and 500 °C–5 min samples are $5.8 \times 10^{11}$, $5.6 \times 10^{11}$, $4.94 \times 10^{11}$, $1.32 \times 10^{11}$, $5.06 \times 10^{11}$, $5.1 \times 10^{11}$,
3.7 × 10^{11}, and 2.67 × 10^{11} \text{ cm}^{-2} \text{ eV}^{-1} because all the samples had identical interfaces and Al_{2}O_{3} layer thicknesses and the same pretreatment. The \( D_{it} \) pattern exhibits two characteristics. First, the increasing annealing time decreases \( D_{it} \) (the 5 min time frame presents greater reduction in the density of interface traps than the 2 min case). Second, the interface trap density decreases more at 500 °C than at 300 °C, although there is a little discrepancy in the 400 °C cases. Thus, a high annealing temperature and long annealing time effectively reduce \( D_{it} \).

Figure 4. (a) Interface trap comparison and (b) border trap comparison for all samples.

Figure 4b presents the extracted border trap densities, \( N_{bt} \), of the MOSCAPs. They were determined with the distributed border trap model proposed by Yuan et al. by constructing the best fit between the measured capacitance at the precise voltage in the accumulation region and the capacitance calculated from the model [37]. The overall oxide thickness is segmented into a limited number of quantities in this model. Each quantity reflects a certain oxide capacitance that is proportional to the border trap extent and arranged in series with the semiconductor capacitance in a parallel admittance model. In [30,31], the \( N_{bt} \) model and extraction method were thoroughly described. In the extraction process, the effective electron mass of the Al_{2}O_{3} film was considered to be 0.23 \( m_0 \), where \( m_0 \) represents the electron rest mass [27,38]; the trap capture/emission time constant \( \tau_0 \) was a fitting parameter. In addition, a one-dimensional Poisson–Schrodinger solver simulation tool (nextnano) was used to calculate the semiconductor capacitance \( C_s \) at the border trap extraction voltage [39]. Here, almost the same pattern was observed as interface trap density (\( D_{it} \)) in the extracted densities of the border trap. Many of these special oxide traps disappear at high annealing temperature and with longer annealing time, which is supposed to more stoichiometrically change at these conditions. According to Figure 4b, the 300 °C–10 min MOSCAP has the lowest amount of border traps.

Figure 5 shows the \( V_T \) shifts in the constant voltage stress measurement. The CVS was measured at 1.5 and 2.0 V stress biases for 0, 10, 30, 60, 200, 300, 400, 1000, and 2000 s. The \( V_T \) shift indicates how much degradation occurred due to stress in the sample. Figure 5a,b indicates that the 300 °C–5 min annealed sample has the lowest dispersion after stress for both stress bias voltages, while the as-grown sample has the highest dispersion, and other MOSCAPs are in the intermediate range. Evidently, the post-deposition heat treatment improves the film quality. However, at a relatively high temperature, the scenario has dramatically changed. According to the insets in Figure 5a, b, in the results of the samples 500 °C–2 min and 500 °C–5 min, the \( V_T \) shifts left after the stress treatments. This is probably due to excessive ion diffusion from the oxide layer to the n-Si substrate. Because positive Al^{3+} ions diffuse to the Si layer, the electron concentration of the n-doped Si layer may be changed [22]. The increase in positive ions (holes) reduces the number of negative ions (electrons). Consequently, the n-Si layer, which functions as the donor, attracts more
electrons and, therefore, functions as the acceptor. Constant voltage stress experiments on MOSCAPs have not been performed; according to the results, this is the most convenient and realistic explanation for this behavior. Therefore, there is a possibility of some changes in the lifetime of the MOS capacitors in terms of annealing [40]. The relation between lifetime and annealing conditions will be further discussed in an extension of this work.

Figure 5. Threshold voltage shift after application of constant voltage stress for 2000s: (a) 1.5 V stress bias; (b) 2.0 V stress bias. Inset: 500 °C samples after stress application.

Figure 6 presents the leakage current densities and breakdown voltage characteristic transformation in various PDA conditions after applying a positive bias voltage from 0 to 15 V. The sample 300 °C–5 min exhibits the lowest leakage current and highest breakdown voltage among all the samples; with increasing PDA time and temperature, the MOSCAP breaks down at a lower voltage. As a result, the sample 500 °C–5 min has the lowest breakdown voltage and highest leakage current. This behavior can be described with ion diffusion theory. Because the surface morphology has changed with increasing temperature, the interface between the oxide and semiconductor becomes leakier and cannot absorb the high bias voltage.

Figure 6. Breakdown voltage and leakage current of MOSCAPs.

4. Conclusions

In this study, the characteristics of Al₂O₃ PDA annealed under different conditions on the Si substrate were investigated. The Al₂O₃ layers were deposited with H₂O as an oxidant and ALD. The capacitance, hysteresis, dielectric constant, constant voltage stress, leakage current, breakdown voltage, interface trap, and border trap characteristics of annealed and nonannealed samples were compared. In addition, their surface morphologies were
studied with XRD. The results clearly indicate that the annealed samples show better characteristics than the nonannealed samples. Moreover, the diffusion properties of the silicon and oxide layers were discussed. This article divulges an unopened scenario and also presents the optimal conditions for post-deposition annealing of Al/Al2O3/n-Si stacks.

**Author Contributions:** A.B. prepared the samples, conducted the characterizations, wrote the manuscript, and prepared the figures. T.-W.K. provided the main idea, initiated the work, and supervised the entire process. Both authors analyzed and discussed the results. All authors have read and agreed to the published version of the manuscript.

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**References**

1. del Alamo, J.A. Nanometre-scale electronics with III–V compound semiconductors. *Nature* 2011, 479, 317. [CrossRef] [PubMed]

2. Heyns, M.; Alian, A.; Brammertz, G.; Caymax, M.; Chang, Y.C.; Chu, L.K.; De Jaeger, B.; Eneman, G.; Gencarelli, F.; Groeseneken, G.; et al. Advancing CMOS beyond the Si roadmap with Ge and III/V devices. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011; Volume 3, pp. 13.1.1–13.1.4.

3. Kamata, Y. High-k/Ge MOSFETs for future nanoelectronics. *Mater. Today* 2008, 11, 30–38. [CrossRef]

4. Ye, P.D. Main determinants for III–V metal-oxide-semiconductor field-effect transistors (invited). *J. Vac. Sci. Technol. A* 2008, 26, 697–704. [CrossRef]

5. Robertson, J.; Falabretti, B. Band offsets of high K gate oxides on high mobility semiconductors. *Mater. Sci. Eng. B* 2006, 135, 267–271. [CrossRef]

6. Xuan, Y.; Wu, Y.Q.; Shen, T.; Yang, T.; Ye, P.D. High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al2O3, HfO2 and HfAlO as gate dielectrics. In Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 10–12 December 2007; pp. 637–640.

7. Lin, J.Q.; Lee, S.J.; Oh, H.J.; Lo, G.Q.; Kwong, D.L.; Chi, D.Z. Inversion-mode self-aligned In0.53Ga0.47 As metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate. *IEEE Electron. Device Lett.* 2008, 29, 977–980. [CrossRef]

8. Goel, N.; Heh, D.; Koveshnikov, S.; Ok, I.; Oktaybrsky, S.; Tokranov, V.; Kambhampati, R.; Yakimov, M.; Sun, Y.; Pianetta, P.; et al. Addressing The Gate Stack Challenge For High Mobility InxGa1-xAs Channels For NFETs. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 1–4.

9. Zadeh, D.H.; Oomine, H.; Suzuki, Y.; Kakushima, K.; Ahmet, P.; Nohira, H.; Kataoka, Y.; Nishiyama, A.; Sugii, N.; Tsutsui, K.; et al. La2O3/In0.53Ga0.47 As metal-oxide-semiconductor capacitor with low interface state density using TiN/W gate electrode. *Solid-State Electron.* 2013, 82, 29–33. [CrossRef]

10. Chobpattana, V.; Mates, T.E.; Zhang, J.Y.; Stemmer, S. Scaled ZrO2 dielectrics for In0.53Ga0.47 As gate stacks with low interface trap densities. *Appl. Phys. Lett.* 2014, 104, 182912. [CrossRef]

11. Albertin, K.F.; Valle, M.A.; Pereyra, I. Study of TiO2 and SiO2/TiO2 as Gate Dielectric Materials. *ECS Trans.* 2007, 4, 409–416. [CrossRef]

12. Koo, J.; Lee, J.; Kim, S.; Do Kim, Y.; Jeon, H.; Kim, D.S.; Kim, Y. Characteristics of hafnium-aluminum-oxide thin films deposited by using atomic layer deposition with various aluminum compositions. *J. Korean Phys. Soc.* 2005, 47, 501–507.

13. Rahman, M.M.; Kim, J.-G.; Kim, D.-H.; Kim, T.-W. Characterization of Al Incorporation into HfO2 Dielectric by Atomic Layer Deposition. *Micromachines* 2019, 10, 361. [CrossRef]

14. Wilk, G.D.; Muller, D.A. Correlation of annealing effects on local electronic structure and macroscopic electrical properties for HfO2 deposited by atomic layer deposition. *Appl. Phys. Lett.* 2003, 83, 3984–3986. [CrossRef]

15. Yun, M.; Kim, M.S.; Ko, Y.D.; Moon, T.H.; Hong, J.H.; Myoung, J.M.; Yun, I. Effects of post-metallization annealing of high-K dielectric thin films grown by MOMBE. *Microelectron. Eng.* 2005, 77, 48–54. [CrossRef]

16. Hashizume, T.; Kaneki, S.; Oyobiki, T.; Ando, Y.; Sasaki, S. Effects of postmetallization annealing on interface properties of Al2O3/GaN structures. *Appl. Phys. Express* 2018, 11, 124102. [CrossRef]

17. Thesis, M.; Kuriyama, A.; Ohmi, S.I.; Tsutsui, K.; Iwai, H. Effect of Post Metallization Annealing for La2O3 Gate Thin Film. *Jpn. J. Appl. Phys.* 2005, 44, 1045–1051.
