Neat: Low-Complexity, Efficient On-Chip Cache Coherence

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Abstract—Cache coherence protocols such as MESI that use writer-initiated invalidation have high complexity—and sometimes have poor performance and energy usage, especially under false sharing. Such protocols require numerous transient states, a shared directory, and support for core-to-core communication, while also suffering under false sharing. An alternative to MESI’s writer-initiated invalidation is self-invalidation, which achieves lower complexity than MESI but adds high performance costs or relies on programmer annotations or specific data access patterns.

This paper presents Neat, a low-complexity, efficient cache coherence protocol. Neat uses self-invalidation, thus avoiding MESI’s transient states, directory, and core-to-core communication requirements. Neat uses novel mechanisms that effectively avoid many unnecessary self-invalidations. An evaluation shows that Neat is simple and has lower verification complexity than the MESI protocol. Neat not only outperforms state-of-the-art self-invalidation protocols, but its performance and energy consumption are comparable to MESI’s, and it outperforms MESI under false sharing.

I. INTRODUCTION

Today’s general-purpose processors have multiple cores with private and shared caches. To provide the abstraction of shared memory in this context, processors implement cache coherence, which is defined by two invariants—the single writer, multiple readers (SWMR) invariant and the data-value invariant [56]. The SWMR invariant requires that at any given time, a memory location can only be written by a single core or read by multiple cores. The data-value invariant requires that a read must see the up-to-date value of the corresponding memory location it reads. Most multicore processors use a variant of the MESI cache coherence protocol [36], [23]. MESI enforces the two invariants using writer-initiated invalidation and ownership tracking: whenever a core writes to a cache line, the protocol invalidates shared copies of the line, by tracking where in the system a valid copy or copies of a line reside; the protocol also records the ID of the writer (i.e., owner ID) so that subsequent reads can be directed to the writer to get up-to-date values of the line. As a result, MESI and its variants are efficient because they perform coherence actions only when accesses to a line by multiple cores conflict.

While often efficient, MESI has some serious drawbacks. Protocol races—which occur even in executions of data-race-free programs—necessitate transient states that complicate implementation and verification. Optimized MESI implementations rely on a shared directory that maintains the coherence state and the owner ID of each line, typically containing an entry for every line in the shared cache. MESI messages between cores’ private caches and the shared cache require acknowledgments to ensure the SWMR and the data-value invariants, e.g., for writer-initiated invalidations and dirty writebacks, incurring latency. MESI maintains coherence states at the granularity of cache lines and is consequently susceptible to false sharing [21].

Researchers have introduced new cache coherence designs that aim to be simpler than MESI [19], [30], [13], [38], [37], [55]. A key aspect of these designs is that they exploit the data-race-free (DRF) assumption of language-level memory consistency models [11]. These simpler coherence protocols exploit DRF to leverage the semantics of synchronization to enforce coherence. As a result, they do not require cores to exchange eager invalidations that directly implement the SWMR invariant. Using these techniques, a core instead self-invalidates its valid lines at a synchronization acquire operation. Further, by exploiting DRF, the coherence protocols do not require cores to write back dirty data or register the owner ID in the shared cache immediately upon each individual write. A core can defer flushing dirty data or ownership registration to the shared cache until a synchronization release operation. Assuming a DRF program, such self-invalidations and deferred flushes are sufficient to ensure coherence.

Self-invalidation has potential advantages over MESI: lower protocol complexity (by avoiding MESI’s numerous transient states), lower power (mainly by eliminating MESI’s coherence directory states), and lower per-operation latency (by eliminating protocol acknowledgments, as well as cache invalidations due to false sharing). At the same time, self-invalidation can degrade performance by invalidating up-to-date lines, causing unnecessary cache misses. Some self-invalidation protocols...
try to improve performance by relying on mechanisms to infer data access patterns or on programmers to write in new languages or use annotations about which cache lines need to be invalidated [30], [13], [38], [35]. To implement the data-value invariant, some self-invalidation-based approaches retain some of MESI’s directory and protocol complexity [19]; or defer ownership registrations and dirty write-throughs by buffering them, which incur performance and energy cost when the buffers overflow [30], [13], [38], [35]. Section II details closely related prior approaches.

Table I’s first two rows compare MESI and self-invalidation protocols. The table highlights the performance–complexity tradeoff between MESI and self-invalidation, and self-invalidation’s performance advantage under false sharing.

This paper’s goal is to get the advantages of performing self-invalidations and deferred flushes without most of the disadvantages and issues—achieving (1) significantly lower complexity than MESI, (2) performance and energy usage on par with MESI and significantly better than prior designs that use self-invalidations and deferred flushes, and (3) out-of-the-box support for legacy programs. To achieve this goal, we introduce a novel, low-complexity approach to multicore cache coherence called Neat. Neat consists of two main design elements that contribute to its efficacy, one for each type of coherence action at synchronization operations. First, Neat uses novel lightweight mechanisms to reduce self-invalidation costs significantly by improving reuse of both dirty and clean data across synchronization acquires, which differs from prior work that relies on programmer annotations or inferred sharing patterns [30], [13]). Second, in Neat, writes to privately cached lines are not propagated until synchronization releases, which differs from prior work that either uses MESI-style mechanisms to maintain ownership and propagate data at individual memory accesses [19] or uses buffers to defer flushes (i.e., write-throughs or ownership registration requests) until overflowing buffers or reaching synchronization releases [30], [13], [38].

We perform two evaluations of Neat compared with state-of-the-art approaches. First, we evaluate Neat’s complexity by implementing and verifying Neat and MESI in the Murphi model checking tool [15]. Our evaluation shows that Neat is about an order of magnitude less complex to verify than the MESI protocol. Second, we implement a trace-based simulation of Neat, compared with MESI and two self-invalidation-based coherence protocols called SARC and VIPS [19], [39], and evaluate on the PARSEC benchmarks [6], three real server programs, and the Phoenix benchmarks [29]. Our evaluation shows that Neat has competitive performance and energy usage with MESI, and outperforms MESI significantly under false sharing. Neat also typically outperforms SARC and VIPS. Neat reduces static power compared with MESI and SARC by eliminating the coherence directory. Neat outperforms VIPS because Neat’s mechanisms are more effective in avoiding unnecessary self-invalidation than VIPS’s; VIPS’s optimizations are applicable to Neat, improving Neat’s performance further. These comparative results—summarized qualitatively in Table II—suggest that Neat is a compelling alternative to MESI and state-of-the-art self-invalidation approaches in terms of complexity, performance, and energy.

II. BACKGROUND: SELF-INVALIDATION-BASED COHERENCE PROTOCOLS

This section overviews state-of-the-art cache coherence protocols that self-invalidate readers’ copies at acquire operations [19], [30], [13], [38], [35], [17]. These protocols differ from each other mainly in their strategies for committing dirty lines to implement the data-value invariant:

- SARC retains MESI’s directory to keep track of cache lines’ ownership, and a new writer initiates the write-back and invalidation of the old writer’s copy [19] (Section II-A).
- GPU coherence uses write-through caching for all data [35], [17], while VIPS classifies private and shared data and uses write-back caching for private data and write-through caching for shared data [30] (Section II-B).
- DeNovo and other DeNovo-based protocols rely on registering the ownership of dirty data in the LLC, rather than writing back dirty data directly [13], [38], [35], [17] (Section II-C).

A. Using MESI-Style Write-Backs

SARC’s design retains part of MESI’s directory to track ownership of dirty lines [19]. A writer initiates the write-back and invalidation of the last writer’s line. SARC extends MESI by supporting tear-off copies of lines for reads, avoiding the need to maintain read-sharers in the directory. A core’s private cache self-invalidates a tear-off copy of a line at an acquire. Neat also avoids tracking sharers in the directory and uses self-invalidation to ensure coherence. Unlike SARC, Neat eliminates the directory and MESI protocol entirely, and writes back all dirty bytes at releases to provide coherence.

1Self-invalidation and deferred write-backs originated as release consistency mechanisms for distributed shared memory systems [20], [2].
B. Using Delayed Write-Throughs

While CPUs use the complex MESI protocol or its variants, GPUs prefer a simpler coherence protocol that the literature refers to as GPU coherence \[35\], \[17\]. GPU coherence uses self-invalidation at acquires and private write-through caches to keep the shared cache up to date. To reduce the costs of write-through caching, the write-throughs can be buffered and delayed until the next release or buffer overflow. This paper’s baseline Neat design resembles GPU coherence in spirit, but the following important differences exist between the two designs:

- **Neat defers write-backs for all dirty data**, while GPU coherence uses buffers to hold outstanding write-throughs, which is subject to the capacity limits of the buffers.
- **Neat introduces lightweight mechanisms that reduce unnecessary self-invalidation costs**.

The above differences help Neat achieve significantly better performance and energy efficiency than prior work.

Similar to GPU coherence, VIPS uses self-invalidation at acquires and delays write-throughs until a timeout, a miss status handling register (MSHR) eviction, or a release operation \[30\]. Neat avoids write-through costs imposed by VIPS by deferring all write-backs until releases.

To reduce performance costs due to unnecessary self-invalidations, VIPS optimizes self-invalidation by classifying pages as private or shared. For all shared pages, VIPS further distinguishes between read-only and read-write pages, and self-invalidates only shared read-write pages. While often beneficial, VIPS’s classifications are sensitive to a program’s data access patterns and have limited impact on programs that mainly access data on shared read-write pages. In contrast, our Neat design introduces lightweight mechanisms to avoid unnecessary self-invalidations without relying on specific data access patterns.

C. Using Ownership Registration

DeNovo and DeNovo-based protocols rely on registering the ownership of dirty data \[13\], \[38\], \[35\], \[3\], while Neat writes back dirty lines in bulk at releases.

**DeNovo** uses self-invalidation for out-of-date reads and registration in the LLC to track a line’s writers \[13\]. Registration requires inclusion at the LLC and an extra level of indirection for writing back the data, hurting LLC capacity and introducing latency. DeNovo further requires the program to be written in a deterministic, data-race-free language \[10\]. **DeNovoND** extends DeNovo to allow parts of a program to be nondeterministic \[38\], but relies on the compiler to identify atomic accesses to maintain coherence. DeNovo and DeNovoND are thus not applicable to programs written in standard languages.

While much of the DeNovo line of work relies on programmer annotations (or has other major differences from Neat, e.g., DeNovoSync \[37\], see Section \[VI\]), DeNovo and its ideas have been applied to GPUs without requiring programmer annotations \[35\]. This protocol uses registrations on dirty data; the registrations can be buffered and committed upon buffer overflow or at releases. The protocol uses self-validations on all non-registered data at acquires to improve reuse of dirty data.

In contrast to the above DeNovo line of work, a Neat core writes back all dirty data to the LLC in bulk at releases, avoiding shared ownership metadata entirely. Neat uses lightweight mechanisms to improve reuse of both dirty and clean data without requiring programmer annotations.

**Heterogenous lazy release consistency (hLRC)** builds on DeNovo, but exploits synchronization locality by registering only synchronization variables and lazily performing coherence actions only when a remote synchronization operation is detected \[3\]. Neat does not detect synchronization locality since it targets CPU coherence where synchronization is mostly global, but it would be straightforward to extend Neat to exploit synchronization locality by avoiding coherence actions at detected local synchronization operations.

In summary, researchers have explored various self-invalidation approaches to provide simple, efficient cache coherence that avoids the complex directory and transient states of MESI \[30\], \[13\], \[38\], \[35\], \[3\]. Existing solutions for avoiding unnecessary self-invalidations either depend on program data access patterns or require programmer annotations. Further, in order to implement the data-value invariant, these approaches either retain part of the directory to maintain shared ownership metadata, or incur write-through costs.

III. THE NEAT COHERENCE PROTOCOL

This section first overviews Neat’s design. It then presents a baseline version of Neat, which self-invalidates all private cache lines at acquires, and commits all dirty data at releases. Finally, we present the full version of Neat that improves data reuse across synchronization operations, improving performance and energy with acceptable additional complexity.

A. Neat Overview

Neat is a set of modifications to a multicore processor that lacks support for cache coherence and core-to-core communication. A core’s cache associates with each cache line a valid bit that is either valid (V) or invalid (I). Without loss of generality, this section assumes that each core has a single-level private cache and that all cores share a last-level cache (LLC). It is straightforward to extend Neat’s support to multiple private cache levels (L1 and L2 caches), as in our performance and energy evaluation (Section \[V\]). Unlike common implementations of MESI or prior work that tracks ownership in the LLC \[36\], \[19\], \[13\], \[38\], \[35\], \[3\], Neat does not require that the LLC be inclusive of the L1 caches. Neat does not require that the processor’s interconnect supports core-to-core messages as implementations of MESI or prior work such as SARC and DeNovo do \[36\], \[19\], \[13\], \[38\], \[35\], \[3\].

Neat does not explicitly maintain the SWMR invariant maintained by MESI and other protocols that use writer-initiated invalidation. Instead, in Neat a core may read from out-of-date copies of lines, and it may write to a line without immediately updating or invalidating other cores’ valid copies.
of the line. Neat consequently provides coherence only for data-race-free (DRF) programs, exploiting the DRF assumption that languages such as C++ provide. Our work assumes that the compiler distinguishes synchronization operations from regular memory operations in the compiled code so that Neat operates with respect to synchronization from the original program source.

Neat maintains the data-value invariant and ensures that, for DRF programs, each read sees the value written by the last ordered (well-synchronized) write to the memory location. To provide this guarantee, private caches self-invalidate valid lines and commit dirty data at acquires and releases, respectively. Unlike prior work that buffers and delays write-throughs or registrations of dirty data until the buffer is full or a release is reached, Neat does not rely on buffers and instead holds all dirty data in private caches until committing them at the next release. A core’s private cache keeps track of whether each byte is dirty, using one write bit per byte. This feature is necessary for correctness: non-dirty bytes may be out of date and should not in general be written back to the LLC. This feature also optimizes write-backs by writing back only a line’s dirty bytes. Note that multiple (write) bits per cache line have been explored in prior work on precise conflict detection and sector caches.

A core normally executes in a normal execution (NE) state. When a core performs an acquire operation, it transitions to the self-invalidation (SI) state, during which a core invalidates all of the valid lines in its private cache. If any valid line is dirty, then the private cache writes back its dirty bytes. Similarly, when a core performs a release, it enters the commit (CM) state, during which a core writes back all dirty bytes in its dirty lines to the LLC.

Figure 1 shows the MESI and Neat architectures that are both implemented on the base multicore processor, where MESI- and Neat-specific components are shaded grey. Note that Figure 1(b) includes support for mechanisms that avoid unnecessary self-invalidations and improve data reuse across synchronization operations—write signatures and PI state—introduced and explained in Section III-C. Compared with MESI, Neat eliminates the complex coherence directory and support for core-to-core communication, and introduces relatively small structures (write signatures) in the shared LLC and extra metadata for private cache lines.

B. Baseline Neat Protocol

Figure 2 shows baseline Neat, which provides correct coherence for DRF programs and efficiently defers coalesced write-backs until synchronization operations. Note that the basic protocol is inefficient because private caches invalidate all lines at acquires. The table includes separate states and transitions for (a) private cache lines, (b) a core’s private cache as a whole, and (c) the LLC as a whole. Note that Neat avoids the need for complex transient protocol states required by MESI, and Neat adds no per-line state to the LLC (e.g., no directory; Figure 1).

As in prior work (e.g., [13]), we assume each L1 controller has a request buffer, the storage array for which could be implemented as an explicit hardware buffer or using existing miss status handling registers (MSHRs). The request buffer tracks outstanding requests to the LLC. The L1 controller adds a request buffer entry while waiting for a response from the LLC, which is either a data request or a write-back message due to eviction of a dirty line, and it removes the entry from the request buffer after receiving a response. In Neat, accesses to invalid (I) and valid (V) states in private caches are straightforward, handled as misses and hits, respectively, except that a write set corresponds to write bits. When a private cache evicts a clean line (i.e., a valid line without any write bits set), it does so silently (i.e., without communicating with the LLC). When a private cache evicts a dirty line (i.e., a valid line with at least one write bit set), the private cache sends a write-back message to the LLC that includes the dirty bytes and corresponding write bits, and a count value CNT=1 (detailed below), which directs the LLC to send back an acknowledgment message PutAck immediately after receiving this one write-back message. The private cache changes the line state to I immediately, and the core may continue execution in general (as long as there is no dependency with the pending requests in the request buffer), but the core must wait for acknowledgments of all outstanding write-backs before executing operations after the next release. An access miss or write-back message does not
lead to transient states for cache lines because there are no conflicting access requests forwarded from other cores. Neat does not risk deadlock either because the LLC responds to an access miss or write-back directly without relying on any responses from other cores.

A core transitions to a commit (CM) state at a release and to a self-invalidation (SI) state at an acquire. While in the CM or SI state, a core does not fetch or execute instructions, and instead waits for the L1 controller to perform operations iteratively over all dirty lines (if in CM state) or valid lines (if in SI state).

During the CM state, the L1 controller writes back all its dirty lines and avoids per-line acknowledgment of each write-back by having the LLC send a single PutAllAck message once it has received all write-backs. To facilitate the LLC acknowledging such bulk write-backs, each write-back message has an integer field $CNT$ that indicates the number of write-backs that the LLC should receive before sending back an acknowledgment. The L1 controller counts the number of write-backs when committing dirty lines; after sending all

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| Read | Write | Replacement | Self-invalidation | Commit | Data |
|------|-------|-------------|------------------|--------|------|
| I    | read miss to LLC/-; | write miss to LLC/-; | N/A | N/A | N/A | if write: set corresp. Wbs/V; if read: -/V |
|      | write miss to LLC/-; | | | | | |
| V    | -/- | set corresp. Wbs/-; if dirty: write-back ($CNT = 1$) to LLC and clear all Wbs/I; if clean: -/I | if dirty: write-back ($CNT = 0$) to LLC and clear all Wbs/I; if clean: -/I | if dirty: write-back ($CNT = 0$) to LLC and clear all Wbs/-; if clean: -/I | N/A |
| PI   | if read clean bytes: read miss to LLC/-; if read dirty bytes: -/- | if dirty: write-back ($CNT = 1$) to LLC and clear all Wbs/I; if clean: -/I | -/- | -/- | merge data at clean bytes/V |

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| NE | in addition to per-line actions and state transitions specified above, a) at a synchronization release: -/CM; b) at a synchronization acquire: -/SI |
| SI | perform Self-inv on each valid line, send a data-less write-back message with $CNT = \text{total number of write-backs}$, and wait for PutAllAck and all PutAcks/NE |
| CM | perform Commit on each dirty line, send a data-less write-back message with $CNT = \text{total number of write-backs}$, and wait for PutAllAck/NE |

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(a) L1 controller's per-line state transitions.

(b) L1 controller's core-wide state transitions.

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| GetLine | Write-back (data+Wbs+CNT) from core |
|---------|-----------------------------------|
| send Data to Req | update line data corresponding to Wbs and if $CNT = 0$: wbReceived++; if $CNT = 1$: send PutAck to Req; if $CNT > 1$: send PutAllAck to Req and reset wbReceived to 0 when wbReceived = CNT |

(c) LLC controller's state transitions. Req = the requesting core. The LLC receives GetLine for each access miss and data+Wbs+CNT for each write-back from an L1. wbReceived is a per-core counter at the LLC side that counts the write-backs by the LLC during a core's self-invalidation or commit.

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(a) L1 controller's per-line state transitions.

(b) L1 controller's core-wide state transitions.

(c) LLC controller's state transitions. Req = the requesting core.

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During the CM state, the L1 controller writes back all its dirty lines and avoids per-line acknowledgment of each write-back by having the LLC send a single PutAllAck message once it has received all write-backs. To facilitate the LLC acknowledging such bulk write-backs, each write-back message has an integer field $CNT$ that indicates the number of write-backs that the LLC should receive before sending back an acknowledgment. The L1 controller counts the number of write-backs when committing dirty lines; after sending all

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Fig. 2. Baseline Neat protocol. In each table, (non-bolded) entries show actions and state transitions, indicated by *action/newState* with ‘-’ indicating no action or changed state, in response to messages from other components (shown in **bold** column headers). The L1 controller’s per-line and core-wide transitions take different actions and transitions depending on the current state (shown in bold row headers). Note that the protocol is described for a two-level cache hierarchy: core-private L1 cache and shared LLC. Wbs = write bits.

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Fig. 3. Full Neat protocol, with differences from Figure 2 highlighted in green. Write sig. = write signature.
write-backs, the L1 sends an extra write-back message to the LLC with CNT set to the number of write-backs and no data. The LLC knows to wait before acknowledging write-backs because the L1 controller sets CNT to 0 for write-backs sent during the CM state. The LLC maintains per-core counters \( \text{wbReceived} \) that count the write-backs received from each core with CNT=0. After receiving the extra write-back with a CNT greater than 0, the LLC compares the CNT and \( \text{wbReceived} \) of the same core; if the two are equal, it sends back a PutAllAck message to acknowledge all of the core’s write-backs and clears the \( \text{wbReceived} \) counter. We support the more general case of an out-of-order network between cores and the LLC, so a core’s bulk write-backs may be reordered with its extra write-back, allowing the LLC to receive a CNT greater than write-backs from the core so far. In such a case, the LLC keeps waiting for more write-backs to arrive from the core, incrementing \( \text{wbReceived} \) when appropriate. To ensure that a core’s dirty data are correctly written back and become visible at releases, a core in the CM state does not transition back to the NE state until it receives acknowledgments (PutAllAck and any PutAcks) for all outstanding write-backs.

We assume a centralized LLC for the above discussion, but it is straightforward to apply Neat’s bulk write-backs to a distributed LLC. With a distributed LLC, during the CM state, the L1 controller counts the number of write-backs it sends to each LLC bank and sends an extra write-back message to each bank with the corresponding count number. Each bank acknowledges receiving all the write-backs by sending back a PutAllAck message. A core in the CM state does not transition back to the NE state until it receives PutAllAcks from all LLC banks. To handle dropped packets on an unreliable network, if a core does not receive a response within a time limit, it should retry committing write-backs from the beginning.

During the SI state, the L1 controller invalidates all valid lines. It writes back dirty data for any dirty lines that it invalidates, in the same way as the CM state’s write-backs, avoiding per-line acknowledgment of each write-back. After invalidating all valid lines, the L1 controller transitions back to the NE state only after receiving a PutAllAck message. This behavior preserves that each core sees its own last write even in the context of an out-of-order network. Note that the L1 controller does not need to wait for outstanding PutAck responses (for write-backs due to dirty evictions) before transitioning from SI to NE because the corresponding write-backs occupy request buffer entries while waiting for acknowledgements.

### C. Full Neat Protocol

Conservative self-invalidation is expensive in terms of run-time performance and energy because it conservatively invalidates lines that may be out of date, which can hurt cache locality and result in avoidable cache misses. We introduce two mechanisms that significantly help reduce the costs of self-invalidation and improve data reuse across cores. Figure 3 shows the corresponding full version of the Neat protocol.

1) **Partially invalid state:** We observe that, at an acquire operation, a core can delay self-invalidating a line until its next read access to any clean byte in the line. In other words, a core can write to the line or read a byte that the core has already written, since these values will be up to date for a DRF execution. To make use of this observation, we introduce a partially invalid (PI) state for private cache lines to indicate that a line may have out-of-date data in its clean bytes. During self-invalidation, instead of invalidating each valid line (i.e., changing its state to I), the private cache partially invalidates each valid line, by changing its state to PI. Any subsequent write to a PI line is a hit, and a read to a dirty byte of a PI line is also a hit. But a read to clean byte(s) of a PI line is a miss; the private cache fetches updated value(s) of the byte(s) from the LLC, merges them into the private cache line (overwriting only clean bytes), and marks the line valid (i.e., PI \( \rightarrow \text{V} \)).

Note that with this mechanism, while an L1 controller is in the SI state (i.e., at an acquire) it does not clear any line’s write bits, regardless of whether the line is partially invalidated or left valid (a line may remain valid after self-invalidation only if using the write signature mechanism, described below). In contrast, during the CM state (i.e., at a release), the L1 controller clears a line’s write bits when writing back dirty bytes, and does not invalidate or partially invalidate any lines. In a DRF program, it is correct for a core to read from its own bytes at least until an acquire operation.

The PI state has some similarities to DeNovo’s touched bit [13], but there are some key differences. The touched bit indicates that a word is exclusively read by the current core and the core has up-to-date data for this word at the end of the current parallel phase. The PI state indicates the current core may have stale data for those bytes that were not written by the core. The touched bit is at word granularity while the PI state is at line granularity. Finally, DeNovo’s use of the touched bit relies on programmer annotations, while Neat’s use of the PI state does not rely on annotations.

2) **Per-core write signatures:** Our second observation is that a core \( c \) can skip self-invalidating a line if that line has not been updated in the LLC by another core since \( c \)'s last acquire operation. To identify such lines, Neat maintains per-core write signatures at the LLC. A core \( c \)'s write signature indicates which of \( c \)'s private lines were updated in the LLC by any other core since \( c \)'s last acquire operation. Each write-back to an LLC line by core \( d \) adds the line (address) to the write signatures for all cores other than \( d \).

A core fetches its write signature at the start of self-invalidation and only invalidates (or partially invalidates) those lines contained in the write signature. The LLC clears a core’s write signature once it services the core’s fetch request for the write signature. We note that a core fetches its write signature only after the core succeeds on an acquire, so under the DRF assumption, there is no race on write signatures.

The write signature mechanism is important mainly when acquire operations and thus self-invalidations are frequent. When acquire operations are infrequent, self-invalidations are less frequent, and their costs tend to amortize better over
other execution costs. We can thus optimize for frequent self-invalidations by making write signatures small, which saves time and area by avoiding sending and storing large write signatures. Our implementation uses Bloom filters for over-approximated write signatures and sends compressed versions of sparsely populated write signatures (Section V).

IV. EVALUATION OF CORRECTNESS AND COMPLEXITY

We validated Neat’s correctness and quantitatively evaluated Neat’s complexity, directly comparing to the complexity of a MESI protocol implementation, in the widely used Murphi model checking tool [15].

A. Methodology

We implemented MESI in Murphi based on the GEMS two-level MESI protocol [27]. We implemented Neat in Murphi by directly specifying the protocol described in Section III. For both MESI and Neat, our specifications model two cores, a two-level cache hierarchy (i.e., private L1s and a shared LLC), an unordered network with unlimited capacity, two data values, and up to two lines and two bytes per line. In addition to modeling standard cache operations due to reads, writes, and evictions of lines, the MESI and Neat specifications model acquire and release operations.

Verification using a Murphi model serves two purposes: providing a demonstration that the protocols are correct, and allowing a comparison of the complexity of the protocols. We will make our Neat model and modified MESI model publicly available so that others can reproduce and modify our evaluation of correctness and complexity.

To check correctness, both specifications check a “last-write” assertion for each state explored by Murphi: any read by a core of a byte in a cache line should see the same value written by the last write by any core. (The specifications also check protocol-specific assertions, e.g., the MESI specification checks the “single writer” invariant that there is at most one modifiable protocol state (i.e., the state before execution starts), effectively cutting off exploration of racy states.

B. Protocol Complexity Results

Table II reports how many execution states Murphi explored for the MESI specification and three variants of the Neat specification. Neat base is the baseline Neat; Neat pi-only includes the partially invalid (PI) state mechanism; and Neat is the full version of Neat and includes the PI state and write signature mechanisms. For each configuration, the table reports states explored by Murphi for the four combinations of 1–2 lines and 1–2 bytes per line.

As the results show, MESI’s complexity (i.e., number of states) increases more quickly than Neat’s complexity as the number of lines in the cache increases. This is because MESI requires per-line transient states to keep the lines coherent. In contrast, Neat’s complexity increases more quickly than MESI’s as the number of bytes per line increases, because Neat maintains per-byte write bits for private cache lines. However, Neat’s relative complexity for an additional byte is lower than MESI’s relative complexity for an additional line, since MESI’s per-line state space is considerably larger than Neat’s per-byte state space: MESI adds many transient states per line, while Neat adds a single write bit per byte.

The verification state space is large for a Neat or MESI configuration with two lines and two bytes per line. Except for Neat base, Murphi never completed checking any of the configurations (indicated by Timeout in the table), even after exploring hundreds of millions of states, which took several days running on a VM hosted by Google Compute Engine.

The main takeaway from these results is that Neat is considerably less complex than MESI. MESI and the full Neat configurations with just one line have comparable numbers of states, with Neat having somewhat fewer states. For the two-line, one-byte configuration, Neat has 20× fewer states than MESI, due to Neat’s small per-line state space.

V. EVALUATION OF PERFORMANCE AND ENERGY

This section evaluates the performance and energy usage of Neat, compared with a state-of-the-art MESI protocol implementation [28], [36] and two self-invalidation-based protocols from the literature [19], [30].

A. Implementation and Methodology

Our experiments measure run-time performance and energy consumption, using the RADISH simulator [14] modified to implement (1) Neat, (2) a directory-based MESI protocol implementation [36], and two self-invalidation-based protocols, (3) SARC [19] and (4) VIPS [30]. We will make our simulation and modeling infrastructure publicly available. All simulator backends consume the same trace of instructions from a PIN-based front end [26]. Each core has a two-level private cache hierarchy, and the LLC is backed by off-chip main memory. A core’s L2 is inclusive of its L1. The LLC is not inclusive of private caches for SARC, VIPS, and Neat (and need not
be), but the LLC is inclusive of the L2 for MESI to support an inclusive directory cache embedded in the LLC [36].

Our simulators model and measure execution cycles and on-chip traffic, using parameters shown in Table III. The simulators model single-issue, in-order cores in which non-memory instructions have an IPC of one, and an interconnect network that uses 16-byte flits. The Neat and VIPS simulators model the cycle cost of performing self-invalidation and commit (either bulk write-backs by Neat or delayed write-throughs by VIPS) at synchronization operations based on the total size of messages sent and the bandwidth available between a core and the LLC. We report the maximum cycles of any core as execution time.

To measure energy consumption, we use the McPAT energy modeling tool [23], providing it with the output statistics from our simulator. We report total energy for the cache and memory subsystem, including the on-chip interconnect and LLC-to-memory communication. We exclude reporting energy for operations within the cores because our simulator does not collect detailed core-level statistics such as ALU and branch instructions, which McPAT needs to compute a core’s energy usage. However, these excluded operations and thus the excluded energy should be identical across all configurations.

We use McPAT to model energy of all MESI, Neat, SARC, and VIPS components across the cache and memory subsystem, with one exception: It is unclear how to model Neat’s Bloom-filter-based write signatures (Section III-C) in McPAT, so we estimate the per-access energy of Bloom filters using values reported by prior work [34]. Each core’s write signature is a 1008-bit Bloom filter (which fits in eight 16-byte flits including a control message). Specifically, we assume L-CBFs, each with 1008 1-bit counters, and derive their per-operation dynamic energy by assuming linear relationships between the per-operation energy and entry count (as well as count width) for an L-CBF. We compute total dynamic energy due to write signature operations by multiplying the per-operation energy by the numbers of write signature operations counted in the simulator.

**Evaluated configurations:** Table IV shows the configurations we evaluate.

**Neat base** is baseline Neat; **Neat pi-only** includes the partially invalid (PI) state mechanism; and **Neat** is the full version of Neat and includes the PI state and write signature mechanisms. **Neat cla** is Neat plus two page-level classification optimizations used by VIPS: private vs. shared pages, and read-only vs. read-write pages [30] (Section II-B).

We evaluate a configuration called SARC based on the design described by prior work [19]. We also implemented and evaluated an idealized (perfect) implementation of SARC’s writer prediction [19], but found that it had negligible performance impact, so we exclude writer prediction from the evaluation for simplicity.

In contrast with Neat and SARC, VIPS uses write-through caches; MSHRs buffer write-throughs until they run out, or a timeout or synchronization release is reached [30]. To approximate the MSHRs’ behavior, our simulator implements a write-through buffer with an LRU eviction policy and an infinite timeout.

VIPS classifies private and shared memory pages and read-only and read-write pages to avoid unnecessary self-invalidation. **PI** = Neat’s partially invalid state. **WS** = Neat’s write signatures. **CLA** = VIPS’s page classifications.
through and self-invalidates all lines, effectively treating all lines as shared and read-write. VIPS unopt is like Neat base in how both protocols commit and self invalidate cache lines at synchronization operations, though VIPS unopt is subject to the limited capacity of the write-through buffer (10 entries) and does not wait until the next release to commit all dirty lines as the Neat configurations do. We note that VIPS unopt represents so-called “GPU coherence” (Section [11-12]). VIPS cla adds the classifications to VIPS unopt, writing through and self-invalidating only those lines that are marked as shared and read-write. For lines that are marked as private, VIPS cla writes them back to the LLC only on L2 eviction if they are dirty.

Workloads: Our experiments run the PARSEC 3.0 benchmarks \([6]\), three real server programs, and the Phoenix benchmarks that contain false sharing \([29]\).

For most of the PARSEC benchmarks, we use simsmall inputs; we use simmedium for swaptions since simsmall does not support \(>16\) threads. We use 11 of 13 PARSEC programs; facesim fails to finish executing with the simulators, and freqmine uses OpenMP instead of pthreads.

The experiments execute three real server programs: Apache HTTP Server 2.4.23 (httpd), Memcached 1.5.2 (memcached), and MySQL Server 5.7.16 (mysqld). We configure each program to create a single process with 32 worker threads. For httpd, we launch 32 client processes that repeatedly and concurrently perform simple HTTP requests to HTML pages randomly selected from a pool of 100 pages. For memcached and mysqld, we use the benchmark tools memtier benchmark and sysbench, respectively, to generate workloads. Each of the benchmark tools starts 32 client threads to send workloads that perform different mixes of set and get operations (memcached) or addition/deletion/update and select operations (mysqld). We configure memtier benchmark to generate mixed Memcached requests with the following ratios of gets to sets: 0:100, 10:90, 50:50, and 10:90. For mysqld, sysbench generates transactions of mixed SQL queries using the benchmark tool’s build-in read-only (ro), read-write (rw), and write-only (wo) workloads. In our experiments, client processes or threads executing natively send 32,768 HTTP requests (httpd), 262,144 Memcached requests (memcached), or 8,192 SQL transitions (mysqld), distributed evenly over all 32 client processes or threads.

To evaluate Neat’s benefits on false sharing, our experiments run three Phoenix benchmarks: histogram, linear_regression, and word_count. We selected the benchmarks in which prior work detected false sharing \([21]\), excluding benchmarks in which false sharing is mostly inside pthread functions (according to Linux’s perf c2c utility), whose code is ignored by our simulators. As observed by prior work, gcc eliminates false sharing at certain optimization levels \([23]\). Our experiments compile each program with gcc 4.8.5 at the highest optimization level at which false sharing exists: histogram and linear_regression at O1, and word_count at O3.

Our simulators only compute cycles for the “region of interest” (ROI). For each PARSEC or Phoenix program, its ROI includes its whole parallel phase; vips lacks an ROI annotation so we treat its entire execution as the ROI. For server programs, the ROI is all execution except the startup and shutdown phases.

Handling pthreads functions and atomic instructions: All simulators identify each pthreads function call as a synchronization operation. Self-invalidation-based configurations perform relevant coherence actions at synchronization operations, while Mesi ignores all synchronization operations. All simulators ignore all instructions executed inside pthreads functions.

The Neat, SARC, and VIPS simulators each treat non-pthreads atomic instructions (i.e., instructions with the LOCK prefix) as lock operations but not region boundaries, and thus do not perform any coherence actions but instead execute a distributed queue-based locking protocol \([33]\). Mesi treats atomic instructions as regular memory accesses.

Our Neat (and SARC and VIPS) implementations do not deal with how to implement spin-waiting efficiently under self-invalidation; we assume a Neat implementation would use an existing mechanism \([31], [32], [33]\).

B. Results

Figures 4 and 5 evaluate Neat’s performance and energy consumption, respectively, compared with Mesi, SARC, and VIPS, for all programs. Each bar is normalized to Mesi in all figures. Table \(V\) shows how many lines are self-invalidated and committed per synchronization operation. Note that the table’s commit counts include (i) all write-throughs made by the VIPS configurations at write buffer evictions and synchronization operations and (ii) all write-backs made by the Neat configurations at synchronization operations, but do not include any regular write-backs due to L2 evictions.

Performance: Figure 4 compares execution cycles (maximum cycles of any core) for all programs. The data show that, for most of the PARSEC benchmarks, the configurations have similar performance. For canneal, fluidanimate, and streamcluster, the SARC and VIPS configurations are 3–16% slower than Mesi \([7]\). In contrast, the full Neat configuration achieves virtually the same performance as Mesi. On average, Neat and Neat cla are nearly at parity with Mesi, with an average run-time difference of less than 1%.

For the server programs, some self-invalidation-based configurations are as much as \(4\times\) slower than Mesi. Neat performs significantly better than SARC and VIPS, with Neat executing 1.2× and 1.6× faster than SARC and VIPS cla, respectively. A run-time breakdown (results not shown) shows that the significant slowdowns for self-invalidation-based configurations are caused mainly by cache misses due to unnecessary self-invalidation. Table \(V\) shows that both of Neat’s mechanisms are collectively effective in reducing self-invalidations. VIPS’s classifications are effective, too, further helping Neat cla achieve performance close to Mesi’s (11% slower on average).

For two of the Phoenix benchmarks, Neat and VIPS improve performance significantly over Mesi and SARC by eliminating

\(^{2}\)The VIPS paper also evaluated canneal, raytrace, and x264, but reported different results, presumably due to different architectural parameters used for simulation \([30]\). The VIPS paper acknowledges that VIPS is slightly (less than 3%) slower than Mesi for 256KB private caches, which agrees with our results.
writer-initiated invalidations caused by false sharing. Neat and VIPS do not benefit word_count as much since the program does not contain as much false sharing as the other two. Neat’s mechanisms and VIPS’s classifications to avoid unnecessary self-invalidations have negligible impact on performance since the programs all execute few synchronization operations (by using fork–join parallelism).

Energy: Figure 5 compares the energy consumption of all configurations for all the programs, which is divided into energy due to static and dynamic energy consumption. For configurations with the write signature mechanism, dynamic energy is further divided into energy from write signature operations and from other sources (see Section V-A).

Neat imposes a lower static power cost than MESI and SARC because it eliminates the need to maintain a large, shared coherence directory. Neat’s mechanisms that avoid unnecessary self-invalidations further help reduce energy since they help reduce execution time. VIPS imposes an even lower static power than Neat because it does not require per-byte metadata in the private caches as Neat does for the write bits.

On average, for the PARSEC benchmarks, Neat (and Neat cla) consume approximately 6% and 7% less energy than MESI and SARC, respectively, but 6% more than VIPS cla. For the server programs, Neat consumes 44% more energy than MESI, but 18% and 30% less than SARC and VIPS cla, respectively. Neat cla consumes 9% more energy than MESI, much less than the SARC and VIPS configurations. For the Phoenix benchmarks, Neat (and Neat cla) consume approximately 32%,
In summary, the results in this section show that for less-complex programs such as the PARSEC benchmarks, Neat has performance and energy competitive with MESI and outperforms SARC and VIPS. Neat has significant benefits over MESI and SARC specifically for programs with false sharing. For complex server programs, Neat is slower and consumes more energy than MESI, but still has significant benefits over SARC and VIPS. VIPS’s classifications benefit Neat and improve Neat to be competitive with MESI. The evaluations in this section and Section [IV] show that Neat is not only a novel system design, but it improves in complexity compared to MESI and improves in performance and energy consumption compared to SARC and VIPS (and MESI for programs with false sharing).

VI. RELATED WORK

Sections III compared Neat qualitatively with closely related work that uses self-invalidations [19], [30], [13], [38], [35], [12]. This section discusses other related work. Other DeNovo-based work: DeNovoSync uses DeNovo’s protocol that employs self-invalidation and registration, but—like SARC, VIPS, and Neat—DeNovoSync applies to general shared-memory programs [37]. DeNovoSync’s contribution focuses on supporting arbitrary synchronization operations in the context of self-invalidation. The evaluation limits self-invalidation costs by assuming programmer annotations. In contrast, Neat uses automatic mechanisms to reduce self-invalidation and assumes no additional knowledge.

Spandex provides a flexible interface that supports various coherence protocols, including MESI, GPU coherence, and DeNovo [4]. It necessarily suffers MESI’s complexity overhead, including transient states, Inv and Ack messages, and support for core-to-core communication. In contrast, Neat does not need to support MESI or other protocols.

Exploiting self-invalidation-based coherence: ARC uses self-invalidation and defers dirty write-backs until release operations [22]. While Neat assumes data race freedom (DRF), ARC checks DRF, leading to a more complex system. Although ARC optimizes self-invalidation and dirty write-back costs, its optimizations differ from Neat’s by leveraging mechanisms for performing conflict detection.

Jimboorean et al. use compile-time analysis to detect extended DRF regions and thus reduce the frequency of self-invalidation [18]. Extended DRF regions would apply to Neat.

Using write signatures to represent write sets: Prior work has used write signatures to represent a core’s own write set [38], [39]. In contrast, in Neat a core’s write signature represents writes by all other cores (and the signatures are thus maintained at the LLC). An exception is Racer [32], which maintains write signatures in a similar way to Neat, but for a distinct purpose: detecting read-after-write races in order to treat them as synchronization points.

VII. CONCLUSION

Neat is a new cache coherence design that avoids unnecessary self-invalidations and performs bulk write-backs at synchronization operations. Unlike other self-invalidation approaches, Neat does not rely on programmer annotations or specific access patterns for efficiency. Our evaluation shows that Neat is simpler than MESI, performs competitively with MESI especially under false sharing, and provides better performance and energy efficiency than two state-of-the-art self-invalidation-based approaches. These results suggest that Neat provides sufficient, complexity-effective coherence.

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REFERENCES

[1] S. V. Adve and H.-J. Boehm. Memory Models: A Case for Rethinking Parallel Languages and Hardware. *CACM*, 53:90–101, 2010.
[2] S. V. Adve, A. L. Cox, S. Dwarkadas, R. Rajamony, and W. Zwaenepoel. A Comparison of Entry Consistency and Lazy Release Consistency Implementations. In *HPCA*, pages 26–37, 1996.
[3] J. Alsop, M. S. Orr, B. M. Beckmann, and D. A. Wood. Lazy Release Consistency forGPUs. In *MICRO*, pages 1–14, 2016.
[4] J. Alsop, M. D. Sinclair, and S. V. Adve. Spandex: A Flexible Interface for Efficient Heterogeneous Coherence. In *ISCA*, pages 261–274, 2018.
[5] B. N. Bershad and M. J. Zezula. Midway: Shared Memory Parallel Programming with Entry Consistency for Distributed Memory Multiprocessors. Technical Report CMU-CS-91-170, Carnegie Mellon University, 1991.
[6] C. Bienia, S. Kumar, J. P. Singh, and K. Li. The PARSEC Benchmark Suite: Characterization and Architectural Implications. In *PACT*, pages 72–81, 2008.
[7] S. Biswas, R. Zhang, M. D. Bond, and B. Lucia. Rethinking Support for Region Conflict Exceptions. In *IPDPS*, pages 1095–1106, 2019.
[8] B. H. Bloom. Space/Time Trade-offs in Hash Coding with Allowable Errors. *CACM*, 13:422–426, 1970.
[9] M. A. Blumrich, K. Li, R. Alpert, C. Dubnicki, E. W. Felten, and J. Sandberg. Virtual Memory Mapped Network Interface for the SHRIMP Multicomputer. In *ISCA*, pages 142–153, 1994.
[10] R. L. Bocchino, Jr., V. S. Adve, S. V. Adve, and M. Snir. Parallel Programming Must Be Deterministic by Default. In *HotPar*, pages 4–9, 2009.
[11] H.-J. Boehm and S. V. Adve. Foundations of the C++ Concurrency Memory Model. In *PLDI*, pages 68–78, 2008.
[12] M. Castro, P. Guedes, M. Sequeira, and M. Costa. Efficient and Flexible Object Sharing. In *ICPP*, August 1996.
[13] B. Choi, R. Komuravelli, H. Sung, R. Smolinski, N. Honarmand, S. V. Adve, V. S. Adve, N. P. Carter, and C.-T. Chou. DeNovo: Rethinking the Memory Hierarchy for Disciplined Parallelism. In *PACT*, pages 155–166, 2011.
[14] J. Devielli, B. P. Wood, K. Strauss, L. Ceze, D. Grossman, and S. Qadeer. RADISH: Always-On Sound and Complete Race Detection in Software and Hardware. In *ISCA*, pages 201–212, 2012.
[15] D. L. Dill, A. J. Drexlert, A. J. Hu, and C. H. Yang. Protocol Verification as a Hardware Design Aid. In *ICCD*, pages 522–525, 1992.
[16] C. Fensch and M. Cintra. An OS-Based Alternative to Full Hardware Coherence on Tiled CMPs. In *HPCA*, pages 355–366, 2008.
[17] B. A. Hechtman, S. Che, D. R. Hower, Y. Tian, B. M. Beckmann, M. D. Hill, S. K. Reinhardt, and D. A. Wood. QuickRelease: A Throughput-oriented Approach to Release Consistency onGPUs. In *HPCA*, pages 189–200, 2014.
[18] A. Jimboorean, J. Waern, P. Ekemark, S. Kaxiras, and A. Ros. Automatic Detection of Extended Data-Race-Free Regions. In *CGO*, pages 14–26, 2017.
| Program     | SARC | VIPS unopt | VIPS cla | Neat base | Neat pi-only | Neat | Neat cla |
|-------------|------|------------|----------|-----------|--------------|------|---------|
| blackscholes| 142 / - | 64 / 463 | 25 / 30 | 64 / 71 | 2 / 70 | 0 / 70 | 0 / 30 |
| bodytrack   | 780 / - | 823 / 304 | 786 / 48 | 823 / 82 | 751 / 41 | 697 / 41 | 380 / 21 |
| canneal     | 3,030 / - | 3,590 / 182 | 3,420 / 73 | 3,590 / 126 | 233 / 130 | 233 / 130 | 119 / 54 |
| dedup       | 90 / - | 613 / 3,650 | 82 / 33 | 613 / 600 | 123 / 496 | 95 / 496 | 12 / 11 |
| ferret      | 159 / - | 335 / 11,400 | 68 / 323 | 335 / 336 | 32 / 169 | 28 / 169 | 5 / 41 |
| fluidanimate| 8 / - | 17 / 10 | 12 / 2 | 17 / 10 | 15 / 5 | 1 / 5 | 0 / 1 |
| raytrace    | 563 / - | 589 / 1,956 | 566 / 247 | 589 / 103 | 19 / 52 | 15 / 52 | 14 / 37 |
| streamcluster| 55 / - | 61 / 4 | 57 / 2 | 61 / 4 | 60 / 4 | 13 / 4 | 5 / 2 |
| swapplings  | 24 / - | 26 / 2,640,000 | 10 / 12 | 26 / 317 | 3 / 317 | 0 / 317 | 0 / 12 |
| vips        | 45 / - | 152 / 389 | 47 / 12 | 152 / 192 | 37 / 96 | 17 / 96 | 4 / 10 |
| x264        | 247 / - | 579 / 10,800 | 341 / 1,790 | 579 / 806 | 105 / 493 | 103 / 493 | 65 / 156 |

httpd       | 154 / - | 203 / 235 | 166 / 123 | 203 / 128 | 153 / 68 | 144 / 68 | 120 / 54 |
| memcached-0:100 | 11 / - | 25 / 19 | 11 / 3 | 25 / 20 | 22 / 10 | 8 / 10 | 1 / 2 |
| memcached-10:90  | 11 / - | 26 / 18 | 13 / 4 | 26 / 20 | 23 / 10 | 9 / 10 | 1 / 2 |
| memcached-50:50  | 9 / - | 21 / 15 | 12 / 4 | 21 / 16 | 18 / 8 | 6 / 8 | 2 / 3 |
| memcached-90:10  | 9 / - | 19 / 14 | 11 / 4 | 19 / 15 | 16 / 8 | 6 / 8 | 2 / 3 |
| mysql-ri         | 9 / - | 19 / 14 | 11 / 4 | 19 / 15 | 16 / 8 | 6 / 8 | 2 / 3 |
| mysql-ri         | 102 / - | 117 / 23 | 104 / 4 | 117 / 20 | 111 / 10 | 9 / 10 | 2 / 2 |
| mysql-ri-wo      | 89 / - | 103 / 25 | 90 / 5 | 103 / 20 | 96 / 10 | 11 / 10 | 3 / 3 |

| histogram     | 37 / - | 44 / 25,341 | 26 / 20,460 | 44 / 51 | 2 / 51 | 0 / 51 | 0 / 46 |
| linear_regression | 421,976 / - | 20 / 6 | 4 / 6 | 20 / 7 | 2 / 7 | 0 / 7 | 0 / 6 |
| word_count    | 6,403 / - | 21 / 5,516,724 | 9 / 1,513,546 | 21 / 1,399 | 2 / 1,399 | 0 / 1,399 | 0 / 500 |

TABLE V

AVERAGE LINES SELF-INVALIDATED/COMMITTED PER ACQUIRE/RELEASE, RESPECTIVELY (ROUNDED TO 3 SIGNIFICANT FIGURES OR NEAREST INTEGER) FOR THE PARSEC BENCHMARKS AND SERVER PROGRAMS. Note: SARC does not have a commit operation (denoted “-”).

[19] S. Kaxiras and G. Keramidas. SARC Coherence: Scaling Directory Cache Coherence in Performance and Power. *IEEE Micro*, 30(5):54–65, 2010.

[20] P. Keleher, A. L. Cox, and W. Zwaenepoel. Lazy Release Consistency for Software Distributed Shared Memory. In *ISCA*, pages 13–21, 1992.

[21] T. A. Khan, Y. Zhao, G. Pokam, B. Mozafari, and B. Kasikci. Huron: Hybrid False Sharing Detection and Repair. In *PLDI*, pages 453–468, 2019.

[22] R. Komuravelli, S. V. Adve, and C.-T. Chou. Revisiting the Complexity of Hardware Cache Coherence and Some Implications. *TACO*, 11(4), 2014.

[23] S. Li, J. H. Ahn, R. D. Strong, J. B. Brockman, D. M. Tullsen, and N. P. Jouppi. McPAT: An Integrated Power, Area, and Timing Modeling Framework for Multicore and Manycore Architectures. In *MICRO*, pages 469–480, 2009.

[24] T. Liu, C. Tian, Z. Hu, and E. D. Berger. PREDATOR: Predictive False Sharing Detection. In *PPoPP*, pages 3–14, 2014.

[25] B. Lucia, L. Ceze, K. Strauss, S. Qadeer, and H.-J. Boehm. Conflict Exceptions: Simplifying Concurrent Language Semantics with Precise Hardware Exceptions for Data-Races. In *ISCA*, pages 210–221, 2010.

[26] C.-K. Luk, R. Cohn, R. Muth, H. Patil, A. Klauser, G. Lowney, S. Wallace, V. J. Reddi, and K. Hazelwood. Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation. In *PLDI*, pages 190–200, 2005.

[27] M. M. K. Martin, D. J. Sorin, B. M. Beckmann, M. R. Marty, M. Xu, A. R. Alameldeen, K. E. Moore, M. D. Hill, and D. A. Wood. Multifacet’s Analysis Tools with Dynamic Instrumentation. In *PLDI*, pages 190–200, 2005.

[28] M. D. Sinclair, J. Alsop, and S. V. Adve. Efficient GPU Synchronization without Scopes: Saying No to Complex Consistency Models. In *MICRO*, pages 647–659, 2015.

[29] A. Ros and S. Kaxiras. Complexity-Effective Multicore Coherence. In *PLDI*, pages 13–21, 1992.

[30] E. Safi, A. Moshovos, and A. Veneris. L-CBF: A Low-Power, Fast Counting Bloom Filter Architecture. *VLSI*, 16(6):628–638, 2008.

[31] H. Sung, R. Komuravelli, and S. V. Adve. DeNovoSync: Efficient Support for Arbitrary Synchronization Without Writer-Initiated Invalidations. In *ASPLOS*, pages 545–559, 2015.

[32] Y. Yao, G. Wang, Z. Ge, T. Mitra, W. Chen, and N. Zhang. Efficient Timestamp-Based Cache Coherence Protocol for Many-Core Architectures. In *ICS*, 2016.