Efficient design of 15:4 counter using a novel 5:3 counter for high-speed multiplication

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Abstract
This paper proposes an efficient approach to design high-speed, accurate multipliers. The proposed multiplier design uses the proposed efficient 15:4 counter for the partial product reduction stage. This proposed 15:4 counter is designed using a novel 5:3 counter. The proposed 5:3 counter uses input re-ordering circuitry at the input side. As a result, the number of output combinations can be reduced from 18 to 12. As a result, the circuit complexity reduces. The proposed 5:3 counter and 15:4 counter are on average 28% and 19% improvement in the power delay product compared with the existing designs. The 16-bit multiplier designed using 5:3 and 15:4 counters is an average 22.5% improvement in power delay product compared with the existing designs.

1 | INTRODUCTION
Multiplier circuit is a data-path element of the processor and specialised hardware circuits that are used for signal/image processing applications. The high-speed multiplier design is still a need of the hour. One can design a high-speed multiplier by reducing the delay of the partial product reduction stage. Many techniques are available in the literature for the reduction of partial products. Among all, the compressor and counter-based reduction techniques are popular ones [1,2]. The basic difference between compressor and counter depends on the carry and Cout weights [1,2]. For example, a 4:2 compressor will be designed using two full adders, as shown in Figure 1, with the following equations:

\[ X_0 + X_1 + X_2 + X_3 + \text{Cin} = (\text{Cout} \cdot 2^3 + \text{Carry} \cdot 2^1 + \text{Sum} \cdot 2^0) \]  

(1)

The 5:3 counter is designed using two full adders and one half adder, as shown in Figure 2. The 5:3 counter will have the equation as follows:

\[ X_0 + X_1 + X_2 + X_3 + X_4 = \text{Cout} \cdot 2^3 + \text{Carry} \cdot 2^1 + \text{Sum} \cdot 2^0 \]  

(2)

From the compressor Equation (1), the Cout and Carry will have the same weights (2^1), but from the counter Equation (2), the Cout and Carry will have different weights, that is, 2^1 and 2^3, respectively. The compressor and counter functionality is the same (both counts the number of 1’s present in the input). It produces the results as binary in different weights. For example, consider X_0 = 1, X_1 = 1, X_2 = 1, X_3 = 1, and Cin = 1 then the 4:2 compressor produces the result as (Cout, Carry and Sum) = 111 (value is five based on Equation (1)) and the 5:3 counter will produce the result as (Cout, Carry and Sum) = 101 (value is five based on the Equation (2)). The rest of the input combinations and their corresponding outputs for the compressor and counter is shown in truth Tables 1 and 2.

This paper proposes a novel 5:3 counter and the proposed design is efficient in terms of area, power and delay. The proposed 5:3 counter is used in designing the 15:4 counter. The 15:4 counter block diagram is shown in the Figure 3. The 15:4 counter will have 15 inputs and 4 outputs and the equations for the 15:4 counter is as follows:
The designed counters are used in the partial product reduction stage of the multiplier. The energy per operation of the proposed multiplier is less than the existing one from the literature.

The rest of the paper is organised as follows. Section 2 presents a detailed literature review of counter-based multipliers. Section 3 gives the details of the proposed 5:3 and 15:4 counters and multiplier design methodology. Section 4 discusses implementation details and results and followed by the Section 5 Conclusion.

2 | LITERATURE REVIEW

The basic 5:3 counter is designed by two full adders and one half adder as shown in the Figure 2. Each full adder is designed by two XOR gates and a majority circuit [3]. In total, the 5:3 counter is designed using five XOR gates, five AND gates, and two OR gates. Since the basic 5:3 counter uses five XOR gates and it consumes more power and delay. Chowdhury et al. [4] has proposed a 5:3 counter with a lesser delay than the basic 5:3 counter. The authors have replaced the full adder design using two XOR gates and one multiplexer as shown in the Figure 4. The overall 5:3 counter design will have five XOR gates and two multiplexers, and one AND gate. The authors have used their proposed 5:3 counter to design 15:4 counter [4]. Authors [5] have proposed a 15:4 counter using a 5:3 counter. The 5:3 counter design of Marimuthu et al. [5] has shown in the Figure 5. The authors have focused on reducing the delay using 4:1 multiplexer. Asif and Kong [6] have proposed a 4:3 counter, 5:3 counter and 7:3 counter using propagation and generation blocks. The existing three types of counters are used in the 16-bit Wallace tree multiplier. Few more designs from the literature are available in Hsiao et al. [7] and its circuit diagram is shown in Figure 6.

The authors have designed a 5:2 compressor using a 4:2 compressor and 3:2 counter. The proposed 5:2 compressor is used in designing multiplier, and thereby they have designed 16 × 16 MAC [8]. The worst path of this 5:2 compressor will
TABLE 2  Truth table of conventional 5:3 counter

| X0 | X1 | X2 | X3 | X4 | Value | Cout | Carry | Sum |
|----|----|----|----|----|-------|------|-------|-----|
| 0  | 0  | 0  | 0  | 0  | 0     | 0    | 0     | 0   |
| 0  | 0  | 0  | 0  | 1  | 1     | 0    | 0     | 1   |
| 0  | 0  | 0  | 1  | 0  | 1     | 0    | 0     | 1   |
| 0  | 0  | 1  | 0  | 1  | 2     | 0    | 1     | 0   |
| 0  | 0  | 1  | 0  | 1  | 1     | 0    | 0     | 1   |
| 0  | 0  | 1  | 1  | 0  | 2     | 0    | 1     | 0   |
| 0  | 0  | 1  | 1  | 1  | 3     | 0    | 1     | 1   |
| 0  | 0  | 0  | 0  | 1  | 0     | 0    | 1     | 0   |
| 0  | 1  | 0  | 0  | 1  | 2     | 0    | 1     | 0   |
| 0  | 1  | 0  | 1  | 0  | 2     | 0    | 1     | 0   |
| 0  | 1  | 0  | 1  | 1  | 3     | 0    | 1     | 1   |
| 0  | 1  | 1  | 0  | 0  | 2     | 0    | 1     | 0   |
| 0  | 1  | 1  | 0  | 1  | 3     | 0    | 1     | 1   |
| 0  | 1  | 1  | 1  | 1  | 4     | 1    | 0     | 0   |
| 0  | 1  | 1  | 1  | 1  | 4     | 1    | 0     | 0   |
| 1  | 0  | 0  | 0  | 0  | 0     | 0    | 0     | 0   |
| 1  | 0  | 0  | 1  | 2  | 0     | 1    | 0     | 0   |
| 1  | 0  | 0  | 0  | 2  | 0     | 1    | 0     | 0   |
| 0  | 0  | 0  | 1  | 0  | 2     | 0    | 1     | 0   |
| 0  | 0  | 0  | 1  | 1  | 3     | 0    | 1     | 1   |
| 1  | 0  | 1  | 0  | 0  | 2     | 0    | 1     | 0   |
| 1  | 0  | 1  | 0  | 1  | 3     | 0    | 1     | 1   |
| 1  | 0  | 1  | 1  | 0  | 3     | 0    | 1     | 1   |
| 1  | 0  | 1  | 1  | 1  | 4     | 1    | 0     | 0   |
| 1  | 1  | 0  | 0  | 0  | 2     | 0    | 1     | 0   |
| 1  | 1  | 0  | 1  | 3  | 0     | 1    | 1     | 1   |
| 1  | 1  | 0  | 1  | 1  | 4     | 1    | 0     | 0   |
| 1  | 1  | 1  | 0  | 0  | 3     | 0    | 1     | 1   |
| 1  | 1  | 1  | 0  | 1  | 4     | 1    | 0     | 0   |
| 1  | 1  | 1  | 1  | 0  | 4     | 1    | 0     | 0   |
| 1  | 1  | 1  | 1  | 1  | 5     | 1    | 0     | 1   |

FIGURE 3  15:4 counter block diagram

FIGURE 4  The existing 5:3 counter by Chowdhury et al. [4]

FIGURE 5  The existing 5:3 counter by Marimuthu et al. [5]

2.1  Contribution of this paper

This paper proposes a novel accurate 5:3 counter and 15:4 counter. The proposed 15:4 counter is designed using the proposed 5:3 counter. The design of the 5:3 counter is done by...
using the input re-ordering circuit to reduce the circuit complexity. As the proposed counter uses primitive gates, XOR gate, and one 2:1 multiplexer. This paper also proposes a 16-bit multiplier design using proposed 15:4 and 5:3 counters. The circuit complexity of the proposed design is lesser than the existing counters based multiplier design. As a result, the power delay product reduces.

3 | PROPOSED HIGH-SPEED MULTIPLIER DESIGN USING PROPOSED COUNTERS

This Section proposes a high-speed multiplier design using the proposed novel 5:3 and 15:4 counters. The rest of this Section is organised into three parts. Part A presents the proposed novel 5:3 counter design methodology, followed by part B illustrate the design of 15:4 counter using the proposed 5:3 counter, and finally, part C explains the design methodology of high-speed multiplier design using the proposed counters.

3.1 | Proposed novel 5:3 counter

The basic operation of the 5:3 counter is to count the number of 1's present in the input combinations, and the resultant output will vary from value 0 to 5, as shown in the truth Table 2. In truth Table 2, the value column represents the number of 1's present in the input combination. The value 1 as output has occurred for five different input combinations in Table 2. All these five input combinations can be reduced to fewer combinations if one can re-order the inputs. For example, value 1 occurs for different input combinations such as 00001, 00010, 00100, 01000 and 10000. These five combinations are applied to the input re-ordering circuit to produce the output as three combinations 10000, 00001 and 00100. On the same-line rest of the combinations can also be reduced using the input re-ordering circuit. The basic intuition is to reduce the number of output combinations from the input using the input re-ordering circuit, as shown in Figure 7 for the truth Table 2.

\[
\begin{align*}
  \text{Cout} &= Y_0 \cdot (Y_1 + Y_2) \\
  \text{Carry} &= Y_0 \cdot (Y_1 + Y_2) \oplus P \\
  \text{Sum} &= R \oplus Y_4 \\
\end{align*}
\]

where

\[
\begin{align*}
  P &= \overline{R} \cdot Y_3 + R \cdot Y_4 \\
  R &= Y_0 \cdot \overline{Y_1} \oplus Y_2 \cdot Y_3
\end{align*}
\]

The proposed 5:3 counter is shown in Figure 8. The existing design, as shown in Figure 4, will take the three XOR gate delay to compute the Sum, and the proposed design requires only two XOR gate and AND-OR-Inverter gate. The proposed 5:3 counter is efficient in terms of power and delay compared with the literature's existing designs, and its detailed gate-level analysis presented in Table 5.

3.2 | Proposed novel 15:4 counter design

This Section proposed a novel 15:4 counter [5] design using the proposed 5:3 counter of the above Section and optimised the parallel adder of the final stage. The proposed 15:4 counter consists of five numbers of full adders connected in parallel in stage one. In stage two, it uses proposed 5:3 counters, and followed by stage three uses 4-bit parallel adder. In stage one, all the 15 inputs are connected to five full adders. As a result, full adders output 10 outputs (five Carrys and five Sums).
These 10 outputs are fed to all the carrys to one 5:3 counter, and all the sums are fed to another 5:3 counter. As a result, it produces three outputs (Cout, Carry, Sum) from each 5:3 counter. These six outputs are added using a parallel adder.

3.3 Proposed high-speed multiplier design

The high-speed multiplier design uses the proposed 15:4 counter and 5:3 counters. The Figure 10 shown 16 × 16 multiplier design using 5:3 counters and 15:4 counter. The entire design will have a depth of three stages, where in the first stage uses 6 numbers of 15:4 counter, 25 numbers of 5:3 counters, 2 half adders and 11 numbers of full adders. The second stage of the multiplier uses 18 numbers of 5:3 counters, 12 numbers of full adders and 9 half adders. In the third stage, one 5:3 counter, 24 numbers of full adders and 3 half adders are in parallel. The 5:3 counter at 5th column in the Figure 10 will get one more input from the carry of

| X0 | X1 | X2 | X3 | X4 | Value | Y0 | Y1 | Y2 | Y3 | Y4 |
|----|----|----|----|----|-------|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 0  | 0     | 0  | 0  | 0  | 0  | 0  |
| 0  | 0  | 0  | 0  | 1  | 1     | 1  | 0  | 0  | 0  | 0  |
| 0  | 0  | 0  | 1  | 0  | 1     | 1  | 0  | 0  | 0  | 0  |
| 0  | 0  | 0  | 1  | 1  | 2     | 1  | 1  | 0  | 0  | 0  |
| 0  | 0  | 1  | 0  | 0  | 1     | 0  | 1  | 0  | 0  | 0  |
| 0  | 0  | 1  | 0  | 1  | 2     | 1  | 0  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 0  | 2     | 1  | 0  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
| 0  | 0  | 1  | 1  | 1  | 3     | 1  | 1  | 1  | 0  | 0  |
the 4\textsuperscript{Th} column half adder. The Cout and Carry of 5:3 counter at 5\textsuperscript{Th} column will be fed carry as input to 6\textsuperscript{Th} column 5:3 counter and Cout is fed as input to the 7\textsuperscript{Th} column. In the column, 12 is mapped to 15:4 counter, where the other two inputs to this 15:4 counter are fed from the previous column (11\textsuperscript{Th}) carries of the two 5:3 counters. The three carries (O1, O2 and O3) of the 15:4 counter of 12\textsuperscript{Th} column is fed to 13\textsuperscript{Th}, 14\textsuperscript{Th} and 15\textsuperscript{Th} columns, respectively.

### RESULTS AND DISCUSSIONS

Each design has been modelled using Verilog HDL, simulated using Cadence Inclusive Unified Simulator v6.1. All the designs are implemented using the TSMC 45 nm technology library \((\text{tcbn45gsbwpc0988_cs.lib})\) using the Cadence Genus electronics design automation tool. The derived net-list was then passed to the Cadence tool for floor planning and routing. All
the simulations are done with single drive strength. The comparison results of the existing 5:3 counter and proposed 5:3 counter is shown in the Table 6. The percentage of improvement in the power, delay and power delay product (PDP) with the existing designs are shown in the Table 6.

The comparison results and the percentage of improvement of the proposed 15:4 counter and existing 15:4 counter’s area, PDP is shown in the Table 7. The implementation results and percentage of the 16 × 16 bit multiplier’s area, PDPs are tabulated as shown in Table 8. The area, PDP of the 32-bit multiplier is shown in Table 9.

The proposed 5:3 counter achieved on average of 28% improvement in power delay product, as shown in Table 6. The proposed 15:4 counter is achieving on average of 19.25% improvement in power delay product compared with the existing designs, as shown in Table 7. The proposed 16-bit multiplier achieves a 22.5% improvement in power delay product, as shown in Table 8.

We have synthesised 16 × 16 bit multiplier using 4:2 compressors, along with radix-4 Booth encoder with the final stage as Kogge-Stone adder, where we obtained area, power, delay, and power-delay product are 2005μm², 230.78μW, 1.67ns and 385.40fJ respectively. As Booth encoder is used to reduce the

**Table 6** Comparison results of proposed and existing 5:3 counter

| 5:3 counter | Area (μm²) | Power (nW) | % Power Reduction | Delay (ps) | % Delay Reduction | PDP (fJ) | % PDP Reduction |
|-------------|------------|------------|-------------------|------------|-------------------|---------|-----------------|
| Basic Figure 2 | 13 | 1840 | 8 | 135 | 9 | 248.4 | 15 |
| Existing [4] | 13 | 1701 | -0.35 | 147 | 16 | 250.04 | 16 |
| Existing [5] | 26 | 1960 | 13 | 163 | 24 | 319.48 | 34 |
| Existing [6] | 33 | 2868 | 41 | 137 | 10 | 392.91 | 47 |
| Proposed design | 14 | 1707 | – | 124 | – | 211.66 | – |

Abbreviation: PDP, power, delay and power delay product.

**Table 7** Comparison results of proposed and existing 15:4 counter

| 15:4 counter | Area (μm²) | Power (nW) | % Power Reduction | Delay (ps) | % Delay Reduction | PDP (fJ) | % PDP Reduction |
|-------------|------------|------------|-------------------|------------|-------------------|---------|-----------------|
| Basic Figure 2 | 62 | 10,973 | 7 | 275 | 4 | 3.02 | 11 |
| Existing [4] | 63 | 10,724 | 5 | 291 | 9 | 3.12 | 13 |
| Existing [5] | 89 | 11,305 | 10 | 304 | 13 | 3.43 | 21 |
| Existing [6] | 103 | 13,491 | 25 | 290 | 9 | 3.91 | 31 |
| Proposed design | 64 | 10,207 | – | 266 | – | 2.71 | – |

Abbreviation: PDP, power, delay and power delay product.

**Table 8** Comparison results of proposed and existing 16-bit multiplier

| 16 × 16 multiplier | Area (μm²) | Power (nW) | % Power Reduction | Delay (ps) | % Delay Reduction | PDP (fJ) | % PDP Reduction |
|---------------------|------------|------------|-------------------|------------|-------------------|---------|-----------------|
| Basic Figure 2 | 1568 | 245,330 | 8 | 1345 | 4 | 329.96 | 10 |
| Existing [4] | 1568 | 237,549 | 4 | 1384 | 6 | 328.76 | 10 |
| Existing [5] | 2309 | 262,330 | 14 | 1560 | 17 | 409.23 | 28 |
| Existing [6] | 2694 | 298,915 | 24 | 1671 | 22 | 499.48 | 41 |
| Proposed design | 1626 | 228,088 | – | 1304 | – | 297.42 | – |

Abbreviation: PDP, power, delay and power delay product.

**Table 9** Comparison results for 32-bit multiplier

| 32 × 32 Design | Area (μm²) | Power (nW) | Delay (ps) | PDP (fJ) |
|----------------|------------|------------|------------|----------|
| Basic Figure 2 | 6272 | 981,320 | 2600 | 2639.75 |
| Existing [4] | 6272 | 950,196 | 2768 | 2630.14 |
| Existing [5] | 9236 | 1,049,320 | 3120 | 3273.87 |
| Existing [6] | 10,776 | 1,195,660 | 3342 | 3995.89 |
| Proposed design | 6504 | 912,352 | 2608 | 2379.41 |

Abbreviation: PDP, power, delay and power delay product.
number of partial products during the partial product generation stage, partial products are reduced using the 4:2 compressors/counter. The effectiveness of the Booth encoder will be advantageous when we go for a higher bit of multiplier.

5 | CONCLUSION

This paper has proposed a novel 5:3 counter design, which is, on average, 28% improved in PDP compared to the existing designs. The same 5:3 counter is used to design the 15:4 counter. The proposed 15:4 counter is 19% improved in PDP compared with the existing designs. The proposed 5:3 and 15:4 counters are used to design the $16 \times 16$ bit multiplier design. The proposed design is 22.5% improved in PDP than the existing counter-based multiplier designs.

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