Asynchronous Many-Task (AMT) runtime systems take advantage of multi-core architectures with light-weight threads, asynchronous executions, and smart scheduling. In this paper, we present the comparison of the AMT systems Charm++ and HPX with the main stream MPI, OpenMP, and MPI+OpenMP libraries using the Task Bench benchmarks. Charm++ is a parallel programming language based on C++, supporting stackless tasks as well as light-weight threads asynchronously along with an adaptive runtime system. HPX is a C++ library for concurrency and parallelism, exposing C++ standards conforming API. First, we analyze the commonalities, differences, and advantageous scenarios of Charm++ and HPX in detail. Further, to investigate the potential overheads introduced by the tasking systems of Charm++ and HPX, we utilize an existing parameterized benchmark, Task Bench, wherein 15 different programming systems were implemented, e.g., MPI, OpenMP, MPI + OpenMP, and extend Task Bench by adding HPX implementations. We quantify the overheads of Charm++, HPX, and the main stream libraries in different scenarios where a single task and multi-task are assigned to each core, respectively. We also investigate each system’s scalability and the ability to hide the communication latency.

Keywords Asynchronous Many-Task (AMT) · Charm++ · HPX · Task Bench.
1 Introduction

Asynchronous Many-Task (AMT) systems emerge as an effective solution to the demands of adaptive applications. However, by utilizing the fine-grained parallelism, AMTs tend to generate runtime overheads which inhibits performance and counteracts their benefits. We are mainly interested in systems that expose distributed execution, which is the prevalent technique for massive computational experiments. Many options exist in the realm of parallel runtime systems, e.g., Uintah [1], Chapel [2], Legion [3], and PaRSEC [4]. For a more detailed survey of various AMTs, we refer to [5]. This research focuses on Charm++ [6] and HPX [7] since both systems provide a similar underlying programming model.

Charm++ delivers a highly abstracted environment for productivity bound to a flexible and performant execution paradigm. On the other hand, HPX provides a C++ standards conforming API and extends the standard parallel facilities by providing asynchronous and distributed components. Our goal is to objectively quantify the overheads of those two systems by evaluating measurements from intrinsic benchmark implementations characteristics. Further comparisons are presented against MPI and OpenMP for distributed and within-node parallel execution, respectively. For that, we utilize Task Bench, a unified benchmarking solution that evaluates these systems under a common ground.

Task Bench was proposed by Slaughter et al. [8] as a standardized solution that unifies the benchmarking process of various existing concurrency frameworks. It provides a backend benchmarking kernel that is exposed through a parameterized interface. Once Task Bench is implemented in a given programming system, it enables a straightforward comparative analysis with every other system in the Task Bench pool. Task Bench has already been implemented for Chapel [2], Dask [9], MPI, OmpSs [10], OpenMP, PaRSEC, Realm [11], Regent [12], Spark [13], StarPU [14], Swift/T [15], TensorFlow [16] and X10 [17]. This makes it suitable for our task of a fair comparison of two different systems under a common ground. The centralized results enable a direct comparison of the performance of each system in a wide spectrum of tasking paradigms that model various execution schemes corresponding to real-world experiments like the stencil pattern, the FFT pattern etc. We extend this work [8] by adding HPX implementations, and reproducing the same results for Charm++ and HPX with using MPI, OpenMP and MPI+OpenMP as a common denominator for the comparisons. Our results reflect those of the original authors and are accompanied by elaborate remarks.

The three major contributions of our work are:

1. This is the first work comparing Charm++ and HPX using the same benchmark. Different HPX implementations with respect to the Task Bench library are implemented, namely HPX local and HPX distributed, in order to fairly compare HPX with Charm++ against the mainstream MPI, OpenMP, and MPI+OpenMP. The optimizations of HPX implementations to minimize the overheads are further introduced.
2. The commonalities, differences, and advantageous scenarios of Charm++ and HPX, are analyzed in detail. The performance results further validate the analysis.
3. The overheads of Charm++ and HPX, along with several other programming systems, are quantified in terms of shared-memory parallelism and distributed-memory parallelism, in various scenarios wherein a single task and multi-task are assigned to each core, respectively.

The paper is structured as follows: Section 2 introduces the existing state-of-the-art performance evaluations. In Section 3 Charm++ and HPX are briefly introduced and the similarities and differences are discussed. In Section 4 we briefly introduce the ingredients of Task Bench used in this work. Section 5 summarizes the improvements to further reduce the overhead. Section 6 shows simulations in various scenarios without/with overdecomposition. Finally, Section 7 concludes the work.

2 Related work

Many existing works evaluate the performance of task-based parallel programming models. In what follows, we consider studies focusing on mini-apps: simple applications designed to represent the performance characteristics of full-fledged applications.

Karlin et al. [18] evaluate the performance and productivity characteristics of several traditional and task-based parallel programming models using the LULESH [19] mini-application for shock hydrodynamics. In [20], the authors implement a block eigensolver in OpenMP [21] and OpenACC [22] to assess the performance portability of these models. The Parallel Research Kernels [23–26] are a suite of mini-applications and microbenchmarks designed to assess the performance of different parallel systems and programming models. The authors in [27] implement a stencil mini-application in Legion [28] and MPI, observing similar weak-scaling performance between Legion and MPI. In [29],
the mini-application and communication microbenchmark performance of Python ports of established programming models Charm++ and MPI is compared. An extensive study at Sandia National Laboratory [30] compares 3 many-task programming models on qualitative and quantitative metrics.

While studies based on mini-application performance provide insight into the performance and programmability of different programming models, the $O(m \cdot n)$ complexity of implementing $m$ mini-applications in $n$ frameworks makes it onerous to comprehensively evaluate even a few programming models on a range of benchmarks. Section 4 describes another approach to facilitate such comparisons.

3 Asynchronous many-task systems

3.1 Charm++

Charm++ is a parallel programming language based on C++. Unlike the bulk-synchronous and process-centric approach taken by MPI, Charm++ implements a migratable-objects programming model. The basic unit of object in Charm++ is called a chare which is typically a class in C++. Functions in a chare can group logically-related execution and communication tasks, supporting data-encapsulation and locality. Users can designate some methods as entry methods for a chare class which are the methods that can be invoked by other, potentially remote, chares asynchronously. With the object-oriented approach, Charm++ supports overdecomposition, where the user can define multiple collections (“arrays”) of chares corresponding to the domain of the problem. Charm++ applications typically partition the domain into finer grains than the amount of available execution units (e.g. cores). The location of individual chares is controlled dynamically by Charm++’s adaptive runtime system (aRTS). On each core (or node, in some configurations), a user-space scheduler is used to asynchronously but non-preemptively execute the set of available method invocations. This data-driven execution allows Charm++ applications to adaptively overlap communication and computation. By leveraging migratability of chares, the aRTS supports dynamic load-balancing, as well as other capabilities such as fault-tolerance, shrinking or expanding the set of nodes assigned to a job in the middle of execution, power/energy/thermal optimizations etc.

3.2 HPX

HPX is a C++ Standard Library for parallelism and concurrency [7]. HPX is implemented as a lightweight user-level task manager running on top of kernel threads. It is widely known that thread creation and destruction managed by the operating system are expensive and reserve lots of memory. For that reason, HPX creates one thread per core and binds each of them to one of the cores. Therefore, the performance can be improved since there is no kernel-level interruption when the tasks are running. HPX is the first implementation of an advanced parallel execution model [31], which essentially resolves critical issues that prevent effective usage of new HPC systems: Starvation, Latency, Overheads, and Waiting for Contention. The HPX asynchronous programming model exposes a C++ standard API entirely conforming to interfaces as defined by C++11/C++14/C++17/C++20 and adds on top of the latest C++ standard by providing distributed and heterogeneous computing scenarios, which makes HPX portable and uniformly usable for local and remote parallelism. HPX aligns with the ongoing C++ standardization proposal with a goal of providing a uniform interface, in particular, related to parallelism and concurrency. HPX is widely used for applications that utilize both shared and distributed memory. PeriHPX [32] is an example of using HPX for shared-memory parallelism, and Octo-Tiger [33] is one example of using HPX for a distributed memory application.

3.3 Commonalities and differences

Both Charm++ and HPX are highly performant and feature rich AMTs that leverage asynchrony, overdecomposition, and migratability. These features are either implicitly or explicitly exposed to the user. For instance, Charm++ supports built-in migrations while HPX implements user assisted migrations. Furthermore, they bring different interpretations and consequently implementation details on certain key concepts. Charm++ defines a “Processing Element” (PE) that can be an OS thread or a process. Each chare is assigned to a PE by keeping it anchored to PEs to enhance locality of the computation. Note that chares can move to another PE according to load-balancing strategies to minimize communication or achieve more balanced load distribution. Multiple chares are assigned to a PE and user-level scheduler schedules entry method executions non preemptively based on availability of data (messages). On the other hand, HPX keeps the notion of locality explicit and the user needs to assign parallel execution to occur on a certain locality or locally if no locality is provided. Moreover, they both support threading, including features like thread suspension and resumption. While any parallel execution on HPX is run on an HPX thread, Charm++ threading is mainly utilized only in specially designated threaded entry methods that use blocking primitives (such as access to futures) that can otherwise block the scheduler if not run on a thread. The default entry methods are not threaded,
and can be considered as stack-less tasklets. Finally, Charm++ implements continuations by utilizing callbacks, while HPX utilizes C++ conforming futures that can retrieve the underlying computation result.

While both AMTs are feature rich, there are a few key areas in which Charm++ is advantageous. As HPX utilizes HPX threads for any parallel execution, it suffers from the overheads of the threading subsystem and further overheads of the networking interface. Charm++ schedules over each PE individually, i.e. anchoring each shares to a particular PE (and thereby to a core) except when load-balancing, enhances locality and allows lock-less interaction between entities assigned to the same PE. Furthermore, Charm++ supports load-balancing, automatic checkpoint-restart, and multiple communication protocols. Similarly, HPX supports load-balancing by enabling work-stealing scheduling policy, and supports explicit checkpoint, restart techniques, and several communication layers, e.g. TCP, MPI, and libfabrics, with others currently under work.

HPX provides some clear advantages over Charm++ as well. Given HPX exposes an ISO C++ conforming API, porting any standard C++ application to HPX is a mere search and replace. Porting to Charm++ requires careful restructuring of the program. Furthermore, HPX supports all the C++17 parallel algorithms along with various execution policies. An application developer can use these execution policies to achieve NUMA aware parallelism, explicit vectorization of loops, asynchronous algorithm execution, and much more. Charm++ requires the user to explicitly implement some of these features in their code. Given that HPX allows tracking of all function parameters and associated data either as a constant value reference or as rvalue references, the overheads associated are minimal. Charm++’s parameter marshalling and related copying overheads, resulting in higher overheads in the single node shared-memory setting.

Thus, Charm++ and HPX have similarities and differences, with multiple performance-oriented trade-offs based on the machine and programming model.

4 Task Bench

Task Bench is a parameterized benchmark for evaluating runtime system performance. Notably, Task Bench benchmarks are defined by task graphs expressing communication and task dependency patterns common in real-world applications. This task graph representation enables the evaluation of systems for benchmarks with $O(m+n)$ implementation effort, rather than the $O(m \cdot n)$ effort required by other benchmark suites. This dramatically reduces the programming effort required to evaluate new systems and benchmarks.

While strong and weak scaling have been the prevalent solutions for performance measurement, they both have the potential to yield misleading results. Strong scaling cannot isolate system overheads from application cost while weak scaling could hide the system overheads if large problem size is being used [8]. Task Bench uses METG (Minimum Effective Task Granularity) as a metric, which essentially indicates the scaling capabilities of the system on-target. METG exposes how high the computing performance (FLOP/s) can be maintained as the amount of work per task gets smaller. The reasoning behind METG is that for large problem sizes, all systems are expected to behave (almost) optimally. Conversely, for small problem sizes, parallelism becomes challenging. In this work, we use the same choice of 50% as the Task Bench paper [8] to compare the smallest average task granularity such that each system reaches at least 50% peak efficiency. We briefly introduce the ingredients of Task Bench used in this paper. For more details, we refer to [8].

5 Improvements

5.1 Charm++

Charm++ has organically grown over 20+ years, along with many applications and research projects, such as fault tolerance and energy management. As a result, the most general implementation tends to have accumulated overheads. Especially for running fine-grained benchmarks, it is useful to select build-time options carefully. The following briefly describes relevant options:

- **Eight-Byte Message Priority:** Charm++ supports arbitrary-length bit-vector message priorities, complicating the message receive path. A build option to use eight-byte message priorities simplifies it.
- **Simplified Scheduling Path:** We further simplify the message delivery path in Charm++ with these additional changes: no message priorities, no idle detection, and no condition-based or periodic callbacks.
- **Intranode IPC via Shared Memory:** By default, Charm++ uses the NIC for inter-process communication within a node. We assess the performance impact of shared-memory communication within a node.
Table 1: **Left** column: Compilers and libraries used to compile all systems. **Right** column: Hardware details of the rostam nodes.

| Software     | Hardware                     |
|--------------|------------------------------|
| gcc 11.2.0   | CPU AMD EPYC 7352 24-Core    |
| hwloc 2.6.0  | Memory 16 GB DDR-4 memory    |
| boost 1.78.0 | Interconnect 200Gb/s EDR Infiniband |
| gperftools 2.9.1 | cmake 3.22.0              |

Figure 1: Stencil pattern, 1 node (48 cores), 48 tasks.

(a) Tera FLOP/s vs grain size.  
(b) Efficiency vs task granularity

While we use the Charm++ implementation of Task Bench presented in [34], with the default build here, we provide some data with different build options to evaluate their impacts on fine-grained performance in section 6.3.

### 5.2 HPX

For HPX, two implementations are available, one is HPX local and another is HPX distributed. Their similarity is that a scheduling facility that is based on top of the current C++ Standard execution proposal [35], called executor, is deployed on both of them. Utilizing such an executor, HPX implementations benefit from retaining the spawning threads alive by allocating existing work to these threads. Further, such executor offers more ability and flexibility, e.g. users can determine the priority of worker threads, the stack size of the work threads, and enable or disable work-stealing policy. Note that work-stealing policy is advantageous when we consider overdecomposition, wherein each worker thread has a set of work in queue and the worker thread that finishes its local work can steal the work from currently active worker threads. HPX local and HPX distributed are also different. HPX local relies on HPX local facilities and does on-node computation, while HPX distributed depends on equivalent distributed facilities and manages communication on top of parallelization.

### 6 Experiments

All experiments were conducted on Buran nodes of the Rostam cluster. The hardware and software details are shown in Table 1. In Section 6.1 the overheads of Charm++, HPX, and other systems are measured when considering the scenario where the runtime overhead is dominant, and one computational task is assigned to each core. In Section 6.2, overdecomposition is adopted where more than one computational tasks are assigned to each core. We investigate the fine-grained performance of Charm++ in Section 6.3, where we use POSIX shared memory for intra-node communication, as described in Section 5.1. Each run is 1000 time steps long. Each data point has run 5 times, and a confidence interval with 99% confidence level is shown for the variance in the 5 runs.

### 6.1 Performance of a single task on each core

To characterize the performance limited by runtime overhead, the number of tasks is set to the number of total cores.
Table 2: METG (µs) of each system for the stencil pattern without/with different overdecomposition, using 1 node.

| System              | single task per core | 8 tasks per core | 16 tasks per core |
|---------------------|----------------------|------------------|-------------------|
| Charm++             | 9.8                  | 37.8             | 84.1              |
| HPX distributed     | 19.3                 | 39.2             | 54.1              |
| HPX local           | 22.4                 | 54.5             | 77.9              |
| MPI                 | 3.9                  | 6.1              | 7.6               |
| OpenMP              | 36.2                 | 36.9             | 41.8              |
| MPI+OpenMP          | 50.9                 | 152.5            | 258.6             |

(a) Stencil pattern, overdecomposition 8 (8 tasks per core).

(b) Stencil pattern, overdecomposition 16 (16 tasks per core).

Figure 2: METG of each system with varying number of nodes for different overdecomposition. METG is short for Minimum Effective Task Granularity, is an efficiency-constrained metric for runtime-limited performance, introduced in Task Bench paper [8].

Figure 1a presents the TeraFLOP/s reached with a compute-bound kernel, varying the grain size. Note that the time for each vertex to execute such a kernel with a grain size of one is 2.5 ns. Almost all systems achieve peak Tera FLOP/s, i.e. $2.44 \times 10^{12}$, when the grain size is large enough. Figure 1b shows the efficiency of each system responding to the peak Tera FLOP/s vs. task granularity. Task granularity is measured by: wall time $\times$ number of cores / number of tasks. Figure 1 shows METG of each system, which is the intersection of its efficiency curve and the 50% efficiency red dashed line in Figure 1. To calculate METG, we first measure the peak Tera FLOP/s and get the efficiency percentage of each system responding to the peak Tera FLOP/s. For more details about METG, we refer to [8]. For the shared-memory system, i.e. OpenMP and HPX local, we observe that HPX local performs better than OpenMP. For the distributed-memory system, we find that MPI has the smallest METG, 3.9 µs. METGs of other systems for this scenario are listed in the first column of Table 2.

6.2 Performance of overdecomposition

To quantify the performance of overlapping communication with computation, the total size of tasks is set to $N$ times the number of total cores, such that each core processes $N$ tasks. In this subsection, $N$ is set to 8 and 16, respectively.

Table 2 lists METGs of each system for the stencil pattern with/without overdecomposition, using one node, respectively. For all systems, MPI achieves the smallest METG for these three scenarios.

Figure 2 presents METGs of each system with varying number of nodes. Lower is better because a lower METG indicates a smaller task granularity required to achieve at least 50% overall efficiency. Flat is ideal because a flat line implies that the communication topology does not affect METG by increasing the number of nodes. We observe that Charm++ and MPI have lower and flat trends, while HPX distributed and MPI+OpenMP have higher and rising tendencies. For shared-memory parallelism, OpenMP has smaller METGs than HPX local for both scenarios.
6.3 Fine-grained Charm++ performance

In Figure 3, we evaluate the performance impact of the different build options meant for fine-grained applications described in Section 5.1, which were not used in the above experiments. Default is the standard Charm++ build used above. Char. Priority denotes a build using eight-byte message priorities; SHMEM denotes the build that uses shared-memory for intra-node communication. Combined is a build using all optimizations, and Simple Sched. denotes Charm++ built with the simplified scheduling path described in Section 5.1.

We find that SHMEM and Combined yield an average throughput increase of 5.7% and 5.3%, respectively. Using eight-byte message priorities and a simplified scheduling path did not yield a significant increase in throughput. Consequently, we find that scheduling overhead is not substantial even at this grain size, and that communication latency dominates. To further explore the performance impact of scheduling, additional investigation with different Task Bench dependency patterns is required.

7 Conclusion and outlook

This work is the first work comparing Charm++ and HPX using the same benchmark. Using Task Bench enabled us to study the overheads introduced by the two AMTs compared to the more traditional approaches. The asynchronous scheduling using light-weight threads as in HPX or stackless tasks as in Charm++ incurred some costs. We see, for larger grain sizes, the overhead was negligible. However, for smaller grain sizes, the overhead was observed. To conclude, the overheads of fine-grained parallelism were not inherent to the programming models, and benchmark studies like this one were expected to lead to further optimizations to reduce or eliminate the gap with respect to MPI.

This study has shown that there is potential for improvement for both AMTs for smaller grain sizes. Here, we need to investigate the differences with respect to MPI and do some profiling with the tools provided by both AMTs. For distributed HPX, we plan to try different libraries for communication, e.g. libfabric and LCI. For Charm++, the support for active messaging in the communication layer (such as UCX) will be tested. As a next step, a comparison with other AMTs would be interesting.

References

[1] J. Davison de St. Germain et al., “Uintah: a massively parallel problem solving environment,” in Proceedings the Ninth International Symposium on High-Performance Distributed Computing, 2000, pp. 33–41.
[2] B. Chamberlain et al., “Parallel programmability and the chapel language,” *International Journal of High Performance Computing Applications*, vol. 21, pp. 291–312, 08 2007.

[3] M. Bauer et al., “Legion: Expressing locality and independence with logical regions,” in *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis*, 2012, pp. 1–11.

[4] G. Bosilca et al., “Parsec: Exploiting heterogeneity to enhance scalability,” *Computing in Science Engineering*, vol. 15, no. 6, pp. 36–45, 2013.

[5] P. Thoman et al., “A taxonomy of task-based parallel programming technologies for high-performance computing,” *The Journal of Supercomputing*, vol. 74, no. 4, pp. 1422–1434, 2018.

[6] B. Acun et al., “Parallel programming with migratable objects: Charm++ in practice,” in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, 2014.

[7] H. Kaiser et al., “Hpx—the c++ standard library for parallelism and concurrency,” *Journal of Open Source Software*, vol. 5, no. 53, p. 2352, 2020.

[8] E. Slaughter, W. Wu, Y. Fu, L. Brandenburg, N. Garcia, W. Kautz, E. Marx, K. S. Morris, Q. Cao, G. Bosilca, S. Mirchandaney, W. Lee, S. Treichler, P. McCormick, and A. Aiken, “Task bench: A parameterized benchmark for evaluating parallel runtime performance,” in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*. IEEE, 2020.

[9] M. Rocklin, “Dask: Parallel computation with blocked algorithms and task scheduling,” 01 2015, pp. 126–132.

[10] A. Duran et al., “Ompss: a proposal for programming heterogeneous multi-core architectures.” *Parallel Processing Letters*, vol. 21, pp. 173–193, 06 2011.

[11] S. Treichler et al., “Realm: An event-based low-level runtime for distributed memory architectures,” *Conference Proceedings, PACT*, 08 2014.

[12] E. Slaughter et al., “Regent: a high-productivity programming language for hpc with logical regions,” 11 2015, pp. 1–12.

[13] M. Zaharia et al., “Spark: Cluster computing with working sets,” in *Proceedings of the 2nd USENIX Conference on Hot Topics in Cloud Computing*. USA: USENIX, 2010, p. 10.

[14] C. Augonnet et al., “Starpu: A unified platform for task scheduling on heterogeneous multicore architectures,” in *Euro-Par 2009 Parallel Processing*, H. Sips, D. Epema, and H.-X. Lin, Eds. Berlin, Heidelberg: Springer, 2009, pp. 863–874.

[15] J. M. Wozniak et al., “Swift/t: Large-scale application composition via distributed-memory dataflow processing,” in 2013 13th IEEE/ACM International Symposium on Cluster, Cloud, and Grid Computing, 2013, pp. 95–102.

[16] M. Abadi et al., “Tensorflow: Large-scale machine learning on heterogeneous distributed systems,” 2016.

[17] P. Charles et al., “X10: An object-oriented approach to non-uniform cluster computing,” in *Proceedings of the 20th Annual ACM SIGPLAN Conference on Object-Oriented Programming, Systems, Languages, and Applications*. New York, NY, USA: ACM, 2005, p. 519–538.

[18] I. Karlin et al., “Exploring Traditional and Emerging Parallel Programming Models Using a Proxy Application,” in *2013 IEEE 27th IPDPS*, May 2013, pp. 919–932.

[19] ——, “Lulesh programming model and performance ports overview,” Tech. Rep. LLNL-TR-608824, December 2012.

[20] F. Rabbi et al., “Evaluation of Directive-Based GPU Programming Models on a Block Eigensolver with Consideration of Large Sparse Matrices,” in *Accelerator Programming Using Directives*, ser. LNCS, S. Wienke and S. Bhalachandra, Eds. Cham: Springer, 2020, pp. 66–88.

[21] L. Dagum and R. Menon, “Openmp: an industry standard api for shared-memory programming,” *Computational Science & Engineering, IEEE*, vol. 5, no. 1, pp. 46–55, 1998.

[22] S. Wienke et al., “Openacc — first experiences with real-world applications,” in *Euro-Par 2012 Parallel Processing*, C. Kaklamanis, T. Papatheodorou, and P. G. Spirakis, Eds. Berlin, Heidelberg: Springer, 2012, pp. 859–870.

[23] R. F. Van der Wijngaart and T. G. Mattson, “The Parallel Research Kernels,” in 2014 *HPEC*, Sep. 2014, pp. 1–6.

[24] R. F. Van Der Wijngaart et al., “Using the Parallel Research Kernels to Study PGAS Models,” in 2015 9th *International Conference on Partitioned Global Address Space Programming Models*, Sep. 2015, pp. 76–81.

[25] R. F. Van der Wijngaart et al., “A New Parallel Research Kernel to Expand Research on Dynamic Load-Balancing Capabilities,” in *High Performance Computing*, ser. LNCS, J. M. Kunkel, R. Yokota, P. Balaji, and D. Keyes, Eds. Cham: Springer, 2017, pp. 256–274.
[26] R. Wijngaart et al., “Comparing Runtime Systems with Exascale Ambitions Using the Parallel Research Kernels,” in High Performance Computing, ser. LNCS. Cham: Springer, 2016, pp. 321–339.

[27] E. Raut et al., “Porting and Evaluation of a Distributed Task-driven Stencil-based Application,” in Proceedings of the 12th International Workshop on Programming Models and Applications for Multicores and Manycores. Virtual Event Republic of Korea: ACM, Feb. 2021, pp. 21–30.

[28] M. Bauer et al., “Legion: Expressing locality and independence with logical regions,” in Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis. Washington, DC, USA: IEEE, 2012.

[29] Z. Fink et al., “Performance evaluation of python parallel programming models: Charm4py and mpi4py,” in 2021 IEEE/ACM 6th ESPM2, 2021.

[30] G. M. Baker et al., “ASC ATDM Level 2 Milestone# 5325: Asynchronous Many-Task Runtime System Analysis and Assessment for Next Generation Platforms.” Sandia National Lab, Tech. Rep., 2015.

[31] H. Kaiser et al., “Hpx: An advanced parallel execution model for scaling-impaired applications,” Los angeles, USA, 2009, pp. 394–401.

[32] P. Diehl et al., “An asynchronous and task-based implementation of peridynamics utilizing hpx—the c++ standard library for parallelism and concurrency,” SN Applied Sciences, vol. 2, no. 12, pp. 1–21, 2020.

[33] D. C. Marcello et al., “octo-tiger: a new, 3D hydrodynamic code for stellar mergers that uses hpx parallelization,” Monthly Notices of the Royal Astronomical Society, vol. 504, no. 4, pp. 5345–5382, 2021.

[34] E. Slaughter et al., “Task Bench: A Parameterized Benchmark for Evaluating Parallel Runtime Performance,” arXiv:1908.05790 [cs], Nov. 2020.

[35] M. Dominiak et al., “P2300r4 std::execution (draft proposal),” 2022. [Online]. Available: http://www.open-std.org/jtc1/sc22/wg21/docs/papers/2022/p2300r4.html