A Low-Power Accelerator for Deep Neural Networks with Enlarged Near-Zero Sparsity

Yuxiang Huan, Student Member, IEEE, Yifan Qin, Yantian You, Lirong Zheng, Senior Member, IEEE, and Zhuo Zou, Member, IEEE

Abstract—It remains a challenge to run Deep Learning in devices with stringent power budget in the Internet-of-Things. This paper presents a low-power accelerator for processing Deep Neural Networks in the embedded devices. The power reduction is realized by avoiding multiplications of near-zero valued data. The near-zero approximation and a dedicated Near-Zero Approximation Unit (NZAU) are proposed to predict and skip the near-zero multiplications under certain thresholds. Compared with skipping zero-valued computations, our design achieves 1.92X and 1.51X further reduction of the total multiplications in LeNet-5 and Alexnet respectively, with negligible lose of accuracy. In the proposed accelerator, 256 multipliers are grouped into 16 independent Processing Lanes (PL) to support up to 16 neuron activations simultaneously. With the help of data pre-processing and buffering in each PL, multipliers can be clock-gated in most of the time even the data is excessively streaming in. Designed and simulated in UMC 65 nm process, the accelerator operating at 500 MHz is > 4X faster than the mobile GPU Tegra K1 in processing the fully-connected layer FC8 of Alexnet, while consuming 717X less energy.

Index Terms—Deep Neural Network, energy-efficient learning, Internet-of-Things, near-zero approximation, sparse data

I. INTRODUCTION

It is an inevitable trend that trillions of devices with sensing and processing capabilities will be connected to form the Internet-of-Things (IoT). Beyond today’s IoT systems that are based on Radio Frequency Identifications (RFIDs) and Wireless sensor networks (WSNs), recent advances in low power design and artificial intelligence help to shift the functionalities of devices from sensing to perception. This paradigm shift requires ubiquitously embedded nodes to be capable of extracting features or patterns from sensed raw data, so as to enable intelligent perception of the surrounding world. The emergence of Deep Neural Network (DNN) models make it feasible, as they exhibit superior performance over traditional approaches in learning of data. Due to the complexity of the DNNs, they require high performance platforms, like CPU, GPU [1], [2], or FPGA [3], [4], and thus are usually run on high performance servers or clusters. Rather than sending raw data to the cloud, local processing on-device is more preferred in terms of security, communication overhead, and delay. It is beneficial that DNN models can be optimized to fit in resource-constrained IoT devices [5].

To meet the requirements of IoT devices, complex DNN models should be processed in a more compact manner as most of them are heavily over-parameterized. ReLU activation [6] and network pruning [7] are thus widely used to simplify the inference of the DNN, enlarging the sparsity of the neural input data and the weights in most of DNN layers. Computation of sparse data can be omitted, as it contributes negligible efforts to the final results but occupies the limited processing resources. Existing platforms, such as CPU, DSP, or GPU, are inefficient to run the sparse model due to the weak support for sparse data detection and skipping. In addition, they suffer from high energy consumption and cost, which doesn’t meet power and cost constraints of IoT devices. Specialized designs have been implemented to avoid the multiplications of the sparse data [8], [9], [10], yet the sparsity is only restricted to zero-valued data.

This paper extends the zero-valued sparsity to near-zero-valued sparsity, in order to avoid complex multiplications of near-zero valued data through approximation. A corresponding Near-zero Approximation Unit (NZAU) is proposed to predict and skip near-zero multiplications under certain thresholds. Based on the NZAU, a low-power accelerator with 256 multipliers is designed for energy-efficient processing of DNNs. By adjusting the threshold of the NZAU, the design achieves a 1.92X and 1.48X further reduction of the total multiplications than zero-skipping in LeNet-5 [11] and Alexnet [6], respectively. With the help of data pre-processing and buffering in each Processing Lane, the multipliers can be clock-gated in most of the time with no stall in processing. Implemented in UMC 65 nm process, the accelerator operating at 500MHz is > 4X faster than the mobile GPU Tegra K1 in processing the fully-connected layer FC8 of Alexnet [6], while consuming 717X less energy.

The remainder of this paper is organized as follows. Section II gives the mechanism of near-zero approximation. Section III describes the implementation details of the proposed accelerator. The near-zero approximation and the performance and energy consumption of the accelerator are evaluated and discussed in Section IV. Finally, conclusions are drawn in Section V.

II. APPROXIMATION MECHANISM

As a key part of the Deep Neural Network, matrix-vector multiplications are commonly used to compute the activation
of a neuron. The activation usually follows the (1) (biases are omitted here).

$$y_i = ReLU \left( \sum_{j=0}^{N} (W_{i,j} \cdot x_j) \right)$$

(1)

Existence of sparsity in both the weight matrix $W$ and the input vector $x$ implies opportunities of optimizing the complex matrix-vector multiplication. As depicted in Fig. 1, the sparsity of the input vector may result from the original input data or the activation by ReLU, while the weight matrix becomes sparse if the network pruning is used.

A. Near-Zero-valued Sparsity

Though skipping multiplications of the sparse data brings benefits for improving energy efficiency, the sparsity is only restricted to zero-valued data. Due to the resilience nature of the neural network, small error is tolerable during the inference of the network. It is possible to discard the multiplications whose results are so small that cause little effect on the final results. As indicated by (2), (3), (4) and (5), the computation of (1) can therefore be divided into three parts:

$$y_i = ReLU \left( P1 + P2 + P3 \right) \approx ReLU \left( P1 \right)$$

(2)

$$P1 = \sum_{j \in \{W_{i,j} \cdot x_j, \neq 0\}} (W_{i,j} \cdot x_j)$$

(3)

$$P2 = \sum_{j \in \{W_{i,j} \cdot x_j = 0\}} (W_{i,j} \cdot x_j)$$

(4)

$$P3 = \sum_{j \in \{W_{i,j} \cdot x_j = 0\}} (W_{i,j} \cdot x_j)$$

(5)

$P1$ refers to the part of multiplications that result in none-zero values; $P2$ refers to the part of multiplications that result in zero value and can be bypassed through zero-skipping techniques; $P3$ refers to the part of multiplications that can be approximated to zero if constrained by a certain threshold. As both of the $P2$ and the $P3$ are discarded if a proper threshold is used, data involved in the $P3$ can be regarded as "sparse". To distinguish the sparsity that only covers the zero-valued data, we extend the sparsity to include the portion of multiplications in $P3$ and define new sparsity as near-zero-valued sparsity (NZ-sparsity). Therefore, large scale matrix-vector multiplications can be further optimized if near-zero multiplications are effectively handled.

B. Near-Zero Approximation

For a given threshold of a multiplication, value ranges of the two operands are dynamic. There are no restrictions directly applied to the operands. Therefore, constraining the result of the multiplication is more beneficial than constraining the operands, as the first one allows wider value ranges of the operands. In this case, the result of a multiplication should be predicted without doing the complex floating-point or fixed-point computation. Hence, we devise an approach to predict and approximate the result of a multiplication based on detecting the most significant bits of the operands.

The most significant bit of the data is a good indicator for its relative value, which can be determined through leading zero detection. Assuming that there are two N-bit operands, which have the leading zero counts as $l_A$ and $l_B$ correspondingly. Binary numbers that have the same leading zero count as $l_A$ or $l_B$ lie in the ranges indicated as:

$$2^{N-l_A-1} \leq A < 2^{N-l_A}, 2^{N-l_B-1} \leq B < 2^{N-l_B}$$

(6)

When multiplying the two operands, the result is then expressed as:

$$2^{2N-(l_A+l_B)-2} \leq A \cdot B < 2^{2N-(l_A+l_B)}$$

(7)

If applying the function of leading zero counting (denoted as $f_l()$) to (7), it can be re-written as:

$$f_l(2^{2N-(l_A+l_B)}) < f_l(A \cdot B) \leq f_l(2^{2N-(l_A+l_B)-2})$$

(8)

It can be further inferred as:

$$l_A + l_B - 1 < f_l(A \cdot B) \leq l_A + l_B + 1$$

(9)

It can be found that the leading zeros of the result is either $l_A + l_B$ or $l_A + l_B + 1$. In other words, the total leading zeros of the two operands can determine the relative value of the result. Based on this, constraining the results can be turned into constraining the total leading zeros of the operands.
Fig. 2. Architecture of the proposed accelerator: the Near-Zero Approximation Unit pre-processes the excessive streaming data, while the 16 Processing Lanes are responsible for buffering and computation of the operands that can not be skipped.

(a) The Near-Zero Approximation Unit that pre-processes 16 multiplications simultaneously
(b) Architecture of the Processing Lane: both of the buffering circuits and the computational units are clock-gated, and the operands registers isolate the computational units from the local buffers, halting the processing when assembling the operands.

Fig. 3. Key building blocks of the proposed accelerator (denoted as _ltotal_). If _ltotal_ is larger than the given threshold, the operands will be discarded and the multiplication result will be approximated to 0. Otherwise, these operands will be kept for further multiplication.

The effectiveness of such near-zero approximation has been preliminarily examined in a handcrafted Neural Network in our previous work [12]. In this work, we apply the approximation mechanism to two more complex models: LeNet-5 and Alexnet. Comparing with skipping zero-valued multiplications, this mechanism further reduces of the total multiplications of the two models by 1.92X and 1.51X respectively with negligible lose of accuracy. Detailed discussion and evaluation will be given in Section III.

III. HARDWARE IMPLEMENTATION

As most of the existing platforms, such as CPU or GPU, are inefficient to perform the proposed near-zero approximation, an low-power accelerator for matrix-vector multiplications is implemented with dedicated support of the proposed approximation mechanism.

The architecture of the accelerator is illustrated in Fig. 2. This accelerator adopts a SIMD-like architecture to enable efficient parallel operations of the data. The computational units of the accelerator are consisting of 256 multipliers and 16 adder trees. To minimize the overhead of memory operation and data delivery, the computational units and the local buffers are grouped into 16 Processing Lanes (PL), and each PL is capable of handling one neuron’s activation. A Near-Zero Approximation Unit (NZAU) is designed and integrated as a pre-processing unit, reducing the near-zero multiplications under a specified threshold. The threshold can be adjusted to match a specific model, as the data input and the parameters of the model may affect the tolerance of error. A optimal threshold can be determined by increasing it gradually while keeping the error rate of the model, and thus maximum NZ-Sparsity can be achieved. With the NZAU and local buffers, the implemented accelerator can perform near-zero sparse matrix-vector multiplications without the involvement of computational units in most of the time.

A. Near-Zero Approximation Unit (NZAU)

The Near-Zero Approximation Unit is implemented to support the aforementioned mechanism of approximation. To detect the leading zeros of the operands, 16-bit Leading-Zero-Counting (LZC) units are employed in the design. This LZC unit adopts a shared-carry propagate architecture and features small area and high energy efficiency [13], thus reducing the overhead of NZAU.

The block diagram of the NZAU is given in Fig. 3a. Two 16-bit fixed point operands are first transferred to absolute values and then fed to Leading Zero Counting (LZC) units to calculate the leading zeros. After that, the leading zero counts are summed up and compared with a 5-bit threshold, which is adjustable to control the constraint of the near-zero approximation. If the total leading zeros exceed the threshold value, the corresponding multiplication is approximated to 0, and the operands are discarded. Otherwise, the approximation is not acceptable, and the operands will be passed to a PL.
designed to store the 16-bit input data sub-words and assemble them into a 256-bit full data word. When the data buffering is enabled, the operand registers save the data word, isolating the data buffering from computation.

In Fig. 4a, an example of matrix-vector multiplication with near-zero sparsity is given for illustration. In every cycle, one column of 16 weights and one neuron input are fetched from the two memories. The red boxes indicate the multiplications that need to be performed, while other multiplications are discarded due to the near-zero approximation. Operands that are stored in the data buffers of PL1 are shown in Fig. 4b. The first 8 cycles contain only 3 multiplications that need processing, so only in cycle 1, 5 and 8, the corresponding pair of operands are loaded to the buffer. After n cycles, the buffers are filled with 16 operands, then the 256-bit data word is flushed out and registered for computation. Thanks to the adjustable threshold, the near-zero sparsity can be enlarged to decrease the duty cycle of computational units. Therefore, the computational units can be clock-gated in most of the time, leading to significant reduction of the energy consumption.

IV. EVALUATIONS

A. Validation of Near-Zero Approximation

To validate the effectiveness of the proposed near-zero approximation, we apply the near-zero approximation to two classical Convolutional Neural Networks: LeNet-5 and Alexnet, as they are more typical to represent the real case. Various threshold values are employed to alter the NZ-Sparsity...
so as to test the models’ error rate under different approximation levels.

The experimental results of LeNet-5 is illustrated in Fig. 5 due to dense image data in Cifar-10, the first two layers have a relatively small sparsity lower than 25% since they are close to the original data. However, as the layer goes deeper, the sparsity increases dramatically. It is mainly because that ReLU activation has an accumulating effect of producing zero-valued data. In other words, the zero-valued data produced by ReLU activation in the previous layer tend to result in more zero-valued data in current layer. Though the model has a zero-valued sparsity of 29.40%, it can be further enlarged by applying the proposed near-zero approximation. When the model is constraint by the threshold of $2^{-1}$, the NZ-Sparisty of the whole model can reach 63.35% with only 0.58% increase of the error rate. Compared with zero-valued sparsity, the near-zero approximation reduces total number of multiplications by 1.92X. Similar results are found in testing the Alexnet, as shown in Fig. 6. The sparsity of Alexnet can be enlarged from 45.9% to 64.1% with negligible loss of accuracy, corresponding to 1.51X reduction of the total multiplications.

B. Evaluation of the accelerator

The proposed accelerator was synthesized in UMC 65nm Low Leakage Process by Synopsys Design Compiler. Switching activity of processing the Alexnet-FC8 layer was annotated in Synopsys Prime Power to estimate the power consumption of the accelerator. Operating at 500 MHz, the entire accelerator consumes 59 mW without optimization of sparse data at 500 MHz, and the number drops to 38 mW when the zero-skipping is used. When the near-zero approximation is applied without sacrificing the accuracy, the power consumption is reduced to 31 mW, corresponding to 18.4% further improvement. Table I summaries this work and compares with other existing mainstream platforms. It can be seen that the proposed accelerator is > 2X and > 4X faster than the high performance CPU for PC and the mobile GPU when processing the last fully-connected layer of Alexnet. Considering the total energy of executing the task, our accelerator exhibits 717X energy reduction than mobile GPU Tegra K1.

V. Conclusion

There exists a large sparsity in the Deep Neural Network model, which can be utilized to optimize the DNN for IoT devices. But the sparsity is only restricted to zero-valued data. In this work, we extend the zero-valued sparsity to near-zero valued sparsity (NZ-Sparisty) and proposed a near-zero approximation technique to reduce the near-zero multiplications in learning models. Dedicated hardware of the approximation scheme, named Near-Zero Approximation Unit, is designed and integrated in the accelerator for energy-efficient processing of DNNs.Evaluated in the UMC 65nm process, the 500 MHz accelerator is > 4X faster than the mobile GPU Tegra K1 in processing the fully-connected layer FC8 of Alexnet, while consuming 717X less energy.

TABLE I

| Platform          | Type   | Technology | Frequency (MHz) | Power (W) | Processing Time Alex-FC8 (us) | Processing Energy Alex-FC8 (μJ) |
|-------------------|--------|------------|-----------------|----------|-----------------------------|---------------------------------|
| Core-i7 5930k [9] | CPU    | 22nm       | 3500            | 73        | 1134.9                      | 82847.7                          |
| GeForce Titan X [9] | GPU    | 28nm       | 1075            | 159       | 80.5                        | 12799.5                          |
| Tegra K1 [9]      | mGPU   | 28nm       | 852             | 5.1       | 2252.1                      | 11485.71                         |

This work

No multiplications skipped
Zero skipping
Near-zero approximation

ASIC
65nm
500
0.059
0.038
0.031
516
19.6
16

REFERENCES

[1] Z. Chen and et al., “A fast deep learning system using gpu,” in 2014 IEEE International Symposium on Circuits and Systems (ISCAS), June 2014, pp. 1552–1555.
[2] A. Coates and et al., “Deep learning with cots hpc systems,” in Proceedings of the 30th International Conference on Machine Learning (ICML-13), May 2013, pp. 1337–1345.
[3] Chakradhar and et al., “A dynamically configurable coprocessor for convolutional neural networks,” in Proceedings of the 37th Annual International Symposium on Computer Architecture, ser. ISCA ’10, New York, NY, USA, 2010, pp. 247–257.
[4] V. Gokhale and et al., “A 240 g-ops/s mobile coprocessor for deep neural networks,” in 2014 IEEE Conference on Computer Vision and Pattern Recognition Workshops, June 2014, pp. 696–701.
[5] S. Venkataraman and et al., “Efficient embedded learning for iot devices,” in 2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC), Jan 2016, pp. 308–311.
[6] A. Krizhevsky and et al., “Imagenet classification with deep convolutional neural networks,” in Advances in neural information processing systems, 2012, pp. 1097–1105.
[7] S. Han and et al., “Learning both weights and connections for efficient neural network,” in Advances in Neural Information Processing Systems, 2015, pp. 1135–1143.
[8] Y. H. Chen and et al., “Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” in 2016 IEEE International Solid-State Circuits Conference (ISSCC), Jan 2016, pp. 262–263.
[9] S. Han and et al., “Eie: Efficient inference engine on compressed deep neural network,” in 2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA), June 2016, pp. 243–254.
[10] B. Moons and M. Verhelst, “A 0.3-2.6 tops/w precision-scalable processor for real-time large-scale convnets,” in 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), June 2016, pp. 1–2.
[11] Y. LeCun and et al., “Gradient-based learning applied to document recognition,” Proceedings of the IEEE, vol. 86, no. 11, pp. 2278–2324, 1998.
[12] Y. Huang and et al., “A multiplication reduction technique with near-zero approximation for embedded learning in iot devices,” in 2016 29th IEEE International System-on-Chip Conference (SOCC), Sept 2016.
[13] G. Dimitrakopoulos and et al., “Low-power leading-zero counting and anticipation logic for high-speed floating point units,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 7, pp. 837–850, July 2008.