Fabrication and Structural Characterization of Co-implanted Ultra Shallow Junctions for Integration in Piezoresistive Silicon Sensors Compatible with CMOS Processing

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Abstract. Fabrication and structural characterization of Indium and Carbon implanted n-type Silicon layers forming ultra-shallow junction for integration in piezoresistive sensors compatible with CMOS processing is studied in detail. The co-implantation technology together with medium range annealing temperature regimes seem to play an important role at atomistic level and provide a process control to engineer the strain and maintain the quality of surface/layer/active device region for further manufacturing process cycle. This is likely to impact the yield and reliability for the fabrication of these devices for diverse applications.

1. Introduction

Piezoresistors are commonly used in accelerometers, pressure sensors and different kinds of sensor arrays. These devices have also emerged as the industry’s choice while manufacturing the Scanning Probe Microscopy (SPM) and Atomic Force Microscopy (AFM) systems. The manufacturing industry of these systems utilizes the piezoresistors to sense the deflection in cantilevers [1-4]. A commercial piezoresistor consists of doped (diffused or ion-implanted) silicon which in comparison to rest of the materials exhibits remarkable and optimized response characteristics [5-6]. Realization of large area and fast high resolution imaging is incomplete without a sensible integration between various components of microsystem (piezoresistive sensors, actuators, CMOS processing compatible cantilever, etc.). The creation of various doped layers, regions with tailored physical properties, engineered surfaces, stable interfaces and ultra-shallow junctions are extremely important to realize such Microsystems, particularly the ultra-thin and fully integrated piezoresistive sensors.

It is important to ascertain the maintainability of the material properties of the junction after a certain process recipe employed in fabricating the Ultra Shallow Junctions for CMOS nano-electronics [7, 8, 9]. The processing protocol to examine the formation and subsequent electrical characterization of under study co-implanted Si layers (doping concentration, sheet resistance, mobility and junction depth) is already reported in depth [9]. In order to fully optimize the test process and fabrication strategy, a controlled behavior of tailored films and surfaces on atomistic level is required to ascertain process yield and manufacturing cost. X-rays (in various forms such as XRD, XRF, X-rays scattering measurements etc.) are widely used in semiconductor manufacturing industry to examine, evaluate, and analyze the surfaces, interfaces, thin films and device regions. XRD, in particular, has emerged as standard diagnostic technique for structural investigation in ion implantation technology particularly to study the stress, strain and distortion created in the ion implanted layers due to the creation of point defects and/or extended defects in the crystal. Some End-of-Range (EOR) defects may reportedly be responsible for the clustering of silicon interstitials in this region where indium dopant profile dominates in the Si matrix [7, 10, 11].
the similar fashion, diffusion of carbon into silicon has also been reported to act as an effective sink for silicon interstitials [12, 13, 14, and 15]. XRD studies of Si-layers with Indium and Carbon co-implantation with pre-defined post-implant annealing schedules were also carried out with a reported recovery of Si lattice constant to its original value by post-implant annealing cycles (600°C-1050°C) [10]. Further, the reduction in strain with increasing indium dose corresponding to a reduction in the dopant deactivation was also reported in detail [16]. The aim of this paper is to present the findings on the reliability (in terms of quality of the processed material for direct utility in Si-based piezoresistors and consequent integration with rest of the processes to achieve a total device solution) using structural techniques with special reference to the surface roughness and structural morphology. Such strain engineering in nanoscale materials, surfaces and devices as well as quantum structures is applied as an important and powerful process strategy to develop improved functionalities and high performance devices [17, 18, and 19].

2. Experimental Conditions, Design and Details

Detailed experimental design is elaborated in one of the previously published work [9]. The important experimental parameters are tabulated below (Table 1). The implant parameters in this work (Also; previously used to form junctions reported in references 8 and 9) are purposely chosen to be similar or close to those studied earlier [7 and their relevant work] in order to check the reliability of the physical process as well utilize their complimentary analysis to improve the process’s functionality requirements.

**Table 1:** Co-implantation Assisted USJ Formation in Silicon: Design & Fabrication Parameters

| Process/Fabrication Step                              | Parameters                                                          |
|-------------------------------------------------------|---------------------------------------------------------------------|
| Selection/Growth of Starting Material                 | Commercially grown, CZ n-type Si wafers of (100) orientation with initial resistivity between, 4-7 Ω/square |
| Activation-specific Pre-amorphization Implantation    | Si at an energy of ~500eV and a fluence of ~5×10^{15} at/cm²         |
| Junction Formation: Ion Implantation                  | Ion: Indium (In⁺); Dose: 5.7×10^{14} at/cm²; Implant Angles: 8° tilt and 24° twist; Energy: 70 keV |
| Junction Formation: Co-Implantation                   | Ion: Carbon (C⁺); Dose: 3.4×10^{15} at/cm²; Implant Angles: 8° tilt and 24° twist; Energy: 10keV |
| Cleaving                                              | squares of 1-1.5cm² sizes                                           |
| Dopant Activation via Rapid Thermal Processing        | Rapid Thermal Annealing (RTA) between 600 and 800°C for 60s dwell and carefully designed ramp-up time |

Atomic Force Microscopy and XRD facilities were used to image the extent of surface roughness (structural morphology) and scan the diffraction data revealing the structural changes due to ion irradiation of the as-implanted and annealed Si layers. The machine parameters are summarized in Table 2.

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Table 2: Process Control and Precision Check by Structural and Imaging Techniques: Parameters

| Technique                  | Measurement Parameters                                                                                                                                 |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| X-ray Diffraction         | Rotating anode X-ray diffractometer (Philips X’pert); CuKα radiation of wavelength 0.154 nm                                                                 |
| Atomic Force Microscopy   | AFM Agilent system 2500 picoscan; Maximum Scan Rate: 48 lines/sec at 256x256; 100μm with large scanner and atomic resolution with small scanner          |

3. Results, Analysis and Discussion

The 2θ diffraction scans of as-implanted samples of co-implanted Si layers were taken to identify the structure and phase. The assignment of signal peaks at ~33° and 39° was made to Indium (111) and (110) diffractions, respectively. Similarly, the peaks observed at ~43° and 44.5° were assigned to Carbon (100) and (101) respectively. The XRD spectra shown in figure 1 exhibits the presence of C, In and Si atoms in n-type Si matrix. While looking at the spectra carefully, one notices that the as-implanted samples (un-annealed) have relatively a maximum intensity at ~69.13° assigned to Si (400). Further, the effect of post-implant annealing on co-implanted layers is obvious when samples are annealed at \( T_{\text{anneal}} = 600°C \). A sharp peak appears as a little hump with a change in the extent of relative intensity of In (110). This may be a signature of the physical process being activated on atomistic level suggesting an increase electrical activation efficiency of indium atoms at 600°C, hence a lowering intensity of Si (400) as compared to un-annealed cases. We know from a previously reported study \[2\] that the junction depth increases in the devices under discussion in the temperature ranging from 600°C to 700°C. This increase in junction depth may be attributed to the movement of indium atoms back to their original positions \[20\]. Interestingly, a slightly different behaviour of physical processing at atomistic level is observed when we anneal the samples further at 750°C. The signature of this process emerges in the form of increase in lattice strain and hence the junction depth decreases \[20\]. The breaking of C-In complexes may be responsible for this structural activity. At 800°C, the ion-implantation-induced strain in the lattice seems to decrease. Ion related strain is known to be removed almost fully by high temperature annealing in Si. The implantation-induced strain in the lattice and activated indium atoms present near the substitutional lattice sites (and hence forming the C-In acceptor centers) and their subsequent physical behavior while undergoing the post-implant annealing schedules play an important role in making the doped Si layers either relaxed or strained directly impacting the fabrication yield and efficiency of piezoresistors integrated with the Microsystems. There are certain evidences that the vacancies also interact with substitutional Indium atoms to relax the strain field duly introduced by the relatively larger covalent radius of In ~0.144 nm compared to that of Si ~0.11 nm \[20\]. Also, it has also been observed that the dopants (indium and carbon in this case) in Si may be responsible to make the lattice contracted or expanded depending on the host-impurity covalent bond radii \[16\]. Our results summarized in figure 2 also augment these findings where strain caused due to co-implantation in Si layers vary with increasing annealing temperature and consequently impact the depth of the junction formed.
Figure 1. XRD Spectrum of In and C co-implanted Si layers undergone a rapid thermal annealing process at temperature regime 600-800°C. (a) as-implanted (b) annealed at 600°C (c) annealed at 650°C (Spectra obtained for other annealing temperatures are not shown here due to space limitations. The key features/trend, however, are summarized in figure 4)

Surface morphology of a material/layer/thin film is an important structural parameter to assess the quality and utility of any fabrication process undergoing a full-device cycle. At present, the most promising approach to study an in-depth morphology is Atomic Force Microscopy. Surface representing a non-Gaussian distribution and an exponential autocorrelation function may be examined by Atomic Force Microscopy. An output measurement parameter RMS (the root mean square of the vertical deviations from the reference) is connected with the distribution’s probability density function, and serves as a quick evaluation tool to analyze the pre-and post-processed surface morphologies [21].

RMS roughness tends to increase with the increasing post-implant annealing temperature as exhibited in figure 3. Figure 3 demonstrates the topographical view of the In and C co-implanted Si layers before annealing reflecting the extent of roughness and uniformity of the irradiated surface. The presence of impurity concentration at different depths is also visible as background structural information. This three dimensional view shows negligible degradation of the morphology of the surface after the devised and processed implant strategy. Positioning of thermal flux due to annealing considerably reduces damages (refer to Figure 4) and is crucial to study the consequent damage re-engineering in Si-based devices, particularly in thin/ultra-thin doped/damaged layers (utilized in the fabrication of piezoresistors), shallow/ultra-shallow junctions (utilized in source or drain engineering for Si-CMOS manufacturing as well as integration with piezoresistors based Microsystems) and region definition for contact fabrication. Figure 4 shows the variation of RMS as a function of annealing temperatures for ion implanted Si layers. The values reported do averages of six different measurements at different locations (regions of the surface) of the sample, clearly reflecting a trend owe the changes on the atomistic level analogous to the finding and discussion on XRD measurements.
Figure 2. Variation of % change in Strain obtained from XRD as a result of In and C co-implantation in n-type Si layer with respect to annealing temperature ranging from 600°C to 800°C. Junction depth obtained on these samples by various complimentary techniques reported previously [8,9] are also plotted to correlate the results.

Figure 3. Representative Atomic Force Microscopic (AFM) topographical view of the In and C co-implanted Si layers (un-annealed): Extent of roughness and uniformity of the implanted indium and carbon co-implants. This three dimensional viewgraph shows negligible degradation of the morphology of the surface after the devised and processed implant strategy for effective utilization in the formation and integration of piezoresistive sensors and CMOS ultra-shallow junction.
Figure 4. Variation of surface roughness amplitude parameter as a function of post-implant annealing temperature for co-implanted silicon layers

4. Conclusion

In summary, we studied the thermal effects on structural and morphological properties of the layers engineered by co-implantation technology in Si to provide a controlled, reliable, repeatable and easy-to-drive process to fabricate ultra-thin piezoresistors and ultra-shallow junctions for CMOS compatible fully integrated systems. This study suggests that a careful design of implant-annealing processes may provide a useful process control directly impacting the physical activity at atomistic level such as defect clustering, defect migration and annihilation, movement of dopant atoms within the atom distribution profiles, and surface roughness, lattice relaxation and strain duly controllable by the residual thermal flux during the annealing process.

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