Dataplant: Enhancing System Security with Low-Cost In-DRAM Value Generation Primitives

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Abstract—DRAM manufacturers have been prioritizing memory capacity, yield, and bandwidth for years, while trying to keep the design complexity as simple as possible. DRAM chips are passive elements that store data, but they do not carry out any computation or other important function in the system, such as security. Processors implement and execute most of the existing security mechanisms that protect the system against security threats, because 1) executing security mechanisms usually require non-trivial computational capabilities (e.g., encryption), and 2) commodity DRAM chips are not designed to perform computations or tasks other than data storage.

In this work, we advocate for DRAM as a key component for providing security mechanisms to the system. To this end, we propose Dataplant, a new class of low-cost, high-performance, and reliable security primitives that can be integrated in commodity DRAM chips with minimal changes. The main idea of Dataplant is to slightly modify the internal DRAM timing signals to expose the inherent process variation found in all DRAM chips for generating unpredictable but reproducible values (e.g., keys) within DRAM, without affecting regular DRAM operation.

We use Dataplant to build two new security mechanisms. First, a new Dataplant-based physical unclonable function (PUF) with non-destructive read-out, low evaluation latency, robust responses, resiliency to temperature changes, and data-independent responses. Second, a new cold boot attack prevention mechanism based on Dataplant that automatically destroys all data within DRAM on every power cycle with zero run-time energy and latency overheads. These mechanisms can be integrated with current DDR memory chips without changing the DRAM array.

Using a combination of detailed simulations and experiments with 136 real commodity DRAM chips, we show that our Dataplant-based PUF has 1.8x higher throughput than the best state-of-the-art DRAM PUFs while being more resilient to temperature changes, and totally independent of the values stored in memory. We also demonstrate that our Dataplant-based cold boot attack protection mechanism is 19.5x faster and consumes 2.54x less energy when compared to existing mechanisms.

1. Introduction

Modern processors have security support for encryption and memory isolation [1] that protects secret data in memory from attackers. Unfortunately, these mechanisms cause significant performance and energy overheads [2] and introduce new vulnerabilities [3], [4]. Although DRAM is a key component of many systems that often store critical or secret information, there is no hardware security support implemented in commodity chips that accelerates or enhances security.

We make a case for incorporating security primitives in commodity DRAM chips based on three fundamental observations. First, DRAM is ubiquitous in computer systems today, from high-end servers to low-cost Internet of Things (IoT) devices [5]. Therefore, millions of users can benefit from having simple and low-cost security primitives in DRAM (e.g., easy to adopt by the industry). Second, critical data usually resides in main memory, and it is usually replicated across the processor caches. This introduces new sources for potential security breaches that make the system vulnerable to attacks (e.g., cache side channels). To reduce this security risks, one solution is to minimize data replication across the system and process critical data close to where it resides (e.g., memory). Third, the data movement throughout the memory hierarchy causes energy, performance and bandwidth overheads [6].

Our goal is to develop low-cost primitives in commodity DRAM chips for supporting commonly-used security mechanisms. To this end, we propose Dataplant, a novel low-cost, high-performance, and reliable class of in-DRAM security primitives. The key idea of Dataplant is to take advantage of inherent DRAM behavior to generate unpredictable values, which can be used to support several system-level security mechanisms. This work is the first to propose security primitives that are simple enough so that can be integrated with existing commodity DRAM chips. Our primitives are variants of existing DRAM commands (e.g., activation) that only require minimal timing changes to certain internal DRAM signals. Therefore, Dataplant primitives require no changes to the DRAM array. We propose two Dataplant primitives that complement each other: 1) US-Dataplant generates values in the DRAM Sense Amplifiers (SAs), and 2) UC-Dataplant generates values in the DRAM cells.

US-Dataplant and UC-Dataplant enable the implementation of security mechanisms efficiently in DRAM. We analyze and evaluate two such security mechanisms in this work: (1) physical unclonable functions (PUFs) [7]–[19] and (2) cold boot attack prevention [20]–[23].

1. Physical Unclonable Functions (PUFs). PUFs are usually used in cryptography to identify devices or to create authentication keys. The main advantage of DRAM-based PUFs is that DRAM is ubiquitous in many computer systems today. However, existing DRAM PUFs have at least one of these four main issues. First, most DRAM PUFs have destructive read out (e.g., they destroy the memory content). Second, most DRAM PUFs have a latency that is very high to be used at runtime without system interference. Third, most DRAM PUFs are very noisy, so they require a filtering mechanism to calculate the PUF responses. Fourth, most of the DRAM PUFs provide responses that highly depend on temperature, which can affect the reliability of the generated keys. Avoiding this issue requires extra engineering effort (e.g., maintaining the DRAM at a constant temperature, or making the sys-
2. Background

2.1. DRAM

We provide background on the DRAM architecture relevant to this work. We describe the organization of a DRAM chip, the architecture of its sense amplifiers and the operations that are performed on a DRAM chip.

DRAM Organization DRAM chips are manufactured in a variety of configurations [43], including a range of capacities and data bus widths ranging between 4 and 16 pins. Since an individual DRAM chip has a small capacity and a limited data width, multiple DRAM chips are usually grouped together in the same DRAM module to form a rank, providing a larger data bus (usually 64-bits wide). Specialized DRAM for IoT can have fewer chips and a narrower bus [5], [30], [31].

Each DRAM chip consists of multiple banks, and each bank contains multiple 2D arrays (or subarrays) of DRAM cells as shown in Figure 1. The cells are stacked in rows of 4 or 8 KB that share a wordline. Each cell consists of a capacitor which stores the data in form of charge, and an access transistor controlled by the wordline that connects the cell to the Sense Amplifier through the bitline.

DRAM Sense Amplifier (SA) The Sense Amplifiers (SAs) are used for sensing and amplifying the small charge of the cell capacitor to a CMOS-readable value. A set of SAs connected to a row of cells is called row buffer. Figure 1 shows how a cell is connected to a SA via a bitline. The actions related to the functioning of the SA can be summarized into three steps. First, to be able to sense the cell’s charge, the SA sets the bitline to the precharge level \((V_{dd}/2)\). Second, the cell (at \(V_{dd}\) or 0V) shares its charge with the bitline, which produces a small change in the voltage of the bitline \((V_{dd}/2 \pm \delta)\). Third, the SA is activated and it amplifies the delta of the bitline voltage towards the original value of the cell.

DRAM Operation The memory controller issues three basic commands as part of a DRAM read or write operation: 1) the Activation (ACT) command senses and amplifies the data from the target row into the row buffer; 2) the read/write (RD/WR) command transfers data from/to the row buffer to/from the DRAM bus; 3) the Precharge (PRE) command clears the row buffer and prepares the subarray for subsequent read/write operations (precharges the bitlines).

Figure 2 details the steps for reading a DRAM cell. Initially, the bitline is precharged to \(V_{dd}/2\) with the wordline set to 0V. To access data from DRAM, the memory controller first issues an ACT command, which raises the voltage of the target wordline and connects the

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**Figure 1: DRAM organization, sense amplifier, and cell.**

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cells of that row to the bitline. This causes the deviation of the bitline voltage in one direction (charge sharing). As a result, the sense amplifier senses and amplifies this deviation (sensing phase). After reaching this phase, the memory controller can issue RD or WR commands. The time needed to finish the ACT command is specified by the timing parameter \( t_{RCD} \). The sense amplifier continues to amplify the deviation until the voltage of the cell is fully restored. After that, the controller issues a PRE command to lower the wordline voltage back to 0V and drive the sense amplifier and bitline to \( V_{dd/2} \). The time needed to complete a PRE command is specified by the timing parameter \( t_{RP} \). Once precharged, the subarray is ready for the next access.

![Figure 2: DRAM Activation (ACT), Read (RD) and Precharge (PRE) commands.](image)

### 3. Overview of DATAPLANT

Dataplant is a new class of low-cost in-DRAM primitive that enables high-performance implementations of security mechanisms via generating unpredictable yet reproducible values in DRAM. We propose two variants of Dataplant, which enable a 1) new class of high-performance and robust PUF, and 2) a new cold boot attack prevention mechanism that does not incur performance and energy overheads at runtime.

#### 3.1. Dataplant Primitives

**US-Dataplant** (Unpredictable Values in the DRAM SAs) generates unpredictable values in a DRAM SA by exploiting process variation inherent in DRAM SAs. We implement US-Dataplant by simply altering the timing of two DRAM signals during a standard activation operation. The generated values can be read by the processor from the SAs without overwriting the data in DRAM, or they can be optionally stored in DRAM.

**UC-Dataplant** (Unpredictable Values in the DRAM Cells) generates an unpredictable value in a DRAM cell by exploiting process variation inherent in DRAM cells. We implement UC-Dataplant by altering the timing of only one DRAM signal during a standard precharge operation. UC-Dataplant requires two steps. First, UC-Dataplant sets a DRAM cell to the precharge voltage. Second, when the cell is next activated, the cell assumes an unpredictable value based on process variation. Unlike US-Dataplant, UC-Dataplant requires overwriting the original content of the cell for generating a value.

The Dataplant primitives are very similar to DRAM activation and precharge commands. This makes our approach easy to integrate into commodity DRAM chips, and facilitates its adoption by industry and standards bodies.

Section 4 describes the circuit-level implementation details of the two primitives, and Section 7.1 evaluates their latency, energy, and area. We also propose a new Dataplant implementation that generates **deterministic** values by introducing an additional transistor in the SA. Appendix A describes and evaluates this implementation.

### 3.2. Implementing Security Mechanism Using Dataplant Primitives

To demonstrate the potential of Dataplant, we use UC-Dataplant and US-Dataplant to implement new approaches of two common security mechanisms.

**Dataplant PUFs.** We propose two new Dataplant DRAM PUFs (based on US-Dataplant and UC-Dataplant) that have four unique characteristics. First, the US-Dataplant-based PUF does not have a destructive read out. Second, the latency of Dataplant PUFs is very low (i.e., the same as a precharge or activation latency), which makes Dataplant suitable for runtime access. Third, Dataplant PUF responses are not as noisy as other state-of-the-art DRAM PUFs, which results in more stable PUF responses. Fourth, Dataplant PUF responses are very stable across a wide range of temperatures.

**Preventing Cold Boot Attacks.** Although DRAM memory is volatile, the stored data does not immediately disappear at power-off. Data can be naturally retained in DRAM cells up to minutes after a power-off [33], which enables cold boot attacks [20]–[23], [32], [33] (i.e., the data can be read as soon as the device is powered back up). We propose a mechanism completely implemented in DRAM chips (i.e., it does not require external DRAM commands) that destroys all the data in DRAM by automatically issuing Dataplant primitives when the chip is powered up. Unlike prior mechanisms to prevent cold boot attacks [34]–[39], our Dataplant-based mechanism protects against even a computationally unbounded adversary, as it makes brute-force attacks impossible. Our mechanism requires no changes aside from the existence of the Dataplant primitives, incurs no latency or energy overhead at runtime as it operates only at power-up, and is secure because it is an automatic mechanism self-contained in DRAM.

Section 5 and Section 6 discuss the implementation of these mechanisms in detail. Additionally, Appendix B describes and evaluates secure deallocation, an additional security mechanism that can be implemented with Dataplant.

### 4. Dataplant Implementation

This section shows the implementation details of two Dataplant variants that have different features. To illustrate how they operate, we use a detailed SPICE model to simulate the SA, cell, bitline and wordline. We implement the SA using 55nm DDR3 model parameters [44] and PTM low-power transistor models [45], [46]. We use cell/transistor parameters from the Rambus power model [44] (cell capacitance = 22fF; transistor width/height = 55nm/85nm).
For reference, Figure 3a shows the simulation of a standard DRAM activation command. As explained in Section 2.1, a standard activation command 1) raises the voltage of the wordline \((V_{WL})\) to connect the cell to the bitline, which causes a deviation in the bitline voltage, and 2) triggers the SA \((V_{SA})\) for sensing this bitline voltage variation and restoring the charge of the cell towards its original value.

### 4.1. US-Dataplant Primitive

US-Dataplant generates unpredictable values by exploiting mainly SA process variation. The value generated by US-Dataplant has little influence from the process variation of other components (e.g., bitline). The key idea is to trigger the SA \textit{without} raising the voltage of the wordline, i.e., the cell doesn’t deviate the voltage of the bitline. By doing so, the SA amplifies the bitline voltage towards an unpredictable value that 1) doesn’t depend on the charge of the cell, and 2) depends on the SA process variation. Once the SA drives the bitline towards the final generated unpredictable value, US-Dataplant can optionally write this value into the cell by raising the wordline voltage.

Figure 3b shows how US-Dataplant generates a value (including the optional overwriting of the cell). The dashed lines and the arrow \((\rightarrow)\) highlight that, when writing to the cell (optional), US-Dataplant raises the voltage of the wordline always after triggering the SA logic. US-Dataplant triggers the SA \((V_{SA})\) \(1\) when the bitline \((V_{BL0})\) is precharged (i.e., \(V_{dd}/2 = 0.5V\) \(2\)), and the SA drives the bitline towards a value (0V in the figure) that depends on process variation \(3\). At this point, the memory controller can issue a read command to get the generated value from the SA. After generating the value, US-Dataplant can optionally write the generated value in the DRAM cell by raising the voltage of the wordline \((V_{WL})\) \(4\), which overwrites the content of the cell with the generated value \((V_{Cell})\) \(5\). Notice that the voltage of the wordline must be raised after triggering the SA \((\rightarrow)\).

To illustrate the effects of process variation in the values generated by US-Dataplant, we perform SPICE simulations for five instances of a common SA design (details in Section 7.1) with small changes in their physical characteristics that simulate process variation. Figure 4 shows the generated values for five SAs examples with different process variation values depending on the voltage of the bitline. US-Dataplant always amplifies a bitline with \(V_{dd}/2\) voltage (precharge voltage) to generate a value. We observe that the generated value for \(V_{dd}/2\) bitline voltage depends on the SA’s process variation: SAs with variation \(-\delta, 0 +\delta\) an \(+2\delta\) generate a zero value, while \(-2\delta\) generates a one value. These process variation at fabrication time cannot be controlled or cloned, and their layout is unpredictable and unique for each device.

### 4.2. UC-Dataplant Primitive

UC-Dataplant generates unpredictable values by exploiting mainly DRAM cell process variation. The value generated by UC-Dataplant has little influence from the process variation of other components (e.g., bitline, wordline, SA). They key idea is to set the cell to the same voltage as the bitline precharge voltage \((V_{dd}/2)\) by triggering the precharge logic and raising the wordline voltage at the same time. In the next activation, raising the voltage of the wordline doesn’t disturb the bitline voltage (because the cell has the same \(V_{dd}/2\) voltage as the bitline), and the SA amplifies towards an unpredictable value. The anomalies and perturbations introduced by the cell process variation [47] are the main factors that determine the unpredictability of the generated value.

Figure 3c shows how UC-Dataplant sets the cell to \(V_{dd}/2\) voltage. The dashed lines and the arrow \((\uparrow)\) are
for highlighting that UC-Dataplant activates the precharge logic instead of the SA logic. The wordline voltage ($V_{WL}$) is raised at the same time as the precharge logic is triggered ($V_{\text{precharge}}$), which drives the cell ($V_{\text{cell}}$) towards $V_{dd}/2$. Our SPICE simulations show that UC-Dataplant consumes the same power independently of the initial value of the cell (as the final value is always $V_{dd}/2$).

Section 7.2.2 evaluates the feasibility of UC-Dataplant by emulating the values it generates on real DRAM chips.

### 4.3. Hybrid-Dataplant Primitive

We propose a low-cost Hybrid-Dataplant primitive that 1) implements US-Dataplant and UC-Dataplant into the same DRAM module, and 2) provides a mechanism to select the Dataplant implementation at runtime.

Different applications might require different characteristics that a single implementation cannot provide. Our two Dataplant implementations have three main trade-offs. First, UC-Dataplant relies on destroying the previous content of the cell for generating data, while US-Dataplant can generate data in the SA with or without destroying the DRAM content. Second, UC-Dataplant executes faster than US-Dataplant, but it requires an additional activation command to generate the unpredictable value. US-Dataplant, however, can generate and access the data with only one command. Third, UC-Dataplant value generation relies on the DRAM cell process variation, which are orders of magnitude smaller than the SA. Consequently, UC-Dataplant is potentially more sensitive to technology scaling effects.

Hybrid-Dataplant primitive enables to choose the primitive that better fits the requirements of the application. Hybrid-Dataplant implements US-Dataplant and UC-Dataplant together with low hardware overhead by leveraging one free bit in the in-DRAM mode registers (MR) to encode the implementation to use, and the load mode register (LMR) command to change the implementation to use at runtime. In commodity DDR4 modules, the MR3 register has 13 unused bits that enable to select the Dataplant primitive independently in 13 different DRAM partitions (e.g., in different DRAM banks).

### 4.4. Security and Reliability

In this section we discuss the security and reliability of US-Dataplant and UC-Dataplant primitives.

**Security.** US-Dataplant does not leak any information about the previous content of the cell because it generates values that are independent of the cell content (Figure 3). UC-Dataplant, as described in Section 4.2, first discharges the DRAM cells in a row, and it then activates the sense amplifiers. If an attacker manages to interfere between these two steps, they could try to bias the cells towards some particular value before the amplification (e.g., row hammer [49]). However, these two steps are executed back-to-back in a few nanoseconds, which is not enough time to induce any row hammering [49] or similar attacks that require milliseconds to succeed [50], [51].

**Reliability.** We observe that the main reliability issue related to DRAM is associated with the reduction of the amount of charge that can be stored in a DRAM cell, which can make the sensing phase unreliable [48], [52]. SAs are in general more resilient to reliability issues [48], [53] because they are three orders of magnitude larger than DRAM cells [44]. Based on these observations, we make two conclusions. First, we do not expect major reliability issues on US-Dataplant as it does not use the cells for generating values. Second, although UC-Dataplant uses the DRAM cells for generating values, UC-Dataplant does not have a sensing phase because the cell is set to $V_{dd}/2$ voltage. Therefore, we expect the reliability of a US/UC-Dataplant primitive to be higher than the reliability of a regular activation/precharge.

### 4.5. Hardware Cost

The hardware cost of implementing Dataplant in DRAM is very low. Incorporating our new Dataplant primitives require very few modifications in the control logic that generates the control signals. The changes are limited to add a few extra logic gates to delay the wordline signal in a regular activation (US-Dataplant), and to trigger the access transistor and the precharge logic at the same time (UC-Dataplant). To the best of our knowledge, there is no public information about how vendors implement the control logic, or what is the specific circuit design of that logic (see Appendix C). The hardware cost of our primitives is very low in any case, because our mechanism can reuse most of the logic for generating the activation and precharge timing signals.

### 5. Dataplant PUFs

A PUF is a hardware primitive that maps a set of challenges to a set of static random responses that are derived from the physical characteristics of an integrated circuit (e.g., process variation). A PUF can be used as a building block for implementing low-cost authentication protocols [54]–[57] and key generation applications [7], [9], [10].

One or more parameters (e.g., the address of a memory segment, temperature, etc.) define a challenge, and the data read from DRAM is the response to that challenge. Together, they define a Challenge-Response pair (CR pair). In this work, we use the address of the segment as the only parameter that defines a challenge.

**Limitations of State-of-the-art DRAM PUFs.** Prior DRAM-based PUF proposals exploit variations in DRAM start-up values [24], DRAM write access latencies [25], DRAM cell retention failures [26], [28], [58] and reduced DRAM timing parameters [29], [40]. There are five main limitations with most of these approaches. First, most of these PUFs rely on the charge that is contained in DRAM cells, thus all the content of the memory region employed for the PUF is irreversibly overwritten. Using these PUFs requires either 1) exclusive memory regions for PUFs or 2) copying and restoring the original contents for each PUF challenge request. Second, most DRAM PUFs [29] have high evaluation time, which can potentially cause system interference when the PUF is accessed at runtime. Third, many of these PUFs require heavy
filtering mechanisms to deal with the inherent noisy nature of the DRAM responses, which increases the evaluation latency and the reliability of the responses. Fourth, the responses to the same challenge suffer great variations with temperature changes, which is an issue in systems with a non-controlled environment (e.g., IoT devices in the wild). Fifth, some DRAM PUFs are data dependent, which might cause mismatching responses that depend on the content of the memory. Our Hybrid-Dataplant PUFs overcome all of these five limitations.

**US-Dataplant PUF.** US-Dataplant PUF has six key distinctive properties. First, US-Dataplant PUF does not require destroying the current memory content, because it does not need to assert the wordline to generate a response. Second, US-Dataplant PUF responses do not depend on the actual content of the cell, because the charge of the cell shared and amplified. Third, US-Dataplant PUF can be evaluated with a latency as low as the latency of a regular activation. Fourth, a US-Dataplant PUF response is less noisy than most state-of-the-art DRAM PUFs, which enables lighter filtering mechanisms and reduced latency. Fifth, US-Dataplant PUF is particularly robust because SAs are much less sensitive to environmental conditions, interference from other elements, and scaling issues [49]. Sixth, the downside of US-Dataplant PUF is that it has a small CR pair space that is limited by the number row buffers in DRAM (~8MB in a 4GB DRAM).

**UC-Dataplant PUF.** UC-Dataplant PUF has six distinctive properties. First, UC-Dataplant has a CR pair space as large as the DRAM capacity, because it uses DRAM cells to generate responses. Second, the evaluation latency of UC-Dataplant PUF is as low as the latency of a precharge operation. Third, UC-Dataplant PUF is more reliable under temperature variations than the state-of-the-art solutions, as we demonstrate in our evaluation (Section 7.1). Fourth, UC-Dataplant PUF requires an additional activation to read out the PUF response. Fifth, UC-Dataplant PUF is more sensitive to scaling issues than US-Dataplant PUF, because the generated responses depend mainly on the DRAM cells. Sixth, UC-Dataplant PUF necessarily destroys the current memory content.

**Hybrid-Dataplant PUF.** To get the best properties of our two Dataplant PUFs, we can easily implement US-Dataplant PUF and UC-Dataplant PUF in the same DRAM module with minimal hardware overhead. The application can choose, according to its requirements, the PUF to use (US-Dataplant or UC-Dataplant) by configuring the MRs accordingly (see Section 4.4).

**System-Level Support for Accessing Dataplant PUFs.** There are at least two ways of enabling software access to Dataplant PUFs, either by adding a new instruction to the instruction set architecture for reading the PUF response [59], [60], or by using a dedicated address range to map the PUF operations to regular load instructions.

On the DRAM side, there are two implementation options. First, adding a new mode that provides the US-Dataplant and UC-Dataplant functionalities instead of the regular activation and precharge commands. The mode can be selected by changing dedicated MRs (see Section 4.4). Second, introducing a new command in the DDR specification. The new command has the same general requirements as a regular activation (US-Dataplant) or as a regular precharge (UC-Dataplant). We can integrate the new command in the JEDEC standard specification [43] without extra cost, as there is unused, reserved space as part of the standard for new commands.

**Security Analysis** Dataplant PUFs are more secure, less noisy, and more stable with temperature changes than state-of-the-art DRAM PUFs. The Dataplant PUF responses responses pass all the NIST randomness tests. Note that all DRAM PUFs have a CR pair space that is limited by the DRAM capacity. Security applications that use DRAM PUFs as a building block have to engineer the security mechanism carefully to avoid, for example, that an attacker with physical access to the device characterizes the entire device and compromise its security.

### 6. Preventing Cold Boot Attacks

This section shows how Dataplant enables an efficient and simple mechanism to prevent cold boot attacks. Cold boot attacks [20]–[23] are possible because the data stored in DRAM is not immediately lost when the chip is powered-off. This is due to the capacitive nature of DRAM cells that can hold their data up to some seconds [33]. This reminiscent effect can be even more significant if the DRAM module is cooled down. Taking advantage of this property, an attacker can either take the victim’s DRAM module off and place it in a system under their control with minimal information loss, or boot a small special purpose program from a cold reset to recover the secret information.

#### 6.1. State-of-the-Art Defenses

There are three classes of mechanisms for preventing cold boot attacks. First, mechanisms that rely on encrypting memory either explicitly [20], [34]–[39], [61], or implicitly through some CPU extensions (e.g., Intel SGX [1]). These mechanisms are effective and secure, but are too complex and expensive (in terms of energy and performance overhead) to be implemented in many low-cost devices. Second, modern systems scramble the data in the memory controllers, which helps to obscure the DRAM contents. This mechanism is simple and is also required for other purposes (e.g., improve signal integrity in the DRAM bus), but it has been shown to be insecure against cold boot attacks [20]. Third, the mechanism proposed by the Trusted Computing Group (TCG) [62] to reset the DRAM content upon power-off (or power-on if the last power-off was not clean). This mechanism is implemented on the host platform firmware and depend on the OS, which makes it vulnerable to attacks [63].

#### 6.2. Threat Model

We tackle an attacker that gains physical access to a live uncompromised machine/device for an unlimited amount of time and whose goal is to obtain some information stored in the device’s DRAM. Note that, for any interesting information to be present in DRAM the attacker
should get the memory while it is still powered-on. We then assume that, as part of the attack, the DRAM chip is powered-off for an arbitrarily short amount of time. This power loss occurs when transplanting the DRAM module to an attacker-controlled machine and during attacks that reboot the victim machine to load a malicious OS. Note that some computers allow warm reboots, in which the power is not cut off. Our cold boot attack prevention mechanism is not compatible with those systems.

We are not aware of alternative methods to power-on the DRAM, other than using the corresponding DRAM PINs. Therefore, until a technique that can attach a stable external power supply (while the chip is already powered on) to the DRAM chip is engineered, transplanting a chip from one machine to another would inevitably involve a power loss. However, even if this is possible, we speculate that it would require expensive specialized equipment, significantly increasing the cost of an otherwise cheap attack.

In summary, to the best of our knowledge, transplanting the DRAM and rebooting to a different OS are the only ways to perform a cold boot attack today, and both involve a power loss. In particular, we are not aware of any other techniques that allow measuring the charge in the DRAM capacitors, including x-ray techniques.

6.3. Destroying Data at Power-On

We make the observation that it is possible to protect from cold boot attacks by deleting all memory contents during the DRAM power-on. Based on this observation, we propose two new cold boot attack prevention mechanisms. First, Self-destruction, a low-cost in-DRAM mechanism based on Dataplant that destroys all the DRAM content without the intervention of the memory controller. Second, Command-based Destruction, a low-cost mechanism orchestrated by the memory controller that allows a more flexible implementation at the cost of providing weaker security guarantees.

6.3.1. Self-destruction. The key idea of Self-destruction is to refresh the whole DRAM memory in self-refresh (SR) mode at power-on, but using Dataplant primitives instead of activation commands. This way, the DRAM chip executes a destructive DRAM refresh that can be performed autonomously without the intervention of the memory controller.

The basic principle of a DRAM refresh is to perform an activation and a precharge command to the row to be refreshed. As we show in Section 4, US-Dataplant is very similar to an activation command, and UC-Dataplant is very similar to a precharge command, which allows to easily incorporate them in the refresh operations, leveraging the circuitry that launches regular SR cycles. With Self-destruction, the data is destroyed in a complete SR window, i.e., 64ms (32ms for LPDDR). During the destructive SR, the DRAM does not allow any memory commands to ensure the atomicity of the process.

Self-destruction in a Burst refresh. Burst refresh is a refresh mode that is available on Low-power DDRn (LPDDRn) devices. The main idea of the burst refresh is to complete all the required refreshes in a single burst, with the goal of meeting the deadlines of real-time applications. Our Self-destruction mechanism is also compatible with this refresh mode that allows destroying data much quicker (e.g., 9ms for a 4GB DDR4 memory module).

Security Analysis. Our mechanism is automatically triggered in DRAM when power is detected, without requiring external actions. Therefore, the security of Self-destruction depends on the reliability of the power-on detection circuit of the DRAM module. There are two ways in which an attacker can potentially bypass this circuit. We describe both ways and explain why, in practice, they do not pose a security threat.

First, an attacker could operate DRAM at low voltage on the compromised system using, for instance, Dynamic Voltage and Frequency Scaling (DVFS), with the goal of not triggering the power-on detection circuit. The power-on circuit triggers when it detects a voltage ramp up from 0V, but it does not need to reach \(V_{DD}\) (it triggers as long as a voltage ramp up starting from 0V is detected). Therefore, operating the DRAM at very low voltage would not help the attacker.

Second, an attacker could fry the DRAM power-on detection mechanism. In practice, however, the FSM that initializes the chip is in the same internal controller that regulates other functions (i.e., timing signals for activate, precharge, and other commands). Consequently, frying that component would most likely make the whole DRAM unusable.

Hardware Cost Analysis. The hardware cost of implementing our Self-destruction mechanism in DRAM is very low. The implementation of Dataplant has very low overhead (Section 4.4), and the logic to trigger a self-refresh window at DRAM power-on is negligible. Triggering Dataplant instead of regular activations in the refresh process requires minimal modifications on the in-DRAM control logic (see Section 4.5).

6.3.2. Command-Based Destruction. The key idea of Command-Based Destruction is to force DRAM to obey a particular sequence of commands issued from the memory controller that leads to the destruction of the whole memory content during the initialization procedure. The mechanism can be implemented with regular write commands, with Rowclone [59], with Lisa-clone [60] or with our new Dataplant primitives.

The Command-Based Destruction relaxes the security guarantees since it is conducted by the memory controller. An attacker could easily bypass this procedure by using a customized memory controller or a programmable one [64]. To solve this issue, we add a mechanism in DRAM that ensures the execution of the appropriate sequence of commands in the initialization procedure. The mechanism uses a latch that indicates when the DRAM is performing the initialization and, during this phase, the DRAM chip filters out any other command. Implementing this mechanism requires adding a new FSM in
DRAM, which adds hardware and energy overhead to the existing circuitry. Also, a DRAM module that implements Command-Based Destruction can operate only with compatible memory controllers (i.e., no backward compatible).

**Security Analysis.** Compared to Self-destruction, Command-based Destruction has weaker security guarantees, because it is not self-contained in-DRAM, and it does not destroy the memory contents automatically in-DRAM at power-on. Nevertheless, it is very challenging to bypass the DRAM FSM that disables read commands until the memory is destroyed by the memory controller. Compared to TCG (Section 6.1), Command-based Destruction provides better security guarantees, as our mechanism does not provide any software interface to control the DRAM initialization mechanism.

**Hardware Cost Analysis.**

Self-destruction does not require modifications in the memory controller, and it requires minimal changes in the DRAM logic that controls the signals to issue Dataplant commands instead of regular activation and precharge commands.

Compared to Self-destruction, Command-based Destruction is more complex to integrate into current systems. It requires the modification of the memory controller, and it requires the addition of dedicated DRAM logic to ensure the integrity and atomicity of the destruction protocol.

Command-based destruction issues Rowclone/Lisa/Dataplant requests from the memory controller. Similar to the PUF mechanism (Section 5), there are two options to issue these requests. First, adding a new DRAM command to the DDR JEDEC standard specification [43] by leveraging the unused and reserved bits available in the standard protocol. Second, adding new logic in the in-DRAM command decoder that decodes existing commands (e.g., activation, precharge) into Rowclone/Lisa/Dataplant commands depending on some new configuration bits in the SR registers (similar to Section 4.4).

7. Evaluations

We evaluate the Dataplant primitives (Section 7.1), the Dataplant DRAM PUFs (Section 7.2) and our cold boot attack prevention mechanism (Section 7.3).

7.1. Dataplant: Latency, Energy, and Area

**Methodology.** In this section we study the latency and energy overhead of Dataplant primitives for generating and overwriting values in a single DRAM row. We compare our Dataplant primitives to the state-of-the-art mechanisms for copying data within DRAM, namely Lisa-clone [60] and Rowclone [59]. Rowclone and Lisa-clone propose in-DRAM methods to initialize data to zero by copying a reserved row filled with zeros to the destination row. Both solutions modify the internal architecture of DRAM and slightly reduce the DRAM’s capacity since they need helper data to work. We compare Dataplant primitive against Rowclone and Lisa-clone because there are no other works that generate data within DRAM in the same way Dataplant does.

We estimate the latency of US-Dataplant, UC-Dataplant, Rowclone and Lisa assuming DDR3 timing constraints. We calculate their energy consumption by using the activation and precharge energy consumption described in the power model of the DRAMPower simulator [65].

**Latency and Energy Results.** Table 1 shows the absolute value and the reduction of latency and energy of the evaluated techniques, when generating a value in a 8 KB DRAM row. We also show the in-DRAM latency and energy consumption of standard activation and precharge commands. The baseline generates data by overwriting the memory contents with regular write commands from the memory controller. We make three major observations. First, the latency and energy consumption of our two Dataplant primitives are significantly reduced compared to the baseline, Lisa-clone and Rowclone. Second, UC-Dataplant is significantly faster than US-Dataplant, mainly because it avoids the activation of the SA. However, the UC-Dataplant numbers on the table do not include the additional activation command needed read the values out of DRAM (see Section 4.2). Third, the latency and energy consumption of US-Dataplant/UC-Dataplant is the same as a standard activation/precharge command.

**Table 1:** Latency and energy of different in-DRAM primitives for overwriting 8KB of data, and standard activation and precharge commands.

| Primitive   | Lat. (ns) | Ener. (nJ) | Lat. | Ener. |
|-------------|-----------|------------|------|-------|
| Baseline    | 546       | 2000       | 1.0x | 1.0x  |
| Lisa-clone  | 148.5     | 90         | 3.67x| 22.2x |
| Rowclone    | 90        | 50         | 6.06x| 41.5x |
| Activation  | 35        | 17.3       | 15.6x| 116x  |
| Precharge   | 13        | 17.2       | 42x  | 116x  |
| US-Dplant   | 35        | 17.3 + 7.3 + 10 | 15.6x| 116x  |
| UC-Dplant   | 13        | 17.2       | 42x  | 116x  |

Table 1 also shows the Dataplant energy breakdown (value generation + overwriting). The energy consumption is very close on the two Dataplant implementations because of two main reasons. First, the two implementations need to route the address within DRAM, which is one of the main sources of energy consumption (around 40%). Second, the energy consumption of the sense amplifier (used in US-Dataplant) and the precharge logic (used in UC-Dataplant) are similar (around 40%). Notice that overwriting in US-Dataplant is optional, hence they require only 7.3nJ and 8nJ respectively to generate an 8KB value, while in UC-Dataplant both processes are indivisible, requiring always 17.2nJ for generation-overwriting.

Our SPICE simulations show that the power demanded by US-Dataplant can vary up to 5% depending on the initial value contained on the cell.

**Area Overhead.** US-Dataplant and UC-Dataplant has negligible area overhead caused by the additional logic that controls the signal timings (more detail in Section 4.5). Lisa-clone has an area overhead of 1% caused by the additional isolation transistors, additional control logic, and one additional zero-filled row per bank. The overhead
of Rowclone (0.2%) is caused by the additional zero-filled row per subarray.

### 7.2. Evaluating the Quality of Dataplant PUFs

To evaluate US-Dataplant and UC-Dataplant PUFs, we reproduce the responses of US-Dataplant with SPICE simulations, and we reproduce the responses of UC-Dataplant in real DRAM chips with an FPGA-based infrastructure.

#### 7.2.1. Simulating US-Dataplant PUF with SPICE.
We evaluate US-Dataplant PUF with SPICE simulations. Unfortunately, it is unfeasible to conduct experiments on real DRAM chips, as US-Dataplant requires changes to the internal DRAM timings, which are hard-wired in commodity DRAM chips.

**Methodology.** To show the effects of process variation on the values generated by US-Dataplant, we evaluate a detailed SA SPICE model (see Section 4) using Monte Carlo simulations. We model variations in all the affected components of the SAs (transistor length/width/threshold voltage). Our SA model always generates ‘1’ bits in absence of process variation. When we introduce process variation into the simulation, we observe that some SAs generate ‘0’ bits as well (called unpredictable values). We run 100,000 simulations for each variation.

**Results.** Table 2 shows the percentage of SAs that generate unpredictable values for different levels of process variation and different temperatures.

| PV effects | Temperature effects (4% PV) |
|------------|------------------------------|
| Unpred.    | 2%  3%  4%  5%  30 C  60 C  70 C  85 C |
|            | 0%  0%  0.02% 0.19% 0.02% 0.19% 0.21% 0.15% |

We make two main observations. First, small process variations (<4%) are not enough to generate unpredictable values. Second, large process variations increase the unpredictability of the generated values. As the technology scales, process variation becomes more significant, which increases the unpredictability of the values generated by US-Dataplant PUF (i.e., it increases the PUF quality). Third, temperature changes do not cause significant variation in the unpredictability of the generated values.

#### 7.2.2. Evaluating UC-Dataplant PUF Responses in Real DRAM Chips.
We evaluate the quality of the UC-Dataplant PUF responses with a new methodology that allows us to recreate the functional behavior of the UC-Dataplant PUF without implementing it in real DRAM chips. Notice that it is not possible to implement UC-Dataplant PUF in commodity DRAM devices, because Dataplant requires changes to the internal DRAM timings. We perform an exhaustive evaluation using 136 real DRAM chips from 15 modules.

**Methodology.** An UC-Dataplant primitive 1) sets a cell to $V_{dd}/2$ with the precharge logic, and 2) activates the SA to generate an unpredictable value from that cell. As we don’t have the resources to make a real DRAM implementation, we emulate this behavior in real DRAM chips in two steps. First, based on the observation that a DRAM cell leak towards $V_{dd}/2$, we disable the DRAM refresh for 48 hours with the goal setting the cell to $V_{dd}/2$. Second, we activate this cell to obtain the PUF response. This methodology allows us to reproduce the responses that would produce a real UC-Dataplant PUF implementation. Recall that discharging the cells would take a few nanoseconds (not 48h) in a real implementation (Section 7.1). We perform our experiments with a customized memory controller built with SoftMC [64] and a Xilinx ML605 FPGA on 136 different DDR3 DRAM chips from three major vendors.

Table 3 shows the main characteristics of the 136 DRAM chips we use in our evaluation, including vendor, number of chips (#Chips), capacity of a chip (capacity/chip), frequency, and voltage.

**TABLE 3: Characteristics of the 136 DDR3 DRAM chips used in our evaluation.**

| Vendor | #Chips | capacity/chip | Frequency | Voltage  |
|--------|--------|---------------|-----------|----------|
| A      | 32     | 512MB         | 1600      | 1.35V (DDR3L) |
| A      | 32     | 512MB         | 1600      | 1.5V (DDR3) |
| B      | 32     | 256MB         | 1333      | 1.5V (DDR3) |
| B      | 8      | 512MB         | 1600      | 1.35V (DDR3L) |
| C      | 32     | 512MB         | 1600      | 1.35V (DDR3L) |

Emulating the UC-Dataplant PUF functional behavior with our methodology is challenging, because DRAM cells can retain their content for a long time [66], i.e., not refreshing the DRAM does not guarantee that a cell will be end up with the precharge voltage ($V_{dd}/2$), even after a long period.

To deal with this issue, we tailor a custom test to determine if a cell is set to the precharge voltage. As discussed in Sections 4.1 and 4.2, when a cell is set to the precharge voltage, the value that UC-Dataplant generates should be always the same regardless of the initial value of the cell. Based on this observation, our test analyzes the final value of a DRAM cell after 48 hours without refresh, in two different scenarios: 1) all initial values are zero and 2) all initial values are one. The test has two possible outcomes. First, the test passes if the final value is the same regardless of the initial value. Thus, we can conclude that the cell is set to the precharge voltage. In this case, the final value should be the one that a real UC-Dataplant implementation would generate. Second, the test fails if the final value is different. In that case, we cannot conclude that the cell is set to the precharge voltage (i.e., we cannot infer the value generated by UC-Dataplant), so we do not consider that cell in our results.

**Results.** Our experiments cover between 34% to 99% of all cells, which are the cells that end up with the precharge voltage using our methodology. The percentage of generated values that are unpredictable because of process variation is between 0.01% and 0.22%, which is in line with the results we obtained with our SPICE simulations. To measure the uniqueness and similarity of a PUF, we apply Jaccard indices [67] as suggested by prior works [29], [58], [68], [69]. We determine the uniqueness of the values generated by UC-Dataplant in Section 7.2.4.
Jaccard indices by taking two sets of unpredictable values \((u_1, u_2)\), i.e., two sets of PUF responses, from two memory segments, and calculating the ratio of their shared values over the full set of unique unpredictable values \(\frac{|u_1 \cap u_2|}{|u_1 \cup u_2|}\).

A ratio close to 1 represents high similarity, and a ratio close to 0 represents uniqueness.

We use the term Intra-Jaccard for representing the similarity of two sets from the same memory segment, and Inter-Jaccard for representing the uniqueness of two sets from different memory segments. An ideal PUF should have an Intra-Jaccard index close to 1 (a unique challenge has a unique response), and an Inter-Jaccard index close to 0 (different challenges have different and random responses).

We compute the distribution of Intra- and Inter-Jaccard indices obtained by running experiments on 136 different DRAM chips with segments of 8KB (this size is used by prior work [29]). We calculate the Intra-Jaccard indices for 10,000 random pairs of memory segments (each pair composed of two responses from the same memory segment), and the Inter-Jaccard indices for 10,000 random pairs of memory segments (each pair composed of two responses from different memory segments) from all DRAM chips.

We compare UC-Dataplant PUF with the DRAM latency PUF [29]. The DRAM Latency PUF accesses DRAM with reduced timing parameters, which causes some read failures that fulfill the requirements of a good PUF. We implement the DRAM Latency PUF by reducing \(t_{RCD}\) to 2.5ns, as it is the timing value that reports the best results in our setup. For improving the repeatability of the responses, the DRAM latency PUF implements a filtering mechanism that removes the cells with low failure probability from the PUF response. To this end, the mechanism reads the memory segment 100 times, and it composes a response that contains only the failures that repeat more than 90 times [29].

The values generated by UC-Dataplant are much less noisy than the values obtained by reducing the access latency, so UC-Dataplant PUF needs a much more lightweight filtering mechanism: we actually observe that one read is enough to get a robust UC-Dataplant PUF response in most cases, but we apply a conservative filter of 10 UC-Dataplant requests to obtain more robust PUF responses in worst case conditions. While a DRAM latency PUF with a lightweight filtering mechanism (e.g., 1-10 reads) could be as fast as Dataplant PUFs, the PUF quality would decrease significantly (Section 7.2.3), compromising the functionality and security of the PUF-based authentication protocol.

Figure 5 shows the Intra- and Inter-Jaccard indices of UC-Dataplant PUF and DRAM Latency PUF [29] for 64 DDR3 chips operating at 1.5V and 72 DDR3L chips operating at 1.35V.

We make four main observations. First, the UC-Dataplant PUF shows very good Intra-Jaccard indices (almost all indices are one), and pretty good Inter-Jaccard indices (the indices are distributed next to zero). Second, the DRAM latency PUF without filter has Intra-Jaccard indices distributed all over the spectrum (far from ideal), which does not satisfy the similarity property of a good quality PUF. This issue is solved by using the filtering mechanism, which biases the values of the Intra-Jaccard indices towards one, at the cost of increasing the evaluation time (Section 7.2.3). Third, the DRAM Latency PUF has very good Inter-Jaccard indices, very close to zero. Fourth, the results from DDR3L chips are better than those from DDR3 chips, for both the DRAM Latency PUF and the UC-Dataplant PUF. We conclude that the UC-Dataplant PUF is very effective on getting very similar responses to the same challenge, while maintaining uniqueness between responses from different memory segments.

Based on our results, a naive challenge-response authentication mechanism implemented with UC-Dataplant that correctly authenticates only when the response is exactly the expected (i.e., no filtering mechanism), has an average false rejection rate of 0.64% and an average false acceptance rate of 0%.

**Temperature and Aging Effects.** To demonstrate how temperature affects the similarity of different responses to the same challenge, we evaluate the UC-Dataplant PUF and the DRAM latency PUF under different temperatures, ranging from 30°C to 85°C. We use the experimental setup from the previous experiment, a DRAM heater, and a fine-grain temperature controller that can control the temperature with a precision of \(\pm 0.1\)°C. For this experiment, we only need to wait for 4 hours (instead of 48 hours), since cells discharge faster at high temperatures. Figure 6 shows the Intra-Jaccard indices between the same segments under different temperatures. Our main observation is that the UC-Dataplant PUF is very robust to temperature changes, as the responses to the same challenge are very similar even for extreme temperature changes (55°C). The responses of the DRAM latency PUF are much more sensitive to temperature changes, confirming the results of the original work [29]. We conclude that the UC-Dataplant PUF performs much better than the DRAM Latency PUF under changing temperature conditions.

To demonstrate how aging affects the similarity of different responses to the same challenge, we use accelerated aging techniques to artificially age our DRAM chips [70–74]. We artificially age the DRAM chips by operating them at 125°C degrees running stress tests during 8 hours. Figure 7 shows the Intra-Jaccard indices between the same segments before and after the aging. We observe that UC-Dataplant is very robust to aging (most of the Jaccard
7.2.3. Evaluation Time. The evaluation time of our Dataplant PUFs is in the same order of magnitude or faster than the fastest state-of-the-art DRAM PUF. The evaluation latency of the UC-Dataplant PUF is the same latency as executing a precharge command, an activation command, and reading 8KB of data. The evaluation latency of US-Dataplant PUF is the same latency as performing an activation command, and reading 8KB of data.

We observe that, in the worst DRAM chip we tested, Dataplant PUF responses to the same challenge are exactly the same 99.72% of the times. To ensure reliable PUF behavior, we also implement a filtering mechanism similar to the filter implemented in DRAM Latency PUF, but using only 5 Dataplant requests. Using this filtering mechanism, all responses to the same challenge are exactly the same in our experiments. We also implement an alternative to the filtering mechanism (similar to PreLatPUF [40]) that profiles the DRAM memory and identifies the DRAM cells that provides robust PUF responses, which enables to eliminate the filtering mechanism. We compare our PUF to the same DRAM Latency PUF [29] we use in the previous section, and to a PreLatPUF [40] that generates PUF responses by reducing the precharge latency. Table 4 summarizes the total evaluation time of the evaluated DRAM PUFs.

TABLE 4: PUF evaluation time of the DRAM Latency PUF, PreLatPUF, and the Dataplant PUF, using 8KB memory segments.

| Latency PUF | PreLatPUF | Dataplant PUFs | Dataplant PUFs (no-filter) |
|-------------|-----------|----------------|---------------------------|
| 88.2ms      | 1.59ms    | 4.41 ms        | 0.88 ms                   |

We make two observations. First, the Dataplant PUFs with/without filter have 20x/100x lower evaluation latency than a DRAM Latency PUF. Second, the Dataplant PUFs without filter are 1.8x faster than the PreLatPUF, but Dataplant PUFs with filter is 5x slower than PreLatPUF. Although the filter mechanism slows down the PUF evaluation latency, it also avoids other issues related to the no-filter mechanism, such as initial profiling, metadata accesses and management, etc. We also perform experiments using a filtering mechanism with 5 responses in the DRAM Latency PUF, but this causes a large degradation of the PUF quality (Section 7.2.2) and compromises the functionality and security of the PUF-based authentication protocol.

We conclude that our mechanism is faster that the best state-of-the-art DRAM PUFs.

7.2.4. Randomness Analysis. A secure key or seed should be random and have high-entropy. Although we already demonstrated the uniqueness of the responses between different memory segments (Section 7.2.2), this does not guarantee properties such as high-entropy.

Methodology. We analyze the randomness of the values generated by UC-Dataplant with real DRAM chips (Table 3), with the experimental setup of Section 7.2.2. We generate a sequence of numbers composed by the relative position of the unpredictable values in a cache line. We use the NIST statistical test suite [41] to analyze the numbers generated by UC-Dataplant.

Results. We run the NIST test suite with the responses to different challenges from all the tested DRAM chips. We collect the PUF responses and we form up to 250KB sequence numbers. Table 5 shows the average NIST p-values and NIST final results for the numbers generated by UC-Dataplant. We use a customized version of the Von Neumann extractor [75] for whitening the random stream.

TABLE 5: Dataplant average results with the NIST randomness test suite.

| NIST Test                               | P-value | Result |
|----------------------------------------|---------|--------|
| monobit                                | 0.681   | PASS   |
| frequency_within_block                 | 1.000   | PASS   |
| non_overlapping_template_matching      | 0.298   | PASS   |
| longest_run_ones_in_a_block            | 0.287   | PASS   |
| binary_matrix_rank                     | 0.536   | PASS   |
| dft                                    | 0.165   | PASS   |
| mauvers_universal                      | 0.987   | PASS   |
| linear_complexity                      | 0.0185  | PASS   |
| serial                                 | 0.988   | PASS   |
| approximate_entropy                    | 0.194   | PASS   |
| cumulative_sums                        | 0.940   | PASS   |
| random_excursion                       | 0.951   | PASS   |
| random_excursion_variant               | 0.693   | PASS   |

Our main observation is that the numbers generated by UC-Dataplant pass all 15 NIST tests, which demonstrates that our PUF is able to generate good quality random numbers.

7.3. Preventing Cold Boot Attacks

We evaluate our new Command-Based Destruction and the Self-Destruction mechanisms described in Section 6. We customize the memory controller to implement the Command-Based Destruction with Rowclone, Lisa-clone, US-Dataplant, and UC-Dataplant. We implement Self-Destruction with US-Dataplant and UC-Dataplant. We also implemented the TCG specification [62] for preventing cold boot attacks (see Section 6.1).
Methodology. We customize Ramulator [76] to support the two proposed Dataplant implementations, Rowclone and Lisa-clone. Table 6 shows the summary of the DRAM and memory controller configurations used in our evaluation.

Our baseline is the TCG software cold boot attack prevention mechanism. We evaluate TCG by simulating a firmware approach that overwrites the memory with zeros by issuing regular write requests. To force writing back the data to memory from cache, we use an instruction that invalidates the data on cache (i.e., the CLFLUSH instruction in x86). TCG does not require any hardware changes other than the BIOS customization.

We implement our Self-Destruction and Command-Based Destruction. Self-Destruction takes place entirely within DRAM, and it is implemented only with Dataplant. We implemented the two variants of Self-Destruction described in Section 6.3.1, namely Self-Destruction using self-refresh and Self-Destruction using burst refresh. Command-Based Destruction issues commands from the memory controller that destroy data in DRAM with Rowclone, Lisa-clone, US-Dataplant, and UC-Dataplant primitives.

To calculate latency of Dataplant we use the SA design described in [77], and to calculate the energy we use a customized version of DRAMPower [65]. For US-Dataplant, we use the same timing parameters as a regular activation, and for UC-Dataplant, we use the same timing as a regular precharge (see Section 4 for details).

TABLE 6: System configuration for evaluating our cold boot attack prevention mechanism.

| Proc. | in-order core, 32KB L1 D&I, 512KB L2 |
| Mem. Ctr. | 64/64-entry read/write queue, FR-FCFS [78], [79] |
| DRAM | 1-2 channels, DDR3-1600 x8 11/11/11 |

We have already done a security analysis and hardware cost analysis of our mechanisms in Section 4.4. In this evaluation we show the latency improvements and the energy savings.

Latency Results. Figure 8 shows the destruction time (in seconds, logarithmic scale) of the TCG software implementation, the Command-Based Destruction (Cmd-D) using all primitives, the Self-Destruction with Burst Refresh (Self-D-Burst) using Dataplant, and the Self-Destruction with Self-Refresh (Self-D-SR) using Dataplant. We assume the same timing parameters for US-Dataplant and UC-Dataplant as regular activation and precharge commands (e.g., tFAW and tRDD) to meet internal DRAM power restrictions. Although we show that UC-Dataplant can perform faster than US-Dataplant for individual primitives (Table 1), the power restrictions are very similar, which limits the throughput of UC-Dataplant. In practice, the latency results of US-Dataplant and UC-Dataplant are identical for the cold boot attack prevention mechanism (Cmd-D Dataplant and Self-D-SR Dataplant in the figure).

We test different DRAM sizes, from 64MB, used in memories specifically designed for IoT [5], to 64GB, used in high-end servers [80]. Our simulator takes into account all timing parameters defined by the DDR standard [43]. The timing parameters for each size are taken from public datasheets released by vendors [81]. For the memories that we don’t have enough information about timing parameters (e.g., 64MB, 64GB), we extrapolate the parameters from existing memory modules.

![Figure 8: Time (log scale) to destroy all DRAM data using a software implementation (TCG), our Command-based Destruction (Cmd-D), our Self-Destruction using Burst refresh (Self-D-Burst Dataplant) and our Self-Destruction using Self-Refresh (Self-D-SR Dataplant).](image)

We make four major observations. First, Self-Destruction based on burst refresh performs 19.5x better than Rowclone and 32.6x better than Lisa. Second, the Command-based destruction (Cmd-D) shows tolerable values for small and medium memory sizes. The Command-based Dataplant implementation performs 1.5x better than Rowclone, and 2.5x better than Lisa. Third, Self-Destruction based on Self-Refresh has the same latency as a regular refresh window. This approach shows the best trade-off between performance and complexity (see Section 6.3.1). Fourth, the software-based destruction mechanism (TCG) has a high latency, especially for large DRAM sizes, which delays the boot time of the system significantly. Also, TCG does not provide strong security guarantees, as we discuss in Section 6.1.

Energy Results. Table 7 shows the energy savings of our mechanism implemented with different hardware primitives, compared to TCG.

TABLE 7: Energy savings of different mechanisms that destroy all DRAM data, compared to TCG.

| Command | Lisa | Rowclone | Self-Burst & Self-SR Dataplant |
|---------|------|----------|-------------------------------|
| 25x     | 45x  | 114x     |

The energy consumption of Self-Destruction is approximately the same as the Command-Based approach (excluding the energy of the bus). We observe that our Dataplant implementations show large energy savings compared to TCG (114x), and very significant energy savings compared to Lisa-clone (4.5x) and Rowclone (2.54x).

Comparison with other State-of-the-Art Mechanisms. There exist other mechanisms that protect against cold boot attacks that are fundamentally different to our approach. This is the case with memory encryption, which provides strong security guarantees at the cost of additional energy consumption. Table 8 shows the performance, power, and area overhead of our Self-Destruction mechanism compared to ChaCha-8 [20] and AES-128 [20], two low-cost ciphers that can be used to prevent cold boot attacks efficiently [20].
TABLE 8: Overhead of our Self-Destruction mechanism based on Dataplant compared to two other mechanisms to prevent cold boot attacks on an Intel Atom N280 processor.

|                      | Self-Destruction | ChaCha-8 [20] | AES-128 [20] |
|----------------------|------------------|---------------|--------------|
| **Runtime Performance** |                  |               |              |
|                      | 0%               | 0%            | 0%           |
| **Runtime Power**    |                  |               |              |
|                      | 0%               | 17%           | 12%          |
| **Area**             | −0%              | 0.3%          | 1.25%        |

1 when less than 16 back-to-back row hits.
2 at peak bandwidth utilization.

We make two main observations. First, our Self-Destruction mechanism has zero performance and power overhead at runtime, and very low hardware cost, which make it difficult to beat as a low-cost method for preventing cold boot attacks. Second, although ChaCha-8 and AES-8 can be implemented for hiding the encryption latency in the common case [20], the power and area overheads of ChaCha-8 and AES-128 are significant in low-cost processors such as the Intel Atom N280. We conclude that our zero-overhead proposal is a very efficient way to protect against cold boot attacks in systems where encryption is not an option.

8. Related Work

To our knowledge, this is the first paper to propose low-cost in-DRAM primitives that enable security mechanisms in all systems that use DRAM. We demonstrate two applications of our primitives: (1) PUF-based authentication and (2) cold boot attack prevention.

In-Memory Operations. We already compare Dataplant to Lisa [60] and Rowclone [59]. As we discussed, Dataplant is a very low overhead set of in-memory primitives to generate data for security mechanisms. Prior works on in-memory operations target other basic functionalities in commodity DRAM chips, such as AND/OR bitwise operations [82]–[85]. A number of works perform processing near memory using 3D-stacked memories, which often contain a logic layer, but such logic requires a much greater logic cost [86]–[89].

PUFs. We have already compared our Dataplant PUFs to the DRAM Latency PUF [29] and to the PreLatPUF [40]. Many PUFs have been investigated in different components, such as SRAM [90]–[95], ASIC logic [96], [97], and DRAM [24], [28], [29], [40], [58]. There is one DRAM PUF that can be accessed during runtime (other than the DRAM Latency PUF). The Runtime DRAM PUF [58] disables refresh in certain memory regions that are initialized with specific values. The PUF response is a function of the errors produced in the cells due to a lack of refresh after some time $t$. Our Dataplant-based PUFs have lower evaluation times than the state-of-the-art DRAM PUFs. In addition, our Dataplant PUFs provide 1) non-destructive read-out, 2) low evaluation latency, 3) robust responses, 4) resiliency to temperature changes, and 5) data-independent responses, characteristics that any other DRAM PUFs can provide all together.

3. While AES-128 and ChaCha-8 provide additional security features, we evaluate their ability to prevent cold boot attacks, as studied in recent literature [20].

Cold Boot Attacks. Several works propose encryption mechanisms to protect data against different attacks, including cold boot attacks [35]–[37], [39], which usually introduce performance and energy overheads. Various proposals attempt to reduce these overheads [34], [36], [38], [98]. Intel’s Software Guard Extensions (SGX) [1] can create protected areas of memory that ensure confidentiality and integrity of the data by using strong encryption (AES) and message authentication codes (MAC). Other papers propose to use modern stream ciphers as a fast way to encrypt memory [20], [99].

A work on data lifetime management [100] proposes to disable access to the data in DRAM, as another solution for cold boot attacks. The authors provide a new flag in the DRAM decoder, controlled by a DRAM command, that controls the access to a DRAM row for untrusted programs. Unlike our Dataplant-based cold boot attack prevention mechanism, this prior work does not prevent an attacker with physical access from having free access to the rows.

Seol et al. [101] propose a mechanism to initialize DRAM with a reset operation based on connect/disconnect power lines. This reset operation has larger latency than Dataplant, as it requires a precharge and an activation command. In comparison, Dataplant requires only one command to destroy the content of the cell. Memory scramblers are the main protection against cold boot attacks in modern unencrypted memory systems. However, these scrambling mechanisms are not sufficient to protect against cold boot attacks, as demonstrated by prior works [20], [33].

Our mechanism for protecting cold boot attacks improves the state-of-the-art by proposing a very simple mechanism with no performance or energy overhead at runtime.

9. Conclusion

We propose Dataplant, a set of low-cost, highly efficient, and reliable in-DRAM primitives that can enable important security mechanisms at low-cost on any device that uses DRAM. The main idea of Dataplant is to slightly modify the internal DRAM timing signals to expose the inherent process variation found in all DRAM chips for generating unpredictable but reproducible values within DRAM. We build two low-cost security mechanisms using Dataplant for demonstrating the potential of our primitive. First, a Dataplant-based physically unclonable functions (PUFs) that improve state-of-the-art DRAM PUFs. Second, a new cold boot attack prevention mechanism based on Dataplant that has zero performance and energy overhead at runtime.

We show in our evaluation that these two mechanisms are significantly faster and more energy-efficient than their state-of-the-art counterparts, with the same or better security guarantees. We conclude that Dataplant can effectively enable low-cost and low-power security mechanisms for all types of devices that use DRAM, from low-cost devices to high-end servers. This paper is a first step towards a more secure DRAM memory. We hope and expect that the availability ofDataplant in commodity DRAM chips will enable new security features and applications.
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### Appendix A.

**D-Dataplant primitive**

In this Appendix we discuss D-Dataplant (Deterministic Dataplant), an alternative Dataplant implementation with different characteristics than US-Dataplant and UC-Dataplant. D-Dataplant generates deterministic values within the SAs by adding a transistor to each SA in the row buffer. The generated values can be stored in DRAM, or can be read by the processor from the SAs without overwriting data in DRAM.

D-Dataplant **deterministically** drives the bitline voltage level to zero (0V) or one (Vdd), and optionally writes the generated value into the cell. The key idea is to add an additional path connecting a fixed voltage level to the bitline. To this end, we add an additional transistor controlled by a *Dataplant* signal. Figure 9 (left) shows how this transistor is connected into the SA to generate a “zero” or a “one” value. Figure 9 (right) illustrates how the Dataplant transistor drives the cell towards a deterministic value (zero in this case).

Figure 9: Dataplant transistor placement (left), and behaviour (right).

Figure 10 shows how the value is generated (including the optional overwriting of the cell). First, the *Dataplant* (V_Dplant) and the SA (V_SA) signals are triggered for driving the bitline to the deterministic voltage level (zero in the example). Then, if the wordline is triggered (V_WL), the generated value is moved to the DRAM cell (V_Cell), overwriting the previous content of the cell.

Figure 10: SPICE simulation of the internal DRAM signals involved in D-Dataplant. Vdd=1V and the original content of the DRAM cell is “one” (V_Cell).

### A.1. Evaluation

Table 9 shows the absolute value and the reduction of latency and energy of D-Dataplant when generating a value of 8 KB, compared to the baseline, Rowclone, Lisa, US-Dataplant and UC-Dataplant. We also show the in-DRAM latency and energy consumption of standard activation and precharge commands. The table also shows the Dataplant energy breakdown (value generation + overwriting) of D-Dataplant (D-Dplant). The energy consumption of D-Dataplant is very similar to US-Dataplant and UC-Dataplant because the additional transistor of D-Dataplant has a very low effect on the energy consumption.
TABLE 9: Latency and energy of different primitives for generating 8KB of data.

| Primitive | Absolute Lat. (ns) | Ener. (nJ) | Reduction Lat. | Ener. |
|-----------|--------------------|------------|----------------|-------|
| Baseline  | 546                | 2000       | 1.0x           | 1.0x  |
| Lisa-clone| 148.5              | 90         | 3.6x           | 22.2x |
| Rowclone  | 90                 | 50         | 6.06x          | 41.5x |
| Activation| 35                 | 17.3       | 15.6x          | 116x  |
| Precharge | 13                 | 17.2       | 42x            | 110x  |
| US-Dplant | 35                 | 17.3 ± 7.3 + 10 | 15.6x | 116x  |
| UC-Dplant | 13                 | 17.2       | 42x            | 110x  |
| D-Dplant  | 35                 | 18 ± 8 + 10 | 15.6x          | 111x  |

Area Overhead. The main area overhead of D-Dataplant is caused by an additional transistor per SA. Our SPICE simulations show that this transistor can be very small, but we consider a full-size transistor to avoid possible layout and fabrication issues. Considering an SA composed of 20 transistors [77], the worst case overall area overhead is between 0.4% and 2% depending on the DRAM design.

Appendix B.

Secure Deallocation

In this Appendix we describe and evaluate secure deallocation, a security application that can be efficiently implemented with any Dataplant primitive. However, this application is especially suitable for D-Dataplant (Appendix A) because most Operating Systems require that newly allocated memory is filled with zero values.

Today’s applications, especially web servers, web browsers, and word processors, do not immediately remove data from memory when it is no longer needed. Instead, the data is physically erased only when the memory is required for other uses. As a consequence, sensitive data could remain in memory for an indefinite amount of time, which augments the risk of exposure.

Secure deallocation [42], [102]–[106] is a technique that set the data to zero at the moment of deallocation, or as soon as the data is not needed anymore. This technique reduces the time that critical data is exposed to attacks. Vanish [105] proposes a similar idea in which the old copies of data are self-destroyed after a specific amount of time. Dataplant enables the implementation of the previous techniques with very low latency, energy, and area overhead.

B.1. Evaluation

Methodology. We simulate US-Dataplant (Section 4.1), UC-Dataplant (Section 4.2), D-Dataplant (Appendix A), Lisa-clone [60], Rowclone [59] and a software secure deallocation mechanism [42].

We customize Ramulator [76] to support all the mechanisms in in-order cores. To generate the traces that drive our simulator, we use PIN [107] for user-level traces, and the Bochs [108] full-system emulator to generate the memory traces that include Linux kernel page allocations and deallocations.

To calculate the area, energy, and latency of our Dataplant primitives, we use the SA design described in Section 4. To estimate the energy consumption of the DRAM module, we use a customized version of DRAM-Power [65]. Table 10 shows the system configuration used in our evaluation.

TABLE 10: System configuration.

| Processor | 1-4 cores, in-order, |
| Cache     | L1:64KB, L2:512KB per core, 64B lines |
| Mem. Ctr. | 64/64-entry read/write queue, FR-FCFS [78], [79] |
| DRAM      | 1 channel, DDR3-1600 x8 11/11/11 |

Table 11 describes the 6 memory-allocation-intensive benchmarks we use. For the multicore evaluation (4 cores), we choose 50 mixes of workloads, in which each mix is composed by two memory-allocation-intensive benchmarks, and two benchmarks that are non-memory-allocation-intensive. The non-memory-allocation-intensive benchmarks are TPC-C [109], TCP-H [109], STREAM [110], SPEC2006 [111], DynoGraph (pagerank, bfs, stream) [112], and HPCC RandomAccess [113]. Table 12 shows 5 representative benchmark mixes.

TABLE 11: Memory-allocation-intensive benchmarks used for evaluating secure deallocation.

| Bench. | Description |
|--------|-------------|
| mysql  | MySQL [114] loading the sample employees.db |
| mcached| Memcached [135], a memory object caching system |
| compiler | Compilation phase from the GNU C compiler |
| bootup | Linux kernel booting up phase |
| shell  | Script running 'find' in a directory tree with 'ls' |
| malloc | stress-ng [116] stressing the malloc primitive |

TABLE 12: Five representative mixes (out of 50) used in the multicore evaluation for secure deallocation.

| MIX1: malloc, bootup, tpcc64, lsqquantum | MIX4: malloc, shell, xalancbmk, bzip2 |
| MIX2: shell, bootup, bmem, xalancbmk | MIX5: malloc, malloc, astar, condmat |
| MIX3: bootup, shell, pagerank | |

Results. Figure 11 shows the single-core speedup (higher is better) and energy savings (higher is better) of Dataplant and other state-of-the-art mechanisms (Rowclone and Lisa-clone) normalized to a software secure deallocation implementation.

We make three observations. First, all hardware implementations improve the performance up to 21% and the energy savings up to 34%, compared to a software implementation. Second, Dataplant performs better than Lisa-clone and Rowclone in all cases, both in performance and energy consumption. Third, the performance improvements and energy savings of Dataplant compared to Rowclone and Lisa-clone are not very large for some benchmarks. Note, however, that our approaches are much easier to integrate on commodity DRAM chips than Lisa-clone or Rowclone (Section 4).

Figure 12 shows the speedup and energy savings of Dataplant and other state-of-the-art mechanisms in a 4-core processor, normalized to a software secure deallocation implementation.
There are at least two types of logic styles that can be used to issue signals in DRAM [77]. First, the delay-chain logic style is composed of a mixture of combinational gates, monostable multivibrators, and latches. This logic is implemented with a series of delays such that a sequence of functions can be executed without a clock. Second, the domino logic uses logic gates that require a clock signal, and it enables to implement logic functions from a cascade of events. The hardware cost of our primitives is very low in both cases, because our mechanism can reuse most of the logic for generating the activation and precharge timing signals.

Figure 11: Single core speedup (larger is better) and energy savings (larger is better) of the secure deallocation hardware approaches compared to a software approach.

Figure 12: 4 core speedup (larger is better) and energy savings (larger is better) of the secure deallocation hardware approaches compared to a software approach.

We make the same observations as for a single core processor: 1) all hardware approaches improve the software implementation, 2) Dataplant performs better than Lisa-clone and Rowclone, and 3) the performance improvements and energy savings of Dataplant compared to Rowclone and Lisa-clone are not very large.

We conclude that 1) implementing secure deallocation with hardware approaches can have significant performance and energy benefits, and 2) Dataplant is the best option to accelerate secure deallocation because it has the best performance and energy results, and it is the approach that is simpler to integrate in commodity DRAM chips.

Appendix C.
DRAM Logic

To the best of our knowledge, there is no public information about how vendors implement the control logic, or what is the specific circuit design of that logic. However, this logic should be very similar to other DRAM logic.