Majority Logic Decoding under Data-Dependent Logic Gate Failures

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Abstract

A majority logic decoder made of unreliable logic gates, whose failures are transient and data-dependent, is analyzed. Based on a combinatorial representation of fault configurations a closed-form expression for the average bit error rate for an one-step majority logic decoder is derived, for a regular low-density parity-check (LDPC) code ensemble and the proposed failure model. The presented analysis framework is then used to establish bounds on the one-step majority logic decoder performance under the simplified probabilistic gate-output switching model. Based on the expander property of Tanner graphs of LDPC codes, it is proven that a version of the faulty parallel bit-flipping decoder can correct a fixed fraction of channel errors in the presence of data-dependent gate failures. The results are illustrated with numerical examples of finite geometry codes.

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I. INTRODUCTION

Increased integration factor of integrated circuits together with stringent energy-efficiency constraints result in increased unreliability of today’s semiconductor devices. As a result of supply voltage reduction and the process variations effects, a fully reliable operation of hardware components cannot be guaranteed [1].

Von Neumann first considered a problem of reliability of systems constructed from unreliable components [2]. His approach includes multiplexing of component logic gates and relies on high redundancy to achieve the desired system reliability. Dobrushin and Ortyukov [3] refined von Neumann’s method and provided upper bounds on the required redundancy for reliable computation of a Boolean function implemented using faulty gates. On the other hand, Elias [4] applied more general coding techniques to the problem of reliable computing. He showed that except for some particular cases, such as exclusive-OR function, there is no code that outperforms von Neumann’s multiplexing method. Overviews of problems in fault tolerant computation is given by Winograd and Cowan [5] and Pippenger [6].

Error control coding, as a method for adding redundancy to ensure fault-tolerance of memory systems built from unreliable hardware, was introduced in the late sixties and early seventies by Taylor [7] and Kuznetsov [8]. In their memory system an information sequence, encoded by a low-density parity-check (LDPC) code, is stored in unreliable memory cells, which are periodically updated using a “noisy” correcting circuit. They proved that, under the so-called von Neumann failure model, such a memory – even with a number of redundant gates linear in memory size – is capable of achieving arbitrary small error probability [7]. The equivalence between Taylor-Kuznetsov (TK) fault-tolerant memory architectures and a Gallager-B decoder, built from unreliable logic gates, was first observed by Vasić et al. in [9] and [10], and developed by Vasić and Chilappagari [11] into a theoretical framework for analysis and design of faulty decoders of LDPC codes.
Performance of ensembles of LDPC codes under faulty iterative decoding was studied by Varshney in [12], who showed that, if certain symmetry conditions are satisfied, the density evolution technique is applicable to faulty decoders which he used to examine the performance of faulty Gallager-A and belief-propagation algorithms. Density evolution analysis of noisy Gallager-B decoders was presented in the series of complementing papers by Yazdi et al. in [13] and [14] and by Huang et al. in [15]. In [13] the authors studied the performance of the binary Gallager-B decoder used to decode irregular LDPC codes and proposed optimal resource allocation of noisy computational units, i.e., variable and check nodes of varying degrees, in order to achieve minimal error rate. The faulty decoder of non-binary regular LDPC codes was analyzed in [14] in the presence of von Neumann errors. In [15] a more complicated failure model was considered, which includes transient errors and permanent memory errors. Similar analysis was done by Leduc-Primeau and Gross in [16], where the faulty Gallager-B decoder, improved by a message repetition scheme, was studied. More general finite-alphabet decoders were investigated by Huang and Dolecek in [17], while a noisy min-sum decoder realization was considered by Ngassa et al. in [18] and by Balatsoukas-Stimming and Burg in [19]. Dupraz et al. [20] have improved the notion of a noisy threshold by introducing the so-called functional threshold, which accurately characterizes the convergence behavior of LDPC code ensembles under noisy finite-alphabet message passing decoding.

Although complex soft-decision iterative decoders, built from reliable components, typically outperform low-complexity majority logic decoders, this is not necessarily true for faulty decoders. In addition, a simple probabilistic gradient decent bit-flipping decoder, recently proposed by Al Rasheed et al. [21], achieves high level of fault-tolerance. Recently, Vasić et al. [22] showed that probabilistic behavior of the Gallager-B decoder due to unreliable components can lead to the improved performance. This resulted in an increased interest in hard-decision decoders. In our previous work [23] we investigated the performance of Gallager-B decoder under timing errors and showed that the density evolution technique is not applicable to that case.

In all the above references a special type of so-called transient failures is assumed. Transient failures manifest themselves at particular time instants, but do not necessarily persist for later times. These failures have probabilistic behavior and we assume the knowledge of their statistics. The simplest such statistics is
the von Neumann failure model [2], which assumes that each component of a (clocked) Boolean network fails at every clock cycle with some known probability. Additionally, failures are not temporally nor spatially correlated. In other words, failures of a given component are independent of those in previous clock cycles and independent of failures of other components.

However, the von Neumann failure model is only a rough approximation of physical processes leading to logic gate failures. The actual probability of failure of a logic gate is highly dependent on a digital circuit manufacturing technology, and for high integration factors the failures are data-dependent and/or temporally correlated, as it was shown by Zaynoun et al. [24]. For example, errors caused by incorrect switching of a gate output are heavily dependent on data values processed by the gate in previous bit intervals and cannot be represented accurately by the von Neumann model.

One-step majority logic (OS-MAJ) decoding, introduced in the sixties by Rudolph [25], is an important class of algorithms in the context of faulty decoding. A OS-MAJ decoder can be seen as a Gallager-B/bit-flipping decoder [26] in which the decoding process is terminated after only one iteration, and bits are decoded by a majority vote on multiple parity-check decisions. In contrast to iterative decoders, the bit error rate performance of these decoders can be evaluated analytically for finite-length codes, as shown by Radhakrishnan et al. [27]. Instead of error rate analysis, iterative decoders are analytically evaluated in terms of guaranteed error correction capability.

Guaranteed error correction of LDPC codes has been only studied for the iterative decoders built from reliable components. Sipser and Spielman [28] showed that expander LDPC codes can be conveniently used to guarantee the correction of a fraction of errors, i.e. there exist some $\alpha$, $0 < \alpha < 1$, for which the decoder can correct $\alpha n$ worst case errors, where $n$ is the code length. They proved that both serial and parallel bit-flipping algorithms can correct a fixed fraction of errors if the underlying Tanner graph is a good expander. In the later work Burshtein [29] generalized their results and proved that a linear number of errors can be corrected by the parallel bit-flipping algorithm with almost all codes in $(\gamma \geq 4, \rho > \gamma)$-regular ensemble. The expander graph arguments can be also used to provide guarantees of the message passing algorithms, at it was shown by Burshtein and Miller [30] and linear programming shown by Feldman et al. [31]. Recently, Chilappagari et al. [32] provided another look on the guaranteed error correction problem.
correction of the bit-flipping algorithms. They found the relation between the girth of the Tanner graph and the guaranteed error correction capability of an LDPC code.

In this paper we examine the effects of data-dependent gate failures to performance of the bit-flipping decoding. We propose a gate state model that captures the effects of data-dependent and correlated nature of gate failures. We derive a closed form expression of the bit error rate (BER) at the output of the OS-MAJ decoder for an ensemble of regular LDPC codes free of four-cycles. Then, we derive bounds on BER performance under a simplified data-dependent model, called the probabilistic gate-output switching model. Additionally, we investigate the error correction capabilities of the noisy bit-flipping decoders and show that expander graph arguments can be used to establish lower bounds on the guaranteed error correction capability in the presence of data-dependent gate failures.

The rest of the paper is organized as follows. In Section II the preliminaries on codes on graphs are discussed. In Section III we give a description of novel approach to gate failure modeling. Section IV is dedicated to the theoretical analysis of the OS-MAJ decoder under general modeling approach. The special case of the data-dependent failure model is further analyzed in Section V. The error correction capability of the noisy bit-flipping decoder is investigated in Section VI. The numerical results are presented in Section VII. Finally, some concluding remarks and future research directions are given in Section VIII.

II. Preliminaries

Let $G = (U, E)$ be a graph with a set of nodes $U$ and a set of edges $E$. An edge $e$ is an unordered pair $(v, c)$, which connects two neighborly nodes $v$ and $c$. The cardinality of $U$, denoted as $|U|$, represents the order of the graph, while $|E|$ defines the size of the graph. A set of neighbors of a particular node $u$ is denoted as $\mathcal{N}(u)$. The number of neighbors of a node $u$, denoted as $d(u)$, is called the degree of $u$. The average degree of a graph $G$ is $\bar{d} = 2|E|/|U|$. The girth $g$ of a graph $G$ is the length of smallest cycle in $G$. A bipartite graph $G = (V \cup C, E)$ is a graph constructed from two disjoint sets of nodes $V$ and $C$, such that all neighbors of nodes in $V$ belong to $C$ and vice versa. The nodes in $V$ are called variable nodes and nodes from $C$ are check nodes. A bipartite graph is said to be $\gamma$-left-regular if all variable nodes have degree $\gamma$, and similarly, a graph is
Consider a \((\gamma, \rho)\)-regular binary LDPC code of length \(n\) and its graphical representation given by \(\gamma\)-left-regular and \(\rho\)-right-regular Tanner bipartite graph \(G\), with \(n\gamma/\rho\) check nodes and \(n\) variable nodes. In a part of this paper we consider expander codes, i.e. LDPC codes whose Tanner graphs satisfy expansion property defined as follows.

**Definition 1.** \(^{(28)}\) A Tanner graph \(G\) of a \((\gamma, \rho)\)-regular LDPC code is a \((\gamma, \rho, \alpha, \delta)\) expander if for every subset \(S\) of at most an \(\alpha n\) variable nodes, at least \(\delta|S|\) check nodes are incident to \(S\).

Let \(x = (x_1, x_2, \ldots, x_n)\) be a codeword of a binary LDPC code, which appears at the input of a binary symmetric channel (BSC). The output of the channel \(r = (r_1, r_2, \ldots, r_n)\), where \(\Pr\{r_k \neq x_k\} = p\), is being decoded by our majority logic decoder. The number of flipped bits represents the Hamming distance between the transmitted codeword \(x\) and the received word \(r\), and is denoted as \(d_H(x, r)\). The decoder is divided into processing units that correspond to nodes in Tanner graph representation of the decoder. Let \(\vec{m}_i(e)\) and \(\vec{m}_i(e)\) be messages passed on an edge \(e\) from variable node to check node and check node to variable node, during the \(i\)-th decoding iteration, respectively. Similarly \(\vec{m}_i(F)\) and \(\vec{m}_i(F)\) denote sets of all messages from/to a variable node over a set of edges \(F \subseteq E\). We next summarize our majority logic decoder.

- At iteration \(i = 0\) the variable-to-check messages are initialized by using values received from the channel, i.e. \(\vec{m}_i(e) = r_v, \forall e \in \mathcal{N}(v)\). At iteration \(i, i > 0\), a variable node processing unit \(v\) performs the majority voting on binary messages received from its neighboring check nodes as follows
  \[
  \Phi(\vec{m}_{i-1}(\mathcal{N}(v))) = \begin{cases} 
  s, & \text{if } |\{e' \in \mathcal{N}(v) : \vec{m}_{i-1}(e') = s\}| > \lceil \gamma/2 \rceil, \\
  r_v, & \text{otherwise},
  \end{cases}
  \]
  \[(1)\]
  where \(s \in \{0, 1\}\) and \(\lceil \gamma/2 \rceil\) denotes the smallest integer greater than or equal to \(\gamma/2\). The output of the majority logic (MAJ) gate, described by the function \(\Psi(\cdot)\) is then passed to all neighboring check nodes, i.e \(\vec{m}_i(e) = \Phi(\vec{m}_{i-1}(\mathcal{N}(v)))\), \(\forall e \in \mathcal{N}(v)\).

- During each iteration \(i, i \geq 0\), a check node processing unit \(c\) performs \(\rho\) eXclusive-OR (XOR)
operations defined as follows

\[
\Psi(\widetilde{m}_i(N(c) \setminus \{e\})) = \bigoplus_{e' \in N(c) \setminus \{e\}} \widetilde{m}_i(e'), \ \forall e \in N(c).
\]

(2)

The results of the XOR operations represent estimates of bits associated to neighboring variable nodes and they are passed by mapping \(\widehat{m}_i(e) = \Psi(\widetilde{m}_i(N(c) \setminus \{e\}))\), \(\forall e \in N(c)\). If the decoding is terminated after the \(i\)-th iteration, the result of \(\Phi(\widehat{m}_i(N(v)))\) represents the decoded bit \(x_v\). Note that, when built from perfectly reliable logic gates, our decoder is functionally equivalent to the parallel bit-flipping decoder [28]. Hardware unreliability in the decoder comes from unreliable computation of the operations \(\Psi(\cdot)\) as XOR logic gates performing these functions are prone to data-dependent failures, which are described in the following section.

After each decoding iteration, the code bits are estimated based on the function \(\Phi(\cdot)\), which results in probability of error of an estimated bit that is greater than or equal to the probability of failure of the MAJ gate performing this function. Since the error probability of the MAJ gate lower bounds the BER performance, MAJ gates must be made highly reliable. Otherwise, the probability of error would be determined by this gate, not by the error control scheme. Thus, it is reasonable to make an assumption that MAJ gates are perfect and that only the XOR gates are faulty. Reliable MAJ gates can be realized, for example, by using larger transistors. Similar assumptions regarding perfect gates were also used in other relevant literature [7], [12], [33].

When the decoding is terminated after only one iteration, and a bit \(x_v\) is decoded by \(\Phi(\widehat{m}_0(N(v)))\), our decoder is reduced to the known OS-MAJ decoder, recently analyzed in our previous works [33], [34]. In the first part of this paper we specially consider the OS-MAJ decoder, due to its simplicity.

III. DATA-DEPENDENT GATE ERROR MODEL

A. General Modeling Approach

Let \(f : \{0,1\}^m \to \{0,1\}, \ m > 1\), be an \(m\)-argument Boolean function. The relation between input arguments \(y_1^{(k)}, y_2^{(k)}, \ldots, y_m^{(k)}\) and an output \(z^{(k)}\), at time instant \(k \geq 0\), of a perfect gate realizing this function is \(z^{(k)} = f(y_1^{(k)}, y_2^{(k)}, \ldots, y_m^{(k)})\). The output of a faulty gate is \(f(y_1^{(k)}, y_2^{(k)}, \ldots, y_m^{(k)}) \oplus \xi^{(k)}\).
where $\oplus$ is Boolean XOR, and the error at time $k, \xi^{(k)} \in \{0, 1\}$, is a Bernoulli random variable. Denote by $y^{(k)} = (y_1^{(k)}, y_2^{(k)}, \ldots, y_m^{(k)})$ a gate input vector, i.e., a vector of arguments. Denote by $\{y^{(k)}\}_{k \geq 0}$ a time-sequence of input vectors, and by $\{\xi^{(k)}\}_{k \geq 0}$ a corresponding error sequence. In this manuscript we will interchangeably use the terms “failure” and “error” meaning that failures are “additive” errors. In the classical von Neumann transient failure model the error values $\{\xi^{(k)}\}_{k \geq 0}$ are independent of the input sequence $\{y^{(k)}\}_{k \geq 0}$.

In order to capture data and time dependence of gate failures more accurately, we propose the following gate-state model. Namely, we assume that $\xi^{(k)}$ is affected by the current and $M - 1$ prior consecutive gate input vectors, i.e., its probability depends on the input vector sequence in the time interval $[k - (M - 1), k]$, denoted as $\{y^{(j)}\}_{j \in [k - (M - 1), k]}$, where $M$ is a positive integer. Denote this probability by $\Pr\{\xi^{(k)} = 1 | s^{(k)}\}$, where a gate state $s^{(k)}$ at time $k$ is defined as $s^{(k)} = \{y^{(j)}\}_{j \in [k - (M - 1), k]}$. As previously stated, in our decoder only XOR gates are unreliable. The number of states grows exponentially with $M$ and $\rho$, i.e., for a $(\rho - 1)$-input XOR gate, used in our decoder, there are $2^{M(\rho - 1)}$ states.

The inputs of a (perfect) MAJ gate are the outputs of $\gamma$ XOR gates in the neighboring check nodes. Thus, at time $k$ these gates can be associated with a state array $\sigma^{(k)} = (s_1^{(k)}, s_2^{(k)}, \ldots, s_\gamma^{(k)})$, whose elements represent states of particular XOR gates. Based on $\sigma^{(k)}$, an error probability vector can be formed as $\varepsilon^{(k)} = (\varepsilon_1^{(k)}, \varepsilon_2^{(k)}, \ldots, \varepsilon_\gamma^{(k)})$, $\varepsilon_m^{(k)} = \Pr\{\xi^{(k)} = 1 | s_m^{(k)}\}, 1 \leq m \leq \gamma$. The values of the error probability vector can be obtained by measurements or by simulation of the selected semiconductor technology. Thus, in our analysis we assume that these values are known.

B. Probabilistic Gate-Output Switching Model

Due to supply voltage reduction, switching of a gate output is prolonged and the signal is sampled or used in the next stage before it reaches a steady value. Recently, Amaricai et al. [35] investigated the probabilistic nature of gate switching for subpowered CMOS circuits. They proposed several fault injection models in CMOS circuits in which errors are added only when the gate output changes. Translated to our model, this means that it is sufficient to consider the case $M = 2$.

In this subsection we define the probabilistic gate-output switching model (GOS), in which the logic
Gate switches incorrectly with a probability that depends on a supply voltage, temperature and considered gate delay. This model was shown to have reduced complexity with minor degradation of accuracy when compared to more complex models that take into account the fact that different input patterns cause failures with different probabilities.

In the GOS error model the probability that a XOR gate fails to switch at time $k$ is $\Pr\{\xi^{(k)} = 1|z^{(k)} \neq z^{(k)}\} = \bar{\varepsilon}$, where $\bar{\varepsilon} > 0$. On the other hand, when the gate output is unchanged during two consecutive time instants, the function $f$ is always correctly computed as assumed in [35] and [36], i.e. $\Pr\{\xi^{(k)} = 1|z^{(k)} = z^{(k-1)}\} = 0$.

Note that the GOS model does not capture all effects which may lead to timing-related errors, since changes of the multiple inputs can cause a gate failure, even if the ideal output remains unchanged [24]. However, in the most recent literature dedicated to CMOS circuits operating with a voltage supply near or below the threshold voltages [35], [36], the above effects were neglected. The general framework presented in the previous subsection is applicable to other more complicated scenarios.

IV. ANALYSIS OF THE OS-MAJ DECODER UNDER THE GENERAL GATE ERROR MODEL

In this section we present an analytical method for performance evaluation of an ensemble of regular LDPC codes with girth at least six decoded by the faulty OS-MAJ decoder, described in the previous sections. In the Tanner graph of a code with girth at least six, the variable nodes connected to the neighboring $\gamma$ checks, of a variable node $v$, are all distinct. First, we consider a particular code bit $x_v$ and calculate the probability that it is miscorrected, under a fixed state array associated to the XOR gates used for decoding of $x_v$.

Let $q_l$ be a vector corresponding to one lexicographically ordered $u$-subset of a set $[l] = \{1, 2, \ldots, l\}$ and let a vector $q_r$ contain the remaining elements of $[l]$, arbitrary ordered. We create a vector $q$ by juxtapositioning $q_l$ and $q_r$. We can arrange all possible vectors $q$ into rows of an $\binom{l}{u}$ by $l$ array $Q^{u,l}$. For example, if $l = 4$ and $u = 2$, the rows of $Q^{2,4}$ are $(1, 2, 3, 4)$, $(1, 3, 2, 4)$, $(1, 4, 2, 3)$, $(2, 3, 1, 4)$, $(2, 4, 1, 3)$ and $(3, 4, 1, 2)$. The array $Q^{u,l}$ is instrumental in book-keeping of data-dependent error probabilities as described in the following lemma.
Lemma 1. The probability that a code bit $x_v$ of a $(\gamma, \rho)$-regular LDPC code is incorrectly decoded by the faulty OS-MAJ decoder, whose gates fail according to an error probability vector $\varepsilon$, is given by

$$P_v(p, \varepsilon) = \sum_{i=\lceil \gamma/2 \rceil}^{\gamma} \sum_{j=1}^{i} \prod_{m=1}^{\gamma} P_{q_{i,m}} \prod_{m=i+1}^{\gamma} (1 - P_{q_{j,m}}) + \frac{(-1)^{\gamma/2} + 1}{2} \prod_{j=1}^{\gamma} P_{q_{j,m}} \prod_{m=\lceil \gamma/2 \rceil + 1}^{\gamma} (1 - P_{q_{j,m}}),$$

(3)

where $P_{q_{j,m}} = \varepsilon_{q_{j,m}}(1 - A) + (1 - \varepsilon_{q_{j,m}})A$,

$$A = 0.5(1 - (1 - 2p)^{\rho - 1}),$$

(4)

and $q_{t,m}$ denote the element in the $t$-th row and the $m$-th column of the matrix $Q^{i,\gamma}$.

Proof: Given the fact that each received bit is erroneous with the probability $p$, the probability that the output of a fully reliable XOR gate is also erroneous is equal to $A$. As $j$-th XOR gate fails with the probability $\varepsilon_j$, the error at the output of $j$-th XOR is given by $P_j = \varepsilon_j(1 - A) + (1 - \varepsilon_j)A$. Each row of the error configuration matrix $Q^{i,\gamma}$ represents one possible error configuration which results in appearance of exactly $i$ erroneous bit estimates at inputs of the MAJ gate. The total number of such error configurations is $i\gamma$.

A bit $x_v$ will be incorrectly decoded if the majority of its estimates are incorrect. Thus, for odd values of $\gamma$, only probabilities of $i$ being greater than or equal to $(\gamma + 1)/2$ leads to a miscorrection. If $\gamma$ is even, then there is a possibility of a tie (equal number of correct and incorrect estimates). For such cases $\gamma/2$ incorrect estimates can result in miscorrection, which is depicted by the second part of Eq. (3). ■

Let $\{x^{(k)}\}_{k \geq 0}$ be a codeword sequence transmitted through the channel. Clearly, decoding error of $x^{(k)}$ depends on $M - 1$ codewords, previously transmitted through channel. Let $x_{m,v} = \{x^{(j)}_{m,v}\}_{j \in [k - (M - 1), k]}$, $1 \leq m \leq \gamma$, $1 \leq v \leq n$, be a sequence of code bits that, if transmitted with no errors, will appear at inputs of $m$-th XOR gate connected to a node $v$, in a time interval $[k - (M - 1), k]$. Then, we formulate the theorem which captures the decoder performance under correlated data-dependent gate failures.

Theorem 1. The average bit error rate (BER) of a $(\gamma, \rho)$-regular LDPC code, when a codeword sequence
\{x^{(j)}\}_{j \in [k-(M-1),k]} \text{ is decoded by the faulty OS-MAJ decoder is}

\[ P_e(\text{error}|x^{(k)}, \ldots, x^{(k-M+1)}) = \frac{1}{n} \sum_{v=1}^{n} \sum_{t=1}^{2(\rho-1)\gamma M} P_v(p, \varepsilon^{(t)}) \prod_{m=1}^{\gamma} p_{\text{even}}(s^{(t)}_{m,v}, x_{m,v}) (1-p)^{M(\rho-1)-d_H(s^{(t)}_{m,v}, x_{m,v})}. \]

(5)

Proof: See Appendix A.

The error probability vectors in general depend on transmitted codewords and the expression (5) describes the conditional error probability. The computational complexity of the BER expression grows exponentially with the left- and right-degree of Tanner graph and the memory order of the state model. However, different error probability vectors, \(\varepsilon^{(1)}, \varepsilon^{(2)}, \ldots, \varepsilon^{(t)}\), may lead to the same bit error probability, \(P_v(p, \varepsilon^{(1)}) = P_v(p, \varepsilon^{(2)}) = \ldots = P_v(p, \varepsilon^{(t)})\), and in practice the number of terms that need to be calculated is significantly lower. For example, in some important cases the average BER in the presence of errors caused by incorrect switching of the gate output can be obtained by computing only \(\gamma + 1\) terms. The detailed analysis of the decoder under these errors is presented in the next section.

In the transient gate failure model, introduced by von Neumann, the code bit error probability is independent of state arrays, i.e., \(P_v(p, \varepsilon^{(t)}) = P(p, \bar{\varepsilon}), 1 \leq t \leq 2(\rho-1)\gamma M, 1 \leq v \leq N\). Thus, for a special case of von Neumann errors, that we previously investigated in [34], the BER expression given by Eq. (5) reduces to Eq. (3). In addition, as all XOR gates have the same failure rates \(\varepsilon_i = \bar{\varepsilon}, 1 \leq i \leq \gamma\), any configuration of \(i\) incorrect estimates is equally likely and Eq. (5) simplifies into expression

\[ P_v(p, \bar{\varepsilon}) = \sum_{i=\lceil(\gamma+1)/2\rceil}^{\gamma} \binom{\gamma}{i} P^i (1-P)^{\gamma-i} + \frac{(-1)^\gamma + 1}{2} p^{\gamma/2} (1-P)^{\gamma/2}, \]

(6)

where \(P = (1-A)\bar{\varepsilon} + A(1-\bar{\varepsilon})\).

V. ANALYSIS OF THE OS-MAJ DECODER UNDER THE GOS ERROR MODEL

The XOR gate output will remain unchanged if gate input vectors from two consecutive time points \(k-1\) and \(k\), \(k > 0\), are the same or differ in an even number of positions. Thus, for example, the \(m\)-th XOR, used for the decoding of a bit \(x_v\), will produce correct output at time \(k\), if transmitted vectors \(x^{(k-1)}_{m,v}\) and \(x^{(k)}_{m,v}\) satisfy the relation \(d_H(x^{(k-1)}_{m,v}, x^{(k)}_{m,v}) = 0 \text{ (mod } 2\) and no channel errors occur. Similarly,
the gate output will be erroneous with the probability \( \bar{\varepsilon} \) if all bits are received without errors, and if
\[
d_H(x_{m,v}^{(k-1)}, x_{m,v}^{(k)}) = 1 \pmod{2}.
\]
However, the parity of the gate input vectors can change due to channel induced errors, that is when an odd number of gate inputs from two consecutive time points are flipped.

The probability of the union of all such events is equal to
\[
B = \sum_{j=0}^{\rho-2} \binom{2(\rho-1)}{2j+1} p^{2j+1} (1 - p)^{2\rho - 2j - 3} = \frac{1}{2} (1 - (1 - 2p)^2(\rho-1)).
\]
(7)

Therefore, the gate output will be erroneous with the probability \( \bar{\varepsilon}B \) when the relation
\[
d_H(x_{m,v}^{(k-1)}, x_{m,v}^{(k)}) = 0 \pmod{2}
\]
is satisfied. Let all XOR gates, used for decoding \( x_{v} \), with this property, form a set \( G_v \). Similarly, \( H_v \) is composed of all gates for which
\[
d_H(x_{m,v}^{(k-1)}, x_{m,v}^{(k)}) = 1 \pmod{2}.
\]
It is clear that \( G_v \cup H_v = \gamma \).

We now extend the previous discussion on faulty XOR gates, and formulate the lemma that describes data-dependence of the OS-MAJ decoding.

**Lemma 2.** Let \( x^{(k-1)} \) and \( x^{(k)} \) be codewords decoded in two consecutive bit intervals. The faulty OS-MAJ decoder will operate the worst if the cardinality of \( G_v, |G_v| = 0, 1 \leq v \leq n \), while the best performance corresponds to decoding of consecutive codewords for which \( |G_v| = \gamma, 1 \leq v \leq n \).

**Proof:** Failures of XOR gates from the set \( G_v \) happen with probability \( B\bar{\varepsilon} \), while the failure rate under condition that a gate is an element of \( H_v \) is equal to \( (1 - B)\bar{\varepsilon} \). Since \( B < 0.5 \) a gate from \( H_v \) will be erroneous more often. The proof of lemma follows from the fact that the probability \( P_v(p, \varepsilon) \) monotonically increases with the increase of hardware unreliability, i.e., for every \( \varepsilon^{(t_1)} \) and \( \varepsilon^{(t_2)} \) with property \( \varepsilon^{(t_1)}_m \leq \varepsilon^{(t_2)}_m, 1 \leq m \leq \gamma, P_v(p, \varepsilon^{(t_1)}) \leq P_v(p, \varepsilon^{(t_2)}) \) holds.

The previous lemma reveals a fundamental property of the OS-MAJ decoding performance under data dependent hardware failures: the dependence on a codeword decoding order. It can be seen that, for example, consecutive decoding of two identical codewords will result in the lowest error rate, while if two complementary codewords are consecutively decoded the decoder will operate worst.

The OS-MAJ decoder built entirely from reliable components satisfy the symmetry theorem, which states that performance of the decoder is independent of codewords being decoded. We see that the symmetry condition does not hold for the OS-MAJ decoding in the presence of errors caused by incorrect
switching of the gate output.

Let the cardinality of the set \(G_v\), be equal to \(|G_v| = t_v\). The bit miscorrection probability, given by Eq. (3), depends only on the number of non-zero elements of \(\varepsilon\), but not on its order. Thus, we can simplify the notation by introducing \(\tilde{\varepsilon}(t) = (\tilde{\varepsilon}_1(t), \tilde{\varepsilon}_2(t), \ldots, \tilde{\varepsilon}_\gamma(t))\): an error probability vector with \(t\) non-zero elements. This allows us to formulate the following corollary of Theorem 1 that gives the bit miscorrection probability under the GOS error model.

**Corollary 1.** The probability that a code bit \(x_v\) of a \((\gamma, \rho)\)-regular LDPC code is incorrectly decoded by the faulty OS-MAJ decoder under the GOS error model is given by

\[
\bar{P}_v(t_v) = \sum_{t=0}^{\gamma} P_v(p, \tilde{\varepsilon}(t)) \sum_{j=t_{\min}}^{t_{\max}} \binom{t_v}{j} \binom{\gamma - t_v}{t - j} B^{t - j} \gamma - t_v (1 - B)^{t_v + t - 2j}, \tag{8}
\]

where, \(t_{\min} = \max(t + t_v - \gamma, 0)\) and \(t_{\max} = \min(t_v, t)\).

**Proof:** The probability that \(j\) non-zero failure rates in \(\tilde{\varepsilon}(t)\) originated from the set \(G_v\) and \(t - j\) from the set \(H_v\) is equal to \(\binom{t_v}{j} \binom{\gamma - t_v}{t - j} B^{t - j} \gamma - t_v (1 - B)^{t_v + t - 2j}\). The sum of all possible ways that \(t\) non-zero failure rates can appear represents the contribution of \(P_v(p, \tilde{\varepsilon}(t))\) in the overall miscorrection probability value. The final summation for all \(\gamma + 1\) values of \(t\) gives the bit miscorrection probability. 

Based on Lemma 2 and Corollary 1 we can measure the effect of data-dependence by bounding the BER, as described in the following lemma.

**Lemma 3.** The BER of a \((\gamma, \rho)\)-regular LDPC code decoded by the faulty OS-MAJ decoder under the GOS error model, \(\bar{P}_{e,GOS}\), is bounded by

\[
\sum_{t=0}^{\gamma} \binom{\gamma}{t} B^t (1 - B)^{\gamma - t} P_v(p, \tilde{\varepsilon}(t)) \leq \bar{P}_{e,GOS} \leq \sum_{t=0}^{\gamma} \binom{\gamma}{t} B^\gamma (1 - B)^{t_v + t - 2j} P_v(p, \tilde{\varepsilon}(t)). \tag{9}
\]

**Proof:** According to Lemma 2, the lower bound is obtained by setting \(t_v = \gamma\) in Eq. (8). Similarly, the upper bound can be calculated by setting \(t_v = 0\). 

The bounds presented in Eq. (9) are obtained under conditions described in Lemma 2, i.e., they represent the lowest and the highest possible BER values. These bounding values depend on all parameters \(\gamma, \rho, \ldots\).
and \( \bar{\epsilon} \) and \( p \) and can differ by orders of magnitude. The analysis of the decoder performance, for several classes of LDPC codes, is presented in Section VII.

VI. GUARANTEED ERROR CORRECTION UNDER THE GOS ERROR MODEL

In this section we prove that the correcting capability of the iterative majority logic decoder, built partially from unreliable gates, increases linearly with code length, when Tanner graph of a code satisfies the expansion property, defined in Section III. We assume that following two conditions are satisfied: (i) the MAJ gates used in the decoder are reliable, and XOR failures follow the error mechanism introduced in Section III-B, and (ii) no more than \( |C_{XOR}| \) gates are erroneous in the first iteration. The need for previously described assumptions will be discussed later. Now we formulate the theorem that gives the error correction capability of the noisy majority logic decoder.

Theorem 2. Consider a \( (\gamma, \rho, \alpha, (7/8 + \epsilon)\gamma) \) expander, \( 1/8 \geq \epsilon > 0 \). The majority logic decoder built from unreliable check nodes can correct any pattern of \( |V_1| < \left( \frac{3(3 + 8\epsilon)\alpha n}{32} - \sqrt{2}|C_{XOR}| \right) \) errors.

Proof: Let \( V_i \) be a set of corrupt variables at the beginning of the \( i \)-th decoding iteration. A set of corrupt variables at the beginning of the \( (i + 1) \)-th iteration (i.e., end of the \( i \)-th iteration), \( V_{i+1} \), can be divided into two disjunct subsets: (i) \( (V_{i+1} \cap V_i) \), a subset of corrupt variables that remained corrupt at the end of the \( i \)-th iteration, and (ii) \( (V_{i+1} \setminus V_i) \), a subset of newly corrupted variables, i.e., variables that were correct in the \( (i - 1) \)-th iteration, but became corrupt during the \( i \)-th iteration. Let \( S_i \) be a set of variables that were corrected during the \( (i - 1) \)-th iteration and also stayed correct at the end of the \( i \)-th iteration. Since variables in \( S_i \) are flipped in the \( (i - 1) \)-th iteration, from the definition of the GOS error model, it follows that any variable in \( S_i \) may cause a failure of the neighboring XOR gates in the \( i \)-th iteration and consequently the incorrect estimates of variables with whom it shares the neighbors. On the other hand, no failure of the XOR gate output occurs in the check nodes connected to only un-flipped variables in the \( (i - 1) \)-th iteration.

Each incorrect estimate of a particular variable in \( V_{i+1} \setminus V_i \) is due to the variable’s connection (through shared neighbors) to variables from the set \( V_i \cup S_i \). This comes from the fact that the check node, which sends an incorrect estimate to a node in \( V_{i+1} \setminus V_i \), must be also connected to at least one other node.
which causes that incorrect estimate. Thus, each incorrect estimate indicates that a check is shared by
two variables in $V_i \cup S_i \cup V_{i+1}$. On the other hand, there are no restrictions on possible neighbors of a
check producing all correct estimates – they can be variables in $V_{i+1} \setminus V_i$ or variables outside of the set
$V_i \cup S_i \cup V_{i+1}$. From Eq. (1), the number of correct estimates of each newly corrupt variable in $V_{i+1} \setminus V_i$
cannot be greater than $\gamma/2$, which means that the correct estimates are produced by at most $\gamma/2$ different
neighboring check nodes. The set $V_i \cup S_i \cup V_{i+1}$ has the highest number of neighbours when $S_i$ and
$V_{i+1} \setminus V_i$ are disjunct. Then for some $\delta$, $0 < \delta \leq 1$, we have
\[ |\mathcal{N}(V_i \cup S_i \cup V_{i+1})| \leq \delta \gamma |V_i \cup S_i| + \gamma/2 |V_{i+1} \setminus V_i|. \] (10)
Variables corrected during the $i$-th iteration (a set $V_i \setminus V_{i+1}$), as well as variables from $S_i$ can be connected
to all different check nodes. Since a variable from $V_i \cap V_{i+1}$ shares at least half of its neighbours with
other variables from $V_i \cup S_i$, it contributes with at most $3\gamma/4$ additional check nodes in $\delta \gamma |V_i \cup S_i|$ and we have
\[ \delta \gamma |V_i \cup S_i| \leq \gamma (|V_i| + |S_i| - |V_{i+1} \cap V_i|) + 3\gamma/4 |V_{i+1} \cup V_i| \]
\[ = \gamma (|V_i| + |S_i|) - \gamma/4 |V_{i+1} \cap V_i|. \] (11)

If we assume that
\[ |V_i \cup V_{i+1} \cup S_i| < \alpha n \] (12)
for all $i > 0$, then, by the expansion property,
\[ |\mathcal{N}(V_i \cup S_i \cup V_{i+1})| \geq (7/8 + \epsilon) \gamma (|V_i| + |S_i| + |V_{i+1} \setminus V_i|). \] (13)
Combining previous expression with Eq. (10) and Eq. (11) we obtain
\[ |V_i|(1 - 8\epsilon) \geq (3 + 8\epsilon)|V_{i+1} \setminus V_i| + 2|V_{i+1} \cap V_i| + (8\epsilon - 1)|S_i| \geq 2|V_{i+1}| - (1 - 8\epsilon)|S_i|. \] (14)
Because all elements of $S_i$ were corrupted before the $(i - 1)$-th iteration, we know that $|S_i| \leq |V_{i-1}|$,
which, based on the previous inequality, implies
\[ (1 - 8\epsilon)|V_i| \geq 2|V_{i+1}| - (1 - 8\epsilon)|V_{i-1}|. \] (15)
Let $|V_2| \leq \beta |V_1|$, $\beta > 0$. Then, $|V_i|$ can be bound as presented in the following lemma.

**Lemma 4.** The number of corrupt variables before the $i$-th decoding iteration, $i > 1$, $|V_i|$ is bounded by

$$|V_i| \leq \frac{4\sqrt{1 - 8\epsilon} + (2\beta - 1 + 8\epsilon)(\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon})}{(1 - 8\epsilon)\sqrt{9 - 8\epsilon}} \left(\frac{2\sqrt{1 - 8\epsilon}}{\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon}}\right)^i |V_1|. \quad (16)$$

**Proof:** See Appendix B. ■

In order to complete this part of the proof of Theorem 2, we have to analyze the first decoding iteration and bound $|V_2|$. In the following lemma we show that the upper bound of the value $|V_2|$ can be expressed in terms of $|V_1|$ and $|C_{XOR}|$, the number of XOR gate failures in the first iteration.

**Lemma 5.** The number of corrupt variables after the first decoding iteration, $|V_2|$, under the condition $|V_1| < (3 + 8\epsilon)\alpha n/4$, is bounded by

$$|V_2| \leq \frac{1 - 8\epsilon}{2} |V_1| + |C_{XOR}|. \quad (17)$$

**Proof:** From the analysis presented in [28], we know that the decoder built from reliable components reduces the number of corrupt variables to at most $(1 - 4\delta)|V_1|$, for all $1/4 \geq \delta > 0$. The first summand in Eq. (17) is obtained noting that $\delta = 1/8 + \epsilon$. The second summand in Eq. (17) follows from the fact that each XOR gate failure can corrupt at most one additional variable. ■

Combining Eq. (16) and Eq. (17), we obtain

$$|V_i| \leq \frac{4\sqrt{1 - 8\epsilon}|V_1| + 2(\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon})|C_{XOR}|}{(1 - 8\epsilon)\sqrt{9 - 8\epsilon}} \left(\frac{2\sqrt{1 - 8\epsilon}}{\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon}}\right)^i |V_1|. \quad (18)$$

The previous equation shows that, for all $\epsilon \in (0, 1/8]$, the number of corrupt variables reduces over time, which after a sufficient number of iterations leads to the correction of all initially corrupt variables.

Note that in our derivation we also assumed that $|V_i \cup V_{i+1} \cup S_i| < \alpha n$, for all $i > 0$ (Eq. (12)). We next prove the previous statement by using mathematical induction.

Let us assume that $|S_i \cup V_{i-1} \cup V_i| < \alpha n$. This means that Eq. (18) is satisfied for the first $i - 1$ iterations and that we can use it to bound $|V_{i-1}|$ and $|V_i|$. Assume, by the way of contradiction, that $|S_i \cup V_i \cup V_{i+1}| \geq \alpha n$. Then, since we know that $|S_i \cup V_i| < \alpha n$, there must exists some $D \subset V_{i+1} \setminus (V_i \cup S_i)$
for which $D \cup S_i \cup V_i = \alpha n$, and $|N(D \cup S_i \cup V_i)| \geq (7/8 + \epsilon)\gamma \alpha n$. On the other hand, for some $\delta$, $7/8 + \epsilon \leq \delta \leq 1$, the number of checks connected to $D \cup S_i \cup V_i$ is bounded by

$$|N(D \cup S_i \cup V_i)| \leq \delta \gamma (|S_i| + |V_i|) + \gamma / 2 (\alpha n - |S_i| - |V_i|).$$

Combining the previous relation with the lower bound given by the expansion, we obtain

$$|S_i| + |V_i| \geq \frac{3 + 8 \epsilon}{8 \delta - 4} \alpha n \geq \frac{3 + 8 \epsilon}{4} \alpha n. \tag{20}$$

On the other hand, since

$$|S_i| + |V_i| \leq |V_{i-1}| + |V_i|, \tag{21}$$

based on Eq. (18) we finally obtain

$$|V_1| \geq \left[ g_1(\epsilon) \frac{3 + 8 \epsilon}{4} \alpha n - g_2(\epsilon) |C_{XOR}| \right] \frac{1}{\sqrt{1 - 8 \epsilon}}, \tag{22}$$

where

$$g_1(\epsilon) = \frac{\sqrt{9 - 8 \epsilon} - \sqrt{1 - 8 \epsilon}}{4(\sqrt{9 - 8 \epsilon} + \sqrt{1 - 8 \epsilon})} \left( \frac{\sqrt{9 - 8 \epsilon} - \sqrt{1 - 8 \epsilon}}{2 \sqrt{1 - 8 \epsilon}} \right)^{i-1}, \tag{23}$$

and

$$g_2(\epsilon) = \frac{\sqrt{9 - 8 \epsilon} - \sqrt{1 - 8 \epsilon}}{2} \tag{24}.$$

The function $g_1(\epsilon)$ is monotonically increasing on the interval $(0, 1/8]$, and its minimal value on this interval satisfies $\min_{0<\epsilon\leq1/8} (g_1(\epsilon)) > 3/8$. Similarly, the maximal value of the function $g_2(x)$ on the same interval is $\max_{0<\epsilon\leq1/8} (g_2(\epsilon)) = \sqrt{2}$. Since $1/\sqrt{1 - 8 \epsilon} > 1$ we can conclude that inequality (24) contradicts our initial assumption about $|V_1|$ given in the theorem formulation, and hence $|S_i \cup V_i \cup V_{i+1}| < \alpha n$ for all $i > 2$. When $i = 2$, Eq. (20) reduces to

$$|V_1| \geq \left[ g_1(\epsilon) \frac{3 + 8 \epsilon}{4} \alpha n - |C_{XOR}| \right] \frac{2}{3 - 8 \epsilon}, \tag{25}$$

which also contradicts our initial assumption. Finally, the condition $|V_1 \cup V_2| < \alpha n$ follows from the Eq. (17) and initial condition for $|V_1|$. This proves the theorem. ■

In the previous analysis we assumed that XOR gates are unreliable, but not the MAJ gates. If we allow MAJ gates to be prone to data-dependent gate failures, the error correction cannot be guaranteed. This
follows from the fact that in the worst case scenario correction of every variable can be annulled by the
MAJ logic gate failure.

Note that the decoder’s correcting capability depends not only on the expansion property of its Tanner
graph, but also on the number of XOR failures in the first iteration ($|C_{\text{XOR}}|$). For too many XOR gate
failures during the first iteration, the decoding process will not converge to a correct codeword. Recall
from the GOS error model that $|C_{\text{XOR}}|$ depends on the XOR gates failures at time instant prior to the first
decoding iteration. We do not have any control over the number of XOR gate failures before decoding
has started, but there is a practical way to overcome this, and force $|C_{\text{XOR}}|$ to be zero. Before we start
decoding a new codeword we can force all transistor-level transient processes in the decoding circuitry
to reach a stationary state, so that there are no transitions at gate outputs nor accumulated errors, prior to
the start of decoding. Practically, this can be done by slightly slowing down the clock in the first iteration
and letting the signal level stabilize. Since the clock is slower, there are no-timing errors and the XOR
computations are reliable, which yields $|C_{\text{XOR}}|=0$.

We next compare our results with the results from [28] where a reliable decoder was considered. It can
be observed that the presence of the XOR gate failures reduces the number of errors that can be tolerated
by the bit-flipping decoder. For example, when the Tanner graph has the expansion of $(7/8 + \epsilon)$, the
perfect decoder can correct $9/16\alpha n$ errors, which is two times higher than the error correction capability
of the faulty decoder. In the limiting case $\epsilon = 1/8$ the number of correctable errors is upper bounded
by $3\alpha n/8$, which is only the $3/8$ of the number of errors correctable by the decoder built from reliable
components.

The problem of explicit construction of expander graph, with the expansion arbitrary close to $\gamma$ (called
lossless expanders), was investigated by Capalbo et al. in [37], where it was shown that the required
expansion $7/8 + \epsilon$ can be achieved with graph left-degree $\gamma = \text{poly} (\log(\gamma/\rho), 8/(1 - 8\epsilon))$. This proves
the existence of a expander code that can tolerate a fixed fraction of errors under data-dependent gate
failures.

Another proof of the guaranteed error correction of LDPC codes was provided by Chilappagari et al. in [32], where the correction capability of an LDPC code was expressed in terms of girth of Tanner
graph. In the following theorem we extend the results presented in \cite{32} to the case of the noisy decoder.

**Theorem 3.** Consider an LDPC code with $\gamma$-left-regular Tanner graph with $\gamma \geq 8$ and girth $g = 2g_0$. Then, the majority logic decoder built from unreliable check nodes can correct any error pattern $|V_1|$ such that $|V_1| < 9n_0(\gamma/4, g_0)/32 - \sqrt{2}|C_{\text{XOR}}|$, where

$$n_0(\gamma/4, g_0) = n_0(\gamma/4, 2j + 1) = 1 + \frac{\gamma}{4} \sum_{i=0}^{j-1} \left(\frac{\gamma}{4}\right)^i, \ g_0 \ odd,$$

$$n_0(\gamma/4, g_0) = n_0(\gamma/4, 2j) = 2 \sum_{i=0}^{j-1} \left(\frac{\gamma}{4}\right)^i, \ g_0 \ even.$$  \hfill (26)

**Proof:** In order to prove the theorem we use the following lemma.

**Lemma 6.** The number of checks connected to a set of variable nodes $V$ in $\gamma$-left-regular Tanner graph with girth $g = 2g_0$ satisfies

$$|\mathcal{N}(V)| \geq \gamma|V| - f(|V|, g_0),$$  \hfill (27)

where $f(|V|, g_0)$ represents the maximal number of edges in an arbitrary graph with $|V|$ nodes and girth $g_0$.

**Proof:** See \cite{32}. \hfill □

Based on the Moore bound, we know that the number of nodes $n(\bar{d}, g_0)$ in a graph with the average degree $\bar{d} \geq 2$ and girth $g_0$ satisfies \cite{38}

$$n(\bar{d}, g_0) \geq n_0(\bar{d}, g_0),$$  \hfill (28)

where $n_0(\bar{d}, g_0)$ is defined in Eq. (26). On the other hand, since $\gamma/4 \geq 2$ the graph with $|V| < n_0(\gamma/4, g_0)$ nodes must have average degree smaller than $\gamma/4$. Then, based on the definition of the average degree follows

$$f(|V|, g_0) < \gamma|V|/8.$$  \hfill (29)

Combining the previous expression with Eq. (27) we obtain

$$|\mathcal{N}(V)| > 7\gamma/8.$$  \hfill (30)
Note that it was shown in [32] that $\gamma \geq 4$ represents a sufficient condition for the guaranteed error correction on a Tanner graph with girth $g$. However, due to logic gate failures higher expansions (Eq. (30)) are required compared to the perfect decoder, but the other conclusions remain the same as for the perfect decoder.

VII. Numerical Results

A. Error Probability Analysis

The codes designed from finite geometries are considered to be an important class of one-step majority logic decodable codes [39]. It was proven that for an LDPC code, derived from finite geometries, the OS-MAJ decoder can correct up to $\lceil \gamma/2 \rceil$ errors. In this section we investigate 2-dimensional affine and projective geometry LDPC codes over the Galois field $GF(2^s)$, denoted as $AG(2, 2^s)$ and $PG(2, 2^s)$ codes, $s > 0$, respectively. The affine geometry codes, $AG(2, 2^s)$, have right-degree $\rho = 2^s + 1$, left-degree $\gamma = 2^s$ and minimum distance $d_{\text{min}} = 2^s + 1$. The $PG(2, 2^s)$ code is characterized by $\rho = \gamma = 2^s + 1$ and minimum distance $d_{\text{min}} = 2^s + 2$.

The average bit error probabilities for several PG and AG codes, under the GOS error model, are presented in Fig. 1. The performance upper bounds are calculated using Eq. (9) for the case of two XOR gate error rates $\bar{\varepsilon} = 10^{-3}, 10^{-2}$ and compared to the case of $\bar{\varepsilon} = 0$, i.e., with the perfect decoder. It should be noted that lower the above bounds correspond to rare hardware failures, and can be well estimated using 

$$
\sum_{t=0}^{\gamma} \binom{\gamma}{t} B^t (1 - B)^{\gamma-t} P_v (p, \bar{\varepsilon}(t)) \approx P_v (p, (0, \ldots, 0)).
$$

This is the reason why they are omitted from Fig. 1.

It can be seen that frequent hardware failures can lead to significant performance degradation. This degradation is especially pronounced in the region with low BSC crossover probabilities. For example if $p = 10^{-3}$, extremely unreliable XOR gates (with $\bar{\varepsilon} = 10^{-2}$) can reduce the bit error rate by an order of magnitude for all presented codes. On the other hand, hardware failures corresponding to $\bar{\varepsilon} = 10^{-3}$, cause
significantly smaller performance loss. Performance loss is lower for higher \( s \), which results in negligible BER degradation for codes with \( s = 4 \), i.e., AG(2, 2^4) and PG(2, 2^4). Since \( \bar{\varepsilon} = 10^{-3} \) is considered to be a large value of the gate failure probability, the OS-MAJ decoder is in general proved to be resistant to hardware unreliability. For smaller values of \( \bar{\varepsilon} (\bar{\varepsilon} < 10^{-3}) \), the BER degradation is negligible for all the analyzed codes.

As a convenient measure of the performance variation caused by incorrect output switching, we define a *data-dependence factor*, \( F \), as the ratio of the two border BER values, given by Lemma 3 as follows

\[
F = \frac{\sum_{t=0}^{\gamma} \binom{\gamma}{t} B^t (1-B)^{\gamma-t} P_v (p, \bar{\varepsilon}(t))}{\sum_{t=0}^{\gamma} \binom{\gamma}{t} B^{\gamma-t} (1-B)^{t} P_v (p, \bar{\varepsilon}(t))}. \tag{32}
\]

The values of \( F \), for different \((\gamma, \rho)\) classes of LDPC codes, are presented in Fig. 2. It can be seen that the degradation is higher in codes with larger \( \gamma \). For example, when \( p = 10^{-3} \), for codes with \( \gamma = \rho = 5 \), the BER upper bound is more than seventy times higher than the corresponding lower bound. As error correction capability of a code increases with \( \gamma \), it is interesting to notice that the better codes are more susceptible to negative effects of hardware failures, for the same \( \rho \) value. Additionally, it can be shown that the performance loss can be reduced by increasing the degree of check nodes.
Fig. 2: The data-dependence factor values for different $(\gamma, \rho)$ classes of LDPC codes ($\varepsilon = 10^{-2}$).

B. Guaranteed Error Correction

From Theorem 2 follows that the number of errors that can be corrected depends on the expansion property, represented by $\alpha$ and $\epsilon$, and the hardware failures inherited from the time instant prior to the decoding, $|C_{\text{XOR}}|$. Here we provide an upper bound on a fraction of channel errors, $\alpha_{\text{total}} = 3(3 + 8\epsilon)\alpha/32 - \sqrt{2}|C_{\text{XOR}}|/n$, that can be corrected by the decoder. We use the following lemma to numerically obtain the upper bound.

**Lemma 7.** Let $\alpha^*$ and $\epsilon^*$ be such that $\alpha_{\text{total}}(\alpha^*, \epsilon^*) \geq \alpha_{\text{total}}(\alpha, \epsilon)$, $0 < \alpha < 1$, $0 < \epsilon \leq 1/8$. Then, they satisfy the following relation

$$\epsilon^* = (1 - (1 - \alpha^*)\rho)/\alpha^* - 7/8.$$  \hspace{1cm} (33)

**Proof:** The previous relation follows from the [28, Theorem 25], where it was shown that a set of $\alpha n$ variables can have at most $n\gamma(1 - (1 - \alpha)\rho)/\rho + O(1)$ neighbors and the fact that we look for graphs which expand by at least a factor of $(7/8 + \epsilon)$.

In Fig. 3(a) we express $\alpha_{\text{total}}(\alpha^*, \epsilon^*)$ in terms of $|C_{\text{XOR}}|/n$, for different $\rho$-right-regular Tanner graphs.
We consider only cases where $\rho \geq 8$. We can observe that, for example for $\rho = 8$, when the influence of inherited failures can be neglected, we can potentially correct more than 1% of erroneous bits. In addition, a code correction capability reduces with the increase of $\rho$. When XOR gate failures prior to the decoding become comparable with the correction capability of a code, a threshold is reached and the bound rapidly decreases. The threshold is independent of $\rho$. For sufficiently large $|C_{XOR}|/n$ the decoder performance is degraded up to the point where no error correction can be guaranteed. This happens, for example for $\rho = 8$, when $|C_{XOR}|/n \geq 1\%$.

Another perspective on the error correction of the noisy decoders is provided in Fig. 3(b). Here we examine how the girth of $\gamma$-left-regular Tanner graphs affects the decoder performance. In addition, we compare the results given by Theorem 3 with the correction capability of the noisy OS-MAJ decoder, expressed by $\lfloor \gamma/2 \rfloor - |C_{XOR}|$. It can be observed that the error correction bound, guaranteed by Theorem 3, for small girth ($g \leq 8$), is not tight. It is actually lower compared to the known OS-MAJ decoder correction capability. However, for higher girths of Tanner graphs, the results given in Theorem 3 are significant. For example, when $g = 12$, $|C_{XOR}| = 0$ and $\gamma = 12$, we can guarantee correction of error patterns with weight 7, which is not possible using the OS-MAJ decoder.
VIII. Conclusion

While the von Neumann error model is suitable for theoretical evaluation of fault-tolerant systems, applicability of the results obtained under this error model to real-world systems is limited. In practice, unreliability of logic gates is usually data-dependent and correlated in time. Hence, in order to describe hardware unreliability phenomenon more accurately, a change of modeling paradigm is required. We advocate the use of the state models, which provide a more general modeling approach. Then, based on the data-dependent gate failure model, we developed an analytical method for the performance evaluation of the OS-MAJ decoders. Our method enables calculating the BER of any regular LDPC code of girth at least six. These BER values are highly dependent on the decoded codewords and we have succeeded to bound them for the case of errors caused by the probabilistic nature of gate switching.

In addition, based on the expander properties of Tanner graphs, we established conditions required that correction capability of the majority logic decoder increases linearly with the code length. Although we were able to show that this property is achievable for codes with high left- and right-degrees, our results present the first known results regarding the guaranteed error correction of LDPC decoders made of unreliable components.

The future research includes the investigating fault-tolerant schemes which use other types of LDPC decoders, under data-dependent hardware failures. We are working on generalization of our results to more complex iterative decoders, such as, for example, finite-alphabet iterative LDPC decoders. Based on the structural property of Tanner graphs of LDPC codes, we are also investigating possibility of designing novel decoders that can work well under data-dependent hardware failures.

Appendix A (Proof of Theorem 1)

The expression given by Eq. (3) represents the miscorrection probability for an arbitrary chosen bit under one hardware failure scenario, i.e., one state array $\sigma^{(t)}$.

A particular XOR state $s_{m}^{(t)}, 1 \leq m \leq \gamma$, will appear if channel errors change only certain bits of the code sequence $x_{m,v}$. The number of such bits is equal to the Hamming distance between the error-free code sequence and the XOR state $s_{m}^{(t)}$. As the inputs of XOR gates are not mutually dependent,
the probability of the state array \( \sigma^{(t)} \) occurrence can be derived by multiplexing individual XOR state probabilities and we have

\[
P(\sigma^{(t)}) = \prod_{m=1}^{\gamma} P_{d_H} (s_{m,v}^{(t),x_{m,v}}) (1 - p)^{M(p-1)-d_H (s_{m,v}^{(t),x_{m,v}})}.
\] (34)

The error probability of a bit \( x_v^{(k)} \), under assumption that a fixed sequence of \( M \) codewords was transmitted through the channel, can be derived by summing the products \( P(\sigma^{(t)}) P_v(p, \varepsilon^{(t)}) \) obtained for all possible error vectors \( \varepsilon^{(t)}, 1 \leq t \leq 2^{(\rho-1)\gamma M} \) and the BER can be derived by performing one additional averaging over all code bits.

**APPENDIX B (The Proof of Lemma 4)**

Based on Eq. (17) we know that for \( i > 1 \)

\[
\sum_{i=2}^{\infty} (2|V_{i+1}| - K|V_i| - K|V_{i-1}|)x^i \leq 0,
\] (35)

where \( K = 1 - 8\epsilon \). The previous expression can be rewritten as,

\[
v(x)(2 - Kx - Kx^2) - (2|V_2| - K|V_1|)x + 2|V_1| \leq 0,
\] (36)

where \( v(x) \) represents the generating function defined as

\[
v(x) = \sum_{i=0}^{\infty} |V_{i+1}|x^i.
\] (37)

The function \( v(x) \) can be bound as follows

\[
v(x) \leq \frac{(2\beta - K)x + 2}{(x_1 - x)(x_2 - x)} |V_1| = \left[ - \frac{(2\beta - K)x_2 + 2}{K(x_1 - x)(x_2 - x)} + \frac{2 \beta + K}{K(x_1 - x)} \right] |V_1|
\]

\[
= \left[ \frac{(2\beta - K)x + 2}{K(x_1 - x_2)} \left( \sum_{i=0}^{\infty} x_1^{-i-1}x^i - \sum_{i=0}^{\infty} x_2^{-i-1}x^i \right) + \frac{2 \beta + K}{K} \sum_{i=0}^{\infty} x_1^{-i-1}x^i \right] |V_1|,
\] (38)

where \( x_1 = -(1 + \sqrt{1 + 8/K})/2 \) and \( x_2 = (\sqrt{1 + 8/K} - 1)/2 \). Then, we have

\[
|V_1| \leq \left[ \frac{2 + (2\beta - K)x_2}{K(x_2 - x_1)} x_2^{-i} - \frac{2 + (2\beta - K)x_1}{K(x_2 - x_1)} x_1^{-i} \right] |V_1|
\]

\[
= \frac{2 + (2\beta - K)x_2}{K(x_2 - x_1)} x_2^{-i} \left[ 1 - \frac{2 + (2\beta - K)x_1}{2 + (2\beta - K)x_2} \right] |V_1|.
\] (39)
Since for all $i > 0$ and $2\beta \geq K$

$$1 - \frac{2 + (2\beta - K)x_1}{2 + (2\beta - K)x_2} \left(\frac{x_2}{x_1}\right)^i \leq 2,$$

we finally have

$$|V_i| < \frac{4 + 2(2\beta - K)x_2}{K(x_2 - x_1)} \frac{x_2^{-i}}{x_1^{-i}}|V_1|$$

$$= \frac{4\sqrt{1 - 8\epsilon} + (2\beta - 1 + 8\epsilon)(\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon})}{(1 - 8\epsilon)\sqrt{9 - 8\epsilon}} \left(\frac{2\sqrt{1 - 8\epsilon}}{\sqrt{9 - 8\epsilon} - \sqrt{1 - 8\epsilon}}\right)^i |V_1|. \quad (41)$$

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