NeuroPack: An Algorithm-level Python-based Simulator for Memristor-empowered Neuro-inspired Computing

Jinqi Huang 1,∗, Spyros Stathopoulos 1, Alex Serb 1, and Themis Prodromakis 1

1 Centre for Electronics Frontiers, Electronics and Computer Science, University of Southampton

Correspondence*: Jinqi Huang
J.Huang@soton.ac.uk

ABSTRACT
Emerging two terminal nanoscale memory devices, known as memristors, have over the past decade demonstrated great potential for implementing energy efficient neuro-inspired computing architectures. As a result, a wide-range of technologies have been developed that in turn are described via distinct empirical models. This diversity of technologies requires the establishment of versatile tools that can enable designers to translate memristors’ attributes in novel neuro-inspired topologies. In this paper, we present NeuroPack, a modular, algorithm level Python-based simulation platform that can support studies of memristor neuro-inspired architectures for performing online learning or offline classification. The NeuroPack environment is designed with versatility being central, allowing the user to choose from a variety of neuron models, learning rules and memristors models. Its hierarchical structure, empowers NeuroPack to predict any memristor state changes and the corresponding neural network behavior across a variety of design decisions and user parameters options. The use of NeuroPack is demonstrated herein via an application example of performing handwritten digit classification with the MNIST dataset and an existing empirical model for metal-oxide memristors.

Keywords: memristor, neuro-inspired computing, neuromorphic computing, neural networks, online learning, offline classification

1 INTRODUCTION
Over the last decade, neuro-inspired computing (NIC) has experienced an immense growth, manifesting itself in a range of advances across theory, hardware and infrastructure. Theoretical NIC has proposed a very wide range of artificial neural network (ANN) configurations, such as Convolutional neural networks (LeCun et al., 1999) and LSTMs (Hochreiter and Schmidhuber, 1997) that may operate at various levels of weight and signal quantisation (Dundar and Rose, 1995) and spanning across both spiking (Wu and Feng, 2018) and non-spiking (Sengupta et al., 2019) approaches. Evidently, this design process comprises multiple decision points that overall renders a very substantial and complex design space.

Simultaneously, research on novel hardware technologies has developed along multiple strands including fully digital architectures (Davies et al., 2018; Akopyan et al., 2015; Painkras et al., 2013), supra-threshold (Schmitt et al., 2017) and sub-threshold (Benjamin et al., 2014) analogue architectures, with some more recent contenders (Burr et al., 2016) utilising post-CMOS electronic components
called "memristors" (Chua, 1971). This latter category is the focus of this work. Fundamentally, memristive devices are electrically tuneable (non-linear) resistors which have shown great promise at efficiently implementing the most numerous components found in neural networks: the synapses and mapping of their weights. Memristors feature the potential for extreme downscaling (Khiat et al., 2016), back-end-of-line (BEOL) integrability (Xia et al., 2009), sub-ns switching capability (Choi et al., 2016) and very low switching energy (Goux et al., 2012). Multiple families of memristive devices have been developed exploiting different electrochemical effects ranging from atomic-level effects in metal-oxides (Prodromakis et al., 2010) and atomic switches (Aono and Hasegawa, 2010), to bulk crystallisation/amorphisation effects in phase-change memory devices (Bedeschi et al., 2009) and magneto-resistive effects in Spin-Torque-Transfer (STT) devices (Vincent et al., 2015), to name a few. Each of these families features its own idiosyncrasies in terms of electrical behaviour and correspondingly are described via distinct empirical models.

The broad interest in employing memristors within neuro-inspired hardware mainly stems from their Multi-bit storage (Stathopoulos et al., 2017) capability and their simple architecture that can be tessellated in large arrays (Sivan et al., 2019). Those excellent features make memristors good candidates for multiply-accumulate operations (Serb et al., 2017) required in in-memory computing (IMC) applications. Moreover, the intrinsic properties of memristors are similar to those of biological synapses (Serrano-Gotarredona et al., 2013). Inspired by this fact, designs such as Serb et al. (2016) and Covi et al. (2016) successfully applied memristors as synapses in online learning with spike-timing-dependent-plasticity (Markram et al., 1997), which is a learning rule inspired from biological NNs. Memristors have also been employed as components for NIC, from offline classification (Yao et al., 2020) to online learning (Payvand et al., 2020). Along these lines, software-based simulation platform designed for memristor-based neuromorphic systems become significant for fast validation of design ideas and predicting device behaviour.

Current simulators (e.g. MNSIM (Xia et al., 2018) and NeuroSim (Chen et al., 2018)) focus more on circuit-level designs, serving as tools either to simulate the behaviour of different hardware modules, or to estimate the performance of memristor-based neuromorphic hardware in integrated circuit designs. Sitting at a higher level of abstraction would be an "algorithm-level device-model-in-the-loop" simulator (or "algo-simulator" for short) designed to test functionally defined (as opposed to explicitly designed) circuits with memristive device models at algorithm level, e.g. performing specific online or offline learning tasks with memristors as synapses in spike-based NNs. Such tool would allow fast verification of design concepts before serious hardware design effort is committed, in essence answering the question: Is my design likely to function given knowledge on my memristive devices, assuming the rest of the circuit functions flawlessly? If yes, work can proceed to the next stage.

In this paper, we present NeuroPack: a simulator for memristor-based neuro-inspired computing at algorithm level. NeuroPack is a complete, hierarchical framework for simulating spiking-based neural networks, supporting various neuron models, learning rules, memristor models, memristor devices, neural networks, and different applications. Written in Python, it can be easily extended and customised by users, as will be shown. NeuroPack also integrates an empirical memristor model proposed by (Messaris et al., 2017b). Between processing algorithms and setting & monitoring memristor states, there is the significant step of applying a pulse of specific voltage and duration to trigger a memristor state change corresponding to some desired weight change calculated from learning rules. NeuroPack integrates a module to convert desired weight changes to estimated stimulation pulse parameters for bridging this gap. In terms of applications, we use NeuroPack to demonstrate image classification on MNIST dataset in our 'Results'
Figure 1. NeuroPack workflow. The system reads three configuration files: connectivity matrix, (neural) stimuli and config. The memristor model is embedded within the virtual memristor array, which initialises a number of memristor devices according to instructions in the configuration and connectivity matrix files. Neuron models and learning rules are placed in the core file. In “updating fire history” stage, there are three separate steps: calculating fire states assuming neurons fire ‘freely’; adding network-level constraints; and updating the fire history matrix. "Calculating ΔW" is supported by most learning rules except STDP. By replacing the core file, users can apply different neuron models and learning rules.

section. We also give result analysis for systems with different R tolerance, a parameter used in weight updating, and two biasing methods as examples to showcase that NeuroPack assists users to investigate how key design, device and architectural factors affect memristor-based neuromorphic computing systems. Finally, NeuroPack includes a built-in analysis tool with a user-friendly graphic user interface (GUI) for visualising and processing classification results. The main contributions of this work include:

1. Developing an algo-simulator for memristor-powered neuro-inspired computing with selectable neuron and device models, as well as learning rules.
2. Modelling memristor state changes in neuro-inspired computing tasks given user-defined memristor parameters.
3. Converting expected weight changes prescribed by learning rules into parameters of bias pulses used for triggering memristor state changes in weight updating.

The rest of the paper is organised as follows: in section 2 we introduce the architecture of NeuroPack with core parts and the workflow. Section 3 demonstrates an example application of handwritten digit recognition in MNIST dataset performed in NeuroPack and section 4 summarises the paper.

2 METHODS

2.1 Design Overview

NeuroPack is designed for predicting the outcomes of online learning or offline classification tasks under selectable neuron, plasticity and memristive device models, as well as for triggering and monitoring
memristor state changes. To achieve those two tasks NeuroPack’s workflow (see Figure 1) is divided into five parts: input file handling, virtual memristor array, neuron core, plasticity core, and analysis tool.

For input data handling, there are three input files that need to be generated from users: configuration file, connectivity matrix file, and stimuli file. The configuration file contains the main parameters for building up NNs (e.g. network size, NN depth, number of neurons for each layer etc), setting up neuron models (e.g. leakage, noise scale etc), and initialising memristor devices (e.g. up and bottom boundaries for memristor resistance). The connectivity matrix file is used to define neuron connectivity and to map synapses to virtual memristors. The stimuli file stores both input signals and output labels. When loaded in the NeuroPack main panel, input signals and output labels are split by checking if the neuron is an output neuron using the information provided by the configuration file.

We now walk through the procedure for carrying out a classification task in a spiking network. First, the input signals to the neuron model are converted to spikes and saved in the stimuli file. Training and test datasets are loaded separately. At each time step an input neuron can either be spiking (1) or silent (0). Next, the neuron core reads out the resistive states (RS) from a virtual memristor array, and calculates internal variables, such as membrane voltages, according to the selected neuron model. The new fire states are then calculated in two steps: firstly considering whether neurons are supposed to fire by checking if the membrane voltages surpass the threshold, and secondly adding network-level constraints (for example winner-take-all networks). When the current input stimuli belong to a training dataset, inference results are sent to the plasticity core to trigger weight update as per selected learning rule. When the test dataset is processed, plasticity updates are skipped.

Weight updates happen during the plasticity phase. For STDP, long-term potentiation (LTP) or long-term depression (LTD) “events” are directly applied to memristor devices based on a calculation taking nothing into account except for spike timing information. For other learning rules other types of information may be necessary. These can be made available to the system configuration file. Importantly, there are two main conceptual ways of specifying plasticity events. The simpler way is to create a function that maps plasticity-relevant variables directly to pulsing parameters. Thereafter the physics of the memristor (correspondingly the response of the memristor model) will determine the actual resistive state change, which in turn will be reflected into a weight change via a resistance-to-weight mapping function. The more complex route involves mapping plasticity-relevant variable configurations to a requested weight change, and then searching the device model (a model is necessary for this approach) for a solution predicting that some set of pulse parameters will result in the required change. The same process will be repeated for the given number of epochs. Inference results as well as internal variable and parameters, including membrane voltages, fire history, and weights, can be sent to the built-in analysis tool for further visualisation and analysis.

2.2 Neuron Models and Learning Rules

Neuron models and learning rules are placed in “neuron core” and “plasticity core” respectively in Figure 1. For some learning rules, such as backpropagation which requires calculation of error gradients, the equations depend on the neuron model. Therefore, neuron models must be treated as first-class objects. However, a simpler solution implemented in this tool is to ensure that each learning rule is paired with one neuron core and be placed together in the same “core” document. NeuroPack provides four example core files: leaky-integrate-and-fire neuron (LIF) (Abbott, 1999) with STDP, leaky-integrate-and-fire neuron with backpropagation (BP) (Rumelhart et al., 1986), Tempotron (Gütig and Sompolinsky, 2006), Izhikevich neuron (Izhikevich, 2003) and direct random target projection (DRTP) (Frenkel et al., ...
Other neuron and plasticity rules can be customised according to users’ needs by simply using existing example cores as standard templates and introducing user-defined cores. In this section, we provide one specific example, where we use a LIF neuron model and BP, to implement a fully-connected multi-layer spiking neural network with winner-take-all functionality (Oster et al., 2009).

### 2.2.1 Leaky-integrate-and-fire neuron and Back-propagation

Leaky-integrate-and-fire (LIF) is a simple and relatively computationally friendly neuron model. Most neuromorphic accelerators, with (e.g. Guo et al. (2019)) or without memristors (e.g. Merolla et al. (2011); Yin et al. (2017)), use LIF neurons. LIF has been implemented in NeuroPack using the equations below adapted from the differential form (Gerstner et al., 2014) by assuming discretised time steps:

\[
V_t = \sum W x_t + \alpha V_{t-1} (1 - y_{t-1}) \\
y_t = h(V_t - V_{th})
\]  

(1)

Where \(V_t\) represents membrane voltage at time \(t\), \(W\) is the weight, \(x_t\) is incoming spike to the neuron (considered as 1 or 0), \(\alpha \in [0, 1]\) is a leakage term, \(y_t\) is the output spike, \(h(x)\) is the step function and \(V_{th}\) is the neuron threshold. The equations describe that the neuron membrane voltage at any time step is determined by two parts: the weighted sum of incoming spikes at this time step and the membrane voltage at the last time step. If the membrane voltage surpasses the threshold, a spike is generated and the membrane voltage is reset. The cost function \(E\) at time step \(t\) is then given by:

\[
E(t) = \frac{1}{2N} \sum_{i=0}^{N} (y_{i,t} - \hat{y}_{i,t})^2
\]  

(2)

where \(N\) is the number of output neurons, \(i\) is the output neuron index, and \(\hat{y}_{i,t}\) is the correct firing state of output neuron \(i\) at time step \(t\). Finally, weight changes are given by:

\[
\Delta W_k = -\eta \delta_{k,t} x_{k,t}^T \\
\delta_{k,t} = \begin{cases} 
\frac{1}{N} (y_{k,t} - \hat{y}_{k,t}) \odot h'(V_{k,t} - V_{th}) & \text{if } k = K \\
(W_{k+1,t} \delta_{k+1,t}) \odot h'(V_{k,t} - V_{th}) & \text{otherwise}
\end{cases}
\]  

(3)

where \(\eta\) is the learning rate, \(k\) is the layer index, and \(K\) is the number of layers. \(W_k\) gives the weight matrix between layer \(k - 1\) and \(k\). \(\odot\) means element-wise multiplication. \(\delta\) gives the error back-propagated from output neurons. The step function \(h(V_t - V_{th})\) is discontinuous, so the derivation is replaced by noise as suggested in Lee et al. (2016). For the full derivation, please refer to supplementary material. We note that the only potentially problematic variable is \(\hat{y}_{i,t}\) which is provided in stimuli file; everything else is accessible directly to NeuroPack.

### 2.2.2 Adding winner-take-all functionality

We now introduce winner-take-all (WTA) functionality, which constrains the output layer to have at most one firing neuron at each time step. This is done by adding one softmax layer and making the neuron that has the largest softmax result fire:
\[ S_t = \text{softmax}(V_t \odot y_t) \quad (4) \]

The cost function correspondingly needs adjusted by taking a cross-entropy form:

\[ E = - \sum_{i=0}^{N} \hat{y}_{i,t} \ln(S_{i,t}) = -\ln(S_{j,t}) \quad (5) \]

Where \( j \) is the index of the output neuron that should fire. Based on new cost function, weight changes are calculated as:

\[ \Delta W_k = -\eta \delta_{k,t} x_{k,t}^T \]

\[ \delta_{k,t} = \begin{cases} 
(S_t - \hat{y}_t) \odot (y_t + V_t \odot h'(V_{k,t} - V_{th})) & \text{if } k = K \\
(W_{k+1,t}^T \delta_{k+1,t}) \odot h'(V_{k,t} - V_{th}) & \text{otherwise}
\end{cases} \quad (6) \]

as before application of WTA, all variables are accounted for; the freshly introduced softmax can be computed entirely within the same core file by simply adding network-level constraints. For the full derivation, please refer to supplementary material.

In summary, to configure a multi-layer spiking neural network with WTA using LIF neurons with BP in NeuroPack, parameters including learning rate, noise scale, threshold and leakage are loaded from the configuration file. Input spikes encoded from stimuli files are fed to the "neuron core" in the core file. The "neuron core" reads the memristor states from the device array, calculates membrane voltages, and updates fire history during the inference phase. If training is enabled, inference results, ground truth information as well as internal variables are loaded into the "plasticity core" which then adjusts the memristive weights according to calculated weight changes, precisely as summarised in Figure 1.

2.3 Memristor Model

When using virtual memristive devices, as is the case in Figure 1, a memristive model has to be used for predicting memristor RS as a function of read-out voltage and RS changes in response to plasticity events. Here we use an empirical memristor model proposed by Messaris et al. (2017b), but other user-defined models are also compatible with NeuroPack. With different values of parameters, this model has shown flexibility to model large ranges of memristor devices. The model expresses RS switching rate \( \frac{dR}{dt} \) as a function of initial RS and biasing voltage. The switching rate equation is reproduced here for convenience:

\[ \frac{dR}{dt} = m(R, v) = \begin{cases} 
A_p(-1 + e^{\frac{v}{t_p}})(r_p(v) - R)^2 & \text{if } v > 0, R < r_p(v) \\
A_n(-1 + e^{\frac{v}{t_n}})(R - r_n(v))^2 & \text{if } v \leq 0, R \geq r_n(v)
\end{cases} \quad (7) \]

where \( A_n \) and \( A_p \) are scaling factors. The \( (e^{\frac{v}{t_{p,n}}}) - 1 \) term marks the main, exponential dependency of the switching rate on bias voltage with \( t_n, t_p \) as fitting parameters extracted during modelling. Next, the last term encapsulates the dependence of the switching rate on the current resistive state with the aid of fitting parameters \( a_{0p}, a_{1p}, a_{0n}, a_{1n} \). The main effect here is that the closer the RS is to the upper (lower) limit, the harder it is to continue pushing it further up (down), implementing "RS saturation".
Finally, \( r_{p,n}(v) \) is a simple, 1st order polynomial helper function that helps capture the exact nature of the switching rate’s dependency on current RS:

\[
r(v) = \begin{cases} 
  r_p(v) = a_{0p} + a_{1p}v & \text{if } v > 0 \\
  r_n(v) = a_{0n} + a_{1n}v & \text{if } v \leq 0 
\end{cases}
\]

Whilst models may take different forms (e.g. charge-flux models (Shin et al., 2010)), the fundamental condition that is observed is that the device model is always fed a series of time-wise discretised voltages and then must be able to calculate current and change in resistive state. Models that by default take current inputs are presently not supported. \( dt \) is treated as a pre-defined, fixed parameter and remains constant throughout simulation in the current implementation. NeuroPack organises memristor model instances in a virtual array with user-defined parameters as inputs by using a class \texttt{ParametricDevice(*args)} to create a device object and methods \texttt{initialise(R)} and \texttt{step_dt(V, dt)} in the same class to set the current resistance and send a pulse with magnitude of \( V \) and pulsewidth of \( dt \) to the memristor device correspondingly. "Virtual memristor array” also provides methods such as \texttt{read(w,b)} and \texttt{pulse(w, b, v, pw)} to read the RS of the device at a given wordline \( w \) and bitline \( b \) address within the virtual array and apply a pulse with magnitude of \( v \) and pulse-width \( pw \) to the device at said address correspondingly. It is these functions that neuron models and learning rules in the core files use to access memristor RS and trigger RS change. Using model parameter sets from different types of devices (different stacks or even devices with different underlying electrochemical mechanisms), as well as varying the parameters of the model in an exploratory fashion are great tools to gain an understanding of how different memristive devices can influence the outcome of basic machine learning algorithms.

### 2.4 Weight Mapping and Updating

Most memristor-based neuromorphic designs (e.g Hu et al. (2018) and Li et al. (2018)) store weights as memristor conductance and apply incoming inputs as voltages across memristors, so that the multiplication results can be easily attained by measuring the current according to Ohm’s law. Therefore, weights are mapped linearly to memristor conductance by default in NeuroPack, but users are allowed to define other mapping methods if needed. However, memristor being nonlinear devices, obtaining well-controlled weight changes is challenging because the resistive state after application of a triggering pulse depends both on the current resistance state and biasing parameters (typ. pulse voltage and duration). To deal with this issue, NeuroPack includes a module for calculating biasing parameters, expected to produce the desired weight changes. In this module, inputs are memristor model parameters for initialising a memristor device, current state, target state, \( dt \), and a list of tuples, each of which contains magnitude and pulsewidth to represent a pulse.

Inside the module, a \texttt{ParametricDevice} object is created by passing memristor model parameters. Resulting resistance for each set of pulse parameters is calculated by calling \texttt{step_dt(V, dt)} method. After all resulting resistance values are attained, distance to the resistance expected to be written to memristors is calculated, and the set of parameters that lead to shortest distance will be selected. The pseudo code of this module has be included in supplementary material.

The weight update scheme using the pulse parameter selection module is as follows: to begin with, user-defined R-tolerance, which is defines as the maximum \( \frac{R_{\text{new}}-R_{\text{expected}}}{R_{\text{expected}}} \) that NeuroPack assumes the device state has converged, and maximum updating steps are loaded in NeuroPack. After calculating the target resistance for a device, actual resistance is read and the resulting value is used as the initial resistance.
in the pulse parameter selection module. After attaining the set of parameters that will lead to closest resistance a pulse is sent and the new resistance is read. This predict-write-verify process is repeated until the calculated $\frac{R_{\text{new}} - R_{\text{expected}}}{R_{\text{expected}}}$ is smaller than the R-tolerance or the maximum step number is reached.

2.5 Customisation, usage scenarios and interface

With Python as programming language, NeuroPack can be flexibly customised at both algorithm level and device level. At algorithm level, NeuroPack can apply user-defined neuron models and learning rules. As it is shown in Figure 1, neuron core and plasticity core are placed in the same core file. In NeuroPack there are four example core files which will be explained in details in the next section. By writing and selecting user-defined core files, users can apply any customized neuron models and plasticity rules. At device level, users can easily set and change memristor parameters to describe different device characteristics.

There are two main usage scenarios for NeuroPack. One is as a supporting tool to explore how different parameter values and settings affect classification performance in NIC tasks (Figure 2 (A)). In this scenario, Users can load parameters in the configuration file with different values to monitor how memristor devices behave differently, or to investigate how classification accuracy or error rate is affected. Another usage scenario is to use NeuroPack to test and validate NN algorithms, including neuron models and learning rules (Figure 2 (B)). In this scenario, a user-defined core file or an example template is loaded to perform NN simulations. Users can then quickly test the algorithm and validate the idea by visualising and displaying memristor device state and other NN key variables (such as membrane voltage).

The visualisation and analysis tool in NeuroPack provides a user-friendly GUI to display inference results. This tool is separated from the main panel of NeuroPack. When executing a classification task, NeuroPack saves variables in every epoch including membrane voltages, input stimuli, fire history, output errors, weights as measured from the memristors, etc in a Numpy (.npz) file. Array-related variables such as weights are displayed in a color map, and neuron-related variables, for example membrane voltages and fire history, are visualised in curves to show the changing tendencies.

3 RESULTS

We use an MNIST handwritten digit recognition task as an example application to validate NeuroPack. Original images with $28 \times 28$ pixels from the MNIST dataset have been cropped to $22 \times 22$ and binarised.
Figure 3. Image recognition task with TiOx memristor-based neural network simulation in NeuroPack. (A) Binary handwritten digits from MNIST dataset cropped to $22 \times 22$. Dark blue and yellow represent weights 0 and 1 respectively. (B) - (D) Conductance sets before training (B), after 2000 epochs (C) and after 10000 epochs (D). Conductance spans from 0.0000869S to 0.0004416S, indicating final memristor RSs ranging from around 2264 ohms to 11507 ohms. (E) Concept diagram of spiking neural network used in this image recognition task. In practice the network is fully connected. $22 \times 22$ -pixel images are unrolled to 484-bit input sending to 484 input neurons correspondingly as input spikes. In this task, a two-layer network with 484 input neurons and 10 output neurons is applied. (F) Accuracy curves over the training process for both memristor version and non-memristor version. Minibatch size of 100 are used to calculate the accuracy changes during the training. Provided 2000 images from a separated test set, memristor version and non-memristor version achieved accuracy of 82.00% and 83.55% respectively. (see input images for 10 digits in Figure 3(A)). Background pixels and digit pixels are represented as 0 and 1 respectively. A single image is unrolled to a 484-dimensional vector with 0 and 1 only to be sent to input neurons in parallel. The spike encoding scheme sends a spike when the input bit is 1, and no spike...
The neural network used in this task is a 484-input 10-output two-layer feedforward winner-take-all spiking neural network with leaky-integrate-and-fire neuron model and gradient descent learning rule (see Figure 3(E) for neural network architecture for this task). To map all 484×10 synapses, a 100×100 array of memristors is used. The network was trained for 10000 epochs before being fed with 2000 test images to evaluate classification accuracy. Parameters used in NeuroPack for MNIST handwritten digit classification task can be found in Table 1. Memristor parameters listed in table are based on the extraction method from (Messaris et al., 2017a) and devices presented in (Stathopoulos et al., 2017), given voltage range from 0.9V to 1.2V for positive bias and from -0.9V to -1.2V for negative bias with 11kΩ as initialised resistance. Therefore, pulse options used to update memristors are all within those ranges. The model yielded an estimated memristor operating range between 2.23-12.8kΩ given bias voltage of ±1.2V and 12.5-18.9kΩ given bias voltage of ±0.9V. The resulting conductance caused by the bias voltages of ±0.9V-±1.2V is $5.3 \times 10^{-5}$-$4.48 \times 10^{-4}$S. To make sure the weights can be mapped to range [0, 1], the linear mapping between memristor conductance and weights is given by the equation as below:

$$W = 2.53 \times 10^3 \times G - 0.1337$$

Before training, memristor RSs are initialised to 11kΩ with a maximum variation of ±500 Ω. Memristor initial RSs are mapped to small weights close to the bottom boundary of the operating range, given conductance as the linear mapping of synaptic weights. Conductance sets before training, after 2000 epochs, and after 10000 epochs can be found in Figure 3(B)-(D). During training, conductance associated with digit pixels and labelled output neurons will be increased gradually, while other conductance stay small, therefore targeted digits show up in the conductance sets along the training process. The weight sets show the same tendency as the mapping is linear. Figure 3(F) shows the accuracy evolution curve during training with minibatch size = 100. 2000 images from a separated test set were fed to the network after training, and 1640 out of 2000 got classified correctly, giving general inference accuracy of 82.00%. The baseline given by the version storing weights directly without using memristor models achieved a test accuracy of 83.55%, which indicates the accuracy bottleneck is not the memristor model.

We now use NeuroPack to illustrate how the intimately device- and programming protocol-related issue of selecting an appropriate R-tolerance affects recognition accuracy. Figure 4(A) and (B) shows the training accuracy curves and test set accuracy results for different R-tolerance values. When R-tolerance is small (within 1%), the accuracy is not affected significantly. With a larger R-tolerance, training accuracy increases initially but then starts to drop. This is also reflected in the corresponding test set accuracy. To investigate the causes, we look into the resistance changes in both stimulated and non-stimulated synapses with different R-tolerance values, as displayed in Figure 4(C). The red line shows the baseline virtual resistance values calculated according to the weight mapping scheme for a stimulated synapse (specifically the one between input neuron 250 and output neuron 6) as yielded by a non-memristor, software synapse. The baseline shows a gradual decrease tendency through out the whole 10000 training epochs. In contrast, resistance update with different R-tolerance values cuts off increasingly early as R-tolerance increases: for 0.1%, 1%, 2%, and 3% saturation occurs roughly at epochs ~ 9000, 7000, 1000, and 100 respectively. Intuitively speaking, if we use a smooth, continuous curve to fit the baseline trace, we find that its gradient progressively decreases. This can be explained by the decreasing gradient of the cost function during the training process. This indicates that the required resistance changes between successive time steps reduce as training continues. Meanwhile, R-tolerance is defined as $\frac{R_{\text{new}} - R_{\text{expected}}}{R_{\text{expected}}}$ in NeuroPack, therefore it can be regarded as the cut-off ratio of memristor RS change. In other words, when resistance change between
two time steps is smaller than the R-tolerance, the resistance update stops. Therefore, the larger the R-tolerance, the earlier memristor RSs stop updating. Figure 4 (D) - (H) shows the memristor RS sets before training (D), after 1000 epochs (with R tolerance of 2% (E) and 0.1% (F), and after 10000 epochs (with R tolerance of 2% (G) and 0.1% (H)). There are three color regions that can be clearly seen: blue (high resistive range), white (middle resistive range), and red (low resistive range). Before training, memristor RSs are initialised to the high resistive range. After 1000 epochs, both versions with R tolerance of 2% and 0.1% with show distinguishable high and middle resistive ranges, reflecting the increasing training accuracy before 1000 epochs in Figure 4 (A). After 10000 epochs, the version with R-tolerance of 0.1%
clearly displays high, middle, and low resistive regions, while low resistive region is merged to middle region in version with R-tolerance of 2% because the cut-off of a too large R-tolerance. The version with R-tolerance of 2% is not able to distinguish specific images when middle region becomes larger as stimuli from different digits will all be assigned to weights with middle values. Therefore, the accuracy curves for large R-tolerance display decreasing tendency after certain points in Figure 4(A).

Finally, we present a comparison between two biasing schemes: a) bias voltages are only applied to selected devices (corresponding selector-based crossbar array) scenarios, and b) half-bias voltages are also applied to unselected devices in the same bitlines and wordlines (as in selectorless crossbars). Figure 5(A) shows the accuracy of both versions. In the training accuracy curves, both versions show the same tendency with a noticeable gap in between. The test accuracy bar chart further displays the \(~20\%) gap. In order to explore the cause of the accuracy gap, we look into the resistance change curves of memristors representing a stimulated synapse (between input neuron 250 and output neuron 6) and a non-stimulated synapse (between input neuron 10 and output neuron 6). The baseline curves (red) are given by virtual resistance values of the baseline which stores weights directly without using memristor
models. The resistance change for the stimulated synapse in the selector-based version (dark blue trace) shows the same decreasing tendency as the baseline (red), while the resistance in the selectorless version (orange) displays an increasing tendency. Zooming into epochs 0 to 200, we observe unexpected resistance increases when no resistance update should happen for the selectorless scenario. This is because some memristors representing synapses connected to the neurons that are not supposed to fire have been applied pulses to increase the weights according to the learning rule, and they shared the same wordlines or bitlines with those whose resistance are supposed to decrease. A cycle of half-voltage bias only caused a trivial resistance increment, but there were many cycles of unexpected resistance drop happening in the same time step as there were many devices in the same wordlines/bitlines, therefore the resistance increment accumulated and caused a large gap to the baseline. For the non-stimulated synapse, both the selector-based (purple) and the baseline (green) traces stay around their initial values throughout the whole training phase, whilst unexpected resistance increases occur in the selectorless version. However, the resistance in memristors representing the stimulated synapse is still slightly smaller than that of the non-stimulated synapse in the given examples in the selectorless scenario. Because of this slight resistance difference, the NN based on selectorless array is still able to learn images and classify correctly in some cases. We present the memristor resistive states before and after training for both versions in Figure 5 (C) - (E). Due to the half-voltage bias, the new memristor operation range changes to \(2.23k-28k\Omega\), giving the new conductance range from \(3.57 \times 10^{-5} S\) to \(4.48 \times 10^{-4} S\). Therefore, the linear mapping from conductance to weights now is changed to the equation below:

\[
W = 2.42 \times 10^3 \times G - 0.0866
\]

Memristor RSs are initialised as \(\sim11k\Omega\) before the training. After 10000 epochs, the resistive states of stimulated memristors in selector-based array (Figure 5 (D)) decrease to low resistive range (\(\sim2.26k\Omega\)), while the non-stimulated stay in high resistive range (\(\sim11k\Omega\)). In the selectorless version, stimulated memristor RSs increase to very high resistive range (\(\sim18k\Omega\)) with non-stimulated ones increasing even higher to (\(\sim22k\Omega\)). Thus, NeuroPack has helped us uncover the perhaps surprising result that even in the presence of invasive unexpected weights update the NN is still capable of distinguishing the MNIST digits substantially better than chance, albeit with a very different weight distribution than the selector-based network.

4 CONCLUSION

In this paper, we presented NeuroPack, a versatile algorithm-level software emulator for memristor-based neuro-inspired computing systems. NeuroPack allows users to customise the simulator at both system level and device level. This platform can work as a standalone tool to emulate neuro-inspired computing with different neuron models, learning rules, memristor models, different types and numbers of memristor devices, different neural network architectures, and different applications. We further showcased an application example using NeuroPack to simulate a two-layer SNN for handwritten digit recognition with the MNIST dataset. We explored how different factors such as R-tolerance in weight updating and biasing methods in different array structures affect system classification accuracy and quickly reached two conclusions: a) That even a surprisingly lax 1% tolerance in resistive state (an engineering parameter) allows for sufficient training efficiency to closely match the performance of an ideal model for this architecture and dataset. This indicates that memristor-based systems may be able to achieve competitive performance without requiring expensive precision circuits are least in some scenarios. b) That even in a scenario with unexpected weight updates due to the half-voltage biasing method in selectorless
Table 1. Parameters used in NeuroPack for MNIST handwritten digit classification task.

|                | Value                                  |
|----------------|----------------------------------------|
| **Global settings** |                                         |
| array size     | 100×100                                |
| array type     | with selectors                         |
| read noise     | 0.1%                                   |
| **Neuron model** |                                         |
| threshold      | 25.16 or 24.16(for biasing method comparison only) |
| leakage        | -0.3                                   |
| **Learning rule** |                                         |
| learning rate  | 3.5 × 10^{-6}                          |
| noise scale    | 10^{-6}                                |
| **Memristor model** |                                         |
| $A_p$          | 0.21389                                |
| $A_n$          | -0.81302                               |
| $\tau_p$      | 1.6591                                 |
| $\tau_n$      | 1.5148                                 |
| $a_{0p}$       | 37087                                  |
| $a_{0n}$       | 43430                                  |
| $a_{1p}$       | -20193                                 |
| $a_{1n}$       | 34333                                  |
| **Weights updating** |                                         |
| voltage        | ±0.9, ±1.1, ±1.2, ±1.2, ±1.2, ±1.2     |
| pulsewidth     | 10^{-6}, 10^{-6}, 10^{-6}, 5 × 10^{-6}, 10^{-5}, 5 × 10^{-5} |
| R tolerance    | 0.1%                                   |
| max update steps| 5                                      |

arrays it may be possible to decode useful information from the state of the system after training. These investigations illustrate the role NeuroPack can play in assisting users to design and validate neuro-inspired concepts and improve system performance involving emerging nanoscale memory technologies. We envisage that by varying datasets, biasing and other experimental parameters, device technology and connectivity patterns, users from across the community will be able to use this tool to generate the results that suit their needs quickly and efficiently.

**CONFLICT OF INTEREST STATEMENT**

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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**DATA AVAILABILITY STATEMENT**

The original code of this work can be found in https://github.com/hjq310/NeuroPack.
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Supplementary Material

1 DERIVATION OF BACK PROPAGATION FOR LEAKY INTEGRATE-AND-FIRE NEURON MODELS (WITHOUT WINNER-TAKE-ALL)

Leaky integrate-and-fire neuron model in matrix form:

\[ V_t = W x_t + \alpha V_{t-1} \odot (1 - y_{t-1}) \]
\[ y_t = h(V_t - V_{th}) \]
\[ E = \frac{1}{2N} \sum_{i=0}^{N} (y_{i,t} - \hat{y}_{i,t})^2 \]
\[ \Delta W = -\eta \frac{\partial E}{\partial W} \]

Where \( V_t \) is membrane voltage vector in the selected layer at time \( t \) with the size of \( n \times 1 \) (\( n \) is the total number of neurons in this layer), \( x_t \) is the input signals fed to selected layer at time \( t \) with the size of \( m \times 1 \) (\( m \) is the total number of neurons in last layer), \( W \) represents the weight matrix between current current layer and the last layer with the size of \( n \times m \), \( \alpha \) is the leakage factor, \( \odot \) means the element-wise product, \( V_{th} \) is the membrane voltage threshold, \( y_t \) is the output vector for the selected layer with only 0 and 1 to indicate if there is a spike generated with the size of \( n \times 1 \), and \( \hat{y}_t \) is the correct output state for output layer with the same size of that of the output layer, \( E \) is the cost function calculating the distance between \( y_t \) in the output layer and \( \hat{y}_t \), \( N \) is the number of output neurons, and \( \Delta W \) gives the weight update matrix with the same size as that of \( W \).

According to chain rule, \( \frac{\partial E}{\partial w_{l,t}} \) for the output layer can be derived as below:

\[ \frac{\partial E}{\partial w_{l,t}} = \frac{\partial E}{\partial y_{l,t}} \cdot \frac{\partial y_{l,t}}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l,t}} \]
\[ = (y_{l,t} - \hat{y}_t) \odot h'(V_{l,t} - V_{th}) \cdot x_{l,t}^T \]
\[ = \delta_{l,t} x_{l,t}^T \text{ let } \delta_{l,t} = (y_{l,t} - \hat{y}_t) \odot h'(V_{l,t} - V_{th}) \]

After that we can back propagate the error from output layer:
\[ \frac{\partial E}{\partial w_{l-1,t}} = \frac{\partial E}{\partial y_{l,t}} \cdot \frac{\partial y_{l,t}}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l-1,t}} \]

\[ = (y_{l,t} - \hat{y}_l) \odot h'(V_{l,t} - V_{th}) \cdot \frac{\partial V_{l,t}}{\partial W_{l-1,t}} \]

\[ = (W_{l,t}^T \delta_{l,t} \odot h'(V_{l-1,t} - V_{th})) x_{l-1,t}^T \]

\[ = \delta_{l-1,t} x_{l-1,t}^T \text{ let } \delta_{l-1,t} = (W_{l,t}^T \delta_{l,t} \odot h'(V_{l-1,t} - V_{th})) \]

Therefore, the weight update matrix \( \Delta W \) can be expressed as follow:

\[ \Delta W_k = -\eta \delta_{k,t} x_{k,t}^T \]

\[ \delta_{k,t} = \begin{cases} \frac{1}{N} (y_{k,t} - \hat{y}_l) \odot h'(V_{k,t} - V_{th}) & \text{ if } k = K \\ (W_{k+1,t}^T \delta_{k+1,t}) \odot h'(V_{k,t} - V_{th}) & \text{ otherwise} \end{cases} \]

Where \( K \) is the index of the output layer.
2 DERIVATION OF BACK PROPAGATION FOR LEAKY INTEGRATE-AND-FIRE NEURON MODELS (WITH WINNER-TAKE-ALL)

To have winner-take-all network-level restriction to only allow at most one neuron to fire at each time step, a softmax layer is added to the previous output layer:

\[ S_t = \text{softmax}(V_t \odot y_t) \]

Where \( S_t \) is a vector with the size of \( N \times 1 \). With the new output representation becoming continuous values, we apply cross entropy loss as the cost function:

\[ E = -\sum_{i=0}^{N} \hat{y}_{i,t} \ln(S_{i,t}) = -\ln(S_{j,t}) \]

Where \( j \) is the index of the output neuron that should fire according to the ground truth.

Therefore, the derivation of the gradient for the output layer is as below:

\[
\frac{\partial E}{\partial w_{l,t}} = \frac{\partial E}{\partial S_t} \cdot \frac{\partial S_t}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l,t}} \\
= \frac{\partial E}{\partial S_t} \cdot \frac{\partial S_t}{\partial Z_{l,t}} \cdot \frac{\partial Z_{l,t}}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l,t}} \quad \text{let } Z_{l,t} = V_{l,t} \odot y_{l,t} \\
= (S_t - \hat{y}_t) \odot (y_{l,t} + V_{l,t} \odot h'(V_{l,t} - V_{th}) x_{l,t}^T \\
= \delta_{l,t} x_{l,t}^T \quad \text{let } \delta_{l,t} = (S_t - \hat{y}_t) \odot (y_{l,t} + V_{l,t} \odot h'(V_{l,t} - V_{th}))
\]

From the output layer results, we can back propagate the errors and get the expression for other layers as follow:

\[
\frac{\partial E}{\partial w_{l-1,t}} = \frac{\partial E}{\partial S_t} \cdot \frac{\partial S_t}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l-1,t}} \\
= \frac{\partial E}{\partial S_t} \cdot \frac{\partial S_t}{\partial Z_{l,t}} \cdot \frac{\partial Z_{l,t}}{\partial V_{l,t}} \cdot \frac{\partial V_{l,t}}{\partial W_{l-1,t}} \quad \text{let } Z_{l,t} = V_{l,t} \odot y_{l,t} \\
= (W_{l,t}^T \delta_{l,t} \odot h'(V_{l,t} - V_{th})) x_{l-1,t}^T \\
= \delta_{l-1,t} x_{l-1,t}^T \quad \text{let } \delta_{l,t} = ((W_{l,t}^T \delta_{l,t} \odot h'(V_{l,t} - V_{th}))
\]

Therefore, the final weight update matrix expression is as below:
\[
\Delta W_k = -\eta \delta_{k,t} x_{k,t}^T
\]
\[
\delta_{k,t} = \begin{cases} 
(S_t - \hat{y}_t) \odot (y_t + V_t \odot h'(V_{k,t} - V_{th})) & \text{if } k = K \\
(W_{k+1,t}^T \delta_{k+1,t}) \odot h'(V_{k,t} - V_{th}) & \text{otherwise}
\end{cases}
\]
3 PSEUDO CODE FOR PULSE PARAMETER SELECTION MODULE

```plaintext
procedure PULSE PARAMETERS SELECTION ACCORDING TO ΔW
    memristor = ParametericDevice(*args)
    res = []
    for pulse in pulseList do
        memristor.initialise(R)
        for timestep in range(pulse[1] / dt) do
            step_dt[pulse[0], dt]
        end for
        res.append(memristor.Rmem)
    end for
    resDist = abs(res - R_expected)
    selectedPulseIndex = argmin(resDist)
    selectedPulse = res[selectedPulseIndex]
end procedure
```

- Create a ParametericDevice object
- Create an empty list to store resulting resistance
- Loop over all options of pulse parameters
- Set current resistance to R
- pulse[1] stores pulsewidth
- pulse[0] stores magnitude
- Append resulting resistance to the list
- Calculate distance between expected and calculated resistance
- Find the index of minimal distance
- Find parameters of the pulse option