BiFSMNv2: Pushing Binary Neural Networks for Keyword Spotting to Real-Network Performance

Haotong Qin, Xudong Ma, Yifu Ding, Xiaoyang Li, Yang Zhang, Zejun Ma, Jiakai Wang, Jie Luo, and Xianglong Liu, Member, IEEE

Abstract—Deep neural networks, such as the deep-FSMN, have been widely studied for keyword spotting (KWS) applications while suffering expensive computation and storage. Therefore, network compression techniques such as binarization are studied to deploy KWS models on edge. In this article, we present a strong yet efficient binary neural network for KWS, namely, BiFSMNv2, pushing it to the real-network accuracy performance. First, we present a dual-scale thinnable 1-bit-architecture (DTA) to recover the representation capability of the binarized computation units by dual-scale activation binarization and liberate the speedup potential from an overall architecture perspective. Second, we also construct a frequency-independent distillation (FID) scheme for KWS binarization-aware training, which distills the high- and low-frequency components independently to mitigate the information mismatch between full-precision and binarized representations. Moreover, we propose the learning propagation binarizer (LPB), a general and efficient binarizer that enables the forward and backward propagation of binary KWS networks to be continuously improved through learning. We implement and deploy BiFSMNv2 on ARMv8 real-world hardware with a novel fast bitwise computation kernel (FBCK), which is proposed to fully use registers and increase instruction throughput. Comprehensive experiments show our BiFSMNv2 outperforms the existing binary networks for KWS by convincing margins across different datasets and achieves comparable accuracy with the full-precision networks (only a tiny 1.51% drop on Speech Commands V1–V12). We highlight that benefiting from the compact architecture and optimized hardware kernel, BiFSMNv2 can achieve an impressive 25.1× speedup and 20.2× storage-saving on edge hardware.

Index Terms—Deep learning, keyword spotting (KWS), model compression, network binarization, speech.

I. INTRODUCTION

RECENTLY, deep learning techniques using neural networks have achieved significant progress and have shown great potential in various fields, including but not limited to computer vision, natural language processing, speech recognition, etc. [10], [11], [12], [13], [23], [24], [25], [26], [27], [43], [46], [47], [48], [52], [53], [58], [66], [69], [71], [72], [73], [74], [75], [76]. The deep speech processing models also emerge and become popular [38], [59], [60], [61], [63], such as the feedforward sequential memory networks (FSMN) [68], compact FSMNs (cFSMN) [6], and deep FSMNs (deep-FSMN) [67]. Among these, deep neural networks for keyword spotting (KWS) are increasingly being studied for real-world applications [2], [5], [17], [37], [62], [68]. They allow users to activate devices by speaking keywords or specific phrases while keeping the device in a dormant state when inactive. However, these deep KWS networks are often computationally and storage expensive and are deployed on edge devices with limited resources that must constantly be on standby for possible speech input. Thus, the deployment of the advanced KWS models faces the significant challenge of resource constraint in practice. To address the challenge, various novel algorithms, such as cFSMN [6], dc-CNN [70], and BC-ResNet [16], have been designed for lightweight deep learning for KWS. Though the existing KWS methods have achieved remarkable storage compression and computation saving, they still suffer massive floating-point parameters and computation. Thus, room for compression still exists from a bit-width perspective.

Network binarization, as demonstrated in recent studies such as [35], [42], [49], [50], [57], [64], [77], is a highly efficient form of network quantization that uses 1-bit binarized parameters to compress networks for extreme computational and storage efficiency. The resulting binarized models take advantage of compact weights and activations, which use efficient bitwise XNOR and pop-count instructions with minimal memory to save computation resources and time far more than floating-point ones. For example, Rastegari et al. [36] shows that the compression and speedup ratios of binarized convolution units can theoretically reach up to 32.00× and 62.27×, respectively. However, despite the progress made in network binarization, applying the existing methods to quantize neural networks for KWS still results in a significant drop in accuracy. It is because both the weights and activations are binarized, which constrains the representation capability of the 1-bit models to the limited value space of the parameters. In addition, binarization makes it challenging to optimize the models, as it introduces high discretization into deep models. In comparison to other compression methods such as pruning and architecture design, network binarization possesses powerful

2162-237X © 2023 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to the terms of the applicable license agreement with IEEE. Restrictions apply.
topological characteristics as it only affects parameters [10], [34], [40]. And it is widely researched in academic studies as a standalone compression technique rather than simply a 1-bit specialization of quantization [4], [79]. Furthermore, the existing architectures for KWS have fixed model scales and topologies, which cannot adaptively balance resource budgets at runtime. Moreover, the existing deployment frameworks are still far from reaching the theoretical upper limit of acceleration for binarized networks when implemented on real-world hardware.

This article presents a lightweight and strong binary neural network for the KWS task dubbed as BiFSMNv2, with lightweight computation yet high accuracy (see the overview in Fig. 1). BiFSMNv2 is constructed based on the binarization of deep-FSMN with a pure feedforward structure: 1) we present a dual-scale thinnable 1-bit architecture (DTA), which recovers the representation capability of the binarized computing units by dual-scale activation binarization and liberates the speedup potential from an overall architecture perspective; 2) we also construct a frequency-independent distillation (FID) scheme for training binarized KWS models, which distills the high- and low-frequency components independently to match the corresponding information between the full-precision and binarized representations; 3) we design the learning propagation binarizer (LPB), a general and efficient binarizer that enables the forward and backward propagation of binary KWS networks to be continuously improved through learning; and 4) BiFSMNv2 is implemented and deployed on real-world ARMv8 devices with an efficient fast bitwise computation kernel (FBCK), which enjoys impressively faster inference than that using the existing binarization frameworks.

This work extends our prior conference publication [33], which presented the first binary network specifically for the KWS tasks. Despite efforts made in the field, the existing binary networks still have a significant accuracy gap compared with their full-precision counterparts due to high discretization. To address this, we further improve the optimization, representation, and architecture of binarization in this work and compare the proposed method with the state-of-the-art (SOTA) binarization algorithms. Compared with the conference version, the detailed improvements of this work are presented as follows.

1) We improve the architecture for the binarized KWS network, which increases the performance of binarized computing units while maintaining computational flexibility during inference. Based on the adaptively thinnable architecture, we further recover the binarized representation through dual-scale feature construction and liberate the speedup potential through an adaptively thinnable architecture from an overall perspective.

2) We present a stronger distillation scheme for binarized KWS networks that independently distills the high- and low-frequency components from the full-precision network, enabling binarization-aware distillation to mitigate the mismatch of information capacity from high and low frequencies and fully use the knowledge from full-precision representations.

3) We propose a generic yet efficient binarizer that enables the forward and backward propagation of binary KWS networks to be continuously improved through learning. It introduces a learnable threshold to mean-shift the representation in forward and a ratio parameter to achieve gradient error reduction in backward.

4) We compare our BiFSMNv2 with more SOTA binarization algorithms on KWS, including XNOR++ [3], ReActNet [21], ReCU [55], and FDA [54]. Moreover, we compare it with more binarized architectures (including a compact BiFSMNv2 version) in Table IV. The results show that BiFSMNv2 performs well among various binarization algorithms and architectures on different KWS datasets.

5) Benefiting from the latest implementation, we greatly reduce the number of parameters and inference calculations while improving the accuracy and achieving 20.2× compression and 25.1× acceleration in the deployment of ARMv8 hardware.

Our BiFSMNv2 first pushes binary neural networks for KWS to real-network accuracy. Comprehensive experiments on the Google Speech Commands V1 and V2 datasets [51] show that BiFSMNv2 completely outperforms the SOTA binarization methods and is even almost lossless compared with full-precision counterparts among 12, 20, and 35 keyword classification tasks, e.g., BiFSMNv2 enjoys 96.34% accuracy on Speech Commands V1–12 with a tiny 1.51% drop. Besides, we highlight that the efficient implementation makes our BiFSMNv2 easy to deploy and fast to inference in real-world devices on edge ARM devices. BiFSMNv2 can achieve up to 20.2× storage-saving and 25.1× speedup compared with the full-precision deep-FSMN. The code is released at https://github.com/htqin/BiFSMNv2.

II. RELATED WORK

A. Neural Network Binarization

With various advanced binarization methods emerging, the neural networks can be compressed and accelerated by binarization despite the different neural architectures or downstream learning tasks [15], [18], [35]. There are several ways to generically improve the binarized networks. The typical practices are 1) quantization error minimization: reducing the information loss during sign function transformation from 32-bit value to 1-bit value [36]; 2) loss function improvement: optimizing the binarized networks to close the accuracy gap from their full-precision counterparts [9], or distilling the knowledge from representations of full-precision networks to binarized networks [28]; and 3) gradient approximation: designing the approximation of binarization function for the backward propagation to match the gradient [9]. Moreover, a practice to boost the performance for different architectures is to design the specific binarization algorithm or binarized structure for each network and task, such as CNNs [21], [22], transformer-based [1], [31], and MLP-based networks [30] for computer vision, natural language processing, etc. But as for the KWS tasks, the general binarization algorithms are not satisfying due to the high-accuracy demands, and even the
specific binary neural network suffers a significant accuracy gap. Binary neural networks nowadays heavily depend on the support of hardware libraries when deployed. The binarization operations are constructed by XNOR and pop-count instructions on target hardware platforms (e.g., CPUs, GPUs, and FPGAs). Though some binarization frameworks, including daBNN [65] and Bort [14], can deploy some representative networks and tasks, such as ResNets for image classification, the support is still not ready for KWS networks.

B. Deep Neural Networks for KWS

Deep neural networks are widespread in many applications, including KWS tasks, due to their overwhelming superiority in performance. The recurrent neural network (RNN) [44] is originally designed to capture the context in a sequence, combining the advantages of the convolutional and recurrent layers to use both the local structure and long-range context. However, RNNs are usually computationally and energy expensive with poor parallelism on hardware. To reduce the consumption, the CNN-based (BC-ResNet [16]) models for KWS are also proposed with better performance and less energy cost, which applies most residual functions as 1-D temporal convolution while still allowing 2-D convolution together to expand the temporal output to the frequency–temporal dimension. Besides, RNNs also suffer from the vanishing of gradient, which is solved by FSMNs [68] afterward. FSMN has many variants, such as compact cFSMN [6], deep-FSMN [67], and pyramidal FSMNs (pFSMN) [56]. They are efficient in computation and also fast in convergence. However, FSMNs still conduct floating-point operations (FLOPs), which have redundancy in parameters and leave room for model quantization and binarization to further compress and accelerate inference on resource-constraint devices.

III. BiFSMNv2

We first introduce a basic binarization framework on deep-FSMN for KWS application and then present BiFSMN equipped with FID and DTA techniques and efficient FBCK for deployment on ARMv8 devices.

A. Basic Binarization Framework

First, we build a basic binarization framework on the deep-FSMN [67] architecture for the KWS task. Deep-FSMN is one of the variants of FSMN, which is particularly deep with shortcuts to capture inherent features in the input speech audios. It is binarization-friendly since: 1) deep-FSMN is a pure feedforward structure stacked by memory blocks to capture and store the information of sequential input and 2) the skip connections in adjacent layers are proved important for the accuracy performance of binarized networks [22] to allow the information to flow directly to the next block.

In the typical binarization network, we replace the floating-point parameters (weights and activations) with 1-bit by inserting sign function in the forward propagation

$$b_x = \text{sign}(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ -1, & \text{otherwise} \end{cases}$$

As for the backward propagation, the straight-through-estimator (STE) [7] is a simple but widespread solution for the problem of zero-gradient

$$g_x = \begin{cases} g_{\text{sign}(x)}, & \text{if } |x| \leq 1 \\ 0, & \text{otherwise} \end{cases}$$

where $g_x$ and $g_{\text{sign}(x)}$ denote the gradients of $x$ and sign($x$), respectively. $x$ denotes the element in floating-point weights or activations. The scaling factor $\alpha$ is only for weights to keep the magnitude of the real values

$$\alpha_w = \text{mean}(|w|)$$

where mean($\cdot$) denotes taking the mean value. We make $w \approx \alpha_w b_w$ to reduce the quantization error, where $b_w$ is the 1-bit weight binarized by sign function. Therefore, the whole computation process of the convolutional layer is denoted as follows:

$$o = \alpha_w (b_w \otimes b_a)$$

where $b_w$, $b_a$, and $o$ denote the binarized weights, binarized activations, and outputs, respectively, and $\otimes$ denotes the inner product with bitwise operation constructed by XNOR and pop-count instructions.

Applying the binarization operation on both the floating-point weights and activations for linear and convolutional layers, where the Matmul operation costs the majority of the computational resources and time,
we build the basic binarized deep-FSMN. We denote the input \( \ell \)-th hidden states as \( R^\ell_t = \{ R^\ell_{1,t}, \ldots, R^\ell_{T,t} \} \), and for each \( R^\ell_t, t \in [1, T] \), which is the fixed-size representation of the long context surrounding at time instance \( t \). The \( \ell \)-th binarized memory block in the network can be written as

\[
\hat{p}^\ell_t = \sum_{i=0}^{N^\ell_i} a^\ell_{ai} (b^\ell_{ai} \otimes b^\ell_{p_{t,i-1}}) \\
+ \sum_{j=1}^{N^\ell_j} a^\ell_{cj} (b^\ell_{cj} \otimes b^\ell_{p_{t,j+2}}) \\
+ \mathcal{H}(\hat{p}^{\ell-1}_t) + p^\ell_t
\]

(5)

where \( \mathcal{H}(\cdot) \) means the skip connection (identity mapping) within the block. The output of the binarized linear projection layer is denoted as

\[
p^\ell_t = \alpha v (b^\ell v^\ell \otimes b^\ell_{h^\ell}) + b^\ell
\]

(6)

while \( \hat{p}^\ell_t \) denotes the output of the full-precision memory block. \( N^\ell_i \) and \( N^\ell_j \) are the look-back and lookahead orders and \( s_1 \) and \( s_2 \) are the strides for the look-back and lookahead filters, respectively. The next hidden layer consists of \( T \) time instances as \( R^{\ell+1} = \{ R^{\ell+1}_1, \ldots, R^{\ell+1}_T \} \), and each of the time instance \( t \) can be expressed as

\[
\hat{R}^{\ell+1}_t = f'(U^\ell \otimes \hat{b}^\ell_u + b^{\ell+1}_t)
\]

(7)

where \( f'(\cdot) = BN \cdot \text{Nonlinear}(\cdot) \) denotes the composition of batch normalization and nonlinear functions (PReLU in the binarized network [28]).

B. DTA: Adapting Runtime Resources for Accuracy–Efficiency Tradeoff

As discussed earlier, binarization is an efficient compression approach with extremely lightweight 1-bit parameters, enabling fast bitwise operations, enabling fast inferences on resource-limited devices. However, there are still two challenges in the practical use of binary neural networks: 1) feature binarizing causes severe degeneration of representation capability in the prediction and 2) the energy budget varies between devices and is even different in wake-up and powering modes. Therefore, an adaptive yet powerful binarized architecture is required to permit instant accuracy–efficiency tradeoffs for KWS applications in runtime.

In the existing KWS networks that have been proposed, including full-precision and binary neural networks [6], [33], [67], [68], we can disassemble their design motivations of the network architectures into two steps: first, defining individual layers and/or blocks, such as using residuals connections and 1-bit computationally intensive layers; then, define the combination layers and/or blocks, including thinnable architectures and block-stacking structures. One of the well-recognized challenges for binary neural networks is that the representation capability of a single binarization layer is severely limited due to its restricted weights and activations. Therefore, it is promising to improve the tradeoff in the architecture design specifying for the binary KWS network, sacrificing the computational savings of a single 1-bit layer/block to allow stronger representation capabilities and cooperate with a lighter overall topology.

Along with this motivation, we present a DTA for KWS. In the proposed architecture, the representation capability of binarized computing units is significantly strengthened while the overall topology is simplified to be lighter; thus, it enjoys a balance between accuracy and efficiency and enables switching to thinner versions at runtime for online resource constraints. First, we build the strengthened binarized computing units to recover their representation capability, including 1-dim convolutional, 2-dim convolutional, and linear units. As (4) presents, the activation is directly binarized by sign function, which makes representations highly discrete and loses information. We introduce a dual-scale binarization to quantizing computing units, where the first and second scales of features are

\[
\begin{align*}
\text{1st scale: } & b^{1\text{st}}_u = \text{sign}(a) \\
\text{2nd scale: } & b^{2\text{nd}}_u = \text{sign}(a - b^{1\text{st}}_u)
\end{align*}
\]

(8)
where $\alpha^2 \equiv$ mean($a - b^1$) is the scaling factor of the second-scale residual feature and should be calculated in real-time during inference. Since the more fine-grained feature is introduced, the single binarized unit can represent more detailed information. Taking the convolutional unit as an example, the process can be formulated as

$$o_{\text{dual}} = \alpha_w (b_w \otimes b^1) + \alpha_w \alpha_a (b_w \otimes b^2)$$

and the binarized linear unit has the similar form. The illustration and example of DTA are presented in Fig. 2.

Our dual-scale binarization strengthens binarized representations, focusing on recovering the fine-grained binarized activations. In previous literature, a few works also recognized this positive effect on the accuracy of binarized and applied multiple or fine-grained weights/activations to boost representation [19], [20], [36]. Different from these studies, we solve representation degeneration of binarization directly with minimal cost. First, we find that the capability of the binarized model is mainly limited by binarized activations, which reflects that the information degradation of the data flow is more severe than the weights with scaling factors. Thus, we do not introduce additional weights and maintain the storage consumption of binarized computing units the same as before. Moreover, since scaling factors for activations would be calculated in real-time during inference, we only use scaling factors on the second-scale binarized features instead of rescaling for two activations. It adds little computational overheads while greatly recovers the information loss of the purely binarized one (only first-scale). However, although our dual-scale binarization can significantly enhance representation capabilities with limited storage and computation costs, applying it directly to the original overall topology still brings additional computational burden (compared with the vanilla binarization methods). For example, for an eight-layer deep-FSMN architecture, the inference FLOPs of directly using binarization methods are about 1.6. Thus, we do not introduce additional weights and maintain the storage consumption of binarized computing units the same as before. Moreover, since scaling factors for activations would be calculated in real-time during inference, we only use scaling factors on the second-scale binarized features instead of rescaling for two activations. It adds little computational overheads while greatly recovers the information loss of the purely binarized one (only first-scale). However, although our dual-scale binarization can significantly enhance representation capabilities with limited storage and computation costs, applying it directly to the original overall topology still brings additional computational burden (compared with the vanilla binarization methods). For example, for an eight-layer deep-FSMN architecture, the inference FLOPs of directly using dual-scale quantization are about 1.5x that of applying the DoReFa-Net binarization method [78]. The strengthened binarized units request us to design a lighter overall architecture. Therefore, since the strengthened binarized computing units with dual-scale binarization bring additional computation overhead, we should also design a flexible and compact architecture for an accuracy–efficiency tradeoff. When we focus on the full-precision backbone in FSMN, which is computationally expensive, the basic binarization architecture $M$ containing $2N$ blocks ($2N$ defaults to 8) is expressed as

$$M(x) = \psi^{2N} \cdot \psi^{2N-1} \cdots \psi^1(x)$$

where $M$ and $\psi^\ell$ are the binary neural network and $\ell$th binarized deep-FSMN block, respectively, and $x$ is the input of the network. A compact thinnable binarization architecture $M_{\text{DTA}}$ using dual-scale binarized computing units can be derived from $M$ for adaptive switching on deployment

$$M_{\text{DTA}}(x; \delta) = \Phi^N_{\text{dual}} \cdot \Phi^{N-1}_{\text{dual}} \cdots \Phi^1_{\text{dual}}(x)$$

where the block number $N$ is reduced to $N$ due to the strengthened single-unit representation capability, and $\delta$ is the interval of selected layers, which is confined to be divisible into $N$. Each thinnable block $\Phi^\ell_{\text{dual}}$ can be defined as

$$\Phi^\ell_{\text{dual}}(x) = \begin{cases} \psi^\ell_{\text{dual}}(x), & \ell \in [i \delta, i \in [1, N/\delta]) \\ x, & \text{otherwise.} \end{cases}$$

The batch normalization in the function $f(\cdot)$ for the $\ell$th dual-scale binarized block $\psi^\ell_{\text{dual}}$ is preassigned as (9) according to different variants in the thinnable network. The thinnable network architecture will skip the intermediate blocks in every $\delta$ layer by replacing them with identity functions.

Fig. 1 shows the formalization of our proposed DTA, and we also provide an instance for the $N = 4$, $\delta = 1, 2, 4$ setting in Fig. 3, which is also our default experiment setting. Under this setting, compared with the existing binary KWS network, our architecture has stronger representation capability and lower resource consumption.

C. FID: Matching Information in Binarization-Aware Training

Usually, the accuracy of binarized networks will drop severely compared with full-precision counterparts since the representation capability is extremely limited by compact parameters. We visualize the intermediate representation of both full-precision and binarized networks in Fig. 4. It is a natural result that the information is richer in full precision but monotonous in the binarized ones since it restricts the values to binary. Therefore, some binarization methods are devoted to globally retaining the information using the binarized representations during training. For example, Qin et al. [32] base on entropy maximization and Liu et al. [21] apply learnable mean-shift to both weights and activations. However, in binarized representations, the outlines of the object may convey more important information than plane blocks. The values on the edge always fall to 1 or −1, which displays the main feature of the input. While compared with the plane blocks, the edges are the locally gradient-maximized part of the feature map and are hard to be directly optimized globally.

Fortunately, we find that the information trends to gather in edges because the binarized features are better at capturing high-frequency components. First, we define the high- and low-frequency components of the intermediate representations and the related metrics. We use 2-D Haar wavelet transform (WT) [29] to isolate the horizontal and vertical edges as one of the most frequently used separable transforms. By this way, the intermediate representations are decomposed into low- and high-frequency components. We sum up the wavelet function family weighted, and the input representation $R$ of one specific layer can be written as

$$f_{\text{WT}}(R) = \sum_{j=-N}^{-1} \sum_{k} C_{j}(k) \phi_{j,k}$$

where $\phi$ is the mother wavelet function with a specific time parameter, $j = -1, \ldots, -N$ is the resolution level, and $k$ determines the translation of the waveform. The relative
wavelet energy is used as a metric to measure the information amount of the intermediate representation that has been decomposed

$$\mathcal{E}_j = \sum_k |C_j(k)|^2.$$  

Therefore, the relative wavelet energy of low- and high-frequency components ($C_j \in \{C_L, C_H\}, N = 2$) after one decomposition could be represented as

$$p_H = \frac{\mathcal{E}_H}{\mathcal{E}_{\text{total}}}, \quad p_L = \frac{\mathcal{E}_L}{\mathcal{E}_{\text{total}}}$$

where $\mathcal{E}_{\text{total}} = \mathcal{E}_H + \mathcal{E}_L$ denotes the total relative wavelet energy of representation. If the information is richer in some components, the corresponding energy is also larger.

Then we can obviously find the differences in frequency for the representations of full-precision and binarized networks. As Fig. 4 shows, compared with the representation in the full-precision network, the relative wavelet energy (values in the bottom-right) of the high-frequency components rapidly increases after being binarized but the low-frequencies decreases, which indicates that the binarized representation inclines higher frequency components. As mentioned in Section II-A, many current binarization-aware training methods focus on making binarized features close to full-precision ones, including numerical approximating and distillation-based approaches. Our findings suggest that directly learning from full-precision to binarized features will lead to a mismatch between their high- and low-frequency components. Specifically, comparing the full-precision to binarized representations directly is to consider not only the content of high and low frequencies but also the proportion of frequency information. Since the capability of capturing frequency is fundamentally different for the two representations, the mismatch caused by the proportion gap will usually exist and be hard to mitigate, which in turn significantly affects the training performance.

According to the discussion above, we design a distillation scheme that is tailored to binarization-aware training, named FID. As general distillation schemes, a well-trained full-precision deep-FSMN model is required as the teacher model, and the FID scheme is applied to transform knowledge from a full-precision model to a binarized one. Specifically, we decompose the original representations by Haar WT for full-precision teacher and binarized student models to make the frequency components of their representations independent and then obtain the representations of the corresponding components by applying inverse WT (IWT). For the teacher model, the process can be formulated as follows:

$$\hat{R}_H = f_{\text{IWT}} \left( \sum_k \hat{C}_H(k) \phi_{TH,k} \right)$$

$$\hat{R}_L = f_{\text{IWT}} \left( \sum_k \hat{C}_L(k) \phi_{TL,k} \right)$$

where $\hat{C}_H(k)$ and $\hat{C}_L(k)$ denote the high- and low-frequency components, respectively, and $\hat{R}_H$ and $\hat{R}_L$ denote the corresponding transformed representations. For the student model, we can also obtain $R_H$ and $R_L$ following the same steps. Then, inspired by Martinez et al. [28], we minimize the distillation loss with attention form between separated representations from the teacher and student models, which is expressed as

$$\mathcal{L}_{\text{FID}} = \sum_{\ell=1}^N \left( \frac{\|R_H^{\ell 2}\|}{\|R_H^{\ell 2}\|} - \frac{\|\hat{R}_H^{\ell 2}\|}{\|\hat{R}_H^{\ell 2}\|} \right) + \frac{\|R_L^{\ell 2}\|}{\|R_L^{\ell 2}\|} - \frac{\|\hat{R}_L^{\ell 2}\|}{\|\hat{R}_L^{\ell 2}\|}$$

(17)

where $\ell$ denotes the $\ell$th block and $\|\cdot\|$ is the L2-norm. Since the frequency mismatch between binarized and full-precision representations is mitigated, the proposed FID scheme makes the optimization of the binarized student network accurate using the knowledge from the full-precision model.

Furthermore, to optimize the proposed TDA, we adopt a uniform layer mapping strategy in FID to align and learn representation

$$\mathcal{L}^g_{\text{FID}} = \sum_{\ell=1}^{N/\delta} \left( \frac{\|R_H^{\ell \delta 2}\|}{\|R_H^{\ell \delta 2}\|} - \frac{\|\hat{R}_H^{\ell \delta 2}\|}{\|\hat{R}_H^{\ell \delta 2}\|} \right) + \frac{\|R_L^{\ell \delta 2}\|}{\|R_L^{\ell \delta 2}\|} - \frac{\|\hat{R}_L^{\ell \delta 2}\|}{\|\hat{R}_L^{\ell \delta 2}\|}.$$  

(18)

The gradients from different switches are accumulated during backward propagation to update the weight jointly. According to the compression ratio in the thinnable architecture, the weighted loss can be calculated as

$$\mathcal{L}_{\text{tot}} = \sum_{\delta} \frac{1}{N-1} \left( \mathcal{L}^g_{CE} + \gamma \mathcal{L}^g_{\text{FID}} \right)$$

(19)

Authorized licensed use limited to the terms of the applicable license agreement with IEEE. Restrictions apply.
expression capability of the binarized parameters significantly. We find that the existing binarizers have limitations in both forward and backward, impacting the update the parameters \((2)\). We find that the existing binarizers, which could lead to suboptimal models and negatively impact the overall performance.

D. Propagating Learnable Binarizer: Learning Forward and Backward Propagation for Binarization

Through our DTA architecture and FID optimization design, we have developed a powerful and lightweight binary neural network that can perform accurate and flexible reasoning on edge devices. However, our research has shown that this is still not the limit of what binary neural networks can achieve on the KSW tasks. There is still room for improvement in existing parameter binarizers, which could lead to even more efficient and effective binary neural networks for KWS.

As mentioned in Section III-A, in binary neural networks, binarizers are used to quantize the weights and activations of the computation-intensive units in the neural network. Specifically, during forward propagation, the parameters are quantized to 1 and \(-1\) using the discrete sign function [as shown in (1)]; during backward propagation, the clip function is applied to approximate the derivative of the sign function to update the parameters [(2)]. We find that the existing binarizers have limitations in both forward and backward, impacting the expression capability of the binarized parameters significantly.

1) Rigid forward parameterization. Using the sign function in the training process results in full-precision parameters being directly quantized to \(-1\) or 1 with a threshold of 0. This makes it difficult for the quantizer to adjust to the overall distribution, as direct adjustments at the global level are challenging to achieve. The adjustment of the quantizer to the overall distribution must rely on indirect pixel-level parameter updates, which greatly restricts the representation capability of the binarized parameters.

2) Backward error accumulation. The use of the clip function leads to the gradient in the region \(x \in [-1, 1]\) being passed directly with a ratio of 1. However, the derivative of the sign function in this area is just 0, resulting in a ratio close to infinity, indicating a significant error that cannot be adjusted during the training process. This error can lead to suboptimal models and negatively impact the overall performance.

These observations suggest that the currently applied binarizers have limitations in both the forward and backward propagation, which can significantly affect the expression capability of the quantized parameters. Further research is needed to develop new binarizers that address these limitations, to improve the performance of binarized neural networks.

Refer to Fig. 5 as an illustration. We propose the LPB, a generic yet efficient binarizer that enables the forward and backward propagation of binary KWS networks to be continuously improved through learning. In the forward propagation, we introduce a learnable threshold \(\theta\) based on the sign function to mean-shift the representation. Through this operation, the features of the forward propagation can be conveniently shifted from the global level, and the diversity is greatly enriched, thereby improving the representation ability of the binary quantization model. In the backward propagation, we also introduce a ratio parameter \(r\) for gradient approximation and adjust the ratio of the approximate function in the backward propagation to reduce the gradient error. The forward and backward propagation of LPB can be expressed as follows:

Forward: \(\text{LPB}(x) = \text{sign}(x - \theta) = \begin{cases} 1, & \text{if } x \geq \theta \\ -1, & \text{otherwise} \end{cases} \)

(20)

Backward: \(\frac{\partial \text{LPB}(x)}{\partial x} \approx \begin{cases} rg_x, & \text{if } |x - \theta| \leq r \\ 0, & \text{otherwise} \end{cases} \)

(21)

where \(\text{LPB}(\cdot)\) denotes the LBP function. Since the improvements are limited to the binarizer, it can be used universally in all the binarized computing units, including convolutional and linear layers.

The detailed training procedures for BiFSMNv2 are listed in Algorithm 1.

E. FBCK for Efficient Hardware Deployment

The FLOPs [22] of a single binarization layer are theoretically reduced by an extremely high level of 64×, benefiting...
from the binarization weights and compression to the original bit width 1/32. However, when we implement and deploy the entire binary neural network on real-world hardware using the existing binarization deployment frameworks, its overall inference efficiency is often significantly lower than the theoretical upper limit, such as daBNN [65] and Bolt [14]. One of the key bottlenecks in speedup is the use of binarized general matrix multiplication (BGEMM), which is performed by bitwise XNOR and Bitcount. In the existing deployment frameworks such as daBNN, the corresponding instructions on ARMv8 are EOR, CNT, etc. However, owing to the limit of register and instruction throughput, the efficiency of BGEMM hardware implementation is far less than that of its theoretical design. Therefore, for efficient deployment on edge devices with limited computational resources, we further optimize the 1-bit computation with new instruction and register allocation strategy to accelerate the inference on ARMv8-A architecture which are widely used on edge devices. We dub it FBCK.

According to the number of registers on the ARMv8 architecture, we first reallocate the registers in the kernel as five partitions to improve the register utilization and reduce the memory footprint: partition A has four registers (except register v0) for one input (weight/activation), B has two for the other input, C has eight for intermediate results of EOR and CNT, D has eight for the output in one loop, and E has eight for the final results. Each input is packed as INT16. Each register in A stores an input that is repeated eight times, while each register in B stores eight different inputs. We first apply EOR and CNT for A with one register of B to get 32 INT8 results in intermediate partition C, and then perform ADD to accumulate the INT8 to D, and do the same for the other register of B. After 16 times loop, we finally accumulate the INT8 data stored in D to an INT16 register (in E) using long instruction ADALP, which extends INT8 data to double width. FBCK makes full use of registers almost without idle bits during the computation. Refer to Fig. 6 as an illustration.

IV. EXPERIMENTS

In this section, to verify the effectiveness of our BiFSMNv2, we conduct comprehensive experiments on the Google Speech Commands V1 and V2 datasets [51] and compare it with the SOTA binarization methods on various KWS deep network architectures.

BiFSMNv2: Our BiFSMNv2 is implemented and trained by PyTorch since it enjoys a strong automatic differentiation function and high flexibility. To build a binarized KWS model, we use binarization methods to quantize convolutional and linear units on specified neural architectures.

Neural Architecture: We test the performance of the proposed BiFSMNv2 on both normal and compact architecture versions, dubbed as BiFSMNv2 and BiFSMNv2s, respectively, on the Google Speech Commands datasets in our experiments. BiFSMNv2 for experiments has four memory blocks with 128 backbone memory size and 224 hidden size.

To verify the accuracy and efficiency advantages of our method, we also compare BiFSMNv2 with the binarized networks with different neural architectures [16], [33], [43], [67], [68]. We binarize the convolutional and linear units in KWS networks except for the first and last layers.

Hyperparameters and Training Setups: To evaluate our BiFSMNv2 fairly, we mostly apply the original hyperparameter settings and training steps or follow exactly the presented results in their articles [3], [21], [22], [32], [33], [36], [54], [55]. Specifically, among the experiments of BiFSMNv2, we apply the SGD optimizer and use a cosine annealing scheduler decaying learning rate to 0. For other networks and binarization methods, we mostly follow the hyperparameter settings of their original articles. We train all the binarized models 300 epochs, the same as their full-precision counterparts.

Evaluation Metric Definition: Following the existing works for KWS [16], [33], we use accuracy as the metric to evaluate the classification tasks on the Speech Commands V1 and V2 datasets. The accuracy is the fraction of predictions the model got right and has the following definition:

\[
\text{Accuracy} = \frac{\text{Number of correct predictions}}{\text{Total number of predictions}}.
\]

The metric definition is generic for 12, 20, and 35 classification tasks (CLS 12, CLS 20, and CLS 35) on the Speech Commands V1 and V2 datasets.

Computational FLOPs: For 1-bit weights and activations, the multiplication between \(m\)-bit and \(n\)-bit parameters approximately takes \(mn/64\) FLOPs for a CPU using 64-bit instructions [22], [78], so we calculate the FLOPs for a single binarized computing unit as 1/64 of its full-precision counterpart.

Deployment Hardware: To validate the practicability of BiFSMNv2, we test the actual speed of BiFSMNv2 on Raspberry Pi 3B+ with 1.2-GHz 64-bit ARMv8 CPU Cortex-A53.

A. Ablation Study

We conduct ablation experiments on the Google Speech Commands datasets (V1–12 tasks) to investigate the impact of the components of the proposed BiFSMNv2, including DTA and FID.

1) Effect of DTA: We first verify the effect of DTA. Compared with the traditional architecture, DTA significantly reduces the activation binarization error through two-scale binarization, so the information in the features can be recovered. In Fig. 7, we randomly sample the activations in

Authorized licensed use limited to the terms of the applicable license agreement with IEEE. Restrictions apply.
TABLE I
ABSTRACTION STUDY OF OUR BiFSMNv2 ON THE SPEECH COMMAND V1 (SC-V1) AND V2 (SC-V2) DATASETS WITH 12 CLASSIFICATIONS

| Arch.     | Quant       | #Bits (WA) | FLOPs (M) | SC-V1 (%) | SC-V2 (%) |
|-----------|-------------|------------|-----------|-----------|-----------|
| Deep-FSMN | Full Prec.  | 32         | 10.15     | 97.93     | 98.05     |
| Deep-FSMN | Vanilla     | 1/1        | 40.46     | 87.71     | 89.53     |
|           | Distill     | 1/1        | 40.46     | 90.02     | 90.95     |
|           | l2-norm     | 1/1        | 40.46     | 93.23     | 93.76     |
|           | FID         | 1/1        | 40.46     | 94.08     | 94.37     |
|           | FID + LPB   | 1/1        | 40.46     | 96.21     | 96.22     |
| BiFSMNv2  | Vanilla     | 1/1        | 35.01     | 95.09     | 95.30     |
|           | Distill     | 1/1        | 27.96     | 94.75     | 95.12     |
|           | l2-norm     | 1/1        | 27.96     | 94.93     | 95.55     |
|           | FID         | 1/1        | 27.96     | 96.08     | 94.08     |
|           | FID + LPB   | 1/1        | 27.96     | 96.23     | 94.45     |

Fig. 8. Training curves for deep-FSMN in FID, BiFSMNv2 in vanilla, and BiFSMNv2 in FID.

Fig. 9. Percentage of the relative wavelet entropy of low/high frequency in each layer of full-precision and binarized models.

Fig. 7. Comparison of activation quantization error measured by MSE between vanilla and DTA units on the eight-layer deep-FSMN architecture.

each layer in one forward and calculate the quantization error by comparing the binarized activation with the original floating-point ones measured by mean square error (MSE). It shows the error in the corresponding layer in deep-FSMN and DTA architectures, and we can see that DTA has significantly reduced quantization error. In addition, the training curves in

Authorized licensed use limited to the terms of the applicable license agreement with IEEE. Restrictions apply.
TABLE II

| Part         | 32-bit | 1-bit |
|--------------|--------|-------|
| Head         |        |       |
| Layer1.1     | 14.08  | 14.08 |
| Layer1.2     | 105.64 | 3.47  |
| Neck         |        |       |
| Block2.1     | 33.55  | 1.18  |
| Block3       | 69.34  | 3.82  |
| Block4       | 69.34  | 3.82  |
| Block5       | 69.34  | 3.82  |
| Block6       | 69.34  | 3.82  |
| Block7       | 69.34  | 3.82  |
| Block8       | 69.34  | 3.82  |
| Classifier   | 1.57   | 1.57  |

The application of the proposed LPB pushes BiFSMNv2 to a higher accuracy, and jointly using DTA, FID, and LBP further narrows the accuracy gap between the binarized model and the full-precision counterpart. The performance of 1-bit BiFSMNv2 on the Speech Commands V1–12 tasks achieves 96.42%, just 1.51% drop compared with the 32-bit counterpart.

5) Efficiency Ablation Results: We present the ablation results for the FLOPs of the full-precision and binarized architecture to measure the acceleration effect of our proposed binarization. The results in Table II show that our binarization algorithm achieves a super-high speedup of 18.1× for a single block in backbone, while the FLOPs produced by the unbinarized layers are only a relatively small fraction of the full-precision counterpart. This guarantees the ultrahigh speedup of our BiFSMNv2.

B. Comparative Experiments

First, we compare our BiFSMNv2 with the existing SOTA structure-independent binarization methods, including BNN [8], DoReFa [78], XNOR [36], Bi-Real [22], IR-Net [32], RAD [9], ReCU [55], ReActNet [21], XNOR++ [3], LCR [41], and FDA [54]. We evaluate these binarization methods on eight-block deep-FSMN and BiFSMN with a similar size as the largest variant of four-block BiFSMNv2.

The results in Table III show that our 1-bit BiFSMNv2 completely outperforms the existing SOTA binarization methods by a wide margin. On Speech Commands V1–12 tasks, BiFSMNv2 surpasses the classic XNOR and IR-Net 13.68% and 9.61%, respectively, and even outperforms the recent FDA and ReCU methods by 9.61% and 2.68%. The advantages of BiFSMNv2 are also presented on V1–20 and V1–35 tasks and bring 3.87% and 3.40% accuracy improvement compared with the SOTA binarization methods, respectively, though these tasks are considered to be more challenging. Compared with the first version of BiFSMN, BiFSMNv2 wins by a great margin, including in the comparison of the accuracy of all thinner variants. A similar phenomenon is on the Speech Commands V2 datasets. BiFSMNv2 surpasses the SOTA binarization methods and BiFSMN on V2–12, V2–20, and V2–35 tasks. It is noteworthy that BiFSMNv2 even enjoys competitive accuracy to full-precision counterparts within a 1.60% accuracy drop on both the datasets, e.g., it only drops 1.51% accuracy in the Speech Command V1–12 tasks. Furthermore, from the perspective of inference cost, the thinner version BiFSMNv2_{0.5x} with two blocks and BiFSMNv2_{0.25x} with one block achieves an amazing 25.40× and 29.07× FLOPs saving without sacrificing accuracy (only 0.19% and 1.77% drop) on Speech Commands V1–12 tasks.
To further validate the advantage of our BiFSMNv2 from the neural architecture perspective, we also compare it with various networks widely used in KWS, including FSMN [68], VGG19bn [43] (selected from the open-source project [45] for Speech Commands KWS tasks), BC-ResNet-4/BC-ResNet-8 [16], MHAtt-RNN [39], and BiFSMN (the conference version) [33]. We binarized these architectures with four representative binarization methods, XNOR, IR-Net, ReActNet, and ReCU. In Table IV, our FID can generally be applied in deep-FSMN-based architectures, including deep-FSMN, BiFSMN, and BiFSMNv2 and improves their performance. The results show that our BiFSMNv2 has a significant advantage compared with the existing binarized architectures. Except for deep-FSMN with a similar number of parameters, BiFSMNv2 also far surpasses the binarized VGG19bn by 30.32% on the V1–12 tasks, which has several thousand times of parameters. BiFSMNv2 has also achieved significant advantages compared with the binarized versions of the architectures specially designed for KWS. Specifically, compared with binarized BC-ResNet, BiFSMNv2 can achieve up to 40.32% advantage, and it can even exceed at least 29.91% compared with the binarized BC-ResNet-8 with more parameters and higher FLOPs. The binarization of MHAtt-RNN also causes a severe accuracy drop, which shows that it is difficult and risky to binarize the existing KWS architecture directly, and shows the significant advantages of our BiFSMNv2 compared with the existing architecture of binarization. We further slim the model width and provide an extremely tiny BiFSMNv2s (kernel size is 3 × 3, and the number of channels is 12 in the front-end, 32 backbone memory layers, and 56 in hidden layers, respectively) with only 0.03 M parameters and 8.06–10.18 M FLOPs. The results show that our BiFSMNv2s still surpasses BiFSMNs though the latter has heavier storage and computation, demonstrating that our techniques also work well on tiny binarized networks.

In addition, we compare the parameter amount and time delay of different binarization methods under the same deployment environment in Table III. We use daBNN [65], one of the most widely used binarization open-source deployment frameworks, to deploy different architectures on real edge hardware and evaluate the inference speed (“-” indicates the binarization method cannot be supported). The results show that our BiFSMNv2 outperforms other methods by a large margin both in parameter amount and in time delay. Because the structure can be thinned and has fewer FLOPs, BiFSMNv2 has the least delay, and its 0.25× variant can even have an inference delay of only 22.9 ms, which is 57.8 ms less than BNN, and less than the 0.25 variant structure of BiFSMN 5.9 ms. Due to fewer blocks, the parameter number of BiFSMNv2 is less to 0.32 M, only 1/2 of other methods.

### C. Deployment Efficiency

As mentioned, low memory footprint and fast real-time response are highly expected in KWS while running on real-world edge devices.

According to Fig. 10, due to the proposed optimized 1-bit FBCK, our BiFSMNv2 delivers 20.2× storage saving compared with the full-precision counterparts. Furthermore, benefiting from the thinnnable architecture, BiFSMN can adaptively balance accuracy and efficiency at runtime.
according to the resources on the device and switches to BiFSMNv2\textsubscript{0.5×} (2 blocks) or BiFSMNv2\textsubscript{0.25×} (1 blocks) for further 19.9× and 25.1× speedups, respectively. It is much faster than the existing open-source, high-performance binarization frameworks (daBNN and Bolt) and shows that our BiFSMNv2 can satisfy different resource constraints.

V. CONCLUSION

We propose BiFSMNv2, an accurate and highly efficient binary neural network for KWS. We first construct a DTA to recover the representation capability of the binarized computation units by dual-scale activation binarization and liberate the speedup potential from an overall architecture perspective. We also construct an FID scheme to distill the high- and low-frequency components independently to mitigate the information mismatch between full-precision and binarized representations. BiFSMNv2 outperforms the existing binarization methods by convincing margins and is comparable to its full-precision counterparts. Furthermore, our ARMv8 real-world device with BiFSMNv2 implementation achieves an impressive 25.1× speedup and 20.2× storage-saving with the help of the proposed FBCK. Our work demonstrates the great potential of binarization for KWS on resource-limited hardware and first pushes it to real-network performance. We hope our work will inspire future research on lightweight KWS.

REFERENCES

[1] H. Bai et al., “BinaryBERT: Pushing the limit of bert quantization,” 2020, arXiv:2012.15701.
[2] A. Berg, M. O’Connor, and M. Tairum Cruz, “Keyword transformer: A self-attention model for keyword spotting,” 2021, arXiv:2104.00769.
[3] A. Bulat and G. Tzimiropoulos, “XNOR-Net++: Improved binary neural networks,” in Proc. 30th Brit. Mach. Vis. Conf. (BMVC), Cardiff, U.K., Sep. 2019, p. 62.
[4] Z. Cai, X. He, J. Sun, and N. Vasconcelos, “Deep learning with low precision by half-wave Gaussian quantization,” in Proc. IEEE Conf. Comput. Vis. Pattern Recognit. (CVPR), Jul. 2017, pp. 5918–5926.
[5] G. Chen, C. Parada, and G. Heigold, “Small-footprint keyword spotting using deep neural networks,” in Proc. IEEE Int. Conf. Acoust., Speech Signal Process. (ICASSP), May 2014, pp. 4087–4091.
[6] M. Chen, S. Zhang, M. Lei, Y. Liu, H. Yao, and J. Gao, “Compact feedforward sequential memory networks for small-footprint keyword spotting,” in Proc. Interspeech, Sep. 2018, pp. 1–5.
[7] M. Courbariaux, Y. Bengio, and J.-P. David, “BinaryConnect: Training deep neural networks with binary weights during propagations,” in Proc. NeurIPS, 2015, pp. 1–9.
[8] M. Courbariaux, I. Hubara, S. Doudry, R. El-Yaniv, and Y. Bengio, “Binarized neural networks: Training deep neural networks with weights and activations constrained to +1 or −1,” 2016, arXiv:1602.02830.
[9] R. Ding, T.-W. Chin, Z. Liu, and D. Marculescu, “Regularizing activation distribution for training binarized deep networks,” in Proc. IEEE/CVF Comput. Vis. Pattern Recognit. (CVPR), Jun. 2019, pp. 11408–11417.
[10] J. Guo, J. Liu, and D. Xu, “JointPruning: Pruning networks along multiple dimensions for efficient point cloud processing,” IEEE Trans. Circuits Syst. Video Technol., vol. 32, no. 6, pp. 3659–3672, Jun. 2022.
[11] J. Guo, J. Liu, and D. Xu, “3D-pruning: A model compression framework for efficient 3D action recognition,” IEEE Trans. Circuits Syst. Video Technol., vol. 32, no. 12, pp. 8717–8729, Dec. 2022.
[12] J. Guo, W. Ouyang, and D. Xu, “Multi-dimensional pruning: A unified framework for model compression,” in Proc. IEEE/CVF Conf. Comput. Vis. Pattern Recognit. (CVPR), Jun. 2020, pp. 1508–1517.
[13] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proc. IEEE Conf. Comput. Vis. Pattern Recognit. (CVPR), Jun. 2016, pp. 770–778.
[14] Huawei Noah. (2021). Bolt. https://github.com/huawei-noah/bolt.
[15] X. Jiang et al., “Toward pixel-level precision for binary super-resolution with mixed binary representation,” IEEE Trans. Neural Netw. Learn. Syst., early access, Sep. 7, 2022, doi: 10.1109/TNNLS.2022.3201528.
[16] B. Kim, S. Chang, J. Lee, and D. Sung, “Broadcasted residual learning for efficient keyword spotting,” 2021, arXiv:2106.04140.
[17] D. Leroy, A. Coucke, T. Lavril, T. Gisselbrecht, and J. Dureau, “Federated learning for keyword spotting,” in Proc. IEEE Int. Conf. Acoust., Speech Signal Process. (ICASSP), May 2019, pp. 6341–6345.
[18] K. Li et al., “Local means binary networks for image super-resolution,” IEEE Trans. Neural Netw. Learn. Syst., early access, Oct. 21, 2022, doi: 10.1109/TNNLS.2022.3212827.
[19] Z. Li, B. Ni, W. Zhang, X. Yang, and W. Gao, “Performance guaranteed network acceleration via high-order residual quantization,” in Proc. IEEE Int. Conf. Comput. Vis. (ICCV), Oct. 2017, pp. 2584–2592.
[20] X. Lin, C. Zhao, and W. Pan, “Towards accurate binary convolutional neural network,” in Proc. NeurIPS, 2017, pp. 1–9.
[21] Z. Liu, Z. Shen, M. Savvides, and K.-T. Cheng, “ReActNet: Towards precise binary neural network with generalized activation functions,” in Proc. ECCV, 2020, pp. 143–159.
[22] Z. Liu, B. Wu, W. Luo, X. Yang, W. Liu, and K.-T. Cheng, “BiRealNet: Enhancing the performance of 1-bit CNNs with improved representational capability and advanced training algorithm,” in Proc. ECCV, 2018, pp. 722–737.
[23] Z. Ma et al., “Fine-grained vehicle classification with channel max pooling modified CNNs,” IEEE Trans. Veh. Technol., vol. 68, no. 4, pp. 3224–3233, Apr. 2019.
[24] Z. Ma, Y. Lai, W. B. Kleijn, Y.-Z. Song, L. Wang, and J. Guo, “Variational Bayesian learning for Dirichlet process mixture of inverted Dirichlet distributions in non-Gaussian image feature modeling,” IEEE Trans. Neural Netw. Learn. Syst., vol. 32, no. 6, pp. 3659–3672, Jun. 2022.
[25] Z. Ma et al., “Dirichlet process mixture of generalized inverted Dirichlet distributions for positive vector data with extended variational inference,” IEEE Trans. Neural Netw. Learn. Syst., vol. 33, no. 11, pp. 6089–6102, Nov. 2022.
[26] Z. Ma et al., “On the comparisons of decorrelation approaches for non-Gaussian neutral vector variables,” IEEE Trans. Neural Netw. Learn. Syst., early access, Mar. 31, 2020, doi: 10.1109/TNNLS.2020.2978858.
[27] Z. Ma, J. Xie, Y. Lai, J. Taghia, J.-H. Xue, and J. Guo, “Insights into multiplies/single lower bound approximation for extended variational inference in non-Gaussian structured data modeling,” IEEE Trans. Neural Netw. Learn. Syst., vol. 31, no. 7, pp. 2240–2254, Jul. 2020.
Y. Xu, K. Han, C. Xu, Y. Tang, C. Xu, and Y. Wang, “Learning frequency domain approximation for binary neural networks,” in Proc. Adv. Neural Inf. Process. Syst., vol. 34, 2021, pp. 25553–25565.

Z. Xu et al., “ReCU: Reviving the dead weights in binary neural networks,” in Proc. IEEE/ICVF Int. Conf. Comput. Vis., Oct. 2021, pp. 5198–5208.

X. Yang, J. Li, and X. Zhou, “A novel pyramidal-FSMN architecture with lattice-free MMI for speech recognition,” 2018, arXiv:1810.11352.

J. Ye, J. Wang, and S. Zhang, “Distillation-guided residual learning for binary convolutional neural networks,” IEEE Trans. Neural Netw. Learn. Syst., vol. 33, no. 12, pp. 7765–7777, Dec. 2022.

Z. Yin et al., “Improving generalization of deepfake detection with domain adaptive batch normalization,” in Proc. 1st Int. Workshop Adversarial Learn. Multimedia, 2021, pp. 21–27.

H. Yu, Z. Ma, M. Li, and J. Guo, “Histogram transform model using MFCC features for text-independent speaker identification,” in Proc. 48th Asilomar Conf. Signals, Syst. Comput., Nov. 2014, pp. 500–504.

H. Yu, A. Sarkar, D. A. L. Thomsen, Z.-H. Tan, Z. Ma, and J. Guo, “Effect of multi-condition training and speech enhancement methods on spoofing detection,” in Proc. 1st Int. Workshop Adversarial Learn. Multimedia, 2021, pp. 1–5.

H. Yu, Z.-H. Tan, Z. Ma, and J. Guo, “Adversarial network bottleneck features for noise robust speaker verification,” in Proc. Interspeech, 2017, pp. 1492–1496.

H. Yu, Z.-H. Tan, Z. Ma, R. Martin, and J. Guo, “Spoofing detection in automatic speaker verification systems using DNN classifiers and dynamic acoustic features,” IEEE Trans. Neural Netw. Learn. Syst., vol. 29, no. 10, pp. 4633–4644, Oct. 2018.

H. Yu, Z. H. Tan, Y. Zhang, Z. Ma, and J. Guo, “DNN filter bank cepstral coefficients for spoofing detection,” IEEE Access, vol. 5, pp. 4779–4787, 2017.

B. Zhang, R. Wang, X. Wang, J. Han, and R. Ji, “Modulated convolutional networks,” IEEE Trans. Neural Netw. Learn. Syst., early access, Mar. 9, 2021, doi: 10.1109/TNNSL.2021.3060830.

J. Zhang, Y. Pan, T. Yao, H. Zhao, and T. Mei, “daBNN: A super fast inference framework for binary neural networks on arm devices,” in Proc. ACM MM, 2019, pp. 840–848.

M. Zhang et al., “MotionDiffuse: Text-driven human motion generation for virtual characters,” in Proc. IEEE/CVF Conf. Comput. Vis. Pattern Recognit., 2022, arXiv:2208.15801.

S. Zhang, M. Lei, Z. Yan, and L. Dai, “Deep-FSMN for large vocabulary continuous speech recognition,” in Proc. IEEE Int. Conf. Acoust., Speech Signal Process. (ICASSP), Apr. 2018, pp. 5860–5873.

S. Zhang, C. Liu, H. Jiang, S. Wei, L. Dai, and Y. Hu, “Feedforward sequential memory networks: A new structure to learn long-term dependency,” 2015, arXiv:1512.08301.

X. Zhang et al., “Diversifying sample generation for accurate data-free quantization,” in Proc. CVPR, Jun. 2021, pp. 15658–15667.

Y. Zhang, N. Suda, L. Lai, and V. Chandra, “Hello edge: Keyword spotting on microcontrollers,” 2017, arXiv:1711.07128.

Z. Zhao et al., “CDDFuse: Correlation-driven dual-branch feature decomposition for multi-modality image fusion,” 2022, arXiv:2211.14461.

Z. Zhao, S. Xu, C. Zhang, J. Liu, and J. Zhang, “Bayesian fusion for infrared and visible images,” Signal Process., vol. 177, Dec. 2020, Art. no. 107734.

Z. Zhao, S. Xu, C. Zhang, J. Liu, and J. Zhang, “DIDFuse: Deep image decomposition for infrared and visible image fusion,” in Proc. IJCAI, 2020, pp. 970–976.

Z. Zhao, S. Xu, J. Zhang, C. Liang, C. Zhang, and J. Liu, “Efficient and model-based infrared and visible image fusion via algorithm unrolling,” IEEE Trans. Circuits Syst. Video Technol., vol. 32, no. 3, pp. 1186–1196, Mar. 2022.

Z. Zhao, J. Zhang, S. Xu, Z. Lin, and H. Pfister, “Discrete cosine transform network for guided depth map super-resolution,” in Proc. IEEE/ICVF Conf. Comput. Vis. Pattern Recognit. (CVPR), Jun. 2022, pp. 5687–5697.

Z. Zhao et al., “FGF-GAN: A lightweight generative adversarial network for pansharpening via fast guided filter,” in Proc. ICME, Jul. 2021, pp. 1–6.

S. Zhong, X. Zeng, S. Wu, and L. Han, “Sensitivity-based adaptive learning rules for binary feedforward neural networks,” IEEE Trans. Neural Netw. Learn. Syst., vol. 23, no. 3, pp. 480–491, Mar. 2012.

S. Zhou, Y. Wu, Z. Ni, X. Zhou, H. Wen, and Y. Zou, “DeReFa-Net: Training low bitwidth convolutional neural networks with low bitwidth gradients,” 2016, arXiv:1606.06160.

C. Zhu, S. Han, H. Mao, and J. William Dally, “Trained ternary quantization,” in Proc. ICLR, 2017, pp. 1–10.