Simulation-Assisted Design of a Power Stack for Improving Static Current Sharing Among Three IGBT Modules Connected in Parallel

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ABSTRACT In this study, Q3D and Simploer software were adopted to design a single-phase power stack with equal output current on three paralleled IGBT modules in high power application, therefore, the derating of total current will be reduced, which can improve the current utilization and power density of power stack. The performance of the designed stack was verified using a double-pulse test (DPT). The circuit used in the DPT regarded the power stack output current as static current, which is a critical index to evaluate current sharing. The static current sharing among the IGBT modules was mainly dependent on the stray inductance of the DC busbar, IGBT modules, and phase output bar (POB), which is used to connect the IGBT modules to load, in the power stack. Cosimulation was performed with Simploer and Q3D to determine the stray inductance of the IGBT modules, DC busbar and POB, and a constant-current-slope method was used to verify the inductance. Subsequently, design the shapes of the DC busbar and POB for attaining maximum ratio of imbalanced current (MRIC) of the three IGBT modules is within 3% under 200% (2400A) rated current. The cosimulation results indicated that the MRIC of the current paths in power stack were 0.8%. Finally, three IGBT modules and a gate driver were used to construct power stack with 1000V DC link. The experimental results obtained by DPT indicated that the MRIC was 0.9% under 200% rated current, demonstrating the effectiveness of the proposed stray inductance design method.

INDEX TERMS IGBT module, power stack, cosimulation, current sharing, paralleled operation

I. INTRODUCTION
Insulated-gate bipolar transistors (IGBTs) are widely used in medium-voltage, high-voltage, and high-power systems because of their high current rating, high withstand voltage, and low loss. A half-bridge module with two IGBTs connected in series is typically used as a basic unit in converter or motor drive applications for the convenience of these applications [1], [2]. Therefore, a converter or an inverter is composed of low- or medium-voltage IGBT modules connected in series [3], [4] or parallel to increase the output power [5], which reduces the cost of wind turbine [6], traction driver [7], and ventilation [8] applications. Although IGBTs connected in parallel can effectively increase the output current, the power circuit should be designed such that it provides equal current to each IGBT [9]. The authors of [10] demonstrated that the derating of total current must be conducted by considering the current imbalance of IGBTs connected in parallel. They derived a formula that indicates that the derating of total current is 17.4% under an imbalance current ratio of 15% for three IGBTs connected in parallel.

To reduce cost and stock, the inverter used in wind generation applications usually contains multiple IGBT modules connected in parallel for constructing a single-phase power stack. A three-phase inverter is formed using three power stacks [11], [12]. According to the current change rate, the current of a power stack with IGBTs connected in parallel can be divided into static current and dynamic current, which have low and high change rates, respectively. Fig. 1(a) displays the dynamic and static current flow paths of a power stack with IGBT modules connected in parallel in a double-pulse test (DPT) method. The relationship between the IGBT module current and the DPT pattern is shown in Fig. 1(b).
The static current provides the required load current when the low-side IGBT is turned on, and dynamic current occurs at the turn-on and turn-off transients of the low-side IGBT. The main difference between the static and dynamic current flow paths is that static current flows through the load inductor to the POB, whereas dynamic current flows through the parasitic diode of the high-side IGBT and the \( C_{oss} \) of the low-side IGBTs. Because of the low switching frequency of IGBTs in high-power applications, the power stack loss is dominated by static current [13] when compared with short turn-on and turn-off transient times.

Moreover, the DC+ and DC− terminals of IGBT modules connected in parallel should be adjacent to each other on the same side [20], [21] for reducing the stray inductance difference between the DC busbar and each IGBT module. In addition to IGBT modules, the gate driver circuit can effectively improve current sharing. In [19] and [22], active gate voltage control with online IGBT current detection was implemented to achieve superior static current sharing. Because of the requirement of real-time control during the IGBT turn-on period, most circuits are constructed using complex FPGAs, DSPs, and high-bandwidth current sensors [23]. However, such circuits cannot drive parallel IGBT modules by using a single-gate driver. In [24], [25] choking were added to the phase outputs of IGBT modules connected in parallel to achieve balanced current distribution.

Studies [24], [26] have indicated that a gate driver with a common mode choke can achieve balanced static current distribution. A study [14] used a slotted DC busbar to improve dynamic current sharing; however, the optimal method for balancing static current remains unclear because the DC busbar incorporates a small percentage of stray inductance into the static current path. Moreover, the POB of the power stack is used to not only connect the IGBT modules [26]-[28] but also achieve static current balancing for IGBT modules. To ensure static current balancing, some studies [27], [28] have employed the same individual stray inductance from each IGBT module to load terminal in the POB. However, the studies cited in the aforementioned text have not described the POB design method and have not mentioned why the stray inductance of each IGBT path in the POB must be similar for achieving static current balancing. IGBT modules are included in the static current flow path depicted in Fig. 1(a); however, limited research has been conducted on the influence of the stray inductance of these modules on static current balancing. Furthermore, the DPT [22], [29] is generally used to test the current balancing of IGBT modules connected in parallel. Studies [9], [14], [17], [30] are generally used to test the current balancing of IGBT modules connected in parallel. Studies [9], [14], [17], [30]

### TABLE 1. Studies on Current Balancing in IGBTs Connected in Parallel.

| Characteristic of power module | Investigate the influence of \( V_{CEsat} \) stray impedance and temperature on current sharing. | \[14\]-[18] |
| --- | --- | --- |
| Gate driver | New module package provides + and - in the same side to reduce the DC-link stray inductance. | \[20\], \[21\] |
| DC Busbar | Demonstrate placement of the DC link capacitors with slotted busbar which can provide good transient and static current sharing by experiment. | \[14\] |

**FIGURE 1.** Schematic of the power stack used in the DPT: (a) circuit; (b) definitions of the static and dynamic current.

Table 1 summarizes recent studies on current balancing for IGBTs connected in parallel. The factors affecting current distribution are as follows [14], [15]: characteristics of IGBTs, the gate driver circuit, the DC busbar, and the POB. Turn-on saturation voltage, stray resistance, and inductance of IGBTs, and the temperature difference among IGBT modules connected in parallel may affect the current sharing [14]-[18]; therefore, the same die production batch should be preselected and the parallel modules should be connected to the same heatsink to achieve superior current balancing [19].

**TABLE 1.** Studies on Current Balancing in IGBTs Connected in Parallel.
[30] have indicated that the wiring from the load inductor to the POB in the DPT setup affects output current balancing. The aforementioned discussion indicates that appropriately designing the DC busbar and POB is important. The traditional design method for DC busbars is based on Maxwell’s equations for calculating the trend of stray inductance [31], [32]. For complex-shaped POBs and DC busbars, Ansys Q3D or Maxwell 3D has been used for the quantitative analysis of the stray inductance [33]-[36]. The measurement of stray inductance inside the IGBT module is crucial. Studies [18] have only described the measurement of the internal resistance of IGBT modules but have not described the measurement of the stray inductance.

In this study, a single-phase power stack containing three half-bridge IGBT modules connected in parallel was constructed for achieving static current balancing. To design a laminated DC busbar and POB, the Q3D simulation software was adopted for analyzing the stray inductance of the IGBT modules. Moreover, the Simplorer software was used with Q3D to ensure that the stray inductances in the three static current paths of the IGBT modules were nearly the same for achieving static current balancing. The current balancing of the three IGBT modules was analyzed through cosimulations, and the suitability of the design was verified through careful measurements. Finally, a single-phase power stack with a DC link voltage of 1000V was constructed according to the specifications presented in Table 2. to verify the effectiveness of the design. The designed power stack contains a DC link capacitor tank with nine film capacitors (50.R19-764NT1, ELECTRONICON), three half-bridge IGBT modules (Mitsubishi Electric CM1200DW-34T) with 1200A rated current connected in parallel; a single-gate driver (Tamura, 2DUC51008CML1), which is used to drive the IGBT modules; a carefully designed DC busbar; and a carefully designed POB. The results by the DPT method indicated that the maximal current difference among the three IGBT modules was 38A at 200% rated current per IGBT module. Moreover, the maximum ratio of imbalanced current (MRIC) was 0.9% under a 200% (2400A) rated current of an IGBT module. The aforementioned results indicate the effectiveness of the proposed stray inductance design method.

II. DESIGN OF THE POWER STACK

The proposed power stack comprises a DC busbar, DC link capacitors, IGBTs, a gate driver, a heat sink, a POB, and a ferromagnetic-metal housing. The exploded view of this stack is presented in Fig. 2. Because limited energy is required by the designed power stack in the DPT method, the DC link capacitors are regarded as ideal voltage sources, with each capacitor providing the same current for testing in the DPT. Therefore, the stray inductions from the DC busbar, IGBTs, and POB (Fig. 3) are major factors influencing the static current balancing of IGBT modules connected in parallel. Design results indicated that the POB is the main part to be modified for ensuring that the stray inductances are the same.

| TABLE 2. Electrical specifications of proposed power stack. |
|----------------|----------------|
| **Parameter** | **Value** |
| Parallel number of IGBT | 3 |
| Rated input DC voltage (V) | 1000 |
| Peak current under DPT (A/Total) | 7200 |
| Power factor of AC power grid | 0.95 |
| Turn on period under DPT (μs) | 40 |
| Number of phase | 1 |
| MRIC | Within ±3% |

![FIGURE 2. Exploded view of the proposed power stack.](image)

![FIGURE 3. Equivalent circuit of current flow paths for the proposed power stack in the DPT.](image)
B. GATE DRIVER

The adopted gate driver (Tamura 2DUC51008CMCL1), which contains an in-built isolated DC–DC converter and performs soft turn-off and desaturation, is used to drive the three IGBT modules (Fig. 5). The gate driver serves as a master and connects two expansion slave boards with similar matching impedances to drive the three IGBT modules simultaneously. The gate resistance \( R_g \) is 0.6Ω, turn on and off gate to emitter voltage are 15V (\( V_{ge-on} \)) and -9.6V (\( V_{ge-off} \)), respectively.

\[
\begin{align*}
L_{st,S} &= L_s + L_3 + L_4 \\
L_{st,D} &= L_4 + L_2 + L_3 + L_4 - 2M
\end{align*}
\]

Where

- \( L_{st,S} \) and \( L_{st,D} \): total stray inductances of the static and dynamic current paths in the IGBT module, respectively.
- \( L_s \): stray inductance between the phase terminal and the IGBT die.
- \( L_1 \) and \( L_2 \): stray inductances from DC+ to the die and from the die to the \( L_o \) of the high-side IGBT die, respectively.
- \( L_3 \) and \( L_4 \): stray inductances from \( L_s \) to the die and from the die to the DC− of the low-side IGBT die, respectively.
- \( M \): mutual inductance between \((L_1, L_2)\) and \((L_3, L_4)\) under the assumption that the bonding wire is symmetrical in the high- and low-side IGBTs in the IGBT module.

FIGURE 6. Adopted IGBT module (Mitsubishi CM1200DW-34T) and its simplified flat copper bonding model.
\[ R_{\alpha-S} = 0.14\text{m} \Omega \text{ is considerably smaller than } R_X, \text{ the effect of } R_{\alpha-S} \text{ can be disregarded in the further analysis.} \]
D. DC BUSBAR DESIGN

Because of the usage of a high-voltage film capacitor and the need for cost reduction, a double-layer laminated busbar was selected for the designed power stack. To reduce the stray inductance of the DC busbar, the overlap area of the two layers should be as high as possible and the gap between the two layers [42] should be as low as possible under the consideration of safety regulations. The symmetrical connection of capacitors to the DC busbar can reduce the current imbalance [34], [43] among them. Moreover, the connections between capacitors and the DC busbar should have rounded edges for reducing the eddy current loss [34]. Fig. 10(a) depicts the shape and dimension of the designed DC busbar. The current flow starts from the positive terminals of the capacitors, passes through the positive layer to the load inductor, and moves from the POB to the negative layer through the negative terminal of the IGBT modules; finally, it returns to the negative terminals of the capacitors. Therefore, the magnetic field coupling effect occurs. This effect is induced by the current that flows between capacitors and IGBT modules. Consequently, the following assumptions were made in the adopted stray inductance simulation method [Fig. 10(b)]:

1) The DC link capacitors are ideal.
2) The DC busbar can provide balanced current to the three IGBT modules.
3) The connection between the capacitor and the DC busbar can be regarded as a short circuit.

On the basis of the aforementioned assumptions, the DC link capacitors can be regarded as ideal voltage sources, with each capacitor providing the same current. Therefore, the terminals of these capacitors can be set as short circuits during the simulation. In the cosimulation conducted with Simplorer and Q3D, the ideal current with a fixed slope increased from 0 to 2400 A in 80 μs for each current path. These currents were used for determining the stray inductances. The stray inductances of the three parallel paths in the DC busbar are expressed as follows:

\[
\begin{bmatrix}
    v_1 \\
    v_2 \\
    v_3
\end{bmatrix} =
\begin{bmatrix}
    L_{b1} & L_{b2} & L_{b3} \\
    L_{b4} & L_{b5} & L_{b6} \\
    L_{b7} & L_{b8} & L_{b9}
\end{bmatrix}
\begin{bmatrix}
    \frac{di}{dt} \\
    \frac{di}{dt} \\
    \frac{di}{dt}
\end{bmatrix}
\]

(5)

where

\[
\begin{align*}
    v_1, v_2 \text{ and } v_3 & \text{ : induced voltages.} \\
    i_1, i_2 \text{ and } i_3 & \text{ : injected currents.} \\
    L_{b1}, L_{b2} \text{ and } L_{b3} & \text{ : self-inductance.} \\
    L_{b4}, L_{b5} \text{ and } L_{b6} & \text{ : mutual inductance.} \\
    L_{b7}, L_{b8} \text{ and } L_{b9} & \text{ : mutual inductance.}
\end{align*}
\]

If equal injected currents are assumed along the three paths, then \( i_1 = i_2 = i_3 = i \). In this case, (5) can be simplified as follows:

\[
\begin{bmatrix}
    v_1 \\
    v_2 \\
    v_3
\end{bmatrix} =
\begin{bmatrix}
    L_{b1} & L_{b2} & L_{b3} \\
    L_{b4} & L_{b5} & L_{b6} \\
    L_{b7} & L_{b8} & L_{b9}
\end{bmatrix}
\begin{bmatrix}
    \frac{di}{dt} \\
    \frac{di}{dt} \\
    \frac{di}{dt}
\end{bmatrix}
\]

(6)

Where is the equivalent stray inductance in the DC busbar and is expressed as \( L_{sx} = L_{b1} + L_{b2} + L_{b3}, \ x = 1, 2, 3 \).

![Fig. 10. Proposed DC busbar and its stray inductance measurement setup: (a) shape and dimension; (b) measurement setup under simulation.](image)

Fig. 11 depicts the simulated waveforms and results of the DC busbar. The simulated values of \( L_{b1}, L_{b2} \) and \( L_{b3} \) were 22nH, 19nH, and 22nH, respectively. The parameter \( L_{b2} \) is smaller than \( L_{b1} \) and \( L_{b3} \) because of the DC busbar structure and location of load inductor. The maximum difference among the stray inductances was only 3nH, which indicates that the DC busbar design and proposed stray inductance simulation method were effective for achieving near-equal stray inductances among the three current flow paths.

![Fig. 11. Simulated stray inductance values of the DC busbar.](image)
E. POB DESIGN
A T-type POB, which is an improvement over the traditional POB, was designed using Q3D to connect and enable satisfactory current sharing among the three IGBT modules. Fig. 12 presents the structures of the traditional and proposed POB. According to the current flow, the aforementioned POBs can be divided into two parts: the convergence and common parts. The convergence part is used to merge the three IGBT module currents. In Fig. 12, the red, blue, and green paths correspond to the current paths of IGBT 1, IGBT 2, and IGBT 3, respectively. Because the blue path (IGBT 2) of the traditional POB is the shortest path to the load inductance in Fig. 12(a), this path has the lowest stray inductance. This finding is in line with the results of the DC busbar simulation. The proposed POB [Fig. 12(b)] contains a polygonal hollow part for adjusting its stray inductances. Moreover, it compensates for the stray inductance of path 2 (blue path) of the DC busbar. The common part of the aforementioned two POBs is used for conducting current with the same stray inductance; therefore, this part has no influence on the current balancing and can be regarded as part of the load inductor. Consequently, the polygonal hollow part is the only part that affects the current balancing.

![Fig. 12. POB structure: (a) traditional POB; (b) proposed POB.](image)

The design procedure for the proposed POB (Fig. 13) is described as follows:

1) **STEP1: DESIGN THE SIZE OF THE POB**
Because the stray inductances are varied by changing the hollow area, the convergence part of the proposed POB is larger than that of the traditional POB.

2) **STEP2: DETERMINE THE LENGTH (L) AND WIDTH (W)**
The maximum ratio of inductance difference (MRID) and average inductance $L_{POB(Avg)}$ of the convergence part can be defined as follows:

$$MRID(\%) = \frac{|L_{POB,1} - L_{POB,2}|}{L_{POB(Avg)}} \times 100$$ (7)

$$L_{POB(Avg)} = \frac{\sum_{k=1}^{3} L_{POB,k}}{3}$$ (8)

where $L_{POB,1}$, $L_{POB,2}$ and $L_{POB,3}$ are the equivalent stray inductances of the proposed convergence part along three paths.

![Fig. 13. Design procedure for the proposed POB structure.](image)

Fig. 14 displays the simulated results for the relationship among the length (L), width (W), and MRID of the convergence part. The MRID can be minimized by adjusting the hollow dimensions under the assumption that the inductances of paths 1 and 3 in the convergence part are nearly the same because of the symmetrical structure of this part. The simulation results indicated that the smallest MRID is less than 2% in the area where L is greater than 140mm and W is approximately 10–15mm. Because the shape of the POB can be easily adjusted for obtaining the required stray inductances which compared with 20nH average value of the DC busbar, the stray inductance of the convergence part dominates the adjustment of all the stray inductances.

![Fig. 14. Relationship between the hollow dimensions (L and W) and MRID of the proposed convergence part.](image)
Fig. 15 displays the simulated stray inductances of the convergence part for the L and W values presented in Fig. 13. The stray inductances of the three paths are nearly 30\(nH\) which are larger than those of DC busbar when L=140mm and W=15mm. Although the stray inductances can be increased by enlarging the hollow area of the convergence part, the voltage drop induced by the path impedance under a large current must be considered in the design of the POB.

which indicates that the stray inductances of the proposed convergence part are closer and larger than those of the traditional POB. The simulated stray inductances of the common parts of the proposed and traditional POBs were near 100nH and 102nH, respectively. Moreover, the stray inductance of the proposed convergence part along path 2 was marginally higher than those along paths 1 and 3 for compensating for the stray inductance in the DC busbar.

![Graph showing inductance vs length and width](image)

3) STEP3: FINE-TURN THE PROPOSED POB
To compensate for the low stray inductance along current path 2 of the DC busbar, the rectangular area A in Fig. 13 is removed. In addition, the triangular area B is removed to reduce the weight of the POB without affecting the required stray inductance.

The stray inductances simulated method of the POB and DC busbar was similar (Fig. 16). The current sources exhibited a constant-current-slope of 2400A/80\(\mu\)s for testing the convergence part and entire POB. The simulation results of the traditional and proposed POBs are presented in Table 3,

![Diagram of circuit](image)

**TABLE 3.** Simulated stray inductance of the convergence parts of the traditional and proposed POBs.

| Convergence part | Inductance (nH) |
|------------------|----------------|
| Traditional POB | L_{POBC,1} 12.3, L_{POBC,2} 3.7, L_{POBC,3} 12.3 |
| Proposed POB    | L_{POBC,1} 29.3, L_{POBC,2} 31.0, L_{POBC,3} 29.3 |
III. COSIMULATION OF THE STATIC IMBALANCED CURRENT OF THE DESIGNED POWER STACK

For further analyzing the current balancing, cosimulation was conducted using Simplorer and Q3D to predict the current distribution among the IGBT modules and examine the validity of the aforementioned stray inductance and current balancing estimations. Fig. 17 shows the cosimulation setup of the power stack in the DPT. The parameters and settings of the cosimulation environment are listed as follows:

1) The DC source voltage $V_{DC}$ was 1000V.
2) The nine film capacitors had the same electric parameters, and these capacitors, including their ESR and ESL, were connected one-by-one to the nine connectors of the DC busbar that was constructed using Q3D.
3) Because the Spice model of the IGBT modules was not available, the high-side IGBT was assumed to be always off and the low-side IGBT was assumed to be driven by an ideal gate driver in the DPT. Moreover, the relationship between the turn-on voltage $V_{CE(on)}$ of the low-side IGBT and the current was determined using (4) to simulate the behavior of this IGBT.
4) The simulated results of two types of POBs, namely the traditional and proposed POBs, were compared.
5) The output signal of the gate driver was ideal, and the signal sequence comprised two on–off cycles with on and off periods of 40 $\mu$s each.
6) The maximal current of the IGBT modules in the DPT was 200% rated current; thus, the total output current was 7200A for the three IGBT modules, with each IGBT having a rated current of 1200A. The required load inductance was calculated to be 9.5 $\mu$H by considering a $V_{DC}$ of 1000V, which was also assumed to be the voltage drop of the resistance; a maximal current of 7200A; and the signal sequence of gate driver. Moreover, the inductive load was replaced by a RL series circuit in the cosimulation to neglect the magnetic coupling effect induced by the load inductor.
7) Cosimulation was conducted using Simplorer and Q3D to consider the proximity effect caused by various currents along each path of the POB.

Fig. 18 displays the simulated current sharing results for the designed power stack in the traditional and proposed POBs. The inferences drawn from the simulation results are as follows:

1) Because path 2 of the traditional POB exhibited the lowest stray inductance (Table. 3), the peak current of this path ($i_{peak,2}$) was larger than those of the other two paths ($i_{peak,1}$ and $i_{peak,3}$), which were equal.
2) Similarly, $i_{peak,2}$ was smaller than the other two peak currents because path 2 had highest stray inductance, with $i_{peak,1}$ being equal to $i_{peak,3}$ for the proposed POB.
The MRIC can be defined as follows:

\[ i_{\text{peak}(\text{avg})} = \frac{1}{3} \sum_{k=1}^{3} i_{\text{peak},k} \]  

(9)

\[ \text{MRIC}(\%) = \max \left[ \frac{i_{\text{peak},k} - i_{\text{peak}(\text{avg})}}{i_{\text{peak}(\text{avg})}} \right] \times 100 \]  

(10)

where \( i_{\text{peak},k} \) is the peak current of the IGBT module along path \( k \) and \( i_{\text{peak}(\text{avg})} \) is average peak current of the three IGBTs. The MRIC of the traditional and proposed POBs were 5.9\% and 0.8\%, respectively, and the and maximal current difference (MCD) of these POBs were 216 and 30\( \mu \)A, respectively. These results indicate that the proposed POB enabled better current sharing among the IGBT modules than did the traditional POB.

Fig. 19 shows the cosimulation results of current sharing in the power stack in the proposed POB when only considering the convergence part. The three path currents displayed in Fig. 19 are close to those depicted in Fig. 18(b), which indicates that the common part of the POBs had no influence on current sharing. Fig. 20 depicts the stray inductance distribution presented in Table 4. Table 4 summarizes the stray inductances of the DC busbar, IGBT modules, and convergence part of the POB along the three static current flow paths in the designed power stack. The following phenomena can be observed from Table 4:

1) The proposed POB (Design 2) exhibited almost identical stray inductances along the three current paths. Thus, current balancing occurred among the three IGBT modules.

2) Although the stray inductances of the traditional POB varied considerably, the stray inductances of the IGBT modules represented nearly 50\% of the total, thus reducing the influence of traditional POB. Thus, the stray inductances of the IGBT modules have an important influence on static current balancing.

![FIGURE 19. Cosimulation results of current sharing in the power stack in the proposed POB when only considering the convergence part. (Vcc: 1000V, load inductor: 9.5\( \mu \)H, drive signal: ideal PWM, IGBT module: CM1200DW-34T)](image)

![FIGURE 20. Stray inductance distribution of the power stack: (a) the traditional POB; (b) the proposed POB.)](image)

**TABLE 4. Stray inductances (nH) of two type of power stack design.**

| Current flow path | DC busbar | IGBT | Design 1 (Traditional POB (convergence)) | Total | Design 2 (Proposed POB (convergence)) | Total |
|-------------------|-----------|------|----------------------------------------|-------|--------------------------------------|-------|
| 1                 | 22.0      | 30.3 | 12.3                                   | 64.6  | 29.3                                 | 81.6  |
| 2                 | 19.0      | 30.3 | 3.7                                    | 53.0  | 31.0                                 | 80.3  |
| 3                 | 22.0      | 30.3 | 12.3                                   | 64.6  | 29.3                                 | 81.6  |

IV. EXPERIMENTAL RESULTS

Fig. 21 illustrates the proposed power stack and its setup in the DPT. The dimensions of the power stack are 680 \times 425 \times 230\text{mm}^3. The experimental conditions were the same as the simulation conditions. The Lecroy HRO 64Zi and Rohde & Schwarz RTE1054 digital oscilloscopes and PEM CWT Mini HF30B 6kA current probes were used for measurements. The gating signal of the DPT was generated using a DSP-based (TMS320F28075) control board, and the constant-current-slope of load inductor obtained in the DPT had to be the same as that depicted in Fig. 18 for comparing the simulation and experimental results.
using Q3D ($L_{\alpha,S} \approx 30.3 \mu H$) possibly because the IGBT module of Mitsubishi Electric is simplistic. In this module, flat copper is used to connect dies and terminals instead of a multiple wire-bonding model. The stray inductance for flat bonding is smaller than that for wire bonding.

**FIGURE 22.** Measured waveforms of the voltage $V_{CE(module)}$ and current $i_c$ of the lower-side IGBT. ($V_{GS}: 30 V$, load inductor: $0.68 \mu H$, $R_g: 0.6 \Omega$, $V_{ge_{on}}: 15 V$, $V_{ge_{off}}: 9.6 V$, temperature: $25^\circ C$, IGBT module: CM1200DW-34T)

**B. VERIFICATION OF POB INDUCTANCE**

The verification method for the stray inductances in the POB is similar to the inductance extraction in (6). However, in contrast to the simulation, the manufactured POB is an integrated structure and cannot be separated into the convergence and common parts in practice. Therefore, the measured waveforms of the entire POB (Fig. 23) and the measurement setup are the same as those depicted in Fig. 16(b). To reduce the influence of resistances in the POB and measured error caused by high current, the DC voltage is set as $300 V$ to let the peak current be less than 400 A in each current path. The measured and simulated stray inductances are listed in Table 5. The maximal error between the simulation and experimental results is less than 3.1%, which indicates a satisfactory match between the cosimulation and measurement results.

**FIGURE 23.** Measured stray inductance measurements for the proposed POB. ($V_{GS}: 300 V$, load inductor: $9.5 \mu H$, $R_g: 0.6 \Omega$, $V_{ge_{on}}: 15 V$, $V_{ge_{off}}: 9.6 V$, temperature: $25^\circ C$, IGBT module: CM1200DW-34T)
The parameters \( L_{POB,1} \), \( L_{POB,2} \) and \( L_{POB,3} \) denote the entire stray inductances of the proposed POB along paths 1, 2, and 3, respectively.

C. CURRENT SHARING TEST OF SINGLE POWER STACK

Table 6 and Fig. 24 present the experimental results for the three IGBT modules and a comparison between the simulation and experimental results of these modules, respectively. The following inferences can be drawn from the results presented in Table 6:

1) The simulated and experimental MRIC and MCD of the proposed POB were smaller than those of the traditional POB. Moreover, the proposed POB met the design criterion of the MRIC being less than 3%. The simulated and experimental MRIC values of the proposed POB were 0.8% and 0.9%, respectively. In the experiment, the MCD decreased from 161 to 38A when the traditional POB was replaced with the proposed POB. Such a decrease in the MCD can reduce the derating current of the three IGBT modules.

2) The proposed design method of POB can improve current sharing from simulation results as shown in Fig. 18, which are also good match with experimental results. Possibly because the proximity effect on the three IGBT modules was considered in the experiment, which resulted in an increase in the impedance of IGBT 2 for reducing the current along path 2.

| TABLE 5. Simulation and experimental results for the stray inductance of the proposed POB. |
|---|---|---|---|
| Inductance (nH) | \( L_{POB,1} \) | \( L_{POB,2} \) | \( L_{POB,3} \) |
| Simulation | 133.3 | 133.9 | 133.0 |
| Experiment | 128.9 | 131.1 | 133.9 |
| Error (%) | 3.1 | 2.1 | 0.7 |

\[ Error(\%) = \frac{Sim. - Exp.}{Exp.} \]

FIGURE 24. Measured current sharing of the power stack in different POBs: (a) the traditional POB; (b) the proposed POB. (V\( _{DC} \): 1000V, load inductor: 9.5\( \mu F \), \( R_{C} \): 0.6\( \Omega \), \( V_{ge_off} \): 15V, \( V_{ge_on} \): -9.6V, temperature: 25°C, IGBT module: CM1200DW-34T)

Notably, the method of wiring the load inductor in the DPT affects the test results. Fig. 25(a) indicates that the imbalance currents of the IGBTs increased when the wiring of the load inductor was parallel to the POB. Therefore, the wiring of the load inductor must be perpendicular to the POB and DC busbar during the DPT, as depicted in Fig. 25(b), to reduce the effect of electromagnetic coupling on current sharing. In order to keep the maximum current less than 2400A in each IGBT module under serious EM coupling condition, \( V_{DC} \) is adjusted to 800V.

| TABLE 6. Comparison between the simulation and experimental results for the three IGBT modules. |
|---|---|---|---|
| | Simulation | Experiment |
| | MRIC | MCD | MRIC | MCD |
| Traditional POB | 5.9% | 216A | 4.4% | 161A |
| Proposed POB | 0.8% | 30A | 0.9% | 38A |

FIGURE 25. Influence of the method of wiring the load inductor on the current balancing among the IGBT modules by experiment: (a) the wiring is parallel to the POB and (b) the wiring is perpendicular to the POB and DC busbar. (\( V_{DC} \): 800V, load inductor: 9.5\( \mu F \), \( R_{C} \): 0.6\( \Omega \), \( V_{ge_off} \): 15V, \( V_{ge_on} \): -9.6V, temperature: 25°C, IGBT module: CM1200DW-34T)
V. CONCLUSION
In this study, a power stack with equal stray inductances along the static current flow paths in three IGBT modules connected in parallel was developed. Moreover, a cosimulation was conducted with Simplorer and Q3D to guide the design of a DC busbar and POB for achieving current balancing among the three IGBT modules. A power stack with a DC link voltage of 1000V and a maximal output current of 7200A was constructed and tested using the DPT to verify the effectiveness of the design. The main contributions and conclusions of this study are as follows:

1) The current in the IGBT modules was defined as static or dynamic in the DPT. The results of the DPT confirmed that the static current balancing among IGBT modules is mainly affected by the DC busbar, IGBT modules, and POB in the power stack.

2) A method is proposed for measuring the stray inductance along static current flow paths in the IGBT modules to verify the results simulated using a simplified model. The measured and simulated stray inductances were 36.5nH and 30.3nH, respectively. Although the measured value was larger than the simulated value, the simulation results were reasonable because the simulation was conducted using a simplified flat copper wiring model rather than a multiple wire-bonding model for the IGBT modules.

3) A design procedure is proposed for achieving suitable current sharing among IGBT modules connected in parallel. The DC busbar and POB were designed through cosimulation with Simplorer and Q3D to enable each stray inductance along the three static current paths to be nearly equal for achieving static current balancing. The stray inductances could be varied effectively by changing the shape of the hollow part in the proposed POB. The proposed POB exhibited almost identical stray inductance along the three current paths in the simulation.

4) The simulated and experimental MRIC and MCD of the power stack with proposed POB were smaller than those of traditional POB. Moreover, the proposed POB met the design criterion of the MRIC being less than 3%. The simulated and experimental MRIC values of the proposed POB were 0.8% and 0.9%, respectively. In the experiment, the MCD decreased from 161A to 38A when the traditional POB was replaced with the proposed POB. The almost-equal stray inductances along the three static current flow paths in the proposed POB enabled satisfactory current balancing to be achieved among the three IGBT modules.

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