A Hybrid Low-Dropout Regulator with Load Regulation Correction

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This work was supported in part by the Research Grant Council of Hong Kong SAR Government under project no. CUHK 14204917, Direct Grant of CUHK 4055153, Natural Science Foundation of Guangdong Province under project no. 2020A1515011406, and the National Natural Science Foundation of China under project no. 61874143.

ABSTRACT A hybrid low-dropout regulator (LDO) based on proposed load-regulation correction (LRC) is presented in this paper. The proposed hybrid LDO operates at an ultra-low supply of 0.6 V. It provides fast load transient response by proposed three-level switching and achieve high output accuracy by proposed LRC. The hybrid LDO is implemented in a 65-nm CMOS technology. The normalized error of dc output voltage and figure-of-merit are 0.0067 V/V and 0.951 ns, respectively.

INDEX TERMS Hybrid low-dropout regulator, power management, voltage regulator.

I. INTRODUCTION

In power management circuits, low-dropout regulators (LDOs) are widely used as post-regulators of switched-mode dc-dc converters to achieve high accuracy and high efficiency. Analog LDO (ALDO) has the merits of low quiescent current ($I_Q$), fast transient responses, accurate voltage regulation and high power-supply rejection ratio, but its performance is greatly degraded when the supply voltage is close to one threshold voltage of MOSFET [1]–[5]. Digital LDO (DLDO) provides relatively higher driving capability under ultra-low supply [6]–[11], but it has poor regulation accuracy due to quantization errors.

A hybrid LDO structure, shown in Fig. 1 [12], was proposed to combine the accurate small-signal regulation of ALDO and fast large-signal (LS) response of DLDO together. The hybrid LDO in [12] is a parallel structure of DLDO and ALDO, where the ALDO handles about 10–20% of load current while the DLDO controls the remaining 80–90% theoretically. Both DLDO and ALDO are used to handle load transient together, and thus the speed requirements of the ALDO is very demanding. Its loop gain and loop bandwidth are needed to be high which can only be achieved at a high supply voltage ($V_{DD}$) of more than 1.1 V with a high $I_Q$. For the case that the response time of the ALDO is shorter than the recovery time of output voltage ($V_{OUT}$) regulated by the DLDO only, it can supply current to the load with the DLDO together during load transient such that the number of switches to be turned on in the DLDO will not exceed the ideal value for the targeted level of $V_{OUT}$. The supply current from the DLDO is less than the load current. In this case, $V_{OUT}$ is settled to the targeted level perfectly by the ALDO, since the DLDO is frozen within the dead-zone. However, when the response time of the ALDO is longer than the recovery time of $V_{OUT}$ regulated by the DLDO only, the ALDO cannot respond upon receiving load transient and the load current is completely supplied by the DLDO by turning on more switches. The number of turned-on power switches may exceed the ideal value to cause $V_{OUT}$ higher than the target level since the current supplied by the DLDO is more than the load current. In this case, the ALDO in [12] can only source current to the load, and it cannot correct any transient error caused by the DLDO when $V_{OUT}$ is higher than the expected value due to overcharging of the output capacitor by the DLDO. Moreover, it is not possible to use the ALDO in [12], which uses a PMOSFET, to withdraw the excess charges stored at the output capacitor, no matter how to adjust the $V_{SG}$ of the power PMOS transistor, when the required load current is less than the output current from the DLDO where the output current from the DLDO is
discrete which depends on the sizing and number of turned-on power transistors. Due to this reason, the reported steady-state error voltage is high and is 32 mV.

To overcome the problem of the afore-mentioned steady-state error and high demanding of loop gain and loop bandwidth of the ALDO in the hybrid LDO structure, an auxiliary ALDO to achieve the proposed load regulation correction (LRC) is added to deal with relatively smaller error voltage within the dead-zone defined in the DLDO but not the whole load transient response. Thus, the requirements of loop gain and loop bandwidth of the auxiliary ALDO, even at a low supply voltage, are relaxed. The auxiliary ALDO therefore consumes a low $I_Q$, and the loop bandwidth is only a function of the settling time required by the design requirements of the applications.

This paper is organized as follows. Sections II presents the principle of operation, circuit implementation and design issues of the proposed hybrid LDO. Measurement results are reported in Section III. Finally, the conclusion of this paper is given in Section IV.

II. PROPOSED HYBRID LDO

The proposed hybrid LDO is shown in Fig. 2. It includes a DLDO with three-level switching (TLS) formed by a super-coarse, coarse and fine loop, a sinking auxiliary ALDO, and a freeze-mode control. The details of each part of circuits and how the circuit parts interact with each other will be discussed later in this section.

A. Proposed TLS

Coarse-fine switching [6]–[10] is widely used in DLDO to solve the speed limit of load transient response of shift register (SR) based DLDO [11]. The size of the power switches in the fine and coarse loops are $1\times$LSB and $L\times$LSB, respectively, where $L$ is the total number of power switches in the fine loop. Thus, every unit of power switch in the coarse loop can provide $L$-times more of the driving current than the fine loop, to enhance the load transient response of the coarse-fine-based DLDO over the SR-based counterparts. However, the coarse-fine switching shows the shortfalls when the DLDO receives a large and rapid load step. Though a much higher switching frequency ($f_{sw}$) and a larger output capacitance ($C_{OUT}$) can improve load transient response, a higher $I_Q$ and more chip area are needed.
ALDO consists of an error amplifier, NMOSFET and which will be discussed in next sub-section. The sinking Fig. 2 shows the modeling which includes the equivalent To investigate the loop stability of the sinking ALDO, Fig. 4(a) shows the modeling which includes the equivalent resistances from the power switches of DLD0 (i.e., R_{DLDO}) and the load of the hybrid LDO (i.e., R_{LOAD}) into the analysis. A single-stage error amplifier is used, and so there is only one dominant pole at the output of the error amplifier. The system basically has two poles (p_D and p_1), p_D = [R_{OEA}(C_{OPT} + C_D)]^{-1}, where R_{OEA} and C_{OPT} are the output resistance of error amplifier and the gate capacitance of NMOSFET. p_1 = [(R_{OPT}/R_{DLDO}/R_{LOAD})C_{OUT}]^{-1}, where R_{OPT} is the drain resistance of NMOSFET. Based on the expressions of p_D and p_1, it is known that p_D is load independent, while p_1 shifts to a higher frequency for a larger load current. Certainly, the dc loop gain is lower at a higher load current due to the reduction of R_{OPT}, R_{DLDO} (more power switches are turned on for a higher load current) and R_{LOAD}. Since C_{OUT} is in the order of a hundred pF and the output resistance of the hybrid LDO is small due to the small on-resistance of R_{DLDO}, p_1 locates at a frequency higher than the unity-gain frequency (UGF) of the loop-gain response. The loop-gains responses of the light and high load cases are shown in Fig. 4(b). A well design of C_D can easily stabilize the sinking ALDO. As a remark, the UGF of the sinking ALDO is limited to 700 kHz to avoid the effect from p_1 to affect the closed-loop stability.

For the design of the error amplifier, a signal- and transient boosting (STCB) structure proposed in [13], as shown in Fig. 5, is used, since STCB enables ultra-low-voltage operation, such that the sinking ALDO can function properly at V_{DD} = 0.6 V. Moreover, it provides a single-pole characteristic with high gain, where the voltage gain can be designed by the size ratio (i.e., k) of the current mirrors.

To verify the stability of the sinking ALDO, a loop-gain response simulation based on load conditions of the proposed hybrid LDO is used, where the load current ranges between 0.8 mA and 4.9 mA. The simulation results are shown in Fig. 6. The loop gains, UGFs and phase margins at 0.8 mA and 4.9 mA are [30 dB, 690 kHz, 83°] and [20 dB, 210 kHz, 94°], respectively.

Fig. 7 shows the conceptual diagram of the proposed LCR incorporated with the dead zones of the DLD0 in Fig. 2. When the load current (I_{LOAD}) switches from low to high level instantaneously, the hybrid LDO cannot respond
immediately and $V_{OUT}$ drops to $V_{DZ-2}$. The super-coarse loop is activated and turns on more big-size power switches to supply current to the load. Then, $V_{OUT}$ starts to recover and goes into the dead-zone with a lower boundary of $V_{DZ-1}$, the coarse loop is then activated only to supply more current to the load. The fine loop takes the control when $V_{OUT}$ is close to $V_{REF}$. Since the sizing of power switches are discrete, any extra power switch(es) in these three loops turned on will make $V_{OUT}$ go above the desired level. Finally, the whole DLDO is deactivated (or say operating the DLDO in proposed freeze mode), such that only the auxiliary sinking ALDO is enabled to regulate $V_{OUT}$ back to the $V_{REF}$ level. It is noted that the sinking ALDO is disabled when the DLDO is operating. Thus, $V_{OUT}$ is not under the mutual influence by the DLDO and sinking ALDO.

The timing diagrams of the control signals used in the proposed hybrid LDO when the hybrid LDO receives load transient is shown in Fig. 8. The rapid load transient causes $V_{OUT}$ drops and stay beyond DZ2. Then, both $C_{EN1}$ and $C_{EN2}$ are set. The CLR signal for the 4-bit synchronous up-counter is reset, and the freeze-mode control module resets $Q[3:0]$. The $EN$ and $ENb$ signals are also reset and set, respectively, to disable the sinking ALDO by shorting the gate of NMOSFET to the ground (see Fig. 2). The DLDO parts wakes up, but the signal $C_{TEN}$ for the 4-bit synchronous up-counter remains low to prevent the count to progress. In this moment, the super-coarse loop is activated directly to provide the fastest response to load transients, as the SR shifts one count per clock cycle, which is equivalent to an 8-count shift from the coarse loop and a 64-count shift from the fine loop, respectively. Therefore, the undershoot, $T_R$ and settling time can be significantly reduced with the presence of the proposed super-coarse loop. The $UP2$ signal in the DZ2 control block is used to determine if the bi-directional SR in the super-coarse loop shifts up or down. When $V_{OUT}$ is recovered, the number of turned-on power switches in the super-coarse loop is equal to the expected value to meet the requirements of the load. Before returning to the DZ2, the number of the turned-on power switches in the super-coarse loop is still increased by one for every clock cycle. When $V_{OUT}$ is pulled back between $V_{DZ-1}$ and $V_{DZ-2}$, $C_{EN1}$ and $C_{EN2}$ are “1” and “0”, respectively. In this stage, the excess number of the turned-on power switches in the super-coarse loop cannot be removed. Moreover, only the coarse loop is activated to provide a medium resolution and speed for the recovery of $V_{OUT}$, since the SR shifts one count per clock cycle, which is equivalent to an 8-count shift from the fine loop. The $UP1$ signal in the DZ1 control block is used to determine if the bi-directional SR in the coarse loop shifts up or down. When $V_{OUT}$ is within the DZ1, $C_{EN1}$ and $C_{EN2}$ are “0”. In this case, only the fine loop is activated to provide accurate voltage regulation, as the SR shifts one LSB per clock cycle. In this stage, the signal $C_{TEN}$ is high, such that the 4-bit synchronous up-counter in the freeze-mode control module starts to count for 16 clock cycles until $Q[3:0]$ are all set. The clock frequency used for the up-counter is 9.5 MHz, which is one-fourth of the system clock of 38 MHz. These relatively slow 16 clock cycles are used to guarantee $V_{OUT}$ regulated by DLDO part settled in the steady state before further regulation by the sinking ALDO. Once $Q[3:0]$ are all set, the $EN$ signal is set and $C_{TEN}$ is reset to prevent the progression of count to keep all high of $Q[3:0]$. Finally, the SR in the fine loop is frozen, such that the DLDO part cannot perform further action on voltage regulation. When $EN$ is set, the sinking ALDO is activated to further rectify the transient error of $V_{OUT}$. In this proposed design, $V_{OUT}$ which is firstly defined by the fine loop, is designed to be slightly higher the targeted value, and therefore only a sinking ALDO is needed to complete the proposed LCR. The sinking ALDO adjusts the $V_{GS}$ of the NMOSFET to discharge the current difference between the output current of the DLDO and $I_{LOAD}$. The proposed LCR is activated after the DLDO part is frozen. The speed constraints of the sinking ALDO are relaxed to <700kHz under an ultra-low-supply voltage of 0.6 V. Thus, the LCR consumes a very low $I_D$. A higher $f_{on}$ can be used to shorten the time required by the regulation by the DLDO to reduce the effect from the mitigation of unexpected transient errors. As a remark, the recovery time by the LCR is dominant by the loop bandwidth of the sinking ALDO. It is possible to enhance the loop bandwidth of the sinking ALDO to shorten the recovery time significantly, but a higher $I_D$ is needed.

A simulation to show the difference of the hybrid LDO under $I_{LOAD} = 2.5$ mA with and without proposed LCR is
shown in Fig. 9. The errors of $V_{OUT}$ with and without LCR is 0.1 mV and 26 mV, respectively. The results verify the effectiveness of the proposed LCR to reduce regulation error in the steady state.

![Figure 9](image_url)

**Figure 9.** Simulated transient responses of $V_{OUT}$ of proposed hybrid LDO with (left) and without (right) LRC.

### C. Freeze-mode Control Module

The block diagrams of the previously mentioned freeze-mode control module and 4-bit up-counter with reset and enable are shown in Fig. 10(a) and 10(b), respectively. The logic of $C_{TEN}$ is determined by $C_{EN1}$ and $EN$, while the logic of $CLR$ is decided by $C_{EN1}$ and set. Moreover, when $Q[3:0]$ are all set, $EN$ is set. As mentioned before, $EN$ is used to freeze the DLDO and activate the LCR. The 4-bit up-counter functions as a normal counter when both $CLR$ and $C_{TEN}$ are set. However, the up-counter stops counting when $CLR$ and $C_{TEN}$ are set and reset, respectively. To guarantee $V_{OUT}$ regulated by the LRC loop only in the steady state before the next load transient, $C_{TEN} = \text{"0\textquotedblright}$ is essential to keep $Q[3:0]$ when $Q[3:0]$ are all set.

![Figure 10](image_url)

**Figure 10.** (a) Block diagram of freeze mode module, (b) 4-bit up-counter with reset and enable.

The circuit of dead-zone control is shown in Fig. 11(a). All the voltage comparators are the same, and the circuit of comparator is illustrated in Fig. 11(b). When $EN$ is reset, the comparator is operated in the amplification phase. The comparator configured as a pre-amplifier. The difference between $VIP$ and $VIN$ is amplified and accumulated to the parasitic capacitances at $VOP$ and $VON$, which are the inputs of the evaluation phase. When $EN$ is set, the comparator is in evaluation phase. The regenerative latch amplifies the small difference rapidly to full swing. Finally, the NAND-type RS latch is used to provide the overall comparator output (i.e., $CMPOUT$). The same topology of bi-directional SR in [11] is used, and D-type flip-flops with asynchronous set and multiplexers are used. The sampling clock of the super-coarse, coarse and fine loop can be gated to reduce $I_Q$. Moreover, the gated clock in the fine loop is used to freeze the DLDO part in the steady state to allow the LRC to rectify and minimize the errors of $V_{OUT}$.

![Figure 11](image_url)

**Figure 11.** (a) Dead-zone control, (b) dynamic comparator.

The overall structure of the proposed hybrid LDO with proposed TLS and LCR is designed and simulated. The simulation conditions are $V_{DD} = 0.6$ V, $V_{OUT} = 0.5$ V, $C_{OUT} = 120$ pF, $f_{SW} = 38$ MHz, $I_{LOAD(min)} = 0.8$ mA and $I_{LOAD(max)} = 4.9$ mA. The output voltage and current range are suitable for the applications of near/sub-threshold logic designs. The edge time of load transient is 3 ns. Two test cases are simulated. The first case in Fig. 12(a) for $I_{LOAD} = 0.8$ mA to 4.9 mA shows very small error of $V_{OUT}$ because the level of $V_{OUT}$ regulated by the DLDO part is already very close to the targeted value. The other case shown in Fig. 12(b) for $I_{LOAD} = 0.8$ mA to 3.4 mA shows the effectiveness of proposed LCR as the level of $V_{OUT}$ regulated by the DLDO part is above the targeted level. The errors of $V_{OUT}$ before and after rectification by the proposed LCR is 17.6 mV and 0.2 mV, respectively.
III. EXPERIMENTAL RESULTS

The proposed hybrid LDO is designed and implemented in UMC 65-nm CMOS technology. The chip micrograph is shown in Fig. 13, and the active area is 0.008 mm$^2$. The value of $C_D$ is 1.8 pF. The measured $I_D$ is 18 to 165 µA. The difference of $I_D$ is due to the sinking current of the auxiliary ALDO for $I_{LOAD}$ between 0.8 mA to 4.9 mA. The value of $I_D$ without the auxiliary ALDO is 15 µA at $V_{DD} = 0.6$ V and $V_{OUT} = 0.5$ V. The measurement conditions are the same as those used for the simulations shown in Fig. 12. The measured load transient responses are shown in Fig. 14, and they are basically same as the simulation results in Fig. 12. As mentioned before, the case in Fig. 14(a) is for $I_{LOAD} = 0.8$ mA to 4.9 mA. It shows very small error of $V_{OUT}$ because the level of $V_{OUT}$ regulated by the DLDO part is already very close to the targeted value. The undershoot and overshoot of $V_{OUT}$ are 296 mV and 100 mV, respectively, with corresponding response times of 44 ns and 32 ns. The steady-state error of $V_{OUT}$ away from the desired 0.5-V level is within ±3 mV. The other case shown in Fig. 14(b) for $I_{LOAD} = 0.8$ mA to 3.4 mA shows the effectiveness of proposed LCR as the level of $V_{OUT}$ regulated by the DLDO part is above the targeted level. The undershoot and overshoot of $V_{OUT}$ are 246 mV and 100 mV, respectively, with corresponding response times of 42 ns and 38 ns. The steady-state error of $V_{OUT}$ away from the desired 0.5-V voltage level after rectification by proposed LCR is within ±2 mV. From Fig. 14(b), it shows that $V_{OUT} = 0.522$ V before rectification. The errors of $V_{OUT}$ before and after rectification by the proposed LCR is 22 mV and 1 mV, respectively. The undershoot and overshoot can be reduced by a large $C_{OUT}$ and higher $f_{sw}$.

Fig. 15 shows the measured current efficiency for different $V_{DD}$ and $I_{LOAD}$. The results show the current efficiency of more than 95% for the operation range of concern. Fig. 16 shows the measured line regulations for different targeted $V_{OUT}$. The worst-case error voltage of $V_{OUT}$ is 3 mV. Finally, Fig. 17 shows the measured load regulations of individual target $V_{OUT}$ under $V_{DD} = 0.5, 0.54, 0.59, 0.64, 0.69$ and 0.74 V. The worst-case load regulation is 1.46 mV/mA, and this result confirms the effectiveness of proposed LCR.

Table 1 shows the summary of the performances of proposed hybrid LDO and some other state-of-the-art designs for comparison. In the comparison, two important comparison parameters, normalized $V_{OUT}$ error and FoM used in [15], [16] are applied to compare the steady-state accuracy and speed of hybrid/digital LDO, and smaller values of the two parameters reflect higher performance in respective aspect. From the summary, the proposed hybrid LDO outperforms other hybrid/digital LDOs. Though the FoM of the hybrid LDO is smallest, the speed performance was obtained at $V_{DD} = 1.2$ V, in which the analog part in [12] can be activated, as mentioned in the introduction part of this paper. It can be predicted that the design in [12] at $V_{DD} = 0.6$ V with digital mode only should perform worse to result in a poorer FoM. However, under a much lower $V_{DD}$ of 0.6 V than the design in [12], the proposed hybrid LDO shows better speed performance.
IV. CONCLUSION

This paper reports a novel hybrid LDO structure with two proposed circuit ideas: three-level switching and load-regulation correction. Theoretical analysis, simulations and experimental results have been provided to explain and prove the effectiveness of proposed ideas. The load transient response is improved by the proposed three-level switching, and the steady-state accuracy of output voltage is enhanced by the proposed load-regulation correction. The comparison with the state-of-the-art hybrid LDOS has revealed the fact that the proposed hybrid LDO outperforms the others on the steady-state accuracy.

TABLE I COMPARISON WITH STATE-OF-THE-ART WORKS

| Year   | [12] | [15] | [16] | This work |
|--------|------|------|------|-----------|
| CMOS   | 2018 | 2019 | 2020 | 2021      |
| Process| 130-nm | 65-nm | 180-nm | 65-nm     |
| Area [mm²] | 0.0818 | 0.0374 | 0.3 | 0.008     |
| Type | Hybrid | Digital | Digital | Hybrid     |
| F0 (V) | 1.1–1.2 | 0.6–1.2 | 0.6–1.1 | 0.6–0.8 |
| F0 (V) | 0.8–1.1 | 0.4–1.1 | 0.7–1.0 | 0.5–0.74 |
| Max. f0 (MHz) | 1000 | 3.9 | 100 | 38        |
| I0 (mA) | 163.2 | 100–1070 | 500 | 18–165    |
| CoC (nF) | 0.5 | 0.04 | 0.39 | 0.12      |
| ILOAD (mA) | 30µA–12mA | 8–100mA | 10–170mA | 8–49mA |
| ΔVOUT (mV) | 10.27 | 50 | 160 | 4.1 |
| Edge time factor | 32 | 8000 | 650 | 30        |
| Load reg. | 2.64 | 57 | 6 | 4        |
| @F0 = 1V | 0.32 | 0.12 | 0.022 | 1.46 (worst case) |
| Max. FoM error (mV) | 48 | 48 | 10 | 4        |
| Normalized FoM (V) | 0.029 | 0.08 | 0.0142 | 0.0067 (worst case) |
| FoM (ns) | 0.3714 | 1.6 | 1.3 | 0.951     |

Remarks: 1. Data estimated from graphs in the papers
2. FoM = K × CoC × (I0/ILOAD) × (ΔVOUT/ILOAD) [15], [16]

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BIOGRAPHIES

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