Design of Parallel Prefix Adder and Subtractor using Majority Logic Formulations

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Abstract. The New Technology is quantum dot cellular automata at Nano metric scale, which has more focal points like lower area (PLBs) requirement and low Power Consumption. It can not be smaller than the present size transistors. The QCA solution applies to one of the alternative ways to resolve this physical edge. We generated AND gate, OR gate and NOT gate with this QCA invention. With the availability of universal gates in this article, we are allowed to execute any digital logic operation by using majority gates, which have the highest quality class contestant features and achieve the best area delay compromise, such as Brent-Kung Adder (BKA), Kogge stone Adder (KSA), ladner fischer adder (KSA). At last, the adjustments such as delay (speed), power usage, field, ADP and PDP were considered.

Keywords: Delay, power consumption, big cellular gates (MG), adders, quantum dot (QCA).

1. Introduction
The QCA are an appealing rising innovation reasonable for the improvement of ultra-thick low-control elite advanced circuits. Hence, over the most recent couple of years, the plan of productive rationale circuits in QCA has gotten a lot of consideration. Exceptional endeavors are coordinated to number-crunching circuits, with the primary intrigue concentrated on the twofold expansion that is the essential activity of any advanced framework. Obviously, the models regularly utilized in customary CMOS plans are viewed as a first reference for the new structure condition. RCA, CLA, and restrictive whole adders. The CFA was an advanced RCA that moderated effects of impending cables. Parallel prefix systems, including the Bent kung adder, Kogge-stone adder and Han Carlson adder, have been dissected and modified in QCA. CLA and RCA have been suggested for highly powerful structures. This briefly incorporates an innovative technique for fast low-zone add-ons in QCA. Low power voltages and smaller numbers of transistors are used to carry out extended 4-bit full adder[10]. For the confirmation of a novel 2-piece extension cut, theoretical meanings proposed for CLA and parallel prefix adders are here mistaken. The above allows the multiplication to be performed by two following piece positions with only one larger piece of MG postponement. Similarly, the sharp top level building prompts traditionalist configurations, as needs be avoiding unnecessary clock stages as a result of long interconnections. A viper arranged as suggested is still in the RCA style, but it demonstrates a machine compromise less than all work-related requirements and performs the lower ADP.
2. ESSENTIALS OF QUANTUM-DOT CELLULAR AUTOMATA

QCA cells are coulombically represented by partners with adjacent cells to influence the polarization of each other. In review some direct, yet main, QCA rational contraptions in continuing with subsections: a larger portion of the entrance, QCA cables and gradually complicated QCA cell blends. The main contraction in QCA is a QCA cell that allows data to be computed and transmitted. A QCA cell has a hypothetical square room that includes four electronic regions and two electrons. The goals of the contraptions called dots and address the area that electrons can have. They are combined by barriers to the quantum mechanical tunnelling and can be tunnelled by electrons according to the state of the structures. Two versatile electrons are unequivocally packed on the phone and will pass by techniques for electron tunnelling to numerous quantum touches in the QCA cell. The lines of the quantum spots in Figure 1 address the tunnelling methods. Coulombic repulsivity can induce only certain electrons that have two unambiguous polarizations on the sides of the QCA cells. Tunneling is assumed to be completely manageable through possible obstacles that can be avoided and eliminated through capacitive flat techniques between adjacent QCA cells.

![Figure 1. Binary 1 and binary 0 representations and QCA cell polarizations](image)

Twice the approaches of two electrons for the evacuated cell in the QCA cell are vigorously insignificant, the predicted cell polarisation $P=+1$ and the cell polarisation $P=-1$. while cell polarisation $P=+1$ is alluding to parallel 1, whilst the cell polarisation $P=-1$ corresponds to 0. In extension, this idea is graphically portrayed, 1. In an unpolarized state, possible interconnections are reduced, usually decreasing the shown zero polarisation, and the telephone displaced the two electron wave limitations

![Figure 2. unpolarized cell](image)

I counting of specks on the handset is from the upper dab with $i=1$, the base with right $I=2$, the base with left $I=3$ and the upper dab with right $I=4$. In this situation, the counting of specks is clockwise. The polarisation $P$ in a cell is defined as the electronic load of specks $I$. The polarisation estimates the configuration of the charge for example, to what extent the electronic charge is suitable among the four dabs.

The basic QCA sensible circuit is the three-input greater part rationale door that shows up in Figure 2.4 from which progressively complex circuits can be fabricated. The fundamental dominant part entryway is acquired by setting four neighboring cells bordering to a gadget cell, which is in the center. Three of the side cells are utilized as data sources, while the staying one is the yield. The gadget cell is continuously expected that lion share polarisation happens where electron aversion resides at least between the electrons and the gadget cell throughout the three knowledge cells.
In order to explain how the cell is more imperative (and from now on \( P = +1 \) in figure 2), consider the coulombenic interface between cells 1 and 5, cell 3 and 4. In cells 1 and 4 coulombic combinations between cells 1 and 4 will usually make four change the polarisation of the cell with electron stun. (Cell 1 is expected to be a cell). Cells 2 and 3 in both cases have equal effects on cell 4 polarisation and \( P = +1 \) polarisation. In addition it would predict this polarisation since the powers of the Coulombic Interaction have been more grounded on it than on 1 in the light of the fact that most of the cells controlling the contraction cell have Polarization 1P.

3. EXISTING METHOD

Figure 4. Conventional prefix graph of carry C16.

\[
(g_i, p_i) \circ (g_j, p_j) = (g_i + p_i p_j, p_i p_j)
\]

\[
(C_4, -) = (g_3, p_3) \circ (g_2, p_2) \circ (g_1, p_1) \circ (C_1, -)
\]
Figure 5. Prefix-Adder associative operator.

The carry C16 is figured utilizing the prefix affiliated operator with the end goal that produce gi= ai.bi and engender pi = ai+ bi. Fig. 4 demonstrates its prefix diagram. In this segment, another acquainted operator is introduced as far as lion's share rationale for acquiring a structure with decreased intricacy (regarding number of doors and postponement in the adder plan).

The motivation for this new administrator's importance is as per the following. The present administrator needs three greater parts, has deduced crisp qualities to diminish the quantity of prevailing lion's share entryways for this current administrator. All things considered, this can be additionally upgraded on the premise that it lessens the measure of greater part entryway for the viper's just explicit stages. For each activity of the prefix in the plan (fig 4), two lion share entries are needed for each stage – 1 and 2; for the remaining stages, the entry need three large portions of each entry. The planned programme requires only two lion share entries in all stages of the prefix progression. In all prefix implementation times, the proposed arrangement needs only two wider doors and reduces the tests on the gi and pi thoroughly.

4. PROPOSED ADDERS
Fig. 6 displays a parallel n-bit adder map. A = N-1 and N-2 are given for the adder contributions B = bn-1 bn-2 ... Sum = 1 sn-2 ... B1b0 and Cin The outer confines of S1S0 and the conveyor Cn have resulted in better prefix add-ons to simplify the conveyors to the "prefix." Numerous methodologies for efficient representation of Sum and Cn have been suggested. This include the CLA and prefix extensions. Although CLA offers a way to fast expansion of two operand,

![Figure 6](image)

**Figure 6.** N-bit binary adder block diagram

Fig. 7 displays the graphic and key entry graph of the proposed prefix administrator. Fig. Fig. 7 Shows the implied C16 prefix table. The C16 door diagram for the lion is seen in the Fig. 8 (The related prefix administrator suggested is divided in Fig 8 by dabbed lines)

![Figure 7](image)

**Figure.** 7 suggested symbol and key gate diagram for the prefix operator.
Figure 8. Proposed prefix graph of carry C16.

Figure 9. a: Majority gate diagram of proposed Kogge-Stone adder

Figure 9. b: Majority gate diagram of proposed Ladner Fischer adder
The suggested administrator prefix is directly suitable for a broad spectrum of adder prefixes. This paper considers three kinds of prefix adders to be specific adders of KSA, LFA, and BKA. Appeared in the figure are MAJ’s suggested gates for various prefix adders. Fig. 9a reveals the proposed 8-bit KSA MAJ gate map, which requires three steps and four main delay gates to compute all under consideration, so that all conveys in the N-bit adder are calculated by \( \log_2 n \) stages. Fig. 9b displays the 8-bit Ladner-Fischer adder suggested dominant Maj gate chart; all considered items need to be calculated by three phases and four MAJ gates. For an approximation, the LFA n-bit includes \( \log_2 n \) moves. Fig. 9c displays the planned 8-bit BKA Maj Gate Skyline. It calls for five phases and causes for an estimation of six larger MAJ gates. For a BKA n-bit, the number of conveys is \( 2\log_2 n \).

5. PROPOSED SUBTRACTORS

In the previous few QCA-dependent circuits are organised and still are dangerous to changes in cell number and zone, vigour and lack of performance. In this article, a successful complete adder and complete subtractor demanding a smaller cell field, less vitality dispersions were suggested alongside less lion share entrances using a single layer of coplanar wire crossing. In addition, a complete n-bit adder and subtractor have been structured.

5.1. 1-bit Full Subtractor

Generally, the subtraction of two infoA andB with input C is done using a complete subtractor. The comparison 'D' and receive 'B' are the two rates of the subtractor circuit. Thus the outflow can be composed by a 1 bit subtractor

\[
B_0 = A'B + BC + CA'
\]

\[
D = ABC + A'B'C + A'BC' + AB'C'
\]

To execute full subtractor in QCA it required to speak to the articulation as far as MGs, which can be given by
\[ B_o = M_3(A', B, C) \]
\[ D = M_5(A', B, C, B_o', B_o') \]

The schematic depiction of full subtractor circuit is appeared by Fig.10. The utilization of 5-input lion's share door make the circuit more straightforward than utilizing just 3-input MG and inverter.

![Figure 10. Schematic of Full Subtractor design](image)

For an adder of An and B for n-bit, then \( S = A + B \). By then, appreciation of the numbers is the improvement of two. In order to then carry out B-A, the principle of two changes states that each component can be modified by adding one NOT with a door. This gives \( S = B + A' + 1 \), which definitely doesn't have a balanced adder to a certain degree.

The control input D that is furthermore connected with the basic pass on, by then the modified adder performs addition when \( D = 0 \), or difference when \( D = 1 \).

This works since the A commitment to the adder is incredibly \( A_n \) when \( D=1 \) and the transmission in is 1. Adding B to An and 1 outcomes in B-A being preferably subtracted.

The first XOR-door dedication is the certified data-bit, which is used by the XOR door to verify number positively or negatively, without the use of a multiplexer on any part. The second commitment to the XOR portal for each is the input D.

Adders are a piece of the focal point of a normal unit for number of ALU operations. The control unit chooses which undertakings an ALU ought to perform (remembering the activity code being...
performed) and sets the action of ALU. One such control line from the control unit would be the D commitment to the adder subtractor above.

The adder subtractor above could without quite a bit of a stretch be contacted join more limits. For instance, on every Bi, a 2 to 1 multiplexer that would switch among zero and Bi could be spoken to, this could be used (related to D=1) to yield the An enhancement of the two since – A=A+1. An another development is to change the 2 to 1 multiplexer on A to a 4 to 1 with the third data being zero, in this way multiplying it on Bi with the going with output possibilities.

| A=0, B=0, D=0 | Output=0 |
| A=0, B=0, D=1 | Output=1 |
| B=0, D=0      | Output=A |
| A=0, D=0      | Output=B |
| B=0, D=1      | Output=A+1 |
| A=0, D=1      | Output=B+1 |
| D=0           | Output=B+A |
| D=1           | Output=A-B |
| A=A BAR, B=0, D=0 | Output=A BAR |
| A=A BAR, B=0, D=1 | Output=-A |
| B=B BAR, A=0, D=0 | Output=B BAR |
| B=B BAR, A=0, D=1 | Output=-B |

6. SIMULATION RESULTS

Figure 12. N-bit Subtractor simulation waveform
Figure 13. Subtractor RTL Schematic

| Logic Utilization        | Used | Available | Utilization |
|--------------------------|------|-----------|-------------|
| Number of SRAMs          | 1    | 32(16)    | 0%          |
| Number of I/O and LUT4 ports | 0    | 12       | 0%          |
| Number of LUTs           | 2    | 70        | 2%          |

Figure 14. N-bit Subtractor design summary

| Gate | Cell:in->out | Cexit | Delay (ns) | Logical Name (Net Name) |
|------|--------------|-------|------------|-------------------------|
| INBF:1->X | 2 | 0.605 | 0.608 | x1_INBF (x1_INBF) |
| LUT5:24->X | 3 | 0.043 | 0.417 | x5_ml/out1 (horiz) |
| LUT5:23->X | 3 | 0.045 | 0.447 | x5_ml/out1 (vert) |
| LUT5:22->X | 1 | 0.039 | 0.339 | x5_ml/out1 | out_6_QBF |
| OBUF:1->X | 0 | 0.000 | 0.000 | out_6_QBF | outc6b |

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Figure 15. N-bit Subtractor Path delays

Total: 2.371ns (0.171ns logic, 2.199ns route)
(7.28 logic, 92.74 route)
Figure 16. N-bit adder simulation waveform

Figure 17. adder RTL Schematic

Figure 18. Kogge-Stone adder design summary

Figure 19. Kogge-Stone Path delays
7. Conclusion

In this article, we remembered numerous rapid additions as Brent Kung, Kogge stone, and 8 bit Ladner Fischer. The reasoning for QCA majority door alone has been revised. If the area is smaller and the delay is not acceptable, so the area is only ideal where it is imperative. Brent kung adder has an ADP app for the great area delay and a tool for all areas for power delay. We have shown that the Kogge Stone has more space with less time Most entrances are more space, power and time competent.
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