Optimization of CMOS power-cell layout for improving junction breakdown

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Abstract: Complementary metal-oxide-semiconductor (CMOS) power cells for power amplifiers (PAs) were implemented and measured using a standard 0.35-µm CMOS process. An experimental analysis on the effect of substrate resistance on junction breakdown voltage is carried out to optimize the power-cell layout for CMOS PA applications. An optimized power-cell layout for improving junction breakdown voltage is proposed and verified through experiments in this work.

Keywords: CMOS, power cell, substrate resistance, junction breakdown, gate finger, gate finger width

Classification: Integrated circuits

References

[1] A. M. Niknejad, D. Chowdhury and J. Chen: IEEE Trans. Microw. Theory Tech. \textbf{60} (2012) 1784. DOI:10.1109/TMTT.2012.2193898
[2] Y. Omura and K. Izumi: IEEE Trans. Electron. Dev. \textbf{35} (1988) 1391. DOI:10.1109/16.2567
[3] C. Park, J. Han and S. Hong: Microw. Opt. Technol. Lett. \textbf{49} (2007) 3085. DOI:10.1002/mop.22908
[4] M.-D. Ker, C.-H. Chuang and W.-Y. Lo: IEEE Electronics, Circuits and Systems (ICECS) (2001) 361. DOI:10.1109/ICECS.2001.957754
[5] F. C. Hsu, P. K. Ko, S. Tam, C. Hu and R. S. Muller: IEEE Trans. Electron. Dev. \textbf{ED-29} (1982) 1735. DOI:10.1109/T-ED.1982.21018
[6] R. T. Chang, M.-T. Yang, P. P. C. Ho, Y.-J. Wang, Y.-T. Chia, B.-K. Liew, C. P. Yue and S. S. Wong: IEEE Trans. Electron. Dev. \textbf{51} (2004) 421. DOI:10.1109/TED.2003.822586
[7] X. Y. Zhang: Ph.D. dissertation, Dept. Elect. Eng., Stanford University, Stanford, CA (2002).
[8] J. Han, M. Je and H. Shin: J. Korean Phys. Soc. \textbf{42} (2004) 224.
1 Introduction

A radio frequency (RF) PA is one of the most crucial elements in wireless communication systems. Because a PA is designed to drive high power into an antenna or a transmission line, it is the most power-consuming RF component, often dominating the power dissipation of an entire transceiver. Despite the progress in CMOS device technologies and circuit design techniques, implementing a CMOS PA with high output power is still challenging [1]. One of main constraints in the design of CMOS PA is the low junction breakdown voltage in sub-micron CMOS technologies. To achieve the target high output power, a high current level is required for CMOS PA designs. Therefore, deploying a unit device with a longer gate finger width and a larger number of gate fingers is inevitable. A combination of multiple unit devices, generally called as a power cell, is usually required to draw the high current. Large signal performances are mostly dependent on power-cell layout structures. In addition, CMOS device layout parameters such as the gate finger width, the number of gate fingers, and metal line connections influence the junction breakdown characteristics. Several studies have demonstrated the relation between the substrate resistance difference due to layout changes and junction breakdown voltage [2, 3, 4].

In this work, we analyze the variation in breakdown characteristics with respect to variations in gate finger widths, the number of gate fingers, and the number of multiple unit devices. In addition, a method for optimizing the power-cell layout for improving junction breakdown is proposed and verified through experiments.

2 Layout structure of power cell and analysis of junction breakdown voltage characteristics

Fig. 1 shows the cross section of an RF n-type metal-oxide-semiconductor field-effect transistor (NMOSFET) with equivalent parasitic substrate/metal resistances. It also includes parasitic lateral NPN bipolar junction transistors (BJTs) that model the p-type substrate region of the NMOSFET. Drain, p-type substrate, and source generate a parasitic NPN BJT [5]. When a multi-finger device with a larger gate finger width is used for power-cell layout, a parasitic NPN BJT is divided into many individual parasitic NPN BJTs with many individual substrate resistors to represent distributed effects. The effective resistance of the shortest and longest paths between the base of the parasitic NPN BJT and substrate contact line are denoted by $R_{\text{sub1}}$ and $R_{\text{sub2}}$, respectively. $R_{\text{line}}$ indicates the resistance of the substrate contact metal line. The ohmic voltage drop across substrate resistance between the source (the emitter of the parasitic NPN BJT) and the substrate may cause a forward bias the source-substrate junction and turn on the parasitic NPN BJT. In this operational region, the MOS device incurs a junction breakdown [2, 3].

[9] T. Li, C.-H. Tsai, E. Rosenbaum and S.-Mo. Kang: Electrical Overstress/Electrostatic Discharge Symposium Proc. (Eosesd) (2009) 281. DOI:10.1109/EoseSD.1998.737048
Because the substrate bias affects the junction breakdown voltage in the power cell [2, 3, 4], the layout has to be carefully optimized to achieve optimal performance.

Several types of power cells, as listed in Table I, were fabricated using a standard 0.35-µm CMOS process. For all power-cell structures, one side of source diffusion region is connected to the substrate contact line, as shown in Fig. 1.

Breakdown voltages obtained from experiment results are listed in Table I. In Table I, W is the gate finger width of the unit device shown in Fig. 1; N, the number of fingers in the unit device; and M, the number of multiple unit device in the power cell. Thus, total gate width is equal to the product of W, N, and M. In this measurement, the breakdown voltage is obtained when the device is damaged permanently and formed an open circuit.

First, we consider power cells with the same total gate width, but different gate finger widths (Table I, power cell 1–3). Threshold voltages for power cell 1–3 are almost the same and are about 0.4 V. In the case of short gate finger widths, the distance between the base of the parasitic NPN BJT and substrate contact line is

Table I. Power cells and their corresponding breakdown voltages obtained using measured results

| Power-cell number | Width per finger (W) [µm] | Number of fingers (N) | Number of multiple unit device (M) | Total gate width (W × N × M) [µm] | Breakdown voltage [V] |
|------------------|--------------------------|-----------------------|-----------------------------------|-----------------------------------|----------------------|
| 1                | 9                        | 32                    | 2                                 | 576                               | 4.7                  |
| 2                | 6                        | 32                    | 3                                 | 576                               | 5.2                  |
| 3                | 3                        | 32                    | 6                                 | 576                               | 5.8                  |
| 4                | 9                        | 32                    | 1                                 | 288                               | 4.7                  |
| 5                | 9                        | 16                    | 1                                 | 144                               | 4.9                  |
| 6                | 9                        | 8                     | 1                                 | 72                                | 5.3                  |
| 7                | 9                        | 32                    | 1                                 | 288                               | 4.7                  |
| 8                | 9                        | 32                    | 2                                 | 576                               | 4.7                  |
| 9                | 9                        | 32                    | 4                                 | 1152                              | 4.7                  |

*Breakdown voltages were obtained using measured data under 1-V V\textsubscript{GS} condition when the device is damaged permanently and formed an open circuit.
short. As the gate finger width increases, the center of the gate finger moves farther away from the substrate contact, increasing $R_{\text{sub1}}$ and $R_{\text{sub2}}$, which are shown in Fig. 1. The effective substrate resistances vary linearly with the gate finger widths [6]. Therefore, the power cell with a larger gate finger width has worse breakdown characteristics, as shown in Fig. 2. In junction breakdown region, drain-substrate breakdown causes substrate current and in turn drain current will be increased exponentially [7]. However, it is hard to pinpoint the starting point of sudden current increase. Thus, the breakdown voltage in Table I is more specifically defined such that a permanent device damage that forms an open circuit is chosen. The trend of junction breakdown voltage characteristics follows the trend of these breakdown voltage characteristics, as shown in Fig. 2.

Second, different numbers of gate fingers are considered (Table I, power cells 4–6). Even if the width per finger of multi-finger devices is the same, among 8-finger, 16-finger, and 32-finger power cells, the effective resistance of the central finger in 32-finger power cells will be the highest due to the distance between gate finger and the end region of substrate contact line [6, 8]. In Fig. 1, because $R_{\text{line}}$ is the metal resistance, it is much smaller than substrate resistances and can be neglected. Then, the effective substrate resistance becomes a parallel combination of $R_{\text{sub1}}$ and $R_{\text{sub2}}$ ($R_{\text{sub1}} // R_{\text{sub2}}$). Increasing number of gate fingers also increases $R_{\text{sub2}}$, resulting in increased effective substrate resistance. Therefore, the power cell with a larger number of gate fingers shows worse breakdown performance.

Third, when the individual finger widths and the number of gate fingers are unchanged (Table I, power cell 7–9), different numbers of multiple unit devices were observed to exhibit almost similar breakdown performances regardless of the difference in their total gate widths.

According to the measured results, the unit device with a smaller gate finger width and a smaller number of gate fingers appear preferable to achieve better junction breakdown performances. However, without increasing the gate finger width and the number of gate fingers, the number of unit device need to be increased for implementing a larger total gate width device that can draw a high current. Although the effective parasitic resistance is reduced by using the unit
device with a smaller gate finger width and a smaller number of gate fingers, an increase in the power-cell size and parasitic inductance/capacitance is caused. Therefore, a careful layout design is required to improve the overall performance of the power cell.

3 Layout structure optimization and experiment verifications

The optimization process take into account the geometry effect on the distributed substrate-base resistance of the parasitic NPN BJT due to a different location away from the substrate contact. To reduce the substrate resistance between the substrate and an NMOSFET, a pick-up guard ring or a substrate contact is inserted into its source region [2, 3, 4]. Unit device NMOSFET model is provided by CMOS foundry supplier for circuit simulations. Since this model is based on the specific layout geometry, such changes can break the integrity of the model and should be avoided when possible. Thus, in this work, this point is fully considered and there is no major change in the layout geometry.

One side of source diffusion is connected to a body contact, as shown in Fig. 3(a). In the proposed optimized power cell, the NMOSFET layout is surrounded by a substrate contact ring on all sides to minimize the effective substrate resistance, as shown in Fig. 3(b). Each of the power cells has three multiple unit devices. Each unit device has 32 gate fingers, each of which is 6 µm wide. Total

![Diagram](image-url)
gate width is 576 µm in both cases. However, the distributed effect for substrate resistance is different in the two cases and the effective substrate resistance for the power cell shown in Fig. 3(b) will be less than that of the power cell shown in Fig. 3(a). Because the source and substrate terminals are grounded together in a common-source configuration, all the source diffusion region and substrate contacts are connected together via metal layers. The layout contains multiple substrate contacts, which might be at different voltage potential owing to metal routing [9]. Even if the metal resistance of the substrate contact line is much lower than the substrate resistance, it needs to be considered to further minimize the external parasitic resistance. Therefore, three-metal stack is used to minimize additional metal resistances. In addition, both sides of source diffusion regions are connected to body contacts, as shown in Fig. 3(b). Non-uniform current distribution of the power line (source connection line) causes a non-uniform turn-on issue in a parasitic NPN BJT [4]. The case shown in Fig. 3(b) provides more uniform current density distribution, thus preventing the non-uniform turn-on issue.

Both structures were fabricated using a standard 0.35-µm CMOS process. Fig. 4 shows the measured DC characteristics for both structures. The junction breakdown voltage performance is observed to be better in the proposed optimized structure.

4 Conclusions

In this research, the junction Breakdown characteristics of power cells with different gate finger widths and numbers of gate fingers have been analyzed. An optimized power-cell layout for improving the junction breakdown voltage is proposed. All CMOS power cells were fabricated using a standard 0.35-µm CMOS process. The junction breakdown performances vary with variation in gate finger widths and the number of gate fingers. To improve the junction breakdown voltage, $R_{sub}$ and $R_{line}$ need to be minimized. The measurement results show that the optimized power-cell layout improves the junction breakdown voltage performance.
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