Lightweight Hardware Architectures for Efficient Secure Hash Functions ECHO and Fugue
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Abstract—In cryptographic engineering, extensive attention has been devoted to ameliorating the performance and security of the algorithms within. Nonetheless, in the state-of-the-art, the approaches for increasing the reliability of the efficient hash functions ECHO and Fugue have not been presented to date. We propose efficient fault detection schemes by presenting closed formulations for the predicted signatures of different transformations in these algorithms. These signatures are derived to achieve low overhead for the specific transformations and can be tailored to include byte/word-wide predicted signatures. Through simulations, we show that the proposed fault detection schemes are highly-capable of detecting natural hardware failures and are capable of deteriorating the effectiveness of malicious fault attacks. The proposed reliable hardware architectures are implemented on the application-specific integrated circuit (ASIC) platform using a 65-nm standard technology to benchmark their hardware and timing characteristics. The results of our simulations and implementations show very high error coverage with acceptable overhead for the proposed schemes.

I. INTRODUCTION

Cryptographic hash functions take arbitrary-length inputs and generate fixed-length outputs. The output of hash function is then utilized to provide authentication and integrity for the transferred data. In this paper, due to the efficiency of the algorithms ECHO [1] and Fugue [2] (which has been improved to Fugue 2.0), and the fact that these are inspired by the widely-utilized Advanced Encryption Standard (AES), we present their respective fault detection schemes. These AES-inspired hash functions (which have been part of the NIST competition) have received much attention in the literature. For instance, in [3] and [4], differential and side-channel analysis attacks for ECHO are presented. Moreover, much effort has been put into developing high-performance and efficient hardware implementations of these algorithms, see, for instance, [5], [6], and [7]. As discussed in [8], one important feature of these hash functions is that one can share some resources between the AES and these hash algorithms. Thus, low-complexity implementations are achieved.

Fault attacks pose serious threats to the implementations of the crypto-algorithms. Therefore, many fault detection schemes have been proposed to date for cryptographic and arithmetic entities, see, for instance, [9], [10], [11], [12], [13], [14], [15], [16], [17], and [18] for some examples. Nonetheless, to the best of our knowledge, the schemes for increasing the reliability of these algorithms have not been presented in the open literature. Effective fault detection schemes with minimal overhead on these algorithms are essential for achieving reliable hardware architectures.

The summary of our contributions is presented in the following.

• We have obtained new formulations for the predicted signatures of different transformations for hash algorithms, i.e., ECHO [1] and Fugue [2]. The presented closed formulations are used for proposing high-performance and effective fault detection schemes.
• Our simulation results show high fault detection capability for the proposed schemes for all the algorithms. This makes the proposed architectures reliable in practice.
• We have used ASIC implementations to benchmark the hardware and timing characteristics of the proposed schemes. The high efficiency of the proposed schemes makes the proposed architectures suitable for high-performance applications.

II. PRELIMINARIES

ECHO (presented by Benadjila et al.) [1] supports any hash output of length from 128 to 512 bits. The hash function ECHO takes a message and a salt as input. Although the output can be of any length from 128 to 512 bits, the four outputs for NIST competition were 224, 256, 384, and 512 bits. The ECHO algorithm with the output size (\(H_{\text{size}}\)) less than 256, i.e., \(128 \leq H_{\text{size}} \leq 256\), uses the compression function called Compress_{512}. However, for \(257 \leq H_{\text{size}} \leq 512\), the compression function is called Compress_{1024} which is very similar to Compress_{512} [1]. More details are presented throughout the paper as needed.

In what follows, we explain the hash function Fugue (presented by the IBM) [2]. Fugue-256 generates a 256-bit output \(H\) for the message \(M\) which is split into 32-bit blocks \(m_i\), \(1 \leq i \leq t\). The chaining value of Fugue-256 (denoted by \(h\)) is also split to 32-bit blocks denoted by \(S_i\), \(0 \leq i \leq 29\). The following transformation sequence is used for updating \(h\) from \(m_i\): TIX, ROR3, CMIX, SMIX, ROR3, CMIX, and SMIX (called one round \(R\)). The sequence ROR3, CMIX, SMIX is called a sub-round. Therefore, a round \(R\) consists of the TIX transformation followed by two sub-rounds [2]. More details are presented throughout the paper as needed.
The next transformation used in BIG.SubWords of ECHO is ShiftRows whose fault detection is straightforward and by rewiring. Moreover, for the two final linear transformations, i.e., MixColumns and AddRoundKey, the 32-bit error indication flag $Ec = \sum_{r=0}^{3} (in_{r,c} + k_{r,c} + out_{r,c}), 0 \leq c \leq 3$, can be used. It is noted that $in_{r,c}$, $k_{r,c}$, and $out_{r,c}$ are the input to MixColumns, the round key, and the output of AddRoundKey, respectively. This error indication flag can be compressed so that an $n$-bit, $1 \leq n \leq 32$, error indication flag for these two transformations are achieved. Finally, after two rounds of the AES, the output of BIG.SubWords is derived.

Fault detection for the next transformation in ECHO, BIG.ShiftRows, is by permutation. As explained in the aforementioned explanation, the last transformation in BIG.Round, i.e., BIG.MixColumns, is an expansion of MixColumns of the AES. Specifically, the output state of BIG.SubWords (input state of BIG.MixColumns) is arranged as a 4-row, 64-column matrix. Then, each $4 \times 4$ sub-matrix is multiplied by the fixed MixColumns matrix. Therefore, we obtain the error indication flags of the BIG.MixColumns (B.MC) transformation for $j$ sub-matrices, $0 \leq j \leq 15$, as follows

$$Ec_i(B.M.C) = \sum_{r=0}^{3} (in_{r,c} + out_{r,c}), \quad 4j \leq c < 4j + 3,$$

where in the sub-matrices, $in_{r,c}$ and $out_{r,c}$ are the input and output of BIG.MixColumns, respectively, for which $0 \leq r \leq 3$ and $0 \leq c \leq 63$.

Finally, the BIG.Final transformation is performed as the last transformation in each Compress512 (see Fig. 1) of ECHO. This transformation includes modulo-2 addition of the input state of the Compress512 and the output state of the eighth BIG.MixColumns. We present the following lemma for obtaining the predicted parities of this transformation.

**Lemma 1:** Let $M^j_i, 0 \leq j \leq 11$, be the 128-bit message blocks and $A^j_{i-1}, 0 \leq j \leq 15$, be the 128-bit outputs of the eighth BIG.MixColumns of the $i$th Compress512 in Fig. 1. In addition, let $v^j_{i-1}, 0 \leq j \leq 3$, be the previous chaining values. Then, the predicted parities of $v^j_i, 0 \leq j \leq 3$ (the current chaining values), after performing the BIG.Final transformation is obtained as

$$\hat{P}(v^j_i) = \sum_{j=0}^{3} P(v^j_{i-1} + A^j_{i-1}) + \sum_{j=0}^{2} P(M^j_i).$$

**Proof:** According to [11], we have $v^j_i = \sum_{j=0}^{3} v^j_{i-1} + \sum_{j=0}^{1} 4A^j_i + \sum_{j=0}^{1} 5M^j_i$. Therefore, for the predicted parity we reach $P(v^j_i) = \sum_{j=0}^{3} P(v^j_{i-1}) + \sum_{j=0}^{1} P(A^j_i) + \sum_{j=0}^{1} 5P(M^j_i)$ and after rearranging, the proof is complete.

It is interesting to note that one can also obtain multiple parities for $v^j_i$ by applying the parity derivation function $(P)$ to selected bits of the arguments $v^j_{i-1} + A^j_{i-1}$ and $M^j_i$.

**B. Fugue**

To propose a fault detection scheme for Fugue, we observe that the Fugue transformations can be divided into three types. The first type is the rotation transformations, i.e., ROR3, ROR14, and ROR15. The second category contains the two
linear transformations TIX and CMIX. Finally, the last one is the nonlinear transformation SMIX.

Each Fugue round has the following sequence: TIX, ROR3, CMIX, SMIX, ROR3, CMIX, and SMIX. First, we propose the following theorem for the first three transformations TIX, ROR3, and CMIX in the round sequence. Then, we propose the fault detection scheme for the nonlinear transformation SMIX.

Theorem 1: Let \( \sigma_{S_i} = \sum_{i=0}^{29} S_i \) be the 32-bit result of modulo-2 additions of \( S_i \), \( 0 \leq i \leq 29 \) (called word-wise signature). Then, the predicted word-wise signature of the transformations sequence TIX, ROR3, and CMIX \((\hat{\sigma}_{TRC})\) in the Fugue round is obtained as

\[
\hat{\sigma}_{TRC} = \sigma_{S_i} + S_{24}. \tag{3}
\]

Proof. For TIX, the following substitutions are performed:
\( S_{10} \leftarrow S_{10} + S_0, S_0 \leftarrow m_0, S_8 \leftarrow S_8 + m_8, \) and \( S_1 \leftarrow S_1 + S_{24}. \)
Therefore, we have \( \hat{\sigma}_{TIX} = \sigma_{S_i} + S_{10} + S_{10} + S_0 + S_0 + m_0 + S_8 + S_8 + m_8 + S_1 + S_{24} = \sigma_{S_i} + S_{24}. \)

The ROR3 transformation, which is just rotations three positions to right, does not change \( \hat{\sigma}_{TIX} = \sigma_{S_i} + S_{24}. \)
Moreover, for CMIX, we have \( S_0 \leftarrow S_0 + S_0, S_1 \leftarrow S_1 + S_2, S_2 \leftarrow S_2 + S_2, S_{15} \leftarrow S_{15} + S_4, S_{16} \leftarrow S_{10} + S_5, \) and \( S_{17} \leftarrow S_{17} + S_6. \)
Consequently, we reach \( \hat{\sigma}_{CMIX} = \sigma_{S_i} + S_0 + S_0 + S_4 + S_1 + S_5 + S_2 + S_2 + S_{15} + S_15 + S_4 + S_16 + S_{16} + S_5 + S_{17} + S_{17} + S_6 = \sigma_{S_i}. \)
Therefore, one reaches \( \hat{\sigma}_{TRC} = \sigma_{S_i} + S_{24} \) and the proof is complete.

The nonlinear transformation SMIX in Fugue consists of two functions. The second one is the linear Super-Mix function. The Super-Mix function consists of multiplication of \( S_0 \) and \( S_1 \) (as a 16-byte input vector) with the following \( 16 \times 16 \) matrix \( N \) with hexadecimal entries to derive a 16-byte output

\[
N = \begin{bmatrix}
1 & 4 & 7 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 1 & 1 & 4 & 7 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 7 & 1 & 1 & 4 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 4 & 7 & 1 & 1 \\
0 & 0 & 0 & 0 & 0 & 4 & 7 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 4 & 7 & 1 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7 & 1 & 0 & 4 \\
4 & 7 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 7 & 0 & 0 & 0 & 0 & 6 & 4 & 7 & 1 & 7 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 7 & 0 & 0 & 0 & 0 & 1 & 6 & 4 & 7 & 1 & 0 & 0 & 0 & 0 \\
7 & 1 & 6 & 4 & 0 & 0 & 7 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 7 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 7 & 4 & 7 & 1 & 6 & 0 & 0 & 0 & 0 & 0 & 0 & 7 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 4 & 0 & 0 & 0 & 4 & 0 & 0 & 0 & 5 & 4 & 7 & 1 & 0 & 0 & 0 & 0 \\
1 & 5 & 4 & 7 & 0 & 0 & 0 & 0 & 0 & 4 & 0 & 0 & 0 & 4 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 4 & 0 & 7 & 1 & 5 & 4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 4 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 4 & 0 & 0 & 0 & 0 & 4 & 7 & 1 & 5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}. \tag{4}
\]

We propose the following theorem for the predicted parity of the Super-Mix function.

Theorem 2: Let \( I_i \in GF(2^8) \) and \( O_i \in GF(2^8), 0 \leq i \leq 15, \) be the 16-byte input and output of the Super-Mix function in Fugue, respectively. Then, the predicted parity for this function, i.e., \( \hat{P}_{SM}, \) is derived as follows (we note that parity is just an example and any other detecting codes can be utilized)

\[
\hat{P}_{SM} = \{3\}h(I_0 + I_5 + I_{10} + I_{15}), \tag{5}
\]
where the multiplication is performed using the irreducible polynomial \( M(x) = x^8 + x^4 + x^3 + x + 1 \).

Proof. We add the elements of the columns of \( N \) to reach the predicted parity \( \hat{P}_{SM}. \) It is interesting to note that adding the elements in all columns except those in columns 0, 5, 10, and 15 would result zero. For instance, if one adds the elements in column 1 of \( N \) (modulo-2), the result would be \( \{4\}h + \{1\}h + \{1\}h + \{7\}h + \{7\}h + \{1\}h + \{5\}h = 0. \) For columns 0, 5, 10, and 15, the addition of elements results in \( \{1\}h + \{4\}h + \{7\}h + \{1\}h = \{4\}h + \{7\}h = \{3\}h. \) And this completes the proof.

We note that the multiplication with \( \{3\}h = \{2\}h + \{1\}h \) is derived by the addition of \( I_0 + I_5 + I_{10} + I_{15} \) with \( x(I_0 + I_5 + I_{10} + I_{15}) \) mod \( M(x) \).

IV. SIMULATION RESULTS AND ASIC IMPLEMENTATIONS

The proposed error detection architectures have been simulated after injecting faults. The proposed architectures have the capability of detecting both permanent and transient faults (this covers both natural and malicious faults). In this paper, we use stuck-at error model. The objective in using this model is to cover the malicious errors injected by the attackers to break the algorithm (by injecting one or more incorrect bits) and to detect natural errors caused by bit flips. The stuck-at error forces one bit (for single stuck-at error model) or multiple bits (for multiple stuck-at error model) to be stuck at logic one or zero. This makes the result value independent of the error-free intended value.

In fault attacks, single error injection is the ideal case for gaining the maximum information. Nevertheless, due to technological constraints, a more realistic error model is to inject multiple errors. Therefore, for covering both natural errors and fault attacks, multiple errors need to be considered. The proposed diagnosis schemes in this paper are independent of the lifetime of errors. Therefore, both permanent and transient stuck-at errors lead to the same error coverage. We also note that intelligent attackers do not get confined to just multiple stuck-at faults and thus the ability to detect single faults is important.

The fault model used to test the proposed architectures is created using external feedback linear-feedback shift registers (LFSRs) to generate pseudo-random fault vectors that can flip random bits in the output of the gates and at random intervals. For the architectures presented, we have injected up to 80,000 faults and counted the number of errors. We have also used the redundant-basis S-boxes in composite field where applicable. Moreover, the false alarm ratios are derived. The error coverage in all the cases is more than 99% (and for the case of single stuck-at faults, 100% if we harden the error indication flag comparison units), with relatively low ratio for false alarms, i.e., 0.1%-0.3% for the cases. As we inject more faults, the difference between the error detection results is, comparably, not high, showing the relatively high accuracy of the results.

Through ASIC and for the constructions of the algorithms in 256-bit form, we also present the performance and implementation metrics of the presented constructions. The benchmarking is performed for the error detection architectures using TSMC 65nm library and Synopsys Design Compiler (shown in Table I for area, frequency, throughput, and efficiency [throughput over GE]). We note that in Table I, in
order to make the area results meaningful when switching technologies, we have also provided the NAND-gate equivalence (gate equivalents: GE). This is performed using the area of a NAND gate in the utilized TSMC 65-nm CMOS library which is 1.41 $\mu m^2$. The results presented in Table I show acceptable overhead (degradation) for performance and implementation metrics. We also note that the utilized platform is merely for benchmark and we expect similar results on field-programmable gate arrays (FPGAs) or different ASIC libraries.

V. CONCLUSIONS

In this paper, we have proposed efficient fault detection schemes by presenting closed formulations for the predicted signatures of different transformations in three hash algorithms. These signatures are derived to achieve low overhead for the specific transformations and can be tailored to include byte/word-wide predicted signatures. Through simulations, we have shown that the proposed fault detection schemes are highly capable of detecting natural hardware failures and are capable of deteriorating the effectiveness of malicious fault attacks. The proposed reliable hardware architectures have also been implemented on ASIC platform using a 65-nm standard technology to benchmark their hardware and timing characteristics. The high efficiency of the proposed schemes makes the proposed reliable architectures suitable for high-performance applications.

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TABLE I

| Algorithm     | Block (bits) | Area [GE]  | Frequency [MHz] | Throughput [Gbps] | Efficiency [Mbps/GE] |
|---------------|-------------|-----------|-----------------|-------------------|----------------------|
| Proposed      | 1,536       | 145.912   | 389             | 6.6               | 44.4                 |
| ECHO-256      | 181.252 (93%) | 389 (4.6%) | 6.18            | (4.6%)            | 53.03 (25.6%)        |
| Proposed      | 32          | 49.040    | 8.77            | 178.8             | 8.33 (5.1%)          |
| Fugue-256     | 57,900 (18.1%) | 519 (5.1%) | 145,912         | 141.1             | (21.1%)              |

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