Current-mode Positive and Negative Rectifier based on DDCC suitable for Higher Frequency operations

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Abstract. In the present proposal current-mode (CM) full-wave rectifiers (FWR) using a differential-difference current conveyor (DDCC) block, two MOS-based diodes and three grounded resistors. Two proposals of rectifiers are presented, the first is CM FW positive rectifier and the second is CM FW negative rectifier. The value 200MHz was observed in the operating frequency of the simulated designs. The SPICE simulations with 180 nm TSMC CMOS technology model file has been used to ensure the proper functioning of both of the proposals.

Keywords: Analog Building Block, Current Mode, Differential Difference Current Conveyor, Full-Wave Rectifier.

1. INTRODUCTION

A full-wave rectifier that is extensively used in signal processing, instruments and measurements, communications, RF modulators and demodulators, AC voltmeters, ammeters, watt-meters, signal polarity detection, peak detection, function fitter, absolute value computation, in-floor detector used in ultra-sonic, average finder, clipper circuits and frequency doubler [1-10]. The MOS based diodes [3,5,6,8,9] and DDCC have been used in rectifiers but offer a low-frequency range of operations. In some literature shows only diodes [2,4,7,10], Current mode (CM) circuits are more versatile nowadays because of more accuracy, high-frequency performance and wide dynamic range [2,3,7,9]. The second generation of current conveyors (CCII) was introduced in 1970 and its applications are summers, differentiators, integrators, amplifiers, filters, oscillation and controllers [11-14].

The differential difference amplifier (DDA) was first reported in 1987 which has two differential input voltage signals and somehow it behaves like Op-Amp [15-16]. The DDCC was introduced in 1996 and it is a combination of DDA and CCII for high input impedance and arithmetic operations [14,17,18]. Table. 3 shows a comparison of the proposed rectifier to existing rectifiers with different analog building blocks (ABB). The salient features of proposed FWRs:

- Employment of only one ABB.
- Used grounded passive components.
- Used MOS based diodes.
- No matching condition is required.
- Eligible for low power and low voltage systems.
- Suitable for high-frequency operations (MHz).

In the proposal, single DDCC based current-mode positive and negative types of full-wave rectifiers...
have been reported. The three sections are reported including the current section. The circuits structure is defined in Section 1, Section 2 includes the analysis of the proposed circuits and verification using simulations, followed by a conclusion in Section 3.

2. CIRCUIT DESCRIPTION

2.1 Differential difference current conveyor

The DDCC symbol is reproduced in Figure 1. It has three Y-ports with differential inputs, one X-port and one Z-port. The low and the high impedance at input ports X and Y respectively and the high output impedance at Z-port. The matrix characteristic is as follows:

\[
\begin{bmatrix}
I_{Y1,2,3} \\
V_X \\
I_Z 
\end{bmatrix} = \begin{bmatrix}
0 & 0 & 0 & 0 \\
1 & -1 & 1 & 0 \\
0 & 0 & 0 & \pm1
\end{bmatrix} \begin{bmatrix}
V_{Y1} \\
V_{Y2} \\
V_{Y3} \\
I_X
\end{bmatrix}
\]  

(1)

\[I_{Y1} = I_{Y2} = I_{Y3} = 0\]  

(2)

\[V_X = V_{Y1} - V_{Y2} + V_{Y3}\]  

(3)

\[I_Z = \pm I_X\]  

(4)

\[\text{Figure 1. Symbol of the plus-type DDCC [17]}\]

In equation (2) it shows the current at all Y-port is zero, the X-port voltage is proportional and varies with the Y-port voltage in equation (3), and current at X-port varies with Z-port either inward or outward direction in equation (4). The CMOS structure of plus-type DDCC is shown in Figure 2.

2.2 MOS based implementation of DDCC

The (M6 and M7) and (M8 and M9) are two input differential stages. By considering the large gain stage, (M1 and M2) a current mirror transforms the differential signal current to the single-ended output signal current (M3). The M4 is copying the current from M3. Figure 3 and Figure 4 show a full-wave rectifier for positive-type and negative-type respectively.
2.3 Proposed rectifiers

One DDCC block and two MOS can be seen in the designed full-wave rectifier. Here, M1 and M2, two NMOS based diodes are behaving like switches. Equation (5) reveals the output current of the implemented rectifiers. Table 1 is shown the working of rectifiers and resulting outputs.

Figure 2. CMOS structure of plus-type DDCC [17]

Figure 3. Proposed positive full-wave rectifier

Figure 4. Proposed negative full-wave rectifier
Table 1: Working principle of full-wave rectifiers

For positive FWR:

| Input current signal (I_in) | Half cycle | M1          | M2          | Output                  |
|----------------------------|------------|-------------|-------------|-------------------------|
| Sine wave                  | Positive   | ON (FB*)    | OFF (RB*)   | I_in (R_1/R_3)          |
|                            | Negative   | OFF (RB)    | ON (FB)     | -I_in (R_2/R_3)         |
| Triangular wave            | Positive   | ON (FB)     | OFF (RB)    | I_in (R_1/R_3)          |
|                            | Negative   | OFF (RB)    | ON (FB)     | -I_in (R_2/R_3)         |

*RB- Reverse bias, FB- Forward bias

For negative FWR:

| Input current signal (I_in) | Half cycle | M1          | M2          | Output                  |
|----------------------------|------------|-------------|-------------|-------------------------|
| Sine wave                  | Positive   | OFF (RB*)   | ON (FB*)    | -I_in (R_2/R_3)         |
|                            | Negative   | ON (FB)     | OFF (RB)    | I_in (R_1/R_3)          |
| Triangular wave            | Positive   | OFF (RB)    | ON (FB)     | -I_in (R_2/R_3)         |
|                            | Negative   | ON (FB)     | OFF (RB)    | I_in (R_1/R_3)          |

*RB- Reverse bias, FB- Forward bias

The output current equation of the proposed FWR would be:

\[
I_o = I_{in} \frac{R_R - R_z}{R_i}
\]  

(5)

3 SIMULATION RESULTS

The DC transfer characteristic of the implemented FWR is presented in Figure 5 with a dynamic range -300 µA to 300 µA of the current. Figure 6 shows simulated rectified outputs on the transient response of FWR for different amplitudes 100 µA, 200 µA and 300 µA at 1 KHz. The maximum operating frequency is 200 MHz and the respective simulation result is shown in Figure 7 for positive FWR and negative FWR. Figure 8 shows the transient response of the triangular output current for the peak to peak -100 µA to 100 µA triangular input current. The PSPICE simulation results verified using 180 nm TSMC CMOS model file with the supply voltages V_{DD} and V_{SS} is ± 0.9 V and two bias voltages of V_B = - 0.1 V and V_{B1} = - 0.31 V. The values of all resistors are 1 kΩ. The power dissipation of the implemented rectifiers is 2.94 mW. Table 2 illustrates the aspect ratio or Width/Length values for various transistors.

Table 2: Transistor’s sizes for DDCC [18]

| Transistors | Transistor’s Size W(um)/L(μm) |
|-------------|-------------------------------|
| All PMOS    | 10/0.4                        |
| All NMOS    | 05/0.4                        |
Figure 5. DC Transfer characteristics of the proposed FWRs

Figure 6. Transient responses of (a) positive FWR (b) negative FWR

Figure 7. The output current of (a) Positive FWR (b) Negative FWR for sine input at 200 MHz
Figure 8. The output current of (a) Positive FWR (b) Negative FWR for triangular input

Table 3: A comparison of proposed FWR.

| Ref. No. | No. of ABB | Mode of Operation | No. of R | Diode/ MOS | Output Impedance | Operating Frequency (Hz) | P. Diss. (mW) | CMOS Technology | Supply Voltage (V) |
|----------|------------|-------------------|----------|-------------|------------------|--------------------------|---------------|-----------------|-------------------|
| 1        | 1 CCII     | VM                | 0        | 0/0         | H                | 100 M                    | 5.200         | 0.18 µm         | ±1.2              |
| 2        | 1 OTA      | CM                | 2        | 2/0         | L                | 1.00 M                   | NA            | 0.25 µm         | ±1.5              |
| 2        | 1 DVCC     | CM                | 3        | 2/0         | H                | 1.00 M                   | NA            | 0.25 µm         | ±1.5              |
| 3        | 1 EXCCII   | CM                | 0        | 0/2         | H                | 125 M                    | 0.690         | 0.18 µm         | ±1.2              |
| 4        | 1 DXCCII   | VM                | 2        | 2/0         | H                | 10.0 M                   | NA            | 0.35 µm         | ±2.5              |
| 5        | 1 CDTA     | MIXED             | 3        | 0/2         | H                | 10.0 M                   | 1.12          | 0.18 µm         | ±1.5              |
| 6        | 1 Op-amp   | VM                | 1        | 0/2         | H                | 5.00 M                   | 2.050         | 3.00 µm         | -2 to 8          |
| 7        | 1 CDBA     | CM                | 0        | 2/0         | L                | 1.00 M                   | NA            | 0.25 µm         | ±1.5              |
| 8        | 1 OTRA     | VM                | 8        | 0/6         | L                | 1.00 K                   | NA            | 0.18 µm         | ±2                |
| 9        | 1 OFCC     | CM                | 0        | 0/2         | H                | 300 K                    | 0.432         | 0.18 µm         | ±1.8              |
| 10       | 2 VC       | MIXED             | 1        | 2/0         | L                | 1.00 M                   | 0.700         | 0.35 µm         | ±1.65             |
| Proposed | 1 DDCC     | CM                | 3        | 0/2         | H                | 200 M                    | 2.940         | 0.18 µm         | ±0.9              |

H: High, L: Low, CM: Current Mode, VM: Voltage Mode, CCII: Second-generation current-conveyor, OTA: Operational Transconductance Amplifier, DVCC: Differential voltage current-conveyor, EXCCII: Extra-X Current Conveyor, DXCCII: Dual-X Current Conveyor, CDTA: Current Differencing Trans-conductance Amplifier, Op-amp: Operational Amplifier, CDBA: Current Differencing Buffered Amplifier, OTRA: Operational Transresistance Amplifier, OFCC: Operational Floating Current Conveyor, VC: Voltage Conveyor.

4 CONCLUSION

In this work, the DDCC based current mode positive and negative types full-wave rectifiers are proposed. The proposed circuits consist of one single active building block, two MOS based diodes and three grounded resistors suitable from the monolithic implementation point of view. The proposed
circuit has a high impedance at the input as well as output terminals, so best from cascadability point of view. This circuit is useful for a higher frequency, low power consumption, low supply voltage, higher and wider input dynamic range. The PSPICE simulations have been performed using TSMC 180 nm CMOS technology parameters and the supply voltage of ± 0.9V. The full-wave rectifiers output can be achieved for the operating frequency of 200 MHz.

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