Vertical Surrounding Gate Transistors Using Single InAs Nanowires Grown on Si Substrates

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We report on the fabrication and characterization of vertical InAs nanowire channel field effect transistors (FETs) with high-k/metal gate-all-around structures. Single InAs nanowires were grown on Si substrates by the selective-area metalorganic vapor phase epitaxy method. The resultant devices exhibited n-channel FET characteristics with a threshold voltage of around −0.1 V. The best device exhibited maximum drain current (\(I_{D,\text{MAX}}/W_0\)), maximum transconductance (\(g_{m,\text{MAX}}/W_0\)), on–off ratio (\(I_{ON}/I_{OFF}\)), subthreshold slope (SS) of 83 μA/μm, 83 μS/μm, 10⁴, and 320 mV/decade, respectively, for a nanowire diameter of 100 nm.

Epitaxially grown semiconductor nanowires (NWs) are very promising as the building blocks of future device applications, such as field effect transistors (FETs), laser diodes, photovoltaic devices, and so on.¹⁻⁵ For instance, several groups have reported on lateral NW FETs that use horizontally scattered NWs as a channel,⁶⁻¹¹ and some of them remark on the superior properties of these FETs to conventional FETs.¹⁰,¹¹ In contrast, there are very few reports on vertical geometry channel NW FETs because of the complicated three-dimensional device processes.¹²⁻⁻¹⁶ However, epitaxially grown free-standing NWs are geometrically suitable for achieving a surrounding gate structure in vertical FETs, which effectively suppresses short channel effects through excellent gate controllability.

To date, we have succeeded in controlling the position and direction of the growth of a III–V NW array on a Si substrate by using catalyst-free crystal growth techniques. These arrays have potential for a wide variety of applications, such as monolithic integration of high performance III–V logic devices and optoelectronic devices on a Si platform.¹⁷,¹⁸ For FETs, InAs NWs are particularly promising since their small effective electron mass leads to high electron mobility and their property of strong Fermi level pinning on conduction bands leads to good Ohmic contact with various kinds of metals. From these viewpoints, InAs NW vertical surrounding gate transistors (NW-VSGTs) on Si substrates have the potential to surpass conventional complementary metal–oxide–semiconductor devices. In this letter, we report on the fabrication and characterization of NW-VSGTs using InAs NWs grown on Si substrates.

InAs NWs were grown by selective-area metalorganic vapor phase epitaxy (SA-MOVPE).¹⁷⁻⁻²¹ First, a 20-nm-thick SiO₂ film was formed on an n-type Si(111) substrate by thermal oxidation. Subsequently, 100 × 100 μm² square masks with only one circular opening at the center were defined by electron beam lithography and wet chemical etching. Next, single InAs NWs were selectively grown on the partially masked substrate in a low-pressure horizontal-MOVPE system, supplying trimethylindium (TMIn) and arsine (AsH₃) as source materials. The growth conditions were as follows: partial pressure of TMIn, [TMIn], was 4.87 × 10⁻² atm; partial pressure of AsH₃, [AsH₃], was 1.25 × 10⁻⁴ atm; growth temperature was 550 °C; and growth time was 20 min. To achieve vertical III–V NWs on the Si substrates, special care was taken to prepare As-terminated (111) surfaces on the Si substrates prior to the growth. Details of the growth processes are reported elsewhere.¹⁷ A scanning electron microscope (SEM) image of a typical InAs NW array grown on a Si substrate is shown in Fig. 1. The length of each NW was 2.5 μm, and their diameters (dNW) were 100 nm, which is almost the same as the mask opening size.

We fabricated InAs NW-VSGTs using single InAs NWs grown on Si substrates with high-k/metal surrounding gates. Process of device fabrication was as follows. First, after the growth [Fig. 2(a)], the whole surface and NWs were covered with 20-nm-thick HfO₂/Al₂O₃ formed by atomic layer deposition for a high-k gate dielectric [Fig. 2(b)]. Second, tungsten gate metal and its contacting pads were formed by plasma sputtering and photolithography [Fig. 2(c)]. Low-k benzocyclobutene (BCB) resin (Dow Chemical CYCLOTENE) was spin-coated once and then etched back to the desired thickness (≈300 nm) by reactive ion etching (RIE) [Fig. 2(d)], followed by dry and wet etching of the metal and high-k remaining on the top portions of the NWs. At this step, the BCB layer worked as a protection mask for etching, whose thickness defined the gate length, Lg [Fig. 2(e)]. Next, the device was spin-coated again with BCB to obtain an electrical separation layer between the gate and top drain electrode and then etched.

Fig. 1. 45°-tilted view of InAs NW array on a Si substrate.
Back by RIE to a thickness such that only the top portions of the NWs were exposed [Fig. 2(f)]. Subsequently, the drain and source metals (Ti/Al) were evaporated on the top of NWs and bottom side of the substrate, respectively [Fig. 2(g)]. Finally, the gate contacting pads were exposed by RIE [Fig. 2(h)]. A schematic cross-sectional structure and cross-sectional SEM image of NW-VSGT are shown in Figs. 3(a) and 3(b), and one can see that the FET structure was formed as expected.

DC characteristics for a single InAs NW-VSGT were measured using a parameter analyzer (Agilent 4156). The measured device showed the characteristics of an n-type InAs NW-FET with unintentionally doped NW channel, similar to many other reported InAs NW-FETs.\textsuperscript{12,13} The output and transfer characteristics for the device showing the best performances at room temperature are shown in Figs. 4(a) and 4(b), respectively. Note that the substrate is grounded and used as a common source. The measured FET properties were as follows: maximum drain current $I_{ds,max} = 25 \mu A$ (at $V_{DS} = 1 V$), peak transconductance $g_{m,max} = 25 \mu S$ (at $V_{DS} = 1 V$), subthreshold slope $SS = 320 mV/\text{decade}$ (at $V_{DS} = 1 V$), on–off ratio $I_{ON/OFF} = 10^4$ (with $V_G$ window of 2 V), and threshold voltage $V_{TH} = -0.1 V$. $I_{ds,max}$ and $g_{m,max}$ were normalized with the gate circumference, $w_g = \pi d_{NW}$, and given to be 83 $\mu A/\mu m$ and 83 $\mu S/\mu m$, respectively. On the basis of the measured transconductance $g_m$, the field-effect mobility $\mu_{FE}$ was calculated using the formula $\mu_{FE} = g_mL_G/C_{OX}w(G - V_{TH})$ and we obtained a $\mu_{FE}$ of 22 cm$^2$ V$^{-1}$ s$^{-1}$, where $C_{OX}$, the gate oxide capacitance of a cylindrical shape, was given by $C_{OX} = 2\varepsilon_0\varepsilon_{high-k}/d_{NW} \ln(1 + 2t_{ox}/d_{NW})$, $\varepsilon_{high-k}$ is relative permittivity, and $t_{ox}$ is the thickness of the high-$k$ dielectric. This value falls far behind that of bulk InAs electron mobility, which is 33,000 cm$^2$ V$^{-1}$ s$^{-1}$ at room temperature. We think there are two main reasons for the deterioration of $\mu_{FE}$. One is interface states at InAs/HfAlO. The other is in a high source resistance, which originates from the band offset at the interface of Si/InAs NWs. In fact, for the latter, we noticed that the current–voltage characteristics between source and drain were asymmetric with respect to $V_{DS} = 0 V$, particularly for large $V_G$, where the channel resistance is smaller. To minimize this effect, it is necessary to optimize the doping density of the Si substrate and InAs NW by band engineering, or it might be necessary to form a source electrode directly on the bottom of the NWs.
To further evaluate the performance of the present NW-VSGT, we simulated the gate voltage–drain current characteristics for $V_{DS} = 0.5 \, \text{V}$ based on the drift-diffusion equation; the results are plotted in Fig. 2. In the simulation, the same structural parameter ($d_{NW}$, $L_G$, $d_{high-k}$), a donor doping density of $10^{17} \, \text{cm}^{-3}$, electron mobility of 10,000 $\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, and the radial symmetry of the NW were assumed, and velocity saturation effect was taken into account. Here we would like to focus on two points. First, the $SS$ was about 65 mV/decade, while it was 320 mV/decade in the experiment. We believe this discrepancy is mainly attributable to the high interface state density between InAs and the high-$k$ dielectric (HfAlO), which has not been investigated in detail so far. Possible ways to minimize interface state density is to remove native oxides completely before high-$k$ deposition and/or to make a core–shell structure at the \textit{in situ} MOVPE growth step for the passivation or the interface-control layer. Second, drain current and transconductance of simulation values were much superior to experimental ones. This is due to too large mobility used in the simulation, but it is noted that the current does not scale with the value of mobility in the simulation. This suggests that the importance of velocity saturation in short channel device. This makes the estimation of actual value of mobility difficult. In addition, the field effect mobility was deduced neglecting the series resistance including access resistance by hetero potential barrier at Si/InAs interface, as mentioned in the previous paragraph. Existence of interface states further results in the reduction of transconductance and lowers the estimated value of field effect mobility. Therefore, we think obtained value of $\mu_{FE}$ is the lower bound of the mobility in our structure. For the core–shell NW approach, using an n-doped wider gap material as a shell structure also functions as an electron supplying layer, so we can achieve a modulation-doped InAs core channel, resulting in a high electron mobility transistor (HEMT). In simulation, we obtained intrinsic cut-off frequency, $f_T$ of over 150 GHz, which was comparable to planar InP HEMT with gate length of 100 nm. Moreover, optimization of the design of the whole transistor structure, including scaling of the gate length, the diameter and doping density of the NWs, is also necessary to further improve the performance of NW-VSGTs.

In summary, we successfully fabricated and demonstrated InAs NW-VSGTs on Si substrates by using the SA-MOVPE growth method. The devices were $n$-type single NW channel FETs having nonlinear characteristics due to the Si/InAs NW hetero band offset. The FET properties were comparable to other reported InAs NW-FETs, but there is still much scope for improvement.

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