A Graph Partitioning Algorithm with Application in Synthesizing Single Flux Quantum Logic Circuits

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Abstract—In this paper, a new graph partitioning problem is introduced. The depth of each part is constrained, i.e., the node count in the longest path of the corresponding sub-graph is no more than a predetermined positive integer value. An additional constraint is enforced such that each part contains only nodes selected from consecutive levels in the graph. The problem is therefore transformed into a Depth-bounded Levelized Graph Partitioning (DLGP) problem, which is solved optimally using a dynamic programming algorithm. As an example application, we have shown that DLGP can effectively generate timing-correct circuit solutions for Single Flux Quantum (SFQ) logic, which is a magnetic-pulse-based, gate-level pipelined superconductive computing fabric. Experimental results confirm that DLGP generates circuits with considerably lower path balancing overheads compared with a baseline full-path-balancing approach. For example, the balancing overhead (a critical measure of quality metric) for the SFQ circuit realization in terms of D-Flip-Flop count is reduced by 3.61× on average for 10 benchmark circuits, given \( p=5 \).

I. INTRODUCTION

Graph partitioning (GP) consists of dividing nodes of a graph into smaller (typically, equal size) parts to minimize a cost function subject to some constraints. GP plays an important role in many different applications including parallel processing, processing complex networks, image processing, and VLSI design [1]. Partitioning large VLSI circuits has an important impact on placement, routing, and testability of those circuits. A good partitioning can result in lower total wire-length, which has direct impact on reducing the critical path delay of the circuit and total area of the chip. Moreover, in hardware simulation and test, a good partitioning solution can reduce the number of required multiplexers for passing inter-block signals to the bus architecture of the hardware simulator [2]. For GP problems in VLSI, a circuit graph is generated by considering gates or modules as nodes of the graph and wires connecting them as edges of the said graph.

In this paper, we present the Depth-bounded Levelized Graph Partitioning (DLGP) problem as a new GP problem and provide optimal solution for it using a Dynamic Programming (DP) algorithm. Thanks to DLGP, an important problem in the design flow of the superconductive, Single Flux Quantum (SFQ) circuits is addressed. SFQ gates with switching delay of \( 1 ps \) and energy consumption of \( 10^{-19} J \) per switching are considered as potential candidates for achieving super high-performance and ultra energy-efficient systems [3]–[5]. Despite the superiority of SFQ gates in achieving super fast and ultra energy-efficient circuit realization, there are a few challenges in their design flow.

In a SFQ design most circuit elements (including all logic cells) are clocked elements, i.e., each logic cell becomes a pipeline stage. For correct operation of a SFQ logic cell, it is necessary for different inputs of the cell to arrive at the cell input at the same clock cycle. Hence, when different inputs take different path lengths to traverse they must be explicitly path balanced using D-flip-flops (DFFs). In this paper, we will address path balancing overhead as an important challenge in the SFQ circuit design process.

II. PRELIMINARIES

A. Background on Graph Partitioning

Definition: Given a graph \( G = (V,E) \), with non-negative edge weights, \( w: E \rightarrow \mathbb{R}^+ \), and a size \( s(v) \) for each vertex \( v \in V \), the graph partitioning problem (GPP) is defined as dividing set \( V \) into subsets \( V_1, V_2, ..., V_K \) such that Eqs. 1, 2 hold and an objective function (read below) is minimized.

\[
V_1 \cup V_2 \cup ... \cup V_K = V
\]

\[
V_i \cap V_j = \emptyset \quad \forall i \neq j
\]

The above problem is called \( K \)-way partitioning as well. Size of part \( i \) is denoted by \( |V_i| \), i.e., \( \sum_{v \in V} s(v) = |V_i| \). The bounded-size GPP is defined as a GPP problem in which size of the \( i^{th} \) part is bounded by \( B_i \) (\( |V_i| \leq B_i \)). A special case is balanced partitioning, where the size of all parts should be equal modulo a correction factor. More precisely, Eq. 3 should hold:

\[
\forall i \in \{1,2,...,K\}, \quad |V_i| \leq \frac{1+\epsilon}{K} \times |V|
\]

This problem is commonly denoted as a \( (K, 1+\epsilon) \)-balanced partitioning problem. If \( \epsilon = 0 \), the problem is called perfect partitioning, and the special case of \( K=2 \) and \( \epsilon=0 \) is called the minimum bisectioning.

As mentioned before, in GPP an objective function should be minimized. The most used objective function for GPP is the total cut size, which is defined by the following equation:

\[
\sum_{e \in C} w(e)
\]

\[
C = \{e = (u,v) \in E : u \in V_i, v \in V_j, i \neq j\}
\]

Level of a node \( n \) in a graph \( G \) is defined as the length of the longest path in terms of the node count from primary inputs of \( G \) to node \( n \); if nodes of the graph are logical gates, it is called the logic level. Depth of a graph is defined as the highest level among all nodes in the graph. Depth of a part in
Fig. 1: Schematic of an SFQ inverter and its waveforms.

Fig. 2: Gate-level schematic of Example 1 for showing the necessity of path balancing for correct operation in SFQ circuits.

A partitioning problem is the difference between the highest and the lowest levels among nodes of this part plus 1.

B. Background on SFQ

SFQ gates are pulsed-based and the presence and absence of a pulse are considered as “1” and “0”, respectively. A pulse is a single quanta of magnetic flux ($\Phi_0=\hbar/2e=2.07mV \times ps$) with a duration of a few ps and amplitude of a few mV. In the following, some key properties of SFQ circuits are explained.

1) Gate-level pipeline: SFQ gates (except for confluence buffers, splitters, I/O cells, and T-Flip-Flops) need to receive a clock signal and their operation is synchronized by the clock. Fig. 1 shows the circuit diagram of an SFQ inverter and the corresponding waveform to show its functionality. As seen, after the clock pulse comes, when there is no input pulse (which means “0”), a pulse is generated at the output of the gate representing a “1”. On the other hand, when there is an input pulse, no pulses are generated at the output, meaning a “0”.

2) Path Balancing: In standard SFQ circuit design, to guarantee the correct operation, all fanins of a gate should have the same logic level. Otherwise, some path balancing DFFs should be inserted into shorter paths. This is called path balancing. Here is an example of necessity of path balancing in SFQ circuits.

Example 1: suppose that there is a digital signal $a_i=1010...10$ and we want to AND it with invert of another digital signal $b_i=0101...01$. The correct output is: $x1010...10$. The first bit in the output is not valid because in the first clock, second input of the AND gate ($in_{i2}$) is unknown. Without path balancing, generated values at the output of the AND gate will be $x0000...00$ which is not correct (Fig. 2a). The error occurred because the signals on $in_{i2}$ are one level behind the signal on $in_{i1}$. By inserting a path balancing DFF, all fanins of the AND gate will have the same logic level. In the path balanced circuit, as shown in Fig. 2b, the correct sequence of bits are generated at the output of the AND gate.

3) D-Flip-Flops (DFFs) in SFQ: There are two types of DFFs in SFQ: Destructive Read Out (DRO), and Non Destructive Read Out (NDRO). In DROs, after reading the internal data of the DFF, it will be destroyed and cannot be read until another value is written into it. In NDRO, read operation will not destroy the stored data in the DFF.

III. PRIOR WORK

The balanced min-cut k-way partitioning problem is NP-complete [6], [7]. It remains NP-complete even for $K=2$ with identical vertex size and unit edge weight [6], [8]. The first well-known heuristic for solving 2-way balanced partitioning problem is Kernighan-Lin heuristic (K-L) [9]. In K-L, a pairwise interchange process is performed by exchanging vertex pairs that yield the largest decrease in the cut-size. The exchanged vertices are locked and the process continues until all vertices are fixed. A well-known modification of K-L heuristic is presented by Fiduccia and Mattheyses in [10]. Fiduccia and Mattheyses heuristic (F-M) handles unbalanced parts, supports hyper-edges, and has a linear run-time in total number of circuit pins. After F-M, many other papers presented effective partitioning heuristics using simulated annealing [11], multilevel approach [12], network flow [13], [14], spectral methods [15], [16] or a unified approach by combining a few methods [13], [17].

In [18], a module labeling and clustering algorithm is presented which is known as Lawler’s clustering algorithm. In Lawler’s clustering algorithm, an optimal solution for tree clustering to minimize delay with constraints on cluster size and the maximum pin number of each cluster is given. A unity delay model is used for each cluster and it is assumed that delays of interconnects are zero. Lawler’s algorithm provides optimal solution for DAGs if replication of modules are allowed. Rajmohan et al. presented a clustering algorithm for minimizing the delay in combinational circuits [19]. Unlike Lawler’s algorithm, in [19] a general delay model is used and an optimal solution subject to area capacity constraints is given. In [1], [2], [20], [21], good surveys on GP and its applications are given.

Different from other GPPs, in Depth-bounded Levelized Graph Partitioning (DLGP) problem, there is a constraint on the delay of each part while balancing each part in terms of total size is not of an interest. In the standard definition, DLGP is considered as un-balanced partitioning. However, since in DLGP the depth of parts should be the same, it can be called as depth-balanced or depth-limited partitioning. In this context, the standard balanced partitioning problem can be called size-
balanced partitioning problem.

IV. PROBLEM FORMULATION AND PROPOSED ALGORITHM

Depth-bounded Levelized Graph Partitioning (DLGP) problem definition: Given a directed acyclic graph $G = (V, E)$, a mapping function $\Lambda$ which specifies the level of each node in $V$ to be between 1 and a maximum value of $L$ (i.e., the longest node distance from any source node of $G$), and a positive integer $p$, partition set $V$ into $K$ parts $V_1, V_2, ..., V_K$, each of which giving rise to an induced sub-graph $G_1, G_2, ..., G_K$, such that (i) the depth of each sub-graph is no more than $p$, and (ii) if a node of level $l$ is included in some part $V_i$, then all nodes of level $l$ also belong to part $V_i$. Furthermore, the total cut-size (TCS) as defined below is minimized:

$$TCS = \sum_{n=1}^{L-1} \text{cut} \_\text{size}(<\text{Pre}(n), \text{Post}(n)>)$$

where $\text{Pre}(n)$ denotes all nodes $i$ in $G$ belonging to parts $V'_n$ such that $n' < n$, $\text{Post}(n)$ denotes all nodes $j$ in $G$ belonging to parts $V''_n$ such that $n'' \geq n$. $\text{cut} \_\text{size}(<\text{Pre}(n), \text{Post}(n)>)$ denotes the edge separator between levels $n-1$ and $n$ in $G$ i.e., the set of edges in $G$ in which, any node of level $n$ exists between $\text{Pre}(n)$ and $\text{Post}(n)$; $\text{cut} \_\text{size}(<\text{Pre}(n), \text{Post}(n)>)$ calculates the number of edges in $G$ that exist between $\text{Pre}(n)$ and $\text{Post}(n)$ sets.

Next, we define a weighted directed chain graph $C = (U, F, w)$ with nodes labeled 1...$L$ where $L$ is equal to the depth of graph $G = (V, E)$. Each such node represents all nodes of $G$ which are at the same level. There will be a directed edge $uv$ in $F$ between nodes $u$ and $v$ only when $v=u+1$. Weight of the incoming edge to node $v$ accounts for total number of edges connected to any node with level $\geq v$ from nodes with level $< v$. More precisely, if $v=u+1$, the weight $w_{uv}$ of the $uv$ edge is defined as the number of directed edges in $G$ that connect any nodes in $\{\text{Pre}(u), u\}$ and any other nodes in $\text{Post}(v)$. If $v \neq u+1$, $w_{uv}=0$.

Note that the above definition and weight assignment function work equally well for hyper-graphs and hyper-edges (simply add “hyper” before any occurrence of “graph” or “edge”). A directed hyper-edge is one with a distinguished connected node called a source node, thereby, establishing a clear sense of directionality between the source node and all other sink nodes connected by the hyper-edge.

Depth-bounded Chain Graph Partitioning (DCGP) problem definition: Given a weighted chain graph $C = (U, F, w)$ and a positive integer $p$, partition set $U$ into $K$ parts $U_1, U_2, ..., U_K$ such that (i) the depth of each part is no more than $p$, (ii) the total cut weight as defined by Eq. $6$. Notice that $G_i$ is an induced graph obtained from $G$ by including all nodes of $G$ with levels less than or equal to $i$. $\text{OPT}(i)$ denotes the optimal solution for our problem. We initialize $\text{OPT}(i)=\text{OPT}(0)$ for all $1 \leq i \leq p$. Next the value of the optimal solution, $\text{OPT}(i)$, which is defined as the minimum value for $TCW$ for induced graph $G_i$, is calculated recursively as follows:

$$\text{OPT}(i) = \min_q\{\text{OPT}(i-q) + \text{cut} \_\text{weight}(<\text{Pre}(i-q+1), \text{Post}(i-q+1)>)\} \quad \text{for} \quad 1 \leq q \leq p$$

Proof of optimality: It should be shown that the optimal solution of a subset of problem $O(i)$ is built of optimal solutions for its sub-problems. For this purpose, we use the induction hypothesis as follows: suppose that the $i^{th}$ instance of the problem with optimal solution $O(i)$ has a sub-problem $O(i-q)$ with optimal solution $O(i-q)$ and optimal value of $\text{OPT}(i-q) = M$. Suppose that $O(i)$ is built of a solution for $(i-q)^{th}$ sub-problem with value $M' > M$. Let’s call this solution $O'(i-q)$. Now, we can generate another solution for the $i^{th}$ instance of the problem by replacing $O'(i-q)$ with $O(i-q)$. Since $M < M'$, then the new solution for the $i^{th}$ instance of the problem is better than the first one which is a contradiction, because the first solution was supposed to be the optimal solution. Therefore, the optimal solution for $i^{th}$ instance of the problem is built of the optimal solutions for its sub-problems.

Theorem: The DLP problem can be solved optimally. Proof: Using lemma 1 and lemma 2, the proof is straightforward.

After finding the optimal solution, parts can be generated by tracing the $O(L)$ solution back as follows: Generate an empty set of selected levels $N_{sel}$. Add the indices of sub-problems of $O(L)$ to $N_{sel}$, i.e. if $j=q-i$ yields the minimum value for $O(L)$ in Eq. $7$, add $j$ to $N_{sel}$. Repeat these steps for $O(j)$, and trace all the way back to reach the boundary sub-problems. At the end, we will have $N_{sel} = \{m_1, m_2, ..., m_{K-1}\}$. Having $N_{sel}$, the $i^{th}$ sub-set of nodes, $V_i$, corresponding to the $i^{th}$ part in DLP problem is obtained using the following equation:

$$V_i = \begin{cases} \{v \in V | 0 < \Lambda(v) \leq m_i\} & : i = 1 \\ \{v \in V | m_{i-1} < \Lambda(v) \leq m_i\} & : 1 < i < K \\ \{v \in V | \Lambda(v) > m_{K-1}\} & : i = K \end{cases}$$

in which, $\Lambda(v)$ returns the level of node $v$. Algorithm 1 shows the pseudo code of DLP. Complexity of line 1 and also line 4 are $O(m+n)$, where $n$ is the node count and $m$ is the edge
Algorithm 1: DLGP

Input: $G = (V, E)$,
$p$: constraint on depth,
a mapping function $\Delta$ which returns level of a node in $G$.
Output: An optimal set $P = \{V_1, V_2, ..., V_K\}$ of parts.
1 $L = \text{Compute\_Graph\_Node\_Depth}(G)$.
2 if $p \geq L$ then
3 \hspace{1em} return $P = \{V\}$
4 Generate the weighted directed chain graph
5 $C = (U, F, w)$.
6 \hspace{1em} for $i=1$; $i \leq p$; $i++$ do
7 \hspace{2em} $OPT(i) = 0$
8 \hspace{1em} for $i=1$; $i \leq L$; $i++$ do
9 \hspace{2em} Find $O(i)$ and calculate its value, $OPT(i)$, using Eq. 7.
10 \hspace{1em} Find $N_{sel} = \{m_1, m_2, ..., m_{K-1}\}$ by tracing back from the $O(L)$ solution.
11 \hspace{1em} for $i=1$; $i \leq K$; $i++$ do
12 \hspace{2em} Find $V_i$ using Eq. 8.
13 return $P = \{V_1, V_2, ..., V_K\}$.

Example 2: For the graph shown in Fig. 3a with depth $L=5$, by having $p=2$, $K=3$, and using hyper-edges for calculating weights, the corresponding weighted directed chain graph will be as shown in Fig. 3b. Using the DLGP algorithm, the selected levels will be $N_{sel} = \{2, 3\}$, and the sub-set of nodes corresponding to optimal parts will be $V_1 = \{v_1, v_2, v_3, v_4\}$, $V_2 = \{v_5, v_6\}$, and $V_3 = \{v_7, v_8, v_9, v_{10}\}$. Please note that since hyper-edges are used, the edge weights for the weighted directed chain graph will be $\{6, 3, 2, 3\}$ as shown in Fig. 3b instead of $\{7, 4, 4, 3\}$, which is for the case of using regular edges in weight calculations.

V. REDUCING PATH BALANCING OVERHEAD IN SFQ CIRCUITS

Evaluation of SFQ gates is destructive with respect to any internal state (loop current state) of the gate and any incoming input pulses. In other words, after an SFQ gate receives a clock pulse to produce its output, any stored internal state of the gate is destroyed and the input pulse is consumed. For example, if a 2-input AND gate receives a 1 pulse on its input before the clock signal arrives, it will store the said input pulse as a persistent current in one of its internal loops. Next, if the gate receives a second 1 pulse on its input again before the clock comes, it will store this input pulse value in a second internal loop as a persistent current. Finally, when the clock input to the gate arrives, both loop currents will reset (revert back to the other direction of current flow) and an output pulse is reproduced to signify the output for the AND gate. Now consider a situation in which input arrives in clock cycle 1 whereas input arrives in clock cycle 2. One would expect that the AND gate will produce a 0 at the end of clock cycle 1 and a 1 at the end of clock cycle 2. However, this is not the case. In SFQ logic, the AND gate will receive and consume input pulse on in1 during clock cycle 1 producing a 0 output and then it will receive and consume input pulse on in2 in cycle 2, again producing a 0 output. This is precisely why the full path balancing method is employed to make sure that the AND gate will produce the correct 1 pulse output at the end of clock cycle 2.

Our key observation is that to avoid path balancing DFFs, all we have to do is to make sure that the producer of the 1 pulse on in1 produces that same pulse in both clock cycles 1 and 2. Therefore the AND gate will produce a wrong value of 0 at the end of clock cycle 1 but the correct value of 1 at the end of clock cycle 2. So, as long as we initiated new data toward the AND gate with a slow clock frequency which is half of the fast clock frequency used to clock the AND gate, then the AND gate will produce the correct output at multiples of the slow clock.

To the best of our knowledge, this is the very first paper that makes this observation and uses it to effectively eliminate path balancing DFFs inside an SFQ logic circuit although the method comes at the expense of using two different clocks (micro and macro clocks) and a number of NDRO (output-replicating or repeating) DFFs. These NDRO DFFs are read by micro clock and are written by macro clock. Since they are then being read by micro clock, in each cycle of the micro clock the correct pulses will be re-generated and put on the primary inputs of each part. Please note that DRO DFFs cannot be used here, because the read operation in DRO DFFs is destructive, hence they cannot re-generate the correct pulses for $p$ times.

As explained above and in Section II-B2, for correct operation of SFQ circuits, full path balancing is required. One way of addressing the path balancing problem is to add as many DFFs as required to remove any differences among levels of inputs to any SFQ gate. This approach is called Full Path Balancing (FPB). In [22], it is suggested to apply the standard retiming algorithm after a heuristic FPB algorithm to minimize the number of path-balancing

![Fig. 3: (a) Graph of Example 2, (b) Corresponding weighted directed chain graph. Cuts $C_1$ and $C_2$ generate three parts $V_1$, $V_2$, and $V_3$ with minimizing the inter-part net weight.](image)
DFFs (called FPB+retiming). In spite of this algorithm, our experiences show that the FPB+retiming will add a large number of DFFs to the circuit which can dominate the original gate count in the network even considering the fact that the area cost of an SFQ DFF is somewhat less than the area cost of say 2-input SFQ AND gate [24]. In this section, we will show how DLGP algorithm helps solving this problem.

As hinted earlier, we propose to use a fast micro and a slow macro clock and to use the DLGP algorithm to minimize the aforementioned overheads of FPB. Thanks to the DLGP algorithm, it is possible to divide the corresponding graph of a given SFQ circuit into a few depth-limited parts and add NDRO DFFs only on the hyper-edges which are cut by various part boundaries. These DFFs will pass values that go from one part to the other one with the macro clock, while gates inside each part operate with the micro clock. Since the DLGP algorithm guarantees giving the minimum total cut weight, the number of inserted NDRO DFFs in the circuit will be minimized. Furthermore, since the NDRO DFFs which are placed at the inputs of each part are also clocked by the micro clock to continuously reproduce their outputs, there is no need to add any path balancing DFFs inside each part. The resulting SFQ circuit is thus functionally pipelined allowing a number of $K$ data instances to exist in the circuit at the same time, each being operated in the corresponding part of the $K$-part circuit. The number of parts will thus affect the total operational throughput of the circuit (when there are no pipeline installs). Fig. 4 shows FPB, and DLGP-based Dual Clocking Method (DCM) for an example circuit. As seen, the DLGP-based DCM requires 4 fewer number of DFFs compared with FPB. Note that although NDRO DFFs are more expensive than the DRO DFFs, the reduction in total DFF count far outweighs this difference in element cost. See experimental results.

In our DLGP-based DCM, the depth of each part is at most $p$. Since gates in each part are evaluated by the micro clock and the speed of micro clock is $p$ times faster than the macro clock, between two consecutive edges of the macro clock, $p$ different values will hit the inputs of DFFs at the inter-part boundaries. If every such value reaches the NDRO DFFs, this will cause wrong values to be stored in the NDRO DFFs, which will be passed to the next part. Indeed we want that only the value which is generated in the last cycle of the micro clock is written into the NDRO DFFs, because only this value is valid. This issue can easily be addressed using the following pulse-repeating gate and by ensuring that the macro clock is synchronized with the micro-clock but has a clock frequency which is $p$ times slower.

1) Pulse-Repeating Gate: We have invented an SFQ pulse-repeating gate shown in Fig. 5 to address the aforesaid challenges in the DLGP-based DCM. In this gate, an AND gate is added to the input of the NDRO DFF gate. One of the inputs of this AND gate is connected to the macro clock which is “0” while the correct value is not generated on the “in” port. Therefore, it will pass a “0” to the input of the NDRO DFF as desired. Only in the last cycle of the micro clock the AND gate will be transparent and pass the valid value to the NDRO DFF. In addition, due to usage of NDRO DFF, inputs of each part will be re-generated (repeated) at each cycle of the micro clock.

Before passing these circuits to the DLGP-based DCM, they are passed to the technology mapping engine of ABC [25] and its default optimization are performed on them. After that, mapped circuits are passed to the DLGP algorithm to find the optimum places for inserting pulse-repeating gates. After this step, splitter insertion and balancing of Primary Outputs (POs) are performed. Algorithm 2 shows the pseudo code for DLGP-based DCM. In line 1, the given circuit is mapped using the technology mapping engine of ABC. In line 2, the optimal parts are determined. In line 3, the pulse-repeating gates are inserted on the hyper-edges which are cut. Line 4 takes care of balancing POs, and finally, line 5 inserts the required splitters.

VI. EXPERIMENTAL RESULTS

We implemented the DLGP algorithm inside ABC. An SFQ library of gates as in [24] is used. This library consists of the following gates: \texttt{and2} with 12 JJs, \texttt{or2} with 8 JJs, \texttt{xor2} with 8 JJs, \texttt{DFF} with 7 JJs, \texttt{splitter} with 3 JJs, \texttt{JTL} with 2 JJs, and \texttt{not} with 9 JJs. A few benchmark circuits from ISCAS [26], EPFL [27], and some other arithmetic circuits are chosen to test the effectiveness of the proposed algorithm in reducing the overhead of FPB.
Algorithm 2: DLGP-based Dual Clocking Method

Input: a graph $G = (V, E)$ corresponding to the input circuit,
p: constraint on depth
Output: A timing-correct circuit represented by graph $G' = (V', E')$

1. $G_m = Technology\_Mapping(G)$
2. $Parts = \{V_1, V_2, \ldots, V_k\} = DLGP(G_m, p)$
3. $Pulse\_Repeating(G_m, Parts)$
4. $PO\_Balancing(G_m)$
5. $G' = Splitter\_Insertion(G_m)$
6. return $G'$

Tables I and II show experimental results for DLGP-based DCM with two values for $p$, 10 and 5. For a better comparison, two baselines are considered: Baseline1 is the FPB, and Baseline2 is the FPB-retiming algorithm. As seen, DLGP-based DCM provides substantial savings in total number of Josephson junctions (#JJs), area, run-time, and DFF count (#DFFs). Area and #JJs are area and JJ count for gates, DFFs and splitters. The overhead of AND gates (in pulse-repeating gates) and second clock in DLGP-based DCM are considered in the experimental results of DLGP. #DFFs for DLGP includes NDRO DFFs inserted to the boundary of parts and DRO DFFs used for PO balancing. In DLGP-based DCM and both baselines, the cut-based technology mapping of ABC (command “map”) which involves a delay optimization pass followed by a few area optimization passes is employed. Other than what mentioned so far, no other optimization function is used.

DLGP-based DCM for i10 MCNC benchmark circuit consumes 1.54× and 1.37× fewer #JJs compared with Baseline1 and Baseline2, respectively when $p=10$. For the same, DLGP-based DCM provides 2.24× and 1.65× improvements on total area, and 6.85× and 4.47× improvements on #DFFs compared with Baseline1 and Baseline2, respectively. For $p=5$ the amount of improvements are less than these values. For example, for the same circuit, the saving of 2.24× and 1.65× on area is reduced to 1.50× and 1.09×, and the saving on #DFFs is decreased from 6.85× and 4.47× to 3.99× and 2.60× all compared with Baseline1 and Baseline2, respectively.

On average for all 10 benchmark circuits, the saving on area, #JJs, and #DFFs for DLGP-based DCM when $p=10$ is 89%, 77%, and 7.7×, respectively over Baseline1 and 30%, 23%, and 4.26×, respectively over Baseline2. The reason behind not seeing the huge saving of #DFFs in the total area is the overhead of second clock and also the AND switches used in the pulse-repeating gates. DLGP-based DCM also decreases the run-time significantly. For example for c432 benchmark circuit, the run-time is decreased by 3.10× and 6.63× when $p=5$ compared with Baseline1 and Baseline2, respectively. The main reason behind larger run-time for baselines is requirement of inserting many DFFs plus performing retiming, which both are slow processes specially for large benchmark circuits. We tried to extract experimental results for larger benchmark circuits (larger than voter with 13758 nodes, 1002 IOs, 27516 edges, and 13758 cubes which is already reported in Tables I and II) such as log2 and hypotenuse [27], but the memory of our system (64GB RAM) was not enough for finishing DFF insertion and retiming steps of Baseline1 and Baseline2, and the processes were killed after 30+ minutes.

To verify the correct operation of the circuits, we simulated a 2-bit Kogge-Stone Adder (KSA2) generated by DLGP-based DCM given $p=2$. Four sets of random values as shown in Fig. 6 are applied to the inputs and for all of them the correct outputs are generated. Please note that since $p=2$, the inputs are repeated and there are 2 copies of each input.

These savings come in one expense; the peak throughput of circuits generated by DLGP-based DCM will be roughly $p×$ less than FPB method. This is because the effective frequency of these circuits is the same as macro clock compared with the frequency of circuits generated by FPB which is micro clock. Note that the actual throughput is typically much less than the peak throughput (due to instruction data dependencies, program branches, etc.); so some throughput loss may be acceptable. In addition, due to the following property of SFQ circuits, the throughput loss will be less than $p×$ after place-and-route; in SFQ circuits, the delay of interconnects are typically larger than the delay of gates, hence, the longest interconnect usually determines the worst case delay. Therefore, since DLGP-based DCM reduces the total gate count significantly, it will help reducing the length of the longest interconnect, resulting in having faster local clock frequency. This helps gaining some of the lost throughput in DLGP-based DCM. For example, the throughput loss for ISCAS c432 circuit generated by DLGP-based DCM ($p=5$) after place-and-route is reduced to 4.3× compared with FPB. A more advanced wire-routing method such as what presented in [28] can help reducing this gap further.

VII. Conclusion

This paper introduces a new graph partitioning problem called Depth-bounded Levelized Graph Partitioning (DLGP). In DLGP, there is a depth constraint on the resulting subgraphs of each part. We showed that by transforming the DLGP problem into a Depth-bounded Chain Graph Partitioning (DCGP) problem, an optimal solution which minimizes the total cut set is achieved using the Dynamic Programming

Fig. 6: Simulation results for a 2-bit Kogge-Stone adder (KSA2) generated by DLGP-based DCM given $p=2$. clk refers to the fast clock. Four sets of random inputs are applied: $a_0=1010, a_1=0101$, $b_0=0111, b_1=1100$, $c_0=1001, c_1=0101$. The correct outputs are: $S_0=0101, S_1=0011, C_{out}=1100$, which are generated every 2 clock cycle (fast clock).
algorithm. It is shown that DLGP algorithm can be applied to SFQ circuits for reducing the path balancing overheads. Experimental results show that if the depth constraint is equal to 5, this overhead reduction is as high as $3.8\times$ in terms of JJ count, and $4.79\times$ in terms of DFF count.

### Table II: Comparing DFF count for DLGP-based DCM and two baselines.

| circuits | Baseline1 | Baseline2 | #DFFs Baseline1 | #DFFs Baseline2 | #DFFs DLGP(5) | #DFFs DLGP(10) |
|----------|-----------|-----------|------------------|-----------------|--------------|--------------|
| i10      | 12832     | 8382      | 3219             | 1872            |
| c1908    | 1004      | 683       | 282              | 144             |
| c1355    | 614       | 442       | 193              | 119             |
| c432     | 847       | 655       | 224              | 118             |
| c880     | 1345      | 772       | 362              | 187             |
| c3540    | 2848      | 1220      | 776              | 282             |
| voter    | 18491     | 11114     | 7204             | 3732            |
| int2float| 539       | 277       | 117              | 39              |
| ADD16    | 235       | 200       | 104              | 50              |
| MULT16   | 21373     | 3390      | 4460             | 2111            |

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