Research of the operation voltage limiter in pulsed mode

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Abstract. This paper presents the results of investigations on the matter of withstanding power and switch-on time of the voltage limiter operating in a pulsed mode. The voltage limiter is based on a silicon p⁺−n−n⁺ structure obtained using the «batch» method of simultaneous two-way diffusion of boron and phosphorus out of solid phase.

1. Introduction
The transistor, diode or thyristor semiconductor structures utilized for data transmission and processing systems produce a capacitive current while operating. If no proper elimination measures are taken, this current leads to a deterioration in noise immunity and reliability of the entire electronic circuit. As reported in the work [1], a capacitive current increases the duration of the output voltage transition to a high level state and increases the resorption time of carriers. To suppress the influence of capacitive current, the authors of work [2] propose to create a low-impedance capacitive current tap circuit using a voltage limiter instead of traditional resistor. The advantage of the voltage limiter lies in its very low impedance in switch-on mode, as well as its high frequency range. However, these parameters differ from each other depending on the technology and design of a particular voltage limiter. The shorter the carrier resorption time, the less time it takes for an output voltage to rise and the greater the frequency range, thus expanding the range of voltage limiter application [3].

This paper presents the results of investigations on the matter of withstanding power and switch-on time of the voltage limiter operating in a pulsed mode. The voltage limiter is based on a silicon p⁺−n−n⁺ structure obtained using the new «batch» method [4] of simultaneous two-way diffusion of boron and phosphorus out of solid phase.

2. Materials and Experimental Procedures
The voltage limiters based on silicon p⁺−n−n⁺ structures utilized in the study are produced using diffusion technique. n-type silicon of «КЭФ» grade (i.e. phosphorous doped silicon with electronic conductivity) with an initial thickness of 200 μm and a resistivity of 0.02 Ohm×cm was chosen as the base region. The diffusion process was carried out simultaneously on several samples placed in a quartz cartridge («batch» method). A microrelief was created by means of grinding on the surface of the initial crystals with a given resistivity to improve adhesion with the diffusant. The first diffusant, «КБК-45» (containing 45% of boric acid), which forms a p−n junction with the initial crystal, is applied to the surface of the crystal twice, while the second diffusant, «КФК-54» (containing 54% of phosphoric acid) is applied as a single layer. In order to provide infinite source conditions, the n⁺- and p⁺-type gaskets matted with corundum, 800 μm in diameter and 1 mm in thickness, are placed between the initial crystals. The initial crystals are placed inside the cartridges in such a way as to enclose gaskets between the homogeneous sides, as it is shown in Figure 1.
Figure 1. Layout of components for diffusion process: 1 – quartz cartridge, 2 – base crystals, 3 – gaskets, 4 – p⁺-type diffusant, 5 – n⁺-type diffusant.

The diffusion process itself is carried out in a furnace chamber. The temperature profile of the diffusion process comprises the heating of the system from 650 ºC up to 1250 ºC in a nitrogen atmosphere, holding for 48 hours and then cooling to 650 ºC in a dry oxygen environment. The use of the «batch» diffusion method in incorporation of boron and phosphorus impurities into silicon made it possible to reduce the surface resistance of the p⁺-layer to 1.1–1.2 Ohm/square and that of the n⁺-layer to 0.3–0.4 Ohm/square, in contrast to the values achieved for diffusion out of the gas phase, which are 2.2 – 1.8 Ohm/square. Specific to the proposed method, in the area with a depth of up to 25 μm the resistivity close in value to the surface resistivity is obtained, which is then rather sharply increases by 3–4 orders of magnitude, creating an abrupt p–n junction.

The distribution of the impurity over the thickness of the base region, as well as the occurrence depth of p–n junction were determined by analyzing the structure of the transverse section of the crystal using scanning electron microscope (SEM).

The calculated value of the diffusion coefficient was equal to $7.47 \times 10^{-12}$ cm$^2$/s. The depth of boron diffusion into silicon increases in a sublinear manner depending on the diffusion time and at 48-hour point reaches the values of 50–70 μm. A similar dependence also takes place in the diffusion process of phosphorus. Thus, we can assume that the thickness of the diffusion regions on one side, p⁺-type, is about 60 μm in depth, while the thickness of those on another side, n⁺-type, is 70 μm.

Taking into account the low rate of thermal diffusion and electrodiffusion, as well as low penetrating ability into silicon, the following systems of metals were chosen as the contact material for the p⁺–n–n⁺ structures obtained: V – Ag, Ti – Ni – Au, in which case Ag and Au provide reliability of soldering process. Contact materials were deposited sequentially with thickness in the range of 0.1–0.65 μm. Then, Ag layers with a thickness of 5 μm were galvanically deposited on their surfaces, the p⁺–n–n⁺ structures have a hexagonal crystal shape (3.4 mm 3.0 mm) with an area of 0.0742 cm$^2$.

Afterwards, the thermal expansion joints were formed on both surfaces of the crystals by means of fusing with a silver solder alloy, 2–3 μm in thickness. Thermal expansion joints are made of a 380 μm thick copper disc with a diameter of 0.33 cm, on both surfaces of which layers Ni, 6 μm in thickness, are applied.

The structures prepared this way were installed in plastic shells with metal leads (Figure 2), soldered using the soft solder of «ITCp-2.5» grade with a melting point of 295–300 ºC. On the basis of technology described above, samples of voltage limiters with different resistivity of the base area and breakdown voltages ranging from 12 to 340 V were manufactured.
Figure 2. The structures assembled in a plastic shell.

3. Experimental
Investigations of the capacity-voltage and current dependences, as well as the study of the dependence of the maximum pulse power on the pulse duration, were carried out on the structures obtained.

As shown in Figure 3, the obtained dependence of the barrier capacity of the p⁺–n–n⁺ structure on the blocking voltage is in accordance to the power law $1/C^2 = V$.

Figure 3. Dependence of barrier capacity on blocking voltage.

The thickness of the space charge layer of the p⁺–n junction is derived based on data of the barrier capacity values in the specified voltage range:

$$W_{p-n} = \frac{\varepsilon_0 S}{C_V}$$  \hspace{1cm} (1)

which provides us with a value of 0.09914 μm at zero offset and 0.27 μm at a voltage of 14 V. The concentration of charge carriers at the boundaries of the depleted layer, valid for any distribution of charge density at small increments of the offset voltage, can be determined from the equation [5]:

$$N_n(W_{p-n}) = -\left(\frac{2}{q\varepsilon_0 S^2}\right)\left(\frac{1}{d(C^{-2})/dV}\right)$$  \hspace{1cm} (2)

which provides us with a value of $1.3 \times 10^{15} - 1.2 \times 10^{16}$ cm$^{-3}$ (Figure 4).
4. Discussion of the results

The current–voltage characteristics of the p$^+$–n–n$^+$ structures, obtained using the measuring bench by setting the reverse current and voltage fixation, allowed us to prevent the transition to the mode with a steep rise in the reverse current. Investigations of the current-voltage characteristics showed that their breakdown voltages increase within the temperature range of −60 ± 2 °C to 125 ± 2 °C (Figure 6), which is typical of avalanche breakdown [5]. Concurrently, the electric field intensity in case of the observed breakdown voltage of 23 V equals 8.5×10⁵ V/cm.
Figure 6. Dependence of the reverse current on the voltage of the silicon p$^+$–n–n$^+$-structure at different temperatures, C: 1 — 125 ± 2, 2 — 25 ± 2, 3 — -60 ± 2.

In the avalanche breakdown mode, the newly generated avalanche shock front passing through the diode leaves a populated plasma with a weak electric field. In this case, the current flowing through the diode is increased significantly due to the additional multiplication of carriers in the base, while the produced plasma reduces the voltage on the diode to near-zero values. Furthermore, the holes situated in the base region drift to the p$^+$ region, whereas the electrons drift to the n$^+$ region at a speed significantly lower than the drift saturation velocity. The plasma gradually dissolves keeping the current unchanged and the process repeats. The process of carrier multiplication is characterized by a high value of the diode field intensity and precedes the new formation of the avalanche shock front, which possesses the longest duration [6]. In this mode, the longer the pulse duration is, the higher the temperature will be and the less withstanding power will be.

The behavior of the withstanding power dependence on the pulse duration is characterized by equal decrease as the pulse duration increases in case of voltage limiters of 0.5 kW and 1.5 kW values (Figure 7). In particular, as the pulse duration increases, the switch-on time will increase, as well, leading to a rise in the temperature of the limiter.

Figure 7. Dependence of the maximum pulse power on the pulse duration for the voltage limiters of the following power: 1 — 1.5 kW, 2 — 0.5 kW.

Since the steepness of reverse current growth in the breakdown mode is rather sharp and the voltage increment is very small, the switch-on time value will be very small, as well (the frequency range value will be high, correspondingly).

When a sharply increasing reverse current pulse is applied to the limiting diode, a capacitive current will flow through it before reaching the breakdown voltage. In p–n junction structures, the main condition for the existence of an inductance is the presence of a voltage drop in the high-
resistivity region, as well as the injection of minority carriers into this region, which leads to an increase in its conductivity. The proportionality factor connecting the voltage and the rate of capacitive current change $\frac{dI}{dt}$ is the inductance. The magnitude of the current is proportional to the barrier capacitance and the rate of voltage change, which is also associated with the base series resistance. The electric field will increase across all cross-sections at rate

$$\frac{dE}{dt} = \frac{j(t)}{\varepsilon \varepsilon_0}$$

(3)

The field will proceed to build up as such until the electric field at some point reaches the maximum value of $E_m$. When the field exceeds this value, an avalanche shock front is generated, which passing through the diode leaves a populated plasma with a weak electric field. The current build-up occurs so fast that the process of carrier drift can be neglected. The cross section in which the field reaches the maximum value ($E > E_m$) moves rapidly in the direction of the n$^+$ region where the shock wave propagates (Figure 8).

Figure 8. Shock wave propagation in the region of the p–n junction.

The slope of the field to the right of the $X_0$ section is determined by the equation

$$\frac{dE}{dt} = \frac{a}{\varepsilon \varepsilon_0} N_b$$

(4)

where $N_b$ is the impurity concentration in the depletion region. The velocity of shock wave propagation can be calculated if we divide equation (3) by (4), which results in the following

$$V_{sw} = \frac{dx}{dt} = \frac{j(t)}{aN_b} N_b$$

(5)

The maximum carrier velocity is $v_s \ll v_{sw}$, but even assuming that $v_s < v_{sw}$ the generated plasma will not have enough time to dissipate and the shock wave will be developed as a result.

The ratios obtained allow one to calculate the total switch-on time of the limiting diode $t_{sw}$. It comprises the sum of the time required to charge the barrier capacitance of the p–n junction $t_{RC}$ within the voltage range of $V_m$ to $V_b$ with the initial current $I = jS$, where $S$ is the area of the p–n junction,

$$t_{RC} = \frac{C_b(V_b-V_m)}{I} - \frac{y\varepsilon \varepsilon_0 S E_m W}{2jS} = y\varepsilon E_m$$

(6)

$C_b$ – the p–n junction capacitance, $C_b = 0.01$, and the shock wave propagation time

$$t_{sw} = \frac{W}{2V_{sw}} = \frac{aWN_b}{2j}$$

(7)
It is necessary to add the energy relaxation time $t_e \approx 10^{-12}$ s to these components, i.e. the time required for the energy to transfer from carriers to the lattice.

Accordingly, the total switch-on time of the limiting diode will be determined by the following equation

$$ t_{on} = Y \frac{\varepsilon_0 E_m}{j} + \frac{qW N_b}{2j} + t_e $$  

(8)

As can be deduced from this equation, after the shock wave occurs the diode dynamics is largely defined by the switching circuit, which determines the current density $j$. The diode is turned off shortly after the impact of the current pulse. The time period is determined by the resorption time of the plasma arising in the depletion region.

The distinctive feature of the diodes under study is that the current increases with a low limiting coefficient (1.13 as opposed to 1.18), in comparison with the conventional alternatives [7], while the current density is very high, predisposing the voltage limiter to low switch-on values in accordance with equation (8). In case of the experimental data $\gamma = 0.01$, $E = 8.5 \times 10^5$ V/cm, $Wp-n = 0.27$ μm and current density (100 mA/0.0742 cm$^2$) = 1.35 $10^{-3}$ A/cm$^2$ the switch-on time $t_{on}$, equals 13 μs, according to (8).

5. Conclusions
1. It has been experimentally demonstrated that the presented technological and design solutions allows one to obtain semiconductor structures that, acting as voltage limiters, possess an increased resistance to impulse loads and a shorter operating switch-on time. The data on the withstanding impulse power obtained over the course of the experiment showed that the nominal power decreases according to the same law with an increase in the pulse duration, which indicates that the parameters of the designed structures remain the same in the limiter obtained.

2. The relationship between transition times (switch-on and switch-off) and the characteristic parameters of the voltage limiter structure is presented. The possibility that some part of power might dissipate at the resonating frequency acts as an additional stimulus for increasing the withstanding power values.

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