Switch-back based on charge equalization switching technique for SAR ADC

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Abstract: A switch-back based on charge equalization switching technique for successive-approximation-register (SAR) analog-to-digital converters (ADCs) is proposed. With the proposed switching technique the average switching energy is reduced by 96.86% as compared with the conventional method. This switching scheme can also reduce the total capacitance about 75% with the comparison of the conventional architecture. With the proposed switching scheme the common mode voltage shifts only by 1LSB during all conversion steps, so the dynamic offset of comparator becomes negligible in this case.

Keywords: analog-to-digital converter, charge equalization, common mode voltage, switch-back, successive-approximation-register

Classification: Integrated circuits

References

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1 Introduction

In SAR ADCs the dominant sources of power dissipation are capacitive DAC arrays, the comparator and digital logic. The power reduction of comparator and digital logic circuits can benefit from CMOS technology scaled down. Thus, it can be reduced significantly in advanced technology under lower supply voltage. However, the switching power of capacitive array is independent of technology. Unlike conventional switching method [1] recently several switching techniques such as set-and-down [2], MCS [3], tri-level [4] are proposed to reduce the average
switching energy. These techniques show great power efficiency but with drawbacks of common mode voltage shift by $V_{\text{ref}}/2$ in [2, 4], extra reference voltage [3, 4], respectively. In this letter a novel switch-back based on charge equalization switching scheme is proposed. By splitting MSB capacitors to two equal parts charge equalization is used to perform a reference voltage of $V_{\text{ref}}/2$, thus, the extra reference voltage $V_{\text{ref}}/2$ used in [4] can be saved. Also, together with top-plate sampling the $V_{\text{ref}}/2$ is reused in the last conversion step, so the total capacitance can be reduced by 75% as compared to conventional architecture. For an N-bit SAR ADC the common mode voltage shift only by $V_{\text{ref}}/2^N$ during all conversion steps with the proposed switching scheme, while it shifts by $V_{\text{ref}}/2$ with set-and-down and tri-level switching schemes.

2 Switch-back based on charge equalization switching scheme

To explain the proposed switching scheme a 4-bit differential capacitive DAC switching procedure is shown in Fig. 1 and Fig. 2. The procedure of the first 2 bits conversion is shown in Fig. 1, and the procedure of the next 2 bits conversion is shown in Fig. 2. In Fig. 1 the MSB capacitor $2C$ is split to two equal parts $(C + C)$ with different bottom-plate reset level as $V_{\text{ref}}$ and GND. The LSB capacitor $C$ and the dummy capacitor $C$ are also set with different bottom-plate reset level as $V_{\text{ref}}$ and GND.

When sampling finishes the comparator compares the differential input ($V_{\text{inp}}$ and $V_{\text{inn}}$) immediately without any switching. For simplicity only the condition of $V_{\text{inp}} > V_{\text{inn}}$ is discussed in details. If $V_{\text{inp}} > V_{\text{inn}}$, the bottom plates of all capacitors connected to $V_{\text{ref}}$ in DACP and GND in DACN are switched together with charge equalization. In this condition a $-V_{\text{ref}}/4$ shift on top plate of DACP is generated and a $V_{\text{ref}}/4$ shift on top plate of DACN is also generated at the same time. So $V_{\text{inp}} - V_{\text{inn}} - V_{\text{ref}}/2$ is performed by this switching procedure.

![Fig. 1. Proposed switching scheme for 4-bit example (first 2-bits)](image-url)
In Fig. 2, if $V_{\text{inp}} - V_{\text{inn}} > V_{\text{ref}}/2$ the capacitor connected together of MSB in DACP is switched back to GND, and in DACN which is switched back to $V_{\text{ref}}$. In this case, a $-V_{\text{ref}}/8$ shift on top plate of DACP is generated and a $V_{\text{ref}}/8$ shift on top plate of DACN is also generated, so $V_{\text{inp}} - V_{\text{inn}} - 3V_{\text{ref}}/4$ is performed. The node M is set to $V_{\text{ref}}/2$ through charge equalization in previous conversion step as shown in Fig. 2. The reference voltage of $V_{\text{ref}}/2$ is generated internally and it can be reused for an additional bit. If $V_{\text{inp}} - V_{\text{inn}} > 3V_{\text{ref}}/4$, the bottom plate of the
dummy capacitor in DACP is switched back to GND while the bottom plate of the dummy capacitor in DACN is still maintained at $V_{\text{ref}}/2$, so $V_{\text{inp}} - V_{\text{inn}} - 7V_{\text{ref}}/8$ is performed. Only in the last conversion step, the common-mode voltage has a 1LSB shift.

3 Switching energy analysis

The behaviour simulation of a differential 10-bit SAR ADC with comparison of other switching schemes is performed and analyzed. The total average switching energy is:

$$E_{\text{avg}} = \left( \sum_{i=1}^{n-2} 2^{n-3-2i} + 2^{-n} \right) \times CV^2_{\text{ref}}$$  \hspace{1cm} (1)

Fig. 3 shows the behaviour simulation results of average switching energy for different switching schemes. The switching energy at each output code for several switching schemes is plotted in it. The proposed switching scheme achieves 96.86% average switching energy ($E_{\text{avg}} = 42.7CV^2_{\text{ref}}$) saving compared with conventional scheme ($E_{\text{avg}} = 1365CV^2_{\text{ref}}$). While the split scheme[1] achieves 37.4% ($E_{\text{avg}} = 852.3CV^2_{\text{ref}}$), the set-and-down scheme[2] achieves 81% ($E_{\text{avg}} = 255CV^2_{\text{ref}}$), the MCS scheme[3] achieves 93.4% ($E_{\text{avg}} = 84.7CV^2_{\text{ref}}$) and tri-level scheme[4] achieves 96.9% ($E_{\text{avg}} = 42.4CV^2_{\text{ref}}$). As the average switching energy of the proposed switching scheme approximately equals to the tri-level scheme, so the average switching energy curve of tri-level scheme is not plotted in Fig. 2.

Table I is a comparison of the average switching energy savings and capacitor array area reduction of different switching schemes. The proposed switching scheme consumes only $42.7CV^2_{\text{ref}}$ and achieves 96.86% energy saving as well as 75% area reduction with respect to the conventional switching method.

Fig. 3. Switching energy versus output codes comparison
Table I. Comparison of average switching energy, energy saving and area reduction for different switching schemes of a 10-bit SAR ADC

| Switching Scheme | Switching Energy | Energy Saving | Area Reduction |
|------------------|------------------|---------------|----------------|
| Conventional     | $1365.3CV^2_{ref}$ | reference     | reference       |
| Set-and-down     | $255.5CV^2_{ref}$ | 81%           | 50%             |
| MCS              | $170.1CV^2_{ref}$ | 93.4%         | 50%             |
| Tri-level        | $42.4CV^2_{ref}$  | 96.9%         | 75%             |
| Proposed         | $42.7CV^2_{ref}$  | 96.86%        | 75%             |

Table II. Comparison of common mode shift and whether extra reference voltage needed for different switching schemes of a 10-bit SAR ADC

| Switching Scheme | Common Mode Shift | Extra Reference Voltage Used |
|------------------|-------------------|------------------------------|
| Conventional     | 0LSB              | Yes                          |
| Set-and-down     | 256LSB            | No                           |
| MCS              | 0LSB              | Yes                          |
| Tri-level        | 256LSB            | Yes                          |
| Proposed         | 1LSB              | No                           |

Table II is a comparison of the common mode voltage shift and whether needs an extra reference voltage for these switching schemes. The tri-level switching scheme shows great energy efficiency at the expense of common mode voltage shifts by $V_{ref}/2$ and requires an extra reference voltage $V_{cm}$. With the proposed switching scheme, the common mode voltage shifts only by 1LSB and does not require any extra reference voltage.

4 Summary

A switch-back based on charge equalization switching technique for SAR ADC is proposed. The average switching energy is reduced by 96.86% compared with conventional switching scheme. Thus, both power and area efficiency can be achieved simultaneously. Additionally, it does not require any extra reference voltage and the common-mode shifts only by 1LSB during all conversion steps.

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