Ancilla-Quantum Cost Trade-off during Reversible Logic Synthesis using Exclusive Sum-of-Products

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Abstract—Emerging technologies with asymptotic zero power dissipation, such as quantum computing, require the logical operations to be done in a reversible manner. In recent years, the problem of synthesizing Boolean functions in the reversible logic domain has gained significant research attention. The efficiency of the synthesis methods is measured in terms of quantum cost, gate cost, garbage lines, logic depth and speed of synthesis. In this paper, we present a modification of the existing approaches based on Exclusive Sum-of-Products (ESOP), which allows to explore the trade-off between quantum cost and garbage lines. The proposed technique adds a new dimension to the reversible logic synthesis solutions. We demonstrate by detailed experiments that controlled improvement in quantum cost and gate count by increasing garbage count can be achieved. In some cases, improved quantum cost and gate count compared to state-of-the-art synthesis methods are reported. Furthermore, we propose a novel rule-based approach to achieve ancilla-free reversible logic synthesis starting from an ESOP formulation.

I. INTRODUCTION

Charles Bennett, in 1973, showed that reversible computation at logical plane can be done in a reversible manner to achieve theoretically zero power dissipation [2] in physical reversible computing. Several target technologies in nanoscale computing as well as technologies beyond CMOS, in particular Quantum computing, relies on reversible logic. Recent studies show that reversible logic synthesis can be applied to other directions [33] as well. Synthesis of a given Boolean function for reversible logic is, therefore, an important open problem. Before further discussion, we present some background on reversible logic.

A. Preliminaries

An n-variable Boolean function \( f \) is a mapping \( f : \{0,1\}^n \rightarrow \{0,1\} \), which can also be represented by a truth table. Alternatively, an \( n \)-variable Boolean function \( f(x_1, \ldots, x_n) \) can be considered to be a multivariate polynomial over \( GF(2) \). This polynomial can be expressed as a sum-of-products representation of all distinct \( k \)-th order products \( (0 \leq k \leq n) \) of the variables. This representation of \( f \) is called the algebraic normal form (ANF) of \( f \). The number of variables in the highest order product term with nonzero coefficient is called the algebraic degree, or simply the degree of \( f \) and denoted by \( \text{deg}(f) \). The ANF representation is also known as Positive-Polarity Reed-Muller expression (PPRM). This is a canonical form of a more general Exclusive Sum-Of-Product (ESOP) realization.

An \( n \)-variable Boolean function is reversible if all its output patterns map uniquely to an input pattern and vice-versa. It can be expressed as an \( n \)-input, \( n \)-output function or alternatively, as a permutation function over the truth value set \( \{0,1, \ldots, 2^{n-1}\} \). The problem of reversible logic synthesis is to map such a reversible Boolean function on a reversible logic gate library.

The gates are characterized by their implementation cost in quantum technologies, which is dubbed as Quantum Cost (QC) [21], [23], [1]. Few prominent classical reversible logic gates are presented below.

- NOT gate: \( f(A) = \bar{A} \),

- CNOT gate: \( f(A, B) = (A, A \oplus B) \),

- CCNOT gate: Also known as Toffoli gate. \( f(A, B, C) = (A, B, AB \oplus C) \). This gate can be generalized with Tof \( n \) gate, where first \( n-1 \) variables are used as control lines. NOT and CNOT gates are denoted as Tof \( 1 \) and Tof \( 2 \) respectively.

- Peres gate: A sequence of Tof \( 3 \)\((A, B, C)\), Tof \( 2 \)\((A, B)\) or its inverse is known as Peres gate.

- Controlled Swap gate: Also known as Fredkin gate. \( f(A, B, C) = (A, \overline{A} \cdot B + A \cdot C, \overline{A} \cdot C + A \cdot B) \). This gate can be generalized with Fred \( n \) gate \( (n > 1) \), where first \( n-2 \) variables are used as control lines.

Multiple sets of reversible gates form an universal gate library for realizing classical Boolean functions such as, (i) NCT: NOT, CNOT, Toffoli, (ii) NCTSF: NOT, CNOT, Toffoli, SWAP, Fredkin. (iii) GT: Tof \( n \). (iv) GTGF: Tof \( n \) and Fred \( n \).

Following the QC assumption of [11], we use a QC of 1 for all 2-qubit elementary reversible logic gates. Optimized implementation of larger gates are assumed for the corresponding QC computation, following [23] and [31]. The used QC values of a generalized Toffoli gate \( (\text{Tof}_{n+1}) \) is \( 2n^2 - 2n + 1 \), of a generalized Fredkin gate \( (\text{Fred}_{n+1}) \) is \( 2n^2 - 2n + 3 \), of a generalized Peres gate \( (\text{Per}_{n}) \) is \( n^2 \).

Reversible logic synthesis begins from a given \( n \)-variable Boolean function, which can be irreversible. The first step is to convert it to a reversible Boolean function by adding distinguishing input bits initialized with a constant value. If these constant values are recovered after the reversible circuit
execution, then these are known as *ancilla* and otherwise, as *garbage*.

II. RELATED WORK AND MOTIVATION

Reversible logic synthesis methods can be broadly classified in four categories as following. A different and more detailed classification is presented in a recent survey of reversible logic synthesis methods [26].

**Exact and Optimal methods:** In these methods, for small-scale reversible circuits the optimal implementation is found by making a step-by-step exhaustive enumeration or by formulating the reversible logic synthesis as a SAT problem [10] or reachability problem [12]. Optimal implementation up to 4-variable Boolean functions are known via exhaustive methods [28], [9] and up to few 6-variable Boolean functions are known via SAT-based synthesis approach [10]. Exact methods perform well for small-scale circuits only since, reversible logic synthesis is shown to be an NP-hard problem [4].

**Transformation-based methods** [17], [3]: These methods apply controlled transformations to map output Boolean functions to input Boolean functions. The method outlined in [3] utilizes Boolean functions’ nonlinearity measure and propose a column-wise synthesis approach, while [17] proceed row-wise in the boolean truth-table.

**Methods based on decision diagrams** [32], [18], [14]: In these methods, each node of the decision diagram is converted to an equivalent reversible circuit structure. These methods reported excellent scaling for large Boolean functions, low QC at the cost of high number of garbage bits. A matrix-based representation is used to construct Quantum Multiple-valued Decision Diagram (QMDD) for reversible Boolean functions [20]. This realizes ancilla-free reversible circuit and achieved QC comparable to transformation-based methods [30].

**ESOP-based methods:** The advantage of ESOP formulation has been studied for classical logic synthesis, leading to state-of-the-art synthesis tools for obtaining an ESOP formulation with low number of cubes and literals [22], [13]. For reversible logic synthesis, the ESOP formulation maps directly to the basic reversible logic gates. This synthesis method led to two different approaches so far. The first one, begins from a PPRM formulation, and heuristically searches for common kernels at each logic depth [11]. In the other ESOP-based synthesis methods, each cube in the ESOP is converted into an equivalent Toffoli gate and all the cubes are xor-ed in the dedicated output line, leading to a fixed garbage count. An example of straightforward application of this method is shown in the Figure 1, where the reversible circuit for Grover’s oracle (4 mod 5) is synthesized. The corresponding ANF is $1 \oplus x_1 \oplus x_2 \oplus x_1 x_2 \oplus x_3 \oplus x_2 x_3 \oplus x_4 \oplus x_1 x_4 \oplus x_3 x_4$.

Realizing that the QC and gate count can be further reduced by sharing the common cubes, a shared-cube synthesis algorithm is proposed in [8], [24]. Another method, proposed in [25], identified two transformations to reduce the garbage and gate count. An evolutionary algorithm to generate reversible circuit using ESOP formulation is proposed in [7].

**Motivation:** Despite significant research in the reversible logic synthesis methods, the major focus has been so far towards synthesis with optimal garbage lines. While this is justified due to the difficulty of realizing a qubit in current quantum technologies, this also offers a restricted view of the synthesis performance. As it is shown in the methods based on the decision diagram [32], [18], [30], it is possible to achieve significantly less gate cost and QC than other state-of-the-art garbage-free synthesis method. Fundamentally, this reflects a trade-off, which is explored in this paper. The trade-off between ancilla and QC is presented in a recent paper [19]. We propose similar approach, for ESOP-based reversible logic synthesis. We show that, complementing the approach outlined in [19], the trade-off can be performed early in the logic synthesis flow. Several ESOP-based synthesis techniques [35], [24], [25] focussed on reducing QC and gate count by common cube sharing and a set of transformations. In this paper, we attempt to generalize this and explore the link between ESOP minimization and reversible circuit synthesis performance.

A natural question at this point is whether it is possible to achieve ancilla-free reversible logic synthesis starting from an ESOP formulation, which represents one extreme point of the ancilla-cost trade-off. We propose a rule-based approach to achieve the same.

In short, our contributions are twofold.

- First, we show that diverse trade-off points between ancilla count and QC/Gate cost is achievable. We propose a tool-flow to perform the trade-off systematically.
- Second, we propose a rule-based, ancilla-free reversible logic synthesis technique starting from an ESOP formulation.

The rest of this paper is organized as following. In the Section III the overall synthesis flow is outlined. The ancilla-free ESOP-based reversible logic synthesis is detailed in the Section IV. The results are presented in the Section V. The paper is concluded with future directions in the Section VI.

**III. ESOP-BASED SYNTHESIS FLOW**

The proposed ESOP-based synthesis flow starts from a canonical ANF representation. This is not an optimized ESOP representation like the one [22] adopted in other ESOP-based synthesis flows [11], [8]. However, the rationale of selecting this representation is that it offers an insight into the effect of the ESOP optimizations onto the quality of synthesis results. This is previously studied, in an evolutionary algorithm [7].
A. ANF Construction

Constructing an ANF from a Boolean truth table specification can be done using $O(n2^n)$ operations with standard algorithm. The input to the algorithm is the truth table $f = [f(0), f(1), f(2) ... f(2^n - 1)]$, and the output is the coefficient vector of the ANF, represented as $C = [c_0, c_1, c_2, ... c_{2^n - 1}]$. For an $n$-variable Boolean function, $C = fA_n$, where $A_n$ can be computed as following.

$$A_n = \begin{bmatrix} A_{n-1} & A_{n-1} \\ 0 & A_{n-1} \end{bmatrix}, \text{where } A_0 = 1.$$

Subsequently, the ANF is converted into an $n$-ary, directed acyclic graph (DAG) $G(V, E)$ for the optimization and mapping to reversible circuit. Note that, the ANF is considered as a starting point for the subsequent ESOP-based optimizations. Alternatively, this could be done with an ESOP-based form as available in [22]. However, we started from a canonical representation to have better control at the optimizations of our choice. The DAG, that is generated from the ANF, is not the final circuit but, an intermediate representation for optimization and mapping. Here, $G(V, E)$ is defined as a set of nodes $V$ and a set of edges $E$, where $e_{i,j}$ indicates an edge between $v_i$ and $v_j$. The nodes can be of these types - constant, identifier, root, and and and xor. An exemplary DAG for one output of $nth_{\text{prime}}_3_{\text{inc}}$ circuit is shown in the following Figure 2. The root node is for combining all the different output functions of the reversible circuit. For every node, the depth is appended as a suffix. The reversible Boolean specification of $nth_{\text{prime}}_3_{\text{inc}}$ in permutation form is $\{0, 2, 3, 5, 7, 1, 4, 6\}$ [23].

![Graph-based Representation of $nth_{\text{prime}}_3_{\text{inc}}$](image)

B. Optimization Engines

In order to reduce the QC, gate cost and garbage count from the default implementation flow outlined in the previous section, several optimization engines are plugged in. These are described in the following subsections.

**Kernel Extraction**: Kernel extraction from a polynomial expression is a well-studied problem in classical logic synthesis [6]. We start from an existing recursive kernel extraction algorithm (algorithm 3.4, [6]). The algorithm returns all possible kernels, $K(f)$ for a given function $f$. From those candidate kernels, the kernel with minimum remainder term ($k_t$) is chosen and termed as the divisor. After this initial kernel computation, this same process is repeated for the divisor, quotient and the remainder. Additionally, an user-defined threshold parameter is chosen to control the size of the selected Kernel. This ensures that the generated and-xor graph is not skewed in nature and there is a fair distribution of edges across multiple depths. If no suitable kernel is found, the dividend is retained as it is with 2-level and-xor graph formation.

**Algorithm 1: ExtractKernel**

Input: $K(f)$
Output: $k_t$

for all $k \in K(f)$ do
  if $rem(f,k)$ is minimum then
    if $k \rightarrow size() > threshold$ then
      return $k$;
  end
end
return NULL;

**Common Cube Sharing**: As identified in several ESOP-based synthesis methods, sharing common cubes improves the synthesis quality significantly. With the graph-based representation, it is convenient to perform the cube sharing optimization. Shareability of a pair of nodes is determined by the number of common children amongst them. If for either of the nodes, all the children are part of another node, then it is considered shareable. Otherwise, if the number of common children is more than half of the total children count of the two nodes, then the nodes are declared shareable. The nodes are shared across multiple depths of the and-xor graph, which again can be controlled as an input parameter.

**Algorithm 2: CommonCubeSharing**

for $depth = depth_{\text{max}} - 1 \rightarrow 1$ do
  $depth_j = depth$;
  for all node$_i \in G(depth)$, node$_j \in G(depth_j)$ do
    if shareable(node$_i$, node$_j$) then
      share(node$_i$, node$_j$);
      break;
    end
  end
  $depth_j = depth_j - 1$;
end

**Parent Reduction Optimization**: A key observation from existing minimum garbage synthesis solutions [17] is that the final Toffoli network, when presented in the and-xor graph form (see Figure 2) allows for a perfect execution of the mapping algorithm to be presented later (Algorithm 3). This formed the motivation of the parent reduction optimization. In this optimization, before every iteration of target node determination, the leaf node with minimum parents is identified as
a candidate node. The number of parents for that particular
node is minimized by applying the following expansion rules.

\[ a = (a \oplus b) \oplus b \]  
\[ a.b = ((a \oplus b)b) \oplus b \]

For both the rules, direct parents of node \( a \) are avoided by
adding an edge from the \( a \oplus b \) node. This is beneficial only if
there is an already and existing \( a \oplus b \) parent node. This reduces
the parent count of node \( a \) at the cost of increased parent
count of node \( b \). This optimization is applied until no further
reduction of node \( a \) parent count is possible. Clearly, several
more complex expansion rules can be formulated as well as
a complex heuristic for determination of the target leaf node.
However, that leads to a long runtime and therefore omitted.
In principle, there exists one or more set of transformation
rules to convert any given ESOP formulation to the ESOP
representation realized by minimum garbage reversible logic
synthesis methods \(^{[17]}\). For example, the following expansion
rule is a more general form of the rule \(^{[2]}\) where \( x = 0 \).

\[ a(b \oplus x) \oplus x = a(a \oplus b \oplus x) \oplus (a \oplus x) \]  

Note that, these optimizations can be applied to any ESOP-
based flow \(^{[24, 7, 8, 11]}\). While, existing ESOP-based
optimization approaches focus on reducing gate count or QC,
we attempt to reduce line count here and in particular, to
identify the trade-off between line count and QC.

C. Mapping to Generalized Toffoli Network

Starting from the aforementioned graph representation, the
mapping to Generalized Toffoli (GT) network is done by
repeated determination of a target node (\( t_{\text{node}} \)) and then
mapping it to the corresponding reversible circuit representa-
tion. Naturally, the target node determination forms the core
algorithmic part, which is done heuristically as shown in the
following Algorithm \(^{[5]}\).

The heuristic works in a greedy manner to minimize the
garbage count. It traverses all the nodes in \( \text{depth} \) above the
leaf nodes. Whenever there is an available \( \text{xor} \) node with a
leaf node (\( \text{leaf_single} \)) connected only to the \( \text{xor} \) node, the
\( \text{xor} \) node is selected. All the other children of that node can
perform the \( \text{xor} \) operation and use the node \( \text{leaf_single} \) as
target. If no such node is found, it proceeds towards all the
\( \text{and} \) nodes and looks for its parents, if it contains a similar \( \text{xor} \)
parent in \( \text{depth}_{\text{max}} - 2 \) with single-parent leaf node. If no such
node is found, the algorithm returns a node with maximum
leaf node children. In case of a tie, the node with minimum
parent is chosen. This leads to the creation of a garbage line.
However, it creates the possibility to find single-parent in the
next iteration. The callee mapping algorithm maps one node
in one iteration, which is demonstrated the Figure \(^{[3]}\) In the
Figure \(^{[3]}\) for every identified target node, the corresponding
Toffoli circuit is shown in the middle and the modified graph
is shown in the rightmost columns. Three different kinds of target
identification, as presented in the Algorithm \(^{[3]}\) are shown. It
is straightforward to show that the algorithm \(^{[3]}\) always returns
a valid node for mapping to the equivalent Toffoli circuit,
ensuring that the mapping algorithm always terminates with a
valid circuit synthesis.

### Algorithm 3: FindTarget

**Input:** \( G(V, E) \)

**Output:** \( t_{\text{node}} \)

forall \( node \in G(\text{depth}_{\text{max}} - 1) \) do
  if \( node \to \text{getType}() = t_{\text{xor}} \) and
    \( node \to \text{containSingleChild}() \) then
    return \( node \);
  end
  if \( node \to \text{getType}() = t_{\text{and}} \) and
    \( node \to \text{Parent}() \to \text{containSingleChild}() \) and
    \( node \to \text{Parent}() \to \text{getType}() = t_{\text{xor}} \) then
    return \( node \to \text{Parent}() \);
  end
end

return \( \text{nodeWithMaxChildMinParent}() \);

### Fig. 3. Mapping of ESOP to Generalized Toffoli Circuit

IV. A\textsc{ncilla-free, ESOP-based Reversible Logic Synthesis}

The proposed ancilla-free reversible logic synthesis algo-

rithm treats the problem in a step-wise fashion starting from
the output ESOP expressions. Each step applies a reversible
transformation in order to reach a step, when all the functions
are linear. From linear functions, the reversible circuit can be
easily constructed. For example, the possible set of reversible
transformations in a 3-variable circuit consists of all possible
\( T_{of2} \) and \( T_{of3} \) gates. We refer the application of these gates
as transformation of types \( T2 \) and \( T3 \) respectively. All possible
transformations are available as rules, one of which is chosen
at each step by following a heuristic process.

A transformation is adjudged suitable if it reduces the
number of non-linear terms in the expression or reduces the
number of literals in an already linear expression. Initially the
non-linear terms are reduced using transformation of type \( T2 \).
If it is no longer possible to apply \( T2 \) or two consecutive
transformation are same, then transformation of type $T3$ are examined and a suitable transformation is chosen following a heuristic procedure. After all the output expressions have reduced to linear expressions, only $T2$ type transformation are applied which trivially reduce the expressions to single literal form. The key steps in the algorithm are checking the suitability of applying a specific transition with control and target variables, for which we developed heuristic techniques. These steps are explained in the following.

**Suitability check of transformation type $T2$:** The algorithm checks for the occurrence of two non-linear terms in a single expression and then applies the $T2$ transformation with the control from the common variable and the target on one of the unique variables. The target is assigned arbitrarily. For example if $ab + bc$ is detected in an expression, the unique variables are $a$ and $c$. Either of these are arbitrarily chosen as the target variable with a $T2$ transformation.

**Suitability check of transformation type $T3$:** When $T2$ type transitions fail to further simplify the ESOP expressions, a target is arbitrarily fixed and appropriate control variables are searched for in the expressions where the target occurs. If the application of $T3$ leads to a decrease in the number of non-linear terms in the expressions then it is adjudged as suitable.

**Terminating Condition:** After a cascade of changes the output expressions keep simplifying until the take the form of basic variables. This is when the algorithm terminates. It can be shown that either of these two previous transformations are always found to be suitable and the terminating condition is always achieved for 3-variable functions.

We explain the algorithm flow with the following example. The three output expressions for the benchmark circuit \(3 \_17 \text{[15]} \) are as following.

\[
\begin{align*}
    f_1 &= ac \oplus bc \oplus a \oplus c \oplus 1 \\
    f_2 &= a \oplus b \oplus c \oplus 1 \\
    f_3 &= ab \oplus bc \oplus b \oplus c \oplus 1
\end{align*}
\]

At the first stage, the presence of two nonlinear terms in \(f_1\) is found, where \(T2\) is suitable. The application of \(T2\) with \(b\) as control and \(a\) as target line means that one needs to replace \(a\) with \(a \oplus b\) in all the expressions. The according changes in the aforementioned equations are as following.

\[
\begin{align*}
    f_1 &= ac \oplus a \oplus b \oplus c \oplus 1 \\
    f_2 &= a \oplus c \oplus 1 \\
    f_3 &= ab \oplus bc \oplus c \oplus 1
\end{align*}
\]

In the next step, two nonlinear terms in \(f_3\) is found and again \(T2\) with \(c\) as control and \(a\) as target line. By repeating these steps, one reaches the terminating condition.

The algorithm is presented in form of pseudo-code in Algorithm 4. The algorithm is run over the complete set of 3-variable functions, of which the results are presented in the following section. For scaling the algorithm to more than 3 variables, further heuristics with \(Tof_{a}\) gates are applied. There, the goal is to first reduce the ESOP functions to consist of 2-literal cubes only. Then onwards the above algorithm can be applied again. This gives rise to the possibility of reducing an \(n\)-variable reversible logic synthesis to \(n-1\)-variable form recursively. It must be noted that, \(n\)-literal cubes cannot be present for a \(n\)-variable reversible Boolean function to maintain balancedness property of the output functions.

**V. Results and Discussion**

The abovementioned algorithms are implemented using C++, with around 3000 lines of code. The code is compiled with GCC version 4.6.6 and it is executed on an AMD Phenom \(\text{TM} \text{II X6 1100T}\) Processor running Linux-based OS. In the following, we present a series of experiments to identify the advantage and disadvantage of the proposed methods vis-à-vis state-of-the-art reversible logic synthesis methods. The optimization kernels are controllable through command line parameters allowing various experiments. Though no specific optimization is turned on for increasing the count of Peres gates, those gates, when formed, are identified and accounted for in the QC and gate count computation. It must also be noted that final ordering of the output functions are chosen such as to minimize the QC \([\text{14]}\).

**A. QC-Ancilla Trade-off**

For this experiment, the user-controllable parameters in the tool include the choice to run parent reduction (P), common cube sharing (C) optimization, the choice of threshold for kernel extraction (K) and selection of the size of the Toffoli gate (T). The last one is controlled when creating the initial \(n\)-ary ESOP graph. If the value of C is set to true, the selection of T has less influence. To show the trade-offs, two Boolean functions with significant relevance in cryptography, namely the S-Boxes for AES (8-variable) and PRESENT (4-variable) block ciphers are chosen. For the different values of parameters, corresponding gate cost, garbage count and QC values are presented in the Table 1. The best results for these functions obtained from \([\text{29]}\) using BDD-based reversible logic synthesis is presented for comparison.

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**Algorithm 4: Ancilla-Free Reversible Logic Synthesis**

```plaintext
\begin{algorithm}
\begin{align*}
    f_{\text{curr}} &= f_{\text{end}}; \\
    \text{while } f_{\text{curr}} \neq f_{\text{in}} \text{ do} \\
    \quad \text{if } f_{\text{curr}} \text{ is nonlinear then} \\
    \quad \quad \text{found}_{-}T2 = \text{check}_{-}T2(f_{\text{curr}}, f_{\text{mod}}); \\
    \quad \quad \text{if } \text{found}_{-}T2 = \text{false OR } f_{\text{last}} = f_{\text{mod}} \text{ then} \\
    \quad \quad \quad \text{apply}_{-}T3(f_{\text{curr}}, f_{\text{mod}}); \\
    \quad \quad \text{else} \\
    \quad \quad \quad f_{\text{mod}} = \text{apply}_{-}T2(f_{\text{curr}}); \\
    \quad \quad \quad f_{\text{last}} = f_{\text{mod}}; \\
    \quad \quad \text{end} \\
    \quad \text{else} \\
    \quad \quad f_{\text{mod}} = \text{apply}_{-}T2(f_{\text{curr}}); \\
    \quad \text{end} \\
    \quad f_{\text{curr}} = f_{\text{mod}}; \\
    \text{end}
\end{align*}
\end{algorithm}
```
Table I shows that the backend for mapping to Toffoli network can reduce the minimum garbage limit set by existing ESOP-based synthesis flows [24]. For PRESENT S-Box, with maximum gate size being To[fo]l, garbage count is 3. With decreasing Toffoli size, QC decreases and gate count and garbage count increases, which is the effect of flattening. Enabling cube sharing reduces the gate count and garbage count to the original values and also significantly reduces the QC due to small-sized Toffoli gates. By enabling kernel extraction, QC can be further reduced at the expense of increased garbage count. Similar trend is found for the AES S-Box.

For rest of the experiments, the focus is set on improving QC. We try to experiment with the proposed methodology and check if the QC and gate count obtained by state-of-the-art synthesis methods can be reduced by compromising garbage count. To achieve that, common cube sharing is set to true, parent reduction optimization is set to false and size of garbage count. To achieve that, common cube sharing is set to true, parent reduction optimization is set to false and size of garbage count is obtained below the threshold value of 1 until the QC values starts degrading. Typically, the best QC and garbage count is obtained below the threshold value of 7.

B. Comparison with state-of-the-art ESOP-based Methods

It is important to study the benefits of the proposed trade-off capability of ESOP against existing ESOP-based methods reported in [24], [11], [25]. All of these methods begin with an optimized ESOP representation produced by [22]. In [24] several results for Boolean functions with large number of variables are reported. In [11] detailed results for small Boolean functions are presented. However, both of these works have a minimum garbage count (which is greater than 0). Reduced garbage count is reported in [25]. The benchmarks presented in these papers are synthesized with our approach and presented in the Table II. The improved or matching QC values are marked with gray background.

Compared to the method proposed in this paper, all existing methods has considerably less execution time due to the fast heuristic ESOP minimization of EXORCISM-4 [22]. However, as can be observed from the results in the Table II the solution is constrained by the output of EXORCISM-4, leading to poor results in some cases. This is expected, since none of the approaches [24], [11], [25] experimented with the ESOP optimization parameters except for fixed transformations and cube sharing. Furthermore, in some cases the QC as well as the gate count is improved in our approach (e.g. rd73, 5one245). This reflects the importance of combined ESOP optimization and Toffoli-network mapping.

C. Comparison with Decision Diagram-based Methods

While transformation-based methods represent the best results with minimum garbage for small functions, recent improvements in QMDD-based approach showed that the QC can be further lowered without increasing the garbage [30]. On the other hand, BDD-based synthesis achieve extremely small QC at the cost of increased garbage count. To do a fair benchmarking, our method is compared against the BDD-based method and QMDD-based method for the benchmarks reported in [30]. The results are presented in the Table III. In the same mode as the previous experiments, our goal is set to reduce QC compared to the reported results by increasing garbage count.

In the Table III instead of garbage count, the total lines are mentioned to synchronize with the results presented in [30]. The circuits for which QC is improved or matching compared to BDD-based flow are marked with gray scale. Compared to QMDD-based flow (as well as for [17]), the QC for all the circuits are improved. This is expected since the garbage count is compromised. It is interesting to note that, compared to BDD-based flow several circuits report improved performance in QC, gate count as well as garbage count for our ESOP-based method. This is possibly due to the difference in the Boolean structure optimization performed by BDD-based and ESOP-based method. The nature of Toffoli network mapping
TABLE III

| Function | I/O |
|----------|-----|
| adr4     | 8/5 |
| clip     | 9/5 |
| cm42a    | 4/10|
| cycle10_2| 12/12|
| dc1      | 4/7 |
| dc2      | 8/7 |
| dist     | 8/5 |
| max46    | 9/1 |
| misex    | 8/7 |
| plus127mod8192 | 13/13 |
| plus63mod4096 | 12/12 |
| radd     | 8/5 |
| rd73     | 7/3 |
| rd84     | 8/4 |
| root     | 8/5 |
| sao2     | 10/4|
| sqrt8    | 8/4 |
| squar5   | 5/8 |
| sqn      | 7/3 |
| wim      | 4/7 |
| z4       | 7/4 |

TABLE IV

| Function     | Optimal/Known Best Result | this work |
|--------------|---------------------------|----------|
|              | QC | Gates | Garbage | QC | Gates | Garbage |
| 2&5          | 75 | 17    | 5       | 39 | 16    | 9       |
| 3&7          | 12 | 6     | 0       | 19 | 11    | 4       |
| 4&9          | 28 | 14    | 0       | 78 | 34    | 10      |
| 4mod5        | 7   | 5     | 4       | 9  | 5     | 4       |
| 5mod5        | 76  | 10    | 5       | 36 | 16    | 8       |
| 6sym         | 62  | 20    | 9       | 71 | 20    | 12      |
| 9sym         | 94  | 28    | 11      | 488| 183   | 81      |
| cycle10_2    | 1198| 19    | 0       | 145| 30    | 25      |
| ham3         | 10  | 4     | 0       | 7  | 3     | 0       |
| ham7         | 49  | 25    | 0       | 76 | 32    | 11      |
| hb4b         | 19  | 13    | 0       | 64 | 24    | 8       |
| hw5b         | 80  | 38    | 0       | 229| 73    | 23      |
| hw6b         | 107 | 47    | 0       | 446| 172   | 58      |
| hwb7         | 2611| 331   | 0       | 991| 364   | 120     |
| hw8b         | 6940| 2710  | 0       | 1846| 686   | 234     |
| nth_prime_3_inc | 6 | 4  | 0 | 6 | 4 | 0 |
| nth_prime_4_inc | 26 | 14 | 0 | 70 | 26 | 8 |
| nth_prime_5_inc | 80 | 36 | 0 | 176| 68 | 22 |
| nth_prime_6_inc | 667 | 55 | 0 | 383| 139 | 44 |
| nth_prime_7_inc | 3172| 1427 | 0 | 950| 354 | 116 |
| nth_prime_8_inc | 7618| 3346 | 0 | 1741| 625 | 218 |
| rd32         | 8   | 4     | 2       | 8  | 2     | 2       |
| rd73         | 64  | 20    | 7       | 94 | 29    | 17      |
| rd84         | 98  | 28    | 11      | 208| 58    | 26      |
| xor5         | 4   | 4     | 4       | 4  | 4     | 4       |

leads to high garbage count for both BDD and the ESOP-based method proposed in this paper.

D. Comparison with Optimal and Known Best Results

It is interesting to verify the performance of the presented method against the known optimal results, in terms of gate-count and MCT library. The QC reductions considering Peres gates are also accounted for. The same library and QC model is also used in the performance assessment of our technique. We chose a set of benchmarks available in [28, 9, 23] and present the details in Table [IV] where the improved or matching QC values are marked with gray shade. The results show that for Boolean functions with large variable count, the QC and gate count is improved while compromising the garbage count. Additionally for several small functions, we obtained overall improved or matching performance.

For an exhaustive run on all 3-variable Boolean function an average gate count of 7.6, maximum gate size of 14 and average garbage count of 2.3 is obtained. In [11], garbage-free synthesis is done with an average gate count of 6.1. The optimal gate count for NCT library is found as 5.87 [28]. Note that, in comparison with [11], our method is several orders of magnitude faster. While [11] reports half a second to 5 seconds for an exhaustive run on all 3-variable Boolean function an average gate count of 5.92 and an average garbage count of 0.95 is obtained. This shows that for small variable count, the optimized output produced by EXORCISM-4 [22] outweighs the optimizations presented in this paper.

In the presented flow, it is observed that for Boolean functions with large variable count (> 10), most of the processing time is spent in the optimization engines. The determination of target node and mapping to Toffoli circuit is extremely fast. When no optimization engine is run, the synthesis takes similar execution time compared to that reported in BDD-based methods. Presumably, the coupling of a fast and rule-based ESOP optimization flow such as [22] can improve the overall synthesis runtime. Interestingly, the generation of optimized ESOP in [22] uses a BDD-based representation.

With a simple trade-off approach between QC and garbage count, we showed that improvement of QC is possible in a controlled manner. Moreover, better QC and gate count compared to state-of-the-art synthesis methods can be obtained, too. This findings can be crucial to develop reversible logic.
synthesis tools with more control over the synthesis outcome and to investigate further into the potential of ESOP-based synthesis methods.

E. Ancilla-Free ESOP-based Reversible Logic Synthesis

For the ancilla-free approach outlined in the section [LV] we experimented with all 3-variable Boolean functions and selected 4-variable Boolean functions. For all the 3-variable circuits our approach converged to an ancilla-free reversible circuit. For the 4-variable Boolean functions, which we studied, all but one (αβγ15, 4) function converged to ancilla-free result. Due to our focus on achieving ancilla-free synthesis from an ESOP formulation, the QC and gate counts fared poorly. For example, in case of 3-variable circuits, our heuristics selected Tof2 gates in a greedy manner. This potentially neglects globally optimal solutions with Tof3 gates.

For the 3-variable Boolean functions, an average gate count of 9.28 and an average QC of 17.14 is obtained in our method. In contrast, the average gate count and QC values for optimal 3-variable circuits are 5.87 and 13.74 respectively [23].

VI. CONCLUSION AND OUTLOOK

In this paper, a parameterizable ESOP-based reversible logic synthesis flow is presented, which allows trade-off between QC and garbage count. The results are compared with state-of-the-art synthesis tools. It shows that significant benefits in performance can be obtained by tuning the optimizations and/or compromising the garbage count. Furthermore, ancilla-free ESOP-based reversible logic synthesis is proposed. The results, in terms of QC, is comparable to transformation-based reversible logic synthesis.

In future, further investigation will be done to appreciate the interplay between ESOP minimization and the quality of reversible circuit. Methods to relax the garbage count for better QC will be explored in the context of other reversible logic synthesis methods. Furthermore, the QC adopted for this paper needs to be updated with latest Clifford+T model of Quantum computing primitives.

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Garbage-free Synthesis
Transformation-based Method

Garbage-free Synthesis
ESOP-based Method