A stable and two-step settling digital controlled AGC loop for GNSS receiver

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Abstract: Based on a statistic algorithm, a novel all-digital controlled AGC loop for GNSS receiver chip is proposed in this paper. The algorithm achieves the AGC function as well as low cost by using the Gaussian white noise characteristic of GNSS signal. Gain settling procedure is optimized to at most two steps by accurate power estimation. The stability of the proposed feed-forward AGC loop is discussed, which is rarely involved in some similar GNSS chips. The AGC loop further composed of PGA is applied in a GNSS receiver chip and occupies an area of 0.21 mm\textsuperscript{2}. The measured settling time is less than 32 µs.

Keywords: digital AGC loop, fast settling, GNSS receiver chip, Gaussian white noise, high stability

Classification: Electron devices, circuits, and systems

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1 Introduction

Automatic gain control (AGC) circuitry is an important part in global navigation satellite system (GNSS) receivers, which contains the global positioning system (GPS), Galileo, GLONASS, and COMPASS (also known as BeiDou), due to indoor circumstance, temperature variation or radio frequency interference and so on. All digital assisted AGC loop is widely used in receiver chips because of low cost and fast settling.

Conventional digital controlled AGC system estimates the power with peak-to-peak or root mean square (RMS) power detection. And almost all digital AGC adopt a multi-step scheme for accurate gain adjustment, which will lead to longer settling time. Besides settling time, loop stability is another important topic for AGC loop. But the stability of feed-backward digital AGC loop is rarely discussed in reported GNSS receiver chips [1, 2, 3]. Unstable AGC may result in continuously gain adjusting in practice, which means the loop cannot converge.

So a novel digital controlled AGC algorithm based on Gaussian white noise distribution statistic characteristic of GNSS signal is presented to improve the performance. By solving the inaccurate power estimation problem caused by clipping effect error of ADC in the AGC loop, we limit the gain adjustment procedure to two steps at most, which means faster settling time. The stability is simultaneously ensured. The AGC loop circuitry is applied in a GNSS receiver chip and implemented in 0.18 µm CMOS process, as shown in Fig. 1, the measurement result shows the functionality and performance of the AGC algorithm and circuitry.

2 AGC algorithm

2.1 Basic idea

As all of the GNSS system is a spread spectrum system, and the received signal power is less than $-130$ dBm in GNSS RF band which is approximately 20 dB below the thermal noise [4]. Therefore, the received signal power strength is actually dominated by thermal noise with Gaussian distribution [1], even after down-converted to intermediate frequency (IF) signal. Assuming the strength of AGC input signal obeys Gaussian distribution $N(\mu, \sigma)$, where $\mu$ is equal to zero without considering of DC, and $\sigma$ actually represents the power strength of IF signal, as shown in Fig. 2(a). The probability density function (PDF) of the input signal can be expressed by Eq. (1).
An important problem of digital AGC is the clipping effect error due to ADC dynamic range limitation, so the function of AGC is usually regarded as matching the input signal amplitude to the dynamic range of ADC [5]. Because of the randomness of Gaussian white noise, the clipping error is unavoidable which will result in inaccurate power estimation and then a multi-step gain adjusting procedure. In this paper, the clipping effect is considered as a restriction range \([-a, a]\) in the PDF curve as shown in Fig. 2(a), so the signal quantified percentage within the restriction of \([-a, a]\) can be denoted as follows:

\[
P(-a, a) = \frac{1}{\sqrt{2\pi}a} \int_{-a}^{a} \exp\left(-\frac{r^2}{2a^2}\right) dr
\]

where \(K = \frac{a}{\sigma}\), \(\Phi(K) = \int_{-\infty}^{K} \frac{1}{\sqrt{2\pi}} e^{-\frac{t^2}{2}} dt\)

The value of \(\Phi(K)\) can be found from standard normal distribution table. The relation between clipping error, \(P(-a, a)\) and \(K\) is shown in Fig. 2(b) that indicates when \(K\) is greater than 2.5, the clipping error is very small to be ignored, \(P(-a, a)\) is approximately 98% at this point. Obviously, if \(P(-a, a)\) is determined by designer, \(K\) and \(\Phi(K)\) are all constants, which indicate that whatever the input power (represented by \(\sigma\)) changes, once \(P(-a, a)\) is previously determined, the boundary \(a\) will follow to change in order to keep \(K\) as a fixed value. The AGC loop is based on the analysis above, the architecture of proposed AGC loop is shown in Fig. 3.

![Fig. 2.](image1.png)  
(a) Probability density curves of AGC input signal with boundary condition  
(b) Relation of quantified percentage and clipping error with \(K\)

![Fig. 3.](image2.png)  
Architecture and tracking model in log-domain of proposed AGC loop
The power estimation of ADC input signal $r(t)$ can be calculated by the output signal $x(n)$ as follows:

$$P_{est}(n) = \sum_{n=0}^{M-1} |x(n)| / M \quad (M = 2^i, i = 1, 2, 3 \ldots)$$  \hspace{1cm} (3)

The absolute value operation is adopted to reduce the cost of on-chip digital circuit, which caused by complicated multiplication or square operation in conventional RMS power estimation. $M$ is the sample period in a statistic interval, which is usually set to $2^i$ ($i = 1, 2, 3 \ldots$), so the division operation can be replaced by shift operation.

Based on Eq. (2), the accurate power estimation result $P_{est}$ can be regarded as the expectation of absolute value for $r(t)$ within $[-a, a]$ (region III in Fig. 2(a)), which can be written as Eq. (4). Then, the ratio of $E(|r(t)|)$ and boundary condition $a$ is a function of $K$, which can be derived and simplified as:

$$E(|r(t)|) = \frac{1}{\sqrt{2\pi}\sigma} \int_{-\infty}^{\infty} |r| \exp\left(-\frac{r^2}{2\sigma^2}\right) dr = \frac{2}{\sqrt{2\pi}\sigma} \left( \int_{a}^{\infty} r \exp\left(-\frac{r^2}{2\sigma^2}\right) dr + \int_{-\infty}^{a} a \exp\left(-\frac{r^2}{2\sigma^2}\right) dr \right)$$  \hspace{1cm} (4)

$$\frac{E(|r(t)|)}{a} = \frac{2}{\sqrt{2\pi}\sigma} \left(1 - \exp\left(-\frac{K^2}{2}\right) \right) + 2(1 - \Phi(K)) = g(K)$$  \hspace{1cm} (5)

Eq. (5) illustrates an important fact that once the quantified percentage $P[-a, a]$ (such as 98%) is determined, then $K$ is a constant, and the ratio of $E(|r(t)|)$ and boundary $a$ is also a constant. Therefore, when the boundary condition $[-a, a]$ equals to ADC dynamic range $[-A_d, A_d]$, $E(|r(t)|)$ should be a fixed value that is actually the reference power $P_{ref}$ (region I in Fig. 2(a)). Then $P_{ref}$ can be derived by the proportional relation mentioned in Eq. (5) as follows:

$$\frac{P_{ref}}{A_d} = \frac{E(|r(t)|)}{a} = g(K)|_{K=K_0} \quad \text{where} \quad K_0 = \frac{A_d}{\sigma_0}$$  \hspace{1cm} (6)

$\sigma_0$ represents the reference power and $K_0$ is determined by the preset $P[-a, a]$. Then the essence of the proposed AGC algorithm can be described from a new perspective that the function of AGC loop can be considered as the strength PDF curve approaching from arbitrary curve to reference curve by gain adjusting.

### 2.2 Gain adjustment

In theory, only one step is enough for the gain adjustment procedure from $P_{est}$ to $P_{ref}$. But the clipping error problem will lead to inaccurate power estimation, so almost all digital AGC loop need a multi-step gain adjustment scheme.

In this paper, the gain adjusting steps or settling time can be decreased by improving accuracy of power estimation. Assuming the power estimation circuit works with much quantization errors, then $P_{est}$ is actually calculated within the boundary $[-A_d, A_d]$ rather than $[-a, a]$ (region II in Fig. 2(a)). Now, $P_{est}$ is actually calculated as follows:

$$\frac{P_{est}}{A_d} = \frac{2}{\sqrt{2\pi}K'} \left(1 - \exp\left(-\frac{K'^2}{2}\right) \right) + 2[1 - \Phi(K')] = g(K)|_{K=K'} \quad \text{where} \quad K' = \frac{A_d}{\sigma}$$  \hspace{1cm} (7)

$\sigma'$ represents current power. Now, $P_{est}$ have deviated from accurate power estimation and cannot meet the preset $P[-a, a]$ or $K_0$. But according to the proportional relation in Eq. (5), the estimated power can be corrected as follow:
\[
\frac{P_{\text{est,cor}}}{a} = \frac{P_{\text{ref}}}{A_d} = g(K)|_{K=K_0} \quad \text{and} \quad \begin{cases} K' \cdot \sigma' = A_d \\ K_0 \cdot \sigma = a \end{cases} \Rightarrow P_{\text{est,cor}} = \frac{K_0}{K'} \cdot P_{\text{ref}} \quad (8)
\]

\(K'\) can be derived from Eq. (7). And then, based on the corrected power estimation value \(P_{\text{est,cor}}\) the logarithmic domain AGC tracking model in Fig. 3 [6], the gain adjustment method can be derived as follow:

\[
G(n) = \begin{cases} G(n-1) - \alpha \cdot (P_{\text{est,cor},dB} - P_{\text{ref},dB}) & \text{for} \quad |P_{\text{est,cor},dB} - P_{\text{ref},dB}| > \Delta P_{\text{lock}} \\ G(n-1) & \text{for} \quad |P_{\text{est,cor},dB} - P_{\text{ref},dB}| \leq \Delta P_{\text{lock}} \end{cases} \quad (9)
\]

\(G(n-1)\) is the current gain of AGC, \(G(n)\) is the gain of next step. \(P_{\text{est},dB}, P_{\text{ref},dB}, P_{\text{est,cor},dB}, \) etc. are the corresponding variables in logarithmic domain of \(P_{\text{est}}, P_{\text{ref}}, P_{\text{est,cor}}, \) etc. \(\alpha\) is the gain factor of each step for the multi-step gain adjustment method in [6], and \(\alpha\) equals to 1 for the one step method presented in this paper. \(\Delta P_{\text{lock}}\) is a hold window (such as 1 dB range). AGC loop is considered as a locked and stable system in the window to avoid continuous gain adjusting.

According to the analysis above, the gain adjustment procedure will be only once in most cases. But a fact must be point out that the gain adjustment steps sometimes need to be twice. Main reason is input signal changes in the middle of a statistic interval, which leads to inaccurate power estimation. Another reason is the calculation accuracy restriction due to bit width of ADC and VGA gain step.

2.3 Stability of proposed AGC loop

The tracking model in Fig. 3 can also be used to analyze the stability of AGC loop, the system is linear in logarithmic domain. For \(P_{\text{in},dB}\) and \(P_{\text{ref},dB}\) are step signals, after step response analysis based on the system model, the estimated power can be expressed in Z domain as follow [6]:

\[
P_{\text{est,db}}(z) = \frac{z P_{\text{in},dB}}{z - 1 + \alpha} + \frac{\alpha \cdot z P_{\text{ref},db}}{(z - 1)(z - 1 + \alpha)} \quad (10)
\]

One of the stability criterions is the final value theorem that expressed in Eq. (11). It illustrates the convergence property of AGC loop that the signal \(P_{\text{est,db}}\) will eventually be stabilized to \(P_{\text{ref,db}}\) by gain adjustment.

\[
P_o = \lim_{z \to 1} (z - 1)P_{\text{est,db}}(z) = P_{\text{ref,db}} \quad (11)
\]

Another stability criterion is the unit circle stability criterion. According to the criterion, if the condition, \(0 < \alpha < 2\), is satisfied in Eq. (10), the AGC is a stable system, actually it equals to 1 in the proposed AGC. Simulation result shows the comparison of gain adjustment procedure between proposed method and other conventional method in same change of input signal, as shown in Fig. 4. Obviously, the proposed method is less steps and continuous adjustment does not occur.

![Simulation result of conventional and proposed gain adjustment procedure](image-url)
3 Circuit implementation

3.1 PGA circuit

The programmable gain amplifier (PGA) is designed as a three-cascaded stage architecture [7], as shown in Fig. 5(a). The first two stages are designed to achieve a 20 dB gain tuning range from −4 dB to 16 dB with a 4 dB gain step respectively, providing the coarse gain tuning control. While the third stage is designed to achieve a 22 dB gain tuning range from −2 dB to 20 dB with a 2 dB gain step, which provides the fine gain-tuning control. The whole PGA has an overall gain range of 62 dB gain range (from −10 dB to 52 dB, in 2 dB steps) and 120 MHz bandwidth.

Fig. 6 gives the schematic of the single-stage PGA, which mainly consists of a source-degenerated differential gain amplifier, a gm-boosting circuit, and a CMFB circuit [7]. The gain is adjusted by switched resistors array of \( R_s \) and \( R_{Ld} \) for coarse gain tuning and fine gain control, respectively.

![Fig. 5. (a) Three-stage PGA architecture (b) Schematic of the digital AGC](image)

Fig. 6. Schematic of the implemented single-stage PGA

3.2 Digital control part

Fig. 5(b) gives the schematic of digital AGC part, which is designed fully according to the proposed AGC algorithm. A multiplexer is adopted to obtain the absolute value by the sign bit selection. An accumulator and a shifter calculate the estimated power according to Eq. (3). The Look Up Table (LUT) circuit is suitable to implement the complicated algorithm with low cost, which generates the gain adjustment from corrected estimated power, reference power and current gain according to Eq. (9).

4 Measurement result

The die micro-photograph of the implemented GNSS RF front-end chip including the AGC loop is shown in Fig. 1(b). The PGA and digital AGC totally occupy an
area of 0.21 mm², and current consumption of PGA and AGC is 2.1 mA with a 1.8 V power supply. The AGC loop is configured as closed loop mode and measured by importing a GNSS carrier signal which is modulated with a 150 µs pulse [8]. The wave of input and output signal is shown in Fig. 7. It shows that when input signal changes between about 20 mV and 300 mV, the output of AGC loop is finally stabilized at about 200 mV after two steps gain adjustment. The settling time is about 30 µs, current clock is 62 MHz and the sample period is 1024 per statistic interval. Because input signal changed in the middle of a statistic period, the AGC adjusted twice. A summary of the measured results is provided in Table I, along with a comparison with the similar AGC loops for GNSS chips.

![Input modulated Gaussian white noise](image1) ![AGC output response](image2)

**Fig. 7.** Measured waveform of AGC loop

| Items            | ASSCC’10 [9] | ICSICT’10 [2] | J.Semicond’12 [3] | This work |
|------------------|--------------|---------------|-------------------|-----------|
| Process (nm)     | 180          | 180           | 65                | 180       |
| Gain control     | Analog       | Digital       | Digital           | Digital   |
| Dynamic range (dB)| 55           | 29.5          | 50                | 62        |
| Settling time (µs)| 900         | <250          | <180              | 16–32*    |
| Die area (mm²)   | -            | 0.275         | 0.23              | 0.21      |
| Power (mW)       | 3.6          | -             | 2                 | 3.7       |

*The settling time is limited by the clock frequency and statistic interval

## 5 Conclusion

Based on the Gaussian white noise statistic characteristic of GNSS signal, a novel digital AGC loop has been proposed in this paper. The whole circuitry composes of three-stage PGA, digital AGC part and 4bits ADC. The area and power consumption of the digital control part is 0.09 mm² and 1.1 mW, which benefited from the AGC algorithm. The gain adjustment procedure is at most two steps and settling time is less than 32 µs when circuit works in 62 MHz clock and 1024 sample period per statistic interval. The settling time can be further improved by higher clock and sample frequency. Algorithm analysis and simulated result shows the AGC loop is stable. The proposed AGC loop can also apply to other similar Gaussian white noise signal system, even the sine wave signal system.

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