Development of Low Frequency Small Signal Amplifier using BJT-JFET in Sziklai Pair Topology

Sachchidanand Shukla, Pratima Soni, Naresh Kumar Chaudhary, Geetika Srivastava

Abstract: A new PSpice Model of BJT and JFET is proposed and its hybrid combination is used in Sziklai pair topology to design small signal amplifier. The proposed amplifier with maximum voltage gain 30.41, maximum current gain 43.05 and THD 2.44% is capable of amplifying low magnitude signals in a frequency range distributed from 3.035Hz to 93.808Hz. This feature explores the possibility to use proposed amplifier circuit in EEG, seismographs and underwater communication circuits. Three different circuit/device combinations are also exposed during the exploration of proposed amplifier and therefore mentioned with primary details. Qualitative behaviour, e.g. temperature dependency, noise behaviour, effect of the variation of biasing resistances and capacitors, small signal AC analysis etc., of the proposed circuit, is also studied to observe its performance under different environment.

Keywords: Sziklai pair, Circuit Simulation, Small signal Amplifier.

I. INTRODUCTION

Sziklai pair utilizes a very similar topology of Darlington Pair with comparable beta boosting configuration to provide very high levels of current amplification factor $\beta$ [1]. Darlington pair holds a current amplification factor $\beta_{D}=\beta_1\beta_2+\beta_1+\beta_2$ whereas this for Sziklai Pair is slightly less ($\beta_{S}=\beta_1\beta_2+\beta_1+\beta_2$) as there is no individual contribution from second unit [1-2]. Sziklai pairs are often used in the output stage of power amplifiers due to their effectiveness in linearity, switching speed and moreover with half of the base turn-on voltage than Darlington Pair [3]. However, its use in development of small signal amplifiers is still the area of interest for the researchers [4-6]. In recent years, Shukla et. al. have proposed a number of Sziklai pair topologies with unlike BJTs and hybrid combination of BJT, JFET, MOSFET to constitute small signal amplifiers [4-6].

Present investigation includes the development and analysis of a small signal amplifier, the active device of which accommodates user defined models of NPN-type BJT and P-type JFET to constitute a hybrid amplifying unit under Sziklai pair topology. The proposed amplifier is an extended version of the circuit proposed by Shukla et. al. with superior and magnificent outcomes that suggests its usefulness in biomedical applications, seismic operations and underwater communication systems [6].

II. CIRCUIT DETAILS

Present investigation is furnished with the aid of PSpice simulation [7]. It consists of a qualitative comparison between the two circuits of small signal Sziklai pair amplifiers referred herein as Circuit-1 and Circuit-2 [6]. Circuit-1 (the reference circuit) represents the amplifier design of Shukla et. al. whereas its modified version is proposed and analyzed herein as Circuit-2 (the proposed Circuit) [6].

Fig.1. Describing basic circuit structure of the amplifiers under discussion

| Component | Circuit-1 | Circuit-2 | Case-1 | Case-2 | Case-3 |
|-----------|-----------|-----------|--------|--------|--------|
| QN (NPN)  | Qbreakn   | QMODN     | Qbreakn| QMODN  | Q2N2222 |
| JP (P-JFET) | Jbreakp   | JMODP     | Jbreakp| JMODP  | JMODP  |
| Rs        | 10Ω       | 10Ω       | 10Ω    | 10Ω    | 500    |
| R1        | 70KΩ      | 500KΩ     | 500KΩ  | 66KΩ   | 100K   |
| R2        | 40KΩ      | 45KΩ      | 45KΩ   | 45KΩ   | 47K    |
| R3        | 8KΩ       | 200KΩ     | 200KΩ  | 10KΩ   | 9K     |
| R4        | 6KΩ       | 4KΩ       | 4KΩ    | 4KΩ    | 5K     |
| R5        | 20KΩ      | 20KΩ      | 20KΩ   | 10KΩ   | 10K    |
| C1 and C2 | 10µF      | 10µF      | 10µF   | 10µF   | 10µF   |
| C0        | 100µF     | 100µF     | 100µF  | 100µF  | 100µF  |
| C3        | 10µF      | 0.1µF     | 0.1µF  | 0.1µF  | 0.1µF  |
| Vcc       | +15V      | +10V      | +10V   | +10V   | +15V   |
| AC Source | 1V        | 1V        | 1V     | 1V     | 1V     |

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During exploration with reference and proposed circuits, some interesting findings are also observed with three different circuits/device combinations. Along with reference and proposed amplifiers (Circuit-1 and Circuit-2), component details of other three circuits are also listed in Table-I as Case-1, Case-2 and Case-3. However, the basic circuit configuration describing all the respective circuits is depicted in Fig.1. Since related findings of the Case-1, Case-2 and Case-3 circuits are not exactly covering the context of the present paper hence these circuit cases are not attempted herein for the analysis purpose but a line of discussion corresponding to these three special cases are included in the manuscript. In addition, simulation parameters used to model BJT and JFET under Sziklai pair topology are listed in Table-II [7].

### Table-II: Simulation Parameters used in Device Modelling

| PSpice device parameters | Qbreakn | QMODN | Jbreakp | JMODP |
|--------------------------|---------|-------|---------|-------|
| BS                       | 100.0E-18 | 1.1105E-15 | NA     | 1.00E-12 |
| BF                       | 100     | 173   | NA     | NA    |
| NF                       | 1       | 1     | NA     | NA    |
| VAF                      | Default | 103.3 | NA     | NA    |
| BR                       | 1       | 1     | NA     | NA    |
| NR                       | 1       | 1     | NA     | NA    |
| CJE                      | Default | 960.00E-15 | NA     | NA    |
| CIC                      | Default | 4.00E-12 | NA     | NA    |
| CN                       | 2.42    | 2.42  | NA     | NA    |
| TF                       | Default | 489.80E-12 | NA     | NA    |
| TR                       | Default | 4.900E-09 | NA     | NA    |
| VTO                      | NA      | NA    | -2     | 4     |
| BETA                     | NA      | NA    | 100.00E-0 | 1.00E-03 |
| RD                       | NA      | NA    | Default | 50    |
| RS                       | NA      | NA    | Default | 50    |

(NA : Not Admissible)

Refer Table-I and Table-II. Reference amplifier (Circuit-1) has default models of NPN-type BJT ‘Qbreakn’ at the driver position and P-channel J-FET ‘Jbreakp’ at the follower position [6]. However, the proposed amplifier (Circuit-2) has user defined models of NPN-type BJT ‘QMODN’ and P-channel J-FET ‘JMODP’ at driver and follower positions respectively. Since NPN transistor is kept at driver position in the hybrid units of respective amplifiers, the respective device models are treated as to hold N-type Sziklai pair topology [3]. C_L has to be essentially included in the proposed circuit to receive the reported findings. The Case-1 circuit uses a different Sziklai pair composition with default model of NPN-type BJT ‘Qbreakn’ and user defined model of P-type JFET ‘JMOPD’ but AC source and biasing combinations are kept similar to Circuit-2. On the other hand, Case-2 circuit uses a Sziklai pair composition having user defined Spice model of NPN-type BJT ‘QMODN’ and default Spice model of P-type JFET ‘Jbreakp’ with a different biasing combination but AC source similar to Circuit-2. However, the Case-3 circuit accommodates a combination of commercial NPN-type BJT ‘Q2N2222’ and user defined Spice model of P-type JFET in Sziklai pair topology with different biasing environment but AC source similar to Circuit-1.

### III. RESULTS AND DISCUSSIONS

Table-III describes the values corresponding to various performance parameters recorded for Circuit-1, Circuit-2, Case-1, Case-2 and Case-3 amplifiers. These performance parameters are Maximum Voltage Gain (AVG), Maximum Current Gain (AG), Higher Cut off Frequency (F_H), Lower Cut off Frequency (F_L), Bandwidth (BW), Peak Output Current (I_O), Peak Output Voltage (V_O), Input to Output Signal Phase Difference (θ) and Total Harmonic Distortion (THD). However, Fig.2 depicts the variation of voltage gain with frequency for Circuit-1 and Circuit-2. It can be observed by Fig.2 that the response curve of Circuit-1 peaks around 6Hz whereas for Circuit-2 it peaks around 16Hz.

### Table-III: Performance Parameters of the Circuits under Discussion

|                      | Circuit 1 | Circuit 2 | Case-1 | Case-2 | Case-3 |
|----------------------|-----------|-----------|--------|--------|--------|
| AVG                  | 5.738     | 30.413    | 21.585 | 2.1707 | 124.151|
| AG       | 5.517     | 43.054    | 29.924 | 0.627 | 63.887 |
| F_H                 | 15.47Hz   | 93.80Hz   | 92.32Hz | 6.94KHz | 492.40KHz |
| F_L                 | 2.05Hz    | 3.03Hz    | 2.41Hz  | 130.13Hz | 45.75Hz |
| BW                  | 13.41Hz   | 90.77Hz   | 89.90Hz | 6.81KHz | 492.35KHz |
| I_O                 | 7.098mA   | 1.046mA   | 722.47mA | 136.80mA | 12.67μA |
| V_O                 | 144.28mV  | 20.85mV   | 14.47mV | 1.361mV | 126.70mV |
| θ°                  | 178.56°   | 143.33°   | 141.76° | 109.90° | 180° |
| THD                 | 6.30%     | 2.44%     | 2.47%   | 4.06%  | 0.83%  |

Data in Fig.2 and Table-III reveals that the reference amplifier (Circuit-1) provides faithful amplification in 2.058Hz to 15.476Hz frequency range with Bandwidth BW=13.418Hz, Maximum voltage gain AVG=5.738, Maximum current gain AG=5.517 and Total Harmonic Distortion THD=6.30%. However, the proposed amplifier (Circuit-2) provides significantly enhanced voltage gain (AVG=30.413) and current gain (AG=43.413), reduced THD (2.44%) and wider Bandwidth (BW=90.773Hz) with an extended frequency range of faithful amplification distributed from 3.035Hz to 93.808Hz.

### Fig.2. Frequency response of the Circuits under discussion

Performance parameters in Table-III and the Fig.2 indicates that the reference amplifier (Circuit-1) is capable of amplifying signals of 2Hz to 15Hz range of frequency, representing delta, theta and alpha type of waves, released by human brain [8-9]. However, with the user defined Spice model of BJT and JFET under Sziklai pair topology, the proposed amplifier (Circuit-2) can amplify a wider array of low frequency waves (namely Delta, Theta, Alpha, Beta and Gamma waves) falling in 3Hz to 93Hz range [8-10].
Thus, the proposed amplifier covers almost the complete frequency spectrum of the vibrations released by human brain or emerged during seismic operations and therefore can play an important role in pre-amplifier stage of seismometers and dealing with the variety of patients’ problems like stress, lack of sleep, anxiety, abrupt sleep patterns etc., if used at preamplifier stage in biomedical instrument like EEG (Electroencephalogram) [8-10]. It is also to mention that observations in Table-III for proposed amplifier (Circuit-2) are recorded for 1V AC input signal source from which 1mV, 100Hz signal is provided for the amplification purpose whereas reference amplifier (Circuit-1) uses 1mV,1KHz signal for the purpose of amplification.

It is also observed that if the proposed amplifier (Circuit-2) is fed with 1mV, 10Hz signal, THD of the amplifier dips to 0.967% with almost unaltered values of $A_{VG}$, $A_{G}$ and $B_{w}$ whereas if 1mV, 1KHz signal is provided for amplification, respective circuit comes up with 9.707% THD with almost unchanged values of other performance parameters. Moreover, the proposed amplifier is found capable of amplifying 1μV (THD 2.513%) to 10mV (THD 5.153%) range of AC input signal at 100Hz frequency.

In addition, initial findings with Case-1, Case-2 and Case-3 circuits (refer Table-II and Table-III) are reported as follows –

Case-1: When PSpice default model of NPN-type BJT ‘Qbreakp’ is used at driver position and user defined model of P-type JFET ‘JMODP’ in Sziklai pair topology with similar biasing environment of Circuit-2 (refer Table-II), respective circuit produces $B_{w}=89.90Hz$ ($F_{1}=2.418Hz$ and $F_{1G}=92.323Hz$), $A_{VG}=21.585$, $A_{G}=29.924$ and THD=2.47%. The respective findings suggest that this circuit behaves more or less like Circuit-2 amplifier and therefore holds almost similar application range. However, if $C_{1}$ is removed from Case-1 circuit, the amplifier emerges with maximum voltage gain $A_{VG}=22.22$. Maximum current gain $A_{G}=30.495$ and THD=1.54% and starts behaving like a high pass filter with lower cut-off frequency $F_{1}=2.548Hz$.

Case-2: When user defined model of NPN-type BJT ‘QMODN’ is used at driver position with default position of model of P-type JFET ‘Jbreakp’ in Sziklai pair topology along with the biasing components as depicted in Table-I, respective amplifier circuit produces 6.817KHz bandwidth with voltage gain above unity and current gain below unity. Respective values of other performance parameters are as listed in Table-III. This design can possibly be used in various communication systems where system requirement is to amplify low strength signals in frequency band extended from 130.135 Hz to 6.948 KHz.

Case-3: When a commercial model of NPN-type BJT ‘Q2N2222’ is used at driver position with user defined Spice model of P-type JFET ‘JMODP’ in Sziklai pair topology along with the biasing components as depicted in Table-I, the circuit responds with significantly widened bandwidth (492.355 KHz), enhanced voltage and current gains and considerably reduced THD. This indicates that the respective design may be favourably used to explore small signal general purpose audio amplifier [11-12].

Behaviour of Performance parameters with respect to temperature variation for proposed amplifier is listed in Table-IV. The proposed amplifier shows gradual elevation in voltage and current gains with rising temperature up to 27°C. Beyond this limit respective parameters start decreasing whereas bandwidth and THD continue to increase with temperature. Declination in voltage and current gains beyond limiting temperature is probably due to the ‘negative temperature coefficient’ property of drain current of the JFET at follower position in Sziklai pair topology [13]. The drain current in JFET is mainly comprised of majority carriers whose mobility decreases the rise of temperature due to enhanced collision rate between them and remaining ions in the semiconductor channel [14]. This perhaps decreases the drain current of JFET at follower position and therefore the effective current and voltage gain of the amplifier system. In addition, the proposed amplifier provides faithful amplification in the temperature range -30°C to +50°C.

| Temp. (°C) | $A_{VG}$ | $A_{G}$ | $F_{1}$ (Hz) | $F_{1G}$ (Hz) | $B_{w}$ | THD (%) |
|-----------|----------|--------|--------------|--------------|--------|--------|
| -30       | 20.458   | 33.541 | 2.248        | 92.367       | 90.119 | 2.53   |
| -20       | 22.510   | 36.086 | 2.434        | 92.761       | 90.327 | 2.52   |
| -10       | 24.425   | 38.347 | 2.603        | 93.412       | 90.809 | 2.49   |
| 0         | 26.212   | 40.355 | 2.750        | 94.600       | 91.850 | 2.48   |
| 10        | 27.879   | 42.150 | 2.952        | 94.628       | 91.676 | 2.46   |
| 20        | 29.437   | 43.755 | 3.076        | 93.695       | 90.619 | 2.45   |
| 27        | 30.413   | 43.054 | 3.035        | 93.808       | 90.773 | 2.44   |
| 30        | 28.106   | 31.140 | 3.976        | 102.755      | 98.779 | 3.28   |
| 40        | 18.921   | 2.629  | 7.303        | 148.280      | 140.977 | 3.09 |
| 50        | 14.079   | 1.447  | 9.089        | 190.499      | 181.410 | 3.78 |

During the circuit operation, electronic circuits, because of the essential presence and distinct behaviour of active and passive components at different frequencies, generate noises in Input and Output sections of the circuit system [7]. Input and Output noises, appear during the amplification process for proposed amplifier at operating frequency (100Hz), comparatively low frequencies (10Hz) and at relatively high frequency (1KHz) are observed at different temperatures. A respective observation, listed in Table-V, clearly indicates that noises at defined frequencies for proposed amplifier are found low enough and within the permissible limit.

| Temp. (°C) | Noise at 10Hz (V/Hz) | Noise at 100Hz (V/Hz) | Noise at 1KHz (V/Hz) |
|-----------|---------------------|----------------------|---------------------|
| -30       | 5.587               | 2.749                | 2.455               |
| -20       | 5.991               | 2.686                | 2.466               |
| -10       | 6.376               | 2.642                | 2.406               |
| 0         | 6.744               | 2.611                | 2.359               |
| 10        | 7.098               | 2.591                | 2.324               |
| 20        | 7.437               | 2.578                | 2.296               |
| 27        | 7.653               | 2.573                | 2.281               |
| 30        | 6.965               | 2.596                | 2.291               |
| 40        | 4.249               | 2.733                | 2.362               |
| 50        | 3.018               | 2.874                | 2.437               |

| Noise at 10Hz (V/Hz) | Noise at 100Hz (V/Hz) | Noise at 1KHz (V/Hz) |
|---------------------|----------------------|---------------------|
| OUT (x10^-5)        | IN (x10^-5)          | OUT (x10^-5)        |
| -30                  | 5.481                | 2.545               |
| -20                  | 5.991                | 2.464               |
| -10                  | 6.376                | 2.403               |
| 0                    | 6.744                | 2.357               |
| 10                   | 7.098                | 2.321               |
| 20                   | 7.437                | 2.293               |
| 27                   | 7.653                | 2.278               |
| 30                   | 6.965                | 2.287               |
| 40                   | 4.249                | 2.358               |
| 50                   | 3.018                | 2.433               |
It is observed by the records in Table-V that Output noise of the proposed circuit at operating frequencies 10Hz, 100Hz and 1KHz increases with elevation of temperature up to room temperature 27°C and thereafter it decreases. Contrarily, the Input noise at frequencies 10Hz, 100Hz and 1KHz decreases with temperature elevation till room temperature, then starts increasing. Table-V reveals that the temperature ranging in -30°C to 50°C provides favourable amplification environment for the proposed amplifier with low order input and output noises.

Variation of performance parameters with DC biasing voltage is also observed. It is found that the permissible range of DC biasing voltage for proposed amplifier limits to +10V to +20V. Beyond this limiting value of DC biasing voltage the proposed amplifier does not provide faithful amplification. The corresponding values of performance parameters at lower limit of DC biasing voltage (+10V) for proposed circuit are depicted in Table-III whereas at the upper limit (+20V) these parameters are \( V_{CC}=3.292, \quad A_{IG}=0.074, \quad F_{3dB}=37.868\,\text{Hz}, \quad F_{HF}=1.368\,\text{kHz}, \quad B_{W}=1.330\,\text{KHz} \) and THD=7.45%.

### Table- VIA: Performance Parameters at Distinct \( C_L \)

| \( C_L \) (µF) | \( A_{VCC} \) | \( A_{IG} \) | \( F_3dB \) (Hz) | \( F_{HF} \) (Hz) | \( F_{3dB} \) (Hz) | \( B_W \) (KHz) | THD (%) |
|--------------|--------------|-------------|-----------------|-----------------|-----------------|--------------|---------|
| 0.10pF       | 31.5         | 3.374       | 0.1657MHz       | 1.6656MHz       | 1.50            |             |
| 1.00pF       | 31.5         | 3.373       | 1.4273MHz       | 1.4272MHz       | 1.50            |             |
| 0.01µF       | 31.5         | 3.373       | 584.092KH       | 584.088KH       | 1.50            |             |
| 0.10µF       | 31.5         | 3.451       | 83.969KH        | 83.965KH        | 1.49            |             |
| 1.00µF       | 31.5         | 3.372       | 8.774KH         | 8.770KH         | 1.48            |             |
| 0.01µF       | 31.4         | 3.347       | 887.485HZ       | 884.111HZ       | 1.47            |             |
| 0.10µF       | 30.4         | 3.035       | 90.773HZ        | 90.773HZ        | 2.44            |             |
| 1.00µF       | 22.7         | 2.073       | 14.282HZ        | 12.209HZ        | 3.95            |             |

Behaviour of performance parameters of proposed amplifier (Circuit-2) with respect to allowable variations in \( C_D \) or \( C_L \) are depicted in Tables VIA and VIB. Observations in respective tables show that the faithful amplification against distinct values of \( C_L \) is obtained in lower capacitance range distributed from 0.10pF to 1.00µF whereas this for \( C_D \) is observed in higher capacitance range extended from 50µF to 100F. It is also observed that almost all the performance parameters for \( C_D=100\,\mu F \) and \( C_L<0.1\,\mu F \) gradually tends towards state of constancy. The only exception is the gradually increasing values of higher cut off frequency and bandwidth for \( C_L<0.1\,\mu F \).

### Table- VIB: Performance Parameters at Distinct \( C_D \)

| \( C_D \) (µF) | \( A_{VCC} \) | \( A_{IG} \) | \( B_W \) (Hz) | THD (%) |
|--------------|--------------|-------------|--------------|---------|
| 100.0 F      | 31.39        | 44.13       | 88.64        | 2.50    |
| 10.00 F      | 31.39        | 44.13       | 88.64        | 2.50    |
| 1.000 F      | 31.39        | 44.13       | 88.65        | 2.50    |
| 100 mF       | 31.39        | 44.13       | 88.66        | 2.50    |
| 1.00 mF      | 31.39        | 44.13       | 88.67        | 2.50    |
| 100 µF       | 30.41        | 43.05       | 90.77        | 2.44    |
| 50.0 µF      | 29.41        | 42.03       | 94.93        | 3.13    |

On the other hand, all the performance parameters of proposed amplifier except THD decrease at higher \( C_V \) values whereas decreasing value of \( C_L \) is found responsible for considerable widening of the bandwidth (\( B_W \)) with almost stagnant values of Voltage gain, Current gain and THD. The advantageous part of this feature is that the bandwidth widens with shifting of upper cut off frequency \( (F_3) \) only, keeping lower cut off frequency \( (F_L) \) to reside almost in 2-3Hz range. This feature of proposed amplifier provides it a versatile capability of amplifying low magnitude AC signals with a wide range of frequency extended almost from 2Hz to 1.66MHz. More interesting results are received if \( C_L \) is removed from the proposed Circuit-2. The faithful amplification range of the proposed amplifier extends from 3.373Hz to 1.697MHz with widening of the bandwidth \( (B_W=1.6789\,\text{MHz}) \), further enhancement in voltage gain \( (A_{VCC}=31.94) \) and current gain \( (A_{IG}=44.193) \) and considerable reduction in THD (1.50%). However, if \( C_D \) is removed from the Circuit-2, respective amplifier comes up with \( A_{VCC}=3.929, \quad A_{IG}=7.675, \quad F_L=0.415\,\text{Hz}, \quad F_H=88.341\,\text{Hz}, \quad B_W=87.926\,\text{Hz}, \quad \text{THD}=0.985 \).

Biasing resistances play pivotal role in the performance of amplifier circuits, thus a compilation describing the variation range of biasing resistances for seamless amplification is recorded in Tables VIA, VIIB and VIIC. The limiting values of the resistance variation range for distinct biasing resistances, namely \( R_1, R_2, R_D, R_S \) and \( R_t \) are depicted as MIN (minimum resistance value) and MAX (maximum resistance value). Observations recorded in Tables VIA, VIIB and VIIC are received by varying one resistance at a time keeping others constant.

### Table- VIA: Performance Parameters of Circuit-2 at Maximum and Minimum Values of \( R_1 \) and \( R_2 \)

| Performance Parameters | \( R_1 \) (MIN) | \( R_2 \) (MAX) |
|------------------------|-----------------|----------------|
| \( A_{VCC} \)          | 13.242          | 4.237          |
| \( A_{IG} \)           | 1.150           | 8.517          |
| \( B_W \)              | 205.056         | 88.09          |
| \( F_3 \)              | 215.552         | 88.860         |
| \( F_H \)              | 10.496          | 0.771          |
| THD (%)                | 4.765           | 0.518          |
| \( R_1 \)              | 1.774           | 16.719         |
| \( R_2 \)              | 2.483           | 1.805          |
| \( R_3 \)              | 87.909          | 164.789        |
| \( R_4 \)              | 88.624          | 173.636        |
| \( THD \)              | 0.586           | 4.078          |

### Table- VIIB: Performance Parameters of Circuit-2 at Maximum and Minimum Values of \( R_D \) and \( R_S \)

| Performance Parameters | \( R_D \) (MIN) | \( R_S \) (MAX) |
|------------------------|-----------------|----------------|
| \( A_{VCC} \)          | 13.620          | 2.918          |
| \( A_{IG} \)           | 1.200           | 2.628          |
| \( B_W \)              | 200.818         | 87.732         |
| \( F_3 \)              | 211.378         | 88.168         |
| \( F_H \)              | 10.56           | 0.436          |
| THD (%)                | 4.737           | 0.527          |
| \( R_D \)              | 6.999           | 11.379         |
| \( R_S \)              | 10.404          | 1.238          |
| \( R_3 \)              | 404.361         | 191.413        |
| \( R_4 \)              | 407.816         | 199.865        |
| \( THD \)              | 0.918           | 3.847          |

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Though the variation in $R_L$ above and below to its optimum value (as depicted in Table-I) for proposed amplifier does not produce considerable enhancement in voltage and current gains but this facilitates bandwidth to move between 87Hz to 200Hz with capability of amplifying Very Low Frequencies. Similarly, variations in $R_L$ makes amplifier capable to receive a wide range of $A_{VG}$, $A_{BG}$ and $B_W$ with an interesting feature. At maximum value of $R_L$ voltage gain $A_{VG}$ raised to its extreme on the cost of significantly reduced current gain and bandwidth whereas at minimum $R_L$ value current gain and bandwidth receive maximum elevation on the cost of considerably reduced voltage gain. This behaviour of the proposed amplifier with $R_L$ variation is quite in accordance of the small signal Sziklai pair and Darlington pair amplifiers [4-5][11-12]. However, variations in $R_L$, $R_2$ and $R_S$ above and below its optimum value (as depicted in Table-I) do not contribute to elevate voltage and current gains to a considerable level except widening of bandwidth in 87Hz to 404Hz range.

Interesting results are received if $R_{SS}$ is varied between its minimum (0.1Ω) and maximum (100KΩ) possible values for faithful amplification. Variation in $R_{SS}$ helps amplifier to keep THD low, $A_{BG}$ almost unaltered but facilitates to receive $A_{VG}$ in 6.715 to 30.424 range and makes it capable of amplifying signals ranging in 2Hz to 94.840Hz.

Thus, the observations in Tables VIIA, VIIB and VIIC reveal the flexible behaviour of amplifier to amplify signals falling in 0.7Hz (at $R_2$=30KΩ) to 1.6KHz (at $R_1$=1KΩ) frequency range at distinct values of respective biasing resistances with significant elevations in voltage gain (at $R_L$=900KΩ) and current gain (at $R_L$=1KΩ) and considerable declination in THD (at $R_{SS}$=100KΩ).

Conclusively, the appropriate variation in load capacitor $C_L$ or the biasing resistances $R_1$, $R_2$, $R_D$, $R_{SS}$ and $R_L$ makes the proposed amplifier capable of amplifying Very Low Frequency (VLF signal ranges in 3Hz-30Hz) and Super Low Frequency (SLF signal ranges in 3Hz-300Hz) signals which can penetrate seawater to a depth of approximately 20 meters and 100 meters respectively [15-16]. This capability makes proposed amplifier (Circuit-2) suitable to use in VLF receivers/SONAR/autonomous underwater vehicle used for underwater communication [15-16]. Moreover, proper tuning of $C_L$ in proposed amplifier may also facilitate amplification of low frequency low strength signals released by human brain or appears during seismic operations [8-10].
Development of Low Frequency Small Signal Amplifier using BJT-JFET in Sziklai Pair Topology

As depicted in Table-VIII, NPN BJT of the Sziklai unit in Circuit-2 consists base-emitter resistance $r_{be}=98.2\,\Omega$, collector-emitter resistance $r_{ce}=2.08\,\Omega$ and DC current gain factor $\beta=172$. However, P-type JFET of Circuit-2 consists gate-source voltage $V_{GS}=-0.458\,\text{V}$ and small-signal transconductance $g_{m}=1.00\,\text{mA/V}$ whereas drain-source resistance can be calculated to be $r_{ds}=574.21\,\Omega$.

Mathematical analysis of the AC Equivalent Circuit of the proposed amplifier (Fig.6) suggests the following expression for Small Signal AC voltage gain –

$$A_V = \frac{V_D}{V_I} = -\frac{1}{\beta} \frac{R_C}{R_S}$$

Where $R_C=R_{dc}$.

In addition, the Small Signal AC current gain of the proposed amplifier may be obtained as follows -

$$A_I = \frac{i_D}{i_I} = -\frac{1}{\beta} \frac{R_C}{R_S}$$

Where $R_C=R_{dc}$.

On the basis of AC parameters in Table-VIII and the expressions for voltage and current gains, the respective gain values are computed and received as $A_{V\text{-Computed}}=31.723$ and $A_{I\text{-Computed}}=41.023$. These computed values of voltage and current gains are quite closer to simulated values of Voltage gain ($A_{V\text{Simulated}}=30.413$) and Current gain ($A_{I\text{Simulated}}=43.053$) and therefore establish the authenticity of the proposed amplifier configuration of Circuit-2.

### IV. CONCLUSIONS

Small signal amplifier using hybrid combination of the user defined PSpice models of BJT and JFET in Sziklai pair topology is developed and analyzed on the qualitative scale. The proposed amplifier design, due to simultaneously high voltage and current gains and faithful amplification range extended from 3.035Hz to 93.808Hz, can be effectively used in preamplifier stage of EEG, seismograph and underwater communication system. The appropriate variation in biasing resistances and capacitors of the proposed amplifier can bring a wide amplification range of VLF and SLF signals. Observed and computed values of voltage and current gains effectively establish the authenticity of the proposed design. Apart from the proposed amplifier design, three more amplifier systems with similar design but different kind of BJT and JFET models are primarily explored. With low and permissible range of input/output noises, the proposed circuit is found to produce optimum performance in -30°C to 50°C range of temperature at +10V DC biasing source.

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