Characterization of carrier transport properties in strained crystalline Si wall-like structures as a function of scaling into the quasi-quantum regime

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(Dated: May 26, 2015)

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Abstract

We report the transport characteristics of both electrons and holes through narrow constricted crystalline Si “wall-like” long-channels that were surrounded by a thermally grown SiO$_2$ layer. The strained buffering depth inside the Si region (due to Si/SiO$_2$ interfacial lattice mismatch) is where scattering is seen to enhance some modes of the carrier-lattice interaction, while suppressing others, thereby changing the relative value of the effective masses of both electrons and holes, as compared to bulk Si. Importantly, as a result of the existence of fixed oxide charges in the thermally grown SiO$_2$ layer and the Si/SiO$_2$ interface, the effective Si cross-sectional wall widths were considerably narrower than the actual physical widths, due the formation of depletion regions from both sides. The physical height of the crystalline-Si structures was 1500 nm, and the widths were incrementally scaled down from 200 nm to 20 nm. These nanostructures were configured into a metal-semiconductor-metal device configuration that was isolated from the substrate region. Dark currents, dc-photo-response, and carrier “time-of-flight” response measurements using a mode-locked femtosecond laser, were used in the study. In the narrowest wall devices, a considerable increase in conductivity was observed as a result of higher carrier mobilities due to lateral constriction and strain. The strain effects, which include the reversal splitting of light- and heavy- hole bands as well as the decrease of conduction-band effective mass by reduced Si bandgap energy, are formulated in our microscopic model for explaining the experimentally observed enhancements in both conduction- and valence-band mobilities with reduced Si wall thickness. The role of the biaxial strain buffering depth is elucidated and the quasi-quantum effect for the saturation hole mobility at small wall thickness is also found and explained. Specifically, the enhancements of the valence-band and conduction-band mobilities are found to be associated with different aspects of theoretical model.
I. INTRODUCTION

For over 40 years the microelectronics market place has driven the very large scale integration (VLSI) industry to make continuous improvements in computational power, bandwidth and speed. These continued enhancements in performance have come in the form of “cramming” more components onto integrated circuits, as was predicted in 1965 by Gordon E. Moore.

The push to increase the speed and density of the transistors on a chip has come in the form of shrinking the transistor size, in particular the channel length. However, reductions in channel length have come with challenges i.e., short channel effects. Short channel effects lead to higher leakage currents, poor signal-to-noise ratios and instability during operation, such as loss of channel’s gate control.

In order to improve the transistor’s gate control and switching speed, the contemporary metaloxide-semiconductor (CMOS) industry has looked for alternative solutions to the traditional planar transistor designs and substrates.

Over the past several years, the CMOS industry has narrowed their focus into multi-gate field effect transistor designs for improving the gate control, and strained substrates to enhance carrier carrier mobilities and ultimately the switching speed and drive currents.

One particular multigate transistor design that has gained considerable interest among the industry, as a replacement for the planar design, is the FinFET. The FinFET has a tri-gate architecture and reductions of short-channel effects have been observed in these devices. This design provides gate control, not only from the top of the channel, but also from the channel sides as well. This in itself improves the overall (on/off) gate control process, however, the drawback is that these devices require higher operating voltages to achieve faster switching speeds. S. W. Bedell et al., has reported that in the present FinFET technologies, the carrier mobilities are not seen to be enhanced, since the active region of these devices would require two opposite kinds of strain (i.e. tensile and compressive) on the same substrate, which would be possible by converting the tensile strain of silicon-on-insulator substrates to compressive strain in localized regions via a combination of selective SiGe (> 40%) growth. Such FinFET devices have not yet been experimentally demonstrated. However, similar embedded silicon/germanium layered structures that would provide process
induced stressors in the source and drain regions have been theoretically modeled. The results of these simulations show only a modest performance increase, approximately one-half enhancement in mobility, as compared to similar size planar FETs. Process induced strain in a FinFETs would be most effective if it was directly under the gate region, as its stressor’s effectiveness diminishes with depth. Incorporation of wafer level strain using SiGe-on-insulator (SGOI) and Strained Silicon-On-Insulator (sSOI) in small pitched circuits may be possible by converting the tensile strain of sSOI to compressive strain by selective growth of silicon-germanium. However, these type of configurations would certainly add complexities in a high volume manufacturing environment, which could negatively affect yield.

In this paper we report an comprehensive experimental and theoretical study on the nature of carrier transport, of both electrons and holes, through narrow constricted crystalline Si “wall-like” long-channels that were surrounded by a thermally grown SiO$_2$ layer. The carrier transport characteristics are evaluated as a function of dimensional scaling of the Si wall widths from 200 nm to 20 nm. The Si wall-widths were reduced by the process of thermal oxidation, where stress naturally accumulates in the channel. Basically, this structure configuration allows us to investigate the effects of strained regions that are “closing-in” from both sides. Additionally, as the wall-widths approach the quasi quantum regime, the carriers start to become confined and therefore react to the narrow paths, and possibly behave more like waves then particles, thus altering the macroscopic nature of resistance, capacitance and inductance to a more exotic microscopic one. However, this transition into the quantum mechanical regime does not come about abruptly. Rather, there is a transition region in which the bulk properties begin to slowly weaken while the quantum effects begin to strengthen.

The effects of quantum confinement on carrier transport properties, however, have been primarily investigated in ternary and quarternary material heterostructures and superlattices, in which scattering is seen to enhance some modes of the electron-lattice interactions while suppressing others, thereby changing the relative value of the carrier’s effective masses of electrons and holes, as compared to bulk semiconductors. To date such studies in Si have been very limited. We believe that these wall structures are a useful starting point for a broader study, as these can be configured into novel high density 3-D VLSI devices, where
thermal effects, such as heat buildup, can also be efficiently managed.\cite{18}

We organize the rest of the paper as follows: In Sec.\hspace{1mm}II the process for fabricating the crystalline Si wall structures is described, and the two electrode, metal-semiconductor-metal device structure fabrication is also discussed. In Sec.\hspace{1mm}III the experimental dc measurements as a function of wall width thickness are presented, including dark currents and photocurrents.

The electron and hole transient time responses and analysis are done in Sec.\hspace{1mm}III. Section \hspace{1mm}IV provides a detailed model to explain the role of strain effects and how they impact both the electron and hole mobilities, while we summarize in Sec.\hspace{1mm}V.

II. FABRICATION

A. Rationale for substrate material

Silicon-on-insulator (SOI) wafers with a top active layer of \textless 100 > crystal orientation were used to fabricate the wall-like structured devices for this study. The initial SOI structure had a 1500 nm active layer on top of a 3000 nm buried oxide. The SOI configuration allowed complete electrical isolation of the Si wall-like structures from the underlying substrate. All five samples in this study had identical \textit{p}-type active layer with a lightly doped concentration of \text{	extasciitilde}10^{14} \text{cm}^{-3} boron atoms. Intrinsic SOI wafers would have been an ideal choice for the experiment; however, due to the commercial unavailability of 100% intrinsic material, the above choice of dopant type and concentration was adequate enough to minimize the effects of impurity scattering. Boron tends to segregate away from the Si interface and into the thermally grown oxide\cite{19}, thus reducing the impurity concentration near the Si interface with SiO$_2$. Thus the segregation coefficient, which is defined as the ratio of the dopant concentrations at the interface, is less than one in our case. The thermal oxidation process leads to the formation of an oxide trapped charge ($Q_{ot}$), which contribute to the formation of a depletion region near the Si/ SiO$_2$ interface.\cite{20,21} Now, if we combine this oxide trapped charge with the fixed charge ($Q_f$) which naturally results from the excess Si atoms not reacted with the oxygen, and the interface trapped charge ($Q_{it}$) which results from the mismatch between the number of atomic bonds in the Si crystal surface and the number of available bonds in the SiO$_2$ layer, these all sum to ($Q_{ot} + Q_f + Q_{it}$). Combined these form an depletion
region in Si that extends several nanometers away from the SiO$_2$ interface.\textsuperscript{21,22} Thus the effective Si cross-sectional wall widths were considerably narrower than the actual physical widths, due this formation of depletion regions from both sides.

### B. Crystalline silicon wall nanostructure fabrication

In order to fabricate the wall structures, photoresist nano-scale patterning was required. The precursors to the wall structures were patterned using interferometric lithography (IL)\textsuperscript{23} and reactive-ion-etching (RIE)\textsuperscript{24,25}. IL is a well-developed technique for inexpensive nano-patterning process.\textsuperscript{26} IL, in its simplest form, is interference between two coherent waves resulting in a 1-D periodic pattern defined by $\lambda/2\sin \theta$ where $\lambda$ is the optical wavelength and $2\theta$ is the angle between the interfering beams. A typical IL configuration consists of a collimated laser beam incident on a Fresnel mirror (FM) arrangement\textsuperscript{27} mounted on a rotation stage for period variation. There is no $z$-dependence to an IL exposure pattern, which is limited only by the laser coherence length and beam overlaps\textsuperscript{28}. The 1-D nanoscale patterns were first formed in the photoresist followed by pattern transfer onto the underlying substrate using RIE in a parallel plate reactor using SF$_6$ plasma chemistry. Figure 1 shows a scanning electron microscope (SEM) cross-sectional image of an array of nano-wall structures with a remaining layer of patterned photoresist after RIE has been performed. Note at this stage these structures are merely the precursors to the thin Si wall structures that are then reconfigured into metal-semiconductor-metal (MSM) devices. After the photoresist was removed, the wall structures are thermally oxidized. The oxidation process accomplished two things. First, it consumes the Si, thus thins the wall width. Secondly, the thermally grown oxide preserves a low defect, clean Si/SiO$_2$ interface, and at the same time passivates the surfaces of the nanostructures.\textsuperscript{23,29} The Si/SiO$_2$ interface has low defects and it is important to note that strain is present at the interface and it reduces with distance from the interface. This reduction in strain as a function of depth has been seen experimentally in Si/SiO$_2$ interfaces using a scanning transmission electron microscope using Z-contrast imaging which produces strain contrast imaging\textsuperscript{30}. Using this technique, the $1/e$ decay length was measured at approximately 1 nm. The modeling of the thermal oxidation parameters needed for the desired thicknesses was complicated due to the fact that in a three dimensional wall structure there are several crystal lattice orientations that have different thermal oxidation rates. As
a first order approximation, we used average values of oxidation rates between the various lattice orientations \textit{i.e.} oxygen ow rate, pressure, temperature and time. These parameters were then fine-tuned empirically during the actual thermal oxidation runs. Figure 2(a)-2(c) show SEM images of the cross-sectional views of the wall structures after the respective thermal oxidations. As can be seen from the SEM images, due to the high aspect ratio of these structures the oxidation rate was not fully uniform throughout the height of the walls. The rate was faster at the top part of the walls and slower at the bottom part due to higher availability of oxygen atoms in the upper regions. The resulting wall-like Si structures surrounded by the thermally grown oxide are then configured into the active region of the MSM devices as described in the next section.

C. MSM device fabrication

The wall structured samples were then configured into two terminal metal-Si/nanowall-metal (MSM) devices for optical and electrical characterization. The MSM device configuration was specifically designed so the current would ow within the wall boundaries between the electrodes. This allowed the physical cross-section of the wall structures to dictate the current ow properties. The mesa structures were fabricated to cutoff any stray current paths that could bypass the intended active region (wall) carrier path. Figure 3(a) shows a SEM picture of a typical pre-device mesa structure. After the walls were oxidized to achieve the desired wall width, the thermally grown oxide was selectively removed from the planar un-textured Si pad locations [Figure 3(b)] using an appropriate photo-mask and a chemical 1:6 buffered oxide etch (BOE) process.

Following the resist removal the samples were cleaned using a sulfuric-acid/hydrogen-peroxide solution, and a DI water rinse followed by a nitrogen gas dry step. The samples were then re-patterned using photoresist and a second mask was used in the process to form the electrode contact regions. Three separate evaporations (30 nm of Ni) were performed. The first one was performed at a normal incidence to the sample surface and the other two at a 30° degree tilt angles in order to ensure complete coverage of the mesa step height. After Ni evaporation, liftoff was performed to remove the unwanted metal and resist using acetone. Following a thorough clean using methanol/DI-water, the samples were again dehydrated and spin-coated with a thick resist layer. The samples were patterned using a
final metallization mask set. A layer of Cr and Au was evaporated on the electrode regions. 30 nm/200 nm of Cr/Au were evaporated and liftoff process was used to remove the resist and unwanted metal. Figure 3(c) shows SEM pictures of a fully fabricated wall device.

III. ELECTRICAL AND OPTICAL MEASUREMENTS AND ANALYSIS

A. DC measurements

At room temperature only a small number of carriers are thermally generated (as dark current) for a Si bandgap of 1.15 eV. At low bias voltages (linear region of operation) the slope of the $I-V$ dark current is proportional to the device resistance that includes contributions of thermally generated carriers from both the wall channels and the metal/semiconductor contact regions. At higher biases the current saturates when all thermally generated carriers are collected. Any further increase in the current can be attributed to leakages across the contact metal-semiconductor barrier and to non-linear generation of carriers across the barrier. The back interpolation of this leakage current to the zero bias (0 V) is a measure of the saturated dark current ($I_{ds}$). Although the photocurrents are a few orders of magnitude larger than the thermally generated dark currents, the analysis of the photocurrent ($I_{ps}$) $IV$ function is the same as the dark current ($I_{ds}$) $IV$ plots. For dc response analysis, two sets of measurements were performed. These include: (i) dark currents as a function of wall width thickness, and (ii) photocurrents as a function of wall width thickness. These results are discussed and analyzed below.

B. Dark currents versus wall width thickness

To study the carrier conduction properties versus dimensionally scaling down the width of the wall structures into the nano-regime, the samples were characterized in batches. Using samples with wall widths of 200 nm, 95 nm, 75 nm, 40 nm, and 20 nm, the room temperature dark currents were measured with a probe station and digital $I-V$ curve tracer. As the physical cross-sectional area of the wall widths was reduced from 200 nm to 20 nm, we know from Ohm’s law, the resistance should increase linearly as a function of area. In other words the resistivity in units of Ω/□ should remain constant. However, as can be seen from the Figure 4, the resistivity is not constant but drops significantly as the width of the wall is
reduced below 95 nm. This suggests that there is an increase in conductivity as the wall thickness decreases from 95 nm to 20 nm. Since the number of thermally generated carriers is directly proportional to the volume of the active region, any increase in the conductivity, as wall width cross-sectional region decreases from 95 nm to 20 nm, cannot be attributed to the volume of the semiconductor material, but must be the result of a substantial increase in the carrier velocity. Confirmation of this hypothesized mechanism was obtained with the use of transient time analysis as discussed in subsection III D.

C. Photocurrents versus wall width thickness

DC steady state photocurrents were measured using a 365 nm wavelength, 1.132 W/cm² argon-ion laser and a 633 nm wavelength, 3.96 W/cm² HeNe laser. The laser beam spot diameter was less than 8 µm and was focused within the active region of the electrode spacing covering several wall structures. By using 365 nm and 633 nm wavelengths, a more complete insight into absorption and carrier transport as a function of wall thickness can be achieved. At 365 nm, absorption occurs within the top first 10 nm of the Si wall structures with heights of 1500 nm. For 633 nm the total photon absorption extends through the entire wall height. Figure 5(a) and 5(b) show the conductivity versus wall thickness profiles respectively. As can be noted from the figures, a peak in the conductivity occurs around the 40 nm (physical wall width) samples followed by a decrease around 25 nm width samples. The significance of this can be explained through the effects of strain inside the wall structures that affect the carriers mobilities as the dimensions are reduced, as discussed in section IV.

D. Transient time response measurements and analysis

The schematic of the pulsed carrier transport experiment is shown in Figure 6. This setup is based on a modified version of the Haynes-Schockley experiment. This measurement provides an unambiguous direct measure of the actual transit time of electrons and holes through the channel. When a narrow pulse of light strikes the wall structured active region of the device near the left electrode as shown in Figure 6, equal number of electrons and holes are generated, and are then subjected to diffusion and drift forces in a presence of an electric field. Based on the experimental configuration the electrons will be rapidly collected
near the positively biased electrode and the holes will have to travel the entire channel to the negatively biased electrode. From the measured time response signal profile at the opposite electrode, the hole transient time limited carrier velocity can be determined, provided the carrier lifetime is greater than the total transit time. If the optical pulse of light strikes near the opposite electrode, the holes will be rapidly collected and the electrons would have to transit through the channel, thus the measured signal at the opposite electrode would be electron transit time limited.

The pulsed response measurements were taken using a 150-fs duration excitation at $\lambda = 400$ nm from a cw mode-locked Ti:Al$_2$O$_3$ laser (doubled for the short wavelength, 0.2 mW average power at a 77 MHz repetition rate).

The wall structured MSM devices were probe tested using an 18 GHz probe and a high-speed digital sampling oscilloscope with an approximately 1 ps resolution capability. The laser spot size was 1 $\mu$m in diameter and the electrode gaps were 8 $\mu$m. Normal incidence was used for the experiment. The time response measurements were taken for low electric field strengths $3 \times 10^3$V/cm, (2.5 V across 8 $\mu$m gap) thus avoiding velocity saturation.

Before the experimental data and analysis is provided it is useful to review the three primary factors that can impact the carrier transport through a semiconductor region. These factors are:

- Field dependent velocity of carriers through the active region. At high $E$-fields, the velocities of both electrons and holes in Si saturate at about $1 \times 10^7$ cm/s, provided the field within the electrodes exceeds the saturation value for most of its length, we can assume that the carriers move with a average velocity drift. Velocity saturation is not an issue in our experiment since the applied field is much lower than what is required for saturation.

- Diffusion of carriers in the active region. The time it takes for carriers to diffuse a distance $d$ is $\tau_{\text{diff}} = d^2/2D$ where $D$ is the carrier diffusion coefficient. The diffusion of carriers becomes a two dimensional process as the thickness of the Si wall-structures is reduced and carriers are physically constricted in movement by the Si/SiO$_2$ interfaces from all sides.
Junction and parasitic capacitance effects. A metal-semiconductor junction under reverse bias exhibits a voltage-dependent capacitance caused by the variation in stored charge at the junction represented by the relation \( C_J = \frac{A}{2} \sqrt{2\varepsilon \varepsilon_0 \varepsilon r N_d / V} \), where \( A \) is the junction cross-sectional area, \( N_d \) is the ionized donor density, \( \varepsilon_r \) is the dielectric constant and \( V \) is the junction voltage. This capacitance is usually quite small for MSM device structures as a result of their planar electrode design. There are also parasitic circuit capacitances associated with the probing and cabling that usually dominate the electrical response as well as the limiting response of the electronics. For this study all film devices have an identical circuit limitation.

Figure 6 shows the bias polarity of our experiment in which the left electrode polarity is positive and the right electrode is ground. With this bias configuration once a pulse of light with a spot size < 1 µm, as in the case of our experiment, strikes within the active region, the holes travel towards the right electrode and the electrons travel in the opposite direction towards the left electrode. Figure 7(a)-7(d) shows the experimental results of the time response measurements for 200 nm, 95 nm, 40 nm and 20 nm thick wall devices for both electron and hole dominated signals. From a first pass, as can be seen from these plots, as the thickness of the wall-channels are decreased, the time response signal decays faster. In particular in the case of the 40 nm and 20 nm thick walls the signal decays over an order of magnitude faster then the 200 nm sample for both electrons and holes. The rise time of the signals is an important parameter, since it directly provides the carrier transit time. The rise time \( t_d \) is defined as is the time-lapse from moment when the pulse of light strikes one end of the active region of the MSM, near one electrode, and the moment when the photo-generated carrier signal is detected at the opposite electrode. From the rise time data, provided on Fig. 7(a)-7(d), we can determine the carrier mobilities as a function of wall thickness as follows.

First from the experimental time response measurements we can calculate the average carrier velocities by applying the given relation,

\[
 v_{\text{Carrier-Velocity}} = \frac{\text{(Electrode gap)}}{t_d} \quad \text{(cm/s)},
\]

where \( t_d \) is the average time it takes for the pulsed carrier signal to cross the electrode gap distance. The pulse travels in the presence of a field and expands from its originating point.
due to diffusion. In this case we are ignoring the RC time delay that the pulsed signal experiences once it reaches the edge of the depletion region near the electrodes since the widths of the depletion regions are very small in the sub-micron range compared to the electrode gap which is 8 µm in length.

By definition the average carrier mobility can be written as,

\[ \mu_{\text{avg}} = \frac{v_{\text{Carrier-Velocity}}}{V_{\text{bias}}/(\text{Electrode gap})}, \]

where \( V_{\text{bias}} \) is the external bias applied to the electrodes.

Figure 8 shows a plot of average field dependent electron and hole limited mobility values using experimental values of rise time, \( t_d \), and the above expression as a function of wall thickness. We know that the carrier transport of electrons and holes in the thickest wall sample (200 nm) is essentially similar to the transport properties in bulk silicon. However we observe a considerable increase in low field dependent mobility values below 75 nm wall thicknesses. Recall the fact that we actually have a much narrower effective cross-sectional regions from which carriers propagate due to the repulsive nature of the boundary at the Si/SiO\(_2\) interface, and the carrier profile tends to peak a certain distance away from the interface close to the center of the wall structures. At these nanoscales we must account for the strain effects, which include the reversal splitting of light- and heavy- hole bands as well as the decrease of conduction-band effective mass by reduced Si bandgap energy. These strain effects are formulated in our microscopic model for explaining the experimentally observed enhancements in both conduction- and valence-band mobilities with reduced Si wall thickness, i.e. consider the case where the hole mobility is given by \( \mu_h = e\tau_h/m^*_h \), where \( 1/m^*_{ij} = (1/h^2) (\partial^2 E(k)/\partial k_i \partial k_j) \). The narrower light-hole band dominating the transport can have a significant enhancement on the overall mobility which is consistent with our experimental result. Specifically, the enhancements of the valence-band and conduction-band mobilities are found to be associated with different aspects of physical mechanisms. The role of the biaxial strain buffering depth is elucidated and its importance to the scaling relations of wall-thickness is reproduced theoretically. A detailed theoretical model is described in the next section which explains our experimental results in a comprehensive manner.
IV. STRAIN EFFECTS MODELING TO EXPLAIN THE RISE IN ELECTRON AND HOLE MOBILITY

Figures 9(a)-9(c) represent the thickest wall channels and Figures 10(a)-10(c) represent the thinnest wall channels. Note that the associated E-k diagrams of Fig. 9(c) and Fig. 10(c) represent the center regions of the wall channel structures where the carriers flow through.

If we consider a total valence-band hole concentration \( n_v \) then, the light-hole (\( n_{LH} \)) and the heavy-hole (\( n_{HH} \)) concentration will satisfy the charge-conservation relation

\[
 n_{LH} + n_{HH} = n_v
\]

where

\[
 n_\sigma = \frac{g_T g_s}{V} \sum_k \left[ 1 + \exp \left( \frac{E_k^\sigma \mp \Delta E_{str}^v}{k_B T} - u_v \right) \right]^{-1}
\]

\[
 \approx 2 g_T \left( \frac{m^*_\sigma k_B T}{2\pi \hbar^2} \right)^{3/2} \exp \left( \frac{u_v \pm \Delta E_{str}^v}{k_B T} \right).
\]

(3)

Here, the subscript \( \sigma \) takes HH or LH and the upper (lower) sign corresponds to HH (LH) state. In the above expressions, the approximations are made for high temperatures, \( V \) is the volume of the silicon film, \( T \) is the system temperature, the zero energy is chosen at the middle point between the split pair of light-hole and heavy-hole bands, \( k \) is the three dimensional wave vector of carriers, \( g_T = 2 \) (not 6 due to strain effect) is the \( \Gamma \)-valley degeneracy for holes and \( g_s = 2 \) is the spin degeneracy for both light-holes and heavy-holes. In addition, \( u_v \), which depends on both \( T \) and \( n_v \), is the chemical potential to be determined for valence bands, \( E_{kHH}^v = \hbar^2 k^2/2m_{HH}^* \) is the kinetic energy of heavy holes and \( E_{kLH}^v = \hbar^2 k^2/2m_{LH}^* \) is the kinetic energy of light holes, where \( m_{HH}^* = 0.49 m_0 \) and \( m_{LH}^* = 0.16 m_0 \) (\( m_0 \) is the free-electron mass) are the effective masses for heavy holes and light holes, respectively. Additionally, \( \Delta E_{str}^v \) introduced in the above expressions stands for the half of the valence-band splitting due to the existence of strain.

From Eq. (3) and \( n_{LH} + n_{HH} = n_v \), we obtain

\[
 n_{LH}/n_v = [1 + \gamma^{3/2} \exp(2\Delta E_{str}^v/k_B T)]^{-1}
\]

and

\[
 n_{HH}/n_v = 1 - n_{LH}/n_v, \quad \text{where} \quad \gamma = m_{HH}^*/m_{LH}^* > 1.
\]

For biaxial and shear strains\(^{33,34}\), we have the valence-band splitting, given by

\[
 \Delta E_{str}^v = \pm \left\{ \left( \frac{b^2}{2} \right) \left[ (\epsilon_{xx} - \epsilon_{yy})^2 + (\epsilon_{yy} - \epsilon_{zz})^2 + (\epsilon_{zz} - \epsilon_{xx})^2 \right] + d^2 \left[ \epsilon_{xy}^2 + \epsilon_{yz}^2 + \epsilon_{xz}^2 \right] \right\}^{1/2},
\]

where the upper sign is for the compressive strain while the lower sign for the tensile strain in the direction perpendicular to the interface of silicon and silicon-dioxide materials, \( b \) and \( d \) are the optical
deformation potentials, and $\epsilon_{jj'}$ represents the strain tensor in the three dimensional space with $j, j' = x, y,$ and $z,$ the diagonal matrix elements $\epsilon_{jj}$ are associated with biaxial strain, and the off-diagonal matrix elements $\epsilon_{jj'}$ with $j \neq j'$ correspond to contributions from the shear strain. For silicon crystals, we have $b = -2.33 \text{ eV}$ and $d = -4.75 \text{ eV}$.

If we choose the $z$ direction as the direction perpendicular to the interface for biaxial strain we simply get $\epsilon_{xx} = \epsilon_{yy} = \epsilon_\parallel, \epsilon_{zz} = \epsilon_\perp,$ and $\epsilon_{ij} = 0$ for $i \neq j,$ where $\epsilon_\parallel = (a_{\parallel, \text{ Si}}/a_{\text{ Si}} - 1),$ $\epsilon_\perp = (a_{\perp, \text{ Si}}/a_{\text{ Si}} - 1).$ Moreover, the perpendicular lattice constant $a_{\perp, \text{ Si}}$ is related to the parallel lattice constant $a_{\parallel, \text{ Si}} = a_{\text{ SiO}_2}$ by $a_{\perp, \text{ Si}} = a_{\text{ Si}} [1 - (2c_{12}/c_{11}) (a_{\text{ SiO}_2}/a_{\text{ Si}} - 1)],$ where $c_{11} = 16.75 \times 10^{10} \text{ N/m}^2,$ and $c_{12} = 6.5 \times 10^{10} \text{ N/m}^2$ are the elastic constants of silicon. For silicon and silicon-dioxide, we have $a_{\text{ SiO}_2} = (2 \times 4.914 + 5.405)/3 = 5.078 \text{ Å}$ and $a_{\text{ Si}} = 5.431 \text{ Å}$ for amorphous silicon-dioxide materials. Therefore, we obtain $a_{\perp, \text{ Si}}/a_{\text{ Si}} = 1.050.$ This leads to $\epsilon_\parallel = -0.065$ (compressive), $\epsilon_\perp = 0.05$ (tensile), and $2\epsilon_\parallel + \epsilon_\perp = -0.08.$

The total mobility $\mu_\nu$ for holes can be expressed as

$$\frac{\mu_\nu}{\mu_\nu^{(0)}} \approx \eta_\nu \mathcal{F}_\nu \left( \frac{L}{\lambda_\nu} \right) \frac{(1 + \gamma^{3/2})(\gamma^\alpha + \gamma^{1/2} e^A)}{(1 + \gamma^{3/2} e^A)(\gamma^\alpha + \gamma^{1/2})} + (1 - \eta_\nu), \quad (4)$$

where $\mathcal{A} = 2\Delta E_{\text{str}}^\nu/k_B T$ and $\tau_{\text{ LH}}/\tau_{\text{ HH}} = \gamma^\alpha$ (for details of calculating hole scattering time, see Appendix A). $\mathcal{F}_\nu(L/\lambda_\nu) = 1 + (Q_\nu - 1)/\sqrt{1 + (L/\lambda_\nu)^2}$ comes from the mobility saturation effect, $\lambda_\nu \sim \sqrt{3\pi^2 \hbar^2/2m_{\text{ LH}}^* k_B T}$ is the quasi-quantum confinement width, $\mu_\nu^{(0)} = [(e\tau_{\text{ LH}}/m_{\text{ LH}}^*) + \gamma^{3/2} (e\tau_{\text{ HH}}/m_{\text{ HH}}^*)]/(1 + \gamma^{3/2})$ corresponds to the hole mobility in the absence of strain for $L/\lambda_\nu \gg 1,$ $\tau_{\text{ LH}}$ and $\tau_{\text{ HH}}$ are the scattering times for light holes and heavy holes, respectively. Moreover, the factor $Q_\nu$ introduced in the definition of $\mathcal{F}_\nu(L/\lambda_\nu)$ is given by $Q_\nu = (\mu_{\nu}^{\text{ max}}/\mu_\nu^{(0)})(1 + \gamma^{3/2} e^A)(\gamma^\alpha + \gamma^{1/2})/[(1 + \gamma^{3/2})(\gamma^\alpha + \gamma^{1/2} e^A)],$ where $\mu_{\nu}^{\text{ max}}$ is the maximum of the hole mobility in the limit of $L/\lambda_\nu \to 0.$ It is clear that $\mu_\nu$ increases with decreasing $L$ for the tensile strain ($E_{\text{str}}^\nu < 0$) in the direction perpendicular to the interface of silicon and silicon-dioxide materials, as observed by us in Fig.11.

The values of $\eta_\nu$ introduced in Eq. (4) can be scaled as $\eta_\nu = 1/\sqrt{1 + (L/2D_\nu)^2},$ where $L$ is the film thickness and $2D_\nu/L$ represents the average spatially-dependent strain due to lattice mismatch between embedded Si crystal and surrounding amorphous SiO$_2$ material at their interface, and $L - 2D_\nu > 0$ represents the film effective thickness for unstrain part. The scale of interest for these calculations of the effects of strain near a Si/SiO$_2$ interface of a silicon nanowire was studied using molecular dynamics by Ohta, et. al. In this study,
strain was most pronounced within 1-2 nanometers of the interface, tensile in the [001] direction (perpendicular to the substrate) and compressive in the [110] direction parallel to the substrate resulting in form of biaxial strain.

For a given conduction-band electron concentration \( n_c \), the electron chemical potential \( u_c \), which depends on both \( T \) and \( n_c \), is decided from

\[
n_c = \sum_{\xi=X,L} n_\xi = \frac{g_\xi}{V} \sum_{\xi=X,L} g_\xi \sum_k \left[ 1 + \exp \left( \frac{E_k + E_G^\xi - u_c}{k_B T} \right) \right]^{-1}
\]

\[
\approx 2 \sum_{\xi=X,L} g_\xi \left( \frac{m^*_\xi k_B T}{2\pi\hbar^2} \right)^{3/2} \exp \left( \frac{u_c - E_G^\xi}{k_B T} \right), \quad (5)
\]

where the high-temperature approximation is made in the above expression, \( E_G^\xi = \varepsilon_G^\xi(T) + \Delta E_G^\xi \) is the bandgap energy of strained silicon crystals, which depends on \( T \) and the hydrostatic part of the strain, \( \varepsilon_G^\xi \) stands for the bandgap energy of unstrained silicon crystals, \( g_{X,L} = 2 \) (not 6 due to strain effect) represents the \( X \) (in \( <100> \) direction) or \( L \) (in \( <111> \) direction) valley degeneracy for electrons at the two minima of conduction band, \( E_k^\xi = \hbar^2 k^2 / 2m^*_\xi \) is the kinetic energy of electrons and \( m^*_\xi \) is the transverse effective mass of conduction-band electrons with \( m^*_X = 0.19 m_0 \) and \( m^*_L = 0.1 m_0 \).

The \( T \) dependence of \( \varepsilon_G^\xi(T) \) (based on the Bose-Einstein phonon model) is given by

\[
\varepsilon_G^\xi(T) = \varepsilon_G^\xi(0) - 2\alpha_B \Theta_B \left[ \coth(\Theta_B / 2T) - 1 \right], \quad \alpha_B = 2.82 \times 10^{-4} \text{eV/K}
\]

\( k_B \Theta_B \) is a typical phonon energy with \( \Theta_B = 351 \text{K} \), \( \varepsilon_G^X(T) = 1.12 \text{eV} \) and \( \varepsilon_G^L(T) = 2.4 \text{eV} \) at \( T = 300 \text{K} \) for the X and L valleys. Moreover, the strain part of the bandgap energy \( \Delta E_G^\xi \) is calculated as

\[
\Delta E_G^\xi = \Xi^{(X,L)} - \Xi^{(X)} + \Xi^{(L)} \cdot \hat{e}_{\xi} \cdot \hat{e}_{\xi} + a \cdot T \cdot \langle \hat{e} \rangle,
\]

where \( \Xi^{(X,L)} \) and \( \Xi^{(X)} \) are the deformation potentials of the conduction band for an indirect-gap silicon crystal \( (\Xi^{(X)} = 1.1 \text{eV} \) for the X valley and \( \Xi^{(L)} = -7.0 \text{eV} \) for the L valley), \( a = 2.1 \text{eV} \) is the difference of the deformation potentials of conduction and valence bands at two different valleys due to hydrostatic component of the strain for the silicon crystal, and \( \hat{e}_{\xi} \) is the unit vector pointing to the specific X or L valley. It is clear from the above equation that \( \Delta E_G^\xi < 0 \) for the tensile strain and \( \xi = X \) or \( L \).

The change in the bandgap energy by strain also affects the effective mass of conduction band, given by.

\[15\]
\[ \Delta \left( \frac{m_0}{m^*} \right) \approx -\frac{E_P(2\epsilon_\parallel + \epsilon_\perp)}{\varepsilon_G(T) + \Delta_0/3} \left[ 2 + \frac{3\alpha}{\varepsilon_G(T) + \Delta_0/3} \right], \]  
where we have neglected the shear strain and assumed a weak strain with \(|2\epsilon_\parallel + \epsilon_\perp| \ll 1\), \(\Delta_0 = 44\, \text{meV}\) is the spin-orbit splitting and \(E_P = 21.6\, \text{eV}\) is the Kane energy parameter.

The total mobility \(\mu_c\) of conduction-band electrons is obtained as

\[ \frac{\mu_c}{\mu_c^{(0)}} \approx \eta_c \mathcal{F}_c \left( \frac{L}{\lambda_c} \right) \frac{[m_0/m_X^* + \Delta(m_0/m_X^*)]^{1+\alpha}}{(m_0/m_X^*)^{1+\alpha}} + (1 - \eta_c), \] 
where \(\mathcal{F}_c(L/\lambda_c) = 1 + (Q_c - 1)/\sqrt{1 + (L/\lambda_c)^2}\) comes from the mobility saturation effect, \(\lambda_c \sim \sqrt{3\pi^2\hbar^2/2m_X^*k_B T}\), \(Q_c = (\mu_c^{\text{max}}/\mu_c^{(0)})(m_0/m_X^*)^{1+\alpha}/[m_0/m_X^* + \Delta(m_0/m_X^*)]^{1+\alpha}\), \(\mu_c^{(0)} = e\tau_X/m_X^*\) corresponds to the electron mobility in the absence of strain for \(L/\lambda_c \gg 1\), \(\tau_X,\lambda\) represents the scattering times of conduction-band electrons at two different valleys and the high-energy \(L\) valley has been assumed depopulated, and \(\tau_X = \tau_X^0 (m_0/m_X^*)^\alpha\) (for details of calculating electron scattering time, see Appendix A). In addition, \(\eta_c\) for electrons has the similar meaning of \(\eta_v\) for holes. It is clear that the electron mobility is increased for \((2\epsilon_\parallel + \epsilon_\perp) = -0.08\), as observed by us in Fig. 11.

Our numerically calculated results for electron \((\mu_c)\) and hole \((\mu_c)\) mobilities are presented in Fig. 11 along with their comparisons with our experimental data. In our model calculations, we have taken \(T = 300\, \text{K}\) and the other model parameters can be found from Tables I and II. The good agreement between our numerical calculated results and measured data strongly support the physical modeling present in this section.

V. SUMMARY AND CONCLUSION

The semiconductor processing, fabrication and the resulting carrier transport characteristics of MSM devices fabricated as wall like structures in silicon on insulator technology were reported. MSM device dark current, DC photocurrents, and the time response of carrier transport were investigated. The resulting conducting channels were actually smaller than their physical dimensions, a result of depletion of carrier near the interfaces. As the physical channel widths were reduced by oxidation, strain was produced near the interface and strained lattice became a significant portion of the conducting channel. The increase in mobilities for both holes and electrons stemming from the strained silicon resulted in a
dramatic increase in carrier mobility for both electrons and holes as the physical channel width was reduced from 200 nm to 20 nm. The theoretical model incorporating the effects of strain present in these nanoscale MSM devices compared favorably with experimental results, showing that hole mobilities increased with decreasing $L$. Additionally, if these electron and hole mobilities can be retained with the application of gate electrodes, then this technique may yield a much simpler path towards high performance CMOS, both $n$-channel and $p$-channel, than current techniques for either planer ultra-thin body FETs or FinFETs.

**Acknowledgments**

The authors would like to acknowledge the Air Force Research Laboratory, Space Vehicles Directorate for their support and interest in this work.

**Appendix A: Carrier Scattering Time**

In general, the carrier concentration includes both the doping and photo-excitation contributions. If the sample is undoped, we can simply neglect the impurity scattering and have $n_c = n_v$. The optical-phonon scattering and the inter-valley scattering are only important at high temperatures, while the acoustic-phonon scattering becomes more important at low temperatures. The surface-roughness scattering, on the other hand, is largely independent of temperature.

For the impurity scattering, by using the Fermi’s golden rule, its scattering rate $1/\tau_{\text{imp}}$ is calculated as

\[
\frac{1}{\tau_{\text{imp}}} = \frac{2}{N_c} \sum_k \frac{n_k}{\tau_{\text{imp}}(k)} = \frac{2}{N_c} \sum_k n_k \left[ N_i \frac{2\pi}{\hbar} \sum_q \left| \frac{-Ze^2}{\epsilon_0 \epsilon_r (q^2 + Q_s^2)} \right|^2 (1 - n_{k+q}) \delta(E_{k+q} - E_k) \right]
\]

\[
\approx n_i Z^2 e^4 m^* \frac{2}{N_c} \sum_k n_k \frac{Q_s^2}{k(4k^2 + Q_s^2)^2},
\]

where $N_c$ is the total number of carriers in the system, $n_i = N_i/V$ is the impurity concentration, $Z$ is the impurity charge number, $\epsilon_r = 11.9$ is the silicon dielectric constant, $Q_s^2 = (e^2 n_c / \epsilon_0 \epsilon_r k_B T)$ at high temperatures with $n_c = N_c/V$, $E_k = \hbar^2 k^2 / 2m^*$ is the carrier
kinetic energy, and \( m^* \) stands for the carrier effective mass. For this case, we have \( \alpha = 1 \).

In addition, at high temperatures we get conduction-band electron distribution

\[
n_c^\alpha = \frac{1}{1 + \exp[(E_k - u_c)/k_B T]} \approx \frac{n_c}{2g_\infty} \left( \frac{2\pi \hbar^2}{m^* k_B T} \right)^{3/2} \exp \left( -\frac{E_k}{k_B T} \right), \tag{A2}\]

where we have assumed the high-energy \( L \) valley becomes depopulated. Similar results can be obtained for valence-band hole distributions.

For the longitudinal-acoustic-phonon scattering at high temperatures (\( \hbar \omega_q \ll k_B T \)), its scattering rate \( 1/\tau_{ac} \) is calculated as \(^{[10,11]}\)

\[
\frac{1}{\tau_{ac}} = \frac{2}{N_c} \sum_k \frac{n_k}{\tau_{ac}(k)} = \frac{2}{N_c} \sum_k n_k \left\{ \frac{2\pi}{\hbar} \sum_q \frac{\hbar}{2\rho_0 \nu q} \left[ D_{ac}^2 q^2 + \frac{9}{32}(\hbar \omega_{14})^2 \right] \left( \frac{q^2}{\sqrt{q^2 + Q_s^2}} \right)^2 \right. \\
\times \left[ (1 - n_{k+q}) N_q \delta(E_{k+q} - E_k - \hbar \omega_q) + (1 - n_{k-q}) (N_q + 1) \delta(E_{k-q} - E_k + \hbar \omega_q) \right] \right\}
\approx \frac{2\pi D_{ac}^2 k_B T}{\rho_0 \hbar \nu_s^2} \frac{2}{N_c} \sum_k n_k g_{3D}(E_k), \tag{A3}\]

where \( g_{3D}(E) = m^*^{3/2} \sqrt{2E/\pi^2 \hbar^3} \) is the three-dimensional density of states of carriers, \( N_q \equiv N_0(\hbar \omega_q/k_B T), N_0(x) = 1/[\exp(x) - 1] \) is the Bose function for thermal-equilibrium phonons, \( \omega_q = v_s q, v_s = 9 \times 10^5 \text{ cm/s} \) is the sound velocity, \( \rho_0 = 2.33 \text{ g/cm}^3 \) is the atomic mass density, \( D_{ac} = 5.39 \text{ eV} \) is the deformation potential for acoustic phonons, and \( h_{14} \) is the piezoelectric constant neglected. For this case, we have \( \alpha = 3/2 \).

For the longitudinal-optical-phonon scattering, its scattering rate \( 1/\tau_{op} \) is calculated as \(^{[10,11]}\)

\[
\frac{1}{\tau_{op}} = \frac{2}{N_c} \sum_k \frac{n_k}{\tau_{op}(k)} = \frac{2}{N_c} \sum_k n_k \left\{ \frac{2\pi}{\hbar} \sum_q \frac{\hbar \Omega_0}{2V} \left( \frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_s} \right) \frac{e^2}{\epsilon_0(q^2 + Q_s^2)} \right. \\
\times \left[ (1 - n_{k+q}) N_{LO} \delta(E_{k+q} - E_k - \hbar \Omega_0) + (1 - n_{k-q}) (N_{LO} + 1) \delta(E_{k-q} - E_k + \hbar \Omega_0) \right] \right\}
\approx \left( \frac{D_{op}}{e \ell_{op}} \right)^2 \frac{e^2}{8\pi^2 \rho_0 \Omega_0} \frac{2}{N_c} \sum_k n_k \left[ (N_{LO} + 1) g_{3D}(E_k - \hbar \Omega_0) + N_{LO} g_{3D}(E_k + \hbar \Omega_0) \right], \tag{A4}\]

where \( N_{LO} \equiv N_0(\hbar \Omega_0/k_B T), \hbar \Omega_0 = 63 \text{ meV} \) is the energy of optical phonons, \( (D_{op}/e \ell_{op}) = 2.2 \times 10^{10} \text{ V/m} \) is the optical-polarization field. For this case, we also have \( \alpha = 3/2 \).

For the surface-roughness scattering, its scattering rate \( 1/\tau_{sr} \) is calculated as \(^{[32]}\)
\[ \frac{1}{\tau_{sr}} = \frac{2}{N_c} \sum_k n_k \frac{n_{depl}}{\tau_{sr}(k)} = \frac{m^* \Lambda^2 e^4 n_{depl}}{\hbar \epsilon_0^2 \epsilon_r^2} \left( \frac{\delta b}{L} \right)^2 \frac{2}{N_c} \sum_k n_k \frac{1}{\sqrt{1 + k^2 \Lambda^2}} \mathcal{E} \left( \frac{k \Lambda}{\sqrt{1 + k^2 \Lambda^2}} \right), \quad (A5) \]

where \( \delta b \) is the average roughness, \( \Lambda \) is the roughness spatial-correlation length in a Gaussian model, and \( \mathcal{E}(x) \) is the a complete elliptic integral. Additionally, \( (e/\epsilon_0 \epsilon_r) n_{depl} \) stands for the surface depletion-charge field, and \( n_{depl} \) is the surface depletion-charge areal densities. For this case, we have \( \alpha = 1 \).

For the inter-valley scattering, its scattering rate \( 1/\tau_{iv} \) can be calculated in a similar way for phonons, which gives

\[ \frac{1}{\tau_{iv}} = \frac{2}{N_c} \sum_{\xi} n_{\xi}^\xi \frac{n_{\xi}^\xi}{\tau_{iv}(\xi)} = \sum_{\xi, \xi'} \left( \frac{D_{\xi\xi'}}{e\ell_{\xi\xi'}} \right)^2 \frac{e^2}{8\pi^2 \rho_0 \omega_{\xi\xi'}} \frac{2}{N_c} \sum_k n_{\xi}^\xi \times \left\{ \left[ N(\omega_{\xi\xi'}) + 1 \right] g_{3D}^\xi (E_k^\xi - \Delta E_{\xi\xi'} - \hbar \omega_{\xi\xi'}) + N(\omega_{\xi\xi'}) g_{3D}^\xi (E_k^\xi - \Delta E_{\xi\xi'} + \hbar \omega_{\xi\xi'}) \right\}, \quad (A6) \]

where \( (D_{\xi\xi'}/e\ell_{\xi\xi'}) \) is the inter-valley optical-polarization field, \( N(\omega_{\xi\xi'}) \equiv N_0(\hbar \omega_{\xi\xi'}/k_B T) \), \( \omega_{\xi\xi'} = v_s |K_{\xi'} - K_{\xi}| \), and \( \Delta E_{\xi\xi'} = E_{\xi'}^\xi - E_G^\xi \). For this case, we have \( \alpha = 3/2 \).

The finite-size effect in the direction perpendicular to the silicon film becomes significant as \( \pi^2 \hbar^2 / 2m_X^* L^2 \gg k_B T \). The existence of such a quantum well modify the splitting of heavy and light holes by \( E_{HH} \rightarrow E_{HH} + \Delta_{qw}^X \) and \( E_{HH} \rightarrow E_{LH} - \Delta_{qw}^X \), where \( 2\Delta_{qw}^X \) stands for the quantum-well induced valence-band splitting, as well as \( g_T \rightarrow 1 \). It also affects the bandgap energy by \( \varepsilon_G^X(T) \rightarrow \varepsilon_G^X(T) + \Delta_{qw}^X \), as well as the density of states of carriers by \( g_{3D}(E_k) \propto \sqrt{E_k} \rightarrow g_{2D}(E_k) \propto \text{constant} \). Additionally, the coulomb potential in the momentum space is changed by \( e^2/\epsilon_0 (q^2 + Q_s^2) \mathcal{V} \rightarrow e^2/\epsilon_0 (q + Q_s) \mathcal{A} \), where \( \mathcal{A} \) is the area of the quantum well and \( 1/q_s \) is the Thomas-Fermi screening length for quantum wells. It is clear that the film quantization effect tends to reduce the strain-induced mobility enhancements of both electrons and holes.
TABLE I: Model parameters used in calculating mobility of electrons in strained Si film.

| $\mu_{c}^{\text{max}}$ (cm$^2$/V·s) | $\mu_{c}^{(0)}$ (cm$^2$/V·s) | $\lambda_{c}$ (nm) | 2$D_{c}$ (nm) |
|----------------------------------|------------------|-----------------|-----------------|
| 5500                             | 806              | 15              | 42              |

TABLE II: Model parameters used in calculating mobility of holes in strained Si film.

| $\mu_{v}^{\text{max}}$ (cm$^2$/V·s) | $\mu_{v}^{(0)}$ (cm$^2$/V·s) | $\lambda_{v}$ (nm) | 2$D_{v}$ (nm) |
|----------------------------------|------------------|-----------------|-----------------|
| 3000                             | 100              | 143             | 42              |

1 David C. Brock “Understanding Moore’s Law: Four Decades of Innovation” (Chemical Heritage Foundation, 2006).
2 G. E. More, Electron. 38, 8 (1965).
3 K. J. Kuhn, Microelectronic Engineering 88, 1044 (2011).
4 M. Bohr, IEEE Solid-State Circuits Conference-Digest of Technical Papers, 23 (2009).
5 S. Veeraraghavan and J. G. Fossum, IEEE Trans, Electron Devices 36, 522 (1989).
6 D. Hisamoto, T. Kaga and E. Takeda, IEEE Trans. Electron. Devices 38, 1419 (1991).
7 M. Rostami and K. Mohanram, IEEE Trans. Comp.-Aided Design for Integr. Circuits & Systems 30, 337 (2011).
8 H. M. Manasevit, I. S. Gergis and A. B. Jones, J. Electron. Mater. 12, 637 (1983).
9 N. Xu, B. Ho, M. Choi, V. Moroz, H. J. King Liu, IEEE Trans. Electron Devices 59, 1592 (2012).
10 M. Veshala, R. Jatooth and K. R. Reddy, Int. J. Engineer. & Innovative Technol. 2, 2277 (2013).
11 X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi and K. Asano, IEEE Trans. Electron. Devices 48, 880 (2001).
12 L. Chang, D. J. Frank, R. K. Montoye, S. J. Koester, B. L. Ji, P. W. Coteus, R. H. Dennard and W. Haensh, Proc. IEEE 98, 215 (2010).
13 S. W. Bedell, A. Khakifirooz and D. K. Sadana, MRS Bulletin 39, 131 (2014).
14 Y. Sun, S. E. Thompson and T. Nishida, J. Appl. Phys. 101, 104503 (2007).
15 David K. Ferry, Superlattices & Microstructures 27, 61 (2000).
16 N. J. Stone and H. Ahmed, Appl. Phys. Lett. 73, 2134 (1998).
S. Bhattacharya and K. P. Ghatak, “Effective Electron Mass in Low-Dimensional Semiconductors” (Springer, New York USA, 2013).

M.-C. Cheng, J. A. Smith, W. Jia, R. Coleman, IEEE Trans. Electron Devices 61, 202 (2014).

S. Wolf and R. N. Tauber, “Silicon Processing” (Vol. 1, 2nd edition Lattice Press, Sunset Beach, CA 2000).

W. Windl, M. M. Bunea, R. Stumpf, S. T. Dunham and M. P. Masquelier, Phys. Rev. Lett. 83, 4345 (1999).

W. Hansch, T. Vogelsang, R. Kircher and M. Orlowski, Solid-State Electron. 32, 839 (1989).

E. S. Yang, “Microelectronic Devices” (McGraw-Hill, Inc., 1988).

S. H. Zaidi, S. R. J. Brueck, F. M. Schellenberg, R. S. Mackay, K. Uekert and J. J. Persoff, Proc. SPIE 3048, 248 (1997).

M. Zhang, J. Z. Li, I. Adesida, and E. D. Wolf, J. Vac. Sci. Technol. B 1, 1037 (1983).

A. J. van Roosmalen, J. A. G. Baggerman and S. J. H. Brader, “Dry Etching for VLSI” (Springer Science & Business Media LLC, 1991).

X. Chen and S. R. J. Brueck, J. Vac. Sci. Technol. B 16, 3392 (1998).

A. J. Bourdillon, C. B. Boothroyd, J. R. Kong and Y. Vladimirsky, J. Phys. D: Appl. Phys. 33, 2133 (2000).

S. H. Zaidi and S. R. J. Brueck, J. Vac. Sci. Technol. B 11, 653 (1993).

S. Alexandrova, A. Szekeres and E. Halova, IOP Conf. Ser.: Mater. Sci. Eng. 15, 012037 (2010).

G. Duscher, S. J. Pennycook, N. D. Browning, R. Rupangudi, T. Takoudis, H-J Gao and R. Singh, AIP Conf. Proc. 449, 191 (1998).

S. Vitkavage, E. A. Irene and H. Z. Massoud, J. Appl. Phys. 68, 5262 (1990).

J. R. Haynes and W. Shockley. Phys. Rev. 81, 835 (1951).

M. Grundmann, “The Physics of Semiconductors” (2nd ed., Springer-Verlag, Berlin Heidelberg, 2010).

T. B. Bahder, Phys. Rev. B 41, 11922 (1990).

F. Schäffler, Semicond. Sci. Technol. 12, 1515 (1997).

E. G. Barbagiovan, D. J. Lockwood, P. J. simpson and L. V. Goncharova, Appl. Phys. Rev. 1, 011302 (2014).

H. Ohta, T. Watanabe, and I. Ohdomari, Jpn. J. Appl. Phys. 46, 3277 (2007).

D. E. Aspnes and M. Cardona, Phys. Rev. B 17, 726 (1978).
39 M. V. Fischetti and S. E. Laux, J. Appl. Phys. 80, 2234 (1996).

40 D. H. Huang, P. M. Alsing, T. Apostolova and D. A. Cardimona, Phys. Rev. B 71, 195205 (2005).

41 G. Gumbs and D. H. Huang, “Properties of Interacting Low-Dimensional Systems” (Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim Germany, 2011).

42 T. Ando, A. B. Fowler and F. Stern, Rev. Mod. Phys. 54, 437 (1982).

43 D. H. Huang and D. A. Cardimona, Phys. Rev. A 64, 013822 (2001).
FIG. 1: Scanning electron microscope (SEM) cross-sectional image of an array of wall precursor structures with a remaining layer of patterned photo-resist after reactive ion etch process step.

FIG. 2: SEM cross-sectional images of an array of wall structures after thermal oxidation: (a) 200 nm wall structures; (b) 95 nm wall structures; (c) 40 nm wall structures.

FIG. 3: SEM image of (a) pre-oxidized Si mesa configuration with precursors to wall structures in the active region in-between planar un-textured regions where the metal contacts will be deposited; (b) Planar un-textured Si where thermally grown oxide was removed for metal contact deposition connecting walls; (c) Fully fabricated wall device with interdigitated electrodes.
FIG. 4: Plot showing resistivity characteristics as a function of down scaling the wall widths.

FIG. 5: Plots of photoconductivity characteristics as a function of down scaling the wall widths (a) for $\lambda = 365\,\text{nm}$; (b) for $\lambda = 633\,\text{nm}$.

FIG. 6: (Color online) Schematic configuration of a wall structured MSM device used for carrier time response measurements.
FIG. 7: Measured time response signals of 200 nm wall (row-1), 95 nm wall (row-2), 40 nm wall (row-3), and 20 nm wall (row-4).
FIG. 8: Carrier mobility values calculated from direct measure of rise time values as a function of wall thickness.

FIG. 9: SEM image of single 200 nm wall (left) and artists depiction of Si and O atoms shown by light and dark gray spheres, respectively (middle). In the middle panel, region-[1] is unstrained while region-[2] is strained. In thickest structures strained region is near the interfaces, but due to fixed oxide charges the current flows away in the unstrained region. The right panel shows $E$-$k$ band diagram of unstrained region-[1].
FIG. 10: SEM image of single 20 nm wall (left) and artists depiction of Si and O atoms shown by light and dark gray spheres, respectively (middle). Note unstrained region-[1] in the middle panel has vanished as strained region-[2] closed in from both sides. In thinnest structures the strain is continuous throughout the wall. The right panel displays $E-k$ band diagram of strained region-[2].

FIG. 11: (Color Online) Theoretical modeling for electron (left panel) and hole (right panel) mobilities as functions of film thickness $L$ with $\alpha = 1.0$ (red solid curves) and 1.5 (black dashed curves) and their comparisons with experimental data (black dots) in both panels.