A high-speed low side GaN e-HEMT driver with gate ringing and overshoot suppression

Jian Jin¹, Mengyuan Sun¹, Yannan Yang¹, Min Xu¹a), and David Wei Zhang¹

Abstract A new circuit architecture to drive GaN e-HEMT power device was proposed in this work, which was taped out on TSMC 0.18um BCD process and successfully tested. With the proposed driver circuit, gate voltage overshoot as well as ringing on GaN e-HEMT device has been successfully suppressed, while not sacrificing GaN e-HEMT advantage of high switching speed. The proposed GaN driver realized 1.1ns rising time, 910ps falling time, and minimum 1.8ns output pulse width with almost no gate ringing and overshoot. This technology could potentially improve the system stability and reliability when driving GaN e-HEMT power devices.

key words: GaN e-HEMT, high-speed switching, wide-bandgap power semiconductors, gate driver

Classification: Power devices and circuits

1. Introduction

Wide-bandgap (WBG) power semiconductors such as GaN e-HEMT typically has fast switching speed and high-frequency operation, high breakdown voltage, high thermal conductivity and low on-resistance [1, 2, 3, 4, 5, 6, 7, 8]. Therefore, they are gaining more and more attention nowadays. For example, high frequency operation can miniaturize the power converter and improve the power density [9, 10, 11, 12, 13, 14, 15]. Fast switching speed helps Lidar system generate nanosecond pulse, which is of vital importance for the mapping accuracy [1]. For these applications, the gate capacitor of GaN e-HEMT needs fast charging and discharging speed [26, 29]. Therefore, a specific driver is needed to provide large driving current. However, providing large driving current in a short time means high di/dt, thus causing gate ringing and overshoot due to the parasitic inductance [17, 18, 19, 20]. Exceeding the gate operating voltage range can affect the stability of the device or even damage it [14], and excessive ringing can also cause GaN devices to switch on and off by mistake (due to the low threshold voltage of GaN e-HEMT devices, usually ~1.5V) [21, 22, 23, 24, 25]. In addition, gate ringing can cause EMI problems [26, 27].

Recently, Texas Instrument has released a low side GaN e-HEMT driver-LMG1025, which can achieve rising and falling time of about 700ps and minimum output pulse width of 2.6ns with 0Ω pull-up and pull-down resistors [28]. The corresponding test waveform shows there is large gate ringing and overshoot as seen in Fig. 1 [29].

Fig. 1. Test waveform from TI LMG1025 datasheet [29].

There are two ways to solve the gate ringing and overshoot issue. One way is to use large pull-up and pull-down resistors, which can reduce di/dt but sacrifice the switching speed [26, 29]. The second method is to reduce gate parasitic inductance [28, 29]. The total gate parasitic inductance includes package inductance and PCB track inductance. Usually, the parasitic inductance from package is about 1nH [31]. Assuming that driver sinking/sourcing current is 3A, and rising/falling time of 1ns, the gate overshoot voltage can be calculated of 3V, according to Eq. (1), by considering only the influence of package parasitic inductance.

\[
V = L \times \frac{di}{dt} = 1nH \times \frac{3A}{1ns} = 3V. \tag{1}
\]

Therefore, specific technology is needed to suppress the gate ringing and overshoot.

In this work, a novel driver circuit was proposed to suppress the gate ringing and overshoot phenomenon, while maintaining nanosecond switching speed.

2. Chip circuit design and simulation results

In a traditional GaN driver circuit, pull-up and pull-down resistors are connected to the GaN e-HEMT gate to control the di/dt, as shown in Fig. 2, thus adjusting the gate ringing and overshoot [26, 29]. However, the use of pull-up and pull-down resistors increases the rise and fall time significantly.
and is not desired in certain applications where nanosecond gate pulse is needed, such as in Lidar [1].

To overcome this challenge, an architecture of self-adaptive charging and discharging GaN e-HEMT gate has been proposed, and the main circuit is illustrated in Fig. 2. VDD supply voltage and driving voltage are both 5V. ‘OUTH’ and ‘OUTL’ are short to GaN gate. When ‘EN’ is high, the chip starts to work. When ‘PWM’ signal is high, ‘Logic-driver’ outputs low, and power VDD charges GaN gate capacitor to VDD; when ‘PWM’ signal is low, ‘Logic-driver’ outputs high, and GaN gate is discharged.

When the GaN gate voltage is 0V, PMOS2 turns on, and the power supply VDD fastly charges the GaN gate through charging path 1 until the GaN gate voltage is approaching 5V. Then PMOS2 turns off, and the power supply VDD continues to charges the GaN gate through charging path 2, i.e., through resistor R2. Since the resistance of R2 is selected much larger than the Ron of PMOS2, it can greatly slow down di/dt, thus self-adapting the charging current to suppress the GaN gate ringing and overshoot.

Similarly, when the GaN gate voltage is 5V, NMOS2 turns on and the GaN gate is quickly discharged through discharging path 1, until the GaN gate voltage approaches 0V. This shuts NMOS2 off and the GaN gate is discharged through the discharging path 2. With careful selection of R1, the di/dt can be self-adapted to a lower level to suppress the GaN gate ringing and overshoot. Since di/dt decreases only when the GaN gate voltage is approaching 0V (falling edge) and 5V (rising edge), the switching speed will be little impacted.

The chip was designed on TSMC 0.18um BCD process. The simulation test-bench with EPC2019 (a product of EPC company) was constructed as in Fig. 3. The conventional driving circuit was also simulated for comparison. As shown in Fig. 4(a), @1MHz with 20ns pulse width input, the gate ringing and overshoot was significantly suppressed with the rising time increased from 680ps to 960ps under the gate parasitic inductance of 1nH. The falling time was almost not impacted, because the selected R1 is smaller than R2 which has been sufficient to suppress the gate ringing and overshoot.

The minimum 1.2ns (from 50% to 50%) pulse width was still achievable for the new driver system as demonstrated in Fig. 4(b) with successful suppression of gate ringing and overshoot. The detailed simulation data are summarized in Table I.

| Voltage (V) | PWM | EN | VDD | PMOS1 | NMOS1 | GaN | NMOS2 | R1 | R2 |
|------------|-----|----|-----|-------|-------|-----|-------|----|----|
| -1V-5.5V   |     |    |     |       |       |     |       |    |    |

![Fig. 3. Simulation test-bench](image)

![Fig. 4. Simulation results(The rising time Tr refers to the time required for the gate voltage to rise from 20% to 80%, and falling time Tf refers to the time required for the gate voltage to fall from 80% to 20%)](image)

### Table I. Comparison of simulation data for conventional driver and the proposed driver.

| Simulation results                  | Conventional driver with EPC2019 | Our proposed driver with EPC2019 |
|-------------------------------------|----------------------------------|----------------------------------|
| Rise Time(Tr)                       | 680ps                            | 960ps                            |
| Fall Time(Tf)                       | 683ps                            | 688ps                            |
| Gate Voltage Range                  | -4V-7.4V                         | -1V-5.5V                         |
| Whether there is wrong switch       | Yes                              | No                               |
| Minimum Pulse Width                 | 1.2ns                            | 1.2ns                            |
To check the effectiveness of our proposed circuit, we connected all gates of PMOS1, PMOS2, NMOS1, and NMOS2 to the output of Logic-Driver in the simulation test-bench as shown in Fig. 5. With 20ns pulse width input @1MHz, the comparison circuit obviously cannot suppress the gate voltage overshoot and ringing as expected in Fig. 6. Because when all gates of PMOS1, PMOS2, NMOS1, and NMOS2 were connected together, PMOS1&PMOS2 or NMOS1&NMOS2 were always turned on/off at the same time. Therefore, the GaN gate capacitor cannot be charged/discharged through the designated R2/R1 resistor thus, the gate voltage overshoot and ringing cannot be suppressed. This comparison strongly verified the effectiveness of our proposed driving circuit.

![Comparison circuit 1: Gates of PMOS1, PMOS2, NMOS1, and NMOS2 are connected to the output of Logic-Driver](image1)

**Fig. 5.** Simulation test-bench of comparison circuit with all gates of PMOS1, PMOS2, NMOS1, and NMOS2 are connected to the output of Logic-Driver

![Simulation results of GaN gate voltage for proposed driver circuit and comparison circuit](image2)

**Fig. 6.** Simulation results of GaN gate voltage for proposed driver circuit and comparison circuit

### 3. Test results

The fabricated chip photo and the designed chip test board were shown in Fig. 7 and Fig. 8. Consistent with the simulation test bench, EPC2019 GaN e-HEMT was used in the test board. The test was conducted at PWM frequency of 1MHz and 20ns pulse width @26°C. As shown in Fig. 9, the proposed driver circuit successfully suppressed the gate ringing and overshoot, making the GaN e-HEMT Vgs range almost perfectly between 0-5 V. On the other hand, the conventional driver system led to GaN e-HEMT Vgs ranging between -3.5V and 7.7V (the allowable operating range is -4.0-6.0 V), which could potentially degrades the devices’ stability and reliability [30]. The rising time of GaN e-HEMT gate was increased of 260ps, while the falling time was only slightly increased of 65ps, which is consistent with the simulation results. Comparable minimum pulse width of 1.8ns was tested for both driver circuits, which is larger than simulation due to the parasitic gate inductance, as shown in Fig. 10. The detailed test data are summarized in Table II.

As confirmed by test results, the proposed driving circuit realized high switching speed, meanwhile retained the advantage of suppress and the GaN gate voltage overshoot and ringing which was due to its large di/dt. Therefore, our driving architecture should be also suitable for steadily driving other type of power transistors to realize high-speed switching with large di/dt.

![Designed chip test board](image3)

**Fig. 8.** Designed chip test board
### 4. Conclusion

A novel driver circuit with gate ringing and overshoot suppression was proposed and taped out on TSMC 0.18um BCD process. The chip was successfully tested with perfect suppression of gate ringing and overshoot on GaN e-HEMT, with little impact on the rising/falling time and minimum pulse width. This technology may provide a promising application on driving high-speed GaN e-HEMT devices with high stability and reliability.

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