C-for-Metal: High Performance SIMD Programming on Intel GPUs

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Abstract—The SIMT execution model is commonly used for general GPU development. CUDA and OpenCL developers write scalar code that is implicitly parallelized by compiler and hardware. On Intel GPUs, however, this abstraction has profound performance implications as the underlying ISA is SIMD and important hardware capabilities cannot be fully utilized. To close this performance gap we introduce C-For-Metal (CM), an explicit SIMD programming framework designed to deliver close-to-the-metal performance on Intel GPUs. The CM programming language and its vector/matrix types provide an intuitive interface to exploit the underlying hardware features, allowing fine-grained register management, SIMD size control and cross-lane data sharing. Experimental results show that CM applications from different domains outperform the best-known SIMT-based OpenCL implementations, achieving up to 2.7x speedup on the latest Intel GPU.

Index Terms—SIMD, SIMT, GPU programming

I. INTRODUCTION

Mainstream GPU programming as exemplified by CUDA [1] and OpenCL [2] employ a “Single Instruction Multiple Threads” (SIMT) programming model. The CPU host code in an OpenCL application defines an N-dimensional computation grid where each index represents an element of execution called a “work-item”. An OpenCL kernel describes the algorithm that will be executed on GPU for one work-item. Work-items are grouped together into independent “work-groups” that execute concurrently. Work-items inside one work-group may communicate through fast on-chip shared local memory (SLM) and barrier synchronization.

OpenCL’s programming model is a powerful paradigm to express data parallelism, as developers can write purely scalar code for their kernels without knowing the details of how the work-items are mapped to the hardware execution units. This abstraction has profound performance implications, however, as the Intel GPU architecture (also called Gen) and the underlying instruction set architecture (ISA) is “Single Instruction Multiple Data” (SIMD). Intel GPUs feature an expressive instruction set that supports variable SIMD-sizes as well as powerful regioning capabilities that allow for fast cross-lane data sharing. An execution unit (EU) on Gen has a fixed number of hardware threads, and each thread executes SIMD instructions on its dedicated 4KB byte-addressable register file. The OpenCL compiler is responsible for vectorizing the kernel into one of the three SIMD sizes (8, 16, 32) for thread dispatch, and work-items execute the same instructions on one thread in lock-step. SIMD size selection is thus the most important optimization decision for the compiler, as it affects thread occupancy, instruction-level parallelism (ILP), SIMD-lane utilization due to divergence, and register spill.

A high-performance program on Gen needs to exploit a thread’s dedicated register file to cut down memory traffic while avoiding register spill, which is often fatal for performance. This can be surprisingly difficult to achieve for OpenCL programs, however, as in order to stay portable the language offers no mechanism for direct register file control. Register pressure estimate at the source level is often wildly inaccurate due to the various compiler optimizations and transformations that must happen to lower OpenCL C into Gen ISA.

Since under the SIMT model each work-item executes independently, OpenCL programs also lose control of data sharing among the cooperative items in the same thread. Furthermore, the SIMT model prevents OpenCL programs from directly accessing Gen ISA’s powerful regioning mechanisms, which allows one SIMD lane to access another lane’s data at no additional cost. The introduction of subgroups in OpenCL 2.0 partially alleviates the gaps by exposing some of the underlying hardware capabilities through builtin functions, but getting close to the metal performance with OpenCL on Intel GPUs remains challenging.

This paper presents the C-for-Metal (CM) development framework, an explicit SIMD programming model designed specifically for coding to the metal on Intel GPUs. The CM language is an extension to C/C++ that provides an intuitive interface to express explicit data-parallelism at a high level of abstraction. At the core of the language are two special vector and matrix types that form the foundation of its programming model. Vector and matrix variables are to be allocated in registers, which makes it much easier to control register usage at the source level. A CM kernel describes the algorithm for an entire hardware thread instead of a single work-item through builtin operations on vectors and matrices; of particular importance is the select operator that supports efficient register-gather of elements in a variable and is mapped directly to the Gen ISA regions. Programmers explicitly control an instruction’s SIMD size by varying the number of elements
returned in a select operation, and different SIMD sizes may be used based on considerations such as register demand and divergence.

The CM compiler (CMC) is based on the LLVM infrastructure and is responsible for generating Gen ISA SIMD instructions from the high-level vector and matrix operations. A number of CM-specific intrinsics are introduced to effectively represent such operations in the LLVM intermediate representation (IR). A sequence of CM-specific optimizations and transformations are developed around those intrinsics. One unique challenge in developing this compiler is that we need to strike a careful balance between compiler optimizations and What-You-Write-is-What-You-Get. CM kernels are fully compatible with the Intel GPU OpenCL runtime and oneAPI Level Zero and can be launched directly as if they are written in OpenCL. While Gen is CM’s native architecture, CM kernels may also be executed on CPU for debugging purposes. The CM development framework is open source and can be found in [6].

We present a comprehensive experimental evaluation of representative applications from different domains implemented in CM and OpenCL. For each workload we provide an implementation sketch on how to code to the metal on Gen using CM. We show that CM kernels achieve up to 2.7x speedup compared to the best-known OpenCL implementations that use available Intel-specific GPU extensions. The speedup offered by CM does not mean a sacrifice to productivity; while OpenCL may allow for rapid prototyping of sequential code, this advantage is often negated by the subsequent tuning efforts required to obtain good performance on GPUs. Results from the development process of several compute kernels indicate that CM provides 2-3x more productivity in terms of the development effort than OpenCL.

The rest of the paper is organized as follows: Section II briefly covers the related work; Section III discusses the main motivations of CM as an efficient SIMD programming model; Section IV describes the CM programming language; Section V describes the CM compiler; Section VI presents several applications implemented in CM and their experimental evaluation; and finally Section VII concludes this paper.

II. RELATED WORK

SIMT and SIMD are two dominant programming models that express data parallelism. CUDA [1] and OpenCL [2] are two representative SIMT programming languages. In addition to SIMT execution, OpenCL also supports a task parallel programming model in which a work-group contains a single work-item and parallelism is expressed via vector data types and multiple task enqueues. However, SIMT remains the dominant choice by far for OpenCL GPU implementations.

As OpenCL is designed to be cross-platform, it does not reflect the full architectural features for any specific hardware implementations. As a result, OpenCL is generally acknowledged to suffer from poor performance portability, and time-consuming tuning efforts including the use of non-portable vendor extensions are often mandatory to obtain good performance. Auto-tuning has long been suggested as a method to improve OpenCL’s performance portability, but given the wide disparities among the underlying hardware architecture it is unclear if such techniques can be generally applicable.

[13] presented a comprehensive performance comparison of CUDA and OpenCL and concluded that OpenCL programs can achieve similar performance to CUDA “under a fair comparison” once differences in optimization strategies and compilers are accounted for. Their study is performed on NVIDIA GPUs which employ a SIMT architecture that naturally match both CUDA and OpenCL’s execution model. In contrast, CM is designed specifically for Intel GPUs and adopts an explicit SIMD programming model to fully exploit the Gen architecture. Most implementation techniques used in our CM workloads are simply not available in the OpenCL language.

SIMD programming on the CPU is conventionally done via C-style intrinsics, but such assembly-like interface demands significant coding efforts. As a result many high level SIMD programming models for C++ have been proposed. Together they cover a wide design spectrum from implicit vectorization (e.g., OpenMP) akin to OpenCL to explicit vectorization (e.g., std::experimental::simd in C++ [15]) similar to CM. [16] provides an evaluation of several SIMD programming models against intrinsic programming. None of these SIMD programming models are natively designed for Gen, although a few such as OpenMP have been ported. More recently Intel has announced oneAPI Data Parallel C++ [17], which provides a unified, standards-based programming model for Intel architectures including CPU, GPU, FPGA, and AI accelerators. We choose OpenCL for performance comparison as it is the most common language for general-purpose GPU programming on Gen and has very mature toolchain support.

CM is inspired by C* [18] and VecImp [19]. Every statement including control flow branch in VecImp is executed in a scalar or vector context explicitly. C* declares parallel variables with shape that contain many data elements. Arithmetic operators on parallel variables perform operation on all elements of a parallel variable at the same time.

In terms of compiler infrastructure, such as LLVM, vector representations and transformations that we have explored for implementing CM are ongoing research topics. Recently, authors in [20] introduce MLIR, an extensible multi-level intermediate representation, which is aimed to “improve compilation for heterogeneous hardware, reducing the cost of building domain specific compilers”. MLIR community is actively working on a vector dialect. One rationale explained in [21] for developing this vector dialect is “higher-dimensional vectors are ubiquitous in modern HPC hardware”.

CM can also serve as a back-end compiler of other domain-specific languages aimed to tackle computationally expensive problems. Recent proposals for neural networks and image analysis provide high level of abstraction where the CM back-end compiler naturally fits in to target Intel GPU.
The CM language was invented more than ten years ago, and hundreds of CM applications have been developed inside and outside Intel. As an example in [25] and [26], authors study the extension of linearization properties to SIMD programming using CM, including the implementation of a concurrent data structure using atomic operations.

III. MOTIVATIONS FOR A NEW PROGRAMMING MODEL ON GEN

Here we describe three main challenges faced by SIMT models as represented by OpenCl on Intel GPUs to formally motivate the need for CM.

1) **Register file control**: Effective use of the register file to reduce unnecessary memory traffic is perhaps the most important optimization strategy for Intel GPUs [27]. Careful management of register pressure is difficult to achieve in OpenCL, as its language leaves the decision of register allocation entirely in the compiler’s hands. Hundreds of compiler transformation and optimization passes take place for an OpenCL kernel to be compiled into Gen assembly; most of them can have significant impact to register pressure, yet their behavior is nontransparent and usually non-controllable for the programmer. For example, divergence analysis [28] is a critical analysis for SIMT GPU compilers, and its results may be used to reduce register usage by allocating a scalar register for a variable if can prove all lanes hold identical values. The analysis results are often overly conservative in the presence of complex data and control dependencies, but offers no mechanism for the programmer to assist the analysis. By contrast, CM variables are register-allocated by default, and vectors and matrices can have arbitrary size within hardware limit. CM developers can thus directly allocate their uniform variables in one register, and they may also coalesce variables into large matrices for explicit lifetime management.

2) **Cross-lane data sharing**: A well-known limitation of the SIMT execution model is the lack of data sharing among the work-items in a hardware thread. Even though SIMD lanes in a thread share the register file, the SIMT abstraction prevents one lane from accessing another lane’s register data, and this invariably leads to redundant computation and memory operations. Both CUDA and OpenCL have introduced explicit SIMD primitives to facilitate cross-lane communications, and functionalities provided include shuffle, reduction, and barrier operations [29], [30]. These extensions help bridge the gap between the SIMT model and the underlying SIMD hardware, but they do not represent actual hardware capabilities. By contrast, CM’s select operation directly maps to hardware regioning and may be used directly in compute instructions, thus eliminating unnecessary shuffle moves.

3) **Vector length control**: Each Gen ISA instruction has its own execution size, and per-instruction SIMD size can be an important optimization technique. One immediate use of varying vector size is register pressure control. Most applications go through phases of high and low register demand, and a kernel should mix its SIMD size to avoid spills in high-pressure regions while achieving maximum bandwidth for vector memory gather/scatter operations. Similarly, branch divergence can significantly reduce a program’s efficiency [31], [32]; in the absence of hardware mechanisms, the inactive channels will not execute until control flow re-converges. By running with a lower SIMD size inside divergent regions, a kernel could reduce the amount of wasted work. Because of CM’s explicit SIMD model, programmers can easily control each instruction’s SIMD size through the size of vector and matrix selects. The SIMT model offers no such capabilities, however, as OpenCL GPU compilers perform implicit vectorization on the kernel. An OpenCL kernel may specify its dispatch size, but all non-uniform instructions will have that size by default.

We use a simple 3 by 3 box blur filter (aka linear filter) to compare and contrast CM and OpenCL’s programming models. We first show a straightforward OpenCL implementation and point out its efficiencies on Intel GPUs. In Section [V] we present the CM implementation to showcase the language’s key features, while Section [VI] explains how the CM kernel is compiled into the base ISA. In Section [VI] we evaluate the performance of our CM kernel against an optimized OpenCL kernel that uses Intel-specific extensions, and show that even this optimized version can only reach less than 50% of CM’s performance.

**Algorithm 1** Linear filter in OpenCL with SIMT model

```c
1: kernel LINEAR(image2d src, image2d dst, int width, int height)
2:   int x = get_global_id(0);
3:   int y = get_global_id(1);
4:   float4 pixel1 = 0.0f;
5:   float4 pixel = 0.0f;
6:   int tempx, tempy;
7:   #pragma unroll
8:   for i = -1; i <= 1; i++ do
9:     tempx = min(width-1, max(0, x+i));
10:    tempy = min(height-1, max(0, y+i));
11:    pixel1 = read(src, sampler, (int2)(tempx,tempy));
12:    pixel.z += pixel1.z;
13:    pixel.y += pixel1.y;
14:    pixel.x += pixel1.x;
15:   end for
16: end kernel
```

In Algorithm 1, every work-item computes the result of one pixel, whose position is indicated by the work-item’s x and y global id, by taking the average value of its neighbors...
in the input image. Intel’s OpenCL compiler vectorizes this kernel into SIMD16 instructions where each lane corresponds to one pixel in the input and output image. Both images are in 3-channel RGB format, and the hardware image read unit converts the 8-bit integer in each channel into normalized floating-point values in structure-of-array (SoA) format. The image write performs the format conversion in reverse. The generated assembly consists of 9 image-gather loads (line 11), 27 floating-point additions (line 12-14), and one image-scatter write (line 18).

This simple implementation suffers from severe redundant loads in each hardware thread, as in one iteration each work-item is reading pixel values that were already loaded in previous iterations by its adjacent lanes. A more efficient method is to have the work-items in a thread cooperatively load a 2D block of the image in raw format (i.e., the pixels are loaded into registers without format conversion), then convert each channel into floating-point values for subsequent computation. This special 2D block read/write functionality is provided by Intel’s cl_intel_media_block_io extension.

The effectiveness of this approach is still limited by the SIMT model, however, as the builtin function’s return data must be evenly distributed among the work-items in a subgroup. Thus, a subgroup shuffle operation is required to read the neighbor lanes’ pixels and convert them from array-of-structure (AoS) into SoA layout. The OpenCL compiler is generally not able to optimize away these costly moves, as to satisfy the SIMT model it must maintain the values being computed in SoA format. As a last resort one could avoid the shuffle moves by transposing the input image in host code, but this increases CPU overhead and real-world applications do not necessarily have control over their input layout.

As we will show in the next section, these issues can be easily addressed in CM. Since a CM kernel describes the algorithm for one thread, it can naturally store the data for the 2D block read/write in a matrix, and it can also choose the best matrix size without being constrained by the dispatch size. Explicit vectorization means CM developers can structure their code to accommodate the block load’s layout, and the select operations efficiently extract the sub-elements for computation. The CM compiler’s ability to break up matrix operations into variable-size Gen instructions simplifies programming efforts while maintaining high performance.

IV. CM PROGRAMMING LANGUAGE

The CM programming language is implemented using Clang and supports a subset of the standard C++ with some restrictions (more details in section 2.6 of the CM language specification [6]). Two container types, vector and matrix, are added to the Clang base type system. These new base types form the foundation for the CM explicit SIMD programming model. On top of these two types, we add operations and builtin functions that closely resemble the Gen instruction set. These new types and functions together form the abstract interface for close-to-the-metal programming on Gen. The following subsections illustrate the major features of the language. For all the details needed to write CM code, refer to the CM language specification [6].

A. Vector and Matrix Types

These types are defined using syntax similar to C++ template classes. The parameters are the type of data element and the size of a vector/matrix. Element type must be one of the basic types supported by CM and sizes must be positive integers and compile-time constants.

vector<short, 8> v; // A vector of 8 shorts
matrix<int, 4, 8> m; // A 4x8 integer matrix

Additionally, CM provides two reference component data types: vector_ref and matrix_ref. They define references to basic vector or matrix objects. No extra memory space is allocated to reference variables. For example, the second row of matrix m could be defined as a reference variable as:

vector_ref<int, 8> vref(m.row(2));

Vector or matrix variables map to a sequence of consecutive elements residing in the general register file (GRF) of the Gen hardware. A vector or matrix variable may not have its address taken; indirect access is performed via the reference types instead. Reference variables are usually constructed from operations on base variables which provide alternative views to the base objects. Reading a reference variable is mapped directly to Gen’s region based addressing scheme, which provides zero-overhead data pack, unpack, and shuffling within two registers.

For vectors, matrices, and their corresponding reference variables, CM supports member functions and operations including constructor and assignment; arithmetic, shift, logic and comparison; and row, column and element accesses. The main operations unique to CM vector and matrix types are:

- **select**: a set of select functions for referencing a subset of vector/matrix elements are supported. Each select operation returns a reference to the elements of the base object, and they can be used as l-value expressions. Select operations are of the form (with v being a vector and m a matrix):

  v.select<size,stride>(i)
  m.select<vsize,vstride,hsize,hstride>(i,j)

  In the second case, it returns a reference to the sub-matrix starting from the (i, j)-th element. vsize indicates the number of selected rows; vstride indicates the distance between two adjacent selected rows; hsize indicates the number of selected columns; and hstride indicates the distance between two adjacent selected columns. As Figure 1 shows, v.select<4, 2>(1) is an l-value expression of type vector_ref<float, 4>, which refers to odd elements in the 8-float vector v. In the case of matrix m, the example shows that the operation selects 4 elements (vsize=2, hsize=2) with vstride and hstride of 2 and 4 respectively. The initial offset is m[1, 2]. Nested vector or matrix select operations are efficiently mapped into direct register addressing operations on Gen.

- **iselect**: CM allows the user to perform indexed access into another vector. Indirect selects are always r-value
Just like in standard C++, users may want to add explicit vector<int, 8> i;
vector<float, 8> f;

conversion can be:

conversion rules. A simple example of an implicit and explicit type conversions to change the default type promotion and type promotion (using template specialization mechanisms).

source operand data types following standard C++ rules for the element type for the destination operand based on the rules for vector/matrix classes. The CM compiler determines is checked at compile time using template specialization identical number of elements. The operand shape conformance

CM also supports mixed operations of vector and matrix variables, which are treated as thread private variables. They can be used to facilitate data sharing among the main function and its callee functions in the same thread. Optionally, CM supports two variants of global variable usage. The first variant, denoted by the _GENX_VOLATILE_ qualifier, informs compiler to perform conservative optimizations on these variables in order to decrease register pressure and improve code quality. The second variant, denoted by the _GENX_VOLATILE_BINDING_(Offset) qualifier, indicates the global variable should be mapped to a GRF block starting from the specified byte offset. Such register binding feature enables programmer to achieve fine-grained register allocation control and effectively tackle other challenges such as bank conflict for performance critical applications.

B. Memory Intrinsics

CM provides a set of memory-access functions that resemble the underlying Gen hardware operations. By default a buffer-indexed based addressing mode is used. A kernel includes a number of SurfaceIndex arguments, each of which represents a handle to the underlying memory object. A read or write intrinsic takes one surface index and accesses its elements specified by the offsets. Application host code is responsible for binding each kernel argument to a memory object through runtime API calls. The most useful intrinsics include:

• 2D-block read/write: For an image identified by its SurfaceIndex, a block-read loads a block of pixels at the given x/y location into a matrix. A 2D-block write stores a matrix into a block of pixels in an image at the given x/y location. The following intrinsic definition is for 2D-block read.

    template<typename T, int N, int M>
    void read(SurfaceIndex index,
              CmBufferAttrib attr, int X, int Y,
              matrix_ref<T, N, M> output)

• Oword-block read/write: For a linearly-addressed buffer, a block-read reads a consecutive sequence of owords (16 bytes per oword) at a given offset into a vector. A block-write writes a vector into a consecutive sequence of oword at the given offset into the buffer. The following intrinsic definition is for Oword-block read.

    template<typename T, int N>
    void read(SurfaceIndex idx,
              CmBufferAttrib attr, int offset,
              vector_ref<T, N> output)

• Scattered read/write: Vector gather and scatter of various granularity are also supported. Zero-based offsets of each element (relative to a global offset) to be read/written are specified in a vector. For scattered read and write functions, the address, source payload, and return data must be vector type of the same size. The following intrinsic definition is for scattered read.

    template <typename T, int N>
    void read(SurfaceIndex index,
• **Atomics**: CM supports all native atomic operations on Gen including and, add, max, inc, compxchg, etc. Like scattered read/write, atomic functions must also have vector type. The following is the intrinsic definition for atomic inc.

```c
void write_atomic(vector<ushort, 8> mask, SurfaceIndex index, vector<uchar, N> elementOffset)
```

In addition to SurfaceIndex, CM also supports a flat addressing model where a kernel argument is a pointer that may be directly used for memory access. This allows host and kernel code to share data structures and concurrently access them.

### C. Boolean Reductions

To facilitate boolean reductions on mask vectors, CM provides two predefined boolean functions:

```c
ushort vector<ushort, size>::any(void)
ushort vector<ushort, size>::all(void)
```

*any()* returns 1 if any of the value in the mask is non-zero; it returns 0 otherwise. *all()* returns 1 if all the values in the mask are non-zero; it returns 0 otherwise. Notice that the same functions are also available for matrix types. The result of either function can be used as a scalar value and be used in the standard C++ control-flow constructs. Reduction functions are efficiently mapped to Gen’s compare instructions.

### D. SIMD Control Flow

In CM, the default control-flow statement is just the C++ scalar controlflow statements – conditional statements (if-else/switch), loop statements (for/while/do-while), jump statements (break/continue/goto/return) or function calls. For those statements, the conditions must be scalars, and all SIMD lanes branch uniformly.

Beyond that, CM also provides per-lane SIMD control-flow mechanisms utilizing the Gen `simd-goto` and `simd-join` instructions that support divergent control-flow under SIMD execution \[33\]. This feature provides an alternative to predicating long sequence of instructions, as inactive channels do not execute inside SIMD control flow regions.

SIMD control flow in CM is expressed by predefined C++ macros. For instance, a divergent *if* is represented by macros `SIMD_IF_BEGIN` and `SIMD_IF_END`, and are used as follows:

```c
vector<uchar, 16> v(0);
vector<uchar, 8> s; cond = ...
SIMD_IF_BEGIN(cond > 0){
  // ...
  v.select<2, 0>(0) = 1;
}SIMD_ELSE{
  // ...
  v.select<2, 0>(1) = 1;
}SIMD_IF_END;
```

The comparison cond > 0 produces a vector mask that determines whether a lane is active. Both the *then* statement and the *else* statement may get executed for their active lanes.

A SIMD control flow block is skipped if none of the lanes are active. Notice that the size of SIMD operations within a SIMD control-flow must be either the same size as the mask or scalar.

### E. Linear Filter in CM

We now describe how the linear filter can be implemented in CM (Algorithm \[2\]). Each thread in the CM kernel reads a 8x32-byte matrix and outputs a 6x24-byte matrix corresponding to 6x8 pixels. Although we only need 8x30 bytes for 8x10 input pixels, adding two-byte padding to each row gives a good layout in register file for computation. The select operation acts as follows: after the input pixels are loaded into the 8x32-byte matrix \(m\), at each step, we extract a 6x24-byte sub-matrix through a select operation, convert all elements into float, then add them to the running total, which is a 6x24-floating matrix. Figure 2 shows the first 6x24-byte sub-matrix select operation performed in Algorithm 2.

#### Algorithm 2 Linear filter written in CM

1: \[1\] **kernel** LINEAR(Surface inBuf, Surface outBuf, uint hpos, uint vpos)
2:   matrix<uchar, 8, 32> in; //8x32 input matrix
3:   matrix<uchar, 6, 24> out; //6x24 output matrix
4:   matrix<float, 6, 24> m;
5:   //Compute sums of neighbor elements
6:   m = in.select<6, 1, 24, 1>(1, 3);
7:   m += in.select<6, 1, 24, 1>(0, 0);
8:   m += in.select<6, 1, 24, 1>(0, 3);
9:   m += in.select<6, 1, 24, 1>(0, 6);
10:  m += in.select<6, 1, 24, 1>(1, 0);
11:  m += in.select<6, 1, 24, 1>(1, 6);
12:  m += in.select<6, 1, 24, 1>(2, 0);
13:  m += in.select<6, 1, 24, 1>(2, 3);
14:  m += in.select<6, 1, 24, 1>(2, 6);
15:  //Compute average (implicit type conversion)
16:  out = m*0.1111f;
17:  write(outBuf, hpos*24, vpos*6, out);
18: **end kernel**

![Fig. 2. Select a 6x24 sub-matrix from a 8x32 matrix](image)

m = in.select<6, 1, 24, 1>(1, 3);

The 2D-block read/write functions are used to perform the load and store on line **5** and line **18**. As mentioned in Section **III** for this filter the specialized 2D block messages are much more
efficient than the image gather/scatter operations in the vanilla OpenCL implementation (Algorithm 1) due to the elimination of redundant memory traffic.

V. CM Compiler

Like Intel Graphics Compiler (IGC) [33], the CM Compiler consists of three layers:

- **Front-end:** The clang front-end compiler [34] converts CM source code into LLVM intermediate representation (IR) [3].

- **Middle-end:** The middle-end performs generic and CM specific optimizations and transformations before converting the LLVM IR into the virtual-ISA (vISA) assembly language. The vISA is very close to Gen ISA but offers more convenience as a compilation target as it has unlimited virtual registers and hides various hardware-specific restrictions.

- **Finalizer:** The vISA finalizer [27] is a code generator for Intel GPU. Taking vISA assembly as input, it performs local optimizations, register allocation and scheduling to generate the final instructions for the target Intel GPU.

The general flow of the CM custom optimizations is illustrated in Figure 3 (inside middle-end module). The input corresponds to LLVM IR generated by LLVM generic optimizations. The lowering pass gradually converts the high-level CM language constructs to code sequences that are closer to the target Gen ISA. Afterwards, several optimizations are performed at each IR level to improve the code quality. Two of these optimization passes are highlighted in the remainder of this section: bailing and legalization and vector optimization.

The following is a simplified example to illustrate the design. The original vector `a` is defined as an $8 \times i32$ value %a0. The `rdregion` intrinsic extracts $4 \times i32$ elements from %a0 based on the given parameters: vertical stride = 0, width = 4, horizontal stride = 2, starting byte offset = 4. The `wrregion` intrinsic inserts the elements of %b to the old value of a (%a0) based on the other given parameters: vertical stride = 0, width = 4, horizontal stride = 2, starting byte offset = 0. The SSA property is maintained as the `wrregion` intrinsic returns a different %a1 to represent the new value of vector a.

```
vector<int, 8> a(init_v);
vector<int, 4> b;
b = a.select<4, 2>(1);
a.select<4, 2>(0) = b;
%a0 = <8xi32> ...
%b = call<4xi32> @llvm.genx.rdregioni...
(<8x32> %a0, i32 0, i32 4, i32 2, i16 4);
%a1 = call<8x32> @llvm.genx.wrregioni...
(<8x32> %a0, <4x32> %b, i32 0, i32 4, i32 2, i16 0);
```

Due to its expressiveness one vISA instruction may be represented in the LLVM IR by multiple instructions. Baling is the process of determining which group of LLVM instructions can be combined (baled) together and efficiently mapped to vISA. A bale has a root instruction as well as optional modifiers and region instructions on the source and destination operands. The baling analysis pass constructs a map to mark which IR instructions are selected and what roles they play in their resulting bales. The root of a bale is the last instruction in the program order of all instructions in the bale, which is also the only instruction whose value is used outside the bale. Since the baling pass may decide to bale in an instruction with multiple uses as a non-root instruction, the instruction is cloned to ensure it has only a single use inside the bale.

vISA is designed to be close to Gen ISA and inherits similar restrictions (e.g., the size of an operand may not exceed two GRFs). After the initial baling analysis, the legalization pass may split up one bale into multiple instructions to conform to vISA restrictions. In general, the splitting must be done carefully to take advantage of the maximum SIMD width allowed by the target platform. Other examples of transformations performed here include un-baling an instruction due to conflicting legalization requirements, aligning operands for memory access operations, and promoting byte type operations into equivalent short ones to work around hardware restrictions.
The vector optimization pass performs optimizations based on \textit{rdregions} and \textit{wrregions} tailored for vector and matrix. The following are a few examples:

- Constant folding: We have extended LLVM constant folding so that it can fold and propagate vector constants through \textit{rdregions} and \textit{wrregions}.
- Promoting C-array into LLVM vector: Although it is not recommended, users can use a C-array in CM instead of a CM vector. The CM compiler can replace C-array loads and stores with \textit{rdregions} and \textit{wrregions}.
- Region collapsing: This can be viewed as instruction-combining transformation specific to \textit{rdregions} and \textit{wrregions}.
- Dead vector removal: This is a more general form of dead-code elimination on vector values. The uses of every vector element are tracked to determine if the whole vector is dead.
- Vector decomposition: Given a large vector, if compiler can show that it can be divided into multiple segments, where the \textit{rdregions} and \textit{wrregions} on these segments are disjoint, then this large vector can be converted into multiple small ones, which increases the flexibility for the register allocator.

As an example of the compiler code generation, consider again the linear CM implementation presented in Algorithm 2. Figure 4 illustrates how a 6x24 sub-matrix char-to-float conversion is done through a select operation (line 7 in Algorithm 2).

\begin{center}
\begin{tabular}{cccccc}
1 & 2 & 3 & 4 & 5 & 6 \\
7 & 8 & 9 & 10 & 11 & 12 \\
13 & 14 & 15 & 16 & 17 & 18 \\
19 & 20 & 21 & 22 & 23 & 24 \\
25 & 26 & 27 & 28 & 29 & 30 \\
31 & 32 & 33 & 34 & 35 & 36 \\
\end{tabular}
\end{center}

\texttt{m = in.select\!<\!<6,1,24,1\!>\!(1,3);}

Fig. 4. Sub-matrix layout of a 6x24 char-to-float select operation.

This select operation is compiled into 9 SIMD16 instructions as shown below:

1) \texttt{mov (16|M0) r11.0<1>:f r4.3<8;8,1>:ub} \\
2) \texttt{mov (16|M0) r13.0<1>:f r4.19<16;8,1>:ub} \\
3) \texttt{mov (16|M0) r15.0<1>:f r5.11<8;8,1>:ub} \\
4) \texttt{mov (16|M0) r17.0<1>:f r6.3<8;8,1>:ub} \\
5) \texttt{mov (16|M0) r19.0<1>:f r6.19<16;8,1>:ub} \\
6) \texttt{mov (16|M0) r21.0<1>:f r7.11<8;8,1>:ub} \\
7) \texttt{mov (16|M0) r23.0<1>:f r8.3<8;8,1>:ub} \\
8) \texttt{mov (16|M0) r25.0<1>:f r8.19<16;8,1>:ub} \\
9) \texttt{mov (16|M0) r27.0<1>:f r9.11<8;8,1>:ub}

In Gen ISA, a source operand’s region is a 2D-array in row-major order with the format \texttt{<W:W,H>}, where \(W\) (width) is the number of elements in a row, \(H\) (horizontal stride) is the step size between two elements in a row, and \(V\) (vertical stride) is the step size between two rows. This example shows the power of CM programming on Gen; programmers express their algorithms using high-level matrix operations, and the compiler generates them into multiple SIMD instructions while taking advantage of the region-based address scheme to efficiently access register data.

VI. EXPERIMENTAL EVALUATION

This section presents a set of applications from different domains implemented in CM and OpenCL with their experimental evaluation on an Intel GPU. We also analyze results in terms of the productivity and development effort from the development process of several compute kernels.

\textbf{A. Applications}

We briefly highlight the implementation strategy of every CM kernel that enables them to achieve close-to-the-metal performance. The source code and description of the applications benchmarked can be found in [6] and in the appendix of this paper. The OpenCL kernels are from the Intel OpenCL SDK [35] except for histogram and k-means which were developed internally by expert OpenCL programmers. All of them have been tuned and represent state-of-the-art OpenCL implementations for Intel GPUs. As baseline, all kernels were compiled with -O2 for the optimization level.

Typical input parameters were used for benchmarking the applications and their specification is described in every subsection; a detailed study of application behavior with varying input sizes is beyond the scope of this paper.

The Intel IceLake (ICL) processor was used to run the workloads. The ICL system includes an Intel Core i7 with 4 CPU cores, 16GB of system memory and a Gen11 integrated GPU with 64 EUs. Performance comparison is done by measuring the total execution time.

1) \textbf{Bitonic Sort}: it is a classic parallel algorithm for sorting elements [36]. Given \(2^n\) input elements, the bitonic network takes \(n\) stages to sort, producing chunks of sorted elements in ascending and descending order in every stage. At every stage there is a split procedure that cuts one bitonic sequence into two smaller ones. The SIMT bitonic sort implementation benefits from using vector data types (e.g. \texttt{int4}) available in OpenCL, however, it involves global memory access within every stage. To avoid excessive global memory access and global synchronizations, our CM kernel takes advantage of the large register space to hold 256 data elements in registers, processing several split steps locally. Experimental results show that our CM implementation outperforms the OpenCL version by 1.6x to 2.3x as shown in Figure 5. The higher speedup with larger input sizes is due to additional savings from memory accesses and global synchronizations.

2) \textbf{Histogram}: it is a common statistical tool used in image processing applications. It collects the distribution of pixel intensities from an image. Both CM and OpenCL are based on local and global histograms to perform the parallel computation. However, while in the OpenCL implementation each thread’s local histogram is stored...
in the SLM, in the CM kernel it is efficiently stored in registers. Also, in the OpenCL kernel one additional step is needed: after the local histogram computation the first thread in a work-group atomically updates the global histogram with local results. Figure 5 shows that CM significantly outperforms OpenCL, achieving up to 2.7x speedup. Furthermore, OpenCL’s performance is very sensitive to different input patterns. The performance gap is narrower for randomly-generated input, where the OpenCL kernel is unlikely to incur SLM bank conflicts and serialized atomic increments. For real-world images with homogeneous background (e.g., earth), however, OpenCL’s performance degrades significantly due to contention among atomic operations.

3) K-means Clustering: it is a popular clustering algorithm used in data mining and machine learning [3]. K-means stores \( k \) centroids that it uses to define clusters. A point is considered to be in a particular cluster if it is closer to that cluster’s centroid than any other centroid. The CM k-means kernel is divided into two phases that iterate alternatively until the centroids converge. The first phase divides input data into chunks of elements. Each hardware thread processes the clustering for each chunk and computes the minimum distance to determine which cluster (centroid) a point belongs. The second phase sums up the accumulated coordinates and the number of points in each cluster and computes the new centroid positions. In a final step, coordinates of the thread’s cluster are produced. Compared to the OpenCL implementation, in Figure 5 it can be seen that the CM k-means is 30% to 50% faster with three different data sets. This performance difference is mainly because the CM k-means efficiently shares centroids and other auxiliary data structures in the register file instead of using SLM and thread barriers. The CM kernel also benefits from efficient scattered memory reads, which are overlapped by the CM compiler for latency hiding.

4) Sparse Matrix-Vector Multiplication (SpMV): for a sparse matrix \( A \), SpMV computes the result of \( Y = AX \), where \( Y \) and \( X \) are two dense vectors. It is widely used in many graph algorithms and scientific applications. The SIMT OpenCL implementation uses the \text{cl\_intel\_subgroup} extension and SLM efficiently, however, the presence of irregular memory accesses due to the nature of the input limits its performance. The CM implementation tackles this issue by adding the capability of dynamically varying the instruction SIMD. Since issuing wider vector loads than necessary wastes memory bandwidth and increases contention, we use dynamic branches to check different block sizes and select the best execution size accordingly. This capability of varying SIMD size to improve both memory and compute efficiency is an important CM advantage over OpenCL. Another advantage is the use of boolean reductions that are applied to detect if all input rows are zero and skip the entire computation. This also improves both memory and compute efficiency for sparse matrices. Experimental results in Figure 5 show that the CM kernel outperforms the OpenCL implementation by 10% and 25% for the Protein and Nd24k matrices which have the highest number of non-zero elements per row (around 200). For Webbase which has low density and high variance of non-zero elements (3 non-zeros/row), varying SIMD width is effective on achieving high memory efficiency and it performs 160% better than OpenCL.
5) **Matrix Transpose:** it is a fundamental linear algebra operation that is heavily used in machine learning workloads. An optimized SIMT GPU implementation typically utilizes the SLM to avoid uncoalesced global memory access. For an out-of-place matrix transpose, threads within a thread group cooperatively copy a tile of the matrix from global memory into SLM, perform barrier synchronization, then copy SLM data using transposed array indices to the global output buffer. The CM implementation can completely bypass SLM and avoid synchronization overhead by directly performing the transpose on registers. Transpose is performed using a combination of CM’s select and merge operations to shuffle each element to their transposed position. For example, the following CM code sequence transposes a 2 × 2 matrix

\[
\begin{pmatrix}
a & b \\
c & d
\end{pmatrix}
\]

\[
v_0 = v.txt\_replicate\langle 2, 1, 2, 0 \rangle (0); // [a,b,b,b]
\]

\[
v_1 = v.txt\_replicate\langle 2, 1, 2, 0 \rangle (2); // [c,c,d,d]
\]

\[
v_2 = \text{merge}(v_0, v_1, 0b101); // [a,c,b,d]
\]

We view \( m \) as a vector \( v = [a, b, c, d] \) and \( v_2 \) as the transpose of the original input matrix. Transpose of bigger matrices can be solved by recursively applying the above steps to each sub-matrix.

Experimental results on different matrix sizes, as illustrated in Figure 5, show that this CM implementation achieves a speedup of up to 2.2x compared to the SLM-based OpenCL implementation. OpenCL’s subgroup shuffle functions do not help here since they are not expressive enough to exploit Gen’s operand regioning.

6) **SGEMM and DGEMM:** General Matrix-to-Matrix Multiplication (GEMM) is a function that performs matrix multiplication of the form \( C = \alpha AB + \beta C \), where \( A, B \) and \( C \) are dense matrices and \( \alpha \) and \( \beta \) are scalar coefficients. It is at the heart of many scientific applications and achieving peak theoretical performance is critical for every architecture. Here we focus on single precision floating-point (SGEMM) and double precision floating-point (DGEMM). Even though OpenCL and CM GEMM kernels employ a similar register-blocking strategy—OpenCL is able to do so by using the cl_intel_subgroup extension and mimicking the CM implementation, the CM kernel is able to process more data per thread thanks to more efficient management of the register file. As a result, CM outperforms OpenCL by 8.5% in DGEMM and around 10% in SGEMM for different input sizes as illustrated in Figure 5.

7) **Prefix Sum:** it is the cumulative sum of a sequence of numbers and plays an important role in many algorithms, e.g., stream compaction, radix sort, etc. The OpenCL implementation is based on Blelloch’s algorithm and uses a tree-traversal approach to build the prefix sum with parallel reductions and partial sums. It exploits the SLM but incurs several data movements between local and global memory, plus multiple barriers. Our CM implementation uses a similar approach but threads perform the parallel reduction and partial sums entirely in registers, updating their results in place on the input array through scattered writes. Figure 5 depicts that the CM implementation achieves 1.6x speedup compared to the OpenCL kernel for different input sizes.

### B. Productivity

Programmability is a common concern for the adoption of close-to-the-metal programming models, as one must carefully weigh their performance advantages against the potential developer productivity loss due to the ramp-up overhead and a lower level of abstraction. CM has been extensively used for high-performance library development inside Intel, however, and user experiences overwhelmingly suggest that programmers are much more productive using CM once performance tuning efforts are considered. During the early stages of kernel development for Intel’s deep learning neural network libraries, there was an intense debate on the choice of programming model. To ensure a fair comparison, a team of GPU compute architects implemented several key kernels in both OpenCL and CM. The architects in the study have years of experiences developing workloads in both models for Intel GPUs. Table I details the development efforts as well as the performance achieved by both programming models. Development effort is measured as the amount of work performed to implement each kernel from scratch and meet the minimal performance requirement. Performance data are collected on a simulator for a future GPU platform and thus not included in the evaluation earlier in this section. Performance speedup is calculated as

\[
\frac{\text{OpenCL execution time}}{\text{CM execution time}}
\]

| Kernel                  | OCL effort (person-week) | CM effort (person-week) | Performance (OCL/CM) |
|-------------------------|--------------------------|-------------------------|----------------------|
| Systolic GEMM           | 8                        | 3                       | 1.09x                |
| DGEMM and SGEMM         | 12                       | 4                       | 1.06~1.09x           |
| Conv. 3x3               | 4                        | 4                       | 1.08x                |
| Conv. 3x3               | 15                       | 4                       | 1.3x                 |
| Stencil2D               | 2~3                      | 1                       | 2.2x                 |

Table I shows that for these deep learning kernels CM yields 2-3x more productivity than OpenCL on average while achieving better performance. The study found that developers could deliver functional OpenCL kernels quickly, but the initial version’s performance is often far below the desired targets. During the subsequent performance tuning, they have to spend considerable efforts fighting with the programming model and the compiler to get the desired assembly code. To achieve the best performance, developers need to control multiple aspects of kernel behavior including register usage, data sharing, latency hiding, copy coalescing, and bank conflict avoidance. The SIMT abstraction makes it difficult for even expert GPU programmers to control a kernel’s full optimization needs, and
their OpenCL implementation suffers from poor performance predictability; an innocuous one-line change could result in significant variation in generated code if it causes the kernel to spill or copy moves to not be coalesced. On the contrary, CM allows users to manage critical machine resource explicitly to instruct the compiler to generate expected code sequence. The first working CM version is frequently able to approach or sometimes even exceed the performance target, thus greatly reducing the need for intensive tuning and rewrites later.

VII. CONCLUSIONS

This paper presents C-for-Metal, a high-level yet close-to-the-metal programming language for Intel GPUs. Major features are illustrated for how to expose underlying hardware capabilities: vector/matrix variables represent registers and express SIMD parallelism, select operation maps to register regioning, block read/write enables efficient memory access, and divergent control flow constructs allow for mixing SIMT and SIMD models. We evaluate several applications and their experimental results show that the performance gap between CM and OpenCL can be significant, ranging from 20% to over 100%.

This paper is not meant to be an attack on SIMT programming models; they are popular on GPUs for a reason and several of the authors are active contributors to Intel’s OpenCL compiler. Rather, we have shown that the convenience of the SIMT abstraction carries a performance cost that can be difficult to overcome even with expert programming. A programming model that is natively designed to harvest hardware capabilities fully thus fills an essential void, and this metal-level expressiveness is especially important for performance-critical applications.

CM is positioned as a low-level programming tool for Intel GPUs. Different languages’ front ends have started using CM as their back end. For instance, DPC++-ESIMD \([41]\) integrates some CM language features into DPC++, and ISPC \([42]\) also generates CM vector intrinsics and relies on CM optimizations and code generation. Moreover, given the rising importance of vector and matrix data types for neural-network programming, we foresee that IR extensions similar to our \texttt{rdregion} and \texttt{wrregion} may be added into LLVM for other target machines.

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APPENDIX

A. Abstract

Our artifact contains the implementation of the CM compiler (CMC) as well as the applications and benchmarks used in the experimental evaluation section. We provide the required scripts to compile and execute the benchmarks, which allows the reproducibility of our results on any system with Intel Gen9 (Skylake) GPU or above.

B. Artifact Meta-Information

- **Program**: The CM compiler implemented in C++; CM applications; OpenCL applications (all sources and binaries included).
- **Compilation**: With provided scripts via gcc/g++.
- **Data set**: Applications use input data sets included either as separated files or generated at runtime. For the former case, they are located in each application directory.
- **Run-time environment**: Linux Ubuntu 18.04 or above, CM runtime and OpenCL runtime.
- **Hardware**: Intel Gen9 GPU or above.
- **Output**: Performance results in text files for every application evaluated with CM and OpenCL.
- **Publicly available**: The CM compiler as well as all the CM and OpenCL examples are publicly available except from those listed in the productivity section (section 6.1).
- **Code license**: The Intel(R) CM compiler and examples are distributed under the MIT license.

C. Description

1) How Delivered: The CM compiler is available on Github: [https://github.com/intel/cm-compiler](https://github.com/intel/cm-compiler). The CM and OpenCL examples, as well as scripts to build and run all the benchmarks are available on [https://github.com/jfuentes/C-for-Metal_CGO2021](https://github.com/jfuentes/C-for-Metal_CGO2021) Binaries of the CM compiler and benchmarks are also included in the artifact repository.

2) Hardware Dependencies: We recommend running the benchmarks on an Intel Gen11 GPU (Icelake), however, any other Intel GPU above Gen9 (Skylake) should give similar results. Notice that due to hardware configuration differences, further application-specific tuning may be required to achieve peak performance on different Gen platforms.

3) Software Dependencies: This artifact was prepared using Ubuntu 18.04. Similar Linux distributions should also work. The artifact repository contains the CM compiler build and its dependencies to compile all the benchmarks. To build the CM and IGC compilers from sources, specific details about dependencies and how to build them can be found in their repositories:
- **CMC**: [https://github.com/intel/cm-compiler](https://github.com/intel/cm-compiler)
- **IGC**: [https://github.com/intel/intel-graphics-compiler](https://github.com/intel/intel-graphics-compiler)

To run the benchmarks the CM runtime and OpenCL runtime are required, which can be found in their repositories:
- **CM runtime**: [https://github.com/intel/media-driver](https://github.com/intel/media-driver)
- **OpenCL oneAPI Level Zero Runtime**: [https://github.com/intel/compute-runtime](https://github.com/intel/compute-runtime)

D. Installation

First, install elemental dependencies for this artifact: g++, git, make, cmake and jansson.

```bash
$ sudo apt install g++ git git-lfs make cmake
```

1) **CM Compiler, Runtime and Benchmarks**: Download the artifact repository. It contains a build of the CM compiler and all the benchmarks. If building the CM compiler from sources is preferred, visit the CM compiler repository for more details (https://github.com/intel/cm-compiler). Also, notice that some applications files are uploaded via lfs. So make sure they are downloaded properly.

```bash
$ git clone https://github.com/jfuentes/C-for-Metal_CGO2021
$ cd C-for-Metal_CGO2021
$ git-lfs pull
```

Now, we need to build and install the media driver which contains the CM runtime needed to run CM applications. Install prerequisites:

```bash
$ sudo apt install autoconf libtool libdrm-dev xorg-dev libx11-dev libgl1-mesa-glx
```
libgl1-mesa-dev xutils-dev

Build and install libva:

```
$ git clone https://github.com/intel/libva.git
$ cd libva
$ ./autogen.sh --prefix=/usr
   --libdir=/usr/lib/x86_64-linux-gnu
$ make
$ sudo make install
```

Finally, build the media driver:

```
$ git clone https://github.com/intel/media-driver.git
$ git clone https://github.com/intel/gmmlib.git
$ mkdir build_media & cd build_media
$ cmake ..
$ make -j8
$ sudo make install
```

Notice that at this point you might need to set the path of the driver and make sure the path for dynamic libraries is set:

```
$ export LIBVA_DRIVERS_PATH=/usr/lib/x86_64-linux-gnu/dri
$ export LIBVA_DRIVER_NAME=IHD
$ export LD_LIBRARY_PATH=/usr/lib
$ export LD_LIBRARY_PATH:=$LD_LIBRARY_PATH:
```

2) OpenCL Compiler (IGC) and Runtime for Intel GPU:

To install IGC and NEO runtime download the packages and follow the instructions from the compute runtime repository at https://github.com/intel/design-of-cue/releases

Then, install OpenCL headers:

```
$ git clone https://github.com/KhronosGroup/OpenCL-Headers.git
$ cd OpenCL-Headers
$ sudo mv CL/ /usr/include/
```

Additionally, you need to install the OpenCL C++ headers. Follow the installation steps from https://github.com/KhronosGroup/OpenCL-CLHPP

Finally, install the OpenCL Installable Client Driver (ICD)

```
$ git clone https://github.com/KhronosGroup/OpenCL-ICD-Loader.git
$ cd OpenCL-ICD-Loader
$ mkdir build & cd build
$ cmake ..
$ make
$ sudo make install
```

E. Experiment Workflow

Once the above packages are installed, all the CM and OCL benchmarks can be built. Locate at the artifact repository and simply run:

```
$ cd benchmarks
$ sh build_CM_all.sh
$ sh build_OCL_all.sh
```

The above command will generate both the kernel binaries and host executables for every benchmark. Notice that as the CM compilation is offline compilation it will ask the GPU platform you are compiling for (SKL, ICL, etc.). Then, run the benchmarks:

```
$ sh run_CM_all.sh
$ sh run_OCL_all.sh
```

F. Evaluation and Expected Result

Once the benchmarks are finished, performance results are reported to the standard output as well as text files located in the results directory. For each benchmark the kernel execution time and total execution time are reported. Performance results are in milliseconds and organized by input data.

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