Design of a Dynamic Parameter-Controlled Chaotic-PRNG in a 65 nm CMOS process

Partha Sarathi Paul, Maisha Sadia, and Md Sakib Hasan
Department of Electrical and Computer Engineering
University of Mississippi
University, MS 38677, USA
Email: ppaul@go.olemiss.edu, msadia@go.olemiss.edu, mhasan5@olemiss.edu

Abstract—In this paper, we present the design of a new chaotic map circuit with a 65 nm CMOS process. This chaotic map circuit uses a dynamic parameter-control topology and generates a wide chaotic range. We propose two designs of dynamic parameter-controlled chaotic map (DPCCM)-based pseudo-random number generators (PRNG). The randomness of the generated sequence is verified using three different statistical tests, namely, NIST SP 800-22 test, FIPS PUB 140-2 test, and Diehard test. Our first design offers a throughput of 2.00 MS/s with an on-chip area of 0.024 mm² and a power consumption of 2.33 mW. The throughput of our second design is 300 MS/s with an area consumption of 0.132 mm² and power consumption of 2.14 mW. The wider chaotic range and lower-overhead, offered by our designs, can be highly suitable for various applications such as, logic obfuscation, chaos-based cryptography, re-configurable random number generation, and hard-ware security for resource-constrained edge devices like IoT.

Index Terms—Nonlinear dynamics, chaos, IoT, CMOS, PRNG, cryptography, logic-obfuscation, NIST, FIPS, Diehard.

I. INTRODUCTION

In recent decades, the nonlinear dynamic system has attracted the attention of researchers in the field of physics, biology, economics, finance, and engineering. Chaotic system is a particular type of nonlinear dynamic system whose behavior is characterized by deterministic equations. These irregular (aperiodic) but deterministic systems are very sensitive to the initial states. Even a tiny difference in the initial state makes the trajectory of two chaotic sequences, from the same chaotic system, significantly diverged. This phenomenon is popularly known as the butterfly effect. Some significant properties including, deterministic-aperiodicity and initial-state-sensitivity make the chaotic system very popular in security applications, including pseudo-random number generator (PRNG), cryptography, image encryption, and logic obfuscation. However, the present-day advancement in machine-learning algorithms is making the chaos-based security systems vulnerable to potential adversaries. Therefore, the chaos-based security community remains in an ongoing quest for a superior-quality chaotic system. A higher dimensional chaotic system promises a more complex and secure chaotic sequence but brings the computation-cost into play as well. Hence, the design of a new chaotic system, with a simple structure but improved performance, is vital.

In this paper, we present the design of a new chaotic map circuit with a 65 nm CMOS process. The general framework of the map circuit includes the three-transistor chaotic map circuit, proposed by Dudek et al. [1], and dynamic parameter-control topology, proposed by Hua et al. [2]. We propose the design of a novel PRNG circuit using our dynamic parameter-controlled chaotic map (DPCCM). Three statistical tests, NIST, FIPS, and Diehard, are performed on the PRNG output to verify the randomness of the generated sequence.

The remaining portion of the paper is organized as follows: section II describes the structure of the DPCCM. The proposed PRNG design and statistical analysis are described in section III and IV, respectively. Section V talks about the overhead analysis of the proposed PRNG. Finally, section VI gives the concluding remarks.

II. DESIGN OF DPCCM

The transistor-level design of the DPCCM circuit is done using a 65 nm CMOS process in Cadence, with the supply voltage of 1.2 V. The structure of the circuit can be described by separating it into three abstraction levels: a) the map circuit, b) the chaotic oscillator, and finally, c) the DPCCM.

A. Map circuit

The schematic of the three-transistor map circuit is shown in Fig. 1(a). The size of the transistors, $M_1$, $M_2$, and $M_3$, are carefully chosen to get a V-shaped transfer characteristic, which is vital for generating a chaotic sequence [3]. The gate voltage of $M_2$ (i.e. $V_c$) is used as the control voltage of the map.

B. Chaotic oscillator

The chaotic oscillator (shown in Fig. 1(b)) comprises of two feed-back connected map circuits, using the same control voltage. The initial state voltage, $X_n$, is applied through the clock, clk$_{ini}$. $X_n$ passes through the first map circuit block and we get the first output voltage, $V_{out1}$. $V_{out1}$ is then passed to the map circuit block in the feedback path through another clock, clk$_{n}$. The first iteration loop concludes when the generated output voltage, $V_{out2}$, is passed to the first map circuit through the clock, nclk$_{n}$. As the cycle continues, we get two analog voltages per iteration. Since, the clock signals, clk$_{n}$ and nclk$_{n}$, are non-overlapping, we use them to sample-and-hold the analog output voltage of the chaotic oscillator. Conventional designs use capacitors in the sample-and-hold circuit to store the data. In this topology, to reduce the on-chip area overhead,
the parasitic capacitance of the pass transistors are leveraged to store the data. The total area consumption of the chaotic oscillator, along with the clocking circuits, is 0.556 \( \mu \text{m}^2 \) and the total power consumption is 18.4 \( \mu \text{W} \). Fig. 2(a) shows the bifurcation plot of the chaotic oscillator and Fig. 3(a) shows the corresponding Lyapunov exponent.

C. DPCCM

The block diagram of the DPCCM is presented in Fig. 1(c). The analog output voltage from a chaotic oscillator (seed map) undergoes a linear transformation before going into another chaotic oscillator (controlled map) as its control voltage parameter. The linear transformation is chosen in such a way that the output voltage of the first chaotic map is always mapped into a range of control voltages that generates chaotic sequence from the controlled map. The transformation is done according to Eq (1) [2].

\[
V_{\text{control}} = \left( \frac{b_{\text{max}} - b_{\text{min}}}{a_{\text{max}} - a_{\text{min}}} \right) \times (a_{\text{max}} - V_{\text{seed}}) + b_{\text{min}} \tag{1}
\]

In Eq (1), \( V_{\text{seed}} \) denotes any particular output voltage from the seed map, while \( V_{\text{control}} \) is the transformed control voltage for the controlled map. The chaotic range for the control voltage is within \( a_{\text{max}} \) and \( a_{\text{min}} \) whereas, the span of the seed map output voltage is from \( b_{\text{max}} \) to \( b_{\text{min}} \).

The term, dynamic parameter-control, comes from the fact that, at each iteration, the control voltage of the controlled map is being controlled by the output of the seed map. It is obvious from Fig. 2(a) and Fig. 3(a) that, there are two distinct chaotic regions in the chaotic oscillator’s output map, which shows positive Lyapunov exponent. The first range of the control voltage is between 0.5275 \( V \) and 0.6225 \( V \). The second range is between 0.89 \( V \) to 0.9525 \( V \). The output voltage covers a larger range for the case of the first control-voltage range (0.5275 \( V \) - 0.6225 \( V \)). Moreover, it is found that the transistor delay increases with the increase of the control-voltage [4]. Hence, we chose the transformation of the DPCCM within the range of the first control voltage. The seed map and the controlled map starts with the same initial voltage. The bifurcation diagram from the DPCCM and the corresponding Lyapunov exponent is shown in Fig. 2(b) and Fig. 3(b), respectively. The bifurcation plot of the DPCCM shows a wider chaotic range, compared to the bifurcation plot of the chaotic oscillator. A chaotic map circuit with a wider chaotic range can be extremely useful in applications like chaos-based logic and side channel obfuscation and re-configurable chaotic pseudo-random number generators (PRNG), where a wider chaotic range offers a larger design space. Here, we show the application of our DPCCM topology in a PRNG circuit.

III. DESIGN OF PRNG

The DPCCM topology is implemented to design a PRNG. The schematic of the proposed PRNG is shown in Fig. 4. Two DPCCM blocks, \( \text{DPCCM}_a \) and \( \text{DPCCM}_b \), are used in the PRNG design to get the required entropy in the generated sequence. Two phase-shifted clocks, \( \text{clk}_a \) and \( \text{clk}_b \), runs the
IV. STATISTICAL TESTES RESULTS

A. NIST SP 800-22 Test Suite

National Institute of Standards and Technology (NIST) test suite offers 15 statistical tests to measure the randomness in a sequence. The test was performed with a bit-stream length of 1 million. The significance level was set to 0.01. That means, a sequence with 100 million bits will pass a particular test if at least 96 out of the 100 bit-streams generate a $p-value$ of greater than 0.01. The 100 million-bit sequence, generated from design-I, passes all 15 tests with an ADC of bit-size $\geq$ 8. Whereas, design-II passes the test with an ADC of bit-size $\geq$ 10. Table I shows the NIST test result for design-I (8-bit ADC) and design-II (10 bit ADC).

B. FIPS PUB 140-2

Federal Information Processing Standards Publications (FIPS PUB) 140-2 Test was developed by NIST. FIPS tests the randomness of a binary sequence by dividing it into 20,000-bit blocks. The blocks are subjected to 4 sub-tests - the Monobit test, Poker test, Runs test and Long run test. The Monobit test counts the number of 1’s in the 20,000-bit block. This number must be within the range of (9725,10275) to pass the test. The Poker test divides the 20,000-bit block into 5,000 successive 4-bit segments. The 4-bit segment can have 16 possible values and the occurrence of these 16 values is counted and stored. This sub-test verifies the uniformity of the 4-bit segment. Runs test counts and stores the maximum sequence of consecutive bits of 1’s or 0’s in a 20,000-bit block. A run of 26 or more of either 1’s or 0’s is defined as a Long run. The total number of Long runs in a 20,000-bit block is counted in the total failure. Table II shows the FIPS test result for design-I (8-bit ADC) and design-II (10 bit ADC).

---

**TABLE I: NIST Test results for design-I and design-II** (*shows the average of multiple tests*)

| Test                | design-I | design-II |
|---------------------|----------|-----------|
| Frequency           | 0.99     | 1.00      |
| Block frequency     | 0.98     | 0.99      |
| Cumulative sums     | 1.00     | 1.00      |
| Runs                | 1.00     | 1.00      |
| Longest runs of ones| 0.99     | 0.98      |
| Rank                | 1.00     | 0.99      |
| FFT                 | 0.99     | 0.99      |
| Non-overlapping template | 0.99 | 0.99 |
| Overlapping template | 0.99     | 0.98      |
| Universal           | 1.00     | 1.00      |
| Approximate entropy | 0.98     | 0.99      |
| Random excursion*   | 0.99     | 0.99      |
| Random excursion variant* | 1.00 | 1.00 |
| Serial*             | 1.00     | 0.99      |
| Linear complexity   | 1.00     | 1.00      |

**TABLE II: FIPS test results**

| PRNG     | Total success | Monobit | Poker | Runs | Long run |
|----------|---------------|---------|-------|------|----------|
| design-I | 4999          | -       | -     | 1    | -        |
| design-II| 4996          | -       | 3     | -    | 1        |
The sequence is considered to be random if the \( p - \text{values} \) are within the range of \([0,1)\). A sequence will fail the test if it produces six or more (out of 219) \( p - \text{values} \) of either 0 or 1. Our test sequence size is 100,000,032 bits. Fig. 5 shows the plot of the generated \( p - \text{values} \), sorted in ascending order. The linear fit shows close conformity with the generated \( p - \text{value} \) trend and demonstrates the randomness of our sequence.

V. OVERHEAD ANALYSIS OF THE PRNG

Each of the two DPCCM blocks, shown in Fig. 3 used in the design, consumes an area of 1.1 \( \mu m^2 \) and a power of 36.8 \( \mu W \). The 8-bit ADC, used in design-I, can be implemented from the proposed design of Wei et al. in [8]. This 8-bit ADC takes 0.024 \( mm^2 \) on-chip area and consumes 1.8 \( mW \) power. As we can see, the ADC is responsible for most of the area and power consumption of the circuit making it the primary overhead contributor to the whole PRNG design. The maximum bit generation rate of this 8-bit ADC is 250 MS/s. However, design-I generates binary sequence with a rate of 200 MS/s. The throughput of the slower component dictates the overall throughput of the system. Hence, the throughput of the overall PRNG system, with design-I, is limited to 200 MS/s. We have determined that our design-II can offer a maximum throughput of 600 MS/s (i.e. three times higher than design-I).

The 10-bit ADC, used in design-II, can be implemented from the design reported by Ma et al. [9]. This 10-bit ADC covers an on-chip area of 0.132 \( mm^2 \) and consumes 1.6 \( mW \) power. For our design-II, we are taking the last three ADC bits at every even iteration. Therefore, the throughput from the 10-bit ADC, with 100 MS/s bit-rate, will eventually become 300 MS/s (i.e. three times 100 MS/s) in our design. For this reason, the throughput of the overall PRNG system, with design-II, is limited to 300 MS/s. The total area overhead for design-I, including chaotic oscillators, ADC, shift register, MUX, and XOR gate, is 0.024 \( mm^2 \) and the power overhead is 2.33 \( mW \).

Design-II, total area and power overheads are 0.132 \( mm^2 \) and 2.14 \( mW \), respectively. Table III presents a comparison between the PRNG designs of this paper and prior works on different PRNG circuits. Compared to previous works, both of our designs cover significantly less on-chip area. Our design-I is a suitable choice for applications with high area-constraint whereas design-II offers better throughput. It should be noted that design-II can be generalized for higher-bit ADC while compromising the area and power.

VI. CONCLUSION

A new design of a chaotic map circuit, with dynamic parameter control, is presented in a 65 \( nm \) CMOS process. It has been shown that this design provides a wide chaotic region in the bifurcation plot, offering a large design space for various security applications such as, logic obfuscation, chaos-based cryptography and re-configurable random number generator circuits. The map circuit is used in a novel PRNG design. The randomness of the generated sequence is verified using three statistical tests. It is found that the dynamic parameter-control leads to a low-overhead PRNG design. Future work may include, the exploration of various CMOS topologies and different post-processing schemes for the bit generation.

REFERENCES

1. P. Dudek and V. Juncu, “Compact discrete-time chaos generator circuit,” *Electronics Letters*, vol. 39, no. 20, pp. 1431–1432, 2003.
2. Z. Hua and Y. Zhou, “Dynamic parameter-control chaotic system,” *IEEE transactions on cybernetics*, vol. 46, no. 12, pp. 3330–3341, 2015.
3. A. S. Shanta, M. B. Majumder, M. S. Hasan, M. Uddin, and G. S. Rose, “Design of a reconfigurable chaotic gate with enhanced functionality space in 65nm cmos,” in *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2018, pp. 1016–1019.
4. A. S. Shanta, M. S. Hasan, M. B. Majumder, and G. S. Rose, “Design of a lightweight reconfigurable prng using three transistor chaotic map,” in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 2019, pp. 586–589.
5. A. Rukhin, J. Soto, J. Nechvatal, M. Smid, and E. Barker, “A statistical test suite for random and pseudorandom number generators for cryptographic applications,” Booz-allen and hamilton inc meclan va, Tech. Rep., 2001.
6. N. F. PUB, “140-2: Security requirements for cryptographic modules,” Information Technology Laboratory, National Institute of Standards and Technology, 2001.
7. G. Marsaglia. The marsaglia random number cdrom including the diehard battery of tests of randomness. [Online]. Available: https://web.archive.org/web/20160125103112/http://stat.fsu.edu/pub/diehard/
8. H. Wei, C.-H. Chan, U.-F. Chio, S.-W. Niu, U. Seng-Fan, R. Martins, and F. Maloberti, “A 0.024 \( mm^2 \) 2.8 \( bh \) \( 400m/s \) sar adc with 2h/cycle and resistive dac in 65nm cmos,” in *2011 IEEE International Solid-State Circuits Conference*. IEEE, 2011, pp. 188–190.
9. J. Ma, Y. Guo, L. Li, Y. Wu, X. Cheng, and X. Zeng, “A low power 10-bit 100m/s sar adc in 65nm cmos,” in *2011 9th IEEE International Conference on ASIC*. IEEE, 2011, pp. 484–487.
10. F. Pareschi, G. Setti, and K. Rovatti, “Implementation and testing of high-speed cmos true random number generators based on chaotic systems,” *IEEE transactions on circuits and systems I: regular papers*, vol. 57, no. 12, pp. 3124–3137, 2010.
11. C.-Y. Li, Y.-H. Chen, T.-Y. Chang, L.-Y. Deng, and K. To, “Period extension and randomness enhancement using high-throughput reseeding-mixing prng,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 2, pp. 385–389, 2011.
12. H.-T. Yang, J.-R. Huang, and T.-Y. Chang, “A chaos-based fully digital 120 mhz pseudo random number generator,” in *The 2004 IEEE Asia-Pacific Conference on Circuits and Systems, 2004. Proceedings., vol. 1*. IEEE, 2004, pp. 357–360.

| Parameter | Reported works | This work |
|-----------|----------------|-----------|
| Technology (nm) | 180 | 180 | 180 | 65 | 65 | design-I | design-II |
| Supply voltage (V) | 1.8 | 1.8 | 1.8 | 1.2 | 1.2 | 65 | 65 |
| Area (\( mm^2 \)) | 0.126 | 0.275 | 0.767 | 0.132 | 0.024 | 0.132 |
| Power (\( mW \)) | 22 | 13.9 | 37 | 2.12 | 2.33 | 2.14 |
| Throughput (MS/s) | 100 | 6400 | 120 | 100 | 200 | 300 |

TABLE III: Overhead comparison