Design of SOPC digital frequency meter based on MicroBlaze

Haixin Sun, Yujie Fan and Qiang Xiang*

School of Electrical and Information Engineering, Southwest Minzu University, Chengdu, China

*Corresponding author e-mail: xqiang_0426@163.com

Abstract. A method of SOPC implementation of digital frequency meter is presented in this paper. In the method, Encapsulated AXI IP core for frequency measurement and duty cycle measurement are configured with the embedded soft core MicroBlaze processor. The parameter measurement of the digital frequency meter is implemented by FPGA logic resources, and the measured data are transmitted to the soft core processor via AXI bus. The computation, control and display is completed by Microblaze soft core. The system is verified and tested on the Basys3 board card launched by digilent company. The results show that the system has the advantages of accurate measurement, good stability, simple scheme and low cost.

Keywords: Digital frequency meter, SOPC, MicroBlaze.

1. Introduction

With the development of electronic technology, as a basic tool in electronic measurement application field, digital frequency meter is also developing towards integration and miniaturization. In the traditional design scheme, an FPGA chip and a microprocessor work together. This design method not only wastes a lot of resources, but also increases the design cost. The development of SOPC technology closely combines the advantages of FPGA and microprocessor system in a certain extent. Through the use of soft core, the traditional design is completed on a chip, which not only reduces the design cost, but also makes the product design more concise. The method of periodic frequency measurement is to count the time interval between two successive rising or falling edges of the measured signal through a counter, and then invert the counting result to obtain the frequency. This method needs high precision clock reference signal, which is high accuracy in middle and high frequency measurement. The system is designed on the FPGA frequency circuit. The measured results are transmitted to the Microblaze soft core via FPGA for data processing, and the signal cycle, frequency, duty cycle and other parameters are measured.

2. Principle and framework of system frequency measurement

2.1. Principle of system measurement

2.1.1. Principle of periodic frequency measurement

Using a standard clock signal, the counter records the value between two consecutive rising or falling edges of the measured signal, and then obtains the frequency through certain calculation of the obtained counting results.
The reference clock signal named clk is a period signal with 250MHz. For convenience, we name the measured signal is data_in, and the counting result is data_out. When the rising edge of clk and the reset signal is logic high, and the measured signal comes, the counter starts to work. If the result of one cycle count of the measured signal is Nx and the frequency of the reference clock signal is FHz, then the frequency of the measured signal is Fx, The calculation formula is as follows:

\[ F_x = \frac{F}{N_x} \quad (1) \]

2.1.2. Duty cycle measurement principle

This paper adopts the method of periodic frequency measurement, so it is easy to measure the duty cycle. When the rising edge of clk_in and the reset signal are set to 1, the measured signal comes and the counter records the time interval between the rising edge and the adjacent falling edge of the measured signal in one cycle. On the basis of the test cycle, the duty ratio is calculated. If the high level count value of the measured signal is N, and the duty cycle is expressed by R, then:

\[ R = \left( \frac{N}{N_x} \right) \times 100\% \quad (2) \]

2.2. Systematic framework

The system block diagram with functions of frequency measurement and duty cycle measurement is shown in figure 1.

![System block diagram](image)

**Figure 1.** System block diagram

The input clock of the system is an external 100MHz clock, which generates a 150MHz clock and a 250MHz clock after frequency doubling through MMCM. The 150MHz clock is used for MicroBlaze core processor, and the 250MHz clock is the reference clock of FPGA frequency measurement module. As shown in figure 1, the signal generated by the signal source is transmitted to the FPGA frequency measurement circuit after being processed by the digital front-end conditioning circuit. This digital front-end conditioning module circuit is used to process sinusoidal signals and weak signals, so that the signal can reach the degree that FPGA can recognize. After the FPGA frequency measurement and duty ratio measurement are completed, the measured data will go through the AXI bus and be transferred to the MicroBlaze soft core for processing, and the measured results will be displayed through the OLED screen.

3. FPGA Frequency measurement module design

As a new generation of electronic technology, EDA technology has been widely used in the design of electronic products. Xilinx company provides a complete design platform such as system logic design platform, Xilinx Vivado Integrated Development Environment, Xilinx SDK, Vivado HLS, logic synthesis, timing simulation, download configuration. It provides the basic design platform for the design of SOPC.

As shown in figure 2 and figure 3, they are the flow of frequency measurement module and duty cycle measurement module. The input end of the signal is data_in. Before the signal enters the main circuit, it passes through the data_in_buf register and the data_in_pwm_buf register. The main function of the two registers is to judge the rising and falling edges of the signal. By judging the edge, and when the rising edge of the clock comes, start the 32-bit cycle counter and the time counter of the
height level. After the counting is completed, the counting results are sent to the 32-bit data_out and data_out_pwm registers respectively when the rising edge of the clock arrives. The AXI bus is transferred to the MicroBlaze soft-core controller.

![Figure 2. Frequency measurement module](image)

![Figure 3. Measured duty cycle module](image)

4. **Soft core processor system design**

4.1. *MicroBlaze processor*

AMicroBlaze is a configurable 32-bit soft-core processor with a simple instruction set provided by sering. Its basic structure is shown in figure 4. Users can configure it according to the performance and cost design requirements of the development system.
4.2. **Digital frequency meter embedded processing system**

The MicroBlaze processor system of the entire digital frequency meter is shown in figure 5. The MicroBlaze processor core, AXI bus and system peripherals are included.

**Figure 4. MicroBlaze processor structure**

**Figure 5. Digital frequency meter embedded MicroBlaze processor system**

AXI bus is an efficient bus protocol used in the design of programmable chip systems. It describes the port connection relationship between master and slave components and the timing relationship of communication between components. The peripherals in the system, such as OLED display interface module and frequency and duty cycle module, are realized by the internal logic resources of FPGA.

4.3. **SOPC System module generation**

This system is developed in the Xilinx Vivado Design version 2015.4. Vivado integrates the development environment of SOPC, it simulates and synthesizes the Verilog code, and encapsulates it into the IP core to verify the correctness and feasibility of the IP core. In the Vivado Diagram platform, various modules are connected through the IP core, and bitstream files are generated and integrated to the Xilinx SDK tool for software development.

It includes AXI bus Module, AXI_Freq_PWM_vl.0 test frequency test duty ratio Module, MicroBlaze Debug Module, Memory Module, MicroBlaze soft core Processor Module, Clocking Wizard System clock Module, oled_vl.0 display interface Module, Processor System Reset Module.
5. The software design of MicroBlaze system

This system software is developed on the Xilinx SDK software development platform and is written and designed in the form of C language.

The design of digital frequency meter system software is mainly realized in the form of read-write register. Each part is initialized in the main function, which mainly includes the initialization of OLED display module, frequency and duty cycle module, code switch and data algorithm, and then enters the main loop function to read and write registers and process data. The flow chart is shown in figure 6.

![Figure 6. System main function flow chart](image)

This system transmits data on the AXI bus. The frequency measurement and duty cycle module is written by Verilog code, which seals the target code into the IP core in the form of AXI bus, and finally transfers the measured data to the specified register, and processes the measured results through the writing of C code.

6. System testing

The system test was carried out on the BASYS3 development platform provided by Xilinx company. The HMF2550 function generator of Rohde & Schwarz company provides the signal source. When the reference clock is 250MHz, the measured signal is square wave, and the measured results in table 1 are shown on OLED display.

When the reference clock is 250MHz and the measured signal is a square wave of 5KHz, the duty cycle measurement results are shown in table 2.

By observing table 1, since the measurement period method is adopted, the system measurement frequency is slightly unstable in the low frequency stage, and the data is stable in the middle frequency measurement process, and the error is also small. Table 2 shows that in the duty cycle measurement of 5KHz square wave, the system measurement is stable and the measured data is relatively accurate.
Table 1. Measured data of the 250MHz reference clock

| Standard Frequency(Hz) | Actual Frequency(Hz) | Relative Error(%) | Standard Counting | Measurement Accuracy |
|------------------------|----------------------|-------------------|-------------------|----------------------|
| 5                      | 4.99992              | 0.008             | 5000008           | 10^4                 |
| 50                     | 49.99992             | 0.008             | 5000008           | 10^4                 |
| 500                    | 499.99999            | 0.001             | 500001            | 10^4                 |
| 5K                     | 49.99999K            | 0.001             | 50002             | 10^4                 |
| 50K                    | 49.99999K            | 0.001             | 5001              | 10^4                 |
| 500K                   | 499.99999K           | 0.001             | 500               | 10^4                 |
| 5M                     | 4.99999M             | 0.001             | 50                | 10^4                 |
| 10M                    | 9.99999M             | 0.001             | 25                | 10^4                 |
| 25M                    | 24.99999M            | 0.001             | 10                | 10^4                 |

Table 2. Reference clock is 250MHz measured signal for the 5KHz square wave duty cycle measurement data

| Actual Duty Cycle(%) | 25  | 30  | 35  | 40  | 50  | 55  | 60  | 65  | 70  | 75  |
|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Measured Duty Cycle(%) | 24.99 | 29.99 | 35.99 | 44.99 | 49.99 | 54.99 | 59.99 | 64.99 | 69.99 | 74.99 |
| Relative Error(%)   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

7. Conclusion

In this paper, a new digital frequency meter based on SPOC technology is proposed. The test results show that the measurement accuracy of the frequency of the system can reach 10^4, and the relative error of the duty ratio can reach 1%, which indicates that it is a feasible and effective method to design digital frequency meter with "FPGA + embedded SOPC soft core processor".

8. Acknowledgments

This work was financially supported by the Fundamental Research Funds for the Central Universities (2015NZYQN77).

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