Analysis and validation of low-frequency noise reduction in MOSFET circuits using variable duty cycle switched biasing

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Randomization of the trap state of defects present at the gate Si-SiO$_2$ interface of MOSFET is responsible for the low-frequency noise phenomena such as Random Telegraph Signal (RTS), burst, and 1/f noise. In a previous work, theoretical modelling and analysis of the RTS noise in MOS transistor was presented and it was shown that this 1/f noise can be reduced by decreasing the duty cycle ($f_D$) of switched biasing signal. In this paper, an extended analysis of this 1/f noise reduction model is presented and it is shown that the RTS noise reduction is accompanied with shift in the corner frequency ($f_c$) of the 1/f noise and the value of shift is a function of continuous ON time ($T_{on}$) of the device. This 1/f noise reduction is also experimentally demonstrated in this paper using a circuit configuration with multiple identical transistor stages which produces a continuous output instead of a discrete signal. The circuit is implemented in 180 nm standard CMOS technology, from UMC. According to the measurement results, the proposed technique reduces the 1/f noise by approximately 5.9 dB at $f_s$ of 1 KHz for 2 stage, which is extended up to 16 dB at $f_s$ of 5 MHz for 6 stage configuration.

I. INTRODUCTION

The 1/f noise is a dominant noise source in the low-frequency region and is one of the major bottlenecks in applications like CMOS image sensors. The high noise limits the dynamic range of an image sensor. The primary sources of noise affecting an image sensor pixel are the thermal noise from the switches and the low-frequency 1/f noise from the in-pixel buffer. The thermal noise can be efficiently reduced using correlated double sampling (CDS) and an image sensor with 0.7e$^-$ noise has been reported [1]. The major limiting factor for the dynamic range now is the 1/f noise from the source follower (buffer). An image sensor is a time variant system due to time-varying biasing conditions. The low-frequency noise has an inverse relationship with frequency and aspect ratio of the device, which becomes more prominent with decreasing dimensions of transistors with technology scaling [2]. The decreasing dimensions of the transistors are needed to increase the spatial resolution of an image sensor and thus, reducing 1/f noise becomes more critical in improving the overall performance of a CMOS image sensor.

Random trapping and de-trapping of the charge carriers into the trap defects present at the gate Si-SiO$_2$ interface of MOSFET is believed to be one of the major reasons responsible for the low-frequency noise phenomena such as random telegraph signal (RTS) and 1/f noise [3-5]. There are a few models available which define the 1/f noise conditionally but no model exists which can explain the 1/f noise phenomena completely [6-13]. Hooge’s $\Delta\mu$ model [14] considers that the 1/f noise is caused by fluctuation in carrier mobility inside the bulk of MOS device. Carrier density fluctuation ($\Delta N$) model by McWhorter [15] is based on the variation in the number of charge carriers inside the channel due to random behavior of the trap states present at the interface. This model states that the 1/f noise is a resultant of the RTS noise components from each trap. These traps are bias voltage dependent and have widely distributed emission/capture rates [16] [17]. Due to time-varying biasing conditions, the non-stationarity is introduced in the behavior of the trap state, which makes the RTS noise and consequently the 1/f noise non-stationary.

The 1/f noise in MOS transistors can be reduced by rapidly switching the device between accumulation and strong inversion region [18] [19]. To model the noise for systems with time-varying biasing conditions, a proper stochastic model for trap state is required [18] [20]. H. Tian et al. [27] modeled the random activity of a single trap as a stochastic process and presented the first non-stationary RTS noise model using autocorrelation analysis of trap states in the time domain. The model in [27] [28], predicted that the noise reduction is independent of switching frequency ($f_s$) and concluded that the corner frequency ($f_c$) of the 1/f noise is independent of time-varying emission/capture rates. A. G. Mahmutoğlu et al. [20] found that the limits taken in [27] to calculate the time-averaged autocorrelation function (ACF) for trap state $N(t)$, were incorrect. In [29] and [30], an improved analysis of the RTS noise was presented for switched biasing, using square wave (50% duty cycle ($D$)) as input to a MOS transistor gate. In these and other papers on the low-frequency noise reduction [18] [23] [27] [33] the transistors are switched with either 50% or 25% duty cycle and without multiple stages thereby leading to a discontinuous output.

If the device is kept ON for a shorter duration of time, it is obvious that the total noise will be less than what it would be if the device was always ON but this would lead
to a discontinuous output. What is required is a technique that can lead to noise reduction while keeping the output continuous. In [35], we have proposed to use variable duty cycle with multiple stages of transistors for continuous output and have shown that such configuration can lead to $1/f$ noise reduction. The $1/f$ noise is modeled for a complete range of duty cycle (0 to 100%) of the switched biasing signal and its effect on the overall noise is studied. Decreasing the duty cycle reduces the overall low-frequency noise by reducing the time for which the trap states are correlated. It is additionally shown that if multiple transistors are used with the same duty cycle (so as to ensure a continuous output), the total noise would still be less than what is obtained by using a single transistor which is ON all the time. Thus, if $n$ transistors are ON for time $T/n$ (only one transistor is ON at any given time so as to ensure a continuous output), the total noise keeps decreasing as $n$ increases. This was shown using a mathematical model in our previous paper [35]. In this paper, an extended analysis of this $1/f$ noise model is presented and conclusions are verified with experimental results. A source follower implementation using multiple transistors, is presented to verify the noise reduction while maintaining a continuous time output.

The paper is organized as follows: A brief analysis of the RTS and $1/f$ noise is presented in Section II.A. The mathematical model for RTS noise model with variable duty cycle switched biasing is discussed in Section II.B. The $1/f$ noise reduction method using multiple transistors are described in section II.C. In Section III a circuit level implementation of the variable duty cycle switched biasing is presented using source follower transistor in standard CMOS image sensors. The simulation and experimental results are presented in Section IV. The paper is concluded in section V.

II. $1/F$ NOISE ANALYSIS, MODELING AND REDUCTION TECHNIQUE

A. RTS and $1/f$ noise analysis

In order to understand the nature and mechanism of the RTS noise, the nature of the trap or defect state must be analyzed. Trapping and de-trapping of electrons into a single active trap can be characterized by an electron capture number or trap state $N(t)$, which is “one” when the trap is filled and “zero” otherwise. The probability of the trap being empty or filled is different when the transistor is ON or OFF.

The trap capture rate $\lambda_c(t)$ and emission rate $\lambda_e(t)$ can be given as:

$$\lambda_c(t) = \frac{1 - P(t)}{\tau_c} ; \quad \lambda_e(t) = \frac{P(t)}{\tau_e}, \quad (1)$$

where $P(t)$ is the probability of trap occupancy (PTO) at time $t$. $\tau_c$ and $\tau_e$ are the mean time before capture and mean time before emission of an electron, respectively [36]. $\tau_c$ is inversely proportional to the drain current. On the other hand $\tau_e$ is independent of the drain current. Due to the time-varying nature of the biasing condition and capture/emission meantime, the capture ($\lambda_c$) and the emission ($\lambda_e$) rates of the trap also become time variant [11]. Note that in the above equation, the values of $\tau_c$ or $\tau_e$ are taken from the same distribution as for a stationary model and thus have no influence on the proposed noise reduction technique.

For a continuous ON device with constant biasing, $\lambda_e = \lambda_c = \lambda$, which implies that probabilistically the trap would remain in each state (filled or empty) for approximately $\lambda^{-1}$ time. The value of ACF, for the samples separated by a time interval less than $\lambda^{-1}$ is high and increases as the time difference between samples decreases. This is due to the fact that the probability of the trap being in the same states is higher if the samples are taken within lesser time interval. If the samples are separated by time interval more than $\lambda^{-1}$, the correlation becomes weaker but never quite reaches zero. The ACF for $N(t)$ can be expressed as [9]:

$$C_{\lambda}(\tau) = 0.25e^{-2\lambda \tau}. \quad (2)$$

The double sided PSD corresponding to $C_{\lambda}(\tau)$ can be written as:

$$S_{\lambda}(f) = 0.25\lambda/(\lambda^2 + (\pi f)^2). \quad (3)$$

For stationary case the RTS noise spectrum is Lorentzian which is flat upto corner frequency ($\lambda$) and decays with a slope of -20 dB/decade for sampling frequencies above $\lambda$ (where $\lambda = (\tau_e^{-1} + \tau_c^{-1})/2\pi$). The value of the stationary RTS noise can be given as [31]:

$$S_{RTS}(f) = A_0^2\frac{\beta}{(1 + \beta)^2} \frac{1}{4\pi^2} \frac{\lambda}{(\lambda^2 + (\pi f)^2)}, \quad (4)$$

where $A_0$ is RTS noise amplitude and $\beta = \tau_c/\tau_e$. The RTS noise plots for different values of $\lambda$ are shown in Fig. I(a). The RTS noise decreases for the sampling frequencies below $\lambda$ due to increase in correlation between samples with smaller time interval. Whereas, RTS noise PSD becomes flat for the sampling frequencies below $\lambda$ or corner frequency ($f_c$), due to very weak correlation between the sampled trap states.

The $1/f$ noise representation as a cumulative effect of the RTS noise from each trap is shown in Fig. 1(b). Multiple traps are present at the gate Si-SiO$_2$ interface with widely distributed trapping/de-trapping rates ranging from $\lambda_L$ to $\lambda_H$. Due to these distributed rates, the $1/f$ noise plot can be divided into three different regions as shown in Fig. I(b).

First (i) is the flat region, for the sampling frequencies below $\lambda_L$. The second region (ii) is between the frequency $\lambda_L$ and $\lambda_H$, where few traps are experiencing increasing correlation (reduction in the noise) with frequency while others have flat shaped RTS noise. In this region, the $1/f$ noise curve is proportional to the $f^{-1}$. In the final region (iii) (for the sampling frequencies above the $\lambda_H$), the Brownian noise is proportional to the $f^{-2}$. 

B. Trap noise modeling for transistor with variable duty cycle switched biasing

In [29], the RTS noise PSD is derived for a MOSFET device with switched biasing using square waveform (50% duty cycle) at the gate of the MOSFET as a control input. In [29] it is concluded that the RTS noise reduction depends on the $f_s$. In continuation with our previous work [35], the RTS noise is modeled in a time-varying biasing condition for a more general case, where the duty cycle of switched bias signal varies between 0 and 100%. It is shown that the noise reduction depends on the continuous ON time ($T_{on}$) of the device, which can be controlled by varying the duty cycle ($D$) of the periodically switched biasing signal. It is also concluded that the noise reduction is independent of $f_s$ for constant $T_{on}$. The higher noise reduction can be achieved by decreasing the duty cycle for constant $f_s$, as compared to the model presented in [27, 29, 37]. As the variable biasing condition is periodic, the randomization of a single trap can be modeled by considering its behavior as a cyclo-stationary stochastic process [38]. The capture and emission processes are random and governed by Poisson statistics. This Poisson process is inhomogeneous and exhibits non-stationarity, due to the dependency of $\lambda_c$ and $\lambda_e$ on voltage-dependent variables $\tau_c$ and $\tau_e$.

For switched biasing, $\lambda_c = \lambda_e = \lambda_{on}$ for ON state and $\lambda_c = \lambda_{off}$, $\lambda_e \approx 0$ for OFF state of the device. The value of ACF is almost zero during the OFF state of the device. Switching the transistor OFF between consecutive ON time period, for sufficient time ($\approx \lambda_{off}$), resets the probability of trap occupancy to zero. The value of the PTO is close to zero (during OFF state of the device) due to very high emission rate in the absence of conduction. If the periodic ON time ($T_{on}$) is less than $1/\lambda_{on}$, then the trap state are reset in every $T_{rst} = T_{on} + \lambda_{off}^{-1} \approx T_{on}$ (for $\lambda_{off}^{-1} \ll T_{on}$). Thus, the trap states separated by $T_{rst} \approx T_{on}$ time interval or more, have zero correlation.

For sampling frequencies below $T_{on}^{-1}$, the region in the noise spectrum can be seen in Fig. 2 and above that the trap states are correlated and the switched noise PSD curve overlaps with stationary noise PSD curve [37, 39]. The reduction in the noise occurs by varying correlation due to which the noise PSD becomes flat for the sampling frequencies below $T_{on}^{-1}$ Hz. The corner frequency of the noise is thus limited by $T_{on}$. From the above analysis, it can be stated that the noise reduction increases with a decrease in value of $T_{on}$ or duty cycle of the switched biasing signal and following conclusions can be derived.

1. Decrease in the $1/f$ noise power sampling frequencies above $T_{on}^{-1}$ is due to the increasing correlation between trap states. Due to switching action, the correlation between the samples, separated by more than $T_{on}$ time, becomes very weak. This makes the noise PSD “flat” for the sampling frequencies $T_{on}^{-1}$. Hence, The corner frequency is shifted to a new value of $T_{on}^{-1}$ for $T_{on} < \lambda_{on}^{-1}$, which causes reduction in the noise power.

2. For the trap states of a single transistor sampled during ON time and separated by time interval less than $T_{on}$, have the same correlation as DC biasing condition. Hence, the noise power for sampling frequencies above the $T_{on}^{-1}$ is $10\log(n)$ dB less than the noise power of the stationary noise PSD (reduction of $10\log(n)$ dB in the noise power is due to OFF state of the device).

3. A higher noise reduction can be achieved by lowering the value of $T_{on}$ either by increasing $f_s$ or decreasing duty cycle. If $T_{on}$ is kept constant by suitably varying the duty cycle the obtained noise reduction is also constant for varying $f_s$.

The RTS noise modeling is given as follows:
\textbullet{} The probability of trap being filled in ON state is:

\[ P_{on}(t) = 0.5 + ae^{-2\lambda_{on}t}, \quad \text{for} \quad 0 \leq t < T/n, \]  

(5)

where ‘a’ is a constant which is dependent on the PTO at initial condition \((t = 0)\) of the ON state, ‘T’ is the time period of the biasing signal, ‘n’ is an integer given by \(n = T/T_{on}\).

\textbullet{} The probability of trap to be filled in OFF state is:

\[ P_{off}(t) = be^{-\lambda_{off}t} \quad \text{for} \quad T/n \leq t < T, \]  

(6)

where ‘b’ is a constant which is dependent on the PTO at initial condition of the OFF state.

The value of initial conditions of ‘a’ and ‘b’ can be derived as:

\[ a = -(1 - \beta)/(1 - \alpha\beta); \quad b = (1 - \alpha)/(1 - \alpha\beta), \]  

(7)

where \(\alpha = e^{-2\lambda_{on}T/n}; \quad \beta = e^{-\lambda_{off}(\frac{n-1}{n})T}.\)

In the usual cyclo-stationary noise models only 50% duty cycle and ON time noise PSD is considered. In the OFF state, the traps remain empty due to very high emission rate and negligibly small capture rate. This makes the initial probability of trap occupancy (PTO) at the beginning of ON time to be almost zero, if \(\lambda_{off}T_{off} \gg 1\). In the proposed model, the ON time and OFF time may not be equal, as the OFF time of the device \(T_{off}\) increases as duty cycle decreases. The PTO before commencement of ON time becomes negligibly small \(P_{on}(0) \approx 0\). Thus for ON time PSD the value of variable ‘a’ would be -0.5. The PTO at the initial condition of OFF state is equal to the PTO at time \(T/n\) during ON state which can be calculated by Eq. (5).

The noise PSD during OFF state can be calculated with this initial condition. The PTO decreases exponentially and can be given by Eq. (9). As \(\lambda_{off}\) is very high the PTO at time equal to \(T(n-1)/n\) during OFF state, is negligibly small (considered as zero). Thus, OFF time PSD can be considered as negligible.

From Eqs. (5), (6), and (7), it can be seen that the PTO function depends on capture/emission rates, switching frequency \((1/T)\) and initial condition of the trap state. Using these equations the values of ‘a’ and ‘b’ obtained are -0.5 and 0 respectively, with the assumption that \(\lambda_{on}T_{on} \ll 1\) and \(\lambda_{off}T_{off} \gg 1\) as in [40, 41].

Trap state \(N(t)\) is a cyclo-stationary random process, whose ACF is given by [42]. During ON state:

\[ C_{\lambda_{on}}(t, \tau) = (1/4)e^{-2\lambda_{on}|\tau|} - a^2 e^{-4\lambda_{on}t}. \]  

(8)

The double sided PSD of the RTS noise of a single trap is calculated using the Fourier transform of the ACF during the ON time period of the transistor.

\[ S_{\lambda_{on}}(\omega) = \mathcal{F}[C_{\lambda_{on}}(\tau)], \]  

(9)

where \(C_{\lambda_{on}}(\tau)\) is the time average values of \(C_{\lambda_{on}}(t, \tau)\).

\[ S_{\lambda_{on}}(\omega) = \frac{1/4T}{(4\lambda_{on}^2 + \omega^2)} \left[ \frac{4T\lambda_{on}}{n} - A - \frac{Be^{-2\lambda_{on}T}}{4\lambda_{on}^2 + \omega^2} \right], \]  

(10)

\[ A = a^2 e^{-4\lambda_{on}T/n} + (16a^2 + 8)\lambda_{on}^2 + a^2 4\omega^2 - 2\omega^2, \]  

\[ B = (40a^2 + 6)\lambda_{on}^2 \cos \left(\frac{\omega T}{n}\right) - 8\omega \lambda_{on} \sin \left(\frac{\omega T}{n}\right). \]

In a similar way the noise PSD \(S_{\lambda_{off}}(\omega)\), for OFF state, can also be calculated by taking Fourier transformation of time average of \(C_{\lambda_{off}}(t, \tau)\). In this work, a variable duty cycle is used for biasing signal in which OFF time is higher. As OFF time increases the probability of trap to be empty is high due to higher \(\lambda_{off}\), and to get filled again is very low as \(\lambda_{on}\) is very low [40, 41]. Thus, the noise in OFF state of the device can be neglected and the RTS noise PSD can be given as:

\[ S_{\lambda_{off}}(\omega) \approx S_{\lambda_{on}}(\omega). \]  

(11)

According to Eq. (10) the RTS noise PSD of a single trap is a function of the duty cycle of the switched bias signal \((T/n)\), emission/capture rate, and initial condition of PTO during ON time.

The 1/f noise is calculated by superposition of the noise generated by individual traps with different capture/emission rates. The overall 1/f noise PSD is given by [19]:

\[ S(\omega) = \int_{\lambda_L}^{\lambda_H} S_{\lambda}(\omega)g(\lambda)d\lambda. \]  

(12)
where \( g(\lambda) \) is the distribution function of the emission and capture rate, \( \theta \) is the absolute temperature in Kelvin, \( k \) is Boltzmann constant, \( A \) is the channel area (1 \( \mu m^2 \)), \( t_{ox} \) is the effective gate oxide thickness (10 nm), \( N_t \) is the trap density, \( \lambda_H \) and \( \lambda_L \) are the fastest and slowest transition rates, respectively. These rates are related to \( t_{ox} \) through the equation \( \log(\lambda_H / \lambda_L) = \gamma t_{ox} \), where \( \gamma \) is the tunneling constant. The 1/f noise voltage PSD is given by:

\[
S_{1/f}(\omega) = \left( \frac{q}{AC_{ox}} \right)^2 S(\omega),
\]

where \( C_{ox} \) is the unit area channel capacitance and \( q \) is electron charge.

Equations (10), (11), and (14) are valid for the entire range of sampling frequency including the frequencies below and above the switching frequency. The entire range is selected to verify if the noise reduction due to duty cycling with multiple stages happens at all frequencies or only at specific frequencies. In our analysis, the noise reduction is observed only for frequencies below the corner frequency. Above the corner frequency, the noise remains 10log\((n)\) dB less than the stationary noise due to OFF state.

### C. 1/f noise reduction by using multiple transistors with varying duty cycle switched biasing

As discussed in section II B, the 1/f noise PSD decreases with a decrease in the duty cycle \( (D) \) of the switched biasing signal. The derived model is also validated as higher RTS noise reduction can be obtained with an increase in the values of ‘n’, as per (11). Multiple transistors are connected between the input and the output wherein the noise contribution of each transistor is assumed to be non-correlated. Thus overall 1/f noise PSDs would be the summation of the noise PSDs of each source follower and is given as:

\[
S_{\lambda^{/p}}(\omega) = n \times S_{1/f}(\omega),
\]

where \( S_{1/f}(\omega) \) is the worst case noise PSD of each stage. In [8], \( \lambda_{on} = 10^8 \) Hz, \( \lambda_{off} = 10^{-20} \) Hz, and \( T = 10^{-11} \) s (with 50% duty cycle) is selected such that \( \lambda_{off}T_{off} >> 1 \) and \( \lambda_{on}T_{on} << 1 \). The reason behind these limitations can be explained from the analysis shown in section II B. If \( \lambda_{on}T_{on} << 1 \), trap states are getting reset by switching. However, \( \lambda_{off} \) and \( \lambda_{on} \) depend on time, biasing voltage and are different for each trap. \( \lambda_{off}T_{off} >> 1 \) is true only when \( T_{off} \) and \( \lambda_{off} \) are very large. If this condition does not hold, then there may be a non-zero probability of trap to remain filled until the starting of the next ON time of the transistor. If the initial PTO for ON state of the device is not zero, the noise PSD does not remain the same as in [29].

Initial PTO of ON state of the device would be zero only if enough OFF time is available for emission, which can be achieved by reducing the duty cycle of the biasing signal as per Eq. (5). Reduction in duty cycle results in the higher noise reduction as per Eq. (10). In Fig. 2 comparison is shown between stationary PSD and switched PSD based on the models proposed in [27, 29], and this work. The model, shown in [27] predicts 33 dB reduction in the RTS noise PSD as compared to the standard model, whereas in [29] a noise reduction of 86 dB is claimed. As predicted in Eq. (15), if \( n \) increases from 2 to 4 (the duty cycle changes from 50% to 25%) additional 9 dB reduction is obtained which further increases up to 27 dB for \( n = 16 \).

Based on the above analysis, a circuit level noise reduction technique is proposed for the source follower transistor in standard CMOS image sensors. The switching activity makes the output discrete in nature, which is not suitable for image sensor applications. Complementary switches are used to obtain a continuous output in [43]. The two MOSFET switches are periodically switched between strong inversion and accumulation or depletion regions which lead to a reduction in the low-frequency noise. The model in [9] is limited to two switches, which is extended to multiple transistors configuration (in this work), with higher noise reduction.

### III. DETAILED CIRCUIT IMPLEMENTATION

A source follower (SF) or buffer stage is implemented as a test circuit, using multiple transistors with a variable duty cycle switched biasing. The source follower is used to show the reduction of 1/f noise reduction in an active pixel sensor (APS). A conventional APS employs three or more transistors where all transistors, except the SF, act like a switch. The switches mostly contribute to the thermal noise, while the SF contributes to the low-frequency noise. The SF low-frequency noise is becoming more evident as transistor sizes are becoming smaller with technology scaling. The thermal noise in the pixel can be reduced using CDS [46]. In CDS, first a reset signal is sampled and after the integration period of the photons, the signal is sampled. In CDS, the reset sample is subtracted from the signal and since the thermal noise components of both signals are correlated, the overall thermal noise gets reduced. However due to the increased time period of sampling the reset and the signal, the low-frequency noise becomes uncorrelated and thus the overall low-frequency noise increases. Thus, the 1/f noise remains as a dominant source of the noise at the imager output and must be reduced to improve the overall signal-to-noise ratio.

The implemented circuit is shown in Fig. 3(b) in which multiple transistors are used to implement single stage
FIG. 3: (a) Single transistor source follower, (b) SF action achieved through multiple transistors with programmable ring counter, and (c) Timing diagram.

FIG. 4: The switched bias RTS noise PSD for single transistor, calculated from derived model given in Eq. [10] [MATLAB simulation], with variable duty cycle (D) to demonstrate (a) Equal shift in $f_c$ for equal ON time ($T_{on}$) = $5 \times 10^{-11}$ s; (b) Different shift in $f_c$ with variable $T_{on}$ and equal time period ($T$) or switching frequency ($f_s = 1/T$); and (c) Relationship between $f_c$ and $T_{on}$.

For switched biasing, a programmable ring counter is used to generate non-overlapping clocks with a desired duty cycle, as shown in Fig. 3(b) and (c). The high level of the clock corresponds to the input voltage ($V_{in}$). The

buffer/amplifier, to reduce the low-frequency noise. The purpose of multiple and identical stages is to retrieve the continuous signal at the output of the system which uses switched biasing. The output signal is discrete in nature due to switched biasing and the time for which signal is available at the output is decreased with a decrease in the duty cycle. To retain the continuous nature of the output, multiple stages are used, as shown in Fig. 3(b), which is an example of switched bias multiple transistor source follower. Individual source followers, among the multiple paths, are selected periodically for a small interval of time as shown in Fig. 3(c). Thus, among multiple paths, only one path from input to the output is ON at a given time. Since one path is always ON between the input and the output, the output remains continuous. If each transistor is ON for $T_{on} = T/n$ time in a time period $T$, to achieve a continuous output, ‘$n$’ number of stages would be required such that one stage is ON at a time. Thus, in this paper ‘$n$’ is number of stages and used for $T_{on} = T/n$, duty cycle ($D$) = $100 \times T/n$ %.
programmable ring counter can be configured to select a variable number of stages. The ring counter activates one transistor at a time. The frequency of the counter can be controlled by an external clock, thus, allowing for varying the duty cycle of each transistor, externally. As only one transistor is ON at a time in the input to the output path, the noise generated from each stage is non-correlated. Thus, the overall noise at the output is equal to the additon of the noise power of each stage transistor. This non-correlated noise sampling is one of the major keys behind the total noise reduction.

IV. RESULTS

A. Simulation results

Equation (15) is evaluated using MATLAB to demonstrate reduction in the 1/f noise. It is evident from the evaluated results, shown in Fig. 4, that the RTS noise PSD experiences an equal shift in $f_c$ for equal $T_0$ with different switching frequencies. The RTS noise PSD is plotted for stationary noise (DC biasing) [10], switched noise PSD based on stationary noise model [27], and the noise PSD from the model presented in this paper. Figure 4(a) shows the RTS noise power evaluated from Eq. (10) for different values of time period ($T$) and $T_0$ (= $T/n$). For calculations the value of $\lambda_{on}$ has been chosen as $10^8$ Hz. The RTS noise is plotted for $T$ varying from $10^{-6}$ s to $10^{-10}$ s and for each value of $T$, $T_0$ is kept equal to $5 \times 10^{-11}$ s by adjusting the value of $n$. From Fig. 4 it can be observed that for each case the $f_c$ is shifted to approximately $T_0^{-1}$.

In Fig. 4(b) the RTS noise evaluated from Eq. (10) is plotted for varying values of $T_0$ from $5 \times 10^{-7}$ s to $5 \times 10^{-10}$ s while keeping $T = 10^{-5}$ s. As predicted in section III-C for the noise plots with $T_0^{-1} < \lambda_{on}$, the corner frequency doesn’t shift and remains approximately equal to $\lambda_{on}$ ($10^8$ Hz). For these plots the noise power reduces by ‘$n$‘ time as compared to stationary noise. Hence, there is no reduction in the RTS noise. While for the plots with $T_0^{-1} \geq \lambda_{on}$ the corner frequency shifts to $T_0^{-1}$ and the reduction in noise is higher than ‘$n$’ time as compared to stationary noise. A higher shift in the $f_c$ accompanies a higher reduction in the low-frequency noise. It can be concluded from the results that the noise reduction depends on the $T_0$ rather than $T$ or $f_c$. Thus, the same reduction can be achieved by switching the transistor at a comparatively lower frequency by decreasing the duty cycle of switching signal. The relation between $T_0^{-1}$ and $f_c$ is plotted in Fig. 4(c).

Equation (10), thus shows an increased RTS noise reduction with decrease in duty cycle ($100T/n$) or increase in value of ‘$n$’. The reduction in the noise is more than $10\log(n)$. Hence, when multiple transistors are used with the same duty cycle to ensure a continuous output, the total noise (with non-correlated noise components from multiple stages) would be less than what is obtained by using a single transistor which is ON all the time. This was shown using a mathematical model in our previous paper [35]. The RTS noise PSD of single stage ($S_{\lambda, on}(\omega)$) and multiple stages ($n \times S_{\lambda, on}(\omega)$) with variable duty cycle is shown in Fig. 5(a). The figure shows that the RTS noise PSD decreases with decrease in duty cycle or increasing the number of stages.

In Fig. 5(b), the 1/f noise PSD evaluated from Eq. (12) with the multiple stages is compared with the noise...
PSD from the standard model (stationary noise model), and other models reported in [27] and [29]. Greater noise reduction is obtained, as shown in the figure, as compared to other models while the output is still continuous in nature. As the number of stages is increased from 2 to 4, an additional 1/f noise reduction of 3 dB is observed, while the RTS noise reduction obtained is 9 dB, as in Fig. 2. When the number of stages is increased from 2 to 16 an additional 1/f noise reduction of 10 dB is achieved. 

The model, given in [27] claimed to obtain the lower noise power at higher frequencies, due to incorrect boundary conditions used. The 1/f noise evaluated from Eq. (15) is shown in Fig. 8 for varying time period from 1 KHz to 5 MHz and the number of transistor stages from 2 to 6. The stationary noise has also been plotted in the figure for comparison. At 100 Hz sampling frequency and \( f_s = 1 \) KHz, the 1/f noise reduction obtained is 17.44 dB, 19.2 dB, 20.45 dB, 21.42 dB, and 22.21 dB for 2, 3, 4, 5, and 6 stages, respectively. This increases to 54.74 dB, 56.6 dB, 58.05 dB, 59.12 dB, and 60.21 dB for 2, 3, 4, 5, and 6 stages, respectively for 100 Hz sampling frequency and \( f_s = 5 \) MHz. As the \( T_{on} \) decreases with increase in the number of stages and \( f_s \) both, it can be concluded from the results, evaluated from the derived equations, that 1/f noise reduction depends on the \( T_{on} \) and independent of \( f_s \) when \( T_{on} \) is kept constant.

The noise PSD for multiple stage configuration, generated by the periodic steady state (PSS) and noise analysis from Spectre simulator by Cadence IC-615, is shown in Fig. 7. The MOSFET model used is Star-Hspice level 49 (BSIM3V3.2) with UMC 0.18um Mixed-mode/RFCMOS 1.8V 1P6M P-sub twin-well CMOS salicide process. The different graphs (a), (b), and (c) show the noise results for switching frequencies of 1 KHz, 100 KHz, and 1 MHz respectively. According to simulation results, a total reduction in the noise power is 10log(n) dB for n stage configuration. It can be seen in the graphs that corner frequency shifts to \( f_s \) and the noise reduction is almost constant, which is different from the results obtained from Eq. (12).

### B. Measurement results

The measurement setup is similar to that reported in [44,45]. The low noise SR570 current preamplifier is used to provide the biasing current to the test circuit and to amplify the noise power. As shown in Fig. 8(b) the drain to source voltage \( V_{DS} \) (or \( V_{bias} \)) of test transistors, is equal to \( V_{ref} \) of the preamplifier. The value of \( V_{DS} \) can thus be set to a desired value by varying \( V_{ref} \) to keep transistors in saturation region during ON state. The noise current generated from the test circuit is amplified by \( R_{gain} \), to produce the noise voltage at the output of the preamplifier. The current to voltage sensitivity of the preamplifier was set at 10 \( \mu A/V \) to get amplified noise voltage at the output. The input referred noise of current preamplifier is as low as 5 \( fA/\sqrt{Hz} \), which makes it quite suitable for precise noise measurement. The preamplifier noise signal voltage is fed into the SR785 dynamic signal analyzer (DSA). DSA plots the Fourier transform of the noise voltage signal coming from the preamplifier. The input referred noise of DSA is as low as -160 dBVrms/\( \sqrt{Hz} \) and the maximum bandwidth is 102.4 KHz. The noise PSD is plotted with 400 line FFT resolution and 400 Hz span to set 1 Hz frequency resolution. The span of the dynamic signal analyzer was kept as 400 Hz with 400 line FFT. As the maximum frequency was 400 Hz, the sampling rate is 1024 samples/sec with 1024 number of points in a time record. Dynamic signal analyzer is employed with a digital anti-aliasing filter with variable cut off frequency. The cut off frequency of the filter depends on the span of FFT spectrum. The time record length also depends on the span of the spectrum. After sampling, an anti-aliasing filter is used which suitably rejects the out-of-band spectral components. In the measurement cutoff frequency of the digital low-pass filter contained is 512 Hz with flat response upto 400 Hz and roll-off from 400 Hz to 512 Hz. To improve the measurement accuracy, each noise PSD curve is plotted after taking an RMS average of 100 measured samples.

The DUT has a configurable ring counter which generates non-overlapping clocks (\( clk_{k1}, clk_{k2},..., \text{and} \ clk_{kn} \)) to select one MOS transistor at a time, as described in section III. Non-overlapping clocks make sure that the noise components from different stages are non-correlated. The noise measurements for DC biasing are carried out with \( V_{DS} = V_{GS} = 1 \) V for nMOS transistors. For switched biasing, \( V_{DS} = V_{GS} \) is set to 1 V during ON time to keep transistors in the saturation region while \( V_{GS} = 0 \) V for OFF time to keep the transistor in cutoff region. First, the noise measurements are carried out on a single transistor with constant biasing. Then measurement are carried out for single as well as multiple transistors, with switched biasing and a variable duty cycle (D). The noise power at the output node for the circuit shown in Fig. 3(b) can be calculated by MOSFET noise current (\( I_{DS,n} \)) (the noise current flows from drain to source of the device) and the load resistance. The load resistance only contributes thermal noise, thus 1/f noise can be analyzed by measuring the noise current \( I_{DS,n} \) at low frequencies. The measurement setup, shown in Fig.
TABLE I: Summary of Anticipated Reduction in The Noise power for Multiple Stage Transistor from The Measured Noise of Switched Biased single Transistor

| $n$ | 6 | 4 | 3 | 2 | 6 | 4 | 3 | 2 | 6 | 4 | 3 | 2 |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|
| $T = 10^{-3}$ s | 100 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 |
| $T = 10^{-5}$ s | 100 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 |
| $T = 10^{-6}$ s | 100 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 | 16.6 | 25 | 33.3 | 50 |

$T = \text{Time period;}$; $n = \text{Number of stages;}$; $D = \text{Duty cycle [%];}$ $f_m = \text{Sampling frequency [Hz].}$
FIG. 8: [Color online] (a) Measurement setup for design under test (DUT) (b) Chip microphotograph.

FIG. 9: Measurement results for the switched bias 1/f Noise PSD for single stage configuration with a variable duty cycle (D) or continuous ON time ($T_{on}$) with (a) $T = 10^{-3}$ s, (a) $T = 10^{-5}$ s, (a) $T = 10^{-6}$ s, and (d) $T = 5 \times 10^{-7}$ s.

From the noise measurement results obtained by DSA, the reduction in the noise current of DUT are an-
The measured noise power of a single stage transistor with constant and switched biasing is shown in Fig. 9. The noise plots, shown in Fig. 9(a), (b), (c), and (d) demonstrates the reduction in the low-frequency noise power of single transistor, switched bias at $f_s = 1 \text{ KHz}$, $100 \text{ KHz}$, $1 \text{ MHz}$, and $5 \text{ MHz}$ respectively. For each $f_s$, the duty cycle is taken as 16.6\%, 20\%, 25\%, and 50\%. The average reduction in $1/f$ noise power for single stage configuration with varying duty cycle, (for sampling frequency up to 40 Hz and $f_s = 1 \text{ kHz}$) evaluated from Eq. (12), using MATLAB simulation, is 29.57 dB, when the duty cycle varies from 100\% (DC biasing) to 50\%. After which when the duty cycle reduces to 25\%, 20\% and 16.6\% the average noise reduction increases to 35.5 dB, 37.6 dB, and 39.11 dB, respectively. While the measurement results (Fig. 9) shows an average reduction obtained in $1/f$ noise, for $f_s = 1 \text{ KHz}$ is 7.02 dB when the duty cycle varies from 100\% to 50\%. As the duty cycle further reduces to 25\%, 20\% and 16.6\%, the noise reduction increases to 15.5 dB, 17.3 dB, and 18.72 dB respectively. The sampling frequency has been chosen only up to 40 Hz, to show the low-frequency noise reduction.

As discussed in section II C, the low-frequency noise can be reduced using variable duty cycle and multiple stages. The noise from each of these stages are non-correlated in nature; hence, the overall noise PSD at the output can be calculated by summing the noise power from an individual stage. In order to compare the noise from single stage transistor with DC biasing and a vary-
ing duty cycle switched biasing, a factor of $10\log_{10}(D)$ is added into the later. By this addition, the noise from multiple stage configuration is predicted and summarized in Table II.

The measured noise power sampled at frequency points at 10 Hz, 40 Hz, 270 Hz, and 380 Hz for varying $f_s$ and $D$, as given in Table II. The noise reduction with multiple stages (calculated from the switched noise PSD of single transistor) should vary from 4.2 dB with 50% duty cycle to 12.3 dB with 16.6% duty cycle at 10 Hz sampling frequency, while the reduction should be 0.4 dB with 50% duty cycle to 4.8 dB with 16.6% duty cycle at 380 Hz sampling frequency, for $f_s = 1$ KHz. The random points are selected to avoid the effects of spikes generated due to power supply noise at 50 Hz and its harmonics. It can be concluded from the summary given in Table II that the noise power decreases with a decrease in the duty cycle at a given $f_s$. The same trend is seen when the $f_s$ is increased while the noise reduction decreases for higher sampling frequencies. The decrease in the noise reduction at higher sampling frequencies is due to the dominance of the thermal noise over low-frequency noise above $f_c$.

The measured noise power of single stage nMOS with constant biasing and multiple nMOS transistors with switched biasing, for a varying duty cycle, is shown in Fig. 10. The output noise power for 2 to 6 stages, switched with $f_s = 1$ KHz, 100 KHz, 1 MHz, and 5 MHz are presented in Fig. 10(a), (b), (c), and (d) respectively. For the measurements, the ring counter is configured to select 2 to 6 transistor stages, as shown in Fig. 3(b). $f_s$ is varied from 1 KHz to 5 MHz for a variable number of stages. The duty cycle is varied from 50% to 16.6% for 2 to 6 transistor stages. From the measured results variation can be seen in the integrated noise reduction (for sampling frequency up to 40 Hz) from 5.9 dB, for 2 stages to 12.3 dB, for 6 stages, with $f_s = 1$ KHz. Reduction in the noise is increased with increase in a number of stages (or decrease in the duty cycle) and $f_s$. In both the cases, the noise reduction is increased due to the decrease in continuous ON time of the transistor, as predicted by Eq. (10).

By comparison, between the results shown in Table II (the predicted noise power of 'n' stages configuration from the measured noise for single stage with variable duty cycle by adding $10\log_{10}(n)$ dB) and Fig. 10 (measured noise of multistage configuration), it can be seen that reduction in the noise power, with $f_s = 1$ KHz, should be 4.2 dB for 2 transistor stages to 12.3 dB for 6 stages (at 10 Hz sampling frequency) and 0.4 dB for 2 stages to 4.8 dB for 6 stages (at 380 Hz sampling frequency). While the measured noise reduction obtained is 3.9 dB for 2 stage to 11.2 dB for 6 stage configuration (at 10 Hz sampled frequency) to 0.7 dB for 2 stages to 5.7 dB for 6 stages (at 380 Hz sampling frequency). The comparison shows that the low-frequency noise power of multistage configuration is approximately same as calculated from the noise of single transistor with a variable duty cycle switched biasing. The reason of the small difference in the noise powers is the presence of other circuits like ring counter and switched transistors.

The average reduction in the $1/f$ noise power (for sampling frequency up to 40 Hz) is summarized in Table II and Fig. 11, for $f_s = 1$ KHz, 100 KHz, 1 MHz, and 5 MHz. The $1/f$ noise power calculated by Eq. (15) (the noise PSD shown in Fig. 6) predicts the average reduction varies from 24.8 dB to 31.32 dB when the number of stages vary from 2 to 6, for $f_s = 1$ KHz. It can be concluded from results that the $1/f$ noise power depends on the continuous ON time of the device rather than $f_s$. For higher sampling frequencies the switched bias noise PSD is approximately equal to the stationary noise PSD, as the thermal noise start dominating above the $1/f$ noise corner frequency.

One drawback of using multiple transistors with switched biasing is that switching action of the transistors introduces ripples at the output. These ripples are generated due to clock feed-through of the overlapping capacitance present between drain and gate of the switching transistor. The ripples can be filtered out through a switch capacitor low-pass filter. The low pass filter can be placed in the column of the CMOS image sensor, which will not affect the fill factor of the pixel. The mismatch of the source followers would increase the column FPN. The column FPN needs to be characterized with an imaging array in place. The focus of this work is to show the noise reduction obtained using multiple stages as compared to simply duty cycling a single device. In future, an imaging array with the proposed low-frequency noise reduction method will be fabricated and the effects of multiple source followers on the column FPN and other imaging performance will be characterized.
TABLE II: Summary of The 1/f Noise Power (Measured) Reduction with Multistage Configuration at varying switching frequencies

| No. of stage \( (n) = \) | 6 | 5 | 4 | 3 | 2 |
|--------------------------|---|---|---|---|---|
| \( f_s \downarrow \) | Reduction in the Noise Power in \( V^2/Hz \) [dB] |
| 1KHz | 12.3 | 11.4 | 10.4 | 7 | 5.9 |
| 100KHz | 12.9 | 12.5 | 11.2 | 7.6 | 5.93 |
| 1MHz | 14 | 12.5 | 11.7 | 9.7 | 6 |
| 5MHz | 16 | 14.3 | 13.4 | 10 | 6.1 |

FIG. 12: ACF plots for the theoretical calculated and measurement data

V. DISCUSSION AND CONCLUSION

In this paper, a mathematical model of the RTS noise, for a MOSFET device with time-varying biasing conditions, is presented. It is concluded that the RTS noise and consequently the 1/f noise of an MOS transistor decreases with a decrease in the \( T_{on} \). It is shown that reduction in the noise occurs due to varying correlation between trap states which is a function of \( T_{on} \) rather than switching frequency. Based on this conclusion a circuit level low-frequency noise reduction technique is presented. It is observed by measurement that the noise reduction which is 5.9 dB with \( f_s = 1 \) KHz for 2 stage is extended up to 16 dB for 6 stages with \( f_s = 5 \) MHz.

The nature of the low-frequency noise measurement results presented in this paper is similar to the results given in literature. There is some discrepancy in the low-frequency noise behavior between the measurement results shown in Fig. 9 and 10 and the theoretical results shown in the Fig. 6. As per the theoretical results the noise PSD is flat for low frequencies while, the measurement results show a decreasing profile. There are two possible reasons for the discrepancy between theoretical and measured results. Firstly, the ACF calculated in the theory and the autocorrelation obtained from the measurements are different. Secondly, there is a reappearance of 1/f noise in the low frequency region.

In Fig. 12 the theoretical ACF given by Eq. (8) is plotted for a device which is ON for \( T_{on} \) time period during a time interval of \( T \). This graph has been compared with the ACF calculated for the experimentally measured noise data with 50% and 25% duty cycles. The measurement ACF is obtained from the measured noise samples. There are mainly two important differences between these ACF plots which could be the reason for the discrepancy observed between the theoretical and measured FFT plots:

- The experimentally obtained curve is not as smooth as the theoretically obtained curve which also causes discrepancy in the nature of PSD plots.
- It can be seen that the theoretical correlation plot has non-zero values only for time samples between \(-T_{on}\) to \(T_{on}\). However, the experimentally obtained correlations are non-zero beyond this range.

The other reason for the discrepancy is the reappearance of the 1/f noise. This effect has been discussed in [29 - 32]. Our model is based on the assumption that \( \lambda_{off} T_{off} \gg 1 \), as \( \lambda_{off} \) is very high for all traps. However, this condition need not be true for all traps, and thus all traps might not be affected uniformly in OFF condition during switching. The distribution of \( \lambda_{off} \) depends on a space dependent parameter \( 'm' \) [32]. Emission rate during off time is not uniform and can be given as:

\[
\lambda_{off} (emission) = m.\lambda_{on} (emission)
\]  

(16)

The value of \( 'm' \) needs to be \( \infty \) to ensure that the trap is empty during OFF state. However \( 'm' \) is not uniform
among all traps as it depends on the location of the trap with respect to the surface of the channel \[31, 32\]. The value of ‘m’ is less for slow traps which are located away from the channel surface. If ‘m’ for a trap is small enough to make sure that \( \lambda_{\text{off}} T_{\text{off}} \ll 1 \), then it’s state (filled or empty) does not change with switching and hence, the noise PSD from these traps represents the noise similar to the stationary case which decreases with increase in frequency. Hence, another factor is added in the expression of the noise PSD to take account of the reappearance of the noise similar to the channel surface \([31, 32]\). The value of ‘m’ is less for slow traps which are located away from the channel surface. If ‘m’ for a trap is small enough to make sure that \( \lambda_{\text{off}} T_{\text{off}} \ll 1 \), then it’s state (filled or empty) does not change with switching and hence, the noise PSD from these traps represents the noise similar to the stationary case which decreases with increase in frequency. Hence, another factor is added in the expression of the noise PSD to take account of the reappearance of the noise similar to the channel surface \([31, 32]\).

As for ON state of transistor \( \lambda_{c} \approx \lambda_{v} \approx \lambda_{\text{on}} \), the probability of a capture or emission event in \( \Delta t \) time is equal to \( \lambda_{\text{on}} \Delta t \) and if \( \Delta t \) is infinitesimally small, \( 17 \) can be simplified as:

\[
\frac{dp_{\text{on}}(t)}{dt} + 2p_{\text{on}}(t)\lambda_{\text{on}} = \lambda_{\text{on}}. \quad (A2)
\]

\[
P_{\text{on}}(t) = 0.5 + ae^{-2\lambda_{\text{on}}t}, \quad 0 \leq t < T/n, \quad (A3)
\]

where ‘a’ is the initial PTO during ON time.

Similarly \( p_{\text{off}}(t) \) is the PTO at time \( t \), during OFF time of the device. As \( p_{\text{off}}(t) \) is also a time-varying function, the probability of any event in infinitesimally small time interval \( \Delta t \), can be given as:

\[
p_{\text{off}}(t+\Delta t) = p_{\text{off}}(t).(1-\lambda_{c}f f \Delta t). \quad (A5)
\]

\[
p_{\text{off}}(t+\Delta t) = p_{\text{off}}(t).l_{\text{on}}.t(t-1)/n_{\text{on}}.t < T/n \quad \text{for} \quad T/n < t < T, \quad (A7)
\]

with ‘b’ is the constant depends on the PTO at initial condition of the OFF state of transistor. The value of ‘a’ and ‘b’ can be arrived as:

\[
a = -b/1-b; \quad b = (1-a)/1-b; \quad (A8)
\]

where \( \alpha = e^{-2\lambda_{\text{on}}T/n}, \quad \beta = e^{-\lambda_{\text{off}}(T/n)T/n}. \quad (A9)\]

In order to calculate the ACF function for trap state \( N(t) \), it is necessary to calculate condition probability of trap to be filled at time \( t + \tau \), with the condition that \( p(t) = 1 \) (applicable for both ON as well as OFF time).

This way conditional probabilities for trap occupancy at some arbitrary time \( t + \tau \), with the condition that trap is full at time \( t \), is:

\[
P_{\text{on},11}(t) = \frac{1}{2}(1 + e^{-2\lambda_{\text{on}}|\tau|}), \quad 0 \leq t < T/n, \quad t \geq 0, \quad (A9)
\]

\[
P_{\text{off},11}(t) = e^{-\lambda_{\text{off}}|\tau|}, \quad 0 \leq t < (T-1)/n, \quad t \geq 0, \quad (A10)
\]

Derivation of time averaged ACF function \( C_{\lambda}(t, \tau) \) of \( N(t) \) for ON and OFF time of transistor:

\[
C_{\lambda}(t, \tau) = E[N(t-\tau/2)\cdot N(t+\tau/2)] -E[N(t-\tau/2)]E[N(t+\tau/2)], \quad (A11)
\]

\[
\int_{\Delta} p_{\text{off}}(t+\Delta t) = p_{\text{off}}(t).(1-\lambda_{c}f f \Delta t). \quad (A5)
\]

As for ON state of transistor \( \lambda_{c} \approx \lambda_{v} \approx \lambda_{\text{on}} \), the probability of a capture or emission event in \( \Delta t \) time is equal to \( \lambda_{\text{on}} \Delta t \) and if \( \Delta t \) is infinitesimally small, \( 17 \) can be simplified as:

\[
\frac{dp_{\text{on}}(t)}{dt} + 2p_{\text{on}}(t)\lambda_{\text{on}} = \lambda_{\text{on}}. \quad (A2)
\]

\[
P_{\text{on}}(t) = 0.5 + ae^{-2\lambda_{\text{on}}t}, \quad 0 \leq t < T/n, \quad (A3)
\]

where ‘a’ is the initial PTO during ON time.

Similarly \( p_{\text{off}}(t) \) is the PTO at time \( t \), during OFF time of the device. As \( p_{\text{off}}(t) \) is also a time-varying function, the probability of any event in infinitesimally small time interval \( \Delta t \), can be given as:

\[
p_{\text{off}}(t+\Delta t) = p_{\text{off}}(t).\lambda_{\text{on}}.t(t-1)/n_{\text{on}}.t < T/n \quad \text{for} \quad T/n < t < T, \quad (A7)
\]

with ‘b’ is the constant depends on the PTO at initial condition of the OFF state of transistor. The value of ‘a’ and ‘b’ can be arrived as:

\[
a = -b/1-b; \quad b = (1-a)/1-b; \quad (A8)
\]

where \( \alpha = e^{-2\lambda_{\text{on}}T/n}, \quad \beta = e^{-\lambda_{\text{off}}(T/n)T/n}. \quad (A9)\]

In order to calculate the ACF function for trap state \( N(t) \), it is necessary to calculate condition probability of trap to be filled at time \( t + \tau \), with the condition that \( p(t) = 1 \) (applicable for both ON as well as OFF time).

This way conditional probabilities for trap occupancy at some arbitrary time \( t + \tau \), with the condition that trap is full at time \( t \), is:

\[
P_{\text{on},11}(t) = \frac{1}{2}(1 + e^{-2\lambda_{\text{on}}|\tau|}), \quad 0 \leq t < T/n, \quad t \geq 0, \quad (A9)
\]

\[
P_{\text{off},11}(t) = e^{-\lambda_{\text{off}}|\tau|}, \quad 0 \leq t < (T-1)/n, \quad t \geq 0, \quad (A10)
\]

Derivation of time averaged ACF function \( C_{\lambda}(t, \tau) \) of \( N(t) \) for ON and OFF time of transistor:

\[
C_{\lambda}(t, \tau) = E[N(t-\tau/2)\cdot N(t+\tau/2)] -E[N(t-\tau/2)]E[N(t+\tau/2)], \quad (A11)
\]

For OFF state of transistor, the probability of trap to capture an electron is almost zero, as the number of charge carriers are negligible, then \( \lambda_{c} \approx 0 \) and \( \lambda_{c} = \lambda_{\text{off}} \),

\[
p_{\text{off}}(t+\Delta t) = p_{\text{off}}(t).l_{\text{on}}.t(t-1)/n_{\text{on}}.t < T/n \quad \text{for} \quad T/n < t < T, \quad (A7)
\]

where ‘b’ is the constant depends on the PTO at initial condition of the OFF state of transistor. The value of ‘a’ and ‘b’ can be arrived as:

\[
a = -b/1-b; \quad b = (1-a)/1-b; \quad (A8)
\]

where \( \alpha = e^{-2\lambda_{\text{on}}T/n}, \quad \beta = e^{-\lambda_{\text{off}}(T/n)T/n}. \quad (A9)\]

In order to calculate the ACF function for trap state \( N(t) \), it is necessary to calculate condition probability of trap to be filled at time \( t + \tau \), with the condition that \( p(t) = 1 \) (applicable for both ON as well as OFF time).

This way conditional probabilities for trap occupancy at some arbitrary time \( t + \tau \), with the condition that trap is full at time \( t \), is:

\[
P_{\text{on},11}(t) = \frac{1}{2}(1 + e^{-2\lambda_{\text{on}}|\tau|}), \quad 0 \leq t < T/n, \quad t \geq 0, \quad (A9)
\]

\[
P_{\text{off},11}(t) = e^{-\lambda_{\text{off}}|\tau|}, \quad 0 \leq t < (T-1)/n, \quad t \geq 0, \quad (A10)
\]

Derivation of time averaged ACF function \( C_{\lambda}(t, \tau) \) of \( N(t) \) for ON and OFF time of transistor:

\[
C_{\lambda}(t, \tau) = E[N(t-\tau/2)\cdot N(t+\tau/2)] -E[N(t-\tau/2)]E[N(t+\tau/2)], \quad (A11)
\]
ACF function $C_{λ,on}(t, τ)$ for ON time

$$C_{λ,on}(t, τ) = \rho_{on}(t - τ/2)ρ_{on,11}(τ) - \rho_{on}(t - τ/2)ρ_{on,11}(t + τ/2),$$

$$= 0.25e^{-2λ_{on}|τ|} - a^2e^{-4λ_{on}τ}, \text{ for } |τ/2| ≤ t < T/n - |τ/2|$$

$$\text{with } |τ| ≤ T/n. \hspace{1cm} (A12)$$

Time average of $C_{λ,on}(t, τ)$ for ON state of the transistor can be given as:

$$C_{λ,on}^t(τ) = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} C_{λ,on}(t, τ)dt,$$

$$= (1/4T)[e^{-2λ_{on}|τ|}(T/n - a^2/λ_{on} - |τ|)$$

$$+ (a^2/λ_{on})(e^{-2λ_{on}τ} - e^{2λ_{on}τ})], \text{ for } |τ| ≤ T/n. \hspace{1cm} (A13)$$

The Fourier transform of time averaged ACF gives the noise PSD. The RTS noise PSD for ON state of switched bias transistor, with a variable duty cycle, can be given as:

$$S^o_{λ,on}(ω) = \mathcal{F}(C^t_{λ,on}(τ)) = \int_{-\frac{T}{2}}^{\frac{T}{2}} C^t_{λ,on}(τ)e^{-jωτ}dτ. \hspace{1cm} (A14)$$

$$S_{λ,on}(ω) = \frac{1}{4T(4λ_{on}^2 + ω^2)} \left[ 4Tλ_{on} \frac{n}{A} - Be^{-2λ_{on}T_n} \right],$$

$$A = a^2e^{-2λ_{on}T_n} + \frac{(16a^2 + 8)λ_{on}^2 + a^24ω^2 - 2ω^2}{(4λ_{on}^2 + ω^2)},$$

$$B = (40a^2 + 6)λ_{on}^2 \cos(ωT/n) - 8ωλ_{on} \sin(ωT/n). \hspace{1cm} (A15)$$

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