Leveraging state sparsity for more efficient quantum simulations

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High-performance techniques to simulate quantum programs on classical hardware rely on exponentially large vectors to represent quantum states. When simulating quantum algorithms, the quantum states that occur are often sparse due to special structure in the algorithm or even in the underlying problem. We thus introduce a new simulation method that exploits this sparsity to reduce memory usage and simulation runtime. Moreover, our prototype implementation includes optimizations such as gate (re)scheduling, which amortizes data structure accesses and reduces memory usage. To benchmark our implementation, we run quantum algorithms for factoring, computing integer and elliptic curve discrete logarithms, and for chemistry. Our simulator successfully runs a factoring instance of a 20-bit number using 102 qubits, and elliptic curve discrete logarithm over a 10-bit curve with 110 qubits. While previous work needed a supercomputer to simulate such instances of factoring, our approach succeeds in less than 4 minutes using a single core and less than 100 MB of memory. To the best of our knowledge, we are the first to fully simulate a quantum algorithm to compute elliptic curve discrete logarithms.

Additional Key Words and Phrases: quantum computing, quantum circuit simulation, sparse simulation

1 INTRODUCTION

Quantum computers promise to solve certain computational tasks exponentially faster than their classical counterparts. Speedups are expected for applications from various domains, including cryptography [36] and computational chemistry [33].

To quantify the advantage of a future quantum computer for practical applications, a host of software packages has emerged over the recent years. These tools allow domain experts to implement quantum algorithms for the purposes of verification and resource estimation [1, 6, 18, 27, 39, 40]. Due to the exponential overhead in resources needed to simulate a quantum algorithm on classical hardware, verification is usually performed on individual subroutines and for small inputs. However, as quantum algorithms are being optimized, existing simulation approaches are no longer powerful enough for simulating even the smallest problem instances.

While some (non-universal) quantum circuits allow for efficient classical simulations (e.g., permutation-only circuits), state-of-the-art implementations of quantum algorithms employ certain optimizations that prohibit the use of such approaches for testing and debugging. For example, while a so-called Toffoli simulator can simulate a straightforward implementation of the modular exponentiation in Shor’s algorithm for factoring, this is no longer the case when the coset-representation optimization from the work by Zalka [43] is used.

Moreover, certain optimizations reduce the required quantum resources but, at the same time, reduce the algorithm’s success probability, e.g., to $O(1/N)$ [16, 35], where $N$ grows with the problem size. For testing and debugging such implementations, simulations at nontrivial sizes are necessary.

Related Work. To address these issues, a variety of simulation approaches have been proposed. Full state vector simulation is advantageous when the state is dense, as is the case for random circuits. Because this approach stores all $2^n$ entries for $n$ qubits, quantum algorithms that require more than 40 qubits are challenging to simulate [23]. For low-depth circuits, approaches based on
Table 1. The largest instances of algorithms for factoring and for computing integer and elliptic curve discrete logarithm that we simulated, compared to previous state of the art. All simulations were carried out on a single core and with less than 100 MB of memory.

| Problem         | Instance   | Qubits | Median Runtime | Previous record                                      |
|-----------------|------------|--------|----------------|------------------------------------------------------|
| Factoring       | $N = 961307$ | 102    | 219 s          | Dang et al. [10]: >7 hours on 216 nodes using 14 TB of RAM with emulation |
| EC DLog         | $p = 665$  | 110    | 69s            | None                                                 |
| Integer DLog    | $p = 32797$| 82     | 74s            | None                                                 |
| Energy estimation with qubitization | $H_2$ with 8s0 | 27     | 968s           | The same simulation as [30] did not finish in 6 days |

Tensor network contraction and a combination of (approximate) Feynman path and Schrödinger simulation have been shown to work best [7, 26, 32, 42].

For quantum circuits dominated by so-called Clifford gates, the method Bravyi and Gosset [8] introduced can be used. Yet, algorithms for chemistry and cryptography mostly consist of non-Clifford gates, making this approach ill-suited for testing such algorithms. Decision-diagram based simulation [20, 44] performs well, e.g., for QFT and Grover search. Nevertheless, simulating full quantum algorithms with more than 40 qubits seems to be out of reach also for this method [20].

Dang et al. [10] used matrix product states and an optimized entanglement mapping in order to simulate Shor’s algorithm for factoring a 20-bit number in approximately 7 hours on a supercomputer. In particular, they employ emulation [24], meaning that they directly implement modular multiplication in the simulator, instead of executing an actual implementation of modular multiplication in terms of quantum gates. However, gate-level simulation is necessary to test and debug optimized implementations (e.g., of modular multiplication).

Contributions. We introduce a new approach for simulating quantum algorithms that leverages sparsity in the quantum state (in a fixed basis). We present several optimizations that increase sparsity and reduce the number of write-operations to the sparse datastructure. We then benchmark our implementation by running quantum algorithms for factoring, computing elliptic curve discrete logarithms, and for quantum chemistry (both Trotter-based and qubitization-based implementations). To this end, we expose our simulator through the Q# runtime, allowing us to rely on existing implementations of quantum algorithms in Q#.

More specifically, our contributions are as follows:

- We introduce a new approach to quantum algorithm simulation that leverages sparsity in the state vector for improved performance and memory usage.
- We implement our simulator in C++ and expose it through the Q# runtime.
- We optimize the performance of our simulator using local quantum circuit rewrites, C++ code optimizations, and multithreading.
- We show that our implementation is capable of simulating larger quantum algorithms than existing methods. In particular, we successfully simulate quantum algorithms for factoring, for elliptic curve discrete logarithms and for quantum chemistry that use up to 105, 110, and 27 qubits, respectively; see Table 1 for a summary of the largest simulations.
- To the best of our knowledge, we are the first to report a successful simulation of the quantum algorithm for computing elliptic curve discrete logarithms, see Table 1. Even the smallest instance, a 3-bit curve, requires 40 qubits.
- We present the first simulation of all of the circuit-level quantum optimizations for integer factoring by Gidney and Ekerä [16].
2 QUANTUM COMPUTING

This section introduces the basic of quantum computing and classical simulation of quantum computers. For a more in-depth treatment, we refer the reader to the textbook by Nielsen and Chuang [34].

2.1 Quantum States, Bits, and Gates

Quantum computers consist of multiple quantum bits (qubits). Similar to its classical counterpart, a qubit can be in a classical state (0 or 1).

**Notation.** We denote the 0-state by \(|0\rangle\) ("ket zero") and the 1-state by \(|1\rangle\) ("ket one"). The \(|\cdots\rangle\)-notation is part of the so-called "bra-ket" notation: In our setting, \(|\psi\rangle\) is a column vector, whereas \langle\psi|\) ("bra") denotes a row vector – the Hermitian conjugate of \(|\psi\rangle\). With this notation, the inner product between \(|\psi\rangle\) and \(|\phi\rangle\) can be written as \langle\psi|\phi\rangle\) and their outer product is \(|\psi\rangle\langle\phi|\).

**Qubits.** The state of a single qubit \(|\psi\rangle\) can be written as

\[ |\psi\rangle = \alpha_0 |0\rangle + \alpha_1 |1\rangle, \]

where \(\alpha_0, \alpha_1 \in \mathbb{C}\) and \(|\alpha_0|^2 + |\alpha_1|^2 = 1\). The latter is the normalization condition, which ensures that \(p_i = |\alpha_i|^2\) can be viewed as a probability. Namely, \(p_i\) is the probability of a measurement resulting in the outcome \(i \in \{0, 1\}\). By identifying \(|0\rangle\) and \(|1\rangle\) with the canonical basis vectors of \(\mathbb{C}^2\), \(|\psi\rangle\) can be written as a column vector in \(\mathbb{C}^2\),

\[ |\psi\rangle = \alpha_0 \begin{pmatrix} 1 \\ 0 \end{pmatrix} + \alpha_1 \begin{pmatrix} 0 \\ 1 \end{pmatrix} = \begin{pmatrix} \alpha_0 \\ \alpha_1 \end{pmatrix}. \]

Analogously, the state of an \(n\)-qubit system is a complex superposition over all \(n\)-bit strings:

\[ \sum_{i=0}^{2^n-1} \alpha_i |i\rangle, \]

where \(|i\rangle := |i_{n-1}\rangle \otimes \cdots \otimes |i_0\rangle\) and \(i_k\) denotes the \(k\)-th bit of the integer \(i\) and \(\otimes\) is the Kronecker product. As before, the corresponding column vector in \(\mathbb{C}^{2^n}\) has entries \(\alpha_i\).

**Quantum Gates.** Quantum computation is performed by applying operations – so-called quantum gates – to qubits. We distinguish gates from measurements. A measurement of all \(n\) qubits results in the outcome \(i = i_{n-1}, \ldots, i_0\) with probability \(p_i = |\alpha_i|^2\). A quantum gate that acts on \(n\) qubits can be represented as a \(2^n \times 2^n\)-dimensional complex matrix, and gate application is modeled as matrix-vector multiplication. In contrast to measurements, which project the state onto the observed outcome (i.e., \(|i\rangle\) will be the post-measurement state when \(i\) was observed), gates must be unitary. That is, the matrix \(U\) describing a gate must satisfy \(U^\dagger U = UU^\dagger = 1\), where \(U^\dagger\) is the Hermitian conjugate of \(U\).

Some common single-qubit gates and their respective matrices are the Hadamard gate \(H = \sqrt{\frac{1}{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}\), the S gate \(S = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}\), the Pauli gates \(X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}\), \(Y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}\), \(Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}\), and Pauli rotation gates \(R_P(\theta) = e^{-0.5i\theta P}\), where \(P \in \{X, Y, Z\}\).

An example of a two-qubit gate is a controlled single-qubit gate, which only applies the single-qubit gate if a control qubit is in \(|1\rangle\). Since \(|i\rangle\langle i|\) is the projector onto \(|i\rangle\), we can write a controlled single-qubit gate \(U\) as

\[ CU = |0\rangle\langle 0| \otimes 1 + |1\rangle\langle 1| \otimes U. \]

We note that this definition may be iterated to construct \(n\)-ary controlled gates, which we denote by \(C^nU\).
There are several common quantum operations which just permute computational basis states, meaning they are equivalent to reversible classical operations. This includes the Pauli X or NOT gate, swap, CNOT, and C^n NOT, which denotes an n-ary controlled NOT.

2.2 Classical Simulation

A natural method to simulate a quantum computer is the Schrödinger full-state simulation, where an array of $2^n$ complex numbers represents the quantum state. The coefficient of state $|i\rangle$ is stored at location $i$ in the array. This method is widely used in the literature [23, 28, 38].

One advantage of this approach is its generality. Any quantum operation, including noisy operations, can be simulated using this method. Unfortunately, the space requirement is exponential in the number of qubits and going significantly beyond 45 qubits is impractical [23].

While actual quantum computers will also face strict qubit limits, we expect more flexible space-time trade-offs. One reason is that longer, more complex algorithms will require more error correction which, in turn, increases the overhead in terms of the number of physical qubits. In addition, the trade-offs may be very one-sided. For example, new algorithms for quantum chemistry can reduce gate complexity by a factor of 1000 with only a factor of 20 more qubits [5], and for factoring integers, 50% more qubits can reduce the gate count by 2000 times [16]. These algorithmic improvements thus significantly reduce the runtime of a quantum algorithm. However, the increase in qubit numbers makes classical testing and debugging a challenging task. Approximate arithmetic adds $k$ qubits and fails with probability $\Omega(2^{-k})$, requiring many qubits to simulate modestly accurate results. The lowest number of qubits for computing elliptic curve discrete logarithms [21] is estimated at $8n + O(\lg n)$. We find the smallest possible $n = 3$ uses 40 qubits. At this size, the point addition circuits will fail for 3/6 points on the curve.

3 SPARSE STATES FOR SIMULATION

Many quantum algorithms with space-time trade-offs will result in states of the form

$$\sum_{i \in \{0,1\}^n} \alpha_i |i, f(i)\rangle$$

for some function $f : \{0,1\}^n \rightarrow \{0,1\}^m$. This state belongs to a vector space of dimension $2^{n+m}$, but it is a sparse vector, at least in the computational basis. This means full-state simulators will waste both memory and time on an exponentially large number of zero-amplitudes.

Our new approach makes use of this sparsity by only storing nonzero entries, thus reducing both memory usage and simulation runtime. Specifically, our simulator stores a quantum state $\sum_{b \in \{0,1\}^n} \alpha_b |b\rangle$ as unordered key-value pairs $(b, \alpha_b)$ for all $\alpha_b \neq 0$, for which we use the efficient hash map by Skarupke [37]. We refer to $b$ as the label and $\alpha_b$ as the amplitude.

Compared to a full-state simulator, we use slightly more memory to represent each amplitude, as we store not only the label, but 1 byte for metadata in the hash map. However, we save memory for every zero-amplitude in the corresponding full state representation.

3.1 Operations

We implement the intrinsic operations in the Q# language. These include Pauli gates, phase rotations, Pauli rotations, measurements, and Pauli exponentials, as well as multiply-controlled versions of all the above (besides measurements). A useful feature of all of these operations is that, when expressed as matrices, at most 2 entries in each row and column are non-zero. We conceptually divide the operations into those with at most 1 non-zero entry, and others.

For the second category, performing an operation requires some computation on pairs of basis states $|b\rangle$ and $|b'\rangle$. We can represent the action of the operator on the space that $|b\rangle$ and $|b'\rangle$ span.
\begin{equation}
\begin{pmatrix}
    a'_1 \\
    a'_2
\end{pmatrix} = \begin{pmatrix}
    a_{11}(b) & a_{12}(b) \\
    a_{21}(b) & a_{22}(b)
\end{pmatrix} \begin{pmatrix}
    a_1 \\
    a_2
\end{pmatrix} \tag{2}
\end{equation}

where \( a_{ij} \) are easily computable functions of \( b \). For all the quantum gates we implement, \( b' \) is easy to compute from \( b \) and vice versa.

To compute an operation, we iterate through all label-amplitude pairs in the hash map. For each one, we compute new label-amplitude pair(s) and insert them into a new hash map. This requires at most one look-up in the original hash map because each label has at most one partner. Since each pair of partner labels differs in at least one bit, if both are present in the table, we only insert when the iteration reaches the label with 1 at this bit location.

While the use of a new hash map doubles the memory requirements, an online algorithm to modify an existing hash map in-place would be challenging. A major issue is that most operations would drastically change the labels, which could force re-sizing or re-hashing. Preserving the ordering of an iteration in an unordered map during a re-hashing is a difficult problem that we did not attempt to solve. However, a benefit of our simple approach is that we can queue operations with exactly one non-zero entry.

3.2 Queueing phases and permutations

Because the arithmetic intensity of each gate is low, a large portion of the computation is spent on look-ups, insertions, and initialization of the new hash map. To minimize these overheads, we queue gates where possible.

As matrices, Pauli gates and phase rotations with any number of controls only have a single non-zero entry per row. We will refer to these as phase/permutation gates. Their structure allows us to define such a gate \( G \) through functions \( f \) and \( g \) such that \( G(a_{b} | b\rangle) = f(b)a_{b} | g(b)\rangle \). Such operations can be chained together. If \( G_1 \) and \( G_2 \) are defined by functions \((f_1, g_1)\) and \((f_2, g_2)\), we can evaluate \( G_2 \circ G_1(a_{b} | b\rangle) = f_1(b)f_2(g_1(b)) | g_2(g_1(b))\rangle \), with a similar pattern for any number of these gates.

To evaluate a queue of \( n \) phase/permutation gates, we iterate through the hash map as before. For each pair \((b, a_{b})\), we compute the action of all \( n \) gates before inserting the result into the new hash map. This amortizes the overheads of hash map look-ups, insertions, and initializations.

3.3 Gate commuting

For two types of quantum gates \( G_1 \) and \( G_2 \), there are often well-known and simple relationships between the serial applications \( G_1 \circ G_2 \) and \( G_2 \circ G_1 \), known as commutation relations. Using these relations, a circuit can be arbitrarily rewritten by altering the order of gates.

We use simple strategy with queues of four types of gates: Phase/ permutation gates, \( H, R_x, \) and \( R_y \). When the Q# runtime sends a gate \( G \) to the simulator, it checks for any \( R_y, R_x, \) then \( H \) gates queued on the requested qubit, and attempts to commute \( G \) through each in turn. If a simple commutation relation exists, it modifies \( G \) as necessary and continues. If, on the other hand, the commutation relation is difficult to compute, it executes all queued gates on those qubits, including any phase/permutation gates. Fig. 1 illustrates this process and, in particular, the interaction between gate commuting and the queue.

Besides the possibility of canceling gates and never needing to execute them, this saves memory by postponing \( H, R_x, \) and \( R_y \) gates, each of which may increase the number of states in superposition.

4 ALGORITHM BENCHMARKS

In order to benchmark our simulator, we choose three variants of Shor’s algorithm and two quantum chemistry algorithms. We run all but one type benchmark 30 times on a single core of an Intel
Fig. 1. Illustration of gate queues and commuting on 8 qubits. Instructions from Q# come in at the top, each column corresponds to a qubit, and the phase/permutation gate queue is at the bottom. Original state is in black. (a) Q# sends an $H$ gate to qubit 0. Since no other gates are queued, it will set the $H$ queue on qubit 0 to 1. (b) Q# sends an $H$ gate to qubit 1. Since $HR_y(\theta) = R_y(-\theta)H$, it will flip the sign of the angle of the $R_y$ gate. Because $H^2 = I$ (the no-op gate), it will reset the $H$ queue on qubit 1 to 0 and not modify the state vector. (c) Since $XH = HZ$, it will add a $Z$ gate (in red) to the phase/permutation queue and not change the $H$ queue. (d) Q# sends a CCNOT gate to qubits 3, 4, and 5, but the simulator cannot commute this gate through the queued $R_x$ gate (nor the $H$ gates), so it first sends all the gates in the phase/permutation queue to modify the state vector. It then applies both $H$ gates on qubits 3 and 4 to the simulator, then the $R_x(0.75)$ rotation. Since all queues are clear, it then adds the original CCNOT to the (now empty) phase/permutation queue. (e) An $R_x(-\pi/4)$ gate might double the superposition size, but the simulator does not apply it during any of the previous steps.

Xeon Platinum 8168 CPU at 2.70 GHz with 32 GiB of RAM. For the quantum-optimized factoring implementation, we used 8 cores on the same machine and ran it 200 times.

Because our simulator’s runtime is almost independent of the number of qubits, we did not always choose implementations with the fewest possible qubits.

4.1 Integer factoring

Background. Shor’s algorithm for integer factoring [36] has attracted a lot of attention because of its impact on cryptography. Much of the previous quantum circuit design literature focuses on the subroutine which performs modular exponentiation in superposition [3, 12–16, 22, 41, 43], since this is the most expensive part.

The method with the fewest qubits uses Fourier-basis quantum arithmetic. However, this requires more quantum gates than other techniques and so other analyses use reversible classical addition. Recent techniques use even more qubits to drastically reduce both circuit size and depth, using quantum modifications of reversible classical techniques [16].

The semi-classical quantum Fourier transform [19] is standard for Shor’s algorithm, and reduces the number of qubits by $2n - 1$ to factor an $n$-bit integer. For our simulator, this is particularly effective, as we only end up with a superposition of all powers of a generator and one control qubit, rather than a superposition of $2^{2n+1}$ control states.

Setup. We use a semi-classical Fourier transform with a reversible classical adder (“CDKM adder”) [9] and a windowed style of in-place modular multiplication [15]. For comparison, we also simulate Fourier-basis quantum arithmetic (“QFT adder”) [11]. We use an implementation of Shor’s algorithm that uses $2n + 1$ bits for the phase estimation.
Fig. 2. Box plots from simulations of integer factoring with Shor’s algorithm. Boxes have a minimum thickness for readability.

Since the size of the superposition depends on the order of a randomly-chosen generator, we pre-selected a generator of maximal order to benchmark worst-case performance.

We also implemented all of the quantum optimizations of [16]: coset representations, windowed exponentation and modular multiplication, and oblivious carry runways. We used one oblivious carry runway per integer, and added the runway into the entire register before multiplication (see discussion). Since this circuit failed so frequently, we ran 200 benchmarks for each modulus, of which only 82 and 112 (respectively) finished successfully.

Results. Table 2, Table 3, and Fig. 2 show our results. Without quantum-specific optimizations, the maximum size of the superposition is exactly double the group order, as expected. The number of qubits is $5n + 2$ for the CDKM adder and $2n + 3$ for the QFT adder. Even in the QFT adder, only 2% of the computational basis states are non-zero at $N = 589$, though the CDKM adder uses less than $10^{-11}$%.

Quantum-specific optimizations such as the coset representation and oblivious carry runways result in larger superpositions, as can be seen in Table 3. Consequently, simulations are challenging even for small instances.

Discussion. The runtime of our simulator scales almost linearly with the group order when the CDKM adder is used, since each gate requires time linear in the size of the superposition, which is double the group order in this case. Fourier-basis arithmetic poses a greater challenge for our simulator because it represents integers with a superposition of computational basis states. The states in this algorithm are thus much more dense.

Our simulator clearly outperforms other simulators when using the CDKM adder. Factoring 961307 took 7.2 hours on a 216 node cluster using matrix product states [10], though this used a full quantum Fourier transform (QFT) and emulation for the modular arithmetic. A full QFT would be more difficult for our simulator, since it would create $\approx 2^{2n+1} \approx N^2$ states in superposition, rather than the $\approx 2N$ that we found; however, a full gate-level simulation would be more challenging for the matrix product state simulator. The decision-diagram simulator by Grurl et al. [20] took approximately 20 s to simulate factoring 187 with 34 qubits. Our implementation uses more qubits...
Table 2. Parameters of the factoring instances. $N = pq$ is the integer being factored, of the given bit-size. The group order is $(p - 1)(q - 1)/\gcd(p - 1, q - 1)$.

| $N$ | Bit-size | Group Order | Qubits | Max. state size | Qubits | Max. state size |
|-----|----------|-------------|--------|-----------------|--------|-----------------|
| 15  | 4        | 4           | 22     | 8               | 11     | 128             |
| 35  | 6        | 12          | 32     | 24              | 15     | 1536            |
| 143 | 8        | 60          | 42     | 120             | 19     | 30720           |
| 589 | 10       | 90          | 52     | 180             | 23     | 184320          |
| 3599| 12       | 1740        | 62     | 3480            | -      | -               |
| 14351| 14      | 1008        | 72     | 2016            | -      | -               |
| 36089| 16      | 17850       | 82     | 35700           | -      | -               |
| 216067| 18     | 35856       | 92     | 71712           | -      | -               |
| 961307| 20     | 479568      | 102    | 959136          | -      | -               |

Table 3. Parameters of factoring instances with all quantum optimizations from Gidney and Ekerå [16].

| $N$ | Bit-size | Group Order | Coset/Runway | Window Sizes | Success Rate | Exp. Mult. | Exp. | Actual | Qubits | Max. state size |
|-----|----------|-------------|--------------|--------------|--------------|------------|------|--------|--------|-----------------|
| 15  | 4        | 4           | 4            | 3            | 4            | 0.30       | 0.41 | 40     | 557056 |
| 21  | 5        | 6           | 5            | 3            | 5            | 0.46       | 0.56 | 49     | 25952256 |

for a roughly equivalent problem (factoring 143), but still simulates this with a median runtime of 0.47 s. Even with Fourier-basis arithmetic, our simulator’s median runtime was 5.1 s.

The quantum-optimized circuit poses a much greater challenge for our simulator in terms of both runtime and success probability. This is not surprising, given that it relies on large superpositions and, while the error rate scales exponentially with the number of padding bits, so does the superposition size and hence the memory requirements and runtime of our simulator.

Each addition adds an error of approximately $2/2^{c_{pad}}$ [14], where $c_{pad}$ is the number of padding bits, and the factor of 2 accounts for both coset representation and oblivious carry runway errors. This means even a smaller factoring sample, which may require only a few dozen additions, quickly becomes lost to noise. To benchmark any examples successfully, we thus increase the window sizes for exponentiation and multiplication, which reduces the number of additions to 12 and 16 for factoring 15 and 21, respectively.

We decode and measure all integers in between multiplications and abort if the measurements are non-zero. This saves the simulator from storing unnecessary superpositions. Each window of each multiplication involves 2 additions; however, the first of these is into an all-zero register, so it cannot cause an error in the carry runways or the coset. Thus we expect 9 and 12 additions that could actually cause errors for the two benchmarks. The error rate of each addition should be $1/2^3$ and $1/2^4$, respectively, leading to expected success rates of $(1 - 2^{-3})^9$ and $(1 - 2^{-4})^{12}$. These are both lower than what we found.

**Oblivious Carry Runways.** Modular multiplication uses the individual bits of an integer (possibly several at once) to control addition of multiples of a constant. This works because if an integer $x$ is represent by bits $(x_0, x_1, \ldots, x_n)$ such that

$$x = x_0 + 2x_1 + 2^2x_2 + \cdots + 2^n x_n$$

(3)
then we can compute \( bx \mod N \) as
\[
(x_0(b \mod N) + x_1(2b \mod N) + x_2(2^2b \mod N) + \cdots + x_n(2^nb \mod N)) \mod N.
\]
(4)

This relies on the modulo operation acting as a homomorphism between addition over the integers to addition modulo \( N \). With a carry runway, the integer \( x \) is represented by \( k \)-bit words \((x_0, x_1, \ldots, x_n)\) and runways \((r_0, \ldots, r_{n-1})\) such that
\[
x = x_0 + 2^k r_0 + (x_1 - r_0)2^k + \cdots + (x_n - r_{n-1})2^{kn}.
\]
(5)

This could be used directly to control multiplication modulo \( N \), though it will require more additions than necessary because of the extra runway bits. However, it’s not clear how \( x_i - r_i \) is represented, since this number may be negative. The approach by Gidney [14] is to perform this subtraction modulo \( 2^k \). This means we cannot perform a bit-by-bit controlled addition of multiples of a constant \( b \), because if \((x_i - r_i) \mod 2^k \) is represented as a bitstring \( y_0 + 2y_1 + \cdots + 2^{k-1}y_{k-1} \), then it may occur that
\[
\left(b(x_i - r_i) \mod 2^k\right) \mod N \neq \left(y_0(2^0b \mod N) + \cdots + y_{k-1}(2^{k-1}b \mod N)\right) \mod N
\]
(6)
because addition modulo \( 2^k \) is not homomorphic to addition modulo \( N \).

When \( x_i \geq r_i \), there is no issue since \( x_i - r_i \mod 2^k = x_i - r_i \) as integers. Gidney and Ekerà [16] proposed a runway size of only around 30 qubits, and the register contains more than 1000 qubits, so the number of states with \( x_i < r_i \) is negligibly small and the technique works without issue.

However, when we implemented these circuits, we had to use runways that were the same size as the register including coset padding, meaning \( x_i < r_i \) for approximately half the states in superposition. To reduce the probability of failure, we had to fully propagate and decode the runways into the registers before using them as inputs into multiplications. This adds only a small overhead in depth compared to the optimized decoding by Gidney and Ekerà [16].

### 4.2 Integer Discrete Logarithms

**Background.** Shor’s algorithm also applies to finding discrete logarithms in abelian groups. We tested this for the multiplicative of integers modulo a prime number. The IETF standard [17], the Microsoft Schannel Provider, and ElectionGuard [4] rely on the difficulty of discrete logarithms in this setting.

For Shor’s algorithm, the main difference compared to factoring is that we multiply by powers of two different elements of the group, and the result consists of two numbers \((j, k)\) such that \( j + dk \approx 0 \mod 2^m \), where \( m \) is the number of bits we used in the phase estimation, and \( d \) is the discrete logarithm.

**Setup.** We use the same arithmetic circuits as our integer factoring benchmarks, with a semi-classical quantum Fourier transform for the phase estimation, and a generator of maximal order. In all benchmarks we used a discrete logarithm of 7.

**Results.** Table 4 and Fig. 3 show the runtimes of our simulator. We see a similar qubit count of \( 5n + 2 \) for \( n \)-bit primes.

**Discussion.** The performance is very similar to integer factoring, since both are simply controlled modular multiplication, from the perspective of the simulator.

It may seem surprising that the state size is 4 times the group order, whereas it was \( 2x \) for factoring. The reason is that the semi-classical QFT is performed from the most-significant bit to the least significant, and the group order of RSA-style moduli is always even. Thus, until the final modular multiplication, the superposition only contains powers of the *square* of the generator, not
Table 4. Parameters of integer discrete logarithm simulations. $p$ is the prime modulus of the given bit-size, and the group order is $p - 1$.

| $p$ | Bit-size | Group Order | Qubits | Max. state size |
|-----|----------|-------------|--------|-----------------|
| 11  | 4        | 10          | 22     | 40              |
| 19  | 5        | 18          | 27     | 72              |
| 59  | 6        | 58          | 32     | 232             |
| 113 | 7        | 112         | 37     | 448             |
| 151 | 8        | 150         | 42     | 600             |
| 433 | 9        | 432         | 47     | 1728            |
| 821 | 10       | 820         | 52     | 3280            |
| 1321| 11       | 1320        | 57     | 5280            |
| 2659| 12       | 2658        | 62     | 10632           |
| 4759| 13       | 4758        | 67     | 19032           |
| 9743| 14       | 9742        | 72     | 38968           |
| 17033| 15      | 17032       | 77     | 68128           |
| 32797| 16      | 32796       | 82     | 131184          |

Fig. 3. Box plots of simulations of integer discrete logarithm with Shor’s algorithm. Boxes have a minimum thickness for readability.

the generator itself. In contrast, integer discrete logarithm performs a full semi-classical QFT on the generator before moving to the target integer. After the full semi-classical QFT, the full group is present in superposition.

The particular implementation of modular addition we used performs a measurement-based un-computation of a comparison, which temporarily doubles the state size. Thus, since integer discrete logarithms continue to perform modular multiplication after creating a full group superposition, but factoring does not, the maximum superposition size in factoring is only twice the group order.

4.3 Elliptic curve discrete logarithm

Background. Another major application of Shor’s algorithm to cryptography is solving the discrete logarithm problem for elliptic curve groups. The structure of Shor’s algorithm is the same as integer
Table 5. Parameters of the elliptic curves we tested. “Failures” is the number of instances where the measurement of the auxiliary register yielded non-zero and we stopped the test. The maximum state size is the maximum over all runs.

| Prime | Group | Order | Exp. Failures | Semi-classical QFT | Windowed QFT |
|-------|-------|-------|---------------|--------------------|--------------|
|       | Size  |       | Qubits | State size | Failures | Qubits | State size | Failures | Window size |
| 31    | 5     | 41    | 9.0    | 59        | 742      | 8      | 63        | 502      | 4          | 3          |
| 61    | 6     | 73    | 5.6    | 68        | 1960     | 3      | 72        | 786      | 2          | 3          |
| 97    | 7     | 89    | 4.6    | 77        | 4334     | 2      | 81        | 3442     | 3          | 3          |
| 251   | 8     | 271   | 1.8    | 87        | 4476     | 0      | 92        | 5328     | 1          | 4          |
| 509   | 9     | 503   | 1.0    | 96        | 9036     | 0      | 101       | 14118    | 0          | 4          |
| 661   | 10    | 665   | 0.8    | 105       | 48682    | 0      | 110       | 48977    | 0          | 4          |

discrete logarithms, but the arithmetic of the underlying group is much more involved. In particular, the arithmetic requires many more auxiliary registers, meaning that a full-state simulation would be limited to curves of only 2-3 qubits.

**Setup.** We used a mix of “low-width” and “low-T” elliptic curve operations from the Q# implementation by Häner et al. [21], with a set of prime-order curves defined over primes of 5 to 10 bits. We also used the signed windowed quantum Fourier transform, with a window size equal to $\lfloor \log_2 n \rfloor$ for $n$-bit primes.

The quantum circuit for elliptic curve point addition adds a classical point $P$ to a quantum point $Q$, but fails if $P = Q$, $P = -Q$, or $P + Q = -P$. The behaviour in these cases results in states representing “points” which are not on the elliptic curve. Once a point is not on the curve, the behaviour of the addition formulas is not defined, and they may produce more pairs of points that are not on the curve.

For an elliptic curve over a prime $p$, the order is $p \pm O(\sqrt{p})$ [25], but there are $p^2$ possible pairs of points $(x, y)$ modulo $p$. Thus, fully simulating this imperfect point addition creates far more states in superposition than a perfect point addition. We measured an auxiliary register in the addition circuit which is returned to 0 for well-defined point addition. This either removes some of the undesired states, or causes a complete failure of the addition. In the second case we abort the benchmark and do not include it in the results.

**Results.** Table 5 and Fig. 4 show the results. We find the number of required qubits for an $n$-bit prime are $9n + \lfloor \log n \rfloor + 12$.

**Discussion.** The minimum possible qubit count is $8n + \lfloor \log n \rfloor + 15$, so a full state simulator could run a 3-bit curve (no prime-order 2-bit curve exists) with 40 qubits. To the best of our knowledge, this has not been done.

Our simulator runs larger sizes, allowing us to test the scaling of the error rate with the order of the curve. The probability of each type of failure is upper-bounded by $(2 + \lfloor \log(r-1) \rfloor) \frac{1}{2^{(r-1)}}$ for an $m$-bit QFT and a curve of order $r$ [35]. The types of failures are mutually exclusive. The expected value of failures over 30 trials is given in Table 5. Our results suggest it is a slight overestimate, even at these sizes.

The maximum state size is much more than double the group order. Inspecting the wavefunction during execution shows that much of this superposition consists of points not on the curve with low amplitude, i.e., accumulated point addition errors. Some point addition errors will still result in a 0 state in the auxiliary qubits we measured, and thus contribute to the wavefunction. The superposition size is also much lower than the square of the prime modulus, meaning it was not a superposition over all possible pairs of points.
Our simulation of windowed point addition represents a logical qubit simulation of the state-of-the-art implementation of Shor’s algorithm over elliptic curves. Windowing the point addition is beneficial from a quantum resource perspective, but it actually benefits our simulator as well. We might expect that a \( k \)-bit window will increase the superposition size by a factor of \( 2^{k-1} \). Instead, we see little difference. Windowing means fewer point additions, though each one adds more points, and thus should have the same failure rate. The state size at all points is still higher than \( 2^k \) times the group order.

4.4 Quantum Chemistry

**Background.** The application we consider is finding the ground state energy of a molecular Hamiltonian. Several quantum algorithms are known that address this problem. Here, we focus on two algorithms, both of which apply quantum phase estimation to a subroutine that implements a function of the Hamiltonian \( H \).

One such function is the time evolution operator \( U_t = e^{-iHt} \), where \( t \) denotes the duration of time evolution. Given an implementation of \( U_t \) and a trial state \( |\tilde{\psi}_0\rangle \) with a nontrivial overlap with the true ground state \( |\psi_0\rangle \), quantum phase estimation outputs an estimate of the ground state energy \( E_0 \) with probability \( p = |\langle \tilde{\psi}_0 |\psi_0 \rangle|^2 \).

**Setup.** The two algorithms that we use as benchmarks are qubitization [31] and a Trotter-Suzuki based implementation [29]. We refer to the papers by Low and Chuang [31] and Lanyon et al. [29], respectively, for more details. Both algorithms are available in the QDK [40], allowing us to run them using Q#. We ran them with our sparse simulator and with the full-state simulator from the QDK. As examples, we use an \( H_2 \) molecule using 2 or 4 spatial orbitals, corresponding to 4 and 8 spin-orbitals, respectively.

**Discussion.** Our simulator improves upon the full-state simulation, especially for larger number of orbitals and qubitization, which uses more qubits than a Trotter-Suzuki based implementation. This improvement in runtime is possible because the large qubitization benchmark occupied at most 0.02% of the state vector.
Table 6. Results and parameters of chemistry benchmarks for H₂. Tests are parameterized by the number of spin-orbitals (SO), the number of bits in the quantum phase estimation (QPE), and the Trotter step size.

| Algorithm      | SO | QPE Bits | Step size | Qubits | State size | Min. | Median | Max. | Min. | Median | Max. |
|----------------|----|----------|-----------|--------|------------|------|--------|------|------|--------|------|
| Trotter-Suzuki | 4  | 7        | 0.4       | 5      | 4          | 0.20 | 0.20   | 0.46 | 0.22 | 0.23   | 0.44 |
|                | 8  | 8        | 0.1       | 9      | 30         | 9.7  | 9.8    | 9.9  | 9.8  | 9.8    | 10.0 |
| Qubitization   | 4  | 7        | n/a       | 13     | 64         | 3.6  | 3.6    | 3.8  | 11.5 | 11.5   | 11.7 |
|                | 8  | 8        | n/a       | 27     | 24998      | 929  | 958    | 1020 | >6 days | >6 days | >6 days |

For the smallest Trotter-Suzuki simulation, only about 1 ms was spent in the simulator; the rest of the time was Q# overhead. The overhead decreased to 11% on average for the 8 spin-orbital qubitization benchmarks.

5 PARALLELISM

It is nontrivial to add efficient multi-threading support to our simulator. The reasons are that (1) most operations need very little computation for each state in superposition and (2) while the hash map is thread-safe for reading, it is not for writing. As a result, it is to be expected that a multi-threaded implementation provides a minor benefit over the serial implementation.

The first issue can be addressed when there is a long queue of phase/permutation gates. The time to apply all queued permutations is then large relative to a write access to the hash map. We find that processing the queue in parallel on each state is beneficial for long queues and large superpositions. Specifically, we only parallelize if the queue is longer than 64 gates and if there are more than 4096 states in the superposition.

Unfortunately, (1) remains an obstacle for other gates. Consequently, only a fraction of the total runtime is subject to parallelism. For example, we find that the simulator spends approximately 60% of the total serial runtime on large permutations when simulating Shor’s algorithm for factoring and elliptic curve discrete logarithms. From Amdahl’s law [2], we thus expect a speedup of at most 2.5×.

We tested our multi-threaded implementation on the largest parameter sizes for factoring and elliptic curve discrete logarithms, with a number of cores increasing from 1 to 8. We ran these benchmarks on the same machine as in Section 4. We plot the runtime in Fig. 5 and compare to the theoretical performance from Amdahl’s law [2].

While multi-threading noticeably reduces simulation runtime, our implementation fails to reach the theoretical maximum speedup. We expect that contention to write to the new hash map is causing the issue. Despite spending slightly less time on parallelizable computations, the elliptic curve arithmetic benchmark benefits more from parallelism. This may be another consequence of contention: The factoring circuits used measurement-based uncomputation for comparisons and table look-ups, and measurements force execution of gate queues. In contrast, the elliptic curve arithmetic has no such quantum optimizations built in. Therefore, it can build larger queues of gates, leading to more time spent on processing the gates, rather than competing for write-access to the new hash map.

6 CONCLUSION AND OUTLOOK

We introduce a new approach for testing and debugging quantum algorithms. In contrast to the state of the art, our simulator enables complete test runs of optimized implementations of arithmetic with table look-ups and measurement-based uncomputation, and quantum chemistry with qubitization.
Fig. 5. Parallel speed-up of Shor’s algorithm for elliptic curve discrete logarithm of a 10-bit curve and factoring 961207, relative to the median runtime with a single core. Theoretical speed-up (solid lines) from Amdahl’s law is based on the average proportion of time spent on parallelizable gates (0.602 and 0.577, respectively).

We envision that this simulator can help reduce resource requirements further, as it enables testing of optimizations that could not be tested thus far, and testing many smaller examples even faster. This will also improve the confidence in these optimizations by better testing their accuracy.

Future work on this kind of simulation could incorporate other simulation optimizations, such as separate data structures while states are separable. A hash map which is thread-safe for writing could also improve parallelism, which may be necessary for extremely large simulations that would require a distributed computation.

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