Real-time Processing System for Cavity Ring Down Signal Based on ZYNQ Chip

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Abstract The traditional cavity ring-down signal processing system usually consists of a computer and a high-speed data acquisition card, and it has some problems such as large volume, high cost and inconvenience to carry in practical engineering applications. Aiming at the deficiency of traditional signal processing system, a compact real-time data acquisition and processing scheme is proposed and realized based on the Xilinx ZYNQ chip. In which, the FPGA and ARM core integrated into the ZYNQ chip are used to replace the data acquisition card and PC, and the whole system are built and implemented on the circuit board. The experimental results show that, compared with the traditional signal acquisition and processing system, the relative deviation of V-shaped cavity decay time between the two systems is 0.38%, and the repeated measurement standard deviation of the new system is much smaller, which is about 1/3 of the traditional system. Furthermore, the ENOB (Effective Number of Bits) and SFDR (Spurious-Free Dynamic Range) of the new system are measured as > 10.4 bit and > 72dB respectively.

Key words: real-time; ZYNQ chip; cavity ring-down; processing system;
Classification: Integrated circuits

1. Introduction

With the rapid development of cavity ring-down (CRD) technology in recent years, its application has ranged from solving the problem of ultra-high reflectivity measurement to the most widely used cavity ring-down spectroscopy technology. It covers the fields of spectroscopy, atomic and molecular chemistry, applied chemistry, and biochemistry[1, 2, 3, 4, 5, 6]. The decay time constant of the ring-down process is a core physical information of the cavity ring-down technology[7, 8, 9, 10, 11], and its measurement accuracy directly affects the reliability of the entire system. The ring-down time of the CRD signal is extremely short, usually in the order of μs or even ns. Therefore, the requirements of higher accuracy and better real-time performance are put forward to improve the measurement system. It is very meaningful when applied to the cavity ring-down spectroscopy to detect trace gases, and can more accurately reflect the change of the measured gas concentration in the ring-down cavity[12, 13, 14, 15, 16]. In the measurement of the resonant cavity loss, the resonant cavity can be adjusted in real-time, which can reduce the loss of the resonant cavity and improve the yield and excellent rate of the resonant cavity efficiently[17, 18, 19]. The traditional measurement system consists of a DAC (Data Acquisition Card) and a computer which obviously has the disadvantages of large size, complex operation, and poor scalability. To solve the problems mentioned above, the microprocessor ARM (Advanced RISC Machine) or DSP (Digital Signal Processor) is used as a upper computer to realize data fitting, and the FPGA is used as a lower computer for A/D (Analog to Digital) conversion and data acquisition[20, 21, 22, 23, 24]. However, the ARM/DSP system has two problems limiting higher sampling rate and faster transmission speed in process of CRD signal. The first question is that it has no high-speed interface in the system. The second is that the complex peripheral hardware circuits are required for the simultaneous existence of multiple control chips.

To improve the quality of CRD signal processing and the practicability of the system, a novel system based on Xilinx ZYNQ series chip (XC7Z100-2EFG900I) is proposed, in which the ZYNQ series chip integrates the PS (Process System, two Cortex-9 ARM cores) and the PL (Program Logic, FPGA)[25]. This on-chip system can perfectly replace the upper computer and the lower computer in the traditional system[26, 27, 28]. Moreover, benefited from integration of the data acquisition and processing parts, the volume of the whole system is greatly reduced. In addition, the speed of AXI transmission bus used between FPGA part of the ZYNQ chip and ARM core part is up to 100Gbps. Besides ordinary I/O ports, GTX high-speed serial bus interfaces are also equipped as the external interface. As applicable SRIO protocol and JESD204 protocol[29, 30], the ZYNQ-based system’s signal transmission speed can reach ten Gbps. It create a good hardware condition for the high-speed acquisition and processing of CRD signals.

2. General design of system

A block diagram of the CRD signal acquisition and
processing system based on ZYNQ chip is presented in Fig.1. The system consists of power supply module, system clock support module, analog data acquisition module, internal interconnection transmission module and data fitting module.

![Fig. 1 Real-time processing system of cavity ring down signal based on ZYNQ chip](image)

After the system is powered on, the power module supplies power to the whole system to ensure its normal operation. The ZYNQ chip works as the control core by the configuration circuit, and the stored program is downloaded to ZYNQ from the QSPI FLASH chip. The CRD signal is converted from optical signal to analog voltage signal by photo-detector. Then the voltage signal is modified by processing module to meet the acquisition requirements of the high-speed ADC. Next, the ADC converts the analog signal into digital signal which is received by the PL part of ZYNQ chip. When PL receives the trigger signal, the digital data will be transmitted to the PS part of ZYNQ chip through AXI4 bus. Finally, the ARM core is used to realize exponential fitting of CRD signal and store or display the results.

2.1 Analog signal acquisition module
The analog signal acquisition module includes front-end photo-detector, signal pro-process and analog-to-digital conversion. The A/D converter is TI(Texas Instruments)’s 16bit / 500MHz high-speed serial analog-to-digital converter ADC31JB68 with advantages of low power consumption, wide bandwidth and large SFDR. Considering the range of differential input(-0.85V~0.85V) and the common mode voltage(1.6V), AD8138 chip is selected as the core to process the collected analog signal, which includes pull low level and differential output. The Pin ‘Vin’ is directly connected to ADC’s common mode output voltage. It is shown as Fig.2.

![Fig. 2 The process of analog signal acquisition and transmission](image)

The output of ADC31JB68 is dual channel differential output, which adopts JESD204 protocol. It adapts to the GTX high speed serial bus interface of ZYNQ chip. Then, the IP core of JESD204B is called by software of Xilinx(VIVADO), and the high-speed serial data is received and converted into four 16 bit real digital signals by synchronous clock. An AXI bus with 32 bit bit-width is selected for data transmission. The analog signal is converted into digital signal by ADC and decoded by JESD204 protocol. One rising edge of PL part receives four 16bit data, so the total number of bits is 64. However, the bit-width of selected AXI bus is 32 bits, so FIFO IP core can be called to realize data cache and bit width conversion.

2.2 Internal interconnection transmission module
In ZYNQ chip, there are three PS-PL interfaces(AXI_GP, AXI_HP, AXI_ACP) provide data path with low latency, high throughput and data consistency[31]. When a large number of data needs to be transmitted, DMA (Direct Memory Access) can be used to move data through the DDR; When the data is small, the requirement of speed is not high, and the data interaction of PS-PL can be completed through GPIO (General Purpose Input/Output) interface. To improve the transmission speed, BRAM(Block Random Access Memory) mode with high throughput is selected in this design. Data interaction between PL and PS is realized through BM(Block Memory).

![Fig. 3 The block design of Internal interconnection transmission module](image)

As shown in Fig.3, write data and address to BM through BRAM_PORTB. When the number of stored data reaches the requirement, the ‘gpio_0’ receives signal ‘1’ and triggers peripheral interrupt. By setting the read function in SDK, the data in BM is read to perform exponential fitting processing when the interrupt occurs. Finally, through “XGpio_Discretewrite” function writes the result to ‘gpio-1’ which is read in the PL section.

2.3 Data fitting module
As shown in the figure above, when GPIO receives the signal ‘1’, GPIO interruption is triggered. At this point, the program in the SDK jumps into the interrupt program.
and starts to read the data in BM. Then the exponential fitting processing of the transmitted data is started, and successive integration method is used as fitting algorithm. In 2004, Halmer et al. [32] used some typical properties of exponential function and integral to convert the problem of exponential fitting into linear regression by integral method, which greatly reduced the calculation amount, and this method was faster than the general linear regression algorithm. The principle of this method is that the integral of an exponential function can appear itself again, and then find the original function by re-integration. For the general formula (1) of decay signal, its integral can be obtained

\[ I(t) = I_0 \exp(-\tau / t) + A_0 \]  

(1)

\[ \int_0^t I(\xi) d\xi = \tau (I_0 + A_0) - \tau I(t) + A_0 t \]  

(2)

\[ \Leftrightarrow I(t) = I_0 + A_0 - \frac{1}{\tau} \int_0^t I(\xi) d\xi + \frac{1}{\tau} A_0 t \]

This leads to a linear two-dimensional equation,

\[ I(X, t) = A + BX + Ct \]

Then the least square method is used to calculate the best coefficient A, B and C. So we can use the equation with coefficient and decay time constant to calculate \( \tau \). A brief comparison of several commonly used exponential fitting algorithms is shown in Table I.

| Table I. Brief comparison of exponential fitting algorithms |
|----------------------------------|---------|
| Linear Least Square Method (LS)  | faster  |
| Discrete Fourier Transform (DFT) | slow    |
| Fast Fourier Transform (FFT)     | lower   |
| Method of Successive Integration (MSI) | fastest |
| Linear Regression Summation Method (LRS) | fastest |
| Levenberg Marquardt Algorithm (L-M) | slow    |

2.4 System Clock Support Module

The mainly clock is used in this system, includes analog signal acquisition module and ZYNQ chip’s working clock. To meet the needs of ADC, 500 MHz sampling clock and 500KHz SYSREF_CLK synchronization clock are needed. We choose the clock chip LMX2582 and LMK2482, the former generates a 500 MHz sampling clock, the latter generates a synchronous clock and a 125 MHz receiving clock for JESD204B core in the PL. All of them support JEDEC (Joint Electron Device Engineering Council) JESD204 protocol. The ZYNQ chip’s working clock is generated by its PLL (Phase Locked Loop) IP (Intellectual Property) core after the peripheral clock is input. There are two types of crystal oscillators in this system. One is Constant temperature crystal oscillator FCOX8-113 with low frequency error, small temperature frequency difference and stable output, the output clock frequency is 100MHz, and the other one is crystal oscillator SG3225VEN and SG5032CAN which provides the ZYNQ chip’s working clock. The whole clock module is shown in Fig.4

2.5 Power supply module

The power supply module is designed as DC/DC (Direct Current to Direct Current) combination with LDO (Low Dropout Regulator) in this system. The DC/DC primarily converts higher voltages into lower voltages and directly supply power to digital circuit part which less affected by noise. The LDO mainly provides a power supply with low noise for the analog signal transmission circuit because of noise will affect signal quality. A stable voltage supply is used to provide 12V, and the power chips are to convert the 12 V to the required supply voltages. The main chip’s power supply is shown as Fig.5.

The PS part and PL part are powered in the chip as
independent sequence parts. However, there is a requirement for power sequence between each power supply inside the PS and PL. The official recommended PS power-on sequence is \( V_{CCINT} \rightarrow V_{CCPAUX} \) and \( V_{CCPLL} \rightarrow PSV_{CCO} \) \((V_{CCO_MIO0}, V_{CCO_MIO1}, V_{CCO_DDR})\). The official recommended PL power-on sequence is \( V_{CCINT} \rightarrow V_{CCBRAM} \rightarrow V_{CCAUUX} \rightarrow V_{CCO} \). The power supply description of each module of the ZYNQ chip is shown in the Table II.

| Type          | Pin Name    | Normal Voltage | Description                  |
|---------------|-------------|----------------|------------------------------|
| **PS Power**  | \( V_{CCINT} \) | 1.0V           | Internal logic               |
|               | \( V_{CCPAUX} \) | 1.8V           | I/O buffer pre-driver        |
|               | \( V_{CCPLL} \) | 1.8V           | Three PLL clocks, analog     |
|               | \( V_{CC_MIO} \) | 1.8V to 3.3V   | MIO bank 0, pins 0:15        |
|               | \( V_{CC_MIO} \) | 1.8V to 3.3V   | MIO bank 1, pins 16:53       |
|               | \( V_{CC_DDR} \) | 1.2V to 1.8V   | DDR memory interface         |
| **PL-power**  | \( V_{CCO} \) | 1.6V           | Internal core logic          |
|               | \( V_{CCBRAM} \) | 1.6V           | PL block RAM                 |
|               | \( V_{CCAUUX} \) | 1.8V           | I/O buffer pre-drive         |
|               | \( V_{CCO} \) | 1.2V to 3.3V   | I/O buffers drivers (per bank)|
|               | \( V_{CC_BATT} \) | 1.5V           | PL decryption key memory back up |
|               | \( V_{CCAUUX_32G} \) | 1.8V to 2.0V  | PL auxiliary I/O circuits    |

Photograph of the designed real-time processing system board is presented in Fig.6.

![Fig. 6 Photograph of the designed real-time processing system board](image)

3. Experimental results

After completing the software and hardware of the system, we carried out the test work. At 12V voltage input, the working current of the entire circuit is observed to decrease from 0.94A at the beginning to 0.72A at steady operation. The analysis shows that this is caused by the temperature rise of crystal oscillator FCOX8-113 to the operating temperature of 80°C. So the power consumption of the system can be calculated as 8.64W. In contrast, a conventional system will consume 300W. On the other hand, in terms of volume, ZYNQ-based system is integrated on 132×100mm board integrated circuit which is far less than traditional system.

3.1 Acquisition performance test result

The performance of ADC acquisition part is tested first, and the ENOB and SFDR are shown in Fig.7. It can be found that, when the signal frequency is less than 300MHz, the ENOB of ADC>10.6bit, SFDR > 76dB; in the frequency range of 300MHz~500MHz, the ENOB of ADC>10.4bit, SFDR>72dB. They are both close to the values in the data sheet and better than DAC. This shows the ZYNQ-based system has higher SNR(Signal-to-Noise Ratio) and better dynamic performance.

![Fig. 7 Acquisition performance test result](image)

3.2 The analysis of practical test result.

A V-shaped CRD spectrometer was used to verify the performance of the new open system. For a detailed description of the CRD spectrometer, please refer to reference [33]. Losses of V-shaped spectrometer are measured using different systems at specific wavelengths, and the measurement results of decay time using our system are compared with those of the traditional system which uses 100M/14bit DAC and PC [33]. The signal quality of the two systems is shown in the Fig.8.

![Fig. 8 Cavity ring down signal acquired by data acquisition card](image)
From the test result, the residual of ZYNQ-based system is about half of DAC. Therefore, the following conclusions can be drawn: the signal error of CRD signal acquired by ZYNQ-based system is smaller than traditional system. The decay time constant as core parameter of CRD signal. Then, the multiple measurements of decay time constant by two system are carried out, their results are all shown in the Table III

| Number of times | Average (µs) | Variance (µs) |
|-----------------|-------------|---------------|
| ZYNQ(µs)        |             |               |
| 1               | 3.462       |               |
| 2               | 3.534       | 3.52          |
| 3               | 3.532       | 3.52          |
| 4               | 3.538       | 3.52          |
| 5               | 3.453       | 3.52          |
| 6               | 3.453       | 3.52          |
| 7               | 3.453       | 3.52          |
| 8               | 3.453       | 3.52          |
| 9               | 3.453       | 3.52          |
| 10              | 3.453       | 3.52          |
| DAC+PC(µs)      |             |               |
| 1               | 3.394       |               |
| 2               | 3.394       |               |
| 3               | 3.394       |               |
| 4               | 3.394       |               |
| 5               | 3.394       |               |
| 6               | 3.394       |               |
| 7               | 3.394       |               |
| 8               | 3.394       |               |
| 9               | 3.394       |               |
| 10              | 3.394       |               |

It can be found that the standard deviation of the measurement result of the ZYNQ-based system is less than DAC+PC, this means the measurement of ZYNQ-based system is more reliable and its repeatable measurement is more accurate.

4. Conclusion

Nowadays, the rapid development of engineering technology puts forward higher requirements for detection and acquisition of various signals. As one of the research hotspots in engineering application, the measurement of decay time constant has played an important role in many field, including CRD, Attenuation of Scintillator and Attenuation of Neutron etc. Therefore, the system with faster measurement speed, higher accuracy and succinct measurement method is proposed for the acquisition of decay time constant. Compared with the traditional CRD signal acquisition and processing system, the real-time processing system of CRD signal based on ZYNQ chip in this paper is suitable for measurements of decay time constant, which is in possession of many advantages including smaller volume, lower power consumption, higher accuracy and simpler operation.

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