Study on the Boost Converter with Parasitic Parameters of SiC MOSFET

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Abstract. As a new type of transistors, SiC MOSFETs have excellent performance on switching speed and are capable to improve the energy efficiency and energy density of power conversion devices. On the other hand, the parasitic parameters associated with them bring potential problems when designing switching regulators or analysing the converter performances. In this paper, a boost converter model based on the switching characteristics of SiC MOSFETs is presented for describing the power conversion behaviours comprehensively and accurately. Applying that model, a feedback control system is designed and simulated to explore the influence of each parasitic capacitance on the boost converter. Also, the power loss of the converter during steady operation is analysed and simulated. The research method and simulation results in this paper can be referenced for the design of boost converter with parasitic parameters of SiC MOSFET.

1. Introduction
As a switched-mode power supply (SMPS), the boost converter relies on the variation of the on-to-off ratio (duty-cycle) of pass transistors to achieve voltage regulation [1]. Therefore, the switching characteristics of these power transistors are critical in real power conversion applications. On the one hand, switching performance will be reflected in the dynamic behavior of the main circuit within one operation period, and thus influence the power transmission. On the other, the low-dissipation states of the transistors will cause additional power loss and result in distinct cost calculations.

Nowadays, the appearance of SiC MOSFETs makes relevant researches to be attached even higher importance. In high-frequency, high-voltage, and high-power applications, SiC MOSFETs’ characteristics of high speed can improve the power density and efficiency of power conversion devices, thus achieving good economic benefits [2]. But at the same time, the parasitic parameters of SiC MOSFETs influence more on power conversion devices during switch transient [3]-[5]. So far, a lot of researches have been done to address the issue regarding power dissipation, in which describing MOSFETs’ switching energy loss [6]-[8] is discussed as an independent research topic. However, when designing and analyzing the voltage regulation of SMPS, the ideal switching assumption remains in most documents [9]-[12].

In this paper, by introducing the effect of parasitic parameters, an analytical circuit model for boost converter based on switching characteristics of SiC MOSFET is constructed in Section 2. In Section 3, the input-output function is derived and applied to the process of PID feedback control simulation. As a critical engineering calculation, the power loss of the converter is analyzed and simulated in Section 4 by applying the model obtained.
2. Modelling of the Boost Converter

The boost converter with parasitic capacitors is shown in figure 1. Providing that during one operating period, input voltage $V_i$ is a constant; parasitic capacitor $C_{gd}$ and $C_{gs}$ are gate-drain and gate-source capacitors; the voltage drop of the diode is $u_D$ and the turn-on voltage drop of the SiC MOSFET is zero. $V_G$ is the peak voltage of the PWM signal produced by the voltage regulator.

![Boost Converter Diagram](image)

**Figure 1. Boost converter with parasitic capacitors**

Under continuous conduction mode (CCM), the boost converter has two working states [13]. In typical boost converter analysis, the SiC MOSFET behaves as an ideal switch, which means the boost converter switches between two working states instantaneously. In reality, the existence of parasitic capacitors can cause a switching delay, and thus influence the input-output relationship. To analyze that influence in detail and deduce the transfer function of the boost converter circuit with parasitic parameters, the following converter operating mode is considered.

According to the characteristics of SiC MOSFETs [14], one operation period of the boost converter can be divided into multiple operating stages. Take the turn-on process as an example.

**a) 0–$t_1$: Sub-threshold**

Right after the voltage regulator outputs $V_G$, the device is still off while the gate voltage starts to rise, until it reaches the threshold. In this stage, $V_G$ charges capacitors $C_{gd}$ and $C_{gs}$. According to KCL,

$$ \frac{V_G - V_D}{R_G} = (C_{gs} + C_{gd}) \frac{dV_G}{dt} $$

The duration of this stage is given by

$$ t_{0-1} = (C_{gs} + C_{gd})R_G \ln \frac{V_G}{V_G - U_{th}} $$

**b) $t_1$–$t_2$: Current Climbing**

In this stage, due to the clamping effect of the diode, drain voltage remains unchanged. The two parasitic capacitors continue being charged. At the same time, channel current increases from zero, until the device approaches Miller Plateau. The channel current is approximately equal to the drain current and given by [6]

$$ i_d = (V_G - U_{th})g_{fs} $$

where $g_{fs}$ is the transconductance of the SiC MOSFET. This stage lasts until commutation finishes and the drain current reaches $i_{on}$. Thus, the gate voltage during Miller Plateau is given by

$$ V_p = \frac{i_{on}}{g_{fs}} + U_{th} $$

The duration of this stage is

$$ t_{1-2} = (C_{gs} + C_{gd})R_G \ln \frac{V_G - U_{th}}{V_G - V_p} $$
c) $t_2$ to $t_3$: Turn-on Miller Plateau

During the Miller Plateau stage, the clamping effect removes, the change of the gate voltage is much less than that of the drain voltage. Thus, $V_G$ can be considered to charge $C_{gd}$ merely. According to KCL,

$$C_{gd} \frac{d(v_p-v_d)}{dt} = \frac{v_G-v_p}{R_G}$$

Thus, $V_d$ decreases linearly with a slope of $-\frac{v_G-v_p}{C_{gd}R_G}$. This stage terminates when the drain voltage decreases to zero.

The duration of this stage is

$$t_{2-3} = \frac{v_o+u_D}{v_G-v_p} C_{gd} R_G$$

(7)

d) $t_3$ to $t_4$: Operation State 1

After the Miller Plateau stage, the gate voltage still increases, that change would bring a negligible effect to the main loop and the device has already been conducted since $t_3$.

During $t_3$ to $t_4$, the boost converter is under the Operation State 1 and $t_4$ is equal to $DT$, where $D$ is the duty cycle of the voltage regulator, and $T$ is the period of the square wave in PWM. The duration of this stage is

$$t_{3-4} = DT - \Delta t_{on}$$

(8)

where

$$\Delta t_{on} = t_{0-1} + t_{1-2} + t_{2-3}$$

(9)

The same ideas can be applied when analysing the turn-off process. The features of eight operating stages are shown in Table 1.

| Order | Operating Stage       | Inductor Voltage | Duration                                      |
|-------|-----------------------|------------------|------------------------------------------------|
| 1     | Sub-threshold         | $V_i - V_o - u_D$ | $(c_{gs} + c_{gd})R_G \ln \frac{V_G}{V_0 - U_{th}}$ |
| 2     | Current Climbing      | $V_i - V_o - u_D$ | $(c_{gs} + c_{gd})R_G \ln \frac{V_G}{V_0 - U_{th}} - \frac{V_G - V_p}{V_G - V_p}$ |
| 3     | Turn-on Miller Plateau| $V_i - V_o - u_D + \frac{V_G - V_p}{C_{gd}R_G} t$ | $\frac{V_o + u_D}{V_G - V_p} C_{gd} R_G$ |
| 4     | Operation State 1     | $V_i$             | $DT - t_{on}$                                  |
| 5     | Voltage falling       | $V_i$             | $R_G (c_{gs} + c_{gd}) \ln \frac{V'_p}{V'_p}$ |
| 6     | Turn-off Miller Plateau| $V_i - \frac{V'_p}{C_{gd}R_G} t$ | $(V_o + u_D) \frac{C_{gd} R_G}{V'_p}$ |
| 7     | Current Falling       | $V_i - V_o - u_D$ | $R_G (c_{gs} + c_{gd}) \ln \frac{V'_p}{U_{th}}$ |
| 8     | Operation State 2     | $V_i - V_o - u_D$ | $DT - t_{off}$                                |

where $V'_p$ is the Miller voltage in the turn-off process and is given by

$$V'_p = \frac{i_{off}}{g_{fs}} + U_{th}$$

(10)

Compare with the change during the normal operation states, the change of inductor current $i_L$ during switching is negligible. At Operating State 1, the inductor is charged by the input voltage of the Boost converter, and its current increase linearly with a slope of $\frac{V_i}{L}$. Providing $DT >> t_{on}$, $i_{off}$ can be calculated as [8]

$$i_{off} = \frac{V_i}{L} DT + i_{on}$$

(11)

Thus, the relationship between turn-on and turn-off Miller voltage is shown in formula (14).
\[ V_p' = V_p + \frac{V_p DT}{I_d f_s} \]  

The turn-off time can be written as
\[ \Delta t_{off} = t_4-5 + t_5-6 + t_6-7 \]  

3. Voltage Regulator Design

In this paper, the feedback control system of the boost converter is considered to be a single-loop control system [15]. Its block diagram is shown in Figure 2.

![Figure 2. The closed-loop control system of the boost converter](image)

In each operation period, the difference between the output voltage \( V_o \) and the reference voltage \( U_{ref} \) is sent to the PID controller as the control error \( e(t) \). The PID controller then outputs a DC voltage \( u_{pid} \) to tune the duty cycle in PWM. As a control variable, the duty cycle \( D(t) \) is going to adjust the operating point of the boost converter and produce a new output level.

3.1. The PID Controller

A feedback controller with proportional, integral, and derivative control is considered and given in formula [16] (14)
\[ u_{pid}(t) = K_p e + \frac{K_p}{T_i} \int_0^t e \, dt + K_p T_d e \]

where \( u_{pid} \) is the controller output, and \( e \) is the control error signal
\[ e(t) = U_{ref} - V_0 \]

\( K_p, T_i \), and \( T_d \) represent proportional gain, integrate time, and derivative time, respectively.

3.2. The PWM Transfer Function

In the Pulse-Width Modulation (PWM), \( u_{pid} \) is used to compare with a sawtooth wave to output the duty cycle \( D(t) \). The PWM transfer function is given in formula [14] (16)
\[ \frac{D}{u_{pid}} = \frac{1}{K} \]

where \( K \) is the rising slope of the sawtooth wave.

3.3. Main Loop Input-Output Function

At steady-state, within one period, the electric energy that is stored by the inductor in the boost converter is zero.

The inductor voltage is integrated over one operating period.
\[ \int_0^T V_L(t) \, dt = \int_0^T V_i \, dt - \int_0^{t_3} (V_o + u_o) \, dt + \int_{t_3}^{t_4} (V_o + u_o) \, dt + \int_{t_2}^{t_3} \frac{V_o - V_p}{C_{gs} R_G} \, dt - \int_{t_5}^{t_6} \frac{V_p'}{C_{gd} R_G} \, dt \]  

Thus, the average inductor voltage over one period is given by
\[ \overline{V_L(t)} = V_i - (V_o + u_o)D' + \frac{\tau_1}{T} \ln \left( \frac{V_o + u_o}{V_o} \right) + \frac{\tau_2}{2T} \left( \frac{1}{V_o - V_p} - \frac{1}{V'} \right)(V_o + u_o)^2 \]

where the time constants \( \tau_1 \) and \( \tau_2 \) are
\[ \tau_1 = R_G (C_{gs} + C_{gd}) \]  

\[ \tau_2 = \frac{1}{2} \left( \frac{1}{V_o - V_p} - \frac{1}{V'} \right) \]

\[ \tau_3 = \frac{1}{C_{gs} R_G} \]

\[ \tau_4 = \frac{1}{C_{gd} R_G} \]

\[ \tau_5 = \frac{1}{C_{gs} R_G} \]

\[ \tau_6 = \frac{1}{C_{gd} R_G} \]
At steady-state, \( V_i(t) \) is equal to zero. Thus, formula (18) can be written as

\[
V_i = (V_o + u_D)D' + \frac{\tau_1}{T} \ln \frac{V_G - V_p}{V_p'} (V_o + u_D) - \frac{\tau_2}{2T} \left( \frac{1}{V_p'} - \frac{1}{V_G - V_p} \right) (V_o + u_D)^2 = 0
\]

(21)

where \( u_D \) appears in pair with \( V_o \), corresponding to the effect of the diode. The extra linear term describes the effect of SiC MOSFET switching delay before and after the Miller Plateau due to the charging of parasitic capacitors, while the quadratic term describes the delay effect during two Miller Plateaus.

Equation (21) is a non-linear input-output equation. In the control process, the output voltage in each period is calculated by solving the equation for \( V_o \) (see Section 3.4).

Equation (21) can also be written as

\[
\frac{V_o + u_D}{V_i} = (D' - k_1 + k_2)
\]

(22)

For small disturbance, equation (22) can be linearized with respect to the steady-state operating point, by substituting \( V_o \) on the right-hand side with \( U_{ref} \). The input-output function is given in formula (23)

\[
V_i = (V_o + u_D)[D' - k_1 + k_2]
\]

(23)

where \( k_1, k_2, V_o \) are given by

\[
k_1 = \frac{\tau_1}{T} \ln \frac{V_G - V_p}{V_p'}
\]

(24)

\[
k_2 = \frac{U_{ref} + u_D}{2V_e}
\]

(25)

\[
V_o = \frac{T}{\tau_2} \left( \frac{1}{V_p'} - \frac{1}{V_G - V_p} \right)^{-1}
\]

(26)

If all the parasitic parameters and the voltage drop of the diode are neglected, the input-output function becomes

\[
V_i = V_o D'
\]

(27)

By comparing Equation (23) and (27), it can be concluded that under small disturbance, the boost converter modelled in this paper is approximated as a shifted ideal system.

For a given SiC MOSFET, the duty cycle is limited by the turn-on and turn-off time, which is shown below.

\[
D > \frac{\Delta t_{on}}{T}
\]

(28)

\[
1 - D > \frac{\Delta t_{off}}{T}
\]

(29)

Thus, the range of the duty cycle is given by

\[
\frac{\tau_1}{T} \ln \frac{V_G}{V_G - V_p} + \frac{\tau_2 V_o + u_D}{T} \left( \frac{V_G}{V_G - V_p} \right) < D < 1 - \left( \frac{\tau_1}{T} \ln \frac{V_G}{V_{th} + D_j} + \frac{\tau_2 V_o + u_D}{T} \right)
\]

(30)

3.4. Feedback Control Simulation

3.4.1 Simulation algorithm design

To implement the voltage feedback control system, the discretization form of the PID controller should be determined. Riemann sum and Backward Euler are used to discretize the integral control and the derivative control, respectively, equation (14) becomes

\[
u_{pid,j} = K_p e_j + \frac{K_p}{\tau_1} \sum_{m=0}^{j} e_m \delta t + K_p T_d \frac{e_{j+1} - e_j}{\delta t}
\]

(31)

According to the design specified by a given source voltage \( V_i \) and target output \( U_{ref} \) after the duty cycle \( D \) has been calculated by the PID controller, the output voltage for each operation period of the boost converter is obtained

\[
V_o,j = V_e \left[ k_1 - D_j' + \left( (D_j' - k_1)^2 + \frac{2V_e}{V_e} \right)^{1/2} \right] - u_D
\]

(32)
3.4.2 Simulation Parameters
The model has been evaluated using the SiC device, CPM2-1200-0080B (Wolfspeed). The values of the parasitic capacitances and conduction parameters have been obtained from the device datasheet. As a high frequency, high voltage application, the simulation parameters are listed in Table 2.

Table 2. Simulation parameters

| Parameter | Value | Parameter | Value |
|-----------|-------|-----------|-------|
| $K_p$     | $5.26\times10^{-6}\text{s}$ | $C_{gv}$ | 95pF |
| $K$       | 500000 V/s | $C_{gdmin}$ | 7.6pF |
| $f_{sw}$  | 50kHz | $C_{gdmax}$ | 800pF |
| $T_t$     | $\pi/40500$ s | $g_{fs}$ | 8.1$\Omega$ |
| $T_d$     | 0.2 s | $U_{th}$ | 5.5V |
| $U_{ref}$ | 700V | $R_{DS(on)}$ | 80m$\Omega$ |
| $V_i$     | 350V | $R_G$ | 5$\Omega$ |
| $L_1$     | 2mH | $V_G$ | 20V |
| $C$       | 500$\mu$F | $V_p$ | 5.3V |
| $R$       | 500$\Omega$ | $V_p'$ | 5.5V |

3.4.3 Simulation Result and Analysis

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig3.png}
\caption{Simulation result i) in an ideal case; ii) with parasitic parameters}
\end{figure}

a) Figure 3 shows a voltage control system with and without parasitic parameters. Comparing with the ideal case, the maximum overshoot of the boost converter with parasitic parameters changes from 524.66V to 486.55V; the settling time decreases from 0.0135s to 0.0030s; the steady-state error decreases from 11.351V to 3.279V.

b) The response characteristics over the value of the parasitic parameters are illustrated below. The values of $C_{gs}$ and $C_{gdmin}$ had a minimum effect on the settling time of the boost converter. But with the increasing of $C_{gs}$ and $C_{gdmin}$, the maximum voltage overshoot $M_p$ and the steady-state error $e_{ss}$ were increased linearly. The value of $C_{gd}$ could improve the response characteristics of the boost converter. With the increasing of $C_{gd}$, the settling time of the response $t_s$, maximum voltage overshoot $M_p$ and the steady-state error $e_{ss}$ were all decreased.
Figure 4. Settling Time vs. Parasitic Capacitances

Figure 5. Maximum Overshot vs. Parasitic Capacitances
4. Energy Loss Analysis

4.1. Power Loss Calculation

The power loss of the Boost converter consists of three main parts. Conduction loss is the power dissipated by the conduction resistance $R_{on}$ when the SiC MOSFET is conducted and work at its linear region. Switching loss is due to the Joule heat produced by channel current during switching transient. The last part of the power loss comes from the charge of the parasitic capacitors.

The conduction loss is given by [8]

$$P_{CND} = i_{on}^2 R_{on} D$$  \hspace{1cm} (33)

Switching energy loss within one period can be derived by using the integral of the product of drain current and drain voltage over one operation period.

$$P_{sw} = \int_0^T i_d(t)v_d(t) \, dt$$  \hspace{1cm} (34)

During stage $b)$ of the turn-on process, the drain voltage is clamped to be a constant $V_o + u_D$, and the drain current is climbing with the gate voltage. During the next stage, the drain current is almost unchanged, while the drain voltage decreases linearly.

Therefore, the switching power loss can be calculated by formula (35)

$$P_{sw} = \frac{f_{sw}(V_o + u_D)}{2} (i_{on}t_{1-3} + i_{off}t_{5-7})$$  \hspace{1cm} (35)

Where the switching frequency is $f_{sw} = \frac{1}{T}$.

The power loss due to charging parasitic capacitors is given by [7]

$$P_{CRG} = \frac{f_{sw}}{2} \left[ C_{gs} V_G^2 + (C_{ds} + C_{gd})(V_o + u_D)^2 \right]$$  \hspace{1cm} (36)

Thus, the total power loss due to switching is calculated by the formula (37).

$$P_T = P_{CND} + P_{sw} + P_{CRG}$$  \hspace{1cm} (37)

4.2. Simulation

Under the influences of the parasitic parameters, the simulation results of the total power loss are shown in figure 7.

Figure 6. Steady State Error vs. Parasitic Capacitances
The results illustrate that among all the three parts of the power loss, conduction loss plays the least significant role in the entire power loss calculation and is only determined by on-state resistance of the SiC MOSFET. Switching loss is the most critical one and accounts for around 50% of the total loss, followed by power loss due to charging, which is around 38.8%.

Different from the little influence exerted by $C_{gs}$ and $C_{gdmin}$, the total power loss increases linearly with the increase of $C_{gdmax}$ and $C_{ds}$. Specifically, the switching loss is almost merely determined by $C_{gdmax}$.

4. Conclusion

In this paper, a boost converter model with SiC MOSFET parasitic capacitors and a voltage feedback control system are presented. The voltage regulator consists of a PID controller, a Pulse-Width Modulation controller, and the main converter loop. In steady-state, the transfer function was derived and linearized with respect to the reference output voltage. According to the characteristics of the MOSFET, one operation period of the boost converter can be divided into eight operating stages. During computer simulation, the switching delay and parasitic capacitors charging are taken into account. Finally, switching loss of the converter is also analyzed by using the model obtained.

The simulation results showed that:

1) The gate-drain capacitance was the key influence factor of the given boost converter due to the parasitic effect. With the increase of its value, the settling time, maximum overshoot, and the steady error of the system response were decreased.

2) The switching loss which was determined by the gate-drain capacitance also accounted for the most significant component of the total power loss.

For future research, we will optimize the design of the voltage feedback control method to improve the response characteristics of the boost converter and reduce the total power loss.

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