METRO: A Software-Hardware Co-Design of Interconnections for Spatial DNN Accelerators

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Abstract

Tiled spatial architectures have proved to be an effective solution to build large-scale DNN accelerators. In particular, interconnections between tiles are critical for high performance in these tile-based architectures. In this work, we identify the inefficiency in the widely used traditional on-chip networks and the opportunity of software-hardware co-design. We propose METRO with the basic idea of decoupling the traffic scheduling policies from hardware fabrics and moving them to the software level. METRO contains two modules working in synergy: METRO software scheduling framework to coordinate the traffics, and METRO hardware facilities to deliver the data based on software configurations.

We evaluate the co-design using different flit sizes for synthetic study, illustrating its effectiveness under various hardware resource constraints, in addition to a wide range of DNN models selected from real-world workloads. The results show that METRO achieves 56.3% communication speedup on average and up to 73.6% overall processing time reduction compared with traditional on-chip network designs.

1. Introduction

Recently, spatial architectures have become a popular solution to build high throughput accelerators for deep neural networks (DNNs). A spatial architecture normally consists of many processing elements (PEs) and a memory hierarchy \cite{4,5,12,14,18,25,32}. As its computation throughput scales up to hundreds of Tera Operations Per Second (TOPS), the huge number of PEs in a spatial accelerator are organized hierarchically. Multiple PEs are organized as a group, also called tile in this work. These tiles are normally connected with an on-chip interconnection to enable data communication during processing.

A flexible on-chip interconnection is critical for high performance spatial accelerator design. First, to handle diverse dimensions of DNN layers, researchers propose different dataflows to improve data reuse and reduce data communication \cite{4,6,9,11,20,31}. When processing a DNN layer, the dataflow describes the assignments and execution sequence of its computation tasks on the tiles of a spatial accelerator \cite{25}. Second, to improve its hardware utilization and processing efficiency, researchers propose to process multiple DNN layers on a high performance spatial accelerator \cite{12,14,32}. As each DNN layer may be processed with a different dataflow, it further complicates the data communication patterns. Consequently, the goal of this work is to design a flexible, high performance, and low cost on-chip interconnect for high performance spatial accelerators.

A straightforward solution is to connect the tiles in spatial accelerators with a network-on-chip (NoC) \cite{12,14,32}. However, we argue that traditional NoCs designs are inefficient for spatial DNN accelerators for three reasons. First, traditional NoCs are not elastic enough to handle the bursting bandwidth requirements in DNN processing efficiently \cite{20,22,23}. Second, traffic scheduling policies (e.g., routing and flow control) of traditional NoCs are fundamentally lost the global information \cite{7}, no matter the scheduling is adaptive \cite{10} or deterministic \cite{27}. Third, in traditional NoCs, the scheduling choices are made by hardware. This approach not only increases NoC implementation costs but also induces choice-making delay to the data delivering process. These inefficiencies of traditional NoC designs make spatial accelerators, which adopt traditional NoCs to deliver data between tiles, spend considerable resources on the interconnections to meet their communication requirements. For example, in Simba \cite{32}, the interconnections (including NoCs and NoPs) consume 18.5% area in total.

To address the inefficiency of traditional NoCs, we propose METRO, a software-hardware co-design interconnection for spatial DNN accelerators, with two major insights. First, METRO decouples the traffic scheduling policies from hardware fabrics and moves them to the software level. This is inspired by the determinism of DNN processing. With the specified workloads and given dataflows, we could obtain the entire traffic information of the execution in advance. METRO leverages this feature to dedicate scheduling policies for every workload with software approaches. Second, we simplify the network device implementation, which works with low-level configuration from the software. With the two insights, we propose two components of METRO which work in synergy: METRO software framework that performs traffic status extraction, routing, and flow control; METRO hardware router design that forwards traffic flow with the configuration from the software framework.

The main contributions of this work are listed as follows:

- We identify the inefficiency of traditional NoCs and clarify their fundamental drawbacks.
- We propose, design, and implement METRO, a software-
hardware co-designed interconnection to achieve higher data transmission efficiency.

- Our evaluations using cycle-accurate simulation and widely-used DNN models show that METRO greatly improves data transmission efficiency in terms of energy and time over the basic NoC design. It achieves up to xx communication speedup, as well as up to 73.6% overall processing time reduction.

The rest of this paper is organized as follows: We first introduce the backgrounds in Section 2 and illustrate the motivations of this work in Section 3. Section 4 first introduce the basic rationales of METRO, following with detailed descriptions on software (Section 5) and hardware (Section 6). We test our proposal in Section 7 and conclude our work in Section 8.

2. Background

2.1. Spatial DNN Accelerators

Spatial architectures refer to a category of architecture paradigms, which employ massive simple processing elements (PEs) to exploit the high computing parallelism of applications. For DNN applications, a typical PE can perform a single or multiple multiply-and-accumulate (MAC) operations at a time. To leverage data reuse, a spatial accelerator normally employs a memory hierarchy, which may include PE registers, on-chip scratchpad memory, and HBM or off-chip DDR memory [20, 21, 25]. PEs and memory components are connected with carefully designed interconnections to enable efficient data movement.

To keep pace with the rapid advancement of DNN models, the computing throughput of spatial accelerators scales up to tens or hundreds of TOPS [1, 3, 14]. And the number of PEs in a spatial accelerator also increases rapidly at the same time. Consequently, to facilitate PE management, massive PEs in a spatial accelerator are also organized in a hierarchical style [1, 3, 12, 34, 37]. As shown in Figure 1, multiple PEs are grouped together as a tiled processing engine (i.e. tile). Each tile may contain a global buffer shared by all of its PEs. Then, these tiles are further manipulated to achieve high processing throughput.

Having a spatial architecture, the next critical step is to design the so called dataflow for the architecture. As addressed in prior works [12, 20, 21, 25, 28], a dataflow refers to the implementation of DNN operations on a spatial architecture. As most DNN operations can be described using loop nests, a spatial DNN accelerator’s dataflow handles two important issues: 1) how to map a loop instance to PEs, 2) how to execute the mapped loop instance on PEs [25]. For a spatial architecture, the dataflow actually determines the data transfer among PEs and memory components.

2.2. Multiple Layer Processing on a Spatial Accelerator

We assume a DNN layer is assigned to one or more tiles and is processed with the following execution steps:

1. Each tile fetches a tile of weights from the off-chip memory to its private buffer. The data is delivered with a traffic flow from memory controllers to the tile.
2. Similar to fetching weights, each tile fetches a tile of input activations from the off-chip memory to the private buffer.
3. Tiles compute and generate partial results, which are temporarily stored in the private buffers.
4. Select a tile T to accumulate partial results. T will reduce them if the layer execution scheduling requires.
5. Pipeline the off-chip memory fetching, computing, and reducing (i.e., we assume double buffer for inputs, weights, and outputs). Prefetch the input activations and weights for the next iteration, and forward the partial results of the last iteration to T during tiles are computing.
6. When a layer is finished, set tile T to serve the input activations for the next layer, taking part of memory controllers to reduce off-chip memory access. When the buffer of T is insufficient for holding the entire intermediate activations, it saves the activations back to off-chip memory in a tiled manner, resulting in the traffic from T to the memory controllers. When the data transmission is blocked due to traffic contention, the pipeline is described in step 3 will stick waiting for the completion of the transmission.

3. Motivation

3.1. Requirement for Flexible Interconnection

A flexible interconnection is necessary for spatial architectures. Reasons are many folded: first, due to the diverse dimensions and types of DNN layers, different dataflows should be adopted to improve data reuse and hardware utilization [5, 25, 28]. Accordingly, the interconnection of a spatial accelerator should support various dataflows.

Second, as the computation capacity of a spatial accelerator scales up, processing a single DNN layer using all tiles is becoming less efficient. As pointed out by a previous work [32], the increasing communication overhead makes a layer’s processing communication-bounded. To this end, it
has become a common trend to process multiple layers from a DNN model on high throughput spatial accelerator simultaneously [3,12,32,34,34,37]. It means that a spatial accelerator is partitioned into multiple disjoint regions, which may operate under different dataflows. Thus, tiles in these regions may also need different interconnections.

Third, in many practical scenarios (e.g. autonomous driving), an application includes multiple DNN models. Thus, multiple layers from multiple models should also be processed at the same time, greatly increasing the communication complexity of spatial accelerators.

To satisfy these requirements, a network-on-chip (NoC) should be used to connect the tiles and enable flexible data transfer, as shown in Figure 1. Prior works have employed different NoC designs to enable flexible dataflows [5,22,23], multi-layer processing [21] and both of them [1,3,32]. However, we found that traditional NoC designs cannot handle the data transfer on spatial NN accelerators efficiently, considering both their performance and their design overheads. More details are presented in the following two subsections.

### 3.2. Traffics in Spatial Accelerators

Under a dataflow, the data traffic in a DNN spatial accelerator exhibits explicit regularity [20,22,28]. Without loss of generality, we classify the traffic into three primary communication patterns, as shown in Figure 2. **Multicast** pattern delivers input data (e.g. feature maps and layer weights) from a source tile to a group of destination tiles for parallel computing. Particularly, the multicast degrades to unicast when the group size is 1. **Reduce** pattern collects intermediate results (e.g. partial sums) from multiple source tiles to one destination tile. **Link-Transfer** pattern represents one-to-one data transfer among tiles. It normally happens when the data are shared among tiles to improve data reuse. Data traffic in a systolic array dataflow and row sharing dataflow [4] are two typical cases that contain **Link-Transfer** patterns.

Among these patterns, **Link-Transfer** can be easily handled without causing contention [18,19]. However, both **Multicast** and **Reduce** patterns are very possible to incur traffic contention. We will discuss it in the next section.

### 3.3. Baseline Architecture and Its Inefficiencies

We focus on the implementation of **Multicast** pattern and **Reduction** pattern on interconnections. We illustrate the fundamental inefficiency of traditional hardware scheduled on-chip network designs.

#### 3.3.1. Baseline Routing of Patterns:

The baseline interconnection architecture implements all the traffic patterns with uniform one-to-one unicasts. For example, the **Multicast** is implemented by sending a separate copy of data from source to each destinations, and the **Reduce** sends multiple partial sums individually to the reduction node. However, this unicast-based implementation will result in serious contention, which is enabled by two major reasons.

We use a simple spatial architecture with 3×3 tiles to illustrate its inefficiency in Figure 3. The tiles are connected with a typical mesh NoC with X-Y routing policy. We assume that two DNN layers are mapped to dedicated tiles following the specific dataflows. With the baseline implementation, the first reason of contention is that the massive unicast flows increase the entire traffic of the network. For example, to deliver the input feature maps, two **Multicast** patterns are introduced from the memory controller, as shown in Figure 3 (a). And these **Multicast** patterns incur bursting number of unicast flows from the memory controller, making very heavy burden on channel resources.

The second reason is the natural hotspots of DNN traffic patterns. Because the unicast flows drawn by the same pattern shares the same traffic sources ( **Multicast** ) or destinations ( **Reduction** ), making channels around these nodes to be loaded relatively heavier. For example, all the traffic flows forwarding input feature maps need to pass the channels around MCs, making these channels overwhelmed. In addition, when the computation finishes, partial sums of different tiles are accumulated by a specific tile to perform reduction. And two **Reduce** patterns take place on the tiles assigned to two layers, separately. The traffic flows caused by a **Reduce** have the same destination. Since they are issued simultaneously, these **Reduce** destination tiles also become the hotspot.

#### 3.3.2. Baseline Flow Control:

Previous works proposed various flow control mechanisms to provide backpressure by informing the upstream nodes whether the downstream chan-
Without loss of generality, the baseline architecture employs a dedicated software scheduling policy to guide the traffic pattern among spatial accelerator tiles. This phenomenon starts with some channels adjacent to the hotspot resources being overwhelmed by the heavy traffic load caused by the routing inefficiency, as mentioned in the last subsection. These overwhelmed channels form the first level of the tree. This effect continues to influence the channels two hops from the resource to wait on the congested channels in the first level. The resulting structure of blocked channels forms a tree. The spread of contention in hotspots is due to the delay of routers to respond to the congestion. The queues between the decision point and the blocked point should be fulfilled completely before the decision point sense the contention. However, multiple flows have already been sent to worsen the traffic status. The limitation of the backpressure methods is the propagation delay of the contention information, which will cause tree saturation. The tree saturation is the universal effect of hotspots on those traffic flows not requesting the hotspot resources, spreading the local contention to the whole network. This phenomenon starts with some channels adjacent to the hotspot resources being overwhelmed by the heavy traffic load caused by the routing inefficiency, as mentioned in the last subsection. These overwhelmed channels form the first level of the tree. This effect continues to influence the channels two hops from the resource to wait on the congested channels in the first level. The resulting structure of blocked channels forms a tree. The spread of contention in hotspots is due to the delay of routers to respond to the congestion. The queues between the decision point and the blocked point should be fulfilled completely before the decision point sense the contention. However, multiple flows have already been sent to worsen the traffic status.

4. METRO Overview

In this section, we propose METRO, a novel software-hardware co-design approach to implement efficient inter-tile interconnection for spatial DNN accelerators. The first insight of METRO is to decouple the traffic scheduling policy from hardware fabrics and move it to the software level. The rationale is that, after mapping DNN layers to a spatial accelerator, the data traffic among these tiles is deterministic. According to the layer processing dataflows, we can obtain the full knowledge of 1) the source and the destination of each traffic pattern and 2) the timing when each traffic pattern is issued. Having the knowledge, we can prepare a dedicated software scheduling policy to guide the traffic during DNN layers processing. Compared to the traditional hardware approach, the advancement of a software scheduling approach lies in two folds. First, with knowing the sources and destinations of each traffic patterns, the software scheduling approach is able to harmony the their paths with global view to minimize the sharing channels. Second, with knowing the issue time, the software approach can estimate the occurrence of traffic contention precisely, which provides the opportunity to minimize their effects on others, or even avoid them in advance.

Having the software scheduling approach, we present the second key insight of METRO: the underlying hardware fabric of interconnection can also be simplified substantially. The hardware components in traditional NoC, as an example, credit management module for deciding whether to forward flits, can be removed.

The overall flow of METRO is illustrated in Figure 4. We first design the software traffic scheduling framework taking the workload descriptions and dataflow specification. The METRO framework answers two major questions on traffic scheduling: (1) Which paths do the traffic flows take from source to destination, i.e., the routing problem. (2) When are the flows injected into the network, i.e., the flow control problem. Specifically, the framework first extracts the traffic status from specified workloads based on tensor analysis approaches. After that, the routed path of traffic flows are optimized heuristically to improve the traffic efficiency. And follow with it, the injection control harmonies the injection timing of traffic. The resulted scheduling policies are dumped as configurations of hardware fabrics. And we build the cycle-accurate latency model to estimate the performance of the present scheduling. The performance will further guide the tuning of scheduling policies. The recurrence will continue until the algorithm finds the best solution or meets ending conditions.

In addition to software proposals, we co-design the communication architectures to facilitate the software scheduling policies with efficiency. Specifically, we design the routers enabling the hybrid routing mechanism to reduce the bit overheads of dual-phase routing policies. And then, we propose the chunk-level flow control specialized for the DNN processing traffics.

5. Software Scheduling Framework

The working flow of METRO’s software scheduling framework is illustrated in Figure 5, which consists of four steps.

- **Step-1.** The descriptions of both DNN model layers and mapping results on the spatial accelerator are sent into the framework as input. An example is shown in Figure 5 (a).
VGG16_layer1 and Resnet50_layer2 will be processed on the same spatial accelerator. VGG16_layer1 is mapped to tile 1 – 3, while Resnet50_layer2 is mapped to tile 4 – 7.

- **Step-2.** The communication status is constructed from the workload descriptions, the example is shown in Figure 5 (b). It contains all information to generate the scheduling policy. The detailed method for status construction is introduced in subsection 5.1.

- **Step-3.** Having the traffic status, a dual-phase routing method is proposed to find the routing paths for each traffic flow, as shown in Figure 5 (c). This dual-phase routing can help reduce the amount of traffic, which is presented in subsection 6.1.

- **Step-4.** As shown in Figure 5 (d), the traffic flow control is determined to further reduce contention. Its design details are introduced in subsection 5.3.

Before introducing the details of software scheduling, we make two assumptions, which are common cases in practice. First, each DNN layer is mapped to the tiles in a consecutive region to reduce communication overhead.

Second, a double buffer design is employed in each tile to overlap communication and computation. Thus, the scheduling problem turns out to be a latency-objective QoS problem. It means that the scheduling policies try to hide the communication latency by the computation latency.

### 5.1. Communication Graph Generation

METRO uses a set of traffic flows with two or more terminals to represent the entire traffic status. A traffic flow describes a communication pattern mentioned in section 3.2 in logic, and its implementation relies on the routing and injection control mechanisms, which will be discussed as follows. A traffic flow has two parameters to formulate spatial traffic behaviors: (1) volumes, which denotes the size of transmitted data, and (2) participators, involved terminals including traffic sources and destinations. And one parameter to describe temporal features: ready time, when the data is generated by the sources and tends to be injected into the network. Particularly, we use the traffic flow with a single source and a single destination to represent the general one-to-one data transmission.

We construct the traffic status descriptions for each DNN layer via spatial-temporal analysis. Specifically, we track the mapped tensors for each tile at every cycle and generate the traffic flows based on the tensor variation between two consecutive cycles. For example, if the two tiles A and B require the same new tensor held by another tile C at the last cycle, we generate a traffic flow of Multicast with three terminals, including tile C as the source and tile A and B as destinations. And the volume of this traffic pattern is the tensor size.

### 5.2. Dual-Phase Routing

The routing methods allocate the physical forwarding path for every traffic flow on the spatial accelerator. We perform the static routing for the entire traffic in software framework. Particularly, we propose a dual-phase routing method to reduce the overall traffic amount induced by Multicast and Reduce patterns to alleviate the potential traffic contention.

#### 5.2.1. Descriptions of basic ideas:

We use an example of Multicast pattern (VGG16_layer1 in Figure 5) to explain how the dual-phase routing method works. In this example, VGG16_layer1 is mapped onto tile 4 – 7. The memory controller (MC) needs to broadcast the input data to all these tiles. First, we select a tile, denoted as the multicast “hub”, from four destination tiles. In this example, tile-4 is selected as the “hub”. Then, the Multicast is operated in two phases: (1) transmitting the input data from the source to the “hub” using a single one-to-one flow and (2) broadcasting the input data to all destination tiles from the “hub”. The case for a Reduction pattern is similar. Data from multiple sources are first aggregated at the “hub”. Then, the reduced data are sent to the destination using a single unicast flow.

To enable dual-phase routing for Broadcast, we need to solve three problems: (1) selecting a “hub”, (2) finding the path from the source to the “hub” in the first phase, and (3) finding the paths for broadcasting in the second phase. The case for Reduce is similar but in a reverse style. Theoretically, given all traffic flows, there exist a global optimal solution for these problems. However, it is challenging to find the optimal solution due to the huge search space. Thus, in our...
current implementation, we solve these problems separately and provide a heuristic solution for each of them.

- **“Hub” selection.** For each layer, we select the tile, which has the minimum Manhattan distance from the source (for Multicast) or destination (for Reduce), as the hub.
- **Phase-1 Routing.** We adapt the idea of oblivious routing to balance the traffic. Specifically, we employ the Evolutionary Algorithm (EA) to search a sequence of intermediate nodes, and employ the X-Y routing to determine the path between two intermediate nodes.
- **Phase-2 Routing.** We use Breath First Search (BFS) to build the spanning tree rooted from the “hub” for the lowest propagation depth. And we perform tree-based multicast distribute the flow to all destinations.

Evaluation results show that these heuristic methods can provide promising solutions. Note that the users may propose use their own methods if needed.

### 5.2.2. Benefits of dual-phase routing:

In both of the two collective communication patterns, traffic occurs between a single terminal node \(s\), and a group of participating nodes \(G\). Particularly, the group \(G\) is located at a consecutive region in spatial, while \(s\) is relatively remote to \(G\). In conventional unicast-based routing methods, the collective communication patterns are performed by sending a separate flow between \(s\) and each node in \(G\). The major drawback of this scheme is that multiple flows are injected to traverse a relatively long distance between \(s\) and \(G\).

The dual-phase routing reduces the total traversing hops by inducing an intermediate hub node \(h\) for each flow. Node \(h\) locates within the physical region of \(G\), and works as the agency of \(s\). The node \(h\) performs one-to-one communication with \(s\), which may go through a long path. And it performs one-to-many communication with \(G\), where the flows are transmitted within a relatively small region with few hops. For example, given the Multicast with \(m\) destinations. The average hops between the source and destinations are \(l\), and the average length between destination nodes is \(k\). The total hops of unicast-based routing are \(l \times m\), while the hops of dual-phase routing are \(k \times m + l\). Typically, there is \(l \gg k\); therefore, the promotion of dual-phase routing is given by \(l \times (m - 1) - k \times m\) hops.

### 5.3. The Slot-Based Injection Control

The injection control arranges the injection time for traffic flows. We propose software-enabled injection control to prevent the tree saturation pathology.

#### 5.3.1. Descriptions of basic ideas:

The slot-based control divides time into small fixed-size slots. We use time-division multiplexing (TDM) to allocate channel resources for traffic flows in the granularity of the time slot. TDM reserves the passing channels for a particular traffic flow and “lockdowns” them to prevent other flows from using them. The reservation will keep several time slots until the tail of flow passes, and the channels are released to be reused by other flows at that time. Knowing the information of channels’ reserved time slots, we only allow a particular traffic flow to be injected to the network when all its passing channels are released. This flow will traverse the network without meeting any channel conflicts.

We use Fig. 5 (c) (d) as an example to illustrate this injection control mechanism. In this example, we assume the wormhole flow control that the entire traffic flow is separated into a sequence of flits. And the network forwards flows flit-by-flit. With this assumption, we intuitively divide the time into the slot that a flit takes to pass a channel (passing wires and routers). As shown in the first entry of the figure, we start with injecting flow-1 at slot 1, when no traffic is in the network. And the flow-1, with two flits, takes 2 slots to pass the channel between MC and the tile array, holding it until the third slot. Consequently, flow-2, which also needs to pass this channel, is delayed to be injected at the third slot. Similarly, flow 3 also passes the same channels as flow-1. Therefore, it is injected after flow-1 releases the sharing channel.

However, the injection time of flow-3 is three slots later than flow-2. That is because the waiting channels of flow-2 and flow-3 are different. And it takes flow-1 three slots to travel between them. Consequently, flow-3 needs to wait three more slots than flow-2. This phenomenon is general among various flow control mechanisms. Therefore, we build the latency model for it. Without loss of generality, we use “flit” to represent the flow segment that a router holds at each slot.

We model the traffic flow injection as a two stage pipeline that the end-to-end delay is \(S_{2}\) = \(S_{1}\) + \(S_{3}\). The head flit traversal time is given by \(S_{tr} = H \times S_{c}\), where \(H\) is the number of hops, and \(S_{c}\) denotes the slots to traverse a single hop. Serialization time for a flow is given by \(S_{ser} = \lceil L/F \rceil\), where \(L\) denotes the bits of the flow, and \(F\) is the bit length of flits. With this latency model, we can estimate the slot-accurate holding and release time for every channel. For example, the head flit of flow-1 takes 3 slots from the output channel of MC to the channel between tile-6 and tile-7. The channel between tile-6 and tile-7 is held during slots 4 and slots 5. And that’s why flow-4 is able to be injected at slot 1, which will release this channel before flow-1 grab it.

In aforementioned example, we inject flow-1 first, and delay flow-2 and flow-3. However, we could also schedule the injection in reverse that inject flow-2 and flow-3 first. The choice of which flow goes first is a typical scheduling problem, which is proved to be an NP problem [7]. In our implementation, we adopt greedy algorithm to solve it. We assign the flow priorities based on the QoS requirements. The flow with earliest QoS requirements will be injected first, and flows will be injected concurrently as much as possible if they have no conflicting channels.

In addition, we do not use additional buffer to store the delayed flows. Instead, we keep them in the computing tile’s buffer. Because of the double-buffering assumption, the delayed data won’t disturb the computing process. How-
ever, when the next computing iteration finishes and the core switches to use this buffer, we assume the tile will be blocked if the data has not been forwarded yet.

5.3.2. Benefits of slot-based injection control: In traditional hardware-enabled injection control mechanisms, the flows are injected as long as they’re ready. However, they’re unaware of whether their passing channels is busy or not. Consequently, these flows will be very possible to be obstructed waiting for the channels in the saturation tree, as mentioned in Section 3.3. Even though they do not access to the overwhelmed resources in hot-spot regions. The saturation tree will consequently expand to the entire network, resulting in traffic overloads.

However, this injection control addresses this problem by delaying the flow that will suffer predictable channel conflicts. By making flows store in the tile buffers instead of network buffers, we alleviate the resource shortness caused by traffic contention. And we prevent tree-saturation to spread the traffic flow blocking. Furthermore, we guarantee no contention within the traffic, which could be leveraged to simplify hardware designs. (Section 6)

6. Architecture Supports

6.1. Hybrid Routing

To support the aforementioned dual-phase routing with low control overheads, we propose a hybrid routing mechanism that combines both source routing and table-based routing. We will first briefly revisit the two basic routing mechanisms with an analysis on their advantages and disadvantages. Then we will illustrate our proposal with an example.

Figure 7 (a) illustrates the commonly used source routing mechanism. In source routing, all the routing decisions are made by the source terminal. The route is prepended to the traffic flow and used to steer the flow through the network with no further computation. Routers only need to read the pre-computed output channels from the flow and forward the flits. Source routing is simple, high performance, and scalable. Furthermore, it dissociates the design of hardware routers with routing policies, enabling the fixed hardware to support flexible traffic scheduling. However, source routing is not efficient for multi-end data transmission. For multi-destination flows, the header should store a separate path for each destination resulting in high overheads of transmitting these controlling bits. Furthermore, the long channel selection field results in long decoding overheads.

In addition to source routing, another widely used routing mechanism is table-based routing, where flows only carry the destination coordination. As shown in figure 7 (b), routers decode the destination coordination and make routing decisions by looking up their local pre-configured routing tables which is easy to perform one-to-many data forwarding at each router. [13] However, this approach has two major drawbacks: (1) As performing a lookup at every step of the router, the table-based routing has long latency for a flow to pass through a router (2) Table-based routing is not scalable, since every node should contain a table large enough to hold routing decisions for all the destinations.

In this work, we adopt the two routing mechanisms to perform the hybrid routing. Note that the routing of METRO framework has two phases: 1) One-to-one routing between the hub and the source node (Multicast) and destination node (Reduce). In this phase, we can employ source routing to exploit the path diversity to balance the traffic loads and reduce the routing overheads. 2) One-to-many routing phase that transmits data within a relatively small region, when we could use table-based routing to leverage its natural broadcast capability.

Our router architecture has two separated routing modules
to support the two phases in hybrid routing mechanism. As shown in figure 6 (a). In the phase of routing data from the source to the captain tiles, routers are in the source routing mode.

The source routing module determines the output ports by extracting the first entry of the routing information field carried in the packet header. Then shifts the field to pop the first entry out. We employ 3 bits to indicate the output ports for source routing, with an additional NOP to indicate the end of the information field.

Once all the routing information entries are popped (i.e., NOP is the first entry ), the router switches to the table-based routing mode. The table-based routing module is implemented as a local look up table, which is pre-configured by software. Routers look up the routing table with flow ID to determine the output ports. Particularly, to leverage the natural broadcast capability of table-based routing, we adopt one-hot encoding for each output channel, as shown in the following table. As an example, to broadcast flow to the south and west output ports, route information is 00110, and the crossbar is configured as Figure 6 (b) illustrates.

| Source Routing (3bits) | Distributed Routing (5bits) |
|------------------------|-----------------------------|
| Output Port | Encoding | Output Port | Encoding |
| East   | 001   | East     | 00001 |
| South  | 010   | South    | 00010 |
| West   | 011   | West     | 00100 |
| North  | 100   | North    | 01000 |
| Output | 101   | Output   | 10000 |
| NOP    | 000   | NOP      |       |

To further illustrate the hybrid routing mechanism, we will go through an example that two nodes inject multicast flows to two overlapped regions. Figure 8-(a) shows parts of flow headers that are related to the routing. Flow 001 is injected to router R(0, 0), targeting the four right-bottom tiles. In this region, R(1, 1) is selected as the captain, and the spanning-tree taking R(1, 1) as the root is generated to do local broadcast. The tree topology information in the blue region is stored in the routing tables shown in Figure 8 (c1). The flow injected by R(1, 0) is routed to the region that has overlap with flow 001’s region. The flow 001 is forwarded in the source routing mode at R(0, 0) and R(0, 1). When it reaches R(1, 1), router R(1, 1) recognizes flow 001 and starts to use distributed routing mode to forward the flow. The routing table for distributed routing in Figure 8 (c1) shows that router R(1,1) needs to forward the data to east, south, and output ports. The forwarding of flow 001 has the similar process.

The overhead of distributed routing is highly related to the routing buffer’s capacity. We argue that each DNN layer will involve 3 traffic patterns at most, as each input tensor, output tensor, and weight tensor will incur one pattern at most. And a tile could only be assigned one layer at a time. Therefore, the routing table for each router will accommodate 3 entries at most.

| ID | Routing Info | Destinations |
|----|--------------|--------------|
| 01 | 001 (East, South) | ... (2,2) (2,3) (3,2) (3,3) |

| ID | Routing Info | Destinations |
|----|--------------|--------------|
| 01 | 010 (East) | ... (2,2) (3,2) |

(b) FOCUS in action with the flows

(c1) Routing Table of R (1, 1)

(c2) Routing Table of R (2, 2)

Figure 8: Routing two multicast flows to overlapped regions on a (3x3) Mesh network. Routers are indicated with their coordinates, and the left top corner router is denoted as R(0, 0). (a) parts of flows that are related for source routing; (b) the process of forwarding the flows, numbers next to arrows indicate the traversal cycles at that hop. (c) routing tables R(1, 1) and R(2, 1).

When a layer is switched on and being initialized, we upload the configuration of both table-based routing and source routing to the interconnection. As the controlling bits are relatively small compared with the computed tensor (hundreds of bits v.s. ten thousand bits ), we do not perform special optimization for the configuration in the present implementation.

6.2. Data-Chunk Level Flow Control

This section describes the data-chunk level flow control specialized for large data transmission between tiles. Figure 9-(a) shows the traditional packet-based flow control mechanism. The entire data chunk is divided into multiple messages, and each message is composed of several packets. Each packet can be further partitioned into multiple flits, which can be transmitted in a cycle. Typically, data are routed with the granularity of packets, and additional controlling bits are introduced in packets. Furthermore, the overhead of controlling bits will be large if we employ the source-routing mechanism, storing the routing path for each packet.

Note that packets of the same large data chunks share the same control information. Consequently, to mitigate traffic overhead, we expand message-based flow control in [16] to a data chunk granularity. As shown in figure 9-(b). We flatten the hierarchy of message and packet. Thus, the whole data chunk is transmitted consecutively with a single header. This approach achieves the near minimum control bits overheads to improve performance and energy efficiency.

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accurate simulators with RTL synthesis tools to estimate interconnection performance and consumption. We set the interconnection fabrics and computation tiles with the 1 GHz frequency, and we adopt the same High Bandwidth Memory (HBM) employed by TPu4 [18] as the main memory, which provides 1200 GBps memory bandwidth. We assume 8 memory controllers with 150 GBps bandwidth each. We distribute them equally to the middle of four edges.

We use timeloop [28] to estimate the computation latency of processing tiles. And we use Accelergy [38] to build the cost model of tiles in terms of area and energy, along with gem5-Alladin [2] to estimate the energy and area of primary logical components (e.g., muxes and adders), and CACTI [26] to evaluate the SRAM buffers. We adapt the hardware parameters of NVDLA cores in [32], and we scale them up 512 GOPs. We assume the tiles with double buffer to break the dependency of the communication process and computation process. We also assume a split buffer for three tensors. The detailed configuration parameters are listed in Table 1 (b).

We use Booksim2 [17] to estimate the performance of traditional on-chip networks, and we extend it to support the traffic trace extracted by METRO framework. We assume 5-port routers with virtual channel (VC) flow-controls with credit-based backpressure. We config routers with 8 virtual channels and each virtual channel with 8 flits buffers. And the 7 VCs are allocated in round-robin style, and 1 VC is reserved as an escape channel. We set the router delay as 4 cycles working in the pipeline and the bidirectional wire with 1 cycle delay.

We test the performance of baseline NoCs with 4 routing algorithms, with the implementation provided in the Booksim. 1. Dimension Ordering Routing (DOR): The flow is routed first in x-dimension and then in the y-dimension. 2. XY-YX (XYXY) Routing [17]: The flow is routed in either dimension ordering or in reverse dimension ordering, depending on the when packet is injected to the network. 3. Randomized, Minimal Routing (ROMM) [27]: This algorithm randomly select an intermediate node lying in the minimal quadrant between the source and destination. The flow is first routed to the intermediate node in dimension ordering, then routes to its destination. 4. Minimal-Adaptive Routing (MAD) [10]: The algorithm greedily select the channel with most available buffer at each router. The path is not allowed to detour.

To simulate the performance of METRO hardware, we first implement the RTL descriptions of the routers in Chisel3. And we build the cycle-accurate behavior model of the routers based on simulation results to accelerate performance estimation. The cycle-accurate model is driven by the traffic trace of DNN workloads, which is also extracted by software frameworks. We further estimate the area and power of the METRO routers (including crossbars, registers, controlling logic) with Synopsys Design Compiler using 45nm.

Our router implementation has 5-ports with a 2-cycle pipeline. It has only one virtual channel with a single-flit
register to maintain the frequency. We do not implement arbiters as no channel conflicts will happen. We implement the distributed routing (DR) module as registers with 15 bits.

To show the generality and effectiveness of METRO on different hardware resource constraints, we study the interconnection performance on multiple wire widths, ranging from 256 to 2048 bits. To perform a fair comparison, we keep the wire width the same of METRO and traditional NoCs.

7.1.2. Workloads: To illustrate the generality and high performance. We select 8 DNN models [8,15,24,30,33,35,36,39] from real-world workloads and MLPerf [29], and build the benchmark workloads with various parallel approaches. We first fully pipeline the bert-basic [8] model mapped onto the entire tile array. Then we explore the hybrid layer parallel by building three workloads of Hybrid A-C. In these workloads, models are divided into multiple fixed-size segments, and we process each in a pipeline and parallelize the segments from different models. In the hybrid parallelizing workloads, we manually allocate tiles for different pipeline segments, as Table 2 shows.

| Workload | Model          | T/Ls  |
|----------|----------------|-------|
| Pipeline | bert-basic     | 256/73|
|          | wide_resnet50  | 64/4  |
|          | resnext50_32x4d| 64/4  |
|          | resnet50       | 64/8  |
|          | vgg16          | 64/4  |
| Hybrid-A | unet           | 64/8  |
|          | resnet50       | 64/4  |
|          | bert-large     | 64/32 |
|          | ssd_r34        | 64/4  |
| Hybrid-B | unet           | 128/19|
|          | vgg16          | 64/4  |
|          | mnasnet        | 32/4  |
|          | inception      | 32/8  |

Table 2: Benchmarking Workloads

We manually assign the tile numbers for layers, and we adopt the NVLDA-like weight stationary as the default dataflow. We employ the optimization algorithm in timeloop to tune the dataflow for leverage computing resources as much as possible. We assign the spatial locations for each layer’s tiles based on the Hilbert curve.

7.2. Evaluation Results

7.2.1. Performance Improvements: We first estimate the overall performance METRO and the four NoC baselines on the four benchmarking workloads. The evaluation is done on the 128 TOPs spatial accelerator with 256 processing tiles. The interconnection topology is an 16 × 16 mesh. We attach the 8 memory controllers to the routers at the middle of four edges of the array. To show the METRO performance improvement on various hardware resources, we vary wire width from 256 bits to 2048 bits. Fig. 10 shows the average slowdown of the communication-bounded cores, which is represented by the ratio of data transmission time to computation time, and we term it as “bounded ratio”. If the bounded ratios are greater than 1, the computation time is not large enough to overlap the communication time and the traffic bounds overall performance.

As shown in Fig. 10, METRO always achieves the smaller bounded ratio compared to all the baselines, particularly at small wire width. Specifically, METRO reduces up to 73.6% traffic time when wire width is 256 bits. It’s because when the wire width is small, a data chunk needs to be divided into more flits. Once the header is blocked, the Head-of-line (HOL) blocking will consume more buffer resources. Thus the network is more likely to suffer traffic congestion. However, METRO optimizes the scheduling not only avoids the contention but also reduces the entire traffic loads. We could also obtain that METRO achieves ideal performance with the least wire width requirements in most benchmarks. Noted that we have relatively fewer buffers than the traditional NoC routers (1 virtual channel to 8 virtual channels). That means METRO has a particularly high resource utilization compared with traditional on-chip networks.

As shown in Fig. 10 (a), in Pipeline workloads, traditional NoCs are insensitive to the change of NoC wire width. That’s because some layers in this workload are over-paralleled. In these layers, the number of flits is larger than the QoS cycles. It means that even if cores inject at the highest rate, i.e., on flit a cycle, the QoS requirements cannot still be met. This situation will maintain until the wire width promotes 4096 bits. As the flit size is large enough, flit numbers will decrease than the QoS cycle requirements. Consequently, the performance traditional NoCs promotes. However, METRO still finds its way to utilize the NoC wire width fully. Although the QoS requirements cannot meet, METRO reduces the slowdown by scheduling the flows with the earliest QoS time first. And it successfully to promotes the overall performance.

7.2.2. Improvement Breakdown: To better understand the contributions of different optimization approaches of METRO’s high performance, we demonstrate the latency reduction breakdown in Fig. 11 and evaluate it on the Hybrid-B benchmark. We modify the METRO hardware simulator to support the traffic contention handling. We set the baseline to run the workload on the single-flit register router of METRO. Directly adopting the slot-based injection controlling will result in 64% latency reduction due to removing HOL blocks. Employing dual-phase routing without heuristic search will further reduce the latency by 45% due to reducing traffic amount. Using the evolutionary algorithm to balance the traffic contributes to 34% latency reduction. And use the chunk-level flow control will reduce the control bits, reducing the latency by 3%.
Figure 10: Overall performance relative to infinite on-chip bandwidth for multiple workloads.

Figure 11: Relative latency improvements on the Hybrid-B workload with 1024 wire width.

8. Conclusion

This work focuses on the data transmission on tiled NN accelerators. We propose METRO, a hardware-software co-designed interconnection. We propose METRO, a hardware-software co-designed interconnects for inter-tile traffics in spatial DNN accelerators. METRO leverages the determinism of DNN processing, which contains two parts working in synergy. METRO software framework performs traffic scheduling, including routing and flow control. METRO architecture forwards the traffic based on configurations of METRO software framework, with relatively low power and area overheads. By decoupling the schedule policies from hardware fabrics, METRO significantly improves performance and implementation costs.

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