Reconfigurable Quadratic Converters for Electrolyzers Utilized in DC Microgrids

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ABSTRACT In this paper, three topologies of quadratic buck DC-DC converters were proposed that are capable of reconfiguring to semi-quadratic buck-boost converters, in case of an open-circuit fault in their power switch. In other words, with the aid of graph-based circuit synthesis concepts, a topology is obtained for a safe transition from one switch to another, where all other components maintain their role in contributing to optimal power conversion. Knowing that the quadratic buck converters have been proven to be an effective DC-DC circuit to supply an electrolyser as a load with specific characteristics i.e., low-voltage and high-current, the reconfigurability feature adds an extra measure of success for safer power delivery for such a load that an undesirable shut-down would negatively impact its life-cycle. The performances of three proposed synthesised topologies were compared and validated through simulation and experiments on laboratory prototypes.

INDEX TERMS DC-DC converter, DC microgrid, electrolyser, green hydrogen, reconfigurabale converter.

I. INTRODUCTION

Transition to renewable energy systems has been associated with extensive research and development activities in different areas, such as photovoltaic (PV) panels, power converters and energy storage systems to ensure that a reliable, efficient and cost-effective power delivery would be viable [1]. Many studies and technical reports have regarded hydrogen as a suitable energy storage system with a high energy density, which could be of benefit in maintaining a reliable power in a renewable energy microgrid in conjunction with batteries [2]. However, in a carbon-neutral environment, the produced and consumed hydrogen should be green, i.e., produced via renewable energy and electrolysis. The power electronics aspect of hydrogen production through electrolysis is particularly of interest when considering the power conversion stages from the source to the load. As shown in Fig. 1 (a), knowing that electrolyser is a DC load, depending on the power source, the power conversion unit is required to transform either an AC power (e.g. grid) or a DC power (e.g. PV) to a DC power, and hence either an AC-DC rectifier or a DC-DC converter would be required [3], [4].

Figs. 1 (b)-(c) illustrate a typical electrical equivalent model of an electrolyser. The capacitors are typically a contributor to the transient state and are deemed negligible in...
steady state. With that said, assuming a fixed temperature, an electrolyser stack is normally modelled as a small resistive load in steady state [5], [6]. As such, the power converter’s terminal will be connected to a low-voltage and high-current resistive load. Fig. 2 shows typical applications of power converters in a renewable energy system, where in both cases the converter is supposed to step down the voltage and supply the electrolyser. Fig. 2 (a) applies to a typical low power system, which resembles a residential rooftop solar system comprised of PV arrays, batteries and Maximum Power Point Tracking (MPPT) charge-controller. As such, considering a typical 24 V system, an electrolyser stack can be connected to this system via a DC-DC converter that typically owns a voltage gain ratio of 6 : 1 and 4 : 1 respectively for a 4 V two-layer and 6 V three-layer stacks. Fig. 2 (b) represents a high-power DC microgrid, where the scalability and reliability of a microgrid require a more sophisticated arrangement of PV arrays, batteries and loads in comparison with Fig. 2 (a). In more details, the voltage level of the busbar is rated roughly at 400 V, which allows AC load connection via inverters as well as a battery connection via bidirectional DC-DC converters. It is worth noting that a typical electrolyser of this power range is expected to have more number of stacks which conveys a higher power and/or higher voltage level (e.g. 48 V). As an instance, a DC-DC converter that liaises between the busbar and electrolyser would typically require the voltage gain ratio of 8 : 1. Therefore, considering the discussions made above in regards to Fig. 2, due to the relatively high voltage step-down and high current step-up capability required in both cases, the conventional buck converter might not be a perfect choice due to its limited gain. Hence, various solutions have been proposed in the literature to overcome this limitation. In [7], it was suggested to use an interleaved buck converter, where the high output current is distributed over different branches of the outgoing node. In [8], the authors proposed the quadratic buck converter due to its high voltage conversion capability. In [9], the direct coupling of PV and electrolyser for loss minimisation was investigated.

It has been investigated and proven that the consistency of the power supplied to the electrolyser would have an impact on its lifecycle. Therefore, a converter that can guarantee less intermittency of power across the electrolyser’s terminal, would have a better chance of getting an electrolyser operated as usual in long run [10], [11]. Thus, a topology that is capable of coping with the faults and minimising the shut-down occurrences of a power converter supplying an electrolyser is deemed beneficial for extending the lifecycle of such an equipment. In [12], [13], [14], [15], and [16], a team adopted the graph-theory concepts according to works from Maksimovic [17] and Zhou [18] and proposed a synthesis approach to derive fault-tolerant versions of the existing converter topologies. This paper attempts to investigate the quadratic buck converters [19] so that an electrolyser can be supplied with a high step-down voltage gain via a reconﬁgurable structure. While single-switch quadratic buck and buck-boost converters are the focus of this study [20], [21], [22], the approach may be applied to other quadratic topologies [23], [24], [25].

In this paper, the reconfigurable dc-dc converters are proposed that are tolerant to the faults created due to the open-circuit of switches, and can transition from one topology to another, i.e., from quadratic buck to semi-quadratic buck-boost. The main motivation behind this work was the electrolyser applications in microgrids, where i) the load has high current and low voltage levels, but the busbar has low current and medium voltage levels, and ii) the reliability is of concern as the converter failure can affect the lifecycle of equipment. Therefore, based on the literature, it has been investigated to find a topology that has these benefits. Previously, it has been proven that reconﬁgurable topologies are possible to be made from graph theory concepts. However, the concept has not been applied to quadratic topologies, before. In addition, application-wise, there has been minimum effort to address such a concern for particular applications. Therefore, via graph and circuit theories, it has been mathematically proven that two quadratic buck and buck-boost are capable of being merged so that a reconﬁgurable topology is made, which is suitable for hydrogen applications. Furthermore, a comparison has been made for pre- and post-failure modes so that the fidelity of the discussion is validated through comparison and experiments. Section II proposes three new topologies and their synthesis. Section III presents a comprehensive comparison, while section IV presents the obtained results. Finally, section V concludes the paper.

II. GRAPH-BASED SYNTHESIS APPROACH

The converter synthesis approach was originally presented in [17] and [18], then adopted to derive reconﬁgurable
FIGURE 3. Quadratic topologies presented in [19]: (a) quadratic buck type I, and (b) semi-quadratic buck-boost type I.

topologies in [12] and [14]. Originally, the synthesis approach is established by two equivalent circuits, namely AC and DC equivalents, represented as graphs. After extraction of the equivalent graphs for two different converters, one may investigate the possibility of introducing a reconfigurable topology by merging two (or more) graphs, albeit via the following steps and considerations imposed by the graph theory concepts.

A. PROPOSED TOPOLOGY I

The quadratic converters that were originally presented in [19], are the starting point. In simple terms, as shown in Fig. 3, having two back-to-back cells with the gain of $D$, of which the second is the conventional buck converter, a quadratic buck converter is made with the gain of $D^2$ as shown in Fig. 3 (a). The same steps, i.e., cascading the first cell with the conventional buck-boost converter will lead to semi-quadratic buck-boost converter with the gain of $-D^2/(1 - D)$ as shown in Fig. 3 (b).

1) STEP 1: AC AND DC EQUIVALENTS

In the first step, we intend to obtain the DC and AC equivalent graphs. In summary, the DC and AC graphs are obtained as follows.

- For DC graphs: The capacitors are removed while the inductors are shorted. The sources and loads are considered as external one-port elements and can be removed in DC mode.
- For AC graphs: The voltage sources and capacitors are shorted while the current sources and inductors are removed.

Accordingly, Fig. 4 shows the equivalent circuits, where the quadratic buck type I - with the modified position of switch - along with its DC and AC equivalents are presented in Figs. 4 (a), (b) and (c), respectively; and the semi-quadratic buck-boost type I -with the modified position of switch - along with its DC and AC equivalents are presented in Figs. 4 (d), (e) and (f), respectively.

2) STEP 2: SUPERPOSITION RULE

In the second step, we start to investigate the possibility of merging these two converters to establish a reconfigurable fault-tolerant topology. By superimposing the DC graphs in Fig. 4 (b) and Fig. 4 (e), a new DC graph is built up, as per Fig. 4 (g). It is worth noting that diodes are located identically in both DC graphs, while the switches are connected to different nodes which implies the new DC graph will contain two switches and three diodes. Similarly, superimposing the AC graphs leads to a new AC graph shown in Fig. 4 (h). Noteworthy, despite connecting to the same nodes, $S_1$ and $S_T$ both should appear in the AC graph as they have previously appeared in DC graph.

3) STEP 3: INCIDENCE MATRICES

In the third step, we build the incidence matrices for the resultant DC and AC graphs, i.e. $A_d$ and $A_a$ which are presented in (1) and (2). According to the graph theory, the $m_{th} \times n_{th}$
(row m, column n) array is noted as 1, -1, and 0 respectively when the current is outgoing, incoming and not flowing.

\[
A_d = \begin{pmatrix}
0 & -1 & -1 & 1 & 0 & 1 \\
1 & 0 & 0 & -1 & 0 & -1 \\
1' & 0 & 0 & 1 & -1 & 0 \\
2 & 1 & 0 & 0 & 0 & 1
\end{pmatrix}
\]  

(1)

\[
A_a = \begin{pmatrix}
a & -1 & -1 & -1 & 1 & 0 \\
b & 1 & 1 & 0 & 0 & 1 \\
c & 0 & 0 & 1 & -1 & -1
\end{pmatrix}
\]  

(2)

4) STEP 4: MODIFIED INCIDENCE MATRIX \( (A_d') \)

As the penultimate step before introducing the reconfigurable topology, we need to shape the modified incidence matrix to accommodate the missing inductors and/or capacitors. To obtain this, we need to add the missing nodes to the matrix \( A_d \). To understand why some nodes might have been missed, we need to recall the definition of DC graph. Fig. 5 (a) corresponds to \( A_d \), where four nodes are present. We know that in DC graph, capacitors and sources are removed so we can presumably locate \( V_{in} \) and \( V_{out} \) by a simple inspection. Then, noting that the capacitors and sources were shorted in AC graphs, we can imagine an analogy between \( A_d \) and \( A_a \). In other words, we can conclude that nodes 0 and 1 are grouped into node \( a \). By comparing the corresponding rows of nodes 0 and 1 in \( A_d \) with the corresponding row of node \( a \) in \( A_a \), one can claim that row 0 of \( A_d \) is actually the result of aggregation of row 0 and part of row 1 in \( A_d \). This will get us to the corresponding rows of nodes 0 and 0' in \( A_d' \). The same steps are valid when assuming that nodes 2 and 1 in \( A_d \) are grouped into node \( c \) in \( A_a \), which yields 2 and 2' of \( A_d' \). This is also true for nodes 1, 1' and \( e \) in \( A_d \) and \( A_a \). Consequently, \( A_d' \) is expressed as (3), which represents Fig. 5 (b).

\[
A_d' = \begin{pmatrix}
0 & -1 & -1 & 1 & 0 & 1 \\
0' & 0 & 0 & -1 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & -1 \\
1' & 0 & 0 & 1 & -1 & 0 \\
2' & 0 & 1 & 0 & 0 & 0 \\
2 & 1 & 0 & 0 & 0 & 1
\end{pmatrix}
\]  

(3)

B. PROPOSED TOPOLOGIES II AND III

There are other possible topologies that could be synthesised with the same number of components, same voltage gain ratio and same reconfigurability, albeit with different combination. Considering the quadratic buck topology type I presented in Fig. 6 (a), with an intention to merge with semi-quadratic Zeta converter as shown in Fig. 6 (c), one might follow the five mentioned steps and build the graphs and matrices and obtain a reconfigurable topology. However, for the sake of simplicity of calculation, as it has been proven above, the common cell including \( S_2, S_2', L_1, C_1 \) in Fig. 6 (a) and Fig. 6 (c) can be excluded for investigation of reconfigurability. In other words, merging a buck converter with a Zeta converter will lead to a reconfigurable buck and buck-boost topology as presented in [12], which could then be transformed into a quadratic buck and semi-quadratic buck-boost topology by inserting the buck cell, known as topology II, as illustrated in Fig. 6 (d). If one considers the quadratic buck topology II, as presented in Fig. 6 (b), and intends to merge it with the semi-quadratic Zeta converter, the same synthesis steps that were presented for topology I should be followed, which by inspection, leads to the topology III as depicted in Fig. 6 (e). With a closer look at this topology, one could confirm that this aligns with topology II derivation concepts. In other words, the auxiliary switch \((S_c)\) connects to the same node that the main switch \((S_1)\) is connected to in both topologies, i.e. right before the buck cell in topology II and right after the buck cell in topology III. Fig. 7 shows the summary of the proposed converters of which (a), (b) and (c) respectively represent topologies I, II and III.

III. CIRCUIT ANALYSIS AND COMPARISON

Each circuit has got two operating modes, depending on the switch that is in operation. When the switch \( Q_1 \) is in operation, the circuit, namely the \( Q_1 \)-based configuration, operates a quadratic buck converter. Accordingly, when \( Q_1 \) is out of order due to an open-circuit fault, the circuit is reconfigured by putting \( Q_2 \) into operation, namely the \( Q_2 \)-based configuration, operates as a semi-quadratic buck-boost converter.

A. STEADY-STATE ANALYSIS

Each of these six configurations- i.e., three quadratic buck \((Q_1\)-based) and three quadratic buck-boost \((Q_2\)-based) configurations- have partially been previously analysed in the literature as a separate circuit. Therefore, for the sake of simplicity and to avoid excessive repetition of steady-state circuit analysis, Fig. 8 in conjunction with Table 1 summarised the equivalent circuit of each configuration as well as the steady-state equations. The steady-state parameters of this table are obtained according to the volt-second balance and charge-second balance over a duty cycle, on the voltage waveform.
FIGURE 6. Derivation of topologies II-III: (a) quadratic buck type I, (b) quadratic buck type II, (c) semi-quadratic zeta, and (d)-(e) proposed topologies II-III.

FIGURE 7. Proposed reconfigurable quadratic buck / semi-quadratic buck-boost converters: (a) Topology I, (b) Topology II and (c) Topology III.

The same goes for the voltage across capacitors, respectively. As an instance, for topology II, applying KVL to the first loops of Fig. 9 (a) and Fig. 9 (b), one can express the voltage across the inductor $L_1$ indicated as (4) and (5), respectively for the case that the switch $Q_1$ is on and off, similarly, applying KVL to the second loops of Fig. 9 (a) and Fig. 9 (b), yields (6) and (7) for the voltage across the inductor $L_2$. Considering the volt-second balance, i.e. assuming that the average voltage across inductors over a duty cycle of the switch $Q_1$ is zero, one can substitute (4) and (5), and (6) and (7) into (8), and obtain the voltage across capacitors $C_1$ and $C_2$, expressed as (9), in line with the information provided in Table 1.

\[
\begin{align*}
V_{L1 \text{ (on)}} &= V_{in} - V_{C1} \quad (4) \\
V_{L1 \text{ (off)}} &= -V_{C1} \quad (5) \\
V_{L2 \text{ (on)}} &= V_{C1} - V_{C2} \quad (6) \\
V_{L2 \text{ (off)}} &= -V_{C2} \quad (7) \\
\overline{V_L} &= D V_{L \text{ (on)}} + (1 - D) V_{L \text{ (off)}} = 0 \quad (8) \\
\begin{cases} V_{C1} = D V_{in} \\ V_{C2} = V_{out} = D^2 V_{in} \end{cases} \quad (9)
\end{align*}
\]

The same goes for the current through capacitors $C_1$ and $C_2$ which are expressed as (10) and (11), when KCL applies to the first nodes of Figs. 9 (a)-(b). Similarly, (12) and (13) are the results of KCL on the second nodes of Figs. 9 (a)-(b). Considering the charge-second balance, i.e. assuming that the average current through capacitors over a duty cycle of the switch $Q_1$ is zero, one can substitute (10) and (11), and (12) and (13) into (14), and obtain the voltage through inductors $L_1$ and $L_2$, expressed as (15), in line with the information provided in Table 1.

\[
\begin{align*}
I_{C1 \text{ (on)}} &= I_{L1} - I_{L2} \quad (10) \\
I_{C1 \text{ (off)}} &= I_{L1} \quad (11) \\
I_{C2 \text{ (on)}} &= I_{out} - I_{L2} \quad (12) \\
I_{C2 \text{ (off)}} &= I_{out} - I_{L2} \quad (13) \\
i_C &= DI_{C \text{ (on)}} + (1 - D)I_{C \text{ (off)}} = 0 \quad (14) \\
\begin{cases} I_{L1} = DI_{out} \\ I_{L2} = I_{out} \end{cases} \quad (15)
\end{align*}
\]

The same discussion is valid for the $Q_2$-based topology, i.e. when the volt-second and charge-second balance are applied to the loops and nodes of Fig. 9 (c) and Fig. 9 (d).
As indicated before, all three topologies are using the same number of components, i.e. two capacitors, three diodes, and two switches (one active and one reserved switch). This is also evident in Fig. 8, where Figs. 8 (a), (c) and (e) are quadratic buck converters \((M = D^2)\) and Figs. 8 (b), (d) and (f) are semi-quadratic buck-boost converter \((M = D^2/(1−D))\). According to Table 1, the voltage gain ratio is the same for all \(Q_1\)-based topologies, and \(Q_2\)-based topologies. However, the other parameters might slightly differ, depending on the topology. Since the duty cycle varies in each reconfiguration, a closer look is worth having at the variations of voltage and current stress values for the switches and diodes versus variations of voltage gain. Figs. 10 (a)-(b), show these variations for the \(Q_1\) and \(Q_2\) voltage and current stress, while Figs. 10 (c)-(d) represent the voltage stress of \(D_1\) and \(D_1\) or \(D_2\) versus voltage gain differences. The rest can be derived from Table 1. It is evident that this transition, is paid at the cost of increased stress, to avoid the shut-down, whereas the quadratic buck converter is designed for, i.e. higher step-down capability. Though there have been other quadratic buck converters in the literature which this paper is actually derived from, a fair comparison would be a comparison based on the reconfigurable converters. Therefore, Table 1 along with Fig. 10 could potentially be used as a guideline for the selection of components as well as choosing the right circuit based on a particular application.

**B. TRANSIENT ANALYSIS**

State-space averaging method, particularly small-signal modelling is used to achieve the control-to-output transfer function so that the transient behaviour of the system is analysed in more details. According to the literature, there are four steps to follow, which have been thoroughly explained by the author in [22] and [26], and are summarised as follows.

- **Step i:** State-space equations for each operating state, when the switch is on and off.

- **Step ii:** Time-weighting and averaging the state-space equations according to their time intervals \(DT_1\) and \((1−D)T_s\).

- **Step iii:** Applying a small ac perturbation the vicinity of steady-state operating points.

- **Step iv:** Applying the Laplace transform and obtaining the transfer function

Following the steps above, the state-space equations are expressed as (16), where \(X = [i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}]^T\) is the state vector, and \(U = [v_{in}, d]^T\) is the control vector. \([A], [B], [C]\) and \([D]\) are the averaged state-space equations, respectively defined as \(A = dA_{on} + (1−d)A_{off}\), \(B = dB_{on} + (1−d)B_{off}\), and \(C = dC_{on} + (1−d)C_{off}\), and \([D]\) is zero.

\[
\begin{align*}
\dot{X} &= AX + BU \\
y &= CX + DU
\end{align*}
\]  

(16)

For the quadratic buck (\(Q_1\)-based) and the semi-quadratic buck-boost (\(Q_2\)-based) circuits in topology II and their operating states as presented in Fig. 9. After applying a small perturbation, using the Laplace transform, the control-to-output transfer function is expressed as (16).

\[
G(s) = \frac{\hat{V}_{out}}{d} = C(sI − A)^{-1}B(\cdot, 2)
\]

\[
= \frac{s^2 + a_1s + a_0}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0}
\]

(17)

The coefficients \(a_1, a_0, b_4, b_3, b_2, b_1, \) and \(b_0\) for topology II with the parameters presented in section IV are as follows, respectively for \(Q_1\)-based and \(Q_2\)-based circuits.
TABLE 1. Comparison for topologies I, II and III in quadratic buck (Q₁-based) and semi-quadratic buck-boost (Q₂-based) modes.

| Topology   | Topology I | Topology II | Topology III |
|------------|------------|-------------|--------------|
|            | Q₁-based   | Q₂-based    | Q₁-based     | Q₂-based    |
| V_{in}/V_{ln} | D²         | D²/(1 - D)  | D²           | D²/(1 - D)  |
| V_{D1}/V_{ln} | D         | D           | D            | D           |
| I_{D2}/I_{out} | 1         | 1/(1 - D)   | 1            | 1/(1 - D)   |
| I_{D1}/I_{out} | D         | D/(1 - D)   | D            | D/(1 - D)   |
| V_{Q2}/V_{ln} | 1/(1 - D) | 1/(1 - D)   | 1            | 1/(1 - D)   |
| I_{Q2}/I_{out} | -         | -           | -            | -           |
| V_{Q1}/V_{ln} | 1 + D      | 1 + D       | 1 + D        | -           |
| I_{Q1}/I_{out} | 1         | 1           | 1            | 1           |
| V_{D3}/V_{ln} | D         | D/(1 - D)   | D            | D/(1 - D)   |
| I_{D3}/I_{out} | 1         | 1/(1 - D)   | 1            | 1/(1 - D)   |
| V_{D2}/V_{ln} | 1         | 1           | 1            | 1           |
| I_{D2}/I_{out} | 1         | 1           | 1            | 1           |
| V_{D1}/V_{ln} | 1         | 1           | 1            | 1           |
| I_{D1}/I_{out} | 1 - D      | 1 - D       | 1            | D           |

Further discussions in regards to the transfer function derivation is presented in Appendix.

Accordingly, the Bode diagrams associated with each of the transfer functions for (Q₁-based) and (Q₂-based) topologies are shown in Fig. 11. This is the key to design an appropriate controller for the closed-loop experiments. In this case, the optimum closed-loop proportional-integral (PI) controller parameters were obtained from Sisotool in MATLAB and the results will be presented in section IV.

C. EFFICIENCY ANALYSIS

The input power goes through several power conversion stages, which are associated with power losses, typically dissipated as heat. In a power converter, one can consider four main types of losses classified as follows.

- The inductor loss \( P_L \), which is made up of two terms namely conduction loss \( P_{w} \) caused by winding resistance and the core loss \( P_{core} \) caused by hysteresis and eddy current in the magnetic core.

- The capacitor loss \( P_C \), which is generically negligible and made by the parasitic resistor.

- The switch loss \( P_S \), which is made up of two terms, namely conduction loss \( P_{SC} \) caused by the switch resistance in on mode, and switching and the switching losses \( P_{sf} \) that occurs over the rise-time and fall-time.

- The diode loss \( P_D \), which is due to the forward voltage drop of the diode, during the conduction mode.

As per the explanation above, the efficiency formula can be expressed as (18), where \( \eta \), \( P_{out} \) and \( P_{in} \) denote the efficiency, output power and input power, respectively.

\[
\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_L + P_C + P_S + P_D}
\]  

The efficiency equation along with the datasheet information shall be used to obtain the analytical efficiency of a power converter. This has been applied to the proposed converter and
signals are generated via two separate digital signal processor (PCBs) in Fig. 13. Furthermore, the switching frequency was tors are located at the bottom layers of printed circuit boards used for switches Figs. 13 (a)-(c), there is only one gate-driver UCC21320 set at 64 kHz, provided by TI’s F28069M. As inferred from:

| Power Switches \( Q_1, Q_2 \): Rohm RGTH007K65GC11 | Diodes \( D_1, D_2, D_3 \): IXYS DPF30I300PA |
|---|---|
| Inductors \( L_1, L_2 \): 1 mH on Fair-Rite 5978018601 | Capacitors \( C_1, C_2 \): 100 µF 470 µF Vishay 136RVI |
| Load: 0.5 Ω (paralleled RS100 1R) |

It is worth noting that some components including capacitors are located at the bottom layers of printed circuit boards (PCBs) in Fig. 13. Furthermore, the switching frequency was set at 64 kHz, provided by TI’s F28069M. As inferred from Figs. 13 (a)-(c), there is only one gate-driver UCC21320 used for switches \( Q_1 \) and \( Q_2 \), in a sense that the gate-source signals are generated via two separate digital signal processor (DSP) pins, connected to the gate-driver, and generating the gate-source voltages \( V_{GS1} \) and \( V_{GS2} \). The scenario is formed in a way that if \( Q_1 \) stops working for any reason, the circuit is reconfigured through \( Q_2 \), i.e., \( V_{GS1} \) is initially generated so that the circuit operates as a quadratic buck converter; As soon as \( Q_1 \) is disconnected due to an open-circuit fault, \( V_{GS2} \) is generated, albeit at a different duty cycle ratio to meet the voltage gain requirements of reconfigured topology that is changed from \( D^2 \) to \( D^2/(1 - D) \). Therefore, there is no (or minimum) impact on the output voltage of the converter supplying the external load. It is also worth noting that the load has intentionally been selected to be a relatively low voltage and high current, as per the justifications made in introduction to mimic a three-layer electrolyser stack. In particular, one might find an equivalent lab electrolyser membrane stack of similar specifications. As an instance, a 3-layer stack electrolyser of model Titan EZ-180 is a 0.6 Ω (10A, 6 V) load in steady-state, which resembles the same external load used for experiments.

Fig. 14 shows the captured waveforms from the experiments. Fig. 14 (a)-Fig. 14 (c) illustrate the case for topology I. The circuit was initially operating with \( Q_1 \). As a result, one would expect the circuit to operate as a quadratic buck converter (Topology I), as per Table 1 and Fig. 7. Therefore, prior to the incident, having a duty cycle of 50%, with the input voltage of 24V, output voltage should roughly be equal to 6V, which is evident in this figure. In addition, according to Table 1, the voltage stress on diodes \( D_1, D_2 \) and \( D_3 \) and the current through \( L_1 \) and \( L_2 \) are respectively equivalent to 24V, 24V and 12V, and 6A and 12A. When the incident occurs, i.e., \( Q_1 \) is opened and \( Q_2 \) comes to effect, the converter transitions from quadratic buck to semi-quadratic buck-boost topology. That being said, the duty cycle clearly needs to be adjusted to 39% so that the output voltage is maintained at the original value. In addition, the voltage stress on diodes, as well as the current through inductor, all follow the expectations (Table 1) and are 24V, 24 V, 16 V and 8 A, 20 A, respectively for \( D_1, D_2, D_3, \) and \( L_1 \) and \( L_2 \). Figs. 14 (d)-(e) and Figs. 14(f)-(h) show the same scenario for topologies II and III, respectively. Both circuits are experiencing a transition from quadratic buck to quadratic buck-boost when \( Q_1 \) is disconnected and \( Q_2 \) is activated. In both cases, the duty cycles are adjusted accordingly so that the output voltage is maintained at the original value. In addition, the values for diode voltage and

**FIGURE 13.** Experiments on the prototypes: (a) topology I, (b) topology II, (c) topology III, and (d) setup.
inductor current have confirmed the analysis and equations of Table 1. In details, for topology II, $V_{D1}$, $V_{D2}$, $V_{D3}$ and $I_{L1}$ and $I_{L2}$ before and after incident are recorded as 24 V, 24 V and 12 V, and 6 A and 12 A and 24 V, 24 V, 16 V and 8 A and 20 A respectively. For topology III, $V_{D1}$, $V_{D2}$, $V_{D3}$ and $I_{L1}$ and $I_{L2}$ before and after incident are recorded as 24 V, 24 V and 12 V, and 6 A and 12 A and 24 V, 24 V, 16 V and 12 A and 20 A respectively.

The converter has also been tested in closed-loop with a PI controller designed as per the discussions in section III. A step-change in the load or the input voltage, leads to a stable transient behavior in the output voltage. This was not far from the expectation as the duty cycle would easily be adjusted in case of perturbations. This is evident from Figs. 15 (a)-(b) when the load changes from 1 $\Omega$ to 0.5 $\Omega$ or Figs. 15 (c)-(d), when the input voltage changes from 24 V to 18 V, but the output is almost stable at 6 V. Please note the high(er) noise in Figs. 15 (c)-(d), in comparison with Figs. 15 (a)-(b) is due to the different time division. This would also convey that in case of an appropriate controller design, the reconfiguration transition either in the load or the source side, would minimise the impact on the load or input busbar in Fig. 2.

Eventually, the efficiency discussion in section III is applied to the converter and the efficiency has been calculated versus load variations as presented in Fig. 16 (a). The efficiency variations follow the expected paradigm, i.e. the higher the power rating is, the higher the efficiency drop will be as the current across the components increases. In addition, for this particular converter, it would be of interest to find out the efficiency changes in case there is a switch failure and the converter is reconfigured. Fig. 16 (b) presents this
FIGURE 16. topology II efficiency variations vs (a) load, and (b) gain changes.

perception, with a similar fashion followed in Fig. 10. As an instance, when the output voltage is set at 6 V, with the input voltage level of 24 V, the efficiency undergoes a slight change, as noted in Fig. 16 (b), from 92% to 88%.

V. CONCLUSION

According to the graph theory for electrical circuits, three quadratic buck topologies were synthesised with three semi-quadratic buck-boost topologies in a way that three new reconfigurable topologies were proposed. The resultant topologies are capable of coping with the open-circuit fault of switches so that as soon as one switch fails, the circuit is reconfigured to another topology via the other switch; as such, all other circuit components are utilised in the power conversion process via different paths. The quadratic buck topologies are a good choice for electrolyser applications, where a high step-down voltage conversion ratio is required. In addition, the reconfigurability of such circuits would meet the requirements of electrolyser’s lifecycle, where a power outage would have a negative impact. The proposed circuits were analysed, simulated and prototyped to validate the feasibility of the investigated approach. For future work, one can explore the possibility of applying the same approach to the isolated topologies, where the input-output isolation is a requirement and/or another degrees of freedom for changing the voltage gain ratio, namely the transformer, is available.

APPENDIX

SMALL-SIGNAL MODELLING

The following shows the steps for derivation of the control-to-output transfer function that was presented in section III.

**Step i:** For topology II, the equivalent circuits are shown in Fig. 9. For $Q_1$-based topology, respectively when the switch is on and off, KVLs and KCLs lead to (19) and (20).

\[
\begin{align*}
L_1di_{L1}/dt &= V_{in} - V_{C1} \\
L_2di_{L2}/dt &= V_{C1} - V_{C2} \\
C_1dv_{C1}/dt &= I_{L1} - I_{L2} \\
C_2dv_{C2}/dt &= I_{L2} - V_{C2}/R
\end{align*}
\]

\[
\begin{align*}
L_1di_{L1}/dt &= -V_{C1} \\
L_2di_{L2}/dt &= -V_{C2} \\
C_1dv_{C1}/dt &= I_{L1} \\
C_2dv_{C2}/dt &= I_{L2} - V_{C2}/R
\end{align*}
\]  

**Step ii:** Averaging the state-space equations, according to the Volt-second and charge-second balance, i.e. to weigh-average with $D$ and $(1 - D)$ leads to the matrices presented in Table 2. Please note the output matrix $C$ is defined as $[C]=\{0 \quad 0 \quad 0 \quad 1\}$ and the matrix $[D]=\{0 \quad 0\}$.

**Step iii:** Applying a small perturbation to the inputs replaces them with $v_{in} = V_{in} + \hat{v}_{in}$ and $d = D + \hat{d}$, where “$\wedge$” represents the small-signal perturbation. Neglecting the second-order terms will lead to the updated matrix $B$ as presented in table 3.

**Step iv:** One can use the Laplace transform to obtain the transfer functions. Thanks to MATLAB, ss2tf($A$, $B$, $C$, $D$, $n$) can be used to obtain the transfer function via the state-space equations presented above, where $n = 1$ derives the $V_{out}/V_{in}$

**TABLE 2. Step ii: Averaged State-Space.**

| $Q$ | $A$ | $B$ |
|-----|-----|-----|
| 1   | \[
\begin{bmatrix}
0 & 0 & -\frac{1}{L_1} & 0 \\
0 & 0 & -\frac{1}{L_2} & -\frac{1}{RC_2} \\
0 & \frac{1}{C_1} & 0 & -\frac{1}{RC_2} \\
\end{bmatrix}
\] |
| 2   | \[
\begin{bmatrix}
0 & 0 & -\frac{1}{L_1} & 0 \\
0 & 0 & \frac{1}{L_2} & -\frac{(1-D)}{RC_2} \\
0 & \frac{1}{C_1} & 0 & \frac{(1-D)}{RC_2} \\
\end{bmatrix}
\] |

**TABLE 3. Step iii: $[B]$ after applying a perturbation.**

| $Q$ | $[B]$ |
|-----|-----|
| 1   | \[
\begin{bmatrix}
0 & \frac{v_{in}}{L_1} \\
0 & \frac{v_{in}}{L_2} \\
0 & \frac{V_{in}}{(1-D)L_2} \\
0 & \frac{V_{out}}{(1-D)RC_2} \\
0 & 0
\end{bmatrix}
\] |

The same goes for (21) and (22) for $Q_2$-based topology.

\[
\begin{align*}
L_1di_{L1}/dt &= V_{in} - V_{C1} \\
L_2di_{L2}/dt &= V_{C1} \\
C_1dv_{C1}/dt &= I_{L1} - I_{L2} \\
C_2dv_{C2}/dt &= I_{L2} - V_{C2}/R
\end{align*}
\]

\[
\begin{align*}
L_1di_{L1}/dt &= -V_{C1} \\
L_2di_{L2}/dt &= -V_{C2} \\
C_1dv_{C1}/dt &= I_{L1} \\
C_2dv_{C2}/dt &= I_{L2} - V_{C2}/R
\end{align*}
\]
and $n = 2$ derives $V_{out}/d$. The Bode diagrams for the numerical and the parametric transfer functions of $Q_1$-based topology were derived as (17), (23), and plotted in Fig. 17.

\[
\begin{align*}
& a_1 = -D^2/RC_1 \\
& a_0 = 2/L_1 C_1 \\
& b_4 = 1 \\
& b_3 = 1/RC_2 \\
& b_2 = (L_1 C_1 + L_2 C_2 + D^2 L_1 C_2)/L_1 L_2 C_1 C_2 \\
& b_1 = (L_2 + D^2 L_1)/R L_1 L_2 C_1 C_2 \\
& b_0 = 1/L_1 L_2 C_1 C_2
\end{align*}
\]  

(23)

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