Nomenclature

- $V_{DC}$: input DC voltage
- $V_{ref}$: reference voltage
- $T_s$: sampling time
- $N$: total number of samples
- $N_{max}$: maximum number of samples
- $T_1, T_2$: dwell time for active voltage vectors
- $T_z$: dwell time for zero voltage vector
- PWM: pulse width modulation

1 Introduction

Three-level inverters have several advantages over two-level inverters. The output voltage and current waveforms of three-level inverters contain low harmonics compared to a conventional two-level inverter for the same switching frequency. The blocking voltage of each semiconductor switch is reduced in a three-level configuration. Therefore, the switches in three-level can handle more DC bus voltage than two-level inverter with the same voltage ratings. These features enable three-level inverters for medium voltage drive applications. There are three inverter configurations, namely Neutral Point Clamped (NPC), Flying Capacitor and Cascaded H-Bridge multilevel configuration. Three-level NPC VSI configuration is widely used because of its simplicity and easy pulse width modulation (PWM) implementation.

Various modulation methods for PWM are developed for the multilevel inverters [1–6]. The space vector PWM (SVPWM) is the most popular method for two-level and multilevel inverters because of its flexibility in implementing both in hardware and software. SVPWM provides relatively better performance compared to the triangle comparison approach even with a lower modulation index. The commonly used approaches involve the use of conventional SVPWM. It does not involve lookup table and uses a voltage comparison approach for the generation of PWM.

The current harmonic distortion and switching loss are the main performance parameters of a PWM inverter. The current distortion is strongly influenced by the switching sequence used in SVPWM technique. Different SVPWM schemes for three-level inverter based on the equivalent two-level inverter are discussed in [7] to reduce total harmonic distortion (THD). The switching losses are reduced in three-level inverters by keeping the pulse number (ratio of switching frequency to fundamental frequency) to a low value. The output voltage is synchronised with the fundamental component to eliminate subharmonics. The pulse number is chosen as an odd number to achieve synchronisation and symmetry.

The research works that are available in [8–10] discuss the systematic approach of SVPWM implementation for three-level inverters. The past decade has seen increasing research on the topology of three-level inverter and three-level PWM algorithms. A generalised control algorithm for the multilevel inverter is discussed in [8]. The performance of the three-level VSI is influenced by the switching algorithms [9–21]. The three-level space vector algorithm for high power applications ensuring synchronised PWM with quarter-wave symmetry and half-wave symmetry is discussed in [8–13]. The majority of work reported in literature involves specific issues like simplification of the algorithm [14], neutral point voltage balancing [15] and SVPWM for reducing harmonics [16]. A simple method of dwell time computation using g-h coordinate system is reported in [17]. However, the rounding off error due to abc-gh coordinate and gh coordinate-abc conversion results in the identification of the incorrect triangle and all the redundant switching states cannot be realised using this method. The reduced common-mode voltage [18], virtual SVPWM and current ripple reduction are discussed in [19, 20]. Discontinuous PWM and Hybrid PWM methods developed are discussed in [21–23]. Previously reported works to realise all switching states in advanced processors like DSPs, Field programmable gate array (FPGA). The main objective of using a high-end processor is to reduce the execution time which increases hardware implementation cost.
Deng et al. [17] implement a novel approach to identify the triangle where the reference vector lies and computes three nearest voltage vectors which are the end points of the identified triangle. However, it is based on sampling phase voltages ($V_a$, $V_b$, and $V_c$) which require high-performance multichannel analogue-to-digital converter (ADC) hardware. High-performance ADC is required to reduce ADC sampling error which improves the accuracy of triangle identification algorithm. Controlling multi-channel ADC hardware needs a high-performance FPGA board. Existing approaches use digital-to-analog converter (DAC) and drive circuitry to generate the gate pulses. Deng et al. [17] is the best available implementation for multilevel SVPWM inverter configuration. However, this method requires high-performance multichannel ADC, DAC and FPGA board which increases implementation cost and complexity.

The main objective of this paper is to address hardware complexity reduction by eliminating the need to sample phase voltages and removing the requirement of high-performance multichannel ADC/DAC and the corresponding FPGA-based ADC controller hardware with zero increase in software computing overhead. The exact placement of samples in three-level inverter configuration to detect single switching violation, bus-clamping support, optimised computation and voltage imbalance issues and double switching SVPWM sequences for three-level inverters resulting in synchronised PWM output waveforms with half-wave symmetry and three-phase symmetry are additional objectives of the proposal. This work targets to perform the critical task of dwell time computation for three levels based on sine and cosine functions with a low-cost eight bit PIC microcontroller (PIC18F452). The limitation of the eight bit microcontroller is overcome by compiler optimised SVPWM architecture. Compared with other simplified algorithms [14–23], the proposed method does not require any complex optimisation technique and feedback signals. A detailed mathematical analysis is presented for dwell time computation for three-level VSI. The sector I is divided into six regions. The active and zero vectors for Triangles 1–4 for the sector I is given in Table 1.

2. Development of the proposed framework for three-level VSI

2.1 Background

The space vector diagram for three-level VSI can be considered as six overlapped hexagons as shown in Fig. 1. Each small hexagon presents a space vector diagram of a conventional two-level VSI. There are 27 switching states in a three-phase three-level VSI. Out of 27 switching states, there are 24 active vectors and 3 zero vectors. The vectors with a relative length of 0.5 are termed as zero vectors of each small hexagon which are generated from the switching states PPP, NNN and OOO. Generally, the switching sequence in SVPWM method begins from a zero vector and ends with the same zero vector. Hence the zero vector is applied twice in a subcycle. The active vectors of the equivalent two-level inverter are located on the edges of the triangles. There are six sectors of 60° each in three-level SVPWM similar to the two-level SVPWM. Fig. 2 shows the circuit diagram of a three-level NPC VSI and the corresponding space vector diagram is shown in Fig. 1 [4]. The dwell time equations are calculated for the first sector only as all the sectors are symmetrical to each other. The sector I is divided into six regions. The active and zero vectors for Triangles 1–4 for the sector I is given in Table 1.

2.2 Motivation

The motivation of the proposal is:

i. to provide an efficient SVPWM implementation with reduced hardware requirement (microcontroller ADC hardware replaces multichannel ADC and associated FPGA board) without increasing software complexity;

ii. to reduce THD and to provide neutral point voltage balancing for NPC three-level configuration;

iii. to provide the capability to place the sample in a three-level inverter configuration to verify single switching violation while crossing sector and subsector boundaries.

2.3 Dwell time computation

The mathematical expressions of optimised dwell time for three-level VSI are developed in this section. The identification of the regions are considered for the modulation index ($m_i$)>0.5. Fig. 3...
shows the flowchart of the region identification algorithm for the three-level SVPWM. $V_{\text{ref}}$ indicates the voltage magnitude corresponding to the reference vector. The boundary identification is done by limiting the reference vector trajectory between Triangle 1 and Triangle 2 and represented by $V_B(\alpha)$. From Fig. 4, $V_B(\alpha)$ indicates the boundary regions corresponding to Triangles 1 and 2. Geometrically, the magnitude of $V_B(\alpha)$ can be expressed as

$$V_B(\alpha) \cos(\alpha) = V_B(\alpha) \sin(\alpha) = 0.5 \tag{1}$$

Multiplying $\sqrt{3}/2$ on both sides

$$V_B(\alpha) = \frac{\sqrt{3}}{4 \sin(\beta - \alpha)}; \quad 0 < \alpha < 30^\circ \tag{2}$$

The region lies in Triangle 1 if the reference exceeds this length.

$$V_{\text{ref}} > V_B(\alpha) \tag{4}$$
To calculate the dwell time of the reference vector, the region in which the reference vector tip falls has to be identified. The inverse of the tangent function takes more time than the normal trigonometric functions. To reduce the execution time by the microcontroller, new dwell times (\(T_1\) and \(T_2\)) are assigned to the negative value of the angle \(\alpha\) for Triangles 3 and 4 as shown in Fig. 2. The exact region is determined by comparing \(V_1\) and \(V_2\). The angle \(\alpha\) assigned to the negative value of the angle \(\alpha\) for Triangle pairs 3, 4.

The dwell time equations for Triangle pairs 1, 2 are given by

\[
T_1 = \frac{V_\beta \sin(60 - \beta)}{\sin 60} \quad (9)
\]

\[
T_2 = \frac{V_\beta \sin \beta}{\sin 60} \quad (10)
\]

where \(V_\beta\) and angle \(\beta\) are the local reference vector and angle with respect to the vector \(V_1\).

This requires evaluation of \(V_\beta\) and angle \(\beta\) which includes inverse of the tangent function. Determining the angle \(\beta\) with the inverse of the tangent function takes more time than the normal trigonometric functions. To reduce the execution time by the microcontroller, new dwell times (\(T_1\) and \(T_2\)) equations for Triangle 1 and Triangle 2 are derived based on geometry and given as below Triangle 1:

\[
\frac{V_{\text{ref}} \cos(\alpha)}{\sin(\alpha)} = 0.5 \left[ \frac{\cos(0)}{\sin(0)} + V_\beta \frac{\cos(\beta)}{\sin(\beta)} \right]
\]

From this

\[
V_{\text{ref}} > \frac{\sqrt{3}}{4 \sin(60 - \alpha)}: \quad 0 < \alpha < 30^\circ \quad (5)
\]

\[
V_{\text{ref}} \sin(60 - \alpha) > \frac{\sqrt{3}}{4}: \quad 0 < \alpha < 30^\circ \quad (6)
\]

Fig. 4 Diagram for boundary identification

\[
V_{\text{ref}} > \frac{\sqrt{3}}{4 \sin(60 - \alpha)}: \quad 0 < \alpha < 30^\circ \quad (5)
\]

\[
V_{\text{ref}} \sin(60 - \alpha) > \frac{\sqrt{3}}{4}: \quad 0 < \alpha < 30^\circ \quad (6)
\]

Substituting (9) and (11) in (3) and (4), respectively, we get

\[
T_1 = \frac{2}{V_{\text{DC}}} (V_{\text{ref}} \times \cos \alpha) - 1 - \frac{1}{V_{\text{DC}} \sin 60} (V_{\text{ref}} \times \sin \alpha) \quad (15)
\]

\[
T_2 = \frac{2}{V_{\text{DC}} \sin 60} (V_{\text{ref}} \times \sin \alpha) \quad (16)
\]

Similarly in Triangle 2

\[
\frac{V_{\text{ref}} \cos(\alpha)}{\sin(\alpha)} = 0.5 \left[ \frac{\cos(0)}{\sin(0)} + V_\beta \frac{\cos(120 - \beta)}{\sin(120 - \beta)} \right] \quad (17)
\]

\[
V_{\text{ref}} \cos(120 - \beta) = V_{\text{ref}} \cos(\alpha) - 0.5V_{\text{DC}} \quad (18)
\]

\[
\sin(\beta) = \frac{\sqrt{3}}{2} \cos(120 - \beta) + \frac{1}{2} \sin(120 - \beta) \quad (19)
\]

From the above equations, substitution gives Triangle 2 timing values. Triangle 2:

\[
T_1 = \frac{1}{V_{\text{DC}} \sin 60} (V_{\text{ref}} \times \sin \alpha) - \frac{2}{V_{\text{DC}}} (V_{\text{ref}} \times \cos \alpha) - 1 \quad (20)
\]

\[
T_2 = \frac{1}{V_{\text{DC}} \sin 60} (V_{\text{ref}} \times \sin \alpha) + \frac{2}{V_{\text{DC}}} (V_{\text{ref}} \times \cos \alpha) - 1 \quad (21)
\]

The above equation indicates the simplified dwell time computation for duty ratio calculation in three-level inverters. Subdivisions of the dwell time for seven sequences (1012, 2721, 0121, 7212) are done by shift operations in an efficient manner. The shift operation takes very less time than the multiplication or division operation. Therefore, the region identification algorithm meets the desired timing requirement for implementing a fast SVPWM signal generation. The dwell time equations for Triangles 1–4 for the sector 1 are shown in Table 2.
2.4 Analysis of double switching SVPWM technique for three-level VSI

In this section, double switching SVPWM techniques [8] for three-level VSI are analysed based on the modified dwell time computation. The computation of the duty cycle for double switching sequences 0121/1012 can be obtained as follows in Triangle 1:

\[
d_R = \frac{T_i}{T_s} = \frac{2}{V_{DC}} \left[ (V_{ref} \times \cos \alpha) - \left( \frac{1}{2} V_{DC} \right) + \frac{1}{\sqrt{3}}(V_{ref} \times \sin \alpha) \right]
\]

(22)

\[
d_I = \frac{T_s + T_i}{T_s} = 0.5 + \frac{2}{V_{DC}} \left[ (V_{ref} \times \cos \alpha) - \left( \frac{1}{2} V_{DC} \right) + \frac{1}{\sqrt{3}}(V_{ref} \times \sin \alpha) \right]
\]

(23)

\[
d_B = \frac{T_s + T_i + T_3}{T_s} = 0.5 + \frac{2}{V_{DC}} \left[ (V_{ref} \times \cos \alpha) - \left( \frac{1}{2} V_{DC} \right) + \frac{1}{\sqrt{3}}(V_{ref} \times \sin \alpha) \right]
\]

(24)

Similarly for Triangle 2, the duty cycle can be obtained as follows:

\[
d_R = \frac{T_i}{T_s} = \frac{2}{V_{DC}} \left[ \left( \frac{3}{2} V_{DC} \right) \times \sin 60(\alpha) \right]
\]

(25)

\[
d_I = \frac{T_s + T_i}{T_s} = 0.5
\]

(26)

\[
d_B = \frac{T_s + T_i + T_3}{T_s} = 0.5 + \frac{2}{V_{DC}} \left[ (V_{ref} \times \cos \alpha) - \left( \frac{1}{2} V_{DC} \right) \right]
\]

(27)

The duty cycle computation is done for sequences 2721/7212 for Triangle 1 as follows:

\[
d_R = \frac{T_i}{T_s} + \frac{T_s + T_i}{T_s} = 0.5 + \frac{2}{V_{DC}} \left[ (V_{ref} \times \cos \alpha) - \left( \frac{1}{2} V_{DC} \right) \right]
\]

(28)

(see (29))

\[
d_R = \frac{T_i + T_3}{T_s} = \frac{2}{\sqrt{2} V_{DC}} [V_{ref} \times \sin \alpha] + \frac{2}{V_{DC}} [V_{ref} \times \cos \alpha] - \left( \frac{1}{2} V_{DC} \right) \left( \frac{1}{\sqrt{3}} V_{ref} \times \sin \alpha \right)
\]

(30)

Similarly for Triangle 2

\[
d_R = \frac{T_i + T_3}{T_s} = 0.5 + \frac{2}{\sqrt{3} V_{DC}} [V_{ref} \times \sin \alpha] + [V_{ref} \times \cos \alpha] - \left( \frac{1}{2} V_{DC} \right) \left( \frac{1}{\sqrt{3}} V_{ref} \times \sin \alpha \right)
\]

(31)

\[
d_I = \frac{T_s}{T_s} = 0.5
\]

(32)

\[
d_B = \frac{T_s + T_i + T_3}{T_s} = \frac{2}{V_{DC}} \left[ \frac{3}{2} V_{DC} \times \sin 60(\alpha) \right] - \left( \frac{1}{2} V_{DC} \right)
\]

(33)

2.5 Sample placement and waveform generation

Mapping of three-level voltage vectors to equivalent two-level voltage vectors reduces the complexity for calculating the dwell times for three-level inverter. In general, the samples are placed equidistantly to maintain symmetry in three-level inverter space. However, the uniformity is lost when the corresponding sampling points are converted into an equivalent two-level inverter. On account of this non-uniform placement of equivalent samples in two-level inverter, the SVPWM technique uses multiple chosen optimum switching sequences. This leads to a double switching transition between neighbouring samples with existing approaches. The existing approaches assign the specific sequences to a specific region of an equivalent two-level inverter. These approaches do not provide the capability of specifying switching sequence corresponding to a sample point of the reference voltage at a reference angle \( \alpha \) in three-level inverter. This violates the property of single transition between switching sequences at the crossover point of different samples in a sector and at the sector boundary as well. The pivot vector selection is fixed for each sector in the three-level hexagon. Advantage of the proposed framework is that the samples are placed with respect to three-level inverter configuration. Hence, it is possible to verify single switching violation between subsequent samples at the sector boundary or at the sub sector boundary.

In this work, samples are placed symmetrically in each sector around the middle sample to have three-phase symmetry (TPS) and half-wave symmetry (HWS). In the space vector domain, synchronised three-phase PWM waveforms can be defined regarding (i) number of samples corresponding to the reference vector per sector, (ii) positions of samples in every sector, and (iii) parallel switching sequence.

| Triangle number (Tr.No.) | \( T_i \) | \( T_3 \) |
|--------------------------|---------|---------|
| 1, 2                     | \( \frac{2}{V_{DC}} (V_{ref} \times \cos \alpha) - \frac{1}{V_{DC}} \sin 60(\alpha) \) | \( \frac{2}{V_{DC}} (V_{ref} \times \cos \alpha) - \frac{1}{V_{DC}} \sin 60(\alpha) \) |
| 3, 4                     | \( \frac{1}{V_{DC}} \sin 60(\alpha) \) | \( \frac{2}{V_{DC}} (V_{ref} \times \cos \alpha) - \frac{1}{V_{DC}} \sin 60(\alpha) \) |

\[
d_I = \frac{T_i}{T_s} = \frac{2}{V_{DC}} [V_{ref} \times \cos \alpha] - \left( \frac{1}{2} V_{DC} \right) \left( \frac{1}{\sqrt{3}} V_{ref} \times \sin \alpha \right)
\]

(29)
switching sequences used for every sample in a given sector. The sample number, sample positions and the sequences used in the sector I for the synchronised PWM strategies for three-level inverter level inverters are shown in Table 3.

Bus-clamping SVPWM algorithm can be implemented in this framework. Samples can be placed exactly at 30° in a sector as required by clamping strategies [8]. This is possible as the angle increment for the sample placement is controlled centrally. The switching states are selected by the triangulation of the space vector. The switching triangles are classified for three-level inverter and tracing of the reference vector in triangle varies with the modulation index value accordingly. The active triangle switching sequence starts from one vertex and ends in the same vertex during the end of the sampling period during the conventional sequence. The last switching sequence and first switching sequence are arranged in such a manner that double switching between the phases is avoided.

The switching pattern for sequences is determined by upper and lower triangles. The PWM switching sequence adheres by the following guidelines:

i. The pulse of opposite polarity is avoided in the line voltage waveform.
ii. Three phases and half-wave symmetry are ensured for the pole voltage waveform.
iii. The continuous switching of a phase is avoided.
iv. Double switching of the phases during switching transitions are avoided at the sector boundaries.

### 2.6 Hardware optimisation

The proposed method follows digital control framework and eliminates the need to sample phase voltages ($V_a$, $V_b$, $V_c$) separately. The digital controller framework consists of three stages. They include (i) modules that sample output voltage and compute error, (ii) compensation to generate command value for the Digital Pulse Width Modulator (DPWM) module, (iii) DPWM signal generation. The proposed algorithm samples rms voltage of one phase and generates eight bit modulation index command by a suitable compensation algorithm. The implemented SVPWM algorithm takes the modulation index command value and generates phase voltage values ($V_a$, $V_b$, $V_c$) by multiplying with the stored sine angle values. Sine angle values are stored only for the sample points between 0° to 90° (at most 18 values assuming 12 samples per sector) and rest of the sine angle values are generated from the symmetry of the sine function. The optimised sequences for the proposed strategy for different modulation index are stored as a part of the code segment. In this implementation, 6 kB instruction memory is used (150 combinations are stored for various modulation index corresponding to the linear range) whereas total available instruction memory is 64 kB. Switching sequences and the corresponding angles are stored in the lookup table only for the first sector (Fig. 5).

As the phase voltage values are generated from modulation index command, ADC requirement is simplified. PIC microcontroller ADC can be used to sense RMS value of the phase voltages. In the existing implementation [17, 24–27], phase voltages ($V_a$, $V_b$, $V_c$) are sampled and corresponding g–h values are generated. These implementations are very sensitive towards g–h rounding error which results in wrong triangle identification and spurious pulse generation. Authors in [27] solved the issues of rounding error by computing the centre value without the intermediate rounding operation. However, the requirement of high-performance ADC remains. High-performance ADC with four channels (two voltage sensing and two current sensing) needs to be controlled with a high-end FPGA board which increases implementation complexity significantly. The proposed algorithm achieves the same with the inbuilt ADC of the microcontroller.

### 2.7 Software optimisation

In [2], the sample values ($V_a$, $V_b$ and $V_c$) are sensed to generate the corresponding $V_{ref}$ and angle $\alpha$ (Three-level reference angle) implicitly. The algorithm needs six multiplications and a few additions to generate the SVPWM pulses. However, the algorithm generates two pivot vectors for every sample point and it has to choose one pivot vector out of the two to balance the capacitor voltages.

The proposed algorithm does six different capacitor balancing algorithms can be used in conjunction with [2] for three-level inverter.

The proposed algorithm samples rms voltage of one phase and generates eight bit modulation index command by a suitable compensation algorithm. Modulation index command is taken as input for every sample. A total number of samples $N$ for the fundamental cycle over six sectors is another static input (during compilation) to the program. Timing generation for the sample processing is controlled centrally by the PIC controller. The reference angle $\alpha$ is incremented after each sample is processed. There is a delay involved in between the samples and sector identification and dwell time calculation. This delay does not affect sample placement and can be aggregated with controller delay for calculating phase margin. The proposed algorithm also does six multiplications and a few addition operations as in [2] to compute dwell time and identify the sector for a sample. The region detection algorithm is implemented with multiplication operation only. Division and arc tan operations are avoided. Double switching SVPWM algorithm divides the dwell time for a specific vector in to multiple instances. The dwell time calculation is achieved for double switching techniques by shift operation as equal division of active vectors time corresponding to each vector is followed. Hence, the architecture is scalable as higher levels can be implemented with additional shift operations. The optimised sequences for the proposed strategy for different modulation index are stored as a part of the code segment. In this implementation, only 6 kB instruction memory is used (150 combinations are stored for various modulation index corresponding to the linear range) whereas total available instruction memory is 64 kB. Switching sequences and the corresponding angles are stored in the lookup table only for the first sector. Sequences for the other sectors are derived from the first sector. Therefore, space constraint is not an important issue in lookup table. The simplification of the algorithm enables to perform various double switching sequences and placement of different samples at a specific location. In this proposal, sine $\alpha$, cos $\alpha$ and sin (60–$\alpha$) corresponding to the first sector sample angles are computed and stored in an array and this part of computation is outside the critical loop. This is the part of initialisation code. The sine values are stored in an eight bit unsigned format by multiplying it by 100 and adding 100. Lookup table memory requirement to store sine angle values is $N/6$ bytes which is negligible. ($N_{max}$ = 72 for switching frequency = 2 kHZ for CSVPWM sequence).

A total number of samples $N$ for the fundamental cycle over six sectors is another input (during compilation) to the program. The sine values and the optimised sequences for various modulation index and angle $\alpha$ values for other sectors are mapped to the values of the first sector based on symmetry. Second sample of third sector is mapped to the second sample of the first sector with the modification of corresponding active vectors. The dwell time

### Table 3 Voltage vectors in sector I of three-level inverter

| Sample number | Sequences | Location of angles in first sector |
|----------------|-----------|-----------------------------------|
| 7              | 0127, 7210, 0127, 7210, 0127, 7210, 0127 | $-26.75^\circ, -11.25^\circ, -3.75^\circ, 3.75^\circ, 11.25^\circ, 18.75^\circ, 26.75^\circ$ |
| 7              | 1012, 2101, 1012, 2101, 1012, 2101, 1012 | $-26.75^\circ, -11.25^\circ, -3.75^\circ, 3.75^\circ, 11.25^\circ, 18.75^\circ, 26.75^\circ$ |
| 7              | 2721, 2721, 1272, 2721, 1272, 2721, 1272 | $-26.75^\circ, -11.25^\circ, -3.75^\circ, 3.75^\circ, 11.25^\circ, 18.75^\circ, 26.75^\circ$ |
| 7              | 2127, 7212, 2127, 7212, 2127, 7212, 2127 | $-26.75^\circ, -11.25^\circ, -3.75^\circ, 3.75^\circ, 11.25^\circ, 18.75^\circ, 26.75^\circ$ |
values of the first sample of the first sector are similar to the corresponding value of the first sample of the second sector. The implementation is done using a PIC microcontroller and timings are generated centrally by the microcontroller in a synchronised manner. The floating point computation complicates the approach for hardware implementation. Eight bit fixed-point arithmetic is adopted to carry out the calculations in this design to achieve efficiency in computation. The proposed method use trigonometric computations (with the help of lookup table) only three times per sample. The entire division operation is converted into multiplication to reduce the execution time.

2.8 THD minimisation and neutral point voltage balancing

The proposal addresses THD minimisation, balancing of capacitor voltages and generation of SVPWM signals for double switching sequences in a simple manner. The pivot vector selection is fixed for each sector in the three-level hexagon. The orientation of the switching vectors which forms the sides of the hexagon is decided for each sector. In three-level sector I, R phase value is greater than the Y phase and B phase. To keep the THD value low, ONN is chosen as a pivot vector instead of POO. The orientation of sequences in the first sector is obtained as ONN-ONO-ONO-ONN, ONN-PNN-PNO-PNN-ONN, ONN-PNN-PONPNN-ONN, ONN-ONO-ONO-PON-ONO-ONN for the four triangles, respectively. It is observed from Figs. 6b and 7b that there is a peak and notch for $I_{c1}$ and $I_{c2}$, respectively corresponding to every sector. In a sector I, $R$ phase sequences produce even symmetry for capacitor current $I_{c2}$. First 30° of $B$ phase and the last 30° of $Y$ phase produce even symmetry for capacitor current $I_{c1}$ in the sector I for three-level inverter. Similarly, first 30° of $Y$ phase and the last 30° of $R$ phase produce even symmetry for capacitor current $I_{c2}$ in sector II for three-level inverter. In sector II, $B$ phase sequences produce even symmetry for capacitor current $I_{c1}$.

In three-level sector II, $B$ phase value is the least in comparison with $R$ and $Y$ phases and THD is reduced by choosing PPO instead of OON. OON is used as a pivot for all switching sequences in three-level sector I and PPO is used as a pivot vector for all switching sequences in three-level sector II. Hence, the switching sequence is obtained as PPO-POO-PON-POO-PPO, PPO-PNN-PNO-PNN-PNO-PNO, PPO-ONO-ONO-ONO-ONO-ONO, PPO-OPO-OPN-OPN-OPO-PPO for the triangles, respectively. The switching sequences orientation is determined on the basis of optimised THD and are arranged in an array, and angle values are incremented in a centralised and symmetrical manner. Sectors I, III and V of the three-level inverter use the lowest possible $R$-value in the pivot vector. Sectors II, IV and VI of the three-level inverter use the highest possible $R$-value in the pivot vector. In this procedure, voltage imbalance for sector I is equal and opposite of
the voltage imbalance occurring in sector II. Similarly, voltage imbalance in sector III is equal and opposite of the voltage imbalance of sector IV. Sector V voltage imbalance is equal and opposite to the voltage imbalance of sector VI. In this proposal, the redundancies are sacrificed to balance neutral point voltage and to reduce THD. Fixed switching states are chosen in this proposal.

3 Design implementation and results

SVPWM involves an intensive computation in three-level inverter configuration. The simplified data representation forms an important part of the implementation. To maximise the computation precision over the whole calculation, data normalisation approach is adopted. In this method, only sine and cosine trigonometric functions are used. sin $\alpha$ and cos $\alpha$ are calculated once for dwell time equations and sin $(60-\alpha)$ is calculated once for region identification algorithm. Hence, the proposed method uses trigonometric functions only three times per sample. This is true for three levels as well. The division operation takes more time than the multiplication operations in the microcontroller. Hence all division operations in the equations are converted into multiplication operations to reduce the execution time. The simulations developed for the testing of controller are done based on the actual implementation code. Actual implementation code generates MATLAB EML files for simulation. In Matlab simulation, the sector time is provided by a ramp signal. One period of ramp signal ($r$) corresponds to one sector time. Samples and reference values are the input variables and the code generates the PWM signals.
The delay time of the switching state of a vector is maintained by a variable. The value of the variable is updated for every sample in the sector by ramp signal. The PWM control of the inverter system and control algorithm are modelled in the MATLAB/Simulink environment. The optimised flow chart is shown in Fig. 3. Three-level NPC inverter using double switching space vector modulation technique has been modelled and simulated with an induction motor load of 415 V, 50 Hz, 3 hp, 1460 rpm. The DC bus voltage of the multilevel inverter is varied using an auto transformer. The generated code is programmed in PIC18F452 microcontroller and is verified experimentally with the insulated gate bipolar transistor (IGBT) based three-level NPC VSI. The experimental prototype of a three-level inverter is verified on an induction motor load of 415 V, 2.2 kW fed with a DC bus voltage of 400 V. Table 4 shows the hardware details.

### Table 4 Hardware requirements

| Parameter       | Ratings          |
|-----------------|------------------|
| DC bus voltage  | 400 V            |
| three-level switch | SK30MLI066     |
| induction motor | 415 V, three-phase, 2.2 kW |
| PWM frequency   | 550–950 Hz       |

3.1 Simulation and experimental results

3.1.1 Simulation results: The different SVPWM strategies are implemented in MATLAB/SIMULINK. The existing conventional SVPWM technique and double switching SVPWM technique have been implemented based on the constant fundamental frequency. Fig. 8a represents the pole voltage waveform for conventional SVPWM and Fig. 8b represents pole voltage waveform for double switching sequence 2721 on a three-level inverter.

3.1.2 Experimental results: An IGBT (SK30MLI066) based 2 kVA three-phase three-level NPC voltage source inverter (VSI) with 400 V DC is designed and developed. The proposed work has been experimentally verified on the three-level NPC inverter with a three-phase induction motor (415 V, 2.2 kW) load. Figures are provided as proof of the experimental results. The experimental results for the double switching SVPWM sequences are collected. The pole voltage and line voltage waveform of different SVPWM double switching sequences indicate the experimental validation of the approach with an eight bit controller.

The experimental waveform for conventional SVPWM includes three-phase pole voltage waveform and line voltage waveform as shown in Figs. 9a and b, respectively. The three-phase pole voltage waveform and line voltage waveform for double switching

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Fig. 8 Simulation result of pole voltage of
(a) Conventional sequence, (b) 2721 for three-level VSI

Fig. 9 Experimental result of conventional sequence
(a) Three-phase pole voltage waveform, (b) Line voltage waveform, (c) FFT spectrum of line voltage waveform

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sequence 2721 are shown in Figs. 10a and b, respectively. The three-phase pole voltage and line voltage waveform for double switching sequence 1012 are shown in Figs. 11a and b, respectively. The three-phase pole voltage and the line voltage waveform of the 2721 and 0121 are shown in Figs. 12a, 13a, 12b, and 13b, respectively. The spectrum analysis indicates the THD performance of double switching sequences. The FFT spectrum in the figure indicates that 7212 sequence performs the best and is followed by 0121, 1012 and 2721 double switching sequences in the decreasing order. This performance is observed at a modulation index of 0.7. The memory utilisation of double switching sequences is given in Table 5.

The performance analysis of the double switching SVPWM is given in the next section. The experiment is performed for an induction motor under no load and full load conditions. A single pivot vector is used for the complete sector. The dc link balancing is determined by the dc link midpoint current. The application of pivot vector in each sector is done in a manner to cancel out the effect of variation of neutral point current. In symmetrical SVPWM, the voltage imbalance during an adjacent active vector interval is cancelled by the voltage imbalance carried out the other active vector in every sample. The variation of dc bus midpoint voltage in a sector is equal but opposite to that of the next sector. Hence, the dc bus capacitor voltages are balanced over every \((2\pi/3)\) radians because a single pivot vector is used for the
complete three-level sector. Perfect balancing of dc bus capacitor voltages helps in preserving HWS and thus even harmonics in the motor are eliminated. It is observed from Figs. 6 and 7 that the average value of neutral point current is less and the corresponding neutral point shift is limited by 4 V with limited oscillations for the zero point. This method avoids the use of additional feedback signals. The capacitor voltage balancing for CSVPWM and double switching 1012 sequence with dc link voltage waveforms, dc link capacitor currents with neutral point current and three-phase current waveform is shown in Figs. 6a–c and 7a–c.

3.2 Performance evaluation of double switching sequences for three-level VSI

The performance of the proposed method is presented in Table 6. The comparison table of the proposed method is shown which is advantageous with reference to memory requirement and computation time. The modulation index range of study is chosen in the range of 0.55–0.85. The voltage THD of the line voltage waveform in the linear modulation range is shown in Fig. 14a. The performance of double switching sequence 1012 and 7212 are better in the range <0.75 and performance of sequence 0127 and 2721 are better above this range. The switching loss analysis is shown in Fig. 14b. The switching losses of 2721 and 2127 are better in the corresponding lag and lead power factor range. The

![Fig. 12 Experimental result of 7212 sequence](image1)

(a) Three-phase pole voltage waveform, (b) Line voltage waveform, (c) FFT spectrum of line voltage waveform

![Fig. 13 Experimental result of 0121 sequence](image2)

(a) Three-phase pole voltage waveform, (b) Line voltage waveform, (c) FFT spectrum of line voltage waveform
The performance of sequences is done in Table 7. The performance is computed as

$$\text{THD}_{\text{index}} = \frac{V(T\text{HD}_{\text{sequence}})}{V(T\text{HD}_{\text{conventional}})} \times 100$$ (34)

$$\text{Loss}_{\text{index}} = \frac{SW_{\text{loss}_{\text{total}}}}{SW_{\text{loss}_{\text{CPWM}}}} \times 100$$ (35)

### 4 Main contributions of the proposal

i. The proposed method follows digital control architecture and eliminates the need to sample phase voltages ($V_a$, $V_b$, $V_c$) separately. The proposed algorithm samples rms voltage of a phase and generates eight bit modulation index command by a suitable compensation algorithm. The implemented SVPWM algorithm takes the modulation index command value and generates phase voltage values ($V_a$, $V_b$, $V_c$) by multiplying with the stored sine angle values. As the phase voltage values are generated from modulation index command, ADC requirement is simplified. PIC microcontroller ADC can be used to sense RMS value of the phase voltages.

ii. Existing approaches use DAC and drive circuitry to generate the gate pulses. Gate pulses are generated in the proposed implementation by the hardware PWM block and there is no need for DAC.

iii. Neutral point voltage balancing is provided by sacrificing the redundancy of the switching vectors. THD is minimised by choosing the appropriate pivot vector and neutral point voltage shift is limited by 4 V by choosing a specific representation of the switching vector depending on the sector.

iv. Bus-clamping SVPWM algorithm can be implemented in this framework. Samples can be placed exactly at 30° in a sector as required by clamping strategies [8]. This is possible as the angle increment for the sample placement is controlled centrally.

v. The proposed framework is similar to the existing approaches in terms of software computation overhead. Another advantage of the proposed framework is that the samples are placed with respect to three-level inverter configuration. Hence, it is possible to verify a single switching violation between subsequent samples at the sector boundary or at the sub sector boundary.

### 5 Conclusion

This paper proposes a generalised SVPWM scheme, dwell time computation formulated for three-level inverters in the linear modulation region. The proposed algorithm facilitates an efficient three-level SVPWM implementation to provide THD reduction, neutral point voltage balancing with a small lookup table. The proposal reduces the hardware complexity significantly by removing the requirement of high-performance multichannel ADC and the associated FPGA board. The proposal does not increase the software computing overhead and completes computation for the sample with six multiplication and a few add/sub operations. The framework also implements bus clamped SVPWM algorithms and can be implemented with a dsPIC microcontroller and a hardware PWM block. Hence, the proposed algorithm is termed as simplified to indicate significant hardware reduction. The SVPWM scheme is successfully tested in the developed controller with real-time simulation and hardware results.
Table 7  Performance Evaluation of sequences in three-level VSI for modulation index of 0.7

| Parameter          | CSVS | 1012 | 2721 | 2127 |
|--------------------|------|------|------|------|
| three-level – THD index | 100  | 38   | 35   | 40   |
| three-level – loss index | 100  | 101.66 | 109.6 | 103.6 |

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