An ion-implanted silicon single-electron transistor

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We report on the fabrication and electrical characterization at millikelvin temperatures of a novel silicon single-electron transistor (Si-SET). The island and source-drain leads of the Si-SET are formed by the implantation of phosphorus ions to a density above the metal-insulator-transition, with the tunnel junctions created by undoped regions. Surface gates above each of the tunnel junctions independently control the tunnel coupling between the Si-SET island and leads. The device shows periodic Coulomb blockade with a charging energy $e^2/2C \sim 250 \, \mu eV$, and demonstrates a reproducible and controllable pathway to a silicon-based SET using CMOS processing techniques.

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Single-electron transistors (SETs) have excellent potential as elementary devices in large scale circuits due to their small dimensions and low power dissipation. Applications for SETs in single-electron logic and memory cells have also been demonstrated. Silicon-based SETs (Si-SETs) are of particular interest because of their compatibility with CMOS technology. While the fabrication of Si-SETs devices is a non-trivial process, a number of different approaches have been demonstrated such as gated two-dimensional electron gases (2DEGs), pattern dependent etching of silicon-on-insulator (SOI) materials, and random formation of Coulomb islands by nano-particles or defects in silicon. Some difficulties of integrating such approaches into more complex single-electron circuits include inconsistent island formation resulting in random electron potentials and excessive gating requirements for electrostatically defining Coulomb islands and tunnel junctions.

The work presented in this letter features a Si-SET comprising of a single well-defined island and source-drain leads fabricated by a patterned phosphorus ion implantation process. This approach is not reliant on random island formation, and offers a new method for controlled, reliable and reproducible formation of Coulomb islands. This Si-SET essentially consists of two nano-scale metal-oxide-semiconductor field effect transistors (MOSFETs) in series with a micron scale central island, with the MOSFETs acting as tuneable tunnel junctions. As the island is solely defined by the patterned ion implantation, no gates are required to electrostatically define the island structure. Furthermore, the controlled formation of well-defined islands makes the coupling of multiple single-electron devices for more complex circuits a simpler task. We discuss the device fabrication and electrical measurements performed at $T = 50 \, mK$ in which Coulomb blockade behavior is observed.

Devices were fabricated on a high resistivity ($>5 \, k\Omega \cdot cm$) n-type silicon wafer. Firstly, ohmic contacts for the source and drain leads of the device were defined via phosphorus diffusion. A 5 nm gate oxide was then grown using a thermal oxidation process. Electrical characterization of (large-scale) MOSFET devices fabricated with gate oxides grown using the same process indicate typical trap densities of $2 \times 10^{11} \, cm^{-2}$ at $T = 4.2 \, K$. High-resolution TiPt (15 nm Ti, 65 nm Pt) alignment markers, 100 nm $\times$ 100 nm in dimension, were de-
dilution refrigerator using standard lock-in techniques at frequencies $< 200$ Hz. Initial characterization of these devices focused on the effect of the electrostatic barrier gates on the tunnel junctions. Figure 2(a) shows the conductance of a device with 150 nm wide tunnel junctions as a function of $V_{B1}$ and $V_{B2}$. The behavior observed in this device is representative of all of the devices that were measured. With increasing barrier gate voltage, the device conductance is increased as expected for an enhancement-mode MOSFET (see figure 2(b)). Resonances observed in the device conductance are visible in figure 2(a) as vertical and horizontal lines, and indicate that each barrier gate is primarily coupled to its respective tunnel junction. These resonances most likely arise from the random potentials in the tunnel junctions, due to stray dopants, charge traps and other defects. These form unintentional islands that exhibit either Coulomb blockade or resonant tunnelling phenomena. Even with these resonances present, the measurements indicate good gate control of the overall conductance of the tunnel junctions.

In figure 3(a), the grey trace shows the conductance of a Si-SET with 100 nm wide tunnel junctions as a function of $V_{C1}$ with $V_{B1} = V_{B2} = 0$ mV and $V_{SD} = 350$ µV. In the measurement, periodic Coulomb blockade oscillations are observed indicating a constant capacitance between the gate and the Si-SET island. The consistent form of the conductance peaks also indicates that the tunnel junctions are not significantly changing. Figure 3(b) shows a bias spectroscopy measurement for the same device. Coulomb charging diamonds with a constant charging energy are observed, consistent with charging a single metallic island as opposed to a random minimum potential in the tunnel junctions. This is in contrast to Coulomb blockade associated with unintentionally formed islands in the channel of FETs where the charging energy and periodicity changes significantly with island occupancy. In common with other SETs, the device is sensitive to $1/f$ charge noise and nearby two-level fluctuators (TLF) which perturb the device conductance, as observed in figure 3(b) around $V_{C2} = 110$ µV.

Further measurements were performed on the Si-SET with 100 nm wide tunnel junctions to observe how gate tuning of the tunnel barriers could be used to control the device conductance whilst maintaining Coulomb blockade behavior. A number of different voltages were applied to the barrier gates ($B1$ and $B2$). Under low source-drain bias conditions and $V_{B1} = V_{B2} = 0$ V, the device conductance is actually below the measurable threshold for standard lock-in amplifier techniques ($I_{SD} < 1$ pA). At $V_{B1} = V_{B2} = -200$ mV, the barrier gates are biased close to some resonance in the barriers which results in an overall increase in the conductance of the device. The black trace in figure 3(a) shows the Si-SET conductance under these barrier conditions and Coulomb blockade oscillations are clearly observed. In comparison to the grey trace in the same figure, which shows Si-SET conductance when $V_{B1} = V_{B2} = 0$ mV and $V_{SD} = 350$ µV, the peak conductance observed in the black trace is an order of magnitude higher ($G_{SET}^{grey} \sim 7 \times 10^{-3} e^2/h$ and $G_{SET}^{black} \sim 4 \times 10^{-2} e^2/h$). The periodicity of the oscillations are consistent between both traces reinforcing the notion that
Coulomb blockade in a single well-defined metallic island is being observed. Similar behavior is seen for barrier conditions where large positive voltages are applied to the barrier gates to increase the transparency of the tunnel junctions.

From the bias spectroscopy data shown in figure 3(b), the charging energy of the island in the Si-SET with 100 nm wide tunnel junctions is determined to be $e^2/2C_\Sigma \sim 250 \mu eV$ with a total capacitance $C_\Sigma \sim 320 aF$. The capacitances of gates $C_1$ and $C_2$ to the island are determined from the period of the measured Coulomb blockade oscillations to be 27 aF and 2.1 aF respectively. The capacitances of barrier gates $B_1$ and $B_2$ to the island were not measured for this device, however these values have been measured for other devices and are typically of order 100 aF. The asymmetry of the Coulomb diamonds is a result of the different capacitances between the implanted island and the source and drain leads, which are determined from the Coulomb diamonds to be 21 aF and 55 aF. This difference in capacitance can be attributed to the barriers being of slightly different dimensions and differences in their complex potential landscape.

A proof-of-principle has been demonstrated for the controlled formation of Coulomb blockade islands using CMOS processing techniques. The Si-SET demonstrates highly controllable single-island charging behavior due to the well-defined electron potential. The tunnel coupling between the Coulomb blockade island and leads can be changed by using electrostatic gates above the tunnel junctions (MOSFETs). The development of Si-SET as elements in more complex single-electron circuits requires the ability to controllably couple multiple islands and future work will focus on this. Whilst characterization of this device demonstrates Si-SET behavior at low temperature ($T = 50 mK$), further development of this fabrication technique will involve scaling down of the island size to enable the charging energy $E_C$ to dominate at higher temperatures ($E_C > k_B T$). In addition, related devices may provide a platform for the study of electron transport between locally doped regions in silicon, which is of particular relevance to silicon-based quantum computing.

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