N³H-Core: Neuron-designed Neural Network Accelerator via FPGA-based Heterogeneous Computing Cores

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ABSTRACT
Accelerating the neural network inference by FPGA has emerged as a popular option, since the reconfigurability and high performance computing capability of FPGA intrinsically satisfies the computation demand of the fast-evolving neural algorithms. However, the popular neural accelerators on FPGA (e.g., Xilinx DPU) mainly utilize the DSP resources for constructing their processing units, while the rich LUT resources are not well exploited. Via the software-hardware co-design approach, in this work, we develop an FPGA-based heterogeneous computing system for neural network acceleration. From the hardware perspective, the proposed accelerator consists of DSP- and LUT-based General Matrix-Multiplication (GEMM) computing cores, which forms the entire computing system in a heterogeneous fashion. The DSP- and LUT-based GEMM cores are computed w.r.t. a unified Instruction Set Architecture (ISA) and unified buffers. Along the data flow of the neural network inference path, the computation of the convolution/fully-connected layer is split into two portions, handled by the DSP- and LUT-based GEMM cores asynchronously. From the software perspective, we mathematically and systematically model the latency and resource utilization of the proposed heterogeneous accelerator, regarding varying system design configurations. Through leveraging the reinforcement learning technique, we construct a framework to achieve end-to-end selection and optimization of the design specification of target heterogeneous accelerator, including workload split strategy, mixed-precision quantization scheme, and resource allocation of DSP- and LUT-core. In virtue of the proposed design framework and heterogeneous computing system, our design outperforms the state-of-the-art Mix&Match design with latency reduced by 1.12-1.32× with higher inference accuracy. The N³H-Core is open-sourced at: https://github.com/elliothe/N3H_Core.

KEYWORDS
Hardware-software co-design; neural network accelerator; agile design; machine learning for EDA

1 INTRODUCTION
In the past decade, Deep Neural Networks (DNN) has succeeded in various computer vision and natural language processing tasks [14]. Accelerating the DNN with domain-specific accelerator [4, 5, 15] has been widely explored to counter the excellent computing power demanded by the mammoth DNN model that is growing exponentially [1, 12]. Compared to other off-the-shelf hardware accelerators, FPGA can quickly adapt to the fast-evolving algorithms with outstanding performance (e.g., latency, throughput, etc.), owing to its reconfigurability. It is known that the dominant operation in the DNN inference is the Multiplication and Accumulation (MAC) [4]. As the Digital Signal Processing (DSP) units in the FPGA can perform MAC efficiently, prior FPGA-based DNN accelerator designs heavily use the DSP resources to construct the processing elements (aka. DSP-core) as DNN inference engine. In contrast, as another significant on-chip resource of FPGA, Look-Up Table (LUT) is merely utilized to build the peripheral computing units that perform the computations of batch-normalization, activation, etc.

Thanks to recent advances in DNN compression algorithms [6, 11, 18, 27], parameters of DNN can be converted from 32-bit floating point to extremely low bit-width (e.g., <4-bits) with negligible inference accuracy degradation, but significantly simplify the computation complexity and mitigate the on-/off-chip data access bottleneck (aka. “memory wall”) [32, 36]. Moreover, researchers are aware that the layers of DNN own different sensitivity to the quantization noise resulted from different bit-width. Thus, the DNN quantization with varying bit-width emerges as an alleged compression scheme to minimize the overall model size. Note that, DSP-Core cannot efficiently support MAC operations with varying bit-width, due to the overhead caused by flexibility. Although a recent design proposed by Yaman et. al. called BISMO [29] can efficiently support mixed-precision MACs via a bit-serial computing method, the inference latency of BISMO is still much higher than the pure DSP-based bit-parallel counterpart, to achieve the identical accuracy for low bit-width quantization. For example, our preliminary experiment of 8-bit quantized ResNet-18 on ImageNet

CCS CONCEPTS
• Computer systems organization → Neural networks.

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dataset [8, 16] shows the inference latency of DSP-based and LUT-based (i.e., BISMO-based) design are 182ms and 309ms respectively. Thus, with the available DSP/LUT resources in the pool, an FPGA system that supports fully-flexible bit-width and outperforms other DSP-centric designs [15] is desired.

Furthermore, to maximize the performance of FPGA-based DNN accelerator, prior works [30, 37] have conducted the design space exploration. These studies either use the roof-line model to limit the design space or build the latency/performance model w.r.t the workload and architecture design parameters to explore the design space. While the former one cannot reflect the design parameters of the architecture, the latter does not impose constraints on parameters sufficiently, resulting in a enormous design space.

In summary, the preliminary architecture design of the FPGA-based DNN accelerator mainly counters the following drawbacks: 1) Rich on-chip LUT resource are not well utilized; 2) A high-performance architecture supporting mixed-precision operation is absent; 3) Lacking the systematic design methodology for the single-chip heterogeneous system. As the countermeasure, in this work, we propose a heterogeneous computing architecture, which fully utilizes the on-chip resources (including LUT, DSP, BRAM, etc.) for computing instead of control. Our proposed architecture consists of LUT-core and DSP-core that work jointly as a high-performance computing system. Such two computing cores handle computation with operands in flexible and fixed bit-width, respectively. To ease the manpower to optimize the complicated system configuration on large design space, we develop the end-to-end optimization framework as a systematic design methodology for the proposed single-chip heterogeneous system. Our contributions can be summarized as:

- To fully exploit the on-chip resource of the target FPGA, we propose a heterogeneous DNN accelerator architecture called N³H-Core that consists of DSP- and LUT-centric computing units (aka. DSP-core and LUT-core, respectively).
- For maximum throughput and minimum latency, we design the DSP- and LUT-core to operate w.r.t the predefined instructions in the intra-layer asynchronous fashion.
- We construct scalable and adaptable cost model across different DNNs and FPGA, to precisely estimate the resource utilization, inference latency, and other metrics-of-interests.
- Through the cost model of the N³H-Core, we apply the Reinforcement Learning (RL) technique to build the end-to-end optimization framework that automatically generate the architecture configurations (resource allocation), data flow (layer-wise workload split ratio), and DNN (quantization bit-width of weights and activations) respectively. Thus, given the target DNN and FPGA platform, an agile and optimal design can be rapidly achieved.

2 PRELIMINARY AND RELATED WORKS

2.1 DNN Inference Acceleration on FPGA

Recently, many studies [15, 28, 31] have been conducted to explore using FPGA in DNN acceleration for flexibility and high computation performance. Those designs can be generally categorized into bit-parallel and bit-serial counterparts, specified as follow.

2.1.1 Bit-parallel Acceleration. For bit-parallel computing, the bits of operands are fed in parallel into the computing unit, e.g., the DSP on FPGA that typically used to compute multiplications. Prior designs [3, 15, 28, 31] focus on bit-parallel accelerator with DSP for optimized latency, throughput, etc. For latency reduction, [31] proposes a latency-centric optimizer to explore design space efficiently. [28] presents a systematic design space exploration methodology to maximize the throughput of an OpenCL-based FPGA accelerator, taking source available on-chip as constraints. [3] proposes a heterogeneous architecture that utilizes DSP and LUT resources. The logarithmic quantization is used to replace the multiplication with bit-shift. However, the architecture of [3] is not bit-width flexible and without automated architecture optimization.

2.1.2 Bit-serial Acceleration. In bit-serial scheme, accelerator is designed to support highest operand bit-width, even when some operands are in low bit-width, thus lead to great hardware overhead. To mitigate that, bit-serial scheme computes one binary multiplication per cycle which can compose operations on higher bit-width operands. Given integer matrix \( L \) and \( R \), their multiplication is:

\[
L = \begin{bmatrix}
2 & 0 \\
1 & 3
\end{bmatrix}, \quad R = \begin{bmatrix}
0 & 1 \\
2 & 1
\end{bmatrix}, \quad P = L \cdot R = \begin{bmatrix}
2^1 L^{[1]} + 2^0 L^{[0]} \\
2^1 R^{[1]} + 2^0 R^{[0]}
\end{bmatrix}
\]

\[
= 2^1 L^{[1]} \cdot R^{[1]} + 2^1 L^{[1]} \cdot R^{[0]} + 2^0 L^{[0]} \cdot R^{[1]} + 2^0 L^{[0]} \cdot R^{[0]}
\]

\[
= \begin{bmatrix}
0 & 1 \\
1 & 0
\end{bmatrix}
\]

where \( L \times R \) is decomposed into weighted sum of the binary matrix multiplication. Such computation transform is hardware-friendly and can be efficiently implemented with LUT on FPGA, which is adopted in BISMO design [29]. Based on Eq. (1), BISMO propose a GEMM core (depicted in Figure 1 composed of a M-by-N DPU array, where each DPU unit performs the binary vector dot-product via the XNOR and pop-count). According to the bit-serial computing fashion, the computing latency of BISMO is proportional to the operand bit-width of \( L \) and \( R \). Thus, such computing architecture is prone to compute with the low bit-width operands.

2.2 Model Quantization

DNN model quantization has emerged as a mandatory technique for high-performance DNN inference. Thanks to the advances in
model quantization algorithm [6, 7, 18, 19, 21, 38], the activations and weights in 32-bit floating-point (fp32) can be quantized into extreme low bit-width with negligible inference accuracy degradation, using uniform [20] or non-uniform quantizer [23] in quantization-aware training [18, 19] or post-training quantization [21]. In this work, we focus on the model quantization using $N_{\text{bits}}$-bit uniform quantizer, and its quantization function can be expressed as:

$$\hat{x} = f_q(x, s) = \text{clip}(\text{round}(\frac{x}{s}), \hat{a}, \hat{b})$$

where $s$ is the step size, $\hat{a} = -2^N_{\text{bits}} - 1$ and $\hat{b} = 2^N_{\text{bits}} - 1$ are the upper and lower bound for the $N_{\text{bits}}$ integer representation. clip($\cdot$, $\hat{a}$, $\hat{b}$) = $\min(\text{max}(\cdot$, $\hat{b}$), $\hat{a}$) is the clipping function, and round($\cdot$) denotes the round function. With the uniform quantizer adopted, two quantization schemes (uniform precision and mixed precision) are usually applied upon the entire DNN mode.

**Uniform Precision.** Uniform precision quantization assigns identical bit-width to each layer of target DNN. Researchers [7, 13, 38] have shown that INT8, even INT4, can retain accuracy on many neural networks. For the general-purpose computing hardware (e.g., CPU or GPU), due to the hardware constraint, only INT4 and INT8 are supported. Thus, uniform precision quantization is a relatively general method, as most hardware platforms only support computation (e.g., MAC) in specific bit-width.

**Mixed Precision.** As the prior investigations [2, 33, 34] reveal the fact that layers of DNN own different redundancy, the quantization with varying bit-width on different layers emerges as a potential scheme to minimize the model size of target DNN. [39] determines the layer-wise bit-width based on the entropy of weights and activations. [9] utilizes the second-order information, i.e., Hessian matrix, to determine the bit-width, where the block with higher top Hessian eigenvalue will be assigned with higher bit-width. Elhakeb et al. [10] use the sample efficiency of Proximal Policy Optimization (PPO) to find the optimal bit-width, which is the first to use RL for quantization. Wang et al. [33] predict the layer-wise bit-width via Deep Deterministic Policy Gradient (DDPG) algorithm with the target hardware taken into consideration.

### 3 ARCHITECTURE OF N$^3$H-CORE

In this work, we propose a heterogeneous neural network accelerator called N$^3$H-Core, which fully exploits both the DSP and LUT resources in a heterogeneous fashion. Its architecture, data flow and cost and latency models are specified as follows.

#### 3.1 Architecture Overview of N$^3$H-Core

As depicted in Fig. 2, N$^3$H-Core architecture consists of (1) instruction generator, heterogeneous computing cores (i.e., (2) LUT-core and (3) DSP-core), (4) address generator, and (5) peripheral buffers.

**Instruction Generator.** N$^3$H-Core is an intra-layer asynchronous and inter-layer synchronous instruction-based neural network accelerator. Thus, the instructions adopted can be generally separated into two categories: operation instruction and synchronization instruction, which jointly work for accurate pipelining computation within LUT- and DSP-_core. Within each layer, Operation Instructions are generated asynchronously and specifically for the LUT-Core and DSP-Core, consisting of three types $\{\text{Fetch, Execute, Result}\}$ that corresponds to three operating phases of LUT- and DSP-core, respectively. 1) In Fetch phase, Direct-Memory Access (DMA) module loads weight and activation data from the off-chip DDR to on-chip buffers; 2) In Execute phase, data is transmitted from buffers to computing cores for multiplication and accumulation; 3) In Result phase, the calculation results from the LUT- and DSP-core are written back to the shared result buffer. Thanks to the synchronous instructions (Sync), two cores are synchronized after they complete the assigned workloads, then launch the computation of successive layer without conflicts.

Based on prior designs [22, 29], we propose a new schedule for matrix multiplication and design Fetch, Execute and Result engines to run the corresponding instructions, as described in Fig. 3. Referring to Eq. (1), we assume the activation buffers possess the capacity of the activation matrix $L$, and weight buffer is the half capacity of weight matrix $R$. To begin with the first part $L$ and $R$, $R_0$ is fetched by fetch engine, then $L_0$ is fetched as well. Meanwhile, execute and fetch engines are in waiting status, i.e., Wait-Fetch (WF) and Wait-Execute (WE). When fetch instructions is completed, the fetch engine sends a synchronization signal to activate the execute engine, i.e., Sync-Execute (SE). After the execute engine receives the signal, it immediately transfer from WF status to run the execute instruction of $L_0 \times R_0$. While the $L_0 \times R_0$ is executing, the fetch engine start to load following binary matrix $L_1$ for pipelining. After fetching the first tile of weight data $R_2$ and $R_3$, the weight buffer is filled, so the fetch engine is in WE status, waiting for a synchronization signal from execute engine. After the signal is received, the fetch engine continues to fetch the next tile of weight data $R_2$ and $R_3$. Once the $R_2$ is fetched, the execute engine multiplies the pre-loaded binary matrices of $L$ in a sequence. When all the multiplications are done, the result engine receives the synchronization signal (Sync-Execute, SE) from the execute engine, then shift from Wait-Execute (WE) status to run Result instruction that store the computation result back to DDR. In this way, the design bridges the gap between data movement and processing.

For instruction compatibility for DSP- and LUT-core, all instructions are 128-bits composing different segments for information representation. For Fetch and Result instructions, they consist of base address (16-bits), stage control (3-bits), read/write range (1-bit)

![Figure 2: Overview of proposed N$^3$H-Core architecture, which includes the DSP- and LUT-core. The grey and green lines are the instruction flow and data flow respectively.](image-url)
of on-chip buffer and base address (32-bits), offset (24-bits), and write/read range (16-bits) of the DDR. For Execute instruction, it includes the on-chip buffer data address, and the GEMM-Core parameters listed in Table 1. For sync instruction, it includes the current (1-bit) and next state (2-bits) of each Engine and the flag (3-bits) indicating the sent of synchronization token.

**Heterogeneous Computing Core.** To fully utilize the on-chip resource of a target FPGA for boosted computing power, we develop a heterogeneous computing core that consists of **LUT-core** and **DSP-core**. Given a computing task (e.g., inference with one layer of DNN), the computation workload is split w.r.t a designated ratio, then performed by the LUT- and DSP-core asynchronously. Note that, the optimization of workload split ratio will be discussed in Section 5.3. For the LUT-core, we adopt the open-sourced BISMO\(^2\) [29] as its backbone, which is a GEMM kernel with run-time adjustable operand bit-width in virtue of the bit-serial computing mechanism. In contrast to the LUT-core operating in the bit-serial fashion, the DSP-core is developed for bit-parallel computing. Overall, the heterogeneous computing core incorporates prior-neglected rich LUT resources and introduces a more flexible weight-activation quantization scheme for accuracy lossless mapping.

**Peripheral Buffer.** To avoid the frequent off-chip memory access that hampers the overall inference latency and improve the throughput via pipelining, the proposed architecture allocates each computing core with input/weight/result buffers. Weight and activation data are fetched via Direct Memory Access (DMA) to the dedicated buffers, then transferred to the computing cores. Once the computation is done, the result stored in the result buffer is then written to DDR as the activation of the next layer.

**Memory Control.** Two workload partitions allocated to two computing cores are stored at different regions on DDR to make the data access more efficiently and avoid conflict. **Address Generator** controls the base address and strides to instruct two partitions fetched from DDR. After the computation of one layer is finished, **DMA** gives new base addresses and strides to store the result.

### 3.2 Heterogeneous Computing Core

#### 3.2.1 LUT-Core

Through the conversion function (i.e., \(\text{im2col}\)), the computation of various parametric layers (e.g., convolution layer, fully-connected layers) can all be computed via the matrix multiplication (GEMM). Fig. 1 illustrates the architecture of LUT-Core. In LUT-Core, the buffers allocated to the row are designated as the activation buffer (indexed from 0 to \(M−1\) in Fig. 1), the activation buffers have the depth of \(D^a_{L,buf}\) whose interface width is \(K\). Similarly, the buffer allocated to the column is weight buffers indexed from 0 to \(N−1\), and the depth is \(D^w_{L,buf}\) whose interface width is \(K\) as well. Each DPU reads \(K\)-bits from the activation buffers and \(K\)-bits from weight buffers simultaneously, then store the binary dot multiplication results as partial sum. The LUT-Core can process \(M \times N \times K\) bits in parallel. As listed in Table 1, \(\{M, N, K, D^a_{L,buf}, D^w_{L,buf}\}\) are five important configuration parameters significantly affect the latency, which will be explored at design time.

#### 3.2.2 DSP-Core

The architecture detail of DSP array is illustrated in Fig. 4. Note that, the DSP core performs the GEMM in tiling fashion as well. In Execute phase, a tile of input activation data and weight data are read from buffers into register arrays. The register array of activation data has \(N^a_{\text{reg.row}}\) rows and \(N^a_{\text{reg.col}}\) columns. Correspondingly, the register array of weight data has \(N^w_{\text{reg.row}}\) rows\(^3\) and \(N^w_{\text{reg.col}}\) columns. For activation buffer, the size of each row of activation register array is same as the activation buffer. Thus, the total bit-width of each buffer is \(N^a_{\text{reg.col}}\times B^w\), where \(B^w\) is the activation bit-width. During the computing, each row of the activation array is filled with an activation buffer per cycle. For weight

### Table 1: Architecture design knobs for \(N^3\)H-Core.

| Notation | Description |
|----------|-------------|
| \(M\)    | Numbers of rows in LUT-Core (DPU array) |
| \(N\)    | Numbers of columns in LUT-Core (DPU array) |
| \(K\)    | Input bit width of DPU |
| \(D^a_{L,buf}\) | Depth of activation buffers in LUT-Core |
| \(D^w_{L,buf}\) | Depth of weight buffers in LUT-Core |
| \(N^a_{\text{reg.row}}\) | Numbers of rows in activation register array |
| \(N^a_{\text{reg.col}}\) | Numbers of columns in activation register array |
| \(N^w_{\text{reg.row}}\) | Numbers of columns in weight register array |
| \(D^a_{D,buf}\) | Depth of activation buffers in DSP-Core |
| \(D^w_{D,buf}\) | Depth of weight buffers in DSP-Core |
| \(B^a\) | Bit-widths of quantized activation |
| \(B^w-L\) | Bit-widths of quantized weight on LUT-Core |
| \(B^w-D\) | Bit-widths of quantized weight on DSP-Core |

\(\text{BISMO}: \) https://github.com/EECS-NTNU/bismo

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\(^2\)BISMO: https://github.com/EECS-NTNU/bismo

\(^3\)Note that, the row size of weight register array is identical to the column size of activation register array.
A Buffer
[53x85]which means DSP
⌈
we use the 32-bits for convenience. Thus, the BRAM size consumed
weight buffer.
To minimize the latency by finding the optimal architecture config-
uration buffers. Likewise, since we allocate data in one buffer to two
ime. The DSP-Core utilizes all the DSP resource available on chip,
is mainly consumed by the instruction generator and the control
is
\[ N \]
one activation buffer consumes, and
bit-width ranges from 2 to 4 bits. When the activation bit-width
core is designed for 4-bit multiplication, the quantized activation
the depth of
buf
a
ber of activation buffer equals to the
 latency model describes the end-to-end inference latency.

DSP-Core Cost Model. As described in Section 3.2.2, the num-
ber of activation buffer equals to the \[ N_{\text{reg}, \text{col}} \times 32 \], and each buffer has the depth of \[ D_{\text{buf}} \], with the interface of \[ N_{\text{reg}, \text{col}} \times B^a \]. Since our DSP-core is designed for 4-bit multiplication, the quantized activation bit-width ranges from 2 to 4 bits. When the activation bit-width \[ B^a \] is less than 4, we pad zeros to make it 4-bits for storing in buffers. The BRAMs forming buffers are 1024 in-depth and 36-bits wide, and we use the 32-bits for convenience. Thus, the BRAM size consumed by DSP-Core is formulated as:

\[
\text{BRAM}_{\text{D-core}}(N_{\text{reg}, \text{row}}, N_{\text{reg}, \text{col}}, N_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}]) = \left\lfloor \frac{N_{\text{reg}, \text{row}} \cdot 32}{2} \right\rfloor \cdot (N_{\text{reg}, \text{col}} \cdot \left\lfloor \frac{D_{\text{buf}, \text{dy}}}{1024} \right\rfloor + N_{\text{reg}, \text{col}} \cdot \left\lfloor \frac{D_{\text{buf}, \text{w}}}{1024} \right\rfloor) \tag{3}
\]

where \[ \left\lfloor \frac{N_{\text{reg}, \text{col}} \times 4}{32} \right\rfloor \cdot \left\lfloor \frac{D_{\text{w}, \text{buf}}}{1024} \right\rfloor \] is the BRAM size that one activation buffer consumes, and \[ N_{\text{reg}, \text{row}} \] is the size of activation buffers. Likewise, since we allocate data in one buffer to two columns of the weight register array, the amount of weight buffers is \[ \left\lfloor \frac{N_{\text{reg}, \text{col}} \times 4}{32} \right\rfloor \cdot \left\lfloor \frac{D_{\text{w}, \text{buf}}}{1024} \right\rfloor \] is the BRAM size that one weight buffer consumed. For LUT usage of DSP-Core, it is mainly consumed by the instruction generator and the control module, which is about 1000 as a constant (LUT_{DSP-core} = 1000). The utilization rate of DSP resources is predefined as 100% at design time. The DSP-Core utilizes all the DSP resource available on chip, which means \[ \text{DSP}_{\text{D-core}} = \text{DSP}_{\text{Available}} \].

LUT-Core Cost Model. Since we adopt the BISIMO [29] as the backbone of LUT-core, we inherits its cost model as:

\[
\text{LUT}_{\text{L-core}}(M, K, N) = M \cdot N \cdot (aK + b + c) + d \tag{4}
\]

\[
\text{BRAM}_{\text{L-core}} = \left\lfloor \frac{K}{32} \right\rfloor \cdot (M \cdot \left\lfloor \frac{D_{\text{buf}, \text{dy}}}{1024} \right\rfloor + N \cdot \left\lfloor \frac{D_{\text{buf}, \text{w}}}{1024} \right\rfloor) \tag{5}
\]

where \[ \{a, b, c, d\} = \{1.17, 120.1, 44.1, 718\} \] are the fitting coefficient. From Eq. (4), the LUT utilization is proportional to \( M, K, \) and \( N \). We use 1024 in-depth and 36-bits wide BRAMs to build the buffer, and we only use 32-bits of the original interface. As mentioned before, there are \( M \) activation buffers and each of them is comprised of \( [K/32] \cdot [D_{\text{buf}, \text{dy}}/1024] \) BRAMs. Similarly, the BRAMs consumed by weight buffer is calculated by Eq. (5).

DSP-Core Latency Model. As the DSP-core is an instruction-orien-
ted computing unit whose instruction pipeline is organized in a specific pattern, we build its latency model with its instruction pipeline. We focus on the execute engine and count the latency as following queues: \( L_{\text{wait}}, L_{\text{run}}, L_{\text{rst}} \) and \( L_{\text{sig}} \). These four parts of latency are relevant to the parameters \( [N_{\text{reg}, \text{row}}, N_{\text{reg}, \text{col}}, N_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}}] \) in Table 1. Then, we trace the instructions streams and accumulate the latency of each phase on execute engine. Note that, \( L_{\text{wait}} \) is the latency of waiting for fetching data (i.e., phases denoted by 0 in Fig. 3), \( L_{\text{run}} \) is the latency of execution (phases denoted by 1), \( L_{\text{sig}} \) is the latency of sending signal (indicated by 2), and \( L_{\text{rst}} \) is the latency of result phase. By accumulating each latency, the computational latency of one layer is formulated as:

\[
L_{\text{DSP}} = g(N_{\text{reg}, \text{row}}, N_{\text{reg}, \text{col}}, N_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}}) = \sum L_{\text{wait}} + \sum L_{\text{run}} + \sum L_{\text{sig}} + \sum L_{\text{rst}} \tag{6}
\]

To fully utilize the DSP resource on-chip, we adopt a simple simulation method that \( N_{\text{reg}, \text{col}}, N_{\text{buf}, \text{dy}} \) are fixed to 16, and only \( N_{\text{reg}, \text{row}} \) can be modified that determines the latency performance. Therefore, it ensures that DSPs are fully-utilized by modifying only one parameter, and a simple core design method is provided at the same time. Then, the calculation of Eq. (6) can be simplified as:

\[
L_{\text{DSP}} = g(N_{\text{reg}, \text{row}}, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}}) \tag{7}
\]

LUT-Core Latency Model. Likewise, the latency model of LUT-
core is built in the same manner via describing and simulating the instruction streams. However, the main difference is that LUT-Core computes the MACs in a bit-serial fashion, whose latency is determined by the bit-width of activation \( B^a \) and weight \( (B^w)^2 \) matrices. Thus, the parameters that relevant to the LUT-Core latency is \( [B_{\text{bits}}, D_{\text{bits}}, M, K, N, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}}] \), and the latency model of LUT-Core is formulated as:

\[
L_{\text{LUT}} = f(B_{\text{bits}}, D_{\text{bits}}, M, K, N, D_{\text{buf}, \text{dy}}, D_{\text{buf}, \text{w}}) = \sum L_{\text{wait}} + \sum L_{\text{run}} + \sum L_{\text{sig}} + \sum L_{\text{rst}} \tag{8}
\]

Note that, the weight buffer reads one tile at once. Thus, the capacity of the weight buffer is the size of one tile weight data, while the depth change will not affect the latency. Correspondingly, we simplify the latency model of LUT-Core as:

\[
L_{\text{LUT}} = f(B_{\text{bits}}, D_{\text{bits}}, M, K, N, D_{\text{buf}, \text{w}}) \tag{9}
\]

such where simplification also shrink the design space to be explored by reducing the variation of \( D_{\text{buf}, \text{w}} \).

Figure 4: DSP-Core architecture. Activation and weight data are computed in tiling fashion via DSP array.
4 HYBRID QUANTIZATION WITH MIXED PRECISION

Suppose an N-layer DNN as \( \{ W_i, X_i \}_{i=1}^N \), \( W_i \in \mathbb{R}^{c_{in} \times d \times d \times d_i} \) and \( X_i \) denotes the i-th layer weight and input/activation tensor respectively, where \( d \) is the kernel size\(^4\), \( c_{in} \) and \( c_{out} \) are number of input and output channels. The weight tensor \( W_i \) can be viewed as a set \( W_i = \{ W_k^{i}_{\text{LUT}}, W_k^{i}_{\text{DSP}} \} \), where \( W_k^{i}_{\text{LUT}} \in \mathbb{R}^{c_{in} \times d \times d} \) denotes the k-th filter. Our work applies filter-wise quantization, which takes a finer-grained strategy with \( k \) as its granularity. For different filters in one layer, 3-D tensor \( W_k^i \) is assigned with different quantization bit-width.

The hybrid quantization method integrates both uniform- and mixed-precision quantization in this work. The computation of one layer for DSP- and LUT-core is allocated in the granularity of filters. All the computations conducted by DSP-core are 4-bits quantized on weights. The rest of filters computed by LUT-core are quantized with \( B^\text{w-L} \) bits (2 ~ 8-bits) which is determined by our optimization framework (Section 5). Note that, \( B^\text{w-L} \) varies in different layers. The filter allocation ratio will be discussed in Section 5.3, which determines the number of filters allocated to DSP-/LUT-core on each layer. Besides, we need to consider which filters should be allocated to DSP-/LUT-core. In this work, the filter allocation (to DSP/LUT) depends on the KL-divergence \( D_{KL} \) of the original filter weight distribution \( W_k^i \) and its quantized weight distribution (calibrated via one batch of images). The filters with greater \( D_{KL} \) in one layer will be allocated to the computing core with higher bit-width, since the quantization bit-widths \( B^\text{w-L} \) of LUT filters is flexible. Now, the filter number and type allocation problems are settled.

We adopt the layer-wise quantization manner for activations shared by both LUT- and DSP-core. The activation and weight of first and last layer are quantized into 8-bits. In our work, we set the activation bit-widths range as 2-4 bits for all other layers, as the LUT-core enjoys much less latency with operands in low bit-width. Moreover, we linearly quantize the weights and activations of each layer using \{ 4, \( B^\text{w-L} \) \}-bits and \{ \( B^\text{w-L} \) \}-bits respectively. The linearly quantized model only requires fixed-point computing unit, which is more efficient in our heterogeneous architecture. The proposed quantization method of the \( i \)-th convolution layer is depicted in Fig. 6.

5 FRAMEWORK FOR OPTIMIZED SYSTEM

5.1 Framework Overview

This section describes our framework to automatically generate the optimized system configuration for N3H-Core to achieve the optimized performance across varying DNNs and FPGAs. The objects to be optimized by the framework come in threefold: 1) Resource Allocation. The framework configures the design parameters listed in Table 1 to achieve the optimized resource allocation for both LUT-core and DSP-core; 2) Workload Split. As the N3H-Core splits the computing task into LUT- and DSP-core in the layer-wise fashion, the framework is expected to split the computation task for workload balance properly; 3) Quantization bit-width. Since LUT-core supports operands with flexible bit-width while DSP-core only supports the fixed one (i.e., 4 in this work), the quantization bit-width affects the overall inference latency and accuracy.

\(^{4}d = 1\) for fully-connected layer

Figure 5: Experiments of Latency model. (a) shows the matching of predicted and measured latency. (b) reveals the trend of prediction error w.r.t design size. The layer in larger workload has higher latency and smaller prediction error.

As N3H-Core performs the DNN inference in a layer-wise synchronization manner, the total computation latency of target DNN with N-layers can be expressed as:

\[
\text{Latency} = \sum_{i=1}^{N} \max \left( L^i_{\text{LUT}}, L^i_{\text{DSP}} \right) \tag{10}
\]

where the \( L^i_{\text{LUT}} \) and \( L^i_{\text{DSP}} \) denotes the computation latency taken by the LUT-core and DSP-core to complete the assigned workload for \( i \)-th layer respectively. Since the instructions of our LUT-core and DSP-core are scheduled in static pipeline, the latency model formulated via accumulated execution time of schedule instruction is relatively accurate. To verify our latency model, we test 10000 design points with design knobs listed on Table 1 of original manuscript using randomly generated value, where the result is shown in Fig. 5 with prediction error less than 2%.

Figure 6: Proposed hybrid quantization scheme. Filters in each layer computed by DSP-core and LUT-core are quantized with uniform- and mixed-precision respectively.
As discussed in Section 3, we formulate the latency model for LUT- and DSP-core, and design factors influencing the latency and the corresponding ranges are tabulated in Table 2. Design factors $K, M, N, D^a_{\text{L,buf}}, D^b_{\text{D,buf}}, D^w_{\text{D,buf}}$ are related to resource allocation.

The left design factors $K, M, N, D^a$ are the quantization bit-widths of LUT filters and activations of each DNN layer. We leverage the Reinforcement Learning (RL) with DDPG algorithm [25] for the design space exploration (can be viewed as sequential decision making) to identify the optimal system configuration with low latency but high accuracy. The change of design factors leads to different resource usage estimated by our cost model, which is constrained by the available resources on the target FPGA devices.

### 5.2 Resource allocation & Quantization

As discussed in Section 3, we formulate the latency model for LUT- and DSP-core, and design factors influencing the latency and the corresponding ranges are tabulated in Table 2. Design factors $K, M, N, D^a_{\text{L,buf}}, D^b_{\text{D,buf}}, D^w_{\text{D,buf}}$ are related to resource allocation.

The left design factors $K, M, N, D^a_{\text{L,buf}}$ are in the format of $0 < v < 5, v \in \mathbb{N}$, and the rest $0 < v < 5, v \in \mathbb{N}$.

| Design Factors | Range on $D_A$ | Range on $D_B$ |
|----------------|----------------|----------------|
| $K$            | $64 \cdot v$   | $64 \cdot v$   |
| $M$            | $1-50$         | $1-252$        |
| $N$            | $1-50$         | $1-252$        |
| $D^a_{\text{L,buf}}$ | $1024 \cdot v$ | $1024 \cdot v$ |
| $D^b_{\text{D,buf}}$ | $1024 \cdot v$ | $1024 \cdot v$ |
| $D^w_{\text{D,buf}}$ | $1024 \cdot v$ | $1024 \cdot v$ |

The left design factors $K, M, N, D^a_{\text{L,buf}}, D^b_{\text{D,buf}}, D^w_{\text{D,buf}}$ are related to resource allocation.

The overview of our DDPG based RL learning framework [17] to explore both the architecture configuration and workload assignment between heterogeneous cores is depicted in Fig. 8. Details of action space, state space, reward, and etc are given as follows.

### 5.4 RL implementation details

The overview of our DDPG based RL learning framework [17] to explore both the architecture configuration and workload assignment between heterogeneous cores is depicted in Fig. 8. Details of action space, state space, reward, and etc are given as follows.

#### 5.4.1 Action Space

The action space contains two tasks of actions: action-1 $a_1$ and action-2 $a_2$ in sequence. The action-1 decides the resource utilization design factors which is constrained by the available resources of given FPGA devices. Table 2 provides the range of resource utilization design factors on two FPGAs. In each episode, the RL agent takes $6 + 2N$ action steps, where $N$ is the number of layers of given DNN.

For action-1, the agent chooses the hardware-related factors $K, M, N, D^a_{\text{L,buf}}, D^b_{\text{D,buf}}, D^w_{\text{D,buf}}$ sequentially at the first 6 time steps. For each time-step, the agent output one action applies on one aforementioned hardware factor, which can be described as:

$$a^h_t = \text{round} \left( a_t \cdot \text{value}_{\text{max}} - \text{value}_{\text{min}} \right) + \text{value}_{\text{min}}$$

where $t \in [0, 5]$. The continuous action $a_t$ (range: $[0, 1]$) of the DDPG agent is discretized by round function(round) into the range of 6 design factors in integer. Note that, $K, D^a_{\text{L,buf}}, D^b_{\text{D,buf}}, D^w_{\text{D,buf}}$ are in the format of $c \cdot v$ where $c$ is a constant parameter and $v$ is a variable. For these 4 parameters, $[\text{value}_{\text{min}}, \text{value}_{\text{max}}]$ is the range of the parameter $v$, so the actions $[a^h_1, a^h_2, a^h_3, a^h_4]$ will be multiplied with their corresponding constant parameters $c$ which are shown in Table 2.
For action-2, the agent chooses the software-related factors \((B^{Lw}, B^{sw})\) with 2N steps. The actions can be described as:

\[
   a_t^2 = \text{round}(a_t \times (b_{\text{max}} - b_{\text{min}} + 1) + b_{\text{min}} - 0.5) \quad (14)
\]

where \([b_{\text{min}}, b_{\text{max}}]\) is the bit-width range in Table 2.

5.4.2 State Space. The state space \(S_t\) for the \(t\)-th time step is expressed as:

\[
   S_t = (\text{id}_\text{func}, i, \text{NN}_i, \text{ratio}_i, a_t) \quad (15)
\]

where \(\text{id}_\text{func}\) is the binary indicator for the current task (0 for \(a_t^1\), 1 for \(a_t^2\)), \(i\) is the layer index, \(\text{NN}_i\) is the DNN information of the \(i\)-th layer, \(\text{ratio}_i\) is the calculated filter number allocation ratio in the \(i\)-th layer, \(a_t\) is the action of the current time step. \(i, \text{NN}_i\) and \(\text{ratio}_i\) are set as 0 when \(\text{id}_\text{func}=0\). The DNN information of the \(i\)-th layer \(\text{NN}_i\) is a group of parameters defined as:

\[
   \text{NN}_i = (c_{i,\text{in}}, c_{i,\text{out}}, s_{\text{kernel}}, s_{\text{stride}}, s_{\text{map}}, n_{\text{params}}, \text{id}_{\text{ac}\&\text{dw}}, \text{id}_{\text{m}/n}) \quad (16)
\]

where \(c_{i,\text{in}}\) and \(c_{i,\text{out}}\) are input/output channels, \(s_{\text{kernel}}\), \(s_{\text{stride}}\), and \(s_{\text{map}}\) are the sizes of the kernel, stride and feature map. \(n_{\text{params}}\) denotes the parameters. \(\text{id}_{\text{ac}\&\text{dw}}\) is the binary indicator for shortcut layers of ResNet [16] and depthwise layers of MobileNet [26]. If shortcut or depthwise, it is set 1, otherwise 0. \(\text{id}_{\text{m}/n}\) is the binary index for the type of the current action: 0 for quantization of LUT filters \(B^{\text{Lw}}\), 1 for quantization of activations \(B^{\text{sw}}\).

Thus, the entire state space \(S_t\) can be unfolded as:

\[
   S_t = (\text{id}_\text{func}, i, c_{i,\text{in}}, c_{i,\text{out}}, s_{\text{kernel}}, s_{\text{stride}}, s_{\text{map}}, n_{\text{params}}, \text{id}_{\text{ac}\&\text{dw}}, \text{id}_{\text{m}/n}, \text{ratio}_i, a_t) \quad (17)
\]

In addition, we normalize each dimension of the state space \(S_t\) into \([0, 1]\) to make them in the same scale.

5.4.3 Reward. After actions are taken in each episode, the model latency with current design configuration is estimated by our latency model, and the DNN is quantized w.r.t the identified quantization scheme. Then, we retrain the quantized model for one epoch to recover the accuracy, denoted as \(\text{acc}_q\). The reward function \(R\) is designed by combining the model latency \(L_m\) and accuracy \(\text{acc}_q\), which is formulated as:

\[
   R = \begin{cases} 
   \frac{L_m - L_t}{L_t} - 1 & L_m > L_t \\
   \text{acc}_q - \text{acc}_b & L_m \leq L_t 
   \end{cases} \quad (18)
\]

where \(L_t\) is the latency bound or target latency, \(\text{acc}_b\) is the baseline accuracy of our model, \(\lambda = 0.01\) is a scaling factor. Note that, the reward remains less than -1 when the model latency exceeds the latency bound, otherwise the reward is in the interval of \((-1, 1)\).

6 EXPERIMENTS

In this section, we conduct experiments on various representative DNNs and FPGA devices to demonstrate the merits of hardware and software parts of \(\text{N}^3\)-Core.

6.1 Experimental Setup

Networks and Dataset. In this work, we use two of the classic image classification neural architectures, i.e., ResNet-18 [16] and MobileNet-V2 [26] with large-scale ImageNet dataset [8]. The data augmentation is identical as stated in [16]. The full-precision pre-trained model utilized in the \(\text{N}^3\)-Core is obtained from the Pytorch model hub [24].

Hyper-parameters of software framework. The RL agent explores 900 episodes for each experiment setting. For each episode, if the model latency is within the latency bound, we will retrain the quantized model for one epoch to recover its accuracy for reward evaluation. We use SGD as optimizer with a fixed learning rate of 0.001 and momentum of 0.9. We randomly sample 100 categories of ImageNet to accelerate the exploration process.

FPGA platforms. Two FPGA boards, i.e., XC7Z020 and XC7Z045, are chosen as the target hardware platforms. With the \(\text{N}^3\)-Core architecture deployed upon different FPGAs, the device-specific configuration scheme is given by the framework automatically, constrained by the available hardware resources (e.g., DSP, LUT and BRAM). The operating frequency is set to 100MHz.

6.2 Results and Analysis

We evaluate the framework under different target latency bounds, and generate 8 configuration combinations for the two DNNs and two FPGAs. The accuracy and latency of each configuration are tabulated in Table 5, where the configuration details are given in Table 3. For each configuration, we also provide the quantization bit-widths and the workload-split ratio of each layer in Figs. 9 to 12.

6.2.1 Resource allocation Analysis. From Table 3, on DA we can find that \(K\) is greater when the DNN is ResNet-18. \(K\) denotes the computational parallelism of input channels of activation. A large \(K\) allows more input channels to be computed in parallel, improving the computation efficiency. Compared with ResNet, MobileNet contains depth-wise layers which occupy one-third of the number of layers. Since depth-wise layers has a small number of input channels, the agent tends to assign a small \(K\) to LUT-Core. It indicate that LUT-Core is more efficient in computing ResNet than MobileNet. Thus, for MobileNet, the agent allocates more BRAMs to DSP-Core, which allows DSP-Core compute faster to compensate for the inefficiency of LUT-Core. As shown in Fig. 11, for the same reason, the split ratios of many depthwise layers in MobileNet...
Table 4: Comparisons with state-of-the-art implementations on ImageNet

| Implementation | MobileNet-V2 [35] | ResNet-18 [3] | MobileNet-V2 Ours¹ | ResNet-18 Ours¹ | MobileNet-V2 Ours² |
|----------------|-------------------|---------------|--------------------|----------------|--------------------|
| Device         | ZU2EG             | ZU9EG         | XC7Z020            | XC7Z045        | XC7Z020            | XC7Z045            |
| Bit-width (W/A)| 8/8               | 4/4           | 4/4                | Flexible       | Flexible           | Flexible           |
| Top-1 Accuracy | 68.1              | 70.27         | 65.64              | 70.45          | 70.39              | 66.25              |
| Frequency (MHz)| 430               | 333           | 100                | 100            | 100                | 100                |
| LUT            | 31198             | 161944        | 28288              | 145049         | 39623              | 152868             | 45765              | 192624             |
| DSP            | 212               | 2070          | 220                | 900            | 220                | 900                | 220                | 900                |
| BRAM           | 145               | 771           | 56                 | 225.5          | 137                | 541                | 137                | 461                |
| Latency (ms)   | -                 | -             | 8.29               | 7.28           | 35.79              | 32.47              | 7.51               | 6.62               |
| Throughput (GOPS)| -                | -             | 7.70               | 359.2          | 101.3              | 446.8              | 80.1               | 363.5              |
| Frame Rate (FPS)| -                | -             | 21.3               | 99.1           | 120.7              | 549.3              | 27.9               | 123.2              | 133.2              | 604.2              |
| GOPS/DSP       | -                 | -             | 0.350              | 0.391          | 0.326              | 0.363              | 0.460              | 0.496              | 0.364              | 0.404              |
| GOPS/LUT       | -                 | -             | 2.725              | 2.475          | 2.538              | 2.252              | 2.557              | 2.923              | 1.750              | 1.887              |

¹ Config. D₁₆N₁₀ResNetT₃₀ms & Config. D₁₆N₂₀ResNetT₃₅ms
² Config. D₈N₈MobileNetT₃₀ms & Config. D₈N₈MobileNetT₃₅ms

6.2.2 Quantization Analysis. In Fig. 9, it reveals that the RL agent assigns more bit-width in down-sampling layers (layer 8, 13, 18). To avoid the information bottleneck, higher bit-width is assigned to those layers (e.g., 7-bits for LUT-Core filters and 4-bits for shared activations). When the target latency bound is set to 30ms, the quantization bit-width becomes lower under the strict limitation. Consequently, the LUT-Core latency is reduced, and more workload is assigned to the LUT-Core to keep the latency below the bound. This proves that the agent can automatically analyze the latency and adjust the bit-width and ratio. As shown in Fig. 11, LUT-Core is not efficient to compute depth-wise layers, thus the workload split ratio of depth-wise layers is lower than point-wise layers. When the bound is set to 5ms, the bit-width across layers is further lowered compared to the 7ms counterpart. On D₈B, the configuration of quantization and ratio shows the same trend.

6.2.3 Comparison with the state-of-arts accelerators. We selected the results of ResNet18 and MobileNet networks on two devices XC7Z020 and XC7Z045, as shown in Table 4, and compare the experimental results with the existing state-of-arts designs. When deploying ResNet18 on the given two FPGA devices, we obtain comparable accuracy while reducing latency by $\frac{32}{35}$ and $\frac{24}{25}$ compared to the Mix&Match design [3]. The Mix&Match is also a heterogeneous architecture utilizing DSP and LUT resources, but without exploring the design space, our latency-centric architecture outperforms it on resource utilization, quantization bit-width flexibility, and performance (e.g., latency, throughput and frame rate), even though they adopt more hardware-friendly power-of-2 [21] quantization scheme.
Figure 11: Layer-wise bit-width setting and workload split ratio in Config. $D_{AN_{MobileNet}}T_{5ms}$ and $D_{AN_{MobileNet}}T_{7ms}$.

Figure 12: Layer-wise bit-width setting and workload split ratio in Config. $D_{BN_{MobileNet}}T_{5ms}$ and $D_{BN_{MobileNet}}T_{6ms}$.

As can be found in Table 4, our proposed optimization framework makes better utilization of the on-chip resources, consuming more BRAMs and LUTs to boost the performance. In terms of the throughput per resource unit, the GOPS/DSP is higher on both devices. The GOPS/kLUT on XC7Z020 is less, but when more batches are computed simultaneously on XC7Z045, it outperforms the design in [3]. On MobileNet, we get the speedup by about 1.12× on both FPGA devices. The lower performance improvement on MobileNet over ResNet is due to the low computation efficiency of LUT-Core on MobileNet. This is also reflected in the efficiency of hardware resource usage. Despite the performance improvement, the throughput per resource unit on both devices is lower than Mix&Match [3]. Therefore, the proposed heterogeneous architecture has a limited effect on depth-wise acceleration. Moreover, in terms of the frame-rate (FPS), our design outperforms the mix&match, and will outperforms design in [35] (2.48 ×2.89× FPS) as well when it operates at 100MHz.

### 7 CONCLUSION

In this paper, we propose a heterogeneous architecture on FPGA with two cores (DSP/LUT-core) computing synchronously for efficient DNN inference. We also propose a hybrid quantization scheme which quantizes the NN weights according to the filter computation allocation. To rapid hardware-mapping evaluation and find the optimal resource allocation (BRAM, LUT) scheme for DSP- and LUT-core, we build the latency and cost models for both that parameterized by architecture configuration knobs. Based on aforementioned models, we utilize the reinforcement learning agent to identify the optimal design considering both resource allocation and quantization in an end-to-end fashion, for low latency and high accuracy. The framework can adapt to different FPGAs by changing the available resources in the cost model. We utilize two FPGAs XC7Z020 and XC7Z045 as the test-beds to evaluate our framework, and the explored configuration can reduce latency by 1.12×-1.32× compared with the state-of-the-art Mix&Match design.

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| Table 5: Evaluation Accuracy, IDE simulated and FPGA measured latency of $N^3$H-Core running with ResNet18 and MobileNet-v2 on ImageNet dataset. |
|-----------------------------|-----------------|-----------------|-----------------|-----------------|
| $N^3$H-Core                | Bit width (W./A.) | Accuracy (%) (Top1/Top5) | Model latency (ms) | Measured latency (ms) |
| Configuration               |                 |                 |                  |                  |
| ResNet-18                  |                  |                  |                  |                  |
| Pretrained Baseline         | 32/32           | 69.76/89.08     | N/A              | N/A              |
| Manual Config. $D_{AN_{ResNet}}$ | 4/4          | 69.65/89.11     | 40.96            | 42.26            |
| Auto. Config. $D_{AN_{ResNet}}T_{5ms}$ | Flexible | 67.28/87.85     | 29.14            | 31.43            |
| Auto. Config. $D_{AN_{ResNet}}T_{7ms}$ | Flexible | 70.45/89.54     | 34.95            | 35.79            |
| MobileNet V2               |                  |                  |                  |                  |
| Pretrained Baseline         | 32/32           | 71.88/90.29     | N/A              | N/A              |
| Manual Config. $D_{BN_{MobileNet}}$ | 4/4          | 65.18/75.77     | 8.85             | 9.15             |
| Auto. Config. $D_{AN_{MobileNet}}T_{5ms}$ | Flexible | 62.76/73.32     | 4.93             | 5.66             |
| Auto. Config. $D_{AN_{MobileNet}}T_{7ms}$ | Flexible | 66.25/76.09     | 6.95             | 7.51             |
| Auto. Config. $D_{BN_{MobileNet}}T_{5ms}$ | Flexible | 63.41/73.56     | 4.86             | 5.33             |
| Auto. Config. $D_{BN_{MobileNet}}T_{6ms}$ | Flexible | 66.04/75.88     | 5.93             | 6.62             |
