THD Analysis on a Single Phase 7-Level Diode Clamped MLI with LC Filter Based on Multicarrier Anti-Phase SPWM Technique

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Abstract. Inverter is an electronic device which is an important part to convert DC-AC energy. Increased use of renewable energy as a substitute for fossil energy that is running low encourages the increased performance of the inverter. Multilevel inverter offer many advantages for improving the performance of an inverter system. Diode Clamped Multilevel Inverter are explored with 7-level circuits that are analyzed and simulated specifically on the quality of the output ie the amount of harmony. The power switch control technique uses Anti-Phase SPWM with multicarrier. Further to maximize damping harmonics, LC filter is applied and researched. This research is using PSpice A / D Lite to simulate a system that worked. The results obtained harmonic attenuation reached 3.93% after LC filter.

1. Introduction

Power electronic as an interesting topic to be discussed, especially in the field of renewable energy to produce electrical energy generating systems that are economical, efficient and environmentally friendly. One important device in renewable energy systems is the DC-AC converter or commonly called an inverter [1][7]. Several researched were conducted to produce inverters with good performance. An important parameter of inverter performance by taking into account the harmonic values arising from the conversion or switching process. The high harmonics content can cause damage to electrical devices [2][7]. Passive filter design with inductor and capacitor configurations can reduce harmonic [4]-[6]. But it has a size large enough so that it requires a large amount of space and cost also in a conventional inverter [3]. The addition of semiconductor components as a power switch with various multilevel inverter (MLI) topologies to produce multilevel output waves and close to sinusoidal waveforms. The advantages of MLI have a low harmonic number adjusted to the number of levels produced and has a higher efficiency because it operates at low switching frequency [7]-[12]. The output of the MLI inverter has a low harmonic magnitude helping in designing filter with smaller and economical size [11]. This research uses a diode clamped multilevel inverter (DCMLI) topology that has a simple structure using a single voltage source. In addition, DCMLI has a voltage balance and has high efficiency because the device is activated based on a basic frequency [15][16][17]. As with other MLI, increasing the number of output levels at DCMLI proportional to the increase in the number of components used. Thus, the use of filters is still needed to improve the quality of the output.
of MLI in general, the resulting waves are still shaped like a sinusoidal ladder. LC filter is included in the classification of Low Pass Filter (LPF) which function to pass low frequency signal and block high frequency signal. LC filters are effective in reducing harmonics caused by the DC-AC conversion process or switching process in the circuit [13][14].

Figure 1. Shows that this research emphasizes the simulation and analysis of unfiltered and filtered 7-level DCMLI output. The parameters analyzed were Total Harmonic Distortion (THD) from DCMLI. As for controlling the power switch using the Anti-phase SPWM technique with multicarrier. The advantages of the SPWM anti-phase technique are easy to implement and offer a good reduction in current harmonics [7][15].

Figure 1. Renewable energy block diagram

2. Diode Clamped Multilevel Inverter Topology (DCMLI)

The proposed single-phase DCMLI topology can be seen in Figure 2, a DC source connected directly to the multilevel inverter circuit. The use of capacitors C1 to C6 in series functions as DC Link which divides the voltage into 7 voltage levels at each point. Clamped diodes arranged to push the input voltage at a certain voltage level connected to the capacitor and based on the switching process by the power switch. The strategy of the power switch switching process can be seen in table 1.

![Figure 2. Diode Clamped Multilevel Inverter Topology (DCMLI)](image_url)

Table 1. Switching strategies on 7-Level DCMLI

| $V_{out}$ | $V_{DC}/2$ | $V_{DC}/4$ | $V_{DC}/6$ | $V_{DC}/6$ | $V_{DC}/4$ | $V_{DC}/2$ |
|-----------|------------|------------|------------|------------|------------|------------|
| Switch State | M$_6n$ | M$_5n$ | M$_4n$ | M$_3n$ | M$_2n$ | M$_1n$ | M$_1m$ | M$_2m$ | M$_3m$ | M$_4m$ | M$_5m$ | M$_6m$ |
| $V_{DC}/2$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_{DC}/4$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_{DC}/6$ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_{DC}/6$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $V_{DC}/4$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| $V_{DC}/2$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
3. Anti-Phase SPWM with multicarrier
Generally SPWM anti-phase has the same modulation technique with the SPWM technique, which is
to compare between reference signal \( V_r \) with carrier signal \( V_c \). Where if \( V_r > V_c \), the modulation result is 1 and vice versa \( V_r < V_c \) the modulation result is 0. The SPWM anti-phase uses two reference signals to produce a power switch control signal. This research uses a multilevel inverter that is DCMLI so that to control the power switch requires a multilevel control signal.

The number of Multicarrier signals is adjusted by the number of levels in MLI. Figure 3 (a) presents an illustration of the SPWM anti-phase technique with multicarrier, multicarrier arranged to be modulated with sine1 producing an output signal that will be used to control the power switch \( (M_{1n}, M_{2n}, M_{3n}, M_{4n}, M_{5n}, M_{6n}) \) as shown in figure 3 (b). Meanwhile, the multicarrier and sine2 modulation process will produce an output signal to control the power switch \( (M_{1m}, M_{2m}, M_{3m}, M_{4m}, M_{5m}, M_{6m}) \).
4. LC Filter

The switching process on the inverter to convert the DC voltage source into AC using a high switching frequency results in harmonics. Therefore, Low pass filter (LPF) is the right choice based on its characteristics. LPF works to block high frequencies and pass low frequencies. LC filters are simple, easy to implement and effective in reducing harmonics. Figure 4 (a) shows an LC filter circuit consisting of an inductor that is inserted against a load and a capacitor that is paralleled with the load.

\[ f_c = \frac{1}{\sqrt{L_C}} \]  

(1)

IEEE Std. 519-1992 has determined harmonic limit standards for voltage and current. Where, the good THD limit is below 5%. THD voltage and current can be obtained by the equation.

\[ THD_V = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1}} \]  

(2)

and

\[ THD_I = \sqrt{\frac{\sum_{n=2}^{\infty} I_n^2}{I_1}} \]  

(3)
5. Simulation Result
This research uses PSpice A / D Lite software to do simulations based on the circuits that have been made. The simulation carried out is to find out the output characteristics of DC-AC converter (DCMLI) based on the SPWM anti-phase technique with multicarrier. Then display the LC filter characteristics, the percentage of THD before and after passing the filter. The following parameters in conducting this simulation can be seen in table 2.

Table 2. System parameters

| Parameter   | Value | Unit |
|-------------|-------|------|
| V_{DC} (Source) | 500 | V    |
| f_{sw}      | 10   | kHz  |
| f_{o}       | 50   | Hz   |
| L_{f}       | 330  | µH   |
| C_{f}       | 27   | µF   |
| R_{load}    | 330  | Ω    |

Figure 7 shows the output of the 7-level DCMLI before and after filtering. The waveform before filtering does not resemble sinusoidal, the voltage amplitude of 218.4 with a fundamental frequency of 50 Hz and has a 8.02% THD percent is still above the standard determined by EEE Std. 519-1992 i.e. <5%. Meanwhile, the Golombang form after passing through a filter approaches pure sinusoidal. The voltage amplitude of 223.3 with a fundamental frequency of 50 Hz and has a THD of 3.95% in accordance with predetermined standards.

![Graph showing output of 7-level DCMLI before and after filtering.](a)

**Figure 5.** (a) 7-Level DCMLI output based on unfiltered and filtered SPWM anti-phase techniques (b) percent THD Unfiltered (c) percent THD filtered.
6. Conclusion
In this research, a 7-level single-phase DCMLI was successfully carried out with the aim of improving the quality of output and reducing the size of single-phase inverters. Unfiltered DCMLI output obtained based on SPWM anti-phase technique with a switching frequency of 10 kHz can reduce the THD percent. However, it still has a THR percent that does not meet IEEE Std standards. 519-1992. LC filter that has been designed to significantly reduce THD percent output. Of course, a multilevel inverter output reduces the size of the filter. When the filter is used the output quality of the inverter is closer to the sine wave.

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