Digital nonlinearity calibration for pipelined ADCs using sampling capacitors splitting

Fan Chaojie, Lu Yuxiao, Wang Ke, and Zhou Jianjun
School of Microelectronics, Shanghai Jiaotong University, 800 Dongchuan Road, Minhang, Shanghai 200240, China
a) zhoujianjun@sjtu.edu.cn

Abstract: A digital background calibration method correcting non-linear errors of residue amplifiers in pipelined ADCs is presented. The technique makes use of the proportional scaling feature of linear systems to measure and correct severe nonlinearity errors, and is highly effective once there is a non-zero input to the ADC, regardless of the input distribution. Simulation shows that using the proposed digital calibration, SNDR is improved from 58 dB to 91 dB and SFDR from 68 dB to 104 dB, in a 16 bit prototype pipelined ADC with 1% capacitor mismatches and a residue amplifier having up to 10.3% gain compression in the 1st pipeline stage.

Keywords: pipelined ADC, nonlinearity error, digital calibration
Classification: Integrated circuits

1 Introduction

Pipelined ADCs are popular in applications where high conversion speed (over 100MSPS) and high resolution (12–16 bit) are simultaneously required, such as wideband wireless communications. Traditionally, capacitor mismatch is the main error source limiting the resolution of pipelined ADCs, which can be
corrected by various calibration algorithms. However, as device sizes continuously scale down, the amplifier nonlinearities has become more and more prominent, severely degrading the ADC performance, especially at high conversion rates when the conventional high-gain amplifiers are no longer proper due to limited settling speed. Several nonlinearity calibration techniques have been published [1, 2, 3, 4] but few has been widely accepted as a practical solution, due to either the very limited nonlinearity correcting ranges or the effective correction relying on certain input distributions. This paper proposes a novel digital background calibration scheme to correct severe nonlinearity errors of inter-stage residue amplifiers in pipelined ADCs. The proposed calibration algorithm makes use of the proportional scaling feature of linear systems to extract error information of nonlinear gain stages and is able to correct severe nonlinearity with a very short convergence time and little dependence on input distributions. Furthermore, the implementation of the proposed calibration only introduces small analog circuit modifications and little digital computational complexity to the ADC design.

This paper is organized as follows. Section 2 models the nonlinear inter-stage gain errors in pipelined ADCs, and briefly reviews the calibration concept. Section 3 describes the proposed nonlinear calibration mechanism in detail, with the simulation results presented in section 4. Section 5 concludes this paper.

2 Nonlinearity calibration basics

Fig. 1 shows the mathematical model of a pipelined ADC, where the 1st stage with a nonlinear inter-stage residue amplifier, denoted by f(x), is described in detail. To focus on inter-stage gain calibration, the sub D/A converter in stage1 and the subsequent stages are assumed error-free in this section. Generally, the residue amplifier presents an odd function when implemented with fully differential circuits, expressed by its Tyler Expansion: \( f(x) = a_1x + a_3x^3 + a_5x^5 + a_7x^7 \), where higher order terms are negligible in practice, and offset is assumed to be measured and canceled by some other techniques such
as chopping [5]. The residue of stage1, \( V_{\text{res}} \) is firstly amplified by \( f(x) \) to ease the quantization of subsequent stages, whose output is then recovered in digital domain to \( D_{\text{res}} \), by another odd function \( g(x) \), and summed with the digital output \( D_1 \) of stage1, resulting in the final digital code \( D_{\text{in}} \) representing the original input \( V_{\text{in}} \):

\[
D_{\text{in}} = D_1 + D_{\text{res}} = D_1 + g(f(V_{\text{res}}))
\]

\[
= D_1 + g(f(V_{\text{in}} - V_{\text{DAC}1})) = D_1 + g(f(V_{\text{in}} - D_1))
\]

Note that \( V_{\text{DAC}1} \) is equal to \( D_1 \) because an ideal sub-DAC in stage1 is assumed.

The basic concept of any inter-stage gain calibration technique is to solve proper parameters of \( g(x) \) so that the combined function \( g(f(x)) \) equals unity, and \( D_{\text{in}} \) equals \( V_{\text{in}} \), in most cases, a 3\(^{rd}\) order polynomial is sufficient to approximate the inverse of \( f(x) \) so that the remaining error does not limit the ADC resolution, as shown in Fig. 1. The techniques in [1, 2] both create an additional mode, and measure the difference between them as an indicator of nonlinear errors, however, the differences are measured at fixed input levels so that the calibration efficiency strongly depends on input signal distributions. A variant of the two-mode technique was introduced in [3], where a covariance computation helped avoid input distribution dependency, at the cost of significantly increased digital circuit complexity. In [4], the HDC technique inserts several calibration sequences into the MDAC input, extracts the parameters of \( f(x) \) at the output of backend stages, and uses \( b_1 \approx 1/a_1 \), \( b_3 \approx -a_3/a_1^3 \) to approximate the correction function \( g(x) \), but this approximation limits the degree of nonlinear errors it can handle, furthermore, the correlation used to extract \( a_3 \) and \( a_1 \) leads to a very long convergence time. In all the preceding works, a common idea is to first linearize the combined function \( g(f(x)) \), by solving \( b_3 \), then the linear gain estimation of \( b_1 \) becomes an easy work given many existing methods [3, 4, 6], therefore, the way to solve \( b_3 \) is the main determinant of the technique’s performance and efficiency.

### 3 The proposed calibration method and circuit implementation

The basic idea of the proposed technique is depicted intuitively in Fig. 2, where the curve representing the function of \( D_{\text{res}} = g(f(V_{\text{res}})) \) is plotted in solid line. Linearity requires that a function’s output is strictly proportional to its input, meaning that when input is halved, the output should also be halved. Therefore, it is appropriate to set the objective of nonlinearity calibration as to solve a certain \( b_3 \) so that Eq. (2) is satisfied, as explained geometrically in Fig. 2:

\[
e = 2 \cdot g(f(V_{\text{res}}/2)) - g(f(V_{\text{res}})) = 0
\]

To explain the circuit implementation of this method, the conventional MDAC operation in a multi-bit pipeline stage is reviewed in Fig. 3. In the sampling phase, all unit capacitors are charged to input \( V_{\text{in}} \); in the amplification phase, each unit capacitor \( C_k \), \( k = 1 \sim n \), connects its top plate to
$d_k V_{ref}$, where $d_k = \pm 1$ is controlled by sub-ADC output and $V_{ref}$ is the reference voltage, while leaving the bottom plate floating, this is equivalent to applying a combined sub-DAC output voltage $V_{DAC}$ to all unit capacitors, as expressed by Eq. (3):

$$V_{DAC} = \frac{V_{ref}}{C_1} \sum_{k=1}^{n} d_k W_k, \quad W_k = \frac{C_k}{\sum_{j=1}^{n} C_j} \quad \text{(3)}$$

where $W_k$ is the weight of unit capacitor $C_k$ in the array. The difference between $V_{in}$ and $V_{DAC}$ forms the quantization residue $V_{res}$, and is amplified by the residue amplifier (implemented either in closed-loop or open-loop form):

$$V_{res} = V_{in} - V_{ref} \cdot \sum_{k=1}^{n} d_k W_k \quad \text{(4)}$$

Inspired by the conventional MDAC operation analyzed above, $V_{res}/2$ can be achieved by evenly splitting each unit capacitor $C_k$ of the stage to be calibrated into $C_{1k}$ and $C_{2k}$, $k = 1 \sim n$, as shown in Fig. 4(a), resulting in two capacitor arrays $C_1(1:n)$ and $C_2(1:n)$ instead of one, and using one of them in
sampling and amplification while keeping the other grounded. Fig. 4(b) illustrates a new operation pattern wherein $C_{11} \sim C_{1n}$ serve the roles as $C_1 \sim C_n$ conventionally do, and $C_{21} \sim C_{2n}$ are always grounded. We denote this operation pattern as MODE', the equivalent input as $V'_{in}$, and the equivalent sub-DAC output as $V'_{DAC}$, then these quantities can be expressed as:

$$V'_{in} = V_{in} \cdot \sum_{k=1}^{n} W_{1k}, \quad V'_{DAC} = V_{ref} \cdot \sum_{k=1}^{n} d_k W_{1k}, \quad W_{1k} = \frac{C_{1k}}{\sum_{j=1}^{n} (C_{1j} + C_{2j})}$$

where $W_{1k}$ is the weight of $C_{1k}$. The quantization residue $V'_{res}$ in MODE' is:

$$V'_{res} = V_{in} \cdot \sum_{k=1}^{n} W_{1k} - V_{ref} \cdot \sum_{k=1}^{n} d_k W_{1k}$$  

Similarly, a complementary operation pattern to MODE', denoted by MODE'', is available when the roles $C_{1k}$ and $C_{2k}$ are interchanged, and the quantization residue $V''_{res}$ is derived correspondingly:

$$V''_{res} = V_{in} \cdot \sum_{k=1}^{n} W_{2k} - V_{ref} \cdot \sum_{k=1}^{n} d_k W_{2k}, \quad W_{2k} = \frac{C_{2k}}{\sum_{j=1}^{n} (C_{1j} + C_{2j})}$$

where $W_{2k}$ is the weight of $C_{2k}$.

When evenly capacitor splitting is perfectly achieved, we will have $C_{1k} = C_{2k} = C_k/2$, $W_{1k} = W_{2k} = W_k/2$, and $V'_{res} = V''_{res} = V_{res}/2$, thus either MODE' or MODE'', together with the normal operation in Fig. 3, could
be employed to extract the information of nonlinear error \( e \), as suggested in Eq. (2). In practice, the inevitable capacitor mismatches require that both MODE and MODE" be used to obtain an approximation of \( g(f(V_{\text{res}}/2)) \).

From Eq. (4), Eq. (6) and Eq. (7), with notice that \( W_k = W_{1k} + W_{2k} \), it can be derived that \( V'_{\text{res}} + V''_{\text{res}} = V_{\text{res}} \), assuming \( V'_{\text{res}} = V_{\text{res}}/2 - \delta \), and \( V''_{\text{res}} = V_{\text{res}}/2 + \delta \), we have:

\[
g(f(V'_{\text{res}})) + g(f(V''_{\text{res}})) = g(f(V_{\text{res}}/2 - \delta)) + g(f(V_{\text{res}}/2 + \delta))
\approx g(f(V_{\text{res}}/2)) - [g(f(x))]_{x=\frac{V_{\text{res}}}{2}} \cdot \delta + g(f(V_{\text{res}}/2)) + [g(f(x))]_{x=\frac{V_{\text{res}}}{2}} \cdot \delta
= 2g(f(V_{\text{res}}/2))
\]

The approximation in Eq. (8) is quite precise since both \( V'_{\text{res}} \) and \( V''_{\text{res}} \) are very close to \( V_{\text{res}}/2 \) given the degree of capacitor matching in modern fabrication processes, and thus \( \delta \) is small enough for the higher order terms to be ignored, therefore, Eq. (2) can be replaced by a more practical form:

\[
e = g(f(V'_{\text{res}})) + g(f(V''_{\text{res}})) - g(f(V_{\text{res}})) = D'_{\text{res}} + D''_{\text{res}} - D_{\text{res}} = 0
\]

where \( D'_{\text{res}}, D''_{\text{res}}, \) and \( D_{\text{res}} \) are the corrected digital outputs of the back-end ADC when the stage operates in MODE', MODE'', and normal operation, respectively.

![Fig. 5. Estimation of nonlinearity error using boundary values of \( D_{\text{res}} \)](image)

In real applications, no deterministic \( D_{\text{res}} \) levels can be expected or the algorithm will suffer from input signal dependency, therefore, some statistical
quantity of Dres should be employed instead. Two such quantities are directly available, the average and the boundary, wherein the later is preferable for fast convergence and low computational complexity. As long as the stage input V_in falls into one of the sub-ranges defined by neighboring comparator thresholds in the sub-ADC, its distribution in this certain sub-range must have either a highest boundary V_in+|max that generates the maximum values of positive Dres, Δres+, and D''res (denoted as Dres+, Δres+, and D''res+), as illustrated in Fig. 5, or a lowest boundary V_in−|min that generates the minimum values of negative Dres, Δres−, and D''res (denoted as Dres−, Δres−, and D''res−), or both, because of monotonicity. Since Dres+, Δres+, and D''res+ are all generated at the same input level with the same sub-ADC output code d1~d_n, they are appropriate to replace the variables in Eq. (9) in estimation of the nonlinear error. We use \( \hat{e}_+ = \hat{\Delta}_{res+}|_{max} + \hat{\Delta}'_{res+}|_{max} - \hat{\Delta}_{res+}|_{max} \) to denote the estimation of e by collecting a large number of digitized residues in all the three operation modes and selecting the maxima from the positive ones, similarly, \( \hat{e}_- = -(\hat{\Delta}_{res-}|_{min} + \hat{\Delta}'_{res-}|_{min} - \hat{\Delta}_{res-}|_{min}) \) is achieved by selecting minima from the negative ones. In notice that the fidelity of statistical boundary estimation is dependent on the size of the sample space, it is natural to combine \( \hat{e}_+ \) and \( \hat{e}_- \) according to the number of samples collected to estimate them, as formulated below:

\[
\hat{\epsilon} = \frac{N_+}{N} \hat{e}_+ + \frac{N_-}{N} \hat{e}_- \tag{10}
\]

where \( N_+ \) and \( N_- \) are the number of positive and negative digitized residues when V_in falls in this certain sub-range, and N is the total number of samples collected.

Apparently, different \( \hat{\epsilon} \) could be generated from each sub-range of the pipeline stage, so this proposed technique choose to use the sum of them as a combined indicator of nonlinear error in the inter-stage amplifier. For example, in a 3 bit pipeline stage with its output code (in binary) from 000~111, we define the combined indicator \( \hat{\epsilon}_{comb} \) as:

\[
\hat{\epsilon}_{comb} = \sum_{k=000}^{111} \hat{\epsilon}_k \tag{11}
\]

where k identifies the sub-range each \( \hat{\epsilon} \) is generated. \( \hat{\epsilon}_{comb} \) is then used to update the nonlinearity calibration parameter b3 by iteration (b1 is set to unity in the linearization process), where \( \mu \) is the update step:

\[
b_3[k+1] = b_3[k] + \mu \cdot \hat{\epsilon}_{comb} \tag{12}
\]

Note that no matter how V_in is distributed, \( \hat{\epsilon}_{comb} \) always extracts sufficient information from large number of samples, and the weighted sum prevents the estimation from the influence of any isolated samples; even if V_res has only a small magnitude around zero, the slow convergence doesn’t cause problem to the overall performance because in this case little harmonic distortion is created by the nonlinear function f(x). It is therefore reasonable to state that this proposed nonlinear error estimation has little dependence on input signal distributions.
Once $g(f(x))$ converges to a linear function: $g(f(x)) = A \cdot x$, the weight of each unit capacitor $C_{1k}$ and $C_{2k}$ could be readily measured with a linear gain $A (\approx a_1$ when nonlinearity is weak), by various well developed methods [3, 6], but it is suggested that this process be done in foreground and the ratio of capacitor units be stored in memory so that the weight of only one capacitor needs to be measured during normal operation to track the gain drift and determine the linear gain calibration parameter $b_1$ (or $1/A$). In this way, two restoration ratios are obtained to recover the digitized residues in MODE’ and MODE” to its original scale:

$$R' = 1/ \sum_{k=1}^{n} W_{1k}$$

$$R'' = 1/ \sum_{k=1}^{n} W_{2k}$$

Fig. 6 shows the complete calibration flow diagram, the proposed technique described above takes charge of inter-stage residue amplifier nonlinearity correction, and is compatible with the offset measurement (by chopping for example) and linear gain correction (such as capacitor dithering) methods reported previously.

**4 Simulation results**

Behavioral model of a 16bit pipelined ADC is scripted and simulated with Matlab to evaluate the proposed calibration technique. The model is configured as follows:

Stage1 resolves 3bit in a scale of $2V_{pp}$, with 1 full bit as redundancy, the subsequent stages form an ideal 14bit back-end ADC. Based on circuit simulations in 0.18 µm CMOS, the open-loop residue amplifier is modeled by $f(x) = 3.88x - 5.6x^3 - 14.6x^5 + 36.5x^7$, corresponding to about 10.3% gain.
compression at full scale (input range: $-0.25 \text{V} \sim 0.25 \text{V}$), as depicted in Fig. 7, and up to 1% capacitor mismatch is assumed among $C_{1k}$ and $C_{2k}$, as listed in Table I.

Fig. 8(a) shows the convergence of parameter $b_3$ (with initial value 0) in the nonlinearity calibration process with full scale sinusoidal input (coherent sampling was avoided intentionally) when $\mu$ is set at 1. Each $2^{16}$ samples are collected to estimate $D'_{\text{res}}|_{\text{max}}$, $D''_{\text{res}}|_{\text{max}}$, $D_{\text{res}}|_{\text{max}}$, and $D'_{\text{res}}|_{\text{min}}$, $D''_{\text{res}}|_{\text{min}}$, $D_{\text{res}}|_{\text{min}}$ in each sub-range, when both $\text{MODE'}$ and $\text{MODE''}$ appear with probability of 20%.

Fig. 8(b) shows the corresponding dynamic performances variations, the ADC reaches about 15bit ENOB after about $4 \times 10^6$ conversion steps. Quantization spectra with and without the nonlinearity calibration are compared in Fig. 8(c).

It has to be stated that Fig. 8 demonstrates only the effect of nonlinearity calibration, which is one of the three consecutive phases in the background calibration cycle, as shown in the right half part of Fig. 7. In order to manifest the effect more clearly, $b_3$ was intentionally set to 0 before the nonlinearity calibration phase, although in reality its initial value should be the result in the last round, probably much closer to its final convergence.
Fig. 8. Simulation results of the 16bit prototype pipelined ADC

(a) convergence of $b_3$

(b) dynamic performance variations with full-scale sinusoidal input

(c) quantization spectra before and after nonlinearity calibration

**Fig. 8.** Simulation results of the 16bit prototype pipelined ADC

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**Table II.** Performance conclusions

| Reference                              | [1] | [2] | [3] | [4] | Proposed technique |
|---------------------------------------|-----|-----|-----|-----|-------------------|
| Gain compression at full swing (%)    | 0.5 | 1.2 | 5   | 3.2 | 10.3              |
| Convergence time for $b_3$ ($\times 10^8$ conversion) | 3   | 0.01| 0.04| 43  | 0.04              |
| SFDR after Cali. (dBc)                | 105 | 92  | 112 | 88  | 104.8             |
A summary and comparison on the features of different nonlinearity calibration techniques is given in Table II, the proposed technique surpasses the other works in correction range, with calibration speed and effectiveness among the best.

5 Conclusions

A digital background calibration technique for pipelined ADCs is described in this paper. It is shown that by employing the proportional scaling criterion in algorithm and sampling capacitors splitting in circuit implementation, the nonlinear error in inter-stage residue amplifiers can be directly measured and effectively corrected regardless of the input distributions, with a very short convergence time.