Robust Design of Differential Amplifier with Diode-connected Voltage Reference

Swapnil Sourav*, Rishab Mehra and Aminul Islam
Department of Electronics and Communication Engineering, Birla Institute of Technology (Deemed University), Mesra, Ranchi, Jharkhand – 835215, India; meec1003214@bitmesra.ac.in, rishabmehra03@gmail.com, aminulislam@bitmesra.ac.in

Abstract

Objectives: The impact of process, voltage and temperature (PVT) variations on the voltage gain of a CMOS differential amplifier is investigated. Methods and analysis: Appropriate biasing is provided using diode-connected MOS voltage dividers. These dividers are less bulky as compared to their resistive counterparts, save chip area and provide better performance when subjected to variations. In addition, the transistors are sized suitably to minimize the effect of threshold voltage modulation in short-channel devices. Findings: The sensitivity parameters for the voltage gain are modeled and their dependences are studied. All simulation results have been performed using Virtuoso Analog Design Environment of Cadence @ 45-nm technology node. Application/Improvement: Diode-connected MOS voltage dividers are used to bias the amplifier which provide immunity against PVT variations and hence improve system performance.

Keywords: Aspect Ratio, Differential, Gain, MOS Divider, Saturation, Sensitivity, Variability,

1. Introduction

Process, Voltage and Temperature (PVT) variations are one of the major obstacles in the design of reliable and robust analog circuits. This is primarily due to the aggressive scaling of semiconductor devices to the nanometer regime, which has made the reliability and controllability of the fabrication process quite low.

A number of strategies have been reported in literature to overcome the above issues, which include design of robust biasing circuits and current sources. A novel biasing technique for CMOS radio frequency power amplifiers has been proposed in\(^1\), which provides resilience through the threshold voltage adjustment without degradation in the performance. A similar study is carried out in\(^2\) which holds variation in \(V_{th}\) responsible for variability in the gain of standard amplifier topologies where transconductance determines the voltage gain and recommends a compensation scheme for an inductively degenerated cascode LNA. A compensation circuit for LNA and mixers is reported in\(^3\) which reduces the variability in device performance metrics by adapting to the temperature and process variations and generating an appropriate bias voltage accordingly. Another current source topology in reported in\(^4\) which consists of a ring based connection of odd number of inverters and additional transistors and can be used for biasing inverter chains and other integrated circuits. Various post-fabrication methodologies have also been adopted in\(^5\) which increase the verification costs and complexity. Apart from this, subthreshold operation of analog CMOS circuits is examined in\(^6\) and\(^7\) and various issues such as gate leakage, scaling of conventional transistor characteristics, body biasing etc. have been looked upon.

Several analysis and studies of different analog and digital integrated circuits have also been reported which help in better understanding of PVT variations and lay down the guidelines to reduce their impact. In\(^5\), the impact of the intrinsic-parameter fluctuations such as metal-gate Work-Function Fluctuation (WKF) and Random-Dopant Fluctuation (RDF) etc. is estimated for MOS circuits. Further, the static, dynamic and short-circuit power

*Author for correspondence
dissipations are looked upon. A similar study involving the impact of process mismatch on the performance of domino and static 1-bit full adders is presented in [9]. However, a thorough robustness study and sensitivity analysis of a CMOS differential amplifier has not been carried out before. This paper proposes a differential amplifier with appropriate transistor sizing/biasing for enhancing robustness of its design metrics and performs robustness/sensitivity study/analysis. Appropriate transistor sizing to curb impact of PVT variations is a critical piece of our design strategy.

The rest of the paper is organized as follows. Section 2 describes the simulation setup used. In Section 3, the dependence of threshold voltage ($V_{th}$) on transistor aspect ratios is studied and optimum channel lengths and widths are selected. The behavior of differential gain of the differential amplifier when subjected to process, voltage and temperature variations is described in Section 4, 5 and 6 respectively and sensitivity parameters are determined. Finally, the concluding remarks are provided in section 7.

2. Simulation Setup

The differential amplifier Figure 1 is one of the most versatile circuits used in analog design and forms the input stage of most operational amplifiers. The transistors are biased in saturation and the output DC voltage level is kept at $V_{DD}/2$ so as to provide maximum room to swing the amplified output signal. Diode-connected MOS dividers are used to provide the appropriate gate bias to the amplifying transistors. This biasing scheme provides robustness to the amplifier as compared to its resistor-only and resistor-MOS counter parts along with lower sensitivity to temperature variations [10]. Also, transistors are sized such that minimum variation in threshold voltage $V_{th}$ is observed. The bias voltage can be determined by equating the current in the two MOSFETs. Since a diode-connected MOSFET always operates in the saturation region for gate bias above threshold voltage, the beta ratio for the two transistors can be calculated if the $V_{ref}$ is known i.e.

$$\frac{\beta_N}{\beta_P} = \left(\frac{V_{DD} - V_{tp}}{V_{ls} - V_{tp}}\right)^2$$

$$\frac{V_{ref} - \sqrt{\frac{\beta_N}{\beta_P}} (V_{th})}{\sqrt{\frac{\beta_N}{\beta_P} + 1}} = V_{DD} - V_{tp} + \sqrt{\frac{\beta_N}{\beta_P}} (V_{th})$$

The threshold voltage $V_{th}$ is affected by process variations and decreases with decrease in the channel length ($L$) and channel width ($W$) due to short-channel effects [11]. However, the impact of variation of channel length on threshold voltage is more pronounced as compared to that of channel width. To study the above, an NMOS transistor was biased in saturation in such a way that $V_{DD}/2$ and the impact of its channel length on $V_{th}$ were analyzed. The results obtained are shown in Figure 2, it is observed that $V_{th}$ becomes more or less constant after 180 nm (3.5 times 45 nm) making it suitable for circuit design. Hence, considering the above and required bias voltages the transistors are sized. Dimensions of all the MOSFETs used in figure 1 are tabulated in Table 1.

Body of all the NMOSFETs are connected to GND and body of all the PMOSFETs are connected to VDD.

3. Sizing Ratio Selection

The threshold voltage $V_{th}$ is affected by process variations and decreases with decrease in the channel length ($L$) and channel width ($W$) due to short-channel effects [11]. However, the impact of variation of channel length on threshold voltage is more pronounced as compared to that of channel width. To study the above, an NMOS transistor was biased in saturation in such a way that $V_{DD}/2$ and the impact of its channel length on $V_{th}$ were analyzed. The results obtained are shown in Figure 2, it is observed that $V_{th}$ becomes more or less constant after 180 nm (3.5 times 45 nm) making it suitable for circuit design. Hence, considering the above and required bias voltages the transistors are sized. Dimensions of all the MOSFETs used in figure 1 are tabulated in Table 1.
is the slope of the $I_D - V_{GS}$ characteristics at the bias point and is defined in the saturation region as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{OX} \frac{W}{L} V_{OV} \left(1 + \lambda V_{DS} \right)$$

(6)

where, $\mu_n$, $C_{OX}$, $W$ and $V_{OV}$ are mobility, oxide capacitance, channel length, channel width and overdrive voltage respectively. $V_{DS}$ is the drain-to-source bias voltage. From (4), the gain can be represented as

$$A_V = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left( \frac{K_{MN1} W_{MN1}}{I_{SS} L_{MN1}} \right)^{1/2}$$

(7)

where, $I_{SS}$ is the DC bias current through $MN3$ and is the sum of the DC currents through $MN1$ and $MN2$ respectively i.e.

$$I_{SS} = I_{D(MN1)} + I_{D(MN2)}$$

(8)

The sensitivity of open circuit voltage gain ($A_V$) of an amplifier with respect to any parameter $p$ can be modeled as

$$S_p^{A_V} = \frac{\partial A_V}{\partial p} A_V$$

(9)

4. Impact of Process Variations on Differential Gain

The open circuit voltage gain ($A_V$) of the differential amplifier is defined as

$$A_V = g_m(MN2) \left( r_o(MN2) || r_o(MP2) \right)$$

(4)

where, $r_o$ is the output resistance used to model the channel length modulation and is defined by

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{\lambda I_D}.$$ 

(5)

Figure 2. Variation of threshold voltage with channel length.

Table 1. Dimensions of MOSFETs used in Figure 1

| Transistor | Channel Length (L) | Channel Width (W) | Threshold Voltage ($V_{th}$) |
|------------|--------------------|-------------------|-----------------------------|
| MN1, MN2  | 180 nm             | 2.7 µm            | 481.65 mV                   |
| MP1, MP2  | 180 nm             | 950 nm            | -417.46 mV                  |
| MN3       | 180 nm             | 2.7 µm            | 469.45 mV                   |

A small voltage is developed at the source-coupled node X, $V_{BS}$ of MN1 and MN2 are negative and hence their threshold voltages are higher due to body effect. However, the $V_{BS}$ of MN3 is zero and hence its threshold voltage is lower compared to those of MN1 and MN2.

4.1 Sensitivity to Length of Inverting Transistor

The sensitivity of gain $A_V$ to the channel length of the inverting transistor ($L_{MN2}$) can be defined as

$$S_{L_{MN2}}^{A_V} = \frac{\partial A_V}{\partial L_{MN2}} A_V.$$ 

(10)

From (7), the above can be expressed as

$$S_{L_{MN2}}^{A_V} = -\frac{A_V}{2I_{SS}} \frac{\partial I_{SS}}{\partial L_{MN2}} \frac{L_{MN2}}{A_V}.$$ 

(11)

which is equivalent to

$$S_{L_{MN2}}^{A_V} = -\frac{L_{MN2}}{2I_{SS}} \frac{K_{MN2} W_{MN2}}{I_{SS} L_{MN2}} \left( \frac{\partial V_{th}}{\partial L_{MN2}} \left( V_{(MN2)} - V_{th} \right) \right).$$ 

(12)

Considering the change in threshold voltage to be negligibly small due to appropriate sizing of transistors, from figure 2.
4.3 Sensitivity to Width of Inverting Transistor

Partially differentiating (7) with respect to $W_{MN2}$ and substituting in (11),

$$S_{W_{MN2}}^{A_v} = -\frac{A_v}{2I_{ss}} \frac{\partial I_{ss}}{\partial W_{MN2}} \frac{W_{MN2}}{A_v}$$

which is equivalent to

$$S_{W_{MN2}}^{A_v} = -\frac{W_{MN2}}{2I_{ss}} \frac{K_{MN2}}{L_{MN2}} \left( V_{GS(MN2)} - V_{th} \right) \frac{\partial V_{th}}{\partial W_{MN2}}$$

Similarly, assuming the variation in threshold voltage $V_{th}$ due to change in $W_{MN2}$ to be negligibly small i.e.

$$\frac{\partial V_{th}}{\partial W_{MN2}} = 0$$

and hence, simplifying (19) to

$$S_{W_{MN2}}^{A_v} = -\frac{W_{MN2}}{2I_{ss}} \frac{K_{MN2}}{L_{MN2}} \left( V_{GS(MN2)} - V_{th} \right)$$

4.4 Sensitivity to Width of Non-inverting Transistor

The sensitivity of $A_v$ to channel width $W_{MN1}$ of non-inverting transistor can be modeled as

$$S_{W_{MN1}}^{A_v} = \frac{W_{MN1}^2}{2I_{ss}} \left( I_{ss} - \frac{\partial I_{ss}}{\partial W_{MN1}} \right)$$

where,

$$\frac{\partial I_{ss}}{\partial W_{MN1}} = \frac{K_{MN1}}{L_{MN1}} \left( V_{GS(MN1)} - V_{th} \right)$$

Figure 3. Variation of gain and rail-to-rail swing with channel length of inverting and non-inverting transistor of differential pair gives

5. Impact of Supply Variations on Differential Gain

The impact of supply variations is studied for the DC bias current $I_{dc}$ as well as the supply voltage $V_{DD}$ and the sensitivity parameters are determined.
In case of the DC bias current, the current $I_{DC}$ flowing through MN3 consists of only the DC component whereas the AC current due to the input excitation flows to the output load. Hence, the expression for $A_V$ from (7) can be written as

$$A_V = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left[ \frac{K^*_{MN1} W_{MN1}}{2 I_{DC} L_{MN1}} \right]^2. \quad (24)$$

As seen from (24), $A_V$ exhibits a negative dependence on $I_{DC}$ and hence decreases with increase in the bias current which can be verified from Figure 5. The sensitivity parameter for this case can be determined as

$$S_{A_V}^{I_{DC}} = \frac{\partial A_V}{\partial I_{DC}} \frac{I_{DC}}{A_V}$$

where

$$\frac{\partial A_V}{\partial I_{DC}} = -\frac{A_V}{2 I_{DC}}. \quad (26)$$

Substituting the above in (25) gives

$$S_{A_V}^{I_{DC}} = -\frac{1}{2}. \quad (27)$$

A similar analysis is done for the variation in supply voltage $V_{DD}$ which is varied by 10% around the nominal value. The results are depicted in Figure 6. As can be seen, both the open circuit voltage gain $A_V$ and the output swing exhibit a positive dependence on $V_{DD}$ i.e. they increase with increase in the supply voltage.

6. Impact of Temperature Variations on Gain

The temperature dependence of $A_V$ is primarily due to variation in mobility ($\mu$) and threshold voltage ($V_{th}$) which can be modeled using the following

$$\mu(T) = \mu(T_o) \left( \frac{T_o}{T} \right)^m$$

and

$$V_{th}(T) = V_{th}(T_o) - K(T - T_o)$$

where, $T_o$ is the reference temperature (300 K), $K$ is the threshold voltage temperature coefficient whose typical value is 2.5 mV/K and $m$ is the mobility temperature exponent whose typical value is 1.5 (ideally 1).
Differentiating (28) and (29) with respect to temperature,

$$\frac{\partial V_{th}}{\partial T} = -K$$ \hspace{1cm} (30)

$$\frac{\partial \mu}{\partial T} = -\frac{m\mu(T)}{T}. \hspace{1cm} (31)$$

From (30) and (31) it can be seen that both mobility and threshold voltage show a negative dependence on temperature. Since the NMOS transistors of the differential pair are considered to be matched, the DC bias current through them can be assumed to be identical. Hence, \(I_{SS}\) can be approximated to be twice the current through MN1 i.e.

$$I_{SS} \approx 2I_{D(MN1)}.$$ \hspace{1cm} (32)

Using the above result and (24),

$$A_v = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left[ \frac{\mu_n C_w W_{MN1}}{L_{MN1}} \right]^{\frac{1}{2}} (V_{ref} - V_{D(MN1)} - V_{th}). \hspace{1cm} (33)$$

On simplification, (33) reduces to

$$A_v = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left[ \frac{\mu_n C_w W_{MN1}}{L_{MN1}} \right]^{\frac{1}{2}} \left( V_{ref} - V_{D(MN1)} - V_{th} \right). \hspace{1cm} (34)$$

From (2),

$$V_{ref} - V_{th} = \frac{\sqrt{2N}}{\sqrt{N} + 1} \left( V_{DD} - |V_{tp}| - V_{th} \right) \hspace{1cm} (35)$$

which is equivalent to

$$V_{ref} - V_{th} = V_{DD} - |V_{tp}| - V_{th}.$$ \hspace{1cm} (36)

Substituting the above in (34)

$$A_v = \frac{2}{\lambda_{MN2} + \lambda_{MP2}} \left[ \frac{\mu_n C_w W_{MN1}}{L_{MN1}} \right]^{\frac{1}{2}} \frac{1}{V_{DD} - |V_{tp}| - V_{th} - V_{D(MN1)}}. \hspace{1cm} (37)$$

Now, since the threshold voltage \(V_{th}\) and \(V_{tp}\) exhibit negative temperature dependence, the term \(V_{DD} - |V_{tp}| - V_{th}\) increases due to decrease in the threshold voltage val-
ues. Hence, the overall gain decreases with increase in temperature which can be verified from Figure 7.

The dependence of temperature on a parameter \(p\) can be demonstrated using a fractional temperature coefficient \((TC_p)\) defined as

$$TC_F(p) = \frac{1}{p} \left( \frac{\partial p}{\partial T} \right) = \frac{1}{T} S_T^p \hspace{1cm} (38)$$

where, \(T\) is the absolute temperature and \(S_T^p\) is the sensitivity parameter defined in (7). From (38),

$$TC_F(A_v) = \frac{1}{A_v} \frac{\partial A_v}{\partial T} = \frac{1}{T} S_T^{A_v}. \hspace{1cm} (39)$$

Differentiation of (37) with respect to \(T\) gives

$$\frac{\partial A_v}{\partial T} = -\frac{2A_v K}{\left( V_{DD} - |V_{tp}| - V_{th} - V_{D(MN1)} \right)^2} \left[ \frac{\partial V_{tp}}{\partial T} + \frac{\partial V_{th}}{\partial T} \right]. \hspace{1cm} (40)$$

which is identical to

$$\frac{\partial A_v}{\partial T} = -\frac{2A_v K}{\left( V_{DD} - |V_{tp}| - V_{th} - V_{D(MN1)} \right)^2} \left[ \frac{\partial V_{tp}}{\partial T} + \frac{\partial V_{th}}{\partial T} \right]. \hspace{1cm} (41)$$

Using (30),

$$\frac{\partial A_v}{\partial T} = -\frac{2A_v K}{\left( V_{DD} - |V_{tp}| - V_{th} - V_{D(MN1)} \right)^2} \left[ \frac{\partial V_{tp}}{\partial T} + \frac{\partial V_{th}}{\partial T} \right]. \hspace{1cm} (42)$$

where, \(K\) is the threshold voltage temperature coefficient defined in (29).

Figure 7. Dependence of gain \(A_v\) on temperature.
Hence, it can be verified from (42) that $A_v$ exhibits a negative dependence on temperature. Finally, the fractional temperature coefficient $TC_{F}$ can be obtained as

$$
TC_{F}(A_v) = -\frac{2K}{(V_{DD} - |V_p| - V_{th} - V_{D(MN1)})}.
$$

(43)

and sensitivity parameter $S$ as

$$
S_{T}A_v = -\frac{2TK}{(V_{DD} - |V_p| - V_{th} - V_{D(MN1)})}.
$$

(42)

7. Conclusions

This paper proposes a differential amplifier with appropriate transistor sizing/biasing for enhancing robustness of its design metrics. The impact of PVT variations on the differential gain of the proposed amplifier is analyzed. Sensitivity of gain to the PVT variations is demonstrated by deriving suitable sensitivity parameters and fractional temperature coefficient.

8. References

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