An $n$-bit general implementation of Shor’s quantum period-finding algorithm

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The goal of this paper is to outline a general-purpose scalable implementation of Shor’s period-finding algorithm using fundamental quantum gates, and to act as a blueprint for linear optical implementations of Shor’s algorithm for both general and specific values of $N$. This offers a broader view of a problem often overlooked in favour of compiled versions of the algorithm.
I. INTRODUCTION

The superiority of quantum computers over classical computers for problems with solutions based on quantum Fourier transform, as well as database search and quantum simulations continue to attract attention. There are many approaches proposed for building scalable quantum computers or achieving long-distance and high data-rate quantum communications. Major model physical systems include nuclear magnetic resonance, ion trap, neutral atom, cavity QED, solid state, superconducting, and optical approaches. All of these have their own advantages, but unfortunately, also their own drawbacks. None of them on its own is shown to be self-sufficient to build a large-scale practical quantum computer or quantum networks.

Quantum photonic integrated circuits, based on semiconductor technology and compatibility with existing microelectronics infrastructure, have been recently envisioned as the route to utilisable quantum information technologies enabling robust and compact quantum circuit boards and processors of the next generation computers and networking devices [1–7]. However, thousands of stable, interconnected interferometers with low-loss and high performance components are unavoidable for the implementation of practical large-scale quantum algorithms, since quantum error correcting codes are not very helpful at that large scale [2, 6]. Therefore, bulky optical experiments with only several photons have already started to move toward stable, miniaturized integrated quantum circuits with many logic gates like at the heart of classical computers [1, 2, 6, 7].

Silica-on-silicon waveguides [8–14], silicon-on-insulator waveguides [15–18], GaN-on-sapphire waveguides [19], direct laser writing [10, 14, 20–25], and standard lithography techniques [8, 9, 12, 13, 19] were chosen as underlying technologies for the implementations of quantum photonic integrated circuits. Non-classical interference of photon pairs in integrated optical circuits using a phase controlled Mach-Zehnder interferometer [10], directional coupler [8, 15], and integrated two-four-wave mixing waveguide sources in a phase controlled interferometer [17] was shown. In 2008, Politi, et al. [8] demonstrated integrated optical controlled-NOT gate and path-entanglement. The group later implemented Shor’s quantum algorithm on a photonic chip to factorize 15 [9], heralded path-entangled NOON states up to four photons for high precision quantum metrology [11], reconfigurable photonic circuits for the generation and manipulation of entangled states [12, 18, 26], and manipulation of externally generated single photons [13]. Sansoni, et al. [21] reported the realization of a directional coupler functioning as a beam splitter for polarization qubits. This work was then extended to demonstrate the first integrated photonic controlled-NOT gate for polarization qubits [22]. Corrielli, et al. showed the capability of performing arbitrary transformations on polarization qubits in an integrated waveguide circuit [22]. Implementations of quantum walk using integrated photonic waveguides were proposed for potential applications in quantum simulations [20, 23]. Single photon detectors with 20% efficiency [27] and photon-number-resolving detectors with 24% efficiency [22] using superconducting nanowires on GaAs ridge waveguides and single-mode waveguide photon-number-resolving detector with 40% efficiency [14] were shown at telecom wavelengths for photonic quantum circuits. Najafi, et al. [29] demonstrated on-chip detection of externally generated entangled photons by integrating multiple superconducting nanowire single photon detectors. Mower and Englund proposed a theoretical protocol for on-demand generation of single and entangled photons on a silicon photonic integrated chip using a time-multiplexed spontaneous parametric down conversion element [30]. In 2013, Spring, et al. showed the first single photon source on a silica photonic chip based on spontaneous four wave mixing with a heralding efficiency of 40% [24]. Spatial multiplexing of heralded single photon sources on monolithic silicon chip using spontaneous four wave mixing in photonic crystal waveguides was proposed to increase the heralded photon rate [10]. Matsuda, et al. [31] reported generation and demultiplexing of photon pairs on a silicon-silica monolithic waveguide platform. Based on type II-phase
matched spontaneous parametric down-conversion processes, experimental polarization entangled post-selection free photon source \cite{32} and theoretical hyperentangled photon pair generation \cite{33} were shown. Takesue, et al. \cite{34} reported an on-chip single-photon buffering for 150ps based on coupled resonator optical waveguides consisting of high-Q photonic crystal cavities. Mouradian, et al. \cite{35} demonstrated quantum memories with 120µs spin coherence times based on nitrogen-vacancy centers in a photonic circuit. Metcalf, et al. \cite{36} have very recently reported the first experimental demonstration of quantum teleportation on a reconfigurable integrated photonic chip which performs entanglement preparation, Bell-state analysis, and quantum state tomography, similar to the quantum photonic crystal integrated circuits that we envisioned in 2007 \cite{3, 4}. Li, et al. \cite{37} have proposed an experimental calibration method for quantum photonic integrated circuits that are becoming increasingly complex. Tezak, et al. \cite{38} proposed a quantum hardware description language to facilitate the analysis, design, and simulation of complex photonic circuits.

Despite all the promising developments above in theory and experiments, desired level of progress in realization of quantum circuits and algorithms has not been yet achieved. It is essential to explore large-scale integration of high quality single and entangled photon sources on demand, long-lived quantum memories, high-efficiency single photon detectors, reconfigurable implementations of quantum logic gates and protocols.

Here, we construct a general implementation of Shor's algorithm for any appropriate n-bit number using quantum logic gates, which can then be easily translated into quantum photonic integrated circuits based on directional couplers, interferometers, single-photon sources, detectors, and other integrated optical devices. This general representation of Shor's algorithm, as a model, in the physical layer can provide a simple recipe for both experimentalists and theorists toward large-scale practical implementations and help foresee the technological and fundamental limits of photonic integrated circuit approach to determine and focus on the most important experimental and theoretical requirements and aspects that are often overlooked.

Shor's quantum factorization algorithm provides a means to easily factor integers that are the product of two primes. Such numbers, and the difficulty of factorizing them, provide the basis of the common RSA encryption algorithm; a polynomial-time factorization method would greatly impact the effectiveness of this algorithm, with significant influence on the development of software, particularly when dealing with Internet security.

In section II, we introduce the basic design of Shor's period-finding quantum circuit and its component modules. In section III, we begin developing basic arithmetic operations on qubit registers; these are used in section IV to build low-level modular operations. Section V uses this block to build the operations necessary to perform modular arithmetic, while section VI details the use of these block to produce the modular exponentiation module needed by Shor's period-finding circuit. We conclude in section VII.

Unless otherwise stated, we assume that upper-case variables (\(A, B\)) are \(n\)-bit numbers stored in \(n + 1\)-bit registers (the top bit is always a 0, to have room for addition/multiplication by 2), and lower-case variables are single bits. A lower-case variable with a subscript indicates a specific bit of a number, indexed from zero; for example, \(a_2\) is the third bit of \(A\).

\section{II. SHOR'S FACTORIZATION ALGORITHM AND ITS QUANTUM CIRCUIT REPRESENTATION}

Shor's factorization algorithm contains both classical and quantum processes. The only section of the algorithm considered to be non-classical consists of a quantum circuit designed to find the period of a modular exponentiation function. This circuit can be further broken down into three
modules. The complete quantum circuit is depicted below, using three black boxes:

There are two numeric inputs to the circuit: \( N \), the number to be factored, and \( A \), some number coprime to \( N \) chosen in the classical portion of the algorithm. All of the qubit registers are \( n + 1 \)-bits, where \( n \) is the number of bits needed to represent \( N \); that is, \( n = \lfloor \log_2 N \rfloor + 1 \).

The first module is a Hadamard transform. Each qubit in the first register is subjected to a Hadamard gate. Since this register is initialized to zero, the first register is then in a superposition over all states. The number of gates required for this module scales linearly as the number of qubits increases.

The second module takes three values, \( N \), \( A \), and \( Y \), and returns \( A \% N \) where \( \% \) denotes the modulo operator. It also requires a number of ancillary qubits beyond those listed, on the order of \( n^2 \). Note that the \( A^2 \% N \) ancillary result comes only from known values and those from the classical portion of the process, and the 0 register and \( N \) registers do not change, so they can be reclaimed for other uses after the algorithm is finished.

The third module is an inverse quantum fourier transform, or inverse QFT. A general form for this component is well-known, and the number of gates scales quadratically with \( n \).

Current efforts at realizing Shor’s algorithm using photonic gates has focused on proof-of-concept methods for specific values, such as 15 [9] or 21[39]. While the first and third modules are well-known and easily constructed, the modular exponentiation algorithm is more difficult to construct for a general case. Many experimental attempts to realise Shor’s Algorithm rely on a version of this process optimised for specific constants, as in [40]. These “compiled” circuits, while useful for experimental purposes, are restricted to a small subset of \( A \) and \( N \) values, and often obfuscate the nature of the modular exponentiation component. We will focus on creating the modular exponentiation component for a general case from elementary gates in a way that is accessible to experimentalists.

### III. BASIC ARITHMETIC BLOCKS

#### A. CDKM Adder [+] 

The Cuccaro-Draper-Kutin-Moulton (CDKM) adder is a two’s complement reversible ripple-carry adder that uses no ancillary qubits (counting the carry bit as part of the output) [41]. It acts as the basis of many of the blocks we describe later, and itself consists of two blocks: majority and unmajority-and-sum. Several optimisations for the design have emerged [12], but we will be focused on the simplest implementation.
1. Majority \([\text{MAJ}]\)

The majority block computes \(c_i \oplus a_i, a_i \oplus b_i,\) and \(c_{i+1}\) from \(c_i, a_i,\) and \(b_i,\) where \(c_i\) is the \(i\)th carry value, \(a_i\) is the \(i\)th bit of \(A,\) and \(b_i\) is the \(i\)th bit of \(B.\) The majority block is implemented using elementary gates:

\[
\begin{array}{c}
\text{c}_i \\
\text{b}_i \\
\text{a}_i \\
\end{array}
\quad \begin{array}{c}
\text{c}_i \oplus \text{a}_i \\
\text{a}_i \oplus \text{b}_i \\
\text{c}_{i+1} \\
\end{array}
\]

2. Unmajority and Sum \([\text{UMS}]\)

The unmajority-and-sum block computes \(c_i, s_i,\) and \(a_i\) from \(c_i \oplus a_i, a_i \oplus b_i,\) and \(c_{i+1};\) that is, from the outputs of the corresponding majority block:

\[
\begin{array}{c}
\text{c}_i \oplus \text{a}_i \\
\text{a}_i \oplus \text{b}_i \\
\text{c}_{i+1} \\
\end{array}
\quad \begin{array}{c}
\text{c}_i \\
\text{s}_i \\
\text{a}_i \\
\end{array}
\]

[41] offers an alternative version of the UMS block; for ease of implementing the controlled adder, we have selected the simpler implementation.

3. The Complete Adder

A pair of these blocks is needed for each bit to be added; for example, a CDKM adder adding three bits of input would be

\[
\begin{array}{c}
\text{0} \\
\text{b}_0 \\
\text{a}_0 \\
\text{b}_1 \\
\text{a}_1 \\
\text{b}_2 \\
\text{a}_2 \\
\text{0} \\
\end{array}
\quad \begin{array}{c}
\text{MAJ} \\
\text{MAJ} \\
\text{MAJ} \\
\text{UMS} \\
\text{UMS} \\
\text{UMS} \\
\text{UMS} \\
\text{UMS} \\
\text{UMS} \\
\end{array}
\quad \begin{array}{c}
\text{0} \\
\text{s}_0 \\
\text{a}_0 \\
\text{s}_1 \\
\text{a}_1 \\
\text{s}_2 \\
\text{a}_2 \\
\text{c} \\
\end{array}
\]

where \(c\) denotes the carry bit of the sum. The carry bit is omitted in many of our uses of the CDKM adder; as one of the addends is preserved, no information is destroyed by not passing on a carry bit.
B. Controlled CDKM Adder \([+c]\)

A cursory examination of the MAJ and UMS blocks reveals the means to make a controlled CDKM adder: placing the blocks side-by-side gives

Consider the following modification:

If bit \(x\) is high, the gates behave as usual; otherwise, the Toffoli gates do nothing, leaving the central gates to cancel each other out. This disables a single pair of MAJ/UMJ blocks; hooking the control bit \(x\) to every other pair will similarly disable the entire adder \([40]\). Calling the modified blocks CMJ and CUS, the controlled CDKM adder is then

The output of this gate is

C. Alternative Addition Blocks

The CDKM adder presented above is the most intuitive implementation of a quantum adder, but it is not necessarily the best when used in an actual implementation. Each MAJ and UMS block
uses three quantum gates, which means $6n$ gates are needed for an $n$-bit adder, and each result relies on the previous to be computed, so result takes a long time to compute.

Thomsen and Axelsen\cite{42} offer an optimisation of the ripple-carry adder that divides a task of $ck$ bits into $c$ independent $k$-bit adders, which are then combined to give the result in a total of $O\left(ck\right)$ time. The Thomsen-Axelsen adder, while offering a substantial speedup over a $ck$-bit CDKM adder, uses substantially more gates: the hardware cost of the Thomsen-Axelsen adder is $O\left(n\sqrt{n}\right)$, while the CKDM adder is linear. The improvement in runtime is greater asymptotically than the increase in hardware cost, so substituting the Thomsen-Axelsen adder should for large $n$ offer an overall improvement, but the higher hardware cost could prove prohibitive for implementations where the expense of added hardware outweighs the need for fast calculations.

Draper, Kutin, Rains, and Svore\cite{43} propose a carry-lookahead adder which runs in $O\left(\log n\right)$ time, but requires $O\left(n\right)$ ancillary qubits. The additional qubit cost substantially increases the overhead qubits required for modular exponentiation.

Zalka uses parallelised addition in \cite{44} to achieve a reduction of depth of modular exponentiation from $n^3$ to $n^2$, while remaining in $O\left(n^3\right)$ gates and $O\left(n\right)$ qubits. We do not consider parallelisation of Shor’s algorithm extensively in this paper, as it complicates circuit design, but in a physical implementation the change to a parallel adder can be advantageous.

D. CDKM Subtractor

As it is simply a two’s-complement adder, it is simple to adapt a CDKM adder into a CDKM subtractor. The NOT gate is an inherently reversible operation; as we know our inputs will be $n$-bit positive integers, the last bit will always be 0, and thus there is no need for an ancillary carry bit to add 1. A reversible, $n + 1$-bit “add one” block for $n$-bit integers is simply a CDKM adder that substitutes 1 for $A$:

$$B \quad \begin{array}{c} + \end{array} \quad B + 1$$

This requires an entire additional $n + 1$-bit register, which is inefficient; however, we can note that the values of this register are constant across all implementations, and as such can determine the inputs of the $MAJ$ gates. The lowest-order bit has 1 added and a fixed initial carry of 0, giving

$$0 \quad \begin{array}{c} \oplus \end{array} \quad 1 \quad \begin{array}{c} \oplus \end{array} \quad 0$$

which is equivalent to

$$0 \quad \begin{array}{c} \oplus \end{array} \quad 1$$

$$b_0 \quad \begin{array}{c} \oplus \end{array} \quad \neg b_0$$

$$1 \quad \begin{array}{c} \oplus \end{array} \quad b_0$$
The subtract one block is similar, but with the other register initialised to -1 rather than 1. The number of gates cannot be reduced as easily as with the +1 gate, since all it does is replace CNOT with NOT in the MAJ block.

Combining these with an \( n + 1 \)-bit CDKM adder gives an \( n + 1 \)-bit CDKM subtractor:

\[
\begin{array}{c}
A \\
B
\end{array}
\begin{array}{c}
+1 \\
-1
\end{array}
\begin{array}{c}
A - B \\
B
\end{array}
\]

1. **Controlled CDKM Subtractor \([-c]\)**

Creating a controlled subtractor can be accomplished by modifying the regular subtractor: replace each of the components with a controlled equivalent. Controlled NOT is an elementary gate, while the +1 block can be replaced by an ordinary CDKM adder\(^{[41]}\):

\[
\begin{array}{c}
A \\
B
\end{array}
\begin{array}{c}
+ \\
\cdot
\end{array}
\begin{array}{c}
A - Bx \\
B
\end{array}
\]

Note that while the +1 block can be manipulated due to not assuming the value of the first bit, the -1 block must be changed into a controlled version directly.

E. **CDKM Greater-Equal Comparator \([\geq]\)**

To determine if \( a \geq N \), we introduce one more modification to the CDKM adder, the CDKM comparator. The comparator is similar to a subtractor, but replaces unmajority-and-sum blocks with simple unmajority (\([UMJ]\)) blocks, which are the exact opposite of majority blocks:

\[
\begin{array}{c}
c_i \oplus a_i \\
a_i \oplus b_i \\
c_i+1 \oplus a_i
\end{array}
\]

Replacing a CDKM adder’s UMS blocks with UMJ blocks changes the output so that it returns the original inputs and the carry bit only; the sum is not returned. We shall refer to this as the comparator base block, \([CMB]\).
In a subtractor, this will simply return $A$ and $-B$, and the carry qubit will be high if there was a carry from the subtraction:

![Circuit Diagram]

This carry will only be high if $B$ is strictly greater than $A$; it will be 0 if $B = A$. Thus, we want to know if $B + 1$ is strictly greater than $A$; if $B < A$, then $B + 1 \leq A$ and the carry qubit will be low, while if $B \geq A$, $B + 1 > A$ and the bit is high. Thus, by adding one last +1 block, we obtain the greater-equal form of the CDKM comparator:

![Circuit Diagram]

1. Other Comparator Implementations

It is possible to implement a faster, but more complex, comparator by modifying a Thomsen-Axelsen adder in a similar way to the modification of the CDKM adder, with the corresponding performance increases; simply replace the block unmajority and sum with block unmajority, and extract the maximum carry with a CNOT gate and an empty qubit.

F. Doubling Block [$\times 2$]

Our implementation of multiplication necessitates the ability to multiply the input $n$-bit numbers by two. Recall that all of the registers are $n + 1$-bit; as we know that $N$ is an $n$-bit number, $A$ cannot be more than $n$ bits. Thus, a simple series of swaps can be used to multiply $A$ by two. For instance, in the case where $n = 5$,

![Swap Diagram]

It should be simple to see how this can be generalised to an $n$-bit implementation.

G. Controlled Doubling Block [$\times 2_c$]

The controlled doubling block can be constructed simply by attaching all swaps to the control.
IV. RESTRICTED MODULO BLOCK [%]

Consider a modulo operation \( a \% N \) for the special case of \( 0 \leq a < 2N \). In this case, a single controlled subtraction is necessary in order to calculate the result: if \( a \geq N \), subtract \( N \) from \( a \); otherwise, return \( a \) as it is. This case proves sufficient for constructing the modular exponentiation block [40].

Using the ancillary qubit from a CDKM greater-equal comparator as the control bit in a controlled CDKM subtractor gives the desired modulo schematic:

\[
\begin{array}{c}
A \\
\geq C \\
B \\
\downarrow \\
A \% B \\
\end{array}
\begin{array}{c}
A \% B \\
B \\
\uparrow \\
A \geq B \\
\end{array}
\]

The modulus operation requires a single ancillary qubit, which will contain the value of \( A \geq B \).

V. SPECIFIC MODULAR CALCULATION BLOCKS

A. Modular Addition [+%]

This modulo operation only works for cases when \( 0 \leq A < 2N \); however, it will soon become apparent that only this case is necessary to perform modular exponentiation. First, consider the modular addition of two numbers \( A, B \in \mathbb{Z}_N \). By the definition of \( \mathbb{Z}_N \), \( 0 \leq A, B < N \). Thus, \( 0 \leq A + B < 2N \); as such, the modulus part of the operation can be performed by the simple modulo block above, giving the modular adder as

\[
\begin{array}{c}
A \\
B \\
\downarrow \\
A + B \% N \\
\end{array}
\begin{array}{c}
A + B \% N \\
N \\
\uparrow \\
A + B \geq N \\
\end{array}
\]

However, this block leaves an ancillary qubit to contain \( A + B \geq N \). As demonstrated in [42], it is possible to clear this bit, by using the fact that \( A + B \% N < B \) if and only if \( A + B \geq N \). Thus if we invert the ancilla when \( A + B \% N < B \), it is restored to zero. Recall now that our \( CMB \) block will invert a qubit if the second input is greater than the first; as below, it does so if \( B > A + B \% N \), which is what is needed to clear the ancilla.

\[
\begin{array}{c}
A \\
B \\
\downarrow \\
A + B \% N \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
B \% N \\
\end{array}
\begin{array}{c}
CMB \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
0 \\
\end{array}
\]

\[
\begin{array}{c}
A \\
B \\
\downarrow \\
A + B \% N \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
B \% N \\
\end{array}
\begin{array}{c}
CMB \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
0 \\
\end{array}
\]

\[
\begin{array}{c}
A \\
B \\
\downarrow \\
A + B \% N \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
B \% N \\
\end{array}
\begin{array}{c}
CMB \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
0 \\
\end{array}
\]

\[
\begin{array}{c}
A \\
B \\
\downarrow \\
A + B \% N \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
B \% N \\
\end{array}
\begin{array}{c}
CMB \\
\end{array}
\begin{array}{c}
A + B \% N \\
B \\
\uparrow \\
0 \\
\end{array}
\]
This gives us the modular addition block

\[
\begin{array}{ccc}
A & + & \% \\
B & & B \\
N & & N \\
0 & & 0 \\
\end{array}
\]

1. **Controlled Modular Addition \([+\%_C]\)**

Simply replace the addition block with a controlled addition block. When the control is off, the addition block is disabled; as we know that \(A < N\), the modular block will not do anything with the addition block disabled.

B. **Modular Doubling \([\times 2\%]\)**

The other important operation to perform is a specific, simpler case of modular addition: the modular multiplication of \(0 \leq A < N\) by 2. Similarly to the above, we know that \(0 \leq 2A < 2N\), and the modulus can be taken by the simple modulo block. Thus, we can achieve the naive modular doubling operation by means of the doubling block constructed earlier and the naive implementation of the modular adder above:

\[
\begin{array}{ccc}
A & \times 2 & - \% 2A%N \\
N & \% & N \\
0 & -2A & \geq N \\
\end{array}
\]

Unlike the above case, we cannot eliminate the ancillary bit through algebra. Specifying \(2A%N\) and \(N\) is not sufficient to find \(A\) even if we know \(A < N\); as one counterexample, \(N = 4\) and \(2A%N = 2\) yields \(A \in \{1, 3\}\), but no specific value. Thus, it is necessary in the most general case, where the inputs are not known classically, to have an ancillary bit containing \(2A \geq N\). In the case that \(A\) and \(N\) are known classically, it is a simple matter to clear this bit; it will be shown later that we will be able to do so.

1. **Controlled Modular Doubling \([\times 2\%_C]\)**

Simply replace the \([\times 2]\) block with its controlled counterpart; as \(A < N\) the modulo gate will not do anything once the multiplier is disabled.
C. Modular Multiplication $[\times \%]$

Using the $+\%$ and $\times 2\%$ blocks, we can construct a block that takes $A, B, N$, and returns $A + B \% N, 2B \% N, N$, as well as two ancillary bits which will contain 0 and $2B \geq N$:

\[
\begin{array}{c}
A \\
B \\
N \\
0 \\
0
\end{array} \quad \begin{array}{c}
A + B \% N \\
2B \% N \\
N \\
0 \\
0
\end{array} \quad \begin{array}{c}
+\% \\
\times 2\%
\end{array} \\
2B \geq N
\]

Making the adder in the $A + B \% N$ block controlled allows this block to perform a controlled addition of two numbers alongside the doubling:

\[
\begin{array}{c}
A \\
B \\
N \\
0 \\
x
\end{array} \quad \begin{array}{c}
A + xB \% N \\
2B \% N \\
N \\
0 \\
0
\end{array} \quad \begin{array}{c}
+\% \\
\times 2\%
\end{array} \\
2B \geq N
\]

Consider lining up $n$ of these blocks up, indexed 0 to $n - 1$, such that the $k$th block would have the inputs and outputs

\[
\begin{array}{c}
S_k \\
2^k A \% N \\
N \\
0 \\
x_k
\end{array} \quad \begin{array}{c}
S_{k+1} = S_k + 2^k x \% A \% N \\
2^{k+1} A \% N \\
N \\
0 \\
0
\end{array} \quad \begin{array}{c}
+\% \\
\times 2\%
\end{array} \\
2(2^k A \% N) \geq N
\]

where $S_0 = 0$ and $x_k$ denotes the $k$th bit of an $n$-bit number $X$. While the adders can share an ancillary bit, the doublers each require their own bit in the general case. If $2^k A \forall 0 \leq k \leq n$ and $N$ are not known classically, this thus requires $n + 1$ qubits; if these values are known, the doublers can share their ancillary bit as well, making only 2 qubits required.

Without the modulus operation, the resulting sum from all of these blocks is

\[
\sum_{k=0}^{n-1} 2^k A x_k = A \sum_{k=0}^{n-1} 2^k x_k = AX.
\]

As addition and multiplication are well-defined modulo $N$, this is in the same congruence class modulo $N$ as the product with the modulus operations; thus, the chain of blocks defines the basic
modular multiplication block

where the mark $n^*$ is used to indicate the difference in ancilla required if $2^kA$ and $N$ are or are not classically known. In the case where no values are known classically, the multiplication requires five full registers; in the case where all $2^kA$ and $N$ are known classically, it requires only 2 ancillary bits and four registers, but two of the registers are used to store classical values. Thus, to multiply some quantum register $X$ by a known classical value $A$ modulo a classical value $N$ requires $2n + 4$ qubit registers, all of which contain results after the operation finishes.

Note that with the basic block, an empty register is required at the outset, but no empty register is provided at the close; this could pose an issue when laying blocks in succession. However, when $N$ is odd and $A$ is coprime to $N$ (both of can be assumed for Shor’s algorithm), a solution to this issue presents itself. When $A$ and $N$ are both classically known, it is a simple matter to determine $A^{-1}$ modulo $N$ classically prior to the algorithm; when $A$ is not classically known, [46] details an $O(n^2)$ implementation of the quantum extended Euclidean algorithm for coprime $A$ and $N$, which can likewise determine $A^{-1}$.

We know that $N$ is odd (if $N$ were even it would have a trivial factor of 2, making Shor’s algorithm unnecessary), and thus $2^{n+1}$ has an inverse modulo $N$; as both $N$ and $2^{n+1}$ are classically knowable, we can preconstruct a circuit to multiply by $(2^{n+1})^{-1}$ mod $N$; no information is lost, as multiplying by $2^{n+1}$ reverses it.

We now construct the circuit

After the last multiplication, the top register holds $X \oplus A^{-1}AX\%N$, which clearly cancels to 0 in all cases. It is a simple matter of again multiplying by $(2^{n+1})^{-1}$ then reversing the modular inverse gate (which has the added benefit of clearing its ancilla) to yield the modular multiplication block
This block contains two basic modular multiplications which each use $n^\ast + 1$ ancillary bits, though the +1 can be recycled, leaving $2n^\ast$ uncleared ancilla. There are two modular multiplication blocks and two modular inverse blocks, all with performance $O(n^2)$, so this block also is $O(n^2)$.

1. **Controlled Modular Multiplication [$\times_{C\%}$]**

There are multiple ways to construct a controlled multiplication block. The most obvious means is to simply replace all of the adders with a controlled version. Alternately, adding an additional register and two sets of $n + 1$ Fredkin gates gives

This construction reduces the number of controls needed, which reduces the complexity of the overall circuit. It even does not impact the number of ancillary bits; simply make the clearing of the bit after each doubling be controlled by the control bit as well, and clear based on classically-known values if the control states that the multiplication is being performed.

There is no clear advantage of one control implementation over another; the naive implementation requires more complex gates, and introduces a large number of controls, while the Fredkin implementation requires an additional full register of $n + 1$ qubits. In the modular exponentiation case, we will omit the register needed for the Fredkin implementation.

2. **Alternate Modular Multiplication Blocks**

Markov and Saeedi\[40\] construct several multiplication blocks for specific values of $A$ and/or $N$, which offer significant advantages to the circuit above in exchange for loss of generality. They also propose a distinct implementation of the modular multiplication block which uses a division-with-remainder method, as opposed to the repeated-addition method proposed above. This requires $\lfloor \log_2 A \rfloor + n + 1$ ancillary bits, more than the circuit proposed above, but offers significant advantages for some values of $A$ and $N$, particularly when $A^2 < N$.

VI. MODULAR EXPONENTIATION FOR SHOR’S ALGORITHM

In our implementation of Shor’s algorithm, we wish to take a non-classically determined value $A$ and raise it to a superposition of exponents modulo $N$, where $N$ is an input parameter (and thus classically known). We will do so by repeated multiplication by $A^2 \% N$ for $0 \leq k \leq n$, using $n + 1$ modular multiplication blocks.
The $k$th multiplication block is of the form

\[
\begin{array}{c}
\begin{array}{c}
A^{2^k} \\
\vdots
\end{array}
\end{array}
\begin{array}{c}
\times \% C
\end{array}
\begin{array}{c}
A^{2^k}
\end{array}
\]

\[
\begin{array}{c}
P_k
\end{array}
\begin{array}{c}
\vdots
\end{array}
\begin{array}{c}
P_{k+1} = P_k A^{2^k} y_k \% N
\end{array}
\]

where $P_0 = 1$. It is then necessary to square $A^{2^k}$ modulo $N$ between multiplication blocks, as we are working with $A$ not classically known.

For this we will use a naive implementation requires an additional $n + 1$-qubit register into which $A^{2^k} \% N$ is copied using CNOT gates, followed by an additional modular multiplication, which thus requires a total of $3n + 2$ qubits, one of which is recyclable prior to the end of the calculation. More effective quantum circuits for modular square are not considered in this paper, and none were readily found in literature; implementations of Shor’s algorithm for general $N$ focus on classically known $A$, as $A$ can be easily determined classically in the typical case. Thus, our consideration of this is largely to demonstrate the advantages of a partially-classical circuit over a purely quantum one.

Modular exponentiation of classically unknown $A$ thus requires five input registers and $3n^2 + n + 1$ ancillary qubits, for a total of $3n^2 + 6n + 6$ qubits. In the case where $A$ is classically known, the modular multiplication blocks do not have any unclearable ancillary bits, requiring a total of 1 ancillary bit each, and it is not necessary to perform a quantum modular square at all ($A^{2^k} \% N$ can be found classically for all $k$), reducing the number of qubits needed to $5n + 6$ (one ancillary bit and five registers).

**VII. CONCLUSION**

We construct an $n$-bit implementation of modular exponentiation $A^x \% N$ which only requires that $N$ be classically known, and the corresponding implementation where $A$ and $N$ are both classically known. This circuit uses $O(n^3)$ gates, or equivalently $O((\log N)^3)$ gates; this concurs with theoretical expectations of the period-finding routine. When $A$ is classically known, the number of ancillary qubits drops off and reduces to be comparable to other general-$N$ implementations of Shor’s algorithm. This requires a general case of $3n^2 + 6n + 6$ qubits, which can be reduced to $5n + 6$ in the event of a classically-known value of $A$ (assuming that modifications can be made to the circuit based on that classical value), clearly illustrating the advantages of classical control over $A$. This $O((\log N)^3)$ gate count is the best we have found for classically unknown $A$, while $O(n)$ is the minimum necessary to perform Shor’s Algorithm on general $N$. The circuit also operates in $O(n^3)$ depth, as it is not parallelised.

There are numerous variations on the circuit, which offer various advantages and disadvantages. Table II lists a comparison of our construction with other implementations of modular exponentiation; in most cases, it offers situational advantages over other implementations: it has more effective asymptotic behaviour in one area and worse in another. While [17] and [45] offer similar asymptotic behaviour to our own circuit, the former is designed for ion-trap hardware and the latter requires more non-asymptotic qubits.
The number of gates required is linear for a single adder and the derived blocks, quadratic for multiplication, and cubic for exponentiation, which is in keeping with the general circuits discussed in passing by [40] in comparison to their linear specific-case circuits.

There are two clear avenues for further work: first, developing a means to square a number modulo $N$ (a non-reversible operation by itself) on fewer than $n + 1$ ancillary qubits and in less than $O(n^2)$ time should be possible, but no implementation was discovered as this paper was being written; all reviewed implementations of Shor’s algorithm using repeated modular multiplication focused on classically-known values of $A$. This is largely a matter of curiosity, to determine how a quantum $A$ might work, as $A$ can be determined classically rather simply.

Further, we do not consider the impact of error correction on our circuit, instead focusing on simply constructing the framework. An actual implementation would likely require error correction, and thus it would be necessary to determine any consequences that an appropriate scheme might have on the design and performance of the circuit.

While compiled circuits can use much smaller numbers of qubits, and are thus often more useful for experimental tests, they lose out on generality. A general formulation gives a broader view of the problem which the compiled circuits may overlook, and is necessary for any practical realisation of the algorithm in the future. Our proposed general implementation of Shor’s algorithm provides a blueprint for large-scale quantum photonic integrated circuit realizations.
J. Selected Topics in Quantum Electronics 15, 1673 (2009).

[8] A. Politi, M. J. Cryan, J. G. Rarity, S. Yu, and J. L. O’Brien, “Silica-on-silicon waveguide quantum circuits,” Science 320, 646 (2008).

[9] A. Politi, J. C. F. Matthews, and J. L. O’Brien, “Shor’s quantum factoring algorithm on a photonic chip,” Science 325, 1221 (2009).

[10] B. J. Smith, D. Kundys, N. Thomas-Peter, P. G. R. Smith, and I. A. Walmsley, “Phase controlled integrated photonic quantum circuits,” Opt. Express 17, 13516 (2009).

[11] J. C. F. Matthews, A. Politi, D. Bonneau, and J. L. O’Brien, “Heralding two-photon path entanglement on a chip,” Physical Review Letters 107, 163602 (2011).

[12] P. J. Shadbolt, M. R. Verde, A. Peruzzo, A. Politi, A. Laing, M. Lobino, J. C. F. Matthews, M. G. Thompson, and J. L. O’Brien, “Generating, manipulating and measuring entanglement and mixture with a reconfigurable photonic circuit,” Nature Photonics 6, 45 (2012).

[13] J. E. Kennard, J. P. Hadden, L. Marseglia, I. Aharonovich, S. Castelloto, B. R. Patton, A. Politi, J. C. F. Matthews, A. G. Sinclair, B. C. Gibson, S. Prawer, J. G. Rarity, and J. L. O’Brien, “On-chip manipulation of single photons from a diamond defect,” Physical Review Letters 111, 213603 (2013).

[14] B. Calkins, P. L. Mennea, A. E. Lita, B. J. Metcalf, W. S. Kolthammer, A. Lamas-Linares, J. B. Spring, P. C. Humphreys, R. P. Mirin, J. C. Gates, P. G. R. Smith, I. A. Walmsley, T. Gerrits, and S. W. Nam, “High quantum-efficiency photon-number-resolving detector for photonic on-chip information processing,” Optics Express 21, 22657 (2013).

[15] X. Xu, Z. Xie, J. Zheng, J. Liang, T. Zhong, M. Yu, S. Kocaman, G.-Q. Lo, D.-L. Kwong, D. R. Englund, F. N. C. Wong, and C. W. Wong, “Near-infrared hong-ou-mandel interference on a silicon quantum photonic chip,” Optics Express 21, 5014 (2013).

[16] M. J. Collins, C. Xiong, I. H. Rey, T. D. Vu, J. He, S. Shahnia, C. Reardon, T. F. Krauss, M. J. Steel, A. S. Clark, and B. J. Eggleton, “Integrated spatial multiplexing of heralded single photon sources,” Nature Photonics 4, 2582 (2013).

[17] J. W. Silverstone, D. Bonneau, K. Ohira, N. Suzuki, H. Yoshida, N. Iizuka, M. Ezaki, C. M. Natarajan, M. G. Tanner, R. H. Hadfield, V. Zwiller, G. D. Marshall, J. G. Rarity, J. L. O’Brien, and M. G. Thompson, “On-chip quantum interference between silicon photon pair sources,” Nature Photonics 8, 104 (2014).

[18] J. W. Silverstone, R. Santagati, D. Bonneau, M. J. Strain, M. Sorel, J. L. O’Brien, and M. G. Thompson, “Qubit entanglement on a silicon photonic chip,” arXiv:1410.8332.

[19] Y. Zhang, L. McKnight, E. Engin, I. M. Watson, M. J. Cryan, E. Gu, M. G. Thompson, S. Calvez, J. L. O’Brien, and M. D. Dawson, “Gan directional couplers for integrated quantum photonics,” Applied Physics Letters 99, 161119 (2011).

[20] T. Linjordet, “Integrated photonic 3d waveguide arrays for quantum random walks on a circle,” arXiv:1010.3784.

[21] L. Sansoni, F. Sciarrino, G. Vallone, P. Mataloni, A. Crespi, R. Ramponi, and R. Osellame, “Polarization entangled state measurement on a chip,” Physical Review Letters 105, 200503 (2010).

[22] A. Crespi, R. Ramponi, R. Osellame, L. Sansoni, I. Bongioanni, F. Sciarrino, G. Vallone, and P. Mataloni, “Integrated photonic quantum gates for polarization qubits,” Nature Communications 2, 566 (2011).

[23] L. Sansoni, F. Sciarrino, G. Vallone, P. Mataloni, A. Crespi, R. Ramponi, and R. Osellame, “Two-particle bosonic-fermionic quantum walk via integrated photonics,” Physical Review Letters 108, 010502 (2012).

[24] J. B. Spring, P. S. Salter, B. J. Metcalf, P. C. Humphreys, M. Moore, N. Thomas-Peter, M. Barbieri, X.-M. Jin, N. K. Langford, W. S. Kolthammer, M. J. Booth, and I. A. Walmsley, “On-chip low loss heralded source of pure single photons,” Optics Express 21, 13522 (2013).

[25] G. Corrielli, A. Crespi, R. Geremia, R. Ramponi, L. Sansoni, A. Santinelli, P. Mataloni, F. Sciarrino, and R. Osellame, “Rotated waveplates in integrated waveguide optics,” Nature Communications 5, 4249 (2014).

[26] J. C. F. Matthews, A. Politi, A. Stefanov, and J. L. O’Brien, “Manipulation of multiphoton entanglement in waveguide quantum circuits,” Nature Photonics 3, 346 (2009).

[27] J. P. Sprengers, A. Gaggero, D. Sahin, S. J. Nejad, F. Mattioli, R. Leoni, J. Beetz, M. Lermer,
M. Kamp, S. Hofling, R. Sanjines, and A. Fiore, “Waveguide single-photon detectors for integrated quantum photonic circuits,” arXiv:1108.5107.

[28] D. Sahin, A. Gaggero, Z. Zhou, S. Jahanmirnejad, F. Mattioli, R. Leoni, J. Beetz, M. Lermer, M. Kamp, S. Hofling, and A. Fiore, “Waveguide photon-number-resolving detectors for quantum photonic integrated circuits,” Applied Physics Letters 103, 111116 (2013).

[29] F. Najafi, J. Mower, N. C. Harris, F. Bellei, A. Dane, C. Lee, P. Kharel, F. Marsili, S. Assefa, K. K. Berggren, and D. Englund, “On-chip detection of entangled photons by scalable integration of single-photon detectors,” arXiv:1405.4244.

[30] J. Mower and D. Englund, “Efficient generation of single and entangled photons on a silicon photon integrated chip,” Physical Review A 84, 052326 (2011).

[31] N. Matsuda, P. Karkus, H. Nishi, T. Tsuchizawa, W. J. Munro, H. Takesue, and K. Yamada, “On-chip generation and demultiplexing of quantum correlated photons using a silicon-silica monolithic photonic integration platform,” Optics Express 22, 22831 (2014).

[32] H. Herrmann, X. Yang, A. Thomas, A. Poppe, W. Sohler, and C. Silberhorn, “Post-selection free and integrated optical source of non-degenerate and polarization entangled photon pairs,” Optics Express 21, 27981 (2013).

[33] J. Lugani, S. Ghosh, and K. Thyagarajan, “Switchable hyperentangled photon pairs from an integrated optic waveguide device,” Journal of the Optical Society of America B 30, 795 (2013).

[34] H. Takesue, N. Matsuda, E. Kuramochi, W. J. Munro, and M. Notomi, “An on-chip coupled resonator optical waveguide single photon buffer,” Nature Communications 4, 2725 (2013).

[35] S. L. Mouradian, T. Schroder, C. B. Poitras, L. Li, J. Goldstein, E. H. Chen, J. Cardenas, M. L. Markham, D. J. Twitchen, M. Lipson, and D. Englund, “Scalable integration of long-lived quantum memories into a photonic circuit,” arXiv:1409.7965.

[36] B. J. Metcalf, J. B. Spring, P. C. Humphreys, N. Thomas-Peter, M. Barbieri, W. S. Kolthammer, X.-M. Jin, N. K. Langford, D. Kundys, J. C. Gates, B. J. Smith, P. G. R. Smith, and I. A. Walmsley, “Quantum teleportation on a photonic chip,” Nature Photonics 8, 770 (2014).

[37] H. W. Li, J. Wabnig, D. Bitauld, P. Shadbolt, A. Politi, A. Laing, J. L. O’Brien, and A. O. Niskanen, “Calibration and high fidelity measurement of a quantum photonic chip,” New Journal of Physics 15, 063017 (2013).

[38] N. Tezak, A. Niederberger, D. S. Pavlichin, G. Sarma, and H. Mabuchi, “Specification of photonic circuits using quantum hardware description language,” Philosophical Transactions of the Royal Society A 370, 5270 (2012).

[39] Enrique Martin-Lopez, Anthony Laing, Thomas Lawson, Roberto Alvarez, Xiao-Qi Zhou, and Jeremy L. O’Brien, “Experimental realization of Shor’s quantum factoring algorithm using qubit recycling,” Nature Photonics 6, 773 (2012).

[40] Igor L. Markov and Mehdi Saeedi, “Constant-Optimized Quantum Circuits for Modular Multiplication and Exponentiation,” Quantum Information and Computation 12, 361 (2012).

[41] Steven A. Cuccaro, Thomas G. Draper, Samuel A. Kutin, and David Petrie Moulton, “A new quantum ripple-carry addition circuit,” arXiv:quant-ph/0410184.

[42] Thomsen, Michael Kirkedal, Axelsen, and Holger Bock, “Parallel optimization of a reversible (quantum) ripple-carry adder,” Unconventional Computing, 7th International Conference, UC 2008 Vienna, Austria, August 25-28, 2008.

[43] Thomas G. Draper, Samuel A. Kutin, Eric M. Rains, and Krysta M. Svore, “A logarithmic-depth quantum carry-lookahead adder,” Quantum Inf. and Comp. 6, 351 (2006).

[44] Christof Zalka, “Fast versions of Shor’s quantum factoring algorithm,” arXiv:quant-ph/9806084.

[45] Stephane Beauregard, “Circuit for Shor’s algorithm using 2n+3 qubits,” Quantum Inf. and Comp. 3, 175 (2003).

[46] John Proos and Christof Zalka, “Shor’s discrete logarithm quantum algorithm for elliptic curves,” Quantum Inf. and Comp. 3, 317 (2003).

[47] David Beckman, Amalavoyal N. Chari, Srikrishna Devabhaktuni, and John Preskill, “Efficient networks for quantum factoring,” Phys. Rev. A 54, 1034 (1996).

[48] Vlatko Vedral, Adriano Barenco, and Artur Ekert, “Quantum networks for elementary arithmetic operations,” Phys. Rev. A 54, 147 (1996).
[49] Archimedes Pavlidis and Dimitris Gizopoulos, “Fast quantum modular exponentiation architecture for Shor’s factoring algorithm,” Quantum Inf. and Comp. 14, 0649 (2014).
[50] Paul Pham and Krysta M. Svore, “A 2d nearest-neighbor quantum architecture for factoring in poly-logarithmic depth,” Quantum Inf. and Comp. 13, 937 (2013).
[51] Rodney Van Meter and Kohei M. Itoh, “Fast quantum modular exponentiation,” Phys. Rev. A 71, 052320 (2005).
[52] Samuel A. Kutin, “Shor’s algorithm on a nearest-neighbor machine,” [arXiv:quant-ph/0609001].
[53] Austin G. Fowler, Simon J. Devitt, and Lloyd C. L. Hollenberg, “Implementation of Shor’s algorithm on a linear nearest-neighbour qubit array,” Quantum Inf. Comp. 4, 237 (2004).