An improved CMOS-based inductor simulator with simplified structure for low-frequency applications

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Abstract In this paper, an improved inductor simulator structure is presented, which can be configured as either grounded or floating inductor simulator with low component count. To achieve simplified structure, inductor simulator circuits are designed using a minimal number of transistors and small capacitance, rather than the complex components/modules such as current convey and operational trans-conductance amplifier which are traditionally used. The simulation results based on 0.5 µm CMOS process parameters show that the proposed structure is able to produce a broad range of inductance values and compared to other similar structures, it provides wider operational frequency bandwidth for the same or comparable inductance value. Furthermore, the structure can be implemented with much smaller chip area using a small capacitance in the circuit, but at the price that it has a higher minimum operational frequency compared to other structures.

Keywords Grounded inductor simulator · Floating inductor simulator · Active inductor · CMOS integrated circuits · MOSFET · Operational frequency

1 Introduction

Inductance is a vital component for many analog and mixed-signal circuits and systems. Large inductances are often needed if operational frequency of a circuit is not very high, but they are difficult to be integrated into an integrated circuit (IC) due to the large chip area required. There have been a number of attempts to develop inductor simulators, which can perform the analog function of inductance [1–12]. The most commonly used structures of these inductor simulators are composed of multiple passive components and complicated operational modules such as current conveyor and operational trans-conductance amplifier which are traditionally used. However, these are primarily used for high-frequency or RF applications. In this paper, an improved structure for grounded inductor composed of only five active components and one capacitor for low-frequency applications is proposed. Compared to the structure in [1] which was proposed for the same purpose, this structure is further simplified and is able to simulate the same or comparable inductance value with smaller capacitor and wider operational frequency bandwidth. In addition, by adding only three more transistors to the structure, the grounded inductor simulator can be easily upgraded to floating inductor simulator.

The rest of this paper is organized as follows: Section 2 presents the process of designing inductor simulator. Section 3 shows simulation results and analysis of the proposed inductor simulators. Finally, conclusions are drawn in Sect. 4.
2 Proposed inductor simulator

To achieve simplified structure and simulate a range of inductance values at low operational frequency, MOSFET is to be used as prime component rather than CC or OTA. The design method is based on the nullator–norator technique. A nullator represents a port that has no potential difference across its two terminals and has no current flowing into or out of it, as shown in Fig. 1a. A norator represents a port that has arbitrary current flowing through and has arbitrary potential difference across its two terminals, as shown in Fig. 1b. The nullator–norator models of second generation current conveyor (CCII) and MOSFET are shown in Fig. 1c, d [5]. Figure 1 illustrates clearly the structural similarity between CCII and MOSFET, which suggests that instead of CCII, MOSFET may be used to construct an inductor simulator.

There are two key components that are used to build the proposed inductor simulator, MOSFET and capacitor. MOSFET is used to convert voltage signal into current signal. The capacitor is used to emulate voltage–current characteristic of inductor, i.e., [13]

\[
Z_C = \frac{V_C}{I_C} = \frac{1}{j\omega X_C} \\
Z_L = \frac{V_{sim}}{I_{sim}} = j\omega X_L
\]

(1)

where \(V_C\) and \(I_C\) are the voltage and the current applied to capacitor, \(V_{sim}\) and \(I_{sim}\) are the voltage and the current applied to inductor, \(X_C\) is the value of the capacitor, \(X_L\) is the value of the inductor, \(\omega\) is operational frequency, and \(j\) is the imaginary unit representing 90-degree phase shift. It is obvious from Eq. (1) that if \(X_C = X_L\), the impedance of the capacitor is reciprocal of the inductor’s impedance.

To realize simulation of inductor, an inductor simulator is constructed here using a two-port operational module, as shown in Fig. 2. One port (PORT 1) of the module connects to a capacitor \(C_0\). The other port (PORT 2) connects to an arbitrary external circuit. The function of this operational module is to make \(\frac{V_{sim}}{I_{sim}}\) equal to \(\frac{I_C}{V_C}\), so that the impedance of the simulated inductor \((\frac{V_{sim}}{I_{sim}})\) is the same as the reciprocal of the impedance of the capacitor \(C_0\). It operates as follows: Once the voltage \(V_{sim}\) is applied onto PORT 2, the current \(I_C\) that is proportional to \(V_{sim}\) is generated and fed into the capacitor \(C_0\) in PORT 1, therefore producing the voltage \(V_C\) across the capacitor. Then from the \(V_C\), the current \(I_{sim}\) that is proportional to \(V_C\) is generated and fed back into PORT 2.

Following the working explained above, the nullator–norator structure of the inductor simulator is acquired, as shown in Fig. 3.

The relationship between the port voltage \(V_{sim}\) and the port current \(I_{sim}\) can be deduced as [14]

\[
\frac{I_{sim}}{V_{sim}} = \frac{g_{m1}g_{m3}g_{m4}}{g_{m2}} \frac{V_C}{I_C} = \frac{1}{j\omega L_{sim}},
\]

(2)

where \(L_{sim} = \frac{g_{m2}}{g_{m1}g_{m3}g_{m4}} C_0\) is the inductor to be simulated through the capacitor \(C_0\). By replacing the nullator–norator pairs in Fig. 3 with MOSFETs, we can obtain the grounded inductor simulator circuit, as shown in Fig. 4. The \(g_{m1}, g_{m2}, g_{m3},\) and \(g_{m4}\) in Fig. 3 are trans-conductances.
of the MOSFETs M1, M2, M3, and M4 in Fig. 4, respectively. The MOSFET M5 is to provide a current bias for the circuit.

In order to consider the main parasitic parameters that will affect the frequency response of the circuit, Eq. (2) needs to be modified by taking parasitic capacitance and output resistance of MOSFETs into account [14], and then it becomes

$$I_{\text{sim}} \left( V_{\text{sim}} \right) = \frac{G_m R_{O35}}{1 + j \omega / \omega_0} \left( 1 + j \omega / \omega_1 \right) + \frac{1}{R_{O4}} + j \omega \left( C_{gs1} + C_{ds4} \right)$$

(3)

where $G_m = \frac{g_m}{g_{m1} g_{m2} g_{m4}}$ is the open loop trans-conductance, $R_{O35} = R_{O3} | R_{O5}$ is the resultant resistance of the output resistance of M3 ($R_{O3}$) and the output resistance of M5 ($R_{O5}$) in parallel connection, $R_{O4}$ is the output resistance of M4, $C_{gs}$ and $C_{ds}$ are the gate-source parasitic capacitance and the drain-source parasitic capacitance of MOSFET, respectively, and $\omega_0 = g_m / \left( C_{gs2} + C_{gs3} + C_{ds2} + C_{ds1} \right)$ and $\omega_1 = 1/R_{O35} C_0$ are the two poles of the open loop transfer function. The $\omega_0$ is always a very high-frequency pole, which is normally negligible.

According to the conventional calculations [14], if the frequency $\omega > 10 \omega_1$, Eq. (3) can be simplified as

$$\frac{I_{\text{sim}}}{V_{\text{sim}}} = \frac{1}{j \omega L_{\text{sim}}} + \frac{1}{R_{\text{sim}}} + j \omega C_{\text{sim}}$$

(4)

where

$$L_{\text{sim}} = \frac{g_m}{g_{m1} g_{m2} g_{m4}} C_0,$$

$$R_{\text{sim}} = R_{O4},$$

$$C_{\text{sim}} = C_{gs1} + C_{ds4}.$$
Fig. 6 Floating inductor simulator derived from grounded inductor simulator

Fig. 7 Configuration for simulations of grounded inductor simulator

ulator can be acquired, as shown in Fig. 6. This floating inductor simulator has the same function and electrical characteristics as the grounded inductor simulator in Fig. 4, but it is more flexible in terms of its applications since both of its terminals can be connected to other circuits.

3 Simulation results and analysis

The circuit of Fig. 4 is simulated using the configuration shown in Fig. 7. The terminal $V_{\text{bias}}$ connects to a voltage source $V_S$ to provide DC voltage bias for the MOSFET M5. The terminal $V_{\text{sim}}$ connects to a current source $I_S$ to provide the DC current bias $I_{\text{bias}}$ for the MOSFET M4 and to provide the AC signal excitation $I_{\text{sim}}$ as well. The bulks of NMOS and PMOS transistors are connected to the ground GND and the power supply VCC, respectively. The simulations are performed using SPICE based on 0.5 $\mu$m CMOS process BSIM3v3 model (the threshold voltages of NMOS and PMOS are $V_{T_{\text{NO}}} = 0.7619$ V and $V_{T_{\text{PO}}} = -0.9570$ V, respectively; the electron mobility and hole mobility are $u_{0N} = 861.083$ cm$^2$/Vs and $u_{0P} = 568.314$ cm$^2$/Vs.

| Table 1 | Simulation results of grounded inductor simulator: inductance value and operational frequency range |
| --- | --- |
| Circuit construction type | Component dimension/value | Testing condition | Simulation result |
| Type-1 | M1 W × L ($\mu$m$^2$) | M2 W × L ($\mu$m$^2$) | M3 W × L ($\mu$m$^2$) | M4 W × L ($\mu$m$^2$) | M5 W × L ($\mu$m$^2$) | C0 (F) (pF) | V$\text{bias}$ (V) | I$\text{bias}$ ($\mu$A) | Inductance (H) | Frequency (Hz) |
| Type-1 | 2 × 10 | 2 × 10 | 2 × 10 | 2 × 10 | 2 × 10 | 2 × 20 | 2 × 20 | 2 × 20 | 2 × 20 | 2 × 20 |
| Type-2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 | 10 × 2 |
| Type-3 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 | 2 × 2 |
respectively; the thickness of gate oxide is $T_{OX} = 25$ nm).

The dimensions of the CMOS transistors (M1−M5) used in the implementation are given in Table 1. To test the functionality of the circuit in Fig. 4, three types of constructions of the circuit with different sizes of components (Type-1, Type-2, and Type-3) are simulated, as shown in the table, so that a variety of inductor values with their corresponding operational frequency ranges can be produced.

The floating inductor simulator in Fig. 6 has the same simulation results as the grounded inductor simulator in Fig. 4, with the transistors M6−M8 having the same dimensions as the transistors M3−M5.

From the simulation results, it is obvious that compared to an ideal inductor which has no frequency restriction, the simulated inductors work within certain limited frequency range. Taken the Type-2 (35 mH) of the circuit as an example, the magnitude responses of the frequency domain simulations in Fig. 8 show that the circuit has a zero point at 620 Hz and a double-pole point at 4.6 MHz, which are determined by $R_s$ and $C_{sim}$, respectively. This is in accordance with the theoretical values.

![Fig. 8](image1.png)

**Fig. 8** Magnitude responses of each type compared to ideal inductor

![Fig. 9](image2.png)

**Fig. 9** Phase responses of each type compared to ideal inductor

### Table 2: Comparisons between this work and the similar structures in references

| Circuit structure | Number of component (MOSFET) | Simulated inductor (H) | Operational frequency (Hz) | Area ($\mu m^2$) | Test condition (bias) and power consumption |
|-------------------|-----------------------------|------------------------|-----------------------------|----------------|---------------------------------------------|
| Ref. [1]          | 7                           | 9.6 mH                 | 100−100 k                   | $10^8$          | 2.3 mW@VDD = 1.5 V                           |
| Ref. [3]          | 3                           | 1.5 mH                 | 15 k−1.5 k                  | $5 \times 10^4$ | 6.8 mW@VDD = 3 V; $V_{DD} = 5$ V             |
| Ref. [7]          | 3                           | 22 mH                  | 10 k−10 k                   | $10^8$          | 4.0 mW@VDD = 5 V; $V_{DD} = 5$ V             |
| Ref. [9]          | 8                           | 22 mH                  | 10 k−10 k                   | $10^8$          | 62 mW@VDD = 5 V; $V_{DD} = 5$ V             |
| This work (Type-1)| 5 (grounded) or 8 (floating) | 1.08 mH                | 10 k−100 k                  | $10^8$          | 187 mW@VDD = 5 V; $V_{DD} = 5$ V             |
| This work (Type-2)| 10                          | 20.6 mH                | 20 k−10 k                   | $10^4$          | 2.2 mW@VDD = 5 V; $V_{DD} = 5$ V             |
| This work (Type-3)| 15                          | 79.5 mH                | 75 k−35 k                   | $10^3$          | 7.9 mW@VDD = 5 V; $V_{DD} = 5$ V             |
| This work (Type-3)| 30                          | 10.6 mH                | 1.3 M−117 M                 | $10^2$          | 215 mW@VDD = 5 V; $V_{DD} = 5$ V             |

The transistors M6−M8 have the same dimensions as the transistors M3−M5.
retical analysis of the frequency limits described in Sect. 2. The phase responses of the frequency domain simulations are given in Fig. 9, which shows that the zero point of 620 Hz and the double-pole point of 4.6 MHz yield an actual working frequency range from 6.2 kHz (10Ωzero) to 2.3 MHz (calculated through $R_S$ and $\omega_D$-pole).

To compare with the similar structures proposed recently [1, 3, 7, 9], Table 2 is compiled, in which the area is calculated by only taking capacitor into account, as it consumes most of the chip area. It is assumed that 1 fF capacitance takes 1 $\mu$m$^2$ of chip area. The test conditions (bias) and the power consumptions under these conditions are also given.

Table 2 shows that among the similar structures compared, this structure uses the least number of MOSFETs (only 5 for grounded inductor), leading to the simplest circuit. It is capable of simulating a broad range of inductance values that are covered by all other structures. Meanwhile, for the same or comparable inductance value, its operational frequency bandwidth is much wider (e.g., for 1.0 H inductor, Type 1 of this work and Ref. [9] have a bandwidth of 868.2 Hz and 10 kHz, respectively). However, the proposed structure does not operate at as low frequency as others do (e.g., Type 3 of this work and Ref. [3] with the same inductance value of 1.5 mH have a minimum operational frequency of 79.5 Hz and 15 kHz, respectively), since it uses much smaller capacitors (no more than 10 pF) in order to significantly reduce chip area as shown in the table.

4 Conclusions

This paper describes an improved structure for inductor simulator to be used in CMOS integrated circuits for low-frequency applications. The structure features low component count and use of small capacitance, thus resulting in simplified circuit structure and much reduced chip area. The simulation results demonstrate that this structure not only can produce a broad range of inductance values but also compared to other similar structures, it provides wider operational frequency bandwidth for the same/comparable inductance value. Moreover, the structure is implemented with significantly reduced chip area using a small capacitor in the circuit, but this is at the cost of having a higher minimum operational frequency compared to other structures.

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