Optimized fermionic SWAP networks with equivalent circuit averaging for QAOA

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(Dated: November 12, 2021)

The fermionic SWAP network is a qubit routing sequence that can be used to efficiently execute the Quantum Approximate Optimization Algorithm (QAOA). Even with a minimally-connected topology on an n-qubit processor, this routing sequence enables \( O(n^2) \) operations to execute in \( O(n) \) steps. In this work, we optimize the execution of fermionic SWAP networks for QAOA through two techniques. First, we take advantage of an overcomplete set of native hardware operations [including 150 ns controlled-\( \pi \) phase gates with up to 99.67(1)% fidelity] in order to decompose the relevant quantum gates and SWAP networks in a manner which minimizes circuit depth and maximizes gate cancellation. Second, we introduce Equivalent Circuit Averaging, which randomizes over degrees of freedom in the quantum circuit compilation to reduce the impact of systematic coherent errors. Our techniques are experimentally validated on the Advanced Quantum Testbed through the execution of QAOA circuits for finding the ground state of two- and four-node Sherrington–Kirkpatrick spin-glass models with various randomly sampled parameters. We observe a ~60% average reduction in error (total variation distance) for QAOA of depth \( p = 1 \) on four transmon qubits on a superconducting quantum processor.

I. INTRODUCTION

A key challenge for scaling near-term quantum computers to address practical problems is limited qubit connectivity. While qubit mapping techniques can mitigate this limitation, recent results suggest that any mismatch between hardware connectivity and connectivity required for specific applications can erase the potential for a quantum speedup [1, 2]. This poses a particular challenge for superconducting quantum hardware which — despite the advantages of fast operation speed, high gate fidelity, and scalable fabrication — generally has the disadvantage of sparse nearest-neighbor qubit connectivity.

The fermionic SWAP network, introduced in Ref. [3] and studied further in Refs. [4, 5], offers a promising path forward for coping with limited connectivity. In fact, the fermionic SWAP network requires only minimal linear connectivity between qubits; any additional qubit couplings are unnecessary. This property is well-suited to superconducting qubits where it has the additional advantage of minimizing the effect of crosstalk due to frequency crowding [6].

Qubit routing in an \( n \)-qubit fermionic SWAP network follows a sequence of \( n - 1 \) steps, incurring \( O(n) \) total quantum circuit depth. This linear cost suffices to carry out all \( O(n^2) \) pairwise interactions between qubits, even for linearly-arranged qubits. By contrast, naive qubit routing approaches would require \( O(n^3) \) circuit depth to perform all of the necessary operations, because each of the \( O(n^2) \) pair-wise interactions would be serialized and would incur an \( O(n) \) SWAP overhead. The quadratic advantage in circuit depth offered by fermionic SWAP networks persists even in comparison to state-of-the-art qubit routing [7].

There are numerous applications of fermionic SWAP networks, broadly corresponding to evolution under a fully-connected Hamiltonian comprising mutually commuting terms. Examples include the Sherrington-Kirkpatrick spin-glass model [8], Max-Cut for use cases like VLSI circuit design [9], and k-means clustering on large datasets with coresets [7]. Furthermore, Hamiltonian evolution is at the heart of many noisy intermediate-scale quantum (NISQ) [10] algorithms such as the Quantum Approximate Optimization Algorithm (QAOA) [11] and its derivatives [12, 13], making the implementation of fermionic SWAP networks invaluable for near-term applications. In addition, fermionic SWAP networks will be favorable for noise mitigation approaches involving virtual distillation [15], in which multiple copies of a quantum state can be arranged in parallel registers with linear connectivity [16].

Given the fundamental importance of fermionic SWAP networks to many quantum applications, it is important to fully optimize their execution. Here, we introduce and apply two compilation techniques that improve their
performance. The first technique employs a richer gate-set than enabled by standard QASM (Quantum Assembly) representation for circuit decomposition. The second technique, which we term Equivalent Circuit Averaging (ECA), involves randomizing circuit decomposition over degrees of freedom in compilation to mitigate the impact of systematic coherent errors. Both of these techniques are validated at the Advanced Quantum Testbed at Lawrence Berkeley National Laboratory.

The rest of this paper is organized as follows. Section II describes the Advanced Quantum Testbed’s hardware. Section III presents our optimized gate decompositions for the Hadamard, SWAP, and Fermionic SWAP operations. Section IV presents results from cycle benchmarking of our optimized gate sequences. Section V examines the application of fermionic SWAP networks to QAOA, and Section VI introduces Equivalent Circuit Averaging for this application. Section VII concludes. Appendices A and B detail single-qubit and two-qubit parameters for the Advanced Quantum Testbed. Finally, Appendix C presents examples of the full fermionic SWAP network circuits that we executed.

II. THE ADVANCED QUANTUM TESTBED

The experiments in this work were performed on four fixed-frequency transmon \textsuperscript{17} qubits (labeled Q4, Q5, Q6, and Q7; see Table A1 in Appendix A) on an eight-qubit superconducting quantum processor (AQT@LBNL Trailblazer\textsuperscript{8-v5.c2}) at the Advanced Quantum Testbed \textsuperscript{18} (AQT). The qubits are coupled to nearest-neighbors via fixed-frequency resonators in a ring-geometry.

Arbitrary single-qubit SU(2) gates are typically implemented using physical $X_{\pi/2}$ gates (via resonant Rabi-driven pulses) and virtual $Z_{\theta}$ gates (via phase shifts between physical pulses) \textsuperscript{19}:

$$U(\alpha, \beta, \gamma) = Z_{-\pi/2}X_{\pi/2}Z_{-\beta}X_{\pi/2}Z_{-\gamma}X_{-\pi/2}. \quad (1)$$

This $ZXZXZ$-decomposition reduces the time and complexity involved in calibrating and benchmarking single-qubit gates. The disadvantage is that every computational single-qubit gate is actually composed of two physical $X_{\pi/2}$ pulses, each 30 ns in duration; thus, every single-qubit gate (cycle) in a circuit takes 60 ns by default, even if the gate could be implemented with only a single $X_{\pi/2}$ pulse. This needlessly increases circuit depth, leaving the qubits more susceptible to decoherence.

Two-qubit entangling operations are achieved using a tunable ZZ-coupling via off-resonant drives \textsuperscript{20, 21} between neighboring qubits, which is used to implement controlled-$Z$ (CZ) operations between all qubit pairs, as well as controlled-$S$ (CS) and controlled-$S^\dagger$ (CS$^\dagger$) gates. The duration of our two-qubit CZ gate is 200 ns, which is limited by the drive-induced decoherence discussed in Ref. \textsuperscript{20}. However, because the CS or CS$^\dagger$ gate performs half the rotation of a CZ, it can be implemented in less time than the CZ. We calibrate and measure a process infidelity of $4.3(1) \times 10^{-3}$ for a 150 ns CS gate between qubits (Q5, Q6), and process infidelities of $5.0(1) \times 10^{-3}$ and $3.3(1) \times 10^{-3}$ for a 150 ns CS$^\dagger$ gate between qubits (Q4, Q5) and (Q6, Q7), respectively (see Table A2 in Appendix B), which is $\sim 100$ ns faster with an error rate that is $\sim 2\times$ lower than previously measured for superconducting qubits \textsuperscript{22}.

III. OPTIMIZED GATE DECOMPOSITIONS

A. Optimized Hadamard and SWAP

We first optimize decompositions for the Hadamard ($H$) and SWAP operations. The $H$ gate has two equivalent decompositions using the \{X, Z\} basis:

$$H = \begin{pmatrix} X_{\pi/2} & Z_{\pi/2} \\ Z_{\pi/2} & X_{\pi/2} \end{pmatrix}. \quad (2)$$

$$H = \begin{pmatrix} Z_{\pi/2} & X_{\pi/2} \\ X_{\pi/2} & Z_{\pi/2} \end{pmatrix}. \quad (3)$$

The standard $ZXZXZ$-decomposition of the $H$ gate corresponds to Eq. 2. While this is a valid decomposition, Eq. 3 is preferable because it requires a single physical $X_{\pi/2}$ pulse instead of two. Therefore, the optimized Hadamard halves the duration of the gate, taking only 30 ns instead of 60 ns.

Next, we consider the SWAP operation. The default decomposition of the SWAP is

$$\begin{array}{ccc} \hline & H & H \\ \hline H & & \\ \hline \end{array} \quad (4)$$

where $\hline$ indicates the CZ gate. The middle circuit represents the standard QASM decomposition of a SWAP, which involves three alternating $CX$ gates. No further decompositions are possible until we go below the level of QASM \textsuperscript{23}. Each $CX$ decomposes to AQT’s two-qubit $Z$ basis gate by invocation of the identity $CX(q_c, q_t) = H(q_t)CX(q_c, q_t)H(q_t)$, where $q_c$ ($q_t$) is the control (target) qubit. We immediately see that applying the optimized $H$ leads to an improvement: the total SWAP duration is reduced by $4 \times 30$ ns = 120 ns, and the number of required $X_{\pi/2}$ physical pulses is halved from 12 to 6.

We can optimize even further by applying a transposition identity to move the bottom-right $H$ to the top-left. This identity reduces the total SWAP duration by an additional 30 ns, since the two “edge” $H$ gates become parallelized. After annihilating all virtual rotations arising from Eq. (4) via commutation identities, we have the final optimized SWAP:

$$\begin{array}{ccc} \hline & X_{\pi/2} & X_{\pi/2} \\ \hline X_{\pi/2} & & \\ \hline X_{\pi/2} & X_{\pi/2} \end{array} \quad (5)$$

We deployed these optimized Hadamard and SWAP decompositions through the SuperstaQ platform \textsuperscript{24}, which
can target AQT hardware. Section IV presents cycle benchmarking results for these optimizations.

### B. Background on Fermionic SWAP

The core operation needed in a fermionic SWAP network is the fermionic SWAP gate, defined as the unitary operation below, with input parameter $\theta$:

$$
\mathcal{F}_\theta = \begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & e^{i\theta} & 0 & 0 \\
0 & 0 & e^{i\theta} & 0 \\
0 & 0 & 0 & 1
\end{pmatrix}.
$$

The standard QASM-decomposed quantum circuit implementation of $\mathcal{F}_\theta$ comprises three CX gates and a single-qubit $Z_\theta$ rotation:

$$
\mathcal{F}_\theta = \begin{array}{c}
\text{CX} \\
\text{CX} \\
Z_\theta
\end{array}.
$$

It is possible to boost performance beyond this decomposition by leveraging knowledge of the target hardware’s underlying native gate set. For example, [26] compiled the fermionic SWAP operation directly down to 3 native two-qubit Sycamore (SYC) gates, rather than re-compiling each CX down to SYC gates. Relatedly, [27] developed a parametric implementation of the fermionic SWAP via access to a native XY($\theta$) gate (with duration independent of $\theta$) and a native CZ gate.

However, in these examples, the total duration of the fermionic SWAP operation is always constant, regardless of $\theta$. This leaves room for improvement. For example, it has been shown that access to a parametric CZ [i.e. CPHASE($\phi$)] yields significant improvements for the decomposition of many quantum operations [28]: in the next subsection we demonstrate that this is true for the fermionic SWAP operation as well. However, there are experimental obstacles to tuning a high-fidelity parametric gate with variable duration. For example, [29] noted ramp effects at small $\theta$ for a parametric cross-resonance gate.

Rather than incurring the calibration overhead of a parametric gate with variable duration like CPHASE($\phi$), we instead focus on the optimization opportunities from an overcomplete discrete two-qubit gate set. Concretely, we next examine the optimized $\mathcal{F}_\theta$ decompositions possible when we have access to both a CZ and CS = $\sqrt{CZ}$ gate, where the CS is faster than the CZ gate.

In typical applications, multiple fermionic SWAP gates are arranged into a nearest-neighbor fermionic SWAP network that carries out $t = 0, \ldots, n-1$ steps. Each step alternates between an odd and even pattern. At steps with odd $t$, each neighboring qubit pair with indices $(2k, 2k + 1)$ for $k \in [0, \frac{n}{2}]$ is entangled in accordance with a target Hamiltonian and then SWAPPed. Even-$t$ steps perform this interaction for qubit pairs with indices $(2k + 1, 2k + 2)$. Note that each step is highly parallel, with $\sim n/2$ operations occurring simultaneously. A prototypical example is shown in Fig. 1 which implements the Hamiltonian evolution $e^{i\gamma H}$ corresponding to a Sherrington-Kirkpatrick spin-glass model $H = \sum_{i<j<n}J_{ij}Z_i Z_j$ on $n = 4$ nodes. The utility of a fermionic SWAP network is that it efficiently generates an all-to-all interaction with a linear-depth circuit of nearest-neighbor interactions, where each interaction is a single fermionic SWAP gate corresponding to one of the commuting weight-2 terms in $H$.

$$
e^{i\gamma H} = \begin{pmatrix}
\mathcal{F}_{\theta_1} & \mathcal{F}_{\theta_01} & \mathcal{F}_{\theta_13} & \mathcal{F}_{\theta_02} \\
\mathcal{F}_{\theta_23} & \mathcal{F}_{\theta_03} & \mathcal{F}_{\theta_12} & \mathcal{F}_{\theta_02} \\
\end{pmatrix}$$

FIG. 1. Fermionic SWAP network implementing the Hamiltonian evolution $e^{i\gamma H}$ for a four-node Sherrington-Kirkpatrick model $H = \sum_{i<j<n}J_{ij}Z_i Z_j$, where $\theta_{ij} = \gamma J_{ij}$. Note that the qubit order is reversed after the operation.

### C. Optimized Fermionic SWAP Gates

We now introduce optimized, $\theta$-dependent decompositions of the fermionic SWAP gate $\mathcal{F}_\theta$, taking advantage of an overcomplete two-qubit gate set consisting of both CZ and CS or CS† gates.

For $\theta \in \{0, \pi\}$, the fermionic SWAP unitary in Eq. 6 is equivalent (up to virtual phases) to the standard SWAP gate, and so can be decomposed using the optimized SWAP described in Section III A. In the general case, using the optimized Hadamard (c.f. Eq. 3) and virtual Z rotations, the baseline fermionic SWAP decomposition still requires three CZ and six $X_{\pi/2}$ gates:

$$
\mathcal{F}_\theta = \begin{array}{c}
X_{\pi/2} \\
X_{\pi/2} \\
Z_{\theta} \\
X_{\pi/2} \\
X_{\pi/2}
\end{array}.
$$

Unfortunately, in the general case the first and final $X_{\pi/2}$ gates in Eq. 8 cannot be parallelized as they are in the optimized SWAP, and so both contribute to the depth of the standalone fermionic SWAP circuit. In Section III D we will show that this overhead can be mitigated in the context of a full fermionic SWAP network.

A second special case exists for $\theta = \pm \pi/2$, in which the fermionic SWAP is equivalent to the iSWAP (iSWAP†) gate and requires just two CZ gates. Again employing the optimized Hadamard, it can be decomposed:

$$
\pm \begin{array}{c}
X_{\pi/2} \\
X_{\pi/2} \\
X_{\pi/2} \\
X_{\pi/2}
\end{array} = \begin{array}{c}
X_{\pi/2} \\
X_{\pi/2} \\
X_{\pi/2} \\
Z_{\pm\pi/2}
\end{array}.
$$
If we have access to a parameterized CPHASE(φ) gate, we can naturally generalize the optimized SWAP and \( iSWAP \) decompositions to all fermionic SWAP circuits. Setting \( \phi = \pi - 2\theta \),

\[
F_\theta = \begin{pmatrix}
X_{\pi/2} & X_{\pi/2} & X_{\pi/2} & Z_{\pi-2\theta} & Z_{\pi-2\theta} \\
X_{\pi/2} & X_{\pi/2} & X_{\pi/2} & Z_{\pi-2\theta} & Z_{\pi-2\theta}
\end{pmatrix},
\]

(10)
correctly generates the three-CZ optimized SWAP for \( \theta \in \{0, \pi\} \) and the two-CZ optimized \( iSWAP \) for \( \theta = \pm \pi/2 \). Assuming the gate time of any CPHASE(φ) gate to be proportional to \( \phi \) for intermediary \( 0 \leq \phi \leq \pi \), the total time for \( F_\theta \) is the same as \( 2 + 2|\theta| \mod \pi \) for intermediary \( 0 \leq \theta \leq \pi \).

Equations (8) and (10) suggest that a CPHASE(φ) gate is also sufficient to generate any \( F_\theta \) for \( |2\theta - \pi| \leq \phi \). As shown in Fig. 2 by choosing \( \phi = \pi/2 \) (the CS gate) we can implement half of all possible \( F_\theta \) gates with the equivalent of 2.5 CZ gates (that is, two CZ gates and one CS gate). For any \( \pi/4 \leq \theta \mod \pi \leq 3\pi/4 \), we have,

\[
\begin{pmatrix}
X_\mu & X_{\pi/2} & X_{\pi/2} & Z_{5\pi/4} & Z_{5\pi/4} & X_\nu
\end{pmatrix},
\]

(11)
where,

\[
\begin{align*}
\mu &= \csc^{-1}(-\sqrt{2}\sin \theta), \\
\lambda &= \cos^{-1}(-\sqrt{2}\cos \theta), \\
\nu &= -2\cos^{-1}(\sqrt{\cot \theta + 1/\sqrt{2}}). 
\end{align*}
\]

An equivalent decomposition can easily be found using a \( CS^\dagger \) gate in place of CS. The \( X_\mu \) and \( X_\nu \) gates can each be implemented with two \( X_{\pi/2} \) pulses and virtual phases using Eq. 1; however, this complexity can be mitigated within a full fermionic SWAP network (Section III D).

Additional controlled-\( Z_\phi \) operations for fixed values of \( \phi \) would further refine the optimized \( F_\theta \) decomposition toward the lower bound provided by fully-parameterized CPHASE(φ). For example, as shown in Fig. 2 one quarter of all possible \( F_\theta \) are reachable using a \( CT = CPHASE(\pi/4) = \sqrt{CZ} \) gate, and so the addition of a \( CT \) to the gateset would reduce the CZ depth of these decompositions to the equivalent of 2.25 CZ gates.

D. Optimized Fermionic SWAP Networks

We can further simplify the decomposition of fermionic SWAP gates in the context of the larger network. Various discrete and continuous symmetries in the fermionic SWAP operation result in degrees of freedom to its optimized decomposition:

1. \( F_\theta = (X \otimes X)F_\theta(X \otimes X) \)
2. \( F_\theta = (1 \otimes X)F_{-\phi}(X \otimes 1) \)
3. \( F_\theta = (Z \otimes Z)F_{\theta+\pi} \)
4. \( F_\theta(q_0, q_1) = F_\theta(q_1, q_0) \) (qubit interchange),
5. \( F_\theta = F_{\theta}^\dagger \)
6. \( F_\theta = (Z_\theta \otimes Z_\varphi)F_\theta(Z_{-\varphi} \otimes Z_{-\theta}) \forall \theta, \varphi \in \mathbb{R} \)

where \( \theta, \varphi \) are continuous parameters. Symmetry 5 is useful only for \( F_\theta \) gates implemented using a CS or \( CS^\dagger \), in which case it can be used to reverse the order of entangling gates (and corresponding single-qubit gates \( X_\mu \) and \( X_\nu \)) in the circuit. (For the 3-CZ decomposition of \( F_\theta \) the physical implementations of \( F_\theta \) and \( F_{-\theta}^\dagger \) are identical.) When implementing a fermionic SWAP network, these degrees of freedom can be exploited to maximize cancellation of single-qubit gates between sequential fermionic SWAP gates.

We use an automated scheduler which computes the set of logically equivalent decompositions (generated from symmetries 1-5) of each gate in the fermionic SWAP network, and searches for the sequence of decompositions which minimizes circuit depth (corresponding to \( X_{\pi/2} \) count in the critical path). The continuous parameters \( \theta, \varphi \) (symmetry 6) are numerically optimized for each gate in the sequence. Though in general this search space grows exponentially, in practice for the circuits used in this paper a simple best-first search quickly converges on an optimal or near-optimal circuit.
IV. CYCLE BENCHMARKING OF OPTIMIZED DECOMPOSITIONS

FIG. 3. Improved SWAP gates via gate-based optimizations. The process infidelity of the optimized SWAP gate between Q4 & Q5 (top), Q5 & Q6 (middle), and Q6 & Q7 (bottom) is lower than the process infidelity of the standard decomposition due to the elimination of unnecessary gates. The blue, purple, and black data points represent the Pauli infidelity $1 - p_P$ for each Pauli channel $P$ for the standard (Std.) SWAP gate, optimized (Opt.) SWAP gate, and reference (Ref.) cycle, respectively. The solid blue (purple) line is the average process infidelity $e_D$ of the dressed cycle for the standard (optimized) SWAP gate, and the solid black line is the average process infidelity $e_I$ of the Pauli twirling operators. The dashed blue (purple) line is the process infidelity $e_T$ of target cycle (i.e. SWAP gate) estimated via Eq. 16 for the standard (optimized) SWAP sequence. The semi-transparent bands around the average process infidelities represents the 95% confidence interval uncertainty of the estimates.

To benchmark the performance of the optimized pulse sequences relative to their standard decompositions, we utilize cycle benchmarking \[25\] (CB), a scalable protocol for measuring the performance of parallel gate cycles. Cycle benchmarking differs from randomized benchmarking \[30-33\] (RB) in two keys ways: (i) it utilizes Pauli twirling instead of Clifford twirling, which maps gate errors into a stochastic Pauli channel (instead of a global depolarizing channel); (ii) CB benchmarks the performance of quantum gates performed in parallel, providing a measure of their performance in the context of multi-qubit quantum algorithms. In contrast, benchmarking the individual constituent gates of multi-qubit cycles has been shown to be a poor predictor of the global performance of quantum circuits \[34\] due to the presence of coherent errors and crosstalk between qubits, and because such benchmarks fail to capture errors on (or incurred by) idling spectator qubits \[35\].

CB measures the process fidelity of a target cycle by preparing the system in a Pauli basis state (e.g. $XYIZ$ for four qubits), and measuring the exponential decay as a function of sequence depth. A separate exponential decay of the form $A_{PP}$ can be fit for each basis preparation and measurement state $P$ (i.e. Pauli channel), where $A$ is the state-preparation and measurement (SPAM) parameter, and $p$ the fit parameter (i.e. process fidelity). Much like interleaved randomized benchmarking \[36\] (IRB), in which the target gate is interleaved between random Clifford gates, CB interleaves the target cycle between cycles of random single-qubit Pauli gates. Therefore, CB measures the process fidelity of a dressed cycle, which contains the errors due to the interleaved target cycle as well as the Pauli twirling gates. The total process fidelity is the average over $K$ Pauli channels,

$$F = \frac{1}{K} \sum_{P \in \mathcal{P}} p_P,$$

where the number of Pauli channels $K = |\mathcal{P}| \leq 4^n$ (n qubits) in the set $\mathcal{P}$ that are sampled out of the full $4^n$ possible states sets the precision of the fidelity estimate \[25\]. The process infidelity of the dressed cycle is therefore given as $e_D = 1 - F$. To separate the infidelity of the target cycle from the twirling gates, we measure the CB fidelity of the “all-identity” reference cycle, which equates to benchmarking the average performance of only the Pauli twirling gates. Similar to IRB, we can use this to estimate the process infidelity of the target ($T$) cycle by taking the ratio of the process fidelities of the dressed ($D$) and reference ($I$) cycles,

$$e_T = \frac{d-1}{d} \left(1 - \frac{F_D}{F_I}\right),$$

where $d = 2^n$ (n qubits) is the dimension of the system. Using CB has been shown to tighten the upper- and lower-bounds on the fidelity estimate of the interleaved cycle relative to IRB \[20\], which can span orders of magnitude \[37\]. We use this method to estimate a target infidelities for CZ, CS, and CS† gates (see Table A2 in Appendix B).

In Fig. 3, we plot the CB results for the standard and optimized SWAP gates (see Eq. 5) between all three qubit pairs. We see that optimized target cycle infidelity $e_T$ of the SWAP gates is reduced 25%, 23%, and 13% relative to the standard SWAP gate for (Q4, Q5), (Q5,
Q6), and (Q6, Q7), respectively. This average improvement can generally be expected for circuits utilizing basic SWAP gates; however, further optimizations can be implemented in the context of full fermionic SWAP networks with the replacement of one of the CZs in the SWAP gate with a CS or CS† gate, as outlined in the previous section. Furthermore, while the benchmarking results in Fig. [3] show improvements in the SWAP gates between all qubit pairs, they do not capture what improvements can be expected for cycles of gates in any four-qubit application. In Table I, we compare the benchmarked improvements in optimized cycles. All optimized (Opt.) cycles have a lower CB process infidelity than their respective standard (Std.) decompositions.

We see universal improvement in the target cycle infidelity $e_T$ for the optimized circuits, with reductions in $e_T$ ranging from 64% for the all-Hadamard cycle to 12% for the SWAP cycle. These results demonstrate that simple improvements in circuit decomposition and gate optimizations can lead to dramatic improvements in benchmarked gate and cycle performance. Next, we highlight how these fidelity improvements can lead to performance improvements in fermionic SWAP networks.

### Table I. Benchmarked improvements in optimized cycles.

| Error Rate | Ref. | Std. | Opt. | Std. | Opt. | Std. | Opt. | Std. | Opt. | Std. | Opt. |
|------------|------|------|------|------|------|------|------|------|------|------|------|
| $e_I$ ($10^{-5}$) | 9.6(6) | 1.5(1) | 2.11(7) | 3.4(1) | 9.6(7) | 10.2(3) | 1.09(9) | 0.68(9) | 2.3(1) | 9.0(4) | 5.1(2) |
| $e_P$ ($10^{-2}$) | 0.19(8) | 1.09(9) | 2.3(1) | 9.6(7) | 11.7(4) | 10.4(4) | 0.5(1) | 2.11(7) | 1.5(1) | 9.6(7) | 10.4(4) |
| $e_T$ ($10^{-2}$) | 38% | 53% | 53% | 38% | 12% |

We see that the optimized (Opt.) circuits generally perform worse [equivalent] for (Q4, Q5) [(Q6, Q7)] circuits of depth $p = 1$, and from $D_{Opt.} = 0.23(4)$ to $D_{Opt.} = 0.22(6)$ for circuits of depth $p = 2$. For two-qubit networks, the optimized circuits outperform the standard circuits on average for qubits (Q5, Q6), but perform worse [equivalent] for (Q4, Q5) [(Q6, Q7)]. We conjecture that the failure of the optimized circuits to outperform the standard circuits for qubits (Q4, Q5) and (Q6, Q7) is due to systemic coherent errors, whose impacts can dominate algorithm performance and are not accurately captured by randomized benchmarks (see the discussion in Section [VI]). The parameter angle $\gamma$ determines what gate optimizations can be implemented for each network, with $\pi/4 \leq \gamma \leq 3\pi/4$ and $5\pi/4 \leq \gamma \leq 7\pi/4$ defining the angles for which CS or CS† gates can be used in place of CZ gates (see Fig. 2). The $\gamma$ values are randomly chosen in Fig. 4, but they are seeded such that half of the fermionic SWAP networks tested can take advantage of the CS or CS† gates at $p = 1$. These results demonstrate that simple changes to circuit decomposition and gate-based optimizations can lead to clear improvements in algorithm and application performance, highlighting the importance of smart compilers and more continuous gate sets in the NISQ era.

### V. APPLICATION BENCHMARKING OF QAOA

The Quantum Approximate Optimization Algorithm (QAOA) [11] describes a variational ansatz for solving combinatorial optimization problems described by an objective Hamiltonian $H$. QAOA is characterized by a hyperparameter $p$ that specifies the depth of the ansatz. Specifically, the ansatz is $e^{i\beta_1 B}e^{i\gamma_1 H}...e^{i\beta_1 B}e^{i\gamma_1 H}$, where $B = \sum_i X_i$ is a mixing Hamiltonian and $\gamma, \beta$ represent $2p$ classically optimized variational parameters. It is believed that QAOA is hard to approximate even at $p = 1$ and is therefore a leading candidate for demonstrations of quantum advantage [28]. We generate QAOA circuits corresponding to Sherrington-Kirkpatrick spin-glass model Hamiltonians with edge weights $J_{ij}$ randomly selected from $\pm 1$ (see Appendix C for the exact symbolic form of the circuits). Each $e^{i\gamma H}$ is then implemented with fermionic SWAP networks with gates $F_{\pm \gamma}$. Parameters $\beta_i, \gamma_i$ are sampled uniformly from $[0, 2\pi]$.

In Fig. 4, we measure two-qubit ($p = 1$) and four-qubit ($p = 1$ and $p = 2$) QAOA circuits (see Appendix C for example circuits) for various angles $\gamma$ and benchmark the performance using the total variation distance (TVD),

$$D(p, q) = \frac{1}{2} \sum_{x \in X} |p_x - q_x|,$$

where $p_x$ is the probability of measuring a bit string $x$ in a set $X$, and $q_x$ is the ideal (noiseless) probability. We see that the optimized (Opt.) circuits generally provide more accurate performance relative to the standard (Std.) decompositions, reducing the average TVD from $D_{Std.} = 0.20(5)$ to $D_{Opt.} = 0.14(3)$ for four-qubit QAOA circuits of depth $p = 1$, and from $D_{Std.} = 0.23(4)$ to $D_{Opt.} = 0.22(6)$ for circuits of depth $p = 2$. For two-qubit networks, the optimized circuits outperform the standard circuits on average for qubits (Q5, Q6), but perform worse [equivalent] for (Q4, Q5) [(Q6, Q7)]. We conjecture that the failure of the optimized circuits to outperform the standard circuits for qubits (Q4, Q5) and (Q6, Q7) is due to systemic coherent errors, whose impacts can dominate algorithm performance and are not accurately captured by randomized benchmarks (see the discussion in Section [VI]). The parameter angle $\gamma$ determines what gate optimizations can be implemented for each network, with $\pi/4 \leq \gamma \leq 3\pi/4$ and $5\pi/4 \leq \gamma \leq 7\pi/4$ defining the angles for which CS or CS† gates can be used in place of CZ gates (see Fig. 2). The $\gamma$ values are randomly chosen in Fig. 4, but they are seeded such that half of the fermionic SWAP networks tested can take advantage of the CS or CS† gates at $p = 1$. These results demonstrate that simple changes to circuit decomposition and gate-based optimizations can lead to clear improvements in algorithm and application performance, highlighting the importance of smart compilers and more continuous gate sets in the NISQ era.
FIG. 4. Improved fermionic SWAP networks via gate-based optimizations. The TVD performance of fermionic SWAP networks of angle $\gamma$ are plotted for qubits (a) (Q4, Q5), (b) (Q5, Q6), and (c) (Q6, Q7), and four-qubit circuits with (d) $p = 1$ and (e) $p = 2$ stages. For (b), (d), and (e), the optimized (blue, Opt.) circuits outperform the standard (black, Std.) on average (dashed lines). The ECA (purple) results consistently outperform both the standard and optimized circuits. The grey shaded regions define the angles for which $CS$ or $CS^\dagger$ gates can be utilized. The results in (d) are plotted against the $\gamma$ from stage 1 (the triangle markers denote circuits which utilize a $CS$ or $CS^\dagger$ gate in stage 2). (Error bars on the TVD $\sim O[10^{-3}]$ are smaller than the markers.)

VI. EQUIVALENT CIRCUIT AVERAGING

One limitation of benchmarking the average performance of gates or cycles is that randomized benchmarks are not accurate predictors of the global performance of structured quantum circuits due to the presence of coherent errors [34]. When averaging over a twirling group, such as the Clifford (Pauli) group for RB (CB), all errors are converted into a global depolarizing (stochastic Pauli) channel. However, in actual quantum algorithms, the physical error mechanisms are more complex than depolarizing or Pauli channels, as coherent errors can interfere constructively or destructively from one cycle to the next. Therefore, while the optimized pulse sequences show clear improvements in cycle fidelity (cf. Table I) measured via CB, this does not always guarantee improvements in algorithm performance composed of these cycles. This can be seen in Fig. 4, in which the standard circuit decompositions occasionally outperform the optimized circuits for the four-qubit results, and outperform the optimized circuits on average for the two-qubit results for qubits (Q4, Q5).

Being systematic in nature, coherent errors can in theory be measured and corrected via recalibration or added compensation pulses. However, the complexity of fully characterizing coherent errors (i.e. context-dependent rotation axes and angles [39]) on multiqubit processors that arise due to classical and quantum crosstalk is intractable, and no known scalable methods exist for doing so for systems with continuous single-qubit gatesets. Various methods exist for suppressing coherent errors, such as dynamical decoupling [40] and error-correcting composite pulse sequences [41], or randomization methods for “tailoring” them into stochastic noise, such as Pauli twirling [42-45], Pauli frame randomization [46-48], and randomized compiling [49, 50]. However, these methods generally require the modification of single-qubit gates or the inclusion of more gates (e.g. in the case of dynamical decoupling and composite sequences), or require that the two-qubit gates in circuits are Clifford so that inverting Pauli operators can be efficiently computed and applied. Adopting these techniques would therefore require forgoing the circuit optimizations (and corresponding fidelity gains) employed so far in this work — both by necessitating additional $X_{\pi/2}$ pulses and precluding the use of non-Clifford $CS$ and $CS^\dagger$ gates.

A similar strategy has been proposed for circuit synthesis methods, in which systematic approximation errors are rendered incoherent by averaging over various circuits near a target unitary generated from ensembles of approximate decompositions [51, 52]. We employ this general idea (with systematic errors in the physical gates taking the place of approximation errors) using the space of equivalent fermionic SWAP decompositions generated by the degrees of freedom outlined in Section III D. If we were to randomly sample from these decompositions for each gate in a circuit, we would forgo the single-qubit gate reduction achieved by the optimized scheduling pro-
procedure. However, the sequence of gate decompositions which minimizes the depth of the overall circuit is in general not unique. By treating the circuit holistically, we can sample from the subset of logically equivalent circuits which all minimize circuit depth. This is easily implemented by randomizing the search path used by the scheduler. Though the constraints on randomization necessary to preserve circuit depth mean that we cannot make solid guarantees on the mitigation of coherent errors, we empirically find that averaging over equivalent circuits generated in this way is an effective strategy for systematic error mitigation. We call this strategy Equivalent Circuit Averaging (ECA).

For the circuits in Fig. 1 we generate $M = 20$ logically equivalent optimized circuits for each angle $\gamma$ (see Appendix C for example circuits). In order to normalize shot statistics, we measure each equivalent circuit $s = S/M$ times and compute the union over all $M$ results to obtain an equivalent statistical distribution for a circuit measured $S$ times; $S = 10000$ and $s = 500$ for the results in Fig. 4. We see that ECA dramatically reduces the TVD on average in comparison to both the standard and optimized results for all of the two- and four-qubit fermionic SWAP network results, reducing the average TVD by $\sim 60\%$ [26\%] from $D_{\text{Std.}} = 0.20(5)$ to $D_{\text{ECA}} = 0.08(2)$ [$D_{\text{Std.}} = 0.23(4)$ to $D_{\text{ECA}} = 0.17(6)$] for the four-qubit $p = 1$ [$p = 2$] QAOA results, and providing the most accurate measured probability distribution in 88\% of all of the two- and four-qubit circuits measured.

While the classical overhead of generating and measuring $M$ logically equivalent circuits scales roughly linearly in $M$, we observe significant improvements in the measured results. These results demonstrate that ECA is a useful tool for smart compilers which optimize circuit decomposition using various degrees of freedom, and is not limited to circuits only containing two-qubit Clifford gates, adding to the toolbox of randomization methods that can be employed in the NISQ era.

VII. CONCLUSIONS

Quantum compilers play a fundamental role in the translation of abstract quantum circuits to machine instructions in gate-based quantum computing. In the NISQ era, it is necessary to consider the balance between the calibration overhead for large gate sets and optimal circuit decomposition for quantum application performance. In this work, we show that utilizing a smart compiler for cancelling unnecessary single-qubit gates is a simple method for lowering gate error rates in quantum circuits. We further demonstrate that by adding an additional two-qubit gate ($CS$ or $CS^\dagger$) to our gate set for each qubit pair, we observe significant improvement in benchmarked cycle and application performance. While our work focuses on fermionic SWAP networks and their application to QAOA, non-Clifford $CS$ gates also find importance in universal quantum computation and magic-state distillation for fault-tolerance [53-55].

Additionally, we introduce Equivalent Circuit Averaging to mitigate the impact of systematic coherent errors in non-Clifford circuits by utilizing the various degrees of freedom of quantum compilers to generate many logically equivalent circuits. Given the difficulty in characterizing and predicting the impact of coherent errors on algorithm performance, such a method negates the need for doing so and assumes that the average over many circuits will reduce the impact of coherent errors on the algorithm results. We demonstrate the effectiveness of this approach with our application benchmark results, in which we find that ECA improves the accuracy of the measured probability distribution for 88\% of the randomly-generated two- and four-qubit QAOA circuits.

While ECA was employed by taking advantage of the various degrees of freedom of fermionic SWAP networks, a more sophisticated search procedure would likely expand the applicability of our methods for scheduling and generating equivalent circuits for more general applications. We further imagine possible "hybrid" strategies in which ECA is combined with other randomization protocols (e.g. randomized compiling) for maximizing the ways in which logically equivalent circuits can be expressed, thus minimizing residual coherent errors. The cost of ECA (both classically and in terms of single-qubit gate optimization) in the general case and the degree to which it shields noise in quantum systems (i.e. in the manner of other randomization methods which twirl over a specific gateset) are open questions, which we plan to explore in future work.

Finally, as described in Section III C, access to a parameterized $\text{C PHASE}(\phi)$ gate would minimize the $CZ$ gate time for any fermionic SWAP gate. The corresponding gate decomposition (Eq. 10) also avoids the $\theta$-dependent $X_\mu$ and $X_\nu$ gates in Eq. 11, allowing for more efficient gate cancellation and a greater opportunity for randomness in ECA. The experimental validation of this decomposition would be a natural extension of this work, and would provide insight into the value of parameterized two-qubit gates for NISQ systems.

ACKNOWLEDGEMENTS

This work was supported by the U.S. Department of Energy, Office of Science, Office of Advanced Scientific Computing Research Quantum Testbed Program under Contract No. DE-AC02-05CH11231. This material is also supported by the U.S. Department of Energy, Office of Science, Office of Advanced Scientific Computing Research under Award Number DE-SC0021526. A.H. acknowledges financial support from the National Defense Science & Engineering Graduate (NDSEG) Fellowship.

R.R. and P.G. devised the optimized circuit decompositions. A.H. conducted the experiments and analyzed the data. ECA was conceived by A.H. and developed by R.R. and P.G. R.K.N., D.I.S., F.C., and I.S. supervised
all theoretical and experimental work. J.M.K. fabricated the sample. V.O. developed the SuperstaQ software interface to the AQT. A.H., R.R., V.O., and P.G. wrote the manuscript with input from all coauthors.

F.C., P.G., R.R., and V.O. have a financial interest in Super.tech and the SuperstaQ platform. F.C. is also an advisor to Quantum Circuits, Inc. All other authors declare no competing interest.

Appendix A: Single-qubit parameters

| Qubit freq. (GHz) | Q4 | Q5 | Q6 | Q7 |
|------------------|----|----|----|----|
| Anharm. (MHz)    | -275 | -275 | -271.35 | -269 |
| $T_1$ (µs)       | 60(5) | 62(5) | 52(4) | 55(8) |
| $T_2^*$ (µs)     | 36(5) | 37(6) | 36(6) | 33(6) |
| $T_2^{cho}$ (µs) | 62(5) | 73(7) | 68(7) | 54(6) |
| Readout $P(0|0)$ | 0.999 | 0.995 | 0.995 | 0.995 |
| Readout $P(1|1)$ | 0.990 | 0.989 | 0.979 | 0.974 |
| RB (10$^{-3}$)   | 0.68(2) | 1.01(2) | 0.95(5) | 0.67(1) |
| Sim. RB (10$^{-3}$) | 1.49(8) | 2.5(2) | 3.1(2) | 2.4(2) |

Table A1. Single-qubit parameters.

Table A1 lists the relevant qubit parameters for the four transmon qubits used in this work. Qubit frequencies and anharmonicities are measured using Ramsey spectroscopy. Relaxation ($T_1$) and coherence ($T_2^*$ and $T_2^{cho}$) times are extracted by fitting exponential decay curves to the excited state lifetime and Ramsey spectroscopy measurements (without and with an echo pulse), respectively. Readout fidelities $|P(0|0)$ and $P(1|1)|$ are determined by performing ensemble measurements of the qubits prepared in $|0\rangle$ and $|1\rangle$ and classifying the results using a Gaussian Mixture Model fit to the in-phase (I) and quadrature (Q) heterodyne voltage signals. Error rates for single-qubit gates are measured using randomized benchmarking (RB) and simultaneous (Sim.) RB. All error rates are defined in terms of the process infidelity $e_{F} = 1 - p$, where $p$ is the exponential fit parameter in $Ae^{pm}$ for a sequence depth of $m$ and SPAM parameter $A$. This is equivalent to the average gate infidelity $r(\mathcal{E})$,

$$e_{F}(\mathcal{E}) = r(\mathcal{E})\frac{d+1}{d}, \quad (A1)$$

where $d = 2^n$ is the system dimensionality ($n$ qubits).

Appendix B: Two-qubit gate parameters

Table A2 lists the parameters for the individual $CZ$, $CS$, and $CS^\dagger$ gates used in this work. All two-qubit gates are composed of square pulses with cosine ramps. The total gate duration of each pulse (including the ramps) are listed in Table A2, the fraction of the total gate duration for the ramp up and ramp down (individually) are specified under ‘Ramp fraction’. Although the $CS$ and $CS^\dagger$ gates can nominally be performed in half the duration of the $CZ$ gates, the cosine ramps limit the minimum duration of the gates. Instead, the $CS$ and $CS^\dagger$ gates are constructed to contain approximately half the total integrated area under the curve as the $CZ$ gates, thus performing half of the conditional rotation as the $CZ$. This is only approximate, since the conditional stark shift on each qubit will differ depending on the drive frequencies and amplitudes.

The choice of $CS$ versus $CS^\dagger$ for each qubit pair was determined depending on the sign of the Stark-induced ZZ interaction (cf. Refs. [20][21]); it is more efficient (i.e., requires a smaller amplitude) to drive the $CS$ rotation in one direction for some qubits, and in the opposite direction for other qubits, depending on the detuning of the drive signal. While the $CZ$ can be benchmarked using RB, the $CS$ and $CS^\dagger$ gates are non-Clifford, and therefore require either non-Clifford RB [22][53] or cycle benchmarking [23][CB] with refocusing pulses (used in this work). Table A2 lists the average process infidelity $e_{D}$ of the dressed cycle (target gate plus Pauli twirling gates), as well as the inferred process infidelity $e_{T}$ of the target gate alone (cf. Eq. [16]) using the measured CB process infidelity $e_{I}$ of the “all-identity” reference cycle for each qubit pair. Two-qubit RB process infidelities $e_{F}$ are also included for the $CZ$ gates. While the fidelities of the individual two-qubit gates are useful for determining the quality of the gates in general, the process infidelities of the distinct parallel four-qubit cycles are more relevant to the application circuits presented in the body of this work. These values are listed in Table I of the main text.
Appendix C: Example Fermionic SWAP network circuits

Example circuits for the fermionic SWAP networks presented in the main text can be seen in Fig. A1. This includes the symbolic representation of the two- and four-qubit Fermionic SWAP networks of depth \( p = 1 \), and the four-qubit Fermionic SWAP network of depth \( p = 2 \). An example two-qubit circuit is presented in Fig. A1(b) for a random choice of the two Fermionic SWAP angles, \( \gamma \) and \( \beta \). Additionally, the exact decompositions for this circuit in terms of \( CS \) and \( CS^\dagger \) gates are included, as well as logically equivalent variants of each.

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FIG. A1. Example fermionic SWAP networks. Symbolic circuit representations of Fermionic SWAP networks (of depth $p$) for (a) two qubits ($p = 1$), (g) four qubits ($p = 1$), and (h) four qubits ($p = 2$). (b) Baseline decomposition of a two-qubit fermionic SWAP network for a random choice of $\gamma$ and $\beta$ with CZs. (c) Optimized decomposition of the circuit in (b) in terms of the native gateset utilizing a CS instead of a CZ. (d) Logically equivalent decomposition of the circuit in (c). (e) Optimized decomposition of the circuit in (b) in terms of the native gateset utilizing a $CS^\dagger$ instead of a CZ. (f) Logically equivalent decomposition of the circuit in (e).