Low-Precision Hardware Architectures Meet Recommendation Model Inference at Scale

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Abstract—Tremendous success of machine learning (ML) and the unabated growth in ML model complexity motivated many ML-specific designs in both CPU and accelerator architectures to speed up the model inference. While these architectures are diverse, highly optimized low-precision arithmetic is a component shared by most. Impressive compute throughputs are indeed often exhibited by these architectures on benchmark ML models. Nevertheless, production models such as recommendation systems important to Facebook’s personalization services are demanding and complex: These systems must serve billions of users per month responsively with low latency while maintaining high prediction accuracy, notwithstanding computations with many tens of billions parameters per inference. Do these low-precision architectures work well with our production recommendation systems? They do. But not without significant effort. We share in this paper our search strategies to adapt reference recommendation models to low-precision hardware, our optimization of low-precision compute kernels, and the design and development of tool chain so as to maintain our models’ accuracy throughout their lifespan during which topic trends and users’ interests inevitably evolve. Practicing these low-precision technologies helped us save datacenter capacities while deploying models with up to 5X complexity that would otherwise not be deployed on traditional general-purpose CPUs. We believe these lessons from the trenches promote better co-design between hardware architecture and software engineering and advance the state of the art of ML in industry.

I. INTRODUCTION

Machine learning has experienced revolutionary advances in the past decade. The advancement has led to state-of-the-art production models that are complex, compute intensive and consume large amount of memory resources [17] [27] [40] [60] [63] [66]. For instance, the memory requirement of deep learning recommender systems has grown from few tens of GBs to the terabyte regime [41] [63]. To fuel the needs of rising application domains, computer architectures are evolving, be it general-purpose CPUs or GPUs with new features [1] [2] [21] or specialized accelerators [2] [12] [34], targeting deep learning. While these architectural features or architectures are diverse, one major commonality is the support for low-precision arithmetic datatype.

Low-precision arithmetic datatype offers several orthogonal advantages simultaneously. Storing model parameters in low-precision formats greatly increases parameter loading throughput and reduces power consumed on data movement [16] [25] [26] [35] [52]. It also increases compute throughput if computation is well optimized for the underlying architecture. For instance, TPUs are customized [34] with the int8 and fp16 arithmetic to accelerate the inference of neural networks. The latest Intel CPUs added the VNNI feature (Vector Neural Network Instructions) [9] to support neural network acceleration. NVIDIA Tensor Cores support mixed precision of fp32 and fp16 to deliver 7x more flops/s than fp32 on a Tesla V100 GPU [42]. Moreover, int8 is generally supported on many customized accelerators and CPUs, which usually deliver much higher compute throughput than floating point.

To improve user experience, social network services such as those Facebook provides, leverage deep learning in a wide range of applications [27]. Among all the deep learning applications, recent work showed, in 2019, more than 70% of the total machine learning inference cycles served by Facebook’s datacenter fleets are devoted to recommendation use cases [24]. Thus, performance and energy efficiency improvement of deep learning recommendation models will translate into significant infrastructure capacity saving.

Recommender systems have evolved with increasing model complexities: from simple content and collaborative filtering, to matrix factorization [37] [50], multi-layer perceptrons and deep learning models [18] [47] [54] [55] [64] [65] [67]. Facebook’s production recommendation models consist of many tens to a hundred billion parameters to achieve high learning capacity [45]. Despite the continuously growing learning capacity, the inference latency of the recommender systems must meet specified SLA thresholds, such as 100ms, to ensure quality user experience [48]. Low-precision arithmetic is promising to improve the inference efficiency. Nevertheless, deploying low precision in production recommender models at Facebook’s scale proves extremely challenging:

Meeting Stringent Accuracy Requirement: Facebook’s recommendation models are typically trained using the full-precision numerical format. Trained models can be converted to a lower precision format for deployment through post-training quantization (PTQ). We do not deploy a low-precision recommendation model that has more than 0.05% accuracy degradation compared against the original full-precision model [58]. This is a much more stringent requirement compared to other vision or language use cases, not to mention that
there are many recommendation model variants in production serving for different tasks. Our workflow needs to provide accuracy guarantee for all the production models.

**Maintaining Consistent Accuracy and Performance during Online Training:** The recommendation models are periodically updated via online training to adapt to new data. The online training pipeline includes model training, low-precision model transformation, model publishing and then model serving. In each online training cycle, the workflow that converts a full-precision model to low precision needs not only to produce an accurate and robust model, but also do so quickly to meet the online training cadence.

**Maximizing Latency-Bounded Throughput Performance:** In order to meet the aforementioned accuracy requirement, a low-precision model in fact often uses mixed precision: exploiting arithmetic types of various precision commensurate with numerical sensitivity of different operators or workload characteristics. Fine-grained performance profiling is needed to guide the low-precision strategies for the different components. Furthermore, to maximize performance gains, we need optimized low-precision kernels tailored for specific hardware architectures. The kernels should support accuracy compensation techniques required by the low-precision operators, and the implementation details should be consistent across the entire system stack. These implementations are challenging by themselves; the numeric validation and debugging support for such implementations on different hardware platforms are even more so.

This paper presents the low-precision techniques, analysis and tool chain we developed to meet the stringent accuracy and performance challenges and to streamline the deployment of Facebook’s production recommendation models in low precision on existing hardware platforms including CPUs and accelerators. We hope the lessons we learned about the good and bad in these architectures are useful and that the methodologies we are sharing are applicable to many low-precision architectures in general.

The rest of the paper is organized as follows. Section II introduces the low-precision arithmetic architectures and various fundamental techniques to exploit them; Section III describes the recommendation model architecture and the important metric any low-precision version must meet. We then present the important strategies we used to deploy our production models in low precision. Section IV describes the supporting tool chain needed to realize these strategies: numerical issues debugging and accuracy maintenance throughout a model’s lifespan. Section V shares the important lessons we learned in the past couple of years deploying production scale models in low-precision arithmetic. Section VI talks about related works on low-precision architectures. Section VII recaps the key points and outlines an agenda for future work.

## II. Low-Precision Arithmetic Architectures

Floating-point and integer are the two fundamental data types in computer architectures. Traditional computing often use either the 32 or 64 versions of these type: fp\{32/64\}. Since deep learning is real-number based and the numerical range and precision provided by fp32 are clearly sufficient, that has been the default arithmetic type. More recently, researchers demonstrated that effective deep learning inference \[8,32,34,38\], and even training \[8,51\] can rely on numerics in a more limited range and precision than that given by fp32. Storage-only low-precision on CPU can be used with appropriate software, thus improving memory access while relying still on fp32 for computation. Obviously, native arithmetics in the hardware are preferred as they can potentially offer computational savings as well. On traditional Intel general-purpose CPUs, low-precision arithmetics support is limited except for int8 and the recent bfloat16 \[3\] support on Cooper Lake series \[1\]. In contrast, customized accelerators have more flexibility to add low-precision arithmetics, and the resulting performance can be significantly higher. Figure 1 shows the overall hierarchy of the Vendor-X hardware modules in terms of the compute efficiency and programmability. Notwithstanding the great promises of accelerators, fully exploiting low-precision on CPU is invaluable as they can support continuously emerging new models expeditiously and serve as a stepping stone for those most intensive models to be deployed on customized accelerators. Let us examine these low-precision arithmetic and strategies to benefit from them.

### A. Low-precision Floating Point

Low-precision floating-point representations are easy to adopt because of their high programmability. Traditional Intel Broadwell/Skylake CPUs do not support fp16 arithmetic so we can only use fp16 as a storage format. The model can thus be loaded/stored in half precision so that there could be memory size reduction and memory bandwidth savings; but the compute will nevertheless still be done in fp32. In contrast to storage-only support, some custom accelerators support fp16 in storage as well as in computation, offering savings not only in memory footprint and bandwidth, but also boosting compute performance. Indeed, the fp16 arithmetic on accelerators could provide one order of magnitude higher throughput over fp32 on CPUs. A few implementation details are noteworthy:

- Down conversion is required when we either convert the full-precision model parameters to fp16, or when we store computed intermediate results (performed in fp32) in memory as fp16. We found it important to saturate values beyond fp16’s normal range to the fp16’s finite...
values of the largest magnitude rather than following the default IEEE behaviour that results in $\pm\text{Inf}$.

- Down conversion of non-zero numbers in fp16's sub-normal range needs to be handled consistently; either flushing to zero or saturating at $\pm\text{fp16}_{\text{min}}$, the non-zero normal fp16 values of smallest magnitude.

- Proper and consistent support for Inf/NaN handling proves important in guarding against abnormal behavior and large accuracy drop of a model.

Note in particular that these implementation details may vary on different hardware platforms: maintaining consistency between software implementations with hardware across the entire software stack is important.

Although using fp16 doesn’t provide as significant performance wins as shorter integer formats that will be discussed in later sections (especially the fp16 data storage only on CPUs), it’s been a good starting point to migrate the recommendation model inference to the low precision regime and prepare us for the accelerator deployment that relies heavily on low precision numerics to deliver high performance.

### B. Short Integer and Quantization

Alluded to earlier, deep learning intrinsically relies on computing with real numbers. If the representation and computation of these real numbers can use, say, 8-bit integers instead of fp32, the memory saving and performance boost can be superior to the use of fp16. Indeed, on Intel Broadwell/Skylake CPUs, one can expect up to 4x in memory savings and 2x performance wins as short integer formats that will be discussed in later sections (especially the fp16 data storage only on CPUs), the non-zero normal fp16 values of smallest magnitude.

The quantization of all the fully connected layers is based on Equations (1) and (2), but we use a slight quantization variant when handling embedding tables as shown later.

It is evident that $X - D(Q(X)) \neq 0$ in general and this difference is called the quantization error. There are many important design options to explore in order to reduce the quantization error, such as signed/unsigned integer format, symmetric/asymmetric quantization, the rounding function, etc. Particularly, we discuss the following design options for mitigating the accuracy loss:

**Quantization granularity:** We can use one pair of quantization parameters for the entire matrix or a sub-block of the matrix. For example, per-channel quantization (w.r.t. the output channels in fully connected or convolutional layers) leads to better inference accuracy in practice. The cost, however, is the storage of multiple pairs of the quantization parameters and slightly different arithmetics support on customized accelerators to work with a vector of quantization parameters.

**Quantization range:** In Equation (2), the $X_{\text{max}}$ and $X_{\text{min}}$ can either come from the raw data or a refined range eliminating the outliers. There are many ways to refine the data range. One way is to use the aggregated quantization errors as the guidance. The quantization error can be defined in various forms, e.g. L1-norm, L2-norm or KL divergence. And then we search for the range that minimizes the aggregated quantization errors. Empirically, the L2-norm error minimization algorithm provides the best accuracy for the recommendation models.

**Static or dynamic quantization:** The quantization parameters can be chosen either statically or dynamically, based on the history data or the current batch of data for inference. They have pros and cons in terms of both performance and accuracy. For static quantization, we need to insert *Quantize* and *Dequantize* operators around the chain of operators to be quantized and pre-calculate the quantization parameters for the inputs and outputs. For dynamic quantization, each of the operators to be quantized will take fp32 inputs, quantize before doing the compute, and then dequantize after the compute to produce fp32 outputs. Dynamic quantization is more flexible in selecting the operators to quantize without runtime overhead from the extra *Quantize* and *Dequantize* ops when switching between precisions, and it can adapt to the new data in each online training cycle very well. However, the drawback is that the overhead of on-the-fly quantization parameter calculation prevents us from using complex quantization algorithms, such as L2-error minimization algorithm, which might provide better accuracy for the model inference. Moreover, without special support, dynamic quantization is more difficult to deploy on hardware accelerators as quantization/dequantization and actual compute may need to be executed on different hardware modules.

### C. FBGEMM for Compute Performance

Low-precision floating-point and integer representations provide clear memory footprint and bandwidth reduction, and careful quantization choices reduce quantization errors. In
order to realize the compute performance gain made possible by these reduced precision types, we also need to provide optimized low-precision compute kernels. This leads to our development of FBGEMM [5, 6, 36] library to support the fp16 and int8 operators on Intel CPUs, which has been the backend for the low-precision operators in both Caffe2 and PyTorch. For fp16 operators on CPUs, FBGEMM supports the low-precision conversion and prepacking so that we can reduce the model size and save half of the memory bandwidth when loading the weight parameters. The compute kernels are also generalized to accept the packed weight format. The int8 operators in FBGEMM can also leverage the vector instructions on specific CPU architectures to maximize the compute throughput. Quantization/dequantization operations are fused with the compute kernels when possible. For the customized hardware accelerators, we exploit the kernels that come with the accelerators and provide optimization feedbacks from software-hardware co-design perspectives. We will talk more about accelerator specific optimizations in Section III-E.

III. DEPLOYMENT OF FAST AND ACCURATE RECOMMENDERS IN LOW PRECISION ARCHITECTURE

We aim to substitute recommendation models running in full-precision arithmetic with ones that use low precision for higher serving throughput with little to no degradation of the prediction accuracy. The following section discusses performance and accuracy metrics, overall methodology in utilizing low precision compute, finishing with specific strategies on CPUs and accelerators, respectively.

A. Performance and accuracy metrics

For recommendation models, performance is usually measured by the throughput at the p99 latency threshold (e.g., 100ms). Thus, performance optimization techniques such as model partitioning, parallelization, or batching are applied.

The accuracy of recommendation models is evaluated with two kinds of metrics: online and offline. Online accuracy metrics for production models are application dependent, and can only be read after the model is in A/B testing or in production. Consequently, low-precision models must have been evaluated against offline metrics prior being tested online to avoid the potential of significant service quality drop. Normalized (cross) entropy (NE) [23] is an offline accuracy metric that is applicable to various models producing prediction probabilities on binary labeled datasets. Cross entropy is a well accepted loss function for training these models. Normalized entropy is a slight modification, given by Equation 3.

\[
NE = \frac{\sum_{i \in D} -w_i(y_i \log(p_i) + (1 - y_i) \log(1 - p_i))}{\sum_{i \in D} -w_i(y_i \log(1 - p_i) + (1 - y_i) \log(1 - p_i))};
\]

\[
p^* = \frac{\sum_{i \in D} w_i y_i}{\sum_{i \in D} w_i};
\]

The numerator is the standard cross entropy where \(p_i\) is the prediction probability produced by the model and \(y_i = 0\) or \(1\) is the label of the data point \(d_i\), \(i \in D\), weighted by \(w_i\). The denominator is the cross entropy of a naive model that for every data point produces the same probability \(p^*\) equal to the fraction of (weighted) positive labeled data. NE gives an intuitive indication on how well the model predicts better than the most simple predictions.

The NE metric evaluates how good the predictions are using a specific model, the lower the better. To evaluate the low precision impact, we use the relative NE difference by comparing the NE of a low-precision model with the original fp32 model, as shown in Equation 4. Our goal for the low-precision inference is to maximize the performance given the accuracy constraint. One example is to maximize the throughput at 100ms p99 latency while accuracy is within an acceptable threshold (e.g., \(NE_{\text{diff}} \leq 0.05\%\)).

\[
NE_{\text{diff}} = \frac{NE_{\text{fp32}} - NE_{\text{lowp}}}{NE_{\text{fp32}}} \quad (4)
\]

B. Methodology

The design space of low-precision realizations of a full-precision recommendation model is gargantuan: each of many tens of operators can possibly use low-precision for storage and/or computation in floating point or integer, and the latter with different quantization schemes as described earlier, not to mention the interaction with performance optimizations for each operator. Exhaustive search in the design space is out of the question. Our methodology first heuristically explores low-precision models that meet the \(NE_{\text{diff}}\) accuracy requirement before optimizing the performance of such models on the target hardware platform. Note however that performance optimizations, especially on customized hardware, could affect numerics adversely (e.g. cancellation issues from accumulation order differences) and thus one needs to iterate over the performance and numerics optimizations in general. Given a specific recommendation model and target \(NE_{\text{diff}}\) threshold, Figure 2 depicts the process which we now elaborate:

Initial Characterization: We examine the specific operators employed by the given model and arrive at basic theoretical performance characteristics such as memory intensity and footprint. Figure 2 depicts the process which we now elaborate.
as roofline analysis [1][48]. Together with actual profiling, we identify the top performance bottlenecks. Profiling on the target hardware is easier said than done as more often than not the accelerators are not available or the actual low-precision kernels have yet to be written. Thus, we have developed our internal performance characterization and modeling tool for the accelerator based on the CPU profiling reference and the hardware specs [43], which allows us to identify such performance bottlenecks early on.

**Quantization Scheme:** As int8 offers the best performance improvement opportunities, we aggressively explore the possibility of adopting quantization to all operators and use fp16 (or even fp32) as contingency. Based on the understanding obtained in the previous step about performance bottlenecks, we decide on the precision and specific quantization options if necessary for each of the operators in question. We design the heuristic-based iterative quantization scheme search algorithm and automate the process with the automatic quantization workflow, which we will discuss in more details in Section IV.

**Quantization Parameters:** For the int8 quantization, specific quantization parameters are calculated based on the quantization schemes together with histogram of intermediate outputs to determine the effective numerical ranges $[X_{\min}, X_{\max}]$. Note that an operator that behaves numerically faithful to the underlying low-precision computation needs to be present. It could either be the production quantized operator or some form of efficient emulation.

**Graph Level Optimizations:** Operator fusion is commonly used to improve both accuracy and performance. For example, the `FullyConnected` operator can be fused with the following `Relu` operator when possible. Quantization parameters are subsequently based on `Relu`’s output range rather than that of `FullyConnected`’s, thus better utilizing the low-precision bits. There are also some cases where we can fuse a `Q()` operator that is next to a `D()` operator.

**Acceptance Test:** Terminate if we have a low-precision production model that satisfies the accuracy constraint. Otherwise, continue improving the quantization scheme based on the feedback from per-layer quantization errors and heuristics to mitigate the errors with advanced quantization options as listed in Section II-B. However, if the ratio of the skipped FCs in terms of compute flops exceeds a threshold such that the performance gain from the int8 model diminishes, the iterative quantization scheme search algorithm fails. We need to further investigate on the model and possibly leverage techniques such as quantization-aware training or model co-design to unlock the low-precision techniques.

**Performance Optimizations:** This mostly involves kernel optimization on the target hardware platform. Sometimes, the performance optimization involves fundamental changes in the operator implementation, especially on accelerators, which may change the numeric behavior of the operator. At this point, one may return to the early step where different quantization schemes are considered.

Depending on the specific quantization scheme, dynamic or static, fixed quant scheme or adaptive, the optimization cycle can take from seconds to a few hours on a single server-class machine. For instance, static quantization with fixed quant schemes only need a few minutes to collect activation histograms and then calculate the quantization parameters. For static quantization with the auto quantizer, in addition to the histogram collection, the iterative quant scheme search may take $2 \sim 5$ hours depending on whether we need many iterations to skip FCs in order to meet the accuracy target.

**C. Workload characterization for recommendation models**

Recent recommendation model size can easily exceed 100GBs, dominated by the hundred-billion-parameter embedding tables. The representative architecture of the recommendation models has been described in [47], mainly consisting of embedding table lookups and MLPs so as to operate well on both sparse and dense features. Workload characteristics of these components [48] differ. Embedding table lookups are memory capacity and bandwidth bound. While MLPs are significantly more compute intensive than embedding table lookups are, they may also be memory bandwidth bound depending on the inference batch size. When no batching is used or the batch size is small, loading the weight parameters from memory could be the main performance bottleneck. Based on our performance roofline model [48], batching can shift the MLPs from the memory bound to compute bound, which boosts performance in general. However, the batch size cannot be too large in practice because processing too many entities at once for a single user results in high latency, degrading user experience. Figure 3 is one typical profiling snapshot of a particular production recommendation model. It shows the diversity of operators and also underlines the dominance of the `SparseLengthsSum` and `FullyConnected` operators, steering our special attention to them.

A suite of synthetic models, representative of production use cases are released as DLRM benchmarks [4] to facilitate the research in external communities. We have provided representative model architecture parameters and performed in-depth performance analysis in previous papers [24][23]. DLRM has been used as the recommendation benchmark for training and inference by the MLCommons community. Specific sizes are adopted based on industry discussions across multiple companies, including Google, Netflix and Alibaba.

**D. Low-precision strategies on CPUs**

**Int8/Int4 for embedding tables** We use low precisions for embedding tables to reduce memory footprint rather than economize computation. Production recommendation models have over a hundred embedding tables, each having anywhere from hundreds to tens of billions parameters. We have explored 8-bit and 4-bit quantization for the embedding tables [22].

Alluded to previously, quantization and dequantization of embedding tables use a formula slightly different from Equations 1 and 2. Specifically, The quantization and dequantization equations are shown below.

$$X_q = Q(X) = \text{clip}(\text{rnd}((X - \text{bias})/\text{scale}), \text{I}_{\text{min}}, \text{I}_{\text{max}}),$$

$$X = D(X_q) = \text{scale} \times X_q + \text{bias}. \quad (5)$$
Embeddings quantized with uint8 have been deployed in our production models since a few years ago. It successfully reduced the model size by nearly 50% without noticeable accuracy degradation in the final event predictions.

More aggressive quantization techniques using 4-bit or even lower bitwidths can potentially bring more capacity savings, but renders the resulting models less likely to meet prescribed accuracy requirement. We used different ways to compensate for the accuracy loss in those cases: Different algorithms can be used to determine quantization ranges based on L1 or L2 error (Section II-B). We can also use mixed precisions for the embedding tables. An important observation is that 4-bit quantization results in less quantization errors when used on large embedding tables than on small ones. Hence we quantize the output of embedding table lookups to floating point before feeding the features into the interaction component. Using the floating point parameter bias instead of the integer parameter zeropt here saves the compute for dequantization.

Since each embedding table can have billions of parameters, using a single (scale, bias) pair for the entire table usually leads to higher-than-acceptable quantization error. Thus, in practice, we do rowwise quantization, which is to determine one (scale, bias) pair per row, stored adjacent to that row for efficient retrieval.

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Practically, the data is stored as uint8 by packing multiple elements into one byte. Since there is no native support for 4-bit compute on CPUs, we have developed dedicated kernels for the SparseLengthsSum operators in FBGEMM [5] to optimize the compute with low-precision inputs and fuse the dequantization step to get the full-precision outputs.

Fp16/Int8 for the MLPs The MLPs are compute intensive. They are mainly composed of FullyConnected operators in which matrix multiplications dominate inference latency. However, memory bandwidth could also be the bottleneck when the batch size is small and loading the weights from memory is the main overhead. For models running on CPUs, the input sizes of the FullyConnected operators range from 1M to 100M in terms of bytes to read from DRAM. Typical batch sizes range from 1 to 100. To analyze if the operator is compute bound or memory bandwidth bound, we can do some simple calculations as in Equation (7).

\[ T = \max(T_{\text{comp}}, T_{\text{mem}}) = \max(\frac{2mnk}{FE}, \frac{4kn}{B}), \]  

where T is the total latency for the operator, T_{\text{comp}} is the compute latency, and T_{\text{mem}} is the memory read latency assuming the parameters are stored in fp32. The operator is to multiply a m-by-n input matrix with a n-by-k weight matrix. Assume the peak flops of the system is F, memory bandwidth is B and compute efficiency is E, which is limited by how well instructions map to issue ports. The operator becomes memory bandwidth bound when T_{\text{comp}} < T_{\text{mem}}, leading to the criteria on batch size m < 2FE/B. For example, on Intel Broadwell CPUs, we have roughly F = 1Tflops, E = 90%, and B = 70GB/s. Hence, the criteria is m < 2 \times 900/70 \approx 25. Looking at the typical batch size distribution in Figure 4, 44% of the FCs use batch size 1. And 86% of operators use a batch size smaller than 25.
Therefore, we want to use low precisions to first mitigate the memory bandwidth overhead, and then improve the compute efficiency after the workload is moved to the compute bound regime.

**Fp16**: CPUs do not support fp16 compute and some do not even support it as a storage format. We therefore handcrafted software to convert and pack/unpack between fp16 and fp32. Loading fp16 weight parameters at runtime is 2X faster than loading fp32 ones for memory bandwidth bound cases. Down conversion and prepacking the weights into fp16 only happens once offline and incurs little runtime overhead. The precision for the input and output activations stays in fp32. Our fp16 compute kernels are also released as part of the FBGEMM library [5]. Fp16 is one of the highly programmable solutions with little accuracy impact on the model inference, so we have used it for all the recommendation models on CPUs in Facebook datacenters.

**Int8**: Reducing the weights’ precision to int8 can further mitigate the memory bandwidth demand. The 4X bandwidth savings from fp32 to int8 can effectively translate to end-to-end latency reductions for memory bandwidth bound cases. Moreover, as both CPUs and hardware accelerators have native support for int8, we can achieve efficiency wins for compute bound cases as well. To achieve the compute savings, we need to quantize both the weights and activations into int8 and use optimized int8 compute kernels. Weights can be statically quantized and prepacked, but the quantization of the activations needs to be done at runtime. To reduce the runtime overhead, we usually choose the quantization parameters for activations beforehand based on the training data, which is referred to as static quantization. In contrast, dynamic quantization chooses the quantization parameters on the fly, which may incur extra runtime overhead but could adapt to the input data distribution changes during online training.

Although int8 quantization has the potential to deliver much higher efficiency wins (2-4X on CPUs and an order of magnitude higher on hardware accelerators), delivering sufficient inference accuracy on int8 quantized models is more challenging.

As a result, we have explored many different options for the int8 quantization of MLPs. The best quantization algorithm varies for different cases but empirically the L2-error minimization algorithm is more effective for activations and the default min-max algorithm works well for weights. Beyond that, per-channel quantization on weights can further improve the quantization accuracy in cases where the weight data distribution varies across output channels. P99 quantization is effective when the raw data’s range is large only because of some outliers. Equalization techniques can also help in such cases. Moreover, we use the per layer L2-norm quantization errors to guide the quantization exploration at the model level. We forgo quantizing certain layers, so called “skipping them”, if not doing so leads to high quantization error. Figure 5 shows one example of heuristically exploring the quantization schemes on continuous snapshots of a production model and the effectiveness of the schemes in reducing the accuracy gap. The default scheme baseline denotes min-max quantization for weights and activations of FCs.

After choosing the quantization schemes at the operator level, we can further optimize the accuracy and performance at the graph level. Operator fusion is one graph level optimization to improve quantization accuracy. As we have discussed earlier, a FC followed by a Relu can be fused into one operator whose output range is reduced to only the positive part. Furthermore, we can optimize the quantized model graph from the performance perspective. Quantize and Dequantize operators are inserted around the int8 operators during the quantization transformation, but these operators will introduce extra performance overhead. So, we try to fuse the quantization operators with the adjacent operators e.g. Dequantize → Sigmoid → Quantize when the non-linear activation functions need higher precision. However, to mitigate such overhead, we want to avoid switching numeric precisions in the middle of the model unless necessary. Skipping the last FC in the int8 quantization is common since it does not need extra Quantize or Dequantize operators and the last FC is usually sensitive to the quantization errors.

Unfortunately, there is no easy or clear rule of thumb in identifying the best quantization techniques for all models. Thus, automating the exploration of appropriate techniques and support for numeric debugging are important; Section IV discusses the tools we developed to enable them.

### E. Low-precision strategies on inference accelerators

For hardware accelerators, more optimizations can be done based on the specific numerics support on them. We have been collaborating with Vendor-X to deploy their inference accelerators in Facebook datacenters. The Vendor-X accelerators feature large on-chip memory and high memory bandwidth which increases inference performance of our recommendation models according to the previous analysis in [II-C] and [II-D].

1) **Numerics support on accelerators**: The major numeric formats supported in each compute unit of the accelerator are marked in Figure 1. We try to utilize the int8 and fp16 arithmetics in the matrix core as well as the vector core from where the efficiency gains will mainly come. Fp32 on the general-purpose core is the backup when there are new operators in future models that are not supported in the high-performance units.

![Fig. 5: Accuracy impact of different quantization schemes](image-url)
On the vector core where most of the element-wise and non-linear operators are being executed, fp16/int8/int16/int32 are supported to provide high programmability. One limit is that the accumulator for fp16 multiplications is only in fp16, not fp32. This limitation necessitates comprehensive tests to ensure end-to-end accuracy being preserved. For non-linear operators, the vector core supports specialized kernel implementations based on lookup tables and linear or quadratic interpolation. On the matrix core, there are systolic MAC arrays with fp16/int8/int4/int2/int1 arithmetics and FMA (fused multiply-add) support. Accumulation into fp32 is supported for fp16 multiplications, which is proved important to the accuracy of MLPs in recommendation models.

2) Model co-design: The customized accelerators can provide 10X or even higher compute throughput compared to general-purpose CPUs. To fully leverage the high compute power, we need to rethink what kind of models we should run on the accelerators to achieve efficiency wins as well as boost learning accuracies. One general direction is to increase the compute flops for model inference. For example, one of our complex models has 5X more flops than the original model running on CPU. In particular, the FullyConnected operators are wider with more weight parameters and occupy a much higher percentage of the overall inference latency. This greatly increased complexity indeed results in a model with much higher prediction accuracy, but one that would not meet our response time constraint if deployed on CPUs. Deployment on accelerators is a solution provided we can leverage the fast low-precision arithmetic (e.g. fp16/int8), as the low-performance fp32 is also inadequate in this aspect.

3) Low-precision strategies on Vendor-X accelerators: According to our internal performance model on the accelerator, similar to the situation on CPUs, FullyConnected operators and SparseLengthsSum operators also dominate the inference latency so they remain the focus of our numerics and performance optimizations.

**Fp16/Int8 for MLPs:** As both int8 and fp16 are supported in the matrix core, we improve the MLP strategies as follows: Start with leveraging int8 quantization on as many FullyConnected operators as possible. However, if an operator causes very high quantization errors, we fall back to fp16 for that operator and insert Dequantize and Quantize operators around it. The fp16 fallback on the accelerator is not the same as the fp16 on CPU because in addition to storing weights in fp16, we exploit the fp16 arithmetic support on the accelerators to achieve a much higher performance. To guarantee inference accuracy, we found fp32 accumulation is important for the FullyConnected operators. Otherwise, \( \text{NE}_{\text{diff}} \) for some recommendation models can exceed 0.05%. Nevertheless, provided the accuracy constraint is met, exploiting int8 on as many compute intensive operators as possible is important because its throughput is several times higher than fp16.

**Fp16 for SparseLengthsSum and other operators:** The embedding tables are stored in the same numeric format as on CPU to save memory capacity and bandwidth. For the reduction operation in SparseLengthsSums, we choose fp16 because compute is not the bottleneck as it is in MLPs and fp16 provides higher accuracy than int8 does. The SparseLengthsSum operators can thus run on the vector core. We have verified that fp16 accumulation in the vector core is sufficient to meet the end-to-end accuracy requirement. Nevertheless, having fp32 accumulation support would have saved significant validation effort. We also apply fp16 to a wide range of other operators due to its high programmability, including BatchMatMul, Sigmoid, Swish, Quantize, Dequantize, etc. The BatchMatMul operator contributes to the overall inference latency quite noticeably and we could benefit much by quantizing it. This is currently not feasible due to the operator’s inputs consisting of dynamic matrices and that the accelerator does not provide a specialized int8 kernel. This lack can in theory be fixed in the future.

**Graph level optimizations:** Unnecessary switches between numeric precisions result in high overhead because different precisions may need to be processed in different hardware units. In general, we want to apply fp16/int8 to as many operators continuously as possible so that we can maximize the efficiency wins from the high throughput matrix core.

4) Numerics validation: In addition to exploring the best low-precision strategies for our models, a unique challenge of deploying the models on accelerators is to validate that the numeric behaviors of the model inference on the hardware are as expected. Validation is particularly important when the kernel implementations for the hardware from the vendor are not fully transparent. Moreover, the implementations from the vendor could change in different software releases. Although some changes originate from performance optimizations, we need to verify that the numeric behaviors are still correct and consistent after each software release.

To validate numerics, we have numeric reference implementations from our side to match with the vendor’s implementations deterministically including the accumulation order, and then compare the inference results of our reference implementations with the hardware. Since there are usually graph optimizations and fused operator groups for performance, we also run the model inference end-to-end to match the bit-wise accuracy for the full model. We expect bit-wise accuracy at both the net-level and operator-level, including all the fundamental operators in our recommendation models and commonly used fused operator groups. Bit-wise accuracy matching has been challenging but worth to do to avoid debugging quantization error propagations which could be harder to track. To facilitate the validation process, we have open-sourced our reference implementations and unit tests [30] so that the vendor can perform the tests independently after each software release.

After our comprehensive validation testing against hardware, our reference implementations can serve as a proxy to reflect the device and enable efficient emulations on CPU. Then, we run large-scale evaluations with production traffic and compare the end-to-end accuracy in NE with the CPU baseline. The emulation maps all the CPU operators to refer-
ence operators on the accelerator and then run the two models with the same traffic. If the \( NE_{\text{diff}} \) is larger than a threshold, we need to locate the operator that caused the gap and create a repro for the vendor in order to fix the issue in the next software release.

IV. TOOLING SUPPORT FOR REDUCED PRECISION OPTIMIZATIONS

With increasing model size and complexity in recommendation models, finding the best quantization strategies for a specific model becomes challenging and often requires much debugging effort during the search. The quantization workflow also needs to handle a variety of production recommendation models aiming at many different tasks. Moreover, recommendation models are usually online trained, and data distribution changes during online training, which can affect the accuracy of specific quantization scheme. Thus, it becomes prohibitive to manually quantize and debug the accuracy issues model by model. To meet these challenges, we developed a suite of tools to help automate the quantization and debugging process. This section first introduces the typical life cycle of models with int8 FCs, and then discusses the tools we have developed to optimize, debug, and monitor the accuracy of int8 recommendation models throughout their life cycle: automatic quantization workflow, numeric debugger, and continuous accuracy monitor. In this section, int8 models denote models with FCs quantized in int8 that need sophisticated flow and tools, while we found that embedding table quantization works well with a fixed scheme.

A. Int8 Recommendation Model Life Cycle

A typical Int8 recommendation model life cycle involves three major stages: offline experimentation, online experimentation, and model launch.

1) Offline Experimentation: We first do offline experiments, where we quantize the models with various quantization schemes, and then measure offline NE differences of the int8 models from the original fp32 model. This gives us signal on how int8 models perform over the fp32 baseline and helps us choose candidate int8 models for online experiments. This stage uses the automatic quantization workflow to explore various quantization schemes and the numeric debugger to deep dive into the per-layer quantization errors when the accuracy cannot meet the requirement.

2) Online Experimentation: In the next stage, we put the int8 model obtained above to an A/B test. In the A/B test, a small portion of real-time production data flows to the int8 model instead of current production model so that we can compare the end-to-end serving quality. The fp32 model from where we quantize the int8 model is undoubtedly more accurate than current production model but int8 quantization may introduce accuracy loss. The A/B test allows us to judge if the accuracy gain or performance-accuracy trade-off given by the int8 model warrants its deployment. This step uses the continuous accuracy monitor to observe the accuracy of all the int8 model snapshots during online training and uses numeric debugger for troubleshooting whenever the accuracy drop exceeds the accuracy tolerance. We have encountered more subtle accuracy issues during online experiments than offline because of data distribution shifts. Numeric debugger is very useful as it helps resolve these issues by inspecting the weight/activation distributions, analyzing outlier inputs, and emulating alternative quantization schemes that reduce quantization errors.

3) Model launch: If the performance and accuracy of the int8 model in the online experiments meet our launch criteria, we roll out the int8 model into production to serve 100% of real-time data. The continuous accuracy monitor is used to guard against model accuracy degradation caused by changes of data distributions, and the numeric debugger will be used when accuracy degradation is considered too large.

B. Automatic quantization workflow

The automatic quantization workflow is an iterative search for a good quantized model among a vast number of candidates. The flow automates data preparation, histogram collection, quantization scheme search, int8 model transformation, accuracy evaluation, per-layer quantization error measurement, and so on. A model candidate’s speed and accuracy in a current iteration are assessed and its quantization scheme is further refined if needed. Figure [6] shows this workflow. The search comprises of two main stages as follows.

1) Global Quantization Scheme Search: During this stage, weights and activations in all the layers use the same quantization scheme any given time, hence the name global. This greatly reduces the search space by avoiding exponential combinations of varying schemes at each layer. An example global quantization scheme is L2 error minimization algorithm with asymmetric quantization for each layer and skipping the last layer. We enumerate combinations and measure the accuracy as follows. For each global quantization scheme, the model is transformed into an int8 model and evaluated on a small evaluation dataset. The scheme that provides the highest accuracy will be selected as the best global quantization scheme. If the accuracy loss is acceptable, then the int8 model is saved and the quantization process stops. Otherwise, we proceed to the second stage.

2) Iterative Quantization Scheme Search: We identify the layers with the highest per-layer quantization errors. Then, we
apply techniques that can potentially improve the accuracy such as channel-wise quantization on weights and p99 on input/output activations for a layer. If the accuracy is still not good enough, we skip quantizing this layer. The stopping criteria of the iterative search is based on the accuracy loss and the percentage of compute flops we need to skip. When percentage is high, the performance gain from the int8 quantization becomes marginal hence we stop the search.

Two small datasets are used to make the search time manageable: a calibration dataset, sampled from the training data, is used for histogram collection and quantization parameter calculation; an evaluation dataset, sampled from the offline evaluation data, is used for accuracy measurement. After getting an int8 model with satisfactory accuracy on the small evaluation dataset, we then check the accuracy on full evaluation dataset. If accuracy gap happens between the two evaluation datasets, we draw more samples in the small datasets and repeat the quantization scheme search.

C. Numeric debugger

Debugging numerical accuracy issues must be carried out quickly as there are many production models, all updated frequently. The sizes of these models and the related dataset pose a great challenge as merely loading them can take hours. Another challenge is that we aim to identify the root cause of accuracy drop as oppose to finding superficial temporary fix. This will help us accumulate effective measures for accuracy restoration over time. The debugging methodology we adopted is shown in Figure 7 and discussed in detail below.

1) Reproduce NE_{diff} on a small dataset: When the accuracy drop is beyond the prescribed threshold, we first try to reproduce the results with a small dataset, which we can save locally to quickly iterate on debugging in a deterministic way.

2) Identify the inputs that correspond to large accuracy drops: We further narrow down by sorting the small dataset based on per sample error. We calculate the cross entropy error for each sample based on the predictions from the low-precision and original models. The samples are then sorted by the cross entropy errors in descending order. The top samples contribute the most to the accuracy loss in normalized entropy (NE) as the NE_{diff} is basically a summation of the cross entropy errors of all samples divided by a normalizer. With only a few samples, it is much easier to debug and understand the accuracy loss.

3) Identify the operators that are responsible for accuracy drop: We narrow down to a few operators based on their quantization error when running with the problematic input. In this run, a shadow fp32 operator is executed for each low-precision operator with the same input. The difference in outputs is calculated as the quantization error in this layer. The quantization error is used to sort all the operators in order to locate the top problematic operators, which are often responsible for the global accuracy drop.

4) Root cause analysis and resolution: After we reduce the problem size and narrow down to a few inputs and operators, we try to identify the root cause by profiling the distribution of input, output, and weight values of the problematic operators. Based on the profile, we may need to add advanced options in the quantization scheme search space, debug the kernel implementations, validate the kernels on target hardware, etc. in order to fix the accuracy problem. If still not successful, we need to incorporate other techniques such as quantization aware training [20][33][38], equalization [46], or model co-design.

5) Validation: We validate the root cause and fix on the saved local dataset, and then on the full evaluation dataset if the accuracy is good. If there is an accuracy gap between the local and global evaluation datasets, we increase the number of samples in the local dataset and repeat the previous quantization scheme search until the accuracy is good on the full evaluation dataset.

Our numeric debugger enables the above methodology by providing a numeric analysis toolkit and supporting utilities such as dataset extraction and embedding table shrinkage. It is open sourced and also included in PyTorch 1.6 release [10].

D. Continuous accuracy monitor

Our continuous accuracy monitor ensures that the quantization scheme developed for a particular model maintains good accuracy for all online retrained snapshots of the latter. The tool quantizes every snapshot and evaluates the fp32 and int8 models side by side, in order to proactively identify accuracy issues to avoid prolonged degradation of service quality. The evaluation results are logged to a Scuba [14] table so that we can visualize the time series of the accuracy metrics and identify when the accuracy starts to degrade. To diagnose the accuracy degradation, we need the numeric debugger together with the information from the continuous accuracy monitor to locate the problematic model and input data.

In addition, we also support the int8 emulation for Vendor-X accelerators in this workflow to compare the two model runs using the accelerator emulation kernels and CPU kernels side by side. The statistics on the NE_{diff} and per-layer quantization errors can guide the numeric validation process and help locate bugs in the kernel implementations.
V. Lessons Learned

We summarize here the important lessons on low-precision architectures and the hardware-software co-design process we learned. These lessons are accumulated during our long journey in deploying production models in conjunction with hardware vendors refining their platforms.

- **Enhanced Integer Quantization Support**: Computation with int8/int4 provides significant performance gains but we rely on the various quantization techniques to meet our accuracy requirements. Hardware support for these techniques such as asymmetric quantization, fine-grain per-channel quantization and dynamic quantization are important, but not all supported at present.
- **Balanced Floating-Point and Integer Performance**: We prefer good/balanced performance on low-precision floating-point compute such as fp16 or bfloat16 to resources devoted to extreme-low-precision integer performance at the 1 or 2-bit realm. Low-precision floating-point has been the easiest fallback for network layers of high numerical sensitivity, allowing us to meet our accuracy constraints.
- **High-Capacity and Bandwidth Memory**: We foresee the need for large-input-dimension FullyConnected operators in MLPs which help mitigate the effect of quantization errors. Large on-chip and/or high-bandwidth memory will greatly facilitate this.
- **Accurate Non-Linear Functions**: We see high sensitivities to quantization errors in non-linear activation functions such as Sigmoid, Swish, etc. when their input ranges are not covered sufficiently. Enough coverage is important despite the needed slight increase in LUT size and the associated increase of real estate and power consumption.
- **More Optimized Low-Precision Kernels**: Some important and compute heavy operators such as BatchMatMul in existing and emerging models are not supported at the hardware level.
- **Co-Design Support**: Open-source numeric reference implementations from vendors can greatly save engineering effort on the numeric validation of the kernel implementations for the accelerators.
- **Beyond Hardware and the Model**: The tool chains that automate quantization and facilitate debugging is important to the success of deploying low-precision models. They are a major undertaking: any project planing on model deployment need to take that into account.

VI. Related Work

Increasingly complex learning models spur great interest in academia and industry on exploiting low-precision arithmetic to boost inference efficiency. Most of the many academic works on quantization focus on computer vision [25,31,33,38,46,53,57] or natural language processing models [15,57,61,62]. There are several open-source libraries from industry that support low-precision numerics for model inference. Notably, Google open sourced its gemmlowp [7] library for 8-bit matrix multiplications. NVIDIA released its TensorRT [13] library which supports both fp16 and int8 optimizations for GPU inference.

In the meantime, ubiquitous deep-learning applications have also motivated novel deep-learning friendly hardware designs. New features are added to traditional hardware platforms. For example, Intel added bfloat16 [1] as well as VNLI (Vector Neural Network Instructions) [9] in their latest CPU series. NVIDIA Tensor Core supports both fp16 and int8 to achieve higher inference throughput [42]. A variety of AI accelerators [2,34] with high compute throughput and power efficiency are designed to speed up DL models.

On recommendation models in particular, DLRM [47] is representative of Facebook’s deep learning recommendation models. It has also been adopted by the industry-wide MLPerf benchmark suites [43,44,49,56]. Recent works [23,24,29,48] presented in-depth system performance characterization studies and shared the architectural implications for additional optimization opportunities. Our work here demonstrates a hardware-software co-design in action on deploying production-scale recommender systems to low-precision hardware architectures. We also make a number of recommendation-model-specific suggestions on hardware architectures based on our work “in the trenches.”

VII. Conclusion

This paper shared the techniques and software tools we developed for deploying production recommendation models in Facebook datacenters to exploit low-precision arithmetic of both CPUs and accelerators. We learned a number of important lessons and made some concrete suggestions to hardware architects designing for large-scale recommendation models and to software engineers deploying these models.

The work described here can be classified as post-training quantization to low precision. We are exploring several other threads. One is quantization aware training (QAT), which tries to obtain through the training process an easy-to-quantize or already-quantized model (cf. [19,33]). Model pruning is a technique orthogonal to quantization, but a pruned model yields the same resource saving benefits a quantized model gives. Along this line, knowledge distillation from a complex teacher model to a pruned student model may maintain the needed accuracy produced by the latter. Agile sparsity adaptation techniques are also needed for pruning to be effective as data distribution can change significantly during online training [59].

From the hardware-software co-design perspective, we cannot over emphasize the benefits of both parties open sourcing [39] important building blocks of their design and code: making these accessible allows continuous validation of hardware functionality and numerical correctness, greatly shortening the entire development cycle. Co-design does not end when a hardware platform is fully designed or made available: as new software algorithm will be developed to exploit new architecture, whose follow-on version in turn will adapt to the more influential ones of these new algorithms.
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