A Pathway to Thin GaAs Virtual Substrate on On-Axis Si (001) with Ultralow Threading Dislocation Density

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With recent developments in high-speed and high-power electronics and Si-based photonic integration, the concept of monolithic III–V/Si integration through epitaxial methods is gaining momentum. However, the performance and reliability of epitaxially grown devices are still limited by defects in the semiconductor material, especially the threading dislocation density (TDD). Herein, a novel “asymmetric step-graded filter” structure grown by molecular beam epitaxy (MBE) is proposed based on a systematic study of the commonly used techniques for threading dislocation reduction for high-quality GaAs on Si (001) growth. The proposed structure greatly enhances the plastic relaxation in the filter layers. A surface TDD lower than $2 \times 10^6 \text{ cm}^{-2}$ is achieved with a total buffer thickness of only $2.55 \mu\text{m}$. This provides a clear pathway to further reduce defect density down to the theoretical limit in the $10^5 \text{ cm}^{-2}$ regime with a thin buffer structure.

1. Introduction

The arrival of the Zettabyte era has boosted the rapid development of on-chip signaling and processing devices. Si-based waveguides, modulators, and detectors have been extensively investigated over the past decade for photonic integrated circuits. But due to the indirect bandgap nature of Si, the most challenging problem for full integration is realizing a reliable, high-performance on-chip light source. Various approaches have been taken, including a stimulated Raman scattering laser, erbium-doped laser, germanium epitaxial laser, and III–V based laser. Due to the direct bandgap structure of III–V semiconductor materials, a III–V on Si laser still shows the highest performance and is the most practical candidate for an on-chip light source. In addition to the direct bandgap structure, the lower effective masses and higher carrier mobility of III–V materials also render them more suitable for high-speed electronic devices than bulk Si as well.

Hybrid integration based on copackaging, heterogeneous integration based on wafer or die bonding, and direct epitaxial growth are the three main integration approaches for III–V on Si. Heterogeneously integrated lasers currently exhibit the highest performance for light sources on Si and have been commercialized for mass production. III–V compound semiconductors have also been explored as the candidate for the new channel material in high-speed electronic devices, as a means to circumvent the scaling limit of bulk Si. Yet, both applications suffer from the high cost and small size of the III–V wafers. However, the direct epitaxial growth of III–V material on Si could be utilized for the benefit of large wafer sizes, lower costs, and better thermal conductivity of Si relative to heterogeneous silicon-on-insulator platforms. The main problem with direct epitaxial growth is the dissimilarity between III–V materials and Si. Antiphase domains (APD) can form when growing III–V material on on-axis Si (001) due to the polarity mismatch. This problem has largely been solved with various approaches, ranging from highly optimized Si wafer preparation and well-controlled initial III–V nucleation to the use of patterned Si with exposed high index surfaces. A large thermal expansion coefficient mismatch may result in surface cracking during the post-growth cooling process. This problem can be mitigated with lower cooling rates, careful sample cleaning prior to growth, and better design of sample holders.

The most detrimental and yet unsolved issue of direct epitaxial growth is the high density of threading dislocations originating from the high lattice constant mismatch. Various methods have been explored to reduce the threading dislocation density (TDD). Inserting buffer layers with strained dislocation filter layers (DFLs) and thermal treatments during or after buffer growth have been two of the most successful methods. Thermal cyclic annealing (TCA) is known to be an effective technique for reducing the TDD for GaAs films grown on Si substrates. Due to the thermal expansion mismatch between Si and GaAs, which is about 3 ppm K$^{-1}$, temperatures above or below the GaAs film growth temperature generate additional compressive or tensile stress, respectively. The induced thermal stresses promote the lateral motion of the existing TDs in the GaAs film and the attachment.
probability of TD interaction is then increased, which could potentially lead to TD reduction and annihilation. DFLs promote the lateral motion of TDs through plastic relaxation within the intentionally lattice-mismatched layer. Different DFL structures and materials have been studied extensively.\[21,22\] More recently, several groups have demonstrated successes in TDD reduction with the use of multiple strained layer superlattice (SLS) structures as DFLs.\[23–25\] Combined with InAs quantum dots as the active region, high-performance light sources epitaxially grown on Si have been demonstrated.\[18,26,27\] The reliability of the InAs quantum dot (QD) laser grown by molecular beam epitaxy (MBE) emitting around 1.3 μm grown on Si (001) has a strong and monotonic exponential dependence on the TDD of the GaAs-on-Si virtual substrate. Previous reports indicate that the extrapolated time required for doubling the initial threshold current at room temperature increases from about 800 h to more than 10 000 000 h as the TDD decreases from 2.5 × 10^6 cm^−2 to 7.6 × 10^6 cm^−2. The extrapolated lifetime at elevated temperatures for normal operating conditions in data centers is still poor compared with the devices grown on native GaAs substrates. Further reducing the TDD for epitaxially grown GaAs-on-Si virtual substrates is still of great importance and yet becomes increasingly challenging at low TDD levels as the likelihood of two TDs interacting with each other becomes extremely low. The theoretical lower limit of TDD for any heteroepitaxial structure is about 290 10^6–10^7 cm^−2. A TDD of 1.2 × 10^6 cm^−2 has been obtained on an off-cut Si wafer with 4 μm buffer thickness\[30\] and a TDD lower than 10^5 cm^−2 has only been achieved with thick and fully relaxed compositionally graded layers.\[31\] Yet, neither of these is ideal for practical applications due to the buffer thickness and wafer orientation.

As MBE-grown materials hold the record performance for epitaxially grown III–V/Si devices, we report a systematic study on the efficiency of TCA processes and InGaAs DFLs in reducing the surface TDD of the GaAs-on-Si buffer grown on a GaP/Si (001) template under typical MBE growth conditions. The efficiency of the DFL depends strongly on the indium composition and degree of relaxation. An “asymmetric step-graded filter” structure is proposed to further promote relaxation, ultimately achieving a surface TDD as low as 2 × 10^6 cm^−2 with a total buffer thickness of only 2.55 μm. The “asymmetric step-graded filter” provides a pathway to obtaining a thin GaAs-on-Si buffer with TDD in the 10^5 cm^−2 regime, where the extrapolated lifetime of the device grown on Si is expected to be comparable with those grown on native GaAs substrates, especially at elevated temperatures. Even at a TDD of 2 × 10^6 cm^−2, the extrapolated lifetime of the device grown on Si is expected to be more than 100 years at 60 °C.

## 2. Results and Analysis

### 2.1. TCA investigation

The effect of higher-temperature thermal annealing on the defect level in GaAs films grown on Si (001) has been studied by several groups. A higher annealing temperature results in a higher compressive strain in the GaAs layer which leads to fewer cycles for the same threading dislocation reduction.\[20,32,33\] GaAs surface quality can also be significantly improved.\[34\] Yet, previously reported annealing temperatures are either thermocouple target temperatures or ambient temperatures in the furnaces. The TCA temperature limits have not been fully explored for an in situ MBE chamber with pyrometry-based temperature measurement and arsenic overpressure. Figure 1A shows the TDD measured on top of the GaAs film after different TCA processes. The GaAs film was grown at 580 °C. The thermal mismatch strain can be calculated with the following equation.

\[
e_{\text{thermal}} = \int_{T_g}^{T_{\text{max}}} (\alpha_f(T) - \alpha_s(T))dT
\]

where \(\alpha_f\) and \(\alpha_s\) are the temperature-dependent linear thermal expansion coefficient of the film and the substrate, respectively. Both \(\alpha_f\) and \(\alpha_s\) can be approximated to be linearly dependent on \(T\) within the temperature range of interest.\[35,36\] \(T_g\) is the growth temperature and \(T_{\text{max}}\) is the annealing temperature.

By increasing the temperature to 700 °C, an additional 0.037% compressive strain was introduced due to the thermal expansion mismatch between GaAs and Si, which in turn generated a biaxial compressive stress of about 70 MPa. Thus, the TDs would move at a velocity of approximately 1 mm s^−1 at 700 °C, according to the dislocation velocity measured in GaAs.\[37\] During the

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**Figure 1.** A) TDD of the post-TCA GaAs-on-Si template. The minimum TDD achievable via TCA at the given GaAs thickness is about 3 × 10^5 cm^−2. B) Nomarski microscope image of the GaAs surface after annealing above and below 745 °C pyrometry temperature. Gallium droplets are observed when \(T_{\text{max}}\) is higher than 745 °C. C) ECCI images of the as-grown GaAs with no TCA (top) and after 16 cycles of TCA (bottom). The TDD is about 4.18 × 10^6 cm^−2 with no TCA and decreases to 3 × 10^6 cm^−2 after extensive TCA.
hold time of 5 min, the TDs should have enough time to move across the entire wafer (2 cm by 2 cm). As the thermal mismatch is small, we expected that only a small portion of the existing TDs has to move to relax the thermal stress. Thus, the full cycling process including the low-temperature step is required to re-establish the thermal stress in each cycle. Only glissile TDs can move under the induced thermal stress.

The glissile TDs can either react with existing TDs, glissile or sessile, or propagate to the edge of the wafer and exit the crystal, in both cases reducing the TDD. It was previously discussed\(^ {29} \) that the reactions between the TDs in a zinc-blend crystal maintain a glissile versus sessile ratio of 1:1, and this has also been experimentally observed.\(^ {38} \) Therefore, the supply of glissile TDs does not quickly run out. Thus, the plateauing of the TDD with respect to the number of cycles is primarily due to work hardening as the misfit dislocations (MDs) at the GaAs/Si interface elongate in each cycle.

Figure 1A shows that additional cycling produces a minimum reduction of TDD after 12 cycles. Increasing the maximum annealing temperature to 735 °C generates a thermal mismatch strain of 0.049%, which translates to about 93 MPa of bilateral compressive stress. With higher stress, a similar TDD reduction is achieved at 4 (or 8) cycles as with 8 (or 12) cycles of lower thermal mismatch stress. We then expected that the plateau can be reached much sooner if the annealing temperature is sufficiently high. Yet, when the annealing temperature is above 745 °C, the GaAs surface quality degrades catastrophically, as shown in Figure 1B.

The surface TDD after applying DFLs depends on the TDD on the post-TCA GaAs surface (Figure S1, Supporting Information). To ensure reproducibility, all GaAs on Si samples that were used for further filter layer studies have a surface TDD of 3 × 10^7 cm^-2. This is referred to as the GaAs-on-Si template in later sections.

2.2. Defect Filter Efficiency

The technique of using strained-layer structures as DFLs has been widely applied. An SLS is the most commonly used structure in GaAs-on-Si buffer layers.\(^ {24, 25, 39} \) The idea of using alternating signs of misfit strain is to enhance the probability for dislocation interactions as the threading segments move back and forth.\(^ {40} \) The first use of SLS as DFL was proposed by Matthews and Blakeslee with GaAs\(_{0.5}\)P\(_{0.5}\)/GaAs superlattice.\(^ {41, 42} \) The design parameter space for optimizing the effectiveness of SLS is huge, including strain state and thickness of each period, total number of periods, thickness ratio of the two alternating materials in each period, and growth conditions. InGaAs/GaAs SLS was found to be more effective than GaAs\(_{0.5}\)P\(_{0.5}\)/GaAs when grown on a 2 μm-thick InGaAs buffer layer on the native GaAs substrate.\(^ {43} \) The difference was attributed to a larger interlayer strain and elastic constant difference despite the fact that the signs of the initial strain were also different. The SLS structure with lattice-matched alternating layers in each period was found to be effective in dislocation filter as well, though a minimum strain between the alternation layers was expected.\(^ {43} \) While such layers with alternating strain undoubtedly have a role to play in blocking new TDs from possible spiral or Frank-Read multiplication sources,\(^ {44} \) it is not very clear if they help in enhancing existing TD–TD reactions and annihilations. Hull et al. show that SLSs in SiGe on Si do not perform any better than a single composition layer with the same average composition in terms of relaxable strain energy.\(^ {45} \) This may be more pertinent in MBE growth given the sluggish relaxation kinetics at 500 °C. Here, we have investigated the efficiency of the InGaAs DFL as an example based on the growth conditions, indium composition, and structure.

2.2.1. Efficiency of InGaAs/GaAs SLS

We compare InGaAs/GaAs SLS structures with varying periods tending toward a constant composition layer with the same equivalent average strain. InGaAs/GaAs SLS structures with lattice-matched alternating layers were grown on the GaAs-on-Si template with a TDD of 3 × 10^7 cm^-2, with x taking the values of 10, 7, 5, 2, and 0. The structure is capped with 300 nm of GaAs. The results are shown in Figure 2 (the case for x = 7 nm is not shown).

The observed TDs on the surface are circled in the electron-channeling contrast imaging (ECCI) images. The filtering efficiency is improved significantly with a thinner GaAs layer in between the InGaAs/GaAs layers, with the continuous 200 nm InGaAs/GaAs having the highest efficiency. The efficiency of the filter layer depends on the degree of relaxation, especially the degree of relaxation of the InGaAs layer. It can be seen from both the ECCI images, Figure 2A–D, and the Nomarski images, Figure 2E–H, that the surface crosshatch pattern becomes more prominent as the x value decreases to 0. Only very mild surface crosshatches can be observed with the InGaAs/GaAs structure. Faceted trenches (FTs) can be observed in the x = 2 and x = 0 cases. Both the more prominent surface crosshatch pattern and the formation of FTs qualitatively suggest a higher degree of relaxation in the single InGaAs/GaAs layer.\(^ {46} \) The reciprocal space maps (RSMs), centered around the GaAs (224) peak, of the SLS structures are shown in Figure 2I–L. The degree of relaxation, R, is defined as

\[
R = \frac{a_l - a_s}{a_l} \times 100\%
\]

where \(a_l\) is the in-plane lattice constant of the substrate, which is that of GaAs in this case (5.653 Å), \(a_s\) is the in-plane lattice constant of the InGaAs layer if it is fully relaxed (5.714 Å) and \(a_l\) is the measured in-plane lattice constant of the InGaAs layer, which can be extracted from the RSMs.

Figure 3 shows the surface TDD and relaxation of the SLS structures. The relaxation for the as-grown InGaAs/GaAs (10 nm)/GaAs (10 nm) structure is only 17.6%, which increases to 44.6% as the GaAs layer thickness decreases to 0 nm. These relaxation values match well with the previously reported data.\(^ {46} \) The surface TDD simultaneously decreases from 1.3 × 10^7 cm^-2 to 2.1 × 10^6 cm^-2. Thus, the degree of relaxation in the InGaAs/GaAs (10 nm)/GaAs (x nm) DFL has a direct and significant impact on the filtering efficiency, though a mild diminishing return is observed.
The schematics in Figure 4A–F qualitatively show the relaxation process in an SLS structure. Here positive strain values are used to denote compression and the initial mismatch strain between In$_{0.15}$Ga$_{0.85}$As and GaAs-on-Si template is denoted as $\epsilon_0$. Though the calculated Mathew–Blakeslee critical thickness is about 9 nm, the thickness required for significant plastic relaxation can be much larger, and this thickness is found to be about 100 nm under our MBE growth conditions. Thus, the first few periods of the SLS are close to fully strained with respect to the GaAs-on-Si template and the TDs from the GaAs-on-Si template propagate continuously, as shown in Figure 4A,B. After reaching the thickness required for significant plastic relaxation in the In$_{0.15}$Ga$_{0.85}$As layers, all layers within the SLS structure relax together and the TDs move to relax the compressive mismatch strain, as shown in Figure 4C,D. The GaAs layers in between the In$_{0.15}$Ga$_{0.85}$As layers would then be under tension. Segments of the TDs in the GaAs layer would then experience a force opposite to the preferred propagation direction in the In$_{0.15}$Ga$_{0.85}$As layers. As the SLS structure relaxes in response to the compressive strain, having segments experiencing opposite forces would hinder the relaxation process, given the finite growth time and dislocation velocity. As the accumulative tensile strain energy exceeds the value required for significant tensile relaxation, TD segments within the GaAs...
layers would prefer to move in the opposite direction as the segments in the In$_{0.15}$Ga$_{0.85}$As layers, which would further hinder the overall relaxation of the SLS structures, as shown in Figure 4. Thus, the thicker the GaAs in between the In$_{0.15}$Ga$_{0.85}$As, the less the relaxation, with In$_{0.15}$Ga$_{0.85}$As (10 nm)/GaAs (10 nm) being the worst case. It has been reported previously that SLS with intentional tensile layers is less efficient than the InGaAs/GaAs SLS.$^{[48]}$ Thus, having the tensile GaAs layer within an SLS structure degrades the filtering efficiency.

It is important to realize that SLS is not inherently worse than a single-layer filter. Tensile relaxation in the GaAs layer indeed is beneficial to TDD reduction, as discussed in Section 2.2.2. But to utilize the tensile relaxation benefit in a SLS structure, each layer within the SLS structure needs to relax...
significantly. This would require thick layers in each SLS period, as the thickness required for significant relaxation is about one order of magnitude higher than the Matthew–Blakeslee critical thickness.

2.2.2. Effect of Indium Content in the InGaAs DFL

Given that the single layers provide greater TD reduction for a given amount of average strain, we explore this further by testing the composition range over which we may increase the average strain while minimizing new multiplication. A higher average strain intuitively imposes a risk of work hardening for given thickness and forming FTs on the top GaAs capping layer due to the abrupt tensile relaxation, which has been observed in other tensile relaxed films. Around 200 nm single-layer InGaAs filters with 10%, 15%, 17.5%, 20%, and 25% indium composition were grown. The results shown in Figure 5A indicate that the TDD started to increase when the indium composition was higher than 20%.

Figure 5B shows an example ECCI image of 20% InGaAs samples. A clear “blocking” effect has been observed where some TDs are aligned parallel to the crosshatch pattern. The surface cross-hatch pattern is known to be the result of the underlying MD array. The interaction between the stress fields of perpendicular misfits may result in the “blocking” of the threading segment. The blocked TDs would then appear aligned with the surface crosshatch pattern. 300 nm GaAs capping layers were then grown on top of the InGaAs filter layer and the TDD is further reduced through the tensile relaxation in the GaAs capping layer. The formation of FTs was clearly observed in the top GaAs layer with the underlying InGaAs having an indium content higher than 15%, example shown in the inset of Figure 5A. The post-GaAs-cap TDD of the samples with indium content higher than 20% cannot be measured by ECCI due to the high density of FTs. Thus, the tensile relaxation in the top GaAs layer, which would cause TDs to move in the opposite direction as they do in the compressively relaxed InGaAs, is beneficial to TDD reduction. Yet, stacking multiple 200 nm single-layer InGaAs filters with 300 nm GaAs spacers in between does not result in further TDD reduction.

3. Proposed More Efficient Filter Structure

The previous three experiments ultimately lead to a defect filter strategy involving TCA and a quasi-single layer with compositional grading to minimize the formation of FTs and reduce the “blocking” effect. As discussed in the previous sections, the efficiency of the single-layer filter drops when the indium content is above 17.5%. Thus, the maximum indium content in the first proposed structure is limited to 10%. Single-layer InGaAs filters will be used as the building blocks for the proposed filter structure.

To have a DFL structure with a higher efficiency, a higher level of relaxation in the DFL is required. Here, we propose an “asymmetric step-graded filter” structure, as shown in Figure 6A. Graded filters are known to be helpful in promoting more efficient relaxation, as the “blocking” effect is reduced. The indium content is graded in steps up to the maximum value of 10%, with 5% increments in each layer, and then graded down to 0%. The layer thickness on the tensile side (after the layer with maximum indium content) is intentionally thicker as tensile relaxation is expected to be slower and may result in the formation of FTs. In the as-grown structure with 10% maximum indium content, the In$_{0.05}$Ga$_{0.95}$As layer is 80.2% relaxed and the In$_{0.10}$Ga$_{0.90}$As layer is 49% relaxed with respect to the GaAs-on-Si template. For the same structure where each InGaAs layer is subject to a 10 min annealing at 530 °C under arsenic overpressure and the growth is interrupted during the annealing process, the relaxation is further promoted to 88.9% and 58% for In$_{0.05}$Ga$_{0.95}$As and In$_{0.10}$Ga$_{0.90}$As, respectively.

The surface TDD measured in the annealed sample is $2 \times 10^4 \pm 2 \times 10^5$ cm$^{-2}$ at 95% confidence interval. An example ECCI image is shown in Figure 6B. 33% of all ECCI images taken, which cover a total area of about 2000 μm$^2$, are entirely free of TDs (Figure S2, Supporting Information). The RMS surface roughness of the top GaAs

![Figure 5](image-url)  
**Figure 5.** A) TDD measured before and after GaAs capping layer with a single 200 nm InGaAs filter. The TDD starts to increase once the indium composition in the InGaAs layer is above 20%. The inset shows an example Nomarski image of samples with more than 20% of indium in the InGaAs filter layer. No large enough clear regions for ECCI measurements. B) Example ECCI image of the sample with more than 20% indium in the InGaAs layer before GaAs capping. “Blocked” TDs are circled.
The surface is about 2.1 nm. Figure 7 shows the cross-sectional scanning transmission electron microscopy (XSTEM) and plan view scanning transmission electron microscopy (PVSTEM) images of the asymmetric step-graded filter structure with annealing. Both samples are prepared in the Helios 600 DualBeam workstation (FEI, USA) and imaged with a Talos F200X (Thermo Scientific, USA) at 200 kV with (220) and (220) two-beam diffraction conditions for the PVSTEM and XSTEM samples, respectively. The XSTEM in Figure 6A shows the clear asymmetric step-graded filter structure with a darker color, suggesting higher indium composition. Though MD arrays at the last GaAs/In_{0.05}Ga_{0.95}As interface are revealed in the bright-field PVSTEM in Figure 7B,C due to the tilt of the foil with respect to the sample surface, an area of at least 65 μm² appears to be TD free.

4. Conclusion

A systematic study on the limit of TCA processes and the efficiency of InGaAs DFLs has been conducted. It is found that the SLS is less efficient compared with a continuous InGaAs layer under typical MBE growth conditions, due to opposing forces from the nonrelaxed GaAs layers in between. Yet, tensile relaxation is beneficial to TDD reduction. Adding step grading layers on both the compressive and the tensile side has further improved the relaxation and lowered the TDD. A TDD from ECCI measurements of 2 × 10⁶ cm⁻² is achieved with a total buffer thickness of 2.55 μm and large areas entirely free of TDs. Estimated TDD via PVTEM is 1.5 × 10⁶ cm⁻². It is highly possible that with a better designed grading scheme, an even thinner and lower TDD buffer structure can be developed, where light coupling from III–V active regions to Si and high reliability at elevated operating temperatures are feasible.

5. Experimental Section

All the samples were grown in a Veeco Gen-II solid-source MBE. The APD-free GaP/Si(001) on-axis template is commercially available via NaSp III/V GmbH. Multiple 1.6 μm GaAs on GaP-on-Si samples were grown under the conditions described previously. TCA was then conducted on the GaAs on GaP-on-Si samples. We varied the number of cycles to evaluate its impact on the TDD. In these experiments, the low-temperature limit was 400 °C and the high-temperature limit was set as high as possible until the surface quality degraded due to an insufficient supply of arsenic. The sample was held at the maximum annealing temperature (Tmax) for 5 min during each cycle. The arsenic beam-equivalent pressure during TCA was set to 1.2 × 10⁻⁵ torr. It was suggested that gallium droplets form on the GaAs surface if the temperature is too high, regardless of arsenic supply. This high-temperature limit was found to be
745 °C in our chamber. To ensure reproducibility, the maximum cycling temperature was dialed down to 735 °C. The TDD was then measured after TCA with ECCI. At least 100 threading dislocations were counted for each sample to ensure statistical significance. A channeling condition consisting of both [040] and [220] was used so that TDDs with all known Burger’s vectors were visible. The TDs appeared to be bright spots due to the local violation of the channeling conditions.

To further investigate the filtering efficiency based on the structure and growth conditions, all filter layers were grown on a post-TCA GaAs surface with a TDD of 3 × 10^7 cm⁻². The nominal growth conditions and structure of the filter were as follows: 200 nm of continuous InGaAs with 10% indium content, grown at 500 °C, at a growth rate of 0.3 nm s⁻¹ and a V/Ill ratio of 20. We observed that when TDD was in the low-10⁶ cm⁻² range, growing another 1 µm of GaAs did not result in a significant reduction of TDD, so the additional thickness of the filter layer showed a negligible effect. As the device was ultimately at the GaAs lattice constant, a 300 nm GaAs capping layer was grown above the filter layer to bring the surface lattice constant back to that of GaAs. Samples without the top GaAs capping layer were also grown to investigate the effect of tensile relaxation on the top GaAs layer. The indium composition varied from 10% to 25%, with a 5% increment. The relative efficiency of a superlattice and a continuous filter layer was studied. With the growth conditions kept at the nominal values, In₀₋₂GaₓAs/ GaAs (10 nm/x nm) × 20 filters with different x values (10, 7, 5, 2, and 0) were grown, with x = 0 being the continuous 200 nm InGaAs filter. Quantitative degree of relaxation was evaluated from RSMs taken with a Rigaku Smartlab system, where large-angular-range and high-resolution RSMs were taken quickly due to the Hypix2000 large-area detector. Scanning transmission electron microscopy (STEM) analysis was conducted in both the XSTEM and PVSTEM directions on the buffer structure with the proposed asymmetric step-graded filter to further confirm the TDD.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

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