High Precision Phase Measurement Technique for Cell Impedance Spectroscopy

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Abstract. This paper presents a new approach for high precision phase measurement. The new system is developed for biomedical applications such as complex cell impedance measurement and dielectric tissue analysis. In many of the named applications it is necessary to measure the complex dielectric constant of a sample as a function of frequency. Therefore the developed system is capable of measuring amplitude and especially high precision phase of the measurement signal over a wide frequency range from 10 Hz to 10 MHz. The experimental result of the new method shows a phase resolution of up to 0.01 degree at 1 MHz and 0.1 degree at 10 MHz. The excellent phase measurement resolution is achieved by a time transformation of the signal using a digital sampling circuitry. The functional principle of the digital sampling circuitry is based on Delta – Modulation and is implemented inside a cheap standard FPGA. The new system is successfully used in blood analysis applications and allows for a practical implementation of cost efficient capacitive hematocrit sensors for the first time.

1. Introduction
This article presents a new measurement system for measuring amplitude and especially high precision phase shifting caused by biological cells and tissue which serve as complex dielectric inside a measurement capacitor. Figure 1 shows a typical measurement setup for such a biological test cell, as it is used in many biological and biomedical applications [1, 2]. The measurement setup must be capable of generating a sinusoidal test signal over a wide range of frequencies. In addition the measurement setup must have a data acquisition unit for sampling the signal which is distorted in amplitude and phasing by the device under test (DUT). The sampled raw data is then filtered inside a signal processing unit and output to the user for further analysis and interpretation.

![Figure 1](image-url)  
**Figure 1.** Typical measurement setup for measuring complex dielectric properties of biological cells and tissue inside a test cell. Two conductive plates encapsulate the sample material (DUT) and serve as a capacitor. The attached measurement setup generates sinusoidal measurement signals and measures amplitude distortion and phase shift caused by the sample material inside the test cell.
2. System Concept
This section describes the developed new system architecture which allows for high precision phase measurement. The corresponding block schematic is shown in figure 2.

**Figure 2.** Block schematic of the new phase measurement system based on Delta-Modulation. The measurement signal is generated by a DDS-Synthesizer. The sampling unit consists of a comparator which acts as a 1 bit A/D-Converter followed by a digital integrator / counter which is triggered by an independent channel of the DDS-Synthesizer. The integrators curve is filtered by a spline interpolation algorithm inside the FPGA and output to the user for further analysis.

2.1. Measurement Signal Generator
The measurement signal generator module is implemented by using an off-the-shelf Direct Digital Synthesizer (DDS) Chip. The Synthesizer provides two independent output channels. Channel 2 generates the actual sinusoidal measurement signal while channel 1 generates an adjustable trigger signal for the integrator circuit inside the FPGA (Xilinx Spartan3 XC3S400). The DDS-Synthesizer is internally driven by a 500 MHz clock signal. The phase accumulator width is N = 32 bit for both channels which leads to a fine frequency resolution of each output channel of 0.12 Hz [3]. The achieved precision frequency resolution is a key point for the sampling process as discussed later.

2.2. Sampling Unit
The developed digital sampling circuitry is the main component of the new measurement system. The sampling circuitry is based on a pure digital Delta-Modulator (DM) structure and replaces a conventional A/D-Converter. It digitizes the sinusoidal measurement signal which has been affected by the DUT inside the test cell. The DM-module mainly consists of a digital 12-bit counter inside the FPGA which serves as an integrator. Depending on the output state of the external comparator the counter counts either up or down on each rising edge of the trigger signal provided by channel 1 of the DDS-Synthesizer. The actual state of the integrator is converted into a corresponding analogue voltage signal and fed back to the inverting input of the comparator. The high impedance positive input of the comparator is directly connected to the voltage divider of the reference impedance Z and the test cell. As a matter of principle the integrator is forced to track the sinusoidal signal on the comparators positive input. An example of the typical pattern of the integrator curve is shown in figure 3. By setting the trigger frequency, the number of samples taken in each period of the measurement signal can be adjusted. Using appropriate values, an oversampling rate of up to $10^6$ can be achieved which leads to a high theoretical signal to noise ratio (SNR) of up to 120 dB for the DM-structure [4].
2.3. Signal Processing Unit
The output data of the Delta – Modulator is the integrator’s curve which represents the measured signal. Since the comparator inside the sampling system acts as a 1-bit A/D-converter the sampled raw data on the output of the integrator contains high frequency components. In figure 3 these high frequency components appear as ripple on the sampled sine wave. Since the high frequency components are not of interest a method known as noise-shaping is applied to the sampled raw data. The integrator works as a high pass filter for high frequency components in the sampled signal. A digital filter implemented inside the FPGA removes these high frequency components and therefore increases the overall SNR [5]. The used low pass filter is based on an on-line Bezier-Spline interpolation algorithm which can be implemented in hardware inside the FPGA. [6].

3. Operation Theory
The phase measurement system is used to measure amplitude and phasing of sinusoidal signals in a frequency range from 10 Hz to 10 MHz. Due to this wide range of six decades, the operation mode of the sampling unit has to be switched between a conventional oversampling mode for digitizing low measurement frequencies and an undersampling mode for high measurement frequencies.

3.1. Oversampling Mode
The oversampling mode is used to digitize signals at low frequencies in the range of 10 Hz to 10 kHz. In this operation mode the output frequency of channel 1 is set to the absolute maximum which can be processed by the FPGA. In this operation mode all measurement samples are taken during a single period of the sinusoidal measurement signal generated by channel 2. Since the trigger signal frequency is always set to a constant maximum value which is limited by the FPGA speed, this sampling method causes a varying number of samples taken during a single sinusoidal measurement signal period dependent on the measurement signal frequency. The graph in figure 4 illustrates this effect for an assumed maximum frequency of 10 MHz which can be handled by the used FPGA logic.

Figure 3. Simulation of the delta modulator illustrates the basic behavior of the integrator curve which tracks the ideal sinusoidal input signal. The simulation is performed for a 7 bit amplitude resolution system for better visualization.

Figure 4. The graph shows the number of samples taken per sine wave as a function of the measurement frequency. The trigger frequency is assumed to be constant at 10 MHz for the oversampling mode. For the undersampling mode the delta frequency is assumed to be constant at 10 Hz between the trigger- and the measurement frequency.
3.2. Undersampling Mode

The undersampling mode is used if the measurement frequency is in the range of 10 kHz to 10 MHz. In this operation mode channel 1 also generates the measurement signal which is directed to the DUT. In contrast to the oversampling mode channel 1 generates a trigger signal frequency just slightly above the measurement frequency. Due to the fine frequency resolution of the DDS-Synthesizer the delta frequency between both channels can easily be adjusted to values in the range of a few Hz or even below 1 Hz. For the undersampling mode the graph in figure 4 assumes the trigger frequency to be exact 10 Hz above the measurement signal frequency. As a matter of principle in the undersampling mode the shape of the measurement signal is captured by sampling many repetitive measurement signals. On each incoming sine wave of the measurement signal exactly one sample is taken at a slightly delayed point. The trigger process is illustrated in figure 5. The undersampling mode allows for digitizing the sinusoidal measurement signal with a virtual high temporal resolution depending on the settings of the trigger frequency and the measurement frequency. Amplitude and phasing are measured with high accuracy by transforming the real measurement frequency to a lower frequency. Figure 6 shows precision measurement results derived by the new measurement technique in comparison to state of the art equipment (Agilent E4980A) which has been used for reference.

4. Conclusion

The developed precision phase measurement technique is based on a time transformation performed in a Delta-Modulator sampling circuit. Especially high frequency measurement signals in the range of 100 kHz to 10 MHz can be measured with an outstanding phase resolution of better than 0.1 degree (for 10 MHz) which is in the range of conventional expensive laboratory equipment such as the Agilent E 4980A LCR-Meter. The employed Delta-Modulator circuitry allows for reconstructing high frequency measurement signals out of many repetitive sine waves which is equal to a time transformation of the measurement signal. The implementation of the system can be done by using cheap digital standard components which allows for a wide-spread use of an impedance spectroscopy measurement system in many cost sensitive biomedical applications for the first time.

References
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