Anomalous, space-charge-limited piezoresistance in defect-engineered silicon

H. Li¹, A. Thayil¹, C.T.K. Lew², M. Filoche³, B.C. Johnson², J.C. McCallum³, S. Arscott⁴, and A.C.H. Rowe⁵

¹Laboratoire de Physique de la Matière Condensée,
Ecole Polytechnique, CNRS, IP Paris, 91128 Palaiseau, France
²Centre for Quantum Computation & Communication Technology,
School of Physics, University of Melbourne, VIC 3010, Australia
³School of Physics, University of Melbourne, Melbourne, Victoria 3010, Australia and
⁴Institut d’Electronique, de Microélectronique et de Nanotechnologie (IEMN),
Université de Lille 1, CNRS, Avenue Poincaré, Cité Scientifique, 59652 Villeneuve d’Ascq, France

The space-charge-limited, steady-state piezoresistance (PZR) in thin device layers of silicon-on-insulator wafers containing a nominal 10¹⁴ cm⁻³ silicon divacancy defects changes sign as a function of applied bias. Above a punch-through voltage (Vt) corresponding to the onset of a Mott-Gurney-like hole current, the longitudinal (110) PZR \( \pi \)-coefficient is \( \pi \approx 70 \times 10^{-11} \text{ Pa}^{-1} \), similar to the value obtained in charge-neutral, p-type silicon. Below \( V_t \) the mechanical stress dependence of the Shockley-Read recombination parameters, specifically the divacancy trap energy \( E_T \), yields \( \pi \approx -25 \times 10^{-11} \text{ Pa}^{-1} \). This analysis suggests that anomalous (or inverse) PZR in nano-silicon occurs when currents are recombination limited due to strong reductions in carrier lifetime induced by significant densities of Shockley-Read centers, and when the reduced dimensionality lowers \( V_t \) and amplifies space-charge-limited currents.

Piezoresistance (PZR) in nano-silicon has received significant attention over more than a decade [1-10] partly because mechanical stress and device scaling into the nanometre range are important elements of the semiconductor roadmap [11], and partly because of multiple claims and observations of either giant or anomalous PZR that are significantly different from the usual effect observed in bulk silicon [12]. As has been noted on many occasions, unusual PZR in nano-silicon is usually correlated with equilibrium carrier depletion, and with the presence of surface-related electronic defects [2-5, 10-13]. Although there is still discussion about the veracity of reports of steady-state giant PZR, it is widely accepted that chemical surface functionalization and thinning of silicon nanowires and nanomembranes can yield anomalous PZR sign changes [3, 5]. Here the applied voltage bias is observed to induce anomalous, steady-state PZR during space-charge-limited bipolar transport in defect-engineered, silicon-on-insulator (SOI). A quantitative description of the effect is given.

In doped, bulk semiconductor devices at low voltages it is usual and reasonable to assume unipolar, electrical transport in the charge-neutral, i.e. in which the density of non-equilibrium injected charge is negligible compared to the equilibrium free charge density [15]. The electrical conductivity is then given by a Drude expression and ohmic conduction is observed e.g. for holes, \( 1/\rho_p = \sigma_p = p \mu_p q \) where \( p \) is the hole density, \( \mu_p \) is the hole mobility and \( q \) is the electronic charge. In Silicon, the PZR is then principally the result of mechanical-stress-induced changes to the electron and hole effective masses and hence mobilities [12], and its sign is determined only by the doping type. For the case of a resistance measurement made parallel to the direction of the applied stress, the PZR is characterized by a scalar, longitudinal \( \pi \)-coefficient which, in the case of holes, is:

\[
\pi_p = \frac{1}{X} \frac{\Delta \rho_p}{\rho_{p0}} \approx -\frac{1}{X} \frac{\Delta \mu_p}{\mu_{p0}},
\]

where \( \mu_{p0} \) is the zero-stress mobility and \( X \) is the applied stress. A similar expression can be given for electrons. In the devices considered here, resistance is measured parallel to an applied stress along the (110) crystal direction for which [10]

\[
\pi_p \approx +71 \times 10^{-11} \text{ Pa}^{-1},
\]

and

\[
\pi_n \approx -30 \times 10^{-11} \text{ Pa}^{-1}.
\]

The steady-state PZR measured here is approximately bounded by these values, but it is not only due to stress-induced mobility changes. Rather, a solution of the stress-dependent version of the self-consistent Poisson-transport equations shows that anomalous PZR occurs during bipolar transport when carrier lifetimes are strongly reduced by the presence of a significant density of Shockley-Read recombination centers, and when the recombination parameters themselves are stress dependent.

Two-terminal, space-charge-limited current (SCLC) devices are fabricated using standard photo-lithographic processing methods from (001)-oriented, fully-depleted SOI with a 2 \( \mu \)m-thick device layer non-intentionally-doped with Boron (\( p \approx 1 \times 10^{14} \text{ cm}^{-3} \)) shown in dark blue in Fig. [1]. Devices of the type used elsewhere [3, 10] are fabricated with \( p^{++} \)-ohmic contacts (Boron, \( 10^{18} \text{ cm}^{-3} \)) shown in light blue in Fig. [1] and then cut into chips (20 mm \( \times \) 13 mm) whose long axis is parallel to the (110) crystal direction as seen in the left panel of Fig. [1a].

*alistair.rowe@polytechnique.edu
These chips are compatible with a 3-point bending apparatus used to apply a time-modulated, tensile mechanical stress of $\approx 20$ MPa for the PZR measurements 3 along the $\langle 110 \rangle$ crystal direction as indicated by the purple arrow in Fig. 1(a). Fig. 1(a) shows progressive zooms of the devices from the chip level in the left panel, to the multi-device level in the top, right panel, to the individual device level in the bottom, right panel. The zooms are indicated by the red rectangles in the figure. The lateral dimensions of the individual SCLC device active area between the ohmic contacts are $100 \, \mu m \times 100 \, \mu m$. Fig. 1(b) shows a perspective schematic drawing of an individual SCLC device using the same color code as the micrograph images. In the perspective drawing the top $8 \, \mu m$ of the $400 \, \mu m$-thick handle shown in white, the buried oxide (BOX) shown in dark gray, the $p = 10^{13} \, \text{cm}^{-3}$ device layer is shown in dark blue, and the $p^{++}$ contacts are shown in light blue. All dimensions are in micrometers. The variable mesh projection will be used for the device modeling and analysis, and will be commented on further below.

Post-processing, a selection of $20 \, \text{mm} \times 13 \, \text{mm}$ chips are exposed to a $10$ MeV beam of $\text{Si}^{5+}$ ions with the aim of forming a desired density of silicon divacancy defects 17. The total resulting dose is $10^{12} \, \text{cm}^{-2}$. As shown in the supplementary information, SRIM modeling 15 indicates that this should result in an approximately homogeneous $2.5 \times 10^{16} \, \text{cm}^{-3}$ divacancy defects in the device layer, but dynamic annealing is expected to result in a true density which is several orders of magnitude lower, consistent with the device modeling discussed below. Photo-induced current transient spectroscopy (PICTS) on the resulting devices reveals a peak corresponding to an electronically active, deep state $0.44$ eV below the conduction band edge (see Supplementary Information), which is identified as the singly ionized acceptor form of the silicon divacancy defect 19. As will be described below, the two principal effects of the divacancy defects are to introduce a fixed negative charge density into the active volume of the device corresponding to the singly ionized acceptor states, and to drastically shorten the electron and hole lifetimes 17.

Figure 2(a) shows typical zero-stress, current-voltage characteristics obtained in a defect-engineered sample with the wafer handle held at ground. The arrows and colors represent the direction of the bias sweep, and a hysteresis is visible between the up (blue markers and arrow) and the down (red markers and arrow) sweeps. The curves were obtained in quasi-steady-state by applying a series of fixed voltage biases and then waiting until the current stabilized at each point. Stabilization times were in general of the order of a few minutes at most, except near the threshold voltage, $V_t$, where the current abruptly increases. In this bias range stabilization times were long, sometimes of the order of one day. Moreover, at biases around $V_t$ the majority carrier changes type as indicated in Fig. 2(b) by the relative current changes induced by a $+1 \, \text{V}$ change in the handle voltage which acts as a gate for the device layer. Below $V_t$ an increase in the current indicates that electrons are the majority carriers in the device layer while, on the contrary, above $V_t$ holes become the majority carrier. This is the typical behavior observed in the punch-through effect in bipolar junction devices 20.

Figure 3(a) shows the PZR $\pi$-coefficient measured simultaneously with the current-voltage characteristic by applying a uni-axial tensile stress of $\approx 20$ MPa parallel to the current flow along the $\langle 110 \rangle$ crystal direction. The
FIG. 2. (a) Experimentally measured up- (blue dots and arrow) and down- (red dots and arrow) sweep current-voltage characteristics obtained on the defect engineered SCLC devices. The slopes indicated in the log-log plot are a guide to the eye. (b) Relative current change induced by a +1 V change in the voltage applied to the wafer handle. The sign indicates a majority electron current below a threshold voltage, $V_t$, and a majority hole current above this bias. A hysteresis in $V_t$ is clearly visible between the up- and down-sweeps.

color code corresponds to the up- and down- sweeps as indicated in Fig. 2(a). The $\pi$-coefficient changes sign around the previously defined threshold voltage, $V_t$, varying from approximately $-24 \times 10^{-11} \text{ Pa}^{-1}$ at low biases to approximately $+65 \times 10^{-11} \text{ Pa}^{-1}$ at high biases. As Fig. 2(b) indicates, this sign change is not observed in the as-prepared devices prior to defect engineering. The threshold voltage at which the switch in sign of the PZR in the defect-engineered devices is observed exhibits the same hysteresis as the current-voltage characteristic in Fig. 2(a), but this hysteresis is absent prior to defect engineering (see Fig. 3(b)). The hysteresis is therefore correlated with the presence of defects induced by the Si$^{5+}$ ion implant, as is the anomalous PZR at low bias.

Since the measured PZR switches from approximately that of charge-neutral, n-type silicon given in Eq. 3 at low biases to approximately that of charge-neutral p-type silicon given in Eq. 2 at high biases (see Fig. 2(a)), and since this switch occurs where the majority carrier type changes from electrons to holes (see Fig. 2(b)), it is tempting to ascribe the anomalous sign change of the PZR to a simple switch from n-type to p-type PZR. Further analysis however shows that this is incorrect.

To better understand the electrical properties of the defect engineered devices, a numerical solution of the self-consistent Poisson/drift-diffusion equations is sought. This was implemented using a finite volume version of the Scharfetter-Gummel approach [21] on a variable rectangular mesh like that shown in Fig. 1(b). The model is performed on a 2-dimensional mesh in order to properly account for the reduced electrostatic dimensionality of the devices which affects $V_t$ as well as the magnitude of the SCLC [22].

As discussed above, defect engineering creates a density of deep, singly ionized acceptor di-vacancies that is accounted for in the model by introducing a density, $N_{V_2^-}$, of fixed negative charge in the device layer, and by drastically reducing the charge carrier lifetimes appearing in the Shockley-Read recombination term [17]. The introduction of a fixed negative charge renders the device layer n-type and results in a p$^{++}$/n/p$^{++}$ device structure. The value of $N_{V_2^-}$ principally affects $V_t$ (higher $N_{V_2^-}$ results in higher $V_t$), whereas the charge carrier lifetimes affect the magnitude of the recombination-limited electron current for applied biases below $V_t$ (shorter lifetimes result in larger currents). A fuller study of the effects of these parameter values is given in the Supplementary Information.

Figure 4 shows the calculated current-voltage characteristics for carrier lifetimes of 0.1 ps and for $N_{V_2^-} = 2.5 \times 10^{14} \text{ cm}^{-3}$ for the up-sweep characteristic (blue curve), and $N_{V_2^+} = 0.5 \times 10^{14} \text{ cm}^{-3}$ for the down-sweep characteristic (red curve). In both cases the upper limits for the carrier mobilities are used, $\mu_n = 1400 \text{ cm}^2/\text{Vs}$ and $\mu_p = 450 \text{ cm}^2/\text{Vs}$. Many of the features of the experimentally measured data in Fig. 2 are reproduced including the magnitude of the currents even at high voltages where geometric modifications to the SCLC are important [22], the punch-through effect in which the current is dominated by electrons below $V_t$ and holes above it, and the variation from ohmic behavior at very low voltages to
FIG. 4. The calculated current-voltage characteristics (solid lines) calculated using a self-consistent solution of the Poisson-transport equations [21]. The colors correspond to the voltage sweep direction as indicated by the arrows, and the symbols illustrate the switch from an electron to a hole current at $V_t$. The model qualitatively reproduces the punch-through behavior observed experimentally in Fig. 2.

a $\sqrt{V}$-dependence below $V_t$. Since the hysteresis is correlated with the presence of charged defects, it is replicated by changing the fixed negative charge corresponding to the $N_{V^-}$ centers. In the real devices this charge density change is likely to occur progressively with applied bias, so the exact shapes of the calculated and measured current-voltage characteristics are not expected to match. Moreover at high voltages the model produces a typical $V^2$ SCLC characteristic [22, 23] whereas the data in Fig. 2(a) shows a linear dependence. The model includes velocity saturation so this does not account for the linear characteristic. It is likely that the linearity is due to a potential barrier at the contacts which limits hole injection [24], and which is not accounted for in the model. Despite these minor differences, the excellent qualitative agreement between the data and the model allow it to be used to analyze the PZR data shown in Fig. 3(a).

Figure 5 shows the calculated PZR with the same color codes for the up- and down-voltage sweeps as used previously. In terms of the origin of the anomalous sign change of the PZR, consideration of the up-sweep curves is instructive. The dashed, blue curve shows the response obtained when only the usual effective mass change [12] is accounted for. In this case no anomalous PZR is observed. The $\pi$-coefficient remains positive, passing from a small value below $V_t$ to the charge-neutral p-type value at high biases where hole injection occurs. This resembles more closely the PZR response obtained prior to defect engineering as shown in Fig. 3(b) where conduction is unipolar and any stress dependence of the Shockley-Read recombination parameters is irrelevant.

After defect engineering, the electron current below $V_t$ is recombination limited and a stress-dependence of the Shockley-Read parameters may then be important. According to deformation potential theory, the most obvious candidate for a stress dependence amongst these parameters is the trap energy, $E_T$. The solid, blue curve in Fig. 5 is obtained when $E_T$ increases by 20 $\mu$V/MPa of tensile stress, a value comparable to the usual deformation potentials of inorganic semiconductors. This stress-induced increase in $E_T$ slightly increases the Shockley-Read recombination rate resulting in higher currents below $V_t$ and therefore a negative PZR. Above $V_t$ a SCLC hole current proportional to $\mu_p$ which no longer depends on recombination is established, and the PZR naturally tends towards the usual value [12]. Note that this observation also reinforces the conclusion that intervalley transfer causing velocity saturation is negligible. A similar tendency is observed in the calculated, down-sweep PZR (red curves in Fig. 5), where the general form of the curve (although not its exact value) match well the measured data in Fig. 3(a), including the hysteresis in $V_t$.

As far as the origins of anomalous, steady-state PZR in nano-silicon go, this work quantitatively illustrates the central role played by space-charge-limited bipolar transport. Under these conditions recombination limited currents can occur, at which point any stress dependence of the recombination parameters can significantly modify the usual PZR and lead to anomalous sign changes. Here this situation is encountered via defect engineering of this, electrostatically 2D layers, but it can also be encountered in chemically thinned or surface functionalized thin films and nanowires where surface defects can determine the majority carrier in the nano-structure.
The stress dependence of the recombination parameters, in particular the deformation potentials of the trap energies, is estimated to be of the same order of magnitude as those of the bands in inorganic crystals, and as such this can result in anomalous, but not giant, PZR.

[1] R. He and P. Yang, “Giant piezoresistance effect in silicon nanowires,” Nature Nanotechnology 1, 42 (2006).
[2] A. C. H. Rowe, “Silicon nanowires feel the pinch,” Nature Nanotechnology 3, 311 (2008).
[3] K. Reck, J. Richter, O. Hansen, and E.V. Thomsen, “Piezoresistive effect in top-down fabricated silicon nanowires,” in IEEE 21st International Conference on Micro Electro Mechanical Systems (2008) pp. 717–720.
[4] T. Barwicz, L. Klein, S.J. Koester, and H. Hamann, “Silicon nanowire piezoresistance: Impact of surface crystallographic orientation,” Applied Physics Letters 97, 023110 (2010).
[5] J. S. Milne, A. C. H. Rowe, S. Arscott, and Ch. Rennr, “Giant piezoresistance effects in silicon nanowires and microwires,” Physical Review Letters 105, 226802 (2010).
[6] A. Lugstein, M. Steinmair, A. Steiger, H. Kosina, and E. Bertagnolli, “Anomalous piezoresistance effect in ultrastrained silicon nanowires,” Nano Letters 10, 3204 (2010).
[7] T.-K. Kang, “Evidence for giant piezoresistance effect in n-type silicon nanowire field-effect transistors,” Applied Physics Letters 100, 163501 (2012).
[8] H. Jang, J. Kim, M.-S. Kim, J.H. Cho, H. Choi, and J.-H. Ahn, “Observation of the inverse giant piezoresistance effect in silicon nanomembranes probed by ultrafast terahertz spectroscopy,” Nano Letters 14, 6942 (2014).
[9] K. Winkler, E. Bertagnolli, and A. Lugstein, “Origin of anomalous piezoresistive effects in VLS grown Si nanowires,” Nano Letters 15, 1780 (2015).
[10] H. Li, C. T. K. Lew, B. Johnson, J. C. McCaulum, S. Arscott, and A. C. H. Rowe, “Giant, anomalous piezoimpedance in silicon-on-insulator,” Physical Review Applied 11, 044010 (2019).
[11] Y. Sun, SE Thompson, and T. Nishida, “Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors,” J. Appl. Phys. 101, 104503 (2007).
[12] C. S. Smith, “Piezoresistance effect in germanium and silicon,” Physical Review 94, 42 (1954).
[13] Jiaming Li, Le Luo, Jeff Carvell, Ruihua Cheng, Tianshu Lai, and Zixin Wang, “Shot-noise-limited optical faraday polarimetry with enhanced laser noise cancelling,” Journal of Applied Physics 115, 103101 (2014).
[14] H. Li, L. Martinelli, F. Cadiz, A. Bendounan, S. Arscott, F. Sirotti, and A. C. H. Rowe, “Mechanical stress dependence of the Fermi level pinning on an oxidized silicon surface,” Applied Surface Science 478, 284 (2019).
[15] S.M. Sze and K.K. Ng, Physics of semiconductor devices (Wiley-Blackwell, 2007).
[16] Y. Kanda, IEEE Trans. Elec. Dev. 29, 64 (1982).
[17] N.M. Wright, D.J. Thomson, K.L. Litvinenko, W.R. Headley, A.J. Smith, A.P. Knights, J.H.B. Deane, F.Y. Gardes, G.Z. Mashanovich, R. Gwilliam, and G.T. Reed, “Free carrier lifetime modification for silicon waveguide based devices,” Optics Express 16, 19779–19784 (2008).
[18] J.F. Ziegler, M.D. Ziegler, and J.P. Biersack, “Srim—the stopping and range of ions in matter,” Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms 268, 1818–1823 (2010).
[19] B.G. Svensson, B. Mohadjeri, A. Hallén, J.H. Svensson, and J.W. Corbett, “Divacancy acceptor levels in ion-irradiated silicon,” Physical Review B 43, 2292 (1991).
[20] J. Lohstroh, J.J.M. Koomen, A.T. Van Zanten, and R.H.W. Salters, “Free carrier lifetime modification for silicon waveguide based devices,” Optics Express 16, 805–814 (2008).
[21] D. L. Scharfetter and H. K. Gummel, “Large-signal analysis of a silicon read diode oscillator,” IEEE Transactions on electron devices 16, 64–77 (1969).
[22] S. Alagha, A. Shik, H. E. Ruda, I. Saveliev, K. L. Kavanagh, and S. P. Watkins, “Space-charge-limited current in nanowires,” Journal of Applied Physics 121, 174301 (2017).
[23] S. Mott and R. W. Gurney, Electronic processes in ionic crystals (Clarendon Press, 1940).
[24] J. A. Rör, D. Moia, S. A. Haque, T. Kirchartz, and J. Nelson, “Exploring the validity and limitations of the mott–gurney law for charge-carrier mobility determination of semiconducting thin-films,” Journal of Physics: Condensed Matter 30, 105901 (2018).