An improved hysteresis current control scheme during grid voltage zero-crossing for grid-connected three-level inverters

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Abstract
For three-level inverters, hysteresis current control (HCC) has been widely used in applications such as active power filters due to its fast-dynamic response, and it does not need to control each frequency separately with multiple controllers, which makes it simpler. However, the large fluctuation range of switching frequency is a serious disadvantage of hysteresis current control. Especially, the switching frequency decreases significantly during grid voltage zero-crossing. This frequency fluctuation will cause low-frequency harmonics. The purpose of this paper is to propose a sampling compensation scheme, which can solve the problem of switching frequency fluctuation near the zero-crossing of grid voltage. Based on the variable hysteresis band strategy, the virtual sampling and switching time prediction algorithm is designed, which does not need to increase the sampling frequency or add additional controller. Therefore, nearly fixed switching frequency can be achieved while maintaining the control performance. Both simulation and experimental tests have verified the efficacy of the proposed scheme.

1 | INTRODUCTION
In the past decade, the power system is moving from centralized operation to more distributed operation. With this change, grid-connected inverters have been widely employed in both power supply side and end-user side [1, 2]. Consequently, how to further improve the performance of grid-connected inverters has attracted more attention. As an example, multilevel topologies have been introduced to low-voltage applications [3, 4], because they provide benefits such as high-efficiency and high-power-output with reduced harmonics. Neutral-point-clamped (NPC) and T-type converters are typical three-level topologies, which are commonly used in harmonic current elimination and reactive power compensation applications.

There are mainly two types of controllers used for three-level converters, linear controllers and non-linear controllers. For linear controllers, the grid-voltage oriented vector control using PI controllers with outer dc-link voltage control loop and inner current loop control implemented on the $d$-$q$ (rotational) coordinate is widely used [5–7]. The $d$-axis current and $q$-axis current can be used to regulate the active power and reactive power, respectively. And the $d$-axis current reference is obtained from the outer dc-link voltage control loop. In order to extend the control bandwidth of the linear controllers and achieve fast dynamic response, non-linear controllers have also been used such as hysteresis control [8], predictive current control [7], sliding mode control [9, 10]. These non-linear controls are very useful in applications such as active power filters (APF), STATCOMs, where high control bandwidth (e.g., to attenuate high-frequency harmonics) and fast dynamics are required. In this paper, the target application is APF, so the hysteresis control is investigated. For the three-level NPC inverters, the predictive current control is also a commonly used non-linear control method due to its fast dynamic response. In [11], a simplified predictive control strategy for current control of the three-level T-type NPC inverter is presented. Moreover, aiming at improving the quality of output current, the multi-step predictive control is proposed for the NPC grid-connected inverter [12]. Nevertheless, the hysteresis current control still has advantages in lower computational burden and simple control structure. In [13, 14], the hysteresis current controller (HCC) for three-level inverters is proposed, which provides a fast-dynamic response (fast bang-bang control) and acceptable steady-state performance. In addition, the HCC can be seen a special case of...
the conventional sliding mode controller, and it has been widely used for active power filters [13]. For systems with several harmonics to attenuate, the hysteresis control does not need to control each frequency separately [13–16].

The unfixed switching frequency is an inherent problem for HCC, which leads to undesired current harmonics in a wide frequency range, thus generating large output current ripple in certain regions. In an actual three-level inverter system, a variable hysteresis band is a widely accepted solution to stabilize switching frequency [17–20]. It compensates the variation of the grid voltage. In order to obtain smoother and more constant switching frequency, [21] presented an adaptive hysteresis current controller, which instantaneously calculates the hysteresis bandwidth in the half bridge converter-based railway power compensators. Additionally, based on the variable hysteresis band (i.e., adaptive hysteresis current controller), [22] guarantees almost fixed switching frequency operation of single-phase transformer-less inverters. However, significant switching frequency fluctuation still remains around grid voltage zero-crossing of three-level NPC inverters as presented in [23]. Therefore, the variable hysteresis band method cannot maintain the switching frequency constant at all times.

The significant switching frequency fluctuation around grid voltage \(v_g\) zero-crossing is shown in Figure 1 (\(f_s\) is the reference current, and \(f_s\) is the switching frequency). For the hysteretic current control of grid-connected three-level inverters, the current tracking speed in one control period depends on the instantaneous value of \(v_g\). As shown in Figure 1(a,b), around the \(v_g\) zero-crossing, when the inverter output voltage is around zero (very limited controllability), the current response is very slow, which seriously weakens the current tracking performance. It results in that output current cannot track the sinusoidal reference very well and have distortions, which is called “tracking weakness” in this paper. As seen in Figure 1(c), this phenomenon makes the switching frequency fluctuate significantly (the switching frequency reference value is 20 kHz). This switching frequency fluctuation can introduce low order harmonics in the current. [24] and [25] point out that the sampling frequency causes the tracking weakness in \(v_g\) zero-crossing region. In [23, 26, 27], a mixed-level scheme is proposed for the grid-connected three-level inverters to stable switching frequency around \(v_g\) zero-crossing regions. It utilizes a two-level modulation instead of the default three-level modulation in the \(v_g\) zero-crossing regions. Compared with the conventional methods (fixed hysteresis band and variable hysteresis band), the mixed-level HCC can stabilize the switching frequency around the grid voltage zero-crossing region to some extent. However, the increased \(i_o\) ripple is obvious around the \(v_g\) zero-crossing region with the two-level modulation used in the mixed-level HCC. In addition, it is difficult to avoid switching frequency jitter during the transition between the two-level and the three-level modulation of the mixed-level HCC.

In this paper, a sampling compensation hysteretic current control is proposed to overcome the tracking weakness at \(v_g\) zero-crossing for hysteresis control in grid-connected three-level inverters. By combining a virtual sampling and switching time prediction strategy, the proposed scheme not only can mitigate the tracking weakness with a lower sampling frequency but can also avoid excessive current ripple. In this proposed scheme, two-level modulation is also avoided. It should be noted that the proposed scheme does not require voltage zero-crossing detection. The motivation of this work comes from real challenges in industrial applications of active power filters (APFs) in attenuating the harmonics around grid zero-crossing region and passing power quality certification for products. The proposed control scheme has been used in real APF products.

The contribution of this paper is summarized as follows: This paper proposes a sampling compensation HCC strategy to stable \(f_s\) for NPC three-level inverters, where the disadvantages of existing mixed-level HCC such as excessive current ripple can be avoid.

The rest of the paper is organized as follows. The principle of the hysteresis control for three-level inverters is depicted, and the reason for tracking weakness during \(v_g\) zero-crossing is analysed in Section 2. In Section 3, the solution for the tracking weakness is proposed. The simulation and experiment results are presented in Section 4 to verify the proposed control scheme. Finally, the conclusion of this paper is given in Section 5.
2 | ANALYSIS OF THE TRACKING WEAKNESS FOR GRID-CONNECTED THREE-LEVEL INVERTERS

2.1 | Hysteresis current control of three-level inverters

Taking the T-type NPC inverter as an example, the hysteresis control system of three-level inverters is shown in Figure 2. The four series-connected switches work with logics that $S_{x1}$ is complementary to $S_{x2}$ and $S_{x3}$ is complementary to $S_{x4}$ ($x = a, b, c$). The corresponding switching states and related pole voltage are listed in Table 1. For any phase among $a$, $b$, and $c$, there are three stable switching states namely “H,” “O,” and “L,” and the pole voltages are $v_{dc}/2$, 0, $-v_{dc}/2$, respectively with reference to the dc-link midpoint. Regarding the voltage levels, 9 voltage levels can be obtained for each phase output voltage: $2v_{dc}/3$, $v_{dc}/2$, $v_{dc}/3$, $v_{dc}/6$, 0, $-v_{dc}/6$, $-v_{dc}/3$, $-v_{dc}/2$ and $-2v_{dc}/3$. The grid is considered as a stiff grid ($v_a, v_b, v_c$), where the grid impedance is neglected. Please note no matter whether the grid impedance is considered, the tracking weakness issue exists and needs to be solved.

The LCL filter uses resistor based passive damping, which is in series with the capacitors as shown in Figure 2, to attenuate the resonance. The design procedure for an LCL filter has been detailed in literatures such as in [28] and [29]. Its cut-off frequency is able to filter the main switching frequency related harmonics.

The PLL provides the phase angle of the voltage at the point of common coupling (PCC). In this paper, a closed-loop PLL is used to improve the angle-tracking accuracy and robustness. When the grid voltage is unbalanced or the THD is high, the open-loop PLL will cause large fluctuation of phase angle $\theta$ and worsen the control performance. Therefore, the experimental platform uses closed-loop PLL to improve the robustness. The PLL diagram is presented in the Appendices. The PLL is synchronized to the grid fundamental frequency. The sampling frequency of the PCC $v_{dc}$ is fixed 20 kHz.

The dc-link voltage is managed by an additional dc-link voltage controller as shown in Figure 2. The dc-link voltage controller is realized with a PI controller and is used to keep the overall dc-link voltage at the reference value. In consequence of the divided dc link, the upper and the lower dc-link voltages have to be balanced, which is done also by a PI controller. The control diagram is presented in the Appendices part. The active power is mainly used to cover the losses of the inverter.

The $i_q^*$ can be given according to the demand of the reactive power compensation or harmonic compensation. In this paper, to highlight the improvement of hysteresis control, the reference generation of $i_q^*$ is not concerned.

The feedback current is inverter output current $i_x$ ($x = a, b, c$) before filter. For linear controllers such PI controllers, the most convenient and straightforward option is to control of the grid current directly in the LCL filter because it offers an actual closed-loop control of the grid current. However,
hysteresis control does not allow direct control of the grid current; in hysteresis control, the instantaneous value of the inverter output current is compared with the hysteresis threshold to select the switching states. Since the filters remove the ripples, the grid current (after the filters) cannot reflect the real value of the inverter output current so it cannot be used in hysteresis control. Therefore, the inverter output current before the filter is taken as the control target.

2.2 Variable hysteresis band

Figure 3 depicts the principle of the hysteresis controller for the grid-connected three-level inverter. As the Figure 3 shows, switching states are commanded once the \( i_o \) touches or overshoots the upper or lower hysteresis boundaries (\( B_{up}, B_{low} \)), and the pole voltage depends on the \( v_g \) polarity. The performance like segment BC is called free-wheeling. For any phase, the switching states are obtained from the comparing logic in Equation (1), where \( u_o(t) \) is the inverter output pole voltage.

\[
\begin{align*}
\text{if } v_g(t) > 0 & : \\
& \begin{cases} 
 u_o(t) = v_d/2 \text{ when } i_o(t) \leq B_{low} \\
 u_o(t) = 0 \text{ when } i_o(t) > B_{up} 
\end{cases} \\
\text{if } v_g(t) \leq 0 & : \\
& \begin{cases} 
 u_o(t) = -v_d/2 \text{ when } i_o(t) \geq B_{up} \\
 u_o(t) = 0 \text{ when } i_o(t) < B_{low} 
\end{cases}
\end{align*}
\]

(1)

The current path that flows from dc-side to ac-side is defined as a positive path (\( i_o > 0 \)), and reversely the negative path (\( i_o < 0 \)). Figure 3 is the diagram of Figure 1, which illustrates the tracking weakness phenomenon during the \( v_g \) zero-crossing. The reason for this is analysed in Section 2.3.

In hysteresis current control, the width of the hysteresis band (\( B_p \)) plays a critical role and determine most of the control performance, such as current ripple and switching frequency. In this paper, the variable hysteresis band scheme is the basis of the later scheme because it can generally resolve the unfixed switching frequency to a certain extent. For the hysteresis boundary, it is defined as:

\[
\begin{align*}
 B_{up} & = i_{ref}(t) + B_p/2 \\
 B_{low} & = i_{ref}(t) - B_p/2 \tag{2}
\end{align*}
\]

where \( i_{ref} \) is the current reference.

In practice, the grid-side inductance \( L_2 \) is relatively small compared to \( L_1 \), and almost all of the inductor ripple current is absorbed by the capacitor. Thus, the capacitor voltage is similar to the \( v_g \). In order to simplify the modelling and analysis, the filter can be treated as an L-type. This simplified filter modelling is also used in other references such as [23] and [30]. Then, the voltage equation of the grid-connected inverter is:

\[
v_L(t) = u_o(t) - v_g(t) = L \frac{di_o(t)}{dt} \tag{3}
\]

where \( v_L \) is the voltage drop across the filter inductor. Moreover, it is assumed that \( i_{ref} \) and \( B_p \) are fixed values in a switching period, based on the fact that the switching frequency is usually more than ten times of the frequency of \( i_{ref} \). In a switching period \( T_r \), the reference current and the hysteresis boundary can be regarded as constants, so it can be approximated to a right-angled triangle as shown in Figure 4. In this condition, the relation between the current-changing slope and the \( v_g \) polarity changing. Because the midpoint of the dc-link capacitor of the equipment is connected to the neutral of the power grid, the current response can be deduced by:

\[
\frac{B_p}{T_r} = \frac{di_o(t)}{dt} = \begin{cases} 
 \frac{v_d/2 - v_g(t)}{L} & (v_g > 0) \\
 0 - \frac{v_g(t)}{L} & (v_g < 0) 
\end{cases} \tag{4}
\]
where voltages and currents are instantaneous values obtained by sampling; $T_r$ and $T_f$ are for current rising and falling time, respectively; while $di_r/dt$ and $di_f/dt$ imply the rising and the falling slopes of current response, respectively. The calculation of current-changing slope depends on $r_g$ polarity.

Then, $T = T_r + T_f$ is defined as a switching period, and it can be uniformly expressed as:

$$T = \frac{v_d B_w L}{|r_g(t)| (v_g - 2|r_g(t)|)} = \frac{1}{f_s}$$

where $|r_g(t)|$ means the absolute value of $r_g$. It can be seen that switching frequency $f_s$ will vary periodically with $r_g$ while $B_w$ is constant and dc-voltage $v_d$ and inductor $L$ are assumed to be fixed. Therefore, if the expected switching frequency $f_s^*$ is given, the width of the hysteresis band $B_w$ should be changed in real-time as:

$$B_w(t) = \frac{|r_g(t)| (v_g - 2|r_g(t)|)}{f_s v_d L}$$

According to Equations (4) and (5), current response velocity $di/dt$ always changes with $r_g$. Thus, the $T_r$ and $T_f$ are not fixed, and the $T$ is variable. By changing $B_w$ along $r_g$ as the Equation (7), the $T$ can maintain constant.

### 2.3 Analysis of the reason for the tracking weakness

However, the variable hysteresis band is hardly work well in the $r_g$ zero-crossing regions. As illustrated in Figure 3, $i_o$ is easy to overshoot hysteresis boundaries and difficult to return to the band. The significant deviation from $i_{o.ref}$ is presented as a “tracking weakness” feature, which is caused by two critical reasons.

1. The weak 0-state. From Equations (4) and (5), the current response velocity $di/dt$ obtains extremum at zero-crossing points. As shown in Figure 3, in the region near zero points of negative voltage polarity ($r_g < 0$), $di_r/dt$ is much larger than $di_f/dt$. Conversely, in the region near zero points of positive voltage polarity ($r_g > 0$), $di_f/dt$ is much larger than $di_r/dt$. For example, after point B in Figure 3, the rising velocity of $i_o$ under free-wheeling condition is so slow that $i_o$ will not follow $i_{o.ref}$ anymore. Therefore, the $i_o$ cannot follow the reference well, and the switching frequency is reduced unreasonably.

2. The restriction of the sampling. According to Equation (7), $B_w$ comes to almost zero at $r_g$ zero-crossing. In this condition, as the segment AB in Figure 3, the drop velocity of $i_o$ is so fast that it need a very high sampling frequency. However, the actual sampling frequency in practice is limited. As a result, $i_o$ easily overshoots beyond the hysteresis boundary during the sampling interval, and it cannot be noticed until the next sampling arrives. This phenomenon is more serious during the grid-voltage zero-crossing. Even if the sampling frequency is increased, the delay in the sampling and calculation process is inevitable.

In order to mitigate the above issue (current tracking weakness and large variation of switching frequency) without high sampling demand, the sampling compensation scheme is proposed in this paper.
FIGURE 7 Different sampling method. (a) Constant frequency sampling; (b) switching time prediction; (c) combining the switching time prediction with virtual sampling around $v_g$ zero-crossing points

3 PROPOSED SAMPLING COMPENSATION SCHEME

It can be seen from the above analysis, the tracking weakness is also affected by sampling method. As shown in Figure 7(a), the traditional fixed sampling period is the key reason of the hysteresis boundary overshoot. In this condition, $i_o$ is always required to detect as soon as possible by oversampling. Thus, it requires a higher sampling frequency and more sampling points, although most of the sampling results do not lead to the switching state changed. However, the higher sampling frequency means higher hardware cost, and the issue cannot be solved fundamentally ([17] and [19]).

3.1 Switching time prediction scheme

In order to reduce unnecessary sampling points, the switching time prediction scheme is proposed. It means that each sampling takes place at the state switching point, which is the very moment of $i_o$ boundary-touching as is illustrated in Figure 7(b).

According to the model of current response, the time interval between two switching states $\Delta t$ can be calculated by Equations (4) and (5) when the $B_w$ and switching state are determined:

$$\Delta t(k) = \frac{D(k)L}{|u_o(k) - v_g(k)|}$$  \hspace{1cm} (8)

where $u_o$ is the inverter output pole voltage corresponding to different switching states. In order to make the prediction more accurate, the distance between feedback $i_o$ and hysteresis band boundary is used to replace $B_w$, and it is defined as $D$.

Taking the current control process in Figure 7(b) as an example. Once the real-time data of $S(k)$ is sampled, the $B_w(k)$ can be calculated by Equation (7), and current response rising in the next switching state is needed. Therefore, $\Delta t(k)$ can be predicted with:

$$D(k) = B_{wp}(k) - i_o(k)$$ \hspace{1cm} (9)

$$u_o(k) = v_{dc}(k)/2$$ \hspace{1cm} (10)

The new switching state will last $\Delta t(k)$-time until the next new sampling and judgment. In the same way, the selection of sampling interval prediction parameters can be developed in different switching state, as the Equation (1).

3.2 Prediction correction

Due to the errors of sampling and calculation and the requirements of different operation states, the prediction results of the sampling interval need to be corrected.

Usually, in a stable state, the sampling point is the changing point of switching state. Consequently, the switching period can be calculated by

$$T = \Delta t(k) + \Delta t(k + 1)$$ \hspace{1cm} (11)

Switching frequency is usually set an allowable control range, and the corresponding switching period has maximum value $T_{\text{max}}$ and minimum value $T_{\text{min}}$. In this paper, the allowable switching frequency fluctuation range is 18–24 kHz. Thus, there are $T_{\text{max}} = 1/18k$ and $T_{\text{min}} = 1/24k$. The final sampling interval (i.e., switching interval) is corrected and limited in this range.

$$T_{\text{min}} < T < T_{\text{max}}$$ \hspace{1cm} (12)

Thus, for the new prediction results, it needs to satisfy:

$$T_{\text{min}} - \Delta t(k) < \Delta t(k + 1) < T_{\text{max}} - \Delta t(k)$$ \hspace{1cm} (13)

Ideally, the prediction in Equation (8) is always correct as long as the last sampling is accurate, just like $i_o(k) = B_{wp}(k)$. However, prediction errors would be inevitably accumulated step by step.
due to practical issues, such as sampling delay, switching signal delay, calculation delay, and some other data processing errors. Because of the switching time prediction errors, sampling may be triggered before the moment of $i_o$ boundary-touching, such as $S(k+3)$ shown in Figure 7(b), which then leads to inaccuracy of boundary-comparing and the failure of follow-on predictions.

This problem could be resolved by employing the improved comparing method. In order to make $i_o$ track the reference current $i_{ref}$ more accurately, the current reference mode closest to $i_{ref}$ should be selected as:

“fall” current response is needed, if $i_o > i_{ref}$;
“rise” current response is needed, if $i_o < i_{ref}$.

Based on the prediction accuracy and the constraint of Equation (13), $\Delta t(k + 2)$ has met the requirement of switching frequency stability. Hence, the switching state should be changed generally at the point after $\Delta t(k + 3)$-time, unless the error is very large. In this way, unnecessary frequent correction and consequent calculation delays are avoided.

For dynamic responses like the step change of $v_g$, switching state remains unchanged for an extended period of time. In order to avoid no-sampling action during long-time prediction when $i_{ref}$ has step-changes, more samplings should be added to have more feedback. When the new switching state is the same as the previous one, use Equation (14) to replace Equation (13).

$$\Delta t_{min} < \Delta t < T_{min} - \Delta t_{min}$$

(14)

where $\Delta t_{min}$ is the minimum sampling interval, which includes minimum effective pulse, sampling delay, and calculation delay.

As a result, $i_o$, $v_g$, and $B_y$ can be corrected at each additional sampling, which promises more accurate predictions during large reference current changes. Note that when $i_o$ reaches the desired region and the new switching state changes, the next $\Delta t$ can still satisfy Equation (13).

3.3 Virtual sampling

Using above method, the expected control performance can be achieved in most of the regions. However, in regions with sizeable current response slope, such as around points of $v_g$ zero-crossing, very small $\Delta t$ will be obtained. In this condition, a very high instantaneous sampling frequency is needed, and calculation delay becomes a non-ignorable proportion in $\Delta t$. To resolve the problem, virtual sampling is developed based on predictive sampling, as illustrated in Figure 7(c). At the virtual sampling point, there is a calculation result of instantaneous current value instead of the real ADC sampling data.

After normal sampling and calculation at $S(k)$, if $\Delta t(k)$ is less than the set value, which is determined by the maximum acceptable sampling frequency and hardware performance, the virtual sampling data is used at $V(k + 1)$ point to generate a new switching state with the least calculation. The hysteresis bound-

\[ i_{ref}(k + 1) = i_{ref}(k) + \frac{|v_g - v_{ref}|}{L} \Delta t \]

(15)

Since there is no prediction calculation, $\Delta t(k + 1)$ is obtained in the following way

$$\Delta t(k + 1) = T^* - \Delta t(k)$$

(16)

where $T^*$ is the ideal switching period.

At the next real sampling point $S(k + 2)$, the current prediction control is enabled according to the real current sampling value. In this way, the switching state will not be restricted by the sampling frequency, so that $i_o$ ripple is controlled in the hysteresis band during $v_g$ zero-crossing.

For the sampling compensation scheme, the diagram of current control performance in $v_g$ zero-crossing regions is shown by the real line in Figure 8. The implementation process of the proposed control scheme is summarized in a flowchart shown in Figure 9. The maximum acceptable sampling frequency is set as 200 kHz (the threshold value of virtual sampling is 5 $\mu$s), and the reference switching frequency is 20 kHz. The proposed control process can be divided into two paths.

(1) Assuming $\Delta t(0) > 5 \mu$s, the normal sampling and prediction calculations are executed (path I in Figure 9) at point A. The prediction result is $\Delta t(1)$;

(2) Assuming $\Delta t(1) < 5 \mu$s, the virtual sampling is triggered at point B. The controller select the switching state with the fastest speed and obtain $\Delta t(2)$. The path II in Figure 9 is executed.

In this way, for each switching period, Equations (11) and (12) are met to ensure that the switching frequency is controlled within a given range. Moreover, due to the function of Equation (16), the virtual sampling will not appear continuously to ensure that $i_o$ is detected in each switching period.

4 SIMULATION AND EXPERIMENT RESULTS

In order to validate the proposed hysteresis control scheme, an experimental prototype is established in both simulation
Δ in Figure 10. The switching frequency is defined as the forms obtained in simulation with unity power factor is shown corresponding to zero power factor operation in Figure 1. The waveshape is the same as that shown in Figure 1. The parameters are given in Table 2. The resonant (cut-off) frequency is 5.627 kHz, which is able to filter the switching frequency related harmonics around 20 kHz. It can be seen that the hysteresis boundary exceeding problem caused by sampling frequency restriction can be overcome by the proposed sampling compensation scheme. The fixed sampling period is 5 μs (200 kHz), and the minimum of the real-sampling of sampling compensation is also 5 μs. For the [23] scheme, it is based on switching time prediction and use two-level modulation around \( v_g \) zero-crossing. Due to the increase of the bandwidth at the peak of \( i_o \), the current ripple and THD increases clearly, which is not suitable for small filter inductor or easily saturated inductor. Figure 11(b) shows the FFT analysis of the fixed sampling period, [23] scheme, and sampling compensation scheme. The resonant frequency \( f_r \) is 5.627 kHz. It can be seen that the switching frequency can potentially enter the resonant frequency range when the variation of the switching frequency is wide, especially with the fixed sampling period method. In this case, the damping resistor must be used to damp the resonance. In contrast, with the proposed sampling compensation scheme in this paper, the switching frequency is relatively constant around 20 kHz so it will unlikely enter the resonant frequency range and trigger resonance. Therefore, the LCL filter design is easier and can effectively filter the switching frequency harmonics. In addition, the proposed control method has fewer low-frequency harmonics, as shown in Figure 11(c).

4.1 Simulation results

The simulation is carried out with MATLAB/Simulink. Corresponding to zero power factor operation in Figure 1. The waveforms obtained in simulation with unity power factor is shown in Figure 10. The switching frequency is defined as \( f_s = 1/T \), where \( T \) is the time interval between two rising edges of the adjacent switching pulses. Similar to zero power factor case, there is a current tracking weakness issue during \( v_g \) zero-crossing, and the switching frequency fluctuates significantly (the switching frequency reference value is 20 kHz). The dc-link voltage is regulated through a dc-link voltage control loop. In practical applications, for zero power factor operation (reactive power), the current reaches maximum at voltage zero-crossing. And the line inductor may saturate and consequently reduces its value, which intensifies the issues discussed in this paper. Therefore, reactive current is taken as an example in following simulation and experiment.

Figure 11(a) illustrates the comparison of inverter-side current between the reactive current of the traditional fixed sampling period, [23] scheme, and sampling compensation scheme when switching frequency is set as 20 kHz. It can be seen that the hysteresis boundary exceeding problem caused by sampling frequency restriction can be overcome by the proposed sampling compensation scheme. The fixed sampling period is 5 μs (200 kHz), and the minimum of the real-sampling of sampling compensation is also 5 μs. For the [23] scheme, it is based on switching time prediction and use two-level modulation around \( v_g \) zero-crossing. Due to the increase of the bandwidth at the peak of \( i_o \), the current ripple and THD increases clearly, which is not suitable for small filter inductor or easily saturated inductor. Figure 11(b) shows the FFT analysis of the fixed sampling period, [23] scheme, and sampling compensation. The resonant frequency \( f_r \) is 5.627 kHz. It can be seen that the switching frequency can potentially enter the resonant frequency range when the variation of the switching frequency is wide, especially with the fixed sampling period method. In this case, the damping resistor must be used to damp the resonance. In contrast, with the proposed sampling compensation scheme in this paper, the switching frequency is relatively constant around 20 kHz so it will unlikely enter the resonant frequency range and trigger resonance. Therefore, the LCL filter design is easier and can effectively filter the switching frequency harmonics. In addition, the proposed control method has fewer low-frequency harmonics, as shown in Figure 11(c).

The simulation waveforms around \( v_g \) zero-crossing point with different fixed sampling period are depicted in Figure 12. As can be seen, the switching frequency of the fixed sampling period control varies clearly, and it is not stabilized at the setting value (20 kHz), even though the variable \( R_s \) has been accurately calculated by Equation (7). In Figure 12(b), the sampling frequency is increased to 1 MHz. As seen, the \( i_o \) is controlled in hysteresis band, but the improvement of switching frequency is limited.

and laboratory environment. The structure of the prototype is the same as that shown in Figure 1. The parameters are \( v_{dc} = 700 \) V and \( v_g \) (RMS) = 220 V. The damping resistor is used, which is in series with the capacitor branch of the filter to damp the resonance. The parameters of LCL filter are given in Table 2. The resonant (cut-off) frequency \( f_r \) of the LCL filter is chosen to be 5.627 kHz, which is able to filter the switching frequency related harmonics around 20 kHz and above.

Regarding stability, in general, the stability of hysteresis control is very strong [31, 32], which is one of its advantages. It should be noted that the proposed voltage zero-crossing control scheme is independent of the filter type, because the filter can be treated as L-type in modelling and analysis. For poles introduced by the capacitor presence, damping can move the unstable poles more inside the stability region, and the dynamic response remains unchanged with the introduction of damping. [33].

![FIGURE 9] Digital implementation process of the proposed control scheme (Point A and point B refer to those points in Figure 8)

![FIGURE 10] Output current and corresponding switching frequency with unity power factor: (a) output current; (b) switching frequency

|TABLE 2| The filter parameters |
|---|---|---|
|\( L_s \) | 0.4 mH | \( R_s \) | 1 Ω |
|\( L_d \) | 0.1 mH | \( f_r \) | 5.627 kHz |
|\( C_f \) | 10 μF | \( f_r^* \) | 20 kHz |

![FIGURE 10] Output current and corresponding switching frequency with unity power factor: (a) output current; (b) switching frequency

4.1 Simulation results

The simulation is carried out with MATLAB/Simulink. Corresponding to zero power factor operation in Figure 1. The waveforms obtained in simulation with unity power factor is shown in Figure 10. The switching frequency is defined as \( f_s = 1/T \), where \( T \) is the time interval between two rising edges of the adjacent switching pulses. Similar to zero power factor case, there is a current tracking weakness issue during \( v_g \) zero-crossing, and the switching frequency fluctuates significantly (the switching frequency reference value is 20 kHz). The dc-link voltage is regulated through a dc-link voltage control loop. In practical applications, for zero power factor operation (reactive power), the current reaches maximum at voltage zero-crossing. And the line inductor may saturate and consequently reduces its value, which intensifies the issues discussed in this paper. Therefore, reactive current is taken as an example in following simulation and experiment.

Figure 11(a) illustrates the comparison of inverter-side current between the reactive current of the traditional fixed sampling period, [23] scheme, and sampling compensation scheme when switching frequency is set as 20 kHz. It can be seen that the hysteresis boundary exceeding problem caused by sampling frequency restriction can be overcome by the proposed sampling compensation scheme. The fixed sampling period is 5 μs (200 kHz), and the minimum of the real-sampling of sampling compensation is also 5 μs. For the [23] scheme, it is based on switching time prediction and use two-level modulation around \( v_g \) zero-crossing. Due to the increase of the bandwidth at the peak of \( i_o \), the current ripple and THD increases clearly, which is not suitable for small filter inductor or easily saturated inductor. Figure 11(b) shows the FFT analysis of the fixed sampling period, [23] scheme, and sampling compensation. The resonant frequency \( f_r \) is 5.627 kHz. It can be seen that the switching frequency can potentially enter the resonant frequency range when the variation of the switching frequency is wide, especially with the fixed sampling period method. In this case, the damping resistor must be used to damp the resonance. In contrast, with the proposed sampling compensation scheme in this paper, the switching frequency is relatively constant around 20 kHz so it will unlikely enter the resonant frequency range and trigger resonance. Therefore, the LCL filter design is easier and can effectively filter the switching frequency harmonics. In addition, the proposed control method has fewer low-frequency harmonics, as shown in Figure 11(c).

The simulation waveforms around \( v_g \) zero-crossing point with different fixed sampling period are depicted in Figure 12. As can be seen, the switching frequency of the fixed sampling period control varies clearly, and it is not stabilized at the setting value (20 kHz), even though the variable \( R_s \) has been accurately calculated by Equation (7). In Figure 12(b), the sampling frequency is increased to 1 MHz. As seen, the \( i_o \) is controlled in hysteresis band, but the improvement of switching frequency is limited.
Figure 11 depicts comparisons between various sampling methods: Fixed sampling period (top), Mixed-level ([23]) scheme (middle), proposed sampling compensation (bottom) (a) output current; (b) harmonics and THD; (c) low frequency harmonics.

FIGURE 12 Simulation results of output current and corresponding switching frequency during $v_{g}$ zero-crossing with the fixed sampling period: (a) Sampling with 200 kHz; (b) Sampling with 1 MHz.

Figure 13(a) depicts the control performance of [23] scheme around $v_{g}$ zero-crossing point. Although the switching frequency is almost stabilized at the setting value, a large current ripple is introduced. At the same time, it is hard to avoid switching frequency jitter at ‘three-two-level’ switching points. The simulation results of sampling compensation scheme are show in Figure 13(b). In comparison, the switching frequency can be almost stabilized at the setting value. It does not need to increase the hysteresis bandwidth (result in the increase of ripple current), and $i_o$ can be well controlled in the given hysteresis boundary. For the proposed scheme, the limitation is that there is still (only) one switching frequency jump every fundamental (line frequency) period (caused by the 0-state) around $v_{g}$ zero-crossing, as shown in Figure 13(b) below, which makes the switching frequency jitter unable to be completely eliminated, but the impact is very small. Considering the advantages of small current ripple and low sampling demand with the proposed scheme, the jitter limitation is not a concern.

The simulation results during reference step-change is shown in Figure 14. As seen, $i_o$ immediately tracks the step signal at the maximum available speed and is controlled within the hysteresis band without overshoot. This shows the advantages of hysteresis current control.

Consequently, simulation results show that the control performance of proposed scheme is better than the high frequency of fixed sampling and the [23] scheme in $v_{g}$ zero-crossing regions. The comparisons of different scheme are shown in Table 3, where the ☀ is “good,” the ☐ is “neutral,” and the ☖ is “bad.”
TABLE 3  The comparisons of different scheme during grid voltage zero-crossing

| Performance                  | Fixed sampling period scheme | Mixed-level scheme | Sampling compensation scheme |
|------------------------------|------------------------------|-------------------|-----------------------------|
| Sampling frequency           | ⊖ High sampling frequency is required | ⊖ Avoid redundant sampling by prediction | ⊖ Avoid redundant sampling by prediction |
| Stability of switching       | ⊖ It is hard to stabilize | ⊖ Two switching frequency jitter points | ⊖ One switching frequency jitter points |
| frequency                    | ⊖ Large ripple is introduced | ⊖ One switching frequency jitter points | ⊖ The ripple is smaller than others |
| Current ripple                | ⊖ Normal, but it needs high-speed sampling | ⊖ Prediction and two-three-level switching | ⊖ Prediction and virtual sampling |
| Control complexity           | ⊖ It is the simplest | ⊖ Prediction and virtual sampling | ⊖ Prediction and virtual sampling |

FIGURE 14  Simulation results during current reference step-change: (a) Output current; (b) Switching frequency

FIGURE 15  Simulation results of output current for (a) three-level T-type inverter, (b) three-level diode-clamped NPC inverter

The proposed method is now also tested in a three-level diode-clamped NPC inverter and the simulation results are shown in Figure 15. It can be seen that the proposed method yields similar results in both the three-level diode-clamped NPC and T-type converters. This is because the two three-level inverters have similar switching states and current response.

4.2  Experiments results

The proposed controller is tested on a 75-kVA laboratory prototype, which works as a current source and injects reactive current into the grid. The experimental platform is shown in Figure 16 in the revised manuscript. The prototype is controlled by a DSP (TMS320F28377). The target switching frequency is set as 20 kHz, the same as in the simulation model. The LCL filter with a cut-off frequency of 5.627 kHz can filter out all the switching frequency related harmonics. In addition, damping resistors are connected in series with the capacitor branch of the LCL filter to provide damping.

FIGURE 16  Experimental platform of the proposed T-type three-level inverter system

FIGURE 17  Experimental waveform of fixed sampling period control around \( \psi \) zero-crossing: (a) sampling with 200 kHz; (b) sampling with 1 MHz

The \( i_o \) waveform with the traditional fixed sampling period around \( \psi \) zero-crossing are shown in Figure 17, where Figure 17(a,b) show the \( i_o \) under the fixed sampling period control at 200 kHz and 1 MHz, respectively. The 200 kHz and 1 MHz sampling frequency can be implemented by the TMS320F28377.
DSP, which is used in the platform as shown in Figure 16. By comparing Figure 17(a,b), it can be seen that the tracking weakness can be improved partly, but the switching frequency cannot be stabilized near the setting value by simply increasing the sampling frequency. Therefore, a high sampling frequency alone is not enough to solve the problem, because the sampling point is not just near the hysteresis boundary and the delay is inevitable. In theory, only continuous models (infinite high sampling frequency) can realize that every state change occurs at the hysteresis boundary accurately in each time.

An experimental waveform with the [23] scheme hysteresis control is shown in Figure 18. It can be seen that the shortcomings of the [23] scheme are indeed as described in the paper. The current ripple is very large (e.g. 70 A), and there is a significant switching frequency jitter (5.5 kHz vs 19 kHz) at the switching points between the three-level and two-level modulation.

The proposed sampling compensation scheme can help overcome the shortcomings of tracking weakness and deviated switching frequency without high sampling frequency. The setting of the maximum sampling frequency is 200 kHz in experiment. As the experimental result of $i_{d}$ showed in Figure 19(a), the tracking weakness is nearly eliminated, and the switching frequency is stabilized within the range between 18 and 24 kHz around $v_g$ zero-crossing point. Figure 19(b) shows the current waveform and switching frequency of $i_{d}$ zero-crossing region. As seen, the switching frequency is around 23 kHz. The $i_{d}$ has only one large switching period of current free-wheeling (caused by a 0-state), but it avoids introducing excessive current ripple. In the experiment, the switching frequency is not as constant as that in the simulation, which is 20 kHz. This is because switching time prediction errors would be inevitably accumulated step by step due to practical issues, such as sampling delay, switching signal delay, dead time, and some other data processing errors. By adjusting the threshold of the prediction correction, the fluctuation range of the switching frequency can be further limited. Nevertheless, with the proposed method, the switching frequency is much more constant than those without the sampling compensation.

Regarding ensuring the quality of the grid current, firstly, the hysteresis control makes sure the low-frequency current harmonics are eliminated and the LCL filter with a cut-off frequency of 5.627 kHz can filter out all the switching frequency (around 20 kHz) related harmonics, so the grid current quality is guaranteed. Secondly, one of the main contributions of this paper is to make the switching frequency more constant around 20 kHz (rather than large variations in existing hysteresis control schemes). Therefore, the LCL filter design is easier and can effectively filter the switching frequency harmonics. Also, this relatively constant switching frequency around 20 kHz reduces the chances of triggering the resonant frequency of the LCL filter.

Figure 20(a,b) shows the experimental current of one fundamental cycle (50 Hz) with a fixed sampling frequency and a sampling compensated one, respectively. The currents include the inverter output current $i_{d}$ and the grid-side current $i_{grid}$. As seen, the current ripple of sampling compensation scheme is smaller than the fixed one. The inverter-side current FFT analysis is shown in Figure 20(c,d). As seen, the switching ripple is concentrated near the reference value with the proposed scheme. Figure 20(e,f) show the FFT analysis results of grid-side current with fixed and sampling compensation, respectively. At the same sampling frequency, the THD of the fixed sampling period control is 5.58%. By using the proposed sampling compensation scheme, the THD can be greatly reduced to 2.82%, and the low-frequency harmonics are reduced clearly. Therefore, the proposed scheme is helpful to improve the grid-side current quality of grid-connected inverter based on hysteresis control.
5 CONCLUSION

In hysteresis current control, to overcome the tracking weakness during $v_g$ zero-crossing for grid-connected three-level inverters, the sampling compensation scheme has been proposed. Analysis and simulations show the reasons of tracking weakness during $v_g$ zero-crossing, and large current ripple still exists in existing methods. By combining switching time prediction and virtual sampling, tracking weakness can be eliminated with a lower sampling frequency (20–200 kHz), a smaller current ripple, and only one switching period jitter point. The switching frequency can be stabilized around the setting value. At the same time, it does not affect the advantages of fast dynamic response and good robustness of hysteretic control. Due to the mitigation of tracking weakness and the stability of switching frequency, the THD of grid-side current is significantly reduced. The proposed scheme can provide guidelines for improving the hysteresis control performance of grid-connected three-level inverters.

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**APPENDIX**

The PLL control diagram is shown in Figure A.1. This PLL can effectively attenuate the high frequency harmonics, acting as a low-pass filter.

For the inverter as shown in Figure 2, when the two-level hysteresis control is used, the relation between the current-changing slope and the hysteresis bandwidth $B_{w2}$ can be deduced by

$$
\frac{B_{w2}}{T_f} = \frac{di(t)}{dt} = \frac{v_d/2 - v_f(t)}{L} \quad (A.1)
$$

$$
\frac{B_{w2}}{T_f} = \frac{di(t)}{dt} = \frac{v_d/2 + v_f(t)}{L} \quad (A.2)
$$

The equations are valid because the neutral of the load is connected to the dc-link midpoint.

The hysteresis bandwidth changed in real-time as

$$
B_{w2} = \frac{v^2_d}{4f_v v_f L} \quad (A.3)
$$

**FIGURE A.1** Diagram of the PLL

**FIGURE A.2** Diagram of the dc-link control: (a) the dc-link total voltages control; (b) the dc-link voltages balance control
The dc-link voltage controller is realized with a PI controller and is used to keep the overall dc-link voltage constant at the reference value. The whole dc-link voltage control diagram is shown in Figure A2(a) below. The error between the dc-link voltage reference and the real dc-link voltage goes through a PI controller and the output of the PI controller serves as the reference of the $d$-axis current reference. The $i_x^* (x = a, b, c)$ is reference current of each phase. For the three-level converter, the upper and the lower dc-link voltages have to be balanced, which is achieved also by a PI controller. The control diagram is shown in Figure A2(b) below: The error between upper dc voltage and lower dc voltage ($V_{up}$ and $V_{low}$) serves as the input of PI controller. The $i_{c,dc} (x = a, b, c)$ is the dc-link balance compensation component. Then, the $i_{c,dc}$ are added to the reference current $i_x^*$ achieve the dc-link voltage balance.

Given the dc-link voltage ripple is normally very small and there is current control loop to regulate the output current in response to the dc-link voltage change, therefore the impact of the dc-link voltage ripple on the output current is normally ignored in literature and applications.