A Comparison Between Automatically Versus Manually Parallelized NAS Benchmarks

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Abstract. We compare automatically and manually parallelized NAS Benchmarks in order to identify code sections that differ. We discuss opportunities for advancing automatic parallelizers. We find ten patterns that pose challenges for current parallelization technology. We also measure the potential impact of advanced techniques that could perform the needed transformations automatically. While some of our findings are not surprising and difficult to attain – compilers need to get better at identifying parallelism in outermost loops and in loops containing function calls – other opportunities are within reach and can make a difference. They include combining loops into parallel regions, avoiding load imbalance, and improving reduction parallelization. Advancing compilers through the study of hand-optimized code is a necessary path to move the forefront of compiler research. Very few recent papers have pursued this goal, however. The present work tries to fill this void.

Keywords: source-to-source automatic parallelizer · Cetus · NPB Benchmark · manually-parallelized programs · automatically-parallelized programs.

1 Introduction

Since the end of Dennard scaling [22] at the turn of the millennium, nearly all computer systems include parallel architectures that are exposed to their programmers. In the past two decades, we have witnessed a significant increase in computer applications in nearly all domains of science, engineering, business, and our daily lives. As a result, the number of program developers has drastically increased, including many software engineers trained on the intricacies of parallel computer architectures and applications, but also an even larger number of non-experts. Tools that help create and efficiently implement parallel applications on modern architectures are more important than ever. While the relevance of automatic parallelizers is obvious for non-expert programmers, the same tools can also greatly benefit the specialists, assisting them in efficiently performing many of the tedious programming tasks.

After four decades of research in automatic parallelization, a large number of techniques have been developed. Nevertheless, automatic parallelization tools succeed only in about half of today’s science and engineering applications. And there is little success in many of the business and daily-life applications, which represent the major part of today’s software. Users of parallelizers are often frustrated by the unpredictable performance of automatic tools, which at times degrade the speed below that of the original program. Manual parallelization is often a necessity, but its complexity and tediousness make it amenable to only a minority of highly trained experts. Even for these experts, creating parallel applications is an expensive and time-consuming task.
Developing tools that automate these tasks is even more challenging. One of the biggest questions is how to bring about advancements in this area. The premise of this paper is that we need to study representative applications, investigate how manual programmers have performed their tasks, compare the transformations they have applied with those of automatic parallelizers, and learn from these comparisons how to improve our tools. Amazingly, there are very few papers that pursue this direction. We will discuss these papers in the section on related work.

The present paper tries to fill this void. We identify programming patterns that differ between manually parallelized and auto-parallelized codes, find the limitations of auto-parallelizers, and suggest improvements for such tools, so that they generate programs that are closer to hand-optimized code.

We do this by studying the NAS Parallel Benchmark (NPB) applications [14]. The NPB applications are a representation of real-world applications. While their first release was in 1991, they are continually being modernized and include codes containing irregular code and data patterns. The OpenMP versions of NPB are used as our hand-parallelized applications, which we compare to the serial versions parallelized automatically by the Cetus translator [21]. Cetus is an advanced parallelizer and compiler infrastructure for C programs. We use it to represent modern parallelization technology.

The remainder of the paper is organized as follows. Section 2 outlines our experimental design. Section 3 identifies and measures the code sections that differ between manual and automatic parallelization. Section 4 presents the main findings, including a description of the code patterns that differ between automatically and manually parallelized applications, an assessment of the performance impact of each pattern, and a discussion of opportunities for compilers. We describe related work in Section 5, followed by conclusions in Section 6.

2 Experimental Design

Application Benchmarks: We use the NAS Parallel Benchmarks NPB 3.3, which includes serial, OpenMP, and MPI codes for ten applications. The original codes are written in Fortran, but we use the variants written in C [18]. We evaluate the codes EP, IS, BT, SP, MG, and CG, which present opportunities for automatic parallelization. For our experiments, we measure the performance of the applications for input Class A, which is a small data set, but representative of larger sets, as we will show in section 3.4. We report the average performance of three program runs.

Automatic Parallelization: We use the Cetus open-source automatic parallelizer, which is a source-to-source translator for C programs. Cetus represents some of the most advanced parallelization technology [2, 13, 16], including symbolic program analysis. It generates OpenMP-annotated C code on output, invoking GCC as a backend code generator (GCC v4.8.5 with option -O3). We ran Cetus with its default option to parallelize the codes. Among the major passes applied [4] are range analysis, points-to and alias analysis, data dependence analysis, data privatization, induction variable substitution, and reduction parallelization. This experiment uses Cetus as a representative of current auto-parallelizers. Cetus has been actively maintained, with recent improvements [3].

Platforms: The key measurements are performed on a four-core system. All CPUs are located on one NUMA node. Each CPU has a 512 KiB L1d cache and a 512 KiB L1i cache, as well as a 4 MiB L2 cache. This system provides full access for easy experimentation; we refer to it as the Interactive System.

To validate our findings on a larger system, we also make use of the University of Delaware (UD)’s Caviness Cluster [20]. Caviness is a distributed-memory Linux cluster that was initially deployed in
July 2018. A variety of compute nodes are present with different configurations on this cluster. Each node consists of multi-core processors (CPUs), memory, and local disk space. It consists of 126 compute nodes (4536 cores, 24.6 TB memory). The nodes are built of Intel “Broadwell” 18-core processors in a dual-socket configuration for 36 cores per node. Experiments on Caviness need to be submitted via batch queues; we refer to this cluster as the Batch System.

3 Examining Differences between Manual and Automatic Parallelization

This section presents overall experimental results. We compare the performance of the automatically and manually parallelized applications (Section 3.1) and identify program sections that exhibit differences (Section 3.2) between auto- and hand-optimized. We also measure the overheads introduced by program parallelization (Section 3.3). These measurements were taken on the 4-core Interactive System, introduced in Section 2, using data class A. To validate our findings on larger data sets and systems, Section 3.4 and Section 3.5 also measure and discuss the benchmarks for data class B and up to 36 cores, using the Batch System described in Section 2.

3.1 Performance of Auto-Parallelized and Hand-Parallelized Applications on the Interactive System Using 1 and 4 Cores

Table 1 shows execution times and speedups of the auto-parallelized and hand-parallelized codes, running on the 4-core Interactive System, using the Class A data set.

| Application Name | Auto-Parallelized Code | Manually-Parallelized Code |
|------------------|------------------------|-----------------------------|
|                  | Execution Time(s)      | Execution Time(s)           | Speedup | Execution Time(s) | Execution Time(s) | Speedup |
|                  | (1 core)               | (4 cores)                   |         | (1 core)          | (4 cores)         |         |
| SP               | 417                    | 362                         | 1.2     | 425               | 110               | 3.8     |
| BT               | 424                    | 356                         | 1.2     | 450               | 116               | 3.8     |
| EP               | 86                     | 63                          | 1.4     | 87                | 22                | 3.9     |
| MG               | 35                     | 15                          | 2.3     | 31                | 8                 | 3.8     |
| IS               | 8                      | 7                           | 1.1     | 9                 | 3                 | 3.0     |
| CG               | 12                     | 5                           | 2.4     | 11                | 3                 | 3.7     |

With auto-parallelization, the applications SP, BT, EP, MG, and CG have gained noticeable speedup. For the IS application, there is little gain; the code has not been parallelized substantially due to irregular data patterns.

The hand-parallelized code yields speedups for all applications. On average, the hand-parallelized codes perform 2.5 times faster than auto-parallelized.

3.2 Performance of Individual Code Sections

Table 2 on page 4 shows the differences between automatically and manually parallelized code sections. In addition to the execution times, the table identifies the differing programming patterns.
Table 2: Differences in individual code sections between auto- and hand-parallelized applications

| App Loop Name | Auto | Manual | P1 | P2 | P3 | P4 | P5 | P6 | P7 | P8 | P9 |
|---------------|------|--------|----|----|----|----|----|----|----|----|----|
| CG main#1-#3  | 2.13 | 0.57   | 1  | 0  | 3  | 0  | 0  | 1  | 0  | 0  | 0  |
| CG conj_grad#0-#4 | 0.15 | 0.15   | 0  | 0  | 5  | 0  | 0  | 0  | 1  | 1  |    |
| CG sparse#6    | 0.03 | 0.01   | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| CG Program     | 5.00 | 3.00   | 3  | 0  | 8  | 0  | 0  | 1  | 0  | 1  | 1  |
| IS create_seq#0| 3.48 | 0.88   | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 1  |
| IS full_verify #0 | 0.12 | 0.05   | 1  | 0  | 1  | 1  | 1  | 0  | 0  | 1  |    |
| IS rank#1-#7   | 0.38 | 0.09   | 1  | 0  | 3  | 1  | 1  | 1  | 0  | 0  | 1  |
| IS Program     | 7.39 | 2.80   | 2  | 1  | 5  | 2  | 2  | 3  | 0  | 0  | 3  |
| MG rprj3#0     | 0.32 | 0.08   | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  |
| MG norm2n3#0   | 0.42 | 0.12   | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 1  |
| MG comm3#0     | 0.003| 0.003  | 0  | 0  | 3  | 0  | 0  | 0  | 0  | 1  | 1  |
| MG zran3#0     | 1.77 | 0.43   | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 1  |
| MG zran3#1-#3  | 0.25 | 0.03   | 1  | 1  | 3  | 0  | 0  | 0  | 0  | 0  | 1  |
| MG Program     | 15.4 | 8.54   | 4  | 3  | 9  | 0  | 0  | 0  | 2  | 4  |    |
| EP main#0      | 0.002| 0.007  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| EP main#3      | 62.5 | 22.4   | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 1  |
| EP Program     | 63.0 | 22.0   | 1  | 1  | 2  | 0  | 0  | 2  | 1  | 0  | 1  |
| BT initialize#0-#7 | 0.44 | 0.12   | 8  | 7  | 8  | 0  | 0  | 0  | 6  | 0  |    |
| BT exact_rhs#0-#4 | 0.52 | 0.14   | 5  | 3  | 5  | 0  | 0  | 1  | 0  | 2  | 0  |
| BT compute_rhs#0-#10 | 20.5 | 20.4   | 0  | 0  | 11 | 0  | 0  | 0  | 0  | 7  | 0  |
| BT x_solve#0    | 110  | 31.3   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| BT y_solve#0    | 110  | 31.5   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| BT z_solve#0    | 113  | 32.2   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| BT error_norm#1 | 0.08 | 0.02   | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 1  |
| BT rhs_norm#1   | 0.004| 0.003  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 1  |    |
| BT Program      | 356  | 116    | 17 | 14| 29 | 0  | 0  | 4  | 2  | 17 | 2  |
| SP error_norm#1 | 0.04 | 0.01   | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 1  |
| SP rhs_norm#1   | 0.003| 0.002  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 1  |
| SP exact_rhs#0-#4 | 0.77 | 0.13   | 1  | 3  | 5  | 0  | 0  | 1  | 0  | 2  | 0  |
| SP initialize#0-#7 | 0.14 | 0.04   | 1  | 7  | 8  | 0  | 0  | 0  | 1  | 0  | 0  |
| SP lhsinit#0    | 0.71 | 0.13   | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| SP lhsinitj#0   | 1.10 | 0.30   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| SP compute_rhs#0-#10 | 23.3 | 20.1   | 0  | 0  | 11 | 0  | 0  | 0  | 0  | 7  | 0  |
| SP x_solve#0    | 87.2 | 20.4   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| SP y_solve#0    | 123  | 20.8   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| SP z_solve#0    | 123  | 21.4   | 1  | 1  | 1  | 0  | 0  | 1  | 0  | 0  | 0  |
| SP Program      | 362  | 111    | 7  | 14| 30 | 0  | 0  | 6  | 2  | 17 | 2  |

Auto– Execution time of auto-parallelized code (seconds) on 4 cores
Manual– Execution time of manually-parallelized code (seconds) on 4 cores
P1– Number of loops in which the outermost loop is parallelized; more on section 4.1
P2– Number of loops containing function calls inside the region; more on section 4.2
P3– Number of loops inside the parallel region; more on section 4.3
P4– Dynamic schedule (1 means the pattern is applied); more on section 4.4
P5– Irregular patterns like indirect array accesses (1 means the pattern is applied); more on section 4.5
P6– Threadprivate data access (1 means Threadprivate data has been accessed); more on section 4.6
P7– Array reduction (1 means the pattern is applied); more on section 4.7
P8– Number of NOWAIT clauses; more on section 4.8
P9– Code modification (1 means the pattern is applied); more on section 4.10
We number adjacent (nests of) loops in each subroutine from 0. For example, main\#1-\#3 indicates the second through the fourth for loops in function main.

Our comparison of auto- and hand-parallelized codes revealed several differing program patterns. The table shows which of these patterns have been used in the manually parallelized codes. Section 4 explains each of these patterns in more detail and quantifies the performance differences they make. We omit code sections with insignificant performance differences.

We examine the reasons behind the differences between the auto-parallelized and hand-parallelized execution times in Section 4 and discuss the programming patterns responsible for these differences.

### 3.3 Overhead of Parallel Transformations in Hand-parallelized Applications

The inserted OpenMP directives (also called compiler pragmas) determine how the compiler and runtime system transform the code, manage and synchronize teams of threads and distribute work among the threads. Table 3 shows the serial and 1-core parallel execution of the hand-parallelized applications, exhibiting the introduced overhead. Two of the six applications incur overheads of more than 3% while in two of the applications the performance improves by 9% and 12%. Some of the sources of overhead are:

- OpenMP in such compilers as GCC, LLVM, and Intel ICC is implemented using outlining \[12\], extracting the parallel region into its own function. The extra function call, initiating communications with the helper threads, copying shared variables to the helpers, assigning work shares, as well as synchronizing the threads, all contribute to this overhead.
- In addition, we found that parallel regions that use thread-private data may incur extra overheads, as described in more detail in Section 4.6.
- Moreover, the addition of OpenMP directives can sometimes prevent the compiler from performing certain optimizations.

### 3.4 Application Scalability with Increasing Data Set and System Performance

To verify the validity of our findings on larger systems and data sets, we executed our benchmarks on the Batch System described in Section 2. We used the same core counts as in the prior sections (1 and 4 cores) but included in our measurements data set Class B, next to Class A.

| Application Name | Serial Execution Time (s) | Execution Time of hand-parallelized code(s) on 1 core | Difference |
|------------------|--------------------------|------------------------------------------------------|------------|
| SP               | 416                      | 425                                                  | 3%         |
| BT               | 414                      | 450                                                  | 9%         |
| EP               | 86                       | 87                                                   | 1%         |
| MG               | 35                       | 31                                                   | -12%       |
| IS               | 8                        | 9                                                    | 11%        |
| CG               | 12                       | 11                                                   | -9%        |
Tables 4 and 5 show the code performance on the Batch System using Class A and Class B data sets, respectively. Using Class A, the hand-parallelized codes show an average 4-core speedup of 3.6. The corresponding gain for the auto-parallelized codes is 1.9.

Using the larger class-B data set, the average speedups are close to those for Class A – 3.7 for manually parallelized and 2.1 for automatically parallelized. While the hand-parallelized codes achieve a speedup close to the available core count, four out of the six auto-parallelized codes yield substantially lower performance. These findings match the conclusions obtained for Class A on the Interactive System, justifying the use of the more nimble Interactive System and Class A for our detailed experiments.

### Table 4: Performance of auto- and hand-parallelized codes in seconds. Parallel Execution is measured on 1 and 4 cores. Parallel Speedup is calculated as the parallel run-time on 1-core divided by the run-time on 4-cores. The measurements use Class A data set and the Batch System.

| Application Name | Auto-Parallelized Code | Manually-Parallelized Code |
|------------------|-------------------------|---------------------------|
|                  | Execution Time(s)       | Execution Time(s)         |
|                  | (1 core)                | (4 cores)                |
|                  | Speedup                 | Execution Time(s)         |
|                  |                         | (1 core)                |
| SP               | 134                     | 133                       |
| BT               | 146                     | 155                       |
| EP               | 33                      | 33                        |
| MG               | 5.7                     | 5.7                       |
| IS               | 0.8                     | 0.7                       |
| CG               | 2                       | 2                         |

### Table 5: Performance of auto- and hand-parallelized codes in seconds. Parallel Execution is measured on 1 and 4 cores. Parallel Speedup is calculated as the parallel run-time on 1-core divided by the run-time on 4-cores. The measurements use Class B data set and the Batch System.

| Application Name | Auto-Parallelized Code | Manually-Parallelized Code |
|------------------|-------------------------|---------------------------|
|                  | Execution Time(s)       | Execution Time(s)         |
|                  | (1 core)                | (4 cores)                |
|                  | Speedup                 | Execution Time(s)         |
|                  |                         | (1 core)                |
| SP               | 543                     | 556                       |
| BT               | 595                     | 638                       |
| EP               | 133                     | 129                       |
| MG               | 26                      | 25.5                      |
| IS               | 3.4                     | 3.2                       |
| CG               | 84                      | 80                        |

3.5 Application Scalability with Increasing Core Counts Using Class B Data Set

The previous section shows good efficiency of the hand-parallelized codes on four cores. The auto-parallelized versions execute at about half that performance, on average. This section tests the scalability of programs to up to 36 cores, using the Class B data set.
Figures 1 and 2 show the code execution times and speedups, respectively, with increasing core counts. Auto-parallelized codes cannot efficiently utilize the available cores. Except for CG, and MG, adding more than 4 cores does not increase the speed. When increasing the number of cores beyond 32, the performance gain is not significant and may even worsen. For the hand-parallelized codes, as the number of cores increases from 32 to 36, the performance continues to improve, except for MG. In general, the hand-parallelized benchmarks make efficient use of the available cores.
Overall, the qualitative findings of the 4-core measurements remain the same: While the hand-parallelized codes show good scalability, the performance of the auto-parallelized versions is limited. That limitation increases with higher core counts. Hence the importance of the techniques presented in the next section, which aim to bring the efficiency of the auto-parallelized codes closer to manually parallelized, will be even larger than shown by the 4-core evaluation.

4 Code Patterns, Performance Impact, Opportunities for Compilers

We now analyze the program sections in each benchmark that differ between the manually and automatically parallelized versions. We have identified ten programming patterns that represent these differences. In rough order of importance, we first explain the pattern, followed by assessing the performance impact of enabling/disabling the pattern. We then discuss the potential for improving compilers to implement the pattern. We quantify the potential impact of these techniques on our 4-core Interactive System. As mentioned at the end of Section 3, these numbers represent lower bounds, which will increase for systems with higher core counts.

4.1 Parallelizing Nested Loops at the Outermost Level Possible

The Pattern It is well understood that outermost parallelism yields the best performance and that automatic parallelization may fail to do so, finding parallelism in inner loops, only. Running outermost loops in parallel minimizes the number of parallel loop invocations, and the associated fork/join overheads, including implicit barriers at the loop end. Not surprisingly, we found several program sections that differed between manually and automatically parallelized in this way. Among the causes were irregular data accesses, function calls (discussed later), or dependences that could not be disproven.

Performance Impact Subroutines x_solve(), y_solve(), and z_solve() in programs BT and SP are examples of compute-intensive functions that are not parallelized at the outermost level by the Cetus compiler – due to function calls present in the outermost loop. Table 6 shows the differences between the auto- and hand-parallelized code execution times.

Table 6: Impact of parallelizing the outermost loop in nested loops, comparing the execution time of the Cetus-parallelized code with the manually parallelized code.

| Application Name | Loop Name  | Technique Not Applied | Technique Applied | Impact   |
|------------------|------------|-----------------------|-------------------|----------|
| BT               | x_solve#0  | 110                   | 31                | 255%     |
| BT               | y_solve#0  | 110                   | 31                | 255%     |
| BT               | z_solve#0  | 113                   | 32                | 253%     |
| BT               | program    | 356                   | 116               | 206%     |
| SP               | x_solve#0  | 87                    | 20                | 335%     |
| SP               | y_solve#0  | 123                   | 21                | 486%     |
| SP               | z_solve#0  | 123                   | 21                | 486%     |
| SP               | program    | 362                   | 111               | 226%     |
Opportunities for Compilers  The presence of function calls requires inter-procedural analysis or inline expansion capabilities, which we will discuss in the following subsection. Irregular access patterns have long been a challenge for compilers, with both run-time and recent compile-time approaches pursuing improvements. For disproving data dependences, we have often found that the opportunity is in the propagation of information across the program (such as interprocedural symbolic analysis) rather than in increasing the power of data dependence tests themselves.

4.2 Parallelizing Loops Containing Function Calls

The Pattern  Most auto-parallelizers, including Cetus, do not consider loops with function calls or I/O statements for parallelization, unless those functions are known to be side-effect free. Our study found many examples in which a function call inside a loop prevented auto-parallelization. The same loops were parallelized in the manually parallelized codes.

Inline expansion, which replaces a function call with the body of the called subroutine, can help parallelize such patterns. Users of the Cetus compiler have that option available. We will measure the effect of doing so, next.

Performance Impact  We performed an experiment to determine how much parallelization is enabled through inline expansion in Cetus-parallelized codes. Table 7 shows the result.

Table 7: Impact of inlining in parallelizing automatically parallelized codes; Comparing the execution time of auto-parallelized codes before and after inlining.

| App Name | Loop Name | Number of Inlined Functions | Paralleled after Inlining? | Technique Not Applied Inlining Technique Applied | Impact |
|----------|-----------|-----------------------------|---------------------------|-----------------------------------------------|--------|
| BT       | initialize#0-#7   | 9                           | Yes¹                      | 0.44 0.14                                       | 214%   |
| BT       | exact_rhs#0-#4    | 3                           | Yes²                      | 0.52 0.63                                       | -17%   |
| BT       | x_solve#0         | 8                           | No                        | 110 122                                         | -10%   |
| BT       | y_solve#0         | 8                           | No                        | 110 123                                         | -11%   |
| BT       | z_solve#0         | 8                           | No                        | 113 124                                         | -9%    |
| BT       | error_norm#1      | 1                           | Yes³                      | 0.08 0.03                                       | 167%   |
| BT       | Program           | 356                         |                           | 395 395                                         | -10%   |
| SP       | initialize#0-#7   | 9                           | Yes¹                      | 0.14 0.04                                       | 250%   |
| SP       | exact_rhs#0-#4    | 3                           | Yes²                      | 0.77 0.7                                        | 10%    |
| SP       | x_solve#0         | 1                           | No                        | 87 87                                           | 0%     |
| SP       | y_solve#0         | 1                           | No                        | 123 124                                         | -1%    |
| SP       | z_solve#0         | 1                           | No                        | 123 123                                         | 0%     |
| SP       | error_norm#1      | 1                           | Yes³                      | 0.04 0.03                                       | 33%    |
| SP       | Program           | 362                         |                           | 377 377                                         | -4%    |

¹ In nested loop structures, the outermost loops are parallelized. In manually-parallelized code, however, all parallel loops are included in a parallel region.
² In nested loop structures, inner loops are parallelized.
³ While the outermost loop is parallelized, the array reduction implementation differs from the hand-parallelized code that will be discussed later.
We found that auto-parallelization indeed could detect additional parallelism in several of the loops in question after applying inlining. As displayed in Table 7, subroutine `initialize()` in both BT and SP shows significant performance gain due to parallelization of the outermost loops. However, in `exact_rhs()`, the transformation led to performance degradation. While additional loops could be parallelized, these were inner loops where parallelization was not profitable. What’s more, the most compute-intensive loops, in subroutines `x_solve()`, `y_solve()`, and `z_solve()` of both applications, remained unaffected by inline expansion, as Cetus is still unable to disprove data dependences.

**Opportunities for Compilers**  Despite studies on interprocedural analysis (IPA) that have been carried out for more than three decades, IPA is not available in most compilers. Among the reasons are the complexity of the technique, the fact that most analyses need specialized IPA algorithms, and the resulting increase in compilation times.

By interacting with the user, it is possible to identify user functions that have no side effects and add them to the default list of side-effect-free functions, which consist primarily of math functions. Other opportunities include selective subroutine inline expansion during the compiler analysis only. The former technique could identify additional parallelism with user input, while the latter would eliminate overheads, such as excessive code growth.

### 4.3 Parallel Regions Enclosing Multiple Parallel Loops

**The Pattern**  In OpenMP, multiple adjacent parallel loops can be converted into a *parallel region*. This way, the parallel threads are spawned only once, at the beginning of the region, reducing fork/join overhead. The original parallel loops will become *worksharing constructs*, which simply distribute their iterations onto the available threads. In some cases, the programmers had inserted `NOWAIT` clauses to eliminate barrier synchronizations at the end of the worksharing constructs. In the hand-parallelized codes, we found this pattern frequently. By contrast, auto-parallelizers, including Cetus, typically examine and parallelize loops individually.

**Performance Impact**  We have measured the impact of such a technique by converting the hand-parallelized programs to variants without parallel regions. The loops inside the regions were changed to individual parallel loops. Note that doing so also forces a barrier synchronization at the end of each parallel loop. The results are presented in Table 8.

| App Name | Loop Name       | Number of Loops | Technique Not Applied | Technique Applied | Impact |
|----------|-----------------|-----------------|-----------------------|-------------------|--------|
| MG       | comm3#0-#2      | 3               | 0.003                 | 0.003             | 0%     |
| MG       | zran3#1-#3      | 3               | 0.034                 | 0.033             | 4%     |
| MG       | Program         | 6               | 9                     | 8.5               | 6%     |
| BT       | initialize#0-#7 | 8               | 0.124                 | 0.116             | 7%     |
| BT       | exact_rhs#0-#4  | 5               | 0.167                 | 0.142             | 18%    |
| BT       | compute_rhs#0-#10 | 11             | 0.117                 | 0.108             | 8%     |
| BT       | Program         | 24              | 129                   | 116               | 11%    |
Opportunities for Compilers  Developing transformations that combine adjacent parallel loops into a parallel region seems feasible in some situations, but we are not aware of auto-parallelizers that do so. In other cases, creating parallel regions can be challenging because sequential code sections may be present between the parallel loops. There exists work on eliminating barrier synchronization, which can be incorporated into such techniques.

4.4 Avoiding Load Imbalance Through Dynamic Scheduling

The Pattern  Load imbalance can be caused by the uneven distribution of work across worker threads. Loop scheduling defines chunks of loop iterations and their distribution onto the threads. In loops that are prone to uneven workload, due to conditional execution or work that depends on the iteration number, loop scheduling can affect performance noticeably. Two schedule clauses offered by OpenMP for resolving load imbalance are dynamic and guided. They make scheduling decisions at run-time, assigning chunks of iterations to idle threads.

The developers of the hand-parallelized codes have made use of these clauses. By contrast, the Cetus compiler currently does not change the default loop schedule, which is the static distribution of an equal share of iterations to all worker threads.

Performance Impact  We have found some loops where loop scheduling made a substantial difference. Table 9 shows two such loops in the IS program. The improved code performance of 43% and 17%, respectively, translates to a noticeable overall program speed improvement of 6%. The impact of dynamic scheduling on the whole application is significant, as the rank function is invoked multiple times.

Table 9: Impact of adding dynamic scheduling. The execution time of the code when scheduling is disabled is compared to the execution time of the manually parallelized code.

| Application Name | Loop Name   | Technique Not Applied | Technique Applied | Impact |
|------------------|-------------|-----------------------|-------------------|--------|
| IS               | full_verify#0 | 0.07                  | 0.05              | 43%    |
| IS               | rank#1-#7   | 0.10                  | 0.09              | 17%    |
| IS               | program     | 2.14                  | 2.02              | 6%     |

Opportunities for Compilers  Program and loop workloads are affected by both program and execution characteristics. Dynamic factors, such as external programs in shared machines, and conditional executions guided by input data, are difficult to assess. However, the compiler can analyze programs for conditional execution patterns that may depend on input data, iteration numbers that tend to load threads unevenly, and inner loops whose workload depends on outer loop iterations (e.g., triangular loops).

4.5 Analyzing Irregular Data Access Patterns in Hand-parallelized Codes

The Pattern  Applications that have irregular data access patterns with complex code structures prevent auto-parallelizers from succeeding.

The IS application exhibits such patterns. The loops full_verify#0, rank#0, rank#2, rank#4, and rank#6 include indirect array accesses, which prevents Cetus from detecting parallelism.
Performance Impact Table 10 reports execution times of these loops in the IS application when they are not parallelized by the auto-parallelizer due to such patterns, and when they are parallelized in the manually parallelized code.

Table 10: Impact of parallelizing irregular patterns. The execution time of the auto-parallelized code, where irregular patterns remain serial, is compared to the execution time of the manually parallelized code, where the same loops are parallelized.

| Application Name | Loop Name     | Technique Not Applied | Technique Applied | Impact |
|------------------|---------------|-----------------------|-------------------|--------|
| IS               | full_verify#0 | 0.12                  | 0.05              | 135%   |
| IS               | rank#1-#7     | 0.38                  | 0.09              | 318%   |
| IS               | program       | 7.39                  | 2.80              | 163%   |

Opportunities for Compilers Loops containing subscripted subscripts are among the most complex patterns for compilers to analyze. A number of run-time techniques have been developed, such as run-time data-dependence tests and inspector-executor schemes. Recent work has also begun to develop compile-time techniques based on the observation that, in some cases, the information needed to prove the absence of data dependences is present in the application program [3] [5].

4.6 Threadprivate Data

Pattern Explanation The OpenMP threadprivate directive specifies that variables are replicated, with a copy being kept in each thread. It privatizes static or global variables that are modified by multiple parallel regions. Threadprivate variables persist across regions. The manually parallelized benchmarks make use of this concept in a number of program sections.

Auto-parallelizers, including Cetus, do not create threadprivate data. Data that need to be replicated across threads and persist across parallel regions or loops need to be implemented through data expansion or copying region/loop-private data in and out – sometimes through first/last-private clauses.

Performance Impact We measured the impact of using threadprivate data by considering those program sections where conversion to loop-private data was possible. We compared the performance of the variants without threadprivate data (loop-private data only) with the hand-parallelized variants, which use threadprivate data.

The result was unexpected. Table 11 on page 13 shows that using threadprivate data lowers the performance in all of our cases. The compute-intensive loops in BT, subroutine x/y/z_solve, see a 25% performance reduction. The superior performance of regions without the use of threadprivate data is consistent with the findings of others [11], who attribute this effect to inefficient OpenMP implementations.

We did not measure other program sections where additional programming steps would be necessary for the transformation to region/loop-private data. In these cases, the additional steps would likely add overhead, making the threadprivate variant more desirable.
Table 11: Impact of using Threadprivate directives. We compare the execution time of the code where threadprivate data is replaced by loop-private data, with the execution time of the manually parallelized code.

| Application Name | Loop Name | Technique Not Applied | Technique Applied | Impact  |
|------------------|-----------|-----------------------|-------------------|---------|
| EP               | main#0    | 0.003                 | 0.006             | -50%    |
| EP               | main#3    | 20.93                 | 22.40             | -7%     |
| EP Program       |           | 21.0                  | 22.5              | -7%     |
| BT               | exact_rhs#0-#4 | 0.055           | 0.142             | -61%    |
| BT               | x_solve#0  | 23.43                 | 31.24             | -25%    |
| BT               | y_solve#0  | 23.63                 | 31.51             | -25%    |
| BT               | z_solve#0  | 24.45                 | 32.17             | -24%    |
| BT Program       |           | 93                    | 116               | -20%    |

**Opportunities for Compilers** Identifying threadprivate variables would involve analyses similar to current data privatization, combined with liveness analysis across loops. While this appears feasible, careful consideration will need to be given to profitability, so as to avoid situations with negative impacts.

### 4.7 Array Reductions

**The Pattern** Reduction operations are parallelized as follows: Each thread concurrently performs a reduction operation on the assigned loop iterations, creating partial results, followed by a step that combines the partial results. We have found differences in this combination step. For array reductions, the hand-parallelized versions perform the needed mutual exclusion operation on each element individually, using an OpenMP `atomic` construct. By contrast, the Cetus implementation performs the mutual exclusion for the entire array, by means of a `critical section`. This is the major difference, next to a minor variation in how data is allocated.

The following example is taken from the BT, rhs_norm() subroutine. A reduction optimization can be applied to the `rms` array shown in Listing 1.1 on line 6, using a `(+) reduction operator.

```plaintext
1 # Listing 1.1: Example taken from the BT rhs_norm() procedure in which an array reduction technique can be applied
2 for (k = 1; k <= grid_points[2]-2; k++) {
3     for (j = 1; j <= grid_points[1]-2; j++) {
4         for (i = 1; i <= grid_points[0]-2; i++) {
5             for (m = 0; m < 5; m++) {
6                 add = rhs[k][j][i][m];
7                 rms[m] = rms[m] + add*add;
8             }
9         }
10     }
```

Listing 1.1 on page 14 shows how Cetus implements array reduction. On line 3, the temporary reduction array, `reduce`, is dynamically allocated in shared space and initialized by the loop on line 5. The array is used on line 20 to perform the partial reduction. On line 26, a `Critical construct is used
to protect the concurrent update of rms by multiple threads. The critical section encloses a loop that will be executed by each thread sequentially.

```c
#pragma omp parallel if ((10000<((((((−43L+(92L*grid_points[0L]))+(86L*
grid_points[1L]))+(89L*grid_points[2L]))+((−46L*grid_points[0L])*
grid_points[1L]))+((−46L*grid_points[0L])*grid_points[2L]))+((−43L*
grid_points[1L])*grid_points[2L]))+(((23L*grid_points[0L])*grid_points[1L]
)*grid_points[2L]))) ) private(add, i, j, k, m) {
  double * reduce = (double *) malloc(5*sizeof(double));
  int reduce_span_0;
  for (reduce_span_0=0; reduce_span_0<5; reduce_span_0++) {
    reduce[reduce_span_0]=0;
  }
  #pragma loop name rhs_norm#1
  #pragma omp for
  for (k=1; k<=(grid_points[2]-2); k++) {
    #pragma loop name rhs_norm#1#0
    for (j=1; j<=(grid_points[1]-2); j++) {
      #pragma loop name rhs_norm#1#0#0
      for (i=1; i<=(grid_points[0]-2); i++) {
        #pragma loop name rhs_norm#1#0#0#0
        for (m=0; m<5; m++) {
          add=rhs[k][j][i][m];
          reduce[m]=(reduce[m]+(add*add));
        }
      }
    }
  }
  #pragma omp critical
  { for (reduce_span_0=0; reduce_span_0<5; reduce_span_0++) {
    rms[reduce_span_0]+=reduce[reduce_span_0];
  }
  }
} //end of parallel region
```

Listing 1.2: Cetus implementation of the array reduction

Listing 1.3 on page 15 demonstrates how array reduction is implemented in the hand-parallelized code in the same example. This implementation differs from the previous implementation in the following ways:

- Using a privatized version of the reduction array rms_local, instead of a dynamically allocated array.
- On line 7, a NOWAIT clause is used to omit the barrier at the end of the for loop, allowing each thread to immediately proceed to the update step.
- Using an atomic construct inside the for loop on line 18 to combine the partial results.
A Comparison Between Automatically Versus Manually Parallelized NAS Benchmarks

Listing 1.3: Array reduction implemented in hand-parallelized code

double rms_local[5];

#pragma omp parallel default(shared) private(i,j,k,m,add,rms_local) shared(rms)
{
    for (m = 0; m < 5; m++) {
        rms_local[m] = 0.0;
    }

#pragma omp for nowait
for (k = 1; k <= grid_points[2]-2; k++) {
    for (j = 1; j <= grid_points[1]-2; j++) {
        for (i = 1; i <= grid_points[0]-2; i++) {
            for (m = 0; m < 5; m++) {
                add = rhs[k][j][i][m];
                rms_local[m] = rms_local[m] + add*add;
            }
        }
    }
}

#pragma omp atomic
for (m = 0; m < 5; m++) {
    rms[m] += rms_local[m];
}
} //end of parallel region

Performance Impact  We compared the two variants, individual element synchronization (manual) and overall synchronization (automatic), by replacing two of the array reduction patterns in the hand-parallelized codes with the Cetus implementation scheme. We measured the execution time of those code sections and the entire program.

Table 12 shows a significant performance impact on the two loops. The overall effect in the overall programs is minor, as loop rhs_norm#1 is small and executed once per application in both SP and BT. In general, as reduction operations can show up in compute-intensive sections of programs, the impact may be much larger, however.

Table 12: The table compares the performance of the Cetus-applied array-reduction transformation versus the manually applied technique in the hand-parallelized codes.

| Application Name | Loop Name  | Technique Not Applied (Cetus) | Technique Applied (Manual) | Impact |
|------------------|------------|--------------------------------|----------------------------|--------|
| BT               | rhs_norm#1 | 0.005                          | 0.003                      | 66%    |
| BT               | program    | 117                            | 116                        | 1%     |
| SP               | rhs_norm#1 | 0.006                          | 0.002                      | 200%   |
| SP               | program    | 112                            | 111                        | 1%     |
Opportunities for Compilers

Compilers can easily transform array reductions in either of the described variants. The choice of best implementation depends on several factors, including the efficiency of implementation of the OpenMP atomic directive. If the implementation simply uses a critical section (which we have seen in some OpenMP libraries), the current Cetus transformation likely performs the same or better. This calls for compilers having knowledge of architectural and platform parameters, which we will discuss more in Section 4.9 on conditional parallelization.

4.8 NOWAIT -- Eliminating Barrier Synchronizations

The Pattern

A barrier is implicitly included at the end of some OpenMP constructs, including parallel, for, and single constructs. This barrier is the safe default so that all threads have completed their share of work before proceeding with the execution. This synchronization is not needed if threads do not access data previously operated on by a different thread or on the last worksharing loop inside a parallel region. The OpenMP NOWAIT clause eliminates the barrier.

NOWAIT clauses have been inserted on many parallel loops inside the parallel regions in the hand-parallelized programs, reducing substantial overhead. The auto-parallelized code do not include such techniques.

Performance Impact

In order to test the performance impact of the technique, we have created program variants of hand-parallelized codes with removed NOWAIT clauses. Table [13] on page [17] compares these codes with the hand-parallelized variants. The impact in most of the programs is only about 1%, even though individual loops see a gain of up to 16%. It is likely that the impact would increase with a larger number of threads (recall that we use four) or in programs/loops with imbalanced load.

Opportunities for Compilers

Compile-time techniques for barrier elimination have been explored. Engineering them into available compilers is still an opportunity to be seized. Given the relatively minor impact, other techniques may need to be prioritized. Note also that this technique is related to enclosing loops in a parallel region.
### Table 13: Impact of Eliminating Barrier Synchronization: Execution times of removed versus present NOWAIT clauses in hand-parallelized codes.

| Application Name | Loop Name        | Number of NOWAIT Clauses | Technique Not Applied | Technique Applied | Impact |
|------------------|------------------|--------------------------|-----------------------|-------------------|--------|
| CG               | Conj_grad#0-4    | 1                        | 0.173                 | 0.149             | 16%    |
| CG               | program          | 1                        | 3                     | 2.98              | 1%     |
| MG               | norm2u3#0        | 1                        | 0.121                 | 0.119             | 2%     |
| MG               | comm3#0          | 1                        | 0.003                 | 0.003             | 0%     |
| MG               | program          | 2                        | 8.7                   | 8.5               | 2%     |
| BT               | initialize#0-#7  | 6                        | 0.116                 | 0.116             | 0%     |
| BT               | exact_rhs#0-#4   | 2                        | 0.142                 | 0.142             | 0%     |
| BT               | compute_rhs#0-#10| 7                        | 21.343                | 20.345            | 5%     |
| BT               | error_norm#1     | 1                        | 0.019                 | 0.019             | 0%     |
| BT               | rhs_norm#1       | 1                        | 0.003                 | 0.003             | 0%     |
| BT               | program          | 17                       | 117                   | 116               | 1%     |
| SP               | initialize#0-#7  | 6                        | 0.043                 | 0.043             | 0%     |
| SP               | exact_rhs#0-#4   | 2                        | 0.133                 | 0.132             | 1%     |
| SP               | compute_rhs#0-#10| 7                        | 21.452                | 20.050            | 7%     |
| SP               | error_norm#1     | 1                        | 0.012                 | 0.011             | 9%     |
| SP               | rhs_norm#1       | 1                        | 0.002                 | 0.002             | 0%     |
| SP               | program          | 17                       | 111.5                 | 110.5             | 1%     |

#### 4.9 Conditional Parallelization

**The Pattern** A technique present in auto-parallelized codes, but not in the manual variants, is the conditional parallelization of loops. The Cetus compiler estimates the workload of loops, as the product of the number of statements and iterations. It parallelizes only those with high workloads. If the estimate is an expression that cannot be computed at compile time, it uses OpenMP’s conditional parallelization clause with an if condition that the expression exceeds a threshold. The manually parallelized programs do not use such conditional parallelization. One can expect that conditional parallelization benefits programs with small data sets, as some of the loops will not beneficially run in parallel.

**Performance Impact** We have found some conditionally parallelized loops that are too small to run in parallel beneficially. But their impact on the overall programs was very small, even when they were executed in parallel, as these loops do not take significant execution time. We have also found some loops that Cetus did not parallelize since they were not profitable. While conditional parallelization adds a small runtime overhead, due to the if clause added to the OpenMP directive that checks for exceeding a threshold, the technique is generally beneficial.

To estimate the overhead conditional parallelization may add to the execution time of the loop, we measured the execution time of the rhs_norm#1 loop of the BT application with and without conditional parallelization in the Cetus-parallelized code. The results of this measurement are presented in Table 14.
Table 14: Impact of conditional analysis; A comparison is made between the execution time of the code with and without conditional analysis in Cetus-parallelized code.

| Application Name | Loop Name          | Technique Applied | Technique Disabled | Impact |
|------------------|--------------------|-------------------|--------------------|--------|
| BT               | rhs_norm#1         | 0.004             | 0.003              | 33%    |

**Opportunities for Compilers** Like many other optimizers, Cetus uses a crude profitability model. There is much room for improving these models to estimate the execution time of loops or program sections under various optimization variants.

### 4.10 Code Modifications in Hand-parallelized Codes

**The Pattern** Our comparison of hand-parallelized and auto-parallelized versions of the codes revealed additional modifications that were made to the hand-parallelized codes. They include:

- Enclosing a mix of parallel loops and serial sections in a parallel region. An example of this is in the CG application, loops conj_grad#0-#4.
- Changing the scope of variables to enable the creation of parallel regions. An example of this is in the CG application, conj_grad() subroutine.
- Explicitly mapping tasks or iterations to threads. An example is the create_seq#0 loop in the IS application.
- Resolving some dependences (mostly output dependences) to enable parallelization. An example is the IS application’s full_verify#0 loop.
- Improving cache performance. An example is the rank() subroutine in the IS application.
- Merging loops that perform similar tasks. An example is the MG application’s comm3#0 loop.

**Performance Impact** These modifications were often applied to enable later parallelization steps. Their impact was thus difficult to isolate. In general, they contributed significantly to the good performance of the parallel applications.

**Opportunities for Compilers** While, at a high level, the mentioned modifications seem automatic, they tend to make use of application-specific knowledge. They are thus non-trivial to implement with general benefit.

### 5 Related Work

Many studies have been conducted on the NAS Parallel Benchmarks, including analyses, evaluation, parallelization, and tuning, but no comparison has been made between automatically and manually parallelized codes. Some studies do propose improvements to auto-parallelizers, based upon limitations of such tools that they have encountered in their experiments. The following are studies in this regard.

A study by Prema et al. [15] comparing different auto-parallelizers such as Cetus, Par4all [1], Pluto [7], Parallware [10], ROSE [17], and Intel C++ Compiler (ICC) [19] while parallelizing NAS Parallel Benchmarks (NPB) finds that auto-parallelizers have limitations, which programmers should
be aware of in order to intervene manually if necessary during parallelization. The development of an interactive environment that highlights the difficulties encountered while parallelizing loops is proposed.

Blume [6] and Eigenmann et al. [9] discuss the successes and limitations of auto-parallelizers, based on a study performed on the Perfect Benchmarks. A modified version of the KAP restructurer and the VAST restructurer were used as representatives of parallelizing compilers for Fortran programs. Based on the limitations of auto-parallelizers at that time, this study proposes new techniques.

Dave et al. [8] have measured the serial performance as well as the performance of the manually parallelized codes on a subset of the NAS Parallel and SPEC OMP2001 benchmarks. In contrast to the present paper, their experiment compared the performance of these programs with that of auto-tuned codes.

A distinguishing feature of the present paper is that it compares auto-parallelized with hand-parallelized codes in order to identify opportunities for compiler improvements. Performance differences attributable to the identified program patterns are also measured, so as to quantify their importance for future compiler developments. Our proposed improvements could help auto-parallelizers reach performance approaching that of hand-parallelized code.

6 Conclusion

We compared how expert programmers parallelize programs with how automatic parallelization does the same. The goal is to learn how to improve auto-parallelizers so as to approach hand-optimized performance. We believe that such studies are essential to push the forefront of research in compilers for parallel computing.

Currently, auto-parallelized codes are not as efficient as hand-parallelized codes. Our analysis of a subset of the NAS Parallel benchmarks found that auto-parallelized codes perform better than serial codes in many programs, but hand-parallelized codes perform significantly better. We have identified code sections, their program patterns, and the performance where differences occur. Additionally, we found examples in which hand-parallelized codes performed better after the use of threadprivate data was undone.

Among the patterns that showed the biggest performance differences were: Parallelizing the outermost loop in nested loops, parallelizing loops that enclose function calls, parallelizing loops with irregular patterns, enclosing loops in parallel regions, applying dynamic scheduling to cases with imbalanced loads, and using NOWAIT clauses to eliminate implicit barriers.

Opportunities for advancing compilers exist in several areas, including in advancing analysis techniques, improving transforming techniques, and efficient OpenMP code generation. These opportunities are explained along with the differentiating patterns that have been identified. The findings of this study will be used to guide future developments of the Cetus parallelizing compiler platform and the interactive Cetus parallelizer (iCetus) [2].

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