NeuralTree: A 256-Channel 0.227µJ/class Versatile Neural Activity Classification and Closed-Loop Neuromodulation SoC

Uisub Shin, Student Member, IEEE, Cong Ding, Student Member, IEEE, Bingzhao Zhu, Student Member, IEEE, Yashwanth Vyza, Alix Trouillet, Emilie C. M. Revol, Student Member, IEEE, Stéphanie P. Lacour, Member, IEEE, and Mahsa Shoaran, Member, IEEE

Abstract—Closed-loop neural interfaces with on-chip machine learning can detect and suppress disease symptoms in neurological disorders or restore lost functions in paralyzed patients. While high-density neural recording can provide rich neural activity information for accurate disease-state detection, existing systems have low channel count and poor scalability, which could limit their therapeutic efficacy. This work presents a highly scalable and versatile closed-loop neural interface SoC that can overcome these limitations. A 256-channel time-division multiplexed (TDM) front-end with a two-step fast-settling mixed-signal DC servo loop (DSL) is proposed to record high-spatial-resolution neural activity and perform channel-selective brain-state inference. A tree-structured neural network (NeuralTree) classification processor extracts a rich set of neural biomarkers in a patient- and disease-specific manner. Trained with an energy-aware learning algorithm, the NeuralTree classifier detects the symptoms of underlying disorders (e.g., epilepsy and movement disorders) at an optimal energy-accuracy trade-off. A 16-channel high-voltage (HV) compliant neurostimulator closes the therapeutic loop by delivering charge-balanced biphasic current pulses to the brain. The proposed SoC was fabricated in 65nm CMOS and achieved a 0.227µJ/class energy efficiency in a compact area of 0.014mm$^2$/channel. The SoC was extensively verified on human electroencephalography (EEG) and intracranial EEG (iEEG) epilepsy datasets, obtaining 95.6%/94% sensitivity and 96.8%/96.9% specificity, respectively. \textit{In-vivo} neural recordings using soft µECG arrays and multi-domain biomarker extraction were further performed on a rat model of epilepsy. In addition, for the first time in literature, on-chip classification of rest-state tremor in Parkinson’s disease from human local field potentials (LFPs) was demonstrated.

Index Terms—machine learning, neural network, decision tree, closed-loop neuromodulation, epilepsy, Parkinson’s disease, energy-efficient classification, seizure, tremor

I. INTRODUCTION

NEUROLOGICAL disorders are the second leading cause of global deaths and the leading cause of disability worldwide [1]. Epilepsy (>60M) and Parkinson’s disease (>10M) are among common examples, and many patients are living with medication-refractory symptoms of these disorders. Closed-loop brain stimulation has emerged as a promising therapeutic solution to treating such disorders [2]–[6], and a number of FDA-approved and research-based devices are currently available, including NeuroPace’s responsive neurostimulation [7] and Medtronic’s Percept deep-brain stimulation (DBS) [8] systems. However, these devices have a low channel count (4–6) and rely on simplistic symptom detection algorithms (e.g., feature thresholding), which could result in suboptimal detection accuracy and limited therapeutic efficacy.

Over the past decade, we have witnessed a growing adoption of machine learning (ML) for symptom prediction in a variety of neurological conditions such as epilepsy [9], Parkinson’s disease (PD) [10], depression [11], and memory disorders [12]. Through neural signal acquisition, biomarker extraction, and ML-based classification, pathological disease states can be detected more accurately and suppressed more effectively than conventional methods. Moreover, ML intelligence can improve the accuracy of motor intention decoding in brain-machine interfaces (BMIs) for rehabilitation of motor impairments [13], [14]. Despite recent innovations, existing ML-embedded SoCs [5], [15]–[22] are limited in the following aspects:

1) Low channel count: As the analog front-end (AFE) often dominates the overall area of a neural interface system, the channel count of existing ML-SoCs is limited to 8–32, which may not be sufficient to collect clinically meaningful information for accurate disease state prediction.

2) Low hardware efficiency: Despite low channel count, the area and energy consumption of the existing SoCs are prohibitive, making it difficult to scale up the number of channels. This is mainly due to their hardware complexity that grows proportional to the number of channels and biomarkers.

3) Limited application: With limited sets of biomarkers and conventional classifiers, most neural interface SoCs reported so far have targeted a single task, epileptic seizure detection, while there exist many other conditions that could benefit from the closed-loop neural interface technology.

Closed-loop SoCs would advance further with a higher number of channels and greater adaptability to various neural classification tasks. In epileptic seizure detection, for instance, covering a larger brain area with a high-spatial-resolution electrocorticography (ECoG) array will enable more precise localization of epileptic foci and better mapping of seizure onset [23], thus enhancing the seizure detection accuracy of...
the trained classifier. In treating movement disorders such as PD and essential tremor, high-density DBS can engage target brain regions more effectively while reducing stimulation-induced side effects [24]. Furthermore, high channel count can enhance the accuracy of motor intention decoding in prosthetic BMIs by collecting higher-resolution motor and sensory information [25]. Fig. 1 presents the envisioned versatile neural interface platform that integrates a large number of channels. A patient- and disease-specific classifier detects the pathological symptoms of brain disorders and activates a neurostimulator to provide cortical or deep-brain stimulation for symptom suppression. In BMIs, motor intention can be decoded to control prosthetic devices and provide sensory feedback to the brain via electrical stimulation. This high-density, versatile neural interface device could advance our understanding of complex brain dynamics and provide new therapeutic opportunities for people suffering from various neurological/psychiatric disorders and motor conditions. A miniaturized, energy-efficient implementation of such devices is a key to enabling next-generation closed-loop neural SoCs.

To overcome the aforementioned limitations of existing systems and transition towards the next-generation closed-loop neural interface, this paper presents a 256-channel highly scalable, energy-efficient neural activity classification and closed-loop neuromodulation SoC. Four 64-channel chopper-stabilized time-division multiplexed (CS-TDM) AFE modules perform high-density multi-site neural recording to train the classifier. A 16 × 16 switch matrix and row-multiplexing chopper (MUX-CHOP) connect the 256-channel neural inputs to the AFE modules for signal conditioning. In inference mode, the MUX-CHOP is configured such that any subset of 64 input channels can be selected and processed by the main AFE module. The input selection can change dynamically on a window-by-window basis according to the trained input sequence, to perform channel-selective inference. Following signal conditioning by the main AFE module, a finite impulse response (FIR) filter and feature extraction engine (FEE) compute neural biomarkers in temporal, spectral, and phase domains. Up to 64 multi-symptom biomarkers are extracted on demand in a patient- and disease-specific manner. The extracted biomarkers are passed to the NeuralTree classifier for neural activity classification. The flexible NeuralTree model supports both binary and multi-class classification. Upon detection of pathological brain states, a 16-channel HV compliant neurostimulator delivers charge-balanced biphasic current pulses to the brain to close the therapeutic loop.

This paper extends upon our prior work in [26] and presents a review of the state-of-the-art, detailed description of the proposed circuits/algorithms, and more extensive benchtop and in-vivo validation of the SoC. The paper is organized as follows. Section II provides a high-level description of the 256-channel SoC. Section III describes the system-level optimization of the AFE and introduces a 256-channel time-division multiplexed (TDM) architecture with a two-step fast-settling mixed-signal DC servo loop (DSL). Sections IV and V detail the NeuralTree classification processor and the 16-channel high-voltage (HV) compliant neurostimulator, respectively. Benchtop and in-vivo measurement results are demonstrated in Section VI. Finally, Section VII concludes the paper.

II. SoC ARCHITECTURE

Fig. 2 presents the architecture of the proposed 256-channel neural activity classification and closed-loop neuromodulation SoC. Four 64-channel chopper-stabilized time-division multiplexed (CS-TDM) AFE modules perform high-density multi-site neural recording to train the classifier. A 16 × 16 switch matrix and row-multiplexing chopper (MUX-CHOP) connect the 256-channel neural inputs to the AFE modules for signal conditioning. In inference mode, the MUX-CHOP is configured such that any subset of 64 input channels can be selected and processed by the main AFE module. The input selection can change dynamically on a window-by-window basis according to the trained input sequence, to perform channel-selective inference. Following signal conditioning by the main AFE module, a finite impulse response (FIR) filter and feature extraction engine (FEE) compute neural biomarkers in temporal, spectral, and phase domains. Up to 64 multi-symptom biomarkers are extracted on demand in a patient- and disease-specific manner. The extracted biomarkers are passed to the NeuralTree classifier for neural activity classification. The flexible NeuralTree model supports both binary and multi-class classification. Upon detection of pathological brain states, a 16-channel HV compliant neurostimulator delivers charge-balanced biphasic current pulses to the brain to close the therapeutic loop.

The all-in-one integration of high-density recording and stimulation channels, multi-symptom neural biomarkers, and ML intelligence can easily grow the hardware complexity of the system. To overcome this challenge, the proposed SoC employs various circuit-algorithm innovations and system-level...
hardware optimization techniques, which will be discussed in the remainder of this paper.

III. 256-CHANNEL ANALOG FRONT-END

As the sensor count increases, the area constraint on the AFE becomes more stringent and the complexity of the back-end signal processing also grows significantly. We tackle these challenges with an area-efficient TDM AFE with a channel-selective inference scheme. Noting that only subsets of input electrodes capture disease-relevant neural activity, the channel-selective approach can greatly reduce the hardware overhead during inference. To validate this concept, we trained a classifier on 128-channel intracranial electroencephalography (iEEG) recorded from an epilepsy patient [27] to assess the discriminative power of each channel. The NeuralTree classifier (detailed in Section. IV-C) was trained using two common types of seizure biomarkers (line-length and multiband spectral energy) extracted from the 128 channels. The importance of each channel was then assessed based on the number of features extracted during inference using 5-fold cross-validation. The non-uniform channel importance in Fig. 3 implies that high-density training followed by channel-selective inference can save the inference cost significantly while maintaining the classification accuracy.

Fig. 4 depicts the AFE configurations during classifier training and inference modes. In training mode, the four 64-channel CS-TDM AFE modules acquire 256-channel neural signals to exploit high-resolution brain activity information. The digitized 256-channel neural data are then used for offline classifier training, during which informative channel indices and feature types are identified. After loading the trained parameters to an on-chip memory, the MUX-CHOP is configured to select any subset of up to 64 informative channels and connect them to the main AFE module via a shared input path. Here, the three auxiliary AFE modules are disabled to save system power. In the proposed NeuralTree model, the selected channels can change dynamically in each feature computation window to perform on-demand biomarker extraction, thus reducing the number of extracted features and enabling energy-efficient classification. However, the dynamic channel selection approach raises new concerns on electrode DC offset (EDO) cancellation that must be addressed.

A. Challenges of Electrode DC Offset Cancellation

Electrochemical polarization at the electrode-tissue interface develops DC offsets between electrodes [28], the magnitude of which can be as large as ±50mV [29]. Each recording electrode in an array can develop a unique EDO with respect to a common reference electrode. When many electrodes with different EDOs are multiplexed to a single amplifier, these EDOs appear as a large signal that fluctuates at the multiplexing frequency, as shown in Fig. 5. Digitizing small neural signals (∼1µ–1mV) and significantly larger EDOs simultaneously would require a high-resolution (∼16 bits) analog-to-digital converter (ADC), which is nontrivial to design in a compact and power-efficient way. A high-resolution ADC would also increase the hardware complexity of the subsequent filtering and signal processing in the digital back-end (DBE). Another challenge imposed by the channel-selective inference scheme is that the EDO pattern at the amplifier input changes abruptly between successive channels and feature extraction windows.
Fig. 6. Modular architecture of the proposed 256-channel CS-TDM AFE with a two-step fast-settling mixed-signal DSL. In training mode, each AFE module sequentially conditions 64 input channels. In inference mode, the four MUX-CHOPs select up to 64 channels out of 256 and route them to the main AFE module via a shared input path drawn in red.

significant loss of neural activity information.

The 16-channel SoC in [5] multiplexed a low-noise amplifier (LNA) for every two channels to save chip area. Intermediate node voltages were stored on 1.5pF sampling capacitors for fast switching between channels with different EDOs. However, this analog S/H-based approach is area inefficient (\(\sim 0.49\)mm\(^2\)/channel) and thus, it is not a viable option for a high-channel-count system. A mixed-signal coarse-fine DSL was reported in [29]. The coarse loop canceled large EDOs using binary search, while the fine loop suppressed residual offsets. Despite achieving a small area of 0.013mm\(^2\)/channel, the ADC-assisted binary search loop requires many samples to converge, making it inadequate for fast settling in the presence of abrupt EDO changes. Recently, hardware sharing via time-division multiplexing has been increasingly adopted to improve the area efficiency of high-channel-count AFEs. Specifically, to cancel EDOs between successive channels, several DSL designs have been reported, including binary search [50], delta encoding [51], and least-mean-square filtering [52]. While these AFEs can ultimately settle for a fixed input EDO pattern, none are compatible with channel-selective feature extraction scheme as the offset cancellation loops must re-settle in each window when a new set of inputs (with unknown EDO patterns) is fed to the AFE.

B. Two-Step Fast-Settling Mixed-Signal DC Servo Loop

To enable an area-efficient AFE implementation and address the EDO cancellation challenge, a 256-channel CS-TDM AFE with a two-step fast-settling mixed-signal DSL is proposed, as shown in Fig. 6. The timing diagram of the two-step EDO cancellation process during inference is illustrated in Fig. 7. At the beginning of each feature extraction window, coarse offset cancellation using binary search is performed for 64 selected channels. A dynamic comparator detects the polarity of the LNA output, and a successive approximation register (SAR) logic subsequently updates the input code for a 9-bit capacitive digital-to-analog converter (CDAC). This process is repeated 9 times until the LNA output converges, and the EDO (\(\leq \pm 50\)mV) is digitized at 9-bit resolution. The 9-bit EDO code is then stored into a register. This 64-channel coarse EDO cancellation is performed only during the first sampling period (7.8\(\mu\)s/channel) of each window to enable fast settling and minimize neural data loss. Next, a fine loop is enabled to record neural signals and cancel any residual EDOs following coarse offset cancellation (\(< \pm 0.2\)mV). A low-pass filtering digital integrator extracts undesired low-frequency signal components including residual EDOs from the ADC output. The pre-stored 9-bit EDO is added to the 9 most significant bits of the 19-bit integrator output. This newly formed 19-bit code is then \(\Delta \Sigma\)-modulated and fed back to the amplifier input via the 9-bit segmented (6-bit unary+3-
increases the effective number of bits of the 9-bit CDAC to bit binary) CDAC. Here, an oversampling ratio (OSR) of 50 increases the effective number of bits of the 9-bit CDAC to ~17 bits to suppress the DAC quantization noise <1µV [33]. The output of the digital integrator can be bit-shifted to control the feedback gain for loop stability and adjust the highpass pole location in the closed-loop frequency response.

C. Low-Noise Amplifier and Anti-Aliasing Integrator

The feedforward path of the AFE consists of a chopper-stabilized LNA and Gm-C integrator. The LNA is capacitively coupled to provide a precise, moderate closed-loop gain of 26dB (CINFB/Gm). The positive feedback loop (CREF) partially compensates for input impedance degradation due to chopping. The core amplifier in the LNA stage adopts an inverter-based current-reuse topology for improved noise efficiency [34] as shown in Fig. 8(a). The complementary input pairs are biased in weak inversion (gDS/Ip ≈ 25) and constructed using thick-oxide transistors to prevent gate leakage. The cascode transistors boost the open-loop gain to enable a precise closed-loop gain. They further mitigate the Miller effect of the input-pair gate-drain capacitance to prevent signal attenuation.

With a ∆Σ frequency of 6.4MHz, the LNA bandwidth is set to 7MHz, which is much higher than the ADC sampling rate of 128kS/s. This high LNA bandwidth necessitates an anti-aliasing filter prior to digitization to avoid noise folding. Filtering is achieved by a charge-sampling Gm-C integrator, providing a sinc-shape frequency response with notches at integer multiples of the sampling frequency [35, 36]. Fig. 8(b) presents the circuit implementation of the Gm-C integrator and the timing diagram of operation. A folded-cascode amplifier with source degeneration is implemented for improved linearity. The integration time extends to the 96% of the sampling period, during which high-frequency ∆Σ noise and chopper ripples are attenuated. The charge sampling approach relaxes the settling requirement of the amplifier [35], obviating the need for a power-consuming ADC buffer. The 3-bit resistor (Rb) and 5-bit capacitor (CINT) banks provide an additional programmable gain (14–34dB) in the feedforward path.

In a TDM front-end, samples of the current channel can be corrupted by previous channel residues, which manifests as inter-channel crosstalk. To prevent this, our CS-TDM AFE periodically resets the intermediate nodes along the feedforward path between successive channels. The kT/C noise resulting from the reset operation is up-modulated by the chopper and subsequently filtered out by the anti-aliasing Gm-C integrator.

D. Asynchronous Analog-to-Digital Converter

A 10-bit SAR ADC digitizes the Gm-C integrator output at 128kS/s (64 channels). Following charge sampling in the Gm-C integrator, only a short time (312.5ns) is allocated to digitization. To avoid the use of an excessively high clock, we adopt an asynchronous SAR control with a single, master sampling clock [37]. A 9-bit binary-weighted charge-redistribution DAC with top-plate sampling and monotonic-switching is implemented, using 2.3fF metal-oxide-metal unit capacitors and bootstrapped switches [37]. An attenuation capacitor equal to the total 9-bit DAC capacitance is added to halve the effective input range of the ADC without an additional reference voltage generator [38]. This approach relaxes the linearity and gain requirements of the preceding amplifiers with only a marginal area overhead, which is amortized across 64 channels in the proposed TDM AFE.

IV. NeuralTree Classification Processor

The high-level architecture of the proposed NeuralTree classification processor is presented in Fig. 2. The configurable TDM FIR filter performs selective bandpass filtering (BPF) and Hilbert transformation (HT) depending on the type of feature being extracted. Following signal filtering, the multi-symptom TDM FEE extracts up to 64 patient- and disease-specific neural biomarkers in temporal, spectral, and/or phase domains. The NeuralTree classifier uses the extracted feature vectors to perform top-down brain-state inference along the most probable path of the tree. The end-to-end TDM implementation enables a seamless integration of key building blocks without the need for demultiplexing, thus achieving a new class of scalability and energy efficiency. Hardware-friendly feature approximations and energy-aware training algorithm further improve the NeuralTree’s hardware efficiency, as detailed in this section.

A. Bandpass Filtering and Hilbert Transform

Fig. 9 depicts the block diagram of the TDM FIR filter that processes digitized neural signals. To save silicon area, a single
Fig. 9. Configurable TDM FIR filter and multi-symptom TDM FEE.

Fig. 10. Hardware implementations of the TDM FEE: (a) temporal and spectral feature extractor, and (b) phase feature extractor.

set of arithmetic units is shared between 64 channels for 32-tap bandpass filtering [5]. Band-specific FIR coefficients are retrieved from the on-chip memory and multiplexed into the multiplier array. The FIR filter can be reconfigured as a 31-tap Hilbert transformer to obtain analytic signals for instantaneous phase and amplitude extraction. The 64-channel BPF and HT register banks are clocked at 128kHz and selectively clock-gated depending on the feature type. For temporal feature extraction, the ADC output is directly fed to the FEE and the FIR is bypassed.

B. Multi-Symptom Feature Extraction

To enhance the versatility of the SoC for a broad range of neural classification tasks, the FEE integrates multi-symptom neural biomarkers, as summarized in Table I. Without careful design considerations, integrating such a broad range of biomarkers can be hardware intensive. The following subsections describe hardware-friendly feature approximation algorithms and circuit techniques that enable low-complexity, yet accurate feature extraction in the proposed SoC.

1) Temporal features: Line-length (LL) increases in the presence of high-amplitude or high-frequency neural oscillations and has been among powerful biomarkers of epileptic seizures [39]. LL is defined as in [40]:

$$LL = \frac{1}{N} \sum_{t=1}^{N} |x_t - x_{t-1}|$$

where N is the number of samples in a feature extraction window. Fig. 10(a) presents the hardware implementation of the proposed TDM temporal feature extractor. For LL extraction, the absolute differences between successive samples are accumulated with two adders and one absolute value calculator.

The Hjorth statistical parameters are highly correlated with tremor in Parkinson’s disease [10] and used in BMIs for finger movement [40] and gait [41] decoding. The Hjorth activity (ACT), mobility (MOB), and complexity (COM) measure the variance, mean frequency, and frequency change of a signal, respectively, as defined below [42]:

$$ACT = \frac{1}{N} \sum_{t=1}^{N} (x_t - \mu)^2$$

$$MOB = \sqrt{\frac{\text{var}(\Delta x)}{\text{var}(x)}}$$

$$COM = \sqrt{\frac{\text{var}(x) \cdot \text{var}(\Delta^2 x)}{\text{var}(\Delta x)^2}}$$

where $\mu$, $\Delta x$, and $\Delta^2 x$ are the mean, first, and second derivatives of the signal $x$, respectively.

The three Hjorth parameters are difficult to efficiently compute in their original form, due to the intensive multiplication and square root operations. Ref. [43] introduced a similar set of parameters, namely mean amplitude, mean frequency, and spectral purity index (SPI), in which the root of square operator is replaced by simple absolute value approximation.

---

TABLE I

| TASK-SPECIFIC NEURAL BIOMARKERS INTEGRATED ON THE SoC |
|-------------------------------------------------------|
| **Epileptic Seizure** | **Description** |
| Line-Length | Average of absolute temporal derivative |
| Hjorth Activity | Variance of signal |
| Delta Energy | Spectral energy in 1–4 Hz |
| Theta Energy | Spectral energy in 4–8 Hz |
| Alpha Energy | Spectral energy in 8–13 Hz |
| Beta Energy | Spectral energy in 13–30 Hz |
| Low-Gamma Energy | Spectral energy in 30–50 Hz |
| Gamma Energy | Spectral energy in 50–80 Hz |
| High-Gamma Energy | Spectral energy in 80–150 Hz |
| Ripple Energy | Spectral energy in 150–250Hz |
| Phase-Amplitude Coupling | Coupling of the phase in 4–8 Hz to the amplitude envelope in 80–150 Hz |
| Phase Locking Value | Synchronization between two-channel phases in 13–30 Hz |

| Parkinson’s Tremor | **Description** |
| Hjorth Activity | Variance of signal |
| Hjorth Mobility | Mean frequency of signal |
| Hjorth Complexity | Change in signal frequency |
| Tremor Energy | Spectral energy in 1–4 Hz |
| Beta Energy | Spectral energy in 13–30 Hz |
| Low-Gamma Energy | Spectral energy in 30–45 Hz |
| Gamma Energy | Spectral energy in 60–90 Hz |
| High-Gamma Energy | Spectral energy in 100–200Hz |
| Slow High-Frequency Oscillation | Spectral energy in 200–300Hz |
| Fast High-Frequency Oscillation | Spectral energy in 300–400Hz |
| High-Frequency Oscillation Ratio | Ratio of the energy in 200–300 Hz to the energy in 300–400 Hz |
| Phase-Amplitude Coupling | Coupling of the phase in 13–30 Hz to the amplitude envelope in 150–400 Hz |

| Finger Movement | **Description** |
| Local Motor Potential | Mean value of signal |
| Hjorth Activity | Variance of signal |
| Hjorth Mobility | Mean frequency of signal |
| Hjorth Complexity | Change in signal frequency |
| Alpha Energy | Spectral energy in 8–13 Hz |
| Beta Energy | Spectral energy in 13–30 Hz |
| Low-Gamma Energy | Spectral energy in 30–60 Hz |
| Gamma Energy | Spectral energy in 60–100 Hz |
| High-Gamma Energy | Spectral energy in 100–200Hz |
These new parameters are less intensive to compute while preserving a close relation to the measures of EEG amplitude and frequency. We adopt this approach to approximate the Hjorth features as in (5)–(7), with a modification to the SPI parameter by taking its reciprocal, since it is better correlated with the original Hjorth complexity parameter:

\[
\text{ACT} \approx 1 \frac{1}{N} \sum_{t=1}^{N} |x_t| \quad (5)
\]

\[
\text{MOB} \approx \frac{\sum_{t=1}^{N} |\Delta x_t|}{\sum_{t=1}^{N} |x_t|} \quad (6)
\]

\[
\text{COM} \approx (\frac{\sum_{t=1}^{N} |x_t|}{\sum_{t=1}^{N} |\Delta x_t|}) \cdot \left(\frac{\sum_{t=1}^{N} |\Delta^2 x_t|}{\sum_{t=1}^{N} |\Delta x_t|^2}\right) \quad (7)
\]

To calculate the approximated Hjorth features, the absolute values of the input and its first and second derivatives are accumulated selectively, as shown in Fig. 10(a). For MOB and COM extraction, the subsequent multipliers and ratio calculator further process the accumulated derivatives to compute features in fractional form. The ratio calculator employs a reciprocal-multiply approach with bit shifting instead of a complex divider, as depicted in Fig. 10(a).

Local motor potential (LMP) has been used as a low-complexity yet effective marker for motor intention decoding in BMIs \([14, 46]\). The LMP feature quantifies the mean value of a signal as defined in (8):

\[
\text{LMP} = \frac{1}{N} \sum_{t=1}^{N} x_t \quad (8)
\]

The accumulation function can be performed by reusing the ACT extractor and bypassing the absolute value calculator, as shown in Fig. 10(a).

2) Spectral features: Spectral energy (SE) in multiple frequency bands of neural oscillations has been a commonly used biomarker in epilepsy \([5, 16, 17, 19, 21, 22, 40]\), Parkinson’s disease \([10, 45]\), and BMIs \([14, 46]\). As a measure of signal power integrated over time, the SE can be defined in the discrete-time domain, as follows:

\[
\text{SE} = \frac{1}{N} \sum_{t=1}^{N} x_{\text{BAND},t}^2 \quad (9)
\]

where \(x_{\text{BAND},t}\) indicates the bandpass-filtered neural signal.

A common approximation method to avoid the square operation is to take the absolute output of the bandpass filter. The 16-channel EEG processor in [5] demultiplexed the output of the TDM FIR filter to 112 signal paths (16 channels×7 bands) to calculate 112 SE features in parallel. This approach requires an equal number of multi-bit adders and absolute value calculators with significant area overhead. To save chip area, the TDM spectral feature extractor in Fig. 10(a) directly receives the BPF output as the input without demultiplexing, and extracts up to 64 SE features using a single adder. The area efficiency is further improved by reusing the hardware already implemented for ACT and LMP extraction.

High-frequency (>200Hz) oscillations (HFOs) are prominent features in Parkinson’s disease \([47]\) and epilepsy (>80Hz) \([48]\). For instance, \([49]\) reported the energy ratio between the slow (HFO\(_1\), 200–300Hz) and fast HFO (HFO\(_2\), 300–400Hz) as an indicator of rest tremor in PD:

\[
\text{HFO}_R = \frac{\sum_{t=1}^{N} x_{\text{HFO}_1,t}^2}{\sum_{t=1}^{N} x_{\text{HFO}_2,t}^2} \quad (10)
\]

The SE extractor is reused to calculate the slow and fast HFOs, while the ratio between the two is computed using the ratio calculator shared with the Hjorth feature extractor.

3) Phase features: Different brain regions communicate with each other through neuronal oscillations. Abnormal cross-regional synchronization of neural oscillations can indicate disease-related pathological states in neurological and psychiatric disorders. In epilepsy, spatial and temporal changes in cross-channel phase synchronization, quantified by phase locking value (PLV), play as a key indicator of seizure state \([50]\). Phase-amplitude coupling (PAC) is another mechanism for within- and cross-regional brain communication. PAC quantifies the degree to which the low-frequency neural oscillatory phase modulates the amplitude of high-frequency oscillations \([51]\). Excessive PAC has been observed in disorders such as epilepsy \([52]\), Parkinson’s \([53]\), and depression \([54]\).

Measuring PLV and PAC requires Hilbert transformation to obtain analytic signals followed by several complex computations such as extraction of instantaneous phase and amplitude, trigonometric functions, and magnitude computation, as shown in (11) and (12):

\[
\text{PLV} = \frac{1}{N} \left(\sum_{t=1}^{N} \sin \Delta \theta_t\right)^2 + \left(\sum_{t=1}^{N} \cos \Delta \theta_t\right)^2 \quad (11)
\]

\[
\text{PAC} = \frac{1}{N} \left(\sum_{t=1}^{N} A_t \sin \theta_t\right)^2 + \left(\sum_{t=1}^{N} A_t \cos \theta_t\right)^2 \quad (12)
\]

where \(\Delta \theta_t\) in (11) is the cross-channel phase difference, and \(\theta_t\) and \(A_t\) in (12) are the modulating phase and modulated amplitude envelope, respectively.

The SoCs in \([17, 55]\) employed multiple COordinate Rotation Digital Computer (CORDIC) processors to compute these non-linear functions, consuming an excessive amount of power (>200\mu W). Alternatively, Fig. 10(b) depicts the proposed TDM phase feature extractor \([26]\). With band-specific analytic signals (Re and Im) as inputs, the instantaneous phase is approximated using a linear arctangent approximation (LAA) algorithm \([56]\) followed by look-up table (LUT)-based error correction \([57]\). The \(\ell_{\infty}\)-norm is used to approximate the amplitude envelope of high-frequency oscillations in PAC, as well as the magnitude computations in (1) and (2). The TDM phase feature extractor can compute up to 32 PLV/PAC features on demand in a compact area of 0.033mm\(^2\), performing a higher degree of multiplexing compared to the architecture in \([57]\).

To evaluate the accuracy of the proposed feature approximation algorithms, we analyzed the Pearson correlation coefficient between the ideal and approximated features in MATLAB. The phase and 8-band SE features were extracted from an epilepsy iEEG dataset \([27]\), while a PD local field potential (LFP) dataset \([10]\) was used to compute the HFO ratio.
A 41.2nJ/class DBE energy efficiency in 1mm
an ensemble of 8 eXtreme Gradient-Boosted (XGB) DTs. The 32-channel seizure detection classifier in [16] employed for their lightweight inference and low memory utilization. The demand for higher channel counts continues to grow. These constraints become more restrictive as the integrate ML models with high computational and memory constraints on implantable devices make it challenging to feature thresholding [58]. However, stringent area and power requirements. These constraints become more restrictive as the demand for higher channel counts continues to grow.

C. Energy-Aware, Low-Complexity NeuralTree Model

Deployment of ML algorithms in closed-loop neural interfaces can provide a more accurate and personalized treatment option compared to conventional approaches with manual feature thresholding [58]. However, stringent area and power constraints on implantable devices make it challenging to integrate ML models with high computational and memory requirements. These constraints become more restrictive as the demand for higher channel counts continues to grow.

Decision tree (DT)-based ML models are becoming popular for their lightweight inference and low memory utilization. The 32-channel seizure detection classifier in [16] employed an ensemble of 8 eXtreme Gradient-Boosted (XGB) DTs. A 41.2nJ/class DBE energy efficiency in 1mm$^2$ area was achieved, thanks to the on-demand feature extraction and sequential node processing. The 8-channel seizure detection SoC with 1024 AdaBoosted trees in [16] reported low-complexity spectral feature extraction with bit-serial processing, and achieved a 36nJ/class DBE energy efficiency. However, a drawback of conventional DT-based classifiers is that the number of trees and signal processing units can significantly increase as the classification task becomes more complex.

To enhance the hardware efficiency of the on-chip classifier, we propose a hierarchical NeuralTree model. Fig. 12(a) illustrates a graphical representation of the NeuralTree classifier trained with a probabilistic routing scheme [40]. Unlike conventional axis-aligned binary decision trees, the NeuralTree is a single oblique tree with probabilistic splits. With internal nodes represented by two-layer neural networks, the probability of splits in each internal node is computed using the sigmoid function. The feature vector $x_i$ is routed to each leaf node $l$ with a probability $p(l|x_i; \theta)$, where $\theta$ indicates the internal node parameters. The leaf nodes are parameterized by the class probability $\phi$. The probability of $x_i$ belonging to class $y_i$ can be expressed as:

$$p(y_i|x_i; \omega) = \sum_{i=1}^{L} p(l|x_i; \theta)\phi_{i,y_i}$$

where $\omega = \theta \cup \phi$ indicates the trainable weights in the NeuralTree, and $L$ is the number of leaf nodes. In the training process, we simply minimize the cross-entropy loss on the training data:

$$\min_{\omega} \sum_{i=1}^{N} -\log p(y_i|x_i; \omega).$$

The probabilistic NeuralTree is compatible with gradient-based optimization, which allows hardware-efficient model compression techniques such as weight pruning and fixed-point quantization. To enable neural activity inference with optimal energy-accuracy trade-off, the NeuralTree employs energy-aware regularization [59]. Here, the power consumed for feature computation is added to the objective function as a regularization term in the training objective. Specifically, we define the energy-aware regularization term as:

$$\Psi_{energy} = \sum_{i=1}^{I} \sum_{j=1}^{D} p_i \sum_{j=1}^{D} \beta_j |\theta_{i,j}|$$

where $I$ and $D$ represent the number of internal nodes and feature types, respectively, and $\beta$ is the normalized power cost for each feature type estimated using Synopsys PrimeTime. We use $p_i$ to represent the probability of visiting the internal

Fig. 11. Boxplot of the Pearson correlation coefficients between the ideal and approximated features.

and Hjorth features. The boxplot of correlation coefficients in Fig. 11 shows that the approximated features are highly correlated with their ideal counterparts, exhibiting median correlations above 0.9.

Thanks to feature approximations and hardware sharing, the proposed multi-symptom FEE occupies a small silicon area of 0.12mm$^2$, even with the complex features integrated. Aggressive hardware sharing among different feature calculators is possible thanks to the on-demand TDM scheme, even with the complex features integrated.

Fig. 12. NeuralTree classifier: (a) probabilistic NeuralTree trained with energy-aware regularization and network pruning, and (b) the NeuralTree hardware implementation and system operation under the proposed single-path channel-selective inference scheme.
node $i$ and $\theta_{i,j}$ for the weight associated with feature $j$ at
node $i$. Combining (14) and (15), we derive an energy-aware
objective function, which seeks to minimize the classification
error as well as the energy consumption during inference:

$$\min_{\omega} \sum_{i=1}^{N} \text{log} p(y_i|x_i; \omega) + C \cdot \Psi_{\text{energy}}(x_i; \omega).$$  \hspace{1cm} (16)

We introduce a hyperparameter $C$ to control the energy-
accuracy trade-off and penalize power-demanding features. The
proposed NeuralTree is trained using TensorFlow \[60\] with Adam optimizer (learning rate: 0.001) \[61\]. Validated on
the iEEG epilepsy dataset \[27\], the energy-efficient regularization
saves 64% power in filtering and feature extraction during
inference, with only a marginal accuracy loss (<2%). Following
regularization, network pruning is performed to compress the
tree structure by reducing the number of extracted features
(maximum 64 per node). Thanks to network pruning and fixed-
point weight quantization (12 bits), the trained parameters of the
compressed NeuralTree require only 2.93kB of memory.

Through energy-efficient regularization and network pruning,
a set of features that lead to optimal energy-accuracy trade-off
is extracted in a patient- and disease-specific manner.

Considering that most samples are routed with high cer-
tainty during training, the inference can be performed through
top-down conditional computations, as depicted in Fig. 12(b).
By reusing a single multiply-and-accumulate (MAC) unit and a
comparator, the standalone NeuralTree occupies a significantly
smaller area compared to large tree ensembles. In addition
to conventional binary classification tasks (e.g., seizure or
tremor detection), the NeuralTree further supports multi-class
classification tasks such as finger movement detection. This
additional functionality is achieved with only a marginal
memory overhead to store multi-bit class labels in the decision
LUT. As a proof of concept, in a 6-class finger movement clas-
sification task on a human ECoG dataset \[62\], the simulated
NeuralTree decoded finger movements with 73.3% accuracy.

During inference, the NeuralTree performs sequential node
processing along the most probable path, thus reducing the
number of computed features and weighted summations. The
NeuralTree is clocked at 128kHz but only activated during
the last 64 clock cycles in each feature extraction window to
perform 64 feature-weight MAC operations. The lightweight
channel-selective inference coupled with energy-aware learn-
ing considerably enhances the model’s energy efficiency and
scalability.

V. HIGH-VOLTAGE COMPATIBLE NEUROSTIMULATOR

A single chip integration of neurostimulator with other
building blocks is desired to reduce the size of the implantable
device and interconnection complexity. However, depending
on the electrode impedance and stimulation amplitude, the
voltage compliance required at the electrode-tissue interface
can exceed the gate-oxide breakdown limits in standard CMOS
processes \[63\]. To facilitate a seamless integration of the
closed-loop neuromodulation system in a standard low-power
CMOS process, a 16-channel neurostimulator is implemented
with a stacked high-voltage compliant architecture.

Fig. 13(a) presents the 12-stage 4-phase charge pump (CP)
that generates an 8V supply for the current drivers. Each stage
in the 4-phase CP consists of four elements in parallel, thus
reducing output ripples by a factor of four without the need
for large output capacitors \[64\]. To minimize the reversion
loss in the CP, flying capacitors ($C_P$) are controlled by a non-
overlapping clock generator. The ring VCO generates a high-
frequency clock at 1GHz, which allows the use of small flying
capacitors (0.8pF) for improved area efficiency \[63\]. To further
save chip area, a single CP is shared among four stimulation
channels that are individually addressable. Fig. 13(b) shows the
architecture of the stacked H-bridge
output driver. A single current sink ($I_{DAC}$) is used in both
anodic and cathodic phases to reduce charge mismatch. To
ensure precise charge balancing (CB), an offset-regulation
active CB technique combined with passive discharging is
employed \[65\]. The residual voltage at the electrode is mon-
tored following biphasic stimulation. If the residual voltage
exceeds the safety level ($\pm V_{SAFE}$), the active CB is enabled
to provide an additional current such that the two stimula-
tion phases are balanced. Following active CB, any residual
charges on the two electrodes are discharged to the ground.
To provide sufficient flexibility for various applications, the
stimulation parameters such as current amplitude, pulse width,
and frequency are programmable. 
VI. MEASUREMENT RESULTS

The SoC was fabricated in a TSMC 65nm 1P9M low-power CMOS process with a chip dimension of 4mm \times 2mm. The chip micrograph is shown in Fig. 14. The 256-channel SoC only occupies an active area of 3.48 mm\(^2\) (0.014 mm\(^2\)/channel).

A. AFE Characterization

The 256-channel TDM AFE including the digital DSL occupies an area of 1.1 mm\(^2\) (0.004 mm\(^2\)/channel) and consumes 387 \(\mu\)W (1.51 \(\mu\)W/channel) in training mode. During channel-selective inference, the LNAs and DSLs in the three auxiliary AFE modules are disabled, reducing the AFE power to 182 \(\mu\)W. Fig. 15(a) shows the measured AFE gain that is programmable between 40.7 and 57.9 dB. The location of the high-pass pole can be adjusted by bit-shifting the output of the digital integrator, as demonstrated in Fig. 15(b). With a 2.5 mV\(_{PP}\), 40.039 Hz sine input, the full AFE signal chain including the ADC achieved a signal-to-noise and distortion ratio (SNDR) of 49 dB and a spurious-free dynamic range (SFDR) of 61.6 dB, measured with 2048-point FFT. The input-referred noise (IRN) performance is presented in Fig. 15(d). Without chopping, the measured IRN was 60.4 \(\mu\)V\(_{rms}\) in the 1–500 Hz band. The dominant noise source is the \(kT/C\) noise due to the reset operation for crosstalk reduction, which is in agreement with simulations. When chopping was enabled, the IRN reduced to 3.2 \(\mu\)V\(_{rms}\) with the \(kT/C\) and 1/f noise up-modulated by the chopper and filtered out by the \(G_m-C\) integrator, as discussed in Section III-C. With the fine DSL disabled, the IRN was measured at 1.5 \(\mu\)V\(_{rms}\). This indicates that when the fine DSL is active, \(\sim 2 \times\) noise folding occurs due to the LNA’s insufficient bandwidth with respect to the \(\Delta\Sigma\) frequency [33]. The noise performance could be improved by using a wider LNA bandwidth and lower OSR with a higher-order \(\Delta\Sigma\) modulator [32]. Fig. 15(e) demonstrates the fast-settling behavior of the proposed coarse-fine DSL in the presence of abrupt EDO changes over 1s windows, which enables channel-selective inference. With the DSL disabled, the AFE was completely saturated by the offsets. When only the fine DSL was activated, the AFE failed to capture a significant portion of signals during its settling, as other existing DSLs would behave. With a 128 kHz chopping frequency, the input impedance was measured to be 24.5 M\(\Omega\) at 100 Hz. The common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR) at 50 Hz were 70 dB and 71 dB, respectively. Crosstalk between channels was less than \(-79.8\) dB inter-module and \(-72.8\) dB intra-module.

B. Stimulator Characterization

The stimulator occupies a small area of 0.05 mm\(^2\)/channel, which is \(4 \times\) and \(7 \times\) more compact than the stacked architectures in [15] and [63], respectively. Figs. 16(a)–(c) present bipolar stimulation current outputs with different parameters, measured using a 6 k\(\Omega\) + 330 nF load. Each channel can generate moderate currents ranging from 65 \(\mu\)A to 600 \(\mu\)A with a 640 kHz input clock, the pulse width and frequency are programmable within 9.375 \(\mu\)s–203.125 \(\mu\)s and 9.6 Hz–65 kHz, re-
The stimulator output measured in vitro is presented in Fig. 16(d). Under the maximum load current condition, the charge mismatch between the anodic and cathodic phases was measured to be <0.1%.

C. In-vivo Measurements

The neural recording and biomarker extraction capabilities of the SoC were validated in vivo in the experimental setup shown in Fig. 17(a). The animal experiments were performed with the approval of all experimental and ethical protocols and regulations granted by the Veterinary Office of the Canton of Geneva, Switzerland, under License No. GE/33A (33223). All procedures were in accordance with the Regulations of the Animal Welfare Act (SR 455) and Animal Welfare Ordinance (SR 455.1). We implanted two 15-channel 200µm-diameter soft µECoG arrays, shown in Fig. 17(b), into the somatosensory cortex of a Lewis rat. The µECoG arrays were fabricated using an e-dura technology with gold thin films [66]. Pentylenetetrazol (20mg) was injected intraperitoneally to the anesthetized rat to induce seizures [67]. Figs. 17(c) and (d) present ECoG recordings and neural biomarkers during a normal and a seizure state, respectively. Prominent increases in temporal and spectral biomarkers at the seizure onset and strong cross-channel phase synchronization were observed during a seizure event in a short acute recording session. In future work, the real-time seizure detection capability of the SoC will be further validated in vivo with a collection of sufficient seizure activity and objective seizure annotation.

D. Epileptic Seizure Detection

The classification performance of the SoC was validated on the CHB-MIT EEG [68] and iEEG.org [27] datasets of epilepsy patients. We analyzed 983-hour EEG recordings of 24 patients and 596-hour iEEG recordings of 6 patients, which contain 176 and 49 annotated seizures, respectively. Blockwise data partitioning was used to avoid data leakage from training to inference [16]. We performed 5-fold cross-validation for most patients and adopted a leave-one-out approach for patients with fewer than 5 seizures. The number of correctly detected seizures was counted to assess the sensitivity, while the specificity was calculated based on the window-based true negative rate averaged over multiple runs.

In training mode, each patient’s multi-channel neural data (18–28 EEG and 47–108 iEEG channels) were fed to the AFE. The digitized AFE outputs were processed offline to extract features using a bit-accurate FEE model in MATLAB for training the classifier. The trained NeuralTree parameters were then stored to the on-chip memory for inference, and the NeuralTree performance on the test data was evaluated. The SoC achieved 95.6%/94% sensitivity and 96.8%/96.9% specificity on the EEG and iEEG datasets, respectively. The SoC’s seizure detection performance on an epileptic patient is demonstrated in Fig. 17(e).

E. Parkinsonian Tremor Detection

The SoC’s performance was further validated on a PD patient with rest-state tremor recruited by the University of Oxford [10]. A 4-channel DBS lead was implanted into the subthalamic nucleus to collect LFPs, while the acceleration of the contralateral limb was used to label the tremor. Window-based true positive and negative rates were used to assess the sensitivity and specificity, respectively, using a 5-fold cross-validation. The SoC achieved 82.6% sensitivity and 78.4% specificity. Fig. 17(f) presents an example of the SoC’s tremor detection performance, where tremor states with inconspicuous neural activity were successfully detected by the NeuralTree. To the best of our knowledge, this is the first demonstration of PD tremor detection with an on-chip classifier.

F. Comparison with the State-of-the-Art

Table. II compares the proposed SoC with the state-of-the-art seizure detection SoCs with on-chip ML. The 256-channel SoC achieves an 8× improvement in channel count, 9.3× in per-channel area, and 4.3× in system energy efficiency.
12

TABLE II

| Parameter | JSSC'15 [5] | JSSC'18 [15] | IEEE/TCAS’18 [16] | ISCC'18 [17] | ISCC'20 [18] | JSSC'20 [19] | THBioCAS’20 [20] | VLSIF'21 [21] | JSSC'22 [22] | This Work |
|-----------|-------------|-------------|------------------|--------------|--------------|-------------|------------------|-------------|-------------|-----------|
| Process (nm) | 180 | 180 | 65 | 130 | 65 | 40 | 180 | 28 | 40 | 65 |
| Supply Voltage (V) | 1.81 | 1.8 | 0.8 | 1.2 | 1.2 | 0.58 | 1.5 | 0.5 | 1.1 | 1.2 |
| # Recording Ch. | 16 | 16 | 32 \(^*\) | 32 | 8 | 8 | 8 | 8 | 8 | 16 |
| # Stimulation Ch. | 1 | 16 | 32 | 1 | 1 | 2 | 2 | 1 | 16 |
| Area (\(\text{mm}^2\)) | 1.563 | 0.95 | 0.031 \(^*\) | 0.237 | 0.244 | 0.182 \(^*\) | 0.729 | 0.031 \(^*\) | 0.13 | 0.014 |
| Energy Efficiency (RF/Ch) | 2.73 | 64 \(^*\) | 0.0412 \(^*\) | 178.7 \(^*\) | 0.036 \(^*\) | 170.9 \(^*\) | 174.4 \(^*\) | 0.0005 \(^*\) | 0.97 | 0.227 |
| Memory (kB) | 64 \(^*\) | - | 1 | 96 \(^*\) | - | 35.8 \(^*\) | 64 | 0.2 | 134 \(^*\) | 3.17 \(^*\) |
| Classifier | D/A-LSSVM | Ridge Regression | XGB-DT | EDM-SVM | BrainForest | NL-SVM | Course Thr (LS-SVM) | LR + SGD | GTCASVM | NeuroTree |
| Feature Set | SE | FFT, ApEn | LL, POW, VAR, SK | PLV, CFC, SE | RAF Neurons | SE | MODWT-KDE | SE, LL | SE | PLV, PAC, SE, HIPPO, LL, LMP, BPHT |
| Data (\# Patients) | MIT (14) | Local (5) | iEEG (20) | EU-iEEG (4) | EU-iEEG (4) | MIT (24) | MIT (24) | UoM (24) | MIT (24) | MIT (24) |
| Sensitivity (\%) | 95.7 | 96 | 83 | 100 | 96.7 | 96.6 | 97.8 | 97.9 | 97.5 | 100 |
| Specificity (\%) | 98 | 100 | 88 | 0.81/Fpr | 0.87/Fpr | 0.28/Fpr | 99.7 | 98.2 | 98.2 | 99.5 |
| Latency (s) | 1 | 0.76 | 1.1 | <0.1 | - | 0.71 | <0.3 | 2.6 | 1.6 | 0.74 |

* Estimated based on SoC area and \(\#\) of recording channels

\(^*\) Including data storage

\(\Delta\) Estimated based on \(\text{AFI}\) and \(\text{DBE}\) power consumption

over the state-of-the-art. The compressed NeuralTree takes up 2.93kB out of the 3.17kB on-chip memory, enabling more efficient memory utilization than SVM classifiers [5], [17], [19], [20], [22]. For instance, the recent SVM classifier in [22] utilized 70kB of memory to store 256 support vectors for 16 channels. The proposed SoC achieves better multi-channel scalability than previous DT-based SoCs [16], [18] thanks to the end-to-end TDM implementation. Moreover, the SoC integrates the broadest range of neural biomarkers reported so far to provide greater flexibility for multiple neural classification tasks.

VII. CONCLUSION

To pave the way towards next-generation closed-loop neural interfaces, this article presented a highly scalable, versatile neuroactivity classification and closed-loop neuromodulation SoC integrating an area-efficient dynamically addressable 256-channel mixed-signal front-end, multi-symptom biomarker extraction, an energy-aware NeuralTree classifier, and a 16-channel HV compliant neurostimulator. A channel-selective inference scheme was introduced to overcome the limited scalability and low hardware efficiency of the existing SoCs. Through aggressive system-level time-division multiplexing and energy-efficient circuit-algorithm co-design, the proposed 256-channel SoC achieved the highest level of integration reported so far, as well as the highest energy and area efficiency. The versatility of the SoC was demonstrated using human epilepsy and Parkinson’s datasets with multiple signal modalities (EEG, iEEG, and LFP). This high-channel-count SoC with the multi-class NeuralTree model can be further used for motor intention decoding in prosthetic BMIs.

ACKNOWLEDGMENT

The authors acknowledge Ivan Furfaro for his contribution to the in-vivo experimental setup. This work was partially supported by the National Institute of Mental Health Grant R01-MH-123634 and funding from EPFL.

REFERENCES

[1] V. L. Feigin et al., “Global, regional, and national burden of neurological disorders during 1990–2015: A systematic analysis for the global burden of disease study 2015,” The Lancet Neurology, vol. 16, no. 11, pp. 877–897, Nov. 2017.

[2] T. L. Skarpaas and M. J. Morrell, “Intracranial stimulation therapy for epilepsy,” Neurotherapeutics, vol. 6, no. 2, pp. 238–243, Apr. 2009.

[3] A. C. Meidahl, G. Tinkhauser, D. M. Herz, H. Cagnan, J. Debarros, and J. Yoo, “A 16-channel patient-specific closed-loop neural-stimulation system for the treatment of Parkinson's disease and related disorders,” Expert Review of Medical Devices, vol. 18, no. 4, pp. 319–332, Apr. 2021.

[4] L. Yao, P. Brown, and M. Shoaran, “Improved detection of Parkinsonian resting tremor with feature engineering and Kalman filtering,” Clinical Neurophysiology, vol. 131, no. 1, pp. 274–284, Jan. 2020.

[5] M. A. B. Altaf, C. Zhang, and J. Yoo, “A 16-channel patient-specific seizure onset and termination detection SoC with impedance-adaptive transcranial electrical stimulation;” IEEE Journal of Solid-State Circuits, vol. 50, no. 11, pp. 2728–2740, Oct. 2015.

[6] M. Shoaran et al., “A 16-channel 1.1mm\(^2\) implantable seizure control SoC with sub-\(\mu\)W/channel consumption and closed-loop stimulation in 0.18\(\mu\)m CMOS,” in IEEE Symposium on VLSI Circuits (VLSI-Circuits). IEEE, Jun. 2016, pp. 1–2.

[7] B. Jarosiewicz and M. Morrell, “The RNS System: Brain-responsive neurostimulation for the treatment of epilepsy;” Expert Review of Medical Devices, vol. 18, no. 2, pp. 129–138, Feb. 2021.

[8] J. Jimenez-Shahed, “Device profile of the percept PC deep brain stimulation system for the treatment of Parkinson’s disease and related disorders,” Expert Review of Medical Devices, vol. 18, no. 4, pp. 319–332, Apr. 2021.

[9] A. H. Shoeb, “Application of machine learning to epileptic seizure onset detection and treatment,” Ph.D. dissertation, Massachusetts Institute of Technology, 2009.

[10] L. Yao, P. Brown, and M. Shoaran, “Improved detection of Parkinsonian resting tremor with feature engineering and Kalman filtering;” Clinical Neurophysiology, vol. 131, no. 1, pp. 274–284, Jan. 2020.

[11] O. G. Sani, Y. Yang, M. B. Lee, H. E. Dawes, E. F. Chang, and M. M. Shanachi, “Mood variations decoded from multi-site intracranial human brain activity;” Nature biotechnology, vol. 36, no. 10, pp. 954–961, Nov. 2018.

[12] Y. Ezyyat et al., “Closed-loop stimulation of temporal cortex rescues functional networks and improves memory;” Nature communications, vol. 9, no. 1, pp. 1–8, Feb. 2018.

[13] T. L. Skarpaas and M. J. Morrell, “Intracranial stimulation therapy for epilepsy,” Neurotherapeutics, vol. 6, no. 2, pp. 238–243, Apr. 2009.

[14] L. Yao, P. Brown, and M. Shoaran, “Fast and accurate decoding of finger movements from ECoG through Riemannian features and modern machine learning techniques,” Journal of Neural Engineering, vol. 15, no. 1, p. 016037, Feb. 2022.

[15] C.-H. Cheng et al., “A fully integrated 16-channel closed-loop neural-prosthetic CMOS SoC with wireless power and bidirectional data telemetry for real-time efficient human epileptic seizure control;” IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3314–3326, Sep. 2018.

[16] M. Shoaran, B. A. Haghhi, M. Taghavi, M. Farivar, and A. Emami-Neyestanak, “Energy-efficient classification for resource-constrained biomedical applications;” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 8, no. 4, pp. 693–707, Jun. 2018.
[59] B. Zhu, M. Taghavi, and M. Shoaran, “Cost-efficient classification for neurological disease detection,” in *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*. IEEE, Oct. 2019, pp. 1–4.

[60] M. Abadi et al., “TensorFlow: A system for large-scale machine learning,” in *12th USENIX symposium on operating systems design and implementation (OSDI 16)*, Nov. 2016, pp. 265–283.

[61] D. P. Kingma and J. Ba, “Adam: A method for stochastic optimization,” arXiv preprint arXiv:1412.6980, Dec. 2014.

[62] K. J. Miller et al., “Human motor cortical activity is selectively phase-entrained on underlying rhythms,” *PLOS Computational Biology*, vol. 8, no. 9, p. e1002655, Sep. 2012.

[63] J. P. Uehlin et al., “A single-chip bidirectional neural interface with high-voltage stimulation and adaptive artifact cancellation in standard CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1749–1761, May 2020.

[64] T. Van Breussegem and M. Steyaert, “A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler,” in *2009 Symposium on VLSI Circuits*. IEEE, Jun. 2009, pp. 198–199.

[65] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns, “A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 244–256, Sep. 2011.

[66] I. R. Minev et al., “Electronic dura mater for long-term multimodal neural interfaces,” *Science*, vol. 347, no. 6218, pp. 159–163, Jan. 2015.

[67] L. Velisek, H. Kubova, M. Pohl, L. Stankova, P. Mareš, and R. Schickerova, “Pentylenetetrazol-induced seizures in rats: An ontogenetic study,” *Naunyn-Schmiedeberg’s archives of pharmacology*, vol. 346, no. 5, pp. 588–591, Nov. 1992.

[68] A. L. Goldberger et al., “PhysioBank, PhysioToolkit, and PhysioNet: Components of a new research resource for complex physiologic signals,” *Circulation*, vol. 101, no. 23, pp. e215–e220, Jun. 2000.