Simulation Study of the Double-Gate Tunnel Field-Effect Transistor with Step Channel Thickness

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Abstract
Double-gate tunnel field-effect transistor (DG TFET) is expected to extend the limitations of leakage current and subthreshold slope. However, it also suffers from the ambipolar behavior with the symmetrical source/drain architecture. To overcome the ambipolar current, asymmetry must be introduced between the source and drain. In this paper, we investigate the performances of DG TFET with step channel thickness (SC TFET) by utilizing the 2D simulation. The asymmetry between source and drain is introduced through the step channel thickness; hence, the ambipolar behavior is expected to be relieved. The results show that the SC TFET exhibits significant reduction of ambipolar current compared with the conventional DG TFET. The mechanisms of SC TFET are thoroughly discussed to explore the physical insight. The impacts introduced by the structure parameters on onset voltage, subthreshold slope, drain current in on-state and ambipolar-state are also exhibited in determining the optimal structure.

Keywords: Tunnel field-effect transistors, Double-gate, Step channel thickness, Ambipolar current, TCAD simulation

Background
As the extreme scaling process continues, CMOS technology with conventional MOSFET encounters various challenges such as the increasing leakage current and subthreshold slope (SS). Tunnel field-effect transistor (TFET), which utilizes the band-to-band tunneling (BTBT) mechanisms, is expected to extend the limitations of leakage current and SS [1–8]. Silicon-based TFET shows advantages such as high reliability and low cost. However, conventional silicon-based TFET exhibits a relatively low on-current in comparison with the MOSFET due to the constrained BTBT rate [9–11]. To develop the potential of silicon-based TFET, various novel TFET structures have been recently proposed to enhance the on-state current. The double-gate TFET (DG TFET) shows improved BTBT rate, leading to the enhanced on-current [12–14]. However, the ambipolar current of DG TFET is also increased since the BTBT rate improvement is activated in the ambipolar state as well [15]. To further overcome the ambipolar current, asymmetry must be introduced between source and drain [16]. DG TFETs with gate-drain underlap and less drain doping concentration are common methods to relieve the ambipolar problem [17–19]. But the gate-drain underlap requires greater S/D distance and less drain doping concentration increases the series resistances [15]. A previous work has shown that the ambipolar effects in the TFET with drain underlap could be further relieved by using the low-k spacers and by placing the contacts in the top and bottom configuration [15], suggesting that combined asymmetry strategies could be meaningful in improving the performance of the TFET. In our previous work, the FinFET with asymmetry fin width has been demonstrated to improve the performance of FinFET [20]. It is also believed that the channel thickness $t_{ch}$ has a significant impact on the BTBT rate of DG TFET [21]; hence, the asymmetry between the source thickness and the drain thickness might further

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relieve the ambipolar current and need to be studied thoroughly.

In this paper, we investigate the various performances of DG TFET with step channel thickness (SC TFET), the asymmetry between the source and drain is introduced through the step channel thickness so that the ambipolar current is expected to be reduced. The rest of this paper is arranged as follows: Section 2 presents the device structure and simulation setup. In Section 3, the mechanisms of the SC TFET is thoroughly discussed. The detailed discussion regarding the impacts of structure parameters on the transfer curves, onset voltage ($V_{\text{onset}}$), average SS and drain current in on/ambipolar-state is also presented. Finally, the findings of this paper are enlightened in section IV.

Structure and Simulation
The schematic diagram of the SC TFET considered in this paper is shown in Fig. 1a. The channel thickness near the source region is not equal to the channel thickness near the drain region. The channel thickness changes stepwise at a certain point in the channel region. The step height and the step position are denoted as $H$ and $L_s$ respectively. $t_{si1}$ and $t_{si2}$ are the channel thickness near the source region and the drain region respectively. The effective oxide thickness (EOT) is 1 nm in our simulation. The source region is highly p-doped ($10^{20}$ atoms/cm$^3$) and the drain region is highly n-doped ($10^{20}$ atoms/cm$^3$) to reduce the series resistance [15], the channel region is lightly n-doped ($10^{17}$ atoms/cm$^3$). In order to analysis the onset voltage with various channel thickness setups, the work function of metal gate is fixed to 4.5 eV, the gate length is equal to the channel length $L_{ch}$ and set to 50 nm [22–25]. The simulations are carried out using Sentaurus TCAD release I-2013.12 [26, 27]. The doping dependence model and the field dependent mobility model are Philips unified mobility model and Lombardi mobility model, respectively. The Fermi–Dirac statistics, Shockley–Read–Hall and Auger recombination model are also utilized. In order to account for the highly doped source/drain regions, the band gap narrowing model is activated. The nonlocal BTBT model based on Wentzel–Kramer–Brillouin (WKB) approximation tuned with the experimental results of [28] and the density-gradient quantization model are enabled to achieve the accurate simulation [29, 30]. The onset voltage is defined as the gate voltage at which the subthreshold slope is maximum. The average SS is extracted from the off-state current to $I_d = 10^{-11}$ A/µm.

Results and Discussion
Transfer Curves and Mechanism
Figure 1b shows the transfer curves of SC TFET and conventional DG TFET in log and linear scale, respectively. We mark out the on-state, off-state, and ambipolar-state in Fig. 1b. For TFETs, a higher current of on-state and a lower current of ambipolar-state are always desired, which requires that the $V_{\text{onset}}$ and SS should be low while the off-state should have a wide voltage range. As shown in Fig. 1b, the $V_{\text{onset}}$ of conventional DG TFET with channel thickness of 10 nm are lower than that of the DG TFET with channel thickness of 20 nm. The extracted $V_{\text{onset}}$ of DG TFET with $t_{si} = 10$ nm is 0.04 V and its extracted average SS is 44.8 mV/dec, the $V_{\text{onset}}$ and the average SS of conventional DG TFET with $t_{si} = 20$ nm is 0.1 V and 50.6 mV/dec, respectively. The drain current of conventional DG TFET with $t_{si} = 10$ nm is improved by 94.7% compared to the conventional DG TFET with $t_{si} = 20$ nm. The main reason of this drain current improvement is the reduced SS.
and $V_{\text{onset}}$. However, the off-state range of the conventional DG TFET with $t_{\text{si}} = 10$ nm is only 0.17 V. The conventional DG TFET with $t_{\text{si}} = 20$ nm, in comparison, exhibits off-state range of 0.45 V. As a result, the ambipolar-state current of the conventional DG TFET with $t_{\text{si}} = 20$ nm is reduced by 3 orders of magnitude compared to the conventional DG TFET with $t_{\text{si}} = 10$ nm.

For the fair comparison, the $t_{\text{si1}}$ and $t_{\text{si2}}$ of SC TFETs are equal to the channel thicknesses of above conventional DG TFETs, respectively. The narrower channel thickness $t_{\text{si1}}$ of SC TFET is 10 nm and the wider channel thickness $t_{\text{si2}}$ of SC TFET is 20 nm. The position of step is assumed at the middle of the channel and the $L_{s}$ is 25 nm. One can observe that the SC TFET shows promising characteristics including the high drain current in the on-state as well as the wide range off-state. The drain current of SC TFET in the on-state is similar compared to the conventional DG TFET with $t_{\text{si}} = 10$ nm, the average $SS$ is 45.8 mV/dec and the $V_{\text{onset}}$ is 0.03 V. However, the off-state range of SC TFET is improved up to 123.5% and the ambipolar-state current is also reduced by 3 orders of magnitude in comparison with the conventional DG TFET with $t_{\text{si}} = 10$ nm. As a result, the on-state characteristics of SC TFET is similar to the conventional DG TFET with narrow channel thickness, the SC TFET also shows nearly parallel off/ambipolar curves to the conventional DG TFET with wide channel thickness. Hence, the SC TFET can achieve low $SS$, reduced $V_{\text{onset}}$, and wide off-state range simultaneously.

To explore the physical mechanism of the SC TFET, we compare the BTBT rates and energy band diagrams in the on-state, near onset point and ambipolar-state, respectively. Figure 2a shows the BTBT rates of the SC TFET and the conventional DG TFETs. It can be seen that the BTBT rate strongly depends on the channel thickness. In fact, the relationship between the channel thickness and the BTBT current $I_{\text{BTBT}}$ can be expressed as [31].

$$I_{\text{BTBT}} \propto \exp \left( -\frac{4\lambda \sqrt{2m^*E_g^{2/3}}}{3h(\Delta\Phi + E_g)} \right)$$

(1)

Where $\lambda = (\epsilon_{\text{si}}t_{\text{si}}t_{\text{ox}}/2\epsilon_{\text{ox}})^{1/\alpha}$ is the natural length, $\epsilon_{\text{si}}$ and $\epsilon_{\text{ox}}$ are the silicon and oxide permittivity respectively and $t_{\text{ox}}$ is the oxide thickness. $\Delta\Phi$ is the energy range over which tunneling can take place, $E_g$ is the band gap at the tunnel junction, and $m^*$ is the tunneling mass. Equation (1) indicates that the $I_{\text{BTBT}}$ should increases as $t_{\text{si}}$ reduces. Therefore, the BTBT rate of conventional DG TFET with $t_{\text{si}} = 10$ nm should greater than that of the conventional DG TFET with $t_{\text{si}} = 20$ nm. The SC TFET shows similar distribution of BTBT rate to the conventional DG TFET with $t_{\text{si}} = 10$ nm. This is because that the BTBT mainly occurs near the source junction in the on-state, hence the channel thickness near the source junction will determine the on-state BTBT rate. Figure 2b shows the energy band diagram of the SC TFET and the conventional DG TFETs. Since the BTBT rate is fundamentally related to the tunneling distance, the energy band diagram, which can present the tunneling distance clearly, will explain the origin of BTBT rates variation. In Fig. 2b, the minimum tunneling distance of the SC TFET is located near the source junction and is more or less equal to that of the conventional DG TFET with $t_{\text{si}} = 10$ nm. The minimum tunneling distance of conventional DG TFET with $t_{\text{si}} = 20$ nm is significantly wider; hence, its BTBT rate is reduced compared to the SC TFET and the conventional DG TFET with thinner channel thickness.

Figure 3a shows the BTBT rates when the gate voltage is zero and is close to the onset voltage. It can be seen...
that the SC TFET owns the highest BTBT rate, followed by the conventional DG TFET with $t_{si} = 10$ nm. The conventional DG TFET with $t_{si} = 20$ nm shows the lowest BTBT rate. Figure 3b exhibits the corresponding energy band diagram. One can observe that the location of minimum distance from the valence band to the conduction band is at the center of channel region. Besides, the minimum distance of the conventional DG TFET with wider channel thickness is longer than that of the SC TFET and conventional DG TFET with thinner channel thickness. It indicates that the channel thickness also has a significant impact on the BTBT rate at the onset point. Hence, the $V_{onset}$ is dependent on the channel thickness as well. Another fact is that the SC TFET exhibits greater BTBT rate than that of the conventional DG TFET with $t_{si} = 10$ nm even though their minimum channel thicknesses are equal. This phenomenon is attributed to the variation of potential distribution introduced by the corner of gate electrode, as can be also observed in other work [32, 33]. As a result, the SC TFET shows the lowest $V_{onset}$ followed by the conventional DG TFET with thin channel thickness, and the conventional DG TFET with wide channel thickness exhibits the highest $V_{onset}$.

Figure 4a shows the comparison of BTBT rates in the ambipolar-state. Since the BTBT rate is strongly dependent on the channel thickness, the conventional TFET with $t_{si} = 10$ nm shows the most significant BTBT rate compared to the other two TFET structures. The SC TFET, however, shows the similar BTBT rate to the conventional DG TFET with $t_{si} = 20$ nm. It is because that the tunneling is mainly generated near the drain region and the SC TFET has wider channel thickness near the drain region. In Fig. 4b, the energy band diagram in the ambipolar-state is also exhibited. It can be clearly seen that the minimum tunneling distance is located near the drain region. Besides, the tunneling distances of
Fig. 5 The impacts of $H$ on the a transfer curves, b Vonset and BTBT rate, c average SS, and d drain current in on/ambipolar state, $H$ is the height of the step and $H = 0$ nm represents the conventional DG TFET.

Fig. 6 The impacts of $L_s$ on the a transfer curves, b Vonset and BTBT rate, c average SS, and d drain current in on/ambipolar state, $L_s$ is the lateral distance from the source region to the step, $L_s = 0$ nm represents the conventional DG TFET with corresponding $t_{si2}$ and $L_s = 50$ nm represents the conventional DG TFET with corresponding $t_{si1}$. 
SC TFET and conventional DG TFET with wider channel thickness are greater than that of the conventional DG TFET with thinner channel thickness, resulting in the low ambipolar current of SC TFET and conventional DG TFET with wider channel thickness.

Impacts of \( H \) and \( L_s \) on DC Characteristics

Figure 5a shows the transfer curves of the SC TFET with various \( H \) and \( t_{si1} = 10 \) nm. It can be seen that the \( H \) has less impact on the on-state current. The ambipolar current, however, reduces significantly as the \( H \) increases, the off-state range improves with the rise of \( H \) as well. It can be also seen that the reduction of the ambipolar current decreases as the \( H \) increases. The reason for this is that the coupling effect of the double-gate structure tends to be less significant with a larger channel thickness \([31]\). Therefore, as the \( H \) increases, the BTBT rates become more independent of the channel thickness, leading to the saturation of ambipolar current.

To further explore the optimal structure parameter, the effects of \( H \) varies from 0 to 15 nm on the device performances are extracted and shown in Fig. 5b–d. Figure 5b exhibits the \( V_{onset} \) and the BTBT rate variation with different \( H \) and \( t_{si1} \). It can be seen that the \( V_{onset} \) decreases monotonically with the increase of \( H \). This is because that the corner of gate electrode would introduce the variation of the potential distribution in the channel region \([32, 33]\), resulting in the alteration of the BTBT rate and the \( V_{onset} \). Figure 5b demonstrates that the BTBT rate increases as the \( H \) improves. As a result, the decreased \( V_{onset} \) can be found with the increased \( H \). One can also observe that \( V_{onset} \) increases as the \( t_{si1} \) increases. The main reason is that the increased \( t_{si1} \) weakens the BTBT rate, resulting in a higher \( V_{onset} \). In Fig. 5c, the extracted average \( SS \) of SC TFET with various \( H \) and \( t_{si1} \) is shown. The trend of the \( SS \) with different \( H \) is opposite to that of the \( V_{onset} \). In another word, the \( SS \) rises as the \( H \) increases. We have mentioned that the on-state drain current is dependent on the \( t_{si1} \), so that the SC TFETs with different \( H \) but with the same \( t_{si1} \) should have the similar drain current in the on-state. Besides, it is also known that the \( V_{onset} \) decreases with the increase of \( H \). This implies that the range of gate voltage to drive the same drain current is improved as the \( H \) increases. As a result, the average \( SS \) increases monotonically with the rise of \( H \). It can be also seen that the increase of \( t_{si1} \) will undermine the \( SS \), which is due to the reduced gate control capability. Figure 5d shows the drain current in the on-state and ambipolar-state with different \( H \) and \( t_{si1} \), respectively. The on-state current is nearly independent on the \( H \), but it is greatly affected by the \( t_{si1} \), which corresponds to our previous result that the on-state tunneling mainly occurs near the source region and is strongly dependent on the channel thickness near the source region. The ambipolar current, however, reduces as the \( H \) increases. Since the ambipolar-state tunneling is dominated near the drain region, the increase of \( H \) will improve the channel thickness at the drain side and thus weakens the ambipolar current. It can be also seen that the ambipolar current drops more significantly when the \( H \) is less than 10 nm, which is due to the greater coupling effect with thinner channel thickness.

In Fig. 5a, the transfer curves of SC TFET with different \( L_s \) are presented respectively. \( L_s = 0 \) nm represents the conventional DG TFET with corresponding \( t_{si2} \), and \( L_s = 50 \) nm represents the conventional DG TFET with corresponding \( t_{si1} \). It can be seen that the location of step has a significant impact on the ambipolar current and the off-state range. The SC TFETs with \( L_s \) less than 30 nm show similar ambipolar current and off-state range. As the \( L_s \) exceeds 30 nm, the ambipolar current is greatly enhanced. Fig. 6b shows the \( V_{onset} \) and the BTBT rate variation with...
various $L_s$ and $t_{sil}$, the trend that the $V_{onset}$ increases as the $t_{sil}$ improves can be clearly observed as well. The change inflection point on the $L_s = 10$ nm is a result of the variety of the $t_{sil}$. Since $L_s = 0$ nm is the conventional DG TFET with a larger channel thickness, the BTBT rate would reduce, leading to an increased $V_{onset}$ and a decreased on-state current. Barring the case of conventional DG TFET, the $V_{onset}$ of SC TFET is increased monotonically as the $L_s$ rises, which is due to the reduced BTBT rate induced by the step channel structure. Figure 6c exhibits the impacts of the $L_s$ and $t_{sil}$ on the SS of SC TFETs. The increased $t_{sil}$ results in the degraded SS. According to Eq. (1), a raised channel thickness would lower the coupling effects between the gate electrodes, leading to a reduced gate control capability and an increased SS [12]. As the $L_s$ drops, the region with greater channel thickness will expand and would weaken the overall gate control capability. As a result, a reduced $L_s$ will undermine the SS of SC TFETs, which can be clearly observed in Fig. 6c. Figure 6d presents the drain current in the on-state and ambipolar-state with different $L_s$ and $t_{sil}$, respectively. One can observe that the on-state current of SC TFET is more or less equal to the conventional DG TFET with corresponding $t_{sil}$. As for the ambipolar current, the SC TFETs with $L_s$ less than 30 nm show the similar current to the conventional DG TFETs with corresponding $t_{sil2}$. When the $L_s$ increases to 40 nm, the ambipolar current rises dramatically. In fact, for the case of SC TFET with $L_s = 40$ nm and $t_{sil} = 20$ nm, its ambipolar current is even greater than that of the conventional DG TFET with $t_{sil} = 20$ nm. This is because that the vertical part of gate electrode can enhance the tunneling area especially when the vertical part of gate electrode is close to the PN junction [34]. It indicates that the $L_s$ should be less than 40 nm for the purpose of reducing ambipolar current.

To determine the optimal structure parameters of the SC TFET, an orthogonal simulation is conducted by studying the combined effect of the $H$ and the $L_s$ on the device performance. The $t_{sil}$ is fixed at 10 nm to achieve a greater on-state current. In Fig. 7a, the ambipolar current is extracted as a function of the $L_s$ with various $H$. It can be clearly seen that the ambipolar current reduces significantly as the $H$ decreases, which suggests that a higher $H$ is promising in terms of achieving a lower ambipolar current. However, one can observe that the benefit from a greater $H$ is less significant. Therefore, a $H = 15$ nm would be the optimal value considering that a larger $H$ could only increase the device area. Meanwhile, a decreased $L_s$ will also lower the ambipolar current especially with a greater $H$. Hence, a lower $L_s$ is desired for the purpose of minimal ambipolar current. Nevertheless, a lower $L_s$ could also lead to an increase of

![Fabrication process of the SC TFET](Fig. 8 Fabrication process of the SC TFET. a Silicon substrate preparation with SiN and photoresist deposition. b Etching, implantation, and annealing. c Isolation oxide deposition. d Reducing the thickness and width of SiN by ashing and trimming. e The step channel thickness is introduced. f Gate oxide forming, gate deposition, gate planarization, and source region implantation)
the subthreshold slope, as can be observed in Fig. 7b. The subthreshold slope increases slowly with a higher \( L_s \) but rises rapidly with a lower \( L_o \) indicating that a \( L_s \) about 25 nm would be the compromise value. As a result, the optimal device parameters would be \( H = 15 \) nm and \( L_s = 25 \) nm where both the ambipolar current and the subthreshold slope are relatively low.

Fabrication Method
A feasible fabrication process of the SC TFET is exhibited in Fig. 8. Due to the unique shape of channel, the step channel thickness can be achieved more easily by adopting the vertical structure. The process begins by preparing the silicon substrate with SiN and photoresist deposition, as shown in Fig. 8a. In Fig. 8b, the SiN patterning is achieved by lithography, following by the etching to form the channel region, then the N⁺ region is introduced by a vertical As implantation and annealing [35]. After that, the isolation oxide is deposited to prevent the drain region from etching in the following process, as shown in Fig. 8c. In Fig. 8d, the ashing and trimming are adopted by utilizing the reaction ion etching [36] to reduce the thickness and width of SiN. The step channel thickness is then introduced by etching, as shown in Fig. 8e. The remain processes are similar to the conventional vertical TFET, involving gate oxide forming, gate deposition, silicon exposure, and source region implantation [35, 37], as shown in Fig. 8f.

Conclusion
We investigate the electrical performances of DG TFET with step channel thickness (SC TFET) by utilizing the 2D simulation. The asymmetry between the source and drain is introduced through the step channel thickness; hence, the ambipolar behavior is significantly relieved. The SC TFET exhibits similar on-state characteristics of the conventional DG TFET with corresponding \( t_{si1} \) and parallel off/ambipolar curves of the conventional DG TFET with corresponding \( t_{si2} \). As a result, the SC TFET can achieve wide off-state range, low ambipolar current, and maintain the low SS simultaneously. The mechanisms of SC TFET are thoroughly discussed to explore the physical insight. The impacts introduced by the structure parameters on onset voltage, subthreshold slope, drain current in on-state, and ambipolar-state are also studied to determine the optimal structure. The SC TFET with \( H \) of 15 nm and \( L_s \) of 25 nm shows the optimal performances. Moreover, the architecture of step channel thickness provides an alternative asymmetry method. Since the combined asymmetry strategies are proved to be effective, our work could further provide performance improvement of the TFET.
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