Design and Implementation of Dual-channel 100MSPS Data Acquisition Module

Hong Yang¹ᵃ*, Xuemei Li¹ᵇ*, Yifan Wang²ᶜ* and Bo Xu²ᵈ*

¹ School of Mechanical and Electrical Engineering, Chengdu University of Technology, Chengdu, Sichuan, 610051, China
² School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan, 611731, China

ᵃ yh283737060@163.com,ᵇ 278417025@qq.com,ᶜ 353946294@qq.com,ᵈ 835636728@qq.com

Abstract—Aiming at the problems of single channel acquisition mode of traditional oscilloscope recorder, insufficient acquisition flexibility, low acquisition frequency, transmission delay, etc., this paper proposes a design method of dual-channel signal acquisition module based on FPGA hardware platform. This design uses a high-sampling-rate ADC chip AD9268 as a dual-channel acquisition port to achieve 100MSPS sampling frequency acquisition, while simultaneously transmitting the converted digital signal through the SerDes serial port. In the FPGA implementation process, a channel conditioning module is added to adjust the gain and offset of the input data. The test results show that the system can realize synchronous sampling, processing, and transmission of the input analog signal, and the acquisition process is stable, and the collected signal has a high degree of restoration and no distortion.

1. Introduction

The current electronic measuring instrument working environment is complicated, the working frequency is getting higher and higher, and the generated signal is also becoming more diversified, which puts forward higher requirements on the measuring instrument. In recent years, large foreign technology companies, including Tektronix in the United States, Yokogawa in Japan, and Rohde & Schwarz in Germany, have shifted their focus to the research of measuring instruments, especially recorders, to seize new markets. The domestic development in the field of electronic measurement technology is relatively late, and domestic brands are not very competitive in the international market, but many domestic brands including Unitech, Puyuan, Hantai and other domestic brands are also constantly launching a variety of new oscilloscopes. In scientific research institutions, researchers have further increased their research efforts on oscilloscope recorders. Literature [1] proposed a multi-channel synchronous acquisition design scheme for oscilloscope recorders; literature [2] used PC-DAQ hardware structure and The LabVIEW software platform designed a multi-channel virtual oscilloscope recorder to reduce the cost of the instrument; Literature [3] uses an independent electrical isolation signal channel to realize a handheld oscilloscope with an analog signal isolation circuit from DC to 300Mhz; Literature [4] The oscilloscope recorder with four modes of normal, peak, high resolution, and average is realized by using the pipeline structure. Most traditional oscilloscope recorders mainly measure electrical signals and adopt single-channel acquisition mode. The mode based on hardware platforms such as embedded also makes traditional recorders unable to achieve large-scale data acquisition and processing, and it is
also difficult to solve signal synchronization. Sampling problem. In view of the wide application market and actual development needs of the existing oscilloscope recorder, this paper proposes a design scheme of a dual-channel 100MSPS oscilloscope data acquisition module based on FPGA hardware platform. Command control, realize 100MSPS sampling frequency through dual-channel ADC chip. The output uses SerDes high-speed interface to complete dual-channel data synchronous transmission, and with the help of FPGA hardware platform parallel transmission structure to improve data collection, processing, and transmission speed.

2. Principle

2.1. UART Transport Protocol
Universal Asynchronous Receiver/Transmitter is a commonly used serial data transmission protocol in the communication field. The transmission interface only includes the power supply VCC, the ground line GND, the sending data line TX, and the receiving data line RX. Its transmission structure is shown as in Fig. 1.

![Fig.1 UART transfer interface](image)

The UART serial port transmission protocol can transmit data bit by bit in a single bit form. This method is simple to operate, and is widely used in program debugging and communication modules that do not require high transmission speed. Since there is no control signal line and transmission clock signal line, the data transmitted by the UART serial port must meet the specified protocol format, as shown in Fig. 2.

![Fig.2 UART transfer interface](image)

The start bit changes to logic 0 to indicate the start of data transmission. The check bit can verify the correctness of the transmitted data by judging whether the total number of "1"s is odd or even. The stop bit is a sign of the end of data transmission, and it can be selected to be 1-bit, 1.5-bit, or 2-bit high-level representation. The data transmission rate is set by the baud rate, which controls the number of binary digits transmitted per second [5-7].

2.2. SerDes Transport Structure
SerDes, that is, serializer/deserializer, this transmission structure is the key core to realize source synchronization technology, which can realize the synchronous transmission of data and reference clock, and its characteristic is that the clock and data always keep relative The fixed phase relationship, the connection example diagram of the transceiver channel port is shown in Fig.3.

![Fig.3 SerDes port connection](image)
SerDes uses differential data lines to transmit data, which can effectively suppress common mode interference and support higher transmission frequencies and longer transmission distances. The SerDes structure contains a CDR (Clock Data Recovery) circuit, which can extract the clock from the data edge information and find the optimal sampling position. Therefore, the SerDes interface path does not include a clock signal line [8-12].

2.3. ADC9268
AD9268 is a more commonly used analog-to-digital conversion chip. It supports a maximum sampling rate of 125MSPS and an analog input range of 1.0V peak-to-peak to 2.0V peak-to-peak. It adopts a 1.8V single power supply and a multi-stage, differential pipeline structure. It has low power consumption and output Stability and other characteristics. AD9268 supports SPI transmission interface, through which the internal registers can be configured to control the ADC. The input port can realize dual-channel data synchronization acquisition, the output port supports 16bit data parallel transmission, and supports 1.8V CMOS or LVDS mode output [13]. AD9268 also has a synchronization input port (SYNC), allowing users to synchronize the clock divider through flexible synchronization options, thereby ensuring the synchronization of the sampling clocks of multiple ADCs.

As shown in Fig.4, when AD9268 selects CMOS mode for output, the data output timing of channel A and B are the same, and data is transmitted on the falling edge of the DCOA/DCOB data clock. As shown in Fig.5, when AD9268 selects LVDS mode for output, channel A transmits data on the rising edge of the DCOA data clock, and channel B transmits data on the falling edge of the DCOB data clock. As shown in Figure 6, the user can access the AD9268 address space and read and write the address space through the clock signal line SCLK, chip select signal line CSB, serial data input/input data line SDIO according to the SPI transmission protocol to meet specific functions And operational needs.
3. System Design

3.1. Overall Plan
The overall design of the dual-channel 100MSP data acquisition module is shown in Fig.7. The entire system includes a decoder module, AD sampling module, digital filter module, synchronous transmission module, and dual-channel conditioning module. The data acquisition transmission channel is mainly through the AD9268 analog-to-digital conversion chip, matched with peripheral circuits, to form a data acquisition port. The collected data passes through the CH1 and CH2 channel differential data lines, filtered by the digital filter, and transmitted to the processing board through the source synchronization interface. Since the input analog signal requires an indicator of 20mV-200V, and the selected AD9268 supports no more than 2.0V peak-to-peak input, the design introduces a dual-channel conditioning module, which is embedded into the two-stage attenuation circuit through 4 DAC chips, and passes the stage The way of joint program control realizes the attenuation quantization of the input signal.

3.2. Control Instruction Module Design
The input part of the control instruction module is divided into three parts: UART interface, SPI interface, and instruction address interface, as shown in Fig.8. The UART interface realizes the communication between the acquisition board and the back-end processing board. It is divided into single-ended UART and differential UART dual modes. The differential mode can effectively suppress the influence of common mode noise. In dual-mode operation, single/differential port data input can be controlled through the selector signal line switch_control.

The UART transmission protocol supports a single transmission of up to 8bit data. In order to achieve long-bit wide data transmission, the data is divided into multiple 8-bit data packets for transmission, and then restored to multiple-bit wide data after passing through the UART_MODE module. According to design needs, two UART data packets are used as the address space, and eight UART data packets are
used as the data space for command control. Therefore, in the end, each frame of data string consists of 6 data packets, with a bit width of 48bit, including 16bit address and 32bit data. In theory, 65536 data address spaces can be generated, but according to actual system design needs and taking into account the maximum resource utilization, in this design, the input 16bit address is divided into the lower 12 effective bits, and 4096 data addresses are generated for the system to use, and each address corresponds to a 32bit effective data. Because the data adopts serial transmission mode, in order to identify the starting position of each frame of data string, this design adds two 0x55 UART data packets as the start signal of the data string before each valid data. Table 1 contains the main control commands and corresponding register addresses in this design, which can decode the UART serial port (single-ended or differential), SPI serial port, and upper computer input data.

| Register address | Command             | Implication                        |
|-----------------|---------------------|------------------------------------|
| 0x0010          | oserdes_data_sel    | Select mode for sending data       |
| 0x0011          | dac_select          | DAC chip selection                 |
| 0x0012          | dac_data            | DAC configuration data             |
| 0x0013          | pc_cmd              | PC instruction                     |
| 0x0014          | ch1_control         | Functional control of channel 1    |
| 0x0015          | ch2_control         | Functional control of channel 1    |
| 0x0016          | flash_wr            | FLASH cache data                   |

3.3. Channel Conditioning Module Design

After the system is powered on, before data acquisition, the output port should maintain 0V output, and the electronic components in the hardware circuit are connected by DC coupling, and the gain amplifier circuit and the differential circuit will produce voltage offset. Therefore, the system uses four LTC2642 DAC chips as two-channel calibration control. The input command of the channel calibration module is sent by the upper computer and decoded by the decoder to obtain 16bit calibration data. The calibration data is processed by the spi_DAC module and then transmitted to the channel selection module spi_mux_choose using the SPI transmission protocol. The select_dac port can select the calibration channel. 00 means to adjust the impedance offset of channel 1, 01 means to adjust the VGA gain of channel 1, and 10 means to adjust the impedance offset of channel 2. 11 represents the VGA gain adjustment for channel 2, as shown in Fig.9.

3.4. ADC Data Module Sampling Design

According to AD9268 chip data manual\(^\text{[13]}\), control the SCLK/DFS pin to connect to the external voltage of AGND, and select the output data format as offset binary mode. The formula for the relationship between the output data and the collected voltage and the collected analog voltage is shown in (1).

\[
V_{in} = \frac{2 \times V_{ref}}{2^n} \times D - V_{ref}
\]

\[
V_{ref} = 0.5 \times (1 + \frac{R}{R_1})
\]
\( V_{in} \) indicates the voltage value of the collected analog signal. \( n \) represents the effective bit width of the output parallel data, which supports a maximum of 16bi, namely \( n_{\text{MAX}} = 16 \). In this design scheme, the sampling accuracy is 12bit width, so \( n = 12 \). \( D \) represents the decimal value of the output data. It is the AD9268 peripheral reference voltage. This value is determined by the resistance ratio in the peripheral circuit. The formula is shown in (2). According to the peripheral hardware circuit design of AD9268 in this system, \( R_s / R \) ratio is 3, and \( V_{ref} = 4V \).

The collected data enters the AD9268 sampling module through the two pairs of differential data signal lines \( \text{ad1}_p, \text{ad1}_n, \text{ad2}_p, \text{ad2}_n \) to achieve dual-channel analog data acquisition. Since the internal data of the FPGA adopts a parallel transmission architecture, first use the primitive IBUFDS pair provided by Xilinx. The collected data is converted from differential to single-ended operation, and 6 bits of parallel data are obtained respectively. The data output format of AD9268 is DDR mode, and data is transmitted twice in each clock cycle, and the data is reduced in a ratio of 1:2 using IDDR primitives. The IDDR IP core sends the low bit of the input 1bitDDR data to the data_even port on the rising edge of the clock, and sends the high bit to the data_odd port on the falling edge of the clock. Under the single-channel acquisition model, the interface module requires 6 pairs of IDDR parallel blocks to analyze the collected data. Under the dual-channel acquisition model, to complete the analysis and speed reduction of 12 pairs of differential signals with one sampling clock, at least 12 pairs of IDDR parallel block synchronization processing are required. In the Verilog code implementation, the generate_for statement is used to cyclically generate 6 groups of DDR_bit_inst[i] modules in channel 1, and 6 groups of DDR_bit_inst[j] modules are cyclically generated in channel 2. This method can reduce the amount of code, standardize the code, and improve the code Readability and executable. After the speed is reduced, 1bit data will output 2bit adjacent data stream, and the 6bit data collected by a single channel will be reduced to 6 pairs of cross data pairs, which are logically combined to form a 12bit data stream.

The AD9268 sampling clock is provided by the SERDES module to ensure the synchronization of the acquisition and transmission clocks. However, in order to ensure the synchronization of the entire system clock domain during data processing, the PLL clock frequency division module generated by the 50M crystal oscillator circuit on the hardware platform is used. After the 100MHz clock signal. Therefore, it is necessary to import the received data into the FIFO IP core for cross-clock domain processing. Since the smallest unit of the FPGA chip Block ROM supports 18bit width and 1024 depth, in order to ensure maximum resource utilization, two Block ROMs are combined in parallel to form a 32bit width and 1024 depth FIFO memory. The FIFO write clock signal uses the acquisition clock deo differential clock line, and the read clock signal uses the system 100M clock line. Dual-channel 12-bit data high-order zero-filling, combined into a 32-bit data stream, after FIFO cross-clock domain processing, logically separated into dual-channel 12-bit data stream, processed by the digital filter and led to the odata_ch1 and odata_ch2 output ports, as shown in Fig.10.

3.5. Data Transmission Module Design
The design supports dynamic reconfiguration in hardware, and the transmission interface adopts a source synchronous interface to transmit data and clock at the same time to achieve the purpose of high-speed
and synchronous transmission. The core of the module uses the high-speed SerDes interface primitives provided by Xilinx, which includes the sender OSERDES2 and the receiver ISERDES2. In this design, only the problem of sending data is considered, so OSERDES2 primitives are embedded in the transmission module Oserdes_trans to realize the conversion of parallel data to serial data. The formula for calculating the bandwidth required for high-speed transmission is as shown in formula (3).

\[ W_{\text{BandWidth}} = \omega_1 \times \omega_2 \times \omega_3 \]  

(3)

\( \omega_1 \): Sampling frequency; \( \omega_2 \): Sampling resolution; \( \omega_3 \): Number of sampling channels. The maximum sampling rate of this design is 100MSPS, dual-channel structure, 12bit resolution, the data is brought into formula (3), and the result is that the actual bandwidth of the SerDes interface is not less than 2.4Gbps as shown in Formula(4).

\[ W_{\text{BandWidth}} = 100\text{Ms} \times 12\text{bit} \times 2\text{ch} = 2.4\text{Gbps} \]  

(4)

Fig.11 ADC sampling module

The single-ended clock input CLK_IN of the OSERDES2 primitive of the SerDes transmitter is set to 200Mhz, the serialized input clock CLK_DIV_IN in the I/O logic is set to 100Mhz, and 8 data differential channels and 32bit data input ports are configured. Select the data sampling mode as DDR mode. At the same time, to facilitate system debugging, two modes are configured in the transmission module. In normal mode, Oserdes_trans receives 12bit data sampled and filtered from ADC_9268. In calibration mode, Oserdes_trans pulls up the calibration enable signal every 10 microseconds and transmits 0x7000_0000 once. The receiving module at the back end will use the shift port Bitslip of the ISERDES2 IP core to shift the input calibration data 0x7000_0000 by one bit to the right and three bits to the left, find the correct boundary position, and complete the word alignment calibration, as shown in Fig.11.

4. System Testing and Validation

As shown in Fig.12, the complete test platform of this design includes an acquisition board embedded with AD9268 for dual-channel data sampling; a maximum sampling frequency of 500Msa/s produced by Puyuan Jingdian Technology Co., Ltd., and the maximum output frequency The 160Mhz dual-channel signal generator is used to test the experimental analog input signal source; a DC stabilized power supply is used to supply power for the acquisition board; two signal lines connect the signal generator output port and the acquisition board input port, and a JTAG downloader The line is used to download the main program to the acquisition board. The host computer prepares the UART serial port debugging tool for sending instructions, and uses the Vivado2019.2 software to compile, synthesize and download the Verilog code. At the same time, the serial waveform data can be captured through the ILA IP core to facilitate the observation of the experimental results.
4.1. Control Instruction Verification

The host computer transmits control commands to the UART serial port on the board according to the system design requirements. The UART data packet uses 0x55_55 as the frame header to indicate the starting position of the data. The serial port sending interface is shown in Fig.13.

After the control instructions are processed and classified by the serial-to-parallel module inside the FPGA, they include 16-bit address data and 32-bit instruction data. First, input the oserdex_data_sel transmission port data selection command 0x0000_0000 to the address 0x0010, 0x0011, 0x0012, 0x0013, 0x0014, 0x0015, 0x0016 in turn to select the acquisition mode transmission; input dac_select DAC selection command 0x0000_0001 to control the DAC chip of channel 1; input dac_data to control the DAC Input command 0x0000_f012; input pc_cmd host computer command 0x0000_0001 to select the write function; input channel one ch1_control and channel two ch2_control initial configuration command 0x0000_0018; input flash write data 0x12ae_ad21. The input result is shown in Fig.14. The output display after decoding by the decoder is shown in Fig.15. Experimental results show that the design can serialize and process serial data, complete the address and data decoding operations, and achieve command control of other sub-modules.
4.2. Verify the Data Collection Function

First connect the input port of the system, set the output amplitude to 2V, the frequency is 20Mhz sine wave signal. The signal is collected by the acquisition board and quantized to obtain the dual-channel sine signal waveform at a sampling rate of 100MS/s as shown in Fig.16. As shown in Fig.17, the data conversion time of the quantization of the analog signal is 10ns, and the data resolution of the sampling point after quantization is 12bit. Experimental results show that the design module can complete the acquisition, hold, quantization, and coding of analog signals, complete analog-to-digital conversion, and achieve the design requirements of 100MS/s sampling rate.

4.3. Channel Conditioning and Data Transmission Function Verification

The acquisition module can quantize and process the analog signal to obtain a 12-bit wide digital signal. The digital signal will be adjusted through the conditioning channel in the hardware circuit for gain and offset adjustment, and finally output by the SerDes high-speed serial port. The channel conditioning control command refers to the LTC2642 chip data manual[14], and the data transmission function verification experiment control command configuration table is shown in Table 2.

---

**Table 2: Data Transmission Function Verification Control Command Configuration**

| Name            | Value |
|-----------------|-------|
| data_ch[1][11:0]| 2854  |
| data_ch[2][11:0]| 2854  |

---

| Name  | Value |
|-------|-------|
| CK_100M | 1     |
| data_ch[1][11:0] | 166   |
| data_ch[2][11:0] | 164   |
Table 2. Verify the experimental control instruction configurastion.

| Name               | Send_data | Select_dac | Channel | Channel bias |
|--------------------|-----------|------------|---------|--------------|
| Original sampling  | 16h8126   | 2b00       | ch1     | 0            |
| Original sampling  | 16h8014   | 2b01       | ch1     | 0            |
| Original sampling  | 16h8122   | 2b10       | ch2     | 0            |
| Original sampling  | 16h812f   | 2b11       | ch2     | 0            |
| Gain validation    | 16h8014   | 2b00       | ch1     | -1.5         |
| Gain validation    | 16h8002   | 2b01       | ch1     | 0            |
| Gain validation    | 16h8013   | 2b10       | ch2     | -1.5         |
| Gain validation    | 16h8001   | 2b11       | ch2     | 0            |
| Forward bias       | 16h81e0   | 2b00       | ch1     | 0            |
| Forward bias       | 16h8600   | 2b01       | ch1     | +1V          |
| Forward bias       | 16h81ff   | 2b10       | ch2     | 0            |
| Forward bias       | 16h8709   | 2b11       | ch2     | +1V          |
| Negative bias      | 16h8422   | 2b00       | ch1     | 0            |
| Negative bias      | 16h8000   | 2b01       | ch1     | -1V          |
| Negative bias      | 16h8323   | 2b10       | ch2     | 0            |
| Negative bias      | 16h800f   | 2b11       | ch2     | -1V          |

In the original signal sampling experiment, the channel_handle module is configured to ensure that the sampling signal is in a zero-bias, full-scale output state. The peak-to-peak value of the sine wave of the theoretical sampling signal is +3V, but in the actual sampling experiment, the peak-to-peak value of the sine wave collected by ch1 is +3.124V and -2.999V, the error is 4.13% and 3.37%, respectively; the peak-to-peak value of the sine wave collected by ch2 is +2.932V and -2.798V, the error is 2.27% and 6.73% respectively.

The gain verification experiment is based on the original signal sampling experiment, based on the full-scale and zero-bias state, the configuration signal gain is -1.5. The peak-to-peak value of the sine wave of the theoretical sampling signal is +2V, but in the actual sampling experiment, the peak-to-peak value of the sine wave collected by ch1 is +2.142V and -1.781V, and the errors are 7.10% and 10.95%, respectively; the peak-to-peak value of the sine wave collected by ch2 They are +1.982V and -2.121V, and the errors are 0.90% and 6.05%, respectively.

The forward bias verification experiment is based on the original signal sampling experiment, and the collected signal is controlled to be forward biased by 1V. The sine wave of the theoretical sampling signal is offset by 1V to the positive half axis, and the theoretical peak value is +3V and -2V. But in the actual sampling experiment, the peak-to-peak value of the sine wave collected by ch1 is +3.210V and -1.822V, the error is 7.00% and 8.90%, respectively; the peak-to-peak value of the sine wave collected by ch2 They are +1.982V and -2.121V, and the errors are 0.90% and 6.05%, respectively.

The negative bias verification experiment is based on the original signal sampling experiment, and the collected signal is controlled to be negatively biased by 1V. The sine wave of the theoretical sampling signal is shifted by 1V to the negative half axis. Because the full-scale output has been selected, the trough of the sine wave is clipped after the negative shift, and the theoretical peak-to-peak value is +2V and -3V. But in the actual sampling experiment, the peak-to-peak value of the sine wave collected by ch1 is +1.877V and -3.112V, and the errors are 6.15% and 3.73% respectively; the peak-to-peak value of the sine wave collected by ch2 is +2.148V and -2.981V , The errors are 7.4% and 0.63% respectively.
All test experiments use the ILA core provided by Xilinx to capture the output waveform of the SerDes serial port of the system output port, and the display result is shown in Fig.18. Among them Fig.(a) the sine wave waveform collected in the figure and the experimental data provided by the waveform generator only have an error value within 7%, and the collected signal shows basically the same reduction degree, indicating that the transmission interface is normal and the data transmission is stable. Fig.(B) The figure mainly verifies the dual-channel gain adjustment. Through the configuration command, the original signal amplitude is reduced by 1.5 times. The experimental results prove that although there is an error value of about 7%, the basic gain adjustment function can be realized. Fig. (c) and Fig.(d) respectively bias the collected sinusoidal signals by 1V in the positive and negative directions. The experimental results show that the system can complete the bias of the collected signals without considering the error value in the range of 9%. control.

5. Conclusion
This design uses FPGA as the hardware platform and proposes a dual-channel 100MSPS data acquisition module design program. Test experiments prove that the program can not only meet the dual-channel synchronous acquisition, and reach the design requirements of 12bit resolution, but also adopts SerDes high-speed synchronous serial port. Support data transmission under 2.4Gbps bandwidth. The input serial port in this design contains three protocols of UART, SPI, and parallel input, unified data packet format, and performs address-instruction one-to-one decoding operation on input data, which makes the system run more smoothly, with better compatibility and better portability. The dual-channel simultaneous working mode can sample and transmit two analog signals at the same time, which effectively expands the application of the use scene and has more practical value. The next step will be to use this design as the general architecture of the acquisition board. By adding and modifying the sampling circuit, modifying the serial port protocol, etc., a multi-function oscilloscope recorder that can support multiple sampling modes such as strain, temperature, acceleration, etc. is designed.

References
[1] He, X.S. (2019) Research on Acquisition Board Hardware Design and Multi-channel synchronization technology of Oscillograph Recorder. University of Electronic Science and Technology of China, Chengdu.
[2] Gao, Z.J., Zhou, J., Zhou, F.Q., et al. (2010) Design and implementation of multichannel virtual Oscillograph System. J. Computer measurement and control., 18(5):1221–1224.

[3] Zhou, Y. (2016) Isolation Channel design of 300Mhz Handheld Oscilloscope. University of Electronic Science and Technology of China, Chengdu.

[4] Zhao, J., Ren, W., Yang, Y., et al. (2020) Design of acquisition module of oscillograph Recorder based on FPGA. J. Electronic Measurement Technology., 43 (11) : 132-137.

[5] Wang, Y.B., Wang, H.B. (2020) Design of UART Serial Port between FPGA and PC. J. Journal of Lanzhou Institute of Technology, 27 (5) : 56-61.

[6] Chang, L., Bi, J.Z., Jiang, J.Q. (2020) The Method of UPGRADING FPGA by UART. J. Journal of Jilin University, 38(3) : 286-290.

[7] Lv, Y., Liu, L.N., Zheng, L.G., et al. (2020) Design and Implementation of Universal UART Module based on Verilog HDL. J. Electronic Design Engineering, 28(8) : 174-179.

[8] Song, L.F., Shen, X., Ying, W.Y., et al. (2021) Research on high-speed SerDes debugging method based on serial port. J. Electronics & Packaging, 21(3) : 1-6.

[9] Wang, J.X. (2020) Design of 28Gbps SerDes Tx Module Based on 28nm Process. University of Electronic Science and Technology of China, Chengdu.

[10] Li, P.J., Shen, J.L., Yuan, H.X., et al. (2021) A Multi-protocol SerDes Circuit for Interconnected Systems defined by Application Software. J. Acta Electronica Sinica, 49(4) : 817-823.

[11] Dong, J.Y. (2020) Design of 16Gbps SerDes controller. Xidian University, Xian.

[12] Guo, K.L., Wang, H.M., Liu, T., et al. (2020) Design of a Novel High Linearity Phase interpolator based on High-speed SerDes Non-equivalent Current Source Technology. J. Journal of Air Force Engineering University, 21(4) : 61-67.

[13] Analog Devices. (2009) AD9268 Datasheet. https://www.analog.com/cn/products/ad9268.html.

[14] Analog Devices. (2007) LTC2642 Datasheet. https://www.analog.com/cn/products/ltc2642.html.