Progress towards innovative and energy efficient logic circuits

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Abstract. The integration of superconductive nanowire logic memories and energy efficient computing Josephson logic is explored. Nanowire memories are based on the integration of switchable superconducting nanowires with a suitable magnetic material. These memories exploit the electro-thermal operation of the nanowires to efficiently store and read a magnetic state. In order to achieve proper memory operation a careful design of the nanowire assembly is necessary, as well as a proper choice of the magnetic material to be employed. At present several new superconducting logic families have been proposed, all tending to minimize the effect of losses in the digital Josephson circuits replacing resistors by adequate combinations of inductors in the logic gates. Among those, the nSQUID concept relies on the propagation of vortices along underdamped Josephson transmission lines. While, in principle, this logic family provides very low dissipation, several issues, such as speed and stability, have yet to be addressed. The current status of design and testing of n-SQUID logic gates and circuits as well as of the design and implementation of the nanowire memories is reported.

1. Motivation
This work is part of the Future Energy Efficient eLectronics (FEEL) INFN project, which is aimed to the development of new ideas for advancing the capabilities of superconducting digital logic in the directions of energy efficiency and scalability. More specifically, the integration of nanowire logic memories and energy efficient computing Josephson logic is explored.

Nanowire memories [1] are based on the integration of switchable superconducting nanowires with a suitable magnetic material. They exploit the electro-thermal operation of the nanowires to efficiently store and read a magnetic state. To achieve a proper memory operation a careful design of the nanowire is necessary, as well as a proper choice of the magnetic material to employ.

Several new superconducting logic families have been proposed, to minimize the effect of losses in the digital Josephson circuits replacing resistors by adequate combinations of inductors in the logic gates. Among those, the nSQUID [2-4] concept relies on the propagation of vortices along underdamped (no additional resistors) Josephson transmission lines introducing extra SQUID-like structures in each
section of the interferometer. While in principle this logic family provides very low dissipation, several issues, such as speed and stability, have yet to be fully addressed.

2. Energy efficient computing

Energy consumption has become the limiting factor for modern silicon digital electronics. Figure 1 shows a collection of achievements of several logic families, both semiconductive and superconductive [5]. While it is clear that CMOS are limited both in speed and energy consumption essentially by thermal dissipation, the superconductive Rapid Single Flux Quantum (RSFQ) logic shown two orders of magnitude less energy requirements, together with a substantial increase in speed. However, the necessity to operate at very low temperature (4K) almost nullifies the energy gain, as 1 W dissipated at 4 K corresponds, in the best case, to few hundred Watts dissipated at room temperature. Therefore, the necessity of developing much more energy efficient superconducting logic has come out, resulting in a variety of proposals, the blue squares in figure 1, that move towards the intrinsic quantum and thermal limits (dashed lines in figure 1). Among the proposed energy efficient logic families, the nSQUID is very promising [2-4], although somewhat difficult to control.

To investigate the energy requirements and operation of energy efficient superconducting logic, a test chip has been realized, using HYPRES 1 kA/cm² and 4.5 kA/cm² processes, containing ERSFQ and nSQUID technology circuits.[8] In figure 2 is shown the layout of the realized chip.

![Figure 1](image1.png)

**Figure 1.** Energy consumption per gate vs clock cycle for different digital logic families [5].

![Figure 2](image2.png)

**Figure 2.** Photograph of a 5 × 5 mm² test chip.

The results of tests of the realized circuits are reported in details in [8]. In figures 3 and 4 are summarized the main results obtained with ERSFQ and nSQUID technologies respectively. In figure 3 is shown the output signal obtained from a 13 bit divider realized with ERSFQ technology. The input frequency was 19.456 GHz with an amplitude of −25 dBm. In the figure is also shown a reference signal of frequency 593.75 kHz = (2375 / 4) kHz = (19.456 / 2₁⁵) GHz. The timing between the two signals shows the correct operation of the divider. The estimated power dissipated is less than 100 nW/gate @ 20 GHz, corresponding to the star symbol in figure 1.

In figure 4 is shown the result of the test of nSQUID logic. Input–output signal of the nSQUID NOT array obtained applying ±5 mA as “1” and “0” input signal. The output signal amplitude is about 6 μVpp. The experiment was performed only at very low frequency.
3. Nanowire memories

While superconducting logic has proven to be able to achieve very low dissipation, there is still a problem in realizing superconducting memories of small size. The actual RSFQ technology relies on SQUID loops to store the bits of information, but each loop has a minimum size of the order of 10 $\mu$m$^2$, which strongly limits the possibility of realization of large capacity memories.

Alternative memory elements have been proposed, based mostly on Josephson junctions with magnetic layer near or in the barrier.

The approach used here is different: it is based on a nanowire memory. The device is based on a superconducting nanowire of which there is a small magnetic core. The working principle is to heat the small magnetic volume through the induced switching to the normal state of the nanowire and therefore bring it above its Curie temperature for a short time. In this condition if a magnetic field is applied, much smaller of the magnetic material coercive field, a magnetization can be induced in the material while it is cooling. The resulting magnetic state affects the nanowire critical current and can be non-destructively read by a suitable current pulse.

In figure 5 a sketch of the proposed device is shown. On top of a superconducting a nanowire is deposited a thin rectangular layer of a suitable ferromagnetic material, having a Curie temperature below 20 K. The nanowire can be switched to the normal state by a short current pulse and, during this process, the temperature can reach the ferromagnet Curie temperature bringing it in the paramagnetic state.

By properly applying a small magnetic field, the ferromagnet can be easily magnetized in different directions, leading to two different magnetic configurations, as shown in figure 6.

A logic state 1, with a residual magnetization perpendicular to current flow and with field lines not crossing the nanowire, obtained by cooling the ferromagnet in presence of a small bias current.

A logic state 0 with a residual magnetization parallel to current flow and with field lines crossing the nanowire, obtained by cooling the ferromagnet in absence of bias current.

The two states are stable, if the temperature is kept at 4 K, and can be non-destructively read by suitable current pulses in the nanowire. A detailed discussion of the proposed memory is reported in [1].

Figure 3. Test of ERSFQ logic.

Figure 4. Test of nSQUID logic.
3.1. Nanowire realization
To test the proposed memory a set of nanowires, having different geometrical configuration has been realized and characterized. In figure 7 the layout of the test chip is shown, consisting in 22 strips of varying width (two in 4 wire contact mode), big pads for bonding, wide common electrode for all strips, on a 10x10 mm substrate. The fabrication process includes the following main steps: realization of Al contact and marker layer and geometrical definition by using a lift-off process, realization of the ultrathin NbN layer and geometrical definition by lift-off process, EBL sub-micron patterning with PMMA and RIE process to remove unwanted material.

As an example of the obtained nanowires, in figure 8 is shown the current voltage characteristic of a nanostrip having length 5µm and width 333 nm. The critical current was 35 µA at 4.2 K and at room temperature, normal resistance of 14.6 kΩ.

In figure 9 the temperature dependence of the current voltage characteristic of another test strip is shown. From the figure it can be seen that the nanostrip shows and hysteretic curve up to a temperature of 8.5 K. The nanostrip critical current is reduced with increasing temperature and vanishes at T = 9.5K (figure 10).
3.2. Choice of the appropriate magnetic material
The realization of the nanowire memory requires the use of a ferromagnetic material having a very low Curie temperature (below 20 K) and a reasonable coercive field.

Europium Sulfide (EuS) has a FCC crystal lattice with a rock salt structure and does not have intrinsic crystalline anisotropies, can be realized in the form of thin films, it is ferromagnetic at low temperatures, with a Curie Temperature $T_{cu} = 16.6$ K, a coercive field $H_c = 60$ Oe (at 2 K), and a magnetic moment $m = 6 \text{ mu}_B/\text{Eu}^{2+}$ (also at 2 K). At $T = 4$ K, the operational temperature of superconducting electronics, the magnetic moment of EuS is $m = 5 \text{ mu}_B/\text{Eu}^{2+}$. From the EuS density and molecular weight, it is possible to compute the material saturation magnetization $M_{sat} = 873 \text{ kA/m}$ and the saturation flux density $B_{sat} = 1.1 \text{ T}$. While the EuS magnetic properties are certainly in line with the requirements for the nanowire memories, the material requires a high deposition temperature (800°C) to make good quality thin films, and this is not compatible with standard superconducting electronic processing technology.

An alternative material to be explored is NdNi$_5$. This material has been realized for the first time in form of thin films. It shows an amorphous structure, room temperature deposition, and an expected low Curie temperature (below 20 K). These properties are encouraging. However, a full magnetic characterization is still needed and is in progress.

Meanwhile the transport properties of NdNi$_5$ thin films, having 40 and 200 nm thickness have been investigated. At low temperature ($< 50$ K for the 200 nm film) a characteristic upturn of resistivity can be observed (figure 11). By looking at the experimental data it is not possible to unambiguously determine the source of such behaviour, as both Kondo scattering, 3D weak localization and Sheng tunnelling model all fit equally well the experimental data.

However, by recording the low frequency noise spectrum generated by the material, it is possible to evidence a magnetic field dependence of the noise amplitude at temperatures below the resistivity minimum (figure 12). Such behaviour is a strong signature in favour of Kondo scattering as the source of the resistivity upturn.
4. Conclusions
The current state of development of energy efficient superconductive logic circuits and of a new type of superconductive memory has been reported. The work on ERSFQ and nSQUID is aimed at determining the energy consumption and stability of practical circuits employing these technologies. The activity on nanowire memories is aimed at optimization of the nanowire properties and on the identification of the best material to be used as magnetic memory. The overall goal is to demonstrate the operation of the superconducting nanowire memories and to integrate them with energy efficient logic.

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Figure 11. Temperature dependence of resistivity of two NdNi$_5$ thin films of different thickness. The full curves are best fits with theoretical models, shown in the legend.

Figure 12. Low frequency noise spectra of a 200 nm thick NdNi$_5$ film at different temperatures and for different values of an applied dc magnetic fields in the film plane.
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