Enabling Fast and Flexible Distributed Deep Learning with Programmable Switches

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ABSTRACT
Deep learning has been used in a wide range of areas and made a huge breakthrough. With the ever-increasing model size and training data volume, distributed deep learning emerges which utilizes a cluster to train a model in parallel. Unfortunately, the performance is often far from linear speed-up due to the communication overhead between cluster nodes.

To address this challenge, this paper designs and implements Libra, a network aggregator, that utilizes in-network computation to optimize the communication for distributed DL training in two aspects: i) reduce active connections and ii) aggregate exchanged network packets. We implemented our Libra on Intel Tofino switches, customized a lightweight host stack and integrated it into an open-source training framework PS-lite. The experimental result shows that our Libra can achieve 1.5–4× speedup.

1 INTRODUCTION
High-dimensional sparse data widely exits in Internet-scale deep learning (DL) applications, such as search engine, recommendation systems and online advertising [34, 39]. To enable efficient DL training with sparse data, sparse DL models [31, 32, 34] typically use a two-tier architecture, where the first tier is a SparseNet that embeds high-dimensional sparse data into a low-dimensional space via representation learning, and the second is a DenseNet that models the relationship between between the dense embedding representation and supervised labels. Two unique features distinguish the sparse DL models from the dense DL ones: (i) data sparsity that the samples from training data contain a large number of features, but only a few are non-zero; (ii) model sparsity that the most gradients are zero in each training iteration.

We have witnessed the huge increasing of the size of sparse DL models and the training datasets in recent years. For example, for a business advertising system [34], petabytes (PB) of training data is generated everyday, and the trained DL model consists of billions of features. Indeed, training a sparse DL model is a time-consuming task, and the distributed sparse DL training, which leverages a cluster of nodes to perform training tasks cooperatively, emerges and becomes a practice [49, 58].

A popular architecture for distributed DL is the parameter server (PS) architecture with data parallelism [26, 34, 38]. The training dataset is divided into equal-sized parts (called chunks). In each iteration, workers pull the up-to-date model from parameter servers and perform local training with a chunk of data. The local training results are then sent to parameter servers for the global DL model update. Distributed sparse DL training also follows the above procedure. It has been found that with the increasing of used workers, the communication between workers and parameter servers will become the performance bottleneck [13, 30]. Specifically, a recent measurement study [45] reveals that the two factors that hurt the performance: intensive and bursty communications.

A straightforward way to mitigate intensive communication is to reduce transmission data volume via gradient compression (e.g. gradient quantization [13] and sparse parameter synchronization [12]). Other solutions aiming at mitigating communication burstiness decouple the dependency between computation and communication [30, 33, 48] through scheduling. These solutions improved the performance at the end node side (i.e. workers). Another recently emerging direction is to explore the computation capacity in network devices, especially programmable switches, for gradient aggregation [17, 40, 50, 51], which can further accelerate the training process. Nevertheless, all the previous in-network aggregation solutions are targeted for dense distributed DL models. We found they indeed fall short in accelerating the distributed sparse DL training, because their streaming-based aggregation assumes synchronising all the local updates (i.e. gradients) in every worker in each training iteration, regardless of whether individual updates are zero or non-zero. This assumption no longer holds in distributed sparse DL training, as only the non-zero embedding vectors and non-zero gradients are transmitted in <key, value> pairs.

To address the above gap, we design and implement Libra to enable in-network gradient aggregation for distributed sparse DL training. Libra is built on our key observation from industrial sparse DL applications that the update frequencies of parameters in sparse deep models are extremely biased, where about 50% of updates are for only the top 30,000 parameters (out of over millions of parameters) (§ 3.1). Libra thus aggregates the gradients on programmable switches only for these hot parameters, and let the servers aggregate the gradients for the remaining cold ones. That said, rather than offloading the gradient aggregation task for all the parameters in [17, 40, 50, 51], Libra only offloads the task for the hot parameters, while keeping the aggregation task for the cold parameters in PS servers.

We address several challenges to implement Libra. First, we propose a sampling-based mechanism to identify the hot parameters by running the training task with a small sample (4% – 8%) of the whole dataset (§ 3.3). Second, we design a heat-based parameter placement mechanism at the switch side and a parameter layout (on switch registers) aware gradient packaging mechanism at the worker side to cooperatively reduce the probability that the associated parameters of one gradient packet belong to one register (§ 3.4). In doing so, we reduce the chances that one packet writes a register multiple times in a pipeline, which is not supported by programmable switches. Third, we propose a table-lookup mechanism that enables the on-the-fly floating-point summation on switches.
which is essential for gradients aggregation (§ 3.5). Last but not least, we enhance the reliability of Libra from the perspectives of packet loss recovery and switch failover (§ 3.6).

We implement Libra and integrated it with PS-Lite [7] and Intel Tofino [9] programmable switches (§ 4). We perform extensive experiments using a benchmark that includes various sparse DL training tasks (§ 5). The results demonstrate the superior performance of Libra, in comparison with the state-of-the-art solutions. In summary, our contributions are three-fold:

- We design Libra that accelerates the distributed sparse DL training with in-network gradient aggregation on programmable switches. Specifically, it offloads the aggregation task for “hot” parameters from PS servers to programmable switches.
- We propose the solutions that include the sampling-based hot parameter identification, the heat-based parameter placement on switches, the parameter layout aware gradient packaging on workers, the table-lookup mechanism for the on-the-fly floating-point operation on switches, and two enhancements for improving reliability.
- We implement Libra, and integrate it with PS-lite and Intel Tofino switches. Extensive experiments with real-world sparse DL applications demonstrate that Libra improves the aggregation throughput by 1.5–4x with limited extra overhead.

The remainder of this paper is organized as follows. Section 2 describes the background and the motivation. We present the design of Libra in Section 3. Section 4 shows some implementation details. We evaluate our Libra in Section 5 and present some discussion in Section 6. We finally discuss the related work in Section 7 and conclude our work in Section 8.

2 BACKGROUND AND MOTIVATION

2.1 Distributed Deep Learning

Distributed deep learning (DDL) leverages a cluster of training nodes (called workers) to cooperatively train DL models. We consider the widely used data parallelism mode, where the training dataset is divided into equal-sized parts to feed training nodes for local training. A widely adopted DDL architecture in industry is the parameter server (PS) architecture (see Figure 1); Microsoft Multiverso [2], Alibaba XDL [34] and ByteDance BytePS [48] are all built with this architecture. In the PS architecture, workers train their local DL models, while PS servers manage globally shared but non-overlapped DL model parameters. That said, the parameters that a PS server manages are non-overlapped with the parameters of any other PS servers. In each iteration of training, workers first pull the up-to-date model from parameter servers, and then perform forward-backward computation with one chunk of training data locally. At the end of an iteration, workers push the trained results (i.e., gradients) to the servers for updating the DL model.

**Synchronous vs Asynchronous.** Training jobs can be scheduled in either synchronous or asynchronous mode. Synchronous training requires PS servers to collect all the gradients from all workers at each integration; it is less effective when workers are equipped with different computation capacities. Asynchronous training, on the other hand, allows workers to work at their own pace, without waiting for other workers to finish their training.

**Reliable Transmission.** Although distributed DL training can tolerate some packet losses due to their special algorithm properties (e.g., bounded-loss tolerant) [55], reliable transmission is still a must in industry for two reasons [48]. First, distributed DL application developers assume reliable transmission in network substrate; they may optimize their training algorithms based on this assumption. Second, the gradient loss (due to transmission) will slow the training convergence and degrade the the end-to-end job performance. As such, the approaches that do not provide reliable transmission may not be viable in practice.

2.2 Sparse Deep Learning

High-dimensional sparse data widely exists in Internet-scale applications (e.g., search engine and online advertising). Data sparsity could cause low training efficiency if not handled properly; to this end, several sparse DL models have been proposed [31, 32, 34]. These models typically follow a two-tier architecture (see Figure 2): representation learning (SparseNet) and function fitting (DenseNet). The representation learning embeds high-dimensional sparse data into a low-dimensional space via embedding layers, while the function fitting models the relationship between dense embedding representation and supervised labels.

**Sparse model training.** Specifically, in the forward pass, a training node reads a batch of sparse data samples, maps them into

![Figure 1: The parameter server architecture.](image-url)

![Figure 2: A conceptual architecture of sparse deep training, and it consists of two types of training networks.](image-url)
dense embedding vectors via SparseNet\(^1\), and then feeds the results into DenseNet. The backward propagation reverses this data flow and output gradients. The generated gradients in each iteration consist of two parts: the sparse gradients for SparseNet and the dense gradients for DenseNet; only a few vectors of the SparseNet gradients are non-zero.

Table 1: Neural Network Characteristics of Multiple layer perception [32] (MLP), Crossmedia [24] (CM) and Deep interest network [59] (DIN).

| Deep Model | Neural Net. | # parameters |
|------------|-------------|--------------|
| MLP        | SparseNet   | 18 Billion   |
|            | DenseNet    | 1.2 Million  |
| CM         | SparseNet   | 5 Billion    |
|            | DenseNet    | 1 Million    |
| DIN        | SparseNet   | 18 Billion   |
|            | DenseNet    | 1.7 Million  |

Two unique features of the SparseNet distinguish sparse deep training from dense deep training. First, as listed in Table 1 which shows the model characteristics of three popular sparse models, the SparseNet uses a much larger training network with billions of parameters than that in DenseNet (millions of parameters). Second, while many gradients of SparseNet in each iteration are zero (i.e., sparse), there are still many heavy non-zero vectors. Let us take a NCF [31] model with a typical training dataset [29] as an example. In each iteration, out of 680MB of SparseNet gradients, \(\sim 104\text{MB}\) are for non-zero vectors; in comparison, the DenseNet only generates 0.4MB of gradients.

**Distributed sparse training.** In distributed sparse training, each worker runs the local training job showed in Figure 2, and synchronizes with other workers for both the SparseNet model and DenseNet model. To reduce the amount of gradient data for transmission, individual workers encode gradient vectors as a list of key-value pairs, and push only the non-zero vectors to PS servers in each iteration. Consequently, the parameters (indices) involved in the transmitted gradients from different workers may not be overlapped.

![Figure 3: Gradient updates in distributed sparse training.](image)

Figure 3 shows such an example. In the \(i\)-th iteration, Worker 1 pushes 3 non-zero gradients \((\theta_1, \theta_{201}, \theta_{901})\) for updating the global model, while Worker 2 and Worker 3 transmit non-zero gradients for other parameters (e.g., \(\{\theta_9, \theta_{919}, \theta_{990}\}\) from Worker 2). It is worth noting that the parameters with non-zero gradients in individual workers are unknown in advance.

### 2.3 Limitations of Prior In-network Aggregation

Recently, a large amount of research effort [17, 40, 51] has been devoted to in-network gradient aggregation in order to reduce the communication volume and improve the overall training performance. Specifically, programmable switches are exploited to sum the gradients sent by workers and send only the summation results to PS servers. By doing so, the data volume to PS servers is greatly reduced.

We particularly focus on two state-of-the-art systems that leverage programmable switches for in-network gradient aggregation: SwitchML [51] and ATP [17]. While being effective for dense training, they fall short in speeding up sparse DL training because of their streaming-based aggregation.

To show this, we briefly describe their workflow. As illustrate in Figure 4, the gradients are chunked into \(m\) streams at each worker, where the \(j\)-th \((j < m)\) stream in each worker contains the gradients for the same set of parameters. Each worker sends one stream at each time slot to programmable switches for aggregation. Programmable switches will aggregate (i.e., sum) the gradients of the \(j\)-th streams from all workers. This approach works well in dense deep learning, where in each iteration, the gradients of all the parameters need to be sent out for aggregation. Besides, because of the limited storage space in programmable switches, some approaches (e.g., ATP) require synchronization of time slots among workers — all workers not to transmit the next stream of gradients until the programmable switches relieve the last aggregated results. That said, they may not support asynchronous training.

![Figure 4: The Streaming-based in-network gradient aggregation in [17, 51].](image)

The above streaming-based approach does not work for deep sparse training, simply because in each iteration, only the non-zero gradients are sent to PS servers for aggregation. Worse still, the parameters with non-zero gradients in individual workers are unknown in advance. Simply applying existing approaches will lead to limited chances of aggregations on programmable switches, or even incorrect aggregation.

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\(^1\)Usually, one can look up a huge dictionary or utilize a few CNN/RNN models to implement data mapping.
Another design component in existing approaches that we aim to improve is about floating-point arithmetic. Because the state-of-the-art Tofino programmable switches only support integer summation [57], both SwitchML and ATP adopt a float-to-integer approach that converts floating-point gradients into integers via multiplying a scaling factor at the worker side. To reduce the accuracy loss introduced by this float-to-integer approach, a negotiation mechanism may be used. For instance, SwitchML requires all workers to negotiate with each other to decide an appropriate value of the scaling factor before transmitting the streams of gradient. Such frequent negotiations would introduce performance overhead. Another possible solution is to equip each switch with a floating-point unit (using FPGAs or ASICs) directly as in [56]. Unfortunately, this solution indeed increases the cost of switches while those “legacy” programmable switches that have been in widespread use today often do not have such units. That said, our Libra aims to calculate float-point gradients on the “legacy” programmable switches directly with high accuracy and low overhead.

3 LIBRA DESIGN
This section presents the design of Libra that is able to accelerate asynchronous distributed sparse DL training. We begin with the key observation that encourages the design of Libra, and then detail Libra’s main components.

3.1 Characterizing “Hot-cold” Phenomenon
We first present our observation on the highly skewed update frequency of parameters in distributed sparse DL training. This observation is derived from our (industrial) training tasks of two typical sparse deep learning models: search engine and online advertising recommendation.

Experimental setup. We use a testbed with 16 workers and 1 PS server to train DDL models for online advertising recommendation (Task 1) and search engine (Task 2). The model of Task 1 consists of 150 million parameters, while Task 2 contains about 9 million model parameters. During training, we collect logs from the PS server, and count the update frequency of each parameter.

Observation. We sort the DL model parameters based on their update frequency, and present the cumulative proportion of update frequency for the top 100K parameters in Figure 5. Our most surprising finding is that they contain very “hot” parameters who contribute the bulk of the update. For example, across the 150 million parameters, the top 30,000 parameters of Task 1 constitute over half of all updates. Likewise, for Task 2, its top 30,000 parameters even account for about 70% of updates.

Summary. High-dimensional sparse deep learning tasks exhibit a hot-cold phenomenon where the hot parameters contribute most traffic. Some independent research [45] also reported this phenomenon. Putting this in the context of in-network gradient aggregation, we envision a system that aggregates the gradients only for the “hot” parameters as they contribute most of the updates. By doing so, we can accelerate the distributed sparse training with a limited storage requirement on programmable switches.

3.2 Design overview
To restate, our Libra uses programmable switches for in-network sparse gradient aggregation. Figure 6 shows its two components on the switch, namely Libra_p and Libra_s. Libra_p is deployed on the switch pipeline to implement gradient aggregation, while Libra_s runs on the local CPUs of the switch to facilitate reliable transmission (see Section 3.6). Given the “hot-cold” phenomenon we observed, Libra adopts a hot-cold separation mechanism. Specifically, it selects those “hot” model parameters that are frequently updated for aggregation on switches, while the remaining “cold” parameters are handed over to the parameter servers without in-network aggregation. It is noteworthy that such a separation does not require synchronization between workers; workers can pull the up-to-date aggregation results from the switch and the parameter servers.

Figure 5: Cumulative distribution of the parameter update frequency for two production sparse models.

Figure 6: The overview of Libra.
3.3 Identifying Hot Parameters

Without running the training work, the hot parameters are unknown. In fact, the hot parameters cannot be accurately predicted because the update frequency of parameters do not follow a pre-defined pattern and thus may vary from a sparse DL task to another (see Figure 5).

To this end, we adopt a sampling-based mechanism to approximately capture the update frequency distribution of DL model parameters. To this end, we first extract a small training dataset by randomly sampling the whole dataset. We then train the DL model with the sampled dataset and record the update frequency of each model parameter. Finally, we sort the parameters based on their update frequency, and label the top k parameters as hot ones. As we show in §5.3, by running the training with only 8% of the whole dataset as input, we can identify hot parameters with an accuracy 90%.

The number of hot parameters (k) whose gradients will be aggregated also depends on the available resources on switches. Specifically, we identify hot model parameters based on Principle 1.

**Principle 1. (Hot parameter Identification).** Consider a list of parameters \( \theta = \{\theta_1, \theta_2, ..., \theta_n\} \) that are ranked in descending order by the update frequency. We use \( UF = \{u_1, u_2, ..., u_n\} \) to refer to their corresponding update frequency. We also assume that one programmable switch is equipped with 20MB on-chip memory, and storing a model parameter in a switch consumes 4 bytes of memory. We say that the \( \text{top-k} \) parameters \( \{\theta_1, ..., \theta_k\} \) are hot if they satisfy the following two conditions:

\[
\begin{align*}
T_k/T_n &\geq p \\
4B \times k &\leq c \times 20MB
\end{align*}
\]

where \( T_k = \sum_{i=1}^{k} u_i \), \( T_n = \sum_{i=1}^{n} u_i \), \( p \in (0, 1) \) and \( c \in (0, 1) \) are two design parameters.

The parameter \( c \) is the fraction of on-chip memory that we would like to use for gradient aggregation. In practice, \( c \) should be small (0.05 \text{--} 0.1) because occupying too much memory would affect conventional functions of switches (e.g., packet forwarding). The parameter \( p \) is the expected proportion of traffic that will be intercepted and processed by the switch. While a larger \( p \) is preferred (so as \( k \)), more memory would be required. Nevertheless, as showed in Figure 5, the marginal benefit in terms of traffic saving (i.e. the growth of \( p \)) when increasing \( k \) beyond some points (called trade-off points) becomes very small. Let us take Figure 5(b) as an example. Increasing \( k \) beyond 30K will bring very limited benefit in terms of traffic saving. In this example, \( k \) will be set as 30,000 in our implementation.

![Figure 7: An example of a register caching multiple parameters.](image)

3.4 Parameter Orchestration

**Parameter layout in switch registers.** The on-chip memory in a switch is physically organized as registers. A register is similar to an array (see Figure 7), which consists of multiple register slots. One hot parameter takes one register slot to cache its gradient; a new gradient will be added to the cached gradient to get the final summation of all the gradients of this parameter. A practical restriction on switches is that one register can be operated only once in one pipeline. That said, if a register cached gradients of two parameters whose updates are carried in one packet, they would not be able to be aggregated in one pipeline. While we could use the recirculation operation in programmable switches to recirculate the packet back to the pipeline, recirculations can degrade the performance. As such, we need to carefully assign hot parameters to registers so that the chances that the updates of two parameters assigned in one register are carried in the same packet is low.

Before delving into the detail of parameter layout, we first describe the mapping of parameter indices. Gradients in distributed deep sparse training are transmitted in the form of \(<key, value>\) pairs, where \( key \) is the index of a parameter. Because we will use the index to directly locate their corresponding register slots, we need to map the indices obtained from the models into the range of \([0, M-1]\), where \( M \) is the number of register slots used for gradient aggregation. Suppose we rank the parameters in descending order based on the update frequency; then a parameter’s index after mapping is its rank (from 0 to \( M-1 \)). Workers store the mapping information locally, which is used to restore the indices of the aggregation results.

![Figure 8: The heat-based parameter placement, where \( m \) registers are used to cache \( n \) hot parameters.](image)

Next we describe the parameter layout in registers using a heat-based parameter placement mechanism (see Figure 8). Specifically, let us consider a list of hot parameters \( \{\theta_1, \theta_2, ..., \theta_n\} \) ranked in descending order of their update frequency (i.e. heat). Our method places the \( n \) parameters into \( m \) registers as follows. The \( i \)-th register stores the \((i + m \times j)\)-th parameters, where \( 0 \leq j \leq \lfloor n/m \rfloor \). Our intuition is that the “heat” distribution of the hot parameters is non-uniform (see Figure 5), so the heat of \( \theta_i \) would be much higher than that of \( \theta_{i+m} \). Therefore, the probability that the gradients of \( \theta_i \) and \( \theta_{i+m} \) are encapsulated into one packet is low. That said, we can use one register to store \( \theta_i \) and \( \theta_{i+m} \). With this basis, we deduce the above conclusion that \( \theta_{i+m+j} \) where \( 0 \leq j \leq \lfloor n/m \rfloor \) are assigned to one register. We will show the effectiveness of this layout in §5.4.

**Packaging gradients at workers.** At the worker side, we adopt a parameter layout aware gradient packaging mechanism for encapsulate gradients into packets (see Algorithm 1). The core idea is to encapsulate parameter gradients into packets in order to achieve two goals: (i) reducing the likelihood that the parameters encapsulated to one packet are cached in one register; (ii) using as few
packets as possible. We assume that workers know the number of registers \( m \). When a batch of gradients for the hot parameters need to be transmitted, we use Algorithm 1 for packaging gradients into packets. The algorithm first estimates how many packets\(^2\) (denoted by \( P \)) are needed to carry these parameter gradients (line 2), and then process each parameter \( \theta \) as follows, where \( \theta \) is the (rank) index of the parameter.

- First, it uses the index of \( \theta \) to locate the register ID (\( k \)) that caches \( \theta \) (line 4) at switches;
- Second, it filters out the packets that have carried at least one parameter that also belongs to the \( k \)-th register (line 7 to 9);
- Third, it appends \( \theta \) in a candidate packet and updates corresponding states. (line 10 to 16);
- Fourth, if there is no such packet, \( \theta \) will be recorded to a set \((G')\) for further processing (line 17 to 18).

\[ G' \leftarrow \emptyset; P_1 \leftarrow P; \]  
\[ \text{// P is a list of packets.} \]
\[ \text{// Packaging G to n packets} \]
\[ \text{for } \theta \in G \text{ do} \]
\[ k \leftarrow \theta.id\%m; \]  
\[ \text{// Get register ID} \]
\[ P_2 \leftarrow P_1; \]  
\[ \text{// P_2 carries candidates for } \theta \]
\[ \text{is_inserted } \leftarrow \text{false}; \]  
\[ \text{// Find out pkts having already include the} \]
\[ \text{parameters sharing the same register with } \theta \]
\[ \text{res } \leftarrow \text{same_reg_pkt_find}(k); \]
\[ \text{if res } \neq \text{NULL then} \]
\[ \quad \text{P}_2 \text{.erase(res.begin(), res.end());} \]
\[ \quad \text{pkt } \leftarrow \text{P}_2 \text{.first();} \]
\[ \text{if pkt } \neq \text{NULL then} \]
\[ \quad \text{// pkt will carry } \theta. \]
\[ \quad \text{// P_1 tracks the full state of pkts.} \]
\[ \quad \text{Update(P1, pkt, } \theta); \]
\[ \quad \text{// Final results.} \]
\[ \quad \text{is_inserted } \leftarrow \text{true; } \]
\[ \quad \text{if is_full(pkt) } \equiv \text{True then} \]
\[ \quad \text{P}_1 \text{.erase(pkt);} \]
\[ \quad \text{if is_inserted } \equiv \text{true then} \]
\[ \quad \text{G'.append( } \theta ); \]
\[ \text{if G' } \neq \emptyset \text{ then} \]
\[ \quad \text{P_.insert(create_pkt_padding(G'));} \]
\[ \text{return } P; \]

\(^2\text{Because we need to parse the whole packet by the parser of programmable switches, the packet size is limited to 192 bytes.}\)

Finally, if \( G' \) is not empty, the worker will encapsulate the parameter gradients in \( G' \) into a number of packets without considering the parameter layout in switch registers (line 19-20). The reason why we do not use the packets in \( P \) to carry the parameters in \( G' \) is as follows. Let us assume that the number of parameters in \( G' \) is \( n \). If we used the packets in \( P \) to carry \( G' \), it would lead to \( n \) times recirculation operations. On the contrary, if we encapsulate them into new packets directly, the usage of recirculation operations can be significantly saved, because the parameters in \( G' \) are unlikely to belong to one register.

### 3.5 Gradient aggregation on switches

Switches parse the received gradient packets using their programmable parser. By doing so, the switch will get the a list of <key, value> pairs, each of which is the gradient (value) of a parameter with key as the index. Specifically, for an update of the parameter \( \theta \), the switch locates the register as well as the slot in the register that caches \( \theta \). More specifically, we use a hash table to map the the index of one parameter into the position of the registers. Then the update (i.e. gradient) is added to the cached value.

**Floating-point summation on switches.** Gradients are typically represented as 32-bit floats. Nevertheless, the pipeline in programmable switches does not support floating-point summation. Rather than using the aforementioned floating-to-integer method that may introduce accuracy loss, we propose a table-lookup method that enables the on-the-fly floating-point summation for 32-bit floats. Our method is inspired by [19] that implements floating-point operations for 16-bit floats.

For any two positive numbers \( x \) and \( y \), the following equation holds: \( x + y = 2^x \log_2(1 + 2^y) \), where \( i = \log_2(x) \) and \( j = \log_2(y) \). A 32-bit floats in IEEE 754 consists of three portions: the sign field (1 bit), the exponent field (8 bits) and the fraction field (23 bits); they together form a key for table lookup. Thus, a strawman solution is to set up three tables on switches: (i) a \( \log \text{Table} \) that is used to record the logarithm values of all possible keys; (ii) a \( \text{mitable} \) that is used to get \( \sigma(\theta) = \log_2(1 + 2^\theta) \) for a given \( \theta \); (iii) an \( \exp \text{Table} \) that is used to get the exponential value for a given key. Let us consider two 32-bit floats \( x \) and \( y \) to illustrate the floating-point operations using the these 3 tables. Both \( x \) and \( y \) are first mapped into the logarithmic number system [37] by looking up the first table (\( \log \text{Table} \)), yielding \( \log_2(x) \) and \( \log_2(y) \). Next it computes \( \theta = \log_2(y) \) minus \( \log_2(x) \) and uses \( \theta \) to look up the second table (\( \text{mitable} \)) and gets \( \log_2(1 + 2^\log_2(y) - \log_2(x)) \), which then is added by \( \log_2(x) \). Finally, the summation is taken as the key to look up the third table (\( \exp \text{Table} \)) to get the value of \( x + y \).

Unfortunately, the bit width of the key in \( \log \text{Table} \) can be up to 32 bits, so it would consume \( \sim 16 \text{GB} \) (\( 2^{32} \times 4 \) B) on-chip memory, which is unacceptable in practice. To this end, we further propose an approximate method to divide the large \( \log \text{Table} \) into a few small tables in order to reduce the memory consumption. More specifically, a positive IEEE 754 32-bit float \( p \) is represented as \( p = 2^{e-127} + 1.f_1f_2...f_{23} \), and we assume that \( m = 1.f_1f_2...f_{11} \) and \( \Delta m = 0.f_{13}f_{14}...f_{23} \approx 2^{-11} \). Consequently, \( p = 2^{e-127} + m + \Delta m \), and \( \log(p) = (e - 127) + \log(m + \Delta m) \). For any \( \log(m + \Delta m) \), it can be converted into a polynomial via Taylor series [8], and further be
We consider two sources of failures that would undermine Libra: packet loss and equipment failure.

**Packet Retransmission.** While packet loss happens much less frequently in data center networks (< $10^{-3}$ [28]), it indeed may happen. A packet loss would result in the loss of all the gradients the packet carries and thus degrading the training performance. To this end, we leverage the per-packet ACK mechanism for loss detection and retransmit the lost packets. Specifically, the receiver of a packet will immediately return an ACK to the sender. That said, switches will ack the gradient packets sent from workers; PS servers will ack the packets for cold parameters; and workers ack the aggregation packets that are sent either from switches or PS servers. The sender of a packet will mark the packet as loss if it does not receive the ack before the timer expires; the retransmitted packet has the same sequence number as the original one.

To implement the above mechanism, switches need to keep the unacked aggregation packets locally for possible retransmissions. To this end, when sending out aggregation packets to workers, switches also forward one copy to its local CPUs (Libra.s). That said, the local CPUs are only involved for reliable transmission.

In practice, we also observe the other error related to packet loss: *repeat-write-error*, where the ack packet is lost (see Figure 10). It happens in the case that the ack packet sent from a switch to a worker is lost, but the switch has aggregated the gradients carried by the packet that is being acknowledged. The worker deems the gradient packet has been lost, so it retransmits the packet. Without a local recording in the switch, the switch will wrongly aggregate the gradients twice.

![Figure 10: An illustration of the repeat-write-error.](image)

We address the issue caused by the repeat-write-error as follows. Workers will explicitly mark the retransmitted packet (e.g. using one bit in the packet header). When receiving a retransmitted packet, the switch will check the local records to figure out whether the gradients in the packet has been aggregated. The local records can be implemented either in local CPUs on the switch or using a Bloom Filter in the pipeline. Our current implementation relies on local CPUs.

**Failover mechanism.** Switches may fail unexpectedly in practice. For the traditional switches that only forward packets, we can reroute packets to detour around the failed switches. However, because now the switches have been leveraged for gradient aggregation, the above bypass-based mechanism will result in the loss of aggregated gradients on programmable switches and thus crash down the training task.

To this end, we design a detection-migration failover mechanism (see Figure 11), which leverages the controller of the switches for the detection of failure and invoking the task migration. Specifically, the controller periodically requests the status of switches through heartbeat messages. Switches reply with statistics of the switches (e.g. resource utilisation). The controller then uses these statistics along with the response delay to detect whether the switch is about to fail (e.g. high packet loss rates, high on-chip memory usage). If the controller finds out the abnormal status of the switch via the heartbeat packets, the switch states (a.k.a. aggregation results) are passively pulled by the controller.

Because the layout of the hot parameters on registers are predefined, Libra can deploy Libra.s and Libra.p to the standby switches in advance. The controller selects one of these standby

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1. While this on-chip memory demand is acceptable in practice, we can also leverage the prefix-based compression proposed in [19] to further reduce the memory consumption.

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3.6 System Reliability

The system reliability is important in production environments. We consider two sources of failures that would undermine Libra: packet loss and equipment failure.

**Packet Retransmission.** While packet loss happens much less frequently in data center networks (< $10^{-3}$ [28]), it indeed may happen. A packet loss would result in the loss of all the gradients the packet carries and thus degrading the training performance. To this end, we leverage the per-packet ACK mechanism for loss detection and retransmit the lost packets. Specifically, the receiver of a packet will immediately return an ACK to the sender. That said, switches will ack the gradient packets sent from workers; PS servers will ack the packets for cold parameters; and workers ack the aggregation packets that are sent either from switches or PS servers. The sender of a packet will mark the packet as loss if it does not receive the ack before the timer expires; the retransmitted packet has the same sequence number as the original one.

To implement the above mechanism, switches need to keep the unacked aggregation packets locally for possible retransmissions. To this end, when sending out aggregation packets to workers, switches also forward one copy to its local CPUs (Libra.s). That said, the local CPUs are only involved for reliable transmission.

In practice, we also observe the other error related to packet loss: *repeat-write-error*, where the ack packet is lost (see Figure 10). It happens in the case that the ack packet sent from a switch to a worker is lost, but the switch has aggregated the gradients carried by the packet that is being acknowledged. The worker deems the gradient packet has been lost, so it retransmits the packet. Without a local recording in the switch, the switch will wrongly aggregate the gradients twice.

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switches and sends the states to this switch. The selected switch then uses the migrated states to resume the training.

4 IMPLEMENTATION

We implement a prototype of Libra on commodity servers and programmable switches. Specifically, data plane components at switches are implemented with P416 language (1500+ LoC) and compiled with the Intel Capilano software suite; they are deployed to 3.2 Tbps Intel Tofino switches. Libra host stack is customised on lwIP, a lightweight user-level TCP/IP stack. Finally, we further integrate our Libra into PS-lite, an open-source parameter server platform.

Data plane component. Programmable switches like the Intel Tofino switch that we use have some restrictions on the access of registers and tables. A particular restriction that we have to deal with is that a register can only be read and written once per packet processing. In case we need to read and write a register more than once, we adopt the recirculation operation that recirculate to the packet back to the pipeline. In our implementation, a packet is at most recirculated once, i.e. it goes through the pipeline twice at most.

Host Stack. lwIP is a lightweight user-level TCP/IP stack; the current versions running on Linux servers only provide TAP/TUN virtual adapters. TAP/TUN adapters incur multiple packet copy operations and context switches between the kernel space and user space, degrading the whole performance. To this end, we turn to DPDK (Data Plane Development Kit). Specifically, we use DPDK APIs to implement a network device driver based on the template provided by lwIP; by doing so, lwIP can send/receive packets at line speed.

System integration. PS-lite utilizes ZeroMQ, which is a high-performance asynchronous messaging library, to enable high-performance communication between workers and PS servers. However, the vanilla ZeroMQ is based on the kernel stack. Thus, we use lwIP to replace its kernel stack via replacing the interfaces invoked in ZeroMQ.

5 EVALUATION

5.1 Methodology

Testbed Setup. Our testbed includes 8 physical machines connecting to an Intel Tofino programming switch (3.2T/s) that is equipped with two ARM cards (ARMv8.1 SoC, 24 cores). Each physical machine is equipped with 2 32-core Intel® Xeon®@2.14GHz CPU, 128GB memory and Mellanox CX-5 dual-port 100G NICs; the OS is Ubuntu 16.04.

Benchmarks. Our benchmark models include two types of sources: two industrial sparse DL applications and several real-world sparse models. The two industrial applications are search engine (SE) and on-line advertising (OA) from a large Internet enterprise (see Figure 5 for their characteristics). The real-world sparse models include DeepLight, LSTM and NCF, which are trained by a number of open-source datasets.

Baselines. We compare Libra with SwitchML, a state-of-the-art in-network aggregation solution, and the PS-lite framework which transmits non-zero gradients in form of <key, value>. To enable SwitchML to support sparse DL training, the gradients of the entire sparse DL model are transmitted in each iteration, rather than only the non-zero gradients. It is noteworthy that the default available memory of programmable switches for aggregation is limited to 1MB for both Libra and SwitchML.

We evaluate Libra from five aspects: (i) the effectiveness of sparse gradient aggregation; (ii) the feasibility of our sampling-based method for identifying hot model parameters; (iii) the benefit of the hot parameter layout and orchestration; (iv) the performance of the table-lookup floating-point summation compared with the float-to-integer solution used in SwitchML; (v) the overhead due to the introduced mechanisms for reliability; and (vi) the resource consumption on the switch data plane.

5.2 Aggregation Throughput

We first evaluate the aggregation throughput of Libra, and compare it with the two baselines. To this end, we use the tensors generated by training the benchmark models to test the aggregation throughput, where each worker transmits the tensors it generated when training individual models. It is noteworthy that in SwitchML, each worker has to transmit all gradients in each iteration, regardless whether the gradients are zero or not. Besides, we selected the top 30,000 parameters with the most update frequency as hot parameters for OA and SE (see Figure 5), top 40,000 for DeepLight, and top 60,000 for LSTM and NCF.

Figure 12 shows the aggregation throughput over 5 models. Libra consistently achieves higher aggregation throughput than that of the baselines, because of its sparse-awareness to aggregate only the hot parameters on programmable switches. Indeed, SwitchML falls short in terms of aggregation throughput in supporting these deep sparse training, because of its streaming-based aggregation that has to aggregate all gradients for all parameters on switches.

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4Each switch consists of two pipelines (i.e., ingress and egress pipelines), which contains 12 stages in total.

5We choose PS-lite as one baseline because it is the basis of many PS-based learning systems (e.g. MXNet).

6As in [40], we do not directly compare the end-to-end training performance in order to eliminate the impacts of computation capacities on workers on training performance.
(See §2.3). Because of the limited memory in the data plane for gradient aggregation (1MB), the benefit of in-network aggregation in SwitchML may even be out-weighted by its extra overhead, leading to even poorer performance than the PS-lite, especially for the models with high sparsity (e.g., DeepLight). Note, the PS-lite follows the typical deep sparse training where only the non-zero gradients are transmitted. We also find that the advantage of Libra becomes more significant as the number of the workers gets larger, because more workers means more opportunities of in-network aggregation. Specifically, with 32 workers, the aggregation throughput can be improved by 1.5∼4× in comparison with the PS-lite-sparse.

To show the impact of memory cap in the data plane on throughput, we increase the memory cap for in-network aggregation from 1MB to 2MB for SwitchML. We correspondingly double the number of hot parameters from 30K to 60K for Libra. We use 16 workers for this set of experiments.

Figure 13 shows the results. Both Libra and SwitchML benefit from increasing the switch memory. However, for Libra, the brought improvement is limited. Even if the offloaded hot parameters are increased up to 2.67 times, the improvement is below 7% for OA and 1.7% for SE. This is because that the extra offloaded parameters only correspond to a few traffic that can be aggregated. SwitchML seems more sensitive to the switch memory, and we double the used memory so that SwitchML is able to achieve more than 2.23X speedup comparing with its own default result. Indeed, for SwitchML, a large of switch registers enable SwitchML to aggregate more parameters at the same time. However, even so its aggregation throughput is far away from Libra equipped with the default configuration (only reaching 45.6%), since SwitchML indeed aggregates too much zero gradients. In addition, the available switch memory for in-network aggregation actually is often limited, which cannot provide sufficient resources to accelerate aggregation.

5.3 Precision of Hot Parameter Identification

We identify the hot parameters by running the training with a sampled small dataset (§3.3). In this set of experiments, we evaluate the precision in identifying the hot parameters. To this end, we first aggregated. Nevertheless, even with doubled memory usage, the aggregation throughput of SwitchML is only 45.6% of the throughput of Libra with default configuration. These results show the importance of sparseness-awareness when aggregating gradients for distributed deep sparse training.

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train the sparse models on our testbed with the whole datasets, and record the update frequency of each model parameter at the PS server side. By doing so, we get the global hot parameters. Specifically, we sort the model parameters in descending order according to the update frequency, and add each time 1,000 parameters to the hot parameter list \( H_g \) from the highest rank to the lowest, till the increase of the cumulative update frequency falls below a predefined threshold (1% in our experiment). We then train the sparse model with the sampled datasets, and use the same method to get the hot parameter list \( H_s \). Finally, we use \(|H_g \cap H_s|/|H_g|\) to evaluate the precision.

Figure 15: Precision of the sampling-based method in identifying hot parameters under different sampling rates.

Figure 15 shows the results. For the considered benchmark models, the precision exceeds 80% even with a sampling rate as low as 4%. Increasing the sampling rate to 8% improves the precision to over 90%. These results demonstrate the high accuracy of identifying hot parameters using our sampling-based method.

5.4 Evaluation of Hot Parameter Layout and Orchestration
We next evaluate the benefit of the parameter orchestration (see §3.4) in terms of the reduction of recirculations. In this set of experiments, we use the two benchmark models (OA and SE) from industry. We first design the parameter layout in registers and generate the packets accordingly at workers. We then count the number of recirculation operations needed on the switch and report the average number of recirculations for each packet. For the comparative purpose, we take a random parameter placement as the baseline.

Figure 16 shows the results, which demonstrate the effectiveness of our algorithm. Specifically, the average number of recirculations per packet is less than 1 for both models. In comparison, the random layout requires 10 recirculations per packet. The results also show the additional benefits of our gradient packaging method. We also notice that more recirculations are required in the OA model than the SE model. This is because the heat (i.e. update frequency) distribution of hot parameters in OA is less biased than SE (see Figure 5).

5.5 Benefit of Floating-Point Summation
We next evaluate the benefit of the on-the-fly floating point summation enabled by our table-lookup mechanism (§3.5). To this end, we first show in Figure 17 the extra delay introduced by the float-to-integer solution that is used in SwitchML [40] due to the scaling factor negotiation. We can see that for each iteration of negotiation, the extra delay is over 100ms when only 8 workers are used; the extra delay increases to 130ms when 32 workers are used for training. Note that our table-lookup solution does not need this negotiation and thus can save the extra delay.

Next we evaluate the precision of the two solutions using two datasets: 1) gradients from our benchmark models (\( R_1 \)); and 2) randomly generated floating-point numbers between (-1, 1) (\( R_2 \)). For the float-to-integer solution, we use a negotiated scaling factor as in [40]; in our table-lookup mechanism, each table is equipped with 30,000 entries (large enough to hold all possible numbers in our experiments). We selected 100,000 pairs of floating-point numbers from each of the two datasets and compute the summation of each pair of floats using the two mechanisms respectively.
Figure 17: The extra delay incurred in each iteration for negotiating the scaling factor in the float-to-integer mechanism in SwitchML [40].

Table 2: The precision of float summation.

| Solution          | Dataset | Median | Average |
|-------------------|---------|--------|---------|
| Float-to-integer  | $R_1$   | 99.97% | 99.89%  |
|                   | $R_2$   | 36.79% | 62.46%  |
| Table-lookup      | $R_1$   | 99.92% | 99.87%  |
|                   | $R_2$   | 100%   | 99.84%  |

Table 2 shows the results for the two solutions. Both solutions can achieve over 99.98% precision on the the DL benchmark dataset ($R_1$). However, on the random dataset $R_2$, the float-to-integer solution fail to provide a high precision, while the table-lookup solution still achieves a precision over 99.8%. The reason is that the range of decimals in deep learning applications are relatively small, so the float-to-integer mechanism can find out an appropriate scaling factor. In the random decimal dataset, however, the range becomes much larger and it cannot identify a proper scaling factor. It is worth noting that, as computed in §3.5, the table-lookup mechanism uses only about 408KB on-chip memory in the switch data plane.

In summary, the proposed table-lookup mechanism eliminates the need of scaling factor negotiation (and thus the extra delay) and achieves a high precision in gradient summation with very low overhead.

5.6 Evaluation of Packet Loss Recovery

To enable packet loss recover, the switch local CPUs are interleaved in the gradient packet processing (See §3.6). This may introduce extra delay. To evaluate this overhead, we trained the OA model in our testbed with packet loss rate varying from 0.01% to 0.1% as in [28]. Figure 18 shows performance loss with different packet loss rates, where the performance loss is measured by the increase of training time. We find that our packet loss recovery mechanism is practical, as even with 0.1% packet loss rate, the performance loss is under 3%.

5.7 Resource consumption on Switches

Finally, we evaluate the resource consumption on the switch data plane. Libra uses extra switch on-chip memory for gradient caching and float-pointing operation, and consumes the pipeline stages on switches. We deploy the OA benchmark model in Libra, and use P4i, a visualization tool offered by Intel, to observe the resource consumption.

Libra consumes 9 pipeline stages in total. In case that Libra affects the basic functionality of a switch (e.g. packet forwarding), we can utilize one recirculation to halve the the number of pipeline stages in use. In addition, Libra requires about 118KB for 30,000 hot parameters, 408.5KB for floating-point calculation, and 130KB for logic control. In total, it uses 656.5KB on-chip memory—only 3.21% of the 20MB on-chip memory in our Tofino switch. Other types of resources include VLIW instructions (37 out of 384) and hash dist units (16 out of 32).

6 DISCUSSION

Multi-tenant training. Libra can be easily extended to multi-tenant training. Specifically, we can divide the switch on-chip memory into equal-sized parts, each of which is assigned to one training task; workers and PS servers belonging to one task label their transmitted packets with a specific job ID that will be parsed by switches. Multi-tenant training tasks can share the tables used by the table-lookup mechanism for floating-point operations.

Multi-rack switches. Note that Libra can also work with multi-rack switches in data centers. Specifically, we can designate the ToR (Top-of-rack) switches with which individual PS servers connect to run Libra's two components (Libra$_p$ and Libra$_a$) for sparse gradient aggregation.

RDMA and Libra. AllReduce implementations make use of RDMA to speed up communication. The authors in [17] showed that in-network aggregation achieves better performance than the allreduce approach over RDMA, when training deep models for dense-data applications. We leave the comparison between Libra and RDMA, as well as the possibility of integrating them as one of our future works.

Encrypted traffic. Although AES encryption/decryption algorithms can be deployed on programmable switches directly [16], Libra does not consider it necessary to accommodate for encryption traffic in this paper. This is because implementing AES encryption/decryption on programmable switches will consume not
a few resources (e.g., stages and on-chip memory); Libra cannot support both sparse gradient aggregation and traffic encryption/decryption on one switch. Another possible solution is to utilize multiple switches to mitigate the limited resources, and we leave it as our further work.

7 RELATED WORK

In-network computation. With the rise of SmartNICs and programmable switch-ASICs (e.g., Tofino [9]), in-network computation emerges [53] for speed up data transmission for many applications. For example, NetCache [35] implements a key-value cache on programmable switches to process more than 2B queries/second; Beamer utilizes programmable switches to improve the performance of load balancers; Sailfish [46] proposes a cloud-scale gateway accelerated by programmable switches so that it can process dozens of Tbps traffic; AccelTCP [43] offloads complex TCP operations to SmartNICs in order to significantly improve the host stack; Jaqen [41] designs a switch-native approach for volumetric DDoS defense that can handle large-scale hybrid and dynamic attacks within seconds. Besides, in-network computation has also been recently used to accelerate distributed deep learning training via in-network gradient aggregation on programmable switches [17, 25, 50, 51]. However, these approaches target dense models and they fall short when training sparse models. Thus, this paper presents Libra whose target is to accelerate sparse model training.

Acceleration of distributed sparse DL training. NCCL [6], MPI [23] and Gloo [5] design high-performance collective communication libraries that are used to accelerate distributed DL training; RDMA [27] is adopted to accelerate data transmission with an extra in-network support (e.g., infiniband network). Other solutions reduce data transmission volume via gradient quantization or parameter synchronization. TernGrad [54] quantizes floating-point gradients into three numerical levels {-1,0,1}; Google proposes to shorten the width of each gradient to a 4-bit vector [52]. The deep model training can also be accelerated either through flow scheduling to minimize flow completion time [18, 42], or through communication scheduling to decouple the dependence between gradients and change their transmission order [48] [50]. These works accelerate the training at end host side, and are complementary to Libra. Recently, Omnireduce [22] exploits the data sparsity to improve the effective bandwidth use for distributed deep sparse training; it does not consider the highly skewed distribution of update frequency of individual parameters. Nevertheless, incorporating Libra with Omnireduce is worth further investigation.

8 CONCLUSION

In this paper, we present the design of Libra that perform in-network gradient aggregation in order to accelerate distributed sparse DL training. Overall, Libra is motivated by the key observation on the highly skewed update frequencies of parameters from industrial sparse DL models—the hot-cold phenomenon. Based on this observation, Libra offloads the aggregation of hot parameters from PS servers to programmable switches. To this end, we carefully design the solutions that include the sample-based hot parameter identification, the parameter orchestration at both switches and workers, the table-lookup mechanism to implement the on-the-fly 32-bit floating-point operations, and also two enhancements to improve the system reliability. We implemented Libra on Intel Tofino switches and integrated it with PS-lite. Extensive experiments with different sparse models have shown the superior performance of Libra. We believe our Libra paves the way towards the high-throughput distributed sparse DL system.

REFERENCES

[1] 2015. Click Prediction Dataset. https://docs.microsoft.com/en-us/archive/blogs/machinelearning/notebook-click-prediction.
[2] 2015. Microsoft Multiverso. https://github.com/Microsoft/multiverso/wiki.
[3] 2018. ITP stack. http://savannah.nongnu.org/projects/iptp.
[4] 2021. Data Plane Development Kit. https://github.com/DPDK/.
[5] 2021. Facebook, Gloo. https://github.com/facebookincubator/gloo.
[6] 2021. NVIDIA Collective Communications Library. https://developer.nvidia.com/ncccl.
[7] 2021. PS-lite platform. https://github.com/dmlc/ps-lite.
[8] 2021. Taylor series. https://simple.wikipedia.org/wiki/Taylor_series.
[9] 2021. Tofino switch. https://www.intel.com/content/www/us/en/products/network-interfaces/programmable-network-infrastructure.html.
[10] 2020. Implementing AES encryption on programmable switches from industrial sparse DL models—the hot-cold phenomenon. In Proceedings of the 2020 Conference on Empirical Methods in Natural Language Processing.
[11] 2020. Xiao, Bing Xu, Chiyuan Zhang, and Zheng Zhang. 2015. Mxnet: A flexible and efficient machine learning library for heterogeneous distributed systems. arXiv preprint arXiv:1512.02745 (2015).
[12] 2021. Xiaoqiang Chen. 2020. Implementing AES encryption on programmable switches via scrambled lookup tables. In Proceedings of the Workshop on Secure Programmable Network Infrastructure. 8–14
[13] 2014. Mosharaf Chowdhury, Yuan Zhong, and Ion Stoica. 2014. Efficient codeword scheduling with varies. In Proceedings of the 2014 ACM conference on SIGCOMM. 443–454.
[14] 2019. Penghai Cui, Heng Pan, Zhenyu Li, Jiaoren Wu, Shenghuo Zhang, Xingwu Yang, Hongtao Guan, and Gaoyang Xie. 2021. NetFC: enabling accurate floating-point arithmetic on programmable switches. In ICNP.
[15] 2021. Wei Deng, Junwen Pan, Tian Zhou, Deguang Kong, Aaron Flores, and Guang Lin. 2021. DeepLight: Deep Lightweight Feature Interactions for Accelerating CTR Predictions in Ad Serving. In Proceedings of the 14th ACM international conference on Web search and data mining. 922–930.
[16] 2022. Facebook. 2022. Writing Distributed Applications with PyTorch. https://pytorch.org/tutorials/intermediate/dist_tuto.html.
