InGaAs/InP single-photon detectors with 60% detection efficiency at 1550 nm

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InGaAs/InP single-photon detectors (SPDs) are widely used for near-infrared photon counting in practical applications. Photon detection efficiency (PDE) is one of the most important parameters for SPD characterization, and therefore increasing PDE consistently plays a central role in both industrial development and academic research. Here we present the implementation of high-frequency gating InGaAs/InP SPD with a PDE as high as 60% at 1550 nm. On one hand, we optimize the structure design and device fabrication of InGaAs/InP single-photon avalanche diode with an additional dielectric-metal reflection layer to relatively increase the absorption efficiency of incident photons by ~20%. On the other hand, we develop a monolithic readout circuit of weak avalanche extraction to minimize the parasitic capacitance for the suppression of the afterpulsing effect. With 1.25 GHz sine wave gating and optimized gate amplitude and operation temperature, the SPD is characterized to reach a PDE of 60% with a dark count rate (DCR) of 340 kcps. For practical use, given 3 kcps DCR as a reference the PDE reaches ~40% PDE with an afterpulse probability of 5.5%, which can significantly improve the performance for the near-infrared SPD based applications.

I. INTRODUCTION

Single-photon detectors (SPDs) are the most sensitive tools for weak light detection.1–6 In the near-infrared range, SPDs are extensively required in numerous applications such as quantum key distribution,7–11 long-distance quantum communication,12 and optical time-domain reflectometer.13 Currently, the practical technologies for infrared single-photon detection include superconducting nanowire single-photon detector (SNSPD),14 up-conversion single-photon detector,15 and InGaAs/InP single-photon detector.16–18 Each SPD technology has its advantages and disadvantages. For instance, InGaAs/InP SPDs are widely used in practical applications due to the features of small size, low cost, and easy operation, with a cost of relatively poor performance.19 The typical parameters to characterize InGaAs/InP SPDs include photon detection efficiency (PDE), dark count rate (DCR), afterpulse probability (Pap), maximum count rate, and timing jitter, among which PDE is one of the most important figure of merits. Commercially available InGaAs/InP SPDs exhibit a typical PDE of ~20% with a DCR of ~500 cps at 1550 nm.20–22 Recently, a miniaturized InGaAs/InP SPD with a PDE of 30% and a DCR of 2 kcps has been reported.23 As a comparison, so far record values of PDE have been achieved as high as 93% for SNSPD and up-conversion SPD, respectively.

For an InGaAs/InP SPD consisting of a single-photon avalanche diode (SPAD) and a readout circuit, PDE is defined as the probability that the SPD system produces a desired output signal in response to an incident photon, which is determined by the coupling efficiency, the absorption efficiency, and the avalanche efficiency of InGaAs/InP SPAD.24 Given a pigtailed SPAD device, the coupling efficiency and the absorption efficiency are fixed, while the avalanche efficiency highly relies on the excess bias. However, one cannot simply increase the excess bias to obtain high PDE since apart from PDE other parameters, particularly DCR and Pap, are also related with the excess bias. In practice, InGaAs/InP SPADs are operated either in free-running mode or gating mode.25 The free-running mode is suited for asynchronous single-photon detection, and so far many approaches for free-running operation have been reported.26 Nevertheless, the long hold-off time has to be applied to suppress the afterpulsing effect in such mode, resulting in a limited count rate for applications. High-frequency gating, including self-differencing,27 and sine wave gating (SWG) is an effective technique to suppress the afterpulsing effect so that the count rate of SPAD can be drastically increased. In such a scheme, the gating time is limited to a few hundreds picoseconds. As a result, the charge carrier quantity and thus the afterpulsing effect can be considerably suppressed, and meanwhile, the avalanche signals become very weak that may bring technology challenge to design readout circuit.28

In this paper, we present the implementation of 1.25 GHz sine wave gating InGaAs/InP SPDs with a PDE up to 60% at 1550 nm. We perform the structure design op-
timization of InGaAs/InP SPADs by adding a dielectric-metal reflection layer, and calibrated results on the fabricated sample SPAD devices show that the reflectivity of the dielectric-metal reflection layer to the incident photons at 1550 nm reaches ~ 80%. Further, we design and fabricate a monolithically integrated readout circuit (MIRC) dedicated to extracting weak avalanches for the scheme of 1.25 GHz sine wave gating. By optimizing the gate amplitude and operation temperature, the InGaAs/InP SPDs are characterized to achieve PDE of 60.1% at 300 K with a DCR of 340 kcps and a $P_{ap}$ of 14.8%. For practical use, the SPD exhibits significantly better performance than commercial products, e.g., ~ 40% PDE with 3 kcps DCR and 5.5% $P_{ap}$ at 253 K.

II. SPAD DESIGN AND FABRICATION

Following the approach, we perform semiconductor parameter design and optimization of InGaAs/InP SPAD based on a separate absorption, grading, charge, and multiplication (SAGCM) structure with a stepped PN junction, with an active area diameter of ~ 25 µm, as illustrated in Fig. 1a. Specifically, compared with our previous design and fabrication, a dielectric-metal reflection layer with high reflectivity is added to enhance the absorption efficiency of incident photons. Once incident photons pass through the absorption layer from the substrate region, the unabsorbed photons are reflected by the reflection layer and reabsorbed during the absorption layer, which can effectively increase the overall absorption efficiency.

The dielectric-metal reflection layer, consisting of a dielectric layer and a metal layer, is located on the top of the photosensitive region. The dielectric layer lies between the metal layer and the InP multiplication region. The material of dielectric layer is SiO$_2$, and the thickness of the dielectric layer is 220 ~ 230 nm. The reflectivity is enhanced due to the interference of reflected light between the semiconductor-dielectric interface and the dielectric-metal interface. We calculate the relationship between the reflectivity of the reflection layer and the angle of incident light at 1550 nm, and further optimize the thickness of the dielectric layer film. Fig. 1b plots the reflectivities of S-polarization and P-polarization components of the incident light as a function of incident angles, given that the angle perpendicular to the reflection layer is defined as 0°. At 0° incident angle, the reflectivities of S-polarization and P-polarization components are the same, and the average reflectivity reaches the largest value. Further, we simulate the relationship between the average reflectivity and the light wavelength given 0° incident angle, as plotted in Fig. 1c. The simulation results show that the optimal reflectivity of the dielectric-metal reflection layer to the incident photon of 1550 nm can reach 95%.

Apart from the reflection layer, the parameters of other layers are also optimized. The electric field distributions in the absorption and multiplication layers are regulated by tuning the doping concentration in the grading and charge layers. The electric field strength in the absorption layer is regulated in the range of 1 ~ 1.4×10$^5$ V/cm to guarantee the saturation drift rate of the photogenerated carriers while avoiding avalanche breakdown. The thickness of the multiplication layer is regulated in the range of 1 ~ 1.5 µm to guarantee enough electric field strength for avalanche breakdown while reducing the carrier transit time and thus the timing jitter. The total thickness of the depletion region is ~ 3 µm.

The InGaAs/InP SPAD chips are fabricated via an epitaxial process of the metal-organic chemical vapor deposition (MOCVD). During the fabrication, the background impurity concentration of epitaxial materials is reduced within the range of 2×10$^{14}$ cm$^{-3}$ and the surface charge density in the charge layer is controlled with an accuracy of 5%. The depth of PN junction is regulated with an accuracy of ±50 nm via double-diffusion process technology using a Zn source. The p-contact region, located on the top surface of the stepped Zn-doped region, is coaxial with the photosensitive region, which can achieve high reflectivity due to the reflection layer while maintaining the contact resistance as small as possible.

In order to verify the effectiveness of the reflection layer, we design and fabricate two kinds of InGaAs/InP sample SPADs with and without the reflection layer, respectively. Apart from the reflection layer, all the other structure parameters in the two cases are exactly the same. Fig. 1d plots the measured photocurrent-voltage (I-V) curves of sample SPADs in two cases, in response to incident light at 1550 nm. The photocurrents at the turning point of reach-through voltage in two cases are suited to calculate the reflectivity of the reflection layer. The small offset of reach-through voltages in two cases is due to the parameter fluctuations during the fabrication process. As shown in the inset of Fig. 1d, under the same
light illumination the photocurrents at the reach-through voltages are 1.30 $\mu$A and 1.09 $\mu$A with and without the reflection layer, respectively, which clearly indicates that the absorption efficiency and thus PDE can be relatively increased by $\sim 20\%$ with the help of adding reflection layer. Further, according to the measured photocurrent, light intensity, and absorption layer thickness, the reflectivity of the reflection layer is calculated to be $\sim 80\%$, which is less than the optimal simulation result of 95%. Such difference is primarily contributed by two factors, i.e., the imperfect flatness of the dielectric layer during the fabrication process, and incident angle deviation from 0° induced by the coupling lens.

### III. SPD SYSTEM AND CHARACTERIZATION

![Diagram of SPD system](image)

**FIG. 2.** (a) Experimental setup for SPD characterization. (b) A typical avalanche signal captured at the output of MIRC. (c) A typical detection event distribution measured by a TDC with an intrinsic deadtime of $\sim 88$ ns.

The fabricated InGaAs/InP sample SPADs are operated in the high-frequency sine wave gating mode\cite{12}. The schematic diagram in Fig. 2(a) illustrates the SPD module, calibration system, and measurement setup. One channel (Ch1) of the signal generator (SG, Keysight 81150A) generates a 10 MHz clock, which is used as the reference signal of the phase-locked loop (PLL) to generate an initial 1.25 GHz square-wave signal. After passing through a band-pass filter (BPF) with a center frequency of 1.2 GHz, the 1.25 GHz square-wave signal is transformed into a 1.25 GHz sine wave gate. The sine wave gate is further regulated with a narrow-band radio frequency power amplifier (PA) and a variable attenuator (ATT), and then is alternating current (AC) coupled to the cathode of SPAD. The amplitude of the sine wave gate can be amplified up to 30 V of $V_{pp}$ without distortion and be adjusted continuously. In such SWG scheme, due to the pure frequency spectrum characteristic of sine waves, the capacitive response signals of SPAD are only composed of sine waves with the fundamental frequency and higher order harmonics, which can be easily eliminated by bandstop filters (BSFs)\cite{33,34,31} or low-pass filters (LPFs)\cite{12,13,14}.

In the SPD system, we design a MIRC with a size of 15 mm $\times$ 15 mm to extract weak avalanche signal\cite{14}. MIRC integrates two LPFs and a two-stage radio frequency low-noise amplifier (LNA), in which each LPF has a cutoff frequency of $\sim 1$ GHz and a rejection ratio of $\sim 60$ dB at 1.25 GHz and the LNA has a gain of $\sim 40$ dB below 1 GHz. After testing with a network analyzer, MIRC exhibits radio frequency performance with a gain of $\sim 40$ dB below 1 GHz and a rejection ratio of $\sim 80$ dB at 1.25 GHz\cite{34}. MIRC is fabricated using the technology of low temperature co-fired ceramics, which is a standard printed circuit board like manufacturing process with multi-layer ceramic dielectric tapes and screen printing of conductors materials, e.g., silver, and is thus well suited for the integration of radio frequency components. Using MIRC instead of conventional readout circuits composed of discrete electronic components can minimize the parasitic capacitance around the SPAD, which, therefore, substantially reduces the afterpulsing effect. A typical avalanche signal at the output of MIRC is captured by a high-speed oscilloscope (Keysight MSOS804A), as plotted in Fig. 2(b). The rising edge of the avalanche signal is slowed down by the LPFs inside the MIRC, which contributes to the timing jitter of the SPD system. The output signals of MIRC are further discriminated by a high-speed comparator. The threshold of the comparator is chosen to be the value as small as $\sim 15$ mV to ensure that no signals are discriminated given the bias below the breakdown voltage. The intrinsic deadtime of the SPD system is limited by the discrimination and monostable circuits, i.e., $\sim 3$ ns.

We then follow the single-photon calibration scheme\cite{12} to characterize the primary parameters of InGaAs/InP SPDs. The second channel (Ch2) of SG generates a clock of 625 kHz to drive a picosecond pulsed laser diode (LD, QuantumCTek QCL-102). The optical pulses emitted from the LD at 1550 nm with a full width at half maximum (FWHM) of 50 ps pass through a 99:1 beam splitter (BS), in which the 99% port is monitored by a power meter (PM, EXFO IQS-1600) and the 1% port is connected with a variable optical attenuator (VOA, EXFO IQS-3150). The intensity of laser pulses is attenuated down to a level of mean photon number per pulse of 1. The synchronized signals of Ch2 and the output signals from the discriminator are fed into a time-to-digital converter (TDC, PicoQuant picoharp 300) with an intrinsic deadtime of $\sim 88$ ns as “start” and “stop”, respectively. TDC performs a timing tag for each detection event and transmits data to a personal computer (PC). Fig. 2(c) plots a typical histogram of detection event distribution.

With such measurement settings, the primary parameters of InGaAs/InP SPDs can be calculated. Considering the Poisson distribution of laser source, PDE can be calculated as\cite{12}

$$PDE = \frac{1}{\mu} \ln \frac{1 - R_d/ f_g}{1 - R_{ph}/ f_l},$$  \hspace{1cm} (1)$$

where $\mu$ is the mean photon number per laser pulse, $R_d$ is the measured count rates without laser illumination, $f_g$ is the gating frequency, $f_l$ is the laser repetition frequency, and $R_{ph}$ is the photon detection count rate with laser illumination, i.e., the coincidence rate between detections and laser pulses after subtracting the DCR contribution. The normalized DCR, which is usually used for fair comparison in different conditions, can be calculated as $R_d/(f_gt_w) \times 10^9$, where $t_w$ is the effective gating width\cite{12}. From the detection event distribution, $P_{ap}$ can
be calculated as
\[ P_{ap} = \frac{R - R_{ph} - R_d}{R_{ph}}, \]
where \( R \) is the total count rate with laser illumination.

IV. RESULTS AND DISCUSSION

Two InGaAs/InP SPDs based on sample SPADs, i.e., SPAD #1 and SPAD #2, are characterized. In the SWG scheme, gate amplitude and operation temperature are the most important factors for performance optimization. First, SPAD #1 is characterized at a fixed operation temperature to investigate the effect of gate amplitude. Fig. 3a plots the normalized DCR as a function of PDE with gate amplitudes varied from 8.0 V to 23.0 V at 273 K. At each point, \( t_w \) is measured by scanning the relative delay between laser pulses and sine wave gates. For instance, the inset in Fig. 3a shows a typically measured result and the fitting curve with 20.4 V \( V_{pp} \) and 50% PDE. From Fig. 3a, one can clearly observe that the lines of normalized DCR versus PDE with \( V_{pp} \) from 8.0 V to 20.4 V overlap each other, which indicates that the normalized DCR-PDE trend is independent of the gate amplitude in such range. The case with 23.0 V \( V_{pp} \) is exceptional, and particularly in the region of >50% PDE the normalized DCR is abnormally high. This is probably due to the fact that gating width is too narrow to produce avalanches with enough signal-to-noise ratio in such case.

In addition, gate amplitude significantly affects the relationship between \( P_{ap} \) and PDE, as illustrated in Fig. 3b. Given a certain PDE, \( P_{ap} \) distinctly decreases as gate amplitude increases. Such effect is due to that for the same excess bias \( V_{ex} \), or PDE, higher gate amplitude results in smaller effective gating width and thus less charge carrier quantity of avalanche\(^{12}\). As a consequence of the afterpulsing effect suppression, the maximum achievable PDE is also promoted with an increase of gate amplitude.

Then, we investigate the relationship between operation temperature and performance optimization. Fig. 4a and Fig. 4b plot the parameters of normalized DCR and \( P_{ap} \) as a function of PDE at different temperatures for SPAD #1 and SPAD #2, respectively. At each temperature, the gate amplitude is optimized. From Fig. 4 one can observe that with an increase of operation temperature \( P_{ap} \) apparently decreases given a fixed PDE, due to short lifetimes of trapped carriers at high temperatures. More interestingly, the maximum achievable PDE also increases with temperature. On one hand, the absorption coefficient of InGaAs and thus the absorption efficiency of incident photons increases with an increase of temperature\(^{35}\). On the other hand, as the temperature increases the breakdown voltage and the gap between the breakdown voltage and the reach-through voltage of SPAD enlarge as well\(^{39}\), which means that it is possible to apply enough high bias voltage to achieve the highest PDE only in the regime of high operation temperature. At 303 K the maximum achievable PDE of SPAD #1 reaches 58.4% with 542 kcps DCR (1172 kcps normalized DCR) and 16.4% \( P_{ap} \), while at 300 K the maximum achievable PDE of SPAD #2 reaches 60.1% with 340 kcps DCR (744 kcps normalized DCR) and 14.8% \( P_{ap} \). For practical use, the SPD exhibits significantly better performance than commercial products, e.g., \( \sim 40\% \) PDE with 3 kcps DCR (14.5 kcps normalized DCR) and 5.5% \( P_{ap} \), at 253 K using SPAD #2.

V. CONCLUSION

In conclusion, we have reported a high-frequency gating InGaAs/InP SPD with a PDE up to 60% at 1550 nm. By performing structure design optimization with a dielectric-metal reflection layer, the absorption efficiency of SPAD is significantly enhanced. A monolithic read-out circuit of avalanche extraction for 1.25 GHz SWG scheme is also designed to suppress the afterpulsing effect due to parasitic capacitance. We have then optimized the conditions of gate amplitude and operating temperature to achieve a PDE as high as 60%, with 340 kcps DCR and 14.8% \( P_{ap} \). For practical use, the SPD exhibits \( \sim 40\% \) PDE with 3 kcps DCR and 5.5% \( P_{ap} \), which can considerably improve the performance of diverse applications requiring InGaAs/InP SPDs for near-infrared
single-photon detection.

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