Open standards for automation of testing of photonic integrated circuits

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Open Standards for Automation of Testing of Photonic Integrated Circuits

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(Invited Paper)

Abstract—Foundry services for photonic integration enable access to such technologies and facilitate fab-less businesses models. The technologies are sufficiently mature for proof-of-concept demonstrators, advanced prototypes, and two-medium small-volume production. Further improvement of the technology processes behind those services requires extensive research and development efforts in order to advance the foundry offerings and assure scalability, process control, and the yield required for volume production. A high-level automation of test and assembly processes in the PIC manufacturing chain is essential to improve statistical process control and scalability of all processes. These allow for early known-good-die identification, optimization of fabrication process window, improved yield, and volume production. In this paper we propose a standardized approach to chip layout that supports automated test and assembly processes already at the design phase. Moreover, we describe a modular test software framework based on open standards. Within this test framework, standard file formats for chip, equipment, and measurement description, and the open file formats for storage and exchange of data are described. This test framework is a part of the openEPDA initiative and enables test automation, user-defined testing, data analysis, exchange-ability, and traceability across the full manufacturing chain from design to product.

Index Terms—Photonic integrated circuits, photonic integration, test, test automation.

I. INTRODUCTION

PHOTONIC integrated circuits (PICs) offer numerous advantages over their counterparts based on discrete components and bulk optics. A large degree of integration results in reduced footprint, improved stability and reduced energy consumption [1]–[3]. PICs are readily present in solutions for telecommunication networks [2], [4]–[8], but also increasingly attract attention of other domains. Emerging areas of applications include data-center networks [9], sensing [10], [11], wireless communications, millimeter and terahertz [12]–[14], cryptography [15], [16] and quantum computing [17]–[19]. This widening range of applications of photonic ICs can be attributed to an increased availability and accessibility to photonic integration technologies via open access foundry services that are based on standardized, generic processes [1], [3], [20]. A number of photonic integration technology platforms using different material systems is available in photonic foundries [21]–[25]. The maturity of the processes behind allows for fabrication services to be offered on a commercial basis. Most of the foundries provide access to their generic integration technology via multi-project wafer (MPW) runs [3], in addition to providing customer specific, dedicated fabrication services. The MPW runs enable a seamless path to design and fabrication of application specific photonic integrated circuits (ASPICs), Fig. 1. Such photonic foundries call for the emergence of other services at different points of the PIC manufacturing chain, as schematically depicted in Fig. 2a. A large variety of electronic-photonic design automation (EPDA) tools is available from several vendors [26]–[29]. Software packages support creation of layout and provide tools for simulation at the component and circuit level. The availability and functionality of process design kits (PDKs) for the main technology platforms continuously increases. Offerings from design houses and packaging service providers complete the manufacturing chain from an idea to module, see Fig. 2a. The increasing maturity of the EPDA tools, PDKs and generic technology processes allows for the development of proof-of-concept demonstrators, advanced prototyping and small-to-medium volume production.

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Fig. 1. Application specific photonic integrated circuit designed using a standardized layout and fabricated in a generic integration process. (a) Layout of a PIC for validation of an automated die tester. (b) Microscope image of the InP chip fabricated in an MPW run at SMART Photonics.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.
Despite those advantages, many of the technology processes and tools in the manufacturing chain of PICs require substantial improvements in terms of standardization at the design [20], the front-end fabrication [30], and the back-end processes [31]. In addition, an increased level in automation of test, assembly and packaging processes is necessary [32]. These processes have been identified as the three main contributors to the overall cost of PIC-based product manufacturing, reaching around 80% of the total cost of a module based on an InP chip, Fig. 3, [33], [34]. The fraction of the cost of testing on its own can be as high as 29% due to its spread across the full value chain, Fig. 2b. The performance of a fabrication process has to be validated for every run, as well as the performance of every fabricated device. Testing performed at different stages of the fabrication (Fig. 2b) pursues different objectives. On-wafer testing during and after the fabrication is done for process qualification. Bar and chip testing is first run by the foundry for building block qualification, and later can be done for measuring circuit-level performance. This is frequently overlooked, particularly in fragmented manufacturing eco-systems, and has led to underdevelopment in testing, which affects other processes. Consequently, such manufacturing chains suffer from lack of standardization and automation of test both in the software and hardware layers for data collection and storage. This results in limited exchangeability, interoperability and traceability of data as well as difficulty in collection of statistically significant data sets. The latter are compulsory for adequate statistical process control (SPC) and for optimization of process windows. Data feedback across the manufacturing chain allows for development of correlations between different process steps and enables early identification of known-good-dies (KGD). Process variation data, as well as functional characterization of basic components and circuits will enrich compact models in PDKs and increase the functionality of EPDA tools. Ultimately, increased research and development efforts to improve test processes are needed in order to reduce the cost and to improve scalability and yield, which enable volume production.

In this paper we propose a standardized approach to PIC layout enabling access to automated testing and generic assembly and packaging services [35]. To satisfy the increasing demand in data amount, quality, and traceability our approach incorporates a framework for measurement automation and data handling, openEPDA [36]. The proposed concept is to interface the photonic integrated circuit designers who define the test protocol during the design stage with the test facilities. This is achieved through a modular approach to the test infrastructure, which enables automation of the process and at the same time allows the user to define measurement procedures and their parameters. In the following section we also introduce an open data format which is used to store heterogeneous measurement data together with the experiment metadata, and is compatible with the openEPDA framework. In the last section we demonstrate a practical implementation of the standardized layout and openEPDA framework in a semi-automated die test system. The
edges of the die may be necessary, e.g., due to the and or PEN south and west and south side of a chip. The layout should also T µ north and north west or at both sides of the PIC. The layout should also is carried out according to a user-defined test sequence.

II. STANDARDIZED LAYOUT TEMPLATES

In order to enable automation of the test and assembly processes, a set of standard conventions and design rules regarding layout of PICs has been defined in line with the framework of the PIXAPP pilot line [35] as presented in Fig. 4.

Standardization of layout templates will greatly benefit customers with low and mid volumes as well as the automated test and assembly tooling vendors. In the first case by lowering the entry barrier for production of PIC modules and in the latter by enabling development of modularized and standard tooling.

The scope of the definitions covers naming and allowed positions of electrical and optical input/output (IO) ports, die orientation aspects, placement of fiducials supporting test and assembly process automation, and limitations imposed on the design area taking into account back-end processes and automated testing.

The die orientation should be clearly marked, e.g., with a compass rose with the directions being referenced as north, south, east and west, as presented in Fig. 4. Optical ports should be placed on either east or west, or on both, should a transmission measurement be carried out. In all cases, a clearance from the north and south edges of the die may be necessary, e.g., due to the placement of the electrical pads. In this particular example, we considered edge optical coupling. For vertical optical coupling through grating couplers, as commonly used in membrane and silicone photonic circuits, design rules adapted to that situation can be implemented.

Depending on the assembly process, there may be additional design rules for the placement of the optical ports. The electrical ports can be placed on all sides of a die while placement of optical and electrical IOs on the same side is not allowed. In addition to allowed positions, the electrical contacts have to respect clearance sections resulting from an overspray of coatings and/or assembly processes e.g., fiber attach or wire-bonding. The naming format of the IO ports indicates the type of the port, its location on the die, and a number in a group. Having standard names and locations will facilitate the communication between designers, testers and packaging partners. The label ‘dc’ (low frequency) or ‘rf’ (higher frequency) indicates electrical ports that can be located at north, east, south and west side of a chip. The ‘io’ prefix indicates optical ports that can be located either at east, west or at both sides of the PIC. The layout should also include at least two fiducials that allow to position a die in three dimensions (in-plane position and angle) in a unique way, to support automation of the test and assembly process. More fiducials can be added for redundancy. The shapes of fiducials should be tolerant for the fabrication errors and defined in the layers that are fabricated with most accurate process steps. Two examples of the possible shapes (bars with crosshair and three discs) are presented in the Fig. 4. In addition, size, spacing (pitch) and type of the contact pads are defined within those allowed by a particular fabrication technology. An example of standard layout of electrical dc pads with all relevant dimensions indicated is shown in Fig. 5.

Implementation of those standards in EPDA tools in the form of assembly design kits (ADK) allows to take test and packaging aspects into account at an early design stage [26]–[29]. An example of implementation of such a standardized template for the design of a PIC for the automated die tester development and a microscope image of a fabricated chip is shown in Fig. 1.

While designing the mask layout, the EPDA tools will produce a chip description file (CDF). The CDF includes the type, label, and coordinates of all electrical and optical input-output ports and of the fiducials that can aid automation of the measurement and assembly processes.

III. OPEN TEST FRAMEWORK

The primary objective for the test framework is to decouple the software control of the test equipment hardware, run by the test facility, from the test settings provided by a PIC designer. This is done with standardized software APIs that link well-defined tasks with a configuration file provided by the user that uniquely specifies the tasks to be carried out. In addition, a configuration
A data landscape is essential for the design, fabrication, and testing of PICs. The data generated during the measurements is used for different purposes: pass-fail procedure, process control, device model development, and calibration. This involves various parties, such as the foundry, measurement labs, designers, and software companies which use different tools to generate and process the test data. Therefore, the generated data comes from different sources and can be heterogeneous. The experimental data is obtained from the measurement equipment directly when a measurement or observation is performed. It is usually numeric data in the form of scalars or arrays. The identifiers of the wafer, die, and observation is performed. It is usually numeric data in the form of scalars or arrays. The identifiers of the wafer, die, and circuit under test represent some of the metadata for the given observation. Metadata may also include the information regarding the equipment used, particular settings, date of calibration, ambient conditions, etc. The metadata can be of various types, for example simple numeric or textual data, or structured as arrays or maps. An overview of the datatypes is presented in the Table I.

To summarize, the described above data landscape sets several requirements to the data format to be used for representing the data. It should be able to store heterogeneous unstructured metadata together with potentially large arrays of numeric measurement data. The format should be both human- and machine-readable and self-explanatory.
TABLE I
EXAMPLES OF DATA TYPES

| Data type | Description | Examples | Remarks |
|-----------|-------------|----------|---------|
| Number    | Any numeric value | 2.3 .inf 1.9e-3 | Representation is same as defined in section 10.2.1.4. of [32] |
| String    | A list of characters | spectrum analyzer’ ’SPM18-3’ | |
| Array     | A sorted list of string values | [1, 2, 3, 4] [west, ’east’, ’north’] | Values may have mixed types, which is discouraged. Also called a named array, a look-up table, or a dictionary. |
| Map       | Mapping of a set of values to another set of values in the key: value form. | (’wafer’, ’SPM18-3’, ’die’, 38X23’, ’design’, ’SP00-38’) | |

B. Standardized File Format

We have developed a standard file data format, which satisfies the abovementioned requirements. The file format only describes the syntax of the data file (how the data is stored), and does not define any data schema (what is stored). This format is sufficiently flexible to include any arbitrary structured data, including arrays and maps. The generated files are human-readable and are straightforward to be imported by any software or analysis tool. The proposed data exchange file format has the following structure. The first line is a format identifier with a version number, “#openEPDA DATA FORMAT”. After this, the data part follows, which contains two sections. The first section adheres to the YAML format [38] and contains all scalar (numeric and textual) data in a “name: value” form. This format is applicable for storing all previously mentioned types of the data. The second section is a CSV-formatted [39] part to store the tabular measurement data. This is suitable for most common data, and can be imported in nearly all existing software. In those occasions when the CSV format would not be adequate, or when large binary data need to be included, the YAML section can be extended to contain a reference to an external file.

The proposed format defines how to write the information into the file. Besides this, the YAML section contains reserved keys which start with an underscore symbol. At this moment, “_openEPDA_version” and “_timestamp” are the two required keys, which describe the version of the data file and the time the data was created respectively. In future, other reserved key may be defined.

An example of (part of) a measured optical spectrum is shown in Fig. 7. Line 1 specifies the file format. Lines 2 to 14 contain metadata in YAML-format, two of which (lines 2 and 3) provide values for the two required keys. In the example, only string and float data types are used, however arrays and maps can also be included. Line 15 contains a standard document-end marker. Lines 16 to the end of the document contain the CSV-formatted tabular data with a single header line.

V. SEMI-AUTOMATED DIE MEASUREMENTS

As a demonstration of the proposed design, data, and test description standards, we present a test case with a measurement defined according to these standards and performed on an automated setup.

A photograph of the chip that was characterized is shown in Fig. 8. It was fabricated in an InP active-passive MPW run by Smart Photonics [21], and its layout is designed according to the description presented in Section II, with a single row of electrical contacts. It contains two groups of 2 × 2 3-dB MMI couplers [40], which are each referred to as a Device Under Test (DUT). The first group of couplers, 30 in total, has input waveguides implemented in a shallow (low contrast) cross-section [3]; the second group contains 20 couplers with input waveguides in the deep (high contrast) cross-section. All MMI couplers have variations in their geometric design parameters, such as MMI region width, width of input waveguides, taper length. For each coupler, 4 combinations of input (1, 2) and output (3, 4) waveguides for...
each polarization have to be measured to characterize coupler’s performance: transmission 1–3, 1–4, 2–3, 2–4. Each combination of input and output for a given MMI coupler represents a single measurement, resulting in 120 and 80 measurements for the MMI couplers with shallow and deep inputs respectively.

Besides DUTs, the chip contains straight waveguides, which are used to reference the chip coordinate system with the positioning stage coordinate systems: 2 in the south part of the chip, $2 \times 5$ in the middle, and 2 in the north part. The reference waveguides in the south and north part contain an integrated SOA for ease of alignment: when forward biased, they generate an optical signal in the waveguide, which enables easier and independent alignment of the input and output waveguides. This is significantly simpler as compared to the “passive” alignment, when no light is generated or detected on-chip, in which case both input and output fibers have to be coupled to the waveguide simultaneously.

A simplified schematic of the measurement setup is shown in Fig. 9. For InP-based technologies, edge coupling though cleaved chip facets is typically used. To reduce the fiber mode size for better matching with the waveguide mode, a lensed polarization maintaining fiber is used in the setup. In the experiments, a broadband light source connected to the input side of the setup and a power meter measuring the output optical power were used.

Before the automated measurement can start, a mapping of the stage and chip coordinates has to be done. This is performed by aligning both input and output fibers sequentially to one reference waveguide in the south and one in the north part of the chip. Full automation of this mapping step is foreseen in the next release of the test framework. After each alignment, stage and chip coordinates have to be done. This is performed by aligning both input and output fibers sequentially to one reference waveguide in the south and one in the north part of the chip. Full automation of this mapping step is foreseen in the next release of the test framework. After each alignment, stage and chip coordinates were calculated using the transformation matrix calculated on the calibration step. Realignment was done by iteratively adjusting the position along 6 axes (3 orthogonal axes per side) using the signal from the power meter as a feedback. With edge coupling, the power transmission coefficient is described by theory of overlapping Gaussian beams [41] in first approximation, which means that an optimum fiber tip position exists for all three axes. Finally, the measurement itself consisted of taking a power meter readout at the optimized coupling position.

We have performed a transmission measurement of 30 MMI couplers with shallow inputs. The measurement was done in three sessions ($s = 1..3$), each consisting of 120 single measurements ($n = 1..120$), resulting in 360 power values $P_{n,s}$. All measurements were done on the same chip. The chip placement did not change between the sessions, however the reference waveguide calibration was done independently for each session.

The first session was used as a reference for comparison with the other two sessions. For each measurement $n$, we used the transmission from the first session $P_{n,1}^\text{ref} = P_{n,1}$ and calculated the power difference for other two sessions:

$$\Delta P_{n,s} = P_{n,s} - P_{n,1}^\text{ref}$$

where $n$ is the measurement index, and $s = 2, 3$ is the session index. The histogram of the obtained values $\Delta P_{n,s} (s = 2, 3)$ is presented in Fig. 10. The plot shows the number of measurements for which a particular power difference from the reference power $\Delta P_{n,s}$ was measured. The standard deviation of the power difference is $\sigma_{\Delta P} = 0.012$ dB (see inset of Fig. 10), which shows a very good repeatability of the positioning and realignment procedures. Fig. 10 also shows a small number of outliers, with power difference reaching $-31$ to $-34$ dB. This may happen when the initial alignment is offset from the optimum position by more than $5 \mu m$. There are local maxima and accidentally automated realignment algorithms finds these maxima instead of global maximum. This pattern is similar for every measurement, which explains the small spread of power values: $-31$ to $-34$ dB below the optimum coupling. Although the power difference is disruptive for DUT characterization, we
clearly recognize these outliers and found a reliable way to avoid them in an updated alignment procedure.

To quantify the fiber tip positioning repeatability, we have measured the transmitted power dependency on the offset from the optimum coupling position. The plots are shown in Fig. 11. Fig. 11a shows measured and fitted power for three axes: lateral, vertical, and focus corresponding to x, y, and z directions in Fig. 9. As described in [41] the fitting was done to a Gaussian function in the vertical and lateral directions, and to a Lorentzian function in the focal direction. For the focal direction, two different widths of a Lorentzian function were used for offsets below and above 0 μm. Fig. 11b shows a zoom of the fitted curves and a dashed line showing the 0.02 dB margin from the maximum of each curve. From the fit for a given margin of 0.02 dB, a maximum total range of the fiber tip position near the optimum can be calculated: 0.13 μm, 0.19 μm, and 0.76 μm for vertical, lateral, and focal directions respectively.

VI. CONCLUSION

A standardized approach to PIC layout that enables developments of generic and automated processes for test, assembly, and packaging has been proposed. The generic assembly and packaging services are very well suited for prototyping and low volume manufacturing [35], [42], [43]. Layout standardization allows for increased automation of the technology processes at front-end and back-end. It enables and eases scaling to volume production. However, at a certain volume threshold at individual businesses, one will likely require customization in order to optimize the overall efficiency and cost. Furthermore, the standardized layouts allow for testing automation at different points of the manufacturing chain, at die, bar and wafer levels. In order to handle the test process and data generated, we introduced the openEPDA modular test framework and standardized data formats, which are available for everyone to implement and can enable easy exchange of measurement specifications and data exchange between various partners. Both standardization and modular framework have been validated in a semi-automated test environment, showing a clear advantage in terms of reliability and reproducibility of the achieved results. If deployed on fully automated and speed optimized hardware they will facilitate high throughput testing. These will benefit statistical process control for improvement of the manufacturing processes, enrich EPDA tools and enable design-for-test and first-design-right methodologies and lead to the reduction of the costs associated with the test.

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