Considerations for neuromorphic supercomputing in semiconducting and superconducting optoelectronic hardware

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Abstract

Any large-scale spiking neuromorphic system striving for complexity at the level of the human brain and beyond will need to be co-optimized for communication and computation. Such reasoning leads to the proposal for optoelectronic neuromorphic platforms that leverage the complementary properties of optics and electronics. Starting from the conjecture that future large-scale neuromorphic systems will utilize integrated photonics and fiber optics for communication in conjunction with analog electronics for computation, we consider two possible paths towards achieving this vision. The first is a semiconductor platform based on analog CMOS circuits and waveguide-integrated photodiodes. The second is a superconducting approach that utilizes Josephson junctions and waveguide-integrated superconducting single-photon detectors. We discuss available devices, assess scaling potential, and provide a list of key metrics and demonstrations for each platform. Both platforms hold potential, but their development will diverge in important respects. Semiconductor systems benefit from a robust fabrication ecosystem and can build on extensive progress made in purely electronic neuromorphic computing but will require III-V light source integration with electronics at an unprecedented scale, further advances in ultra-low capacitance photodiodes, and success from emerging memory technologies. Superconducting systems place near theoretically minimum burdens on light sources (a tremendous boon to one of the most speculative aspects of either platform) and provide new opportunities for integrated, high-endurance synaptic memory. However, superconducting optoelectronic systems will also contend with interfacing low-voltage electronic circuits to semiconductor light sources, the serial biasing of superconducting devices on an unprecedented scale, and cryogenic infrastructure.

1 Introduction

The foundations of cognition remain a great frontier of science, with potentially enormous ramifications for technology and society. A hardware capable of simulating spiking neural networks with the scale and complexity of the brain or even beyond could be a powerful tool in deciphering this enigma. Achieving such large-scale systems has proven to be non-trivial with established CMOS hardware [1]. A significant challenge will be to enable efficient communication with low-latency amongst billions or trillions of neurons. Optics appears well-matched to the task, as the lack of resistive, capacitive, and inductive parasitics makes optical links more amenable to high fan-out than electrical interconnects [2]. While digital systems partially circumvent this issue by leveraging time-multiplexing to artificially increase fan-out [3], multiplexing introduces latency that scales exponentially above a certain data load [4]. Optical interconnects may enable direct connections between neurons which would eliminate all traffic-induced delays and support larger, faster, and more interconnected networks. However, while the lack of interaction between photons is beneficial for reducing parasitics during communication, it is a detriment to computation. Electronic circuits are better suited to implement complex, nonlinear neuronal functions. It is reasonable to anticipate performance gains from optoelectronic neural systems leveraging optics for communication and electronics for computation, provided the hardware can be realized.

Our proposal to fabricate a direct, physical connection between every pair of connected neurons is known as the fully dedicated axon approach to communication [5]. While this strategy requires largely fixing network topology in hardware—a chief disadvantage when compared with highly reconfigurable digital systems—the reduced overhead and elimination of communication bottlenecks will greatly benefit performance. We further specify that all synapses, dendrites, and neurons utilize fully dedicated electronic circuits, so that each element of hardware has a one-to-one correspondence with its information-processing role in the neural system. This fully dedicated approach is advantageous if one aspires to create a diverse array of synaptic and dendritic behaviors at each neuron, as observed in biological neural systems [6, 7]. For instance, a different time constant or plasticity mechanism could be implemented at every synapse on a single neuron. Perhaps more importantly, fully dedicated components eliminate the auxiliary hardware required to perform multiplexing operations. Further, performing synaptic weighting and temporal dynamics in the electronic domain allows for binary optical communication, which minimizes the amount of optical energy per spike and reduces noise incurred by
Figure 1: An abstract schematic of the class of optoelectronic neurons meeting our three criteria. Each synapse ($S_e$ and $S_i$ for expiratory and inhibitory synapses respectively) is implemented with a physical circuit block containing a detector and a temporal filter. The detector produces an all-or-nothing electrical pulse upon receipt of an optical spike which is then processed by the filter. The parameters of the filter (time constant, weight, etc.) can be set individually for each synapse. A local weight update circuit (W) implements plasticity mechanisms at each synapse. Synaptic outputs are integrated in the soma (N) which drives an optical transmitter to downstream connections upon reaching threshold.

The scope of this paper is therefore limited to networks meeting these three conditions:

1. Direct, optical connections are utilized for communication between neurons (fully dedicated axons).

2. Optical communication is binary. The amplitude of the optical signal carries no information.

3. All synaptic, dendritic, and somatic computations are performed by fully dedicated electronic circuits.

With these conjectures established, a picture of the hardware under consideration begins to emerge. There is a single optical transmitter at each neuron. This light emitter produces a short pulse of light each time the neuron spikes. The optical pulse is coupled into a waveguide, and optical power is tapped from the waveguide for each downstream synapse. Each synapse contains a photodetector which registers an all-or-nothing synapse event. From there, all synaptic weighting, spike-train filtering, dendritic processing, signal summation, neuronal thresholding, and plasticity mechanisms are implemented in the electronic domain with tailored integrated circuits.

A schematic of this general framework is shown in Fig. 1.

There are potentially multiple ways to physically implement this model. The remainder of this paper will discuss two possible implementations—a superconducting platform and a room-temperature all-semiconductor system. The superconducting platform, known as SOENs (Superconducting OptoElectronic Networks) is discussed in prior work [2,8–10]. In short, optical links are formed from semiconductor light sources and superconducting nanowire single photon detectors (SNSPDs). Computation is performed with analog Josephson junction (JJ) circuits and memory is implemented with persistent current in superconducting loops. The semiconductor implementation is imagined as an exact analogue of the SOENs platform, except without the benefits (or limitations) of cryogenic elements. Traditional photodiodes enable optical communication, analog CMOS circuits provide computation, and emerging memory devices provide synaptic memory.

This paper seeks to analyze the suitability of both platforms for implementing large-scale optoelectronic neuromorphic networks. Despite limiting our discussion only to architectures meeting our three conjectures, there remains a vast space of design choices, making it difficult to draw hard-and-fast conclusions. Nevertheless, interesting guidelines can be obtained by analyzing limits of technologies most likely to be used in each platform. Important benchmarks for device performance are also identified, which may be of use in monitoring the development of this field.

2 Communication

2.1 Optical Receivers

We begin analysis of optical interconnects with receivers. There are two ways the receiver influences the power bud-
get of an optical link: (1) The receiver (and the electrical components it must produce) sets the minimum optical signal that must be produced by the light source, and (2) the receiver may require electrical power of its own to run. It is found that the energy per spike may be quite similar in both platforms once cooling is accounted for in the superconducting case. However, the optical power required from light sources is reduced by a factor of 1000 in the superconducting case, at least when compared to the semiconductor receivers of comparable total efficiency, which omit transimpedance amplifiers [11].

### 2.1.1 Superconductor Receivers

As stated previously, the SOENs platform utilizes SNSPDs to detect optical signals as faint as a single photon. Physically, an SNSPD is a superconducting nanowire biased with a current source \( I_{\text{spd}} \approx 10 \mu\text{A} \). The simple structure makes fabrication and waveguide integration straightforward [12–19]. Photons travelling through a waveguide evanescently couple to a nanowire on the surface of the waveguide. A single photon has enough energy to drive the nanowire from the superconducting phase to a resistive state. In SOENs receivers, this momentarily redirects the bias current along an alternate conduction pathway that activates a JJ circuit to register the synapse event and conduct further synaptic processing (Fig. 2(a)).

While an SNSPD itself dissipates zero static power, electrical power is still required for superconducting receivers. Current biases will require some power, but should be shared by many devices (Sec. 3), ameliorating the cost. More important is dynamic electrical power consumption associated with detection events. The nanowire has an inductance, \( L_{\text{spd}} \), that stores energy from the current bias. During a detection event, this energy is dissipated in the resistor \( r_{\text{spd}} \). The electrical energy necessary to detect each photon is then \( \frac{1}{2} L_{\text{spd}} I_{\text{spd}}^2 \). \( L_{\text{spd}} \) can be as low as 100 nH, resulting in an electrical energy consumption \( (E_{\text{spd}}) \) of around 5 aJ/spike.

Since an SNSPD is capable of detecting single photons, it will operate near the quantum limit of optical communication [20]. We assume that the detection of a single photon will be treated as the registering of a synaptic event. The probability of a light source producing a spike with a certain number of photons within a fixed time window is given by a Poisson distribution. We will also conservatively assume a detection efficiency \( \eta_D \) of 70\% (higher detection efficiency is certainly possible [21, 22]). The probability of measuring zero photons during a spiking event is then given by:

\[
P(0) = \sum_{k=0}^{\infty} \frac{N_{ph}^k e^{-N_{ph}}}{k!} (1 - \eta_D)^k = e^{-N_{ph} \eta_D},
\]

where \( N_{ph} \) is the average number of photons per spiking event. Neural systems are known for remarkable robustness to and even utilization of noise [23, 24]. Detecting only 99\% of spikes may be tolerable and would still represent a significant improvement over biology, wherein synapse reliability is typically in the range of 5\% - 80\% [25, 26]. From Eq. 1, this would correspond to roughly 7 photons (0.9 aJ for \( \lambda = 1.5 \mu\text{m} \)) needed to reach the receiver. The total number of photons produced by the source will need to be higher to account for energy losses in the link. The total optical energy per spike, \( E_{\text{opt}} \), will be:

\[
E_{\text{opt}} = \frac{N_{ph} h \nu}{\eta}.
\]

\( h \nu \) is the energy of a single photon and \( \eta \) is the total energy efficiency of the optical link. \( \eta \) includes all optical losses and the inefficiency of the transmitter. This efficiency factor will be highly dependent on the specifics of the platform, but for now we will leave it as a free variable. The total power consumed by the optical link is the sum of \( E_{\text{opt}} \) and \( E_{\text{spd}} \). Accepting a 1\% error rate, these two contributions to the total energy will be roughly equal when \( \eta = 20\% \). Such a high efficiency is likely near the limits of physical possibility. For more realistic values of \( \eta \), \( E_{\text{opt}} \) will dominate.

Importantly, superconducting electronics come with a cooling overhead (Sec. 5). We conservatively assume that every watt of power produced at low temperature will require 1 kW of refrigeration power. System-level effective optical energy per spike for superconducting links will be no less than 1 fJ.

Fabrication of waveguide-integrated SNSPDs has become commonplace in recent years [12–19]. SNSPD materials include NbN, NbTiN, WSi, and MoSi. Superconducting films (3 nm - 10 nm) can be sputtered at room temperature atop many substrates and patterned into wires from 50 nm to 5 \( \mu \)m wide using conventional lithography and etching. Multiple planes of SNSPDs have also been demonstrated [27]—a promising development for future large-scale neuromorphic systems (Sec. 5). Waveguide-integrated NbN SNSPDs can reach photon count rates exceeding 1 GHz [28, 29]. However, slower detectors, such as MoSi and WSi SNSPDs with 20 MHz count rates, have demonstrated the best yields to date (99.7\% [30]). Previous statements that SOENs were limited to 20 MHz were motivated by these pragmatic concerns about the current state of fabrication [2].

### 2.1.2 Semiconductor Receivers

While semiconductor receivers are the predominant technology for long-distance optical communication, intrachip optical receivers deviate significantly from their long-distance counterparts, as traditional transimpedance amplifiers likely consume too much electrical power, despite impressive optical sensitivities. This has led to the proposal of “receiverless” designs that omit amplifiers altogether [11]. Receiverless communication uses a photodetector to directly drive the input of CMOS gates. Photons produce electron-hole pairs in the photodetector, which in
It is reasonable to consider values for CMOS gate capacitance, and any wiring capacitance. For 0.8 V, the receiver to reset. In principle the resistor is unnecessary if an optical reset is used as described in [31]. The resistor would increase the minimum optical power necessary to register a spike and limit the bandwidth of the receiver.

With optical link efficiency \( \eta \), the necessary optical energy required to drive the receiver to a voltage \( V \) is [11]:

\[
E_{\text{opt}} = \frac{C_{\text{tot}} V}{\eta R}. \tag{3}
\]

\( R \) is the responsivity of the detector, typically of order 1 A/W. \( C_{\text{tot}} \) includes the photodiode capacitance, the CMOS gate capacitance, and any wiring capacitance. It is reasonable to consider values for \( C_{\text{tot}} \) at the femtofarad level. For 1.5 µm photons and a required voltage swing of 0.8 V, \( E_{\text{opt}} \approx 0.7 \) fJ (5000 photons) for unit efficiency. This is similar to the superconducting case, except cooling is considered. If two optical communications links were identical in all measures (source efficiency, optical losses, etc.) except one was cooled to 4 K with SNSPDs and the other operated at room-temperature with photodiodes, then communicating a spike would cost nearly the same energy at the system level in each link. The power required for cryogenic cooling pays for itself with reduced light levels in the optical link. Cooling superconductor receivers to 4 K does not appreciably improve the situation, as the number of photons required in the receiverless case is related to charge, capacitance, and voltage, not thermal noise. For capacitances below 1 fF (a difficult task), semiconductor receivers could potentially consume even less energy than their superconducting counterparts. Waveguide-integrated femtofarad photodiodes have been demonstrated in both SiGe and Ge [32]. Polysilicon photodiodes are also attractive for increased manufacturability [33]. Most photodiodes have far better speed than required for neuromorphic applications, reaching up to 45 GHz [32].

Just as with SNSPDs, semiconductor receivers will also require electrical power, even if it is minimized by the receiverless approach. In this case, there will be static power dissipation through the leakage current of the photodiode. Assuming a 1 V bias, a leakage current on the order of 1 nA [34], and an optical link efficiency of 1%, this static dissipation would dominate power consumption for average spiking rates below 10 kHz. The development of low capacitance, zero-bias photodiodes [35] would be a major advantage towards making efficient, low frequency networks. Static power consumption is also a major question for many avalanche photodiode (APD) receivers. Avalanche gain could provide a significant (at least one order of magnitude) reduction in the necessary optical power per spike [11]. While often associated with higher bias voltages, germanium waveguide-integrated avalanche detectors have been demonstrated to provide 10 dB of gain even at 1.5 V bias [36]. However, dark current is still typically in the microamp range for such detectors [36, 37], meaning that brain-scale networks are likely out of reach due to power constraints (Sec. 5). APDs may be of interest in smaller, faster spiking networks, however. Another intriguing possibility is to reduce static power consumption through cooling, as the dark current could potentially be reduced by orders of magnitude [38]. However, in that case one forfeits a major advantage of the semiconductor approach.

While the receiverless scheme is promising for achieving low energies per spike, it places significant burden on the transmitter side of the link. Neuromorphic applications magnify this burden, as neurons are expected to drive thousands of downstream connections in parallel. Additionally, the receiver capacitance must be charged quickly to maintain high spiking frequencies. The result is that relatively large optical power is required from transmitters. The best case (\( \eta = 1 \)) scenario is shown in figure 3. Semiconductor receivers can be expected to require around one thousand times the optical power of superconducting receivers and the highest spiking frequency of a neuron could very well be limited by the power output of the light source. The ramifications of this result on prospective light sources are discussed in the next section.

2.2 Optical Transmitters

The transmitter is expected to dominate the power budget of optical links for both platforms. Room-temperature, CMOS-integrated light sources have been a holy grail for decades, but materials integration issues have kept this prized objective out of reach. For superconducting systems, SNSPDs drastically lower the power requirements of light sources, while cryogenic temperatures improve light source efficiency. Light sources are likely significantly simpler in the superconducting case. However, interfacing low-voltage superconducting electronics with semiconduc-
tor light sources [39] presents an obstacle that is absent from the all-semiconductor platform.

### 2.2.1 Integrated Light Sources

Optical coherence is not a requirement for the envisioned system. NanoLEDs are thus an attractive option due to their ease of fabrication, lack of threshold current, and improving efficiency with shrinking scale [40]. However, nanoLEDs struggle to produce optical power significantly greater than $1 \mu W$ [40]. While semiconductor systems targeting spiking frequencies in excess of $1 MHz$ may be forced to turn to lasers, nanoLEDs should be more than sufficient for superconducting platforms. Either way, integrating millions of light sources on a $300 mm$ wafer remains highly challenging. The indirect band gap of silicon drastically reduces light emission. Off-chip light sources are used in some applications, but are likely untenable for massive systems, as their high static power consumption is incommensurate with the sparsity of neural activity. Integrated light sources would be a tremendous boon, if not a requirement for the success of large-scale optoelectronic neuromorphic computing. There are two courses of action: (1) force silicon to emit light through either material and/or environmental modifications or (2) integrate direct bandgap materials on silicon.

Many strategies towards silicon light sources have been pursued [41, 42] including quantum confinement in Si-based superlattices [43] and nanocrystals [44], emission from embedded erbium [45, 46], point-defect emitters [47–50], extended defects [51], strain dislocations [52], and engineering of the local density of optical states [53]. Total efficiency from 0.1% [52] to 1% [53] has been demonstrated at room temperature, but not at powers and areas suitable for the semiconductor receivers introduced in the previous section.

Abandoning silicon as an active optical element, many researchers turned towards epitaxial germanium grown on Si [54]. Like silicon, germanium is an indirect-gap semiconductor. However, the direct gap is only $136 meV$ higher than the indirect gap, and clever implementation of strain [55–57] and heavy $n$-type doping [58–62] can lead to appreciable direct, radiative recombination. These efforts have led to Ge-on-Si lasers [63, 64], but it has proven difficult to reduce the threshold current and increase device efficiency. Another approach is to grow SiGe with a hexagonal lattice on GaAs, leading to a direct gap [65], but this does little to solve integration problems.

At present, neither Si nor Ge emission has proved satisfactory for the needs of digital communication, so integrating III-V materials on silicon substrates has received significant attention. Pending a watershed moment in silicon sources, III-V integration will be required for the semiconductor platform (although not necessarily in the superconductor case, where low-temperature changes the physical context). Epitaxial growth would be an attractive solution for III-V integration due to the high throughput [66], but defects due to lattice mismatch have so far prevented this method from large-scale adoption. III-V quantum dots are more robust to such defects and have demonstrated high optical powers with small footprints [66–68], albeit typically grown on offcut Si substrates that are not CMOS compatible or with thick buffer layers that make optoelectronic contact difficult. More work is required to realize scalable, cost-effective integration of III-V quantum dot light sources with CMOS electronics, passive photonic waveguides, and efficient photodetectors. Without epitaxial growth, the semiconductor platform would be less scalable due to the limited size of III-V wafers and the expense of performing wafer bonding. A variety of schemes have been proposed [66, 69], including die-level bonding [70, 71], wafer-level bonding [72–74], transfer printing [75–77], and selective-area epitaxy [78], but these approaches still appear cumbersome when seeking the scale of integration considered here.

The situation is significantly more favorable for cryogenic systems. Low temperature often reduces non-radiative recombination [79–81], improving efficiency for both silicon and III-V light sources. The case of Ge at low temperature is more subtle due to the peculiarities of the pseudo-direct gap and inter-valley scattering that is more prevalent at higher temperatures [54]. The benefits are further compounded by the low optical power requirements of SNSPDs. When integrating III-V light sources with CMOS, the light sources must be integrated on top of the electronics after the high-temperature dopant activation steps have been performed. Superconductor electronics have no such high-temperature processing steps, so the light sources can be produced on a Si wafer before the electronics are realized. Problems related to offcut Si wafers and thick buffer layers are eliminated. Additionally, silicon light sources, with their superior potential for integration, demand exploration with the superconducting platform. Several silicon point defects typically quenched at...
room-temperature emerge as narrow-linewidth candidates for light sources in the telecommunications band [82–86]. While single-photon emission [87–89] is not the objective in the present context, the narrow linewidth is also attractive for further efficiency gains via the Purcell Effect [90]. LEDs have already been demonstrated with the W-center defect [84, 91], albeit with poor (10−6) efficiencies, limited by electrical injection efficiency rather than emitter lifetime. Photoluminescence studies are promising for orders of magnitude improvement [92], but more work is required to improve emission efficiency in an integrated-circuit context. If cryogenic silicon light sources become viable, the superconducting platform might hold a major scalability advantage over the semiconducting analogue.

2.2.2 Driving Circuitry

Both platforms require neurons to drive semiconductor light sources. The transmitter circuitry is thereby required to produce voltages on the scale of the bandgap of the optical source (≈ 1 V). CMOS circuitry, itself a semiconducting technology, naturally operates on this voltage, rendering the driving circuitry a non-issue. Standard MOSFET LED or modulator driving circuits [93, 94] can be straightforwardly adapted for neuromorphic applications. Superconductors, however, operate in an entirely different regime, with signals usually on the order of the superconducting energy gap (≈ 1 mV). The optimal method for interfacing superconducting electronics with semiconductor devices is still an area of active research. Recent progress has been made with devices utilizing the massive change in impedance during a phase transition between superconducting and resistive states. In Ref. 39, a resistive element was heated using 50 mV pulses to thermally trigger a transition in a superconducting meander. The meander transitioned to a state with resistance in excess of 10 MΩ and was used to drive a cryogenic silicon light source waveguide-coupled to an SNSPD. While these results are promising, the light source was only pulsed at 10 kHz (due to poor source efficiency) and was fabricated on a separate chip. More work is needed to improve the speed, efficiency, and to monolithically integrate driving circuitry with LEDs.

3 Electronic Neuronal Computation

Electronic circuitry capable of performing neuronal dynamical operations will also be necessary. Biological neurons are increasingly recognized as sophisticated computational units [95–98]. Emulating such complicated behavior has been the subject of extensive investigation in both semiconducting [99–104] and superconducting platforms [9, 105, 106]. We do not attempt a comprehensive review of circuitry, but rather draw attention to issues specific to optoelectronic networks in both cases.

3.1 Semiconductor Electronics

The maturity of CMOS processing has allowed great strides in neuromorphic computing. While optical communication would likely also be advantageous in digital approaches, we focus on analog CMOS neurons for their perceived efficiency advantages [107, 108]. At a basic level, a neuron must perform three mathematical functions: summation of synaptic inputs, temporal filtering, and threshold detection leading to action potential generation. Summation can be achieved by exploiting Kirchhoff’s current law. Filtering can be implemented with elementary resistor-capacitor circuits. Thresholding is a natural function of transistors. Building upon this basic mapping, analog neurons have demonstrated a litany of biologically-inspired models [100, 109].

It was found in the previous section that optical communication requires a minimum of about 1 fJ of energy to deliver a spike signal to each synapse. For realistic optical link efficiencies, this value will be at least an order of magnitude larger. Somatic processing circuits would therefore ideally operate with an energy budget of 10 fJ - 100 fJ to process a single spike. Somatic computation could comfortably consume power larger than that of synaptic processing by a factor of the average fan-out (perhaps 1000). Many low-energy neuromorphic demonstrations are promising for reaching these targets. By reducing the membrane capacitance and supply voltage, a neuron capable of 25 kHz spike rates was demonstrated to consume only 4 fJ/spike [110]. Many other analog neurons, with energies ranging from femtoJoules to picoJoules per spike, fall comfortably below the power consumption of optical communication [111]. However, it remains to be seen if more complicated neurons and synapses, implementing a critical subset of behavior necessary for cognition, will be able to maintain such low power operation. In terms of speed, CMOS neurons have demonstrated spike rates in excess of 100 MHz [112]. Optical communication should face few issues achieving such speeds, if sufficiently bright light sources can be efficiently integrated with CMOS circuits.

One challenge for the CMOS approach has been to design compact circuits with long time constants. Long time constants are important for systems targeting biological time scales (upwards of 500 ms) [111] or power-law distributions of timescales to implement critical behavior [113]. Subthreshold transistor circuits operating with currents in the femtoamp to picoamp range minimize the size of capacitor needed to implement a specific time constant [100]. The area constraints of this scheme are discussed in Appendix A and compared to the superconducting approach.

For a concrete example, a circuit diagram for a memristor implementation of the popular differential-pair integrator (DPI) synapse is shown in Fig. 4(b) [114]. The DPI produces a decaying exponential post synaptic signal in response to an input voltage pulse—potentially from an optical receiver. This leaky integrator behavior is charac-
terized by a time constant set by the value of the filtering capacitance and the rate of leakage off the capacitor [115]. The time constant could potentially be programmed using memristors—an advantage over superconducting circuits that have been proposed to date.

3.2 Superconducting Electronics

Superconducting neurons have been studied nearly as long as CMOS implementations, with a mapping between neuronal functions and superconducting electronics identified in the early 1990s [116, 117]. In this case, Faraday’s Law, governing the addition of magnetic flux through mutual inductors to superconducting loops provides the necessary synaptic summation function. Filtering is achieved through resistor-inductor blocks (or RC circuits in some cases [105]). Josephson junctions (JJs) provide the requisite nonlinear thresholding element.

Like their CMOS counterparts, many superconducting circuits have now been designed to implement sophisticated neuronal dynamics. Superconducting neuromorphic circuits have been designed to implement a variety of bio-inspired neuron models [105, 106, 118], dendritic processing [9], and have performed image classification in simulation [119]. The natural spiking behavior of JJs may even require a lower device count than analogous CMOS circuits for various leaky-integrate-and-fire models [105]. In short, it does not appear that superconducting circuits are any less capable of complex neuronal computation than CMOS, although experimental demonstrations lag far behind.

Superconducting electronics has long been pursued for gains in energy efficiency and speed. Indeed, superconducting elements dissipate zero static power and spike energies are frequently reported in the sub-femt joule range, including refrigeration. Optical communication is likely to dominate power consumption for superconducting optoelectronic systems (Appendix B). In terms of speed, fully electronic superconducting neurons may be capable of spike rates up to 100 GHz [118, 119]. However, this is orders of magnitude faster than any SNSPD can respond. This speed disparity is a notable difference between the superconducting and semiconducting architectures. While optical communication could be integrated with CMOS neurons with no degradation in speed, optoelectronic superconducting systems will likely be significantly slower than their fully electronic counterparts. This may be the cost of highly connected systems. That said, the extraordinary switching speed of JJs is still leveraged in optoelectronic networks to perform analog computations within synapses, dendrites, and neurons.

The ability of superconducting electronics to go slow might be just as compelling as their ability to go fast. While it can be challenging to implement long, biologically realistic time constants in CMOS neurons, superconducting loops can create time constants orders of magnitude higher than biology by adjusting the $L/R$ ratio in synaptic and neuronal loops (See Fig. 4(a) and Appendix A). The ability to generate dynamics across many orders of magnitude in time also dovetails nicely with suggestions that critical behavior is important for cognition [120].

Fan-in has traditionally been considered a liability of superconducting electronics. If this were the case, it would clearly be an impediment to mature superconducting neuromorphic systems. For superconducting neurons designed to use single fluxons as synaptic signals, fan-in has recently been analyzed [121], and it has been found that if a single synapse must be able to drive a neuron above threshold, fan-in may be limited to around 100. However, it is often not necessary for each synapse to be able to trigger a neuronal spike event. It has been analyzed elsewhere that if analog signals containing multitudes of fluxons are communicated from synapses to the neuron cell body, fan-in can likely scale to biological levels through the use of mutual inductors [2]. Using more fluxons comes with larger power consumption, but for optoelectronic systems, light production will likely still dominate.

While most diagrams of superconducting circuits (including those here) show many separate biases delivering current to various elements, the ability to construct circuits that can be biased in series will be critical to the scalability of this hardware. A separate bias for every synapse would be untenable in large-scale systems [122]. This mimics the evolution that occurred in superconducting digital electronics, in which the field has turned away from parallel biasing schemes and embraced serially biased platforms [122] and current recycling schemes [123]. SOENs are potentially amenable to serial biasing, but this important point demands further analysis.

A superconducting synaptic filtering circuit is shown in Fig. 4(a). Synaptic weighting is implemented in the receiver circuit (Fig. 2(a)), so this circuit block is only responsible for converting a train of fluxons into a decaying exponential post-synaptic potential reminiscent of biological and CMOS synapses. A resistor, $r_{si}$, converts a superconducting persistent current loop into a leaky-integrator in a similar manner to the DPI synapse. The time constant is set by $L_{si}/r_{si}$, and the synaptic current can be added to a neuronal circuit through mutual inductors. Unlike the DPI synapse, this circuit does not have a programmable time constant, but does hold the potential to implement a wide range of different time constants by fabricating different values of $L_{si}$ and $r_{si}$.

4 Synaptic Memory

It has been apparent to the neuromorphic community for some time that large-scale neural systems will require innovative approaches to synaptic memory. A local, analog memory element unique to every synapse will provide the most efficient performance by eliminating memory retrieval and digital conversion. Important metrics for analog synaptic memory technologies include weight precision,
volatility, area, write energy, write speed, and endurance (the effective number of cycles in a device’s lifetime). We attempt to provide desired benchmarks for a few of these metrics in the specific case of optoelectronic networks. For this section, we assume a speedup of about $10^4$ over biology, for an average spike rate of $10$ kHz and a maximum of $10$ MHz. This is commensurate with both the maximum count rates of high-yield SNSPDs and some of the fastest CMOS electronic neuromorphic systems built to-date.

4.1 Memory Benchmarks

4.1.1 Endurance

Large-scale neural systems require significant investments in money and time. Operational lifetimes on the scale of decades ($10^9$ seconds), if not longer, are therefore essential. Such systems will be expected to learn continually during that lifespan, placing significant requirements on the durability of memory technologies. The number of times a synapse is updated in its lifetime is a function of neuron spiking frequency ($f$) and the number of synapses that are typically updated after each post-synaptic spike. Neuroscientific evidence has been presented that the number of active presynaptic inputs required to trigger a post-synaptic spike goes as $\sqrt{N}$, where $N$ is the fan-in of the neuron—exceeding 1,000 for brain-like systems [124, 125]. We assume all synapses that contributed to the spiking of the post-synaptic neuron are updated with each spike. We then estimate the number of weight updates ($N_{update}$) in the synapses’s lifetime ($L$) will be:

$$N_{update} = \frac{Lf}{\sqrt{N}}$$

(4)

For a decades-long lifetime, and a mean spiking frequency of $10$ kHz, the total number of weight updates will be $10^{11}$. This is a challenging demand for many emerging non-volatile memory technologies.

4.1.2 Update Energy

One would like the power dedicated to weight updates not to exceed the power used for optical communication. Once again invoking the assumption that $\sqrt{N}$ synapses are updated with each postsynaptic spike, we arrive at the following relation between the energy to produce a single spike ($E_{opt}$) and that to update a single weight ($E_{update}$):

$$E_{update} < \sqrt{N}E_{opt}$$

(5)

Using the analysis in Sec. 2, 1 fJ of energy needs to be delivered to the receiver in either platform. Assuming a transmitter efficiency of 1%, this would mean $E_{opt}$ is 100 fJ. Therefore, for a fan-in of 1,000 synapses, $E_{update}$ would ideally be no more than about 3 pJ. This value includes any energy consumption of peripheral circuitry, both static and that associated with programming. This efficiency appears to have already been met by several emerging memory technologies [126, 127].

4.1.3 Update Speed

An ideal system would be capable of implementing synaptic updates within the minimum inter-spike interval. While semiconductor optoelectronic systems could potentially produce spike rates in excess of $10$ GHz (assuming sufficiently bright, integrated light sources can be achieved), synapses might need to be taken offline during WRITE operations, as it is unlikely that sophisticated plasticity mechanisms can be implemented in under 100 ps. Lower maximum frequencies would allow plasticity to be implemented without ever neglecting a spiking event. For our 10 MHz target, we desire memory updates in under 100 ns. Slower updates may not be completely intolerable, if network dynamics are robust to missed spikes during synaptic updates or to synaptic weights that are in the process of being altered.

4.1.4 Weight Precision

The necessary weight precision will be determined by the specifics of a chosen learning model and the desired application. Weight precision has been the subject of much discussion. It has been suggested that 4-bit precision is sufficient for state-of-the-art mixed signal neuromorphic systems [128]. Deep learning systems have also demonstrated success with 8-bit precision—a significant reduction from 32-bit floating point numbers [129]. Hippocampal synapses in rats have been inferred to allow at least 26 different states ($\approx 5$ bit), which squares nicely with computer science findings [130]. It has also been argued that metaplasticity mechanisms are more important for lifelong learning than the bit-depth of the synapse [131, 132].

Target values for these key synaptic memory metrics are summarized in Table 1.
Table 1: List of desired performance metrics for synaptic memory in a system with average fan-out of 1000, maximum spike rate of 10 MHz, average spike rate of 10 kHz, and spike energy of 100 fJ.

| Metric        | Goal                  |
|---------------|-----------------------|
| Endurance     | $>10^{11}$ updates    |
| Update Energy | $<3$ pJ               |
| Update Speed  | $<100$ ns             |
| Weight Precision | 4-8 bits            |

4.1.5 Programming Signals

One important criterion that eludes quantitative benchmarking is the complexity of programming circuitry for synaptic memory. Significant infrastructure for producing programming signals could limit scalability. For example, floating-gate synapses often require programming signals at significantly higher voltages than are likely to be used in other parts of the network. For large-scale systems, memories with simple programming requirements will be at an advantage. Superconducting loop memory (Sec. 4.2.4) is intriguing from this standpoint, as the plasticity circuits operate with nearly identical signals and circuit blocks as those found in the rest of the network.

4.2 Proposed Technologies

4.2.1 Room-temperature Analog Memories

Many technologies have been proposed to implement synaptic weighting for room-temperature neuromorphic hardware, each with strengths and weaknesses [133]. The quest to find a suitable device for local synaptic memory dates back to the origins of the field, when Mead and colleagues investigated floating gate transistors [134]. Since then, floating gate synapses have been used to implement STDP [135], are attractive as a mature alternative to emerging devices, and have been proposed for use in large-scale systems [136]. However, there are concerns about high programming voltages, speed, and endurance that may limit floating-gate memories to situations with less-frequent updates. More recently, momentum has shifted to other technologies [126]. Memristive devices [137–139], commonly used in resistive random-access memory have emerged as a popular alternative, with recent demonstrations including monolithic integration with CMOS [140] and unsupervised pattern recognition with a simple network of synapses [141]. Questions remain about high variability (both cycle-to-cycle and device-to-device) [114], linearity, and endurance [126]. Phase-change memory is another option, with its own demonstration of STDP [142]. Thermal management and endurance have been raised as issues [126,133]. Ferroelectric transistors present another alternative, as they have low variability, good potential for CMOS integration, and linearity [143]. Spin-torque memory, 2D materials, and organic electronics have also been proposed as solutions. Interested readers should consult one of the many review articles on this topic [133,144,145]. The field is burgeoning with new devices for synaptic memory, but to-date none has been dominant enough to monopolize research. To our knowledge, no technology has been able to simultaneously meet the targets in Table 1, but progress in this area is encouraging.

4.2.2 Superconducting Technologies

Many of the aforementioned technologies may also apply to superconducting optoelectronic systems, but their cryogenic operation has been scarcely explored. Two other types of memory, only accessible at low temperatures, have received the most attention for superconducting systems: magnetic Josephson junctions (MJJs) and superconducting loop memories. An important distinction from room-temperature technologies is that for superconducting memory to be truly non-volatile, it must retain its state both in the absence of a power supply and upon warming to room-temperature.

4.2.3 Magnetic Josephson Junctions

MJJs have been proposed as a (nearly) non-volatile memory technology for superconducting neuromorphic computing. A two-terminal device, the critical current of an MJJ can be programmed by changing the magnetic order of a ferromagnetic material placed in the tunneling barrier of a JJ [127]. MJJs are non-volatile with respect to electrical power, and there is optimism they can be made to retain their memory through a warm-up to room-temperature. Additionally, they provide remarkable performance with respect to the metrics given in Table 1. The energy per update is on the order of femtojoules (including cooling overhead), switching speeds are commensurate with firing rates exceeding 100 GHz, and devices can be scaled to tens of nanometers. All of these metrics surpass the requirements for optoelectronic networks, and can be exploited in all-electronic superconducting networks as well [118]. More work is needed to analyze the scaling potential of MJJs with respect to yield. The magnetic fields used during programming can be produced with magnetic control lines, but spin-torque mechanisms may provide a more scalable solution. Finding an efficient, scalable solution to programming MJJs in large-scale systems thus remains an area of research that will be critical to their potential for adoption.

4.2.4 Loop Memory

Superconducting loop memories have been in use for decades by the superconducting electronics community [146,147], but are not ideal for dense memory arrays commonly utilized as RAM in digital computing due to area...
concerns. In the case of optoelectronic spiking neural systems considered here, the objective is not to produce large RAM arrays, and size as well as addressing challenges do not emerge as significant impediments. Therefore, straightforward extensions of binary loop memories are the synaptic memory technology that appears most promising for the SOENs platform [2,148]. In these memory cells, circulating current persists indefinitely in a loop of superconducting wire. The current in the loop can be controlled by adding/removing magnetic-flux quanta with standard JJ circuitry. This memory loop is then inductively coupled to a wire supplying a bias current to a Josephson junction at the synapse (\(J_{\text{ef}}\) in Fig. 2(a)). When the synaptic SNSPD detects a photon, the biased junction will add an integer number of fluxons to another integrating superconductive loop (analogous to the membrane capacitance of a neuron). The number of fluxons added to the integration loop is a function of the bias supplied to the JJ, which is determined by the magnitude of current circulating in the memory loop. The number of analog memory levels in the memory loop is determined by the inductance of the loop, which is easily set with the length of a wire. High-kinetic-inductance materials [149] enable memory storage loops with over a thousand levels (10 bits) to be fabricated in an area of 5 \(\mu\)m \(\times\) 5 \(\mu\)m.

The loop-memory approach has several strengths. The memory is nearly analog and updates are nearly linear. Memory is updated by the switching of a JJ, which involves only a change of the phase of the superconducting wave function. This phase can switch \(10^{13}\) times in a second, so the endurance metric defined in the previous section is not an issue. This stands in contrast to room-temperature memories requiring material changes (filament formation, phase changes, etc.) which are often associated with degradation over time. Loop memory is also attractive from a fabrication perspective as it requires no additional materials or devices. The simplicity of the memory lends itself favorably to 3D integration, provided cross-talk from nearby loops can be mitigated. Plasticity circuits based on loop memories will also operate at the energy scale of single photons and flux quanta (\(10^{-19}\) J), which is commensurate with the rest of the circuitry in the network. This allows weight updates to be performed with the spikes the network produces in standard operation, reducing peripheral circuitry. There is no need to engineer differently shaped pulses for READ and WRITE operations, and the synapse does not need to be taken offline during programming. Simulations have demonstrated STDP learning with circuits containing four additional Josephson junctions [2].

Two aspects of loop memory are concerning. First, loop memory is not strictly non-volatile. While circulating current can persist in a superconducting loop without any power supply, superconductivity must be maintained. If the temperature of the system is raised above the critical temperature of the superconducting material, the memory will be lost. Mechanisms for transferring weights stored in current loops to non-volatile solutions will need to be developed if the system’s state is to be persevered upon reaching room-temperature (i.e. for maintenance or during a power interruption). The second weakness of loop memory is the size. The employed superconducting loops, as well as the transformers that couple them, will be large compared to all of the other solutions discussed. The consequences of these large-area components must be considered in the context of the entire system, which we discuss next.

5 System Level Considerations

Here we consider aspects concerning the integration of the components previously discussed and how systems may reach the scale of the brain. Basic graph theory metrics and the assumption of 300-mm fabrication processes allow us to assess area constraints and the benefits of 3D integration. It is found that at least five planes of photonic routing will be required in either platform to achieve brain-scale systems. Prospects for 3D integration of active elements are addressed. It also must be stressed that an optoelectronic system of the complexity of the human brain will be abjectly impossible on a single 300-mm wafer in either case. A possible vision for connecting many wafers is discussed. Finally, we analyze cooling and power concerns, finding that neither should preclude the development of brain-scale systems in either platform.

5.1 Considerations from Graph Theory

Neurons in brain regions active in cognition, such as the cerebral cortex and hippocampus, are characterized by a high degree of connectivity—often in excess of ten thousand connections per neuron [150,151]. These connections often extend across appreciable spatial distances. Creating and maintaining these connections comes with high metabolic and spatial costs. The severely constrained biological brain would not support such expenditures if they were not advantageous to cognition [152].

One reason why such high connectivity is necessary relates to efficient communication across the network. Rapid communication can only be achieved if the average path length across the network is small. In the language of graph theory, a network is a collection of nodes connected by edges. To calculate the shortest average path length across the network, one calculates the number of edges that must be traversed to travel from one node to another node in the network. One takes the mean of this quantity over all pairs of nodes. The shortest average path length (\(L\)) is a global metric that offers a glimpse at the efficiency with which information can be communicated across space.

Equation 6 provides the relationship between \(L\) and the number of edges connected to a node, or in our case, the number of synapses per neuron (\(k\)) for a random net-
work. In a random network, nearby and distant connections are equally probable. Specifically, the equation holds for Erdős–Rényi random graphs of networks with $N_{\text{tot}}$ neurons [153]:

$$\bar{k} = \exp \left[ \frac{\ln(N_{\text{tot}}) - \gamma}{L - 1/2} \right],$$

where $\gamma \approx 0.5772$ is Euler’s constant. For a network with $10^6$ neurons, each neuron must make nearly 10,000 connections to support an average path length of two, and 200 synapses must be formed to support a path length of three. For a network with $10^8$ neurons, more than 100,000 synapses are required for a path length of two, and more than 1,000 for a path length of three. The human hippocampus is a module with roughly $10^8$ neurons, each with 10,000-50,000 nearly spatially random connections. The objective of achieving an average path length between two and three may be an important reason why the hippocampus prioritizes this exceptional degree of connectivity [151]. The cerebral cortex in the human brain contains more than $10^{10}$ neurons, each with roughly 10,000 connections. This analysis indicates that a path length between two and three cannot be achieved across the entire cortex, and accordingly the cortex is constructed with a hierarchical, modular architecture [154,155] with high connectivity and efficient communication within smaller modules, and more sparse connectivity between modules separated by larger distances [155–158].

While more sophisticated graph metrics can further elucidate the network concepts underlying cognition [159], the simple, global metric of average shortest path length can help inform scaling analysis of artificial cognitive hardware at this early stage of development. We next consider the constraints $L$ puts on the size of synaptic circuits.

### 5.2 Generic Spatial Constraints

Based on the significance of the interplay between the hippocampus and cerebral cortex in cognition [160], we assume hardware for artificial neural systems will make use of similar architectural principles. Here we assume optoelectronic circuits will be fabricated using the conventional sequential, planar processing techniques of the silicon microelectronics industry. Photonic planes will implement the passive optical interconnects and electronic planes will accommodate all active electronics for neuronal function. We further specify to consideration of 300-mm wafers and seek a relationship between the network path length and the size of components on the wafer.

The area of a neuron occupied by its photonic waveguides can be approximated in a similar manner to the wires for electronic circuits [161]. This gives the following expression for the area of passive photonic circuitry:

$$A_p = \left( \frac{k w_{\text{wg}}}{p_p} \right)^2,$$

$p_p$ is the number of photonic waveguide planes, $k$ is the degree of each neuron (assumed identical), and $w_{\text{wg}}$ is the pitch of waveguides. The area of a neuron due to electronic synaptic circuits is given by

$$A_e = \frac{k w_{\text{sy}}^2}{p_e}.$$

$w_{\text{sy}}$ is the width of a synapse and $p_e$ is the number of planes of electronic circuits. Both $N_{\text{tot}}A_p$ and $N_{\text{tot}}A_e$ are subject to the area constraint of a 300-µm wafer. We use these relations to calculate the number of planes (electronic and photonic) that will be required to maintain a path length of 2.5 across a network of a given size (Fig. 5). See Appendix C for analysis of path length dependence on $w_{\text{sy}}$ and $w_{\text{wg}}$. A specific routing scheme is analyzed in reference [2]. More than ten million neurons (less than a mouse brain) on a single 300-mm wafer appears out of reach for any platform.

### 5.3 Fabrication Processes

We assume 300-nm silicon wafer processing. Wafer-scale integration has already been demonstrated for electronic neuromorphic systems [162]. Still, even at this scale, reaching $10^6$ optoelectronic neurons per wafer is a tall order for either platform (Fig. 5). We choose this integration metric somewhat arbitrarily; $10^6$ neurons per wafer corresponds to $10^4$ wafers for a human-cortex-scale system. This is roughly the same order as the number of processing units in modern supercomputers. If this target is to be reached, 3D integration at some level will be necessary. From Fig. 5, it is clear that either platform will require a minimum of five photonic planes. Fortunately, photonic planes are quite amenable to 3D integration. Common waveguide materials include amorphous silicon (aSi), silicon nitride (SiN$x$) and silicon oxynitride (SiO$_x$N$_y$). These dielectric materials can be deposited at low temperature, enabling several multi-planar demonstrations [163–166]. Additionally, low-temperature deposition makes such processes compatible with back-end CMOS fabrication. It
should be noted that five photonic planes represents a best-case scenario, as wider waveguides have lower loss and only minimal reduction in average path length (Appendix C).

3D integration of active electronics is less straightforward, particularly for the semiconductor approach. 3D CMOS integration has been the subject of decades of research [167–174] and still faces uncertainty. Required high-temperature processing steps for dopant activation and contact anneals typically have a degrading effect on previous layers. Much of 3D integration of silicon microelectronics takes place at the die scale [173], which is incommensurate with the scale of systems under consideration. For the semiconductor scenario, the best course of action may be to abandon 3D active electronics altogether in favor of simply reducing the footprint ($w_{xy}$) of synapses. We see again from Fig. 5 that nearly $10^6$ neurons can be integrated on a single plane if each synapse is on the order of $10 \mu m \times 10 \mu m$. This may be a challenging benchmark to reach with high-functionality synapses implementing complex plasticity and dynamics. Subthreshold circuits that have embraced larger CMOS nodes for decreased variability may need to adjust to more modern nodes, of which there is some precedent [175]. Additionally, photodetectors will be on the micron scale and long time-constant capacitors can require significant area (Appendix A) [111]. Both of these elements would however be fabricated on separate planes from MOSFETs.

Superconducting platforms would likely take the opposite approach, embracing 3D integration in the face of necessarily large device areas. Superconducting electronics, including active JJs, are routinely deposited at low temperatures ($< 180^\circ C$). Integrated circuits with two stacked planes of JJs have been demonstrated by two research laboratories [176, 177], along with multiple of planes of SNSPDs [27]. This is particularly important, as superconducting systems will not be able to reach $10^6$ neurons per wafer without 3D integration. A reasonable estimate for a superconducting synapse may be $30 \mu m$ on a side (Appendix B). Such a size would require eight electronic planes.

We note that even if $p_p = p_e = 1$, it is still possible to fabricate wafers with $10^6$ neurons, provided $k = 100$, giving $L = 3.5$ (Figs. 9 and 10 in Appendix C). While this does not match the short path lengths of cognitive circuits in the brain, such a network is likely to have significant technological and scientific utility while offering an intermediate-term practical objective.

5.4 Constructing Multi-Wafer Systems

Given that neither system will scale to billions of neurons on a single wafer, many wafers ($\sim 10,000$) will need to be connected together to support human-brain-scale computing. A vision for a multi-wafer system is discussed in reference [178] for the SOENs platform. Briefly, wafers are stacked and free-space optical communication is used to form highly inter-connected columns mimicking the modular structure of biological circuits [155–158, 179]. Columns are coupled to each other with lateral inter-wafer connections, but such connectivity is more sparse than that within a column. Optical fibers provide low-loss communication over long distances.

Achieving systems of this scale requires advances, particularly in wafer-scale circuit integration and system-level construction. A phenomenon akin to Moore’s law, with ever-decreasing feature sizes enabling ever-higher integration density is unlikely to carry this concept forward, as many device sizes are limited by other physical considerations. Metrics related to number of planes of integrated circuits and number of wafers in a system may be more relevant to chart progress in neuromorphic supercomputing. Gradual progress may be possible by consistently scaling up, but it is difficult to envision this sustained trend without a powerful economic drive.

5.5 Power Consumption and Cooling

5.5.1 Cooling Systems

Cooling systems will be a key component to either platform. For superconducting electronics, the system will fail completely if the temperature rises above the critical temperature ($T_c$). Superconducting neuromorphic systems will rely on niobium ($T_c = 9.3 K$) or a material with a similarly low $T_c$. Liquid helium (4.2 K) is the cryogen of choice for such temperatures. Cooling systems will add significantly to the power consumption of superconducting electronics. The power efficiency of a refrigeration system is measured by its specific power [180]. The specific power gives the number of watts consumed by the refrigeration system for every watt of heat removed. The theoretical limit for specific power, given by the Carnot limit, is $\frac{T_c - T_a}{T_a}$. For liquid helium temperature (4.2 K), the Carnot limit demands that at least 74 watts of refrigeration power are required to remove every watt of heat produced on-chip if the system is operated in a 300 K ambient. State-of-the-art systems have reached specific powers below 400 W/W. Auspiciously, the most efficient refrigeration systems also tend to have the highest heat loads. The ability to cool heat loads as high as 10 kW at 4.4 K have already been demonstrated by commercially available systems [181]. Throughout this paper we assume a more conservative specific power of 1000 W/W, representative of the smaller scale cryogenic systems used in most laboratories today. It does not appear that cryogenic capability will be an insurmountable obstacle towards large-scale superconducting neural systems.

5.5.2 Power Limitations

Modern supercomputers typically consume megawatts of power. Tianhe 2, for instance, requires 17.8 MW for operation (and another 6.4 MW for cooling) [122]. If we thus assume a total power budget of 10 MW, we can analyze the
trade-off between average firing rate and number of neurons. We assume 1 fJ of optical energy is required to initiate a firing event at each synapse and plot the maximum average frequency spiking frequency for several different optical link efficiencies in Fig. 6.

![Figure 6: Tradeoff between size and average spiking frequency for a population of optoelectronic neurons with a power budget of 10 MW (\( P = 10^{13} \text{W} \)). Fan-out (N) is 10^3 and the optical energy needed at each synapse is assumed to be 1 fJ (accounting for cooling in superconductor case). This likely would correspond to the limits of either superconductor or semiconductor neurons.](image)

Power does not appear to be a limiting factor in achieving brain-scale and brain-speed optoelectronic networks. If the power resources of modern supercomputers were dedicated to a brain-scale optoelectronic neuromorphic system, average spiking rates on the order of 10 kHz (10^4 speedup over biology) appear feasible even with relatively inefficient optical links. Such a system may enable brain-scale computation with time accelerated by four orders of magnitude.

Another factor to consider is power density. There is a maximum power density that can be handled by heat removal systems for both the semiconducting and superconducting case. In the semiconductor case, high-performance computing routinely generates power densities of hundreds of watts per square centimeter [122]. A theoretical limit of around 1 kW/cm^2 is postulated in Ref. 182. In contrast, superconducting systems will be required to operate at significantly lower power densities. Roughly 1 W/cm^2 is a conservative limit for on-chip power density that can be cooled with liquid helium [122]. Superconducting optical links appear to be capable of dissipating about three orders of magnitude less energy per bit, approximately cancelling out the limited power density requirements of superconducting systems in comparison with semiconductors. In practice, it might well be the case that mature, sophisticated synapses and neurons will occupy so much area that these power density limitations will be of no consequence. For instance, even with link efficiency of \( \eta = 10^{-4} \), a synapse would require a lateral dimension of less than 30 \( \mu \)m for power density considerations to limit spiking to less than 1 GHz. Section 5 argued that superconducting synapses are not likely to be smaller than this. 10\( \mu \)m semiconducting synapses could reach 1 GHz with \( 1 \times 10^{-3} \) efficiency. However, optoelectronic systems will have nonuniform power dissipation across the chip/wafer, with most of the power being dissipated at the light sources. A more in-depth analysis is required to see if heat removal will be an issue near the light sources in particular, but for the superconducting case it is convenient that the light sources themselves are not superconducting, and can afford to be raised to higher temperatures without failure. Concerns about local heating may be assuaged with layouts that sufficiently shield and/or separate thermally sensitive devices from the light sources.

6 Conclusion

The prospects of neuromorphic systems at the scale of the brain and beyond are tantalizing. The fan-out capability of optical communication coupled with the computational power of electronic circuitry makes optoelectronic systems a promising framework for realizing these high ambitions. However, there is no technology platform that is ready to support optoelectronic spiking networks of the scale and sophistication of the human brain. Making this vision a reality will require breakthroughs at the device level, no matter which path is chosen, particularly with regard to integrated light sources. Beyond that, several different classes of devices must be integrated alongside each other, which further reduces the likelihood for success. Efficient, densely integrated light sources, waveguide-coupled detectors, local memory devices, and capable neuronal circuitry all must be consolidated onto a single platform. Candidates for all requisite devices can be proposed for either semiconducting or superconducting platforms, and the two systems may be capable of similar performance. However, the technological paths toward achieving brain-scale systems with the two platforms diverge in important respects.

Semiconductor platforms hold advantages in technological maturity, room-temperature operation, and perhaps speed. Spike rates in excess of 10 GHz may be feasible, but only for systems significantly smaller than the human brain due to power constraints. Semiconductor receivers can potentially operate with extremely low energies per spiking event (sub femto-joule), making them a worthy competitor of superconducting single photon detectors. However, these low energy receivers require significant optical power from integrated light sources. To achieve biological-scale fan-out, either very bright light sources, repeatering schemes (costing area and yield), or additional gain stages (costing power) will need to be included. In terms of neuronal computation, semiconductor neurons have already demonstrated impressive functionality and low-power operation that should be capable of integration with optical communication infrastructure, provided the long-standing challenges with CMOS-integrated
Both Platforms

| Monolithic integration of light sources, detectors, memory, and electronics |
| At least five planes of passive photonic waveguides |
| Wafer-scale processing |
| Inter-wafer optical links |
| Memory meeting requirements in Sec. 4.1 |

Semiconductor Platform

| Femtojoule optical receivers with low static power |
| One million III-V light-sources per wafer integrated with CMOS electronics |
| Synapses and local plasticity circuits in area 10μm x 10μm |

Superconductor Platform

| One million III-V or group-IV light sources per wafer operating at cryogenic temperature |
| Interface superconducting electronics with semiconductor light sources |
| Serial biasing or current recycling for synapses and neurons |
| Eight planes of Josephson junctions and transformers per wafer with near-zero cross talk |

Figure 7: Summary of necessary hardware demonstrations for each platform if human-brain-scale artificial cognition is to be achieved.

III-V light sources can be overcome. Synaptic memory is a major open question, but a variety of non-volatile memory solutions have seen extensive investigation, and time will tell if one technology can meet the requirements we have laid out for brain-scale optoelectronic systems. 3D integration of transistors, photodetectors, and memory may not be a feasible solution, meaning aggressive scaling of synaptic circuits while maintaining complex functionality is perhaps a better strategy. The fabrication processes for mature semiconductor neural systems may prove to be prohibitively complicated and heterogeneous, perhaps requiring different processing strategies for sources, detectors, and memories. If wafer-scale monolithic integration of these components cannot be achieved, and chip-scale die-stacking techniques are required, the outlook for achieving brain-scale systems is limited.

Superconducting optoelectronic neural systems suffer from a comparatively primitive fabrication ecosystem, but the incorporation of superconducting devices provides several intriguing properties. SNSPD receivers place nearly the theoretical minimum burden on integrated light sources. This attribute compounds positively with the improvements in efficiency for light sources operating at cryogenic temperatures. Integration of light sources with superconducting electronics does not appear to have the same material integration challenges as integration with CMOS, but this state of affairs may be due to the lack of attention the effort has received. These factors make the large-scale integration of light sources appear more tractable than in the semiconductor case—perhaps even opening the door to silicon as an active optical material. Driving these light sources with superconducting electronics, however, has yet to demonstrate the performance required for this application. The implementation of a high-impedance pulse-and-reset circuit remains an open challenge. For computation, superconducting neuronal circuits appear just as capable of implementing complex neuronal and synaptic behaviors as their CMOS counterparts, but will need to be designed with serial biasing in order to scale. Additionally, some speed advantages present in superconducting electronics will be negated by the response time of SNSPDs (<1 GHz). Of course, even if maximum spike rates are limited to 20 MHz, this would still represent a speed-up of four orders of magnitude over biological systems. Memory seems to be a strength for the superconducting platform, as superconductivity provides new avenues of storing synaptic weights. Loop memory in particular may be capable of implementing plasticity mechanisms that operate with only the signals produced through normal network activity. Caution is in order here, however, as superconducting synaptic plasticity mechanisms have scarcely been explored. 3D integration may yield more readily in the superconductor platform. The inconvenience of cryogenic cooling is a serious consideration, but power and heat removal estimations indicate this is unlikely to be a limiting factor for brain-scale systems. If all these issues can be resolved, superconducting optoelectronic systems may require simpler manufacturing processes than the semiconductor approach, as the material ecosystem could potentially be parsimonious. Of course, superconducting foundries are far less developed than their semiconductor counterparts, which may negate these advantages in the near-term.

We would be remiss to paint the quest for neuromorphic supercomputing as only a question of hardware. The inner workings of the brain are the subject of intense investigation, and the emergent phenomena of cognition and
consciousness remain taunting, increasingly lonely enigmas entrenched in the netherworld between philosophy and science. Watershed breakthroughs in neuroscience and algorithmic development will be required for the discussed hardware platforms to have practical applications, although the hardware platforms themselves may be of use in helping to unravel some of these mysteries. The question of whether it is prudent to develop hardware before algorithms has pestered the field of neuromorphic computing since its inception. In this case, we believe that the length of development, rich opportunities for spin-off technologies, and inestimable potential make such hardware development well-worth pursuing even at this incipient stage.

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A Implementing Long Time Constants

For the DPI synapse (Sec. 3) the time constant is given by [115]:

$$\tau = \frac{C_{si} V_{th}}{\kappa I_r},$$

where $I_r$ is the current leaking off of the capacitor, set with transistor $T_3$, $V_{th}$ is the thermal voltage, and $\kappa$ is the subthreshold slope factor (typically order 1). Operating in the subthreshold regime allows $I_r$ to be reduced to femtoamps [183]. Metal Insulator Metal (MIM) capacitors utilizing high-k dielectrics can reach capacitance densities around 20 fF/µm² [184]. The maximum achievable time constant as a function of synapse width is shown in figure 8 for $I_r = 10$ fA, $\kappa = 1$, and $V_{th} = 25$ mV. Since MIM capacitors can be fabricated on a separate layer from transistors, the entire 10 µm × 10 µm area per synapse target identified in Sec. 5 could be dedicated to capacitor area. For SOENs synapses, $L_{si}/r_{si}$ sets the time constant. Inductors and resistors will most likely be fabricated on separate layers, again conserving space. A meandering geometry gives the maximum inductance $L_{si}$, that can be fabricated in an area $w_{sy}^2$ as:

$$L_{si} = \frac{w_{sy}^2 L_\square}{w_{wire}(w_{wire} + w_{gap})},$$

where $L_\square$ is the inductance per square of the material, and $w_{wire}$ and $w_{gap}$ are the minimum feature sizes. Small value resistors are fabricated by putting many wide resistances in parallel. The smallest (nonzero of course) resistor that can be fabricated in an area $w_{sy}^2$ is then:

$$r_{si} = \frac{R_s w_{gap}(w_{wire} + w_{gap})}{w_{sy}^2},$$

where $R_s$ is the sheet resistance. The maximum time constant ($\tau_{max}$) in area $w_{sy}^2$ is given by $L_{si}/r_{si}$:

$$\tau_{max} = \frac{w_{sy}^2 L_\square}{R_s w_{wire} w_{gap}(w_{wire} + w_{gap})^2}$$

The maximum achievable time constants as a function of synapse width is plotted in figure 8 for $R_s = 0.001 \Omega/\square$ (corresponds to a 200 nm gold layer with resistivity of $2 \times 10^{-10} \Omega\cdot m$ at 4 K [185]), $w_{wire} = w_{gap} = 100$ nm, and $L_\square = 160$ pH/\square, corresponding to MoSi. For the large synaptic areas expected to be available to superconducting synapses via 3D integration, the superconducting approach can support significantly larger time constants than the semiconducting case. In Ref. 111, it is suggested that the human brain itself is limited by the maximum achievable time constant, and relies on network dynamics for certain types of long-term memory. The ramifications of hardware with time-constants far greater than biology are intriguing.

B Area and Energy in Superconducting Synapses

JJJs will never be as small as MOSFETs [122], but the area of synaptic circuits is not limited by JJJs. Large inductors/transformers that couple flux from storage loops to receiving SQUIDs are likely to be the components that consume the most area. The size of these components is determined by the critical current of the junctions used in the SQUIDs ($I_c$), the permeability of free space ($\mu_0$), SQUID inductance ($L$), and the magnetic flux quantum ($\Phi_0$). Based on the typical SQUID design criterion [186] we expect $2LI_c/\Phi_0 = 1$. For a simple washer-type inductor geometry, $L \approx 1.25 \mu_0 w_{sq}^2$, where $w_{sq}$ is the inner dimension of the hole [187]. The energy, $E_{sq}$ to produce two fluxons is approximately $2L\Phi_0$ for an appropriately biased junction. There is thus a trade-off between the size
of a SQUID and its energy consumption:

\[
w_{sq} \approx \frac{\Phi_0^2}{1.25 \mu_0 E_{sq}}
\]  

(13)

\(I_c\) is further constrained by noise and the ability to interface with SNSPDs. \(I_c = 300 \mu A\) is reasonable and would correspond to \(w_{sq} \approx 2.2 \mu m\) and \(E_{sq} \approx 1.2 \text{ aJ}\). If the optical energy per synapse is around 100 aJ for a 1% efficient link, about 170 fluxons can be produced per synapse event without dominating the power budget. In practice, each SQUID may require a lateral dimension about five times larger than \(w_{sq}\) to account for washer width, wiring, and spacing to minimize cross-talk. Additionally, each synapse will likely be composed of three or four SQUIDs—one for synaptic integration, one for loop memory, and perhaps two more for various plasticity functions. A reasonable estimate for synaptic size is then about 30 \(\mu m \times 30 \mu m\).

C Further Scaling Analysis

Figures 9 and 10 provide insight into how network connectivity constrains hardware for any planar fully-dedicated system. Figure 9 plots Eq. 6, giving the average node degree (number of synapses per neuron) necessary to maintain a given path length as a function of network size.

Figure 9: Average node degree as a function of network size for different path lengths.

Figure 10 plots the minimum achievable path length as a function of synaptic width and waveguide width (Eqs. 8 and 7). Path length is relatively insensitive to waveguide pitch, suggesting that wider, and therefore lower loss waveguides may be beneficial. In contrast, we see that the synaptic size (\(w_{syn}\)) can be a major impediment to achieving low path lengths.

C References

[1] Steve Furber. Large-scale neuromorphic computing systems. Journal of neural engineering, 13(5):051001, 2016.

[2] Jeffrey M Shainline, Sonia M Buckley, Adam N McCaughan, Jeffrey T Chiles, Amir Jafari Salim, Manuel Castellanos-Beltran, Christine A Donnelly, Michael L Schneider, Richard P Mirin, and Sae Woo Nam. Superconducting optoelectronic loop neurons. Journal of Applied Physics, 126(4):044902, 2019.

[3] Aaron R Young, Mark E Dean, James S Plank, and Garrett S Rose. A review of spiking neuromorphic hardware communication systems. IEEE Access, 7:135606–135620, 2019.

[4] John L Hennessy and David A Patterson. Computer architecture: a quantitative approach. Elsevier, 2011. Appendix F, pg. F-53.

[5] C. Segal, A. Dalakoti, M. Miller, and F. Brewer. Connectivity Effects on Energy and Area for Neuromorphic System with High Speed Asynchronous Pulse Mode Links. SLIP, 16, 2016.
[6] E Marder. Neurotransmitters and neuromodulators. In The crustacean stomatogastric system, pages 263–306. Springer, 1987.

[7] Thomas Euler and Winfried Denk. Dendritic processing. Current opinion in neurobiology, 11(4):415–422, 2001.

[8] Jeffrey M Shainline, Sonia M Buckley, Richard P Mirin, and Sae Woo Nam. Superconducting optoelectronic circuits for neuromorphic computing. Physical Review Applied, 7(3):034013, 2017.

[9] Jeffrey M Shainline. Fluxonic processing of photonic synapse events. IEEE Journal of Selected Topics in Quantum Electronics, 26(1):1–15, 2019.

[10] J.M. Shainline. Optoelectronic Intelligence. Appl. Phys. Lett., 118:160501, 2021.

[11] David AB Miller. Attojoule optoelectronics for low-energy information processing and communications. Journal of Lightwave Technology, 35(3):346–396, 2017.

[12] J.P. Sprengers, A. Gaggero, D. Sahin, S. Jahanmirinejad, G. Frucci, F. Mattioli, R. Leoni, J. Beetz, M. Lerner, M. Kamp, S. Höfling, R. Sanjines, and A. Fiore. Waveguide superconducting single-photon detectors for integrated quantum photonic circuits. Appl. Phys. Lett., 99:181110, 2011.

[13] W. Pernice, C. Schuck, O. Minaeva, M. Li, G. Goltsman, A. Sergienko, and H. Tang. High speed travelling wave single-photon detectors with near-unity quantum efficiency. Nat. Comm., 3:1325, 2012.

[14] Mohsen K Akhlaghi, Ellen Schelew, and Jeff F Young. Waveguide integrated superconducting single-photon detectors implemented as near-perfect absorbers of coherent radiation. Nature communications, 6(1):1–8, 2015.

[15] S. Ferrari, O. Kahl, V. Kovalyuk, G.N. Goltsman, A. Korineev, and W.H.P. Pernice. Waveguide-integrated single- and multi-photon detector at telecom wavelengths using superconducting nanowires. Appl. Phys. Lett., 106:151101, 2015.

[16] D. Sahin, A. Gaggero, J.-W. Weber, I. Agafonov, M.A. Verheijen, F. Mattioli, J. Beetz, M. Kamp, S. Höfling, M.C.M. van de Sanden, R. Leoni, and A. Fiore. Waveguide nanowire superconducting single-photon detectors fabricated on gaas and the study of their optical properties. IEEE J. Sel. Top. Quant. Electron., 21:3800210, 2015.

[17] J.M. Shainline, S.M. Buckley, N. Nader, C.M. Gentry, K.C. Cossel, J.W. Cleary, M. Popović, N.R. Newbury, S.W. Nam, and R.P. Mirin. Room-temperature-deposited dielectrics and superconductors for integrated photonics. Opt. Express, 25:10322, 2017.

[18] Simone Ferrari, Carsten Schuck, and Wolfram Pernice. Waveguide-integrated superconducting nanowire single-photon detectors. Nanophotonics, 7(11):1725–1758, 2018.

[19] S.M. Buckley, A.N. Tait, J. Chiles, A.N. McCaughan, S. Khan, R.P. Mirin, S.W. Nam, and J.M. Shainline. Integrated-Photonic Characterization of Single-Photon Detectors for Use in Neuromorphic Synapses. Phys. Rev. Applied, page 054008, 2020.

[20] Behzad Razavi. Design of integrated circuits for optical communications. John Wiley & Sons, 2012.

[21] F. Marsili, V.B. Verma, J.A. Stern, S. Harrington, A.E. Lita, T. Gerrits, I. Vayshniker, B. Baek, M.D. Shaw, R.P. Mirin, and S.W. Nam. Detecting single infrared photons with 93% system efficiency. Nat. Photon., 7:210, 2013.

[22] D.V. Reddy, R.R. Nerem, S.W. Nam, R.P. Mirin, and V.B. Verma. Superconducting nanowire single-photon detectors with 98% system detection efficiency at 1550 nm. Optica, 7:1649, 2020.

[23] Richard B Stein, E Roderich Gossen, and Kelvin E Jones. Neuronal variability: noise or part of the signal? Nature Reviews Neuroscience, 6(5):389–397, 2005.

[24] Mark D McDonnell and Lawrence M Ward. The benefits of noise in neural systems: bridging theory and experiment. Nature Reviews Neuroscience, 12(7):415–425, 2011.

[25] Christina Allen and Charles F Stevens. An evaluation of causes for unreliability of synaptic transmission. Proceedings of the National Academy of Sciences, 91(22):10380–10383, 1994.

[26] J.E. Lisman. Bursts as a unit of neural information: making unreliable synapses reliable. Trends Neurosci., 20:38, 1997.

[27] V.B. Verma, F. Marsili, S. Harrington, A.E. Lita, R.P. Mirin, and S.W. Nam. A three-dimensional, polarization-insensitive superconducting nanowire avalanche photodetector. Appl. Phys. Lett., 101:251114, 2012.

[28] D Rosenberg, AJ Kerman, RJ Molnar, and EA Dauler. High-speed and high-efficiency superconducting nanowire single photon detector array. Optics express, 21(2):1440–1447, 2013.
[29] Andreas Vetter, Simone Ferrari, Patrik Rath, Ra-  
soul Alaee, Oliver Kahl, Vadim Kovalyuk, Silvia  
Diewald, Gregory N Goltsman, Alexander Korneev,  
Carsten Rockstuhl, et al. Cavity-enhanced and  
ultrafast superconducting single-photon detectors.  
Nano letters, 16(11):7085–7092, 2016.

[30] E.E. Wollman, V.B. Verma, A.E. Lita, W.H. Farr,  
M.D. Shaw, R.P. Mirin, and S.W. Nam. Kilopixel  
array of superconducting nanowire single-photon de-  
tectors. Opt. Express, 27:35279, 2019.

[31] Christof Debaes, Aparna Bhatnagar, Diwakar Agar-  
wal, Ray Chen, Gordon A Keeler, Noah C Helman,  
Hugo Thienpont, and David AB Miller. Receiver-  
less optical clock injection for clock distribution net-  
works. IEEE journal of selected topics in quantum  
electronics, 9(2):400–409, 2003.

[32] Christopher T DeRose, Douglas C Trotter,  
William A Zortman, Andrew L Starbuck, Moz  
Fisher, Michael R Watts, and Paul S Davids. Ul-  
tra compact 45 ghz cmos compatible germanium  
waveguide photodiode with low dark current. Optics  
express, 19(25):24897–24904, 2011.

[33] K.K. Mehta, J.S. Orcutt, J.M. Shainline, O. Tehar-  
zahav, Z. Sternberg, R. Meade, M.A. Popović, and  
Rajeev J. Ram. Polycrystalline silicon ring resonator  
photodiodes in a bulk complementary metal-oxide-  
semiconductor process. Opt. Lett., 39:1061, 2014.

[34] Yu Zhang, Anirban Samanta, Kuanping Shang, and  
SJ Ben Yoo. Scalable 3d silicon photonic electronic  
integrated circuits and their applications. IEEE  
Journal of Selected Topics in Quantum Electronics,  
26(2):1–10, 2020.

[35] Kengo Nozaki, Shinji Matsuo, Takuro Fujii, Koji  
Takeda, Akihiko Shinya, Eiichi Kuramochi, and  
Masaya Notomi. Forward-biased nanophotonic de-  
tector for ultralow-energy dissipation receiver. APL  
Photonics, 3(4):046101, 2018.

[36] Solomon Assefa, Fengnian Xia, and Yuriii A Vlasov.  
Reinventing germanium avalanche photodetector for  
nanophotonic on-chip optical interconnects. Nature,  
464(7285):80–84, 2010.

[37] Léopold Virot, Paul Crozat, Jean-Marc Fédéli,  
Jean-Michel Hartmann, Delphine Marris-Morini,  
Eric Cassan, Frédéric Boeuf, and Laurent Vivien.  
Germanium avalanche receiver for low power inter-  
connects. Nature communications, 5(1):1–6, 2014.

[38] Andrea Pizzone, Srinivasan Ashwini Srinivasan, Pet-  
er Verheyen, Guy Lepage, Sadhishkumar Balakrish-  
nan, and Joris Van Campenhout. Analysis of dark  
current in ge-on-si photodiodes at cryogenic temper-  
atures. In 2020 IEEE Photonics Conference (IPC),  
pages 1–2. IEEE.
[52] V. Kveder, M. Badylevich, E. Steinman, A. Izotov, M. Seibt, and W. Schröter. Room-temperature silicon light-emitting diodes based on dislocation luminescence. *Appl. Phys. Lett.*, 84:2106, 2004.

[53] Martin A. Green, Jianhua Zaho, Aihua Wang, Peter J. Reese, and Michael Gal. Efficient silicon light-emitting diodes. *Nature*, 412:805, 2001.

[54] Xiaochen Sun, Jifeng Liu, Lionel C Kimerling, and Jurgen Michel. Toward a germanium laser for integrated silicon photonics. *IEEE Journal of Selected Topics in Quantum Electronics*, 16(1):124–131, 2009.

[55] Yasuhiko Ishikawa, Kazumi Wada, Douglas D Cannon, Jifeng Liu, Hsin-Chiao Luan, and Lionel C Kimerling. Strain-induced band gap shrinkage in Ge grown on Si substrate. *Applied Physics Letters*, 82(13):2044–2046, 2003.

[56] A Ghrib, M De Kersauson, M El Kurdi, R Jakomin, G Beaudoin, S Sauvage, G Fishman, G Ndong, M Chaigneau, R Ossikovski, et al. Control of tensile strain in germanium waveguides through silicon nitride layers. *Applied Physics Letters*, 100(20):201104, 2012.

[57] Kazuki Tani, Katsuya Oda, Momoko Deura, and Tatemi Ido. Enhanced room-temperature electroluminescence from a germanium waveguide on a silicon-on-insulator diode with a silicon nitride stressor. *Optics Express*, 29(3):3584–3595, 2021.

[58] Jifeng Liu, Xiaochen Sun, Dong Pan, Xiaoxin Wang, Lionel C Kimerling, Thomas L Koch, and Jurgen Michel. Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si. *Optics express*, 15(18):11272–11277, 2007.

[59] M El Kurdi, T Kociniewski, T-P Ngo, J Boulmer, D Debarre, P Boucaud, JF Damlencourt, O Kermarec, and D Bensahel. Enhanced photoluminescence of heavily n-doped germanium. *Applied Physics Letters*, 94(19):191107, 2009.

[60] Xiaochen Sun, Jifeng Liu, Lionel C Kimerling, and Jurgen Michel. Direct gap photoluminescence of n-type tensile-strained Ge-on-Si. *Applied Physics Letters*, 95(1):011911, 2009.

[61] Rodolfo Camacho-Aguilera, Zhaohong Han, Yan Cai, Lionel C Kimerling, and Jurgen Michel. Direct band gap narrowing in highly doped Ge. *Applied Physics Letters*, 102(15):152106, 2013.

[62] Michele Virgilio, CL Manganelli, Giuseppe Grosso, G Pizzi, and G Capellini. Radiative recombination and optical gain spectra in biaxially strained n-type germanium. *Physical review B*, 87(23):235313, 2013.

[63] Xiaochen Sun, Jifeng Liu, Lionel C Kimerling, and Jurgen Michel. Room-temperature direct bandgap electroluminescence from Ge-on-Si light-emitting diodes. *Optics letters*, 34(8):1198–1200, 2009.

[64] Jifeng Liu, Xiaochen Sun, Rodolfo Camacho-Aguilera, Lionel C Kimerling, and Jurgen Michel. Ge-on-Si laser operating at room temperature. *Opt. Lett.*, 35(5):679–681, Mar 2010.

[65] Elham M.T. Fadaly, Alain Dijkstra, Jens René Suckert, Dorian Ziss, Marvin A.J. van Tilburg, Chenyang Mao, Yizhen Ren, Victor T. van Lange, Ksenia Korzum, Sebastian Kölling, Marcel A. Verheijen, David Busse, Claudia Rödl, Jürgen Furthmüller, Friedhelm Bechstedt, Julian Stangl, Jonathan J. Finley, Silvana Botti, Jos E.M. Haverkort, and Erik P.A.M. Bakkers. Direct-bandgap emission from hexagonal Ge and SiGe alloys. *Nature*, 580(7802):205–209, 2020.

[66] Justin C Norman, Daehwan Jung, Yating Wan, and John E Bowers. Perspective: The future of quantum dot photonic integrated circuits. *APL Photonics*, 3(3):030901, 2018.

[67] S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S.N. Elliott, A. Sobiesierski, A.J. Seeds, I. Ross, P.M. Snowton, and H. Liu. Electrically pumped continuous-wave III-V quantum dot lasers on silicon. *Nat. Photonics*, 10:307, 2016.

[68] Daehwan Jung, Justin Norman, MJ Kennedy, Chen Shang, Bongki Shin, Yating Wan, Arthur C Gossard, and John E Bowers. High efficiency low threshold current 1.3 µm InAs quantum dot lasers on on-axis (001) gap/Si. *Applied Physics Letters*, 111(12):122107, 2017.

[69] Mingchu Tang, Jae-Seong Park, Zhechao Wang, Siming Chen, Pamela Jurczak, Alwyn Seeds, and Huiyun Liu. Integration of III-V lasers on Si for Si photonics. *Progress in Quantum Electronics*, 66:1–18, 2019.

[70] B. Song, C. Stagarescu, S. Ristic, A. Behfar, and J. Klamkin. 3D integrated hybrid silicon laser. *Opt. Express*, 24:10435, 2016.

[71] G. Crosnier, D. Sanchez, S. Bouchoule, P. Monnier, G. Beaudoin, I. Sagnes, R. Raj, and F. Raineri. Hybrid indium phosphide-on-silicon nanolaser diode. *Nat. Photon.*, 11:297, 2017.

[72] Y. Hu, D. Liang, K. Mikherjee, Y. Li, C. Zhang, G. Kurcveil, X. Huang, and R.G. Beausoleil. III/V-on-Si MQW lasers by using a novel photonic integration method of regrowth on a bonding template. *Light: Science & Applications*, 8:93, 2019.
B. Szelag, K. Hassan, L. Adelmini, E. Ghegin, P. Rodriguez, F. Nemouchi, P. Brianceau, E. Vermande, A. Schembri, D. Carrara, P. Cavalié, F. Franchin, M.-C. Roure, L. Sanchez, C. Jany, and S. Olivier. Hybrid iii-V/Silicon Technology for Laser Integration on a 200-mm Fully CMOS-Compatible Silicon Photonics Platform. IEEE J. Sel. Top. Quant. Electron., 25:8201210, 2019.

Y. Jiao, J. van der Tol, V. Pogoretskii, J. van Engelen, A.A. Kashi, S. Reniers, Y. Wang, X. Zhao, and W. Yao et al. Indium Phosphide Membrane Nanophotonic Integrated Circuits on Silicon. Physica Status Solidi, 217:1900606, 2020.

J. Justice, C. Bower, M. Meitl, M.B. Mooney, M.A. Gubbins, and B. Corbett. Wafer-scale integration of group III-V lasers on silicon using transfer printing of epitaxial layers. Nat. Photonics, 6:610, 2012.

J. Zhang, B. Haq, J. O’Callaghan, A. Gocalinska, E. Pelucchi, A.J. Trindade, B. Corbett, G. Morthier, and G. Roelkens. Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser. Opt. Express, 26:8821, 2018.

Jing Zhang, Grigorij Muliuk, Joan Juvert, Sulakshna Kumari, Jeroen Goyvaerts, Bahawal Haq, Camiel Op de Beeck, Bart Kuyken, Geert Morthier, Dries Van Thourhout, et al. Iii-v-on-si photonic integrated circuits realized using micro-transfer-printing. APL photonics, 4(11):110803, 2019.

Y. Han, Y. Xue, Z. Yan, and K.M. Lau. Selectively Grown III-V Lasers for Integrated Si-Photonics. J. Lightwave Technol., 39:940, 2021.

M Gurioli, A Vinattieri, M Colocci, J Massies, G Neu, A Bosacchi, and S Franchi. Temperature dependence of the radiative and nonradiative recombination time in gaas/al x ga 1- x as quantum-well structures. Physical Review B, 44(7):3115, 1991.

V Dolores-Calzadilla, B Romeira, F Pagliano, S Birindelli, A Higuera-Rodriguez, PJ Van Veldhoven, MK Smit, A Fiore, and D Heiss. Waveguide-coupled nanopillar metal-cavity light-emitting diodes on silicon. Nature communications, 8(1):1–8, 2017.

D.J. Sandiford. Temperature Dependence of Carrier Lifetime in Silicon. Proc. Phys. Soc., 71:1002, 1958.

Gordon Davies. The optical properties of luminescence centres in silicon. Physics reports, 176(3-4):83–188, 1989.

H. Sumikura, E. Kuramochi, H. Taniyama, and M. Notomi. Ultrafast spontaneous emission of copper-doped silicon enhanced by an optical nanocavity. Sci. Rep., 4:5040, 2014.

Sonia Buckley, Jeffrey Chiles, Adam N McCaughan, Galan Moody, Kevin L Silverman, Martin J Stevens, Richard P Mirin, Sae Woo Nam, and Jeffrey M Shainline. All-silicon light-emitting diodes waveguide-integrated with superconducting single-photon detectors.Applied Physics Letters, 111(14):141101, 2017.

C. Beaufils, W. Redjem, E. Rousseau, V. Jacques, A.Y. Kuznetsov, C. Raynaud, C. Voisin, A. Benali, T. Herzig, S. Pezzagna, J. Meijer, M. Abbarchi, and G. cassabois. Optical properties of an ensemble of G-centers in silicon. Phys. Rev. B, 97:035303, 2018.

C. Chartrand, L. Bergeron, K.J. Morse, H. Riemann, N.V. Abrosimov, P. Becker, H.-J. Pohl, S. Simmons, and M.L.W. Thewalt. Highly enriched 28Si reveals remarkable optical linewidths and fine structure for well-known damage centers. Phys. Rev. B, 98:195201, 2018.

M. Hollenback, Y. Berencén, U. Kentsch, M. Helm, and G.V. Astakhov. Engineering telecom single-photon emitters in silicon for scalable quantum photonics. Opt. Express, 28:26111, 2020.

W. Redjem, A. Durand, T. Herzig, A. Benali, S. Pezzagna, J. Meijer, A. Yu. Kuznetsov, H.S. Nguyen, S. Cueff, J.-M. Gérard, I. Robert-Philip, B. Gil, D. Caliste, P. Pochet, M. Abbarchi, V. Jacques, A. Dréau, and G. Cassabois. Single artificial atoms in silicon emitting at telecom wavelengths. Nat. Electronics, 3:738, 2020.

L. Bergeron, C. Chartrand, A.T.K. Kurkjian, K.J. Morse, H. Riemann, N.V. Abrosimov, P. Becker, H.-J. Pohl, M.L.W. Thewalt, and S. Simmons. Silicon-Integrated Telecommunications Photon-Spin Interface. PRX Quantum, 1:020301, 2020.

Bruno Romeira and Andrea Fiore. Purcell effect in the stimulated and spontaneous emission rates of nanoscale semiconductor lasers. IEEE Journal of Quantum Electronics, 54(2):1–12, 2018.

Jiming Bao, Malek Tabbal, Taegon Kim, Supakit Charrvanichborikarn, James S Williams, Michael J Aziz, and Federico Capasso. Point defect engineered si sub-bandgap light-emitting diode. Optics Express, 15(11):6727–6733, 2007.

Sonia M Buckley, Alexander N Tait, Galan Moody, Bryce Primavera, Stephen Olson, Joshua Herman, Kevin L Silverman, Satyavolu Papa Rao, Sae Woo Nam, Richard P Mirin, et al. Optimization of photoluminescence from w centers in a silicon-on-insulator. Optics express, 28(11):16057–16072, 2020.
[93] John E Bowers, Tin Komljenovic, Michael Dav- enport, Jared Hulme, Alan Y Liu, Christos T Santis, Alexander Spott, Sudharsanan Srinivasan, Eric J Stanton, and Chong Zhang. Recent advances in silicon photonic integrated circuits. In Next-Generation Optical Communication: Components, Sub-Systems, and Systems V, volume 9774, page 977402. International Society for Optics and Photonics, 2016.

[94] Hubert Halbritter, Claus Jäger, Rolf Weber, Michael Schwind, and Frank Möllmer. High-speed led driver for ns-pulse switching of high-current leds. IEEE Photonics Technology Letters, 26(18):1871–1873, 2014.

[95] C. Koch and I Segev. The Role of Single Neurons in Information Processing. Nature Neuroscience, 3:1171, 2000.

[96] G.J. Stuart and N. Spruston. Dendritic integration: 60 years of progress. Nature Neuroscience, 18:1713, 2015.

[97] J. Hawkins and S. Ahmad. Why neurons have thousands of synapses, a theory of sequence memory in neocortex. Frontiers in Neural Circuits, 10:23, 2016.

[98] S. Sardi, R. Vardi, A. Sheinin, A. Goldental, and I. Kanter. New types of experiments reveal that a neuron functions as multiple independent threshold units. Scientific Reports, 7:18036, 2017.

[99] Giacomo Indiveri, Bernabé Linares-Barranco, Tara Julia Hamilton, André Van Schaik, Ralph Etienne-Cummings, Tobi Delbruck, Shih-Chii Liu, Piotr Dudek, Philipp Häfliger, Sylvie Renaud, et al. Neuromorphic silicon neuron circuits. Frontiers in neuroscience, 5:73, 2011.

[100] T. Pfeil, A. Grubl, S. Jeltsch, E. Müller, M.A. Metrovici, M. Schmuker, D. Brüderle, J. Schemmel, and K. Meier. Six networks on a universal neuromorphic computing substrate. Frontiers in Neuroscience, 7:1, 2013.

[101] S. Brink, S. Nease, and P. Hasler. Computing with networks of spiking neurons on a biophysically motivated floating-gate based neuromorphic integrated circuit. Neural Networks, 45:39, 2013.

[102] B.V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A.R. Chandresekaran, J.-M. Bussat, R. Alvarez-Icaza, J.V. Arthur, P.A. Merolla, and K. Boahen. Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations. Proceedings of the IEEE, 102:699, 2014.

[103] K. Abu-Hassan, J.D. Taylor, P.G. Morris, E. Donati, Z.A. Bortolotto, G. Indiveri, J.F.R. Paton, and A. Nogaret. Optimal solid state neurons. Nat. Comm., 10:5309, 2019.

[104] Patrick Crotty, Dan Schult, and Ken Segall. Josephson junction simulation of neurons. Physical Review E, 82(1):011914, 2010.

[105] Emily Toomey, Ken Segall, and Karl K Berggren. Design of a power efficient artificial neuron using superconducting nanowires. Frontiers in neuroscience, 13:933, 2019.

[106] Carver Mead. Neuromorphic electronic systems. Proceedings of the IEEE, 78(10):1629–1636, 1990.

[107] Bipin Rajendran, Yong Liu, Jae-sun Seo, Kailash Gopalakrishnan, Leland Chang, Daniel J Friedman, and Mark B Ritter. Specifications of nanoscale devices and circuits for neuromorphic computational systems. IEEE Transactions on Electron Devices, 60(1):246–253, 2012.

[108] S.-C. Liu, T. Delbruck, G. Indiveri, A. Whatley, and R. Douglas, editors. Event-based neuromorphic systems. John Wiley and Sons, 2015.

[109] Ilia Sourikopoulos, Sara Hedayat, Christophe Loyez, François Danneville, Virginie Hoel, Eric Mercier, and Alain Cappy. A 4-fj/spike artificial neuron in 65 nm cmos technology. Frontiers in neuroscience, 11:123, 2017.

[110] Giacomo Indiveri and Yulia Sandamirskaya. The importance of space and time for signal processing in neuromorphic agents: the challenge of developing low-power, autonomous agents that interact with the environment. IEEE Signal Processing Magazine, 36(6):16–28, 2019.

[111] Johannes Schemmel, Laura Kriener, Paul Müller, and Karlheinz Meier. An accelerated analog neuromorphic hardware system emulating ndma- and calcium-based non-linear dendrites. In 2017 International Joint Conference on Neural Networks (IJCNN), pages 2217–2226. IEEE, 2017.

[112] Thomas Dalgaty, Melika Payvand, Filippo Moro, Denys RB Ly, Florian Peyab-Peyroula, Jerome Casas, Giacomo Indiveri, and Elisa Vianello. Hybrid neuromorphic circuits exploiting non-conventional
properties of rram for massively parallel local plasticity mechanisms. APL Materials, 7(8):081125, 2019.

[115] Elisabetta Chicca, Fabio Stefanini, Chiara Bartolozzi, and Giacomo Indiveri. Neuromorphic electronic circuits for building autonomous cognitive systems. Proceedings of the IEEE, 102(9):1367–1388, 2014.

[116] Y. Harada and E. Goto. Artificial neural network circuits with josephson devices. IEEE Trans. Magnetics, 27:2863, 1991.

[117] M. Hidaka and L.A. Akers. An artificial neural cell implemented with superconducting circuits. Supercond. Sci. Technol., 4:654, 1991.

[118] Michael L Schneider, Christine A Donnelly, and Stephen E Russek. Tutorial: High-speed low-power neuromorphic systems based on magnetic josephson junctions. Journal of Applied Physics, 124(16):161102, 2018.

[119] Michael L Schneider, Christine A Donnelly, Stephen E Russek, Burm Baek, Matthew R Pufall, Peter F Hopkins, Paul D Dresselhaus, Samuel P Benz, and William H Rippard. Ultralow power artificial synapses using nanotextured magnetic josephson junctions. Science advances, 4(1):e1701329, 2018.

[120] Furqan Zahoor, Tun Zainal Azni Zulkifli, and Farooq Ahmad Khanday. Resistive random access memory (rram): an overview of materials, switching mechanism, performance, multilevel cell (mlc) storage, modeling, and applications. Nanoscale research letters, 15:1–26, 2020.

[121] ML Schneider and K Segall. Fan-out and fan-in properties of superconducting neuromorphic circuits. Journal of Applied Physics, 128(21):214903, 2020.

[122] Sergey K Tolpygo. Superconductor digital electronics: Scalability and energy efficiency issues. Low Temperature Physics, 42(5):361–379, 2016.

[123] D.E. Kirichenko, S. Sarwana, and A.F. Kirichenko. Zero static power dissipation biasing of rsfq circuits. IEEE Trans. Appl. Supercond., 21:776, 2011.

[124] C. van Vreeswijk and H. Sompolinsky. Chaos in neuronal networks with balanced excitatory and inhibitory activity. Science, 274:1724, 1996.

[125] T.P. Vogels, K. Rajan, and L.F. Abbott. Neural network dynamics. Annu. Rev. Neurosci., 28:357, 2005.

[126] Jennifer Hasler and Harry Bo Marr. Finding a roadmap to achieve large neuromorphic hardware systems. Frontiers in neuroscience, 7:118, 2013.

[127] D.B. Strukov, G.S. Snider, D.R. Stewart, and R.S. Williams. The missing memristor found. Nature, 453:80, 2008.
[138] J.J. Yang, D.B. Strukov, and D.R. Stewart. Memristive devices for computing. Nat. Nanotech., 8:13, 2012.

[139] I. Abraham. The case for rejecting the memristor as a fundamental circuit element. Nature, 8:10972, 2018.

[140] Shihui Yin, Yulhwa Kim, Xu Han, Hugh Barnaby, Shimeng Yu, Yandong Luo, Wangxin He, Xiaoyu Sun, Jae-Joon Kim, and Jae-sun Seo. Monolithically integrated rram-and cmos-based in-memory computing optimizations for efficient deep learning. IEEE Micro, 39(6):54–63, 2019.

[141] Daniele Ielmini. Brain-inspired computing with resistive switching memory (rram): Devices, synapses and neural networks. Microelectronic Engineering, 190:44–53, 2018.

[142] Stefano Ambrogio, Nicola Ciocchini, Mario Laudato, Valerio Mio, Agostino Iprovano, Paolo Fantini, and Daniele Ielmini. Unsupervised learning by spike timing dependent plasticity in phase change memory (pcm) synapses. Frontiers in neuroscience, 10:56, 2016.

[143] Min-Kyu Kim and Jang-Sik Lee. Ferroelectric analog synaptic transistors. Nano letters, 19(3):2044–2050, 2019.

[144] Sun Gil Kim, Ji Su Han, Hyojung Kim, Soo Young Kim, and Ho Won Jang. Recent advances in memristive materials for artificial synapses. Advanced Materials Technologies, 3(12):1800457, 2018.

[145] Yang Zhang, Zhongrui Wang, Jiadi Zhu, Yuchao Yang, Mingyi Rao, Wenhao Song, Ye Zhuo, Xuneng Zhang, Menglin Cui, Linlin Shen, et al. Brain-inspired computing with memristors: Challenges in devices, circuits, and systems. Applied Physics Reviews, 7(1):011308, 2020.

[146] T. Van Duzer and C.W. Turner. Principles of superconducting devices and circuits. Prentice Hall, USA, second edition, 1998.

[147] Alan M. Kadin. Introduction to superconducting circuits. John Wiley and Sons, USA, first edition, 1999.

[148] J.M. Shainline, S.M. Buckley, A.N. McCaughan, J. Chiles, A. Jafari-Salim, R.P. Mirin, and S.W. Nam. Circuit designs for superconducting optoelectronic loop neurons. J. Appl. Phys., page 152130, 2018.

[149] S.K. Tolpygo, V. Bolkhovsky, D.E. Oates, R. Rastogi, S. Zarr, A.L. Day, T.J. Weir, A. Wynn, and L.M. Johnson. Superconductor Electronics Fabrication Process with MoN_x Kinetic Inductors and Self-Shunted Josephson Junctions. IEEE Transactions on Applied Superconductivity, 28(4):1100212, 2018.

[150] V. Brautengb and A. Schuz. Cortex: statistics and geometry of neuronal connectivity. Springer, Berlin, Germany, 1998.

[151] G. Buzsáki. Rhythms of the Brain. Oxford University Press, 2006.

[152] E. Bullmore and O. Sporns. The economy of brain network organization. Nature Reviews Neuroscience, 13:336, 2012.

[153] A. Fronczak, P. Fronczak, and J.A. Holyst. Average path length in random networks. Phys. Rev. E, 70:056110, 2004.

[154] T. Van Duzer and C.W. Turner. Principles of superconducting devices and circuits. Prentice Hall, USA, second edition, 1999.

[155] M. Bota, O. Sporns, and L.W. Swanson. Architecture of the cerebral cortical association connectome underlying cognition. PNAS, page E2093, 2015.

[156] V.B. Mountcastle. The columnar organization of the neocortex. Brain, 120:701, 1997.

[157] K. Friston and G. Buzsáki. The Functional Anatomy of Time: What and When in the Brain. Trends in Cognitive Sciences, 20(7):500, 2016.

[158] R.W. Keyes. The wire-limited logic chip. IEEE J. Sol.-Sta. Circuits, SC-17:1232, 1982.

[159] Johannes Schemmel, Daniel Brüderle, Andreas Grübl, Matthias Hock, Karlheinz Meier, and Sebastian Millner. A wafer-scale neuromorphic hardware system for large-scale neural modeling. In 2010 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1947–1950. IEEE, 2010.

[160] K. Shang, S. Pathak, B. Guan, G. Liu, and S.J.B. Yoo. Low-loss compact multilayer silicon nitride platform for 3D photonic integrated circuits. Opt. Express, 23:21334, 2015.
