A New High-speed Drive Topology of Wide-bandgap Power MOSFET Based on Dynamic Procedure Model

Chuang Zhao¹, ², ³, Wenyong Guo¹, ², ³, *, Wenhan Zha¹, ², ³, Shaoqun Cao¹, ², ³, Benkang Yang¹, ², ³, Huijuan Gao¹, ², ³, Yang Cai¹, ², ³ and Chenyu Tian¹, ², ³

¹University of Chinese Academy of Sciences, Beijing, China
²Institute of Electrical Engineering Chinese Academy of Sciences, Beijing, China
³Key Laboratory of Applied Superconductivity Academy of Sciences, Beijing, China

*Corresponding author e-mail: wyguo@mail.iee.ac.cn

Abstract. More and more attention is being drawn on the wide-bandgap power MOSFET, for its performance is far superior to the traditional silicon MOSFET. Driving technology is one of the key factors that influence the performance of device. In this paper, a high-speed drive circuit topology is proposed. The principle of the improved drive circuit is simple and easy to be implemented. Compared with the traditional design, it can reduce the switching time while maintaining the original driving performance.

1. Introduction

As the performance of silicon MOSFET (Metal-Oxide-Semiconductor Field Effect transistor) gradually reaches the theoretical limit of silicon materials, the development of MOSFETs with wider band gap semiconductor materials such as silicon carbide (SiC) and gallium-nitride (GaN) have become the mainstream development direction [1]. The wide-bandgap (WBG) power MOSFET has the advantages of high breakdown voltage, high operating frequency, high temperature resistance and low on-resistance [2, 3, 4]. The power electronic equipments developed with wide-bandgap power MOSFETs have higher power density, smaller volume, lower loss and stronger high temperature resistance than the traditional equipment of the same power level [5].

Wide-bandgap power MOSFET and silicon MOSFET have the same structure and operating principle, but differ in their semiconductor materials and manufacturing processes [6]. Compared with silicon MOSFET, the wide-bandgap power MOSFET has more stringent requirements for driving [7, 8]. In recent years, many efforts have been made to improve the driving performance of the wide-bandgap power MOSFET. In [9], an optocoupler isolating drive circuit was used, and a capacitor was connected in parallel with the gate and source to suppress oscillation. The additional capacitance increases the input capacitance, which reduces the switching speed and increases of switching loss. A negative voltage clamp drive circuit is presented in [10], which imposes negative voltage on the gate during turn-off process, so as to avoid misfiring device caused by gate voltage oscillation. Increasing the drive resistance method is proposed in [11] to suppress oscillation, which suppresses the transient process. However, it results in decreasing switching speed in [12] and [13], a Zener diode was added on the gate-source side. Once the gate-source voltage is too large, it will break down to prevent the gate-source of the device.
In this paper, a high-speed drive circuit topology is proposed based on the dynamic model of wide-bandgap power MOSFET. The proposed topology can further reduce the switching time and improve the switching reliability of power MOSFET.

2. New high-speed drive circuit topology

Fig. 1(a) shows the proposed drive circuit topology. It includes the original traditional drive circuit (shown in black in Fig. 1(a)) and the additional part (shown in red in Fig. 1(a)). The original traditional drive circuit can have different structures and functions. And the additional part is a current-increasing branch, it can further increase the turn-on speed.

The input signals of the drive circuit are Pulse Width Modulation (PWM) signals. PWM1 is the input drive pulse signal, and PWM2 is the auxiliary turn-on pulse signal. \(U_{gsh1}\) is the auxiliary drive voltage source. The capacitance \(C_{g1}\) acts as the DC power supply when the branch is turned on. \(Q_3\) and \(Q_4\) control the charge and discharge of the capacitance \(C_{g1}\). \(R_{g1}\) is the current-increasing branch resistor.

![Figure 1. The proposed gate drive circuit topology.](image1)

3. Principle Analysis based on Dynamic Procedure Model

The switching process of wide-bandgap power MOSFET is a complex physical procedure. Its external appearance is reflected in dramatic changes in current and voltage. It can be regarded as the charging and discharging process of the varying input capacitance.

During the turn-on procedure, the gate-source voltage will exceed the threshold voltage and eventually reach the set forward drive voltage; the drain current \(I_d\) will rise from zero to the operating current; the drain-source voltage drops to the on-state voltage drop \(U_{ds(on)}\). It can be divided into four phases: Turn-on Delay (0-\(t_1\)), Current Rise Phase (\(t_1\)-\(t_2\)), Voltage Drop Phase (\(t_2\)-\(t_3\)), Overdrive (\(T > t_3\)). Among the three phases, the voltage drop phase plays the dominant role in the turn on procedure.

![Figure 2. Equivalent circuit models of the turn-on procedure.](image2)

In this phase, the channel resistance continues to reduce, and the drain current keeps the operating current (\(I_0\)), resulting in a rapid drop in the drain-source voltage. This stage is also known as "Miller plateau". Fig. 2(c) shows the equivalent circuit model of this stage. At the end of this phase, both the drain current \(I_d\) and the drain-source voltage \(U_{ds}\) reach the working value, the device is fully turned on. \((U_{gel} = \text{drive voltage of turn-off. } I_0 = \text{the operating current. } g_m = \text{the transconductance. } U_{mp} = \text{the Miller plateau voltage. } U_{ds(on)} = \text{the on-state voltage drop between drain and source. } U_{ab} = \text{the voltage applied to the drain electrode. } R_g = \text{the drive resistance. } C_{gs} = \text{the gate-})
source capacitance. $C_{gd}$ is the gate-drain capacitance. $U_{gsh}$ is the drive voltage of turn-on. $I_g$ is the drive current. $I_d$ is the drain current. $I_{gs}$ is the charging current of $C_{gs}$. $I_{gd}$ is the charging current of $C_{gd}$.)

Through the electrical analysis, the equation expressions of the main parameters of the device can be obtained as follows.

$$I_g(t) = \frac{U_{gsh} - U_{dss}}{R_g} - C_{gd} \frac{dU_{ds}}{dt}, \quad t_2 \leq t < t_3$$  \hspace{1cm} (1)

$$U_{ds}(t) = U_{dss} - \frac{I_g(t)}{C_{gd}}(t - t_2), \quad t_2 \leq t < t_3$$ \hspace{1cm} (2)

$$U_{gs}(t) = \frac{I_g}{g_m} + U_{dss} - U_{ds}, \quad t_2 \leq t < t_3 \quad \tau = R_g \left( C_{gs} + C_{gd} \right)$$ \hspace{1cm} (3)

In the time of $t_2$-$t_3$, the decline rate of the drain-source voltage is proportional to the value of the drive current. It is a very important information. It means that increasing the drive current will accelerate the drop of the drain-source voltage. However, it is known that the drive current is inversely proportional to the drive resistance. So increase the drive current is the key to reduce the voltage drop time when the drive resistance is determined.

An auxiliary branch is added in the proposed topology. It can provides an additional drive current $I_x$ during the voltage drop phase, which does not affect other phases. The voltage drop time decreases with the increases of the drive current. It could further reduce the turn-on time without changing the overall structure and performance of the original driver.

![Figure 3](image)

**Figure 3.** Waveform of the key parameters in the turn-on procedure. (The black line is the original driving characteristic. The red line is the improved driving characteristic.)

The effects of the additional current-increasing branch on the drive current, the drain-source voltage, the gate-source voltage and the drain current are shown in Fig. 3. The turn-on time of the proposed drive topology is significantly shortened.

4. Operating procedure

The detail operation of this process can be divided into three stages:

4.1. Stage I: 0-$t_y$

$t_y$ is approximately equal to $t_2$ which is in the turn-on procedure. In the time of 0-$t_y$, PWM1 is high level, $Q_1$ is turned on, and the drive current charges the input capacitance of the MOSFET. PWM2 is high level, $Q_3$ is turned on, and the auxiliary drive voltage source $U_{gsh1}$ charges the auxiliary branch capacitance $C_{g1}$. Fig. 4 (a) shows the equivalent circuit of this period. The variations of the parameters in this stage are the same as those in the phases of turn-on delay and current rise.
4.2. Stage II: $t_1-t_2$

$t_2$ is slightly larger than $t_3$ which is in the turn-on procedure. In the time of $t_1-t_2$, PWM1 remains at the high level, PWM2 becomes low level. Q3 is cut off, Q4 is turned on. The auxiliary capacitor $C_{g1}$ discharges energy to the gate, and provides an auxiliary current $I_x$ for the gate. The value of the drive current increases $I_x$ on the original basis. Fig. 4 (b) shows the equivalent circuit of this period.

4.3. Stage III: $T > t_c$

After the time of $t_c$, PWM2 becomes the high level. Q4 is cut off, Q3 is turned on. Fig. 4 (c) shows the equivalent circuit of this period. The auxiliary branch is cut off, and the value of $I_x$ drops to zero. The auxiliary drive voltage source recharges the capacitor $C_{g1}$.

**Figure 4.** Operating of the proposed gate drive circuit.

5. Simulation Results

The new high-speed drive circuit topology is simulated by PSPICE software. A 650V GaN MOSFET (GS66516B) manufactured by the company of GaN Systems was selected as the device under test. Establish a dual-pulse simulation test circuit (Dual-pulse test circuit is a common method to detect the dynamic performance of power devices).

5.1. Effect of Drive Resistance on Switching-on Time

Fig. 5 shows the switching-on time of different values of drive resistance (1Ω, 3.1Ω, 10Ω, 20Ω, 30Ω, 40Ω, 50Ω). As the value of drive resistance increases, the switching-on time increases. The increase rate of the voltage drop time is greater than that of the current rise time. This means that the value of the drive resistance has a greater impact on the voltage drop time than on the current rise time in the turn-on procedure.

5.2. Optimization of Driving Performance

Fig. 6- Fig. 8 are the changes of driving performance with or without the auxiliary branch.

Fig. 6 shows the change of the drive current $I_g$. The black line is the waveform of the drive current in the original traditional driver. The red line is the waveform of the current in the auxiliary branch ($I_x$). The green line is the waveform of the drive current in the proposed drive circuit. After the auxiliary branch is turned on, an additional drive current (the red line in Fig. 6) is provided to the gate, which increases the drive current of the proposed drive circuit (the green line in Fig. 6).

Fig. 7 shows the change of the drain-source voltage $U_{ds}$. The green line is the drain-source voltage waveform in the original traditional driver. The red line is the drain-source voltage waveform in the proposed drive circuit. The drop rate of drain-source voltage increases due to the increasing drive current increases, just as shown in equation (2). The change brought about by the auxiliary branch is obvious.

Fig. 8 shows the change of the gate-source voltage $U_{gs}$. The green line is the gate-source voltage waveform in the original traditional driver. The red line is the gate-source voltage waveform in the proposed drive circuit. The Miller platform time is significantly reduced.
5.3. Turn-on Time

Table 1 shows the changes of turn-on time with or without the auxiliary branch. The proposed drive circuit can significantly reduce the turn-on time. When drive resistance is 10Ω, the turn-on time is reduced by 6.4 nanoseconds, which is a decrease of 41%, and the voltage drop time is reduced by 56.6%.

|                   | Traditional | Improved | Ton (ns) | Tri (ns) | Tfu (ns) |
|-------------------|-------------|----------|----------|----------|----------|
| Rg = 10Ω          |             | Rg = 10Ω | 15.6     | 4.3      | 11.3     |
|                   |             | Rg = 20Ω | 31.3     | 8.7      | 22.6     |

Table 1. Statistics of turn-on time
When drive resistance is 20Ω, the turn-on time is reduced by 17.2 nanoseconds, which is a decrease of 55%, and the voltage drop time is reduced by 76%.

6. Conclusion
A New high-speed drive circuit topology is proposed. Compared with the original driver, the improved drive topology can further reduce the switching time on the basis of the original driving performance. The simulation results prove the effectiveness of this improvement. The proposed idea in this paper can provide reference for the drive circuit design of the wide-bandgap power MOSFET in the future.

Acknowledgments
This work was financially supported by the National Key Research and Development Program of China under Grant 2018YFB0905800 and the National Natural Science Foundation of China under Grants 51877206 and 51721005.

References
[1] F. Iacopi, M. Van Hove, M. Charles, and K. Endo, “Power electronics with wide bandgap materials: Toward greener, more efficient technologies,” MRS Bull, vol. 40, no. 5, pp. 390–395, 2015.
[2] J. Rabkowski, D. Pefitisis, and H.-P. Nee, “Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated,” IEEE Ind. Electron. Mag, vol. 6, pp. 17–26, Jun. 2012.
[3] L. F. Eastman and U. K. Mishra, “The Toughest Transistor Yet [GaN Transistors],” IEEE Spectrum, vol. 39, pp. 28–33, May 2002.
[4] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, “SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors,” Industrial Electronics, IEEE Transactions on, vol. 58, no. 7, pp. 2872–2882, 2011.
[5] A. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, “Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges,” IEEE Transactions on Transportation Electrification, 2019:1-1
[6] Z. M. Chen and S. Z. Li, "Wide Band-gap Semiconductor Power Electronics Devices and Applications," China Machine Press, 2009.
[7] H. Muhsen, J. Lutz, S. Hiller, "Design and Evaluation of Gate Drivers of SiC MOSFET," Pcm Europe ; International Exhibition & Conference for Power Electronics. VDE, 2015.
[8] J. Yuan, "Research on Driving Technology of SiC MOSFETS," Ph.D. dissertation, Beijing Jiaotong University, 2015.
[9] O. Stalter, B. Burger, S. Lehrmann, "Silicon Carbide (SiC)D-MOS for grid-feeding solar-inverters," 2007 European Conference on Power Electronics and Applications, pp. 1517-1526, 2007.
[10] Z. Chen, M. Danilovic, D. Boroyevich, Z. Shen, "Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," Proceedings of the 2011-14th European Conference on Power Electronics and Applications, pp. 1-10, 2011.
[11] X. Zhang, M. Chen, and D. Xu,"Driving Circuit and Experimental Analysis of SiC MOSFET." Journal of Power Supply, vol. 3, pp. 71-76, 2013.
[12] F. Liu, L. Xiao,"Switching Characteristics and Driving Circuit Design of SiC MOSFET", vol. 50, no. 6, pp. 101–104, 2016.
[13] K. Haehe, B. Wild, W. Heering, C. Simon, and R Kling. "Design of a 5-MHz-Gate-Drive for SiC-MOSFETs," 7th IET International Conference on Power Electronics, Machines and Drives, 2014.