An 82.3- to 87.4-GHz modified differential Colpitts VCO in 0.18-µm CMOS

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Abstract: A millimeter-wave 0.18-µm CMOS VCO with measured oscillation frequency from 82.25 to 87.43 GHz is presented in this paper. In this work, three varactor rows are utilized to improve the VCO tuning range. The first varactor row is deposited at bottom of the cross-coupled pair for alleviating the loading effect on the VCO core. Moreover, the other two varactor rows are connected between the drain and source terminations of the cross-coupled pair for enhancing the tuning range. Compared to conventional differential Colpitts VCO, the loading effects on VCO core can be effectively alleviated. In addition, due to the second-harmonic superposition technique, the signal strength of the output signal (2f₀) can be enhanced. The enhanced 2f₀ output signal is extracted from the middle of the varactors, resulting in an elimination of the required λ/4 microstrip or coplanar waveguide (CPW) line for a RF choke. This leads to a minimized chip size of 0.549 mm². Based on the proposed VCO architecture, the fabricated 0.18-µm CMOS VCO core consumes 5.8-mW low dc power at 1.0-V supply voltage. At this bias condition, the measured phase noise is −77.92 dBc/Hz at 1-MHz offset from an 84.02-GHz carrier, and the tuning range is 6.11%. Notably, this modified differential Colpitts VCO demonstrates the highest operation frequencies (82.25 GHz to 87.43 GHz) among previously published 0.18-µm CMOS VCOs.

Keywords: coplanar waveguide (CPW), differential Colpitts VCO, voltage-controlled oscillator (VCO)

Classification: Microwave and millimeter wave devices, circuits, and systems

References

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1 Introduction

Requirements of high-speed integrated circuits for microwave and millimeter wave applications are accelerated. The most effective way to generate high-frequency oscillation signal is utilizing push-push VCO topology [1, 2, 3, 4, 5]. In [1], a positive feedback type push-push VCO is presented. Phase shifters are connected in series with the feedback loop for adjusting the oscillation frequency. The high-electron-mobility transistors (HEMTs) were used as the active devices for signal generation, and the diodes (M/A COM, MA46H120) were operated as the varactors. The hybrid circuits were integrated on a 0.8-mm-thickness dielectric substrate, and the measured second-harmonic output signal ($2f_o$) is 21 GHz.

To deliver $2f_o$ output frequency in V band (50 to 75 GHz), the coplanar waveguide (CPW) and asymmetrical coplanar strip are combined with a cross-coupled pair [2]. In addition, the $\lambda/4$ line is implemented with CPW and connected to a bypass capacitor for performing the RF choke. Therefore, the fabricated push-push VCO can operate from 62 to 66.5 GHz in V band. In [4], the VCO core utilizes a self-bias technique to reduce the parasitic effects and enhance the tuning range. Based on this technique, the push-push VCO can oscillate from 64.2 to 69.4 GHz at 1.2-V supply voltage. However, an RF choke, composed of a bypass capacitor and a $\lambda/4$ microstrip or CPW line, is needed for providing a dc current path and high impedance at the $2f_o$ output frequency [1, 2, 3, 4]. The implemented $\lambda/4$ microstrip or CPW line in silicon is about several hundreds of micrometers in length, occupying a considerable chip size.

To overcome the difficulty, the $2f_o$ output frequency is extracted from the middle of the varactors, leading to a reduced chip size and design complexities [5]. In this work, an 82.25- to 87.43-GHz 0.18-µm CMOS VCO have been designed, fabricated, and measured. According to the authors’ knowledge, the presented VCO demonstrates the highest operating frequency among previously published 0.18-µm CMOS VCOs.

2 Circuit design

Fig. 1 shows the circuit schematic of a regular differential Colpitts VCO. It consists of a cross-coupled pair, a row of varactor ($C_{VAR}$), and three capacitors. Although the Colpitts VCO can achieve low phase noise due to the good mechanism of impulse sensitivity function (ISF), the varactors connected at the drain terminations of the MOSFET (M3-M4) arises the loading effects of the VCO core.
In order to alleviate the loading effects, the varactor row is connected on the source terminations of the MOSFET (M1-M2), as shown in Fig. 2. Moreover, the varactor rows are deposited between the drain and source terminations of the MOSFET (M1-M2) to increase the tuning range. Furthermore, due to the second-harmonic superposition technique, the signal strength of the output signal \((2f_0)\) can be effectively enhanced. In addition, the enhanced \(2f_0\) output signal is extracted from the middle of the varactors, resulting in an elimination of the required \(\lambda/4\) microstrip or coplanar waveguide (CPW) line for the RF choke. This leads to a minimized chip size of 0.549 mm\(^2\) for this work. Table I lists the circuit parameters of the proposed 82.25- to 87.43-GHz modified Colpitts VCO.

To improve the VCO operation frequency from [5], the considerations of maximum available gain (MAG)/maximum stable gain (MSG) of the device size for VCO cores are shown in Fig. 3. Moreover, the fundamental oscillation frequencies of the VCOs in [5] and this work are around 38.9 GHz and 43.5 GHz, respectively. From Fig. 3, it is observed that the device size of four fingers with total device size of 12 µm (4f12) in this work achieve higher MAG/MSG than that of 6f12 in [5]. Furthermore, the 0.208-nH inductor (\(L_{D1}\)) of VCO [5] shown in Fig. 4(a) are reduced to 0.14-nH inductors (\(L_{D1}\)), as shown in Fig. 4(b). The minimized the inductor (\(L_{D1}\)) is with lower parasitic capacitance between the passive components and lossy silicon substrate, leading to an improve VCO operation frequency. According to these techniques, the measured operation frequency of the proposed VCO is significantly improved from 77 GHz in [5] to 87 GHz.

To minimize the supply voltage (\(V_{DD}\)) and dc power consumption, the supply voltage of the proposed 87-GHz VCO is reduced from 1.2 V of in [5] to 1.0 V, as shown in Fig. 2. In addition, the corresponding dc power consumption of VCO core is reduced from 7.5 mW of [5] to 5.8 mW in this work.
Table I. Circuit parameters of the proposed VCO

| Device          | Design Value          |
|-----------------|-----------------------|
| $M_1, M_2$      | 12 µm/0.18 µm         |
| $M_3, M_4$      | 12 µm/0.18 µm         |
| $C_{var1}, C_{var2}$ | 32 µm/0.25 µm      |
| $C_{var3}, C_{var4}$ | 20 µm/0.25 µm       |
| $C_{var5}, C_{var6}$ | 20 µm/0.25 µm       |
| $L_{D1}$        | 0.14 nH               |
| $L_S$           | 0.2 nH                |

Fig. 2. Schematic of the proposed 82.25- to 87.43-GHz modified differential Colpitts VCO in 0.18-µm CMOS.

Fig. 3. Simulated MAG/MSG.
3 Measured results

Fig. 4 shows the microphotographs of the proposed 87-GHz VCO and 77-GHz VCO in [5]. From this figure, it is observed that the fabricated 77-GHz VCO in [5] is with an overall chip size of $0.66 \times 0.94 \text{mm}^2$ ($= 0.62 \text{mm}^2$). In addition, the overall chip size including the testing pads is $0.695 \times 0.79 \text{mm}^2$ ($= 0.55 \text{mm}^2$) in this work. The passive components and routing of the VCO core in this work are compact. Moreover, the distance between the dc pads in the low row and RF pads are reduced, leading to a chip size reduction from $0.62 \text{mm}^2$ in [5] to $0.55 \text{mm}^2$ in this work, as shown in Fig. 4. Furthermore, the on-chip passive components including inductors, capacitors, and interconnections are simulated by adopting full-wave electronic-magnetic (EM) simulation tool in detail. The comparison of the chip size for VCO core area is shown in Table II. From this table, it is observed that the chip size for VCO core area in ref. [4], ref. [5], and this work are $0.1344 \text{mm}^2$, $0.068 \text{mm}^2$, and $0.065 \text{mm}^2$, respectively. Therefore, the chip size for VCO core area is more compact than that of other circuits.

![Microphotographs](image)

Fig. 4. Microphotographs of the (a) fabricated 77-GHz VCO with the overall chip size of $0.66 \times 0.94 \text{mm}^2$ ($= 0.62 \text{mm}^2$) in ref. [5], and (b) fabricated 87-GHz VCO with the overall chip size of $0.695 \times 0.79 \text{mm}^2$ ($= 0.55 \text{mm}^2$) in this work.

Table II. Comparison of the chip size of core area for VCOs.

|          | Unit (mm$^2$) |
|----------|--------------|
| Ref. [4] | 0.1344       |
| Ref. [5] | 0.068        |
| This Work| 0.065        |
To evaluate the high-frequency performance, the output spectrum and phase noise were characterized by a 50-GHz spectrum analyzer with an external harmonic mixer for W band measurement (75 to 100 GHz). On-wafer probing was used to test the VCO performance. The losses of the experimental setups were de-embedded and calibrated in the measurement results.

While operating at the supply voltage ($V_{DD}$) of 1.0 V, the VCO cores (M1-M2) consumes total 5.8 mW. Fig. 5 shows the characterized oscillation frequency of this VCO. While sweeping the control voltage ($V_{ctrl2}$) from −0.8 V to 1.8 V and $V_{ctrl1}$ from −0.6 V to −0.3 V, the measured operation frequency is from 82.3 to 87.4 GHz, exhibiting a tuning range of 6.11%. Fig. 6 shows the characterized VCO output power over all operation frequency. At this bias condition, the measured output spectrum of the fabricated VCO is shown in Fig. 7. From this figure, it is observed that the output power is −47.27 dBm at 84.1 GHz. Fig. 8 shows the measured phase noise of the fabricated VCO. It is indicated that the phase noise is −77.92 dBc/Hz at 1-MHz offset from the 84.02-GHz carrier. Fig. 9 depicts the recorded high-frequency 0.18-μm CMOS

![Fig. 5](image1.png)

**Fig. 5.** Measured oscillation frequency of the presented VCO.

![Fig. 6](image2.png)

**Fig. 6.** Measured output power of the presented VCO.
Fig. 7. Measured output spectrum of the fabricated VCO.

Fig. 8. Measured phase noise of the fabricated VCO.

Fig. 9. Recorded high-frequency 0.18-µm CMOS VCO.
VCOs. It is found that this work demonstrated the highest operation frequency. Table III summarizes the measured performance of this VCO. It is indicated that this VCO can operate at millimeter-wave frequency with low dc supply voltage and low dc power consumption.

4 Conclusion

A modified differential Colpitts VCO in 0.18-µm CMOS with operation frequency from 82.25 to 87.43 GHz is demonstrated. Using varactors connected the source terminations of the cross-coupled pair, the loading effect on the VCO core can be effectively alleviated, leading to the high operation frequency. Moreover, the VCO tuning range is enhanced by adopting two varactor rows connected between the drain and source terminations of the cross-coupled pair. Furthermore, an enhanced second harmonic signal is extracted from the middle of the varactors to eliminate the λ/4 microstrip or coplanar waveguide (CPW) line from a regular push-push VCO, leading to a minimized chip area. Notably, this modified differential Colpitts VCO in this work demonstrates the highest operation frequencies (82.25 GHz to 87.43 GHz) among previously published 0.18-µm CMOS VCOs.

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Table III. Performance summarized of the fabricated VCO.

| Performance                        | Value                        |
|------------------------------------|------------------------------|
| Frequency                          | 82.25 to 87.43 GHz           |
| Tuning Range                       | 6.11%                        |
| Phase Noise at 1-MHz Offset        | −77.92 dBc/Hz                |
| VDD                                | 1.0 V                        |
| DC Power                           | 5.8 mW                       |
| Chip Size                          | 0.549 mm²                    |

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