Phase-Change Logic via Thermal Cross-Talk for Computation in Memory

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Herein, logic function implementations are computationally demonstrated using lateral and vertical multicontact phase-change devices integrated with complementary metal–oxide–semiconductor (CMOS) circuitry, which use thermal cross-talk as a coupling mechanism to implement logic functions at smaller CMOS footprints. Thermal cross-talk during the write operations is utilized to recrystallize the previously amorphized regions to achieve toggle operations. Amorphized regions formed between different pairs of write contacts are utilized to isolate read contacts. Typical expected reduction in CMOS footprint is ~50% using the described approach for toggle-multiplexing, JK-multiplexing, and 2 × 2 routing. The switching speeds of the phase-change devices are in the order of nanoseconds and are inherently nonvolatile. An electrothermal modeling framework with dynamic materials models is used to capture the device dynamics, and current and voltage requirements.

Typical data-heavy computations are limited by memory access latencies due to the input/output bottleneck to dynamic random access memory (DRAM), flash memory, and hard drive.[1,2] If large amounts of high-speed nonvolatile memory (100s of GBs) could be integrated atop the central processing unit (CPU), the need for off-chip DRAM, hard drive (storage), and even motherboard could be eliminated for some applications. These computer-on-chip and computation-in-memory approaches can achieve significant speed improvements at a fraction of the power for data intensive computations.

Silicon complementary metal–oxide–semiconductor (CMOS) is still at the forefront of scaling, driving process technologies, which also enables integration of complementary nanoscale nonvolatile resistive random access memory (RRAM) technologies such as phase-change memory (PCM)[3] (Figure 1) or conductive bridging RAM (CBRAM).[4–7] RRAM structures are compact 2-terminal devices that utilize reversible changes in resistance of a small volume of material through 1) electrothermal effects by changing a materials phase between amorphous and crystalline (PCM)[1,3,8–11] 2) electrochemical effects by formation of metallic filaments in nonconductive thin layers[4–7] or generation and annihilation of oxygen vacancies in metal oxides[12–17] (CBRAM); or 3) magnetic switching (magnetoresistance) as in magnetic RAM (MRAM).[18]

All RRAM devices experience joule heating,[19–24] electrical breakdown,[25] thermal transport,[26,27] thermoelectric effects,[19,20,28,29] electromigration,[30,31] and percolation transport,[16,17,32] which make them harder to model compared with conventional electronic devices.[33–37] However, their compatibility with backend-of-the-line low-temperature processing makes them very attractive.

Typical PCM devices are vertical mushroom cells (Figure 1) composed of a bottom-contact, a shared top-contact, and a phase-change material that offers a large resistivity (ρ) contrast between the amorphous (a-GST) and crystalline (x-GST) phases, such as Ge2Sb2Te5 (GST).[33,38–41] The set and reset operations are achieved through localized self-heating via short voltage pulses (Vpulse) to transition between the set (crystalline) and reset (amorphous) states. These devices can provide ~106–108× contrast in total device resistance[9] (kΩ to MΩ range), cycled >1012 times[42] (flash memory can be cycled ~109–1010 times)[43] and retain data for >10 years at CPU temperature. Memory window increases over time due to upward drift of the ρa-GST.[44,46] This resistance drift limits the multibit-per-cell implementation of conventional PCM cells. Cells with shunt resistances are demonstrated to overcome this difficulty.[42] The high-density PCM implementations typically use ovonic threshold switches (OTS) as the access devices in cross-bar architecture.[47–50]

Emergence of PCM as a viable memory technology has sparked interest in its implementation as switches[31] as well as components of neural networks complementing CMOS circuitry.[9] Complementing CMOS circuitry with functional phase-change elements in the memory layer to achieve memory control, multiplexing, routing, and neuromorphic computations will relieve the area concerns in the underlying CMOS layer, making it easier to realize computer-on-chip and computation-in-memory as well as hardware implementation of artificial neural networks (Figure 2).

The multicontact phase-change devices described in this article can be used to implement flip-flops,[52] routers,[53,54] multiplexers,[55] counters, and state machines at a smaller CMOS footprint as discussed later. These nonconventional phase-change devices can be integrated with CMOS access devices to offer more functionality and/or reduced area compared with conventional nonvolatile memory devices and CMOS circuitry, and can also enable computations using intermittent power.

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssr.202000422.

DOI: 10.1002/pssr.202000422

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Phys. Status Solidi RRL 2021, 15, 2000422

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Multicontact phase-change elements offer the possibility to implement functions and reconfigurable routing, going beyond conventional PCM devices. The main drawback for all phase-change logic, similar to other non-CMOS approaches, is the inability to amplify the signal back to the supply level ($\pm V_{DD}$). However, complementing CMOS with multicontact phase-change elements offers significant advantages in logic circuit footprint (area) and standby power. The multicontact phase-change elements described here utilize: 1) localized heating to amorphize portions of a phase-change patch to isolate read contacts; 2) thermal cross-talk to crystallize an amorphous region when a nearby area is being amorphized.

A family of lateral (Figure 2) and vertical phase-change logic devices and circuits can be implemented using these processes. The basic circuit configuration and operation of a toggle (T-) multiplexer is shown in Figure 2b,c and Figure 3. This six-contact device, interfaced with five metal–oxide–semiconductor field-effect transistors (MOSFETs), isolates the output ($Y$) from one of the inputs ($X_1, X_2$) by amorphizing a region between two write contacts each time a write signal ($A$) is received (Figure 2c). The geometry of each amorphized region is affected by the thermal losses and the current path, which tends to form a filament due to thermal runaway as polycrystalline phase-change materials become more conductive at elevated temperatures.

When the cell is written the very first time, two parallel high current density paths are formed between top and bottom write terminals. If the two top-contacts are shorted as shown (Figure 2b), the path which heats up slightly more experiences thermal...
runaway and melts (Figure 3b). Upon rapid termination of the write pulse, the molten path becomes amorphous, isolating one of the read contacts (Figure 3c). When the same write pulse is applied again, current predominantly flows through the second path, which was not amorphized previously (Figure 3d). The write pulse is kept long enough to recrystallize the previously amorphized region. Therefore, when the second write pulse is terminated, the second current path is amorphized and the first path is crystallized (Figure 3e). The interaction between the two paths through thermal cross-talk gives rise to the toggle operation. The device remains in the "read" state whenever it is not receiving a write pulse, controlled by the CMOS access circuitry. We demonstrate the toggle operation of the six-contact device in a circular geometry using our electrothermal finite element modeling framework with dynamic materials.\[35–37,63\]

The access devices, electrical waveforms, device geometry, and thermal losses have to be designed appropriately to achieve the desired operation.

It is possible to achieve a deterministic initial state by breaking the symmetry either through increased series resistance for one of the write contacts or an asymmetric phase-change device geometry. One example of such an asymmetric device is shown in Figure 2d. Here, two separate paths of different lengths are defined between two pairs of write contacts. These seven-contact structures can also be used to realize a JK flip-flop where the two of the write terminals (J and K) are accessed by independently controlled MOSFETs (Figure 2d).

Implementation of the six-contact phase-change logic + CMOS as a toggle multiplexer yields \(\approx 50\%\) less footprint compared with its conventional CMOS counterpart (Figure 4), accounting for the increased widths for the MOSFETs used for write access. The conventional CMOS JK-multiplexer requires 18 transistors, while the PCM-JK multiplexer requires only six transistors, corresponding to \(\approx 66\%\) savings in footprint. The PCM-logic alternatives come with the added advantage of nonvolatility, which makes these circuits good alternatives for intermittent power applications (sensor networks) where conventional CMOS circuits would need frequent write/read access to nonvolatile memory to successfully complete the computation between unpredictable intermittent power periods.

**Figure 3.** Crystallinity profiles and temperature contours as the device is cycled with \(W_1\), \(W_2\), and \(W_3\). Grain orientation is plotted in light rainbow (component \(C_{D1}\) of the crystal density), amorphous in peach, and melt in pink. The same signal is applied to \(W_1\) and \(W_2\) for each melt/quench cycle. Initially, the heating is symmetric, but a single path soon dominates. After the device cools, the next pulse is applied and current flows through the more conductive crystalline path, while thermal cross-talk between the two paths crystallizes the previously amorphous area.

**Figure 4.** Layouts illustrating the 50% area reduction using the phase-change T-flip-flop using six transistors (left) compared with the conventional T-flip-flop built with four NOT AND gates (right). Both offer the same logic functionality.
Each lateral phase-change element can also be configured to have a larger number of contacts as in the case of the ten-contact structure, as shown in Figure 2e. Connecting the two side contacts (S1 and S2) together yields a 2 × 2 router that is configured by four contacts (Figure 5), an alternative to a cylindrical structure. This device can be configured with high-speed sequential pulses to amorphize the paths between the top- and bottom-contact pairs, avoiding recrystallization of the paths formed earlier. Reconfiguration can be achieved by keeping the first pulse sufficiently long to recrystallize the areas amorphized in the last pulse sequence. The snapshots in Figure 5 show the thermal profiles during configuration and the resulting resistivity maps corresponding to the applied pulse sequences. Here, the two configurations implement \( \{Y_1 = X_1, Y_2 = X_2\} \) (through) and \( \{Y_1 = X_2, Y_2 = X_1\} \) (swap). A wider contact is used on the left side to reduce electrical resistance.

A subsection of these ten-contact structures (Figure 3c) can be used to implement toggle operations as in Figure 3a,b with nearest neighbor interactions. Larger structures with phase-change strips with large number of contacts on two sides can also be envisioned for this purpose.

Vertical multicontact phase-change devices can also be used to implement logic functions similar to lateral multicontact devices. An example of such a structure is a side-by-side double mushroom device with three contacts accessed with six MOSFETs (Figure 6). Here, the read and the write operations are achieved through the same contacts. Therefore, the write and read access MOSFETs are tied to the same contacts. The toggle operation is achieved through cross-talk between the two mushroom cells each time the toggle signal (A) is applied to the gates of the MOSFETs. Some of the access MOSFETs such as the pass transistor in Figure 6a can be replaced with OTS devices to save area. However, introduction of such nonlinear devices requires variable voltage operation such as in conventional and multibit-per-cell PCM devices. In this study, possible rail-to-rail implementations are the main focus.

While established functions can be implemented using these device concepts, they are intended to be enabling technologies rather than become a replacement technology, and therefore go beyond what is typically achievable by integration of nonvolatile memory elements with CMOS.

The typical supply voltages (\( V_{\text{supply}} \)) needed for the devices discussed here are 2–3.3 V and the structures are designed for 10 nm minimum feature size. It is possible to achieve lower voltage and faster operation than what is demonstrated in the aforementioned examples by using higher growth velocity materials such as Ag–In–Sb–Te alloys instead of GST, thermal engineering of the structure, sizing the access devices, and engineering the write pulses. While it is typically assumed that reset operation requires melting, it is possible to amorphize grain boundaries and interfaces at temperatures substantially below bulk melting temperature \( (T_{\text{MELT}}) \). It is also possible to amorphize at lower temperatures by substantial hole injection at steep thermal gradients or junctions, through impact ionization by high-voltage short duration pulses.

PCM cells have been demonstrated with endurance >10^{12} cycles, while 10^{15}–10^{17} cycles of endurance are necessary to achieve logic operations at the CPU clock speed. The typical PCM cell failures are due to void formation and elemental segregation. The lateral devices described here differ from the compact two-terminal vertical cells in two ways that make them more resilient: 1) devices utilize thermal cross-talk, therefore

![Figure 5](https://www.advancedsciencenews.com)

**Figure 5.** Sequence of write pulses applied and the corresponding thermal profiles and resistivity maps at the indicated times. Simulated thermal profile during a write pulse (left) and the resulting resistivity map during the read cycle (right) for a planar ten-contact router. All contacts other than the left contact is designed to be 10 nm. The side contacts are electrically short circuited through a wire. Sizing one of the side contacts wider than the other is desired to decrease the electrical resistance. Blocking of the narrower side contact with amorphized GST is sufficient to electrically isolate the two sides. Electrothermal model with effective media approximation used for these simulations. a) In the first set of write pulses, electrical paths in GST between \( W_1 \) and \( W_4 \) and \( W_2 \) and \( W_3 \) are amorphized one at a time with high-speed sequential pulses. The device is set to the \( Y_1 = X_1, Y_2 = X_2 \) state. b) In the second set of electrical pulses, electrical paths between \( W_1 \) and \( W_3 \) and \( W_2 \) and \( W_4 \) are amorphized setting the device to the “swap” \( Y_1 = X_2, Y_2 = X_1 \) state.
dielectric breakdown is not required for recrystallization and the structure does not experience fields as strong as conventional cells that drive elemental segregation. 2) These lateral structures deliver the same functionality even if there is a high density of voids in the phase-change material (Figure 7). The devices can also be perforated by etching a pattern formed by block copolymers and capped after crystallization for controlled densification of the GST thin films, and for distribution of the mechanical stresses to avoid formation of large voids.

The electrothermal model we have constructed to simulate phase-change device operation self-consistently solves the heat transfer (1) and current continuity (2) equations, using the COMSOL Multiphysics finite element tool. The electrothermal model and the materials’ parameters are described in detail in our recent publications. Access transistors are integrated with the finite element simulations by using the basic nFET circuit model available in COMSOL.

\[ \frac{dG}{dt} C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = -\nabla \cdot \left( \hat{\phi} (q V + q \Pi) \right) \]

Heat absorbed
Heat loss through conduction
Energy flux

\[ = -\nabla \cdot \left( \hat{I} (V + \Pi) \right) = -\nabla \cdot \left( \bar{J} V \right) - \nabla \cdot \left( \bar{J} \Pi \right) \]

Joule heating
Thermoelectric heat

\[ \nabla \cdot \bar{J} = -\nabla \cdot \sigma(T) V V - \nabla \cdot \sigma(T) S T V = 0 \]

Ohm’s law
Seebeck current

where \( d_G \) is the mass density, \( C_p \) is the heat capacity, \( k \) is the thermal conductivity (including electronic and lattice contributions), \( \hat{\phi} \) is the charge carrier flux, \( q \) is the elementary charge, \( V \) is the electric potential, \( \Pi = ST \) is the Peltier coefficient, \( S \) is the Seebeck coefficient, \( T \) is temperature, and \( \sigma \) is the electrical conductivity. This model accounts for the thermoelectric effects through the introduction of the Seebeck current term in (1) and the Thomson heat term in (2). We include thermal boundary resistances to account for reduced thermal conductivity at the interfaces and a field-dependent electrical conductivity component for phase-change material to capture dielectric breakdown (set operation). The electrothermal model and the materials’ parameters are described in detail in our recent publications. Access transistors are integrated with the finite element simulations by using the basic nFET circuit model available in COMSOL.
The dynamic materials modeling is handled through a rate Equation (3) using published nucleation rates and growth velocities, either using a course mesh modeling a large volume, or using $\approx 1$ nm mesh to capture discrete nucleation

$$\frac{dCD}{dt} = \text{Nucleation}(T, CD, \text{random}) + \text{Growth}(T, CD) + \text{Amorphization}(T, CD)$$

This approach is significantly more efficient compared with discrete nucleation models using individual domains to define the material characteristic. The models used for Figure 6 include grain boundary amorphization which initiates amorphization at the grain boundaries and material interfaces as we describe in the study by Scoggin et al. and accounts for latent heat of fusion as we describe in the study by Scoggin and co-workers.

We have demonstrated that the thermoelectric contribution is substantial, therefore there is a significant impact of the device polarity through our computational studies, as was also experimentally demonstrated by others. Changing the contact material does not only impact cell resistance and thermal losses, but also the thermoelectric heating of the active area. The out of plane thickness used for simulations is 20 nm.

Thermal cross-talk in phase-change devices can be utilized as a coupling mechanism to achieve logic functions and decrease the CMOS footprint necessary for high-density PCM arrays. Multicontact devices utilizing thermal cross-talk integrated with CMOS allow rail-to-rail operation and significantly reduce the area necessary to implement logic functions and routing for memory access. The switching speed of these devices are comparable to PCM switching speeds and these devices are suitable for memory control and routing. Therefore, the presented approach to reduce CMOS resources can enable computer-on-chip implementations with very high-density nonvolatile storage monolithically integrated with logic in a single chip.

Acknowledgements

This work was performed with support of US National Science Foundation grant # ECCS 1150960 and ECCS 1711626.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrothermal modeling, phase-change logic, phase-change memory, routers, toggle multiplexers

Received: September 2, 2020
Revised: November 16, 2020
Published online: December 10, 2020

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