Structural Characterization on Different Type of Silicon Wafer on The Formation of Porous Silicon Structure

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Abstract. A set of n-type and p-type porous silicon (PS) layers were fabricated by photoelectrochemical etching using direct current (DC) and pulse current (PC) techniques. The study aims to compare the effect of different wafer type on the formation of the PS structure. The samples were etched in a solution of HF:C2H6O with a composition ratio of 1:4. All the samples were etched at a current density of J = 10 mA/cm2 for 30 minutes. During the PC etching process, the current was supplied through a pulse generator with 14 ms cycle time (T) which the on time (T_on) set to 10 ms and pause time (T_off) set to 4 ms respectively. The samples were then being characterized in terms of surface morphology by using FESEM, EDX, AFM and XRD. The FESEM results indicates that the p-type porous silicon structure produces more uniform structure as compared to the n-type porous silicon structure. On the other hand, XRD results shows that the intensity of p-type porous silicon exhibited higher intensity as compared to n-type porous silicon for both etching techniques applied for fabricating the porous structure.

1. Introduction
Silicon is one of the most basic material for semiconductor which is unstable for optoelectronic application due to its poor properties such as indirect band gap. Therefore, many works on improving the properties of silicon for example light emission properties of silicon has been done in low-dimensional silicon such as porous silicon [1]. Besides that, having a unique property such as high resistivity and wide energy bandgap has make porous silicon suitable for photo-detectors application [2]. Advances in porous silicon-based technologies depending on the possibilities to form porous silicon layers with high degree of reproducibility. There are many etching techniques can be used to form a porous silicon structure under different conditions. One of the common methods that has greatly been used for porous silicon fabrication is electrochemical etching where a constant current density source was applied in HF electrolyte [3-5]. In this project, the porous silicon was fabricated by using pulse current etching technique. The pause time (T_off) has a significant effect on the size of pores and porosity formation which can improve the porosity of the porous silicon [6]. Other than pulse current etching technique, the common technique used were direct current (DC) anodic etching technique where the parameters such as current density and etching time maintained for both etching techniques. Hence, the
comparison between the two techniques DC and pulse involving different doping type of wafers will be observed and investigated in terms of its structural characterization.

The structural characterization of each samples were done by using Field Emission Scanning Microscopy (FESEM), Energy Dispersive X-Ray (EDX), Atomic Force Microscope (AFM) and High Resolution X-Ray Diffraction (HR-XRD). The FESEM analyzed the pore structure and surface morphology while the composition of each elements of the fabricated samples were analyzed by EDX. The surface morphology of the PS samples were then being observed by using AFM where a damage on the sample surfaces can be prevented by applying tip scanning using “tapping” mode. The degree of crystallinity for the fabricated PS samples were analyzed using HR-XRD spectrum.

2. Experimental Procedures

In this research work the n-type Si (100) and p-type Si (100) were cleaved into square shape with dimension of 10 mm × 10 mm. The procedure begins with RCA cleaning process which involves three (3) process using different solution. The first process uses a mixture of H₂O:NH₄OH:H₂O₂ with ratio 5:1:1 and the second process uses a mixture of HF:H₂O with ratio 1:50. The last cleaning process uses a mixture of H₂O:HCL:H₂O₂ with ratio 6:1:1. The cleaned wafers were then being etch in a cell filled with electrolyte solution consist of HF (49 %), ethanol (95 %), and hydrogen peroxide (H₂O₂) with the volume ratio of 1:2:2.

Figure 1 shows the schematic diagram for the etching process setup. All the samples were etched using two different technique, DC etching and pulse etching technique. The two samples (PDC & NDC) for DC technique were being etched with supplied current of 10 mA for 30 minutes. Whereas the other two samples (PPC & NPC) for pulse technique were being etched with etching parameters of pulse current with total cycle time, T = 14 ms for 30 minutes where applied pause time, T_{off} = 4 ms. All these samples were etched at room temperature inside fume chamber. Hence, all the samples were rinsed with deionized (DI) water after the etching process.

3. Results and discussion

The FESEM image shown in Figure 2 describes the formation of pores structure of the fabricated samples, P-type direct current (PDC), N-type direct current (NDC), P-type pulse current (PPC) and N-type pulse current (NPC). Figure 2(a) PDC and Figure 2(c) NDC represent the samples fabricated using DC etching while Figure 2(b) PPC and Figure 2(d) NPC represent the samples fabricated using PC etching. The FESEM image shows that P-type wafer form a circulate pores structure for both etching techniques used. The uniformity has increased when the pulse current technique being applied to the P-type wafer (PPC, which is shown in Figure 2(b). The application of pulse current etching technique did affect the formation of pores structure by referring to Figure 2(b) PPC and Figure 2(d) NPC where the pores become homogeneous as compared to the samples fabricated by using DC etching technique. The
non-uniformly etched pores produced for both samples which has been etched by DC etching technique were due to the hydrogen bubbles formation on the surface of the substrate which is in agreement with the work reported by Amran et. al [6]. However, the improvement in the uniformity of the pores structure during PC etching technique is believed to be caused by the reaction of the HF species with the silicon wall during the pause time while the etching rate is maintained [7].

Figure 2. FESEM images for PS samples. (a) PDC, (b) PPC, (c) NDC and (d) NPC.

Figure 3 shows the EDX results for all samples showing the composition of elements in atomic percent. The introduction of pulse current etching technique has increased the percentage of Si elements in both P-type (PPC) and N-type (NPC) wafer. The high value of silicon element indicates that small area of silicon has been oxidized during the fabrication process.

The AFM images for each sample are shown in Figure 4 shows the roughness of the sample surface. Base on the AFM images, samples which undergo pulse current etching technique for both wafer type (Figure 4(b) and 4(d)) have more uniform and steeper sidewalls separating the Si columns as compared to the samples fabricated using DC etching technique which is also agreed by previous work done in 2016 [8]. However, P-type sample (Figure 4(b)) which was etched using pulse current technique has most uniform surface roughness as compared to other three samples.
Figure 3. EDX results for PS samples. (a) PDC, (b) PPC, (c) NDC and (d) NPC.

Figure 4. AFM images for PS samples. (a) PDC, (b) PPC, (c) NDC and (d) NPC.
The crystallite size can be calculated from the data obtained by XRD analysis. Figure 5 shows the XRD analysis for each sample and As grown has been included for comparison. From the figure indicates that the highest intensity was obtained from the P-type wafer which was etched using pulse current technique (PPC) and improved the intensity of As grown itself. It is clearly seen that the application of pulse current technique has increased the intensity of each type of wafer as compared to the samples etched by using DC etching technique. The two pronounce peaks reflects the cubical structure of silicon at (400) and (422).

![Figure 5. HR-XRD results for PS samples. (a) PDC, (b) PPC, (c) NDC and (d) NPC.](image)

Table 1 shows the calculated crystallite size for each samples using Debye-Scherrer equation. From the data in Table 1, both wafer type fabricated using DC etching technique showing a similar value of crystallite size. However, the crystallite size has decreased when the wafer being etched using pulse current technique. The P-type wafer which has been fabricated using pulse current technique (PPC) having the smallest size of crystallite size as compared to other samples.

| Samples   | 2θ (degree) | FWHM (degree) | Crystallite size (nm) |
|-----------|-------------|---------------|-----------------------|
| As Grown  | 69.13       | 0.11          | 77.28                 |
| PDC       | 69.13       | 0.09          | 88.34                 |
| PPC       | 69.12       | 0.12          | 66.25                 |
| NDC       | 69.13       | 0.09          | 88.34                 |
| NPC       | 69.12       | 0.11          | 72.27                 |
4. Summary
In conclusion, the surface morphology indicated that the PS from the PC etching technique exhibited a more uniform structure for both Si wafer doping. However, the P-type wafer having the most uniform and homogeneous structure as compared to others. The periodical ON and OFF of the anodic current apparently initiates the recovery of HF concentration inside the pores and it can finally optimize the etching conditions. Atomic force microscopic observations of the surface reveal that the pulsed etching with P-type Si wafer creates isolated Si columns with steeper sidewalls, which are in favor of achieving the quantum confinement effect.

Acknowledgement
The authors wish to thank Universiti Teknologi MARA, Cawangan Pulau Pinang, the members Nano Optoelectronics Lab, USM and Department of Applied Sciences, Universiti Teknologi MARA, Cawangan Pulau Pinang for their endless technical assistance. The financial support from the Ministry of Higher Education Malaysia (MOHE) through Fundamental Research Grant Scheme (600-RMI/FRGS 5/3 (0107/2016) is gratefully acknowledged.

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