A 0.6 V full wave rectifier with current mode nested and periodic feedback loops

Fanyang Li, Jiwei Wang
The Key Lab Microelectronics of F.J Province, Fuzhou University, Fuzhou, China
a) t12046@fzu.edu.cn

Abstract: A 0.6 V full wave rectifier with current mode nested and periodic feedback loops is presented, for the improved dynamic range with the low supply voltage. Compared with the conventional rectifiers, the rectifier with the loops is characterized by the micro feedback loop nested in the periodic macro one, so as to enlarge the dynamic range of the current mode signal with the ultra power supply voltage. With the technique, the dynamic range of the fully rectified signal should be optimized. Fabricated with a 0.18 µm CMOS process, with the typical 0.6 V supply voltage, the minimum amplitude of the fully rectified signal reaches 10 nA with the input signal bandwidth of 10 kHz and the power dissipation of 50 nW.

Keywords: current mode, rectifier, feedback loops

References

[1] S. J. G. Gift: “A high-performance full-wave rectifier circuit,” Int. J. Electron. 87 (2000) 925 (DOI: 10.1080/002072100404587).
[2] C. Chanapromma and K. Daoden: “A CMOS fully differential operational transconductance amplifier operating in sub-threshold region and its application,” Proc. IEEE 2nd Int. Conf. Signal Proc. Systems - ICSPS 2010 (2010) V2-73. (DOI: 10.1109/ICSPS.2010.5555220).
[3] S. Khucharoensin and V. Kasemsuwan: “High performance CMOS current-mode precision full-wave rectifier (PFWR),” Proc. Int. Symp. Circuits and Systems I (2003) 1-41 (DOI: 10.1109/ISCAS.2003.1205495).
[4] H. Mitwong, et al.: “A 0.5 V quasi-floating gate self-cascade DTMOS current-mode precision full-wave rectifier,” 2012 9th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON) (2012).
[5] J. Koton, et al.: “Current-mode dual phase precision full-wave rectifier using current-mode two cell Winner-Takes-All (WTA) circuit,” Radioengineering 20 (2011) 428.
[6] J. Koton, et al.: “Minimal configuration versatile precision full-wave rectifier using current conveyors,” Proc. Advances in Communications Computers, Systems, Circuits and Devices (2010) 111.
[7] D. Biolek, et al.: “High-performance current differencing transconductance amplifier and its application in precision current-mode rectification,” Int. J. Electron. Commun. 62 (2008) 92 (DOI: 10.1016/j.aeue.2007.03.003).
[8] N. Minhaj: “OTA-based non-inverting and inverting precision full wave rectifier circuits without diodes,” Int. J. Recent Trends Eng. 1 (2009) 72.
1 Introduction

In the medical system with the ultra low power and supply voltage, the accuracy optimized full-wave rectifier is demanded to value the energy of the weak signal input. However, the performance of the rectification would be easily degraded because of the supply voltage going down.

Conventionally, the approaches of the rectification are: i) The operational amplifier used to implement the rectification; ii) The current mode approach to widen the dynamic range of the rectified output signal. Although the first approach is able to rectify the signal, the increase of the input signal’s magnitude would cause the decrease of the rectifier’s DC open loop gain and the precision of the rectification would be degraded seriously [1, 2, 3, 4]. To improve the dynamic range of the signal, the current mode approach is presented [5, 6, 7, 8]. To implement the conventional current mode technique, the cascoded topology with diodes is necessary to rectify the signal. The topology would enlarge the dynamic range of the signal. However, with the power supply voltage decreased, the performance of the rectification is also becoming poor because of the diode’s voltage drop [9, 10].

To improve the dynamic range of the signal with the ultra low supply voltage, this paper presents a full wave rectifier with current mode nested and periodic feedback loops, which is characterized by the micro feedback loop nested in the periodic macro one. The topology is able to have the macro feedback loop operate and rest according to the signal’s orientation. With the topology, the dynamic range of the rectification could be improved with the ultra low supply voltage. The paper is organized as follows: The principle of current mode nested and periodic feedback loops is proposed in section II. And the corresponding circuits are described in section III. The measurement results are presented in section IV. Conclusions are drawn in section V.

2 The principle and analysis of the proposed technique

2.1 The drawback analysis of the conventional current mode approaches

The conventional current mode approach [5, 6] is shown in Fig. 1(a). Conventionally, it is designed with the current mode differencing OTA and the cascoded diodes.
In order to optimize the rectification performance, the OTA is designed to enhance the current mode signal’s accuracy. However, considering of the rectification, the cascoded diodes has to be designed to output the rectified signal. And the minimum operation voltage is not able to be improved because of the diodes’ voltage drop, as shown in Fig. 1(a).

2.2 The principle of the proposed technique

 Unlike the conventional cascoded topology with the diodes, the principle of the proposed one is the cascaded topology without diodes. The mathematical model of the technique principle is given in Fig. 1(b): the proposed rectifier has the macro feedback loop, which plays the role on the signal’s rectification. The micro feedback loop is nested in the cascaded macro feedback loop. The open loop gain of the macro feedback loop is in inverse proportion to the signal $I_{in}$. (the characteristics can be realized with a simple cascaded two stage OTA). According to the mathematical model, the input current signal should be expressed as follows:

$$I_{in} = I_{in-1} + I_{in-2} = \frac{A_1(s)}{1 + A_1(s)} I_{in} + \frac{A_1(s)}{1 + A_1(s)} \frac{A_2(s)}{1 + A_2(s)} I_{in}$$  \hspace{1cm} (1)

Where $I_{in-1}$ and $I_{in-2}$ are the divided currents of $I_{in}$; and $A_1(s)$ and $A_2(s)$ are the open loop gains of the micro and macro feedback loops, respectively.

With the model and the corresponding equations, it is known that the divided currents $I_{in-1}$ and $I_{in-2}$, which should be generated with $I_{in}$ varied. Specifically, with the input positive signal $I_{in}$ increasing to some extent, the gain of $A_2(s)$ should be ignored. Therefore, the current $I_{in-1}$ should be formulated as follows:

$$I_{in-1} = \frac{A_1(s)}{1 + A_1(s)} I_{in}$$  \hspace{1cm} (2)

The above equation demonstrates that the current $I_{in-1}$ is almost equal to the input current $I_{in}$; and the current $I_{in-2}$ should be without consideration.
Likewise, with the negative input signal increasing, the $A_2(s)$ is enhanced. So the divided current $I_{in,2}$ should be expressed as follows:

$$I_{in,2} = \frac{A_1(s)}{1 + A_1(s)} \frac{A_2(s)}{1 + A_2(s)} I_{in}$$

(3)

The equation shows that: finally, the current $I_{in,2}$ is almost equal to the negative input current $I_{in}$; and the current $I_{in,1}$ should be ignored. Therefore, if the current $I_{in,2}$ is inversely mirrored and conveyed to the output, the fully rectified signal should be achieved.

3 The implementation of the current mode high pass filtering circuit

3.1 The circuit implementation

The topology of the rectifier is shown in Fig. 2: R is the V-I resistor on chip; C is the off-chip decoupling capacitor, which is to decoupling external DC voltage and maintain the operating point of the micro amplifier. As shown in Fig. 2, the micro amplifier is the single stage differential amplifier, which is constituted by the transistors $M_{8-12}$ and biased by the rectifier’s bias current source.

Specially, unlike the conventional rectifiers, the rectifier consists of the micro and macro current mode feedback loops. In order to stabilize the micro and macro feedback loops, the capacitor $C_1$ and $C_2$ are designed. As shown in Fig. 2, the micro current mode feedback loop is constituted by the micro-amplifier, the MOS transistors $M_{1,3}$ and the capacitor $C_1$. With regards of the macro feedback loop, it includes the micro feedback loop and the cascaded amplifier, which is constituted by MOS transistors $M_{2,4,5}$ and the capacitor $C_2$.

Accordingly, with the input positive signal increasing, the gate-source voltage $V_{GS,M3}$ is going up to sink the input current, and the current of $I_{in,1}$ is enhanced; and meanwhile, the gate-source voltage $V_{GS,M5}$ decreases and the current of signal $I_{in,2}$ is degraded. On the other hand, with the input negative signal increasing, the gate-source voltage $V_{GS,M5}$ increases; and the current of signal $I_{in,2}$ is enhanced with the gate-source voltage $V_{GS,M1}$ going up to source the input current, and the current of $I_{in,1}$ is decreased. Finally, the rectified current $I_{rect}$ is generated by the current mirroring groups $M_{3,6}$ and $M_{5,7}$.

With the topology, the minimum supply voltage of the circuit can be expressed as follows:

![Fig. 2. The topology of the (a) proposed rectifier (b) micro amplifier](image)
According to the equation above, with the .18 μm CMOS process and the overdrive voltage designed to be 200 mV, the minimum supply voltage could be 500 mV.

3.2 The optimization of the rectification performance

Since there is the nested micro feedback loop in the macro one, the characteristics of stability has to be improved. Firstly, the decoupling capacitor C should be large, in order to generate a zero point and cancel the pole point, which is caused by the input impedance.

Hence, within the positive input period, the corresponding equivalent circuit is given: $A_1$ is the gain of the micro amplifier in the nested micro feedback loop; $G_m6$ is the trans conductance of the transistor $M_6$. Accordingly, the transfer function in current mode should be expressed as follows:

$$H_{\text{open-loop}}(s) = \frac{A_1}{1 + A_1} \left( 1 + \frac{s}{\omega_{\text{dominant-pole}2}} \right)$$

Where $\omega_{\text{dominant-pole}2} = \frac{1}{r_{\text{out}1}C_1}$;

$\omega_{\text{dominant-pole}2}$ is the dominant pole of the loop; $r_{\text{out}1}$ are the micro amplifier’s output resistance.

Likewise, with the negative input period, the corresponding equivalent circuit is given in Fig. 3(b): $A_2$ is the gain of the cascaded amplifier in the macro feedback loop; $G_m5$ is the trans conductance of the transistor $M_5$. Correspondingly, the location of the open loop’s poles is illustrated in Fig. 3(a).

According to the equivalent circuit model and the open loop gain characteristics, the transfer function of the macro loop in current mode should be generally expressed as follows:
\[ H_{\text{open-loop}}(s) = \frac{A_2}{1 + A_2} \left( 1 + \frac{s}{\omega_{\text{dominant-pole}}(s)} \right) \left( 1 + \frac{s}{\omega_{\text{nondominant-pole}}} \right) \]

Where \( \omega_{\text{dominant-pole}} \) and \( \omega_{\text{nondominant-pole}} \) are the dominant pole and non-dominant pole of the loop, respectively; \( C_1 \) and \( C_2 \) are the capacitors for the frequency compensation; \( G_m \) and \( r_{\text{out}} \) are the micro amplifier’s trans conductance and the cascaded amplifier’s output resistance.

With the analysis above, in this design, in order to make the bandwidth in the positive and negative phases to be equal, the values of the capacitor \( C_1 \) and \( C_2 \) are designed to be equal. The corresponding magnitude characteristics are shown in Fig. 3: their respective margin phases are \( 45^\circ \) and \( 90^\circ \), respectively.

Also, according to the analysis above, the minimum input signal, which can be fully rectified and detected, should be approximately expressed as follows:

\[ I_{\text{rect, min}} = \frac{A_2(s) + 1}{A_2(s)} I_{\text{bias}} \] (5)

Where \( I_{\text{bias}} \) is the bias current of the circuit; and \( A_2(s) \) is the gain of the cascaded amplifier at the orientation transition of the input signal. According to the equation above, for the optimization of the rectification accuracy, \( I_{\text{bias}} \) is designed to be 8 nA. With the bias current, to design the bandwidths of the two phases above to be 10 kHz, the values of the capacitors are designed to be 100 fF.

4 The results of measurement and discussion

The full wave rectifier is designed and fabricated with a 0.18 µm CMOS standard process. The prototype of the chip is shown in Fig. 4. It is measured with the 0.6 V supply voltage and 8 nA bias current.

![Fig. 4. The prototype of the proposed reference on chip](image)

4.1 The measurement of the transfer characteristics

To evaluate the performance of the transfer characteristics, the output rectified signal is plotted with the increasing input amplitude. As shown in the Fig. 5, with the 10 kHz sine input signal, the minimum fully rectified signal is 10 nA.
4.2 The comparison

The comparison with the previous works and products is concluded in the Table I. In the Table I, compared with the conventional approaches, the proposed one is able to operate with the ultra low supply voltage 0.6 V, and the minimum fully rectified signal can be optimized to be 10 nA.

Table I. Performance comparison

| Ref# | Process Technology | Supply Voltage (V) | Minimum Fully Rectified Signal (nA) | Power (nW) | Signal Bandwidth (MHz) |
|------|--------------------|--------------------|-----------------------------------|------------|-----------------------|
| [2]  | 0.5 µm             | 3                  | 300 nA                            | 5.8 * 10⁶  | 100 MHz               |
| [3]  | 0.35 µm +/−1.8     | /                  | /                                 | 6.31 * 10⁶ | 5 MHz                 |
| [5]  | 0.35 µm +/−1.5     | /                  | /                                 | /          | 70 MHz                |
| [7]  | 0.25 µm            | 1                  | /                                 | /          | 10 MHz                |
| This work | 0.18 µm            | 0.6                | 10 nA                             | 50         | 10 KHz                |

5 The conclusion

This paper has presented a 0.6 V full wave rectifier with current mode nested and periodic feedback loops. According to the measurement results, with the ultra low supply voltage, the proposed rectifier realizes the improved fully rectified signal.

Acknowledgement

This work is funded by the national natural science funds. (No: 61501122)