Development of TRL5 Space Qualified Hardware for Tuning, Biasing, and Readout of Kilopixel TES Bolometer Arrays

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ABSTRACT

The next generation of space-based mm-wave telescopes, such as JAXA’s LiteBIRD mission, require focal planes with thousands of detectors in order to achieve their science goals. Digital frequency-domain multiplexing (dfmux) techniques allow detector counts to scale without a linear growth in wire harnessing, sub-Kelvin refrigerator loads, and other scaling problems. In this paper, we introduce Technology Readiness Level 5 (TRL5) electronics suitable for biasing and readout of LiteBIRD’s Transition Edge Sensor (TES) bolometers using dfmux techniques. These electronics sit between the spacecraft’s payload computer and the cryogenic focal plane, and provide detector biasing, tuning, and readout interfaces between these detectors and the spacecraft’s on-board storage. We describe the overall architecture of the electronics, including functional decomposition into modules, the numerology and interconnection of these modules, and their internal and external interfaces. We describe performance measurements to date, including power consumption, thermal performance, and mass, volume, and reliability estimates. This paper is a companion piece to a description of the electronics’ on-board Field-Programmable Gate Array (FPGA) firmware.

Keywords: Bolometer, FPGA, CMB, satellite, SQUID

1. INTRODUCTION

Transition Edge Sensors (TESes) are widely used for ground-based observations of the Cosmic Microwave Background. Their success in experimental cosmology reflects both the exquisite sensitivity of these devices at microwave frequencies, as well as the technological maturity of TES readout systems as a whole. Over the past decade, the scale of TES arrays deployed for cosmology has increased by over an order of magnitude, with SPT-3G currently fielding an array of 15,000 TESes within a single focal plane.

The rapid pace of development for ground-based TES readout systems heralds adoption of the technology in space. Several proposed space observatories have baselined large arrays of TES detectors for microwave, infrared, or X-ray missions. The first of these missions is JAXA’s LiteBIRD Space Observatory, scheduled to launch by 2029.

Although ground-based technologies have progressed into sophisticated and reliable systems, there is much work still to be done in qualifying such systems for launch and use in space environments. One important aspect of this effort is the development of space-qualified control electronics, capable of performing the multiplexing operations required to operate large TES arrays.

Multiplexing systems have been an enabling technology for ground-based observatories. The most common systems fall into two categories: time-division multiplexing (TDM), and frequency domain multiplexing (FDM). The system described here implements digital frequency-domain multiplexing (dfmux). Each TES in an array is operated with distinct AC bias voltages between 1-10 MHz. Incident power is recorded through amplitude modulation of these carrier sinusoids, in an operation analogous to AM radio. A description of the associated firmware and signal processing pipeline is given in a companion paper (Ref. 1).

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In this document, we describe the overall design of a TRL-5 readout system implementing power-efficient, highly-multiplexed FDM. This system is designed to be composable to scale across a variety of space-based TES applications. It has been selected as a baseline for the LiteBIRD Space Observatory.

2. CONCEPT OF OPERATIONS

The readout system is the interface between the cryogenic circuitry and the digital electronics that transfer and store data for offline analysis. The readout system has two functions:

- to “tune” the cryogenic hardware (detectors and cryogenic amplifiers) into the appropriate state to take data; and
- to digitize and process focal-plane signals into a form suitable for transfer, storage, and offline analysis.

A third essential requirement, which becomes acute in space, is uninterrupted operation in spite of environmental conditions including radiation. Because TES detectors operate in their superconducting transition, they are prevented from entering the superconducting state through precisely calibrated application of electrical power from the readout. Interruptions to that bias power can dramatically alter the state of the cryogenic hardware. Recovery from interruptions require a series of tuning operations before the system is fit to resume taking data. Rapid and efficient fault detection and recovery is an active area of investigation at all levels of mission design, including detector fabrication, readout electronics design, and system integration.

2.1 Architectural Overview

The overall architecture of the readout system matches the ground-based “ICE” system and previous development work on a space-qualifiable system. A single modular unit is known as a Signal Processing Unit (SPU). A cutaway view of a single SPU is provided in Figure 1a. A partially integrated SPU is shown in Figure 1b. Each SPU contains its own Power Conditioning Assembly (PCA), Signal Processing Assembly (SPA), and up to 4 Digitizer Assemblies (DAs), which are all mechanically and thermally contained within a Signal Processing Unit Enclosure (SPUE). Each SPU can operate 16 SQUID channels at a multiplexing factor of up to 128 detectors per SQUID. Signal processing firmware operating on an FPGA within each SPU is described in a companion paper.1
Figure 2: The architecture and numerology of LiteBIRD’s readout electronics. There are 6 active and 6 cold-spare SPUs communicating with 82 SQUIDs split across 3 telescopes (LFT, MFT, and HFT). Cross-strapping between primary and redundant units occurs between SCUs and SPUs, and between SPUs and payload computers (DPUs). In LiteBIRD, redundancy is provided by cold-spare SPUs and DPUs.

Between the SPU and focal plane are SQUID Controller Assemblies (SCAs) enclosed within SQUID Controller Units (SCUs). SCAs interface directly to the cryogenic stage, performing amplification of analog signals and conditioning of the bias voltages and nulling currents. Both SCAs and DAs accommodate up to 4 multiplexed SQUID channels. For the LiteBIRD mission, a flight-qualified SCA based on an earlier TRL-5 design is being built by the National Institute for Nuclear Physics (INFN) in Italy. Although all tests reported in this document use a ground-based SCA (MGNGSQ4), the two SQUID controller designs are functionally equivalent.

2.2 System Scalability

Each SPU is an independent, modular unit. It can be configured as either a primary or redundant system, and may be populated with up to 4 DAs. This flexibility allows the system to scale in size without lowering the overall TRL.

Figure 2 shows the readout system as configured for the LiteBIRD mission. Three separate telescopes (Low-Frequency Telescope, Mid-Frequency Telescope, and High-Frequency Telescope) house a combined 82 SQUIDs and approximately 4,500 TES bolometers. To control them, a total of 12 SPUs are required: 6 primary, and 6 cold spares. Each SCA has two DA interfaces: one primary, and one cold spare. In this configuration, the SCAs are the only element of the warm readout electronics with no cold-spare – they are also the lowest-power element, have limited digital circuitry, and a low integrated risk of failure (see Section 4.4 for a discussion on reliability).

Various SQUID-focal-plane mappings can be accommodated by this design. Although the warm readout electronics can multiplex as high as 128 detectors per SQUID, the LiteBIRD configuration doesn’t use a multiplexing factor higher than 68. As the LiteBIRD focal-plane has matured, the optimal readout electronics numerology has evolved. We have accommodated these changes by optimizing the multiplexing factor assigned for each telescope and the number of DAs populated in each SPU. These changes have no TRL impact, and require no additional R&D or qualification.
2.3 Detector Tuning and Operation

The high-level algorithms that tune a detector array involve complex interactions between cryogenic elements (bolometers, SQUIDs) and electronics that control them (SPUs, SCUs, and active elements in the cooling chain). These algorithms are implemented in a Data Processing Unit (DPU), which performs top-level telescope control operations and handles data streamed from SPUs to on-board storage. The DPU is outside the scope of hardware described here.

Primary and redundant DPUs communicate with SPUs through point-to-point, bidirectional serial links. Each link is full-duplex and has an usable bandwidth of 40 Mbit/s accounting for encoding overhead. (See Ref. 1.)

After power-up, SPUs must be configured by a DPU to initialize DAs and SCAs, and to assign bias parameters (e.g. frequencies, phases, amplitudes) required by the dfmux signal paths. All DPU-to-SPU commands consist of reads and writes into memory-mapped registers in the SPA’s FPGA.

Once an SPU is active, it continuously streams data for all 128 multiplexed channels on all 16 SQUIDs. This data accounts for about 20 Mbits/s of the available bandwidth from the SPU to the DPU. The remaining bandwidth is available for commanding and data returns associated with tuning operations, and is wide enough not to be a limiting factor in tuning speed.

3. SPU ASSEMBLIES

Below we briefly describe the designs of the major elements of the SPU: the SPA, DA, and SPUE.

3.1 Signal Processing Assembly (SPA)

The SPA executes the real-time synthesis and demodulation algorithms that are central to a dfmux readout system. It consists of an FPGA (XQRKU060) and associated power supply, interface, and support circuitry allowing it to operate. The FPGA is mounted on the PCB’s underside and bonded directly to the enclosure to facilitate a short thermal path to radiators on the spacecraft. A block diagram of the SPA is shown in Figure 3.

All oscillators in the system are synchronized to a single, externally-supplied clock to ensure EMI throughout the system is controlled. The sole exception is an oscillator within the FPGA, which is unavoidable but not used or exposed outside the FPGA. Point-of-load regulators in the SPA operate at 500 kHz, and are phase-locked to the 10 MHz input clock. When the SPA is powered up, all converters free-run around their nominal frequencies until the FPGA firmware is fully loaded, at which time it provides the synchronization signal for each converter.

To minimize power consumption and design complexity, no external RAM is present on the SPA. The only storage elements are the non-volatile flash containing the FPGA’s bitstream, and volatile memory inside the FPGA itself.

3.2 Digitizer Assembly (DA)

The Digitizer Assembly (DA) houses ADCs, DACs, filters, and amplifiers that interface between the analog signals on the focal plane and the digital algorithms executed in the SPA. Each SPA connects to up to 4 DAs via flexible harnesses. Each DA attaches via a 37-pin D-subminiature wire harness to an SCA. A block diagram of the DA is shown in Figure 5. A prototype DA is shown in Figure 4b.

Neither the fast ADC nor DAC come from vendors’ radiation-qualified product lines. (Radiation-hard parts exist but are not competitive in terms of noise performance, power consumption, or channel density.) Both the ADC and DAC have been radiation tested. Test results are favourable, though a detailed analysis is ongoing.

3.3 Signal Processing Unit Enclosure (SPUE)

The SPU Enclosure is shown in Figure 1b. The enclosure:

- protects the delicate column grid array (CGA) of the FPGA,
- maintains rigidity for launch stresses,
- conducts heat away from the FPGA and other highly dissipative components, and
- fully encloses the system to prevent electromagnetic interference.

The SPUE is constructed from gold-plated aluminum.
Figure 3: Signal Processing Assembly (SPA) block diagram.

(a) A Signal Processing Assembly (SPA). The FPGA is mounted on the underside of the board, facilitating a good connection to the thermal interface on the chassis (see Figure 1b). The 8 large, white connectors attach to 4 DAs via flexible adapters. Other ports (2 DPU connectors, 1 Ground-Support Equipment (GSE) connector, and 1 PCA connector) attach to bulkhead interfaces on the chassis via short “pigtail” cables. A block diagram of the SPA is shown in Figure 3.

(b) A Digitizer Assembly (DA). Each DA contains carrier, nuller, and demodulator ADCs/DACs for 4 SQUID channels, plus associated amplifiers, filters, and housekeeping. A flexible harness (top) connects to the SPA. A connector (bottom) interfaces to the connector at the bottom via an external wire harness. A block diagram of the DA is shown in Figure 5.

Figure 4: Major assemblies within the Signal Processing Unit (SPU). These assemblies’ orientations within an assembled SPU can be seen in Figure 1a.
3.4 Power Converter Assembly (PCA)

The Power Converter Assembly (PCA) provides an isolated power-conversion stage between unregulated bus supplies and the internal supplies used by the SPA and DA. The PCA also supplies power to SCAs attached to each SPU. The PCA is synchronized to a clock supplied by the SPA.

PCAs are off-the-shelf units, with varying power-conversion efficiencies (typically, 70%-90% depending on power-conversion ratio). For LiteBIRD, the spacecraft supply voltage is between 38-52 V and we assume a nominal PCA efficiency of 72%.

4. PERFORMANCE

Detailed analysis and testing, including thermal-vacuum (TVAC), launch-load, and shake-table testing was completed during a recent technology development (STDP) contract from the Canadian Space Agency (CSA). The SPU meets LiteBIRD’s current requirements. A summary of analyses and/or tests to date is provided in Table 1.

Below, we provide details associated with power consumption, thermal dissipation, mass, and reliability. Performance and validation activities were performed using a COTS power supply for the PCA and the ground-based SCA that is part of the ICE readout system. Noise and tuning benchmarks with the INFN SCA and flight-representative cryogenic hardware will follow. For firmware performance, see Ref.1.

4.1 Power consumption

A fully populated SPU dissipates 31 W under nominal conditions at room temperature (25°C) and excluding PCA losses. This SPU must be coupled with 4 SCAs (1.8W each for the INFN design; 2.5W each for the ground-based design, excluding PCA losses) to read out 16 SQUID channels. With 2.5W per SCA and a PCA efficiency of 72% PCA efficiency, a complete readout system for 16 SQUIDs at a multiplexing factor of up to
### Table 1: Key Parameters for a single SPU, excluding the PCA (which is expected to be a COTS unit). Results not marked “simulation” represent tests/measurements. Power consumption is extrapolated from 1 DA and 1 SCA to 4 of each, and includes losses assuming 72% PCA efficiency. The baseline LiteBIRD readout uses 6 active SPUs.

| Parameter                                      | Value                      |
|-----------------------------------------------|----------------------------|
| Mass                                          | 9.5 kg                     |
| Volume                                        | 34cm x 33cm x 27cm         |
| Lowest Eigenfrequency (simulation)            | 466 Hz                     |
| Quasistatic Launch Load (simulation)          | 55G                        |
| Random vibration (in-plane)                   | 9.9 Grms                   |
| Random vibration (out-of-plane)               | 15.2 Grms                  |
| Power Consumption                             | 43 W                       |
| Multiplexing Factor                           | up to 128×                 |
| Total Supported TES channels                  | 2,048                      |
| Survival Temperature                          | -50°C - 100°C              |
| Operational Temperature                       | -50°C - 76°C               |

### Table 2: Power consumption for architectural elements and scenarios. These are room-temperature measurements, not specifications, and do not include design margin. Unlike Ref. 3, these figures are inclusive of power-converter losses. Although the INFN SCA is more power-efficient than the ground-based SCA, we use the more pessimistic figures here to match testing completed to date.

| Parameter                                      | Value                      |
|-----------------------------------------------|----------------------------|
| 1 SPA, 128× multiplexing                      | 15.4 W                     |
| 1 DA                                          | 3.9 W                      |
| 1 ground-based SCA                            | 2.5 W                      |
| PCA Efficiency                                | 72%                        |
| LFT SPU, (3 DAs, 3 SCAs)                      | 48 W                       |
| MFT/HFT SPU, (4 DAs, 4 SCAs)                  | 57 W                       |
| **LiteBIRD configuration, total (6 SPUs)**     | **324 W**                  |
| **LiteBIRD configuration (4500 TESes)**        | **72 mW/TES**              |

128× dissipates 57 W (84 mW/bolometer at 6×: 45mW/bolometer at 128× multiplexing). The SPA’s power consumption was measured at a full 128× multiplexing factor and decreases at lower multiplexing factors.

The LiteBIRD configuration operates 6 SPU/SCU pairs (the other 6 SPUs are cold spare). The 2 LFT SPU/SCU pairs have only 3 DAs and 3 SCAs each. The 2 MFT and 2 HFT SPU/SCU pairs are fully populated. The total configuration for LiteBIRD dissipates 324 W. With LiteBIRD’s baseline flight configuration (4,500 TESes), power dissipation is 72 mW/TES. (This hardware configuration is capable of reading out 11,264 TESes at 128× multiplexing, corresponding to a per-TES power consumption of 29 mW/TES.) A detailed breakdown of power consumption is given in Table 2.

### 4.2 Thermal dissipation

About 80% (43 W) of the power supplied to the SPU is dissipated as heat within the SPU itself. (The remainder is dissipated in the SCAs powered by the SPU.)

The SPU manages thermal dissipation from the readout with only conductive cooling. The FPGA is the single largest source of thermal dissipation, and is mounted on the underside of the SPA. The FPGA is bonded directly to the SPUE chassis, providing both mechanical and thermal support. The total thermal path between FPGA die and spacecraft radiators is only a few centimeters and has a temperature gradient of approximately 10°C. For the flight FPGA and flight bonding materials, the simulated thermal gradient is 7°C. Measurements in a TVAC chamber using demonstration hardware showed a 14°C gradient, consistent with the material and configuration differences. The maximum operating temperature (before derating) of the flight FPGA is 125°C,
which provides substantial margin for radiator capacity. (Current requirements on the LiteBIRD radiator deck specify an operational maximum of 40°C.)

The DA cassettes are also designed to conduct heat towards the radiator deck, but the dissipative sources are more distributed. Most of the SPUE structure is in service of rigidity rather than thermal management.

4.3 Mass
An assembled SPU has a mass of 9.5 kg, excluding the PCA. Both the structural and thermal performance of the SPUE exceed target requirements. A preliminary analysis suggests it is possible to reduce the mass by 20% without degrading structural or thermal performance.

4.4 Reliability
In a CMB mission such as LiteBIRD, science products require long-term data collection over wide angular scales. A given map of the CMB is formed numerically by combining many sweeps of each telescope’s beam, which is constantly in motion, across the region of interest. This approach is in sharp contrast to telescopes operating at small angular scales and producing short-term images of specific targets. It is consistent with ground-based CMB experiments, including SPTPol\(^5\) and SPT.\(^6\) Mission success is driven by good overall availability of the instrument, and does not require perfect operation of every bolometer at all times.

The overall reliability of the readout system is determined by four factors:

- The individual reliabilities of the subsystems comprising it,
- The manner in which they are interconnected (e.g. cross-strapping),
- The method in which the instrument is operated, and
- The quality required for data products to be considered “good”.

Here, we focus only on the first factor, which is determined by the hardware itself and not mission-level architecture. (In the case of LiteBIRD, SPUs are redundant, SCAs are not, and the ability to operate with failed SQUIDs or bolometers – due to yield, aging, failure to tune, or any other reason – is expected.) A payload-level Fault Detection, Isolation, and Recovery analysis will provide payload-level reliability analysis and will be completed in an upcoming mission phase.

With 2 exceptions (see Section 3.2), components for all assemblies in the system are chosen from vendors’ radiation-tolerant or radiation-hardened product lines. The minimum total dose (TID) rating for all rad-tolerant/rad-hard components in the system is 20 krad. Critical components within the system have higher total-dose ratings: for example, the FPGA, switching, and linear power regulators are rated to a TID of 100 krad or higher.

Estimated failure rates for various architectural elements of the readout system are given in Table 3. These failures were calculated by considering specific (where possible) or typical FIT rates for individual components. Rates are exclusive of firmware errors, including radiation effects, which can interrupt operation but cannot cause permanent damage. For the DA and SCA, we have separated FIT rates into failures affecting common circuitry used by the entire assembly (i.e. shared power supplies and control interfaces) and failures that can be isolated to only one channel (affecting only bolometers associated with a single SQUID). These failures are treated separately because of their relative impacts.

5. NEXT STEPS
In this work, we described the major design elements and demonstration for a TRL-5 space-qualified readout system for TES detectors. The next phase of development includes integrated full-scale functional testing, and a detailed characterization of noise performance with space-representative hardware.

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Table 3: Expected Failure-in-Time (FIT) Rates for individual architectural elements. FIT rates indicate expected failures per $10^9$ hours of operation. These values are calculated by considering specific (where possible) or typical FIT rates for individual components. FIT rates for mechanical/structural elements and cable assemblies are not included. The PCA FIT rate is known to be high relative to commercially available, space-qualified units and will be revised. The combined SPU FIT rate does not consider continued operation with failed units.

| Subsystem | Failure Type | FIT Rate | MTTF (Years) |
|-----------|--------------|----------|--------------|
| SCA       | single channel | 123      | 930          |
|           | common        | 119      | 960          |
| DA        | single channel | 167      | 680          |
|           | common        | 166      | 690          |
| SPA       | common        | 510      | 220          |
| PCA       | common        | 2,304    | 50           |
| Complete SPU (SPA, PCA, 4 DAs) | any | 6,150  | 18          |

REFERENCES

[1] Smecher, G., Cliche, J.-F., Dobbs, M., and Montgomery, J., “Development of TRL5 firmware for tuning, biasing, and readout of kilopixel TES bolometer arrays,” in [SPIE Proceedings], SPIE (July 2022).

[2] Bandura, K., Bender, A. N., Cliche, J. F., de Haan, T., Dobbs, M. A., Gilbert, A. J., Griffin, S., Hsyu, G., Ittah, D., Parra, J. M., Montgomery, J., Pinsonneault-Marotte, T., Siegel, S., Smecher, G., Tang, Q. Y., Vanderlinde, K., and Whitehorn, N., “ICE: a scalable, low-cost FPGA-based telescope signal processing and networking system,” J. Astronomical Instrumentation 5(4) (2016).

[3] Bender, A., Cliche, J.-F., Haan, T., Dobbs, M., Gilbert, A., Montgomery, J., Rowlands, N., Smecher, G., Smith, K., and Wilson, A., “Digital frequency domain multiplexing readout electronics for the next generation of millimeter telescopes,” Proceedings of SPIE - The International Society for Optical Engineering 9153 (07 2014).

[4] Xilinx Inc., [UltraScale Architecture Configuration User Guide], no. UG570 (2020).

[5] Austermann, J. E., Aird, K. A., Beall, J. A., Becker, D., Bender, A., Benson, B. A., Bleem, L. E., Britton, J., Carlstrom, J. E., Chang, C. L., Chiang, H. C., Cho, H.-M., Crawford, T. M., Crites, A. T., Datesman, A., de Haan, T., Dobbs, M. A., George, E. M., Halverson, N. W., Harrington, N., Henning, J. W., Hilton, G. C., Holder, G. P., Holzapfel, W. L., Hoover, S., Huang, N., Hubmayr, J., Irwin, K. D., Keisler, R., Kennedy, J., Knox, L., Lee, A. T., Leitch, E., Li, D., Lueker, M., Marrone, D. P., McMahon, J. J., Mehj, J., Meyer, S. S., Montroy, T. E., Natoli, T., Nibarger, J. P., Niemack, M. D., Novosad, V., Padin, S., Pryke, C., Reichardt, C. L., Ruhl, J. E., Saliwanchik, B. R., Sayre, J. T., Schaefer, K. K., Shirokoff, E., Stark, A. A., Story, K., Vanderlinde, K., Vieira, J. D., Wang, G., Williamson, R., Yefremenko, V., Yoon, K. W., and Zahn, O., “SPTPol: an instrument for CMB polarization measurements with the south pole telescope,” in [SPIE Proceedings], Holland, W. S., ed., SPIE (Sep 2012).

[6] Sobrin, J. A., Anderson, A. J., Bender, A. N., Benson, B. A., Butcher, D., Foster, A., Goeckner-Wald, N., Montgomery, J., Nadolski, A., Rahlin, A., Ade, P. A. R., Ahmed, Z., Anderes, E., Archipley, M., Austermann, J. E., Avva, J. S., Aylor, K., Balkenhol, L., Barry, P. S., Thakur, R. B., Benabed, K., Bianchini, F., Bleem, L. E., Bouchet, F. R., Bryant, L., Byrum, K., Carlstrom, J. E., Carter, F. W., Cecil, T. W., Chang, C. L., Chaudhuri, P., Chen, G., Cho, H.-M., Chou, T.-L., Cliche, J.-F., Crawford, T. M., Cukiernian, A., Daley, C., de Haan, T., Denison, E. V., Dibert, K., Ding, J., Dobbs, M. A., Everett, W., Feng, C., Ferguson, K. R., Fu, J., Galli, S., Gambrel, A. E., Gardner, R. W., Gualtieri, R., Guns, S., Gupta, N., Guyser, R., Halverson, N. W., Harke-Hosemann, A. H., Harrington, N. L., Henning, J. W., Hilton, G. C., Hivon, E., Holder, G. P., Holzapfel, W. L., Hood, J. C., Howe, D., Huang, N., Irwin, K. D., Jeong, O. B., Jonas, M., Jones, A., Khaire, T. S., Knox, L., Kofman, M., Kukla, D. L., Kuhlen, D., Kuo, C.-L., Lee, A. T., Leitch, E. M., Lowitz, A. E., Lu, C., Meyer, S. S., Michalik, D., Millea, M., Natoli, T., Nguyen, H., Noble, G. I., Novosad, V., Omori, Y., Padin, S., Pan, Z., Paschos, P., Pearson, J., Posada, C. M., Prabhu, K., Quan, W., Reichardt, C. L., Riebel, D., Riedel, B., Rouble, M., Ruhl, J. E., Saliwanchik, B., Sayre, J. T., Schiappucci, E., Shirokoff, E., Smecher, G., Stark, A. A., Stephen, J., Story, K. T., Suzuki, A., Tandoi, C., Thompson,
K. L., Thorne, B., Tucker, C., Umilta, C., Vale, L. R., Vanderlinde, K., Vieira, J. D., Wang, G., Whitehorn, N., Wu, W. L. K., Yefremenko, V., Yoon, K. W., and Young, M. R., “The design and integrated performance of SPT-3g.” *The Astrophysical Journal Supplement Series* **258**, 42 (Feb 2022).