Development of microwave monolithic integrated circuit of power amplifier 26 – 30 GHz band for information and communication systems of new generation (5G)

E V Erofeev¹, D A Shishkin, I V Fedin

Research Institute of Electrical Communication Systems, Tomsk State University of Control Systems and Radioelectronics, 40 Lenina Avenue, Tomsk634050, Russian Federation

¹E-mail: erofeev@sibmail.com

Abstract. Development of information and communication systems of new generation (5G) takes much time, needs financial support, and causes many debates around the most suitable frequency bands for its application. Meanwhile, single band are likely to be designated on a worldwide basis for millimeter-wave 5G in the immediate future. This paper describes the design, layout, and performance of power amplifier monolithic microwave integrated circuit (MMIC) 26 – 30 GHz band. The design was implemented on 0.25µm gate length GaAs pHEMT process and has an output power capability of 1 W at 1dB gain compression (P-1dB) and PAE of 20% with a small signal gain of 20dB.

1. Introduction

The first generation (1G) of mobile network was developed in Japan by Nippon Telephone and Telegraph Company (NTT) in the beginning of 1980s. There was the analog system and had many disadvantages due to technology limitations. Second generation (2G) of mobile communication system introduced a new digital technology for wireless transmission also known as Global System for Mobile communication (GSM). GSM technology became the base standard for further development in wireless standards later. This standard was capable of 64 kbps maximum data rate which is sufficient for SMS and email services. Third generation (3G) mobile communication started with the introduction of Universal Mobile Terrestrial / Telecommunication Systems (UMTS). UMTS had the higher data rate of 384 kbps and it supported video calling for the first time on mobile devices. After the introduction of 3G mobile smart phones became popular across the globe. Specific multimedia applications were developed for smartphones which handles chat, email, video calling, games, social media and healthcare. 4G systems are enhanced version of 3G networks developed by IEEE and offer higher data rate and capable to handle more advanced multimedia services [1-2].

Fifth-generation (5G) wireless is the latest iteration of mobile technology engineered to greatly increase the speed and responsiveness of wireless networks. The advantages of 5G systems are the highest data rate of 10 Gbps, extremely low latency of 1 ms and uniform coverage over a wide area. Although there is still much debate about the precise form that 5G will take, there is a degree of consensus that the standard will require existing cellular frequency of mm-wave band where there is greater spectral availability.
The perspective bands for 5G communications include the 28 GHz (27.5 - 28.35 GHz), 37 GHz (37 - 38.6 GHz) and 39 GHz (38.6 – 40 GHz) bands, all of which are already licensed by the FCC in the USA. In Europe the Radio Spectrum Policy Group (RSPG) has recommended the 28 GHz band (27.5 to 28.35 GHz) as the pioneer band for 5G and development work is now underway targeting this band [3-6].

The modern 5G systems are based on phased-array or switched beam antenna architectures. The key radiofrequency (RF) components required for these systems are power amplifiers (PA), low-noise amplifiers (LNA), phase shifters and switches of mm-wave band [7-11]. Power amplifiers based on GaAs pHEMT technology is an attractive candidate for 5G front end. It offers the adequate output power, high linearity and power added efficiency (PAE) at a low power supply voltage [12-14]. GaN HEMT technology is another attractive candidate for mm-wave high power amplifiers. It offers the higher power density and PAE but has the disadvantage of requiring a higher power supply voltage [15-16].

In this paper we report about development of microwave monolithic integrated circuit (MMIC) of power amplifier 26 – 30 GHz band based on 0.25 µm GaAs pHEMT process for information and communication systems of new generation (5G).

2. Experimental

2.1. Epitaxial structure

The GaAs pHEMT was formed on the GaAs/AlGaAs/InGaAs pseudo-morphic structures grown by using molecular beam epitaxy. The GaAs epi-structure was optimized for a maximum drain voltage of 6V. The semi-insulating GaAs buffer, AlAs/GaAs super-lattice buffer, AlGaAs spacer layer, InGaAs channel layer, AlGaAs spacer layer, AlGaAs donor layer and n+ GaAs cap ohmic contact layer were grown on 4-inch diameter semi-insulating GaAs substrates. An AlAs etch stop layer is inserted in the AlGaAs donor layer to consistently maintain the height of Schottky junction to achieve desired pinch-off voltage and trans-conductance. In addition, two Si planar doping layers were inserted on both sides AlGaAs/InGaAs/AlGaAs to increase the current density of the channel. Hall measurements produced a sheet carrier concentration of $1.8 \times 10^{12} \text{cm}^{-2}$ and mobility of 7950 cm$^2$/V·s at room temperature.

2.2. Fabrication process

After mesa isolation the source and drain ohmic metals were formed. There were used AuGeNi based ohmic contacts deposited by the electron beam evaporation under a vacuum of $1 \times 10^{-4} \text{torr}$. Then the wide recess and 0.25 um T-gates were fabricated by electron beam lithography and lift-off process. There was used a tri-layer resist stack of 950 PMMA/LOR 5B/495 PMMA (from bottom to top). The resists were spin coated onto the substrate. Each resist layer was baked for 5 min at $180 \degree \text{C}$ on the hotplate. The Raith-150$^{\text{TM}}$ e-beam nanolithography system was used for a single exposure of the resist with 30 kV electron beam energy. The optimum conditions, to define T-shape gates at 250 nm level for pHEMTs were obtained when the footprint dose is 600 μC/cm$^2$, the head dose was 140 μC/cm$^2$. The top layer was developed in a 1:1 mixture of MIBK:IPA for 60 sec and then rinsed in IPA and blown dry in nitrogen. The second layer was developed in MF-319 developer and then rinsed in water. The third layer was developed for 30 s in MIBK:IPA (1:3) followed by rinsing in an IPA and blown dry with nitrogen. Then narrow recess etching was performed using citric acid based solution as an etchant to remove GaAs cap layer. After that T-gate metallization of Ti/Pt/Au was deposited by e-beam evaporation under a vacuum of $5 \times 10^{-7} \text{torr}$ and lifted off in acetone. A 150 nm layer of Si$_3$N$_4$ was deposited on the wafer in order to passivate the surface of the transistors. Other MMIC components were fabricated on the front side processing and included NiCr based resistors, metal interconnects, gold plated air bridges, Si$_3$N$_4$ based capacitors and dielectric protective overcoat. After the front side processing, the substrates are thinned down to 100 μm followed by via hole formation by dry etching and gold backside metallization by electrochemical deposition.
3. Results and discussion

3.1. GaAspHEMT characteristics
Figure 1 shows DC measurements of 600 µm cell (6x100 µm) GaAspHEMT at Vds = 6V. The maximum trans-conductance is 420 mS/mm with drain-source current of 475 mA/mm. The gate-drain breakdown voltage is 14 V. It provides the sufficient margin for the 6V device operation.

![Figure 1. DC measurements (Transconductance and drain-source current) of 6x100 µm GaAspHEMT (Vds = 6V).](image1)

Figure 2 shows load-pull measurements of 600 µm cell (6x100 µm) GaAspHEMT at Vds=6V and Ids=90 mA/mm. The maximum output power density is 625 mW/mm with PAE of 52% at F = 11 GHz.

![Figure 2. Load-pull measurements (Pout, gain and PAE) of 6x100 um GaAspHEMT (Vds = 6V, Ids = 90 mA/mm, F = 11 GHz).](image2)

3.2. MMIC design approach
The design of microwave monolithic integrated circuit of power amplifier (PA) commenced by selection of the transistor sizes for each stage of the PA. Selection of the transistor size for a mm-wave
PA is a trade-off between output power capability and available gain. A physically larger transistor (more gate fingers and/or wider unit finger width) will have a higher available RF output power. However, the higher parasitics of the physically larger transistor result in a reduction in available gain. The best way to address this issue is to select a transistor with the largest gate periphery that can provide a practical level of available gain and to combine multiple transistors in a low-loss on-chip combining and matching structure. For the power amplifier described here, an output stage of 8 power-combined 4-finger 100 µm transistors was selected to achieve the target output power of 1W. Similar trade-offs were then undertaken to select the size and number of transistors in the preceding stages. The overall impact on compression and linearity of the complete cascaded arrangement must also be considered in making this selection. This process resulted in selecting a pair of power combined transistors to drive the output stage and a single transistor to drive this. The topology adopted is evident from the layout plot of the power amplifier MMIC shown in Figure 3. The MMIC was very compact design with a die size of 8.75 mm² (3.5 mm x 2.5 mm) and the total output FET periphery is 3.2 mm.

Figure 3. Layout plot of the power amplifier MMIC.

Power amplifier MMIC (figure 4) is consists of three amplification stages with the following gate peripheries: 16x100µm FET cells at the 1st stage, 32x100µm at the 2nd stage and 32x100µm at the output stage.

Figure 4. Block diagram of power amplifier MMIC.
3.3 RF performance

Figure 5 shows the s-parameters of the power amplifier MMIC. The measured small signal gain S21 is about 18 - 20 dB at frequency from 26 to 30 GHz. The maximum in-band input S11 and output S22 return losses are 17 dB.

![Figure 5. S-parameters of the power amplifier MMIC.](image)

The large-signal performance of power amplifier MMIC is shown in Figure 6. The output power at P-1dB of 1W (30dBm) was demonstrated over a range of frequency from 26 to 30 GHz. The efficiency at P-1dB is 10% at the 26 GHz and dropping to 22% at 30 GHz.

![Figure 6. Large-signal performance of the power amplifier MMIC.](image)

4. Conclusions

5G communications promises to offer the user the perception of near infinite capacity. This requires a step change in data rates that will be facilitated by a move to higher transmission frequencies where
wider bandwidths are more readily available. The 28 to 30 GHz band is a strong candidate for the new 5G radio interface and much of the research undertaken to date has considered this band.

This paper describes the design, layout and performance of power amplifier (PA) monolithic microwave integrated circuit (MMIC) 26 – 30 GHz band based on 0.25µm gate length GaAspHEMT process. Power amplifier provides an output power capability of 1 W at 1dB gain compression (P-1dB) and PAE of 20% with small signal gain of 20 dB. The developed PA MMIC has similar RF performance to the same RF devices from the biggest mass-production vendors [17 – 18]. The reliability of fabricated devices will be investigated in the future work.

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