Capstan: A Vector RDA for Sparsity

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ABSTRACT

This paper proposes Capstan: a scalable, parallel-patterns-based, reconfigurable dataflow accelerator (RDA) for sparse and dense tensor applications. Instead of designing for one application, we start with common sparse data formats, each of which supports multiple applications. Using a declarative programming model, Capstan supports application-independent sparse iteration and memory primitives that can be mapped to vectorized, high-performance hardware. We optimize random-access sparse memories with configurable out-of-order execution to increase SRAM random-access throughput from 32% to 80%.

For a variety of sparse applications, Capstan with DDR4 memory is 18× faster than a multi-core CPU baseline, while Capstan with HBM2 memory is 16× faster than an Nvidia V100 GPU. For sparse applications that can be mapped to Plasticine, a recent dense RDA, Capstan is 7.6× to 365× faster and only 16% larger.

CCS CONCEPTS

• Hardware → Hardware accelerators; Reconfigurable logic applications; Emerging languages and compilers; • Computer systems organization → Reconfigurable computing; • Computing methodologies → Parallel programming languages.

KEYWORDS

reconfigurable dataflow accelerator, RDA, CGRA, parallel patterns, sparsity, sparse iteration, vectorization

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With all else equal—process node, die area, and algorithm—a single-purpose ASIC would outperform its programmable counterparts by hyper-specializing its memory hierarchy, data movement, and compute-memory ratio. However, when building bespoke accelerators, every specialization (e.g., low precision and on-chip memory capacity) is a gamble that ML algorithms will remain unchanged over the roughly five years between design and decommissioning. Furthermore, expensive hardware (e.g., HBM, large die, or leading process nodes) and complicated design steps (e.g., multiple power domains, full-custom datapaths, or low-swing interconnects [26]) are hard to justify in bespoke accelerators. Finally, every semi-reconfigurable accelerator introduces a new compiler, which prevents the development of cross-domain applications. These factors motivate unified accelerators.

Prior accelerators have focused on a few kernels (e.g., BLAS) with hand-written implementations stitched together by end-users. However, kernel-driven programming makes it challenging to design new applications and eliminates the opportunity for on-chip kernel fusion [5, 79]. For example, Krylov methods (a building block for optimization, simulation, and scientific computing [64]) run multiple sparse and dense kernels which must be fused for efficient execution. Kernel-driven programming has also driven ML towards large batches, which have higher inference latency [33] and worse statistical properties [37].

Furthermore, naïve fusion of streaming kernels is insufficient because every sparse program is also parameterized by input formats, which exploit problem-specific structure in input data. Compiling sparse applications avoids writing, optimizing, and testing hundreds of unique kernels; instead, programmers can get optimized code for tensor computations from an algebraic expression and a list of input data formats. Recent sparse tensor compilers optimize applications over sparse iteration spaces, which are analogous to affine loop nests in dense linear algebra [40]. Sparse iteration spaces support any problem expressible as a tensor sum or product, including ML training and inference, graph analytics [36], simulation, and optimization. Due to the benefits of kernel fusion and input-format specialization, an ideal accelerator for datacenter applications should be programmable beyond stitching together individual kernels.

Reconfigurable dataflow architectures (RDAs) are a promising class of accelerators being explored by industry and academia [8, 55, 57, 66, 68]. RDAs provide a sea of flexible compute and memory resources in a programmable interconnect, enabling dataflow pipelines that exploit parallelism within and between iterations [79]. Most proposed RDAs have focused on primitives benefiting dense workloads, with a vectorized datapath to exploit SIMD parallelism,
a simple memory system, and short buffers at each node’s input to avoid global pipeline interlocks. However, sparse applications present several challenges to efficient use of SIMD datapaths and on-chip memory bandwidth due to their irregularity and dynamic, data-dependent communication patterns. Ideally, unified sparse-dense RDAs should retain efficiency for dense workloads when adding native support for sparse ones.

Mapping sparsity to dense RDAs is complicated by structural hazards (when accessing memory) and control hazards (when iterating). First, sparse applications frequently use pointer-indexed accesses. Multiple concurrent accesses may point to the same memory bank, even though each bank can only serve one access every cycle. Current solutions either tolerate low throughput or over-provision banks and crossbars to minimize conflicts [14]. Second, sparse iteration may have inter-loop control dependences when iterating over two sparse dimensions. Using a scalar programming model [14], each non-zero input would have to be compared before deciding whether to dequeue from one list or another, because each comparison’s result changes the next comparison’s inputs.

Scheduling accesses to avoid structural hazards is complicated by positional dataflow, the typical paradigm for RDAs. In positional dataflow, senders and receivers are synchronized, and loop indices are communicated implicitly via the sequence of data elements [25]. A compute graph can thus be mapped to parallel, pipelined execution units without reordering data elements or sending control information across the network. However, sparsity requires moving a memory request from the originating lane to the correct bank; integration with positional dense computation requires that this shuffling is precisely undone.

In this paper, we introduce Capstan, a positional-dataflow, sparse-dense hybrid RDA that is programmable while approaching bespoke ASICs’ performance. Capstan uses a parallel-patterns abstraction for declarative sparsity: users express what they want to compute, which permits optimized hardware for vectorized sparse iteration and dynamic memory reordering. Capstan supports all sparse-iteration tensor applications with a low-level map-reduce programming model based on Spatial [41] and a clear path to high-level programming (e.g., via TACO [40]).

Capstan lessens the impact of memory-bank structural hazards by scheduling on-chip memory accesses over multiple cycles to increase request-level parallelism without increasing crossbar size. A flexible memory-shuffle network then increases memory parallelism beyond the number of SIMD lanes while respecting the positional constraints needed for sparse-dense kernel fusion. Finally, to enable vectorized sparse iteration in the presence of control hazards, Capstan uses a scanner to make multiple control-flow decisions per cycle while still supporting a wide range of applications. Capstan’s key contributions are:

- An evaluation of a programmable RDA that supports efficient sparse and dense computation, including a comparison against multiple state-of-the-art baselines.
- A memory reordering pipeline that exploits the timing flexibility of a loosely-coupled RDA to increase random-access throughput from 32% to 80%.
- Specialized sparse iteration hardware that exploits declarative sparsity’s flexibility to run multiple loop iterations in a single cycle.

Our primary baseline design is Plasticine [55], a state-of-the-art dense vector RDA. Capstan adds only 16% chip area and 12% power, retains its baseline’s flexibility, performance, and programmability for dense applications, and outperforms all general-purpose and many application-specific baselines. Capstan provides significant performance improvements over Plasticine for sparse applications. The specific speedup varies depending on the limiting characteristic: structural hazards when reading on-chip memory (17×), data hazards when modifying memory (SRAM 18×, DRAM est. 1000×), and control hazards during sparse iteration (est. 17×–131× faster). We also compare with an Nvidia V100 GPU and a four-socket Xeon E7–8890v3, using Capstan with DDR4 memory for the CPU comparison. Capstan outperforms the CPU by 4.4× to 327× and the GPU by 4.9× to 118× despite using fewer resources. Finally, Capstan outperforms state-of-the-art bespoke sparse accelerators (SCNN [53], GraphChic [22], and MatRaptor [61]); Capstan is slower than EIE [23] because it does not have enough SRAM to store matrix data entirely on-chip.

## 2 DECLARATIVE TENSOR SPARSITY

Capstan operates on sparse tensors: k-dimensional arrays of data with some elements being zero. The fraction of non-zero elements is the density, ranging from around one in two to less than one in one quadrillion. Capstan exploits hierarchical parallelism (i.e., along multiple tensor dimensions simultaneously) via loop nests, with multiple iterations of the same loop running in parallel.

We use a low-level programming model based on sparse iteration to express complex computations as linear loops and support a wide variety of tensor formats. This is a declarative model because users do not traverse sparse data structures with comparisons and pointer

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### Table 1: Some formats for sparse matrices (2-D tensors).

| Name | Description |
|------|-------------|
| CSR  | Dense rows, compressed columns. |
| CSC  | Dense columns, compressed rows. |
| COO  | Compressed non-zeros with row/column pointers. |
| DCSR | Compressed rows, compressed columns. |
| DCSC | Compressed columns, compressed rows. |
| Banded | Dense along a subset of diagonals. |
| BCSR | CSR, with \( k \times k \) blocks instead of \( 1 \times 1 \) non-zeros. |

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![Figure 1: Several formats for sparse vector storage. The bit-vector and bit-tree formats are specialized for implementation using fixed-length memories.](image-url)
Table 2: Capstan’s applications expressed as sparse iteration spaces. Brackets indicate iterations: M\(r\)[c] iterates over rows, then columns, while M\(r,c\) iterates over non-zeros (rows and columns simultaneously).

| App       | Data       | Format        | Loop Over               | Iteration            | Rand. Accesses | Operation                  |
|-----------|------------|---------------|-------------------------|----------------------|----------------|-----------------------------|
| CSR SpMV  | V[c]       | Dense         | 1. Matrix Rows          | dense(r)             | Out[r]         | Out[r] = reduced           |
| PR-Pull   | M[r][c]    | CSR           | 2. Cols in Row          | dense(len(M[r]))     |                 | reduced \(\Rightarrow\) M[r][c]*V[c] |
| COO SpMV  | V[c]       | Dense         | 1. Matrix Values        | dense(nnz(M[r]))     | Out[r]         | Out[r] = M(r)*V[c]         |
| PR-Edge   | M[r][c]    | COO           |                         |                      |                 |                             |
| CSC SpMV  | V[c]       | CSC           | 1. Non-Zero Inputs      | sparse(V)            | M[r][c]        | Out[r] = M(r)[c]*V[c]      |
|           | M[r][c]    | Dense         | 2. Rows in Col          | dense(len(M[r]))     |                 |                             |
| Conv      | In[i][c][r] | Dense/COO     | 1. Input Non-Zeros      | sparse(In)           | M[r][c]        | Out[r] = In[i][c][r]*M[r][c] |
|           | K[i][c]    |               | 2. Kernel Non-Zeros     | dense(nnz(K[i][c]))  |                 |                             |
|           | Out[o]     |               |                         |                      |                 |                             |
| BFS       | Fr[n]      | Bitset        | 1. Frontier Nodes      | sparse(Fr)           | G[s]           | Pr[d] = Rch[d] \(\Rightarrow\) Pr[d] = Rch[d] |
|           | Dist[n]    |               | 2. Adj. Nodes           | dense(len(G[s]))     | G[s], Dist[s]  | Pr[d] = Rch[d] \(\Rightarrow\) Pr[d] = Rch[d] |
|           | G[n][a]    | CSC           |                         |                      |                 |                             |
|           | Ptr[n]     | Dense         |                         |                      |                 |                             |
| SSSP      | Fr[n]      | Bitset        | 1. Frontier Nodes      | sparse(Fr)           | G[s]           | Pr[d] = Rch[d] \(\Rightarrow\) Pr[d] = Rch[d] |
|           | Dist[n]    |               | 2. Adj. Nodes           | dense(len(G[s]))     | G[s], Dist[s]  | Pr[d] = Rch[d] \(\Rightarrow\) Pr[d] = Rch[d] |
|           | G[n][a]    | CSC           |                         |                      |                 |                             |
|           | Ptr[n]     | Dense         |                         |                      |                 |                             |
| M+M       | A[r][c]    | CSR-BitTree   | 1. Matrix Rows          | dense(r)             | A[r][c], B[r][c] | C[i][l] = end \(\Rightarrow\) C[i][l] = 0 + C[i][l-1] \(\Rightarrow\) end |
|           | B[r][c]    |               | 2. Cols in Rows (\(\_\)) | sp-sp(A[r],B[r])    |                 |                             |
|           | C[i][l]    | CSR-BitTree   |                         | sp-sp(A[r],B[r])    |                 |                             |
|           | CSR        |               |                         | sp-sp(A[r],B[r])    |                 |                             |
| SPMspM[21] | A[i][j]    | CSR           | 1. Output Rows          | dense(i)             | A[i][j], B[j][k] | C[i][l] = end \(\Rightarrow\) C[i][l] = 0 + C[i][l-1] \(\Rightarrow\) end |
|           | B[j][k]    | CSR-Bit      | 2. Dim C                | dense(len(A[i][j]))  |                 |                             |
|           | C[i][k]    | CSR           | 3. Output Cols          | dense(len(B[j][k]))  |                 |                             |
|           | Val[i][k]  | Bitset        | 3c. Output Cols         | sp-Val[i][k]         |                 |                             |
|           | Bitset     |               |                         | sp-Val[i][k]         |                 |                             |

 increments. Instead, hardware transforms the sparse data-structure into an iterable list of pointers, which permits a higher-performance implementation.

2.1 Sparse Tensor Formats

There are many ways to store sparse tensors [11], as shown in Table 1. Formats are specialized based on both the structure of the tensor (are the non-zeros clustered together?) and the operation to be performed (row-first or column-first iteration?). Any multi-dimensional tensor storage format is a hierarchy of lower-dimensional formats, with the lowest-level formats storing vectors (Figure 1).

For example, consider the venerable compressed-sparse row (CSR) matrix format. Iterating along rows, the matrix is dense with one entry per row; sparsity is only exploited among columns within a row. If iteration along rows were sparse, the matrix—with the same row format—would be a doubly-compressed sparse row (DCSR) matrix. Compressed-sparse column (CSC) also uses one dense and one sparse axis; it permits skipping columns that would be multiplied by zero. Coordinate (COO) matrices permit iteration only over non-zero tensor values—not rows or columns—with more efficient storage for extremely sparse matrices. Other formats—especially for vector architectures—use block sparsity (e.g., BCSR), with small (e.g., 16 × 16) dense regions instead of individual elements.

Finally, some dense vectors (e.g., frontier sets) have boolean elements, motivating a packed bit-vector format. Bit-vectors can also implicitly point to elements in a compressed array. Capstan is designed to support all of these formats; we test it with CSR, CSC, and COO matrices to capture a variety of traversal behaviors. As described below, we convert compressed vectors to packed bit-vectors (and a bit-tree variant, Section 2.3) for certain operations.

2.2 Sparse Iteration Spaces

Map-reduce parallelism breaks every problem into three parts: an iteration space, a pure (no side effects) scalar function, and a reduction function. Consider multiplying two dense matrices \(A\) and \(B\), with sizes \(i \times j\) and \(j \times k\): \(C_{ik} = \sum_j A_{ij}B_{jk}\). This kernel iterates over three dimensions: \(i \times k \times j\) ⇒ \(A_{ij}B_{jk}\), and the reduction sums along the \(j\) dimension to yield a two-dimensional result: \(C_{ik} = \sum_j A_{ij}B_{jk}\).

In a dense system, \(i, j, k\) would be generated by counters, which can be generalized to sparse iteration spaces by making one or more iterated dimensions sparse. Kjolstad [40] provides a comprehensive introduction to sparse iteration spaces; here, we focus on the theory needed to map sparse applications to dataflow architectures.

Compressed dimensions are the simplest case and can be handled entirely by indirect memory accesses. Assume that \(B\) is dense and \(A\) has a compressed-sparse row (CSR) format, which is dense along \(i\) and sparse along \(j\). We start by iterating over \(i\) and \(k\), which are dense, but only iterate over the subset of \(j\) which is non-zero in \(A_i\). Thus, our \(i \times k\) iteration space yields a compressed third dimension that uses a counter \(j'\) to index \(A_i\). This yields a data value \(A_{ij'}\) and
a dense (uncompressed) index \( j \). We are left with dense iteration on a smaller space: \( i \times k \times j' \rightarrow j \Rightarrow A_{ij}B_{jk} \).

Alternately, both \( A \) and \( B \) could be sparse along the \( j \) dimension. For this case, we introduce a hit-vector format to permit efficient intersection or union computation (Figure 2). Intersecting the \( A \) and \( B \) bit-vectors yields an iteration space \( j' \), which maps to compressed indices \( j'A \) and \( j'B \). The indices \( j'A \) and \( j'B \) are not guaranteed to equal \( j' \), because \( j' \) references a dense iteration space (a sequential counter, as in CSR), while \( j'A / j'B \) may skip values in the compressed tiles. This is the optimal iteration space because it does not multiply by zero: \( i \times k \times \text{intersect}(A_i, B_k) \rightarrow j', j'A, j'B \) \( \Rightarrow A_{ij}B_{jk} \).

Finally, values along the \( j \) dimension must be summed. If the \( j \) dimension is the last (innermost) iterated dimension, then all temporary values for one \((i, k)\) pair will be adjacent and can be summed with a dense reduction. However, an outer-product GEMM, for example, starts by iterating along \( j \) and creates temporary results in random order. For such cases, atomic accesses permit coherent in-place updates: \( C_{ik} = C_{ik} + A_{ij}B_{jk} \).

### 2.3 Programming Capstan

Having identified a map-reduce model for sparse iteration, we need to provide users with an equivalent, easy-to-use programming abstraction. Spatial [41] uses a loop-nest abstraction, which lets users nest map-reduce iterations via loop levels. Our Capstan dialect extends current loops (Foreach and Reduce) by adding a Scan statement in the place of counters:

\[
\text{Dense:}\ \text{Foreach}(\text{min until max by step par p}) \{ j => \ldots \} \\
\text{Sparse:}\ \text{Foreach}(\text{Scan(par=p, len=1, A.deq, B.deq)}) \\
\{ j, jA, jB, jorime => \ldots \}
\]

Users can nest dense loops within sparse, sparse within dense, and so forth. They can also write arbitrary code (including atomic accesses) in loop bodies and use sparse and dense reductions at multiple levels. By composing sparse loops natively with dense primitives, Capstan supports the wide variety of applications shown in Table 2. More importantly, by providing an orthogonal, regular programming abstraction, Capstan is more likely to support future applications.

**Bit-Tree Iteration.** Bit-vector sparsity begins to break down when applied to extremely sparse problems (e.g., less than 1% input density), including our matrix-matrix addition benchmark. For such problems, sparse iteration can be nested to support the bit-tree format shown in Figure 1. A two-level bit-tree can encode 262,144 zeros with 512 bits. Streaming iteration on bit-trees is possible using a two-pass algorithm. In the first pass, sparse-sparse iteration over the top-level vectors realigns the lower-level bit-vectors. In union mode, zeros are inserted to balance unmatched second-level vectors; in intersection mode, unmatched second-level vectors are dropped. Finally, the top-level vector and second-level vectors are processed by nested sparse-sparse loops.

For randomly-distributed sparse datasets, bit-tree sparsity would allow low-vectorized throughput. However, real-world datasets are frequently not randomly distributed: instead, values are clustered near the diagonal or in blocks away from the diagonal. When values are clustered, bit-tree iteration is able to vectorize across the values in a cluster.

**Memory Ordering Constraints.** Capstan offers a choice of memory ordering strictness (Table 3). For certain cases (e.g., SSSP and deterministic floating-point accumulation), same-address access reordering is not permissible. Programmers can select address ordering, which permits reordering across addresses but not to the same address. Finally, certain programs may require that no reordering be performed: full ordering is provided for this edge case, although it is slower than our arbitrated baseline (which reorders accesses within a vectorized request).

### 2.4 Case Study: SpMSpM

Row-based (Gustavson’s [21]) sparse matrix-matrix multiply (SpMSpM) is an asymptotically-efficient algorithm that processes each output row in parallel, which makes it a good candidate for pipelined architectures. This SpMSpM variant loops along three dimensions, starting with rows in the output, \( C \), and left input matrix, \( A \). Next, it loops over non-zero column entries in \( A \)’s row \((A_{ij})\) and fetches the corresponding rows from the right matrix \( B \); it multiplies each row \((B_j)\) by the left matrix’s value and (sparingly) adds them to produce the output row: \( C_{ik} = \sum_j A_{ij}B_{jk} \).

When computing each output row on Capstan, the first step is computing the union of the input rows’ bit-vectors, which yields a bit-vector indicating which entries in \( C_i \) will be non-zero. Then, each input bit-vector is intersected with the output indices; this produces addresses that can be used to accumulate directly into a compressed local tile. Finally, the compressed local tile is swapped with zero (to prepare for the next iteration) and written to DRAM using sparse iteration. Pre-computing indices may output zeros if two added values sum to zero, but is more efficient and generally accepted [30]. If zeros in the output are unacceptable, a second sparse iteration pass on \( C_i \) can remove them.

### 3 THE CAPSTAN ARCHITECTURE

This section describes key architectural features in Capstan: dynamically scheduled on-chip sparse accesses, shuffle networks for...
application outer-parallelization, and scanners for sparse iteration. Like Plasticine, Capstan is built as a checkerboard grid of compute units (CUs) and memory units (MUs) surrounded by address generators (AGs), as shown in Figure 3a. In this section, we fix Capstan’s lane count \((l = 16)\), banks per SpMU \((b = 16)\), and local buffer depth \((d = 16)\).

### 3.1 Sparse Memory Unit (SpMU)

On-chip sparse accesses are handled by sparse memory units (SpMUs), which dynamically schedule sparse requests to banks (Figure 3b). The SpMU’s main architectural component is a reordering pipeline added to Plasticine’s MU.

Dense programs have a fixed non-conflicting lane-bank mapping, which is typically an identity map: lane 0 to bank 0, and so forth. However, sparse programs have a random mapping, where multiple lanes may request the same bank; this would require a multi-cycle stall while accesses are resolved. Therefore, Capstan introduces a scheduled pipeline where \(d\) vectors are buffered to stop a single bank conflict from creating a multi-cycle stall.

Scheduling the lane-bank crossbar is non-trivial: up to \(l \cdot d\) candidates from \(l\) lanes bid every cycle for access to \(b\) banks. A greedy solution (lane 0 gets its choice of banks, then lane 1, etc.) is sub-optimal because one lane-bank matching can block multiple other candidates. Making matters worse, head-of-line blocking by straggling requests means that even an exact solution may cause slowdowns later. To identify the best approximation (one that balances hardware resources and performance), we conduct sensitivity studies with random access traces.

Furthermore, some applications (e.g., Conv) have pathological strided access patterns: with a naive, linear bank-mapping scheme, accesses strided by \(2^n\) for \(n \geq \log_2 b\) will hit the same bank and must be serialized. Therefore, we hash addresses to get a bank ID \((a_0; 3 @ a_4; 7 @ a_8; 11 @ a_{12}; 15)\) that guarantees that any stride will map to sequential banks. Hashing is a common technique for eliminating pathological effects of strided accesses (e.g., in caches [58]).

As shown in Figure 3b, every memory access pending in the issue queue first bids for access to its bank \(\Theta\). Then, an allocator computes a valid crossbar configuration. Following allocation, the SpMU configures its crossbars to route requests from the input queue lanes to banks \(\Theta\). Because the issue queue can only issue one request per lane regardless of queue depth, crossbar size is independent of scheduling depth. Otherwise, the crossbar needed would grow from \(1 \times b\) to \(l \cdot d \times b\). The allocator’s decisions travel through the pipeline over multiple cycles—the decision made for crossbar traversal in cycle \(n\) will control reads in cycle \(n + 1\) and writes and the output crossbar in cycle \(n + 2\).

Each request then enters an independent read-modify-write (RMW) execution pipeline with one SRAM bank and an FPU (Floating Point Unit) \(\Theta\), which is capable of integer and floating point addition and subtraction along with several bitwise operations. The execution unit has separately configurable result muxes for returned data and updated memory values, which allows operations like test-and-set, write-if-memory-zero, swap, min-report-changed, and max. For example, min-report-changed can be used for SSSP distance updates, and write-if-memory-zero can be used to avoid overwriting backpointers in BFS. Finally, another crossbar inversely permutes the data based on the bank allocation and writes to the
output queue $\mathcal{Q}$. When all requests in a vector complete, the vector is ready to dequeue.

### Allocation

The detailed allocation process is shown in Figure 3c. The first stage of allocation is hashing input addresses into bank requests and converting them to one-hot vectors ($b \times l$). The $d$ one-hot vectors in each lane are bitwise-ORed into a vector with all requested banks $\mathcal{B}$; concatenating lanes' requests forms a $l \times b$ request matrix. The request matrix's rows correspond to banks and columns correspond to lanes: if $R_{ij} = 1$, then there is at least one request from lane $i$ to bank $b$. A three-iteration, input-first $l \times b$ separable allocator identifies a set of non-conflicting accesses (at most one per lane and one per bank). If a lane in the issue queue contains multiple requests to the same bank (e.g., lane 1 has two requests for bank 3), a per-lane priority encoder grants the oldest request again.

Every separable allocation [6] iteration consists of two stages of fixed-priority arbiters. The first stage prunes the matrix so that every lane requests at most one bank, and the second stage ensures that every bank selects at most one lane. These two pruning steps guarantee at most one grant per bank and lane. However, if the first iteration chooses suboptimally, more grants could be added. Successive stages consider requests that were not previously granted and do not conflict with established grants.

Our allocator prioritizes older requests because they can cause head-of-line blocking. In Capstan’s 16-slot queue, the first five slots bid in the first round of allocation, the first ten slots bid in the second round, and all bid in the third. The performance benefits of multiple priorities are shown in Table 4, with every design point showing a fully ordered pipeline. For our final design, we choose a 16-entry queue without speedup to balance area and performance; however, it is interesting that the 16-entry queue with speedup is faster than the 32-entry queue while consuming less area.

### Crossbar Size

In most banked memory systems, arbitration is simplified by overprovisioning banks. However, with allocation, adding crossbar inputs can also increase throughput (Table 4). Banking the input queue to feed a $2 \times l \times b$ crossbar (i.e., 2+ input speedup [16]) improves performance slightly but adds 11,559 $\mu$m$^2$.

For our final design, we choose a 16-entry queue without speedup to balance area and performance; however, it is interesting that the 16-entry queue with speedup is faster than the 32-entry queue while consuming less area.

### Address Ordering

The SpMU’s pipeline performs arbitrary reordering of requests, which is typically (but not always) permissible. To ensure address-based ordering, the SpMU must stall requests before they enter the reordering pipeline if they may conflict with in-flight requests. The first step is splitting request vectors if two lanes request the same address. Splitting is visible in Figure 4 as the first access to bank 10 being stalled by one cycle due to a split at bank 12. Next, a 128-entry Bloom filter checks for potential conflicts with pending in-queue requests. Using 128 entries provides reasonable performance for this less-common access mode while consuming less area.

### Repeated-Read Elision

During enqueuing, duplicate read-only accesses are squashed and replaced with metadata indicating the lane of the initial (un-squashed) access. When the vector is dequeued, duplicate lanes fill from the one read that performed.
The scanner, which implements sparse loop headers, is a relatively simple block: the key insight is that it requires \( O(\log n) \) levels of logic, which is less than the \( O(n) \) levels that would be required to run arbitrary independent decisions (e.g., stream join [14]). The simplest scanner is the data scanner, which identifies one 32-bit non-zero element in a 16-element vector per cycle. Because the data scanner can only scan 16 elements per cycle, vectorization could not out-perform dense computation; therefore, the data scanner is not used in inner loops.

The bit-vector scanner (Figure 3f), which is used for vectorized sparse iteration, starts by computing either the intersection or union of its inputs ➊. It then identifies the first 16 set bits, which, in a single cycle, it passes into a pipeline and then clears. Because this is a fairly simple operation, the scanner can easily process one input per cycle.

In the pipeline, the 16 selected bits are passed into encoders ➋ as a 256×16 array to produce the dense indices ➋. Finally, the scanner uses these indices to index prefix sums over the inputs and provide indices into compressed input vectors \( (A^j/B^j) \). If the bit was not set in the input (union mode only), −1 is returned as the index. Table 5 shows how scanner area varies with width and vector length. By choosing a 256-input, 16-output scanner, we use 54% less area than the largest option, 512×16, which also fails to meet timing.

Scanning is performed before values enter the counter chain: in the first cycle, the scanner outputs the number of valid elements. This count is written into the appropriate counter and used for iteration, which avoids the need to replicate one scanner per counter level. For programs that nest more than one scanner, a CU can be used in a scanner-only mode to feed a second CU. This scanner-only CU also reduces vector input buffer requirements: the follower CU only needs one vector buffer to hold packed indices, instead of two buffers to hold bit vectors. Finally, SpMUs do not have the full scanner provisioned, but instead have a single-input, scalar-output scanner that adds less area. When a complicated scan operation is needed for address generation, a CU must be used instead.

### 3.4 Off-Chip Access Support

Atomic DRAM Accesses. Capstan’s atomic DRAM support uses a similar pipeline to the on-chip SRAM and is present in every DRAM address generator (AG). The AG tracks the current status of outstanding bursts; when a new request vector arrives, each access is checked against pending bursts and issued if necessary. After executing the relevant accesses, the burst is written back to DRAM, ensuring that no reads race writes—if a read would race a write, it is instead marked as pending and executed when the write returns. To parallelize DRAM accesses, the shuffle network ensures that each AG is responsible for a mutually-exclusive memory region. Random-access DRAM bandwidth is limited by the memory controller and technology, so Capstan’s DRAM AGs are less sensitive to architectural parameters.

Compressed Dense DRAM. Read-only DRAM compression is used to optimize applications that read tiles of pointers (which have closely-spaced values). Capstan uses a packet-based memory compression format, with each burst encoded using a base/off-set format; a one-byte header specifies the base and offset sizes. Unlike GPUs, which compress framebuffers in large tiles without programmer input, Capstan requires pre-compression and restricts compressed loads to tile boundaries. Removing support for writes and random reads permits denser compression and saves area.

### 3.3 Sparse Loop Headers: Scanner

Table 5: Area of various scanner configurations (\( \mu \text{m}^2 \)).

| Width | Output Vectorization |
|-------|----------------------|
|       | 1       | 2       | 4       | 8       | 16      |
| 128   | 2157    | 2765    | 3445    | 5591    | 9456    |
| 256   | 3985    | 5231    | 6927    | 10674   | 19898   |
| 512   | 7777    | 10447   | 14377   | 22562   | 42997   |

The scanner, which implements sparse loop headers, is a relatively simple block: the key insight is that it requires \( O(\log n) \) levels of logic, which is less than the \( O(n) \) levels that would be required to run arbitrary independent decisions (e.g., stream join [14]). The simplest scanner is the data scanner, which identifies one 32-bit non-zero element in a 16-element vector per cycle. Because the data scanner can only scan 16 elements per cycle, vectorization could not out-perform dense computation; therefore, the data scanner is not used in inner loops.

The bit-vector scanner (Figure 3f), which is used for vectorized sparse iteration, starts by computing either the intersection or union of its inputs ➊. It then identifies the first 16 set bits, which, in a
Table 6: The datasets used to evaluate Capstan. Convolution dimensions are dim\*kdim\*inCh\*outCh and activations\*kernel for non-zeros and density.

| Name            | Dim. | Non-Zeros | % Dense |
|-----------------|------|-----------|---------|
| chkl11752_d0    | 49762| 333,029   | 0.014   |
| Trefethen_20000 | 20000| 554,466   | 0.139   |
| bcast430        | 28924| 2,043,492 | 0.244   |
| usroads-48      | 12646| 323,900   | 0.002   |
| web-Standard    | 281903| 2,312,497 | 0.003   |
| flickr          | 820,878| 9,837,214 | 0.001  |
| spaceStation_4  | 950   | 14,158    | 1.6     |
| qc324           | 324   | 27,054    | 25.7    |
| mbeaccc         | 496   | 49,920    | 20.3    |
| ResNet-50 #1    | 56,044| 8837,1229 | 44.3\%  |
| ResNet-50 #2    | 56,044| 47,574,1105| 23.7\%  |
| ResNet-50 #29   | 13,025,256| 41,552,176,460| 82.8\% |

Table 7: Capstan’s design parameters.

| Off-Chip Bandwidth | HBM-2E | 1,800 GB/s |
|--------------------|--------|------------|
| Grid Size          | Compute Unit | 200 |
| SpMU               | Banks   | 16         |
|                    | Capacity | 256 KB     |
| Shuttle Network    | On-Chip | 2\times16 |
|                    | Off-Chip | 4\times16 |

Applications, we start with binding assumptions about several parameters: vector length, grid layout, and on-chip SRAM banks and dimensions (Table 7).

**4 EVALUATION**

We evaluate Capstan’s performance using a custom cycle-accurate C++ simulator, which has previously been used to evaluate other Plasticine-based RDA [65, 75, 77]. Our simulator models the effects of a hybrid static-dynamic network [75] and uses Ramulator [38] to model DRAM behavior. Applications are written in a dialect of the Spatial language and simulated using the datasets shown in Table 6; for DRAM bandwidth and scanner sensitivity studies, p2p-Gnutella31 [44] is substituted for Flickr to make simulation more feasible. Datasets with many nodes (e.g., Flickr [44]) stress the performance of cross-tile applications—important when scaling out to larger graphs. To evaluate convolution, we train a ResNet-50 model and prune it to be 30% dense. For CSC SpMV (sparse matrix-vector multiplication), we use a 30%-dense input vector (based on the datasets used to test EIE [23]). Graph datasets are tiled using Metis [35] with nodes weighted by edge count to give load-balanced tiles. Linear algebra datasets are tiled using a round-robin division of rows, columns, or non-zero matrix values.

**Convolution Mapping.** All of our evaluated applications can be mapped using Spatial. However, due to halo exchange, convolution maps poorly to positional dataflow: in a streaming-positional architecture, each tile’s accumulation buffer would need eight links (input and output) to neighboring tiles. Although we can map convolution to the shuffle network using Spatial (using 100% of the on-chip shuffle resources), using the dynamic network [75] in a non-positional (i.e., out-of-order) mode yields 3.8x higher performance. Without manual mapping, Capstan still outperforms a CPU and GPU; however, manual mapping is used to compare against SCNN (which uses a similar tiled architecture).

**4.1 Capstan Architectural Parameters**

We use Plasticine, a recent dense RDA [55], to evaluate Capstan’s hardware costs. Both Capstan and Plasticine are programmed using the Spatial language [41] and SARA low-level compiler [27]. Because modifying Plasticine could lower performance for dense slowing execution. Therefore, special-purpose format conversion hardware is added to the compute tile with minimal area overhead.

**4.2 Hardware Resources**

To estimate Capstan’s hardware requirements, we synthesize Plasticine and the added Capstan units with Synopsys Design Compiler and the 15 nm FreePDK15 predictive library [45] at 1.6 GHz. Because FreePDK15 lacks a memory compiler, we scale SRAM area from a 28 nm industrial memory compiler; this scaling is represented equally in the Plasticine and Capstan results. To simplify application mapping (important for getting good on-chip network performance [55]), we matched our baseline’s homogeneous compute layout with one scanner per compute tile and one scheduler per memory tile.

Overall, Capstan is 16% larger than Plasticine and consumes 12% more on-die power (Table 8)—with Capstan’s speedup, this would yield much lower energy consumption. Capstan’s critical path is
in the CU’s compute pipeline, so it has the same clock frequency and dense performance as Plasticine. A detailed area comparison of Capstan and the V100 is challenging because the GPU has both additional hardware (DRAM interfaces, IO, etc.) and more efficient physical design. However, the significant difference (185 mm$^2$ vs. 815 mm$^2$) points to Capstan beating the V100 by a wide margin.

Finally, our area and power overheads are shown for a homogeneous design: every CU, MU, and AG is sparsity-enabled, which demonstrates the best sparse performance achievable. However, if sparse algorithms were less important than dense ones, a designer could provision a fraction of the sparse logic (e.g., 50% of CUs and MUs with sparsity). This would halve peak sparse performance while linearly decreasing the area and power overhead.

### 4.3 Sensitivity Studies

In Section 3, we performed several sensitivity studies using synthesis and microbenchmark simulation to quantify the trade-offs involved in individual units. Here, we detail broader studies performed using full applications.

**Resources.** One reason that Capstan was designed as an extension to Plasticine is to *scale up* to large chips and high memory bandwidth. Figure 5b demonstrates Capstan’s area scaling as outer-parallelization is varied—nearly linear scaling implies that Capstan could be extended to even larger die sizes if memory bandwidth were available. Similarly, the most data-parallel Capstan applications (SpMV, PR) are memory-bound even with 900 GB/s HBM2 memory bandwidth (Figure 5a); even less parallel applications (BFS, SSSP) still benefit from up to 500 GB/s. PREdge and COO see the best compression speedups (Figure 5c) because they load two point-ers for every data element, with repeated (i.e., highly compressible) source-node pointers.
Table 12: Runtimes normalized to the fastest Capstan-HBM2E version of each application. Bolded points are used for geometric means; not all baselines support all application variants.

|                | SpMV | PageRank |
|----------------|------|----------|
|                | CSR  | COO      | CSC    | Conv | Pull | Edge | BFS  | SSSP | M+M | SpMSpM | BiCGStab | gmean |
| Capstan (Ideal Net & Mem) | 0.83 | 1.21 | 0.81 | 0.95 | 0.79 | 1.06 | 0.65 | 0.73 | 0.86 | 0.88 | 0.94 | 0.82 |
| Capstan (HBM2E) | 1.25 | 1.67 | 1.00 | 1.00 | 1.00 | 1.33 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Capstan (HBM2) | 1.78 | 2.26 | 1.27 | 1.01 | 1.37 | 1.73 | 1.28 | 1.20 | 1.35 | 1.53 | 1.19 | 1.27 |
| Capstan (DDR4) | 18.16 | 21.94 | 10.49 | 1.53 | 12.08 | 14.00 | 5.24 | 3.89 | 8.20 | 6.89 | 13.43 | 6.45 |
| Plasticine (HBM2E) | 17.94 | 184.16 | 365.09 | 8.48 | 7.57 | 10.30 | 7.57 | 10.30 | 7.57 | 10.30 | 7.57 | 10.30 |
| V100 GPU | 6.16 | 119.39 | 8.68 | 31.64 | 13.59 | 12.25 | 41.79 | 22.19 | 20.50 | 22.19 | 20.50 | 22.19 |
| 128-Thread CPU | 67.86 | 640.31 | 485.64 | 99.86 | 52.91 | 62.29 | 68.29 | 73.90 | 2,254.09 | 143.03 | 117.50 | 117.50 |

![Figure 6: Capstan’s sensitivity to scanner width, relative to a maximal (512 input, 16 output) scanner.](image)

**On-Chip Memories.** In addition to system-level evaluations, we performed several sensitivity studies to capture the impact of Capstan’s allocated sparse memories and cross-partition communication for outer-parallelized apps. If Capstan’s memories were arbitrated (executing accesses from one vector at a time), it would be 27% slower on average and up to 90% slower for certain applications (Table 9), even with address hashing. As we previously demonstrated, using a multi-iteration, multi-priority allocator further improves theoretical throughput, and this carries forward to a system-level speedup—an average of 15% and peak of 39%. The allocator is small (Table 8), so these speedups are effectively free, just from using the crossbar and memory banks more efficiently. Capstan’s allocated design is also only 8% slower than an ideal SpMU that does not model any bank conflicts. Finally, Table 10 confirnns, at a system level, the microbenchmark results in Figure 4.

The shuffle network (Table 11) improves performance by keeping cross-tile accesses on-chip; the speedup is more pronounced for DDR4, which has less bandwidth. As mentioned in Section 3.2, the shuffle network is not a full crossbar, which would be too expensive. Instead, we shift input lanes in each vector by up to one position (Mrg-1) to increase the merge success rate. Shifting arbitrarily (full crossbar, Mrg-16) provides minimal benefits, and not shifting lanes at all (Mrg-0) slows down applications with cross-partition communication. Data partitioning reduces cross-partition communication for graph applications, but convolution uses the shuffle network to avoid a separate halo-exchange pass. For convolutions with $3 \times 3$ kernels, Mrg-0 is up to 15% slower.

**Scanners.** Finally, we investigated scanners’ impact on performance (Figure 6). Bit scanners—which traverse more zeros—are sensitive to scanner length, with a massive slowdown for the scalar case (a single bit). Even scanning 128 bits would slow M+M by 21%, so we scan 256 bits per cycle. Shorter data scanners are less impactful, with a peak slowdown of only 16% on Conv. However, data scanners are small, so we use a data scanner with 16 inputs.

Scanner output vectorization is also important, with impact varying based on the application. Only outputting eight elements per cycle has a significant performance impact on SpMSpM, because its datasets are relatively dense; for M+M, which is evaluated with sparser matrices, the gains from added vectorization are lower. However, even very sparse matrices have denser sections (frequently, near the diagonal); vectorization helps run these faster.

### 4.4 Performance

Table 12 shows Capstan’s performance compared to several optimized baseline designs. CPU baselines are TACO [39] for sparse linear algebra and GraphIt [76], both using 128 threads on a four-socket Xeon E7-8890 v3 [31]; GPU baselines are cuSparse [50] and Gunrock [67] run on a V100 GPU [49]. Capstan outperforms the CPU and GPU baselines by a large margin, with the largest performance increases for applications relying heavily on sparse memory accesses. Several Capstan features, including cross-tile sparse updates (Conv), sparse DRAM updates (PREdge), and sparse iteration (BFS, SSSP, M+M, and SpMSpM) cannot be mapped efficiently to Plasticine, so only some applications have Plasticine baselines.

To demonstrate the benefits of streaming kernel fusion, we implemented a stabilized Biconjugate Gradient solver (BiCGStab) [64], which is a linear least squares solver that combines sparse matrix-vector multiplication and dense dot products. The CPU and GPU baselines implement BiCGStab using sparse and dense kernels; the inter-kernel overhead causes up to a 3× slowdown relative to sparse SpMV alone. However, Capstan (and Plasticine) can fuse these kernels into a streaming pipeline, which lowers memory bandwidth requirements and the latency of each iteration. Capstan’s Plasticine-relative speedup is lower on BiCGStab because they have the same dense performance.

**ASIC Comparison.** Table 13 shows Capstan’s performance compared against recently-proposed ASICs. The EIE and SCNN comparisons are run against an ideal (i.e., ignoring network delays,
bank conflicts, and load/store time) model of each baseline. When comparing against EIE, we exclude Capstan’s network latency and load/store time to provide a comparison of compute throughput between the two architectures. For SCNN, we use the manually mapped non-positional variant described earlier in this section. The Graphicionado comparison is run against published edge-processing rates on the flickr and fb [69] datasets using DDR4 memory for Capstan, providing a more accurate result. Also, we use BFS and SSSP variants that do not write back-pointers for a fairer Graphicionado comparison. MatRaptor is compared against its highest demonstrated throughput (10 GOP/s). Because the Graphicionado and MatRaptor baselines use detailed simulations, we include load and store time for the Capstan comparison.

Capstan starts with the advantage of a higher core clock (1.6 GHz) than most accelerators, due to aggressive pipelining in the CU and SpMU. A faster clock provides the biggest advantage for convolution and matrix-matrix multiply, which are almost entirely on-chip; the graph algorithms see little benefit because they are heavily DRAM-limited. CSC is an intermediate case, having significant on-chip processing interspersed with DRAM loads of matrix data.

Capstan under-performs EIE for two key reasons: EIE stores model weights entirely on-chip, while Capstan fetches them from HBM, and EIE has more scalar tiles, which do not suffer from under-vectorization. Vectorization can provide significant benefits, though, by increasing peak throughput. Capstan can process up to 128 elements per cycle—16× more than MatRaptor, which uses eight scalar pipelines. Capstan and Graphicionado are both DRAM-limited; this comparison shows that Capstan does not rely solely on DRAM bandwidth for performance.

SCNN is designed using a 2-D multiplier array that processes four activations and four weights per cycle; for layers with few activations, 75% of this array is unused. However, for layers with more activations and fewer weights, the shorter vector lengths can increase utilization. Capstan’s relatively large on-chip memory also provides a slight performance benefit: SCNN is forced to tile its outputs, which limits the amount of available weight parallelism and forces multiple iterations.

Stall Breakdown. Every Capstan application has multiple outer-parallel pipelines, each with sixteen vector lanes. In Figure 7, we look at limiting factors to identify why every lane is not performing useful work in every cycle. We start with a synthetic analysis, which tells us how many cycles would be needed if every lane were active in every cycle (Active). We then look at lanes that are inactive because their associated scanner is processing an all-zero vector (Scan) and lanes that are waiting for data to be loaded from or stored to DRAM (Load/Store). For the synthetic analysis, load/store time assumes zero-latency, infinite-bandwidth DRAM. Next, our synthetic analysis shows lanes that are underused because vectorized loops are too short (Vector Length) or because workload interleaving generates unevenly-sized tiles (Imbalance). We then simulate, adding in on-chip pipelining and network effects (Network), bank conflicts (SRAM), and the Ramulator HBM2E model (DRAM). By adding these one at a time, we identify the cycles that are lost to each stall source.

The on-chip network has a large impact on BFS and SSSP because they cannot be pipelined between iterations; conversely, SpMSpM can easily be pipelined, which leads to high activity factors. Load times are over-represented for some applications (COO–CSC) because we assume that all data is loaded from and stored to DRAM and measure end-to-end latency for a single iteration. If these kernels were run as part of a pipeline, data could be passed through SRAM multi-buffers [55] and efficiency would increase. Moreover, PRPull and PREdge behave differently. PRPull suffers from under-vectorization because many graph vertices have very few in-edges. However, PREdge suffers from SRAM conflicts on datasets which have a power-law distribution, where some vertices have many in-edges that cannot be coalesced. Therefore, it is important to be able to choose between pull and edge-based execution.

5 RELATED WORK

Graph Accelerators. FPGAs have been proposed for graph analytics, including primitives [46, 51, 71, 80] and specialized compilers [15, 48]. However, FPGAs are too flexible: Capstan provides optimized iteration hardware for common parallel patterns, with better logic density and faster clocks. Graph accelerator ASICs like Tesseract [2, 73], GraphPR [60], and Graphicionado [22] use memory systems (HMC, ReRAM, and eDRAM) and architectures specialized for graph analytics. Intel’s PIUMA [1] is similar but CPU-based, with highly multi-threaded cores and gather/scatter offload engines. Finally, PolyGraph [13], which adds a task-scheduling core to an RDA for frontier-set graph algorithms, demonstrates the value of switching between graph algorithm variants. However, separating graph analytics and linear algebra may preclude new applications, like graph neural networks [72]. Furthermore, having high-level
compilers targeting performant hardware for graph analytics will let domain experts focus on optimizing their algorithms instead of forcing them to design hardware or write low-level code.

**Sparse Linear Algebra Accelerators.** Other ASICs have been proposed for sparse linear algebra and deep-learning inference, as summarized by Dave et al. [17]. ExTensor [28] uses hardware to hierarchically eliminate computations on sparse tensors. Gamma [70] and MatRaptor [61] implement row-product SpMSpM while OuterSPACE [52] and SpArch [78] use outer-product SpMSpM; Capstan supports these algorithms (but not SpArch’s priority-queue-driven scheduler). Capstan adds vectorization with bit-vector sparsity. These architectures can only process one intersection per compute stream, per cycle, while Capstan can process up to 16 intersections in a single CU.

Bespoke deep-learning accelerators also limit the available parallelism dimensions: for example, the A100 [10] only supports a sparse matrix-matrix multiply with a restrictive two-of-four format. SCNN [53] requires that parallelism be exploited first across data tiles and then across four weights and four activations per cycle. Cnvlutin [3] skips zeros in CNN activations, and Eyeriss [9] and EIE [23] skip zeros in activations and weights using CSC. Capstan, on the other hand, has generic sparse iteration primitives, flexible inner- and outer-loop parallelism, and automatic pipelining. Capstan’s allocated scratchpad adds area relative to specialized memories like Cambricon-X’s [74] offset indexing. However, the scratchpad is far more powerful, letting programmers change data formats without re-designing hardware.

**Plasticine & Spatial.** Plasticine’s programs are statically banked so no two lanes access the same memory bank in a cycle; memory duplication and buffering are performed as necessary. In the worst banking cases (random accesses), each memory only supports one access per cycle, leaving 15 banks inactive. Plasticine also does not permit read-modify-write (RMW) accesses—for consistent random RMWs, each read must block on the preceding write, introducing multi-cycle bubbles. This is most visible in COO and CSC SpMV, which rely on modifying data. Furthermore, Plasticine has no sparse iteration support, which limits which programs that can be mapped. Finally, Gorgon [65], which is based on Plasticine, can perform joins but lacks support for random memory accesses and updates.

**Other RDAs.** Reconfigurable architectures like DySER [20], Wave-Scalar [62], PipeRench [19], and TRIPS [7] provide support for efficient computation. However, these are designed to execute small, scalar program fragments, which prevents the loop-unrolling parallelism that Plasticine and Capstan use. The MIT Raw [63] processor provides sparse accesses, but relies on the compiler to ensure memory consistency; its sparse accesses are also not vectorized. Compared to these designs, Capstan brings Plasticine’s dense performance improvements to a wider range of sparse problems.

Dadu et al. [14] have recently proposed the SPU, an architecture with tiles combining a sparse memory with an RDA fabric. Each SPU has both a highly-banked scratchpad optimized for sparse operations and a linear scratchpad optimized for dense operations. However, the SPU uses a 16×32 crossbar that only exposes 50% of bank bandwidth—a lower limit than Capstan’s average performance—and its stream-join programming model prevents vectorized sparse iteration. The stream-join model exposes an arbitrary compare-dequeue abstraction, where the results of one comparison change the dequeue decision and thus the arguments to the next comparison. Therefore, vectorizing stream-join would require packing 16 sequential comparisons into a single cycle, which scales poorly to high frequencies. Finally, the SPU’s alias-free indirectness corresponds roughly to Capstan’s unordered memory mode, which precludes applications that require stricter memory ordering.

**Optimizing Accelerator Memories.** Other works propose logical primitives for transferring and packing data into accelerator scratchpads. Buffets [54] coordinate loading and sharing tiles of data between levels of the memory hierarchy, and Stash [42] provides cache-like functionality without the overhead of tag checks. CoRAM [12] optimizes memory transfers to and from an FPGA’s fabric using a programmable, DMA-like interface. Capstan’s SpMU is orthogonal to these approaches: for example, Buffets could be used instead of Spatial to coordinate bulk data transfers between the SpMU and DRAM. Alternately, Capstan’s allocated pipeline could be added to a Buffet or Stash scratchpad, which would simultaneously provide random-access performance and data coordination for dedicated accelerators. Memory compression has also been used before, including for GPUs [27, 43, 59] and sparse matrices [34]; Capstan’s approach is similar to GPUs’ delta-compression but specialized for sparse pointers.

**Allocation.** Allocators have also been explored in networking for crossbar configuration [6, 16]. Network allocators optimize for network metrics, including iSLIP [47] and PIM [4] for fairness and age-based allocation for QoS [32]. Capstan introduces these concepts to memory bank scheduling, evaluating allocation’s benefit and trade-offs in a new context.

**6 CONCLUSION**

In this paper, we introduce Capstan, a reconfigurable, vectorized, streaming, scalable sparse accelerator that also supports dense data analytics. Capstan unifies applications and hardware with sparse iteration modes: these permit algorithmic optimizations and hardware optimizations like vectorization. Capstan’s novel bank-allocation scheme also provides high random throughput (80%) to distributed sparse memories—more than double that of an arbitrated baseline.

With only 16% more area and 12% more power, Capstan brings new applications to Plasticine and runs existing ones 7.6× to 365× faster. Capstan is also significantly faster than CPU, GPU, and several accelerator baselines; the only baseline with better performance is EIE [23] because it is able to store models entirely on-chip, which is impractical for a general-purpose accelerator. We believe that Capstan will drive future research into sparse hardware—it demonstrates that vectorized RDAs can run sparse applications and that using an explicit, limited set of sparse iteration primitives lets hardware extract more parallelism.

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