Design of weak magnetic signal detection system for residual stress detection

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Abstract. The residual stress detection based on eddy current method belongs to weak signal detection. Aiming at the problems of sensor output signal with many channels, large amount of data, wide frequency range and low signal-to-noise ratio, a weak magnetic signal detection system is designed and implemented with Zynq-7020 (ARM+FPGA) as the development board and peripheral hardware circuit. Among them, FPGA controls the peripheral chip to complete the signal source excitation and 8-channel high-speed data acquisition and preprocessing, and then the data is transmitted to ARM through AXI bus. ARM extracts the signal characteristics through digital orthogonal lock-in amplification technology according to the control parameters provided by the upper computer, and feeds back the results to the upper computer. The test results show that the system has high stability and detection accuracy, and meets the overall requirements of the system.

1. Introduction

Eddy current testing technology [1] is a nondestructive testing method based on electromagnetic induction effect to judge the properties and states of conductive materials by detecting the changes of induced eddy current inside conductive materials. Compared with other nondestructive testing methods, it has the advantages of low cost, fast detection speed and easy operation. The reason why residual stress is detected by eddy current method is that the residual stress inside the metal component causes the change of material conductivity, thus affecting the eddy current magnetic field distribution. Therefore, the residual stress can be detected by detecting the change of eddy current magnetic field [2]. Residual stress testing using planar array type electromagnetic sensors [3] as the sensitive element. In the detection process, the change of transfer impedance caused by residual stress is very small, and the output signal of planar array sensor is very weak with high signal frequency, fast acquisition speed and large data volume. However, the current weak magnetic signal detection system has a large volume problem, and the detection speed and accuracy need to be improved. From the perspective of miniaturization, high speed and high precision, this paper designs a weak magnetic signal detection system for residual stress detection based on ARM+FPGA. The system provides sinusoidal excitations for magnetic sensors and collects signals. Secondly, the digital orthogonal locking amplifier is designed, and the feature extraction is completed by giving full play to the advantages of digital orthogonal technology, such as large dynamic range, small linear distortion, small zero drift and high measurement accuracy.
2. Overall analysis of detection system
The magnetic eddy current detection system adopts modular structure and embedded system. The system takes the TMR planar array magnetic sensor as the sensing element, provides excitation to it, amplifies, filters and collects the output signal, and obtains the amplitude and phase information of the signal after the digital orthogonal locking amplification processing, so as to realize quantitative detection of the nature and state of the conductive material.

2.1. Development platform
This system uses Zynq-7020 development board, based on Xilinx company's Vivado design suite for development. Zynq has two functional modules, one is the Programmable Logic (PL) module, which is the FPGA part; the second is the Processing System (PS) module, which is the System on a Chip (SoC) part of ARM independent of FPGA. Vivado provides designers with a design process centered on Intellectual Property (IP) core, and the SDK suite provides all the tools needed to create, develop, debug, and deploy embedded software applications on Zynq devices [4].

2.2. Design of overall architecture
The overall structure of the detection system is shown in Figure 1, which is mainly divided into two modules. The first part is the data acquisition module based on PL, including signal source generation chip, A/D acquisition chip and related circuits. It mainly realizes signal source excitation and eddy current signal acquisition of magnetic sensor, and realizes high-speed communication between PL and PS through AXI. The second part is the signal feature extraction module based on PS, which mainly uses the digital orthogonal lock-in amplification technology to extract the features of the acquired signals and communicate with the upper computer.

3. Design of system hardware
The system hardware mainly includes two parts: the signal source excitation of FPGA, 14-bit 8-channel A/D acquisition and signal transmission, and the data processing and control part based on ARM processor.

3.1. Design of FPGA peripheral circuit
The peripheral circuit with FPGA as the core mainly completes the generation of excitation signal, signal acquisition and processing, and the circuit connection is shown in Figure 2. Direct digital frequency synthesis (DDS) technology [5] was used for signal source excitation of the detection system, and AD9954 of ADI company was used as the chip. The AD9954 has an internal 14-bit DAC, which can produce sinusoidal signals up to 200MHz, and can generate zero-crossing signals through the comparator as the basis for timing control. The relationship between output frequency of DDS, frequency tuning word (FTW) and system clock is:

\[ f_s = \frac{(FTW)(f_c)}{2^{32}}, (0 \leq FTW \leq 2^{32}) \]  
\[ f_s = f_c \times (1 - \left(\frac{FTW}{2^{32}}\right) ), \quad (2^{32} < FTW < 2^{32} - 1) \]
Because the output signal of the planar array sensor is very weak, a series of amplification and filtering processing must be carried out on the output signal of the sensor [4]. Only after passing through the conditioning circuit can the signal be collected in the acquisition system, and the collected signal is sent to FPGA through the SPI interface. Analog Device company’s LTC2325-14 was used as the main chip of A/D module in the detection system. The LTC2325-14 is a low-noise, 4-channel, 14-bit ADC with a sampling rate of up to 5MHz and a maximum drift of 20ppm/°C when the reference $V_{REF}$ is 4.096V. Its sampling rate reaches the highest 5MHz and the reference voltage $V_{REF}$ is 4.096V. In this design, COMS mode and DDR mode are respectively used for SPI serial interface and data transmission of A/D acquisition chip. The signed integer data corresponding to the amplitude of sinusoidal signal collected is:

$$D = \frac{V_{\text{max}} - V_{\text{min}}}{2}$$  \hspace{1cm} (3)

Since the A/D chip selected is a 14-bit chip, the amplitude of sinusoidal signal collected is:

$$v = \frac{D}{2^{14}} V_{\text{ref}}$$  \hspace{1cm} (4)

![Figure 2. Peripheral circuit of FPGA.](image)

### 3.2. ARM core control circuit

The Zynq7000 series provides ARM with a rich peripheral interface. The Multiplexed I/O (MIO) module provides the use and control of up to 54 pins of the software. In this system, the MIO is connected by Quad SPI Flash, USB, SD, UART and GPIO MIO, taking up 27 pins in total. The upper computer is connected to the development board through UART interface, and then it is connected to ARM processor through MIO and APB protocols, SD card is connected to ARM processor through MIO and AHB bus protocols, and DDR3 is connected to ARM processor through L2-Cache for data interaction. In order to meet the demand of high-speed data transmission, data transmission between FPGA and ARM follows AXI bus protocol [6], adopts high-performance AXI_HP interface, and through DDR3 controller realizes reads and writes data in memory. The connection diagram is shown in Figure 3.

![Figure 3. ARM control circuit.](image)
4. System software design

The system software design mainly includes two parts: design of FPGA software and design of ARM software.

4.1. Design of FPGA software

DDS excitation, A/D acquisition and AXI protocol are all completed in FPGA. This system uses Vivado software to encapsulate each part of the program into IP cores, and completes the overall design of FPGA program through the inter-connection of each input and output port of IP cores. The clock control of FPGA software is realized by calling Clock-in-Wizard to multiply the system clock. In FPGA, the DDS exciter can output sinusoidal exciter signals of different frequencies by writing registers and FTW set by upper computer, while the A/D acquisition program can carry out 8-way high-precision acquisition and output. AXI program defines AXI protocol parameters, designs read-write verification program, and communicates with PS through AXI-Smart-Connect. Its structure is shown in Figure 4.

4.2. Design of ARM software

ARM software design mainly uses the SDK part of Vivado design suite to realize the read-write control of interface data and digital orthogonal lock-in amplification technology [7]. Among them, the read-write control of interface data mainly includes SD card read-write control, UART initialization, interrupt control, UART read-write control and DDR read-write control. Digital orthogonal lock-in amplification technology is a weak signal detection technology, with the help of A/D conversion and logical operation, has great flexibility, greatly improves the measurement accuracy, and can accurately extract the signal amplitude and phase characteristics.

The system carries out the design of digital orthogonal lock-in amplification algorithm according to the principle of Figure 5, and the amplitude and phase obtained should be:

\[ A = 2\sqrt{I^2 + Q^2} \]  \hspace{1cm} (5)

\[ \varphi = \begin{cases} \arctan\left(\frac{Q}{I}\right), & I > 0 \\ \arctan\left(\frac{Q}{I}\right) + \pi, & I < 0 \end{cases} \]  \hspace{1cm} (6)
After Zynq SoC is started from BootROM on the chip, the user-created first-stage Boot Loader (FSBL) is executed and the user software is executed in the next Stage. The FSBL works by: initializing the PS; Configure PL according to the Bitstream file; Load bare-metal application to DDR3 from SD card; Start executing the bare-metal application. The flow chart of ARM software of the detection system is shown in Figure 6.

![Software flowchart of ARM](image)

### Figure 6. Software flowchart of ARM.

5. The experimental results

In this paper, two aluminum alloy 7075 test blocks of the same specification are used as experimental materials to detect the stress in different depths of the material. One of them is strengthened by laser impact, and residual stress will exist in the surface layer, while the other one is not strengthened by laser impact. The induced eddy current in the conductive material has skin effect [8], and the skin depth is determined by the excitation signal frequency, the permeability of the measured material, and the conductivity of the measured material. The specific relationship is as follows:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$  \hspace{1cm} (7)

The change of material conductivity and permeability caused by residual stress is relatively small, so the skin depth of induced eddy current is mainly related to the frequency of excitation signal. The higher the frequency of the excitation signal, the smaller the skin of the induced vortex and the eddy current detection range. In the experiment, the excitation current was set at 110mA and the excitation frequency was set at 400kN^2Hz, (N= 10, 8,...2), so the eddy current skin depth approximate uniform decline. The characteristic values of magnetic sensor under excitation of different frequencies are calculated respectively. The amplitude and phase of the output signal corresponding to the strengthened test block and without strengthened block are respectively denoted as V<sub>1</sub> and φ<sub>1</sub>, V<sub>2</sub> and φ<sub>2</sub>, so ΔV=V<sub>2</sub>-V<sub>1</sub>, Δφ=φ<sub>2</sub>-φ<sub>1</sub>. The test results are shown in the table:
Table 1. The amplitude and phase of the output signal under different excitation frequencies.

| Frequency | V₁ (mV) | V₂ (mV) | ΔV (mV) | φ₁ | φ₂ | Δφ |
|-----------|---------|---------|---------|-----|-----|-----|
| 4000      | 5.632   | 5.648   | 0.016   | 3.921 | 1.78 | 2.141 |
| 6250      | 7.322   | 7.343   | 0.021   | 4.187 | 1.931 | 2.256 |
| 11111     | 10.159  | 10.189  | 0.030   | 4.657 | 2.267 | 2.39  |
| 25000     | 15.821  | 15.879  | 0.058   | 5.262 | 2.68 | 2.582 |
| 100000    | 32.33   | 32.48   | 0.15    | 6.084 | 3.234 | 2.85  |

It can be seen that under a given excitation frequency, the amplitude and phase of the output signal of the sensor are smaller than those without residual stress when there is residual stress inside the conductive material, and the skin depth decreases when the excitation frequency increases. In both cases, the extracted signal features will increase significantly, while the difference between amplitudes and the difference between phases will also increase. At the same time, the system has high measurement accuracy, the signal source output frequency error is 0.1%, the signal acquisition amplitude error is 0.13%, and the detection depth is up to 2.2mm. The measured results are in agreement with the actual situation, and the stability and effectiveness of the system are verified.

6. Conclusion
This paper presents a weak magnetic signal detection system based on FPGA and ARM structure for detecting residual stress. FPGA is responsible for providing signal source excitation and controlling data acquisition system, while ARM is responsible for signal feature extraction and communication with upper computer. The detection system is small in size, high in accuracy and good in consistency, and the detection depth can reach 2.2mm. The transmission speed of AXI bus and the computing speed of ARM processor ensure the real-time and stability of the system, which greatly reduces the detection speed and has a good application prospect.

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