Open-Source Memory Compiler for Automatic RRAM Generation and Verification

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Abstract—The lack of open-source memory compilers in academia typically causes significant delays in research and design implementations. This paper presents an open-source memory compiler that is directly integrated within the Cadence Virtuoso environment using physical verification tools provided by Mentor Graphics (Calibre). It facilitates the entire memory generation process from netlist generation to layout implementation, and physical implementation verification. To the best of our knowledge, this is the first open-source memory compiler that has been developed specifically to automate Resistive Random Access Memory (RRAM) generation. RRAM holds the promise of achieving high speed, high density and non-volatility. A novel RRAM architecture, additionally is proposed, and a number of generated RRAM arrays are evaluated to identify their worst case control line parasitics and worst case settling time across the memristors of their cells. The total capacitance of lines SEL, N and P is 5.83 fF/cell, 3.31 fF/cell and 2.48 fF/cell respectively, while the total calculated resistance for SEL is 1.28 Ω/cell and 0.14 Ω/cell for both N and P lines.

I. INTRODUCTION

Random Access Memories (RAMs) and processing units are critical components of a digital system. Commonly known volatile memories are Static Random Access Memories (SRAMs) and Dynamic Random Access Memories (DRAMs) [1], [2]. SRAMs are of particular interest since they can be used in System-On-Chip (SoC), Application Specific Integrated Circuit (ASIC) and microprocessor designs [3], [4].

Memory design is however a tedious task for an Integrated Circuit (IC) design engineer, and requires plethora of time and multiple design cycles [3], [4]. Additionally, commercial Process Design Kits (PDKs) that are available to academia or small and medium size enterprises (SMEs), do not provide memory compilers. Access to memory IP is typically licensed through third party vendors, often providing just limited flexibility and reconfigurability [3]. Modern applications require customised memories (such as single port, dual port, multi port) [5]. Depending on the desired performance, different fabrication technology may be required [3], therefore, memory compilers should be able to create scalable and customisable memories [3], [4]. Driven by the above mentioned needs, various attempts have been made to create memory compilers [3]–[6].

Conventionally, memory compilers mainly deal with SRAMs or other volatile memories [3]–[8]. These memories can have advantages such as high packing density and high read/write speed. Nevertheless, the volatility of the states of their cells produces the necessity of constantly refreshing their

![Diagram of RRAM Architecture](image-url)

Fig. 1. Architecture of proposed RRAM: Top Right - RRAM array. The size of the array is \( M = 2^Y \) rows and \( N = 2^X \) columns. The blue coloured cells represent a word of \( b \) bits. Left - A \( Y \) bits to \( 2^Y \) bits Decoder to choose the address (enable horizontal SEL line) of the desired word. Bottom - two \( 2^X \) to \( b \) De/Multiplexers (enable vertical P, N lines) to provide the necessary connections based on the read/write operation. These are connected to the Sense Amplifier Array and the Write Circuits Array shown in orange and purple colour respectively.

cell values (DRAMs) or restoring them on power-up (SRAMs). As a result the energy consumption is high [1], [9]. On the other hand, commercially available non-volatile memories (flash memories, suffer of low speed, high write voltage and low endurance [1]. Both volatile and non-volatile memories face the problem of the memory wall, as the write/read speed of memories does not scale at the same rate as the operation frequency of processing units does [2], [10], [11].

It is clear that novel material memories exploiting new memory architectures are necessary to achieve non-volatility, scalability, high speed, high density and low power performance [1], [2], [11]–[13]. These devices can be characterised as emerging Non-Volatile Memory (NVM) technologies [1], [12]. Such a device is the memristor [9], [13], [14]. A promising type of memory using memristors and addressing the above mentioned problems is the Resistive RAM (RRAM) [2], [9], [15].

Even though, a RRAM compiler has been presented before [15], the authors of this paper acknowledge the need of an open-source RRAM compiler for academia and industry. The compiler should be able to generate a RRAM and its peripheral circuits. Additionally, the compiler should provide automatic
layout verification and memory characterisation. The proposed tool should be independent of fabrication technology and should provide reconfigurability options on the architectures and the circuits of the memory. Such a tool is essential in order to investigate novel properties and capabilities of RRAMs. This is developed as part of the Functional Oxide Reconfigurable Technologies (FORTE) programme. FORTE's aims are threefold: develop and optimise the manufacturing processes of RRAM devices; create the technology tools and design rules required for integration with CMOS; and showcase potential applications of CMOS/Memristor integrated circuits.

This paper presents an early version of the first open-source RRAM compiler which automatically creates and verifies the schematic and the layout of a $M \times N$ dimensions RRAM. Additionally, it extracts parasitics and generates a post layout view. Suitable files with parasitic information are generated which can be imported in MATLAB and further information on control lines capacitance and resistance can be obtained. The RRAM compiler has been published on Github:

https://github.com/akdimitri/RRAM_COMPILER

The proposed architecture of the RRAM of the compiler is shown on Fig. 1. The subcircuits are quite similar to an SRAM [16], however, RRAM architecture requires additional peripheral circuitry to control the RRAM cells which operate on very strict voltage conditions as explained in Section II. Section III describes the operation flow of the proposed compiler. Section IV compares the characteristics of the various RRAM macros created by the compiler. Finally, Section V discusses future improvements, challenges and concludes the results.

II. RRAM ARCHITECTURE OVERVIEW

The proposed RRAM cell consists of a memristor and an NMOS transistor as shown in Fig. 3. In order to write a value to the cell, the SEL line has to be set to high voltage and an appropriate voltage difference has to be applied between P and N terminals (depending on memristor characteristics). In order to read the value of the memristor, SEL line has to be set to high voltage and an extremely small voltage difference has to be applied between P and N terminals, ensuring the voltage difference is not large enough to change the resistive state of the memristor. Thus, it is made clear that suitable peripheral circuits have to be designed in order to accurately control these sensitive pins.

The RRAM cells can form a RRAM array by sharing horizontal SEL lines and vertical P and N lines as it is shown on Fig. 3. Based on this topology a $M \times N$ RRAM array can be generated. Given that a word length is $b$ bits, a $2^Y \times b2^X$ RRAM array can be generated, where $M = 2^Y$ and $N = b2^X$ with resemblance to the arrays of Figs. 1 and 3.

Thus for both read and write operation, a SEL line decoder is needed to select the desired horizontal line and multiplexers to connect the P and N vertical lines of the desired word memory cells to read/write circuits. Since the array has $2^Y$ SEL lines, a word of $Y$ bits is enough to describe the address of the desired SEL line. Therefore a decoder of $Y$ to $2^Y$ is required.

Regarding P and N lines, it is essential to take under consideration the read and write operations. During the read operation, a small voltage (less than 0.5 V) has to be applied on the desired P lines. Therefore, a multiplexer $b2^X$ to $b$ is necessary to connect the selected memory word to read circuits. A word of $X$ bits is enough to control the multiplexer. Since the voltage difference has to be extremely small, the N pins can be connected to ground (See Fig. 1 ground on N Multiplexer). Therefore, a signal can be used (not shown on figure) during read operation to ground all N pins. On the other hand, during write operation a larger voltage value has to be applied across P and N pins, thus in this case both desired P and N lines will be connected to write circuits using $b2^X$ to $b$ multiplexers. A simplified diagram of Read and Write Operations is shown on Fig. 2. In Fig. 1 N multiplexer is connected with pink line with the write circuits as it is needed only for write operation. On the other hand, P multiplexer is connected on both read and write circuits, thus a black line is used on the figure. The write circuits are shown on Fig. 1 with WR blocks.

As far as the read operation is concerned, a novel sense am-
The proposed compiler was created using SKILL language which can be used to customise and extend Cadence Design Environment (IC6.1.8) [19], [20]. In this case, multiple SKILL scripts and functions have been created and integrated in a main function SKILL script which performs the automatic memory generation and layout verification. Both the main function and subfunctions are generic functions, highly customisable and reconfigurable.

The arguments of the compiler are the $M \times N$ dimensions and the name of the library where the generated RRAM should be saved. Additionally, the database representation [19] of the RRAM cell and the Calibre cell-map file can be provided as arguments or they can be directly hard-coded.

A simplified compilation flow is shown on Fig. 5. Initially the compiler creates the schematic, the layout and the symbol of a row of RRAM Cells of size $1 \times N$. Based on the row cellview, the RRAM macro is generated.

Subsequently, the compiler creates three folders inside the cellview folder for DRC, LVS and PEX respectively. The necessary files (runset files, Spice netlist, GDS) are generated by the compiler in order to invoke Calibre DRC, LVS and PEX in batch mode through the Command Interpreter Window (CIW) of Virtuoso [21], [22]. After these operations are finished, the compiler invokes Calibre View Setup in batch mode and creates a Calibre post-layout view of the RRAM.

The parasitics output files of the compiler are located inside the cellview folders.

The layout (metals and poly layers) of a generated $128 \times 128$ RRAM array is presented on Fig. 4. The layout size is $294.42 \mu m \times 642.41 \mu m$.

Using the compiler, a number of $N \times N$ square RRAM arrays were created. By importing the output files of the compiler in MATLAB, the worst case Capacitances and Cross Capacitances ($C + CC$) were extracted. The results are shown on Fig. 6a. Fig. 6a shows that $C + CC$ rises linearly with respect to the number of cells of a line. The SEL lines have greater capacitance. The memory cell has greater horizontal length compared to its vertical width with resemblance to the cellview folder of Fig. 4. Lines N and P are shared vertically and occupy less area, thus they suffer of less capacitance.

It is worth mentioning that the SEL line capacitance does not include the additional capacitance of the gates of the transistor switches and also that the additional capacitance due to the connections of the cell to the memristor has not been taken into account.
Additionally, the worst case scenario settling time of voltage across the memristor on the post layout views of RRAM cells was investigated. This case was found for \( VDD \) on N pin and \( VSS \) on P pin. As it is expected, the worst case was found for the maximum high resistive state where \( R=5 \, \text{M} \Omega \). Based on these conditions a testbench was set in Virtuoso and a corner analysis was conducted for a number of RRAM arrays. The settling time range was set equal to 1% of the final value. Slowest settling time was achieved for Slow NMOS, Slow PMOS (SS) model library. Results are shown on Fig. 6c. For small array row/column size the settling time is almost stable around 550 ps, however as the size grows the settling time rises exponentially. This is because both the resistance and the capacitance of the lines increase and therefore the loading time of the line increases.

Based on the SPICE model of the technology library for layout layers, the resistance of lines SEL, N and P were calculated. N and P lines have the same layout shape, thus it was found that they have the same resistance. The results are shown on Fig. 6b. The resistance also rises linearly with respect to the number of cells of the line.

The RRAM cell used for the results produces arrays of density equal to 0.082 Mb/mm\(^2\) for a 180 nm technology. The RRAM cells have approximately the same size with SRAM implementations at 180 nm technology. Assuming linear scaling, the RRAM cells follow the scaling trend of SRAM implementations shown in the below table.

| Table I: Memories density comparison. |
|--------------------------------------|
| Ref. | Feature Size | Technology | Mb/mm\(^2\) |
|------|-------------|------------|-------------|
| [23] | 40 nm | CMOS | 0.94 |
| [24] | 45 nm | CMOS | 0.33 |
| [3]  | 45 nm | FreePDK45 | 0.826 |
| [25] | 65 nm | CMOS | 0.77 |
| RRAM Compiler | 180 nm | CMOS | 0.082 |
| [26] | 180 nm | CMOS | 0.067 |
| [3]  | 0.5 \( \mu \)m | SCMOS | 0.005 |

\(^1\) Memory cell array density. \(^2\) Memory cell size.

V. CONCLUSION

To the best of our knowledge, this paper has reported the first open-source memory compiler specifically for RRAM with supporting RRAM architecture. An early version of the compiler has been designed and already been made publically available. Even though, the compiler is a preliminary version, it is able to generate large sized arrays and verify their layout. The authors of this document are currently investigating novel suitable circuits to sense the stored value of a memory cell without altering its resistive state. Next steps include the research and integration in the compiler of write circuits, decoders and multiplexers.

Besides providing a powerful tool to academia and industry for boosting memory design time, the authors believe that the compiler will facilitate the research of NVMs and RRAMs and their operation.

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