An energy- and area-efficient limiting amplifier with interleaving feedback for 25 Gb/s optical receiver

Sheng Xie¹, Daiquan Shi¹, Gaolei Zhou², and Luhong Mao², a)

Abstract A 25 Gb/s energy efficient limiting amplifier (LA) with active feedback is presented. To obtain high energy efficiency, the inverter-based amplifier is employed, and the use of interleaving feedback in the four stages enhances the bandwidth of LA core while maintaining a flat frequency response within the –3 dB bandwidth. Fabricated in SMIC 55 nm CMOS technology, the measurement results demonstrate that the proposed LA achieves a bandwidth of 18.5 GHz with a gain of 36.8 dB, and consumes only 17.3 mW at 1.5 V supply voltage, corresponding to an energy efficiency of 0.69 pJ/bit at 25 Gb/s operation. Due to the absence of passive inductors and capacitors as well as compact structure, the LA core area is only 0.0008 mm².

Keywords: limiting amplifier, inverter-based amplifier, interleaving feedback, energy efficient, low area

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the rapid development of mobile terminal, intelligent sensor, and cloud computing, the global data volume grows explosively in the past two decades. To deliver the vast amount of data, higher data rates are urgently required from Internet, super-computing, and data centers [1]. Since conventional copper-based electrical interconnection is seriously constrained beyond 10 Gb/s due to skin effect, fiber-optic scheme becomes the best current solution to handle huge traffic streams with features of broad bandwidth, low crosstalk, and high energy efficiency, etc [2, 3]. Thus, new technologies are required for 100 Gb/s and beyond [4, 5].

As a key building block of optical receiver, the limiting amplifier (LA) with high gain and wide bandwidth is indispensable to enlarge the relatively small output from the transimpedance amplifier (TIA) to a constant logic level. For high-speed optical communications beyond 25 Gb/s, the design challenge of LA is to lower the power consumption and area while sustaining high gain and large bandwidth simultaneously.

For the design of high-speed LA, SiGe BiCMOS technology is favored because of the large bandwidth and low noise characteristics of HBTs, but it normally consumes more power due to its high supply voltage [10, 11, 12]. Although deep-submicron CMOS technology manifests competitive advantage in energy efficiency, many bandwidth expansion techniques are necessary to support higher transmission rates when the gain bandwidth product (GBP) is limited by the relatively lower transition frequency (fT) of MOSFETs. In general, inductive peaking technique [13, 14, 15] is widely employed to broaden the bandwidth, however, on-chip inductors occupy a large chip area, thus increasing the cost of chip implementation. As a result, various inductor-less bandwidth expansion techniques have been explored. Capacitive peaking, such as capacitance degeneration [16, 17] and negative capacitance compensation [18, 19], is a commonly used approach to enhance the bandwidth. However, the high-pass characteristic of capacitive peaking technique, high-frequency noise will be introduced, which degrades the receiver’s sensitivity. Furthermore, passive capacitor also occupies relatively large chip area compared to the size of MOSFETs. Cherry-Hooper (CH) configuration [15, 17, 20] improves the bandwidth through resistance feedback, but it will consume more power than that of inductive or capacitive peaking, and the bandwidth will be deteriorated significantly when multi-stage CH is cascaded to provide appropriate gain. Recently, active feedback technique [18, 21, 22, 23, 24] is proposed for its remarkable bandwidth expansion effect. However, large fluctuation of the frequency response may be occurs, and there is large headroom to optimize the energy efficiency. To cope with these challenges, design of broadband LA with high energy efficiency and low area is urgently required.

In this letter, a 25 Gb/s high energy efficiency LA with interleaving feedback fabricated in 55 nm CMOS technology is presented. An inverter-based topology [25, 26, 27] is adopted as gain cell to reduce the power consumption, and a four-order interleaving feedback is introduced to expand the bandwidth and improve the flatness of frequency response. The absence of on-chip inductors and capacitors, a significant area reduction is achieved. The proposed broadband LA consumes only 17.3 mW at a single 1.5 V supply, corresponding to an energy efficiency of 0.69 pJ/bit.

¹ Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, School of Microelectronics, Tianjin University, Tianjin 300072, China
² School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China

a) lhmao@tju.edu.cn

DOI: 10.1587/elex.18.20210112
Received March 8, 2021
Accepted March 19, 2021
Publicized March 29, 2021
Copyedited April 25, 2021

Copyright © 2021 The Institute of Electronics, Information and Communication Engineers
at 25 Gb/s operation, and its core area is only 0.0008 mm².

2. Circuit design

The block diagram of proposed LA is shown in Fig. 1. The overall circuit is composed of input buffer, LA core and output buffer, where the input and output buffers are added with the aim of impedance matching. The number of LA stages is set to four in consideration of the trade-off among gain, bandwidth, and power. A fourth-order interleaving feedback is introduced to alleviate the bandwidth deterioration caused by coincident poles.

2.1 Inverter-based gain cell

Due to the drain current sharing and equivalent transconductance promotion of CMOS inverter, the inverter-based configuration has the advantages of large bandwidth and low power at the same gain [25, 26, 27] compared to other circuit topologies. Based on these features, an inverter-based gain cell composed of transconductance and transimpedance amplifiers is constructed, as shown in Fig. 2(a), in which the transconductance amplifier provides a large transconductance, the transimpedance amplifier uses resistance feedback to achieve high voltage gain and large bandwidth simultaneously. Since the PMOS and NMOS transistors are connected to the input node in parallel, the equivalent transconductance is given by $g_m = g_{mn} + g_{mp}$. Assuming the overall effect of a single inverter is represented by $M_{inv}$, and the output capacitances of each single inverter are $C_X$ and $C_Y$, respectively. Then the equivalent circuit of the inverter-based gain cell can be illustrated as Fig. 2(b). Where $G_1(s)$ and $G_2(s)$ denote the transfer functions of the transconductance and transimpedance amplifiers, respectively.

Based on the small-signal analysis, the transfer functions can be derived as

$$G_1(s) = \frac{V_X}{V_{in}} = \frac{-g_m(1 + sC_YR_f)}{g_{n2} + sC_X + sC_Y + s^2C_XC_YR_f}$$  \hspace{1cm} (1)

$$G_2(s) = \frac{V_Y}{V_X} = \frac{1 - g_{m2}R_f}{1 + sC_YR_f}$$  \hspace{1cm} (2)

![Fig. 1 Block diagram of proposed LA](image)

![Fig. 2 Schematic diagram of (a) inverter-based gain cell and (b) its equivalent circuit](image)

$$H(s) = G_1(s) \cdot G_2(s) = \frac{g_m g_{n2}R_f - g_m}{g_{n2} + sC_X + sC_Y + s^2C_XC_YR_f}$$  \hspace{1cm} (3)

Therefore, the low-frequency gain is given by

$$H(0) = \frac{g_m g_{n2}R_f - g_m}{g_{n2}}$$  \hspace{1cm} (4)

And the low-frequency pole can be calculated by

$$\omega_c = \frac{C_X + C_Y - \sqrt{(C_X + C_Y)^2 - 4g_{m2}C_XC_YR_f}}{2C_XC_YR_f}$$  \hspace{1cm} (5)

As shown in (4) and (5), large feedback resistance and high transconductance are desired to achieve a high low-frequency gain. Unfortunately, large $R_f$ will pull down the low-frequency pole, and high transconductance realized by large $W/L$ also increases the node capacitances, $C_X$ and $C_Y$, which causes severe bandwidth deterioration. Moreover, large size transistors increase bias current, thus consuming more power. Comprehensive considering the trade-off among bandwidth, gain and power, an optimal $R_f$ of 515 Ω is selected, and the $(W/L)_1$ and $(W/L)_2$ are carefully designed to 15 μm/60 nm and 20 μm/60 nm, respectively. The gate length of transistors is fixed at 60 nm feature size to guarantee the optimal performance. In addition, to maintain high driving capacity of CMOS inverter and achieve high energy efficiency, a supply voltage of 1.5 V is chosen. In such a case, the bias current of a single gain cell is 2.8 mA, corresponding to a power dissipation of 4.2 mW. As a result of this design, the optimal gain cell achieves 10.7 dB of gain and 20.8 GHz of bandwidth.

To verify the broadband and low-power capabilities of the inverter-based topology, Table I summaries the simulated performance of inverter-based topology, and compares it to other LA topologies. To compare the comprehensive performance, a figure of merit (FoM), GBW per unit power, is defined as

$$FoM = \frac{GBW \text{ (GHz)}}{power \text{ (mW)}}$$  \hspace{1cm} (6)

As shown in this table, the FoM of inverter-based topology is the highest.

| Topology | Common-source | Cherry-Hooper | Inverter-based |
|----------|---------------|---------------|---------------|
| Gain (dB) | 10.2 | 10.1 | 10.7 |
| Bandwidth (GHz) | 14.5 | 20.7 | 20.8 |
| Supply voltage (V) | 1.4 | 1.5 | 1.5 |
| Power (mW) | 5.3 | 12.6 | 4.2 |
| FoM (GHz/mW) | 8.85 | 5.26 | 16.98 |

2.2 LA with interleaving feedback

As is well known, the overlapped poles will cause severe bandwidth deterioration when the similar gain cell are cascaded. To expand the LA bandwidth to support higher data transmission, active feedback technique, as an effective solution to improve the gain-bandwidth product, is commonly
Similarly, the transfer function of feedback stage $G$ can be expressed by

$$H(s) = \frac{H^2(s)}{1 + 7H(s)G_f(s) + 10H^2(s)G_f^2(s) + H^3(s)G_f^2(s)}$$

$$= \frac{H^2(s)}{1 + 9.21H(s)G_f(s) + 0.25H^2(s)G_f(s)}$$

$$= \frac{H^2(s)}{1 + 0.18H(s)G_f(s)}$$

$$= H_A(s) \cdot H_B(s) \cdot H_C(s)$$

As shown above, the LA with FIFB designed in this work can be equivalent to a LA with three-stage non-interleaving feedback. And the corresponding transfer functions of this equivalent LA can be expressed as $H_{FIFB}(s) = H_A(s) \cdot H_B(s) \cdot H_C(s)$. As a result, the signal flow shown in Fig. 3 can be simplified as shown in Fig. 4.

In the following, a cascaded two-stage gain cell with transconductance feedback shown in Fig. 5 will be analyzed in detail. In practice, the size of $M_f$ is much smaller than that of transistors in inverter-based amplifier, so $C_X$ and $C_Y$ can be regarded as the same as that without feedback. Therefore, the analysis of $G_1(s)$ and $G_2(s)$ in section 2.1 are still valid. Similarly, the transfer function of feedback stage $G_f(s)$, can be expressed by

$$G_f(s) = \frac{g_{mf}(1 + sC_Y R_f)}{g_{m2} + sC_X + sC_Y + s^2 C_X C_Y R_f}$$

Then the transfer functions of cascaded two-stage gain cell without/with feedback can be derived as

$$H_1(s) = H^2(s)$$

$$= \left(\frac{g_{m1}g_{m2}R_f - g_{m1}}{g_{m2} + sC_X + sC_Y + s^2 C_X C_Y R_f}\right)^2$$

$$H_2(s) = \frac{H^2(s)}{1 + H(s)G_f(s)}$$

$$= \frac{(g_{m1}g_{m2}R_f - g_{m1})^2}{(g_{m2} + sC_X + sC_Y + s^2 C_X C_Y R_f)^2 + A}$$

Here, $A = (g_{m1}g_{m2}R_f - g_{m1})g_{mf}(1 + sC_Y R_f)$. It is noted that an additional term $A$ is introduced in the denominator of (10) due to the feedback effect, which splits the overlapped poles caused by direct cascading, thus improving the bandwidth.

By observing the expressions of transfer function in (7), (8) and (9), we found that $H_A(s)$, $H_B(s)$ and $H_C(s)$ have similar pole response effect as that of $H_2(s)$, but the unlikely feedback coefficients make their pole responses different. Consequently, this equivalent LA with three-stage non-interleaving feedback alleviates the rapid bandwidth fall due to the poles overlapping.

In order to obtain the optimal frequency response of the LA, an appropriate coefficient of $G_f(s)$ needs to be selected. To this purpose, the frequency responses under different feedback coefficients are analyzed. Since $g_{mf}$ is correlated with the width of feedback transistor $W_f$, the variation of $G_f(s)$ can be represented by $W_f$.

Fig. 6 shows the variation of gain, bandwidth and corresponding gain peaking with $W_f$ for the LA. The gain decreases linearly in the whole range, while the bandwidth expands significantly before 3 μm and then gradually reaches the maximum. In addition, the gain peaking rapidly grows initially, and approaches a peak at 5 μm. In order to obtain an approximate 20 GHz bandwidth with a high gain and better flatness simultaneously, an optimal $W_f$ of 1.25 μm is selected finally.

Note that the non-interleaving feedback configuration in Fig. 4 is only to facilitate the analysis, the actual circuit could not be constructed with this feedback since the required widths of feedback transistors are less than 1 μm for our designed performance, which is not allowed in SMIC 55 nm process.

The frequency responses of the equivalent three stages, and the cascaded LA with/without FIFB is illustrated in

---

**Fig. 3** Signal flow of LA with fourth-order interleaving feedback

**Fig. 4** Signal flow of equivalent cascaded LA with three-stage non-interleaving feedback

**Fig. 5** Cascaded two-stage gain cell with transconductance feedback
Fig. 6 (a) Variation of the gain and bandwidth with $W_f$ for the LA. (b) Associated gain peaking

Fig. 7 Frequency responses of the equivalent independent three stages, and the cascaded LA with/without FIFB

Fig. 8 Chip microphotograph

Fig. 9 Simulated and measured S-parameters

3. Experimental results

With the design of transimpedance input buffer and active inductor-based output buffer [28, 29], the proposed LA has been fabricated in SMIC 55 nm CMOS process. The chip microphotograph is shown in Fig. 8. The total chip area including PAD, electro-static discharge (ESD), dummy capacitor and seal-ring is about 0.3068 mm$^2$, and the core area of overall circuit is only 0.0014 mm$^2$, of which LA core occupies 0.0008 mm$^2$.

The prototype chip was measured by on-wafer probing for frequency response and transient measurements. The electronic S-parameters are measured by utilizing an Keysight N5247B vector network analyzer. Fig. 9 demonstrates the measured response of the overall circuit with the simulated results for comparison. The measured $S_{21}$ has good flatness and agrees well with the simulation result, but the simulated one has a steeper slope at high frequencies. The measured $S_{11}$ is better than $-8$ dB, and the measured $S_{22}$ is better than $-23$ dB over the $-3$ dB bandwidth.

The transimpedance gain of the overall circuit can be derived from measured S-parameters as [30]

$$Z_T = \frac{S_{21}}{S_{11} - 1} Z_0$$

Where $Z_0$ is 50 $\Omega$. As shown in the Fig. 10, the measured $Z_T$ achieves a bandwidth of 15.5 GHz and a transimpedance gain of 52.6 dB$\Omega$, which matches well with the simulated one.

To guarantee good performance for the overall circuit, the bandwidths of the input and output buffers are considered preferentially, thus making the relative low gains (13.2 dB/16.2 GHz for input buffer and 2.6 dB/16.4 GHz for output buffer). The measured and simulated frequency response of proposed LA excluding the input and output buffers is also presented in Fig. 10. Good agreement between measurements and simulation within the $-3$ dB bandwidth is obtained. The difference at higher frequencies may be caused by the parasitic effect.

To characterize the transient response, $2^{31} - 1$ pseudo-random bit sequence (PRBS31) is generated by Anritsu MP1900A pulse pattern generator, and the chip output is fed to the wide-band oscilloscope (Keysight DCA-X 86100D).
Fig. 10 Simulated and measured Zf- and frequency response of the LA

Fig. 11 Measured eye diagram at 25 Gb/s

Table II Performance comparison of reported CMOS limiting amplifier

| Parameter                  | Ref. [15],a | Ref. [23],b | Ref. [6],a | This work,a |
|----------------------------|-------------|-------------|-------------|-------------|
| Technology                 | 65 nm       | 65 nm       | 28 nm       | 55 nm       |
| Gain (dB)                  | 32.1        | 38.5        | 31°         | 36.8        |
| Peaking inductor           | yes         | no          | no          | no          |
| Bandwidth (GHz)            | 21.6        | 18          | 11.5        | 18.5        |
| Core area (mm²)            | 0.1218      | 0.11        | 0.0025      | 0.0008      |
| Power (mW)                 | 33.3        | 61          | 13.6        | 17.3        |
| Energy efficiency (pJ/bit) | 1.33        | 3.05        | 0.68        | 0.69        |

*a Measured result.
*b Simulated result.
+c Simulated result of the LA.
+d Measured result of the overall optical receiver (TIA+LA+buffer).

With a 10 mVpp input voltage, the eye diagram at 25 Gb/s operation is shown in Fig. 11. It can be seen that the opening degree is 79.0 mVpp with a SNR of 5.87 dB.

Table II summarizes the LA performance parameters designed in this letter and compares them to recently published literatures. The LA only consumes 17.3 mW due to the utilization of inverter-based topology. The LA core area is only about 0.0008 mm² due to the absence of passive inductors and capacitors. Comparing with the reported results, our proposed LA takes great advantages in area and energy efficiency.

4. Conclusion

An inverter-based LA with fourth-order interleaving feedback technique was designed and fabricated in SMIC 55 nm CMOS process. The bandwidth expands nearly 1.5 times by optimizing the feedback coefficients. The designed LA chip successfully operates at 25 Gb/s, and the results indicated that the LA has a -3 dB bandwidth of 18.5 GHz with a gain of 36.8 dB. Although a 1.5 V supply voltage is applied, the power is only 17.3 mW, corresponding to an energy efficiency of 0.69 pJ/bit. Due to the absence of passive inductors and capacitors in the circuit implementation, the LA core area is only 0.0008 mm². The LA proposed in this letter is extremely suitable for monolithic optical receiver frontend, especially for the low-cost, low-power and high-speed parallel optical receiver.

Acknowledgments

This work was partially supported by the National Natural Science Foundation of China (No. 61774113) and partially supported by the National Key Research and Development Program of China (2018YFE0202500).

References

[1] D. Liu, et al.: “What will 5G antennas and propagation be?” IEEE Trans. Antennas Propag. 65 (2017) 6205 (DOI: 10.1109/TAP.2017.2774707).
[2] R. Cartwright: “An internet of things architecture for cloud-fit professional media workflow,” SMPTE Motion Imaging Journal 127 (2018) 14 (DOI: 10.5594/JMI.2018.2816879).
[3] L. Zhao, et al.: “A new multi-resource allocation mechanism: a tradeoff between fairness and efficiency in cloud computing,” China Communications 15 (2018) 57 (DOI: 10.1109/CCH.2018.8331991).
[4] T. Sakamoto, et al.: “Strongly-coupled multi-core fiber and its optical characteristics for MIMO transmission systems,” Optical Fiber Technology 35 (2016) 8 (DOI: 10.1016/j.yofte.2016.07.010).
[5] T. Rokkas, et al.: “Techno-economic evaluations of 400G optical interconnect implementations for datacenter network,” Optical Fiber Communication Conference and Exposition (OFCC) (2018) 1 (DOI: 10.1364/OFC.2018.M1A.1).
[6] L. Szilagyi, et al.: “A 0.68 pJ/bit inductor-less optical receiver for 20 Gbps with 0.0025 mm² area in 28 nm CMOS,” IEEE International System-on-Chip Conference (SOCC) (2015) 39 (DOI: 10.1109/ SOCC.2015.7406905).
[7] L. Szilagyi, et al.: “Area-efficient offset compensation and common-mode control circuit with switched-capacitor technique in an 18 Gbps optical receiver in 80 nm CMOS,” IEEE Optical Interconnects Conference (OIC) (2015) 59 (DOI: 10.1109/ OIC.2015.7156858).
[8] L. Szilagyi, et al.: “An inductor-less ultra-compact transimpedance amplifier for 30 Gbps in 28 nm CMOS with high energy-efficiency,” IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS) (2014) 960 (DOI: 10.1109/MWSCAS.2014. 6908575).
[9] X. Shen, et al.: “Medium access control protocol and resource allocation for passive optical interconnects,” IEEE J. Opt. Commun. Netw. 9 (2017) 555 (DOI: 10.1109/JOCN.2017.00055).
[10] D. Li, et al.: “A 25 Gbps low-noise optical receiver in 0.13 µm SiGe BiCMOS,” IEEE International Conference on Electronics, Circuits and Systems (ICECS) (2016) 579 (DOI: 10.1109/ICECS.2016.7841267).
[11] Z. Xuan, et al.: “A low-power hybrid-integrated 40-Gb/s optical receiver in silicon,” IEEE Trans. Microw. Theory Techn. 66 (2018) 595 (DOI: 10.1109/TMTT.2017.2712144).
[12] S. Park, et al.: “Design of a 0.13 µm SiGe limiting amplifier with
14.6 THz gain-bandwidth-product,” Advances in Radio Science 15 (2017) 115 (DOI: 10.5194/ars-15-115-2017).

[13] D. Li, et al.: “A low-noise design technique for high-speed CMOS optical receivers,” IEEE J. Solid-State Circuits 49 (2014) 1447 (DOI: 10.1109/JSSC.2014.2322868).

[14] P.-C. Chiang, et al.: “4 × 25 Gb/s transceiver with optical front-end for 100 GbE system in 65 nm CMOS technology,” IEEE J. Solid-State Circuits 50 (2015) 573 (DOI: 10.1109/JSSC.2014.2365700).

[15] Z. Hou, et al.: “A 25-Gb/s 32.1-dB CMOS limiting amplifier for integrated optical receivers,” IEEE International Conference on ASIC (2013) 4 (DOI: 10.1109/ASICON.2013.6811897).

[16] A. Sharif-Bakhtiar and A.C. Carusone: “A 20 Gb/s CMOS optical receiver with limited-bandwidth front end and local feedback IIR-DFE,” IEEE J. Solid-State Circuits 51 (2016) 2689 (DOI: 10.1109/JSSC.2016.2602224).

[17] Q. Pan, et al.: “A 30-Gb/s 1.37-pJ/b CMOS receiver for optical interconnects,” J. Lightw. Technol. 33 (2015) 786 (DOI: 10.1109/JLT.2014.2381266).

[18] S. Xie, et al.: “An inductorless CMOS limiting amplifier with stream-mode active feedback,” IEICE Electron. Express 15 (2018) 20180640 (DOI: 10.1587/elex.15.20180640).

[19] Y. Shi, et al.: “A 112Gb/s low-noise PAM-4 linear optical receiver in 28nm CMOS,” IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) (2019) 3 (DOI: 10.1109/EDSSC.2019.8753978).

[20] J. Luo, et al.: “A 64dB gain 60GHz receiver with 7.1dB noise figure for 802.11ad applications in 90nm CMOS,” IEEE International Symposium on Circuits and Systems (ISCAS) (2015) 2404 (DOI: 10.1109/ISCAS.2015.7169168).

[21] S. Ray and M.M. Hella: “A 53 dB 7-GHz inductorless transimpedance amplifier and a 1-THz+ GBP limiting amplifier in 0.13-μm CMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers 65 (2018) 2377 (DOI: 10.1109/TCSI.2017.2788799).

[22] X. Chang, et al.: “A 25-Gb/s optical receiver front-end in 65-nm CMOS,” Photonics & Electromagnetics Research Symposium - Fall (PIERS - Fall) (2019) 1656 (DOI: 10.1109/PIERS-Fall48861.2019.9021350).

[23] R. He, et al.: “A 20 Gb/s limiting amplifier in 65nm CMOS technology,” IEEE 10th International Conference on ASIC (2013) 4 (DOI: 10.1109/ASICON.2013.6811865).

[24] S. Ray and M.M. Hella: “A 10 Gb/s inductorless AGC amplifier with 40 dB linear variable gain control in 0.13 μm CMOS,” IEEE J. Solid-State Circuits 51 (2016) 440 (DOI: 10.1109/JSSC.2015.2496782).

[25] K. Park and W.-S. Oh: “A 40-Gb/s 310-fJ/b inverter-based CMOS optical receiver front-end,” IEEE Photon. Technol. Lett. 27 (2015) 1933 (DOI: 10.1109/LPT.2015.2447283).

[26] K. Zheng, et al.: “An inverter-based analog front-end for a 56-Gb/s PAM-4 wireline transceiver in 16-nm CMOS,” IEEE Solid-State Circuits Lett. 1 (2018) 252 (DOI: 10.1109/LSSC.2018.2894933).

[27] G.-Z. Qi, et al.: “A wideband multi-stage inverter-based driver amplifier for IEEE 802.22 WRAN transmitters,” Asia Symposium on Quality Electronic Design (ASQED) (2013) 9 (DOI: 10.1109/ASQED.2013.6643554).

[28] X. Chen and Y. Takahashi: “Floating active inductor based trans-impedance amplifier in 0.18 μm CMOS technology for optical applications,” Electronics 8 (2019) 1547 (DOI: 10.3390/electronics8121547).

[29] J.S. Gaggatur and D. Thulasiraman: “A power efficient active inductor-based receiver front end for 20 Gb/s high speed serial link,” AEUE - International Journal of Electronics and Communications 111 (2019) 152886 (DOI: 10.1016/j.aeue.2019.152886).

[30] A.F. Ponchet, et al.: “Design and optimization of high sensitivity transimpedance amplifiers in 130 nm CMOS and BiCMOS technologies for high speed optical receivers,” 28th Symposium on Integrated Circuits and Systems Design (SBCCI) (2015) 33 (DOI: 10.1145/2800986.2801001).