1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are widely investigated and developed for power switching and power radio-frequency (RF) applications, thanks to their potential superior performance compared with Si- and SiC-based devices. For example, in terms of the Baliga Figure Of Merit (B-FOM)—that relates the breakdown voltage, $V_{BR}$, to the specific on-resistance ($R_{ON}$) × Area via material intrinsic properties—GaN has an outstanding value of 870 compared with 340 of SiC, with Si taken as reference (i.e., equal to 1).[1] The reduction of the off-state punch-through currents to increase the high-voltage capability of AlGaN/GaN HEMTs is often achieved by introducing acceptor trap states in the buffer associated with carbon (C) dopant.[2]

Herein, we discuss the critical role of carbon doping in the electrical behavior of AlGaN/GaN high electron mobility transistors (HEMTs) on semi-insulating SiC substrates is assessed by investigating the off-state three-terminal breakdown, current collapse, and dynamic on-resistance recovery at high drain–source voltages. Extensive device simulations of typical GaN HEMT structures are conducted and compared with experimental data from published, state-of-the-art technologies to 1) explain the slope of the breakdown voltage as a function of the gate-to-drain spacing lower than GaN critical electric field as a result of the nonuniform electrical field distribution in the gate–drain access region; 2) attribute the drain current collapse to trapping in deep acceptor states in the buffer associated with carbon doping; and 3) interpret the partial dynamic on-resistance recovery after off-state stress at high drain–source voltages as a consequence of hole generation and trapping.

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Herein, we discuss the critical role of carbon doping to achieve lower drain–source leakage current and higher breakdown voltage as well as its impact on the dynamic $R_{ON}$. The analysis is conducted by means of numerical device simulations. Experimental data from state-of-art technologies reported in the open literature are adopted to calibrate device simulations and to show their suitability to explain actual device behavior. More specifically, three experimentally observed phenomena are analyzed: 1) $V_{BR}$ dependence on gate-to-drain length, $L_{CD}$, with a slope lower than GaN critical field; 2) current collapse in pulsed measurements of output characteristics; and 3) dynamic $R_{ON}$ recovery with increasing off-state stress bias. The rest of the article is organized as follows. Section 2 describes the simulated device cross section and the models used to reproduce experimental data. Section 3 shows the results of the calibration process and the comparison between simulations and experimental data on $V_{BR}$ versus $L_{CD}$ and $I_{D} – V_{DS}$ current collapse. In Section 4, we exploit the device model to interpret the results on the dynamic $R_{ON}$ recovery found in several device technologies reported in the literature.[3–6] Conclusions are drawn in Section 5.

2. Simulated Device Structure and Models

The simulated device cross section is shown schematically in Figure 1. Device dimensions resemble the ones of the fabricated device in ref. [2]. Gate–source spacing ($L_{GS}$), gate length ($L_{G}$), and gate field plate overhang ($L_{FP}$) are 1.0, 0.7, and 0.6 μm, respectively. The substrate is semi-insulating SiC, left floating during both measurements and simulations (except for the dynamic $R_{ON}$ recovery analysis, as explained in Section 4). In general, the epitaxy of GaN HEMTs is more complex than that of ref. [2], especially in technologies for power switching
Simulated AlGaN/GaN HEMT cross section to reproduce I_E–V_L curves, showing the agreement between measurements from ref. [2] (red squares) and simulations (black solid curves).

The choice of the C-doping model adopted in this work is justified by the fact that by adjusting the donor–acceptor autocompensation ratio, it is possible to accurately reproduce dynamic effects in different AlGaN/GaN power HEMTs.[9–13] Moreover, a higher donor concentration in C-doped GaN compared with the donor density measured in unintentionally doped samples was experimentally confirmed in ref. [14], and attributed to the autocompensation between C-related donors and acceptors, as assumed here. Finally, a similar C-doping model with high donor–acceptor autocompensation was found also by other authors to be instrumental to reproduce breakdown effects in C-doped AlGaN/GaN HEMTs by means of device simulations.[15]

3. Breakdown and Current Collapse

The calibration of the simulation setup against experimental results from ref. [2] is shown in Figure 2. Figure 2a shows the comparison between simulated and measured transfer characteristics of the GaN HEMTs under study. Figure 2b shows the comparison between measurements and simulations of breakdown voltage for devices with different L_CD. The breakdown condition is defined as the V_DS bias necessary to reach 1 mA mm⁻¹ of off-state I_D,[2] Detailed comparison between measured and simulated off-state I_D = V_DS curves was reported elsewhere.[16] The achieved agreement shows that the model used for the C-doping in the back-barrier is indeed effective in the prediction of the lateral breakdown limits of the fabricated devices. As shown in Figure 2b, the slope of the V_BR versus L_CD curve is lower than...
the critical field of GaN (of about 3.9 MV cm\(^{-1}\)) despite breakdown being induced, according to our simulations, by avalanche generation. This is attributed to the highly nonuniform electric field distribution in the depletion region between gate and drain,\(^{[16]}\) allowing the critical field to be reached in a localized spot at the drain end of the gate-drain access region even if the average field is still much smaller than the critical field.

One shortcoming of introducing traps in the GaN buffer is the DC-to-dynamic drain current dispersion, also referred to as current collapse, that limits the maximum achievable output power. This effect is commonly estimated through pulsed \(I_D - V_{DS}\) measurements with different baseline conditions to either induce or suppress trapping. This is shown in Figure 3, where two different baseline biases are applied during \(I_D - V_{DS}\) simulations and measurements (taken at \(V_{GS}\) of 1 and 2 V), namely, \((V_{GS,BL1}, V_{DS,BL1}) = (0, 0)\) V and \((V_{GS,BL2}, V_{DS,BL2}) = (-0.8, 30)\) V. Measurements are still taken from ref. [2]. The first baseline for gate and drain is benign with respect to charge trapping. On the contrary, the second baseline biases the device in semi-on conditions with a high drain voltage (corresponding to class-AB operating point\(^{[2]}\)), causing the acceptor states in the buffer to accumulate negative charges (by emitting holes) and giving rise to current dispersion as the device is pulsed to on-state conditions. The model adopted for the C-doping in the simulations (Figure 3a) is able to reproduce the experimental data (Figure 3b), and also the drain current dispersion due to the acceptor traps associated with C-doping.

4. Dynamic \(R_{ON}\) Recovery

In this section, we exploit the device model used in Section 3 to give an interpretation of the partial recovery of the dynamic \(R_{ON}\). This behavior was observed in several different state-of-art power GaN HEMT technologies on silicon substrates for \(V_{DS}\) stress voltage beyond some critical value in the 100–300 V range.\(^{[3–6]}\)

A similar behavior is exhibited also by devices simulated in this work. The phenomenon is illustrated by the simulation results, as shown in Figure 4a. The simulations were conducted on a structure similar to the one, as shown in Figure 1, with grounded substrate and with a gate-to-drain spacing \(L_{GD}\) of 10 \(\mu\)m. All other parameters are the same as for simulations allowing to reproduce DC, breakdown, and current collapse curves described in Sections 2 and 3. All simulations were conducted with the same off-state gate bias \(V_{GS,OFF} = 5\) V, whereas the drain stress bias was increased from 0 to 600 V, activating/deactivating impact ionization. The results shown in Figure 4a indicate that the \(R_{ON}\) recovery at high \(V_{DS,OFF}\) can be reproduced only when impact ionization is included (red squares). In fact, if impact ionization is deactivated (yellow triangles), \(R_{ON}\) saturates and does not recover.

![Figure 3](image-url). Current collapse (CC) in the a) simulated (lines) and b) measured (symbols) pulsed \(I_D - V_{DS}\) curves. Curves have been taken for above-threshold \(V_{GS}\) of 1 and 2 V. CC is evaluated as the drain current decrease \(\Delta I_D\) occurring due to stress in the condition determined by the baseline voltages \(V_{GS,BL}\) and \(V_{DS,BL}\).

![Figure 4](image-url). Dynamic \(R_{ON}\) degradation and recovery in a) simulated and b) measured devices. In part (a) simulations are conducted with (red squares) and without (yellow triangles) impact ionization, to show that only with hole generation it is possible to qualitatively reproduce the \(R_{ON}\) recovery behavior found in experimental data shown in part (b). A typical stress time of 100 s was adopted for simulations.
not invert the degradation trend at high drain stress voltages. This can also be appreciated with the aid of Figure 5a, showing the simulated $I_D - V_{DS}$ curves taken at $V_{GS} = 2$ V after the off-state stress, for low and high drain prestress voltage ($V_{DS,OFF} = 100$ and 600 V, blue and red curves, respectively), activating/deactivating impact ionization (solid and dashed curves, respectively). Indeed, Figure 5a shows that the drain current in the linear regime, where the drain access resistance has an impact, is increased after the stress at $V_{DS,OFF} = 600$ V with respect to the case at $V_{DS,OFF} = 100$ V only if impact ionization is included in the device simulation. This result is consistent with the plot in Figure 4a and with measured $I_D - V_{DS}$ taken from ref. [3] under similar conditions, as shown in Figure 5b. The degradation followed by (partial) recovery of $R_{ON}$ was observed in several different devices as documented in the literature [3–6] (Figure 4b). We interpret this recovery behavior as a result of hole trapping into C-doping-related acceptor traps in the buffer. This is, in turn, due to the generation of holes by impact ionization. This process is shown in Figure 6, showing contour plots of the net ionized acceptor trap concentration (i.e., $N_A - N_D^0$) under the same conditions, with and without impact ionization. In the case with impact ionization included, compare Figure 6a and b, it is possible to observe a decrease in the concentration of the ionized acceptors with increasing drain stress voltage due to avalanche-generated holes in the buffer and resulting hole trapping into C-related acceptor traps. Conversely, in the case without impact ionization included, compare Figure 6c and d, the ionized acceptor concentration increases (up to the effective acceptor concentration) with increasing stress, leading to the saturation of $R_{ON}$.

Other effects might arise which could explain the results discussed in this section. For example, the model in ref. [4] relies on the vertical leakage paths between 2D electron gas and the C-doped GaN layer to explain the partial recovery of $R_{ON}$. In this work, we consider a simplified scenario with no leakage paths and focus only on the role of C-doping and show that impact ionization might be at the origin of (or might contribute to) the recovery of $R_{ON}$ for high stress bias.

**Figure 5.** a) Simulated $I_D - V_{DS}$ curves taken at $V_{GS} = 2$ V for low ($V_{DS,OFF} = 100$ V, blue curves) and high ($V_{DS,OFF} = 600$ V, red curves) drain prestress in off-state ($V_{GS,OFF} = -5$ V) held for 100 s. Solid (dashed) lines are simulations with (without) impact ionization activated. The drain current recovers for high stress only if the impact ionization is active, indicating less electron charge is trapped in the gate-to-drain access region. b) Comparison with measurement data taken from ref. [3] shows a similar trend with respect to the simulation results.

**Figure 6.** Contour plots of the net ionized acceptor trap density for the cases a,b) with and c,d) without impact ionization activated after 100 s of applied off-state stress with $V_{GS,OFF} = -5$ V and a,c) $V_{DS,OFF} = 100$ V, b,d) $V_{DS,OFF} = 600$ V. The scale of the legend is chosen to emphasize the difference in the buffer of the net ionized acceptor density (the maximum value actually exceeds this range).
5. Conclusion

We conducted systematic device simulations of AlGaN/GaN HEMTs to assess the critical role of C-doping in the buffer. Through the simulation setup calibrated through comparison with measurement data, we analyzed the breakdown voltage dependence on the gate-to-drain spacing, the current collapse under pulsed operation, and the dynamic $R_{ON}$ recovery at increasing drain stress biases. We concluded that the observed breakdown voltage versus gate-to-drain spacing slope lower than the GaN critical field is due to the nonuniform electric field causing avalanche breakdown to occur in a localized spot of the drain access region. Current collapse is attributed to hole detrapping from the deep acceptor states associated with C-doping in the buffer during the off-state stress phase of pulsed measurements. Finally, it is suggested that generation of holes by impact ionization and subsequent hole trapping into the C-related acceptors can contribute to the dynamic $R_{ON}$ recovery at high drain stress voltages.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

breakdown, C-doping, current collapse, dynamic on-resistance recovery, GaN high electron mobility transistors, impact ionization

Received: September 17, 2019
Revised: November 20, 2019
Published online: December 10, 2019

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