Are Extended Defects a Show Stopper for Future III-V CMOS Technologies

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Abstract. The paper briefly reviews some of the present-day state-of-the art III-V devices processed on a Si platform reported in the literature, before addressing defect engineering aspects for III-V processing on a Si substrate from both a structural and electrical performance perspective. The identification of the extended defects will be illustrated by some case studies based on leakage current and lifetime investigations, Deep Level Transient Spectroscopy (DLTS) analysis and low frequency noise spectroscopy. Information on the basic defect parameters can be used as input for TCAD simulation of the electrical device performance, enabling a further optimization of the materials’ growth and process conditions.

1. Introduction

The developments in microelectronics to achieve increased device performance and lower power consumption without penalizing too much the overall manufacturability and yield performance are mainly driven by scaling according to Moore’s law [1]. This requires the implementation of optimized process modules, new materials and the introduction of alternative device architectures compared to the planar transistor concept.

From 90 nm technologies onwards a variety of new process/materials options are being commonly introduced, such as e.g. stress engineering approaches to boost up the drive current, high-mobility channel materials (strained Si, SiGe, Ge, strained Ge, III-V), ultra-shallow junctions, complex gate-stacks (high-κ materials, cap layers, metal barrier and gates) with EOT’s below 1 nm, tuning of the effective work functions, optimization of process sequences (e.g. gate-first versus replacement gate or gate-last), raised source/drain for resistance control, contact technology, low-κ dielectrics for multi-level metallization schemes, Cu interconnects etc. Some of these basic process blocs are discussed in [2, 3]. The main challenges are restricting the manufacturing cost associated with the increased process complexity and the control of defects in both the substrate and the different layers.

For planar devices, improved device performance can be achieved by using Fully Depleted (FD) technologies with ultra-thin body and buried oxide (UTBB SOI), which have the potential for scaling down to 14 nm technologies and beyond [4]. Extensive research and development has been focusing on
multi-gate concepts, FinFETs, gate-all-around, horizontal and vertical nanowires and tunnelFETs, which can be processed on Si or SiGe, Ge and III-V materials on a Si substrate.

Ge has a 4% lattice mismatch with Si so that Ge layers can be directly grown on a Si substrate while controlling the layer quality by the suppression or minimizing the formation of misfit and threading dislocations. It is also possible to grow Ge selectively on Si using the aspect-ratio-trapping (ART) heteroepitaxy technique, originally proposed to grow GaAs on Si [5] and based on the selective epitaxial growth on a STI (shallow-trench isolated) patterned silicon substrate. This approach will be discussed in detail in section 2 for selective III-V growth on Si substrates.

The fact that both Ge and III-V materials can be selectively grown on Si has strongly triggered the interest in heterogeneous integration of these materials. A recent review on the topic is given in ref [6]. Heterogenous integration of Ge and III-V technologies on a silicon platform enables to fabricate System-on-Chip applications.

The monolithic integration of an InGaAs FET and a GaAs/AlGaAs laser for low power and high speed opto-electronic integrated circuits (OEICs) has recently been reported, as illustrated in Figure 1 [7].

*Figure 1.* Cross-sectional schematic of an InGaAs FET and GaAs/AlGaAs laser. (a) TEM image of an InGaAs FET with raised S/D, channel, and the gate stack. (b) HRTEM image showing gate metal, HfO$_2$/Al$_2$O$_3$ high-$\kappa$, and channel (c) XTEM image of a complete laser with AlGaAs cladding layer and GaAs/AlGaAs QW on a Si substrate. (d) HRTEM of the GaAs/AlGaAs QW [7].

This paper first discusses some defect-related issues of the use of selective hetero-epitaxy for growing III-V layers on Si substrates, before studying more in detail the electrical activity of the different defects. Leakage current and lifetimes analyses on InGaAs p$n$-diodes are complemented with Deep Level Transient Spectroscopy (DLTS) studies and by low frequency noise characterization in InGaAs FinFETs, allowing to determine the trap parameters leading to a possible identification of the origin of the traps.

2. Selective hetero-epitaxial growth
The selective epitaxial process flow, based on ART in Si regions defined by shallow trench isolation (STI), is illustrated in Figure 2 for Ge epitaxial growth on Si. The quality (defect formation and morphology) of the Ge layers depends on the epitaxial growth temperature and is linked to the trench design dimensions [8]. A better Ge quality is obtained by increasing the growth temperature with 50°C (Figure 2).
Figure 2. Schematic illustration of the process flow for the fabrication of Ge on Si structures according to the aspect-ratio-trapping (ART) technique, showing facet formation (a) and extended defects (b), which are suppressed by increasing the Ge growth temperature from 450°C (b) to 500°C (c).

Crucial remains in the first place the defect control, but also other device-related issues such as the choice of the surface passivation for high-quality gate dielectrics and contact formation are important [9]. In the case of Ge, the selective epitaxial growth has been successfully applied for the fabrication of non-planar devices like for Gate-all-around structures, FinFETs and TFETs.

The epitaxial ART technique has also been applied to III-V materials on Si and has compared to MBE or MOVPE a higher throughput and a lower process complexity. Also here defect control is of key importance and as the lattice mismatch between Si and e.g. InGaAs is 8% beneficial use has been made of a Ge buffer layer. For an InGaAs process, the process flow begins with defining a template for the InP growth in STI wafers and subsequently the Si in the active regions is etched in-situ by HCl vapor and a Ge seed layer deposited on which the nominally undoped InP buffer layer is finally grown [10]. A V-shape Si recess etch is used for defect confinement [11]. Figure 3 illustrates the process flow for InGaAs/InP growth on a Ge seed layer for 100 nm and 200 nm wide trenches and shows the defect formation [12]. The threading dislocations (TDs) are trapped in the bottom of the trench. This approach enables the co-integration of Ge p-channel devices with III-V n-channel devices on a Si platform.

Figure 3. (left) Process flow for InGaAs layers using the ART technique, and (right) Bright field cross-sectional TEM (g=[004]) images of InP in 100 nm (a) and 200 nm (b) wide trenches [12]. The TDs are trapped near the bottom of the trench.

InGaAs/InP quantum well (QW) FinFETs (fin lengths and width of 50 nm and 55 nm) processed on 300 mm Si wafers, showed a subthreshold slope SS of 190 mV/dec and an extrinsic transconductance of 558 µS/µm for an EOT of 1.9 nm [13]. In the case of an InGaAs nanowire FET a peak transconductance of 2200 µS/mm at 50 nm gate length is achieved [14]. As comparison, InGasAs quantum well MOSFETs on 300 mm wafers fabricated using a blanket MOCVD approach, resulted for In0.53Ga0.47As/In0.52Al0.48As devices in an SS = 80 mV/dec, and for a channel thickness of 15 nm a record effective mobility of 2.190 cm²/Vs at room temperature [15].

The ART technique has the advantage that a hybrid structure can be fabricated (e.g. optimized p-channel devices and optimized III-V devices in combination with standard Si CMOS), enabling System-
on-Chip integration. Although hybrid integration based on layer transfer by wafer bonding has been reported in the literature [e.g. 16-18], this isn’t a viable solution for high volume manufacturing on 300 mm Si wafers. However, good quality 300 mm InGaAs-on-insulator (InGaAs-OI) substrates have been fabricated making use of direct wafer bonding and the Smart Cut™ technology, leading to a low cost process, taking into account the reclaim of the III–V on Si donor substrate [19]. The 3D monolithic integration of III-V and (Si)Ge FETs for CMOS applications has recently been reviewed in [20].

3. Electrical activity of the defects in III-V epitaxial layers

The electrical activity of the defects in hetero-epitaxially grown III-V layers has been studied by leakage current and lifetime analysis. Additional information on the defects is obtained by DLTS and low frequency noise measurements. Attention was given to n-type InGaAs, which can be used for the fabrication of both FinFETs and TFETs and used for optical interconnects. The investigated p+n-diode structures is shown in Figure 4 [21], while the studied FinFETs had a gate stack consisting of 1 nm Al2/O3/3 nm HfO2/ TiN.

![Figure 4](image)

**Figure 4.** Schematic lay-out of the p’n InGaAs diode structure and cross-section SEM image after processing.

3.1. Leakage current and lifetime analysis

The area leakage current study shown in Figure 5a illustrates that the current density increases with the dislocation density due to the fact that the dislocations reduce the generation lifetime. The forward current analysis enables to determine the recombination lifetime, while the leakage current determines the generation lifetime. Both lifetime components are represented in Figure 5b. It can noticed that there is only an impact of the dislocation density on the lifetime if the density is higher than $5 \times 10^6 \text{ cm}^{-2}$ [21].

![Figure 5](image)

**Figure 5.** (a) Current density versus bias for a set of In0.53Ga0.47As p’n-junction diodes with different TDD, (b) Generation (black square) and recombination lifetime (red dot) extracted from the diode I-V as a function of the TDD. The dashed curves serve mainly as a guide to the eye.
A similar TDD threshold behaviour has been reported for GaAs solar cells [22]. The minority carrier lifetime can be modelled by [23]

$$\tau_R^{-1} = \tau_{max}^{-1} + \pi^3 D_{min} TDD/4$$

(1)

Although the data in Figure 5b gives an exponent -0.53 ($\tau_0$) and -0.72 ($\tau_0$), much more data points are needed to determine an accurate relationship. It should be remarked that the classical Shockley-Read-Hall analysis based on a discrete energy level in the band gap cannot be used as dislocations are known to rather introduce an one-dimensional density of states resulting in a non-SRH capturing of charges in the potential barrier around the dislocation [24]. The ratio of generation/recombination lifetime can be used to determine the trap level, which in this case is around 0.4 eV.

3.2 DLTS analysis
The used analysis procedure for the p+n-diodes allows to determine the defects in the n-layer. As shown in the DLTS-spectra in Figure 6, one broad electron trap E1 and two hole traps H1 and H2 are detected. The E1 trap has an activation energy $E_C-E_T = 0.45$ eV and is linked to the dislocations. The origin of the holes traps is less clear; H1 may be associated with the dislocations while H2 could be due to surface states along the edges of the diodes. There is also a possibility that H2 is related to the used Al$_2$O$_3$ passivation [25]. More information on the identification of the traps has been obtained from an Arrhenius plot, as indicated in Figure 6.

![Trap information derived from Arrhenius plot](image)

**Figure 6.** DLTS-spectra for an InGaAs-on-GaAs p+n junction with a TDD of $10^9$ cm$^{-2}$. The used bias pulses are indicated in the figure. A pulse frequency $t_\omega=51.2$ ms and a pulse duration $t_p=1$ ms has been utilized. The information derived from an Arrhenius plot is also indicated.

3.3. Low frequency noise investigations
The GR noise power spectral density (PSD) exhibits a plateau $A_0$ at low frequency and a $1/f^2$ roll-off, corresponding to:

$$S_{Id} = \frac{A_0}{[1+(f/f_0)^2]}$$

(2)

with $f_0 = 1/2\pi\tau_0$ the characteristic frequency of the GR center and $\tau_0$ the characteristic time constant. A least-square fit to the experimental $f^nS_{Id}$ spectrum allows to determine these parameters for the independent Lorentzians.
It has been reported that if the corner frequency is independent of the gate voltage, the noise is related to a trap level in the depletion layer, while otherwise, Lorentzians corresponding with gate-oxide traps exhibit a clear gate-voltage dependence [26]. This dependence is related to the strong $V_{GS}$ dependence of the free carrier density $n$ and the Shockley-Read-Hall (SRH) expression for the capture time constant:

$$\tau_c = 1/(n \sigma_n v_{thn})$$

with $\sigma_n$ the electron capture cross section and $v_{thn}$ the thermal velocity.

The two different types of $V_{GS}$ behaviour has been observed in InGaAs FinFETs as shown in Figure 7.

![Frequency normalized spectra as a function of frequency: (a) $f_0$ stays constant with $V_{GS}$, indicative for traps located in the depletion region (b) $f_0$ increases with $V_{GS}$, indicating traps in the gate dielectric.](image)

**Figure 7.** Frequency normalized spectra as a function of frequency: (a) $f_0$ stays constant with $V_{GS}$, indicative for traps located in the depletion region (b) $f_0$ increases with $V_{GS}$, indicating traps in the gate dielectric.

In case of $V_{GS}$-independent Lorentzian noise, a study of the noise performance at different temperatures allows via an Arrhenius plot to obtain more information on the trap parameters of the defects involved. The temperature dependence is given by [27]

$$\ln(\tau_c T^2) = \frac{E_C - E_T}{kT} + \ln \left( \frac{h^3}{4k^2 \sigma_n \sqrt{6\pi} M_c m_e^{1/2} m_h^{1/2}} \right)$$

with $E_C$ is the conduction band minimum, $k$ is Boltzmann’s constant, $h$ is Planck’s constant, $M_c$ the number of equivalent maxima in the conduction band, $m_e^*$ and $m_h^*$ are the conduction effective mass for electrons and for holes, respectively. The trap activation energy can be derived from the slope of the Arrhenius plot, while the capture cross section is calculated from the intercept.

The activation energies extracted from In$_{0.3}$Ga$_{0.7}$As nFinFETs are shown in Figure 8. To identify the different defects, one can make a comparison with data reported in the literature obtained by other techniques such as e.g. DLTS. Such a comparison is given in Table I and allows to conclude that the levels around 0.33 eV can be related to oxygen. The oxygen may in-diffuse from the STI SiO$_2$ regions into the InGaAs layer during either the layer deposition or at a later stage in the processing sequence. The levels around 0.37 and 0.44 eV are most likely associated with the dislocations in the material.
Figure 8. Arrhenius plot from the Lorentzian spectra at different temperatures for L=5.03 µm In0.3Ga0.7As nFinFETs at constant drain and gate voltage, while varying the temperature between 300 and 400 K.

Table 1. Activation energy comparison between literature and this work.

| Results from literature | This work |
|-------------------------|-----------|
| 0.44 ± 0.01 eV          | Fe³⁺/Fe²⁺ acceptor level/dislocation [28] | 0.45 eV |
| 0.33 ± 0.01 eV          | O-related trap (residual defect) [29, 30] | 0.33 eV |
| 0.37 eV                 | Fe acceptor level/dislocation [31] | 0.47 eV |
| 0.38 ± 0.03 eV          | Rh-related level [32] | 0.37 eV |
| 0.40 ± 0.03 eV          | Ir-related level [32] | 0.37 eV |

The amplitude of the Lorentzian spectrum gives information on the trap concentration, according to [33]

\[ A_i = \frac{q^2N_{\text{eff}}\tau_i}{(\omega_{\text{eff}}LC_{\text{ox}}^2)} \]  

with \( N_{\text{eff}} \) an effective surface trap density, \( C_{\text{ox}} \) the oxide capacitance density and \( \tau_i \) the characteristic time constant of trap i, derived from \( f_0 \). Table II shows the effective trap densities calculated for the investigated devices, showing that the density of the deep levels varies from \( 10^{11} \) to \( 10^{12} \) per cm².

Table 2. Effective densities of deep level traps.

| Traps           | \( E_a \) (eV) | \( T \) (K) | \( N_{\text{eff}} \) (cm²) |
|-----------------|---------------|------------|-----------------|
| O-related traps | 0.33          | 300-400    | 6.36x10^{11}    |
| Dislocations    | 0.37          | 300-400    | 7.28x10^{11}    |
| Dislocations    | 0.45          | 300-400    | 5.78x10^{12}    |
4. Conclusions
The potential for hetero-epitaxy on Si substrates is very larger and may lead to the breakthrough of monolithic integration on a Si-platform. Especially for III-V integration on 300 mm wafers excellent electrical performance has been demonstrated. The main challenge remains of course the defect control in the different layers which are influencing the electrical parameters resulting in increased diode leakage current (power consumption) and carrier lifetime degradation. However, very important is the observation that there is a threshold dislocation density required before a significant impact is noticed. Although not discussed in this paper, also the defects in the gate dielectrics have to be controlled as the can lead to generation-recombination and random telegraph signal noise.

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