Development of Transmission Grating for EUV Interference Lithography of 1X nm HP

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The advanced feature size patterning process of semiconductor conductor devices was being charged with the important role with development of an information-technology oriented society. Extreme ultraviolet lithography (EUVL) is expected as a leading candidate of the next generation lithography for semiconductor electronic devices. The development of EUV resist which has high resolution, high sensitivity, low LWR, and low out gassing is a second critical issue of the EUVL. Development of the two-beam interference exposure tool using the EUV light has been upgraded for the critical dimension of 10-nm-order in EUV resist patterning process. This tool was installed at the 10.8-nm-long undulator beamline BL09B of NewSUBARU synchrotron radiation facility. Using this EUV interference lithographic method, 15 nm hp resist pattern had been replicated on a silicon wafer. The transmission grating fabrication is the most significant key technology in the EUV interference lithography. The advanced fabrication process is applied for the transmission-grating fabrication for the EUV resist patterning beyond the feature size of 15 nm, such as 12.5 and 10 nm.

Keywords: EUV lithography, interference lithography, transmission diffraction grating

1. Introduction

EUVL [1] will be used in the semiconductor electronic device high volume manufacturing for the patterning in the 16 nm feature size around 2016. The top three issues of the EUVL are the development of 1) source, 2) resist, and 3) mask. The critical issues of EUV resist are the simultaneous achievement of the high resolution, sensitivity, low LER, and low out gassing [2]. Currently, on Feb. 25, 2015, ASML press release announced that using ASML NXE3300B exposure beta tool, the EUV-light-source power increased to 90 W at the intermediate focus position, and TSMC semiconductor chip manufacturer exposed 1022 wafers in 24 hours. 10-nm-feature-size-patterning technology is required in 2020 for the high volume manufacturing listed in the international technology roadmap for semiconductor (ITRS) [3].

The resolution specification of ASML NXE3300B EUV exposure tool is 22 nm. Thus it cannot reach to the resolution of 10-nm order. To accelerate the EUV resist development of 10-nm order, it is very significant to develop the EUV interference lithographic exposure tool for the resolution achievement of 10-nm order [4]. The EUV interference lithography had been developed and replicated 15 nm line and space (L/S) resist pattern by using two window-type transmission-diffraction grating (TDG) on which has 30 nm L/S grating pattern. In addition, 28-nm-diameter-hole resist pattern had been replicated by four window-type TDG which has 40 nm L/S grating pattern [5, 6, 7]. The replicated 15 nm L/S and 28 nm hole resist patterns on a silicon wafer are shown in Fig. 1(a) and (b), respectively.

![Fig. 1 (a) 15-nm-L/S inorganic-resist pattern, and (b) 28-nm-diameter hole organic-resist pattern using EUV-IL](image)

The reduction of the vibration amplitude from a dry pump is a significant factor for the resist patterning of a small feature size in the EUV-IL exposure. The displacement of the vibration amplitude between the TDG and wafer should be reduced to approximately 1/3 of the target resolution of 10 nm in EUV-IL [8]. The vibration amplitude displacement of the frequency range
from 0 to 50 Hz has been suppressed less than 3 nm. However, with taking care of the vibration suppression, since the TDG fabrication for 10-nm-order EUV resist patterning is most significant, this paper focused on the fabrication of the TDG for the EUV resist patterning of 10-nm-order resolution achievement using EUV-IL.

2. Experiment

2.1. Interference lithography

A schematic view of the interference lithography which was installed is shown in Fig. 2. An experimental chamber was installed at 10.8-m-long undulator beamline BL09C. The 1.0 GeV electron linear accelerator of the large synchrotron radiation facility of SPring-8 is used as an injector for the New SUBARU electron beam storage ring which is a medium scale light source. The circumstance of this ring is approximately 118.9 m and the schematic view of this facility was shown in Fig. 3.

Fig.2 A schematic view of the interference lithography which was installed

In the resolution region of 10 nm and below, since the replicated pattern is easy to be affected by the flare of the imaging optics, the flare control of the optics is very significant. However, since in the case of EUV-IL, EUV-IL need not to use optics, there is no flare to be affected to the fine pattern replication. Thus EUV-IL is a powerful exposure tool to evaluate resist resolution and LWR performance for the development of EUV resist material.

2.2 Transmission-diffraction gratings

A TDG is the significant key element of EUV-IL for the advanced fine resist patterning. A schematic view of a fabrication process of a TDG is shown in Fig. 5 [10]. Diffraction efficiency strongly depends on the absorber material and its thickness. TaN material was selected to employ as an absorber grating of the TDG because of the high diffraction efficiency, the good sputtering and dry-etching performance.

First, 25 nm TDG tried to fabricate. And then 20 nm TDG process was evaluated. To achieve the advanced fine patterning for these TDGs, the following three specified process should be employed.
1) The SiO2 hard mask process should be employed for the patterning of the TaN layer with aspect ration of approximately 3.
2) The low stress sputtering of the TaN and SiO2 layers was required.
3) The center stop process was employed to cut off the incident light for the interference patterning.

The transmission fabrication flow is listed as follows.
1) The low stress 100-nm thick Si$_3$N$_4$ double coated 4-inches Si substrate was performed as the TDG substrate.
2) The TaN and SiO$_2$ layers which employed as an absorber grating and hard mask respectively were sputtered on the substrate.
3) Electron beam resist was coated.
4) The resist was patterned by 50-keV-electron-direct-writing tool.
5) The EB resist pattern was transformed to the SiO$_2$ hard mask layer by dry etching process.
6) The hard mask pattern was transformed to the TaN absorber grating by dry etching process.
7) The back side Si$_3$N$_4$ layer was dry etched.
8) The back side Si was removed by the KOH wet etching process at the temperature of 90 ºC to perform the Si$_3$N$_4$ membrane.
9) A 2 µm thick EB resist was coated to perform the center stop layer to cut off the direct incident EUV light.
10) The center stop resist on the window area was exposed by EB, and development and rinse processing were carried out.
11) The remained resist was removed by O$_2$ ashing process.

Fig. 5 Fabrication process flow of TDG

2.3 Resist processing
In this fabrication process of TDG, the electron beam lithography plays an important role to form a grating pattern with a small feature size. ZEP520A (Nihon Zeon) resist had been employed as the EB patterning of the TDG. However this resist resolution limit was 25 nm in the EB direct writing. A higher resolution EB resist is required to fabricate a TDG with 25 and 20 nm L/S. In addition, resist with higher etching tolerance is needed.

gL3002T (Gluon Lab.) resist which is a revised version of ZEP520A resist and HSQ resist (XR-1541-002, Toray Dow Corning) were tried to use in the fabrication process of the TDG. The averaged molecular weight of gL3002T resist is 10 times larger than that of ZEP520A resist and also has higher resolution and process stability comparison to the organic positive type resist.

HSQ resist is a negative type resist on the basis of the silicon containing resist and has a resolution of 6 nm. However, the sensitivity of HSQ resist is approximately 10 times lower than that of ZEP520A resist.

As results, gL3002T and HSQ resists were employed for the fabrication of the TDG with a feature size of 25 and 20 nm L/S grating pattern.

3. Results and Discussions
3.1 gL3002T resist process
The resist was spin coated on a SiO$_2$ layer to be the thickness of 50 nm. Prebake was carried out at the temperature of 180 ºC in 180 s. O-xylene and 2-propanol was employed as a developer and rinse solutions, respectively. A SEM image of the cross sectional view of the replicated gL3002T resist pattern is shown in Fig. 6. Both scanning electron microscope (SEM) images of 25 and 20 nm L/S resist patterns were replicated on a SiO$_2$ layer as shown in Fig. 6(a) and (b), respectively.

Fig. 6 SEM images of (a) 25 nm and (b) 20 nm L/S gL3002T resist pattern on SiO$_2$ layer

A fine rectangular cross sectional shape of 25 nm L/S gL3002T resist pattern was formed. However, since it couldn't be formed in the case of 20 nm L/S resist pattern, gL3002T was employed in the fabrication of TDG with a
feature size of 25 nm.

SiO₂ 25 nm L/S pattern was formed by dry etching using the 25 nm L/S gL3002T resist pattern as a mask. The cross sectional SEM image of SiO₂ 25 nm L/S pattern is shown in Fig. 7(a). For this CF₄ etching process, RF and bias power were 100 W and 25 W, respectively. And chamber vacuum pressure was 1.3 Pa, and the CF₄ gas flow rate was 60 sccm.

TaN 25 nm L/S pattern was formed by dry etching using the 25 nm L/S SiO₂ pattern as a mask. The cross sectional SEM image of TaN 25 nm L/S pattern is shown in Fig. 7(b). For this Cl₂ etching process, RF and bias power were 100 W and 25 W, respectively. And chamber vacuum pressure was 1.3 Pa, and Cl₂ gas flow rate was 25 sccm.

After the Si substrate back side etching and formulation of the center stop processes, 25 nm L/S TDG was succeed to fabricate. Using TDG, 12.5 nm L/S resist pattern will be replicate in the EUV-IL exposure.

3.2 HSQ resist process

Replicated 20 nm L/S HSQ resist pattern on a bare Si wafer using 50 keV EB direct writing tool is shown in Fig. 8(a). However, HSQ resist pattern with a waving shape was replicated because of charging up in EB lithography. Since the exposure sensitivity of HSQ resist has approximately 10 times lower than that of ZEP520 resist, large amount of negative electric charges are accumulated on the resist surface during EB exposure. It is easier to occur this charging up phenomenon using low sensitivity EB resist material. Thus Espacer (Showa Denko) was employed as a top coating material to avoid charging up phenomenon. Espacer is water soluble and has a large conductivity. Fig. 8(b) shows the CD-SEM image of 20 nm L/S HSQ resist pattern applied Espacer top-coating process before the EB exposure. As shown in this Figure, the waving shape disappeared and 20 nm L/S HSQ pattern was succeed to replicate. The top-coating condition was 2,500 rpm in 60 s using spin coater, after the HSQ resist coating on the substrate. For HSQ resist process condition, spin-coating condition was 2,500 rpm in 60 s and prebake was carried out at the temperature of 80 °C in 80 s. And the initial HSQ resist thickness was 36 nm. The 2.38% TMAH alkali aqueous solution and deionized water were employed as a developer and rinse solution.

Development and rinse conditions were at the temperature of 22 °C in the period of 30 s, and at the room temperature in the period of 30 s, respectively.

In the case of a TDG fabrication, resist pattern should be replicate SiO₂ layer for the hard mask process. Figure 9 shows cross sectional SEM image of 20 nm L/S HSQ pattern on a SiO₂ layer.

2.38% TMAH alkali aqueous solution was employed for the development. The cross sectional resist pattern shape is not a rectangular. To obtain the rectangular cross sectional shape of HSQ resist pattern, the alkaline strong NaOH aqueous solution was employed. To raise osmosis of NaOH into the HSQ resist material, NaCl was added. Finally, mixture aqueous solution of 1% NaOH and 4%
NaCl was employed as a developer. As a result, 20 nm L/S HSQ resist pattern with a rectangle-cross-sectional shape was replicated with employing the mixture developer solution of NaOH/NaCl. This cross sectional SEM image is shown in Fig. 10(a). The thickness was 36 nm.

SiO₂ 20 nm L/S pattern was formed by dry etching using the 20 nm L/S HSQ resist pattern as a mask. The cross sectional SEM image of SiO₂ 20 nm L/S pattern is shown in Fig. 10(b). Thickness was 20 nm. For this CF₄ etching process, RF power, Bias power, chamber pressure, CF₄ gas flow rate were 100 W, 25 W, 1.3 Pa, and 60 sccm, respectively.

As shown in this figure, the cross sectional shape of 20 nm SiO₂ pattern is rectangle. TaN 20 nm L/S grating pattern could be replicate employing this SiO₂ pattern as a mask in dry etching in Cl₂ gas.

4. Conclusions

25 nm L/S gL3002T resist pattern with a rectangular cross sectional shape was formed. TaN grating pattern was formed by CF₄ and Cl₂ gas dry etching. Fabrication of a TDG which has 25 nm L/S grating pattern was completed by forming the back side etching of Si substrate and the center stop process.

HSQ resist with 20 nm L/S rectangular cross sectional pattern was formed by employing mixture aqueous solution of 1 % NaOH and 4 % NaCl as a developer. 20 nm L/S of SiO₂ was formed by CF₄ gas dry etching. 20 nm L/S of a TaN grating pattern can be transform by SiO₂ 20 nm L/S pattern as a Cl₂ dry-etching mask. Using the TDG with 20 nm L/S grating pattern, EUV resist will be evaluated in EUV-IL exposure.

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