Generalized Fast Decoding of Polar Codes
Carlo Condo, Valerio Bioglio, Ingmar Land

Abstract—Research on polar codes has been constantly gaining attention over the last decade, by academia and industry alike thanks to their capacity-achieving error-correction performance and low-complexity decoding algorithms. Recently, they have been selected as one of the coding schemes in the 5th generation wireless standard (5G). Over the years various polar code decoding algorithms, like SC-list (SCL), have been proposed to improve the mediocre performance of the successive cancellation (SC) decoding algorithm for finite code lengths; however, like SC, they suffer from long decoding latency. Fast decoding of polar codes tries to overcome this problem by identifying particular subcodes in the polar code and decoding them with efficient decoders. In this work, we introduce a generalized approach to fast decoding of polar codes to further reduce SC-based decoding latency. We propose three multi-node polar code subcodes whose identification patterns include most of the existing subcodes, extending them to SCL decoding, and allow to apply fast decoding to larger subsets of bits. Without any error-correction performance degradation, the proposed technique shows up to 23.6% and 29.2% decoding latency gain with respect to fast SC and SCL decoding algorithms, respectively, and up to 63.6% and 49.8% if a performance loss is accepted, whose amount depends on code and decoding algorithm parameters, along with the desired speedup.

I. INTRODUCTION

Polar codes are a class of error-correcting codes proposed in [1]. With infinite code length, under successive-cancellation decoding (SC), they can provably achieve capacity over binary memoryless channels. However, their error-correction performance degrades at finite code lengths, while SC yields long decoding latency, due to its inherent serial nature.

SC-list (SCL) decoding was proposed in [2]; it relies on a number of parallel SC decoders, and can substantially improve the error-correction performance of SC, especially when the polar code is concatenated with a cyclic redundancy check (CRC). This comes at the cost of additional complexity and latency. SC-flip decoding [3] limits the increase in complexity by running a series of SC attempts, sacrificing decoding speed. Improved SC-based algorithms have led polar codes to be included in the 5th generation wireless systems standard (5G) as one of the coding schemes for the enhanced mobile broadband communication scenario.

Different works over the years have attempted at reducing the decoding latency of SC-based algorithms at a limited complexity cost. The techniques described in [4]–[6] rely on the recursive construction of polar codes to identify particular subcodes in their structure, and propose fast decoders for these subcodes that can be used in SC decoding. In [7]–[11], the decoding of some of these subcodes has been extended to SCL and applied to SC-flip, reducing their latency and making them more practical to implement.

In this work, we introduce a generalized approach to fast decoding of polar codes to further reduce SC-based decoding latency. We propose three multi-node polar code subcodes whose identification patterns also envelop most of the existing subcodes [4]–[6]. Moreover, we provide their extended decoding rules for both SC-based and SCL-based fast decoding: along with new subcodes, the codes identified in [6] can thus be applied to SCL decoding. The impact of the proposed approach on SC and SCL decoding latency is evaluated, showing substantial speedup with respect to existing fast decoding algorithms [5], [8]. The error-correction performance loss brought by one of the new subcodes is then studied in terms of code, subcode and decoding algorithm parameters.

The remainder of this work is organized as follows. Section II introduces polar codes, their decoding algorithms and existing fast decoding approaches. The proposed generalized fast decoding is detailed in Section III, while its speed and error-correction performance evaluation is carried out in Section IV. Conclusions are finally drawn in Section V, along with future research directions.

II. PRELIMINARIES

A. Polar Codes

Polar codes are linear block codes of length \( N = 2^n \) and rate \( R = K/N \). They can be constructed using the transformation matrix \( G^\otimes n \) as

\[
x = uG^\otimes n,
\]

that encodes vector \( u = \{u_0, u_1, \ldots, u_{N-1}\} \) into vector \( x = \{x_0, x_1, \ldots, x_{N-1}\} \). The matrix \( G^\otimes n \) is obtained as the \( n \)-th Kronecker product of the polarizing kernel \( G = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \).

The polar encoding process identifies \( K \) reliable bit-channels out of the \( N \) available ones, and assigns the \( K \) information bits to them. The remaining \( N - K \) bit-channels in \( u \) are set to a known value, and represent the frozen set \( F \). To easily distinguish between frozen and information bits, a flag \( s_i \) is assigned to each bit-channel, where

\[
s_i = \begin{cases} 0 & \text{if } u_i \in F, \\ 1 & \text{otherwise} \end{cases}
\]

B. SC-Based Decoding

The SC decoding algorithm proposed in [1] can be interpreted as a binary tree search, as portrayed in Fig. 1. Every node at stage \( t \) receives soft information in the form of logarithmic likelihood ratios (LLRs) from its parent node \( (2^{t+1} \text{-element } \alpha \text{ vector}) \), and returns the hard decision vector \( \beta \). The tree is explored depth-first, with priority being given to the left branches.
The LLR vector $\alpha^t$ sent to the left child node is computed through the $f_t$ function as
\[
\alpha^t_i = f_t(\alpha) = 2\tanh\left(\frac{\alpha_i}{2}\right) \tanh\left(\frac{\alpha_{i+2^t}}{2}\right),
\] (3)
where (3) identifies the $f_t$ function. The LLR vector $\alpha^t$ directed to the right child node is instead calculated through the $g_t$ function:
\[
\alpha^t_i = g_t(\alpha) = \alpha_{i+2^t} + (1 - 2\beta^t_i) \alpha_i.
\] (4)
Partial sums $\beta$ are computed as
\[
\beta_i = \begin{cases} 
\beta^t_i \oplus \beta^t_j & \text{if } i < 2^t, \\
\beta^t_{i-2^t} & \text{otherwise},
\end{cases}
\] (5)
where $\oplus$ is the bitwise XOR operation. At leaf nodes, $\beta_i$ is set to the estimated bit $\hat{u}_i$:
\[
\hat{u}_i = \begin{cases} 
0 & \text{if } s_i = 0 \text{ or } \alpha_i \geq 0 \\
1 & \text{if } s_i = 1 \text{ and } \alpha_i < 0
\end{cases}
\] (6)

The SC decoding process, and in particular the exploration of the tree according to its schedule, can be viewed as a sequence of $f_t$ and $g_t$ operations. For example, the exploration of the tree represented in Fig. 1 can be expressed as $\{f_2, f_1, f_0, 0, 0, 1, 0, 1, 0, 1, 1, 0\}$.

SCL decoding [2] maintains $L$ concurrent decoding candidates. At leaf nodes, $\hat{u}_i$ is estimated as both 0 and 1 when not a frozen bit, doubling the number of candidates. To limit the exponential increase in complexity, a path metric (PM) is assigned to each candidate [12]:
\[
PM_i = \begin{cases} 
PM_{i-1} + |\alpha_i|, & \text{if } \hat{u}_i \neq \text{HD}(\alpha_i), \\
PM_{i-1}, & \text{otherwise},
\end{cases}
\] (7)
where PM is initialized as 0 and
\[
\text{HD}(\alpha_i) = \begin{cases} 
0 & \text{if } \alpha_i \geq 0, \\
1 & \text{otherwise}.
\end{cases}
\] (8)

The $L$ candidates with the lowest PM are allowed to survive. SCL error-correction performance can be further improved by concatenating the polar code with a CRC, that help in the selection of the final candidate.

### C. Fast SC-Based Decoding

To increase the speed of SC-based decoding, in [4]–[6], particular sequences of frozen and information bits have been identified, and efficient fast decoders have been proposed. The decoding of the subcodes identified by these patterns, called special nodes, avoids the complete exploration of the SC-tree, allowing substantial speed increment.

Fast simplified SC decoding (Fast-SSC, [5]) considers four special nodes, whose structures are summarized as follows:

- **Rate-0 Node**: all bits are frozen, $s = \{0, 0, \ldots, 0\}$.
- **Rate-1 Node**: all bits are information bits, $s = \{1, 1, \ldots, 1\}$.
- **Repetition (Rep) Node**: all bits are frozen except the last one, $s = \{0, \ldots, 0, 0, 1\}$.
- **Single parity-check (SPC) Node**: all bits are information bits except the first, $s = \{0, 1, 1, \ldots, 1\}$.

Additional special nodes and their efficient SC decoders have been observed in [6]:

- **Type-I Node**: all bits are frozen except the last two, $s = \{0, \ldots, 0, 1, 1\}$.
- **Type-II Node**: all frozen bits except the last three, $s = \{0, \ldots, 0, 1, 1, 1\}$.
- **Type-III Node**: all information bits except the first two, $s = \{0, 0, 1, \ldots, 1\}$.
- **Type-IV Node**: all information bits except the first three, $s = \{0, 0, 0, 1, \ldots, 1\}$.
- **Type-V Node**: all frozen bits except the last three and the fifth-to-last, $s = \{0, \ldots, 0, 1, 0, 1, 1, 1\}$.

### III. Generalized Fast Decoding

The nodes described in Section II-C identify patterns in the frozen and information bits. While in [5], along with Rate-0, Rate-1, Rep and SPC nodes, some node mergers have been identified, literature and decoding methods have mostly focused on single node types. However, the identification of multi-node patterns leads to a generalized approach to fast decoding of polar codes. In this section, we describe three multi-node frozen and information bit patterns that can be exploited to increase the decoding speed at low complexity. They envelop Rep and SPC nodes, together with Type-I to V nodes, and extend their properties to a wider set of patterns. Moreover, general identification and decoding rules for both SC and SCL fast decoding are provided.

#### A. Generalized Repetition Node

Repetition nodes are so named due to the pattern identified in the calculation of $\beta$ (5). In fact, vector $\beta$ of a Rep node can be computed by performing a hard decision on the sum of the LLRs present in vector $\alpha$ and replicating this result. However, this repetition pattern can be applied to a more general class of nodes. We call generalized Rep node (G-Rep) any node at stage $t$ for which all its descendants are Rate-0 nodes, except the rightmost one at a certain stage $p < t$, that is a generic node of rate $C$ (Rate-C). The structure of a G-Rep node is depicted in Fig. 2. A G-Rep node can be decoded under SC
using only the partial sum vector $\beta'$ of its Rate-C descendant and repeating it $2^{t-p}$ times.

**Lemma 1.** The partial sum vector of a G-Rep node is given by $\beta = \{\beta',\ldots,\beta'\}$, where $\beta'$ is calculated on the basis of the LLRs vector $\alpha'$ defined as $\alpha'_i = \sum_{j=0}^{2^{t-p}-1} \alpha_{i+j2^{t-p}}$.

**Proof.** If we call $P$ the list of operations needed to decode the Rate-C node, the list of operations needed to decode the G-Rep node is given by $(g_t, g_{t-1}, \ldots, g_{p+1}, P)$. By induction, the LLR vector $\alpha'$ of the Rate-C node is calculated as $\alpha'_i = \sum_{j=0}^{2^{t-p}-1} \alpha_{i+j2^{t-p}}$ since all the left nodes are Rate-0 and hence $\beta'_i = 0$ in (4). This vector is then used to decode the node performing the operations in $P$, that return the vector $\beta'$. The partial sum vector $\beta$ at stage $p$ is then calculated recursively using (5) with $\beta'_i = 0$ by construction, obtaining that $\beta = \{\beta',\ldots,\beta'\}$. \hfill \Box

According to the lemma, the output of a G-Rep node can be calculated as follows. First, the LLR vector $\alpha'$ of its Rate-C node is calculated as

$$\alpha'_i = \sum_{j=0}^{2^{t-p}-1} \alpha_{i+j2^{t-p}}. \quad (9)$$

Then, the Rate-C node is decoded under SC, obtaining the partial sum vector $\beta'$. In the case that the Rate-C node is a special node, partial sums can be computed through fast decoding techniques. Finally, the partial sum vector $\beta$ of the G-Rep node is given by

$$\beta = \{\beta',\ldots,\beta'\} \quad (10)$$

Several special nodes identified in the past are particular cases of the G-Rep node class: aside from the straightforward Rep node, also Type-I, Type-II and Type-V nodes fit into this category, as long as all information bits are found in the rightmost child node.

**B. Generalized Parity-Check Node**

Frozen bits drive the decoding process thanks to their predetermined value: since they are assigned to low-reliability channels, bit estimations likely to be incorrect can be avoided and LLRs representing wrong values can be influenced positively. From an algebraic point of view, each frozen bit adds a constraint on the possible value of the codeword. Given the recursive nature of polar codes, the same concept applies to the decoding of constituent codes, or nodes in the SC tree. The constraint imposed by the frozen bit in SPC nodes is that of even parity in the codeword [5]: it can be exploited through Wagner decoding, i.e computing the parity of all the node bits and, if not fulfilled, flipping the one associated to the least reliable LLR. The two frozen bits in the leftmost positions of a Type-III node impose even parity constraints on the codeword, namely even and odd bit indices are treated as separate SPC nodes. Type-IV nodes rely on the same concept: the three frozen bits impose even parity constraints on bit indices modulo 4. However, since the fourth bit is an information bit, a suboptimal artifice is developed so that a parity constraint is imposed on the remaining bits, and four separate SPC nodes can be identified and decoded with Wagner decoding.

This even parity constraint can be generalized to a wider category of frozen bit patterns. We call generalized parity-check node (G-PC) a node at stage $t$ having all Rate-1 descendants, except the leftmost one at a certain stage $p < t$ that is Rate-0. This structure, depicted in Fig. 3, imposes $N_p$ parallel single parity checks as follows.

**Lemma 2.** A G-PC node at stage $t$ with the Rate-0 note at stage $p$ contains $N_p$ parallel SPC constraints such that $\sum_{i=0}^{2^{t-p}-1} \alpha_{iN_p+j} = 0$ for all $j = 0, \ldots, N_p - 1$.

**Proof.** A G-PC node identifies a code of rate $R = 1 - N_p/N_t$, for which $N_p$ bits out of $N_t$ are redundancy. So, if there exist $N_p$ independent parity check constraints, we have that those ones are the only constraints that should be used in the decoding, since all other constraints are linear combinations of these independent constraints. The generator matrix of the code identified by the G-PC node is $M = (G^{\otimes_{t-p}})_{0} \otimes G^{\otimes_{p}}$, where $(G^{\otimes_{n}})_{0}$ represents the matrix obtained by the $n$-Kronecker power of $G$ excluding the first row. All the rows of $(G^{\otimes_{t-p}})_{0}$ have even weight by construction. This imposes an even parity check on the codewords of the code defined by $M$. More in detail, given $j \in \{0, \ldots, N_p - 1\}$, the XOR of bits with index $i \mod N_p = j$, $0 \leq i < N_t$ is equal to zero. These parity check constraints are clearly independent, since they have no bits in common. \hfill \Box
The lemma suggests to decode a G-PC node with \( N_p \) parallel Wagner decoders. The LLRs vector \( \alpha \) of the G-PC node is thus divided into \( N_p \) parts \( \alpha^0, \ldots, \alpha^{N_p-1} \) such that
\[
\alpha^j_i = \alpha_{iN_p+j}.
\]
Every LLRs sub-vector \( \alpha^j \) is treated as an SPC and decoded independently through a Wagner decoder. For every sub-vector, the index of the least reliable position is identified as \( p^j = \arg \min \{ \alpha^j_i \} \), and the partial sum vector \( \beta^j \) is calculated through hard-decisions as
\[
\beta^j_i = \begin{cases} 
\text{HD}(\alpha^j_i) \oplus \text{Parity} & \text{if } i = p_j \\
\text{HD}(\alpha^j_i) & \text{otherwise},
\end{cases}
\]
where Parity = \( \oplus \text{HD}(\alpha^j_i) \) for all \( i \). Finally, each element in the partial sum vector \( \beta \) of the G-PC node is calculated as
\[
\beta_i = \beta^j_{i \mod N_p}.
\]
It is worth noticing that the proposed decoding algorithm for G-PC nodes allows to reduce the decoding latency not only through SC tree pruning, but also by allowing decoder parallelization with a factor \( N_p \), since the Wagner decoders are independent.

The even parity constraints imposed by the frozen bits in G-PC are the only independent ones present in the constituent code: thus, the proposed fast decoding technique is optimal. However, this technique can be applied also if other frozen bits are present, i.e. if some of the Rate-1 nodes are in fact Rate-C nodes with \( C \simeq 1 \). In this case, the even parity constraints are still valid, but other constraints brought by the inner frozen bits should be taken into account. We propose to ignore those additional constraints and apply Wagner decoding as if the node was a G-PC. In this case, we call this node a relaxed G-PC (RG-PC), and identify the frozen bits in the Rate-C node as additional frozen (AF) bits. The proposed decoding algorithm is suboptimal, and introduces a tradeoff between error-correction performance and decoding latency.

C. Path Metric for List Decoding

Fast list decoding of polar codes poses the question of how to compute the PM without descending the tree. It has been proven that fast decoding of Rate-0, Rate-1, Rep and SPC can be performed in list decoding as well, with the path metric computed exactly from the LLRs input to the node \([7]–[10], [13]\).

In the same way, the proposed generalized fast decoding allows to compute exactly the path metrics at the top of the tree. Path metrics for G-Rep nodes are computed in two stages: the first one is relative to the Rate-C node, and is computed according to the decoding criterion of its particular frozen bit pattern. Once the Rate-C node has been decoded, the G-Rep node path metric calculation follows the same criterion of standard Rep nodes \([8]\):
\[
PM_{G\text{-Rep}} = PM_{\text{Rate-C}} + \frac{1}{2} \sum_{i=0}^{N_t/N_p-2} \left( \sum_{j=0}^{N_p-1} \text{sgn} \left( \alpha^j_i \right) \alpha^j_i - \eta_j \alpha^j_i \right),
\]
where \( \eta = 1 - 2\beta \) is output by the Rate-C node, and \( \alpha \) is received from the parent of the G-Rep node.

Since G-PC nodes are compositions of parallel SPC nodes, the path metric at the top of the tree is computed in the same way \([8]\), but considering \( N_p \) independent SPC nodes:
\[
PM_{G\text{-PC}} = \sum_{j=0}^{N_p-1} PM_{\text{SPC}_j}.
\]
The same calculation applies to RG-PC nodes: while it is suboptimal, since it ignores the constraints imposed by the AF bits, it is still exact with respect to the same metric computed descending the tree and ignoring said additional constraints.

IV. PERFORMANCE ANALYSIS

In this section, we analyze the impact of generalized fast decoding on both SC and SCL in terms of both speed and error-correction performance.

A. Speed

Table I shows the number of time steps required to decode a set of polar codes with different lengths and rates, and different decoding algorithms. In particular, four code lengths are considered, namely \( N = \{128, 256, 512, 1024\} \), and five code rates \( R = \{1/2, 2/3, 5/6, 1/4, 1/8\} \). All combinations of \( N \) and \( R \) have been constructed targeting the AWGN channel, and a noise standard deviation \( \sigma = 0.5 \). Two baseline decoding algorithms are considered, i.e. Fast-SSC \([5]\) and SSCL-SPC \([8]\); to each of these algorithms, the proposed generalized fast decoding is progressively applied, evaluating the impact on the decoding speed of G-Rep nodes first, then G-Rep and G-PC combined, and finally the three proposed node types, with increasingly high number of AF bits for RG-PC nodes.

The cost of decoding operations for the considered SC-based algorithms is computed as follows: both \( f_g \) and \( g_r \) operations have a cost of 1 time step, regardless of the stage \( t \). Rate-0 and Rate-1 nodes cost 1 time step each, while Rep nodes and SPC nodes cost 2 and 3 time steps, respectively. G-Rep nodes have a cost of 1 time step plus whatever is the cost of the Rate-C node, while both G-PC and RG-PC require 3 time steps to be completed. These cost assumptions do not assume any kind of resource limitation. For SCL-based decoding, we instead assume a common structure in SCL decoders, in which the bit estimates memory structure implements a hardwired XOR tree so that partial sums relative to all SC tree stages are updated as soon as a bit is estimated \([8], [12]\). This implies that information bits need to be estimated one at a time. Moreover, every bit estimation is coupled with the path metric calculation and sorting, and selection of the surviving paths. Thus, given that the size of a node at stage \( t \) is \( 2^t \), the cost of Rate-1 nodes rises to \( 2 \times 2^t \), that of Rep nodes to \( 1 + 2^t \), and that of SPC nodes to \( 2 \times 2^t - 1 \). In the same way, G-PC and RG-PC node require \( 1 + 2 \times (2^t-1) \) time steps. The cost of Rate-0 and G-Rep nodes is unchanged.

G-Rep nodes can be mostly found close to the imaginary border between the majority of unreliable bit-channels and the
TABLE I: Generalized fast decoding time steps.

| $N$ | $R$ | Fast-SSC | + G-Rep | + G-PC | + RG-PC | SSCL-SPC | + G-Rep | + G-PC | + RG-PC |
|-----|-----|---------|--------|--------|---------|---------|--------|--------|---------|
|     |     | 1 AF    | 2 AF   | 3 AF   | 1 AF    | 2 AF    | 3 AF   | 1 AF    | 2 AF    | 3 AF    |
| 128 | 1/8 | 31      | 28     | 26     | 17      | 51      | 47     | 47     | 42      | 34      | 33      |
|     | 1/4 | 61      | 60     | 54     | 42     | 42      | 51      | 47     | 47     | 42      | 34      | 33      |
|     | 1/2 | 82      | 80     | 80     | 49     | 39      | 176     | 172    | 172    | 172     | 113     | 103     |
|     | 2/3 | 52      | 51     | 51     | 40     | 35      | 200     | 198    | 198    | 192     | 170     | 137     |
|     | 5/6 | 55      | 54     | 42     | 34     | 25     | 20      | 247    | 245    | 175     | 142     | 129     | 124     |
| 256 | 1/8 | 116     | 114    | 114    | 96     | 78      | 127     | 125    | 124    | 114     | 106     | 96      |
|     | 1/4 | 142     | 140    | 140    | 120    | 115     | 187     | 184    | 184    | 184     | 156     | 151     |
|     | 1/2 | 113     | 111    | 108    | 85     | 75      | 323     | 317    | 312    | 307     | 269     | 235     |
|     | 2/3 | 115     | 114    | 105    | 75     | 57      | 408     | 402    | 370    | 355     | 318     | 285     |
|     | 5/6 | 79      | 75     | 72     | 64     | 45      | 476     | 468    | 455    | 455     | 440     | 358     |
| 512 | 1/8 | 116     | 109    | 109    | 92     | 82      | 194     | 188    | 182    | 176     | 156     | 134     |
|     | 1/4 | 232     | 220    | 211    | 155    | 140     | 394     | 382    | 342    | 342     | 324     | 252     |
|     | 1/2 | 238     | 231    | 221    | 163    | 131     | 650     | 641    | 641    | 624     | 515     | 477     |
|     | 2/3 | 202     | 193    | 190    | 151    | 121     | 805     | 797    | 785    | 771     | 707     | 617     |
|     | 5/6 | 136     | 125    | 116    | 86     | 78      | 940     | 925    | 891    | 881     | 831     | 793     |
| 1024| 1/8 | 250     | 240    | 240    | 185    | 160     | 398     | 386    | 386    | 380     | 309     | 276     |
|     | 1/4 | 353     | 344    | 344    | 269    | 224     | 712     | 702    | 697    | 697     | 589     | 496     |
|     | 1/2 | 420     | 405    | 405    | 311    | 256     | 1274    | 1251   | 1251   | 1241    | 1091    | 936     |
|     | 2/3 | 344     | 335    | 334    | 254    | 211     | 1444    | 1432   | 1422   | 1397    | 1280    | 1174    |
|     | 5/6 | 232     | 224    | 215    | 173    | 141     | 1477    | 1470   | 1431   | 1350    | 1305    | 1195    |

majority of reliable ones. Regardless of the code rate, their number is small, and the gain in terms of time steps limited. The size of G-Rep nodes tends to increase as the code length increases.

As pointed out in Section III-B, G-PC nodes revert to SPC nodes when $N_p = 1$. Additional G-PC nodes where $N_p > 1$ are not always found: this can be noticed by the fact that the number of time steps in the “+ G-PC” columns in Table I is sometimes unchanged from the “+ G-Rep” columns. Nevertheless, the speedup brought by the fast decoding of G-PC nodes can be significant: for SC decoding, G-PC can save up to 21.8% time steps with $N = 128$, $R = 5/6$, for a combined gain of 23.6% with G-Rep nodes. With SCL decoding, the gain brought by G-PC nodes is larger, since $N_p$ SPC nodes of shorter length can be decoded in parallel: G-PC nodes save up to 28.3% time steps, and up to 29.2% when combined to G-Rep nodes.

Similar behavior can be observed for RG-PC nodes. With higher number of AF bits, the number of RG-PC nodes found in a code increases, and so does their time step saving. For SC decoding, RG-PC nodes with a single AF bit can save up to 14.5% time steps with $N = 128$, $R = 5/6$, for a combined contribution with G-Rep and G-PC nodes of 38.2%. The combined gain can reach 54.5% if the AF bits increase to 2, and to 63.6% with 3 AF bits. The gain brought by RG-PC nodes in SCL decoding is larger in absolute value, but averagely smaller in percentage. With one AF bit, the time step gain can reach 18.4%, with $N = 128$, $R = 1/4$, for a combined contribution with G-Rep and G-PC nodes of 20.4%. The combined time step gain can instead reach 47.8% and 49.8% with 2 and 3 AF bits, respectively. As shown in the next Section, with a higher number of AF bits comes more significant error-correction performance loss.

The decoding speed can be further increased with respect to the results detailed in Table I by ad-hoc code construction that maximizes the occurrence of the identified special nodes, as shown in [14].

### B. Error-Correction Performance

The proposed G-Rep and G-PC nodes do not impact the error-correction performance of the considered Fast-SSC and SSCL-SPC decoding algorithms. However, the approximation introduced by the RG-PC nodes can cause a performance loss. As an example, Fig. 4 and Fig. 5 report the block error rate (BLER) curves for $N = 1024$, $R = 1/2$ and $N = 256$, $R = 1/8$, respectively. The SSCL-SPC curves have been obtained with a list size $L = 4$, and a CRC length of 16 for Fig. 4 and of 8 for Fig. 4. It can be seen that as the number of AF bits increases, a larger error-correction performance degradation is observed. The entity of this degradation depends on the number of RG-PC nodes encountered, the length and rate of the code, and the effectiveness of the decoding algorithm. List-based decoding shows a higher degree of resilience to the RG-PC degradation in both cases, while the weaker code used in Fig. 5 suffers larger losses than its stronger counterpart in Fig. 4.

### V. Conclusion and Future Work

In this work, we introduced a generalized approach to fast decoding of polar codes. It identifies three multi-node subcode patterns that, along with including most existing
subcodes, allow fast decoding of a wide variety of frozen and information bit patterns. Decoding rules are provided for any SC-based decoding algorithm, while fast path metric calculation for SCL is derived as well. The proposed decoding approach is evaluated in terms of speedup and error correction performance against baseline fast decoding algorithms, over a wide set of code lengths and rates. Without any error-correction performance degradation, our technique shows up to 23.6% and 29.2% decoding latency gain with respect to fast SC and SCL decoding algorithms, respectively. These figures can rise up to 63.6% and 49.8% if a performance loss is accepted: the entity of the degradation depends on the combination of code and decoding algorithm parameters, and on the desired speedup.

The framework described in this work is not limited to polar codes; since the three identified subcodes are multi-node patterns, they valid for multi-kernel codes as well [15], that are constructed with combinations of kernels of different sizes. Future work foresees the evaluation of the effectiveness of the proposed generalized fast decoding to practical multi-kernel codes.

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