Ge-Source Based L-Shaped Tunnel Field Effect Transistor for Low Power Switching Application

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Abstract
In this work, the performance of the heterojunction L-Tunnel Field Effect Transistor (LTFET) has been analyzed with different engineering techniques such as bandgap engineering, pocket engineering, work-function engineering, and gate dielectric engineering, respectively. The electrical characteristics of the device have been investigated by using Synopsys Sentaurus TCAD tool and compared with some recent other TFETs. The device has been analyzed in terms of DC as well as AC analysis and offers ON-state current of $2.12 \times 10^{-5} \, \text{A} \mu \text{m}^{-1}$, OFF-state current of $1.09 \times 10^{-13} \, \text{A} \mu \text{m}^{-1}$, current ratio of ~$10^8$ and sub-threshold slope (SS) of 21 mV/decade and the threshold voltage of 0.26 V and compared to the conventional Si/Ge source L-shaped TFETs without pocket simulation result. The pocket engineering techniques suppress the leakage without degrading the ON current, threshold voltage and SS of the proposed device. The simplified fabrication steps of the proposed device have also been discussed. The proposed L-TFET is free from ambipolarity issues and can be used to develop low-power switching devices.

Keywords Tunnel field effect transistor · Heterojunction · Band-to-band tunneling · Ambipolarity · Subthreshold swing

1 Introduction
In the rapid advancement of Internet of Things (IoT) and wearable technology, low power operation is a huge concern for digital applications [1]. Though MOS devices can be utilized in microprocessor and static RAM (SRAM) for low power application but the subthreshold swing (SS) cannot be lowered below 60 mV/dec [2]. On the current technology nodes, rapid switching and scaling are the substantial factors as per the device requirements. The downscaling of metal oxide semiconductor field-effect transistors (MOSFETs) dimensions in sub-nanometre region increases the proximity between source and drain increases that further reduces the controlling capability of the gate over the channel. Also, scaling down the MOSFET leads to high SS, short channel effects, and leakage current [3]. The gated reverse-biased p-i-n diode named Tunnel Field-effect transistor (TFET) works on the principle of band-to-band-tunneling (BTBT) and exhibits low leakage current and reduced short channel effects. It has been appeared as a promising candidate due to its steep slope (SS < 60 mV/dec) and can be used for low power applications [4, 5]. However, TFET withstands some limitations like low on-state current, large ambipolar current, and poor RF performance that demand additional improvements [6, 7]. These technical issues can be entangled by using different design approaches like using high-k material as dielectric [8], III-V semiconductors [9], low-band gap material [10], and making different shaped TFET [11, 12].

Several researchers have reported different strategies to overcome the shortcomings of TFET [12, 13]. The on-state current can be increased by increasing the gate-source overlap that enhances the tunneling area, using doped pocket [14], and hetero gate dielectric [15]. Another solution is to increase the effective channel length by structural changes like recessed channel and mesa structure [16]. The ambipolarity can be reduced by considering asymmetric source-drain doping, large band gap materials for drain, gate-drain overlap, and heterogeneous gate dielectric, etc. [17, 18] but it is not possible to fully remove the ambipolar current in TFET. Also, these strategies can result in some serious problems in TFETs like increases in drain resistance, lowers on-state current or makes
the process more complex [19]. The ultra-low power applications require high on-state current to enhance the fan-out and low off-state/leakage current to reduce the stand-by power consumption. The leakage current depends upon the device design parameters. The moderate body doping suppresses the off-state current and enhances the on-state current. The optimization of device parameters is done in a way to achieve high on-state current, low off-state current, and negligible ambipolar behaviour.

Considering all the above points in mind, in this paper, authors reported Ge-source based L-shaped gate Tunnel Field Effect Transistor (LTFET) with pocket has been reported and compared with Si based LEFET with and without pocket by using Synopsys TCAD tool. The proposed device has been optimized in terms of various parameters such as source doping, pocket doping, different BTBT models, gate oxide variation, work function variation. This paper is organized as follows. The proposed TFET structure and simulation methodology are described in section 2. In section 3, homo and heterojunction TFET with and without pocket are explained. Section 4 and 5 deal with the optimization of the proposed device and fabrication process flow respectively. In section 6, DC analysis and AC analysis are presented. Section 7 deals with the comparative analysis of the proposed device with already existing structures. Finally, this paper is concluded.

## 2 Proposed TFET Structure and Simulation Methodology

In TFET, the movement of the carrier depends upon the BTBT phenomena and the tunneling probability depends upon the height, width, shape of the potential barrier, and tunneling mass of charge carriers. Kane’s approach and Wentzel-Kramers-Brillouin’s approach (WKB) approaches can be used to calculate the rate of BTBT [20]. The rate of tunneling is given in eq. (1) [21]:

$$T = \exp \left[ \frac{\sqrt{2m_e F_\perp} E_t^{5/2}}{3q\hbar} \exp \left( \frac{-E_\perp}{E_m} \right) \right]$$

where q = electron charge, F = average junction field, E_\perp = transverse component of total carrier energy, E = the impact of the transverse-energy-state carriers on the tunneling magnitude.

Figure 1 shows the cross-sectional view of proposed LTFT device with Ge as source material and HfO_2 as gate dielectric.

| Parameters                  | Symbol | Values | Unit |
|-----------------------------|--------|--------|------|
| Equivalent oxide thickness  | t_ox   | 0.57   | nm   |
| Source doping concentration | N_s    | 1 × 10^{18} | cm\(^{-3}\) |
| Drain doping concentration  | N_d    | 1 × 10^{18} | cm\(^{-3}\) |
| Pocket doping concentration | N_p    | 1 × 10^{18} | cm\(^{-3}\) |
| Channel length              | L_ch   | 32     | nm   |
| Gate work function          | \phi_{mg} | 4.3 eV | eV   |
| SOI thickness               | t_{si} | 30     | nm   |
| BOX Thickness               | t_{box} | 5     | nm   |

Fig. 1 Schematic diagram of LTFET
In the source region, the low band gap material Ge offers higher tunneling in the on-state while on the drain side the high band gap material Si lower the tunneling. The Aluminium as metal gate and HfO2 as gate oxide of 4 nm physical thickness has been used. For all simulation, the value of dielectric constant of HfO2 is 27. The length of source and drain regions are 40 nm each while width of source is 40 nm and drain is 55 nm. The width of pocket and channel regions are 15 nm while length of pocket is 40 nm, respectively. The length and width of gate material is 40 and 50 nm whereas the gate length is 32 nm, respectively. Table 1 shows the TFET device parameters considered for simulation.

In Sentaurus TCAD, all the simulation has been done by using non-local BTBT model. To account the effect of high doping concentration on carrier mobility, Doping Dependent Mobility model has been used. Also, Shockley-Read-Hall (SRH) Recombination Model has been used. The accurate modeling of charge carrier transport in LTFET is achieved by activating, doping density, band gap narrowing, and thermionic models. All the simulations have been carried out at room temperature.

### 3 Proposed Device Justification

#### 3.1 Homo and Hetero Junction TFET with and without Pocket

Considering the device dimensions mentioned in Table 1, the simulation study of LTFET structure using Si and Ge as source region material was performed. The analysis has been carried out for LTFET with pocket and without pocket structures by taking Si and Ge as source materials. It has been observed that LTFET device using Ge as source material exhibits very good performance as it has high on-state current and low leakage current. But in Si based LTFET though the

| Parameters     | Si (without pocket) | Si (with pocket) | Ge (without pocket) | Ge (with pocket) |
|----------------|---------------------|------------------|---------------------|------------------|
| $I_{ON}$ (A)   | 1.52*10^{-9}        | 1.59*10^{-9}     | 2.11*10^{-5}        | 2.12*10^{-5}     |
| $I_{OFF}$ (A)  | 2.41*10^{-18}       | 2.88*10^{-18}    | 6.99*10^{-12}       | 1.09*10^{-13}    |
| $I_{ON}/I_{OFF}$ Ratio | 0.63*10^{-9} | 0.55*10^{-9}     | 0.30*10^{-7}        | 1.94*10^{-8}     |
| $g_m$ (S/m)    | 4.32*10^{-9}        | 4.21*10^{-9}     | 3.59*10^{-5}        | 3.54*10^{-5}     |
| $V_{th}$ (V)   | 0.62                | 0.60             | 0.30                | 0.26             |
| SS (mV/dec)    | 33                  | 31               | 27                  | 24               |
off-state current is low, the on-state current is also poor. On comparing the results with pocket and without pocket structures, the Ge-LTFET with pocket device shows very good results because of the high $I_{ON}/I_{OFF}$ ratio. Further analysis has been carried out using Ge with pocket structure. The influence of the use of pocket is more noticeable in off-state current than in on-state current. The simulated results of Ge-LTFET and Si-LTFET with pocket and without pocket are plotted in Fig. 2.

Ge-LTFET device shows very good performance as there is no ambipolarity observed in the results. All the obtained results $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$ ratio, SS, $g_m$, $V_{th}$ for both Si and Ge based LTFTFs with and without pocket structures are given in Table 2.
3.2 Calibration of Proposed Device

First of all, the simulation data of the proposed LTFET structure is calibrated against the experimental data of reference [22] at drain voltage 0.5 V as shown in Fig. 3. It is observed that there is a good matching of both data, which certifies the validity of the selected models.
4 Optimization of the Proposed Device

The optimization of the proposed LTFET has been done by changing different parameters like using the different band to band models, variation in source and pocket doping concentration, gate oxide variation, work function variation and the transfer characteristics, $I_{ON}/I_{OFF}$ ratio, SS, and threshold voltage of the device are obtained.

4.1 Different Band to Band Models

BTBT can be achieved by two processes; the first is direct tunneling and the other one phonon-assisted tunneling. In direct tunneling, there are two models, local and non-local [23]. In Sentaurus TCAD, various local BTBT tunneling models are Hurkx BTBT model, Schenk BTBT model, Simple (E1, E2, E1_5) BTBT model. The non-local model is named as Non-local BTBT model. In both local and non-local models, the electron-holes generation profiles are different. In the former case, electron-holes generation profiles are the same while in the latter case holes are generated at the beginning, and electrons are generated at the end of tunneling.

In TCAD tool, for Schenk BTBT model bandgap narrowing model can be used in two ways. Simply, bandgap narrowing can be computed without depending on temperature (at $T = 0$ K) and in the other way, temperature dependence is accounted. In Hurkx model, tunneling carriers are modelled by an additional generation-recombination process. The Hurkx model can be written as eq. 2 [24]:

$$R_{BTBT} = A D e^{B/e}$$

(2)

where $R_{BTBT}$ is the BTBT rate, and the coefficients $A, B, D, and p$ can be specified in the BTBT parameter set. These coefficient values can be used to define carrier generation and recombination. E1, E2, E1_5 selects the simple models.

The Non-local BTBT model implements the nonlocal generation of electrons and holes that occurs because of the direct and phonon-assisted BTBT processes. In the direct bandgap semiconductors, direct tunneling occurs. But in the indirect semiconductors (Si and Ge), the phonon-assisted tunneling process dominates. The electron-holes generation rate is obtained by nonlocal path integration. Suppose a tunneling path of length $l$ is given that starts at $x = 0$ and ends at $x = l$. The holes are generated at $x = 0$ and electrons are generated at $x = l$. The net hole recombination rate due to phonon-assisted tunneling can be written as eq. 3 [25]:

$$R_{net}^p = |\nabla E_V(0)| C_p \exp \left( -\frac{2 \kappa_V d x - 2 \kappa_C d x}{\kappa_C d x} \right) \left( \exp \left( \frac{E_F - E_p(l)}{kT(l)} \right) + 1 \right)^{-1} \left( \exp \left( \frac{E_F - E_p(0)}{kT(0)} \right) + 1 \right)^{-1}$$

(3)
\[ C_p = \frac{1}{\hbar} \left( \frac{1 + 2N_{op}}{\rho \varepsilon_{op}} \right) D_{op}^2 \int_0^{l_{opt}} \frac{m_Y m_C}{\hbar \sqrt{2m_Y E_{g,tun}}} \left( \frac{dx}{x \kappa_Y} \right)^{-1} \left( \frac{dx}{x \kappa_C} \right)^{-1} \left[ 1 - \exp \left( - \frac{k_Y x_0}{\hbar \kappa_Y} \right) \right] \left[ 1 - \exp \left( - \frac{k_C x_0}{\hbar \kappa_C} \right) \right] \] 

where \( \hbar \) is the Planck’s constant, \( g \) is the degeneracy factor, \( \rho \) is the mass density, \( \kappa_Y \) and \( \kappa_C \) are the magnitude of imaginary vectors.

\( D_{op}, \varepsilon_{op} \) and \( N_{op} \) are the deformation potential, energy, and the number of optical phonons, respectively.

Figure 4 shows the simulation results of proposed LTFET using different models. Both local and non-local were used one by one and results were obtained. In non-local models, different tunneling paths are considered. For every different tunneling path, the electric field at each point of the path...
changes dynamically. Using non-local model, the change in the electric field at each point of every tunneling path is determined and hence more accurate results are obtained. Also, from the results, it is very evident that non-local BTBT model gives the best results among all the models.

4.2 Source & Pocket Doping Variation

The effect of changing the doping concentration in source region and pocket region has been discussed here. For both cases, three different concentration values were considered.

As shown in Fig. 5a, for source doping region, the concentration values 1E17, 1E18, and 2E18 were taken for simulations. From the obtained results it has been found that the source concentration 1E18 can be considered for further analysis as it shows high on-state current and low off-state current. Figure 5b shows the obtained results for variation in pocket doping concentration. In this analysis, the concentration values 1E18, 1E19, and 2E18 were considered for simulations. It is evident from the results that pocket doping with concentration value 1E18 shows low off-state current and high on-state current. For further analysis, the source and pocket doping concentration values are fixed i.e. 1E18.

4.3 Gate Oxide Variation

The gate dielectric should be chosen carefully to achieve high on-state current and low SS. In this analysis of LTFET, the
results of 4 nm thick dielectric materials with different dielectric constants are compared.

It is very clear from Fig. 6 that the high dielectric constant material HfO$_2$ shows superior performance over the other two materials (SiO$_2$ and Si$_3$N$_4$). On increasing the dielectric constant, the on-state current increases. The small dielectric thickness offers the solution to the problem of low on-state current.

### 4.4 Work Function Variation

In LTFET, the variation in the work function of gate metal was done to observe the effect on drain current. The work function values were varied from 4.3 eV to 4.7 eV. Figure 7 shows the simulated results of drain current vs gate voltage at different work functions. Increasing the work function reduces the on-state current.

For the work function value of 4.3 eV, the LTFET exhibits high on-state current and low off-state current. The variation in work function causes the variation in threshold voltage, on-state current, and off-state current. The simulated value of threshold voltage of 0.58 V was achieved for $\phi_m = 4.3$ eV and 0.87 V was obtained for $\phi_m = 4.7$ eV.

### 5 Fabrication Details of the Proposed Device

The proposed LTFET can be fabricated by using CMOS compatible process flow as shown in Fig. 8. Following steps have been required for the possible fabrication of the proposed device. Firstly, intrinsic silicon layer is deposited over SiO$_2$ (Fig. 8a).

**Thermal Oxidation and Diffusion** Thermal oxidation is used to grow the oxide layer for passivation of i-channel region. Diffusion method is used to dope the silicon layer (n + layer) for the formation of pocket and drain regions (Fig. 8b). The drive-in process is followed by diffusion process. In this process, the dopants are forced to drive inside the doping windows of the wafer as a result surface concentration decreases and dopants move further. **Etching:** The etching of Si can be done by using dry etching method or wet etching method. In dry etching, gas plasma etches Si (isotropic/anisotropic) depending upon the gas recipes used. In wet etching method, chemicals are used to etch Si. After patterning the oxide, etching of Si layer is done (Fig. 8c and d).

**Low Pressure Chemical Vapour Deposition (LPCVD)** LPCVD method has been used to deposit a 40 nm thick Ge layer to form the source region. Further the Ge layer is p + doped by using diffusion method (Fig. 8e).

**Atomic Layer Deposition** This technique has been used to deposit HfO$_2$ as gate oxide (Fig. 8f).

### 6 Results and Discussion

The simulated results of LTFET device have been presented in this section. The source and back gate is kept at ground potential. The different device analysis like DC analysis, AC analysis and the effect of different parameters on the device performance are presented in subsections.

![Fig. 10](image-url)  
**Fig. 10** a Drain current vs. $V_{gs}$ for different drain voltages b Drain current vs. $V_{ds}$ for different gate voltages
6.1 DC Analysis

6.1.1 Energy Band Diagram

The electrostatic potential distribution of simulated LTFET using optimised device dimensions is presented in Fig. 9a. Figure 9b depicts the energy band diagram of Si and Ge LTFET with pocket structures.

In the proposed device, when the gate overlaps the source, line tunneling occurs and such a TFET structure is also known as line TFET [26]. In this case, increasing the Vgs bends the energy band towards the gate oxide until the conduction band edge crosses the valence band edge and BTBT happens. The uniform electric field beneath the gate oxide implies that in line tunneling the effect of Vdon the source can be ignored. Below the gate-source overlap, all tunnel paths are available at the same amount of band bending but the paths get shorten as Vgs is increased. As the tunneling is located near the gate region and both electric field and tunnel path are aligned, a small amount of Vgs is sufficient for band bending. When the TFET is conducting, the stronger the band bending makes shorter the tunnel path. In short, ION depends upon the overlapping between gate and source. From the energy band diagram plotted in Fig. 9b, it is observed the using Ge as source material in LTFET shortens the tunneling path and more tunneling occurs as compared to Si-LTFET.

6.1.2 Input and Output Characteristics

The transfer characteristic of proposed LTFET is shown in Fig. 10a. The Vgs was varied from −0.2 V to 1.2 V for various drain voltages. It is evident from the results that the proposed LTFET works very efficiently for the wide range of applied gate voltages. As applied Vgs is increased, tunneling current increases. When the applied Vgs is equal to Vdd, the transistor is in on-state and the corresponding current value is ION. The ION of 4.4 μA, 2.12*10^{-5} A, 4.32 *10^{-5} A and IOFF of 1.03 *10^{-13} A was observed for Vds 0.3 V, 0.5 V, 0.7 V. The proposed LTFET structure works very efficiently with high on-state current, low off-state current and no ambipolar behaviour has been observed. The output characteristics of proposed LTFET for the drain voltages range from 0 to 2.4 V for different gate voltages are shown in Fig. 10b. For small values of Vds, BTBT is inefficient because of low carrier density but BTBT rises as Vds is increased. The drain current increases as the Vds is increased until the edge of conduction band in drain region falls below the edge of the conduction band in the channel. After that drain current saturates and Vds has no longer affect the tunneling. On increasing the gate voltage, the exponential rise in drain current demonstrates better gate control. The flat saturation region indicates that the effects like kink effects are highly suppressed in this proposed LTFET.

6.1.3 Variation in Drain Voltage

Figure 11 shows the influence of changing the Vds on threshold voltage, SS, and gm.

Figure 11a shows that as Vds is increased, the threshold voltage obtained by the constant current method remains the same whereas the threshold voltage obtained by the transconductance method, increases. Figure 11b depicts that...
point SS and average SS. The increase of Vds increases the transconductance as shown in Fig. 11c.

**Fig. 12** Capacitance plot of proposed LTFET

**Fig. 13** Proposed LTFET (a) $g_m$ vs. $V_{gs}$ (b) $g_d$ vs. $V_{ds}$ (c) $A_v$ vs. $V_{gs}$
6.2 AC Analysis

To determine the AC performance, it is very important to determine the capacitance of the device. Capacitance creates a path between the input and output that leads to circuit oscillations and signal distortion. The change in total gate capacitance \( C_{gg} \), gate-drain capacitance \( C_{gd} \), and gate-source capacitance \( C_{gs} \) with variation in gate-source voltage is plotted in Fig. 12. The increase in \( V_{gs} \) increases both \( C_{gg} \) and \( C_{gd} \) whereas \( C_{gs} \) decreases. The capacitances \( C_{gg} \) and \( C_{gd} \) are accounted when charge carriers are injected from drain to gate. On increasing the gate voltage, an inversion layer is formed that decreases the potential barrier at the drain terminal. Hence, capacitance is increased [27].

The analyzed current driving capability or amplification of LTFET at different \( V_{gs} \) is shown in Fig. 13. The reciprocal of output resistance is known as \( g_{ds} \). For high amplification ability of the device, \( g_{ds} \) should be low [28, 29]. The \( g_m \) and \( g_{ds} \) can be expressed by (5) and (6):

\[
g_m = \frac{\partial I_D}{\partial V_{ds}} \tag{5}
\]

\[
g_{ds} = \frac{\partial I_D}{\partial V_{gs}} \tag{6}
\]

\( g_m \) depends upon the slope of transfer characteristics that determine the switching speed of the device. For high switching speed, a high value of \( g_m \) is required. As the applied gate voltage is increased, the drain current increases and \( g_m \) also increases, as shown in Fig. 13a. The output conductance as a function of \( V_{ds} \) is also shown in Fig. 13b. For saturation-like region, when \( V_{gs} \) is increased, due to BTBT drain current increases and as a result \( g_{ds} \). The ratio of \( g_m/g_{ds} \) is known as intrinsic gain or maximum voltage gain \( (A_v) \) as given in eq. (7) [29].

\[
A_v = \frac{g_m}{g_{ds}} \tag{7}
\]

Figure 13c depicts that the intrinsic gain of proposed device remains the same for low gate voltage but then abruptly increases for high gate voltages.

Equation (8) states that \( f_T \) is directly proportional to \( g_m \) and inversely proportional to the total gate capacitance. At low voltage values, \( g_m \) dominates but on increasing the voltage values, total gate capacitance starts dominating. So, the \( f_T \) starts decreasing once it attains maximum peak as shown in Fig. 14a.

| Table 3 | Comparison of proposed LTFET with other TFETs |
|---|---|
| Ref. no. | \( V_{dd} \) (V) | \( I_{ON} \) (A/\( \mu \)m) | \( I_{OFF} \) (A/\( \mu \)m) | \( I_{ON}/I_{OFF} \) | SS (mV/dec) | EOT (nm) | Device specification |
| [31] | 0.75 | \( 10^{-7} \) | \( 10^{-16} \) | 1E9 | 26 | 1 | Si TFET |
| [32] | 0.4 | \( 18*10^{-6} \) | \( 6*10^{-15} \) | 1E9 | 20 | 0.682 | Ge TFET (FD) |
| [33] | 1 | \( 10^{-7} \) | \( 10^{-15} \) | 1E8 | – | 1 | Si LTFET |
| [12] | 0.5 | \( 10^{-4} \) | \( 10^{-12} \) | 1E8 | 14 | 0.5 | III-V heterojunction TFET |
| [26] | -1 | – | – | – | 27–56 | 2–4 | Cylindrical gate TFET |
| Proposed work | 0.5 | \( 2.12*10^{-5} \) | \( 1.09*10^{-13} \) | 1.94E8 | 24 | 0.57 | Ge sourcebased LTFET |
\[ f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad (8) \]

The mathematical expression for GBP is given in eq. (9) that shows GBP depends upon \( g_m \) and \( C_{gd} \) [30]. For the proposed LTFET, Fig. 14b shows the results obtained for GBP with variation in \( V_{gs} \). GBP firstly attains a maximum value as the voltage is increased and then decreases.

\[ GBP = \frac{g_m}{2\pi C_{gd}} \quad (9) \]

7 Comparison with Other LFETs

The comparison of the proposed LTFET device with already reported TFET devices like Si TFET, fully-depleted (FD) SOI-TFET with Ge source, Si LTFET, TFET using III-V, etc. is given in Table 3. From the comparison, it can be concluded that the proposed LTFET using Ge as source region is performing very efficiently and further RF noise analysis can be done to observe the performance.

8 Conclusion

Ge-source based LTFET with and without pockets has been investigated and compared with Si based LEFET with and without pocket by using Synopsys TCAD tool. The proposed device has been optimized in terms of various parameters such as source doping, pocket doping, different BTBT models, gate oxide variation, work function variation. The device offers high on-current of \( 2.12 \times 10^{-5} \) A\(\mu \)m\(^{-1}\), off-current of \( 1.09 \times 10^{-13} \) A\(\mu \)m\(^{-1}\), current ratio of ~10\(^8\) and SS of 24 mV/decade and \( V_{th} \) of 0.26 V. The investigation shows that proposed device is free from ambipolarity and drain voltage variation does not much effect SS and OFF current. Furthermore, the AC analysis of the device has also been studied to find that the proposed LTFET device is a low power device and it is a suitable candidate for low power digital applications. Moreover, in the current scenario of an information-based society, it can be used for Internet of Things (IoT) application.

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Declarations

Ethics Approval Not Applicable.

Disclosure of Potential Conflicts of Interest Not Applicable.

Competing Interests Not Applicable.

Research Involving Human Participants and/or Animals Not Applicable.

Informed Consent Not Applicable.

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Consent for Publication All authors are giving consent for publication.

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