A Nine-Level Inverter With Single DC-Link and Low-Voltage Capacitors as Stacked Voltage Sources With Capacitor Voltage Control Irrespective of Load Power Factor

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ABSTRACT This article proposes a multilevel inverter topology with single dc-link and series-connected capacitors as stacked voltage sources for multilevel voltage generation. The voltage deviation of a dc-link capacitor will occur whenever a phase terminal connects to the balanced neutral points (NPs: terminal joints of dc-link capacitors). On the contrary, if the voltage of a dc-link capacitor deviates from the nominal voltage, the same phase currents can be utilized to balance these NPs. This new technique is being proposed for the first time in the literature. Any voltage disturbance of the dc-link capacitors is balanced using the motor phase currents, irrespective of load power factor and modulation indices. For the balanced NPs, whenever a phase connects to an NP, the other phase terminal tapping positions are varied on the dc link to establish \( i_A + i_B + i_C = 0 \) for that NP. The pole voltage level variation at motor phase terminals is undisturbed by adding extra cascaded H-bridges (CHBs) at each phase leg. The voltages of CHB capacitors are controlled conventionally by inverter pole voltage redundancies. The detailed experimental results for open-loop V/f and closed-loop field-oriented control on an induction motor are presented using a nine-level laboratory prototype.

INDEX TERMS Cascaded H-bridge (CHB), common coupling point balancing, induction motor, inverter, multilevel, neutral point (NP) balancing, single dc-link, split dc-link, stacked dc-link.

I. INTRODUCTION

Multilevel inverters (MLIs) are used extensively in applications such as motor drive [1], [2], high-voltage dc transmission [3], renewable energy resources [4], and power-factor correction application [5]. The wide variety of applications of MLIs is due to benefits, such as low switching loss, low \( dv/dt \) stress, near sinusoidal phase voltage and phase current with less harmonic content, low-voltage switching devices, and low electromagnetic interference (EMI) to the surroundings. The neutral points clamped (NPC) MLIs using a single dc link gained popularity in industry and academia over other basic inverters (flying capacitor (FC) and cascaded H-bridge (CHB) based inverters) due to their simple construction. The voltage balancing of the dc-link capacitors or voltage balancing of the neutral points (NPs) is the major drawback of a NPC-based MLI. But, it is worth noticing that splitting a dc link into more levels provides the benefit of using low-voltage switching devices. Techniques found in the literature [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] to solve the NP voltage balancing problem can be categorized as follows.

1) Creating the dc-link NPs using isolated dc power supplies in [6], [7], and [18].
   a) One of the conventional techniques.
   b) Bulky and inefficient phase-shifting transformers are employed with multiple diode bridge rectifiers.
c) Each time, a new transformer design is required to increase NP numbers.

2) Auxiliary balancing circuit for the NPs in [8], [9], [10], and [17].
   a) Separate isolated dc power supplies are required to drive the auxiliary circuits.
   b) Complexity for the auxiliary circuits increases as more dc-link capacitors are added in series.

3) Smart control of the converter switches by the controller in [11], [12], [13], [14], [15], and [16].
   a) No extra power supply and no multiphase transformer are required.
   b) Complexity is less even if more dc-link capacitors are added across the dc link.

Out of these three categories, smart control of the converter switches using switching state redundancies is the easiest way to control the voltage deviation of dc-link capacitors. The techniques using switching state redundancies presented in [11] and [12] have reported limitation on load power factor and modulation indices. The other dc-link capacitor voltage balancing technique from [19] uses only single NP, and the voltage stress on the switches is high, either $V_{dc}$ or $V_{dc}/2$. A minimum stored energy-based cost function is used in [14] for the voltage control of dc-link capacitors. A space vector redundancy based dc-link capacitor balancing technique using inverter phase currents is proposed by Hotait et al. [20], but this work does not highlight anything about the auxiliary capacitors charging, discharging, or balancing. The work presented by Lalili et al. [21] for dc-link capacitor voltage balancing is limited by only simulation results; no details of phase voltage and phase current are presented during the balancing action.

However, these above-mentioned techniques control the voltage of dc-link capacitors on an average time basis of an entire fundamental cycle. The techniques presented in [22], [23], and [24] have introduced an instantaneous voltage balancing scheme using a six-phase induction machine (IM) load. Zero NP current is asserted either by placing two opposite phase terminals on the same NP or by placing the terminals in the dc-link buses. Any imbalance in two opposite phase currents may deviate the NPs, which is only controlled using bleeder resistors with high time constants. Moreover, the solid-state switches have unequal turn-ON and turn-OFF times, which may also disturb the balancing of dc-link capacitors during the pulselength modulation operation. These works do not address the initial or steady-state voltage deviation of the dc-link capacitors. In addition, most of the existing drive systems in the present industry are supplied as a three-phase load.

This work presents a voltage deviation control technique for the stacked dc-link capacitors using the phase currents of a three-phase IM. In the presence of voltage disturbance of a dc-link capacitor, the currents at the NPs are judiciously controlled utilizing the pole voltage redundancies. This control charges/discharges the dc-link capacitors to balance the voltage to their nominal reference voltage. Once the dc-link capacitors achieve their steady-state nominal voltage, zero instantaneous currents are drawn from all the NPs to keep the dc-link capacitors balanced in further PWM operations.

In general, for conventional MLIs, as the number of levels increases, the device requirement also increases for inverters with a single dc link. The tradeoff stands among the number of isolated dc supply, device voltage ratings, and the number of components. The multilevel works in [25], [26], [27], [28], and [29] have introduced new topologies for motor drive and grid-tied applications with high components count and less $dv/dt$ stress. The major drawback of the topologies from [25], [26], and [27] is the requirement of isolated dc power supplies. The work by Rodriguez et al. [26] is a high-power synchronous motor drive application, which requires 18 isolated dc power supplies. The work presented in [27] is a general topology with only CHB inverter cells. Although this nine-level inverter requires lesser components (36 switches, 9 CHB capacitors), it also requires three isolated dc power supplies.

The topology proposed by Saedifard et al. [28] is a seven-level hybrid MLI with large component count. This topology has addressed the issue of dc-link capacitors and FCs voltage balancing using switching state redundancies for the resistive-inductive load. Still, the topology has a serious limitation on voltage balancing at higher modulation indices for high power factor load. The topology from [29] is a five-level active NPC topology that addresses NP voltage balancing and FCs voltage balancing with low component count. But this low component count for this topology is compromised by using high voltage devices. Moreover, both these topologies [28] have the drawback of balancing dc-link capacitors based on average zero currents drawn from an NP in each $60^\circ$ sector of a fundamental cycle.

Compared to these topologies mentioned above, this article is proposing another new unique topology with a single dc link. The stacked dc-link capacitors’ voltages are balanced using pole voltage redundancies, irrespective of the front-end converter operation. The key points of the presented work can be highlighted as follows.

1) A voltage deviation of the dc-link capacitors is controlled using only the motor phase currents of a three-phase IM load. No auxiliary circuit is employed for this control.

2) If the voltage of the dc-link capacitors reaches their steady-state nominal during the PWM operation, no current is drawn or injected from any NP in the next PWM cycles, to retain the balanced NPs state.

3) Complexity of such control is less even if more dc-link capacitors are added in series across the dc link.

4) The voltage of CHB capacitors is also self-balanced to their nominal value using switching state redundancies. No extra balancing circuits are required for charge balancing of these CHB capacitors.

II. THREE-PHASE NINE-LEVEL INVERTER

The proposed MLI topology with single dc-link with series-connected capacitors as multiple dc sources for the present
study is shown in Fig. 1. Four series-connected capacitors across the dc link are: \( C_t \): the top most dc-link capacitor; \( C_{mt} \): middle top dc-link capacitor; \( C_{mb} \): middle bottom; and \( C_b \): bottom most dc-link capacitor. Three NPs from the terminal joints of these capacitors are: \( O_t \): top NP; \( O_m \): middle NP; and \( O_b \): bottom NP. The modular nine-level inverter of Fig. 1 consists of four basic inverter cells, one five-level stacked inverter, and three CHB inverter cells. The voltage levels only from the stacked inverter are \( V_{dc} \), \( 3V_{dc}/4 \), \( V_{dc}/2 \), \( V_{dc}/4 \), and \( 0 \) with respect to the negative terminal of the dc bus (\( O \)). The stacked inverter can connect a phase terminal to one of these five tapping points on the dc link: PB (positive terminal of the dc bus), \( O_t \), \( O_m \), \( O_b \), or \( O \).

The combination of a five-level stacked inverter and a three level CHB inverter is a nine-level inverter [24], [30]. The nominal voltage of this level booster CHB inverter cell (CHB1 of Fig. 1) is \( V_{dc}/8 \). Hence, the minimum voltage resolution of this nine-level inverter is \( V_{dc}/8 \). For ease of the readers and presentation, the voltage levels \( V_{dc} \), \( 7V_{dc}/8 \), \( 3V_{dc}/4 \), \( 5V_{dc}/8 \), \( V_{dc}/2 \), \( 3V_{dc}/8 \), \( V_{dc}/4 \), \( V_{dc}/8 \), and 0 will also be referred to as levels (L) 8, 7, 6, 5, 4, 3, 2, 1 and 0, respectively, in the following texts, tables, and figures.

The other two CHBs (namely, CHB2 and CHB3) of Fig. 1 with \( V_{dc}/4 \) nominal voltage are the NP balancing CHB. The individual contribution of these inverter cells is \( V_{dc}/4 \), 0, –\( V_{dc}/4 \). These two CHBs help to shift the phase terminals connected to the dc link. The proper placing of a phase terminal on the NPs help to control the voltage of the dc-link capacitors. Individual contributions of all these inverter cells for a pole voltage, the switching states, capacitors charging/discharging, and the clamping diodes conduction status are tabulated in Table 1.

The status for the CHB3 inverter cell is similar to CHB2; the repetition is avoided in the same table. The minimum blocking voltage for the switches is \( 3V_{dc}/4 \): S1, S4; \( V_{dc}/4 \): S1, S2, S7, S8, S9, S10, \( V_{dc}/8 \): S5, S6, and \( V_{dc}/2 \): D1, D2. The level requirement for each phase and PWM information is determined by comparing carrier waves to the reference waves (\( m_A \), \( m_B \), and \( m_C \) for phase A, phase B, and phase C, respectively), as shown in Fig. 2(top). All the pole voltage levels for sector 1

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**TABLE 1. Levels From the Stacked Inverter and CHB Inverter Cells With Their Corresponding Switching States**

| Inverter Section | Level      | Switching States | \( i_A > 0 \) | \( i_A < 0 \) |
|------------------|------------|------------------|---------------|---------------|
|                  | \( v_{PO} \) | S1 S2 S3 S4      | D1            | D2            |
| Stacked Inverter | \( V_{dc} \) | 8 6              | 0 0           | 0 0           |
|                  | \( 3V_{dc}/4 \) | 2              | 0 0           | 0 0           |
|                  | \( V_{dc}/2 \) | 2              | 0 0           | 0 0           |
|                  | \( V_{dc}/4 \) | 2              | 0 0           | 0 0           |
| CHB1 (\( V_{dc}/8 \)) | \( 1 \) | 0 0 0 0 0 0 0 0 | \( \uparrow \) | \( \uparrow \) |
|                  | \( 0 \) | \( \uparrow \) | \( \uparrow \) | \( \uparrow \) |
|                  | \( -1 \) | \( \uparrow \) | \( \uparrow \) | \( \uparrow \) |
| CHB2 (\( V_{dc}/4 \)) | \( 2 \) | \( \uparrow \) | \( \uparrow \) | \( \uparrow \) |
|                  | \( 0 \) | \( \uparrow \) | \( \uparrow \) | \( \uparrow \) |
|                  | \( -2 \) | \( \uparrow \) | \( \uparrow \) | \( \uparrow \) |

Note 1: “\( \uparrow \)” is charging state and “\( \downarrow \)” is discharging state of the capacitor.
Note 2: Switch on-state = “1” and switch off-state = “0”
of space vector region are shown in Fig. 3. Conventionally, the three-digit integer numbers indicate the required inverter pole voltage levels for phases A, B, and C to generate a space vector. For instance, vector location 530 can be achieved when the pole voltage level for phase A is $5V_{dc}/8$, phase B is $3V_{dc}/8$, and phase C is 0. This explanation is valid for all the other vectors in the space vector region.

A pole voltage level of this nine-level inverter in Fig. 1 is the level contribution of each inverter cell (i.e., stacked inverter, CHB1, CHB2, and CHB3). Therefore, the resultant pole voltage level for a phase can be presented as an arithmetic, $v_{AO} = v_{PO} + v_{QP} + v_{RQ} + v_{AR}$. The redundancies for nine pole voltages and different tapping points on the dc link by a phase are tabulated in Table 2. In fact, it is evident from Table 2 that a phase can tap at multiple points on the dc link for a single pole voltage level. For instance, level 2 can be obtained by using R1, R2 (tap from O), R6, R7, R8 (tap from $O_b$), R11, R12 (tap from $O_m$), or R16 (taps from $O_t$). The NP tapping by a phase, inverter switching states, and contribution of pole voltage levels from CHBs for R8 redundancy of level $V_{dc}/4$ is shown in Fig. 4. The pole voltage contributions of the stacked inverter ($v_{PO}$), CHB1 ($v_{QP}$), CHB2 ($v_{RQ}$), and CHB3 ($v_{AR}$) are $V_{dc}/4$, 0, $V_{dc}/4$, and $-V_{dc}/4$, respectively. The selection of proper redundancy for all the phases is crucial to simultaneously achieve the following three controls and implementing a space vector from Fig. 3.

1) Control any unexpected disturbance or deviation on the dc-link capacitors.

2) Ensure that zero instantaneous current is drawn from the NPs during the PWM operation once the dc-link capacitors are balanced to their nominal voltage.

3) Also, balance the voltages of CHB capacitors to their nominal voltage during steady-state PWM operation.

III. INVERTER OPERATION TO VOLTAGE CONTROL THE DC-LINK CAPACITORS AND TO VOLTAGE BALANCE THE CHB CAPACITORS

Equations (1) and (2) tell that for a constant dc-link voltage ($V_{dc}$) if a dc-link capacitor experiences any disturbance and deviates from its nominal voltage, at least one of the remaining capacitors has to compensate for the deviation, i.e., if $C_t$ is undercharged, one of the remaining three capacitors $C_{mt}$, $C_{mb}$, or $C_b$ must be overcharged.

$\frac{d}{dt}(v_{Ct} + v_{Cmt} + v_{Cmb} + v_{Cb}) = V_{dc}$

$\frac{d}{dt}(v_{Ct} + v_{Cmt} + v_{Cmb} + v_{Cb}) = 0$. 

FIGURE 2. Top: Modulating reference and carrier waves for three phase. Bottom: Level requirement for three phases during sector 1.

FIGURE 3. Space vector locations for sector 1 of a nine-level inverter.

FIGURE 4. NP tapping and pole voltage contribution of CHBs explaining R8 redundancy for level $V_{dc}/4$ from Table 2.
At the start of a PWM cycle, the dc-link capacitor can have one of the three voltage conditions: overcharged, undercharged, or within the hysteresis band about its nominal voltage level. Prioritizing control for the dc-link capacitors voltage deviation more than the CHB capacitors voltage deviation, the following two situations arise at the start of a PWM cycle.

1) The voltages of the dc-link capacitors, at least two, are not within their nominal voltage level.
2) All the dc-link capacitors are balanced to their nominal voltage level.

### A. VOLTAGE DEVIATION CONTROL OF DC-LINK CAPACITORS

A dc-link capacitor can either be overcharged or undercharged during an unbalanced condition. Therefore, $2 \times 4$ unbalanced states from the four dc-link capacitors must be addressed to balance all capacitors. However, if the dc-link NPs are considered for voltage control, such unbalanced states are reduced to $2 \times 3$. Therefore, the voltages of the three NPs are considered for the voltage control of the dc-link capacitors. The nominal voltages of the NPs of Fig. 1 are $V_{Ot} = \frac{3V_{dc}}{4}$, $V_{Om} = \frac{V_{dc}}{2}$, and $V_{Ob} = \frac{V_{dc}}{4}$ with respect to $O$ of Fig. 1. The instantaneous voltage deviations of the NPs from the nominal voltages are obtained as follows:

$$\Delta v_{Ot} = v_{Ot} - \frac{3V_{dc}}{4}$$  \hspace{1cm} (3)

$$\Delta v_{Om} = v_{Om} - \frac{2V_{dc}}{4}$$  \hspace{1cm} (4)

$$\Delta v_{Ob} = v_{Ob} - \frac{V_{dc}}{4}$$  \hspace{1cm} (5)

where $v_{Ot}$, $v_{Om}$, and $v_{Ob}$ are the instantaneous voltage errors of the three NPs $O_t$, $O_m$, and $O_b$, respectively, measured with respect to $O$ of Fig. 1 at the start of each PWM cycle.

The combined levels contribution of CHB2 and CHB3 inverter cells in Fig. 1 are +4, +2, 0, −2, or −4. These flexible levels from these two CHBs make it possible to shift the phase terminal tapping on the dc link. Therefore, while generating a space vector from Fig. 3 for low reference amplitude, all the three-phase terminals can connect to any common point on the dc link. Accessing any point on the dc link is possible due to the addition of common-mode voltage while generating the vector. For instance, a space vector $210$ can have multiple alternate vectors: $321$, $432$, $543$, $654$, $765$, and $876$. On the other hand, it is not possible to shift all three phases to the same NP other than $O_m$ for a space vector with high reference amplitude. Only the access of $O_m$ is likely due to maximum...
and minimum combined level contributions of CHB2 and CHB3 of each phase being +4 and -4. The control action is thereby divided into the following two separate cases:

1) \textit{CASE—MAX}(L_A, L_B, L_C) > 4

2) \textit{CASE—MAX}(L_A, L_B, L_C) ≤ 4

where \( L_x \) (\( x = A, B, \) or \( C \)) is the level required of the phases for a reference vector from Fig. 3.

1) \textbf{CASE—MAX}(L_A, L_B, L_C) > 4

For high space vector references from sector 1, phase A taps PB or \( O_t \) (zone 1), phase C taps \( O_t \) or \( O_m \) (zone 2), and phase B tapping changes from O to PB (zone 1 to zone 3), as shown in Fig. 2(bottom). Phase terminal positions on the dc link will interchange for the vectors of the other sectors. The possible combinations of tapping on the dc link by the phases are shown in Fig. 5(a) to (h). Irrespective of connections from the phase terminals (A, B, and C) on the dc link, the currents are renamed as \( i_t \) for the top NP connected phase, \( i_m \) for the middle NP connected phase, and \( i_b \) for the bottom NP connected phase. It is certain that for a three-phase system, \( i_t + i_m + i_b = i_A + i_B + i_C = 0 \).

Let the controller triggers an overvoltage(undervoltage) state for \( O_t \), which requires \( C_t \) to be discharged(charged) to balance \( O_t \). Fig. 5(a)–(c) shows the configurations for \( O_t \) disturbance control using the phase current. The branch currents for Fig. 5(a) are obtained by solving (6), (7), \( i_1 = \frac{3i_m}{4} \), and \( i_2 = -\frac{i_m}{4} \).

\[
i_1 = C \frac{d}{dt} (v_{Cm}) = I_{dc} + i_b
\]
\[
i_2 = -\frac{C}{3} \frac{d}{dt} (v_{Ct}) = I_{dc} + i_b.
\] (7)

The time required to charge(discharge) \( C_t \) can be found using the following equation for the configuration of Fig. 5(a):

\[
\Delta T = C \frac{\Delta V_{Ot}}{3I_m/4}
\] (8)

where \( \Delta V_{Ot} \) is obtained from (3). The instantaneous current \( I_m \) and instantaneous voltage error for the top NP of the dc link \( (\Delta V_{Ot}) \) are both sensed at the start of the PWM operation. Finally, \( \Delta T \) is calculated from the known capacitance value of the dc-link capacitors. Similarly, branch currents \( i_1 \) and \( i_2 \) are also found for \( O_m \) and \( O_b \) with balancing configurations in Fig. 5(d)–(g), respectively. Fig. 5(h) configuration is preferred in the absence of suitable redundancy for NP voltage control, i.e., the voltages of the NPs are undisturbed.

The procedure to control of overcharged \( O_t \) is explained for a random space vector location, \( \overline{V} = 720 \), from Fig. 3. The details are presented in Table 3. There are six current conditions from the phase currents, as tabulated in Table 3.

If the phase current polarity is positive, then it is allowed to tap from \( O_t \) to discharge the NP; hence, the phase currents control the voltages of dc-link capacitors. If the phase currents polarity and the level information are not suitable to discharge \( O_t \), the phase terminals are sent to the dc buses (PB or O). While altering the phase terminals on the dc link, it is ensured by the CHB2 and CHB3 level contributions that the final pole voltage level is the required pole voltage during that PWM operation.

2) \textbf{CASE—MAX}(L_A, L_B, L_C) ≤ 4

As mentioned earlier, it is possible to shift the phase terminals and tap all the NPs for a space vector with low reference amplitude. This is possible using common-mode voltage addition and levels from CHB2 and CHB3 inverter cells. The possible circuit configurations are shown in Fig. 6(a)–(h). The branch currents for Fig. 6(a) \( i_1 = \frac{3i_m}{4} \), \( i_2 = -\frac{i_m}{4} \), are calculated by solving (9) and (10).

\[
i_1 = C \frac{d}{dt} (v_{Ct}) = I_{dc} + i_b
\]
\[
i_2 = -\frac{C}{3} \frac{d}{dt} (v_{Cm} + v_{Cmb} + v_{Cb})
\] (9)
\[
= -\frac{C}{3} \frac{d}{dt} (v_{Ct}) = I_{dc}
\] (10)

The time required to control \( O_t \) can be found using (11) for the configuration of Fig. 6(a).

\[
\Delta T = C \frac{\Delta V_{Ot}}{3I_m/4}.
\] (11)
TABLE 3. Tapping Point on the DC Link by the Phase Terminals When \( O_t \) is Overcharged

| Level | Phase Current Status | The phase terminals tapping point on the dc link | Final Vector \((L_A, L_B, L_C)\) | Circuit Type |
|-------|----------------------|-----------------------------------------------|-------------------------------|-------------|
| 720   | \( i_A > 0, i_B < 0, i_C < 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(b) |
|       | \( i_A < 0, i_B > 0, i_C < 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(a) |
|       | \( i_A < 0, i_B < 0, i_C < 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(b) |
|       | \( i_A > 0, i_B < 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(h) |
|       | \( i_A < 0, i_B > 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(h) |
|       | \( i_A > 0, i_B < 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 5(h) |
| 210   | \( i_A > 0, i_B < 0, i_C < 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 6(a) |
|       | \( i_A < 0, i_B > 0, i_C < 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 6(b) |
|       | \( i_A < 0, i_B < 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 6(b) |
|       | \( i_A > 0, i_B < 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 6(b) |
|       | \( i_A < 0, i_B > 0, i_C > 0 \) | \( L_A = 7 \) | \( L_B = 7, L_C = 0 \) | 720 Fig. 6(b) |

Note: \( L_A, L_B, \) and \( L_C \) are the levels for phase A, phase B, and phase C, respectively.

are both sensed and calculated at the start of the PWM operation. It is also possible to find branch currents for other configurations, as shown in Fig. 6(b)–(h). The configurations in Fig. 6(a) and (b) are for \( O_t \) control, and Fig. 6(c)–(f) are \( O_m \) control configurations, and Fig. 6(g) and (h) are \( O_b \) control configurations.

Another random space vector location, \( \vec{V} = 210 \), is chosen to explain the control of overcharged \( O_t \). The details are tabulated in Table 3. A common-mode voltage level 4 or 6 is added to \( \vec{V} \) to control \( O_t \), utilizing the phase current polarity. The phase terminals are shifted on the dc link based on the current polarity. This terminal shifting utilizes the levels from CHB2 and CHB3 inverter cells.

B. ALL THE DC-LINK CAPACITORS ARE BALANCED TO THEIR NOMINAL VOLTAGE REFERENCE LEVEL

If the voltages of the dc-link capacitors are within the nominal range, retaining the balanced state during the PWM operation is crucial. Therefore, the following conditions need to be ensured while generating a space vector.
TABLE 4. CHB Capacitor Voltage Balancing for Space Vector Location 410 From Fig. 3

| SL | Preferred phase and capacitor status | Redundancies form Table 2 for other phases | DC-link Tapping | Final Vector |
|----|-------------------------------------|------------------------------------------|----------------|-------------|
|    | Level A (L_A)                       | Level B (L_B)                            | Level C (L_C)  |             |
| 1  | L5 = 0+1+2+2                        | L2 = R1/R2                               | L0 = R1/R2/R3  | 520          |
| 2  | L5 = 8+1-2-2                        |                                          |                | 520          |
| 3  | L7 = 8+1-2+0                        | L4 = R1/R21                              | L2 = R1/R2     | 742          |
| 4  | L7 = 8+1+0-2                        |                                          |                | 742          |
| 5  | L7 = 8-1+2-2                        | L4 = R1/R21                              | L2 = R1/R2     | 742          |
| 6  | L7 = 8-1-2+2                        |                                          |                | 742          |
| 7  | L5 = 2-1+2+2                        | L2 = R6/R7/R8                           | L0 = R6/R7     | 520          |
| 8  | L7 = 8-1-2+0                        |                                          |                | 520          |
| 9  | L7 = 8-1+0-2                        |                                          |                | 520          |

Note: “−” = no effect, “↑” = Charging and “↓” = Discharging of the CHB capacitors, assuming positive phase current into the motor.

1) Bring all three phases to a single NP for \( i_A + i_B + i_C = 0 \).

2) If it is not possible to bring all phases to a single NP, shift the phase terminals to the dc buses (PB or O) to avoid tapping by any phase terminal.

In a PWM cycle, let \( d_1 \) to \( d_6 \) are the duty ratios of the switches \( S_1 \) to \( S_6 \) of Fig. 1. From Table 2, if the pole voltage level requirement in a PWM cycle is odd, the CHB1 inverter cell contributes either +1 or −1 level, and \( d_5 \) · \( d_6 \) (logical AND operation) = 1 when the level from CHB1 is −1. Now, \( d_1 \) to \( d_4 \) of the stacked inverter switches are:

\[
d_{1X} = 1 \quad \text{when} \quad m_X > 0.875
\]
\[
d_{2X} = 1 \quad \text{when} \quad m_X > 0.625
\]
\[
d_{3X} = 1 \quad \text{when} \quad m_X > 0.5
\]
\[
d_{4X} = 1 \quad \text{when} \quad m_X > 0.25
\]

where \( X = A, B, \) or \( C \) phases. The NP tapping by each phase is \( d_{XOt}, d_{XOm}, \) and \( d_{XOb} \) and can be obtained, respectively, from the following equations:

\[
d_{XOt} = d_{3X} \cdot \overline{d_{4X}} \quad (16)
\]
\[
d_{XOm} = d_{4X} \cdot \overline{d_{3X}} \quad (17)
\]
\[
d_{XOb} = d_{2X} \cdot \overline{d_{4X}}. \quad (18)
\]

The current drawn from the NPs is \( i_{Ot}, i_{Om}, \) and \( i_{Ob}, \) and these are found, respectively, using the following equations:

\[
i_{Ot} = i_{AOt} + i_{BOt} + i_{COt}
\]
\[
i_{Om} = i_{AOM} + i_{BOM} + i_{COM}
\]
\[
i_{Ob} = i_{AOb} + i_{BOb} + i_{COb}
\]

The flexible level contributions of CHB2 and CHB3 inverter cells make it possible to equalize the duty ratios on each NPs. Certainly, the instantaneous current at \( O \) \( (i_{Ob}) \) is always zero for \( d_{AOb} = d_{BOb} = d_{COb} = d_{Ot} \). Thus, zero instantaneous currents are drawn from all the three NPs of the dc link.
FIGURE 8. Photograph of the experimental setup. (a) Four series-connected dc-link capacitors. (b) Stacked inverters with SKM75GB123D IGBTs and gate drivers. (c) Current sensor board. (d) and (e) CHB capacitors and inverters with IRF260 N MOSFETs and gate drivers. (f) Voltage sensor board. (g) DSP- and FPGA-based digital controllers. (h) Three-phase IM.

FIGURE 9. Block diagram of the control and experimental setup.

C. COMPLETE CONTROL ALGORITHM FOR VOLTAGE DEVIATION CONTROL OF DC-LINK CAPACITORS AND VOLTAGE BALANCING OF CHB CAPACITORS

Voltage deviation control of the dc-link capacitors and voltage balancing of the CHB capacitors are illustrated with the help of a flowchart in Fig. 7. The level and PWM information are calculated from the user speed reference input. The dc-link capacitors voltages, capacitor voltages of CHBs, and the phase currents polarity are sensed at the start of the PWM cycle. The switching states are selected from the lookup tables (LUTs) based on whether the NPs are balanced or not.

At the start of a PWM cycle, \(2 \times 3 \times 3 = 18\) (undercharged or overcharged status of three CHBs of three phases) voltage statuses are determined from the sensed voltage. Attending all CHB capacitors for balancing in a single PWM instant makes the control action difficult. A cycle of phases (A -> B -> C -> A and so on) is thereby altered among the three phases during the steady state of PWM operation.

If the dc-link NPs are not balanced, the phases are placed on the dc link such that it charges/discharges an NP based on the phase currents polarity. Less priority is given to the voltage balancing of CHB capacitors while controlling the voltage of dc-link capacitors. Therefore, an alternative cycle of phase and NPs \((O_t \rightarrow A \rightarrow B \rightarrow C \rightarrow O_t \rightarrow A \rightarrow B \rightarrow C \rightarrow O_t \text{ and so on})\) is followed for NP balancing. This cycle also checks that CHB capacitors do not deviate much from their nominal voltage. It should be noted that a change in LUT (from the NP balancing LUT to the other LUT) for the switching state is required during the PWM interval once the NPs reach their steady-state nominal voltages. The charging/discharging time is found using (8) and (11) at the

| Parameters                              | Value       |
|-----------------------------------------|-------------|
| DSP clock cycle time                   | 6.67 nS     |
| FPGA clock cycle time                  | 20 nS       |
| PWM switching frequency                | 2 kHz (approximately) |

| Digital Controllers | Name       |
|---------------------|------------|
| DSP                 | TMS320F28335 |
| FPGA                | Xilinx Spartan 3 XC3S400 |

| Capacitors       | Value         |
|------------------|---------------|
| C1A, C1B, and C1C| 4.7 mF, 200V  |
| C2A, C2B, and C2C| 2.2 mF, 200 V |
| C3A, C3B, and C3C| 2.2 mF, 200 V |
| C1, C\text{cm}, C_m, and C_b   | 3.3 mF, 200 V |

| Switches | Type               |
|----------|--------------------|
| S1/S6 to S4   | IGBT (SKM75GB123D) |
| S5/S8 to S10/10 | MOSFET (IRF260N)  |

TABLE 6. THD of Phase Voltage at Different Fundamental Frequencies

| Fundamental frequency | Samples per cycle | THD [%] |
|-----------------------|-------------------|--------|
| 10 Hz                 | 120               | 34.51  |
| 15 Hz                 | 120               | 25.47  |
| 20 Hz                 | 72                | 17.90  |
| 25 Hz                 | 72                | 13.74  |
| 30 Hz                 | 60                | 11.52  |
| 35 Hz                 | 45                | 11.24  |
| 40 Hz                 | 45                | 9.60   |
| 45 Hz                 | 40                | 8.13   |

TABLE 7. Parameters of the Induction Motor Under Experiment

| Parameters                           | Value |
|--------------------------------------|-------|
| Number of pole                       | 4     |
| Stator resistance, \(R_s\)           | 1.0 \(\Omega\) |
| Rotor resistance, \(R_r\)             | 1.932 \(\Omega\) |
| Stator leakage inductance, \(L_{1s}\) | 9.13 mH |
| Rotor leakage inductance, \(L_{1r}\)  | 9.13 mH |
| Magnetising inductance, \(L_m\)      | 260.0 mH |
| Mechanical time constant, \(J/\omega^2\) | 18 s  |

TABLE 5. Details of Components and Parameters Used for the Inverter and the Controller
beginning of PWM and is utilized for the change in LUT. If, $T_{\text{charge}}/T_{\text{discharge}} > T_{\text{PWM}}$ ($T_{\text{PWM}}$: time for a PWM cycle, see Fig. 2), the switching state will be chosen from the NP balancing LUT. If a phase is preferred, or voltages of the dc-link capacitors reach their nominal during the PWM, the switching state LUT is changed from the NP balancing LUT to the other LUT for instantaneous zero NP current.

1) CAPACITOR VOLTAGE BALANCING OF CHBs
The voltages of CHB capacitors are balanced using the same set of redundancies from Table 2. Capacitors voltage balancing for CHBs is demonstrated for a space vector $\overrightarrow{V}_1 = 520$, located in the triangle with vertices (420, 520, 530) of Fig. 2(b). Table 4 presents the CHB capacitor voltage balancing and redundancies of other two phases while keeping all the phases to a single NP or shifting the phases to the dc bus terminals. The common-mode voltages are added to the vector $\overrightarrow{V}_1$, which generates a redundant space vector 742. When a phase is preferred from the cycle A -> B -> C -> A, other phases are forced to satisfy the conditions from Section III-B during the steady state. This forcing to shift the other phases to a single NP is possible due to level contributions from CHB2 and CHB3 inverter cells. The balancing action with phase preferences is as follows.

1) Phase A: vectors with serial 1 to 9 are implemented to balance all CHB capacitors ($C_{1A}$, $C_{2A}$, and $C_{3A}$) of phase A.
2) Phase B: vectors with serial 10 to 13 are implemented to balance $C_{2B}$ and $C_{3B}$ capacitors, and $C_{1B}$ capacitor is undisturbed.
3) Phase C: vectors with serial 14 to 19 are implemented to balance $C_{2C}$ and $C_{3C}$ capacitors, and $C_{1C}$ capacitor is undisturbed.

IV. EXPERIMENTAL SETUP
The photograph of the lab prototype and block diagram of the experimental setup are shown in Figs. 8 and 9, respectively. The control algorithm of Fig. 7 is implemented using a digital signal processor (DSP) (TMS320F28335) and a field-programmable gate array (FPGA) (Xilinx Spartan 3 XC3S400) controller boards. DC-link, CHB capacitors voltage, and phase currents are sensed using the build-in ADC block of the DSP. The PWM and level information are

![FIGURE 10. Waveforms of the phase voltage, pole voltage, phase current, and voltage of the CHB capacitors at 45 Hz and 10 Hz under $V/f$ control. Steady-state waveforms in (a) and (c) for LPF load condition, and in (b) and (d) for UPF load conditions. Traces: (1) Motor phase voltage ($v_{AN}$), (2) inverter pole voltage ($v_{AO}$), (3) motor phase current ($i_A$). (e) Harmonic spectrum of the phase voltage with respect to fundamental phase voltage at 45 Hz.](image1)

![FIGURE 11. Independent discharging/charging of CHB capacitors. Traces: (1) Motor phase voltage ($v_{AN}$), (2) Voltage across CHB3 capacitor ($v_{C3A}$), (3) Voltage across CHB2 capacitor ($v_{C2A}$), (4) Voltage across CHB1 capacitor ($v_{C1A}$), and (5) Motor phase current ($i_A$). (a) 45 Hz, LPF.](image2)
calculated in the DSP for open-loop V/f control and field-oriented control (FOC). The level and PWM information, current status, and capacitors voltage status information are passed to the FPGA controller for proper switching signals. The right switching signals are decoded from the stored LUT of FPGA. The dead-time delay (OFF delay to ON delay) is kept at 1 μs. Approximately, 2 kHz switching frequency is ensured for the entire frequency of operation. The rotor speed feedback ($\omega_{m}$) for the closed-loop control is obtained from a shaft-mounted encoder.
FIG. 14. Waveforms of the voltages across dc-link capacitors, currents, and voltages at the NPs of Fig. 1 during O_m (a) overcharged and (b) undercharged. (a), (b) Currents from three dc-link NPs and voltage across four dc-link capacitor. Traces: (1) Voltage at O_m (v_m), (2) current from O_t (i_{Ot}), (3) current from O_m (i_{Om}), (4) voltage across C_t (v_{Ct}), (5) voltage across C_{mt} (v_{Cmt}), (6) voltage across C_{mb} (v_{Cmb}), (7) voltage across C_b (v_{Cb}). (c), (d) Voltage at the dc-link NPs with respect to negative terminal of the dc bus. Traces: (1) Voltage at O_t (v_{Ot}), (2) voltage at O_m (v_{Om}), (3) voltage at O_b (v_{Ob}), and (4) motor phase current (i_{A}). (a) O_m : Overcharged. (100 ms/div). (b) O_m : Undercharged. (100 ms/div). (c) O_m : Overcharged. (5 s/div). (d) O_m : Undercharged. (5 s/div).

FIG. 15. Waveforms for the speed reversal of the motor from −30 Hz to +30 Hz under FOC. Traces: (1) Motor phase voltage, (v_{An}), (2) motor speed feedback (\omega_m), (3) motor magnetizing current (i_{mr}), (4) motor torque producing component (i_{sq}), and (5) motor phase current (i_{A}).

To maintain ± 5% voltage ripple at 10 A peak phase current, the capacitor values can be calculated by 
\[
C = \frac{I_p \cdot 3/\Delta V}{T_{PWM}}
\]
where \(I_p\) is the peak phase current, \(T_{PWM}\) is the PWM interval, and \(\Delta V\) is the allowable voltage ripple. As discussed in an earlier section, the voltage balancing of CHB capacitors is preferred like A \rightarrow B \rightarrow C \rightarrow A and so on during the steady state. Therefore, three worst-case delays of the sampling interval (\(T_{PWM}\)) are considered for capacitor design. In this work, 4.7 mF, 200 V capacitors for CHB1, 2.2 mF, 200 V for CHB2 and CHB3 capacitors, 3.3 mF, 200 V for dc-link capacitors, SKM75GB123D IGBTs for the stacked inverter, and IRF260 N MOSFET switches for the CHB inverter cells are chosen from the off-the-shelf devices to realize this nine-level inverter. A standard design procedure for dc-link capacitors is followed for the grid-connected bridge rectifier and can be optimized for constant dc sources. The list of components is also tabulated in Table 5.

V. EXPERIMENTAL RESULTS

The dc-link voltage deviation control algorithm is verified at low power-factor (LPF) and unity power-factor (UPF) conditions. A three-phase IM at no-load and a resistive load is used to demonstrate the effectiveness of the proposed control. Only two set of frequencies are presented in Fig. 10: 10 and 45 Hz. These frequencies also represent low and high modulation indices under \(V/f\) operation. Fig. 10 shows the steady-state results under \(V/f\) operation for the inverter pole voltage, CHB capacitors voltage, phase voltage, and phase currents. The traces (1)–(3) (phase voltage, pole voltage, and phase current, respectively) in Fig. 10(a) and (b) are results at 45 Hz and in Fig. 10(b) and (d) are results at 10 Hz at two power-factor conditions.

The pole voltage asymmetry during the low-speed operation is due to the voltage contribution of CHB2 and CHB3 to the pole voltages to bring all the three phases to a single NP or dc bus terminals, as explained in Section III-B. Although the pole voltages are asymmetric, the phase voltages are sinusoidal as conventional MLIs, but nine voltage levels of pole voltage during the PWM operation are evident in the zoomed view of 45 Hz result with UPF load. The harmonic content in phase voltage at 45 Hz is presented in Fig. 10(e).
The major harmonics appear around the 40th harmonic of the fundamental frequency. This spectrum confirms that the switching frequency for this fundamental frequency is 1.8 kHz (near to 2 kHz). The total harmonic distortion (THD) of phase voltage at different fundamental frequencies under V/f control is tabulated in Table 6.

The experimental result presented in Fig. 11 is aimed to show the voltage regulation capability of the CHB capacitors by the control technique. The voltages of the CHB capacitors are regulated independently using the switching state redundancies. Reference voltages of the CHB capacitors are changed intentionally during the PWM operation. Moreover, the voltages of the CHB capacitors are self-balanced to their nominal during the steady state of the PWM operation. Traces (2), (3), and (4) of Fig. 11 show the voltage of the CHB capacitors of CHB3, CHB2, and CHB1, respectively.

The experimental results for forced unbalancing of the dc-link NPs are shown in Figs. 12 and 13. Fig. 12 shows the LPF operation result, and Fig. 13 shows the result for the UPF operation. Each NP (\(O_t\), \(O_m\), and \(O_b\)) is externally overcharged and undercharged. Traces (2), (3), and (4) of Figs. 12 and 13 show that the voltages of the NPs have returned to their nominal voltages very quickly. After that, the NPs maintain the nominal voltage by drawing zero instantaneous current from the NPs.

The claim of zero instantaneous currents drawn from the balanced NPs is evident from the results shown in Fig. 14(a) and (b). Intentional overcharging and undercharging of \(O_m\) are repeated in this experiment. The traces (2), (3), and (4) of Fig. 14(a) and (b) show the NPs currents drawn from \(O_t\), \(O_m\), and \(O_b\), respectively, during the steady state and transient. Observe that the glitches on the NPs currents are only present during the unbalanced dc-link capacitor voltage conditions. No NP current is drawn from an NP once the voltage of the dc-link capacitors reaches their steady-state nominal voltage reference. The steady-state reference voltage is calculated from the total dc-link voltage. The voltage across each dc-link capacitor (\(C_t\), \(C_m\), \(C_{mb}\), and \(C_b\)) is presented in the traces (6), (7), (8), and (9) of Fig. 14(a) and (b). More interesting results are presented in Fig. 14(c) and (d), which validate the overall performance of the proposed technique. Here, intentional \(O_m\) disturbance is repeated, and the dc-link capacitors are allowed to balance only using the 15 kΩ bleeder resistors across each dc-link capacitor. A comparison of NP voltage among Fig. 14(a), (b), and (c) reveals that the time required for dc-link capacitor voltage control with bleeder resistor control is considerably higher than the time needed for the control algorithm. Therefore, fast balancing is achieved without implementing any extra balancing circuit and only using the phase currents of a three-phase load. Once the dc-link capacitors are balanced, instantaneous balancing is followed after that.

The dynamic performance of the control algorithm is tested with rotor FOC of the induction motor. The experiments are carried out on a 7.5 kW, 415 V, 50 Hz IM. The control technique is tested under an open-loop V/f control and closed-loop FOC. The parameters of the IM are tabulated in Table 7. Three standard PI controllers (speed controller (\(\omega_c\) control), flux controller (\(I_{sd}\) control), and torque controller (\(I_{sq}\) control) have been implemented for the FOC. The experimental results for −30 Hz to +30 Hz speed reversal are presented in Figs. 15 and 16. The traces (2), (3), and (4) of Fig. 15 show the speed feedback (\(\omega_m\)), magnetizing component (\(I_{mr}\)), and torque producing component (\(I_{sq}\)) of the stator current. During the entire speed transition, \(I_{sq}\) changes, but \(I_{mr}\) is constant, which indicates that the decoupled control is achieved on the induction motor under experiment.

The objective of the control action is that if the dc-link capacitors’ voltages are already balanced, avoid disturbing them by ensuring zero instantaneous currents at the NPs. Fig. 16(a) results affirm that even during the fast transient, no NP currents are drawn from \(O_t\), \(O_m\), and \(O_b\). The NP currents can be seen from the traces (1), (2), and (3) of Fig. 16(a). Therefore, the dc-link NPs voltage for \(O_t\), \(O_m\), and \(O_b\) are strictly maintained to their nominal voltage during the whole speed reversal action, as shown in traces (1), (2), and (3) of Fig. 16(b). A diode bridge rectifier circuit is used at the front-end side of the inverter to power the dc-link capacitors. The minute disturbance in dc-link NP voltages is due to the sudden high current demand and the corresponding increase in rectifier side voltage drop. This disturbance is also reflected
in the CHB capacitors’ voltage since the voltages of CHB capacitors strictly follow the nominal voltage references. The voltage references for CHB capacitors voltage are derived from the total dc-link voltage. The traces (1), (2), and (3) of Fig. 16(c) show the voltages of the CHB capacitors during the speed transition.

VI. CONCLUSION

For the first time in the literature, this article proposes a technique for voltage control of the series-connected dc-link capacitors using the motor phase currents of a three-phase IM. The following points can be summarized for the proposed technique.

1) The voltage deviation control for the dc-link capacitors is possible using the load phase currents and pole voltage redundancies. This control is tested by intentional deviation to all the dc-link NP's from their nominal voltage.
2) Once the voltages of the dc-link capacitors are restored to their nominal voltage reference, instantaneous zero currents are drawn from the NPs to retain the balanced state of the dc-link NPs.
3) Simultaneously, voltages of the CHB capacitors are also regulated by the same inverter pole voltage redundancies.
4) The performance of the balancing technique remains the same even during the fast dynamic condition, which is tested with FOC of an IM.
5) This balancing scheme is independent of the load power factor and modulation indices.
6) The nine-level inverter can be built using low-voltage devices. The voltage stress for most of the switches is rated less than or equal to one-fourth of the dc-link voltage.

The other advantages of this voltage control technique of NPs are: 1) a single dc link at the source makes the topology suitable for four-quadrant medium-voltage motor drive applications; 2) low-voltage series-connected dc-link capacitors can be replaced by battery cells for EV applications; 3) inherent voltage control of the batteries is possible using the switching state redundancies and the load phase currents, and no external circuit is required for voltage balancing of these battery cells. Moreover, the proposed balancing technique is general in nature and more dc-link series capacitors can be added to extend the level for MLI, which can be realized using low-voltage switching devices.

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