Abstract—This work presents an algorithm to generate depth, quantum gate and qubit optimized circuits for $GF(2^n)$ squaring in the polynomial basis. Further, to the best of our knowledge the proposed quantum squaring circuit algorithm is the only work that considers depth as a metric to be optimized. We compared circuits generated by our proposed algorithm against the state of the art and determine that they require 50% fewer qubits and offer gates savings that range from 37% to 68%. Further, existing quantum exponentiation are based on either modular or integer arithmetic. However, Galois arithmetic is a useful tool to design resource efficient quantum exponentiation circuit applicable in quantum cryptanalysis. Therefore, we present the quantum circuit implementation of Galois field squaring based on the proposed quantum Galois field squaring circuit. We calculated a qubit savings ranging between 44% to 50% and quantum gate savings ranging between 37% to 68% compared to identical quantum exponentiation circuit based on existing squaring circuits.

Index Terms—quantum computing; Galois field arithmetic;

I. INTRODUCTION

Among the emerging computing paradigms, quantum computing appears to be promising due to its applications in number theory, cryptography, search and scientific computation [1] [2]. Quantum computing is also being investigated for its promising application in high performance computing [1] [2]. Quantum circuits do not lose information during computation and quantum computation can only be performed when the system consists of quantum gates. Quantum circuits generate a unique output vector for each input vector, that is, there is a one-to-one mapping between the input and output vectors. Any constant inputs in the quantum circuit are called ancillae and garbage output refers to any output which exists in the quantum circuit to preserve one-to-one mapping but is not one of the primary inputs nor a useful output. The inputs regenerated at the outputs are not considered garbage outputs [3].

Fault tolerant implementation of quantum circuits is gaining the attention of researchers because physical quantum computers are prone to noise errors [2]. Fault tolerant implementations of quantum gates and quantum error correcting codes can be used to overcome the limits imposed by noise errors in implementing quantum computing [2]. Recently, researchers have implemented quantum logic gates and circuits such as the controlled phase gate, controlled square-root-of-not gate, Toffoli gate, Fredkin gate and quantum full adders with the fault tolerant Clifford+T gate set due to its demonstrated tolerance to noise errors [3].

A Galois field is a set that possesses a particular set of mathematical properties. Galois fields and Galois field arithmetic have drawn interest of many researchers because of its applications in encryption, error correcting codes and signal processing [3] [4]. Galois field squaring has drawn interest because it is a lower cost alternative to multiplication when both operands are the same. There are existing designs of quantum circuits for Galois field squaring such as the designs in [7]. The Galois field squaring designs in [7] are 2 input and 2 output circuits. They have the mapping $(A, B)$ to $(A, A^2 + B)$. To implement $A^2$, $B$ is replaced by ancillae. In a quantum circuit, the ancillae and garbage outputs are considered overhead and need to be minimized. This is because an increase in number of ancillae inputs and garbage outputs will increase the number of qubits in the quantum circuit. Therefore, in applications that require repeated squaring operations such as Galois field exponentiation, the use of the existing quantum squaring circuit design in [7] will result in significant ancillae overhead.

In this work we present an algorithm to realize depth, qubit and quantum gate optimized circuits for Galois field squaring. Further, to the best of our knowledge the proposed quantum squaring circuit algorithm is the only work that considers depth as a metric to be optimized. In this work, depth is defined as the number of parallel sets of quantum gates in a circuit. Quantum gates that operate on independent sets of qubits are considered parallel. The quantum Galois field squaring circuits are based on the Feynman gate. The Feynman gate is a member of the fault tolerant Clifford+T gate set [2]. The quantum squaring circuit based on our proposed algorithm is compared and is shown to be better than the existing design of quantum Galois field squaring circuits in [7]. The comparison is performed in terms of number of gates and qubits.

Further, existing quantum exponentiation are based on either modular or integer arithmetic. However, quantum exponentiation based on Galois arithmetic is applicable in quantum cryptanalysis [1]. Therefore, we present the quantum circuit implementation of Galois field exponentiation based on the proposed quantum Galois field squaring circuit. We calculated
a significant qubit and quantum gate savings compared to identical quantum exponentiation circuit based on existing squaring circuit in [7].

The paper is organized as follows: the basics of Galois fields is presented in section II, the proposed Galois field squaring circuit algorithm and analysis are presented in sections III and IV. The proposed Galois field exponentiation circuit algorithm and analysis are presented in sections V, VI and VII while sections V, VI and VIII provide the comparison of the Galois field squaring circuits, Galois field exponentiation circuits and conclusions, respectively.

II. BASICS OF GALOIS FIELDS

A Galois field is a set that possesses a particular set of mathematical properties. The number of elements in the field is determined by the field basis \( f(x) \). In our work, we represent \( f(x) \) with irreducible polynomials. The set of elements in the Galois field will contain all possible polynomials that are less than the basis \( f(x) \). A field element is given as:

\[
\alpha_{m-1} \cdot x^{m-1} + \alpha_{m-2} \cdot x^{m-2} + \cdots + \alpha_1 \cdot x + \alpha_0
\]

Where \( \alpha \in GF(2) \) and \( \{0, 1\} \in GF(2) \).

Galois field applications make use of the Galois field addition, multiplication and exponentiation operations. Next, we discuss these important Galois field arithmetic operations.

A. Galois field arithmetic

Addition in Galois fields is the bit-wise exclusive-OR (XOR) operation. In quantum computing, the bit-wise XOR operation is implemented with the Feynman gate. Figure 1 shows the schematic symbol of the Feynman gate.

Multiplication in Galois fields evaluates the following equation:

\[
Y = A \cdot B \mod f(x)
\]

Where \( f(x) \) is the field basis and \( A, B \in GF(2^m) \). In the most straight-forward implementation, partial products are produced with the AND operation. All addition is Galois and it along with the reduction modulo \( f(x) \) is performed with the XOR operation. In quantum computing, the AND operation is implemented with the Toffoli gate. Figure 1 shows the schematic symbol of the Toffoli gate.

Squaring is a special case of multiplication where both operands are the same. Squaring in Galois fields evaluates the following equation [5]:

\[
A^2 = \sum_{i=0}^{n-1} \alpha_i \cdot x^{2i} \mod f(x)
\]

Where \( n \) is the order of the field basis \( f(x) \) and \( A \in GF(2^m) \). Equation 3 is implemented in hardware with the XOR operation.

Exponentiation is performed with repeated applications of the Galois field squaring and Galois field multiplication operations. In our work, we are interested in quantum circuits that realize the following exponential equation:

\[
Y = A^{2^n-2} \mod f(x)
\]

Where \( n \) is the order of the field basis \( f(x) \) and \( A \in GF(2^m) \). Equation 4 has drawn interest of researchers because equation 4 is an implementation of the Galois field inversion operation [8]. The literature shows that polynomial basis implementations of equation 4 can excel against alternative Galois field basis representations in terms of total bit operations [8].

III. PROPOSED GALOIS FIELD QUANTUM SQUARING ALGORITHM

The quantum Galois field squaring circuit is designed with less qubit and quantum gate cost compared to existing Galois field squaring circuit design approaches [7]. Further, the proposed algorithm includes circuit depth as an optimization criterion. Consider the squaring of one \( n \) bit field number \( A \) stored at quantum register \( |A\rangle \). At the end of the computation, the quantum register \( |A\rangle \) will have \( |Y\rangle \) (where \( Y = A^2 \mod f(x) \) and \( f(x) \) is the field basis).

The generalized algorithm of designing a Galois field squaring circuit is explained below along with an illustrative example in figure 2 of a Galois field squaring circuit for a field of size 10 defined with basis \( f(x) = x^{10} + x^3 + 1 \) that can perform the squaring of any field element. Details of the proposed algorithm are discussed below:

A. Steps of Proposed Algorithm for Galois Field Squaring Circuits

- Step 1: For \( i = 0 : 1 : n - 1 \): Evaluate the following:

\[
\alpha_i \cdot x^{2^i} \mod f(x)
\]

If equation 5 equals \( \alpha_i \cdot x^{2^i} \), then at the end of computation the qubit \( |\alpha_i\rangle \) will have the value \( |Y_{2^i}\rangle \). Else, equation 5 equals the following:

\[
B_{n-1} \cdot x^{n-1} + B_{n-2} \cdot x^{n-2} + \cdots + B_1 \cdot x + B_0
\]

Where \( B_j \in 0, 1 \) and \( 0 \leq j \leq n - 1 \). At the end of computation the qubit \( |\alpha_i\rangle \) will have the value \( |Y_j\rangle \) provided \( B_j = 1 \) and \( |Y_j\rangle \) is not already assigned to another qubit in \( |A\rangle \).

Thus, the values in \( |Y\rangle \) will not be in sequential order but the generated squaring circuits will require no ancillae. The
Proposed Quantum GF(2) squaring algorithm

Step 1:
- Assign output indices to qubits
- Place Feynman Gates
- Optimize for Depth

Step 2:
- Step 1: select a gate as a reference gate
- Step 2: If a gate shares a qubit with reference gate, move it to the end of the circuit
- Step 3: If more than 1 gate is moved then repeat Steps 1 and 2 with only the moved gates

Theorem: Let \( A \) be a \( n \) bit binary number and \( A \in GF(2^n) \), then the steps in the proposed Galois field squaring circuit algorithm results in a quantum Galois field squaring circuit that functions correctly. The proposed algorithm designs an \( n \) bit Galois field squaring circuit that produces the output \( A^2 \) on the quantum register where \( A \) is originally stored.

Proof: The proposed algorithm will make the following changes on the input:

- Step 1: Step 1 of the proposed algorithm transforms the input states to
  \[
  \left\{ \sum_{i=0}^{\lfloor \frac{n-1}{2} \rfloor} A_i \cdot x^{2^i} \mod f(x) \right\} \quad (7)
  \]
  Where \( f(x) \) is the field basis.

- Step 2: Feynman gates are applied during this Step. Thus, the input states are transformed to
  \[
  \left\{ \sum_{i=0}^{n-1} A_i \cdot x^{2^i} \mod f(x) \right\} \quad (8)
  \]
  Where \( f(x) \) is the field basis.

- Step 3: Step 3 of the proposed algorithm does not perform any new transformations on the input states.

Thus, we can see that the proposed algorithm will produce \( A^2 \) on the quantum register where \( A \) is stored originally. This proves the correctness of the proposed quantum Galois field squaring algorithm.

IV. QUANTUM GATE AND QUBIT COST ANALYSIS

The proposed quantum Galois field squaring circuits can be designed by following the three steps described previously in section III. The quantum gate and qubit cost analysis of the squaring circuits is performed by analyzing the steps involved in the proposed quantum Galois field squaring circuit algorithm. In our work, the quantum gate cost is defined as the total number of Clifford+T gates in the circuit. Each Clifford+T gate’s cost is considered as unity.

- Step 1:
  - This Step has a qubit cost of \( n \).
  - This Step has a quantum gate cost of 0.

- Step 2:
  - This Step does not add to the qubit cost
  - This Step has a different quantum gate cost for each Galois field. The quantum cost will depend on the result of:
    \[
    \alpha_i \cdot x^{2^i} \mod f(x) \quad (9)
    \]
    for each input qubit \( |\alpha_i\rangle \) where \( \left\lceil \frac{n-1}{2} \right\rceil \leq i \leq n-1 \).

- Step 3:
  - This Step does not add to the qubit cost
  - This Step has a quantum gate cost of 0.

Thus from Step 1, Step 2 and Step 3, the total quantum qubit cost of the Galois field squaring cost for each Galois field. The quantum cost will depend on the result of:

V. COMPARISON OF QUANTUM GALOIS FIELD SQUARE CIRCUITS FROM OUR PROPOSED ALGORITHM

There are existing designs of quantum circuits for Galois field squaring such as the designs in [7]. Table I illustrate the comparison between our proposed Galois field squaring

Fig. 2: Generation of quantum Galois field squaring circuit for the field with basis \( f(x) = x^{10} + x^3 + 1 \): Steps 1-3.

existing quantum squaring circuit design in [7] requires \( n \) ancillae. Thus, the proposed circuits reduce qubit cost by 50%.

- Step 2: Repeat Step 2 For \( i = \left\lceil \frac{n-1}{2} \right\rceil : 1 : n-1 \):
  - For \( k = 0 : 1 : n - 1 \):
    - If \( B_k = 1 \) in equation (3) for qubit \( |A_i\rangle \) and qubit \( |Y_i\rangle \) will not have the value \( |Y_k\rangle \), apply a Feynman gate such that \( |A_i\rangle \) and the qubit that will have the value \( |Y_k\rangle \) are passed to the inputs \( A \) and \( B \) respectively.

- Step 3: This Step has three sub-steps:
  - Step 1: select a gate as a reference gate
  - Step 2: If a gate shares a qubit with reference gate, move it to the end of the circuit
  - Step 3: If more than 1 gate is moved then repeat Steps 1 and 2 with only the moved gates
TABLE I: Comparison of the quantum circuits generated by the proposed Galois field squaring algorithm against the circuits in paper [7] for several field basis.

| Quantum Squaring Circuit Performance Comparisons | Qubits | Gates | Depth |
|------------------------------------------------|--------|-------|-------|
| Size 1 | 1 | This work | % Imp. w.r.t. | 1 | This work | % Imp. w.r.t. | 1 | This work | % Imp. w.r.t. |
| 10 | 20 | 10 | 50.00 | 16 | 6 | 62.50 | 4 | 2 | 
| 15 | 30 | 15 | 50.00 | 22 | 7 | 68.18 | 2 | 1 | 
| 20 | 40 | 20 | 50.00 | 31 | 11 | 64.52 | 4 | 2 | 
| 50 | 100 | 50 | 50.00 | 129 | 79 | 38.76 | NA | 6 | 
| 64 | 128 | 64 | 50.00 | 165 | 101 | 38.79 | NA | 7 | 
| 100 | 200 | 100 | 50.00 | 264 | 164 | 37.88 | NA | 8 | 
| 127 | 254 | 127 | 50.00 | 190 | 63 | 66.84 | 2 | 1 | 
| 256 | 512 | 256 | 50.00 | 652 | 396 | 39.26 | NA | 6 | 
| 512 | 1024 | 512 | 50.00 | 1291 | 779 | 39.66 | NA | 8 | 

1 is the design in [7]. Table entries marked NA where data is unavailable for design in [7].

circuits with those in [7] for several representative Galois fields. The quantum gate cost, qubit cost and depth will be used for comparison. Table I shows that the quantum Galois field squaring circuits from our algorithm excel against the existing Galois field squaring designs in [7] in terms of quantum gate cost, qubit cost and depth. Circuit depth was reported for Galois field squaring designs in [7] for only Galois fields defined by irreducible trinomials. From Table I it can be seen that the Galois field squaring circuits from our proposed algorithm achieve improvement ratio of 50.00% and improvement ratios ranging from 37.88% to 68.18% compared to the designs in [7] in terms of qubit cost and quantum gate cost.

VI. PROPOSED GALOIS FIELD EXPONENTIATION ALGORITHM

The proposed quantum Galois field exponentiation circuits is designed to minimize ancillae, is without any garbage outputs and has reduced quantum gate cost from all squaring operations. The proposed quantum Galois field exponentiation circuit is based on the proposed quantum Galois field squaring circuit, the logical reverse of the proposed quantum Galois field squaring circuit, an existing quantum Galois field multiplication circuit and the logical reverse of the existing quantum Galois field multiplication circuit. Figure 3 shows the graphical representation of components used in the proposed Galois field exponentiation circuit.

The proposed quantum Galois field squaring circuit and the logical reverse of the proposed quantum Galois field squaring circuit are 1 input and 1 output quantum circuits. The proposed quantum Galois field squaring circuit has the mapping $A \rightarrow A^2$ and the logical reverse of the proposed quantum Galois field squaring circuit has the mapping $A^2 \rightarrow A$. Existing designs of quantum Galois field multiplication circuits such as the designs in [1] are 3 input and 3 output quantum circuits. The existing designs of quantum Galois field multiplication have the mapping $A, B, C \rightarrow A, B, A \cdot B + C$. To implement $A \cdot B, C$ is replaced by ancillae. The logical reverse of the quantum Galois field multiplication circuit is a 3 input and 3 output quantum circuit and has the mapping $A, B, A \cdot B + C$ to $A, B, C$.

Consider the exponentiation of an $n$ bit field element $a$ stored at quantum register $|A\rangle$. Further consider a vector of $n - 1$ quantum registers $|B\rangle$. Each quantum register stores $n$ ancillae. At the end of computation, quantum register $|B[n-2]\rangle$ will have $A^{2^n-2} \mod f(x)$, while the quantum register $|A\rangle$ keeps the value $a$. Further, at the end of computation the quantum registers $|B[0:n-3]\rangle$ leave the circuit unchanged.

The generalized design methodology of designing the quantum Galois field exponentiation of an $n$ bit field value is shown in figure 4. The generalized algorithm for designing the quantum Galois field exponentiation circuit is discussed below.

A. Steps of the Proposed Algorithm for Galois field exponentiation

- **Step 1** has the following three sub-steps
  - **Step 1:** At location $|A\rangle$, apply a quantum Galois fields squaring circuit from our proposed algorithm.
  - **Step 2:** For $i = 0 : 1 : n$
    - Apply a Feynman gate such that the locations $|A_i\rangle, |B[0]_i\rangle$ are passed to the inputs $A, B$ respectively.
  - **Step 3:** For $i = 2 : 1 : n-1$
    - At location $|A\rangle$, apply a quantum Galois fields squaring circuit from our proposed algorithm.
    - Apply a quantum Galois field multiplication circuit such that the locations $|A\rangle, |B[i-2]\rangle$ and $|B[i-1]\rangle$ are passed to the inputs $A, B$ and $C$, respectively.

The quantum Galois field exponentiation circuit for an $n$ bit Galois field after this Step is shown in figure 4.

- **Step 2** has the following four sub-steps
  - **Step 1:** For $i = n-2 : -1 : 2$
    - At location $|A\rangle$ apply the logical reverse of the quantum Galois field squaring circuit from our proposed algorithm.
    - Apply the logical reverse of the quantum Galois field multiplication circuit such that the locations $|A\rangle, |B[i-2]\rangle$ and $|B[i-1]\rangle$ are passed to the inputs $A, B$ and $C$, respectively.
aation circuits that produces the result
proposed algorithm designs a quantum Galois field exponenti-
Galois field exponentiation circuit that works correctly. The
field exponentiation circuit algorithm results in a quantum
changes on the inputs:

| registers a is stored is restored to the value

Let Theorem: Let a be a n bit binary number represented as
| A ⟩ and let | B ⟩ be a n − 1 element quantum register vector
of n qubit ancillae, then the steps of the proposed Galois
field exponentiation circuit algorithm results in a quantum
Galois field exponentiation circuit that works correctly. The
proposed algorithm designs a quantum Galois field exponenti-
ation circuits that produces the result $a^{2^{-n-2}} \mod f(x)$ at
the quantum register | B[n − 2] ⟩, while the quantum register
where a is stored is restored to the value a. Further, the quantum
registers | B[0 : n − 3] ⟩ are restored to their original values.

Proof: The proposed algorithm will make the following
changes on the inputs:

- Step 1: Step 1 of the proposed algorithm transforms the
input states to

$$|A^2| |A^2⟩ \left( \prod_{i=2}^{n-1} A^{2^j} \right) \mod f(x) \right) \tag{10}$$

Where $f(x)$ is the field basis.

- Step 2: Step 2 of the proposed algorithm transforms the
input states to

$$|A⟩ \left( \bigotimes_{i=0}^{n-3} |B[i]⟩ \right) |A^2| \mod f(x) \right) \tag{11}$$

Where $f(x)$ is the field basis.

Thus, we can see that the proposed algorithm will produce
the result at the quantum register where | B[n − 2] ⟩ is stored
initially, while the quantum register | A ⟩ initially holding a is
restored to the value a. The quantum registers | B[0 : n − 3] ⟩
will be restored to their initial values after Step 2. This
proves the correctness of the proposed quantum Galois field
exponentiation algorithm.

VII. QUANTUM GATE AND QUBIT COST
ANALYSIS

TABLE II: Comparison of the quantum exponentiation circuits
with the proposed Galois field squaring circuits against identical
Galois field exponentiation circuits using the Galois field
squaring circuits in [7].

| Quantum Exponentiation Circuit Performance Comparisons | Gate cost from squarings | Qubits |
|--------------------------------------------------------|-------------------------|--------|
| Field Size | w.1 | w. This Imp. | w.r.t 1 | w. 1 | w. This Imp. | w.r.t 1 |
| 10 | 144 | 54 | 62.50 | 180 | 100 | 44.44 |
| 15 | 308 | 98 | 68.18 | 420 | 225 | 46.43 |
| 20 | 589 | 209 | 64.52 | 760 | 400 | 47.37 |
| 50 | 6321 | 3871 | 38.76 | 4900 | 2500 | 48.98 |
| 64 | 10395 | 6363 | 38.79 | 8064 | 4096 | 49.21 |
| 100 | 26136 | 16236 | 37.88 | 19800 | 10000 | 49.49 |
| 127 | 23940 | 7938 | 66.84 | 32004 | 16129 | 49.60 |
| 256 | 166260 | 100980 | 39.26 | 130560 | 65536 | 49.80 |
| 512 | 659701 | 398069 | 39.66 | 512 | 262144 | 49.90 |

* 1 is the design in [7].

The proposed quantum Galois field exponentiation circuit
can be designed with the two steps described in section [VI].
The quantum gate and qubit cost analysis of the proposed
quantum Galois field exponentiation circuit are performed by
analyzing the steps involved in the design of the proposed
circuits. In this analysis, $G_K$ represents the quantum gate cost
of the proposed Galois field squaring circuits, $G_U$ represents
the quantum gate cost of the quantum Galois field multiplier
and $G_{K^{-1}}$ and $G_{U^{-1}}$ are the quantum gate costs for the logical
reverses of the Galois field squaring circuits and Galois field
multiplication circuits respectively.

- Step 1:
  - This Step has a qubit cost of $n^2$.
  - This Step has a quantum gate cost of $(n − 1) \cdot G_K +
(n − 2) \cdot G_U$. 

Fig. 4: Circuit generation of Galois field exponentiation of an $n$ bit field value: Steps 1-2.
• Step 2:
  - This Step does not add to the qubit cost.
  - This Step has a quantum gate cost of \((n - 1) \cdot G_{K-1} + (n - 2) \cdot G_{U-1}\).

Thus from Step 1 and Step 2, the total quantum gate cost of the quantum exponentiation circuit can be summed up as
\[(n - 1) \cdot G_K + (n - 2) \cdot G_U + (n - 1) \cdot G_{K-1} + (n - 2) \cdot G_{U-1},\]
while the qubit cost is \(n^2\).

VIII. COMPARISON OF QUANTUM GALOIS FIELD EXPONENTIATION CIRCUITS

We present the quantum circuit implementation of Galois field exponentiation for the first time in the literature. Thus, we are comparing the proposed quantum Galois field exponentiation circuits made using our proposed Galois field squaring circuits with the proposed quantum exponentiation circuits made using the Galois field squaring circuit designs in [7] in terms of quantum gate costs from all squaring operations and qubit cost. Table I illustrates the comparison of the proposed quantum Galois field exponentiation circuit with squaring circuits from our proposed algorithm with proposed Galois field exponentiation circuit with the existing squaring circuit designs in [7] for several representative Galois fields. Table I shows that quantum Galois field exponentiation circuit with squaring circuits from our proposed algorithm excel against quantum exponentiation circuits made with existing squaring circuit designs in terms of qubit cost and the quantum gate cost from all squaring operations. From table I it can be seen that quantum Galois field exponentiation circuits made with squaring circuits from our proposed algorithm see improvement ratios ranging from 44.44% to 50.00% and 37.88% to 68.18% compared to quantum Galois field exponentiation circuits made with the squaring circuit designs in [7] in terms of qubit cost and the total quantum gate cost from all squaring operations.

IX. CONCLUSION

In this work, we have presented an algorithm to generate quantum circuits for Galois field squaring using Feynman gates. The generated quantum Galois field squaring circuits are optimized for gate cost, depth and have zero overhead in terms of number of ancillae compared to existing designs. Further, we present an algorithm for the quantum circuit implementation of Galois field exponentiation that uses proposed quantum squaring circuit. The proposed algorithm to generate quantum circuits for Galois field exponentiation is verified by formal proof and with functional verification of generated Galois field squaring circuits in MATLAB. The proposed algorithm to generate quantum circuits for Galois field exponentiation is verified by formal proof. The Galois field squaring circuits and Galois field exponentiation circuits generated from our proposed algorithms will find promising applications in quantum computing and could form components of quantum Galois field processing architectures.

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