Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking

This paper studies beyond-CMOS devices in detail and proposes a uniform methodology for their benchmarking.

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ABSTRACT | Multiple logic devices are presently under study within the Nanoelectronic Research Initiative (NRI) to carry the development of integrated circuits beyond the complementary metal–oxide–semiconductor (CMOS) roadmap. Structure and operational principles of these devices are described. Theories used for benchmarking these devices are overviewed, and a general methodology is described for consistent estimates of the circuit area, switching time, and energy. The results of the comparison of the NRI logic devices using these benchmarks are presented.

KEYWORDS | Adder; beyond complementary metal–oxide–semiconductor (beyond-CMOS); computational throughput; electronics; integrated circuits: logic; power dissipation; spintronics

I. INTRODUCTION

The development of complementary metal–oxide–semiconductor (CMOS) integrated circuits has had unprecedented success from the scaling with its dimensions with each new technology generation. Its further development is charted over the next several years by the International Technology Roadmap for Semiconductors [1] (ITRS). From the ITRS projections it is apparent that the scaling will be influenced by fundamental physical limits of device switching [2]. Due to this observation, research thrusts in the academia and the industry [most prominently, the Nanoelectronic Research Initiative (NRI)] gained significant momentum toward demonstrating and thoroughly investigating feasible alternatives to CMOS.

The NRI group has also performed benchmarking of the “beyond-CMOS” devices [3]. Such an investigation is of utmost importance, since it permits identification and focusing of resources on researching the most promising devices. However this benchmarking investigation provided only a summary report of the results (e.g., Fig. 1), without providing a uniform common methodology and details behind the benchmarking calculations needed to reproduce them. Also different investigators made sometimes widely different assumptions regarding the operating conditions and characteristics of individual devices. One of the main goals of this study was to obtain the values for the area, switching time, and switching energy of a set of standard circuits—an inverter with a fanout of 4, a two-input NAND gate, and a 32-b adder. We adopt the same circuits in this paper and have improved the benchmarking accuracy through the use of the proposed methodology. Such benchmarks are very useful as they allowed for the first time a comparison of the promise of beyond-CMOS computing with the mainstream, CMOS, computing. However, one needs to be aware of limitations of such an approach. It well may happen that a different circuit
architecture needs to be developed for optimal performance of beyond-CMOS devices. For example, spintronic devices are nonvolatile (preserve their state when the power is switched off), and a different circuit is needed to make use of this property to create normally-off instantly-on logic chips. Present benchmarks are not designed to measure this utility of devices. Moreover, different devices may prove to be best suited for different roles within a circuit. We conjecture that future integrated circuits will still contain a majority of CMOS devices with a few other beyond-CMOS devices performing various specialized functions. Also, by focusing on the switching energy, one comprehends only the active power dissipation, but not the standby (“leakage”) power. Such benchmarks need to be a subject of future research.

In this paper, we are setting out to establish a consistent standard methodology for benchmarking beyond-CMOS logic devices in order to obtain a reliable set of metrics and fair comparison of these devices. In treatment of the devices we chose simplicity rather than rigor. Wherever possible, we used analytical expressions, rather than simulations, for calculations of benchmarks. At the present time, the structure of the devices and their operational characteristics are not firmed up. We believe it presumptuous at this early stage of the research to expect the benchmarks to be accurate within less than a factor of 2. We strived for uniformity of benchmarking: same assumptions, relations, and schemes are applied to all devices to which they may pertain. Therefore, the relative benefits of the devices under study might be more accurate than their absolute values. We also insisted on complete transparency of our benchmarks. All the equations and parameters used are listed in this paper. We provide the Matlab code used to generate all plots in this paper [4]. This way the readers can reproduce all the results of the paper. Also they can plug in their values and assumptions and explore “what if” scenarios.

The paper is structured as follows. The requirements of logic technologies are outlined in Section II. Non-traditional computational variables are described in Section III. The nomenclature of beyond-CMOS devices is introduced in Section IV. Physical constants and device parameters are listed in Section V. The principles of layout and assumptions about the gate size are described in Section VI. The method used for estimating the circuit area is explained in Section VII. General considerations for time and energy of capacitance charging are considered in Section VIII. Simple analytical expressions for the switching time and energy of electronic circuits are proposed in Section IX. Estimates for various methods of magnetization switching are collected in Section X. Section XI contains the estimates of performance for spintronic devices. Overall benchmarks for devices are compared in Section XII. The consequences for the computational throughput and dissipated power are calculated in Section XIII. The results of the paper are discussed in Section XIV.

In this paper, we limit the scope to only digital circuits. We do not consider analog, mixed, or digital-to-analog conversion circuits. Moreover, we only consider Boolean logic, thereby excluding non-Boolean [6] or neuromorphic [7] computing.
II. TENETS OF LOGIC AND DEVICE INTERCONNECTION

Before it can be considered as a candidate for an element of an integrated logic circuit, a solid-state device needs to satisfy a set of requirements [8], “logic tenets,” such as:

1) nonlinear characteristics (related to noise margin and the signal-to-noise ratio);
2) power amplification (gain > 1);
3) concatenation (output of one device can drive another);
4) feedback prevention (output does not affect input);
5) complete set of Boolean operators (not, and, or, or equivalent).

In addition, it needs to be competitive in the quantitative physical measures of:

1) size (i.e., scalability);
2) switching time;
3) switching energy (i.e., power dissipation).

Finally, the following technological requirements may decide the fate of a device in the competition to be the next technology of choice:

1) room temperature or higher operation;
2) low sensitivity to parameters (e.g., fabrication variations);
3) operational reliability;
4) CMOS architectural compatibility (interface, connection scheme);
5) CMOS process compatibility (fabricated on the same wafer);
6) comprehending intrinsic and extrinsic parasitic and their interface to interconnect.

Devices considered in this study are at various levels of technological maturity. Some have been demonstrated experimentally, operation of others has been simulated, while some are still at the concept stage. In this paper, we do not review the status of experimental work of the devices or discuss the issues of their manufacturability. Neither are we trying to predict the success of their integration to logic circuits. We assume that devices would work as they are intended and estimate their performance starting from physical relations governing phenomena underlying them. We make optimistic assumptions about the material parameters, lithography capabilities, and device structures without pushing these values to their physical limits.

III. COMPUTATIONAL VARIABLES AND DEVICE CLASSIFICATION

The beyond-CMOS devices encode information by various physical quantities, which we call “computational variables.” A list and a pictorial representation of types of computational variables are shown in Fig. 2. We use them to classify devices.

1. Charge, current, voltage (Q, I, V)
2. Electric dipole (P)
3. Magnetic dipole = spin (M)
4. Orbital state (Orb) in e.g. quantum well, molecule, crystal, also excitons, esp. Bose condensate (BEC)

The first set of variables comprises charge, current, and voltage (designated as Q, I, and V, respectively). It is very familiar to the readers, as it is the underlying group of variables in electronic devices, which comprise the overwhelming majority of mainstream computing and a few beyond-CMOS options. Ferroelectric devices are based on electric dipoles (designated as P). Ferroelectric transistors [8] have been researched and demonstrated for many years now, and we do not include them in this study. Spintronic [9] devices [10] rely on magnetic dipoles represented by ferromagnetic elements or electrons with polarized spins (designated as M). Orbitronic devices are the least understood ones, as they involve the orbital state (designated as Orb) of electrons in a molecule or a crystal, and sometimes a collective state of electrons, such as Bose condensate of excitons (designated as BEC). In the current study, they are represented by a single device, the bilayer pseudospin FET (BisFET). There are other computational variables, described in the ITRS [1] ERD chapter, such as: mechanical position for NEMS devices, light intensity for photonic devices, timing of signals in neuromorphic computing, etc. But they are not used in this study.

The computational variables can have various roles in a logic circuit. To explain them, we envision a very abstract black-box diagram of a logic device shown in Fig. 3. The computational variables embody the internal state, input and output signals, and the controls for switching devices (including clocking).

One of the tenets of logic (in Section II) is that the output of one stage needs to be able to drive the input to
the next stage. If this condition is not satisfied for a device, e.g., the input is a voltage signal but the output is a magnetization signal, special purpose devices, which we call “transducers,” are needed to convert one variable to another. The most important transducers discussed below are the ones converting electronic signals to spintronic ones and vice versa.

IV. NOMENCLATURE AND SHORT DESCRIPTION OF THE DEVICES

Devices are classified according to their computational variables as they represent inputs, outputs, and the internal state (Section III) when the devices are connected in an integrated circuit; see Table 1. The subclass is assigned according to a phenomenon underlying the device operation. This is explained in more detail as we go over devices one by one. We aim to give a very short description of the features of each device and the nature of connections relevant for our discussion.

A. CMOS

The CMOS FET (Fig. 4) is a familiar device. Its internal state is a charge on the capacitor of the gate dielectric. The input and gate voltages determine the output voltage (Fig. 5). Switching is done by raising and lowering of the potential barrier for electrons in the channel due to a change of the gate voltage. For high-performance CMOS (CMOS HP) we use the values from the 2011 edition of ITRS [1] PIDS chapter. There the technology node \( F = 15 \text{nm} \), which was chosen for the first NRI benchmarking study, corresponds to the 2018 column. The low-power CMOS (CMOS LP) used in the NRI benchmarking study is envisioned as a low supply voltage (0.3 V) device from [11].

Table 1 Nomenclature and Classification of the Evaluated Devices

| Device name               | acronym       | input | control | int. state | output | class         | subclass |
|---------------------------|---------------|-------|---------|------------|--------|---------------|----------|
| Si MOSFET high performance| CMOS HP       | V     | Vg      | Q          | V      | electronic    | barrier  |
| Si MOSFET low power       | CMOS LP       | V     | Vg      | Q          | V      | electronic    | barrier  |
| Homojunction TFET         | HomITFET      | V     | Vg      | R          | V      | electronic    | tunneling|
| Heterojunction TFET       | HetITFET      | V     | Vg      | R          | V      | electronic    | tunneling|
| Graphene nanoribbon TFET  | gnrITFET      | V     | Vg      | R          | V      | electronic    | tunneling|
| Graphene pn-junction (Veselago) | GpnJ   | V     | Vg      | R          | V      | electronic    | refraction|
| Bilayer pseudospin FET    | BisFET        | V     | Vg      | BEC        | V      | orbitronic    | exciton |
| SpinFET (Sughrar-Tanaka)  | SpinFET       | V     | Vg, Vm  | Q, M       | V      | spintronic    | spin drift|
| Spin torque domain wall   | STT/DW        | I     | V       | M          | I      | spintronic    | domain wall|
| Spintronic majority gate  | SMG           | M     | V       | M          | M      | spintronic    | domain wall|
| Spin torque triad         | STTriad       | I     | V       | M          | I      | spintronic    | nanomagnet|
| Spin torque oscillator    | STOlogic      | I     | V       | M          | I      | spintronic    | nanomagnet|
| All spin logic device     | ASLD          | M     | V       | M          | M      | spintronic    | spin diffusion|
| Spin wave device          | SWD           | M     | I or V  | M          | M      | spintronic    | spin wave |
| Nanomagnetic logic        | NML           | M     | B or V  | M          | M      | spintronic    | nanomagnet|
B. Tunneling FET

Tunneling FETs (TFETs) [12] are considered under three material options: homojunction III–V material (HomJFET; Fig. 6) specifically InAs double-gate transistor, heterojunction III–V material [13] (HetJFET; Fig. 7) specifically InAs/GaSb double-gate transistor, and graphene nanoribbon (gnrFET; Fig. 8). They have the same principle of operation and differ in performance parameters: supply voltage and drive current. Parameters for TFET are taken from simulation, such as [14]. Conduction in a TFET occurs through band-to-band tunneling (BTBT). Gate voltage shifts the bands in energy and drastically changes the probabilities of tunneling. The block diagram of TFET (Fig. 10) is very similar to that of CMOS. Simulations show that charge on a gate of the TFET is smaller than the corresponding CMOS [15]. Therefore, we prefer to associate the state of the device with the resistance of the channel \((R)\). Besides, this smaller gate capacitance contributes to faster switching of circuits, an advantage of TFET beyond just comparing drive currents.

C. Graphene \(pn\)-Junction

A graphene \(pn\)-junction (GpnJ; Fig. 9) [16] device uses the junctions to switch the path of electrons. It shares the block diagram with the TFET (Fig. 10) signifying the change of the resistance as an internal state, but relies on a completely different physical phenomenon. Reflection of electrons from \(pn\)-junctions in graphene is highly dependent on the angle due to its peculiar band structure. Therefore, by switching the electrostatic \(p\) and \(n\) doping of graphene by applying voltage to electrodes, it is possible to achieve either a very high transmission or a total internal reflection of electrons. Thus, current is directed to one versus another output of the device.

D. BisFET

A BisFET (Fig. 11) [17] is another graphene device. It exploits tunneling between two monolayers of graphene. Due to a stronger interaction of electrons and holes in graphene, it is expected that they will bind into excitons at a higher temperature than in traditional semiconductors. If holes are injected into one monolayer and electrons into another monolayer, they may bind into excitons and these excitons might relax into a Bose–Einstein condensate (BEC) state. Considerable controversy exists about the critical temperature of BEC in bylayer graphene: the original proposal [18] suggested that it is above room temperature, while subsequent calculations [19] predict that it is much lower than 1 K. The presence of BEC is expected to drastically increase the probability of tunneling due to its
collective nature. BEC state can be destroyed due to changing the balance between electrons and holes by applying a gate voltage. Thus, voltage controls the internal state \( R \) of the device related to the presence of the condensate; see Fig. 12. The current between source \( (S) \) and drain \( (D) \) in Fig. 11 is expected first to grow with the increase of voltage \( V_{ds} \) and then decrease as the carrier imbalance destroys BEC (thus exhibiting negative differential resistance). The device proposal [17] postulates the current–voltage \( (I/V) \) curve with a peak at voltage of 5 mV. For the present benchmarks, we use the results of quantum transport simulations [20]–[22], which exhibit \( I/V \) curves with peak voltages of 150–400 mV, though they were performed for a different value of the interlayer coupling constant and different wiring of the device. Gates \( V(+) \) and \( V(-) \) are designed to maintain certain high densities of electrons and holes in the bottom and top graphene layers, respectively. These potentials need to be kept constant. Gate \( G \) covers only a half of the channel and is used to control the BisFETs in logic circuits. Its intended use is “current crowding”: the applied voltage causes current to flow on one side of the channel. If current density there exceeds the peak value, conduction there drops, and the current is forced to the other side and it exceeds the peak current density there as well.

E. SpinFET

A spinFET (Fig. 13) [24] combines a MOSFET and a switchable magnetic element. Its source and drain are made of ferromagnetic metals and another ferromagnet is positioned over a drain in order to detect its direction of magnetization via a tunneling magnetoresistance (TMR) effect. In addition to the usual FET functionality \( R(Q) \), the resistance of a spin FET depends on the magnetization state \( R(M) \); see Fig. 14. If the magnetizations of the source and drain are parallel, the resistance of the channel is low. If they are antiparallel, the resistance is high. In addition to the current through the channel, the magnetization of the drain can be switched by a current from a terminal controlled by voltage \( V_m \).

F. Spintronics Features

As in most of the spintronic devices, the magnetic tunnel junction (MTJ) is required only at the output magnets in order to detect the direction of magnetization. MTJ is a stack of a ferromagnet, a tunneling dielectric, and another ferromagnet. It has a huge advantage in the values of magnetoresistance (MR) compared to spin valves, but at the price of around three orders of magnitude higher
resistance-area product. A spin valve is a stack of a ferromagnet, a nonmagnetic metal, and another ferromagnet. When only a switching based on the spin torque principal is required, a spin valve is preferable and gives a comparable polarization of the spin current.

Most of the spintronic devices are nonvolatile, i.e., their computational state is preserved even when the power to the circuit is turned off. The condition for nonvolatility is stability of nanomagnets against thermal fluctuations. In other words, the magnet should have two states of equilibrium separated by a barrier with energy greater than 60 \( k_B T \).

**G. Spin Transfer Torque Domain Wall Device**

A spin transfer torque/domain wall (STT/DW) device (Fig. 15) [26] operates by motion of a domain wall in a ferromagnetic wire. The motion is caused by a spin transfer torque effect of a current along the wire (unlike a current perpendicular to the wire used in the rest of the spin torque devices in this paper). As the domain wall moves, the magnetization below the MTJ stack (in the middle of the device) switches, resulting in high or low resistance of the stack. Then, a current from the “clock” terminal to the output through the MTJ is either high or low. The current is used to drive the inputs of next stages (Fig. 22).

**H. Spintronic Majority Gate**

A spintronic majority gate (SMG; Fig. 16) [27], [28] is implemented with a “cross” of ferromagnetic wires. It has three inputs and one output terminals formed over the ends of the “cross” as nanopillars with their own ferromagnetic layer. Current from each nanopillar exerts spin torque which aims to switch magnetization to a certain direction, depending on the sign of the current. The majority of the inputs win and enforce their direction of the magnetization. This is sensed via the tunneling magnetoresistance (TMR) effect using a sense amplifier (Fig. 23). Like a few other spintronic devices, inputs can be switched and outputs can be sensed by a magnetoelectric (ME) cell (rather than spin torque and TMR); see Fig. 24. For the principle of operation of an ME cell, see Section X. It should be noted that electrical-to-spin conversion (= writing and sensing of magnetization) does not need to occur at every majority gate input/output. Instead, multiple majority gates can be cascaded into a larger magnetic circuit. For example, three majority gates are enough to form a one-bit full adder. Electrical-to-spin conversion then happens only at the adder interface between the magnetic and electronic circuits.

**I. Spin Transfer Torque Triad**

A spin transfer torque triad (STT/etriad) [29] element works in a manner similar to the SMG. However, it consists of triangular structures (Fig. 17) with two inputs and one output. Then, the current from one triangle is used to drive spin torque switching in other triangles, in a manner similar to STT/DW (Fig. 22). This geometry implies electrical-to-spin conversion at every computing element, rather than cascading magnetic signals.
J. Spin Torque Oscillator Logic

Spin torque oscillator (STO) logic [30] contains oscillators which are driven by spin torque from currents entering each of them through nanopillars on top (Fig. 18). STOs are combined into a majority gate with three input and one output oscillator. The oscillators have a common ferromagnetic layer, similar to SMG. Oscillations cause spin waves to propagate in the common layer and thus the oscillators’ signal couple. The frequency of the output oscillator is determined by the majority of inputs and serves as the logic signal in the circuit. By the nature of the signals, STO logic is described by the block diagram in Fig. 19. Since in order to oscillate the STOs must have only one position of equilibrium, therefore this type of logic is volatile.

K. All Spin Logic

An all spin logic device (ASLD) [31], [32] is formed by nanomagnets placed over a copper wire (Fig. 20). Each nanomagnet has input and output sides separated by an insulator. Voltage supplied to the top of each nanomagnet drives a current to the ground terminal nearby. Due to this current, spin polarized electrons accumulate near each nanomagnet. Concentrations of polarized spins are different at the input and output sides of the two neighboring magnets, which causes a diffusion spin current to occur. This spin current exerts torque on a nanomagnet and is able to switch its polarization. The nanomagnets are often arranged into majority gates. The nanomagnets can be concatenated according to the block diagram in Fig. 23, for example, to produce a one-bit full adder, as in Fig. 20.

L. Spin Wave Device

A spin wave device (SWD; Fig. 21) [34], [35] contains nanomagnets connected by ferromagnetic wires. Spin waves are excited in the wires and propagate along them. Short pulses of spin waves containing a wide range of frequencies are used. There are two versions of the device in which: 1) spin waves are excited and detected by a radio-frequency (RF) antenna; this version does not need nanomagnets and is volatile, corresponding to the scheme in Fig. 23; and 2) spin waves are excited and detected by a magnetoelectric cell; it includes nanomagnets and is non-volatile, corresponding to the scheme in Fig. 24. The magnetization of a nanomagnet determines the phase of the spin wave at a given coordinate. In its turn, this phase determines to what direction magnetization will switch in the output nanomagnet. SWD gates are readily amenable to cascading.

M. Nanomagnetic Logic

Nanomagnetic logic (NML; Fig. 22) [36] consists of a chain of nanomagnets. They interact by magnetic dipole coupling. NML is the only device in the NRI suite of spintronic devices which uses Bennett clocking [36]. In other words, its operation occurs by preparing all nanomagnets in a quasi-stable equilibrium state by the action of a magnetic field from a current in a wire (current clocking, Fig. 23) or effective magnetic field from the charging a magnetoelectric cell (voltage clocking, Fig. 24). In both cases, the state of magnets at the input causes the magnets in the circuit to choose one of the stable equilibrium states determined by the dipole interaction between magnets. It is easy to cascade NML gates.

N. Other Devices

Beyond-CMOS devices previously considered within the NRI studies or in other research overviews that are not included in this study are: Datta–Das spin modulator [37]; electronic ratchet [38]; graphene thermal logic [39]; SET/BDD [40]; electron structure modulation transistor [41]; RAMA [42], [43]; resonant injection enhanced FET [44]; magnetic domain-wall logic [45]; domain wall
majority gate logic [46]; MottFET [47]; spin Hall effect transistor [48]; few spin device [49]; and MTJ plus CMOS logic [50]–[53]. We also do not cover the optoelectronic excitonic transistor, which was demonstrated [54]–[56], as well as other proposed versions of excitonic FETs [3], [57], [58]. The reason for noninclusion is either lack of input information to build benchmarks or insufficient research activity on this device at NRI.

V. CONSTANTS AND PARAMETERS

For the estimates of the device performance, we use the constants and parameters collected in Tables 2 and 3.

VI. LAYOUT PRINCIPLES

In this section, we propose a simple but general method to estimate the areas of beyond-CMOS circuits. The semiconductor process generations are labeled by characteristic...
lithography size called the DRAM’s half-pitch \( F \). It is set to 15 nm in this study. ITRS [1] projects values of many device parameters depending on \( F \). We use the device parameters listed in Table 4.

The layout of the devices is governed by the design rules which specify minimum width and spacing of various elements in the circuit [63]. Scalable design rules are formulated in units of maximum mask misalignment \( \lambda \), where typically \( \lambda = F/2 \). An example of design rules is shown in Fig. 25.

We see in Fig. 26 that the pitch of metal-1 in the contacted transistor is \( p_m = 8\lambda \). Fig. 27 shows the historical trend of the metal 1 contacted gate pitch scaling with the process generations [65].

From this plot, we approximately obtain that the metal 1 pitch is \( p_m = 4F \). This confirms the previous relation \( F = 2\lambda \). Since all the logic circuits (even spintronic circuits) need electrical contacts at the terminals of gates, their size will be determined by the metallization pitch much more than by their intrinsic device sizes. We proceed to draw layouts for simple circuits for all of the considered devices in the following section. We are using the color scheme shown in Fig. 28 to designate mask layers. We notice that their area can be estimated by counting the pitches of the most important lines (diffusion, gate (“poly”), metal 1) [64], as shown in Fig. 29. Here and in the rest of the document, one cell of the grid corresponds to size \( \lambda \). The contacted pitch for all these important lines proves to be \( 8\lambda \). Thus, in the rest of the paper, we take the minimum pitch between any contacted circuit elements to be \( 8\lambda = 4F \).

\[ a_{int} = \left( w_{X/S} + 2F \right) \left( p_m + 2F \right). \]  \hspace{1cm} (1)

**VII. CIRCUIT AREA ESTIMATION**

We use the parameters in Table 5 to calculate the sizes of devices and circuits.

The size of the intrinsic device (a transistor-like device has subscript \( X \), and a spintronic device has subscript \( S \)) is obtained as

\[ a_{int} = \left( w_{X/S} + 2F \right) \left( p_m + 2F \right). \]  \hspace{1cm} (1)

**A. Area of Transistor-Like Devices**

First, we deal on the same footing with the area estimates of transistor-like devices (CMOS HP, CMOS LP, HomJTFET, HETJTFET, gnrTFET, BisFET, SpinFET) and the area of the STT/DW, which all have the same or similar circuit architecture.

The sizes of the inverter with fanout-4, two-input NAND fanout-1, and two-input XOR fanout-1 gates are calculated using the factors in Table 5, which are derived from layout diagrams. We only include interconnects between neighbor gates. The interconnect length is important for calculating its capacitance and is estimated as

\[ l_{ic} = 5p_m. \]  \hspace{1cm} (2)
This interconnect’s area is not an additive term in the area calculation of the circuits, since it is positioned in the metal-1 layer. However, when interconnect area is needed to properly route interconnects, we account for the extra empty area needed around the gates and 1-b adder cells by introducing the empirically derived area overhead factors listed in Table 5. These factors work as follows. The area of a gate is obtained by estimating the gate length and width of the layout cell, and then multiplying it by the gate overhead factor. We assume that the inverter is made with the standard transistor width $w_X$. We take the $n$- and $p$-transistors to be of the same width due to an assumption of them having approximately equal on-current. The usual electrode pitch would accommodate transistors of width $w_X$. Extra width of transistors results in an increase of the gate area. So for the fanout-4 inverter its area is (Fig. 29)

$$ a_{inv4} = 2p_m \cdot (3p_m + 2w_X)M_{gate}. $$

For the NAND2 gate, we make the width of transistors in the pull-down network (nFET in this case) to be twice the

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### Table 3 Material Constants Used in the Analysis

| PHYSICAL QUANTITY                  | SYMBOL | UNITS  | TYPICAL VALUE |
|-----------------------------------|--------|--------|---------------|
| Ambient temperature               | $T$    | K      | 300           |
| Dielectric constant of SiO$_2$    | $\varepsilon$ | 3.9   |               |
| Dielectric constant of interlayer dielectric | $\varepsilon_{ILD}$ | 2    |               |
| Particle velocity in graphene     | $v_F$  | m/s    | 8e5           |
| Resistivity of copper             | $\rho$ | $\Omega \cdot m$ | 1.9e-8      |
| Magnetization in a ferromagnet, in plane | $M_S$  | A/m    | 1e6           |
| Magnetization in a ferromagnet, perpendicular | $M_{SP}$ | A/m | 0.3e6         |
| Injected spin polarization        | $P$    |        | 0.8           |
| Gilbert damping                   | $\alpha$ | 0.01  |               |
| Perpendicular magnetic anisotropy | $K_u$  | J/m$^2$| 6e5           |
| Current density for domain wall motion | $J_{dw}$ | A/m$^2$ | 1.4e11   |
| Magnetic permeability around wires | $\mu$  |        | 4             |
| Magnetic induction from a wire, required | $B_{mf}$ | T | 0.01       |
| Multiferroic electric polarization [59] | $P_{mf}$ | C/m$^2$ | 0.55  |
| Multiferroic switching field [59] | $E_{mf}$ | V/m | 2e7         |
| Multiferroic exchange bias        | $B_{mf}$ | T | 0.03       |
| Magnetostrictive switching field [60] | $E_{ms}$ | V/m | 6e5         |
| Magnetostrictive effective field [61] | $B_{ms}$ | T | 0.03       |
| Dielectric constant of piezoelectric [60] | $E_{ms}$ |        | 20000       |
| Magnetoelastic coefficient [62]   | $\alpha_{me}$ | s/m | 5.6e-9     |
| Dielectric constant of magnetoelastic | $\varepsilon_{me}$ |        | 1000         |

### Table 4 Device Parameters Used in the Analysis

| PHYSICAL QUANTITY                  | SYMBOL | UNITS  | TYPICAL VALUE |
|-----------------------------------|--------|--------|---------------|
| Gate length                        | $L_g$  | m      | 1.28e-8       |
| Equivalent oxide thickness, nominal | $EOT_0$ | m | 0.68e-9     |
| Equivalent oxide thickness, electrical | $EOT$ | m | 1.08e-9     |
| Contact resistance                 | $R_c$  | $\Omega \cdot m$ | 1.6e-4  |
| Contact capacitance                | $C_C$  | F/m    | 1.2e-10       |
| Magnetic induction to switch NML   | $B_{nd}$ | T | 0.01         |
| Ferromagnet thickness              | $d_{fn}$ | m | 2e-9         |
| Piezoelectric thickness for magnetoelastic effect | $d_{me}$ | m | 25e-9       |
A tunneling FET needs to have the source and the drain to have doping of opposite polarities close to each other. That would violate the traditional scalable CMOS design rules related to p-doped diffusion in an n-well (as we show in Fig. 30). We adopt a new design rule of minimum spacing of $2\lambda$ between n- and p-diffusion. Thus, a new process flow needs to be developed. Also, TFETs commonly have gate-drain underlap [11], which we set at the most stringent value of $2\lambda$. (Note that a version of a layout of vertical TFET performed according scalable MOS design rules was shown in [66].) With these two changes, the inverter for TFET has the same area as CMOS, while the area of NAND2 is increased to

$$a_{\text{nand}} = 3p_m \cdot (3p_m + 3w_X)M_{\text{gate}}.$$  \hspace{1cm} (4)

$$a_{\text{nand,tfet}} = 4p_m \cdot (3p_m + 3w_X)M_{\text{gate}}.$$  \hspace{1cm} (5)

In spite of the fact of an addition of an MTJ, the size of the SpinFET cell is the same as that of CMOS; see Fig. 31.

The layouts of BisFET circuits, according to the scheme in Fig. 12, are shown in Fig. 32. It is apparent that the area for BisFET circuits is larger due to many additional electrodes.

The logic diagram of 1-b of a full adder [67] (Fig. 33) shows that it consists of two XOR gates with two inputs and
three AND/OR gates with two inputs, and thus its area is approximately

\[ a_1 = (2a_{\text{xor}} + 2a_{\text{nand}})M_{\text{bit}}. \]  \hspace{1cm} (6)

We approximately set the xor area to \( a_{\text{xor}} = 3a_{\text{nand}} \). Note that the circuit diagram of a BisFET-based adder (Fig. 34; despite a different principle of device operation)

The area of the full 32-b adder is calculated as

\[ a_{32} = 32a_1M_{\text{add}}. \]  \hspace{1cm} (7)

**B. Area of STT/DW**

The structure of STT/DW is somewhat different and presents a special case. Three independent electrodes (two
inputs and one output) are required for one device which represents a NAND gate (Figs. 15 and 35). Therefore

\[
a_{\text{inv}} = 4a_{\text{STT}}M_{\text{gate}}. \tag{10}
\]

\[
a_{\text{STT}} = (w_S + F)(2p_m + 2F) \tag{8}
\]

\[
a_{\text{nand}} = a_{\text{STT}}M_{\text{gate}} \tag{9}
\]

(8) The adder consists of “two fanout-4 NANDs, one fanout-2 NAND, six fanout-1 NANDs, and nine COPY

---

**Fig. 30.** Layout and area estimation for a TFET inverter and a two-input NAND gate.

**Fig. 31.** Layout and area estimation for a SpinFET inverter and a two-input NAND gate.
elements” [26]; see Fig. 36. We neglect the area of copy elements and thus estimate the area of a 1-b adder as

\[ a_1 = 14a_{\text{nand}}M_{\text{lat}}. \]  

Note that from here on we do not explicitly consider the area occupied by driving transistors for spintronic circuits and just show the contacts to them, like in Fig. 35. The reason for this is that spintronic elements are placed between metallization layers, while the transistors are at the semiconductor level. We also assume that the area of spintronic circuits is limited by the size of spintronic elements rather than transistors.

C. Area of GpnJ

The layout of a single MUX is shown in Fig. 37 and a GpnJ adder is shown in Fig. 38. Red, white, and blue rectangles are top electrodes, and yellow and green triangles are p- and n-doped areas of graphene requiring bottom electrodes. One rectangle consisting of four graphene triangles realizes a MUX; it contains six electrodes along its length and two along its width. We estimate the area of a MUX (not limited by the width of graphene is \( w_g = 2F \))

\[ a_{\text{mux}} = 2p_m \cdot 6p_m. \]  

We assume that a fanout-4 and a two-input \textit{nand} gate can be composed from just one MUX

\[ a_{\text{inv}} = a_{\text{mux}}M_{\text{gate}} \]  \[ a_{\text{nand}} = a_{\text{mux}}M_{\text{gate}}. \]  

---

Fig. 32. Layout and area estimation for a BisFET inverter and a two-input \textit{nand} gate.

Fig. 33. Logic diagram for a transistor adder [67].
A 1 b of a full adder consists of ten MUXes and its area is

\[ a_1 = 10a_{\text{nand}}M_{\text{int}}. \]  

(15)

D. Area of Spintronic Devices

Last, we treat the area of spintronic devices (SMG, STOlogic, ASLD, SWD, and NML) similarly, because they are based on majority gates. The example of SMG is used in Fig. 39, but we claim that the area estimate is applicable to all spintronic devices. The size of the majority gate is taken as a size of one cross in Fig. 39.

We approximate the length of the majority gate by

\[ l_{\text{maj}} = 2p_m \]  

(16)

and the area of a majority gate is

\[ a_{\text{maj}} = l_{\text{maj}}^2 \]  

(17)

with the exception of STOlogic, where an additional factor of 3 is introduced to account for wiring of driving transistors in accordance to the layout; see Fig. 40.

The inverter with fanout-4 and a NAND gate can be implemented with just one majority gate

\[ a_{\text{inv4,nand}} = a_{\text{maj}}M_{\text{gate}}. \]  

(18)
Fig. 37. Three-dimensional scheme (top) and layout (bottom) of a GpnJ MUX, after [69].

Fig. 38. GpnJ adder scheme. The circuits for generating the sum (left) and the carry (right) signals.

Fig. 39. Layout of an SMG adder composed of three majority gates.
The 1-b full adder's area is determined by the number of majority gates required

\[ a_1 = N_{maj} a_{maj} M_{bit}. \]  

(19)

We assume that \( N_{maj} = 3 \) majority gates are needed to form a 1-b adder, as it has been pointed out in [70]. In some cases, fewer majority gates are required or a denser packing of them is possible. In these cases, we adjust the effective number of majority gates to be \( N_{maj} = 2 \) for SWD (see Fig. 41) and \( N_{maj} = 1 \) for NML (see Fig. 42).

While ASLD has two majority gates per adder due to a clever use of the device's functionality, we still set \( N_{maj} = 3 \) to correctly account for the cell area (see Fig. 43).

E. Area of STT Triad

The area of a STT Triad triangle element in Fig. 45 is estimated to be \( 17 \times 10 \text{ F}^2 \). It coincides with the area of a NAND gate the same. An inverter with fanout-4 requires four such triangles

\[ a_{inv4} = 4a_{maj} M_{gate}. \]  

(20)

A 1-b full adder requires nine triangles (Fig. 44), therefore

\[ a_1 = 9a_{nand} M_{bit}. \]  

(21)

The resulting estimates for the areas of beyond-CMOS devices are summarized in Table 6. Note that the intrinsic elements of spintronic logic are larger than those of electronic logic, but the areas of the adders implemented with them are smaller. This is due to the richer functionality of the spintronic majority gates which enables circuits with fewer elements.
VIII. GENERAL CONSIDERATIONS FOR SWITCHING TIME AND ENERGY

The switching time and energy of the devices strongly depends on the voltage and the current at which they operate. The most fruitful avenue for improvement of beyond-CMOS devices will be to find a lower operating supply voltage [71]: lower power alternatives with resulting large improvement in computing efficiency. In this study, we use a relatively low supply voltage of 10 mV for spin torque switching of spintronic devices. The reason this is possible is that magnetization switching by a current (see Section XI) is unlike transistor switching. Charging the gate capacitor of a transistor results in raising and lowering of a potential barrier, which needs to be several...
times higher than the thermal energy $kT$ (which corresponds to 26 mV) \[2\] in order to ensure sufficient turnoff of the transistor to suppress standby power dissipation. In magnetization switching the potential barrier separating the logical states is not changed, therefore such a consideration does not limit the supply voltage.

Another factor relevant to both electronic and spintronic circuits is the distribution of power and ground to the device. In order to minimize active power, the voltage controlling the power needs to be switched on only when a device is being switched. It may be problematic to switch a power network at a supply voltage smaller than the threshold voltage of a transistor. By setting this low supply voltage for spintronic devices, we implicitly neglect the dissipated power in controlling the low voltage power supply source and in the network for the power and ground distribution. Even though this contribution is significant, a correct account of it goes beyond the scope of this study. Therefore, we provide optimistic estimates for switching delay and energy of the circuits with a supply voltage of 10 mV. For comparison, we provide a more realistic calculation with a supply voltage of 100 mV.

For voltage-controlled switching of spintronic devices we always use the supply voltage of 100 mV. It is sufficient, considering that the necessary electric field proves to be small. In this case as well, the operating voltage is not related to raising and lowering the energy barrier and is not connected to standby power dissipation.

Table 7 contains the input parameter values we use in the benchmark calculations for each device. Such values need to be obtained from device-level simulations of the device characteristics. If these inputs change, so might the overall conclusions from the device comparison. For electronic devices, the on-current $I_{on}$ is taken as an input parameter. For spintronic devices, $I_{on}$ designates the current of the driving transistors, for when an electrical signal is needed, and we utilize the high-performance CMOS device for this purpose.
Since most devices (including spintronic) involve charging and discharging of a capacitor of some sort, charging/discharging make a major contribution to their performance. We treat capacitances consistently assuming that the most advanced gate stack is available for all of the devices. The ideal single gate dielectric capacitance per unit area (F/m²) is determined via the equivalent oxide thickness (EOT)

$$c_{gd} = \frac{\varepsilon \varepsilon_0}{\text{EOT}}.$$  \hfill (22)

This capacitance, through the use of EOT, includes both the dielectric capacitance and the semiconductor (aka quantum) capacitance, while EOT₀ would include only the dielectric capacitance. The ideal single gate capacitance per unit width (F/m) is

$$c_{gd} = c_{gd} L_g.$$  \hfill (23)

The device-dependent adjustment factor $M_{adj}$ specifies by how much the intrinsic gate capacitance is larger (or smaller) than the capacitance of a single gate dielectric. We take it larger for BisFET and SpinFET due to the capacitance of additional elements in the device, and we take it smaller for tunneling devices to account for a small gate charge in the on-state; see Table 7. We also include an additional factor of 2 for the BisFET to account for the top and bottom gates. The expression $M_{par}$ indicates the value of the parasitic capacitance [gate-to-source, gate-to-drain (Miller), gate-to-contact, etc.] in terms of the ideal single gate value. We take this factor to be the same for all devices. The total capacitance (F/m) with the parasitics and the device-dependent adjustment factor as well as the contact capacitance $C_c$ is

$$c_{il} = c_{gd}(M_{adj} + M_{par}) + C_c.$$  \hfill (24)

We estimate the capacitance of wires per unit length (F/m) by using the equations [72] for the capacitance of a line surrounded by two ground planes (above and below) and two neighboring lines

$$c_{il} = 2(c_{gr} + c_{tol}).$$  \hfill (25)

We use geometrical parameters as described in Table 5. The capacitance (F, farads) of a typical interconnect between gates is proportional to its length defined in (2)

$$C_{ic} = c_{il} L_{ic}.$$  \hfill (26)

For $F = 15$ nm, these capacitances are $c_{il} = 126$ aF/μm and $C_{ic} = 37.8$ aF.

**IX. SWITCHING TIME AND ENERGY FOR ELECTRONIC DEVICES**

The switching time and energy of transistor-like devices (CMOS HP, CMOS LP, HomJTFET, HEJTTFET, gnrTFET, SpinFET, BisFET) are all treated in the same manner. Even though the SpinFET is a spintronic device, the benchmarks considered here use only static combinational logic circuits, in which the magnetization state of SpinFET is not reconfigured.

**A. Intrinsic Values for Electronic Devices**

We use extremely simple algebraic equations to estimate the performance of electronic devices. The device capacitance is

$$C_{dev} = c_{il} w X$$  \hfill (27)

and the device on-current is

$$I_{dev} = I_{on} w X.$$  \hfill (28)

The intrinsic switching time and energy of the device is

$$t_{int} = \frac{C_{dev} V_{dd}}{I_{dev}}, \quad E_{int} = C_{dev} V_{dd}^2.$$  \hfill (29)
We approximate the time and energy of an interconnect as

\[ t_{ic} = \frac{0.7C_{ic}V_{dd}}{I_{dev}}, \quad E_{ic} = C_{ic}V_{dd}^2. \quad (30) \]

We also include an additional factor of 2 in the interconnect delay and energy for the BiSfET to account for more complex interconnects to the device.

**B. Switching Time and Energy of GpnJ**

The resistance of the graphene element is composed of the collimation resistance and the contact resistance

\[ R_{dev} = R_{coll} + R_{cont}. \quad (31) \]

Graphene resistivity is estimated according to [73]. The collimation resistance

\[ R_{coll} = \frac{R_q}{M_q} \quad (32) \]

is determined by the number of quantum modes that can propagate in the graphene sheet

\[ M_q = \frac{2k_Fw_g}{\pi} \quad (33) \]

which, in turn, is determined by the Fermi momentum set by applied bias voltage \( V \), which causes electrostatic \( p \)- or \( n \)-doping of graphene

\[ k_F = \frac{E_F}{\hbar v_F} \quad (34) \]

where \( E_F \) is the Fermi energy of carriers in graphene [73]

\[ E_F = \frac{1}{\gamma EOT_0} \left( \sqrt{\varepsilon^2 + 2\varepsilon\gamma eV_g EOT_0} - \varepsilon \right) \quad (35) \]

where \( V_g = V_{dd}/2 \) and the constant

\[ \gamma = \frac{1}{\varepsilon_0} \left( \frac{e}{2\pi\hbar v_F} \right)^2. \quad (36) \]

The contact resistance is inversely proportional to graphene width

\[ R_{cont} = \frac{R_c}{w_g}. \quad (37) \]

The on-current per width (A/m) in the device is

\[ I_{on} = \frac{V_{dd}}{(R_{dev}w_g)}. \quad (38) \]

The device capacitance \( C_{dev} \) which is being switched is that of the middle and side gates (shown in orange in Fig. 37). Their total area is 9F by 3F. To obtain the total capacitance of the switched MUX one needs to multiply it by \( c_0 \). The interconnect capacitance \( C_{ic} \) is calculated the same way as for other electronic devices, with an accounting of the area of the graphene device. The quantum capacitance is included in EOT. The intrinsic device delay and the interconnect delay are

\[ t_{int} = C_{dev}R_{dev}, \quad t_{ic} = C_{ic}R_{dev}. \quad (39) \]

The device intrinsic switching energy \( E_{int} \) and the interconnect energy \( E_{ic} \) are calculated the same way as for other electronic devices.

**C. Circuit Values for Electronic Devices**

The performance of simple circuits is calculated via the empirical factors in Table 8 that are chosen to approximately agree with the simulations done with PETE [67]. They approximately relate to the estimates obtained from comparing the logical efforts of these gates. For the fanout-4 (FO4) inverter, the fanout factor of 4 multiplies the expressions for delay and energy

\[ t_{inv} = 4(M_{inv}t_{int} + t_{ic}), \quad E_{inv} = 4(M_{Ein}E_{int} + E_{ic}/2). \quad (40) \]

| PARAMETER | TYPICAL VALUE |
|-----------|--------------|
| Time factor for inverter, \( M_{inv} \) | 0.8 |
| Energy factor for inverter, \( M_{Ein} \) | 0.8 |
| Time factor for adder, \( M_{add} \) | 1.4 |
| Energy factor for adder, \( M_{Eadd} \) | 0.3 |
| Parasitic capacitance factor, \( M_{cap} \) | 1.5 |
For the two-input NAND gate with fanout-1

\[ t_{\text{nand}} = M_{\text{inv}} t_{\text{int}} + t_{\text{ic}}, \quad E_{\text{nand}} = 2M_{\text{Einv}} E_{\text{int}} + E_{\text{ic}} \quad (41) \]

where the factor of 2 in the expression for the energy corresponds to two transistors in the pull-up or pull-down networks. For the XOR gate

\[ t_{\text{xor}} = 3t_{\text{nand}}, \quad E_{\text{xor}} = E_{\text{nand}}. \quad (42) \]

For the 1-b full adder

\[ t_1 = M_{\text{add}}(t_{\text{xor}} + 2t_{\text{nand}}), \quad E_1 = M_{\text{Eadd}}(2E_{\text{xor}} + 3E_{\text{nand}}). \quad (43) \]

D. Circuit Values for GpNJ

GpNJ constitutes a special case. Here an adder consists of ten MUXes, but the critical path, from carry-in to carry-out, traverses just one MUX. The energy involves switching all ten MUXes

\[ t_1 = M_{\text{add}}(t_{\text{int}} + t_{\text{ic}}), \quad E_1 = M_{\text{Eadd}}(10E_{\text{int}} + E_{\text{ic}}). \quad (44) \]

In order to approximately obtain the time and energy benchmarks for a 32-bit adder, the benchmarks for 1 b are multiplied by the number of bits = 32

\[ t_{32} = 32t_1, \quad E_{32} = 32E_1. \quad (45) \]

X. COMMON METHODS OF MAGNETIZATION SWITCHING

All spintronic devices considered here contain ferromagnets. In order to switch the logical state in them, their magnetization needs to be switched. Presently, the preferred way of switching magnetization is with current-controlled switching.

One example, where magnetization switching is done with the magnetic field of current, is clocking of NML.

Magnetization can also be switched by current via the effect of spin-transfer torque (STT).

For the case of in-plane magnetization with STT it is assumed that the nanomagnet has the aspect ratio of 2 and thus the area and volume of

\[ a_{\text{nm}} = 2w_S^2, \quad v_{\text{nm}} = a_{\text{nm}} d_{\text{fm}}. \quad (46) \]

The energy barrier height [74] is determined via the difference of the element of the demagnetization tensor in the plane of the nanomagnet \( \Delta N = N_{yy} - N_{xx} \) (which are a function of the ratios of the length, width, and thickness and of the shape of a nanomagnet) as follows:

\[ U_b = \frac{\Delta N \mu_0 M_s^2 v_{\text{nm}}}{2}. \quad (47) \]

See parameter definitions in Table 3. We take values approximately corresponding to the alloy CoFe. The critical current density (after [74]) is

\[ J_c = \frac{e \alpha \mu_0 M_s^2 d_{\text{fm}}}{\hbar P}. \quad (48) \]

We chose to operate with the switching current

\[ I_{\text{dev}} = 3I_c = 3J_c a_{\text{nm}}. \quad (49) \]

Then, the switching time is described by [74], [75]

\[ t_{\text{stt}} = \frac{e M_s v_{\text{nm}}}{g \mu_0 P(I_{\text{dev}} - I_c) \log \left( \frac{2\pi \sqrt{2k_b T}}{\sqrt{U_b}} \right)}. \quad (50) \]

Thus, the energy needed to switch is

\[ E_{\text{stt}} = I_{\text{dev}} V_{\text{dd}} t_{\text{stt}}. \quad (51) \]

For the case of the perpendicular magnetization STT, it is assumed the aspect ratio is 1, i.e.,

\[ a_{\text{nm}} = w_S^2, \quad v_{\text{nm}} = a_{\text{nm}} d_{\text{fm}}. \quad (52) \]

The barrier height is determined by the perpendicular magnetic anisotropy (PMA) [76]

\[ U_b = K_v v_{\text{nm}}. \quad (53) \]

We take parameters corresponding to a material with a relatively small saturation magnetization and high PMA such as CoPtCrB [77]. The critical current density [76] is

\[ J_c = \frac{2e \alpha K_v d_{\text{fm}}}{\hbar P}. \quad (54) \]
The switching time is given by the same expression (50).

A more energy efficient, but less technologically mature means of switching of magnetization is the voltage-controlled switching.

Voltage-controlled switching with an adjacent multiferroic material occurs due to the effective magnetic field at the interface that arises through the exchange bias effect. For this case, we take parameters corresponding to bismuth-ferrite (BiFeO₃, BFO) [59], [78]. To switch the ferroelectric polarization of the multiferroic material, the capacitance must be charged from a power supply with a CMOS transistor (we will use the parameters for CMOS HP here). The switching occurs in a hysteretic manner and is characterized by the critical field $E_{mf}$ and remanent polarization $P_{mf}$. See parameter values in Table 3. The total charge that needs to be supplied is

$$Q_{mf} = P_{mf} w_S^2 + c_0 w_S V_{dd}. \quad (55)$$

The required thickness of the multiferroic is

$$d_{mf} = \frac{V_{dd}}{E_{mf}}. \quad (56)$$

The charging energy is

$$E_{mf} = Q_{mf} V_{dd}. \quad (57)$$

The charging time is

$$t_{mf} = \frac{Q_{mf}}{I_{dev}}. \quad (58)$$

and the magnetization switching time is

$$t_{mag} = \frac{\pi}{2\gamma B_{me}}. \quad (59)$$

The total switching time is the combination of the two. Another way of doing voltage-controlled switching is with an adjacent piezoelectric material. Changing the polarization in a piezoelectric material causes strain, and the stress at the interface switches magnetization in the ferromagnet by the magnetostrictive effect. In an example of switching using a piezoelectric material such as lead magnesium niobate-lead titanate (PMN-PT) [60], the switching also has a hysteretic character. The expressions are similar to (55)–(59) with subscript changed to “ms,” except the polarization is determined via the dielectric constant

$$P_{ms} = \varepsilon_0 \varepsilon_{ms} E_{me}. \quad (60)$$

We also describe here for completeness a similar magnetostrictive switching by the linear magnetoelectric effect [62]. The strength of coupling is expressed by the magnetoelectric coefficient (Table 3). However, none of the devices in the present study envision using this type of switching. The electric field in the piezoelectric is

$$E_{me} = \frac{V_{dd}}{d_{me}}. \quad (61)$$

The resulting magnetic field [62] is

$$B_{me} = \alpha_{me} E_{me}. \quad (62)$$

The induced polarization is

$$P_{me} = \varepsilon_0 \varepsilon_{me} E_{me}. \quad (63)$$

Another way of switching is by means of a voltage change of surface anisotropy [79]. We do not cover this method in this paper.

The estimates in this section are used in benchmarking multiple spintronic devices.

Note that we incorporate only the energy contribution of driving transistors, but not reading circuits (e.g., sense amplifiers). In some cases, that latter contribution can become significant.

**XI. SWITCHING TIME AND ENERGY FOR SPINTRONIC DEVICES**

In Section X, we calculated the switching time and energy for an intrinsic device switching magnetization. Now we expand it to calculating the performance of spintronic majority gate circuits. Table 9 specifies which method of controlled switching of magnetization is assumed, e.g., current controlled or voltage controlled, and therefore which estimates from Section X are used for the device’s intrinsic switching time and energy. For a few of the devices, their method of magnetization switching is specific, and is described below. As the reader can see, the magnetostrictive rather than multiferroic option for voltage-controlled switching was selected for the benchmarking since it gives slightly better projections. For some of the devices, we do not envision (indicated with N/A in
Table 9) a voltage-controlled option using the principle of the device operation relying exclusively on STT.

Here, we describe device-specific estimates of the switching time and energy. SMG uses the intrinsic values from Section X directly.

A. ASLD Intrinsic Values

The net electrical current flows from the top electrode to the ground and produces the spin polarization in the interconnect between nanomagnets. This current determines the Joule heating dissipation. The spin-polarized electrons diffuse in both directions between the two nanomagnets which causes switching of nanomagnets by spin torque. We introduce an additional factor of 1.5 to account for the spin-polarized diffusion current being smaller than the electrical current.

B. STT-DW Intrinsic and Circuit Values

The magnetization is switched by STT of electrons crossing a domain wall and thus causing its motion. The required current per unit length is (see Tables 3 and 4 for material and device parameters)

\[ I_{\text{on}} = 1.5I_{\text{dw}}d_{\text{in}} \]  

(64)

where factor 1.5 is introduced for the excess of the switching current over the critical current, and this current is passed through the magnetic wire of width \( F \). The speed constant corresponding to spin torque in domain walls is \( \nu_{\text{stt}} \)

\[ \nu_{\text{stt}} = \frac{\mu_B P_{\text{dw}}}{(eM_s)} \]  

(65)

The speed of domain walls varies and can be approximated by \( \nu_{\text{dw}} \)

\[ \nu_{\text{dw}} = 3\nu_{\text{stt}} \]  

(66)

The intrinsic device (a ferromagnetic wire with domain wall driven along it) switching time will be the time to move the domain wall past the magnetic tunnel junction (length \( 2F \)). The switching energy will be the energy supplied by the clock such that the domain wall receives sufficient current to switch

\[ t_{\text{int}} = \frac{2F}{\nu_{\text{dw}}}, \quad E_{\text{int}} = I_{\text{on}}w_3V_{dd}t_{\text{int}}. \]  

(67)

STT/DW is the only spintronic device envisioned with the \text{nand} (rather than \text{majority} gate) logic functionality. The interconnects for the device are the usual electrical ones. Their delay and energy proves to be small compared to intrinsic device values.

For the fanout-4 (FO4) inverter

\[ t_{\text{inv}} = t_{\text{int}} + t_{\text{ic}}, \quad E_{\text{inv}} = 4(E_{\text{int}} + E_{\text{ic}}). \]  

(68)

For the two-input \text{nand} gate with fanout-1

\[ t_{\text{nand}} = t_{\text{int}} + t_{\text{ic}}, \quad E_{\text{nand}} = E_{\text{int}} + E_{\text{ic}}. \]  

(69)

For the 1-b full adder, the critical path goes through two \text{nand} gates and the total energy is proportional to the area of all the \text{nand}s in the adder

\[ t_1 = 2t_{\text{nand}}, \quad E_1 = 14E_{\text{nand}}. \]  

(70)

C. SWD Intrinsic Values

We assume that the electrical signal exiting the magnetoelectric cell is a harmonic wave with a frequency \( f_{sw} = 100 \text{ GHz} \), the corresponding wavelength of spin waves is \( \lambda_{sw} = 30 \text{ nm} \), and the resulting speed of spin waves is

\[ \nu_{sw} = f_{sw}\lambda_{sw}. \]  

(71)

Then, the intrinsic switching time is estimated as

\[ t_{\text{int}} = \frac{10}{f_{sw}} \]  

(72)

and the interconnect delay is

\[ t_{\text{ic}} = \frac{2d_{\text{maj}}}{\nu_{sw}} \]  

(73)
D. STO Logic Intrinsic Values

The estimates for the device parameters follow the perpendicular STT series of equations in Section X, with the exception that we take a typical frequency of oscillations to be $f_{osc} = 30$ GHz, and assume that it has a switching time of

$$t_{int} = \frac{30}{f_{osc}}. \quad (74)$$

The interconnection between spin torque oscillators is done via spin waves. The interconnect delay is calculated via the same expression (73).

In the case of voltage-controlled switching, the energy estimates are obtained as in Section X. In the case of the current-controlled switching, the spin wave is excited by a magnetic field generated by a current in a wire. The estimate of the switching energy is based on the current required to produce $B_{wi}$ of the magnetic induction at a distance of one pitch of metal-1

$$I_{dev} = \frac{2\pi B_{wi} p_m}{(\mu \mu_0)}. \quad (75)$$

We use parameters from Table 3 here. The permeability of the substance surrounding the wire has been demonstrated to have values of 2–6; see [82]. Then, the dissipated energy in a transmission line with impedance of $Z = 50 \, \Omega$ is

$$E_{int} = I_{dev}^2 Z t_{int}. \quad (76)$$

E. NML Intrinsic Values

For NML [83], the switching time of one nanomagnet in the chain forming majority gates is taken as an empirical value $t_{nm} = 0.1$ ns [84]–[86], which presumably does not change much with the size. The number of nanomagnets (spaced at 2F center to center) across a majority gate is

$$N_{nm} = \frac{t_{maj}}{2F}. \quad (77)$$

We also assume that the interconnect between the majority gates requires one half of the number of nanomagnets as the path through a majority gate. Then, the intrinsic switching time and the interconnect delay are

$$t_{int} = t_{nm} N_{nm}. \quad (78)$$

In the case of voltage-controlled switching, the energy estimates are obtained as in Section X. In case of the current-controlled switching, the magnetic field from a set of electrical wires is applied to clock the nanomagnets; see Fig. 46. We take the wire width to be $p_m$, the wire pitch to be $2p_m$, and the aspect ratio of wires $AR = 3$ (corresponding to tall wires). The required current in a wire is

$$I_{dev} = \frac{2B_{wi} p_m}{(\mu \mu_0)}. \quad (79)$$

The resistance of the clocking set of wires covering the area is proportional to the area. Each set of wires is used to clock multiple gates simultaneously. To calculate the power dissipation of one majority gate, we substitute its area into the expression for resistance

$$R_{clk} = \frac{\rho a_{maj}}{p_m^2 \cdot AR}. \quad (80)$$

The energy required to switch for both the device and the interconnect delay is

$$E_{int} = t_{dev}^2 R_{coil}(t_{int} + t_{ic}). \quad (81)$$

For the case of voltage-controlled clocking of NML, we assume that the magnetoelectric (multiferroic or
magnetostrictive) material is driving the area of all nanomagnets in the majority gate

\[ a_{\text{NML}} = 2N_{\text{nm}}2F^2 \]  

and this area replaces \( w_3^2 \) in the expression for the energy [see (55)].

**F. Common Analysis of Spintronic Circuits**

After the intrinsic device switching time and energy are calculated, the treatment is similar for spintronic devices SMG, ASLD, SWD, NML, and STOlogic.

We assume that interconnects between gates take the same time to switch as connections within the gate, but they are driven by the energy in the gate (i.e., no additional energy per interconnect). It is only true for short enough interconnect between gates as specified by (2). It is applicable unless we explicitly state otherwise for a device

\[ t_{\text{ic}} = t_{\text{int}}, \quad E_{\text{ic}} = 0. \]  

One exception is NML, where the interconnect requires 1/2 of the time and energy as the intrinsic device (due to smaller number of nanomagnets)

\[ t_{\text{ic,NML}} = \frac{t_{\text{int,NML}}}{2}, \quad E_{\text{ic,NML}} = \frac{E_{\text{int,NML}}}{2}. \]  

An inverter can be accomplished with one magnetization switching terminal, but the energy is proportional to the number of outputs in a fanout-4 gate. Thus

\[ t_{\text{inv}} = t_{\text{int}} + t_{\text{ic}}, \quad E_{\text{inv}} = 4(E_{\text{int}} + E_{\text{ic}}). \]  

A NAND gate is implemented by a majority gate with three inputs. We assume that it takes the same time to switch as a single input, but the energy is proportional to the number of inputs

\[ t_{\text{nand}} = t_{\text{int}} + t_{\text{ic}}, \quad E_{\text{nand}} = 3(E_{\text{int}} + E_{\text{ic}}). \]  

The contributions of interconnects are accounted for in majority gates, except that a full adder requires an additional interconnect.

**G. STT Triad Circuit Values**

The switching time and energy of STT triad is a special case.

We start with the estimates for the switching time and energy for a triangular in-plane nanomagnet [see (50) and (51)] of side length 4.5F. The interconnect energy and delay are calculated like any other electrical interconnect; see Section IX. The gate switching time and energy contain a factor of 2, since it is necessary to reset the triangles before switching. In addition, the switching energy contains another factor of 2 for the two inputs

\[ t_{\text{nand}} = 2(t_{\text{int}} + t_{\text{ic}}), \quad E_{\text{nand}} = 4(E_{\text{int}} + E_{\text{ic}}). \]  

Additionally, a fanout-4 inverter requires a triangle per output with the corresponding multiplying factor in the switching energy

\[ t_{\text{inv}} = 2(t_{\text{int}} + t_{\text{ic}}), \quad E_{\text{inv}} = 16(E_{\text{int}} + E_{\text{ic}}). \]  

A 1-b full adder contains in total nine triad triangles and two output interconnects (for the sum and the carry) that contribute to the energy. The delay is defined by the critical path through six triad triangles

\[ t_1 = 6t_{\text{nand}} + t_{\text{ic}}, \quad E_1 = 9E_{\text{nand}} + 2E_{\text{ic}}. \]  

**XII. COMPARISON OF DEVICES**

First, we assemble the summary of intermediate results: the intrinsic device and interconnect times and energies for devices (as defined in Sections IX and XI). The estimates (Table 10) are performed assuming the use of magnetostrictive switching for those spintronic devices which can use it, and spin torque switching for those devices that are exclusively based on it. Zero switching energy of interconnects means that either this energy is neglected compared with the intrinsic device switching energy, or the energy to drive an interconnect is accounted for in the intrinsic device switching energy.

Now, we summarize the results for all circuits composed of the NRI devices under consideration. We plot the switching energy versus the switching delay of the three circuits: fanout-4 inverter, two-input NAND (see the Appendix), and a 32-b adder. The plots are done for various cases of magnetization switching. We note that these results are mostly affected by the estimates of intrinsic
device switching, as described in Sections IX–XI. The size and geometry of circuits produce a smaller (albeit noticeable) effect.

The most striking observation from these plots is that spintronic devices on the whole have longer switching delays and higher switching energies. (SpinFET is an exception, because its magnetic state is not being switched in the circuit operations. For cases considered in this paper, SpinFETs realize electronic circuits rather than spintronic circuits.)

The root cause for a longer delay is that the inherent time of magnetization propagation is longer than that of electrical switching. In other words, the typical speed of an electron ($\approx 10^5$ m/s) is much faster than the speed of a magnon ($\approx 10^3$ m/s). This remains true across many devices with different ways of switching. The situation with switching energy differs dramatically between voltage-controlled switching and current-controlled switching of magnetization. With current-controlled switching (Figs. 47 and 48), the switching energy of spintronic circuits is limited by the current dissipated energy (Joule heating), the product of current, voltage, and the switching time. It is much higher than the intrinsic energy of the magnetic state, thus spin torque switching is inefficient in this respect. One way to decrease this dissipated energy is to lower the operating voltage. We show the results (Fig. 47) with an extremely low supply voltage of 10 mV. In this range, the circuit operation may be disrupted by thermal noise, e.g., fluctuations of switching current. Even then, the switching energy of spintronic circuits is not

| device name  | Delay, int | Energy, int | Delay, ic | Energy, ic |
|--------------|------------|-------------|-----------|------------|
|              | units      | ps          | aj        | ps         | aj         |
| CMOS HP      | 0.25       | 19.63       | 0.18      | 20.16      |
| CMOS LP      | 92.08      | 3.32        | 66.20     | 3.40       |
| HomJTJFET    | 3.27       | 0.98        | 3.53      | 1.51       |
| HetJTJFET    | 0.33       | 3.93        | 0.35      | 6.05       |
| gnJTJFET     | 0.79       | 1.53        | 0.85      | 2.36       |
| GpJ          | 2.17       | 142.77      | 0.28      | 18.54      |
| BisFET       | 1.36       | 22.10       | 1.18      | 27.24      |
| SpinFET      | 1.02       | 30.08       | 0.44      | 18.54      |
| STT/DW       | 1762.90    | 111.06      | 0.02      | 0.00       |
| STMG         | 297.61     | 1.38        | 297.61    | 0.00       |
| STTtriad     | 298.03     | 10.92       | 0.02      | 0.38       |
| STOlogic     | 1000.00    | 351.60      | 80.00     | 0.00       |
| ASLD         | 205.16     | 108.20      | 205.16    | 0.00       |
| SWD          | 297.61     | 1.38        | 80.00     | 0.00       |
| NML          | 400.00     | 19.31       | 200.00    | 9.65       |

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**Table 10** Switching Delay and Switching Energy for Intrinsic Components and Interconnects of Devices for Magnetostrictive Switching

![Fig. 47. Energy versus delay of 32-b adders. Spintronic devices use current-controlled switching with $V_{dd} = 0.01$ V. The preferred corner is bottom left.](image1)

![Fig. 48. Energy versus delay of 32-b adders. Spintronic devices use current-controlled switching with $V_{dd} = 0.1$ V. The preferred corner is bottom left.](image2)
competitive with that of electronic ones. For a higher supply voltage, 100 mV, the switching energy is correspondingly ten times higher (Fig. 48).

With voltage-controlled switching (Figs. 49 and 50) the switching energy of spintronic circuits significantly improves and becomes competitive with that of electronic ones. (The exceptions are ASLD, STT/DW, and STO logic which cannot employ voltage control switching since they inherently rely on spin torque for operation.) The reason for this is that in both cases the energy is limited by charging a capacitor. Though the capacitances and operation voltages vary between devices, they are of the same order of magnitude (see Fig. 64). Magnetostriuctive (Fig. 50) switching results in somewhat better switching energy than multiferroic switching (Fig. 49). The switching speed still remains slower than that for electronic devices. The reason for this is that the speed is not limited by capacitor charging, but by a slower magnetization response to the magnetoelectric stimulus (see Section X). In our opinion, it is not a fundamental limitation. One should be encouraged to look for materials with faster magnetization dynamics as well as for other computational variables which can be switched faster (e.g., antiferromagnetic polarization).

Finally, we compare (Fig. 51) the benchmark results obtained in the present study with the ones reported at the 2011 NRI benchmarking workshop [88]. Some of the
devices’ benchmarks differ significantly. In some cases (e.g., BisFET), the reason is the different assumptions about device parameters ("on" current, voltage). In the case of STT/DW, the difference is due to a dramatic change in how it is used to implement logic circuits and also the fact that perpendicular magnetic anisotropy materials were used.

XIII. COMPUTATIONAL THROUGHPUT AND POWER DISSIPATION

The computational throughput is a measure of useful work performed by a circuit and is defined as a number of integer operations (32 bit additions in this case) per second per unit area. We estimate it as

$$T_{\text{add}} = \frac{1}{a_{32} t_{32}}.$$  \hspace{1cm} (91)

In the process of computation, the expended energy is dissipated as heat power density (W/cm²)

$$P_{\text{diss}} = T_{\text{add}} E_{32}. \hspace{1cm} (92)$$

Table 11 Summary of Comparison of Devices for Magnetostrictive Voltage-Controlled Switching

| device name | Area (µm²) | Delay (ps) | Energy (fJ) | Power density (W/cm²) | Throughput (Pops/s/cm²) | Thr@<10W/cm² (Pops/s/cm²) |
|-------------|------------|------------|-------------|-----------------------|------------------------|---------------------------|
| CMOS HP     | 63.0       | 84         | 2.48        | 46.5                  | 18.79                  | 4.04                      |
| CMOS LP     | 63.0       | 31331      | 0.42        | 0.0                   | 0.05                   | 0.05                      |
| HetJFET     | 84.0       | 1378       | 0.15        | 0.1                   | 0.86                   | 0.86                      |
| gnFET       | 84.0       | 331        | 0.23        | 0.8                   | 3.60                   | 3.60                      |
| Gpnl        | 46.7       | 110        | 15.49       | 301.5                 | 19.47                  | 0.65                      |
| BisFET      | 102.4      | 508        | 3.00        | 5.8                   | 1.92                   | 1.92                      |
| SpinFET     | 63.0       | 282        | 3.20        | 18.0                  | 5.63                   | 3.13                      |
| STT/DW      | 6.8        | 112820     | 50          | 6.5                   | 0.13                   | 0.13                      |
| STMG        | 3.1        | 38094      | 0.40        | 0.3                   | 0.84                   | 0.84                      |
| STT/Triad   | 37.2       | 114450     | 13.04       | 0.3                   | 0.02                   | 0.02                      |
| STOlogic    | 6.2        | 69120      | 101         | 23.5                  | 0.23                   | 0.23                      |
| ASLD        | 2.1        | 26261      | 20.78       | 38.2                  | 1.84                   | 0.48                      |
| SWD         | 2.1        | 12084      | 0.26        | 1.1                   | 3.99                   | 3.99                      |
| NML         | 1.0        | 38400      | 1.24        | 3.1                   | 2.51                   | 2.51                      |

Fig. 53. Energy versus delay of inverters with fanout-4. Spintronic devices use current-controlled switching with $V_{\text{dd}} = 0.01$ V. The preferred corner is bottom left.

Fig. 54. Energy versus delay of two-input NAND gates. Spintronic devices use current-controlled switching with $V_{\text{dd}} = 0.01$ V. The preferred corner is bottom left.
Since leakage directly determines the standby power, it is on its own a metric. Those devices with significant leakage will need power supply gating and this will add to their power. In this calculation, we only account for the active power and for the moment we neglect the standby power (e.g., from the leakage currents). The activity factor is determined by the logic function of the ripple-carry adder and is thus equal to 1/32. We do not introduce additional activity factors which may be pertinent to specific usage models of circuits. We also do not incorporate any pipelining in this calculation, even though some logic technologies not constrained by power dissipation may produce higher computational throughput with pipelining.

For the sake of simplicity, we do not consider the use of multiphase clocks.

As we will see from Fig. 49, some of the beyond-CMOS devices have exceptionally low power dissipation and thus are useful for mobile computing. Benchmark numbers for other devices result in a much higher dissipation. Meanwhile, there is a practical upper limit to the power dissipation set by the ability of a heat sink to remove power. In this study, we (somewhat arbitrarily) set the power density limit ("cap") to $P_{\text{cap}} = 10 \text{ W/cm}^2$. Note that it is not the whole power dissipated on chip, since we have not included the contribution of: 1) long interconnects (longer than bit-to-bit); 2) the clock distribution circuits; and
3) other systems on chip. If the dissipated power exceeds the limit, one needs to run the circuits slower or spread them apart, thereby decreasing useful throughput.

Therefore, we postulate as a figure merit the computational throughput with a limit on (capped) power and area (fixed)

\[ T_{\text{cap}} = T_{\text{add}} \min \left( 1, \frac{P_{\text{cap}}}{P_{\text{diss}}} \right). \]  

(93)

The relationship between capped throughput and dissipated power is shown in Fig. 52. The unit of throughput there is peta-integer-operations per second (PIOPS) per square centimeter. We see that only the heterojunction TFET is expected to provide higher throughput than high-performance CMOS (and do it with lower dissipated power). BisFET and SpinFET have lower but comparable throughput at the same power. Other tunneling FETs as well as a few of the spintronics devices (e.g., SWD and NML) provide comparable throughput at significantly lower power.

We remind the reader that spintronic logic has the major attribute (advantage) of nonvolatility and reconfigurability.

Alternatively, these data are also summarized in Table 11.
XIV. DISCUSSION OF BENCHMARKS

We observe that two major conclusions are derived from this study.

1) For electronic devices, the most promising avenue of improvement is decreasing the operational voltage. Tunneling FETs seem to be the leading option.

2) Spintronic devices have an advantage in implementing complex logic functions with a smaller number of devices/elements. The key factor toward making them competitive with CMOS is using voltage-controlled switching.

We would like to stress two additional advantages of spintronic devices that are not captured by the current set of benchmarks: nonvolatility and reconfigurability. In order to utilize these advantages new types of circuits need to be designed.

To make the task tractable, we considered only a small set of circuits. In order to cover all elements necessary for an arithmetic logic unit (ALU), one needs to extend this treatment to state elements, latches, multiplexors/demultiplexors, etc.

XV. CONCLUSION

An approach with simple but general estimates of benchmark parameters has been described that is applicable to multiple devices and provides a consistent and
reproducible methodology that can be used in the benchmarking of NRI devices. By publishing this paper, the authors solicit inputs and suggestions from the researchers in the field in order to find uniform consensus on the way to do benchmarking for beyond-CMOS devices.

**APPENDIX**

This section contains the comparison plots Figs. 53–67 for devices in addition to those in the main text. These provide a bigger perspective on the relative differences among the devices. Note from the scale of the plots in Figs. 47–51, and 53–60 that the switching time and energy for the intrinsic devices or the smaller circuits (the inverter and NAND) are 100–1000 times smaller than that of the corresponding 32-b adders. This is naturally explained by the number of bits in the adder and a more complex structure of each bit of an adder. Apart from the difference in the scales, the relative positions of various beyond-CMOS devices are similar (but not the same):

compare, e.g., Figs. 47 and 53. This is the manifestation of the fact that the switching of intrinsic devices and interconnects, for a circuit based on a certain device, is limited by the same switching phenomena. For example, in electronic circuits, the intrinsic devices operate by charging a gate capacitor and the interconnects pass the signals by charging the parasitic and wire capacitances. Similarly, in nanomagnetic logic, both intrinsic devices and interconnects operate by flipping a neighbor nanomagnet. Thus, the device and circuit benchmarks are not exactly the same, but approximately proportional. The departures from this rule are the spintronic majority gates and GpnJ: they have a smaller ratio of an adder to intrinsic device delay (Fig. 61). This is the result of a more efficient architecture requiring fewer gates for the same function. Also, the ratio of a circuit and device energy is higher for STTTriad and STT/DW (Fig. 62) This is the result of a less efficient architecture that can only be implemented for an adder.

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