A Low-Phase-Noise CMOS Ring Voltage-Controlled Oscillator Intended for Time-Based Sensor Interfaces

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ABSTRACT We describe in this paper an improved ring voltage-controlled oscillator (VCO) showing a reduced phase noise while allowing an extended frequency tuning range. The phase noise improvement is obtained through the minimized contribution of tuning line noise while maintaining a rail-to-rail swing. The proposed VCO features a linear tuning characteristic yielding a constant gain over a wide range of operating frequencies. An analytical model is extracted resulting in closed-form expressions for the VCO phase noise. Employing the analytical expressions, the contributed noise and phase noise limitations are fully addressed, and all the effective factors are investigated. The VCO prototype was fabricated in a 0.35 \( \mu \)m CMOS process. It consumes 0.903 mW from a 3.3 V supply when running at its maximum oscillation frequency of 9.37 MHz. The measured VCO phase noise is -147.57 dBc/Hz at 1 MHz offset from the 9.37 MHz oscillation frequency, and the circuit occupies a silicon area of 0.005 mm\(^2\). A state-variable Matlab\textsuperscript{®} model of a time-based sensor interface has been developed including the impact of phase noise nonideality. The system-level simulations demonstrate that the PLL-based sensor interface exploiting the proposed VCO characteristics can achieve an 88.43 dB signal-to-noise ratio over a 1-kHz bandwidth.

INDEX TERMS Sensor interface, ring oscillators, voltage-controlled oscillator, phase noise, linear characteristics.

I. INTRODUCTION The voltage-controlled oscillator (VCO) is a critical circuit in modern analog and mixed-signal integrated system designs such as phase-locked loops (PLLs), clock/data recovery, frequency modulation/demodulation, on-chip clock distribution, and synchronizing circuits [1], [2], [3], [4]. Over the past decades, the semiconductor industry has been directed towards smaller technologies that are especially effective for digital circuits while raising some difficulties in designing analog systems [5], [6]. Supply voltage reduction, weak intrinsic transistor properties (e.g., lower gain and devices’ mismatch), large power and chip area result in poor portability of purely analog solutions to other technology nodes [7]. Therefore, time-based and digitally-oriented structures became increasingly popular among electronic research trends.

Moreover, VCO-based architectures are of great interest in time-based integrated circuits (ICs) such as time-domain comparators, analog-to-digital converters (ADCs), time to digital converters, time-based sensor interfaces, etc. This stems from the fact that VCOs offer highly digital, energy-efficient, and scalable solutions [8]. Also, they realize relatively simple configurations of multi-bit noise shaping in A/D conversion or quantizer in delta-sigma modulator [9], [10]. Fig. 1 conceptually illustrates the VCO’s function in two important types of time-based sensor interfaces or sensor to digital converters. The inherent first-order noise-shaping
Usually employed [20]. Although the VCO in a loop ensures a closed-loop interface architecture depicted in Fig. 1(b) is VCO-based sensor interface shown in Fig. 1(a), the VCO's limited nature of voltage-to-time conversion provokes a linearity issue for timing in digital circuits that are widely used in industrial platforms.

The most common techniques to implement VCOs are ring structures, LC resonant configuration, or relaxation circuits [15], [16], [17]. LC-VCOs exhibit better phase noise performance owing to the high Q resonator. However, besides the limited tuning range of these structures, adding high-performance bulky passive devices (such as inductors) to a CMOS process leads to chip complexity, and area and cost inefficiency [15]. On the contrary, ring VCOs are a popular alternatives in scaled CMOS technologies since they offer a wide tuning range, less die area, straightforward integrated design, multi-phase output capability, and good power performance [18]. Consequently, a ring-type VCO is a promising approach for voltage-to-time conversion, frequency translation, and generating required periodic signals for timing in digital circuits that are widely used in industrial platforms.

However, nonlinear performance and poor phase noise are the key issues in ring VCOs. For instance, the nonlinear nature of voltage-to-time conversion provokes a linearity issue in a time-domain comparator, and the VCO phase noise has a great impact on its resolution [8], [21]. Besides, the performance of VCO-based ADCs is severely distortion limited by VCO gain variation (tuning nonlinearity) that causes an inter-stage gain error [22]. Moreover, in an open-loop VCO-based sensor interface shown in Fig. 1(a), the VCO’s nonlinearity leads to the appearance of harmonic spurts in the output spectrum and limits the overall system signal-to-noise ratio (SNR) [19], [23]. To tackle this issue, the closed-loop interface architecture depicted in Fig. 1(b) is usually employed [20]. Although the VCO in a loop ensures higher linearity, the operating frequency range is narrowed, and the additional feedback network results in a low conversion speed, a larger area, and an increased power budget [24]. The limiting factor in these close-loop time-based interfaces is the VCO phase noise [20]. As a result, an on-chip VCO design with improved linearity correction, less gain variations, low phase noise, and full-swing is significantly required in any analog/digital applications.

Generally, there are two types of ring VCOs: single-ended and differential. Single-ended VCOs are widely used in digital nature applications due to their low complexity, smaller area, lower temperature coefficient, and wider tuning range. Also, a differential ring VCO may show larger phase noise compared to a single-ended VCO at the same power, operation frequency, and the number of delay stages. While, its phase noise performance could even be worse without tail current noise minimization technique [25]. In contrast, differential VCOs offer better common-mode noise rejection with a lower sensitivity to substrate and supply noises. In a single-ended ring VCO, these sensitivities can be reduced to some extent through proper layout design consideration. In addition, in the closed-loop time-based sensor interface shown in Fig. 1(b), the common-mode sensitivity of the single-ended VCO can be suppressed by having two identical oscillators laid out close together. It is due to the fact that when two oscillators operate in the same physical environment, the related noise appears as a common mode perturbation on their oscillation frequencies [24]. Therefore, the above factors should be considered when selecting the appropriate design of ring VCO for a particular application.

In an attempt to obtain a VCO with low phase noise, authors in [26] promote rail-to-rail voltage swings. However, their employed delay cells limit the noise performance by injecting a substantial noise during the VCO’s transition periods. Another study presented in [15] focused on reducing injected channel thermal noise in transistors during VCO’s output transitions. Nevertheless, the VCO performance remains limited due to the low-frequency tuning range and the large power consumption. A band switch function is employed in [2] to suppress the control line noise and compensate for tuning range. However, the additional mechanism for band switch control increases the overall phase noise while suffering from power overhead. An ultra-low-power ring VCO was reported in [27]. It uses a differential delay cell to generate negative conductance without requiring the cross-coupled latch. This design suffers from an unattractive phase noise performance, a low frequency tuning range, and a large occupied area due to the passive components used in the delay cell implementation.

This work presents a compact, wide-swing, enhanced phase-noise, and low-power CMOS ring VCO. The delay elements used in the proposed VCO show a full-swing output, a linearized characteristic, and a steady gain. A theoretical analysis considering the impact of intrinsic and extrinsic sources of noise has been developed to study the VCO phase noise. Also, the effectiveness of this architecture is validated through a Matlab/Simulink model of a closed-loop

**FIGURE 1.** Block diagram of two types of VCO-based sensor interfaces: (a) the count-based open-loop [19], and (b) the PLL-based closed-loop sensor interface [20].
PLL-based sensor interface. The rest of the paper is organized as follows: Section II describes the general phase noise definitions for ring-type VCOs. The design and the theoretical analysis of the proposed VCO architecture are revealed in Section III. Section IV presents the measurement results of the fabricated VCO, while Section V discusses the proposed VCO’s performance compared to the prior art and examines its potential in a time-based sensor interface by employing a state-variable Matlab® model. The conclusion is drawn in Section VI.

II. PHASE NOISE IN THE RING OSCILLATOR DESIGN

There is an inherent trade-off between ring oscillators’ diverse properties, including phase noise, tuning range, linearity, gain, voltage swing, power dissipation, and supply voltage. In a practical VCO, noise sources add uncertainty to zero crossing times and create a variable interval between transitions known as jitter. As a result of the time-domain deviation from perfect periodicity, oscillation frequency varies from the ideal constant, causing a nonuniform output phase. In the frequency domain, this short-term instability or random fluctuations in the phase of an output signal is defined as phase noise [28]. Phase noise induces various interferences and errors in integrated circuits’ functionality, so it is a leading concern in a VCO circuit design.

Several models have been developed to quantify these fluctuations, analyze the phase noise of the oscillator, and characterized it in terms of the normalized single side-band (SSB) noise spectral density [25], [28], [29], [30]. According to the type of devices used to implement the VCO, the contributing noise sources can be thermal noise of parasitic resistance, thermal noise of transistors’ channels, and transistors’ flicker noise (1/f noise) which is responsible for the phase noise at low frequency. Since the band of interest for most applications is usually dominated by white noise and flicker noise, the VCO phase noise power spectral density (PSD) can be represented as a simplified model of [13], [31]

\[ L(\Delta f) = \frac{b_{-2}}{\Delta f^2} + \frac{b_{-3}}{\Delta f^3}, \]

where \( b_{-2} \) and \( b_{-3} \) are the noise levels for the white and the flicker noise dominated regions, respectively.

As noted earlier, phase noise and jitter are different ways of quantifying the same phenomenon. Several attempts have been made to link these two parameters, resulting in a direct relationship that holds for white noise sources. Therefore, to analyze the effect of white noise on the phase noise of a VCO, the time-domain jitter calculation method is often used [30], [32]. In the presence of 1/f noise, however, the assumption of uncorrelated sources of jitter between successive oscillator periods is no longer valid [25]. So, it is difficult to determine the correlation between the jitter of transitions, induced by low-frequency noise sources, over multiple cycles. Therefore, to account for flicker noise, a straightforward circuit analysis on random VCO modulation is preferred [30].

The output oscillation frequency of a VCO is determined by its control voltage through the VCO gain (or sensitivity), \( K_{VCO} \). Suppose an injected voltage noise at the tuning node of the oscillator. For a given noise amplitude, the noise in the output frequency is amplified by \( K_{VCO} \). Clearly, it will affect the noise spectral density and thereby the phase noise behavioral model. Accordingly, the flicker noise impact on phase noise can be determined by considering the direct modulation of oscillation frequency caused by the circuit transfer function. As any noise generated in the control scheme can provoke additional phase noise, it is necessary to examine the disturbance of the output phase and frequency arising from the circuit’s integrated noise and the extrinsic noise accompanied by the control voltage. We leverage these principles to find the phase noise expression for the proposed VCO, which is described in detail in section III-C.

III. PROPOSED VCO ARCHITECTURE

Fig. 2(a) presents the architecture of the proposed VCO. It consists of five delay cell stages in addition to a buffer at the output of the VCO to sharpen the generated signal and drive the VCO load. The implementation of the proposed linearized delay cell is illustrated in Fig. 2(b). In each current-starved delay cell, the control voltage \( V_{\text{cont}} \) is applied to the voltage-controlled current source \( M_{P1} \) and the resulting current, \( I_{\text{cont}} \), is mirrored to the inverter (constructed from \( M_{P4} \) and \( M_{N4} \)) through the current mirror \( M_{N1}, M_{N2}, \) and \( M_{P2} \). The replica current source \( M_{P4} \) in each stage dynamically biases the current-starved inverter and avoids current variation at \( I_{\text{cont}} \) which may lead to some linearity error. Also, the

**TABLE 1. Aspect ration of the used transistors.**

| Transistor | W/L (μm) | Transistor | W/L (μm) |
|------------|----------|------------|----------|
| \( M_{P1} \) | 4/7      | \( M_{N1} \) | 5/0.5    |
| \( M_{P2} \) | 8/4      | \( M_{N2} \) | 5/0.5    |
| \( M_{P3} \) | 5/4      | \( M_{N3} \) | 3/0.5    |
| \( M_{P4} \) | 5/5      | \( M_{N4} \) | 2/5      |
replicated current mirror is chosen to transfer the current and clamp the voltage of nodes with high parasitic capacitance and assure that currents in each stage are equivalent and a full swing can be attained at the output of the delay cell.

The target point of this VCO design is to generate pulse signals up to 10 MHz; thus, five delay cells \(N = 5\) are found to be sufficient to cover this range of frequency. Also, fewer number of delay cells mitigates phase errors that might be added due to the mismatch of delay cells [23]. Transistors’ aspect ratios shown in Table 1 are considered for the constituent transistors of the VCO delay cells.

A. LINEARIZATION

For a single-ended VCO, the oscillation frequency is primarily realized by the number of stages \(N\) and the average propagation delay \(t_p\) of delay cells, as

\[
f_{osc} = \frac{1}{t} \simeq \frac{1}{2N \cdot t_p}. \tag{2}\]

The propagation delay is measured when the output signal crosses the toggle point, which is assumed to be in the middle of transition at \(V_{DD}/2\). According to the proposed design, the \(j\)th delay cell can be viewed as the operation of an inverter with a pull-up and pull-down current supplies, \(I_{P_j}\) and \(I_{N_j}\) respectively. So, the oscillation frequency in the \(j\)th delay cell of an \(N\)-stage ring VCO can be calculated as [30]

\[
f_{osc} = \frac{2}{V_{DD} \cdot C_{tot}} \left( \sum_{j=1}^{N} \frac{1}{I_{N_j}} + \frac{1}{I_{P_j}} \right)^{-1}, \tag{3}\]

where \(C_{tot}\) is the total parasitic capacitance seen at the output of each delay element [32].

Supposing \(I_{N_j} \simeq I_{P_j} \simeq I_{out}\), the nominal frequency of oscillation is given by

\[
f_{osc} = \frac{I_{out}}{N \cdot V_{DD} \cdot C_{tot}}. \tag{4}\]

Therefore, the output frequency of a ring VCO is directly related to the current supplied to the inverter branches. Fig. 2(c) shows the conventional current-starved delay stage without linearization, where the control voltage applied to the pull-up PMOS (\(M_{P3}\)), and \(M_{N3}\) remains always on. In this design the gate-source voltage of \(M_{P3}\), \(V_{GS_{P3}}\), determines the VCO control voltage and the current flowing through it is related to \(V_{GS_{P3}}^2\). This results in a nonlinear output current with respect to \(V_{cont}\), and hence a nonlinear output frequency. Thus, to enhance the linearity of the \(f_{osc} - V_{cont}\) characteristic in a VCO, a linear current (with \(V_{cont}\) variation) should be supplied to the inverter stacks of the delay cells.

In the proposed delay cell implementation, shown in Fig. 2(b), this nonlinear circuitry is rectified by means of entering \(V_{cont}\) to a voltage-controlled current source, \(M_{P1}\), and using a current mirror biased in strong inversion. As depicted in Fig. 3(a), owing to the saturation-operating of \(M_{P1}\), the resulting control current, \(I_{cont}\), shows a nonlinear behavior with \(V_{cont}\). To compensate for this nonlinearity, the current mirror transistors are designed to transfer a linear biasing voltage (\(V_{CP}\) or \(V_{CN}\)) as functions of \(V_{cont}\) to the load transistors \(M_{P2}\) or \(M_{N3}\) in the pull-up or pull-down operation, respectively.

Considering the pull-up network activation moment, the load transistor \(M_{P3}\) is biased in the triode region, and its drain-source current equals \(I_{out}\). So, the output current of the proposed VCO is linearly related to its \(V_{GS_{P3}}\) and, hence, to its bias voltage \(V_{CP}\) (see Fig. 3(b)). This feature, along with the linear behavior of \(V_{CP}\) versus the controlling voltage \(V_{cont}\) (see Fig. 3(c)) ensures that the proposed VCO maintains a linear relationship between \(I_{out}\) and \(V_{cont}\) and controls the frequency response nonlinearity. Fig. 4 shows the operation frequency of the proposed VCO with and without the linearization versus its control voltage. As can be seen, a good enhancement in the VCO linearity compared to the design without the proposed linearization is obtained.

B. VCO GAIN

The VCO’s gain is defined as

\[
K_{VCO} = 2\pi \frac{\partial f_{osc}}{\partial V_{cont}}. \tag{5}\]

Since the propagation delay time is estimated by the average output tail current going through the output capacitance,
the gain can be expressed as

$$K_{\text{VCO}} = 2\pi \frac{\partial I_{\text{out}}}{2 \cdot N \cdot V_{\text{sw}} \cdot C_{\text{tot}} \cdot \partial V_{\text{cont}}}.$$  \hspace{1cm} (6)

where $V_{\text{sw}}$ is the voltage swing of $V_{\text{out}}$. It is noteworthy that $V_{\text{sw}}$ may be reduced at a quite small $I_{\text{out}}$ due to slowed swing and increased voltage headroom of MOS transistors. Since the minimum operation mode in the proposed VCO is around 100 kHz, $V_{\text{sw}}$ can be assumed to be independent of the bias current and $V_{\text{cont}}$ at such range. On the other hand, in contrast to some conventional ring VCOs which are tuned by supply voltage variation, the proposed delay cell boosts the output swing by coupling the control signal to the gate of the current source transistor, $M_{\text{P1}}$. This bias-controlled voltage/current configuration is optimized in such a manner that the current mirror transistors remain in the saturation region for the entire control voltage range and the load transistors in the inverter tail make a narrow voltage headroom. Hence, a maximized voltage swing and a wide tuning range are obtained.

Therefore, the current-source biasing leads to a high steepness in transition slope, faster transition, output swing augmentation, and tuning range improvement. These features in addition to the optimized MOS sizing diminish the VCO gain. As explained in section II, reducing the gain can decrease the phase fluctuation due to low-frequency noise in components and the control terminal. However, to achieve a reasonably wide tuning range, a large $K_{\text{VCO}}$ is required [2]. Thus, for applications that require low phase noise and a wide tuning range, manufacturers typically design oscillators with a moderate gain and a large input voltage range to satisfy these conflicting requirements at the cost of power consumption. Lowering the $K_{\text{VCO}}$ has a minimal impact on the functionality of the proposed VCO since the required frequency tuning range is only from 0.01 MHz to 10 MHz over a 2 V input range.

C. NOISE ANALYSIS

To derive the proposed VCO’s noise contribution, the generated noise by means of each delay stage has to be first calculated. Likewise, the extrinsic noise at the control line should be included in the total noise associated with the circuit. The noise in the MOSFETs can be referred to the gate as a series noise voltage source with a PSD of $\nu_{\text{SN}}^2$ (or equivalently noise current source $\overline{I}_n$ across the drain) [29]. By considering the $M_{\text{P1}}$ reflected current to the current-starved inverter stacks, the equivalent noise transfer model of the proposed delay cell can be illustrated as shown in Fig. 5. It is worth mentioning that pull-up and pull-down currents incorporate the uncorrelated noise effect of $M_{\text{P1}}$ and the current mirror transistors.

1) PHASE NOISE DUE TO WHITE NOISE

The uncertainty in propagation delay of the proposed VCO can be modeled in the output current $I_{\text{out}}$ across the $C_{\text{tot}}$. This current is accompanied by a noise current source with a white noise spectral density of $S^w_{\text{VCO}} = \overline{I}^2_n = 4kBT\gamma g_m$, where coefficient $\gamma$ is typically equal to 2/3 for long-channel transistors. $\overline{I}^2_n$ would result in a Gaussian distribution of the propagation delay ($t_p$), which can be referred to as timing jitter. The total variance of the period jitter in view of the uncertainty in rising edge ($t_{\text{rise}}$) and falling edge propagation delay ($t_{\text{fall}}$) can be calculated as

$$\sigma^2_t = N \cdot \left[ \sigma^2_{\text{rise}} + \sigma^2_{\text{fall}} \right].$$  \hspace{1cm} (7)

where the variance of the jitter due to the uncorrelated white noise is $\sigma^2_{\text{lp}} = \frac{\overline{I}^2_n}{2I_{\text{out}}} \cdot f_p$ [32].

Using equations (7) and (2), the total period jitter approximated as

$$\sigma^2_t = \frac{2 \cdot k_B \cdot T}{I_{\text{out}} \cdot f_{\text{osc}}} \left[ \frac{\gamma_n}{(V_{\text{DD}} - V_{\text{thp}})} + \frac{\gamma_p}{(V_{\text{DD}} - V_{\text{thp}})} \right].$$  \hspace{1cm} (8)

The general relationship between phase noise and jitter, where the phase noise is dominated by white noise, is [14], [20], [30]

$$\sigma^2_c = \mathcal{L}(\Delta f) \cdot \frac{\Delta f^2}{f_{\text{osc}}^3}.$$  \hspace{1cm} (9)

Therefore, the SSB phase noise of VCO due to white noise can be estimated as

$$\mathcal{L}(\Delta f) = \frac{2k_B T}{I_{\text{out}}} \cdot \frac{f_{\text{osc}}^2}{(\Delta f)^2} \left[ \frac{\gamma_n}{(V_{\text{DD}} - V_{\text{thp}})} + \frac{\gamma_p}{(V_{\text{DD}} - V_{\text{thp}})} \right].$$  \hspace{1cm} (10)

2) PHASE NOISE DUE TO FLICKER NOISE

Flicker noise should be interpreted differently than white noise since its fluctuation rate is much lower than the oscillation frequency, and it relies on distinct mechanisms of phase noise...
noise and jitter [30]. From the principal analysis, explained in section II, input noises can be multiplied with the modulation sensitivity, yielding the frequency deviation that can be translated to an equivalent RMS phase deviation. Therefore, the SSB spectral density caused by a given noise in the VCO can be written as [30]

\[
\mathcal{L}(\Delta f, K_{\text{VCO}}) = S_{\text{in}}(\Delta f) \cdot \frac{K_{\text{VCO}}^2}{4 \cdot \Delta f^2} = \frac{(\nu_{\text{nt}})^2 \cdot K_{\text{VCO}}^2}{4 \cdot \Delta f^2},
\]  

(11)

where \( \nu_{\text{nt}} \) represents voltage noise sources in series with circuit branches. It comprises the channel integrated noise as well as the external noise at the VCO tuning node, which modulate the carrier frequency.

The delay is directly modulated by the flicker noise associated with pullup and pulldown current supplies. Therefore, according to (3) and (11), the equivalent SSB phase noise due to flicker noise contribution can be written as [30]

\[
\mathcal{L}(\Delta f, K_{\text{VCO}}) = S_{\text{in}}^{1/f}(\Delta f) \cdot \frac{K_{\text{VCO}}^2}{4 \Delta f^2} = \frac{1}{4 \Delta f^2} \left( \frac{f_{\text{osc}}}{2 \cdot N \cdot I_{\text{out}}} \right)^2 \cdot \left( \frac{I_{\text{out}}^2}{I_{\text{osc}}^2} \right) \approx \frac{1}{4 \Delta f^2} \cdot \left( \frac{f_{\text{osc}}}{2 \cdot N \cdot I_{\text{out}}} \right)^2 \cdot \left( \frac{I_{\text{out}}^2}{I_{\text{osc}}^2} \right),
\]  

(12)

where \( S_{\text{in}}^{1/f}(\Delta f) \) is spectral density of flicker noise in the inverter line current and \( K_T \) is the sensitivity of \( f_{\text{osc}} \) to the pull-up (or pull-down) current.

Concerning the control-line noise contribution in the phase noise of the VCO, an extrinsic noise coming from other components or circuitry with a PSD of \( v_{\text{nt}}^2 \) has been assumed at the tuning gate of \( M_{P1} \). This noise will be added to \( M_{P1} \) voltage noise (\( \nu_{\text{nt}} \)) and mirrored to the inverter line current noise with the mirroring factor of the \( K_m \). As a result, the total input current noise density is arisen from the current fluctuations of inverter tail transistors, controlling PMOS, and the extrinsic noise injected into the tuning node. Therefore, the SSB phase noise of \( N \) stage VCO can be calculated as

\[
\mathcal{L}(\Delta f, K_{\text{VCO}}) = \frac{1}{4 \Delta f^2} \left( \frac{f_{\text{osc}}}{2 \cdot N \cdot I_{\text{out}}} \right)^2 \cdot N \left[ \left( \frac{I_{\text{out}}^2}{I_{\text{osc}}^2} \right)^2 + \frac{K_{\text{VCO}}^2}{4 \Delta f^2} + \frac{I_{\text{out}}^2}{I_{\text{osc}}^2} \right].
\]  

(13)

The MOSFET flicker noise PSD in the active region is \( \nu_{\text{nt}}^2 = \frac{K_f}{2 \cdot f_{\text{osc}} \cdot \Delta f} \), where \( K_f \approx 10^{-25} (\text{V}^2/\text{Hz}) \) is a process dependent constant and \( K_f \) is usually lower than \( K_N \). By substituting the equivalent current noise \( \nu_{\text{nt}}^2 = g_{mn}^2 \nu_{\text{nt}}^2 \) in equation (13), the SSB phase noise caused by flicker noise can be described as

\[
\mathcal{L}(\Delta f, K_{\text{VCO}}) = \frac{1}{16 \cdot N \cdot I_{\text{out}}^2} \cdot \frac{f_{\text{osc}}}{(\Delta f)^2} \cdot \left[ \frac{2 \cdot I_{\text{out}}}{I_{\text{osc}}} \cdot \frac{K_{\text{VCO}}^2}{4 \Delta f^2} + \frac{K_{\text{VCO}}^2}{4 \Delta f^2} + \frac{\nu_{\text{nt}}^2}{I_{\text{osc}}^2} \right] + \mu_m \cdot \frac{K_{\text{VCO}}^2}{I_{\text{osc}}^2} + \frac{K_{\text{VCO}}^2}{I_{\text{osc}}^2} + \frac{I_{\text{out}}^2}{I_{\text{osc}}^2} + \frac{K_{\text{VCO}}^2}{4 \Delta f^2} + \frac{I_{\text{out}}^2}{I_{\text{osc}}^2}.
\]  

(14)

Consequently, equation (14) combined with (10) approximate the total phase noise characteristics of the proposed VCO. Usually phase noise is expressed in decibels (dB) as \( 10 \cdot \log(\mathcal{L}(\Delta f)) \), and its units are dB below the carrier in a 1 Hz bandwidth, generally abbreviated as dBc/Hz [31].

As specified in the analytical model equations (10) and (14), the white and flicker phase noise are inversely proportional to the drain current of MOSFETs in the inverter stack. This is because the delay is directly affected by the noise associated with the transistors connected to the output nodes [15]. Therefore, as the current noise associated with the current mirror transistors is reflected to the inverter with a \( K_m \) of less than one, the noise originating from those MOSs is not included in the model to simplify the analysis.

At the low offset frequency, the flicker noise of transistors used to implement the delay element is the dominant close-in phase noise source. Generally, transistors operating in a periodically stable region have more contribution to the circuit phase noise than transistors functioning in a switching mode. Thus, transistors composing the current source (\( M_{P1} \)), and inverter (\( M_{P2}-M_{N4} \)), which run in a period stable state, generate more \( 1/f \) noise. This impact was reduced by adopting PMOS transistors for input controlling source since holes are less likely to be trapped and leads to inherent lower flicker noise than NMOS transistors. Also, the transistors’ sizes are selected large enough with respect to the \( I_{\text{out}} \) and \( f_{\text{osc}} \).
The package is soldered to a custom printed-circuit board (PCB) for the test. Decoupling capacitors with values of 0.1 μF and 10 μF are utilized to filter the power lines. Fig. 6(b) illustrates the oscilloscope transient waveform of the proposed VCO’s output signal at a control voltage of 0 V and the maximum oscillation frequency.

The simulated and measured oscillation frequency and its corresponding core power consumption of the integrated VCO as a function of its tuning voltage are depicted in Fig. 7(a). The proposed VCO visually exhibits improved linear performance. The simulated and measured nonlinearity error over the tuning range is presented in Fig. 7(b), yielding a maximum error of 0.8% and 0.9%, respectively. As can be seen in the figure, nonlinearity might be increased for \( V_{\text{cont}} \geq 2 \) V.

The VCO was designed to generate an output frequency between 0.01 MHz and 10 MHz for a control voltage varying from 0 to 2 V. However, the measured output is from 0.01 up to 9.37 MHz resulting in a tuning range, \( TR_f \), of 199.5%. This slight reduction in the maximum measured frequency is due to process variations and the parasitic capacitances from PCB traces and the coaxial cable in the signal path.

Fig. 8 shows the measured VCO phase noise behavior, where it exhibits -87.69, -114.87, -145.80, and -147.57 dBc/Hz at 1 kHz, 10 kHz, 100 kHz, and 1 MHz offset from 9.37 MHz carrier, respectively. Furthermore, it shows the measured RMS jitter at 1 MHz bandwidth of integration equal to 17.64 ps (or 1.039 mrad). Since SSB phase noise follows a slope of -30 dB/dec up to 100 kHz offset frequency, we can conclude that flicker noise is the main contributor to the proposed VCO’s phase noise, as was expected based on its operating frequency range. In addition, the measured spectrum of the presented VCO circuit, when tuned to generate a maximum frequency of 9.37 MHz (with \( V_{\text{cont}} = 0 \) V), is shown in Fig. 9(a). Fig. 9(b) illustrates the output signal power of the proposed VCO corresponding to the operating frequencies over a control voltage varying from 0 to 2 V. The results include the loss associated with the cable and interfaces.

IV. MEASUREMENT RESULTS

The proposed ring-VCO is designed and fabricated using a 0.35 μm standard CMOS technology with a supply voltage of 3.3 V. The chip micrograph of the proposed linear ring VCO prototype, which is a part of a monitoring and readout circuit in a projected industrial sensor interface, is shown in Fig. 6(a). The VCO occupies an area of 0.005 mm\(^2\) with a form factor of 34 μm \( \times 161 \) μm. The chip is wire-bonded inside a pin grid array (PGA) package for measurements.
TABLE 2. Performance summary and comparison of the proposed VCO with prior-art publication.

| Reference   | Tech. (nm) | Supply (V) | Oscillation Freq. (MHz) | Pdiss (mW) | Phase Noise (dBc/Hz) | Frequency TR (%) | Area (mm²) | FoM₁ (dBc/Hz) | FoM₂ (dBc/Hz) |
|-------------|------------|------------|------------------------|------------|----------------------|------------------|------------|----------------|----------------|
| This Work   | 350        | 3.3        | 0.01-9.37              | 0.32³      | -114.87              | -147.57          | 199.5      | 0.005          | -174.75        |
| TVLSI’15 [2]| 180        | 1.2        | 12.6-48                | 1.2        | -109.38              | 116.83           | 0.0216     | -121.05        | -140.41        |
| JSSC’06 [3] | 250        | 2.4        | 7                      | N.A        | N.A                  | N.A              | N.A        | N.A            | N.A            |
| TCAS’18 [4] | 130        | 1.2        | 2.2-20                 | 0.227      | 147.8                | 163.4            | 0.01⁶      | -120.2         | -177.4         |
| JSSC’13 [5] | 130        | 1          | 5.822-8                | 0.031      | -112.46              | 27.33            | 0.025⁶     | -142.8         | -184.8         |
| JSSC’16 [6] | 180        | 1.4        | 10.5                   | N.A        | N.A                  | N.A              | N.A        | N.A            | N.A            |
| JSSC’17 [9] | 40         | 0.8        | 1.05                   | 0.017      | -84.4                | N.A              | N.A        | N.A            | N.A            |
| JSSC’20 [32]| 180        | 1.8        | 0.7-9.5                | 0.01       | -127                 | 172.54           | 0.0237     | -156           | -154           |
| TVLSI’19 [34]| 180      | 1.2        | 13.4                   | 0.158      | -124.07              | N.A              | 0.117      | -139.24        | -154.6         |

³ At 1 MHz offset frequency. ⁴ Considering the output buffer consumption. ⁵ Estimated from die micrograph. ⁶Estimated from measured phase noise plot. ⁷At 0.6 MHz offset frequency

Fig. 10 shows the measured phase noise of the proposed VCO at different oscillation frequencies compared to the noise analytical model @ $f_{osc} = 9.37$ MHz.

![Fig. 10. Measured phase noise of the proposed VCO at different oscillation frequencies compared to the noise analytical model @ $f_{osc} = 9.37$ MHz.](image)

In the inset. The carrier frequency in the analytical equations is optimized with respect to the measured value of the maximum oscillation frequency of 9.37 MHz. Since the control voltage is provided from a DC generator during measurement, the measured PSD of $\nu_{\text{ext}} = 5$ nV/$\sqrt{\text{Hz}}$ is used for the extrinsic noise accompanying the bias voltage. As the tuning voltage increases, the output current and the oscillation frequency decrease. As shown in analytical equations (10) and (14), oscillation frequency and output current have opposing effects on the phase noise. Thus, control voltage increments have only resulted in a few dB improvements.

Comparison of the analytical model prediction with the measured phase noise shows that the average phase noise difference is less than 8% as the frequency offset changes from 1 kHz to 1 MHz. This slight difference stems from some correlated noise sources on different nodes of the oscillator. For instance, substrate and supply noise arising from current switching in other parts of the chip are considered negligible in the analytical model. Also, the induced phase noise of the output buffer, which is not considered in the analytical model, influences the total phase noise result. Because of this, the measured phase noise for the offset of more than 10 kHz does not follow the same slope as the estimated
phase noise from the analytical equations. A temperature evaluation is performed in the temperature range of $-5^\circ$C to $80^\circ$C. Fig. 11 illustrates the measured drift in the normalized frequency at the nominal value of 9.37 MHz (measured at room temperature) due to temperature variation. It shows that the average temperature sensitivity is less than $\pm10\%$.

V. DISCUSSION

A. COMPARISON TO THE STATE OF THE ART

Table 2 summarizes the measured performance of the proposed ring-VCO compared with prior VCO designs implemented in various CMOS processes, from 40- to 250-nm technologies, while operating at a low-frequency similar to the one of the proposed VCO. Using almost the same carrier frequency, the proposed design shows a better phase noise performance, an extended frequency range, and a smaller silicon area. The energy-efficient designs given in [5], [19], and [33] suffer from poor phase noise, even though they operate at low frequencies of 5.822 MHz, 1.05 MHz and 2.24 MHz, respectively.

In favor of a fair comparison with other relevant works at different oscillation frequencies and power dissipation, the following well-known Figure-of-Merit (FoM) is utilized [15]:

$$\text{FoM}_1 = L(\Delta f) - 20 \log \left( \frac{f_{\text{osc}}}{\Delta f} \right) + 10 \cdot \log \left( \frac{P_{\text{dis}}}{1 \text{ mW}} \right)$$

where $L(\Delta f)$ is the phase noise at the offset frequency of $\Delta f$, $f_{\text{osc}}$ is the oscillation frequency and $P_{\text{dis}}$ is the VCO’s consumed power. In addition, another FoM (FoM$_2$) with respect to the total frequency tuning range ($TR_f$) is defined as [17]:

$$\text{FoM}_2 = L(\Delta f) - 20 \log \left( \frac{f_{\text{osc}} \cdot TR_f}{10 \cdot \Delta f} \right) + 10 \cdot \log \left( \frac{P_{\text{dis}}}{1 \text{ mW}} \right)$$

with

$$TR_f = \frac{f_{\text{max}} - f_{\text{min}}}{f_{\text{central}}} \%.$$

From the FoM$_1$ perspective, the performance of all VCOs in terms of power consumption and phase noise with respect to two different carrier frequencies are examined. The FoM$_1$ of the proposed VCO is $-174.75$ and $-167.5$ dBc/Hz at 10 kHz and 1 MHz frequency offset, respectively. As shown in Table 2, the presented work shows a better FoM$_1$ amidst the designs with roughly the same operating frequency. Structures reported in [16], [33], and [34] have good FoM$_1$ or FoM$_2$, but exhibit high phase noise, large area, and limited tuning frequency range.

The proposed VCO achieves low power and a small integration area compared with similar designs listed in Table 2. The average power consumption is 0.32 mW, and the power dissipation at a maximum oscillation frequency of 9.37 MHz is 0.903 mW including the power of the output buffer. Despite the high supply voltage and the long-channel technology whose power consumption is inferior, the proposed VCO shows a wide frequency range with a tuning voltage up to 2 V and a FoM$_2$ of $-193.45$ dBc/Hz. In addition, it shows a linear voltage tuning range over 60% of VDD while significantly outperforming conventional techniques in terms of phase noise property.

Additionally, the VCO contributed noise can be characterized by the input-referred phase noise spectrum as a function of the offset frequency. Phase noise can be accurately represented as input-referred noise by applying the inverse of the system transfer function [13], [14]. Since phase is the integral of the frequency, the VCO acts as an ideal integrator for the control voltage when the output variable is a phase. So, its transfer function can be simply expressed as $H_{\text{VCO}}(s) = \frac{1}{sK_{\text{VCO}}}$. The one-sided PSD of input-referred phase noise as a function of the certain $\Delta f$, can be defined as [13] and [31]

$$S_{\text{IRPN}}(\Delta f) = S_\phi(\Delta f) \cdot \frac{\Delta f^2}{K_{\text{VCO}}^2} = L(\Delta f) \cdot \frac{2\Delta f^2}{K_{\text{VCO}}^2},$$

where $S_\phi(\Delta f)$ is the one-sided PSD of phase noise. So, the input-referred noise of the proposed VCO with a phase noise of $-147.57$ dBc/Hz at 1 MHz offset and a gain of 4.7 MHz/V is calculated to be $12.58 \text{nV}/\sqrt{\text{Hz}}$.

As explained, the proposed VCO is designed for a sensor interface application where a low-frequency range was adopted. However, by adjusting transistors’ feature size in the proposed design, a higher oscillation frequency could be achieved. Generally, the maximum oscillator frequency
as a function of the CMOS technology development has an ascending behavior while the phase noise performance is descending. Therefore, the proposed design at higher frequencies and scaled technology nodes may experience some degradation in its phase noise performance.

B. SYSTEM-LEVEL SENSOR INTERFACE ARCHITECTURE

To evaluate the efficiency of the proposed VCO as an embedded sub-block, a system-level time-based sensor interface is performed with Matlab/Simulink. The measured VCO circuit parameters are adopted in this implementation and the overall performance is examined. Fig. 12 shows the corresponding simulation model of the closed-loop PLL-based sensor interface presented in Fig. 1(b) [14], [20]. The conversion is based on the locking of two identical VCOs (VCOsens and VCOref). To model a practical VCO, its frequency is represented with a polynomial based on (5). The multi-bit PFD (phase frequency detector), which can be modeled as a time-domain quantizer, generates an N-bit code (Dout), which is the digitization of the sensor input signal (Vin(t)). The system’s sampling rate is determined by the reference frequency. In the locking condition, the frequency of VCOsens is on average equal to the frequency of VCOref (or sampling frequency fs).

Simulations are performed with the consideration of the oscillator phase noise at the output of the VCO (φspn and ϕpfn). The phase noise can be expressed in the time domain as a cycle-to-cycle jitter, σj2 [30]. The jitter contributions can be transferred by σc · randn(), where randn() is a Matlab® function used to generate normally distributed random numbers [14]. The measured jitter result of the proposed VCO (17 ps) is employed in simulation to provide a reasonable evaluation. The input signal with frequency of f_in = 260 Hz and peak-to-peak amplitude of 0.5 Vpp is applied. Fig. 13 shows the simulated power spectrum with and without the impact of phase noise for the PLL-based sensor interface. Fig. 14 illustrates the SNR of the interface circuit as a function of the input bandwidth (BW) while considering the proposed VCO measured characteristics. As can be seen, the SNR of 88.43 dB is achieved with low phase noise VCO at 1 kHz input bandwidth, fosc = 9.37 MHz, and quantizer number of bits (Nbit = 4).

The impact of VCO’s phase noise is usually applied to the system-level model by the matter of jitter. Since the analytical link between flicker-induced phase noise and jitter needs a complicated approximation, most of the prior arts consider only the white noise (1/f2) in phase noise to jitter conversion [30]. Thus, the phase noise nonideality is estimated from the 1/f2 phase noise using (9) [14] and [20]. Although the result of this approximation is not quite realistic, it is a tolerable approach to evaluate the influence of the VCO phase noise on the system’s SNR. Fig. 15 shows the SNR as a function of the VCO phase noise and oversampling ratio (OSR = f_s/(2BW)). It is visible that decreasing the VCO phase noise and increasing the OSR leads to SNR and hence resolution increment. However, OSR boosting is a more energy-efficient strategy at the cost of input bandwidth [14]. Fig. 16 shows the cross-section view of Fig. 15 at OSR = 5000. It can be seen when the phase noise is insignificant (for the phase noise less than -160 dBc/Hz), the gain has no effect on the SNR performance while the SNR increases by 6.02 dB for each quantizer bit as expected from the ideal definition. On the contrary, in the phase noise dominant region (right-side), doubling the VCO gain improves SNR by around 4 to 8 dB depending on the phase noise value.

We can conclude that in a VCO-based sensor interface, the oscillator phase noise performance has a major impact.
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on the overall system SNR. According to Fig. 14, the system can achieve over 14 effective number of bits (ENOB) of resolution for the practical VCO phase noise value of -147.57 dBc/Hz at a 1-MHz offset frequency (or 17.64 ps jitter), 4.7 MHz/V gain, 1 kHz bandwidth and an OSR of 4685. This substantiates the capability of the proposed VCO in the realization of a high-resolution sensor interface.

VI. CONCLUSION

We presented in this paper the design and analysis of a linear, low-noise, and wide-tuning range ring VCO operating as part of a constituent block of an integrated readout sensor interface. The prototype was implemented in the AMS 0.35 μm CMOS technology under a 3.3 V supply. The measured oscillation frequency range extends from 0.01 to 9.37 MHz which represents a 199.5% frequency tuning range over a 2 V control voltage. At maximum frequency, the measured phase noise is −147.57 dBc/Hz at 1 MHz offset frequency, while the FoM of the proposed VCO is −167.5 dBc/Hz. The average power consumption is 0.32 mW while taking a silicon area of 34 μm x 161 μm. Also, we have discussed the performance analysis of a PLL-based sensor interface via a Matlab/Simulink model and showed the impact of the VCO phase noise on the SNR performance of the targeted application. Simulated results indicate that a SNR of 88.43 dB can be obtained in a time-based readout interface utilizing the proposed VCO measured characteristics. Therefore, the proposed configuration allows realizing a compatible VCO structure for a wide range of analog/digital circuits requiring VCO, such as time to digital converters and sensor interfaces for numerous applications.

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