Symmetric Synthesis*

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Abstract

We study the problem of determining whether a given temporal specification can be implemented by a symmetric system, i.e., a system composed from identical components. Symmetry is an important goal in the design of distributed systems, because systems that are composed from identical components are easier to build and maintain. We show that for the class of rotation-symmetric architectures, i.e., multi-process architectures where all processes have access to all system inputs, but see different rotations of the inputs, the symmetric synthesis problem is \textsc{EXPTIME}-complete in the number of processes. In architectures where the processes do not have access to all input variables, the symmetric synthesis problem becomes undecidable, even in cases where the standard distributed synthesis problem is decidable.

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1 Introduction

Many classical protocols and distributed systems are symmetric. This means that every process, independently of its identity, starts in the same initial state and follows the same set of transitions. Symmetric systems are easier to understand and maintain; especially in VLSI designs, which usually contain large numbers of identical components, this is a significant cost factor. Constructing symmetric systems is also a step towards building arbitrarily scalable systems \cite{7, 2, 11}.

There is a large body of results \cite{1, 18, 5, 12, 26, 13} that deal with the question of which distributed systems need symmetry breaking and which do not. Leader election among the processes on a ring, for example, cannot be implemented symmetrically \cite{1}; similarly, in resource-sharing problems, like the Dining Philosophers, the only way to avoid starvation is to break the symmetry \cite{18}.

Our goal is to automate this type of reasoning. Given a specification of a reactive system in temporal logic, we wish to automatically determine whether there exists a symmetric implementation. This is a refinement of the classic distributed synthesis problem, which asks whether a temporal specification has an implementation where the processes are arranged in a particular architecture. Distributed synthesis is well-studied \cite{25, 21, 14, 15, 16, 9, 24}.

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However, the approach presented in this paper is the first to synthesize symmetric implementations. We consider rotation-symmetric system architectures. Rotation-symmetric architectures are multi-process architectures where all processes have access to all system inputs, but see different rotations of the inputs. Figure 1 shows a simple rotation-symmetric architecture. Rotation-symmetric architectures are suitable to reason about distributed systems that lack a central coordination process. They can, for example, model leader election scenarios and distributed traffic light controllers [6]. The fact that the processes obtain their input in different rotations is important: since all processes have the same implementation, they would otherwise also produce the same output. The synthesis problem for such systems could trivially be reduced to the standard synthesis problem by adding a constraint that the outputs are the same all the time.

We present an algorithm for the synthesis of symmetric systems in rotation-symmetric architectures from specifications in linear-time temporal logic (LTL). Most standard synthesis algorithms follow the automata-theoretic approach [22], whereby the given temporal formula is translated into a tree automaton that accepts exactly those computation trees that satisfy the formula. Hence, the specification is realizable if and only if the language of the automaton is non-empty. The synthesis algorithm then simply extracts some finite-state implementation from the language of the automaton. The situation is more difficult when we wish to decide the existence of a symmetric solution, because the language of the automaton may contain both computation trees that belong to symmetric implementations and computation trees that belong to asymmetric implementations. As we show in Section 4, symmetry is not a regular property: we therefore cannot check symmetry with a separate tree automaton or encode symmetry as a temporal logic formula and add it to the specification.

The key insight of our algorithm is that the paths in the computation trees produced by symmetric implementations are guaranteed to be invariant under rotations: if, in each position of two (finite or infinite) computation paths, the values of the input variables of the $j$th process in the first path correspond to the values of the input variables of the $((j + k) \mod n)$th process, for some $k$, in the second path, then the values of the output variables of the $j$th process must also, in each position, correspond to the values of the output variables of the $((j + k) \mod n)$th process (for all $0 \leq j < n$, where $n$ is the number of
processes). Our algorithm exploits this observation to simplify the computation trees. Paths that are just rotations of each other are collapsed into a single representative. Computations in different processes that must lead to identical outputs are thus kept in the same path of the reduced tree; the paths only split when the symmetry is broken by some input. While symmetry is difficult to check on the original computation tree, it becomes a local condition on individual paths in the reduced tree: as long as the output never spontaneously introduces asymmetry, i.e., as long as every asymmetry in the output can be explained by a previous asymmetry in the input, the reduced tree can be expanded into a full computation tree that we know, by construction, to be symmetric.

As we show in Section 4, the running time of our synthesis algorithm is single-exponential in the number of processes. In Section 5, we show that our algorithm is asymptotically optimal: the problem is \(\text{EXPTIME}\)-complete in the number of processes. In Section 6, we study the extension of the synthesis problem to the case where the processes no longer have access to all variables. Here, our result is negative: under incomplete information, the symmetric synthesis problem is undecidable even for system architectures where the standard synthesis problem is decidable. This paper is based on previously unpublished results from the first author’s PhD thesis [6], where also additional details of the presented results can be found.

2 Preliminaries

A reactive system produces a valuation to the output propositions in some set \(\text{AP}^O\) and reads the values of the input propositions in some set \(\text{AP}^I\) in every step of its execution. The behavior of a reactive system can be described as a computation tree \(\langle T, \tau \rangle\), where \(T = (2^{\text{AP}^I})^*\) is the set of tree nodes and \(\tau : T \rightarrow 2^{\text{AP}^O}\) labels every tree node \(t\) by the output propositions \(\tau(t)\) that the system sets to true after having read \(t\) as its (prefix) input sequence.

A trace in a computation tree \(\langle T, \tau \rangle\) is an infinite sequence \((\tau(\epsilon) \cup t_0)(\tau(t_0) \cup t_1)(\tau(t_0t_1) \cup t_2)(\tau(t_0t_1t_2) \cup t_3)\ldots \in (2^{\text{AP}^I} \cup \text{AP}^O)^\omega\). Given some language \(L \subseteq (2^{\text{AP}^I} \cup \text{AP}^O)^\omega\), reactive synthesis is the process of checking if there exists a computation tree \(\langle T, \tau \rangle\) with \(T = (2^{\text{AP}^I})^*\) as node set such that every trace of \(\langle T, \tau \rangle\) is in \(L\). A classical logic to denote specification languages is linear temporal logic (LTL, [19]). LTL formulas for reactive system specifications are built according to the grammar

\[
\varphi ::= p \mid \neg \varphi \mid \varphi \lor \varphi \mid \varphi \land \varphi \mid X \varphi \mid G \varphi \mid F \varphi \mid \varphi U \varphi,
\]

using the temporal operators \(G\) (globally), \(F\) (eventually), \(X\) (next), and \(U\) (until). All elements from \(\text{AP}^I\) and \(\text{AP}^O\) can be used as propositions \(p\). A more formal definition of LTL is given in [19, 4].

For LTL specifications, it is known that if and only if there exists a computation tree all of whose traces satisfy a specification (i.e., the specification is realizable), there exists a regular such computation tree. A computation tree is regular if it has only finitely many different sub-trees. Given a computation tree \(\langle T, \tau \rangle\), a tree \(\langle T', \tau' \rangle\) is a sub-tree of \(\langle T, \tau \rangle\) if and only if \(T = T'\) and there exists a \(\hat{t} \in T\) such that for every \(t \in T\), we have \(\tau'(t) = \tau(\hat{t})\). Regular computation trees can be translated to finite-state machines and implemented in hardware or software using a finite amount of memory. A tree language for some sets \(\text{AP}^I\) and \(\text{AP}^O\) is a subset of all trees \(\langle T, \tau \rangle\) with \(T = (2^{\text{AP}^I})^*\) and \(\tau : T \rightarrow 2^{\text{AP}^O}\). A tree or word language is called regular if it can be recognized by some finite tree or word automaton (with a Muller acceptance condition, see [10] for details).
In distributed synthesis, we search for a distributed implementation of a finite-state machine. Given is an architecture that defines several processes and the signals that connect the processes among themselves and with the global input and output of the architecture. Starting from a specification over all signals, we search for implementations for all of the processes such that the computation tree induced by the process implementations and the architecture satisfies the specification. In the induced computation tree, all processes are executed at the same time and in parallel, using the usual parallel composition semantics.

It is known since the seminal work by Pnueli and Rosner [21] that not all architectures have a decidable distributed synthesis problem. Figure 2 depicts the $A0$ architecture that they defined as an example for an undecidable architecture. Finkbeiner and Schewe [9] later proved that the distributed synthesis problem is decidable if and only if there exists no information fork in the architecture. An information fork is a pair of processes that are incomparably informed, i.e., for which each of the processes has access to some global input that the other process cannot read. For a more formal definition of distributed synthesis, the interested reader is referred to [9].

A Turing machine is a tuple $M = (Q, \Sigma, \Gamma, \delta, q_0, g)$ in which $Q$ is a finite set of states, $\Sigma$ is an input alphabet, $\Gamma \supseteq \Sigma$ is a (finite) tape alphabet, $\delta : Q \times \Gamma \rightarrow (Q \times \Gamma \times \{-1, 0, 1\})^2$ encodes the Turing machine transition function, $q_0 \in Q$ is an initial state, and $g$ maps every state to its type, which can be accepting, rejecting, or transient. The $\delta$ function maps every state/tape content combination to exactly two possible successor state/tape content/tape motion combinations. For deterministic Turing machines, the two successor combinations are always the same. Alternating Turing machines [3] extend the non-deterministic Turing machines by partitioning the transient states into universally branching and existentially branching states. An (alternating) Turing machine accepts a word $w \in \Sigma^\ast$ if there exists an accepting run tree when starting in state $q_0$ with the tape empty except for a copy of $w$ where the machine head starts on the first character of $w$. In all universal states, the Turing machine execution must be accepting for both possible transitions.

We assume that the modulo function always returns a non-negative number, such that, e.g., $-13 \mod 5 = 2$.

## 3 The Symmetric Synthesis Problem

We consider distributed reactive synthesis problems in which all processes share the same implementation. A process has an interface $\mathcal{N} = (AP_I, AP_O)$ with the local input proposition set $AP_I$ and a local output proposition set $AP_O$. The connections between the processes are described in an architecture.

> **Definition 1 (Symmetric architecture).** Given an interface $\mathcal{N} = (AP_I, AP_O)$, a symmetric architecture over $\mathcal{N}$ is a tuple $\mathcal{E} = (S, P, AP_G, E^{in}, E^{out})$ with:
>
> - the set of (internal) signals $S$,
> - the process set $P$,
> - the global input signal set $AP_G$,
> - the input edge function $E^{in} : (P \times AP_I) \rightarrow (S \cup AP_G)$, and
> - the output edge function $E^{out} : (P \times AP_O) \rightarrow S$.

As an example, the architecture given in the right part of Figure 2 hosts processes with the interface $\mathcal{N} = \{a, b\}$ and has the components $S = \{y, z\}, P = \{0, 1\}, AP_G = \{x\}, E^{in} = \{(0, a) \mapsto x, (1, a) \mapsto y\}$, and $E^{out} = \{(0, b) \mapsto y, (1, b) \mapsto z\}$. We only consider architectures in which every internal signal is written to by exactly one local output of one process. Given a FSM for a process with an interface $\mathcal{N}$ and an architecture $\mathcal{E} = (S, P, AP_G, E^{in}, E^{out})$ over
\( \mathcal{N} \), we can construct an FSM with \( \mathcal{AP}^{I}_G \) as input proposition set and \( S \) as output proposition set that implements the behavior of the complete architecture when using the FSM as process implementation. Without loss of generality, we use the standard synchronous composition semantics to do so. We define the symmetric synthesis problem as follows:

**Definition 2.** Given an interface \( \mathcal{N} = (\mathcal{AP}^{I}, \mathcal{AP}^{O}) \), an architecture \( \mathcal{E} = (S, P, \mathcal{AP}^{I}_G, E^{in}, E^{out}) \), and a specification \( \varphi \) over the propositions \( \mathcal{AP}^{I}_G \cup S \), the symmetric synthesis problem is to check if an FSM implementation \( \mathcal{F} \) with the input proposition set \( \mathcal{AP}^{I} \) and output proposition set \( \mathcal{AP}^{O} \) exists such that the FSM obtained by plugging \( \mathcal{F} \) into \( \mathcal{E} \) satisfies \( \varphi \). In case of a positive answer, we also want to obtain \( \mathcal{F} \).

### 4 Rotation-Symmetric Synthesis

Many symmetric architectures found in practice consist of a ring of processes, all of which read all the input to the overall system. A slight generalization of this architecture shape is the class of rotation-symmetric architectures.

**Definition 3.** A symmetric architecture \( \mathcal{E} = (S, P, \mathcal{AP}^{I}_G, E^{in}, E^{out}) \) over the interface \( \mathcal{N} = (\mathcal{AP}^{I}, \mathcal{AP}^{O}) \) with \( n \) processes is called rotation-symmetric if and only if there exists a local designated proposition set \( \mathcal{AP}^{I}_L \) for every process instance such that the following conditions hold:

- \( \mathcal{AP}^{I}_G = \mathcal{AP}^{I} = \mathcal{AP}^{I}_L \times \{0, \ldots, n-1\} \) and \( P = \{p_0, \ldots, p_{n-1}\} \).
- \( S = \mathcal{AP}^{O} \times \{0, \ldots, n-1\} \).
- For every \( p_i \in P \), every \( x \in \mathcal{AP}^{I}_L \), and every \( j \in \{0, \ldots, n-1\} \), we have \( E^{in}(p_i, (x, j)) = (x, (j - i) \mod n) \), and
- For every \( x \in \mathcal{AP}^{O} \) and \( p_i \in P \), we have \( E^{out}(p_i, x) = (x, i) \).

We show in this section that the symmetric synthesis problem for rotation-symmetric architectures and linear-time temporal logic (LTL) is decidable.

The key observation that we use to prove decidability is that the computation trees that characterize the input/output behavior of a process implementation plugged into a rotation-symmetric architecture have a useful property that we call the symmetry property. While this property is non-regular and thus cannot be encoded into the specification (Lemma 6), we show how to decompose it into two sub-properties, one of which is regular. The other one is still non-regular, but has the advantage that we can enforce it in a synthesis process by post-processing the computation tree obtained from a synthesis procedure to contain only rotations of the computation tree paths along so-called normalized inputs. Since every tree with the symmetry property is left unaltered by this step and we also describe how to ensure that the result of the post-processing step is guaranteed to be a correct solution, this approach is sound and complete.

We assume some fixed rotation-symmetric architecture \( \mathcal{E} = (S, P, \mathcal{AP}^{I}_G, E^{in}, E^{out}) \) over some local process interface \( (\mathcal{AP}^{I}_L, \mathcal{AP}^{O}) \) to be given, define \( \mathcal{I} = 2^{\mathcal{AP}^{I}_G} \) to denote the global input alphabet to all processes, while \( \mathcal{O} = 2^{(\mathcal{AP}^{O} \times \{0, \ldots, n-1\})} \) denotes the global output. The local output of one process is given as \( \hat{O} = 2^{\mathcal{AP}^{O}} \).

The following rotation function will become useful in the analysis below. Let \( U = 2^{\mathcal{AP} \times \{0, \ldots, n-1\}} \) for some other set \( \mathcal{AP} \). We define a rotation operator \( \text{rot} : U \times \mathbb{Z} \to U \) with \( \text{rot}(u, k) = \{(p, (j + k) \mod n) \mid (p, j) \in u\} \) for every \( u \in U \) and \( k \in \mathbb{Z} \). Furthermore, we extend the rot function to LTL formulas and define \( \text{rot}(\psi, k) \) for an LTL formula \( \psi \) over the set of propositions \( \mathcal{AP} \times \{0, \ldots, n-1\} \) and \( k \in \mathbb{Z} \) to be \( \psi \) with all atomic propositions \( (p, j) \) replaced by \( (p, (j + k) \mod n) \) for \( p \in \mathcal{AP}, j \in \mathbb{Z} \). For clarity, when dealing with the rot function for some
set $U = 2^{AP \times \{0, \ldots, n-1\}}$, we often partition the elements of $AP \times \{0, \ldots, n-1\}$ by their process indices and for example write $(X_0, \ldots, X_{n-1})$ instead of $(X_0 \times \{0\}) \cup \ldots \cup (X_{n-1} \times \{n-1\})$ for $X_0, \ldots, X_{n-1} \subseteq AP$. The rotation function is extended to sequences of elements in $U$ by rotating the individual sequence items.

> **Definition 4** (Symmetry property). Given a tree $\langle T, \tau \rangle$ over $T = I^*$ and $\tau : T \to O$, we say that the tree has the symmetry property if for each $t \in T$ and $0 \leq i < n$, $\tau(\text{rot}(t, i)) = \text{rot}(\tau(t), i)$.

> **Lemma 5** (Symmetry lemma). The set of regular trees having the symmetry property is precisely the same as the set of trees that are induced by a rotation-symmetric architecture for some process implementation.

A proof of the lemma can be found in the appendix. The symmetry property is not a regular tree property, and hence cannot be encoded into a tree or word automaton.

> **Lemma 6.** The set of symmetric computation trees for the two-process rotation-symmetric architecture with process interface $\mathcal{N} = (AP_L^I \times \{0,1\}, AP^O)$ and $AP_L^I = \{i\}$ and $AP^O = \{o\}$ is not a regular tree language.

**Proof.** For a proof by contradiction, suppose that the set of symmetric computation trees is regular. The language includes a tree with the symmetry property in which the node labels on the path $((\emptyset, \{i\})^*$ and, symmetrically, on the path $((\{i\}, \emptyset)^*$ form the sequence $l = (\emptyset, \emptyset)^i((\{o\}, \{o\})((\emptyset, \emptyset)^e((\{o\}, \{o\})\ldots$, i.e., the length of the $(\emptyset, \emptyset)$-sequences grows according to the distance to the root. According to the pumping lemma for regular tree languages, however, the sequence $l$ can be partitioned into $l = u \cdot v \cdot w$, such that, for every $k > 0$, there exists a tree in the language where the label sequence on $((\emptyset, \{i\})^*$ is $l = u \cdot v^k \cdot w$, while the label sequence on $((\{i\}, \emptyset)^*$ is still $l$. Clearly, these trees are not symmetric. $\blacksquare$

Since the symmetry property is non-regular, we need to alter the synthesis process itself to account for it. In order to synthesize an implementation for one process, we synthesize implementations for all processes together. These only need to work correctly on normalized input sequences $t \in I^*$. An input sequence is normalized if $\min_i \text{rot}(t, i) = t$, where the min function uses the lexicographic ordering over the strings in $I^*$. For the ordering of the elements in $I$, we consider the lexicographic ordering of their tuple representation. For example, we have $(0,1,0) < (0,1,1)$ and $(0,1,0) < (1,0,0)$ for a three-process architecture.

A tree with the symmetry property is fully determined by the labels along normalized input sequences, as for every non-normalized input sequence $t' \in I^*$, we have $\tau(t') = \text{rot}(\tau(t), i)$ for every $i$ such that $t' = \text{rot}(t, i)$.

When only considering the normalized input sequences during synthesis, we can take the computation tree for all processes in the architecture together and complete it by filling all other tree labels with rotations of the tree labels along normalized inputs. We call the resulting tree its symmetric completion. If afterwards, we have $\tau(\text{rot}(t, i)) = \text{rot}(\tau(t), i)$ for all $t \in I^*$ and $i \in \mathbb{N}$, then the symmetry lemma guarantees that the resulting tree is induced by some process instantiated in a rotation-symmetric architecture. So if we can guarantee that (1) $\tau(\text{rot}(t, i)) = \text{rot}(\tau(t), i)$ is actually the case for all normalized $t$ and $i \in \mathbb{N}$ and (2) that the symmetric completion of the tree satisfies the specification along all paths, then we can obtain a correct process implementation by synthesizing a computation tree for the complete architecture. Our construction for symmetric synthesis consist of these two components, which we describe in more detail below.
4.1 Ensuring Symmetric Completability

Not every $O$-labeled computation tree can easily be made symmetric by replacing the tree labels for non-normalized input sequences. Take for example a tree $\langle T, \tau \rangle$ for the architecture given in Figure 1 with $\tau(x) = (\emptyset, O, \{y\})$. Since the output of the processes is initially different, this means that they cannot have the same implementation. We show in this section that detecting such cases is simple, and the formalization of the observation is a regular property that can be easily encoded into LTL.

> **Definition 7.** Let $AP$ be some set, and $P = \{p_0, \ldots, p_{n-1}\}$ be a list of process identifiers. For every $x \subseteq (AP \times \{0, \ldots, n-1\})$ and $w = w_0w_1w_2 \ldots w_l \in (2^{AP \times \{0,\ldots,n-1\}})^*$, we define

$$\text{rep}(x) = |\{j \in \{0, \ldots, n-1\} \mid \text{rot}(x, j) = x\}|$$

$$\text{reps}(\epsilon) = n$$

$$\text{reps}(w) = \gcd(\text{reps}(w_0 \ldots w_{n-1}), \text{reps}(w_n)),$$

where $\gcd$ denotes the greatest common divisor function.

For some word $t \in \mathcal{I}^*$, $\text{reps}(t)$ represents how many different rotations in $\{0, \ldots, n-1\}$ of $t$ exist that map the word to itself.

> **Lemma 8 (Second symmetry lemma).** Let $\langle T, \tau \rangle$ be a computation tree with $T = \mathcal{I}^*$ and $\tau : T \rightarrow O$ for which for every $t \in T$, we have that $\text{reps}(t) \mid \text{reps}(\tau(t))$ (where the $|$ symbol refers to division without remainder). The unique symmetric completion of $\langle T, \tau \rangle$ has the symmetry property. Furthermore, if $\langle T, \tau \rangle$ is regular, then so is its unique symmetric completion.

By the second symmetry lemma, it suffices for a computation tree to have $\text{reps}(t) \mid \text{reps}(\tau(t))$ for all $t \in T$ to ensure that the symmetric completion of the tree has the symmetry property.

We can encode this requirement in LTL as

$$\varphi_{out\text{cond}} = \bigwedge_{d \in \{1, \ldots, n\}, d \mid n} \neg (\text{sym}(\mathcal{I}, d, n) \cup \neg \text{sym}(O, d, n))$$

for the function

$$\text{sym}(AP, d, n) = \bigwedge_{a \in AP, j \in \{0, \ldots, n-1\}} (a, j) \leftrightarrow (a, j + \frac{n}{d})$$

that encodes, for each $i \subseteq AP \times \{0, \ldots, n-1\}$ whether $d \mid \text{rep}(i)$ (for $d \in \mathbb{N}$ with $d \mid n$).

4.2 Ensuring That the Tree Completion Satisfies the Specification

If we have a computation tree $\langle T, \tau \rangle$ all of whose traces satisfy some linear-time specification $\varphi$, this does not imply that its rotation-symmetric completion satisfies $\varphi$ as well. If all traces of $\langle T, \tau \rangle$ however satisfy $\varphi \land \text{rot}(\varphi, 1) \land \ldots \land \text{rot}(\varphi, n-1)$, then since we know that every infinite trace in the rotation-symmetric completion is a rotation of a trace in the original tree by some value $i \in \mathbb{N}$, we know that the rotation-symmetric completion also satisfies $\varphi$ along every trace. So if we synthesize a tree for $\varphi' = \varphi \land \text{rot}(\varphi, 1) \land \ldots \land \text{rot}(\varphi, n-1)$ as specification instead of $\varphi$, taking the rotation-symmetric completion maintains $\varphi$.

Note that strengthening $\varphi$ to $\varphi'$ comes without loss of generality if we are interested in rotation-symmetric implementations. By the symmetry property, if the tree $\langle T, \tau \rangle$ induced by a rotation-symmetric architecture and a process implementation satisfies $\varphi$, then it also satisfies $\text{rot}(\varphi, i)$ for all $i \in \mathbb{N}$ as every rotation of every trace in the tree is also a trace in the tree. Hence, to satisfy $\varphi$, it also needs to satisfy $\text{rot}(\varphi, i)$ as otherwise we could take a trace not satisfying $\text{rot}(\varphi, i)$, rotate it by $-i$, and obtain a trace that does not satisfy $\varphi$. 
4.3 Putting Everything Together

Using the concepts defined above, we are now ready to tie them together to a complete synthesis process. We start with a specification $\varphi$ over the architecture input propositions $\mathcal{AP}_I^G$ and the output proposition set $\mathcal{AP}_O^0 \times \{0,\ldots,n-1\}$ for $|P| = n$.

1. We modify the specification $\varphi$ to $\varphi' = \varphi \land \text{rot}(\varphi,1) \land \ldots \land \text{rot}(\varphi,n-1)$.
2. We modify $\varphi'$ to $\varphi'' = \varphi' \land \varphi_{\text{outcond}}$ (as described in Section 4.2).
3. We synthesize a regular tree $\langle T, \tau \rangle$ that satisfies $\varphi''$ along all paths using a classical reactive synthesis procedure. If there is no such tree, the specification is unrealizable.
4. If a regular computation tree $\langle T, \tau \rangle$ is found, we replace every label along non-normalized directions by rotations of $\tau$’s labels along normalized directions to get a tree $\langle T', \tau' \rangle$ with the symmetry property.
5. We cut off the labels of $\tau'$ except for the output of the first process in the architecture. The resulting (regular) tree is the synthesized process implementation.

Proposition 9. The above synthesis process from LTL has a complexity that is $2\text{EXPTIME}$ in the length of the specification and exponential-time in the number of processes.

Proof. We use the automata-theoretic approach to reactive system synthesis from [17, 24] and the concepts defined in these works. We start by translating the specification to a universal co-Büchi word (UCW) automaton, which is of size $2^{O(|\varphi|)}$ in the size of the specification. As UCWs do not blow up under conjunction, executing step 1 from the construction above leads to an automaton of size $n \cdot 2^{O(|\varphi|)}$. A deterministic automaton for the added property in step 2 can be built with at most $n$ states, so executing step 2 leads to at most $n$ additional states, and we obtain an automaton with $n + n \cdot 2^{O(|\varphi|)} = n \cdot 2^{O(|\varphi|)}$ many states. The bounded synthesis approach works with specifications given as co-Büchi word automata [24] and takes time exponential in the number of states of the automaton. The overall time complexity so far is thus $2\text{EXPTIME}$ in $|\varphi|$ and exponential in $n$. Step 4 leads to a blow-up of at most a factor of $n^2$ and can be done in time polynomial in the number of states in the synthesized finite-state machine (whose size is proportional to the time complexity of the synthesis procedure executed in the previous step). Step 5 is simple and takes time linear in the size of the FSM.

Note that even though the construction above discards all non-normalized parts of the synthesized computation tree, asking the synthesis algorithm to nevertheless synthesize these parts according to the specification comes without loss of generality, as trees with the symmetry property (which we are actually searching for) fulfill $\varphi''$ along all paths if all of their paths satisfy $\varphi$. So the synthesis process does not report spurious unrealizability.

5 Rotation-Symmetric Synthesis – Complexity

The symmetric synthesis construction from the previous section has a time complexity that is doubly-exponential in the length of the specification and singly-exponential in the number of processes. We want to show in this section that this matches the complexity of the problem by giving a corresponding hardness result. The $2\text{EXPTIME}$-hardness in the specification length is inherited from the complexity of LTL synthesis [20]. For the $\text{EXPTIME}$ complexity in the number of processes, we provide the following result:

Lemma 10. Given an $f(k)$-space bounded alternating Turing machine $M = (Q, \Sigma, \Gamma, \delta, q_0, g)$, we can reduce the acceptance of a word $w \in \Sigma^k$ by $M$ to the symmetric realizability problem of $n = f(k)$ processes with a specification in LTL of size polynomial in $|Q| \cdot |\Gamma| \cdot |w|$.
Proof. We build a specification that requires the processes to output the Turing tape configuration along an execution of the machine. The specification is realizable if and only if the Turing machine does not accept the word. Every process outputs the value of one Turing tape cell and if the tape head is at the cell, also the state of the Turing machine. There are $n$ input signals to the architecture, and when the processes start, the left-most local input signals of the processes is used to tell one or more processes that the Turing tape computation should start at that cell with the tape head being initially there (with $w$ as the initial tape content). To account for the rotation-symmetry, the processes output not only the tape content and tape head position, but also the current boundaries of the tape. The specification is modeled such that if start and end markers collide, the simulation of the Turing machine can stop.

The specification also includes conjuncts that require all processes together to simulate the Turing machine computation correctly and to never reach an accepting state. Whenever the alternating Turing machine branches universally, the left-most local process input signal is used to select which successor state is picked. In case of existential branching, the processes can decide which successor state to pick. Enforcing the specification to be realizable if and only if the word $w$ is not accepted by the Turing machine helps with taking care of the diverging computations of the Turing machine and those computations that exceed the space bound. Both count as non-accepting in the definition of space-bounded Turing machines. Since these runs never visit accepting states and/or permit the simulation to stop, they are allowed to be simulated by a synthesized implementation.

The specification can be written with size polynomial in $|Q| \cdot |\Gamma| \cdot |w|$ as we only need to define the specification for one process. By the symmetry of the architecture, the other processes have to fulfill it as well.

A more detailed proof can be found in the appendix.

\textbf{Corollary 11.} The rotation-symmetric realizability problem (for LTL) has a time complexity that is exponential in the number of processes.

Proof. Given the question whether a word $w = w_0 \ldots w_{k-1}$ is in the language defined by some $(c+1)$-EXPTIME = $(c)$-AEXPSPACE problem for some $c \in \mathbb{N}$, we can reduce it to the symmetric realizability problem for an LTL specification of length polynomial in $k$ and with a number of processes that is $(c)$-exponential in $k$. Since by the space hierarchy theorem [23], the $(c)$-EXPTIME hierarchy is strict for increasing $c$, we can conclude that in general, we cannot solve the symmetric realizability problem faster than in time exponential in the number of components.
The synthesis problem for standard, not necessarily symmetric, distributed systems is decidable as long as the processes can be ordered with respect to their relative knowledge about the system inputs [9]. The problem becomes undecidable as soon as it contains an information fork, i.e., a pair of processes with incomparable knowledge. The simplest such architecture is Pnueli and Rosner’s A0 architecture [21], shown on the left in Fig. 2. In this section, we show that for symmetric synthesis, even architectures without information forks, such as the S0 architecture shown on the right in Fig. 2, are undecidable. Our proof is based on Pnueli and Rosner’s undecidability argument for A0:

- **Lemma 12** ([21]). For a given Turing machine $M$, there exists an LTL formula $\psi$ that is realizable in the distributed architecture A0 if and only if $M$ halts and such that the two processes of the unique implementation of $M$ sequentially output binary encodings of the configurations of the Turing machine on $y$ (or $z$, respectively) upon the first $true$ value on the input $u$ (or $v$, respectively).

Because of the undecidability of the halting problem, Lemma 12 means that the distributed synthesis problem of architecture A0 is undecidable. We prove the undecidability of the symmetric synthesis problem of architecture S0 in two steps. First, we establish the undecidability of the larger architecture S2, depicted in Figure 3, by showing that the realizability of $\psi$ in A0 can be reduced to the symmetric realizability of an LTL formula over S2; in the second step, we encode the synthesis problem of S0 into the synthesis problem of S2 and thus establish that the synthesis problem for the simpler architecture S0 is undecidable as well.

- **Lemma 13.** The symmetric synthesis problem for architecture S2 is undecidable.
Proof. We show that there exists an implementation for the specification $\psi$ in the $A_0$ architecture if and only if there exists a joint implementation for the two processes in the $S_2$ architecture that satisfies $\psi' = \psi_d \land G(v \leftrightarrow Xo) \land G(w \leftrightarrow Xp)$, where $\psi_d$ results from prefixing all occurrences of the signals $y$ and $z$ in $\psi$ with a next-time operator.

The results of the two synthesis problems can be translated into each other. A distributed implementation of $\psi$ over $A_0$ is necessarily symmetric: both processes output the same bitstream when reading a true value as their local input for the first time. To obtain an implementation for $S_2$, we simulate the process with input $a$ and use $g$ as the local output. Additionally, we copy all values from $b$ to $e$, and $c$ to $f$.

Conversely, an implementation found by the symmetric synthesis of $S_2$ provides an implementation for $\psi$ in $A_0$. The key property of the architecture $S_2$ is that the process does not know if the local input $b$ is the (delayed) $a$ input to the other process, or if its $c$ input is the (Turing machine tape) output of the other process. Thus, it cannot find out if it is the top process or the bottom process in the architecture and must prevent violating the specification in either case. A more detailed proof is given in the appendix.

In order to reduce the symmetric synthesis problem of $S_2$ to the symmetric synthesis problem of $S_0$, we introduce compression functions that time-share multiple signals of $S_2$ into a single signal in $S_0$.

Let $AP$ be a set of signals. We call a function $f : (2^{AP})^\omega \to (2^{\chi})^\omega$ for some Boolean variable $\chi$ a compression function if $f$ is injective. We call a function $f'$ that maps a specification over the signal set $AP$ to a different specification over the signal set $\{\chi\}$ the adjunct compression function to $f$ if for all $w \in (2^{AP})^\omega$ and specifications $\psi$ over $AP$, we have that $w \models \psi$ if and only if $f(w) \models f'(\psi)$.

In the appendix, we give such a pair of compression functions for LTL. The compression mechanism is illustrated in Figure 4. One clock cycle in the four-bit-per-character version of a word is spread to 10 computation cycles in the one-bit-per-character version of the word. Every 10 cycles, the 2-cycle character start sequence (CSS) $\{\chi\}{\chi}$ is instantiated, followed by four two-cycle slots for every signal in $AP$. Note that the construction ensures that whenever we have $\{\chi\}{\chi}{\chi}$ as a part in a compressed word, then we know that a character start sequence begins on the first occurrence of $\{\chi\}$ in this part.

\[\mbox{Theorem 14. The symmetric synthesis problem for architecture $S_0$ is undecidable.}\]

Proof. In order to reduce the symmetric synthesis problem of architecture $S_0$ to the symmetric synthesis problem of architecture $S_2$, we compress $u, v, w$ into signal $x$; $a, p, q$ into signal $y$; and $x, y, z$ into signal $z$. A more detailed proof is given in the appendix. \[\mbox{\blacksquare}\]
Conclusions

In this paper, we have studied the problem of synthesizing symmetric systems. Our new synthesis algorithm is a useful tool in the development of distributed algorithms, because it checks automatically if certain properties in a design problem require symmetry breaking.

Our algorithm synthesizes implementations of rotation-symmetric architectures, i.e., architectures where the processes observe all inputs. The undecidability result for the architecture $S_0$ indicates that it is impossible to extend the synthesis algorithm to architectures where the processes no longer have access to all inputs. A promising direction of research, however, is to use our results to extend existing semi-algorithms for synthesis under incomplete information to such symmetric architectures. An example for such an approach is bounded synthesis [24], which determines if there exists an implementation with at most $n$ states, where $n$ is a given bound. The specification is translated into a universal co-Büchi automaton, which is then, together with the bound $n$, encoded into a satisfiability modulo theory problem. To ensure correctness under incomplete information, constraints are added that ensure that if a process cannot distinguish two inputs, it transitions to the same successor state. Similarly, for symmetric synthesis, constraints can be added that ensure that the outputs of the individual processes are identical in states that are indistinguishable for them.

Algorithms for symmetric synthesis procedures also offer a new perspective on the problem of synthesizing arbitrarily scalable (i.e., parametric) systems. Due to the undecidability of the problem, only very limited solutions to this problem have been found so far. For example, Jacobs and Bloem [11] tackle the case of asynchronous processes with local input in a ring architecture and use the bounded synthesis approach mentioned above. Emerson and Srinivasan [7] present a solution for a multi-process version of a small subset of the temporal logic CTL while Attie and Emerson [2] give a different solution allowing a bigger subset of CTL but only guaranteeing correctness of the solution if certain other conditions are fulfilled, like the dead-lock freeness of the solution produced. In such a setting, symmetric synthesis can be used to detect specifications that are unrealizable even for small system sizes – if there is no solution for a fixed number of processes $n$, then there is certainly none for scalable systems as well.

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A Appendix – Proof Details

A.1 Additional Preliminaries

We use Moore machines as finite-state model for regular computation trees. Formally, a Moore machine is a tuple $M = (S, \mathcal{I}, O, \delta, s_{init}, L)$ with the (finite) set of states $S$, the input alphabet $\mathcal{I}$, the output alphabet $O$, the initial state $s_{init} \in S$, and the labelling function $L : S \rightarrow O$. A Moore machine induces a computation tree $(T, \tau)$ with $T = T^*$ and $\tau : T \rightarrow O$ such that for all $t_0 \ldots t_n \in T$, we have that $\tau(t_0 \ldots t_n) = L(\delta(\ldots (\delta(s_{init}, t_0), t_1), \ldots), t_n-1), t_n))$. Moore machines induce regular computation trees, i.e., computation trees that only have a finite number of distinct sub-trees.

Given a Moore machine, an extended computation tree induced by it is the same as a computation tree induced by the Moore machine, except that the tree labels are in $S \times O$, where for every node $t$, the first label element of $\tau(t)$ describes the state of the Moore machine after reading the input $t$ from the initial state, and the second label element describes the last output after reading $t$ from the initial state as before.

A.2 Additional Definitions

In Definition 2, we used the standard definition of parallel composition to say what it means to plug a process implementation into a symmetric architecture. For the sake of completeness, let us formally define this special case of parallel composition.

> Definition 15. Given an architecture $\mathcal{E} = (S, P, \mathcal{AP}_I, E^{in}, E^{out})$ for some process interface $\mathcal{N} = (\mathcal{AP}_I, \mathcal{AP}_O)$ and some Moore machine $M = (Q, \mathcal{I}, O, \delta, q_0, L)$ with $I = 2^{\mathcal{AP}_I}$ and $O = 2^{\mathcal{AP}_O}$, we define the aggregated Moore machine of the architecture and $M$ as $M' = (Q', I', O', \delta', q_0', L')$ with:
- $Q' = (P \rightarrow Q)$,
- $I' = 2^{\mathcal{AP}_I}$,
- $O' = 2^S$,
- for all $f \in Q'$, we have $L'(f) = \{ s \in S \mid \exists (p, x) \in P \times \mathcal{AP}_O : E^{out}(p, x) = s, x \in L(f(p))\}$,
- for all $f \in Q'$ and $X \subseteq \mathcal{AP}_I$, $\delta'(f, X) = f'$ such that for all $p \in P$, $f'(p) = \delta(f(p), \{ x \in \mathcal{AP}_I \mid E^{in}(p, x) \in X \cup L(f(p))\})$, and
- for all $p \in P$, $q_0'(p) = q_0$.

This definition ensures that the values of all signals are “exported” from the aggregated finite-state machine. Thus, when specifying the system behaviour of an aggregated system in a language such as linear-time temporal logic (LTL), we can refer to the signals used internally between the components.

In the main part of the paper, we also define computation trees that encode the behaviour of a rotation-symmetric architecture after we plug one process into it. If the process is a finite-state machine, then the resulting computation tree for the behavior of the complete architecture is regular, and hence can be translated (back) to a Moore machine. We call this Moore machine for the behavior of the complete rotation-symmetric architecture implementation the symmetric product of the single process, whose definition we give next. The reader is reminded that $O$ and $\mathcal{O}$ are defined on page 5.

> Definition 16 (Symmetric product). Given a Moore machine $M = (S, \mathcal{I}, O, \delta, s_0, L)$, we say that a Moore machine $M' = (S', \mathcal{I}, O, \delta', s'_0, L')$ is the symmetric product of $M$ if $S' = S^n$, $s'_0 = (s_0)^n$, and for all $s'_0, \ldots, s'_{n-1} \in S$, $(i_0, \ldots, i_{n-1}) \in \mathcal{I}$:

$\delta'(s'_0, \ldots, s'_{n-1}, (i_0, \ldots, i_{n-1})) = (s'_0, \ldots, s'_{n-1})$
WE can show by induction that for every 
\[ \forall 0 \leq j < n : s^m_j = \delta(s^m_j, \text{rot}((i_0, \ldots, i_{n-1}), -j)) \] and 
\[ L'(s^*_{0}, \ldots, s^*_{n-1}) = (L(s^*_{0}), L(s^*_{1}), \ldots, L(s^*_{n-1})). \]

Note that Definition 16 is just a combination of Definition 3 and the usual definition of parallel composition of Moore machines, applied to architectures consisting of a single cycle of processes.

A.3 Proof of the Symmetry Lemma

Let in the following for every \( i \in \mathbb{N} \) the expression \( \mathcal{O}_i \) denote the local output of process \( i \), i.e., let us define \( \mathcal{O}_i = 2^{\mathcal{AP}_C \times \{i\}} \).

Proof. \( \Leftarrow \): The fact that the computation tree induced by the symmetric product of some Moore machine has the symmetry property follows directly from the definitions.

\( \Rightarrow \): For the converse direction, we prove that from every regular computation tree with the symmetry property, we can construct a Moore machine that is an implementation for one process, and by taking the symmetric product of the Moore machine, we obtain a product machine whose computation tree is in turn the one that we started with.

Let \( (T, \tau) \) be the computation tree to start with. As it is regular, we have an equivalence relation over the nodes in the tree. Let \( [\cdot] \) be the function that maps a tree node in \( T \) onto a tree node representing its equivalence class, so for all \( t, t' \in T \), we have that the sub-trees induced by \( t \) and \( t' \) are the same if and only if \([t] = [t']\), and for every \( t \) there is some \( t' \) such that \([t] = t'\). We build a Moore machine for one process in the symmetric architecture from \( (T, \tau) \) by setting \( \mathcal{M} = (S, \mathcal{I}, \mathcal{O}, \delta, s_{\text{init}}, L) \) with:

\[
\begin{align*}
S &= \{[t] \mid t \in T\} \\
\delta(s, x) &= [sx] \text{ for all } x \in \mathcal{I} \text{ and } s \in S \\
s_{\text{init}} &= [e] \\
L(s) &= \tau(s)_{|\mathcal{O}_n} \text{ for all } s \in S
\end{align*}
\]

We now show that the symmetric product of \( \mathcal{M} \) induces a computation tree that is the same as \( (T, \tau) \). If we take the symmetric product (Definition 16) of \( \mathcal{M} \), we obtain \( \mathcal{M}' = (S', \mathcal{I}, \mathcal{O}, \delta', s_{\text{init}}, L') \) with:

\[
\begin{align*}
S' &= \{([t_0], \ldots, [t_{n-1}] \mid t_0, \ldots, t_{n-1} \in T\} \\
\delta'(t_0, \ldots, t_{n-1}, x) &= ([t_0 \text{ rot}(x, 0)], [t_1 \text{ rot}(x, -1)], \ldots, [t_{n-1} \text{ rot}(x, -n+1)]) \\
s_{\text{init}}' &= ([e], \ldots, [e]) \\
L'((t_0, \ldots, t_{n-1})) &= (\tau(t_0)_{|\mathcal{O}_n}, \tau(t_1)_{|\mathcal{O}_n}, \ldots, \tau(t_{n-1})_{|\mathcal{O}_n})
\end{align*}
\]

Let \( (T', \tau') \) be the extended computation tree induced by \( \mathcal{M}' \) with \( \tau' : T' \to S' \times \mathcal{O} \). We can show by induction that for every \( t \in T' \), we have that \( \tau'(t)_{|S'} = ([\text{rot}(t, 0)], [\text{rot}(t, -1)], [\text{rot}(t, -2)], \ldots, [\text{rot}(t, -n+1)]) \). The induction basis is trivial, as \( \tau'(t)_{|S'}(\epsilon) = ([e], [e], [e], \ldots, [e]) \). For the inductive step, we have:

\[
\begin{align*}
\tau'(tx)_{|S'} &= ([t_0 \text{ rot}(x, 0)], [t_1 \text{ rot}(x, -1)], \ldots, [t_{n-1} \text{ rot}(x, -n+1)]) \\
\text{ for } \tau'(t)_{|S'}(t) &= (t_0, t_1, \ldots, t_{n-1}) \\
\tau'(t)_{|S'}(\epsilon) &= ([\text{rot}(t, 0)], [\text{rot}(t, -1)], \ldots, [\text{rot}(t, -n+1)]) \\
\text{ for } \tau'(t)_{|S'}(t) &= (t_0, t_1, \ldots, t_{n-1}) \\
\tau'(t)_{|S'}(\epsilon) &= ([\text{rot}(t, 0)], \ldots, [\text{rot}(t, -n+1)])
\end{align*}
\]
In step (1)-(2) of this deduction, we applied the definitions of the elements of $\mathcal{M}$ and $\mathcal{M}'$. In step (2)-(3), we used the inductive hypothesis. In step (3)-(4), we used the regularity of the tree: for some $t \in T$ and $x \in \mathcal{I}$, we need to have $[[t]x] = [tx]$ as the subtree induced by $[t]x$ has to be the same as the one induced by $tx$, as otherwise $[t]$ and $t$ would not be in the same equivalence class of subtrees (which is a contradiction). The last step uses the fact that if we concatenate two strings that are rotated by the same number of indices, then we can also first concatenate, and then rotate.

Now let us have a look at the outputs in the extended computation tree $(T', \tau')$. For every $t \in T'$, we have:

$$\tau'(t)|_{\mathcal{O}}$$

$$= L'((\tau'(t)|_{\mathcal{O}}))$$

$$= L'(\{\text{rot}(t,0), \ldots, \text{rot}(t,-n+1)\})$$

$$= (\tau(\{\text{rot}(t,0)\})|_{\mathcal{O}}, \ldots, \tau(\{\text{rot}(t,-n+1)\})|_{\mathcal{O}})$$

$$= (\tau(t)|_{\mathcal{O}}, \tau(t)|_{\mathcal{O}}, \ldots, \tau(t)|_{\mathcal{O}})$$

$$= \tau(t)$$

In step (8)-(9), we simply applied the definition of $L'$. In step (9)-(10), we used the fact that we are dealing with equivalence classes over nodes in the computation tree $(T, \tau)$ that respect the labelling of the system. In step (10)-(11), we use the symmetry property of $(T, \tau)$. For every $i \in \{0, \ldots, n-1\}$, we have $\tau(\{\text{rot}(t,i)\})|_{\mathcal{O}} = \text{rot}(\tau(t),i)|_{\mathcal{O}}$ by this property, and then $\text{rot}(\tau(t),i)|_{\mathcal{O}} = \tau(t)|_{\mathcal{O}}$ by renaming. In the last step, we just plug together the tuple.

**A.4 Correctness of the rep$_S$ Function**

The definition of the rep$S$ function in Section 4.1 is supposed to describe how to compute the symmetry degree of a word, i.e., the number of processes getting the same rotations of an input proposition valuation or the number of rotations of the output of the processes that lead to the same element of $\mathcal{O}$. We prove that the definition of the rep$S$ function achieves this goal in two steps and start with the following sub-lemma:

**Lemma 17.** If there are precisely $m$ values $j \in \{0, \ldots, n-1\}$ (for some $m \in \mathbb{N}$) such that $\text{rot}(t, j) = t$ for some $t \in \mathcal{I}^*$, then the list of indices $L = \{0, \frac{n}{m}, \frac{2n}{m}, \ldots, \frac{(m-1)n}{m}\}$ is precisely the list of indices $\geq 0$ but $< n$ such that for all $l \in L$, we have $\text{rot}(t, l) = t$ but for all $l' \notin L$, we have $\text{rot}(t, l') \neq t$ or either $l' < 0$ or $l' \geq n$.

**Proof.** For all $j, j' \in L$, we know that $j + j' \in L$ as well since for all $t \in \mathcal{I}^*$, $\text{rot}(t, j + j') = \text{rot}(\text{rot}(t, j), j) = \text{rot}(t, j') = t$. Furthermore, $\text{rot}(t, n) = t$.

To show that all elements in $L \cup \{n\}$ are equally spaced (modulo $n$), consider the converse. So we have $0 \leq l < l' < l'' < n$ with $l' - l \neq l'' - l'$ and there are no indices in $L$ in between $l'$ and $l$ or $l''$ and $l'$, respectively. By the argument above if $l' - l < l'' - l'$ we also have $l' + (l' - l) \in L$ or if $l' - l > l'' - l'$ we also have $l + (l'' - l') \in L$, which is a contradiction. The case that involves wrapping around in the modulo space can be proven similarly.

So we know that there are $m$ equally spaced elements in $L$, and by the same line of reasoning, we can also deduce that the spacing between the elements in $L$ is the same as the spacing between $n$ and the largest element in $L$. Since furthermore $\text{rot}(t, 0) = t$ and $\text{rot}(t, n) = t$ for all $t \in \mathcal{I}^*$, the claim follows.
Lemma 17 can alternatively be shown by applying a theorem by Fine and Wilf [8] on the combinatorics on words. To use it, we would however have to rearrange the letters in a word, and describing that construction would be more complicated than giving a direct proof, which is why the latter has been done here.

Lemma 18. For every \( t_0 \ldots t_{k-1} \in \mathcal{I}^k, k \in \mathbb{N} \), we have

\[
\text{rep}_S(t_0 \ldots t_{k-1}) = |\{ j \in \{0, \ldots, n - 1 \} : \text{rot}(t_0 \ldots t_{k-1}, j) = t_0 \ldots t_{k-1} \}|
\]

Proof. The proof is done by induction on the length of \( t \).

Basis: Trivial, since \( \text{rot}(\epsilon, j) = \epsilon \) for every \( j \in \mathbb{Z} \).

Inductive step: Assume that the number of neutral rotations for \( t_0 \ldots t_{k-2} \) is \( m \) (we denote those rotation values \( j \) of \( t_0 \ldots t_{k-2} \) to be neutral for which \( \text{rot}(t_0 \ldots t_{k-2}, j) = t_0 \ldots t_{k-2} \) and the number of neutral rotations for \( t_0 \ldots t_{k-1} \) is \( m' \). By the inductive hypothesis, \( \text{rep}_S(t_0 \ldots t_{k-2}) = m \).

Clearly, \( m' \) is a divisor of \( m \) since otherwise there exists a \( y \in \{ \frac{0}{m'}, \ldots, \frac{(m'-1)n}{m'} \} \) such that \( \text{rot}(t_0 \ldots t_{k-2}, y) \neq t_0 \ldots t_{k-2} \), so:

\[
\text{rot}(t_0 \ldots t_{k-1}, y) = \text{rot}(t_0 \ldots t_{k-2}, y) \text{rot}(t_{k-1}, y) \neq t_0 \ldots t_{k-2} \text{rot}(t_{k-1}, y) = t_0 \ldots t_{k-1}
\]

Analogously, \( m' \) is a divisor of \( \text{rep}(t_k) \). In both cases, we would otherwise get a contradiction with Lemma 17.

On the other hand, for every \( m' \) that is a divisor of \( m \) and \( \text{rep}(t_k) \), we have for all \( y \in \{ \frac{0}{m'}, \ldots, \frac{(m'-1)n}{m'} \} \):

\[
\text{rot}(t_0 \ldots t_{k-1}, y)
= \text{rot}(t_0 \ldots t_{k-2}, y) \text{rot}(t_{k-1}, y)
= t_0 \ldots t_{k-2} \text{rot}(t_{k-1}, y)
= t_0 \ldots t_{k-2} \text{rot}(t_{k-1}, y)
= t_0 \ldots t_{k-1}
\]

Clearly, the greatest common divisor of \( m \) and \( \text{rep}(t_k) \) is the (unique) greatest such number, therefore \( \text{rep}_S(t_0 \ldots t_{k-1}) = m' \).

\[\text{Lemma 18}\]

A.5 Proof of Lemma 8 (The Second Symmetry Lemma)

To keep the presentation of the following proof concise, we need to give a name to the normalization function that maps all input streams that can be unified by rotation onto the same input stream. For all \( t \in \mathcal{I}^* \), we define:

\[
\eta_S(t) = \min_{i \in \{0, \ldots, n-1\}} \text{rot}(t, i)
\]

Definition 19 (Symmetric completion). Let \( \langle T, \tau \rangle \) be a computation tree with \( T = \mathcal{I}^* \) and \( \tau : T \rightarrow \mathcal{O} \). We call a tree \( \langle T, \tau' \rangle \) with \( \tau' : T \rightarrow \mathcal{O} \) a symmetric completion of \( \langle T, \tau \rangle \) if for all \( t \in T \), we have \( \tau'(t) = \text{rot}(\tau(\eta_S(t)), i) \) for some \( i \in \mathbb{N} \) with \( \text{rot}(\eta_S(t), i) = t \).

We are now ready to discuss the proof of Lemma 8.

Proof. The first part of the claim follows directly from the definition of the symmetric completion. For all \( t \in T, i \in \mathbb{N} \), we have

\[
\tau(\text{rot}(t, i))
\]
\[ = \tau(\text{rot}(\eta_S(t), i + j)) \]
\[ = \text{rot}(\tau(\eta_S(t)), i + j) \]
\[ = \text{rot}(\tau(t), i) \]

for \( j = \min_{j \in \mathbb{N}} \text{rot}(r, -j') \) if the symmetric completion actually exists. The symmetric completion exists if and only if having \( \tau'(t) = \text{rot}(\tau(\eta_S(t)), i) \) for some \( i \in \mathbb{N} \) with \( \text{rot}(\eta_S(t), i) = t \) for every \( t \in T \) is possible. The only way for this property to be unfulfilled is if for some \( t \in T \) and \( i, j \in \mathbb{N} \), we have \( \text{rot}(t, i) = \text{rot}(t, j) \) but \( \tau(\text{rot}(t, i)) \neq \tau(\text{rot}(t, j)) \). Equivalently, we can ask if there is the possibility to have \( t = \text{rot}(t, j - i) \) but \( \tau(t) \neq \tau(\text{rot}(t, j - i)) \). Since we require \( \langle T, \tau \rangle \) to have the property that for every \( t \in T \), we have \( \text{rep}_S(t) = \text{rep}_S(\tau(t)) \) and by Lemma 17, the neural rotations are evenly spaced, we can see that \( t = \text{rot}(t, j - i) \) and \( \tau(t) \neq \tau(\text{rot}(t, j - i)) \) cannot hold at the same time.

For the second part, we assume that we are given some finite-state machine \( M = (S, \Sigma, \mathcal{O}, s_{\text{init}}, \delta, L) \) that induces the computation tree \( \langle T, \tau \rangle \). Since the classes of regular trees and finite-state (Moore) machines \( M \) are isomorphic, this assumption comes without loss of generality.

We prove the regularity of \( \langle T, \tau' \rangle \) by building a finite-state machine \( M' = (S', \Sigma, \mathcal{O}, s'_{\text{init}}, \delta', L') \) that induces \( \langle T, \tau' \rangle \).

The states in \( M' \) are the equivalence classes of nodes in \( \langle T, \tau \rangle \). Without loss of generality, let us assume that elements \( t, t' \in T \) such that \( \text{rep}_S(t) \neq \text{rep}_S(t') \) are never put into the same equivalence class. Note that this can only blow up the number of equivalence classes by a factor of at most \( n \).\(^1\) Furthermore assume that the representative element chosen for every equivalence class is a normalized prefix input whenever possible (again, without loss of generality). Thus, for every \( s \in S \) representing a normalized input sequence and \( i \in \mathcal{I} \), \( \min_{u \in \mathbb{N}} \text{rot}(s, u) \) is normalised as well, and so is then \( \min_{u \in \mathbb{N}} \text{rot}(s, u) \). We construct \( M' \) as follows:

\[
S' = S \times \{0, \ldots, -n - 1\}
\]

\[
s'_{\text{init}} = (s_{\text{init}}, 0)
\]

\[
\delta'((s, k), i) = \left( \min_{j \in \mathbb{N}} \text{rot}(s, k) i, j \right), -\argmin_{j \in \mathbb{N}} \text{rot}(s, k) i, j \right)
\]

\[
L'(s, k) = \text{rot}(L(s), k)
\]

Let us now prove that \( M' \) represents the symmetric completion of \( \langle T, \tau \rangle \). For this, it suffices to show that for every \( t \in T \), we have \( \delta'(s_{\text{init}}, t) = (\eta_S(t), -\argmin_{j \in \mathbb{N}} \text{rot}(t, j)) \). By the definition of \( L' \), we then have that \( L'(\delta'(s_{\text{init}}, t)) = \text{rot}(L(\eta_S(t)), -\argmin_{j \in \mathbb{N}} \text{rot}(t, j)) \) (as \( L(\eta_S(t)) = \eta_S(\eta_S(t))) \), which corresponds to the symmetric completion of \( \langle T, \tau \rangle \).

Let us show that we have \( \delta'(s_{\text{init}}, t) = (\eta_S(t), -\argmin_{j \in \mathbb{N}} \text{rot}(t, j)) \) for every \( t \in T \) by induction. The induction basis for \( t = \epsilon \) is trivial. For the inductive step, we have (for \( t \in T \) and \( x \in \mathcal{I} \)):

\[
\delta'(s_{\text{init}}, tx) = (\min_{j \in \mathbb{N}} \text{rot}([\eta_S(t)] j, -\argmin_{j \in \mathbb{N}} \text{rot}(t, j)] x, j)),
\]

\(^1\) In principle, forcing two tree nodes to not be in the same equivalence class if they do not have some common property can make the number of equivalence classes infinite. This is however not the case here as for every \( t \in T \) and \( x \in \mathcal{I} \), \( \text{rep}_S(tx) \) can be computed from \( \text{rep}_S(t) \) and \( x \). This way, computing the \( \text{rep}_S \) values of the prefix input stream can be done on-the-fly by a finite-state machine while reading the input, and when we compute its product with \( M \), the set of states of the resulting finite-state machine is then finite and serves as set of equivalence classes for the tree \( \langle T, \tau \rangle \) such that no tree nodes with different \( \text{rep}_S \) values are put into the same equivalence class.
The proof is done by constructing a specification

\[ \text{rot}((\eta_S(t)), - \arg \min_{j \in \mathbb{N}} \text{rot}(\eta_S(t), x, j)) \]  

\[ = (\min_{j \in \mathbb{N}} \text{rot}(\min_{l \in \mathbb{N}} \text{rot}(t, l), x, j)), \]  

\[ = (\min_{j \in \mathbb{N}} \text{rot}(t, j)) \]  

The first line in this deduction is obtained by applying the induction hypothesis to the definition of \( \eta \). From line (13) to line (14), we applied the definition of \( \eta_S \). From line (14) to line (15), we used the property that by the fact that we are concerned with an equivalence relation over subtrees, we know that for all \( t \in T \) and \( i \in \mathbb{Z} \), we have \( [t]x = [tx] \). This fact also holds for all rotations of \( [t]x \) and \( tx \). From line (15) to line (16), we simplify \( \text{rot}(\min_{j \in \mathbb{N}} \text{rot}(t, l), x, j) \) to \( t \), as in this equation, the two rotations even up. The step to the last line just uses the definition of the \( \eta_S \) function.

\[ \text{A.6 A Complete Proof of EXPTIME-hardness (in the Number of Processes) for Rotation-symmetric Synthesis} \]

We start by concretizing the definition of space-bounded alternating Turing machines.

\[ \text{Definition 20 ([3]).} \] We say that the Turing machine \( M = (Q, \Sigma, \Gamma, \delta, q_0, g) \) is \( f(k) \)-SPACE bounded for some function \( f : \mathbb{N} \to \mathbb{N} \) if for every accepted word of length \( k \), \( M \) also accepts the word when considering all runs whose space usage exceeds \( f(k) \) to be rejecting.

For the scope of this paper, when discussing \( f(k) \)-space bounded Turing machines, we only consider functions \( f(k) \) that are easy to compute (in time polynomial in \( f(k) \)). For every accepted word, we can arrange a set of runs of an alternating Turing machine for that word in a run tree that splits whenever a state with universal branching is visited. All runs in this tree also do not exceed the space bound. By definition, for every accepted word, there exists such a tree, and all of its leaves are accepting configurations.

\[ \text{Lemma 21.} \] Given an \( f(k) \)-space bounded alternating Turing machine \( M = (Q, \Sigma, \Gamma, \delta, q_0, g) \), we can reduce the acceptance of a word \( w \in \Sigma^k \) by \( M \) to the symmetric realizability problem of \( n = f(k) \) processes with a specification in LTL of size polynomial in \( |Q| \cdot |\Gamma| \cdot |w| \).

\[ \text{Proof.} \] The proof is done by constructing a specification \( \psi \) that is realizable in the symmetric setting if and only if \( w = w_0 \ldots w_{k-1} \) is not accepted. We define \( \psi = \psi_1 \land \psi_2 \) for \( \psi_1 \) and \( \psi_2 \) to be given below. We have \( \text{AP} = \{C\} \) and \( \text{AP}^O = \{S^0, \ldots, S^{AP^O}\} \) of sufficient cardinality to encode every element from the set \( \Gamma' = (\Gamma \cup \{\epsilon\} \cup (Q \times \Gamma)) \times 2^{[1,l]} \). This way, the output signals of the individual processes represent locations on the Turing machine tape. For simplicity, in the following, for all \( 0 \leq j < n \), we denote the set of output atomic propositions for process \( j \) by \( S_j \) (with the additional shorthand \( S_{-1} := S_{k-2} \)). We also encode the current state of the machine and tape end markers onto the tape. Note that in the symmetric setting we do not have a designated process for the initial state. The formula \( \psi \) makes sure that precisely the processes retrieving a \( C \) in the first round start a Turing computation (provided that the
two transitions are possible in each state. For this rule is also applied. Note that without loss of generality, we can assume that precisely removing the state information from the part of the tape. If a rejecting state is reached, that the computation is never left of the tape.

Hence, there is only one computation of the Turing machine whereas for universal branching, the choice is made by the external input whereas for universal branching, the choice is made by the system.

We syntactically extend LTL slightly for improved readability by allowing Boolean operations over sets of symbols. For example, $S_0 = X(S_0)$ can be unfolded to $\bigwedge_{p \in S_0} (p \leftrightarrow Xs)$. Furthermore, $S_{-1}, S_0, S_{+1} \xrightarrow{\delta} X(S_{-1}), X(S_0), X(S_{+1})$ for $a \subseteq \{1, 2\}$ is true if for the part of the tape represented by $S_{-1}\{r, s\rceil, S_{+1}\rceil r\}$, the transition from $S_0\{Q\}$ can be made such that afterwards $S_{-1}, S_0, S_{+1}$ is a valid part of the configuration (at the same place on the tape), the next state is included at the respective position on the tape, and we have taken the 6th of the two possible transitions for $b \in a$. Furthermore the tape is extended correctly such that the computation is never left of the \[ marker or right of the \[ marker (as seen from the initial configuration). If two markers collide, the next configuration is obtained by simply removing the state information from the part of the tape. If a rejecting state is reached, this rule is also applied. Note that without loss of generality, we can assume that precisely two transitions are possible in each state. For $\hat{\Gamma} = (\epsilon \cup \Gamma) \times 2^{\{1, 2\}}$, we set:

\[
\psi_2 = G(S_0) \text{ is in } Q \times \Gamma \times 2^{\{1, 2\}} \wedge g(S_0|Q) = "\wedge" \rightarrow \\
(S_{-1}, S_0, S_{+1} \xrightarrow{\delta} X(S_{-1}), X(S_0), X(S_{+1}))) \\
\wedge G(S_0) \text{ is in } Q \times \Gamma \times 2^{\{1, 2\}} \wedge g(S_0|Q) = "\vee" \wedge \neg C \rightarrow \\
(S_{-1}, S_0, S_{+1} \xrightarrow{\delta} X(S_{-1}), X(S_0), X(S_{+1}))) \\
\wedge G(S_0) \text{ is in } Q \times \Gamma \times 2^{\{1, 2\}} \wedge g(S_0|Q) = "\vee" \wedge C \rightarrow \\
(S_{-1}, S_0, S_{+1} \xrightarrow{\delta} X(S_{-1}), X(S_0), X(S_{+1}))) \\
\wedge G((S_0 \text{ is in } \hat{\Gamma}) \wedge (S_{-1} \text{ is in } \hat{\Gamma}) \wedge (S_{+1} \text{ is in } \hat{\Gamma}) \rightarrow \\
S_0 = X(S_0) \\
\wedge G(\neg g(S_0|Q) \text{ is accepting})
\]

Assume that there exists an accepting tree of $M$’s computations for $w$. In this case, the environment could set the input to the first process to true in the first round and to false for the other processes. Hence, there is only one computation of the Turing machine being simulated. By the environment choosing the existential branching according to the acceptance tree it can be assured that eventually an accepting state is reached, which is not allowed by $\psi$. Therefore $\psi$ is unrealizable in this setting.

On the other hand, if $w$ is not accepted by $M$, then there exists no tree of accepting runs of $M$ (that do not use more than $f(k)$ space) for $w$. Since in this case the implementation can decide which transition to take in case of universal branching, it can assure that the run simulated by an implementation of $\psi$ either ends in a rejecting state or exceeds the space limit. Since in case of collisions of end markers on the tape, the state information can be removed from the output and the processes can then output their last tape contents forever, the specification is trivially fulfilled in this case. The same applies for the case of reaching a rejecting state, so $\psi$ is realizable by a symmetric system.
A.7 Proof of Lemma 13

Proof. Let $\psi$ be the specification from Lemma 12. We show that there exists an implementation for the specification $\psi$ in the A0 architecture if and only if there exists a joint implementation for the two processes in the S2 architecture that satisfies $\psi' = \psi_d \land G(v \leftrightarrow Xo) \land G(w \leftrightarrow Xp)$, where $\psi_d$ results from prefixing all occurrences of the signals $y$ and $z$ in $\psi$ with a next-time operator. Without loss of generality, we assume that $\psi$ encodes the termination of a Turing machine.

$\Rightarrow$: If we have an implementation for the A0 architecture satisfying $\psi$, then the implementation needs to be a symmetric one: both processes output the same bitstream when reading a true value from their respective local input signal for the first time. We can take an implementation for one of these processes, and turn it into an implementation for a process in the S2 architecture: just simulate the process over the input signal $a$ and use $g$ as the local output for the tape content. At the same time, copy all values from $b$ to $e$, and from $c$ to $f$. This makes sure that $G(v \leftrightarrow Xo) \land G(w \leftrightarrow Xp)$ is satisfied by the resulting system. Since the bottom process in the S2 architecture then outputs $q$ with one computation cycle of delay to $y$, $y$ in the S2 architecture always represents the output of the left process in the A0 architecture with a delay of one cycle. For the signal line from $v$ to $z$, the same line of reasoning holds: the data from $v$ appears at the signal $o$ with a delay of one, and then, since every process in the S2 architecture simulates a process in the A0 architecture reading from $a$ and writing to $g$, $z$ is the output of the A0 process for the input $v$ with a delay of one cycle. Thus, $\psi_d$ is fulfilled by the system. Taking all of these facts together, the architecture with the implementation also fulfills $\psi$.

$\Leftarrow$: Assume that $\psi'$ is realizable for the S2 architecture and we have a process that ensures that $\psi'$ is satisfied in the Moore machine that represents the behavior of the complete architecture with the process implementation. We argue that the process has to behave like a process for the A0 architecture for the input $a$ and output $g$. The important feature of this architecture is that the process does not know if the local input $b$ is the (delayed) $a$ input to the other process, or if its $c$ input is the (Turing machine tape) output of the other process. Thus, it cannot find out if it is the top process or the bottom process in the architecture and must prevent violating the specification in either case.

Recall that without loss of generality, we assumed $\psi_D$ to encode the computation/acceptance of a Turing machine (in the same way as Pnueli and Rosner defined it [21]). First of all, in order to satisfy the specification, both processes have to output the first two Turing tape computations on their $g$ outputs when obtaining a true value to the $a$ input. This follows from the fact that the specification only allows the processes to forward information from the inputs $b$ and $c$, so the overall requirement to start with the first two tape contents on $y$ when reading a true-bit on $u$, and to start with the first two tape contents on $z$ when reading from $v$ can only be fulfilled by distributing the writing of the two tapes among the processes.

Now assume that a process receives the first Turing tape configurations on local input $c$, then a start signal on input $a$ while the second Turing tape content starts, and after both Turing tape contents have been seen, we get a starting signal on $b$. Let this input stream be called the reference stream.

Since the process does not know whether it is the top-most one in the architecture, it also has to output the third Turing tape configuration on its local output $g$ after the first two of these, as the input to $b$ might have been forwarded to the bottom-most process, where it triggered the other process to output the first two tape configurations. Then, $\psi_D$ would be violated if the top-most process did not output the first three configurations. But then,
if the process is the lowest-most one, as the local input \( c \) might actually be the output of the top-most process, must also output the first three Turing tape configurations in order not to violate the specification. Note that the lower-most process must do that regardless of its local input \( b \), as it is just forwarded garbage from global input \( w \) then.

But then, this means that the top-most process also has to output the first four Turing tape configurations when reading the reference stream by the same reasoning - it might be the top-most process, and since it has forwarded a signal that would trigger the other process to start the Turing tape computation one tape content later, it would otherwise violate the specification.

We can iterate this argument ad infinitum. Now if the process ensures that the overall system, when the process is instantiated in the S2 architecture, satisfies the specification, then this means that the Turing machine has to terminate — since we can force the system to output the correct Turing tape computations along a run of the Turing machine, and we also require it to eventually halt, there is no other way that the specification can be satisfied.

### A.8 Proof of Theorem 14

We first provide a pair of compression functions for LTL.

> **Definition 22.** Let \( \text{AP} \) be some set of signals, which, w.l.o.g, we assume to be \( \{x_1, \ldots, x_n\} \).

We define a compression function \( f^{\text{LTL}} \) over \( \text{AP} \) as follows: for every \( w = w_0w_1w_2 \ldots \in (2^{\text{AP}})^\omega \), we set \( f^{\text{LTL}}(w) = w'_0w'_1w'_2w'_3 \ldots \) such that:

\[
\forall i \in \mathbb{N}, \quad w'_{2i(n+1)} = w_{2i(n+1)+1} = \chi,
\]

\[
\forall i \in \mathbb{N} \text{ and } j \in \{1, \ldots, n\}, \quad w'_{2i(n+1)+2j} = \emptyset, \text{ and}
\]

\[
\forall i \in \mathbb{N} \text{ and } j \in \{1, \ldots, n\}, \quad \chi \in w'_{2i(n+1)+2j+1} \text{ if and only if } x_j \in w_i.
\]

The compression function \( f^{\text{LTL}} \) is exemplified in Figure 4.

Our interest in \( f^{\text{LTL}} \) lies in the fact \( f^{\text{LTL}} \) has an adjunct specification compression function \( f^{\text{LTL}} \) for LTL properties. For the following lemma, we use the fact that the LTL operators \( F \) and \( G \) can be encoded using the \( X \) and \( U \) operators, so we only need to consider the latter two here. Given a word \( w = w_0w_1w_2w_3 \ldots \in (2^{\text{AP}})^\omega \), an index \( i \in \mathbb{N} \), and an LTL formula \( \varphi \), we write \( w, i \models \varphi \) if and only if \( w_0w_1w_2w_3 \ldots \models \varphi \).

> **Lemma 23.** A specification compression function \( f^{\text{LTL}} \) that corresponds to \( f^{\text{LTL}} \) can be defined inductively over the structure of an LTL formula as follows (for \( \text{AP} = \{x_1, \ldots, x_n\} \)):

For \( \psi = \text{false} \), we set \( f^{\text{LTL}}(\psi) = \text{false} \). Likewise, for \( \psi = \text{true} \), we set \( f^{\text{LTL}}(\psi) = \text{true} \).

For \( \psi = \psi_1 \land \psi_2 \), \( \psi = \psi_1 \lor \psi_2 \), and \( \psi = \neg \psi_1 \) for some LTL formulas \( \psi_1 \) and \( \psi_2 \), we have \( f^{\text{LTL}}(\psi) = f^{\text{LTL}}(\psi_1) \land f^{\text{LTL}}(\psi_2) \), \( f^{\text{LTL}}(\psi) = f^{\text{LTL}}(\psi_1) \lor f^{\text{LTL}}(\psi_2) \), and \( f^{\text{LTL}}(\psi) = \neg f^{\text{LTL}}(\psi_1) \), respectively.

For \( \psi = x_j \) for some \( x_j \in \text{AP} \), we set \( f^{\text{LTL}}(\psi) = X^{2j+1} \).

For \( \psi = X \psi_1 \) for some LTL formula \( \psi_1 \), we set \( f^{\text{LTL}}(\psi) = X^{2(n+1)} f^{\text{LTL}}(\psi_1) \).

For \( \psi = \psi_1 U \psi_2 \), we set \( f^{\text{LTL}}(\psi) = (X \land X \land X^2 \land \chi) \land \psi_1 \lor ((X \land X \land X^2 \land \chi) \land \psi_2) \).

**Proof.** We show the lemma by structural induction. More specifically, we show that for every \( w \in (2^{\text{AP}})^\omega \) and \( i \in \mathbb{N} \), we have \( w, i \models \psi \) if and only if \( w', 2(n+1) \cdot i \models f^{\text{LTL}}(\psi) \) for \( w' = f^{\text{LTL}}(w) \).

Case \( \psi = \text{true} \), \( \psi = \text{false} \): trivial
Case \( \psi = x_j \) for some \( x_j \in \text{AP} \). The definition of \( f^{\text{LTL}} \) ensures that for all \( j \in \{1, \ldots, n\} \), we have \( x_j \in w_i \) if and only if \( \chi \in w_{2(i(n+1)+j+1)} \). Thus, we have \( w', 2(n+1) \models X^{j+1} \chi \) if and only if \( w, i \models x_j \).

Case \( \psi = \psi_1 \land \psi_2 \), \( \psi = \psi_1 \lor \psi_2 \), and \( \psi = \neg \psi_1 \): trivial

Case \( \psi = X \psi_1 \): follows from the inductive hypothesis and the definitions of \( f^{\text{LTL}} \) and \( f'^{\text{LTL}} \)

Case \( \psi = \psi_1 \cup \psi_2 \). Here, \( \chi \land X \chi \land X^2 \neg \chi \) is true precisely at time points \( 2(n+1)i \) for some \( i \in \mathbb{N} \), thus anything of interest for evaluating \( f'\text{LTL}(\psi) \) happens at these time instants. For \( f'\text{LTL}(\psi) \) to be true, we must have that for some \( i, u, v, w \), we get that \( w', 2(n+1)i \models f'\text{LTL}(\psi_2) \), which by the induction hypothesis is equivalent to \( w, i \models \psi_2 \).

For all \( j < i \), we must have \( w', 2(n+1)j \models f'\text{LTL}(\psi_1) \), which by the induction hypothesis is equivalent to \( w, j \models \psi_1 \).

Reconsider the setting from Figure 4. As an example, the specification \( x_3 \cup x_3 \) for the original case translates to \( ((\chi \land X \chi \land X^2 \neg \chi) \rightarrow X^9 \chi) \cup ((\chi \land X \chi \land X^2 \neg \chi) \land X^7 \chi) \) for the compressed case. In both variants, the specification is not fulfilled for this example.

Using Lemma 23, we can now prove Theorem 14:

**Proof.** Since we can compress (1) the input signals \( u, v, \) and \( z \) into one signal (named \( x \) in the S0 architecture), (2) \( a, p, \) and \( q \) into one signal, (3) \( u, v, \) and \( z \) into one signal, and (4) adapt \( \psi' \) accordingly (and all of these compressions can use the same encoding), the undecidability of the symmetric synthesis problem for the S0 architecture follows from the undecidability of the symmetric synthesis problem for the S2 architecture. Definition 22 and Lemma 23 describe how this word compression step can be performed. However, we need to make sure that (1) the correct functioning of the processes in the S0 architecture is only enforced on input streams that result from compressing a word over \( 2^{u,v,w} \) according to Definition 22 and (2) the output streams of the processes need to be correct compressions if the input to the first process is a valid compressed word. For this, we take the adapted version of \( \psi' \) and replace it by \( (\psi' \land \phi_{\text{correct}}) \lor F\phi_{\text{invalid}1} \lor \phi_{\text{invalid}2} \), where \( \phi_{\text{invalid}1} \) and \( \phi_{\text{invalid}2} \) encode that a part of the input stream is found that shows that it can not have been obtained by word compression according to Definition 22. Formally, we can describe these properties as:

\[
\phi_{\text{invalid}1} = \chi \land X \chi \land XX \neg \chi \land \left( -X^8 \chi \lor -X^3 \chi \lor X^{10} \chi \lor \bigvee_{i \in \{1, \ldots, 3\}} X^{2i} \chi \right)
\]

\[
\phi_{\text{invalid}2} = \neg \chi \lor \neg X \chi \lor XX \chi
\]

Intuitively, \( \phi_{\text{invalid}1} \) states that starting from a character start sequence, the next character start sequence does not come after exactly 8 cycles (or we have an illegal bit encoding along the way), and \( \phi_{\text{invalid}2} \) states that the input stream does not start with a character start sequence.

In the same way, we can encode that \( y \) and \( z \) represent correctly compressed streams:

\[
\phi_{\text{correct}} = \bigwedge_{p \in \{x,y\}} p \land Xp \land X^2 - p \land G\left( \neg p \lor \neg Xp \lor X^2 p \lor \left( \bigwedge_{i \in \{1, \ldots, 3\}} X^{2i} p \land X^8 p \land X^9 p \land X^{10} \neg p \right) \right)
\] (18)