Advanced superionic conductor (ASIC)/electrochemical indifferent electrode (IE) heterostructures are the key elements of ion transport. Heterojunctions (in the area of DE/L) is a cause of the low K. The absence of FIT in the area of ASIC/IE functional electrolytes and superionic conductors (SICs) [1]. Advanced batteries and supercapacitors) can be made on the basis of some types of microsources (thin-film rechargeable NSs) necessary for development of NMST and WNs. Fuel cells provide the response of solid state ionic material/electrochemical interfaces with high energy densities (smaller $\rho _E$ than conventional capacitors. The delayed ion transport in DEL is the cause of more low $\rho _E$. The experiments on the creation of ASIC/IE lattice-matched heterojunction with FIT in DEL were first carried out at the IMT RAS (1991-1992) [4]. The appropriate results were first published in [10, 11, 13]. Recently, for the increase of $\rho _E$ and $\rho _W$ densities in DEL the conception of ASIC/IE functional coherent interfaces (with $\rho _C \sim 100 \, \mu F/cm^2$ at the high frequencies) was proposed [10-14].

In this work the approach «from advanced materials to advanced devices» [13] and nanoionics [15] are used to create solid-state nanionic sources (NS) [2-4]. The aim is to create innovative heterostructures with a special interface design of heterojunctions on the ASIC basis, providing record high values of capacity and functioning frequency. The heterostructures considered are the basis of high-frequency NSs necessary for development of NMST and WNs.

## 1. INTRODUCTION

The response of solid state ionic material/electrochemical indifferent electrode (IE) interfaces to external electric fields is of both fundamental and practical interest. For instance, the main obstacle for development of nano(micro)system technology (NMST) and wireless microsensors and microrobots networks (WN) is the absence of autonomous microsources with high energy $\rho _E$ and power $\rho _W$ densities. Traditional approaches to the creation of devices for energy storage are based on rational use of volume. However, at the nano- and microscale “surface-to-volume” relation is large. Therefore, it needs the maximum use of interface properties to achieve effective energy storage and power generation.

Some types of microsources (thin-film rechargeable batteries and supercapacitors) can be made on the basis of solids with fast ion transport (FIT), i.e. on the basis of solid electrolytes and superionic conductors (SICs) [1]. Advanced superionic conductors (ASICS) present the subclass of SICs [2-4]. ASICS are solids with specific crystal structure (close to optimal for FIT), record high level of ionic conductivity $\sigma_1$ ($=0.1 \, \text{Ohm}^{-1} \cdot \text{cm}^{-1} \, 300 \, \text{K}$) and small activation energy of FIT ($=0.1 \, \text{eV}$). Decades, ASICS are used in supercapacitors - devices where the energy and charge store in double electric layers (DELS) at the ASIC/IE functional interfaces. The DEL-thickness is an order of molecule size. In the existing designs of supercapacitors with liquid electrolytes and volume-distributed electrodes from various kinds of nanostructured carbon, specific capacities are $=100 \, \text{F/g}$ at internal surfaces $=10^7 \, \text{cm}^2 / \text{g}$ [5], which gives a true $\rho _C$ value of $\approx 10 \, \mu F/cm^2$. Values of the same order are characteristic of DELs on ASIC/IE electrode heterojunctions [6]. However, liquid electrolytes are not applicable in microelectronics. Solid state supercapacitors on the basis of ASIC have DEL with real surface capacity $\rho _C \approx 100 \, \mu F/cm^2$ only at low frequencies ($f \approx 10^{-2}-10^{-7} \, \text{Hz}$) and $\rho _C \approx 10 \, \mu F/cm^2$ when $f \approx 10^{-2}-10^{-1} \, \text{Hz}$ [6]. It looks like a paradox because the mobile ions in the ASIC crystal structure oscillate between neighbor next crystallographic positions with frequencies of $\approx 10^{15}$ Hz at 300 K. The absence of FIT in the area of ASIC/IE functional heterojunctions (in the area of DEL) is a cause of the low operational frequencies. Distortion and disorder of specific ASIC crystal structure at the heterointerfaces lead the delayed ion transport.

The microsources with different “energy-power” relation are needed for NMST and WN. Fuel cell provide $\rho _E \approx 6$ times larger but $\rho _W$ lower than those of the Li-ion microbatteries [7-9]. On the Ragone plot ($\rho _E / \rho _W$) [8], ASIC based supercapacitors occupy an intermediate place between Li-ion batteries and conventional capacitors. Supercapacitors have more $\rho _E$ (smaller $\rho _W$) than conventional capacitors. The delayed ion transport in DEL is the cause of more low $\rho _E$. The experiments on the creation of ASIC/IE lattice-matched heterojunction with FIT in DEL were first carried out at the IMT RAS (1991-1992) [4]. The appropriate results were first published in [10, 11, 13]. Recently, for the increase of $\rho _E$ and $\rho _W$ densities in DEL the conception of ASIC/IE functional coherent interfaces (with $\rho _C \sim 100 \, \mu F/cm^2$ at the high frequencies) was proposed [10-14].

In this work the approach «from advanced materials to advanced devices» [13] and nanoionics [15] are used to create solid-state nanionic sources (NS) [2-4]. The aim is to create innovative heterostructures with a special interface design of heterojunctions on the ASIC basis, providing record high values of capacity and functioning frequency. The heterostructures considered are the basis of high-frequency NSs necessary for development of NMST and WNs.

## 2. EXPERIMENTAL RESULTS

Experiments on the creation of ASIC/IE coherent heterojunctions at the UHV conditions were carried out at IMT RAS in 2004-2005 for the first time. They give the patent important information. The NS laboratory samples with a special ASIC/IE heterojunction design and giant values of capacity density ($\rho _C$) and charge density ($\rho _Q$) were created. In this paper we report the electric characteristics of three samples (A, B, C) with the same type of the ASIC/IE interface design, and, simultaneously with different compositions and crystal structures of ASICS and/or IEs. The electrical characteristics of the samples were investigated by means of impulse technique. II-impulses of voltage from generator were applied to series circuit of the investigated heterostructure and load resistance. The dependences of voltage on the heterostructures during of charge-discharge process were registered by an oscilloscope.

The oscillograms of charge (duration 0.17 ms) – discharge (in coordinates “voltage-time”) of the experimental heterostructure (sample A) with a smooth IE (without microroughness) are presented in Fig.1. On the time intervals $\approx 0.2$ ms and current densities $j \approx -0.01 -0.3 \, \text{A/cm}^2$ (300 K) the heterostructure demonstrates “capacitor-like” behavior with $\rho _C \approx300 \, \mu F/cm^2$. This value found by the comparison with a charge-discharge curve (osscillogram 5) of conventional capacitor with the known capacity. At the accumulation charge density $\rho _Q \approx 2 \times 10^8 \, \text{C/cm}^2$ (osscillogram 2), the transition to “battery-like” behavior occurs (osscillogram 3). The distinctive features of the “battery-like” behavior are the flat sections...
Fig. 1. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample A) at 300 K in coordinates “voltage–time”. Horizontal scale is 0.05 ms/div.

1 - heterostructure, charge-discharge through relative resistance 100r, discharge current density \( j = 0.02 \text{ A/cm}^2 \), “capacitor-like” behavior, \( \rho_c \approx 300 \mu\text{F/cm}^2 \); 2 - heterostructure (10r, \( j = 0.3 \text{ A/cm}^2 \), “capacitor-like” behavior, \( \rho_0 \approx 10^{-5} \text{ C/cm}^2 \)); 3 - heterostructure (1r, \( j = 2 \text{ A/cm}^2 \), transition from “hybrid” to “battery-like” behavior, \( \rho_0 \approx 5 \times 10^{-3} \text{ C/cm}^2 \); 4 - heterostructure (0.1r, \( j = 8 \text{ A/cm}^2 \), “battery-like” behavior, failure of the charge accumulation mode); 5 - conventional capacitor (reference capacitor), charge-discharge through relative resistance 100r; 6 - the form of impulse of applied external voltage to heterostructure.

Fig. 2 shows the charge (1.7 ms) – discharge oscillograms for experimental heterostructure (A) at 300 K. The transition to “battery-like” behavior occurs within ±0.5 ms when the stored charge density \( \rho_0 \approx 1.5 \times 10^{-4} \text{ C/cm}^2 \) (oscillogram 2) is achieved. The data of Fig. 1 and Fig. 2 suggest the existence of the critical value \( \rho_0 \approx 10^{-5} \text{ C/cm}^2 \) (300 K). It is of the order of \( \rho_0 \) on the densely packed planes (ions of the same sign) in the ionic crystals. It can be assumed that the transition to “battery-like” behavior occurs when mobile ions leave the contact layer of ASIC (nearest to IE). It also follows from Fig. 2 (oscillogram 1 and 4), that \( \rho_{eq} \approx 170 \rho_0 \) (\( \rho_c \approx 300 \mu\text{F/cm}^2 \)). So, the equivalent capacitor should have \( \rho_{eq} \approx 50000 \mu\text{F/cm}^2 \) for the time intervals ~2 ms (\( f \approx 1 \text{ kHz} \).

The oscillograms of charge (18 ms) – discharge of the experimental heterostructure (300 K, sample A) are given in Fig. 3. The transition to “battery-like” behavior occurs at \( \rho_{eq} \approx 2 \times 10^{-4} \text{ C/cm}^2 \), which corresponds to the data of Fig. 1 and Fig. 2. For the oscillograms 1 (Fig. 1) and 4 (Fig. 3), the values of \( \rho_0 \) differ by 2000 times, so within 20 ms time intervals (frequencies \( f \approx 100 \text{ Hz} \)) the equivalent capacitor should have \( \rho_{eq} \approx 600000 \mu\text{F/cm}^2 \). The same value was obtained by the comparison with an accumulative charge of the conventional capacitor (Fig. 3, the oscillogram 5).

Fig. 3. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample A) at 300 K. Horizontal scale is 5 ms/div.

1 - heterostructure, charge-discharge through relative resistance 100r, discharge current \( j = 0.03 \text{ A/cm}^2 \), transition to “battery-like” behavior, \( \rho_0 \approx 10^{-5} \text{ C/cm}^2 \); 2 - heterostructure (10r, \( j = 0.3 \text{ A/cm}^2 \), “battery-like” behavior, \( \rho_0 \approx 5 \times 10^{-3} \text{ C/cm}^2 \)); 3 - heterostructure (1r, \( j = 2 \text{ A/cm}^2 \), “battery-like” behavior, \( \rho_0 \approx 5 \times 10^{-3} \text{ C/cm}^2 \); 4 - heterostructure (0.1r, \( j = 8 \text{ A/cm}^2 \), “battery-like” behavior, failure of the charge accumulation mode, \( \rho_0 \approx 10^{-2} \text{ C/cm}^2 \)); 5 - conventional capacitor, charge-discharge through 100r; 6 - the form of applied external voltage impulse.
Fig. 4 shows the charge (370 ms) – discharge oscillograms for experimental heterostructure (A) at 300 K. The comparison of the charge accumulation by the heterostructure within 370 ms time and by conventional capacitor (Fig.4, oscillograms 3 and 5) gives \( \rho_{C_Q} \approx 600000 \, \mu \text{F/cm}^2 \).

Fig.4. Charge-discharge oscillograms of the ASIC/Smooth IE experimental heterostructure (sample A) at 300 K. Horizontal scale is 100 ms/div.
1 - heterostructure, charge-discharge through relative resistance 100r, discharge current \( j \approx 0.03 \, \text{A/cm}^2 \), "battery-like" behavior, \( \rho_0 \approx 1 \times 10^2 \, \text{C/cm}^2 \); 2 - heterostructure (10r, \( j \approx 0.3 \, \text{A/cm}^2 \), "battery-like" behavior \( \rho_0 \approx 1 \times 10^3 \, \text{C/cm}^2 \)); 3 - heterostructure (1r, \( j \approx 2 \, \text{A/cm}^2 \), "battery-like" behavior, failure of the charge accumulation mode, \( \rho_0 \approx 3 \times 10^3 \, \text{C/cm}^2 \)); 4 - heterostructure (0.1r, \( j \approx 6 \, \text{A/cm}^2 \), "battery-like" behavior, failure of the charge accumulation mode, \( \rho_0 \approx 2.4 \times 10^3 \, \text{C/cm}^2 \)); 5 - conventional capacitor, charge-discharge through 100r; 6 - the form of applied external voltage impulse.

The influence of temperature on the internal resistance, \( \rho_{CQ} \), \( \rho_{Cm} \) and \( \rho_0 \) in the experimental heterostructures was investigated. The oscillograms of charge (370 ms) – discharge of the sample A at 370 K are given in Fig.6.

Fig.5. Charge-discharge oscillograms of the ASIC/Smooth IE experimental heterostructure (sample A) at 300 K. Horizontal scale is 5 \( \mu \text{s/div} \).
1 - heterostructure, charge-discharge through relative resistance 10r, discharge current \( j \approx 0.2 \, \text{A/cm}^2 \), "capacitor-like" behavior, \( \rho_C \approx 100 \, \mu \text{F/cm}^2 \); 2 - heterostructure (1r, \( j \approx 0.3 \, \text{A/cm}^2 \), "capacitor-like" behavior); 3 - heterostructure (0.1r, \( j \approx 10 \, \text{A/cm}^2 \), "capacitor-like" behavior); 4 - conventional capacitor, charge-discharge through 10r; 5 - the form of applied external voltage impulse.

The oscillograms of charge (20 \( \mu \text{s} \)) – discharge of the experimental heterostructure (A) at 300 K are given in Fig.5. The comparison of the charge accumulated by the heterostructure and by conventional capacitor (Fig.5, oscillograms 1 and 4) gives \( \rho_C \approx 100 \, \mu \text{F/cm}^2 \). (f \( \sim 10^5 \) Hz).

Fig.6. Charge-discharge oscillograms of the ASIC/Smooth IE experimental heterostructure (sample A) at 370 K. Horizontal scale is 100 ms/div.
1 - heterostructure, charge-discharge through relative resistance 100r, discharge current \( j \approx 0.04 \, \text{A/cm}^2 \), "battery-like" behavior, \( \rho_0 \approx 1.6 \times 10^2 \, \text{C/cm}^2 \); 2 - heterostructure (10r, \( j \approx 0.4 \, \text{A/cm}^2 \), "battery-like" behavior, \( \rho_0 \approx 1.6 \times 10^3 \, \text{C/cm}^2 \)); 3 - heterostructure (1r, \( j \approx 3 \, \text{A/cm}^2 \), "battery-like" behavior, beginning of failure of the charge accumulation mode, \( \rho_0 \approx 1.2 \, \text{C/cm}^2 \)); 4 - heterostructure (0.1r, \( j \approx 17 \, \text{A/cm}^2 \), "battery-like" behavior, failure of the charge accumulation mode, \( \rho_0 \approx 6 \, \text{C/cm}^2 \)); 5 - conventional capacitor \( C_1 \), charge-discharge through 100r resistor; 6 - conventional capacitor \( C_2 = 4.3 \, \text{C} \), charge-discharge through 100r; 7 - the form of applied external voltage impulse.
Fig. 7 shows the charge (200 ms) – discharge oscillograms of the experimental heterostructure (sample B) with smooth IE (at 440 K). The heterostructure displays a distinct “capacitor-like” behavior with $\rho_C > 200000 \mu\text{F/cm}^2$ and $\varphi \approx 880^\circ$ (oscillogram 1). The conventional capacitor (oscillogram 5) had $\varphi \approx 790^\circ$ under the same conditions. The transition to the “battery” behavior occurs at $\rho_Q \approx 0.1 \text{C/cm}^2$ (oscillogram 2).

![Fig. 7. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample B) at 440 K. Horizontal scale is 50 ms/div.](image)

1 - heterostructure, charge-discharge through relative resistance $10r$ relative number, discharge current $j = 0.3 \text{A/cm}^2$, “capacitor-like” behavior, $\rho_C > 200000 \mu\text{F/cm}^2$, $\rho_Q = 6 \times 10^4 \text{C/cm}^2$; 2 - heterostructure $(1r, j = 5.5 \text{A/cm}^2$, transition to “battery-like” behavior, $\rho_Q = 1 \text{C/cm}^2$, $\rho_C \approx 3.7 \text{F/cm}^2$); 3 – heterostructure $(0.1r, j = 50 \text{A/cm}^2$, “battery-like” behavior, $\rho_Q = 10 \text{C/cm}^2$, $\rho_C \approx 33 \text{F/cm}^2$); 4 - heterostructure $(0.01r$, $j = 260 \text{A/cm}^2$, “battery-like” behavior failure of the charge accumulation mode, $\rho_Q = 40 \text{C/cm}^2$, $\rho_C \approx 40 \text{F/cm}^2$); 5 - conventional capacitor, charge-discharge through $10r$; 6 - the form of applied external voltage impulse.

The oscillagrams of charge (200ms) – discharge of the sample B at 300K are given in Fig.8. At the time intervals $\approx 200 \text{ms}$ and $j \approx 0.3-5 \text{A/cm}^2$ the value $\rho_C \approx 200000 \mu\text{F/cm}^2$ is achieved. Thus, the obtained experimental data of $\rho_C$ for ASIC/IE heterojunctions with special interface design considerably exceed the known experimental values [6,16] and recent theoretical estimations [3,4].

![Fig. 8. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample B) at 300 K. Horizontal scale is 50 ms/div.](image)

1 - heterostructure, charge-discharge through relative resistance $10r$, discharge current $j = 0.01 \text{A/cm}^2$, “capacitor-like” behavior, $\rho_C > 200000 \mu\text{F/cm}^2$; 2 - heterostructure $(10r, j = 0.2 \text{A/cm}^2$, “capacitor-like” behavior, $\rho_C > 200000 \mu\text{F/cm}^2$); 3 - heterostructure $(1r, j = 4 \text{A/cm}^2$, transition to “battery-like” behavior, $\rho_Q = 0.7 \text{C/cm}^2$, $\rho_C \approx 2 \text{F/cm}^2$); 4 - heterostructure $(0.1r, j = 33 \text{A/cm}^2$, “battery-like” behavior, beginning of the failure of the charge accumulation mode, $\rho_Q = 5 \text{C/cm}^2$, $\rho_C \approx 15 \text{F/cm}^2$); 5 - heterostructure $(0.01r, j = 90 \text{A/cm}^2$, “battery-like” behavior, failure of the charge accumulation mode); 6 - conventional capacitor, charge-discharge through $10r$; 7 - the form of applied external voltage impulse.

The influence of the II-impulse amplitude of applied external voltage on the plateau position at “battery-like” behavior was investigated. Figures 9, 10 and 11 present the charge-discharge oscillograms obtained at the same sensitivity (V/div) when the voltage steps of the fixed form were applied to the heterostructure (sample B). The ratio of the maximum impulse amplitudes in the figures is 1:2:4. Figure 9 shows that an increase of the external voltage amplitude by 2 times after the heterostructure transition to “battery-like” behavior does not affect the position of charge (discharge) plateau. However, if this transition occurs at the voltage twice as large, it is the voltage that determines the position of charge (discharge) plateau. The charge plateau voltage virtually coincides with that of discharge. Similar conclusions can be drawn from Fig. 11, which shows that an increase in the external voltage amplitude of the step by 2 times (as compared to the corresponding step in Fig.10) shifts the charge (discharge) plateau to the position corresponding to external voltage twice as large.
Fig. 9. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample B) at 440 K. Horizontal scale is 100 ms/div. 
1 - heterostructure, charge-discharge through relative resistance 100 r; 
2 - heterostructure, charge-discharge through 10 r; 
3 - heterostructure charge-discharge through 1 r, failure of the charge accumulation mode; 4 - the form of applied external voltage impulse.

Fig. 10. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample B) at 440 K. Horizontal scale is 100 ms/div. 
1 - heterostructure, charge-discharge through relative resistance 100 r; 
2 - heterostructure, charge-discharge through 10 r; 
3 - heterostructure charge-discharge through 1 r, failure of the charge accumulation mode; 4 - conventional capacitor, 100 r; 
5 - the form of applied external voltage impulse.

Fig. 11. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample B) at 440 K. Horizontal scale is 100 ms/div. 
1 - heterostructure, charge-discharge through relative resistance 100 r; 
2 - heterostructure, charge-discharge through 10 r; 
3 - heterostructure charge-discharge through 1 r, failure of the charge accumulation mode; 4 - heterostructure charge-discharge through 0.1 r, failure of the charge accumulation mode; 5 - conventional capacitor, 100 r; 
6 - the form of applied external voltage impulse.

The data of figures 9, 10 and 11 prove that no electrochemical deposition of a new phase with permanent composition occurs in the case of "battery-like" behavior. Apart from samples (A) and (B) one more ASIC/IE heterostructure (sample C) was investigated. It exhibits the same features of behavior (but with worse characteristics) as the sample (A). Fig. 12 shows the "battery-like" behavior and failure of the charge accumulation mode in the sample (C).

Fig. 12. Charge-discharge oscillograms of the ASIC/smooth IE experimental heterostructure (sample C) at 430 K. Horizontal scale is 100 ms/div. 
1 - heterostructure, charge-discharge through relative resistance 100 r, discharge current $j \approx 0.03$ A/cm$^2$, "battery-like" behavior, $\rho_{C_{eq}} > 8000 \mu$F/cm$^2$; 
2 - heterostructure (10 r, $j \approx 0.2$ A/cm$^2$, failure of the charge accumulation mode, $\rho_{q} = 6 \cdot 10^{-3}$ C/cm$^2$); 
3 - conventional capacitor, charge-discharge through 100 r; 
4 - the form of applied external voltage impulse.
The similarity of behavior and properties of A, B and C heterostructures having the same ASIC/IE heterojunctions design but differing in chemical composition of ASIC and/or IE structures strongly suggest the universal character of “battery-like” behavior. The following mechanism of charge accumulation can be proposed: (1) accumulation of a threshold charge density $\rho_{Q_{\text{crit}}}^{\text{ASIC}}$ on the ASIC/IE interface; (2) electron transfer from the ASIC valence band to the anode in strong electric field (order of molecular field) and simultaneous escape of positively charged mobile ions to the cathode, to produce neutral complex point defects on the basis of holes and cation vacancies, and (3) distribution of the neutral defect zone with the defect concentration determined by an applied external voltage) into the depth of ASIC volume via self-organization. In the case of “battery-like” behavior defect concentrations in the ASIC subsurface layers can be detected by optical methods.

The experimental observation of supergiant capacity phenomenon on the investigated heterostructures with special interface design can be connected with formation of the ordered single-layer new phase containing alternating IE-cations and ASIC-anions at the interface. The great $\rho_Q$ value may be achieved by fractal surface geometry.

3. CONCLUSION

The discovery of giant and supergiant capacitor phenomena as well as “battery-like” behavior in the special designed ASIC/IE heterojunctions is a fact of a great practical interest. Is there new physics on horizon?

* Electronic address: despot@ipmt-hpm.ac.ru

[1] B.B. Owens. J. Power Sources 90, 2 (2000).
[2] A.L. Despotuli, A.V. Andreeva, B. Rambabu. “Nanoionics of Advanced Superionic Conductors”// in: Book of Abstracts "Patras Conference on Solid State Ionics -Transport Properties" September 14-18, 2004, P. 66.
[3] A.L. Despotuli, A.V. Andreeva, B. Rambabu. Nano- and microsystem engineering 2, 5 (2005).
[4] A.L. Despotuli, A.V. Andreeva, B. Rambabu. Ionics 11, 1 (2005).
[5] Ch. Emmenegger, Ph. Mauron, P. Sudan, P. Wenger, V. Hermann, R. Gallay, A. Zuttel. J. Power Sources 124, 321 (2003).
[6] S. Bredikhin, T. Hattory, M. Ishigame. Phys.Rev. B 50, 2444 (1994).
[7] S. Roundy, D. Steingart, L. Frechette, P.K. Wright, J. Rabaey “Power sources for wireless networks” // Proc 1st European Workshop on Wireless Sensor Networks (EWSN’04), Berlin, Germany, Jan. 19-21, 2004.
[8] T. Christen, M.W. Carlen. J. Power Sources 91, 210 (2000).
[9] J.B. Bates, N.J. Dudney, B. Neudecker, A. Ueda, C.D. Evans. Solid State Ionics 135, 33 (2000).
[10] A.L. Despotuli, A.V. Andreeva. Double-layer thin-film supercapacitors for nano-electro-mechanical systems (NEMS) // Proc. IARP International workshop "Micro Robots, Micro Machines, Micro Systems", Moscow, April 24-25. 2003. P. 129-141.
[11] A.L. Despotuli, A.V. Andreeva. Chemistry Preprint Archive 2003, # 6, 283 (2003).
[12] A.L. Despotuli, A.V. Andreeva. Chemistry Preprint Archive 2003, # 9, 4 (2003).
[13] A.L. Despotuli, A.V. Andreeva, Microsystem engineering 11, 2 (2003).
[14] A.L. Despotuli, A.V. Andreeva, Microsystem engineering 12, 2 (2003).
[15] A.L. Despotuli, V.I. Nikolaichic. Solid State Ionics 60, 275 (1993).
[16] F.A. Karamov. Superionic conductors. Heterostructures and elements of functional electronics on their base (Moscow, Science Press, 2002).