Compression-Based Optimizations for Out-of-Core GPU Stencil Computation

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Abstract

An out-of-core stencil computation code handles large data whose size is beyond the capacity of GPU memory. Whereas, such an code requires streaming data to and from the GPU frequently. As a result, data movement between the CPU and GPU usually limits the performance. In this work, compression-based optimizations are proposed. First, an on-the-fly compression technique is applied to an out-of-core stencil code, reducing the CPU-GPU memory copy. Secondly, a single working buffer technique is used to reduce GPU memory consumption. Experimental results show that the stencil code using the proposed techniques achieved 1.1\times speed and reduced GPU memory consumption by 33.0\% on an NVIDIA Tesla V100 GPU.

Keywords: On-the-fly compression, stencil computation, out-of-core, GPU
1 Introduction

Stencil computation is an important class of scientific application which pertains in a wide range of research and industry fields, such as geophysics simulations [1–3], computational electromagnetics [4], and image processing [5]. Stencil computation updates every element in given arrays (i.e., datasets) according to one or more fixed calculating patterns (i.e., stencils), which is an embarrassingly parallelizable task for graphics processing units (GPUs). A GPU has thousands of cores and its memory bandwidth is 5–10 times higher than that of a CPU, thus excelling at accelerating both compute- and memory-intensive scientific applications [6–8]. However, as a GPU has a limited capacity of device memory (tens of GBs), it fails to directly run a large stencil code whose data size exceeds the memory capacity.

A large entity of research on GPU-based out-of-core stencil computation has been performed to address this issue [3, 9–12]. For a large dataset whose data size exceeds the capacity of the device memory, out-of-core computation first decomposes the dataset into smaller blocks and then streams the blocks to and from the GPU to process. Nevertheless, the performance of this approach is often limited by data movement between the CPU and GPU because the interconnects fail to catch up with the development of the computation capability of GPUs as described in [6].

Existing techniques such as temporal blocking and region sharing to reuse the on-GPU data and to avoid redundant data transfer [3, 9, 12] were studied, yet new optimizations are in demand to further reduce data movement overhead.

On-the-fly compression based techniques are promising. Such techniques can be used to compress the data on the GPU before moving it to the CPU and decompress the data on the GPU before processing. Studies on the acceleration of GPU-based out-of-core stencil computation with on-the-fly compression are rare. According to a comprehensive review [13], studies on leveraging compression techniques in scientific applications mainly focused on scenarios such as post-analysis and failure recovery.

To fill the research gap, this article proposes compression-based optimization techniques for out-of-core stencil computation. The major contribution of this article is therefore summarized as follows:

- An on-the-fly compression technique is integrated into an out-of-core stencil code to reduce the amount of data movement between the CPU and GPU, shifting the performance bottleneck from data movement to GPU computation.
- A single working buffer technique is proposed, which significantly reduces GPU memory consumption.
- A detailed analysis is given to demonstrate the usefulness of our approach to optimize out-of-core GPU stencil computation.

The remainder of this article is organized as follows: Related work on accelerating stencil and similar scientific applications with compression techniques
are introduced in Section 2. Background of out-of-core stencil computation are briefly described in Section 3. Section 4 gives the basics of integrating an on-the-fly compression technique into out-of-core computation. The proposed memory-saving technique is described in Section 5. In Section 6, experimental results are presented and analyzed. Finally, Section 7 concludes the present work and suggests future research directions.

2 Related work

Tao et al. [14] and Calhoun et al. [15] used lossy compression techniques to compress checkpointing data to improve restart performance. Jin et al. [16] used GPU-based lossy compression for post-analysis for cosmological simulations. These studies are more relevant to a stand-alone procedure rather than an on-the-fly one.

Wu et al. [17] simulated large quantum circuits using lossy or/and lossless compression techniques adaptively, increasing the simulation size by 2–16 qubits. Their research is based on a CPU-based supercomputer.

Zhou et al. [18] extended MPI libraries to reduce communication time in a GPU cluster by compressing the messages transferred between nodes. The size of messages was up to 32 MB. On the other hand, our method compressed large datasets for stencil computation that were more than 10 GB to reduce the data transfer time between the CPU and GPU.

Sun et al. [19] proposed an accelerator platform that eliminates the data movement bottleneck between PCIe-attached FPGAs and their host servers via compression. Their approach mainly focuses on optimizing the ZFP compression algorithm [20] on a hardware (i.e. FPGA) level. On the other hand, our work does not change the compression algorithm itself, but focuses on how to efficiently use compression in the scenario of GPU acceleration.

3 Background

The background of out-of-core stencil computation is provided in this section. Above all, we explain the reason why out-of-core stencil computation can benefit from compression.

3.1 Out-of-core stencil computation

Stencil computation is an iterative data processing solution that updates array elements according to one or more fixed patterns called stencils. In a stencil, the value of the element to be updated is computed with the values of surrounding elements called halo (Fig. 1(a)).

Out-of-core approaches tackle with large data of stencil computation that is beyond the capacity of GPU memory. Out-of-core stencil computation decomposes the original data into smaller data chunks, each of which can fit in the
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Fig. 1 Example of out-of-core stencil computation. (a): Updating an element in a five-point stencil computation code for two time steps. (b) Transferring data chunks with halo regions.

GPU memory. Chunks are streamed to and from the GPU for processing. However, such an approach incurs frequent data movement between the CPU and GPU, which is prone to performance degradation.

Temporal blocking [12], is a widely used optimization to reduce data movement in hierarchical memory systems. In the scenario of out-of-core stencil computation, temporal blocking piggybacks halo regions with chunks according to the number of time steps we want to compute with chunks on the GPU (Fig. 1(b)). In doing so, we can reduce the time of CPU-GPU data movement.

A region sharing technique [3, 9, 21] can be leveraged to further reduce CPU-GPU data movement. That is, two contiguous chunks share a common...
Fig. 3  Hierarchical memory system of the testbed in the work that comprises an NVIDIA Tesla V100 GPU [22, 23] and an Intel Xeon Silver 4114 CPU. The PCIe 3.0 interconnect between the CPU main memory and GPU device memory limits the performance of the system in terms of data movement.

(i.e., overlapped) area (Fig. 2(a)), and a chunk moved to the GPU can therefore share such common data on the GPU to the next chunk. As a result, we can move the next chunk to the GPU without the redundant data (Fig. 2(b)).

3.2 Data movement bottleneck

Temporal blocking requires moving valid data with halo data to the GPU. The more time steps you want to compute using a data chunk on the GPU, the more halo data the chunk must piggyback. Throughout the hierarchical structure of CPU-GPU memory system (Fig. 3), the interconnect between the CPU memory and the GPU memory has a relatively small bandwidth, making the performance of an out-of-core GPU application sensitive to increased CPU-GPU data movement. Figure 4 shows that the CPU-GPU data movement limited the performance of a 25-point out-of-core GPU stencil code [3], even though the code was implemented the aforementioned techniques, which calls for techniques to further reduce the data movement.
4 Integrating on-the-fly compression

This section provides the basics of integrating on-the-fly compression into out-of-core stencil computation. We minimize the length of this section because you can refer to our previous work [25] for more details.

4.1 Separate compression

As mentioned in Section 3.1, contiguous chunks share an overlapped area on the GPU to avoid redundant data transfer. Therefore, we compress the overlapped area of a chunk separately from and the remnant of the chunk, in order to solve runtime data dependency.

4.2 Pipeline execution

As shown in Fig. 4, CUDA streams are used to overlap data movement with computation, to some extent hiding the overhead of data movement.

Our approach utilizes a powerful GPU-based compression library cuZFP [20], which excels at both execution time and information preservation with a customized compression rate. We modified the original project of cuZFP to conform to pipeline execution, overlapping CPU-GPU data movement with GPU kernels including decompression, computation, and compression.

5 Single working buffer technique

In a GPU stencil code without compression, a three-stage pipeline is most commonly used to overlap CPU-GPU data movement with GPU computation. Implementing such an approach with the CUDA language requires three CUDA streams and each stream needs a GPU buffer to store the data for GPU computation (Fig. 5(a)). In our previous work, we also use three CUDA streams, each of which requires a compressed buffer and a full-size working buffer. The size of a compressed buffer is determined by a user-specified compression rate. We use 32 bits to store a double floating-point value, making the compression rate 32/64=1/2 (i.e. half size). Compressed data is first moved from the CPU to the half-size buffers, and is then decompressed to the full-size buffer for computation (Fig. 5(b)). Such an approach is straightforward to implement but increases GPU memory consumption compared to a stencil code without compression.

To improve the efficiency of memory usage, we propose a single working buffer method. Observing that GPU kernels cannot overlap with each other for stencil computation with large datasets (Fig. 4), we determine that using three full-size working buffers is unnecessary. Therefore, we reduce the number of working buffers to one. Each of the three half-size buffers stores its own data assignment, and in turn uses the full-size working buffer to perform decompression, computation, and compression (Fig. 6). Nevertheless, although such
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Fig. 5 Architecture of an out-of-core stencil program (a) w/o compression or (b) w/ compression. Three CUDA streams are used to overlap data movement and GPU computation.

Fig. 6 An out-of-core stencil program w/ compression and proposed single working buffer method. Note that we still have three compressed (i.e. half-size) buffers yet only one full-size working buffer.

a method reduces the amount of GPU memory consumption, we must carefully orchestrate the three CUDA streams to avoid resource conflicts because now the streams share the same working buffer.
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Fig. 7 Securing correct execution order for proposed single working buffer method: (a) directed acyclic graph (DAG) showing dependencies among operations of the stencil program using compression and single working buffer and (b) scheduling operations to avoid resource conflicts.

Task graph based methods [26, 27] can be used to schedule the GPU kernels to prevent resource conflicts, considering inter-stream dependencies. Figure 7(a) illustrates the directed acyclic graph (DAG) of an out-of-core GPU stencil computation code using compression and the proposed single working buffer method. An arrowed line across streams denotes an inter-stream dependency that a stream waits for its cyclically prior stream to take control of the working buffer to execute GPU kernels (decompression, computation, and compression).

We can schedule the operations by applying topological sorting [28] to the DAG (Fig. 7(b)). CUDA events [29] are used to realize fine-grained synchronizations between streams. At the beginning of an arrowed dotted line, we record an event with the stream the line starts from, whereas at the end of the arrowed dotted line, we wait for the event with the stream the arrow is pointed to. Algorithm 1 shows the proposed method of scheduling GPU kernels without resource conflicts.

6 Experimental results

In this section, we provide experimental results to demonstrate the usefulness of the proposed methods in terms of reducing execution time and GPU memory consumption.
Algorithm 1 Conflict-free scheduling.

Require: (1) $chk[0:n]$, compressed data chunks on the CPU, (2) $strm[0:3]$, CUDA streams, (3) $evt[0:3]$, CUDA events, (4) $hf.buf[0:3]$, half-size buffers on the GPU to manage compressed chunk, (5) $fl.buf$, full-size working buffer on the GPU to perform kernels

Ensure: Updated $chk[0:n]$

\[
\begin{align*}
si & \leftarrow 0 \\
prev_s & \leftarrow -1 \quad \triangleright \text{Index of previous stream} \\
prev_c & \leftarrow -1 \quad \triangleright \text{Index of previous chunk} \\
\text{for } i = 0 \text{ to } n - 1 \text{ do} \\
\quad \text{if } prev.s \neq -1 \text{ then} \\
\quad \quad \text{Compress data in } fl.buf \text{ to } hf.buf[prev.s] \text{ using } strm[prev.s] \\
\quad \quad \text{Record } evt[prev.s] \text{ using } strm[prev.s] \\
\quad \quad \text{Transfer data in } hf.buf[prev.s] \text{ to } chks[prev.c] \text{ using } strm[prev.s] \\
\quad \quad prev.s & \leftarrow -1 \\
\quad \quad prev.c & \leftarrow -1 \\
\quad \text{end if} \\
\quad \text{Transfer data in } chk[i] \text{ to } hf.buf[si] \text{ using } strm[si] \\
\quad prev & \leftarrow (si - 1) < 0 \, ? \, 2 : (si - 1) \\
\quad \text{Wait } evt[prev] \text{ using } strm[si] \\
\quad \text{Decompress data in } hf.buf[si] \text{ to } fl.buf \text{ using } strm[si] \\
\quad \text{Compute on data in } fl.buf \text{ using } strm[si] \\
\quad prev.s & \leftarrow si \\
\quad prev.c & \leftarrow i \\
\text{end for}
\end{align*}
\]

Table 1 Target stencil code.

| No. of datasets | Data type | Dim. info. | Entire data size |
|-----------------|-----------|------------|------------------|
| 4               | Double    | (1152+2×HALO)³, HALO=4 | 46 GB |

Table 2 Testbed for experiments.

|                  |                  |
|------------------|------------------|
| GPU              | NVIDIA Tesla V100-PCIe |
| Device memory    | 32 GB            |
| CPU              | Xeon Silver 4110 |
| Host memory      | 500 GB           |
| OS               | Ubuntu 18.04     |
| CUDA             | 10.1             |
| cuZFP            | 0.5.5            |

The stencil code used in the experiments is an acoustic wave propagation program [2, 3]. A 25-point stencil computation is applied to a 3-d volume that sums up to 46 GB. Such excess data was decomposed into eight chunks with 12 halo regions in conformity with 12 temporal blocking time steps. Table 1
6.1 Evaluation of performance improvement

In this section, we compare the execution time of the stencil code without compression with that of the stencil code with compression and the proposed single working buffer method. Both codes were executed for 36 time steps.

Figure 8 shows that utilizing on-the-fly compression reduces the overall execution time of the out-of-core stencil code. The code with proposed compression method achieved a speedup of $1.1 \times$, compared to the code without compression. Such a speedup can be further increased because we did not optimize the GPU kernels of the code. Actually, the compression technique shifts the bottleneck for the stencil code from CPU-GPU data movement to GPU computation (Fig. 9), which is a favorable finding because optimizing GPU kernels has been much more sufficiently studied [30, 31] than optimizing CPU-GPU data movement does.

Fig. 8 Comparing execution time of the code without compression with that of the code with compression and single working buffer method.

Fig. 9 A part of profiling output of stencil code with proposed compression method. Note that GPU kernel time is longer than CPU-GPU data movement time, becoming the performance bottleneck.

Note that the experimental results focus on the reduced execution time and GPU memory usage. The section excludes analyzing accuracy loss caused by compression, because such an analysis was given in our previous work [25], showing that the accuracy loss was tolerable for our real-world stencil code after the code ran for more than 4,000 time steps.
6.2 Evaluation of GPU memory usage improvement

Figure 10 illustrates that the code with compression and single working buffer method significantly reduces GPU memory consumption by 33.0%, compared to the code without compression. We can do a simple math to verify this improvement. First, the four datasets of the stencil code are a read-only dataset, two read-write datasets, and a write-only dataset. Although no data is moved to and from the write-only dataset, we still need to prepare a working buffer for it on the GPU for computation. Now assume that the size of a working buffer is 1. For the code without compression, the GPU memory consumption is $1 \times 4 \times 3 = 12$, where the number 3 means three CUDA streams. On the other hand, for the code with compression and single working buffer method, three half-size buffers and a full-size working buffer are used, and no half-size buffer is needed for the write-only dataset. Therefore, the memory consumption is $0.5 \times 3 \times 3 + 1 \times 4 = 7.5$. The ratio of the reduction is $(12 - 7.5)/12 = 37.5\%$. The discrepancy between the theoretical and practical results is because the procedure of on-the-fly compression consumes some additional memory at runtime.

7 Conclusion

In this article, we proposed compression-based optimizations for out-of-core GPU stencil computation. On-the-fly compression was integrated into the stencil code, which improved the overall execution time by reducing memory copy (i.e., data movement) between the CPU and GPU. The performance bottleneck was thus shifted CPU-GPU memory copy to GPU computation. Such a shift is promising because further performance improvement can be achieved if GPU computation is optimized, which is not done in this work but many mature techniques are available. Furthermore, the proposed single working buffer method can significantly reduce GPU memory consumption, which improves the efficiency of resource usage. Experimental result shows that the stencil code with proposed optimizations achieved a $1.1 \times$ speedup and saved GPU memory by 33.0%, compared to the code without compression.
Future work includes (1) comparing various compression libraries and (2) fully releasing the potential of on-the-fly compression by optimizing GPU computation.

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