Formation of high-quality SiC(0001)/SiO₂ structures by excluding oxidation process with H₂ etching before SiO₂ deposition and high-temperature N₂ annealing

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Received October 14, 2020; revised October 26, 2020; accepted November 1, 2020; published online November 12, 2020

We formed SiC/SiO₂ structures by various procedures that excluded an oxidation process. We found that a SiC/SiO₂ interface with a low interface state density near the conduction band edge of SiC (D₁ – 4 × 10¹⁰ cm⁻² eV⁻¹ at E₁ – 0.2 eV) is obtained for a fabrication process consisting of H₂ etching of the SiC surface, SiO₂ deposition, and high-temperature N₂ annealing. D₁ is rather high without H₂ etching, indicating that etching before SiO₂ deposition plays a significant role in reducing D₁. The key to obtaining low D₁ may be the removal of oxidation-induced defects near the SiC surface.

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have attracted considerable attention as promising devices for high-voltage and fast-switching power applications.¹² The performance of SiC MOSFETs is constantly being improved.³–⁸ However, the on-resistance of medium voltage class (~1 kV) SiC MOSFETs is still dominated by a high channel resistance due to the high density of interface states (~10¹³ cm⁻² eV⁻¹) in SiC/SiO₂ systems.⁹–¹² To reduce the channel resistance, most commercial SiC MOSFETs have relatively short channels (<1 μm). However, further shortening of the channel length is problematic because it will induce short-channel effects, such as decreasing the threshold voltage, non-saturation of the drain current, and subthreshold slope degradation.¹³,¹⁴ Therefore, it is important to reduce the interface state density (D₁) to improve the performance of SiC MOSFETs.

Post-oxidation annealing of nitric oxide (NO) is commonly used as a passivation method for interface states in SiC/SiO₂ structures.¹⁵–¹⁹ NO annealing can improve the channel mobility from 3–5 to 30–40 cm² V⁻¹ s⁻¹. However, further improvements are necessary to take full advantage of the potential of SiC. Various studies have been conducted to achieve high channel mobility.²⁰–²⁵ Several passivation methods have achieved high channel mobility (~70–100 cm² V⁻¹ s⁻¹) (e.g. sodium enhanced oxidation²⁶,²⁷ and annealing in phosphonyl chloride (POCl₃) ambient²⁸,²⁹). However, these methods are not suited for industrial applications because of the threshold voltage instability caused by ion drift³⁰ or carrier trapping.³¹

The origin of high D₁ is unclear at present, though carbon defects are a possible explanation.³,⁹,³²–³⁵ Recently, first-principles calculations have suggested that dicarbon antisites are very stable under oxygen-rich conditions, and can create defect levels near the conduction band edge.³⁴ Another possible candidate is conduction band fluctuation.³⁵–³⁷ Research has indicated that high D₁ may arise from crystalline disorder of SiC surfaces caused by SiC oxidation. Thus, one solution may be elimination of oxidation from the SiO₂ formation process as much as possible. Recently, we reported that a significantly lower D₁ can be obtained by creating a SiC/SiO₂ structure via Si deposition.³⁸ In this process, a gate oxide was created by the following process. First, a thin Si film was deposited on a SiC surface after H₂ etching. Then, SiO₂ was formed by oxidation of Si at a low temperature (750 °C). Finally, high-temperature N₂ annealing was conducted. The key to obtaining low D₁ in this process was suppressing SiC oxidation.

In this study, we propose another approach to exclude oxidation process for SiO₂ formation using chemical vapor deposition (CVD). In addition to suppressing SiC oxidation, we have found that surface etching of SiC by H₂ plays a vital role in reducing D₁ near the conduction band edge (E₁c) of SiC. We discuss the possible mechanism of the observed reduction in D₁ based on our results. We believe the key to obtaining low D₁ is removing oxidation-induced defects near the SiC surface.

MOS capacitors were formed on n-type 4H-SiC (0001) epilayers (donor density: 1 × 10¹⁵ cm⁻³). The processing conditions for gate oxide formation are indicated in Fig. 1. After RCA cleaning, some of the samples were etched in H₂ ambient at 1350 °C and 0.1 MPa for 15 min, giving an etched thickness of about 5 nm. After H₂ etching, sacrificial oxidation was performed at 1300 °C for some samples (the oxide thickness was about 18 nm and was removed by buffered HF). Some samples were etched in H₂ ambient again. The gate oxides were deposited by plasma-enhanced CVD at 400 °C, resulting in an oxide thickness of 20–30 nm. Then, high-temperature N₂ annealing³⁹,⁴⁰ at 1400 °C for 45 min or Ar annealing at 1400 °C for 10 min was performed. Finally, circular Al electrodes were deposited (diameter: 300–500 μm). Designations for the prepared samples are indicated in Fig. 1.

For comparison, MOS capacitors with SiO₂ (thickness: 30 nm) formed by dry oxidation were prepared. NO annealing was performed at 1250 °C for 70 min. The sample not subject to annealing is designated “As-Ox.”

Figure 2(a) depicts the quasi-static and 1 MHz capacitance–voltage (C–V) characteristics of the MOS capacitors at 300 K. High-frequency and quasi-static C–V characteristics were simultaneously measured using KEITHLEY 82 C–V System. Voltage sweeping was conducted from the depletion side to the accumulation side. In the figure, the ideal C–V curve with an oxide thickness of 25 nm and a donor density of 1 × 10¹⁵ cm⁻³ is also indicated for comparison. A large frequency dispersion is observed for the As-Ox sample. The dispersion is well reduced in the CVD-N₂ sample and further suppression is achieved by performing H₂ etching prior to...
SiO₂ deposition (H₂-CVD-N₂ sample). The densities of the effective fixed charge estimated from the flat-band voltage shifts are $6.7 \times 10^{11}$ cm$^{-2}$ (negative), $7.5 \times 10^{11}$ cm$^{-2}$ (positive), and $1.7 \times 10^{12}$ cm$^{-2}$ (positive) for the As-Ox sample, the CVD-N₂ sample, and the H₂-CVD-N₂ sample, respectively.

Figure 2(b) illustrates the energy distributions of $D_{it}$ estimated by a high (1 MHz)–low method. A substantial reduction in $D_{it}$ is achieved when H₂ etching was performed before SiO₂ deposition.

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Fig. 1. (Color online) Processes for fabrication of gate oxide investigated in this study. The designations for the fabricated samples are also indicated.

Fig. 2. (Color online) (a) Quasi-static and 1 MHz $C-V$ characteristics of the prepared MOS capacitors. The ideal $C-V$ curve is also indicated for comparison. (b) Energy distribution of $D_{it}$ extracted by a high (1 MHz)–low method. A substantial reduction in $D_{it}$ is achieved when H₂ etching was performed before SiO₂ deposition.

Fig. 3. (Color online) Energy distribution of $D_{it}$ extracted by a high (1 MHz)–low method for the prepared MOS capacitors. (a) Comparison with the case with sacrificial oxidation performed after the H₂ etching. The SiO₂ formed by oxidation was removed by BHF before the CVD. (b) Effect of Ar annealing (+N₂/H₂ FGA) instead of N₂ annealing after the SiO₂ deposition.
is achieved by performing H₂ etching prior to SiO₂ deposition (about 4 × 10¹⁰ cm⁻² eV⁻¹ at E<sub>c</sub> = −0.2 eV). The D<sub>s</sub> value is about one order-of-magnitude lower than the reported D<sub>s</sub> for an N₂-annealed sample with a pre-annealing process (4 × 10¹¹ cm⁻² eV⁻¹ at E<sub>c</sub> = −0.2 eV) and for the NO sample. These results indicate that removal of surface defects is essential for a substantial reduction in D<sub>s</sub>.

To clarify that SiC oxidation increases D<sub>s</sub>, we performed sacrificial oxidation after the H₂ etching. Figure 3(a) shows the effect of sacrificial oxidation on D<sub>s</sub>. The figure shows that D<sub>s</sub> is not effectively reduced when sacrificial oxidation was performed after H₂ etching (and prior to SiO₂ deposition: H₂-Ox-CVD-N₂), though D<sub>s</sub> energy distribution is reduced when H₂ etching was performed again after sacrificial oxidation (H₂-Ox-H₂-CVD-N₂). We also confirmed that the D<sub>s</sub> energy distribution was not reduced when SiO₂ was formed by oxidation after H₂ etching (H₂-Ox-N₂). The following summarizes the above experimental results: (1) A substantial reduction of D<sub>s</sub> is achieved by H₂ etching prior to SiO₂ CVD. (2) SiC oxidation results in higher D<sub>s</sub> even after performing H₂ etching. (3) Even after SiC oxidation, D<sub>s</sub> decreases when H₂ gas etching is performed again. Based on the above results, we consider that oxidation creates a high density of defects on the SiC surface and these surface defects are the major origin of a high D<sub>s</sub> at the SiC/SiO₂ interface. The removal of such surface defects might decrease D<sub>s</sub>, and these defects can be removed by H₂ etching of SiC by about several (∼5) nm. These defects are difficult to directly characterize by standard surface analyses, such as by X-ray photoelectron spectroscopy measurements, because the defects might be formed within only a few sub nm from the SiC surface.

Next, high-temperature Ar annealing was performed instead of N₂ annealing to investigate whether N₂ annealing is necessary for reducing the interface states. Figure 3(b) depicts a comparison of the energy distribution of D<sub>s</sub> for N₂-annealed and Ar-annealed MOS capacitors. For Ar annealing, D<sub>s</sub> is relatively high (1 × 10¹² cm⁻² eV⁻¹ at E<sub>c</sub> = −0.2 eV). We also performed forming gas annealing (H₂/N₂: 1/9) at 800 °C for 2 min after Ar annealing. However, this resulted in only a slightly lower D<sub>s</sub> than when only Ar annealing was performed.

To evaluate the nitrogen atom profiles near the interface, secondary ion mass spectrometry measurements were performed after depositing SiO₂ and annealing in N₂ at high temperature. Figure 4(a) shows the depth profiles for the nitrogen atom density in samples with and without H₂ etching (CVD-N₂ and H₂-CVD-N₂). The depth profiles for N atoms are almost identical in CVD-N₂ and H₂-CVD-N₂, as expected. Figure 4(b) shows the results for NO and N₂ samples for comparison. Inside the oxide material, the nitrogen atom density is about 2–3 times higher in the samples with a deposited oxide than in the samples with a thermal oxide. However, at the interface, the incorporated nitrogen atom density is comparable among all the samples (7–10 × 10¹⁰ cm⁻³). These results suggest that the depth profile for N atoms is independent of H₂ gas etching. Hence, removing C-related defects or a layer with disordered crystallinity near the SiC surface induced by the thermal oxidation of SiC may lower D<sub>s</sub>. Here, we briefly summarize the key points in common between this study and our previous work:Ω for obtaining low D<sub>s</sub>. There are three common processes: (1) H₂ etching of the SiC surface, (2) SiO₂ formation without oxidation, and (3) high-temperature N₂ annealing. We conclude that all of these processes are necessary for a substantial decrease in D<sub>s</sub>.

Figure 5(a) shows bi-directional 1 MHz C–V curves measured for the H₂-CVD-N₂ sample (EOT ∼ 20 nm) at 448 K. Before voltage sweeping, a bias voltage of 10 (5 MV cm⁻¹) or −10 V was applied for 600 s. Voltage sweeping was immediately conducted in the reverse direction from the initial voltage after the bias stress. The bi-directional C–V curves show a negligibly small hysteresis, meaning that the density of mobile ions and electron traps inside the oxide is negligibly small. Note that the density of holes at the MOS interface without light illumination is extremely low due to the wide bandgap of SiC. Hence, only the electron trapping is evaluated in this measurement.

Figure 5(b) depicts the current–voltage (I–V) characteristics of the prepared SiC MOS capacitors under a positive-bias condition (accumulation state). For comparison, the I–V characteristics of the As-Ox, Ox-NO, and Ox-N₂ samples are also indicated. Above 6–7 MV cm⁻¹, a Fowler–Nordheim (F–N) tunneling current is observed. The breakdown electric fields of the oxides were about 11.5 MV cm⁻¹ for the As-Ox and Ox-NO samples, 10 MV cm⁻¹ for the Ox-N₂ sample, and 10.5 MV cm⁻¹ for the H₂-CVD-N₂ sample. The breakdown electric field for the H₂-CVD-N₂ samples is similar to those of other samples. In conclusion, we demonstrated that H₂ etching prior to SiO₂ deposition is effective in reducing D<sub>s</sub> at the SiC/SiO₂ interface.
interface while suppressing SiC oxidation. A significant reduction of $D_E (4 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1})$ at $E_c = -0.2 \text{eV}$ was achieved for the procedure of H$_2$ etching of the SiC surface, SiO$_2$ deposition, and high-temperature N$_2$ annealing. C defects induced by the thermal oxidation of SiC are strong candidates for interface states in SiC/SiO$_2$ systems, and such defects are removed by H$_2$ etching. Surface etching of SiC before SiO$_2$ deposition is likely to be the key for obtaining a high quality SiC/SiO$_2$ structure.

Acknowledgments This work was supported in part by the Open Innovation Platform with Enterprises, Research Institute and Academia ( OPERA) Program from the Japan Science and Technology Agency (JST), the 2019 Innovation Platform with Enterprises, Research Institute and Academia (OPERA) Program from the Japan Science and Technology Agency (JST), the 2019 Block-Gift Program of the II-VI Foundation, and the Japan Society for the Promotion of Science (JSPS) KAKENHI Grant Number 19J23422.

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