Centralized Recursive Optimal Scheduling of Parallel Buck Regulated Battery Modules

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Abstract—This paper presents a centralized recursive optimal scheduling method for a battery system that consists of parallel connected battery modules with different open circuit voltages and battery impedance characteristics. Examples of such a battery system can be found in second-life, exchangeable or repurposed battery systems in which batteries with different charge or age characteristics are combined to create a larger storage capacity. The proposed method in this paper takes advantage of the availability of buck regulators in the battery management system (BMS) to compute the optimal voltage adjustment of the individual modules to minimize the effect of stray currents between the parallel connected battery modules. Our proposed method recursively computes the optimal current scheduling that balances (equals) each module current and maximize total bus current without violating any of the battery modules operating constraints. Recursive implementation guarantees robust operation as the battery modules operating parameters change as the battery pack (dis)charges or ages. In order to demonstrate the capability of this method in real battery system, an experimental setup of 3 parallel placed battery modules is built. The experimental results validate the feasibility and show the advantages of this current scheduling method in a real battery application, despite the fact that each module may have different impedance, open circuit voltage and charge parameters.

I. INTRODUCTION

Electric vehicles (EVs) are widely regarded as a promising environmental-friendly solution for future automotive industry, due to technological developments and an increased focus on renewable energy [1], [2], [3]. Most EVs use lithium-ion batteries (LIBs) to storage energy and supply power to the electric grid including communication and control systems, because LIBs have higher specific power and energy density, longer life span and lower self-discharge rate than most other practical batteries [4], [5].

Typically, a series connection of LIBs are used to create a battery module that achieves a desired open circuit or battery terminal voltage, while a parallel connection of battery modules is used to increase the total energy storage capacity of the battery pack. Parallel connected battery modules also increase power capacity to both fulfill an acceptable driving range and maintain high performance of EVs [6], [7], [8], [9]. Such configuration also shows significant benefits in second-life battery applications, such as demand charge management, renewable energy integration and regulation energy management in EVs [10], [11].

Unfortunately, variability in the production process of LIBs can not ensure identical battery modules and moreover, parallel placed battery modules exposed to the same (dis)charge cycles might age differently. Both effects cause discrepancies in internal resistance (impedance), temperature gradients, and operation conditions, such as power storage/delivery demand and environmental conditions. These discrepancies may limits the ability to extract or store the full electrical energy capacity in the battery system [12], [13], [14], [15]. Therefore, it is essential to build a battery management system (BMS) for a high power battery pack with parallel placed battery modules, so as to accurately estimate the state of charge (SOC) and state of health (SOH) of the modules to protect the battery from operating outside its Safe Operating Area (SOA) [16], [17], [18], [19], [20].

Fig. 1. Exchangeable battery module with a series connection of LIBs in a suitcase size format. Multiple of these battery modules are connected in parallel to increase power and energy storage capabilities.

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A high power battery pack with parallel connected battery modules that allow exchangeable modules can be viable alternative to increase power storage capacity and operation efficiency in a flexible way [21], [22]. In this paper we consider the use of separate and exchangeable battery modules that consists of a series connection of LIBs in a suitcase format, as shown in Fig. [1] Several LIBs are connected in series to achieve a large open circuit voltage, whereas a buck regulator is included in the battery module to control the battery module terminal voltage. The buck regulator uses
a digital Pulse Width Modulation (PWM) signal to several MOSFETs with an RLC filter (an electrical circuit consisting of a resistor (R), an inductor (L), and a capacitor (C)) to effectively reduce the full scale OCV. Subsequently, multiple modules can be placed in parallel on a single DC connection bus to create the full battery pack/system with a desired power and energy storage specification.

With such configuration, the efficiency and flexibility of this particular battery system is significantly improved, because partly empty or failing modules of the battery pack can be exchanged for fast charging and fault correction capabilities. As such, this configuration is applicable to second-life battery applications and/or EVs with partly exchangeable batteries. However, there are some challenges and bottlenecks with this configuration: each individual battery module may have different SOCs, instantaneous and nominal capacity, and internal impedances. Therefore, the terminal voltage of each parallel placed battery module must be controlled, and denoted by ‘scheduling’ in this paper, when charging and discharging battery modules.

The scheduling problem for parallel placed battery modules is solved in this paper by computing the optimal voltage adjustment of the individual modules to minimize the effect of stray currents between the parallel connected battery modules. The scheduling can compute various charging/discharging solutions and we consider a solution where the module currents are closely matched. The actual implementation of voltage regulation is achieved via the digital PWM signal used in the buck regulator included in the battery module. The scheduling solution proposed in this paper comprises the PWM in % of full scale for each module, without the explicit knowledge of the electrical module parameters of open circuit voltage and impedance of each module and the impedance/load connected to the battery pack. A recursive formulation of the scheduling solution allows estimation of electrical module parameters and adaptation to time varying load conditions on the battery pack. Finally, experimental results are included in this paper to validate the feasibility and performance of the proposed current scheduling control technique in different scenarios of a real battery system.

II. PARALLEL BUCK REGULATED BATTERY MODULES

A. Introduction and Assumptions

For scheduling of parallel placed battery modules, we assume that each module is characterized by an modulated ideal voltage supply in series with an impedance. For each module we make the following assumptions:

- The ideal voltage supply is given by \( V_k = \alpha_k V_{k, OCV} \), where \( V_{k, OCV} \) is the open circuit voltage (OCV) or terminal voltage of the battery module in case of no load and where voltage modulation can be only down via \( 0 < \alpha_k < 1 \).
- The internal impedance of a module is given by \( Z_k \) and is slowly time varying.

The slowly time varying nature of the model impedance \( Z_k \) is in comparison to the time varying nature of the external load impedance \( Z_l \) connected to the battery pack, as shown in Fig. 2. Following the electrical diagram of Fig. 2, application of Kirchhoff’s current and voltage law now leads to the following results for parallel placed modules characterized by an modulated ideal voltage supply \( V_k \) in series with an impedance \( Z_k \):

- The current \( I_k \) of each module ensures that the bus current \( I_{bus} = \sum_{k=1}^{n} I_k \) (1) due to Kirchhoff’s current law.
- The bus voltage \( V_{bus} \) satisfies \( V_{bus} = V_k - Z_k I_k \) (2) for each module \( k \) due to Kirchhoff’s voltage law.

B. Bus voltage as a function of module voltages

The above results can be combined to compute the bus voltage \( V_{bus} \) or bus current \( I_{bus} \), when a load \( Z_l \) is applied to battery pack that consists of a set of parallel placed modules. For a given set of values for the modulated voltages \( V_k \), \( k = 1, 2, \ldots, n \), with the individual module currents \( I_k \) given by

\[
I_k = \frac{V_k - V_{bus}}{Z_k}
\]

we have

\[
V_{bus} = Z_l I_{bus} = Z_l \sum_{k=1}^{n} I_k = Z_l \sum_{k=1}^{n} \frac{V_k - V_{bus}}{Z_k}
\]

From this last expression we can solve \( V_{bus} \) via

\[
V_{bus} = Z_l \sum_{k=1}^{n} \frac{V_k}{Z_k} - Z_l V_{bus} \sum_{k=1}^{n} \frac{1}{Z_k}
\]

making

\[
V_{bus} = \frac{\sum_{k=1}^{n} \frac{V_k}{Z_k}}{1 + \sum_{k=1}^{n} \frac{1}{Z_k}}
\]
Although this expressions may look complicated at first, it is important to recognize that the bus voltage $V_{bus}$ is determined by the linear combination

$$V_{bus} = \frac{1}{Z_f} g_1 V_1 + \frac{1}{Z_f} g_2 V_2 + \cdots + \frac{1}{Z_f} g_n V_n$$

where

$$g_j = \frac{Z_j}{Z_f + \sum_{k=1}^{n} \frac{1}{Z_k}}$$

for $j = 1, 2, \ldots, n$.

in which the "gain factors" $g_k$, $k = 1, 2, \ldots, n$ are given by a familiar parallel connection formula of impedances $Z_k$ and $Z_f$.

C. Module currents as a function of module voltages

With knowledge of $V_{bus}$, clearly also $I_{bus} = V_{bus}/Z_f$ can be computed. It is tempting to write $I_{bus}$ also as a similar linear combination by using (4) to obtain

$$I_{bus} = \frac{V_{bus}}{Z_f} = \frac{g_1}{Z_f} V_1 + \frac{g_2}{Z_f} V_2 + \cdots + \frac{g_n}{Z_f} V_n$$

and conclude based on (1) that the individual module currents are given by $I_k = \frac{g_k}{Z_f} V_k$, but that is incorrect. The individual module currents $I_k$ are typically a linear combination of all the modulated module voltages $V_k$, for which an expression is derived here.

With the individual module currents $I_k$ given in (3) and $V_{bus}$ given in (2), we can then obtain

$$I_k = \frac{1}{Z_k} \left( \frac{V_k}{Z_f} + \sum_{m=1}^{n} \frac{V_m}{Z_k} - \sum_{m=1}^{n} \frac{V_m}{Z_m} \right)$$

where the summation index has been changed to $m$ to avoid confusion with the specific module current $I_k$ indexed with $k$. The expression for $I_k$ can be simplified to the insightful expression

$$I_k = d_{k,1} V_1 + d_{k,2} V_2 + \cdots + d_{k,n} V_n,$$

where

$$d_{k,j} = \begin{cases} \frac{1}{Z_k} - \frac{1}{Z_f} & \text{for } j \neq k \\ \frac{1}{Z_k} + \sum_{m=1}^{n} \frac{1}{Z_m} & \text{for } j = k \end{cases}$$

with $d_{k,j}$ given in (5), and will be useful for the explicit computation of module currents $I_k$ as a function of the module voltages $V_k$ and visa versa.

It can be observed from the definition of the matrix $D = [d_{k,j}]$ that $D$ is symmetric. With all resistive values positive, it can also be shown that $D$ is also positive definite, making $D$ non-singular. With $D$ invertible, we can also compute module voltages $V_k$ as a function of desired module currents $I_k$ for the parallel placed battery modules.

III. CENTRALIZED RECURSIVE OPTIMAL CURRENT SCHEDULING

A. Relative scaling of module currents

Given the knowledge on the internal impedances $Z_k$, $k = 1, 2, \ldots, n$ and a fixed (but unknown) load impedance $Z_l$, the idea of module scheduling is formulated in this paper as the following problem. Compute the buck regulated module voltage $V_k \leq OCV$, such that module currents $I = [I_1, I_2, \ldots, I_n]^T$ are scaled to satisfy

$$I = \beta \begin{bmatrix} \beta_1 \\ \beta_2 \\ \vdots \\ \beta_n \end{bmatrix}, \quad 0 \leq \beta_k \leq 1, \quad k = 1, 2, \ldots, n \tag{7}$$

in which $\beta$ is used for absolute scaling, whereas $0 \leq \beta_k \leq 1$ specifies the relative scaling of the module current $I_k$. The value $\beta$ satisfies $\beta > 0$ for battery module discharging, whereas $\beta < 0$ for battery charging. Ideally, module scheduling should be done despite the lack of knowledge on the internal module impedance $Z_k$ and the externally applied load impedance $Z_l$. A recursive solution will be formulated to accomplish this later in the paper.

The motivation for the relative scaling $\beta_k$ of module currents $I$ according to (7) is to discharge/charge current $I_k$ out/in of a module $k$ based on the individual SOC of each battery module. For example, if the SOC of module $k$ is denoted by $0 \% < SOC_k \leq 100\%$, an appropriate relative scaling $\beta_k$ of a module current $k$ could be defined as

$$\beta_k = \frac{SOC_k}{\max_{k=1,2,\ldots,n} SOC_k} \leq 1$$

to ensure that battery modules with a smaller SOC will discharge less current compared to battery modules with a larger SOC. Similarly, for charging we may want

$$\beta_k = \frac{\min_{k=1,2,\ldots,n} SOC_k}{SOC_k} \leq 1$$

to satisfy that battery modules with a smaller SOC will charge faster with a larger current compared to battery modules with a larger SOC. If all modules have the same storage capacity with the same relative SOC and are required to follow the same (dis)charging profile, the relative scaling $\beta_k$ of module currents $I$ according to (7) can be required to satisfy $\beta_k = 1$, $k = 1, 2, \ldots, n$ causing

$$I_1 = I_2 = \cdots = I_n$$

will be denoted by equal SOC balancing in this paper.
B. Module scheduling via Linear Programming

In case of full information on the external load impedance \( Z_l \) and the internal impedance \( Z_k \), the optimal modulated module voltages \( V_k \) can be computed directly. With the definition of the (invertible) impedance matrix \( D \) in (6), we can actually compute the set of internal module voltages \( V = [V_1 V_2 \cdots V_n]^T \) directly from a desired set of module currents \( I = [I_1 I_2 \cdots I_n]^T \). Using the vector notation
\[
V = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}, \quad V_{\text{OCV}} = \begin{bmatrix} V_{\text{OCV}}^1 \\ V_{\text{OCV}}^2 \\ \vdots \\ V_{\text{OCV}}^n \end{bmatrix}
\]
and the module currents in the vector format \( I \) of (7), the problem of module scheduling requires the computation of the maximum value of the current scaling \( \beta > 0 \) such that \( V \leq V_{\text{OCV}} \).

With the (invertible) impedance matrix \( D \) in (6), the problem of module scheduling can be written as a linear programming (LP) problem that can compute a globally optimal value of the current scaling \( \beta \). By recognizing that
\[
V = D^{-1} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}^T \beta
\]
and the optimization for \( \beta > 0 \) (for discharging) of the module current can be written as
\[
\max_{\beta \geq 0} \beta \\
\text{s.t.} \quad D^{-1} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}^T \beta \leq V_{\text{OCV}}
\]
equivalent to the LP problem
\[
\beta_{\text{opt}} = \min_{\beta} f^T \beta, \quad \text{s.t.} \quad A \beta \leq b,
\]
with
\[
A = D^{-1} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}, \quad f^T = -1, \quad \text{and} \quad b = V_{\text{OCV}}.
\]
The LP problem in (9) will compute the optimal value of \( \beta_{\text{opt}} \). Once \( \beta_{\text{opt}} \) is known, the (optimal) module currents are given by
\[
I_{\text{opt}} = \beta_{\text{opt}} \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}
\]
and the (optimal) module voltages are readily computed via
\[
V_{\text{opt}} = \beta_{\text{opt}} D \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}
\]
(10)
based on (6).

C. Centralized recursive module scheduling

The LP solution in (9) requires knowledge of the impedance matrix \( D \) in (6) that is fully characterized by the internal module impedances \( Z_k \) and the external load impedance \( Z_l \). Once the impedance matrix \( D \) is known, the linear optimization problem in (9) can be solved to compute the optimal value \( \beta_{\text{opt}} \) of the (equal) balancing module currents, given the constraints on the OCV’s \( V_{\text{OCV}} \) for each module.

Although the internal module impedances \( Z_k \) may be monitored by the battery management system (BMS), the external load \( Z_l \) may not be known. In fact, the external load \( Z_l \) may be time-varying fairly fast due to varying power demands, while internal module impedances \( Z_k, k = 1, 2, \ldots, n \) typically only vary slowly over time. Clearly, module scheduling must be done without explicit knowledge of the external load \( Z_l \). In recursive module scheduling we will update the impedance matrix \( D \) recursively to allow for the computation of the optimal modulated module voltages \( V_k \).

The external load \( Z_l \) can be estimated by monitoring the bus voltage \( V_{\text{bus}} \) and the bus current \( I_{\text{bus}} \). Using Ohm’s law, we may estimate \( Z_l = \frac{V_{\text{bus}}}{I_{\text{bus}}} \) so that the value of \( Z_l \) in the impedance matrix \( D \) can be replaced by the ratio of \( V_{\text{bus}} \) and \( I_{\text{bus}} \).

Since the optimal values of the internal module voltages \( V \) and the resulting bus voltage \( V_{\text{bus}} \) again depend on the impedance matrix \( D \), a straightforward recursive procedure can be used to recursively update \( D \) and compute the optimal modulated module voltages \( V \) for (scaled) balancing module currents. Starting from an initial choice for the internal module voltages \( V = [V_1 V_2 \cdots V_n]^T \), the bus voltage \( V_{\text{bus}} \) and the bus current \( I_{\text{bus}} \) are measured to compute \( Z_l = \frac{V_{\text{bus}}}{I_{\text{bus}}} \). With knowledge of the external load \( Z_l \), the impedance matrix \( D \) in (6) can be updated and used to solve the LP problem in (9) to obtain the optimal current scaling \( \beta_{\text{opt}} \). With \( \beta_{\text{opt}} \) and the the impedance matrix \( D \), the resulting (optimal) individual module voltages \( V_{\text{opt}} \) in (10) can be communicated to each of the modules. The procedure can be implemented recursively in time and summarized in the procedure below.

Procedure: Assuming fixed internal impedances \( Z_k, k = 1, 2, \ldots, n \) but a time-varying load impedance \( Z_l \), the (centralized) recursive implementation is as follows:

1. Set time index \( t = 0 \) and communicate the \( n \) elements \( V_k[0] \) of the initial module voltages \( V[0] = [V_1[0] V_2[0] \cdots V_n[0]]^T \) to each of the modules \( k = 1, 2, \ldots, n \).
2. At time index \( t \), perform a measurement of \( V_{\text{bus}}[t] \) and \( I_{\text{bus}}[t] \) and compute the external impedance
\[
Z_l[t] = \frac{V_{\text{bus}}[t]}{I_{\text{bus}}[t]}
\]
(11)
and update the impedance matrix \( D[t] \) at time index \( t \) using (6).
3. Before the subsequent time step \( t + 1 \), compute the module voltages \( V_{\text{opt}}[t + 1] \) according to
\[
V_{\text{opt}}[t + 1] = \beta_{\text{opt}}[t] D[t] \begin{bmatrix} \beta_1 \\ \beta_2 \\ \cdots \\ \beta_n \end{bmatrix}
\]
(12)
where \( \beta_{\text{opt}}[t] \) is found by the LP problem in (9) using the updated impedance matrix \( D[t] \) and communicate the \( n \) elements \( V_k[t + 1] = V_{\text{opt}}[t + 1] = [V_1[t + 1] V_2[t + 1] \cdots V_n[t + 1]]^T \) to each of the modules \( k = 1, 2, \ldots, n \).
4. At time step \( t + 1 \), all modules \( k = 1, 2, \ldots, n \) update the module voltage \( V_k \) to \( V_k = V_k[t + 1] \).
5. Increment time index \( t = t + 1 \) and restart at step 1).

It should be noted that the recursive updates of \( V_{\text{opt}}[t] \) explained above converges in a single time step in case \( Z_l \) is fixed. In order to be able to track (fast) time-varying changes in the external load \( Z_l \), the above procedure should allow high
frequent measurements (and communication) of bus voltage $V_{bus}$ and bus current $I_{bus}$. Furthermore, the LP problem in (9) is solved and the results are used to communicate and update all the module voltages $V_{opt}[t+1] = [V_1 \ V_2 \ \cdots \ V_n]^T$ in (12). Since the LP program is solved and the elements of $V_{opt}[t+1]$ are communicated to each module, this is a centralized implementation of the recursive module scheduling. Each module $k = 1, 2, \ldots, n$ simply only receives its $V_k[t+1]$ from the (centrally) computed optimal LP solution $V_{opt}[t+1]$.

**IV. EXPERIMENTAL SETUP**

An experimental setup is built to demonstrate current scheduling, where the modulation demand signal can be applied and at the same time, voltage and current of each battery module can be measured. To explain the experimental setup, please refer to schematic diagram of Fig. 3 that indicates the parallel connection of 3 buck regulated battery modules. In addition, the parallel connection of 3 buck regulated battery modules is connected to a common DC bus and connected to an electrical load which is composed by a parallel connection of load resistors. Specifically, each parallel buck regulated battery module is composed of an adjustable power supply in series with an impedance, and a buck regulator. The buck regulator is composed by a pulse-width modulation (PWM) driven metal-oxide-semiconductor field-effect transistor (MOSFET), a fly-by diode, an inductor, and an Arduino Uno board.

**V. EXPERIMENTAL RESULTS**

For experimental verification of the centralized recursive balanced scheduling, 3 parallel placed battery modules with scaled down OCVs $V_1^{OCV} = V_2^{OCV} = V_3^{OCV} = 5\text{V}$ and internal impedance values $Z_1 = 3\Omega, Z_2 = 4.5\Omega,$ and $Z_3 = 6\Omega$ are used, subjected to a time-varying external load shown at the top of the Fig. 5. Specifically, in entire 700s experimental period, the external load is automatically increased 10 $\Omega$ every 100s from $t_0 = 0\text{s}$ to $t_1 = 400\text{s}$, and decreased 10 $\Omega$ every 100s from $t_1 = 400\text{s}$ to $t_2 = 700\text{s}$.

The resulting time-varying PWM modulation factors for the recursive updates of the internal voltage is shown in the bottom of the Fig. 5. Module 3 is always fixed at 100% modulation, because of its highest impedance $Z_3 = 6\Omega$, which needs to modulate down other battery modules to keep equal (balanced) currents. It should be noted that increasing PWM requires ramp function with 5s ramp-up period and decreasing PWM can happen instantaneously in order to protect the battery modules.

The experimental setup tester description is summarized by a photograph shown in Fig. 4. The power supply used in the experiment is GOPHERT CPS-6005 0-60V 0-5A Adjustable Switched Mode DC Power Supply. The MOSFET on the buck regulator is switched by corresponding control signals sent from PWM pins of the Arduino Uno board to modulate down OCV of that battery module. The Arduino Uno board can be employed to get current/voltage measured real-time signals by its analog input pins, and can also communicate with the computer through USB cable. In the computer, the MATLAB-Arduino interface is applied to automatically implement current scheduling algorithms and save measured real-time data simultaneously. Moreover, the MOSFETs applied in the experiment are driven by 62.5 kHz PWM modulation output frequency from Arduino PWM pins, and they are with low drain-to-source on-resistance that is suitable for high current of battery modules.

![Fig. 4. Photograph of the experimental battery tester.](image_url)
The experimental results for centralized recursive time-varying balanced scheduling are shown in Fig. 6. It can be seen that individual module currents keep relatively closed to each other in spite of time-varying external load, which verifies the feasibility of proposed centralized recursive scheduling for balancing individual battery module current.

VI. CONCLUSIONS

The efficiency and flexibility of a battery system that consists of parallel placed battery modules can be significantly improved when partly empty or failing modules of the battery pack can be exchanged for fast charging and fault correction capabilities. However, control or scheduling of battery modules is required to account for differences between state of charge, instantaneous and nominal capacity, and internal impedances of the battery modules.

In this paper a solution is provided that allows for centralized recursive current scheduling of parallel placed battery modules. The current scheduling algorithm uses a Linear Programming formulation to compute the optimal open circuit voltage values of each battery module so that currents of all battery modules are balanced to avoid stray currents between modules. This centralized current scheduling can adjust individual module currents to be equal (balanced) and increase the total bus current after optimization. Furthermore, an experimental setup with 3 parallel placed battery modules validates the optimal current scheduling algorithms. The experimental results indicate that the proposed method is able to effectively balance (equal) individual battery currents under time-varying external load conditions.

The future work of this study is to propose a decentralized recursive current scheduling method by solving the similar LP problem to efficiently reduce the centralized communication requirements on speed and reliability of the communication hardwares. By doing so, we hope to show that the decentralized solution can balance (equal) individual module currents and optimize total bus current in order to eliminate the need for high speed central communication between battery modules.

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Fig. 6. Current in battery modules for recursive centralized module scheduling of 3 parallel placed battery modules.