Resistance analysis and device design guideline for graphene RF transistors

Seul Ki Hong¹, Sang Chul Jeon², Wan Sik Hwang³ and Byung Jin Cho¹

¹ Department of Electrical Engineering, KAIST, Daejeon, 305-701, Korea
² National Nanofab Center (NNFC), Daejeon, 305-701, Korea
³ Department of Materials Engineering, Korea Aerospace University (KAU), Goyang-si, Gyeonggi-do, 412-791, Korea

E-mail: bjcho@kaist.edu

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Abstract
Graphene has attracted enormous attention in recent years because of its high carrier mobility and saturation velocity. High-performance graphene transistors for radio-frequency (RF) applications are especially attractive. Synthesis of high quality graphene sheets and application of various materials for gate dielectrics and substrates have been demonstrated. However, very few studies have been performed on the effects of graphene transistor parameters, such as parasitic resistances and graphene quality, in relation to RF applications. Here we report a systematic study of those effects on electrical performance depending on the transistor structure. It is found that the access resistance and contact resistance are the dominant factors leading to degradation of the device performance, especially in deep scaled devices. A guideline for device structural parameter design for required RF performance is discussed. Furthermore, we demonstrate that the newly proposed self-aligned structure can minimize access resistance component, resulting in 6 times higher cut-off frequency compared to that of the conventional structure, when the gate length is 50 nm. The findings of this study can be used to predict the device RF performance and thus help the design of graphene transistor structures to meet specific requirements.

1. Introduction
Graphene is considered one of future channel materials in high speed semiconductor devices because of its high carrier mobility, high saturation velocity, high current density, and ultra-thin geometry structure [1–7]. Within the past few years, significant progress has been made in the areas of graphene synthesis, device fabrication, and integration for graphene radio-frequency (RF) electronic applications [8–10]. These achievements have led to demonstration of cut-off frequency (fT) of 100 GHz and higher [11, 12] and further improvement can be achieved by enhancing graphene quality and/or device integration techniques. At the early stage of graphene device research, significant efforts were focused on investigating the charge carrier transport property, which is affected by the graphene quality, substrate materials, graphene-dielectric stacks, and fabrication process [8–11]. Despite these efforts, the device performance of graphene RF electronics is still far from the ideal level that graphene promises [2]. Recent reports on graphene RF devices claim that device integration often generates undesirable parasitic components. In particular, the parasitic resistances of the graphene transistors are the critical factor degrading performance in graphene RF devices [13]. The total resistances (R_{TOTAL}) in the MOS transistors consist of the channel resistance (R_{CH}) and parasitic resistances, which mainly include contact resistance (R_C) and access region resistance (R_A), as shown in figure 1. The access resistance, R_A, is the series resistance of the graphene between the gate electrode edge and the source/drain electrode edge. R_C is an undesirable resistance component that degrades the device performance, as the resistance is beyond the control of the gate bias. R_A and R_C become more prominent as the device is scaled down below the sub-micrometer regime because they are not scaled proportionally to the R_{CH}, and eventually the parasitic resistance can dominate the total resistance in deep scaled devices. It is therefore very timely and necessary to study these parasitic
resistances and understand their impact on the device performance, especially for graphene RF devices. In this work, we identify the critical device structural parameters in both a long channel device and a scaled device. This is an important step to expedite successful realization of graphene RF devices.

2. Experiment

CVD growth of graphene was carried out by an inductively coupled plasma enhanced chemical vapor deposition process. A 4 inch SiO2/Si wafer with a 300 nm thick Cu film was used for the substrate for graphene growth. During the synthesis of graphene, the wafer was heated to 750 °C at 50 mTorr in an Ar ambient, and H2 plasma was supplied to the process chamber for sample treatment. After purging with Ar for 2 min, a mixture of C2H2 and Ar (C2H2:Ar = 1:40 sccm) was then flowed into the chamber with 150 W RF plasma; this is the main step of graphene growth. Subsequently, the wafer was cooled in a vacuum ambient for 2 h. Synthesized graphene on the metal film was transferred onto 100 nm thick SiO2 on a p+ silicon wafer using PMMA. The transferred graphene layer was then annealed in a H2 ambient at 400 °C for 30 min to remove residues on the graphene layers. A graphene channel was defined with standard lithography. For the metal electrode of the device, an Au (50 nm)/Pd (10 nm) layer was deposited by a thermal evaporator and patterned by a lift-off process. The graphene area under source/drain electrode is 10 × 6 μm. The device was then annealed in a vacuum ambient (∼1 × 10−7 Torr) for 12 h to remove possible adsorbates on graphene. The electron beam lithography was used to form short channel device. Gate dielectric consist of 0.5 nm Al seed layer deposited by thermal evaporation and a 20 nm Al2O3 layer by atomic layer deposition. A stack of gate dielectric and 50 nm Au deposited by thermal evaporation was patterned by a lift off process. To form a self-aligned structure, a thin Pd layer (10 nm) was also deposited and patterned by a lift-off process.

The current–voltage characteristics of the graphene transistor were determined using a parameter analyzer (Agilent B1500). A vector network analyzer (Anritsu 37397D) with standard ground-signal-ground probes was used to study high-frequency scattering parameters (S) of the graphene transistors. The system was calibrated using the short-open-load-through (SOLT) method, and on-chip open and short structures were used to de-embed parasitic effects such as the pad capacitance and interconnection resistance. The ‘open’ test structure only consisted of large photolithography-defined pads, while the short test has additional metal to short the gate, source, and drain pads. The mobility was extracted from the current–voltage characteristics and Hall effect measurement.

3. Results and discussion

In order to evaluate the impact of various resistances on the RF performance of graphene devices, the values of $R_{CH}$, $R_C$, and $R_A$ in the given devices must be extracted. In this work, for better accuracy in the resistance measurement, the transfer length method [14–17], which can define the various channel lengths ($L_{CH}$) and access region lengths ($L_A$), was used. Figure 2(a) shows the measured total resistance plotted as a function of $L_A$. Since the total resistance is $R_{CH} + 2R_C + 2R_A$, the extrapolation of the data points down to $L_A = 0$ nm gives the value of $R_{CH} + 2R_C$ and the sheet resistance of the access region can be found from the slope of the line, which value is 1.17 kΩ/□. The $R_{CH} + 2R_C$ values extracted from figure 2(a) were again plotted as a function of $L_{CH}$ with different gate voltages in figure 2(b). Again, the extrapolation down to $L_{CH} = 0$ nm gives the value of $2R_C$. In this plot, the corresponding $R_C$ was found to be 136.5 Ωμm. The slope in figure 2(b) represents the resistivity of $L_{CH}$ depending on different gate voltages, which modulate...
the charge carrier density in the channel. $R_{CH}$ is changed from $\sim 1.6 \text{ K} \Omega$ to $\sim 1.9 \text{ K} \Omega$ at $V_G = -3$ to $3 \text{ V}$. Using this method, the resistance components, $R_{CH}$, $R_A$, and $R_C$, were extracted through a large data set of more than 150 devices. This systematic analysis enables us to evaluate the effects of these resistances on the RF performance of graphene devices with various device dimensions.

The dependence of resistance components ($R_{CH}$, $R_A$, and $R_C$) on different device dimensions is illustrated in figure 3. First, the ratio of each resistance component was plotted as a function of $L_A$ when $L_{CH}$ is fixed at 50 nm and 1000 nm, in figures 3(a) and (b), respectively. The device with $L_{CH} = 1000 \text{ nm}$ (figure 3(b)) shows that $R_{CH}$ is the dominant resistance term and thereby the charge carrier transport is well controlled by the gate voltage, as is normally expected in field effect transistors. However, in the case of the short channel devices, as shown in figure 3(a), the $R_{CH}$ term is merely a small portion of the total resistance and $R_C$ and $R_A$ dominate the total resistance. In this case, the charge carrier transport becomes insensitive to $R_{CH}$ and consequently the device loses gate controllability. For example, when $L_{CH} = 50 \text{ nm}$ and $L_A = 300 \text{ nm}$, $R_{CH}$ is only around 10% of the total resistance. This means that only 10% of the modulation of the channel carrier density is reflected to the change of the drain current. This result vividly shows how $R_C$ and $R_A$ are the critical performance killers in graphene transistors, especially when $L_{CH}$ is below 100 nm. In addition, it also should be noted that for short channel devices, when $L_A$ decreases, $R_C$ increases in a quadratic manner.

Figures 3(c) and (d) show the resistance ratio as a function of $L_{CH}$ when $L_A$ is fixed at 10 and 500 nm, respectively. This result shows that under a high $R_A$ ($L_A = 500 \text{ nm}$), in figure 3(d), the short channel device can never be properly operated because the $R_A$ term accounts for more than 80% of the total resistance. On the other hand, under a low $R_A$ ($L_A = 10 \text{ nm}$), in figure 3(c), $R_C$ is recognized as a critical factor for the short channel devices of $L_{CH} < 100 \text{ nm}$. The resistance ratio in figure 3 clearly shows that as the device is scaled down, more effort should be given to minimizing parasitic resistances rather than charge carrier transport.

Next we extended this analysis to the RF performance of a graphene FET. Figures 4(a) and (b) show the cut-off frequency of graphene devices as a function of $L_{CH}$ at different $R_C$ and $R_A$, which were extracted from figure 2. The cut-off frequency ($f_T$) is given by $f_T = g_m/2\pi C_G$, where $C_G$ is the total gate capacitance (in this experiment, 330 nF cm$^{-2}$) and $g_m$ is the maximum transconductance [18], which was extracted from the current–voltage ($I_D$–$V_G$) characteristics. $I_D$–$V_G$ characteristics is given by $I_D = V_D/R_{TOTAL}$ ($R_{TOTAL} = R_{CH} + 2R_C + 2R_A$). The $R_C$ and $R_A$ are unaffected by the gate voltage, so they cannot be changed by $L_{CH}$. The $R_C$ and $R_A$ are already extracted in figure 2. The $R_{CH}$ has linear relationship with $L_{CH}$ and reference values of $R_{CH}$ ($L_{CH}$ at 100, 500 and 1000 nm) for each $V_G$ are also extracted in figure 2. The $R_{TOTAL}$ at this point for each $L_G$ are found to be summation of calculation values.

Here, the top straight curve in figures 4(a) and (b) indicates the maximum achievable ($f_T$) at the given channel length when the parasitic resistances $R_C$ and $R_A$ do not exist. According to this, $f_T$ of 1 THz is achievable when the channel length is 90 nm with a CVD graphene channel if $R_C$ and $R_A = 0$. However, in the real situation, as can be seen in the result, when $R_C$ is larger than 250 $\Omega$, $f_T$ is weakly correlated to $L_{CH}$. This means, in this situation, even though the device $L_{CH}$ is shortened, the RF performance of the graphene devices would not be improved. $f_T$ becomes inversely correlated to $L_{CH}$ in a logarithm scale only when $R_C$ approaches zero. Similar results can be observed in figure 4(b), which shows $f_T$ as a function of $L_{CH}$ with

![Figure 2](image_url)

Figure 2. (a) Total resistance as a function of access length with a parameter of channel length, and (b) resistance $R_{CH} + 2R_C$ as a function of channel length when $L_A$ is fixed at zero.
different $L_A$ at $R_C = 0 \Omega$. The extracted $f_T$ is again weakly linked to $L_{CH}$ at $L_A > 1 \mu m$, while $f_T$ becomes inversely proportional to $L_{CH}$ in a logarithm scale as $L_A$ approaches zero. Figures 4(c) and (d) show $f_T$ as a function of $L_{CH}$ with a parameter of graphene channel mobility at $L_A = 250$ nm and $L_A = 0$ nm, respectively, under $2R_C = 50 \Omega$, which is a low parasitic resistance situation. This result shows that under such low parasitic resistances, improvement of graphene quality can have a direct impact on the RF performance of the device. The intrinsic mobility of graphene is known to be as high as $200,000$ cm$^2$ V$^{-1}$ s$^{-1}$, while the field-effect mobility of CVD graphene devices is reported to be around $1000$ cm$^2$ V$^{-1}$ s$^{-1}$. This difference results in a more than two orders of magnitude difference in $f_T$ [2, 19–22].

Low $R_A$ and $R_C$ values appear to be beneficial to $f_T$. However, the contact resistance $R_C$ has a fundamental limit [23] and is often determined by metal selection and the deposition method. Also, it is desirable to minimize $L_A$ as much as possible, in order to reduce $R_A$, but at the same time it cannot be zero because the gate electrode must be electrically isolated from the S/D electrodes. Therefore, optimization of these parameters is extremely important. The results in figure 4 can be used as an RF device design guideline as $f_T$ can be projected at the given device structure. As a practical solution to minimize $L_A$ in order to improve the RF performance, we propose a new process scheme for a self-aligned graphene RF device. The schematic fabrication process of a graphene transistor with a self-aligned gate is illustrated in figure 5. Large area monolayer graphene was synthesized and transferred onto a Si substrate with a 90 nm thick top SiO$_2$ layer, as done in previous reports [6, 24, 25]. The channel length of the fabricated self-aligned graphene RF devices is $\sim 50$ nm which shown in figure 5(h). For comparison, a conventional graphene RF device with the same channel length was fabricated as well. By adopting the self-aligned structure, $L_A$ becomes as short as 10 nm, while the conventional graphene RF device has a $L_A$ of 250 nm. The self-aligned structure proposed here differs from that provided by previous methods to fabricate self-aligned transistors [25–27], where lift-off techniques were used to achieve the gate stack. The current gain of the self-aligned gated graphene device and the conventional graphene device are plotted as a function of frequency in figure 6(a).
The frequency characteristics of the two graphene devices were obtained in a range of gate voltage from −3 to 3 V at $V_{DS} = 0.5$ V. In addition, the standard on-chip S-parameter measurements were used with a vector network analyzer over a frequency range of 1–40 GHz. The measurements were first calibrated to the probe tips using an off-chip calibration substrate by a SOLT procedure. A de-embedding procedure was then used to eliminate the effect of the co-planar waveguide pads on the RF performance by measuring on-chip ‘open’ and ‘short’ test structures [28, 29]. The current gains denoted as ‘none’ and ‘de-embedded’ are the results before and after the de-embedding procedure, respectively.

The conventional graphene devices with $L_{CH}/L_A = 50/250$ nm show a $f_T$ of 25 GHz, whereas the self-aligned gated graphene devices with $L_{CH}/L_A = 50/10$ nm show a $f_T$ of up to 150 GHz. Since all other device parameters of the two devices are identical except $L_A$, these experimental results clearly show the significance of reduction of the access resistance in terms of RF performance. The inset shows maximum frequency of self-aligned gated graphene devices, and it is up to 30 GHz. Figure 6(b) shows a comparison between the results in figure 6(a) and the calculated $f_T$ from the analysis from figures 1 to 4. The measured $f_T$ matches very well with the calculated $f_T$, which strongly supports the accuracy of our analysis in figures 1–4. This confirms the analysis results here can successfully be used as a design guideline for graphene RF devices.

4. Conclusions

In summary, we have analyzed the resistance ratio of $R_{CH}$, $R_A$, and $R_C$ in a graphene RF device and discussed its impact on RF performance. This analysis will help design graphene RF device structures according to the target operating frequency. The proposed self-aligned structure can be a solution to minimize the parasitic resistance, thereby improving the RF performance of the graphene device.
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Figure 5. Schematic diagram of fabrication process for self-aligned graphene RF device. (a) Graphene is transferred onto a 90 nm thick SiO2 substrate and (b) a pad electrode is deposited by thermal evaporation. (c) E-beam resist is exposed and developed. (d) A gate stack of Al2O3 and Pd/Au is deposited and (e) patterned by a lift-off process. (f) A thin Pd layer is deposited to form self-aligned source and drain contacts. (g) Complete self-aligned graphene RF device. (h) SEM images of self-aligned graphene RF device and gate electrode with short channel length.

Figure 6. (a) Current gain (H21) before (black line) and after (red line) the de-embedding procedure of conventional and self-aligned graphene transistors. The inset shows the maximum frequency. (b) Comparison of experimental cut off frequency (fT) with the calculated results from the resistance analysis described in figures 1–4.
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