Depleted fully monolithic CMOS pixel detectors using a column based readout architecture for the ATLAS Inner Tracker upgrade

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ABSTRACT: Depleted monolithic active pixel sensors (DMAPS), which exploit high voltage and/or high resistivity add-ons of modern CMOS technologies to achieve substantial depletion in the sensing volume, have proven to have high radiation tolerance towards the requirements of ATLAS in the high-luminosity LHC era. DMAPS integrating fast readout architectures are currently being developed as promising candidates for the outer pixel layers of the future ATLAS Inner Tracker, which will be installed during the phase II upgrade of ATLAS around year 2025. In this work, two DMAPS prototype designs, named LF-Monopix and TJ-Monopix, are presented. LF-Monopix was fabricated in the LF Foundry 150 nm CMOS technology, and TJ-Monopix has been designed in the TowerJazz 180 nm CMOS technology. Both chips employ the same readout architecture, i.e. the column drain architecture, whereas different sensor implementation concepts are pursued. The paper makes a joint description of the two prototypes, so that their technical differences and challenges can be addressed in direct comparison. First measurement results for LF-Monopix will also be shown, demonstrating for the first time a fully functional fast readout DMAPS prototype implemented in the LF Foundry technology.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Front-end electronics for detector readout; VLSI circuits

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1 Introduction

Monolithic active pixel sensors (MAPS) have already matured enough to be used in high energy physics experiments, as high precision tracking and vertexing devices [1–3]. They are now making their path into the high-rate and high-radiation applications, where a depleted sensing volume is mandatory for charge to be collected sufficiently fast by drift. CMOS pixels with depleted sensing volume, also labelled as depleted monolithic active pixel sensors (DMAPS), can be achieved by exploiting the high-resistivity and/or high-voltage add-ons of modern CMOS technologies [4]. Many such devices have been reported, showing high radiation tolerance towards the requirements of the ATLAS experiment in the High-Luminosity LHC (HL-LHC) era [5–8]. Moreover, multiple nested wells, available in many commercial CMOS processes, allow to implement full CMOS electronics inside the pixel (see section 2). As a result, more complex and faster readout architectures are possible for monolithic CMOS pixels, beyond the traditionally used rolling shutter readout. As a part of the CMOS program for the future ATLAS Inner Tracker (ITk) at HL-LHC, DMAPS integrating fast readout architectures are under development. They may serve as a high performance and cost effective option for the outer pixel layers of ITk, replacing the complex and expensive hybrid pixel modules. Such DMAPS devices need to sustain particle fluence of $10^{15}$ n$_{eq}$/cm$^2$ combined with 50 Mrad total ionizing dose. Meanwhile, they should be able to deal with the particle rate expected at HL-LHC and exhibit timing precision of 25 ns.

This work presents two DMAPS prototypes, both integrating on the sensor substrate a column based readout architecture called column drain readout, which is similar to the FE-I3 readout chip for the present ATLAS pixel detector [9]. The use of column drain readout is mainly driven by its proven rate capability for the inner layers of the current ATLAS pixel detector, where the particle rate is similar to what is expected at the outer pixel layers of ITk. The first prototype, named LF-Monopix, has been fabricated in the LFoundry 150 nm CMOS technology, featuring a large charge collection electrode, usually preferred for high radiation tolerance. In contrast, a small
sensing node is employed in the second prototype with the name of TJ-Monopix, where a fully depleted sensitive layer can be expected by profiting from a modified process in the TowerJazz 180 nm CMOS imaging technology [10]. The two prototypes will be jointly described regarding the sensor concept (section 2) and chip design (section 3), in order to address their technical features and challenges in a direct comparison. In section 4, first measurement results for LF-Monopix will be shown. Section 5 will summarize the work.

2 Sensor concepts

The implementation of DMAPS can be categorized by the fill factor, i.e. the ratio of the sensing electrode area to the total pixel area [11]. The two prototypes in this work employ respectively the large and small fill factor concepts, and are implemented as described in the following.

**Figure 1.** Cross section view of one pixel cell implemented (a) in the LFoundry 150 nm technology with the large fill factor design and (b) in the TowerJazz 180 nm technology with a small fill factor design.

**LF-Monopix.** Figure 1(a) shows the simplified cross section view of a pixel cell in LF-Monopix. The sensing volume is a high resistivity P-substrate (> 2 kΩ·cm). The charge collection node is formed by a very deep N-well, which encloses the in-pixel electronics. Full CMOS circuitry is possible because of the isolation between the N-well, hosting the PMOS transistors, and the charge collection N-well, by a deep P-well. High charge collection efficiency after radiation damage can be expected from a large charge collection electrode, and the irradiation studies of the LFoundry sensor based on a previous prototype can be found in [6, 7]. However, such a sensor design may suffer from large detector capacitance up to ~ 400 fF, especially when complex in-pixel logic is needed to implement a fast readout architecture [11, 12]. The large detector capacitance will slow down the pre-amplifier and increase the noise, which can only be compensated by increasing the power. Moreover, the substrate noise introduced by the in-pixel electronics is directly coupled to the sensing node, and many design efforts are needed to mitigate this issue, including customized in-pixel digital logic and careful layout design [12]. The typical pixel size of the sensors developed in the LFoundry technology is 50 × 250 μm², with a fill factor higher than 50%. Although much smaller pixels are possible for passive sensor designs and for simple active pixels (e.g. 3T pixel), it is very challenging to have a small pixel, e.g. 50 × 50 μm², for fast readout monolithic designs. Another note for the LFoundry sensor is that the sensor can be thinned from the back side down to ~ 100 μm, and reverse bias can be applied from the back side in order to achieve uniform drift field. Thanks to the high resistivity substrate, only ~ 30 V of reverse bias can already fully deplete the 100 μm thinned sensor [7].
**TJ-Monopix.** As depicted in figure 1(b), TJ-Monopix uses a high-resistivity (> 1 kΩ·cm) P-type epitaxial layer, grown on top of a highly P-doped wafer substrate, as the sensitive layer. The typical thickness of the epitaxial layer is 25 µm. The charge collection electrode is a small N-well of several µm². A deep P-well is used to shield the N-wells that host the PMOS transistors, which would otherwise work as competing charge collection nodes. The use of a small collection node in high radiation environment is encouraged by the R&D progress recently made to improve the sensor depletion by using a modified process developed together with the foundry [10]. The irradiation study on a test chip, fabricated in the modified process, has showed uniform efficiency for 25 µm and 30 µm square pixels, even after fluence of $10^{15}$ n$_{eq}$/cm$^2$ [8]. The main motivation to push forward the R&D of DMAPS with a small sensing diode is its very small detector capacitance (e.g. < 5 fF), which allows to minimize the analog power with given analog performance [13]. In addition, the small footprint of the sensing diode, together with a very compact front-end (FE) circuit made possible by the small detector capacitance (see section 3.2), allows to implement highly granular pixels, which is very difficult for the large fill factor design. However, more studies are still needed to prove sufficient radiation tolerance for large pixels (e.g. > 50 µm×50 µm), in case a very complex in-pixel circuit is needed to implement a fast readout architecture. It is noted that the small detector capacitance will also lead to very low noise, i.e. less than 20 e$^-$. However, this doesn’t necessarily result in better signal to noise ratio than the LFoundry design, because the expected signal is also smaller for the TowerJazz sensor due to the slim sensitive layer.

### 3 Chip overview

| Parameter          | LF-Monopix          | TJ-Monopix          |
|--------------------|---------------------|---------------------|
| CMOS tech.         | LFoundry 150 nm     | TowerJazz 180 nm    |
| Sensor concept     | Large fill factor   | Small fill factor   |
| Chip size          | ~ 1 × 1 cm$^2$      | ~ 1 × 2 cm$^2$      |
| Pixel pitch        | 50 × 250 µm$^2$     | 36 × 40 µm$^2$      |
| Matrix size        | 129 × 36            | 224 × 448           |
| Static current/pixel| ~ 20 µA            | < 1 µA              |
| Output data link   | 1× LVDS@160 MHz     | 4× CMOS@40 MHz      |

The LF-Monopix chip is the first fully monolithic prototype of a DMAPS series implemented in the LFoundry technology aimed for high radiation environment [14, 15]. Its design has significant inputs from its ancestor LF-CPIX [15], e.g. pre-amplifier, guard ring structure, chip floor plan. The TJ-Monopix chip was later designed as a part of the TowerJazz DMAPS R&D, aimed to translate the well understood column drain architecture, based on the experience of LF-Monopix, into the TowerJazz small fill factor sensor design. Both of the two prototypes are large scale demonstrator chips, and some main parameters are listed in table 1.
3.1 Chip architecture

Though having different layout floor plans, both LF-Monopix and TJ-Monopix follow the same chip architecture as depicted in figure 2. The readout chain starts with the pixel FE circuit, i.e. the pre-amplifier and the discriminator. The discriminator fires when the analog signal pulse crosses its threshold, and the output holds until the analog pulse falls below the threshold. Coarse analog information can be obtained by measuring the width of the digital pulse at the discriminator output, a technique called time over threshold (ToT). Two gray encoded time stamps, corresponding to the leading edge (LE) and trailing edge (TE) of the discriminator output, are written into the two in-pixel RAM cells to record the hit time and pulse width. The pixel readout is arbitrated by a token propagation, with the topmost pixel having the highest readout priority. The pixel column interfaces with the End-of-Column (EoC) circuitry, which includes the gray counter running at 40 MHz to generate the time stamp with 25 ns steps, the sense amplifiers to receive the column data, and the EoC logic to perform the column-level readout priority scan and transmit data to the serial link. In these first prototypes, for design simplicity, the readout controller, which controls the readout sequence, is implemented in an FPGA. Triggering buffers are not included either, hence all the hit data is transmitted sequentially through the serial link off chip.

3.2 Pixel

This section describes the pixel design. As a result of the two distinctive sensor concepts, the pixel designs for the two prototypes are very different regarding the sensor geometry and the FE circuit.

LF-Monopix. The layout of a typical pixel in LF-Monopix is shown in figure 3 (upper). The pixel size is $50 \times 250 \mu m^2$. The charge collection well is represented by the shaded area, giving a fill factor about 55%. The schematic of the FE circuit is also shown in figure 3 (lower). The pre-amplification stage is a typical charge sensitive amplifier (CSA), AC coupled to the sensor. The signal charge is...
integrated on the feedback capacitor $C_f$. The DC feedback, mainly composed of the current mirror M1 and M2, stabilizes the operation point and continuously discharges the integrated signal. The output of the CSA is sent to a discriminator, whose threshold can be trimmed by a 4-bit in-pixel DAC (digital-to-analog converter). Thanks to the AC coupling between the CSA and discriminator, the baseline of the discriminator input is set to $V_{BL}$ via the MOS resistor M3, independent of the DC level of the CSA. The biasing of M3 is set globally by an on-chip current DAC adjusting the current $I_{BL}$. The detailed schematics of CSA and discriminator can be found in [12]. The total bias current of the FE is $\sim 20 \, \mu A$.

**Figure 3.** Layout of a typical pixel cell in LF-Monopix (upper) and schematic of its FE circuit (lower).

**TJ-Monopix.** The layout of 4 neighboring pixels in TJ-Monopix is shown in figure 4 (left). Each pixel has an area of $36 \times 40 \, \mu m^2$. The region for digital circuit is shared by two columns, so that the analog FE circuit and its biasing lines are well separated from the digital cross talk. The charge collection well is located in the center of each pixel, and it has an octagon shape with a diameter of $2 \, \mu m$. The spacing between the charge collection node and its nearest P-well is $3 \, \mu m$ (refer to

**Figure 4.** Layout of four neighboring pixels (left) and schematic of the FE circuit (right) of TJ-Monopix.
The estimated detector capacitance is less than 5 fF, almost two orders of magnitude smaller than LF-Monopix. The small detector capacitance allows the use of a very compact and low power FE circuit derived from the ALPIDE chip [16]. As shown in figure 4 (right), the signal charge is integrated on the capacitance of the input node $\text{PIX}_\text{IN}$. The low capacitance leads to large voltage excursion at the input node, and the resulting voltage signal is amplified and shaped by the FE circuit, generating a voltage pulse at the node $\text{OUTA}$. At the designed bias condition, the charge-to-voltage conversion gain at $\text{OUTA}$ was simulated to be $\sim 500 \mu \text{V}/\text{e}^-$. Such a high gain makes it possible to use a simple inverting stage (M6 - M8) as the discriminator without threshold trimming. Therefore, the layout of the FE is very compact, allowing for small pixel area. As compared to the ALPIDE FE, the circuit in figure 4 removes the clipping scheme introduced in ALPIDE to compress the pulse from large signals. The purpose is to preserve the analog information through ToT. In addition, the FE has been optimized for fast rising time ($< 25 \text{ ns}$) by careful trade-off between power and speed, and the resulting bias current is less than 1 $\mu \text{A}$ per pixel.

## 4 First results for LF-Monopix

The LF-Monopix wafers were received in March 2017. Extensive characterization is currently in progress, both in lab and in beams. This section shows some first laboratory results.

![I-V curve](image)

**Figure 5.** I-V curve of LF-Monopix at room temperature. The voltage value refers to the reverse bias voltage.

**I-V curve.** A high bias voltage is essential to ensure sufficient sensor depletion after high level irradiation. The highest voltage that can be applied is limited by the sensor breakdown behavior. Therefore, the sensor leakage current was measured as a function of reverse bias voltage. Figure 5 shows the I-V curve of LF-Monopix measured at room temperature. The breakdown was measured at -280 V, a value much higher than a previous chip generation in the same technology [14]. The improvement was made possible by optimizing the guard ring structure based on TCAD simulation. The study of guard rings is beyond the scope of this paper, and can be found in [17]. It is noted that the depletion depth is expected to be well beyond 50 $\mu \text{m}$ with bias voltage over 100 V after fluence of $10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ [7], and the high breakdown voltage measured for LF-Monopix is a strong indication of sufficient signal after particle fluence of the HL-LHC level.

**Noise and threshold distribution.** The noise performance and threshold distribution were studied by scanning an external injection signal into the sensing node and recording the probability of pixel firing with a fixed threshold setting, obtaining the so-called “S curves”. The noise and threshold
parameters of each pixel can be extracted by fitting the corresponding “S curve” with the error function. The injection signal was calibrated by comparing the response of the sensor to the injected voltage with the peak position of the spectra obtained by exposing the sensor to an $^{241}$Am radioactive source and the X-ray fluoresce of Terbium. Figure 6 shows the measured noise and threshold distribution of four pixel columns, composed of one pixel variant with full in-pixel readout logic. The average noise value is $191 \, e^-$, with dispersion of $27 \, e^-$. The threshold was tuned to around $2500 \, e^-$, and the threshold dispersion is about $100 \, e^-$ after tuning. It is noted that these results are comparable to the current ATLAS pixel detector [18].

![Figure 6.](attachment:image.png)

**Figure 6.** (a) Noise distribution and (b) Threshold distribution before (blue) and after (red) tuning for one pixel variant with full in-pixel readout logic.

## 5 Summary

Two large scale DMAPS prototypes are presented in this work, both having the column drain readout electronics integrated on the sensor substrate. The goal is to demonstrate the feasibility of using fully monolithic CMOS pixels in the outer pixel layers of the future ATLAS ITk.

The LF-Monopix, fabricated in the LFoundry 150 nm CMOS technology, employs the large fill factor sensor concept, as a safe choice for radiation hardness. Preliminary test results on the LF-Monopix IC (Integrated Circuit) have demonstrated that LF-Monopix is, at least matrix-wise (i.e. missing high speed output link, trigger memory, etc.), a fully functional ATLAS pixel chip having full readout with ToT and tunable threshold. Systematic study on the performance of different pixel variants is still ongoing, which will allow us to choose the best pixel design. Two test beam campaigns have been recently performed, one using the electron beam at ELSA (University of Bonn), the other with pions at CERN SPS. The efficiency and timing analysis will be available soon. Chip samples irradiated with neutrons and protons, with dose levels up to $2 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ and 150 Mrad respectively, will also be characterized to study the irradiation performance.

The TJ-Monopix, which has been recently submitted, is implemented in the TowerJazz 180 nm CMOS technology. By using a novel modified process, a fully depleted sensitive layer is expected even with a small sensing electrode. The small detector capacitance brings the benefits of very low power ($< 2 \mu\text{W/pixel}$) and small pixel ($< 50 \mu\text{m} \times 50 \mu\text{m}$). The TJ-Monopix demonstrator is expected to be back from the foundry at the end of 2017.
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