tcFFT: Accelerating Half-Precision FFT through Tensor Cores

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ABSTRACT
Fast Fourier Transform (FFT) is an essential tool in scientific and engineering computation. The increasing demand for mixed-precision FFT has made it possible to utilize half-precision floating-point (FP16) arithmetic for faster speed and energy saving. Specializing in lower precision, NVIDIA Tensor Cores can deliver extremely high computation performance. However, the fixed computation pattern makes it hard to utilize the computing power of Tensor Cores in FFT. Therefore, we developed tcFFT to accelerate FFT with Tensor Cores. Our tcFFT supports batched 1D and 2D FFT of various sizes and it exploits a set of optimizations to achieve high performance: 1) single-element manipulation on Tensor Core fragments to support special operations needed by FFT; 2) fine-grained data arrangement design to coordinate with the GPU memory access pattern. We evaluated our tcFFT and the NVIDIA cuFFT in various sizes and dimensions on NVIDIA V100 and A100 GPUs. The results show that our tcFFT can outperform cuFFT 1.29x-3.24x and 1.10x-3.03x on the two GPUs, respectively. Our tcFFT has a great potential for mixed-precision scientific applications.

CCS CONCEPTS
• Theory of computation → Massively parallel algorithms.

KEYWORDS
FFT, DFT, mixed precision, GPU, Tensor Cores

1 INTRODUCTION
Fast Fourier transform (FFT) is essential in many scientific and engineering applications, including large-scale simulations [6], time series [30], waveform analysis [4], electronic structure calculations [15], and image processing [8]. Due to its wide range of applications, improving the performance of FFT is of great significance. Many efforts have been made from algorithm and hardware aspects. Lots of optimized implementations of FFT have been proposed on the CPU platform [11, 12], the GPU platform [5, 22] and other accelerator platforms [18, 25, 28].

The demand for mixed-precision FFT is also increasing, while half precision (FP16) is gaining popularity with its faster speed and energy saving ability [20]. Most of the popular FFT frameworks such as cuFFT, FFTW for ARM (Arm Performance Libraries), Vulkan FFT, include support for half precision besides single and double precision. And a noticeable number of scientific applications use half-precision FFT. The gravitational wave data analysis software pyCBC [4] and the cosmological large-scale structure N-body code CUBE [6, 32] use half precision to speed up the long-length FFT calculation. Medical image restoration applications [8, 19] use lower precision or mixed precision to speed up the computation of batched 2D FFT. Specializing in lower precision, NVIDIA Tensor Cores can deliver extremely high performance which makes it worthwhile to take on the challenge of designing and implementing novel FFT algorithms on them.

However, there are still following challenges to accelerate FFT with Tensor Cores which are specialized for GEMM operations. The first challenge is how to efficiently support FFT’s special operations on Tensor Cores. Second, memory can easily become the bottleneck of FFT algorithms due to their modest arithmetic intensity and unique memory access pattern. To give full play to the computation performance of Tensor Cores, the algorithm needs to be well-designed in data arrangement. Third, FFTs of different sizes use different kernels. Large size FFTs use more complicated kernels. Therefore, it is difficult to obtain a relatively consistent optimization effect on various FFT sizes.

Several approaches [7, 9, 29] have been proposed for using Tensor Cores in the computation of FFT. Sorna [29] and Cheng [7] gave the theoretical basis and an example implementation which resorted to cuBlas to utilize Tensor Cores. But the performance of their implementation is far inferior to cuFFT. In Durrani’s poster [9], their implementation with Tensor Core WMMA APIs outperformed cuFFT, but only on the basic small size 1D FFT. They did not deal with the memory bottleneck caused by the unique memory access pattern of large size or multidimensional FFT, and there is still considerable room for improvement in their method to support FFT’s special operations.

We designed and implemented tcFFT, the first FFT library on Tensor Cores which supports batched 1D and 2D FFT in a wide range of sizes with high performance, and it is open-source at https://github.com/given_in_the_official_version. It can outperform cuFFT in common half-precision FFT applied scenarios [4, 6, 8, 19, 32] and uses the similar interface to cuFFT. We have overcome the key challenges in implementing such a universal size supported FFT library with two major novel techniques. (1) First, FFT’s special operations, complex matrix accesses and element-wise multiplications, are not natively support by Tensor Cores. This reduces the benefits of using Tensor Cores. To perform these operations more efficiently, we proposed a method to operate Tensor Core fragments with single element granularity according to the map of matrix elements into each thread’s registers. (2) Second, merging processes of large size or 2D FFT require strided memory accesses, and uncoalesced strided global memory accesses are quite inefficient on GPU. Besides using shared memory to reduce the number of global memory accesses, we redesigned the data layout in memory and implemented a continuous memory access pattern with variable size. This pattern can ensure that there are sufficient continuous elements when accessing the data.

In summary, this paper makes the following contributions.
• We developed tFFT to accelerate FFT on Tensor Cores with high performance, which supports batched 1D and 2D FFT of various sizes. (Sec 3).
• We propose two major novel techniques to improve its performance: a) a single-element manipulation on Tensor Core fragments to efficiently support special operations needed by FFT (Sec 4.1); b) a special design for data arrangement and a continuous memory access pattern with variable size to alleviate the memory bottleneck (Sec 4.2);
• We evaluate tFFT on NVIDIA Volta and Ampere GPUs. On V100, it achieves 1.90x speedup on average on 1D FFTs and 1.29x-3.24x speedup on 2D FFTs over half-precision kernels on CUDA cores from cuFFT. On A100, it achieves 1.24x on average and 1.10x-3.03x, respectively (Sec 5).

2 BACKGROUND

2.1 FFT in Matrix Form

Fast Fourier transform is an efficient algorithm to compute the discrete Fourier transform (DFT) of a sequence. The DFT converts an N-point sequence into a same-length sequence, according to the following equation, where \( x \) denotes the original sequence and \( X \) denotes its DFT:

\[
X[k] = \sum_{n=0}^{N-1} x[n] e^{-j2\pi nk/N} \tag{1}
\]

This process can be viewed as a matrix-vector multiplication between the DFT matrix and the original sequence. The computational complexity of this process is \( O(N^2) \). The DFT is useful in many fields, but computing it directly from the definition is often too slow to be practical. One of the most widely used FFT algorithm, Cooley-Tukey FFT algorithm, reduce the computational complexity to \( O(N\log(N)) \). This algorithm can calculate the DFT of an N-point sequence from \( N_1 \) DFTs of its \( N/N_1 \)-point subsequences according to equation 2 which can be used recursively until the size of the subsequences is 1. The basic flow of the algorithm has three steps:

1. Divide the original N-point sequence into \( N_1 \) subsequences of length \( N_2 \) which equals \( N/N_1 \).
2. Use Cooley-Tukey FFT algorithm on each \( N_2 \)-point subsequence recursively.
3. Combine \( N_1 \) subsequences to get the DFT of the original N-point sequence, according to equation 2.

The above \( N_1 \) Cooley-Tukey algorithm reduces the computational complexity to \( O(N_1 N \log_{N_1} N) \). \( \log_{N_1} N \) is the number of major recurrences and \( N_1 \) is the number of operations in each iteration, where \( N_1 \) usually takes the value 2 or 4 to simplify the calculation in traditional implementations of FFT.

\[
X[k] = \sum_{m=0}^{N_1-1} W_N^{mk} X_m[k \mod N_2] \tag{2}
\]

We call step (3) of the original algorithm a merging process for the rest of the paper. It is the core of FFT. The complete FFT algorithm consists of multiple merging processes. The merging process can be expressed in the form of matrix as equation 3. It is rewritten from equation 2 according to the periodicity of \( W_N^{mk} \).

\[
X_{out} = F_{N_1} \cdot (T_{N_1N_2} \odot X_{in}) \tag{3}
\]

where, \( \cdot \) denotes matrix product, \( \odot \) denotes element-wise product. \( X_{out} \) represents the matrix form of the output N-point DFT of the original sequence. The matrix is \( N_1 \times N_2 \) and is shown as follows:

\[
F_{N_1} = \begin{bmatrix}
W_0^{N_1} & W_0^{N_1} & \cdots & W_0^{N_1}
W_1^{N_1} & W_1^{N_1} & \cdots & W_1^{N_1}
\vdots & \vdots & \ddots & \vdots 
W_{N_1-1}^{N_1} & W_{N_1-1}^{N_1} & \cdots & W_{N_1-1}^{N_1}
\end{bmatrix}
\]

\[
T_{N_1N_2} = \begin{bmatrix}
W_0^N & W_0^N & \cdots & W_0^N
W_1^N & W_1^N & \cdots & W_1^N
\vdots & \vdots & \ddots & \vdots 
W_{N_2-1}^N & W_{N_2-1}^N & \cdots & W_{N_2-1}^N
\end{bmatrix}
\]

\[
X_{in} = \begin{bmatrix}
X_0[0] & X_0[1] & \cdots & X_0[N_2-1]
X_1[0] & X_1[1] & \cdots & X_1[N_2-1]
\vdots & \vdots & \ddots & \vdots 
X_{N_1-1}[0] & X_{N_1-1}[1] & \cdots & X_{N_1-1}[N_2-1]
\end{bmatrix}
\]

\[
X_{out} = \begin{bmatrix}
X[0] & X[1] & \cdots & X[N_2-1]
X[N_2] & X[N_2+1] & \cdots & X[2N_2-1]
\vdots & \vdots & \ddots & \vdots 
X[(N_1-1)N_2] & X[(N_1-1)N_2+1] & \cdots & X[N_1N_2-1]
\end{bmatrix}
\]

\( F_{N_1} \) denotes the \( N_1 \times N_1 \) radix-\( N_1 \) DFT matrix. It can fit well in the Tensor Cores when \( N_1 \) is 16. \( T_{N_1N_2} \) is an \( N_1 \times N_2 \) twiddle factor matrix, it has the same size as \( X_{out} \) and \( X_{in} \). \( F_{N_1} \) and \( T_{N_1N_2} \) are shown as follows:

\[
X_{in} \text{ denotes the input } N_1 \text{-point DFT sequences as follows:}
\]

\[
X_{in} = \begin{bmatrix}
X_0[0] & X_0[1] & \cdots & X_0[N_2-1]
X_1[0] & X_1[1] & \cdots & X_1[N_2-1]
\vdots & \vdots & \ddots & \vdots 
X_{N_1-1}[0] & X_{N_1-1}[1] & \cdots & X_{N_1-1}[N_2-1]
\end{bmatrix}
\]
Table 1: Performance of Tensor Cores on V100 and A100.

| Performance | Tesla V100 | Tesla A100 |
|-------------|------------|------------|
| Peak FP64   | 7.8 teraFLOPS | 9.7 teraFLOPS |
| Peak FP32   | 15.7 teraFLOPS | 19.5 teraFLOPS |
| FP16 Tensor Core | 125 teraFLOPS | 312 teraFLOPS |

Figure 1: The complete execution process of tcFFT: First, create a plan based on the dimensions and the size of the input data. This plan selects an optimal set of merging kernels from the pre-implemented merging kernel collection. Then, the execution function is called with the plan and the original data as input. In the execution function, the previously determined merging kernels are executed in turn in multiple iterations. Meantime, multiple types of memory in GPU is fully utilized to increase the reuse of data. After all iterations are executed, the FFT of the original sequence is obtained.

By decomposing the FFT process into a series of merging kernels, we improved the code reusability and also greatly reduced the workload of subsequent performance-related optimization work.

Support FFTs of all power-of-two sizes. We have developed a series of merging kernels of different radices to support FFTs of all power-of-two sizes. The radices of these kernels cover all powers of 2 from 16 to 8192 and larger size FFTs can be realized by combining these basic kernels. Tensor Cores only provide computing power for computing $16 \times 16 \times 16$ GEMM, which can be used in power-of-16 radices. To implement more radices, smaller radices should be introduced. We introduced radix 2 and radix 4, for their DFT matrices only have 0, 1 and -1, and have high computational efficiency. They are computed using FP16 CUDA Cores and account for a small proportion in the total calculation time.

By implementing a collection of merging kernels of a lot of sizes, we enable tcFFT to support FFTs of all power-of-two lengths.

Support batched FFT and 2D FFT. Batched FFT and 2D FFT are of vital importance in application scenarios. 2D FFT performs FFT on each dimension of 2D sequences in turn. It can be implemented by strided batched FFT. Take a 2D FFT on an $N_1 \times N_2$ row-major matrix as an example, an $N_1$ batch of $N_2$-point FFT is applied on the $N_1$ rows and then an $N_2$ batch of strided $N_1$-point FFT is applied on the $N_1$ columns. The order of these two processes can be changed but strided batched FFT is essential.

We have implemented merging kernels that support batch and strided data. Batched FFT and 2D FFT can be implemented by calling them with proper parameters. tcFFT has the following plan functions for batched 1D and 2D FFTs:

- tcfftPlan1D (tcfftHandle *plan, int nx, int batch): This function is used to create a configuration to execute FFT on a batch of 1D sequences of equal length. nx gives the length and batch is the number of sequences.
- tcfftPlan2D (tcfftHandle *plan, int nx, int ny, int batch): This function is used for FFT on batched 2D sequences. nx gives the size of the first dimension and ny is the size of the second dimension. The data are stroed in row-major, which means that the second dimension continues in memory.

These functions can create plans for batched 1D FFT and 2D FFT. They pre-selected a series of optimal merging kernels of different radices for the special size.

3.2 Merging Kernels

Algorithm 1 shows the radix-512 batched merging kernel. It takes $N_1$ groups of data as input. There are 512 FFT sequences of size
Radix-16 sub-merging kernel. Radix-16 sub-merging kernel is the base of tcFFT, because a $16 \times 16$ matrix can fill a Tensor Core fragment, bringing the highest computational efficiency. We treat the $X_{out}$ matrix and the $X_{in}$ matrix as multiple $16 \times 16$ matrices, which can be calculated in parallel. A radix-16 sub-merging kernel can execute a radix-16 merging process described by the equation $X_{out} = F_{N_1} \cdot (T_{N_1} \cdot X_{in})$ from section 2.1. Radix-16 merging process combines FFTs of 16 sequences into an FFT of a sequence of 16 times the length. Strided data layout is also supported, and we will optimize the efficiency of memory accesses in section 4.2.

As shown in line 1-11 in algorithm 1, the sub-merging process firstly loads the radix-16 DFT matrix and calculates twiddle factors while reading input. These matrices are divided into $16 \times 16$ fragments and distributed to the GPU warps for parallelization. Then wraps execute matrix-multiplication with Tensor Cores and element-wise multiplication with FP16 CUDA Cores on these fragments. After that, all fragments are put together, and $N_1 \times 512$ FFT sequences of size $N_2$ are merged into $N_1 \times 32$ FFT sequences of size $16N_2$. Throughout the sub-merging process, intermediate results are stored in the Tensor Core fragments, we will discuss how to manipulate them efficiently in section 4.1.

Combine multiple mergings. The log $N$ merging processes of the FFT algorithm requires log $N$ times of memory accesses, and the arithmetic intensity of an original merging process is not large enough. To reduce the times of global memory accesses and increase the arithmetic intensity, a complete merging kernel consists of multiple sub-merging processes and uses shared memory to exchange data in the middle.

The range of data exchange taking place in the whole FFT process has different scales. Take radix-512 merging kernel as an example, after the first radix-16 merging, each warp can exchange data internally through shared memory, for it holds all the elements needed. This can be done without synchronization. After the second radix-16 merging, data are exchanged between warps also through shared memory, but a block-range synchronization is needed. After the second radix-2 merging, data exchanges between blocks are needed, which can only be done through global memory.

We implemented merging kernels so that global memory accesses are performed only when necessary and only unavoidable synchronizations are introduced. This implementation achieves the purpose of reducing bandwidth requirements and increasing arithmetic intensity.

4 PERFORMANCE OPTIMIZATION

4.1 Optimizations to Tensor Cores

FFT requires complex-matrix access and element-wise multiplication operations. However, they can not be performed efficiently when the data is stored as a Tensor Core fragment due to the limitations of Tensor Core APIs.

The limitations of Tensor Core APIs. NVIDIA provides Warp Matrix Multiply Accumulate (WMMA) APIs for leveraging Tensor Cores to accelerate matrix problems of the form $D = A \cdot B + C$. There are four functions as follows [24]:

- load_matrix_sync: All warp lanes load a matrix fragment from memory, synchronously.
NVIDIA does
A more flexible way to work with Tensor Cores.

fragment (1) First, the data for FFT is usually stored in complex form. There-
in shared memory.

take the fragment element map and the thread ID in a warp as
include which threads in the warp store the element, for exam-
tile stored in this fragment. The numbers in the matrix indi-
and the class
impl. The map of a

A more flexible way to work with Tensor Cores. NVIDIA does
provide a method to access an individual fragment element but
this can only be done uniformly, because we don’t know which

elements are stored in each thread. Prior work has showed some of
these element distributed maps on specific GPU models. However,
these maps differ when fragment parameters change and differ
on different GPU models. So we developed a tool to help obtain
specific maps when needed. The map of a half datatype, 16×16
shape, row-major layout, matrix_b type fragment on V100 is shown
in figure 2. It is used to store tiles from the input data matrix in
tcFFT. The 16 × 16 matrix in the figure represents the matrix tile
stored in this fragment. The numbers in the matrix indicate which
threads in the warp store the element, for example, 16 and 20
in the second row and fifth column indicate that threads 16 and 20
have stored element InFrag2,5. The arrow in the first column
shows the order of elements stored in thread 0, 4.

With the above maps, specified individual fragment element can
be accessed. This individual element access is implemented using
the fragment class member fragment::num_elements and the class member
fragment::x[num_elements]. The first one keeps the num-
of fragment elements in this thread and the second one stores them
in the above order.

Implement FFT’s special operations efficiently. With the
above method, we implemented efficient element-wise multiplica-
tions and complex matrix accesses to accelerate tcFFT. Moreover,
we interleaved these two operations to hide latency.

Algorithm 2 demonstrates this process. The calc_eid function
takes the fragment element map and the thread ID in a warp as
parameters and returns the element id in the matrix tile. Then the
thread can load the element from memory while calculating the

\[
\text{calc_eid} = \text{calc_eid} \times \text{get_twi}(\text{block_start}, \text{warp_start}, \text{eid})
\]

By developing a tool to help find the map of matrix elements into
each thread’s fragment, we extended the programming methods
of Tensor Cores, gained individual fragment element control, and
showed how to use this method to optimize the tcFFT library. The
effect of this optimization is shown and discussed in section 5.

4.2 Alleviate the Memory Bottleneck

Memory can easily become the bottleneck of FFT algorithms on
GPU for two reasons: First, the original log \(N\) merging processes
of FFT algorithm require log \(N\) times of global memory accesses,
and the arithmetic intensity of a single merging is small. Second,
merging processes in FFT require strided memory accesses, and
uncoalesced strided accesses are quite inefficient on GPU. For the
first problem, we have combined multiple mergings when design-
ing tcFFT. This reduces the times of global memory accesses and

\[
\text{merge}_2 = \text{merge}_1 \times \text{InFrag}_n
\]

Figure 2: The map of the input fragment used in tcFFT on
V100: The 16 × 16 matrix in the figure represents the matrix
tile stored in this fragment. The numbers in the matrix indicate
which threads in the warp store the element, for example, 16 and 20
in the second row and fifth column indicate that threads 16 and 20
have stored element InFrag2,5. The arrow in the first column
shows the order of elements stored in thread 0, 4.

Algorithm 2: FFT’s special operations

/* Complex-matrix access and element-wise multiplication in a thread view */

Input: fragment element map

fragment frag_in_real;
fragment frag_in_imag;

for i ← 0 to frag_in_real.num_elements − 1 do

eid ← calc_eid(threadid, i, map);
half2 twiddle ← get_twi(block_start, warp_start, eid);
half2 in_ele ← ln([block_start+warp_start+eid]);
in_ele = cMul(in_ele, twiddle);
frag_in_real.x[i] ← ele.x;
frag_in_imag.x[i] ← ele.y;
end

By developing a tool to help find the map of matrix elements into
each thread’s fragment, we extended the programming methods
of Tensor Cores, gained individual fragment element control, and
showed how to use this method to optimize the tcFFT library. The
effect of this optimization is shown and discussed in section 5.
Trovato and Tobin, et al.

(a) Original out-of-place merging with a fixed data order

(b) tcFFT’s in-place merging with a changing data order; two adjacent butterflies are joined and warps can access memory with continuous size 2.

Figure 3: tcFFT’s in-place and coalesced memory access pattern: the last radix-2 merging process of an 8-point sequence as an example.

Table 2: Achievable Global Memory Bandwidth under Different Continuous Size

| Cont. Sizes | Cont. Bytes | Mem. TP. (GB/s) | BLKs |
|-------------|-------------|-----------------|------|
| 4           | 16          | 208.09          | 8    |
| 8           | 32          | 384.58          | 8    |
| 16          | 64          | 553.48          | 6    |
| 32          | 128         | 836.25          | 3    |
| 64          | 256         | 715.83          | 1    |

increases the arithmetic intensity. For the second problem, we redesigned the data layout and memory access pattern as follows.

In-place computation data layout. We first used an in-place computation data layout before coalescing memory accesses. Merging is an out-of-place process when data is stored in a fixed order in multiple iterations. Figure 3(a) shows the last radix-2 merging process of an 8-point sequence as an example. The upper is the output, and the lower is the input. A pair of output elements is stored with a stride length 4. When implemented on GPU, an out-of-place algorithm requires twice the size of shared memory. This limits the continuous size that can be achieved by coalescing.

tcFFT stores data in a changing order in multiple iterations, figure 3(b) shows the same merging process in tcFFT. It rearranges the original sequence according to parity. This allows the process to be executed in place. This rearrangement is executed recursively in multiple iterations to ensure that all mergings are in-place. The actual rearrangements are based on larger changing radices, although the principle is the same.

Coalesced global memory accesses. After in-place computation is implemented, a merging process includes multiple butterflies as shown in figure 3(b). Memory access in each butterfly is strided, but we can join adjacent butterflies together. In the figure, two adjacent butterflies are joined and warps can access memory with continuous size 2. Actually, in tcFFT, different continuous sizes are used for different radices.

Increasing the continuous size will increase continuity in memory access, but a bigger size makes a kernel use more shared memory and results in fewer concurrent blocks. To achieve higher performance, a proper continuous size is necessary. For radix-256 merging process as an example, the achievable global memory throughputs under different continuous sizes are shown in table 2. From the table, we can find that the achievable memory throughput increases as the continuous size increases when it is no more than 32. It is reasonable for the largest cache line size on GPU is 128 bytes. After that, the bandwidth drops instead. This is because that when the size exceeds 32, the number of concurrent blocks on a streaming multiprocessor reduces to one, and this will make the latency generated by block synchronization unable to be hidden.

5 EVALUATION

5.1 Experimental Setup

Methods. We compare tcFFT with NVIDIA cuFFT which is the state-of-the-art FFT library on GPU. Other GPU FFT libraries are either not open source or slower than cuFFT. The version of cuFFT we used is 11.0 released in Aug. 2020. As of the time of this writing, it is the latest version on our testing DGX-2 platform and DGX-A100 platform. We compare them in terms of accuracy and performance. We show the performance of batched 1D and 2D FFTs of adequate sizes on Tesla V100 GPU and Tesla A100 GPU to evaluate the generalization of our algorithm.

Platform We measured the performance of tcFFT on two platforms, as shown in Table 3, including two generations of NVIDIA GPUs (Volta, and Ampere microarchitectures).

Table 3: Platform Information.

| Platform | Volta | Ampere |
|----------|-------|--------|
| GPU      | Tesla V100 | Tesla A100 |
| CPU      | Intel Xeon 8168 | AMD Rome 7742 |
| OS       | CentOS 7 | CentOS 7 |
| CUDA     | 11.0 | 11.0 |
| Peak FP16 (CUDA Core) | 31.4 TFlops | 78 TFlops |
| Peak FP16 (Tensor Core) | 125 TFlops | 312 TFlops |
| Memory Bandwidth | 900 GB/sec | 1555 GB/sec |

TestCase. In the 1D performance test, we measured batched 1D FFTs of short length, moderate length and long length, from 256 to 134,217,728. For each length, we used a batch size big enough to fully utilize all the Streaming Multiprocessors and Tensor Cores. As for 2D FFT, we measured the six common lengths with adequate batch size. In the follow-up batch size test, we fixed the length, and then measured the performance versus different batch sizes. For
all the tests, the input sequences were generated randomly in the interval -1.0 to 1.0.

**Performance Metric.** In the performance tests, the data are first transferred from CPU to GPU and a plan is created. Then, the `execute function` are executed thousands of times and the average performance is reported. The time spent on the data transferring and plan creating are not counted, for a plan can be reused during the whole life of real applications. We use radix-2 equivalent Trillion Floating Point Operations per Second (TFLOPS) as the Performance metric, because the total number of calculations depends on the specific radix. It can be calculated with equation 4.

\[
TFLOPS = \frac{6 \times 2 \times \log_2 N \times N \times N_{\text{Batch}} \times \text{RepeatingTimes}}{\text{TotalTime} \times 10^{12}}
\]

where \( N \) denotes the length of a sequence and \( N_{\text{Batch}} \) denotes the num of sequences.

**Precision Metric.** tcFFT uses different FFT radices in the divide-and-conquer progress from common FFT algorithms, which influences the result to some degree, so we compare the relative error which is defined as equation 5.

\[
\text{RelativeError}(X) = \frac{1}{N} \sum_{i=0}^{N-1} \left| \frac{X_{\text{double}}[i]}{X[i]} - 1 \right|
\]

where \( X_{\text{double}} \) denotes the sequence calculated by the FFTW library in double precision. It is used as the standard result.

### 5.2 Precision

Table 4 shows the average relative error comparison between our tcFFT and cuFFT in 1D and 2D cases.

|          | cuFFT-1D | tcFFT-1D | cuFFT-2D | tcFFT-2D |
|----------|----------|----------|----------|----------|
| Relative Error | 1.78±0.5% | 1.76±0.5% | 1.65±0.1% | 1.65±0.1% |

Table 4: Average relative error of 1D and 2D FFT, comparison between cuFFT and tcFFT

The above results show that, in bandwidth-bound cases, tcFFT can achieve an average 1.24x speedup. The benefits on A100 are less than those on V100. One reason is that, compared to V100, A100 has 2.5x half-precision computing power but only a 1.7x global memory bandwidth. As a result, optimized FFT algorithm that resorts to more computing power can only bring less performance gain.

**2D FFT.** Figure 5(a) shows the performance of doing FFT of batched 2D sequences on V100. 2D FFT performs 1D FFTs in turn on each dimension of the data. Like cuFFT and FFTW, tcFFT use row-major order to store 2D sequences. This means that the data in the first dimension does not continue in memory and the FFT along this dimension is the main performance factor. When the size of the first dimension is 256, tcFFT is faster than cuFFT by 1.29x on average. And when the first dimension is 512 tcFFT is faster by 3.24x on average. Like long length 1D FFT, mergings along the first dimension require thread synchronizations, so this benefit comes from both improvement in calculation speed and our data arrangement design. Figure 5(b) shows the results on A100, similar to the situation of 1D FFT, performance improvement brought by tcFFT on A100 is also less than than on V100. However, tcFFT is still faster than cuFFT by 3.03x when the first dimension is 512.

The above results show that, in bandwidth-bound cases, tcFFT can use up almost all the bandwidth. And in non-bandwidth-bound cases, tcFFT can outperform cuFFT by a notable margin across different GPU architectures. This significant benefit comes from the extremely high computation power of Tensor Cores and our novel kernel optimizations.

### 5.4 Analysis

Since similar patterns are shown on V100 and A100, we will focus on the results on V100 in the following analysis.

**Benefit of optimizations to Tensor Cores.** We extended the programming methods of Tensor Cores with the fragment storage map, gained element-level control over Tensor Core fragments, and used this method to optimize tcFFT. With element-level control, tcFFT can accomplish element-wise multiplication and complex-matrix accesses without use of shared memory. This greatly reduces the latency of these operations. We shows the performance benefits of this optimization in both figure 4 and figure 5 with Optimized TC label. From the figures, we can find this optimization brings 1.15x-1.32x speedup.

**Benefit of data arrangement redesign.** Figure 6(a) shows the global memory throughput of different size 1D FFTs. In the figure,
we divide the sizes of 1D FFTs into three parts: short, moderate, and long, according to the required stride lengths of memory accesses. FFTs of larger sizes require longer stride lengths and use merging kernels with less computation overlap, so their memory throughput is lower. In short cases, thanks to our redesign of data arrangement and the memory access pattern, the memory throughput of tcFFT is close to the peak global memory bandwidth, and in other cases, tcFFT can outperform cuFFT nearly 2x.
Things are similar in 2D FFT cases. Figure 6(b) shows the global memory throughput of different size 2D FFTs. The elements in the first dimension of 2D FFTs are scattered in the memory. From the figure, we can find that tcFFT obviously exceeds cuFFT in all the cases and when the size of the first dimension increases the performance of cuFFT drops a lot while that of tcFFT almost remains the same.

Performance of small batch sizes. The performance results above are measured with a batch size big enough to fully utilize the GPU resources. Here we give the performance results of smaller batch sizes. Figure 7(a) shows the performance comparison between our tcFFT and cuFFT when transforming batched 1D 131072-point sequences. tcFFT is faster than cuFFT when batch size is larger than 4, and the speedup ratio gradually increases. Figure 7(b) shows the performance of batched 2D 512 × 256 FFTs. tcFFT begins to outperform cuFFT when batch size is 2. This result shows that tcFFT also performs well on small batch sizes.

6 RELATED WORK

Accelerating HPC workload through AI-specific hardware, such as Tensor Cores, has attracted many research efforts. This work is broadly related to the researches under three topics:

Utilizing Tensor Cores for dense linear algebra. Some work utilized Tensor Cores to accelerate dense linear algebra in the performance critical steps [1, 14, 21, 31]. Haidar [13] utilized Tensor Cores to accelerate LU factorization which solves a system of equations. EGEMM-TC [10] used precision recovery GEMM on Tensor Cores to accelerate some scientific applications. Most of the existing work focused on GEMM, convolution, or other dense linear algebra which meet the primitive of Tensor Cores. In contrast, tcFFT exploits Tensor Cores in FFT which is more challenging to be re-expressed with matrix-matrix operators.

Exploiting Tensor Cores in FFT. Sorna [29] and Cheng [7] gave the theoretical basis of using Tensor Cores in FFT and their example implementation resorted to cuBlas to utilized Tensor Cores. But the performance of their implementation was far inferior to cuFFT. Durran [9] has proposed an optimized 1D FFT algorithm in their poster. Their implementation with Tensor Core WMMA APIs outperformed cuFFT and used shared memory to improved the arithmetic intensity, but only on the basic small size 1D FFT. They did not deal with the memory bottleneck caused by the unique memory access pattern of large size or multidimensional FFT, and there is still considerable room for improvement in their method to support FFT’s special operations. Different from prior work, our experimental results show that tcFFT can achieve higher performance than cuFFT in 1D and 2D FFT of universal sizes.

Implementing distributed FFT on Heterogeneous System. Several approaches have been proposed for large size distributed FFT on heterogeneous systems. Some work, like PFFT [27] and P3DFFT [26], focused on how to implement distributed FFT in the highly efficient and scalable way. heFFTe [2, 3] built a multi-node communication model for distributed FFT and achieved more than 2× speedup for the whole FFT computation. Their work focuses on the optimization of communication between computing nodes, and tcFFT can be integrated to accelerate the FFT on each node.

7 CONCLUSION

We design and implement tcFFT which utilizes Tensor Cores to accelerate half-precision FFT in both 1D and 2D forms of various sizes. And we exploit a set of optimizations to efficiently support FFT’s special operations and to alleviate memory bottleneck. We evaluate tcFFT and the NVIDIA cuFFT in various sizes and dimensions on the latest two generations of NVIDIA GPUs, V100 and A100. The results show that our tcFFT can outperform cuFFT 1.29x-3.24x and 1.10x-3.03x on the two GPUs, respectively. tcFFT shows a great potential to use this AI-specific hardware to accelerate FFT and the methods of tcFFT can be generalized to higher precision on higher precision Matrix Operation Units.

We have identified three major avenues for future work. First, the current version of tcFFT achieves a significant performance improvement, while it only supports half-precision. Follow-up efforts can be made to support higher precision on higher precision Matrix Operation Units; Second, tcFFT has no consideration of precision recovery. We will try to introduce some precision recovery algorithms to improve the precision of tcFFT on low precision Matrix Operation Units; Finally, as tcFFT can provide a significant speedup,
we will use tcFFT in some real-world scientific applications to further confirm that tcFFT can extend the usage of Tensor Core in scientific computing.

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