TEM analysis of Si-passivated Ge-on-Si MOSFET structures for high performance PMOS device technology

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Abstract. In this paper, we present a transmission electron microscopy analysis of novel Ge-on-Si MOSFETs using a JEOL 2010F and an aberration-corrected JEOL 2200FSC. A key feature of these devices is the incorporation of a very thin (~1 nm) Si passivation layer on top of the Ge virtual substrate, which is partially oxidised to form SiO₂ (~0.5 nm) prior to depositing HfO₂ dielectric. We will show that the thin SiO₂ layer is not purely amorphous but has some degree of crystal ordering due to being bonded to crystalline materials. Moreover, we will examine the presence of small monolayer variation in Si/SiO₂ interface roughness.

1. Introduction
In recent years, there has been an increased drive to incorporate strained Ge into conventional Si-based complementary metal-oxide-semiconducting (CMOS) device structures. The effects of such pseudomorphic straining are to enhance carrier (hole) mobility in these types of devices [1].

One particular set of device structures that have been investigated are Ge-on-Si MOS field-effect-transistors (MOSFETs). Here, a relaxed layer of pure Ge, or Si₁₋ₓGeₓ, with high Ge content x, onto a (001) Si wafer to produce a Ge-on-Si virtual substrate (VS) and MOSFET devices can then be processed onto these wafers [2]. One of the issues associated with fabricating devices onto these wafers is the need to form, on the wafer surface, a stable dielectric prior to fabricating the gate electrode. One of the drawbacks of Ge-based devices, however, relates to the poorer thermal oxide quality compared with that of Si, which has been found to give rise to a higher interface trap density [3]. Methods have been developed, therefore, to reduce this through Ge passivation [4]. One possible route for such passivation involves depositing an ultra-thin epitaxial Si layer on the surface of the Ge substrate which is then partially oxidised, prior to the growth of a high-k gate dielectric [4]. Issues to be considered, however, relate to the uniformity of the Si/SiO₂ interface, as roughness can lead to carrier scattering, and also whether Ge segregation during growth of the epi-layer will affect passivation and consequently the interface trap density [5].
In this paper, we present a TEM/STEM analysis of MOSFETs on a Ge-on-Si VS. Such devices incorporate a narrow partially oxidised Si passivation layer onto which MOSFET devices are processed. As device dimensions shrink to the sub-nm level, it is necessary to perform analysis at even higher resolution using aberration corrected microscopy techniques.

2. Experimental Details

Ge p-MOSFETs were fabricated using a silicon-compatible process flow on (001) Si wafers with a thick (~2µm) relaxed Ge layer grown on the surface. After the p-well and channel implants, the Ge-on-Si wafer was passivated by growing a thin epi-Si layer (~1nm) which was then partially oxidised at room temperature in a water bath with ozone; see [4]. To avoid further oxidation, a thin layer of HfO$_2$ (~4nm) was then deposited by atomic layer deposition onto the SiO$_2$ before growing the TaN (~10nm) and next the TiN (~70nm) metal layers. The remaining processes, i.e. the dry metal gate etch, As halo’s, BF$_2$ extension implants, spacer definition, B implant, NiGe formation in source and drain regions and metal contact fabrication are all detailed elsewhere [6].

The processed wafers include a narrow region of device lines of MOSFETs of various gate lengths which could be processed into TEM specimens. [110] cross-sectional specimens for TEM, were prepared in the usual manner with 3mm disks thinned mechanically to ~30-40µm followed by Ar$^+$ ion thinning to electron transparency. Finished specimens were then analysed using a JEOL 2010F field-emission gun instrument, operating at 197kV, and equipped with a Gatan imaging filter and STEM analysis using bright-field (BF) and annular dark-field (ADF) detectors. Specimens were also analysed using a double aberration corrected JEOL 2200FSC microscope operating at 200kV.

3. Results and Discussion

The low magnification image in Figure 1(a) provides an overview of the MOSFET device structures. The thickness of the Ge VS is 1.63µm and the surface is uniformly flat. These particular devices have a 325nm gate length and are spaced ~160nm apart. A higher magnification BF STEM image is shown in Figure 1(b), and shows the various components which make up the device structure. The dark layer at the base of the gate electrode is the heavy TaN layer (~14nm) under which are the HfO$_2$ (3.6nm) and SiO$_2$ (0.5nm) gate dielectrics. On top of this is a TiN (~70nm) metal electrode above which is a SiO$_2$ ‘hard mask’. In the source and in the drain regions, the NiGe (~12nm) is clearly visible.

![Figure 1](image.png)

Figure 1. (a) Low magnification BF STEM image of device structures on Ge VS; (b) higher magnification BF STEM image with architecture of device defined; (c) even higher magnification image of side-wall spacer and NiGe of larger gate length device.

An even higher magnification BF STEM image of the edge of a large device is provided in Figure 1(c). Here, the Si$_3$N$_4$ + SiO$_2$ side-wall-spacer (SWS) is visible with dimensions of ~55-60nm wide and ~150nm high. The important region in terms of device performance is the passivation and dielectric region beneath the gate electrode (region boxed in Figure 1(b)) which we will now focus upon.
The dielectric region, of a shorter gate-length device, was imaged using planar illumination under HREM conditions, using a JEOL 2010F microscope, and is shown in Figure 2(b). One feature of the present device structures is the incorporation of a Si passivation layer grown on top of the Ge VS. This is partially oxidised to form a very thin SiO$_2$ layer, which (from Figure 2(b)) was measured to be 0.5±0.2nm, in line with previous estimates [2]. A closer examination of this image shows that the SiO$_2$ layer is bounded by the crystalline Ge/Si VS and the crystalline HfO$_2$ layer which seem to have a common set of lattice fringes across the SiO$_2$. This would suggest that the SiO$_2$ layer is not purely amorphous but instead has some degree of crystalline order due to the fact that it is so thin and is bonded on each side to crystalline materials. Indeed, from Figure 2(b) there appear to be lateral regions within the SiO$_2$ layer which exhibit some degree of crystallinity such as that marked (x). Fourier transforms of the crystalline HfO$_2$ and Ge VS were obtained to determine lattice spacings and orientations, and these are shown in Figures 2 (c) and (d), respectively. From these, {111} lattice spacings of 0.305nm (HfO$_2$) and 0.336nm (Ge) were measured. Also, there seems to be an orientational relationship between the HfO$_2$ and the Ge VS where $d_{111}$(HfO$_2$) is near parallel to $d_{111}$(Ge).

It is difficult to confirm the presence of the residual unoxidised Si from the phase contrast image in Figure 2(b). An attempt was made, therefore, to determine the presence of a residual Si layer by ADF (Z-contrast) imaging, and such an image is shown in Figure 2(a). The width of the dark region indicated corresponds to the sum of the thicknesses of the residual Si and SiO$_2$ layers (1.2±0.2nm). Hence, a comparison of these images shows that the thickness of the residual Si passivation layer is 0.7±0.3nm, again in line with previous estimates [2]. However, the point resolution of the JEOL 2010F is 0.19nm, which is insufficient to resolve individual monolayers of spacing $d_{004}$=0.14nm in Ge.

We have then performed HREM experiments using a JEOL 2200FSC aberration corrected instrument, to look in more detail at the morphology of the Si/SiO$_2$/HfO$_2$ regions. A high resolution image obtained from a similar region to that shown in Figure 2(b) is shown in Figure 3(a). For this, the spherical aberration ($C_s$) was set to −3µm and images were obtained in overfocus so that atomic columns in thin regions appear with positive contrast (white on black), as opposed to classical Scherzer conditions [8]. The beam tilt coma was corrected to ~20nm amplitude and all other aberrations were near their optimum for this instrument to give a uniform phase plate up to an angle of ~30mrad, which corresponds to an information transfer out to $(0.08$nm)$^{-1}$ in reciprocal space. From the image in Figure 3(a), the Ge dumbbells are clearly resolved at 0.14nm spacing and a Fourier transform of the image (Figure 3(b)) shows the presence of the {551}Ge reciprocal lattice position (circled), confirming information transfer out to 0.08nm.

An examination of the Si/SiO$_2$ boundary shows that there is monolayer scale roughness. Bi-layer step edges appear at positions (A)-(D) indicated, demonstrating a non-uniform variation in the Si passivation layer thickness. The origin of such roughening is still unclear; however, it may be due to the fact that the Ge VS surface exhibited small scale roughness or surface undulations prior to
deposition of the Si passivation layer. Oxidation of this layer may therefore lead to a Si/SiO$_2$ interface which displayed some degree of roughness. This, of course, has implications on device performance where enhanced roughness of this boundary may contribute to greater carrier scattering at high source/drain bias.

One further concern is whether there is any Ge present within the residual Si and SiO$_2$ layers. It is known that during growth, Ge may segregate from the surface of the Ge substrate through the epitaxially grown Si passivation layer [7] and may be incorporated into the processed SiO$_2$ layer, or accumulate at the lower Si/SiO$_2$ boundary by ‘snowploughing’. However, verifying this is difficult since the layers concerned are extremely narrow. Further work is in progress to determine the Ge distribution more precisely, using the JEOL 2200FSC instrument in ADF-STEM mode.

4. Conclusions
Ge-on-Si MOSFET structures have been analysed using TEM-based techniques using two different electron microscopes; a JEOL 2010F and a double aberration corrected JEOL 2200FSC. The latter instrument confirmed an information transfer of 0.08nm in one direction and resolved monolayer dumb-bells in Ge of 0.14nm spacing. A feature of the present device structures was the use of Si passivation which required the deposition of a very thin epi-layer of Si (1nm) on the Ge-on-Si wafer, which was then partially oxidised. High resolution TEM images showed that the thin SiO$_2$ layer is not likely to be purely amorphous but instead has some degree of crystalline ordering due to it being only a few monolayers wide and bonded on each side to crystalline materials. Moreover, the Si passivation layer exhibits monolayer scale roughness which could impact on device performance through enhanced interface roughness scattering. Our results confirmed Si passivation with the residual Si passivation layer being 0.7±0.3nm and the SiO$_2$ layer thickness 0.5±0.2nm.

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