A Gb/s Parallel Block-based Viterbi Decoder for Convolutional Codes on GPU

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Abstract—In this paper, we propose a parallel block-based Viterbi decoder (PBVD) on the graphic processing unit (GPU) platform for the decoding of convolutional codes. The decoding procedure is simplified and parallelized, and the characteristic of the trellis is exploited to reduce the metric computation. Based on the compute unified device architecture (CUDA), two kernels with different parallelism are designed to map two decoding phases. Moreover, the optimal design of data structures for several kinds of intermediate information are presented, to improve the efficiency of internal memory transactions. Experimental results demonstrate that the proposed decoder achieves high throughput of 598Mbps on NVIDIA GTX580 and 1802Mbps on GTX980 for the 64-state convolutional code, which are 1.5 times speedup compared to the existing fastest works on GPUs.

Index Terms—CUDA, convolutional codes, Viterbi algorithm, parallel decoding, SDR.

I. INTRODUCTION

The convolutional codes are widely used in digital communication systems to correct the transmission errors, which have been adopted by almost all advanced wireless communication standards. There are strong requirements to develop high performance decoding components with good scalability and reconfigurability to support various standards, which can be applied to new radio communication systems such as the Software Defined Radio (SDR) and Cognitive Radio (CR). As the Viterbi algorithm [1] is the most popular method for decoding convolutional codes, our discussion focuses on the techniques of Viterbi decoder implementations.

Traditional communication systems mainly use Field-Programmable Gate Array (FPGA) and Application Specific Integrated Circuit (ASIC) in hardware platforms. Enormous researches of the Viterbi decoder implementation are based on FPGA/ASIC and Gb/s throughput is achieved [2] [3]. However, these high performances are always along with expensive cost and long development cycle, and these techniques can not provide the flexibility required by SDR or CR systems. Alternative microprocessors like Central Processor Unit (CPU) are more flexible than FPGAs/ASICs. Some works on CPU-based software decoding use single-instruction multiple-data (SIMD) instruction sets to achieve parallel decoding [4] [5]. But restricted by their computation resources, the data processing speed and decoding throughputs are much lower.

High performance computing (HPC) on GPUs is developed rapidly over the last decade. Compared with FPGAs/ASICs, GPU-based implementations have very good flexibility and scalability using high-level programming language. Compared with CPUs, GPUs have more massive ALU cores to ensure large-scale parallel execution, which can gain higher throughput with appropriate optimization. A lot more works have focused on GPU-based decoding in recent years. [6] [7] [8] [9] [10] use CUDA to design Viterbi decoders for SDR systems on NVIDIA GPUs. [11] uses opening computing language (OpenCL) to achieve accelerating Viterbi decoding on an AMD GPU. However, most of these works just simply design a parallel decoder for block-coded convolutional codes, and basic level of optimizations are presented. Compared with these works, a better parallel Viterbi decoding algorithm with lower computational complexity is proposed in this paper. Fine-grained and coarse-grained parallelism optimizations are both presented, to maximize the execution efficiency of mathematical operations, memory transactions and data transfer between the host and the device. The good generality means our parallel block-based Viterbi decoder can work for most kinds of convolutional codes, and some optimizations can also be adopted to implementations of other GPU-based decoders.

II. THE VITERBI DECODING ALGORITHM

The Viterbi algorithm (VA), a maximum likelihood sequence estimator, uses the trellis to exhaustively search the sequence that is closest to received bits from channel. It consists of two procedures in two directions: the forward procedure and the traceback procedure. Three kind of units will be calculated: the path metric (PM), the branch metric (BM) and the survivor path (SP). BM is calculated to measure Hamming/Euclidean distance from the received bits to the legal codewords at each stage. PM is the accumulated distance added by BMs. SP takes a record of the path with minimum distance to each state. Forward computing starts at stage 0 with all metrics set to zero. For each state at current stage, an add-compare-select (ACS) operation is carried out to update their PM at next stage and rewrite their SP relatively. The ACS operation can be described by equation [1]. $PM_n^i$ denotes the path metric of state $i$ at stage $n$. $BM_n^{i,j}$ denotes the branch metric from state $i$ at stage $n - 1$ to state $j$ at stage $n$. $PM_n^{i-1}$ and $BM_n^{i,j}$ are added up for all state $i$ connected to state $j$ and a minimum result is chosen to update $PM_n^i$.

$$PM_n^i = \min_j \left( PM_n^{i-1} + BM_n^{i,j} \right) \quad (1)$$
While the forward ACS computing finishes at the end of the data stream, a state with minimum PM should be estimated as the beginning of traceback procedure. The selected state $S_E$ is believed to be the true encoding tail state with high probability. Therefore, the traceback process goes along the final survivor path $SP_E$ to obtain decoded bits.

In below sections, the $(R, 1, K)$ convolutional code with code rate $1/R$ and constraint length $K$ is concerned. The number of states is denoted by $N$.

III. Proposed GPU-based Decoder and Methods for Efficient Decoding

A. Parallel Block-based Viterbi Decoder

The original VA is not suitable to decode the convolutional codes encoded in a stream, as a huge amount of storage resource would be required and high decoding latency would not be acceptable. Thus, we propose a parallel block-based Viterbi decoder (PBVD) based on the GPU architecture.

Fig.1 shows a schematic of the decoding procedures using PBVD. A real-time constraint is introduced into the decoding procedure. A data segment from stage $t - M$ to $t + D + L$ called a parallel block (PB) consists of a truncated block, a traceback block and a decoding block. Assuming that the block to be decoded starts at stage $t$, with the length of $D$, the PBVD should start at stage $t - M$. A forward ACS procedure is carried out with unknown initial state metrics (typically set to zero). The ACS operation goes through stage $t - M$ to $t + D + L$ and survivor paths with length of $M + D + L$ are estimated and stored, so as the PMs for each state. At the end of the interval, a traceback procedure starts from a random state (state $S_0$, for example). After L times traceback along a randomly picked survivor path, state $S_E$ is reached and regarded as the authentic state at stage $t + D$. Afterwards, traceback procedure would continue and the data segment from stage $t$ to $t + D$ is decoded.

Unlike the original VA, there is no state estimation between forward and backward procedure in PBVD. That means the shortest path would not need to be picked out as the unique selection for backward decoding. This simplification benefits from the traceback block, which provides $L$ stage for all survivor paths merging to an authentic state at stage $t + D$. The length $L$ is called decoding depth and typically equal to $5K$ [12]. Similarly, by a number of $M$ iterations on the truncated block, the truncation error due to the unknown initial metrics is negligible. Thus, the strong probability of successful decoding for the mid block is guaranteed.

To decode a stream of convolutional codes, the input data could be blocked to a series of segments of length $D$. Each segment extends a length of $L$ in both sides as the truncated block and traceback block, to form a parallel block ($M$ is set equal to $L$ in the following description), so the biting length for adjacent PB is $2L$. To achieve high decoding throughput on a GPU, these $N_t$ PBs should be decoded concurrently by two individual GPU kernels (denoted by K1 and K2) with different parallelism to match the different computational complexity of procedures in two directions. Each PB should be successively handled by GPU thread cluster in K1 and K2, which are named virtual processors (VP). After synchronization, the outputs of all VPs in K2 are finally gathered to form the decoded stream. An example of the design for stream decoding using GPU-based PBVD with $N_t = 4$ is shown in Fig.2

B. Optimized Parallelism for Forward ACS Computation

Typically, the commonly used schemes for the forward ACS operations are the state-based parallel execution [8] and the butterfly-based parallel execution [10]. In this paper, a group-based parallel scheme is proposed by exploiting the characteristics of the trellis, to reduce the amount of branch metric computation in the forward procedure.

For a $(R, 1, K)$ convolutional code, the state in the trellis is defined by the contents of the $v$ binary memory cells $D_{v-1} − D_0$ in the encoder, which can be denoted by $S_d$ and $d = (D_{v-1}D_{v-2} \cdots D_1D_0)/2$. There are $R$ filters in the encoder, the $r$th of which has impulse response $g^r(r) = [g^{(r)}_{K-1} \cdots g^{(r)}_0]$, called the generator polynomials. $c(S_d, x) = [c(1)^{(r)}c(2)^{(r)} \cdots c(R)^{(r)}]$ is used to express the encoder output corresponding to input bit $x$ at state $S_d$. $c(r)$ is the output of the $r$th filter, 0 or 1, which can be calculated by:

$$c(r) = (x \cdot g^{(r)}_{K-1} \oplus (D_{K-2} \cdot g^{(r)}_{K-2}) \oplus \cdots \oplus (D_0 \cdot g^{(r)}_0)) \ (2)$$

All operations $\oplus$ are module-2 additions in field GF(2). Consider a butterfly structure from the trellis, the contiguous
states \( S_{2j} \) and \( S_{2j+1} \) in th\( b \) butterfly \((j = 0, 1, 2, ..., N/2 - 1)\) would like to shift to the states \( S_j \) or \( S_{j+2} \) for different input bits. \( \alpha \) and \( \beta \) denote the output of encoder at state \( S_{2j} \) with input bit \( x = 0 \) and \( 1 \) respectively. So as the \( \gamma \) and \( \theta \) for state \( S_{2j+1} \). The \( r \) th bit \( \alpha(r) \) in \( \alpha = [\alpha(1), \alpha(2), ..., \alpha(R-1), \alpha(R)] \) can be obtained by:

\[
\alpha(r) = e^{(r)}(S_{2j}, 0) = (x \cdot g_{K-1}^{(r)}) \oplus (D_1 \cdot g_1^{(r)}) \oplus (D_0 \cdot g_0^{(r)})
\]

\[
= (0 \cdot g_{K-1}^{(r)}) \oplus (D_1 \cdot g_1^{(r)}) \oplus (0 \cdot g_0^{(r)})
\]

\[
= (D_{K-2} \cdot g_{K-2}^{(r)}) \oplus (D_1 \cdot g_1^{(r)})
\]  

(3)

Similarly, \( \beta(r), \gamma(r) \) and \( \theta(r) \) can be obtained as follows:

\[
\beta(r) = e^{(r)}(S_{2j}, 0) = g_{K-1}^{(r)} \oplus \alpha^{(r)}
\]

\[
\gamma(r) = e^{(r)}(S_{2j+1}, 0) = \alpha^{(r)} \oplus g_0^{(r)}
\]

\[
\theta(r) = e^{(r)}(S_{2j+1}, 0) = g_{K-1}^{(r)} \oplus \alpha^{(r)} \oplus g_0^{(r)}
\]  

(6)

From equation (3) to (6) we can conclude that for given generator polynomial pair, once the \( \alpha \) is established, other outputs \( \beta, \gamma \) and \( \theta \) in the butterfly would be uniquely derived. Therefore, all the \( N/2 \) butterflies in the \( N \)-state trellis can be classified to \( 2^R \) (denoted by \( N_c \)) groups. The groups are distinguished by \( \alpha \), which means that butterflies in the same group have the same branch metrics at one stage. As a result, for the \( N/N_c \) states in the same group, only four branch metrics need to be calculated, to update the \( N/N_c \) path metrics. Thus, the total computation of branch metrics for all the ACS operations at one stage can be calculated as \( 2^{K+2} \). For the widely used convolutional codes which have \( R = 2 \) and \( K = 5, 7, 9 \), or \( R = 3 \) and \( K = 7, 9 \), the forward ACS operations can be accelerated due to lower computation of branch metrics than state-based or butterfly-based parallelism scheme \((2^{K+2} < 2^K)\).

IV. FRAMEWORK OF KERNELS AND MEMORY ORGANIZATION ON GPU

A. Kernel Execution and Thread Mapping Strategies

In our GPU-based implementation, two individual kernels K1 and K2 with different thread dimensions are initiated. K1 finishes the forward computing, followed by K2 which carries out the traceback and decoding procedures. To describe the thread organizations in kernels, blockDim and threadDim are used to represent the number of threadblocks and the number of threads in each threadblock. In K1, the group-based parallel execution mode is employed. For the forward computing of a PB, all the \( N \) states will be sorted to \( N_c \) groups using the given criteria. Then for each group, a thread is dispatched to calculate four (or two in special) branch metrics to update all the path metrics and survivor paths at each stage. Thus, \( N_c \) threads are required to build a virtual processor in K1. Considering that 32 CUDA threads are managed cooperatively in batches called a warp, a threadblock in K1 is regulated to accommodate 32 virtual processors. That means the threadDim of K1 is \( N_c \) times the warp size.

In the second kernel K2, as the backward procedure is a completely serial processing that can not be executed in parallel, only one thread is enough to constitute the virtual processor in K2. For convenience narration, we let the threadDim of K2 equal to K1, so that each threadblock in K2 contains \( 32 \times N_c \) virtual processors. If we allocate \( N_{bl} \) threadblocks in K1, the total number of PBs \( N_t \) should be equal to \( 32 \times N_{bl} \). Thus, to handle the \( N_t \) PBs simultaneously, \( N_{bl}/N_c \) threadblocks should be allocated in K2. Inter-frame parallelism and intra-frame parallelism are introduced to indicate the number of virtual processors in each kernel and the number

| Kernel | Thread dimension | Parallelism |
|--------|-----------------|-------------|
|        | blockDim | threadDim | Inter-frame | Intra-frame |
| K1     | \( N_{bl} \) | 32\( N_c \) | 32\( N_{bl} \) | \( N_c \) |
| K2     | \( N_{bl}/N_c \) | 32\( N_c \) | 32\( N_{bl} \) | 1 |

Algorithm 1 Parallel block-based Viterbi decoding algorithm

Kernel 1: Forward procedure

1: for thread block \( b = 0 \) to \( N_{bl} - 1 \), warp \( w = 0 \) to \( N_c - 1 \) and thread \( t = 0 \) to 31 parallel do
2: for stage \( s = 0 \) to \( D + 2L - 1 \) do
3: \( sp = 0 \), \( tid = b \times 32 + t \);
4: Load input symbol and calculate four branch metrics;
5: for all \( j \in Group(w) \) do
6: \( pm_t = PM[2j][t] \), \( pm_{t+1} = PM[2j + 1][t] \);
7: \( reg[j] = \min(pm_t + BM_a, pm_{t+1} + BM_b) \);
8: take a bitwise record in \( sp \) for state \( j \);
9: \( reg[j + 2K - 2]\) = \( \min(pm_t + BM_a, pm_{t+1} + BM_b) \);
10: take a bitwise record in \( sp \) for state \( j + 2K - 2 \);
11: end for
12: Store: \( PM[s][t] = reg[s] \), \( SP[s][w][tid] = sp \);
13: end for
14: end for

Kernel 2: Backward procedure

15: for thread block \( b = 0 \) to \( N_{bl}/N_c - 1 \), warp \( w = 0 \) to \( N_c - 1 \) and thread \( t = 0 \) to 31 parallel do
16: \( i = j = g = \text{state} = 0 \), \( tid = b \times N_c \times 32 + w \times 32 + t \);
17: for stage \( s = D + 2L - 1 \) to \( L \) do
18: Obtain \( i \) by state from lookup tables;
19: for \( g = 0 \) to \( N_c - 1 \) do
20: Load \( SP[s][g][tid] \) and store into \( sp \);
21: end for
22: if \( s \leq D + L - 1 \) then
23: Output decoded bit: \( \text{state} = (\text{state} \gg (K - 2)) \& 0x01 \);
24: end if
25: \( j = \text{state} \times 2^{K-2} \), \( sp = (sp \gg i) \& 0x01 \);
26: \( \text{state} = \times 2 \times j + sp \);
27: end for
28: end for
of threads each virtual processor contains, respectively. Table 1 gives a summary about the thread dimensions and execution parallelism of K1 and K2.

B. Memory Organization for Various Information

In the parallel block-based Viterbi decoder, there are several kinds of data information: (i) the input/output data streams, which can only be stored in the off-chip global memory as they need to be exchanged from the host machine; (ii) the cumulative path metrics and the branch metrics, which are only updated in the forward procedure, so on-chip register resources and shared memory can be used under the conditions of enough capacity; (iii) the survivor paths, which are generated in forward procedure and fetched in decoding phase, that they can only be placed in global memory and designed to meet the alignment requirement for coalesced memory access of two individual kernels.

It is a challenge to design a suitable data structure for the survivor paths due to the different intra-frame parallelism in K1 and K2. Once the coalesced memory access is satisfied in one of the two kernels, the memory transactions in the other kernel would face to horrible inefficiencies. To solve this inconsistency, an optimized construction is exploited in Fig.3. At the current stage, states from 32 PBs are gathered and reordered. All states would be collected to Nc groups followed by the state classification criteria. These Nc groups of states are mapped to different warps allocated in K1. Inside a group, N/Nc states from the same PB are processed in order by the same thread, which means threads with the same threadIdx.x from these Nc warps make up a virtual processor in K1. As the survivor path is a record of selected forward path which can be presented by bit data (for example, bit 0 denotes the upper branch, and bit 1 denotes the lower branch), these N/Nc results can be stored by bit in a same unit as:

\[
SP[x][y][z] = 1101 \cdots 01_{(N/Nc)bits}
\]

As a result, the survivor paths should be allocated as SP[D + 2L][Nc][Nl] to ensure coalesced access for contiguous PBs inside a warp. For each backward stage in K2, Nc individual results are merged because only one warp is needed for the backward phase of these 32 PBs. For a single thread in this warp, all survivor path messages from a PB are loaded with Nc memory requests, but all in the form of aligned transaction. After all, the memory requests in both K1 and K2 are managed without duplicate transactions and extra time overhead.

The shared memory are allocated based on thread blocks and threads with the same threadIdx.x in different warps need to swap data to jointly accomplish the forward phase for a PB. To avoid the bank conflict in shared memory transactions, the data structure should be devised as PM[N][32] to ensure that the accesses for path metrics with the same state id are aligned and fall into individual shared memory banks. As a result, for each shared memory store/load instruction, no transaction for the same request replays and maximum bandwidth utilization is reached. Remarkably, additional registers are necessary as the temporary places to store the updated results for path metrics, and shared memory store transactions would not be carried out until all the calculations at a stage are finished.

C. Asynchronous Data Transfer and Throughput Analysis

The time overhead of data transfer between host and device should be taken into account when evaluating a GPU-based decoder. CUDA supports asynchronous streams technique to achieve the overlap for data transfer tasks and kernel launches in different streams. The decoder should activate a suitable number of CUDA streams and arrange tasks to the idle streams consecutively to ensure the high occupancy of the GPU device.

For our GPU-based Viterbi decoder, the H2D messages are blocked input data streams and D2H messages are decoded bits. A kernel throughput Sk is introduced to evaluate the kernel execution efficiency and it can be obtained by P × Nl, where Tk is kernel execution time. For the H2D data transfer, a parameter U1 is defined to indicate the number of bytes for an input symbol storage. Similarly, a parameter U2 is defined to indicate the number of bytes for the storage of a decoded bit in D2H data transfer. Thus, the time cost of H2D and D2H transfer can be calculated by: 

\[
T_{h2d} = \frac{(D + 2L) \times N_l \times U_1}{B} \quad T_{d2h} = \frac{D \times N_s \times U_2}{B}
\]

where B denotes the PCI-E bandwidth. To hide data transfer latency, Ns CUDA streams can be allocated (in each stream, Nl parallel blocks are arranged). Ideally, all the data transfer batches can be completely hidden by the kernel executions, besides the first H2D batch and the last D2H batch. Thus, the decoding throughput can be approximately calculated by:

\[
\frac{D \times N_l \times N_s}{T_{h2d} + \sum T_k + T_{d2h}} 
\]

\[
= \frac{B \times N_s}{(1 + 2L/D) \times U_1 + N_s/S_k + U_2}
\]

(7)
Notice that the approximation $\sum T_k \approx N_s \times T_k$ can be used, though the concurrent kernel execution (CKE) technique or the Hyper-Q technique in CUDA may be applied.

To improve the decoding throughput, one way is to make the kernels operate efficiently by the approaches in above sections, to achieve a higher $S_k$. Another way is to develop suitable methods of the storage for input/output messages, to reduce $U_1$ and $U_2$. For a soft-decision decoding over the AWGN channel, received symbols should be converted to soft messages and stored by several bits. In fact, a $q$-bit fixed-point quantization scheme can be designed and $[32/q]$ messages can be packed and stored into a same integer unit. As a result, the value $U_1$ decreases from $4R$ to $4R/[32/q]$. For the storage of decoded bits, we can use a similar packing scheme to store each decoded bit by bitwise operations. In this case, a character type can store 8 individual decoded bits that reduce $U_2$ to 1/8.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

The experimentations are carried out on Intel i7-4790k platform with NVIDIA GTX580 (1544MHz, 512 CUDA cores, and PCI-E 2.0 supported) and Nvidia GTX980 (1126MHz, 2048 CUDA cores, and PCI-E 3.0 supported). The program-sare complied with GCC 4.8.2 and CUDA 6.5.

A (2,1,7) convolutional code with generator polynomials $g^{(1)} = [1111001]$ and $g^{(2)} = [1011011]$ is chosen from CCSDS standard [13] for convenient comparison with other works. As the code rate is 1/2, the 64 states can be divided into $2^2 = 4$ groups using the given classification methods, and the result is shown in Table II. The BER performance under AWGN channel for various $L$ are presented in Fig. 4. (D is fixed to 512, which is an less important factor). It is shown that as $L$ rises to 42, which is about 6 times the constraint length, the BER result is approximate to the theoretical performance. Actually, in the proposed decoder, larger $L$ results in better error correction performance, but too large $L$ can cut down the decoding throughput. Thus, $D = 512$ and $L = 42$ are selected for the parallel block in the following tests.

To demonstrate the improvements by using the proposed strategies and methods, experimental results of both the original decoder and the optimized decoder are given for comparison in Table III including the kernel execution times, the data transfer times, the kernel throughput and the decoding throughput. The proposed decoder is operated on different GPU devices with various numbers of $N_{bl}$ and $N_t$. The original parallel block-based Viterbi decoder launches only one kernel to finish the whole decoding procedure. 32-bit float-point quantization is used for the input soft messages, and decoded bits are stored in integers. In the optimized decoder, two kernels with different number of threads are launched and execution times $T_{k1}$ and $T_{k2}$ are recorded individually. It can be seen that the total execution times are reduced significantly by at least 40%, which results in an improvement of kernel throughput $S_k$. Input messages are quantized to 8-bit, which are stored using the packing scheme, and bitwise storage is designed for decoded bits. As a result, the H2D/D2H data transfer sizes are both cut down and $T_{H2D}/T_{H2D}$ are greatly shorted to improve the decoding throughput ($T/P$). To hide data transfer latency, asynchronous transfer technique is adopted and throughput results with three CUDA streams (3S) are presented. By comparing with the performance under the synchronous mode which only uses one CUDA stream (1S), it shows that the more powerful the GPU is, the more efficient overlap and more throughput improvement become. Furthermore, as the increase in the number of concurrently executed parallel blocks $N_t$, the GPU will finally run at full capacity and the decoder will reach the peak throughput.

Table IV shows the decoding throughput comparison between our work and existing works on various GPU platforms, which are all for convolutional codes with code rate 1/2 and constraint length 7. A metric named TNDC (Throughput under Normalized Decoding Cost) introduced in [14] is provided in order to make fair comparison. As the normalized results show, the proposed decoder achieves about 1.5∼9.2 times speedup compared with the existing GPU-based implementations.

In addition, compared with the existing fastest x86-CPU work [5], which runs a 64-state VA decoder on the Intel Core 2 Extreme X9650 (4 cores, 3.0GHz) at the speed of 60Mbps, our results show significant throughput advantages. Compared with the newest results on FPGA platforms, e.g., 865Mbps for a 64-state VA decoder on Stratix III 340 (216MHz) [13] and 10Gbs for a 32-state VA decoder on Xilinx Virtex 7 XC7VX690T-2 [16], our results reach a comparable speed.
and the good scalability and compatibility make it easy to transplant our decoder onto future powerful GPU devices to achieve higher performance.

### TABLE IV

Decoding throughput comparison with existing works

| Work | Device   | T/P(Mbps) | TNDC | Speedup |
|------|----------|-----------|------|---------|
| 0    | GTX275   | 28.7      | ≈0.085 | ×9.20 |
| 1    | 8800GTX  | 29.4      | ≈0.170 | ×4.60 |
| 2    | GTX580   | 67.1      | ≈0.085 | ×9.20 |
| 3    | 9800GTX  | 90.8      | ≈0.420 | ×1.86 |
| 4    | HD7970   | 391.5     | ≈0.207 | ×3.78 |
| 5    | Tesla C2050 | 240.9  | ≈0.468 | ×1.67 |
| 6    | GTX580   | 404.7     | ≈0.512 | ×1.53 |
| This work | GTX980  | 598.3     | ≈0.757 | ×1.03 |
|       | GTX980   | 1802.5    | ≈0.782 | ×1.00 |

### VI. CONCLUSION

This paper introduces a parallel block-based Viterbi decoder. The data stream is divided to a series of parallel blocks for concurrently decoding. Implementation on GPU uses two individual kernels mapping to two decoding phases, and optimized parallelism inside kernels are presented, which are based on the proposed state classification criteria. Aiming to accelerate the decoding, appropriate GPU memory and data structure are developed for intermediate messages. Storage for input/output data are designed and multiple CUDA streams are used to reduce the overhead of data transfer. Experimental results show that proposed GPU-based decoder achieves about 1.5 times speedup than the existing fastest work on GPU. The proposed decoding architecture can be used in the software-defined radio systems, as a flexible Viterbi decoding unit with strong reconfigurable ability.

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