BSIM3 parameters extraction of a 0.35 µm CMOS technology from 300K down to 77K

Laurent Varizat¹, ², Gerard Sou¹ and Malik Mansour²

¹ Electrical and Electromagnetism Laboratory, Pierre and Marie Curie University, 4 Place Jussieu, 75252 Paris Cedex 05, France
² Laboratory of Plasma Physics, CNRS, Ecole Polytechnique, Route de Saclay, 61128 Palaiseau, France
E-mail: laurent.varizat@upmc.fr

Abstract. In this work, we present a commercial 0.35 µm/3.3 V CMOS technology behaviour study of both linear and gate-enclosed transistors from room temperature down to 77 Kelvin. Cryogenic setup used to complete this study is first described. Measurement results are then discussed and a model based on a BSIM3 parameters extraction is proposed.

Keywords: Cryogenic temperature MOSFET; BSIM3 model; Gate-enclosed layout.

1. Introduction
At low temperature, MOSFETs behaviour is modified. Gain and charge carrier mobility modifications as well as thermal noise and parasitic effect reductions are observed. Accurate knowledge of transistors behaviour is essential to design fully integrated instrumentation electronics and to achieve the best performances of integrated circuit in many fields like space instrumentation or nuclear science. Unfortunately, simulation models available from industrial foundries are meant to work only from −40 °C to 150 °C. Previous works have investigated technology behaviours at low temperature. For instance, in [1] an evaluation of AMS 0.35 µm CMOS technology to be implemented in Mars landers is presented but the study is not going below 165K. However the knowledge of the transistors behaviour at low temperature is required for many other space applications for which cryogenic environment can help improving performances [2,3] by:

- Increasing speed due to the increase charge transport properties
- Reducing interconnect resistance
- Decreasing the thermal electrical noise
- Reducing parasitic effects and thus improving reliability regarding latch-up, leakage currents of electromigration
- Increasing gain

2. Setup and methods
A dedicated test bench has been developed to characterize electrical transistors properties at cryogenic temperature. A test device composed of both PMOS and NMOS transistors with...
different sizes and geometries was designed. Table (1) lists the transistors geometries indexed into four main domains.

| Type     | Size (W x L)    | Layout architecture |
|----------|-----------------|---------------------|
| NMOS     | 50 µm x 0.35 µm | Linear              |
|          | 50 µm x 10 µm   | Linear              |
|          | 1000 µm x 10 µm | Linear              |
|          | 50 µm x 0.35 µm | Gate-enclosed       |
|          | 50 µm x 10 µm   | Gate-enclosed       |
|          | 1000 µm x 10 µm | Gate-enclosed       |
| PMOS     | 50 µm x 0.35 µm | Linear              |
|          | 50 µm x 10 µm   | Linear              |
|          | 1000 µm x 10 µm | Linear              |
|          | 50 µm x 0.35 µm | Gate-enclosed       |
|          | 50 µm x 10 µm   | Gate-enclosed       |
|          | 1000 µm x 10 µm | Gate-enclosed       |

Table 1: List of transistors used for characterisation.

For each size, both linear and gate-enclosed transistor geometries have been studied. Gate-enclosed transistors [4] show a better resistance to ionising radiation which is an asset for space applications. This design removes gate’s edges and reduces leakage currents due to the bird’s beak effect [5]. Figure (1a) shows the layout of a linear NMOS 50µmx10µm while figure (1b) shows the equivalent gate-enclosed transistor.

2.1. Cryogenic setup

Figure (2) shows the cryogenic test bench. The circuit under test is inserted inside a cryostat immersed in a liquid nitrogen tank. Vacuum is maintained inside the cryostat to prevent air condensation and freeze on the device. A metallic frame is used to keep the cylinder in place during measurements. The cryostat immersion depth in the liquid nitrogen tank is controlled thanks to a micro-controller and a PT100 thermistor positioned on the device side. During
measurement the desired temperature is set by moving the cryostat up and down. This setup allows to do measurements at different temperatures from room temperature down to 77K.

Figure 2: Cryogenic test bench.

2.2. Extraction tools
A DC generator is used to supply the device while a semiconductor analyser\(^1\) performs current-voltage and capacitive measurements. Capacitive measurements shown on figure (3) allow data extraction of following parameters:
1. BD’s junction;
2. Gate oxide;
3. Intrinsic capacities;
4. Overlap effect;
A voltage sweep is performed from \(-0.3V\) to \(3.6V\) with a \(0.1V\) step between \(Hi\) and \(Lo\) terminals (fig (3)). All instruments are controled by IC-CAP\(^2\) software controls. Measurement points are corrected from the parasitic resistances of the drain and the source according to the temperature [6]. BSIM3v3 model parameters are extracted for each transistor category with IC-CAP using a precise extraction flow. An optimisation phase is then performed to improve the model’s precision using Levenberg-Marquart algorithm which presents the best performance compared to other available algorithms.

3. Thermal study
To obtain a valid model describing the transistors behaviour around 100K, characteristics have been measured at 77K, 100K, 150K, 200K and 300K as a comparison.

\(^1\) Keysight\(^\text{TM}\) B1500A Semiconductor Device Analyser
\(^2\) Keysight\(^\text{TM}\) Technologies : http://www.keysight.com/
3.1. Current-voltage measurements

Foundry model is meant to work from $-40 \, ^\circ C$ to $150 \, ^\circ C$. Figure (4) shows a transistor drain current temperature dependency for a given size and polarisation. On the same graph are plotted the foundry model simulation, the measurements and the extracted model. Below $-40 \, ^\circ C$ a divergence between measurement and foundry model is observed. This divergence is growing as the temperature decrease so that around 100K the foundry model can not be used anymore.

One of the most important temperature dependant parameter is the threshold voltage.
Threshold voltage $V_{th0}$ defines the gate polarisation voltage split between two transistors states. Before threshold voltage, the transistor is in off mode, corresponding to a low current from drain to source. Conversely, after threshold voltage, the transistor is in linear or saturate mode. Table (2) shows the threshold voltage variation with temperature. The absolute value of the threshold increases as the temperature decreases. This implies that for cryogenic temperature, the lowest transistor polarisation has to be greater than at room temperature. For PMOS transistors, a drift of half a volt is observed from room temperature down to 77K and reaches the value of $-1.2V$.

|       | 300K | 200K | 150K | 100K | 77K |
|-------|------|------|------|------|-----|
| NMOS  | 0.5V | 0.58V| 0.66V| 0.72V| 0.76V |
| NMOS HR| 0.39V | 0.4V  | 0.49V |       |      |
| PMOS  | -0.7V | -0.9V | -1.0V | -1.2V| -1.2V |
| PMOS HR| -0.86V | -0.89V | -1.1V |       |      |

Table 2: $V_{th0}$ temperature dependence for different types of transistors.

Furthermore, silicon conductance is modified and evolves conversely to the temperature as shown on figure (5) by the output conductance curves, $g_{ds}$, which quantify the drain current variation with a drain-source voltage variation while keeping the gate-source voltage constant (1).

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{GS}}$$

Figure 5: $G_{DS} = f(V_{DS}, T)$ for a 50 $\mu$m $\times$ 10 $\mu$m NMOS.

3.2. Capacitive measurements
Capacitive measurements are useful to extract physical parameters of BSIM3’s model. Figure (6) shows the capacity between the gate and drain-source-bulk in function of its polarisation. Besides a slight offset due to $V_{th}$ drift no significant difference in capacitive measurements between 300K and 77K is observed.
3.3. Physical interpretation: freeze-out effect
The diminution of temperature provokes an increase in electron’s mobility which is observed by
an increase of the drain current. In the meantime, there is a diminution on charge carrier density
with temperature [7]. When the density is too low, a drop in transistors current is observed.
This well known freeze-out effect corresponds to a charge carrier gel and depends on the doping
concentration. Figure (7) shows the electron density according to the temperature. The dots
correspond to the electron density and the Fermi energy at 77K. The electron density decreases
about two order of magnitude from 300K to 77K. As a result the current flowing in transistors
decreases rapidly according to the temperature.

Figure 7: Electron density evolution with temperature and the corresponding Fermi energy.\(^3\)
4. BSIM3 parameters extraction

BSIM3 model [8] does not take into account low temperature physical effect like the freeze-out effect. Whereas some works present new models in order to take the freeze-out effect into account [2,9], we have adjusted BSIM3 physical parameters to bypass this lack. Figure (8) shows $I_DV_G$ and $I_DV_D$ curves between measurements and simulations based on extracted model at 100K. Both simulations and measurements are in good agreement.

![Figure 8: $I_DV_G$ and $I_DV_D$ measurements (dots) and extracted model simulations (lines) from a standard 50 $\mu$m × 10 $\mu$m NMOS at 100K.](image)

5. Conclusion

We presented a cryogenic study of a commercial standard 0.35 $\mu$m bulk CMOS technology for both normal and gate-enclosed layout between 77K and 300K. For this purpose, an integrated circuit with transistors, resistors and capacitors of several dimensions and geometries has been designed, as well as a dedicated cryogenic set-up. Current-voltage capacitive measurements and parameters extraction have been performed using IC-CAP (Keysight™) software. As expected, a deviation, growing with decreasing temperature between measurements and foundry based models simulations is observed and is being assigned to physical phenomena, like freeze-out effect. Around 100K, deviation is such that models become unusable for a large variety of integrated circuit design. A model based on a BSIM3 parameters extraction has been proposed. Ready to use Cadence libraries have been developed. Libraries are suitable for the accurate design of cryogenic circuits in a wide temperature range from 300K down to 77K and for given transistor sizes.

References

[1] Ramos-Martos J, Ragel-Morales A, Ceballos-Cerces J, Mora-Gutirrez J M, Lagos-Florido M A and Espejo-Meana S 2012 URL http://digital.csic.es/handle/10261/84095
[2] Zhao H and Liu X 2014 Cryogenics 59 49–59 ISSN 00112275 URL http://linkinghub.elsevier.com/retrieve/pii/S0011227513000969
[3] Yangbo Y, Zhe G and Haisong L 2009 Chinese J. Electronics 18 215

adapted from Bart Van Zeghbroeck equations (1997)
[4] Fan X, Li P, Li W, Zhang B, Xie X, Wang G, Hu B and Zhai Y 2011 *Journal of Semiconductors* **32** 084002 ISSN 1674-4926 URL http://stacks.iop.org/1674-4926/32/i=8/a=084002?key=crossref.0b69fd2af8f7ede9b5f2a54a0c1cb0bf

[5] Oldham T R and McLean F B 2003 Total Ionizing Dose Effects in MOS Oxides and Devices URL http://ntrs.nasa.gov/search.jsp?R=20030032300

[6] Desai P D, James H and Ho C Y 1984 *Journal of physical and chemical reference data* **13** 1131–1172

[7] Street R A 1982 *Physical Review Letters* **49** 1187–1190 URL http://link.aps.org/doi/10.1103/PhysRevLett.49.1187

[8] Sheu B J, Scharfetter D L, Ko P K and Jeng M C 1987 *IEEE Journal of Solid-State Circuits* **22** 558–566

[9] Jia K, Sun W and Shi L 2011 *Journal of Semiconductors* **32** 064002 ISSN 1674-4926 URL http://stacks.iop.org/1674-4926/32/i=6/a=064002?key=crossref.e3cf1a8b488df63b355f9938e0294db