High Performance 3.3 kV SiC MOSFET Structure with Built-In MOS-Channel Diode

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Abstract: Built-in freewheeling diode metal–oxide–semiconductor field-effect transistors (MOSFETs) that ensure high performance and reliability at high voltages are crucial for chip integration. In this study, a 4H–SiC built-in MOS-channel diode MOSFET with a center P+ implanted structure (CIMCD–MOSFET) is proposed and simulated via technology computer-aided design (TCAD). The CIMCD–MOSFET contains a P+ center implant region, which protects the gate oxide edge from high electric field crowding. Moreover, the region also makes it possible to increase the junction FET (JFET) and N-drift doping concentration of the device by dispersing the high electric field. Consequently, the CIMCD–MOSFET is stable even at a high voltage of 3.3 kV without static degradation and gate oxide reliability issues. The CIMCD–MOSFET also has higher short-circuit withstanding capability owing to the low saturation current and improved switching characteristics due to the low gate-drain capacitance, compared to the conventional MOSFET (C–DMOSFET) and the built-in Schottky barrier diode MOSFET (SBD–MOSFET). The total switching time of a CIMCD–MOSFET is reduced by 52.2% and 42.2%, and the total switching loss is reduced by 67.8% and 41.8%, respectively, compared to the C–DMOSFET and SBD–MOSFET.

Keywords: body diode; high breakdown voltage; high reliability; MOS-channel diode; reverse recovery; silicon carbide; switching loss

1. Introduction

Silicon carbide (SiC) is receiving considerable attention as an alternative to silicon for use in next-generation power semiconductors owing to its high thermal conductivity and breakdown voltage resulting from its wide bandgap [1–3]. SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) enable faster switching operations than Si insulated-gate bipolar transistors (IGBTs) [4]. Therefore, several power modules using SiC MOSFET devices that can withstand voltages in the range of 650 V to 1.7 kV have been proposed [5–7]. Research on SiC MOSFETs for applications with a high voltage of 3.3 kV and higher is also being actively pursued [8,9].

SiC Schottky barrier diodes (SBDs) are the most widely used external anti-parallel diodes in power module systems. An SBD has a low diode turn-on voltage, which can reduce the dead time loss; moreover, its unipolar device operation significantly reduces the reverse recovery charge [10–12]. In addition, the switching loss is small even at high temperatures because the reverse recovery charge of the SiC SBD does not depend on temperature [13,14]. However, an additional external SBD requires a large assembly area, which increases the size of the power module system [15]. In addition, an increase in the operating voltage increases the size of the SBD, thus requiring a larger active area [16]. The built-in PIN body diode can be used to reduce the size of the power-module system. However, the high turn-on voltage and bipolar degradation cause conduction loss. Additionally, the high reverse recovery charge and temperature-dependent bipolar operation cause a large switching loss in high-temperature and high-speed switching operations [17,18].

Several methods for embedding a unipolar diode in a MOSFET have been developed to address these limitations. The best-known approach is to embed an SBD within...
a MOSFET [19–23]. Through this approach, the size of the power module system was reduced using the built-in SBD MOSFET while reducing the energy loss through a low turn-on voltage and small reverse recovery charge. However, barrier lowering occurs in the Schottky junction owing to image force, and additionally, the thermionic emission and tunneling process at the lower energy barrier increases the off-state leakage current at high voltage and high temperature conditions of the built-in SBD MOSFETs [24–26].

Embedded polySi/SiC heterojunction diode MOSFETs (HJD–MOSFETs) are designed to reduce the reverse recovery charge of the body diode [27–29]. The HJD–MOSFET operates as a unipolar body diode and the reverse recovery charge can be reduced to a level that is similar to that of the SBD. However, it is not suitable for use at high voltages because of the low critical electric field of polysilicon and the large off-state leakage current due to the interfacial trap charge at the polySi/SiC interface [30,31].

A built-in MOS-channel diode MOSFETs (MCD–MOSFETs) have also been proposed to reduce the diode turn-on voltage and reverse recovery charge of the body diode [32–34]. However, because only one channel is formed in the on state of the MCD–MOSFET, the static characteristics deteriorate, and the low P-base doping concentration causes a reach-through problem at high voltages [35]. In addition, the split gate structure and thin gate oxide film create a large electric field at the oxide edge due to electric field crowding and impair the reliability of the gate oxide film [32,36]. This reduces the stability of the MCD–MOSFET at high voltages.

In this study, a 3.3 kV center-implanted embedded MOS-channel diode MOSFET (CIMCD–MOSFET) was proposed and analyzed via technology computer-aided design (TCAD) simulations. The proposed structure has P+ doping in the center region, which distributes the electric field and reduces electric field crowding at the oxide edge of the MCD–MOSFET. Therefore, the CIMCD–MOSFET operation is stable even at a high voltage of 3.3 kV without the reliability issues resulting from the oxide film. Moreover, the diode turn-on voltage can be further reduced by reducing the oxide thickness of the MOS-channel diode. In addition, the doping concentration of the junction FET (JFET) and drift region can be increased owing to the shielding effect of the central P+ doping region, thereby minimizing the degradation of static characteristics. The simulation results demonstrate that the CIMCD–MOSFET has improved static characteristics, switching characteristics, and short-circuit capability compared with conventional diffusion MOSFETs (C–DMOSFET) and built-in Schottky barrier diode MOSFETs (SBD–MOSFET).

2. Device Optimizations and Methods

Figure 1 shows the cross-sectional views of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. To prevent the reach-through problem, P+ doping was applied to the P-base region of the MCD–MOSFET, except for the channel region [37]. As shown in Figure 1b, it is possible to use the built-in Schottky barrier diode through the Schottky contact in the mesa region of the SBD–MOSFET, compared to the C–DMOSFET. The work function of the SBD–MOSFET was set to 4.33 eV, which is the same as that of titanium [38,39].

As shown in Figure 1c, the CIMCD–MOSFET has a split-gate structure. The right-side split dummy gate is in contact with the source while the left-side split gate is in contact with the gate. When the MOSFET is turned on, a channel is formed in the left P-base and current flows. When the MOSFET is turned off and the diode is turned on, a channel is formed in the right P-base due to the voltage difference between the source and drain and current flows. To reduce the turn-on voltage of the MOS-channel diode, the thickness of Tox$_2$ should be 5 nm, which is much smaller than that of Tox$_1$.

A shielding region was also formed by the P+ doping in the center region of the MCD–MOSFET structure, as shown in Figure 1c. The central P+ shielding region overlaps with the oxide edge below the split gate to directly protect the oxide from the high electric field and prevent field crowding at the oxide edge. In addition, the center-implanted P+ region improves the breakdown capability of the MOSFET by dispersing the high electric
field in the P+ base region, thereby increasing the doping concentration of the JFET and N-drift region. Table 1 summarizes the parameters of the device structure. Figure 2a shows Baliga’s figure of merit (B–FOM) of the CIMCD–MOSFET according to the N-drift doping concentration (N_D) and JFET width (W_JFET). The B–FOM is defined as the square of the breakdown voltage (BV) divided by the specific on-resistance (R_{on-sp}) \cite{40}. The W_{JFET} and N_D are important parameters that affect the R_{on-sp} and BV. The longer the W_{JFET}, the lower the JFET resistance. However, the BV decreases and the cell pitch increases. This decreases the device integration in the active area. Also, the doping concentration of the N-drift increases, and the R_{on-sp} and BV decrease. As shown in Figure 2a, the CIMCD–MOFSET has the highest B–FOM value when W_{JFET} = 1.8 \mu m and the doping concentration of N-drift is 3.5 \times 10^{15} \text{ cm}^{-3}. Figure 2b shows the body diode turn-on voltage V_F that is based on the width of the W_D. A longer W_D improves the diode current flow, decreases the V_F, and decreases the cell density because the cell pitch increases. As the V_F does not change significantly for a W_D length of 1 \mu m or more, it is reasonable to maintain the W_D length at 1 \mu m.

![Figure 1](image)

**Figure 1.** Cross-sectional view of (a) C–DMOSFET, (b) SBD–MOSFET, and (c) CIMCD–MOSFET.

**Table 1.** Device parameters.

| Parameter                  | C–     | SBD–   | CIMCD– |
|----------------------------|--------|--------|--------|
| Cell pitch [\mu m]        | 9      | 10.8   | 10.55  |
| Gate oxide thickness Tox1 [nm] | 50    | 50     | 50     |
| Gate oxide thickness Tox2 [nm] | -     | -      | 5      |
| P channel width [\mu m]   | 0.5    | 0.5    | 0.5    |
| P+ base width [\mu m]     | 3      | 3      | 3      |
| P+ base depth [\mu m]     | 1      | 1      | 1      |
| N-drift thickness [\mu m] | 30     | 30     | 30     |
| N+ substrate thickness [\mu m] | 100  | 100    | 100    |
| W_{JFET} [\mu m]          | 3      | 2.8    | 1.8    |
| W_D [\mu m]               | -      | 1      | 1      |
| W_F [\mu m]               | -      | -      | 1.75   |
| N-drift doping N_D [cm^{-3}] | 2.8 \times 10^{15} | 3 \times 10^{15} | 3.5 \times 10^{15} |
| JFET doping [cm^{-3}]      | -      | -      | 2 \times 10^{16} |
| P+ doping [cm^{-3}]        | 2 \times 10^{18} | 2 \times 10^{18} | 2 \times 10^{18} |
| P channel doping [cm^{-3}] | 2 \times 10^{17} | 2 \times 10^{17} | 2 \times 10^{17} |
| N+ substrate doping [cm^{-3}] | 1 \times 10^{19} | 1 \times 10^{19} | 1 \times 10^{19} |

The simulation results of each device were obtained using the Sentaurus TCAD simulation package. The electron/hole continuity equations and Poisson equations were solved by considering mobility degradation and recombination in the simulation. The Lombardi interface charge model and high-field saturation were applied to the mobility
The Shockley–Read–Hall recombination and Auger recombination models were considered and the Hatakeyama model was applied. In addition, we applied an incomplete ionization model, anisotropic mobility, and bandgap narrowing. Barrier lowering, barrier tunneling, and thermionic emission were considered for the Schottky contacts. Furthermore, the channel mobility was estimated to be 15–20 cm²/V·s through the SiC/SiO₂ interface charge and a thermodynamic model was considered for a high-temperature simulation.

Figure 2. Comparison of the (a) B–FOM characteristics for WJFET and N₂ variation of CIMCD–MOSFET (b) third-quadrant characteristics for different WD of CIMCD–MOSFET.

3. Simulation Results and Analysis

3.1. Static Performances

Figure 3 shows the off-state characteristics of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. They have a breakdown voltage of over 3.3 kV at T = 300 K. At T = 450 K, additionally, the off-state leakage current is high in the SBD–MOSFET compared to the C–DMOSFET and CIMCD–MOSFET. Due to the tunneling effect of electrons in a thermally excited metal, called thermionic-field emission, the reverse leakage current of SBD–MOSFET is highly temperature-dependent. Figure 4 shows the electric field distribution of each device. For improved reliability of the gate oxide film, the maximum electric field E_MOX of the gate oxide is preferably ≤3 MV/cm. In Figure 4a,b, the E_MOX of the C–DMOSFET and SBD–MOSFET is approximately 3 MV/cm at V_DS = 3 kV. The MCD–MOSFET without the center implant region applies a large electric field of 7.45 MV/cm to the oxide edge, even at V_DS = 2 kV (Figure 4d). A large electric field across the thin gate oxide causes a large off-state leakage current due to tunneling and causes premature breakdown at low voltages. Conversely in Figure 4c, the center implant region of the CIMCD–MOSFET overlaps with the oxide edge to block the electric field. Moreover, by dispersing the electric field, a lower electric field is applied to the oxide film compared to the C–DMOSFET and SBD–MOSFET, even at a high voltage of V_DS = 3 kV.

Figure 5 shows the on-state characteristics of each device. The CIMCD–MOSFET uses only a single channel in the on state, resulting in static degradation. Its saturation current is also smaller compared to the C–DMOSFET and SBD–MOSFET. However, owing to the increase in the breakdown voltage capability of the center implant region, the doping concentration of the JFET and N-drift can be increased and the static degradation can be minimized. As a result, the CIMCD–MOSFET has the highest B–FOM compared to the C–DMOSFET and SBD–MOSFET, despite being a single-channel MOSFET.
Electric field distribution of (Figure 4.

Figure 3. Off-state characteristics of C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET at T = 300 K and 450 K.

Figure 4. Electric field distribution of (a) C–DMOSFET, (b) SBD–MOSFET, (c) CIMCD–MOSFET, and (d) MCD–MOSFET without the center implant region.

Figure 5. On-state characteristics of C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET.
Figure 6a shows the third quadrant characteristics of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. Owing to the Schottky barrier, the SBD–MOSFET has the lowest $V_F$. The $V_F$ of the CIMCD–MOSFET is proportional to $Tox_2$. In Figure 6b, the $V_F$ decreases as $Tox_2$ decreases, but the electric field crowding at the oxide edge increases. Owing to the center implant shielding region, reducing the thickness of $Tox_2$ to 5 nm does not cause oxide film reliability issues, resulting in a lower $V_F$ than the C–DMOSFET’s PiN body diode. Table 2 summarizes the static characteristics of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. The CIMCD–MOSFET shows the highest oxide reliability characteristics among the three devices owing to the center implant area. The B–FOM is improved by 2.05% and 11.17% compared to the CMOSFET and SBD–MOSFET, respectively, by minimizing static degradation.

**Table 2.** Static characteristics of devices.

| Parameter                  | C–DMOSFET | SBD–MOSFET | CIMCD–MOSFET |
|----------------------------|-----------|------------|--------------|
| $BV$ [V]                  | 4089      | 3926       | 4045         |
| $R_{ON-SP}$ [mΩ·cm$^2$]   | 9.8       | 10.61      | 9.4          |
| $E_{Mox}$ (@$V_{DS} = 3$ kV) [MV/cm] | 3         | 3.07       | 2.34         |
| $B–FOM$ [kV$^2$/mΩ·cm$^2$] | 1.706     | 1.566      | 1.741        |
| $V_F$ (@$I_{DS} = –80$ A·cm$^2$) [µm] | 3.27      | 1.81       | 2.44         |

### 3.2. Dynamic Performances

Next, we simulated the dynamic characteristics of the device via mixed-mode simulation in TCAD. The short-circuit reliability, parasitic gate capacitance, reverse recovery characteristics, and switching performances of the device were simulated. Figure 7a shows the short-circuit (SC) test circuit diagram. The short-circuit roughness was tested at $V_{DS} = 1700$ V and $V_{GS} = 15$ V. The thermal runaway time in the short-circuit condition was observed by applying a pulse voltage to the gate for a fixed duration. Figure 7b–d show the SC withstand capabilities of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. The temperature represents the highest temperature of the device. In the SBD–MOSFET, when the SC time is 3 μs, the leakage current and the internal temperature of the device rapidly increase in thermal runaway. The SBD–MOSFET has a very short SC withstand time ($T_{SC}$) of approximately less than 3 μs and the lowest SC reliability. Conversely, the CIMCD–MOSFET has the longest $T_{SC}$ compared to the C–DMOSFET and SBD–MOSFET, where device failure occurred at $T_{SC} = 23$ μs. $T_{SC}$ is generally inversely proportional to the device’s drain saturation current ($I_{DSat}$) [48]. Since CIMCD–MOSFETs have a smaller $I_{DSat}$ than C–DMOSFETs, they have the longest SC withstand time and consequently, the highest SC capability. Figure 8 shows the total current density and lattice temperature of the device at the SC thermal runaway point after the gate is turned off. As is evident from Figure 8a,c, the thermal runaway mechanism of the C–DMOSFET and CIMCD–MOSFET.
results in device failure owing to the drain leakage current that is caused by the parasitic npn transistor turn-on [49]. However, as shown in Figure 8b, the off-state leakage current of the SBD–MOSFET occurs at the Schottky contact. The elevated lattice temperature near the Schottky contact enhances the thermionic-field emission there and moves many electrons, generating a large off-state leakage current even in the gate-off state [50,51]. Consequently, the SBD–MOSFET undergoes early thermal runaway and has a very poor short-circuit capability compared to the CIMCD–MOSFET.

**Figure 7.** (a) Equivalent circuit diagram of short-circuit test. Short-circuit waveforms of (b) C–DMOSFET, (c) SBD–MOSFET, and (d) CIMCD–MOSFET.

**Figure 8.** Total current density distribution and lattice temperature distribution at the SC thermal runaway point (\(\theta_{DSS} = 1\, \text{kA/cm}^2\)) of (a) C–DMOSFET, (b) SBD–MOSFET, and (c) CIMCD–MOSFET.

Figure 9 compares the parasitic capacitances \(C_{rss} (C_{GD}), C_{rss} (C_{GD} + C_{GS}),\) and \(C_{rss} (C_{GD} + C_{DS})\) of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET. \(C_{rss}\) is an important parameter that has high correlation with the switching time. In general, because the values of \(C_{rss}\) are proportional to the switching time, it is advantageous to minimize the values of \(C_{rss}\). As the CIMCD–MOSFET has a split gate structure, the overlap area between the gate-drain can be minimized, thereby reducing the parasitic capacitance that is generated from the gate-drain coupling [52]. Consequently, the CIMCD–MOSFET has a low \(C_{rss}\) value that is reduced by 71.06% for the C–DMOSFET and 61.98% for the SBD–MOSFET.
of the time from 90% $V_{DS}$ to 10% $V_{DS}$ ($T_{on}$) is defined as the sum of the time from 10% $V_{GS}$ to 90% $V_{DS}$ ($T_{on}$) and the rise time from 90% to 10% $V_{DS}$ ($T_r$). Similarly, the switching-off time $T_{off}$ is defined as the sum of the time from 90% $V_{GS}$ to 10% $V_{DS}$ ($T_{off}$) and the fall time from 10% to 90% $V_{DS}$ ($T_f$) [54].
As the $C_{rs}$ decreases due to the split gate structure, the CIMCD–MOSFET has a shorter switching time than the C–DMOSFET and SBD–MOSFET. With a short switching time and small $Q_I$, the switching on and off energy losses ($E_{ON}$, $E_{OFF}$) of the CIMCD–MOSFET are greatly reduced, and the total switching energy loss ($E_T$) is reduced by 67.8% and 41.8%, respectively, compared to the C–DMOSFET and SBD–MOSFET. Table 3 lists the dynamic characteristics of the C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET devices.

![Figure 11](image1.png)

Figure 11. (a) Comparison of the (a) drain voltage switching waveforms and (b) drain current switching waveforms of C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET.

![Figure 12](image2.png)

Figure 12. Comparison of the (a) power dissipation and (b) total switching energy loss of C–DMOSFET, SBD–MOSFET, and CIMCD–MOSFET that were obtained via the double pulsed test.

| Table 3. Dynamic characteristics of devices. |
|----------------------------------------------|
| Parameter        | C–  | SBD– | CIMCD– |
| $T_{SC}$ [µs]    | <10 | <3   | <23    |
| $C_{rs}$ [pF·cm$^{-2}$] | 37.94 | 28.88 | 10.98  |
| $T_T$ [ns]      | 114 | 70.4 | 42.2   |
| $I_{RM}$ [A/cm$^{-2}$] | 167  | 35   | 45     |
| $Q_T$ [µC·cm$^{-2}$] | 10.69 | 1.02 | 1.17   |
| $T_{ON}$ [ns]   | 139 | 122  | 92     |
| $T_{OFF}$ [ns]  | 1206| 991  | 551    |
| $E_{ON}$ [mJ·cm$^{-2}$] | 25.48 | 11.44 | 9.28   |
| $E_{OFF}$ [mJ·cm$^{-2}$] | 17.26 | 12.22 | 4.48   |
| $E_T$ [mJ·cm$^{-2}$] | 42.74 | 23.66 | 13.76  |

3.3. Proposed Fabrication Process

Figure 13 shows the proposed fabrication process of CIMCD–MOSFET through S-process simulation. Figure 13a illustrates the formation of the drift region by SiC epitaxial growth on the N+ substrate, and the formation of the P+ shielding region, p-base region, and source region through multi-ion implantation [55,56]. Next, an oxide film is formed by dry thermal oxidation and doped polysilicon is deposited as shown in Figure 13b [57]. Then, in Figure 13c, the polysilicon is etched by anisotropic etching, leaving only the gate region. After making the thin oxide film (Tox2) of the MOS-channel diode through anisotropic oxide etching in Figure 13d, polysilicon is deposited again as shown in Figure 13e [58].
Subsequently, excluding the gate part and the dummy gate part, the remaining polysilicon region is anisotropically etched as shown in Figure 13f. After that, N inter-level dielectric (ILD) oxide film is deposited through CVD in Figure 13g, and finally, the source contact is completed through metal deposition after etching the source region of the ILD oxide as shown in Figure 13h [59].

**Figure 13.** Proposed fabrication process of CIMCD–MOSFET. (a) The drift region is formed through epitaxial growth on an N+ SiC substrate, and P+ shielding, P base, and N+ source are formed through multi-implantation. (b) An oxide film is formed through dry oxidation and doped polysilicon is deposited by CVD. (c) Anisotropic polysilicon etching to form a gate region. (d) Anisotropic etching of SiO$_2$ to form a thin oxide film. (Tox). (e) Deposition of polysilicon through CVD. (f) Anisotropic etch polysilicon to form a dummy gate. (g) Deposition of inter-level dielectric (ILD) oxide through CVD. (h) Etching the oxide and metallization.

### 4. Conclusions

In this study, a built-in MOS-channel diode MOSFET with a center-doped P+ region was investigated via TCAD simulation. The CIMCD–MOSFET effectively protects the gate oxide owing to the center P+ shielding region that overlaps with the oxide edge. Moreover, this region minimizes static degradation by increasing the doping concentration of the JFET and N-drift via electric field dispersion. In addition, the low saturation current allows CIMCD–MOSFET to exhibit better short-circuit withstand capability than the C–DMOSFET and the SBD–MOSFET. The reverse recovery charge, similar to that of the SBD and the split gate structure of the device, greatly reduces the switching time and loss of the CIMCD–MOSFET. Consequently, the B–FOM of the CIMCD–MOSFET is improved by 2.05% and 11.17%, and the switching loss is improved by 67.8% and 41.8%, respectively, compared to those of the C–DMOSFET and SBD–MOSFET. These results demonstrate that the CIMCD–MOSFET can be effectively used as a 3.3 kV high-voltage power module system with a body diode configuration owing to its high reliability and improved switching characteristics.

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