Comparative analysis of electronic loads with two regulators

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Abstract. While developing and testing spacecraft power supply systems, we need devices that simulate various electrical characteristics of the spacecraft payload – electronic loads. Providing high bandwidth of these electronic loads at power carrying several kW may become a difficult task, and one of possible solutions is the use of electronic loads with two controllable regulators – a linear regulator and a switching regulator. Such electronic loads allow combining wide bandwidth of a linear regulator and possibility of energy recovery provided by a switched regulator. In the paper we studied possible topologies of these electronic loads, we developed a mathematical description of the electronic load used in the test, we performed the analysis of admittances and quality of noise suppression for various topologies. The most promising topologies that can be used as electronic loads for spacecraft power systems tests were highlighted.

1. Introduction
Electrical testing of spacecraft power supply system (SPS) is an essential part of spacecraft development process. Compliance of the developed SPS with the claimed requirements is determined during these tests, which are carried out using specialized electronic loads (EL) that simulate static and dynamic electrical characteristics of the payload. Since these ELs are used to solve a wide range of tasks arising during testing [1-6], a number of technical requirements to the load are specified:
- ranges of input voltage and current;
- shapes of input I-V curves;
- permissible deviations of stabilized quantities;
- energy utilization factor (when energy recovery is used);
- input current bandwidth (when EL is used as an AC current source).

Providing all the specified requirements simultaneously may become a difficult task, especially if it is necessary to provide high bandwidth of the input current stabilization at a power carrying several kW. One of the possible solutions is the use of electronic loads with two controllable regulators: a linear regulator and a switching regulator. These ELs allow combining the wide bandwidth of the linear regulator and the possibility of energy recovery (provided by a switched regulator), which also leads to the improvement of mass-dimensional characteristics of EL. [7-15]

2. Possible structures of electronic loads with two regulators.
The main idea of EL with two control loops is that the stabilization of input current is performed by a linear regulator (LR), while a switching regulator (SR) limits the power dissipated by LR. There are two possible ways of connecting LR and SR in such EL: parallel and series. In a parallel circuit the power stabilization of LR is achieved by limiting the LR current, in series – by limiting the LR voltage. In other words, SR in the parallel circuit performs the function of a current stabilizer, and in the serial circuit it serves as a voltage stabilizer. Control loops in the parallel circuit must contain two current sensors (one is for LR and another one is for SR), in the series circuit – one current sensor (CS) and one voltage sensor (VS). In order to simulate different types of input I-V curves (constant power and/or constant resistance stabilization), it is also necessary to add an input voltage sensor to both circuits. There are three possible locations for the current sensors in the parallel circuit and two possible locations in the series circuit; that leads to eight possible different topologies of EL with two control loops (figure 1). Table 1 gives general comparison of parallel and series topologies.
Table 1. Common features of parallel and series topologies

| Advantage | Parallel topologies (a)-(f) | Series topologies (g)-(h) |
|-----------|-----------------------------|--------------------------|
| Possibility of independent current stabilization through LR and SR | Wide-bandwidth LR suppresses disturbances in input current more effectively |
| Disadvantage | An amplitude of induced pulsations is limited by the magnitude of the LR current | Performance of circuit strongly depends on input line/source impedance |

In figure 1, the following designations are used for the set-points: $I_{in}$ – required EL input current, $I_{LR}$ – required LR current, $I_{LR_{max}}$ – maximum permissible LR current, $V_{LR}$ – required LR voltage, $V_{ip}$ – required SR voltage. Reference signals of LR and SR are generated by the control unit (CU) and depend on the position of the current sensors. In addition, CU can perform protection functions; it allows to reduce the total cost of the EL. However, in topologies (b)-(e) and (g)-(h), CU receives information about the magnitude of the current only in one of the elements of EL (LR or SR) which creates additional difficulties in the case when CU performs as a protection device as well.

![Figure 1. Topologies of electronic loads with two control loops](image-url)
Table 2. Individual features of each topology

| (a) | (b) | (c) | (d) | (e) | (f) | (g) | (h) |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 1. Increased durability | +   | +   | +   |     |     |     |     |
| 2. Independent interference induction by LR/SR | +   | +   |    |     |     |     | +   |
| 3. Wide bandwidth of inducted test signal | +   | +   | +   |     |     |     |     |
| 4. LR and SR can be developed independently | +   | +   | +   |     |     |     |     |
| 5. Input current filtration | +   | +   |    |     |     |     | +   |
| 6. Input current magnitude monitoring | +   | +   | +   | +   | +   |     |     |
| 7. Diagnostics of LR and SR |     |     |     |     |     |     | +   |
| 8. Input current can be increased rapidly | +   | +   | +   | +   | +   |     |     |
| 9. Input current can be decreased rapidly |     |     |     |     |     | +   | +   |

Table 2 shows distinguishing features of each topology, namely:

1) **Increased durability** – if LR breaks down, there is an opportunity to continue the work by means of SR only;
2) **Independent interference induction by LR/SR** – the possibility to induce noise of arbitrary waveform on LR or SR current independently; it allows achieving minimal harmonic distortion of this waveform;
3) **Wide bandwidth of inducted test signal** – noise induction is performed through LR which has wide bandwidth;
4) **LR and SR can be developed independently** – LR or SR can be turned on and tested; it is not necessary to connect it to the second regulator (SR or LR respectively);
5) **Input current filtration** – LR reduces noise and pulsations induced on EL input current, in particular, LR reduces input current ripples of SR;
6) **Input current magnitude monitoring** – topology contains current sensor that measures the main stabilizing variable – EL input current; it leads to increasing of stabilization accuracy;
7) **Diagnostics of LR and SR** – it is possible to implement the diagnostics function in the control unit without introducing additional elements into the circuit;
8) **Input current can be increased rapidly** – in parallel topologies (a)-(f), the current increases with the rate corresponding to the bandwidth of LR (but when the current decreases significantly, there is a risk that LR can close completely, and then this current continues to decrease with the rate corresponding to the bandwidth of SR, which is significantly smaller than the bandwidth of LR);
9) **Input current can be decreased rapidly** – in series topologies (g)-(h), the current decreases with the rate corresponding to the bandwidth of LR (but when the current increases significantly, there is a risk that LR can open completely, and then this current continues to increase with the rate corresponding to the bandwidth of SR).

On the basis of the above mentioned positive and negative qualities of each topology, we concluded that the topologies (a)-(c) and (g) were of the greatest interest for further consideration.

3. **Mathematical model**

Figure 2 shows the testing circuit for SPSS with EL that is described by the following system of equations:

\[
\begin{align*} 
  v_{in} &= e_{SPS} - i_{in}Z_{SPS} \\
  i_{out} &= (v_{SRout} - e_{DC})Y_{DC} 
\end{align*}
\]

where \( v_{in} \) – EL input voltage, \( e_{SPS} \) – equivalent output voltage of SPS, \( i_{in} \) – EL input current, \( Z_{SPS} \) – equivalent common impedance of SPS, \( i_{out} \) – EL output current (recovered current), \( v_{SRout} \) – EL output voltage, \( e_{DC} \) – equivalent voltage of DC network (to which energy recovery is performed), \( Y_{DC} \) – equivalent common admittance of DC network.
Figure 2. EL as a part of testing setup

Figure 3. Topologies of electronic loads with two control loops
A control unit (CU) in general case is described by nonlinear dependences of the control voltage of LR \(v_{LR_{cont}}\) or SR \(v_{SR_{cont}}\) on the voltage of sensor input \(v_{VS}\). Further, these dependencies will be denoted as \(f(K_{VS}v_{in})\) for LR and \(g(K_{VS}v_{in})\) for SR, where \(K_{VS}\) is voltage sensor gain.

On the basis of the functional relationships presented in figure 1, it is possible to compile systems of equations describing the relationships between current and voltage in the circuits. The topology (a) is described as:

\[
\begin{align*}
v_{LR_{cont}} &= f(K_{VS}v_{LR}) - i_{LR}K_{CS1} \\
v_{SR_{cont}} &= g(K_{VS}v_{LR}) - i_{SR}K_{CS2} \\
i_{in} &= i_{LR} + i_{SR}
\end{align*}
\]

(2)

where \(K_{CS1}\) and \(K_{CS2}\) are current sensors gains, \(i_{LR}\) and \(i_{SR}\) – LR and SR current respectively.

The topology (b) is described as:

\[
\begin{align*}
v_{LR_{cont}} &= f(K_{VS}v_{LR}) - i_{in}K_{CS1} \\
v_{SR_{cont}} &= i_{LR}K_{CS2} - g(K_{VS}v_{LR}) \\
i_{in} &= i_{LR} + i_{SR}
\end{align*}
\]

(3)

The topology (c) is described as:

\[
\begin{align*}
v_{LR_{cont}} &= f(K_{VS}v_{LR}) - i_{in}K_{CS1} \\
v_{SR_{cont}} &= i_{LR}K_{CS2} - g(K_{VS}v_{LR}) \\
i_{in} &= i_{LR} + i_{SR}
\end{align*}
\]

(4)

The topology (d) is described as:

\[
\begin{align*}
v_{LR_{cont}} &= f(K_{VS}v_{LR}) - i_{in}K_{CS} \\
v_{SR_{cont}} &= v_{LR}K_{VS} - g(K_{VS}v_{LR}) \\
i_{in} &= v_{LR} + v_{SR}
\end{align*}
\]

(5)

On the basis of systems (1)-(5) we constructed the functional diagrams shown in figure 3.

The description of the "LR" block can be obtained both analytically (based on the system of equations describing the structure and elements of the LR) and by identification of the real LR. Figure 4 (a) shows the internal structure of LR on the basis of an identified model in two inputs and single output (MISO), where: \(W_{C1}(s)\) is the transfer function of the LR controller, \(V_{F}\) – forward voltage of p-n junction of controlled switch, \(X_i, U_i = [v_{LR} v_{LR_{cont}}]^T, Y_i = [i_{LR}]\) – state, control and output vectors respectively, \(A_i, B_i, C_i, D_i\) – coefficient matrices of the identified LR model. The scheme of identified MISO-model being used is shown in figure 4 (b).

Identification of the SR model in the "SR" block in figure 5(a) is difficult due to nonlinear operation of SR. In cases where the cutoff frequency of the SR is significantly lower than its switching frequency, SR can be represented as a continuous linear model. Using of continuous linear model of SR is quite justified, because in electronic loads there are no bandwidth requirements that are imposed on SR. In addition to the MIMO-model, the "SR" block also includes \(W_{C2}(s)\) – transfer function of SR gain and \(K_{PWM} = 1/V_{saw}\) – the pulse width modulation (PWM) gain, where \(V_{saw}\) is the magnitude of PWM sawtooth.
It is possible to use any switch-mode converter as SR that meets the requirements for the device. However, in order to protect the equipment under test, there is a requirement for the galvanic isolation of the input and output terminals, which can be realized by means of bridge converters based on the boost and buck schemes (figure 5).

Due to the fact that at the input of SR it is necessary to maintain constant current, we have to set a filter at the input of SR that will smooth the current (inductor) or voltage (capacitor) ripples.

$$W_{C2}(s) = K_{PWM}d$$

$$v_{SRin} = v_{SRout}$$

$$X_2 = A_2X_2 + B_2U_2$$

$$Y_2 = C_2X_2 + D_2U_2$$

$$i_{SR} = n_i i_{out} + L \frac{d}{dt} i_{SR}$$

$$C \frac{dv_{SRin}}{dt} = \frac{2}{n} i_{SR} \cdot (1 - d) - i_{out}$$

Figure 5. Examined switched-mode converter models: (a) block diagram and (b) circuit of boost-based full-bridge converter, (c) and (d) – of buck-based full-bridge converter

It should be noted that in the buck-based circuit (figures 5(c) and 5(d)), when large input current is stabilized, the pulsed current flowing through the input capacitance $C_{in}$ becomes significant. This current can lead to heating of the input capacitor and, as a consequence, to the failure of SR. Thus, in parallel topologies (a)-(c), it is more preferable to use boost-derived converters (figures 5(a) and 5(b)), which are described by the following system of nonlinear equations:

$$\begin{cases} L \frac{d}{dt} i_{SR} = v_{SRin} - \frac{2}{n} v_{SRout} \cdot (1 - d) \\ C \frac{dv_{SRin}}{dt} = \frac{2}{n} i_{SR} \cdot (1 - d) - i_{out} \end{cases}$$

where $i_{SR}$ – SR input current, $v_{SRin}$ – SR input voltage, $v_{SRout}$ – SR output voltage, $d$ – duty ratio, $i_{out}$ – SR output current (recovery current), $n = N_2/N_1$ – ratio of turns of a power transformer ($N_1$ and $N_2$ – number of turns on the primary and secondary windings respectively), $L$ - inductance, $C$ - capacitance.

In the series circuit (g) the change in the value of the EL input current leads to the change of LR voltage. The rate of this change is much greater than can be compensated by the SR because when the high-frequency interference is induced, the current amplitude is limited by active and inductive components of the impedance of the cable line and the input impedance of SR. In order to increase the amplitude of induced interference, it is necessary to reduce the value of the input impedance of the SR at high frequencies which can be achieved by increasing the capacitance of the SR input capacitor. Thus, in the series topology (g) it is recommended to use buck-derived bridge converters (figures 5(c) and 5(d)) which are described by the following system of nonlinear equations:
where \( C_{in} \) and \( C_{out} \) – capacities of input and output capacitors respectively, \( i_L \) – inductor current.

4. Simulation results

For the further research, four EL topologies (a)-(c) and (g) were developed, each of them meets the following requirements:

- input current – 10 A;
- mean power dissipated by the LR – 100 W;
- the largest deviation of the input current from the stabilized value – 0.1 A;
- the largest peak-to-peak voltage of the input current pulsations – 1 A;
- bandwidth – not less than 100 kHz.

Admittance response. One of the conditions for ensuring stability is the fulfillment of the inequality \( Z_{SPS} Y_L < 1 \), where \( Z_{SPS} \) – the SPS output impedance, \( Y_L = I_{in}/V_{in} \) – input admittance of EL (figure 3(a)). For a current source, the best situation is when the conductivity over the entire frequency range is equal to zero.

From the admittance responses (figure 6) it can be concluded that the parallel topologies (b) and (c) have approximately equal input admittance practically on the entire frequency range, while the topology (a) has much higher admittance at the low frequency range. The topology (g) has the best admittance response for the current source which is equal only to tenths of a \( \mu S \) at low frequencies.

Noise interference. The transfer functions of closed control loops are defined as \( W(s) = I_{in}(s)/V_{ref}(s) \) (figure 7). In topologies (a) and (b) \( V_{ref}(s) \) is the reference voltage of both LR and SR, in topologies (c) and (d) \( V_{ref} \) is the reference voltage only for LR.
There is a decay beginning at approximately 10 kHz in topology (a) which is caused by cut-off frequency of SR. In topology (b), unlike the topologies (c) and (g), there is no explicit resonant peak, which makes it possible to impose test signals without distortion having more complex harmonic composition.

5. Discussion and conclusion
The obtained results make it possible to draw a conclusion regarding the choice of a particular topology on the basis of the EL requirements. With more stringent requirements for survivability, the use of topologies (a) and (b) is more appropriate since they can provide continuation of work in cases where LR is in emergency mode. Topologies (a) and (b) are also simpler in design and development as it is possible to design LR and SR independently.

If it is necessary to induce the pulsations of large amplitude while maintaining high recovery rate, the series topology (g) is the most suitable. However, topologies (b) and (c) have wider bandwidth; it allows to induce pulsations on input current of higher frequency. The topology (g) is characterized by the smallest values of the input admittance at low frequencies, but, on the other hand, the topology (g) is more sensitive to the value of output inductance of the tested SPS.

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