Sulfurization temperature effects on crystallization and performance of superstrate CZTS solar cells.

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Abstract

Kesterite materials based on Cu$_2$ZnSnS$_4$ composition are considered as promising absorber material for the next generation of photovoltaics due to raw materials abundance and low toxicity. Developing a superstrate architecture using kesterite as an absorber could be the key to a better performance, which allows new ways of engineering the formation of a kesterite thin film. In this work, we study the effects of the sulfurization temperature on the crystallization of kesterite film when is fabricated in a superstrate architecture, and how this affects the performance of a solar cell. We noted that the temperature affects the final composition of the absorber due to cadmium diffusion at 500 ºC from the CdS layer, while the temperature above 530 ºC is essential for a complete Zn incorporation into the crystal structure. The crystallinity is highly affected, and a temperature of 550 ºC is found to be favorable for the crystal growth, and the fabricated device gave improved performance. Impedance spectroscopy measurements suggest the performance enhancement is due to the reduction of defects and an increase of the depletion width in the $p$-$n$ junction.

Keywords

Kesterite; Superstrate; Sulfurization; Solution process; Crystallinity

1. Introduction

Efforts have been made during the last decades to find a suitable photovoltaic (PV) technology having no dependence on earth-limited or strategic materials. Semiconductors composed of earth-abundant and non-toxic elements, as Cu$_2$ZnSnS$_4$ (CZTS) with kesterite structure, have received significant attention. The high absorption coefficient allows using it in the form of ultra-thin films, and bandgap energy close to the ideal value of Shockley-Queisser make them suitable as light absorbers for their use in PV. CZTS thin films can be deposited at adequate temperatures (500 to 600 ºC, by wet chemistry methods, making it an ideal candidate for large-scale PV production.

Cu$_2$ZnSnS$_4$ present two main similar crystal phases, with the same lattice structure as chalcopyrite, but with a different atoms position. Stannite is present in samples prepared at low temperatures since it has slightly higher energy formation. Kesterite instead, has a lower energy formation and will be the predominant phase when it is prepared at sufficiently high temperatures (Das et al., 2016; Rakitin and Novikov, 2016).

Advances made on CZTS technology are mostly focused on the substrate architecture, adopted from its counterpart Cu$_2$InGaSe$_4$ (CIGS) due to their composition similarities. Generally, this architecture stack follows Mo-CZTS-CdS-ZnO-ITO, which presents a tricky back contact between Molybdenum and CZTS. Voids, low crystallinity, carbon contamination and the emerge of a high resistive MoS$_2$ interlayer are usual problems reported in the back contact for this architecture, which tends to decrease the generated open-circuit voltage (Martinho et al., 2020; Wu et al., 2017). Similar to CIGS and CdTe-based solar cells, the buffer layer in CZTS is composed of a thin film of CdS. Despite the
toxicity of Cd, the use of Cd containing chalcogenides has been found to have low Cd emissions to the environment, as they are stable and water-insoluble unless it is exposed to acidic environments (Fthenakis and Kim, 2007). Limited efforts have been made to explore alternative configurations, which can influence interface, simplification of the manufacturing process, and cost reduction. Alternatively, superstrate structure based on fluorine tin oxide (FTO) coated glass is currently one of the most studied architecture due to its good thermal and chemical stability, preventing at the same time the use of scarce indium used in indium tin oxide (ITO) as a transparent conductive layer. FTO can deliver excellent performance in PV when is covered by a protective and electron blocking film of TiO$_2$, a methodology adopted in organic and perovskite solar cells using spin coating or spray pyrolysis. The fabrication of CZTS on a superstrate architecture is in line with the motivation of reducing the use of scarce elements, while at the same time, it brings the possibility for new ways of improvements as absorber layer due to the sturdiness of the electrode. Since metal oxides and sulfides of the functional layers can be also processed by wet chemistry methods, CZTS allows the fabrication of solar cells by wet chemistry methods (Chen et al., 2012; Satale and Bhat, 2020; Tumbul et al., 2019).

When CdS is used, the Cd layer is sandwiched between TiO$_2$ and the absorber layer, which is strongly bound to the kesterite structure after annealing, thus reducing the possibilities of direct exposure to the environment. An exposed back contact allows for a simple way to investigate hole transport materials, semi-transparent devices, or tandem PV. Recent works from different groups have shown noticeable improvements on superstrate CZTS based devices, making it an attractive candidate for its study. Power conversion efficiencies (PCE) of 3.3% are reached for CZTSSe when an optimized CdS thickness and selenization process is used (Franckevičius et al., 2019; Pakštas et al., 2020). Opportunities of engineering the front surface have been explored using mesoporous TiO$_2$, reaching a 3.92% efficiency (Kang et al., 2019), and modified TiO$_2$ nano-rods allows to reach a PCE of 5% (Wang et al., 2018a, 2018b), with a considerable increment in the extracted voltage. All these have a common step of sulfurization or selenization at high temperature, where the crystallinity of the absorber material is enhanced and the change in composition suffers due to Cd diffusion from the buffer layer. In this work, we study the effect of the sulfurization temperature in CZTS thin films on a superstrate architecture. Solar cells are fabricated in a stack layer configuration of FTO-TiO$_2$-CdS-CZTS-Au. Except for the front (FTO) and back (Au) contacts, all the layers that composed the PV device are prepared by wet chemistry methods. It was observed that the CdS layer was necessary to fabricate an efficient device, which may be related to the alloying of Cd with the absorber layer, and with a slight improvement of the crystallinity and the grain size. XRD and Raman analysis show that the sulfurization temperature influences the crystallinity and absorber composition, due to the reactivity of the CdS and the inclusion of Cd$^{2+}$ into the lattice structure, which is dominating over Zn$^{2+}$ at lower temperatures. Samples sulfurized at an adequate temperature can form big size grains to yield improved PCE. We noted a reduction of the defect density by impedance-voltage measurements, while an increase of the depletion layer helps to increase the photocurrent.  

2. Experimental

2.1 Samples preparation

TEC-15 FTO coated glass was used after a sequential cleaning procedure. In short, the cleaning procedure includes a sequential ultra-sonication step for 10 minutes of the substrates immersed in Hellmanex-water solution, acetone, and isopropanol, respectively. After drying the substrates with compressed air, they were kept under UV
light to remove any organic residue. A blocking layer of TiO$_2$ of c.a 60-80 nm was then deposited on FTO by spray pyrolysis. For that, a solution containing titanium(IV) disopropoxide bis(acetylacetonate) (Merck) in ethanol (Scharlab) with a volume ratio of 1:9 were sprayed at 500 °C. After the deposition, the samples were maintained at 500 °C for 30 minutes.

A thin film of c.a 60-80 nm of CdS was deposited by chemical bath deposition. The samples were immersed in a bath of 180 mL of deionized water at 65 °C containing 56 mg of Cadmium sulphate (Alfa Aesar 98%). Then 18.2 mL of ammonia solution (30%, Alfa Aesar) were added, followed by 20 mL water solution with 100 mg of thiourea (99%, Alfa Aesar). The bath was maintained at 65 °C and the samples were extracted 20 minutes later. CdS deposited on the glass side was removed with diluted HCl.

CZTS film was prepared on top of CdS by spin coating. The solution contains 0.88 M of anhydrous copper (II) chloride (98%, Alfa Aesar), 0.55 M zinc acetate dihydrate (98%, Fisher), 0.55 M tin(II) chloride dihydrate (98%) and 3 M of thiourea (99%, alfa aesar) dissolved on 2-methoxyethanol. The target was a Cu-poor (Cu/(Sn+Zn)=0.8) composition, with the excess of 50% sulfur, to prevent sulfur loss during the precursor film formation. The solution was stirred until all the salts were dissolved, obtaining a yellowish transparent colour. Then 50 µL of the CZTS precursor solution were spun coated at 1500 rpm for 30 s and dried at 270 °C for 2 minutes on a hot plate in the air to form a CZTS precursor film of 450-500 nm.

Samples were then submitted to a sulfurization process at 500, 530, or 550 °C for 45 minutes inside a close quartz tubular furnace containing 50 mg of sulfur powder (99.5%, Alfa Aesar) in an argon atmosphere. After cooling to room temperature, photovoltaic cells were completed by depositing 70 nm of Au as metallic contact by thermal evaporation, defining an active area of 0.55 cm$^2$ by a mask.

### 2.2 Measurements

XRD diffractograms were measured directly on the finished solar cells with a Cubix3 system from PANalytical with a Cu anode. Raman measurements were acquired with an inVia confocal Raman microscope using a 785 nm wavelength laser as excitation. SEM images were recorded with a Hitachi S-3400 electron microscope. The absorption spectrum was recorded with an Agilent Cary 60 UV-Vis spectrometer. For the device characterization, J-V curves were measured with a 2400 Keithley multi-meter, and the illumination of the samples was performed with a class AAA Oriel solar simulator from Newport. The external quantum efficiency was measured on a PVE300 Bentham system, consisting of a 150 W Xenon lamp and a 1/4m monochromator, in a range from 300 to 1000 nm. Impedance measurements were performed inside a faraday box with a Biologic impedance analyser, by applying a 20 mV perturbation in a frequency range from 1 GHz to 100 Hz, and an applied constant voltage from -1.5V to 1V. EC-LAB software was used to fit the equivalent circuits.

### 3. Results and discussion:

To understand the effect of the temperature on the CZTS crystal structure, XRD measurements were performed directly on the final devices. Fig. 1a shows the measured diffractogram for the samples sulfurized at 500 °C, 530 °C, and 550 °C, and an additional CdS free, pure kesterite device at 550 °C was used as a reference. An evolution of the phases can be distinguished when the temperature is increased. For the sample sulfurized at 500 °C, the characteristic peaks of CdS are predominant, with a very small intensity of the peaks corresponding to the kesterite phase of CZTS. On contrary, for
higher temperatures, the peaks corresponding to CdS start to decrease, while the intensity of the kesterite peaks emerges. At 550 ºC, the highest peak intensity from kesterite can be observed, and peaks of CdS are not found, indicating the enhanced crystallinity in kesterite, while there is a reduction of the CdS phase.

The peaks at [112] and [220] planes are indicated in the Figs. S1a and S1b respectively. Shifting to lower angles can be observed for the sample prepared at 500 ºC, which can be attributed to a higher percentage of Cd in the crystal structure. This, along with the disappearing peaks of CdS aforementioned, is evidence of Cd incorporation into the kesterite crystal. Cd$^{2+}$ can easily replace Zn$^{2+}$, forming an alloy of Cu$_2$(Zn,Cd)SnS$_4$ (CCZTS). The shift in the peaks is in agreement with works that intentionally includes Cd in the absorber structure (Hadke et al., 2019; Yan et al., 2017).

Table 1, shows the lattice parameters values calculated for every sample. As expected, the small size of Zn$^{2+}$ reduces the unit cell volume, causing a shift to higher angles, which can be noticed in the reference sample (without CdS) and pure CZTS is formed. When CdS is used, the maximum Cd incorporation is observed at 500 ºC, showing a larger cell volume. A stannite phase of Cu$_2$CdSnS$_4$ can be formed at temperatures of 460 ºC (Zhang et al., 2017), while a temperature higher than 500 ºC is necessary to promote the reaction of ZnS with Cu$_2$SnS$_3$ to form Cu$_2$ZnSnS$_4$ (Gupta and Mohanty, 2019), and at least 550 ºC to eliminate the secondary phases (Jung et al., 2015). In this case, the incorporation of Zn is not completed at 500 ºC, leading to a visible structure with high content of Cd.

At temperatures higher than 530 ºC, the cell volume is in intermediate values, suggesting that Zn starts to compete with Cd in the incorporation to the crystal structure. When the temperature is lower, the remaining Zn within the absorber material is expected to remain as it forms the highly stable phase of ZnS. According to literature, this phase will not contribute to the PV effect and its presence reduces the photocurrent, however, it does not shows a large effect in the big recombination impact due to its wide band-gap and high resistance (Giraldo et al., 2019; Kumar et al., 2015). The Raman spectra of the samples are presented (Figs.1c to 1e) and the deconvolution of the peaks in the sample prepared without CdS shows four peaks that can be associated with a pure kesterite phase (Moreno et al., 2016). All the samples prepared with a CdS layer present a shift to a lower wavelength. A shift of the main peak has been reported for Cd-alloyed CZTS (Sun et al., 2018), confirming that Cd is been incorporated into the absorber layer. The sample prepared at 500 ºC shows a higher shift with respect to the pure CZTS. This is in agreement with the XRD measurements that show higher Cd incorporation. Also, the sample prepared at 500 ºC shows a tail corresponding to a peak at 400 cm$^{-1}$, which can match with a phase of (Zn, Cd)S (Bakhsh et al., 2016). The samples prepared at 530 ºC and 550 ºC does not show evident secondary phases by Raman spectroscopy.
Fig. 1. a) XRD spectra of samples with different sulfurization temperatures, b-e) are the Raman shifts for the samples prepared at 500 °C, 530 °C, 550 °C, and 550 °C without CdS, respectively, with the values of the fitted peaks indicated.
Table 1. Calculated values for the lattice parameters.

| Temperature | a (Å)  | b (Å)  | c (Å)  | Cell volume (Å³) | Crystalline size (nm) |
|-------------|--------|--------|--------|------------------|----------------------|
| 500 ºC      | 5.485  | 5.485  | 11.048 | 332.4            | 3.6                  |
| 530 ºC      | 5.453  | 5.453  | 10.902 | 324.2            | 4.1                  |
| 550 ºC      | 5.458  | 5.458  | 10.909 | 325.0            | 6.8                  |
| 550 ºC w/o CdS | 5.414  | 5.414  | 10.799 | 316.6            | 6.4                  |

Fig. 2. Cross-sectional and top view of solar cells samples sulfurization temperatures for a), e) 500 ºC, b), f) 530 ºC, c), g) 550 ºC, and d), h) 550 ºC without CdS interlayer.
PV performance is highly dependent on the crystallinity of the materials. The charge carrier conductivity is reduced when it travels across the inter-grains due to a higher density of defects that acts as recombination centers. This effect is particularly harmful in polycrystalline materials based on chalcogenides, so a crystal size equal to the film thickness is preferred to avoid recombination across the conductivity direction.

To compare the effect of the temperature in the absorber crystal size, cross-section SEM images were performed (Fig. 2). All of them present an absorber layer thickness of 450 – 500 nm, with no voids in the interface of the FTO/TiO$_2$ front contact. Samples sulfurized at 500 ºC and 530 ºC shows low crystallinity, making a layer of fine grains with less than 50 nm of diameter size. On the other hand, the crystallinity drastically increases for the sample annealed at 550 ºC, showing large crystals of 100-200 nm.

It can be noticed (Fig.3d) that the grain growth seems to be inhibited when no CdS interlayer is used, producing an absorber film of lower crystallinity. This is in agreement with the calculated crystallite size derived from the Scherrer equation (XRD measurements) represented in Table 1.

To explore the effect of temperature on the optical properties of the films, UV-Vis absorbance spectra were measured, (Fig. S2a). The optical bandgap for direct transitions is calculated (Fig. S2b) by a linear fitting in the Tauc plot $(a h\nu)^2$ versus the photon energy $h\nu$. The absorption increases slightly for the samples prepared at 550 ºC in the UV-Vis range, which can be correlated with a higher phase purity. A similar optical bandgap was noted (1.43 eV to 1.45 eV) for the samples prepared with CdS, while a higher bandgap of 1.51 eV is found for the sample of pure CZTS. Since the incorporation of Cd into the kesterite structure decrease the bandgap, the lower bandgap observed suggest the formation of a Cu$_2$(Zn,Cd)SnS$_4$ alloy with a quantity of Cd of around 20% to 30%. (Li et al., 2018).

The presence of Cd itself in the final structure should not be considered necessarily as a drawback. Previous reports verified that alloys of Cu$_2$(Zn,Cd)SnS$_4$ with different quantities of Cd presented improved PV performance by increasing the minority carrier lifetime (Hadke et al., 2019; Li et al., 2018; Su et al., 2015; Yan et al., 2017) and reducing the interface recombination (Yan et al., 2018).

A schematic of the kesterite-based solar cell is shown (Fig.3a) and the PV properties were evaluated by measuring the current-voltage ($J$-$V$) curve under 1 sun illumination intensity (Fig.3b) and the obtained characteristic parameters are shown in Table 2. Device prepared at lower temperature shows a lower performance due to the reduction in open-circuit voltage ($V_{oc}$), while maintains a similar short circuit current ($J_{sc}$) and fill factor (FF) than the devices fabricated at intermediated temperature (530 ºC). For the sample annealed at 550 ºC, both the $V_{oc}$ and the $J_{sc}$ increases, resulting in a higher PCE, but compromising the FF.

Devices without CdS layers were shunted and gave a negligible PV response. A proper explanation is still unclear but we propose that CdS film could act as both dopant and crystallization seed for CZTS, while the contact with TiO$_2$ can promote oxidation of the secondary phases, such as SnO$_2$ (Wang et al., 2018a), hindering the sulfur incorporation and so the CZTS crystallization.

External Quantum Efficiency (EQE) was measured and represented (Fig.3c), all the samples showed a better photocurrent at shorter wavelengths, with a maximum between 400-500 nm, and a progressive reduction for longer wavelengths. Considering that the longer wavelengths are absorbed deeper in the material, the main collection of electron-
hole pairs is for the ones generated closer to the $p$-$n$ junction, suggesting that the electron-hole pair lifetime is short enough to recombine before reaching the $p$-$n$ junction, causing a high loss of current. A low minority lifetime of lower than 2 ns and electron diffusion length $L_n$ less than 0.5 µm is usually reported even for high-performance devices, resulting in low collection of current for absorber light far from the junction (Hages et al., 2017; Repins et al., 2013), causing a noticeable decrease of the current collected when the depletion width is not sufficiently thick.

In particular, the sample annealed at 550 ºC showed an improved photon to current conversion throughout the whole visible wavelength region which can be attributed to the higher absorption in bigger crystal size, reducing inter-grain recombination. For wavelengths longer than 860 nm, corresponding with a 1.47 eV of photon energy, there is no photo-current generation, in agreement with the calculated bandgap from the tauc plot of 1.43 eV. The sample annealed at 500 ºC shows an extended range of wavelengths contributing to the EQE, until 900 nm, which may be due to a higher Urbach absorption in the band tailings. Conversely, the sample annealed at 530 ºC has better photon conversion at intermediate wavelengths and shows a bandgap of 1.46 eV, similar to the calculated by the tauc plot (1.44 eV).

This supports the hypothesis shown by XRD, where the Zn incorporation to the kesterite lattice requires at least a temperature of 530 ºC. At lower temperatures, such as 500 ºC, the Zn incorporation is smaller, therefore Zn could remain as a secondary amorphous phase of ZnS forming small grains as it was confirmed by SEM images.

Intrinsic instabilities and recombination processes can be evaluated by $J$-$V$ curves measured in dark (Fig. 3d). We suggest that a large leakage of the current at reverse polarization can be the plausible reason that affects the device performance, indicating the existence of shunts in the devices. These shunts can be attributed to a high quantity of conductive secondary phases in the absorber or due to a high surface porosity or crack defects that allows gold to infiltrate the pores between the crystals, increasing the possibilities of being in contact with the FTO.
Fig. 3. a) Scheme of the layer stack deposition, b) $J-V$ curves under one sun illumination, c) EQE spectra, d) $J-V$ curves in dark.

Table 2. Characteristic parameters calculated from the photovoltaic performance. $J-V$ measurements were performed at 100 mV·s$^{-1}$ scan.

| Temperature | $V_{oc}$ (V) | $J_{sc}$ (mA/cm$^2$) | Fill Factor (%) | PCE (%) | $R_s$ (Ω) | $R_{sh}$ (Ω) |
|-------------|--------------|-----------------------|-----------------|---------|-----------|-----------|
| 500ºC       | 0.164        | 2.4                   | 33.2            | 0.128   | 18.31     | 215.9     |
| 530ºC       | 0.220        | 2.5                   | 38.9            | 0.216   | 19.53     | 282.2     |
| 550ºC       | 0.258        | 7.6                   | 26.6            | 0.518   | 17.07     | 208.7     |

To unravel the electrical properties of the samples, impedance spectroscopy (IS) was performed in an applied voltage range from [-1.5 V −1 V] under dark and illumination conditions. The used circuit to fit the impedance curves is shown (Fig. 4a), it is composed of a series resistance ($R_s$) followed by an RC loop, which represents the recombination resistance $R_{pn}$ and the capacitance of the $p$-$n$ junction $C_{PN}$. The second loop consists of a non-ideal capacitor RC circuit, $Q_d$ and $R_d$, which agglomerates other capacitive effects, such as secondary phases defects and metallic contacts interfaces. This circuit fits well with the measurements (Fig. S3) at every voltage. Under illumination, the recombination processes can be noticed. By using IS, a reduction of the semicircle is observed under illumination, (Fig. 3b), which represents the reduction in the recombination resistance $R_{PN}$ due to an increase of the charge carrier density in the depletion region (Mora-Seró et al., 2009).
The resulting values for the circuit elements at the open circuit are summarized in Table 3. The series resistance, mainly limited by the conductivity of the FTO/TiO\textsubscript{2} contact, did not change significantly, suggesting that the blocking layer of TiO\textsubscript{2} protects the FTO even at high temperatures and sulfur atmosphere. R\textsubscript{PN}, seems to increase with the processed temperature, reflecting the increase of the CZTS grain size and decrease of recombination centres. The capacitance of the junction decreases with the increasing temperature. The capacitance mainly depends on the depletion layer width, as indicates (eq. 1), and the drop in the capacitance value entails an increase of the depletion layer thickness.

The characteristic constant time ($\tau$) of the RC circuit is calculated by multiply R\textsubscript{PN} and C\textsubscript{PN}, and is usually associated with the carrier lifetime, as it represents the discharge time of the capacitor. $\tau$ gives a representative value when is measured on direct polarization under small applied voltage, and the recombination takes place mostly at the interface. This lifetime was extracted from the IS under illumination (Fig.4c), revealing that the electron lifetime is dramatically reduced with the voltage for the samples made at 500 ºC and 530 ºC. However, the sample sulfurized at 550 ºC retains a carrier lifetime of 4 µs at 0.6 V, which suggests that fast interface recombination is the main limitation for the current generation in the samples fabricated at 500 ºC and 530 ºC.

Fig. 4. a) An equivalent circuit used to fit the impedance measurements, b) Nyquist plot at $V=0$ for the sample sulfurized at 550 ºC under dark and illumination, c) Carrier lifetime under illumination and d) carrier density profile calculated from the circuit values in dark, with the values at $V=0$ indicated.

The carrier density and the depletion width close to the $p$-$n$ junction can be extracted from the Mott-Schottky measurements (Fig. S3), following the equations (1) and (2), and it is represented in Fig. 4d. The values that correspond to 0 V are marked in black.
\[ W = \varepsilon \frac{A}{C} \]  
\[ N_A = \frac{2\varepsilon}{qW^2} (V_{bi} - V) \]

Where \( W \) is the depletion width in the p side, \( \varepsilon \) the dielectric constant of the absorber with a value of 6.7 for CZTS (Persson, 2010), \( A \) the contact area, of 0.55 cm\(^2\), \( C \) the calculated capacitance (\( C_P \)), \( N_A \) the carrier density of acceptors, \( q \) the electron charge, \( V_{bi} \) the built-in potential and \( V \) the applied voltage.

This method allows studying the electronic properties of the absorber layer, since the depletion width is extended mainly in the layer with lower carrier density, and the n-type carrier density is in the order of \( 10^{20} \) cm\(^{-3}\) due to the FTO contribution. Therefore, any possible impact from the remaining CdS will be small in comparison with the change of the properties of the absorber layer due to Cd alloying.

Samples annealed at 500 °C and 530 °C show a similar trend, with a very thin depletion width and an unusually high concentration of carrier density that drastically increase with the reverse voltage. A high carrier concentration can be due to the result of a high number of defects. According to previous studies, even a small quantity of secondary phases of CuS\(_x\) or SnS\(_x\) can have a huge effect on the electric properties. (Giraldo et al., 2019; Kumar et al., 2015) These phases tend to accumulate in the inter-grains (Wu et al., 2017), consequently, small grain size is expected to contain a higher amount of these secondary phases that acts also as recombination centers. The increase of the carrier concentration also produces a decrease of the depletion layer thickness, following the eq. 2, reducing the carrier concentration (electrons-hole pairs) that can be separated before reaching the p-n junction.

Sample annealed at 550 °C shows a thicker depletion thickness and a lower carrier concentration of \( 2.19 \times 10^{17} \) cm\(^{-3}\), in accordance with typical values reported for CZTS (Payno et al., 2020; Prabhakar and Jampana, 2011). This reduction of carrier concentration can be associated with the increase of the crystal grain size and a reduction of defects, resulting in an improved photo-voltage, while the thicker depletion layer gives a better carrier collection and a better photo-current.

Even with the increase of the depletion width, this value is small compared with efficient PV devices. Attention has to be made to reduce the recombination defects of the absorber material and increase the depletion thickness to a value that allows the collection of most of the photocurrent.

The crystallinity of CZTS can be also stimulated at intermediate sulfurization temperatures for longer periods if a constant supply of sulfur is available(Wu et al., 2017). In a superstrate architecture, a temperature of at least 530 °C for a long time could promote the crystallization with better quality crystals, and ensuring the inclusion of Zn atoms in the lattice over Cd. As shown in Fig.S4, it is also important to consider the influence of the temperature on the FTO film. To avoid a high degradation of the FTO under the sulfur atmosphere, all the FTO area was covered with the blocking layer of TiO\(_2\), which acts conveniently as a protective layer against sulfur. The sheet resistance of protected FTO trends to increase with the increase of the annealing temperature when is higher than 530 °C. At 550 °C, a sheet resistance of 55.5 Ω/sq can be considered sufficient to achieve a good PV performance in our case, but at higher temperatures, the
sheet resistance can limit the PCE. Therefore, the use of a temperature lower than 550 °C is preferable to avoid an excessive reduction of the conductivity of the FTO.

**Conclusions**

Superstrate architecture for CZTS based photovoltaic cells is an attractive candidate if the current challenges can be overcome. Our work reflects the importance of temperature sulfurization and its main effects on the morphological, electrical, and photovoltaic properties of absorber material. We noted the influence on the final composition and crystal structure when the annealing temperature was varied in the range from 500 °C to 550 °C. We noted, the crystal structure starts to form in a high quantity of Cd at a lower temperature, meanwhile, Zn incorporation in the structure is relevant at temperatures of 530 °C. At this temperature, CdS is detected, while CZTS starts to show crystallization. Structural studies revealed crystallinity is enhanced at 550 °C, however, most of the CdS layer is consumed at this temperature and incorporated into the kesterite structure. A larger crystal grain size is associated with a reduction of defects that acts as recombination centers, resulting in improved open-circuit voltage. Impedance measurements suggest an increase of the depletion width in the sample with higher crystallinity, improving efficient separation of electron and hole pairs, and thus increasing, the collected photocurrent in most of the wavelengths. A controlled composition with high crystallinity can allow a competitive use of CZTS on superstrate architecture. Also, on the FTO/TiO\textsubscript{2} contact, nano and mesostructures can be used, while a suitable hole transport layer on the back contact can have better compatibility than in the substrate architecture to fabricate photovoltaic with earth-abundant materials.

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Supporting information

Sulfurization temperature effects on crystallization and performance of superstrate CZTS solar cells.

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Fig. S1 a) Zoom-in at [112], and b) [220] peaks from XRD.

Fig. S2 a) Absorbance spectra of the samples made at 500, 530 and 550ºC and b) Tauc plot with calculated band-gap.
Fig. S3 Nyquist spectra measurements (dots) and circuit fitting (lines) for the samples at 500, 530 and 550 ºC under dark a), c), e), and illumination b), d) and f) respectively. The bias was performed in 0.1 V steps, from -1 V to 1 V in dark and from 0 to 0.6 V under illumination, with every step represented with a different colour.
Fig. S4 Mott-Schottky measurements for the samples prepared at a) 500 °C, b) 530 °C and c) 550 °C. The linear decay at low direct polarization is used for the calculation of the $V_{bi}$, since the Mott-Schottky equation is valid for an applied voltage $V < V_{bi}$.

Fig. S5 Sheet resistance of FTO (TEC-15) after sulfurization at different temperatures. Note that the FTO is conveniently covered by the blocking layer of TiO$_2$, and scratched away with a piece of steel after the annealing. A direct exposition of FTO to a sulphur atmosphere turns the FTO yellowish, shown in the inset, with a sheet resistance in the order of 1-100 kΩ/sq, probably due to formations of SnS$_x$ phases.