User-Level Memory Scheduler for Optimizing Application Performance in NUMA-Based Multicore Systems

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Abstract—Multicore CPU architectures have been established as a structure for general-purpose systems for high-performance processing of applications. Recent multicore CPU has evolved as a system architecture based on non-uniform memory architecture. For the technique of using the kernel space that shifts the tasks to the ideal memory node, the characteristics of the applications of the user-space cannot be considered. Therefore, kernel level approaches cannot execute memory scheduling to recognize the importance of user applications. Moreover, users need to run applications after sufficiently understanding the multicore CPU based on non-uniform memory architecture to ensure the high performance of the user’s applications. This paper presents a user-space memory scheduler that allocates the ideal memory node for tasks by monitoring the characteristics of non-uniform memory architecture. From our experiment, the proposed system improved the performance of the application by up to 25% compared to the existing system.

Keywords—Memory Scheduling; NUMA Architecture; Multicore System; Memory Contention

I. INTRODUCTION

As users require a high performance computer [1] for mass computation, applications need a high-performance computing system to execute jobs more quickly. The demand for high performance has meant CPU architecture has developed from a single CPU to a multicore CPU. Recently, CPU architecture has evolved to a multicore CPU architecture based on non-uniform memory architecture as shown in Figure 1. In response to this, the design of the modern computer faces a very challenging software assignment called thread scheduling. The technique is used to control the memory nodes at the operating system level, and manages the memory usage of tasks to avoid the problem where tasks lean towards one memory node.

However, in the technique of using the operating system level the relative importance among user applications cannot be recognized. Therefore, it is important that we find an automatic memory scheduling method in the user-space. Moreover, users need to have in-depth system knowledge to obtain high performance applications and effective memory utilization in the existing systems. Therefore, users cannot utilize the multicore system based on non-uniform memory architecture (NUMA) [2], [3] because they need to have an in-depth NUMA architecture knowledge. This paper presents a novel memory scheduler that removes unnecessary memory latency and supports high-performance execution of the application. Our proposed system schedules memory nodes after monitoring NUMA architecture automatically in the user-space.

The remainder of this paper is organized as follows. Related work is described in Section II. Section III addresses the design and implementation of the proposed techniques in detail. Section IV shows the evaluation results. Finally, Section V concludes the paper.

II. RELATED WORK

A. NUMA scheduling techniques in kernel-space

SchedNUMA [4] optimizes memory locality in the NUMA system by placing tasks [5] into the same NUMA node. However, this approach cannot maintain the compatibility of API because the approach needs to perform definition and implementation of additional APIs [6] for grouping processes. Automatic NUMA Balancing [7] migrates the pages of a task to another memory node when the page fault handler attempts to swap the unmapped pages from the page table entry. This technique can execute memory scheduling automatically in the kernel space. However, it is very difficult for the operating system to optimize the optimal NUMA tuning. Ultimately, the system administrator needs to fulfill tuning work in addition to the optimization tools.
B. NUMA scheduling techniques in user-space

Sergey Blagodurov [8] addressed the optimization method of performance that uses CPU affinity functions [9] in the user-space to obtain maximization of the application’s performance. However, this technique damages the effective memory utilization of tasks because the proposed idea statically fixes tasks into a specific NUMA node. Moreover, this approach does not handle the automated method of the memory scheduling in the user-space.

III. PROPOSAL OF USER-LEVEL NUMA-AWARE MEMORY SCHEDULER

Our proposed technique maintains an ideal memory locality to help the high-performance execution of the application by removing the possibility of memory latency. To reach this goal, the proposed system automatically executes (re)allocation of jobs by finding the best ideal NUMA node in the user-space with the collected information after monitoring the NUMA bus topology and run-time memory usage.

![Figure 2. System Architecture of our proposed system](image)

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The proposed system creates a thread to collect scheduling information of the tasks from the file system such as procfs and sysfs. The created thread repeatedly executes work collecting scheduling information until in 3) the user-space NUMA scheduler is completed.

A. Algorithm of the runtime monitor

The proposed system creates a thread to collect scheduling information of the tasks from the file system such as procfs and sysfs. The created thread repeatedly executes work collecting scheduling information until in 3) the user-space NUMA scheduler is completed.

![Algorithm 1. Monitor: Runtime monitoring mechanism](image)

Algorithm 1. Monitor: Runtime monitoring mechanism

```plaintext
1. Create a new thread for receiving and dealing with the run-time monitoring data
2. Repeat monitoring until user-space NUMA scheduler stops
3. Sleep for m NUMA specific data
4. Collect the data monitored from proc file system (proc<PID>(stat: numa_maps))
5. End Repeat loop
```

Figure 3. Algorithm of the runtime monitor

B. Algorithm of the reporter

In 2), the Reporter receives monitoring information of the runtime until in 1) the Monitor terminates. First, in 2), the Reporter preserves information that filters NUMA specific data from the collected data. If the distribution status of the memory node is not balanced or the execution flow of tasks is changed by the operating system level memory scheduler, the Reporter in 2) executes the assignment to find a suitable memory node for the high-performance of important applications. Second, in 2), the Reporter calculates runtime high-performance factors, re-sorting processes of the NUMA list, and the ideal memory node for new tasks. Finally, in 2), the Reporter sends this information to 3), the user-space NUMA scheduler.

![Algorithm 2. Reporter: Mechanism to report collected NUMA-specific data](image)

Algorithm 2. Reporter: Mechanism to report collected NUMA-specific data

```plaintext
1. Run-time monitoring data
2. Repeat until runtime monitoring mechanism stops
3. Collect NUMA specific data
4. If loading of system is unbalanced or behavior of the processes changed or powerful core is idle
5. Computing the run-time slowdown factor
6. Sorting the process NUMA list by multi-core slowdown factor
7. Computing the contention degradation factor
8. Sorting the process NUMA list by contention degradation factor
9. Sending signal to trigger schedule
10. End If
11. End Repeat loop
```

Figure 4. Algorithm of the reporter

C. Algorithm of the user-space memory scheduler

![Algorithm 3. User-space scheduler: Automatic NUMA-aware scheduling](image)

Algorithm 3. User-space scheduler: Automatic NUMA-aware scheduling

```plaintext
1. Computing the number of powerful core candidates based on load balanced memory policy
2. Retrieving suitable processes to be scheduled on powerful cores from NUMA list
3. Setting static CPU pin from manual input of administrator
4. If retrieved processes != current processes on powerful cores
5. Migrate the processes
6. End If
7. If current resource contention degradation is too big
8. Scatter the processes with heavy contention
9. Calculating degradation factor in order to minimize resource contention degradation
10. Migrate the processes and the its sticky pages
```

Figure 5. Algorithm of the user-space scheduler
In 3), the User-space scheduler determines a suitable CPU number to ensure high-performance of a specified user-space application using information received from 2), the Reporter. At this time, in 3), the User-space scheduler considers the static CPU affinity information required by the server administrator as well as the NUMA specific information received by 2), the Reporter. Moreover, if the contention of the resource is too high, in 3), the user-space scheduler attempts to distribute the tasks, considering the contention ratio of the task.

IV. EVALUATION

We prepared an experimental system with an Intel Xeon NUMA Server (Server: DELL PowerEdge R910, CPU: Intel Xeon E7-4850 @2.00GHz, 40 Cores, Memory: 32GiB, OS: Linux 3.2, Platform: Ubuntu 12.04 LTS 64bit) to verify the effects of our proposed idea. We set an evaluation system as follows to provide a reasonable experimental condition:

- Half of the workload focuses on the CPU intensive task scheduling with the PARSEC benchmark suite [3], [12].
- The other half of the workload focuses on memory-intensive task scheduling with the PARSEC benchmark suite.

PARSEC [12] is a benchmark suite composed of multithreaded programs. The suite focuses on emerging workloads [13] and was designed to be representative of next-generation shared-memory programs for chip-multiprocessors. Table 1 shows a qualitative summary of the inherent key features of the PARSEC benchmark suite.

Table 1. Key characteristic of PARSEC benchmarks

| Program   | Application domain     | Parallelization model | Parallelization granularity | Data sharing | Data exchange |
|-----------|------------------------|------------------------|-----------------------------|--------------|---------------|
| blackholes| Financial analysis     | data-parallel          | coarse                      | high         | low           |
| bodytrack | Computer vision        | data-parallel          | medium                      | high         | medium        |
| cameral   | Engineering            | unstructured           | fine                        | low          | low           |
|facesim   | Animation              | data-parallel          | coarse                      | low          | medium        |
|femto      | Similarity search      | pipeline               | course                      | low          | medium        |
|fluidanimate | Animation           | data-parallel          | fine                        | low          | medium        |
|heme       | Data mining            | data-parallel          | medium                      | high         | high          |
|streamcluster | Data mining         | data-parallel          | medium                      | low          | medium        |
|swaptions  | Financial analysis     | data-parallel          | course                      | low          | medium        |
|vips       | Media processing       | data-parallel          | coarse                      | low          | medium        |
|s264      | Media processing       | pipeline               | coarse                      | low          | medium        |
characteristics of PARSEC benchmarks. The pipeline model is a data-parallel model which also uses functional partitioning. PARSEC workloads were chosen to cover different application domains, parallel models [14], and runtime behaviors.

Figure 6 shows the correlation of performance reduction between the imbalance of memory utilization and memory contention in the NUMA architecture based multicore system. When we applied our approach to the NUMA system, PARSEC incurred a performance reduction of over 90%. This means that PARSEC is very suitable as a workload generating memory contention in a NUMA architecture based multicore system [15].

Figure 7 shows the experimental result of the application execution time of our proposed system compared to the existing system. From our experiment, our proposed system improved the execution time of PARSEC applications by up to 25% when we adapted our proposed system in the existing system. The proposed system could obtain 85% of improved execution time compared to Automatic NUMA Scheduling because our proposed system can recognize the importance of user-space applications. The Static Tuning technique manually optimizes tasks [16] with the CPU affinity technique, and had good results at the three applications, including bodytrack, blackscholes, and fluidanimate [12]. This means that the Static Tuning technique is not practical and depends on the technical ability of the server administrator. Therefore, we were not able to obtain consistent results for performance improvement with the Static Tuning method.

Additionally, we evaluated the throughput of the webserver and database in the real server environment that executes many service daemons to verify effects of our proposed system. Figure 8 shows the experimental result of performance when we ran the Apache webserver and MySQL database. The y-axis of figure 8 refers to the average time for improvement, the worst time for improvement, and the time deviation for improvement. From our experiment, we verified that our proposed system could improve the throughput by up to 12.6% of the Apache webserver and 7% of the MySQL database without any manual optimization.

The proposed system can improve the execution speed of a specified application dramatically in a server environment that runs memory-intensive applications because the proposed system can execute the memory scheduling of tasks while considering the importance of user applications. We verified that the proposed system is very practical and useful in NUMA architecture based high-performance computing servers.

V. CONCLUSION

The NUMA architecture for a scalable multicore system [7], [18] facilitates the fast high-performance of user-space applications. However, the system administrator needs to perform tuning work with optimization tools because optimal NUMA tuning using the operating system is very difficult. It is impractical for the administrator to understand the memory architecture of the NUMA architecture to obtain stable memory utilization and high-performance. The proposed system reallocates tasks into an ideal memory node with collected information after monitoring the characteristics of the NUMA topology [19] in the user-space without a kernel space. Our approach does not depend on the operating system because the proposed idea rearranges the tasks in the user-space. In other words, our proposed system is a new user-level NUMA aware memory scheduler considering the memory utilization and optimization of performance without the processor affinity technique that damages the memory utilization.

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