Development of Computer Intelligent System-Level Electronic Integrated Package Microsystem Technology

Hao Lv*, Bao Deng, Chenguang Shi
Xi'an Aeronautics Computing Technique Research Institute, Aviation Industry Corporation of China, Xi'an, China

*Corresponding author: lvhao20032003@mail.nwpu.edu.cn

Abstract. Electronic product systems are gradually developing in the direction of miniaturization and high integration, and the post-Moore era has arrived. The boundaries between integrated circuit chips and integrated packaging components are becoming blurred, and a new situation of integration and development has been formed for various system-level applications. Microsystems bring together innovations and breakthroughs in multiple disciplines and technologies, and have been widely used in both military and civilian fields. This article provides an overview of the current status and future development trends of advanced packaging technologies in the field of integrated circuits, focusing on existing advanced packaging technologies, such as wafer-level packaging, 2.5D, 3D, SIP and Chiplet integration, and other advanced packaging technologies. And introduced the application of microsystem technology in the microelectronics industry, military field and other civilian fields. At the end of the article, the microsystem technology is prospected.

Keywords: Microsystem, SIP, Microelectronics Packaging, Chiplet.

1. Introduction
Microsystem technology integrates microelectronics, microelectromechanical and microphotoolectric technologies. Through system architecture and software algorithms, microsensors, microcontrollers, microactuators, microenergy and various interfaces are integrated into software and hardware. Adopt micro-nano manufacturing and micro-integration technology to realize the micro-nano scale of the system structure. It is recognized as one of the revolutionary technologies of the 21st century.

The innovative development of semiconductor technology has accelerated the development of the packaging industry. The requirements of high-performance computing, high frequency and high speed, high reliability and low latency, and microsystem integration have promoted the antenna in package (Antenna in Package, AiP), FC, 2.5D/3D, The application of advanced packaging technologies such as Through Silicon Via (TSV), System in Package (SiP), and Fan-out packaging [1].

This article analyzes the development history of chip packaging technology and points out that SiP packaging technology has greater development potential and advantages. On this basis, the current mainstream advanced packaging technology is introduced and the future development direction of integrated circuit packaging technology is given.
2. **Microsystem IC Technology**

Semiconductor packaging technology is divided into through-hole plug-in packaging, surface-mount packaging, ball matrix packaging, wafer level packaging (Wafer Level Package, WLP) and flip chip, multi-chip assembly (Multi-Chip Module, MCM), New technologies such as SiP and three-dimensional packaging (3D), as well as new technologies such as System on Chip (SoC) packaging, TSV, Micro Electro Mechanical System (MEMS) packaging, Fan-out packaging, etc. 5 stages [2].

MMIC (Monolithic Microwave Integrated Circuit) is a monolithic microwave integrated circuit. The frequency of foreign MMIC chips has developed in the direction of terahertz, and the packaging is developing towards three-dimensional MMIC (3D MMIC). The products cover the frequency range from microwave to millimeter wave. There are many types and excellent performance. MCM (Multi-chip Module) integrates several technologies such as multi-layer PCB, high-density interconnection, SMT, and micro-encapsulation. It has become quite mature and extensive in foreign communications markets and military applications. It is systematic and small an important way to transform. At present, the integration of MCM technology is getting higher and higher, and it is developing from two-dimensional to three-dimensional multi-chip assembly (3D MCM). The United States and Japan are relatively leading in the development of multi-chip assembly technology.

The microcomputer electrical system (ie Micro-electro-mechanical System, referred to as MEMS), is composed of micro-sensors, micro-actuators and micro-energy, and realizes the organic fusion of microelectronic technology and precision machining technology. It adopts silicon micromachining technology, which can manufacture thousands of micro-electromechanical devices on a silicon wafer, which solves the bottleneck of mass production in traditional technology, thereby reducing costs and improving efficiency. System on Chip SOC (System on Chip) is the future of microelectronic integrated circuits. The system includes CPU, memory and peripheral circuits. It takes the embedded system as the core and integrates software and hardware. SOC technology can simplify the circuit design to the greatest extent, and improve the stability, reliability, and low power consumption of the software and hardware design in the entire product system. And so, on are simplified to the IC design to solve.

SiP encapsulates multiple semiconductor chips and passive devices in the same chip to form a system-level chip, instead of using a PCB as a carrier between the chip connections, the density of the internal wiring of the system-in-package can be far greater. Higher than the PCB trace density, it can solve the performance limitation of PCB. SiP technology has the advantages of small size, short development cycle, low cost, high production efficiency, simplified system development, and high performance.
TSV technology can realize vertical stack interconnection between chips without wire bonding. It is one of the most effective technical ways to realize multi-function, high performance, high reliability, lighter, thinner, and smaller system-in-package. 3D TSV is to stack the chips in multiple layers on the Z axis, and it is necessary to laminate and bond bare chips of different materials, types and sizes in the vertical direction to achieve mechanical and electrical interconnection. 3D TSV packaging technology is mainly used in applications such as CMOS, memory, mobile phone RF modules, MEMS, GPU/CPU, and power semiconductor devices.

WLP technology is a technology in which the entire wafer is packaged and tested first, and then cut to obtain the finished chip. The chip size obtained by the package is the same as that of the bare chip. Wafer-level packaging has two major advantages: the chip I/O is distributed on the entire surface of the IC chip, making the chip size reach the limit of miniaturization. Many chips are packaged, burned and tested directly on the wafer, thereby reducing the conventional process flow and improving the packaging efficiency [3].

Chiplet is a common heterogeneous integration and IP reuse strategies (chips) project of Defense Advanced Research Projects Agency (DARPA). Chiplet refers to an IP core and a design pattern, in order to reuse the IP core, it is chipped and packaged separately [4]. Compared with the traditional single-chip scheme, chipet has higher design yield and lower cost. The research shows that when the chip area is less than 10mm2, the yield difference between single-chip and chipet scheme is very small, but once the chip area exceeds 200mm2, the yield of the single-chip scheme will be more than 20% lower than that of the chiplet scheme. It can be expected that the yield of the single-chip scheme may not exceed 10% in the area of 700 ~ 800mm2. Another advantage of chiplet is that it allows chip packages under different processes to be connected. For analog circuit engineers, in order to adapt to the changes of Moore's law, Under the constraints of advanced technology, it becomes very difficult to design the amplifier. If the chiplet scheme is adopted, the analog circuit can be designed at the appropriate process node and the most advanced process design calculation core can be used to improve the utilization efficiency of advanced technology and reduce the cost. The yield of chiplet (small chip, chip particle and bare chip) is good due to its small area. The chiplet model based on bare chips may also be used as a solution to bring subversive changes to various industrial chain links such as upstream IC design, EDA tools, manufacturing technology and advanced packaging and testing. It is the most effective means for the continuous development of the IC industry. The era of post Moore's law has indeed come.
3. Microsystem technology application

Microsystem technology application South Korea's Samsung Electronics announced the use of through silicon via technology to produce a DDR3 dynamic random-access memory with a capacity of 8 Gb. In its Chiplet program Foveros, Intel uses advanced technology for computing chips, and uses large-node technology for power management, analog circuits and various sensors. Chiplet can also combine chips from different companies, such as the recently announced Intel Core processor using MD Radeon Graphics technology. AMD’s 1st generation EPYC processor, 2nd generation EPYC processor and 3rd generation Ryzen processor, Intel's Stratix 10 FPGA and Lakefield processor, Nvidia’s MCM-GPU, French CEA’s 96-core processor, Xilinx (Xilinx) Vertix-7 FPGA, Marvell's MoChi architecture, etc. These chips are based on Chiplet design [5].

The United States, Europe, Japan and other countries are at the forefront of the development of micro-system technology, and have adopted a large number of micro-system technology in the development of missile weapon systems. MMIC is used in the phased array radars of American F-15 and F-16 fighter jets. The two projects of DARPA (US Defense Advanced Research Projects Agency), "Extended Millimeter Wave Architecture for Reconfigurable Transceivers on Radar" and "Three-dimensional Micro Electromagnetic Radio Frequency System", mainly study the 3D stacking of micro system devices Architecture and 3D processing technology.

In the automotive field, MEMS pressure sensors in micro-systems have been used to measure fuel pressure, tire pressure, air bag pressure, and pipeline pressure; in the biomedical field, micro-system technology has been used in diagnostic systems and detection systems; micro-systems are even more non-existent. Everywhere, small drones, sports watches, wearable devices, etc. are all micro systems.

4. Summary and outlook

Microsystem technology is developing in the direction of multifunctional integration, three-dimensional stacking, hybrid heterogeneous integration, and smart sensing. Especially in the military field, there will be more weapon systems in the future based on microsystem technology to achieve microminiaturization, high integration, intelligence, and light weight. The application of SiP packaging technology is also an important realization path beyond Moore's Law. By 2022, 2.5D and 3D technologies will account for more than 50% of the advanced packaging market, and multiple industry participants will adopt 3D technologies and strengthen the overall ecology of advanced packaging technologies through cooperation. Chiplet and OSDA will greatly reduce the threshold of chip design and bring new changes to the chip industry. This is also a great opportunity for the development of China's semiconductor industry.

References

[1] Fuming M A, Wang H, Department N E. Overview of microsystem technology and its development. Electronic Components and Materials, China, 2019.

[2] ZHOU Xiaoyang. Overview of Advanced IC Packaging Technology. Applications of IC, China, 2018, 35(06): 1-7.

[3] LU Yanfei. Study on Status of IC Packaging Technology. Electronic technology, China, 2020, 49(08): 8-9.

[4] YANG Hui. Evolution and Challenge of Chiplet in More Moore. Applications of IC, China, 2020, 37(05): 52-54.

[5] ZHEN Guilin. el. Survey on Chiplets Packaging Structure and Communication Structure. Journal of Computer Research and Development, China, 2021.