3SSC-A-Based Step-Down DC–DC Converters: Analysis, Design and Experimental Validation

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Abstract: This paper proposes two non-isolated step-down DC–DC converters based on the type-A three-state switching cell (3SSC-A), resulting in an alternative to the buck and buck-boost classical converters, respectively. The proposed topologies are part of a group of unexplored converters that employ the 3SSC-A, which has the advantages of 3SSC-based converters, such as high power density, reduced current stress on the semiconductors and suitable thermal loss distribution. In this regard, a complete static analysis is performed, including a detailed study of all semiconductor voltage and current efforts and developing loss models for each one. Moreover, by using simulation models, AC sweep analyses validate the dynamic frequency response of each converter’s small-signal models, and PI-based output–voltage closed-loop controllers are duly designed. Finally, the topologies are experimentally validated through the implementation of adequately designed prototypes, achieving efficiency values greater than 91% under several output power rates varying from 50% to 100%.

Keywords: buck converter; buck-boost converter; DC–DC converter; three-state switching cell (3SSC); 3SSC type-A

1. Introduction

The demand for step-down DC–DC converters with high power density, high efficiency, lower cost, and volume has progressively increased [1]. In this scenario, the development of these structures has been driven mainly by the evolution of electric and hybrid vehicles [2,3], electric aircraft [4], the implementation of smart grids [5], and application in equipment such as voltage regulator modules for microprocessors and data centers [6,7], battery chargers [8] and light-emitting diode lamps [9,10]. Although the classic step-down converters have a relatively simple structure and control system, in higher power processing applications, there is a significant current ripple, an increase in semiconductor conduction and switching losses, and a consequent reduction in the overall efficiency of the topology. In this context, researchers have focused on proposing alternatives to overcome the limitations of classic step-down converters, working mainly on the development of non-isolated architectures that, compared to isolated topologies, have the advantage of having higher power density, greater ease of adaptation to different loads and greater efficiency [11].

Therefore, the interleaved buck converters have been applied for point-of-load (POL), operating normally in hard-switching at low voltage and high current. These converters feature high power density and efficiency, fast transient response, reduced cost, and high...
reliability. Such advantages result from reducing the components’ current stress and cancelling current ripple in input EMI and output filters [12–14].

Despite the advantages mentioned, interleaved buck converters have high sensitivity to the phase errors present in interleaving control, which causes the current imbalance in the converter phases, resulting in the non-elimination of the current fundamental component from the switched operation and in the increase of the volume of the EMI filters. Closed-loop interleaving control can ensure current balance, but it requires that the compensators control the currents of each phase, increasing the control system’s complexity and the converter cost [13–16]. In open-loop interleaving control, the compensator regulates the current in one phase, and the same duty cycle and frequency control the other phase. This implementation is simpler, but small parametric variations between the circuit components, including those resulting from the layout design, cause imbalanced average currents in the phases [16].

Similar to interleaving solutions, the three-state switching cell (3SSC) was introduced in [17], being an interesting solution for increasing power density with a high-efficiency level and without the need for special control strategies. Since the 3SSC was proposed, a variety of topologies for DC–DC, AC–DC, and DC–AC converters have been presented in the literature [18–22]. All of these approaches present interesting advantages inherent to the application of the 3SSC, i.e., reduction of weight and volume of the filter elements, current stress division between the semiconductors, and distribution of the losses, providing the reduction of the heat-sinks size [23–25]. Although the 3SSC uses a high-frequency autotransformer, its dimensions are compact because that element operates in two quadrants of the B-H curve [26]. Furthermore, the operation of the autotransformer naturally doubles the frequency of the inductor current ripple and still ensures that the interleaved currents may be equalized without the need of an active balancer, which does not occur in the classic interleaved converter [22].

It is noteworthy that most of the applications with 3SSC mainly use the type-B cell (3SSC-B) topology [27]. It could be associated with the fact that the 3SSC-B-based buck, boost, and buck-boost converters have a static gain identical to the classic non-isolated converters in the whole range of duty cycle when they operate in continuous conduction mode (CCM).

Therefore, taking into account the reduced amount of research that employs the 3SSC-A and the advantages inherent to the 3SCC applications, this paper contributes to the detailed development and the experimental validation of the 3SSC-A-based buck and buck-boost converters, both operating as step-down DC–DC converters.

In this way, completing the initial study presented by the authors in [28], the proposed research fills a gap related to the exploration and implementation of the 3SSC-A-based DC–DC converters with the following contributions:

- A generalized and detailed static analysis of 3SSC-A-based buck and buck-boost DC–DC converters, including highlights of discontinuous conduction mode (DCM) and critical conduction mode (CRM).
- A complete theoretical and experimental validation of the loss model for both proposed structures, including a study of voltage and current stresses in semiconductors.
- Development and validation of small-signal equivalent models and verification of the dynamic response of the closed-loop control scheme by simulation results.
- A detailed experimental validation by implementing prototypes for each proposed converter, operating under several power ranges at the load side.

This paper is organized as follows: Section 2 describes the analysis of the converters, including loss models, dynamic models, and control systems design. Section 3 presents the experimental validations, which is followed by the final considerations.

2. The 3SSC-A-Based Buck and Buck-Boost: Static Analysis

Figure 1 illustrates the 3SSC-A-based buck and buck-boost converters, which consist of an autotransformer with two windings (T<sub>1</sub>, T<sub>2</sub>), two switches (S<sub>1</sub>, S<sub>2</sub>), two diodes (D<sub>1</sub>, D<sub>2</sub>),
one inductor (L), and one output capacitor (C_o) connected in parallel with the equivalent load (R_o). Similar to the 3SSC-A-based boost converter presented in [28], the 3SSC-A-based step-down topologies do not operate with a duty cycle equal to or greater than 0.5, as an overlap between the pulses will cause a short circuit between the autotransformer terminals through switches S_1 and S_2. Additionally, in this section, to analyze the operating principle of the converters, it is considered that both operate in a steady state and all components are ideal.

![Diagram of 3SSC-A-based buck and buck-boost converters](image)

**Figure 1.** Operation stages of 3SSC-A-based step-down converters: (a) First stage. (b) Second stage. (c) Third stage. (d) MDC only.

### 2.1. Operation Principle

The operation principle study of the 3SSC-A-based buck and buck-boost converters is accomplished under CCM, DCM and CRM, with the help of Figures 1–3. $V_{G_{S1,2}}$ are the gating signals for S_1 and S_2, which are 180° phase shifted. $i_{in}(t)$ is the input current. $i_{S1}(t)$ and $i_{D1}(t)$ are the currents in switch S_1 and diode D_1, respectively. $i_C(t)$ and $v_C(t)$ represent the current and voltage in the inductor. $v_{S1}(t)$ and $v_{D1}(t)$ are the voltages on switch S_1 and diode D_1, respectively. In addition, $i_o(t)$ is the load current and $i_{C_o}(t)$ is the current in the capacitor. It is noteworthy that the waveforms in Figures 2 and 3 are not on the same scale.

#### 2.1.1. CCM

The equivalent circuit stages in CCM and the main theoretical waveforms, defined according to four operation stages, are shown in Figures 1a–c, 2a,b, respectively.

**First Stage (t_0 < t < t_1)**

As shown in Figure 1a, during the first stage, the switch S_1 and diode D_2 are conducting. At this instant, the inductor L is storing energy. As the turns ratio of the autotransformer is unitary, this implies the proper balance of currents and voltages in its windings. For the 3SSC-A-based buck converter, the voltage on the windings $T_1$ and $T_2$ are equal to $V_{in} - V_o$. Meanwhile, for the 3SSC-A-based buck-boost structure, the voltage on the windings $T_1$ and $T_2$ are equal to $-V_{in}$.
Second Stage \( (t_1 < t < t_2) \)

As shown in Figure 1b, the second stage for both converters is characterized by the commutation of the diode \( D_1 \) to state on, while diode \( D_2 \) remains turned on. \( S_1 \) is turned off, and \( S_2 \) remains turned off. At this instant, the inductor \( L \) supplies energy to the load. Due to the short circuit between the terminals of windings \( T_1 \) and \( T_2 \), the magnetic flux in the autotransformer core is null.

Third Stage \( (t_2 < t < t_3) \)

The third stage is similar to the first stage, where the switch \( S_2 \) is turned on, and \( S_1 \) remains turned off. The diode \( D_1 \) remains turned on and \( D_2 \) is turned off. The equivalent circuits to the converters are shown in Figure 1c.

Fourth Stage \( (t_3 < t < T_s) \)

This stage is identical to the second stage, as shown in Figure 1b, where the current through the inductor \( L \) flows through the diodes \( D_1, D_2 \), and the autotransformer windings.

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**Figure 2.** 3SSC-A-based step-down converters waveforms in CCM: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.
According to the waveforms presented in Figure 2a,b, it is verified that the current in the inductor does not become zero in any operating stage, thus characterizing the CCM. Although the operating principle of the converters is similar, the arrangement of the elements in each structure changes the maximum voltage stress to which the semiconductors are subjected. In the 3SSC-A-based buck converter, the maximum voltage blocking of the semiconductors has a module equal to $2(V_{in} - V_o)$. Meanwhile, for the 3SSC-A-based buck-boost structure, the maximum voltage stress in the semiconductors has a module equal to $2V_{in}$.

![Figure 3. 3SSC-A-based step-down converters waveforms in DCM: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.](image)

2.1.2. DCM

In this operating mode, the converters have six operating steps, with the respectively equivalent waveforms shown in Figure 3a,b. Some of the operation stages in DCM are equivalent to the CCM, and these will not be described in detail.
First Stage \( (t_0 < t < t_1) \)
This stage is identical to the first stage in CCM.

Second Stage \( (t_1 < t < t_2) \)
This stage is identical to the second stage when the converters are operating in CCM.

Third Stage \( (t_2 < t < t_3) \)
As shown in Figure 1d, in this stage, the current in the inductor becomes zero, the switches remain turned off, and diodes are turned off. Thus, only the output capacitor \( C_0 \) supplies energy to the load.

Fourth Stage \( (t_3 < t < t_4) \)
This operation stage is identical to the third stage of the CCM.

Fifth Stage \( (t_4 < t < t_5) \)
This operation stage is identical to the fourth stage of the CCM.

Sixth Stage \( (t_5 < t < T_s) \)
This stage of operation is identical to the third stage of the DCM.

In Figure 3a,b, it is verified that the current in the inductor is null during the third and sixth operation stages, characterizing the DCM. Additionally, in this operating mode, the semiconductors of the respective converters are subjected to the same voltage stresses presented in the CCM.

2.1.3. CRM
In this mode, maintaining the 180-degree delay, each switch is turned on at the exact moment when the current in the inductor becomes null, causing the current increases again. The inductor current becomes null every half-time, so the minimum current \( I_m \) is equal to zero, and the current ripple \( \Delta I_L \) in the inductor is equal to its maximum current \( I_M \). The first and second operation stages in CRM are equivalent to the first and second stages in DCM, respectively.

2.1.4. Output Characteristic of the Converters
The static gain expressions for the converters operating in CCM, DCM, and CRM are presented in Table 1.

Table 1. Static Gain.

| Static Gain | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|-------------|-------------------|------------------------|
| \( G_{CCM} \) | \( \frac{2D}{1 + 2D} \) | \( \frac{2D}{D^2} \) |
| \( G_{DCM} \) | \( \frac{\gamma + D^2}{1} \) | \( \frac{\gamma + 2D^2}{\gamma^2 + 2D^2} \) |
| \( G_{CRM} \) | \( \frac{1}{1 + \left( \frac{1}{2} \right)} \) | \( \frac{1}{2} \pm \frac{1}{\sqrt{16 - \gamma}} \) |

Here, \( I_o \) is the average output current, \( f_s \) is the switching frequency, \( D \) is the duty cycle, and \( \gamma \) represents the normalized output current, defined in (1).

\[
\gamma = \frac{L_i f_s}{V_m}
\]  

From the equations in Table 1, the static gain curves of the proposed converters are presented in Figure 4. Analogously to the classic buck and buck-boost converters, the
output voltage of the converters under analysis is also a function of the load current in DCM. For the 3SSC-A-based buck converter, the maximum static gain in CRM occurs at $\gamma = 0.0625$ and $D = 0.25$. In contrast, for the classic buck converter, the maximum static gain in CRM is verified when $\gamma = 0.25$ and $D = 0.5$. So, this implies that the CCM region is wider for the 3SSC-A-based buck structure, so the inductance becomes $1/4$ of that required for the classic buck converter for the same operating point.

![Figure 4](imageURL)

**Figure 4.** Comparison between the static gain curves of classic converters and 3SSC-A-based step-down converters: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.

Making the same analogy with the 3SSC-A-based buck-boost converter, the maximum static gain in CRM also occurs at $\gamma = 0.0625$ and $D = 0.25$. Whereas, for the classic buck-boost converter, the maximum static gain in CRM is verified when $\gamma = 0.125$ and $D = 0.5$. Therefore, the CCM region is also wider for the 3SSC-A-based buck-boost structure, requiring only half the inductance required by the classic buck-boost converter. Additionally, contrasting the two proposed topologies, it is verified that the CCM region is larger for the 3SSC-A-based buck-boost converter, with maximum voltage gain equal to unity, while the 3SSC-A-based buck structure reaches only half.

### 2.1.5. Filter Elements

From the steady-state analysis presented earlier, applying Kirchhoff’s voltage law to the equivalent circuits of Figure 1a, the equation relating the duty cycle and the current ripple $\Delta I_L$ in the inductors is obtained and exhibited in the following expressions for the 3SSC-A-based buck and buck-boost converters:

$$\Delta I_L = \frac{(1 - 2D)V_{in}}{2L_{f_S}}$$

The normalized current ripple $\overline{\Delta I_L}$ for the 3SSC-A-based buck and buck-boost converters is given by Equations (3) and (4), respectively. These expressions are plotted in Figure 5, where it can be seen that the maximum value for the 3SSC-A-based buck converter occurs at $D = 0.25$, while for the 3SSC-A-based buck-boost structure, it occurs at $D = 0.2072$.

$$\overline{\Delta I_{L3SSCA-buck}} = \frac{L_{f_S}\Delta I_L}{V_{in}} = \frac{(1 - 2D)(1 + 2D)}{(1 + 2D)}$$

$$\overline{\Delta I_{L3SSCA-buck-boost}} = \frac{L_{f_S}\Delta I_L}{V_{in}} = (1 - 2D)$$

Compared to the 3SSC-A-based buck-boost converter, the 3SSC-A-based buck structure shows lower overall inductor current ripple; consequently, considering the same operating point, it will result in lower inductor losses.
Figure 5. Ripple current through the inductor.

The inductance $L$ for the two converters is determined by reorganizing (2), according to (5).

$$L = \frac{(1-2D)V_o}{2\Delta I_L f_s}$$

(5)

The critical inductance $L_{\text{crit}}$ that corresponds to the threshold value of inductance between CCM and DCM is described in (6). From Figure 4, for both converters, the threshold value of $\gamma$ is 0.0625, and the critical inductance is calculated by replacing this value in (1).

$$L_{\text{crit}} = \frac{V_i}{\gamma_{\text{thr}} I_{o_s}} = \frac{V_i}{16 I_{o_s} f_s}$$

(6)

By using the voltage ripple equation, the value of output capacitor $C_o$ can be obtained as follows:

$$C_{3\text{SSC}-\text{Buck}} \geq D \left( \frac{1-2D}{1+2D} \right) \frac{P_o}{V_o \Delta V_o f_s}$$

(7)

$$C_{3\text{SSC}-\text{Buck-Boost}} \geq \frac{1-2D}{32} \frac{V_o}{L f_s^2 \Delta V_o}$$

(8)

where $\Delta V_o$ is the voltage ripple of the capacitor.

2.2. Autotransformer Design

For the autotransformer design procedure, the same methodology presented in [28] is considered, starting with an equation that defines the core product $A_e A_w$ as a function of the electromagnetic parameters of the converter.

2.3. Component Voltage and Current Stresses in CCM

Table 2 summarizes the current efforts on the magnetic components and on the capacitor of the proposed converters.

| Parameter | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|-----------|-------------------|------------------------|
| RMS value of $T_1$-$T_2$ current ($I_{T RMS}$) | $\sqrt{\frac{1}{12} (1+6D) \left( \frac{\Delta I_L}{4} + 3 \left( \frac{I_o}{1+2D} \right)^2 \right)^2}$ | $\sqrt{\frac{1}{12} (1+6D) \left( \frac{3\Delta I_L^2}{4} \right)}$ |
| Avg value of $T_1$-$T_2$ current ($I_{T AVG}$) | $\frac{I_o}{2}$ | $\frac{(1+2D)I_o}{2}$ |
| RMS value of $L$ current ($I_{L RMS}$) | $\sqrt{\left( \frac{I_o}{1+2D} \right)^2 + \frac{\Delta I_L^2}{12}}$ | $\sqrt{\frac{I_o^2 + \Delta I_L^2}{12}}$ |
| Avg value of $L$ current ($I_{L AVG}$) | $\frac{I_o}{1+2D}$ | $I_o$ |
| RMS value of $C_o$ current ($I_{C RMS}$) | $\sqrt{2D(1-2D)I_o^2 + (1+6D)\frac{\Delta I_L^2}{12}}$ | $\sqrt{\frac{\Delta I_L^2}{12}}$ |
Table 3 summarizes the maximum voltage stress across all power semiconductors during a period of operation of the 3SSC-A-based buck and buck-boost converters.

Table 3. Voltage Stress across Semiconductors.

| Parameter | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|-----------|-------------------|------------------------|
| Maximum Voltage in $S_{1-2}$ ($V_{S_{\text{max}}}^{\text{Sat}}$) | $2(V_{in} - V_o)$ | $2V_{in}$ |
| Maximum Voltage in $D_{1-2}$ ($V_{D_{\text{max}}}^{\text{Sat}}$) | $-2(V_{in} - V_o)$ | $-2V_{in}$ |

From the perspective of equivalent operating points, comparing the topologies proposed in Table 3, it can be seen that the semiconductors of the 3SSC-A-based buck-boost converter are subject to higher voltage stress. The average and RMS values of the switches and diodes currents are shown in Table 4.

Table 4. Average and RMS Semiconductors Currents for 3SSC-A-based Buck and Buck-Boost converters.

| Parameter | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|-----------|-------------------|------------------------|
| RMS value of $S_{1-2}$ current ($I_{S_{\text{avg}}}^{\text{RMS}}$) | $\sqrt{D \left( \frac{l_o}{1+2D} \right)^2 + \frac{\Delta I^2}{12}}$ | $\sqrt{D \left( \frac{l_o}{1+2D} + \frac{\Delta I^2}{12} \right)}$ |
| Avg value of $S_{1-2}$ current ($I_{S_{\text{avg}}}^{\text{Avg}}$) | $\frac{D I_o}{1+2D}$ | $DI_o$ |
| RMS value of $D_{1-2}$ current ($I_{D_{\text{avg}}}^{\text{RMS}}$) | $\frac{l_o}{2(1+2D)} \left( 1 + \frac{3}{4} \left( \frac{I_o}{1+2D} \right)^2 + \frac{\Delta I^2}{4} \right)$ | $\frac{l_o}{2} \left( 1 + \frac{3}{4} \left( \frac{I_o}{1+2D} + \frac{\Delta I^2}{12} \right) \right)$ |
| Avg value of $D_{1-2}$ current ($I_{D_{\text{avg}}}^{\text{Avg}}$) | $\frac{f_s}{2} I_{D_{\text{peak}}} (t_{on} + t_{off})$ | $f_s I_{D_{avg}}$ |

2.4. Power Losses

The power losses in the proposed converters can be divided into five main groups: (I) conduction ($P_{S_{\text{(cond)}}}$) and switching ($P_{S_{\text{(sw)}}}$) losses in the switches, (II) conduction ($P_{D_{\text{(cond)}}}$) and reverse recovery ($P_{D_{\text{(sw)}}}$) losses in the diodes, (III) ohmic ($P_{TC_{\text{opper}}}$) and core losses ($P_{Tcore}$) in the autotransformer, (IV) ohmic ($P_{Lcopper}$) and core losses ($P_{Lcore}$) in the inductor and (V) capacitor losses ($P_{C}$). Such losses are described following the methodology presented in [28]; therefore, the set of equations to calculate the theoretical losses of the converters is given by:

\[
P_{S_{\text{(cond)}}} = V_{CE_{\text{(sat)}}} I_{S_{AVG}} \tag{9}
\]

\[
P_{S_{\text{(sw)}}} = \frac{f_s}{2} V_{CE_{\text{(max)}}} I_{S_{\text{peak}}} (t_{on} + t_{off}) \tag{10}
\]

\[
P_{D_{\text{(cond)}}} = V_F I_{D_{AVG}} + R_D I_{D_{RMS}}^2 \tag{11}
\]

\[
P_{D_{\text{(sw)}}} = \frac{f_s}{2} t_{rr} I_{1} V_{D_{\text{(max)}}} \tag{12}
\]

\[
P_{TC_{\text{opper}}} = \frac{2 \rho_{cu} I_{D_{RMS}}^2}{n A_{cu}} \tag{13}
\]

\[
P_{Tcore} = P_{Lcore} = 4 k (2 f_s)^a B_p^b M_{core} \tag{14}
\]

\[
P_{Lcopper} = \frac{\rho_{cu} I_{D_{RMS}}^2}{n A_{cu}} \tag{15}
\]
\[ P_C = I_{CRMS}^2 \times ESR \]  \hspace{1cm} (16)

where these losses are calculated by using the following variables: peak of the current switch \((I_{\text{peak}})\), collector–emitter saturation voltage \((V_{CE(sat)})\), turn-on \((t_\text{on})\) and turn-off \((t_\text{off})\) switching times, forward voltage \((V_F)\), dynamic resistance \((R_D)\), reverse recovery time \((t_{rr})\), maximum instantaneous reverse current \((I_r)\), copper resistivity constant \((\rho_{cu})\), length of winding \((l_{wdg})\), number of litz wires \((n)\), core cross-sectional \((A_{cu})\), equivalent series resistance \((ESR)\), core mass \((M_{core})\) and half of the peak AC flux density \((B_{pk})\). In addition, for the magnetic losses, \(k\), \(\alpha\), and \(\beta\) are extracted from the core losses per volume based on the value of flux density and frequency from the datasheet provided by the manufacturer.

2.5. Transfer Function and Control Design

For the analysis of the dynamic characteristics of the proposed converters, aiming at the implementation of the linear control techniques, the AC modeling approach proposed by [29] was applied. Considering the CCM operation stages presented in Section 2.1.1, the output voltage and the inductor current are denoted together by the state vector \(x(t) = [i_L(t) \ v_o(t)]\). Therefore, from the temporal dynamics of the 3SSC-A-based buck structure, (17) and (18) are obtained.

\[
\frac{dx(t)}{dt} = \begin{bmatrix}
0 & -\frac{2}{L} & 1 \\
\frac{2}{C_o} & -\frac{1}{R_oC_o} & 0
\end{bmatrix} x(t) + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}(t) \tag{17}
\]

during \(t_0 < t < t_1\) and \(t_2 < t < t_3\).

\[
\frac{dx(t)}{dt} = \begin{bmatrix}
0 & -\frac{1}{L} \\
\frac{1}{C_o} & -\frac{1}{R_oC_o} & 0
\end{bmatrix} x(t) + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}(t) \tag{18}
\]

during \(t_1 < t < t_2\) and \(t_3 < t < T_s\).

Likewise, from the temporal dynamics of the 3SSC-A-based buck-boost converter, (19) and (20) are obtained.

\[
\frac{dx(t)}{dt} = \begin{bmatrix}
0 & -\frac{1}{L} \\
\frac{1}{C_o} & -\frac{1}{R_oC_o} & 0
\end{bmatrix} x(t) + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}(t) \tag{19}
\]

during \(t_0 < t < t_1\) and \(t_2 < t < t_3\).

\[
\frac{dx(t)}{dt} = \begin{bmatrix}
0 & -\frac{1}{L} \\
\frac{1}{C_o} & -\frac{1}{R_oC_o} & 0
\end{bmatrix} x(t) + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{in}(t) \tag{20}
\]

during \(t_1 < t < t_2\) and \(t_3 < t < T_s\).

For (17)–(20), by applying the state-space average modelling method, and considering \(D' = (0.5 - D)\), matrix \(A\), \(B\) and \(C\) are obtained for each proposed converter as follows:

- **3SSC-A-based buck:**

\[
A = \begin{bmatrix}
0 & \frac{1 + 2D}{L} \\
\frac{1 + 2D}{C_o} & -\frac{1}{R_oC_o}
\end{bmatrix}; B = \begin{bmatrix} \frac{2D}{L} \\ \frac{1}{L} \end{bmatrix}; C = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{21}
\]
3SSC-A-based buck-boost:

\[ A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} \end{bmatrix}; \quad B = \begin{bmatrix} 0 \\ \frac{2D L}{L} \end{bmatrix}; \quad C = [0 \ 1] \quad (22) \]

Thus, using the small-signal perturbations and linearizing around the equilibrium point, the small-signal AC equivalent circuit of the converters was obtained, as shown in Figure 6. From this circuit, the control-to-output transfer function of the converters is obtained and described by (23) and (24), whose validation by the AC sweep analysis performed in the PSIM software (UNESP, Ilha Solteira, Brazil) is shown in Figures 7a and 8a.

\[ G_{v_{\text{d}}buck}(s) = \frac{V_o}{(1+2D)D} \left( 1 + s \frac{2DL}{(1+2D)^2 R_o} \right) \frac{C_o L}{(1+2D)^2} + s \frac{L}{(1+2D)^2 R_o} + 1 \quad (23) \]

\[ G_{v_{\text{d}}buck-boost}(s) = \frac{2V_{in}}{s^2 L C_o + s\frac{L}{R_o} + 1} \quad (24) \]

**Figure 6.** Small-signal AC equivalent circuit of the proposed step-down converters: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.

Analyzing the transfer function \( G_{v_{\text{d}}}(s) \) of the 3SSC-A-based buck converter, we can see the presence of two poles and a zero, all in the left-half plane, characterizing a system of minimum phase. Unlike the \( G_{v_{\text{d}}}(s) \) transfer functions of the classic buck and 3SSC-B-based buck converters, the presence of the zero in the 3SSC-A-based buck structure equation promotes a phase advance, making the step response of the less oscillatory system. Additionally, the absence of right-half-plane (RHP) zeros allows the controller design for the 3SSC-A-based buck converter to be simplified, making it possible to obtain a satisfactory dynamic response without needing additional control loop implementation.
The transfer function $G_{vd}(s)$ of the 3SSC-A-based buck-boost structure is identical to that of the 3SSC-A-based boost [28] topology, thus presenting the characteristic of a minimum phase system due to the absence of right-half-plane zeros. In this way, as mentioned for the 3SSC-A-based buck converter, the implementation of the control design for the 3SSC-A-based buck-boost structure also becomes simplified. Additionally, it is observed that the 3SSC-A-based buck-boost topology has dynamic characteristics that differ from the classic buck-boost and 3SSC-B buck-boost converters [30]. However, the dynamic response is similar to that presented by the classical buck structure operating in CCM, which is mathematically proven by the transfer function expressed in (24).

With the voltage loop transfer functions obtained, the voltage compensators were designed to guarantee satisfactory stability margins both in terms of gain and phase. Thus, using the design specifications in Table 5, the frequency analysis for each $G_{vd}H$ are illustrated in Figures 7b and 8b (blue curve), which include the sensor gains $H = 5.21 \times 10^{-2}$ V/V and $H = 26 \times 10^{-3}$ V/V, respectively. To regulate the output voltage of the converters, a voltage control loop was implemented by using PI controllers, which were tuned according to the conventional criteria of phase and gain margin ($0.25f_s \leq f_c \leq 10f_s$ and $45 \leq PM \leq 90$) to provide a good response with adequate output voltage overshoot and ensures the stability of the converters during the load step. For the 3SSC-A-based buck converter, as shown in Figure 7b (orange curve), the PI controller was designed with proportional gain $K_p = 0.08$ and integral gain $K_i = 2223$, resulting in a voltage control loop with a frequency of 5 kHz crossover and 57º phase margin. Meanwhile, for the 3SSC-A-based buck-boost structure, as shown in Figure 8b (orange curve), a PI controller with $K_p = 0.095$ and $K_i = 1399$ was implemented, obtaining a voltage control loop with frequency crossover and phase margin of 5 kHz and 62º, respectively.

![Figure 7. Frequency analysis of 3SSC-A-based buck converter: (a) Validation of transfer function $G_{vd}(s)$; (b) Open-loop transfer-function.](image-url)
Figure 8. Frequency analysis of 3SSC-A-based buck-boost converter: (a) Validation of transfer function $G_{vd}(s)$; (b) Open-loop transfer-function.

| Table 5. Design specifications. |
|---------------------------------|
| **Parameter** | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
| **Input Voltage ($V_{in}$)** | 180 V | 180 V |
| **Output Voltage ($V_{o}$)** | 48 V | 96 V |
| **Output Power ($P_{o}$)** | 300 W | 600 W |
| **Switching Frequency ($f_s$)** | 50 kHz | 50 kHz |
| **Current Ripple ($\Delta I_o$)** | 0.15$I_o$ | 0.15$I_o$ |
| **Voltage Ripple ($\Delta V_o$)** | 0.065$V_o$ | 0.0055$V_o$ |
| **Inductor ($L$)** | 180 μH, core NEE-42/21/15-IP12 by Thornton, N = 41 turns, $L = 7 \times \text{AWG} 25$. | 180 μH, core NEE-55/28/21-IP12 by Thornton, N = 31 turns, $L = 11 \times \text{AWG} 26$. |
| **Capacitor ($C_o$)** | 4.7 μF/630 V, metal polyester film capacitor, $E_R S = 1.5 \text{m} \Omega$. | 2.2 μF/630 V, metal polyester film capacitor, $E_R S = 3.3 \text{m} \Omega$. |
| **Load ($R_s$)** | 7.68 Ω | 15.36 Ω |
| **Switches $S_1$−$S_2$** | $N_p/N_s = 1$, core NEE-42/21/20-IP12 by Thornton, N = 19 turns, $L = 6 \times \text{AWG} 26$. | $N_p/N_s = 1$, core NEE-55/28/21-IP12 by Thornton, N = 19 turns, $L = 9 \times \text{AWG} 26$. |
| **Diodes $D_1$−$D_2$** | IGBT FGH20N60SFD, $I_C = 20 \text{A}$, $V_{CE} = 600 \text{V}$, by FAIRCHILD, $I_{on} = 29 \text{ns}$, $I_{off} = 114 \text{ns}$, $V_{CEO} = 4.93 \text{A}$, $V_{CE(off)} = 2.4 \text{V}$, $V_{CE(max)} = 132 \text{V}$. | IGBT FGH20N60SFD, $I_C = 20 \text{A}$, $V_{CE} = 600 \text{V}$, by FAIRCHILD, $I_{on} = 29 \text{ns}$, $I_{off} = 114 \text{ns}$, $V_{CEO} = 6.72 \text{A}$, $V_{CE(off)} = 2.4 \text{V}$, $V_{CE(max)} = 180 \text{V}$. |

2.6. Comparison with Classic Topologies

Table 6 compares the proposed step-down converters and the classic topologies. Unlike classical converters, 3SSC-A-based step-down converters have a three-state switching cell arrangement, resulting in more components. However, this configuration allows proper current sharing between the semiconductors, reducing current efforts and power losses.
and increasing power processing capacity. Another interesting aspect is the reduced size of energy storage elements in the proposed converters, since these components operate with twice the switching frequency, contributing to the decrease in weight and volume of the structures. Furthermore, even at higher power levels, this feature allows using only film capacitors, which is convenient as they have a longer lifespan, contrasting with the classical topologies that often rely on electrolytic capacitors.

The static gain of the 3SSC-A-based buck converter has non-linear characteristics and is limited to half the input voltage, differing from the gain of the classical buck structure. In contrast, the 3SSC-A-based buck-boost topology has a linear static gain with a maximum value of unity. Regarding voltage stresses, 3SSC-A-based step-down converters present higher voltage stress on switches. On the other hand, the switches are in the same reference and in the common point of the source, which can provide simpler control circuits (non-isolated drivers).

In addition to the characteristics presented in Table 6, the minimum phase system property given by the transfer function $G_{vd}(s)$ of the 3SSC-A-based step-down converters is unlike the transfer function $G_{vd}(s)$ of the buck structure-boost classic, which features a zero right-half-plane. In this way, the controller design for 3SSC-A-based step-down topologies becomes simplified, making it possible to obtain a satisfactory dynamic response without needing an additional control loop.

### Table 6. Comparison among 3SSC-A-based step-down DC–DC converters and the classical topologies in CCM.

| Parameter                  | Classic Buck | Classic Buck-Boost | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|----------------------------|--------------|--------------------|-------------------|-------------------------|
| Static gain                | $D$          | $D$                | $2D$              | $2D$                    |
| Voltage stress on the      | $V_o$        | $V_i + V_o$        | $2(V_i - V_o)$    | $2V_i$                  |
| switches                   |              |                    |                   |                         |
| # Switches                 | 1            | 1                  | 2                 | 2                       |
| # Diodes                   | 1            | 1                  | 2                 | 2                       |
| Autotransformer            | -            | -                  | 1                 | 1                       |
| # Capacitors               | 1            | 1                  | 1                 | 1                       |
| # Inductors                | 1            | 1                  | 1                 | 1                       |
| Ripple frequency of $i_L$  | $f_s$        | $f_s$              | $2f_s$            | $2f_s$                  |
| Ripple frequency of $i_C$  | $f_s$        | $f_s$              | $2f_s$            | $2f_s$                  |
| Duty cycle range           | $0 < D < 1$  | $0 < D < 0.5^*$    | $0 < D < 0.5$     | $0 < D < 0.5$           |

*Duty cycle limited to the step-down operation.*

### 3. Experimental Results

The two proposed converters were designed according to the specifications presented in Table 5, following the design methodology developed in CCM. The experimental set-up implemented for carrying out the laboratory tests is shown in Figure 9, with details for the power circuit of the converters.

The main experimental waveforms of the 3SSC-A-based buck converter are shown in Figure 10. Figure 10a shows the waveforms of the control signals from switches $S_1$ and $S_2$, current $i_{S1}$ and voltage $v_{S1}$. These results indicate that the converter operates with $D = 0.18$ without overlapping the switches’ command signals. Furthermore, it can be verified that the maximum voltage $v_{S1}$ on the switches is approximately 264 V, which can allow the implementation of components with voltage $V_{CE}$ in the range of 300 V. The current $i_{S1}$ grows linearly up to 5 A. Complementarily, Figure 10b presents the waveforms of voltage and current stress in switches $S_1$ and $S_2$. It is observed that the switches do not conduct simultaneously, evidencing a delay of 180° between the control signals. As with the 3SSCA-based boost topology, the resonance between the leakage inductance of the autotransformer and the collector-emitter capacitance of the IGBT causes the current peaks observed in the currents $i_{S1}$ and $i_{S2}$ during the switching turn-on. However, these peaks were minimized with snubber RLD circuits, mitigating the voltage peaks in the switches.
**Figure 9.** Experimental set-up of the 3SSC-A-based step-down converters: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.

**Figure 10.** 3SSC-A-based buck experimental results at full load (time: 5 μs/div): (a) $v_{S1}$ (200 V/div); $i_{S1}$ (5 A/div); $V_{GS1}$ (20 V/div); $V_{GS2}$ (20 V/div); (b) $v_{S1}$ (200 V/div); $v_{S2}$ (200 V/div); $i_{S1}$ (5 A/div); $i_{S2}$ (5 A/div); (c) $v_{D1}$ (200 V/div); $i_{D1}$ (5 A/div); $i_L$ (2 A/div); $i_{S1}$ (5 A/div); $i_{S2}$ (5 A/div); (d) $v_o$ (100 V/div); $i_L$ (5 A/div); $v_{in}$ (100 V/div); $i_{in}$ (5 A/div).
In Figure 10c, voltage $v_{D1}$, currents $i_L$, current $i_{D1}$ and current $i_{S1}$ are shown. The diodes’ voltage stress is around $-264$ V, which confirms the theoretical analysis. Analyzing the currents $i_{S1}$ and $i_{D1}$, it is verified that the switch $S_1$ and the diode $D_1$ operate in a complementary way, evidencing that they do not conduct simultaneously. In addition, observing the waveform of the current $i_L$, it is verified that the converter operates in CCM, with a current ripple at 100 kHz, that is, twice the switching frequency of the switches with an average value of 4.6 A. Additionally, it can be seen that diodes $D_1$ and $D_2$ conduct simultaneously when the current $i_L$ decreases linearly, that is, the current through each diode is equivalent to half the inductor current at this instant, with an average value of 2.3 A. Therefore, due to the characteristic of 3SSC, the division of current efforts between these semiconductors naturally occurs.

Figure 10d shows the waveforms of input current $i_{in}$, current $i_L$ and voltages $V_{in}$ and $V_o$. These results demonstrate the characteristic of the converter operating as a voltage step-down, with an average output voltage $V_o$ at 48 V, according to the desired voltage gain. Similar to the classic buck converter, the 3SSC-A-based buck structure generates a pulsating ripple current $i_{in}$ with high $d_i/d_t$. In addition, the voltage $V_o$, and the currents $i_1$ and $i_{in}$ present a ripple corresponding to twice the switching frequency of the switches, an intrinsic characteristic of the three-state switching cell, which allows the reduction of weight and volume of the energy storage elements of this structure.

In the same way as the one presented for the 3SSC-A-based buck converter, Figure 11 illustrates the main results obtained during the experimental validation of the 3SSC-A-based buck-boost structure. The waveforms of control signals from switches $S_1$ and $S_2$, voltage $v_{S1}$ and current $i_{S1}$ are shown in Figure 11a. Observing the gate pulses, it is verified that the converter operates without overlapping the command signals, with $D = 0.27$. The $v_{S1}$ voltage stress on switch $S_1$ is 360 V, which is higher than that presented by the 3SSC-A-based buck converter. In a complementary way, Figure 11b illustrates the current and voltage stress in switches $S_1$ and $S_2$, demonstrating that these semiconductors do not remain in conduction simultaneously, with the 180° delay between the command signals being evident. As in the 3SSC-A-based boost and 3SSC-A-based buck topologies, the interaction between the leakage inductance of the autotransformer and the collector–emitter capacitance of the IGBT results in current peaks observed in currents $i_{S1}$ and $i_{S2}$ during the activation of switches, which is a characteristic of the 3SSC-A in these configurations. However, these peaks were also reduced in the 3SSC-A-based buck-boost structure by introducing RLD snubber circuits.

The waveforms of voltage $v_{D1}$, current $i_L$ and currents $i_{D1}$ and $i_S$ are illustrated in Figure 11c. The diodes are subjected to voltage stress equivalent to twice the voltage $V_{in}$, that is, $-360$ V. Analyzing the currents $i_{S1}$ and $i_{D1}$, it is verified that switch $S_1$ and diode $D_1$ do not operate simultaneously, evidencing the complementary operation between these semiconductors. In addition, the current $i_L$ has a ripple frequency equivalent to 100 kHz, that is, twice the switching frequency, with an average value of 6.25 A, and its format indicates that the converter operates in CCM. Additionally, as in other 3SSC-A-based converters, it is verified that diodes $D_1$ and $D_2$ conduct simultaneously when the switches are off, with the current through each of these semiconductors corresponding to half the current $i_L$, with a value average of 3.1 A; therefore, there is a division of the current stresses.

The waveforms of voltage $V_{in}$, voltage $V_o$, current $i_L$ and input current $i_{in}$ are shown in Figure 11d. These results confirm the step-down characteristic of the converter, with $V_o$ at 96 V. Analogously to the classical buck-boost and 3SSC-A-based buck structures, the current $i_{in}$ of the 3SSC-A-based buck-boost converter also shows a pulsating ripple with high $d_i/d_t$. However, in contrast to the classic buck-boost converter, the 3SSC-A-based buck-boost structure has an inductor connected to the output, presenting reduced current ripple, as can be seen in $i_L$, which considerably decreases the RMS current in the output capacitor. Additionally, still, through Figure 11d, it can be seen that both currents $i_L$ and $i_{in}$, as well as voltage $V_o$ present ripple equivalent to twice the switching frequency, which allows weight reduction and volume of energy storage elements.
Figure 11. 3SSC-A-based buck-boost experimental results at full load (time: 5 μs/div): (a) $v_{S1}$ (200 V/div); $i_{S1}$ (10 A/div); $V_{GS1}$ (20 V/div); $V_{GS2}$ (20 V/div); (b) $v_{S1}$ (200 V/div); $v_{S2}$ (200 V/div); $i_{S1}$ (10 A/div); $i_{S2}$ (10 A/div); (c) $v_{D1}$ (200 V/div); $i_{D1}$ (5 A/div); $i_{L}$ (5 A/div); $i_{S1}$ (5 A/div); (d) $v_o$ (100 V/div); $i_o$ (2 A/div); $v_{in}$ (100 V/div); $i_{in}$ (5 A/div).

Figure 12 presents the closed-loop operation of the converters. As can be seen in the experimental results of the 3SSC-A-based buck converter in Figure 12a, the output voltage remains at 48 V for the load steps from 100% power to 50% and from 50% to 100%. Similarly, the same load percentage variation was applied to the 3SSC-A-based buck-boost structure, its dynamic response being shown in Figure 12b, and it can be verified that the output bus is maintained at 96 V.

Figure 12. Dynamic responses of the converters (time: 200 ms/div): (a) 3SSC-A-based buck: $v_o$ (50 V/div); $i_{D1}$ (5 A/div); $i_o$ (2 A/div); $i_o$ (5 A/div); (b) 3SSC-A-based buck-boost: $v_o$ (50 V/div); $i_{D1}$ (5 A/div); $i_o$ (2 A/div).
According to the theoretical model described in Section 2.4 and the parameters in Tables 5 and 7, Figure 13 presents the distribution of power losses in converters operating at full load. The total power losses for the 3SSC-A-based buck and 3SSC-A-based buck-boost topologies are approximately 29.3 W and 50.3 W, with a theoretical efficiency of about 91.1% and 92.3%, respectively. It can be observed that in both converters, even with different operating points, the losses in the switches are dominant, contributing to a higher percentage of the total losses. In addition, the converter capacitors’ power loss is highly reduced compared to the other elements.

The efficiency of the experimental prototypes was evaluated in a load range from 16.67% to 100% of the rated load. Figure 14 presents the normalized practical efficiency of the proposed converters. Both prototypes present performance superior to 85% in the entire defined power range, highlighting, at rated load, the efficiency of approximately 91% for the 3SSC-A-based buck converter and 92% for the 3SSC-A-based buck-boost structure. In contrast to Figure 13, the measured losses at nominal power are practically identical to the calculated losses. Therefore, there is an experimental validation of the theoretical losses model.

![Figure 13](image13.png)

Figure 13. Power loss estimation at full load in percentage: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.

| Component                 | 3SSC-A-Based Buck | 3SSC-A-Based Buck-Boost |
|---------------------------|-------------------|------------------------|
| Switches ($S_1-S_2$)      | 8.65 W            | 16.65 W                |
| Diodes ($D_1-D_2$)        | 7.66 W            | 11.02 W                |
| Autotransformer ($T$)     | 5.86 W            | 10.76 W                |
| Inductor ($L$)            | 7.1 W             | 11.88 W                |
| Capacitor ($C_o$)         | 7.5 mW            | 0.23 mW                |
| Total                     | 29.3 W            | 50.3 W                 |

![Figure 14](image14.png)

Figure 14. Experimental efficiency curve of the converters.
A thermal image of the converters operating at full load is shown in Figure 15. This result also validates the characterization of losses shown in Figure 13, proving the distribution of thermal losses between the components caused by the division of current efforts between the semiconductors and, consequently, validating the potential benefits of the application of 3SSC-A in terms of improving the thermal performance in power processing.

![Thermal image of the converters at full load: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.](image)

**Figure 15.** Thermal image of the converters at full load: (a) 3SSC-A-based buck; (b) 3SSC-A-based buck-boost.

### 4. Conclusions

In this paper, two unexplored topologies based on 3SSC-A for step-down applications were thoroughly analyzed, implemented and experimentally verified. According to the experimental validations, the proposed converters present several advantages compared with the classical topologies, such as reducing current stress between the semiconductors, distribution of power losses between these components, and reducing heat sinks. In addition, the energy storage elements of these topologies operate at twice the switching frequency, allowing weight and volume reduction and, consequently, increased power density. The 3SSC-A-based buck-boost structure presents less current ripple at the load side since the inductor is directly coupled to the output, reducing the RMS current over the capacitor. However, the 3SSC-A-based buck converter presents less voltage stress over the semiconductors. Furthermore, the 3SSC-A-based buck converter has a maximum static gain of half the input voltage, while the theoretical maximum static gain of the 3SSC-A-based buck-boost topology equals the input voltage.

Detailing the loss distribution effects, one can note that the losses in the inductors and autotransformers are very close for the two converters. Table 2 indicates that the current stresses on these magnetic elements are higher for the 3SCC-A-based buck-boost converter, which would result in a relative increase in copper losses. However, the design specifications presented in Table 5 indicate that the inductor and autotransformer winding resistances are lower for the 3SCC-A-based buck-boost converter, which justifies the balance of this losses portion between the two topologies. The losses proportion in the switches is slightly higher for the 3SCC-A-based buck-boost converter due to the higher relative current stresses indicated in Table 4.

Therefore, the power loss characterization of the proposed converters allowed us to conclude that the switches contribute significantly to the power losses of the 3SSC-A converters. Moreover, although the converters were projected at different operating points, both presented a similar power loss distribution with high efficiency, which was around 91% for the 3SSC-A-based buck converter and 92% for the 3SCC-A-based buck-boost converter. Thus, it is up to the designer to analyze the figures of merit of each converter as a starting point for selecting the most suitable topology for a specific application.
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