Coherence Attacks and Countermeasures in Interposer-Based Systems

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Abstract—Industry is moving towards large-scale systems where processor cores, memories, accelerators, etc. are bundled via 2.5D integration. These various components are fabricated separately as chiplets and then integrated using an interconnect carrier, a so-called interposer. This new design style provides benefits in terms of yield as well as economies of scale, as chiplets may come from various third-party vendors, and be integrated into one sophisticated system. The benefits of this approach, however, come at the cost of new challenges for the system’s security and integrity when many third-party component chiplets, some from not fully trusted vendors, are integrated.

Here, we explore these challenges, but also promises, for modern interposer-based systems of cache-coherent, multi-core chiplets. First, we introduce a new, coherence-based attack, GETXspy, wherein a single compromised chiplet can expose a high-bandwidth side/covert-channel in an ostensibly secure system. We further show that prior art is insufficient to stop this new attack. Second, we propose using an active interposer as generic, secure-by-construction platform that forms a physical root of trust for modern 2.5D systems. Our scheme has limited overhead, restricted to the active interposer, allowing the chiplets and the coherence system to remain untouched. We show that our scheme prevents a wide range of attacks, including but not limited to our GETXspy attack, with little overhead on system performance, ~4%. This overhead reduces as workloads increase, ensuring scalability of the scheme.

I. INTRODUCTION

A recent trend in computing systems is the adoption of hardware organization based on chiplets and interposers [35], [56], [57], [71]. Instead of implementing a monolithic system-on-chip (SoC), this approach disaggregates the functional components across multiple smaller chips, i.e., chiplets, which are designed and manufactured separately. These chiplets serve as hard intellectual property (IP) modules, possibly sourced from a variety of vendors, and consolidated on an integration and interconnects carrier, i.e., the interposer [35], [52], [56], [57], [68], [71]. This approach is also known as 2.5D integration.

The adoption of chiplet and interposer integration raises design reuse to the level of the physical system, optimizing yields and streamlining time to market, resulting in significant cost benefits. Such 2.5D integration is already adopted by industry in products such as the AMD Epyc processors [56], [57] or the Intel Embedded Multi-Die Interconnect Bridge technology [50]. Recent industry talks have herald this design style as the next iteration of Moore’s law [21].

A. Security Challenges

Interposer-based systems are vulnerable to not only traditional attacks, but also a range of dedicated, new attacks. For example, vulnerabilities may be introduced through the various third-party chiplets, e.g., via untrusted fabrication [32] of chiplets, malicious or simply buggy third-party IPs [63] within chiplets, or collusion of multiple malicious actors across chiplets. If not addressed properly, the vulnerability of a single chiplet may undermine the entire system’s security.

Coherence is an essential mechanism which ensures all components maintain a consistent view of memory, not only for interposer-based systems, but interconnected SoCs in general. The predictability and prevalence of the coherence system makes it an attractive target, yet only a few related attacks have been proposed [36], [69], [79], e.g., a Trojan interacting with the coherence system can allow attackers to gain, or deny [36], control of the memory system or grant privilege-escalated access. Integrating defenses into the coherence system is a difficult task that requires extensive verification and design effort. Defenses that (naively) interact with the coherence system may cause functional bugs and deadlocks.

While prior work in secure network-on-chip (NoC) fabrics consider untrusted IP modules, they do not address the full scope of a coherence-oriented attack. These defenses are generally limited to the detection of attacks, limited to a single class of attack [8], [64], fail to prevent attacks against coherence-system interactions [24], [61], [65], require additional complex hardware [46], [58], [61], or require packet authentication through error-correction codes [10] or key exchanges [13], [25], [38] which increases network bandwidth pressure. In contrast, our scheme removes the burden of securing the NoC itself and allows for defensive strategies that target securing the coherence-level communications.

Figure 1 outlines a subset of attacks that a hardware Trojan can mount against a hybrid broadcast/directory coherence protocol, e.g., MOESI Hammer [16]. While selected and simple examples, these represent severe threats for interposer-based
GETXspy applies to any 2.5D system that enforces coherence, but is unique to such hardware orchestration because integrating chiplets from different vendors increases the risks for Trojan exposure and multiple actors maliciously colluding across chiplets. Prior works do not address such attacks enabled by legal cache coherence interactions. Note that the goal of this work is to protect not only against this particular covert-channel attack, but against all other system-level threats arising from untrusted chiplets integrated into a 2.5D system.

Establishing some “root of trust” is critical to ensure the security and integrity of data in modern systems containing various third-party IP components and software applications interacting on the system. Commercial solutions such as ARM’s TrustZone [47] and Intel’s SGX [53], as well as academic proposals [38], [44], [49], [82], typically rely on dedicated microarchitectural support and other measures, e.g., memory encryption. These approaches often incur high overheads and are prone to dedicated attacks [45], [62], while being susceptible to hardware Trojans throughout the outsourced supply chains [5], [54], a fact often overlooked in prior art.

B. Security Promise of Interposers, Our Contributions

We leverage the notion of interposer-based system design to establish a secure-by-construction root of trust in modern multi-core, multi-chiplet systems. Importantly, unlike prior art for secure system design, we do not assume/require trusted manufacturing of the whole system, only of the interposer, to provide system-level security promises.

We introduce a security-centric interconnect fabric within an active interposer, which monitors and controls all system-level communication with low performance overheads. Our design does not interfere with the system’s underlying coherence protocol, but rather prevents sensitive information from being divulged to, or manipulated by, untrusted chiplets.

The contributions of our work are as follows:

1) We examine how chiplets of an interposer-based system can be attacked a) directly via unprivileged memory references, b) indirectly via attacks conducted at the NoC level, namely unauthorized access, snooping, spoofing, modifying, or diverting of messages, and c) indirectly via covert-channels. For the latter, we demonstrate a simple but effective attack that allows a hardware Trojan to receive messages from a spy process operating in another chiplet. No prior work has identified this kind of attack and existing security mechanisms cannot mitigate it.

2) To protect against these threats around coherence-oriented system-level communication, we propose an active interposer as the physical backbone for a secure-by-construction root of trust in multi-chiplet systems.

3) We introduce a novel microarchitecture to secure communication passing from untrusted chiplets onto the interposer (and thus into the system) based upon per-packet validation at the interposer ingress links. Our design does not modify the underlying coherence system, but rather prevents it from exposing sensitive information. The key

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(a) Passive Reading: Trojan passively observes write traffic for other chiplets. (1) Misses from Chiplet A cause (2) broadcast invalidations to all chiplets; (3) Trojan snoop invalidation addresses. Our GETXspy attack is an example of this threat.

(b) Masquerading: Trojan acts as another core. (1) Miss causes GETX to directory; (2) broadcast invalidations to each chiplet; (3) Trojan blocks local observation, forges reply with different core ID; (4) requesting core proceeds, leaving local caches incoherent.

(c) Modifying: Trojan forges message to achieve incoherent state. (1) Chiplet A sends GETS to directory; (2) directory forwards request to Trojan’s core which has line in ‘E’ state. Trojan blocks GETS and (3) replies with GETX to requestor, (4) invalidating Chiplet A’s cache entry, leaving the attacker in control of another cache’s contents.

(d) Diverting: Trojan diverts invalidation requests. (1) Chiplet A sends GETX to the directory; (2) directory broadcasts invalidations. (3) Trojan blocks message and diverted a request to another core, (4) which responds with a negative-acknowledge or acknowledgment resulting in (5) the directory allowing original requestor to continue.

Fig. 1: Examples of coherence-oriented Trojan attacks in interposer-based systems. In each case, Chiplet A is the victim of a Trojan attack from Chiplet B.
objective of our proposal is to realize a secure large-scale system out of untrusted chiplets.

4) We implement our proposed technique and examine the implications of our security features. We characterize the performance impact as a low, \( \sim 4\% \) overhead. Further, we show the overhead decreases as workloads scale.

We note that developing a secure operating system (OS) for our system is outside the scope of this work. Prior work in secure OS and virtualization systems [15], [19], [40], [73] or systems described in Sec. II-B4 may be extended accordingly.

II. BACKGROUND, MOTIVATION, AND CONTRIBUTIONS

Here, we review key concepts of interposer technology, hardware security, and cache coherence protocols. We also motivate the contributions of our work considering the security challenges and promises for the respective state-of-the-art.

A. Interposer Technology

Interposer technology, also known as 2.5D integration, is the process of manufacturing two or more chips, or chiplets, separately and subsequently integrating and interconnecting them using a carrier made of silicon or other materials [35], [52], [56], [57], [68], [71]. Compared to traditional, monolithic SoC designs, 2.5D integration drastically reduces time to market. A system designer can procure IP as commodity chiplets and directly integrate them at the physical system level, with effort only required for designing the interposer. 2.5D integration is beneficial in general, as it allows for design and manufacturing process optimization, increasing yield for chiplets. Although future 2.5D designs will be more heterogeneous, current state-of-the-art systems are largely homogeneous, cache-coherent, multi-core chiplet designs [20], [35], [56], [57], [71].

Active interposers contain active devices (e.g., NoC routers, voltage regulators, sensors, etc.), while passive interposers act solely as an integration carrier and wiring medium. Although passive interposers are cheap to manufacture, their physical design can be quite challenging [30], [35]. In contrast to active interposers with buffering of interconnects, passive interposer wires are of considerable length, incurring significant power and delay overheads. An active interposer with an embedded NoC fabric serves well for large-scale chiplet integration and system communication. The chiplet interconnect fabric is encapsulated away from the interposer NoC beyond the edge router on the interposer to which it is attached. Such heterogeneous fabric allows for cross-optimization of topologies across chiplets and interposer, opening up considerable opportunities for system design [4], [17], [20], [30], [71], [80]. Further, active interposers improve testability [27], [68], [71] and thereby help to manage the yield of the final system.

Active interposers are typically manufactured in relatively older nodes [55], [71]. Therefore, it is realistic that a trusted facility is available for manufacturing of such active interposers. Here we propose an active interposer-based root of trust with security features embedded within its NoC routers.

B. Hardware Security

1) IC Manufacturing: Industry has widely adopted a work mode where IC design and verification is carried out by a design house and partners, but fabrication and testing is outsourced to off-shore facilities typically providing access to advanced technologies. While this practice reduces the cost of production and streamlines the time to market [78], it raises concerns regarding the trustworthiness of the outsourced fabrication facilities, which may seek to insert security vulnerabilities in general or hardware Trojans in particular [32].

The threat vector posed by untrusted fabrication facilities implies the ICs they manufacture are untrustworthy. This causes a security challenge for modern systems in multiple ways. First, any hardware security feature embedded in such outsourced IC may no longer offer the desired protection, presenting a profound challenge. Second, a modern system may be composed of chiplets with various levels of trustworthiness. Any malicious chiplet behavior may compromise the whole system due to its interconnected nature.

The interposer technology can help to avoid such complications. This is because an interposer can be fabricated separately in a trusted facility and may also embed security features. Accordingly, an interposer designed to constitute a hardware-enforced root of trust can be built upon to ensure the overall system’s trustworthiness, as we show in this work.

2) Hardware Trojans: Hardware-centric attacks such as the malicious insertion or modifications of circuitry, also known as hardware Trojans, can lead to catastrophic security failures within a system. For example, Bidmeshki et al. [6] provide an attack scenario wherein a hardware Trojan renders the cryptography subsystem vulnerable, Khan et al. [33] demonstrate Trojans that can leak data from cache memory of processors, and Kim et al. [36] introduce Trojans which inject malicious coherence messages to create a denial-of-service attack.

Our work is orthogonal to and compatible with prior art on Trojan detection and mitigation, e.g., [26], [28], [70]. We do not seek to prevent Trojans, rather to prevent their attacks from affecting the system-level security. Specifically, we seek to prevent any hardware-centric attacks that are executed through the memory and coherence system. This notion of system-level security is enforced by a clear physical separation of untrusted commodity chiplets and security features residing in the trusted interposer. Prior art on Trojan detection and mitigation cannot offer such secure-by-construction organization.

3) Secure Interconnect Fabrics: Prior art for NoC security assumes that malicious activities arise from connected components or the network fabric itself. Fiorin et al. [23] propose security features for policy-based message checking against untrusted components. Selected works focus on securing the system through encryption/decryption of packets/messages exchanged through NoC fabrics [22], [25]. Kinsey et al. [38] propose organizing secure and non-secure software/hardware entities as tenants and configure the NoC routers to securely exchange messages. While enabling a secure NoC fabric, the amount of key exchanges required to isolate nodes/tenants incurs high latencies and is not easily scaled.
Nabeel et al. [55] propose an interposer-based architecture where security modules monitor the interconnect fabric at the level of the bus addressing, to block transactions that violate memory access policies. While their design represents a relevant first work toward secure 2.5D integration, it has several limitations. First, the authors consider an overly simplistic architecture, ignoring the fact that state-of-the-art 2.5D designs are fully memory-mapped and cache-coherent. We find addressing the coherence model is critical to providing system-level security. Second, the authors did overlook new security challenges arising for interposer designs. Critically, their design would fail to hinder the GETXspy covert-side-channel attack we study in this work, as GETXspy does not violate memory access policies/permissions.

For most prior art, networks are not secure-by-construction, hence high-overhead solutions are required such as key-based security [13], [24], [64], model checking [9], [61], or additional structures to verify traffic patterns [46], [58], [61]. While packet-checking schemes similar to our design have been proposed in the past, e.g., [65], the underlying defense mechanisms often address only a single attack vector [8], [64] and/or fail to address the coherence system’s exploitable nature [24], [61], [65]. While these works check the message’s memory operation, they do not differentiate between specific coherence message types and the ways that coherence messages can be exploited beyond simple read or write traffic. Even more concerning, most prior art assumes, often implicitly, trusted manufacturing of the whole system. Such an assumption is challenged by outsourced supply chains. These concerns are only exacerbated for 2.5 integration using chiplets from various vendors.

By contrast, our work does not make such overarching assumptions. We enforce system-level security for untrusted commodity chiplets by integrating them on an interposer-based root of trust, the only component requiring trusted fabrication, thereby providing a secure-by-construction NoC. Without the need to secure the integrity of the NoC, a more simplified approach may be taken to ensure the security of the overall system, resulting in lower overheads.

4) Hardware Support for Root of Trust: Intel’s SGX provides an extension to create trusted execution environments (TEEs), called enclaves [18], [53]. Enclaves prevent unprivileged access to secure data during security-sensitive execution. Specifically, SGX maps protected memory pages to reserved memory regions in which the pages are encrypted by a hardware encryption module. However, recent work shows vulnerabilities in SGX, due to programming errors and untrusted software [34], [60], as well as due to speculative execution [11], [14], [41], [66]. ARM’s hardware-enforced TEE isolates secure execution from untrusted software [47]. AMD’s TEE leverages a normal OS running in tandem with a secure OS. The latter has access to the full range of a device’s peripherals and memory, whereas the normal OS only has access to a subset of peripherals and memory regions, to prevent unauthorized access of sensitive resources. However, recent work shows TEEs are prone to vulnerabilities due to architectural, implementation, and hardware issues [12].

In short, these schemes incur high overheads, are prone to dedicated attacks, and are susceptible to Trojans in general. In contrast, our approach has little impact on system performance and its key components are secure-by-construction.

C. Cache Coherence

Coherence protocols ensure updates to cached copies of data are visible to all cores in modern multi-core designs [20], [57], [71]. Broadly speaking, coherence schemes can be categorized as broadcast (or snooping) protocols [1], [7], [67] and directory protocols [2], [43], [81]. Broadcast protocols, while simple to implement, suffer from high traffic due to the amount of messages multi-core systems require to maintain coherence. Directory protocols allow for fine-grained state tracking and unicast messages, making them highly scalable, but difficult to implement and have higher access latencies.

A coherence protocol is generally oblivious to the software and may permit malicious accesses that leak sensitive information [69], [79]. Existing countermeasures address conflict-based and transient-execution side-channel attacks, but do not consider threats from maliciously manipulated/malformed coherence message packets [39], [75]–[77]. Given that the coherence protocol acts only based on rules for how memory is updated across multiple parties, attackers may exploit the coherence protocol’s low-level behavior. We demonstrate one such attack in Sec. IV. It is important to note that coherence is a hardware-managed, micro-architectural feature which is neither influenced by, nor exposed to, the software executing on the system, rendering software-based defenses ineffective.

Our solution does not require modifying the coherence protocol (which would impose extensive verification efforts and can result in complex, adversarial side-effects for the system behavior). Rather, we carefully ensure messages’ integrity and prevent untrustworthy chiplets from exploiting the coherence protocol and system-level memory management.

III. SYSTEM ARCHITECTURE OVERVIEW

Figure 2 outlines the secure, interposer-based, multi-chiplet and multi-core system proposed in this work. The baseline system is loosely based on the architecture of the Rocket-64 design proposed by Kim et al. [35]. In addition to the overview in this section, more details are provided in Sec. VI.

A. Chiplet and Interconnects Architecture

In this system, we employ eight chiplets, each containing eight CPU cores, for 64 cores in total, similar to recent AMD processors [56], [57]. Each core has an L1 instruction and data cache, and a unified L2 cache; all cache levels are private to each core. The cache controllers generate coherence messages which the network interface (NI) in each chiplet converts...
to network packets prior to injection into the interposer NoC (via interface routers). Chiplets are interconnected to each other and to four memory controllers (MC) via an NoC of 2D mesh topology residing in the active interposer. The interface routers, depicted along the east and west edges of the system, serve as ingress links for the chiplets into the interposer NoC.

Many other architectures are practical for interposer-based systems [4], [17], [20], [30], [71], [80]. Assuming a cache-coherent shared memory and an active interposer, our proposed system can be readily ported to such. Furthermore, the security principles leveraged in our work—verification and policy-checking of memory-system messages, as outlined below and further detailed in Sec. VI—are extendable to other coherence schemes as well.

**B. Principles and Features for System-Level Security**

We propose the interposer as root of trust for integration of untrustworthy chiplets into a secure system, namely by enforcing policy checking of all system-level communication. The necessary attributes to enable such a secure system are: (1) the interposer is manufactured separately from the untrusted chiplets, in a trusted facility; and (2) the interposer serves as integration and communication backbone between chiplets.

Any system-level communication across chiplets must pass through the interposer. Accordingly, all memory traffic must traverse the interposer NoC as network packets and are checked before entering the network. If a CPU core wants to read/write data from/to memory, a corresponding coherence message, embedded in a packet, must traverse the interposer NoC. Similarly, if a core wants to communicate with another core in another chiplet, such direct messages must also traverse the interposer NoC. Importantly, all direct communication messages are limited to legal coherence messages, as is typical in most multi-processor systems. Thus, we embed related security features exclusively within the interposer NoC such that all messages must inevitably traverse through, and be checked by, the trusted active interposer.

We add *Coherence Message Checkers (CMCs)* to the physical ingress links to validate all coherence messages coming from the chiplets into the active interposer. We also add CMCs to the physical links connecting with the MCs; the related details are discussed in Sec. VI-A2. Since CMCs are implemented exclusively within the trusted active interposer, their hardware is trustworthy and free from Trojans by construction.

**C. Cache Coherence Protocol**

We focus on the *MOESI Hammer* cache coherence protocol [16] as basis for our implementation, which is used in many AMD systems as scalable protocol for multi-core systems. Our approach, however, is easily extendable to other coherence schemes as well.

MOESI Hammer is a hybrid protocol; it encapsulates the scalability of directory-protocols without high implementation complexity while achieving the low-latency of broadcast protocols without overly increasing broadcasted coherence message traffic. To that end, MOESI Hammer maintains a sparse directory between multiple home nodes to track cache lines’ states and owners. Coherence requests access a cache line’s home-node directory and DRAM in parallel to reduce the cost of a directory miss, cancelling the DRAM response if a directory entry is found. Traffic is reduced by only broadcasting to all cores for specific state transitions. We note that coherence broadcast protocols increase exposure to Trojan attacks, which might snoop broadcast messages to memory regions otherwise inaccessible. Our security approach addresses this threat directly and in a novel way. Next, we showcase one such concrete attack, and then we follow-up with our threat model, which covers other common threats for system-level security of modern interconnected designs.

**IV. THE GETX\textsubscript{spy} ATTACK**

Here we introduce and demonstrate a new attack leveraging the vulnerability of the coherence mechanism to hardware Trojans in untrusted chiplets. Specifically, our attack a) can transmit any data from one chiplet, via a regular user process acting as *spy* that generates tailored write-ownership coherence messages (GETX), and b) employs a hardware Trojan in a compromised chiplet that passively reads those GETX requests. We call the attack GETX\textsubscript{spy} as it relies on GETX requests generated by the spy. No prior security scheme we are aware of is capable of preventing this kind of attack. That is because GETX\textsubscript{spy} observes the addresses of legal invalidation messages; it does not violate the system’s coherence protocol, allowing it to evade the defense mechanisms of prior work.
While the attack demonstration is specific to MOESI Hammer, the working principle can be easily applied to various broadcast or directory protocols in interposer-based systems. Also, while this attack focuses on the threat of a compromised coherence system in interposer-based designs, note that our proposed scheme also prevents further, more generic attack vectors outlined in Sec. V and studied in Sec. VII.

A. Working Principle

MOESI Hammer (Sec. III-C) uses a coarse-grained directory distributed between multiple memory controllers (MCs). Each core has its own local directory to maintain coherence. When an MC directory receives a GETX request without an existing entry, a broadcast message is sent to all cores. This expected interaction can be used to create a simple covert-channel between a spy process and a hardware Trojan placed at the cache controller directory in one of a chiplet’s cores to receive information via broadcasted GETX messages.

While our attack exploits the coherence state of specific addresses, similar to [79], it differs in a few important aspects. First and most importantly, GETXspy does not require the spy and Trojan to operate within the same virtual address space. Second, our covert-channel does not rely on a Trojan process to query the targeted addresses. Third, our attack is not reliant on timing memory accesses. Finally, our Trojan is simply a malicious observer of memory requests, representing a realistic and concerning scenario that is hard to mitigate.

Figure 3 illustrates the attack orchestration. (1) The spy process allocates a large memory region to continually cause remote requests without pausing to flush the L2. (2) The spy writes to targeted sets, causing misses in the L2. (3) Each miss generates a new GETX request. (4) The GETX is sent to the MC to check for a directory entry or “hit” in the probe filter. (5) The GETX misses in the MC, resulting in a broadcast GETX to invalidate any shared copies of the data present in other cores. (6) The chiplet containing the hardware Trojan receives the broadcasted GETX, which buffers the request. Using the L2 set index bits, the Trojan checks if a synchronization message has been received. (7) After synchronization, the Trojan observes GETX requests from the spy process to receive covert messages.

Critically, the chiplet holding the Trojan (Chiplet 8 here) does not need shared access to the spy process’s virtual address range, as the coherence protocol mandates GETX requests be broadcast to all cores, regardless of physical page ownership. Also, the attack does not require the memory region to be primed or the caches to be flushed before a new transmission. GETXspy can be trivially reworked into a side-channel attack. In such case, the GETXspy Trojan would passively watch for GETX-induced, invalidation broadcasts, to spy on the write address patterns of processes in other chiplets. Here again, the chiplet containing the Trojan need not have any access to the virtual address space or physical pages of the processes being spied upon.

B. GETXspy Case Study

We implement GETXspy on the system described in Sec. III, for the unsecured baseline version versus the proposed secure version. The evaluation setting is described in Sec. VII. The system has an 8-way associative L2 cache and 4-way associative MC directory. This means targeting 32 addresses, 16 for each set representing ‘1’ or ‘0’ to transmit, allows for continuous flushing of the L2 target sets (covert transmission).

Figure 4a shows the addresses requested by the spy process via GETX, as seen by the Trojan within a different core and chiplet. The sets referenced by the addresses are shown in Fig. 4b. The spy process performs requests to allocate memory via GETX, as seen by the Trojan within a different core and chiplet. The sets referenced by the addresses are shown in Fig. 4b. The spy process performs requests to allocate memory which are viewed by the hardware Trojan as inconsistent accesses and therefore considered irrelevant. The attack region that is seen by the Trojan, Fig. 4c, shows the spy later sending requests between two distinct sets to represent a ‘1’ or ‘0,’ respectively. The graph in Fig. 4d shows the GETX requests seen by the Trojan—namely none—when the attack is executed on our proposed secure design.

Table I shows the characteristics of the GETXspy attack’s covert-channel for the unsecured baseline system. With a 4.22 Mbps bandwidth, this covert-channel provides the basis for executing a range of data-leakage attacks or other threats.

| Message Size | 128 bits |
|--------------|----------|
| Cycles Taken to Transmit | 28924 |
| Clock Frequency | 1GHz |
| Total Time Taken to Transmit | 28.92µs |
| Megabits per Second | 4.22 |
| Percentage of NoC Bandwidth | 0.013% |

TABLE I: GETXspy Covert-Channel Characteristics
V. Threat Model

The focus of this work is a system wherein multiple chiplets have been fabricated in various facilities and then connected together using interposer technology. The assumption is that the fabrication as well as operational behavior of the chiplets, either designed in-house or composed of third-party IPs, cannot be trusted. In other words, we assume that some Trojan(s) may exist in some chiplet(s).\(^2\) We also assume that attacks are targeted at memory-system traffic which is the only type of traffic physically passing through the interposer.

Attacks on interconnected systems can be broadly categorized as outlined in [3]. Accordingly, our model considers the related four types of threat vectors (shown in Fig. 1):

**Passive reading, aka snooping:** This threat occurs when a malicious chiplet can read data not meant to. The GETXspy attack demonstrated in Sec. IV is an example of such a threat in that the Trojan monitors broadcasted GETX requests to snoop a tailored message.

**Masquerading, aka spoofing:** This threat occurs when a malicious chiplet disguises itself as another chiplet to gain access to sensitive data or control of resources. Malicious chiplets can modify the requester IDs and memory addresses embedded in cache coherence messages, tricking directories or other unsuspecting cores into divulging sensitive data.

**Modifying:** Such threats modify cache coherence messages. For example, a chiplet may attempt to disguise itself as having write access to a memory region it has only read access to.

**Diverting:** In shared-memory applications, a malicious chiplet may divert data meant for one chiplet to another untrusted chiplet, bypassing memory permissions. It may also divert cache coherence messages, undermining the protocol.

In general, we aim to prevent hardware- and software-driven unauthorized access to memory regions at the chiplet granularity, whether by software privilege escalation, transient execution attacks, cache side-channels, or any other means.

Our scheme provides protection on a chiplet granularity. Attacks across cores but within the same chiplet [51], [59], are out of scope of this work. Similarly, out of scope are attacks wherein code running on one core attempts to violate the security of other processes running on that same core or on another core in the same chiplet. Further, attacks wherein one chiplet can leverage memory transactions to its assigned memory region to modify DRAM rows that are not assigned to it, e.g., Rowhammer [37], are out of scope. We note that prior art for protecting against such threats is orthogonal to our work and can be applied in addition.

VI. System Design

Our proposed design prevents attacks running on any given chiplet from violating the security of the overall system, as we physically enforce protection against any unauthorized access to shared-memory regions and conduct continuous checking of the integrity and validity of cache coherence messages. Next, we discuss the system design.

A. Microarchitecture

1) **CMC Overview:** With the proposed CMCs, we monitor and validate all incoming packets to the interposer. Figure 5 depicts the CMC embedded in a router of the interposer NoC. The CMC monitors messages traversing the physical links used by the packet.

\(^2\)Our work is orthogonal to and compatible with prior art on Trojan detection and mitigation, e.g., [26], [28], [70]. We do not seek to prevent Trojans, but to prevent their attacks from affecting the system-level security.
prior to entering the virtual channel buffers within the routers. Each CMC has two components described as follows:

 **Packet Checker/Modifier (PCM):** The PCM monitors and modifies cache coherence messages as needed. Because the proposed system follows standard shared-memory semantics, all legal communication between cores, other IPs, I/O buses, and memory occurs through memory accesses which create cache coherence messages. Thus, the PCM operates on coherence messages to check addresses and permissions; modifying messages as needed. More details are discussed in Sec. VI-C.

 **Address Protection Unit (APU) Table:** This is a direct-mapped, SRAM-based look-up table with entries for each memory region and their associated per-chiplet permissions. As outlined in Sec. VI-B, the main physical memory is partitioned into multiple fixed-size regions. Each memory region has a corresponding entry in the APU; hence, the number of entries within the APU table is determined by the number of regions in the main memory.

2) **CMC Types and Placement:** Recall Fig. 2, depicting CMCs embedded in the secure interposer-based system. The CMCs connected to the physical links coming from chiplets are denoted as “CMC-1” and those connected to the physical links for MCs are denoted “CMC-2.” CMC-1 only monitors and verifies coherence messages entering the interposer, whereas CMC-2 modifies certain coherence messages at the directories (to counter passive-reading threats on broadcast messages). Router-to-router connections running exclusively within the trusted interposer do not require CMC monitoring.

 **CMC-1:** Prevents the attached chiplet from injecting malicious coherence messages into the system that violate the provisions of the shared-memory organization, as outlined in Sec. VI-B. The PCM within CMC-1 monitors all traffic from the attached chiplet based on the physical address the packet refers to. This physical address is compared against the per-region permissions stored in the APU table (described further below). If a message is of an allowed type to an allowed memory region for the given chiplet (e.g., a GETX to a read-only memory region it owns), the message may proceed into the interposer NoC. Otherwise, if the packet is rejected, a dedicated security signal, realized as a machine-check exception, is thrown and system execution stops.

 **CMC-2:** Prevents the broadcast of coherence messages to chiplets which are not permitted to access the related memory regions. As described in Sec. III-C, MOESI Hammer does not maintain per-core sharing information, hence certain message requests cause the directory to broadcast the request to all cores. The cores then respond based on whether the cache block is shared by that core. This raises a concern of passive reading/snooping; recall the GETxspy attacks in Sec. IV.

To prevent snooping, the PCM determines whether a given broadcast message is directed towards a chiplet allowed to access the referred memory region (based on the APU table). If the chiplet does not have access, the broadcast message is converted into an appropriate response message directed only to the original requester. This is legal within the coherence scheme of the system: if a chiplet is not allowed to access a memory region, then its caches cannot contain lines associated with that region. This allows the CMC-2 to safely divert broadcast messages from the directory and prevent snooping.

3) **APU Table:** The APU table is a lookup table containing entries describing the access permissions for applications running within a respective chiplet. Each entry corresponds to a pre-determined physical memory region. The access permissions are determined by a secure OS that is running exclusively within the active interposer, independently of the regular OS running on the chiplets. The permissions are programmed into the APU tables during runtime, as outlined in Sec. VI-B.

Figure 6 details one entry in the APU table. Each entry represents one memory region, with two bits allocated per chiplet to represent the access permissions of applications running in the chiplet: a chiplet may have no access permissions (‘00’), read-only permissions (‘01’), or read/write permissions (‘11’). The encoding ‘10’ is unused.

When the PCM intercepts a packet, the upper bits of its physical address are extracted and used to index into the APU table. The related entry is read and handed back to the PCM to compare the request type, requester ID, and destination ID against the permission levels in the APU table entry.

### B. OS Support and Shared-Memory Organization

Designing a secure OS to capitalize on our active interposer-based root of trust is beyond the scope of this work. However, prior work in security-enabled OS environments [15], [19], [40], [73] and TEEs (Sec. II-B4) may be extended accordingly.\(^3\)

\(^3\)This is a secure and protocol-conform approach. For the sake of system-level throughput, one may want to only isolate the chiplet(s) triggering a security violation. Doing so safely, however, is not trivial, as it would require significant modifications of the coherence protocol itself to prevent deadlocks.
The interposer may include a trusted co-processor to support a secure OS, secure boot-up and execution environments [29], [47], [74]. In our scheme, critical tasks like updating the APU table must be delegated to such a secure environment, as the chiplets are physically unable to access the proposed security features. That is, attacks on the APU table and other components are prevented by construction.

In shared-memory systems, permissions are typically defined per physical page by the OS during memory allocation. Enforcing per-page permissions in a CMC poses several challenges. Specifically, page-level tracking requires a TLB-like structure to cache translations [72]. The required support for maintaining the structure in coherence with the full system’s page table significantly increases hardware complexity and performance overhead. We argue that a page-level implementation at the interposer is excessive in a system of relatively few and coarse-grained chiplets. Instead, we partition physical memory into coarse-grained memory regions, similar to prior art [40], [42], [73], [74].

We aim for a “sweet spot” between too coarse-grained, where only few memory regions are available and capacity is wasted to fragmentation, versus too fine-grained, where the APU table could not hold the excessive number of regions without incurring high access latency or placing entries in a backstore. We find that a total number of memory regions between 4x–8x the number of chiplets is more than sufficient for most use-cases, allowing for diverse private and shared memory regions without too much fragmentation.

Each memory region is designated as read- or write-able independently to any given chiplet, with permissions updated as needed. Data private to a single chiplet is placed in a region (or set of regions) only accessible by that chiplet. A page shared across multiple chiplets is assigned to a memory region the given chiplets are allowed access to.

Initial memory partitioning and permission setting occurs during the initial soft page fault on a virtual page. Region allocations and permissions are updated via an API call from the OS, e.g., similar to Intel’s SGX page allocation model [53]. After a page fault, the OS requests a memory range for the process from the secure OS operating on the interposer. The APU table for the chiplet that requested the page is updated with the new permissions. The secure OS then provides a physical page to the unsecure OS. Since the APU table update occurs on the trusted interposer, the chiplets are unaware of the memory allocation request. Critically, a malicious chiplet that somehow gains knowledge of the request still cannot access the region, due to the newly set permissions in the APU table, before any malicious operation may target the memory region.

C. Implementation Details

1) NoC Configuration: Regardless of the interposer’s NoC topology, CMCs are emplaced at the interface between chiplets or MCs and the active interposer. However, the width of the physical link does impact the CMC design and its logic. In our implementation and evaluation, the link width is 128 bits within chiplets and 64/128 bits within the interposer.

2) Cache Coherence Protocol: The system’s cache coherence protocol directly impacts the CMC logic and as the coherence message fields need to be analyzed by the CMC.

3) Protocol Compliance: First, coherence messages are converted into network packets by the chiplets’ NIs. However, these packets are not guaranteed to adhere to the rules of the network and coherence protocols. For example, a Trojan may fabricate an invalid message type, yielding undefined, possibly vulnerable behavior. Second, messages corresponding to particular virtual networks (VNs) must follow a specific, limited set of requester/destination IDs and message types.

To address both aspects, the PCM checks the possible field values to verify the legality of messages. Since these checks are orthogonal to memory-region permission checking, they are performed in parallel and incur no extra delay.

4) Design Cost: We design the PCM module with three pipeline stages for lookup, packet checking, and packet modification. The third stage is bypassed in CMC-1 instances as they only monitor packets on ingress to the interposer. An APU table requires two bits for identifying each chiplet’s
TABLE II: System Architecture Configuration

| Component               | Variable               |
|-------------------------|------------------------|
| Chiplet Architecture    |                        |
| Core                    | 8 RISC-V cores         |
| Private L1 I-Cache      | 32KB                   |
| Private L1 D-Cache      | 64KB                   |
| L2 Cache                | 2MB                    |
| NoC                     | Eight-port, 128-bit Crossbar |
| vc_per_vnet             | 4, 6, 8, or 10         |
| Chiplet Frequency       | 1GHz                   |
| System Architecture     |                        |
| Chips                   | 8                      |
| MCs                     | 4                      |
| Main Memory             | 4GB                    |
| Memory Regions          | 64, 64MB each          |
| NoC                     | 3x4 2D-Mesh, 64 or 128 bit |
| vc_per_vnet             | 4, 6, 8, or 10         |
| Interposer Frequency    | 250MHz                 |
| Cache Coherence         |                        |
| Model                   | AMD MOESI Hammer       |
| Simulation Configuration|                        |
| Processor Model         | TimingSimpleCPU        |
| Simulation Model        | System emulation       |

We first discuss our evaluation methodology. Then, we examine the performance overheads caused by our scheme.

A. Methodology

We implement and evaluate our proposed system for system emulation using gem5 [48]. Table II depicts the configuration details. The system is inspired by the Rocket-64 design [35]. Thus, we simulate an 8-chiplet, 64-core system as described in Sec. III. The interposer is assumed to be fabricated using an older process node; it operates at 250MHz, a quarter of the chiplets’ frequency.

Performance impact is measured as IPC speedup/slowdown for the secure, CMC-enabled configuration over the unsecured baseline configuration. The CMCs latencies are discussed in Sec. VI-C and disabled for the unsecured baseline. Due to long simulation times induced for this large system, we evaluate the IPC using a subset of the SPEC 2006 benchmarks. We perform single-threaded and multi-programmed benchmark simulations to better understand the impact of the CMCs.

B. Security Analysis

1) Threat Model Coverage: Our scheme addresses each of the threats discussed in Sec. V as follows:

Passive reading: This threat is prevented by rerouting broadcast messages as they enter the CMC-2 located at the interposer/MC boundary. Broadcast messages from the directories are converted into negative acknowledgments back to the requester for chiplets that do not have permissions to the message’s memory region.

Masquerading: Every CMC-1 is programmed with the range of ID’s expected in each coherence message’s requester ID field. For example, in Fig. 2, the CMC-1 in router 72 can expect requestor IDs in the range of 0 to 7 and will reject any message with an ID outside of this range, as discussed in Sec. VI-C3. In this event, the CMC will throw a security check exception and halt execution.

Modification: This threat is detected by comparing a message type, such as GETX/GETS, with the access permissions in the APU table. If a message seeks to access memory outside of its allowed address space, a security check exception is thrown.

2) Security Testing: To test the system’s ability to counter the discussed threats, we inject tailored, malicious coherence messages at the network interface of cores. We verify that, for masquerading, modification, and diversion threats through packet manipulation without malicious hardware intervention.

C. Single-Threaded Performance Impact

Figure 8 shows the speedup/slowdown of the system with CMCs enabled compared to the baseline configuration. All workloads experience a speedup less than 1, which is expected, as the CMCs introduce higher latencies to the network. As the figure shows, the CMCs impose an average performance loss of ∼4%, with several benchmarks (povray, hammer, libquantum) showing little to no impact. sphinx3, however, is an outlier, showing a significant ∼27% performance loss.

To analyze further, we examine the L2 miss rates of each benchmark in Fig. 9. The figure demonstrates that the variation...
between each benchmark’s result in Fig. 8 is highly correlated to a benchmark’s cache hit rate. For instance, sphinx3 shows a much higher L2 cache miss rate than other benchmarks at \( \sim 68\% \). The CMCs must process each packet resulting in increased memory access latencies. Thus, the CMC-enabled system’s performance depends on the number of coherence messages that L2 cache misses inject into the NoC.

The performance degradation in some benchmarks is analyzed in Fig. 10, showing the percentage change for pre-injection queuing latency versus in-network latency and the total latency experienced by packets in the network. Interestingly, while the queuing latency increases by \( \sim 80\% \), the in-network latencies drop by 5–10\%. The increase in queuing latency is expected, due to the extra pipeline delays on network insertion that the CMCs cause. The decrease in in-network latency is due to CMC-2 instances rerouting acknowledgment messages back to only the original requester (as a negative acknowledgment). Thus, the CMC-2 reduces total network load by removing one packet in the transaction.

The total packet latency increases by 39\% on average. Interestingly, although sphinx3 incurs a higher performance impact than the other benchmarks, it does not see a significantly different packet latency. That is, sphinx3’s performance loss is due to a higher L2 miss rate and hence higher packet injection, as discussed above, not a higher per-packet latency. Its higher miss rate exposes sphinx3 more to the increase of network latency than other applications, which have lower miss rates.

Figure 11 depicts the speedup of the benchmarks with three different virtual channel configurations (vc_per_vnet). We observe that the geometric mean speedup approaches 0.98 with more virtual channels. We see a significant improvement in speedup for sphinx3 due to the improvement in queuing latencies at the network interfaces. These significant gains imply that increasing VC count is a good way to improve performance if the application has a high cache miss rate.

In Fig. 12, we analyze the impact of increasing the interposer link widths to 128 bits versus the baseline of 64 bits.\(^4\) This larger bandwidth provides slightly better speedup compared to the baseline. These modest gains imply that increasing the bit-width for the physical links in the interposer is likely not worthwhile, although this depends on the designer’s trade-off for costs/overheads and scalability of the system.

D. Multi-Programmed Performance Impact

We evaluate the impact of the CMCs for multi-programmed workloads using random mixes of two benchmarks each, executed in two cores in separate chiplets. Here we simulate until all applications complete at least five billion instructions and we report the weighted speedup of the combination using a methodology from Kadjo et al. [31].

Figure 13 shows the speedup for these multi-programmed workloads. In general, speedups range between 0.95 and

\(^4\)Due to runtime constraints for such large-scale simulations running on our shared high-performance computing cluster, we focused on a representative subset of benchmark runs for that particular experimentation.
1.06. In some cases, namely bzip2-namd and bwaves-gcc, the speedup with the CMCs enabled was better than the baseline. Further, the mixtures which included sphinx3 showed reduced performance loss versus the stand-alone sphinx3. As before, the improvement is a result of CMC-2 filtering out packets otherwise sent to unauthorized chiplets. This reduces the bandwidth pressure that multiple applications induce on the NoC and appears to reduce the performance overhead as the number of workloads increase.

VIII. CONCLUSION

In this work, we propose the use of an active interposer as root of trust for modern chiplets-based systems, by implementing hardware security features directly within the interposer. More specifically, we devise a coherence message checker (CMC), which we propose to include at the boundary between the interposer and the chiplets/memory controllers. We show how such a scheme addresses various attacks arising from malicious chiplets, with relatively low performance impact, ~4% on average, compared to a non-secure baseline system.

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