A 14.5-bit ENOB, 10MS/s SAR-ADC with 2\textsuperscript{nd} order hybrid passive-active resonator noise shaping

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ABSTRACT A new 2\textsuperscript{nd} order noise shaping (NS) based successive approximation register (SAR) ADC is presented in this paper. In comparison to earlier research, this paper considers hybrid passive-active integrators to compensate for the phase error of the passive integrator. To realize the resonator noise shaping in high-speed asynchronous SAR-ADC, the hybrid passive-active sigma-delta modulator (SDM) is introduced as a multi-input feedforward loop filter to overcome the noise barrier of the conventional asynchronous SAR-ADC generated from the CDAC, quantizer, and dynamic comparator. The proposed noise shaping technique significantly reduces the ADC power consumption and area compared with the active SDM noise shaping approach while overcoming the shortcomings of passive SDM, such as large-area penalty, low resolution, and low speed. It consists of a very low power forward gain \( G \) and a positive feedback path across a 1\textsuperscript{st} order passive switch capacitor (SC) integrator to desensitize the capacitor ratios under PVT variations. Extensive circuits simulation verifications and system-level results have been used to validate the effectiveness of the proposed NS SAR-ADC. The simulation results show that the proposed SAR ADC consumes 0.88mW at maximum speed, with an SNDR of 89.43 dB and SFDR 98.64 dB within 0.1 fs oversampling frequency.

INDEX TERMS discrete-time (DT), low-gain-amplifier-based switched-capacitor (SC) integrator, noise shaping, passive SC integrator, Sigma-Delta modulator

I. INTRODUCTION

In modern communication systems, several high-precision analog-to-digital converters need to be used. To meet the requirements of high precision and wide bandwidth, a series of new ADC structures have successively appeared. Noise shaping successive approximation ADC (NS SAR-ADC) is one of the most popular structures studied in recent five years. While the conventional SAR-ADC has low power consumption and a small area [5–7], the comparator's noise, offset, quantization noise, and the CDAC thermal noise limits its accuracy. The sigma-delta ADC is the most used structure to achieve high precision, but due to the need for many opamps in this structure, its power consumption is high, and the area is large. The NS-SAR ADC structure is a hybrid SAR-ADC and sigma-delta modulator (SDM) that inherits both advantages. It has the characteristics of low power consumption of the SAR ADC and a considerable potential to achieve high precision of sigma-delta ADC. Moreover, NS SAR-ADC requires a lower oversampling ratio (OSR) than the traditional sigma-delta modulator, thus increasing the bandwidth of the circuits.

References [7–9] described methods for reducing the input-referred noise and offset of SAR ADC using a time-domain comparator to reduce the total power at the cost of a slow conversion, making it less desirable for high-speed applications. The SDM is the most critical candidate architecture considering oversampling and noise shaping techniques from a high-resolution perspective. An active integrator based on opamps is the critical component, typically power-hungry and challenging to scale. SAR ADC with an SDM significantly improves the capability of a noise-shaping (NS) SAR-ADC to overcome the deficiencies mentioned above, making it a preferred approach for delivery of both high resolutions and low power consumption simultaneously [1–2]. The authors [1] proposed a noise-shaping technique using FIR and IIR filters. For sampling the residue voltage, a two-tap charge-domain FIR filter is utilized. An IIR noise shaping filter constructed from operational amplifiers serves as an integrator to enhance noise shaping. Nevertheless, an active integrator is introduced, which inevitably deteriorates the energy efficiency and scalability of the circuits. In [3], the authors have proposed a first-order noise shaping without the requirement of opamps.
Using passive integrators, the design has high efficiency without interrupting the normal SAR-ADC operation. In this case, the zero of [3] is set at 0.5, indicating poor noise shaping and the resulting signal attenuation of 6 dB. Furthermore, in recent research publications [4-6], second-order passive shaping techniques are proposed to increase the DC attenuation in the NTF(z), where the values of α and k, which refers to the capacitor ratios and comparator gain, should be increased significantly, as explained in Section II-A, which inevitably increase the area of the chip and the power. Therefore, the loop dynamics in terms of ADC speed and stability will be significantly impacted because the CDAC settling time is one of the most critical bottlenecks for high-speed SAR-ADC.

This paper proposes a second-order low-power hybrid passive-active NS-SAR ADC architecture to overcome the aforementioned problems. In contrast to prior works, the passive-active integrators based on low gain open-loop opamp are used in the loop filter instead of conventional opamp-based active integrators. Zeros in the system are determined solely by the capacitor ratio and positive feedback compensation, insensitive to process, voltage, or temperature (PVT) variations. Moreover, a resonator is introduced in the loop to achieve wide noise-shaped bandwidth.

Aside from noise shaping techniques, the choice of capacitive CDACs is also of critical importance. It has been demonstrated that DAC switching schemes such as monotonic switching (MS) provide very good energy efficiency. Compared to conventional structures, this topology reduces switching-related energy losses by 81% [10]. The MS structure degrades ADC performance due to variations in the common-mode level offset within the comparator. To stabilize the dynamic amplifier's input common-mode (CM) level, a common-mode-stabilization (CMS) circuit is proposed within the MS SAR ADC architecture.

This paper is organized as follows; Section II focuses on the fundamental theory of noise-shaping SAR-ADC and design considerations. Section III details the proposed NS SAR-ADC architecture, including proposed noise shaping architecture and detailed circuits implementation. Section IV describes the extensive simulation results from the system and circuits levels and other building block designs. Section V summarizes the paper's conclusions.

II. FUNDAMENTAL THEORY ANALYSIS OF NOISE SHAPING AND DESIGN CONSIDERATIONS

II-A Passive integrator vs. Active integrator

Fig.1 illustrates the active and passive integrators. The transfer functions for the 1st order active and passive integrators are written as:

\[
\begin{align*}
H_{\text{active}}(z) &= \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_S}{C_i} \frac{z^{-1}}{1 - z^{-1}} \\
H_{\text{passive}}(z) &= \frac{V_{out}(z)}{V_{in}(z)} = \frac{az^{-1}}{1 - (1 - \alpha)z^{-1}}, \text{ where } \alpha = \frac{C_S}{C_S + C_i}
\end{align*}
\]

where \(C_S\) is the sampling capacitor and \(C_i\) is the integrating capacitor. As opposed to the ideal active integrator transfer function (1), the passive integrator's transfer function (2) exhibits both gain and phase error. Due to the built-in analog trade-offs, the passive transfer function cannot be modified to resemble an ideal active transfer function. First, to reduce gain error, \(C_S\) must be greater than \(C_i\), which results in an increase in phase error. Furthermore, \(C_i\) should be greater than \(C_S\) to reduce phase error, which leads to increased gain error. Thus, there is a trade-off between sizing \(C_i\) and \(C_S\). The feedforward gain of the comparator usually can compensate for the gain error in NS-SAR-ADC, while noise shaping is not properly performed if excessive phase error occurs. Since the phase error is crucial, it shifts the pole of the integrator and, therefore, the zero of the NTF of the loop filter as well, according to (3). This pole shift flattens the low-frequency part of the noise transfer function, which in turn significantly reduces the effect of noise shaping within the bandwidth.

\[
NTF(z) = \frac{1}{1 + H(z)} = \frac{1}{1 - (1 - \alpha)z^{-1}} = \frac{1}{1 - (1 - 2\alpha)z^{-1}}, \text{ where } z = 1, NTF(z) = 0.5
\]

Similarly, as shown in Fig.1(c), the works published in [5-6],[9] with 2nd order passive noise shaping have severe limitations, which refers to the DC suppression and stability requirement. To satisfy the noise shaping capability and stability requirement, the 2nd order passive noise shaping requires excessive capacitor ratios, \(\alpha_{1-2}\) Comparator gain \(G\) for noise-shaping, which dramatically reduces the ADC's speed and large area penalty and inevitably introduces considerable kickback noise and dynamic power for the comparator, as discussed below. Assume the complementary capacitive-DAC (CDAC) has a capacitor value equal to \(C\), and
The kickback noise is dynamic in nature, as the input MOS pair in the whole comparison process can operate in a variety of regions (such as cut-off, saturation, or triode), which will have a significant impact on the accuracy of the decision [22]. The full expression of kickback noise of multi-input latched comparator can be written as:

\[ Q_{\text{cut-off}} = V_{cm}C_{GB} + V_{GS}C_{GS} + (V_{cm} - V_{DD})C_{GD} \]  

\[ Q_{G_{\text{sat}}} = \frac{2}{3}(1 + G_1 + G_2)WLC_{ox}(V_{cm} - V_A(t) - V_{th}) + \big( V_{cm} - V_A(t) \big)C_{GS} + \big( V_{cm} - D_1(t) \big)C_{GD} \]  

\[ Q_{G_{\text{trio}}} = (1 + G_1 + G_2)WLC_{ox}(V_{cm} - V_A(t) - V_{th}) + \big( V_{cm} - V_A(t) \big)C_{GS} + \big( V_{cm} - D_1(t) \big)C_{GD} \]

where \( V_{cm} \) is the common-mode level of \( V_p \) and \( V_n \). \( C_{GB} \) is the equivalent capacitance between the gate and substrate, \( C_{gs} \) and \( C_{gd} \) are the gate-source and gate-drain overlap capacitances, respectively. WLC_{ox} refers to the gate oxide capacitance, including the input pair (\( M_{1a}-M_{2a} \)) used for the normal SAR conversion and input pairs (\( M_{1b}-M_{2b}, M_{1c}-M_{2c} \)) used for noise-shaping. In the passive noise-shaping techniques described in the literature, the feedforward gains \( G_{1,2} \) implemented at the inputs of the comparator need to be substantially large to guarantee stability according to (4d), while high \( \alpha_1 \) and \( \alpha_2 \) must be large to reduce the passive integrator's phase error. Since increasing the gains results in increased kickback noise charges, induced at the gate of the input MOS pair \( M_{1,2} \) during both comparison and latch operations, that will degrade the ADC resolution.

The previous analysis concludes that the multi-input comparator gains \( G_{1,2} \) must be large enough to improve the NTF(z) at its DC suppression, satisfying the stability requirement while maintaining small enough to reduce dynamic power and kickback noise, leading to a design trade-off. We can find in the available 2nd order passive NS SAR ADC in the literature, the area of the integrator capacitor is around four times larger than the CDAC capacitor (\( \alpha_{1,2} \equiv 4 \)) and that limits the speed and increases power consumption. Also, the resolution of the ADC is limited by the kickback noise of the multi-input comparator due to high gains \( G_{1,2} \) values.

II-B Direct 2nd order SDM implementation-based noise shaping analysis and its limitations

To improve the noise shaping performance compared to passive implementation, direct noise shaping is derived from an ideal 2nd order SDM. The ideal noise transfer function, \( \text{NTF}_{\text{ideal}}(z) \), is implemented as shown in Fig.3(a)-(b). Since the ideal noise transfer function has no stability issues, it is used directly. Its corresponding loop filter transfer function is:

\[ \text{NTF}_{\text{ideal}}(z) = (1 - z^{-1})^2 \]  

\[ H_{\text{ideal}}(z) = \frac{2z^{-1}-z^{-2}}{(1-z^{-1})^2} \]  

When the normal SAR-ADC conversion is done, the input signal \( V_{in} \) is converted directly into digital outputs through the comparator. Therefore, the STF is always equal to 1 in the NS.
SAR-ADC. Note that the normal SAR-ADC residue after conversion is a low-frequency DC signal and that dictates the choice of the SDM architecture. Two main design strategies could be applied in NS SAR-ADC. The first one refers to the direct implementation method to use a lower-resolution SAR-ADC (< 8-bit) with a noise-shaping module with a strong shaping capability. This strategy is implemented with an active opamp-based integrator, including multiple high-performance opamps, which consume much static power. The second strategy is to use a medium-resolution SAR-ADC (~10-bit) with a noise-shaping module with medium-shaping capability, composed of a very low-power active integrator or passive integrator and consumes less power. Fig.3(a)-(b) shows system-level and circuit-level implementation of the direct implementation refers to the first strategy. When clock φ1 is high, the first stage and the feedforward path sample the normal SAR-ADC conversion residue. The second integrator stage samples the previous value from the first stage integrator output. When the clock φ2 is high, the first stage integrator starts its integration, and at the same time, the second stage integrator and the feedforward path transmit the value sampled in the first half cycle through the output. However, unlike opamp-based sigma-delta modulator design trade-offs, the proposed SAR-ADC requires the SDM input signal to be a DC value, and the amplitude is around 1 LSB of the standard 10-bit SAR ADC without NS, which significantly relieves the slew rate requirement of the opamp. The integration phase has to have a speedy settling response during noise shaping before the comparator works in the following conversion cycle. Consequently, the approximated unity-gain bandwidth of the opamp has to be very high, leading to high power consumption. In addition, opamp with a finite DC gain will introduce higher-order harmonics at the ADC output. As a result, the opamp has to have a fast settling time and large DC gain, but it has a relaxed slew rate requirement.

**II-C Proposed 2nd order passive-Active integrator-based noise shaping analysis**

Fig. 4 illustrates a technique that utilizes positive feedback across a passive 1st order SC integrator, which is inspired by [17-18] and can compensate for the phase error. Moreover, it is possible to compensate for the second stage integrator phase error with an input gain G. A detailed illustration of the block diagram of the proposed SAR-ADC is shown in Figure 5.
The proposed NTF (z) has the following transfer function:

$$H(z) = \frac{\alpha_1 z^{-1} - \alpha_2 (1 - \beta) z^{-2}}{1 - (1 - \alpha_1) z^{-1}}$$

To simplify the design strategy, first, we ignore the resonator optimization. This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/
The proposed NTF(z) has two zeros which refer to as 
\[ z_1 = 1 - \alpha_1 \] and 
\[ z_2 = 1 - \alpha_2(1 - \beta) \]. The closer the zero of the NTF(z) to 1, the stronger the NS capability is, which means the integrator is closer to ideal. Compared with the entirely passive noise shaping techniques, the essential advantage of the proposed solution is that increasing \( G \) to improve the noise shaping capability will not introduce extra power and kickback noise to the comparator. Since the open-loop gain \( G \) and compensation factor \( \beta \) simultaneously work toward achieving better shaping ability, significantly reducing the noise and improving the resolution of the ADC. A better shaping requires a smaller \( \alpha_r \) value that is limited by the KT/C noise. The zero location of \( z_r \) is determined by \( \beta \), where \( \beta \) is set at approximately one to minimize the phase error of the second-stage passive integrator. Moreover, the KT/C noise of the second-stage passive switched capacitor integrator is referred to as the input and will be divided by the opamp gain, so the size of the second-stage integrator capacitors has a negligible effect on the thermal noise. While the lower limit of thermal noise is considered in the first stage passive integrator sampling capacitor \( C_{s1} \) since \( \alpha_1, \alpha_2 \) are designed to be around 0.15~0.25 in the proposed ADC. The minimum \( C_{s1} \) is given by:

\[
C_{s1} = \frac{KT2^{2N}}{OSR(V_{FS})^2} \tag{10a}
\]

where \( K \) represents the Boltzmann constant, \( T \) is the absolute temperature, \( N \) is the effective number of ADC bits and \( V_{FS} \) represents the full-scale input. The second stage output noise is simply equal to the equivalent RC integrator shown in Fig. 1 (b). Thus, the SC resistor \( R \) acts the same as a resistor in terms of thermal noise power which will not influence the noise in the output spectrum. The second stage input-referred noise can be written as:

\[
V_{in,2nd}^2 = \frac{1}{G} \int_0^\infty \frac{4KTR}{1+(2\pi fRC)^2} df = \frac{KT}{GC_{s2}} \tag{10b}
\]
Fig. 8 shows the proposed loop filter designed with passive-active architecture and resonator feedback to improve the ADC noise-shaping performance and bandwidth further. In our proposed noise-shaping module, conjugate zeros are introduced in NTF(z) by adding a local negative feedback loop at the input and output of two cascaded passive-active integrators. The local feedback changes the loop filter poles, making them shift away from DC to enhance the noise shaping performance. To evaluate the performance of the proposed noise shaping module with a resonator, the complete transfer function of the proposed sigma-delta modulator is written as the following, and the simulation of the resonator effect is shown in Fig. 8 (b)-(c).

\[
H_{\text{hybrid-resonator}}(z) = \frac{H_{\text{passive}}(z)H_{\text{active}}(z)+H_{\text{passive}}(z)}{1+\theta H_{\text{passive}}(z)H_{\text{active}}(z)}
\]  

(11)

Reference [17-18] uses a low-gain Opamp with a positive feedback circuit in a discrete-time sigma-delta modulator to solve the gain and phase errors caused by the passive switched capacitor integrator. However, its input signal amplitude is limited to a small range. The ratio of rail-to-rail voltage swing to maximum input swing is 55%. However, in a noise-shaping SAR-ADC, the input signal is first converted fully by the conventional high-speed SAR-ADC and then integrated through the noise-shaping block, and the signal entering the noise-shaping block has a small amplitude. Therefore, this active-passive hybrid noise shaping technique is much more suitable for noise-shaping SAR ADC compared with the sigma-delta modulator. The capacitor ratios \( \alpha_1 \) and \( \alpha_2 \) are composed of capacitance ratios, which have high immunity to process variations. The opamp gain \( G \) is designed by simple common-source amplifiers. The proposed NTF and pole-zero stability analysis in Fig. 7 shows great robustness of the circuits under gain variations. It has demonstrated that with significant variations of \( G \), the proposed NS SAR ADC can maintain its stability as long as \( \alpha_1 \) and \( \alpha_2 \) can be small enough, and the limitations of parameters are the thermal noise of the ADC. Moreover, second-order noise-shaping designed in an active-active module, which realizes an ideal NTF, will not be a proper candidate for two reasons: (1) high sensitivity for the discrete-time loop dynamics compared with the proposed hybrid passive-active solution and (2) common-mode noise leakage from the SAR regular conversion. Like the previous analysis, the stability analysis of active-active noise shaping arrangement is the following:

\[
\begin{align*}
\text{NTF}_{\text{ac}}(z) &= \frac{p_1(z)p_2(z)}{p_1(z)p_2(z) + G_1 \alpha_1 G_2 \alpha_2 z^{-2} + p_2(z)G_1 \alpha_1 z^{-1}} \\
\text{Den}(z) &= p_1(z)p_2(z) \\
\text{NTF}_{\text{ac}}(z = 1) &= \frac{(1-\beta^2)}{2G_2z + G_1(1-\beta)}
\end{align*}
\]  

(12a)

(12b)

Assume \( 1 - \beta = 0 \) due to the positive feedback compensation. \( \text{Den}(z) = z^2 + (G_1 \alpha_1 - 2)z + 1 - G_1 \alpha_1 + G_1 \alpha_2 G_2 \alpha_2 \)

Apply Jury Array for stability gives:

\[
\begin{align*}
\text{Den}(1) &= G_1 \alpha_1 G_2 \alpha_2 > 0 \\
\text{Den}(-1) &= > G_1 \alpha_2 G_2 \alpha_2 - 2G_1 \alpha_1 + 4 > 0 \\
\frac{-z^2}{G_1 \alpha_1} &= 1 < G_2 \alpha_2 < 1
\end{align*}
\]  

(12c)

The active-active module has more strict stability requirements compared with (9c) and (12). Fig. 9 and Fig. 10 demonstrate the active-active module's stability variations and common-mode noise leakage problems. The system simulation of stability analysis shown in Fig. 9 is performed while considering enough design margin of thermal noise from the switch capacitor integrator with, \( \alpha_1 = 0.25 \), \( \alpha_2 = 0.15 \), \( \beta = 1 \) as a typical example. Compared with the proposed technique stability plot in Fig. 7, the stability requirements are stricter, making the circuits more sensitive to PVT variations. Moreover, as shown in Fig. 10, CM noise leakage is severe due to the low opamp gain, which reduces the ADC noise shaping performance. Since the open-loop opamp with low gain will be greatly affected by the common-mode noise suppression from the SAR conversion, the passive stage based on bottom plate sampling is selected as the first stage in the proposed design. While the ideal solution for a low-power NTF implementation is an active-active architecture using an open-loop opamp-based integrator, the variations in the integrator coefficients and the DC gain of the opamp will impact the stability of the entire discrete-time loop dynamics, and it will be sensitive to PVT variations. Equations (12a)-(12c) demonstrate that the gain coefficients \( G_{12} \) are highly related to stability, which is relatively difficult to achieve compared to the proposed passive-active implementation.

III. CIRCUITS IMPLEMENTATIONS AND DISCUSSIONS

Fig. 11 shows the proposed asynchronous SAR ADC architecture. This ADC design adopts the bottom-plate sampling method to minimize charge injection and clock feedthrough from the sampling capacitor during the sampling phase. The bottom-plate sampling mainly takes advantage of disconnecting the sampling capacitor bottom plate so that the leakage charge from the sampling switch will not be injected into the sampling capacitor top plate. Another advantage is that when the proposed NS-SAR-ADC is under the sampling phase, the noise-shaping module can still perform its 2\textsuperscript{nd} integration (refer to Fig. 10 & Fig.14) before the subsequent...
During the normal conversion process of the proposed SAR ADC, the conventional monotonic switching scheme moves the comparator input common-mode level monotonically towards $V_{SS}$ or $V_{DD}$, causing the conversion gain of the comparator to vary with the input, which would introduce signal-dependent offset to the ADC, degrading the linearity and noise-shaping performance of the ADC. The comparator in the preamplification phase has a significant influence on the offset voltage of the comparator [12] and can be written as:

$$V_{os} = \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2} \left( \frac{\Delta S}{S} - \frac{\Delta R}{R} \right)$$

(14)

where $\Delta V_{TH}$ is the mismatch between the threshold voltages of the inputs, $\Delta S$ is the input pair size mismatch, and $\Delta R$ is the

FIGURE 11. Detailed implementation of proposed SAR ADC

FIGURE 12. Circuit of the double tail dynamic comparator (a) self-ring high-speed clock generator (b)

FIGURE 13. Circuit implementation of low gain open-loop amplifier
Loading pair resistance mismatch. In accordance with equation (14), the offset voltage is affected by mismatches in the devices and their bias conditions. The static term in the expression does not impact the precision of the ADC. Moreover, the overdrive voltage has an impact on the second term. MS scheme results in a gradual decrease in the input CM level of the comparator as the MS scheme is employed. To stabilize the comparator input common-mode voltage, [23–26] introduced an additional DC voltage source. The DC voltage reference buffer requires a large driving capacity, introducing extra power consumption. This work proposes the use of identical capacitors in the common-mode-stabilization (CMS) array whose bottom plates will undergo a transition from VSS to VDD to compensate for the CM drop of the MS CDAC as shown in Fig.11. The CMS capacitors are approximately half the size of their MS DAC counterparts. The OR gate that implements the VSS to VDD transition has two inputs: 1P–2P and 1N–2N, respectively. Due to the majority of CM variation occurring around the MSB, CMS is applied to only the first two MSB bits. As a result of the i\textsuperscript{th} comparison, the voltage swing on each side of the DAC is derived as follows:

\[
\Delta V_{\text{pl}} = -B_i \frac{2^{2n-i-1}C_u}{C_T} V_{\text{DD}} + \frac{2^{2n-i-2}C_u}{C_T} V_{\text{DD}} \quad (15)
\]

\[
\Delta V_{\text{nl}} = (B_i - 1) \frac{2^{2n-i-1}C_u}{C_T} V_{\text{DD}} + \frac{2^{2n-i-2}C_u}{C_T} V_{\text{DD}} \quad (16)
\]

where \(\Delta V_{\text{p}l}\) and \(\Delta V_{\text{n}l}\) are the i\textsuperscript{th} positive and negative voltage swings on both sides of the DAC. \(C_u\) is the unit capacitance, \(C_T\) is the total capacitance of the DAC, and \(B_i\) is the i\textsuperscript{th} comparison result. It should be noted in (15)-(16) that the MS network and CMS network are both represented in the first and second terms, respectively. Regardless of the value of \(B_i\), the summation of \(\Delta V_{\text{p}l}\) and \(\Delta V_{\text{n}l}\) remains zero. Therefore, the input CM remains constant at the moment of comparison.

**IV CIRCUITS SIMULATION RESULTS**

Figure 14 shows the proposed NS SAR-ADC timing diagram where the normal SAR-ADC conversion is complete before phi1. The common-mode level remains constant around VDD/2, and the passive integrator1 and active integrator2 are operating when phi1, phi2, and phi3 are switched on, respectively. The CMS circuits allow the comparator to maintain a low offset and prevent metastability. Another advantage of the bottom-plate sampling is that the sampling clock phi1 can also be used as integrator2 integration clock since the new cycle has not yet started during the input sampling phase, increasing the conversion time and improving the ADC speed. The proposed circuits level implementation is working under a 1.8V power supply, 10MHz sampling clock rate, and the dynamic comparator is working under a 150MHz asynchronous clock. Fig.15 shows the power spectrum before and after noise shaping, in which the input signal frequency is about 250KHz, which is within 1/4 of the ADC bandwidth to include the 3\textsuperscript{rd} order harmonics in the bandwidth.

The designed conventional high-speed asynchronous SAR-ADC without noise shaping shown in Fig.15(a) can achieve only 9.01-bit effective number of bits (ENOB). Fig.15(b) and Fig.15(c) show the proposed 2\textsuperscript{nd} order hybrid passive-active noise-shaping SAR-ADC with/without a resonator formed by a negative feedback path between the proposed two cascaded

![Figure 14. Proposed SAR-ADC time-domain working principle](image-url)

![Figure 15. (a) Proposed SAR-ADC without noise-shaping](image-url)

![Figure 15. (b) Proposed SAR-ADC with noise-shaping + resonator](image-url)

![Figure 15. (c) Proposed SAR-ADC without the resonator](image-url)
passive/active integrators. The negative feedback loop is introduced to change the position of the zeros of the NTF(z) so that the bandwidth of the ADC can be further improved and noise suppression capability is strengthened. The signal-to-noise and distortion ratio (SNDR) is improved by 5dB, which demonstrates very good agreement with the system-level simulation results from Fig.6. The performance comparison with other works is summarized in Table I.

| Parameters                      | This work | [4] | [5] | [6] | [8] |
|---------------------------------|-----------|-----|-----|-----|-----|
| Technology                      | 180nm CMOS | 40nm CMOS | ---- | 180nm CMOS | 65nm CMOS |
| Order                           | 2         | 2   | 3   | 2   | 2   |
| integrator phase error optimization | Yes | No | No | No | No |
| NTF zero optimization           | Yes | No | No | No | No |
| ADC bits                        | 14.56     | 13  | 10  | 16.88 | 13.2 |
| bandwidth                       | 1MHz      | 262kHz | 100kHz | ----- | 2MHz |
| Fs (sampling frequency)         | 10MS/s    | 8.4MS/s | 20MS/s | 576MS/s | 100MS/s |
| SNDR                            | 89.4      | 80  | 99.7 | 104 | 81.2 |
| Power(mW)                       | 880       | 143 | ----- | ----- | 561 |

Simulation Results *Measurement Results

V. CONCLUSION

The paper proposed a novel high-speed SAR-ADC with 2nd-order noise shaping. The noise shaping technique is designed as a passive-active arrangement, utilizing a low-gain, open-loop amplifier with positive feedback. This implementation reduces the area required for passive integrator noise shaping and compensates for the gain and phase errors from passive implementation. The common-mode stabilization technique is applied along with the monotonic switching technique, which prevents the common-mode level shift during SAR conversion and helps to improve the circuit’s performance. The circuits simulation results in 180nm achieving an SNDR of 89.4 dB, an SFDR of 98.6 dB, and a THD of 0.003%3. The power consumed is 880 μW at a supply voltage of 1.8V.

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REFERENCES

[1] Fredenburg, J. A., & Flynn, M. P. (2012). A 90-m/s/11-MHz bandwidth 62-dB snr noise-shaping sar adc. IEEE Journal of Solid-State Circuits, 47, 2898–2904.
[2] Chen, Z., Miyahara, M., & Matsuzawa, A. (2016). A second-order fully-passive noise-shaping SAR ADC with embedded passive gain. In 2016 IEEE Asian Solid-State Circuits Conference (ASSCC) (pp. 309–312).
[3] Chen, Z., Miyahara, M., & Matsuzawa, A. (2016). A 9.35-ENOB, 14.8 fJ/conv.-step fully passive noise-shaping SAR ADC. IEICE Transactions on Electronics, 99, 963–973.

[4] Guo, W. N., Zhuang, H., & Sun, N. (2017). A 13b-ENOB 173dBFS 2ndorder NS SAR ADC with passive integrators. In 2017 Symposium on VLSI Circuits (pp. C236–C237).
[5] Payandehnia, P., Mirzaie, H., Maghami, H., Muhlestein, J., & Temes, G. (2017). Fully passive third-order noise shaping SAR ADC. Electronics Letters, 53, 528–530.
[6] Yi, P., Zhu, Z., Li, D. et al. An opamp-free second-order noise-shaping SAR ADC with 4+ passive gain using capacitive charge pump. Analog Integr Circ Signal Process, 105, 125–133 (2020).
[7] Shikata A, Sekimoto R, Kuroda T, et al. A 0.5 V 11 MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS. IEEE J Solid-State Circuits, 2012, 47(4): 1022
[8] Y. Song, C. Chan, Y. Zhu, L. Geng, S. U. and R. P. Martins, "Passive Noise Shaping in SAR ADC With Improved Efficiency," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 2, pp. 416-420, Feb. 2018, doi: 10.1109/TVLSI.2017.2764742.
[9] Z. Chen, M. Miyahara and A. Matsuzawa, "A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain," 2016 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2016, pp. 309-312, doi: 10.1109/ASSCC.2016.7844197.
[10] Ginsburg B P, Chandrakasan A P. "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC". IEEE Int Symp Circuits and Systems (ISCAS), 2005
[11] Liu CC, et al. “A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 _m CMOS process”. Symposium on VLSI Circuits Digest of Technical Papers, 2009.
[12] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill, Inc, 2000
[13] Schinkel D, et al. “A double-tail latch-type voltage sense amplifier with 18 ps Setup-Hold time”, IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2007
[14] Chen M, Brodersen W. A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13- _m CMOS. IEEE J Solid-State Circuits, 2006, 41(12): 2669
[15] Promitzer G. “12-bit low-power fully differential non calibrating successive approximation ADC with 1 MS/s”. IEEE J Solid-State Circuits, 2001, 36(7): 1138
[16] Agnes A et al. "A 0.92 mW 10-bit 50-MS/s SAR ADC with time-domain comparator". IEEE International Solid-State Circuits Digest of Technical Papers (ISSCC), 2008
[17] A. Hussain, S. Sin, C. Chan, S. Ben U, F. Maloberti and R. P. Martins, "Active-Passive _Delta Sigma Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364-374, Jan. 2017, doi: 10.1109/TVLSI.2016.2580712.
[18] A. Hussain, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "NTF zero compensation technique for passive sigma-delta modulator," in Proc. IEEE PRIMEASIA, Oct. 2011, pp. 82–85.
[19] JM de la Rosa. Sigma-Delta Converters: Practical Design GuidelM]. Hoboken, NJ, USA: Wiley–IEEE Press, 2018, 86-90.
[20] S. Pavan and P. Sankar, "Power reduction in continuous-time delta-sigma modulators using the assisted opamp technique," IEEE J. Solid-State Circuits, vol. 45, no. 7, pp. 1365–1379, Jul. 2010.
[21] Liu C, Chang S-J, Huang G-Y, et al. A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 _m CMOS process. Symposium on VLSI Circuits Digest of Technical Papers, 2009: 236
[22] Lei, KM., Mak, Pl. & Martins, R.P. Systematic analysis and cancellation of kickback noise in a dynamic latched comparator. Analog Integr Circ Sig Process 77, 277–284 (2013).
[23] Song H, Leea M. Asymmetric monotonic switching scheme for energy-efficient SAR ADC. IEICE Electronics Express, 2014, 11(12): 1–5
[24] Shahrmoohamadia M, Ashtiani S J. Energy and area efficient tri-level switching procedure based on half of the reference voltage for SAR ADC. IEICE Electronics Express, 2012, 9(17): 1397–1401
[25] Zhang Y, Chen H, Guo G, et al. Energy-efficient hybrid split capacitor switching scheme for SAR ADCs. IEICE Electronics Express, 2016
[26] Zhu Y, Chan C H, Chio U F, et al. A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. IEEE J Solid-State Circuits, 2010, 45(6): 1111–1121
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