Research on the High Speed with Low Noise Signal Processing Circuit

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Abstract. In background of the trends of the high-resolution remote sensing camera, based on the theory of Signal Integrity, taking advantage of a software named Cadence, proposed a resolution of a high speed with low noise signal processing circuit.

Introduction

In view of the current development level of on-board CCD camera, a special research is carried out to further improve the design level of on-board CCD camera video circuit, in order to achieve high-resolution camera to provide a solid technical guarantee. Based on the theoretical research, Combined with the actual circuit, this paper attempt to improve the performance of the signal processing circuit.

Main Function

Select to receive an image analog electronic signal of a CCD in 8 channels via single-ended or differential mode, and convert it into a single signal after filtering noise reduction. Convert analog electrical signals into digital image signals by pre-processing, filtering and related dual sampling, gain control, and module conversion.

Complete the acquisition of CCD camera video signal and through data synthesis and signal conversion.

Provide 2 differential parallel outputs and related clocks and synchronous signals.

Figure 1 below is a functional block diagram of this scenario.

Circuit Design

The entire signal processing circuit can be divided into input and output interface, power supply and filtering, related dual sampling and A/D conversion, data synthesis, timing control and other parts, the following diagram gives the overall structure of the signal processing circuit frame:

Power Filter Design

Because noise on various power supplies is coupled to different degrees into the signal, the
signal-to-noise ratio is reduced\textsuperscript{[1][2]}. Therefore, the CCD power supply is also sufficiently filtered to reduce the noise coupled from the power supply to the CCD analog signal or image digital signal.

At the circuit board input interface, the power supply can be filtered using THE LC filter circuit, and for reliability reasons, two tantalum capacitor series of the connection method, the schematic as shown in Figure 3. The necessary decoupling capacitors should also be designed at the power pin of the device.

![Figure 2. Overall structural diagram of signal processing circuit.](image)

**Amplification Filter Circuit**

The analog electrical signal of the CCD output is weak, and the pre-amplification circuit amplifies the CCD analog signal, and the CCD analog signal is filtered and impeded by the filter design. In order to maintain a high signal-to-noise ratio during amplification, it is required that the pre-amplification circuit should have very low voltage and current noise, and that the lower input bias current be lower\textsuperscript{[3]}.

The line array CCD reads the schematic of the amplification filtering circuit as follows.

![Figure 4. Line array CCD reads out the schematic of the amplification filter ingress circuit.](image)

The choice of using the feedback resistor to be placed is critical, and the following diagram shows the frequency response curve for the amplifier to select a different feedback resistor at the gain of 2V/V.
From the figure above, you can see that a smaller feedback resistor (200Ω) has an overshoot in its frequency response curve, while a larger feedback resistor (700Ω) has a frequency response curve that drops too fast and the bandwidth is narrower. In the circuit design, the gain and bandwidth can be determined by the value of the feedback resistors $R_1$ and $R_2$, and the appropriate feedback resistor is required according to the specific conditions of the circuit.

The feedback resistor $R_F$ obtained by the schematic is $R_f$ in Figure 3, and the filter gain $A_V=2$ is designed, according to the circuit gain formula:

$$A_V = \frac{U_o}{Ui} = 1 + \frac{R_1}{R_2}$$

Therefore $R_1=R_2$, the application of Cadence to the amplifier bandwidth Pspice simulation, testing the feedback resistance of different resistance son to filter circuit bandwidth. Fig.6 is a simulation schematic.

The simulation results are as follows:

When $R_F=300Ω$, 3dB bandwidth cutoff_lowpass_3dB (Vout) is 335.32440 MHz, Although the bandwidth is wide, there is a significant overshoot near 200MHz.
when $R_F=500\Omega$, the overshoot swells impressed, but there are still drum packs around 107MHz.

when $R_F > 600\Omega$, the overshoot disappears completely and the bandwidth decreases accordingly:

- $R_F=620\Omega$, cutoff_lowpass_3dB(Vout)=274.35239Meg
- $R_F=750\Omega$, cutoff_lowpass_3dB(Vout)=244.19178Meg
- $R_F=820\Omega$, cutoff_lowpass_3dB(Vout)=228.72964Meg
- $R_F=910\Omega$, cutoff_lowpass_3dB(Vout)=209.88066Meg
- $R_F=1000\Omega$, cutoff_lowpass_3dB(Vout)=192.44786Meg
- $R_F=1500\Omega$, cutoff_lowpass_3dB(Vout)=124.63946Meg

From the above experimental results, it can be concluded that the analog amplifier bandwidth narrows with the increase of the feedback resistance $RF$, and when the $RF$ is too small to produce overshoot, and the resistance value is too large, the bandwidth becomes too narrow to meet the design requirements\[4\][5]. According to the design requirements require about 200MHz bandwidth, so choose the 1K-plus resistance value as the feedback resistance.

**ADC Circuit**

The mode number conversion is the main function that the signal processing circuit needs to realize in this topic. Its main input and output signal sits below:
However, since the selected AD is packaged for CSP-BGA, this can make it difficult to lay out and route in the PCB design. Due to the large number of pins and the small pitch between the pins, the following measures can be taken in order to ensure the success of the wiring from the point of view:

1) Using the deep hole technology, this measure can maximize the wiring space, so that the wiring is easier. However, this method will encounter many limitations of plate making process. As the same layer cannot appear three or more different buried holes, blind holes cannot appear staggered, both cases are now difficult to complete the plate process. Figure 17 represents the above two unrealized buried hole designs.

As shown in the figure, the TOP layer has three different sinkholes, namely Drill1 from TOP to MID1, Drill2 from TOP to MID2, and Drill3 from TOP to MID3. At the same time, Drill3 and Drill4 are interleaving, and this design needs to be avoided if the deep hole technology is to be used.

2) The design and placement of the perforation, in order to avoid the process limitation of of buried hole processing, can use the perforation design, for the design of the perforation, the placement of the perforation is particularly important. Two schemes can be taken to optimize the hole layout, one, because BGA pins are generally matrix distribution, with its center as the origin, the pin is divided into four quadrant areas, the first quadrant of the pin through the upper fan to the right, the second quadrant pin through the hole to the left upper fan out, the third, the fourth quadrant pin foot per hole respectively in the lower left and lower right direction fan out. In addition, its perforation should be placed in the center of the four pins. This placement design maximizes cabling space.

Figure 9. AD converter part input and output signal graph.

Figure 10. A design schematic of the sinkhole that cannot be realized by the plate-making process.
In addition, the multi-layer circuit board design needs to be used in PCB design, and the device location and PCB lamination are reasonably arranged.

**Conclusions**

The future development of camera to high-resolution digitalization has become an unquestionable trend, to achieve higher resolution not only to the front-end optical system has higher requirements, but also for imaging circuits have different technical indicators than before. Based on the theory of signal integrity, a design scheme for high-speed low-noise signal processing circuit is proposed by using Cadence software. It is hoped that its successful application will make China's remote sensing camera development level set a new level.

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