Hardware-Assisted Detection of Firmware Attacks in Inverter-Based Cyberphysical Microgrids

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Abstract—The electric grid modernization effort relies on the extensive deployment of microgrid (MG) systems. MGs integrate renewable resources and energy storage systems, allowing to generate economic and zero-carbon footprint electricity, deliver sustainable energy to communities using local energy resources, and enhance grid resilience. MGs as cyberphysical systems include interconnected devices that measure, control, and actuate energy resources and loads. For optimal operation, cyberphysical MGs regulate the onsite energy generation through support functions enabled by smart inverters. Smart inverters, being consumer electronic firmware-based devices, are susceptible to increasing security threats. If inverters are maliciously controlled, they can significantly disrupt MG operation and electricity delivery as well as impact the grid stability. In this paper, we demonstrate the impact of denial-of-service (DoS) as well as controller and setpoint modification attacks on a simulated MG system. Furthermore, we employ custom-built hardware performance counters (HPCs) as design-for-security (DfS) primitives to detect malicious firmware modifications on MG inverters. The proposed HPCs measure periodically the order of various instruction types within the MG inverter’s firmware code. Our experiments illustrate that the firmware modifications are successfully identified by our custom-built HPCs utilizing various machine learning-based classifiers.

Index Terms—Microgrids, smart inverters, firmware attacks, hardware performance counters.

I. INTRODUCTION

The electric power grid is transitioning from an utility-centric and hierarchical system to a decentralized, dynamic, and intelligent grid. This transformation relies on incorporating renewable resources, microgrids (MGs), demand-response mechanisms, smart metering infrastructure, and distributed energy resources (DERs). Renewable portfolio standards promote the adoption of DERs including energy storage systems, electric vehicles, solar photovoltaic (PV) plants, and grid-tied solar inverters. For instance, California has a goal to generate 50% of its power demand using only renewable resources by 2030 [1]. According to the International Energy Agency (IEA), the globally distributed solar PV capacity is expected to increase more than 250% in 2019-2024, reaching 530 GW [2]. Furthermore, by 2050, the forecasted solar and wind generated capacity will account for almost 30% of the U.S. electricity demand [3].

The rapid growth of the solar energy market is enabled by the widespread deployment of solar inverters. A solar or PV inverter is an electrical converter which converts the variable direct current (DC) output of a PV solar panel into the utility frequency alternating current (AC), and thus supply the grid or use it locally off the grid. Contrary to traditional plants, solar PV plants and in general DERs are operated by end-users and aggregators; hence, utilities have limited control of the power generation. For instance, residentially deployed solar inverters (e.g., in home installations) are considered consumer electronic devices [4]. Inverter management systems enable users to analyze energy consumption and generation patterns to optimally control home energy expenditure and minimize operational cost [5]. However, to harness these features and fine-tune inverter performance, constant communication with the utility grid is required to ensure current information (e.g., energy prices, demand-response schemes, etc.).

The IEEE 1547 interconnection standard specifies the DER communication requirements as well as the control functions which should be provided to independent system operators (ISO) and distribution system operators (DSO) [6]. Despite the importance of ensuring compliance with the recommendations of IEEE 1547 – as it can significantly reduce threats targeting the communications and control commands issued between utilities and DERs – cyberattacks that can disrupt the normal operation still remain as potential threats. For instance, adversaries can compromise DER-to-utility communications to perform denial-of-service (DoS) attacks severely impacting the distribution system operation.

Although network segmentation could minimize potential attack entry points, it can introduce issues. Enforcing firewall rules, virtual private networks (VPNs), secure enclaves, etc. helps monitoring bidirectional traffic. However, such methods increase latency, network administration overheads, and in the case of DER networks (which are constantly expanding integrating new devices and are not centrally controlled or owned by one entity), they are often infeasible [7]. Only recently, works which address computation overheads induced by securing DER communications have been proposed. For instance, the authors in [8] propose a lightweight hardware-based security primitive leveraging real-time grid device entropy to enable secure communication between power system assets. They validate the framework practicality in a simulation environment where DER and grid devices utilize IEEE 1815-Distributed Network Protocol v3 (DNP3) for secure authentication purposes [9], [10].

Apart from attacks that target the availability of DER assets through their communication functionalities, malicious attacks can also target the actual physical components of DER devices such as smart solar (micro-)inverters and controllers. Following the same trend with most consumer electronics,
manufacturers typically design DER embedded controllers using commercial-off-the-self (COTS) components, and therefore, vulnerabilities of these modules can be also exploited in such critical devices. In addition, DERs' control units often have limited computing capabilities relying on low-level hardware systems for their operation without running an operating system [11]. They typically boot monolithic, single-purpose firmware and the tasks are executed in a single-threaded super-loop based execution.

Furthermore, to minimize cost, manufacturers overlook the security of these controller devices [12]. Software patches are typically issued to address security flaws post-deployment. Such updates can be performed manually, i.e., by the device user or certified personnel, using the wired network that the device is connected to, or over-the-air (OTA) for wirelessly connected devices. In [13], the authors demonstrate that attackers can intercept data in-transit during OTA update procedures, modify them, and update (remotely) malicious firmware images to programmable controller devices compromising their operation. In order to address the evident vulnerability of firmware updates from untrusted sources, the authors of [14] provide a streamlined approach for secure firmware updates, however such solutions have yet been deployed in industrial and commercial embedded systems. Contrary to industrial controllers and other embedded devices of cyberphysical systems which might be protected by sophisticated security perimeters (e.g., firewalls, VPNs, network enclaves, demilitarized zones, etc.), smart inverters are often vulnerable against adversaries with limited system knowledge and resources [15], [16]. Thus, attacks targeting the firmware of such embedded systems, as outlined in Fig. 1 can cause severe impacts to critical infrastructure. A recent example is the Trisis incident in 2017 targeting petrochemical plants in Saudi Arabia. The attackers were able to compromise six emergency shut down controllers managing critical industrial processes (e.g., burner management) [17]. If the attack was not timely identified, human lives would be in danger if harmful gases were released in the petrochemical facility.

In order to mitigate the inherent vulnerabilities of embedded controllers including smart inverters, anti-virus software (AVS) has been utilized for the detection of malicious code. However, attackers have been able to evade AVS through diligently constructing attacks. For example, attackers can create viruses that modify the appearance of the code while maintaining malicious functionality [18]. Thus, a cat-and-mouse race between attackers and AVS ensues. Attackers attempt to develop novel methods for evading AVS, while AVS seeks to fortify its defenses. The persistent bolstering of AVS leads to large computational bandwidth and performance overhead. Furthermore, AVS cannot always identify polymorphic and metamorphic malware that can change their execution format in each iteration of propagation [19]. In order to address the issues with AVS, researchers have proposed hardware malware detectors (HMDs) [20]–[22].

HMDs utilize hardware features which, compared to AVS, are more robust since compromising them is extremely challenging [19]. Moreover, since HMDs operate on actual hardware, the malware detection latency is lower. Hardware performance counters (HPCs) have emerged as a promising candidate for HMDs. HPCs are dedicated registers that keep track of low-level microarchitectural events such as the number of branch-misses, CPU cycles, instructions, etc. Towards malware detection, HPC values collected from the execution of applications can be used to train machine learning (ML) models, which classify the programs as benign or malicious [23]–[25]. Despite the detection and performance benefits of HPC-based HMDs, directly applying it to MG systems is not feasible, since some embedded legacy controllers do not provide HPC support.

In this paper, we leverage custom-built HPCs as design-for-security (DfS) primitives for firmware-based solar inverter controllers. These custom-built HPCs keep track of the sequence of instructions inside the controller firmware. We utilize ML classifiers and differentiate between maliciously modified and benign firmware versions. Specifically, our contributions are as follow:

- We design firmware modification attacks for solar inverters considering their characteristics and how they operate in a MG setup,
- We assess the impact of these attacks targeting the smart inverter controller on a simulated MG architecture,
- We design custom-built HPCs to enable detection of malicious firmware modifications for such inverter controllers that do not support HPC functionality, and,
- We utilize different ML classifiers to detect the firmware modification attacks using our custom-built HPCs values.

The rest of the paper is organized as follows. Section II presents the background and some preliminary definitions. Section III describes related work on power systems cybersecurity and HPC-based malware detection. Section IV describes our proposed methodology and Section V presents the experimental results. Finally, Section VI concludes the paper and gives directions for our future work.
II. BACKGROUND

The following subsections include short descriptions of power systems preliminaries as well as background on HPCs and ML classifiers used in this study.

A. Power System Preliminaries

The next generation of the power grid, often referred to as smart grid, leverages information and communication technologies in order to efficiently and reliably supply electricity [26], [27]. Contrary to traditional power systems where electricity flows in one-way from bulk generation facilities to consumers and loads, smart grid enables bidirectional flow of energy and information between prosumers, consumers, and utilities. A MG is a group of generation resources (e.g., natural gas or biogas generators, wind turbines, solar PV, etc.), energy storage systems (ESS), and loads (residential, commercial, or/and industrial), which can operate either in connected or autonomous/islanding mode. MGs normally operate connected to and synchronous with the grid, but they can also function autonomously if necessary (e.g., extreme weather events, utility load shedding to maintain stability, etc.). MGs retain all the smart grid characteristics including bidirectional energy flow and communication. MGs also serve as buffers between the MG-integrated devices and the actual grid. Utilities, instead of independently communicating and controlling each device on the distribution level (e.g., distributed generators, inverters, energy storage, loads, etc.), hand over control to MG management systems. Thus, by serving as a nexus between utilities and devices, MGs help reduce significant communication delays, costs, and computation resource overuse [28]. We will leverage a similar approach in our impact analysis; the specific details of our MG setup are presented in Section V-A.

Different inverters exist in order to accommodate the field application requirements of grid systems [29], [30]. For instance, depending on the generation source, inverters can be categorized as solar, battery, thermoelectric, and hybrid inverters. Solar inverters are electronic devices which enable the conversion of DC power generated by the PV panels to AC power which can be fed back to the power grid or can be supplied to local appliances. Additionally, based on their output characteristics, inverter technologies can be of square wave, sine wave, or modified sine wave [31]. Depending on the connection practice, inverters are also classified as off-grid or grid-tied. In this work, we focus on solar, pure AC sine, and grid-tied microinverters which are the most prevalent topology in MGs [32].

The main difference between standard solar inverters and microinverters is that for the former, the output of an array of interconnected solar panels is provided to the centralized solar inverter, while for the microinverter, every panel is connected to its own microinverter. The main disadvantage of standard inverters is that the generated power depends on their least efficient solar panel. Microinverters are optimally designed to take full advantage of the connected PV panel reaching power conversion efficiency of up to 96% [33]. This is achieved using the maximum power point tracking (MPPT) mechanism embedded in the microinverter, which ensures that the maximum available power can be extracted from the PV panel under the varying environmental conditions (e.g., shading, high ambient temperature, etc.). In the rest of the paper, the terms inverter and microinverter are used interchangeably, without loss of generality, since similar principles dictate their operation.

The dependency of microinverters on COTS components provides the “smart” functionalities of modern embedded devices such as remote OTA updates, communication and control support functions, and high-speed data sampling and acquisition. However, this also incurs security vulnerabilities [34], [35]. In addition to being deployed in insecure or unsupervised environments, these controllers were not initially developed with security in mind, and their resource-constrained architectures provide limited options for improvements in this direction. Multiple attacks targeting controllers in industrial control systems and critical infrastructure have been reported in literature highlighting the need for potent attack detection frameworks [36]–[40].

B. Hardware Performance Counters

In order to detect firmware attacks on MG systems, we utilize HPCs. HPCs are special-purpose registers, found in most modern processors, that monitor critical low-level microarchitectural events like the number of cache-misses, branch-misses, instructions, etc., and developed to improve system performance. Typically, HPC collection is attained through operating system packages such as perf in Linux systems, or other software binaries like quickhpc utilizing the PAPI framework. The number of HPCs that are accessible as well as the number of HPCs that can be monitored simultaneously differ from processor to processor. Some processors only support a couple of HPCs while others support tracking of multiple events. In situations where HPCs are unavailable or limited, custom HPCs can be designed to keep track of features that encapsulate a program’s functionality. In recent past, HPCs have been utilized along with ML classifiers to detect malicious applications [19], [25].

C. Machine Learning Classifiers

In this part, we furnish a brief explanation for the ML classifiers utilized in our experiments. We also present a background on principal component analysis (PCA) used to reduce the number of features. Finally, we explain the various metrics used for quantifying the performance of the utilized ML algorithms.

1) ML Classifiers: A decision tree (DT) is an algorithm where the classification model that is built is in a top-down recursive tree like structure, using mutually exclusive if-then rule set. The rules for the model are sequentially learned one at a time based on the initial training dataset [41]. A neural network (NN) is a ML classifier that utilizes a set of neurons and layers. Neurons are computational units interconnected between each other, and every connection contains a weight linked to it [42]. The classifier learns and adjusts weights as the model is trained to correctly classify the proper label for the input tuples. A random forest (RF) is a model that operates as an ensemble incorporating many DTs. For classification
problems, the model functions by having each DT furnish a prediction, and the output of the RF classifier is the prediction that is most selected [43]. This model operates on the concept that a group of uncorrelated trees will provide better results as opposed to utilizing a single tree.

2) PCA for Feature Selection: Although a processor can consist of multiple HPCs, only few of them can be monitored simultaneously. In order to reduce the set of HPCs to be monitored, we use PCA, a feature selection technique managing high dimensionality data with multiple variables. It is a data reduction technique allowing the user to specify the number of principal components in the transformed data. PCA first calculates the covariance matrix which is formed from the initial dataset of features. The covariance matrix contains all possible combinations of variance between two variables. Singular value decomposition is used to factorize the matrix and extract data in the directions with the highest variances [44]. Based on the specified principal components, the values in the matrix correspond to the features in the initial dataset. The best features can be selected based on the largest values.

3) ML Terminology and Metrics: In this section, we furnish the definitions for some ML terminology and measurement metrics utilized in this paper. A true positive (TP) is a malicious application correctly labeled malicious and a true negative (TN) is a benign application accurately classified as benign. A false positive (FP) is a malicious application incorrectly classified as benign, while a false negative (FN) is a benign program mistakenly tagged malicious.

Accuracy is the proportion of the number of predictions correctly classified to the total number of predictions made.

\[
\text{Accuracy} = \frac{\text{No. of (TP + TN)}}{\text{No. of (FP + FN + TP + FN)}}
\]  

Precision represents the ratio of positive class classifications that are correct.

\[
\text{Precision} = \frac{\text{No. of TP}}{\text{No. of FP} + \text{No. of TP}}
\]

Recall is the proportion of correct positive classifications to the total number of positive classifications.

\[
\text{Recall} = \frac{\text{No. of TP}}{\text{No. of FN} + \text{No. of TP}}
\]

III. RELATED WORK

The rapid integration of DERs and smart inverters in the power grid, besides the operational benefits, raises many security concerns. Cyberattacks targeting embedded systems and programmable controllers have been launched with varying degrees of impact, ranging from economic losses and power outages to even life-threatening scenarios [37], [39], [45]–[47]. Research has emphasized the impact that cyberattacks targeting smart grid assets, e.g., smart inverters, can have on MGs as well as the power system in general [48]. Despite the cybersecurity standards and mitigation strategies which have been proposed to enhance grid stability, implementing such approaches results in performance overheads and often requires specialized equipment which cannot be retrofitted to deployed legacy devices or ported to proprietary architectures [49], [50]. For instance, security solutions leveraging trusted platform modules (TPMs), secure boot, and cryptographic signatures used to validate the integrity of firmware updates, could address some of the aforementioned issues. However, they incur an additional overhead of extra hardware modules and extensive redesign of the deployed and resource-constrained systems. Thus, novel vendor-agnostic methods – utilizing the inherent embedded system infrastructure – are essential to provide better situational awareness and aid the early detection and recovery of abnormal system operation.

Prior works have shown the capabilities of defending against malicious firmware. The authors in [51] proposed a software-only attestation method, VIPER, that checks the peripherals’ firmware’s integrity. This defense approach assumes that the host CPU and operating system have not been compromised. The work in [52] utilized a signature verification code method in the bootloader, which is assumed to have sufficient memory space, to prevent malicious firmware from being installed onto a mouse. In [53], the authors proposed a cumulative attestation kernel architecture consisting of flash microcontroller units for remote attestation assurance that allowed the inspection of the integrity of an application’s firmware. Other works like [54] utilized the addition of an on-chip control flow monitoring module that detects malicious firmware by checking the control flow integrity in a system. However, this technique incurs high performance and storage overhead.

In this work, we use HPC-based AVS for detecting malicious firmware modifications of MG inverters. Utilization of HPCs for detecting malware was initially proposed by [20], [55], which was improved upon by applying ML models in conjunction with HPCs for application classification [19]. The work in [56] detected malware in cyberphysical systems through real-time quantification of HPCs. The study in [24] proposed 2SMaRT, an approach that selects the best HPCs through feature selection and applies a two-stage classifier for malware detection. In addition, the authors in [57] developed HPCMalHunter which produces behavioral vectors for programs created from the HPCs for real-time malware detection. Furthermore, the works in [22], [25] extended utilizing HPCs in embedded control systems to detect malicious firmware modifications through a comparison-based approach. Since some systems lack adequate HPC capabilities, various methods of custom HPCs have been proposed in prior works for malware detection. Researchers have defined and explored detecting malicious applications through ML models trained on sub-semantic features [21], [58]. On the other hand, custom HPCs that count the ordering of specific instructions at the assembly level are used to train ML classifiers capable of detecting morphing malware [59].

IV. PROPOSED METHODOLOGY

In this section, we provide an overview of our threat model as well as the critical components of the MG inverter controller and the firmware attacks we designed to disrupt MG operations. Furthermore, this section describes our proposed custom HPC-based methodology to detect firmware modifications.
the microinverter operation, or through remote exploits (e.g., by intrusively uploading the malicious firmware and affecting the microinverter operation, or through remote exploits (e.g., OTA firmware update functionality). The attacker exploits the power conversion process, thereby adversely affecting the MG operation by injecting malicious code which either manipulates the operation setpoints or alters the sensor measurements received by the controller unit. These stealthy process-aware attacks targeting embedded devices and programmable logic controllers, are difficult to detect and can have various degrees of impact from equipment failures to catastrophic collapse of the industrial cyberphysical system. We demonstrate and discuss the impact of the attacks on the system in Section V. Further, we exclusively investigate custom-built security primitives which employ the innate functionalities of embedded devices without requiring sophisticated software (e.g., cryptographic signatures), hardware (e.g., TPMS), or compound (e.g., secure boot) security extensions.

A. Threat Model

Our threat model considers an attacker who intends to compromise the microinverter controller aiming to impact the power conversion process. In order to achieve this goal, we assume that the attacker has compiled a counterfeit firmware version and attempts to port it to the actual device. Thus, the attack focal point is on the application level and aspires to trigger abnormal operations via static firmware modifications. The adversarial access can either be physical, by intrusively uploading the malicious firmware and affecting the microinverter operation, or through remote exploits (e.g., OTA firmware update functionality). The attacker exploits the power conversion process, thereby adversely affecting the MG operation by injecting malicious code which either manipulates the operation setpoints or alters the sensor measurements received by the controller unit. These stealthy process-aware attacks targeting embedded devices and programmable logic controllers, are difficult to detect and can have various degrees of impact from equipment failures to catastrophic collapse of the industrial cyberphysical system. We demonstrate and discuss the impact of the attacks on the system in Section V. Further, we exclusively investigate custom-built security primitives which employ the innate functionalities of embedded devices without requiring sophisticated software (e.g., cryptographic signatures), hardware (e.g., TPMS), or compound (e.g., secure boot) security extensions.

B. Microinverter Controller

The objective of a grid-tied inverter is to convert DC power, provided either from PV panels or energy storage systems, into AC power that can be sourced to the AC grid or MGs. This process is supported by CMOS devices used as switches and filters as well as voltage and frequency control modules (e.g., pulse width modulation – PWM). The architectural components of a solar inverter are outlined in Fig. 2.

Microinverters are typically preferred over typical inverter topologies for residential and PV deployments in the distribution grid level (< 33 kV) due to their higher efficiency. A critical component that enables microinverters to attain high power conversion efficiency is their MPPT controller. MPPT algorithms aim to find the optimal voltage or current point which will allow for the maximal power generation under the constantly changing exogenous conditions affecting the solar PV panels (solar irradiance, shading, temperature, etc.). A variety of MPPT tracking algorithms have been proposed by researchers. Two of the most commonly utilized MPPT methodologies, which rely on a hill-climbing process to reach the optimal conversion point, are the perturb-and-observe (PnO) method and the incremental conductance scheme. Both of the techniques require that the PV real-time generation attributes, i.e., voltage and current, are measured periodically. In this paper, we adopt the PnO MPPT strategy. However, given the similarities between PnO and incremental conductance our analysis can be generalized for both methods. The PnO MPPT tracker uses the sensed PV attributes (voltage $V_{rt}$, current $I_{rt}$) to generate the reference current which regulates the DC/DC flyback power stage of the microinverter. An overview of the PnO operation is presented in Algorithm 1.

During operating conditions, the PV generation varies due to environmental factors, e.g., solar irradiance and temperature. The voltage-to-current relationship for each PV module differs according to its operating point, hence MPPT algorithms account for these variations. In both the PnO and the incremental conductance methods, the power gradient is utilized in order to reach the MPPT (hill-climbing methods). By leveraging the real-time $V_{rt}$ and $I_{rt}$ measurements of the PV and the $\frac{\partial P}{\partial V}$, $\frac{\partial I}{\partial V}$ gradient, we can determine if the MPPT point is reached, and if not, which are the necessary steps in order to approach it. Algorithm 1 provides a discretized version of the described procedure, similar to the ones prescribed in commercial solar inverters such as the microinverter module used in our experiments.

Since the microinverter’s MPPT leverages the real-time PV measurements in order to extract the maximum available power from any given PV module, attackers can maliciously control the microinverter operation by stealthily tampering the sensed measurements via firmware modification attacks. Furthermore, attacks on the MPPT module can lead to large-scale impact as the MPPT function also controls the DC/DC boost module which is interfaced to the the DC/AC power conversion block (Fig. 2). As a result, frequency and voltage fluctuations can be ported to the grid-tied end of the microinverter. In Section V we demonstrate three different attack scenarios on the MG system operation with varying degrees of impact.

C. Firmware Attack Designs

Firmware attacks commonly seek to either shutdown the operation of the firmware-controlled device or cause malicious...
behavior that would result in an erroneous system output \[62\]. In this section, we discuss the set of developed attacks which emulate common scenarios that adversaries might exploit in solar microinverter code.

1) DoS Attacks: DoS attacks cause the system to be unavailable and not function properly. In other words, the system is temporarily or indefinitely locked such that the typical services of a system are non-functional. In this paper, we have designed a DoS attack that switches between locking and unlocking the inverter every 10 seconds. This attack is possible through utilizing the system timer and interrupts to set conditional flags that restrict the availability of circuit components. In addition, we applied a diminutive version of the full system DoS attack limited to just the MPPT functional component. The ensuing ramifications on the system are shown in Section V-B1 and Section V-B2.

2) MPPT Input Attacks: The MPPT algorithm output in the solar microinverter code controls the PV panel output current for maximum power transfer. The manipulation of the inputs to the MPPT function can cause lack of efficiency in the grid without allowing the solar PV to operate in its full capacity. In this scenario, we focus on developing two variations of this attack. In the first attack case study, we utilize the system timer and interrupts to constantly switch between correct MPPT inputs and an array of erroneous values. These numbers are arbitrary inputs constantly switched every few interrupts. The second attack redirects MPPT inputs between correct values and the output values of a continuous sinusoidal wave every few interrupts. The resulting effects on the system are demonstrated in Section V-B3.

D. HPC-Aware Firmware Modification Detection

In this part, we describe our DfS technique to propose custom-built HPCs in order to improve the security of MG inverters. In this paper, the MG inverter utilized is a solar microinverter by Texas Instruments (TI). The inverter consists of a \textit{DIMM100 based controlCARD}, which is part of TI’s \textit{F2803x} series, that controls the inverter development board. The available profiling capabilities are extremely limited for \textit{F28x} architecture. Currently, the only profiling that can be accomplished is the count of clock cycles. This is insufficient to detect malicious firmware modifications since it does not provide any information on the structure of the program being executed. Two different applications, one benign and one malicious, being executed for the same number of clock cycles, will incur no difference in HPC values. This motivates us to design custom-built HPCs as DfS primitives of the MG system. The proposed custom-built HPCs, if integrated to next generation inverter controllers, will aid in improving the security and resilience of MG against cyberattacks. It has been seen that HPCs that count instructions such as loads, stores, arithmetic, and branch values are beneficial in capturing the dynamics of an application \[59\]. Furthermore, the order of these instructions differ depending on the program being executed. With very minimal resources to operate with, we have turned to analyze the process and development of custom-built HPCs for firmware attack detection.

Listing 1: Snippet of firmware assembly code for solar microinverter.

```
        mov al,@VarA ;Load AL with VarA
        dec al ;Decrement AL
        and al,#0xFF ;Logical AND AL with 0xFF
        mov al,@VarB ;Load AL with VarB
```

1) Custom-built HPC Design and Collection: The custom HPCs we propose keep track of the order of specific assembly instructions contained inside the binary executable. These HPCs are designed to include various types of instructions: arithmetic (\(a\)), boolean (\(b\)), store (\(s\)), load (\(l\)), and branch/jump (\(b\)). Our custom-built HPCs not only count the occurrence of each of these instruction types, but also the number of sequences of these instruction types.

Our HPC-based feature vector consists of 30 HPCs: \(a, s, l, b, n, a, a, s, a, a, s, a, a, s, a, a, s, a, a, s, a, a, s, a, a, s, a, a, s, l, l, b, n, b, b, n, n, b, n, b, n, n\). In this representation, \(a, s, l, b, n\) and \(b\) indicate arithmetic, store, load, boolean, and branch instructions, respectively. Therefore, the first five HPCs count the number of times each of these instructions are encountered individually. The remaining HPCs in the feature vector, in the form of \(XY\), count the number of \(X\) instructions that are immediately succeeded by \(Y\) instructions. As an example, HPC \(la\) counts the number of load instructions that are immediately followed by an arithmetic instruction. On the other hand, HPC \(al\) counts the number of arithmetic instructions that are immediately followed by a load instruction. We also propose HPCs like \(bb\), which count the number of times a branch instruction follows another. As an example, Listing 1 shows a sample firmware assembly code for the solar microinverter. In this code segment, HPCs \(la, an, na, and ab\) would all be two, while HPC \(bl\) would be one. Meanwhile, HPCs \(n, a, b, and l\) would be two, four, two, and two, respectively.

The imitation of traditional HPC collection during simulation can be addressed by sampling the designed HPCs in the disassembled firmware assembly code at specific intervals. In this paper, we collect HPC counts every 50 assembly instructions, i.e., our sampling interval is 50. Other collection intervals can also be employed, albeit, with a different number of HPC counts. The process flow graph in Fig. 3 outlines our proposed technique. First, the high-level firmware code is converted into assembly code through a disassembler. Next, we sample instructions from the assembly code periodically until we encounter 50 instructions, i.e., our sampling interval. The values of the HPCs are recorded and the counters are reset to zero. This process is repeated until we exhaust all available assembly instructions. The recorded custom-built HPCs form a dataset, which can be used to train ML models and detect malicious firmware modifications, thereby obtaining a DfS solution against these attacks.

Unlike traditional AVS, our DfS technique is robust against
 attackers that aim to obfuscate a malicious firmware through the insertion of statements at the code level. Any insertion of additional statements will engender the disassembled firmware assembly code to differ. Therefore, in the presence of undesired instructions, the sampling of our custom-built HPCs from this assembly code will result in dissimilar values from the golden HPC trace. As a result, the ML model will be able to classify these camouflaged malicious firmware. The static disassembly code utilized is sufficient for distinguishing between benign and malicious firmware. Furthermore, TI currently provides no tools for attaining dynamic traces for applications on our experimental platform. The proposed DfS technique is applied on a real-world commercial firmware, specifically, TI’s solar microinverter that is controlled by a Piccolo TMS320F28035 Isolated ControlCARD. This DfS method can be utilized in other embedded systems where procurement of the assembly code is possible; albeit, with a difference in custom-built HPCs that can be sampled based on the available assembly instructions. Furthermore, our DfS technique is agnostic of the MG model and device. Our method does not utilize any physical measurements directly from the grid which might be maliciously falsified [69]. The custom-built HPCs are sufficient for securing the solar microinverter because any deviations in performance or operational ranges would be engendered from malicious firmware that would be detected by our proposed defense. In addition, compared to previous work that uses custom-built HPCs [59], our proposed technique utilizes a wider variety of features, e.g., we incorporate boolean instructions. Additionally, prior work was focused on protecting general purpose computers, while our work is primarily concerned with securing commercial real-time power grid devices, i.e., solar microinverters.

V. IMPACT ANALYSIS & DETECTION RESULTS

In this section, we demonstrate the effects of firmware attacks on a MG system. We further demonstrate the efficiency of our proposed custom-built HPC-based methodology in detecting modifications in the microinverter’s firmware code.

A. Microgrid System Model

In order to evaluate the impact of the firmware modification attacks discussed in Section IV-C, we develop a simulation model for the MG system. We utilize Matlab to model the MG components including loads, generators, energy storage systems, etc. Furthermore, we use a discrete time model for the microinverter whose MPPT controller leverages the aforementioned PnO methodology (Algorithm 1). The grid architecture used for the MG simulation is depicted in Fig. 4. The simulation model of the MG includes all the components found in a realistic MG setup: a solar PV with its solar microinverter, a lithium-ion battery energy storage system, a diesel generator, and residential and industrial loads. The MG components are connected via a distribution substation transformer with a capacity of 250 MVA to the utility point of connection operating at 13.8 kV. The distribution voltage feeder level is set to 5 kV and step-down transformers are used to interface the generation assets and the loads. The nameplate generation capacity for the diesel generator is set to 1 MW. The maximum generation capacity for the microinverter can reach 250 kW following the PV insolation profile. As for the energy storage system, it can generate up to 100 kW (capacity of 100 kWh). The loads of the MG include an aggregated residential load with a constant power demand of 250 kW and a variable lumped industrial load whose power demand ranges between 250-750 kW.

B. Attack Impact Analysis

The base case for our MG system is in islanded mode of operation. The islanding (or autonomous) feature of MGs is a fail-safe mechanism employed to protect both the distribution and transmission electric grid system if either one operates abnormally. In such scenario, the MG is responsible to meet the power demand of all the contained loads (e.g., industrial, residential, etc.). The islanding operation of the MG is presented in Fig. 5. Specifically, at $t = 0$ sec, the islanding command is issued, either by the DSO or MG operator, which explains the frequency fluctuation. At $t = 35$ sec, we have a power demand increase (from 500 kW to 800 kW) in the MG – also resulting in frequency fluctuation – as can happen in realistic grid applications. We investigate how the MG operation is impacted under three different attack scenarios with regards to the MG operation depicted in Fig. 5. The three attack scenarios involve: (i) a DoS attack on the MPPT controller, (ii) a DoS attack on the microinverter, and (iii) an input-tampering attack of the MPPT controller affecting the overall power conversion process.

1) DoS Attack on the MPPT Controller: In this type of attack, we modify the microinverter firmware and switch off the

Fig. 3: Proposed HPC collection and utilization flow diagram.

Fig. 4: Structure and specifications of the simulated MG model.
MPPT functionality. As explained in Section IV, MPPT is a feature that has been recently included in inverter architectures as it can boost their power conversion efficiency. By disabling this feature via a DoS-type of attack, malicious adversaries can expect that the generated power enabled by the microinverter will be lower. This is validated by simulation results presented in Fig. 6. If the MPPT functionality of multiple inverters is disabled, thus leading to severely curtailed solar generation, it can result in brownout or load shedding events since the power reserves (e.g., alternative generation sources) might not be able to cover the power deficit. Although this type of attack might not have catastrophic impacts on the MG operation, it can elicit uneconomical power grid operation [70].

2) DoS Attack on the Microinverter: In this case study, we demonstrate a DoS attack in which we disable the output (grid-tied) stage of the microinverter. The outcome of the attack is presented in Fig. 7. As a result of the DoS on the solar microinverter and the unavailability of the solar PV to produce power, the ancillary generation sources are required to meet power demands. In our experiment, a DoS attack disables the microinverter at $t = 15\text{ sec}$. The inverter gets back online to operate at $t = 30\text{ sec}$ immediately before the load increases (at $t = 35\text{ sec}$), as per the base case scenario (Fig. 5). Then, the microinverter gets connected to the MG until $t = 45\text{ sec}$ when a DoS attack switches it off again. In this case study, the MG operation is severely impacted due to the frequency fluctuation. Specifically, the malicious control of the inverter in conjunction with the generator switching, which is operated complementarily to meet the MG’s power demand, cause frequency instabilities and adversely effect the grid’s power quality [71]. The impact could vary from damaged equipment, load shedding, brownouts, and even total loss of power (blackout) in case this attack occurs during a peak-load period when the alternative generation sources cannot balance the power demand. This is evident by the widespread power outage across the U.K. in 2019 [72].

3) Input Tampering Attack on the MPPT Controller: As discussed in Section IV-B, the real-time voltage and current measurements of the solar PV module are critical for the efficient operation of the microinverter. The measurements are used by the MPPT in an effort to reach the optimal condition and extract as much power as possible from the PVs under the varying environmental conditions. Thus, by strategically and stealthily tampering the $V_{\text{rt}}$ and $I_{\text{rt}}$ sensed values, attackers can destabilize the MPPT controller and consequently the microinverter power generation [71]. The severity of this attack scenario is illustrated in Fig. 8 and Fig. 9 where two error signals with different frequencies are superimposed over the sensor measurements. In both cases, the applied signal perturbations are constantly moving the operation point (around
C. Attacks Detection Capability

The prompt detection of malware in grid assets’ firmware code is of paramount importance in preventing any of the previously discussed adverse scenarios. In this section, we present the efficacy of our hardware-assisted methodology utilizing HPCs in detecting malicious firmware modifications. The detection accuracy of the proposed approach renders it a viable proposition for real-world power grid applications.

1) Implementation Setup: To demonstrate the effectiveness of our approach, we test our technique with a real-world commercial firmware of an embedded microinverter system [74]. Specifically, the TI solar microinverter supports a F2803x microcontroller, which we utilized for our testing and evaluation phase. We employ our custom-built HPCs in order to detect the firmware modifications within the microinverter’s code. Four firmware modifications are realized into the solar microinverter code according to the attack scenarios simulated in Section V-B, i.e., a DoS targeted attack on the MPPT functionality, a DoS attack on the whole microinverter system, and two MPPT input manipulation attacks. The attacks are flashed into the Piccolo TMS320F28035 Isolated ControlCARD using a DIMM100 Docking Station Baseboard supporting power and JTAG capabilities. To generate the HPC-based signatures, a Python script is utilized to count the number of custom HPCs in the disassembled firmware executable. The TI dis2000 dissembler is used to get the assembly code from the binary executable. Since HPCs are counted in intervals, our script collects the total value for each proposed HPC every 50 assembly instructions. We utilized this sampling rate as it is large enough to capture information about the structure of the program but small enough to furnish an adequate amount of samples. We utilized a 70:30 split where we trained on 70% of the dataset with the remaining 30% used for testing. We aggregate samples from all the attacks and the base code. With the attained simulated custom HPCs, we build three ML classifiers generated using the scikit learn library [75], a DT, a NN and a RF, as mentioned in Section II-C2

2) Detecting Firmware Modifications with ML Models: In order to detect the simulated attacks on the MG model, we use all the 30 custom-built HPCs to construct the ML classifiers as shown in Fig. [10]. It is observed that each model is capable of identifying the firmware modifications with high precision. The best measurement metrics are attained with the RF classifier, which provides an accuracy of 76.4%, precision of 95.1%, and recall of 79.53%. The accuracy and recall for all models is partially diminished because the training dataset has only one benign base version of the solar microinverter code and four malicious firmware variations.

3) PCA Feature Selection in ML Models: Since most modern processors are only capable of tracking a couple of HPCs at a time, we used PCA, as described in Section II-C2, to determine the top best features: boolean, arithmetic and branch instructions (n, a, and b). These features are robust for malicious firmware detection as they can adequately capture many of the malignant tendencies found in pernicious firmware. Compromised firmware will attempt to deviate from the normal control flow of the system which increments branch instructions and engenders malicious activity such as manipulating outputs or internal system functions which increments boolean and arithmetic instructions. Moreover, reducing the number of custom-built HPCs aid in decreasing the hardware overhead of the DIS architecture. These three dominant features are used to train a new set of models as shown in Fig. [11]. Experiments show that the performance metrics for each classifier are bolstered on application of PCA. The DT and RF classifiers have peak accuracy of 75.84% and 79.21%, respectively, and peak precision of 89.51% and 95.8%, respectively. The NN classifier furnishes the best results since the accuracy improves from 75.28% to
TABLE I: Overhead of individual classifiers.

| Design          | lsi_10k Library | saed_90nm Library |
|-----------------|-----------------|-------------------|
| Decision Tree   | Area Overhead   | 2108 sq. units    | 8930.814878 sq. units |
|                 | Power Overhead  | 44.8547 µW        | 478.9462 µW |
| Neural Network  | Area Overhead   | 37062 sq. units   | 153799.401513 sq. units |
|                 | Power Overhead  | 343.7231 µW       | 5429.1 µW |
| Random Forest   | Area Overhead   | 2618 sq. units    | 11004.428258 sq. units |
|                 | Power Overhead  | 47.7563 µW        | 529.3894 µW |

80.33% and the precision improves from 93.7% to 100%. While all models could detect the firmware attacks, the NN is able to detect, with high accuracy and precision, all the malicious firmware samples. This demonstrates the benefit of PCA feature selection utilized in our models. When utilizing 30 HPCs, the model becomes overfitted, but applying PCA engendered us to attain the optimal set of HPCs required to construct an effective model. Only three custom HPCs are sufficient to provide a robust defense against malicious firmware modifications, thus significantly reducing the DfS hardware overhead. We realized the ML classifiers in Fig. 11 in hardware to establish their area and power overhead. We designed the RTL for the DT, NN, and RF and synthesized them through the Synopsys Design Compiler logic synthesis tool. We have employed two digital standard cell libraries, saed_90nm and lsi_10k. Our results related to the power and area overhead acquired from our synthesis of the RTL are presented in Table I.

4) Instruction Elimination Analysis: In this experiment, we train ML models on datasets in which any one of the five instructions, i.e., a, s, l, n, and b, are excluded at a time. As an example, BLAN represents the scenario in which only branch, load, arithmetic and boolean instructions are included. As a result, HPCs like sa and sb are not considered in BLAN. Fig. 12 shows the performance comparison for the ML classifiers on all possible omission combinations. The best results are furnished by the NN classifier trained on the BLAN dataset. The performance metrics of 79.2% accuracy and 98.6% precision are the highest throughout all the models trained. This is significant because the experiments presented in Section V-C3 have shown that boolean, arithmetic and branch instructions are by far the most dominant.

In order to further prove the strength of n, a, and b instructions, we trained a final set of models on datasets in which two of the five instructions are excluded. That is, BAN indicates a dataset in which store and load instructions are omitted. Fig. 13 shows the classification performance attained from all possible instruction datasets. The NN trained on the BAN dataset has the highest precision of 99.3%, which further supports our previous results. Therefore, HPC support for only boolean, arithmetic, and branch instructions can assist in providing better DfS for embedded microinverter controllers.

VI. CONCLUSION

In this paper, we demonstrate the impact of firmware modification attacks on a solar microinverter operating in a MG setup. We propose the detection of such stealthy attacks by leveraging custom-built HPCs as DfS and periodically sampling the instructions within the inverter’s firmware. Our proof-of-concept work validates that devices without native HPC support can be hardened against adversaries leveraging DfS primitives. Specifically, we improve the security of TI’s F2803x microcontroller leveraging custom-built HPCs. Our experiments demonstrate that ML models trained on our HPCs identify firmware attacks with high accuracy and precision. Apart from providing an approach to secure solar microinverters without HPC support, we demonstrate the potential impact of compromised devices in MG deployments operating autonomously.

In the future, we will include custom-built HPC extensions for other firmware-controlled grid assets and formalize our detection methodology for additional firmware attacks (e.g., rootkits, command injection, etc.). We plan to evaluate our framework utilizing hardware-in-the-loop experiments including grid-tied inverters and MG components, refine and improve educational and laboratory tutorials [70], and demonstrate the impact of these attacks in real-time operation.
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