A Single Phase 7-Level Cascade Inverter Topology with Reduced Number of Switches on Resistive Load by Using PWM

H. H. Hamzah¹, A. Ponniran¹, A. N. Kasiran¹, M. A. Harimon¹, D. A. Gendum¹, M. H. Yatim¹,
¹Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, 86400, Parit Raja, Johor, Malaysia.

Abstract. This paper discussing design principles of inverter structure with reduced number of semiconductor devices of seven levels symmetric H-bridge multilevel inverter (MLI) topology. The aim of this paper is to design an inverter circuit with reduction of semiconductor losses, converter size and development cost. The H-bridge and auxiliary structures were considered in order to achieve seven levels output voltage. The performance of design circuit is compared with conventional seven levels structure in terms of voltage output. The circuit development consists of seven switches and three diode. A basic modulation technique is used to confirm the designed circuit. The results show that the designed circuit is able to convert seven level output voltage with low total harmonics distortion (THD) in voltage fundamental output. According to the results, fundamental output voltage is increased up to 8.314%, and the THD is decreased up to 0.81% compared to the conventional seven level inverter.

1. Introduction

Multilevel inverters offer different kind of applications in power electronics field, extending of voltage rate from medium to high, for example, in sustainable sources, modern drives, aviation, broadcasting and transportation. By increasing the output voltage level, it reduces the voltage gap between level, thus it will withstand better voltage, fewer harmonics, high electromagnetic compatibility, reduced switching loss, and better power quality [1]. Cascaded type inverter was designed in the early development of multilevel inverter. Afterward, neutral point clamped MLI were produced and followed by flying capacitor MLI. These three topologies used as instruments to deliver the require output voltage in the required field. The topology presented to begin with, that is, the cascaded MLI, is essentially simple series of connection of H-bridge inverter circuit. In brief, diode-clamped MLI uses an arrangement of capacitor banks, while in flying capacitor MLI, a “float-capacitors” are applied as a part of clamping the produced voltage [1]. Basic H-Bridge inverters requires isolated transformers, then H-bridge cascaded MLI was designed with several isolate DC input sources. Besides, the structure do not requires either diode-clamped or capacitor-clamped. Less parts are utilized in cascaded MLI contrasted with diode-clipped and flying capacitor MLIs [1], [2]. Thus the cascaded MLI arrangement is become popular. At the same time, the evolution of cascaded MLIs structures are concerned. By referring at previous research at [3], a 7-level MLI works with 9 switches, lessening 3 switches from the conventional structure of cascaded MLI [4]. It offers great outcomes by producing desired 7-level output waveform with low THD. Subsequently, a 7 level MLI with 8 switches throwing out 2 more switchers is introduced [5]. Conventionally, in order to achieve further reduction of switches,
researchers develop a topology of 7-level MLI with 4 dc sources and 6 switches in order to achieve 7-level output voltage [5]. However, by using 3 dc sources, 7-level output voltage can be achieved as well, thus the THD is low, and less gate driver circuits are used to drive the switches. Pulse width modulation (PWM) technique is utilized in order to realize the multilevel output voltages achievement. Several numbers of modulation strategy can be utilized as a part of this outline MLIs such as sinusoidal pulse width modulation (SPWM) that consists of phase opposition disposition (POD), phase disposition (PD) [1] and alternate phase opposition disposition (APOD), where every carrier is phase shifted by from its adjacent bearer. Moreover, copious of modulation technique and control paradigm have been produced for different levels of pulse width modulation converters other than SPWM, i.e., selected harmonic elimination (SHE-PWM) and space vector modulation (SVPWM).

2. Conventional cascaded multilevel inverter (MLI)

Every single cell H-bridge produces three different voltage levels, +Vdc, 0, -Vdc associating with the DC sources to the AC output voltage by various combinations of four switches, Q1, Q2, Q3, and Q4 as shown in Figure 1. The cascaded H-bridge multilevel inverter (CHBMLI) as shown in Figure 1 uses three DC sources and it produces seven levels of output voltage.

![Figure 1. Structure of seven levels Conventional Cascaded H-Bridge Multilevel Inverter (CHBMLI).](image)

To acquire +Vdc, switches Q1 and Q4 are turned on in each cell, while -Vdc level is generated by turning on the Q2 and Q3. By considering n as the quantity of cell connected in series connection, m will be the quantity of output levels in each phase, (1). The exchanging of switching scheme of a CHBMLI can be resolved by utilizing (2) [4], [5].

\[ m = 2n + 1 \]  
\[ s_w = 3m \]  

(1)  
(2)

By considering appropriate techniques in modulation and circuit operation, stepped waveforms of the output voltage will be generated. The generated waveforms will be close to sinusoidal waveform as the number of level increases. The output of AC voltage is given by equation (3).

\[ V_o = V_1 + V_2 + V_3 \]  

(3)

Previously it stated that the increasing number of output level will leads to an increasing number of switches. Consequently causes the switch control become complex. In this paper the designed circuit
is analysed according to the content of total harmonic distortion (THD) generated and the fundamental output voltage produced by using FFT analysis. Comparison is made with others number of level by using PWM as modulation technique.

2.1. Design of multilevel inverter structure

Conventionally, seven levels output voltage topology of inverter structure requires 12 switches and three DC sources. With the improvement of structure, the switches are reduced to almost half, seven switches as shown in Figure 2. Consequently construction costs will be reduced as well. Figure 2 demonstrates the designed circuit that comprise seven switches and three DC sources. This approach still uses same switch control technique as conventional cascaded MLI.

![Figure 2. Structure of Seven Levels Cascaded H-Bridge Multilevel Inverter (CMLI).](image)

3. General description

The evolutions of cascaded topology inverter are making the operation more convenient and still produce seven levels output of the designed converter. The designed circuit consists of three DC sources with equal of voltage supply rating. Switches Q1, Q2, Q3 and M4 are the H-bridge cell in the designed MLI and switches M5, M6 and M7 are functioning as controller for the input voltage to generate seven levels of the stepped output voltage. The purpose of diodes D1, D2 and D3 to ensure unidirectional operation for some period of time.

4. Mode operation

4.1. Powering mode

During this mode, Figures 3, both load current and voltages have the same polarity. In the positive half cycle, the output voltage is +Vdc, D2, Q6, Q1 and Q4 are forward biased. Then, when the output voltage is +2Vdc, D3, Q5, Q1 and Q4 are forward biased. While, when the output voltage is +3Vdc, D1, Q7, Q1 and Q4 are forward biased. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

4.2. Free-wheeling mode

This modes exist when one of the main switches is turned-off while the load current needs to continue flow due to the inductance load. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle, Q1 and Q2D or Q4 and Q3D will be forward biased. While in the negative half cycle, Q3 and Q4D or Q2 and Q1D will be forward biased.
5. Experimental results

5.1. Switching scheme

Figure 4 shows the PWM switching scheme for the designed CMLI and gate driver signals on switchers. In order to generate seven levels of the output voltage, a appropriate PWM switching scheme are designed accordingly with dead time consideration. The switchers are separated into two group, i.e., in the H-bridge cell (Q1-Q2-Q3-Q4) and the other three switches (Q5-Q6-Q7) act as controller in order generate seven levels of the output voltage.

(a) Experimental waveforms of PWM for designed CMLI, frequency = 50 Hz, Duty Cycle = 25%-75%
(b) Experimental waveforms of gate drive signals on MOSFET (IRF840)

Figure 4. Experimental results.
5.2. Output voltage waveform

The specifications of the experiment condition are as follows: three-level PWM inverter (Q1-Q2-Q3-Q4), the duty ratio is 0.375, the output voltage is 90 V, the switching frequency is 50 Hz and the output power is 7 W. In this paper, the operations of 3-level and design 7-level CMLI with reduced switchers are evaluated separately by using FFT analysis. The designed prototype circuits are connected with 1300 Ω resistive load. The maximum fundamental voltage output of the 3-level and design 7-level CMLI prototypes are 105.9 V and 76.16 V respectively at the output power of 7 W. Figure 5(a) shows the output voltage of three level PWM inverter. The input voltage is 90 V and the peak-to-peak output voltage is 86.5 V. The existence of anti-parallel diode on the power MOSFET caused voltage spike distortion when the inverter is not connected with any loads as shown in Figure 5(b).

![Output Voltage Waveform](image)

(a) With anti-parallel diode and 1300 Ω resistive load (without filter)  
(b) With anti-parallel diode and no load (without filter)

**Figure 5.** Output voltage waveform of three level PWM inverter by using MOSFET.

Figures 6(a) and 6(b) show the simulation and experimental results of the seven levels designed seven levels inverter, respectively. The duty cycle is between 25% to 75% and the dead-time is 1% from the switching period. Fundamental output frequency is 50 Hz and seven voltage levels are distributed into (+90 V), (+60 V), (+30 V), (0 V), (-30 V), (-60 V) and (-90 V). From the results, a good agreement is shown between experimental and simulation results.

![Output Voltage Waveform](image)

(a) Simulation result  
(b) Experimental result

**Figure 6.** Output voltage waveform of the designed seven levels inverter with 1300 Ω resistive load.

From the results, percentage of total harmonic distortion (THD) is also determined. Expression (4) is used to estimate the THD in the output voltage voltage based on harmonic components. Figure 7 shows the THD and harmonic components in the conventional and designed MLI. Meanwhile Table 1 shows the THD and fundamental voltage of multilevel inverter using PWM modulation technique.
when resistive load is 1300 Ω and frequency is 50 Hz. The total harmonics distortion slightly low and the fundamental output is increase in the designed converter. According to the results, fundamental output voltage is increased up to 8.314%, and the THD is decreased up to 0.81% as compared to the conventional seven level inverter as shown in Table 1.

\[
THD = \left( \frac{\sum_{n=2}^{50} V_n^2}{V_1} \right)^{1/2}
\]

(4)

![Figure 7. THD and harmonic components (1300 Ω resistive load).](image)

(a) Conventional structure  
(b) Designed structure

| Number of level | Fundamental output voltage | THD of Voltage Output (%) |
|-----------------|-----------------------------|---------------------------|
| 2-level         | 114                         | 38.73                     |
| 3-level         | 105.9                       | 28.99                     |
| 7-level         | 72.16                       | 27.55                     |
| 7-level design  | 78.16                       | 22.55                     |
| 9-level         | 82.14                       | 17.45                     |

6. Conclusion
In this paper, the authors have discussed the design principles of inverter structure with reduced number of semiconductor devices of seven levels symmetric H-bridge multilevel inverter (MLI) topology. The designed seven levels inverter with reduced switching devices operation is experimentally confirmed by the experimental results. Besides, from the designed structure, total harmonics distortion (THD) is slightly reduced as compared to the conventional structure. According to the results, fundamental output voltage is increased up to 8.314%, and the THD percentage of the designed converter is decreased up to 0.81% as compared to the conventional seven level inverter. In a future work, applications related to this study will be performed such as for induction motor drive system in closed loop control system.

Acknowledgment
The authors would like to express their deepest appreciation to the Ministry of Higher Education and Universiti Tun Hussein Onn Malaysia for supporting this research under Research and Innovation Fund. Many thank are due to all research members for their tremendous work and cooperation.
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