Deep sub-micron stud-via technology of superconductor VLSI circuits

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Abstract

A fabrication process has been developed for fully planarized Nb-based superconducting interlayer connections (vias) with minimum size down to 250 nm for superconductor very large scale integrated (VLSI) circuits with 8 and 10 superconducting layers on 200-mm wafers. Instead of etched contact holes in the interlayer dielectric it employs etched and planarized Nb pillars (studs) as connectors between adjacent wiring layers. Detailed results are presented for one version of the process that utilizes Nb/Al/Nb trilayers for each wiring layer instead of single Nb wiring layers. Nb studs are etched in the top layer of the trilayer to provide vertical connections between the wires etched in the bottom layer of the trilayer and the next wiring layer that is also deposited as a Nb/Al/Nb trilayer. This technology makes possible a dramatic increase in the density of superconducting digital circuits by reducing the area of interconnects with respect to presently utilized etched contact holes between superconducting layers and by enabling the use of stacked vias. Results on the fabrication and size dependence of electric properties of Nb studs with dimensions near the resolution limit of 248-nm photolithography are presented in the normal and superconducting states. Superconducting critical current density in the fabricated stud-vias is about 0.3 A µm$^{-2}$ and approaches the depairing current density of Nb films.

Keywords: superconductor integrated circuits, Josephson junctions, single flux quantum circuits, Nb/Al–AlO$_x$/Nb tunnel junctions, Nb films, superconducting critical current

1. Introduction

In order to realize the tremendous advantages of superconducting digital integrated circuits over semiconductor circuits in speed and reduction of energy dissipation [1], their integration scale must be increased from its current medium level to very large scale integration (VLSI) levels and beyond. This requires increasing the density of elemental switching devices—Josephson junctions (JJ)—by several orders of magnitude, from the present density of $\sim 10^4$–$10^5$ JJ$s$ cm$^{-2}$ to $10^6$–$10^7$ JJ$s$ cm$^{-2}$, with a corresponding increase in the density of interconnects (Josephson transmission and passive transmission lines) and other passive components (inductors, resistors, vias). These goals can be achieved by scaling down the dimensions of all circuit elements and increasing the number of superconducting metal layers available for circuit integration, a path familiar from the development of semiconductor VLSI and ULSI circuits. Currently, the most advanced fabrication process for Nb-based superconducting circuits utilizes up to ten superconducting metal (Nb) layers, chemical–mechanical polishing (CMP) for planarization of dielectric and Nb layers below the junction layer, minimum JJ size of 1 µm, minimum linewidth $\sim 0.5$-µm, and reaches JJ density $\sim 10^5$ JJ$s$ per chip [2].

Increasing the density of Josephson junctions and the number of superconducting layers leads to an even larger increase in the number and density of vias between metal layers. Although scaling down the dimensions of Josephson
junctons, inducors, and resistors is more or less straightforward by implementing modern deep-UV photolithography and etch tools, the reduction of the sizes of vias between superconducting layers is not. In all existing and reported fabrication processes [2–11], superconducting vias are made by etching contact holes in the inter-metal dielectric and depositing the next Nb layer by physical vapor deposition (PVD), usually by dc magnetron sputtering, as shown schematically in figure 1. This limits the minimum size of contact holes to \( \sim 0.5 \, \mu\text{m} \), as it becomes difficult to achieve reliable contacts with sufficient superconducting critical currents in smaller holes, because increasing their aspect ratio leads to poor step coverage and formation of voids (keyholes). Sloping the contact walls by the usual methods to improve step coverage becomes more difficult with the transition to deep-UV lithography which favors near-vertical photore sist profiles.

In practice, the contact hole also needs to be well surrounded by metal overlay to allow for photolithography misalignment (e.g., overlay mean plus three sigma) and etch bias. In the typical design rules, this surround is also \( \sim 0.5 \, \mu\text{m} \), making the typical smallest via size around 1 \( \mu\text{m} \). This size further increases when many vias need to be stacked on top of each other to make low-inductance connections between bottom and top layers in a 10-metal layer circuit. As a result, vias became one of the largest components in superconducting digital circuits, occupying up to 30% of the circuit area because the number of vias is much larger than the number of Josephson junctions. Clearly, increasing the integration scale of superconducting circuits requires scaling down the size of vias without compromising their reliability or lowering their critical currents.

In the semiconductor industry, a similar problem with contact holes was solved long ago by developing tungsten plugs between wiring layers [12, 13], a process that replaced contact holes in an interlayer dielectric by cylindrical Nb studs (with nearly vertical walls) from Nb film in contact with the bottom wiring layer \( M_i \). Then, an interlayer dielectric could be deposited and planarized using CMP to provide access to the top of the stud. After the structure would look exactly as shown in the left bottom picture in figure 2. Then the top wiring layer deposition would follow. There are two possible practical realizations of such a process. The first version, shown in figure 3, is referred to as a single etch and planarization (SEAP) process.

Here, the bottom Nb wiring layer \( M_i \) is first deposited and patterned, figure 3(a). This layer is then planarized by depositing a thick layer of SiO\(_2\) (figure 3(b)) with subsequent CMP to reach the structure shown in figure 3(c). After this, Nb deposition for subsequent studs follows, figure 3(d). Since etching of Nb studs needs to be stopped on the bottom Nb wiring, it is useful to have a good etch-stop (ES) layer—a material with a lower etch rate than Nb. This ES layer must not degrade the superconducting properties of the interface in order to maintain high critical current in the superconducting
Figure 3. Cross sections of the SEAP version of a stud-via process for superconducting circuits: (a) deposition and patterning of (Nb) wiring layer $M_i$ over the wafer; (b) deposition of a blanket SiO$_2$ layer for CMP planarization; (c) CMP of the SiO$_2$ layer; (d) deposition of an etch-stop layer (ES) and Nb stud metal bi-layer; (e) patterning of Nb studs and ES layer; (f) blanket SiO$_2$ deposition for CMP planarization; (g) CMP of SiO$_2$ to access the top of Nb studs; (h) deposition and patterning of the next Nb wiring layer, $M_i+1$. Prior to step (a) the wafer may already contain several patterned and planarized layers. A convenient etch-stop layer is Al. The bi-layer deposition should be done in situ to minimize contamination of the interface between Al and Nb stud.

state. There are very few materials suitable for this, and a thin layer of aluminum (a few nanometers thick) is one of them. After etching the studs, figure 3(e), the process flow repeats planarization steps (b) and (c) to planarize studs and open access to their top surface, figure 3(g). Finally, the top Nb wiring layer is deposited and patterned to complete the via-stud interconnects between a pair of Nb layers $M_i$ and $M_i+1$.

The process can further be repeated for the next pair of wiring layers $M_i+1$ and $M_i+2$ and so on in a straightforward manner. It also allows for stacking studs on top of each other. The drawback of this processing scheme is the need for two planarization steps to form each stud-via interconnect: one for the bottom wire and another one for the etched stud.

The process can be simplified by noticing that the structure formed after stud etching, figure 3(e), resembles the standard trilayer-type SNS Josephson junction where the base electrode is bottom wiring layer $M_i$, the counter (top) electrode is the stud, and the Al etch-stop layer is N-layer or Al-AlO$_x$ barrier layer in tunnel junction trilayers [14] without oxidation. Therefore, the stud-via formation can be done in the same manner as the formation of Josephson tunnel junctions in a whole-wafer trilayer process [14] with the addition of planarization [15–17]. This second version of the stud-via process, shown in figure 4, is referred to as a dual-etch and planarization (DEAP) process.

Instead of depositing a single wiring layer as in the previous (SEAP) version, in this process each wiring layer is deposited in situ as a Nb/Al/Nb trilayer, figure 4(a). The top layer of the trilayer is then patterned by photolithography and dry etching to form Nb studs as shown in figure 4(b). Aluminum serves as an excellent etch-stop layer for etching Nb in F-based chemistries. Then, the bottom electrode of the trilayer is patterned in Cl-based chemistry to etch through the Al layer and form the wiring pattern $M_i$. Etching is followed by blanket SiO$_2$ deposition and CMP to access the tops of the Nb studs, figure 3(e). Then, the next layer $M_i+1$ is deposited as a Nb/Al/Nb trilayer and patterned in the same manner to form the next layer of interconnects, and so on. If no more stud-vias are required above, a single metal wiring layer can be deposited. The described processing unit needs to be repeated as many times as there are wiring layers in the full process. The only disadvantage of the DEAP process with respect to the SEAP version described earlier is the need to planarize by dielectric CMP twice higher steps in the etched metals (stud plus bottom wire).

Our near-term goal is the development of a 10-metal layer process for superconducting VLSI circuits on 200-mm wafers with deep sub-micron features with the described stacked stud-vias. The cross-section of this target process is shown in figure 5. The target current critical density of this process is 100 $\mu$A $\mu$m$^{-2}$ (10 kA cm$^{-2}$), the minimum JJ size is 0.5 $\mu$m, the wiring pitch (line + space) is 0.5 $\mu$m, and the minimum diameter of Nb stud-vias is 0.3 $\mu$m. As a step towards this goal, in the next section we will describe the results of stud-via fabrication by the DEAP version of the process (trilayer based, figure 4).

3. Stud-via fabrication

Nb/Al/Nb trilayers were deposited over 200-mm Si wafers with 500 nm of thermal oxide. The target thickness of the top
Figure 4. Cross sections of Nb/Al/Nb trilayer-based (DEAP) stud-via process: (a) Nb/Al/Nb in situ trilayer deposition; (b) patterning of the top electrode to etch Nb studs; (c) patterning of the bottom electrode to form wiring layer $M_1$; (d) blanket SiO$_2$ deposition for planarization by CMP; (e) CMP down to the tops of Nb studs; (f) Nb/Al/Nb wiring layer deposition to form wiring layer $M_{i+1}$ and Nb stud to contact next layer $M_{i+2}$. If no additional stud-vias are required above, a single Nb wiring layer $M_{i+1}$ can be deposited instead. This process is to be repeated as many times as there are wiring layers in the entire process.

Figure 5. Cross-section of the target process with ten planarized metal layers and stud-vias for superconducting VLSI circuits. Conventional etched vias are only used to connect to the Nb bottom electrode of the JJs. Making stud-vias for this layer would be too complicated, because the counter-electrodes of the JJs are already Nb studs connecting to the upper wiring layer.

Nb layer (Nb studs) was 250 nm, and of the bottom layer and the wiring layer was 200 nm. The thickness of the Al etch-stop layer was 200 nm.

3.1. Photolithography

The photolithography was performed using a positive deep-UV photoresist, bottom antireflection coating, Canon FPA-3000 EX4 248 nm stepper with $5 \times$ reduction and 250 nm nominal resolution. The circular shape for stud definition was implemented with diameters covering the range from 200 nm to 15 $\mu$m. Clear field masks were used without implementing any resolution enhancement techniques. The average diameter of the developed photoresist features on wafers was measured using a Hitachi CD SEM, and the typical SEM images are shown in figure 6. The wafers were exposed using a $7 \times 7$ grid with 22-mm die size, each die containing 16 test chips. Die locations are referred to as c#r# indicating the column and row numbers of this grid, respectively.

Stud photolithography is identical to photolithography of JJs and contact holes (the latter would differ only by the use of dark field masks). We studied carefully the size dependence of the obtained features on wafers, $d_w$, on the size of the design features $d$ (on the reticles the design size is $5d$ to account for $5 \times$ reduction of the stepper optics) because these results are applicable to the definition of circular JJs, contact holes, and other features with sizes near the optical resolution limit. The obtained dependences are shown in figure 7.

We have found that the size of the obtained photoresist image of the opaque disc shapes on the mask can be well described by the relationship

$$d_w = k(d^2 - d_c^2)^{1/2} - b, \quad d > d_c$$

and $d_w = 0$ for $d \leq d_c$, where $d_c$ is a photolithography cut-off size that depends on the exposure dose, focus, and other lithography parameters, and $b$ is the process bias that can be positive or negative depending on the process conditions. Parameter $k$ is the scaling factor characterizing the accuracy of the projection optics reduction coefficient and SEM magnification, ideally $k = 1$. Based on multiple measurements on many wafers, we have found that for the stable and optimized process $d_c$ is always about 250 nm, about the nominal resolution limit of the stepper set by the light diffraction, $k = 1 \pm 0.7\%$, and $b \approx 0$. Far from the resolution cut-off, the relationship between $d_w$ and $d$ is perfectly linear over a very wide range of diameters. Relationship (1) has some implications for the design and fabrication of JJs and other small objects in circuits. It is usually assumed that the size of the projected objects is given simply by $d_w = d - b$. For circular objects this leads to the concept of a ‘missing’ diameter (radius). It is often used in the description of the size dependence of such parameters as JJ critical currents and normal state conductance that are proportional to the actual area, e.g., $I_c = j_c(\pi/4)(d - b)^2$ [18, 19], where $j_c$ is the critical current density. Our measurements indicate that this concept is not adequate for the description of...
Figure 6. SEM images of the photoresist mask and etched Nb features: (a) tilted view of 400-nm photoresist posts masking the Nb/Al/Nb trilayer used for stud-via definition; (b) top view of a photoresist post with design diameter of 250 nm, showing the automated CD measurement of the mean diameter using 48 points around the feature perimeter and giving 113.9 nm (right upper corner); (c) tilted view of Nb studs obtained after etching the top electrode of the Nb/Al/Nb trilayer.

Figure 7. The mean diameter of features used for defining Nb stud-vias as a function of design diameter: (a) diameter of photoresist posts and the bottom diameter of the etched Nb studs in the center (c4r4) of wafer 1; (b) diameter of etched studs on wafer 2 in the wide range design diameters; (c) diameter of etched Nb studs, zoom in on the range of sizes relevant for via-stud definition (≤600 nm) on two wafers (central die marked c4r4 and left upper die marked c1r6). Solid lines are fits to equation (1), showing the lithography cut-off of about 250 nm and a small negative process bias (the obtained features are larger than the designed).

small features, especially near the resolution limit. At \( b = 0 \), equation (1) rather supports the concept of a ‘missing’ area, also often used in circuit design, \( A_w = A_d - A_c \), where \( A_w \) is the object’s area on the wafer, \( A_d \) — the design area, and \( A_c \) — a cut-off (‘missing’) area. The origin of the lithography cut-off is the diffraction of light. Decreasing the diameter of an opaque disc leads to a blurring of its image on the photoresist and increases the light intensity in the area of the geometrical shade. At a fixed exposure dose, \( d_c \) corresponds to the size at which the diffracted intensity produces the critical exposure of the photoresist in the shade area when it will be completely developed off. Therefore, if a printing of discs with the same diameter or in the narrow range of diameters is only required, the average exposure dose can be optimized to reduce \( d_c \) and allow for resolving the smaller objects, although changing the linearity of relationship between \( d_w \) and \( d \) at other sizes. On the other hand, if printing a range of sizes near the resolution limit is required, a proper biasing of the features on the reticle needs to be done according to equation (1) to produce a linear scaling on the wafer.
3.2. Etching

Nb etching was performed using the high density plasma etching chamber of an Applied Materials Centura system with end-point detection, stopping on the Al etch-stop layer. After stripping the photoresist, the diameter of the Nb studs at their bottom, \( d_{\text{bottom}} \), was measured. The results are shown in figure 7. As can be seen, after etching the bottom diameter of the studs follows the same dependence on the design (drawn) diameter (equation (1)) as the photoresist mask. Only the process bias \( b \) becomes slightly more negative (by about 85 nm) after etching, showing that the features after etching are slightly larger than the photoresist mask. The total process bias is thus the same for all drawn diameters, \( b = b_{\text{photo}} + b_{\text{etch}} \), and is about \(-100 \) nm, see figures 7(a)–(c). The diameter of studs at their tops was measured to be less than at the bottom by between 50 and 70 nm. This gives the side wall angle in the range from \( 80^\circ \) to \( 84^\circ \). Therefore, in the following discussion we will consider cylindrical studs with a diameter equal to the mean of the bottom and top diameters, \( d_{\text{av}} \approx d_{\text{bottom}} - 35 \) (nm). Hence, the effective diameter \( d_{\text{av}} \) is given by the same equation (1) with a modified total process bias (about \(-80 \) nm for studs in figure 7(a), and about \(-50 \) nm for studs in figures 7(b) and (c)).

Next, the photolithography and etching of the bottom electrode was performed to define the bottom wiring layer. We used a few different design rules for the surround, \( s \), of studs by the bottom and top Nb wires (see below). The minimum surround used was 100 nm, close to the typical overlay accuracy (mean + three sigma) of our photolithography tool. For simplicity we used the same set of reticles that we normally use for the fabrication of Josephson junctions. Therefore the surround and via placement were not specially optimized to achieve the minimum possible stud-via area. This is planned to be done in the future.

Etching of the bottom wire was performed in a Cl-based chemistry to break through the Al etch-stop layer first. SEM images of the obtained structures are shown in figure 8. After stripping the photoresist, a SiO\(_2\) film was deposited using plasma-enhanced chemical vapor deposition (PECVD) from a SiH\(_4\)/N\(_2\)/O/Ar mixture for subsequent planarization by CMP. The thickness of the film was about twice the thickness of the Nb/Al/Nb trilayer. CMP was undertaken using an Applied Materials Mirra polisher to planarize and remove oxide up to the level of the tops of the Nb studs, figure 4(c). The thickness of the remaining oxide was controlled by an ellipsometer.

Finally, the top wiring layer of Nb was deposited and patterned similarly to the bottom wiring and with the same overlap. The bottom and top wiring layers connected each stud to a cross-bridge Kelvin resistor (CBKR) geometry for four-point measurements of room temperature resistance and critical current at LHe temperature. The SEM picture of the completed structure is shown in figure 9. Here one can clearly see the L-shape of the top Nb wire and a blurry image of the L-shape of the bottom wire which is seen through the 250 nm interlayer dielectric. The outline of the 350 nm stud can also be seen as it slightly protrudes up after polishing, creating a barely visible image in the top wire.

4. Electrical test results and discussion

4.1. Resistance in the normal state

Electric measurements of the Kelvin resistance of studs \( R_K = (V_+ - V_-)/I \), where \( I \) is the applied current as shown in figure 9, were performed using a semi-automated wafer prober. Because of a very large number of test structures we fully probed a limited set of nine dies out of 49 across the 200-mm wafers. The measurements indicated good uniformity of the fabricated studs across the wafers. The typical results are presented in figure 10.

Since we are interested in the scaling of the stud conductance with area, in figure 10 we plotted \( R_K \) versus the design diameter of the studs. In the simplest (ideal) case (when all parasitics can be neglected) the measured CBKR resistance is the resistance of the stud given by

\[
R_{st} = 4R_s I^2/(\pi d_{av}^2),
\]

(2)
Figure 9. (a) SEM image of the completed CBKR structure with 350 nm stud between two L-shaped wires. Clearly visible is the top Nb wire, the lighter blurry image is the bottom wire as seen through the SiO$_2$ dielectric. The outline of the stud can also be seen due to a difference in niobium grain structure. (b) A sketch of CBKR geometry with a rectangular contact used in the analytical model in [20]. The actual shape of the contact between the studs and the top and bottom wires is circular as in figures 8 and 9(a).

Figure 10. Electrical properties of Nb studs: (a) room temperature Kelvin resistance of the stud structure shown in figure 9 as a function of design diameter of studs in the range relevant to the stud-via process, $d < 1 \mu m$; (b) full range of the studied diameters. Dotted black curves show the expected stud resistance $R_\text{st}$ from equation (2) at $t = 250 \text{ nm}$ and $R_s = 0.86$ $\Omega$/sq. Dashed lines shows the effect of a constant parasitic resistance $R_0$ in series with stud resistance $R_\text{st}$ for two values of $R_0$. Solid lines are the fits to equation (6) with $R_0$ as the only fitting parameter (see text).

where $t$ is the stud height (250 nm), $R_s$ is the sheet resistance of the Nb film from which the studs were etched, and $d_{av}$ is the average diameter of the stud on the wafer that is related to the design diameter $d$ as was discussed in section 3. We assume that the resistivity, $\rho$, of Nb in the studs after etching is nearly the same as the resistivity of the initial 200 nm Nb film ($R_s \approx 1.07$ $\Omega$/sq) in the trilayer, giving $R_s = 0.86$ $\Omega$/sq for the studs. Equation (2) at $t = 250$ nm and $R_s = 0.86$ $\Omega$/sq, and with $d_{av}$ given by equation (1) at $d_c = 0.255$ $\mu m$ and $b = -85$ nm, is shown in figure 10 by a dotted line. It describes the measured dependence only at very small diameters of studs (figure 10(a)) when their resistance is high and dominates the total resistance measured by the CBKR structure.

At large diameters, the measured resistance is much higher than that given by equation (2) and clearly has a tendency to saturation as the stud diameter increases. This could be explained if there exists a small constant parasitic resistance $R_0$ in series with the stud resistance, so the total measured resistance is $R_\text{tot} + R_0$, which approaches $R_0$ with increasing the stud diameter. Although the origin of this parasitic is not exactly clear, we noted its presence, with $R_0$ in the range from $\sim 20$ to $\sim 50$ m$\Omega$, in all of our room temperature measurements of studs and tunnel junctions using the described CBKR geometry. The effect of this parasitic series resistance is shown in figure 10(a) by dashed lines for two values of $R_0$. Although a better agreement could be reached in a narrow range of diameters (e.g., at $R_0 = 250$ m$\Omega$, figure 10(a)), this is clearly not sufficient to describe the measured dependence in a wider range of diameters of studs.

The CBKR geometry shown in figure 9 is frequently used for measurements of contact resistance between two materials or the resistance of various barriers between two materials. There is a great deal of literature devoted to its analysis, both analytical and numerical (see, e.g., [20] and references therein), particularly in cases when the barrier can be considered two dimensional, e.g., an opening in a non-conducting dielectric of very small thickness separating the top and bottom films as shown in figure 9(b). In the superconducting state, when there is no voltage drop associated with current redistribution (crowding) in the wires near the contact, it measures exactly the resistance of the barrier. In all
other cases, the measured Kelvin resistance $R_K$ includes parasitics associated with two-dimensional and three-dimensional current crowding effects. The analytic expression for the 2D parasitic resistance associated with current crowding in both films due to the finite surround of a rectangular contact was given in [20] as

$$R_{\text{geom}} = (8/3) R_{\text{wire}} s^2 / W_x W_y \{1 + 0.5 s / (W_x - s)\}$$

(3)

where $W_x$ and $W_y$ are the widths of the voltage and current electrodes, respectively, $s$ is the surround shown in figure 9(b) and $R_{\text{wire}}$ is the sheet resistance of the top and bottom wire films, assumed to be identical.

In order to make a comparison with equation (3) we replace the circular contact with diameter $d_{av}$ by a square contact with the same area. In our stud-via test structures the width of the wires was constant $W_x = W_y = W = 1.7 \mu$m for $d \leq 0.8 \mu$m, giving an effective surround $s = (W - (\sqrt{\pi}/2) d_{av})/2$, and

$$R_{\text{geom}} = (2/3) R_{\text{wire}} \{1 - (\sqrt{\pi}/2) d_{av}/W\}^2 \times \{1 + 0.5(W - (\sqrt{\pi}/2) d_{av})/(W + (\sqrt{\pi}/2) d_{av})\}$$

(4)

At larger diameters, $d > 0.8 \mu$m, we keep a constant design surround $s_0 = 0.425 \mu$m, so $W = d + 2s_0$ and $s = [d + 2s_0 - (\sqrt{\pi}/2) d_{av}] / 2$, resulting in

$$R_{\text{geom}} = (2/3) R_{\text{wire}} [(d + 2s_0 - (\sqrt{\pi}/2) d_{av})/(d + 2s_0)]^2 \times \{1 + [d + 2s_0 - (\sqrt{\pi}/2) d_{av}] / [(d + 2s_0 + (\sqrt{\pi}/2) d_{av})]\}. \tag{5}$$

We fitted the measured resistance $R_K$ to the sum of all three contributions

$$R_K = R_{\text{st}} + R_{\text{geom}} + R_0,$$ \tag{6}

with $R_{\text{geom}}$ given by equation (4) at $d \leq 0.8 \mu$m (figure 10(a)) and equation (5) at $d > 0.8 \mu$m (figure 10(b)), and treating $R_0$ as the only fitting parameter. We used the measured value of the sheet resistance for the top and bottom wires $R_{\text{wire}} = 1.07 \Omega/$sq and the same value of Nb resistivity for the studs, giving $R_{\text{st}} = 0.86 \Omega$/sq for studs. The obtained fits to equation (6) are shown in figure 10 by solid lines for the two ranges of stud diameters. As can be seen, the overall description of the data is very good in a very wide range of stud diameters and with only one fitting parameter.

4.2. Superconducting critical current

The critical current, $I_c$, of the fabricated studs (figure 11) was measured in liquid helium by taking $I-V$ characteristics. The transition into the resistive state at $I_c$ is very sharp and the return into the superconducting state occurs at a much lower current indicating significant thermal hysteresis.

From figure 11 we can see that $I_c$ scales properly with the actual area of the studs, $I_c = J_c \times$ Area. The current density $J_c$ was found to be $3 \times 10^7$ A cm$^{-2}$ (0.3 A $\mu$m$^{-2}$) and only about a factor of 2.5 lower than the Ginzburg–Landau depairing critical current density $J^{GL}_{c} = (2/3)^{1/2} B_c/\mu_0 \lambda$ in our films, where $\mu_0 = 4\pi \times 10^{-7}$ H m$^{-1}$, $B_c$—the thermodynamic critical magnetic field, $\lambda$—the magnetic field penetration depth [21]. Indeed, for Nb at 4.2 K, $B_c \approx 0.145$ T [22] and $\lambda$ is in the range from 80 to 90 nm for our films. This gives $J_{c}^{GL}$ in the range from $7 \times 10^7$ to $8 \times 10^7$ A cm$^{-2}$, see also [23]. In the actual structure, the critical current density should be somewhat lower than $J_{c}^{GL}$ of the film due to the presence of an 8-nm Al etch-stop layer at the interface between the Nb stud and the bottom Nb wire, making the structure an $SS' S$ junction of which properties depend on the parameters of the $S$ and $S'$ layers and the interface resistance between them [24].

On the other hand, in the studied range, the diameter of the studs is larger than $4\xi$, where $\xi$ is the coherence length that in our films is about 20 nm. Hence, instead of the depairing, the sud critical current can be caused by the entry and motion of Abrikosov vortices when the current-induced magnetic field at the stud surface reaches $B_{c1}$. This gives an estimate for the critical current density $J_c = B_{c1}/(\mu_0 \lambda)$. Using $B_{c1} = B_c \ln(\kappa + 0.08)/(\sqrt{2} \kappa)$ [25] with $\kappa = \lambda/\xi = 4$ for our
films, we get \( B_1 \approx 0.25B_0 \) and \( j_c \approx 0.36 A \mu m^{-2} \) in a perfect agreement with the critical current density observed in the fabricated Nb studs.

Independently of the actual critical current mechanism, the observed critical currents are more than sufficient for the use of stud-vias in superconducting integrated circuits for interlayer connections. At \( d = 0.5 \mu m \) the critical currents of stud-vias exceed those observed in etched contact holes of the same diameter filled with deposited Nb metal.

5. Conclusions

We have developed and demonstrated a novel process for making deep sub-\( \mu m \) superconducting multilayer interconnects for use in VLSI and ULSI superconductive digital circuits. These interconnects are formed using Nb/Al/Nb trilayers for wiring layers by etching Nb studs in the top layer and Nb wires in the bottom layer of the trilayers (a dual-etch process) with subsequent planarization of the formed interconnects by a dielectric CMP (DEAP process). The purpose of this process development is to replace the currently used etched contact holes filled with sputtered Nb that are too big for VLSI SFQ circuits.

Nb stud-vias with diameters as small as 150 nm have been fabricated by the developed process. For design stud diameters of 280 nm and above, the yield of the fabricated Nb stud-vias was 100% on the test structures available. Critical currents of the obtained Nb stud-vias approach the maximum possible superconducting currents for Nb-Ginzburg–Landau depairing current and are certainly sufficient for their use as interconnects in multilayered VLSI circuits.

We presented a detailed characterization of the stud photolithography process near the resolution limit of 248 nm photolithography as well as electric characterization at room temperature of the studs in a CBKR configuration, emphasizing the importance of parasitics related to current crowding around the studs. The performed analysis is also applicable to the fabrication of deep sub-\( \mu m \) Josephson junctions and to the characterization of their room temperature resistance for the purposes of process control and monitoring, especially in cases of junctions with high Josephson critical current densities when their tunnel resistance is low and the measured Kelvin resistance \( R_K \) is dominated by parasitics.

We proposed two versions of the stud-via process and presented a practical realization of one of them. The only other feasible alternative to the described processes would be a dual-damascene-type process with vias and trenches etched in the interlayer dielectric and filled by an advanced PVD (or CVD) process for Nb, and followed by CMP of Nb. It remains to be proven if such a fill process and CMP process can be developed and produce reliable and superconducting interconnects.

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