Improved Analysis Model of SiC Power MOSFET with Staged Critical Parameters

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Abstract. Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have great advantages in improving the power density and performance of power converters due to the high switching frequency, high operating voltage. However, the increase in switching frequency is also increasingly inflicted the voltage and current stresses to the parasitic elements of the SiC MOSFET, which restricts the device’s optimal performance. In addition, many parasitic elements of SiC MOSFET are coupled with each other during the switching process, which makes the analysis complicated and calculation cumbersome. This paper presents an analytical model for SiC MOSFETs, which identifies and selects the dominant elements and key variations of each stage separately according to the change stages of major variables. The complexity of the model is reduced while the accuracy is guaranteed. Using this model, the voltage and current switching rate of SiC MOSFET can be quickly solved, and the impact mechanism of each critical parameter can also be revealed clearly. A double pulse test circuit composed of a 600V/20A SiC MOSFET is set up and experimental results are obtained to verify the accuracy of the proposed analytical model.

1. Introduction

SiC MOSFET has advantages of fast switching speed, high operating voltage, and low on-state resistance, which are widely-used in high power, high frequency, and high temperature applications to improve the power density and efficiency [1-3]. Among these benefits, the fast switching performance plays a key role that determines the performance improvement ability of the power converter. However, accompanied by the large di/dt and dv/dt of the switching process, their effects on the parasitic elements of the SiC MOSFET become obvious and must be considered, they are the critical factors limiting the high performance and stability of the converter [4]. Moreover, the coupling of many parasitic elements also makes the construction of the switching model and the analysis complicated in the whole switching process.

For a non-linear variation switching process of SiC MOSFET, piecewise linear models are the commonly used analytical model [5], [6], which divides the nonlinear switching process into several approximate linear stages according to the change states of the main variables. In order to retain the accuracy of the calculation results, as for the circuits coupled with multiple parasitic elements, the equations need to consider as many details of the parasitic elements. It inevitably increases the order of the circuit equations, which makes the model become too complex [7]. Thus, the numerical solution obtained by such a model structure cannot fundamentally reveal the physical impacts of each parameter on the circuit’s response. However, some unimportant parameters are uniformly omitted to simplify the equations and obtain the analytical solutions of the responses. Such omissions may cause
errors or even ignore the impacts of certain parameters, reducing the accuracy and detailedness of the model [10], [16], [21]. These two aspects become a dilemma of analysis models to analyse the SiC MOSFET switching process.

In this paper, an improved analytical model for SiC MOSFET is proposed. The proposed model comprehensively considers all parasitic elements of the switching devices, including the parasitic capacitances, the parasitic inductances, and the transconductance. However, the dominant elements and key variations of each stage of the switching process are identified and selected separately according to their influence degrees on different variables. Non-critical parasitic elements and variables are omitted. The switching process can be described in detail stage by stage respectively, the complexity of the model can be reduced while ensuring the model accuracy, the impact mechanism of each critical parameter can also be revealed individually. The equivalent circuit for the bridge-leg of each stage are derived. A double pulse test circuit composed of a 600V, 20A SiC MOSFETs and a SiC JBS diode is set up and experimental results are obtained to verify the accuracy of the proposed analytical model.

2. Analysis of switching process
In this section, the switching process of a SiC MOSFET is introduced and a double-pulse-test circuit is used as an example. Fig. 1 shows the double-pulse-test circuit, which includes the parasitic elements of the SiC MOSFET, the freewheeling diode FWD, the power loop, and the driver loop. Parasitic elements of the SiC MOSFET need to consider internal of the device package and the external circuit traces. Internal parasitic elements include interelectrode capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$, parasitic inductances $L_{g,\text{in}}$, $L_{d,\text{in}}$, and $L_{s,\text{in}}$, internal gate drive resistance $R_{g,\text{in}}$, and the antiparallel freewheeling diode $D_b$. Due to the improvement of packaging technology, the inside parasitic inductances of the device are very small. The external parasitic elements are the stray inductances of the electrode pins and the circuit traces connected with gate, source, and drain, which are represented by $L_{g,\text{ex}}$, $L_{d,\text{ex}}$, and $L_{s,\text{ex}}$, respectively. There are extra stray inductances in the power loop lumped by $L_{\text{LOOP}}$. In order to facilitate the analysis, $L_{\text{LOOP}}$ is lumped into $L_{\text{diff,ex}}$ in the subsequent discussion, and $L_g = L_g,\text{ex} + L_g,\text{in}$, $L_d = L_d,\text{ex} + L_d,\text{in}$, $L_s = L_s,\text{ex} + L_s,\text{in}$ are denoted as the total gate, drain, and source inductances. The gate of SiC MOSFET is connected with the gate driver through the driver loop, which include external drive resistances $R_{g,\text{ex}}$. The rise and fall time of the gate driver are neglected in the analysis. The DC input voltage $V_{DD}$ is modeled as a constant voltage source, and the output current $I_{\text{LOAD}}$ is regarded as a constant current source.

![Figure 1. Double-pulse-test circuit and the parasitic elements of the SiC MOSFET](image)

2.1 Turn-on Switching Transition
Before the gate signal turns high, the SiC MOSFET is in the cut-off state, the load current $I_{\text{LOAD}}$ flows through the freewheeling diode FWD.

Stage 1, turn-on delay time: The gate signal become high at $V_{\text{GATE}}$, and the gate current charges the input capacitance $C_{gr}$ and $C_{gd}$. The gate-source voltage $V_{gs}$ starts to rise and the gate-drain voltage experiences a slight drop. Since $V_{gs}$ does not reached the threshold voltage $V_{th}$, the SiC MOSFET...
remains cut-off and almost no drain current flows. The equivalent circuit of this stage is shown in Fig.2, the circuit equations are established as

\[ V_{gs} = V_{gd} + V_{ds} \]  
\[ i_g = C_{gs} \frac{dV_{gs}}{dt} + C_{gd} \frac{dV_{gd}}{dt} \]  
\[ i_d = -C_{gd} \frac{dV_{gd}}{dt} \]  
\[ V_{GATE} = R_i i_g + L_g \frac{di_g}{dt} + V_{gs} + L_s \frac{di_s}{dt} + L_d \frac{di_d}{dt} \]  
\[ V_{DD} = V_{ds} + L_d \frac{di_d}{dt} + L_s \frac{d(i_g + i_d)}{dt} \]

For SiC MOSFET, in general, the value of \( C_{gs} \) is a hundredfold or more than \( C_{gd} \). Thus, the current flowing through \( C_{gd} \) and the small voltage drop on the drain parasitic inductance \( L_d \) can be neglected, the neglected parasitic element and circuits are represented by dashed lines in Fig. 2. The simplified expressions of \( i_g \) and \( V_{gs} \) shown in (2) and (4) become (6) and (7) in this case.

\[ i_g = C_{gs} \frac{dV_{gs}}{dt} \]
\[ V_{GATE} = R_i i_g + \left( L_g + L_s \right) \frac{di_g}{dt} + V_{gs} \]

Combining (1), (3), (5), (6), and (7), The drive loop is a zero-state step response of a second-order circuit, the equations can be obtained as

\[ \left( L_g + L_s \right) C_{gs} \frac{dV_{gs}^2}{dt^2} + R_i C_{gs} \frac{dV_{gs}}{dt} + V_{gs} = V_{GATE} \]

Figure 2. Equivalent circuits for Stage 1.

**Stage 2, channel current rising time:** The equivalent circuit of this stage is shown in Fig.3. When \( V_{gs} \) reaches \( V_{th} \), the SiC MOSFET starts conducting and its channel current \( i_{ch} \) increases from zero. \( I_{LOAD} \) transfer from FWD to the SiC MOSFET. SiC MOSFET works in the saturation region and \( i_{ch} \) is controlled by \( V_{gs} \), their relationship can be described as

\[ i_{ch} = g_f \left( V_{gs} - V_{th} \right) \]

Where \( g_f \) is the transconductance coefficient of the SiC MOSFET, it increases nonlinearly with the increase of \( V_{gs} \) until it becomes gentle and the rising rate of \( i_{ch} \) reaches the maximum. The rapid current switching of the power loop in this stage causes induced voltages on \( L_d \) and \( L_s \), which induces a slight drop on \( V_{ds} \), the circuit equations of the power loop can be expressed as

\[ V_{gs} + \left( L_d + L_s \right) \frac{di_g}{dt} + L_s \frac{di_s}{dt} = V_{DD} \]

For the driver loop, same as Stage 1, most of driver current continues to charge \( C_{gs} \) and the influence of the current flowing through \( C_{gd} \) can still be neglected. The induced voltages on the common source parasitic inductance \( L_s \) are also superimposed in the drive loop, which affects the response of the drive loop. The driver loop equation can be expressed a
\[ R_s i_s + (L_s + L_i) \frac{di_d}{dt} + L_s \frac{di_s}{dt} + V_{gs} = V_{GATE} \quad (11) \]

When the rising rate of \( i_d \) approaches its maximum, the induced voltage on \( L_d \) and \( L_s \) remain constant. Thus, the power loop current can be considered as \( i_d = i_{ch} \). By combining (6) and (9)-(11), the drive loop equation can be obtained as

\[ \left( L_g + L_i \right) C_{gs} \frac{d^2 V_{gs}}{dt^2} + \left( R_g C_{gs} + L_s g_f \right) \frac{dV_{gs}}{dt} + V_{gs} = V_{GATE} \quad (12) \]

In this way, the response of \( V_{gs} \) and \( i_d \) can be deduced as complete responses of second-order circuits.

\[ V_{miller} = I_{LOAD} + V_{th} \quad (13) \]

Thus, the current flowing through \( C_{gs} \) decreases significantly and can be neglected. The equivalent circuit of this stage is shown in Fig. 4. Due to the voltage clamping phenomenon in saturation region, the maximum \( i_s \) is limited by

\[ \text{Figure 3. Equivalent circuits for Stage 2.} \quad \text{Figure 4. Equivalent circuits for Stage 3.} \]
\[ i_g = \frac{V_{GATE} - V_{miller}}{R_g} \]  
(14)

And \( i_g \) can also be expressed as

\[ i_g = C_{gd} \frac{dV_{gd}}{dt} \]  
(15)

Combining (1), (13)-(15), the decrease rate of \( V_{ds} \) can be obtained as

\[ \frac{dV_{ds}}{dt} = (V_{GATE} - V_{ds}) g_f - I_{LOAD} \]  
(16)

**Stage 4, \( V_{gs} \) remaining rising time:** When \( V_{ds} \) reaches the on-state voltage, SiC MOSFET works in the ohmic region and \( i_{ch} \) is separated from the relationship with \( V_{gs} \). \( C_{gs} \) and \( C_{gd} \) start charging and \( V_{gs} \) continues to rise to \( V_{GATE} \). The equations of the driver loop are the same as (11) in Stage 2, \( i_g \) can be expressed as

\[ i_g = (C_{gs} + C_{gd}) \frac{dV_{gs}}{dt} \]  
(17)

Combining (11) and (41), the drive loop equation can be obtained as

\[ (L_g + L_f)(C_{gs} + C_{gd}) \frac{d^2V_{gs}}{dt^2} + R_g (C_{gs} + C_{gd}) \frac{dV_{gs}}{dt} + V_{gs} = V_{GATE} \]  
(18)

### 2.2 Turn-off Switching Transition

**Stage 5, turn-off delay time:** When the gate signal is set to zero, \( C_{gd} \) and \( C_{gd} \) start discharging through the driver loop and \( V_{gs} \) decreases. The SiC MOSFET operates in the ohmic region until \( V_{gs} \) drops to \( V_{miller} \). \( i_d \) keeps flowing through the channel and remains unchanged. The driver loop equation is given by (19), and \( i_g \) still expressed by (17). The characteristics of the driver loop keep same with Stage 4.

\[ V_{gd} + R_{gd} \frac{di_g}{dt} + (L_{gd} + L_{gt}) \frac{di_{gt}}{dt} = 0 \]  
(19)

**Stage 6, voltage rising time:** The SiC MOSFET enters the saturation region in this stage and the channel resistance starts to increase. The load current continues to support through the channel due to FWD is reverse-biased. \( V_{ds} \) starts to rise and the reversed bias voltage of FWD, \( V_F \), decreases until it reaches the forward turn-on voltage. \( C_{gd} \) and \( C_{gd} \) are charged and the junction capacitance of FWD, \( C_F \), discharged, these capacitance displacement currents supply part of load current which causes \( i_{ch} \) decreases to some extent.

If \( I_{LOAD} \) is large, except that the shunt current due to the parasitic capacitances charging process during the voltage rising stage, most of the current needs to be maintained through the channel of the SiC MOSFET. Similar to Stage 3, The main factor that determines the rising rate of \( V_{ds} \) is determined by the driver loop.

However, due to the channel current changes in this stage, the induced voltage is generated on the parasitic inductance of common source, induced voltage on the common source parasitic inductance is superimposed on the drive circuit. The equivalent circuit of this stage is shown in Figure 5. the drive loop equation can be expressed as

\[ R_g \frac{di_g}{dt} + V_{miller} + L_g \frac{di_g}{dt} = 0 \]  
(20)

Where \( i_g \) is same as (15). As for the power loop, the charging circuit contains all the parasitic inductances of the power loop, which must be considered, the equations can be expressed as

\[ -R_g \frac{di_g}{dt} - L_g \frac{di_g}{dt} - V_{gs} + L_d \frac{di_d}{dt} = V_{DO} \]  
(21)

**Stage 7, current falling time:** After FWD reaches the forward voltage, the current begins to transfer from the channel of the SiC MOSFET to FWD. Constrained by transconductance, the decrease rate of
$i_{th}$ is determined by the drop rate of $V_{gs}$ since the constraint of the transconductance. The drive loop equation can be expressed as

$$R_g i_g + \left( L_s + L_r \right) \frac{di}{dt} + L_r \frac{di}{dt} + V_{gs} = 0 \quad (22)$$

Where $i_g$ can be described by (6). When $V_{dt}$ reaches $V_{DD}$, the charge rate of $C_{gd}$ no longer dominates the rising rate of $V_{ds}$, it is paralleled with and involved in the oscillating of the power loop. However, similar to Stage 2, the displacement current of $C_{gd}$ is much smaller than the charge current of $C_{ds}$ and the discharge current of $C_{gs}$, which exerts little influence to the driver loop and can be neglected in this stage. The equivalent circuit of this stage is shown in Fig. 6. Part of the drain current flows through $C_{ds}$ dominates the oscillation of $V_{ds}$. The remaining current flows through the channel, $i_d$ can be expressed as

$$i_{dif} = i_g + C_{ds} \frac{dV_{ds}}{dt} \quad (23)$$

The power loop can be established as

$$\left( L_d + L_s \right) \frac{di}{dt} + L_r \frac{di}{dt} + V_{ds} = V_{LOD} \quad (24)$$

Figure 5. Equivalent circuits for Stage 6.  Figure 6. Equivalent circuits for Stage 7.

Stage 8, $V_{gs}$ remaining dropping time: When the load current flows entirely through FWD, the SiC MOSFET is completely shut down and $V_{gs}$ decreases to zero, while the voltage and current of the power loop keep oscillation, it is damped by the stray resistance of the power loop.

3. Simulation and experimental results

In order to verify the accuracy of the phased key parameter model, the simulation results of the proposed model are compared with the experimental results in consistency. A 600V/20A double pulse test circuit is established, which is composed of the SiC MOSFETs, C2M0080120D, and freewheeling diode, C4D10120D, from CREE company. The circuit parameters and the value of parasitic elements are based on this real circuit configuration within reasonable ranges, and then the switching process can be simulated by MATLAB calculations stage-by-stage. A 20 μH ferrite-core inductor is connected in parallel with the freewheeling diode as the load inductor. The test circuit is fed by 600V dc supply voltage, multiple groups of capacitors are connected in parallel to ensure the stability of the support dc voltage. The external and internal pins of the devices and the printed circuit board PCB layout is implemented by finite-element analysis of ANSYS Q3D [8]. The measurement and extraction results are listed in Table 1. The gate drive resistances are chosen as 10Ω.

In the simulation calculations, for the turn-on stages and Stage 5 and Stage 8 of turn-off process, the key variables can be obtained directly by solving the second-order circuit response, while for Stage 6 and Stage 7, since the overlapping of the voltage and current, the state variables of the model were increased, it is difficult to derive the time domain solutions without simplification. In order to ensure accurate of the simulation, the iterative computation is employed.
Table 1. Initial parameter setup

| Component          | Parameter | Value   | Parameter | Value   |
|--------------------|-----------|---------|-----------|---------|
| Power circuit      | $V_{DDH}$ | 600V    | $L_{d_{ex}}$ | 5.5nH   |
|                    | $I_{DD}$  | 20A     | $L_{LOO}$  | 50nH    |
|                    | $V_{GATE}$| 20V     | $R_{LOO}$  | 120mΩ   |
| SiC MOSFET         | $V_{th}$  | 3.4V    | $L_{s_{in}}$| 1.2nH   |
|                    | $R_{g_{ex}}$| 10Ω    | $C_{gs}$   | 950pF   |
|                    | $R_{d_{in}}$| 3.9Ω   | $C_{ds}$   | 73pF    |
|                    | $L_{g_{in}}$| 1.2nH  | $C_{gd}$   | 7.6pF   |
|                    | $L_{d_{in}}$| 1.0nH  |           |         |
| SiC Diode (C4D10120D) | $V_F$       | 1.5V    | $C_F$     | 754pF   |

In the experimental test, the switching processes of SiC MOSFET under different voltage and current states are tested by setting different dc supply busbar voltages and adjusting the double pulse trigger signal position to change the load current. The comparison of simulation and experiment results are shown in Figure 7.

![Waveforms](image)

(a) (b) (c)

Figure 7. Comparison of experiment and analytical waveforms. Left: turn-on waveforms, right: turn-off waveforms: (a) 600V/20A. (b) 600V/10A. (c) 400V/20A

It can be seen from Figure 7 the analytical results match test results very well. The proposed analytical model can correctly represent the switching transient waveforms in terms of voltage and current switching speed of turn-on and turn-off switching process.

4. The critical parameters induction

At different stages of SiC MOSFET switching process, the critical parameters that are directly related to or indirectly coupled to the main variables are different. Based on the preceding discussion and the experimental verification, the effects of the critical element of each stage on the main variable performance can be summarized in Table 2. The dominant elements that affect the response of the main variables and the key coupling variables are summed up as the critical parameters of each stage. Non-critical parasitic elements and variables can be omitted flexibly.
Table 2. The critical parameters of each stage

| stage | Main variable | Critical parameter | Omit parameter |
|-------|--------------|--------------------|---------------|
| 1     | $V_{gs}$     | $L_s, R_g, C_g$    | $C_{gs}$      |
| 2     | $dV_{ds}/dt$ | $L_s, R_g, C_g$    | $di_{ds}/dt$  | $C_{gd}$      |
| 3     | $V_{gs}$     | $L_s, R_g, C_{gd}$ |               | $C_{gs}, L_s$ |
| 4     | $dV_{gs}/dt$ | $L_s, R_g, C_{gd}$ |               | $C_{gs}, L_s$ |
| 5     | $V_{gs}$     | $L_s, R_g, C_{gd}$ |               | $C_{gs}, L_s$ |
| 6     | $i_d$        | $C_{gd}, R_{ps}, L$| $i_{ds}$      | $C_{gd}, L_g$ |
| 7     | $dV_{ds}/dt$ | $L_s, R_g, C_g$    | $di_{ds}/dt$  | $C_{gd}$      |
| 8     | $V_{gs}$     | $L_s, R_g, C_g$    |               | $C_{gd}$      |

5. Conclusion
In this paper, a staged analysis model of SiC MOSFET switch with key parameters is presented. The proposed model takes into account the effects of parasitic inductances, parasitic capacitances and transconductance on the switching process. The critical parameters are distinguished flexibly and emphatically stage-by-stage according to the change sequence of the main variables. The complexity of the model is reduced while ensuring its accuracy. The switching rate of the SiC MOSFET can be accurately described and the mechanism of key elements' influence can be clearly demonstrated. The proposed analytical model is accurate and matches better with experimental results.

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