Online Training of Spiking Recurrent Neural Networks with Phase-Change Memory Synapses

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Abstract

Spiking Recurrent Neural Networks (RNNs) are a promising tool for solving a wide variety of complex cognitive and motor tasks, due to their rich temporal dynamics and sparse processing. However, training spiking RNNs on dedicated neuromorphic hardware is still an open challenge. This is due mainly to the lack of local, hardware-friendly learning mechanisms that can solve the temporal credit assignment problem and ensure stable network dynamics, even when the weight resolution is limited. These challenges are further accentuated, if one resorts to using memristive devices for in-memory computing to resolve the von-Neumann bottleneck problem, at the expense of a substantial increase in variability in both the computation and the working memory of the spiking RNNs. To address these challenges and enable online learning in memristive neuromorphic RNNs, we present a simulation framework of differential-architecture crossbar arrays based on an accurate and comprehensive Phase Change Memory (PCM) device model. We train a spiking RNN whose weights are emulated in the presented simulation framework, using a recently proposed e-prop learning rule. Although e-prop locally approximates the ideal synaptic updates, it is difficult to implement the updates on the memristive substrate due to substantial PCM non-idealities. We compare several widely adapted weight update schemes that primarily aim to cope with these device non-idealities and demonstrate that accumulating gradients can enable online and efficient training of spiking RNNs on memristive substrates.

1 Introduction

RNNs are exceptionally expressive [1] class of neural networks that have been successfully adapted in many domains such as audio processing, optical flow, language modeling and Reinforcement Learning (RL) [2, 3, 4, 5, 6, 7]. The power of RNNs lie in their architecture that allows processing of long and complex sequential data. Due to its recurrent architecture, each neuron contribute to the network processing at various points of the computation. The resulting efficiency of RNNs is also evident in the mammalian brain with massive lateral recurrent connections in neocortex [8, 9]. However, the training of RNN topologies is notably difficult under constrained memory and computational resources [10].
Current hardware implementations of neural networks still cannot compete with the energy efficiency of biological systems. One of the main reasons for this difference is due to the data movement between the separated processing and memory units of the von-Neumann architectures used to implement the artificial neural networks. Recently, new types of compact nanoscale devices have garnered significant attention for implementing artificial synapses [11, 12, 13, 14, 15, 16] that can implement in-situ learning and break the von Neumann bottleneck [17, 18]. These memristive devices are particularly promising for use in Spiking Neural Network (SNN) architectures, especially for low-power, sparse and massively parallel spike-based neuromorphic systems, that emulate the principles of computation observed in biological brains [19, 20]. In these systems, the synapses (memory) and neurons (processing units) are arranged in a crossbar architecture as shown in Fig. 1a, where memristive devices are placed at the junctions, to store the synaptic efficacy in their programmable conductance values. The crossbar architecture implements in-memory computation of synaptic propagation between neurons by a single physics-based operation following Ohm’s Law and Kirchhoff’s Law, intrinsically supporting the sparse and event-driven nature of SNNs. As recently shown in [21] and [22] for 32 nm technology, compared to a digital Complementary Metal-Oxide-Semiconductor (CMOS) implementation (i.e. Static Random Access Memory (SRAM)) such memristive crossbar arrays enable a denser solution, and have respectively lower and similar dynamic energy consumption during inference and training. Moreover, the non-volatile nature of memristive devices reduces the static power consumption usually linked with volatile CMOS memory storage. Therefore, in-memory acceleration of spiking RNNs with non-volatile multi-bit-resolution memristive devices is a promising direction for scalable neuromorphic hardware for temporal signal processing.

PCM devices are among the most mature emerging resistive memory technologies. Their tiny footprint, fast read/write operation and multi-bit storage capacity make PCMs an ideal candidate for implementing in-memory computation of synaptic propagation [23, 24]. Consequently, there has been an increased interest for the employment of PCM technology in neuromorphic computing applications [11, 25, 26, 27].

Single PCM device can have 3-4 bits of resolution [28], however, unlike conventional digital CMOS memories, they are affected by severe non-idealities as their switching physics is governed by inherently stochastic Joule heating. Moreover, molecular dynamics of PCMs give rise to the $1/f$ noise behavior and the structural relaxation, resulting in cycle-to-cycle variation, in addition to their device-to-device variability present due to fabrication effects.

To account for these device non-idealities, one could follow a hardware-algorithm co-design approach with chip-in-the-loop setups that leverage PCM crossbar hardware [11]. However, training a neural network requires the iterative evaluation of multiple network architectures, modifications to the learning rule and tuning hyperparameters on large datasets, which are extremely time/resource consuming with chip-in-the-loop setups. On the other hand, a software network simulation framework with a statistical model of memristive devices offers much faster iteration times and a better understanding of device effects on the training, due to increased observability of internal state variables. However, it is extremely important to have a very accurate statistical model of the devices simulated, to optimize the training procedure of the network before moving to chip-in-the-loop training.

In this paper, we investigate whether a spiking RNN can be trained with a local learning rule despite the adverse impacts of in-memory computing with memristive devices such as write noise, read noise, temporal conductance evolution (i.e., drift) and the limited bit precision. To do so, we first build on the statistical PCM model from Nandakumar et al. [29] to faithfully model a crossbar array comprising a differential memristor configuration (Section 2.1). Then, we define a target spiking RNN architecture and describe the properties of an ideal learning rule and select e-prop algorithm [30] to train the network (Section 2.2). In order to map ideal weight updates calculated by e-prop to memristor conductances on the crossbar array, we implement multiple memristor-aware weight update methods that are optimized to cope with device non-idealities (Section 2.3). Finally, we report a training scheme for spiking RNNs which exploits in-memory computing with extremely sparse activity and a reduced number of conductance updates for energy efficient training (Section 4).
Figure 1: a. PCM devices can be arranged in a crossbar architecture to emulate both a non-volatile synaptic memory and a parallel and asynchronous synaptic propagation using in-memory computation. b. Mushroom-type geometry of a single PCM device. The conductance of the device can be reconfigured by changing the volume ratio of amorphous and crystalline regions.

2 Building Blocks for In-Memory Acceleration of RNN Training for Neuromorphic Processors

In the following, we describe the main components of our simulation framework for training spiking RNNs with PCM synapses.

2.1 PCM Synapses

The material design of a nanoscale PCM device typically includes the switching material Ge$_2$Sb$_2$Te$_5$ (GST) placed between two metal electrode layers forming a mushroom-type structure (Fig. 1b). By applying short electrical pulses, the temperature distribution inside the PCM device can be momentarily modified via Joule heating. The controlled temperature levels can switch the molecular configuration of GST between the amorphous (high-resistance) and crystalline (low-resistance) states [31].

To increase the volume of the amorphous state in the device, a short and high-amplitude electrical pulse (RESET pulse) is applied to the device terminals. Increasing the temperature to around 900 K melts a significant portion of the GST, and if the GST quenches rapidly, melted region forms an amorphous configuration. On the contrary, to increase the crystalline volume, typically a longer and smaller-amplitude electrical pulse (SET pulse) is applied to the device terminals. In this case, temperature rises to around 400-600 K, which initiates the growth of available crystal nuclei inside the GST and increases the crystalline volume. To read the device conductance, an electrical pulse with an even smaller amplitude (READ pulse) is applied to the device, in order to prevent any phase transition. The amplitude and duration of SET, RESET and READ pulses depend on the GST composition and device volume. Nevertheless for a typical mushroom type geometry with 100 nm GST and 20 nm heater radius (see Fig. 1b), a SET pulse of 2.5V amplitude and 100 ns duration, a RESET pulse of 3.5 V amplitude and 20 ns duration and READ pulse of 0.2 V 50 ns duration can be used [31].

In practice however, the programming operations of such devices suffer from write noise, read noise, and the electrical conductance drift [32]. The asymmetry of the SET and RESET operations, and the nonlinear conductance response with respect to the number and frequency of the pulses applied further complicates the precise programming of the device conductance to target values. It is therefore critical to fully capture these non-ideal phenomena and device dynamics in the network models, because only then important metrics such as the robustness of the weight update rule, hyperparameter choices or the training duration can be realistically evaluated, reflecting the real-world deployment of the neuromorphic system. Many comprehensive models have been proposed to describe electrical [33], thermal [34], structural [35, 36] and phase-change [37, 38] properties of PCMs. These device

\[\text{The code is available at https://github.com/YigitDemirag/srnn-pcm}\]
models either require solving on-the-fly differential equations whose numerical convergence is not guaranteed, or do not incorporate inter- and intra- device stochasticity, or are designed for pulse shapes and current-voltage sweeps that do not reflect the operational conditions on the circuit [31].

In this study, we selected the statistical device model from Nandakumar et al. [29], which comprises all major forms of PCM-specific non-idealities based on measurements from 10,000 devices. The model includes the nonlinear conductance change with respect to applied pulses, conductance-dependent write and read operation stochasticity, and the temporal drift effect (Fig. 2). The model keeps a programming history variable, which represents the nonlinear device response to consecutive SET pulses and is updated after the application of each pulse. Following the application of a new SET pulse, the model samples the conductance change $\Delta G$ from a Gaussian distribution whose mean and standard deviation is based on the programming history and the previous conductance. The drift behavior is then included following the empirical exponential drift model [36] $G(t) = G(T_0) (t/T_0)^{-v}$, where $G(T_0)$ is the estimated conductance after a WRITE pulse at time $T_0$ and $G(t)$ is the final device conductance considering the effect of the drift. Additionally, the model takes into account the $1/f$ READ noise [39], which increases monotonically with the device conductance.

Overall, this statistical PCM model captures the stochastic conductance changes due to the application of SET and READ pulses and estimates the temporal conductance drift arising from the structural relaxation.

In order to integrate this model into neural network simulations, we developed a comprehensive PCM crossbar array simulation framework in PyTorch [40]. Our crossbar array simulation framework can keep track of all simulated PCM devices simultaneously, enabling realistic SET, RESET and READ operations (for implementation details, see Supplementary Note 1). Section 3 will describe how this framework is used to represent synaptic weights of a RNN.

2.2 Credit Assignment Solutions for Recurrent Network Architectures

The credit assignment problem refers to the problem of determining the amount of change required in each synaptic weight to achieve the network’s desired behavior [41]. The nature of this problem is intertwined with network architecture which describes the arrangement of synapses, neurons and their operational principles. Hence many proposed solutions to the credit assignment problem in SNNs landscape are specific to a network architecture components e.g., eligibility traces [42], dendritic [43] or neuromodulatory [44] signals.

In this work, we simulated the neuron dynamics using the Leaky Integrate-and-Fire (LIF) neuron model [45, 46]. LIF neurons are stateful through their membrane potential, and their temporal dynamics in a spiking RNN can be simulated with the following discrete-time equations [30]:

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Figure 2: The chosen PCM model from [29] captures the major device non-idealities. a. The WRITE model enables calculation of the conductance increase with each consecutive SET pulse applied to the device. The band illustrates one standard deviation. b. The READ model enables calculation of $1/f$ noise, increasing as a function of conductance. c. The DRIFT model calculates the temporal conductance evolution as a function time. $T_0$ indicates the time of measurement after the initial programming of the device.
\[ v_j^{t+1} = \alpha v_j^t + \sum_{i \neq j} W_{ji}^{\text{rec}} z_i^t + \sum_i W_{ji}^{\text{in}} x_i^t - z_j^t \theta_{\text{th}} \]

\[ z_j^t = H \left( \frac{v_j^t - v_{\text{th}}}{v_{\text{th}}} \right) \]

\[ y_k^{t+1} = \kappa y_k^t + \sum_j W_{kj}^{\text{out}} z_j^t \]

where \( v_j^t \) is the membrane voltage of neuron \( j \) at time \( t \). The output state of a neuron is a binary variable, \( z_j^t \), that can either indicate a spike, 1, or no spike, 0. The neuron spikes when the membrane voltage exceeds the threshold voltage \( v_{\text{th}} \), a condition that is implemented based on the Heaviside function \( H \). The parameter \( \alpha \in [0, 1] \) is the membrane decay factor calculated as \( \alpha = e^{-\delta t/\tau_m} \), where \( \delta t \) is the discrete time step resolution of the simulation and \( \tau_m \) is the neuronal membrane decay time constant, typically tens of milliseconds. The network activity is driven by input spikes \( x_i^t \). Input and recurrent weights are represented as \( W_{ji}^{\text{in}} \) and \( W_{ji}^{\text{rec}} \) respectively. At the output layer, the recurrent spikes are fed through readout weights \( W_{kj}^{\text{out}} \) into a single layer of leaky integrator units \( y_k \) with the decay factor \( \kappa \in [0, 1] \). This continuous valued output unit is analogous to a motor function which generates coherent motor output patterns [47] of the type shown in Fig. 3.

The aim of the training process is to find optimal network weights \( \{ W_{ji}^{\text{in}}, W_{ji}^{\text{rec}}, W_{kj}^{\text{out}} \} \), that maximize the performance of the network [41]. One approach is to train the spiking RNNs offline, using any optimization method, and then transfer the weights to the crossbar via an iterative procedure for inference applications [48]. However this would not take into account the non-idealities of PCM synapses. Our aim is to develop an online training framework that can compensate for these non-idealities. To be suitable for neuromorphic hardware, this framework must use a learning algorithm that is (i) local, (ii) online and (iii) well-tested beyond toy problems. For example, the FORCE algorithm performs well on motor tasks [49, 47], however the weight updates require the knowledge of all synaptic weights, which violates the first requirement. Similarly, training the network with Back-propagation Through Time (BPTT) using surrogate gradients [50, 51] is not an option as it requires buffering all intermediate neuron states to calculate updates backward in time, which violates the second requirement.

One promising solution to the credit assignment problem in the spiking RNN landscape is provided by the e-prop algorithm [30]. It has been shown that e-prop can offer an accuracy similar to that of Long Short Term Memory (LSTM) networks [52] trained with BPTT on complex temporal tasks. As this algorithm works by factorizing the gradients of BPTT as a sum of products between instantaneous learning signals and local eligibility traces, it is both online and local. Similar to e-prop, the recently published Online Spatio-Temporal Learning (OSTL) algorithm [53] also supports complex recurrent architectures, and in addition it is able to generate the exact gradients calculated with BPTT.

### 2.3 Memristor-Aware Weight Update Optimization

Many neuromorphic processors with on-chip learning include a Learning Block (LB) connected to the neuron circuits [54, 55, 19]. The function of LB is to continuously compare the activity of the neuron with a desired target activity, and (ii) estimate the amount of required change in the neuron’s synaptic weights, based on the implemented learning rule and error function. When the weight update condition is met, which can be on the arrival of the pre-synaptic spike, on the post-synaptic spike, or on a error-driven signal [56], the LB instructs the corresponding synapses to update the weight with the calculated weight change. However, memristive synapses cannot be easily programmed to target specific conductances, due to device non-idealities such as limited bit precision, asymmetric SET/RESET updates and programming noise.

Weight update mechanisms in memristive architectures are primarily designed to cope with memristive non-idealities to execute the desired weight changes on synapses. These mechanisms are typically single-shot, i.e. one or multiple gradual SET pulses are applied without reading the device state. This avoids iterative write-read-verify schemes or modifications of the pulse shape during the training, and hence enables simpler circuits with a better energy efficiency. In our framework we use a differential synaptic configuration [29, 57, 58], where every synapse keeps two sets of memristors (\( G^+ \) and \( G^- \))
whose difference gives the effective synaptic conductance (Fig. 1a), so that both positive and negative synaptic weights can be represented using memristor conductances.

With this differential configurations however the unidirectional updates used to update the synaptic weight may result in the saturation of either or both of the devices in the synapse [29, 57, 58]. One solution to the problem would be to employ a push-pull mechanism: to increase the synaptic efficacy, the positive memristor conductance is increased while the negative memristor conductance is decreased [59]. Unfortunately this mechanism is not compatible with PCM devices as the melt-quenching-based RESET is an abrupt process [60], thus requiring a refresh mechanism by resetting both positive and negative memristors and reprogramming them to their effective conductances when specific criteria is met. In the following, we will describe four weight update methods that the neuromorphic processors have widely adopted and are implemented in the PCM crossbar array simulation framework.

**The Sign Gradient Descent.** In this method, synaptic weights are updated according to the sign of the gradient of the loss function, estimated by the learning algorithm. The idea of the sign gradient descent is to take a fixed step \( \delta \) in the direction of descending gradient, but neglecting its magnitude. Nevertheless, under some assumptions, the convergence is guaranteed [61]. The synaptic weight updates \( \Delta W \) can be computed as

\[
\Delta W = -\delta \operatorname{sign}(\nabla L)SL,
\]

where \( \delta \) is the amount of change, \( \nabla L \) is the gradient calculated by the chosen learning rule, and \( SL = |\nabla L| > \theta \) is a binary variable indicating a stop-learning regime. The latter increases the stability during learning, which enables updates only when the magnitude of the gradient is higher than a fixed threshold \( \theta \).

Due to its simplicity, the sign gradient descent is popular among memristive neuromorphic systems [62, 63, 64]. When implementing it with memristor synapses, the LB sends a single UP (or DOWN) pulse to instruct an increase (or decrease) of the synaptic weights. Hence, on the onset of the weight update, a single SET pulse is applied either to the \( G^+ \) or the \( G^- \) PCM device, determined by the sign of the gradient. However, the effective value of \( \delta \) is not a constant due to the WRITE noise, and not symmetric because SET operation in PCM is gradual whereas RESET is abrupt.

**Stochastic Update.** Conventional optimization methods demand the amount of weight change at every weight update to be 3-4 orders of magnitude smaller than the original weight [65], usually requiring at least an 8-bit weight representation, whereas a typical PCM device can only represent 3-4 bits of information [66].

Therefore, even a single WRITE pulse applied to a PCM device leads to an order-of-magnitude overshoot compared to the desired amount of weight change typically calculated by the LB. One method used by Nandakumar et al. [29] aims at overcoming this scaling disparity by stochastically executing (or skipping) the weight updates depending on the magnitude of the gradient.

We implemented the stochastic weight update on our PCM crossbar simulation by scaling the gradient magnitude with a scaling factor, \( p \), to represent the update probability such that

\[
P(\text{update}) = \frac{|\nabla L|}{p}
\]

By tuning the scaling factor, the number of devices that get programmed can be controlled. Single pulses are applied accordingly to the synapses. The refresh criteria, unlike the original work [29], is checked and applied before the weight update to prevent the execution of the update on saturated devices.

**Multi-memristor Update.** To increase the dynamic range and the resolution of the synaptic weights, the concept of multiple PCM devices per synapses has been proposed in [57], where each synapse consists of \( 2N \) memristors (\( N \) positive and negative pairs in a differential configuration), the total conductance determining the synaptic efficacy. The updates are applied to the devices sequentially, which in turn decreases the smallest mean weight change by a factor of \( 2N \) and reduces the variance due to WRITE noise by a factor of \( \sqrt{2N} \) [57] (see Supplementary Note 3).
Figure 3: Overview of the spiking RNN training framework of the proposed PCM crossbar array simulation framework, illustrated here for a pattern generation task. The network weights are allocated from three crossbar array models, $G_{\text{inp}}$, $G_{\text{rec}}$, $G_{\text{out}}$. The network-generated pattern and the target pattern are compared to produce the learning signal which is fed back to every neuron. The LB calculates instantaneous weight changes $\Delta W$ using the e-prop learning rule and has to efficiently transfer the desired weight change to a conductance change, i.e. $\Delta W \rightarrow \Delta G$, considering PCM non-idealities.

Our multi-memristor implementation first estimates the number of pulses required to match the desired conductance change, by assuming each SET pulse increases the conductance linearly by 0.75 $\mu S$ as the model outlined in Section 2.1 suggests (a more realistic approximation of the number of pulses is available in [29]). Then these SET pulses are applied sequentially among $N$ PCM devices in a circular queue. The refresh is applied if any of the memristor pair conductances is higher than 9 $\mu S$ and their difference is less than 4.5 $\mu S$.

**Mixed-precision Update.** One solution to close the gap between the update resolution requested by the LB and the minimum programmable conductance change of PCMs is to accumulate the updates on a high-precision co-processor until they become reliably transferable to PCMs [58]. Notably, this scheme also corresponds to the quantization-aware training techniques conventionally used for the training of quantized artificial neural networks [67].

In our simulations, the LB accumulates the gradients in a double-precision floating memory until they are an integer multiple of PCM update granularity (corresponding to 0.75 $\mu S$). Then they are converted to a number of pulses and applied to the memristors. The refresh is applied if either one of the memristor pair conductances is higher than 9 $\mu S$ and their difference is less than 4.5 $\mu S$.

3 **Training a Spiking RNN on a PCM Crossbar Simulation Framework**

We used the model of the PCM crossbar array to determine realistic values of the network parameters $\{W_{\text{inp}}^{ji}, W_{\text{rec}}^{ji}, W_{\text{out}}^{kj}\}$. In order to represent synaptic weights, $W \in [-1, 1]$, with the conductance values of PCM devices, $G \in [0.1, 12] \mu S$ [29], we used the linear relationship $W = \beta [\sum N G^+ - \sum N G^-]$, where $\sum N G^+$ and $\sum N G^-$ are the total conductance of $N$ memristors representing the potentiation and the depression of the synapse respectively [29]. At this stage, the forward computation (inference) of Eq. 1 is simulated using the PCM crossbar simulation framework that includes the effects of READ noise and temporal conductance drift.

The weight updates calculated by the e-prop algorithm are applied to the PCM-based crossbar arrays using each of the methods described in Section 2.3.

\[^2N = 1\] for all weight update methods, except when the multi-memristor update is being used.
Table 1: Performance evaluation of spiking RNNs with models of PCM crossbar arrays.

| Method            | Sign-gradient | Stochastic | Multi-mem (N=4) | Multi-mem (N=8) | Mixed-precision |
|-------------------|---------------|------------|-----------------|-----------------|-----------------|
| MSE Loss          | 0.2080        | 0.1808     | 0.1875          | 0.1645          | 0.0380          |

4 Results

We validated the network using a classical one-dimensional continuous pattern generation task relevant for many domains including motor control or value function estimation in RL[47]. The training dataset is the slightly modified version of the one-second-long patterns described in [30] (see Methods for task and training details).

Table 1 summarizes the training performances of spiking RNNs utilizing different weight update methods on PCM crossbar arrays to realize the target weight change calculated by the e-prop algorithm. Out of five configurations, only the mixed-precision approach resulted in an acceptable performance on the pattern generation task (MSE loss < 0.1, see Section 8 for the evaluation). Figure 4 demonstrates extremely sparse spiking activity of about 3.3 Hz in the recurrent layer (see Fig. 14 for mean firing rate evolution during the training), nevertheless the network is able to generate the target patterns well despite PCM non-idealities.

![Figure 4: Dynamics of a network trained with the mixed-precision algorithm. The raster plot (top) shows the sparse spiking activity of recurrent-layer neurons. The training loss (bottom left) demonstrates MSE loss over 250 epochs is averaged over ten best network hyperparameters (see Fig 15 for the best performing hyperparameter). Properly-tuned neuronal time constants and trained network weights result in generated patterns following the targets (bottom right). The generated patterns are extracted from three different spiking RNNs.](image-url)
We also observed that, with our training settings, the weight saturation problem due to the differential configuration does not occur often and only a few devices (< 1%, as shown in Fig 5 (right)) are required to be refreshed. This is partially because the total number of WRITE pulses applied during the training is very low, i.e. only \( \sim 12 \) WRITE pulses are applied per epoch, as shown in Fig. 6. Thanks to the mixed-precision algorithm, only large-enough accumulated gradients lead to the generation of WRITE pulses. Fig. 5 (left) demonstrates the effective weight distribution of the PCM synapses at the end of the training.

To simulate an ideal device model, we disabled all noise and drift effects in the simulation framework (see Supplementary Note 2). We kept a limited weight resolution of 4-bit, an optimistic but achievable target for PCM devices [28]. This ideal PCM model is therefore equivalent to a digital 4-bit memory. Table 2 summarizes the performances of networks utilizing different memristor-aware weight update methods with this ideal model. The results show that the stochastic updates, the multi-memristor updates with \( N = 8 \), and the mixed-precision updates can solve the pattern generation task. Similarly to the realistic device model results in Table 1, the mixed-precision method achieved the best accuracy. Unsurprisingly, all methods performed better in the absence of the previously discussed PCM non-idealities. One remark is that stochastic updates allow for a better performance than both multi-memristor methods, indicating the necessity of having a low number of stochastic updates when the network is trained with the quantized weights.

Moreover, to further evaluate the effect of limited bit precision on the network performance, we trained the same network with e-prop using standard FP32 (single-precision floating point) weights. With the high resolution of the FP32 training, we achieved an mean squared error (MSE) loss of 0.0215, which is comparable to mixed-precision training using either ideal quantized memory or PCM cell model.
Table 2: Performance evaluation of spiking RNNs with an ideal crossbar array model

| Method               | Sign-gradient | Stochastic | Multi-mem (N=4) | Multi-mem (N=8) | Mixed-precision |
|----------------------|---------------|------------|-----------------|-----------------|-----------------|
| MSE Loss             | 0.1021        | 0.0758     | 0.1248          | 0.0850          | 0.0289          |

Similar to [29], we observed that probability scaling factor \( p \) in the stochastic update method allows the tuning of how many number of devices are being programmed during the training. Figure 7 demonstrates that with the increase of \( p \) (decreasing update probability), the number of WRITE pulses applied to PCM devices can be decreased up to one order of magnitude without degrading the loss.

![Number of WRITE pulses applied to recurrent layer and Loss vs. Probability scaling factor](image)

Figure 7: The stochastic update method enables tuning the number of WRITE pulses to be applied to PCM devices.

5 Discussion

On-chip training of spiking RNNs enables the low-power deployment of the intelligent computing systems at the edge with learning and adaptation capabilities [68, 69]. In this work, we evaluated four widely used memristor update mechanisms on spiking RNNs based on the ideal gradient information calculated by the e-prop learning rule. Crossbar architectures with memristive devices intrinsically support the sparse, event-driven, and asynchronous processing of spike flow through in-memory computing, reducing the dynamic power consumption and shrinking the memory area. Implementing learning on-chip imposes both space and time locality constraints in recurrent architectures, which can be met by the e-prop learning rule, for example. By doing extensive hyperparameter exploration, we investigated the performances of weight update mechanisms despite various PCM non-idealities on a second-long pattern-generation task. Solving the pattern generation task demonstrates the recurrent network’s ability to preserve task-relevant information in its activation dynamics for at least one second period. Such ability is required for applications processing temporal inputs such as keyword detection, motor control, and bio-signal processing.

Among the mechanisms we studied, the mixed-precision update leads to the best accuracy. This is because accumulating instantaneous gradients on high-precision enables the use of a low learning rate, making the ideal weight update magnitude comparable to minimum programmable PCM conductance change, resulting in an improved convergence of the network. Mixed-precision hardware resembles the concept of the cascade memory model in neuroscience, where complex synapses hold a hidden state variable which only becomes visible after hitting a threshold [70]. This meta-plastic model has recently been used for solving catastrophic forgetting in some benchmarks [71]. However, the mixed-precision scheme comes at the cost of having a high-precision memory that accumulates the updates. This has previously been done by introducing a co-processor next to the crossbar memristor array [58]. Yet, accumulating the gradients allows reliable PCM programming, reducing the number of programming devices and speeds up the learning. Therefore the synergy between memristor-based

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3Multi-memristor configurations are implemented assuming a 4-bit resolution per memory cell. Hence \( N = 4 \) and \( N = 8 \) is equal to having 7-bit and 8-bit resolutions digital weights per synapse, respectively.
synapses and learning rules that intrinsically allows the accumulation of gradients, e.g., e-prop, is remarkable and worth exploring.

One of the key levers to increase the learning performance is the memory resolution, which comes in line with the mixed-precision learning study of [58]. However, this comes at the price of increasing the synapse size by increasing the number of devices. One solution to this problem is to employ binary synapses with a stochastic rounding update scheme [72]. Introducing stochasticity reduces the learning rate and, in expectation, moves the weight parameters to the optimal binary value. Stochastic rounding approaches have already been employed successfully not only in memristive devices but also in fully-digital designs to apply low learning rate values to quantized weights [73, 74]. It has also been shown that the intrinsic cycle-to-cycle variability of memristive devices can implement stochastic updates in an area-efficient manner [19].

To the best of our knowledge, there is no report yet on the online training of spiking RNN with e-prop learning rule based on realistic PCM synapse models. Our work compares several previously developed methods that are designed to cope with memristor non-idealities and demonstrates that accumulating gradients allows more reliable programming of PCM devices, reduces the number of programming devices and outperforms other synaptic weight-update mechanisms. Future work will need to evaluate the impacts of the implemented weight update schemes using more extensive datasets for a more interpretable benchmarking, further incorporate the PCM devices for emulating temporal dynamics such as eligibility traces [27], as well as exploring other learning rules such as OSTL or Real Time Recurrent Learning (RTRL) [75].

6 Methods

For the chosen pattern generation task, the network consists of 100 input and 100 recurrent LIF neurons, and one leaky-integrator output unit. The network receives a fixed-rate Poisson input, and the target pattern is a one-second-long sequence defined as the sum of four sinusoids (1 Hz, 2 Hz, 3 Hz and 5 Hz), whose phases and amplitudes are randomly sampled from uniform distributions [0, 2π] and [0, 5], respectively. Throughout the training, all layer weights \( W_{ji}^{in}, W_{ji}^{rec} \) and \( W_{kj}^{out} \), are kept plastic and the device conductances are clipped between 0.1 and 12 \( \mu S \). This benchmark is adapted from [76].

We trained \( \sim 1000 \) different spiking RNNs for each of the weight update methods described in Section 2.3. Each network shares the same architecture, except for their synapse implementations, some of their hyperparameters and weight initialization. Because each weight update method requires a few specific additional hyperparameters and may considerably affect the network dynamics, we tuned the network hyperparameters for each of the update methods using Bayesian optimization [77]. Based on network performances over 250 epochs of the pattern generation task, we selected the best performing network hyperparameters out of 1000 candidates. By doing so, we evaluated how well different weight update methods can reflect the ideal weight update calculated by the e-prop learning rule on a PCM substrate.

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8 Supplementary

Supplementary Note 1

We implemented the PCM crossbar array simulation framework in PyTorch [40], which can be used for both the inference and the training of Artificial Neural Networks (ANNs) or SNNs. Built on top of the statistical model introduced by Nandakumar et al. [29], our crossbar model supports asynchronous SET, RESET and READ operations over entire crossbar structures and simultaneously keep tracks of the temporal evolution of device conductances.

A single crossbar array consists of \( P \times Q \) nodes (each node representing a synapse), where single node has \( 2N \) memristors arranged using the differential architecture (\( N \) potentiation, \( N \) depression devices). Each memristor state is represented by four variables, \( t_p \) for storing the last time the device is written (which is used to calculate the effect of the drift), \( count \) for counting how many times it has written (to be used later in the arbiter of N-memristor architectures), \( P_{mem} \) for its programming history (required by the PCM model) and \( G \) for representing the conductance of the device at \( T_0 \) seconds later after the last programming time. The initial conductances of PCM devices in the crossbar array are assumed to be iteratively programmed to High-Resistive State (HRS), sampled from a Normal distribution \( N(\mu = 0.1, \sigma = 0.01) \mu S \).

The PCM crossbar simulation framework supports three major functions: READ, SET and RESET. The READ function takes the pulse time of the applied READ pulse, \( t \), and calculates the effect of drift based on the last programming time \( t_p \). Then, it adds the conductance-dependent READ noise and returns the conductance values of whole array. The SET function takes the timing information of the applied SET pulse, together with a mask of shape \( (2 \times N \times P \times Q) \) and calculates the effect of the application of a single SET pulse on the PCM devices that are selected with the mask. Finally, the RESET function initializes all the state variables of devices selected with a mask and initializes the conductances using a Normal distribution \( N(\mu = 0.1, \sigma = 0.01) \mu S \).

Supplementary Note 2

READ and WRITE operations to simulated PCM devices in the crossbar model are stochastic and subject to the temporal conductance drift. Additionally, PCM devices offer a very limited bit precision. Therefore, to ease the network training procedure, especially the hyperparameter tuning, we developed the perf-mode. When crossbar model is operated in perf-mode, all stochasticity sources and the conductance drift are disabled. READ operations directly access the device conductance without \( 1/f \) noise and drift, whereas SET operations increase the device conductance as

\[
G_N = G_{N-1} + \frac{G_{MAX}}{2CB_{RES}},
\]

where, \( G_{MAX} \) is the maximum PCM conductance set to 12 \( \mu S \) (conductivity boundaries are determined based on the device measurements from [29]), and \( CB_{RES} \) is the desired bit-resolution of a single PCM device. In a nutshell, the perf-mode turns PCMs into an ideal memory cells corresponding to a digital memory with a limited bit precision.
Supplementary Note 3

Here, we demonstrate the impact of using multiple memristor devices per synapse (arranged in differential configuration) on the precision of targeted programming updates. Specifically, we modeled synapses with $N = 1, 4, 8$ PCM devices and programmed them from initial conditions of integer conductance values $G_{\text{source}} \in \{-10, 10\} \, \mu \text{S}$ to integer conductance values $G_{\text{target}} \in \{-10, 10\} \, \mu \text{S}$ using the multi-memristor update scheme described in Section 2.3. The effective conductance of a synapse is calculated by $G_{\text{syn}} = \sum_{i=0}^{N} G^+_i - \sum_{i=0}^{N} G^-_i$, however we normalized the conductance across 1-PCM, 4-PCM and 8-PCM architectures for an easier comparison, such that $G_{\text{syn}} = \frac{1}{N} \left( \sum_{i=0}^{N} G^+_i - \sum_{i=0}^{N} G^-_i \right)$.

Our empirical results verifies the claim of Boybat et al. [57] that the standard deviation and the update resolution of the write process decreases by $\sqrt{N}$. 

Figure 8: The PCM crossbar model supports both the full PCM model from [29] and its corresponding simplified version as an ideal digital memory in perf-mode.
Figure 9: Multi-memristor configuration with 1 PCM (one depression and one potentiation) per synapse
Figure 10: Multi-memristor configuration with 8 PCM (four depression and four potentiation) per synapse
Figure 11: Multi-memristor configuration with 16 PCM (eight depression and eight potentiation) per synapse
Supplementary Note 4

In the differential architectures, consecutive SET pulses applied to positive and negative memristors may cause the saturation of the synaptic conductance and block further updates. The saturation effect is more apparent when a single synapse gets 10+ updates in one direction (potentiation or depression) during the training. For example, this effect is clearly visible in Fig. 9, Fig. 10 and Fig. 11, when the source conductance and target conductances differ by more than 8-10 $\mu$S.

We implemented a weight update scheme denoted as the update-ready criterion, which aims to prevent conductance saturation while applying single large updates. Before doing the update, we read both positive and negative pair conductances, and check if the target update is possible. If not, we reset both devices, calculate the new target and apply the number of pulses accordingly. For example, given $G^+ = 8 \mu$S and $G^- = 4 \mu$S and the targeted update $+6 \mu$S, the algorithm decides to reset both devices because $G^+$ can’t be increased up to $14 \mu$S. After both devices are reset, $G^+$ can be programmed to $11(\mu$S). Although our PCM crossbar array simulation framework supports it, this weight transfer criterion is not used in our simulations because it requires reading the device states during the update.

Figure 12: Update-ready criterion tested with $N = 1$ memristor per synapse.
Supplementary Note 5

We have defined the task success criteria as MSE Loss < 0.1 based on visual inspection. Below in Fig 13, some network performances are shown.

![Figure 13: Comparison of network performances with six different loss values.](image)

Supplementary Note 6

![Figure 14: Mean firing rate of 50 networks with PCM synapses trained using the mixed-precision method.](image)
Figure 15: MSE loss of 50 networks trained with PCM synapses using the mixed-precision method.