Investigation of Ta$_2$O$_5$ as an alternative high $\kappa$ dielectric for InAlN/GaN MOS HEMT on Si

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Abstract - We report on the demonstration and investigation of Ta$_2$O$_5$ as high-$\kappa$ dielectric for InAlN/GaN-MOS HEMT-on-Si. Ta$_2$O$_5$ of thickness 24 nm and dielectric constant \textasciitilde 30 was sputter deposited on InAlN/GaN HEMT and was investigated for different post deposition anneal conditions (PDA). The gate leakage was 16nA/mm at -15 V which was \textasciitilde 5 orders of magnitude lower compared to reference HEMT. The 2-dimensional electron gas (2DEG) density was found to vary with annealing temperature suggesting the presence of net charge at the Ta$_2$O$_5$/InAlN interface. Dispersion in the capacitance-voltage (C-V) characteristics was used to estimate the frequency-dependent interface charge while energy band diagrams under flat band conditions were investigated to estimate fixed charge. The optimum anneal condition was found to be 500° C which has resulted into a flat band voltage spread ($\Delta V_{FB}$) of 0.4 V and interface fix charge ($Q_f$) of $3.98 \times 10^{11}$ cm$^{-2}$. XPS (X-ray photoelectron spectroscopy) spectra of as deposited and annealed Ta$_2$O$_5$ film were analyzed for Ta and O compositions in the film. The sample annealed at 500° C has shown Ta:O ratio of 0.41. XRD (X-ray diffraction) analysis was done to check the evolution of poly-crystallization of the Ta$_2$O$_5$ film at higher annealing temperatures.

Index Terms—2-dimensional electron gas (2DEG), High Electron Mobility Transistor (HEMT), Ta$_2$O$_5$, High $\kappa$, capacitance voltage (C-V)

I. INTRODUCTION

II-Nitride HEMTs have been investigated for over two decades for their high frequency and high power applications [1]. There is an increasing market penetration of GaN HEMTs for power amplification and power conversion applications including those in mobile base stations, SATCOM/TV, radars, converters/inverters for a wide range of power systems and motor drives. Although AlGaN/GaN HEMTs with 20-30 nm barrier are more widely studied devices including the ones used in the commercial sector, InAlN/GaN and AlN/GaN HEMTs offer several advantages such as very high 2DEG density leading to higher current and ultra-thin barrier leading to higher transconductance ($g_m$) and $f_{T}$ [2][3][4][5][6]. These thinner barrier devices suffer from higher gate leakage current which necessitates the use of a gate dielectric at the expense of $g_m$. Lattice matched [7] In$_{0.17}$Al$_{0.83}$N/GaN grown on GaN is relatively stress free. High $\kappa$ dielectric materials such as Al$_2$O$_3$, HfO$_2$ etc were used to reduce the leakage keeping the thickness as low as possible. High power switching applications necessitates very low leakage current and hence use of thicker dielectric with very high-k such as Ta$_2$O$_5$ ($\epsilon = 20$ to 50) [8] can offer a significant advantage. Although Ta$_2$O$_5$ as gate dielectric has been reported AlN/GaN HEMTs [9], Ta$_2$O$_5$/InAlN/GaN HEMT is not yet reported. In this letter, we report on the fabrication and characterization of Ta$_2$O$_5$/InAlN/GaN MOS-HEMT with I$_{DS}$/I$_{OFF}$ ratio >10$^8$ and investigate the Ta$_2$O$_5$/InAlN interface through C-V and band diagram analysis. The material properties of as-deposited and annealed film were investigated using XPS and XRD.

II. EXPERIMENTAL DETAILS

![Figure 1](image-url)

Figure 1 (A) and Fig. 1 (B) shows the epistack with the schematic of HEMT and MOS-HEMT (C) optical microscope image of circular Schottky C-V pad.

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subjected to a post metal anneal (PMA) in forming gas ambiance at 400°C for 5 min. Source-drain contacts were exposed by selectively etching Ta2O5 in buffered hydrofluoric (BHF) acid solution. The gate length for transistors was 3 µm while the gate-source and gate-drain spacing were 3 µm and 15 µm respectively. Capacitance voltage (C-V) characteristics were measured on circular Schottky C-V pads (Fig. 1 (C)) of radius 90 µm.

III. RESULTS AND DISCUSSIONS

DC current voltage (I-V) and C-V measurements were performed to characterize the Ta2O5 as a dielectric for MOS-HEMT. From transfer length measurements for the sample without oxide, contact resistance (Rc) and sheet resistance (Rsh) were found to be 0.35 Ω-mm and 241 ohm/□ respectively. Gate drain leakage was found to be relatively high ~ 2.6 mA/mm (VG=-15 V) for the control sample (without oxide) (Fig. 2) which is expected of thinner barrier HEMTs. It can be seen from Fig. 2 that the use of Ta2O5 as gate dielectric led to a reduction of the gate leakage by 5 orders of magnitude (2.6 mA/mm to 16nA/mm, at 15 V) for PDA conditions 500°C and 600°C. High temperature anneal results in poly crystallization of Ta2O5 film and the main reason behind increased gate leakage compared to 500°C annealed samples. The poly-crystallization of Ta2O5 at higher annealing temperatures has been confirmed using XRD which is discussed later. The grain boundaries in the polycrystalline film serve as current leakage path [11].

Fig. 2. Gate-Drain leakage current of HEMT and MOS-HEMT (Lgs=3 µm, Lg=3 µm, Lgd=15 µm) with different PDA conditions.

The devices were further analyzed for DC steady state current characteristics. Transfer characteristic (ID-VGS) and output characteristics (ID-VDS) are shown in the Fig. 3 and Fig. 4 respectively. The zero-bias saturation current (for VG>Vknee and VG=0 V) was found to be between 500-700 mA/mm while the pinch-off was found to be between -6 to -11 V for all the samples indicating a variation of 2DEG density with PDA conditions. Different annealing conditions results in different interface-states/charges at oxide-nitride interface [12] which leads to modification of net 2DEG of the device. The shift in the pinch-off voltage towards more (less) negative voltage is a result of net decrease (increase) of negative charges at the Ta2O5/InAlN interface (Fig. 3). Sample with PDA condition of 500°C exhibited the highest On/Off ratio > 10^7 with a VTH of -9.7 V which is comparable to those reported for MOS-HEMTs elsewhere [13][14]. Due to variation in VTH of the devices, Ion/Ioff ratios were calculated using Ion-VDS characteristics (Fig. 4) at gate voltage overdrive (VG-VTH) of 6 V and the Ion/Ioff ratios were > 10^7, 10^5 and 10^6 for the samples annealed at 500°C, 600°C, and 700°C respectively.

Fig. 3. Drain current and Gate current of HEMT and MOS-HEMT (Lgs=3 µm, Lg=3 µm, Lgd=15 µm) with different PDA conditions.

Fig. 4. DC Ids-Vgs characteristics of HEMT and MOS-HEMT (Lgs=3 µm, Lg=3 µm, Lgd=15 µm) with different PDA conditions. (A) HEMT, (B) MOS-HEMT with PDA 500°C, (C) MOS-HEMT with PDA 600°C, (D) MOS-HEMT with PDA 700°C.
Capacitance voltage (C-V) characteristics of MOS HEMTs and HEMT are shown in Fig. 5 and inset to the Fig. 5 respectively. These measurements were performed on circular Schottky pads. $V_{TH}$ variation in C-V was observed for the samples analogous to that observed for $I_D$/$V_{GS}$. Parameters summarizing the C-V results for both HEMT and MOS-HEMT are listed Table I. The zero-bias capacitance ($C_T$) of MOS-HEMT can be expressed as: $C_T = (C_{0x} + C_{bar})/(C_{0x} + C_{bar})$, where, $C_{0x}$ and $C_{bar}$ are capacitances related to $Ta_2O_5$ and InAlN respectively. Using the zero-bias capacitance of HEMT (617 nF/cm$^2$) and the net barrier thickness (11 nm, InAlN+AlN), the relative dielectric constant ($\varepsilon_r=7.65$) of the InAlN barrier was calculated. Then, the $C$ of $Ta_2O_5$ was estimated using MOS-HEMT and HEMT zero bias capacitances and the estimated values are listed in the Table I. Some uncertainty in the determination of dielectric constant creeps in due to possible errors in the estimation of thicknesses of both InAlN barrier and $Ta_2O_5$ (growth and deposition related un uniformity). However, no significant change (±0.5 nm) in oxide thickness of the $Ta_2O_5$ on Si (calibration sample) has been observed after post annealing. The calculated threshold voltage ($V_{TH}$=qn/C$_s$, $n_s=2.0\times10^{13}$ cm$^{-2}$) is 2DEG density and $C_T$ is total capacitance considering oxide ($Ta_2O_5$=24 nm) and barrier contributions (InAlN=11nm) for MOS HEMT are tabulated in Table I. This calculated $V_{TH}$ for MOS-HEMT was found to not be in agreement with the experimental $V_{TH}$ (x-axis intercept of the slope line drawn on C-V data) observations. The deviation of experimental $V_{TH}$ from calculated $V_{TH}$ suggests the presence/modulation of charges at $Ta_2O_5$/InAlN interface under different annealing conditions.

![Fig. 5. Capacitance voltage characteristics of HEMT (inset) and MOS-HEMT at different frequencies. Measurements were performed on circular Schottky C-V pads.](image)

Using the above equations (1-3), the fixed charges ($Q_f$) at the InAlN/$Ta_2O_5$ interface for the three samples were estimated as shown in Table I. The fixed charge estimated for the sample (PDA 500$^\circ$C) was $3.98\times10^{13}$ cm$^{-2}$ which compares well with that reported elsewhere ($1.6\times10^{13}$ cm$^{-2}$) [20][21][22] for $AlO_2$/AlN, $Al_2O_3$/GaN and $SiN$/InAlN. The increase in 2DEG density with increase in the positive interface charge has also been reported previously [21]. The PDA condition dependent fixed charges at $Ta_2O_5$/InAlN interface were calculated by considering constant conduction band offset at this interface. However, the dipole formation at the interfaces in the presence of fixed charges can change the band offsets [23]. Different characterization techniques would need to be
investigated to estimate the band offset variations with charges.

Two step C-V characteristics have been widely used to characterize dielectric/barrier and barrier/channel interfaces of MOS HEMTs. Using the conductance method, the G/ω versus frequency characteristics near VTH and near second slope in C-V (for Vc>0 V) were used to estimate the trap densities at barrier/channel and dielectric/barrier interfaces respectively [24][25][26]. The band alignment between widely reported barrier (Al0.25Ga0.75N) and dielectrics (Al2O3, SiO2, HfO2) supports the electron blocking at dielectric/barrier interface. In forward bias condition (Vc>0 V), the electrons get transferred from barrier/channel interface to the dielectric/barrier interface. These electrons neutralize the donor traps and make the acceptor type traps negatively charged as a result the second slope in C-V is observed for Vc > 0 V [24]. Here in this case, the band alignment (Fig. 6) of Ta2O5/InAlN doesn't support electron blocking for positive gate bias due to this reason the conventional conductance method was not employed for trap characterization. As the conduction band offset of Ta2O5/InAlN does not support electron blocking at this interface, Al2O3/Ta2O5 stack on InAlN may be employed to block electrons and the Ta2O5/InAlN interface can be characterized using the conventional conductance method.

Due to these restrictions, C-V measurements (Fig. 5) at various frequencies and the spread in C-V characteristics should be employed for characterizing frequency dependent properties of dielectric and interfaces. The HEMT C-V characteristics show very less spread (difference of flat band voltages (∆VFB) at 10 kHz and 1 MHz was 0.15 V). This negligible spread in C-V characteristics (Fig.5) is an indication of good interface between InAlN barrier and GaN channel. The relatively higher spread in frequency-dependent capacitances of MOS-HEMTs could be attributed to the interface state present at Ta2O5/InAlN interface or in Ta2O5. A measure of spread in C-V characteristics can be defined as the difference in flat band voltages at 10 kHz and 1 MHz. This flat band voltage difference (∆VFB) for MOS HEMT and HEMT is shown in Table I. ∆VFB varies from 0.15 V to 0.8 V for HEMT and MOS HEMT (PDA 700° C) respectively. The least value of ∆VFB observed for MOS HEMT (PDA 500° C) was 0.4 V.

Figure 7 shows the XRD 20 scan of the Ta2O5 films (as deposited and annealed under different conditions) on HEMT. The absence of any Bragg reflection in the as-deposited film confirms its amorphous nature. When Ta2O5 films were subjected to rapid thermal annealing in forming gas at 500° C, 600° C, 700° C for 1 min, 20 scans started to show humps at 20 positions of 28° and 35° (Fig. 7 (B, C, D)). Similar results have been observed in extended X-ray absorption florescence spectroscopic (EXAFS) studies [27]. In-order to confirm that Ta2O5 films were in process of crystallization, one sample was annealed at 700° C for 10 mins (the 20 scan is shown Fig. 7(E)). The Bragg reflections from the planes can be indexed as (003), (200), (203), (006), (220) of α-Ta2O5 (hexagonal) (PDF-00-018-1304). The poly crystallization of Ta2O5 films was confirmed by XRD for the samples annealed at higher temperatures (~700° C) and it is in agreement with previous report [28].

![XRD 20 scans of Ta2O5 films](image)

Table 1: C-V characteristics for different PDA conditions

| PDA Conditions | VFB (V) @ 500 kHz | ∆VFB (10 kHz to 1 MHz) | Qi (2cm^-2) for Delta E=0.52 eV |
|---------------|------------------|------------------------|-------------------------------|
| MOS-HEMT, 500° C | -9.2 | 2.3x10^11 | 34.5 | 8.5 | 0.4 V | 3.98x10^13 |
| MOS-HEMT, 600° C | -11.3 | 2.64x10^11 | 26.3 | 9.3 | -12.6 | 0.6 V | 4.74x10^13 |
| MOs HEMT, 700° C | -6.1 | 1.45x10^11 | 29.2 | 8.9 | -6.6 | 0.8 V | 1.56x10^13 |
| HEMT | -5.95 | 2.2x10^13 | -- | -- | -6.8 | 0.15 V | -- |
Figure 8 shows the XPS spectrum of O (1s) and Ta (4f) for different anneal conditions. The XPS spectra were calibrated using C 1s peak position (284.6 eV). The thickness of the Ta$_2$O$_5$ film used for XPS was 9 nm. Ta-O binding energy of Ta$_2$O$_5$ is characterized by the doublets (peaks corresponding to 4f$_{5/2}$ and 4f$_{7/2}$) observed in the Ta 4f spectra and these peaks have a separation of 1.89 eV [29]. The peak of XPS spectra shifts by ~0.47 eV (towards higher binding energy) for 500°C annealed sample compared to as-deposited sample. The peak shifts were 0.35 eV and 0.40 eV for 600°C and 700°C annealed samples respectively. The shift of the peaks with different anneal conditions were used to quantify the Ta$_2$O$_5$, a fully oxidized film corresponds to higher binding energy peak and a partial oxidation corresponds to lower binding energy [30]. The Ta$_2$O$_5$ film was further analyzed for atomic compositions of Ta and O by analyzing the Ta and O spectra. The ratio of Ta:O in Ta$_2$O$_5$ is 0.4 (2/5) for the ideal film and this ratio was found to be 0.64 for as deposited film. After the FGA, the ratio has changed to 0.41, 0.43 and 0.52 for 500°C, 600°C and 700°C annealed samples respectively. 500°C annealing condition has resulted in better stochiometric film (close to ideal Ta:O ratio) while 600°C and 700°C annealed films have become oxygen deficient (Ta rich). XPS spectra of Ta was dominated with Ta$^{5+}$ state in all the samples [31][32].

The O (1s) spectra were mostly clean for all the samples with surface contamination signatures (~532 eV) [31].

IV. CONCLUSIONS

We have demonstrated Ta$_2$O$_5$/InAlN/GaN MOS HEMT on Si. The dielectric constant of Ta$_2$O$_5$ was found to be ~30. Different anneal conditions were found to affect the net 2DEG density. Under different PDA conditions, fix charge at Ta$_2$O$_5$/InAlN interface and $\Delta V_{FB}$ were estimated. The measure of spread in C-V, $\Delta V_{FB}$ was found least for 500°C PDA sample. XPS spectra of the Ta$_2$O$_5$ film suggest the improvement in oxide quality for 500°C annealing and with higher annealing temperatures (600°C and 700°C) the oxide quality deteriorates. Annealing at higher temperature leads to poly crystallization of Ta$_2$O$_5$ as a result gate leakage current increases. The results presented here show the promise of using Ta$_2$O$_5$ as a very high $\kappa$ dielectric with dielectric/nitride interface of comparable quality to most of the reported dielectric/nitride interfaces. However, quantitative trap densities estimation and XPS analysis of Ta$_2$O$_5$/InAlN (Nitride) interface needs to be done to establish Ta$_2$O$_5$ as an alternative high $\kappa$ dielectric for nitride HEMTs.

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