Abstract—In this work, drain current $I_D$ for 5-nm gate length with dual-material (DM) double-surrounding gate (DSG) inversion mode (IM) and junctionless (JL) silicon nanotube (SiNT) MOSFET have been studied and simulation results are reported using Silvaco ATLAS 3D TCAD. For this work, we used the non-equilibrium Green’s function (NEGF) approach and self-consistent solution of Poisson’s equation with Schrödinger’s equation. The conduction band splitting into multiple sub-bands has been considered and there is no doping in channel in case of IM SiNT MOSFET. The effect of DM gate engineering for SiNT channel radius 1.5 nm with 0.8-nm gate oxide (SiO₂) thickness on $I_D$ has been studied. A comparison of results has been done between IM DM DSG and JL DM DSG SiNT. In case of JL, doping concentration is optimized for two concerns: (i) to get the same $I_{On}$ current as IM device and (ii) to get the same threshold voltage $V_{Th}$ as IM. This has resulted in $10^2$ and $10^3$ times smaller $I_{Off}$ in matching $I_{On}$ and $V_{Th}$, optimized device, respectively, as compared to IM. It is found that DM gate engineering reduces drain-induced barrier lowering (DIBL) for both IM and JL SiNT MOSFET. In this work, JL have much smaller DIBL ~15 mV/V, almost an ideal SS ~60 mV/dec, and higher $I_{On}/I_{Off}$ ratio ~2.18 × 10⁸ as compared to available CGAA literature results.

Keywords: inversion mode, junctionless, DM DSG, Si nanotube MOSFET, NEGF, $I_D$, SS, DIBL

1. INTRODUCTION

For better and faster performance, dimension of MOSFET is being continuously decreased. However, scaling of MOS device below 32-nm technology node faces serious SCEs. Hence conventional MOSFET is replaced with innovative device structures such as double-gate (DG), tri-gate (Fin-FET) and gate all around (GAA) [1, 2]. For 22-nm technology, FinFET was used by Intel in 2011 [3]. But for scaling below 10-nm node, GAA is best structure because of superior electrostatic control over channel charge, more immunity to short-channel effects (SCEs), and larger number of equivalent gates as compared to other structures [4]. One more problem in downsizing is creating abrupt (ultra-steep) and ultra-shallow junctions in CMOS. Key to this solution is by using a junction-less transistor (JLT) that doesn’t need $p$–$n$ junction between source-channel and drain-channel region, which is used in planar inversion mode (IM) MOSFET. In JLT, doping type and concentration from source, channel and drain region uniform. For $n$-channel MOSFET, doping is $N^+–N^+–N^+$ and for that of $p$-channel MOSFET is $P^+–P^+–P^+$. Hence, GAA silicon nanowire (SiNW) without junction is considered to be the promising device as a replacement of planar MOSFET. By using JLT, it is possible to get almost an ideal sub-threshold slope (SS) ~60 mV/decade, which has been obtained in this work. A junction-less NW results in [5–11].

(i) Elimination of requirement of abrupt junction.

(ii) Steeper sub-threshold slope.

(iii) Reduced SCEs.

(iv) Simplified fabrication process.

Tekleab et al. [12] propose a more advanced device structure that is Si nanotube (SiNT) field-effect transistor (FET). SiNT FET has even better control over SCEs as compared to GAA SiNW, due to SiNT device’s two surrounding gates (1st is inside the channel which is called inner gate and 2nd gate is outside the channel which is called outer gate) [11].

In JL FETs, doping concentration in all regions (source, channel, and drain) is $1 \times 10^{19}$ cm⁻³, which results in high source and drain series resistance. To minimize this series resistance, $1 \times 10^{19}$ cm⁻³ doping concentration is done in source and drain region.
which junction-less accumulation-mode (JAM) FETs normally do. For this, JAM FET requires an additional fabrication steps unlike JL FET, hence it does not offer a simpler fabrication process [13–15] as discussed earlier. To avoid this and for a reasonable comparison between IM and JL SiNT, n-type doping is optimized in JL for two concerns: (i) doping is done to get the same $I_{ON}$ as for IM, and (ii) doping is done to get the same $V_{TH}$ as for IM, with this we have also used dual-metal (DM) gate engineering, when the gate is made of two different metals having different work function.

We have considered two cases, each has 3 types of devices. For Case 1, low work function material (tantalum) has larger length, which is 4 nm, while the high work function material (tungsten) has length of 1 nm. For Case 2, both the gates have equal length (2.5 nm each).

For Case 1, doping in JL1 $I_{ON}$ and JL1 $V_{TH}$ devices are done with $4.2 \times 10^{19}$ and $3.4357 \times 10^{19}$ cm$^{-3}$, respectively. For Case 2, doping in JL2 $I_{ON}$ and JL2 $V_{TH}$ devices are done with $3.35 \times 10^{19}$ and $3.21 \times 10^{19}$ cm$^{-3}$, respectively. For IM SiNT, there is no doping in the channel region.

In this work, a novel device structure, dual-material double-surrounding gate (DM DSG) silicon nanotube (SiNT) has been used that shows a better performance than the available solutions. Various important parameters depend on the device structure, channel length, and gate material work function [17, 18]. In this work, drain current $I_D$ for 5-nm gate length DM DSG SiNT has been studied using Silvaco ATLAS 3D TCAD. SiO$_2$ is selected as the gate dielectric material because of its good interface with Si [19]. $I_D$ has been studied with dual-material (DM) gate engineering. Results are obtained with variation in length of both the gates.

2. MODELS USED IN SIMULATION

2.1. Non-Equilibrium Green’s Function

A mode space (MS) approach is used because a large computational time is required to solve a 2D or 3D problem. NEGF formalism in transport direction is coupled with Schrödinger equation in transverse plane. A Schrödinger equation is first solved in each slice of the device to find eigen energies and eigen-functions. Then, a transport equation of electrons moving in the sub-bands is solved. Because only a few lowest eigen sub-bands are occupied and the upper sub-bands are vacant, which can be safely neglected, hence the size of the problem is reduced [20].

3. RESULTS AND DISCUSSION

Figure 1 shows the device structure of 5-nm gate length DM DSG SiNT.

Tantalum (Ta) and tungsten (W) are selected as gate materials with vacuum work function 4.25 and 4.63 eV, respectively. But the metal gate is on SiO$_2$ dielectric, hence to take into account the interface dipole theory, Ta and W metal work functions are modified to their effective work function as [20]

$$H_0 = \frac{\hbar^2}{2m^*_e(r, z)} \left[ \frac{1}{m^*_e(r, z)} \frac{\partial}{\partial r} \left( \frac{1}{r} \frac{\partial}{\partial r} \right) + \frac{1}{m^*_e(r, z)} \frac{\partial}{\partial z} \frac{\partial}{\partial z} \right],$$

where $m^*_e(x, y)$ is a spatially dependent effective mass in the $Y$ direction for the $V_{TH}$ valley.

| Parameter used in this work | Values |
|-----------------------------|--------|
| Si channel radius, nm       | (3.3–1.8) = 1.5 |
| Si band gap, eV              | 1.12 [20, 23] |
| Si electron affinity, eV     | 4.05 [20, 23] |
| Si electron mass             | $m_0 = 0.916m_0$, $m_{11} = 0.191m_0$, $m_{12} = 0.191m_0$, $m_0 = 9.11 \times 10^{-31}$ kg [20, 23] |
| Si conduction band offset with SiO$_2$, eV | 3.2 [23] |
| SiO$_2$ thickness, nm       | 0.8 |
| Electron mass in SiO$_2$     | 0.30$m_0$ [23] |
| Source/Drain region, nm     | 3 |
| Source/drain N$^+$ doping, cm$^{-3}$ | $1 \times 10^{20}$ |
| Gate                        | Metal (Ta, W) |
| Gate length, nm             | 5 |
| Inner gate radius, nm       | 1 |
| Outer gate radius, nm       | 4.1 |
| $V_{DS}$ and $V_{GS}$, V    | 0.8 |

Table 1. Parameter used in this work

Figure 2 shows the $I_D$ vs. $V_{DS}$ curves of DM DSG for 0.8 nm SiO$_2$ thickness at $V_{GS} = 0.8$ V for both IM and JL DM DSG SiNT.

In Fig. 2, two cases are discussed, Case 1 and Case 2, also each case have separate three devices. JL1 $I_{ON}$ and IM1 SiNT have same $I_{On}$ but follow the different path. In the present work, smaller $I_{Off}$ has
been obtained in JL1\_I\_ON as compared to IM1 device. For JL1\_V\_TH device has the same V\_TH as IM1, there is reduction in I\_D of JL1\_I\_ON. About 10^{2} and 10^{3} times decrease in I\_OFF has been obtained in JL1\_I\_ON and JL1\_V\_TH SiNT, respectively, as compared to IM1 SINT MOSFET. Both JL1 curves are well saturated as...
compared to IM1. For Case 2 type, there is small difference for all the curves of three devices. In this case, JL2 \( I_{\text{ON}} \) and IM2 follow different path but have same \( I_{\text{On}} \). Also for JL2, \( I_D \) curve is well saturated as compare to IM2. In this case, we get the 10^3 times reduction in \( I_{\text{Off}} \) in both JL2 devices.

For a given \( V_{\text{GS}} \), with increase in \( V_{\text{DS}} \) there is significant increase in \( I_D \) for both IM and JL SiNT and with continued increase in \( V_{\text{DS}} \) beyond a value, SiNT MOSFET operate in saturation region where \( I_D \) is almost constant. In all JL SiNT MOSFETs, \( I_D \) curve is well saturated due to ideal SS and smaller DIBL as compared to IM as shown in Fig. 2. With increase in work function of the metal gate, for a given \( V_{\text{GS}} \) there is decrease in \( I_D \). It is clear that for Case 1, JL1 \( I_{\text{ON}} \) and IM1 have same \( I_{\text{On}} \) but former curve is well satu-

Fig. 2. \( I_D \) vs. \( V_{\text{DS}} \) curves of DM DSG SiNT with \( \text{SiO}_2 = 0.8 \text{ nm} \) at \( V_{\text{GS}} = 0.8 \text{ V} \) for both IM and JL.

Fig. 3. \( I_D \) vs. \( V_{\text{GS}} \) curves of DM DSG SiNT with \( \text{SiO}_2 = 0.8 \text{ nm} \) at \( V_{\text{DS}} = 0.8 \text{ V} \) for both IM and JL.
rated. For JL1 $V_{TH}$ type device has smaller $I_D$. While for Case 2 both JL are well saturated as compared to the IM2 case. And there is smaller difference in $I_D$ for all curves of Case 2.

Figure 3 shows the $I_D$ vs. $V_{GS}$ curves of DM gate with 0.8-nm SiO$_2$ thickness at $V_{DS} = 0.8$ V for both IM and JL DM DSG SiNT.

Continued increase in $V_{GS}$ more than threshold voltage results in increasing drain current. $I_D$ can be reduced by using metal gate having smaller work function (Fig. 3).

DM gate work function engineering in which smaller work function of Ta is used and called screen gate, which is near to drain. A high work function of metal gate W is used as the control gate, which is near to source.

With increase in screen gate length, due to smaller work function there is increase in drain current.
radius = 1.5 nm and length of SiO₂ = 0.8 nm, Ta = 4 nm, W = 1 nm (Case 1)

Table 2. Results of JL DM DSG SiNT with channel radius = 1.5 nm with length of SiO₂ = 0.8 nm, Ta = 4 nm, W = 1 nm (Case 1)

| Device | JLIₐₙ | Device IM1 | Device JLIₜh |
|--------|--------|-----------|-------------|
| Vₜh, V | 0.173864 | 0.200205 | 0.200205 |
| SS, mV/dec | 59.53 | 73.61 | 59.53 |
| DIBL, mV/V | 19.10 | 72.95 | 15.13 |
| Iₐₙ, A | 3.19 × 10⁻⁵ | 3.19 × 10⁻⁵ | 2.55 × 10⁻⁵ |
| Iₐ₉, A | 1.46 × 10⁻¹³ | 1.40 × 10⁻¹¹ | 2.53 × 10⁻¹⁴ |
| Iₐₙ/Iₐ₉ | 2.18 × 10⁸ | 2.28 × 10⁶ | 1.01 × 10⁹ |

Table 3. Results of JL DM DSG SiNT with channel radius = 1.5 nm and length of SiO₂ = 0.8 nm, Ta = 2.5 nm+, and W = 2.5 nm (Case 2)

| Device | JL2₁ₐₙ | Device IM2 | Device JL2₁ₜh |
|--------|--------|-----------|-------------|
| Vₜh, V | 0.274102 | 0.2758 | 0.2758 |
| SS, mV/dec | 59.53 | 73.03 | 59.53 |
| DIBL, mV/V | 21.95 | 82.70 | 21.95 |
| Iₐₙ, A | 1.35 × 10⁻⁵ | 1.35 × 10⁻⁵ | 1.31 × 10⁻⁵ |
| Iₐ₉, A | 4.60 × 10⁻¹⁶ | 1.20 × 10⁻¹³ | 3.9 × 10⁻¹⁶ |
| Iₐₙ/Iₐ₉ | 2.93 × 10¹⁰ | 1.12 × 10⁶ | 3.36 × 10¹⁰ |

This results in higher and smaller threshold voltage near the source and drain region, respectively; due to this, fast acceleration of electrons in the channel take place along with a screening effect to suppress SCEs due to step in the surface potential profile [24–26].

Smaller work function gate results in smaller DIBL, lower temperature at the drain end results in reduction of hot-electron effect, reduces the SCEs, gives higher electrons transport efficiency; due to this, there is increase in IOS as shown in Fig. 2 [27, 28].

Figures 4 and 5 show performance parameters such as DIBL, SS, and IOS/IOS ratio available in literature for various JL and IM, GAA and FinFET device.

In this work, for JL SiNT MOSFET we got much smaller DIBL ~15 mV/V, almost an ideal SS ~60 mV/dec and higher IOS/IOS ~2.18 × 10⁸ ratio.

Table 2 shows the result for various parameters of three separate different devices of IM and JL type.

From Table 2, in case of IM1, we get the highest IOS, highest SS, and the highest DIBL as Ta gate length is the higher and W gate length is the smaller. In case of JLIₐₙ, we get the smaller IOS current even with same IOS as IM and hence also increase in IOS/Iₐ₉ ratio also smaller DIBL as compared to IM1 device. With JLIₜh device we are getting the smallest DIBL, smallest IOS and highest IOS/Iₐ₉ ratio as compared to other two devices of Case 1 but at the cost of lower IOS as compared to other two devices of Case 1. Almost an ideal subthreshold slope ~60 mV/dec has been observed in all JL cases.

Explanation of all the results in Table 3 is similar to as Table 2.

Table 3 shows the results when control and screen gate have equal length which results in higher Vₜh, higher DIBL, much smaller IOS, and hence higher IOS/Iₐ₉ ratio as compared to Table 2 but at the reduced IOS. Also in Case 2, we get 10³ times reduction in IOS in both JL2 devices as compared to IM2.

For all the JL devices, we get much reduced DIBL and SS as compared to even JL FinFET [29]. Hence we conclude that JL DM DSG SiNT performance is better than IM DM DSG SiNW.

CONCLUSIONS

The effect of DM Engineering on IOS have been studied for IM and JL DM DSG SiNT MOSFET with gate length of 5 nm. We have observed two cases both having 3 device structures. In Case 1, IM1, highest IOS, highest SS, and the highest DIBL have been observed. In JLIₐₙ, smaller IOS is obtained even for the same IOS and in JLIₜh, we have smallest IOS and smallest ID in all the Case 1 JL1₁ₜh. In JLIₐₙ we got about 10² and 10³ time reduction in IOS. Case 2 is when both the gates have 2.5 nm length. For this, we observe increase in Vₜh, DIBL, IOS, and IOS/Iₐ₉ and decreases in IOS for all JL cases, almost an ideal ~60 mV/dec SS has been observed. In Case 2, we get 10³ times reduction in IOS in both JL2 devices as compared to IM2. In present work, JL SiNT MOSFET have much smaller DIBL ~15 mV/V, almost an ideal SS ~60 mV/dec, and higher IOS/Iₐ₉ ratio ~2.18 × 10⁸ as compared to literature results of CGAA structure.

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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