A broadband high efficiency monolithic power amplifier with GaAs HBT

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Abstract: A broadband single-stage power amplifier (PA) is presented in this paper. The proposed PA is designed and implemented using 2-µm GaAs HBT process to be targeted for wide range handset devices at operating frequency around 5 GHz. In this PA, mixed matching networks are designed with transmission lines (TLs) and lumped capacitors for bandwidth enhancement. In conjunction with feedback technology and diode-based bias circuit allow us to achieve the high efficiency and comparable linearity at a low supply voltage. Measured small signal flatten gain, maximum average output powers are all better than 10 dB and 22.5 ± 0.5 dBm over 4.2–5.8 GHz (32%), respectively. The prototype achieves a peak power-added efficiency (PAE) of 47.2% at 5 GHz, and the third-order intermodulation distortion (IMD3) performance below −38 dBc up to saturation power of 23.2 dBm. This work has potential for wideband high efficiency Doherty PA (DPA) used in future mobile communication system.

Keywords: gallium arsenide, transmission lines, wideband, MMICs, power amplifiers, feedback

Classification: Integrated circuits

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1 Introduction

In fourth-generation (4G) even more advanced fifth-generation (5G) wireless mobile communication systems, information content drastically increases, the need for high data rates transmissions results in an rising demand for higher frequencies, wider bandwidth, and lower power consumption for efficient use of precious spectrum [1]. Power amplifier, as one of most critical front module in transmitter, consumes significant part of total power. Particularly, broadband high efficiency PA is desirable for multi-band radio terminals used in future applications. Therefore, it is crucial to improve power efficiency over a broadband frequency range. In 4G systems, the envelope-tracking (ET) is used for efficiency enhancement, but the bandwidth is significantly limited by efficiency [2]. Recent reports [3] in this field show that the DPA architecture is considering as a good candidate for next generation wireless communication systems, however, the bandwidth limitation of DPA has also been documented [4, 5].
DPA consists of both a class AB (carrier) and a class C (peaking) power stages, respectively. The carrier amplifier is combined with peaking amplifier in order to achieve high back-off efficiency [6]. Since overall bandwidth and efficiency both depend on the relevant level achievable by these two amplifiers, thus DPA can be improved if the efficiency and bandwidth of these amplifiers can be properly improved. For this purpose, this paper presents the design and experimental results of a broadband high efficiency class-AB PA at a low supply voltage using mixed matching networks and negative feedback methods. The transmission lines and capacitors in matching network are designed to achieve an optimal impedance for proper bandwidth. In addition, feedback part consists of resistors and capacitors which connect the collector and base of power transistor for flatten gain and efficiency improvement. This work detailed the design and measurements of a broadband high efficiency GaAs HBT MMIC PA in the C-band for future small size Doherty PA in handsets applications.

2 Broadband class-AB PA design

2.1 Circuit topology

The proposed PA is designed using 2-µm GaAs HBT process provided by Sanan Corporation. Selected transistors in this work all have 2 µm width, 20 µm length and 4 fingers emitter-base junction, when biased at \( V_{CE} = 2.4 \) V, it exhibits a maximum oscillation frequency \( (f_{max}) \) of 80.8 GHz and a current-gain cut-off frequency \( (f_T) \) of 26.7 GHz. In order to obtain higher output power, three transistors are paralleled as a super transistor. Moreover, there are two Au interconnect planes, metal1 (M1) and metal2 (M2) of 1 µm and 4 µm thicknesses, respectively, where M2 is used as transmission lines due to lower loss from measurement results. In addition, the metal-insulator-metal (MIM) capacitor has a unit capacitance of 686 pF/mm\(^2\), a 50 Ω per square thin-film resistor (TFR) are also available in this process. Fig. 1 shows the schematic of the proposed GaAs HBT power amplifier which consists of a main power super transistor \( Q \) using three single transistors \( (Q_{1}, Q_{2}, \text{and } Q_{3}) \), a bias circuit, input/output matching networks and RC feedback network.

In HBT power transistors, bias depression is occurred particularly at high input power level [7]. That is, an increasing in the input signal power causes a decrease in the base-emitter DC voltage \( (V_{BE}) \), thus resulting in the change of operating mode in PA and hence distortion. Actually, the practical base bias voltage \( (V_B) \) has been given by Eq. (1), where \( V_{B,DCQ} \) is the transistor base voltage at quiescent mode with no input signal, and \( \Delta V \) is the bias depression term, more detail theoretical analysis is given in [8].

\[
V_B = V_T \cdot \ln\left(\frac{I_{DC}}{I_S}\right) - V_T \cdot \ln(I_0(x)) = V_{B,DCQ} - \Delta V
\]  

In order to improve linearity, bias circuit of this proposed PA is shown in Fig. 1 enclosed by dashed box, where double diodes \( (Q_{B1}, Q_{B2}) \) are used to increase the linear output power range. Shunt capacitor \( (C_{BP}) \) at the base of the emitter-follower \( (Q_{B3}) \) creates a low output impedance for the bias circuit, resulting in an increasing...
RF leakage to the circuit. The increased RF leakage forces the emitter-follower transistor ($Q_{B3}$) into a bias depression to compensate the bias depression of the power transistor ($Q$) due to the high RF input signal. The circuit is able to improve the linear operation range, in addition to its effectiveness in compensating for temperature and process variations, while occupying a small chip area.

### 2.2 Mixed matching networks and feedback

The design of T- or Pi-type matching networks is usually developed with the intent to achieve wider bandwidth of the networks and hence broadband amplifiers. With a little difference from conventional matching method which uses lumped elements in C-band, in this design, mixed approach is utilized by combining lumped and distributed elements, in other words, on-chip spiral inductors in the proposed PA are replaced by transmission lines ($TL_1$, $TL_2$, and $TL_3$) because lumped inductors tend to have higher resistive losses than capacitors [9]. In addition, it seems that impedance matching structure shown in Fig. 1 is configured to L-type, however, transmission lines can be modelled [10] by using lumped elements as shown in Fig. 2, their values are given by Eq. (2), where $Z_0$, $\omega$ and $\theta$ represent characteristic impedance, angular frequency and electrical length, respectively. That means impedance matching networks in this work are configured as Pi-type structure for bandwidth enhancement. Note that $TL_3$ here is a part of output matching network.

$$
\begin{align*}
L &= \left(\frac{Z_0 \cdot \sin \theta}{\omega}\right), \\
C &= \left(\frac{1 - \cos \theta}{\omega \cdot Z_0 \cdot \sin \theta}\right) 
\end{align*}
$$

On the other hand, feedback technology improves linearity-efficiency trade-off dramatically [11]. For an amplifier, feedback techniques are often used to achieve excellent matching to the input part and flatten gain over the required bandwidth, partially cancels distortion products hence improve linearity [12]. Moreover, feedback increases output power because of the power increase in input as a consequence of feedback and thus improving efficiency. However, for PAs, the use of significant feedback is dismissed due to insufficient gain. At a result, optimum values of $C_r$, $R_{F1}$ and $R_{F2}$ in this design are chosen to meet input matching, efficiency and gain over required bandwidth.
2.3 PA layout and fabrication

In this design, the eventual sizes of capacitors, resistors and transmissions lines are determined by simulations and optimizations in Keysight Advanced Design System software. Furthermore, modified has been carried out for all transmission lines based on the EM simulations. The chip photo of proposed GaAs HBT PA is shown in Fig. 3 with a size of 1.5 × 1.1 mm². In order to maximize the gain, the back-via holes at emitter of main transistor are paralleled for reducing parasitic inductance effects. Note that active bias circuit is located nearby power transistor for temperature compensation.

3 Measurement results

The proposed PA is measured via on-wafer with 150 µm spacing GSG RF probing arms. All measurements are performed at a single supply voltage of 2.3 V, provided by HP 6624A dual channel DC power supply, the quiescent current of this PA is 157 mA. S-parameters performance are measured using Agilent PNA E8363B Network Analyzer. Large signal characterization has been carried out with continuous-wave (CW) signal using Agilent E8257D Analog signal generator, E4417A Power Meter and N9030A Signal Analyzer. Due to the limitation of the existing instruments, 30-dB attenuator (JW-SMA-30 dB-18 GHz) are connected to the output in order to measure the output power higher than 20 dBm. Moreover, 13-dB directional coupler (87301D OPT 292) is used to check whether PA is oscillating. The whole instrument setup and connections are shown in Fig. 4.
3.1 Small-signal measurement results

The measured small signal S-parameters of this single stage PA are shown in Fig. 5. The single stage PA has a maximum small signal flatten gain ($S_{21}$) better than 10.0 dB, and a 1.6 GHz 1-dB bandwidth from 4.2 GHz to 5.8 GHz (32%) due to the bandwidth enhance technology of PA circuit with mixed matching network and feedback technology. The input and output reflection coefficients are less than $-8$ dB and $-10$ dB at 5 GHz, respectively. The relatively poor input return loss of about 3 dB is mainly due to the fact that the input matching network is designed to provide a flatter gain.

3.2 Large-signal measurement results

The measured power gain and power added efficiency (PAE) are plotted in Fig. 6. The results demonstrate the saturation output power is up to 23.2 dBm with a PAE of 47.2% for a CW signal at 5 GHz. An average $10\pm1$ dB flatten power gain has been obtained due to feedback, comparable efficiency and gain performance make this single stage PA has potential for Doherty PA architecture. For broadband performance, PAE, large signal gain and saturation output power ($P_{sat}$) have been measured in the frequency from 3.8 GHz to 6.2 GHz, which is given in Fig. 7. The 1-dB $P_{sat}$ bandwidth ranges from 4.2 GHz to 5.8 GHz with average $P_{sat}$ of...
22.5 dBm, the corresponding fraction bandwidth is 32%, and PAE all better than 40% in this frequency ranges.

Two-tone simulation has been performed with a signal centred at 5 GHz with tone spacing of 500 KHz, the results are shown in Fig. 8, where the IMD3 value of

Fig. 6. Measured power gain and PAE at 5 GHz.

Fig. 7. Measured peaking PAE and saturation output power verse frequencies.

Fig. 8. IMD3 results of the proposed HBT PA with and without feedback.

Two-tone simulation has been performed with a signal centred at 5 GHz with tone spacing of 500 KHz, the results are shown in Fig. 8, where the IMD3 value of
The proposed PA is maintained below $-38 \text{ dBc}$ up to an output power of $23 \text{ dBm}$. Note that IMD3 performance is improved at output power from $15 \text{ dBm}$ to $22 \text{ dBm}$ when applied RC feedback to circuit.

Fig. 9 shows the measured frequency spectrum of the output signal at $5 \text{ GHz}$. In this measurement, $30 \text{ dB}$ attenuator is connected to output terminal due to the power limitation of instrument, and $13 \text{ dB}$ coupler is also added in order to detect whether PA is oscillating, considering $2 \text{ dB}$ loss in all measurement path, hence $45 \text{ dB}$ Ref Offset shown in Fig. 9 is reasonable. It is noted that the result shows at least $34.0 \text{ dB}$ suppression of unwanted signal, which owing to linearization technologies of active bias and RC feedback.

![Fig. 9. Measured frequency spectrum at $5 \text{ GHz}$.

Measured results are compared to recent literatures in Table I, the proposed PA exhibits a relative wide bandwidth, high efficiency, and low DC power consumption ($P_{DC}$) performance, while showing comparable die area.

**Table I.** Comparisons of reported PAs and this work

|                | This work$^\dagger$ | [13]$^\ddagger$ | [14]$^\dagger$ | [15]$^\ddagger$ | [16]$^\ddagger$ |
|----------------|---------------------|-----------------|----------------|----------------|----------------|
| BW (GHz)       | 4.2–5.8             | 4.9–5.9         | 4.5–5.5        | 5              | 5.15–5.85      |
| Psat (dBm)     | 23.2                | 29              | 24             | 28             | 31.1           |
| Gain (dB)      | 10 ± 1              | 26 ± 1          | 10             | 22             | 26.6           |
| PAE (%)        | 47.2                | 30              | 38.8           | 31             | 44.5           |
| $P_{DC}$ (mW)  | 361.1               | 809.2           | 647.4          | 2035           | 2777.3         |
| Area (mm)      | 1.65                | 0.70            | 1.07           | 2.17           | 1.40           |
| Process        | GaAs HBT            | GaAs HBT        | Si CMOS HBT    | SiGe HBT       | GaAs HBT       |

$^\dagger$–Single-stage PA  
$^\ddagger$–Two-stage PA  
$^\ddagger$–Three-stage PA
4 Conclusion

This work has developed a broadband GaAs HBT MMIC class-AB power amplifier, which demonstrates broadband and high efficiency performance at a low supply voltage of 2.3 V. Mixed matching network with transmission lines and capacitors are designed for wide bandwidth matching, RC feedback technology is used to achieve a flatter gain and efficiency improving in a wide frequency ranges. Linearizing techniques are applied to bias circuit design in order to compensate base voltage depression, temperature and process variations, thus enhancing the linearity. All above functions are integrated in MMIC PA with size of $1.5 \times 1.1 \text{ mm}^2$, and eventual measured results demonstrate a flatten gain of $10 \pm 1 \text{ dB}$, saturation output power and PAE of better than 22 dBm and 40% respectively in frequencies from 4.2 to 5.8 GHz. The prototype achieves a linear output power of up to 23.2 dBm with a PAE of 47.2% at 5 GHz. Moreover, two-tone simulation show that it can maintain IMD3 below $-38 \text{ dBc}$ up to 23 dBm. These results indicate good performance and great potential for providing high efficiency PA modules used in future broadband handsets wireless applications at a low supply voltage.

Acknowledgments

This work was supported by Advance Research Foundation of China (Grant No. 9140Axxx501), National Defines Advance Research project (Grant No. 3151xxxx301) and Frontier innovation program (Grant No. 48xx4). The chip was fabricated by the Sanan Integrated Circuit Co., Ltd. Xiamen, China.