**PEx: Memory-efficient Microcontroller Deep Learning through Partial Execution**

Edgar Liberis$^{1,2}$  Nicholas D. Lane$^{1,2}$

**Abstract**

Embedded and IoT devices, largely powered by microcontroller units (MCUs), could be made more intelligent by leveraging on-device deep learning. One of the main challenges of neural network inference on an MCU is the extremely limited amount of read-write on-chip memory (SRAM, < 512 kB). SRAM is consumed by the neural network layer (operator) input and output buffers, which, traditionally, must be in memory (materialised) for an operator to execute. We discuss a novel execution paradigm for microcontroller deep learning, which modifies the execution of neural networks to avoid materialising full buffers in memory, drastically reducing SRAM usage with no computation overhead. This is achieved by exploiting the properties of operators, which can consume/produce a fraction of their input/output at a time. We describe a partial execution compiler, PEx, which produces memory-efficient execution schedules automatically by identifying subgraphs of operators whose execution can be split along the feature/"channel" dimension. Memory usage is reduced further by targeting memory bottlenecks with structured pruning, leading to the co-design of the network architecture and its execution schedule. Our evaluation of image and audio classification models: (a) establishes state-of-the-art performance in low SRAM usage regimes for considered tasks with up to +2.9% accuracy increase; (b) finds that a $4 \times$ memory reduction is possible by applying partial execution alone, or up to $10.5 \times$ when using the compiler-pruning co-design, while maintaining the classification accuracy compared to prior work; (c) uses the recovered SRAM to process higher resolution inputs instead, increasing accuracy by up to +3.9% on Visual Wake Words.

1 Introduction

The low cost and versatility of microcontroller platforms have made them an attractive choice for a wide range of applications: an estimated 29B units shipped in 2021 (Grand View Research, 2022). This includes numerous embedded, personal and IoT devices, many of which could be enhanced with computational intelligence brought by deep learning.

A microcontroller unit (MCU) is a single chip mainly consisting of a power-efficient CPU, read-only Flash memory and read-write static RAM (SRAM). Table 1 compares MCUs along compute, memory and storage capacity axes with GPU server and mobile hardware capable of executing neural networks. The low price and power usage of MCUs come with a marked downgrade in the computational ability: memory capacity lies orders of magnitude behind the next-best hardware, and there is little-to-no memory hierarchy and parallelism to exploit for optimisation. This presents a significant challenge to deep learning inference on the device itself, causing applications to rely on fully remote or hybrid deployments (Almeida et al., 2021), which results in sacrifices in data privacy and autonomy.

Enabling on-device network inference has been shown to require specialised research into low-footprint deep learning. TinyML (Warden & Situnayake, 2020) is a research direction that encompasses hardware improvements (Sadiq et al., 2022); systems-level software research, such as run-time...
time (David et al., 2020), layer implementations (Lai et al., 2018) and model compilers (Chen et al., 2018); model discovery, compression and architecture search (NAS) (Liberis et al., 2021; Banbury et al., 2020; Lin et al., 2020).

1.1 Memory usage of neural networks on MCUs

In this work, we focus on the issue of high memory (SRAM) usage of neural network inference, which prevents the MCU deployment of models with large activation tensors.

A neural network is defined as a computational graph of layers, called operators, with data dependencies between them. Most MCU deep learning runtimes and kernel implementations (Chen et al., 2018; David et al., 2020; Lai et al., 2018), have adopted a one-operator-at-a-time execution regime. For each layer/operator in the network, the runtime:

1. Allocates the output buffer for the operator in SRAM;
2. Executes the operator, using inputs read from SRAM and parameters read from the separate Flash storage;
3. Marks the operator’s inputs’ buffers as available memory (i.e. deallocates from SRAM, may be implicit), if the buffers are not used later.

Under this execution regime, called ordinary execution, the memory bottleneck is the size of the largest operator’s working set (input and output buffers) along with any other tensors that must be retained for subsequent operators. This bottleneck must lie within the SRAM capacity constraints.

Some systems-level model-agnostic methods have been developed to reduce SRAM usage of neural networks by optimising buffer layout in memory, such as buffer bin-packing (David et al., 2020) and operator reordering (Liberis & Lane, 2019). SRAM usage is also an optimisation objective in MCU-compatible model discovery methods (Fedorov et al., 2019; Liberis & Lane, 2021; Banbury et al., 2020).

1.2 PEX: Partial execution for memory efficiency

A core contribution of this paper is a novel model compiler, called PEX, which realises further gains in memory usage by moving beyond the paradigm of executing one operator at a time and instead executing operators partially to produce and/or consume one feature/channel of data at a time. The idea of partial execution can be applied to arbitrary neural networks. A particular instance of this was first described in MobileNet-v2 (Sandler et al., 2018) as a memory-efficient trick to execute the inverted residual block (IRB). Figure 1 uses this example to illustrate the concept of partial execution, both diagrammatically and in pseudo-code.

Under ordinary execution, the IRB memory bottleneck resides at the operator C: the bottleneck consists of the input and output buffers of C, as well as output of A retained for operator E, amounting to 52.7 KB (at 8-bit precision).

However, operators B, C and D can be combined along the channel axis. In a partial execution loop, for each of the 144 channels, operator B (conv.) produces one output channel, operator C (depthwise conv.) transforms it, and operator D (conv.) consumes it and writes its contribution
to its output buffer. The memory bottleneck is within the loop at operator $\mathcal{C}$, amounting to 8.5 KB (at 8-bit precision). It consists of the input to $\mathcal{B}$, one channel output of $\mathcal{B}$ (input to $\mathcal{C}$), one channel output of $\mathcal{C}$, and the full output buffer of $\mathcal{D}$, preallocated before the start of the loop.

Such execution has largely become obsolete on mobile platforms due to the abundance of RAM (Table 1) and an inferior data access pattern. However, on MCUs data access pattern is of little concern due to the lack of data caches. Neural networks inspired by the IRB continue to proliferate (Howard et al., 2019; Cai et al., 2018; Tan & Le, 2019), so discovering analogous memory-saving execution schedules for new architectures would greatly benefit deep learning for MCUs by reducing the SRAM footprint of inference.

**Automatic partial execution with PEX.** We devise abstractions and execution rules required to apply partial execution to any network layer layout, and automate the scheduling decisions using a dynamic programming-based algorithm. These form the core of PEX, which discovers computationally-equivalent, yet more memory-efficient network execution schedules for arbitrary neural networks. PEX produces an intermediate representation—a topologically-ordered list of network operators, their execution rules and partial execution loop information—which can be used to generate native microcontroller code.

Figure 2 shows the per-layer memory usage profile of the MobileNet-v2 architecture, showing that partial execution enables a $4 \times$ peak memory usage reduction. However, partial execution alone cannot reduce peak memory usage to arbitrarily low values: a particular layer arrangement at the memory bottleneck may not lend itself to optimisation, or the sizes of buffers allocated at the start of the partial execution loop may cause the memory bottleneck.

**Compiler+pruning network co-design.** We propose using *structured pruning* to change the network architecture automatically to reduce peak memory usage under partial execution. Structured pruning entirely removes the least important feature maps (*e.g.* convolutional channels), and we instruct it to target memory bottlenecks identified by the compiler. PEX is repeatedly invoked during pruning, with new memory bottlenecks reported back to the pruning algorithm at each step. Conversely, removing feature maps changes loop sizes and execution instructions produced by the compiler. Therefore, the two work in tandem to co-design the network architecture and the execution schedule.

We discuss the place of our methodology within related microcontroller deep learning work in Section 2, give the algorithm details in Section 3, including integration with pruning and considerations around quantisation, and perform quantitative comparisons in Section 4.

Overall, the contributions of this work are as follows:

- We devise abstractions and execution rules for arbitrary networks, which enable partial execution.
- We devise a model compiler, PEX, which automatically creates a partial execution schedule while minimising peak memory usage, unlocking significant memory usage reduction compared to ordinary evaluation.
- We leverage partial peak memory usage as an optimisation goal within structured pruning, reducing the model’s memory footprint further automatically.
- We reduce memory usage by up to $10.5 \times$ and establish new state-of-the-art models for three classification tasks in the low SRAM usage regime, improving accuracy by up to 2.9%, compared to prior work.

## 2 RELATED WORK

### 2.1 Deep learning on microcontrollers

Prior work in microcontroller deep learning typically assumes an ordinary execution-based runtime, such as TFLM (David et al., 2020). MCU-friendly resource footprints are achieved by: manual architecture design (Zhang et al., 2017; Mocerino & Calimera, 2019), quantisation (Jacob et al., 2018), network pruning (Liberis & Lane, 2021) or neural architecture search (NAS) (Lin et al., 2020; Banbury et al., 2020). Some methods target inference with sparse matrices (Fedorov et al., 2022; 2019), or use pruning as a nested step within NAS (Liberis et al., 2021). Prior discovered models can operate within the partial execution regime.

Standardised runtimes are an important common ground for hardware, model compression and network design research. However, prior work shows that performance benefits can be reaped by moving beyond standard assumptions. TVM (Chen et al., 2018) is a general model compiler that can perform both computation graph- and inference code-level optimisations and produce binaries for various targets, including microcontroller platforms. MCUNet-v2 (Lin et al.,
forgoes layer-by-layer execution in favour of executing memory-intense layers using one input tile (“patch”) at a time; we discuss this execution style further on.

Alternatively, computational constraints can be relaxed by introducing memory hierarchy. Svoboda et al. (2022) use a microSD card to offload weights and activations of the network, which also significantly increases latency and power usage due to data transfer and the presence of external storage. More promisingly, Sadiq et al. (2022) show that external SDRAM (< 8 MB) and Flash memories can be used to offload selected parameters and activation matrices transparently using DMA. This approaches the latency of on-chip memory inference, but at the cost of additional power usage.

2.2 Computation split approaches

The computation of neural network layers’ outputs can also be split along their spatial axes instead of (or in addition to) the channel axis, resulting in patch-based execution.

Computation split approaches for memory-constrained microcontroller platforms overlap, to some degree, with the techniques developed for model parallelism. Conceptually, the two optimise for different scales: model parallelism maximises utilisation, cache hits, or reduces the multi-gigabyte memory (vRAM) footprint or communication overhead on multi-core GPU/TPU hardware for neural network training; here, we split computation to save 100s KB of SRAM for inference on relatively simplistic single-core hardware, but in the presence of quantisation and greater sensitivity to computation overheads (strict compute budget).

The problems can be approached similarly: both develop frameworks to reason about neural networks, which identify independent computations and optimise their execution schedule. Dryden et al. (2019a) parallelise execution over the sample and spatial dimensions (i.e. patches) and optimise workload assignment under a benchmark-informed cost model using a shortest-path graph algorithm; this methodology is also updated to consider channel and filter dimensions of a CNN (Dryden et al., 2019b); Automap (Schaarschmidt et al., 2021) and FlexFlow (Jia et al., 2019) automatically discover computation sharding axes by leveraging MCTS and predictor-powered randomised search, respectively; Xu et al. (2022b) combine patch-based execution with gradient checkpointing to reduce vRAM usage for high-resolution inputs; Artemev et al. (2022) consider operation pattern matching and replacement, reordering and splitting of operators to conserve memory by reducing the size of intermediate matrices; Ivanov et al. (2021) analyse data flow to minimise data movement in Transformer models by identifying data layout and operator fusion improvements. We are optimistic about any future methodology cross-over.

In deep learning for MCUs, patch-based execution has been explored by MCUNet-v2 (Lin et al., 2021). An analogous idea has been previously explored by Alwani et al. (2016) for avoiding off-chip memory access. Only a spatial segment (a “patch”) of a layer’s output is computed at a time (thus full output is never materialised in memory), before being consumed by subsequent layers. This reduces memory usage at the cost of computation overhead due to the re-computing of intermediate values that are required for more than one patch (edge overlap). The amount of overhead varies per architecture and depends on convolutional kernel size and strides. Extended discussion of this alternative/orthogonal approach is in Appendix B. As it is the closest relevant prior work, we perform a quantitative comparison in Section 4.

3 DESIGN OF PEX

PEX is a compiler for arbitrary neural networks which automatically generates execution schedules with partial execution loops (e.g. Figure 2). This drastically reduces SRAM usage compared to ordinary execution used in prior work.

Conceptually, PEX is built as a progression of the following three components: (1) the partial execution framework: rules, axioms and abstractions, which define how each operator may be executed; (2) execution state and memory model, which allows deriving correct execution schedules for the entire network; (3) a dynamic-programming-based algorithm which finds an execution schedule that minimises the peak memory usage.

In the following, we describe the three components of PEX and discuss the interaction between computational correctness and quantization, as well as using PEX within structured pruning to reduce SRAM usage further. For contextual clarity, we will use convolutional neural network (CNN) terminology and reference the MobileNet-v2 IRB example.

3.1 Partial execution framework

Definition 1. A neural network is a computation graph of tensors, produced by operators (layers). We consider arbitrary neural networks which process $R$-dimensional tensors ($R \geq 2$) of shape $N \times \ldots \times C$, where $N$ is the batch size, and $C$ is the number of channels/feature maps. A “channel” is a tensor slice in the $C$ dimension. This includes 4-dimensional tensors of shape $N \times H \times W \times C$ seen in 2D CNNs, where $H$, $W$ are the width and height of the image. The dimensions’ order is unimportant: for CNNs, NCHW and NHWC are supported; NCHW may be preferred to avoid strided loads/writes.

Definition 2. A tensor $t$ can be present in memory in two forms: fully materialised (denoted by $t^F$) or partially materialised (only one channel, denoted by $t^P$).
Definition 3. There are only two types of operators: channel-wise operators (borrowing CNN terminology; denoted by ‘C’) and aggregating operators (denoted by ‘A’):

- **Channel-wise operators (C-types)** are depthwise convolutions, pooling layers (both local and global) and any element-wise operators such as addition or ReLU. In principle, these operators consume one input channel to produce one output channel. Output channels are independent, and the implementation of the operator is often a simple loop repeating the computation that maps an input channel to an output channel.

- **Aggregating operators (A-types)** are dot products: convolutions and fully connected (dense) layers. To compute the output tensor, they map all input channels to one output channel (multiple times, for all output channels), or, equivalently, compute one input channel’s contribution to all output channels (multiple times, for all input channels). That is, A-types can either generate one channel of their output at a time, providing the full input buffer is present in memory, or consume one channel at a time and write its contribution to the fully allocated output buffer. Due to this generating/aggregating property, they will be found either at the start or the end of partial execution loops.

Remark 4. We describe partial execution loops as processing one channel of data at a time. However, in a loop with a total of \(C\) channels to be iterated over, the number of channels computed at once can be any \(K \ll C\). Increasing \(K\) increases the memory usage but can have a beneficial effect due to the use of SIMD kernel implementations (when \(K\) is a multiple of 4) and lowering overhead associated with operator context switching, if any (implementation-dependent). The highest possible value of \(K\) that does not cause a memory constraint violation can be found for each loop independently using binary search.

Definition 5. An operator is a mapping from input tensors \(i = \{i_1, \ldots\}\) to an output tensor \(o\), denoted \(i \xrightarrow{op} o\). The operator’s type (A or C) allows for multiple ways of executing it using different materialisation forms of inputs \(i\) and output \(o\). For operators with multiple inputs (e.g. addition), all inputs always share the same materialisation form, so the set of inputs can be denoted with \(i^F\) or \(i^P\).

In total, we establish six rules for executing an operator \(op\) (presented diagrammatically in Figure 3):

**Full continue** (for both A- and C-types): \(i^F \xrightarrow{op} o^F\). Input and output buffers are present in memory fully, and the operator is not in a partial execution loop. The compiler may fall back to ordinary execution by only using ‘Full Continue’.

**Partial continue** (C-type only): \(i^P \xrightarrow{op} o^P\). A channel-wise operator is executed for one input channel to produce one output channel. Example: a depthwise conv. operator computing one output channel.

**Generate** (A-type only): \(i^F \xrightarrow{op} o^P\). Computes one output channel from fully-materialised input data.

**Accumulate** (A-type only): \(i^P \xrightarrow{op} o^F\) Consumes one channel of input data and writes its contribution to a fully-materialised output buffer.

The following rules can be applied “spontaneously” to change the materialisation form of a tensor \(t\), when needed. For tensors consumed by multiple operators, the rule does not have to be applied to all branches (graph edges).

**Slice**: \(t^F \rightarrow t^P\). The runtime reads one channel at a time from tensor \(t\) to facilitate partial execution of any subsequent operator that requires partially-materialised input. In this case, \(t^P\) does not need to be explicitly allocated: it is an offset/view into \(t^F\).

**Post-concatenate**: \(t^P \rightarrow t^F\). Channels of \(t\) are written into a preallocated full buffer. In this case, \(t^P\) does not need to be explicitly allocated: the producer of \(t^P\) can write into a particular offset of \(t^F\).

Definition 6. A loop context (\(C\)) is a set of tensors that are kept in memory (fully materialised) due to a current loop that will repeatedly read from or write to these tensors. Loop context tensors are allocated in SRAM prior to the first iteration of the loop and deallocated after the last iteration.

In MobileNet-v2 IRB (Figure 1), the context consists of inputs to operator \([\text{exec. ‘Generate’}]\) and the output of...
operator [□] (exec. ‘Accumulate’). At the \(i\)th iteration of the loop, [□] reads its entire input from the context to produce its \(i\)th channel, and [□] writes the contribution of its \(i\)th input channel to its output buffer in the context.

3.2 Deriving an execution schedule

A compiler produces a sequence of instructions, which determine which operator should be executed (and how), to obtain the network’s outputs from its inputs. Conceptually, an instruction is an action that causes the execution state to transition from some current state to the next state. The instructions are applied until the final state is reached in which all neural network layers were executed.

We are interested in modelling memory usage, so the execution state will consist of information about tensors present in the memory, their materialisation form, and information about the current partial execution loop, if any.

**Definition 7.** The algorithm considers an execution state \(S = \langle \text{Mem}, C \rangle\) and builds up an instruction list (history) \(H\). ‘Mem’ is the state of memory: a set of tensors currently present in memory, each either fully or partially materialised; ‘C’ is the loop context (see Def. 6); \(H\) is a list of instructions required to arrive at state \(S\).

**Remark 8.** The network’s parameters (weights) do not reside in SRAM under any execution regime—individual values are loaded from the read-only on-chip Flash memory.

**Definition 9.** The algorithm works backwards through the network computation graph \(G\)—tensors in ‘Mem’ are treated as tensors yet to be computed. The initial state \(S_0\) is the set of fully-materialised graph output tensors: \(S_0 = \{ o^P | o \in \text{outputs}(G) \} \), and similarly, the final state \(S_f\) is the set of fully-materialised inputs. This acts as a reachability analysis: only required operators will be executed.

**Constraint 10.** No output is computed twice. We do not aim to increase the amount of computation required for a single inference pass of a neural network.

**Definition 11.** Table 2 lists allowed state transitions, called derivation rules. Each rule has a set of conditions which must be satisfied for it to be applied. The transitions closely match the operator evaluation rules described earlier, but also modify the loop context as required.

If derivation rules can be successfully applied to transition from the starting to the final state, we obtain a sequence of instructions (potentially, out of many) to execute a neural network. The instructions, along with any loop metadata, are sufficient for generating microcontroller code. Figure 1 shows the MobileNet-v2 IRB example within the devised framework: first, by erasing particular layer information, leaving only A- and C-type annotations; then, by applying the derivation rules to produce a state transition graph.

**Algorithm 1** OPTIMISEPMU computes a partial execution schedule which minimises peak memory usage.

1: \(\triangleright\) Input: a set of tensors to be computed \(\text{Mem}\) and loop context \(C\) (empty for the initial call).
2: \(\triangleright\) Returns: the instruction list \(H\), the computed PMU and the final loop context \(C^*\) (empty if \(C = \emptyset\)).
3: \(\text{function OPTIMISEPMU}(\text{Mem}, C)\)
4: if End (Mem, C) conditions are satisfied then
5: \(\text{return} \langle H = [], \text{PMU} = \sum_{t \in \text{Mem}} |t|, C^* = \emptyset \rangle\)
6: if LoopEnd (Mem, C) conditions are satisfied then
7: \(\langle H, \text{PMU}, C \rangle \leftarrow \text{OPTIMISEPMU}(\text{Mem}, C)\)
8: \(\text{return} \langle H, \text{PMU}, C, C^* \rangle\)
9: \(\text{bestConfig} \leftarrow (\text{unknown})\)
10: for \(t \in \text{Mem}\) do
11: \(\text{for Rule} \in \{\text{FullContinue, Slice...}\} \) do
12: if Rule (Mem, C) conditions are satisfied then
13: \(\text{Mem}', C' \leftarrow \text{Rule}(t, \text{Mem}, C)\)
14: \(H', \text{PMU}', C^* \leftarrow \text{OPTIMISEPMU}(\text{Mem}', C')\)
15: \(\text{PMU}^* \leftarrow \max(\text{PMU}', \text{LOCALPMU}(t, \text{Mem}', C^*))\)
16: if \(\langle H', \text{PMU}', C^* \rangle\) better than bestConfig then
17: \(\text{bestConfig} \leftarrow \langle H', \text{PMU}', C^* \rangle\)
18: \(\text{return} \text{bestConfig}\)

3.3 An algorithm to minimise peak memory usage

Out of numerous valid derivations, we are interested in choosing instructions that minimise SRAM usage. If we knew which sequence of instructions minimises peak memory usage from a particular execution state, we could record and reuse this information to build up a full execution schedule—a hallmark of a dynamic programming algorithm.

Algorithm 1 describes a high-level pseudocode procedure ‘OptimisePMU’ which enumerates all state transitions to find a sequence of instructions that results in the smallest peak memory usage (PMU) for arbitrary neural network computation graphs. Note that calls are memoised: results for the same input are remembered and not recomputed. In practice, we are interested in not just accumulating execution history \(H\) but also keeping track of the best-seen peak memory usage and the complete loop context (denoted \(C^*\), returned from upstream computation) to calculate the PMU of operators within partial execution loops. The algorithm has exponential computational complexity in the number of operators but, due to small input size (<100 operators) and limited branching in the network architecture, the optimised schedules are obtained within seconds in practice.

The algorithm relies on four straightforward helper functions: (1) ‘rule conditions are satisfied’ checks if Mem and C satisfy set predicates set out in the definition of rule; (2) Rule(...) invocation updates Mem and C according to the rule definition; (3) LOCALPMU(t, Mem, C*) computes the memory usage required (working set size) for tensor t to be computed using tensors in Mem; if loop context is present, it will be counted towards the memory usage; (4) ‘configuration x is better than y’ compares scheduling results: true if x has lower peak memory usage, if y is invalid, or if PMU is
equal but \(x\) is simpler; the latter can express a preference to avoid partial execution when there is no PMU improvement.

### 3.4 Effects on quantisation

Neural network deployment on MCUs requires parameters and activations to be quantised. This both enables the execution and saves space: an MCU may not have floating-point processing units, or they may consume more power; Flash and SRAM usage is reduced when parameters and activations are stored at e.g. 8-bit precision, instead of 32 bits.

Popular runtime and layer implementations use affine quantisation (Jacob et al., 2018), where operators compute a single output element at a time (stored in a CPU register) by accumulating contributions from all input features (multiplied by the learned weight) at 32-bit precision. When all contributions have been added, an activation function is applied, and the output is written to SRAM at 8-bit precision.

This poses a memory usage vs correctness trade-off for operators executed using the ‘Accumulate’ partial execution rule, which accumulate input contributions at each loop iteration: the accumulation/output buffers must be kept in SRAM at 32-bit precision for computational correctness. This would result in a \(4 \times\) memory usage increase for these buffers (changing from 8-bit to 32-bit representation), potentially reducing memory usage gains under partial execution.

To address this issue, we experiment with reducing the precision of the accumulation buffer, thus removing the \(4 \times\) memory inflation. The ‘Accumulate’ rule would only apply to a few layers in the network; we expect other layers to learn to compensate for any performance hit caused by the reduced precision of affected convolutions. We experiment with quantization-aware training using 32-bit, 16-bit and 8-bit precision for accumulation buffers and find no performance degradation in the network (see Section 4.3).

### 3.5 Structured pruning for partial execution

Most deep learning models are too resource-demanding for MCU hardware, not just due to their memory usage but also size or latency, which can be addressed with model compression. Typically, three dimensions of resource usage are optimised for MCU compatibility: (a) peak memory usage (bounded by SRAM size), (b) model size (bounded by Flash memory) and (c) the number of multiply-accumulate operations (MACs, Liberis et al. (2021) show that MACs are a highly accurate proxy for latency on an MCU processor).

We integrate PEX with the state-of-the-art MCU-aware model compression, which operates on the basis of differentiable structured pruning (Liberis & Lane, 2021), with the aim of (a) producing MCU-compatible models for our evaluation and (b) guiding pruning towards the memory bottleneck identified by our compiler. The method removes entire features/channels by repeatedly querying optimisation objectives during compression: we replace the default peak memory usage metric with an invocation of PEX, which reports the peak memory usage under partial execution and which operators’ outputs constitute the bottleneck.

This leads to co-design between the model compression and the partial execution compiler. Both structured pruning and the compiler operate on the channel dimension of the neural network operators. Iteratively, the following takes place: (1) pruning adjusts per-layer channel counts based on the current memory bottleneck, and other resource usage objectives; (2) the compiler computes a new execution schedule using the updated operator channel dimensions: this new schedule is likely different due to new channel dimensions; (3) the compiler reports a new peak memory usage result and new memory bottleneck back to the pruning algorithm.

### 4 Evaluation

In this section, we quantitatively evaluate our contributions:
Table 3. Resource usage of variations of MobileNet-v2 on ImageNet using ordinary, patch-based (4 $H$ and $W$ patches) or partial execution. PMU improvements brought by patch-based or partial execution vary, but partial execution always has zero computational overhead.

| MobileNet-v2 variant | Loop overhead | Total overhead | Peak memory usage (PMU) | Accuracy (8-bit q.) | MACs |
|----------------------|---------------|----------------|--------------------------|---------------------|------|
|                      | Patch† | Partial | Patch† | Partial | Ordinary | Patch† | Partial | Ordinary |
| Original             | +30.6% | 0%     | +9.3%  | 0%     | 1505 kB  | 321 kB  | 376 kB  | 71.52% | 301 M     |
| RD (MCUNet-v2)       | +13.8% | 0%     | +2.9%  | 0%     | 1505 kB  | 283 kB  | 376 kB  | 71.16% | 294 M     |
| Our modification      | +38.9% | 0%     | +11.2% | 0%     | 978 kB   | 278 kB  | 226 kB  | 71.20% | 295 M     |
| PEx-pruning co-design| +36.1% | 0%     | +9.6%  | 0%     | 1505 kB  | 321 kB  | 276 kB  | 71.20% | 288 M     |
| Original, 172×172 res.| +45.2% | 0%     | +12.6% | 0%     | 888 kB   | 218 kB  | 222 kB  | 69.58% | 193 M     |

1. We compare partial execution with patch-based execution (MCUNet-v2), the closest relevant prior work, by considering peak memory usage reduction and overheads of either approach on MobileNet-v2 models.
2. We apply PEX to five classes of architectures, using partial execution alone or the compiler-pruning co-design, to establish new state-of-the-art solutions in the low SRAM usage regime, compared to ten prior low-footprint models on three classification tasks.
3. We test whether storing accumulation buffers at reduced precision affects models’ accuracy (Section 3.4).

4.1 Comparison with patch-based execution

Patch-based execution is an alternative approach of splitting the computation to reduce memory usage (Section 2.2), which uses tensor slices along the image width and height axes (“patches”), instead of the channel axis. For MCUs, it is implemented by MCUNet-v2 (Lin et al., 2021): we compare it to PEX by examining the memory usage reduction and computational overheads for the MobileNet-v2 model, followed by several modifications to it that enable further improvement in SRAM usage.

Table 3 (row 1) considers variations of MobileNet-v2 architecture, evaluated on ImageNet.† The execution takes ≈301 M MACs and has a peak memory usage of 1505 kB. Patch-based and partial execution reduce it to 321 kB (↓4.7×) and 372 KB (↓4×), respectively, at the cost of additional 9.3% increase in MAC operation count for patch-based execution yet zero computational overhead for our approach.

It is impossible to conclusively argue whether a patch-based or partial approach is generally superior at reducing peak memory usage: the outcome depends on the architecture. To illustrate this, we consider two modifications of MobileNet-v2 (see Figure 5 in Appendix B): (a) to reduce overheads of patch-based execution, MCUNet-v2 develop an alternative version with a redistributed receptive field (RD); a change to reduce the resolution and kernel size earlier in the network;

†The resource usage, overheads, and accuracy of MCUNet-v2 models have been adjusted from originally reported data due to differences in evaluation. We explain the rationale in Appendix C.

(b) we present a version that reduces the memory bottleneck via additional spatial downsampling within the first inverted residual block (“MBConv”), in its projection layer, instead of the following block. Table 3 (rows 2, 3) shows that these minor modifications can drastically affect the models’ resource usage: our variation of MobileNet-v2 significantly increases computation faced by patch-based execution compared to the original model (15.5% total MAC increase) but, in the partial execution paradigm, yields the lowest peak memory usage seen so far with no computation overhead.

The modifications above are specific to MobileNet-v2 and cannot be straightforwardly applied to other architectures. Therefore, we consider two other generic ways to reduce an architecture’s peak memory usage: our compiler-pruning co-design and using lower input resolution. Table 3 (rows 4, 5) shows that (a) co-design can reduce PMU under partial execution to match that of patch-based execution while offering comparable accuracy/MACs to the two previously considered modifications; (b) by lowering the input resolution, we observe the lowest peak memory usage achieved so far (218–222 KB) at the cost of a < 2% accuracy drop.

Summary of 4.1. The network’s architecture determines whether patch-based or partial execution will give greater memory reduction, and can be modified to benefit either approach. Partial execution has no computational overhead.

4.2 Models under partial execution regime

In this section, we show the peak memory usage improvements achievable by PEx alone and the compiler-pruning co-design. We limit our scope to CNNs, as the most popular type of low-footprint neural networks, and consider three classification tasks: ImageNet (1000-class image classification) (Deng et al., 2009), VisualWakeWords (person detection) (Chowdhery et al., 2019) and SpeechCommands (keyword recognition via spectrogram classification) (Warden, 2018), and five classes of architectures: MobileNet-v2 (Sandler et al., 2018), EfficientNet (Tan & Le, 2019), RES-15 (Tang & Lin, 2018), MCUNet-v1 networks (Lin et al., 2020) and MicroNets (Banbury et al., 2020). Additional comparison points are provided by the differentiable pruning (DiffPru), DS-CNN (Zhang et al., 2017),
MCUNet-v2 (Lin et al., 2021), RES-8 (Tang & Lin, 2018) and ETinyNet (Xu et al., 2022a) architectures, resulting in ten low-footprint baselines. Models have been reevaluated under the same training pipeline and resource usage metrics (except for MCUNet-v2\(^1\)). We use the peak memory usage (PMU) versus classification accuracy plots for comparison; tabular data with all metrics are available in Appendix D.

**ImageNet under 128 kB of SRAM.** Figure 4 (top) shows the peak memory usage versus accuracy trade-off for ImageNet models. PEX alone improves PMU by 2.2× and 2.5× for MCUNet-v1 and EfficientNet-B0 architectures. The compiler-pruning co-design produces the only set of high-performing models under 128 kB SRAM usage amongst considered baselines in our evaluation environment. The models achieve 64.5%–65.4% accuracy, significantly outperforming a low-resolution MobileNet-v2 model (+13.9%).

**VisualWakeWords under 32 kB of SRAM.** Figure 4 (middle) shows the results for a variety of models for different input resolutions on the Visual Wake Words dataset. On MobileNet-v2, increasing input resolution increases PMU while producing diminishing returns in classification accuracy. At 80×80 input resolution, the compiler-pruning co-design decreases the PMU by 6.8× compared to the baseline, bringing it within the 32 kB range. This constitutes a +2.9% accuracy improvement compared to prior work (MicroNets VWW-2 and DiffPru) within this SRAM usage range. Alternatively, recovered SRAM allows using higher resolution inputs to increase accuracy by +3.9% while retaining comparable SRAM usage to the baseline.

**Keyword spotting under 16 KiB SRAM.** Figure 4 (bottom) shows results for the SpeechCommands dataset. We apply both PEX alone, and the compiler-pruning co-design to the parent architecture of MicroNets-L (i.e. instantiated at full channel counts, abbr. MN-L, in the figure), and the RES-15 architecture. The use of compiler alone yields 2.5× and 1.5× memory reduction, respectively, and the use of pruning brings the models under the desired SRAM limit, with only up to 1% accuracy loss compared to their original unpruned versions. This constitutes a +1.9% accuracy improvement compared to prior work (DS-CNN-S) under the 16 KiB SRAM limit. Applying co-design to the RES-15 architecture yields up to 10.5× memory reduction while matching the classification accuracy compared to the MicroNets-KWS-L baseline (using ordinary execution).

**Summary of 4.2.** PEX and PEX-pruning co-design reduce peak memory usage of high-performing models to establish state-of-the-art results in low SRAM usage regimes.

### 4.3 Accumulation buffer precision analysis

Previously, in Section 3.4, we discussed how the interaction of quantisation and partial execution requires intermediate
Table 4. The impact of reduced accumulator precision for three diverse models. The data shows no to negligible accuracy loss from sacrificing computational correctness for PMU reduction.

| Model                  | PMU:            | Mode:          | Accum. layers | Accum. layers |
|------------------------|-----------------|----------------|---------------|---------------|
| MCUNet-v1-S            | 333 kB          | Ordinary execution in int8 | 0 accum. layers | 0 accum. layers |
| ImageNet 160x160       | 768 kB          | Partial execution w/ 32-bit accumulators (QAT) | 1 accum. layer | 0 accum. layers |
| Acc: 59.89%            | 170 kB          | Partial execution w/ 16-bit accumulators (QAT) | 2 accum. layers | 1 accum. layer |
| 0 accum. layers        | 186 kB (↓1.8×)  | 307 kB (↓2.5×) | 69.0 kB (↓2.5×) | 69.0 kB (↓2.5×) |
| Acc.: 59.91%           | Acc.: 90.14%    | Acc.: 96.77%   | Acc.: 96.71%   | Acc.: 96.71% |
| MobileNet-v2           | 294 KB (↓2.6×)  | Partial execution w/ 8-bit accumulators (QAT) | 3 accum. layers | 2 accum. layers |
| VWW 160x160            | 69.0 kB         | 141 kB (↓2.4×) | 192 kB (↓4.6×) | 65.8 kB (↓2.6×) |
| Acc: 90.12%            | Acc.: 96.99%    | 59.66% (-0.23%) | Acc.: 96.99%   | Acc.: 96.99% |
| MicroNets-KWS-L        | 170 kB          |                |               |               |
| SpeechCommands         | 307 kB (↓2.5×)  |                |               |               |
| Acc.: 59.77%           | Acc.: 96.71%    |                |               |               |
| 0 accum. layers        | 2 accum. layers | 1 accum. layer |               |               |

results of operators executed using the ‘Accumulate’ rule to be stored at 32-bit precision to preserve computational correctness. To remedy the resulting memory usage increase, we suggest sacrificing computational correctness for affected operators by storing accumulation buffers at reduced precision and allowing other operators to learn to compensate for this imprecision.

We aim to see whether reduced precision results in accuracy loss. We extended TensorFlow’s quantisation-aware training (QAT) implementation to learn quantisation parameters for accumulation buffers (pre-activation), which are used during execution to re-quantise the buffers to the desired precision when updated. We experiment with the 32-bit (correct), 16-bit and 8-bit precision. The scheduler is parameterised with the memory cost of increased precision and, therefore, the ‘Accumulate’ rule will be avoided if there is an alternative with a lower PMU and fewer affected layers.

Partial execution is mathematically equivalent to ordinary execution: without quantisation, both approaches have tensor values within the noise introduced by a differing order of operations; with quantisation, this noise is amplified, resulting in accuracy differences. We repeat the QAT for different quantisation levels of accumulation buffers; this also introduces noise due to randomness in the training pipeline, and the reduced precision also acts as a regulariser during QAT.

Table 4 shows the classification accuracy of MCUNet-v1-S, MobileNet-v2, and MicroNets-KWS-L models under ordinary and partial execution, which shows no accuracy loss is observed for all tasks for up to 16-bit accumulation precision, resulting in up to 2.6 × PMU reduction. Lowering the precision to 8-bit results in up to 4 × PMU reduction and -0.23% accuracy loss only in the MCUNet-v1-S experiment.

Summary of 4.3. Operators executed using the ‘Accumulate’ rule can use reduced accumulation precision for lower memory usage: this has no or negligible accuracy loss.

4.4 Limitations and future work

PEX’s ability to reduce memory usage is limited by the network’s architecture (also applies to patch-based execution, see Appendix B), which can be adjusted in an informed way to allow further memory improvement. Here, we leveraged pruning as a general way to do so; PEX could be integrated with a neural architecture search system (NAS) that considers different layer connectivity to avoid some unfavourable layer arrangements automatically.

Additionally, data from an on-device MCU deployment could be of interest as auxiliary evaluation. The classification accuracy results presented in this section have been obtained by faithfully simulating partial execution under the presence of quantisation on a desktop machine. However, because partial evaluation yields deterministic memory gains, we would expect any on-device deployment to only confirm this.

5 Conclusions

A limited amount of SRAM on microcontroller platforms significantly impedes the on-device execution of neural networks on embedded, personal and IoT devices. To address this, we created a partial execution framework for arbitrary neural networks within the PEX model compiler, which automatically finds execution schedules that minimise peak SRAM usage. This is achieved by identifying subgraphs of the network’s layers whose execution can be split along the channel axis, resulting in a computationally-equivalent yet more memory-efficient schedule compared to ordinary execution, at no extra computational cost. We enhance PEX with a structured pruning method, resulting in a co-design between the network’s architecture and its execution schedule, which reduces SRAM usage even further. We evaluate PEX on five architecture classes and establish state-of-the-art performance in low SRAM usage regimes for ImageNet, VisualWakeWords and SpeechCommands datasets with up to +2.9% accuracy increase, compared to ten prior low-footprint models. We find that a 4 × memory usage reduction is possible by applying PEX alone, or up to 10.5 × when using the compiler-pruning co-design, while maintaining the same classification accuracy. Alternatively, the recovered SRAM can be used to process higher resolution inputs, boosting accuracy by up to +3.9% on Visual Wake Words.
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A DERIVATION RULES

A.1 Rule conditions

Each derivation rule listed in Table 2 has a number of conditions that need to be satisfied before the rule can be applied. Some conditions arise naturally from the pattern matching in the definition of the rule, e.g. ‘Partial Continue’ can only be applied to partially-materialised tensors in Mem.

\[ \text{requires the computation from tensors } A \text{ to } B \text{ (in a certain materialisation form) to be a valid transition in the network computation graph. If present, an operator } op \text{ is executed as a part of this transition.} \]

\[ \text{in Loop, No Loop} \text{ check if there is (or, respectively, is not) a partial execution loop currently being built } (C \neq \emptyset). \text{ The presence of partially-materialised tensors in Mem implies } \text{in Loop}. \]

\[ \text{A, C require the producing operator } (\text{‘op’}) \text{ of the considered tensor to be of the aggregating or channel-wise type, respectively.} \]

\[ \text{Eval} \text{ (can be evaluated) checks if an operator } \text{‘op’ with output } t \text{ can be executed within the current state. This is the case when } t \text{ is not a predecessor of (that is, } t \text{ is not required to compute) any other tensor in Mem (including itself in a different materialisation form). If ‘t’ were required to compute another tensor } t', op \text{ would have to be executed again in the computation path for } t', \text{ resulting in redundant computation.} \]

\[ \text{Comp. loop} \text{ (compatible loop) checks if the operator can be added to the current partial execution loop (trivially true for ‘Aggregate’ and ‘Post-Concatenate’, if there is no current loop) by checking if its inputs’ or output’s (as appropriate for the rule) channel dimensions match those of the current loop context tensors.} \]

\[ t \notin C \text{ checks if the tensor is not already in the loop context; used to remove trivial computation sequences (e.g. ‘Generate’ followed by ‘Post-Concatenate’).} \]

A.2 Rule intuition

Loop representation. The proposed scheduling algorithm evolves the memory state \((\text{Mem}, C)\) and attempts to create partial execution loops by introducing partially-materialised tensors \(i^p\) into Mem. The information about the current loop, if any, is represented by its \(i^p\)s in Mem. The loop context \(C\) is only used to store tensors of operators at the start or the end of the loop—those are tensors being repeatedly read from or written to, as loop execution proceeds. The context is completed and “flushed” (see “Loop End” rule) when the loop is finished (no \(i^p\)s remaining), and this complete context, returned through backtracking, is used to correctly measure the peak memory usage in the LOCALPMU helper function in Algorithm 1.

Loop correctness. The rule conditions ensure that only one loop is being built at a time (\([\text{Comp. loop}]\)), the loop building is not interrupted (\([\text{In/No loop}]\)), and the correctness of the underlying network computation graph ensures matching loop iteration dimensions as the scheduling algorithm attempts to continue the loop by applying “Partial Continue”, “Generate” and other rules.

Loop fusion. The scheduling can be alternatively cast a loop fusion problem. Code snippets for each operator can be transformed to perform channel computation at the outermost level and the scheduler must determine the (topologically-correct) order of such snippets, as well as which outermost loops can be fused, to minimise the peak memory usage. In the presented framework, the choice of whether to continue advancing the loop (producing \(i^k\)) vs closing it (producing \(i^k\)) and starting a new loop can be seen as a loop fusion decision.

Facilitating code generation. The primary purpose of the scheduling algorithm is to produce a list of instructions \(H\) that describe the sequence of how each operator should be executed (which rule) in a topologically-correct order. To facilitate code generation, a variety of auxiliary data is captured by the algorithm, such as the loop dimensionality and the complete loop context for each instruction. These two properties are shared by all instructions belonging to the same loop, which, by definition, must form a continuous sequence within \(H\). Upon encountering the first instruction of the loop, memory for loop context tensors is allocated (if not already present), and, similarly, context tensor memory is deallocated after the last introduction of the loop for any tensors not used later on.

B QUALITATIVE COMPARISON AGAINST PATCH-BASED EXECUTION

Instead of the channel axis \(C\), the computation can also be split along spatial axes \(H, W\). In MCU deep learning, patch-based execution is exemplified by MCUNet-v2 (Lin et al., 2021), and in the following, we discuss the advantages, disadvantages and trade-offs of the two approaches.

The performance is architecture-dependent. Results presented in Section 4.1 established that the improvement in memory usage depends on the underlying architecture. That is, it is not possible to conclusively argue that partial or patch-based execution always yields a greater improvement. The considered modifications to the MobileNet-v2 architecture are presented in Figure 5.
patch-based computation transitions between adjacent output “pixels” of a convolutional operator, it may use the same spatial regions of the input (overlapping receptive field) to obtain the output value. If the input patch is deallocated during this transition, this shared fraction of the input will have to be recomputed, leading to computational overheads (we refer to Lin et al. (2021) for a more detailed diagrammatic explanation of this issue). This can be partly alleviated by minimising overlapping input regions for patch-executed operators, which authors do both manually and automatically by searching and adjusting, among other parameters, strides, and kernel and patch sizes within the MobileNet-v2-based backbone. In contrast, our methodology does not result in any redundant computation (Constraint 5).

Both techniques suffer under unfavourable layer arrangements. We showcase an unfavourable case for both approaches: squeeze-excitation (SE) layers in state-of-the-art architectures, such as MobileNet-v3 (small, large) and EfficientNet-B0, which prevent both methods from achieving greater peak memory reduction.

Figure 6 shows the first six layers of the MobileNet-v3-small architecture, which contain squeeze-excitation layers: a global pooling layer (reduction along all spatial dimensions), followed by compression and expansion of the channel dimension using two fully-connected layers (‘squeeze’ and ‘excite’). Reduction across all spatial dimensions requires values from all input patches, which ends the patch-based execution span; similarly, the subsequent ‘squeeze’ layer requires values from all input channels, which terminates the current partial execution loop. Of course, a new partial execution loop can be started further in the network.

A straightforward workaround is modifying the architecture by removing the squeeze-excitation bottleneck from the high SRAM usage parts of the architecture. For example, a sibling architecture, MobileNet-v3-large, does not contain SE layers within the first three inverted residual blocks.

Greater memory reduction potential for very high spatial resolution low-channel layers with patch-based execution. When \( H, W \gg C \), patch-based execution offers a greater memory reduction potential: in the limit, \( 1/HW \) for a \( 1 \times 1 \) patch (and, in that instance, a significant re-computation overhead) versus \( 1/C \) for one channel. Therefore, some high-resolution computer vision neural networks, such as those processing aerial or medical imaging data, may benefit from patch-based execution more, depending on their architecture.

We also note that these approaches are not mutually exclusive: channel-axis partial execution can be applied within patch-based execution to reduce SRAM usage and enable the use of larger tiles, thus lowering the computation overhead. Both approaches can be unified within a more complex framework that jointly considers inter-operator tiling in spatial and channel dimensions.

The discussion above would suggest that channel-axis partial execution offers lesser peak memory usage gains at the benefit of no redundant computation and thus faster execution. We quantitatively examine this claim in Section 4 by evaluating both execution approaches on a high-resolution (for MCU applications) MobileNet-v2 model trained for ImageNet classification. Specifically, we:

1. quantitatively evaluate differences in peak memory usage and computation overhead for both approaches;
2. examine how these quantities change with minor modifications to the architecture that would make it more favourable to either approach.

Both techniques begin by partially consuming input

Patch-based execution span is forced to end at global pooling: all patches are required

All channels are required to compute the ‘squeeze’ layer, forcing the end of a channel-axis partial execution loop

Figure 6. Unfavourable layer arrangement of MobileNet-v3-small.

Figure 5. Modified versions of MobileNet-v2 which, compared to the original architecture, allow greater SRAM usage reduction within patch-based (left) or partial (right) execution (Table 3).
3. consider an automatically compressed model using structured pruning, instead;
4. check if the high-resolution input is actually necessary for the classification task at hand.

C ADJUSTMENTS FOR THE QUANTITATIVE COMPARISON AGAINST MCUNET

There are a number of adjustments that need to be made to the network performance and resource usage reported in the MCUNet-v1 and -v2 manuscripts for a fair evaluation.

Peak memory usage (MCUNet-v2 only). The numbers presented in Evaluation (Section 4 differ from the MCUNet-v2 manuscript, which departs from the evaluation settings of prior work, such as MCUNet-v1 (Lin et al., 2020), differentiable pruning (Liberis & Lane, 2021) or MicroNets (Banbury et al., 2020), by assuming that the full input tensor does not need to be stored in memory. Instead, compressed JPEG-encoded input ought to be available in memory for partial decoding. However, this assumption does not generally hold: while true for applications that have hardware with JPEG camera modules, it would not be the case for audio or sensor data processing applications. Compression of inputs and/or feature maps (and associated additional power usage and decoding overheads) is an interesting but, ultimately, tangential research direction to evaluating execution techniques, so we recompute patch-based execution memory usage within the same general environment for a fair comparison. For cases where the network architecture definition is not available, we assume that peak memory usage occurs in the patch-based execution stage and add the input size to the reported memory usage.

Classification accuracy on Visual Wake Words (VWW) (-v1 and -v2). The authors of VWW dataset provide training and validation data splits and suggest using the “minival” dataset (a small subset of the validation split) for final reporting. However, the “minival” happens to be a biased sample of the validation set, which results in noisier and inflated classification accuracy: models claiming to achieve >94% accuracy only achieve ≈90% on a larger validation set. Some prior work (Liberis & Lane, 2021; Banbury et al., 2020; Saha et al., 2020) uses the full validation set for evaluation, instead of “minival”. For MCUNet-v1, architecture definitions are available, allowing us to re-evaluate the models (and observe the accuracy disparity between the two evaluation sets). For MCUNet-v2, definitions are unavailable; thus we linearly extrapolate from MCUNet-v1 results, assuming both use the same training pipeline.

Miscellaneous differences.

- We note different classification accuracies for the ImageNet dataset (MobileNet-v2 performing at 72.2% in the MCUNet-v2 manuscript vs ours’ 71.5%) due to differences in the training pipeline. As these differences are under 1%, we consider them to be negligible.
- When the input resolution is not reported, we extrapolate from MobileNet-v2 results as to what input resolution would be appropriate to achieve reported resource usage or classification accuracy.

We acknowledge that differing evaluation assumptions and adjustments make the comparison challenging. Still, in the absence of other related work, we believe that the data reported here paint a fairer picture of the relative performance of partial and patch-based execution on common tasks.

D ARCHITECTURE RESOURCE USAGE

The following tables list detailed resource usage and classification accuracy data of models presented in Figure 4 in Section 4. As with the Figure, icons next model name represent ordinary execution (∗), partial execution (p), pruning-compiler co-design (×) or patch-based execution (□). MCUNet-v2 results are adjusted and estimated (†): see Appendix C.
### Properties of ImageNet models.

| Model               | PMU | Size   | MACs  | Acc.  |
|---------------------|-----|--------|-------|-------|
| ETinyNet x1.00      | 552 kB | 979 kB | 114 M | 61.7% |
| ETinyNet x0.75      | 452 kB | 660 kB | 69.7 M | 57.8% |
| MCUNet-v2 M4 [2], † | 273 kB | 1010 kB | 64.9% |
| MCUNet-v2 H7 [2], † | 616 kB | 2032 kB | 71.8% |
| MB-v2 (mod.) r172 [x] | 128 kB | 999 kB | 64.5% |
| MB-v2 (mod.) r256 [x] | 287 kB | 1994 kB | 69.8% |
| MCUNet-v1-S          | 333 kB | 748 kB | 67.4 M | 59.8% |
| MCUNet-v1-M          | 422 kB | 1757 kB | 67.4% |
| MCUNet-v1-L          | 192 kB | 1757 kB | 67.4% |
| MCUNet-v1-L [p]      | 341 kB | 756 kB | 61.0% |
| EfficientNet-B0      | 768 kB | 3987 kB | 69.2% |
| EfficientNet-B0 [p]  | 308 kB | 3987 kB | 69.2% |
| EfficientNet-B0 [x]  | 128 kB | 1999 kB | 65.4% |
| MBNet-v2 x0.5 r90    | 123 kB | 1990 kB | 65.4% |

### Properties of Visual Wake Words models.

| Model               | PMU | Size   | MACs  | Acc.  |
|---------------------|-----|--------|-------|-------|
| MicroNets VWW-1     | 200 kB | 616 kB | 71.6 M | 88.5% |
| MicroNets VWW-2 [p] | 27.9 kB | 103 kB | 3.38 M | 83.5% |
| MCUNet r144 [x]    | 270 kB | 657 kB | 55.9 M | 88.3% |
| MCUNet SFPS [x]    | 96.0 kB | 455 kB | 12.5 M | 86.1% |
| MCUNet 10FPS [x]   | 61.4 kB | 379 kB | 5.97 M | 85.2% |
| MCUNet-v2 [2], †   | 268 kB | unk. | unk. | ≈90.4% |
| MCUNet-v2 [2], †   | 139 kB | unk. | unk. | ≈89.2% |
| MB-v2 (mod.) r224 [x] | 89.6 kB | unk. | unk. | ≈86.4% |
| MB-v2 (mod.) r160 [x] | 223 kB | 1 MB | 209 M | 91.3% |
| MB-v2 (mod.) r96 [x] | 114 kB | 1 MB | 106 M | 89.8% |
| MB-v2 (mod.) r80 [x] | 40.8 kB | 1 MB | 37.7 M | 87.8% |
| MB-v2 (mod.) r80 [x] | 28.4 kB | 511 kB | 21.2 M | 87.0% |
| MB-v2 (mod.) r80 [x] | 27.6 kB | 128 kB | 11.8 M | 86.7% |
| MB-v2 r80 [x]      | 192 kB | 2.3 MB | 42.7 M | 87.4% |
| MB-v2 r96 [x]      | 276 kB | 2.3 MB | 55.1 M | 88.2% |
| MB-v2 r112 [x]     | 376 kB | 2.3 MB | 81.0 M | 88.6% |
| MB-v2 r128 [x]     | 492 kB | 2.3 MB | 97.9 M | 89.3% |
| MB-v2 r144 [x]     | 622 kB | 2.3 MB | 132 M | 89.9% |
| MB-v2 r160 [x]     | 768 kB | 2.3 MB | 153 M | 90.1% |
| MB-v2 r176 [x]     | 929 kB | 2.3 MB | 194 M | 90.6% |
| DiffPru, MB-v2 [x] | 198 kB | 606 kB | 58.3 M | 89.1% |
| DiffPru, MB-v2 [x] | 27.9 kB | 101 kB | 3.34 M | 83.8% |

### Properties of Speech Commands models.

| Model               | PMU | Size   | MACs  | Acc.  |
|---------------------|-----|--------|-------|-------|
| MicroNets-KWS-L [x] | 170 kB | 512 kB | 65.7 M | 96.5% |
| MicroNets-KWS-M [x] | 86.1 kB | 117 kB | 15.6 M | 95.8% |
| MicroNets-KWS-S [x] | 51.6 kB | 63.5 kB | 8.4 M | 95.4% |
| RES-8 [x]           | 23.7 kB | 112 kB | 4.16 M | 93.6% |
| RES-15 [x]          | 66.2 kB | 240 kB | 116 M | 96.8% |
| RES-15 [x]          | 44.6 kB | 240 kB | 116 M | 96.8% |
| RES-15 [x]          | 16.1 kB | 86.7 kB | 41.4 M | 96.5% |
| RES-15 [x]          | 16.1 kB | 55.8 kB | 26.6 M | 96.2% |
| MicroNets-L-Base [x]| 170 kB | 582 kB | 74.3 M | 96.9% |
| MicroNets-L-Base [x]| 69 kB | 582 kB | 74.3 M | 96.9% |
| MicroNets-L-Base [x]| 16.4 kB | 144 kB | 20.5 M | 96.1% |
| MicroNets-L-Base [x]| 16.3 kB | 88.6 kB | 12.5 M | 95.8% |
| DS-CNN-L [x]        | 86.9 kB | 420 kB | 28.3 M | 96.0% |
| DS-CNN-M [x]        | 54.2 kB | 140 kB | 9.83 M | 95.2% |
| DS-CNN-S [x]        | 16.0 kB | 24.3 kB | 2.66 M | 94.6% |