Design of Dual-channel HD Audio and Video Recording and Playback Equipment Based on TMS320DM8168

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Abstract. In order to meet the needs of dual-channel high-resolution audio and video recording, storage, and playback, as well as important control scenarios such as shipboard, vehicle, and airborne, the need for long-term capture and recording of terminal screen information is convenient for post-event technical analysis, Service quality assessment, exercise deduction, and operation accident responsibility identification. Researched the high-performance DaVinci series chip TMS320DM8168 launched by TI, designed and implemented a record playback device that supports dual-channel high-definition video, using the compression algorithm of the H.264 encoding standard to achieve compression and storage of video data, Use advanced and mature technology, follow the generalized, modular and serial design ideas to ensure better applicability and higher reliability. After the design was completed, the functions of video capture, compression encoding and video playback were verified, and the performance and stability were tested. The delay of video capture and display is within 40ms, The equipment can support high-definition single-channel or dual-channel video input, and realize two channels video information is compressed and stored, while the video decompression is stable, the playback picture is clear, and there is no jitter. The system functions and performance reach the expected goals.

1. Introduction

With the development of technology and the upgrading of video codec chips, audio and video monitoring and video image processing systems based on digital video technology are playing an increasingly important role in the civilian and military fields. In particular, the military control system display console, multi-sensor image capture and reproduction become more and more important, and for processing high-resolution video, multi-screen, low latency, long storage time, high compression ratio and equipment miniaturization of the device puts forward higher requirements [1]. This article considers these factors comprehensively, and designs a dual-channel audio and video recording and playback device based on TMS320DM8168.

2. System Design

The DM8168 hardware platform combines ARM and DSP, as well as two video processing VPSS-M3 and Video-M3 core quad-core processing systems. The HDVICP2 supports resolutions up to 1080 p/i with full performance of 60 fps (or 120 fields), which can support multi-channel high-definition video acquisition, encoding, decoding and display Support network transmission of video stream[2]. Equipment mainly includes: DSP processing module, audio and video acquisition module, main processing module, audio and video output module, storage module, Communication Interface Module, system clock, and power supply module, and the functional block diagram of the dual-channel audio and video recording and playback equipment system is shown in Figure 1.
The DM8168 processor platform can support 2-channel real-time H.264 high-definition video encoding and decoding, and provides a complete set of video pre-processing and post-processing mechanisms to ensure the quality of video images, and shorten the time of encoding and decoding operations to ensure the real-time video encoding and decoding performance, reduce system delay, and DM8168 has network transmission capabilities, can support long-distance transmission of video streams. The following describes the composition and function of each part [3].

2.1. DSP Processing Module
DSP uses TI’s TMS320DM8168 DaVinci video SoC. Compared with other DaVinci™ products, the DM8168 has a quad-core physical structure, supports higher ARM and DSP frequencies, and has 3 video coprocessors, which can adapt to most video processing requirements, and at the same time, a wider range of input and output support also provides advantages for the DM8168. As shown in Figure 2 Microprocessor Unit (MPU) Subsystem, The internal Cortex-A8 RISC CPU is an ARM7 architecture, supports integer and floating point operations, and has a built-in NEON processing unit. C674xDSP has 8000MIPS, 64 general 32-bit registers, 6 ALU functional units, and supports fixed-point and floating-point operations [4].

The DM8168 processor is powered on to obtain the startup configuration from the flash memory. The video acquisition chip is configured through the I2C interface to realize the compression, decompression, storage and other functions of audio and video data. During video recording, the video acquisition unit 4:2:2 YCbCr video signal, after image preprocessing, is H.264 encoded and stored on the SATA hard disk, and the H.264 video file is read from the SATA hard disk during video playback to complete the video Decompresses the H.264 video stream data to 4:2:2 YCbCr video data. In addition, it also provides a wealth of external communication interfaces for device debugging and external communication interfaces such as USB, RS232, RS422, CAN interface. Figure 3 shows TMS320C674x Megamodule Block Diagram.

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**Figure 1.** System functional block diagram

**Figure 2.** Microprocessor Unit (MPU) Subsystem

**Figure 3.** TMS320C674x Megamodule Block Diagram
2.2. Audio and Video Acquisition Module

The video capture module adopts the video graphics decoder ADV7604 from ADI. The maximum clock rate is 170MHz, which fully meets the decoding requirements of high-resolution UXGA (1600 × 1200 @ 60Hz) video signals [5]. After the system is powered on and reset, the DM8168 passes the I2C bus Configure the control register of the video decoding chip ADV7604. Audio collection uses the audio codec chip TLV320AIC3101, and the analog audio and video are decoded and sent to the DM8168 for signal compression and storage processing. Figure 4 shows the block diagram of the audio and video acquisition circuit.

![Figure 4. Audio and video acquisition circuit block diagram](image)

2.3. Audio and Video Output Module

The 4:2:2 YCbCr video signal output by DM8168 after decompression, the video conversion chip THS8200 converts the YCbCr video signal into a VGA signal, and outputs it to the display. The decompressed audio of DM8168 is output through the audio codec chip TLV320AIC3101, and the audio and video synchronization is adjusted by DM8168. The device selects the output through video or playback video through the video selection control signal. The video selection control signal is a switch state with self-locking, which needs to be controlled to high or low level inside the board. By reading this signal, the video recording module selects the video output to be through video or playback video, Figure 5 shows the Audio and video output module circuit block diagram.

![Figure 5. Audio and video output module circuit block diagram](image)

2.4. Storage Module

The storage module includes two 4Gb DDR3 MT41K256M16TW, one NANDFLASH chip MT29F2G16ABAEAWP and a 1T SATA interface solid state hard disk. The NAND Flash chip uses Micron's MT29F2G16AAABWP chip with a capacity of 2Gb. It is mainly used to store the BOOT configuration file of the processor. After power-on, the processor obtains the startup configuration program from NAND. The DDR chip uses Micron's MT41J128M16JT-093J. The chip has a capacity of 256MB. It uses 4 parallel modules in the module with a total capacity of 1GB. It is used for data
buffering for algorithm processing. The SATA interface solid-state hard drive is used to store two-way compressed video files. The storage strategy is that when the storage space of the SATA hard drive is full, the video files stored earlier are overwritten cyclically. After the video with 1600x1200 resolution is compressed, the code rate is adjustable from 1Mbps to 10Mbps, and the two channels of video can be recorded for a maximum of about 150hours[6].

2.5. Communication Interface Module
DM8168 provides external communication interfaces such as I2C, 100M Ethernet, USB, RS232, USB, etc. It is used for system software function debugging and communication interaction with the host computer. JTAG interface for DSP program download as well as online simulation.

2.6. Power Module
The power supply module provides the working voltage required by each piece of the system. The entire system is powered by DC 5V power supply, and then the working voltage of DM8168 and peripheral circuits is generated by 5V. Through the design of hierarchical sub-modules, the system can provide a stable working voltage while ensuring the power-on sequence and ensure the reliable operation of the system. The system uses a ±12V power supply to convert the power supply to the required 3.3V / 1.8V / 1.5V / 1V / 0.9V and other power supplies[7], as shown in the figure6. Figure 7 shows the power-on sequence of each voltage in the system.

2.7. System Clock Design
The system uses a 27MHz crystal to access the internal oscillator circuit of the processor as the system clock of the processor. The main frequency and the external interface clocks can be obtained by multiplying or dividing the frequency through the processor's own phase locked loop. In addition, the SATA interface is a 100MHz differential clock, and the external 32.768kHz clock is the reference clock of the timer module, which needs to be provided separately[8]. As shown in the figure 8, it is designed for the system clock.
3. System Software Design

3.1. Multi-core Scheduling
DM8168 integrates four core processors, one Cortex-A8 ARM, one C674x DSP and two Cortex-M3. The four physical cores are respectively responsible for different functions. The Cortex-A8ARM core is mainly responsible for system control and communication between various coprocessors. The C674x DSP core is used to implement user-defined algorithms and supports dynamic scene detection and foreign object intrusion detection, Surveillance and other video processing algorithms; two Cortex-M3 processors are HDVICP2 and VPSS-Media Controller, HDVICP2 core has three high-definition video image coprocessors, responsible for completing video codec function; VPSS-Media Controller is used for control High-definition video processing subsystem, responsible for completing video capture, display and some processing functions[9].

![Figure 9. IPC Overview Diagram](image.png)

As shown in the figure 9, the main processor of DM8168 is Cortex-A8, which usually loads and loads each slave processor (Video-Media Controller, VPSS-Media Controller, C678xDSP), and the HDVICP2 core is managed by Video-Media Controller. Different processing units of SoC use different IPC (Interprocessor Communication) methods, and simplify the IPC mechanism through Mailbox and Spinlock hardware. Mailbox provides a mechanism for processors to send interrupts to other processors by writing registers. A8, C674x DSP and Media Controller communicate through the system's Mailbox (IPC). The three HDVICP2s IP modules have their own independent Mailboxes, and through spinlock (Spinlock) it is convenient to realize the mutual exclusion of system shared resources.

3.2. Embedded Graphical Interface Design
After the system is started, VGA and audio are not collected, and VGA is not output. When receiving the "mode switching" network command message, it enters "playback mode" and the video is immediately output from the 2 VGA channels. The VGA output screen enters the playback mode interface. The playback mode interface is divided into four levels. The first three levels are the folder operation interface and the player interface. In playback mode, all levels of interfaces can support mouse pointer movement and mouse events through the network. And by operating the mouse, you can enter the corresponding folder, play audio and video files. When the "Exit" softkey is clicked, the VGA output is cut off immediately, waiting for subsequent network command messages. Figure 11 shows the process of interface operation, Figure 10 shows the design of a four-level embedded graphical interface.
4. Design and Implementation

The equipment has been designed with a visual embedded graphical interface. As shown in Figure 11, through video selection control signals to achieve the selection output of direct video and playback video, the design of an embedded built-in player is adopted. Only two display terminals are needed to realize the output display of two channels of high-definition straight-through video and playback video. It has strong versatility, easy operation, and friendly man-machine interface.

In this design, when the video selection control signal is low, it enters the "playback mode" graphical interface. The playback player interface design, as shown in Figure 12, includes a borderless video display area, pause and play switches, and progress bar drag, Previous and next video switching, volume adjustment and other playback control toolbars, the control toolbar has the functions of hiding and exiting the player. When the video cannot be played or the video playback is completed, exit the player and return to the "audio and video three-level interface". When the mouse is not operated, the player's control panel is automatically hidden after 3 seconds, and the control panel automatically appears after the mouse slides.
5. Conclusion

The equipment integrates video acquisition, encoding and decoding, and can realize the recording, storage and playback of high-definition dual images. Through the design of the embedded built-in player, only two display terminals are needed to realize the output display of two channels of high-definition direct video and playback video. The video codec delay is within 40ms, the code rate is adjustable from 1Mbps to 10Mbps, and there is no frame loss, jitter, flicker, and lag in the video acquisition process. The product has the characteristics of low power consumption, low delay, high definition, friendly man-machine interface, strong versatility, long storage time, adjustable compression rate, high reliability, etc., and has now achieved mass production and promotion and application. With the further optimization of the embedded software interface design and the further improvement of performance, the application range will be more and more wide in the scenes that require audio and video recording, such as vehicle, ship, and airborne.

6. References

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