An Embedded System Processor Module with PCI Bus and Universal Communication Interface Based on PowerPC

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Abstract. In the high level applications of embedded systems such as Internet and data communication, the processor is an indispensable core module as the center of communication and control. An embedded system processor module with PCI bus and universal communication interface based on PowerPC is proposed in this paper. The central processor uses the Freescale PowerPC family of superscalar microprocessors with processing power of up to 733MIPS@400MHz. The microprocessor and peripheral conversion uses a bridge/memory controller that is seamlessly connected via a 60x bus. Regular large-capacity storage units such as SRAM, SDRAM, flash, and boot ROM are supported. Universal communication interfaces such as PCI bus interface, I²C bus interface, dual UART interface (RS485 level + RS232 level), Gigabit Ethernet interface, etc. are provided. The processor module has the characteristics of strong processor computing capability, common external interface and wide application, and could be directly used by developers, so that could shorten the development cycle.

1. Introduction

In various high level applications of internet and data communication, the processor is an indispensable core module as the center of communication and control. Freescale PowerPC series high-performance CPUs, such as MPC824x, MPC750 and other embedded CPUs, are widely used in various fields such as Internet, communication, and signal processing, because of its excellent performance, low energy loss and low heat dissipation.

It point out the great advantages and application potential of PowerPC in large data volume and high speed signal processing, based on the performance comparison and analysis between PowerPC chip and common DSP chip in Reference [1]. The design and implementation of a PowerPC-based embedded MPEG4 video decoder is studied in the reference [2]. The design and implementation of active radar signal processing software based on PowerPC is presented in the reference [3]. The PowerPC-based micro grid intelligent terminal design is studied in the reference [4]. The design proposals presented in the previous literature all utilize PowerPC to solve various specific problems such as internet, communication, and signal processing. However, due to the complex technology of the processor module and numerous interfaces, the technical difficulty and cost of the development are greatly increased.

Therefore, the research about embedded system processor module based on the Freescale PowerPC, which provides high-performance processors and a variety of common communication interfaces, such as PCI bus interface, I²C bus interface, Ethernet interface, dual UART interface (RS485 level + RS232 level) etc., would be important for satisfying various high-end applications of Internet and data
communication and shortening the development cycle. It is useful to design high-performance processor general-purpose modules, which free developers from complex processor design work, focus only on the design and application of peripheral circuits. Then it would reduce the time and potential for error in processor-partial debugging, and speed time to market and reduce total cost and provide outstanding scalability. The results could be widely used in signal processing, wireless LAN, routers/switches, embedded calculators, multi-channel modems, network storage, RAID system disk controllers, and more.

2. The System Design For Embedded System Processor Module

Freescale PowerPC high-performance processors, such as the MPC750+MPC107 combination\cite{5,6}, are used as the control center, which provide PCI controllers, memory controllers, dual UART controllers, and Ethernet controllers, as shown in Figure 1. The PCI controller is used to provide a PCI bus interface, and the Ethernet controller is connected to the PCI bus for providing an Ethernet communication interface. The storage controller is connected to the peripheral memory. And the dual UART controller is connected to the local bus for providing a two-channel UART communication interface. The system supports conventional large-capacity storage units such as SRAM, SDRAM, flash, and boot ROM, which provide storage applications for various needs. The solution also provides an I2C bus interface, which is connected to the central control unit to provide an I2C standard communication interface.

![Diagram](image)

**Figure 1**: the system design for embedded system processor module

3. The Design For Microprocessor

The CPU system shown in Figure 1 uses the combination of the Freescale MPC750 series RISC microprocessor and MPC107 PCI bridge/memory controller with a maximum operating frequency of 400MHz and a processing capacity of 733MIPS (processing millions of instructions per second)@ 400MHz, which can be used in mid- to high-end applications. The MPC750 Series RISC microprocessors feature a high-performance, low-power, 32-bit Reduced Instruction Set Computer (RISC) architecture that enhances performance for embedded applications, delivery three instructions per clock cycle (two quality + one branch ) to 6 independent execution units (branch processing unit, two integer units, load/store unit, double precision floating point unit, system register unit). Multiple instructions can be executed in parallel, pipelined to deliver instructions, and fast-reduced instructions with fast execution times to maximize system efficiency and throughput. Dedicated L2 cache interface (up to 1MB) supports direct mapped SRAM mode, physically mapped SRAM mode, a fast (general 1/2 core speed) interface for connection memory, instruction mode only or data mode only, and parity for L2 address and the data. The one side of MPC107 is a 60X bus interface, with the bus width 32-bit/64-bit selectable, the highest frequency up to 100MHz, and the 60X bus is seamlessly connected to the MPC750 CPU, and the other side is the PCI bus interface. The MPC107 integrates memory controller, DMA controller, programmable interrupt controller, 4 timers, I2C unit, message unit (I2O),
PCI arbiter, watchdog circuit, dynamic power management unit, PCI bus performance monitoring unit, etc.

The central processor system can also use other integrated microprocessors that integrate CPU and bridge. For example, the Freescale MPC8240 family of integrated microprocessors not only integrates the MPC603E microprocessor core, but also integrates a 32-bit PCI host bridge with a 64-bit bus SDRAM controller. The MPC603E microprocessor core integrates functions such as floating point units, run/store units, and system register units. The MPC8240 series integrated microprocessor provides a standard PCI interface, supports up to 272MB ROM, 2GB SDRAM, and supports dual boot ROM. The maximum operating frequency is 266MHz, and the processing capacity is 488MIPS@266MHz, which is suitable for low-end and mid-range applications.

4. The Design For Local Bus

The local bus is 64 bits wide and is controlled by the MPC107 bridge/storage controller, as shown in Figure 2. SDRAM, FLASH, boot ROM and other memories are connected to the 64-bit local bus of the processor. The dual UART controller uses the ST16C552, one of which uses RS232 level and the other uses RS485 level to meet different communication applications. Boot ROM, flash ROM, SDRAM and other memories are used to provide storage components required for the operation of the processor. The boot ROM is used to read the minimized boot program when the central processor starts, and the flash ROM is used to read and run the program after startup. SDRAM with 64-bit width is used for temporary data storage control while the central processor is running. The system supports up to 1G bytes of DDR SDRAM memory capacity, 144M bytes of Flash ROM capacity, and 1M bytes of Boot ROM capacity.

The dual UART controllers use the chip ST16C552 and is connected to a 64-bit local bus to provide a two-channel UART communication interface. One of the UART controllers uses an external PHY device RS232 level conversion chip ADM3202ARN to provide RS232 level standard debugging interface for short-distance, low-speed serial communication, for example, for online debugging with a computer serial communication port, and the interface signals are RS232_TX and RS232_RX. Another UART controller is directly connected to the daughter card socket for the motherboard to use RS485 level for long distance, higher rate serial communication, and the interface signals are RS485TX, RS485TEN, RS485RX, RS485REN.

5. The Design For PCI Bus And Ethernet Communication Interface

The solution provides a PCI bus interface and an Ethernet communication interface, as shown in Figure 3. The Ethernet controller is externally connected to an Ethernet transformer for providing a 10M/100M/1000M adaptive Ethernet communication interface.
In this solution, the PCI controller is used to provide a PCI bus interface, and the interface signals are P_CLK, P_IDSEL, P_IDSEL2, P_INT<3..0>, P_REQ<3..0>, P_GNT<3..0>, REQ2, GNT2, P_FRAME, P_DEVSEL, P_IRDY, P_LOCK, P_PAR, P_TRDY, P_PERR, P_STOP, P_SERR, P_CBE<3..0>, P_AD<31..0>. The solution is compatible with the PCI2.2 specification, supports 32-bit bus, supports up to 66 MHz, supports up to 5 PCI devices, and requests and permits through REQ<4..0> and GNT<4..0>. Working in PCI main mode or PCI slave mode is supported, and the specific implementation method is:

When operating in PCI master mode (PCI_MODE = 0), P_REQ<3..0>, P_GNT<3..0> are used for external PCI devices. P_REQ4/P_GNT4 is used for the Intel 8254x Gigabit Ethernet controller of the PCI device inside the module.

When working in PCI slave mode (PCI_MODE=1), P_REQ3/P_GNT3 is used for the MPC107 to apply for bus usage rights to the master PCI, and REQ2/GNT2 is used for the Ethernet controller Intel8254x to apply for bus usage rights to the master PCI.

The Ethernet controller uses the Intel Gigabit Ethernet Controller 8254x and is attached to the PCI bus to provide an Ethernet communication interface[9]. The AT93C42 is an EEPROM that stores the MAC address of the Ethernet controller Intel8254x and is connected to the Intel8254x via a communication serial port. An external 1000M Ethernet transformer can provide 10M/100M/1000M adaptive Ethernet communication interface. The interface signals are MDI[0]+, MDI[0]−, MDI[1]+, MDI[1]−, MDI[2]+, MDI[2]−, MDI[3]+, MDI[3]−.

6. The Design For External Input / Output Signals
The externally inputs/outputs general interface signals in the processor module, including system control signals, PCI bus signals, I2C bus signals, Ethernet communication signals, serial communication signals, a total of five kinds of signals. Each input/output signal definition is fully compatible with industry specifications or standards such as PCI2.2, I2C, Ethernet 802.3, RS232/RS485. The specific signal definition is shown in Table 1.

Table 1 | module external common interface signal definition |
| --- | --- | --- | --- |
| Signal category | Signal symbol | Feature | Remarks |
| System control signals | S_RST | A signal indicates system reset | When the module is used alone, it uses the clock inside the module. When the module is inserted into the motherboard, it uses the clock of the motherboard. |
| S_CON | A signal indicates that the module is plugged into the motherboard |  |
| P_RST | A signal indicates PCI reset |  |
| PCI_MODE | A signal indicates the | 0 indicates PCI master; |
| Signal            | Description                                                                                              | Notes                                      |
|-------------------|----------------------------------------------------------------------------------------------------------|--------------------------------------------|
| CLK_S             | A signal indicates Clock selection 0 indicates the selection of the module clock 1 indicates the selection of the motherboard clock |
| P_CLK             | PCI clock                                                                                                | Up to 66MHz                                |
| P_IDSEL           | PCI selection signal for the MPC107/MPC8240 when used as a PCI slave                                     |                                            |
| P_IDSEL2          | Another PCI selection signal for Intel 8254x when used as a PCI slave                                     |                                            |
| P_INT<3..0>       | Signals indicate PCI interrupt request                                                                   | up to 4 signals                            |
| P_REQ<3..0>       | Signals indicate PCI bus request                                                                     | up to 4 signals                            |
| P_GNT<3..0>       | Signals indicate that the PCI bus are licensed                                                           | up to 4 signals                            |
| REQ2, GNT2        | When working in PCI slave mode, the Intel 8254x Ethernet controller in this module use these signals to request the bus usage right to the master PCI. |                                            |
| P_FRAME, P_DEVSEL, P_IRDY, P_PAR, P_TRDY, P_PERR, P_STOP, P_SERR, P_CBE<3..0>, P_AD<31..0> | PCI bus control signals, address signals, data signals                                                 |                                            |
| I2C_SCL, I2C_SDA   | I2C Bus clock signal, I2C Bus data signal                                                               |                                            |
| MDI[0]+, MDI[0]-, MDI[1]+, MDI[1]-, MDI[2]+, MDI[2]-, MDI[3]+, MDI[3]- | 10M/100M/1000M adaptive Ethernet communication differential pair signals                              |                                            |
| RS232_TX, RS232_RX | RS232 serial communication signals                                                                     | RS232 level is provided by this module    |
| RS485TX, RS485TX, RS485TEN, RS485RX, RS485REN | RS485 serial communication transceiver enable signals                                                   | RS485 level is provided by the motherboard |

7. Conclusions
An embedded system processor module based on PowerPC with PCI bus and universal communication interface has a processing capacity of up to 733MIPS@400MHz. It not only provides a complete internal CPU and memory systems, but also provides a standard external interface of PCI bus, Ethernet, serial communication signals, I²C bus, etc. Therefore, during the project development
process, the time spent on processor debugging and possible errors can be reduced, so that the research and development personnel can specialize in the peripheral circuit design, and the design and development cycle could be greatly shortened.

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9. References
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