Abstract—In this article, a dc-link structure feasible for integration with the circumscribing polygon modular integrated drives is proposed. The proposed dc-link structure combines both the dc-link capacitors and the bus-bar together and integrates them with the machine and the converter modules without increasing the outer diameter of the integrated machine/converter structure. A generic design methodology for the proposed dc-link structure is provided and applied on a reconfigurable 15 stator coils concentrated winding axial flux machine for all its possible phase configurations. The design methodology presented in this article involves the determination of the required dc-link capacitance and the multiphysics design of the bus-bar. The parasitics of the bus-bar part of the proposed dc-link structure are evaluated using electromagnetic finite element method (FEM) models and their influence on the dc-link waveforms is evaluated. Due to the expected high ambient temperature inside an integrated drive, electromagnetic and computational fluid dynamics (CFD) models are developed for the proposed dc-link structure to evaluate the loss density and the temperature distribution of the bus-bar to ensure reliable operation. An experimental setup is built to validate the design methodology.

Index Terms—Bus-bar electromagnetic modeling, bus-bar thermal modeling, dc-link bus-bar, dc-link capacitors, dc-link voltage spike, integrated modular drives, parasitic inductance, wide bandgap (WBG) converters.

I. INTRODUCTION

INTEGRATED modular motor drives (IMMDs) represent a modularized and physically integrated machine, power converter, and dc-link structure [1]. IMMDs provide the advantages of high fault tolerance and high power density compared to the conventional drives [2], [3]. The high fault-tolerance results from the redundancy and the flexibility in dividing and configuring the stator modules to maximize the torque that can be generated at a certain fault. The high power density and compactness of the drive results from the elimination of the converter separate housing and the cables connecting the converter to the machine [4].

Many challenges have to be met for the realization of an IMMD. Among these challenges, the small space available for the converter modules has to be efficiently utilized by optimal selection of the converter components, especially the dc-link capacitor as it represents the bulkiest component in the converter module [5] beside the heatsink. One more challenge is the high thermal stresses that the converter switches and capacitors will be exposed to due to their close proximity to the major heat sources in the machine [6].

The small space and the thermal challenges of the integrated drives can be met by utilizing the wide bandgap (WBG) semiconductor devices such as the gallium nitride (GaN) and silicon carbide (SiC) in the implementation of the converter modules due to their lower losses, higher thermal conductivity, and smaller package size for the same voltage and current rating compared to the silicon (Si) devices [7]. Using WBG devices makes it possible to switch with higher frequency than the Si case which results in smaller dc-link capacitance [8].

IMMDs are classified according to the location of the power converter modules with respect to the machine housing and the stator elements into axially stator iron mounted (ASM), radially stator iron mounted (RSM), axially housing mounted (AHM), radially housing mounted (RHM) [9], and circumscribing polygon (CP) integration topology [10]. The RSM, ASM, and CP provide a more compact integrated drive with higher cooling design challenges.

In this article, a dc-link structure feasible for physical integration with CP modular integrated drives is proposed. This dc-link structure combines both the capacitors and the bus-bar. Besides the possibility of the physical integration with the integrated machine/converter structure, the proposed dc-link structure in this article provides four more advantages. The first one is that the proposed dc-link structure does not increase the outer diameter of the integrated machine/converter structure which results in a more compact integrated structure. The second one is that it has a small parasitic inductance from the capacitor terminals to the converter dc input terminals which reduces the voltage spike on the converter switches. The third one is that it has a relatively high inductance from the dc-source input terminals to the capacitor terminals which further smooths the
current supplied from the dc-source reducing the electrical and the thermal stresses on it. The fourth one is that the bus-bar part is easy to manufacture and the capacitors are chosen off the shelf and there is no need for the time-consuming and the expensive custom designed dc-link structure as proposed in [11].

The authors in [5], [12], and [13] address the design of the dc-link capacitor for three phase drives with a single set of stator winding. The authors in [14] and [15] handle the influence of the pulsewidth modulation (PWM) carriers interleaving on the design of the capacitor of the three phase drives with dual stator winding. In [16], the authors illustrated the possibility of using carrier interleaving with IMMDs, but no closed-form generic design equations are given. In [10], the authors presented generic analytical design equations for the dc-link capacitors of the reconfigurable IMMDs. These equations are adopted in this article.

The dc-link bus-bar connects the dc-source, the capacitors, and the converter modules together [17]. In [18]–[21], the authors study the influence of the bus-bar geometry for three phase inverters implemented using commercial half-bridge modules on the value of the parasitic inductance. Lacking in literature is a comprehensive study for an integrated bus-bar structure feasible for IMMDs given their special structure and high ambient temperature.

In this study, a generic design methodology for the proposed dc-link structure feasible for reconfigurable modular integrated drives is provided and applied on a 15 stator coils CP integrated axial flux drive. The design process presented in this article involves the determination of the required dc-link capacitance for each configuration and the multiphysics design of the bus-bar. An electromagnetic finite element method (FEM) model and computational fluid dynamics (CFD) model are developed for the proposed dc-link structure to ensure that the electrical and the thermal stresses on the components of the dc-link structure are within the rated values.

The electromagnetic FEM model is used to extract the dc-link structure parasitics so that the dc-link voltage spike can be estimated and to compute the loss density distribution in the bus-bar. This loss density distribution is used as an input to a CFD model for the dc-link structure to compute the temperature distribution. In this way, both the electrical and the thermal stresses on the bus-bar can be evaluated to ensure reliable operation in the high ambient temperature environment of the integrated drive.

The article is organized as follows. Section II provides a brief description of the CP integrated drive for which the dc-link structure is designed and analyzed. In Section III, the mechanical construction of the proposed dc-link structure is explained. Section IV discusses in detail the design of the proposed dc-link structure. The experimental setup and results are given in Section V. Section VI concludes this article.

II. STRUCTURE OF THE CP IMMD

The integrated dc-link structure proposed in this article is applied on an IMMD with 15 stator coils with CP integration of the power converter modules [10]. Fig. 1 shows the construction of this CP integrated drive. The drive combines the electric machine, the power converter modules, the shared cooling structure, and the dc-link structure. The polygon-shaped shared cooling structure with the converter modules mounted on top is illustrated in Fig. 2. Table I contains the main specifications of this integrated drive topology.

Each converter module has a size of 60 × 40 mm² and is capable of providing up to 1.13 kW. The converter is implemented using GaN technology. Fig. 3 shows a picture of the implemented GaN-based half-bridge module.
TABLE I
KEY SPECIFICATIONS OF THE INTEGRATED DRIVE

| Quantity                  | Value  |
|---------------------------|--------|
| rated power (kW)          | 17     |
| rated speed (rpm)         | 2500   |
| # pole pairs              | 8      |
| # slots                   | 15     |
| axial length (mm)         | 60     |
| outer diameter (mm)       | 190    |
| converter module size (mm²) | 60×40 |

Fig. 3. GaN-based half-bridge module.

Fig. 4. DC-link structure. (1) Bus-bar structure. (2) DC-link capacitors.

III. MECHANICAL CONSTRUCTION OF THE INTEGRATED DC-LINK

Fig. 4 shows the construction of the proposed dc-link structure. It consists of a ring-shaped bus-bar with the dc-link capacitors arranged circumferentially pointing radially inward. In this way, the bus-bar and the capacitors are integrated with the machine/converter structure without increasing the outer diameter which enhances the compactness of the drive.

Fig. 5 shows an exploded view for the bus-bar part of the dc-link structure. It consists of a positive plate, a negative plate, and an electrical insulation layer between them. Each plate has an input tab for the dc-source, a connection terminal for the module capacitor, and a connection terminal for the converter input source. A short distance of 17.5 mm between the capacitor terminal and the converter dc-input terminal is achieved which results in a small ac parasitic inductance and, hence, small switches voltage spike. A relatively longer average distance of 115 mm between the dc-source input tab and the converter input terminal is achieved which results in a relatively greater dc parasitic inductance, and, hence, a smoother dc-source current and smaller dc-source stress will result.

The conducting plates can be made of copper or aluminum. Using aluminum plates results in a lighter drive due to the smaller mass density of aluminum compared to copper, but higher loss and temperature will result due to the smaller electrical and thermal conductivity of the aluminum. The insulation layer can be made of kapton, mylar, nomex, or epoxy glass (FR4). Table II contains the main properties of the insulation materials. Here, $E$ is the breakdown strength, $\epsilon_r$ is the relative permittivity, and $K_{th}$ is the thermal conductivity. As the maximum bus-bar temperature is limited by the rated temperature of the insulation layer, kapton represents the optimal choice from the thermal point of view.

IV. DESIGN OF THE DC-LINK STRUCTURE

The design of the integrated dc-link structure involves the determination of the dc-link capacitors for each possible configuration of the modular drive and the multiphysics analysis of the mechanical outline of the integrated bus-bar part of the dc-link structure.

TABLE II
PROPERTIES OF INSULATION MATERIALS

| Material | $E$ (kV/mm) | $\epsilon_r$ | rated temperature (°C) | $K_{th}$ (W/m.K) |
|----------|-------------|--------------|-------------------------|------------------|
| Kapton   | 196         | 3.7          | 400                     | 0.4              |
| Mylar    | 295         | 3.3          | 105                     | 0.14             |
| Nomex    | 17.33       | 1.6          | 220                     | 0.157            |
| FR4      | 49          | 4.3          | 140                     | 0.31             |
A. Selection of the DC-Link Capacitors

By proper dc-link voltage scaling and stator coils connection, the 15 stator coils of the integrated drive in Fig. 1 can be configured to operate as 3-phase, 5-phase, or 15-phase drive [10]. In case of three-phase operation, five stator coils are connected in series to form one phase as in Fig. 6. In case of five-phase operation, three coils are connected in series to form one phase as in Fig. 7. In case of 15-phase operation, the stator coils can be connected to have one common neutral point as in Fig. 8, divided into five groups with three coils in each group as in Fig. 9 or divided into three groups with five coils in each group as in Fig. 10. For the connections in Figs. 9 and 10, the PWM carriers can be shifted by an interleaving angle $K$ to further reduce the dc-link current stress. Each configuration has its own torque-speed and fault-tolerance characteristics.

Equations (1) and (2) can be used to calculate the dc-link capacitor harmonic currents while (3) and (4) can be used to estimate the value of the needed dc-link capacitance [10]. The equations are valid for each possible configuration of the reconfigurable modular drives. The dc-link capacitance requirement of the reconfigurable drive in Fig. 1 is calculated for each configuration considering 400-V dc-link voltage in case of three-phase operation. For the other configurations, the dc-link voltage is adjusted to keep the phase current and power the same. The design is performed for 1% $V_{pp}$ ripple. Table III contains the calculated dc-link capacitance requirements per module for each

| Variable                        | Connection | Value   |
|---------------------------------|------------|---------|
| Minimum rated voltage (V)      | 3-ϕ        | 400     |
|                                 | 5-ϕ        | 240     |
|                                 | 15-ϕ       | 80      |
|                                 | 5×3-ϕ      | 80      |
|                                 | 3×5-ϕ      | 80      |
| Minimum ripple current rating (A)| 3-ϕ      | 1.92    |
|                                 | 5-ϕ        | 1.8     |
|                                 | 15-ϕ       | 1.75    |
|                                 | 5×3-ϕ      | 0.3     |
|                                 | 3×5-ϕ      | 0.4     |
| Minimum capacitance (μF)       | 3-ϕ        | 2       |
|                                 | 5-ϕ        | 3.2     |
|                                 | 15-ϕ       | 9.5     |
|                                 | 5×3-ϕ      | 0.5     |
|                                 | 3×5-ϕ      | 0.65    |
configuration.

\[ i_{ch}(n, m) = \frac{i_{\text{linepeak}}}{2\pi^2} \sum_{x=1}^{N} \sum_{h=1}^{g} \int_{y_{\min}}^{y_{\max}} f(x, y) dy dx \]

where \( i_{ch}(n, m) \) is the capacitor’s peak harmonic current at harmonic order \( m \) and its side-bands \( n \) around the inverter output fundamental frequency \( f_s \). \( i_{\text{linepeak}} \) is the peak output current of the inverter, \( g \) is the number of groups, \( N \) is the number of phases, \( \phi \) is the phase shift between the fundamental output voltage and the fundamental output current of the inverter, \( \theta \) is the electrical phase shift between the phases, \( K \) is the interleaving angle, \( m_{md} = \frac{L_{ac}}{f_s} \) is the harmonic order of the capacitor’s most dominant harmonic current component, \( f_s \) is the switching frequency, \( f_{md} \) is the frequency of the capacitor’s most dominant harmonic current component, \( I_{mdc} \) is the capacitor’s equivalent most dominant harmonic current, \( V_{\text{ppripple}} \) is the peak to peak capacitor ripple voltage, and \( C_{\min} \) is the minimum required dc-link capacitance.

The film capacitor FB27A6J0335 from AVX with the specifications in Table IV is selected for the capacitor module.

As the ambient temperature inside an integrated drive is expected to be high, the calculation of the capacitor power loss and hot spot temperature is crucial. Equation (5) can be used to calculate the power loss and the hot spot temperature of the capacitor. The worst-case module capacitor loss is calculated to be 0.0814 W which means a temperature rise of 2.3 °C above the ambient. Note that this small loss results thanks to the modular construction of the drive that divides the dc-link current ripple over the capacitor modules.

\[
\begin{align*}
  P_d &= \frac{1}{2} C \tan(\delta) \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} V_{\text{pp Ripple}}^2 f_h \\
  P_t &= \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} I_{\text{chrms}}^2 (n, m) \\
  \theta_{\text{hotspot}} &= \theta_{\text{ambient}} + (P_d + P_t) R_{th}
\end{align*}
\]

Table IV

| Variable                  | Value  |
|---------------------------|--------|
| rated voltage (V)         | 550    |
| rated rms ripple current (A) | 5      |
| capacitance (µF)          | 3.3    |
| ESR (mΩ)                  | 22     |
| tan(δ)                    | 2e-4   |
| thermal resistance \( R_{th} \) (°C/W) | 27.3 |
| rated hotspot temperature (°C) | 100  |
| ESL (nH)                  | 25     |

B. Electromagnetic Analysis of the Bus-Bar

The electromagnetic analysis is performed for two purposes. The first one is to evaluate the dc-link parasitics [17] so that the electrical stresses over the bus-bar insulation and the converter switches can be evaluated. The second one is to evaluate the electromagnetic loss density distribution over the bus-bar due to the dc and the ac currents so that the temperature distribution over the bus-bar can be evaluated.

1) Bus-Bar Parasitics and Electrical Stresses: Fig. 11 shows the per module equivalent circuit of the dc-link structure in Fig. 4. The values of the parasitic components of the dc-link structure are computed using electromagnetic FEM and listed in Table V as per module values. The values are computed for 1-mm-thick copper and aluminum plates considering a 1-mm Kapton insulation layer. \( L_{ac} \) is the plate parasitic inductance from the capacitor terminals to the converter module input terminals. \( L_{ac} \) and equivalent series inductance (ESL) constitute a part of the commutation loop inductance.

Due to the high transition speed of the GaN switches [9], any small parasitic inductance in the commutation loop contributes considerably to the voltage stress on the switches and the bus-bar insulation during turn-off transition of the switches. The switch voltage spike above the dc-link voltage can be estimated from

\[
\begin{align*}
  V_{\text{linepeak}} &= \frac{1}{2} C \tan(\delta) \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} V_{\text{pp Ripple}}^2 f_h \\
  P_t &= \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} I_{\text{chrms}}^2 (n, m) \\
  \theta_{\text{hotspot}} &= \theta_{\text{ambient}} + (P_d + P_t) R_{th}
\end{align*}
\]
To illustrate the influence of the parasitics on the module terminals voltage stress, the circuit in Fig. 11 is simulated considering the three-phase configuration of the drive and the dynamic model of the GaN switch GS66508B used in the implementation of the converter. Fig. 12 (left) shows the resulted converter module terminal voltage; a spike of 73 V above the 400-V dc voltage can be observed. Since the peak voltage is 473 V, this can still be tolerated by the switches and the bus-bar insulation.

\[
V_{\text{spike}} = L_{\text{loop}} \frac{di_a}{dt} \\
L_{\text{loop}} = 2L_{\text{ac}} + ESL + L_{\text{PCB}}
\]

(6) where \(V_{\text{spike}}\) is the switch spike voltage, \(i_a\) is the transistor current during commutation, and \(L_{\text{PCB}}\) is the printed circuit board (PCB) inductance.

The influence of adding four 0.1-μF ceramic capacitors close to the terminals of the converter module is shown in Fig. 12 (right). The additional capacitors reduce the voltage spike to 12 V.

The effect of the parasitics on the line voltage with and without the decoupling capacitors is evaluated and reported in Fig. 13. It can be seen that the effect on the dc-link voltage waveform is directly reflected on the line voltage.

The effect of the parasitics on the phase voltage with and without the decoupling capacitors is evaluated and reported in Fig. 14. A smaller influence on the phase voltage spike can be noticed as it is affected by the transient switching behavior of only one inverter leg. The decoupling capacitors are reducing the phase voltage spike by about 23 V.

\[
L_{\text{dc}} = \text{computed as the total dc inductance seen between the dc input terminals multiplied by the number of modules, smooths the dc-source current which reduces the electrical and thermal stresses on the dc-source. Note that the } L_{\text{dc}} \text{ is 25 times higher than } L_{\text{ac}} \text{ which is an advantage for the proposed dc-link structure.}
\]

The capacitance between the plates and it further smooths the inverter terminal voltage.

\[
R_{\text{ac}} \text{ and } R_{\text{dc}} \text{ cause the power loss and the temperature rise of the bus-bar.}
\]

2) Bus-Bar Loss Density Distribution: The highest bus-bar loss occurs for the 15-phase configuration with common neutral point due to the lowest dc-link voltage and the highest capacitor current. The loss in the bus-bar occurs due to the dc and the ac currents drawn from the dc-source and the capacitors. The dc-current \((I_{\text{dc}})\) is computed from (7) considering 90% efficiency \((\eta)\) and the ac-current is computed from (4). The values of the dc and the ac currents are 236 and 35 A, respectively.

\[
I_{\text{dc}} = \frac{P_r}{\eta V_{\text{dc}}}
\]

(7) where \(P_r\) is the rated drive power and \(V_{\text{dc}}\) is the dc-link voltage.

Both the ac and dc currents are injected in the bus-bar and the loss density is evaluated in case of copper plates (Fig. 15) and aluminum plates (Fig. 16). It can be seen that the maximum loss density is located at the input dc tabs due to the higher dc current compared to the ac one and also the total dc-current of the 15
modules is passing through the input tabs unlike the ac current that divides over the 15 capacitors. The maximum loss density is 1.53 times higher in case of aluminum plates compared to copper plates due to the lower electrical conductivity of the aluminum.

C. CFD Analysis of the Bus-Bar

A CFD model is built to evaluate the temperature of the bus-bar components to ensure that the insulation temperature is below its rated value given the high ambient temperature inside an integrated drive. Assuming an ambient temperature of 50 °C, natural air convection, and the loss density distribution in Figs. 15 and 16, the temperature field is evaluated and shown in Figs. 17 and 18 for the plates and the insulation layer in case of copper and aluminum plates, respectively. The thermal properties of the materials used in the simulation are given in Table VI. Here, \( \rho \) and \( C_p \) are the mass density and the specific heat capacity, respectively.

The insulation temperature rises 97.3 and 165.8 °C above the ambient for the copper and the aluminum plates, respectively. For both materials, the insulation temperature stays below the rated value of the Kapton material. The 68.5 °C more temperature rise in case of aluminum plates is due to the higher loss density and the lower thermal conductivity of the aluminum. The higher temperature gradient in case of aluminum plates due to the lower thermal conductivity can also be seen. The maximum insulation temperature is 15% and 28.5% higher than the average in case of copper and aluminum plates, respectively.

V. EXPERIMENTAL RESULTS

The three-teeth integrated setup shown in Fig. 19 is built to validate the design concepts. It consists of three GaN converter modules (Fig. 3), three stator teeth, an \( R = 11.5 \Omega, L = 3 \) mH load, and a dc-link PCB. The line currents are measured with the on-board current sensor ACHS-7123 while the capacitor currents are measured using the current probe TCPA300 with the
static transfer function of 10 A/mV. All waveforms are visualized using a Tektronix 1-GHz bandwidth scope. The sinusoidal PWM technique is utilized and the control pulses are generated using the dSPACE MicroLabBox. The three modules are operated as three-phase inverter.

The capacitor current is measured at switching frequency 10 kHz, fundamental frequency of 50 Hz, and three different peak line currents of 7.5, 5.5, and 3.8 A to compare the measured rms value with the calculated value (4). With the value of the RL load used and 50 Hz, the resulting power factor is 0.997 near to unity to evaluate the worst-case value [13]. Fig. 20 shows the measured three phase line currents in case of 7.5-A peak.

The capacitor current at 7.5-A peak line current is shown in Fig. 21 for ten power cycles and Fig. 22 for ten switching cycles. The measured and the calculated capacitor rms current at different peak line currents are reported in Table VII with the percentage error between them.

The difference between the measured and the calculated current is mainly resulting from the influence of the parasitics and the decoupling capacitors.

The influence of the switching frequency on the capacitor current is visualized by measuring the capacitor current at a constant peak line current of 6.5 A and two different switching frequencies (10 and 30 kHz). Fig. 23 shows the measured capacitor current at 10 kHz and Fig. 24 at 30 kHz with the rms value marked on the graph. A 20.6% increase in the capacitor rms current can be observed at 10 kHz. The reason for the decrease of the capacitor current with the increase in the switching frequency is the higher inductive impedance of the dc-link that further smooths the current at the higher switching frequency.

The estimation of the capacitor power loss using (5) is assessed by measuring the capacitor temperature at two different line currents (5.5 and 3.8 A) and comparing the thermally measured power with the electrically calculated power. Both measurements are captured at ambient temperature of 25 °C and free air convection. The capacitor is covered with a black tape for a better emissivity and temperature measurement accuracy. The resulted hot spot temperature is 36.7 and 34.1 °C for 5.5 and 3.8 A peak line current, respectively.

Table VIII contains the capacitor power loss measured thermally and calculated electrically with the percentage difference
between both of them. The difference between the measurements and the calculations can be explained as follows: The variation of the ESR and the thermal resistance of the capacitors with temperature is not given in the datasheet of the selected part instead, fixed values at 25 °C are given. Neglecting the variation of these parameters with temperature introduces an error in the calculation of the capacitor losses. The capacitor temperature is measured with the thermal camera (GTC 400), and the measured value has an error of 3 °C; this represents the measurement error. Since the measured capacitor temperature is less than 37 °C, the contribution of the thermal camera measurement error is expected to be the main reason of the discrepancy.

**VI. CONCLUSION**

An integrated dc-link structure topology for reconfigurable modular motor drives was proposed and extensively analyzed in this article. The proposed topology has many advantages for
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