Ultra-Low-Power IoT Communications: A novel address decoding approach for wake-up receivers

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Abstract—Providing energy-efficient Internet of Things (IoT) connectivity has attracted significant attention in fifth-generation (5G) wireless networks and beyond. A potential solution for realizing a long-lasting network of IoT devices is to equip each IoT device with a wake-up receiver (WuR) to have always-accessible devices instead of always-on devices. WuRs typically comprise a radio frequency demodulator, sequence decoder, and digital address decoder and are provided with a unique authentication address in the network. Although the literature on efficient demodulators is mature, it lacks research on fast, low-power, and reliable address decoders. As this module continuously monitors the received ambient energy for potential paging of the device, its contribution to WuR’s power consumption is crucial. Motivated by this need, a low-power, reliable address decoder is developed in this paper. We further investigate the integration of WuR in low-power uplink/downlink communications and, using system-level energy analysis, we characterize operation regions in which WuR can contribute significantly to energy saving. The device-level energy analysis confirms the superior performance of our decoder. The results show that the proposed decoder significantly outperforms the state-of-the-art with power consumption of 60 nW, at cost of compromising negligible increase in decoding delay.

Index Terms—5G/6G, IoT, wake-up receiver, low-power electronics, battery lifetime.

I. INTRODUCTION

The Internet of Things (IoT) use cases, such as massive machine-type communications (mMTC) and ultra-reliable low-latency communications (URLLC), are one of the key drivers of fifth-generation (5G) wireless networks and beyond (6G) [1, 2]. A full realization of IoT can make substantial changes in the life quality by providing an intelligent network covering every object in the daily life, such as in agriculture, surveillance, health care, body implants, home automation, etc [3, 4]. Each IoT node is typically equipped with sensors, microcontrollers, wireless transceivers, and energy sources such as batteries. The principal objective of most reporting IoT devices is to observe their surroundings and report/act upon their gatherings. Since most IoT devices are battery-powered, and once deployed, they are expected to live a long time without human intervention, battery lifetime has always been a key concern of IoT-enabled networks [5]. Hence, the IoT traffic demands support for low-energy consumption.

A. Energy-Efficient Cellular IoT

During the evolution of mobile networks towards 5G and beyond, the energy efficiency of large-scale IoT communications have been improved significantly [5–7]. The implemented methods and solutions to realize the energy-efficient IoT communications are summarized in [8, 9]. As per literature, these solutions can be categorized into evolutionary and revolutionary solutions [10]. The evolution began from LTE Release 12 by supporting low-cost communications over dedicated resources followed by in Release 13 [11] where LTE-MTC (LTE-M) and narrow-band IoT (NB-IoT) systems were introduced. NB-IoT is known as a revolutionary solution and reference signals and random access happen in time instead of frequency [7, 12]. Since in these systems the link budget is improved, the required energy to transmit a bit is reduced [13–15]. However, the access procedures requires listening to the control channel and exchanging signal for random access, synchronization, and resource reservation [6, 15], resulting in a challenge to realize the long-lasting battery limited devices activities [14, 16]. As per the state-of-the-art, extensive efforts are made to improve the energy efficiency of IoT devices such as discontinuous reception (DRX) [17], power-saving mode (PSM) [18], lightweight communications protocols [19, 20], low-power radio transceivers [19, 21], idle listening [22], and duty cycling [20, 23]. These methods imply an inherent trade-off between reachability and energy saving of the devices [24]. Motivated by addressing this challenge, the energy/reachability trade-off can be broken by leveraging device hibernation, and wake-up receivers (WuR) [24].

B. The WuR Approach

In WuR approach, the device is in hibernation mode unless it is paged by the base station (BS) or has a message to exchange. Since the battery is entirely intercepted as it is hibernating [25], no power is consumed except for monitoring whether the device is paged. To page a device, the network broadcasts a wake-up signal, including the device’s unique address, to all devices. The device is equipped with an auxiliary WuR—consuming much less power than the primary device [26]—to receive and decode every wake-up signal and prompt the device if required [22, 27]. As a result, the power consumption of WuR lies in the µW domain, whereas the IoT device may consume several milliwatts [28, 29]. Therefore, reliable self-sufficient energy management is indispensable for achieving an eligible WuR capable of operating indefinitely without compromising the quality of service (QoS) [19]. A WuR contains a radio frequency (RF) receiver, a demodulator, a low noise baseband amplifier, and a digital address decoding unit. In this regard, ultra-low-power, noise-robust address decoders are presented to enhance WuR’s power efficiency. For such ultra-low-power devices, harvesting energy from the environment
can provide enough power, e.g., around 1\(\mu\)W, to keep WuRs charged to operate self-sustainably\(^1\) [33–35].

C. Related Works

1) WuR integration in cellular networks: The 3rd Generation Partnership Project (3GPP) Release 15 introduces the wake-up signal as a unique signal sent from the BS to IoT devices paging them to wake the main receiver up [36, 37]. In order to avoid creating extra interference in orthogonal frequency-division multiplexing (OFDM) across cellular networks, wake-up devices should use out-of-band (or in guard band) signal, as in the NB-IoT [38]. The applicability of leveraging WuR in millimeter wave (mmWave) bands and beamforming systems has been investigated in [39]. In [40], the authors propose a novel approach to transmit a wake-up signals along with the normal transmissions. In [25], a prototype implementation of a WuR-based two-tier system, bridging cellular IoT and Bluetooth low energy (BLE), has been presented. In this implementation, BLE devices are activated using BLE signals, and an 8-bit address comparator module [41] is leveraged in the WuR for address decoding and paging verification. In [42], the performance of WuR-enabled cellular IoT in uplink and downlink has been investigated. The authors derived lower and upper bounds for the success and false wake-up probabilities as a function of signal-to-interference-plus-noise ratio (SINR). In [24], a joint WuR and energy-harvesting connectivity solution have been proposed in which information packets sent on the proposed solution are preceded by a power-optimized preamble. Then, the energy harvested from the preamble at the WuR is used by a low-power receiver for decoding the data packets. In Fig. 1, the approaches aiming at enhancing the battery lifetime of devices are grouped. In this figure, 4G enhancements are in blue, LTE-advanced/pro and 5G enhancements in purple, and proposals for beyond 5G approaches in red. The device-dependent approaches are in orange, i.e., wireless power transfer from a charging drone to remote IoT devices [43].

2) WuR device design: Address decoders, alongside RF receivers and demodulators, consume a considerable portion of the overall power. Although the literature on making efficient demodulators is mature, the literature lacks research on fast yet low-power and reliable address decoders. The majority of proposed WuRs in the literature leverage microcontrollers or digital correlators as their address decoders, as per [25, 51, 52], and these modules consume a considerable portion of the total power in lengthy addresses used in local and wide-area deployments. The authors in [53] have utilized an off-chip lumped element matching network for the wake-up receiver. The study in [51] has utilized PIC12F683 MCU, a 3-volt prototype decoder that consumes 820\(\mu\)W during interception. The authors in [54] have designed a switch-capacitor-based correlation unit inside an ASIC which draws 0.4\(\mu\)A at 20kS/s (kilo samples per second). The studies in [55–57] have utilized flip-flops (FF) based decoder to generate a wake-up interrupt signal which consumes 13.4\(\mu\)W at 0.9 volts and 100Kbps and decodes a 16-bit address in 0.08ms. Moreover, they have presented pipelined FFs to store intercepted signal bits for real-time address validation using logic gates.

D. Motivation and Contributions

The increase in the number of connected devices and the need for security of IoT communications mandate adopting lengthier addresses, which increases the energy consumption of the address decoding module in the WuR. In order to save energy in continuously monitoring the received ambient engines for potential paging, a low-power yet reliable address decoder is needed. Here, a novel address decoder architecture is proposed and evaluated in terms of power efficiency and reliability. The major contributions of this study include:

- We propose a novel address decoder for WuRs, leveraging sequential clocking of gates.
- We investigate the performance of the proposed address decoder in terms of delay and power efficiency, using analysis and simulations.
- We propose a novel architecture to obtain the maximum possible power efficiency. It can decode 32-bit addresses by consuming only 2nW at 1Kbps, which shows a significant improvement in power efficiency than the legacy architecture consuming roughly 12\(\mu\)W to decode a 16-bit address at the same bit rate [58].
- The proposed architecture benefits a light strategy for dealing with noise, and it can detect addresses even though some of the address bits might be corrupted. The technique utilized to achieve this goal is to detect and overlook a certain number of corrupted address bits to a certain extent.
- The address length in the proposed architecture can be adjusted to any length shorter than its maximum capacity. This address length flexibility brings efficiency as a single address decoder embedded in the device could be used in different lengths, e.g., shorter length for personal area communications, and full length in wide-area communications, in order to save energy further.
- We investigate the energy consumption of uplink and downlink IoT communications with/without WuR versus different communications parameters. Find operation regions in which integration of WuR is beneficial, investigate challenges in such integration, and potential solutions for compensation of challenges.

The remainder of the paper is organized as follows. The system model and the problem description are given in Section II. In Section III, the proposed address decoding scheme is presented. In Section IV, modeling of KPIs and device-level performance evaluations are presented. In Section V, the integration of WuRs in uplink/downlink communications is investigated. Finally, the concluding remarks are given in Section VI.

\(^1\)The energy can be harvested from 1) environment such as solar and wind, 2) the ambient wireless radio waves and signals such as TV broadcasts 3) other sources like temperature difference, and motion. The interested readers are referred to [30–32] for in-detail description of the harvesting technologies, the conversion power efficiency, and the sources of energy harvesting.
Solutions for prolonging the battery lifetime

Energy saving

Network access

Energy harvesting

Fig. 1: Classification of various solutions targeting a longer battery lifetime: 4G enhancements for IoT are in blue, LTE-Pro and 5G enhancements are in violet, proposed approaches for beyond 5G are in red, and the device-dependent approaches are in orange.

Fig. 2: A wake-up receiver unit.

II. System Model and Problem Description

As illustrated in Fig. 2, a WuR consists of an analog demodulator and a digital address decoder. The analog demodulator comprises several modules, including an amplifier, rectifier, AC coupling, and comparator (the black boxes in Fig. 2). The demodulated signal is then passed on toward a digital address decoding unit (the red solid area in Fig. 2) which checks if the received signal matches the saved address. If the received signal matches the device’s address, a wake-up interrupt is generated for the primary circuit.

The architecture of an $n$-bit address decoder has been depicted in Fig. 3 for a conventional WuR [56,59,60]. In this architecture, the address decoding unit stores the latest received $n$ bits in a shift register, consisting 8 FFs, and passes the input sequence and the stored address through a tree-shaped structure of XNOR and AND gates for comparison. To better understand, the timing diagram for the operation of an 8-bit address decoder with such architecture is presented in Fig. 4-a. As one observes here, from top to bottom, the clock signal, the saved address in the device (10011101), the received sequence of data, 8 values of $Q_0$ to $Q_7$, related to the output of respective flip flops, 8 values of $X_0$ to $X_7$, related to the output of XNOR gates, and finally the wake-up signal have been depicted. The above-described address decoding method, powered by XNORS, has been vastly utilized in different WuR designs [56,59,60]. In order to save further energy for WuRs, it is of crucial importance to decrease the number of active components in the circuitry. Hence, having the XNOR gates and the FFs activated all the time for online comparison, a considerable amount of dynamic power is consumed even when the device has not been paged. This energy consumption has been visualized indirectly in the timing diagram of Fig. 4-a, where the output values of FFs vary frequently. Then, the first research question (RQ) could be expressed as follows:

RQ.1: Given an $n$-bit constant address and a dynamic bitstream (changes by the clock), how can one leverage a low-power digital circuit to carry the comparison out and generates a wake-up signal as soon as there is a match? Now, assume we have the low-power comparator circuit. The next question comes from the reliability point of view. Consider the fact that there is a possibility of error in the reception of data, demodulation, and other stages. Then, it is vital to ensure our wake-up procedure is resilient to such errors. The first sub-RQ aims at addressing this concern, as follows.

RQ.1.a: How can one introduce $m$-bit error tolerance to the comparison procedure, i.e., if the received sequence matches the input sequence in more than $m-n$ positions, it generates a wake-up signal? Finally, let us consider a device with an $n$-bit address that has been deployed in an application where devices are limited in number, and hence, a much shorter address suffices for their paging. The next sub-RQ aims to make the comparison flexible to enable energy-saving whenever possible, as follows.

RQ.1.b: How can one make the comparison procedure flexible to work with different lengths of the address in order to save energy whenever possible?

In the second research question, we aim to investigate operation regions (in terms of activity, i.e., the rate of reporting and paging) in which the introduction of WuRs to IoT devices can bring energy savings. Towards this end, we need to model energy saving in uplink/downlink IoT communications and see which kind of devices can benefit from WuRs. Then, this problem is expressed as follows.

RQ.2: Given the activity of IoT devices in terms of rates of paging for downlink communications and reporting for uplink communications, for which activity ranges, leveraging WuRs results in significant energy saving for IoT devices?

In Section III, we present our solution for RQ.1. Then, in Section IV, we evaluate the performance of the proposed solution and answer RQ.1.a and RQ.1.b Finally, in Section V, we answer RQ.2.
III. THE PROPOSED ADDRESS DECODING SOLUTION

This section aims to answer RQ.1, i.e., reducing the dynamic power consumption in address decoding. Recall from the timing diagram in Fig. 4-a, where there were many unnecessary transitions and activities in the comparator circuits before the wake-up signal is triggered. Towards reducing power consumption in unnecessary transmissions, which are the primary sources of power consumption, we introduce a
low-power sequence decoder (LPSD) in which a sequential procedure for circuit-activity management is followed, as depicted in Fig. 5. The proposed LPSD leverages a novel block called G-blocks for bit-wise comparison and process flow control. In this architecture, when a bit-match occurs, e.g., at the $A_0$ position of address as in Fig. 5, the respective G-block, i.e., $G_0$, approves it and stores its occurrence in the subsequent FF. The three inputs and the output of a G-block are denoted by $a$, $b$, $c$, and $f$, respectively (pop-outed section in Fig. 5). The $(a,b,c)$ inputs are connected to the sequence input, the respective stored address bit in the memory ($A_i$), and the output state of the FF in the previous stage ($Q_{i-1}$), respectively. The $i^{th}$ G-block’s output becomes 1 when $Q_{i-1}$ is 1 (i.e., the latest $i$ bits have been correct so far), and the current input is also equal to $A_i$. As Fig. 4 and 5 demonstrate, although the comparison employs an XOR gate in the G-block, it is not as active as the XNOR in the legacy design. Because in the legacy address decoder architecture (Fig. 3), one of the inputs of each XNOR gate is directly connected to the input data, which has a high transition probability. In contrast, in the proposed LPSD structure, an AND gate has been placed before the XOR gate to block propagation of the sequence input to the XOR gate. Hence, the XOR gate in the proposed solution remains inactive primarily.

Regarding static power consumption, an XOR gate is connected to the En (enable) input of each FF, as shown in Fig. 5. This gate detects when a FF is likely to change its state on the clock’s edges and enables it. It also deactivates the FF and puts it in sleep mode when no change in the FFs state will happen in the subsequent edge of the clock. From the address decoding perspective, the $i^{th}$ FF needs to change its stored bit in any of the following conditions:

- The transition from 0 to 1 is needed:
  - the $i^{th}$ FF has been in state 0, and
  - the last $i$ bits are matching the corresponding part of the stored address (i.e., the output of the $i^{th}$ G-block is 1)

- The transition from 1 to 0 is needed:
  - the $i^{th}$ FF is already set to 1 (because in the last previous clock cycle, all the last $i$ bits have matched the corresponding part of the stored address), and
  - The latest $i$ bits are not matching anymore.

Based on our design, if any of the above conditions are true, the XOR gate’s output will become 1, and hence, the $i^{th}$ FF will be activated to apply the changes, with the exception of
the first FF which is always active. The LPSD procedure can be better understood through Algorithm 1. As the algorithm suggests, all of the LPSD’s FFs are initially reset. To sync the procedure with the clock signal, the main procedure is wrapped between two await commands, checking for rising and falling edges. The array \( i \), contains the indexes of every set FF. Using the indexes stored in \( i \), the algorithm can determine that in which stages the comparison must carry; except for the first stage which must always do the comparison regardless of the other FFs status and hence it is separately written in the algorithm. Ultimately, the last if statement checks the status of the last FF for triggering the wakeup signal. In other words, the circuit design paradigm has been shifted from always-on to always available, i.e., any module is activated once needed.

In the legacy address validation approaches, as depicted in Fig. 4, the entire received sequence content is in operation in every clock cycle [59]. Hence, the wake-up interrupt command is produced when all XNOR gates’ outputs are 1 (in clock cycle 11 in Fig. 4-a). However, the proposed LPSD works sequentially, and hence, the majority of the LPSD circuit is generally in the inactive mode. As the chance of receiving a 1 or 0 bit in a pure noise ambient is equal, the probability of random activation of the first FF of LPSD, i.e., FF\(_0\) in Fig. 5, is 50%. Then in the subsequent FF, the probability of random activation is half of its predecessor. For example, the probability of random activation of the fifth FF, FF\(_4\), by ambient noise is \( \frac{1}{2^5} \approx 3.1\% \). Thus, most of LPSD’s logic circuit remains inactive in practice, as depicted in the timing diagram of Fig. 4-b. From this figure, it is seen that the state of the fourth and higher FFs are unlikely to change their state. Thereby, the device consumes a negligible amount of power. While comparing the timing diagrams of the legacy and the proposed LPSDs in Fig. 4 clearly shows the superior performance of the proposed scheme in power consumption, we will carry out an in-depth performance analysis in the next section.

IV. KPIs AND PERFORMANCE EVALUATION AT THE DECODER LEVEL

In this section, we investigate the key performance indicators (KPIs) of the proposed address decoder. The KPIs of interest include the reliability of address decoding, latency in address decoding, power consumption in continuous sequence decoding, and solution flexibility to address length. Furthermore, we answer RQ.1.a (presenting an extended version of the LPSD, which is tolerating mismatch in address decoding) and RQ.1.b (flexibility of LPSD to address length) in this section.
A. Reliability

Data corruption due to environmental noise or interference is a fundamental limitation of any wireless communication system and must be considered in the design and operation management of its entities and the services offered through it. To have a probabilistic analysis of this limitation in our problem, let us denote by \( p_b \) the bit-error rate (BER). In [61], \( p_b \) has derived for an OOK address detector operating in additive white Gaussian noise (AWGN) channel, as:

\[ p_b = ce^{-\lambda} \]

In this expression, \( \lambda \) is the signal-to-noise ratio (SNR) of the envelope detector’s input, and \( c \) is a constant. A consecutive sequence of correct address bits must be received for a conventional address decoder, such as the one leveraged in [61], to trigger a wake-up signal. Hence, a single corruption in the sequence traps the full detection procedure, and no signal will be triggered until the full address is re-transmitted. Then, the probability of a conventional \( n \)-bit address decoder detecting an address correctly is given by \( P_{\text{conv}}(n) = (1-p_b)^n \).

In order to avoid being trapped by less than \( m \) bits corrupted bits in address decoding, we proposed to follow a 2-step procedure: (i) allocate address codes such that a minimum hamming distance of \( 2m + 1 \) is achieved between any two devices\(^2\), and (ii) design the address decoder such that it accepts \( m \) mismatches between received sequence and the store address.

Recall from the description of the proposed LPSD in Fig. 5 that investigation of the received sequence proceeds as the first received bit matches the first bit of the address and stops as soon as a mismatch occurs. To count and ignore a certain number of mismatches, the presented architecture for LPSD in Fig. 5 is improved by adding \( S_{\text{in}} \) and \( S_{\text{out}} \) buses, as shown in Fig. 6. Then, multiple redundant LPSD blocks are cascaded in parallel. When a mismatch occurs, the procedure stops at the corresponding LPSD and is continued in the adjacent LPSD, as shown in the improved architecture of Fig. 7. Then, to bring tolerance to \( m \) bits of mismatch, \( m \) adjacent LPSDs are needed in parallel. Following the derivation of \( p_b \) in the above, the probability of correct detection of an \( n \)-bit address by using the updated architecture for tolerating \( m \)-bit mismatch is derived as:

\[
P_{\text{LPSD}}(n,m) = \sum_{k=0}^{m} \binom{n}{k} (1-p_b)^{n-k} p_b^k
\]

Comparison of \( P_{\text{LPSD}}(n,m) \) with \( P_{\text{conv}}(n) \) reveals that since for a non-zero \( m \), \( P_{\text{LPSD}}(n,m) > P_{\text{conv}}(n) \), and the difference becomes much higher by an increase in \( m \). Then, by choosing an appropriate value of \( m \), in accordance with the environment, one can minimize the probability of missing a wake-up signal.

B. Latency Analysis

One of the vital statistical aspects of every digital device is the minimum time at which the device can propagate its input signals towards the outputs. This time length is essentially the minimum required time that the device needs to execute a single operation and is determined by finding the longest path that an input signal needs to pass to reach the output terminals. The maximum time delay of the legacy and proposed \( n \)-bit address decoders are derived as follows:

\[
\hat{T}_{\text{conv}} = nT_{\text{FF}} + (\log_2 n + 1)T_{\text{Gate}}
\]

\[
\hat{T}_{\text{LPSD}} = n(T_{\text{FF}} + 2T_{\text{Gate}}) + T_{\text{G}}
\]

Fig. 8: LPSD’s delay in different address lengths

in which, \( \hat{T}, T_{\text{FF}} \), \( T_{\text{FF}} \), \( T_{\text{Gate}} \), and \( T_{\text{G}} \) denote the maximum time delay of the device, the toggle and enable delay values of an FF, the logic gate delay, and the time delay of a G-block, respectively. From the G-block description in Fig. 5, \( T_{\text{G}} \) is equal to \( 4T_{\text{Gate}} \), respectively. From digital logic design [62], \( T_{\text{G}} < T_{\text{FF}} \). Hence, for large values of \( n \), the dominant element is \( T_{\text{FF}} \), and the rest could be neglected. Thus, (2)-(3) could be simplified as:

\[
\hat{T}_{\text{conv}} \approx nT_{\text{FF}} + t_1
\]

\[
\hat{T}_{\text{LPSD}} \approx nT_{\text{FF}} + t_2
\]

in which \( t_1 \) and \( t_2 \) are constant time delay values, and \( t_1 < t_2 \). From the LPSD architecture in Fig. 5, one observes that adding \( m \) redundant stages of LPSD for error tolerance merely adds \( m \times T_{\text{Gate}} \) delay to \( T_{\text{LPSD}} \), adding the potential of recovery from bit corruption to the address decoder. One must note that this extra latency for noise robustness is negligible for large values of \( n \), i.e., the address length, as one observes in Fig. 8. This figure depicts the maximum delay of the legacy and proposed LPSD architectures for different address lengths. From these results, one observes that delay performances of both architectures are roughly the same, and they follow a trend in order of \( n \) in bytes. In other words, the maximum delay for an \( n \)-bit address decoder is approximately \( n/8 \) nano-seconds.

C. Power Consumption Evaluation

In this section, we investigate the power consumption of the address decoder module as the main KPI of interest and compare it against the legacy solutions. The following results, in Fig. 9, have been obtained by executing several rounds

\( ^2 \)This is to make sure tolerance to mismatch in address decoding does not result in the generation of false wake-up signals.
of power analyses under different configurations, including address length and bitrate (the rate at which address decoder is operating). The simulations have been executed in Synopsys Design Compiler with UMC65 library, powerful software for detailed digital device analysis. A sequence of random input data was generated (Length=5000) for this purpose while some correct address sequences were included in it. To be clearer, we manipulated this sequence manually according to the presumed address so that 7%, 10% and 20% of the bits in the sequence were a part of a totally correct address, an approximately correct address with one or two error bits, and a half correct address, respectively. The rest of the bits remained random and unchanged. Obviously, in a condition that all the address bits were purely random the resultant power consumption of the proposed structure could have been even higher in view of lower activity of the FFs. This procedure was carried out the same for all of the structures in this work.

Now, let us take a deeper look at the power consumption evaluation results. Fig. 9a compares the total power consumption of the proposed LPSD against the legacy architecture [56, 59, 60]. One observes that the consumed power by the legacy solution is roughly 6 times more than the power consumption of the proposed approach for a 64-bit address. Even for a short address length of 16 bits, we observe that the proposed architecture outperforms the legacy approach by reducing the average power consumption in continuous decoding by 67%, i.e., the legacy approach consumes 3 times more power. One must note that this level of reduction has been made possible by detecting and removing the primary sources of power consumption, i.e., unnecessary activity of different parts of the comparator circuit. A detailed analysis of power consumption, including specifying dynamic and static parts of power consumption, has been presented in Fig. 9b. The analytics in this figure suggests dynamic power forms roughly over 95% of the overall device power consumption in both the legacy and LPSD architectures. However, although static power forms an insignificant portion of the overall power, it drains continuously from the power source. Hence, it is also a significant issue, especially when the device is expected to be in the standby state for a long time. From the simulation results in Fig. 9b, one observes that in LPSD architecture, both static and dynamic power is reduced significantly com-
TABLE I: Different address decoder architecture implementation areas.

| Address length | 8-bit | 16-bit | 32-bit | 64-bit |
|----------------|-------|--------|--------|--------|
| State-of-the-Art | 137.88 | 279 | 561.6 | 1126.6 |
| LPSSD | 191.88 | 430.92 | 909.36 | 1866.24 |
| LPSSD (m = 1) | 528.48 | 1156.32 | 2366.64 | 4925.52 |
| LPSSD (m = 2) | 794.52 | 1736.28 | 3551.76 | 7390.08 |

pared to the legacy approach. From Fig. 9a and Fig. 9b, we further notice that power consumption of the legacy approach increases almost linearly with the length of address, while for the proposed LPSSD, the change in power consumption by doubling the address length is less than 20%. To be more specific, for the legacy and proposed approaches, by increasing the address length eight times, the power consumption has increased 440% and 57%, respectively.

Fig. 9b reflects the impact of adding modules for noise robustness on the power consumption. As discussed in Section IV-A, multiple LPSSDs can operate redundantly so that the address decoder can ignore a certain number of corrupted bits. However, adding such redundant LPSSDs, increases the number of active modules in the WuR, and consequently, the overall power might increase. Since the noise robustness level depends on the number of redundant LPSSDs one observes a direct trade-off between power efficiency and the level of robustness. The results show that a 64-bit address decoder based on the proposed architecture and 1-bit robustness consumes 30% less power than the legacy approach without corruption robustness.

Finally, in Fig. 9d we investigate the impact of the bit rate of address decoding on power consumption. In this figure (where power consumption is reported in dBm due to its logarithmic profile, hence a wide range of bit rates could be distinguished), we observe that the impact of address length on the power consumption (the x-axis) is negligible compared to the impact of frequency of operation. Furthermore, it is seen that increasing the bit rate of operation by 10 times results in an approximately 10dB increase in power consumption.

Table I demonstrates that although the LPSSD architecture has been quite beneficial, it roughly occupies up to 60% more area than the state-of-the-art, which can be considered the cost of this architecture. As an example, for 64-bit address length, the LPSSD requires about 1900 $\mu m^2$ to implement using 65nm CMOS technology while the state-of-the-art takes about 800 $\mu m^2$ less with the same technology. Furthermore, adding redundant LPSSD layers for error resiliency can also increase the extent of the area.

D. Address Length Flexibility

As mentioned earlier, the proposed LPSSD can adjust its address to shorter lengths as well. The address length can be shrunk by bypassing a certain number of LPSSD’s stages and leaving only the required number of them functional. Bypassing the stages is feasible using the $S_{in}$ bus, which provides direct access to write on each stage’s FF. Since each

TABLE II: A comparison of different address decoder technologies. $\eta$ (%) is the power consumption ratio of the address decoder to WuR.

| Ref | Tech. | Power ($\mu W$) | Bit Rate (Kbps) | Voltage (V) | Address (bit) | $\eta$ (%) |
|-----|-------|----------------|-----------------|------------|---------------|----------|
| This work | LPSSD | 0.068 | 1000 | 0.9 | 64 | - |
| [56] | FF | 13.14 | 100 | 0.9 | 16 | 97.9 |
| [59] | FF | 25.5 | 1 | 3 | 16 | 65.3 |
| [60] | FF | 101.7 | - | 0.9 | 18 | 34.64 |
| [63] | MCU | 70.6 | 500 | 0.8 | 8 | 98 |

FF stores the comparison result of that stage, pulled-up FFs do not require matching approval to propagate the sequence, and hence, they do not affect the procedure. Then, by leveraging the design in Fig. 6, we have an address decoder that enables operation with a flexible address length (response to RQ.1.c).

A summary of performance evaluation results has been presented in Table II. According to this table, the proposed architecture consumes much less power than the most efficient low-power address decoding technology we found in the literature, which is an incredible improvement in the address decoder’s power efficiency. In Table II, only the power consumption of the address decoder part of WuR for the various works is examined. Furthermore, the proposed design operates twice as fast as its fastest prior art [63], and its supply voltage is amongst the lowest. Also, to check the importance of the address decoder part in the WuRs, we define a parameter ($\eta$) to indicate what percentage of the power consumption of the WuR is due to the address decoder part. The value of $\eta$ for different works is given in Table II. We can say that the address decoder consumes most of the power of the WuR.

V. WuRS in Cellular IoT: Opportunities, Chalanges, Future Research Directions

In this section, we investigate the performance of WuR-enabled cellular IoT. To this end, we first investigate the message exchanges in up/downlink communications with/without WuRs, and compare the performance of these two schemes in terms of energy efficiency in Subsection V-A1. Then, we investigate challenges in the integration of WuRs and future directions for research in Subsection V-B and Subsection V-C, respectively.

A. Integration of WuRs in Cellular IoT

In many IoT applications, IoT devices are in the reporting or actuating state [8]. In the former, the device gathers data such as temperature from the environment and sends the data to the network when the network requests for the data (uplink IoT service). In the latter, the network sends some information to the device base on which the device acts on its environment, e.g., gather data or opens a valve or so on (downlink IoT service).

Let us investigate the downlink and uplink IoT services described above, in detail in Fig. 10. This figure depicts
message exchanges and symbolic energy consumption levels for downlink and uplink IoT communications. First, Fig. 10a depicts a simplified scenario for downlink IoT service in which, device sync itself with the network, check regularly (or in sleep/wake up cycles as in DRX) for paging, sends data as soon as is being paged by the network, and finally sends the ACK to the network. One further observes the respective power consumption levels for listening, transmission, and being in the active and sleep modes for the device. Figure 10b depicts message exchanges and power consumption levels in the case a WuR is embedded in the device to remove the need for listening for potential paging. One observes in this figure that leveraging WuR prevents the device from regular checking of the downlink control channel at the cost of continuous operation of the WuR. In the following subsection, we will quantify the saving brought by leveraging WuRs instead of listening for paging.

Figure 10c presents the uplink IoT service in which, upon having data to transmit, the device turns the radio on, performs synchronization, finds the random access resources, sends RA requests, and sleeps until the reception of the wake-up signal. When the BS intends to schedule the device for data transmission (if needed), the BS sends the WuR message to the device, which is immediately followed by data transmission and reception of the ACK. In the following subsection, we will quantify the savings by leveraging WuRs instead of listening for scheduling responses.

1) Evaluation of Energy Saving: Now, let us evaluate the energy-saving performance of implementing WuRs in uplink and downlink communications. We assume that the IoT device
follows the downlink and uplink communication procedures according to Fig. 10b and Fig. 10d, respectively, and simulation parameters are summarized in Table III. For WuR-enabled IoT devices in uplink and downlink, the device is in sleep mode unless it is paged or has a message to transmit or receive. The wake-up duration in Table III, is defined as the time in which a device listens to the communications signals after receiving a paging signal. This is similar to the wake-up duration in DRX schemes; However, in the former the duration between the listening periods is not fixed. The higher on-time is, the higher energy is consumed. Hence, this parameter should be adjusted considering unreachability/power consumption tradeoff as well as other restrictions of the device application. For instance, in the application of data gathering services, the unreachability of systems with long sleep times (short wake-up duration) is acceptable because most communications are uplink-oriented. In contrast, in other applications, unreachability may cause significant costs to the system. 10 msec is a typical value for this parameter in the state-of-the-art devices and is chosen for this paper as well.

In Fig. 12a, we plot the total power consumption of the IoT device in the downlink where the device is receiving data. The device wakes up according to the wake-up procedures defined in Fig. 10. The total power consumption of the IoT device with WuR is much lower than the IoT devices without WuR. However, as the paging rate increases, the gaps between the power consumption of devices with and without WuR decrease. This is because with the larger arrival rate, there is not much room to sleep, and hence less energy is saved. Therefore, the impact of WuR will be smaller on the total power saving.

In Fig. 12b, we illustrate the uplink power consumption of the IoT device. We assume that the generated packets are transmitted with the uplink transmission success rate of $P_s$. As the packet generation rate increases, the uplink power consumption and the power consumption gap between the device with and without WuR increases because the IoT transmits more power to send more packets. Moreover, devices without WuR should spend more time listening to the channel for the random access response and ACK signal at each transmission. Hence more power is consumed compared to IoT device with WuR.

In Fig. 12c, we investigate the total power consumption of the IoT device in both uplink and downlink. We assumed that devices are paged every 10s and 50s in the downlink. The total power consumption increases when the downlink load is higher, i.e., the paging period is lower. However, in total power consumption, the uplink power consumption is dominant as the transmission power is higher than the power consumption of other modules. Increasing the uplink packet generation rate, the gap between the power consumption of devices with and without WuR increases, highlighting the benefits of using WuR in the uplink, downlink, and total power consumption.

B. Remaining Challenges

In this subsection, we investigate two significant challenges we encounter in the integration of WuRs in cellular IoT systems.

1) Interference of the wake-up and communications signals: In most systems, the wake-up signal is sent on the same channels as used by the primary communications. Therefore, the support of WuRs either reduces the data throughput of the network or will suffer from the interference of the primary communications. To limit the negative impact on the data throughput, we might limit the maximum number of devices that expect a wake-up signal in each cell and limit the wake-up signal’s time duration. However, these limitations will affect the large-scale deployment of WuRs. Out of bound implementation of WuRs or guard band implementation are also two choices. However, they will increase the complexity of end devices, as they need to have separate radios for WuR and communications. Then, here there is a choice of more complexity at the network access side (by joint scheduling of wake-up signals and data packets) or on the device side (two bands for two purposes).

2) Reliability of communications: False alarms and missed alarms: The ubiquitous coverage and reliability of communications are the key performance indicators that distinguish cellular-based solutions. While the introduction of WuRs to IoT serving procedures seems a promising method to maintain the preserved battery power and increase the device’s lifetime, the reliability of WuRs, including (i) the risk of false alarm
(making device awake when another device has been paged); and (ii) risk of missed alarm (missing the paging from the network when data is waiting for the device or input from the device is needed), are to be minimized as much as possible. If such reliability concerns are not addressed properly, while saving energy for IoT devices is of paramount importance, in many applications, this saving could not be achieved at the cost of degrading the reliability of communications. A potential solution for these concerns consists in generating (and continuously updating [64]) radio maps of the service area for the wake-up signals. Based on these maps and the location of devices, they could be categorized into classes, as in NB-IoT [12]. Then, the BS can send wake-up signals with appropriate power and a number of repetitions to the end device to ensure the device has received enough power to detect the wake-up signal.

C. Further Energy Saving for WuR-enabled Cellular IoT

In this subsection, we present directions for future research for the integration of WuRs into cellular IoT, including leveraging passive WuRs and integration of WuRs with grant-free radio access.

1) Passive WuR: Further energy saving: A passive WuR is designed based on passive circuits which harvest energy from the incoming radio signal in the wake-up message to switch itself on and wake up the primary circuit [65]. While passive WuR does not need to be powered by a battery, the received energy from wake-up signals has a limited range, which is a limiting factor of the system. Based on the current technology, the communication range of the passive WuRs is about 3m [65]. This range is much less than the active ones, typically 200m in the range [65].

2) WuR meets GFA for a close-to-zero energy profile in the idle mode: The works in [6, 66] have shown that energy consumption in the signaling states and resource reservation can be as high as in the transmission state (due to the period of being in the listening mode). A potential solution to decrease the overall energy consumption in resource reservation is to use grant-free access (GFA), especially in the uplink communications where WuR cannot save much energy (Fig. 10d and 12b) [15, 47]. The GFA scheme has already been implemented in IoT technologies that operate in the unlicensed spectrum, such as SigFox and LoRaWAN [67]. In GFA, once a packet arrives at the device, it is transmitted without any handshaking and resource reservation. As part of the efforts shaping the 5G new radio (NR) and beyond, using GFA has become a hot topic in recent years [68]. Fig. 11 represents a scenario in which the IoT device leverages both GFA and WuR for uplink and downlink communications. As one observes in this figure, upon having data to transmit, the device turns the radio on, performs synchronization, sends data, and sleeps until reception of the wake-up signal for the ACK or a potential downlink message. Despite the energy benefits in GFA, there are some challenges to be dealt with before the realization of GFA, mainly in terms of resource efficiency and reliability of communications. GFA has been investigated in a several recent works [49, 69, 70] and the 3GPP [48, 71]. In the context of the 3GPP standardization, the set of radio resources that should be allocated to GFA, the choice of modulation and coding scheme, and the impact on grant-based communications are the main study items [48, 71].
VI. CONCLUSION

In this work, we have investigated the integration of WuRs in the uplink/downlink cellular IoT communications. First, we explored the address decoding problem in the design of energy-efficient yet reliable WuRs. Then, we designed a novel address decoder by sequential clocking of address decoders. Closed-form expressions of the key performance indicators have been derived in address decoding, including reliability, delay, and power consumption in operation. A case study, consisting of data gathering IoT devices has also been introduced to investigate the potential of the proposed WuR-based solutions. Using this system-level analysis, regions of traffic load in which the introduction of WuR in the radio of the IoT device is beneficial to have been explored. Then, device-level analysis has been carried out, where performance evaluation results show significant advantages in power efficiency. These promising results promote the integration of WuR in future cellular networks, along with the legacy downlink control channel monitoring schemes used in the existing LTE and NB-IoT systems.

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