Rare-earth based ultra-thin Lu$_2$O$_3$ for high-k dielectrics

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Abstract. Lu$_2$O$_3$ thin film has been deposited on n-type (100) Si substrates using pulsed laser deposition (PLD). Atomic Force Microscopy (AFM) revealed a relatively smooth film surface after high temperature annealing at 900°C with roughness root mean square (rms) value of 0.237 nm. A equivalent oxide thickness (EOT) of 1.68 nm with a leakage current density of $1 \times 10^{-4}$ A/cm$^2$ at 1 V accumulation bias and a k value of 11.6 was obtained for 4.5 nm thick Lu$_2$O$_3$ thin film deposited at room temperature followed by post-deposition anneal (PDA) at 900°C in oxygen ambient. High resolution transmission electron microscopy (HRTEM) analysis has shown that Lu$_2$O$_3$ film remains amorphous at high temperature annealing at 900°C with little or no observable interfacial layer. The results showed that Lu$_2$O$_3$ possesses good properties and has strong potential as an alternative high-k gate dielectric.

1. Introduction

As technology advances, there is a strong demand for faster and more powerful devices to support the increasing complexity of tomorrow’s applications. We have witnessed the success of the semiconductor industry which relies on the continuous improvement of the integrated circuit performances, which is achieved through the reduction of device dimensions. SiO$_2$ is fast reaching its fundamental limit as an effective gate dielectric when the physical thickness is scaled down to below 1.5 nm as the gate leakage current increases rapidly due to quantum mechanical tunneling effect, which will in turn affect the reliability of the device. Among the high-k gate dielectrics, ZrO$_2$ and HfO$_2$ have attracted much attention. However, these materials still have some problems such as interfacial layer and micro-crystal formations during the post deposition annealing process. These problems lead to the increase of EOT and gate leakage current, respectively.

The lanthanide group has shown potential as alternative candidates for gate insulator because of their fairly large band gap, high relative dielectric constant and low leakage current. Moreover, some of the lanthanide oxides show good characteristics without pre-formed interfacial layer, and are regarded as possible candidates for next generation high-k dielectrics. Among the lanthanide oxides, Lu$_2$O$_3$ has the highest lattice energy (-13871 kJ/mol) and the largest bandgap (5.5 eV) and therefore Lu$_2$O$_3$ is expected to show better thermal stability, insulating property and hygroscopic immunity than other lanthanide oxides thin film. Previous reports on Lu$_2$O$_3$ has shown good insulating properties with k value of around 11 and low leakage currents. Numerous methodology of thin film
deposition has been explored, such as high-temperature oxidation of metallic films, ultrahigh vacuum electron-beam deposition, and atomic-layer deposition. We have recently demonstrated a method to form nanodots embedded in Lu$_2$O$_3$ using pulse laser deposition for memory device applications. In this work, we report the materials and electrical properties of an ultrathin Lu$_2$O$_3$ film deposited using pulsed laser deposition (PLD) for high k gate dielectric applications...

2. Experimental Procedure

The Lu$_2$O$_3$ thin films were deposited on n-type (100) Si using pulsed laser deposition with base vacuum of $4.5 \times 10^{-7}$ Torr. The wave length of the excimer laser is 248 nm and the energy density is 1.8 J/cm$^2$ with frequency of 5 Hz. The substrates were firstly cleaned using standard cleaning solution (SC) 1, SC2 mixture, and then dipped in a 1% HF solution to remove the native oxide. The Lu$_2$O$_3$ target for PLD was formed using ball milling for 24 hours followed by high temperature sintering. In order to prevent the formation of SiO$_2$ interfacial layer during the thin film deposition, the Lu$_2$O$_3$ films were deposited in high vacuum without introducing any oxygen gas. The thickness of the as-deposited Lu$_2$O$_3$ thin films was about 4.5 nm. After deposition, these Lu$_2$O$_3$ thin films were subjected to a post deposition annealing (PDA) at 900°C for 60 s in oxygen ambient. Top electrodes of Au with a diameter of 0.3 mm were sputtered for electrical measurement. Atomic force microscope (AFM) was used to examine the topology and smoothness of the films. The film thickness and interfacial property were examined using high-resolution transmission electron microscope (HRTEM) with JEOL 2010 microscope. The electrical characteristics of the fabricated MIS devices, capacitance-voltage (C-V) was measured using a precision LCR meter (HP 4284A) at high frequency (100 kHz). A capacitance equivalent thickness of 1.6 nm was obtained for 4.5 nm thick Lu$_2$O$_3$ thin film deposited at room temperature followed by post-deposition anneal at 600 °C in oxygen ambient. The current density vs. voltage (J-V) was measured by a semiconductor parameter analyzer (Keithley 4200).

3. Results and Discussion

The AFM image as shown in Fig. 1 revealed a smooth film topology for the sample annealed at 900°C with a rms roughness value of 0.237 nm and no evidence of micro-crystallization. Figure 2 shows a cross-sectional HRTEM image of the Lu$_2$O$_3$ thin film on the Si substrate after subsequent PDA at 900°C at oxygen ambient. It can be observed from the HRTEM micrographs that the Lu$_2$O$_3$ thin film is relatively uniform and remains amorphous even after an annealing step at 900 °C. Crystallization should be avoided for gate insulator application as it may cause an increase of the gate current through grain boundaries and/or fluctuation of device characteristics. In addition, there is little or no observable interfacial layer seen in the HRTEM images after annealing in oxygen ambient. The HRTEM micrographs show that Lu$_2$O$_3$ is thermally stable, at least up to 900°C, which is close to the high-temperature thermal annealing step for CMOS processing.

The capacitance versus gate voltage characteristics of MIS device (Au/Lu$_2$O$_3$/Si/Au) measured at room temperature is shown in Fig. 3. A high frequency of 100 kHz was employed during the measurement with a voltage sweep from inversion to accumulation of -3 to 3 V bias. A well shaped C-V curve is obtained, from the 900°C oxygen annealed sample. From the C-V curve, the dielectric constant of the deposited Lu$_2$O$_3$ was evaluated from the accumulation capacitance, without taking into account the quantum mechanical tunneling effect (equation 1).

$$C_{\text{high-k}} = C_{\text{acc}} = \frac{k \varepsilon_0 A}{t_{\text{high-k}}}$$

(1)
The dielectric constant obtained is 11.59, which is consistent with previously reported value for Lu$_2$O$_3$ film. The equivalent oxide thickness (EOT) was evaluated by the relation proposed by Devoivre (equation 2), in which an EOT of 1.68 nm was obtained.

$$EOT = \frac{k_{SiO_2} t_{Lu_2O_3}}{k_{Lu_2O_3}}$$  \hspace{1cm} (2)

The flat band voltage $V_{FB}$ was estimated by the relation proposed by Motorola and we obtained a $V_{FB}$ of -400 mV. This value is rather significant but is still lower than previous work on Lu$_2$O$_3$ deposited using electron beam deposition method. The shift in the flat band voltage is normally interpreted as presence of fixed charge in the film, but it can also arise from oxide damage associated with gate electrode deposition or other forms of processing treatments. Presence of a large fixed charge in the gate dielectric can have serious and deleterious effect on the transistor performance as the threshold voltage $V_T$ possibly becomes too large for adequate compensation by dopant implants. A high interface trap density of $\sim 10^{13}$ cm$^{-2}$ eV$^{-1}$ was calculated using a relation proposed by Hill and Coleman (equation 3) where $q$ correspond to electronic charge, $A$ refers to the area of the capacitor, $G_m$ is the maximum conductance, $C_m$ refers to the corresponding capacitance at the maximum conductance, $C_{max}$ is the maximum capacitance at the accumulation region and $\omega$ is the angular frequency.

$$D_n = \frac{\left(\frac{2}{qA}\right)^2 \left(\frac{G_m}{\omega C_{max}}\right)^2 + \left(1 - \frac{C_m}{C_{max}}\right)^2}{\left(\frac{G_m}{\omega C_{max}}\right)^2 + \left(1 - \frac{C_m}{C_{max}}\right)^2}$$  \hspace{1cm} (3)

The presence of large trapped electrons and holes at the interface may reduce the drive current in the MOSFETs as the trapped electrons and holes act like charge scattering centers that lowers the mobility of the mobile carriers traveling in the surface channel. These interface states can also behave like localized generation-recombination centers that can give rise to generation-recombination leakage.
currents and affect the gate dielectric reliability. Therefore, it is necessary to improve on the interfacial properties by considering the deposition and/or annealing processes.

Figure 4 shows the current density versus voltage (J-V) for the ~5 nm thick Lu$_2$O$_3$ film deposited at room temperature followed by an annealing step at 900°C in oxygen ambient. The leakage current density at the off-state of n-type Si substrate at +1 V bias was found to be $1.0 \times 10^{-4}$ A/cm$^2$. The low leakage current is several orders of magnitude lower than thermally grown SiO$_2$ with similar thickness. The low leakage current observed is attributed to the reduced oxygen vacancy as a result for the annealing step in oxygen ambient, thereby reducing the leakage current path.

![Figure 3. C-V characteristics of ~5 nm Lu$_2$O$_3$ film deposited on n-Si(100) substrate subjected to 900°C RTA in oxygen ambient.](image1)

![Figure 4. J-V characteristics of ~5 nm Lu$_2$O$_3$ film deposited on n-Si (100) substrate subjected to 900°C RTA in oxygen ambient](image2)

### 4. Conclusion

Lu$_2$O$_3$ thin films have been deposited on n-type (100) Si substrates using pulsed laser deposition. HRTEM observation illustrated that the Lu$_2$O$_3$ film has amorphous structure and the interface with Si substrate has little or no observable interfacial layer after a high annealing temperature of 900°C in oxygen ambient. A well shaped C-V characteristic was obtained and a $k$ value of 11.59 with an EOT of 1.68 nm was calculated. The amorphous Lu$_2$O$_3$ films showed a low leakage current density of $1.0 \times 10^{-4}$ A/cm$^2$ at +1 V bias for ~5 nm thick Lu$_2$O$_3$ thin film after the post annealing process in oxygen ambient. The results obtained have shown that Lu$_2$O$_3$ has a good potential as a candidate to replace SiO$_2$ as a gate dielectric.

### References

[1] M. Depas, B. Vermeire, P. W. Mertens et al., Solid State Electronics 38, 1465 (1995).
[2] S. H. Lo, D. A. Buchanan, Y. Taur et al., IEEE Electronic Device Letter 18, 209 (1997).
[3] D. Barlage, R. Arghavani, G. Dewey et al., Int. Electron. Devices Meet. Tech. Dig, 231 (2002).
[4] M. Koyama, K. Suguro, M. Yoshiki et al., Int. Electron. Devices Meet. Tech. Dig, 459 (2001).
[5] W. Zhu, T. P. Ma, T. Tamagawa et al., Int. Electron. Devices Meet. Tech. Dig, 463 (2001).
[6] H. Zhong, S. -N. Hong, Y. -S. Suh et al., Int. Electron. Devices Meet. Tech. Dig, 467 (2001).
[7] G. D. Wilk, R. M. Wallace, and J. M. Anthony, Journal of Applied Physics 89 (10), 5243.
[8] J. A. Gupta, D. Landheer, J. P. McCaffrey et al., Applied Physics Letter 78, 1718 (2001).
[9] T. Gougousi, M. J. Kelly, and G. N. Persons, Applied Physics Letter 80, 4419 (2002).
[10] M. Copel, E. Cartier, and F. M. Ross, Applied Physics Letter 78 (1607) (2001).
[11] S. Guha, E. Cartier, M. A. Gribelyuk et al., Applied Physics Letter 77, 2710 (2000).
[12] J. R. Hauser, "Sub-100 nm CMOS, IEDM short course," (1999).
[13] V. Prokofiev, A. I. Shelykh, and B. T. Melekh, J. Alloys Compd 242, 41 (1996).
[14] K. J. Hubbard and D. G. Schlom, J. Mater. Res. 11, 2757 (1996).
[15] D. Xue, K. Betzler, and H. Hesse, J. Phys.: Condens. Matter 12, 3113 (2000).
[16] R. D. Shannon, Journal of Applied Physics 73, 348 (1993).
[17] S. Ohmi, M. Takeda, H. Ishiwara et al., J. Electrochem. Soc. 151 (279) (2004).
[18] N. V. Lathukina, V. A. Rozhkov, and N. N. Romanenko, Microelectronics 23 (48) (1994).
[19] G. Scarel, E. Bonera, C. Wiemer et al., Applied Physics Letter 85, 630 (2004).
[20] C. L. Yuan, P. Darmawan, Y. Setiawan et al., Nanotechnology 17, 3175 (2006).
[21] C. L. Yuan, P. Darmawan, Y. Setiawan et al., Electrochemical and Solid-State Letter 9, F53 (2006).
[22] C. L. Yuan, P. Darmawan, Y. Setiawan et al., Europhysics Letter 74, 177 (2006).
[23] M. Zhu, J. Zhu, J. M. Liu et al., Applied Physics A: Material Science & Processing 80, 135 (2005).
[24] W. A. Hill and C. C. Coleman, Solid State Electronics 23, 987 (1980).