Design of High-Speed Quaternary D Flip-Flop Based on Multiple-valued Current-mode

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Abstract. A new type of quaternary D flip-flop based on multiple-valued current-mode is presented for high-speed sequential circuit in VLSI systems. It employs master-slave mode and dynamic multiple-valued source-coupled logic. A distinguishable multiple-valued interval, fast switch speed and compact structure are obtained by combining source-coupled logic with differential-pair circuit. The performance evaluation is carried out with HSPICE using 0.18μm CMOS process. A performance comparison with those issued in some references is conducted. The delay in our design is about 74% reduced by comparison with the corresponding binary implementation. The circuitry proposed is simplicity, regularity, and modularity, so well suited for VLSI implementation. Quaternary logic seems to be a potential and feasible method of high-performance VLSI systems.

Keywords: Quaternary D Flip-Flop; Quaternary Logic; Multiple-valued Current-mode.

1. Introduction

Two-valued logic has been well developed and widely used in the field of electronic and information. However, with the increasing demands for smarter, smaller and faster, the deficiencies of two-valued logical systems begin to appear. It becomes pretty difficult to meet the all requirements including high-speed switching, low-power dissipation and low-consumption of chip area simultaneously. Based on this, more and more attention has been paid to multiple-valued logical systems[1-4]. One of multiple-valued logic circuit techniques is the multiple-valued current-mode (MVCM) circuitry which performs arithmetic and logic operation with current mode[5-7]. The potential advantage of MVCM integrated circuits is to decrease the number of wires and devices, since a wire is able to transmit more than 1-bit data and the linear sum is easy to be obtained by simply connecting wires together[7-9]. This paper demonstrates a new type of quaternary D flip-flop (DFF) based on multiple-valued current-mode and employing dynamic multiple-valued source-coupled logic (MVSCL) for high-speed sequential circuit of VLSI systems. A MVSCL circuit employs precharge-evaluation mode to decrease the power dissipation, its threshold detectors use differential-pair circuit (DPC) to work under small-swing signals, and thus fast switching can be achieved[10].

2. Fundamental Principles of Dynamic MVSCL Circuits

A general structure of sequential multiple-valued (MV) circuits based on the current-mode is shown in Figure 1, which is composed of three main units, threshold detectors, storage elements and output generators[9-11]. In a MVSCL circuit, both of the threshold detector and the output generator are implemented with DPCs. DPCs can operate at small-swing input voltages in the threshold detector and switch the output currents on or off in the output generator, so low-power dissipation and high-speed for such a MV circuit can be realized[12].
Figure 1. Diagram of sequential multiple-valued circuits

The dynamic MVSCL circuits generally consist of four components, linear sum, I-V convertor, comparator (CMP) and output generator[11]. The schematic diagrams of these basic components are shown in Figure 2.

An input current signal \( I(X) \) firstly is converted into a voltage signal \( V(X) \) by the I-V converter. Then the comparator compares the \( V(X) \) with a reference voltage \( V(T) \) and generates the two-valued differential-pair output signal \((G, G')\). The logical function of comparators is described by Eq. (1).

\[
\begin{align*}
(G, G') &= (0, 1) \quad V(X) > V(T) \\
(G, G') &= (1, 0) \quad V(X) < V(T)
\end{align*}
\]

(1)

The main function of output generators is to produce multiple-valued current-mode differential output signals \((Y, Y')\) depending on the two-valued differential input signals \((G, G')\), and its logical function is described by Eq. (2).

\[
\begin{align*}
(Y, Y') &= (S, 0) \quad (G, G') = (1, 0) \\
(Y, Y') &= (0, S) \quad (G, G') = (0, 1)
\end{align*}
\]

(2)

Figure 2. Schematic diagrams of MVSCL basic components

3. Threshold Detectors Based on Dynamic SCL and DPC

According to the logic characteristics of the comparator described in equation (1), two threshold detectors are needed for transforming the input quaternary signal \( V_{IN} \) into the corresponding binary differential-pair signals. In order to design the two threshold detectors, three comparators named CMP1, CMP2 and CMP3 are designed which thresholds are set as \( V_{0.5}, V_{1.5} \) and \( V_{2.5} \), respectively. The first threshold detector is composed of CMP2, as shown in Figure 3, by which the binary output \((G_A, G_A')\) is
obtained; the second threshold detector is composed of CMP1, CMP3, Nor gate and invertor, shown in Figure 4, by which the binary output (G_B, G_B') is obtained\(^{[13]}\). The three thresholds \(V_{0.5}, V_{1.5}\) and \(V_{2.5}\) are set as 0.6V, 1.2V and 1.6V. The encoding between quaternary input \(V_{IN}\) and binary output (G_A, G_B) are described by Eq. (3)~(4).

\[
G_A = \begin{cases} 
0 & V_{IN} > V_{1.5} \\
1 & V_{IN} < V_{1.5}
\end{cases}
\]

(3)

\[
G_B = \begin{cases} 
0 & V_{IN} < V_{0.5} \text{ or } V_{IN} > V_{2.5} \\
1 & V_{0.5} < V_{IN} < V_{2.5}
\end{cases}
\]

(4)

Figure 3. First threshold detector

Figure 4. Second threshold detector

4. Principles of the Quaternary D Flip-Flop

The proposed quaternary D flip-flop is based on the master-slave mode, its scheme diagram is shown in Figure 5. The master latch consists of two threshold detectors and four pass-gate-invertor latches which
are effective at the same clock logic level as these threshold detectors. The slave latch simply consists of four pass-gate-invertor latches which are effective at the inverted clock logic level with the master latch. The pass-gate-invertor latch consists of a clock-controlled CMOS pass-gate and a CMOS invertor. The output generator is designed with no any clock signals.

The input quaternary signal \( V_{IN} \) firstly compares with the three reference threshold voltages, \( V_{0.5}, V_{1.5} \) and \( V_{2.5} \), and generates binary differential-pair signals \((G_A, G'_A)\) and \((G_B, G'_B)\) depending on the comparison. These generated signals are transmitted to the pass-gate-invertor latches of the master latch and then to the slave latch. If the master latch is effective at the positive phase of clock, the slave latch should be effective at the reverted phase. In this case, the final output \( V_{OUT} \) of the quaternary DFF produced by the output generator comes out on the trailing edge of the clock signal, which is four-valued and corresponding to the original four-valued input signal \( V_{IN} \).

5. Output Generator

The optimized schematic of the Output Generator is shown in Figure 6. There are two branches, \( I_0 \) and \( 2I_0 \), and which one is closed or not is controlled by the signals applied at the gates of these transistors. The currents of the two branches can be summed and form a four-valued output, \( 0, I_0, 2I_0, 3I_0 \), by wiring them together. Every gate of these transistors is driven by the two-valued outputs of the Slave Latches, \((Q_A, Q'_A)\) and \((Q_B, Q'_B)\), so the generated current signal \( I_{OUT} \) corresponds to the original input signal \( V_{IN} \). The current \( I_{OUT} \) is able to be converted into a corresponding voltage \( V_{OUT} \) by a PMOS transistor used as an I-V converter.

6. Evaluation

An evaluation of the presented quaternary DFF is conducted by HSPICE simulation at 100MHz and 1GHz with a 0.18\( \mu \)m CMOS technology. Figure 7 indicates this simulation, in which the clock period is 10ns (100MHz), the input is quaternary voltage signal, and the output quaternary voltage signal is generated on the trailing edge of the clock. Table 1 indicates the input signal, output signal in this simulation, output signal in theory and sequential analysis.
Figure 7. Results of the simulation

Table 1. Input, output in the simulation and output in theory

| Input | clk | 1↓ | 2↓ | 3↓ | 4↓ | 5↓ | 6↓ | 7↓ | 8↓ |
|-------|-----|----|----|----|----|----|----|----|----|
|       | D   | 0.3V-3 | 1.0V-2 | 1.3V-1 | 1.8V-0 | 1.3V-1 | 1.0V-2 | 0.3V-3 | 0.3V-3 |
| Output in the simulation | Qn+ | 0.3V-3 | 1.0V-2 | 1.3V-1 | 1.8V-0 | 1.3V-1 | 1.0V-2 | 0.3V-3 | 0.3V-3 |
| Output in theory | Qn+ | 3 | 2 | 1 | 0 | 1 | 2 | 3 | 3 |

A contrast with those D flip-flop reported in some reference is summarized in Table 2. The delay of the quaternary DFF in this paper is about 74% reduction while the number of transistors increases a little by comparison with the corresponding binary implementation. The number of transistors decreases significantly while the delay becomes a little longer by comparison with the quaternary implementation using a 90nm CMOS process.

Table 2. Performances of D flip-flop in some references and in the paper

| Parameters | In the paper Based on quaternary | References Based on binary | References Based on quaternary |
|------------|---------------------------------|---------------------------|--------------------------------|
| process    | 0.18µm CMOS, 1.8V               | 0.18µm CMOS, 1.8V 2bit-DFF | 0.18µm CMOS, 1.8V D4-2        |
|            | Ref.[14]                        | Ref.[14]                  | Ref. [12]                      |
| Number of transistors | 65                          | 52                         | 49+4C                         |
| Number of nodes | 169                         | --                         | --                            |
| Average of power | 368µW @100MHz                | 132µW @100MHz              | 57.8µW @100MHz                |
| Average of delay | 65ps                         | 249ps                      | 225ps                         |
|              |                                 |                           | 50ps                          |

7. Conclusion

A novel quaternary D-type flip-flop based on multiple-valued current-mode is demonstrated by a circuit structure using DPC together with dynamic SCL. The delay of the quaternary DFF is improved significantly while the hardware complexity almost has no increase by comparison with the corresponding binary implementation. The threshold detector based on DPC makes it possible to obtain distinguishable multiple-value interval for high reliability and to obtain sufficient current driving capability for fast switching speed. The compactness of the quaternary circuitry presented makes it possible to cost little chip area and to decrease power dissipation. In addition, it is simplicity, regularity, and modularity, so well suited for VLSI implementation. Quaternary logic seems to be a potential method of realizing high-performance VLSI systems.
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