Design and Parametric Variation Assessment of Dopingless Nanotube Field-Effect Transistor (DL-NT-FET) for High Performance

Jeetendra Singh1 · Debapriya Chakraborty1 · Naveen Kumar2

Received: 23 March 2021 / Accepted: 27 May 2021 / Published online: 14 June 2021
© Springer Nature B.V. 2021

Abstract
In this paper, a dopingless nanotube field-effect transistor (DL-NT-FET) has been proposed and its performance analysis is carried out by eliminating doping, which is brought in by the application of the charge-plasma technique. A comparative examination of transfer characteristics, transconductance ($g_m$), gate capacitances ($C_{gs}$, $C_{gd}$), output characteristics, output conductance $g_{ds}$, and various performance parameters are investigated by varying the channel length, radius, gate work function, and temperature. Results revealed that increasing the channel length improves subthreshold slope with greater $I_{ON}/I_{OFF}$ and less threshold voltage. It has been also noticed that increase in the radius of the nanotube or an increase in temperature results in just the opposite effect of that observed in the case of increasing channel length. The $I_{OFF}$ value increases significantly on increasing the temperature while the small degradation in the $I_{ON}$ has been noticed as a result of mobility degradation and velocity saturation. The output conductance $g_{ds}$ also degrades on increasing the temperature. A proliferation of 39% is observed in the $C_{gs}$ at the $V_{GS}$ of 0.45 V on increasing the channel length from 20 nm to 35 m whereas no significant changes are observed in the $C_{gd}$ for the same increment in the channel length.

Keywords Nanotube FET · Dopingless · Charge plasma · Output conductance · Average subthreshold slope · Gate capacitance

1 Introduction
The complementary metal-oxide-semiconductor (CMOS) technology has advanced through the decades to dominate the semiconductor industry with excellent features of low power and cost, dense packaging, and high-speed devices that are continuously scaled down in size [1–3]. When it comes to designing RF/analog circuits in the nanometer regime, several challenges have been encountered due to strict process requirements to maintain sharp source/drain region and short channel effects (SCEs) [4–7]. The electrostatic technique to add doping include additional fabrication steps and hence fabrication cost and complexity [8, 9]. The junctionless field-effect transistor (JLFET) solves many of the issues related to SCEs but still, it suffers from poor carrier mobility due to high channel doping, which leads to transconductance/gain degradation and hence low ON current [10, 11]. Dopingless nanotube FET (DL-NT-FET) can provide a solution by making use of the charge-plasma (CP) technique in which abrupt doped source and drain regions are formed in the intrinsic substrate with the help of suitable work function metal electrode or poly-Si electrode at the high temperature [12–14]. The gate-all-around (GAA) and shell-gated nanotube provide strong gate control over the channel carrier which results in enhanced surface inversion and hence superior drain current [15, 16]. Hence, the proposed device exploits both the advantages of GAA structure (i.e. allowing better electrostatics and reduced SCEs) and dopingless configuration (like reduced random dopant fluctuations(RDFs), less mobility degradation, better gm) [17, 18]. Besides the collective merit of GAA and dopingless nanotube, the impact of temperature on the performance parameters of the proposed DL-NT-FET is the first time investigated along with other design parameters.

Jeetendra Singh
jeetendras15.phd@nitj.ac.in

Debapriya Chakraborty
debapriya2014chak@gmail.com

Naveen Kumar
nk9727@gmail.com

1 Department of ECE, NIT Sikkim, Sikkim, India
2 Dr. B R Ambedkar NIT Jalandhar, Jalandhar, India
In this article, a dopingless nanotube field-effect transistor (DL-NT-FET) is designed and its various performance parameters; transfer characteristics ($I_D$-$V_{GS}$), transconductance ($g_m$), gate capacitances ($C_{gs}$ and $C_{gd}$), output characteristics ($I_D$-$V_{DS}$), output conductance ($g_{ds}$), average subthreshold slope (AVSS), the threshold voltage ($V_t$), the ratio of on-current to off-current ($I_{ON}/I_{OFF}$) are investigated. The impact of nanotube radius ($R$), channel length ($L_g$), and gate work function variations on the performance parameters are examined to achieve high performance. The various performance parameters are also evaluated at a different temperature to study the temperature-dependent variability.

### 2 Device Structure

The 2-D structure of the proposed device is shown in Fig. 1(a) whereas the 3-D structure of the same is depicted in Fig. 1(b). The source, channel, and drain regions have been formed on an intrinsic Si body with the radius being 10nm and the silicon thickness being 7nm leaving the inner oxide thickness. CP technique is used to establish the source and drain regions of this dopingless device [19]. The gate oxide is made of SiO$_2$ and is 2nm in thickness. Both drain and source lengths are 30nm while the channel length is 20nm. P-type polysilicon (workfunction = 3.9 eV) is used in forming the source and
drain core-electrodes. The gate contact is also made of polysilicon (workfunction = 4.6 eV). The poly-Silicon core-electrodes help to induce N+ regions at the source and drain sides. A SiO2 layer surrounds these electrodes followed by an intrinsic Silicon layer in the core. Poly-silicon electrodes are also attached at the bottom and top of this layer. The second layer of SiO2 is muffled on all sides of the Si layer. A shell consisting of polysilicon (work function = 4.6 eV) has been wrapped over the oxide layer to form a contact for the gate. Aluminum is generally preferred for gate material of MOSFET but here the polysilicon is mainly utilized because polysilicon composition matches with the channel bulk-silicon and therefore offers low threshold voltage as compared to that of metal gate material [20]. The proposed device is simulated utilizing Silvaco TCAD to analyze the various results. To account for accurate mobility evaluation in the channel, the Lombardi mobility model along with concentration and field-dependent mobility models are considered. Shockley–Read–Hall (SRH) and Auger generation-recombination models are contemplated to acknowledge the lifetime of constant minority carriers and large current density. The simulation temperature was initially 300 K for the
proposed device and then observations were also taken at different temperatures to compare the effect on different device parameters.

The variation of the electron-hole concentration and the energy band diagram of the proposed DL-NT-FET is illustrated in Fig. 2 for OFF-state conditions \((V_{GS}=0 \text{ V} \text{ and } V_{DS}=1 \text{ V})\) and ON-state conditions \((V_{GS}=1 \text{ V} \text{ and } V_{DS}=1 \text{ V})\) respectively. As it can be noticed from Fig. 2(a) that the concentration of the electrons in the channel region goes high from the low and the holes concentration goes low from high when the device comes into the ON-state condition from OFF-state condition due to the formation of the inversion layer of the electrons and depletion of the holes from the channel [21]. The energy levels of the conduction band and valence band are high in the OFF-state condition as compared to the energy levels of the conduction band and valance band in the ON-state condition Fig. 2(b). The bands bend downwards in ON-state because when a positive gate voltage is applied in the polysilicon gate, the Fermi potential (potential between Fermi level and intrinsic Fermi level) decreases due to an increase in the surface potential, and this result in large electron carriers in the intrinsic (initially) channel region [22]. The introduction of these high electrons shifts the conduction band down towards the Fermi level. Simultaneously the holes are also de-voided from the channel due to positive potential on the gate therefore the valance band also shifts downwards away from the Fermi level.

Figure 3 depicts the variation of electric field and potential in the OFF-state and ON-state conditions. It can be seen from Fig. 3(a) that the electric field uplifts in the interface of source-channel and suppressed at the interface of channel-drain when the device comes in the ON-state condition from the OFF-state, this is due to the application of the positive gate voltage along with the drain voltage [23]. The low electric field at the channel-drain interface indicates less control of the drain to the channel and hence the DL-NT-FET implies low short

---

**Fig. 5** Variation of I-V characteristics for doped and doping-less Nanotube FET

---

**Fig. 6** Variation of \((I_{D_{\infty}}V_{GS})\) characteristics of the DL-NT-FET at \(V_{DS}=1 \text{ V}\) for (a) the varying the channel length \((L_g)\) (b) the varying the gate electrode work function \((\Phi_G)\) (c) at various temperature \((T)\), and (d) the varying the radius \((R)\) of the DL-NT-FET.
channel effects. On the other hand, the surface potential goes high in the ON-state as intended due to more bending in the energy bands, at this stage the surface becomes doubled that of Fermi potential.

Figure 4 shows the variation of the electron mobility and electron-hole pair recombination rate of the DL-NT-FET in OFF-state and On-state conditions. The electron mobility goes lower at the source-channel interface and becomes higher at the channel-drain interface Fig. 4(a). It is because the electric field is higher at the source-channel interface and lower at the channel-drain interface as is seen in Fig. 3(a). It can be observed from Fig. 4(b) that the recombination rate of the electron-hole pairs is zero in the channel region ON-state condition of the device channel region.

The impact of doped and doping-less I-V characteristics of nanotube-FET are plotted in Fig. 5. The source and drain region of the device are initially induced with the help of charge plasma technique to form the doping-less device while for the doped case both the region are defined and doped with the same doping level. It has been seen from the Fig. 5 that there is no changes in the drain current for both the cases so charge plasma technique can be beneficially exploited instead of doped technique so that fabrication steps will be reduced.

The drain current variation with channel length is plotted in Fig. 6(a) and its extracted performance parameters are listed in Table 1, it is noted that on increasing the channel length the ION/IOFF ratio enhances while the threshold voltage and Average sub-threshold slope (AVSS) of the DL-NT-FET reduce. An augmentation of 2 orders in the ION/IOFF ratio and a reduction of 22 and 13 % in the threshold voltage and AVSS respectively have been recorded on increasing the channel length from 15 nm to 35 nm. The impact of the gate work function variation on the transfer characteristics of the DL-NT-FET is shown in Fig. 6(b) and various device properties that are extracted from its transfer characteristics are mentioned in Table 2. It can be observed that the OFF-current (IOFF) reduces significantly as compare to the ON-current (ION) and therefore the ION/IOFF ratio enhances on increasing

| Gate-work function (eV) | AVSS (mV/decade) | Threshold voltage(V) | ION (A/m) | IOFF (µA/m) | ION/IOFF |
|-------------------------|------------------|----------------------|-----------|-------------|----------|
| 4.3                     | 70.7             | 0.494785             | 41.29     | 930,287     | 44.3891  |
| 4.4                     | 68.7             | 0.394785             | 38.03     | 52766.2     | 720.727  |
| 4.5                     | 68.4             | 0.294785             | 34.53     | 1935.24     | 17845.3  |
| 4.6                     | 68.8             | 0.194785             | 30.93     | 64.15       | 482.264  |
| 4.7                     | 71               | 0.0947849            | 27.21     | 2.04        | 13,316,400 |

| Channel length (nm) | AVSS (mV/decade) | Threshold voltage(V) | ION (A/m) | IOFF (µA/m) | ION/IOFF |
|---------------------|------------------|----------------------|-----------|-------------|----------|
| 15                  | 74.58            | 0.219144             | 31.15     | 367.3       | 84711.9  |
| 20                  | 68.8             | 0.194785             | 30.93     | 64.15       | 482.264  |
| 25                  | 67.7             | 0.18286              | 30.81     | 21.95       | 1,403,350 |
| 30                  | 66.0             | 0.176297             | 30.70     | 11.26       | 2,725,660 |
| 35                  | 64.57            | 0.170009             | 30.57     | 7.38        | 4,141,140 |

| Temperature (K) | AVSS (mV/decade) | The threshold voltage(V) | ION (A/m) | IOFF (µA/m) | ION/IOFF |
|-----------------|------------------|--------------------------|-----------|-------------|----------|
| 200             | 48               | 0.14432                  | 31.9      | 0.024       | 1,287,990,000 |
| 250             | 58.6             | 0.168484                 | 31.44     | 2.68        | 11,714,000 |
| 300             | 68.8             | 0.194785                 | 30.93     | 64.15       | 482,264  |
| 350             | 80.7             | 0.222111                 | 30.40     | 637.585     | 47691.7  |
| 400             | 89.2             | 0.249834                 | 29.83     | 3624.34     | 8232.48  |
| 450             | 103.3            | 0.277697                 | 29.22     | 14074.1     | 2076.18  |
the gate work function. The threshold voltage also decreases on augmenting the gate work function whereas the AVSS initially decreases up to a work function of 4.5 eV but then starts increasing. Six orders increment in the $I_{ON}/I_{OFF}$ ratio and an 81 % reduction in the threshold voltage has been observed when the gate work function is augmented from 4.3 eV to 4.7 eV. Figure 6(c) exhibits the variation of $I_D-V_{GS}$ characteristics with temperature. The various performance parameters at different temperatures are summarized in Table 3. The $I_{OFF}$ value increases significantly on increasing the temperature while the small degradation in the $I_{ON}$ has been noticed as a result of mobility degradation and velocity saturation. And therefore 6 orders diminution in the $I_{ON}/I_{OFF}$ ratio is noticed when the temperature is increased from 200 to 450 K.

The AVSS both are rose with the temperature. The threshold voltage rises 92 % while the AVSS rises 114 % on increasing the temperature from 200 to 450 K. The effect of nanotube radius on the transfer characteristics and hence on various performance parameters are depicted in Fig. 6(d) and Table 4 respectively. On enhancing the radius of the nanotube of the DL-NT-FET, the $I_{ON}$ and $I_{OFF}$ both are increasing but the $I_{OFF}$ increases more rapidly as compare to the $I_{ON}$ and therefore the $I_{ON}/I_{OFF}$ ratio reduces. The $I_{ON}/I_{OFF}$ ratio is degraded by 3 orders on augmenting the radius from 8 nm to 16 nm. The threshold voltage and AVSS are increased by increasing the radius of the nanotube; there is an increment of 47 % in threshold voltage whereas an increment of 19 % in the AVSS has been observed while increasing the radius of the nanotube from 8 nm to 16 nm.

Figure 7(a) shows the variation of transconductance with $V_{GS}$ at different channel lengths which is a specific figure of merit of a FET and it measures the precision in the conversion of gate voltage into the current. It is noticed from Fig. 7(a) that the transconductance increases with the increasing channel length (up to 25 nm) then it remains constant. The transconductance increases with the channel length because of higher change in drain current is obtained at the large channel length with a small change in gate voltage. At the 25 nm channel length, the obtained value of the $g_m$ is $5.2 \times 10^{-5}$ S/$\mu$m at the gate voltage of 0.45 V. Figure 7(b) depicts the changes in the gate to source capacitance ($C_{gs}$) and drain to source capacitance ($C_{gd}$) with the gate voltage. A proliferation of 39 % is observed in the $C_{gs}$ at the $V_{GS}$ of 0.45 V on increasing the channel length from 20 nm to 35 m whereas no significant changes are observed in the $C_{gd}$ for the same increment in the channel length.

| Radius(nm) | AVSS (mV/decade) | The threshold voltage(V) | $I_{ON}$ (A/m) | $I_{OFF}$ (µA/m) | $I_{ON}/I_{OFF}$ |
|------------|------------------|-------------------------|---------------|-----------------|-----------------|
| 8          | 67.5             | 0.178221                | 24.17         | 13.05           | 1,852,290       |
| 10         | 68.8             | 0.194785                | 30.93         | 64.15           | 482,264         |
| 12         | 72.2             | 0.212351                | 37.72         | 298.04          | 126,582         |
| 14         | 78.1             | 0.231078                | 44.63         | 1308.17         | 34,118          |
| 16         | 80.3             | 0.250602                | 51.70         | 5366.02         | 9635.24         |

Fig. 7 Variation of (a) transconductance ($g_m$) and (b) gate to source capacitance ($C_{gs}$) and gate to drain capacitance ($C_{gd}$) with gate voltage at various channel length and $V_{DS} = 1$ V.
The behavior of drain current concerning $V_{DS}$ for different values of $V_{GS}$ at the channel length of 20 nm and 35 nm has been shown in Fig. 8(a), where it is again found that $I_D$ is more for channel length 20 nm than that of for channel length 35 nm. Moreover, it is also noticed that at smaller $V_{GS}$, the saturation in the drain current occurs earlier as compared to the large $V_{GS}$; this is because of limited space-charge inversion in the channel which implies greater gate control over the channel. Figure 8(b) shows how the output conductance ($g_{ds}$) varies with $V_{DS}$ where $V_{GS}$ is fixed at 1 V and readings for 20 nm and 35 nm channels are taken. It is well known that $g_{ds}$ is a crucial parameter in determining the intrinsic gain of a device and for better gain, it should be low. It can be seen from Fig. 8(b) that its value does not change with the channel length and the obtained value of the $g_{ds}$ for the designed DL-NT-FET is $3.4 \times 10^{-5}$ (S/μm).

The output characteristics ($I_D-V_{DS}$) at the various temperatures are plotted in Fig. 9(a) and it is observed that the drain current decreases with an increase in the temperature. The $I_D$ decreases with the temperature because scattering phenomena increase with the temperature and these results in low carrier mobility in the channel and hence low drain current at the higher temperature [24]. The $I_D$ degrades 15% on increasing the temperature from 200 K to 400 K. Figure 9(b) shows the variation of the output conductance ($g_{ds}$) with the $V_{DS}$ at different temperature and it is found that $g_{ds}$ also degrades on increasing the temperature and it is due to the reduction of $I_D$ at the higher temperature.

The impact of the nanotube radius in the output characteristics and output transconductance is plotted in Fig. 10(a) and (b) respectively and it is found that both the parameters are increasing with augmenting the radius. The $I_D$ enhances the increasing radius because a large radius renders large space charges in the inversion condition and the large drain current implies the higher output transconductance. An increment of 100% in the drain current and 137% in the output transconductance has been noted when the radius of the nanotube increases from 8 nm to 16 nm.

![Fig. 8](a) Output characteristics for channel lengths 20nm and 35nm at different VGS. (b) Output conductance vs. $V_{DS}$ for channel lengths 20nm and 35nm at $V_{GS}$=1 V

![Fig. 9](a) Variation of (a) output characteristics ($I_{DS}-DS$) at different temperatures and (b) output conductance for different temperatures (both at $V_{GS}$=1 V)
3 Conclusions

This manuscript covers a proposed dopingless nanotube FET structure. Different characteristics of the device have been examined by TCAD simulated results. The obtained AVSS for 20nm channel length, the radius of 10nm simulated at 300 K is 68.80mV/decade which has much scope of improvement by optimization of the device. A comparative analysis of transfer characteristics ($I_D$-$V_{GS}$), transconductance ($g_m$), gate capacitances ($C_{gs}$ and $C_{gd}$), output characteristics ($I_D$-$V_{DS}$), and output conductance ($g_{ds}$), has been made by varying the channel length ($L_g$), radius ($R$), gate work function ($\Phi$) and temperature. An increment of 100% in the drain current and 137% in the output transconductance has been noted when the radius of the nanotube increases from 8 nm to 16 nm. The gate capacitances $C_{gs}$ and $C_{gd}$ are higher for the longer channel. On increasing the temperature from 300k to 400 K, the output conductance is found to decrease as well as the drain current gets saturated to a lower value whereas, by decreasing temperature to 200 K, the opposite happens. An augmentation of six orders in the $I_{ON}/I_{OFF}$ ratio and 81% reduction in the threshold voltage has been observed when the gate work function is enhanced from 4.3 eV to 4.7 eV. The $I_{ON}/I_{OFF}$ decreases with a temperature rise, there are 6 orders diminution in the $I_{ON}/I_{OFF}$ ratio is noticed when the temperature is increased from 200 to 450 K. The threshold voltage and the AVSS both are rose with the temperature. The threshold voltage rises 92% while the AVSS rises 114% on increasing the temperature from 200 to 450 K. The transconductance curve has the highest peak value for the longest channel. It can thus be concluded that, after a thorough investigation of the behavior of the proposed dopingless nanotube FET parameters under several variations, it can be well understood that there are a good number of challenges to get the optimized results.

Author Contributions All authors have equally participated in the preparing of the manuscript during implementation of ideas, findings results, and writing of the manuscript.

Data Availability Current submission does not contain the pool data of the manuscript but the data used in the manuscript will be provided on request.

Declarations

Conflict of Interest The authors declare that they have no conflict of interest.

Ethical Standard The Authors accepted principles of ethical standard and they have no conflict of interest.

Consent to Participate Informed consent.

Consent for Publication Consent is granted.

References

1. Huang JST, Schrankler JW (1987) Switching characteristics of scaled CMOS circuits at 77 K. IEEE Trans Electron Devices 34(1):101–106
2. Kong L, Chen Y, Liu Y (2021) Recent progresses of NMOS and CMOS logic functions based on two-dimensional semiconductors. Nano Res 14:1768–1783
3. Singh J, Raj B (2019) Design and investigation of T72M-NVSRAM with enhanced stability and temperature impact on store/restore energy. IEEE Trans Very Large Scale Integr VLSI Syst 27(6):1322–1328
4. Pourghaderi MA, Pham AT, Ilatikhameneh H, Kim J, Park HH, Jin S, Chung WY, Choi W, Maeda S, Lee KH (2017) Universality of short-channel effects on ultrascaled MOSFET performance. IEEE Electron Device Lett 39(2):168–171
5. Ribeiro TA, Pavanello MA, 2020, February. analysis of the electrical parameters in SOI n-type junctionless nanowire transistors at high temperatures. In: 2020 IEEE Latin America Electron Devices Conference (LAEDC) (pp. 1–4). IEEE, New York
6. Sahu C, Parmar JS, 2017, July. Analog/rf performance comparison of junctionless and dopingless field effect transistor. In: 2017 International Conference on Computer, Communications and Electronics (Comptelix) (pp. 606–611). IEEE, New York
7. Chebaki E, Djellal F, Ferhati H, Bentrcia T (2016) Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions. Superlattices Microstruct 92:80–91
8. Bala S, Khosla M (2018) Electrostatically doped tunnel CNTFET model for low-power VLSI circuit design. J Comput Electron 17(4):1528–1535
9. Bala S, Khosla M (2018) Design and analysis of electrostatic doped tunnel CNTFET for various process parameters variation. J Superlattices Microstructures 124:160–167
10. Kuhn K (2018) Cmos and beyond cmos: Scaling challenges. In: High Mobility Materials for CMOS Applications. Woodhead Publishing, Cambridge, pp 1–44
11. Trojman L, Ragnarsson L, Collaert N (2019) Mobility extraction for short channel UTBB-FDSOI MOSFETs under back bias using an accurate inversion charge density model. Solid State Electron 154:24–30
12. Shan C, Wang Y, Bao MT (2016) A charge-plasma-based transistor with induced graded channel for enhanced analog performance. IEEE Trans Electron Devices 63(6):2275–2281
13. Kumar N, Amin SI, Anand S (2020) Design and performance optimization of novel core–shell dopingless GAA-nanotube TFET with Si 0.5 Ge 0.5-based source. IEEE Trans Electron Devices 67(3):789–795
14. Gupta AK, Raman A (2020) Performance analysis of electrostatic plasma-based dopingless nanotube TFET. Appl Phys A 126(7):1–10
15. Mushtaq U, Kumar N, Anand S, Amin I (2020) Design and performance analysis of core-shell dual metal-dual gate cylindrical GAA silicon nanotube-TFET. Silicon 12(10):2355–2363
16. Tayal S, Nandi A (2018) Optimization of gate-stack in junctionless Si-nanotube FET for analog/RF applications. Mater Sci Semicond Process 80:63–67
17. Liu M, Lentz F, Trenkamp S, Hartmann JM, Knoch J, Grützmacher D, Buca D, Zhao QT (2020) Diameter scaling of vertical Ge gate-all-around nanowire pMOSFETs. IEEE Trans Electron Devices 67(7):2988–2994
18. Raad BR, Sharma D, Kondekar P, Nigam K, Yadav DS (2016) Drain work function engineered doping-less charge plasma TFET for ambipolar suppression and RF performance improvement: a proposal, design, and investigation. IEEE Trans Electron Devices 63(10):3950–3957
19. Oks EM (1992) Physics and technique of plasma electron sources. Plasma Sources Sci Technol 1(4):249
20. Gusev EP, Narayanan V, Frank MM (2006) Advanced high-κ dielectric stacks with polySi and metal gates: Recent progress and current challenges. IBM J Res Dev 50(4.5):387–410
21. Sallese JM, Bucher M, Krummenacher F, Fazan P (2003) Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model. Solid State Electron 47(4):677–683
22. Kang SM, Leblebici Y (2003) CMOS digital integrated circuits. Tata McGraw-Hill Education, New York
23. Assaderaghi F, Parke S, Sinitsky D, Bokor J, Ko PK, Hu C (1994) A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation. IEEE Electron Device Lett 15(12):510–512
24. Blatt FJ (1957) Scattering of carriers by ionized impurities in semiconductors. J Phys Chem Solids 1(4):262–269

Publisher’s Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.