Using Novel One-Bit ADC to Design \( n \)-Bit ADC

Yasser S. Abdalla

Abstract: This work presents two novel styles for designing \( n \)-bit analog to digital converter (ADC). Each of the proposed ADCs is built using novel one-bit cell. The novel cell produces single output bit as a response to an input voltage, in addition, it outputs another analog voltage. The generated analog voltage is used again as an input to the to generate one more bit, and new analog voltage, and so on. The proposed \( n \)-bit ADC is built using the novel one-bit cell in two different styles. One design style, by connecting \( n \) ADC cells together to construct \( n \)-bit ADC that produces parallel binary outputs. The other design style realizes the \( n \)-bit ADC using single ADC cell and outputs \( n \)-bit serially. In both ADC designs introduced in this work, modularity was the main design parameter. The two different \( n \)-bit ADCs have been simulated. The first \( n \)-bit ADC with parallel outputs produces clean outputs at 50MS/s, and the other ADC design shows clean serial bits at 5Ks/s.

Keywords: ADC, Analog-Mixed signal, Serial output, and Parallel Output

I. INTRODUCTION

The nature of quantities like voice, velocity, and temperature are analog. Though, most recent electronic devices are digital. As a result, the necessity for extra (ADC) design diversities is unavoidable. Initial analog to digital converter was offered in 1921. Then, several ADC schemes was issued [1-2]. Circuit designers carry on redesigning ADCs with altered styles and diverse topologies. The architecture of an ADC should be designed for specific performance parameter [3]. Also, the design technique may target technology generation, or any other performance parameter [4-18]. However, not any of the ADC converters was designed for modularity which attained in this paper.

II. PROPOSED ADC

A. Idea

The suggested ADC design excerpts binary outputs as one bit at a time. It begins from most significant bit, and move toward the least significant bit. In order to recognize operation of the planned ADC, look at Fig. 1 that enlightens 16-level with the corresponding 4-bit coding. As presented, the central level \( Lm \) that splits the input range from the middle is used to evaluate MSB b3. When input is above \( Lm \), MSB for b3 becomes one, and when it is below \( Lm \), b3 is zero. After estimating b3, it will has no effect on the assessment the next bits. As presented, the patterns which define the remaining bits splits around \( Lm \) into similar parts where \( Lq1 \), and \( Lq2 \) separate them to produce 4 quaters. Then, b2 is assessed using its location compared to \( Lq1 \) when b3 equals one, otherwise, b2 is identified using its location compared to \( Lq2 \) when b3 equals zero.

Correspondence among the two levels, \( Lq1 \), and \( Lq2 \) in the upper and lower halves respectively when discounting b3 is seen another time among \( Le1 \), \( Le2 \), \( Le3 \), and \( Le4 \) when b3, and b2 are discounted.

| b3 | b2 | b1 | b0 | \( Le1 \) | \( Lq1 \) | \( Le2 \) | \( Lq2 \) | \( Lm \) |
|----|----|----|----|-----|-----|-----|-----|-----|
| 1  | 1  | 1  | 1  | 0   |     |     |     |     |
| 1  | 1  | 0  | 1  |     | 1   |     |     |     |
| 1  | 1  | 0  | 0  |     |     | 0   |     |     |
| 1  | 0  | 1  | 1  |     |     |     | 0   |     |
| 1  | 0  | 0  | 1  |     |     |     |     | 0   |
| 0  | 1  | 1  | 1  |     |     |     |     |     |
| 0  | 1  | 0  | 0  |     |     |     |     |     |
| 0  | 0  | 1  | 1  |     |     |     |     |     |
| 0  | 0  | 0  | 1  |     |     |     |     |     |

Fig. 1 The 16-level and the corresponding bits

The transformation from analog to digital may written as series of stages. These stages could be explained after looking at Fig. 2(a). Dual analog values X, and Y are taken into consideration. The level at X is above \( Lm \) by H. Likewise, Y is above \( Lmin \) by a H. Because X is above \( Lm \), the output MSB resembles to X is one. In contrast, the output MSB resembles to Y is zero. After estimation of MSB regarding X, and Y the following bit to be estimated for them both will be recognized based on its location compared to \( Lq1 \), and \( Lq2 \) correspondingly. Remember. \( Lm \) is in the middle of ADC input range. Therefore, the value of \( Lm \) is deducted from range that is higher than \( Lm \), that upper half shifted so that \( Lm \) overlaps with \( Lmin \). Hence, the ADC range showed at Fig. 2(a) is transformed to be two equivalent halves as seen in Fig. 2(b). Levels \( Lq1 \), and \( Lq2 \) at this situation have equivalents magnitudes equals that of \( Lm \). Magnifying the both halves seen at Fig. 2(b) by a two preserve the relative locations among the quantization levels and points X, and Y as presented in Fig.2(c).

The next bit from the MSB side on behalf of X, and Y is assessed by comparison of their value to that of \( Lm \). Same procedure is repeated for other bits at the output up to the targeted accuracy.. Fig. 3 encapsulates the predictable series of steps which explain the procedure of the suggested ADC.
Using Novel One-Bit ADC to Design n-Bit ADC

Fig. 2 (a) Full range (b) the upper and the lower halves of analog range have combined (c) combined halves after being magnified by 2.

Fig. 3 Operation stages of the proposed ADC.

B. Suggested ADC Cell

Fig. 4(a) presents the architecture of the suggested ADC cell. It is built to obey the procedure depicted in Fig. 3 where $V_{in}$ is compared to the reference voltage $V_m$ which is equivalent to voltage of $L_m$. The cell’s output bit is taken from the comparator. It is one when $V_{in}$ is larger than $V_m$, else it is zero. The voltage $V_c$ controls an analog multiplexer so that $V_a$ becomes GND if $V_c$ represents zero and becomes $V_m$ if $V_c$ represents one. The subtractor that appears at the end has gain of 2. It is used to subtract $V_a$ from $V_{in}$, then multiply the subtraction output by 2. Hence, the subtractor’s output $V_n$ is just a modified version from $V_{in}$. Now, $V_n$ characterizes two values which just have a change at the preceding bit while all the other bits are identical. It also scaled up by two so that it can be compared again with $V_m$ which is the analog value at the midrange quantization level $L_m$ as explained before. For simplification, the symbol of the ADC cell displayed at Fig. 4(b) is used in the remaining work.

The delays that affect the suggested ADC cell; the delay of the output’s bit $T_c$, and the delay required for the signal $V_n$ to be set $T_n$. The delay $T_c$ caused by the comparator and it is likely to be minor. The delay $T_n$ is assembled from three delays and expressed as:

$$T_n = T_c + T_a + T_s \quad (1)$$

Where $T_c$ is comparator’s delay, $T_a$ is multiplexer’s delay, and $T_s$ is the subtractor’s delay.
Fig. 4 (a) Novel ADC cell block diagram (b) symbolic representation

A circuit design for the suggested ADC cell is displayed in Fig. 5 with the op-amp OP1 works as a comparator, MOS transistor M1 in addition to R1 acting as a multiplexer, the op-amp OP2 is a buffer, and op-amp OP3 is connected with 4 resistors to act as a subtractor that have gain of 2. The comparator OP1 compares between input voltage Vin and the midrange Vm so that Vc is high when Vin above Vm and low else. The voltage Vc the ADC cell’s output bit which also controls the multiplexer. If Vc is high, M1 is turned on permitting Vm to pass and reach to the input Va of OP2. The MOS M1 is turned off if Vc is low, results in Vm is obstructed and Va of OP2 is grounded through R1.

Fig. 5 ADC cell’s schematic

C. Schematic of Cascade ADC

An n-bit cascade ADC design is displayed at Fig. 6. It is assembled from n ADC cells where subtractor’s output of each ADC cell applied to the input of the following ADC cell. The first bit to be estimated should be the MSB Bn that becomes ready after delay that equals to Tc for the 1st cell. Then, Bn-1 is estimated and becomes ready after a delay equivalent to the sum of the delay required for Vn to be prepared Tn and the comparator-delay of the 2nd cell. The delay of the output bit Bm generally given by (2):

\[ T_{B_m} = (n - m)T(n) + (n - m + 1)Tc \]

(2)

Where \( T_{B_m} \) is the delay needed for the digital output bit associated with the ADC cell number m.

The number of the demanded bits is equivalent to the number of ADC cells used. This modular construction of the suggested ADC is the foremost benefit of that way of designing the analog to digital converters.

Fig. 6 Cascaded n-bit ADC

A circuit design of the suggested Cascade ADC is displayed in Fig. 7 which built using the cell presented in Fig. 5.

D. The One-Cell n-bit ADC Schematic

Just one ADC cell is configured to achieve n-bit ADC. Its illustration is displayed at Fig. 8 with the addition of 2 exclusive analog switches that controls the ADC cell’s input. The first switch AS1 be governed by clock \( \Phi 1 \) such that it becomes low-impedance connection if \( \Phi 1 \) is high permitting Vin to charge/discharge Cin until Vcin becomes equivalent to Vin. On the other hand, when \( \Phi 1 \) is low, AS1 becomes open-circuit leaving the charge on Cin to be stuck, hence, maintain Vcin unaffected. After Tn, which is the 1st ADC cell’s delay before its output bit is attained, and Vn becomes ready to drive next output bit production. Instead of using the voltage Vn as input to another ADC cell, it is fed-back to the input of the same ADC cell through AS2.

The switch AS2 is operated using clock \( \Phi 2 \) in a way that it turns to be low-impedance connection if \( \Phi 2 \) is high permitting Vn to flow and charge/discharge Cin until Vcin equalized to the feedback voltage Vn. And if \( \Phi 2 \) is low, AS2 is converted to open-circuit leaving the charge on Cin stuck, and Vcin unaffected.

An n-bit ADC can be design based on this schematic with suitable control of clocks \( \Phi 1 \), and \( \Phi 2 \) as follows:

1. Clock \( \Phi 1 \) is activated to sample the input voltage Vin.

2. Clock \( \Phi 1 \) is deactivated
Using Novel One-Bit ADC to Design n-Bit ADC

3- After delay Tn, the output bit is read and the Φ2 is activated to sample the feedback voltage Vn.
4- Clock Φ2 is disabled
5- If more output bit is needed, repeat steps 3, and 4, else go to step 1.
Clocks Φ1, and Φ2 must be non-overlapping clock as displayed in Fig. 9

![Fig. 8 One-cell n-bit serial ADC](image)

![Fig. 9 The non-overlapping clocks Φ1 and Φ2](image)

![Fig. 10 Circuit of one-cell n-bit serial ADC](image)

III. SIMULATION RESULTS

The schematic displayed in Fig. 7 for a 6-bit ADC simulated when the used stimulus Vin as presented in Fig. 11. Vin changes each 20ns. The analog output of the 1st ADC cell which also used to drive the 2nd cell is displayed in Fig. 12. Likewise, the following five figures up to Fig 17 portray the analog outputs of the other cells. The simulated waveforms of the output bits are displayed from Fig. 18 to Fig. 23.

A 1.5 GHz ultrahigh speed operational amplifier is used.
The ADC reach to a speed of 50MS/s and an analog input range of 8V.

The schematic displayed in Fig. 10 is simulated at speed 5k S/s. The simulated waveforms of Φ1, and Φ2 are displayed in Fig. 24, and the sequential binary output in Fig. 25 with range of input equals 8V. The simulation results are summarized in Table-1.

![Fig. 11 Input Vin](image)

![Fig. 12 Input of the 2nd cell V5](image)

![Fig. 13 Input of the 3rd cell V4](image)

![Fig. 14 Input of the 4th cell V3](image)

![Fig. 15 Input of the 5th cell V2](image)

![Fig. 16 Input of the final cell V1](image)

| Table-1: Summary of Simulation Results |
|----------------------------------------|
| Input Range | speed | Number of ADC cells |
| Cascade ADC | 8V    | 50MS/s | 6 |
| Serial ADC  | 8V    | 5kS/s  | 1 |

Retrieval Number: K2237098119/2019 ©BEIESP
DOI: 10.35940/ijitee.K2237.0981119
Fig.17 O/p of the final cell V0

Fig.18 Bit B5

Fig.19 The output bit B4

Fig.20 The output bit B3

Fig.21 Output bit B2

Fig.22 The output bit B1

Fig.23 The output bit B0

Fig.24 The two clocks Φ1 and Φ2

Fig.25 The serial output

IV. CONCLUSION

In this paper, a generalized configurable ADC cell is presented. Realizations of ADC designs based on this ADC cell are presented to confirm the idea supported by simulation results. The two proposed circuits were designed for modularity. They show rational results when simulated. Additional ADC configurations can be targeted as a future work that are based on the architectures presented.

REFERENCES

1. Newnes, Analog Devices, The Data Conversion Handbook, (2005).
2. Kertis R. A. A 20 GHz 5-Bit SiGe BiCMOS Dual-Nyquist Flash ADC With Sampling Capability up to 35 GS/s Featuring Offset Corrected Exclusive-Or Comparators. IEEE Journal of Solid-State Circuits, 44(9), 2295 – 2311, Sept. (2009).
3. Murmann B. A/D converter trends: Power dissipation, scaling and digitally assisted architecture. Custom Integrated Circuits Conference, 105 – 112, Sept. (2008).
4. Ali A. A 16b 250 MS/s IF-sampling pipelined ADC with background calibration. IEEE J. Solid-State Circuits, 45(12), 2602–2612, Dec. (2010).
5. Wei H., Chan C., Chio U., Sin S., Martins U., and Maloberti F. An 8-b 400-MS/s 2-b-per-cycle SAR ADC with resistive DAC. IEEE J. Solid-State Circuits, 47(11), 2763–2772, Nov. (2012).
6. Miyahara Y., Sano M., Koyama K., Suzuki T., Hamashita K., and Song B. Adaptive cancellation of gain and nonlinearity errors in pipelined ADCs. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers., 282–283, (2013).
7. X. Jin, Zhibi Liu, and Jun Yang, (2013) “New Flash ADC Scheme With Maximal 13 Bit Variable Resolution and Reduced Clipped Noise for High-Performance Imaging Sensor”, IEEE Sensors Journal, Vol. 13, no.1, pp. 167-171.
8. J. Mukhopadhyay and S. Pandit, (2012) “Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics”, Hindawi Publishing Corporation VLSI Design, Vol.2012, pp.1-13.

9. C. Donovan and M. P. Flynn, “A Digital 6-bit ADC in 0.25-μm CMOS”, IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, March 2002.

10. Yun-Shiang Shu, (2012) “A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators”, IEEE Symp. on VLSI Circuits Design, ISBN: 978-1-4673-0848-9, pp. 26-2

11. A. Z. Jose, P. de Geyvez (2011) “Low-Power High Resolution Analog to Digital Converters, Design Test and Calibration” ISBN 978- 90-481-9724-8, First edition, Springer New York.

12. A. Tangel and K. Choi, “The CMOS Inverter as a Comparator in ADC Design”, Analog Integrated Circuits and Signal Processing, 39, 147-155, 2004.

13. T. B. Cho and P. R. Gray, ‘A 10-bit, 20-MS/s, 35-mW pipeline A/D converter,’ in Proc. IEEE Custom Integrated Circuits Conf., May 1994, pp23.2.1-23.2.4.

14. M. Nachtipal, and N. Ranganathan, Design and Analysis of a Novel Reversible Encoder/Decoder, 11th IEEE International Conference on Nanotechnology Portland Marriott, Portland, Oregon, USA, 2011.

15. R. Baker, Harry W.Li, David E. Boyce, ‘CMOS Circuit Design layout and simulation,’ IEEE Press.

16. P. Quinn, Maxim Pribyko ‘Capacitor Matching Insensitive 12-bit 3.3MS/s Algorithmic ADC in 0.25μm CMOS’.

17. R.V.D Plassche, ‘CMOS Integrated Analog to Digital and digital to Analog converters’, 2nd edition: Kluwer Academic publisher, 2003.

18. Yasser S. Abdalla. “Design of a compact n-bitADC with serial output”, International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, India, Mar., 3-5 2016.

AUTHORS PROFILE

Yasser S. Abdalla, Egyptian, his B.Sc. and M.Sc. from Eng. Fac., Cairo Uni. at 94, and 99. He joined the ECE Dept. at the Uni. of Waterloo in Canada as a Ph.D student in 2002 until 2006. From Jan. 2007 to date, he is a fac. staff at Suez Uni., Egypt. From Oct. 2016 to date he is a faculty member at the CEN department, faculty of com. and inf.sciences, Jouf Uni. From 2007 to 2010 he was the senior consultant for a major project run by (SSRDP) to enlighten Sinai homes by photovoltaic. He authored one international textbook and more than twenty publications. His major research interest is VLSI.