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ABSTRACT

Low-power, nonvolatile transistors are demanded in the digital electronics development. In our work, molybdenum disulfide (MoS$_2$) acts as the channel material integrated with TiN, which is used as a floating gate to build a floating gate transistor. Our transistor exhibits a large hysteresis of 4 V ($V_d = 0.1$ V), high on/off ratio of $10^5$, and symmetry writing and erase voltage. The excellent device characteristics such as nondestructive data readout, low operation voltage, and wide memory window inherent in single-layer MoS$_2$ show their great potential to be applied in nonvolatile memory cells.

Nonvolatile memory cells have potential advantages in secure and fast data storage devices. Energy consumption and floating gate memory miniaturization are demanded to achieve large-scale integration and higher packing density components. Monolayer molybdenum disulfide (MoS$_2$) has many natural advantages such as direct bandgap, a relatively small dielectric constant, and atomic thickness, which help to suppress short channel effect, beneficial for reducing power dissipation. While MoS$_2$ acts as the channel of a memory transistor, its large on/off ratio can differentiate various memory states. Doped hafnium oxide (HfO$_2$) is considered as the promising candidate for Si-based ferroelectric field-effect-transistors (FeFETs) in which some Hf ions were replaced with zirconium atoms. Doped HfO$_2$ films are thin, atomic layer deposition (ALD)-friendly, compatible with the high aspect ratio three-dimensional capacitor structure, and immune to defect generation. The dielectric constant of hafnium zirconium oxide (HZO) is higher than that of HfO$_2$. The higher the gate dielectric constant, the better the gate control ability of the device. Hence, the high dielectric constant of gate dielectric in HZO helps to reduce the operating voltage of the device. In addition, the ALD grown HZO film with the titanium nitride (TiN) electrode was boosted by the asymmetric strain provided by the TiN electrode. In our work, the monolayer MoS$_2$ channel with TiN in the gate is adopted for the fabrication of the floating gate memory-based transistor. A systematic study on the floating gate memory transistor is demonstrated; especially, the interface properties and the capacitance effects are studied.

The process flow schematics for fabricating the device in this work are shown in Fig. 1(a). TiN was grown from Physical Vapor Deposition (PVD) on SiO$_2$/p++ Si substrates. Following the deposition of TiN, HZO was grown using ALD. HZO films were grown in a 1:1 Hf:Zr ratio, and TiN was grown on HZO. TiN was patterned with photolithography and lift off to form a floating gate. Then, 8 nm HfO$_2$ was deposited by ALD. Chemical vapor deposition (CVD) monolayer MoS$_2$ was transferred on HfO$_2$ covered with a sacrificial Al$_2$O$_3$ layer by ALD. Monolayer CVD-grown MoS$_2$ was characterized with the Raman spectrum, and thicknesses were confirmed. Followed by metallization
with 50 nm Ti and 70 nm Au, lift-off was performed in acetone. Finally, the annealing process was performed at 250 °C in the Ar environment for 2 h to improve the contact and remove the photoresist residue on MoS$_2$. The channel length of the fabricated back-gate device is 10 μm, and the width of the device is 380 μm.

The schematic of the floating gate memory-based monolayer MoS$_2$ transistor is shown in Fig. 1(d). The image of the device is shown in Fig. 1(b). A representative microscope image of floating gate memory-based monolayer MoS$_2$ transistors is shown in Fig. 1(c). The Raman spectrum in Fig. 1(e) was obtained on the as-transferred MoS$_2$ film over Si/TiN/HZO/TiN/HfO$_2$ stacks in the...
device. As shown in Fig. 1(c), two bands corresponding to the in-plane $E_{3g}$ mode and the out-of-plane $A_{1g}$ mode were observed at 385.3 cm$^{-1}$ and 404.1 cm$^{-1}$, respectively. The presence of these two high intensity peaks and the difference of about 18.8 cm$^{-1}$ between the two positions signifies the presence of good quality monolayer MoS$_2$.

The band diagrams of the TiN/HZO/TiN/HfO$_2$ structure under a different voltage bias are shown in Figs. 2(a)–2(c). The electron affinity of monolayer MoS$_2$ is about 4.2 eV, while the work function of the TiN trapping layer is 4.3–4.5 eV.$^{19}$ In the equilibrium state (without bias), the carriers in MoS$_2$ and TiN cannot be exchanged with each other due to the blockage from the HfO$_2$ interlayer. When a positive voltage is applied on the gate, the MoS$_2$ channel generates electrons; in the meantime, the potential of electrons in MoS$_2$ becomes higher than the one in the TiN layer. Due to the potential drop in the HfO$_2$ layer, the effective barrier height of HfO$_2$ is lower and the electron in MoS$_2$ has a higher probability to tunnel through the HfO$_2$ barrier, causing an amount of electrons injected into the TiN trapping layer. The trapped electrons in the TiN layer will stay still after the voltage is removed, which modulates the residue carrier density in the MoS$_2$ and leads to the shifting of $V_{th}$ (threshold voltage) to positive voltage. Similarly, when a negative voltage is applied on the gate, the trapped electron in TiN has a higher potential and then tunnels back to the MoS$_2$ channel, as shown in Fig. 2(c).

Figure 2(d) shows the transfer characteristics of the device with different drain voltages (the scan range of $V_D$ is from $-3$ V to $+3$ V). The forward and reverse sweeps demonstrate a large memory window of about 4 V under the different drain voltages. There are no obvious shifts in the transfer curves with different drain voltages, illustrating a stable electrical performance for these floating gate transistors. For nonvolatile memory usage, we define the 3 V at the gate for the “write” voltage and the –3 V for the “erase” voltage. Those operations of gate voltage modulate the channel current for the device after withdrawing the gate bias. The symmetry of voltages for “write” and “erase” helps to reduce the power consumption and is beneficial for circuit design. We believe that the voltage for the trapping and detrapping operation depends on the tunneling barrier of the electron into and out of the trapping layer. The conduction band offset (CBO) between MoS$_2$ and HfO$_2$ is about 1.7 eV$^{15}$ and 1.8–2.1 eV between the TiN trapping layer and HfO$_2$. The TiN interlayer was chosen due to the relatively small difference between the CBO of the MoS$_2$/HfO$_2$ and that of the TiN/HfO$_2$, which is smaller than that of other metals which have been used as the trapping layer.$^{1}$ Therefore, a relatively symmetrical voltage of ±3 V on the gate to transfer the electron between the trapping layer and the channel is realized. At the same time, the on/off ratio is high up to 10$^5$, as shown in Fig. 2(d). All these demonstrate a sufficiently large memory window with strong potential for the data storage applications.

For a control device, we fabricated the HfO$_2$/MoS$_2$ FET without a TiN top layer using the same fabrication process, as shown in Fig. 3(b). Figure 3(b) presents the transfer characteristic of the 10 µm-long HfO$_2$/MoS$_2$ FET without TiN/HZO/TiN. From the transfer curves in Fig. 3(b), we can see that when the gate voltage sweeps at room temperature from negative to positive voltage and then from positive to negative voltage, the hysteresis is about 0.1 V, much smaller than the device with a TiN top layer. Hence, the large hysteresis of about 4 V in the device with a TiN trapping layer is not from the interface traps or dielectric movable ions.

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**FIG. 2.** (a) Simplified band diagram of the floating gate transistor when $V_G = 0$ V. (b) Simplified band diagram of the floating gate transistor in program operation. Application of a positive control gate voltage $V_{BG}$ programs the device. Electrons tunnel from the MoS$_2$ channel through the 8 nm thick HfO$_2$ and accumulate on the TiN floating gate. (c) Simplified band diagram of the floating gate transistor in erase operation. Application of a negative control gate voltage $V_{BG}$ depletes the floating gate and resets the device. (d) A typical transfer characteristic of the MoS$_2$-based transistor with 30 nm TiN floating gate.
Surface roughness and contact between metal and MoS$_2$ are also examined. Figure 3(c) shows the atomic force microscope image of the deposited HfO$_2$. As shown in this figure, the rms is 0.874 nm. It indicated that the HfO$_2$ layer is compact and well uniform, indicating that there is a uniform deposition of HfO$_2$ followed by the monolayer MoS$_2$ as a channel layer. To verify the contact quality of these devices, $I_{DS}$-$V_{DS}$ curves are studied under a small bias ($V_G$ is from −2 V to 2.5 V). Figure 3(a) presents a nearly linear fitting of the curves even under a relatively small drain-source bias. The curve indicates the formation of ohmic contacts between metal and monolayer MoS$_2$. The current of the MoS$_2$/HfO$_2$ FET, at the level of 16 μA for a 2 V bias, shows that efficient charge injection from the metal to MoS$_2$ is possible. In the future, graphene contacts may be a promising solution to improve source/drain contacts with MoS$_2$, and it is expected to obtain higher output current when applying lower voltage.

In general, the charge trapping at the MoS$_2$/HfO$_2$ interface will degrade the “low” state current and subthreshold swing (SS). Therefore, a high quality HfO$_2$/MoS$_2$ interface is demanded. The control device in Fig. 3(b) shows a small hysteresis of about 0.1 V and SS of about 104 mV/decade, which indicates a good interface property in our device. Notably, 10 nm Al$_2$O$_3$ was also deposited on the surface of MoS$_2$ to eliminate surface contaminations. As a passivation layer, Al$_2$O$_3$ can also be beneficial to reduce the interface charge. It is also demonstrated that the on/off ratio increases with the drain voltage. As predicted above, MoS$_2$/HfO$_2$ interface charges have less effect on the memory windows.

These results demonstrate that the window of the memory-based monolayer MoS$_2$ transistor with TiN is mainly caused by the storage capability of the TiN floating gate layer, not by the charge trapping in the interface between HfO$_2$ and MoS$_2$.

In summary, a method to fabricate high-performance monolayer MoS$_2$ transistors with the TiN floating gate is demonstrated. Importantly, the device demonstrates a stable and symmetric hysteresis window of about 4 V and high on/off ratio of $10^5$. The effect of interfacial quality on the electronic behavior and memory characteristics of memory-based monolayer MoS$_2$ transistors are studied. All these excellent device characteristics as well as the easy architecture process indicate the technology potential of the single-layer MoS$_2$ based floating gate transistor for the development of future energy saving memory devices.
See the supplementary material for a summary of the details for liquid-assist transfer of chemical vapor deposition (CVD) synthesized 2D MoS$_2$ and fabrication of a typical 10 μm-long MoS$_2$/HfO$_2$ FET.

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REFERENCES

1. J. Wang, X. Zou, X. Xiao, L. Xu, C. Wang, C. Jiang, J. C. Ho, T. Wang, J. Li, and L. Liao, Small 11, 208 (2015).
2. H. Tian, L. Zhao, X. Wang, Y. W. Yeh, N. Yao, B. P. Rand, and T. L. Ren, ACS Nano 11, 12247 (2017).
3. Q. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, Nat. Nanotechnol. 7, 699 (2012).
4. S. Salahuddin and S. Datta, Nano Lett. 8, 405 (2008).
5. F. A. McGuire, Y. C. Lin, K. M. Price, G. B. Rayner, S. Khandelwal, S. Salahuddin, and A. D. Franklin, Nano Lett. 17, 4801 (2017).
6. H. S. Lee, S.-W. Min, M. K. Park, Y. T. Lee, P. J. Jeon, J. H. Kim, S. Ryu, and S. Im, Small 8, 3111 (2012).
7. A. Lipatov, P. Sharma, A. Gruverman, and A. Sinitskii, ACS Nano 9, 8089 (2015).
8. A. Sharma and K. Roy, IEEE Electron Device Lett. 38, 1165 (2017).
9. M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, K. D. Kim, and C. S. Hwang, Appl. Phys. Lett. 105, 072902 (2014).
10. J. Müller, T. S. Böscke, D. Bräunhaus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Nikolajick, and L. Frey, Appl. Phys. Lett. 99, 112901 (2011).
11. M. H. Lee, Y. T. Wei, K. Y. Chu, J. J. Huang, C. W. Chen, C. C. Cheng, M.-J. Chen, H.-Y. Lee, Y.-S. Chen, L.-H. Lee, and M.-J. Tsai, IEEE Electron Device Lett. 36, 294 (2015).
12. S. Bertolazzi, D. Krasnozhon, and A. Kis, ACS Nano 7, 3246 (2013).
13. K. Choi, P. Lysaght, H. Alishaftee, C. Huffman, H.-C. Wen, R. Harris, H. Luan, P.-Y. Hung, C. Sparks, and M. Cruz, Thin Solid Films 486, 141 (2005).
14. J. Robertson, J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct.–Process., Meas., Phenom. 18, 1785 (2000).