Single Stage Isolated Zeta Converter (SS-Izc) Circuit with Improved Power Factor for LED’s Application

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Abstract. Light emitting diode specifically White LED has gain a lot of attention from both academics and industrial sector due to its high efficiency, environmentally friendly, and long lifecycle. This is a feasible alternative for conventional bulbs and tubes in domestic, industrial and commercial lighting. However, implementation of this new source requires various parametric regulation. This proposed single stage isolated zeta converter (SS-Izc), with power factor correction maintains constant output for the load of 36 Watts LED, and follow the IEC61000-3-2 standard. The proposed SS-Izc is operating in DCM and controlled with PWM (Pulse width modulation), for power factor improvement and low THD, and obtain more than 0.9 power factor and THD less than ten percentages.

Index Terms— single stage Isolated Zeta converter (SS-Izc), power factor (PF), Pulse width modulation (PWM), Universal AC input, discontinuous conduction mode (DCM), total harmonic distortion (THD).

1. Introduction

The large share of electric power is used for lighting purpose. So, reduction in this required energy will also reduce the greenhouse effect. LED has great advantage over the traditional lighting such as more life that is greater than 150000 h, zero ultraviolet emission, durable quality, operated in extremely low temperature and low voltage application, hence LED lighting have been bringing revolution to this world [1].

The fluorescent tubes have the problem of power factor, cost, flicking etc., to overcome this, electromagnetic ballasts are introduced. Further, enhanced is LED’s, to overcome these problems [2-3]. The converters and rectifiers have further improved the operation of LED [4-7]. However, the non-linear elements present in these system, will pollute the power system standards for power factor and total harmonic distortion respectively. To cope up with these standards, LED’s have power factor correction technique, which can be single or two stage [4-7]. In two stage converter, PF correction circuit is separately connected and hence requires more components.
The single stage converter has wider acceptability than the two stage converter, for PF correction in LED’s. in single stage PF correction circuit and converter is combined in one stage and hence components requirement is less as compared to two stage. Six configuration of converters are more prominent than other, Buck, Boost, Cuk, Buk-boost, Sepic [12-17]. The SS-IZC is generally used for high power and more widely accepted than other converters due to its simplicity and isolation of output from input. This isolation provides a projection mechanism against short circuit condition.

In this work, SS-IZC with PF and THD correction is analysed. For controlling of the gate of power switch, PWM controller is employed, which take output as a feedback and maintain the constant output voltage. The design of IZC is analysed for 36 Watts LED with PF and THD circuit. For controlling THD at the input side, a low pass filter is used at the input side. In part II, the operation of SS-IZC with PF circuit is discussed. In part III, proposed designed of SS-IZC is explained. In part IV, control strategy of SS-IZC based DCM is explained and in last section conclusion is made on behalf of simulated results.

2. Analysis of SS-IZC

The SS-IZC provides isolation between the rectifier and LED shown in Fig. 1. The winding polarity is indicated by dot convention. The \( V_d \) , is rectified voltage of input, \( V_{s1} (t) \). The \( L_{m1} \) symbolizes, magnetizing inductance of the SS-IZC. Energy is stored in \( L_{m1} \) when switch, M, is ON and in OFF condition of Switch the stored energy in primary side of transformer is transferred to secondary side. Smooth voltage across the LED is maintain by the output capacitor \( C_{o1} \). A SS-IZC will work in DCM/CCM depends on the continuity of inductor current. Pulsating input current is developed due to high switching frequency of switch, M. To make line current in phase with line voltage current pulsating. Hence low THD and nearly unit factor at input side achieved.

Also, the SS-IZC working in DCM requires less component as compared to the two stage operation, as SS-IZC operated at fixed duty ratio and fixed frequency.

To simplify the investigation of the SS-IZC for LEDs circuit having high PF, the consideration are:
1. Components of SS-IZC are ideal.
2. The source frequency is to be considerably lesser than the switching frequency.
3. The output voltage \( (V_o) \) is constant during one period as the value of output capacitor is very high.

![Fig. 1 Block Diagram of SS-IZC with Controller](image)

Supposing the turn \( (n = \frac{N_2}{N_1}) \) ratio of the SS-IZC is 0.5 , the waveforms of the SS-IZC is shown in Fig. 5 functioning in the DCM . For one cycle, the SS-IZC operation is divided into three parts:
**Mode I (t_0'<t<t_1')**:

For the time \( t_0' \), switch is ON, diode D is turned off in this mode. The corresponding SS-IZC circuit is shown in Fig. 2. Rectified, \( V_d \), voltage is directly applied to the inductor \( L_{m1} \) and hence \( i_{L_{m1}} \) current across this inductor increases linearly. And current \( i_{L_{o1}} \) also increases linearly across the inductor \( L_{o1} \), since voltage across output inductor is positive voltage i.e. \( nV_d + V_{c_{11}} - V_o \) and the corresponding waveform for this mode is shown in Fig. 5.

![Fig. 2 Mode I operation of SS-IZC](image)

**Mode II (t_1'<t<t_2')**:

In this mode, switch M, is turned off and hence D becomes forward biased. The corresponding SS-IZC circuit is shown in Fig. 3. Since reflected voltage across the capacitor \( C_{11} \) i.e. \( -\frac{V_{c_{11}}}{n} \) is negative, due to this current across the inductor \( L_{m1} \), falls linearly which is shown in Fig. 5. Output inductor \( i_{L_{o1}} \) also fall linearly due to negative terminal voltage \(-V_o\) across it. At this mode diode current is \( i_D = i_{c_{11}} + i_{L_{o1}} \).

![Fig. 3 Mode II operation of SS-IZC](image)

**Mode III (t_1'<t<T_S')**:

In this mode of operation switch M, remained turned off and the current across magnetizing inductor, \( L_{m1} \), and output inductor current continue to fall linearly. In this mode diode is turn off due to sudden fall of diode current to zero. So in this mode both switch and diode are turned off, hence SS-IZC is stated to as operating in DCM, which is shown in Fig. 5.

![Fig. 4 Mode III operation of SS-IZC](image)
3. Design of IZC

The SS-IZC PFC converter is designed to operate in DCM, due to this current across inductor \( L_{m1} \) become discontinuous for one cycle. A PFC SS-IZC converter of 36 W (\( P_{\text{max}} \)) is considered for LED driver Circuit. The line voltage, \( V_{s1}(t) \), varies from 85 V to 270 V. The line voltage \( V_{s1}(t) \) is fed to the SS-IZC PFC converter as,

\[
V_{s1}(t) = V_{m1} \sin(\omega_{s1}t)
\]

(1)

Where \( V_{m1} \) is source maximum voltage and \( \omega_{s1} = 2\pi f_{s1} \), \( f_{s1} \) is the source frequency i.e. 50 Hz.

The instantaneous voltage of DBR is given as,

\[
V_i(t) = |V_{m1} \sin(\omega_{s1}t)|
\]

(2)

Here, \( || \) symbolizes the magnitude of Voltage. The \( V_o \) is output voltage of SS-IZC is given as [18],

\[
V_o = \frac{nD'}{(1-D')} V_d
\]

(3)

Where \( D' \) is taken as 0.5 and symbolizes the duty ratio of linear transformer.

The \( D(t) \) is instantaneous value of duty ratio, and depend upon the value of input Voltage \( V_{s1}(t) \) and the output voltage \( V_o \), And it is obtained from (2) and (3) i.e.

\[
D'(t) = \frac{V_o}{(n)V_{s1}(t)+V_o}
\]

(4)

Instantaneous power at the output capacitor, \( P_i \), is considered as linear function of output voltage \( V_o \) and and given as :

\[
P_i = \left( \frac{P_m}{V_{om}} \right) V_o
\]

(5)

Where \( V_{om} \) denotes the maximum output voltage and \( P_m \) is regarded as a rated power of SS-IZC.

The \( L_{mc1} \) denotes the critical value of magnetizing inductance of transformer of high frequency can be obtained as [19],

\[
L_{mc1} = \frac{R_t(1-D'(t))^2}{2D'(t)f_{sw}(N_2/W_1)^2} = \left( \frac{V_o^2}{P_i} \right) \frac{(1-D'(t))^2}{2D'(t)f_{sw}(n)^2}
\]

(6)

Where load resistance is denoted by \( R_t \), switching frequency is denoted by \( f_{sw} \) (taken as 50KHz) and the instantaneous power, \( P_i \), is consider for lowest possible value of line voltage. Using equation (6) as,

\[
L_{mc1} = \left( \frac{V_o^2}{P_m} \right) \frac{(1-D'(t))^2}{2D'(t)f_{sw}(N_2/W_1)^2}
\]

(7)

Where \( D'_{a} \), duty ratio and calculated for maximum output voltage \( V_{om} \) and at minimum peak supply voltage. And for the operation of SS-IZC in DCM mode, the value of transformer magnetizing inductance  \( L_{m1} \) should be less than the critical inductance \( L_{mc1} \) [20]. Zeta converter operating at the DCM conditions and hence the magnetizing inductance is consider as \( 1/10^{th} \) of critical inductance.

The output inductance \( L_o \) is calculated as [19],

\[
L_o = \frac{V_o(1-D'(t))}{f_{sw} \Delta I_o} = \frac{V_o(1-D'(t))}{f_{sw} \eta I_o}
\]

(8)

Hence, output inductance is designed for rated output voltage for a extreme line voltage and lowest value of duty ratio \( D'_{b} \) corresponding to as [19],

\[
L_{o1} = \frac{V_{om}(1-D'_{b})}{f_{sw} \eta I_o}
\]

(9)

Where \( \eta \) denotes the % ripple of output inductor current, consider as 40% of output inductor current.
The intermediate capacitor value is calculated \( C_{11} \) [19] as,

\[
C_{11} = \frac{v_o D_1(t)}{\Delta V_{c11}(t) f_{sw} R_L} = \frac{v_o D_1(t)}{k(\sqrt{2}v_o + V_o) f_{sw}} \left( \frac{P_o}{V_o^2} \right)
\]  \( (10) \)

Where \( k \) is the allowable ripple voltage through intermediate capacitor and consider as 10 % of \( V_{c11} \). Hence, the value of \( C_{11} \) is designed at extreme value of output voltage , maximum power and at minimum duty ratio, which is given as:

\[
C_{o1} = \frac{V_{om} D_b}{k(\sqrt{2}v_o + V_o) f_{sw}} \left( \frac{P_m}{V_o^2} \right)
\]  \( (11) \)

Hence, value of output capacitor \( C_{o1} \) is considered as [19],

\[
C_{o1} = \frac{I_o}{2\omega V_o} \approx \left( \frac{P_i}{V_o} \right) \frac{1}{2\omega(k V_o)}
\]  \( (12) \)

Where \( \Delta V_o \) denotes the permissible ripple in output voltage, \( k \) denotes the % of acceptable output voltage ripple across capacitor and taken as three percentage of \( v_{om} \).
The wickedest situation design occurred at smallest value of output capacitor voltage i.e. \( v_{omin} \) and calculated as,

\[
C_{o1} = \left( \frac{P_{min}}{v_{omin}} \right) \left( \frac{1}{2\omega(nv_{omin})} \right)
\]

(13)

A low pass filter (LC), is designed to avoid the harmonics of higher order at input side. The filter capacitance \( C_{m1} \), which is taken as maximum value is given as [19],

\[
C_{m1} = \frac{f_{pk}}{\omega v_{m}} \tan(\theta) = \left( \frac{f_{m} \sqrt{2} / V_{c}}{\omega L N V_{s}} \right) \tan(\theta)
\]

(14)

Here \( \theta \) is the angle between line current and line voltage and is consider as 1°. The filter inductance value is calculated by taking the line impedance \( L_{s1} \) is three percentage of base impedance. Therefore the additional value of inductance ( \( L_{f1} \) ) is given as,

\[
L_{f1} = L_{req1} + L_{s1} \Rightarrow L_{req1} = L_{f1} - L_{s1}
\]

\[
L_{req1} = \frac{1}{4\pi^{2}f_{c}^{2}C_{f1}} - 0.03 \left( \frac{1}{\omega L} \right) \left( \frac{V_{c}}{P_{o1}} \right)
\]

(15)

Where \( f_{c} \) is the Cut-off frequency and taken as such that \( f_{L} < f_{c} < f_{SW} \). Hence \( f_{c} \) is consider as \( f_{SW}/10 \). Hence by using above expressions the LC filter with capacitance \( C_{f1} \) and inductance \( L_{f1} \) is taken.

4. Control Strategy of SS-IZC

To control the SS-IZC operated in DCM mode, voltage follower configuration is considered. The control method, consists of voltage controller, reference voltage generator, error voltage generator and PWM generator, which are shown in Fig. 6. Reference voltage produced with ‘Reference Voltage generator’ and voltage error generator compares this reference voltage with output DC voltage and generate error voltage ( \( V_{err} \) ) and resulting voltage error is given as,

\[
V_{err}(n) = V_{ref}(n) - V_{o}(n)
\]

(16)

![Fig. 6 Control Strategy of Isolated Zeta Converter in DCM](image)

And the PI output voltage controller, at nth sampling instant is given as,

\[
V_{cc}(n) = V_{cc}(n - 1) + K_{p} \{ V_{err}(n) - V_{err}(n - 1) \}
+ K_{i} V_{err}(n)
\]

(17)

Where, integral gain and proportional gain denoted by \( K_{i} \) and \( K_{p} \). Gate signal for the switch is generated by PWM to reach unity PF and to minimize the THD by comparing the high frequency Saw tooth signal \( m_{e} \) with output of PI controller \( V_{cc} \) given as,

\[
\begin{align*}
\{ & \text{if } m_{e} < V_{cc} \text{ then Switch is 'ON'} \} \\
\{ & \text{if } m_{e} > V_{cc} \text{ then Switch is 'OFF'} \}
\end{align*}
\]

(18)
5. Result And Discussion

The proposed PFC DCM derived isolated Zeta converter based LEDs driver circuit is designed and modelled in the MATLAB/SIMULINK software and established model is shown in Fig.7, where LED is assumed to be a resistor, high frequency under steady state condition. The proposed PFC converter topology has been implemented through average Voltage control scheme with PI (Proportional Integral) controller. The switching frequency is considered as constant at 50 kHz for PWM generation throughout variations of AC source voltage. The calculated values of the SS-IZC components designed from the mentioned equations and are selected to get less THD and nearly unity PF at different line voltages. These value components and other parameters are given in Appendix.

The waveforms of average current and voltage across LEDs, at rated load at various line voltages are shown in fig.8 to Fig.11. The SS-IZC maintaining steady state voltage at the output.

![Fig. 7 MATLAB Model od Proposed PFC Isolated Zeta Converter](image)

![Fig. 8 Average Output Voltage and Current at 90 V Input](image)

![Fig. 9 Average Output Voltage and Current at 140 V Input](image)
Fig. 10 Average Output Voltage and Current at 200 V Input

Fig. 11 Average Output Voltage and Current at 220 V Input

Table 1
Simulation Results of The Isolated Zeta Converter

| $V_i(t)$ (Volts) | $I_i(t)$ (mA) | $V_o$ (Volts) | $I_o$ (A) | Power Factor | % THD |
|------------------|---------------|---------------|-----------|-------------|-------|
| 90               | 450.13        | 60.9          | 0.61      | 0.998       | 5     |
| 120              | 310.54        | 60.4          | 0.62      | 0.995       | 6.2   |
| 170              | 220.81        | 60.2          | 0.62      | 0.994       | 6.58  |
| 210              | 182.23        | 60.1          | 0.63      | 0.985       | 7.01  |
| 270              | 147.52        | 59.8          | 0.65      | 0.953       | 7.54  |

The performance parameter SS-I2C as a voltage regulator and PF to the LEDs load for various line voltages are concluded in Table 1. Hence from above observation it is found the PF is close to unity and THD less than 10%. And DC load parameter are also, in steady condition for different line voltage.

6. Conclusion
Design and simulation of SS-I2C with improved power factor has been presented, and achieved greater than 0.9 power factor for various supply input voltage (80V - 270V). The utilization of LED depends on its effective design of different parameters have to controlled to meet the international standards. In this work, SS-I2C is analysed, the reason for selection of single stage is that, it has less number of components, which will reduce the overall cost of converter and increase the various indices of given parameters. In the analysis EMI filter is connected at the input side to improve the PF and THD. The PI controller is used for controlling the gate pulse of SS-I2C. Hence, this overall
system has achieved 0.97 PF and 7.54% THD at 270 V. This system is tested for various inputs and obtain results are in-line with standard norms.

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