Challenges of Return-Oriented-Programming on the Xtensa Hardware Architecture

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Abstract—This paper shows how the Xtensa architecture can be attacked with Return-Oriented-Programming (ROP). The presented techniques include possibilities for both supported Application Binary Interfaces (ABIs). Especially for the windowed ABI a powerful mechanism is presented that not only allows to jump to gadgets but also to manipulate registers without relying on specific gadgets. This paper purely focuses on how the properties of the architecture itself can be exploited to chain gadgets and not on specific attacks or a gadget catalog.

I. INTRODUCTION

Cadence Tensilica IP includes Tensilica Xtensa extensible processors [1], a broad range of high-performance application-specific DSPs and a comprehensive development toolchain supporting fast and easy hardware and software tradeoff analysis for digital signal processing and embedded control. By the end of 2012, already 2 billion IP cores were shipped by licensees [2], around 800 million cores per year and with an increasing rate.

With Return-Oriented-Programming (ROP), a technique generalized from return-into-libc attacks by [3], an attacker makes use of already existing code snippets that end with a return instruction. These code snippets are called gadgets and can be used as jump targets instead of the shellcode. By chaining multiple gadgets together it is possible to execute arbitrary code. It has been shown that ROP chaining is turing complete for large enough programs [3], [4].

While finding gadgets can be considered similar to other architectures, chaining these gadgets highly depends on the Application Binary Interface (ABI). Making it more difficult, the Xtensa processor can be configured with two different ABIs. This paper will highlight the important parts of both ABIs that make ROP possible. While for both ABIs ROP is possible, there are differences on how to construct the payload and the kind of gadgets that can be used.

The rest of this paper is structured as follows: section II gives an overview of the related work, section III explains the concept of ROP for the x86 architecture, section IV roughly explains some details of the Xtensa needed to understand the attack while sections V and VI focuses on the attacks for the two different ABIs, and section VII concludes this paper.

II. RELATED WORK

Stack buffer overflows have been a known vulnerability for several decades now [5]. They allow an attacker to manipulate program state or inject shellcode. One of the more frequently manipulated values is the return address of a function. It could for example be used to jump into injected shellcode. While first buffer overflow attacks were shown for the x86 architecture, McDonald showed that the same attack was possible on the SPARC architecture [6]. SPARC contains a sliding register window, which made the attack need one more return before it could work. The first return is used to load the manipulated return address from the stack into the %i7 register. The second return will then jump to that manipulated address.

With the broad introduction of W+X protection for processors, shellcode injection was no longer possible. Return-into-libc attacks were a first form of code reuse attacks that targeted libc functions instead of shellcode. This approach was practical since libc was loaded into almost every C written application. Later, ROP was introduced as a generalization of this technique [3] using gadgets instead of libc functions as jump target.

While the attack was introduced for the x86 architecture first, it was adapted for Reduced Instruction Set Computer (RISC) architectures too [7]–[10]. [7] describes the attack for the SPARC architecture by manipulating local and input registers and provides a gadget catalogue. In [8]–[10] the attack was shown for the ARM architecture by using different instructions than return, i.e. pop pc, but with the same result. In [11] a frame pointer that was saved on the stack was manipulated to shift the top of the stack back into the payload. The same approach is used in this paper to chain gadgets and optimize the size of the payload for the windowed ABI.

In 2018 ROP attacks for the Xtensa were already demonstrated [12] but without making use of the full potential of the windowed ABI and concluded that this ABI makes it harder to find gadgets. They recommended Jump-Oriented-Programming (JOP) attacks instead. In contrast, this paper shows more potential for the windowed ABI, at least for register manipulation, making regular ROP attacks possible.
III. RETURN-ORIENTED-PROGRAMMING - THE CLASSICS

The return address of a function is used to remember where the function was called from and to hand the control flow back to that position once the function is done. Because there is an arbitrary number of functions and functions can also be recursive the space for return addresses cannot be calculated statically. Therefore the return address is put on the stack.

On the x86 architecture the call instruction, that is used to call subroutines, automatically pushes the return address to the stack, while the ret instruction, that is used to return from subroutines, pops the return address from the stack. An attacker can, by abusing a stack buffer overflow vulnerability, overwrite the return address on the stack with a new value of his choice. In case of ROP this new value is the address of a gadget. Because this gadget itself also ends with a ret instruction it can jump again to a new location that can be controlled by the attacker. This is working because the ret instruction does two important things: first it takes an address from the top of the stack, and second it increments the stack pointer. Without the second part the stack pointer would not change and another ret instruction would use the same return address, if no other instructions would change the stack pointer. Chaining different gadgets without this mechanism would be a more difficult task.

Because of these properties the assembly of the attackers payload is pretty straightforward. Fig. 1 shows a simple example. First, the buffer must be filled with random bytes up to the point of the first return address on the stack. After that the gadget addresses can simply be put one after another since the ret instruction of the end of every gadget will point the stack pointer to the next injected gadget address.

Of course the payload becomes more complex when other information is integrated into it, e.g. function arguments or values for pop instructions. Due to the similarities of the architectures it is worth to mention the attack of a SPARC machine described in [7] due to the similarities of the architectures. They exploit the window sliding mechanism by overwriting the local and input register values stored on the stack. Because stack pointer and return address are stored in the input registers, both values can be controlled. This paper will describe a similar technique for the Xtensa architecture in more detail.

IV. XTENSA

This section describes the parts of the Xtensa architecture that are relevant for ROP.

Xtensa has a configurable and extensible architecture, designed to be optimized for a specific application. For example it is possible to extend the instruction set with the Tensilica Instruction Extension (TIE) language. In this paper however, only a configuration with the basic instruction set is covered. The basic instruction set consists of 24-bit instructions with 16-bit (.n narrowed) versions for the most common instructions to save code size. Custom instructions could be even longer, up to 128 bits. The different instruction sizes can be intermixed with each other. This allows to find gadgets on other positions than function epilogues, which is especially important for the windowed ABI.

Most important for this paper, the configuration allows to select between two software ABIs, called call0 and windowed. This selection fundamentally changes the way how gadgets must be chained.

Xtensa is a 32 bit architecture with a word width of 4 bytes. All entries in figures of this paper that represent registers or values in the stack are the size of a word. Xtensa provides a set of 16 general registers a0 to a15. a0 is used to store the return address and a1 holds the function’s Stack Pointer (SP).

All the necessary information regarding the Xtensa architecture addressed in this paper can also be found in greater detail in [13].

V. CALL0

A. Architecture

In the call0 ABI, if a function calls a subroutine, the calling conventions demand that a0 must be saved on the stack and restored before the return. This is done during the function’s prologue and epilogue. The frame of a typical non-leaf function is shown in Listing 1. In the prologue, at the beginning of the function, stack space is reserved for the function by decrementing the SP. Then the return address is stored on the stack. The epilogue reverses this operation. Since there are no push or pop instructions in the instruction set, load and store instructions are used. The position of the return address on the stack is referenced with the SP and an offset, in this example 8. This position is not defined and can differ from compiler to compiler and function to function.

Functions itself are called either with the call0 or callx0 instruction. Return is either done by the ret or ret.n instruction.

B. Gadget Chaining Mechanism

The mechanism of a pop from the stack, or a similar operation, explained in section III, must be replicated. The

```c
// prologue
addi a1, a1, -16 // reserve stack space
s32i.n a0, a1, 8 // store return address
// function body
...
// epilogue
l32i.n a0, a1, 8 // load return address
addi a1, a1, 16 // free stack frame
ret.n
```

Listing 1. call0 function frame
first task is to load the return address from the stack. The
second task is to change the position of the stack pointer.
Since both tasks are not done by the ret instruction directly,
other instructions need to do that in every gadget.

For the call0 ABI function epilogues can be used as gadgets.
Since they load the return address back into a register and also
move the SP, they do all what is needed to chain gadgets.
When building the payload for a ROP attack it is important
to know where the addresses of the gadgets must be placed
within the payload. The l32i.n instruction (see Listing 1)
is used to restore the return address to a0. It uses the SP (a1)
plus an offset to address the position on the stack where the
return address was stored. Therefore the current value of a1 (or
at least its change over time) and the offset must be known
to the attacker. a1 is mainly changed in function prologues
and epilogues. Since the prologue decrements a1, which is
the wrong direction if we want to make use of the payload
of the buffer overflow, it should be avoided in gadgets. In the
epilogue, an addi instruction is used to increment a1. All
that needs to be done is to keep track of this increments in all
gadgets to determine the position for the next gadget address
in the payload. Fig. 2 illustrates how this can be done. It shows
a stack that was already overwritten by a buffer overflow. To
make it as easy as possible the two gadgets that are executed
consist only of the epilogue shown in Listing 1. So first a0
is restored by using the position of a1 with an offset of 8.
This is where the address of the first gadgets must be placed.
After that a1 is incremented by 16 and the gadget returns to
the next gadget. This one, again, uses the same offset. Since
a1 changed by 16, we have to place the next gadget address
4 words apart the previous one in the payload.

VI. WINDOWED

A. Sliding window Mechanism

With the windowed ABI a function also has access to
the general registers a0 to a15. However, in this case these
registers are just a register window of a larger physical register
bank with a size of either 32 or 64. How much the window
slides depends on the call instruction that is used. In contrast
to the call0 ABI there are 6 different call instructions that can
be used: calln and callxn where n denotes how many
registers the window slides. For example a call4 instruction
will cause the window to slide down 4 registers. The return
is done by an retw (windowed return) or retw.n, which
slides the window back.

However, the sliding itself is not done by the call(x)n
instruction, but by the entry instruction. The entry
instruction is required to be the first instruction in every function
and replaces the instructions form the call0 prologue. This is
necessary because sliding the window down by i.e. 4 would
cause a0 to a3 (or more) to get out of the current window. Since
the stack pointer rests in a1, it would no longer be possible
to decrement it and reserve space on the stack. First the old
value of a1 is saved, then the window slides and after that
the decremented value is written back into new a1. For the
return address this problem is solved in the way that call(x)n
simply puts the return address into a0, which will be a0 after
the window slide. However, the caller cannot reserve stack
space for the callee. With the windowed ABI there is no need
for an epilogue in every non-leaf function anymore. In the
call0 ABI the standard epilogue only restores a0 and a1 which
is done automatically in the windowed ABI when window
slides back up.

Both, entry and retw, must know which call(x)n
instruction was used to slide the window. This information is
stored in the two most significant bits of the return address by
the call instruction. During the return the retw will substitute
these two bits by the current Program Counter (PC)'s two
most significant bits. Therefore it is not possible to return to
a different 1GB segment in memory with retw.

B. Register spilling

Due to the limited number of physical registers, window
sliding cannot go on indefinitely. When new registers are
needed and no free physical registers are available, a register
overflow exception occurs. This causes the call of an overflow
handler which saves the affected register’s current values
on the stack. Therefore every window register has its predefined
position in the stack where it can be saved to. The area of
the stack frame, reserved for this purpose, is called Window
Save Area. This area is comprised of two parts, the Base Save
Area (BSA) for the registers a0 to a3 with a fixed size of 16
bytes, and the Extra Save Area (ESA) for the registers a4 to
a11. This area can have a size of 0, 16, or 32 bytes.

Fig. 3 shows the reserved positions of some registers for
the functions foo, bar, and baz. It assumes that the function
foo called bar, which in turn called baz. It shows the stack
frame for the function baz (highlighted by the black box). All
functions were called with the call8 instruction. Therefore
the size of the Extra Save Area is 16 bytes, to contain the
registers a4 to a7.

First it must be noted that the BSA for a function is not
located on the functions own stack frame. This is due to the
fact that a1 is used as the stack pointer. Because all stack
interaction is done through the stack pointer it is not possible to save the first 4 registers in a function’s own stack frame. That’s why the BSA of foo is located in bar’s stack frame and bar’s BSA is located in baz’s stack frame. They are stored with a negative offset to the stack pointer. This way it is also possible to backtrace the stack, because the saved stack pointer in a stack frame points to the next stack frame on the stack.

The ESA is located on a function’s own stack frame on its highest addresses. However, because the size of a stack frame is variable for each function (indicated by the . . .) and these registers are stored at the beginning of the stack frame, a function’s stack pointer cannot be used to address these positions with a fixed offset. But they have a fixed offset to the previous function’s stack pointer. This is why bar’s stack pointer is used to restore baz’s registers a4 to a7. This would be the same for the variable window variant and a call12, with the exception that the registers a4 to a11 would be saved at the beginning of the stack frame. It should be noted that in this case the registers a4 to a7 have a different offset to the stack pointer because they got displaced by the registers a8 to a11. This fact is important when building the payload for the attack.

C. Gadget Chaining Mechanism

Since the function epilogue is mostly replaced by the sliding window mechanism, the method described earlier for the call0 ABI is no longer working. However, the mechanics of the retw instruction itself can be exploited. When registers have been spilled to the stack and have to be reloaded on return, the underflow exception handler can be used to load manipulated register values back into the current register window. With that both essential registers for return address (a0) and stack pointer (a1) can be manipulated by the attacker. There are 3 different handlers, one for each possible window slide. They restore 4, 8, or 12 registers. Because the decision which handler is called is based on the two most significant bits in the return address, it is possible for the attacker to select how many registers should be loaded from the stack back to the register bank. Therefore the values of a0 to a11 can be controlled directly just by using the retw instruction without the need of any actual gadget. The remaining registers a12 to a15 can be controlled too, because of the slide mechanism. It just takes more then one gadget to control them. One gadget that loads the registers a8 to a11 and the second which just slides the register window by 4, or similar constellations.

The underflow exception handlers restore the registers by making use of the fact that the stack can be backtraced to restore the registers a4 to a11. Therefore this property must be reconstructed in the payload that is injected by an attacker. For this, a linked list structure for the payload is introduced. It is a fitting data structure because the saved stack pointer that points to the next stack frame behaves similar to a next pointer of a list element. Fig. 4 shows the beginning of such a list with 3 list elements. The structure of a list element is defined by the stack structure that was introduced in the previous subsection, because all the offsets to the stack pointers must be kept identical. Each list element mimics a BSA on the stack. A potential ESA is indicated by the dotted parts. This is increasing the size of a list element. An underflow exception that is raised within retw, will use this injected BSA (and ESA) to restore the registers and with that load the next gadget address (marked as @Gi for gadget i). Each register has a gadget as subscript to indicate what gadget is being executed when the register value is loaded. The difference of the placement of gadget addresses and its register values that can be observed is caused by the fact that it takes two returns to execute a gadget. The first return will just load the gadget address into the register a0 while the second return will jump to that gadget address. At the same time the underflow exception of the second return will also load the next gadget address and other registers that the first gadget can use. This is why the register values for the first gadget must be placed in the second list element. The registers a4 to a11 are placed in a different list element from the first 4 registers because they are part of the ESA, which is part of a different stack frame from the corresponding BSA. While a0 to a3 are always restored, the other registers are only loaded if the WindowUnderflow8 or WindowUnderflow12 handlers are used. Also, the positions of the register a4 to a7 differs between these two handlers and must be taken into account.

Packing the payload is also a bit different from other architectures. The most important part is the placement of
the first list element because this must align with the SP of a function which returns with an underflow exception. The rest of the list elements can be placed at will. They can even overlap each other as long as the overlapping values are either the same or do not matter for the affected gadgets. But the biggest advantage is that the beginning of the payload, which normally contains junk bytes to fill the buffer, can be used to store list elements. This way attacks with just a handful of gadgets can fit almost entirely inside the buffer, resulting in very small payloads, assuming a reasonable sized buffer. A minimalistic example that does not care about any registers, but a0 and a1, is shown in Fig. 5. While the first gadget address and the first next pointer must be placed further down the stack, the rest of the chaining is done in the original buffer. gadget addresses and next pointers simply alternate, with the next pointer being incremented by two words each time.

D. Differences to the SPARC architecture

The described attack and the attack on the SPARC described in [7] share a lot of similarities. In both cases the restore mechanism of the sliding register window is attacked. But differences occur in details. The biggest advantage of the Xtensa architecture is its flexibility, which unfortunately can be used by the attacker. While on the SPARC the register window always shifts by 16 registers, allowing 8 register values to be handed over to the next gadget, Xtensa allows shifts by 4, 8, or 12 registers. Since the attacker is able to control the window shift it is easier for him to pass values between gadgets and keep them in the register window for a longer time when using a window shift of 4. A drawback from the attacker’s point of view is that the assembly of the attack becomes more complicated because the window shift is an additional variable that needs to be taken into account. However, [7] solved this problem of not being able to passing values between many gadgets by storing all variables in memory. Of course this technique is also applicable for Xtensa.

VII. CONCLUSION

In this paper we showed how the Xtensa architecture can be attacked with ROP no matter what ABI is used in the configuration. We proposed a method for the windowed ABI that allows arbitrary register manipulation combined with an efficient packing of the payload. This makes regular ROP attacks possible for the windowed ABI. This potential can be used additionally to the instructions of the gadget and needs more research to be fully explored, for example if and how an integration in existing ROP compilers is possible.

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