Research on key technologies of high voltage and large capacity static synchronous series compensator control system

Peie Yuan¹, Xiang Wang¹, Guofu Chen¹, Xiaoguang Jia¹, Fengjiao Dai¹, Zhiyong Yu¹ and Yingpei Wang¹

¹ State Key Laboratory of Advanced Power Transmission Technology, Global Energy Interconnection Research Institute Beijing, China
E-mail: haixia28@sina.com

Abstract. With the rapid development of economy, the structure of power grid is becoming more and more complex, which has brought about uneven distribution of power flow, limited transmission capacity and the decline of power quality. The application of new static synchronous series compensator can quickly and effectively regulate power flow, suppress sub-synchronous oscillation and enhance system stability on the basis of guaranteeing transmission capacity. In practical engineering application, the design of control system and the realization of control algorithm are very important. In this paper, the control system of 220 kV 30MW self-excited SSSC device is developed based on the control and protection platform of serial RapidIO technology. Firstly, the main topology structure of SSSC is introduced, and the two-stage DC voltage stabilization and upper steady-state operation control strategy of SSSC using fast response control method which simultaneously regulates modulation ratio and trigger angle are expounded. Secondly, the dual redundancy control system architecture is designed, and the control system implementation scheme is designed. Finally, the RTDS power in the loop experimental system is designed, and the control algorithm is verified by RTDS experiments. The experimental results show that the control strategy and control system implementation scheme adopted in this paper can realize smooth start-up and exit of SSSC device and flexible regulation of power flow. The developed control system can satisfy the long-term reliable and stable operation of the system, especially the design of redundancy mechanism, and increase the reliability of the device operation. Follow-up static synchronous series compensator project and even FACTS project provide reference.

1. Introduction
With the rapid development of economy and the scale of new energy added, the structure of power grid is becoming more and more complex, which brings about problems such as uneven distribution of power flow, limited transmission capacity and decline of power quality. The application of a new type of Static Synchronous Series Compensator (SSSC) can quickly and effectively regulate power flow, suppress sub-synchronous oscillation and enhance system stability on the basis of guaranteeing transmission capacity. It has the advantages of flexible control and simple structure, and has been applied more and more widely [1, 2].

In recent years, scholars at home and abroad have made fruitful achievements in SSSC research [3-6]. In literature [7], a stable start-up strategy is proposed in UPFC project. The start-up of the series part depends on the parallel external devices to increase the start-up time. The paper [8, 9] considers that the unbalanced power exchange on the DC side is the fundamental cause of the unbalanced voltage, and gives the corresponding DC side capacitor voltage balance method for trapezoidal wave modulation. In reference [10], the unbalanced state of chain reactive power compensator is studied,
and the idea of decoupling control is put forward. It can be used for reference in SSC, especially the decoupling control between upper and lower control. Reference [11] introduces the quasi-steady state model of SSSC in H-bridge cascade structure. The impedance compensation domain is analyzed by constant impedance control, but the control mode is too single. Literature [12] compares three kinds of control ideas considering the unbalanced capacitor voltage of H-SSSC, and proposes a comprehensive control strategy which can adjust the modulation ratio and trigger angle simultaneously with rapidity. However, most of these studies remain at the theoretical level, and lack of engineering application practice. Controller design for SSSC is rarely mentioned. Therefore, the high performance SSSC control system and its control strategy for engineering need to be further studied.

Referring to the above research results, the control system of 220 kV 30MW self-excited SSSC device is developed by using the control and protection platform based on serial RapidIO technology. Firstly, the main topology of SSSC is introduced, and the upper steady-state operation control strategy of two-stage DC voltage stabilization and constant active power operation control for SSSC is proposed. Secondly, based on the control and protection platform of serial RapidIO technology, a dual redundancy architecture control system and its engineering implementation scheme are designed. Finally, the RTDS power in the loop experiment system is designed, and the control algorithm is verified by the RTDS experiment, which proves the accuracy of the control strategy and the stability and reliability of the control system.

2. Principle and topology
SSSC is a series compensator based on synchronous voltage source. It provides a voltage which is 90° different from the line current and independent of the line current. It is equivalent to connecting a reactance in series on the transmission line. Therefore, by controlling the voltage amplitude of the SSSC device injection system, the equivalent impedance of the SSSC is controlled, so that the effective impedance of the transmission line can be changed, and finally the purpose of regulating the power flow is achieved. At this kind of circumstance, SSSC and power network exchange only reactive power.

According to the research of SSSC’s main topology from domestic and foreign scholars, when the system is unbalanced, three single-phase H-bridges have the advantage of single-phase voltage and current control being more flexible than three-phase bridges, so the SSSC selects the three-phase H-bridge cascaded main topology in this project. AS show in figure 1, it consists of controller(KZ), series value(HB), DC capacitor(C), filter(L), bypass thyristor(TBS), coupling transformer(T), circuit breaker1(QF1), circuit breaker2(QF2), circuit breaker3(QF31). Because the coupling transformer is connected in series on the Transmission Line, the series value is also effectively connected in series to the transmission line, and series compensation can be realized. The main function of bypass thyristor is: when the series valve is exited, the controller simultaneously issues a command to close the bypass switch and contact the bypass thyristor. Since the bypass thyristor is touched quickly, the series valve can be bypassed very quickly, and after the bypass switch is closed. The circuit breaker is mainly used for the switching of the SSSC. When the SSSC is working normally, the AC breaker QF1 is disconnected, the valve outlet side breaker QF2 is closed, and when the system is faulty, the SSSC is removed from the grid. Each phase converter valve is cascaded by 9 H-bridge modules.
3. Research on control technology

3.1. Control strategy research

3.1.1. Startup strategy

Controlling the phase of the output voltage of the inverters is the same as the phase of the injected current, which can ensure that the inverters are pure resistance in the process of charging from the external system, so it does not consume reactive power and has the highest charging efficiency. This way can also be called the "resistance" mode of SSSC, that is, the full active PWM rectification mode. The expression of equivalent resistance of full active PWM rectifier charging output is as follows:

\[ R = \frac{U(t)}{I(t)} = \frac{mV_{dc}}{I_p} \]  \hspace{1cm} (1)

Among them, R is the injection equivalent resistance, m is the modulation ratio, U (t) is the output voltage of the inverter, I (t) is the injection system current, and V_{dc} is the DC bus voltage.

It is assumed that the injection equivalent resistance is small and the line current remains unchanged during the charging process. In the process of charging, the DC voltage increases continuously until the set value, so the modulation ratio m is inversely proportional to the DC voltage in the control. Through the detection link, the modulation ratio can be calculated by formula (1). At the initial stage of charging, the parallel diode in H bridge is used to pre-charge the DC capacitor, and then the PWM rectifier is carried out.

3.1.2. Steady-state control

Combined with H-SSSC steady-state model, when the total conversion ratio of coupling transformer is 1, Then the DC capacitance equation of series compensation line:

\[ C \frac{dU_{ci}(t)}{dt} = S_{so}(t) \sin(\omega t + \varphi) \]  \hspace{1cm} (2)

Where, C is the DC side capacitance value. U_{ci} is the capacitance voltage of the ith module, and \varphi is the angle between line current and compensation voltage. S_{so} is defined as a switching function.

\[ S_{so}(t) = m_i \sin \omega t \]  \hspace{1cm} (3)

Where, \( m_i \) is the modulation ratio. Then the DC side capacitance voltage can be obtained.

\[ V_{ci}(t) = \frac{I_i m_i}{4C_{so}} [2\omega t \cos \varphi + \sin \varphi - \sin(2\omega t + \varphi)] + V_{ci}(0) \]  \hspace{1cm} (4)
\( I_L \) corresponds to the current RMS of AC line at this time, It is known that its DC component \( V_{dc} \) is:

\[
V_{dc} = \frac{I_L m_i}{4C_{dc}} [2 \cos \phi + \sin \phi] + V_{ci}(0)
\]

(5)

And the line current:

\[
I_L = \frac{|U_1 - U_2|}{X_L - X_{ref}} = \sqrt{\frac{U_1^2 + U_2^2 - 2U_1U_2 \cos \delta}{X_L - X_{ref}}}
\]

(6)

Where, \( U_1 \) and \( U_2 \) are voltage values on both sides of AC line respectively. \( X_L \) is the Line impedance, \( X_{ref} \) is the reference value of line impedance.

It can be seen that the DC side capacitance voltage is positively correlated with the angle \( \phi \) and modulation ratio \( m \) when the line current and capacitance value are constant. The DC side capacitance voltage can be controlled by controlling the angle \( \phi \). At this time, the compensation voltage is not strictly vertical to the line current. Instead, there is a difference in angle \( \delta_1 \):

\[
\delta_1 = k_p \left( NU_{cref} - \sum_{i=1}^{N} U_{ci} \right) + k_i \int \left( NU_{cref} - \sum_{i=1}^{N} U_{ci} \right) dt
\]

(7)

Where: \( \delta_1 \) is the regulation angle during SSSC startup or operation, \( K_p \) and \( k_i \) are PI control loop parameters, \( N \) is the number of submodules, \( U_{cref} \) is the capacitor voltage reference value.

### 3.1.3. Voltage equalization control

Two-stage DC voltage stabilization is to realize DC capacitor voltage balance control by upper and lower layer hierarchical control. The control strategy of calculating modulation ratio \( m \) and phase angle \( \alpha \) is defined as upper control, and the control strategy of calculating modulation ratio \( m_i \) and phase angle \( \alpha_i \) by balancing control algorithm is called lower control. If there is no balance control algorithm, all cascade modules use \( m \) and \( \alpha \) directly, and each module after adding balance control algorithm uses their respective \( m_i \) and \( \alpha_i \).

The purpose of second order dc stable voltage is to obtain modulation ratio and firing angle each sub-module. the correction formula of the secondary voltage regulation:

\[
\begin{align*}
\delta_i &= m_i \sqrt{1 + \left( \frac{U_{ci} - U_{cref}}{U_{ci}} \right)^2} \\
\alpha_i &= \alpha + \arctan \left( \frac{U_{ci} - U_{cref}}{U_{cref}} \right)
\end{align*}
\]

(8)

Where, \( m_i \) is the modulation ratio of \( i \)th sub-module, \( \alpha_i \) is the firing angle of \( i \)th sub-module, \( m \) is the modulation ratio of whole series value, \( \alpha \) is the firing angle of whole series value.

It can be seen that by combining the direct PI control of the DC-side capacitor voltage with the separate adjustment of the modulated waves of each module, the H-bridge SSSC responds faster according to the fast response control method. Combined with the constant active power control method, the overall control block diagram is shown in Figure 2.
Figure 2. The general block diagram of control.

Figure 2 shows the instantaneous active power calculated by collecting the voltage and current values of the line, and the instantaneous active power is compared with the reference power value $P_{\text{ref}}$, and the reference modulation ratio $m$ is generated by PI control. The difference between the total capacitance of the module and the reference value of the capacitor voltage is obtained by the PI link to obtain the first-order DC voltage regulation angle $\beta$. At this time, the overall energy of the H-bridge cascade is balanced, thereby avoiding the overall overcharge. The two-stage voltage regulation finally obtains the modulation ratio $m_i$ and the firing angle $\alpha_i$ of each sub-module, ensuring that a single sub-module does not overcharge and achieve voltage equalization. Then the CPS-SPWM modulation strategy is applied to obtain the trigger pulse of each module of the H-bridge level, and the IGBT is controlled to be turned on and off, and the corresponding output voltage is compensated.

3.2. Dual redundant control system architecture

The figure 3 show the control system structure of SSSC. The control system adopts the way of separate configuration, with high-speed fiber-optic communication between the two to exchange information. In order to improving the reliability of control system, each set of control is equipped with a separate acquisition chassis, and the control system has adopted two sets of redundant configuration, control (A) and control (B) is master-slave redundant configuration, namely only the master control system is in working statement at any time, the slave control system is in stand-by statement. Once the main control system fails, the "master-slave" switching is immediately performed: "master" change to "slave", "slave" change to "master". In the time of "master-slave" switching does not affect the normal operation of the converter.

3.3. Control system design

Based on the H-bridge cascade topology, SSSC adopts two-stage DC voltage regulator three-stage hierarchical control strategy. The SSSC control system is divided into three levels: system level, device level and valve level. The three layers of control are coordinated to achieve specific compensation effects. The control arithmetic in SSSC project is realized as follows: system level control and device level control are implemented in the DSP TMS320C665x of the core CPU board in the control chassis. The valve level control is realized by the DSP TMS320C665x and FPGA in the core CPU board of the valve control VCU chassis. As shown in Figure 4.
In order to ensure the reliable operation of the control system and the implementation of the algorithm, the phase-to-phase voltage equalization algorithm is implemented in the main control program, and the sub-module voltage equalization algorithm is implemented in the valve control program.

The SSSC device receives control commands and scheduling commands from the remote dispatch center through the monitoring background and communication channel of the Shigezhuang substation. The monitoring background is connected to the system level through fiber optics, using the 61850 communication protocol. System-level control mainly includes equipment start-stop control, operation mode selection, two-wire power flow calculation, and power flow optimization distribution and other functions. According to the requirement of adjusting power flow or damping the subsynchronous oscillation, the power flow control target is proposed for the device, and the system level control obtains the final active power command Pref according to the control target, thereby realizing the optimal operation of the distribution network. Pref is the active command of the device level controller, and this active command cannot exceed the power limit of the line.

The device level control receives the system level control command Pref, completes the constant DC voltage control and the fixed active power control, respectively control the DC capacitor voltage and the output active power. At the same time, it completes the first-level DC voltage stabilization algorithm. The device-level control also carries out on-line fault monitoring.

The device level and valve level are connected by optical fiber and communicated by IEC60044-8 protocol. Valve level control mainly achieves three functions, one is sub-module voltage equalization control, the other is sub-module redundancy switching, and the third is CPS-SPWM modulation.

The final modulation wave of each sub-module is the result of three-phase addition of device-level algorithm, phase-to-phase voltage equalization algorithm and sub-module voltage equalization algorithm. Then, according to the CPS-SPWM modulation method, the trigger pulse of each sub-module is generated and sent to the sub-module of the valve.
4. Control system function test

4.1. The design of RTDS system

In this paper, RTDS real-time digital simulation system and SSSC control equipment are used to form a closed-loop simulation system. RTDS real-time simulation system used to simulate the primary equipment, such as AC Equivalent system, transformer, converter value, switch etc, the parameters are shown in Table 1 and Table 2. The SSSC’s control system, which was tested, consists of control A, control B, value-controlled VBC, value-based electronics (VBE), background program of monitoring. SSSC’s control system connect with digital real-time simulation system by the screen of interfaces(DIDO signal, analog and cables), and form a close-loop test system.

| Reference name     | unit | value |
|--------------------|------|-------|
| capacity           | MVA  | 30    |
| ratio              |      | 10.2/22.7 |
| Uk%                | %    | 15    |

Table 1. The main parameters of Series transformer

| Reference name     | unit | value |
|--------------------|------|-------|
| Rated current      | A    | 760   |
| Rated voltage      | k (phase) | 11.4 |
| Module number      |      | 9     |

Table 2. The main parameters of H-bridge

The SSSC control system adopts a self-developed new platform. The core CPU board adopts the DSP + FPGA dual-chip architecture. The DSP adopts the TMS320C665x series chip, which is based on TI's KeyStone multi-core architecture, which can run at a core speed of up to 1.25 GHz. The FPGA uses the XILINX Kintex-7 series chip.

The connection between DSP and FPGA use the method, which is a data interaction between a multichannel low-speed port and a single-channel high-speed port, figure 5 show that, this realize the data interaction between several low-speed channels and a single high-speed channel, among them high-speed serial port is used SRIO protocol, low-speed channel consist of serial port, the difference interface in backboard, light port for input and output.

![Diagram](image)

Figure 5. data interaction between multichannel low-speed port and single-channel high-speed port.

The FPGA chip is used to realize the link of data communication in bottom board, including multi-channel data acquisition and transmission, the fusion of the low-speed channels to the single-channel high-speed transmission, and the single-channel data classification and analysis to the different channels. The DSP chip is used to realize data processing and control algorithm on board, by high-speed serial port from FPGA obtain necessary data, complete data analysis and calculation in
real-time, then send the calculation result to the FPGA by high-speed serial port, realize the Real-time
communication with monitoring background and VBC.
By adopting advanced chips and efficient communication methods, the new platform can shorten the
control cycle and reduce the delay in communication. The multi-channel to single-channel design is
more compatible and portable, and can be reused and reduced the internal complex logic timing
control, and increases system reliability. It provide the support in hardware for successful development
of SSSC.

4.2. Self-excited starting test
Based on the two-stage DC voltage regulation strategy, a self-excited startup scheme suitable for
SSSC devices is designed.
(1) Check if the system has access conditions for SSSC. That is, the line current is in a normal state
and is greater than the starting value, and each device can operate normally.
(2) When the condition (1) is satisfied, close SSSC’s the valve outlet side breaker QF2 and cut off the
AC breaker QF1. At this time, the converter valve is in the locked state. At this time, the converter
valve is in the locked state. Because there is a difference between the power supply amplitude and the
phase angle at both ends of the SSSC device, the current flows through the parallel thyristor in both
side of sub-module, converter value controller obtain the power by current CT.
(3) After the converter valve controller obtain the power successfully and stabilizes, the valve control
returns the “control device allows input” to the main control, then the main controller unlocks the
inverter and enters the zero voltage state, which is control upper bridge arm connecting and under
bridge arm disconnecting, the DC side capacitor voltage is stabilized at a small voltage value, and the
SSSC outlet voltage is a voltage drop of the transformer leakage reactance.
(4) Dc voltage operating, the DC side capacitor voltage is charged following the control curve until the
capacitor voltage reach the rated reference value. In this process, when DC voltage reaches 600V,
converter value is switched from CT to dc voltage.
(5) Power flow control operating, SSSC’s operating module work in regulation statement.
(6) SSSC power flow control input, select SSSC operation mode to enter regulation operation.
The figure 6 show the wave of starting process:

Figure 6. The wave of starting process.

(a)the wave of dc voltage       (b)the wave of current in bridge arm, line voltage and current

Figure (a) is the wave of dc voltage of each sub-module, after equipment is started, the capacitor is
charged according to the slope set in the program. Figure (b) is the waveform of the bridge arm current
and line voltage and current. The experimental results show that during the startup process, the
capacitance voltage of each sub-module rises to the rated 2.5kV with a set slope, and the bridge arm current and line voltage and current have no impact. After reaching stability, the capacitor voltage of each module fluctuates around 2.5kV, and the fluctuation range does not exceed 0.1kV.

4.3. Capacitor voltage equalization algorithms test
In order to verify the correctness of the capacitor voltage equalization algorithm, the RTDS model parameters are modified. According to the technical parameters of capacitors, the capacitance error does not exceed 5%. The capacitance of the first four modules of phase A is set to 4200uF, the capacitance value of phase B is set to 4000uF, and that of the last four modules of phase C is set to 3800uF. The experimental waveform of capacitor voltage equalization is shown in Figure 7.

The experimental results show that when there are differences in capacitance both phases-to-phases and each sub-module, the maximum difference of capacitance voltage between each sub-module is 0.1% in steady state, and the three-phase voltage of the network side of series transformer maintains balance, which meets the design requirements. The correctness and validity of the capacitor voltage equalization algorithm are verified.

4.4. Dynamic performance test
Figure 8 is the waveform of power step test. In the experiment, the active power instruction of the line
jumps from 170 MW to 270 MW, and the change rate of the power instruction is 1 p.u. / 1 point.

(a) the waveform of DC voltage

(b) Waveform of Active and Reactive Power Flow

(c) the waveform of transformer network side voltage

Figure 8. Power step (170-270MW) simulation waveform.

Dynamic experimental results show that in the process of the power step, the active power of the line is stabilized in the power flow instruction, the capacitor voltage of the sub-module is stabilized in the rated voltage, the bridge arm current, system current and voltage have no impact, and the system runs normally. It proves that the fast response control method has good instantaneous characteristics and can satisfy the fast and stable response characteristics of H-bridge cascade SSSC as reactive power compensation device to power flow regulation, thus verifying the correctness of the control system and its algorithm.

5. Conclusion

(1) The self-developed control platform uses advanced chips and efficient communication mode, which improves the calculation speed, shortens the control cycle, reduces the communication delay, and can meet the long-term reliable and stable operation of the system. It provides hardware support for the successful development of the SSSC control system.

(2) The dual redundancy mechanism SSSC control system developed in this paper increases the reliability of the device. The application of two-stage DC voltage stabilization algorithm and fast
response control method can realize smooth start-up and exit of SSSC device, and adjust the power flow flexibly in real time according to the demand of power flow adjustment or damping of sub-synchronous oscillation. The practicability and reliability of the designed SSSC control system are further verified.

In a word, the development of Tianjin SSSC control system and the successful operation of the device can provide reference for the follow-up project of static synchronous series compensator and even FACTS project in China.

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### 6. References

[1] ZHOU Junyu. Review of the applications of static synchronous series compensator in powersystem[J]. *Electrotechnical Application*, 2006, 25 (4):51-54,118(in Chinese).

[2] HE Da-yu. FACTS technology and new progress in the development of its controllers[J]. *Automation of Electric Power Systems*, 1997, 21(2): 1-6.

[3] Javeed Kittur, Saikumar H. Y, Sharath Raj S. Y. Comparative analysis of robust PSS and robust supplementary modulation controller for SSSC [J]. *Biennial International Conference on PESTSE*, 2016, 16(8):4673-6658.

[4] F. J. Chivite-Zabalza, P. Izurza, G. Calvo, M. A. Rodriguez. Modelling and control of a Series Static Synchronous Compensator using low-frequency, fixed-modulation index techniques [J]. *IEEE Power Electronics, Machines and Drives*, 2014, 17(2):1-6.

[5] Wei Wenhui, Song Qiang, Teng Letian, et al. Research on anti-fault dynamic control of static synchronous compensator using cascade multilevel inverters[J]. *Proceedings of the CSEE*, 2005, 25(4):19-24(in Chinese).

[6] Zhao Jianjun, Guo Jianbo, Zhou Xiaoxin. The steady state performance analysis and mathematical model of static synchronous series compensator[J]. *Electric Powe*, 2005, 38 (10):11-14.

[7] Han, B., Baek, S., Kim, H., Karady, G. Dynamic characteristic analysis of SSSC based on multibridge inverter. *IEEE Transactions on Power Delivery*, 2002, 17(2):623-629.

[8] Yusuake Fukuta, Giri venkatataraman. DC bus ripple minimization in cascaded H-bridge multilevel converters under staircase modulation. *37th IAS Annual Meeting*, 2002, 3:1988-1993.

[9] Fang Zheng Peng, McKeever J. w., Adms D. J. A power line conditioner using cascade multilevel inverters for distribution systems. *IEEE Transactions on Industry Applications*, 1998, 34(6):1293-1298.

[10] Y. Wang, Y. Chai, J. Tang, X. Yuan and C. Xia,” DC voltage control strategy of chain star STATCOM with second — order harmonic suppression,” in *IET Power Electronics*, 2016, 14(9):2645-2653.

[11] ZHAO Yang. Study on static synchronous series compensator control strategy and subsynchronous resonance mitigation[ D]. *Beijing, China: North China Electric Power University*, 2009.

[12] LU Zhengang, SONG Jieying, SONG Fangfang, et al. Main parameter design and control technology of cascaded H-bridge SSSC[J]. *Smart Grid*, 2017, 5(6):536-543.