Design and Implementation of Carrier Detection System Based on FPGA

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Abstract. In order to better monitor and manage the signal transmission in the communication system and base station, and carrier detection is more effective. This paper designs a carrier(Carrier frequency) detection system based on FPGA, including system design requirements, FPGA selection, system framework design, carrier detection method design and so on. The performance indexes of the system are tested, such as carrier frequency range, carrier search time, carrier detection number and CPU consumption rate. The system has the advantages of high flexibility and good portability, and has a good application prospect in communication system, base station and other equipment.

Keywords: Communication system; Carrier; FPGA; Frequency range; Search time.

1. Introduction

In recent years, with the rapid development of computer and communication technology, especially the emergence of big data, the Internet of things, cloud computing, artificial intelligence, etc., the rapid transmission of huge information and data volume has become an urgent demand[1,2]. According to the 44th statistical report on the development of Internet Network in China issued by China Internet Information Center in August 2019, by the end of June of that year, the number of Chinese Internet users reached 854 million, the Internet penetration rate reached 61.2%, and the consumption of mobile Internet access traffic reached 55.39 billion GB, an increase of 107.3% year on year[3]. To effectively solve the demand of fast data transmission, we need to constantly improve the speed of network communication, which promotes the rapid development of 4G and 5G communication technology. Therefore, countries have set up 5G technology research departments to promote the development of the fifth generation wireless communication system (5G)[4,5].

In the research of 5G communication system, multicarrier transmission technology is the core to realize 5G, and multicarrier transmission technology is also the key to the future communication physical layer. In the current 4G communication system, orthogonal frequency division multiplexing (OFDM) is mainly used as the transmission technology. Orthogonal frequency division multiplexing (OFDM) is a branch of multicarrier transmission technology[6,7,8]. Compared with 4G, the 5G communication system improves the spectrum utilization, transmission rate, delay and so on. Moreover, it can dynamically configure the corresponding multicarrier transmission parameters according to the business scenarios. Therefore, it is important to study the multicarrier transmission technology to adapt to the development of 5G[9,10].
In order to better monitor and manage the signal transmission in the communication system and base station, the fast and effective detection of carrier becomes a key point. Therefore, a carrier detection system based on FPGA is designed in this paper, which can be used for carrier detection and control of communication system, base and other equipment. The performance indexes of the system are measured, such as carrier frequency range, carrier search time, carrier detection number and system consumption rate.

2. Carrier

First, let's understand what is carrier wave? Although the concept of carrier is similar to carrier frequency, carrier is not a physical concept but a logical concept. A carrier is a frequency point that carries the service, that is, single carrier is a frequency point, double carrier is two frequency points, and so on, and multi carrier is multiple frequency points[11,12,13]. Because of the limited energy, the baseband signal can't be transmitted over long distance or over the air. Therefore, it is necessary to modulate to the carrier for transmission. It's like it's hard to transport the container to a distant place by manpower, but we can put the container on the car and carry it to a distant place. Let's use this example to explain the relationship between carrier and signal, so that we can better understand carrier.

1. Goods are signals.
2. Car is carrier. It's a series of continuous sine waves.
3. Modulation is the form of loading the signal to be sent into the carrier wave and sending it to the destination.

The schematic diagram of carrier wave and signal is shown in Figure 1

![Carrier and signal diagram](image)

Figure 1. Carrier and signal diagram

Multicarrier can overcome frequency selective fading, because its signal bandwidth is smaller than the correlation bandwidth. Although it will have flat fading, this attenuation will not cause signal distortion, but will only lead to signal energy reduction. In the case of single carrier, the method based on cyclic prefix needs a long length, so single carrier generally does not use cyclic prefix method, but uses time-domain equalization at the receiver, but the complexity of time-domain equalizer limits the information rate can not be too high. In order to transmit higher information rate, orthogonal frequency division multiplexing (OFDM) technology is gradually used instead of single carrier.

2.1. System Design Requirements

In order to better realize the signal transmission of communication system, base station and other equipment, this paper designs a carrier detection system based on FPGA. The carrier detection system shall at least meet the following requirements.

1. Tracking the input signal of the communication system, detecting the carrier effectively and calculating the frequency point of the carrier;
2. Detection carrier frequency range is greater than or equal to 75MHz;
3. The search time within 75MHz is less than or equal to 3S;
4. The CPU resource consumption rate of the system should be less than 50%.
3. System Design
According to the functional requirements of the system, the FPGA detection system is designed, and the FPGA system structure is shown in Figure 2.

According to the system structure shown in Figure 2, FPGA detection system mainly includes 12 functional units, namely arm communication interface unit, forward DDC unit, I/O signal strobe switch unit, forward temperature compensation unit, ALC control unit, power detection unit, carrier tracking unit, pilot detection unit, channel separation unit, DUC digital up conversion unit, carrier gain compensation, DAC unit.

According to the system requirements, the carrier search bandwidth is at least 75MHz, and the real-time frequency hopping bandwidth is 25MHz. It needs to be considered that the sampling rate supported by FPGA chip is higher than 150MSps, and the frequency hopping processing involves a lot of high-pass processing resources, which requires FPGA chip to have more resources and higher working frequency. Therefore, the main CPU of FPGA decided to use virtex 6 series chips. Virtex-6 FPGA includes many built-in system level modules. Virtex-6 FPGA provides the best solution to meet the needs of high-performance logic designers, high-performance DSP designers and high-performance embedded system designers. It brings unprecedented functions of logic, DSP, connection and soft microprocessor [14,15].

The top-level pin structure of the carrier search unit in the FPGA chip is shown in Figure 3.
Table 1. Pin description of carrier search unit

| port name          | port type | function description                                      |
|--------------------|-----------|-----------------------------------------------------------|
| i_sys_clk          | IN        | system clock, frequency 184.32MHz: rising edge effective  |
| i_rst_n            | IN        | system reset: effective falling edge                       |
| i_fir_sclr         | IN        | filter reset, high level effective                        |
| i_ddc_data_[15:0]  | IN        | DDC module output data I-channel, data rate 184.32 MSPs   |
| i_ddc_data_q_[15:0]| IN        | DDC module output data Q-channel, data rate 184.32 MSPs   |
| i_gsm_search_en    | IN        | data flag bit, high level effective                       |
| o_car_search_done  | OUT       | carrier search completed, high level effective            |
| o_search_valid     | OUT       | carrier search effective, high level effective            |
| o_car_offset_reg1[15:0]| OUT   | carrier 1 offset                                         |
| ...                | OUT       | ...                                                       |
| o_car_offset_reg16[15:0]| OUT | carrier 16 offset                                       |

As can be seen from the pin list of carrier search unit, the FPGA system can detect up to 16 channels of carriers. Each carrier pin has a register to set the corresponding data. The definition of carrier frequency point information register is shown in Table 2.

Table 2. Definition of carrier frequency point register

| register name (16bit) | Highest position | Low 8 bit | Remarks |
|------------------------|------------------|-----------|---------|
| A1                     | offset center frequency point direction 1: left 0: right | Offset center frequency point position | The value of the lower 8 bits is offset Multiple of central frequency point 200kHz, example: 16'b1000_0000_0000_0011, Represents that the center frequency point of left offset is 3×200=600kHz, So the bandwidth that register can cover is 255×0.2×2=102MHz. When there is no carrier, the register is defined as: 16'b1111_1111_1111_1111 |
| ...                    | offset center frequency point direction 1: left 0: right | Offset center frequency point position | |
| A16                    | offset center frequency point direction 1: left 0: right | Offset center frequency point position | |

4. Algorithm Design

Carrier search unit is the focus of FPGA carrier detection system. In order to meet the system requirements that the carrier search time is less than 3 seconds when the carrier search width is at least 75MHz, the carrier search adopts the three-channel carrier search method, and the carrier search implementation block diagram is shown in Figure 4.

Figure 4. Carrier search block diagram

The carrier search of three channels still belongs to the category of energy detection. The specific steps are as follows: after the input signal (sampling rate is 184.32MSps or twice sampling 92.32MSps) is processed by three DDS frequency shifts with a difference of 200kHz (one channel
number), the area to be detected and two channels on both sides are successively moved to zero frequency. In order to reduce the utilization of resources, the signal after frequency shift is extracted, and then in 1 For the detection within the length of frame or 2-frame data, the lowest signal threshold shall be set here to judge the data of the intermediate channel and accumulate the data larger than the threshold. If it is larger than a time slot, the signal is considered to exist, and its power shall be calculated. After calculating the signal power of the three channels, the ratio between the intermediate channel and the left and right channels shall be compared, if it is larger than the set ratio, Carrier is considered to be present.

At present, the real-time bandwidth of the three channel carrier search is 30MHz, so the block diagram in Figure 4 can adopt the one-way multiplexing processing mode. When the signal bandwidth is greater than 33.3MHz, it is difficult to achieve one-way multiplexing. When the real-time bandwidth is 75MHz, the mixing and extraction can require two or three-way processing in the frequency shift, and the power calculation can adopt the combined way.

The flow of carrier search is shown in Figure 5.

![Figure 5. Carrier search flow chart](image)

Note: (1) the number of points whose intermediate channel number is greater than the set energy threshold is related to the sampling rate and the number of detected frames. For example, when the sampling rate is 2MSps, 1024 points can be set, and the energy threshold is -48dBFS; (2) When the ratio of the intermediate channel to the adjacent channel is greater than 32, the carrier is considered to exist, which is related to the passband of the compensation filter.

The state machine jump chart of carrier search is shown in Figure 6.
Figure 6. Jump chart of carrier search state machine

The status description of carrier search is shown in Table 3.

### Table 3. Status description of carrier search

| status number | status name            | definition                                                                 | transfer condition                                      | new state |
|---------------|------------------------|---------------------------------------------------------------------------|---------------------------------------------------------|-----------|
| 1             | IDLE                   | waiting to start carrier search                                           | carrier search enable                                    | 2         |
| 2             | INITIALIZE            | initialize frequency word address of DDS                                  | initialization complete                                  | 3         |
| 3             | UPDATE_DDS            | generating frequency control words with three consecutive frequency shifts | DDS configuration complete                              | 4         |
|               |                        |                                                                           | detection completed                                      | 8         |
| 4             | CAL_PWR_DELAY         | calculation of power delay                                               | delay completion                                          | 5         |
| 5             | CAL_CENTRAL_PWR       | the energy of the intermediate channel is calculated, in which the number of signal points in a frame of data should be greater than 1024 | when the number of signal points in a frame of data is greater than the set threshold | 6         |
|               |                        |                                                                           | when the number of signal points in one frame data is less than the set threshold | 3         |
| 6             | COMPAR_E_ADJ_PWR      | the comparison between the energy of the intermediate channel and that of the two channels shows that the ratio between the energy of the intermediate channel and that of the two channels should be greater than 32 | the ratio between the energy of the intermediate channel and the energy of the signals on both sides is greater than the set threshold | 7         |
|               |                        |                                                                           | the ratio between the energy of the intermediate channel and the energy of the signals on both sides is less than the set threshold | 3         |
| 7             | CAR_INF_SAVE          | save search carrier                                                      | save finished                                            | 3         |
| 8             | CAR_SEARCH_DONE       | carrier search complete                                                   |                                                         | 1         |
In the implementation, each channel of carrier search interface has a corresponding register, and the definition meaning of corresponding deposit is shown in Table 4.

**Table 4. Register definition**

| register address (hex) | digit (Bit) | name          | description                                                                 |
|------------------------|-------------|---------------|-----------------------------------------------------------------------------|
| 000a                   | <0>         | SEARCH_EN     | carrier search enable switch: 1 is on, 0 is off, and it is on by default     |
| 0010                   | <0>         | CAR_VARY      | represent a change in carrier state, 1 represents a change, and 0 represents no change |
|                        | <15:1>      |               | Not Defined                                                                 |
| 0015                   | <0>         | CON_OVER      | represent that MCU has completed the configuration of various chips, 1 represents that the configuration is completed, 0 represents that the configuration is not completed |
|                        | <15:1>      |               | Not Defined                                                                 |
| 0016                   | <0>         | ERR_INTF      | represent the FPGA and MCU cannot complete the interface communication, and the high bit is valid |
|                        | <1>         | ERR_MODE      | represent the carrier mode of signal unrecognized by FPGA, high bit is valid |
|                        | <2>         | ERR_NOSIG     | represent the FPGA cannot detect the input signal and the high bit is valid |
|                        | <3>         | ERR_MAXSIG    | represents the input signal power detected by FPGA is too high and the high bit is effective |
|                        | <4>         | ERR_MINSIG    | represent the input signal power detected by FPGA is too small and the high bit is effective |
|                        | <5>         | ERR_CONFUSION | the frequency spectrum of representative signal is overlapped                |
|                        | <6>         | ERR_AVERAGE   | represent multiple average errors                                            |
|                        | <7>         | ERR_RST       | represent an error in the carrier search process, and the carrier search program needs to be reinitialized |
|                        | <15:8>      |               | Not Defined                                                                 |
| 0041                   | <15:0>      |               | displays the number of GSM carriers                                          |
| 0051                   | <15>        |               | the description is shown in Table 2                                           |
| 0060                   | <14:0>      |               | the description is shown in Table 2                                           |

5. **Performance Simulation**

In order to test whether the carrier detection performance of the FPGA detection system meets the system design requirements. The performance indexes of the carrier frequency range, carrier search time, carrier detection number and CPU consumption rate of the system are designed. Firstly, the detection frequency range and carrier detection time of the carrier are detected. In this experiment, the carrier frequency range is 1800mhz-1900mhz, and the carrier detection frequency range and carrier detection time are shown in Figure 7.
It can be seen from the experimental results that the carrier detection system based on FPGA can meet the design requirements. When the frequency range is less than 80MHz, the search time is less than 3 seconds. When the frequency range is greater than 80MHz, the search time increases dramatically. Next, the experiment is designed to test the performance of carrier number detection and CPU consumption. When the number of 1-16 carriers is set in the frequency range of 75MHz, the CPU resource consumption of the system is tested. The relationship between the number of carrier detection and the CPU resource consumption of the system is shown in Figure 8.

**Figure 8.** Relationship between carrier detection number and system CPU resource consumption

It can be seen from the test results that the carrier detection system can detect up to 16 channels of carriers. When the number of carrier channels is 8, the CPU utilization rate of the system is relatively low, but with the number of carriers increasing, the CPU utilization rate increases and the growth speed is faster.

6. Conclusion

According to the characteristics of communication system, base and other equipment transmitting signal by carrier wave. In order to better monitor and manage the signal transmission in the communication system and base station, and effectively detect the carrier. This paper designs a carrier detection system based on FPGA. This paper starts from the system design requirements, and describes the requirements from FPGA selection, system block diagram design, carrier detection method design, etc. The performance indexes of the system are tested, such as carrier frequency range, carrier search time, carrier detection number and system consumption rate,. It can be seen from the test results that the maximum detection frequency range of the carrier detection system can meet at least 80MHz, and the maximum number of carrier detection can reach 16 channels. And the system has the advantages of high flexibility and good portability. This design has high application value in communication system, base station and other equipment.

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References
[1] Lan Huan. Research on 5G oriented multicarrier transmission technology[J]. Internet Communication, 2019,(2):14-15.
[2] Wu Wenke. Research on 5G Multicarrier Transmission Technology[J]. Modern Information Technology, 2019,(9):70-71.
[3] http://www.cac.gov.cn/2019-08/30/c_1124938750.htm.
[4] Xue Yujie, Zhou Jie, Liu Xueyang. High spectrum efficiency scheme for single-carrier and multi-carrier MIMO-OFDM[J]. Journal of Nanjing University of Posts and Telecommunications, 2019,39(2):55-62.
[5] Heath, Michael. Refining the Oil and Gas Industry I Through 5G Mobile Technology. Pipeline & Gas Journal, 2019, 246(2):2-3.
[6] Zhaorui Ma, Zheng Dou, Zhigang Li. Research on OFDM Carrier Synchronization. Advanced Hybrid Information Processing, 2018, 219:425-432.
[7] Diez Luis, Cortes Jose A, Canete Francisco Javier, Martos-Naya Eduardo, Iranzo Salvador. A Generalized Spectral Shaping Method for OFDM Signals. IEEE Transactions on Communications, 2019, 67(5): 3540-3551.
[8] Nguyen TLN, Shin Y, Kim JY, Kim DI. Signal Detection for Ambient Backscatter Communication with OFDM Carriers. Sensors (Basel, Switzerland), 2019, 19(3):234-241.
[9] Liu Jiao. Research on Self-carrier Extraction Coherent OFDM System[J]. Ship Electronic Engineering, 2019,(9):69-70.
[10] Li Ji,Wang Hua,WANG Wei. Analysis of Intermittent-Sampling Repeater Jamming Against Multi-Carrier Phase Coded Radar[J]. Signal Processing, 2019,(1):49-56.
[11] Yang Yimin, Liu Tao. Implement for multicarrier modulation technology based on FPGA[J]. Foreign Electronic Measurement Technology, 2018, 37(3):58-61.
[12] Wang W, Du J, Gao J. Multi-Target Detection Method Based on Variable Carrier Frequency Chirp Sequence. Sensors (Basel, Switzerland), 2018, 18(10):437-445.
[13] Lei Lei, You Lei, Yang Yang, Yuan Di, Chatzinotas Symeon, Ottersten, Bjorn. Load Coupling and Energy Optimization in Multi-Cell and Multi-Carrier NOMA Networks. IEEE Transactions on Vehicular Technology, 2019, 68(11): 11323-11337.
[14] https://china.xilinx.com/products/boards-and-kits/device-family/nav-virtex-6.html.
[15] Min Biao, Huang Wei-pei, Cheung Ray C, Yan Hong. A high performance hardware architecture for non-negative tensor factorization. MICROELECTRONICS JOURNAL, 2019, 85:25-33.