Novel optimized design of a piezoelectric energy harvester in a package for low amplitude vibrations

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Abstract. This paper presents a novel piezoelectric energy harvesting device created with the flip-chip bonding of two different parts, one is a MEMS die which plays the role of inertial mass and the other is an associate CMOS chip anchored to the vibrating environment. The flip-chip bonding is performed between the MEMS die, which consists of four piezoelectric beams connected to four PADs or anchor points, and a test PCB, which is used to validate the feasibility of the whole assembled system. The resulting system in package is a proof of concept of a novel design concept that increases the extracted power from an ambient vibration. FEM simulations have been carried out to study the mechanical behaviour of the whole system. Moreover, the fabrication of the piezoelectric die and the test PCB has been successfully performed, as well as their flip-chip integration.

1. Introduction
Nowadays, the use of green energy is becoming almost a requirement for our society. Especially interesting is to scavenge mechanical energy from our environment, because it is virtually omnipresent. On the other hand, the world of electronics devices is moving towards smaller power consumptions. The convergence of these two facts is attracting the interest from researchers in energy harvesting devices at the micro- and mm-scale from ambient vibrations [1]. There are three well-known mechanisms to convert mechanical energy into electricity: they are the electrostatic, electromagnetic and piezoelectric transductions.

In this work, a piezoelectric energy harvester has been designed and its behaviour simulated. Also, the fabrication of a proof of concept device and a preliminary characterization are presented here.

2. Design advantages
The piezoelectric energy harvesting system presented here is created with the flip-chip bonding of two different parts. One is a MEMS die which plays the double role of inertial mass and transduction method. The other is an associate CMOS chip anchored to the vibrating environment. In this way, the resonance motion appears in the way of relative displacement between both chips.
This paper is mainly focused on the MEMS die which consists of four beams connected to four PADs. These PADs work as electrical connection and support point with the CMOS chip where the MEMS die should be mounted or vice versa. Figure 1 shows the 3D model of the whole proposed assembled system, where a CMOS chip with the power management circuitry is mounted on top of a micromachined die with four suspensions covered by a piezoelectric layer.

The use of a whole die as inertial mass has different advantages:

- decrease of the resonance frequency. It is due to the extra mass load provided by the chip substrate itself. If we assume the device to be as a spring-mass system, the resonance frequency is inversely proportional to the squared root of the inertial mass. This mass can be easily increased by changing the size or weight of the die or by adding an additional mass on top of it.
- mechanical energy transferred from the environment to the inertial mass increases. The energy captured from a sinusoidal excitation over the base of a spring-mass system is directly proportional to its inertial mass.
- the majority of the chip area can be utilized for energy transduction, increasing the maximum converted power. The active area is not utilized to create an inertial mass, but to form transduction and suspension elements.
- using different anchor points makes the bandwidth broader. It is due to the superposition of different adjacent resonance modes coming from each anchor element.

When this concept is applied through heterogeneous integration to two different chips, the resulting system can be called Energy Harvester in a Package (EHiP) [3].

![Figure 1. 3D model of the whole system (EHiP) for simulating in COVENTOR®.](image1)

![Figure 2. Cross-section of a suspension after flip-chip and deflection due to an ambient vibration.](image2)

3. MEMS fabrication process and system assembling procedure

The fabrication technology of the piezoelectric die is a variation of a process designed to fabricate Film Bulk Acoustic Resonators (FBARs) with the purpose of achieving mass sensors and RF resonators [2-3]. It is based on an SOI wafer that is both-side patterned with dry etching and consists of a bulk substrate of 500 µm, a silicon dioxide layer of 1 µm and a device silicon layer of 15 µm. Over this wafer a layer of 1 µm is made of AlN and sandwiched between two Pt-Ti layers. Therefore, the new fabrication process can monolithically integrate energy scavenging systems together with FBAR elements.

The technology used to fabricate the piezoelectric device has been recently developed in our group for the integration of FBARs with energy harvesting applications [2]. By using a similar technology, we presented in [3] an energy scavenger with a traditional architecture, i.e. a mass connected to the substrate by means of a beam. It was reported a scavenged power of 0.2 µW extracted at a resonance frequency of 515 Hz and an input acceleration of 0.64 m/s². That device obtained performance results comparable to values extracted from some works with high generated powers in the literature [4-5].
In figure 2 appears a detailed view of cross section of one of the support beams. Figure 3 shows a picture of the fabricated piezoelectric die consisting of four support beams that are covered for a 1µm-thick layer of AlN and internally interconnected in the way that the electrical signals of the top and bottom electrodes are available through the PADS to the CMOS die. When an ambient vibration is present, the whole system resonates along the out-of-plane direction. This resonance motion forces the support beam to be deflected and the AlN layer is bent, getting a strain over this layer that is translated into a piezoelectric potential between the top and bottom electrodes.

Figure 3. Detailed picture of the fabricated piezoelectric die before performing the flip-chip bonding (~5 mm x 5 mm x 515µm, 28 mg).

Figure 4. Photograph of the fabricated PCB (right) and piezoelectric die (left) on top of a 1Euro cent coin (Ø 16.25 mm).

In order to make the flip-chip step more feasible, the role of the CMOS chip was replaced by a test PCB fabricated using a circuit board milling plotter. The PCB has a size of 3 mm x 3 mm, a thickness of around 500 µm and a mass of 23 mg, which is quite similar to the piezoelectric die mass (figure 4). Moreover, in order to gain a security space between both chips, this PCB has four pillars of a height of 1 mm and a width of less than 300 µm.

Figure 5. Assembling process of the test PCB at component alignment system: approaching (a), release of the PCB over the chip after alignment (b), final pasted PCB-chip system (c). Detail of one support beam without external vibration (d) and with a low-level vibration at 5322 Hz (e).
A component alignment system (ERSA PL 550) allowed us to place with precision the PCB over the piezoelectric die. In the case reported in this work, a conductive epoxy has been used to glue both elements. The PCB was pushed over a thin layer of this epoxy was coated on a flat surface in order to get the PCB PADs imprinted. Afterwards, the flip-chip procedure was carried out by aligning the PADs of the PCB and chip (at wafer level), approaching the PCB to the wafer (figure 5(a)), and releasing the PCB over the chip (figure 5(b)) to get the final assembled system (figure 5(c)).

With the goal of avoiding possible issues from the flip-chip step, a test PCB instead of a CMOS chip has been used but the system performance changes from the expected by using the chip. In order to reduce the new resonance frequency, a heavier PCB or an external mass can be utilized. Also an SOI wafer with an active silicon layer of 5 µm will drop off this frequency.

4. FEM simulations and preliminary characterization

COMSOL® and COVENTOR® software tools were used to simulate the mechanical behaviour of the device. Both motion strategies were explored, the single MEMS die anchored by its PADs, i.e. using the MEMS die as inertial mass, and the anchoring of this aforesaid die under the mounted PCB, i.e. the PCB works as inertial mass.

![Figure 6](image)

Figure 6. First (a), second (b) and third (c) resonance modes at 2855 Hz, 2931 Hz, 4080 Hz respectively (in case of using PCB as inertial mass) and electric potential of piezoelectric layers (d) simulated with COMSOL®.

The FEM-based modal simulations show that instead of having a single resonance motion, we have three resonance modes that can be used to harvest mechanical energy from an external vibration. The two first resonance modes (2855 Hz and 2931 Hz, with the PCB as inertial mass, or 2417 Hz and 2481 Hz, with the chip acting as mass) are shown in figure 6(a) and figure 6(b), where the mass is tilted and only two beams are deflected. The out-of-plane resonance motion is obtained at the third mode (4080 Hz, for PCB mass and 3454 Hz for the case of the chip) shown in figure 6(c). In this case, the four beams are bent in the typical way of a clamped-guided beam, obtaining a uniform stress gradient along
the beam that is zero at the middle point and get opposite signs at every beam side. This is translated into an opposite charge density in each piezoelectric layer, and subsequently opposite electric potentials. The use of single electrodes covering the piezoelectric layers of every beam would suppose a cancelation of the majority of the generated charges. To overcome this adverse effect, each beam should have two different electrodes at every beam side. Thus, eight different piezoelectric potentials can be combined to get a global charge generator. Figure 6(d) shows this opposite potential effect and generated voltages of ±4.8V (at open circuit) for a mass vertical displacement of 10 µm.

By using a piezoelectric buzzer, a weak vibration was produced over the wafer close to the assembled PCB (figure 5(c)). A low-amplitude resonance motion was observed (figure 5(d) and figure 5(e)) when applying a sinusoidal wave at 5322 Hz. Regarding its shape, this resonant motion is supposed to be the third mode of resonance of the whole system with the PCB as inertial mass (around 4080 Hz).

5. Conclusions and future tasks
This paper presents a novel piezoelectric energy harvesting device consisting of two different parts bonded by flip-chip. One part is a MEMS die which plays the role of inertial mass and the other is a test PCB used to validate the feasibility of this heterogeneous integration. The resulting system in package is a proof of concept of a novel design concept that increases the extracted power from an ambient vibration. FEM simulations have been carried out to study the mechanical behaviour of the whole system. Also, the fabrication of the piezoelectric die and the test PCB has been successfully performed, as well as their flip-chip integration.

On the other hand, a more sophisticated double side PCB has been designed to allow the electrical connectivity with the piezoelectric chip through the PCB pillars. Moreover, a diode bridge, a capacitor and a SMD circuit for the control and management of piezoelectric energy scavenger will be added. At the same time, an ad-hoc electronic chip will be fabricated in our CNM 2.5-µm CMOS technology.

Finally, the full electromechanical characterization of the presented system is being carried out at this time. Thus, the measurement of frequency and generated power at different resonance modes is our main on-going task.

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