Formal Verification of Flow Equivalence in Desynchronized Designs

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Abstract—Seminal work by Cortadella, Kondratyev, Lavagno, and Sotiriou includes a hand-written proof that a particular handshaking protocol preserves flow equivalence, a notion of equivalence between synchronous latch-based specifications and their desynchronized bundled-data asynchronous implementations. In this work we identify a counterexample to Cortadella et al.’s proof illustrating how their protocol can in fact lead to a violation of flow equivalence. However, two of the less concurrent protocols identified in their paper do preserve flow equivalence. To verify this fact, we formalize flow equivalence in the Coq proof assistant and provide mechanized, machine-checkable proofs of our results.

I. INTRODUCTION

Desynchronization is a popular strategy for designing bundled-data (BD) asynchronous latch-based designs from a synchronous RTL specification. In a desynchronized design, master/slave latches are driven by local clocks controlled by specific classes of asynchronous controllers [1]. Because BD latch-based designs are susceptible to subtle timing assumptions, it is important to ensure that desynchronization preserves the functional behavior of the circuit. Le Guernic et al. [2] propose flow equivalence as a property characterizing when two circuits, either synchronous or asynchronous, have the same functional behavior. Cortadella et al. [1] provide a hand-written proof that a highly concurrent desynchronization controller preserves flow equivalence, and use that result to claim that two less concurrent controllers, called rise-decoupled and fall-decoupled, also preserve flow equivalence.

We identify a subtle flaw in Cortadella et al.’s proof and provide a counterexample showing that the proposed desynchronization controller fails to guarantee flow equivalence. Subtle errors in hand-written proofs are easy to overlook, as evidenced by the wide acceptance of Cortadella et al.’s results.

To ensure that our results are correct, we formalize flow equivalence in the higher-order interactive theorem prover Coq [3], which codifies high-level mathematics (such as induction, case analysis, functions, and relations) in a machine-checkable system. In particular, we show that the core ideas of Cortadella et al.’s work are sound by adapting their flow equivalence proof to the less concurrent fall- and rise-decoupled controllers.

This work illustrates the benefits of applying formal methods to asynchronous design. Other formal techniques in the literature range from verification of hazard-freedom (e.g., [4]) and deadlock-freedom (e.g., [5]), to more general notions of equivalence between gate level implementations, handshaking-level specifications [6–9], and abstract asynchronous communication primitives [10]. Several researchers focus on verifying general properties of asynchronous designs using model checkers [11–13] and proof assistants, including ACL2 [14, 15].

This paper makes several key contributions. Section II describes a counterexample to Cortadella et al.’s hand-written proof in the form of a timing diagram that satisfies the desynchronization protocol but violates flow equivalence, motivating our formal analysis. Section III formalizes the definition of flow equivalence as well as the marked graph specification of the proposed controllers, and Section IV presents Coq proofs that the rise-decoupled and fall-decoupled controllers guarantee flow equivalence.1 Finally, Section V describes some directions for future research, including extending the formalization to Cortadella et al.’s liveness results.

II. COUNTEREXAMPLE

Cortadella et al.’s desynchronization protocol [1] defines a set of requirements for asynchronous controllers of a latch-based circuit. In this section we demonstrate that the desynchronization protocol fails to preserve flow equivalence in general; we give a circuit and a set of clock traces that is valid according to the protocol, but

1 All Coq definitions and proofs can be found in our formalization available at https://github.com/GaloisInc/Coq-Flow-Equivalence.
produces different outputs than the synchronous version of the same circuit.

Consider a three-stage linear pipeline with latches \( A, B, \) and \( C \). Latches \( A \) and \( C \) are even, and have valid initial values \( a_0 \) and \( c_0 \); latch \( B \) is odd, and is uninitialized. When driven synchronously, values for cycle \( n \) are produced for odd latches first, followed by even latches. For \( n > 0 \) we have \( b_n = F_B(a_{n-1}) \) and \( c_n = F_C(b_n) \), where \( F_B \) and \( F_C \) represent the combinational logic before each latch (Figure 1).

The dashed arrows in Figure 1 indicate the timing constraints of the desynchronized protocol, derived from Cortadella et al.’s marked graph specification; asynchronous controllers are allowed to shift the clock transitions arbitrarily forward and backward in time, as long as those constraints are preserved. We construct a counterexample by delaying the first transitions for latch \( A \) as long as possible (Figure 2).

Two circuits are flow-equivalent if the sequences of values stored at their corresponding latches are identical. The trace of values on latch \( C \) in Figure 2 violates flow equivalence: instead of \( [c_0, c_1, c_2, c_3] \), the asynchronous circuit latches \( [c_0, c_1, c_1, c_3] \). Crucially, the second clock pulse of \( C \) ends before the first pulse of \( A \) begins. At this point \( C \) should have latched \( c_2 \), but \( c_2 \) has a transitive data dependency on \( a_1 \), which is not yet available.

The error in Cortadella et al.’s proof arises from a subtle misuse of its induction hypothesis. The proof states that, immediately before the second fall of an even latch’s clock (\( C \)), its predecessor’s clock (\( B \)) must have risen twice, and therefore the induction hypothesis implies that \( B \) has the value \( b_2 \). This is not guaranteed; the induction hypothesis only applies after \( B \) occurs. It appears that the proof assumes that \( B \)’s new value is available as soon as \( B \) occurs, which, as our counterexample shows, is not necessarily the case.

The proof contains a similar statement about even predecessors of odd latches, and it is easy to construct a counterexample to illustrate that case. More complex configurations, including cycles, also give rise to counterexamples.

### III. Formalizing Flow Equivalence

In this section we formalize the definition of flow equivalence in the Coq proof assistant in a way that is amenable to verification later on. Each Coq definition automatically generates an induction principle reflecting the definition’s structure, so different definitions can make proofs easier or harder. Though there are many possible definitions of flow equivalence, the one we present here yields concise and elegant proofs.

Coq is a dependently-typed functional programming language and interactive proof assistant that has been used both to prove significant mathematical theorems [16] and to verify the correctness of realistic software systems [17]. Proof engineers interactively write proof scripts to prove theorems in Coq, from which the system produces a proof term that the Coq kernel can check for validity. Because the kernel is small and trustworthy, the proof scripts used to generate proof terms can be arbitrarily complex and the user can still have confidence that their proof is correct.

We develop the definition of flow equivalence in several stages, illustrating Coq syntax along the way. The resulting formalization could almost certainly be replicated in other provers such as ACL2, Isabelle, or F∗, but Coq’s interactivity, scriptability, and rich inductive definitions were particularly useful in this development.

#### A. Synchronous execution semantics

We first define the synchronous execution of a circuit. Like Cortadella et al., we model circuits with master-
slave latches obtained by decoupling D flip-flops; every latch is either even (master) or odd (slave), and neighboring latches must have opposite parities.

Let even be a set of even latches and let odd be a set of odd latches. We define the type latch of all latches to be made up of both even and odd latches—mathematically, the disjoint union of odd and even.

\[ \text{Inductive } \text{latch} := \text{Odd} : \text{odd} \rightarrow \text{latch} | \text{Even} : \text{even} \rightarrow \text{latch}. \]

In the Coq code, the keyword \text{Inductive} indicates that latch is defined by its constructors, Odd and Even. Odd is a function of type odd \rightarrow latch, so takes an argument drawn from the set odd, and produces a latch.

A state relative to a type \( A \) is a function from \( A \) to values, which are either numbers or undefined.

\[ \text{Inductive } \text{val} := \text{Num} : \text{N} \rightarrow \text{val} | X : \text{val}. \]

\[ \text{Definition } \text{state} (\text{A} : \text{Type}) := \text{A} \rightarrow \text{val}. \]

\textbf{Definition 1 (Circuits).} A circuit consists of lists of neighboring even-odd and odd-even latches, as well as, for each latch, a function that computes its value from the values of its left neighbors. Like Cortadella et al., we model only closed circuits and assume that combinational blocks and latches have zero delay. Any open circuit can be combined with a model of the environment to obtain a closed circuit.

\[ \text{Record circuit} := \]
\[ | \text{eo_nbrs} : \text{list} (\text{even} \times \text{odd}) ; \text{oe_nbrs} : \text{list} (\text{odd} \times \text{even}) ; \text{next}_e (\text{E} : \text{even}) : \]
\[ \text{state} (\text{O} : \text{odd} \& \text{In} (\text{O}, \text{E}) \text{oe_nbrs}) \rightarrow \text{val} ; \text{next}_o (\text{O} : \text{odd}) : \]
\[ \text{state} (\text{E} : \text{even} \& \text{In} (\text{E}, \text{O}) \text{eo_nbrs}) \rightarrow \text{val}. \]

The \text{Record} syntax defines a data type with a collection of functions out of that data type. The \text{circuit} record has four such functions: \text{eo_nbrs} and \text{oe_nbrs} are functions from a \text{circuit} to lists of its even-odd and odd-even neighbors, respectively; \text{next}_e is a function from a \text{circuit}, an even latch \( E \), and a state of the odd left neighbors of \( E \) to the next state of \( E \); \text{next}_o is similar to \text{next}_e, but for odd latches.

In the \text{Record}, the notation \( \{ x : \text{A} \& \text{P}(x) \} \) restricts the type \( \text{A} \) to those elements satisfying the predicate \( \text{P} \). For example, the \text{next}_e function takes as input a state restricted to the odd latches \( O \) satisfying the predicate \( \text{In} (\text{O}, \text{E}) \text{oe_nbrs} \), where \text{In a ls} indicates that the element \( a \) occurs in the list \( \text{ls} \).

When a latch \( l \) can be either even or odd, we write \( \text{next}(c, st, l) \) for the corresponding next-state function.

\textbf{Definition 2 (Synchronous Execution).} The \textit{synchronous execution} of a circuit \( c \) is a function from the initial state \( st_0 \) of the circuit to the state at its \( n \)th clock cycle. In this paper, odd latches update first each clock cycle, followed by even latches.\footnote{Without loss of generality, this ordering could be reversed so that even latches update first; the initial markings of the protocols in Figure 4 would need to be updated to reflect that convention.} That is:

\[ \text{sync}(c, st_0, n)(l) = \]
\[ \begin{cases} 
  \text{st}_0(l) & \text{if } n = 0 \land l \text{ is even} \\
  X & \text{if } n = 0 \land l \text{ is odd} \\
  \text{next}(c, \text{sync}(c, st_0, n), l) & \text{if } n > 0 \land l \text{ is even} \\
  \text{next}(c, \text{sync}(c, st_0, n - 1), l) & \text{if } n > 0 \land l \text{ is odd} 
\end{cases} \]

\textbf{B. Asynchronous execution semantics}

Next, we describe how such a circuit can be executed \textit{asynchronously} by replacing the shared clock with a series of local clocks controlled by bundled data controllers. This section describes the asynchronous execution semantics with respect to sequences of rising and falling transitions of the local clocks. The allowable sequences are constrained by controller specifications described in Section III-C.

\textbf{Definition 3 (Events and Traces).} An event \( e \) is the rise (written \( + \)) or fall (written \( - \)) of a latch \( l \). A trace is a list of events—rises and falls of a latch’s clock. When a latch’s clock rises, the latch becomes transparent; when it falls, the latch becomes opaque.

\[ \text{Inductive } \text{event} := \text{Rise} : \text{latch} \rightarrow \text{event} \]
\[ | \text{Fall} : \text{latch} \rightarrow \text{event}. \]

\[ \text{Definition } \text{trace} := \text{tail_list event}. \]

\[ \text{A tail_list is either empty, denoted } \text{t_empty}, \text{ or is an element } a \text{ appended onto another tail_list } l, \text{ denoted } l \triangleright a. \]

\textbf{Definition 4 (Transparency).} A transparency characterizes whether a latch is transparent or opaque at a particular point.

\[ \text{Inductive } \text{transparency} := \text{Transparent} | \text{Opaque}. \]

\footnote{Note that this definition is well-founded: the values of even latches at time \( n > 0 \) depend on the values of their odd predecessors at time \( n \), which themselves depend on the values of their even predecessors at time \( n - 1 \).}
The function \( \text{latch\_transp} \) computes the transparency of a latch \( l \) after executing a trace \( t \).

\[
\text{latch\_transp}(t, l) =
\begin{cases}
\text{Transparent} & \text{if } t = t\text\_empty \land l \text{ is odd} \\
\text{Opaque} & \text{if } t = t\text\_empty \land l \text{ is even} \\
\text{Transparent} & \text{if } t = t' \triangleright l+ \\
\text{Opaque} & \text{if } t = t' \triangleright l- \\
\text{latch\_transp}(t', l) & \text{if } t = t' \triangleright e \text{ otherwise}
\end{cases}
\]

**Definition 5 (Asynchronous Execution).** Given an initial state \( st_0 \), the asynchronous execution of a trace \( t \) on a circuit \( c \) is defined by a 5-ary relation, for which we introduce the syntax \( \langle c, st_0 \rangle \vdash t \downarrow l \mapsto v \). Here, \( l \) is a latch and \( v \) is the value of \( l \) after executing \( t \). When this relation holds of a 5-tuple, we say that \( l \) evaluates to \( v \) by means of \( t \):

- If \( l \) is transparent in \( t \) and for all left neighbors \( l' \) of \( l \) it is the case that \( \langle c, st_0 \rangle \vdash t \downarrow l' \mapsto st(l') \), then \( \langle c, st_0 \rangle \vdash t \downarrow l \mapsto \text{next}(c, st, l) \).
- If \( l \) is opaque in \( t \) and \( t \) is the empty list, then \( \langle c, st_0 \rangle \vdash t\text\_empty \downarrow l \mapsto st_0(l) \).
- If \( l \) is opaque in \( t \) and \( t = t' \triangleright e \) such that \( e \neq l- \), then \( \langle c, st_0 \rangle \vdash t' \downarrow l \mapsto v \) implies \( \langle c, st_0 \rangle \vdash t' \triangleright e \downarrow l \mapsto v \).
- Finally, if \( t = t' \triangleright l- \) and for all left neighbors \( l' \) of \( l \) it is the case that \( \langle c, st_0 \rangle \vdash t' \downarrow l' \mapsto st(l') \), then \( \langle c, st_0 \rangle \vdash t' \triangleright l- \downarrow l \mapsto \text{next}(c, st, l) \).

Definition 5 has four cases, depending on both the transparency of \( l \) in \( t \) and the structure of \( t \). This choice of decomposition gives rise to a strong induction principle based on those four cases, which we will use in Section IV to prove flow equivalence.

Figure 3 shows the Coq definition of this relation, extended with an additional parameter \( O \) corresponding to the transparency of \( l \) in \( t \). The additional parameter makes the Coq relation easier to work with, as we often need to consider only opaque or only transparent latches. Note that function application in Coq is written as the function name (e.g. \( \text{latch\_transp} \)) next to its arguments (e.g. \( t, l \)) with whitespace separators.

Each constructor in the Coq definition is a logical formula that indicates when the relation is satisfied. For example, when the trace is empty the circuit is in its initial state: even latches are opaque and they have their corresponding initial values. This property is written \( \langle c, st_0 \rangle \vdash t\text\_empty \downarrow E \mapsto \text{Opaque} \) \( st_0(E) \), and the Coq proof term \( \text{async\_nil E} \) is evidence that it holds.

**C. Marked graphs**

Cortadella et al. characterize the traces allowed by a particular instantiation of controllers as a marked graph, a class of Petri net such that each place has exactly one input and one output transition.

**Definition 6 (Marked Graphs).** Given a set \( T \) of transitions, a marked graph is a set of places, each with an associated input and output transitions, with an initial marking—a function from places to natural numbers.

\[
\text{Record marked\_graph } T :=
\{ \text{place} : T \rightarrow \text{Type} ; \text{init\_marking} : \forall t1 t2, \text{place} t1 t2 \rightarrow \text{N} \}.
\]

**Definition marking** \( M : \text{marked\_graph} \) := \( \forall t1 t2, \text{place} t1 t2 \rightarrow \text{N} \).

Definition 6 is equivalent to the standard definition of marked graphs as (1) a set of places, (2) a set of transitions, and (3) a flow relation such that each place has unique input and output transitions. However, the type-theoretic Definition 6 enables easier reasoning in Coq. For example, suppose we have a place \( p \) into \( t \) in the standard definition. Knowing \( t \), there are a finite number of options for \( p \), which can be obtained by iterating over the flow relation. Definition 6 does not require this iteration; Coq automatically identifies the possible options for \( p \) by case analysis.

Cortadella et al. describe marked graph protocols with respect to a circuit’s sets of neighboring latches. For each even-odd and odd-even pair they specify the places corresponding to that pair’s rises and falls, as illustrated in Figure 4. The Coq definition of the desynchronization protocol (Figure 4a) is shown in Figure 5.

**Definition 7 (Enabled Transitions).** A transition is enabled in a marking if all of its input places are positive. An enabled transition can fire to produce a new marking:

\[
\text{fire}(t, M, m)(p) =
\begin{cases}
\{ m(p) - 1 & \text{if } p \text{ leads into } t \\
\{ m(p) + 1 & \text{if } p \text{ leads out of } t \\
\{ m(p) & \text{otherwise}
\end{cases}
\]

A marked graph \( M \) evaluates to the marking \( m \) from a tail-list \( ls \) of transitions, written \( M \vdash ls \downarrow m \), if the following relation holds:

- If \( ls \) is empty, then \( M \vdash ls \downarrow \text{init\_marking}(M) \).
- If \( ls = ls' \triangleright t \) such that \( M \vdash ls' \downarrow m' \) and \( t \) is enabled in \( m' \), then \( M \vdash ls \downarrow \text{fire}(t, M, m') \).

A crucial property of marked graphs is that they preserve the markings of cycles. We write \( p : t_1 \leadsto t_2 \) for a path spanning from \( t_1 \) to \( t_2 \), and \( m(p) \) for the sum of the markings of the places along the path.

**Lemma 1.** If \( p \) is a cycle in a marked graph \( M \) and \( M \vdash ls \downarrow m \), then \( m(p) = \text{init\_marking}(M)(p) \).
Inductive async (c : circuit) (st0 : state latch) : trace → latch → transparency → val → Prop :=
| async_transparent : ∀ l t st v, transparent t l = Transparent →
  ⟨c,st0⟩{- t ↓ l' ↦→ {transparent t l'}} st l' →
  ⟨c,st0⟩{- t ↓ l' → {Transparent} st l'}. 
| async_nil : ∀ E,
  ⟨c,st0⟩ ⊢ t_empty ↓ Even E ↦→ {Opaque} st0 (Even E).
| async_opaque : ∀ e t' v, transparent (t' ⊢ e) l = Opaque →
e <> Fall l →
  ⟨c,st0⟩{- t' ⊢ e ↓ l → {Opaque} v →
  ⟨c,st0⟩{- t' ⊢ e} st l' → {Opaque} v} next c st l.
where "⟨ c , st ⟩{- t ↓ l → { O } v} := \{ async c st t l O v}.
Fig. 3: Coq definition of asynchronous execution of a trace.

(a) Desynchronization Protocol  (b) Rise-Decoupled Protocol  (c) Fall-Decoupled Protocol
Fig. 4: Three marked graph protocols for desynchronization, from Cortadella et al. [1]. A double arrow \( t \leftrightarrow t' \) indicates that there are places in both directions; markings \( t \rightarrow t' \) are indicated by dots appearing closer to \( t' \) than \( t \). For every pair of even-odd (respectively, odd-even) neighbors, the marked graph has the places and initial markings indicated by the diagram on the left (respectively, on the right).

Inductive desync_place : event → event → Type :=
| fall (l : latch) : desync_place (Rise l) (Fall l).
| rise (l : latch) : desync_place (Fall l) (Rise l).
| rise_fall : ∀ l l', neighbor c l l' →
desync_place (Rise l) (Fall l')
| fall_rise : ∀ l l', neighbor c l l' →
desync_place (Fall l') (Rise l).

Definition desynchronization : marked_graph event :=
| place := desync_place
; init_marking := fun x _ p ⇒ match p with
| rise (Even _) ⇒ 1
| fall (Odd _) ⇒ 1
| rise_fall _ _ _ ⇒ 1
| _ ⇒ 0
end |).
Fig. 5: Desynchronization protocol defined in Coq. Given a proof \( p \) that the pair \((E, O)\) is in the list of even-odd neighbors, \( E \_ \_ \_ p \) is a place from \( E+ \) to \( O- \). In the initial marking, the notation \( \text{fun } x \Rightarrow e \) defines a function of type \( A \rightarrow B \) (in this case a marking) by giving a value \( e \) of type \( B \) for every argument \( x \) of type \( A \).
This result follows from the following helper lemma:

**Lemma 2.** If \( t \) is enabled in \( M \) and \( p : t_1 \rightarrow t_2 \), then:

\[
\begin{align*}
&& t = t_1 = t_2 &\implies \text{fire}(t, M, m)(p) = m(p) \\
&& t = t_1 \neq t_2 &\implies \text{fire}(t, M, m)(p) = m(p) + 1 \\
&& t = t_2 \neq t_1 &\implies \text{fire}(t, M, m)(p) = m(p) - 1 \\
&& t \neq t_1 \land t \neq t_2 &\implies \text{fire}(t, M, m)(p) = m(p)
\end{align*}
\]

D. Flow equivalence

Le Guernic et al. [2] define two circuits to be flow-equivalent if and only if (1) they have the same set of latches, and (2) for each latch \( l \), the sequence of values latched by \( l \) is the same in both circuits. It need not be the case that the two circuits have the same state at any specific point in time, but the projection of the states onto each latch should be the same. This ensures that, even if the timing behaviors of the two circuits differ, their functional behaviors are the same.

In this case, we are interested in comparing the same circuit under two different execution models: synchronous and asynchronous. For the synchronous model, the projection of the values latched by a latch \( l \) are given by the function \( \text{sync}(c, st_0, i)(l) \). For the asynchronous model, we have to consider the execution of every trace allowed by the asynchronous controller.

**Definition 8 (Flow Equivalence).** A marked graph \( M \) ensures flow equivalence of a circuit \( c \) with initial state \( st_0 \) if every trace allowable by the marked graph has the same synchronous and asynchronous execution. That is, let \( t \) be a trace compatible with \( M \), and let \( l \) be a latch, opaque in \( t \), such that \( \langle c, st_0 \rangle \vdash t \downarrow l \mapsto v \). Then \( v \) is the \( i \)th value of the synchronous execution of \( c \), where \( i = \text{num}(l-) \), the number of occurrences of \( l- \) in \( t \).

**Definition flow_equiv (M : marked_graph event)**

\[
\begin{align*}
(c : \text{circuit}) (st0 : \text{state latch}) := \\
\forall t \vdash v, (exists m, (M)\neg t \downarrow m) \rightarrow \\
\langle c, st0 \rangle \vdash t \downarrow l \mapsto \{\text{Opaque}\} v \rightarrow \\
v = \text{sync}(c, st0, \text{num}(\text{Fall} l)) t l.
\end{align*}
\]

IV. VERIFIED FLOW-EQUIVALENT PROTOCOLS

In this section we prove in Coq that the rise-decoupled and fall-decoupled protocols illustrated in Figure 4 preserve flow equivalence, and revisit the counterexample of Section II in the context of the formalization.

A. Rise-decoupled protocol

The rise-decoupled protocol, also called fully-decoupled [18] and illustrated in Figure 4b, preserves the invariant that when \( l \) is latched for the \( i \)th time, its predecessors have also been latched the appropriate number of times (either \( i \) or \( i-1 \) times); thus, \( l \) correctly latches its \( i \)th synchronous value. Figure 6 illustrates several possible interleavings of neighboring latches that satisfy the rise-decoupled protocol. Notice that \( B \) may not acquire its correct value by the \( i \)th occurrence of \( B+ \), but it will by the \( i \)th occurrence of \( B- \).

Fix a circuit \( c \) and an initial state \( st_0 \). The definition of the rise_decoupled marked graph with respect to \( c \) is omitted here for space, but is similar that of the desynchronization protocol shown in Figure 5. In the Coq definition, we add two redundant arcs to ensure that there are always arcs from \( l- \) to \( l+ \) and vice versa. Since there is at most one place between two events \( e \) and \( e' \), we write \( (e \rightarrow e') \) for that place when it exists.

To prove that the rise-decoupled protocol preserves flow equivalence, we first prove several lemmas about the rise-decoupled marked graph.

**Lemma 3.** Let rise_decoupled \( \vdash t \downarrow m \). If \( l \) has a right neighbor \( l' \) such that \( m(l- \rightarrow l') > 0 \), then \( l \) is opaque in \( t \).

**Proof.** By induction on \( t \). Using Lemma 1 and some light automation (about 50 lines of Coq tactics that will be re-used for other proofs), this lemma is proved in fewer than 20 lines of Coq proof scripts.

Next, we prove a lemma relating the number of occurrences of \( l- \) in a trace for neighboring latches.

**Lemma 4.** Let rise_decoupled \( \vdash t \downarrow m \). If \( l- \) is enabled in \( m \), then for all left neighbors \( l' \) of \( l \),

\[
\text{num}(l') t = \begin{cases} 
\text{num}(l-) t & \text{if } l \text{ is odd} \\
1 + \text{num}(l-) t & \text{if } l \text{ is even}
\end{cases}
\]

**Proof.** The induction hypothesis must be strengthened to account for three exhaustive cases: \( m(l- \rightarrow l') > 0 \); \( m(l' \rightarrow l+) > 0 \); and \( m(l+ \rightarrow l-) > 0 \). These cases are exhaustive because of Lemma 1: the sum of these three values is exactly equal to 1. The proof then proceeds by induction on \( t \).
Finally, we can prove the main result, that rise_decoupled satisfies flow equivalence.

**Theorem rise_decoupled_flow_equiv :**
flow_equiv rise_decoupled c st0.

Recall that we have already fixed the circuit c and initial state st0 and that the definition of the rise_decoupled marked graph depends on c.

Unfolding the definition of flow equivalence, we can write out the statement of the theorem in English:

**Theorem 5.** If \( \langle c, st0 \rangle \vdash t \downarrow l \rightarrow v \) such that l is opaque in t and rise_decoupled \( \vdash t \downarrow m \), then v = sync(c, st0, num (l−) t)(l).

**Proof.** By induction on the asynchronous evaluation judgment \( \langle c, st0 \rangle \vdash t \downarrow l \rightarrow v \). The structure of that definition leads to an induction principle with four cases.
1) The first case, where l is transparent in t, is vacuous.
2) If t is the empty trace it suffices to consider only even latches, for which the result is immediate.
3) If \( t = t' v e \) such that \( e \neq l− \), the result follows immediately from the induction hypothesis.
4) Finally, the only non-trivial case is when \( t = t' v l− \).

Since \( l− \) is enabled, its left neighbors are all opaque and so have already acquired their correct values.

In this case, \( v = next(c, st, l) \) where, for all left neighbors \( l' \) of \( l \), \( \langle c, st0 \rangle \vdash t' \downarrow l' \rightarrow st(l') \).

Since \( l− \) is enabled in rise_decoupled \( \vdash t' \downarrow l' \), \( l' \) is opaque in \( t' \) (Lemma 3).

Thus the induction hypothesis applies:

\[ st(l') = sync(c, st0, num (l−) t')(l') \]

Unfolding definitions,

\[ sync(c, st0, num (l−) t)(l) = next(c, st', l) \]

where, for all left neighbors \( l' \) of \( l \),

\[ st'(l') = \begin{cases} 
  sync(c, st0, 1 + i)(l') & \text{if } l \text{ is odd} \\
  sync(c, st0, i)(l') & \text{if } l \text{ is even}
\end{cases} \]

and where \( i = num (l−) l' \). The fact that \( st(l') = st'(l') \) follows from Lemma 4.

\[ \square \]

Note that we could have performed induction on the trace t here, but that would not be sufficient for the fall-decoupled proof, which requires us to reason about both transparent and opaque latches.

**B. Fall-decoupled protocol**

The rise-decoupled protocol of the previous section allows the rises of clocks to interleave arbitrarily as long as the falls of those clocks obey the inductive invariant. In the fall-decoupled protocol (Figure 4b), the situation is reversed—a clock may fall either before or after its predecessors’ clocks fall, as long as its rise occurs after its predecessors’ clocks rise, as illustrated in Figure 7.

Under the zero-delay assumption, the model preserves the invariant that each latch will obtain its correct value as soon as it goes transparent, and that value will be stable until it goes opaque again.

For the proof of flow equivalence, we build on the same structure of lemmas as for the rise-decoupled protocols, proving variants of Lemmas 3 and 4 adapted to the fall-decoupled protocol. For example:

**Lemma 6.** Let fall_decoupled \( \vdash t \downarrow m \). If l is opaque in t, then

\[ num (l−) t = \begin{cases} 
  1 + num (l+) t & \text{if } l \text{ is odd} \\
  num (l+) t & \text{if } l \text{ is even}
\end{cases} \]

If l is transparent in t, then for all left neighbors \( l' \) of l:

\[ num (l+) t = \begin{cases} 
  num (l'+) t & \text{if } l \text{ is odd} \\
  1 + num (l'+) t & \text{if } l \text{ is even}
\end{cases} \]

In the rise-decoupled protocol, the proof of flow equivalence relies on the fact that, whenever the event \( l− \) is enabled, all of l’s left neighbors are opaque, so are guaranteed to have their correct values. This is not the case in the fall-decoupled protocol, where l’s left neighbors might be either transparent or opaque.

Therefore, it is necessary to strengthen the statement of flow equivalence to account for the values of both opaque and transparent latches.

**Theorem 7.** If fall_decoupled \( \vdash t \downarrow v \) and \( \langle c, st0 \rangle \vdash t \downarrow l \rightarrow v \), then \( v = sync(c, st0, i)(l) \), where

\[ i = \begin{cases} 
  1 + num (l+) t & \text{if } l \text{ is odd} \\
  num (l+) t & \text{if } l \text{ is even}
\end{cases} \]

**Proof.** By induction on the relation \( \langle c, st0 \rangle \vdash t \downarrow l \rightarrow v \).
1) First, if l is transparent in t, then \( v = next(c, st, l) \) such that, for all left neighbors \( l' \) of l,

\( \langle c, st0 \rangle \vdash t \downarrow l' \rightarrow st(l') \).

Fig. 7: Timing diagram illustrating valid interleavings of the fall-decoupled protocol. Notice that the value \( a_1 \) is always available by the rise of B’s clock.
Notice that $i > 0$: for $l$ odd this follows immediately from the definition; for $l$ even there is at least one occurrence of $l^+$ in $t$ since even latches are initially opaque. Thus, $\text{sync}(c, st_0, i)(l) = \text{next}(c, st', l)$ where $st' = \text{sync}(c, st_0, \text{num}(l^+) - 1)(l)$.  

It suffices to show that for all left neighbors $l'$, $\text{st}(l') = \text{st}′(l')$. By induction, $\text{st}(l') = \text{sync}(c, st_0, i')(l')$ where

$$i' = \begin{cases} 1 + \text{num}(l') & \text{if } l' \text{ is odd} \\ \text{num}(l') & \text{if } l' \text{ is even.} \end{cases}$$

By Lemma 6 we know that $\text{num}(l^+) = i'$, which completes the proof.

2) If $l$ is opaque in the empty trace, it must be odd, and the result is trivial.

3) If $l$ is opaque in $t = t' \triangleright e$ where $e \neq l^-$, the result is straightforward from the induction hypothesis on $l'$.

4) Finally, if $t = t' \triangleright l$, then $v = \text{next}(c, st, l)$ where $\langle c, st_0 \rangle \triangleright l' \triangleright st(l')$ for all left neighbors $l'$ of $l$. Furthermore, $\text{sync}(c, st_0, i')(l)$ is equal to $\text{next}(c, st', l)$ where $st' = \text{sync}(c, st_0, \text{num}(l^+) - 1)(l')$. So it suffices to show that, for all left neighbors $l'$, $\text{st}(l') = \text{st}′(l')$. By the induction hypothesis $\text{st}(l') = \text{sync}(c, st_0, i')(l')$, where

$$i' = \begin{cases} 1 + \text{num}(l') & \text{if } l' \text{ is odd} \\ \text{num}(l') & \text{if } l' \text{ is even.} \end{cases}$$

By Lemma 6 we know $i' = \text{num}(l^+) = i'$, as required. □

Finally, we must show that Theorem 7 implies flow equivalence.

**Corollary 8.** Whenever $(c, st_0) \vdash t \triangleright l \mapsto v$ such that $l$ is opaque in $t$ and fall_decoupled $\vdash t \triangleright m$, then $v = \text{sync}(c, st_0, i)(l)$ where $i = \text{num}(l^-) = t$.

**Proof.** It suffices to show that

$$\text{num}(l^-) = t = \begin{cases} 1 + \text{num}(l^+) & \text{if } l \text{ is odd} \\ \text{num}(l^+) & \text{if } l \text{ is even,} \end{cases}$$

which follows from Lemma 6. □

**C. Less concurrent protocols**

Cortadella et al. also discuss three other protocols that are even less concurrent than the rise-decoupled and fall-decoupled protocols, and claim they are flow equivalent since every trace they accept is also accepted by a known flow-equivalent protocol. Because they are all three subsumed by the rise- and fall-decoupled protocols, this is still true in our case. The formal proofs of this result depend only on the proof that one marked graph refines another. As an exercise, we proved this fact for the semi-decoupled protocol in our Coq repository.

**Program Definition** $c : \text{circuit even odd} := \{ \text{e.o_nbrs} := [(A, SRC); (A, B); (C, SNK)] \}$

$i$ $\triangleright$ $e := \text{fun E \Rightarrow \text{match E with}}$

$A \Rightarrow \text{fun st \Rightarrow st (SRC)}$  $C \Rightarrow \text{fun st \Rightarrow inc_val (st B)}$

$\text{end}$

$t$ $\triangleright$ $e := \text{fun O \Rightarrow \text{match O with}}$

$\text{SRC} \Rightarrow \text{fun st \Rightarrow inc_val (st A)}$  $\text{B} \Rightarrow \text{fun st \Rightarrow inc_val (st A)}$

$\text{SNK} \Rightarrow \text{fun _ \Rightarrow Num 0}$  $\text{end}$

---

**D. Counterexample, revisited**

Finally, we revisit the counterexample to desynchronization described in Section II in the formal setting, providing a concrete circuit and a trace compatible with desynchronization such that, after executing the trace, there is a latch whose value is not equal to $\text{sync}(c, st_0, \text{num}(l^-) - 1)(l)$. The proof of flow equivalence fails in this case because neither of the inductive invariants described in the rise-decoupled or fall-decoupled protocols are satisfied—the desynchronization protocol allows latches to go opaque before all of their left neighbors have gone opaque, which can result in an entire value being dropped, as in Figure 2.

**Theorem 9.** There exists a circuit $c$ for which the desynchronization protocol does not ensure flow equivalence.

**Proof.** Figure 8 shows a three-stage pipeline, similar to the one in Section II but with two additional latches $\text{SRC}$ and $\text{SNK}$ representing the input and output environments respectively. In the initial state, all latches have value $X$, and with each pulse, the source environment $\text{SRC}$ sends integers of increasing value to $A$. Each pipeline stage increments its input by one (denoted $\text{inc_val} v$), and the output environment $\text{SNK}$ consumes the output of $C$.

We take a prefix of the trace illustrated in Figure 2 up until the second fall of $C$’s clock. It is at this point that flow equivalence is violated—the second value latched by $C$ is still $\text{sync}(c, st_0, 1)(C)$.

$$t^e = [\text{SNK}, -C+, C-, B-, C-, \text{SNK+}, \text{SNK}, C+, B+, C-]$$

It is easy to check that there exists a marking $m$ such that $\text{desynchronization} \vdash t^e \triangleright m$, and that $(c, st_0) \vdash t^e \triangleright C \mapsto \text{sync}(c, st_0, 1)(C)$. To complete the proof that flow equivalence is violated, it suffices to check that $\text{sync}(c, st_0, 1)(C) \neq \text{sync}(c, st_0, 2)(C)$.

□
V. SUMMARY AND FUTURE WORK

This paper makes three contributions: we identify a mistake in a hand-written proof, carefully formalize the relevant definitions, and adapt the proof to two variants of the original protocol. This research highlights the benefits of formal theorem proving to verify that a design satisfies desirable properties.

Future work will apply this framework to verify the correctness of gate-level implementations of the controllers by checking that they satisfy the rise- or fall-decoupled protocols. In addition, we plan to extend our Coq framework to account for more abstract design specifications such as FF-based synchronous designs and CSP-like specifications, as well as more realistic delay models. A long-term goal is to develop a comprehensive assurance framework for desynchronization-based design flows, which would account for the correctness of retimed datapaths and liveness. These extensions may require bridging disparate formal frameworks, including static timing analysis, equivalence, and model checking.

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