Efficient Execution of Quantized Deep Learning Models: A Compiler Approach

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Abstract—A growing number of applications implement predictive functions using deep learning models, which require heavy use of compute and memory. For deep learning workloads to run well on a broad range of systems from cloud-scale clusters to low-power edge devices, they need to use available compute and memory resources more efficiently. One popular technique for increasing resource efficiency is 8-bit integer quantization, in which 32-bit floating point numbers (fp32) are represented using shorter 8-bit integer numbers. Although deep learning frameworks such as TensorFlow, TFLite, MXNet, and PyTorch enable developers to quantize models with only a small drop in accuracy, they are not well suited to execute quantized models on a variety of hardware platforms. For example, TFLite is optimized to run inference on ARM CPU edge devices but it does not have efficient support for Intel CPUs and Nvidia GPUs. In this paper, we address the challenges of executing quantized deep learning models on diverse hardware platforms by proposing an augmented compiler approach. A deep learning compiler such as Apache TVM can enable the efficient execution of model from various frameworks on various targets. Many deep learning compilers today, however, are designed primarily for fp32 computation and cannot optimize a pre-quantized INT8 model. To address this issue, we created a new dialect called Quantized Neural Network (QNN) that extends the compiler’s internal representation with a quantization context. With this quantization context, the compiler can generate efficient code for pre-quantized models on various hardware platforms. As implemented in Apache TVM, we observe that the QNN-augmented deep learning compiler achieves speedups of 2.35×, 2.15×, 1.35× and 1.40× on Intel Xeon Cascade Lake CPUs, Nvidia Tesla T4 GPUs, ARM Cortex-A CPUs on Raspberry Pi3 and Pi4 respectively against well optimized fp32 execution. The use of QNN with compilation of pre-quantized models enables developers to achieve model execution performance comparable to the state-of-the-art framework-specific solutions but on a wider range of hardware platforms.

I. INTRODUCTION

A. Background

The effectiveness of deep learning in image processing and natural language processing tasks has led to the development of a growing number of applications that run deep learning models on a wide range of systems, from cloud-scale clusters to resource-limited edge-devices [12,34]. The widespread use of deep learning frameworks such as TensorFlow [3], PyTorch [6] and MXNet [7] drives the applications of deep learning. These frameworks enable model developers to quickly build, train, and deploy models on many hardware platforms. The frameworks provide a set of operators, where each operator represents a mathematical computation, e.g., convolution2D (referred to as conv2d), ReLU (rectified linear unit), batch normalization etc. These operators are typically converted to machine code using a hardware-specific library, e.g., Intel DNNL [8] and Nvidia CuDNN [9].

In general, deep learning models require substantial compute and memory resources [3,4], which can burden even powerful servers leave alone low-power edge devices. Researchers have implemented various techniques – algorithms, software, hardware – to reduce the compute and memory burden of deep learning models to simplify their development and deployment [12,13].

Among these techniques, quantization is a promising and well-studied approach. Quantization represents floating point 32-bit (fp32) numbers, which are used frequently in the deep learning models, with integer 8-bits (int8) [11,14,15], reducing the memory footprint by a factor of four. The most widely-used form of integer quantization is uniform quantization [11], where an fp32 tensor ($A_{fp32}$) is represented with a quantized int8 tensor ($Q_A$) along with quantization attributes - scale ($scale_A$) and zero point ($zp_A$) as shown below

$$A_{fp32} = scale_A \times (Q_A - zp_A) \quad (1)$$

Quantization enables a model to consume fewer compute and memory resources while keeping its accuracy close to that of the unquantized model (where the inputs and parameters are represented in fp32). We have observed that int8 quantization is most widely used in the real world because (1) prior works have shown that int8 representation works well empirically in preserving model accuracy [11,14,15]; (2) popular hardware platforms like Intel CPUs, Nvidia GPUs, and ARM CPUs are introducing low-level instructions support to perform int8 data type computation efficiently.

As a result, deep learning frameworks have of late started to implement uniform int8 quantization. Most of these efforts have focused on retaining accuracy [11,14,15]. For example, instead of scalar scale in Equation 1, we can use per-channel scale to get more fine-grained quantization [16]. Similarly, we can use symmetric or asymmetric quantization based on the value of zero points and choose a suitable performance-accuracy trade-off [11].

However, there is very little focus on the broad deployment and efficient execution of these framework-quantized models (hereafter referred to as pre-quantized models) on a variety of platforms (server and edge). This paper tackles the challenges associated with model inference. Specifically, this paper presents a universally applicable approach to execute pre-quantized models from deep learning frameworks (e.g.
TFLite, MXNet, PyTorch) efficiently on a variety of hardware platforms (e.g. Intel CPUs, Nvidia GPUs, ARM CPUs).

B. Quantization in Deep Learning Frameworks

Adding support for the execution of pre-quantized models in each deep learning framework is not an efficient use of developer time. First, there are several popular frameworks in widespread use, which means that the same task must be duplicated across multiple frameworks. Second, a model is trained and quantized in a framework, it can only run in the same framework on the hardware that the framework supports; i.e. an MXNet model quantized on Intel CPUs cannot run in TFLite on ARM CPUs. Third, a framework typically handles quantization by adding new quantized operators, e.g., TFLite has quantized operators such as quantized_conv2d, quantized_add. However, adding quantized operators to a framework does not automatically enable the framework to execute pre-quantized models efficiently. There are several obstacles facing a framework.

- **Lack of Kernel Library Support.** Frameworks typically rely on high-performance kernel libraries (e.g. Intel DNNL and Nvidia CuDNN) to process computationally-intensive operators. When a new operator is added to the framework, the kernel libraries integrated with the framework must add corresponding support this new operator. Without that support, the quantized model either cannot run well or cannot run at all.

- **Per-operator Overhead.** Operators in the framework are tightly coupled. The best use of a new operator requires corresponding rules and updates across the framework optimization toolchain. For example, one might want to fuse quantized conv2d with a requantize operator.

- **Diverse Hardware Platforms.** Most critically, the hardware platforms have varying levels of support for quantization. Each platform often has specific requirements for these new operators, e.g., Intel CPUs with x86 architecture prefer the input data types of the quantized conv2d to be \texttt{uint8 x int8} due to the Intel Vector Neural Network Instructions (VNNI) requirement [17]. Similarly, CPUs in ARMv8 architecture have special instructions to accelerate the \texttt{int16 multiply-accumulate}, while ARMv8.2 CPUs introduce DOT instructions to directly speed up \texttt{int8 multiply-accumulate} [18]. These requirements percolate up to the framework operators, making it difficult for a framework to support many hardware platforms evenly.

In a nutshell, the quantization mechanism in deep learning frameworks ensures the accuracy of quantized models but is insufficient to ensure their efficiency on a variety of hardware platforms. The lack of a framework-agnostic toolchain capable of executing pre-quantized models on a variety of hardware platforms limits their deployment at scale.

C. Quantization in Deep Learning Compilers

The emergence of deep learning compilers (hereafter referred to as DL compilers) such as Apache TVM [19], Facebook Glow [20] and Google XLA [21], has re-framed the challenge of deploying deep learning models on various hardware platforms. A DL compiler typically converts a model expressed in a framework-specific representation into a common intermediate representation (IR). The DL compiler then successively lowers the graph from the graph-level to the tensor-level. In the graph-level IR, the compiler optimizes the computation graph of the model. In the tensor-level IR, it optimizes the loop structure of tensor operators, which represent the vertices of the computation graph. After successive optimizations, the DL compiler eventually lowers the model to the machine code of a hardware platform using established low-level code generation modules such as LLVM and NVCC. Therefore, compared to deep learning frameworks, deep learning compilers are more effective at handling the multiplicity of front-ends (frameworks) and back-ends (hardware platforms), thereby simplifying the deployment of deep learning models [19][22].

However, current work on DL compilers is based mostly on the \texttt{fp32} data type. Although some compilers support the generation and optimization of quantized operators [20][23], none have focused on compiling and executing pre-quantized models. If a quantized operator is added naively to a deep learning compiler, the new operator must be added across all the IRs. In the graph-level, we need new rules for these new operators. In the tensor-level, we need new computations and possibly new kernel implementations for each platform. The effort could be mitigated somewhat by the overlap between \texttt{fp32} and quantized operator kernel implementation. Nevertheless, the naive approach to adding quantized operators to the compiler would severely limit the pace at which quantization could be applied to deep learning models.

D. Quantized Neural Network Dialect

This paper proposes QNN (Quantized Neural Network) as a graph-level IR dialect that can augment any deep learning compiler. This approach offers an end-to-end solution to read a pre-quantized model and run it across a variety of hardware platforms while reusing most of the existing DL compiler infrastructure. QNN dialect acts as a slightly higher-level IR on top of graph-level IR, specifically designed for handling quantized networks. We add new operators in QNN dialect, but we do not define any graph- or tensor-level optimizations for them. Instead, these operators are lowered to a sequence of DL compiler’s existing operators, which already have well-defined graph- and tensor-level optimizations. QNN operators represent quantization constructs at a higher level than the DL compiler’s graph-level IR, making QNN a quantization-aware IR.

QNN dialect, therefore, enables reuse of almost all of the existing infrastructure, allowing us to quickly add new hardware platforms, and to focus on kernel implementation of only those operators that are affected significantly by the integer operations (like using VNNI instructions for Intel x86). Additionally, we can define new QNN dialect optimization passes to transform the graph to suit a particular hardware platform, e.g., adding a QNN requantize operator before QNN conv2d to satisfy Intel VNNI \texttt{uint8 x int8} data type.
requirements. By reusing existing DL compiler infrastructure, QNN dialect reduces the developer efforts needed to efficiently execute pre-quantized models on many hardware platforms. We implemented QNN dialect on top of the open-source deep learning compiler Apache TVM.

Specifically, the contributions of this paper are

- **QNN Dialect.** QNN dialect, a graph-level IR dialect designed to complement deep learning compilers, enables the efficient execution of pre-quantized models on a variety of hardware platforms without cumbersome manual efforts.

- **Quantization-aware Graph Optimizations.** We augment QNN with quantization-aware graph level optimization mechanisms, enabling the graph to meet the requirements imposed by different instruction sets (like int8 x int8 for Intel VNNI).

- **Comprehensive Real System Evaluation.** We demonstrate that using QNN along with the corresponding graph optimizations, we can compile pre-quantized models from TFLite, MXNet and PyTorch on Intel CPUs, Nvidia GPUs and ARM CPUs equipped on both servers and edge devices and achieve state-of-the-art performance.

Experiments show that, with the assistance of QNN, a deep learning compiler, specifically Apache TVM, is able to take pre-quantized models defined in TFLite, MXNet and PyTorch, and execute them efficiently on different hardware platforms, with an average speedup of 2.35×, 2.15× on Intel Xeon Cascade Lake and Nvidia T4 servers, and 1.35× and 1.40× on ARM Raspberry Pi3 and Pi4 edge devices, compared to tuned TVM fp32 baseline. Generalizability aside, QNN achieves performance comparable to the best state-of-the-art solutions provided by the deep learning frameworks, while also providing better hardware platform coverage than the frameworks. To the best of our knowledge, this is the first unified effort to enable DL compilers for a comprehensive quantized deep learning models support. We have open sourced the QNN work which is also used in production.

II. PROBLEM SETTING

A. Challenges

Quantization is an essential hardware for reducing the compute and memory demand by replacing the compute data type from fp32 to lower-bit integers such as int8. There is an acute need for a software mechanism that can enable developers to take advantage of quantization *easily and rapidly with as little developer effort as possible*. However, building such a mechanism requires that we overcome three major challenges:

**Multiple Frameworks.** Developers build neural networks in the framework with which they are most comfortable. In practice today, developers in academia and industry use a variety of frameworks to produce pre-quantized models. Therefore, a good solution must be able to handle models from multiple frameworks.

**Quantization Approaches.** We briefly discussed various quantization approaches (e.g., symmetric, asymmetric, per-channel, etc.) that developers can choose according to the needs of their application. A good solution must be expressive enough to represent different types of quantization approaches.

**Multiple Hardware Platforms.** Finally, a good solution must be able to run pre-quantized models on a variety of devices across a wide range of compute capabilities. Wherever available, the solution must provide the ability to use fast integer instructions such as Intel VNNI or Nvidia DP4A instructions.

Currently, developers extend the functionality of deep learning frameworks to process quantized models. In Section [A], we argued that frameworks have tight coupling of operators and back-end hardware libraries. This leads to operators that are atomic, i.e., they are not decomposable, making it difficult to efficiently execute them on many platforms. We further substantiate this in Table I showing that frameworks have either limited quantization support or limited hardware support. Therefore, existing deep learning frameworks do not present a good solution to tackle all three challenges.

B. Observations

While the state-of-the-art framework-based approaches fail to tackle the challenges of executing pre-quantized models efficiently, the emerging crop of deep learning compilers is promising. DL compilers typically have a framework-agnostic graph-level intermediate representation (IR). We can convert a model from any framework to this IR, solving the first challenge of framework multiplicity. We can also use different types of quantization approaches in a DL compiler, which addresses the second challenge. Finally, DL compilers rely on established code generators like LLVM and NVCC to cover a broad range of hardware platforms, solving the third challenge.

However, an ideal solution must address all these challenges without burdening the developer with extra effort. Because DL compilers were originally designed to compile models in fp32 data type, they don’t support quantized operators and the corresponding optimizations. As mentioned in Section [C], simply adding new quantized operators requires a lot of effort across both graph- and tensor-level IRs. This again severely limits how rapidly we can deploy quantized models on to various hardware platforms.

| Quantization Approaches | TFLite | MXNet | PyTorch | QNN |
|-------------------------|--------|-------|---------|-----|
| Asymmetric Quantization | ✓      | ✓     |         | ✓   |
| Symmetric Quantization  | ✓      | ✓     | ✓       |     |
| Per-channel Quantization| ✓      |       | ✓       |     |

| Hardware Platforms      | TFLite | MXNet | PyTorch | QNN |
|-------------------------|--------|-------|---------|-----|
| Nvidia GPU              |        |       |         |     |
| Intel CPU               | ✓      | ✓     | ✓       |     |
| ARM CPU                 | ✓      |       |         |     |

TABLE I: Frameworks have different degrees of support for uniform int8 quantization. More importantly, they do not support all available hardware platforms with good performance. Our solution is designed to eliminate the complexity and effort of supporting all quantization approaches across a variety of hardware platforms with good performance.
In solving this problem, our key observation is that the computation of a quantized operator can be easily represented as a sequence of simpler operators (in contrast to frameworks where the quantized operators are atomic and cannot be decomposed). We illustrate this with an example of a quantized conv2d operator below, in which \( \circ \) denotes a convolution computation.

\[
C_{fp32} = A_{fp32} \circ B_{fp32} = [scale_A \ast (Q_A - zp_A)] \circ [scale_B \ast (Q_B - zp_B)] = scale_A \ast scale_B \ast Q_C
\]  
(2)

In Equation (2), \( A_{fp32}, B_{fp32} \) are input tensors and \( C_{fp32} \) is the conv2d output tensor, all in \( fp32 \) data type. We first replace the \( fp32 \) tensors with quantized tensors using Equation (1) and then expand the computation. Further, we observe in Equation (3) that quantized conv2d can be further broken down into four terms. Here, \( k, c, r, s \) and \( n, h, w \) represent output channels, input channels, filter height, and filter width respectively, and \( n, h, w \) represent batch size, output height, and output width respectively. We will show the exact sequence of operations in Section III-B.

\[
Q_C(n, k, h, w) = \sum_{c, r, s} Q_A(n, c, h + r, w + s) \ast Q_B(k, c, r, s)
- \sum_{c, r, s} zp_A \ast Q_B(k, c, r, s)
- \sum_{c, r, s} zp_B \ast Q_A(n, c, h + r, w + s)
+ \sum_{c, r, s} zp_A \ast zp_B
\]  
(3)

We observe that all the quantized operators can be easily decomposed to simpler, existing operators. In contrast, frameworks have a tight coupling between operators and backend libraries that prevents such decomposition. Although the decomposition of quantized operators increases the size of the computation graph initially, we can now reuse the graph- and tensor-level optimizations that the DL compilers provide for models in \( fp32 \) data type. For example, we can reuse the graph fusion optimization pass to find and fuse a sequence of operators because we already have the fusion rules for existing operators. Similarly at the tensor-level, we can reuse optimized kernel implementations for many simple operators like integer addition or multiplication, and rely on code generators like LLVM/NVCC, significantly reducing developer effort.

The little effort that developers do spend can be focused on the operators that need attention due to the \( \text{int8} \) data type. For example, for Intel CPUs, a developer can focus on writing graph-level optimizations to satisfy its \( \text{uint8} \times \text{int8} \) data type requirement and write kernel implementations using Intel VNNI instructions for quantized conv2d operator. Similarly, for ARMv8, one can focus only on graph- and tensor-level optimizations to use the fast \( \text{int16} \) multiply-accumulate instructions. The rest of the graph- and tensor-level optimizations can be left to the DL compiler infrastructure. Based on these observations, our solution is the Quantized Neural Networks (QNN), a graph-level dialect with quantization context that simplifies the efficient execution of pre-quantized models on a variety of hardware platforms as shown in Table I. The QNN dialect enables developers to define a quantized operator simply as a sequence of existing DL compiler operators. Additionally, it allows graph-level optimizations with quantization context to help satisfy the data type requirements imposed by the instruction sets. Therefore, augmented by QNN, DL compilers can make use of quantization across multiple hardware platforms.

III. DESIGN AND IMPLEMENTATION

In this section, we first give an overview of QNN dialect and how it fits in the existing DL compiler infrastructure, followed by the design and implementation of different QNN dialect components. We build QNN dialect on top of Apache TVM [19] - an open source deep learning compiler. We will use the TVM terminology to describe the design details with necessary explanation. TVM stack has two levels of IR - a graph-level IR called Relay [24] and a tensor-level IR (hereinafter referred to as tensor IR). QNN dialect is based on the Relay IR, allowing developers to reuse a large portion of existing TVM infrastructure.

An overview of the complete design is shown in Figure 1. A developer first adds a new QNN operator along with the description of how this operator can be lowered to a sequence of existing Relay (or graph-level) operators. Typically, QNN operators correspond to quantized operators defined in the
deep learning framework. A framework parser parses the framework model to produce a framework-agnostic graph which is the mix of QNN and Relay operators. Since QNN is a Relay dialect, QNN and Relay operators can co-exist in the same graph.

This is followed by QNN graph-level optimizations. We implement two QNN passes - QNN Legalize and QNN Canonicalize. QNN optimization passes, just like any graph-level optimization passes, allow graph transformation. However, the key difference is that QNN dialect is a quantization-aware IR, i.e. QNN operators have quantization scales, zero points and data type, which is not the case with later Relay passes. The quantization context is helpful to perform hardware-specific transformation (also known as legalization) in QNN Legalize, for example, to satisfy the data type requirements imposed by instruction set. Further, the second QNN pass - QNN Canonicalize pass - converts QNN operators into a sequence of Relay-only operators using a developer-provided sequence. Therefore, QNN Canonicalize pass acts as a boundary after which graph-level quantization context is absent.

From here on, we can reuse the existing TVM infrastructure. We first run Relay optimizations, for example, dead code elimination and graph fusion. After Relay optimizations, each fused operator is then lowered to tensor IR, where it goes through another set of tensor-level optimization passes. Here, a developer can focus on only those operators that require extra attention due to int8 data type and customize the kernel implementation for each platform. Finally, the optimized tensor IR is compiled to machine code using off-the-shelf compilers like LLVM/NVCC.

QNN is designed to reduce the developer effort by reusing a large portion of existing DL compiler infrastructure and quickly shifting the developer focus to only those items that are significantly affected by int8 data type. Figure 1 color codes the new efforts required to augment a DL compiler with QNN using black boxes - QNN operators, framework parser, QNN optimization passes and integer operator schedules.

A. QNN Operators and Framework Parsers

QNN operators act as wrappers, i.e., a developer simply defines how a QNN operator can be represented as a sequence of existing Relay operators. As a result, a developer does not have to add any loop-level tensor IR description of any new QNN operator. This developer provided sequence is used by the QNN Canonicalize pass to convert QNN operators to sequences of Relay-only operators.

In order to narrow down the set of QNN operators to support, we first collected quantized operators from the most widely used frameworks - TFLite, MXNet and PyTorch. We observed that the same operator name can mean different computation manners for different frameworks. For example, TFLite quantized conv2d operator performs int8 convolution, requantization of output tensor, ReLU and bias addition in a single operator. The quantized conv2d operator of MXNet goes one step further in aggressive fusion, fusing residual addition operations and folding batch normalization.

To address this computation boundary mismatch, we came up with suitable QNN operators to express different computations for all the mainstream frameworks and all their quantized operators. When necessary, we created finer-grain QNN operators. Essentially, one framework quantized operator can map to a sequence of one or many QNN/Relay operators. We illustrate this idea with the help of an example of conversion of TFLite quantized conv2d operator in Figure 2.

We use a sequence of QNN conv2d, Relay bias_add, Relay clip and QNN requantize operator to parse the TFLite quantized conv2d operator. We define QNN conv2d computation such that it only handles the quantized tensors and adjustments for zero points as shown in Equation (3). For scale handling, we created another QNN operator called requantize, which is extensively used in quantized models to convert one quantized tensor with some scale and zero point to another quantized tensor with another scale and zero point (more details in Section III-B).

A developer, in a similar manner, can follow the computation of a quantized framework operator and can represent it as a sequence of Relay operators with low effort. We added support for different types of quantization approaches in this manner. After the infrastructure was in place, we found that implementing weight per-channel quantization took less than a week of developer effort with QNN dialect requiring no extra work in tensor IR.

B. QNN Canonicalization Pass

Figure 1 shows how TVM stack iteratively optimizes the QNN graph after framework parsing is complete. There are two QNN optimization passes - QNN Canonicalize and QNN Legalize. Note that a developer can add more QNN optimization passes if necessary. In this paper, we discuss above two passes which we found sufficient to support a variety.
of hardware platforms. In this subsection, we discuss QNN Canonicalize. We will discuss QNN Legalize in the next section.

QNN Canonicalize pass converts QNN ops into a sequence of Relay operators using the lowering sequence defined by the developer. Therefore, QNN Canonicalize pass acts as a boundary after which graph-level quantization context is absent, and we reuse existing Relay and tensor-level infrastructure. QNN provides infrastructure where a developer can specify the lowering of a QNN operator to a sequence of Relay operators. This has to be done on an operator-by-operator basis. The difficulty of lowering varies between operators. Here, we show examples of canonicalizing three operators - QNN pooling, QNN conv2d and QNN requantize. The operators are chosen to give a flavor of complexity and share low-level observations and insights about operator designs.

**QNN Pooling Operator** - QNN pooling operator canonicalization requires simple lowering. All the framework quantized pooling operators have the same scale and zero point for pooling input and output tensors. This simplifies lowering for quantized pooling as shown below:

\[ B_{fp32} = \text{AvgPool}(A_{fp32}) \]
\[ \text{scale} \cdot (Q_B - zp) = \text{scale} \cdot \text{AvgPool}(Q_A - zp) \]
\[ Q_B = \text{AvgPool}(Q_A) \]

We can skip scale and zero point handling (as they are equal) and just perform average pooling operation. In the pooling operation, we have to be careful about rounding during division and upcast the inputs to int16 to avoid overflow/underflow while accumulation.

**QNN Convolution Operator** - As mentioned in Section III-A, we only handle convolution of quantized tensors and adjustments due to zero points (no scale handling) in QNN conv2d operator. As shown earlier in Equation 3, QNN conv2d operator can be decomposed into four terms. Each term can be represented using Relay operators. Term 1 is simply Relay conv2d over quantized int8 input tensors. Term 2 can be lowered by performing a reduce sum operation on weight tensor across c, r, s dimension. Term 3 performs a sliding window reduction on input data quantized tensor, which can be represented by pool2d, reduce sum and multiplication operator. And term 4 is just a multiplication of constants.

We have to be careful about zero points because fp32 number 0.0 is represented by zero point in the quantized tensor (which can also be inferred from Equation 1). Therefore, padding a quantized input tensor in QNN conv2d translates to padding the tensor with zero point. We also have to take care of reshapes to match tensor shapes or allow broadcasting whenever possible. We further observe that term 2 and term 4 are compile-time constants - term 2 is dependent on the weight tensor, which is constant for DNN inference. Specifically, the final QNN-to-Relay canonicalization is shown in Figure 3.

An alternative lowering can be similar to QNN pooling, where we first subtract zero points and then perform conv2d over subtracted tensors as shown in Equation 2. However, in this case the tensors have to be upcast to int16 before subtracting zero points, causing the final convolution to happen on int16 tensors instead of int8 tensors. For devices that have fast int8 datatype computation support, like Intel VNNI and Nvidia DP4A, this prevents us from using the relevant int8 instructions. However for ARMv8 that has a fast int16 multiply-accumulate instruction, this lowering gives better performance. QNN Legalize pass, described later, allows this customization for different hardware platforms.

**QNN Requantize Operator** - QNN conv2d operator is typically followed by a requantize operator (also shown in Figure 2). Requantize operator changes one quantized tensor representation to another, i.e. we represent the input quantized tensor with new scale and zero point. This can be mathematically written as follows, where \( Q_A \) and \( Q_B \) are input and output quantized tensors respectively.

\[ \text{scale}_B \cdot (Q_B - zp_B) = \text{scale}_A \cdot (Q_A - zp_A) \]
\[ Q_B = \left( \left( \frac{\text{scale}_A}{\text{scale}_B} \right) \cdot (Q_A - zp_A) \right) + zp_B \]

Note that scales here are of fp32 data type, leading to a floating point multiplication of requantize scale and quantized tensor, which later will have to be converted back to integer data type. This back-and-forth data type conversion can cause severe performance degradation. To solve this problem, we borrow the idea from TFLite requantize operation to use a fixed point multiplication as a proxy for floating point multiplication. An important detail in the implementation is the rounding of fixed point multiplication. Different frameworks choose different rounding methods, which results in minor end-to-end model accuracy differences as shown in the evaluation later.

**C. QNN Legalize Pass**

QNN optimization passes, just like Relay passes, allow graph transformations. However, the key difference is that QNN passes have quantization context, e.g., QNN conv2d operators have scale and zero points for the input tensors. The
quantization context is helpful to perform hardware-specific graph-IR transformations to satisfy the data type restrictions imposed by the hardware instruction set. We call this pass QNN Legalize pass. Legalization is a common compilation pass that transforms an IR for a specific platform to use the instructions natively supported by the platform. QNN Legalize pass allows developers to easily perform these quantization-aware platform-specific graph optimizations. Its backbone is built on existing Relay infrastructure that allows customization of graph optimization for hardware platforms.

For example, TFLite pre-quantized graphs have $\text{uint8} \times \text{uint8}$ inputs for the quantized conv2d operator. However, Intel VNNI instructions-based platforms impose $\text{uint8} \times \text{int8}$ data type requirement. QNN Legalize pass bridges this gap in a developer-friendly manner by allowing one to insert a requantize operator before the second operand of conv2d, converting the data type from $\text{uint8}$ to $\text{int8}$. For ARMv8-based devices, on the other hand, we observe that LLVM performs better code generation if the input tensors are of $\text{int16}$ datatype instead of $\text{int8}$ datatype, and utilizes fast $\text{int16}$ multiply-accumulate instruction ($\text{vmlal}$). Therefore, QNN Legalize performs a graph transformation to insert data type upcasting before both operands of the QNN conv2d operator, changing the QNN conv2d input data type to $\text{int16}$.

D. TVM Schedules for Integer Operators

As shown in Figure [1], after Relay optimization passes have been applied, each fused operator is then lowered to machine code via TVM tensor IR. For many simple operators, like addition or ReLU, that do not have any data reuse, there is not much room for further optimization in addition to relying on off-the-shelf code generators like LLVM/NVCC to get performant machine code. However, operators like conv2d or matmul (matrix multiplication) require specific tensor IR optimizations (also known as a compute and schedule implementation in the context of TVM) to efficiently exploit data reuse. This optimization effort needs to be done for every platform due to drastic architectural differences.

QNN infrastructure quickly shifts the developer focus to only those operators that need extra attention due to integer computations. For example, we can reuse existing TVM schedules for integer pooling, vector addition, ReLU etc. This is in contrast to frameworks, where a new quantized operator (which handles scale and zero points internally) need to be implemented separately. For the operators significantly affected by the integer computation, we can write specific schedules for them to utilize the fast integer instructions provide by the hardware to get desirable performance. We present our observations regarding the usage of these instructions across both server and edge devices.

**Intel VNNI** - TVM relies on off-the-shelf code generators to generate good quality code. However in some cases, it might be difficult for LLVM to use the right instructions automatically. For example, Intel VNNI instruction performs a vector dot-product of 4 $\text{int8}$ values and accumulate them into $\text{int32}$, potentially achieve 4× speedup over $\text{fp32}$ computation. However, by now LLVM is still unable to detect this macro pattern from LLVM IR to replace with proper Intel VNNI instructions. Therefore, in this case a developer can directly embed the LLVM intrinsics in the TVM tensor IR. We used this feature to write high performance TVM schedules for integer convolution operators for Intel CPUs.

**ARM Edge Devices** - In contrast to Intel VNNI, the Raspberry Pi edge devices, based on ARMv8 architecture, do not have hardware support for fast $\text{int8}$ dot product instruction. However, ARMv8 ISA has a fast $\text{int16}$ multiply-accumulate instruction ($\text{vmlal}$) that can perform dot product of 2 16-bit values and accumulate in 32-bit. We observe that LLVM picks up the $\text{vmlal}$ instructions for code generation if the input tensors are of $\text{int16}$ datatype instead of $\text{int8}$. Therefore, we use QNN Legalize pass to insert the up-casting operations before the QNN conv2d operators for ARMv8-based devices.

**Nvidia GPUs** - Similar to Intel VNNI, Nvidia has a DP4A instruction to speedup 8-bit integer computation. Recently, Nvidia has also introduced tensor cores to achieve even further speedup. In this work, we leverage the already existing Nvidia DP4A TVM schedule. Note that given TVM abstractions, in future, a developer can just focus on the TVM schedule for convolution using Tensor Cores, and easily replace the DP4A schedule with the new schedule. Writing TVM schedule using Tensor Core is beyond the scope of this paper.

Overall, QNN is designed to augment DL compilers, in our case, Apache TVM, to deploy pre-quantized models efficiently across many hardware devices with low developer effort. In cases where we need extra attention due to specific integer instructions, QNN can still reduce a significant portion of developer’s time and effort by reusing the existing TVM infrastructure.

IV. Evaluation

This section evaluates our proposed QNN solution by answering the following questions:

1) As a sanity check, is QNN able to compile pre-quantized models to achieve similar model accuracy numbers compared to the framework solutions?

2) What is the performance of QNN-compiled pre-quantized models, in comparison to the original models in $\text{fp32}$?

3) Can QNN get the on-par, if not better, performance on pre-quantized models compared to the framework solutions while covering more hardware platforms than frameworks?

4) How does QNN perform in compiling a newly designed pre-quantized model?

A. Experimental Setup

**Frameworks.** We evaluate QNN across all the available pre-quantized models in TFLite (version 1.13) [25], MXNet (version 1.6) [26], and PyTorch (version 1.4) [27]. We implement QNN on top of open-source Apache TVM (version 0.6) [19]. Note that different frameworks support different sets of pre-quantized models as listed in Table [1], while QNN-augmented TVM is able to compile all of them.

**Server Platforms.** We evaluate QNN on two server platforms on Amazon EC2 - Intel 24-core Xeon Cascade Lake CPU equipped at EC2 C5.12xlarge instance and Nvidia T4 GPU equipped at EC2 C5.12xlarge instance and Nvidia T4 GPU equipped at EC2 C5.12xlarge instance and Nvidia T4 GPU equipped at EC2 C5.12xlarge instance and Nvidia T4 GPU.
TABLE II: QNN achieves accuracy parity across all the mainstream frameworks – MXNet, TFLite and PyTorch – pre-quantized models.

| Quantized Model | Baseline Top1 Accuracy (%) | QNN-TVM Top1 Accuracy (%) | Baseline Top5 Accuracy (%) | QNN-TVM Top5 Accuracy (%) |
|-----------------|---------------------------|---------------------------|---------------------------|---------------------------|
| ResNet-18       | 69.76                     | 69.86                     | 89.02                     | 89.05                     |
| ResNet-50       | 76.13                     | 76.16                     | 92.6                      | 92.73                     |
| ResNet-50-v1b   | 76.66                     | 76.56                     | 92.6                      | 92.6                      |
| ResNet-101      | 77.13                     | 76.97                     | 93.06                     | 93.09                     |
| ResNet-152      | 75.99                     | 75.75                     | 92.52                     | 92.12                     |
| Inception-v3    | 77.84                     | 77.28                     | 93.52                     | 93.32                     |
| Inception-bn    | 71.96                     | 71.79                     | 90.38                     | 90.25                     |
| MobileNet-v1    | 71.27                     | 71.13                     | 90.09                     | 90.16                     |
| MobileNet-v2    | 70.35                     | 70.14                     | 89.45                     | 89.52                     |

Edge Devices. We evaluate QNN on two popular edge devices - Raspberry Pi3 (in-order ARM Cortex A53) and Raspberry Pi4 (out-of-order ARM Cortex A72). In contrast to our server platforms, Raspberry Pi devices do not have any fast `int8` computation instructions. Instead, they have 16-bit multiply-accumulate instructions (`vmlal`) that leads to better data packing in registers.

B. Deploying QNN across Frameworks

First of all, we evaluate the effectiveness of QNN in achieving a wide framework coverage. Since each framework has its own preferred choice of quantization approach (asymmetric, symmetric, per-channel), we simultaneously evaluate the ability of QNN to represent different quantization approaches. Specifically, we compare the accuracy of pre-quantized models achieved by the frameworks and QNN-augmented TVM stack. We measure the accuracy over 10k images from the ImageNet validation dataset [28] and show the findings in Table II.

We observe that QNN achieves accuracy parity for all pre-quantized models across the frameworks with minor differences. As explained in Section III-B, these differences mainly attribute to the rounding operations in fixed point multiplication of the requantize operator. Different frameworks use different rounding methods, leading to small differences in final accuracy.

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| ResNet-152            | 75.99                     | 75.75                     | 92.52                     | 92.12                     |
| Inception-v3          | 77.84                     | 77.28                     | 93.52                     | 93.32                     |
| Inception-bn          | 71.96                     | 71.79                     | 90.38                     | 90.25                     |
| MobileNet-v1          | 71.27                     | 71.13                     | 90.09                     | 90.16                     |
| MobileNet-v2          | 70.35                     | 70.14                     | 89.45                     | 89.52                     |

Fig. 4: QNN on Server - QNN takes advantage of fast `int8` instructions to achieve significant speedup against TVM `fp32` tuned baseline for both Intel Cascade lake and Nvidia T4 servers.

Fig. 5: QNN at edge - QNN enables easy deployment across the edge devices as well. We see performance speedup for both in-order (A53) and out-of-order (A72) ARM cores. The red cross shows that `fp32` resnet-152 model execution was out of memory, while QNN `int8` execution succeeded.

C. Deploying QNN Across Server and Edge Devices

QNN is designed to enable efficient deployment of pre-quantized models across a variety of hardware platforms with different types of computing capabilities. In this subsection, we evaluate QNN effectiveness in performance speedup and memory footprint reduction, when it is deployed across our server and edge devices.

Performance Improvements. In this experiment, we compile the original MXNet models (in `fp32`) and their counterpart pre-quantized model (in `int8`) using QNN-augmented TVM stack. We execute each compiled model for 2000 images (batch size 1) and measure the average end-to-end latency. We also perform auto-tuning [29] to ensure high performance for both original and pre-quantized models.

We compare the performance of TVM-compiled original models (referred to as TVM-`fp32`) and QNN-augmented TVM-compiled MXNet pre-quantized models (referred to as QNN-`int8`). There are two reasons for choosing this baseline. First, no framework can run across all the platforms we are targeting, making TVM-`fp32` a good baseline. Second, MXNet has the largest number of available pre-quantized models amongst all the frameworks, enabling wider model coverage evaluation. The same observation applies to pre-quantized models of TFLite and PyTorch. We present the results for server-class platforms and edge-devices in Figure 4 and Figure 5 respectively. We observe very low standard deviation amongst 2000 runs, and therefore omit the error bars in the barplots.
For servers, we observe significant performance improvements for both Intel Cascade Lake CPU and Nvidia T4 GPU servers as shown in Figure 4. Both processors have support for fast int8 dot-product operations - Intel VNNI and Nvidia DP4A instructions. We also observe lower than expected speedup for resnet-152 and mobilenet models. For resnet-152, MXNet decided to keep the batch normalization operator in fp32 to retain accuracy, causing frequent data type conversions and hurting performance. For mobilenet models, TVM stack currently lacks good depthwise convolution schedules (kernel implementation) using fast int8 instructions. Overall, we observe that QNN-int8 achieves an average speedup of 2.35× and 2.13× for Intel Cascade Lake CPU and Nvidia T4 GPU respectively compared to TVM-fp32.

Similarly for edge devices, we observe significant speedups as shown in Figure 5. In contrast to servers, our edge devices do not have fast int8 instructions, leading to lower speedups than observed in servers. However, these devices have fast int16 multiply-accumulate instructions (vmlal). We observe that LLVM generates highly vectorized and vector register-packed code using vmlal instructions, efficiently utilizing convolution data reuse and achieving better performance than fp32 models. Additionally, we observe that TVM-fp32 resnet-152 model goes out of memory due to large weight size in Pi3 (shown by cross in the figure). QNN-int8 on the other hand, due to smaller memory footprint, can execute the model. Similar to servers, mobilenet models observe sub-optimal performance due to the lack of good TVM schedules for depthwise convolution operator. Overall, QNN-int8 achieves an average speedup of 1.35× and 1.40× for ARM Raspberry Pi3 and Pi4 respectively compared to TVM-fp32.

Note that, although mobilenet models show lower than expected performance speedup, QNN allows developers to just focus on implementing better TVM schedules for depthwise convolution operator, while reusing the existing TVM infrastructure for both graph- and tensor-level optimizations, enabling rapid deployment with less developer efforts.

**Memory Footprint Reduction.** In this experiment, we evaluate QNN effectiveness in reducing the runtime memory footprint. We compare the total runtime memory footprint for TVM-fp32 and QNN-int8 models for all the hosted MXNet models across all hardware platforms. We present the findings in Figure 6 showing QNN-int8 total memory footprint as a percentage of total TVM-fp32 footprint. We also break down total memory footprint into 2 categories - weights (also known as parameters) and intermediate feature maps (also known as activations or intermediate outputs). In contrast to prior works that only show weight memory footprint reduction [11,14], we analyze total memory footprint.

We observe that different models have different memory footprint reduction depending on the contribution of intermediate feature maps to total memory footprint. As opposed to weights that have been pre-quantized to int8 and achieve close to 4× memory footprint reduction, the intermediate features maps that can also be in int32 data type, observe less than 4× memory reduction. For example, mobilenet models have larger contribution of intermediate feature maps, overall reducing the footprint to 33% (or 3× footprint reduction).

We also observe that in edge devices, weights of QNN-int8 see only 50% memory footprint reduction (much less than expected 75% or 4×). This is because we upcast the weights to int16 to use ARM fast int16 multiply-accumulate vmlal instruction. Note that this overhead is unavoidable. TVM stack runs a constant evaluation pass that converts the int8 pre-quantized weights to int16 at compile-time. If we disable constant evaluation optimization pass and keep the weights in int8, the tensor with upcast weights in int16 datatype will still be the part of total memory footprint, still keeping the total memory footprint same. Therefore, we measure total memory footprint to accurately assess the total memory footprint reduction.

**D. QNN Comparison with Frameworks**

Next, we compare the performance between QNN and frameworks of executing pre-quantized models. As shown in Table 3 frameworks do not have efficient pre-quantized model execution support for all hardware platforms. Therefore, we execute all the hosted pre-quantized models for each framework on the hardware platforms it supports, and compare the performance with the same models compiled and executed by QNN-augmented TVM. Therefore, this evaluation compares our work against the best available baseline. We do not show
We found that PyTorch does not use multiple threads for QNNPACK on non-Android or iOS devices including Raspberry Pi4. Therefore, we show comparison with TVM single thread performance in addition to TVM four threads performance. We observe that, similar to our findings with TFLite, there is room of improvement for better ARM sched-
is the fp32 int8 augmented TVM (QNN-ARM Cortex A53 (Raspberry Pi3) edge device using QNN-to quantize the model and then compiled the model for simultaneously. we can co-execute other applications on the same device low latency and resource utilization for this model so that capture the keywords. Therefore, it is imperative to have both these models are executed very frequently on the device to specific keywords or triggers in human speech. Typically, model is an in-house built keyword detection model, which and execute a new unseen pre-quantized model. Our new E. QNN Effectiveness on a New Model

Lastly, we present a scenario where we use QNN to compile and execute a new unseen pre-quantized model. Our new model is an in-house built keyword detection model, which is executed on a resource-constrained edge device, to detect specific keywords or triggers in human speech. Typically, these models are executed very frequently on the device to capture the keywords. Therefore, it is imperative to have both low latency and resource utilization for this model so that we can co-execute other applications on the same device simultaneously.

To reduce the latency, we employed framework quantization to quantize the model and then compiled the model for ARM Cortex A53 (Raspberry Pi3) edge device using QNN-augmented TVM (QNN-int8). For evaluation, our baseline is the fp32 model compiled and executed via TVM (TVM-fp32). We observe that, without any extra developer efforts, QNN-int8 was 2.0× and 2.7× faster than TVM-fp32 for single-threaded and multi-threaded execution (4 threads), while achieving 50% total runtime memory footprint reduction and no accuracy loss. This shows that a QNN-augmented deep learning compiler is effective in rapidly deploying new models on new devices with low developer efforts.

V. RELATED WORK

8-bit Integer Quantization. 8-bit integer quantization is the most widely adopted quantization technique because of prevalence of int8 data type computation support in the commodity hardware platforms. 8-bit integer quantization has also been shown to retain model accuracy with relatively less efforts compared to more aggressive quantization. TFLite 8-bit integer quantization, designed primarily for ARM-based edge devices, was one of the first large-scale effort and set the industry standard for integer quantization [33]. There is a large body of prior work to retain model accuracy for quantization, which can be broken into two categories - Post-training quantization and Quantization-aware training [11][14][35]. Post-training quantization starts from an already trained fp32 model and uses calibration on a cross-validation dataset to find suitable quantization parameters [34][35]. Research has shown that post-training quantization achieves good accuracy for 8-bit quantization. More aggressive quantization requires quantization-aware training. Our approach can leverage all of these research to get a pre-quantized model, and eases its deployment on many hardware platforms.

Deep Learning Frameworks. Deep learning frameworks, like Tensorflow, PyTorch and MXNet, have been at the forefront of deep learning revolution. These frameworks rely on pre-built backend hardware libraries for high-performance machine code - Intel DNNL [36], Nvidia CuDNN [9] and ARM ACL [37]. These backend libraries have hand-optimized kernel implementations to achieve high performance on different platforms. Most of these frameworks use int8 quantization to support lightweight model inference on commodity hardware. A user also has a choice of using symmetric, asymmetric or per-channel quantization approaches to find a suitable performance-accuracy tradeoff. However, as shown in Table I frameworks are not well suited to deploy the models across many hardware platforms. QNN dialect is designed to leverage the extensive work done by the frameworks in quantizing the models and retaining accuracy, and solve the challenges to ease the deployment of pre-quantized models on many platforms with low developer efforts.

Deep Learning Compilers. Deep learning compilers have gained popularity in past few years to design a flexible approach for optimizing and deploying deep learning models. Some of the DL compilers support optimization and code generation for multiple hardware platforms - Apache TVM [19], Glow [20] and XLA [21]. On the other hand, there are compilers focusing on only one class of hardware platforms - Intel nGraph [38], ARM NN [39] and Nvidia TensorRT [9][40]. There has also been recent efforts in improving the compiler design for supporting deep learning hardware accelerators, for example, in Apache TVM [19], Glow [20], PlaidML [41] with stripe IR [42] and MLIR [43]. Quantization support in deep learning compilers has picked up pace very recently and therefore good support is limited to the compilers focusing on a single class of hardware platform - nGraph, TensorRT and ARM NN. This limitation prevents us from rapidly deploying models on many platforms with single unified toolchain. Our work on the QNN dialect is designed to complement the existing DL compilers to solve this challenge. We observe that QNN-augmented DL compiler compiles pre-quantized models from multiple frameworks, supports different types of quantization approaches and enables deployment on many hardware platforms with low developer efforts.

VI. CONCLUSION

In this paper, we offer a universal solution to the challenge of efficiently executing pre-quantized models from a variety of frameworks across a variety of hardware platforms while keeping developer effort low. We note that most deep learning frameworks help developers quantize models but fall short at supporting the efficient execution of models on multiple platforms. This is due to the tight coupling of framework operators and back-end hardware libraries, which hinders the use of quantization. We tackle the problem using the notion of a deep learning compiler enhanced with a new graph-level dialect called Quantized Neural Network (QNN). The QNN dialect provides a quantization context that can augment any existing deep learning compiler (e.g. Apache TVM, Glow, XLA). QNN simplifies the effort of efficiently executing pre-quantized models on variety of hardware devices. We observe that our QNN-augmented deep learning compiler achieves speedups of 2.35×, 2.15×, 1.35× and 1.40× on Intel Xeon Cascade Lake CPUs, Nvidia Tesla T4 GPUs, ARM Cortex-A CPUs on Raspberry Pi3 and Pi4 respectively relative to fp32 execution. QNN also achieves comparable performance against the state-of-the-art framework’s solutions for executing
pre-quantized models while providing much better coverage of hardware platforms.

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