A Simple Picosecond Pulse Generator Based on a Pair of Step Recovery Diodes

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Abstract—A picosecond pulse generator based on a pair of step recovery diodes (SRD), leveraging the transient response of the SRD PN junction and controlling the pulse width by a resistor, is proposed. We first explain the operation principle of the device, decomposing the pulse generation into different phases, and then demonstrate an experimental prototype with two different resistance, and hence pulse width, values.

Keywords—UWB pulse generator, real-time analog signal processing (R-ASP), step recovery diode (SRD)

I. INTRODUCTION

The emerging Real-time Analog Signal Processing (R-ASP) technology [1], using dispersion-engineered structures (analog signal processors) providing specified group delays versus frequency responses for processing high-frequency and widebandwidth signals in real time, may lead to novel low-cost and low-complexity radio systems [2] for future millimeter wave and terahertz wireless communications.

Analog signal processors usually deal with ultra-short pulses with very rich spectral contents. Such pulses may be generated by different techniques [3]. Among them, the step recovery diode (SRD) approach [4]–[6] features simple circuit design, while providing picosecond pulse generation capability. Conventional SRD-based pulse generators usually employ an SRD to generate a pulse with picosecond rising edge, which destructively interferes with its opposite-polarity delayed replica produced by a short-circuited stub, which results in a short pulse whose width is equal to the round trip time along the stub. However, the stub configuration suffers from spurious reflections in both forward and backward directions, whose suppression requires pulse shaping networks [7], and requires complicated tuning schemes [7].

In this paper, we propose a stub-less pulse generator based on a pair of SRDs, which is immune of spurious reflections and which provides flexible control of the pulse width via a simple resistance.

II. PRINCIPLE

The transient behaviour of a PN junction in response to a step voltage from the forward to the reverse bias regimes is shown in Fig. 1. Initially, the PN junction is forward biased with current $i_F$. When the voltage $v_t$ reverses polarity, the junction is not switched off immediately, but rather takes time $\tau_1$ (storage phase), with current $i_{R,\text{transient}}$, to neutralize the charges stored in the depletion region and progressively raise the junction barrier [8]. Note that during the whole storage phase, the junction maintains low resistance, and almost constant junction voltage, i.e. $v_j \approx V_T$. Near the end of the storage phase, the raising junction barrier increases the resistance, finally switching off the junction for a decay time $\tau_2$ (decay phase), which is extremely short (in picosecond range) for an SRD [8]. Assuming constant $i_F$ and constant $i_{R,\text{transient}}$, the storage phase time is given by [8]

$$\tau_1 = \tau_L \ln \left(1 + \frac{i_F}{i_{R,\text{transient}}}ight),$$

where $\tau_L$ is the minority carrier lifetime. We shall next present our pulse generator based on this SRD transient physics.

Figure 2 shows the schematic of the proposed SRD-pair pulse generator. The generator is triggered by the rising edge of the input voltage through PN diode D1, that is always ON for blocking possible negative input voltages. Its core is the parallel connection of SRDs D2 and D3, biased at their cathode by DC $V_s < 0$ through $R_1$ current limiter, with $R_2$ controlling the pulse width, as will be shown later. Finally, Schottky diode D4, operates as a pulse formation switch. The resistor $R_0 = 50 \Omega$ ensures input matching during the pulse production. Assuming square-wave (0-2.5 V) excitation $v_1$, the operation may be decomposed into 5 phases, shown in Fig. 3.

- Phase 1 ($t < t_1$): D2 and D3 are forward biased, and
D4 is off. The excitation $v_1$ is close to 0 V, so the D2 and D3 forward currents are such that $i_{RD2} \gg i_{RD3}$ due to the existence of $R_2$ in the D3 loop. The junction voltages $v_{LD2} = -v_2$ and $v_{LD3} = v_3 - v_2$, where $v_3 < 0$ due to the current flowing in $R_2$ from the ground to node 3, so that D4 is off and $v_4 = 0$.

- Phase 2 ($t_1 < t < t_2$): D2 is in storage regime, D3 is still forward biased, and D4 is still off. The excitation $v_1$ starts rising, driving D2 ($i_{RD2} > 0$) into storage regime before D3 due to the smaller resistance in the D2 current loop than that in the D3 one and hence faster current changing rate ($\frac{\partial i_{D2}}{\partial t} > \frac{\partial i_{D3}}{\partial t}$) in response to the rising edge of $v_1$. According to Fig. 2, $v_{D2} = -v_2$ varies only slightly in storage regime, and $v_3 < 0$ because D3 is still forward biased, and hence keeping D4 off.

- Phase 3 ($t_2 < t < t_3$): D2 and D3 are both in storage regime, D4 is still off. The voltage $v_1$ eventually also drives D3 into storage regime ($i_{RD3} > 0$). Since $i_{RD2}/i_{RD2} \ll i_{RD3}/i_{RD3}$, we have $\tau_{D2} < \tau_{D3}$ according to (1), and therefore D2 will switch off before D3. In the meanwhile, $v_3$ follows $v_2$, with insufficient variation to switch D4 on.

- Phase 4 ($t_3 < t < t_4$): D2 is off, D3 is still in storage regime, D4 is on. The SRD D2 abruptly switches off at $t_3$, while D3 remains in storage regime. Consequently, $v_2$, and following $v_3$, abruptly increase, which switches D4 on, and therefore generates at the output the rising edge of $v_4$. Moreover, the off-switching of D2, and the on-switching of D4, which makes $R_0$ parallel to $R_2$, together boost $i_{RD3}$, starting to shorten the D3 storage time, which would otherwise be longer as expected in Phase 3.

- Phase 5 ($t > t_4$): D2, D3, D4 are all off. The D3 storage phase suddenly ends at $t_4$, nullifying $i_{RD3}$ and $v_3$, and hence switching D4 off, which results in the falling edge of $v_4$.

When the input level goes back to zero, the generator returns to the regime of Phase 1, waiting for the next voltage step to resume the aforementioned pulse formation cycle.

Let us now examine the factors determining the pulse width. Equation (1) assumes constant $i_{RD,transient}$ over the entire storage phase $\tau_{L}$. As explained above, the storage phase for D3 is from $t_2$ to $t_4$. However, since $i_{RD3}(t_2 < t < t_3) \ll i_{RD3}(t_3 < t < t_4)$, the storage time essentially reduces to the interval $[t_3, t_4]$, and $i_{RD,transient}$ in (1) should be replaced by $i_{RD3}(t_3 < t < t_4)$ for the effective storage time of D3. Since this interval $(t_3, t_4)$ corresponds to the pulse duration, this duration can be approximated as

$$T \approx \tau_L \ln \left[ 1 + \frac{i_{RD3}}{i_{RD3}(t_3 < t < t_4)} \right]. \quad (2)$$

with an accuracy that is proportional to $i_{RD3}(t_2 < t < t_3)$ and hence inversely proportional to $R_2$, i.e. the closer $i_{RD}$ to zero in the interval $[t_2, t_3]$ (associated with larger $R_2$), the better the accuracy, as will be shown later in Fig. 4(a). Using Ohm's law, we can write

$$i_{RD} = \frac{V_s - V_L}{R_L}.$$ 

**Table I: Diodes used in the generator with reference to Fig. 2**

| Notation | Model                  |
|----------|------------------------|
| D1       | Avago Tech. HMPS-2822  |
| D2       | Aerolox MNDB30-0805    |
| D3       | Aerolox MNDB30-0805    |
| D4       | Skyworks SMS7630-061-0201 |

**Table II: Resistors used in the generator with reference to Fig. 2**

| Notation | Resistance (Ω) |
|----------|----------------|
| R1       | 25             |
| R2       | 50             |
| R0       | 10             |

**Table III: Capacitors used in the generator with reference to Fig. 2**

| Notation | Capacitance (µF) |
|----------|------------------|
| C1       | 100              |
| C2       | 100              |

**Table IV: Inductors used in the generator with reference to Fig. 2**

| Notation | Inductance (µH) |
|----------|-----------------|
| L1       | 10              |
| L2       | 10              |

**Fig. 2: Proposed SRD-pair pulse generator.**

**Fig. 3: Circuit simulated (a) currents (polarities referred to current directions indicated in Fig. 2) and (b) voltages, with $V_s = -3.5$ V, $R_1 = 25$ Ω, $R_2 = 50$ Ω, and Spice models for the diodes in Table I.**
law, one may further write Eq. (2) in the form
\[
T \approx \tau_L \ln \left( 1 + r \frac{R_2}{R_1} \right) = \tau_L \ln \left( 1 + r \frac{R_L}{\frac{R_2}{R_1} + R_L} \right),
\]
where \( r \) is the ratio of \( v_3 \) in the forward bias regime to \( v_3 \) in the \([t_3, t_4]\) interval. Equation (3) reveals that, for given \( R_L \), one may adjust \( R_2 \) to control the pulse width. This is confirmed by the simulation result in Fig. 4(a), which also show the result for the approximation in (2). Finally, Fig. 4(b) plots the pulse magnitude, which is seen to be essentially flat versus \( R_2 \).

![Fig. 4: (a) Circuit simulated half-magnitude pulse width (solid blue) and calculated pulse width (dash red) by Eq. (2) (with simulated currents and \( \tau_L = 3 \text{ ns} ) \) versus \( R_2 \). (b) Circuit simulated pulse magnitude.](image)

**III. EXPERIMENTAL DEMONSTRATION**

Figure 5 shows the fabricated prototype, whose diode models are listed in Table I, and where \( R_1 \) consists in two 0805 150 \( \Omega \) resistors in parallel, \( R_0 \) is a 0603 50 \( \Omega \) resistor, and \( R_2 \) is a 0603 50 or 560 \( \Omega \) resistor. The experimental results are shown in Fig. 6 (solid red). The half-magnitude pulse widths are 94 and 62 ps for \( R_2 = 50 \Omega \) and 560 \( \Omega \), respectively, which are different from the corresponding simulation pulse widths in Fig. 4(a). Ranging tails are also observed. To understand the cause of the pulse width discrepancy between simulation and experiment and the experimental ranging tails, one should note that the transmission line lengths are assumed to be zero in Fig. 2 and in the corresponding simulation results in Fig. 3 and Fig. 4. However, in the fabricated prototype, nonzero-length transmission lines delay the multiple internal reflections between diodes, which are not perfectly matched, hence generating successive replicas of the intended output pulse corresponding to the ringing tail. Moreover, the spurious pulses may constructively or destructively interfere with the main one, resulting in wider or shorter pulse width compared to the simulated on in Fig. 2(a). One may confirm this explanation by including finite-length transmission lines in the simulation circuit, as shown by the dash-blue curves in Fig. 6. In practice, one may naturally improve the output pulse shape by enhancing the matching of the diodes and using the shortest possible interconnecting lines.

**IV. CONCLUSION**

A simple pulse generator based on a pair of SRDs with pulse width adjustable by a single resistor is presented, analyzed and

![Fig. 5: Experimental prototype.](image)

![Fig. 6: Experimental (solid red) and circuit simulation (with finite-length transmission lines) (dash blue) results corresponding to (a) \( R_2 = 50 \Omega \) and (b) \( R_2 = 560 \Omega \), \( V_s = -3.5 \text{ V} \) and \( v_i = 0/2.5 \text{ V} \).](image)

experimentally demonstrated. Such a pulse generator may find wide applications in R-ASP and other UWB radio systems with low cost and low complexity.

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