GaN is an ideal material for many optoelectronic and power devices due to its advantageous properties, including a 3.4 eV direct bandgap, high switching speeds, low switching losses, and high breakdown voltage. Several transformative devices, such as the blue LED, have been enabled by GaN and its alloys. Moreover, bulk GaN and homoepitaxial GaN on bulk GaN substrates have become available and are used due to their high crystallographic quality, low defect densities, and inherent advantages in a vertical device design topology compared to lateral devices for high blocking voltages. The most readily achievable method of selective doping is via ion implantation and activation. Previous investigations of ion implantation and activation in GaN have focused on heteroepitaxially grown GaN on sapphire. In all, dopants have been activated, including AlN, SiO₂, MgO, and graphite. Amongst these capping materials, AlN has shown the most promise. Previous capping studies of GaN have all focused on the capping of heteroepitaxial GaN thin films (mostly MOCVD-grown GaN on sapphire substrates). Heteroepitaxial GaN and bulk GaN have key differences that can affect the structural properties of the capping layer. Heteroepitaxial GaN grown by MOCVD on sapphire substrates has been previously shown to be in tension due to island coalescence. In MOCVD-grown GaN, the density of dislocations and low angle grain boundaries is usually higher than in bulk HVPE-grown GaN. Additionally, bulk GaN substrates are polished with extremely smooth epitaxial surfaces while high quality MOCVD-grown heteroepitaxial GaN typically have growth steps that result in a slightly rougher surface. In this research, the challenges of capping bulk GaN for high temperature processing are investigated for the first time.

Experimental

In this study, we develop an improved capping process utilizing sputtered AlN encapsulants to protect bulk GaN surfaces during high temperature rapid thermal annealing. The AlN encapsulants investigated include films sputtered at a substrate temperature of 400°C (HT) and 20°C (RT). All caps were 250 nm thick and deposited on both sides of each substrate. The thickness of the capping layers was chosen based on a previous investigation where 250 nm of sputtered AlN enhanced the strength of a 30 nm MOCVD-grown AlN cap. The spurring conditions for the capping layers investigated in this research are shown in Table I. Ga and N-polar bulk GaN substrates were studied in this research for both HT and RT spurring regimes.

Annealing was performed in a custom processing chamber utilizing the multicycle rapid thermal annealing (MRTA) process. The MRTA process has been shown to successfully activate ~8% of implanted Mg in GaN, and includes a moderate nitrogen overpressure of 24 bar, an AlN capping structure, a conventional anneal to reverse some of the implantation damage, and rapid heat pulses to avoid decomposition while activating the dopants. The initial conventional anneal portion of the MRTA process was performed at 1080°C for 30 minutes based on previous optimization studies. The rapid heating pulse portion of the MRTA process consisted of 20 pulses with maximum pulse temperature of 1400°C. The duration of each pulse, which is defined as the time spent above the conventional annealing temperature, was 16 seconds.

Sputtered AlN capping layers deposited at different temperatures were compared for their efficacy in protecting bulk GaN substrates during high temperature annealing. AlN sputtered at a substrate temperature of 400°C on the epi-ready surface of bulk GaN cracked due to the strain associated with the lattice mismatch between AlN and GaN. AlN caps sputtered on the rougher optically-polished surface did not crack due to strain relief that results from polishing damage. During heating pulses with a maximum temperature of 1400°C, the exposed GaN in the cracked regions was damaged due to GaN decomposition. In contrast, AlN capping layers deposited at room temperature did not exhibit cracking since this condition energetically prevents the AlN from orienting to the GaN surface and forming cracks. Even after 20 rapid heating cycles with a maximum temperature of 1400°C, the GaN surface remains very smooth (0.70 nm RMS) over a 350 μm × 260 μm area. The ability to anneal bulk GaN at high temperatures without surface degradation during the AlN cap developed herein is a critical processing step that will enable planar processing for future vertical III-nitride devices.

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Table I. Sputtering conditions for the two capping layers investigated in this research.

| Condition                | 400°C AlN Cap | Room Temperature AlN Cap |
|--------------------------|---------------|--------------------------|
| Ar Flow (sccm)           | 21            | 21                       |
| N₂ Flow (sccm)           | 4             | 4                        |
| Pressure (mTorr)         | 3             | 3                        |
| Substrate Temperature (°C)| 400           | 20                       |
| Power (W)                | 100           | 100                      |
| Thickness (nm)           | 250           | 250                      |
| Deposition Rate (nm/min) | 4             | 4.2                      |

graphite susceptor. The temperature was monitored during annealing using a pyrometer, which was calibrated using a Si melt test. During annealing, the ambient in the chamber was 24 bar of nitrogen overpressure.

Samples were characterized before and after capping and annealing. The surface morphology was investigated using a Zygo optical profilometer, a Bruker Dimension FastScan atomic force microscopy (AFM) system, and differential interference contrast imaging (DIC). Crystallographic orientation was characterized using a Rigaku ATX-E X-ray diffraction (XRD).

Results and Discussion

The surface morphology of the as-received epi-ready surface of the bulk substrates was smooth as shown in Fig. 1 with a root mean squared (RMS) roughness of 0.18 nm. The opposite side of the bulk GaN substrate was optically-polished and was much rougher, with clear polishing damage, as shown in Fig. 2, with an RMS roughness of 2.93 nm.

After sputtering 250 nm of AlN at 400 °C on both sides of the sample, the epi-ready surface is significantly changed, with severe cracking and an RMS roughness of 1.41 nm as shown in Fig. 3. An additional scan focused on the crack reveals that the crack is over 150 nm deep as shown in Fig. 4. The lattice mismatch of AlN and GaN is 2.4%, which is expected to cause tensile strain in the AlN film. It has been reported that this lattice mismatch has resulted in cracking related to tensile strain relaxation in only 7 nm of AlN grown on GaN, which is significantly thinner than the AlN layers deposited on GaN investigated in this research. Thus, the cracking exhibited by the high temperature sputtered layers on bulk GaN is attributed to the lattice mismatch between AlN and GaN. Similar cracking was observed on thinner films (40 nm) as well.

![Figure 1. AFM image of the as-grown epi-ready surface of a bulk N-polar GaN substrate. The surface is smooth with a 0.18 nm RMS roughness.](image1)

![Figure 2. AFM image of the as-grown optical-polished Ga-polar surface of a bulk GaN substrate, which is significantly rougher than the epi-ready surface with an RMS roughness of 2.93 nm.](image2)

![Figure 3. AFM image of the epi-ready N-polar bulk GaN surface with 250 nm AlN sputtered at 400°C.](image3)

![Figure 4. AFM image zoomed in on a crack in the N-polar epi-ready surface with 250 nm AlN sputtered at 400°C. A line scan (inset) indicates that the crack is at least 150 nm deep.](image4)
Interestingly, the AlN film sputtered at 400 °C on the rougher optically polished surface does not exhibit cracking and has nearly the same roughness as before sputtering as shown in Fig. 6 with an RMS roughness of 2.27 nm. It was determined previously that when AlN is sputtered on surfaces with varying roughness, the stress can vary considerably and thus cracking can be reduced on a rough surface.26 Thus, the lack of cracking on the rougher optically-polished side of the bulk GaN substrate can be attributed to strain relief from the polishing damage.

The strain associated with this lattice mismatch was investigated on both the cracked epi-polished surface and the uncracked optically-polished surface by XRD as shown in Fig. 7. The epi-polished surface, which exhibited cracking, is strained as seen by the higher angle shift in the AlN (002) peak. This suggests tensile stress due to the lattice mismatch between GaN and AlN. The (002) peak of the AlN deposited on the epi-polished surface can be accurately fit (R^2 = .997) using two Voigt peaks centered at 36.09 and 36.16 degrees. The peak at 36.09 degrees is attributed to the strain relaxed AlN in close proximity to the cracks. The higher angle peak at 36.16 degrees is attributed to more highly strained AlN located further away from the cracks. AlN deposited using the same sputtering conditions on the optically-polished surface of the bulk GaN substrates exhibits only a single AlN (002) peak shifted to a lower angle. The (002) peak of the AlN deposited on the optically-polished surface can be accurately fit (R^2 = .984) using a single Voigt peak centered at 36.06 degrees, indicating that the roughness or the surface crystalline damage of the optical polish relieves the epitaxial strain, in agreement with previous investigations of sputtered AlN on surfaces with varying surface roughness.26 The intensity ratio of the AlN (002) peaks and AlN (101) peaks shown in Fig. 7 additionally suggest that the AlN sputtered on the epi-polished surface at 400 °C has a higher degree of c-axis orientation compared to the AlN sputtered on the optically-polished surface.

After characterizing the as-deposited 400 °C AlN cap, the capped GaN substrates were subjected to the MRTA process consisting of 20 pulses with maximum pulse temperature of 1400 °C as described in the Experimental section. After annealing, the GaN was badly damaged as shown by the DIC image in Fig. 8. The bare GaN surface, which is no longer protected beneath the cracked AlN areas, is severely damaged. This damage is due to GaN decomposition in these uncapped regions, which will introduce compensating dopants for Mg-implanted GaN.27 Thus, to implant and activate implanted dopants in bulk GaN, an uncracked cap that protects the GaN surface is required.
In an attempt to inhibit strain-related cracking in the AlN layer during deposition, a room temperature sputtered AlN cap was investigated. It was hypothesized that by decreasing the substrate temperature, the AlN would not have sufficient energy to preferentially orient to the GaN surface and form cracks due to lattice mismatch induced strain. Just like the 400 °C cap, a 250 nm AlN cap was sputtered on both sides of a sample. After sputtering, the AlN cap on the epi-ready surface is smooth, without cracks or pinholes, as shown in Fig. 9. Cracks and pinholes have been previously shown to result in decomposition of the underlying GaN.16,17 After sputtering, the epi-ready surface has an RMS roughness of 0.47 nm. This is a slight increase in roughness compared to the as-polished epi-ready surface shown in Fig. 1 due to the small grains deposited during room temperature sputtering.

The RT AlN capped bulk GaN sample was annealed after capping both sides using the same conventional anneal and 1400 °C peak temperature MRTA process as the 400 °C-deposited AlN substrates. No cracks or annealing damage were observed as shown by the DIC image of the GaN surface after annealing as shown in Fig. 10 in contrast to Fig. 8, which shows widespread cracking in the HT sputtered AlN cap. Cracking was also not observed on the optically-polished surface of the bulk GaN protected by RT sputtered AlN. This lack of cracking with the RT-deposited cap demonstrates that the RT sputtered AlN is superior to HT sputtered AlN cap in protecting the surface of bulk GaN samples. Additionally, the RMS roughness of the AlN cap after annealing is 0.48 nm, which is essentially unchanged compared to the as-sputtered sample as shown in Fig. 9.

The AlN cap was removed after the annealing process to allow for further characterization of the GaN surface. The AlN cap was etched using AZ400K photore sist developer solution, which has been shown to preferentially etch AlN over Ga-polar GaN without damaging the GaN surface.28,29 To completely etch the AlN off of both sides of the bulk GaN sample, the sample was submerged in AZ400K for 15 minutes. Because there is KOH in the developer solution, the N-polar side of the bulk substrate was etched. It was determined that the etch rate of N-polar GaN in the AZ400K solution heated to 80 °C is 100 nm/min. In many vertical GaN devices, the back side (which will usually be N-polar) will have a blanket metal contact, and the KOH-etched rough surface will provide lower contact resistance due to increased contact area.30

After annealing and etching off the room temperature-sputtered AlN cap, the Ga-polar GaN surface is extremely smooth as shown in Fig. 11. The RMS roughness of the surface is 0.32 nm, confirming that the RT AlN cap provided excellent protection of the underlying GaN surface. Any surface damage would be evident via thermal etch pits, as have been observed previously in other annealing studies.21 For device applications, large areas of the surface must be protected. A Zygo optical profilometer was utilized to assess the surface roughness over a larger area than AFM’s capabilities as shown in Fig. 12. The RMS roughness was 0.70 nm over a 350 μm × 260 μm area. Thus, the cap developed in this research is capable of providing excellent protection for the underlying bulk GaN and facilitates annealing at high
temperatures, which are required for implanted dopant activation, without GaN decomposition. The RT cap was able to protect unimplanted GaN sufficiently in this research. Implanted dopants will degrade the crystalline structure of the underlying GaN, making the GaN more readily decompose. However, the first step of the SMRTA process is a conventional anneal conducted at thermodynamically stable temperatures. During the conventional anneal, a significant amount of the implantation damage is reversed. Because the conventional anneal is performed at thermodynamically stable temperatures, the cap is not stressed in this step while the crystalline lattice is being recovered and thus the RT cap is expected to sufficiently protect the implanted GaN.

The crystalline quality of the GaN and AlN before and after the MRTA process was compared for the sample with a RT AlN cap using Raman spectroscopy. The raw spectra before and after annealing are nearly identical as shown in Fig. 13. To quantify crystalline quality, the full width at half-maximum (FWHM) of the GaN E2 Raman peak at 567 cm−1 of the two samples is compared.31 Before annealing, the FWHM is 2.83 cm−1 with a standard deviation of 0.02 cm−1. After annealing, the FWHM is 2.84 cm−1 ± 0.02 cm−1, which is well within the standard deviation of the initial crystal quality. While the GaN did not exhibit a statistically significant change in crystal quality, the AlN did. The inset of Fig. 13 shows a zoomed in portion of the raw Raman spectra from 600–750 cm−1. The AlN E2 peak (657 cm−1, which is well within the standard deviation of the initial crystal quality, the AlN did not exhibit a statistically significant change in crystal quality.

Conclusions

In conclusion, performing high temperature annealing on bulk GaN substrates requires additional considerations compared to standard heteroepitaxial GaN. Sputtered AlN capping layers deposited at 400°C develop stresses that lead to cracking on very smooth, epitaxial bulk GaN surfaces. The deep cracks formed in the capping layer resulted in decomposition of the GaN in these cracked regions during high temperature annealing. However, the cracking in the AlN capping layer can be avoided by sputtering the AlN capping layer at room temperature. Lower temperature deposition of AlN capping layers produces smooth continuous films because the AlN does not have the energy to orient to the GaN surface. Finally, the GaN protected by the room temperature, crack-free, sputtered AlN does not exhibit degradation in surface morphology after being exposed to rapid thermal pulses with a maximum temperature of 1400°C. The ability to anneal bulk GaN at high temperatures without surface degradation using the AlN cap developed herein is a critical enabling processing step for future vertical III-nitride devices.

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References

1. S. Nakamura, T. Mukai, and M. Senoh, *Jpn. J. Appl. Phys.*, 30, L1998 (1991).
2. C. Srabanti, L. S. Brian, Y. W. Hoi, and K. M. Umesh, *Semicond. Sci. Technol.*, 28, 074014 (2013).
3. T. Oka, T. Ina, Y. Ueno, and J. Nishii, *Appl. Phys. Express*, 8, 054101 (2015).
4. T. P. Chow, *Microelectr. Eng.*, 83, 112 (2006).
5. S. Chowdhury, B. L. Swenson, and U. K. Mishra, *IEEE Electr. Device Lett.*, 29, 543 (2008).
6. O. Tohru, U. Yukihisa, I. Tsutomu, and H. Kazuya, *Appl. Phys. Express*, 7, 021002 (2014).
7. J. C. Zolper, R. J. Shul, A. G. Baca, R. G. Wilson, S. J. Pearton, and R. A. Stall, *Appl. Phys. Lett.*, 68, 2273 (1996).
8. T. C. Hager, K. A. Jones, M. A. Derenge, and T. S. Zheleva, *J. Appl. Phys.*, 105, 053506 (2009).
9. B. N. Feigelson, T. J. Anderson, M. A. Lefrant, J. K. Hite, C. R. Eddy, and F. J. Kub, *J. Cryst. Growth*, 350, 21 (2012).
10. T. J. Anderson, B. N. Feigelson, F. J. Kub, M. J. Tadjar, K. D. Hobart, M. A. Mastro, J. K. Hite, and C. R. Eddy, Jr., *Electronics Lett.*, 50, 197 (2014).
11. J. D. Greenlee, B. N. Feigelson, T. J. Anderson, J. K. Hite, K. D. Hobart, and F. J. Kub, *ECS Journal of Solid State Science and Technology*, 4, P382 (2015).
12. J. Unfald, B. Onderka, A. Davydov, and R. Schmid-Fetzer, *J. Cryst. Growth*, 256, 33 (2003).
13. J. C. Zolper, D. J. Rieger, A. G. Baca, S. J. Pearton, J. W. Lee, and R. A. Stall, *Appl. Phys. Lett.*, 69, 538 (1996).
14. Y. Nakano and T. Kacha, *Appl. Phys. Lett.*, 79, 1468 (2001).
15. G. S. Siddarth, M. Madhu, V. R. Mulpani, A. S. John, M. A. Mastro, R. E. Charles, Jr., R. T. Holt, R. L. Henry, and A. F. Jaime, Jr., G.-N. Elba, R. D. Vispute, and T. Yong-Lai, *Semicond. Sci. Technol.*, 22, 1151 (2007).
16. F. Gloux, T. Wojtowicz, P. Rutana, K. Lorenz, and E. Alves, *Phys. Status Solidi A*, 205, 2172 (2006).
17. E. Nogales, R. W. Martin, K. P. O’Donnell, K. Lorenz, E. Alves, S. Ruffenach, and O. Briot, *Appl. Phys. Lett.*, 88, 031902 (2006).
18. S. Raghavan, J. Acord, and J. M. Redwing, *Applied Physics Letters*, 86, 261907 (2005).
19. S. Hearne, E. Chason, J. Han, A. A. Floro, J. Figiel, J. Hunter, H. Amano, and I. S. T. Tsong, *Appl. Physics Letters*, 74, 356 (1999).
20. J. L. Weyher, S. Lazar, L. Mach, Z. Lillental-Weber, R. J. Molnar, S. Müller, V. G. M. Sivel, G. Nowak, and J. E. Gezegory, *J. Cryst. Growth*, 385, 384 (2007).
21. J. D. Greenlee, T. J. Anderson, B. N. Feigelson, J. K. Hite, K. M. Bussmann, J. Charles, R. Eddy, K. D. Hobart, and F. J. Kub, *Appl. Phys. Express*, 7, 121003 (2014).
22. J. D. Greenlee, B. N. Feigelson, T. J. Anderson, M. J. Tadjar, J. K. Hite, M. A. Mastro, C. R. Eddy, K. D. Hobart, and F. J. Kub, *J. Appl. Phys.*, 116 (2014).
23. W. M. Yun and R. J. Paff, *J. Appl. Phys.*, 45, 1456 (1974).
24. S. Yoshida, S. Misawa, and S. Gonda, *J. Vac. Sci. Technol. B*, 1, 250 (1983).
25. Y. Cao and D. Jena, *Adv. Mater.*, 23, 1914 (2011).
26. A. Artieda, M. Barbieri, C. S. Sandu, and P. Muralt, *J. Appl. Phys.*, 105 (2009).
27. S. C. Jain, M. Wilander, J. Narayan, and R. V. Overstraeten, *Journal of Applied Physics*, 87, 965 (2000).
28. J. D. Greenlee, T. J. Anderson, B. N. Feigelson, A. D. Koehler, K. D. Hobart, and F. J. Kub, *Appl. Phys. Express*, 8, 036503 (2015).
29. J. R. Mileham, S. J. Pearton, C. R. Abernathy, J. D. MacKenzie, R. J. Shul, and S. P. Kilcoyne, *Appl. Phys. Lett.*, 67, 1119 (1995).
30. H. Hung-Wen, C. C. Kao, H. C. Kuo, S. C. Wang, and C. C. Yu, *IEEE Photonics Technol. Lett.*, 17, 983 (2005).
31. M. Kuball, *Surf. Interface Anal.*, 31, 987 (2001).