Design of a broadband high-efficiency power amplifier by using a simple method

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Abstract This letter proposes a simple method for designing broadband high-efficiency power amplifiers (PAs). Hybrid Class EFJ PAs theory is applied to achieve both high-efficiency and broadband at the same time. In order to make it more practical, a low-pass filter structure is introduced to design output matching circuits that satisfy the impedance conditions of Class EFJ PAs. Moreover, this paper exploits the characteristics of the transistor’s output impedance, and selects three frequency points to design and synthesize a low-pass matching network. For validation, a PA working in 1.3–3.9 GHz is designed and fabricated based on CGH40010F transistor. The measurements illustrate that output power is from 40.5 dBm to 42.3 dBm and drain efficiency is between 61.3% and 71.2% at saturated level in the target frequency band. The ACLR is smaller than $28.4\,\text{dBc}$ in the same frequency band.

Keywords: broadband, class-EFJ power amplifier, high efficiency, low-pass filter matching

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

With the rapid development of wireless communication technology, the amount of information transmitted is getting larger and larger, and the bandwidth required becomes wider and wider [1, 2, 3, 4, 5, 6]. The power amplifier is the key module of the transmitter. In order to keep up with the development trend of modern wireless communications, broadband high-efficiency power amplifiers (PAs) should be further developed [7–10]. Class J PA is a new type of PA proposed by S.C. Cripps [11], which is suitable for broadband application. Class EF PA is presented in [12], which can achieve ideally 100% drain efficiency. Unfortunately, neither class J nor class EF PAs can achieve both broadband and high efficiency at the same time. To solve this issue, several methods of realizing broadband high-efficiency PAs have been proposed. Among them, continuous modes PAs such as continuous F [13], continuous J [14], and continuous F\textsuperscript{1} [15] can realize both broadband and high efficiency at the same time. However, algorithms are often required to iteratively optimize the circuits, which leads to the complexity of realizing continuous mode PAs. Recently, in order to reduce the difficulty of achieving a broadband high-efficiency PA, a PA called hybrid Class EFJ PAs is proposed in [16], in which high efficiency and large bandwidth can be obtained at certain conditions at the same time. The routing of designing Class EFJ PAs is simpler compared with that of continuous mode PAs. The key to achieve Class EFJ PAs is to design output matching circuits that satisfy the impedance conditions. Filter matching structure has been used to design broadband matching circuits for such as Class F, Class F\textsuperscript{1} and Class J PAs [17–24]. It demonstrates that low-pass filter matching network exhibits excellent broadband characteristics.

In this paper, a simple method for designing broadband high efficiency PAs is presented by combining theory of Class EFJ PAs and low-pass matching structure. The low-pass matching structure is used to design output matching circuits that meet the impedance requirements of Class EFJ PAs in a wide frequency range. Compared with previous work in [16], a significant innovation in this paper is the introduction of low-pass matching structure to design output circuits that satisfy the impedance conditions of the EFJ PA. This makes the process of implementing EFJ PA easier and more practical. In addition, this paper exploits the characteristics of the transistor’s output impedance, and selects three frequency points to design and synthesize a low-pass matching network, which improves the accuracy within the working bandwidth. Stepped matching technology is also employed to design wideband input matching circuits. For validation, a broadband high efficiency PA is designed and fabricated.

2. Theoretical analysis

The Class EF PAs and the Class J PAs are integrated when satisfying certain conditions, and such new combined PAs are called hybrid Class-EFJ PAs [16]. Fig. 1 is the circuit topology of a Class EFJ PA. As theory of the Class EFJ PAs described in [16], the fundamental impedance $Z_{f0}$ of

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Fig_1.png}
\caption{Circuit topology of the class EFJ PA.}
\end{figure}

\vspace{1cm}

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the Class EFJ PAs is expressed as:

$$Z_{f_0} = (1 + j) \cdot R^*$$

(1)

where $R^*$ is the load impedance shown as Fig. 1, which is between 15.89 $\Omega$ and 46.29 $\Omega$. The impedance range of $R^*$ provides the possibility of broadband design, which is the main advantage of the EFJ PA. In practical design, the load impedance $R$ can be determined, combined with the load-pull results. The harmonic impedances of the Class-EFJ PAs are defined as following [16]:

$$Z_{2f_0} = 0$$

(2)

$$Z_{3f_0} = \infty$$

(3)

This paper mainly focuses on the realization of the fundamental impedance condition. The requirements of Class EFJ PAs for harmonic impedances are not strict. The realized harmonic impedances only need to be approximate to be ideal as described in (2) and (3).

In [16], we mainly rely on optimization to get the output matching circuit, which limits the further practicality of the Class EFJ PAs. Therefore, in this paper, low-pass matching circuits are introduced to achieve a fundamental matching circuit in a wide frequency band, which make designing EFJ PAs more practical and easier. The real part of $Z_{f_0}$ is taken to design the low-pass matching circuits. In this work, target frequency band is from 1.3 GHz to 3.9 GHz. Three frequency points 1.3 GHz, 2.6 GHz and 3.9 GHz are considered in designing the fundamental output circuits. Load-pull simulation is conducted in ADS software. The obtained load impedances at different frequencies are shown in Fig. 2. It is obviously that the load impedance gradually decreases with increasing frequency as shown in Fig. 2. As mentioned above, the real part of the impedance $R^*$ is a variable range. Therefore, its value can be selected for different frequency points in combination with the result of load-pull simulation. Combining load-pull simulation and the real impedance of $Z_{f_0}$ described in (1), the real part of $Z_{f_0}$ can be taken as 32 $\Omega$ at the center frequency of 2.6 GHz. The real part of $Z_{f_0}$ can also be determined as 37 $\Omega$ and 23 $\Omega$ at 1.3 GHz and 3.9 GHz, respectively.

The second-order low-pass structure should be used to get the 104% of fractional bandwidth in target frequency band [25]. Fig. 3 (a) is the required second-order low-pass filtering prototype based on [26]. At 2.6 GHz, the impedance ratio between the load of 50 $\Omega$ and the real impedance of $Z_{f_0}$ can be calculated as 1.56 : 1. Therefore, the $g_5$ shown in Fig. 2 can be determined as 1.56. Similarly, for 1.3 GHz and 3.9 GHz, the $g_5$ also can be obtained as 1.35 and 2.17, respectively. The $g_1$, $g_2$, $g_3$ and $g_4$ at the above-mentioned frequency points are summarized in Table I, Table II and Table III, respectively.

![Fig. 2 The output impedances of transistor for different frequencies. (Normalized to 50Ω)](image)

![Fig. 3 Second-order low-pass structure (a) low-pass filtering prototype (b) circuit with lumped parameters under 50Ω load system.](image)

| Table I Values of $g_5$, $L_n$ and $C_n$ at 2.6 GHz |
|----------------|----------------|---------|
| $g_1$          | 0.91           | C1      |
| $g_2$          | 1.21           | L1      |
| $g_3$          | 1.36           | L2      |
| $g_4$          | 0.81           | C2      |

| Table II Values of $g_5$, $L_n$ and $C_n$ at 1.3 GHz |
|----------------|----------------|---------|
| $g_1$          | 0.78           | L1      |
| $g_2$          | 1.04           | C1      |
| $g_3$          | 1.17           | L2      |
| $g_4$          | 0.69           | C2      |

| Table III Values of $g_5$, $L_n$ and $C_n$ at 3.9 GHz |
|----------------|----------------|---------|
| $g_1$          | 1.27           | L1      |
| $g_2$          | 1.68           | C1      |
| $g_3$          | 1.89           | L2      |
| $g_4$          | 1.11           | C2      |

![Table I Values of $g_5$, $L_n$ and $C_n$ at 2.6 GHz](image)

![Table II Values of $g_5$, $L_n$ and $C_n$ at 1.3 GHz](image)

![Table III Values of $g_5$, $L_n$ and $C_n$ at 3.9 GHz](image)
operating angular frequency and the normalized impedance, respectively. \( n \) is 1 or 2 in second-order low-pass structure. The obtained values of \( L_n \) and \( C_n \) are listed in Table I, Table II and Table III, respectively, for different frequency points.

The circuit with lumped parameters shown in Fig. 3(b) can be transformed into the circuit with distributed parameters by using the following equations:

\[
\omega L \approx Z_H l_H \quad (6)
\]

\[
l_H \approx \frac{v_p l}{Z_H} \quad (7)
\]

\[
\frac{1}{\omega C} = 2 \frac{Z_L}{\tan \beta l_L} \quad (8)
\]

\[
l_L \approx \frac{\arctan(2\omega Z_L C)}{\beta} \quad (9)
\]

where \( L, C \) refer to the inductor and capacitor in Fig. 3(b). The inductors \( L_1, L_2 \) in Fig. 3(b) are replaced by high-impedance microstrip lines. The capacitors \( C_1, C_2 \) in Fig. 3(b) are replaced by low-impedance open-circuit microstrip lines. \( Z_H, Z_L \) represent the characteristic impedance of the high-impedance microstrip lines and the low-impedance microstrip lines, respectively. \( l_H, l_L \) refer to the length of the high-impedance microstrip lines and the low-impedance microstrip lines, respectively. \( \beta, V_p \) represent the propagation constant and phase velocity of the microstrip lines, respectively. Due to the frequency dispersion of microstrip lines, \( \beta l \) should be expressed as:

\[
\beta l = \frac{\pi f}{2 f_0} \quad (10)
\]

Using (6)–(10) at 1.3 GHz, 2.6 GHz and 3.9 GHz, the low-pass matching structure of distributed parameters that operates in 1.3–3.9 GHz can be synthesized. The completed low-pass matching structure is shown in Fig. 4(a). The simulated input impedance of this low-pass matching circuit is also shown in Fig. 4(b). It can be seen from Fig. 4(b) that the value of input impedance at 1.3 GHz, 2.6 GHz, 3.9 GHz is close to the theoretical value, which verifies the effectiveness of distributed circuits.

Harmonic control networks should be added to make the PA satisfy the requirements of harmonic impedances described in (2) and (3). For the purpose of enhancing the accuracy of output circuits, transistor package parameters are also considered in practical designing process. As shown in Fig. 5, the micro-stripe lines TL1 and TL2 are tuned to let the second harmonic impedance roughly zero. The third harmonic impedance is roughly close to infinite by tuning micro-stripe lines TL1 and TL3. Stepped matching technology is applied to design wideband input matching circuits. In order to obtain the best performance of PA, optimization should be performed in ADS software. After optimization, the complete circuit diagram and related parameters value are shown in Fig. 5.

The simulated impedance of the implemented PA at the current plane and the package plane are plotted in Fig. 6. The impedance result shown in Fig. 6(a) has a certain deviation from that shown in Fig. 4(b). This is due to the introduction of the harmonic control network and parasitic parameters of transistor. The harmonic network not only realizes the adjustment of harmonic impedance, but also eliminates the effect of parasitic parameters on the fundamental matching circuit. Overall, the results shown in Fig. 6(b) are acceptable compared to theoretical value. Voltage and current waveforms are simulated, and are plotted in Fig. 7.
3. Experiment and measurement

To verify the validity of the design method presented in this paper, a broadband high efficiency PA is fabricated using CGH40010F based on the Rogers 4350B. The drain and gate bias voltages are set to 28 V and 2.8 V, respectively. Fig. 8 is a photo of the fabricated amplifier.

The fabricated PA is tested to characterize its performance. The obtained S-parameters are shown in Fig. 9. It is observed that S11 is larger than −10 dB. It is mainly because the PA needs to be kept stable over the entire frequency band.

In order to characterize the actual performance of the fabricated PA, the PA is driven by continuous wave signals. Simulated and measured results are plotted in Fig. 10 and Fig. 11. It reveals that the saturated output power is from 40.5 dBm to 42.3 dBm with a gain of between 10.5 dB and 11.7 dB in 1.3–3.9 GHz. Meanwhile, drain efficiency is from 61.3% to 71.2% in the same interesting frequency band.

In order to characterize the linearity of the fabricated PA, the PA is driven by a 5 MHz W-CDMA signal with peak-to-average ratio of 6.5 dB. And its measured ACLR results are plotted in Figure. 12. It can be seen that ACLR of smaller than −28.4 dBc is got in 1.3–3.9 GHz within about 35.0 dBm average output power. Meanwhile, drain efficiency of from 29.3% to 34.6% are got in the target frequency band.

Table IV [27, 28, 29, 30] lists the performance of some PAs. It is apparently that bandwidth of the proposed PA is larger than that of others. At the same time, the proposed PA has similar power and drain efficiency to other related PAs. Overall, the designed PA can achieve both large bandwidth and high efficiency at the same time. Furthermore, compared with the continuous mode PAs and the previous one reported in [16], the design process of achieving broadband high-efficiency PA presented in this paper is more convenient and...
Table IV  Performances compared with related PAs.

| Ref | Class | Bandwidth (GHz) | Power (dBm) | Saturation DE (%) |
|-----|-------|-----------------|-------------|------------------|
| [27] | EF    | 2.6-3.6         | 40.7-41.6   | 62-78            |
| [28] | B/J   | 1.3-2.4         | 40-41.3     | 63-72            |
| [29] | J     | 1.9-3.0         | 40-42.2     | 58-70            |
| [30] | J     | 1.3-2.4         | 40-41.3     | 63-72            |
| This Work | EFJ | 1.3-3.9         | 40.5-42.3   | 61.3-71.2        |

practical.

4. Conclusion

A novel simple method for design broadband high-efficiency PAs is presented. The theory of hybrid Class EFJ PAs is applied, while a low-pass matching structure is used to design output matching circuits that meet the impedance requirements of Class EFJ PAs. In addition, three frequency points are selected to design and synthesize a low-pass matching network. Stepped matching technology is also exploited in the input matching circuits to expand the operating bandwidth of the PA. For validation, a 1.3–3.9 GHz PA is fabricated. Measurements demonstrate that output power is from 40.5 dBm to 42.3 dBm and drain efficiency is between 61.3% and 71.2% in 1.3–3.9 GHz. Compared to other related PAs, it shows that a good compromise between efficiency and bandwidth is achieved. It is worth noting that the method proposed in this paper makes it easier to achieve high-efficiency broadband PAs. This makes it more potential for practical applications.

Acknowledgments

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