Design and application of low power switch IC

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Abstract—Based on PSM (pulse skip modulation) mode, this paper analyzes and optimizes the system, designs a low-power switching power supply chip, and integrates the high-voltage power MOSFET switch and power controller in one device. Different from the traditional PWM (pulse width modulator) controller, the output voltage is regulated by simple on / off control without loop compensation. The controller consists of oscillator, feedback circuit, 5.8V regulator, bypass pin under voltage circuit, over temperature protection, frequency jitter, current limiting circuit and leading edge blanking of integrated 700V power MOSFET. The chip can be applied to mobile phones, digital cameras, and chargers of low-power electrical appliances, etc.

1. INTRODUCTION
The control modes of smart power integrated circuit (SPIC) are pulse width modulation mode (PWM) with constant frequency widening (CFVW) and pulse frequency modulation mode (PFM) with constant width variable frequency (CWVF). The efficiency of spic with PWM modulation mode is low under low load, and the peak value of control pulse harmonic is large. The PFM control circuit is more complex, and the harmonic distribution is time-varying and too scattered, which makes the subsequent filter design difficult. Pulse Skip Modulation (PSM) is a new modulation mode, which is different from PWM and PFM. It is a constant width and constant frequency modulation mode.

This paper analyzes and optimizes the system based on the pulse trans cycle modulation (PSM) mode, and designs a low-power switching power supply chip, which uses simple on / off control without loop compensation. It can be applied to mobile phones, digital cameras, chargers of low-power electrical appliances, etc.

2. PRINCIPLE OF PSM

2.1 Advantages of PSM system
PWM mode and PFM mode are commonly used in power converter. The principle of PWM mode is simple and the circuit is easy to realize, but the PWM mode has the disadvantages of poor linear adjustment rate and low efficiency under light load. Although PFM modulation mode improves the efficiency under light load, the continuous change of working frequency will bring difficulties to the realization of filtering. [1]

The efficiency of PSM control mode is high. It has the characteristics of light load, high response speed and strong robustness. It is the ideal modulation mode of low power converter.
2.2 Signal-modulating principle
When the detection value is lower than the set output, the pulse sequence will pass through the fixed phase; otherwise, these pulse sequences will be crossed and the power MOS will be turned off until the detection value is higher than the set output. The output voltage of PSM converter is stabilized by controlling the number of cycles. [2]

![Figure 1. PSM system](image)

 Pulse cross period modulation generally adopts double loop control, namely voltage outer loop and current inner loop control. According to the change of load and input voltage, discrete duty cycle is generated to stabilize the output voltage. When the rising edge of each switch clock cycle comes, the output voltage is sampled, and the sampling voltage is compared with the reference voltage to generate "0" or "1" level signals. After that, these level signals representing the output voltage state are saved to the state machine. Through the state machine, the peak current of inductor in each cycle is observed, so as to generate different discrete duty cycles required by the system. When the load is very light, it will span some switching cycles to improve the efficiency of switching power supply, so it is called pulse cross period modulation. [3]

3. BRIEF INTRODUCTION OF PSM CONTROLLER
The main module of PSM controller mainly includes: current limit comparator, reference voltage source and error operational amplifier. The current limit comparator is divided into three parts: inductive current detection circuit, inductive current comparison circuit and slope compensation circuit.

The current duty cycle of the circuit is unique to the PSM system. Voltage reference is a necessary module for almost every analog chip circuit. Its temperature performance and PSRR directly determine the average output voltage and ripple size.

Voltage reference is an important module in integrated circuit. It is often used in the occasion where the output voltage needs to be accurately controlled. It is required to keep stable by overcoming the changes of process, voltage, temperature and load. Its temperature performance and power supply rejection ratio determine the average value and ripple size of the output voltage. Bandgap voltage reference is widely used because of its good temperature characteristics. [4]

The output voltage ripple of PSM modulation switching power supply is large, and LDO is often connected in series to improve the output ripple. For low-voltage LDO, its negative feedback loop can be equivalent to a low-voltage three-stage error operational amplifier.

The chip integrates high-voltage power MOSFET switch and power controller in the device. Unlike the traditional PWM controller, the output voltage can be adjusted by simple on / off control. The controller consists of oscillator, feedback circuit, 5.8 V voltage-regulator, bypass pin under voltage circuit, OTP over temperature protection circuit, current limiting circuit and front-end blanking circuit of integrated 700 V power MOSFET.
3.1 Oscillator circuit
A typical oscillator frequency is set internally to an average of 132 kHz. The oscillator produces two signals: the maximum duty cycle signal and the clock signal indicating the beginning of each cycle.

In the chip design, the OSC module is required to generate square wave oscillation signal, which is output to the automatic restart module and power transistor as the maximum duty cycle signal. At the same time, the output of the oscillator requires a certain frequency jitter to meet the EMI requirements of the chip. The OSC module generates a square wave signal dcmax, which is used as the maximum duty cycle of the circuit; in addition, the signal is also used as the counting signal of the automatic restart counter. [5]

The circuit used in the oscillator introduces a small amount of frequency jitter, usually 9 kHz peak to peak value, to minimize EMI radiation. The modulation rate of frequency jitter is set to 1.5 kHz to optimize the average and quasi peak emission EMI reduction. An oscilloscope triggered at the falling edge of drain waveform shall be used to measure frequency jitter.

3.2 Feedback input circuit
The feedback input circuit of FB pin consists of a source follower with low impedance. When the current input to the pin exceeds 49A, a logic low level is generated in the feedback circuit. At the rising
edge of the clock signal, the output is sampled at the beginning of each cycle. If it is high level, the power MOSFET is on during the cycle, otherwise the power MOSFET is turned off. Sampling is only performed at the beginning of each cycle, so subsequent changes in pin voltage or current during the remainder of the cycle are ignored.

3.3 Thermal-shutdown circuit
Power IC consumes more power and the chip temperature is higher. In order to avoid damage when the chip works at high temperature, the chip is required to have overheating protection module. The protection circuit usually uses the negative temperature characteristic of PN junction to measure the chip temperature. When the measured temperature is higher than a certain value of normal working temperature, the control chip will turn off the circuit; when the measured temperature decreases to a certain value, the control chip will resume normal operation.

The thermal shutdown circuit detects the temperature of the die. The threshold is set at 143 °C and the typical value is 72 °C hysteresis. When the core temperature rises above this threshold (143 °C), the power MOSFET will be disabled and remain disabled until the core temperature decreases by 72 °C, at which time it will be re enabled.

3.4 Current limiting circuit
The current limiting circuit detects the current in the power MOSFET. When this current exceeds the internal threshold, the power MOSFET will turn off for the rest of the cycle. After the power MOSFET is turned on, the leading edge blanking circuit will prohibit the current limiting comparator for a short time. The leading edge blanking time has been set so that the current spike caused by the reverse recovery time of capacitor and rectifier will not lead to the premature termination of switching pulse.

The module can limit the current flowing through the power transistor, and change the duty cycle signal according to the detected chip state, so as to operate in different states under different loads. The module detects the d-pole of the power MOS transistor to determine the current value flowing through the power transistor. When the current reaches the limit value of the rated current, the LDMOS is turned off.

3.5 Automatic restart circuit
If there is an output overload condition, output short circuit or open-loop fault, the chip will enter the automatic restart state. Every time the FB pin is pulled high, the oscillator will reset. If the FB pin is not pulled up to 40ms, the power MOSFET switch will be disabled for 800ms. The power supply is enabled and disabled alternately by automatic restart, and the MOSFET is switched until the fault state is eliminated.

4. CHIP APPLICATION CIRCUIT
The schematic diagram shown in Fig. 4 is the input circuit of the application chip. The circuit eliminates the primary clamping elements by using clamp free technology, which reduces the cost and complexity of the circuit.
4.1 Input circuit

AC input is rectified from D1 to D4 and filtered by large capacity storage capacitors C1 and C2. Resistor RF1 is a fireproof, fusible, wound type resistor used as fuse and current limiter. C1, C2, L1 and L2 form filters and differential mode noise attenuators. Resistor R1 suppresses oscillations caused by L1 and L2.

The input stage, together with the frequency jitter of the chip, the low value Y1 capacitor in T1 and the e-shield winding of PI, enable the design to meet the conducted and radiated EMI limits with a margin of 10dbv. The low value of CY1 is very important to meet the very low contact current specified by the adapter. In this case, a current of 10A is applied to the primary winding of T1 by rectifying and filtering the input voltage. The other side of the primary winding is driven by an integrated MOSFET in U1. Since the low value of the internal current limit and the transformer primary winding capacitance are sufficient to clamp down the leakage induced drain voltage spike, no primary clamping element is required.

4.2 Output circuit

The secondary of Fly-back transformer T1 is rectified by low-cost fast recovery diode d5 and filtered by low ESR capacitor C4. The combined voltage drop between VR1, R2 and U2 LEDs determines the output voltage. When the output voltage exceeds this level, the current will flow through the U2 led. With the increase of LED current, the current fed back to U1 feedback pin increases until the turn-off threshold current is reached. At this time, further switching cycle of U1 is prohibited. At full load, almost all switching cycles are enabled; at very light loads, almost all switching cycles are disabled, providing low effective frequency, high light load efficiency and low no-load power consumption. Resistor R3 provides a 1 mA current through VR1, bringing the Zener diode closer to its test current. Resistor R2 allows the output voltage to be adjusted to compensate for a possible undesirable design of Zener diode values. For higher output accuracy, Zener diodes can also be replaced by reference ICs.

5. STATEMENT

This IC is a low-cost, low standby power chip, mainly used for AC / DC conversion. Its structure is simple, the number of devices is small, the cost is low, and the efficiency is high. At the same time, it has good performance under the working load. The chip can be applied to mobile phones, digital cameras, and chargers of low-power electrical appliances, etc.
REFERENCES
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