Comprehensive Analysis of Source and Drain Recess Depth Variations on Silicon Nanosheet FETs for Sub 5-nm Node SoC Application

JINSEU JEONG, (Student Member, IEEE), JUN-SIK YOON, (Member, IEEE), SEUNGHWAN LEE, (Student Member, IEEE), AND ROCK-HYUN BAEK, (Member, IEEE)
Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, South Korea

Corresponding author: Rock-Hyun Baek (rh.baek@postech.ac.kr)

This work was supported in part by the Ministry of Trade, Industry, and Energy (MOTIE) under Grant 10080617, in part by the Korea Semiconductor Research Consortium (KSRC) Support Program for the development of the future semiconductor device, in part by the National Research Foundation of Korea (NRF) funded by the Korea Government (MSIT) under Grant NRF-2017R1C1B5017795, in part by the POSTECH-Samsung Electronics Industry-Academia Cooperative Research Center, and in part by the IC Design Education Center (IDEC), South Korea.

Abstract Excess source and drain (S/D) recess depth ($T_{SD}$) variations were analyzed comprehensively as one of the most critical factors to DC/AC performances of sub 5-nm node Si-Nanosheet (NS) FETs for system-on-chip (SoC) applications. Variations of off-, on-state currents ($I_{off}$, $I_{on}$) in three-stacked NS channels and parasitic bottom transistor ($tr_{pbt}$), gate capacitance ($C_{gg}$), intrinsic switching delay time ($\tau_d$), and static power dissipation ($P_{static}$) are investigated quantitatively according to the $T_{SD}$ variations. More S/D dopants diffuse into the $tr_{pbt}$ with the deeper $T_{SD}$, so the $I_{off}$ and $I_{on}$ increase due to raised current flowing through the $tr_{pbt}$. Especially, the $I_{off}$ of PFETs remarkably increases above the certain $T_{SD}$ ($T_{SD,critical}$) compared to NFETs. Furthermore, the $I_{on}$ contribution of each channels having the $T_{SD,critical}$ is the largest at the top NS channel and the $tr_{pbt}$ has the ignorable $I_{on}$ contribution. Among the NS channels, the top (bottom) NS channel has the largest (smallest) $I_{on}$ contribution due to its larger (smaller) carrier density and velocity for both P-/NFETs. The $C_{gg}$ also increases with the deeper $T_{SD}$ by increasing parasitic capacitance, but fortunately, the $\tau_d$ decreases simultaneously due to the larger increasing rate of the $I_{on}$ than that of the $C_{gg}$ for all SoC applications. However, the $P_{static}$ enormously increases with the deeper $T_{SD}$, and low power application is the most sensitive to the $T_{SD}$ variations among the SoC applications. Comprehensive analysis of the inevitable $tr_{pbt}$ effects on DC/AC performances is one of the most critical indicators whether Si-NSFETs could be adopted to the sub 5-nm node CMOS technology.

Index Terms Nanosheet FET, parasitic bottom transistor, source/drain recess depth, sub 5-nm node, sub-sheet leakage, TCAD simulation, U-shaped source/drain.

I. INTRODUCTION
For several decades, conventional bulk planar Si-MOSFETs had been successfully scaled down, and several novel strategies were adopted from 90- to 32-nm node to improve the CMOS performance [1]–[4]. However, aggressive scale-down of planar Si-MOSFETs caused the loss of channel controllability, and short channel effects (SCEs) significantly degraded the DC/AC performances. Since 2012, as a solution, 22-nm node Si-FinFETs were adopted to industry for overcoming the SCEs and enabling further scale-down [5]. The Si-FinFETs technologies have been continuously improved down to 7-nm node by decreasing fin pitch and contact poly pitch and increasing aspect ratio of fins [6]–[9]. However, these kinds of fin structures need extremely high fin aspect ratio and are limited by fin pitch [10]. As a result, vertically stacked Si-Gate-All-Around (GAA) nanosheet FETs (NSFETs) were proposed as a promising candidate to replace Si-FinFETs due to those superior electrostatics below 7-nm node [11]–[14]. But both Si-FinFETs and Si-NSFETs have inevitable parasitic channels below the intrinsic channels that critically affect the leakage current, which is the killing factor...
of scaled transistors [15], [16]. Especially, the Si-NSFETs are deeply concerned because of wider parasitic channels than the Si-FinFETs.

Meanwhile, in ultra-scaled transistor, impacts of process variations on DC/AC performances are inevitable inherent problems. Among these variations, source/drain (S/D) process variations should be carefully controlled because those are directly related to source-to-drain leakage current as well as drive current. So far, several studies about the impacts of the S/D process variations on the Si-FinFETs including S/D epitaxy shape, depth [17]–[19], S/D length [20], [21], and S/D doping concentration [22] were addressed, but the studies on the vertically stacked Si-NSFETs were rarely reported.

In this paper, we quantitatively investigated the impacts of S/D process variations on the DC/AC performances of sub 5-nm node Si-NSFETs. We analyzed off- and on-state currents (\(I_{\text{off}}, I_{\text{on}}\)), gate capacitance (\(C_{\text{gg}}\)), and switching delay time (\(\tau_d\)) according to S/D epitaxy shapes and S/D depth variations in the following sections. In Section II, we explained the device design and simulation methodology of the sub 5-nm node NSFETs. In Section III, we investigated the sensitivity of the \(I_{\text{off}}, I_{\text{on}}, C_{\text{gg}}, \tau_d\), and static power dissipation (\(P_{\text{static}}\)) to the S/D process variations. Finally, we gave a conclusion in Section IV.

II. DEVICE DESIGN AND SIMULATION METHODOLOGY

We simulated the sub 5-nm node three-stacked NSFETs with advanced physics models using Sentaurus TCAD simulator [23]. Drift-diffusion model was considered self-consistently with Poisson and carrier continuity equations for carrier transport. Density-gradient model was included to consider quantum confinement effects of the channel region [24], [25]. Slotboom bandgap narrowing model was also included for doping-induced bandgap narrowing in overall device regions [26]. Lombardi mobility model was considered to calculate the mobility degradation induced by transverse field at the interfaces [27]. Inversion and accumulation layer and thin-layer mobility models were included to consider Coulomb, phonon, and surface roughness scatterings [28], [29]. Low-field ballistic mobility and high-field saturation models were also included [30]. Furthermore, we considered recombination using Shockley-Read-Hall, Auger, and Hurkx band-to-band tunneling models [31]–[33]. Finally, a deformation potential model was considered for strain dependency of effective mass, effective density-of-states, carrier mobility, and band structure [34].

Fig. 1 shows the structure of the n-type NSFETs having ideal and U-shaped S/D epitaxies, and its cross-section view. All the NSFETs were formed by fully considering doping, diffusion, and strain effect using Sentaurus process simulator [23]. In reality, S/D recess profile cannot be a perfect vertical shape, so we adopted the U-shaped S/D recess profile, which was taken from [11]. In the U-shaped S/D, inner spacer length (\(L_{\text{sp}}\)) could be the shortest (longest) at the top (bottom) side, while gate length (\(L_g\)) was the same regardless of NS channels positions. Channel length (\(L_{\text{ch}}\)) was defined as distance from the source to the drain epitaxies in each of the NS channels. In addition, \(\text{Si}_{0.5}\text{Ge}_{0.5}\) and \(\text{Si}_{0.98}\text{C}_{0.02}\) epitaxies were formed as the S/D to induce compressive and tensile stress to the NS channels for p/n-type FETs (P-/NFETs), respectively.

Highly doped \(\text{Si}_{0.5}\text{Ge}_{0.5}\) [12] (\(\text{Si}_{0.98}\text{C}_{0.02}\) epilayers with boron (phosphorus) of \(5 \times 10^{20} (1 \times 10^{20})\) cm\(^{-3}\) were formed as the S/D of the PFETs (NFETs), and silicon NS channels and substrate were undoped (\(1 \times 10^{15}\) cm\(^{-3}\)). Punch-through stopper (PTS) was doped with phosphorus (boron) of \(2 \times 10^{18}\) cm\(^{-3}\) in the PFETs (NFETs). Detailed geometry parameters for the sub 5-nm node NSFETs were summarized.
in Table 1. Dielectric constants were 3.9, 5.0, and 22.0 in IL, spacer, and HfO2 for overall regions of the NSFETs, respectively. Each contact resistance (\(R_{\text{con}}\)) of the source and drain defined for contact width was fixed as an optimistic value of 50 \(\Omega \cdot \mu \text{m}\) for both P-/NFETs [36], and operating voltage (\(|V_{dd}|\)) was 0.7 V. All drain currents (\(I_{dd}\)) were normalized to sheet pitch (SHP), and threshold voltage (\(V_{th}\)) for both P-/NFETs [36], and operating voltage (\(|V_{gs}|\)) was 0.7 V. All drain currents (\(I_{dd}\)) were extracted using constant current method at \(W_{ch}/L_{g} \times 10^{-7}/\mu \text{A/mm}\), where \(W_{ch} = 3 \times (W_{top} + W_{bot} + 2 \times T_{BS})\). Finally, the NSFETs structures of this paper were built by process simulation mimicking the real process flow of [11], while electrical simulations were conducted using fully-calibrated physical model parameters of 10-nm node Si-FinFETs including saturation velocity and low-field ballistic coefficient [8], [35]. Here, I-V data of [11] could not be used for calibrating the physical model parameters, because those were presented as arbitrary units. Moreover, to estimate the \(I_{on}/I_{off}\) characteristics of the sub 5-nm node NSFET properly, calibrating the mobility and velocity model from matured and well-known Si-FinFETS technology was reasonable approach. For calibrating our TCAD deck to the hardware data properly, a higher S/D doping concentration (\(N_{SD}\)) of the PFETs than the NFETs was adopted for subthreshold swing (SS) and drain-induced barrier lowering (DIBL), which are relatively poorer for the PFETs than for the NFETs.

### III. RESULTS AND DISCUSSION

#### A. OFF-STATE (|\(V_{GS}| = 0, |V_{ds}| = |V_{dd}|\)) ANALYSIS

Fig. 2 shows transfer characteristics of the NSFETs according to excess S/D depth (\(T_{SD}\)) for both P-/NFETs and several DC characteristics are summarized in Table 2. Here, the \(V_{th}\) of the PFETs at the \(T_{SD}\) of 10-14 nm was not shown because they do not approach to the \(W_{ch}/L_{g} \times 10^{-7}/\mu \text{A/mm}\) even in very large positive gate voltage (\(|V_{gs}|\)). The \(T_{SD}\) splits from 0 to 14 nm, and drain voltage (\(|V_{ds}|\)) is fixed to the |\(V_{dd}|\). The \(I_{off}\) and \(I_{on}\) are defined as the \(I_{ds}\) when the |\(V_{gs}|\) is 0 and the |\(V_{dd}|\), respectively. The ideal S/D NSFETS show the smallest SS comparing to the U-shaped S/D NSFETS due to the longest \(L_{th}\), which mitigated the SCEs. In U-shaped S/D NSFETS, both \(I_{off}\) and \(I_{on}\) increase with the deeper \(T_{SD}\), and especially, the \(I_{off}\) remarkably increases at the certain points of the \(T_{SD}\). To quantify these effects, we defined critical excess S/D depth (\(T_{SD,critical}\)) as the maximum \(T_{SD}\) where the \(I_{off}\) is smaller than 10 times of \(I_{off}\) at the \(T_{SD}\) of 0. The definition of the \(T_{SD,critical}\) is based on a \(I_{off}\) criteria for system-on chip (SoC) applications, where the devices having the \(I_{off}\) of 10 nA/\(\mu\text{m}\) are no longer available for standard performance applications [37]. The \(T_{SD,critical}\) is 4 nm for the PFETs and 10 nm for the NFETs, and it means that DC performance variations to the \(T_{SD}\) are more sensitive in the PFETs than the NFETs.

To analyze which channels mainly contribute to the \(I_{off}\), the \(I_{off}\) density of the U-shaped S/D NSFETS according to the \(T_{SD}\) is shown in Fig 3a. For both P-/NFETs, the \(I_{off}\) density of the NS channels does not change significantly regardless of the \(T_{SD}\). Meanwhile, the \(I_{off}\) of parasitic bottom channel (\(I_{off,pbt}\)) in parasitic bottom transistor (\(I_{pbt}\)) increases as the \(T_{SD}\) increases. The \(I_{off,pbt}\) increases with deeper \(T_{SD}\), because more S/D dopants inevitably diffuse into the PTS region and reduce the \(V_{th}\) of the \(I_{pbt}\). Especially, the \(I_{off,pbt}\) density of the PFETs severely increases above the \(T_{SD,critical}\) because the S/D dopant concentration of the \(I_{pbt}\) for the PFETs begins to increase remarkably above the \(T_{SD,critical}\). On the other hand, in the NFETs, the S/D dopant concentration linearly increases according to the \(T_{SD}\) increase and its amount is smaller than the PFETs’ (Fig. 3b). As a result, the PFETs are more sensitive than the NFETs to the \(T_{SD}\) variations and show larger \(I_{off,pbt}\) density and SCEs.

More details on the PFETs, a critical factor of high \(I_{off}\) sensitivity to the \(T_{SD}\) is channel stress (\(S_{ch}\)) differences between the NS channels and the \(I_{pbt}\). Fig. 4 shows transfer characteristics of the PFETs having the \(N_{SD}\) of \(1 \times 10^{20} \text{ cm}^{-3}\) according to the \(T_{SD}\) (note that the annealing condition has

---

**TABLE 1. Geometry parameters for Sub 5-nm node NSFETs.**

| Parameters          | Values [nm] |
|---------------------|-------------|
| Contact poly pitch  | CPP         |
| Sheet pitch         | SHP         |
| Gate length         | Lg          |
| Channel length      |            |
| (top/middle/bottom) |             |
| Lch                 | Ideal: 22 / 22 / 22 |
|                     | U-shaped: 18.5 / 20 / 22 (when \(T_{SD} = 0\)) |
| NS, Spacing thickness | TSD, Tsp   |
| NS width (top, bottom) | Wtop, Wbot |
| Inner spacer length | Lsp         |
|                     | Ideal S/D: 5 |
|                     | U-shaped S/D: 3 - 5 |
| Interfacial layer / HfO2 thickness | TIL, TIL |
| Excess S/D depth    | TSD         |
|                     | 0 - 14      |

---

**FIGURE 2.** Transfer characteristic of the ideal (black dashed line) and the U-shaped S/D NSFETs (color lines) according to the \(T_{SD}\) for both P-/NFETs. The \(I_{off}\) is fixed to 1 nA/\(\mu\text{m}\) in the ideal S/D NSFETs and in the U-shaped S/D having the \(T_{SD}\) of 0. Drain current is normalized to the SHP.
TABLE 2. SS, $I_{off}$, $I_{on}$, and $V_{th}$ of the sub 5-nm node NSFETs according to the $T_{SD}$.

| $T_{SD}$ [nm] | PFETs | NFETs |
|--------------|--------|--------|
|              | SS [mV/dec] | $V_{th}$ [V] | $I_{off}$ [nA/µm] | $I_{on}$ [nA/µm] | SS [mV/dec] | $V_{th}$ [V] | $I_{off}$ [nA/µm] | $I_{on}$ [nA/µm] |
| Ideal        | 79.8   | -0.272 | 1.00   | 1.13          | 73.9     | 0.244 | 1.00   | 1.14          |
| 0            | 86.2   | -0.294 | 1.00   | 0.99          | 77.8     | 0.264 | 1.00   | 1.32          |
| 2            | 87.0   | -0.293 | 1.10   | 0.98          | 78.0     | 0.260 | 1.16   | 1.34          |
| 4            | 90.4   | -0.292 | 1.54   | 0.98          | 78.3     | 0.256 | 1.34   | 1.37          |
| 6            | 240.9  | -0.161 | 425    | 1.05          | 78.7     | 0.252 | 1.60   | 1.39          |
| 8            | 400.1  | 0.571  | 4.92×10^4 | 1.26          | 80.7     | 0.248 | 2.17   | 1.41          |
| 10           | 1.37×10^3 | 4.17×10^3 | 1.63          | 105.5    | 0.241 | 7.77   | 1.44          |
| 12           | 8.83×10^3 | >> 0.571 | 1.06×10^6 | 2.11          | 203.0    | 0.220 | 73.4   | 1.48          |
| 14           | 1.67×10^4 | 1.74×10^6 | 2.59          | 275.9    | 0.127 | 646    | 1.53          |

FIGURE 3. (a) The $I_{off}$ density profile in the U-shaped S/D NSFETs according to the $T_{SD}$ for both P-/NFETs. The $tr_{pbt}$ is specified as black dashed box. (b) Boron and phosphorus concentrations in the $tr_{pbt}$ for the P-/NFETs, respectively. The concentrations is averaged over the volume from the interface between the interfacial layer and the PTS region to depth $T_{SD}+5$ nm (see the white cuboid in the inset).

been also revised accordingly to reproduce the experimental SS [8]). For accurate characteristic projection of the PFETs having the $N_{SD}$ of $1 \times 10^{20}$ cm$^{-3}$, S/D dopant profile along the NS channel is adjusted to 3-5 nm/dec (inset above in the Fig. 4) [38]–[42]. Note that the PFETs having lower $N_{SD}$ still suffer from severe upsurge of the $I_{off}$ as the $T_{SD}$ increases ($T_{SD,critical}$ is 6 nm). Typically, the compressive $S_{zz}$ of the PFETs retards boron diffusion into the silicon channels [43], and compressive $S_{zz}$ in the $tr_{pbt}$ is much smaller than NS channels. As a result, more S/D dopants can easily diffuse into the $tr_{pbt}$ than the NS channels (inset below in the Fig. 4), and it significantly degrades the SCEs, regardless the $N_{SD}$ of the PFETs.

B. ON-STATE ($|V_{GS}|=|V_{ds}|=|V_{dd}|$) ANALYSIS

Fig. 5 shows the $I_{on}$ density of the U-shaped S/D NSFETs according to the $T_{SD}$ in each NS channel and $tr_{pbt}$, where S/D stress effects are fully considered as [44]. Unlike the off-state operation, on-state operation shows different dependency on the $T_{SD}$ with device types. First in the PFETs, as the $T_{SD}$ increases, the $I_{on}$ density in the $tr_{pbt}$ ($I_{on,pbt}$) remarkably increases, whereas the $I_{on}$ densities in the NS channels decrease. On the other hand, in the NFETs, the $I_{on,pbt}$ density slightly increases, but the $I_{on}$ densities in the NS channels...
The $I_{on}$ densities of each NS channel and the $tr_{pbt}$ in the U-shaped S/D NSFETs according to the $T_{SD}$. The $I_{on}$ densities were extracted at the center of channel length and width. The legends are the same as the Fig. 2.

The $P_{SD}$ according to the $T_{SD}$. The $P_{SD}$ is extracted at the center of channel thickness and width of the top NS channel. Inset represents the definition of the $P_{SD}$ and the S/D contact resistance.

$rarely vary. In common, increasing S/D dopants diffusion into the PTS region with the deeper $T_{SD}$ induces the $I_{on,pbt}$ density increases for both P-/NFETs. The different dependencies of the $I_{on}$ densities on the $T_{SD}$ in the n-/p-channel NS channels are mainly analyzed with potential differences between the ends of the NS channels ($P_{SD}$). The $P_{SD}$ is defined as the valence (conduction) band energy difference between source and drain epitaxies of the PFETs (NFETs) and the $P_{SD}$ is extracted at the center of channel thickness and width of the NS channel (inset of Fig. 6). We investigated the $P_{SD}$ of the top NS only because the other two NS channels also have the same $P_{SD}$ tendencies as the top NS channel (Fig. 6). Increasing $I_{on,pbt}$ with the deeper $T_{SD}$ causes the larger potential reduction by the $R_{cont}$, so the $P_{SD}$ also reduces. Especially, the $I_{on,pbt}$ remarkably increases above the $T_{SD,\text{critical}}$ in the PFETs but increases a little in the NFETs. As a result, the $P_{SD}$ significantly decreases for the PFETs and lowers the $I_{on}$ densities of the NS channels, but the $P_{SD}$ does not vary much for the NFETs.

To reveal the origin of the $I_{on}$, we analyzed the $I_{on}$ contributions of each channel using the U-shaped S/D NSFETs with $T_{SD}$ of the $T_{SD,\text{critical}}$ (Fig. 7a). For comparison, the $I_{on}$ contributions of the ideal S/D NSFETs was also investigated in [45]. The $I_{on}$ contributions of each channel was evaluated by integrating the $I_{on}$ densities over the channel cross-section area at the center of the channels (see Fig. 1c). (b) Averaged carrier densities, mobilities and velocities of each channel in the U-shaped S/D NSFETs having the $T_{SD}$ = $T_{SD,\text{critical}}$ over the channel volumes surrounded by interfacial layers.
for the P-/NFETs, respectively), contrary to the case of the $I_{on}$ (Fig. 3). In addition, the bottom NS channel shows the smallest $I_{on}$ contribution for both P-/NFETs (28.3, 26.8 %, respectively).

The reason why each of the NS channels has the different $I_{on}$ contributions can be clarified using carrier density, mobility, and velocity. Typically, current density is proportional to the product of the carrier density and the velocity (Fig. 7b).

First of all, the carrier density is proportional to gate overdrive voltage ($|V_{gs}| - |V_{th}|$). More S/D dopant diffusion into the channels decreases the $|V_{th}|$ of each channel, resulting in higher carrier density at the same $|V_{gs}|$. The S/D dopant diffusion mainly occurs at S/D annealing steps due to its high annealing temperature. In this step, both the $L_{ch}$ and the $S_{zz}$ complexly affect the S/D dopant diffusion. The shorter $L_{ch}$, the deeper S/D dopants diffuse from the S/D to the channels, whereas compressive (tensile) $S_{zz}$ retards boron (phosphorus) diffusion into silicon channels [43], [46], [47]. Furthermore, the larger S/D volume beside top-side NS channel typically induces more compressive (tensile) $S_{zz}$ than the bottom-side channels in the PFETs (NFETs), but the $S_{zz}$ differences among the NS channels for the NFETs is negligible. Therefore, these two factors (the $L_{ch}$ and the $S_{zz}$) result in the S/D dopant concentrations in channels having order of top $>$ middle $\approx$ bottom (top $>$ middle$>$ bottom) NS channel in the PFETs (NFETs), and the carrier densities of each channels are also in this order. Secondly, carrier mobilities is critically affected by impurity scattering and the $S_{zz}$. The carriers in the top-side NS channel are mostly suffered from impurity scattering due to the largest amount of S/D dopants in the channel. Then, although the $S_{zz}$ can boost the carrier mobility, the carrier mobilities of each NS channels show almost inversely proportional to the amounts of impurities. Finally, the carrier velocities of the PFETs are the largest (smallest) in the top (bottom) NS channel because the shorter $L_{ch}$ makes stonger electric field along the channel direction. On the other hand, the carrier velocities of the NFETs are almost the same among the NS channels because the smaller (larger) carrier mobilities of the top (bottom) NS channel can be compensated (degraded) in carrier velocities by its larger (smaller) electric field. Therefore, for these reasons, $I_{on}$ contributions of each channel are determined like the Fig. 7a, and we summarized the dominant factors determining the $I_{on}$ contributions of each NS channel in Table 3.

### TABLE 3. Relative comparison of electrical parameters of each NS channels and dominant factors.

| Parameters | PFETs | NFETs |
|------------|-------|-------|
| Carrier density | Top $>$ Mid $=$ Bot | Top $>$ Mid $>$ Bot |
| S/D dopant diffusion & $S_{nn}$ | | |
| Carrier mobility | Top $<$ Mid $=$ Bot | Top $<$ Mid $<$ Bot |
| impurity scattering & $S_{nn}$ | | |
| Carrier velocity | Top $>$ Mid $>$ Bot | Top $=$ Mid $=$ Bot |
| carrier mobility & electric field | | |
| $I_{on}$ contribution | Top $>$ Mid $>$ Bot | carrier density $&$ velocity |

### FIGURE 8. (a) Oxide and parasitic capacitance components related to the $C_{gg}$ in the U-shaped S/D NSFETs. (b) The $C_{gg}$ and $C_{inv.pbt}$ of the NSFETs at $|V_{gs}|=|V_{ds}|=0.7$ V according to the $T_{SD}$.

#### C. AC PERFORMANCE ANALYSIS

In this section, the effects of the $I_{pbt}$ on AC operation are investigated comprehensively. In the NSFETs, the $C_{gg}$ consists of intrinsic gate oxide capacitance ($C_{ox}$) and parasitic capacitance ($C_{par}$) consisting of inversion capacitance of the $I_{pbt}$ ($C_{inv.pbt}$), inner ($C_{if}$) and outer fringe capacitances ($C_{of}$) (Fig. 8a). Fig. 8b shows the $C_{gg}$ and $C_{inv.pbt}$ of the NSFETs according to the $T_{SD}$. The $C_{gg}$ was extracted at frequency of 1 MHz, and $C_{inv.pbt}$ was extracted as follow:

1. Integrating inversion charge density in the PTS region over the PTS volume along the $V_{gs}$.
2. Differentiating the results of 1) over the $V_{gs}$, then getting the series-connected capacitance $C_{inv.pbt} + C_{ox}$.
3. Subtracting the $C_{ox}$ from the results of 2), then obtaining the $C_{inv.pbt}$ itself. Here, $C_{ox} = L_{g} \times W_{bot} \times 3.9 \times \varepsilon_{0}/\varepsilon_{0}$, where $\varepsilon_{0}$ is the vacuum permittivity and EOT is the effective oxide thickness with $T_{IL}$ of 1 nm and $T_{HF}$ of 2 nm.
The ideal S/D NSFETs have the smallest $C_{gg}$ due to their longest $L_{sp}$ and negligible $I_{on,pbt}$. The $C_{gg}$ of the U-shaped S/D NSFETs with the $T_{SD}$ of 0 are 9.7% and 7.8% larger than the ideal S/D NSFETs’ for the P-/NFETs, respectively. Meanwhile, the $C_{gg}$ of the U-shaped S/D NSFETs increases up to 7% as the $T_{SD}$ increases. Because gate oxide thickness and width of the $tr_{pbt}$ are not varied with the deeper $T_{SD}$, the $C_{ox}$ is not varied much, then increase of the $C_{par}$ dominantly induces the increase of the $C_{gg}$. Interestingly, the $C_{inv,pbt}$ is negligible when $T_{SD} = 0$, however, its contribution to the increase of the $C_{par}$ gradually increases as the $T_{SD}$ deepens.

The $P_{static} (= I_{off} \times |V_{dd}|)$ versus the $\tau_d (= C_{gg} \times |V_{dd}|/I_{on})$ of the NSFETs is also presented for SoC applications: low power (LP), standard performance (SP), and high performance (HP) (Fig. 9). The $I_{off}$ is fixed to $10^{-10} \text{A/} \mu\text{m}$ for the LP, $10^{-9} \text{A/} \mu\text{m}$ for the SP, and $10^{-7} \text{A/} \mu\text{m}$ for the HP. The ideal S/D NSFETs have the smaller $\tau_d$ than the U-shaped S/D NSFETs with the $T_{SD}$ of 0 because of their superior $I_{on}$ and smaller $C_{gg}$ (Table 2 and Fig. 8b). In the U-shaped NSFETs, the $\tau_d$ decreases with the deeper $T_{SD}$ due to the increasing rate of the $I_{on}$ being larger than the increasing rate of the $C_{gg}$ in both P/NFETs. However, the $P_{static}$ significantly increases as the $T_{SD}$ increases because tremendous amount of current flow in the $tr_{pbt}$ at off-state operation. Fortunately, when the $T_{SD}$ is less than the $T_{SD,critical}$, the variations of the $\tau_d$ and $P_{static}$ according to the $T_{SD}$ are small. In addition, the $\tau_d$ and $P_{static}$ of the PFETs are more sensitive to the $T_{SD}$ than those of the NFETs because the $tr_{pbt}$ of the PFETs drives more leakage current than the NFETs’. Furthermore, the LP is more sensitive to the $T_{SD}$ than the SP and the HP. Therefore, the $T_{SD}$ should be controlled less than $T_{SD,critical}$ to prevent the serious variations of the $\tau_d$ and $P_{static}$ especially in the PFETs than the NFETs and for the LP than the other applications.

**IV. CONCLUSION**

The $T_{SD}$ variations of the sub 5-nm node NSFETs were thoroughly investigated in terms of the DC/AC performances. The $tr_{pbt}$ is a critical killing factor of the NSFETs in advanced technology node. The deeper $T_{SD}$ induces more S/D dopant diffusion into the $tr_{pbt}$ and lowers the $V_{th}$ of $tr_{pbt}$, so the $I_{off}$ and the $I_{on}$ increase due to the $tr_{pbt}$. Especially, the $I_{off}$ remarkably increases above the $T_{SD,critical}(4, 10 \text{ nm for the P-/NFETs, respectively})$, and the $I_{off}$ of the PFETs is more severely degraded than that of the NFETs because the compressive $S_{zz}$ of the $tr_{pbt}$ is inevitably smaller than the $S_{zz}$ of the NS channels for the PFETs. At the $T_{SD,critical}$, the top NS channel is the largest contributor to the $I_{on}$ for both P-/NFETs, but fortunately, the $tr_{pbt}$ is the negligible contributor to the $I_{on}$ (0.5, 1.1% for the P-/NFETs, respectively). The $C_{gg}$ also increases due to the increase of the $C_{par}$ as the $T_{SD}$ deepens, especially, the contribution of the $C_{inv,pbt}$ to the $C_{par}$ also gradually increases. However, the $\tau_d$ decreases as the $T_{SD}$ increases due to the increasing rate of the $I_{on}$ being larger than the increasing rate of the $C_{gg}$ in both P/NFETs for all the SoC applications. Finally, the $P_{static}$ enormously varies compared to the $\tau_d$. The $\tau_d$ and $P_{static}$ are more sensitive to the $T_{SD}$ variations in the PFETs than in the NFETs and for the LP than the other applications. Therefore, the sub 5-nm node NSFETs ensures immune to the $T_{SD}$ variations if the $I_{off}$ can be controlled only.

**REFERENCES**

[1] S. E. Thompson et al., “A 90-nm logic technology featuring strained-silicon,” IEEE Trans. Electron Devices, vol. 51, no. 11, pp. 1790–1797, Nov. 2004.

[2] P. Bai et al., “A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57 μm2 SRAM cell,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2004, pp. 657–660.

[3] K. Misry et al., “A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging,” in IEDM Tech. Dig., Washington, DC, USA, Dec. 2007, pp. 247–250.

[4] P. Packan et al., “High performance 32nm logic technology featuring 2nd generation high-k+ metal gate transistors,” in IEDM Tech. Dig., Dec. 2009, pp. 659–662.

[5] C. Hu, “Future CMOS scaling and reliability,” Proc. IEEE, vol. 81, no. 5, pp. 682–689, May 1993.

[6] C. Auth et al., “A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors,” in Proc. Symp. VLSI Technol. (VLSIT), Honolulu, HI, USA, Jun. 2012, pp. 131–132.

[7] S. Natarajan et al., “A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm2/SRAM cell size,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2014, pp. 71–73.

[8] C. Auth et al., “A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2017, pp. 673–676.

[9] R. Xie et al., “A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2016, pp. 2.7.1–2.7.4.

[10] D.-W. Kim, “CMOS transistor architecture and material options for beyond 5nm node,” in Proc. Symp. VLSI Technol. Short Course, Honolulu, HI, USA, Mar. 2018, pp. 2–57.

[11] N. Loubet et al., “Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET,” in Proc. Symp. VLSI Technol., Kyoto, Japan, Jun. 2017, pp. 230–231.
JUN-SIK YOON (Member, IEEE) received the B.S. degree in electrical engineering and the Ph.D. degree in creative IT engineering from the Pohang University of Science and Technology (POSTECH), South Korea, in 2012 and 2016, respectively. He was a Postdoctoral Research Fellow of POSTECH, from 2016 to 2018, where he has been a Research Assistant Professor in electrical engineering, since 2019. His research interest includes characterization and simulation of advanced nanoscale devices (fin, gate-all-around, tunneling, and nanosheet FETs) and applications (chemical sensors and solar cells).

SEUNGHWAN LEE (Student Member, IEEE) received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), South Korea, in 2018, where he is currently pursuing the M.S. degree in electrical engineering. His research interest includes characterization and compact modeling of multigate field-effect transistors (FinFETs, nanowire FETs, and nanosheet FETs).

ROCK-HYUN BAEK (Member, IEEE) received the B.S. degree in electrical engineering from Korea University, in 2004, and the M.S and Ph.D. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2006 and 2011, respectively. He was a Postdoctoral Researcher and a Technical Engineer with SEMATECH, Albany, NY, USA, from 2011 to 2015. He was a Senior Device Engineer with the SAMSUNG R&D Center (Pathfinding TEAM), South Korea, from 2015 to 2017. Since 2017, he has been an Assistant Professor in electrical engineering with POSTECH. His research interests include technology benchmark by characterization, simulation, and modeling of advanced devices and materials (fin, gate-all-around, nanosheet FETs, 3D-NAND, 3DIC, SiGe, Ge, and III-V).