Implementation of an FPGA-Based Current Control and SVPWM ASIC with Asymmetric Five-Segment Switching Scheme for AC Motor Drives

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Abstract: This paper presents the design and implementation of an application-specific integrated circuit (ASIC) for a discrete-time current control and space-vector pulse-width modulation (SVPWM) with asymmetric five-segment switching scheme for AC motor drives. As compared to a conventional three-phase symmetric seven-segment switching SVPWM scheme, the proposed method involves five-segment two-phase switching in each switching period, so the inverter switching times and power loss can be reduced by 33%. In addition, the produced PWM signal is asymmetric with respect to the center-symmetric triangular carrier wave, and the voltage command signal from the discrete-time current control output can be given in each half period of the PWM switching time interval, hence increasing the system bandwidth and allowing the motor drive system with better dynamic response. For the verification of the proposed SVPWM modulation scheme, the current control function in the stationary reference frame is also included in the design of the ASIC. The design is firstly verified by using PSIM simulation tool. Then, a DE0-nano field programmable gate array (FPGA) control board is employed to drive a 300W permanent-magnet synchronous motor (PMSM) for the experimental verification of the ASIC.

Keywords: SVPWM ASIC; asymmetric five-segment switching; AC motor drives; current control; FPGA control

1. Introduction

The AC motor drives, including induction motors (IM), permanent-magnet synchronous motor (PMSM) drives, synchronous reluctance motors (SynRM), and others, have been very popular, being applied to electric vehicles, railway traction engines, and industrial applications such as CNC tools and robots, because they have higher power density and efficiency as compared to DC motor drives [1–4]. Since the AC motor is a time-varying, multi-variable, and nonlinear control system with very complicated dynamic characteristics, it can be reduced to a simpler linear control system by using the field-oriented vector control method [5–11]. In vector-controlled AC motor drives, various pulse-width modulation (PWM) techniques exist to determine the inverter switch-on and switch-off instants from the control output modulating signals. Popular examples include sinusoidal PWM (SPWM), hysteresis PWM, and space-vector PWM (SVPWM). Among them, the SPWM method generates the inverter switching signals by comparing the modulating signals with a common triangular carrier wave, in which the intersection points determine the switching points of the inverter power devices [12,13]. The hysteresis PWM method controls the inverter output currents to track the reference inputs within the hysteresis band, but with various switching frequencies [14,15]. The SVPWM method is based on the concept of voltage vector space, which can be divided into six sectors, and calculates
the switch dwelling or firing time in each sector to generate the PWM signals [16–40]. The relationship between SVPWM and SPWM was presented in [18], which indicated that the SVPWM can be viewed as a particular form of asymmetric regular-sampled PWM. In [24], the relationship between SVPWM and three-phase SPWM was also analyzed and the implementation of them in a closed-loop feedback converter was discussed as well. The SVPWM technique is the preferred approach in most applications due to the higher voltage utilization and lower harmonic distortion (THD) than the other two methods, and hence it can extend the linear range of the vector-controlled AC motor drives. Furthermore, sensorless and direct torque control (DTC) cooperating with an SVPWM scheme for a flux-modulated permanent-magnet wheel motor and induction motor has been described owing to several advantages, such as low torque/flux ripples in motor drive and reduced direct axis current, over the conventional hysteresis direct torque control method when the motor is operated at a light or a sudden increased load [34,37–40]. The SVPWM scheme has also been extensively applied to the control of a five-phase permanent-magnet motor and multilevel inverters [35,36].

Different SVPWM techniques can be used for three-phase inverters according to the choice of the null vector on the voltage space and the number of samplings during a PWM switching period. They can be divided into seven-segment, five-segment, and three-segment techniques for the switching sequences and the choice of null vector, and classified into symmetric and asymmetric techniques according to the number of samplings during a PWM switching period as well. For the symmetric technique, the sampling period is equal to the switching period, while the sampling period is one half of the switching period for the asymmetric technique. So, the asymmetric methods have only 50% switching action in each switching period as compared with symmetric methods, and hence the sampling frequency of the current control can be doubled at a certain switching frequency.

In [28], three SVPWM strategies, including symmetric seven-segment technique, symmetric five-segment technique, and asymmetric three-segment technique, were compared through simulation analysis. The switching loss of the three-segment scheme is the lowest and the seven-segment scheme performs better in terms of the THD of the output line voltage.

Figure 1 shows the rotor flux-oriented control (RFOC) structure of a PMSM motor drive with a SVPWM modulation scheme, in which an asymmetric five-segment switching is proposed rather than the conventional symmetric seven-segment switching so as to double the sampling frequency and reduce the switching loss. This control structure, from the inner to the outer loops, includes the SVPWM modulation, current control loop, torque and flux control loops, and speed control loop. Conventionally, the execution of all the control tasks is performed by using a high-performance microprocessor or dual digital signal processor (DSP) [21,41–42]. It may take a lot of computation time for the microprocessor or DSP because all the computation of the tasks is very complicated. If the computation of the current control and the SVPWM tasks can be executed by a field programmable gate array (FPGA) device, the computation load can be greatly reduced [16–17,22,25,30]. In such cases, the microprocessor or DSP can have enough time to process higher level tasks, such as position control, motion control, adaptive, fuzzy, or neural-network learning and intelligent control [43]. In [17], an eight-bit SVPWM control IC was realized with a symmetrical five-segment switching scheme, but without current control function included in the chip. In [22], a microcoded machine with a 16-bit computational ALU unit and control sequencer was designed in an FPGA for the execution of the current control and SVPWM modulation of an induction motor with symmetrical seven-segment switching scheme. However, the microcoded machine structure is very complicated.
This paper describes the design and implementation of an application-specific integrated circuit (ASIC) for a discrete-time current control and space-vector pulse-width modulation (SVPWM) with asymmetric five-segment switching scheme AC motor drives. It can not only reduce the computation load of a microprocessor or DSP, but also reduce the power transistor switching loss of the inverter. Traditionally, the current control loop is performed in the synchronously $d-q$ rotating reference frame [3–7]. However, as indicated in Figure 1, the presented current control loop is performed in the stationary reference frame rather than the synchronously rotating reference frame in order to simplify the computation complexity in the FPGA device. Furthermore, because the current reference commands can be updated two times during one switching period, the current control system can also increase the sampling frequency two times so as to increase the bandwidth.

The algorithm of the proposed current control and asymmetric five-segment switching SVPWM scheme was firstly verified by using PSIM simulation tool as applied to the current control of a PMSM AC motor. The proposed SVPWM scheme and the current controller function were implemented on a DE0-nano control board with Altera Cyclone IV E FPGA device for the experimental verification.

This paper is organized as follows. The principle of the asymmetric five-segment switching SVPWM modulation scheme is described in Section 2. The simulation verification in PSIM simulation tool is analyzed in Section 3 and the FPGA implementation and the experimental results are presented in Section 4. A discussion is then given in Section 5. Finally, the conclusion is given in Section 6.

2. The Principle of the Asymmetrical Five-Segment Switching SVPWM Modulation

![Figure 1. The rotor flux-oriented control (RFOC) structure of a permanent-magnet synchronous motor (PMSM) AC motor drive.](image-url)
Firstly, as shown in Figure 2, for a three-phase PWM inverter of Y-connected AC motor with neutral point \( n \), the three-phase stator voltages with respect to the inverter ground can be written as

\[
\begin{align*}
V_{a0} & = V_{an} + V_{n0} \\
V_{b0} & = V_{bn} + V_{n0} \\
V_{c0} & = V_{cn} + V_{n0}
\end{align*}
\]  

(1) (2) (3)

where \( V_{an}, V_{bn}, \) and \( V_{cn} \) are the three-phase voltages with respect to the neutral point of the motor, and \( V_{n0} \) is the neutral-point voltage with respect to the inverter ground.

![Figure 2. The pulse-width modulation (PWM) inverter circuit for a Y-connected AC motor.](image)

For balanced three-phase supply, it can be written as

\[
V_{an} + V_{bn} + V_{cn} = 0
\]

(4)

Thus, by adding (1)–(3) with the condition of (4), the neutral-point voltage with respect to the inverter ground, \( V_{n0} \), can be written as

\[
V_{n0} = \frac{1}{3}(V_{a0} + V_{b0} + V_{c0})
\]

(5)

Substituting (5) into (1)–(3) yields

\[
\begin{bmatrix}
V_{an} \\
V_{bn} \\
V_{cn}
\end{bmatrix}
= \begin{bmatrix}
\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\
-\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\
\frac{1}{3} & -\frac{1}{3} & \frac{2}{3}
\end{bmatrix}
\begin{bmatrix}
V_{a0} \\
V_{b0} \\
V_{c0}
\end{bmatrix}
\]

(6)
Secondly, because the three-phase stator voltages are dependent upon (4), the inputs of the SVPWM circuit can be reduced from the three-phase variables into \( \alpha-\beta \) two-axes components with the Clarke transformation given by (7).

\[
\begin{bmatrix}
  v_\alpha \\
  v_\beta
\end{bmatrix} =
\begin{bmatrix}
  1 & 0 & 0 \\
  0 & 1/\sqrt{3} & -1/\sqrt{3}
\end{bmatrix}
\begin{bmatrix}
  v_{a0} \\
  v_{b0} \\
  v_{c0}
\end{bmatrix}
\]

(7)

where \( v_\alpha \) and \( v_\beta \) are the \( \alpha-\beta \) axes component voltages in the stationary reference frame. Substituting (6) into (7) yields

\[
\begin{bmatrix}
  v_\alpha \\
  v_\beta
\end{bmatrix} =
\begin{bmatrix}
  2/3 & -1/3 & -1/3 \\
  0 & 1/\sqrt{3} & -1/\sqrt{3}
\end{bmatrix}
\begin{bmatrix}
  v_{a0} \\
  v_{b0} \\
  v_{c0}
\end{bmatrix}
\]

(8)

Thus, using (8), one can get the eight output voltage vectors, \( V_0 - V_7 \), corresponding to the eight switching states of the inverter, as shown in Table 1. The resulted space vector diagram is shown in Figure 3, which is divided into six sectors from Sector I to Sector VI. As can be seen, among the eight voltage vectors, \( V_0 \) and \( V_7 \) are the null vectors and \( V_1 - V_6 \) are located on the six corners of the hexagonal diagram.

### Table 1. The eight space voltage vectors.

| Inverter Switch Status \((S_u, S_v, S_w)\) | Three-Phase Stator Voltages with respect to ground \([v_{a0}, v_{b0}, v_{c0}]\) | Space Vectors \([v_\alpha, v_\beta]\) |
|-----------------------------------------|-----------------------------------------------|-----------------------------------------------|
| (1, 0, 0) | \([V_{dc}, 0, 0]\) | \(V_1 = \left[ \frac{2V_{dc}}{3}, 0 \right] \) |
| (0, 1, 0) | \([0, V_{dc}, 0]\) | \(V_3 = \left[ -\frac{V_{dc}}{3}, \frac{V_{dc}}{\sqrt{3}} \right] \) |
| (1, 1, 0) | \([V_{dc}, V_{dc}, 0]\) | \(V_2 = \left[ \frac{V_{dc}}{3}, \frac{V_{dc}}{\sqrt{3}} \right] \) |
| (0, 0, 1) | \([0, 0, V_{dc}]\) | \(V_5 = \left[ -\frac{V_{dc}}{3}, -\frac{V_{dc}}{\sqrt{3}} \right] \) |
| (1, 0, 1) | \([V_{dc}, 0, V_{dc}]\) | \(V_6 = \left[ \frac{V_{dc}}{3}, -\frac{V_{dc}}{\sqrt{3}} \right] \) |
| (0, 1, 1) | \([0, V_{dc}, V_{dc}]\) | \(V_4 = \left[ -\frac{2V_{dc}}{3}, 0 \right] \) |
| (1, 1, 1) | \([V_{dc}, V_{dc}, V_{dc}]\) | \(V_7 = [0, 0] \) |
| (0, 0, 0) | \([0, 0, 0]\) | \(V_0 = [0, 0] \) |
Figure 3. Inverter’s eight output voltage space vectors.

The switching waveform generations of the inverter for driving an AC motor can be accomplished by rotating a reference voltage vector around the vector space. Any instance of the reference voltage vector can be produced by the two nearest adjacent vectors and a null vector in an arbitrary sector. For example, as shown in Figure 4, for providing the reference voltage vector $V_s$ in Sector I to the motor, the voltage-second balance equation in this sector determines the time length of the two adjacent active inverter states in the following:

$$V_s T = V_A T_1 + V_B T_2$$  \hspace{1cm} (9)

where $T_1$ and $T_2$ are the dwelling time length for $V_1$ and $V_2$, respectively, and $T$ is the sampling period, which is one half of the inverter switching period. In order to get the solution of $T_1$ and $T_2$ in (9), it follows that

$$\begin{bmatrix} v_a \\ v_\beta \end{bmatrix} = \frac{2}{3} V_{dc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_1 + \frac{1}{2} \sqrt{3} v_\beta T_2$$  \hspace{1cm} (10)

Thus, $T_1$ and $T_2$ can be, respectively, solved as

$$T_1 = \frac{\sqrt{3} T}{V_{dc}} (\frac{\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta)$$  \hspace{1cm} (11)

and

$$T_2 = \frac{\sqrt{3} T}{V_{dc}} v_\beta$$  \hspace{1cm} (12)
\[
\begin{bmatrix}
  v_a \\
v_\beta
\end{bmatrix} = V_s \begin{bmatrix}
  \cos \gamma \\
  \sin \gamma
\end{bmatrix}
\]  

(13)

then (11) and (12) can be rewritten as the following equations [18]:

\[
T_1 = Ta \frac{2}{\sqrt{3}} \sin \left( \frac{\pi}{3} - \gamma \right)
\]  

(14)

\[
T_2 = Ta \frac{2}{\sqrt{3}} \sin (\gamma)
\]  

(15)

where

\[
a = \frac{V_s}{\frac{2}{3} V_{dc}}
\]  

(16)

Similarly, the switching time interval in the other sectors can be derived. Table 2 summaries the results, in which the condition for sector number selection is also illustrated.

![Diagram](image)

Figure 4. Determination of the switching time in Sector I.

| Sector | Sector Selection | \( T_1 \) | \( T_2 \) |
|--------|------------------|----------|----------|
| I      | \( v_\alpha \geq 0, \ 0 \leq v_\beta < \sqrt{3} v_\alpha \) | \( \frac{\sqrt{3} T}{V_{dc}} (\frac{\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta) \) | \( \frac{\sqrt{3} T}{V_{dc}} v_\beta \) |
| II     | \( v_\beta \geq 0, \ v_\beta \geq \sqrt{3} | v_\alpha | \) | \( \frac{\sqrt{3} T}{V_{dc}} (-\frac{\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta) \) | \( \frac{\sqrt{3} T}{V_{dc}} (\frac{\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta) \) |
| III    | \( v_\alpha \leq 0, \ 0 \leq v_\beta < -\sqrt{3} v_\alpha \) | \( \frac{\sqrt{3} T}{V_{dc}} v_\beta \) | \( \frac{\sqrt{3} T}{V_{dc}} (-\frac{\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta) \) |
| Sector | Conditions | Pulse Sequence |
|--------|-------------|----------------|
| IV     | $v_\alpha \leq 0$, $\sqrt{3}v_\alpha \leq v_\beta < 0$ | $\frac{-\sqrt{3}T}{V_{dc}} v_\beta$, $\frac{\sqrt{3}T}{V_{dc}} \left(\frac{-\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta\right)$ |
| V      | $v_\beta \leq 0$, $v_\beta \leq -\sqrt{3}|v_\alpha|$ | $\frac{\sqrt{3}T}{V_{dc}} \left(\frac{-\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta\right)$, $\frac{\sqrt{3}T}{V_{dc}} \left(\frac{-\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta\right)$ |
| VI     | $v_\alpha \geq 0$, $-\sqrt{3}v_\alpha \leq v_\beta < 0$ | $\frac{\sqrt{3}T}{V_{dc}} \left(\frac{\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta\right)$, $\frac{-\sqrt{3}T}{V_{dc}} v_\beta$ |

For minimizing the number of switchings in a switching period, the asymmetrically alternating-reversing pulse sequence with five-segment ($V_0 - V_1 - V_2 - V_3 - V_4$) switching technique is employed without using the null vector $V_7$, as shown in Figure 5a. The pulse patterns for two consecutive sampling intervals can be configured by beginning with the null vector $V_0$ on the $kT$ sampling time and also by ending with the same null vector $V_0$ on the $(k+1)T$ sampling time, where $k = 1, 3, 5, \ldots$. The time length $T_0$ on the $kT$ and $(k+1)T$ sampling time intervals can be different, either for $T_1$ or $T_2$. Therefore, the PWM pulses are asymmetric with respect to the center point of the switching period. The technique benefits from one of the inverter legs not switching during a full switching period, only one inverter leg switching at a time, and only two commutations per sampling period. Thus, the number of switchings in a switching period is four and is less than the conventional symmetric seven-segment SVPWM method, in which the number of switchings in a switching period is six.

Furthermore, as can be seen from Table 2, the switch dwelling time length $T_1$ and $T_2$ are a function of the component voltages, $v_\alpha$ and $v_\beta$, the sampling period, $T$, and the DC bus voltage, $V_{dc}$. The calculations of the functions are very simple, and hence can be easily carried out by the FPGA-based digital hardware. The pulse waveforms of the proposed asymmetric five-segment switching SVPWM scheme in other sectors are also shown in Figure 6. However, there may be the cases of the reference voltage vector travelling across the sector on the trailing sampling interval. In this case, the sector pulse pattern in the leading sampling interval must change to the next sector pulse waveforms on the trailing sampling interval. Figure 6 illustrates a pulse waveform crossing from Sector I to the other five sectors and from Sector II to I on the trailing sampling interval.
Figure 5. The asymmetric five-segment switching space-vector pulse-width modulation (SVPWM) pulse waveform in each sector: (a) Sector I; (b) Sector II; (c) Sector III; (d) Sector IV; (e) Sector V; (f) Sector VI.
Figure 6. The pulse waveforms of sector crossing on the trailing sampling time: (a) Sector I to II, (b) Sector I to III, (c) Sector I to IV, (d) Sector I to V, (e) Sector I to VI, (f) Sector II to I.

The scaled reference commands can be routed to the circuit block for the calculation of the dwelling time duration $T_1$ and $T_2$ in each sector for generating the PWM signals [17]. However, for reducing the computation complexity, an alternative method is used by calculating the firing time, which is defined as the time interval from the start to the leading edge of the PWM pulse. For example, in Sector I, the PWM firing times for the switches $S_u$, $S_v$, and $S_w$ in the $kT$ sampling period can be obtained as follows:

$$f_u = T_0$$

$$f_u = T - \frac{\sqrt{3}T}{V_{dc}} \left( \frac{\sqrt{3}}{2} v_x + \frac{1}{2} v_y \right)$$

(17)
\[
f_v = T_0 + T_1 = T_s - T_2
\]
\[
= T - \frac{\sqrt{3}T}{V_{dc}} v_\beta
\]
\[
f_w = T
\]
(28)

where \( T_0 = T - T_1 - T_2 \). The resulting equations for the PWM firing time in another sector can be obtained in the same way. Table 3 summarizes the results. As can be seen, the firing-time equations in Sector I are the same as in Sector II. They are the same in Sector III and IV and in Sector V and VI as well. Thus the circuit realization for the sectors with the same firing-time equation can share the same circuit as each other. This can simplify the circuit complexity for the implementation of the ASIC. As shown in Figure 7, the PWM pulse pattern on each phase can be generated by comparing the firing-time signal with a common center-symmetrical triangular wave with amplitude of \( T \) and period of \( 2T \), which can be implemented by an up-down counter. The pulse is low when the firing-time signal is larger than the magnitude of the triangular wave and is high otherwise.

Table 3. PWM firing time calculation in each sector.

| Sector | \( f_u \) | \( f_v \) | \( f_w \) |
|--------|----------|----------|----------|
| I, II  | \( T - \frac{\sqrt{3}T}{V_{dc}} \left( \frac{\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta \right) \) | \( T - \frac{\sqrt{3}T}{V_{dc}} v_\beta \) | \( T \) |
| III, IV| \( T \) | \( T - \frac{\sqrt{3}T}{V_{dc}} \left( -\frac{\sqrt{3}}{2} v_\alpha + \frac{1}{2} v_\beta \right) \) | \( T - \frac{\sqrt{3}T}{V_{dc}} \left( -\frac{\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta \right) \) |
| V, VI  | \( T - \frac{\sqrt{3}T}{V_{dc}} \left( \frac{\sqrt{3}}{2} v_\alpha - \frac{1}{2} v_\beta \right) \) | \( T \) | \( T + \frac{\sqrt{3}T}{V_{dc}} v_\beta \) |

Figure 7. The SVPWM signal generation on one phase.

3. Simulation Verification Using PSIM
Figure 8 shows the simulation verification of the proposed asymmetric five-segment switching SVPWM modulation scheme to drive a PMSM motor by using the PSIM simulation tool, in which the PMSM motor model (Sinano 7CB30-2DE6FKS) was constructed, as shown in Figure 8b. In this simulation, the sampling period is \( T = 40 \mu s \), the DC bus voltage is \( V_{dc} = 40 \text{V} \), \( v_{a} = 23\cos(40\pi t) \), and \( v_{b} = 23\sin(40\pi t) \). The SVPWM modulation scheme algorithm was written in C language inside the C block function of PSIM with the flowchart shown in Figure 9. Figure 10 shows the simulation results of current and speed responses, the three-phase firing-time signals, and the firing-time signal vector trajectory with the 20 Hz voltage reference inputs given above and 0.3 Nm load torque at 0.1 s. As can be seen, the speed is 31.4 rad/s in the steady-state, which can verify the correctness of the algorithm of the proposed SVPWM modulation scheme.

Figure 11 shows the simulation verification of the discrete-time current control of the PMSM motor using the proposed SVPWM scheme. A discrete-time proportional-integral (PI) controller is designed with the pulse transfer function in (20) and the zero-order hold with sampling frequency of 25 kHz, which is two times of the inverter switching frequency. As can be seen, the current responses can track the current reference with the amplitude of 3A and frequency of 20 Hz.

\[
H(z) = \frac{k_p + k_i T - k_p z^{-1}}{1 - z^{-1}}
\] (20)
Figure 8. Simulation verification of the SVPWM scheme: (a) simulation model using C block, (b) PMSM motor model with pole number equal to 8.
Figure 9. Flowchart of the proposed asymmetric five-segment switching SVPWM scheme algorithm.
Figure 10. Simulation results with 0.3 Nm load torque at 0.1 s: (a) the reference voltages, current and speed responses, (b) the three-phase firing-time signals, (c) the firing-time signal vector trajectory.
Figure 11. Simulation verification of the current control with 0.3 Nm load torque at 0.4 s: (a) simulation model, (b) the reference currents, current, and speed responses.

4. FPGA Implementation

A DE0-Nano FPGA control board by Terasic Inc. with Altera Cyclone IV-E device (EP4CE22F17C6) was employed for the implementation and experiment verification of the proposed current control and SVPWM ASIC for driving a PMSM servo motor (Sinano) with rated power of 300 W. Figure 12 shows the designed SVPWM ASIC structure with
optional current control function included. The DE0-Nano board includes a 50 MHz oscillator, which can be used as a source clock to the designed multi-clock generation circuit to give various frequency clock signals, such as 2.5 MHz, 200 kHz, 100 kHz, and 10 kHz, for the design of the ASIC. A cosine and a sine look-up table, each with 500 words and 10 bits/word, were created by using LPM_ROM function to generate the voltage references, $v_a$ and $v_b$, in which the frequency can be determined through the modulus-500 counter as a frequency divider. The voltage references then can be used as the inputs of the sector selection circuit according to Table 2 and the inputs of the firing time calculation circuit in each sector according to Table 3. Because some firing time equations are the same, they can be divided into three groups. The 3:1 multiplexers are used in order to select the three firing-time signals $f_a$, $f_b$, and $f_w$ in each sector. The 50 MHz clock is used as the input of an up-and-down counter, which counts up from zero to 2000 and then counts down to zero, for the generation of a triangular carrier signal with an 80 $\mu$s period. The three firing time signals are then compared with the common triangular carrier counter value, respectively, to generate the three-phase SVPWM signals. A dead-time interval of 2 $\mu$s in each phase is also inserted to generate the six gate signals to drive the inverter. A SPI-DAC interface to a DAC7513 converter was also designed to illustrate the three-phase firing time signals on the oscilloscope.

Figure 12. The SVPWM application-specific integrated circuit (ASIC) structure with optional current control function.

The SVPWM ASIC in the FPGA chip was designed, as shown in Figure 13, by using Altera Quartus II software development system of version 13.1. The experimental results of the SVPWM three-phase switching signals in each sector are shown in Figure 14. They are consistent with the expected pulse waveforms in Figure 5. The open-loop experiment result of the firing-time signal vector trajectory in a steady state is shown in Figure 15, which is also consistent with the simulation result in Figure 10c. Figure 16 shows the experimental result of the open-loop current vector trajectory in steady state with the SVPWM scheme. Two of the three-phase currents are sensed by using two LEM-55P current sensors and filtered through low-pass filters. The filtered currents are shifted up 1.65 V, being the inputs to an ADC128S022 A/D converter, in which the input voltage range is between zero and 3.3 V, for the feedback of the PI current control function with 25 kHz sampling frequency.
Figure 13. FPGA implementation of the proposed SVPWM scheme by using Quartus II version 13.1 tool.

Figure 14. Experiment verification of the three-phase switching signals in each sector of the proposed SVPWM scheme: (a) Sector I; (b) Sector II; (c) Sector III; (d) Sector IV; (e) Sector V; (f) Sector VI.
For saving the hardware resources, the computation architecture of the PI controller in the ASIC is shown in Figure 17, which has a control unit and a data path, which contains a 12-bit adder/subtractor, a 12-bit multiplier, and a limiter. The control unit is a finite state machine (FSM) which generates the control signals to the data path to control the computation procedures of the PI controller. The computation procedures of the PI controller according to the pulse transfer function in (20) are shown in Figure 18. There are five steps (s1–s5) for the computation of the PI control function. For the 25 kHz sampling frequency, the input clock frequency for the PI control function is 200 kHz. Therefore, there are eight clocks, in which three clocks are used for waiting state, needed to accomplish the computation of the PI controller. Figure 19 shows the experimental result for the closed-loop current vector trajectory in steady state with different DC bus voltage values. As can be seen, it can be a circular in the range from 55 to 63 V.
Figure 17. The computation architecture of the ASIC.

Figure 18. The computation procedures of the proportional-integral (PI) controller.
5. Discussion

Several practical aspects for the implementation of the proposed current control and SVPWM ASIC are discussed as follows:

Firstly, as shown in Figure 7, the firing-time signals are the modulating signals and used to compare with a common center-symmetrical triangular carrier wave for generating the PWM gating signals of the inverter in the proposed SVPWM scheme. This is different from the conventional SPWM implementation method, in which the sinusoidal control outputs are the modulating signals. For convenience, the firing time equation of $f_v$ in Table 3 is rewritten as follows:

$$f_v = T - \frac{\sqrt{3} T}{V_{dc}} v_{\beta} = T \left(1 - \frac{\sqrt{3}}{V_{dc}} v_{\beta}\right)$$

(21)

The second term on the right-hand side of the equals sign has a relationship with the duty ratio of the gating signal expressed as

$$d_v = \frac{\sqrt{3}}{V_{dc}} v_{\beta}$$

(22)

Because the duty ratio is $0 \leq d \leq 1$, it follows that

$$v_{\beta} \leq \frac{V_{dc}}{\sqrt{3}}$$

(23)
So, the maximum value of the control signals $v_{\beta}$ or $v_{\alpha}$ is $V_{dc}/\sqrt{3}$ and is larger than $V_{dc}/2$, which is the maximum value of the modulating signals in SPWM method. Thus, as is well known, the SVPWM method has higher voltage utilization by about 115% than the SPWM modulation method.

Secondly, the term $\sqrt{3}/V_{dc}$ in (22) can be seen as the gain from the control signal $v_{\beta}$ to the duty ratio to generate the gating signal in the SVPWM modulation scheme. Thus, this gain can be expressed as

$$ K_{svpwm} = \frac{d_{c}}{v_{\beta}} = \frac{\sqrt{3}}{V_{dc}} $$

(24)

It was found that this SVPWM gain can be included in the PI current controller parameters. So, although the firing time equations are relative to the dc bus voltage, the multiplication of the SVPWM gain to the control output signal $v_{\beta}$ is not necessary for the implementation of the firing-time signal. That means the small perturbation of the DC bus voltage will not affect the performance of the current control and SVPWM ASIC. As can be seen from the experimental results in Figure 19, the closed-loop current vector trajectory in steady state can be a circular for the dc bus voltage of 55 and 63 V, respectively. This finding makes the implementation circuit simpler.

Thirdly, although it is the digital hardware circuit for the computation of the current control and SVPWM scheme, the timing sequence during the sampling interval from the sampling of the feedback currents to the current control and firing-time signal output must be considered for the synchronization, as shown in Figure 20. The computation of the timing signals must be completed before the next sampling time. The resulted firing-time signal values are then loaded into the PWM signal generation circuit for the comparison with an up-down counter at the next sampling time in which the counter starts to count up from zero or count down from 2000.

![Figure 20. The timing sequence of sampling and loading for the proposed current control and SVPWM scheme.](image)
Fourthly, the conventional SVPWM scheme including the symmetric seven-segment technique, symmetric five-segment technique, and asymmetric three-segment technique are shown in Figure 21. As can be seen, the symmetric five-segment technique has four switching times and is the lowest during a switching period, so the switching loss of the scheme is significantly reduced in comparison with the others. However, in the asymmetric three-segment technique, the sampling frequency can be doubled at a certain switching frequency. The proposed asymmetric five-segment technique can not only have the advantages of minimum switching times, but also can double the sampling frequency in the current control loop so as to improve the control performance.

![Diagram of SVPWM switching sequences](image)

**Figure 21.** SVPWM switching sequences: (a) symmetric 7-segment, (b) symmetric 5-segment, (c) asymmetric 3-segment.

### 6. Conclusions

In this work, the design and implementation of an FPGA-based SVPWM ASIC with an asymmetric five-segment switching scheme for AC motor drives have been performed. The inverter switch dwelling and firing times on each sector have been derived. It was found that the firing-time equations in Sector I and II are the same. They are the same in Sector III and IV and in Sector V and VI as well. These finding allow us to simplify the circuit complexity for the implementation of the ASIC. Compared with the conventionally symmetric seven-segment three-phase switching scheme, the inverter switching times and power loss of this proposed scheme can not only be reduced by 33%, but also the asymmetric characteristics mean that the reference voltage command signal can be given in the half period of the PWM switching time interval. Therefore, one can design the closed-loop current control while doubling the sampling frequency, hence increasing the bandwidth, and allowing the motor drive system with better dynamic response. For the verification of the proposed SVPWM modulation scheme, the closed-loop current control function in the stationary reference frame has been also included in the design of the ASIC. The ASIC function is firstly verified by using the PSIM simulation tool. Then, a DE0-nano FPGA control board has been employed to drive a 300 W PMSM AC motor for the experimental verification. The simulation and experimental results show the performance of the proposed SVPWM ASIC both in the open-loop pulse-width modulation and in the current control loop. The proposed current control and SVPWM ASIC can not only be used in PMSM motor drives, but can also be applied in other AC motor drives.

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