About the choice of initial voltages in the synchronous sense amplifier for CMOS memory

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Abstract. It was shown that the choice of initial voltage at the nodes of CMOS memory synchronous sense amplifiers has a significant effect on the amplifier data sensitivity. The research of the sense amplifier sensitivity with various initial conditions was performed. According to the results we gave some recommendations about the choice of initial voltages in synchronous sense amplifiers.

1. Introduction
A sense amplifier (SA) is the most important part of memory devices and is used to convert small data signals to digital signals during the read cycle [1-3]. SA are divided into synchronous (triggered) and a synchronous. The first ones are based on clocked latch circuitry, the last ones – on using asynchronous circuitry without synchronization.

In this work, we analyze the differential synchronous SA without data regeneration in memory. They differ from asynchronous in lower power consumption, the absence of signal output glitch and better embed ability in synchronous memory blocks. In literature, it is paid in sufficient attention to the influence of the SA initial voltages on its most important parameter – the read data sensitivity. In this paper, the sensitivity of synchronous SA with various initial voltages is analyzed.

2. Basic circuits
Many different schematics of synchronous SA without data regeneration are based on basic triggered cell (figure 1a) and its dual version (figure 1b).

Figure 1. Basic circuits of SA (a, b) and switching (c)

The read data comes to the differential inputs D and ND, according to that data SA starts to switch (Figure 1c). Initially, the potentials of internal nodes 1 and 2 are set the same, and the electrical
conditions of symmetrical sides of trigger cell become the same. During the switching, there is a regenerative process, which results in the voltage rise (transient) with amplitude $U_m$. The amplitude of this transient depends on transistor sizing, loading circuitry and the range of differential input signal. It should be rather low because the loading circuits can be switched and produce undesirable pulses.

The most important parameter of the sense amplifier is the sensitivity $U_S$. The sensitivity is a minimum input voltage (differential signal at the inputs $D$ and $ND$), which makes sense amplifier to direct switch.

The performed analysis showed that the sensitivity of SA is determined not only by the transistor parameter variation in the symmetrical sides of SA trigger but also by the difference of loading capacitances in the nodes 1 and 2. So during the design of memory reading circuitry the maximum symmetry of the SA nodes 1 and 2 and the first stages of load, connected to these nodes, should be provided.

The sensitivity is also affected by the initial voltages in the internal nodes 1 and 2 of the sense amplifier (figure 1).

For the subsequent analysis, we chose a basic cell with n-channel input transistors T1-T2 in figure 1b. Practically this variant is the most prevalent in readout data circuitry, as it is consistent with the standard CMOS memory cells [3].

The effect of the initial voltages dependence is caused by the impact of the p-channel transistors specific transconductance $k_p$ variation, the difference of the initial voltages in nodes 1 and 2, the difference of p-channel transistors threshold voltages and the capacitances in nodes 1 and 2 on the SA sensitivity. The experimental analysis showed that the component of sensitivity, related with the specified parameters variation, is:

$$U_S = U_C \left[ \frac{1}{3} \left( 1 + \bar{U} + \bar{U}^2 \right) \delta k_p + K \left( 1 + \bar{U} \right) (\Delta U_{thp} + \Delta U_0) + \left( 1 - \frac{1}{3} \left( 1 + \bar{U} + \bar{U}^2 \right) \right) \delta C \right],$$

where $U_C$ is the factor of the common-mode voltage level at the SA inputs, $\bar{U}$ is the parameter of the initial voltages in nodes 1 and 2, $K$ is a factor of specific transconductance relation.

As can be seen from (1), the impact of the nodal capacitances variation is minimized when $\bar{U} = 1$. This occurs when the initial voltage is equal to the voltage when the nodes 1 and 2 are shorted in a static mode. However, this case is not used because of the significant currents and output noise.

The impact of the initial voltages differences $\Delta U_0$ in nodes 1 and 2 on the sensitivity can be excepted by the complete potential equalization in these nodes until the sense amplifier activation. It can be provided by using the equalizing transistors TS1-TS2 in combination with transistor TS (figure2).

![Figure 2](image)

**Figure 2.** The equalization of the initial voltages by using the extra transistors TS1-TS2 with TS.

The parameter $\bar{U}$ in (1) depends from the initial voltage $U(0)$ and the supply voltage $U_{dd}$:

$$\bar{U} = \alpha \left[ U_{dd} - U_{thp} - U(0) \right],$$

where $\alpha$ is a factor depending on the supply voltage and the threshold voltage.
where $\alpha$ is the parameter of specific transconductance relation of p- and n-channel transistors and the common-mode voltage at the inputs.

As follows from (2), the parameter $\bar{U}$ becomes maximum when $U(0) = 0$. According to (1), this means that the specific transconductance variation and the p-channel transistors threshold voltages variation with zero initial voltage cause the strongest influence on the sensitivity.

3. Experimental results

The experiment to determine the influence of initial voltages in the SA internal nodes on the sensitivity was provided using two variants of sense amplifier: with maximum (figure 3a) and minimum (figure 3b) initial conditions.

Figure 3. Circuits of SA with maximum (a) and minimum (b) initial voltages

Both variants are based on the basic trigger cell on the transistors T1-T4. In the first one the initial voltages of the nodes 1 and 2 are formed at the level of supply voltage $U_{dd}$ through the transistors TS, TS1, TS2, while in the second one – at the level of the ground bus by using the input transistors T1-T2 and TS. In the first case, SA is activated by applying the positive voltage to the clock input C, and in the second – by the negative voltage at the input NC.

The results of the experimental sensitivity determination in the sample of 326 amplifiers of the first type and the sample of 74 amplifiers of the second type are presented in figure 4.

Figure 4. Normalized sensitivity distribution histogram: a – SA type 1, b – SA type 2

As can be seen from figure 4, both histograms have some sensitivity offset related to 0, not exceeding 1% from the supply voltage $U_{dd}$. This offset results from the topological asymmetry of the trigger cell nodes because it is impossible to provide the absolute symmetry of cross-connected circuit layout.
The standard deviation of the normalized sensitivity related to the average value -0.6% for SA type 1 is 1.08%. For the second type of SA, the standard deviation is 3.4 times worse and reaches the value 3.72% from the average value 0.96%.

Therefore, during the readout circuits design preference should be given to the amplifiers based on the circuit in figure 3a. An important factor influencing the yield ratio is to determine the delay of SA activation relatively to the moment of memory cell choice and data reading, ensuring the correct amplifiers switching for all of the parameters variations. The experimental values of the SA sensitivity allow reasonably choose the input signal level at the moment of the amplifier activation.

4. Conclusion

Thus, the initial voltage in the internal nodes of the synchronous SA significantly impacts on its most important parameter – sensitivity. According to our experimental data, the SA sensitivity may vary in 3-4 times depending on the initial voltages. Therefore, the way to maximize the sensitivity is to choose correctly the initial voltage in its internal nodes during the design of synchronous SA schematics.

References

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