Single-phase AC-AC Z-source converter based on asymmetrical gamma structure with continuous input current and safe commutation strategy

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Abstract
This paper examines a new topology of the AC-AC Z-source converter based on asymmetrical Gamma structure is proposed. The proposed converter has all the common features such as common ground between input and output, realizing the continuous input current and the ability of boost in-phase and buck out-of-phase. In order to generate a high voltage gain in the proposed converter, a coupled inductor with Gamma structure is used. In this structure, as the turn ratio approaches to one, it gives a higher voltage gain. In order to damping the voltage and current overshoots on the proposed converter switches, a safe commutation strategy is used. Due to the specific topology of the proposed converter, the output filter has been eliminated, so the size and cost of the proposed converter are reduced. Circuit analysis and performance principles are presented in detail and a laboratory prototype implemented to confirm the practicality of the proposed converter.

1 | INTRODUCTION

Nowadays, power electronic converters play an important role as an interface element in industries, residents, hospitals and etc. There are variable applications in the field of AC power for power electronic converters such as the dynamic voltage restore [1, 2] and solid-state transformers [3, 4]. Generally, AC power converters can be divided into three major parts: AC–AC indirect converters [5, 6], matrix converters [7, 8] and AC–AC PWM direct converters [9–11]. If the goal is to adjust the voltage amplitude, direct ac-ac converters are superior to the other groups, due to the advantages such as simpler control, single-stage conversions, higher efficiency, smaller sizes, and lower prices. Indirect ac-ac converters (AC-DC-AC) require a bulky dc link and the power conversion is done in two steps. Although the Matrix converters have the ability to regulate the output voltage and frequency, their voltage gain is limited and their control is complicated. By modifying and correcting the structure of the dc-de converters and by replacing the bidirectional switches instead of unidirectional switches, they can be used as direct AC-AC converters [12]. Meanwhile, converters based on impedance network are one of the most important and most popular structures among power electronic converters [13–15]. In this decade, AC-AC Z-source converters have attracted researchers’ interest in both single-phase [16–26] and three-phase [27, 28] field.

Traditional single-phase ac-ac Z-source converter has abilities such as boost in-phase and buck-boost out-of-phase. However, problems such as the lack of common ground between input and output, discontinuous input current and needing a snubber circuit for each switch to suppress the voltage overshoots poses a serious challenge to this converter [16]. In order to solve the problems of the traditional converters, the quasi-Z-source converter (QZSC) is presented in [17]. Modified Z-source converter (MQZSC) presented in [18]. This convertor, maintaining the benefits of a quasi-Z-source converter, has reduced the size by eliminating the output inductor filter. The converters in [19] and [20], solved the voltage and current spikes problems on the switches by using a safe commutation strategy. In a quasi-Z-source converter and modified quasi-Z-source converter, the only option for controlling the output voltage of the converter is the duty cycle. Therefore, in order to generate high voltage
gain, the duty cycle must be set close to the maximum duty cycle. To solve this problem, the impedance source based on the transformer was first introduced in [21] and [22]. In these inverters, in addition to the duty cycle, by using the turn ratio of the transformer, it is possible to control the output voltage of the converter and achieve higher voltage gain in smaller duty cycles. The idea of using transformers in AC-AC Z-source converters was suggested by [21] and [22]. The converter presented in [21] uses a \( \Gamma \) shaped coupled inductor to generate the required voltage gain. But this converter has drawbacks such as: discontinuous input current, need LC input filter and requires large filter inductor at the output to remove high-order harmonics. In modified single-phase Z-source converter based on gamma structure presented in [23] output LC filter is eliminated but the input current is discontinuous. Both converters in [22] and [24] are based on the T-structure, but [24] has improved the voltage gain of the converter by replacing a bidirectional switch instead of the output filter inductor. In converters [22] and [24], as the winding turn ratio increases, the magnetizing current increases linearly, which increases the size of the core.

This paper examines a new topology of impedance source converter based on an asymmetric \( \Gamma \) structure with continuous input current and without output inductor filter is proposed. Voltage and current spike problems on the switches are solved by using the safe commutation strategy. In the following principles, steady-state analyses and converter design are provided.

## 2 PROPOSED AC-AC Z-SOURCE CONVERTER

The proposed asymmetric \( \Gamma - Z - source \) converter is shown in Figure 1. In the proposed converter, the output LC filter is eliminated, so the load is directly connected to the impedance source network. On the other hand, due to the selected topology for this converter, the problem of needing an input LC filter has also been resolved. In the proposed converter, the turn ratio of the coupled inductor is limited to the small range and by decreasing the turn ratio, the voltage gain will be increased. The proposed converter consists of input inductor \( (L_i) \), coupling inductors \( (L_1 \ and \ L_2) \), two capacitors \( (C \ and \ C_o) \), two bidirectional switches \( (S_1 \ and \ S_2) \) and load \( (R) \).

### 2.1 Safe-commutation study

As shown in Figure 1, the proposed converter has two bidirectional switches that turn on and off contrary to each other. Each of these bidirectional switches includes two unidirectional switches that are connected to the back to back common emitter. Delays in turning on and off any of these switches, which are due to their non-ideal feature, cause problems. Figure 2(a) shows the problems caused by the non-ideal characteristic of the switches. In the overlap area, due to the non-ideal characteristic of the switches, \( S_1 \) and \( S_2 \) are on at the same time in a short time interval, which results in a sudden change in the voltage of the circuit capacitors and passing the spike current through the bidirectional switches. In the dead time area, due to the non-ideal characteristic of the switches, \( S_1 \) and \( S_2 \) are switched off at the same time in a short time interval, which results in the disconnection of the circuit inductors current and the occurrence of voltage spike on the bidirectional switches. The overlap area is worse than the dead time area because it increases the flow from the source as well as increasing the losses. So all four switches should not be on at the same time. In practice, to solve this problem, according to Figure 2(b), the dead time is applied between the bidirectional switches control pulses. There are two common ways to prevent inductors current disconnection: the hardware method or in other words, the use of a snubber circuit for each switch, and the software method, that is, the use of a safe commutation strategy. Due to the constant losses in the snubber circuit, the second method is superior to the first method.

In order to apply the safe commutation strategy, assume that the input voltage is positive \( (V_i > 0) \) and the control signal is at the end of the \( D T_s \) time interval (Figure 3(a)). \( D \) and \( T_s \) are the duty cycle of switches and the switching period, respectively. In dead time area, \( S_2 \) is turned off while \( S_1 \) is not turned on yet. In this case, there will be two commutation conditions: Condition I, if \( i_{L} > i_{L_{1,1}} \), as shown in Figure 3(b), \( g_1 \) and the \( g_2 \) body diode construct the path for the inductor current to pass. Condition II, if \( i_{L} < i_{L_{1,1}} \), as shown in Figure 3(c), \( g_4 \) and the \( g_3 \) body...
diode construct the path for the inductor current to pass. At the end of the dead time area, the time interval \((1 - D)T_s\) is started (Figure 3(d)).

As described above, the safe commutation strategy for the proposed converter in different operation modes is shown in Figure 4. In boost in-phase mode, when \((V_i > 0)\), \(g_1\) and \(g_4\) are fully turned on and the \(g_2\) and \(g_3\) are modulated complementary in switching frequency. When \((V_i < 0)\), \(g_1\) and \(g_4\) are fully turned on and the \(g_2\) and \(g_3\) are also modulated complementary. It should be noted that due to the fact that the design of the elements is done for the boost in-phase mode, the probability of going to the discontinuous current mode (DCM) or in other words, the presence of return current is very low and can be ignored it. So, in boost in-phase mode, it is possible to help reduce switching losses by turning off \(g_1\) and \(g_2\) in the negative and positive half-periods, respectively.

Figure 4(a) shows the safe commutation strategy for boost in-phase mode. The safe commutation strategy for buck out-of-phase mode is shown in Figure 4(b). When \((V_i > 0)\), \(g_2\) and \(g_3\) are fully turned on and the \(g_1\) and \(g_4\) are modulated complementary in switching frequency. when \((V_i < 0)\), \(g_1\) and \(g_4\) are fully turned on and the \(g_2\) and \(g_3\) are also modulated complementary.

2.2 | Circuit analysis

For analyses of the proposed Z-source converter, the following assumptions are considered: (i) The copper losses of the input inductor \((L)\) and the magnetizing inductor \((L_m)\) are modelled with \(r_L\) and \(r_{L_m}\), respectively. (ii) All the switches and their reverse diodes are considered ideal and the conducting voltage drop is ignored. (iii) The proposed converter operates in continuous conduction mode (CCM). (iv) The coupled inductor is modelled with an ideal transformer with a magnetizing inductor \((L_m)\) and a leakage inductor \((L_k)\). In the following, the performance of the proposed converter will be explained in different operation modes.

In the coupled inductor, the following relationships are established:

\[
\frac{v_{L_1}}{v_{L_2}} = \frac{i_{L_2}}{i_{L_1}} = \gamma \tag{1}
\]

\[
k = \frac{L_m}{L_m + L_k} \tag{2}
\]

**Mode I**: The equivalent circuit of the proposed converter in the first operation mode, is shown in Figure 5(a). In the first operation mode, the switch \(S_1\) is turned off and the switch \(S_2\) is turned on. By turning on \(S_2\), the capacitor \(C\) is charged. By applying KVL and KCL in the equivalent circuit of this mode,
In the steady state, the following relation can be written:

\[
\begin{align*}
L \frac{di_L}{dt} &= 0 \\
L_m \frac{di_{L_m}}{dt} &= 0 \\
C \frac{dv_C}{dt} &= 0 \\
C_o \frac{dv_{Co}}{dt} &= 0
\end{align*}
\]

By applying the volt-second balance principle for inductors and applying ampere-second balance for capacitors, the following equations are calculated. The windings parasitic resistance effects and the coupling transformer coefficient effects on the proposed converter voltage gain, are investigated in (6) and (7), respectively.

\[
\frac{v_o}{v_i} = \frac{1}{1 - \frac{D}{1 + \frac{r_L}{r_T}}}
\]

In the (7), by decreasing the winding ratio, the voltage gain is decreased.

By disregarding windings parasitic resistance and given \(k = 1\), the voltage gain is derived as:

\[
G = \frac{v_o}{v_i} = \frac{1 - D}{1 - D \left(1 + \frac{r_L}{r_T}\right)}
\]

Also the input current, voltage stress of the capacitor \(C\) and current stress across of the magnetizing inductor, are obtained as the following relations:

\[
\begin{align*}
i_L &= \frac{(1 - D)(y_T - 1)}{y_T - 1} \frac{v_o}{R} \\
v_C &= \frac{y_T}{y_T - 1} \frac{y_T - 1}{D} \frac{v_i}{R} \\
i_{L_m} &= \frac{(1 - D)(y_T - 1)}{y_T - 1} \frac{v_o}{R}
\end{align*}
\]

3 | PARAMETER DESIGN

Circuit design is always considered to the worst condition. Due to this fact, the most changes occur during \([0 - DT]\) interval
and the design is based on this interval. With regard to the voltage-current relationships for inductors and capacitors, the following relations are written:

\[ L = \frac{|V_L| \Delta i}{\Delta I_L} \tag{10} \]

\[ C = \frac{|L_C| \Delta i}{\Delta V_C} \tag{11} \]

Where \( \Delta I_L \) and \( \Delta V_C \) are permitted ripple for inductor current and capacitors voltage, respectively. It should be noted that in the parameter design, the ohmic losses of the inductors are ignored.

### 3.1 Asymmetrical \( \Gamma - Z \) source circuit design

The voltage and current of \( L \) and \( L_m \) have been calculated in (3) and (9), respectively. If permitted ripple for each inductor is considered \( x\% \) of its passing current, by replacing the voltage and current equations of the switches (10), the minimum value of the inductors \( L \) and \( L_m \) can be written as following relations, respectively:

\[ L \geq \sqrt{2(1-D)(\gamma_T - 1)} \frac{D V_i^2}{\gamma_T - 1 - D(2\gamma_T - 1)} x\% f_i P_o \tag{12} \]

\[ L_m \geq \sqrt{2\gamma_T^2 D(1-D)} \frac{V_i^2}{(\gamma_T - 1) - D(2\gamma_T - 1)} \left(1 + (\gamma_T - 1)D\right) x\% f_i P_o \tag{13} \]

The currents of \( C \) and \( C_s \) for the first operation mode in (3) and their voltage have been calculated in (8) and (9), respectively. If permitted ripple for each capacitor is considered \( y\% \) of its voltage, by replacing the voltage and current equations of the capacitors in (10), the minimum value of the capacitors \( C \) and \( C_s \) can be written as following relations, respectively:

\[ C \geq \sqrt{2(\gamma_T - 1) - D(2\gamma_T - 1)} \frac{P_o}{\gamma_T} y\% f_i V_i^2 \tag{14} \]

\[ C_s \geq \sqrt{2\gamma_T D} \frac{(\gamma_T - 1) - D(2\gamma_T - 1)}{(\gamma_T - 1)^2(1-D)} \frac{P_o}{y\% f_i V_i^2} \tag{15} \]

where \( P_o \) is the average output power, \( V_i \) is the RMS of the input voltage and the \( f_i \) is the switching frequency.

### 3.2 Voltage and current stress of the switches

By applying KVL in operation modes and using Equations (8) and (9), the maximum voltage stress of the switches \( S_1 \) and \( S_2 \), are obtained as follows:

\[
\begin{align*}
V_{s1-\text{max}} &= \frac{\sqrt{2} \gamma_T}{\gamma_T - 1 - D(2\gamma_T - 1)} V_i \\
V_{s2-\text{max}} &= \frac{\sqrt{2} \gamma_T}{\gamma_T - 1 - D(2\gamma_T - 1)} V_i
\end{align*}
\tag{16}
\]

By applying KCL in operation modes and using Equation (9), the maximum current stress across of the switches \( S_1 \) and \( S_2 \), are obtained as follows:

\[
\begin{align*}
I_{s1-\text{max}} &= \frac{\sqrt{2} p_o}{(1-D)(\gamma_T - 1) V_i} \\
I_{s2-\text{max}} &= \frac{\sqrt{2} p_o}{(1-D)(\gamma_T - 1) V_i}
\end{align*}
\tag{17}
\]

### 4 PROPOSED CONVERTER FEATURES AND COMPARISON

#### 4.1 Proposed converter features

Table 1 for a better comparison of the proposed converter with other topologies is presented. The voltage and current equations, the number of passive and active elements, the continuous input current feature and common ground feature of the previous converters and the proposed converter are compared in Table 1. In this table, \( P_o \) is the average output power and \( f_i \), \( I_{i1} \), \( I_{i2} \), \( I_{i,m} \) and \( V_i \) are the RMS values of input current, inductor(s) current, magnetizing inductor current and input voltage, respectively. \( I_{s-\text{max}} \) and \( V_{s-\text{max}} \) are the peak values of the current and voltage stresses of switches, respectively. This comparison is shown that the proposed converter meets all expectations, including continuous input current, common ground and high voltage gain ratio with fewer elements. Although both the proposed converter and the converter presented in [21], have used the coupling inductor with the \( \Gamma \) structure to generate high voltage gain, but the proposed converter with the same turn ratio generates more voltage gain. The voltage gain of the proposed converter versus the duty cycle for different turn ratios is shown in Figure 6(a). According to this figure, by reducing the ratio of the transformer with a certain duty cycle, the converters’ voltage gain increases, this feature simplifies the design of the transformer and reduces the cost of the winding. If in Equation (6)
TABLE 1 Comparison between the proposed converter and other single-phase AC-AC Z-source converters

|                | [16] | [17] | [18] | [22] | [21] | [24] | Proposed Converter |
|----------------|------|------|------|------|------|------|--------------------|
| \(\frac{v_o}{R}\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) |
| \(\frac{v_{\text{in}}}{R}\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) |
| \(\frac{v_{\text{con}}}{R}\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) | 1 \(D\) |
| \(\frac{v_{\text{out}}}{R}\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) | 1 \(2D\) |
| \(I_{L1} & I_{L2}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) |
| \(I_{\text{con}}\) | – | – | – | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) |
| \(I_{\text{max}}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) | \(\frac{I}{v}\) |
| \(V_{\text{con}}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) | \(\frac{V}{v}\) |

Continuous Input Current | no | yes | yes | yes | no | yes | yes |
Common Ground | no | yes | yes | yes | yes | yes | yes |
Unidirectional Switches with body diodes | 2 | 4 | 4 | 4 | 4 | 6 | 4 |
Coupled Inductor | – | – | – | 1 | 1 | 1 | 1 |
Inductors | 3 | 3 | 2 | 2 | 1* | 1 | 1 |
Capacitors | 3 | 3 | 2 | 3 | 2* | 3 | 2 |

*The capacitor and inductor of the input filter have been ignored.

Experimental results.

assumes that \(\frac{V}{R} = \frac{v_o}{R} = Z_f (Z_f\) is losses coefficient), the voltage gain of the proposed converter can be simplified as:

\[
\frac{v_o}{v_i} = \frac{1}{G + GZ_f \left\{ 1 + \frac{1 + D \gamma_f - 1}{\gamma_f (1-D)} \right\}^2}.
\]

By using Equation (18), the voltage gain versus duty cycle for a constant turn ratio \(\gamma_f = 2\) and different \(Z_f\) is plotted in Figure 6(b). According to Figure 5(b), when all elements are ideal \((Z_f = 0)\) voltage gain can be increased to infinity. But as the losses coefficient increases, the output voltage decreases.

4.2 Proposed converter in comparison with trans-Z-source converters

For fair comparison, all converters must have shared ground, continuous input current and also the turn ratio of them should be adjusted to have the same maximum duty cycle \((D_{\text{max}})\). For example, if \(D_{\text{max}}\) equals to 0.25, then \(n = 2\) and \(\gamma_f = 1.5\) is calculated. Using information presented in Table 1, voltage gain to total component count (TCC) ratio versus duty cycle is depicted in Figure 7(a). This figure shows that the proposed converter as compared to other converters generates a high voltage gain with less number of component counts. In Figure 7(b), the output voltage of the proposed converter and the Z-source converters based on coupled inductor with continuous input current presented in [23] and [24] are compared together. Figure 7(b) shows the voltage gain versus duty cycle for a
constant losses coefficient ($L_L = 0.004$). As can be seen in this figure, the proposed converter under the same conditions has a lower voltage drop and generates more voltage in the output of the converter. The main reason for this difference is that the losses due to the magnetizing current in the converters [22] and [24] are at least $(n + 1)^2$ times greater than the proposed converter.

The energy stored in the inductor and capacitor is calculated from the following equations:

\[ W_L = \frac{1}{2} L I_{\text{max}}^2 \quad (19) \]

\[ W_C = \frac{1}{2} C V_{\text{max}}^2. \quad (20) \]

The amount of energy stored in each of these elements indicates their size and volume. By replacing the voltage of the capacitors and the current of the inductors from Table 1 and the minimum value obtained from the parameter design section in (19) and (20), the total energy stored in the inductors and capacitors of the proposed converter, [22] and [24] is calculated. The results of the calculations are given in Table 2.

In Figure 8, a comparison between the proposed converter and the converters presented in [22] and [24] is done. In this comparison, the equations given in Table 2 are in per-unit base on $\frac{P_i}{\sqrt{2} V_{\text{rms}} f_s}$. The total energy stored in the inductors and the capacitors versus the duty cycle is shown in Figure 8(a) and 8(b), respectively. From Figure 8(a) and 8(b), it is obvious that in the same conditions, the proposed converter requires smaller inductors and capacitors. For example, in $D = 0.2$, the energy stored in the capacitors and inductors of the converters [22] and [24] is about twice or more than twice the proposed converter.

A laboratory prototype is presented to prove the validity of the proposed converter as shown in Figure 9. The experimental results consist of boost in-phase mode and buck out-of-phase mode. In both of operating modes the input peak voltage is considered. Based on theoretical relationships, in order to generate $154V_{\text{peak}}$ in the boost in-phase mode and $501V_{\text{peak}}$ in the buck out-of-phase mode at the output side, the duty cycle is set to 0.15 and 0.6, respectively. The switching frequency of the proposed converter is equal to $32KHz$. According to Equations (12) to (15), the minimum value of capacitors and inductors of the proposed converter has been calculated for in Table 3.

Table 4 provides a list of parameters that were used in the laboratory prototype. The polarity of the input voltage was detected by LM393. Depend on input voltage polarity, an Arduino microcontroller (Pro micro) generated four PWM control signals with small dead time that controlled the converter switches.

### Table 2: Total energy stored in the inductors and capacitors of the proposed converter and converters presented in [22] and [24]

|          | $W_L$ | $W_C$ |
|----------|-------|-------|
| [22]     | $P_i f_s (x+2) (1-2D)$ | $P_i f_s (x+2D)$ |
| [24]     | $P_i f_s (N+4) (1-D)$ | $P_i f_s (N+4D)$ |
| Proposed | $P_i f_s (x-1) (2y_D+1)$ | $P_i f_s (y_D D) (1-D) (2y_D+1)$ |

### Table 3: Minimum value of passive components

|          | $L$ | $L_m$ | $C$ | $C_o$ |
|----------|-----|-------|-----|-------|
| Current  | 20% | 50%   | 10% | 10%   |
| Voltage  |     |       |     |       |
| Ripple   | 480$\mu$H | 510$\mu$H | 3.5$\mu$F | 2.5$\mu$F |

### Table 4: Parameters used in the experiments

| $V_{\text{peak}}$ | $D$  | $f_s$ | $f_r$ | $\text{Load}$ |
|-------------------|------|-------|-------|---------------|
| 100$V_{\text{peak}}$ | 0.15-0.6 | 32KHz | 2     | 50$\Omega$    |
| $L$                | $L_m$ | $L_k$ | $C$   | $C_o$         |
| 880$\mu$H           | 480$\mu$H | 2$\mu$H | 9$\mu$F | 4.5$\mu$F |
4.3 | Boost in-phase

The experimental results of the proposed converter for boost in-phase mode in $D = 0.15$, are shown in Figure 10. As can be seen in Figure 10(a), the input and output voltages are completely in-phase with each other. The input voltage is set to $100V_{\text{peak}}$ and the output voltage is about $144V_{\text{peak}}$. Based on (8), the output voltage is calculated as $154V_{\text{peak}}$. The reason for this difference is that the inductor windings losses have been ignored in this equation. Now, if in the Equation (18), $Z_l = 0.02$, the output voltage is equal to $144V_{\text{peak}}$. Given that the load resistance is $50\Omega$, the values of $r_L$ and $r_{L_{\text{max}}}$ are estimated at $1\Omega$. The input current is shown in Figure 10(b). As shown in this figure, the peak of the input current is $4.6A$. The maximum voltage of these switches are $240V$ and $160V$, respectively. Based on (16), the maximum voltage stress on $S_1$ and $S_2$ are calculated as $360V$ and $180V$, respectively. Figure 10(c) to 10(f) show the current stress flowing through the switches. Based on (17), the maximum current stress flowing through the switches $S_1$ and $S_2$ are calculated as $5.7A$ and $11.4A$, respectively. Figure 10(c) to 10(f), prove that the safe commutation strategy prevents voltage and current spike on switches without any snubber circuit. Figure 10(g) shows the voltage across the capacitor $C$. In the experiment, the $V_C$ peak is about $43V$ and based on (9) equal to $54V$.

4.4 | Buck out-of-phase

The experimental results for the buck out-of-phase mode in $D = 0.6$, are shown in Figure 11. Like boost in-phase operation mode, the input voltage is set to $100V_{\text{peak}}$. As shown in Figure 11(a), the output voltage bucked and exactly has $180^\circ$ shift phase with the input voltage. Input current is shown in Figure 11(b). The voltage and current of the bi-directional switches $S_1$ and $S_2$ are shown in Figure 11(c) and 11(d). These figures show that using the safe commutation strategy has prevented voltage spikes on switches. The voltage across the capacitor $C$ is shown in Figure 11(e). Interesting $V_C$ in buck out-of-phase mode boosted in phase with the input voltage. So by little change, the load can be connected to the capacitor $C$ and fed by it. Figure 11(f) shows a sudden change in the duty cycle. In this change, the converter operation has changed from buck out-of-phase mode ($D = 0.6$) to boost in-phase mode ($D = 0.15$) without any problems.

4.5 | Efficiency

In Figure 12, the efficiency of the proposed converter under the same condition has been compared with other transformer
based AC-AC Z-source converter. As can be seen in this figure, the efficiency of the proposed converter is about 90%. According to Section 4.2, the higher efficiency of the proposed converter was predictable than converters presented in [22] and [24]. Due to the elimination of copper losses related to the output filter inductor and the reduction of the input current ripple by placing an inductor at the input of the proposed converter, the proposed converter has a higher efficiency than the converter [21].

5 CONCLUSION

This paper examines an AC-AC Z-source converter based on asymmetric gamma structure has been proposed. The main features of a single-phase AC-AC converter are included in the proposed converter. These features include: Boost in-phase, buck out-of-phase, shared ground, continuous input current and safe commutation strategy. But proposed converter has two advantages. i) to produce high voltage gain in proposed converter, a coupled inductor with asymmetric gamma structure is used. Under the same conditions, this topology produces more voltage gain than the conventional gamma structure. For example, for \( \gamma = 1.5 \) and \( D = 0.2 \) the voltage gain of the proposed converter and the converters presented in [21] is equal to 4 and 2, respectively. ii) in the proposed converter output LC filter is removed and the load is directly connected to the impedance network. According to the experimental results, removing the output filter not only had a negative effect on the converter performance but also reduced its size and cost. As shown in Figure 7(a) and 7(b), it was illustrated that the proposed converter with a lower number of elements produces higher voltage gain than other converters. According to the above mentioned features, the proposed converter can be declared as a suitable option for voltage sag and swell compensation.

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