A novel 3D detector configuration enabling high quantum efficiency, low crosstalk, and low output capacitance

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Abstract: The benefits of pixelated planar direct conversion semiconductor radiation detectors comprising a thick fully depleted substrate are that they offer low crosstalk, small output capacitance, and that the planar configuration simplifies manufacturing. In order to provide high quantum efficiency for high energy X-rays and Gamma-rays such a radiation detector should be as thick as possible. The maximum thickness and thus the maximum quantum efficiency has been limited by the substrate doping concentration: the lower the substrate doping the thicker the detector can be before reaching the semiconductor material’s electric breakdown field. Thick direct conversion semiconductor detectors comprising vertical three-dimensional electrodes protruding through the substrate have been previously proposed by Sherwood Parker in order to promote rapid detection of radiation. An additional advantage of these detectors is that their thickness is not limited by the substrate doping, i.e., the size of the maximum electric field value in the detector does not depend on detector thickness. However, the thicker the substrate of such three dimensional detectors is the larger the output capacitance is and thus the larger the output noise is. In the novel direct conversion pixelated radiation detector utilizing a novel three dimensional semiconductor architecture, which is proposed in this work, the detector thickness is not limited by the substrate doping and the output capacitance is small and does not depend on the detector thickness. In addition, by incorporating an additional node to the novel three-dimensional semiconductor architecture it can be utilized as a high voltage transistor that can deliver current across high voltages. Furthermore, it is possible to connect a voltage difference of any size to the proposed novel three dimensional semiconductor architecture provided that it is thick enough — this is a novel feature that has not been previously possible for semiconductor components. Yet another feature of the novel three dimensional semiconductor architecture is that despite the thick substrate it can also be efficiently cooled.
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1 Introduction

The maximum thickness of the depleted bulk in planar semiconductor radiation detectors is determined by the electric break down field and by the substrate doping concentration. This means that the planar semiconductor detectors have an upper detection efficiency limit for deeply penetrating radiation unless multiple fully depleted planar detectors are placed on top of each other. Another option to improve the detection efficiency of planar detectors would be to utilize multiple detectors and to point the detector edges towards the radiation source, which is, however, not a truly optimal arrangement unless the radiation is unidirectional. Furthermore, a problem in thick planar detectors is horizontal spreading of the signal charge, which increases the crosstalk and hampers spatial resolution unless the detector is operated in photon counting mode [1] and charge sharing is taken into [2, 3] account.

In a planar semiconductor radiation detector the maximum absolute value of the electric field, which should be always substantially smaller than the absolute value of the electric break down field, is present at a pn junction located in the vicinity of either surface. The depletion of the bulk semiconductor material is provided by the vertical electric field component, which absolute value decays along the vertical direction pointing towards the inside of the bulk. If the semiconductor bulk is homogeneously doped then the absolute value of the vertical electric field component drops linearly in the vertical direction towards the interior of the bulk. In thick pixelated planar detectors there is essentially no horizontal field component except in the proximity of the surface. This means that the radiation induced charge cloud is not confined in the horizontal direction and thus it expands due to electric repulsion and random scattering events so that the charge may be shared amongst several pixels.

In Silicon Drift Detectors (SDDs) [4–6], which are planar detectors, there is a horizontal electric field component present inside the bulk which is not responsible for depleting the detector but instead it acts as a drift field transporting signal charges towards a charge-collecting anode. In the SDD the vertical electric field is responsible for the depletion of the detector and detector thickness is similarly limited by the electric breakdown field and the substrate doping concentration. In pixelated SDDs the horizontal drift field can be used for providing charge confinement in horizontal direction but the pixel aspect ratio (i.e. depth to pixel pitch ratio) cannot be very high since in high aspect ratio pixels the absolute value of the horizontal electric field component decays strongly towards the interior of the bulk.
In thick pixelated SDDs comprising high aspect ratio pixels the problem of the decaying horizontal electric field component could be somewhat relaxed if one could provide on both sides of the detector corresponding concentric SDD ring structures — this type of a detector is later on referred to as double-sided SDD. The difference in the SDD ring structure on the radiation entry side would be only that the charge collecting contact were replaced by an opposite type of doping. If the double-sided SDD pixel had n- bulk and p+ rings then the potential of the p+ rings on the radiation entry side would be shifted by a constant negative value when compared to corresponding rings on the opposite side in order to provide the necessary vertical drift field. Even in the double-sided SDD the pixel aspect ratio would need to be relatively small in order to withstand the effect of the decaying horizontal field since in high aspect ratio double-sided SDD pixels the lack of charge confining horizontal electric field in the central part of the pixel would anyhow cause horizontal charge spreading.

The aforesaid problems of planar detectors can be avoided with three dimensional (3D) semiconductor detectors [7, 8], and [9] comprising 3D electrodes penetrating vertically through a semiconductor substrate. In [9] a 3D Charge Coupled Device (CCD) is presented comprising 3D electrodes that are insulated from the substrate by an insulator layer. In [7] and [8] a 3D detector is presented comprising highly doped n+ and p+ type 3D electrodes. In the 3D detectors — excluding regions in the proximity of the detector surfaces — the electric field inside the semiconductor bulk has a vertically invariant horizontal component but no vertical component. The horizontal electric field depletes the substrate and the depletion voltage of the substrate depends on the substrate doping concentration as well as on the horizontal distance between the 3D electrodes but it is independent of the substrate thickness. Furthermore, photon absorption induced charge sharing between multiple pixels takes only place if the photon is initially absorbed at the pixel boundary, i.e., the charge sharing is independent of the 3D detector thickness. The reason for this is that the horizontal electric field effectively transports the signal charges towards a single electrode providing thus charge confinement and preventing horizontal charge spreading.

From this point onwards [7] and [8] are referred to as conventional 3D detectors, which have the advantage that the maximum drift path length of the signal charges depends only on the horizontal distance between the n+ and p+ electrodes, i.e., the drift length is independent of the thickness of the conventional 3D detector meaning that charge trapping is independent of the detector thickness. Since the distance between the 3D electrodes can be made much smaller than the thickness of the semiconductor substrate the conventional 3D detector enables high aspect ratio pixels that can be depleted with a small voltage and wherein charge sharing and trapping are minimized. Consequently, the conventional 3D detectors enable low crosstalk and good spatial resolution. The low depletion voltage is a substantial advantage when silicon based detectors are utilized in intense radiation environments like in particle accelerators. The reason is that the radiation generates acceptor states in silicon substrate which eventually impedes the full depletion of a thick planar detector whereas full depletion in a 3D detector can be maintained at substantially higher radiation dose levels due to the lower overall depletion voltage.

The problem associated with the conventional 3D detector concept is, however, that in a thick detector the capacitance of the signal charge collecting 3D electrodes is relatively high due to the large surface area of the 3D electrodes and due to the small distance between the 3D electrodes. This means that the thicker the conventional 3D detector is the larger is the capacitance and the poorer is the energy resolution of the detector. In [10] and [11] 3D detectors have been tested in X-ray
detection and imaging confirming low charge sharing properties but also highlighting problems with non uniform spatial response and geometrical inefficiencies. The problem of the 3D CCD is that the signal charge needs to be transported through the substrate multiple times from one 3D electrode to another. This means that in 3D CCD significant signal charge trapping tendency is resulted in by interface defects located at the semiconductor and insulator interface of the 3D electrodes.

In this paper a novel Pixelated Vertical Drift Detector (PVDD) concept [12] is proposed enabling high pixel aspect ratio, high detection efficiency, low crosstalk, and low noise (due to low output capacitance). This combination is enabled by providing inside the detector (excluding regions close to detector surfaces) both a constant vertical electric drift field and a vertically invariant horizontal electric field component. The constant vertical electric field component transports radiation-induced charges towards output contacts located on one surface of the detector. The small surface area of the charge collecting contacts enables low output capacitance that is not dependent on the detector thickness. The benefit of the small output capacitance is that it enables good energy resolution. The vertically invariant horizontal field inside the detector provides efficient confinement of radiation-induced charges even in thick detectors insuring thus low crosstalk and good spatial resolution. The fact that the vertical electric field component is constant means that the detector thickness is not limited by the electric field enabling thus high detection efficiency.

The PVDD is based on the idea of providing resistive paths that reach from one surface throughout the semiconductor detector to the opposite surface. On the front side there are two types of dopings forming contacts — the first type dopings collect the radiation-induced charges and the second type dopings form contacts to the one end of the resistive paths. On the backside there are second type dopings forming contacts to the other end of the resistive paths. By implementing a relatively small reverse bias between the first and second type contacts on the front side a vertically invariant horizontal electric field component is generated around the resistive path that depletes the bulk of the PVDD. The application of a potential difference between the second type contacts that are connected to the opposite ends of the resistive paths and located at the opposite surfaces of the detector results in a current flow inside the resistive paths. In case the resistivity along the resistive path is approximately constant the current flow through the resistive path results in according to the Ohm’s law a constant potential gradient inside the resistive path. This constant potential gradient in the resistive paths (assuming that the resistive paths are oriented vertically) results in also a constant vertical drift field inside the depleted semiconductor bulk transporting radiation-induced charges towards the charge collecting contact located on the front side.

It is important to note that the thicker the PVDD, the larger is the voltage that must be applied in order to ensure an adequate vertical electric field. On the other hand, by providing a thick enough PVDD it is possible to connect a voltage in between the first and second surface that greatly exceeds a voltage that can be connected to a conventional planar device having similar substrate doping, which is a novel feature in high voltage semiconductor applications.

2 Pixelated Vertical Drift Detector

Figures 1a, 1b, and 1d illustrate the front side, the backside, and a central cross-section of the simulated device where the dashed lines correspond to the cross-section presented in figure 1c. The horizontal dashed line in figure 1c corresponds to the cross-section presented in figure 1d.
The simulated PVDD arrangement comprises an n-type high-resistivity silicon substrate wherein holes having p type doped walls and reaching throughout the substrate are situated at the pixel borders. On the backside there is a continuous p type layer to which a p+ type contact P1 is deployed. On the front side a p+ type contact P2 is deployed to a p type layer having a gap in the centre of the pixel wherein there is an n+ type contact N2 connecting to the n-type substrate. On the backside there is an optional n+ type contact N1 that is located inside the backside p layer. Between the p+ type contacts P1 and P2 there is a p type resistive path comprising the front and backside p layers as well as the p type hole-walls. The chip edges have preferably a similar p type doping than the hole-walls and establish a similar resistive path than the hole-walls. The backside is preferably the radiation entry side.

In order to establish the resistive path corresponding to the hole-walls it is important to have on the horizontal pixel cross-section more p type dopant atoms on the hole-walls than n type dopant atoms in the substrate. If this condition is met then the p type hole-walls are not fully depleted even
if the n type substrate is fully depleted corresponding to the case that a sufficiently large reverse bias is applied between the n+ type contacts N2 with respect to the other p+ type contacts. In other words, even if the substrate is fully depleted part of the p type hole-walls will remain non-depleted meaning that a resistive path composed of holes (i.e. free charge carriers of positive type) is present along the hole-walls. When the substrate is fully depleted the amount of charge carrier holes on a horizontal cross-section of the pixel can be easily determined by subtracting the amount of n type dopant atoms from the p type dopant atoms on a horizontal cross-section of the pixel.

The PVDD is operated in the following manner. First a sufficiently large reverse bias (e.g. 15 V) is applied between the contacts P2 and N2 in order to fully deplete the n- type substrate resulting in a horizontal electric field component inside the semiconductor substrate pointing towards the central symmetry axis of the pixel. Next a negative bias (e.g. ~30 V) is applied to the contacts P1 and N1 with respect to contact P2. The potential difference between the contacts P1 and P2 results in a hole-current flow along the p type hole-walls. If the resistivity of the hole-walls is approximately constant then the potential drops constantly along the hole-walls generating a constant vertical electric field component throughout the PVDD. It should be noted that since charge collecting electrodes will be connected to the input of a charge preamplifier in a read-out chip, which potential is typically at ∼ 0 V, all voltages reported here should be shifted by 15 V towards negative values.

When radiation is absorbed inside the substrate the horizontal electric field component draws the radiation-induced holes into the p type hole-walls and pushes the radiation-induced electrons towards the symmetry axis of the pixel. The constant vertical electric field component transports the radiation induced holes inside the p type hole-walls towards the p type contact P1 (located on the backside) as well as radiation-induced electrons located at the symmetry axis of the pixel towards the N2 contact (located on the front side). The amount of electrons collected by the N2 contact is proportional to the amount of radiation absorbed in the pixel volume.

By applying a forward bias between the contacts N1 and P1 a vertical trap-filling electron flow from the contact N1 towards the contact N2 is established at the location of the symmetry axis of the pixel. This mechanism should benefit 3d detectors that are based on other semiconductor materials than silicon. According to [17] it has been observed for diamond detectors that device irradiation at room temperature with penetrating radiation such as X-rays or minimum ionising particles induces an increase of the detector signal resulting in from deep-trap filling in the whole volume of the

Figure 2. Figures (a), (b) and (c) illustrate central horizontal cross-sections of alternative hole arrangements.
detector and being sensitive to the initial state of the device prior to operation. Therefore based on [17] trap filling can actually benefit detector operation depending naturally on temperature, how deep the trap levels are, and how often the traps are filled. The way in which the traps are filled is irrelevant, i.e., the trap filling could equally well be performed via current injection.

The proposed novel 3d structure could also be applied as a high voltage transistor if the device is thick enough since a large voltage difference could be utilised between the nodes N1 and N2 while the current running between the Nodes N1 and N2 could be adjusted by applying a suitable forward bias between the nodes N1 and P1. In this manner current could be transported when necessary across a large voltage difference. Particularly when the proposed novel 3d structure is utilised in a high voltage transistor application incorporating a thick substrate and large current flows efficient cooling may be important. Examples of cooling are presented in [18] and [19]. One possibility to establish cooling could be to provide a vertical flow of coolant gas like e.g. helium inside the holes. In photon detection applications it is important to note that like in conventional 3D detectors charge sharing takes place only initially when a photon is absorbed provided that the photon is absorbed at the pixel border [10].

The PVDD offers several advantages that are listed below.

1) The maximum absolute magnitude of the electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the electric field.

2) The capacitance of the output node N2 is small and does not depend on detector thickness enabling thus low noise. Besides, in an integrating detector configuration the small capacitance enables high charge to signal conversion gain facilitating also low noise operation.

3) The facts that the holes can be tilted along a direction pointing towards the radiation source and that the radiation induced electrons are confined to the centre part of the pixel mean that crosstalk can be substantially reduced. It should be noted, however, that the realisation of the tilted holes is not trivial and that it may be out of the reach for current standard manufacturing tools.

4) The fact that transport of radiation-induced charges is confined to a narrow path along the pixel symmetry axis means also that pixel specific trapping tendency is more predictable.

5) The fact that an electron flow can be generated in the centre of the pixel running from N1 to N2 means that before PVDD is exposed to radiation electron traps located along the electron drift path can be filled with electrons corresponding to the electron flow. Depending on the temperature and whether the radiation source is operated in pulse mode trap filling could be performed in between the radiation pulses reducing thus trapping of radiation-induced electrons.

The first three points facilitate expanding the useful operation regime of direct conversion detectors to higher energy X-ray applications — e.g. a silicon based direct conversion detector reaching 90% conversion efficiency for 30 keV photons must be at least 9 mm thick. While thick detectors have been reported previously [20], it should be noted that the maximum thickness of wafers that present silicon processing tools in foundries can handle is typically around 1 mm. The
fourth and fifth point could facilitate the use of other semiconductor materials than silicon or germanium in direct conversion semiconductor radiation detector applications.

It should be noted that the resistance of the resistive path along the hole-wall can be described by the ohmic relation \( U = I \times R = I \times \rho \times \frac{L}{A} \), where \( U \) is the potential difference between the opposite ends of the hole, \( I \) is the current running along the hole-walls, \( \rho \) is the resistivity of the p type hole-wall material, \( L \) is the vertical length of the hole, and \( A \) is the horizontal cross-section area of the p type hole-wall material. If the horizontal topology of the holes differs from one hole to another and/or if the resistivity \( \rho \) is different than planned, the magnitude of the vertical electric field component remains essentially the same. In case there were holes with different horizontal topologies the only difference would be that the currents running through the resistive paths formed by the hole-walls would differ in different topologies. In case the resistivity of the material forming the hole-walls were different than planned the only difference would be that the currents running through the resistive paths formed by the hole-walls would be changed throughout the detector by the same factor. The requirements to create the essentially constant vertical electric field component are that the quantity \( \frac{\rho}{A} \) is approximately constant along the vertical direction. This reasoning applies also to the detector edge, which can be considered simply as a large hole-wall.

As already previously said the direction of the holes can be aligned along the radiation source, i.e., the centre axis of the holes can be aligned along the ‘local direction’ of the radiation as depicted in figures 3 and 4. In case the radiation is not unidirectional but originates from a point source the arrangements of figures 3 and 4 enable considerable reduction in crosstalk if the alignment direction of all of the holes (and the edge in figure 3) converges towards the point source. In the arrangement of figure 3 all the pixels are functional and the detector edge acts as a resistive path similar to the hole-walls.

![Figure 3. A PVDD design minimising the crosstalk when the observed radiation originates from a point source. The centre axis of the holes point towards the point source.](image)

If the ratio of the detector size to the detector distance from the point source were relatively large then the detector edges on the front side would be relatively sharp — a case that is depicted in figure 3. The problem with the sharp edges is that it may hamper the manufacturability. In order to mitigate this effect the detector edge configuration of figure 4 could be used instead. In this configuration the outermost pixels at the detector edges are, however, not functional. The reason is that they collect radiation-induced charge also from the pixel-like structures that are truncated at the detector edges.

One should note that in the pixels of the detectors corresponding to figures 3 and 4 the previously used terms like horizontal and vertical direction are not anymore adequate. The direction of the drift path in the centre of the pixel pointing towards the point-source corresponds to a ‘local vertical’
direction and directions on the plane orthogonal to the ‘local vertical’ direction correspond to ‘local horizontal’ directions. With the aid of these definitions it can be easily described that the radiation-induced charge is drifting along the ‘local vertical’ direction and that a potential barrier for the radiation-induced charge is formed along a ‘local horizontal’ direction.

An observation that can be made from figures 3 and 4 is that the area of the pixel cross-section along the ‘local horizontal’ plane increases towards the front surface of the pixel. If the doping concentration in the substrate and in the hole-walls is constant and if the hole radius is constant then the amount of non-depleted p type dopant atoms (i.e. the amount of holes) inside the p type hole-walls reduces towards the front side of the detector. The reason for this is that the larger the ‘local horizontal’ cross-section of the pixel is the more p type dopant atoms are required to deplete the n type dopant atoms inside the substrate and thus the less there are holes inside the p type hole-walls. For this reason in the detector configurations of figures 3 and 4 the electric field component along the ‘local vertical’ direction is not strictly constant. Instead the electric field component is at maximum on the front side of the detector and the value inside the detector scales down by a factor of ‘local horizontal’ pixel area inside the detector divided by the ‘local horizontal’ pixel area at the front surface. Also the potential barrier on the ‘local horizontal’ plane from the drift path towards the pixel edge is the bigger the closer one is to the front surface.

3 3D TCAD simulation study

In this simulation study a PVDD pixel according to figure 1 is investigated. The performance of the pixel has been studied by simulating a quarter of the whole pixel using TCAD tools. It was possible to simulate only the quarter of the pixel due to its symmetry and by doing so the required simulation time was considerably reduced.

When the substrate is fully depleted the pixel’s net hole concentration \( N_h \) per distance inside the hole-walls is given with the following equation

\[
N_h = 3\pi \left( r_i^2 - r_o^2 \right) \times C_p - \left( D^2 - 3\pi r_o^2 \right) \times C_n, \tag{3.1}
\]

wherein the pixel size \( D \) is 100 \( \mu \)m. Along the pixel boundary there are 8 partial empty holes corresponding to 3 entire holes, each of the holes having a radius \( r_i \) corresponding to 5 \( \mu \)m. Next to the hole-wall there is a 1 \( \mu \)m thick p type layer which outer radius \( r_o \) corresponds to 6 \( \mu \)m and which p type dopant (boron) concentration \( C_p \) corresponds to 2.2e15 cm\(^{-3}\). The n type substrate
dopant (phosphorus) concentration $C_n$ corresponds to $5 \times 10^{12} \text{cm}^{-3}$. Based on (1) pixel’s net amount of holes inside the hole-walls per hole length is around $1.8 \times 10^9 \text{cm}^{-1}$ when the substrate is fully depleted, i.e., in each vertical hole forming the resistive path there are around 60000 holes per one micrometre thick hole-wall slab. The amount of hole current $I_h$ running in one hole wall in room temperature can be calculated with the following equation

$$I_h = \mu_h \frac{U N_h e}{T}$$

where $\mu_h$ is the hole mobility at room temperature and at $2.2 \times 10^{15} \text{cm}^{-3}$ boron concentration corresponding to $450 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. The vertical electric field value inside the hole wall is given by the division $U/T$ wherein $U$ corresponds to $30 \text{V}$ potential difference between the opposite ends of the hole wall and $T$ corresponds to the detector thickness $300 \mu\text{m}$. The symbol $e$ refers to the elemental charge corresponding to $1.6 \times 10^{-19} \text{C}$. $N_h$ corresponds to equation (3.1) and the division by 3 takes into account that the current $I_h$ corresponds to only one hole wall. Based on equation (3.2) the holes in the hole walls result in a current corresponding approximately to $43 \mu\text{A}$ running in one hole-wall. In case of a thicker device, like for example in a $600 \mu\text{m}$ thick device, the current running through the hole-wall will be the same if the electric field and the hole diameter remains the same (hole aspect ratio would increase from 30:1 to 60:1).

One of the main objectives of this paper was to test whether a constant vertical electric field component could be established inside the simulated PVDD pixel. In order to test this a reverse bias of $15 \text{V}$ was first applied between the contacts P2 and N2. Based on the simulation this was enough to fully deplete the $300 \mu\text{m}$ thick n-type substrate resulting in a horizontal electric field component inside the semiconductor substrate pointing towards the central axis of the pixel. Next a negative bias of $-30 \text{V}$ was applied to the contacts P1 and N1 with respect to contact P2 (being at 0 V). According to the simulation the potential difference between the contacts P1 and P2 resulted in a hole-current flow along the p type hole-walls resulting in a constant potential drop along the hole-walls generating a constant vertical electric field component throughout the PVDD. This was naturally expected since the doping concentration and thereby the resistivity of the p type hole-wall material is constant. The constant vertical electrostatic potential gradient inside a $300 \mu\text{m}$ thick device can be seen on figures 5a and b. The constant vertical electrostatic potential gradient is even more pronounced in figure 6 corresponding to a $600 \mu\text{m}$ thick device wherein the backside contacts P1 and N1 are connected to $-60 \text{V}$, P2 is biased at 0 V, and N2 is biased at $15 \text{V}$. Figure 5b represents the potential gradient on the symmetry axis (L1) and at the edge of the pixel (L2) of the $300 \mu\text{m}$ thick pixel when $-30 \text{V}$ is applied to contacts P1 and N1, P2 is at 0 V, and N2 is at $15 \text{V}$. It can be seen from the figure that a constant potential gradient, i.e., a constant vertical electric field component is created in the mid portion of the pixel (from $100 \mu\text{m}$ to $200 \mu\text{m}$).

Another objective of the paper was to test whether a sufficiently large barrier could be created from the drift path towards the pixel edge in order to insure that no crosstalk is resulted in of signal charge blooming from one pixel to another. In figure 5b one can see two potential graphs which difference corresponds to the horizontal potential barrier, which is constant inside the mid portion of the substrate. The horizontal locations L1 and L2 wherein the potential graphs are taken can be seen in figure 7b. Figure 5b represents electrostatic potential distribution for the case when $-30 \text{V}$ is applied to contacts P1 and N1, P2 is at 0 V, and N2 is at $15 \text{V}$. The barrier from the middle to
the edge of the pixel being constant in the mid portion of the pixel and equalling to around 3 V is more than enough to eliminate the blooming crosstalk. Corresponding simulation results are presented for a 600 \( \mu \)m thick PVDD on figures 6b and 8b. From the figure 6b it can be seen that the barrier equals to around 3 V as well meaning that the thickness of the pixel does not affect the barrier height. Similarly one can deduce that a constant vertical drift field is established inside the substrate when the distance from the surface is around 100 \( \mu \)m or more.

The third objective of this paper was to test whether an electron flow can be established in the centre of the pixel running from the contact N1 to the contact N2 by applying a forward bias between the contacts N1 and P1. In the simulation result presented in figure 9 the contact N1 is biased at −30.5 V, P1 is biased at −30 V, P2 is biased at 0 V, and N2 is biased at 15 V, i.e. a forward bias of 0.5 V is applied between P1 and N1. The forward bias results in a flow of electrons running in the middle of the pixel — the white lines represent the border of a non-depleted area formed around the symmetry axis of the pixel. Figure 10a illustrates a horizontal cross-section of the PVDD quarter-pixel presented in figure 9. Figure 10b illustrates horizontal electrostatic potential barriers from the middle to the edge of the pixel when the forward bias between P1 and N1 is 0.1 V, 0.2 V, 0.3 V, 0.4 V, and 0.5 V. From 9b it can be easily deduced that in the simulated detector configuration the electron current running inside the pixel starts to alter the horizontal potential barrier between the middle and the edge of the pixel only when the forward bias between P1 and N1 is 0.5 V or higher. Even at 0.5 V forward bias the horizontal potential barrier from the middle to the edge of the pixel is reduced only slightly to 2.8 V.

Figure 11 corresponds to a transient simulation wherein the 300 \( \mu \)m thick PVDD quarter-pixel is illuminated with a 100 ns monochromatic 850 nm light pulse having an intensity of 1500 W/cm\(^2\). The curve in figure 11 represents the electron current at the n+ contact (N2) as a function of time. As can be seen from figure 11 the output current increases considerably during the light pulse. Furthermore, according to the curve in figure 11 the photo induced excess output current dies off at around 23 nano-seconds after the termination of the light pulse.

The capacitance of the signal charge collecting contact N2 in the operational 300 \( \mu \)m thick device was simulated to be around 49 fF, which is exactly the same as in the 600 \( \mu \)m thick device meaning that in a thick enough PVDD the capacitance of the contact N2 is not affected by the device thickness.

4 Conclusions

The purpose of this work was to utilize 3D simulations in order to validate the operational principle and the benefits of the PVDD concept. It is fair enough to say that this goal was successfully achieved.

As already stated the PVDD concept offers several advantages. The maximum electric field is not dependent on the detector thickness and thus the detector thickness is not limited by the breakdown electric field. The capacitance of the output node is small and does not depend on detector thickness. The crosstalk is mitigated since the radiation induced electrons are confined to the centre part of the pixel, thus preventing signal charges from spreading into neighbouring pixels. In case a point like radiation source is utilised the crosstalk can be further mitigated if one utilises tilted holes wherein the central axis of the holes is pointed towards the point like radiation
Figure 5. Simulation results for 300 $\mu$m thick PVDD: (a) Electrostatic potential distribution inside the PVDD quarter-pixel. Vertical cutlines L1 and L2 are illustrated. (b) Electrostatic potential on the vertical cutlines L1 and L2 corresponding to the case when P1 and N1 are biased at $-30$ V, N2 is biased at 15 V, and P2 is biased at 0 V. The figure 5b demonstrates that a potential barrier exists between the middle and the edge of the pixel essentially along the whole thickness of the pixel. When the distance from the surface is 100 $\mu$m or more the figure demonstrates that the barrier height is constant at around 3 V and that a constant vertical drift field is established inside the substrate.

Figure 6. Simulation results for a 600 $\mu$m thick PVDD: (a) Electrostatic potential distribution inside the PVDD quarter-pixel. Vertical cutlines are K1 and K2 are illustrated. (b) Electrostatic potential on the vertical cutlines K1 and K2 corresponding to the case when P1 and N1 are biased at $-60$ V, N2 is at 15 V, and P2 is at 0 V. The figure illustrates the realisation of a constant 3 V horizontal potential barrier between the middle and the edge of the pixel as well as the realisation of a constant vertical drift field inside the substrate when the distance from the surface is 100 $\mu$m or more.
Figure 7. Simulation results for 300 µm thick PVDD: (a) Electrostatic potential distribution at a vertical 2D cross-section of the PVDD quarter-pixel. P1 and N1 are at −30 V, N2 is at 15 V, and P2 is at 0 V. The vertical cutline L1 is illustrated. (b) Electrostatic potential distribution on a central horizontal cross-section of the PVDD quarter-pixel of figure 5a. The figure illustrates the realisation of a horizontal electrostatic potential barrier between the middle (L1) and the edge (L2) of the pixel.

Figure 8. Simulation results for a 600 µm thick PVDD: (a) Electrostatic potential distribution at a 2D vertical cross-section of the PVDD quarter-pixel. P1 and N1 are at −60 V, N2 is at 15 V, and P2 is at 0 V. The vertical cutline K1 is illustrated. (b) Electrostatic potential distribution on the central horizontal cross-section of the PVDD quarter-pixel of figure 6a. The electrostatic potential barrier between the middle (K1) and the edge (K2) of the pixel is illustrated in the image.
Figure 9. Electrostatic potential distribution inside the PVDD quarter-pixel when electrons are flowing from N1 to N2. P1 is at $-30$ V, N1 is at $-30.5$ V, N2 is at 15 V, and P2 is at 0 V. The electron flow at the centre of the pixel is so intense that a non-depleted area marked with white lines is formed around the symmetry axis of the pixel.

Figure 10. (a) Electrostatic potential distribution on a central horizontal cross-section of the PVDD quarter-pixel of figure 8. The border of the non-depleted n type substrate is depicted by the white line in the lower left corner of the figure. P1 is at $-30$ V and N1 is at $-30.5$ V, N2 is at 15 V and P2 is at 0 V. A cutline is presented with symbol R. (b) Electrostatic potential graphs C1, C2, C3, C4, and C5 on the cutline R. These graphs correspond to the cases when N1 is biased at $-30.1$ V, $-30.2$ V, $-30.3$ V, $-30.4$ V, and $-30.5$ V respectively. P1 is at $-30$ V, N2 is at 15 V, and P2 is at 0 V.
Figure 11. 100 ns light pulse simulation on a 300 µm thick PVDD quarter-pixel. The curve corresponds to the electron current at the n+ type contact N2 as a function of time. The change in the current is due to the light pulse.

source. The downside of the tilted holes is, however, that it is difficult to realise with existing standard manufacturing tools. In case the PVDD is operated in pulsed manner so that an electron flow is generated sporadically along the pixel drift path then it is possible to fill the electron traps located along the drift path. This would increase the signal particularly in detectors that are made of semiconductor materials being prone to trapping.

Afore said benefits of the PVDD concept may enable to expand the operational range of silicon and germanium based radiation detectors to higher energies without degrading the detector performance. Thus in some applications it may be possible to use silicon or germanium detectors instead of compound semiconductor detectors which are expensive, difficult to process, and prone to lattice defects. On the other hand, the PVDD concept may also improve the performance of compound semiconductor detectors so that it could be possible in some applications to replace indirect conversion radiation detectors with direct conversion compound semiconductor radiation detectors. Yet another advantage of the PVDD in compound semiconductor applications is that the typical disproportion between the electron and hole mobilities can be exploited by choosing the electrons as signal charges and by choosing the holes as the charge type forming the resistive paths. In this manner the signal charge collection time as well as the power consumption could be minimized in the PVDD.

It should be possible to utilise the PVDD concept (comprising a detector edge functioning as a resistive path) in edgeless tileable detector configurations in such a manner that radiation induced charge generated inside an edge or corner pixel is also confined to it. In other words the detector
edge should not repel charge from edge or corner pixels to neighbouring pixels. This would, however, need to be verified with 3D simulations by checking that the horizontal potential barriers in the edge and corner pixels can be made large enough in order to prevent blooming of signal charge from one pixel to another.

The authors acknowledge that manufacturing challenges must be overcome before the PVDD concept could offer a practical alternative to existing radiation detectors. Furthermore, in order to bring forth the research a PVDD demonstrator would need to be manufactured. This is, however, out of reach for the authors of this paper and thus collaboration on the matter would be warmly welcomed.

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