Toward Super-Polynomial Size Lower Bounds for Depth-Two Threshold Circuits

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Abstract

Proving super-polynomial size lower bounds for $TC^0$, the class of constant-depth, polynomial-size circuits of Majority gates, is a notorious open problem in complexity theory. A major frontier is to prove that $NEXP$ does not have poly-size $THR \circ THR$ circuit (depth-two circuits with linear threshold gates).

In recent years, R. Williams proposed a program to prove circuit lower bounds via improved algorithms. In this paper, following Williams’ framework, we show that the above frontier question can be resolved by devising slightly faster algorithms for several fundamental problems:

- **Shaving Logs for $\ell_2$-Furthest-Pair.** An $n^2 \ poly(d) / log^{\omega(1)} n$ time algorithm for $\ell_2$-Furthest-Pair in $\mathbb{R}^d$ for polylogarithmic $d$ implies $NEXP$ has no polynomial size $THR \circ THR$ circuits. The same holds for Hopcroft’s problem, Bichrom.-$\ell_2$-Closest-Pair and Integer Max-IP.

- **Shaving Logs for Approximate Bichrom.-$\ell_2$-Closest-Pair.** An $n^2 \ poly(d) / log^{\omega(1)} n$ time algorithm for $(1 + 1/\log^{\omega(1)} n)$-approximation to Bichrom.-$\ell_2$-Closest-Pair or Bichrom.-$\ell_1$-Closest-Pair for polylogarithmic $d$ implies $NEXP$ has no polynomial size $SYM \circ THR$ circuits.

- **Shaving Logs for Modest Dimension Boolean Max-IP.** An $n^2 / log^{\omega(1)} n$ time algorithm for Bichromatic Maximum Inner Product with vector dimension $d = n^\varepsilon$ for any small constant $\varepsilon$ would imply $NEXP$ has no polynomial size $THR \circ THR$ circuits. Note there is an $n^2 \ polylog(n)$ time algorithm via fast rectangle matrix multiplication.

Our results build on two structure lemmas for threshold circuits: a poly-size $THR \circ THR$ circuit can be written as

- an OR of polynomially many poly-size $THR \circ MAJ$ circuits;
- an OR of sub-exponentially many poly-size $MAJ \circ MAJ$ circuits, or as an OR of polynomially many sub-exponential size $MAJ \circ MAJ$ circuits.

The second structure lemma itself only gives a randomized reduction, which we derandomize nondeterministically to apply Williams’ connection.

With similar techniques, we also show slightly improved algorithms for $MAX$-$SAT$ and $k$-$SAT$ would imply interesting circuit lower bounds:

- **Better Algorithms for $MAX$-$SAT$ Implies Super-quasi-polynomial $SYM \circ AND$ Lower Bounds.** A $2^{n - (1 - 1/\log m)^{\omega(1)}}$ time algorithm for $MAX$-$SAT$ implies that $NEXP$ has no quasi-polynomial size $SYM \circ AND$ circuits. This is to be contrasted with CNF-$SAT$, which admits a $2^{n - (1 - 1/\log(m/n))}$ time algorithm.

- **Better Algorithms for $k$-$SAT$ Breaks the log log $n$ Depth Barrier for TC Circuits.** An algorithm for $k$-$SAT$ in $2^n (1 - 1/k^{\omega(\log \log k)})$ time implies that $E^{NP}$ has no linear size (in terms of wires) $O(\log \log n)$-depth TC circuits. The best known algorithm runs in $2^n (1 - 1/O(k))$ time.

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1 Introduction

What interesting functions do not have polynomial-size $\text{TC}^0$ circuits? Despite substantial research effort on this question [HMP+93, AK10, AM05, CS15, EKL+01, GHR92, GT93, HP10, HP15, IPS13, IPS97, Nis93, PS94, ROS94, Wil14a, Tam16, ACW16, KW16] it is consistent with current knowledge that $\text{NEXP}$ has polynomial-size $\text{THR} \circ \text{THR}$ or $\text{SYM} \circ \text{THR}$ circuits.

In 2011, a breakthrough result of R. Williams [Wil14b, Wil13a] showed that $\text{NEXP}$ does not have polynomial-size $\text{ACC}^0$ circuits, by connecting an appealing algorithmic approach to circuit lower bounds: circuit lower bounds can be proved by slightly-better-than-trivial circuit-analysis algorithms for problems such as satisfiability or derandomization. Along these lines, several subsequent works follow Williams’ program [Wil13b, Wil14a, BV14, JMV15, ACW16, Wil16, Tam16], and lower bounds for more circuit classes have been proved by introducing new algorithms, or tightening the connection itself. For an example of the latter, in the recent exciting work by Murray and Williams [MW17], it is shown that $\text{NTIME}[n^{\text{poly(log(n)}}]$ does not have polynomial-size $\text{ACC}^0 \circ \text{THR}$ circuits, via a new Easy Witness Lemma.

The next big challenge for complexity theorists would be to apply Williams’ connection to prove that $\text{NEXP}$ (even $\text{NQP}^2$) is not contained in depth-2 threshold circuits. In fact, partial results are already made. In [Tam16, ACW16], it is shown that $\text{E}^{\text{NP}}$ is not contained in $n^{2-o(1)}$ size $\text{THR} \circ \text{THR}$ circuits.

In this paper, we apply Williams’ connection, together with many new and old tools from the structure theory of threshold circuits, to show that super-polynomial circuit lower bounds for $\text{THR} \circ \text{THR}$ or $\text{SYM} \circ \text{THR}$ would follow from tiny improvements (shaving all polylogs) over the running time of many fundamental problems in computational geometry.

We also consider two other well-studied fundamental problems MAX-SAT and $k$-SAT: the canonical NP-hard optimization problem and the canonical NP-complete problem. The state-of-the-art algorithms for MAX-SAT are much slower than that of CNF-SAT, and the best known running time for $k$-SAT has remained at $2^{n(1-1/O(k))}$ for 20 years. We show that (very) modest improvements on their current state-of-the-art algorithms would imply lower bounds for $\text{SYM} \circ \text{AND}$ circuits, and for $O(\log \log n)$-depth $\text{TC}$ circuits. These results for MAX-SAT and $k$-SAT can be interpreted in two ways: either as a barrier for getting faster algorithms because proving circuit lower bounds is generally considered hard, or as a new approach for attacking those long-standing open questions in circuit complexity, providing extra motivations for studying these two problems.

1.1 Our Results

Consequence of Shaving Logs from $\ell_2$-Furthest-Pair and Related Problems

Our first result is that shaving logs from $\ell_2$-Furthest-Pair or other related problems in computational geometry would resolve our open problem in circuit complexity.

Theorem 1.1. If any of the following problems has an $n^2 \text{poly}(d)/\log^{\omega(1)} n$ time deterministic algorithm for polylogarithmic $d$, then $\text{NEXP}$ has no polynomial size $\text{THR} \circ \text{THR}$ circuits:

1. $\mathbb{Z}$-OV$_{n,d}$ (Hopcroft’s Problem): Find an orthogonal pair among $n$ points in $\mathbb{Z}^d$.
2. $\ell_2$-Furthest-Pair$_{n,d}$: Find the $\ell_2$-furthest pair among $n$ points in $\mathbb{R}^d$.
3. Bichrom.$\ell_2$-Closest-Pair$_{n,d}$: Given two set $A, B$ of $n$ points in $\mathbb{R}^d$, compute $\min_{(a,b) \in A \times B} \|a - b\|_2$.

$\text{THR} \circ \text{THR}$ refers to depth-2 circuits consisting of linear threshold gates. $\text{SYM} \circ \text{THR}$ refers to depth-2 circuits consisting of a top $\text{SYM}$ gate and many bottom $\text{THR}$ gates. See Section 2.1 for formal definitions.

$\text{NTIME}[n^{\text{poly(log(n)}}]$
4. **Z-Max-IP** \(_{n,d}^\): Given two sets \( A, B \) of \( n \) vectors from \( \mathbb{Z}^d \), compute 
\[
\max_{(a, b) \in A \times B} a \cdot b.
\]

5. **Weighted-Max-IP** \(_{n,d}^\): Given a weight vector \( w \in \mathbb{Z}^d \) and two sets \( A, B \) of \( n \) vectors from \( \{0, 1\}^d \),
\[
\max_{(a, b) \in A \times B} w \cdot a \odot b, \text{ where } a \odot b := \sum_{i=1}^d w_i \cdot a_i \cdot b_i.
\]

The best known algorithms for **Z-OV**, \( \ell_2 \)-**Furthest-Pair**, **Bichrom.**-\( \ell_2 \)-**Closest-Pair** and **Z-Max-IP** are of running time \( n^{2-1/O(d)} \) \([\text{Mat92}, \text{AESW91}, \text{Yao82}]\), which means there is no improvement when \( d = \Omega(\log n) \). But note that we do not require a truly-subquadratic time algorithm here: we only need to “shave all the logs” from the trivial \( n^2 \) poly(\( d \)) running time for polylogarithmic \( d \), and we only need to do so for one of the above problems. We are optimistic that such algorithms exist, given the rich toolkit (which keeps growing) available for solving geometry problems.

We also remark here that all problems above except for the last one requires \( n^{2-o(1)} \) time when \( d = 2^O(\log^* n) \) under SETH \([\text{Che18}]\). But again that conditional lower bound says nothing about whether shaving logs are possible.

**Consequence of Shaving Logs for Approximate Bichrom.**-\( \ell_2 \)-**Closest-Pair**

Our second result is that shaving logs on problems which are easier than those in the previous section would imply circuit lower bounds for **SYM \circ THR**.

**Theorem 1.2.** If any of following problems has an \( n^2 \) poly(\( d \))/\( \log^{\omega(1)} n \) time deterministic algorithm for polylogarithmic \( d \), then **NEXP** has no polynomial size **SYM \circ THR** circuits:

1. **Max-IP** \(_{n,d}^\): Given two sets \( A, B \) of \( n \) vectors from \( \{0, 1\}^d \), compute 
\[
\max_{(a, b) \in A \times B} a \cdot b.
\]

2. Compute a \((1 + 1/\log^{\omega(1)} n)\)-approximation to **Bichrom.**-\( \ell_2 \)-**Closest-Pair**\(_n\).

3. Compute a \((1 + 1/\log^{\omega(1)} n)\)-approximation to **Bichrom.**-\( \ell_1 \)-**Closest-Pair**\(_n\).

The best known algorithms for \((1 + \varepsilon)\)-approximation to **Bichrom.**-\( \ell_1 \)-**Closest-Pair** or **Bichrom.**-\( \ell_2 \)-**Closest-Pair** runs in \( n^{2-\Omega(1/3)} \) time, while the best known algorithm for **Max-IP** \(_{n,d}^\) runs in \( n^{2-\Omega(1/\sqrt{d}\log n)} \) time (for \( d \gg \log n \)). For those algorithms, there is no improvement when \( \varepsilon \ll 1/\log^3 n \) or \( d \gg \log^3 n \).

Also, note that all these problems require \( n^{2-o(1)} \) time when \( d = \omega(\log n) \) under SETH \([\text{Rub18}, \text{Wil05}]\). But again it seems plausible that there are some clever ways to shave logs in higher dimensional cases.

A more fine-grained statement can be made if we relax **NEXP** to \( \text{E}^{\text{NP}} \):

**Theorem 1.3.** Suppose for a real \( k > 2 \), one of the following deterministic algorithms exists:

1. An \( n^2 \) poly(\( k \))-time algorithm for **Max-IP** \(_{n, \log^k n}^\).

2. A \((1 + 1/\log^k n)\)-approximation algorithm for **Bichrom.**-\( \ell_1 \)-**Closest-Pair**\(_n\) in \( n^{2/\log^{\omega(1)} n} \) time.

3. A \((1 + 1/\log^k n)\)-approximation algorithm for **Bichrom.**-\( \ell_2 \)-**Closest-Pair**\(_n\) in \( n^{2/\log^{\omega(1)} n} \) time.

Then \( \text{E}^{\text{NP}} \) has no \( n^{(k-2)/2 - \varepsilon_1} \)-size **SYM \circ SYM** circuits for any \( \varepsilon_1 > 0 \).

**Remark 1.4.** Note that **SYM \circ SYM** and **SYM \circ THR** are equivalent up to a polynomial size blow-up \([\text{HP10}, \text{GHR92}]\). See also Proposition 2.7 (4).
Consequence of Shaving Logs for Modest Dimension Boolean Max-IP

Our third result is that shaving logs from moderate dimension Max-IP would imply super-polynomial lower bound for \( \text{THR} \circ \text{THR} \).

**Theorem 1.5.** If any of the following deterministic algorithms exists, then \( \text{NEXP} \) has no polynomial-size \( \text{THR} \circ \text{THR} \) circuits:

1. An algorithm solving \( \text{Max-IP}_{n,n^\varepsilon} \) in \( n^2 / \log^{o(1)}(n) \) time, for a constant \( \varepsilon > 0 \).
2. An algorithm solving \( \text{Max-IP}_{n,\log^k(n)} \) in \( n^{2-\varepsilon} \) time for a constant \( \varepsilon > 0 \) and any integer \( k \).

Note that for small enough \( \varepsilon > 0 \), \( \text{Max-IP}_{n,n^\varepsilon} \) can be solved in \( n^{2 \cdot \text{polylog}(n)} \) time by applying the fast rectangle matrix multiplication algorithm \( \text{[Cop82]} \) to calculate the pair-wise inner products. Therefore, we only need to shave logs on this naive algorithm.

Two Structure Lemmas for \( \text{THR} \circ \text{THR} \) circuits

The major technical ingredients of our results are two structure lemmas for \( \text{THR} \circ \text{THR} \), of interest in its own right.

Informally, the first lemma says every \( \text{THR} \circ \text{THR} \) is equivalent to a polynomial OR of Threshold-of-Majority circuits and the second lemma says that every \( \text{THR} \circ \text{THR} \) circuit is equivalent to a “subexponential OR” of Majority-of-Majority circuits. For the program of proving \( \text{THR} \circ \text{THR} \) lower bounds, this is significant, as exponential-size Majority-of-Majority and Threshold-of-Majority lower bounds are well-known \( \text{[HMP+93, FKL+01]} \).

In the following, DOR refers to a “disjoint” OR gate: an OR gate with the promise that at most one of its inputs is ever true, and Gap-OR refers to a “gapped” OR gate: an OR gate with the promise that either all inputs are false or at least half of the inputs are true. (See Section 2.1 for formal definitions.)

**Lemma 1.6** (Structure Lemma I for \( \text{THR} \circ \text{THR} \) circuit). Let \( n \) be number of inputs and \( s = s(n) \geq n \) be a size parameter. Every \( s \)-size \( \text{THR} \circ \text{THR} \) circuit \( C \) is equivalent to a Gap-OR \( \circ \text{THR} \circ \text{MAJ} \) circuit such that:

- The top Gap-OR gate has \( \text{poly}(s) \) fan-in.
- Each sub \( \text{THR} \circ \text{MAJ} \) circuit has size \( \text{poly}(s) \).

Moreover, the reduction can be computed in deterministic \( \text{poly}(s) \) time.

**Lemma 1.7** (Structure Lemma II for \( \text{THR} \circ \text{THR} \) circuit). Let \( n \) be number of inputs and \( s = s(n) \) be a size parameter. Let \( \varepsilon \in \left( \frac{\log s}{n}, 1 \right) \). For \( s = 2^{o(n)} \), every \( s \)-size \( \text{THR} \circ \text{THR} \) circuit \( C \) is equivalent to a DOR \( \circ \text{MAJ} \circ \text{MAJ} \) circuit such that:

- The top DOR gate has \( 2^{O(\varepsilon n)} \cdot \text{poly}(s) \) fan-in.
- Each sub \( \text{MAJ} \circ \text{MAJ} \) circuit has size \( s^{O(1/\varepsilon)} \cdot \text{poly}(s) \).

Moreover, the reduction can be computed in randomized \( 2^{O(\varepsilon n)} \cdot s^{O(1/\varepsilon)} \cdot \text{poly}(s) \) time.

We discuss some immediate applications of the structure lemmas.
Equivalence of Non-trivial SAT Algorithms. It is well-known that \( \text{THR} \circ \text{THR} \) circuits can be simulated with depth-3 polynomial MAJ \circ \text{MAJ} \circ \text{MAJ} circuits \cite{GHR92}; however, replacing the output MAJ gate with an extremely simple Gap-OR or DOR gate has extra benefits. For example, any faster SAT algorithm for \( \text{THR} \circ \text{MAJ} \) or \( \text{MAJ} \circ \text{MAJ} \) circuits can be used to obtain a SAT algorithm for \( \text{THR} \circ \text{THR} \) easily! Formally, the following two corollaries follow from Lemma 1.6 and Lemma 1.7 directly.

**Corollary 1.8.** The following are equivalent:

- The satisfiability of \( \text{THR} \circ \text{THR} \) circuits of size \( n^k \) can be solved in \( 2^{n/n^k} \) time for any \( k \).
- The satisfiability of \( \text{THR} \circ \text{MAJ} \) circuits of size \( n^k \) can be solved in \( 2^{n/n^k} \) time for any \( k \).

**Corollary 1.9.** The following are equivalent:

- There is a \( 2^{(1-\Omega(1))n} \) time algorithm for the satisfiability of polynomial size \( \text{THR} \circ \text{THR} \) circuits.
- There is a \( 2^{(1-\Omega(1))n} \) time algorithm for the satisfiability of polynomial size \( \text{MAJ} \circ \text{MAJ} \) circuits.

We remark that the first corollary preserves any non-trivial speed up (\( 2^{n/\omega(1)} \) time algorithms), while the second is coarser, which is due to the sub-exponential blowup (when \( \varepsilon \) is an arbitrarily small constant) in Lemma 1.7.

Generalization to Threshold Circuits of Constant Depth. Also, Lemma 1.7 easily generalizes to threshold circuits of any constant depth. In the following LT\(_d\) denotes threshold circuits of depth-\( d \), while \( \hat{\text{LT}}_d \) denotes depth-\( d \) majority circuits (see Section 2.1 for formal definitions).

**Corollary 1.10.** Let \( n \) be number of inputs and \( s = s(n) \) be a size parameter. Let \( \varepsilon \in \left( \frac{\log s}{n}, 1 \right) \) and \( d \) be a constant. For \( s = 2^{o(n)} \), every \( s \)-size \( \text{LT}_d \) circuit is equivalent to a \( \text{DOR} \circ \hat{\text{LT}}_d \) circuit such that:

- The top DOR gate has \( 2^{O(\varepsilon\cdot n)} \) fan-in.
- Each sub \( \hat{\text{LT}}_d \) circuit has size \( O\left(s^{O(1/\varepsilon)}\right) \).

Structure Lemma for Polynomial Threshold Functions. Our ideas can also be used to derive a structure lemma for polynomial threshold functions of degree \( k \), i.e., \( \text{THR} \circ \text{AND}_k \) circuits:

**Corollary 1.11.** Let \( n \) be number of inputs and \( s = s(n) \) be a size parameter. Let \( \varepsilon \in \left( \frac{\log s}{n}, 1 \right) \) and \( k \) be a constant. Assuming \( s = 2^{o(n)} \), an \( s \)-size \( \text{THR} \circ \text{AND}_k \) circuit is equivalent to a \( \text{DOR} \circ \text{MAJ} \circ \text{AND}_{2k} \) circuit such that:

- The top DOR gate has \( 2^{O(\varepsilon\cdot n)} \) fan-in.
- Each sub \( \text{MAJ} \circ \text{AND}_{2k} \) circuit has size \( O\left(s^{O(1/\varepsilon)}\right) \).

The above still holds if we replaced both \( \text{AND}_k \) and \( \text{AND}_{2k} \) by unbounded fan-in AND gates.

That is, every polynomial threshold function of degree \( k \) with arbitrary weights can be simulated by a subexponential-size disjoint OR of polynomial threshold functions of degree \( 2k \) with small weights.

The following corollary follows from that the SAT problem for \( \text{THR} \circ \text{AND}_k \) circuits is equivalent to the weighted \( \text{MAX}-k\text{-SAT} \) problem (given a CNF formula \( \varphi \) with weights on each clause, find an assignment satisfying clauses of maximum total weight), and that SAT for \( \text{MAJ} \circ \text{AND}_{2k} \) is equivalent to the (unweighted) \( \text{MAX}-2k\text{-SAT} \) problem.
Corollary 1.12. For any integer $k$, if there is a $2^{(1-O(1))n}$ time algorithm for polynomial size unweighted \(\text{MAX-2k-SAT}\), then so does polynomial size weighted \(\text{MAX-k-SAT}\).\(^3\)

An Application in Communication Complexity. Finally, Structure Lemma I also has an application in communication complexity.

The connection between threshold circuits and communication lower bounds dates back to \cite{Nis93}, which showed $\text{MAJ} \circ \text{THR}$ circuits admit efficient $\text{PP}^\text{cc}$ protocols, therefore the $\Omega(n)$ $\text{PP}^\text{cc}$ lower bound for IP2 (Inner Product) \cite{CG88} implies that IP2 requires $2^{\Omega(n)}$ size $\text{MAJ} \circ \text{THR}$ circuits. Later, \cite{FKL+01} showed that $\text{THR} \circ \text{MAJ}$ circuits have efficient $\text{UPP}^\text{cc}$ protocols, hence the $2^{\Omega(n)}$ $\text{THR} \circ \text{MAJ}$ circuit size lower bound for IP2 can be derived from the corresponding $\text{UPP}^\text{cc}$ lower bound for it \cite{For02}.

Naturally, one may seek similar connections for $\text{THR} \circ \text{THR}$ circuits. In a recent work, \cite{AW17} showed that $\text{THR} \circ \text{THR}$ admits efficient $\text{BP} \cdot \text{UPP}^\text{cc}$ protocols. However, it seems quite hard to prove $\text{BP} \cdot \text{UPP}^\text{cc}$ lower bounds, as it contains $\text{AM}^\text{cc}$, which itself has been notoriously hard to prove any non-trivial lower bound on $\text{GPW18}$.

In this work, building on our Structure Lemma I for $\text{THR} \circ \text{THR}$ circuits. We show that $\text{THR} \circ \text{THR}$ circuits admit efficient $\text{RP} \cdot \text{UPP}^\text{cc}$ protocols, which could be potentially easier to prove a lower bound on.

Theorem 1.13. For a function $F : \{0,1\}^n \times \{0,1\}^n \rightarrow \{0,1\}$, suppose it admits a $\text{THR} \circ \text{THR}$ circuit of size $s$, then it also admits a $\text{RP} \cdot \text{UPP}^\text{cc}$ protocol of cost $O(\log s)$.

Remark 1.14. Therefore, a $\log^{o(1)} n$ lower bound on $\text{RP} \cdot \text{UPP}^\text{cc}$ complexity for a function $F$, implies that $F$ requires $n^{\omega(1)}$-size $\text{THR} \circ \text{THR}$ circuits.

See Appendix B for details and a formal definition of $\text{RP} \cdot \text{UPP}^\text{cc}$ protocols.

MAX-SAT and SYM $\circ$ AND Circuit Lower Bounds

Being the canonical NP-hard optimization problem, a huge amount of research effort has been devoted to finding faster-than-$2^n$ algorithms for MAX-SAT \cite{BR99, BF10, BG12, CK04, DW06, GS12, GS17, GK14, GHNR03, GN00, Hir00, Hir03, KMRR05, KK06, Ku05, KK07, MR99, NR00, SST15, SS03, Wi05}.

In terms of getting non-trivial speed up, in \cite{SSTT16}, a $2^{n-n^{\Theta(1)}}$ time algorithm for MAX-SAT of $m = n^k$ clauses is proposed, which doesn’t give any improvement when $m = n^{\Omega(\log n)}$.

This state of affairs is certainly unsatisfactory, as $k$-SAT and CNF-SAT are known to have much better algorithms: $k$-SAT is solvable in $2^{(1-1/O(k))n}$ time \cite{PPSZ05}, while CNF-SAT admits a $2^{(1-\Omega(1)/\log(m/n))n}$ time algorithm \cite{CIP06, DH09}, which gives a non-trivial speedup even for sub-exponential $m$.

Our next result give some evidence why progress on MAX-SAT has been limited. We show that a very modest improvement over the best known MAX-SAT algorithm would imply super-quasi-polynomial circuit lower bounds for SYM $\circ$ AND circuits.

Theorem 1.15. If there is an algorithm for MAX-SAT solving an instance with $2^{\log^k n}$ clauses in $2^n/2^{\log^k n}$ time for every integer $k$. Then $\text{NEXP}$ has no quasi-polynomial size $\text{SYM} \circ \text{AND}$ circuits.

Corollary 1.16. An algorithm for MAX-SAT with $m$ clauses in $2^n\left(1-1/2^{\log m}o(1)\right)$ time implies that $\text{NEXP}$ has no quasi-polynomial size $\text{SYM} \circ \text{AND}$ circuits.

\(^3\)We assume the weights are at most $2^{\text{poly}(n)}$ for making the input polynomial size.
Moreover, if the running time for MAX-SAT can be improved to the same as the best-known algorithms for CNT-SAT, then we would have a much stronger circuit lower bound.

**Theorem 1.17.** If there is a $2^{n-o(n/\log n)}$ time algorithm for MAX-SAT with $m$ clauses, then $E^{NP}$ has no $2^{o(\sqrt{n})}$-size $SYM \circ AND$ circuit.

**SYM \circ AND Circuits Lower Bounds.** The best non-trivial lower bound for $SYM \circ AND$ is an $n^{\Omega(\log n)}$ size lower bound for a function in $ACC^0$ [RW93]. Historically, quasi-polynomial size $SYM \circ AND$ circuits are studied mainly because it contains the circuit class $ACC^0$ by depth-reduction [Yao90, BT94, AG94], and it is connected to Number-On-Forehead communication protocols [HG91]. It was considered as a viable approach to prove $ACC^0$ circuit lower bounds. However, even Williams’ breakthrough work on $ACC^0$ makes crucial use of the depth-reduction result $ACC^0 \subseteq SYM \circ AND$, it is not clear how to prove super quasi-polynomial lower bound on $SYM \circ AND$ itself via his approach, which is unsatisfying.

This question is also interesting as exponential lower bounds for $MAJ \circ AND$ are trivial to obtain (in fact, even exponential lower bound for $THR \circ MAJ$ are known [FKL+01]). It would be good to understand why switching the top gate to a $SYM$ gate makes the problem much harder.

**k-SAT and the log log $n$-Depth Barrier for TC Circuits**

Finally, we show a modestly improved algorithm for $k$-SAT (recall the state-of-the-art running time is $2^{n-(1-1/O(k))}$) would imply lower bounds for $O(\log \log n)$-depth TC circuits. This is based on the reduction from TC-SAT to $k$-SAT in a recent work by Abboud et al. [ABDN18].

**Theorem 1.18.** A $2^{n-(1-k^{1/(\log \log k)})}$ time algorithm for $k$-SAT implies that for any constant $c > 1$, $E^{NP}$ has no $cn$-wire depth-$c(\log \log n)$ TC circuit.

**log log $n$-depth Barrier for TC.** In [IPS97], it is shown that parity requires $n^{1+\epsilon/d}$-wires for depth-$d$ TC circuits, which becomes linear when $d = \Omega(\log \log n)$. No non-trivial super-linear wires lower bounds are known when the depth is $\Omega(\log \log n)$. It is consistent with the current state of knowledge that $E^{NP}$ could be contained in linear-size $O(\log \log n)$-depth TC circuits.

### 1.2 Related Works

**Constant-Depth Threshold Circuit Lower Bounds.** For more history on previous works on lower bounds for constant-depth threshold circuits, see the corresponding sections in [Wil14a, KW16]. We only discuss a few recent results here.

In 2014, Williams [Wil14a] showed that $NEXP$ is not contained in $ACC_0 \circ THR$, by devising a fast satisfiability algorithm for it. The lower bound was recently improved by Murray and Williams [MW17] to that $NQP$ is not contained in $ACC_0 \circ THR$. Tamaki [Tam16], Alman, Chan and Williams [ACW16] proved that $E^{NP}$ is not contained in $n^{2-o(1)}$ size $THR \circ THR$ circuits (the results in [ACW16] is stronger, it in fact showed lower bound against $ACC_0 \circ THR \circ THR$ circuits, with at most $n^{2-\epsilon}$ bottom $THR$ gates). Most recently, Williams [Wil18a] showed that there are functions in $NQP$ that can not be represented by a linear combination of polynomially many $ACC \circ THR$ circuits.

Tell [Tel17] constructed a quantified derandomization algorithm for TC circuits with depth $d$ and $n^{1+\exp(-d)}$ wires, and showed that a modest improvement of his algorithm would imply standard derandomization of $TC^0$, and consequently $NEXP \not\subset TC^0$.

Using random restriction, Kane and Williams [KW16] proved that any $THR \circ THR$ circuits computing Andreev’s function requires $\Omega(n^{1.5})$ gates and $\Omega(n^{2.5})$ wires. Chattopadhyay and Mande [CM17] showed an
exponential size separation between $\text{THR} \circ \text{MAJ}$ and $\text{THR} \circ \text{THR}$, by constructing a function in $\text{THR} \circ \text{THR}$ with exponential sign-rank.

**Shaving Logs Implies Circuit Lower Bound.** Abboud et al. [AHVW16] showed that shaving logs on some well-studied sequence alignment problems like Edit-Distance and Longest Common Subsequence would imply strong circuit lower bounds. In particular, they proved that an $n^2 / \log^{\omega(1)} n$ time algorithm for either of them would imply a $2^{n^2 / \log^7 n} n$ time algorithm for poly-size Formula-SAT, from which it follows $\text{NEXP}$ is not contained in $\text{NC}^1$. Their reduction is later tightened by Abboud and Bringmann [AB18], which showed that an $n^2 / \log^{7+\varepsilon} n$ time algorithm for either of them is already enough to imply a $2^{(\log \log N)^{\varepsilon}} n$ time algorithm for poly-size Formula-SAT. Chen et al. [CGL18] showed that shaving a $2^{(\log \log N)^{\varepsilon}}$ factor from the naive algorithm for (constant factor) approximate Closest-LCS-Pair and many other problems also implies $\text{NEXP}$ is not contained in $\text{NC}^1$.

## 2 Preliminaries

We begin with some notations for operations on vectors. For two vectors $u, v \in \{0, 1\}^*$, we use $u \circ v$ to denote their concatenation. For a vector $u$ and an integer $t$, we use $u^{\otimes t}$ to denote the vector obtained by repeating $u$ $t$ times.

### 2.1 Circuits Classes

Since we discuss many circuits class in this work, we begin with some notations for those classes.

**Notations for Circuit Classes.** Let $x \in \{0, 1\}^n$ be a Boolean input. For $w \in \mathbb{R}^n$ and $t \in \mathbb{R}$, we define $\text{THR}_{w,t}(x)$ (the threshold function) to be the indicator function that whether $w \cdot x \geq t$. Similarly, we define $\text{ETHR}_{w,t}(x)$ (the exact threshold function) to be the indicator function that whether $w \cdot x = t$. The vector $w$ and the real $t$ are called the weights and the threshold of the given function $\text{THR}_{w,t}$ ($\text{ETHR}_{w,t}$). We say these weights and thresholds are realizations of the Boolean functions they defined. Note that a function may have different realizations. One may assume without loss of generality that the weights and thresholds are integers of absolute value at most $2^{O(n \log n)}$ [MTT61, BHPS10]. For a threshold or exact threshold function with weight $w$, we call the linear function $L := w \cdot x$ its associated linear function.

We use $\text{MAJ}_n$ and $\text{EMAJ}_n$ to denote the corresponding threshold (exact threshold) functions when all weights are 1. Slightly abusing notations, we use $\text{THR}$, $\text{ETHR}$, $\text{MAJ}$, $\text{EMAJ}$ to also denote the corresponding classes of functions. We also consider $\text{AND}_n$ and $\text{OR}_n$, with their usual meanings. We use $\text{DOR}_n$ to denote the disjoint OR function, that is, an OR function with the promise that at most one input bit could be true.

We use $\text{Gap-OR}_n$ to denote the gap OR function, that is, an OR function with the promise that either all inputs are false or at least half of inputs are true. We also use $\text{SYM}$ to denote the class of all symmetric functions. For a $\text{SYM}$ function $C$, we have $C(x) := f \left( \sum_{i=1}^n x_i \right)$, and we call $f$ as its associated function.

For a class of function like $\text{THR}$, we use $\text{THR}_k$ to denote its sub-class with at most $k$ inputs. For two classes of functions like $\text{THR}$ and $\text{SYM}$, we use $\text{THR} \circ \text{SYM}$ to denote the corresponding class of depth-2 circuits. Similar notations are used for more than 2 classes.

---

4Given two sets $A, B$ of strings, compute $\max_{(a,b) \in A \times B} \text{LCS}(a, b)$.
We use $\mathsf{LT}_d$ to denote the depth-$d$ THR circuit class, that is, $\mathsf{LT}_d := \mathsf{THR} \circ \ldots \circ \mathsf{THR}_d$. Similarly, we use $\hat{\mathsf{LT}}_d$ to denote its unweighted version, that is, $\hat{\mathsf{LT}}_d := \mathsf{MAJ} \circ \ldots \circ \mathsf{MAJ}_d$.

When we refer to a circuit class without specifying its size, we always assume the size is polynomial.

**Previous Known Containment Results.** We need the following standard circuit classes containment results for this paper.

**Proposition 2.1.** The following holds:

1. $\mathsf{SYM}_k \subseteq \mathsf{DOR}_k \circ \mathsf{EMAJ}$.  
2. $\mathsf{THR} \subseteq \mathsf{MAJ} \circ \mathsf{MAJ}$ \cite{GHR92,Hof96}.
3. $\mathsf{THR} \subseteq \mathsf{DOR} \circ \mathsf{ETHR}$ \cite{HP10}.
4. $\mathsf{SYM} \circ \mathsf{THR}$ and $\mathsf{SYM} \circ \mathsf{ETHR}$ are contained in $\mathsf{SYM} \circ \mathsf{MAJ}$ \cite{GHR92,HP10}.
5. $\mathsf{MAJ} \circ \mathsf{THR}$ and $\mathsf{MAJ} \circ \mathsf{ETHR}$ are contained in $\mathsf{MAJ} \circ \mathsf{MAJ}$ \cite{GHR92,HP10}.
6. $\mathsf{SYM} \circ \mathsf{SYM} \subseteq \mathsf{SYM} \circ \mathsf{MAJ}$.
7. $\mathsf{ETHR} \circ \mathsf{ETHR} \subseteq \mathsf{THR} \circ \mathsf{THR}$ \cite{HP10}.
8. $\mathsf{AND} \circ \mathsf{ETHR} \subseteq \mathsf{ETHR}$ \cite{HP10}.
9. $\mathsf{AND}_k \circ \mathsf{SYM} \subseteq \mathsf{SYM}$ \cite{HP10} for a constant $k$.
10. $\mathsf{EMAJ} \subseteq \mathsf{MAJ} \circ \mathsf{AND}_2$ \cite{HP10}.

Moreover, all statements above have corresponding polynomial-time, deterministic constructions.

**Remark 2.2.** We remark that for Item (4) and (5), only Item (5) is explicitly stated in \cite{HP10}, but it is not hard to see that the technique works equally well with a top $\mathsf{SYM}$ gate.

We also need the following folklore lemma, which helps us to transform between $\mathsf{MAJ} \circ \mathsf{AND}$ circuits and $\mathsf{MAJ} \circ \mathsf{OR}$ circuits.

**Lemma 2.3.** Let $x = x_1, x_2, \ldots, x_k$ be the inputs, there are $k$ OR functions $O_1, O_2, \ldots, O_k$ on the inputs (or their negations) such that:

$$ \mathsf{AND}(x) = \left( \sum_{i=1}^{k} O_i(x) \right) - (k - 1). $$

**Proof.** We define

$$ O_i(x) := \left( \bigvee_{j=1}^{i-1} \lnot x_j \right) \lor x_i. $$

That is, $O_i(x) = 0$ if and only if the first $i - 1$ bits are 1, and the $i$-th bit is 0. Now, note that if $\mathsf{AND}(x) = 1$, then all bits are 1, which means all $O_i(x)$'s are 1. When $\mathsf{AND}(x) = 0$, let $i$ be the index of the first 0-bit, it is easy to see that $O_i(x) = 0$ and all other $O_j(x)$'s are 1, and hence $\sum_{i=1}^{k} O_i(x) = k - 1$. \[\square\]
2.2 Lower Bound From Non-trivial Satisfiability Algorithm

Here we introduce the algorithm-to-lower bound tools established in a serious works of Williams [Wil13a, Wil14b], and simplified by Ben-Sasson and Viola [BSV14].

Let $C$ be a circuit class, we use $C^s_n$ to denote the subset of $C$ with $n$ inputs and size $\leq s$. Slightly abusing notation, we also use $C^s_n$ to denote the corresponding functions of the circuits in $C^s_n$.

We say a circuit class $C$ is efficiently close under projections, if given the description of a circuit $C$ from $C^s_n$, for indices $i, j \leq n$ and a bit $b$, the following functions

$$- C, C(x_1, \ldots, x_{i-1}, x_j \oplus b, x_{i+1}, \ldots, x_n), C(x_1, \ldots, x_{i-1}, b, x_{i+1}, \ldots, x_n)$$

belong to $C^s_n$, and their corresponding circuit descriptions can be constructed in poly($s$) time.

The following is from [BSV14], we reformulate it a bit for our use here.

**Theorem 2.4** (Theorem 1.5 [BSV14]). Let $s : \mathbb{N} \to \mathbb{N}$ be a growing parameter of $n$, $C$ be efficiently closed under projections and $C_n = C^s_n(n)$. If the satisfiability of functions $h = g_1 \land g_2 \land g_3$ where $g_i \in C_{n+n^2}$ in $\text{TIME}(2^n/n^2\text{(1)})$, then there is a function $f$ in $\text{E}^{\text{NP}}$ such that $f_n \notin C_n$ for infinitely many $n$’s.

We also need the following two similar connections with circuit lower bound against $\text{NEXP}$.

**Theorem 2.5** ([BSV14] [Wil13a]). Let $C$ be efficiently closed under projections. If there is an algorithm solving the satisfiability of functions $h = g_1 \land g_2 \land g_3$ where $g_i \in C_{n+n^2}$ in $O(2^n/n^2\text{(1)})$ time for all $k$, then $\text{NEXP}$ does not have polynomial size $C$ circuits.

**Theorem 2.6** ([BSV14] [Wil13a]). Let $C$ be efficiently closed under projections. If there is an algorithm solving the satisfiability of functions $h = g_1 \land g_2 \land g_3$ where $g_i \in C^s_n(n)$ where $s = 2^{\log^k n}$ in $O(2^n-n^k)$ time for all $k$, then $\text{NEXP}$ does not have quasi-polynomial size $C$ circuits.

**Remark 2.7.** We remark that algorithms in both Theorem 2.5 and Theorem 2.6 can in fact be replaced by co-nondeterministic algorithms with the same running times.

3 Structure Lemmas for THR $\circ$ THR Circuits

In this section we present our structure lemmas for THR $\circ$ THR circuits, and discuss some applications.

We first need a simple construction, which will be used in both proofs.

**Lemma 3.1** (Mod $p$ exact threshold gate). Let $G$ be a ETHR gate with $n$ inputs, $p$ be a prime and $G^p$ be the “mod $p$” version of $G$. That is, let $L$ and $T$ be the corresponding linear function and threshold of $G$, $G^p(x) := [L(x) \equiv T \pmod{p}]$.

Then $G^p$ can be written as a DOR $\circ$ ETHR circuit such that

- The top DOR gate has $O(n)$ fan-in.
- All ETHR gates have positive weights and thresholds smaller than $O(np)$.

**Proof.** Let $w_1, w_2, \ldots, w_n$ and $T$ be the corresponding weights and threshold of $G$. We reduce each weight $w_i$ in $G$ to $w_i \mod p$, and get another circuit with associate top linear function $L'(x)$. We set $t = T \mod p$, then $L(x) \equiv T \pmod{p}$ is equivalent to $L'(x) = t + k \cdot p$ for some $k \in \{0, 1, 2, \ldots, n\}$. Therefore, by enumerating $k$ from 0 to $n$, we can construct the equivalent DOR $\circ$ ETHR circuit. $\square$
3.1 Proof for Structure Lemma I

We begin with the proof for Structure Lemma I for THR ◦ THR circuits (restated below).

**Reminder of Lemma 1.6** Let \( n \) be number of inputs and \( s = s(n) \geq n \) be a size parameter. Every \( s \)-size THR ◦ THR circuit \( C \) is equivalent to a \( \text{Gap-OR} \circ \text{THR} \circ \text{MAJ} \) circuit such that:

- The top \( \text{Gap-OR} \) gate has \( \text{poly}(s) \) fan-in.
- Each sub \( \text{THR} \circ \text{MAJ} \) circuit has size \( \text{poly}(s) \).

Moreover, the reduction can be computed in deterministic \( \text{poly}(s) \) time.

**Proof.** Let \( C' \) be the given \( \text{THR} \circ \text{THR} \) circuit. By negating some of its input gates (THR is closed under negation), we can assume all weights in the top THR gate of \( C' \) are \( \leq 0 \). By Proposition 2.1 (3), \( C' \) can be transformed into an equivalent \( \text{THR} \circ \text{ETHR} \) circuit \( C \) of size \( t = \text{poly}(s) \).

Let \( G_1, G_2, \ldots, G_t, w_1, w_2, \ldots, w_t \) be the ETHR gates on the bottom layer and their corresponding weights in the top gate in \( C \). By assumption, we also have all \( w_i \leq 0 \). Let \( T \) be the threshold of the top gate in \( C \). For all input \( x \), we have

\[
C(x) = \left[ \sum_{i=1}^{t} w_i \cdot G_i(x) \geq T \right].
\]

By construction, we can assume that weights in \( G_i \) are bounded by \( 2^{nc} \) for a large constant \( c \). Fix an input \( x \), let \( p \) be a random prime from \( 2 \) to \( n^{2c} \cdot t^2 \cdot 10 = \text{poly}(s) \), then with probability at least \( 1 - 1/10t \), we have \( G_i^p(x) = G_i(x) \). Let \( C^p \) be the circuit obtained by replacing all \( G_i \)'s in \( C \) by corresponding \( G_i^p \)'s.

Then we have: (1) when \( C(x) = 1 \), by a union bound, with probability at least \( 1 - 1/10t \), \( C^p(x) = C(x) = 1 \). (2) when \( C(x) = 0 \), note that for all prime \( p \), we have \( G_i^p(x) \geq G_i(x) \) for all \( i \), therefore we must have \( \sum_{i} w_i \cdot G_i^p(x) \leq \sum_{i} w_i \cdot G_i(x) < T \) (all \( w_i \)'s are \( \leq 0 \)) and \( C^p(x) = 0 \). Hence, \( C \) is equivalent to a \( \text{Gap-OR} \) of all \( C^p \)'s, and by Lemma 3.1 each \( C^p \) can be written as a \( \text{poly}(s) \) size \( \text{THR} \circ \text{MAJ} \) circuit, which completes the proof.

3.2 Proof for Structure Lemma II

We next prove Lemma 1.7. The proof consists of two steps, which are specified by Lemma 3.2 and Lemma 3.4.

**Lemma 3.2 (Weight Reduction at the Top THR gate).** Given a \( \text{THR}_d \circ \mathcal{C} \) circuit (a circuit with a top THR gate of fan-in \( d \)) of size \( s \), it is equivalent to a \( \text{DOR} \circ \text{ETHR} \circ \mathcal{C} \) circuit such that:

- The top \( \text{DOR} \) gate has \( \text{poly}(d) \) fan-in.
- Each \( \text{ETHR} \) gate has fan-in \( d \), whose weights and threshold are positive and smaller than \( \text{poly}(d) \cdot 2^n \).
- The \( \mathcal{C} \) part is unchanged.

The same statement also holds for a \( \text{ETHR}_d \circ \mathcal{C} \) circuit. Moreover, these reductions can be computed in randomized \( \text{poly}(s) \) time.
Proof. We only consider the $\text{THR}_d \circ \mathcal{C}$ case, the $\text{ETHR}_d \circ \mathcal{C}$ case is only simpler.

Let $C$ be the given circuit. First, by Proposition 2.1(5), $C$ can be transformed to an equivalent $\text{DOR} \circ \text{ETHR} \circ \mathcal{C}$ circuit $C'$.

Now, we deal with each $\text{ETHR}$ gate $G$ separately, note that $G$ also has fan-in $d$. Let $D$ be the sub-circuit with top gate $G$. From the construction, $G$ may have weight of absolute value at most $M_{\text{old}} = 2^{\text{poly}(d)}$.

We next define $L : \{0, 1\}^n \to \mathbb{Z}$ such that $L(x)$ is the value of the linear function associated with the gate $G$ when the input is $x$. That is $D(x) = 1$ if and only if $L(x) = T$ for the threshold $T$ of $G$.

Then we pick a random prime number $m$ from 0 to $M_{\text{new}} = d^c \cdot 2^n$, where $c$ is a sufficiently large constant. For a fixed $x \in \{0, 1\}^n$, if $L(x) \neq T$, the probability that $L(x) \equiv T \pmod{m}$ is smaller than

$$\frac{\log(M_{\text{old}})}{M_{\text{new}}/\ln(M_{\text{new}})} = \frac{\text{poly}(d)}{\Theta(2^n \cdot d^c/(n + c \log d))} \leq d^{-c/2}/2^n,$$

for a sufficiently large $c$. Therefore, by a simple union bound, with probability at least $1 - d^{-c/2}$, we have $L(x) \equiv T \pmod{m}$ if and only if $L(x) = T$ for all $x \in \{0, 1\}^n$. We pick such a prime $m$ for gate $G$.

Finally, by applying Lemma 3.3 with prime $m$, we can replace $G$ with an equivalent $\text{DOR} \circ \text{ETHR}$ sub-circuit, whose $\text{ETHR}$ gates have positive weights and thresholds smaller than $\text{poly}(d) \cdot 2^n$.

By a union bound over all $\text{ETHR}$ gates, and choose $c$ to be a large enough constant, we complete our randomized reduction. \hfill $\square$

Remark 3.3. One can observe that the above reduction indeed only introduces one-sided error. That is, even it chooses some “bad” primes, the resulting circuit $D$ satisfies the property that $D(x) = 1$ whenever $C(x) = 1$.

Lemma 3.4 (Decomposition of the top $\text{ETHR}$ gate). Given an $\text{ETHR}_d \circ \mathcal{C}$ circuit $C$ (a circuit with a top $\text{ETHR}$ gate of fan-in $d$) of size $s$ and a real $\varepsilon \in \left(\frac{\log d}{n}, 1\right)$, suppose the top $\text{ETHR}$ gate in $C$ has positive weights and threshold smaller than $2^{2n}$. $C$ is equivalent to a $\text{DOR} \circ \text{MAJ} \circ \text{AND}_2 \circ \mathcal{C}$ circuit such that:

- The top $\text{DOR}$ gate has $2^{O(\varepsilon n)}$ fan-in.
- Each $\text{MAJ}$ gate has fan-in $d^{O(1/\varepsilon)}$.
- The $\mathcal{C}$ part is unchanged.

Moreover, the reduction can be computed in deterministic time.

$$2^{O(\varepsilon n)} \cdot d^{O(1/\varepsilon)} + \text{poly}(s)$$

Proof. Let $G_{\text{top}}$ be the top $\text{ETHR}$ in $C$ and $G_1, G_2, \ldots, G_d$ be its input gates. Let $w_i$’s and $T$ be the weights and the threshold of $G_{\text{top}}$ and $L(x)$ be the associated linear function, we have

$$L(x) = \sum_{i=1}^d w_i \cdot G_i(x)$$

for all input $x \in \{0, 1\}^n$.

Now, note that the binary representations of $w_i$’s and $T$ are of length at most $\log(2^{2n}) \leq 2n$, and we break them into $D = \left\lceil \varepsilon \cdot n \log d \right\rceil$ blocks, each with $B \leq 2/\varepsilon \cdot \log d$ bits. Let $w_{i,j} \in [2^B - 1]$ and $T_j$ be the
value of \( w_i \)'s and \( T \)'s \( j \)-th block respectively (blocks are numbered from the least significant bit to the most significant bit).

Consider adding up \( w_i \cdot G_i(x) \)'s in \( 2^B \) base and enumerate all \( D - 1 \) carries on each position except for the highest one. Let \( c_1, c_2, \ldots, c_{D-1} \in \{0, 1, \ldots, d - 1\}^{D-1} \) be such a carry sequence. We can see
\[
\sum_{i=1}^{d} w_i \cdot G_i(x) = T \text{ with respect to a carry sequence } c \text{ is equivalent to that for all } j \in [D]:
\]
\[
\sum_{i=1}^{d} w_{i,j} \cdot G_i(x) + c_{j-1} = T_j + 2^B \cdot c_j,
\]
where we set \( C_D \) and \( C_0 \) to be 0 for notational convenience.

That is, after fixing \( c_j \)'s, for all \( j \),
\[
\sum_{i=1}^{d} w_{i,j} \cdot G_i(x) \text{ are also forced to be } T_j^c = T_j + 2^B \cdot c_j - c_{j-1}.
\]

Therefore, consider the sum
\[
\sum_{j=1}^{\varepsilon \cdot n} \left( \sum_{i=1}^{d} w_{i,j} \cdot G_i(x) - L_j^c \right)^2.
\]

Checking whether this sum \( \leq 0 \) can be formulated as a \( \text{poly}(d) \cdot 2^{O(B)} = d^{O(1/\varepsilon)} \) size \( \text{MAJ} \circ \text{AND}_2 \)
sub-circuit, with input gates \( G_1, G_2, \ldots, G_d \).

Moreover, since each addition process only corresponds to one carry sequence, by enumerate all possible carry sequence, we can see the above transform \( G_{\text{top}} \) into a \( \text{DOR} \circ \text{MAJ} \circ \text{AND}_2 \) sub-circuit with input gates \( G_1, G_2, \ldots, G_d \), with top fan-in:
\[
d^{D-1} = d^{O(\varepsilon \cdot n / \log d)} = 2^{O(\varepsilon \cdot n)}
\]
which completes the proof. \( \square \)

Finally, Structure Lemma II for \( \text{THR} \circ \text{THR} \) circuits follows directly from Lemma 3.2 and Lemma 3.4

**Reminder of Lemma 1.7** Let \( n \) be number of inputs and \( s = s(n) \) be a size parameter. Let \( \varepsilon \in \left( \frac{\log s}{n}, 1 \right) \),
for \( s = 2^{o(n)} \), every \( s \)-size \( \text{THR} \circ \text{THR} \) circuit \( C \) is equivalent to a \( \text{DOR} \circ \text{MAJ} \circ \text{MAJ} \) circuit such that:

- The top \( \text{DOR} \) gate has \( 2^{O(\varepsilon n)} \) fan-in.
- Each sub \( \text{MAJ} \circ \text{MAJ} \) circuit has size \( s^{O(1/\varepsilon)} \).

Moreover, the reduction can be computed in randomized \( 2^{O(\varepsilon n)} \cdot s^{O(1/\varepsilon)} \) time.

**Proof.** By Proposition 2.1 (3), \( C \) is equivalent to a \( \text{poly}(s) \) size \( \text{THR} \circ \text{ETHR} \) circuit \( C_1 \).

Then we apply Lemma 3.2 to reduce \( C_1 \) into a \( \text{DOR}_{\text{poly}(s)} \circ \text{ETHR} \circ \text{ETHR} \) circuit \( C_2 \), whose second-layer \( \text{ETHR} \) gates have positive weights and thresholds smaller than \( \text{poly}(s) \cdot 2^n < 2^{2n} \).

Next we apply Lemma 3.4 to change all second layer \( \text{ETHR} \) gates in \( C_2 \) into a \( \text{DOR} \circ \text{MAJ} \circ \text{AND}_2 \) sub-circuits, with top gate fan-in \( 2^{O(\varepsilon \cdot n)} \). Putting everything together, and note that \( \text{AND}_2 \circ \text{ETHR} \) can still be represented by an \( \text{ETHR} \) gate, we obtain a \( \text{DOR}_{2^{O(\varepsilon \cdot n)}} \circ \text{MAJ} \circ \text{ETHR} \) circuit, in which all \( \text{MAJ} \circ \text{ETHR} \) sub-circuits have size at most \( s^{O(1/\varepsilon)} \).

Applying Proposition 2.1 (5) completes our proof. And the running time bound follows from the corresponding time bounds in Lemma 3.2 and Lemma 3.4. \( \square \)
The following corollary follows directly by setting the parameter $\varepsilon$ carefully in Lemma 1.7.

**Corollary 3.5.** Let $n$ be number of inputs and $s = s(n)$ be a size parameter. Let $\varepsilon \in \left( \frac{\log s}{n}, 1 \right)$, for $s = 2^{o(n)}$, an $s$-size $THR \circ THR$ circuit $C$ is equivalent to a $DOR \circ MAJ \circ MAJ$ circuit such that:

- The top $DOR$ gate has $s^{O(1/\varepsilon)}$ fan-in.
- Each sub $MAJ \circ MAJ$ circuit has size $2^{O(\varepsilon \cdot n)}$.

Moreover, the reduction can be computed in randomized $2^{O(\varepsilon n)} \cdot s^{O(1/\varepsilon)}$ time.

### 3.3 Some Applications

Finally, we prove these interesting implications of Lemma 1.6 and Lemma 1.7.

The following corollary follows from Lemma 1.6 directly.

**Reminder of Corollary 1.8** The following are equivalent:

- The satisfiability of $THR \circ THR$ circuits of size $n^k$ can be solved in $2^n/n^k$ time for any $k$.
- The satisfiability of $THR \circ MAJ$ circuits of size $n^k$ can be solved in $2^n/n^k$ time for any $k$.

**Proof.** We only need to prove the second item implies the first. Suppose the second item holds, given a $THR \circ THR$ circuit of size $n^k$, by Lemma 1.6, it can be reduced to an equivalent $Gap-OR \circ THR \circ MAJ$ circuit of size $n^{kc}$ for a constant $c$, whose satisfiability can be solved in $2^n/n^{kc}$ time by the first item.

And the following two corollaries follow from Lemma 1.7 directly.

**Reminder of Corollary 1.10** Let $n$ be number of inputs and $s = s(n)$ be a size parameter. Let $\varepsilon \in \left( \frac{\log s}{n}, 1 \right)$ and $d$ be a constant. For $s = 2^{o(n)}$, every $s$-size $LT_d$ circuit is equivalent to a $DOR \circ \hat{LT}_d$ circuit such that:

- The top $DOR$ gate has $2^{O(\varepsilon \cdot n)}$ fan-in.
- Each sub $\hat{LT}_d$ circuit has size $O \left( s^{O(1/\varepsilon)} \right)$.

**Proof.** We apply Lemma 1.7 to the top 2 layers, and then apply Proposition 2.1(5) recursively to obtain an equivalent $DOR \circ \hat{LT}_d$ circuit.

**Corollary 3.6.** For all $d \geq 2$, the following are equivalent:

- There is a $2^{(1-\Omega(1))n}$ time algorithm for satisfiability of polynomial size $LT_d$ circuits.
- There is a $2^{(1-\Omega(1))n}$ time algorithm for satisfiability of polynomial size $\hat{LT}_d$ circuits.
Proof. Suppose we have a $2^{(1-\varepsilon_1)n}$ time algorithm for satisfiability of polynomial size $\widehat{\mathbf{L}}_d$ circuits for a constant $\varepsilon_1 > 0$. Let $c$ be the hidden constant in the big-$O$ notation of the fan-in of the top DOR gate in Lemma 1.7.

We set $\varepsilon = \varepsilon_1/2c$ and apply Lemma 1.7 to the given $\mathbf{L}_d$ circuit. We obtain an equivalent $\mathbf{DOR} \circ \widehat{\mathbf{L}}_d$ circuit with top fan-in $2^c n = 2^{c_1/2-n}$ and polynomial size $\widehat{\mathbf{L}}_d$ sub-circuits. Then we can apply our algorithm for solving polynomial size $\widehat{\mathbf{L}}_d$ to solve the satisfiability of the given $\mathbf{L}_d$ circuit in $2^{(1-\varepsilon_1/2-n)$ time, which completes the proof.

Note that Corollary 1.9 is simply a special case of the above Corollary when $d = 2$.

Similarly, the same techniques can be used to derive a structure lemma for $\mathbf{THR} \circ \mathbf{AND}_k$ circuits as well.

Reminder of Corollary 1.11. Let $n$ be number of inputs and $s = s(n)$ be a size parameter. Let $\varepsilon \in \left(\frac{\log s}{n}, 1\right)$ and $k$ be a constant. Assuming $s = 2^{o(n)}$, an $s$-size $\mathbf{THR} \circ \mathbf{AND}_k$ circuit is equivalent to a $\mathbf{DOR} \circ \mathbf{MAJ} \circ \mathbf{AND}_{2k}$ circuit such that:

- The top $\mathbf{DOR}$ gate has $2^{O((s/n)}$ fan-in.
- Each sub $\mathbf{MAJ} \circ \mathbf{AND}_{2k}$ circuit has size $O\left(s^{O(1/\varepsilon)}\right)$.

The above still holds if we replaced both $\mathbf{AND}_k$ and $\mathbf{AND}_{2k}$ by unbounded fan-in AND gates.

Proof. We simply apply Lemma 3.2 and Lemma 3.4 and merge each $\mathbf{AND}_2 \circ \mathbf{AND}_k$ sub-circuits into a single $\mathbf{AND}_{2k}$ gate.

Together with Lemma 2.3 the following corollary is evident.

Reminder of Corollary 1.12. For any integer $k$, if there is a $2^{(1-\Omega(1))n}$ time algorithm for polynomial size unweighted $\mathbf{MAX}$-$2k$-$\mathbf{SAT}$, then so does polynomial size weighted $\mathbf{MAX}$-$k$-$\mathbf{SAT}$.

Proof. We can use Lemma 2.3 to transform the bottom AND gates to OR gates for $\mathbf{THR} \circ \mathbf{AND}$ and $\mathbf{MAJ} \circ \mathbf{AND}$ circuits, and then the proof are exactly the same as in Corollary 3.6.

4 Shaving Logs from $\ell_2$-Furthest Pair Implies $\mathbf{THR} \circ \mathbf{THR}$ Lower Bound

In this section we show shaving logs on $\ell_2$-Furthest Pair or other related problems would have exciting circuit lower bound consequence.

We first show that slightly faster satisfiability algorithm for $\mathbf{THR} \circ \mathbf{THR}$ implies circuit lower bound against $\mathbf{THR} \circ \mathbf{THR}$. Note that this is not obvious as $\mathbf{THR} \circ \mathbf{THR}$ circuits are not trivially closed under intersection, while we have to solve satisfiability for an AND of 3 $\mathbf{THR} \circ \mathbf{THR}$ circuits faster.

Lemma 4.1. If there is an algorithm solving the satisfiability of $\mathbf{THR} \circ \mathbf{THR}$ circuits of size $n^k$ in $2^n/n^k$ time for any $k$, then $\mathbf{NEXP}$ has no polynomial size $\mathbf{THR} \circ \mathbf{THR}$ circuits.

Proof. From Theorem 2.5 we have to devise a $2^n/\log^{\omega(1)}(n)$ time algorithm for solving $\mathbf{AND}_3 \circ \mathbf{THR} \circ \mathbf{THR}$ circuits of size $s = n^k$ with $n' = n + O(\log n)$ inputs.

Given such a circuit $C$, we first apply Proposition 2.1(3) to transform it into a poly$(s)$ size $\mathbf{AND}_3 \circ \mathbf{DOR} \circ \mathbf{ETHR} \circ \mathbf{ETHR}$ circuit $C'$.

Note that we can switch the order of DOR and $\mathbf{AND}_3$, by treating the first as addition and the second as multiplication. Then $C'$ is equivalent to another $\mathbf{DOR} \circ \mathbf{ETHR} \circ \mathbf{ETHR} \circ \mathbf{ETHR}$ circuit $C''$ of poly$(s)$ size.
Finally, solving $C''$ can be completed by solving $\text{poly}(s) \circ \text{ETHR} \circ \text{ETHR}$ sub-circuits, and note that $\text{ETHR} \circ \text{ETHR} \subseteq \text{THR} \circ \text{THR}$ (Proposition 2.1(7)), hence using the algorithm from the assumption completes the proof.

\textbf{Remark 4.2.} By Remark 2.7 the consequence also holds if the algorithm in Lemma 4.1 is co-nondeterministic.

\textbf{Lemma 4.3.} If there is an algorithm solving $\text{Weighted-Max-IP}_{n,\log^k n}$ or $\text{Z-OV}_{n,\log^k n}$ in $n^2/\log^k(n)$ time for any integer $k$, then $\text{NEXP}$ has no polynomial size $\text{THR} \circ \text{THR}$ circuits.

\textbf{Proof.} We consider $\text{Weighted-Max-IP}$ first. Suppose there is such an algorithm for $\text{Weighted-Max-IP}$. By Corollary 1.8 and Lemma 4.1 we only need to devise an algorithm for the satisfiability of $\text{THR} \circ \text{MAJ}$ circuits of size $n^k$ in $2^n/n^k$ time for all $k$. We do so by reducing the satisfiability problem for $\text{THR} \circ \text{MAJ}$ circuits to $\text{Weighted-Max-IP} \circ \text{Z-OV}$.

For simplicity, we assume $n$ is even. Let $C$ be a $\text{THR} \circ \text{MAJ}$ circuit of size $s = n^k$ and $G$ be its top $\text{THR}$ gate. Let $W_1,W_2,\ldots,W_s,T$ be the weights, threshold and associate linear function of $G$. Let $G_1,G_2,\ldots,G_s$ be the corresponding $\text{MAJ}$ gates on the bottom layers. We use $L_1,L_2,\ldots,L_s$ and $T_1,T_2,\ldots,T_s$ to denote their associated linear functions and thresholds.

For each $x,y \in \{0,1\}^{n/2}$, we interpret $x$ and $y$ as an assignment to the first half and second half of the input to $C$ respectively.

For each linear function $L_j$, we use $X_j(x)$ and $Y_j(y)$ to denote the contribution from $x$ and $y$ respectively. We have

$$G_j(x,y) := [X_j(x) + Y_j(y) \geq T_j].$$

Note that since each $G_j$ has at most $s$ wires, and therefore $0 \leq X_j(x), Y_j(y) \leq s$. So we now define $u_j(x),v_j(y) \in \{0,1\}^{s+1}$, such that $(u_j(x))_i = 1 \text{ iff } i = X_j(x)$ and $(v_j(y))_i = 1 \text{ iff } i + Y_j(y) \geq T_j$. Then we have $G_j(x,y) = u_j(x) \cdot v_j(y)$. Now we set

$$u(x) := \circ_{j=1}^s u_j(x) \quad v(y) := \circ_{j=1}^s v_j(x) \quad w := \circ_{j=1}^s W_j \otimes (s+1).$$

It is easy to see that $u(x) \otimes_w v(y) = L(x,y)$. Therefore, computing the maximum of $u(x) \otimes_w v(y)$ for all $x,y \in \{0,1\}^{n/2}$ solves the problem, which can be reduced to a $\text{Weighted-Max-IP}_{2^{n/2},\text{poly}(n)}$ instance. The proof is completed by applying the algorithm for $\text{Weighted-Max-IP}$ in the assumption.

The reduction to $\text{Z-OV}$ works roughly the same, with the only modification that we transform the $\text{THR} \circ \text{MAJ}$ circuit into an equivalent $\text{DOR} \circ \text{ETHR} \circ \text{MAJ}$ at the beginning (via Proposition 2.1(3)), and solve each $\text{ETHR} \circ \text{MAJ}$ sub-circuit separately via a similar reduction to $\text{Z-OV}$.

Now we are ready to prove Theorem 1.1

\textbf{Reminder of Theorem 1.1} If any of the following problems has an $n^2 \text{poly}(d)/\log^2(n)$ time deterministic algorithm for polylogarithmic $d$, then $\text{NEXP}$ has no polynomial size $\text{THR} \circ \text{THR}$ circuits:

1. $\text{Z-OV}_{n,d}$ (Hopcroft’s Problem): Find an orthogonal pair among $n$ points in $\mathbb{Z}^d$.
2. $\ell_2$-Furthest-Pair$_{n,d}$: Find the $\ell_2$-furthest pair among $n$ points in $\mathbb{R}^d$.
3. Bichrom.-$\ell_2$-Closest-Pair$_{n,d}$: Given two set $A,B$ of $n$ points in $\mathbb{R}^d$, compute $\min_{(a,b) \in A \times B} \|a-b\|_2$.
4. $\text{Z-Max-IP}_{n,d}$: Given two sets $A,B$ of $n$ vectors from $\mathbb{Z}^d$, compute $\max_{(a,b) \in A \times B} a \cdot b$. 

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5. **Weighted-Max-IP** \(\ell_2\)-vector: Given a weight vector \(w \in \mathbb{Z}^d\) and two sets \(A, B\) of \(n\) vectors from \(\{0, 1\}^d\),

\[
\text{compute} \quad \max_{(a, b) \in A \times B} \sum_{i=1} w_i \cdot a_i \cdot b_i.
\]

**Proof.** The cases of Weighted-Max-IP \(\ell_2\)-vector and Z-OV \(\ell_2\)-vector follow directly from Lemma 4.3.

And the cases for other problems follow from the fact there are efficient reductions from Z-OV \(\ell_2\)-vector to all of them [Wil18b] (see also Theorem 4.3, Lemma 4.5 and Lemma 4.6 of [Che18] for explicit reductions). \(\square\)

5 **Shaving Logs from Approximate Bichrom.-\(\ell_2\)-Closest-Pair Implies SYM \(\lor\) THR Lower Bound**

In this section we establish circuit lower bound consequences from shaving logs on Approximate Bichrom.-\(\ell_2\)-Closest-Pair or other related problems.

We first consider Lemma 5.1, whose proof is deferred to the end of this section.

**Lemma 5.1.** Given a size \(s\) AND_3 \(\circ\) SYM \(\circ\) SYM circuit \(C\), there is a \(2n^{5/2} \cdot \text{poly}(s)\) time algorithm reducing it into \(s^3\) Max-IP \(2n^{5/2} \cdot O(s^2n^2)\) instances.

To prove Theorem 1.2, we first show the following reductions from Max-IP.

**Lemma 5.2.** Let \(n, d\) be two integers and \(\varepsilon = 1/10d\), a Max-IP \(n, d\) instances can be reduced to:

- \((1 + \varepsilon)\)-approximation to Bichrom.-\(\ell_1\)-Closest-Pair \(n\).
- \((1 + \varepsilon)\)-approximation to Bichrom.-\(\ell_2\)-Closest-Pair \(n\).

**Proof.** Given a Max-IP \(n, d\) instance with two sets \(A, B \subseteq \{0, 1\}^d\). We first consider Item (2). For each \(x \in A\) and \(y \in B\), we create two points \(p_x\) and \(q_y\) in \(\mathbb{R}^{d+2}\), such that

\[
p_x = \left(x, \sqrt{d - \|x\|^2_2}, 0\right), \quad q_y = \left(y, 0, \sqrt{d - \|y\|^2_2}\right).
\]

We have

\[
\|p_x - q_y\|_2^2 = \|p_x\|^2_2 + \|q_y\|^2_2 - 2 \cdot (p_x \cdot p_y) = 2 \cdot (d - x \cdot y).
\]

Note that a \((1 + \varepsilon)\)-approximation to \(\min_{(x, y) \in A \times B} \|p_x - q_y\|_2\) imply a \((1 + \varepsilon)\)-approximation to \(\min_{(x, y) \in A \times B} \|p_x - q_y\|_2 = \min_{(x, y) \in A \times B} 2 \cdot (d - x \cdot y)\). Note that \(\varepsilon = 1/10d\), we can determine \(\max_{(x, y) \in A \times B} x \cdot y\) from the above approximation immediately, which completes the reduction to Item (2).

For Item (1), we begin by setting up some notations. For \(t \in [d]\), we use \(e^{[t]}\) to denote the Boolean vector with first \(t\) coordinates being 1, and the rest being 0. Recall that for two vectors \(a, b\), we use \(a \circ b\) to denote their concatenation.

For each \(x \in A\) and \(y \in B\), we create two points \(p_x, q_y \in \{0, 1\}^{3d}\), such that

\[
p_x = x \circ e^{[d - \|x\|_1]} \circ e^{[0]}, \quad q_y = y \circ e^{[0]} \circ e^{[d - \|y\|_1]}.
\]

Note that for each \(p_x\) and \(q_y\), there are exactly \(d\) coordinates with value 1. Also, note that their inner product \(p_x \cdot q_y\) corresponds to the number of coordinates on which they are both 1. We have

\[
\|p_x - q_y\|_1 = 2 \cdot (d - p_x \cdot p_y).
\]

Therefore, a \((1 + \varepsilon)\)-approximation to \(\min_{(a, b) \in A \times B} \|p_x - q_y\|_1 = \min_{(a, b) \in A \times B} 2 \cdot (d - p_x \cdot p_y)\) would be enough to solve the given Max-IP instance, which complete the proof for Item (1). \(\square\)
Now we are ready to prove Theorem 1.2 (restated below).

Reminder of Theorem 1.2. If any of following problems has an \( n^2 \) poly(d)/log\(^{\omega(1)}\) \( n \) time deterministic algorithm for polylogarithmic \( d \), then \( \text{NEXP} \) has no polynomial size \( \text{SYM} \circ \text{THR} \) circuits:

1. \( \text{Max-IP}_{n,d} \): Given two sets \( A, B \) of \( n \) vectors from \( \{0,1\}^d \), compute \( \max_{(a,b) \in A \times B} a \cdot b \).

2. Compute a \( (1 + 1/\log^{\omega(1)} n) \)-approximation to \( \text{Bichrom}.-\ell_2\text{-Closest-Pair}_n \).

3. Compute a \( (1 + 1/\log^{\omega(1)} n) \)-approximation to \( \text{Bichrom}.-\ell_1\text{-Closest-Pair}_n \).

Proof. By Lemma 5.2, we only need to consider Item (1) here. Note that by Proposition 2.1 (4), we just need to consider polynomial size \( \text{SYM} \circ \text{SYM} \) circuit.

By Theorem 2.5, we need to show the satisfiability problem for polynomial size \( \text{AND}_3 \circ \text{SYM} \circ \text{SYM} \) circuits with \( n + O(\log n) \) inputs can be solved in \( 2^n / n^{\omega(1)} \) time. With Lemma 5.1 it can be reduced to polynomial many \( \text{Max}_{2n/2+O(\log n),\text{poly}(n)} \) instance, apply our algorithm from Item (1), the needed \( 2^n / n^{\omega(1)} \) time algorithm follows directly.

Finally, we prove Theorem 1.3, which gives more refined circuit lower bounds consequences.

Reminder of Theorem 1.3. Suppose for some a real \( k > 2 \), one of the following algorithms exists:

1. An \( n^2 / \log^{\omega(1)} n \) time algorithm for \( \text{Max-IP}_{n,\text{log}^k n} \).

2. A \( (1 + 1/\log^k n) \)-approximation algorithm for \( \text{Bichrom}.-\ell_1\text{-Closest-Pair}_n \) in \( n^2 / \log^{\omega(1)} n \) time.

3. A \( (1 + 1/\log^k n) \)-approximation algorithm for \( \text{Bichrom}.-\ell_2\text{-Closest-Pair}_n \) in \( n^2 / \log^{\omega(1)} n \) time.

Then \( \text{E}^{\text{NP}} \) has no \( n^{(k-2)/2-\epsilon_1} \) size \( \text{SYM} \circ \text{SYM} \) circuit for any \( \epsilon_1 > 0 \).

Proof. Let \( \epsilon_1 > 0 \), by Theorem 2.4 it suffices to show that the satisfiability of \( s = n^{(k-2)/2-\epsilon_1} \) size \( \text{AND}_3 \circ \text{SYM} \circ \text{SYM} \) circuits with \( n' = n + O(\log n) \) inputs can be solved in \( 2^n / n^{\omega(1)} \) time.

We consider Item (1) first. By Lemma 5.1, in \( 2^{n'/2} \text{poly}(s) = 2^{n/2} \text{poly}(s,n) \) time, the aforementioned problem can be reduced to \( s^3 \) instances of \( \text{Max}_{2n/2+O(s^2n^2),\text{poly}(n)} \). Note that \( s^2n^2 \leq n^{k-\epsilon_1} \).

Therefore, applying the algorithm for \( \text{Max-IP}_{n,\text{log} n} \), these \( s^3 \) instances of \( \text{Max}_{2n/2,\text{log}^k n} \) can be solved in

\[
s^3 \cdot \left( 2^{n/2} \cdot \text{poly}(n) \right)^2 / n^{\omega(1)} = 2^n / n^{\omega(1)}
\]

time, which completes the proof for Item (1). Applying Lemma 5.2 and proceed similarly, the claim for the other two cases can also be established.
5.1 Proof of Lemma 5.1

To prove Lemma 5.1 we introduce two simple lemmas first.

Lemma 5.3. There are two functions $\psi_{rev}^x, \psi_{rev}^y : \{0, 1\}^* \to \{0, 1\}^*$ such that for all integer $d$ and $x, y \in \{0, 1\}^d$, we have $\psi_{rev}^x(x), \psi_{rev}^y(y) \in \{0, 1\}^{2d}$ and $\psi_{rev}^x(x) \cdot \psi_{rev}^y(y) = d - x \cdot y$.

Proof. We define two functions $\varphi_x, \varphi_y : \{0, 1\} \to \{0, 1\}^2$ such that:

$$\varphi_x(0) := (1, 0), \quad \varphi_x(1) := (0, 1), \quad \varphi_y(0) := (1, 1), \quad \varphi_y(1) := (1, 0).$$

It is easy to check that for $a, b \in \{0, 1\}$, $a \cdot b = 1 - \varphi_x(a) \cdot \varphi_y(b)$. Then, for $x, y \in \{0, 1\}^d$, we define $\varphi_x(x) \in \{0, 1\}^{2d}$ as the concatenation of $\varphi_x(x_i)$ for each $i \in [d]$, and similarly define $\varphi_y(y) \in \{0, 1\}^{2d}$ as the concatenation of $\varphi_y(y_i)$ for each $i \in [d]$.

Then we can see $\psi_{rev}^x(x) \cdot \psi_{rev}^y(y) = \sum_{i=1}^d \varphi_x(x_i) \cdot \varphi_y(y_i) = d - x \cdot y$. $\square$

Lemma 5.4. For all integers $d$ and $0 \leq m \leq d$, there are two mappings $\varphi_{d,m}^x, \varphi_{d,m}^y : \{0, 1\}^d \to \{0, 1\}^{O(d^2)}$ and an integer $M_{d,m}$, such that for all $x, y \in \{0, 1\}^d$:

- If $x \cdot y = m$, then $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) = M_{d,m}$.
- Otherwise, $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) > M_{d,m}$.

Proof. We remark the reduction here is essentially the same as the trick used in [Wil18b]. For a vector $v \in \{0, 1\}^k$, we use $v \otimes k$ to denote the concatenation of $k$ copies of $v$.

Consider the following polynomial $P(x, y) := (x \cdot y - m)^2$, we have

$$P(x, y) = (x \cdot y)^2 - 2m(x \cdot y) + m^2 = (x \cdot y)^2 + 2m(d - x \cdot y) + m^2 - 2dm.$$  

For $x, y \in \{0, 1\}^d$, we construct $\bar{x}, \bar{y} \in \{0, 1\}^d$ such that $\bar{x}_i = x_{(i-1)/d} + 1$ and $\bar{y}_i = -y(i \mod d) + 1$. Then we can see $\bar{x} \cdot \bar{y} = \sum_{i=1}^d \sum_{j=1}^d x_i \cdot y_j = (x \cdot y)^2$. Let $\psi_{rev}^x$ and $\psi_{rev}^y$ be the two functions from Lemma 5.3.

For $x, y \in \{0, 1\}^d$, we define

$$\varphi_{d,m}^x(x) := (\bar{x}, \psi_{rev}^x(x) \otimes (2m)) \quad \text{and} \quad \varphi_{d,m}^y(y) := (\bar{y}, \psi_{rev}^y(y) \otimes (2m)).$$

Then we have $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) = (x \cdot y)^2 + 2m(d - x \cdot y) = P(x, y) + 2dm - m^2$. And we set $M_{d,m} = 2dm - m^2$.

Now, if $x \cdot y = m$, we have $P(x, y) = 0$, and therefore $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) = M_{d,m}$. Otherwise, $x \cdot y \neq m$ and we have $P(x, y) > 0$, and hence $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) > M_{d,m}$.

Finally, note that $\varphi_{d,m}^x(x), \varphi_{d,m}^y(y) \in \{0, 1\}^{d^2 + 2dm}$, which completes the proof. $\square$

The following corollary follows directly from composing the reductions in Lemma 5.4 and Lemma 5.3.

Corollary 5.5. For all integers $d$ and $0 \leq m \leq d$, there are two mappings $\varphi_{d,m}^x, \varphi_{d,m}^y : \{0, 1\}^d \to \{0, 1\}^{O(d^2)}$ and an integer $M_{d,m}$, such that for all $x, y \in \{0, 1\}^d$:

- If $x \cdot y = m$, then $\varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) = M_{d,m}$.  

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• Otherwise, \( \varphi_{d,m}^x(x) \cdot \varphi_{d,m}^y(y) < M_{d,m} \).

Now we are ready to prove Lemma 5.1 (restated below).

**Reminder of Lemma 5.1.** Given an \( \text{AND}_3 \circ \text{SYM}_s \circ \text{SYM} \) circuit \( C \), there is a \( 2^{n/2} \ poly(s) \) time algorithm reducing it into \( s^3 \text{Max-IP}_{n,O(s^2n^2)} \) instances.

**Proof.** For simplicity, we assume \( n \) is even throughout the proof. By Proposition 2.1 (1), we can transform \( C \) into an \( \text{AND}_3 \circ \text{DOR}_s \circ \text{EMAJ}_s \circ \text{SYM} \) circuit \( C' \), which can be in turn transformed into a \( \text{DOR}_s \circ \text{AND}_3 \circ \text{EMAJ}_s \circ \text{SYM} \) circuit \( C'' \).

Then, for each \( \text{AND}_3 \circ \text{EMAJ}_s \circ \text{SYM} \) sub-circuit \( D \) of \( C'' \), we reduce it into a \( \text{Max-IP}_{n,O(s^2n^2)} \) instance. For \( j \in [3] \), let \( D_j \) be the \( j \)-th \( \text{EMAJ}_s \circ \text{SYM} \) sub-circuit of \( D \), and let \( G_1, G_2, \ldots, G_s \) be all the \( s \) SYM gates in \( D_j \), and let \( f_1, f_2, \ldots, f_s \) be their corresponding functions. Let \( T_j \) be the threshold of the top EMAJ gate of \( D_j \).

For each \( x, y \in \{0, 1\}^{n/2} \), we interpret \( x \) and \( y \) as an assignment to the first half and second half of the input to \( D \) respectively. We use \( X_i(x) \) and \( Y_i(y) \) to denote the contribution of \( x \) and \( y \) to gate \( G_i \) respectively. Then we have

\[
G_i(x, y) = f_i(X_i(x) + Y_i(y)).
\]

Now, for an integer \( t \in \{0, 1, \ldots, n\} \) and a function \( f : \{0, 1, \ldots, n\} \to \{0, 1\} \), we define two mappings

\[
\psi^f_x(t), \psi^f_y(t) \in \{0, 1\}^n,
\]

such that

\[
\psi^f_x(t)_i = \begin{cases} 1 & \text{if } i = t \\ 0 & \text{otherwise} \end{cases} \quad \text{and} \quad \psi^f_y(t)_i = \begin{cases} 1 & \text{if } f(i + t) = 1 \\ 0 & \text{otherwise}. \end{cases}
\]

Then we can see for two integers \( a, b \in \{0, 1, \ldots, n\} \), \( \psi^f_x(a) \cdot \psi^f_y(b) = f(a + b) \).

Now, for each \( x, y \in \{0, 1\}^{n/2} \), we define

\[
\psi^3_x(x) := \psi^1_{s-1} \psi^3_x(X_i(x)) \quad \text{and} \quad \psi^3_y(y) := \psi^1_{s-1} \psi^3_y(Y_i(y)).
\]

Therefore, we have

\[
\psi^3_x(x) \cdot \psi^3_y(y) = \sum_{i=1}^{s} \psi^f_x(X_i(x)) \cdot \psi^f_y(Y_i(y)) = \sum_{i=1}^{s} G_i(x, y),
\]

and consequently

\[
D_j(x, y) = [\psi^3_x(x) \cdot \psi^3_y(y) = T_j].
\]

Note that \( \psi^3_x(x), \psi^3_y(y) \in \{0, 1\}^{sn} \). In order to compute the AND of \( D_1, D_2 \) and \( D_3 \), we make use of Corollary 5.5 consider

\[
\psi_x(x) := \psi^3_{s-1} \left( \varphi_{sn,T_j}(\psi^3_x(x)) \right) \quad \text{and} \quad \psi_y(y) := \psi^3_{s-1} \left( \varphi_{sn,T_j}(\psi^3_y(y)) \right).
\]

Let \( M = \sum_{j=1}^{3} M_{sn,T_j} \). From Corollary 5.5, we note that \( \psi_x(x) \cdot \psi_y(y) = M \) if \( D_1(x, y) \land D_2(x, y) \land D_3(x, y), \psi_x(x) \cdot \psi_y(y) < M \) otherwise. Therefore, let \( A \) be the set of all \( \psi_x(x) \)’s for \( x \in \{0, 1\}^{n/2} \), and \( B \) be the set of all \( \psi_y(y) \)’s for \( y \in \{0, 1\}^{n/2} \). We can see \( A, B \) form a \( \text{Max-IP}_{n,O(s^2n^2)} \) instance and \( \text{Max}(A, B) = M \) if and only if \( D \) is satisfiable.

Therefore, by reducing all \( O(s^3) \) \( \text{AND}_3 \circ \text{EMAJ}_s \circ \text{SYM} \) sub-circuits of \( C'' \) into \( \text{Max-IP}_{n,O(s^2n^2)} \) instances, we solve the satisfiability problem for the equivalent \( \text{AND}_3 \circ \text{SYM}_s \circ \text{SYM} \) circuit \( C \). This completes the proof. \( \square \)
6 Shaving Logs from Modest Dimension Max-IP Implies THR \circ THR Lower Bound

In this section we prove Theorem 1.2 (restated below).

Reminder of Theorem 1.5 If any of the following deterministic algorithms exists, then NEXP has no polynomial-size THR \circ THR circuits:

1. An algorithm solving Max-IP_{n,n} in \( n^2 / \log^{\omega(1)}(n) \) time, for a constant \( \varepsilon > 0 \).
2. An algorithm solving Max-IP_{n,\log^k(n)} in \( n^{2-\varepsilon} \) time for a constant \( \varepsilon > 0 \) and any integer \( k \).

Proof. We first consider Item (2). We want to apply Lemma 1.7 to simplify the given THR \circ THR circuit. However, the problem here is that Lemma 1.7 only implies a randomized reduction, preventing us from applying Lemma 4.1 as that needs a deterministic algorithm.

Fortunately, by Remark 4.2 we only need to come up with a co-nondeterministic algorithm. That is, we want a nondeterministic algorithm which decides whether a THR \circ THR circuit of size \( n^k \) is unsatisfiable in \( 2^n/n^k \) time for every integer \( k \).

In the following we derandomize the construction in Lemma 1.7 using nondeterminism. Given a THR \circ THR circuit \( C \) of size \( s = n^k \), we also construct its negation \( D = \neg C \), with the same size \( s \).

Let \( \varepsilon_1 > 0 \) be a constant to be specified later. We apply the reduction of Lemma 1.7 to both \( C \) and \( D \), and guess all random primes needed nondeterministically along the way, which takes

\[ 2^{O(\varepsilon_1 n)} \cdot s^{O(1/\varepsilon_1)} \]

nondeterministic time.

After that, we get two DOR \circ MAJ \circ MAJ circuits \( C' \) and \( D' \), whose top DOR gates have fan-in \( 2^{O(\varepsilon_1 n)} \cdot \text{poly}(s) = 2^{O(\varepsilon_1 n)} \), and each sub MAJ \circ MAJ circuit has size \( s^{O(1/\varepsilon_1)} \). We have to verify that \( C \) and \( D \) are indeed equivalent to \( C' \) and \( D' \). We claim that holds if and only if \( C' \land D' \) are unsatisfiable.

One direction is straightforward. If they are equivalent correspondingly, then \( D' \) is the negation of \( C' \) too, and \( C' \land D' \) are unsatisfiable.

For the other direction, note that the reduction of Lemma 1.7 only introduces one-sided error (Remark 3.3). That is, for all possible guess and \( x \in \{0,1\}^n \), when \( C(x) = 1 \), we must have \( C'(x) = 1 \). And the same holds for \( D(x) \) and \( D'(x) \). Therefore, suppose \( C \) is not equivalent to \( C' \) (the case for \( D \) and \( D' \) is similar), it must be the case that there is an \( x \) such that \( C(x) = 0 \) while \( C'(x) = 1 \). Since \( C(x) = 0 \), we have \( D(x) = 1 \) and therefore \( D'(x) = 1 \), which means \( (C' \land D')(x) = 1 \), completes the proof of the claim.

Note that \( C' \land D' \) is an AND_2 \circ DOR \circ MAJ \circ MAJ circuit. We can switch the order of AND_2 and DOR by treating them as multiplication and addition respectively, and obtain an equivalent DOR \circ AND_2 \circ MAJ \circ MAJ circuit, with top-fan in \( 2^{O(\varepsilon_1 n)} \) and sizes of its MAJ \circ MAJ sub-circuits unchanged.

Applying Lemma 5.1 the satisfiability of an AND_2 \circ MAJ \circ MAJ circuit can be reduced to \( \text{poly}(s^{O(1/\varepsilon_1)}) = n^{O(k/\varepsilon_1)} \text{Max-IP}_{2n/2, n\cdot O(k/\varepsilon_1)} \) instances. Therefore, by choosing \( \varepsilon_1 \) small enough comparing to \( \varepsilon \), we can obtain a \( 2^{(1-\varepsilon/2)n} \) time algorithm for the satisfiability of \( C' \land D' \) from the algorithm in Item (2).

Finally, we reject immediately if we find \( C' \land D' \) is satisfiable. Otherwise, we know \( C' \) is equivalent to \( C \), using the same argument we can obtain a \( 2^{(1-\varepsilon/2)n} \) time algorithm for the satisfiability of \( C' \). We accept only if \( C' \) is unsatisfiable.

It is not hard to see the above algorithm solves the unsatisfiability problem of THR \circ THR circuits of size \( n^k \) in \( 2^{(1-\varepsilon/2)n}, \) nondeterministic time for any integer \( k \), which completes the proof.

The case for Item (1) are roughly the same, except for that we apply Corollary 5.5 instead. \( \square \)
7 MAX-SAT

In this section we show that slightly better exact algorithms for MAX-SAT would have interesting circuit lower bound consequences.

To prove Theorem 1.15 and Theorem 1.17 we first establish a simple reduction from a SYM \( \circ \) AND circuit to an equivalent OR \( \circ \) MAJ \( \circ \) OR circuit.

Lemma 7.1. A size \( s \) SYM \( \circ \) AND circuit is equivalent to a poly\((s)\) size OR \( \circ \) MAJ \( \circ \) OR circuit. Moreover, the latter circuit can be constructed in poly\((s)\) time.

Proof. Let \( C' \) be the given SYM \( \circ \) AND circuit of size \( s \). We can first transform \( s \) to an equivalent poly\((s)\) size OR \( \circ \) EMAJ \( \circ \) AND circuit \( C \) with top fan-in \( s \), since SYM \( s \) \( \subseteq \) OR \( s \) \( \circ \) EMAJ \( s \) (Proposition 2.1 (1)).

Now, let \( C_1, C_2, \ldots, C_s \) be all the EMAJ \( \circ \) AND sub-circuits of \( C \). Since EMAJ \( s \) \( \subseteq \) MAJ\( O(s^2) \) \( \circ \) AND\( _2 \) (Proposition 2.1 (10)), each \( C_i \) is consequently equivalent to a poly\((s)\) size MAJ \( \circ \) AND circuit \( D_i \).

Let \( E_1, E_2, \ldots, E_t \) be all the AND gates in \( D_i \), by Lemma 2.3 supposing \( E_j \) acts on \( k \) variables, we can construct \( k \) OR gates \( O_1, O_2, \ldots, O_k \), such that

\[
\sum_{i=1}^{k} O_i(x) = (k - 1) + E_j(x).
\]

Therefore, \( D_i \) can be reduced to an equivalent MAJ \( \circ \) OR circuit, and the proof is completed. \( \square \)

Now we are ready to prove Theorem 1.15 and Theorem 1.17 (restated below).

Reminder of Theorem 1.15 If there is an algorithm for MAX-SAT solving an instance with \( 2^{\log^k n} \) clauses in \( 2^n/2^{\log^k n} \) time for every integer \( k \). Then NEXP has no quasi-polynomial size SYM \( \circ \) AND circuit.

Proof. By Theorem 2.6 it suffices to show that the satisfiability of \( 2^{\log^k n} \) size AND\( ^3 \circ \) SYM \( \circ \) AND circuits with \( n + O(\log n) \) inputs can be solved in \( 2^{n-\log^k n} \) time for any \( k \).

By Proposition 2.1 (9), a size \( s = 2^{\log^k n} \) size AND\( ^3 \circ \) SYM \( \circ \) AND circuit can be transformed into a poly\((s)\) size SYM \( \circ \) AND circuit, which in turn be transformed to a poly\((s) = 2^{O(\log^kn)}\) size OR \( \circ \) MAJ \( \circ \) OR circuit by Lemma 7.1. Note that by our hypothesis, we have an algorithm solving MAX-SAT with \( 2^{\log^{k'} n} \) clauses in \( 2^{n-\log^{k'} n} \) time for any \( k' \), and this algorithm can be used to solve the satisfiability for MAJ \( \circ \) OR sub-circuits.

Therefore, the satisfiability of a \( 2^{\log^k n} \) size AND\( ^3 \circ \) SYM \( \circ \) AND circuit can be solved in \( 2^{n + O(\log n)}/2^{\log^{k'} n} \).

\(2^{O(\log^kn)} \leq 2^{n-\log^{(k'-1)} n} \) time for large enough \( k' \). Then the proof is completed by applying Theorem 2.6 \( \square \)

Reminder of Theorem 1.17 If there is a \( 2^{n-O(n/\log m)} \) time algorithm for MAX-SAT with \( m \) clauses. Then \( E^{NP} \) does not have \( 2^{o(\sqrt{m})} \)-size SYM \( \circ \) AND circuits.

Proof. By Theorem 2.4 it suffices to show that the satisfiability of \( s = 2^{o(\sqrt{m})} \) size AND\( ^3 \circ \) SYM \( \circ \) AND circuits with \( n + O(\log n) \) inputs can be solved in \( 2^n/n^{o(1)} \) time.

Again, with the same step in the proof of Theorem 1.15 this size \( s \) AND\( ^3 \circ \) SYM \( \circ \) AND circuit can be transformed into an equivalent poly\((s) = 2^{o(\sqrt{m})}\) size OR \( \circ \) MAJ \( \circ \) OR circuit. With our MAX-SAT algorithm, the satisfiability of the latter circuit can be decided in

\[
2^{n + O(\log n) - n/\sqrt{m} + o(\sqrt{m})} = 2^{n - \omega(\sqrt{m})}
\]

time, which completes the proof. \( \square \)
8 \( k\)-SAT

We need the following Lemma from [ABDN18].

Lemma 8.1 (Lemma 4.8 in [ABDN18]). There is a polynomial-time many-one reduction from \( \text{TC-SAT} \) to \( \text{CNF-SAT} \) that, given \( \epsilon \in (0, 1) \) and a depth-\( d \) threshold circuit with at most \( cn \) wires, with \( c \geq 1 \), produces a \( k\)-\text{CNF} formula \( \varphi \) on at most \( (1 + \epsilon)n \) variables and with

\[
k \leq (2000(c/\epsilon) \log(2c/\epsilon))^d + 1.
\]

Theorem 8.2. A \( 2^n(1 - 1/k^{1/\omega(\log \log k)}) \) time algorithm for \( k\)-\text{SAT} implies that for any constant \( c > 1 \), \( \mathbb{E}^{\mathbb{N} \mathbb{P}} \) has no \( cn \)-wire depth-(\( c \) log log \( n \)) \text{TC} circuit.

Proof. For any constant \( c \), suppose we are given a circuit of \( (cn/3 - 1) \)-wire and depth-(\( c \) log log \( n \) - 1), in order to apply Theorem 2.4, we need to show the AND of 3 such circuits admits a faster satisfiability algorithm.

Note that AND of 3 such circuits is just a TC circuit of \( cn \)-wire and depth-(\( c \) log log \( n \)), denote that circuit by \( C \). Let \( \epsilon \) be a parameter to be decided later, we apply Lemma 8.1 to transform the satisfiability problem of \( C \) into a \( k\)-\text{CNF} formula \( \varphi \) on \( (1 + \epsilon)n \) variables, with

\[
k \leq (2000(\epsilon/c) \log(4c/\epsilon))^{c \log \log n} + 1.
\]

Now we set \( \epsilon \) so that \( \epsilon^{-1} = 2^{\log^t n} \) for a small constant \( t \). We then have \( \log \log k = \Theta(\log \log n) \).

Applying the assumed \( k\)-\text{SAT} algorithm, the running time can be calculated as

\[
2^{n}\epsilon^{-1} = 2^{n(1 + \epsilon)(1 - \epsilon/c)\omega(1)} = 2^n(1 - \epsilon/c)\omega(1) = 2^n/\log \omega(1) n.
\]

The proof is completed by applying Theorem 2.4.

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References

[AB18] Amir Abboud and Karl Bringmann. Tighter connections between formula-sat and shaving logs. arXiv preprint arXiv:1804.08978, 2018.

[ABDN18] Amir Abboud, Karl Bringmann, Holger Dell, and Jesper Nederlof. More consequences of falsifying seth and the orthogonal vectors conjecture [full version]. In To appear in the proceedings of STOC 2018, 2018.

[ACW16] Josh Alman, Timothy M. Chan, and R. Ryan Williams. Polynomial representations of threshold functions and algorithmic applications. In IEEE 57th Annual Symposium on Foundations of Computer Science, FOCS 2016, 9-11 October 2016, Hyatt Regency, New Brunswick, New Jersey, USA, pages 467–476, 2016.
[AESW91] Pankaj K Agarwal, Herbert Edelsbrunner, Otfried Schwarzkopf, and Emo Welzl. Euclidean minimum spanning trees and bichromatic closest pairs. *Discrete & Computational Geometry*, 6(3):407–422, 1991.

[AG94] Eric Allender and Vivek Gore. A uniform circuit lower bound for the permanent. *SIAM J. Comput.*, 23(5):1026–1049, 1994.

[AHVW16] Amir Abboud, Thomas Dueholm Hansen, Virginia Vassilevska Williams, and Ryan Williams. Simulating branching programs with edit distance and friends: or: a polylog shaved is a lower bound made. In *Proc. of the 48th STOC*, pages 375–388, 2016.

[AK10] Eric Allender and Michal Koucký. Amplifying lower bounds by means of self-reducibility. *J. ACM*, 57(3):14:1–14:36, 2010.

[AM05] Kazuyuki Amano and Akira Maruoka. On the complexity of depth-2 circuits with threshold gates. In *Mathematical Foundations of Computer Science 2005, 30th International Symposium, MFCS 2005, Gdansk, Poland, August 29 - September 2, 2005, Proceedings*, pages 107–118, 2005.

[AW17] Josh Alman and R. Ryan Williams. Probabilistic rank and matrix rigidity. In *Proceedings of the 49th Annual ACM SIGACT Symposium on Theory of Computing, STOC 2017, Montreal, QC, Canada, June 19-23, 2017*, pages 641–652, 2017.

[BF10] Daniel Binkele-Raible and Henning Fernau. A new upper bound for max-2-sat: A graph-theoretic approach. *J. Discrete Algorithms*, 8(4):388–401, 2010.

[BG12] Ivan Bliznets and Alexander Golovnev. A new algorithm for parameterized MAX-SAT. In *Parameterized and Exact Computation - 7th International Symposium, IPEC 2012, Ljubljana, Slovenia, September 12-14, 2012. Proceedings*, pages 37–48, 2012.

[BHPS10] László Babai, Kristoffer Arnsfelt Hansen, Vladimir V Podolskii, and Xiaoming Sun. Weights of exact threshold functions. In *International Symposium on Mathematical Foundations of Computer Science*, pages 66–77. Springer, 2010.

[BR99] Nikhil Bansal and Venkatesh Raman. Upper bounds for maxsat: Further improved. In *Algorithms and Computation, 10th International Symposium, ISAAC ’99, Chennai, India, December 16-18, 1999, Proceedings*, pages 247–258, 1999.

[BSV14] Eli Ben-Sasson and Emanuele Viola. Short pcps with projection queries. In *International Colloquium on Automata, Languages, and Programming*, pages 163–173. Springer, 2014.

[BT94] Richard Beigel and Jun Tarui. On ACC. *Computational Complexity*, 4:350–366, 1994.

[BV14] Eli Ben-Sasson and Emanuele Viola. Short pcps with projection queries. In *Automata, Languages, and Programming - 41st International Colloquium, ICALP 2014, Copenhagen, Denmark, July 7-11, 2014, Proceedings, Part I*, pages 163–173, 2014.

[CG88] Benny Chor and Oded Goldreich. Unbiased bits from sources of weak randomness and probabilistic communication complexity. *SIAM J. Comput.*, 17(2):230–261, 1988.

[CGL+18] Lijie Chen, Shafi Goldwasser, Kaifeng Lyu, Guy Rothblum, and Aviad Rubinstein. Fine-grained complexity meets IP = PSPACE. *arXiv preprint arXiv:1805.02351*, 2018.
[Che18] Lijie Chen. On the hardness of approximate and exact (bichromatic) maximum inner product. *arXiv preprint arXiv:1802.02325*, 2018.

[CIP06] Chris Calabro, Russell Impagliazzo, and Ramamohan Paturi. A duality between clause width and clause density for SAT. In *21st Annual IEEE Conference on Computational Complexity (CCC 2006)*, 16-20 July 2006, Prague, Czech Republic, pages 252–260, 2006.

[CK04] Jianer Chen and Iyad A. Kanj. Improved exact algorithms for max-sat. *Discrete Applied Mathematics*, 142(1-3):17–27, 2004.

[CM17] Arkadev Chattopadhyay and Nikhil S. Mande. Weights at the bottom matter when the top is heavy. *Electronic Colloquium on Computational Complexity (ECCC)*, 24:83, 2017.

[Cop82] Don Coppersmith. Rapid multiplication of rectangular matrices. *SIAM Journal on Computing*, 11(3):467–471, 1982.

[CS15] Ruiwen Chen and Rahul Santhanam. Improved algorithms for sparse MAX-SAT and max-k-csp. In *Theory and Applications of Satisfiability Testing - SAT 2015 - 18th International Conference, Austin, TX, USA, September 24-27, 2015, Proceedings*, pages 33–45, 2015.

[DH09] Evgeny Dantsin and Edward A. Hirsch. Worst-case upper bounds. In *Handbook of Satisfiability*, pages 403–424. 2009.

[DW06] Evgeny Dantsin and Alexander Wolpert. MAX-SAT for formulas with constant clause density can be solved faster than in \( o(s^2) \) time. In *Theory and Applications of Satisfiability Testing - SAT 2006, 9th International Conference, Seattle, WA, USA, August 12-15, 2006, Proceedings*, pages 266–276, 2006.

[FKL+01] Jürgen Forster, Matthias Krause, Satyanarayana V. Lokam, Rustam Mubarakzjanov, Niels Schmitt, and Hans Ulrich Simon. Relations between communication complexity, linear arrangements, and computational complexity. In *FST TCS 2001: Foundations of Software Technology and Theoretical Computer Science, 21st Conference, Bangalore, India, December 13-15, 2001, Proceedings*, pages 171–182, 2001.

[For02] Jürgen Forster. A linear lower bound on the unbounded error probabilistic communication complexity. *J. Comput. Syst. Sci.*, 65(4):612–625, 2002.

[GHNR03] Jens Gramm, Edward A. Hirsch, Rolf Niedermeier, and Peter Rossmanith. Worst-case upper bounds for MAX-2-SAT with an application to MAX-CUT. *Discrete Applied Mathematics*, 130(2):139–155, 2003.

[GHR92] Mikael Goldmann, Johan Håstad, and Alexander A. Razborov. Majority gates VS. general weighted threshold gates. *Computational Complexity*, 2:277–300, 1992.

[GK14] Alexander Golovnev and Konstantin Kutzkov. New exact algorithms for the 2-constraint satisfaction problem. *Theor. Comput. Sci.*, 526:18–27, 2014.

[GN00] Jens Gramm and Rolf Niedermeier. Faster exact solutions for MAX2SAT. In *Algorithms and Complexity, 4th Italian Conference, CIAC 2000, Rome, Italy, March 2000, Proceedings*, pages 174–186, 2000.

[GPW18] Mika Göös, Toniann Pitassi, and Thomas Watson. The landscape of communication complexity classes. *Computational Complexity*, 27(2):245–304, 2018.
[KMRR05] Joachim Kneis, Daniel Mölle, Stefan Richter, and Peter Rossmanith. On the parameterized complexity of exact satisfiability problems. In Mathematical Foundations of Computer Science 2005, 30th International Symposium, MFCS 2005, Gdansk, Poland, August 29 - September 2, 2005, Proceedings, pages 568–579, 2005.

[Kul05] Alexander S. Kulikov. Automated generation of simplification rules for SAT and MAXSAT. In Theory and Applications of Satisfiability Testing, 8th International Conference, SAT 2005, St. Andrews, UK, June 19-23, 2005, Proceedings, pages 430–436, 2005.

[KW16] Daniel M. Kane and Ryan Williams. Super-linear gate and super-quadratic wire lower bounds for depth-two and depth-three threshold circuits. In Proceedings of the 48th Annual ACM SIGACT Symposium on Theory of Computing, STOC 2016, Cambridge, MA, USA, June 18-21, 2016, pages 633–643, 2016.

[Mat91] Jiří Matoušek. Computing dominances in c’n. Inf. Process. Lett., 38(5):277–278, 1991.

[Mat92] Jiří Matoušek. Efficient partition trees. Discrete & Computational Geometry, 8(3):315–334, 1992.

[MR99] Meena Mahajan and Venkatesh Raman. Parameterizing above guaranteed values: Maxsat and maxcut. J. Algorithms, 31(2):335–354, 1999.

[MTT61] Saburo Muroga, Iwao Toda, and Satoru Takasu. Theory of majority decision elements. Journal of the Franklin Institute, 271(5):376–418, 1961.

[MW17] Cody Murray and R. Ryan Williams. Circuit lower bounds for nondeterministic quasi-polytime: An easy witness lemma for NP and NQP. Electronic Colloquium on Computational Complexity (ECCC), 24:188, 2017.

[Nis93] Noam Nisan. The communication complexity of threshold gates. Combinatorics, Paul Erdos is Eighty, 1:301–315, 1993.

[NR00] Rolf Niedermeier and Peter Rossmanith. New upper bounds for maximum satisfiability. J. Algorithms, 36(1):63–88, 2000.

[PPSZ05] Ramamohan Paturi, Pavel Pudlák, Michael E. Saks, and Francis Zane. An improved exponential-time algorithm for k-sat. J. ACM, 52(3):337–364, 2005.

[PS86] Ramamohan Paturi and Janos Simon. Probabilistic communication complexity. Journal of Computer and System Sciences, 33(1):106–123, 1986.

[PS94] Ramamohan Paturi and Michael E. Saks. Approximating threshold circuits by rational functions. Inf. Comput., 112(2):257–272, 1994.

[ROS94] Vwani P. Roychowdhury, Alon Orlitsky, and Kai-Yeung Siu. Lower bounds on threshold and related circuits via communication complexity. IEEE Trans. Information Theory, 40(2):467–474, 1994.

[Rub18] Aviad Rubinstein. Hardness of approximate nearest neighbor search. In STOC, page To appear, 2018.

[RW93] Alexander A. Razborov and Avi Wigderson. n’omega(log n) lower bounds on the size of depth-3 threshold circuits with AND gates at the bottom. Inf. Process. Lett., 45(6):303–307, 1993.
[SS03] Alex D. Scott and Gregory B. Sorkin. Faster algorithms for MAX CUT and MAX csp, with polynomial expected time for sparse instances. In Approximation, Randomization, and Combinatorial Optimization: Algorithms and Techniques, 6th International Workshop on Approximation Algorithms for Combinatorial Optimization Problems, APPROX 2003 and 7th International Workshop on Randomization and Approximation Techniques in Computer Science, RANDOM 2003, Princeton, NJ, USA, August 24-26, 2003, Proceedings, pages 382–395, 2003.

[SST15] Takayuki Sakai, Kazuhisa Seto, and Suguru Tamaki. Solving sparse instances of max SAT via width reduction and greedy restriction. Theory Comput. Syst., 57(2):426–443, 2015.

[SSTT16] Takayuki Sakai, Kazuhisa Seto, Suguru Tamaki, and Junichi Teruyama. Bounded depth circuits with weighted symmetric gates: Satisfiability, lower bounds and compression. In 41st International Symposium on Mathematical Foundations of Computer Science, MFCS 2016, August 22-26, 2016 - Kraków, Poland, pages 82:1–82:16, 2016.

[Tam16] Suguru Tamaki. A satisfiability algorithm for depth two circuits with a sub-quadratic number of symmetric and threshold gates. Electronic Colloquium on Computational Complexity (ECCC), 23:100, 2016.

[Tel17] Roei Tell. Quantified derandomization of linear threshold circuits. Electronic Colloquium on Computational Complexity (ECCC), 24:145, 2017.

[Wil05] Ryan Williams. A new algorithm for optimal 2-constraint satisfaction and its implications. Theor. Comput. Sci., 348(2-3):357–365, 2005.

[Wil13a] Ryan Williams. Improving exhaustive search implies superpolynomial lower bounds. SIAM Journal on Computing, 42(3):1218–1244, 2013.

[Wil13b] Ryan Williams. Towards NEXP versus bpp? In Computer Science - Theory and Applications - 8th International Computer Science Symposium in Russia, CSR 2013, Ekaterinburg, Russia, June 25-29, 2013. Proceedings, pages 174–182, 2013.

[Wil14a] Ryan Williams. New algorithms and lower bounds for circuits with linear threshold gates. In Symposium on Theory of Computing, STOC 2014, New York, NY, USA, May 31 - June 03, 2014, pages 194–202, 2014.

[Wil14b] Ryan Williams. Nonuniform acc circuit lower bounds. Journal of the ACM (JACM), 61(1):2, 2014.

[Wil16] R. Ryan Williams. Natural proofs versus derandomization. SIAM J. Comput., 45(2):497–529, 2016.

[Wil18a] R. Ryan Williams. Limits on representing boolean functions by linear combinations of simple functions: thresholds, relus, and low-degree polynomials. CoRR, abs/1802.09121, 2018.

[Wil18b] Ryan Williams. On the difference between closest, furthest, and orthogonal pairs: Nearly-linear vs barely-subquadratic complexity. In Proceedings of the Twenty-Ninth Annual ACM-SIAM Symposium on Discrete Algorithms, pages 1207–1215, 2018.

[Yao82] Andrew Chi-Chih Yao. On constructing minimum spanning trees in k-dimensional spaces and related problems. SIAM Journal on Computing, 11(4):721–736, 1982.
A An Alternative Proof for Lemma 4.3

Here we present an alternative proof for Lemma 4.3 which reduces the satisfiability problem for \( \text{THR} \circ \text{THR} \) to \( \text{Weighted-Max-IP} \) directly, without applying Corollary 1.3.

Proof of Lemma 4.3 We are going to apply Lemma 4.3 by reducing the satisfiability problem for \( \text{THR} \circ \text{THR} \) circuits to \( \text{Weighted-Max-IP} \) or \( Z-\text{OV} \).

Our reduction here roughly follows Theorem 3.1 of [Wil14a], which is itself inspired by [Mat91]. Let \( \text{LEQ} : \mathbb{Z} \times \mathbb{Z} \to \{0, 1\} \) be the function that \( \text{LEQ}(a, b) := 1 \) if \( a \leq b \) and 0 otherwise. For simplicity, we assume \( n \) is even. Let \( C \) be a \( \text{THR} \circ \text{THR} \) circuit of size \( s = n^k \) and \( G \) be its top \( \text{THR} \) gate. Let \( W_1, W_2, \ldots, W_s, T \) and \( L \) be the weights, threshold and associated linear function of \( G \). Let \( G_1, G_2, \ldots, G_s \) be the corresponding \( \text{THR} \) gates on the bottom layers. We use \( L_1, L_2, \ldots, L_s \) and \( T_1, T_2, \ldots, T_s \) to denote their associated linear functions and thresholds.

For each \( x, y \in \{0, 1\}^{n/2} \), we interpret \( x \) and \( y \) as an assignment to the first half and second half of the input to \( C \) respectively.

For each linear functions \( L_j \), we use \( X_j(x) \) and \( Y_j(y) \) to denote the contribution from \( x \) and \( y \) respectively. We have

\[
G_j(x, y) := \text{LEQ}(T_j, L_j(x, y)) = \text{LEQ}(T_j, X_j(x) + Y_j(y)) = \text{LEQ}(T_j - X_j(x), Y_j(y)).
\]

And therefore

\[
L(x, y) = \sum_{j=1}^s W_j \cdot \text{LEQ}(T_j - X_j(x), Y_j(y)).
\]

Then, for each \( x \in \{0, 1\}^{n/2} \), we construct the vector \( A(x) \), such that \( A(x)_j := T_j - X_j(x) \). Similarly, for each \( y \in \{0, 1\}^{n/2} \), we construct vector \( B(y) \) with \( B(y)_j := Y_j(y) \).

Now, let \( N = 2^{n/2} \). For each \( j \in [s] \), let \( S_j \) be the sorted list of all integers \( A(x)_j \)'s and \( B(y)_j \)'s for \( x, y \in \{0, 1\}^{n/2} \). If two values are the same, items from \( A(x)_j \)'s come first. Then we replace each \( A(x)_j \)'s and \( B(y)_j \)'s by their ranks in the list \( S_j \). It is easy to see that this step reduces the weight to \( 2N \), and preserves the value of \( \text{LEQ}(A(x)_j, B(y)_j) \).

Let \( t \) be a parameter to be specified later, for each \( j \), we partition \( S_j \) into \( t \) buckets, each of size at most \( \lceil 2N/t \rceil \). Let \( x, y \in \{0, 1\}^{n/2} \) be assignments to \( A \) and \( B \), there are two cases:

There is a \( j \in [s] \) such that \( A(x)_j \) and \( B(y)_j \) are in the same buckets. In this case, note that for each \( x \in \{0, 1\}^{n/2} \), there are at most \( s \cdot (2N/t) \) possibly \( y \) such that \( (x, y) \) belongs to this case. Hence, we can enumerate all such pairs and check them in \( N^2/t \cdot s^e \) time for a universal constant \( c \).

For all \( j \in [s] \), \( A(x)_j \) and \( B(y)_j \) are in different buckets. In this case, we can safely replace each \( A(x)_j \) and \( B(y)_j \) by the indexes of their buckets, which reduces their range to \( [t] \).

Now we define some auxiliary vectors to ease our construction. For \( k \in [t] \), we define \( e^k \in \{0, 1\}^t \) such that \( e^k_i = 1 \) if and only if \( i = k \), we also define \( o^k \in \{0, 1\}^t \) such that \( o^k_i = 1 \) if and only if \( k > i \). Recall that for two vectors \( u, v \in \{0, 1\}^* \), we use \( u \circ v \) to denote their concatenation. We define

\[
u(x) := (o^s_1 e^{[A(x)_1]} \circ o^s_2 e^{[A(x)_1]})
\]
Lemma B.2

\( v(y) := (\sigma_{j=1}^s e^{[B(y)j]}) \circ (\sigma_{j=1}^s e^{[B(y)j]}) \),
\( w := (\sigma_{j=1}^s (W_j)^{\otimes t}) \circ (-M)^{\otimes (s+t)}. \)

In which \( M \) denote a sufficient large number (can be treated as infinity) and \((W_j)^{\otimes t}\) denotes a vector repeating \( W_j \) \( t \) times.

Now, consider \( u(x) \otimes_w v(y) \), it is straightforward to verify that that value would be very small if there exists a \( j \in [s] \) such that \( A(x)_j = B(y)_j \), and is equal to \( L(x,y) \) otherwise.

Therefore, computing the maximum of \( u(x) \otimes_w v(y) \) for all \( x,y \in \{0,1\}^{n/2} \) solves this case, which can be reduced to a Weighted-Max-IP\(_{N,2nt} \) instance.

Setting \( t = s^c \cdot n^{k'} \) for an integer \( k' \). The running time becomes \( O(N^2/n^{k'}) \) plus the running time for solving Weighted-Max-IP\(_{2^{n/2},O(n\cdot(1+k'))} \), which is also \( O(N^2/n^{k'}) = O(2^n/n^{k'}) \) by our assumption. Applying Lemma 4.1 completes the proof.

The reduction to \( \text{Z-OV} \) works roughly the same, with the only modification that we transform the THR \( \circ \) THR circuit into an equivalent DOR \( \circ \) ETHR \( \circ \) THR at the beginning (via Proposition 2.1 (3)), and solve each ETHR \( \circ \) THR sub-circuits separately via a similar reduction to \( \text{Z-OV} \).

\[ \square \]

### B Applications of Structure Lemma I in Communication Complexity

In this section we prove Theorem 1.13. First we introduce the formal definition of RP \( \cdot \) UPP\(_{cc} \) protocols.

**Definition B.1** (RP \( \cdot \) UPP\(_{cc} \) Protocols). For a problem \( \Pi \) with inputs \( x, y \) of length \( n \) (Alice holds \( x \) and Bob holds \( y \)), we say a communication protocol is a RP \( \cdot \) UPP communication protocol with cost \( c \) if the following holds.

- Alice and Bob jointly toss \( c \) public coins to get a string \( z \in \{0,1\}^c \).
- Given \( y \) and \( z \), Bob sends Alice \( c \) bits, and Alice decides to accept or not\(^8\) They have an unlimited supply of private random coins (not public, which is important) during their conversation.
  - If \( \Pi(x,y) = 1 \), for at least half \( z \)'s from \( \{0,1\}^c \), Alice accepts with probability \( > 1/2 \).
  - Otherwise, for all \( z \) from \( \{0,1\}^c \), Alice accepts with probability \( < 1/2 \).

Also, we need the following standard fact about THR \( \circ \) MAJ circuits.

**Lemma B.2** ([FKL+01]). For a function \( F : \{0,1\}^n \times \{0,1\}^n \to \{0,1\} \), suppose it admits a THR \( \circ \) MAJ circuit of size \( s \), then it also admits a UPP\(_{cc} \) protocol of cost \( O(\log s) \).

Then Theorem 1.13 follows directly from Lemma 1.6 and Lemma B.2.

**Proof of Theorem 1.13** Given a THR \( \circ \) THR circuit \( C \) of size \( s \) computing \( F \), by Lemma 1.6 it has an equivalent Gap-OR \( \circ \) THR \( \circ \) MAJ circuit \( C' \) of size \( \text{poly}(s) \). Alice and Bob first toss \( O(\log s) \) public coins to select a THR \( \circ \) MAJ sub-circuit of \( C' \) at uniformly random, and simulate the \( O(\log s) \) cost UPP\(_{cc} \) protocols for it by Lemma B.2

\[ \square \]

\(^8\)In UPP, one-way communication is equivalent to the seemingly more powerful one in which they communicate [PS86].