Abstract—This article presents a commutated-inductor–capacitor (commutated-LC) or switched-LC circuit that acts as a radio frequency (RF) delay line. Thanks to its linear-periodically time-varying (LPTV) operation and fully passive implementation, it concurrently achieves long maximum delays, fine delay tuning steps, and wide instantaneous bandwidths while being low loss and highly linear. Unlike existing LPTV switched-capacitor broadband delays, the introduction of inductors in the proposed commutated-LC delay circuit provides a new degree of freedom, allowing it to operate at a much higher RF with a wider instantaneous bandwidth. A proof-of-concept prototype in a 65-nm CMOS process demonstrates a measured 1.3-GHz 3-dB bandwidth around a 4.3-GHz RF, i.e., a 30% fractional bandwidth, when clocked at 250 MHz. The measured maximum delay is 1.4 ns with a 23-dB loss and noise figure; this loss or noise is orders of magnitude lower compared with fully passive linear-time-invariant RF delay lines operating at a similar frequency with the same delay. The measured IIP3 is $+16$ dBm.

Index Terms—Bandwidth, CMOS, delay, inductor, linear-periodically-time-varying (LPTV), N-path, radio frequency.

I. INTRODUCTION

A N INTEGRATED radio frequency (RF) delay line is a key building block for many existing and emerging broadband wireless circuits and systems, such as magnet-less circulators [1], broadband antenna arrays [2], [3], and full-duplex transceivers [4]–[6]. The fundamental challenge associated with an integrated RF delay line is to concurrently achieve a long delay, often on a nanosecond scale, a fine delay tuning step, and a wide instantaneous bandwidth while retaining high linearity, low noise, and reasonable dc power.

By creating quasi-electromagnetic-wave prorogation on chip, LC-based artificial transmission line is a common way of realizing integrated RF delay lines [2], [3]. However, to achieve programmable delays with high tuning resolution, these artificial transmission lines have to be divided into many unit cells, increasing chip area and insertion loss substantially. LC-based all-pass filter RF delay lines have also been reported for larger delay-bandwidth products and lower delay variation compared with artificial transmission lines [7], [8]. But, they still suffer from large chip areas and high insertion loss when both large delay spreads and small delay steps are needed.

For area-efficient and low-loss RF delay generation and/or programming, active components have been included in LC-based delay circuits [3], [9]. However, the presence of active circuits results in degraded linearity performance when compared with an all-passive design (e.g., [7], [8]). Active $G_m$-C circuits also allow compact inductor-less RF delay lines [10], [11]. However, these inductor-less delay lines have limited dynamic range due to the presence of active devices and are often limited to a sub-3-GHz RF due to parasitic effects.

Besides linear time-invariant (LTI) delay elements, linear periodically time-varying (LPTV) N-path switched-capacitor circuits have been reported for delay generation but they possess their own challenges. N-path RF filters with $\geq 10$-ns delay have been demonstrated but have a very limited delay-bandwidth product, resulting in narrowband operation [5], [12], [13]. Compared with an N-path filter, an RF switched-capacitor sampler has a larger delay-bandwidth product hence supporting broad instantaneous bandwidth [4], [14]–[18]. However, an RF switched-capacitor sampler has high insertion loss when used in RF systems with resistive (e.g., 50 $\Omega$) interfaces; this high insertion loss is due to the fact that the RC time constant is much smaller compared with the switch on-time in a sampler. Recently, a broadband switched-capacitor delay has been reported in [1] and [19] with the RC time constant similar to the switch on time. It demonstrates nanosecond-scale delays, fine delay tuning steps, broad fractional bandwidths, high linearity, and low noise at the same time. However, its maximum achievable delay is coupled with its RF, limiting its operation frequencies to low RF bands (e.g., below 1 GHz), when nanosecond delays are needed.

In this work, we present an N-path switched-inductor–capacitor (switched-LC) or a commutated-LC RF delay circuit, as shown in Fig. 1. It allows all-passive, compact, and low-loss RF delay elements with gigahertz-wide instantaneous bandwidths, nanosecond-scale maximum delays, and clock-path-defined fine delay tuning steps, at a beyond 3-GHz RF.

Unlike switched-capacitor broadband delay lines (e.g., [1], [4], [19], [20]), our proposed commutated-LC delay circuit decouples the maximum achievable delay with its RF, since the introduction of inductors provides a new degree of freedom to existing LPTV circuits. This allows it to operate at a much higher RF while preserving key features of an LPTV circuit. Compared with all-passive LC-based delay lines (e.g., [7], [8]), our proposed LPTV commutated-LC RF delay circuit is compact, low loss, and has fine delay resolution.
Section VI concludes this article.

This article is organized as follows. In Section II, we propose an approximated fundamental transfer function for commutated-\(LC\) circuits. In addition, we briefly review the case when a commutated-\(LC\) circuit operates as an \(N\)-path filter (e.g., [21]–[23]), showing its limited delay-bandwidth product and incapability of constant-bandwidth delay tuning.

The \(N\)-path commutated-\(LC\) circuit in Fig. 1 acts as an \(N\)-path filter when the bandwidth of the RLC circuit that consists of the \(LC\) load and the source resistance \(R_0 = R_0 + R_{\text{on}}\) is narrow; that is \((2\pi R_0'' |R_L|)^{-1}\) being small. We will quantify this condition shortly.

Similar to the behavior of a switched-capacitor \(N\)-path filter [12], an \(N\)-path commutated-\(LC\) filter creates many narrow passbands around \(f_R + k f_c\), where \(f_R\) is the \(LC\) resonance frequency, \(f_c\) is the commutation or switching frequency, and \(k\) is an integer [24], [25]. Intuitively, the periodic switching operation translates the \(LC\) load narrow bandwidth frequency response to the switching frequency harmonics [12].

Consider a design example as shown in Fig. 1 with \(C = 2.5\) pF, \(f_R = 1/(2\pi \sqrt{LC}) = 5\) GHz, \(R_0 = 50\) \(\Omega\), \(R_{\text{on}} = 5\) \(\Omega\), \(R_L \rightarrow \infty\), \(f_c = 1.5\) GHz, and \(T_d = T_C/2\). The simulated fundamental transfer function is given in Fig. 3, showing narrow passbands around \(f_R + k f_c\) and is similar to that of an \(N\)-path switched-capacitor filter [12].

Let us quantify this transfer function. Deriving a precise one using an LPTV analysis akin to that in [26] is involved due to the presence of additional inductors. Interestingly, we find that the transfer function can be approximated by the \(N\)-path switched-capacitor circuit transfer function; for example, the one given in [27, eq. (15)] with a frequency shift. Our proposed approximated transfer function is given as

\[
H_0(f + f_R) \approx \frac{N f_c e^{j2\pi f_c(T_C \frac{f}{f_{RC}} - T_d)}}{2\pi f_{BC} \left(1 + \frac{f}{f_{RC}}\right)^2} \times \frac{\left(e^{j2\pi f f_{RC}} - e^{-j2\pi f_{RC} f_c / N}\right)^2}{e^{j2\pi f f_{RC}} - e^{-j2\pi f_{RC} f_c / N}} \cdot \frac{R_0}{R_0}
\]

where \(N\) is the number of paths, \(f_R = (2\pi \sqrt{LC})^{-1}, f_{RC} = (4\pi R_0'' |R_L|)^{-1}\), and \(R_0' = R_0 + R_{\text{on}}\).

While an LPTV network has many harmonic transfer functions [26], we are mostly interested in the fundamental one as the desired input and output in our system are at the same frequency.
Unlike in a switched-capacitor circuit where the transfer function is exact, (1) is an approximated transfer function, and the approximation holds only when the RLC circuit is deeply underdamped; in other words, the RLC circuit satisfies

\[
\alpha = \frac{1}{2 R_0 || R_L C} \ll 2 \pi f_R
\]  

(2)

where \( \alpha \) is the damping factor [28]. As \( \alpha/\omega_R \) increases and approaches 1, the peak of the frequency response of a commutated-LC circuit shifts to lower frequencies compared to \( f_R \), reducing the accuracy of our model. In addition, as we will see in Section III-A, the maximum achievable delay and delay spread are inversely proportional to \( \alpha \). Therefore, a small \( \alpha \) is also needed for large delays.

The rationale behind (1) can be shown using a comparison between a commutated-LC and a commutated-capacitor circuit. Let us consider an internal voltage across one of the LC or capacitor loads as the output equals to a weighted sum of the internal node voltages as \( V_{r2}(t) = \sum_{n=1}^{N} v_n(t) \cdot \text{sw}_{n,R}(t) \) (see Fig. 1). As in Fig. 4, only a single path is needed in this case given memory-less source and load impedance \( R_0 \) and ideal non-overlapping 12.5%-duty-cycle clocks [26]. Without loss of generality, the first path is considered.

For the switched-LC circuit in Fig. 4(a), we have \( v_S(t) = V_0 \sin(\omega_R t) \), \( C = 5 \) pF, \( f_R = 1/(2\pi \sqrt{LC}) = 5 \) GHz, \( R_0 = 55 \) \( \Omega \), \( R_L \rightarrow \infty \), \( f_C = 1.5 \) GHz., and \( T_d = T_C/2 \). The damping factor \( \alpha = [2 R_0 || R_L C]^{-1} = 1.8 \) G rad/s is much less than \( 2\pi f_R = 31.4 \) G rad/s; hence, the RLC circuit is underdamped when the input or output switch is closed.

Since it is underdamped and we have \( \alpha \ll \omega_R \), the voltage across the LC load is proportional to \( e^{-\alpha t} \sin(\omega_R t + \phi) \), where \( \phi \) is a constant and \( \omega_d = (\omega_R^2 - \alpha^2)^{1/2} \approx \omega_R \) is damped natural angular frequency [28]. When both switches are open, the LC load holds the stored energy just like a capacitor, but in both the magnetic and electric fields. We will consider lossy inductors in Section III.

Removing the inductor and doubling the capacitance, we arrive at the switched-capacitor circuit in Fig. 4(b). As can be seen in Fig. 4(d), the internal voltage \( V_1 \) here is essentially the envelope of that in the switched-LC circuit in Fig. 4(a).

Fig. 5. Simulated (solid) and calculated [dashed, using (1)] close-in transfer function and group delay of the commutated-LC filter in Fig. 1 with varying \( C = 1.25, 2.5, \) and 5 pF, fixed \( f_R = 1/(2\pi \sqrt{LC}) = 5 \) GHz, \( R_0 = 50 \) \( \Omega \), \( R_{\text{ON}} = 5 \) \( \Omega \), \( R_L \rightarrow \infty \), \( f_C = 1.5 \) GHz., and \( T_d = T_C/2 \).

Now, we can say that (1) is based on the fact that the output voltage has the form of \( e^{-\alpha t} \sin(\omega_R t + \phi) \), a product of a negative exponential term and a sine term when any of the output switches in Fig. 1 is on.

The negative exponential \( e^{-\alpha t} \) signifies a damped waveform with a time constant \( t_d = 1/\alpha \). This negative exponential is identical to the natural response of an RC circuit with a time constant \( t_{RC} = 2 R_0 C = 1/2\pi f_{RC} \). This effective time constant \( t_{RC} \) corresponds to the effective RC frequency \( f_{RC} = (4\pi R_0 || R_L C)^{-1} \) used in (1). The sine term signifies a frequency shift of \( f_R \) in the transfer function given in (1).

The calculated transfer function of the aforementioned design example using (1) is plotted in Fig. 3, showing a good match with the simulation.

Let us define the ratio between the switch-on time and the time constant as \( \Gamma \) similar to that in a switched-capacitor circuit [26]

\[
\Gamma \equiv \frac{T_C}{N} \frac{2 R_0 || R_L C = \frac{\alpha T_C}{N}}.
\]

(3)

When \( \Gamma \) is small and \( \ll \pi/2 \), the commutated-LC circuit acts as an \( N \)-path filter. We will discuss the choice of \( \pi/2 \) in Section III. For example, in Fig. 3, we have \( \Gamma = 0.3 \).

Like in an \( N \)-path switched-capacitor filter [26], [27], it can be shown that the commutated-LC filter bandwidth and peak group delay around \( f_R \) can be written as follows:

\[
f_{BW, filter} = \frac{1}{2} f_{RC}
\]

(4)

\[
f_{\text{Filter Delay}} = \frac{2}{\pi f_{RC}}.
\]

(5)

Simulated commutated-LC filter close-in fundamental transfer functions are plotted in Fig. 5 with varying capacitance values. As \( C \) increases from 1.25 to 2.5 pF and to 5 pF, the simulated bandwidth reduces from 0.62 to 0.3 GHz and to 0.14 GHz, and the simulated peak group delay increases from 0.6 to 1.2 ns and to 2.2 ns. These simulated bandwidths and peak group delays show a good match between those calculated using (4) and (5).

Equations (4) and (5) show that the delay-bandwidth product of a commutated-LC filter is limited to \( 1/\pi \). Unsurprisingly, an \( N \)-path switched-capacitor filter also has a delay-bandwidth limit of \( 1/\pi \) [1], [29]. Moreover, in an \( N \)-path-filter-based delay circuit, constant-bandwidth delay-tuning is impossible as the delay-bandwidth product is always \( 1/\pi \).
III. COMMUTATED-LC BROADBAND DELAYS

The N-path commutated-LC circuit in Fig. 1 acts as broadband delay when \( \Gamma \approx \pi/2 \). We show that this \( \Gamma \) choice results in a maximum delay-bandwidth of around 4 in an eight-path single-ended design—an order-of-magnitude improvement compared with that of an N-path filter.

As will be discussed momentarily, we choose \( \Gamma = \pi/2 \) as it corresponds to the case, where the effective sampling frequency \( Nf_c \) is twice as large as the RLC tank 3-dB bandwidth, i.e., \( Nf_c = 2f_{3\text{d}B} \), where \( f_{3\text{d}B} = (2\pi R_0||R_1C)^{-1} \).

We also study the impact of on-chip lossy inductors. The proposed commutated-LC delay achieves its low loss and compactness by moving delay tuning from the signal path to the clock path similar to switched-capacitor delay circuits [1], [15]–[17], and by allowing delay non-reciprocity.

Finally, we investigate the effects of switch parasitic and clock overlap on the performance of our commutated-LC broadband delay circuit.

A. Broadband Delay With Independent Clock-Path Bandwidth and Delay Tuning

The broadband delay operation of the N-path commutated-LC circuit can be intuitively explained in the time domain.

As discussed in Section II, a commutated-LC circuit acts like a switched-capacitor circuit but with a frequency shift \( f_R \) and an effective time constant \( \tau_{RC} = 2R_0||R_1C = 1/2\pi f_{3\text{d}B}/R_{RC} \). Unlike the existing broadband N-path switched-capacitor delay circuits that have frequency responses centered around dc [1], [4], [20], introducing an inductor to each path allows our proposed delay circuit to operate at a much higher frequency around \( f_R \). Fundamentally, the introduction of magnetic fields provides a new degree of freedom, breaking the limits of switched-capacitor circuits.

When \( \Gamma \approx \pi/2 \), the time constant \( \tau_{RC} \) is similar to input switch-on duration \( T_C/N \) based on (3). Therefore, the voltage envelope of each LC tank in the commutated-LC circuit tracks that of the input during each switching period (see Fig. 6), instead of storing the average input over many periods when \( \Gamma \ll \pi/2 \) as in an N-path filter.

Together, the \( N \) paths in the commutated-LC circuit operate like a time-interleaved “slow” sampler that faintly tracks the input with an effective sampling frequency of \( Nf_c \). By storing the sampled energies at the LC tanks and releasing them to output at a clock-defined time, a delay can be introduced to the output signal \( v_{2}(t) \).

Commutated-LC delay circuit (Fig. 1) simulation with varying \( \Gamma \) is shown in Fig. 7. As \( \Gamma \) increases from \( \pi/10 \) to \( \pi/2 \), the transfer function magnitude and group delay no longer resemble a comb filter that is seen in N-path filters; instead, they are flattened across multiple local oscillator (LO) harmonics, supporting a broadband operation centered around \( f_R \).

Calculated transfer function magnitudes using (1) are plotted in Fig. 7; the simulation and calculation results match well with each other regardless of \( \Gamma \) choices.

Evaluating the magnitude of the transfer function given in (1) at discrete frequencies \( f = f_R + k f_c \) with \( k \) being an integer results in

\[
|H_0(f_R + k f_c)| = \frac{1 + e^{-2\Gamma} - 2 e^{-\Gamma} \cos(k 2\pi N) }{\Gamma(1-e^{-2\Gamma})} \left[ 1 + \left( \frac{k}{N(2\pi)} \right)^2 \right] \frac{R_0}{R_0^2} \tag{6}
\]

Based on (6), we know the transfer function magnitude peaks at \( 1/(\Gamma \cdot R_0^2) \) when \( k = 0 \). Evaluating (6) numerically with \( \Gamma = \pi/2 \), the magnitude drops by 3 dB when \( |k| > \Gamma N/(2\pi) \); this gives us the lower bound on the 3-dB bandwidth. In addition, since our commutated-LC circuit acts as a sampler with sampling frequency of \( Nf_c \), the one-sided signal bandwidth is bounded by \( N/2f_c \) based on the Nyquist–Shannon sampling theorem. Given that the RF bandwidth corresponds to the two-sided baseband (BB) bandwidth, the RF 3-dB bandwidth upper bound is \( Nf_c \).

Therefore, the delay line RF bandwidth is bounded based on

\[
N \cdot f_c > f_{\text{BW, delay}} > \frac{N}{2} \cdot f_c \tag{7}
\]

Similar to switched-capacitor RF broadband delay circuits [1], [20], the delay is clock-path defined and
non-reciprocal as
\[ \tau_{\text{delay,21}} \approx T_d, \quad \tau_{\text{delay,12}} \approx T_C - T_d \]  \tag{8}
where \( \tau_{\text{delay,21}} \) is the delay when the signal travels from the port 1 to port 2, \( T_d \) is the clock-path delay as defined in Fig. 1, and \( \tau_{\text{delay,12}} \) is the delay when the signal travels in the opposite direction. The magnitude response in (6) applies to signals traveling in either direction. This is because the transfer function magnitude is independent of delay assuming lossless LC tanks and no clock overlapping.

The signal path delay \( \tau_{\text{delay,21}} \) and \( \tau_{\text{delay,12}} \) are approximately the same and smaller compared with the clock-path delay \( T_d \) and \( T_C - T_d \), respectively; the difference between the signal- and clock-path delays is due to the fact that the RLC circuit or the signal delaying component in our design is dispersive. As shown in [1], replacing each LC tank with a dispersion-less ideal transmission line makes the signal-path delay constant and exactly the same as the clock-path delay; however, on-chip transmission lines are very bulky and lossy, and hence, capacitors are used instead in [1].

Equation (8) makes sense intuitively as we discussed earlier—a time delay can be introduced to the signal (see Fig. 6) by storing the sampled energies at the LC tanks and releasing them to output at a clock-defined time. Equation (8) also indicates the non-reciprocal operation of the LPTV delay line.

The maximum achievable delay is set by the switching period \( T_C \) due to the periodic nature of the clocks. For example, looking at the clock waveforms in Fig. 1, a clock-path delay of \( 1.5T_C \) cannot be distinguished from a \( 0.5T_C \) delay. In addition, since clock overlapping between the delay line

where we have substituted \( T_C / N \) with \( \Gamma / \alpha \) based on (3).

Therefore, given a fixed \( \Gamma \approx \pi / 2 \), a small \( \alpha \) or a deeply underdamped LC circuit results in large maximum delay \( \tau_{\text{delay,max}} \) or delay spread \( \tau_{\text{delay,max}} - \tau_{\text{delay,min}} \).

Simulation results of the commutated-LC delay circuit with varying delays \( T_d = T_C / 2 \) and \( T_d = 7T_C / 8 \) are given in Fig. 8, using \( C = 1.45 \text{pF}, \Gamma = \pi / 2, f_C = 1 / (2\pi \sqrt{LC}) = 5 \text{GHz}, R_0 = 55 \Omega, \) and \( f_C = 0.5 \text{GHz} \). The simulated 3-dB bandwidth is 2.4 GHz regardless of \( T_d \) and is larger than \( 8/2 \times 0.5 = 2 \text{GHz} \) as expected based on (7). When \( T_d = T_C / 2 = 1 \text{ns} \), the simulated average group delays in both directions are 0.9 ns with around a \( \pm 0.1 \text{-ns} \) ripple. When \( T_d = 7T_C / 8 = 1.75 \text{ns} \), the simulated average group delay is 1.7 ns in the forward direction and is 0.2 ns in the other; the delay ripple is around \( \pm 0.1 \text{ns} \) in both directions. These delay simulations show good match with those predicted by (8) and (9).

Despite sharing the same schematic, the proposed commutated-LC broadband delay is fundamentally different from the \( N \)-path-filter-based delay element that we discussed in Section II, considering (4), (5), and (7)–(9). First, the maximum delay-bandwidth product is around 4 in an eight-path design, corresponding to an order-of-magnitude improvement. Second, the bandwidth and delay tunings are both relocated from the signal path to the clock path akin to that
in a switched-capacitor sampler [1], [15]–[17]. Third, the bandwidth and delay tunings are de-coupled and controlled by the clock frequency and clock-path delay, respectively, allowing constant-bandwidth delay tuning. Finally, the proposed commutated-LC broadband delay exhibits delay non-reciprocity. It should be noted that while an N-path filter has clock-path-defined phase tuning [29], it relies on changing the signal-path RC time constant for delay control based on (5). In addition, an N-path filter is non-reciprocal in its phase but does not delay [30].

When compared with LTI all-passive LC-based delay circuits (e.g., [7], [8]), the clock-path delay control, similar to that in switched-capacitor delay circuits [1], [14], [20], enables compact, low-loss, and high-resolution delay tuning as it avoids having many series LC sections that are needed to achieve fine delay resolution. The delay non-reciprocity also helps to further reduce the delay line size by half compared with its LTI reciprocal counterpart as discussed under the context of a switched-capacitor delay line design in [1]. Intuitively, this is because the total delay from both propagation directions in an LPTV non-reciprocal delay line is half of that in an LTI reciprocal counterpart. In many applications, such as self-interference cancellation and beam-forming systems, only a one-way delay is needed at a time.

B. Lossy Inductors

Here, we study the impact of lossy on-chip inductors on delay line performance, including insertion loss, noise, bandwidth, and delay generation.

As shown in Fig. 1, we model the inductor loss via an equivalent shunt resistor $R_L$. Assuming $R_L \gg R_0$, the capacitance can be calculated using (3) as $C = T_C/(2N R_0 \Gamma)$. Then, based on $f_R = 1/2 \pi \sqrt{L/C}$, the inductance is

$$L = \frac{1}{\omega_R^2} \cdot \frac{2N R_0 \Gamma}{T_C}. \tag{10}$$

Given $\Gamma = \pi/2$, $f_R = 5$ GHz, $N = 8$, $T_C = 2$ ns, and $R_0 = 55 \ \Omega$, $L$ is calculated to be 0.7 nH using (10). In addition, $R_L = L \cdot Q_{LR} = 219 \ \Omega$ assuming $Q_{LR} = 10$ at 5 GHz. In this case, $R_L$ is only four times larger compared with $R_0$. Hence, $R_L \parallel R_0$ is noticeably smaller than $R_0$, resulting in a higher $\Gamma = 1.9$ based on (3). Nevertheless, we find that the delay circuit performance largely remains unchanged so long as $\Gamma \approx \pi/2$ and keep $\Gamma = 1.9$ in our example design here.

First, let us find the in-band input impedance and insertion loss with lossy inductors.

Given $v_i(t) = V_S \cos(\omega_{Rt})$, $V_S = 0.1 \ \text{V}$, $C = 1.45 \ \text{pF}$, $\Gamma = \pi/2$, $f_R = 5$ GHz, $R_0 = 55 \ \Omega$, $f_c = 0.5$ GHz, $T_d = T_C/2$, and $Q_L = 10$, the simulated steady-state internal node voltage $v_i(t)$ of the commutated-LC circuit (Fig. 1) is plotted in Fig. 9. Since $\alpha^2 \ll \omega_c^2$, we can write the internal node voltage of the i-th path $v_i(t)$ in Fig. 1 as

$$v_i(t) = \cos(\omega_{Rt}) \cdot e_i(t) \tag{11}$$

where $i$ is the path index, i.e., an integer from 1 to 8, and $e_i(t)$ is a periodic function that captures the changing envelope.

Each $e_i(t)$ period can be divided into four phases, corresponding to four windowing functions, $w_{i,b}$, $w_{i,e}$, and $w_{i,d}$, as shown in Fig. 10. It starts when the input-side switch $sw_{i,F}$ changes from open to close, the RLC circuit begins to faintly track the source signal during $w_{i,a}(t) = sw_{i,F}(t)$. In the second phase $w_{i,b}$, both input and output side switches are open, the voltage across the RLC circuit starts to damp out with a smaller damping factor $\alpha = 1/(2R_0/C)$ compared with $a = 1/(2R_0/C)$. During the third phase $w_{i,c}(t) = sw_{i,B}(t)$, the output side switch $sw_{i,B}$ is closed, the energy stored in RLC circuit is slowly released to the output with the damping factor $\alpha$. Finally, the RLC circuit continues its damping in the $w_{i,d}$ with $\alpha$. Assumed the remaining energy at the end of the each $e_i(t)$ period is negligible given lossy on-chip inductors and long delays, the periodic envelope function $e_i(t)$ can be approximated as

$$e_i(t) \approx w_{i,a}(t) \cdot V_S \cdot \frac{R_L}{R_0 + R_L} \left(1 - e^{-T_{e_i}/N} \right)$$
$$+ w_{i,b}(t) \cdot V_{IF} \cdot e^{-a(t-iT_c)/N}$$
$$+ w_{i,c}(t) \cdot V_{IF} \cdot e^{-a(t-(T_d-T_c)/N)} e^{-\frac{T_{PD}}{2}} e^{-a(t-T_d-iT_c)/N}$$
$$+ w_{i,d}(t) \cdot V_{IF} \cdot e^{-a(t-\frac{T_{PD}}{2})} \tag{12}$$

where $V_{IF} = V_S (R_L/R_0 + R_L) (1 - e^{-T_{PD}})$. Now, given $v_i(t)$ is known based on (11) and (12), the commutated-LC delay input impedance and insertion loss with lossy on-chip inductors at $f_R$ are readily to be calculated.

Input voltage $v_{P1}(t)$ in Fig. 1 periodically rotates among all the internal voltages, and hence, can be expressed as

$$v_{P1}(t) = \sum_{i=1}^{N} v_i(t) \cdot sw_{i,F}(t).$$

Substituting $v_i(t)$
with (11)(12), we have

\[
\begin{align*}
\nu_p(t) &= V_S \cos(\omega R t) \cdot \frac{R_L}{R_0 + R_L} \\
&\quad \sum_{i=1}^{N} \left( 1 - e^{-t} e^{-\alpha(t-T_0)} \right) \cdot s_{i,B}(t) \\
&= \frac{V_S \cos(\omega R t) \cdot R_L}{R_0 + R_L} \left( 1 - e^{-t} \right) + \sum_{\text{harmonics}}.
\end{align*}
\]

(13)

The input impedance is the ratio between the input voltage and the input current as

\[
R_i = \frac{V_p}{\nu_p} = \frac{R_0 + R_L}{(V_S - V_p)/R_0 + \sum_{i=1}^{N} \alpha_i v_i(t) \cdot s_{i,B}(t)}
= \frac{1 + e^{-t} R_L}{\frac{1}{\Gamma} R_0} + \sum_{\text{harmonics}}.
\]

(14)

Similarly, output voltage \(v_p(t)\) in Fig. 1 can be expressed as

\[
\begin{align*}
\nu_p(t) &= R_0 \frac{V_p}{R_0} \sum_{i=1}^{N} \alpha_i v_i(t) \cdot s_{i,B}(t) \\
&= \frac{R_0}{R_0} V_p \cos(\omega R t) \cdot \alpha_i(T_0 - T_c)/N \left( 1 - e^{-t} \right) + \sum_{\text{harmonics}}.
\end{align*}
\]

(15)

Based on (15), the gain from \(V_S\) to \(V_p\) at \(f_R\) is

\[
\begin{align*}
G_{21} &= e^{-\alpha(T_0 - T_c)/N} \left( 1 - e^{-t} \right)^2 \left( \frac{R_0 + R_L}{R_0 + R_L} \right) \left( \frac{R_0}{R_0} + \frac{R_L}{R_0} \right) \\
&= e^{-\alpha(T_0 - T_c)/N} \left( 1 - e^{-t} \right)^2 \left( \frac{R_0}{R_0 + R_L} \right) \left( \frac{R_0}{R_0 + R_L} \right) \left( \frac{R_0}{R_0 + R_L} \right) H_0(f_R)
\end{align*}
\]

(16)

where \(\alpha_i = 1/(2 R_L C)\) and \(H_0(f)\) is the transfer function in (1). Similarly, if the source voltage is moved from port 1 to port 2 in Fig. 1, and based on (8), the gain becomes

\[
G_{12} = e^{-\alpha(T_0 - T_c)/N} \left( 1 - e^{-t} \right)^2 \left( \frac{R_0}{R_0} + \frac{R_L}{R_0} \right) \left( \frac{R_0}{R_0} + \frac{R_L}{R_0} \right) H_0(f_R)
\]

(17)

Regarding the transfer function across frequencies, we expect that it should be similar to that with lossless inductors given in (1). This is because the output always connects to one of the LC tanks as \(v_p(t) = \sum_{i=1}^{N} \alpha_i v_i(t) \cdot s_{i,B}(t)\) and the RLC circuit is nearly the same with or without inductor loss so long as \(R_L\) is significantly larger compared with \(R'\). Therefore, a generalized transfer function that considers inductor loss can be written as

\[
H_{0,Gen,21}(f) \approx e^{-\alpha(T_0 - T_c)/N} \left( 1 - e^{-t} \right) R_L \frac{R_0 + R_L}{R_0} H_0(f)
\]

(18)

From (18), we see that \(H_{0,Gen,21}(f)\) is now \(T_d\) dependent, unlike the transfer function (1) assuming lossless inductors. This makes sense intuitively. When input- and output-side switches are off, the energy held by a lossless LC tank never changes. However, for a lossy LC tank, more energy is damped out with a longer delay.

Since the sum of delays in both directions is \(T\) regardless of \(T_d\) [see (8)], the transfer functions sum is independent of \(T_d\). In addition, the generated delays are governed by (8) and (9). Finally, the noise figure of the delay line is dominated by the inductor loss, and hence, in-band noise factor at \(f_R\) can be approximated as \(F_{21} \approx G_{21}^{-1}\) and \(F_{12} \approx G_{12}^{-1}\).

Simulated delay line performance with lossy inductors across different \(T_d\) using \(Q_L = 10, R' = 55 \Omega, f_c = 0.5 GHz, C = 1.45 \mu F, f_R = 1/(2 \pi \sqrt{L C}) = 5 GHz,\) and \(\Gamma = 1.9\). The corresponding calculated results using (8), (14), (16), and (18) are plotted using markers at \(f_R\) or dashed lines across frequencies or \(T_d\).

C. Switch Parasitic

Switch on-resistance has been modeled as \(R_{ON}\) as in Fig. 1. It introduces excess loss through the resistive division term \(R_0/(R_0 + R_{ON})\) in (1). While a small \(R_{ON}\) reduces this loss, an overly small on-resistance results in large transistor size, and hence, not only power-hungry clock buffers but also additional shunting parasitic capacitance. Switch shunting parasitic capacitance introduces extra loss and frequency shift.

We model switch parasitic capacitance as a shunting capacitance \(C_p\), as shown in Fig. 12. Similar to that in an N-path filter circuit [31], \(C_p\) causes the peak of magnitude response to shifting toward lower frequencies due to harmonic effects. We expect the amount of frequency shifts depends on the commutation frequency \(f_c\) as \(f_c\) determines harmonic frequencies. \(C_p\) also introduces additional losses as the parasitic
capacitance shunts harmonic signals to ground [32]. As in Fig. 13, compared with the design example shown in Fig. 11 with purely resistive source impedance, adding a $C_P$ of 0.6 pF, which corresponds to the extracted switch parasitic capacitance in our implementation as discussed in Section IV, causes the peak to shift from 5 to 4.2 GHz and additional loss of 1 dB.

An additional inductor $L_W$ may be introduced to resonate with $C_P$. However, unlike in an LTI network, the shunting effect of $C_P$ in an LPTV circuit includes signals across multiple harmonic frequencies [32]. Since an inductor can only resonate with $C_P$ at one frequency, the shunting effect remains at other harmonic frequencies. Therefore, the performance can be only marginally improved when including an inductor $L_W$. As seen in Fig. 13, adding an inductor $L_W$ slightly changes the peak frequency and the in-band loss. Noted that it has been shown in [31] that the introduction of the additional inductor can restore the peak frequency to $f_R$. However, the $N$-path mixers and filters studied in [31] operate in the large-time-constant regime with a small $\Gamma$; in the frequency domain, a small $\Gamma$ means that the passband bandwidth is much smaller compared with the commutation frequency. Analysis of the effect of source inductance on commutated-$LC$ broadband delay with a moderate $\Gamma$, i.e., when passband bandwidth is significantly larger than the commutation frequency, could be an interesting future research topic.

Given the noticeable peak-frequency shift due to switch parasitic capacitance $C_P$, a natural question arises is that up to what frequency can the parasitic-capacitance-free analyses in Sections III-A and III-B provide useful insights? Similar to [32] that studies small-$\Gamma$ passive mixers, we define a cutoff frequency $\omega_T$ for our moderate-$\Gamma$ commutated-$LC$ broadband delay circuit. We assume that the RF-port parasitic capacitance can be ignored for simplicity if RF is below $\omega_T$ given as

$$\omega_T = \frac{1}{\left(\frac{R_0}{2C_P}\right)} = \frac{1}{\left(\frac{N}{2R_{ON}}\frac{R_0}{\tau_{SW}}\right)} \quad (19)$$

where $C_P = NC_{SW}$, $C_{SW}$ is the parasitic capacitance for each switch, $N$ is the number of paths, and $\tau_{SW} = R_{ON}C_{SW}$ is a technology constant that reduces with CMOS scaling. $\omega_T$ defines the frequency beyond which the delay loses more signal to parasitic capacitance $C_P$ than it passes the commutating switches. We have assumed that the input impedance looking into the delay circuit from $C_P$ is $R_0$. This input impedance $R_0$ is in shunt with source resistance $R_0$, resulting in the factor of $1/2$ in (19). Given a $\tau_{SW}$ of 375 fs in 65-nm CMOS, $N = 8$, $R_0 = 50$ ohm, and $R_{ON} = 5$ ohm, the cutoff frequency is calculated as 10 GHz based on (19).

The $C_P$-induced frequency shift can be compensated by adjusting LC resonance frequency $f_R$. As our simulation shown in Fig. 14, in the presence of $C_P$ (no $L_W$), the peak-frequency can be restored to 5 GHz by reducing inductance or increasing $f_R = 1/(2\pi \sqrt{LC})$ to 6 GHz. Capacitance remains nearly the same for a fixed $\Gamma$. The added loss is dominated by the inductor as its parallel resistance $R_L = Q_L(L/C)^{1/2}$ reduces and shunts away more signal power with a smaller $L$.

### D. Clock Overlap

Similar to $N$-path filters and mixer-first receivers [32], [33], our proposed commutated-$LC$ delay circuit is prone to clock overlaps. Clock overlaps increase insertion loss and reduce delay spread. The loss increase and S11/S22 degradation due to overlaps have been studied within the context of mixer-first receivers and N-path filters [33]. The overlaps can be modeled...
Fig. 15. Simulation results of the commutated-LC circuit with clock overlaps using the same design parameters as those in Fig. 11. Clock overlaps of \( \Delta D = 1.8\% \) increase insertion loss and reduce delay spread.

as an additional shunting impedance in an LTI model [32].

Given a normalized clock overlap \( \Delta D \) (see Fig. 12), the change in the maximum and minimum achievable delays can be expressed as

\[
\Delta \tau_{\text{delay,max}} = -\Delta D \cdot T_C, \quad \Delta \tau_{\text{delay,min}} = \Delta D \cdot T_C.
\]

From (20), we see that the delay spread is changed by \( \Delta \tau_{\text{delay,max}} - \Delta \tau_{\text{delay,min}} = -2\Delta D \cdot T_C \), while the sum of delays in both directions remains the same as \( \Delta \tau_{\text{delay,max}} + \Delta \tau_{\text{delay,min}} = 0 \).

Simulation results of the commutated-LC circuit with clock overlaps are shown in Fig. 15, using the same design parameters as those in Fig. 11. When configured in the maximum delay setting \( T_d = 7/8T_C \), clock overlaps result in direct feed-through from the input to the output, causing significant ripples in delay line frequency responses and unexpected delay reduction. After modifying the maximum delay with \( \Delta \tau_{\text{delay,max}} \), i.e., using \( T_d = (7/8 - \Delta D)T_C \), the large ripples disappear and the delay restores to the expected value. Besides reducing delay spread by \( 2\Delta D \cdot T_C \), the overlaps lead to 4-dB higher loss. Small rise, fall time, and duty-cycle control [34], [35] may be used to reduce the clock overlaps.

E. Summary

The \( N \)-path commutated-LC circuit in Fig. 1 acts as a broadband delay when \( \Gamma \approx \pi/2 \). The damping factor \( \alpha \) given in (2) is designed to be much smaller than the resonance frequency \( \omega_R \) for a large delay spread as in (9).

Considering inductor losses and assuming the entire commutated-LC circuit has no memory component except for its \( RLC \) loads and its clocks have no overlap as in Fig. 1, the generalized transfer functions are given in (18). The in-band noise factors in both directions are \( F_{21} \approx G_{21}^{-1} \) and \( F_{12} \approx G_{12}^{-1} \), where \( G_{21} \) and \( G_{12} \) are given in (16) and (17), respectively.

The signal-path delay can be approximated by (8). Finally, the delay line bandwidth is given in (7), while the maximum and minimum achievable delays are calculated using (9).

IV. IMPLEMENTATION DETAILS

We devised a proof-of-concept commutated-LC broadband RF delay circuit in a standard 65-nm CMOS process. The schematics are shown in Figs. 16 and 17.

Transistor parasitic resistance and capacitance result in additional loss and cause a frequency downshift in the delay circuit transfer function. We have defined a cutoff frequency in (19) for our commutated-LC broadband delay circuit below which the RF-port switch parasitic capacitance may be ignored for simplicity.

As discussed in Section III-D, clock overlaps increase insertion loss and reduce delay spread by \( 2\Delta D \cdot T_C \), where \( \Delta D \) is the normalized clock overlap.

As discussed in Section III-D, clock overlaps increase insertion loss and reduce delay spread by \( 2\Delta D \cdot T_C \), where \( \Delta D \) is the normalized clock overlap.
comes with the expense of halving the maximum achievable delay. Intuitively, this is because each LC tank connects to the source or loads twice as frequently as it does in the single-ended implementation. For example, the first LC tank in the single-ended implementation (see Fig. 1) connects to the source only when sw1,F is on; in the differential version (see Fig. 16), the first LC tank sees the source when either sw1,F or sw5,F is on. This effectively doubles the switching frequency or halves TC, and hence, halves the maximum achievable delay based on (9). Thus, the expected maximum delay-bandwidth product is reduced from 4 to around 2 but it is still nearly seven times larger compared with that in an N-path-filter-based delay line.

Delay line switches are realized using nMOS transistors that are designed to have an on-resistance of 5 Ω, as shown in Fig. 16. While having a smaller R(on) leads to a lower loss and noise figure, it comes with a larger switch size that introduces additional harmonic losses [32] and requires higher clock path dc power.

The inductor is realized using the top thick metal and has an electromagnetic-simulated inductance of 684 pH and a quality factor of 12 at 5 GHz. This corresponds to an inductor equivalent shunt resistance R(L) of 260 Ω. A metal–insulator–metal (MIM) capacitor is used at each LC tank and has a capacitance of 1.5 pF to resonate with the inductor at 5 GHz.

Two on-chip eight-phase clock or LO generation circuits, akin to that used in [36], produce 12.5% non-overlapping pulses which drive the input- and output-side switches, respectively. Each LO generator has a differential input at four times the commutation frequency 4 × fc (see Fig. 16). As in Fig. 17, each input port has a 50-Ω interface and an inverter chain that converts the input sinusoid into a 50% duty-cycle clock. Then, a four-stage differential Johnson counter using the high-speed latch in [37] acts as a divide-by-4 frequency divider, generating eight-phase 50% clocks at fc. Finally, each 12.5% non-overlapping LO pulse is generated using a NOR gate and an AND gate from two of the eight-phase 50% clocks and one further buffered input clock.

The clock path delay is generated off-chip in our proof-of-concept prototype but it can be implemented on-chip (e.g., [29], [38]). In [38], a digitally controlled delay with a resolution of 1 ps has been demonstrated.

V. EXPERIMENTAL RESULTS

The proposed commutated-LC broadband RF delay circuit has been fabricated in a 65-nm CMOS process. Annotated chip photograph is shown in Fig. 18. Annotated chip photograph is shown in Fig. 18 with a core area of 1.2 mm².

The chip is assembled in a 4-mm 20-pin quad-flat-flat-no-Lead (QFN) package and mounted on an FR4 printed-circuit board. Measurement results in this article are referred to as the QFN package input and output.

Given the all-passive implementation, the delay line signal path draws zero dc power. The two CMOS-logic-based LO generation circuits together have a dc power of 26 mW from a 1.2-V supply when fc = 250 MHz.

A. Fixed Commutation Frequency fc

With a fixed commutation frequency fc = 250 MHz, Γ can be calculated as Γ = 1/N/4fc/(2R(L)||R(C) ≈ π/2, and the measured delay line S-parameters in forward and backward directions are plotted in Fig. 19(a) and (b), respectively, across different LO-path delay Td between the maximum and minimum achievable delays.

In both directions, the delay line frequency responses are centered around 4.3 GHz. This is lower than the 5-GHz LC resonance frequency due to the parasitic effects that we discussed in Section III-C. The delay line here is a proof-of-concept demonstration of broadband long delays beyond 3-GHz RF and is not designed for any specific wireless standard. When used in a specific wireless system, the delay line center frequency can be adjusted by changing the LC resonance frequency fr as detailed in Section III.

The measured 3-dB transmission bandwidth is 1.3 GHz from 3.6 to 4.9 GHz, so is the −10-dB reflection bandwidth. As expected, this bandwidth is between 8 × fc = 2 GHz and 4 × fc = 1 GHz based on (7). The average in-band transmission group delay varies from 0.5 to 1.35 ns, resulting in a maximum delay-bandwidth product of 1.8. The measured delay spread of 0.85 ns is smaller compared with our expectation which can be calculated using (9) as 1/4Tc = 1 ns. As we discussed in Section III-C, LO overlaps result in this reduced delay spread. Based on (20), a normalized clock overlap of 1.9% could reduce the 1-ns delay spread to 0.85 ns in our measurement.

The measured transmission loss is 10 dB with 0.5 ns delay and is increased to 23 dB when delay becomes 1.35 ns. The loss difference between 0.5- and 1.35-ns delays can be calculated based on (16) as e−αΔTd = 12 dB, showing a good matching with that in measurement.
Fig. 19. Measured delay line $S$-parameters in (a) forward and (b) backward directions with $f_c = 250$ MHz across different LO-path delay $T_d$ between the maximum and minimum achievable delays. Sum of the measured transmission magnitudes and delays in both directions are plotted in part (c).

Fig. 20. Measured delay line in-band delay variation and normalized variation across in-band average group delays.

Based on our discussion in Sections III and IV, regardless of the $T_d$ setting, the sum of transmission in both directions should be a constant and the sum of their group delay should be close to and slightly smaller than $T_c/2 \approx 2$ ns. The plots in Fig. 19(c) validate our theory. In addition, the simulated results are plotted in dashed lines.

Measured delay line in-band delay variation and normalized variation across in-band average group delays are plotted in Fig. 20. Given a $T_d$ setting, the delay variation is calculated as the absolute difference between the maximum or minimum in-band delay and the average in-band delay. Dividing the delay variation with the corresponding in-band average group delay gives us the normalized delay variation. The measured variation here is similar to those in a switched-capacitor broadband delay circuit (e.g., [1]).

B. Varying Commutation Frequency $f_c$

Measured delay line $S$-parameters with varying $f_c$ are plotted in Fig. 21.

As shown in Fig. 21(a), when $f_c = 400$ MHz, the 3-dB transmission bandwidth is about 1.9 GHz from 3.1 to 5 GHz across all measured $T_d$ settings. The measured average in-band delay is from 0.28 to 0.9 ns. Compared with those obtained using $f_c = 250$ MHz, the bandwidth and delays are scaled up and down, respectively, by a factor of about 400/250 as expected based on (7), (8), and discussion in Section IV. Similarly, when $f_c = 125$ MHz, we expect the bandwidth and delays are scaled up and down, respectively, by 125/250. As shown in Fig. 21(b), the measured bandwidth of 0.7 GHz (3.8 to 4.5 GHz) and delay of 0.55 to 2.15 ns meet our expectations.

To further illustrate the impact of varying $f_c$ on delay line performance, the sum of the measured two-direction transmission magnitudes and group delays are plotted in Fig. 21 (c) and (d), respectively. As we can see, the bandwidth increases with $f_c$, while the delay reduces, maintaining a two-direction delay-bandwidth product of around 2.4 (2.2 to 2.5).

The measured delay line in-band noise figures at 4-GHz RF across $T_d$ and $f_c$ are plotted in Fig. 22. When using the same $T_d$ and $f_c$, the noise figure is almost identical to the insertion loss, as we discussed in Section III-B.

C. Spurious Tones

As shown in Fig. 23, the spurious tones responses of the proposed commutated-LC broadband delay circuit are measured with a $-18$-dBm sinusoidal input at $f_S = 4$ GHz. The delay line is clocked at $f_c = 250$ MHz, and the measurements are performed with $T_d \approx 0.5$ and 1.4 ns.

In each case, we see that the 4-GHz output has an expected strength based on the measured $S$-parameters in Fig. 19. Across a wide frequency range of 0.1 to 6.5 GHz, the strongest spurious tones are located at $f_S \pm N f_c$ which are 10-to-16-dB lower compared with the desired output at $f_S$. These spurious tones at $f_S \pm N f_c$ are due to the time-interleaved sampling operation of the delay line with a sampling frequency of $N f_c$, as we discussed in Section III. Finally, it should be noted that these spurious tones at $f_S \pm N f_c$ are outside of the delay line bandwidth (3.6–4.9 GHz), and hence, can be filtered later.

Similar to switched-capacitor circuits (e.g., [1], [20]), the imperfection of LO signals leads to some in-band spurious...
Fig. 21. Measured delay line S-parameters with varying $f_C$: (a) $f_C = 400$ MHz, (b) $f_C = 125$ MHz, and sum of the measured two-direction transmission (c) magnitudes and (d) group delays. Simulation results are plotted in dashed lines.

Fig. 22. Measured in-band noise figure across $T_d$ and $f_C$.

Fig. 23. Measured spurious tones responses with a $-18$-dBm sinusoidal input at $f_S = 4$ GHz; the delay line is clocked at $f_C = 250$ MHz.

Fig. 24. Measured linearity performance when the delay line is clocked at $f_C = 250$ MHz with the testing input signal at around 4 GHz.

E. Performance Summary and Comparison

A summary of our measurement results is given in Table I together with those from state-of-the-art integrated RF delay line designs. They are divided into three categories—active LTI, passive LTI, and passive LPTV.

Compared with the LPTV switched-capacitor-based RF and BB delay lines, the proposed commutated-LC delay line has a much wider instantaneous RF bandwidth and operates at a center frequency that is more than ten times higher. This is achieved by introducing inductors to the LPTV operation. The utilization of inductors leads to noticeable increases in chip area and noise figure (or power loss) when normalized to the delay. Developments of low-loss and compact commutated-LC broadband delay circuits could be important future research topics for large antenna arrays and self-interference cancellation that have a stringent loss and area constraints.

However, given the same delay, the commutated-LC delay has orders-of-magnitude lower normalized loss or noise and a much smaller area per delay compared with fully passive LTI RF delay lines ([7], [8]) that also uses inductors. This is due to the elimination of signal-path delay tuning and non-reciprocal delay operation. When implemented using similar CMOS technology, the reconfigurable passive LTI RF delay lines handle stronger signals as their static switches are
TABLE I
MEASUREMENT SUMMARY AND COMPARISON WITH STATE-OF-THE-ART INTEGRATED RF DELAY LINES

| Architecture | JSSC 2015 [10] | JSSC 2017 [11] | SSCL 2020 | TMT 2019 [9] | TMT 2020 [7] | ESSCIRC 2021 [16] | SSLC 2020 [17] | TMT 2020 [18] | JSSC 2021 [19] | This work |
|--------------|----------------|----------------|----------|-------------|-------------|----------------|-------------|-------------|-----------|----------|
| Frequency Range (GHz) | 1 to 2.5 | 0.1 to 2 | 6.5 to 9 | 8 to 18 | 3 to 30 | dc to 0.8 | dc to 0.5 | dc to 0.5 | 0.1 to 0.5 | dc to 0.19 |
| dBm Instant. BW (GHz) | 15 | 1.9 | 3.5 | 3.5 | 7 | 0.8 | 0.5 | 0.4 | 0.19 |
| Fractional BW | 86% | 180% | 47% | 19% to 44% | 23% to 200% | 200% | 200% | 133% | 200% |
| Max. Delay (ns) | 0.55 | 1.7 | 0.8 | 0.13 | 0.07 | 3.8* | 1* | 2 | 11 |
| Delay Tuning Method | Signal-Path Tuning | Signal-Path Tuning | Signal-Path Tuning | Signal-Path Tuning | LO-Path Tuning | LO-Path Tuning | LO-Path Tuning | LO-Path Tuning | LO-Path Tuning |
| Delay Variation | 1.8% (10 ps) | 8.3% (140 ps) | 1.7% (14 ps) | 21% (27 ps) | 3% to 42% (3 ps) | N.R. | N.R. | 1% (14 ps) | 2% to 4% (250 ps) |
| NF at max. delay (dB) | 8 | 23 | 4 | 17 | N.R. | N.A. | N.A. | N.R. | 11 |
| Power Loss at max. delay (dB) | N.A. | N.A. | 14 | 17 (8 GHz) | 8 (3 GHz) | N.A. | N.A. | N.R. | 25 |
| IIP3 (dBm) | -13 to -20 | -5 to +5 | N.R. | N.R. | N.R. | N.R. | N.R. | N.R. | +10 |
| IIP3 (dBm) | -21 to -28 | -10 | -17 | N.R. | N.R. | N.R. | 0 | N.R. | +1 |
| Technology | 140-nm CMOS | 130-nm CMOS | 65-nm CMOS | 180-nm CMOS | 28-nm CMOS | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS |
| Area (mm²) | 0.07 | 0.3 | 2.3 | 2 | 0.34 | N.R. | N.R. | N.R. | 0.12 |
| Power, Pdc (mW) | 50 | 112 to 364 | 107 | 0 | 0 | N.R. | N.R. | 10 | N.R. |
| Max. Delay BW in (GHz) | 0.8 | 3.2 | 2.8 | 0.5 | 0.5 | 3 | 0.8 | 2 | 1.8 |
| Chip Area/Delay (mm²/ns) | 1.3 | 0.28 | 2.8 | 15 | 5 | N.R. | N.R. | 0.6 | 0.2 |
| NF/Delay (dB/ns) | 15 | 14 | 5 | 131 (8 GHz) | N.R. | N.A. | N.A. | 9.5 | N.R. |
| Loss/Delay (dBns) | N.A. | N.A. | 18 | 131 (8 GHz) | 116 (3 GHz) | N.A. | N.A. | N.R. | 0.23 |
| IIP3 (dBm) | -36 to -43 | -24 | -22 | N.R. | -110 | N.A. | N.A. | -5.5 | N.R. |

VI. CONCLUSION

We have shown that introducing inductors, essentially adding a new degree of freedom, to an LPTV broadband delay circuit allows it to operate at a much higher frequency with a wider instantaneous bandwidth. We have derived the insertion loss, bandwidth, group delay, and noise performance of a commutated-LC delay circuit, providing various design insights and guidelines. We have devised a 65-nm CMOS proof-of-concept prototype, demonstrating a 1.3-GHz 3-dB bandwidth around a 4.3-GHz RF, 1.4-ns maximum delay, 23-dB loss, and an IIP3 of +16 dBm.

REFERENCES

[1] A. Nagulu, A. Mekkawy, M. Tymchenko, D. Sounas, A. Ali, and H. Krishnaswamy, “Ultra-wideband switched-capacitor delays and circulators—Theory and implementation,” IEEE J. Solid-State Circuits, vol. 56, no. 5, pp. 1412–1424, May 2021.
[2] J. Roderick, H. Krishnaswamy, K. Newton, and H. Hashemi, “Silicon-based ultra-wideband beam-forming,” IEEE J. Solid-State Circuits, vol. 41, no. 8, pp. 1726–1739, Aug. 2006.
[3] M. Li et al., “An 800-ps origami true-time-delay-based CMOS receiver front end for 6.5–9-GHz phased arrays,” IEEE Solid-State Circuits Lett., vol. 3, pp. 382–385, 2020.
[4] A. Nagulu et al., “A full-duplex receiver with true-time-delay cancelers based on switched-capacitor-networks operating beyond the delay–bandwidth limit,” IEEE J. Solid-State Circuits, vol. 56, no. 5, pp. 1398–1411, May 2021.
[5] Y. Cao and J. Zhou, “Integrated self-adaptive and power-scalable wideband interference cancellation for full-duplex MIMO wireless,” IEEE J. Solid-State Circuits, vol. 55, no. 11, pp. 2984–2996, Nov. 2020.
[6] K.-D. Chu, M. Katanbaf, T. Zhang, C. Su, and J. C. Rudell, “A broadband and deep-TX self-interference cancellation technique for full-duplex and frequency-domain-duplex transceiver applications,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2018, pp. 170–172.
[7] M. Jung and B.-W. Min, “A compact 3–30-GHz 68.5-ps CMOS true-time-delay delay for wideband phased array systems,” IEEE Trans. Microw. Theory Techn., vol. 68, no. 12, pp. 5371–5380, Dec. 2020.
[8] M. H. Ghazizadeh and A. Medi, “A 125-ps 8–18-GHz CMOS integrated delay circuit,” IEEE Trans. Microw. Theory Techn., vol. 67, no. 1, pp. 1398–1411, May 2021.
[9] N. Rajesh and S. Pavan, “Design of lumped-component programmable delay elements for ultra-wideband beamforming,” IEEE J. Solid-State Circuits, vol. 49, no. 8, pp. 1800–1814, Aug. 2014.
[10] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, “Compact cascadable g–C all-pass true time delay cell with reduced delay variation over frequency,” IEEE J. Solid-State Circuits, vol. 50, no. 3, pp. 693–703, Mar. 2015.
