Effect of cycling on ultra-thin HfZrO$_4$, ferroelectric synaptic weights

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Abstract

Two-terminal ferroelectric synaptic weights are fabricated on silicon. The active layers consist of a 2 nm thick WO$_3$ film and a 2.7 nm thick HfZrO$_4$ (HZO) film grown by atomic layer deposition. The ultra-thin HZO layer is crystallized in the ferroelectric phase using a millisecond flash at a temperature of only 500 $^{\circ}$C, evidenced by x-rays diffraction and electron microscopy. The current density is increased by four orders of magnitude compared to weights based on a 5 nm thick HZO film. Potentiation and depression (analog resistive switching) is demonstrated using either pulses of constant duration (as short as 20 nanoseconds) and increasing amplitude, or pulses of constant amplitude ($+/-1$ V) and increasing duration. The cycle-to-cycle variation is below 1%. Temperature dependent electrical characterisation is performed on a series of device cycled up to $10^8$ times: they reveal that HZO possess semiconducting properties. The fatigue leads to a decrease, in the high resistive state only, of the conductivity and of the activation energy.

1. Introduction

In artificial neural network accelerators [1, 2], the matrix-vector multiplication, or multiply and accumulate operation, is implemented using analog signals and weights by a parallel accumulation of currents generated across an array of reprogrammable resistances. The use of HfZrO$_4$ (HZO) [3] and more generally HfO$_2$-based ferroelectric compounds [4], receive increasing interest for analog, neuromorphic and in-memory computing. A concept of ferroelectric memristor is based on a ferroelectric layer separating two electrodes of a different material, thin enough to allow electrical conduction and thick enough to stabilize ferroelectricity. The energy profile of the device is modified upon polarization reversal, inducing the remanent modification of the resistance. Such electroresistance effect was first demonstrated using epitaxial ferroelectric perovskites [5–8], and recently using epitaxial thin films of the fluorite HfZrO$_4$ (HZO) [9, 10]. State-of-the-art double-layer polycrystalline HfO$_2$(10 nm)/Al$_2$O$_3$ junctions [11, 12] suffer from non-linear current–voltage characteristic (which can be circumvent by using a logarithmic driver [13]) and a relatively low current density ($\sim1$ $\mu$A cm$^{-2}$ at 2 V).

A direction towards larger current densities and linearity is to thin down the ferroelectric layer. Apart from epitaxial films deposited by pulsed laser deposition [9, 14] or sputtering [15], most films are deposited amorphous e.g. using molecular beam epitaxy [16] or atomic layer deposition (ALD) [3, 4], and subsequently annealed. The crystallisation of ultra-thin films is challenging because of the increased thermal budget required to obtain ferroelectricity as the thickness decreases [17]: using rapid thermal annealing, Liang et al required 600 $^{\circ}$C for 5 nm thick HZO films and Ali et al as much as 800 $^{\circ}$C for 4 nm. In this work, we reduce the thickness of HZO layer to only 2.7 nm, and use a millisecond flash lamp annealing technique, allowing thermalisation at only 500 $^{\circ}$C.
Another limitation of ferroelectric tunnel junctions using a dielectric interlayer is the poor screening of the polarization charges by the later. In this work a transition metal oxide (WO₃) is used instead. At the cost of a reduced On/Off ratio, the 2.7 nm thick HZO layer enables the devices to operate at low bias (<100 mV), in a linear regime, with a large current density of 0.01 A cm⁻² at 100 mV. Such a device operating in the quasiohmic regime was already demonstrated using 5 nm thick HZO films with WO₃ [18] or TiO₂ [19] interlayers: they have the advantage of back-end-of-line compatibility, but the current density was only 1 μA cm⁻² at a read voltage of 100 mV. This work further establishes the depression/potentiation capability of ferroelectric, two-terminals synaptic weights.

2. Ultra-thin HfZrO₄ based devices

The process flow for the fabrication of the synaptic weights is summarized in figure 1(a). A 200 nm thick SiO₂ oxide was grown on Si by thermal oxidation. The active stack was then deposited by plasma-enhanced atomic layer deposition (PE-ALD): 20 nm of TiN is deposited at 300 °C with Tetrakis(dimethylamino)titanium and N₂ as precursors. 2 nm of WO₃ is deposited at 375 °C with (BuN)₂W(NMe₂)₂ and O₂, then 3 nm of HZO is deposited at 300 °C alternating one cycle with Tetrakis(ethylmethylamino) hafnium (IV) and O₂, and two cycles with Bis (methylcyclopentadienyl) (methyl) (methoxy) zirconium (IV) and O₂. Ten additional nanometers of TiN are deposited as a capping layer to promote HZO crystallization in the ferroelectric phase during the annealing [20]. The choice of a stack fully deposited by ALD is motivated by the conformal character of the growth, which opens the door to future 3D integration, towards further reduction of the device footprint. In order to provide HZO with asymmetric interfaces while ensuring a maximal current density, the combination of an ultra-thin metal oxide interlayer and a metallic bottom electrode was preferred to a thick metal oxide electrode. TiO₂ was first studied as a metal oxide interlayer: for 5 nm thick HZO synaptic weights, replacing TiO₂ [19] by WO₃ [18] resulted in a higher On/Off ratio and suppressed the need for a wake-up sequence, indicating that the HZO/metal oxide interface is active on the device characteristics such as On/Off ratio, rather than the bulk of the metal oxide. The crystallization was performed using the millisecond flash lamp annealing technique [21]; the sample was preheated to 500 °C, then a 20 ms long energy pulse of 90 J cm⁻² was applied. The as-grown HZO layer was amorphous [21]. Although 400 °C was sufficient to crystallize 5 nm thick films [18], in this work films flash-annealed at 450 °C did not show any sign of crystallization. The increased temperature required as the thickness decreases was observed by Tahara et al [17] on TiN/HZO/TiN stacks. Thanks to the relatively thin top electrode, it is possible to measure the different layers thicknesses by x-ray reflectivity (HZO was found to be 2.7 nm thick) and to verify the crystallinity of the HZO layer using the grazing incidence x-ray diffraction technique (2θ scan at ω = 0.4°), as shown in figure 1(b). A Bruker D8 Discover diffractometer equipped with a rotating anode generator was used. For comparison, the green lines (resp. purple) correspond to the monoclinic HZO (resp. tetragonal ZrO₂) in Materlik et al [22] and the orange lines to the orthorhombic HZO in Müller et al [23]. The peaks at 2θ = 37° and 43° (CIF 1011102) show that TiN is polycrystalline. No monoclinic HZO is found: the peak observed at 2θ = 30.5° matches the (111) planes of the orthorhombic phase. The peak is broad, which is not attributed to the presence of multiple peaks but to the reduced crystallite size. It is fitted by a Gaussian with a width at half maximum of w = 2.5°. The angle between the incident beam and the surface of the film was ω = 0.4°. Using a k factor of 0.9, the crystallite size (along the direction that is 15° off the surface, approximately in-plane) was estimated using the Scherrer equation [24]:

\[ d = \frac{k \lambda}{2 \cos \theta} \]

as shown in figure 1(b). A Bruker D8 Discover diffractometer equipped with a rotating anode generator was used. For comparison, the green lines (resp. purple) correspond to the monoclinic HZO (resp. tetragonal ZrO₂) in Materlik et al [22] and the orange lines to the orthorhombic HZO in Müller et al [23]. The peaks at 2θ = 37° and 43° (CIF 1011102) show that TiN is polycrystalline. No monoclinic HZO is found: the peak observed at 2θ = 30.5° matches the (111) planes of the orthorhombic phase. The peak is broad, which is not attributed to the presence of multiple peaks but to the reduced crystallite size. It is fitted by a Gaussian with a width at half maximum of w = 2.5°. The angle between the incident beam and the surface of the film was ω = 0.4°. Using a k factor of 0.9, the crystallite size (along the direction that is 15° off the surface, approximately in-plane) was estimated using the Scherrer equation [24]:

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3. Ferroelectric synaptic weights

The analog resistive switching properties of the devices are characterized. Both the programmability of the device for inference and its response under pulses of varying sign, amplitude and width are addressed, emulating—as proposed for example in [26] or [27]—the combination of pre-synaptic pulses (negative bias) and post-synaptic pulses (positive bias). The bottom (TiN/WO$_x$) electrode is grounded.
Prior to each test, the device was set by applying a pulse of 1 V, 1 s followed by a pulse of $-1$ V, 1 s. The measurement scheme is as follows: first, a pulse of amplitude $V_{\text{write}}$ and duration $t_{\text{write}}$ is applied using a B1530A waveform generator/fast measurement unit (WGFMU). The rise and fall time are set to 20 ns. Then, a B1500 analyser high-resolution source measurement unit is used to measure the conductance $G^{\text{PUND}}$ of the device at a read bias of 100 mV. Keeping $t_{\text{write}}$ constant, the write/read operation is repeated with a different $V_{\text{write}}$, as represented in figure 3: the arrows indicate the chronological order.

Electroresistance loops are measured for various $t_{\text{write}}$. The range of the amplitude is adapted in such a way that the saturation of the conductance is observed: it is $+/-2.8$ V for ultra-fast pulses of 20 ns, and $+/-1$ V for long pulses of 2 s. Such dynamics are consistent with the empirical Merz’s law for the switching of ferroelectric domains [28]. Pulses of the same size but with decreasing amplitude allow several micro-amperes to flow through the junction but only slightly modify the resistance (horizontal branches in the hysteresis loops, from 2.8 V to $-0.8$ V), showing that the resistive switching is field- and not current-driven, consistent with a resistive switching mechanism related to the ferroelectric domains switching. The remanent polarisation was measured by the positive up negative down (PUND) method: it is independent of the device area and is $2P_r = 2.25 \, \mu C \, cm^{-2}$ at 500 kHz. This value is significantly lower than what is typically observed for 10 nm thick HZO (16 $\mu C \, cm^{-2}$ [3]), and compares with the values measured by Chernikova et al in 2.5 nm thick films on TiN (2.5–3.5 $\mu C \, cm^{-2}$ [29]). The small polarization in our films is not due to the presence of monoclinic grains (figure 1(b)). The presence of tetragonal grains in ultra-thin HZO films is typically associated (an effect more pronounced in ultra-thin films), typically responsible for a diminution of the ferroelectric polarization due to a finite screening length in the electrodes [31]. The presence of grains oriented along the [634] directions, discussed earlier, also contribute to the small polarization: in these grains, the projection of the polarization (which is parallel to the c-axis of the Ptn21 unit cell) [22] along the normal to the surface is only 53% of its norm.

The proposed devices are energy efficient: 20 ns long pulses allow to update the synaptic weight with an energy in the pico-Joule range. The ‘reading’ operation at 100 mV would dissipates less than a femto-Joule for a reading time of the order of the micro-second.

Potentiation and depression is also obtained by keeping the amplitude $V_{\text{write}}$ constant ($V_{\text{write}} = 1$ V for the depression and $V_{\text{write}} = -1$ V for the potentiation) and increasing duration $t_{\text{write}}$ (upper panel of figures 4(a) and (b)). Figure 3(a) shows the normalised conductance $G$ of the device measured at 0.1 V (blue data points) and at $-0.1$ V (yellow data points) after each pulse of duration $t_{\text{write}}$. The sequence $G^{+100mV}$ is larger than $G^{100mV}$ by a factor 2.5–2.7 due to a moderate diode-like character in the current–voltage characteristics. Two regimes are observed: below 10 $\mu s$, the conductance varies linearly with 10 to the power of $t_{\text{write}}$ and 20% of the dynamic range is covered by the first pulse (20 ns). Above 10 $\mu s$, the dependence is slower, which could involve effects other that ferroelectric domains switching such as reversible charged defects migration within.

Figure 3. (a) Potentiation/depression cycles (40 $\mu$m device). The data is normalized to the [0; 1] range. Prior the test, the device is reset/set by applying a pulse of 1 V, 1 s followed by a pulse of $-1$ V, 1 s. After each pulse of amplitude $V_{\text{write}} = 1$ V (depression) or $V_{\text{write}} = -1$ V (potentiation) and increasing duration $t_{\text{write}}$ (upper panel, from 20 ns to 1 s), the conductance of the synaptic weight is measured at 100 mV (blue data points) and then at $-100$ mV (yellow data points). The first to tenth cycles of the measured data are found in (b), where the green curve represents the resistance $R^{+100mV}$ measured at 100 mV for pulses 1 to 120, and the red curve for 1081 to 1200. The blue data points (right axis) indicate the normalized standard deviation of $R^{+100mV}$ over the ten cycles.
the layers. In figure 3(b), the resistance measured at 100 mV, \( R^{+100mV} = 1/G^{+100mV} \) is represented as a function of the relative pulse number (green curve: first cycle, red curve: tenth cycle). In this representation the two regimes are also visible. For each pulse number, the normalised standard deviation (independently calculated from the conductance or from the resistance), or cycle-to-cycle variation, was measured: it is maximal after the first pulse where it is as low as 0.6%.

4. Effect of fatigue and temperature

Four devices are cycled respectively \( 10^5, 10^6, 10^7 \) and \( 10^8 \) times at +/- 1 V, at a frequency of 100 kHz. Temperature dependent measurements are carried out on these four devices in addition to one in the pristine state. The five devices are in different fatigue states. After setting the temperature, the chip is thermalised for 15 min. The device is first set in the LRS by a DC sweep from 0 to -1 V, then a non-switching \( I-V \) sweep is performed from 0 to 80 mV. The current density \( J^+ \) as a function of the voltage \( V^+ \) (for the device with \( 10^2 \) cycles) is represented by the circles in figure 5(a). The device is then set in the HRS (DC sweep from 0 to 1 V) and measured (diamonds in figure 5(a)). In a first approximation, the transport for a positive bias on the top electrode is Ohmic. It is described by [32]:

\[
\log(J) = \log\left(\frac{\mu q N_C}{T}\right) + \frac{-(E_C - E_F)}{kT} \times \frac{1}{T} + \log(V)
\]

\[J = \sigma E = \mu q N_C \exp\left(-\frac{(E_C - E_F)}{kT}\right) E_t \tag{1}\]

where \( \mu \) the electron mobility, \( q \) the electronic charge, \( N_C \) the carrier concentration at equilibrium, \( E_C - E_F \) the energy difference between the conduction band and the Fermi level, \( k \) the Boltzmann constant, \( T \) the absolute temperature. WO\(_{x}\)<3 is a n-type semiconductor, the transport is metallic for \( x < 2.9 \) [33]. The stoichiometry of the WO\(_x\) layer is not known. The scavenging of oxygen from WO\(_x\) by HZO during the annealing confers metallic properties to WO\(_x\) and will be further discussed elsewhere. In this work, the LRS is obtained after aligning the ferroelectric polarisation towards the WO\(_x\) layer, i.e. when carriers are not accumulated, but depleted in the later. This was already observed for WO\(_x\) (3 nm)/HZO (5 nm) devices fabricated in similar conditions [18], where we showed that the resistive switching occurred within the HZO layer, the WO\(_x\) layer being considered as a metal.

In this work, the electric field is assumed to drop mainly across the ferroelectric layer (i.e., the thickness \( t \) is assumed to be the thickness of HZO, 2.7 nm). For each temperature, the experimental data is fitted in the \( \log(J^+) - \log(V^+) \) representation by a linear regression (solid lines). Figure 5(b) shows the Arrhenius plot of the intercepts of the linear regressions from figure 5(a) (blue data points: LRS, red data points: HRS), as a function of the inverse of the temperature. Again, two linear regressions are performed (solid lines). Using equation (1), the product \( \mu N_C \) (assumed independent of the temperature [34]) and \( E_C - E_F \) in the LRS and the HRS can then be estimated. The same analysis is performed for the five devices with varying fatigue states. Independently on the number of cycles, the On/Off ratio, calculated from the difference of the intercepts of the linear regressions in figure 5(a), decreases with temperature (figure 5(c)). For a given temperature, a decrease of the On/Off ratio is observed for the most fatigued device (red curve), along with a decrease of the resistance in the HRS by 20%, compared to the pristine device (green curve). \( E_C - E_F \) (squares and circles, left axis) and \( \mu N_C \) (diamonds and pentagons, right axis) parameters are measured in the LRS (blue symbols) and the HRS (red symbols) for different number of cycles. They do not capture an eventual gradient within the HZO layer. In the LRS, \( E_C - E_F \) is independent from the fatigue, and equal to 0.28 eV. In the HRS, it is 0.33 eV in the pristine

Figure 4. Conductance measured at 0.1 V after each pulse of duration \( t_{\text{write}} \) and amplitude \( V_{\text{write}} \). The arrows indicate the chronological occurrence.
state, value which decreases gradually with fatigue towards 0.30 eV. These values are relatively small compared to the HZO band gap, which indicate the presence of donor states. The change in $E_C - E_F$ upon switching could be explained by a redistribution of such states, leading to a larger gap in the HRS than in the LRS. Similarly, the product $\mu N_C$ is independent from the fatigue in the LRS. In the HRS, the product decreases from $5.5$ to $2.8 \times 10^{16}$ (cm V s)$^{-1}$ with fatigue, supporting the scenario of electrostatic redistribution of carriers in the HZO as the polarization switches. Such mechanisms can be driven by the self-screening of the polarization charges, as already seen in semiconducting ferroelectrics [35, 36].

5. Conclusion

Ferroelectric synaptic weights were fabricated based on an ultra-thin (2.7 nm) HZO layer. The crystallization using the millisecond flash-lamp annealing requires a thermal budget of only 500 °C, several hundreds of degrees lower than what is required with the conventional rapid thermal annealing technique. Compared to state-of-the-art 5 nm thick HZO devices, the current density is increased by $10^4$. Analog resistive switching is obtained using 20 ns long pulses of increasing amplitude, as well as using $+/−1$ V pulses of increasing duration. Despite the reduced On/Off compared to devices fabricated with thicker HZO, the stochasticity is very small with a cycle-to-cycle variation below 1%. The synaptic weights are thus good candidates in circuits with low requirements on the dynamic range such as circuits based on differential pairs (see for example [37–39]). The devices have a good endurance, with a limited degradation of the functionality after $10^8$ full switching cycles. The analysis of the temperature dependent current–voltage characteristics reveals that HZO can be described as a semi-conductor. As the devices are cycled, the energy difference between the conduction band and the Fermi level, as well as the mobility-carrier density product, decrease. The decay is observed only in the high resistive state, resulting in a reduction of the On/Off ratio upon cycling.

Part of this work was presented at ESSCIRC 2021, see [40].
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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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