Room-Temperature Quantum Ballistic Transport in Monolithic Ultrascaled Al–Ge–Al Nanowire Heterostructures

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Supporting Information

ABSTRACT: Conductance quantization at room temperature is a key requirement for the utilizing of ballistic transport for, e.g., high-performance, low-power dissipating transistors operating at the upper limit of “on”-state conductance or multivalued logic gates. So far, investigating conductance quantization has been restricted to high-mobility materials at ultralow temperatures and requires sophisticated nanostructure formation techniques and precise lithography for contact formation. Utilizing a thermally induced exchange reaction between single-crystalline Ge nanowires and Al pads, we achieved monolithic Al–Ge–Al NW heterostructures with ultrasmall Ge segments contacted by self-aligned quasi one-dimensional crystalline Al leads. By integration in electrostatically modulated back-gated field-effect transistors, we demonstrate the first experimental observation of room temperature quantum ballistic transport in Ge, favorable for integration in complementary metal–oxide–semiconductor platform technology.

KEYWORDS: Ballistic transport, germanium, nanowire, heterostructure, aluminum

After decades, following Moore’s law† by continuously shrinking feature sizes of classical planar metal-oxide-semiconductor field-effect transistors (FETs), physical limitations and the dramatic repercussions of short-channel effects‡ have forced a shift of research efforts toward the integration of new materials, novel processing techniques, and ultrascaled device architectures.‡ Owing to miniaturization in engineering systems as well as increasing interest in fundamental research in accompanying quantum confinement effects and ballistic transport, quasi-one-dimensional nanostructures, such as semiconductor nanowires (NWs), gain particular interest.§ As the minimum feature size approaches the bulk electron mean free path, novel physics due to the confinement of electrons and phonons may pave the way for future high-performance, nanoelectronic devices.‡ Although room temperature ballistic transport was demonstrated in constricted two-dimensional electron gases of high-mobility materials,§ forming quantum point contacts, ballistic transport in NWs was restricted to high magnetic fields (>4 T) and ultralow temperatures.** Motivated by the relevance of ballistic transport for multivalued logic gates,† quantum computing,‡,§,‖ and, recently, the realization of topological superconductivity or Majorana Fermions,‡‡‡,‡‡§ ballistic transport observed in Si–Ge core–shell NWs,‡‡,‡‡§‡‡ triggered further research activities on group IV NWs favorable for complementary metal–oxide–semiconductor (CMOS) process integration. In particular, Ge NWs represent a unique quasi-1D system for exploring quantum coherence phenomena because of the high hole mobility,‡‡§ and an exciton Bohr radius of aGe = 24.3 nm,‡‡§ approximately five times larger than that of Si (aSi ≈ 4.9 nm), leveraging strong quantum confinement effects.‡‡‡ In addition, compared to III–V materials in which hyperfine coupling limits the electron-spin coherence, the prospect of long coherence times in group IV semiconductors with spin-zero nuclei has stimulated a lot of experimental effort also for spin-based quantum information applications.‡‡§ Despite the above-mentioned beneficial properties of Ge to the study of quantum confinement effects,‡‡§ ballistic transport was not observed for temperatures above T = 2 K,‡‡§ which is also attributed to precise nanopatterning and contact-formation issues. Furthermore, in these quasi-1D structures, surface states create inhomogeneities in the local electrostatic environment, increasing the probability of electron reflections and backscattering.

In this letter, we demonstrate for the first time room temperature quantum ballistic transport in ultrascaled Ge NWs with diameters comparable to the Bohr radius of Ge of aGe = 24.3 nm. Therefore, monolithic Al–Ge–Al NW heterostructures with ultrashort Ge segments are integrated in a back-gated FET architecture (Figure 1a) accomplished by a novel...
The necessity of the high-intrinsic VLS-grown Ge NWs were used, negative surface and reproducible electrical performance of the device. Although comparison of the transfer characteristics of Al2O3 passivated and unpassivated Al–Ge–Al NW heterostructures integrated in the FET with respective hysteresis effects. The data were recorded for back-gated FET devices with Ge segment lengths of \( L_{Ge} = 150 \) nm in the gate-voltage range between \( V_G = -15 \) V and \( V_G = +15 \) V for a bias of \( V_D = 10 \) mV at \( T = 300 \) K. The left inset shows the time dependence of the drain current \( I_D \) for the passivated Al–Ge–Al NW heterostructure device \( (L_{Ge} = 150 \) nm) for \( V_G = -15 \) V and a bias of \( V_D = 10 \) mV at \( T = 300 \) K. A comparison of the \( I/V \) characteristic for a passivated (red) and an unpassivated (black) device with a channel length of \( L_{Ge} = 77 \) nm at \( V_G = 0 \) V is provided in the right inset. To exclude the influence of adsorbates on the NW surface, all measurements were performed in a vacuum.

Figure 1. (a) Schematic illustration of the Al–Ge–Al NW heterostructure with self-aligned c-Al leads integrated in a back-gated FET device. The SEM image shows an Al–Ge–Al NW heterostructure with a Ge segment length of \( L_{Ge} = 30 \) nm. A magnified view showing the abrupt metal–semiconductor interface between the quasi one-dimensional c-Al leads and the Ge segment is provided by the TEM image in the inset. (b) A comparison of the transfer characteristics of Al2O3 passivated and unpassivated Al–Ge–Al NW heterostructures integrated in the FET with respective hysteresis effects. In agreement with previous reports, 35,36 using a high-k passivation layer results in less pronounced hysteresis effects. In addition, the ON-current and the \( I_{ON}/I_{OFF} \) ratio of the passivated FET increases by more than two orders of magnitude. However, even the passivated device shows a small hysteresis due to kinetic effects, mostly related to charge-carrier trapping at the interface, and the devices exhibit transient behavior, as shown in the left inset of Figure 1b. For a negative gate voltage of \( V_G = -15 \) V, the accumulation of holes continuously neutralizes trapped electrons, resulting in an exponential decay of the drain current over time. 30 In accordance with Zhang et al., 37 we assume that during atomic layer deposition, a thin GeOx layer is formed at the interface between the Ge NW and the Al2O3 passivation. Dedicated to a multieponential time dependence, indicating a significant spread in the spatial and energetic distribution of the surface trap states as well as kinetic limitation by either a diffusion barrier or a tunnel barrier at the NW surface, the charging and discharging of trapped surface states are relatively slow processes. 30 Therefore, for the actual device geometry and under the given experimental conditions, steady state is achieved after a time span of approximately 1 h, which has to be taken into account to achieve reliable ballistic transport measurements.

Furthermore, as shown in the right inset, a combination of conformal high-k passivation and control of the trap population allows the effective tuning of the electronic transport characteristic of the back-gated Ge NW device. Whereas the devices with uncoated Al–Ge–Al NW heterostructures
Figure 2. (a) I/Vs of passivated Al–Ge–Al NW heterostructures with different Ge segment lengths integrated in back gated FET devices for \( V_G = 0 \) V at ambient conditions and (b) thereof calculated resistance as a function of Ge segment length normalized with respect to the cross-section of the NWs. The enlarged view depicts the resistance of the heterostructure devices with a Ge segment length smaller than \( L_{Ge} = 100 \) nm.

Figure 3. (a) Schematic illustration of the 1D dispersion relation \( E(k) \) and the corresponding density of states \( D(E) \) of an Al–Ge–Al NW heterostructure with thin Ge NWs. The Fermi level as well as the expected \( G-V_G \) characteristic for NWs with filled and depleted surface traps are sketched. (b) Time-dependent \( G-V_G \) behavior for Al–Ge–Al NW heterostructure devices with Ge segment lengths of \( L_{Ge} = 15 \) nm (blue), \( 45 \) nm (green), and \( 150 \) nm (red) at ambient conditions. The upper left inset shows the \( G-V_G \) characteristics recorded for different trap-filling levels of an Al–Ge–Al NW heterostructure device with a \( 15 \) nm long Ge segment for \( V_G = -15 \) V. Fast \( G-V_G \) measurements were performed after the time intervals given in the inset. The upper right inset shows the experimental \( G-V_G \) behavior of Al–Ge–Al NW heterostructures with varying Ge segment lengths with depleted traps. All measurement data were recorded for a bias of \( V_G = 1 \) mV at \( T = 300 \) K in vacuum. The conductance was directly obtained from the measured current \( G = I_D/V_D \). The lower inset schematically depicts the discharging of traps due to an accumulation of holes at negative \( V_G \).

provoke a distinct nonlinear \( I/V \) characteristic, the ohmic behavior and higher conductivity for the passivated devices after trap depletion indicates improved contact properties enabling effective carrier injection (see the Supporting Information).

Two-terminal \( I/V \) measurements of passivated Al–Ge–Al NW heterostructure devices with different Ge segment lengths, shown in Figure 2a, revealed a clear transition from a nonlinear behavior to an almost linear characteristic for devices with channel lengths below \( L_{Ge} = 45 \) nm.

Essentially, one may assume that devices with Ge segment lengths of \( L_{Ge} > 45 \) nm operate as back-gated Schottky barrier FETs, with \( I_D \propto \exp(eV/kT) \) due to two back-to-back Schottky contacts, which is commonly addressed to explain nonlinear \( I/V \) curves of semiconductor NW devices.\(^{38}\)

Figure 2b shows further that the thereof calculated overall resistance of longer devices is directly proportional to the Ge segment length in accordance with Ohm’s law. In contrast, heterostructure devices with Ge segment lengths below \( L_{Ge} = 45 \) nm reveal a linear \( I/V \) characteristic, with the resistance being independent of the Ge segment length. Assuming a square-well confining potential as well as periodic boundary conditions for a Ge NW with a diameter of \( 25 \) nm, the current from the continuous bands in the contact leads is redistributed to a maximum of four conductance channels inside the Ge NW (see the Supporting Information).\(^{39,40}\) According to Figure 2b, we assume that under the given experimental conditions (\( V_G = 0 \) V), we can only access one conductance channel. Thus, Figure 2b actually illustrates the modification of the transmission coefficient as a function of the channel length for the first conductance channel. This is supported by the enlarged view in the inset of Figure 2b, which shows that the resistance of Al–Ge–Al NW heterostructures with ultrascaled Ge channels is approaching the fundamental contact resistance of \( R_C = 12.9 \) k\( \Omega \), which is a first indication of ballistic transport.\(^{39}\)

For thin Ge NWs with diameters of about \( 25 \) nm and thus, close to \( \Delta_{Ge} \) quantum confinement results in a band structure being composed of multiple 1D sub-bands. According to the schematic shown in Figure 3a with the NW axis being oriented along the \( x \)-direction due to the quantum confinement in the \( y-z \) direction, the respective dispersion relation \( E(k) \) for holes of such a quantum wire provokes the corresponding quantization of conductance,\(^{42,43}\) with each 1D sub-band contributing a quantum unit of conductance of \( G_0 = 2e^2/h \).\(^{41}\)

Figure 3b shows the transient behavior of the measured conductance of three Al–Ge–Al NW heterostructure devices with Ge channel lengths of \( L_{Ge} = 15 \), \( 45 \), and \( 150 \) nm at \( V_G = 0 \)
−15 V and a bias of $V_D = 1 \text{ mV}$ in quantum units of conductance, $G_0$. For the 15 nm long Ge segment and, thus, the expected ballistic transport, an initial conductance of $2.5G_0$ indicates that the current from the continuous bands of the microscopic Al leads is redistributed to the first two sub-bands. The corresponding Fermi level and $G−V_G$ characteristic is schematically depicted by the green line in the schematic of Figure 3a. However, with the gate voltage kept constant at $V_G = −15$ V, the traps are discharged resulting in less effective gating (lower inset of Figure 3b). Finally, after approximately 80 min of trap depletion, the Fermi level adjusts close to the edge of the first subband (blue line of Figure 3a). In contrast, applying a positive gate voltage of $V_G = 15$ V provokes the filling of empty traps below the Fermi energy, resulting in a more-negative “effective” gate. This process continues until equilibrium is reached, having a higher number of trap states filled, which results in a Fermi level slightly below the edge of the third sub-band (red line of Figure 3a).

Thus, to support the proposed model, the upper left inset of Figure 3b shows the transfer characteristic for the ultrascaled ($L_{Ge} = 15$ nm) device for different trap filling levels. Initially, without any depletion or filling of the traps, sweeping $V_G$ from 0 to $−15$ V, two distinct step-like features are observed at 1 and $2G_0$ due to the quantization of the density of states, with each step attributed to the population of a single spin-degenerate $1D$ sub-band. As already discussed above and attributed to the almost-insignificant contact resistances, the injection barriers appeared to be negligible, indicating effective carrier injection with hole tunneling at the abrupt Al–Ge interface. However, $G−V_G$ measurements conducted for different trap depletion times between 15 and 60 min show that due to gradually trap depletion, the Fermi level moves upward, and thus, finally, only the first sub-band contributes to ballistic current transport, which is indicated by a step-like feature at $G_0$. Furthermore, operating the device with filled traps due to effective gating, the Fermi level lowers and populates the first three sub-bands, which is supported by distinct step-like features in the $G−V_G$ characteristic at integer multiples of $G_0$. Hence, by investigating the transient behavior of trap neutralization/filling on the electronic transport of ultrascaled Al–Ge–Al NW heterostructures, we demonstrate that although the Fermi level shifts in respect to the trap-filling level, conductance quantization persists.

With increasing channel length, carrier scattering, and, for NWs in particular, surface roughness scattering will influence charge transport, and finally, when exceeding the mean free path, carrier transport will become diffusive. Hence, for the device with $L_{Ge} = 45$ nm in the steady state, the conductance level is in the order of 0.25$G_0$ which is close to the ballistic limit. For the device with the channel length of 150 nm, exceeding the mean free path in Ge, the conductance level is only 0.1$G_0$. For even longer devices in the steady state, the diffusive transport leads to the observed linear dependency of the resistance on the channel length. The upper-right inset in Figure 3b depicts a compilation of steady-state $G−V_G$ measurements at $T = 300$ K of Al–Ge–Al NW heterostructure devices with Ge segment lengths $L_{Ge}$ between 15 and 45 nm. However, with increasing channel lengths, the plateau is shifted to lower conductance values corresponding to an added series resistance and, thus, a decrease of ballistic traversing charge carriers due to increased scattering. Investigations on numerous devices revealed that for devices with Ge segment lengths above $L_{Ge} = 45$ nm, all signs of conductance quantization at room temperature vanish.

Finally, we focus on the investigation of the temperature dependency of the ultrascaled Al–Ge–Al NW heterostructure devices. Figure 4a depicts the $G−V_G$ behavior of a device with a physical channel length of $L_{Ge} = 15$ nm measured in the temperature range between $T = 5$ K and 300 K. Distinct plateau-like features can be observed over the entire temperature range, and neither the overall conductance nor the steepness of the conduction plateaus change with increasing temperature. For the long-channel devices, drift current due to the applied electric field dominates the charge-carrier transport, and in accordance with the work of Jones et al., we observed a distinct decrease of conductivity due to a freeze-out of charge carriers below $T = 25$ K. The lack of such a temperature dependence for the ultrascaled devices is thus further proof of ballistic transport.

In addition to the plateau at $G_0$, the ultrascaled Al–Ge–Al NW heterostructure device with a Ge segment length of $L_{Ge} = 15$ nm exhibits several resonances below $G_0$. A plateau-like
feature at approximately 0.85G₀ could clearly be observed for temperatures up to T = 200 K and is assumed to be a result of spin effects, but so far, there is no generally accepted explanation for the origin of this conductance feature.43 Further plateau-like features observed at T = 5 K, fading away for higher temperatures, can be classified in intrinsic and extrinsic mechanisms.39,43–45 The origins of these conductance anomalies are assumed to be dedicated to tunneling resonances,46 single-electron charging effects,47 or geometric transmission resonances48 arising from impurities.

Figure 4b shows the bias spectroscopy at T = 70 K (Figure 4b) in which the device was cooled down without prior trap neutralization. Based on I/Vs measured for different V₉ values, the depicted curves correspond to dI胸怀/dV胸怀 versus V胸怀. In the low-bias region (linear regime), due to overlapping of measurements at different V胸怀 values, dense regions appear at integer multiples of G₀, which is consistent with quantized conductance plateaus for individual spin degenerate 1D sub-bands, where the influence of the gate voltage on dI胸怀/dV胸怀 is insignificant.49 With increasing bias voltage, we observed the evolution of conductance from integers multiples of G₀ to intermediate values at high bias voltages (±10 mV). As reported previously in quantum point contacts49 and 1D quantum wires,49 such half-plateaus appearing at intermediate values of G₀ at high bias voltages arise when the chemical potentials of source and drain occupy different sub-bands.50 Furthermore, the bias spectroscopy clearly revealed a conductance anomaly at 0.7G₀ which is considered to be an intrinsic low-temperature sub-G₀ feature of mesoscopic devices that is assumed to originate from many-body physics and was the first conduction anomaly that turned out to be independent of the material system.44,45,51

In conclusion, by utilizing a controlled thermal exchange reaction between single-crystalline VLS-grown Ge NWs and Al pads, we demonstrated room-temperature quantum ballistic transport in back-gated Al–Ge–Al NW heterostructure devices with ultrascaler Ge segments. In addition, we have shown that the number of populated sub-bands can be modulated with respect to the trap-filling level. Most importantly, the investigations provide a platform for the exploration of ultrascaler devices based on Ge NWs and, thus, are an important step toward the practical application of ballistic transport at room temperature.

■ ASSOCIATED CONTENT

2 Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b00425.

Basic calculations of the conductance channels and a discussion of injection barriers for passivated and unpassivated Al–Ge–Al NW heterostructures (PDF)

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