Predicting Post-Route Quality of Results Estimates for HLS Designs using Machine Learning

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Abstract—Machine learning (ML) has been widely used to improve the predictability of EDA tools. The use of CAD tools that express designs at higher levels of abstraction makes machine learning even more important to highlight the performance of various design steps. Behavioral descriptions used during the high-level synthesis (HLS) are completely technology independent making it hard for designers to interpret how changes in the synthesis options affect the resultant circuit. FPGA design flows are completely embracing HLS based methodologies so that software engineers with almost no hardware design skills can easily use their tools. HLS tools allow design space exploration by modifying synthesis options, however, they lack accuracy in the Quality of Results (QoR) reported right after HLS. This lack of correctness results in sub-optimal designs with problems in timing closure. This paper presents a robust ML based design flow that can accurately predict post-route QoR for a given behavioral description without the need to synthesize the design. The model is an important design exploration tool where a designer can quickly view the impact on overall design quality when local and global optimization directives are changed. The proposed methodology presents two strong advantages: (i) Accurate prediction of the design quality (QoR), and (ii) complete elimination of the need to execute high-level synthesis for each design option. We predict three post route parameters, (i). Area, (ii). Latency and (iii). Clock Period of a design just by analyzing the high level behavioral code and some intermediate representation codes. We have integrated the methodology with Xilinx HLS tools and have demonstrated accurate estimation on a variety of FPGA families. Our estimated results are within 10% of actual computed values.

Index Terms—High Level Synthesis, Post-Route Parameter Prediction, Regression Models

I. INTRODUCTION

The use of High-Level Synthesis (HLS) tools for FPGA-based flows is becoming common as it allows easy conversion of software descriptions into fairly accurate clocked hardware designs. HLS based design methodologies enable designers to focus on algorithmic variations of high-level programs to obtain the best micro-architectural trade-offs. HLS reduces the overall design time as it allows the generation of different versions of a functionally equivalent design without modifying the behavioral code.

In traditional HLS design flows, there are three control parameters for generating varying RT-level designs[1]. Local Synthesis Directives in the form of pragmas are inserted as comments, Global Synthesis Directives are the options like desired clock frequency that direct the overall global synthesis constraints, and Functional Unit Constraints provide bounds on the number of available functional units of various types. The last parameter allows tighter control for SoC/ASIC style designs. Xilinx’s Vivado HLS [2], and Intel’s HLS compiler [3] do not support the functional unit constraints. The only global synthesis option that the Xilinx Vivado HLX supports is the target synthesis frequency.

Figure 1 illustrates a design flow for HLS based designs targeted on FPGAs. The synthesis directives (Local and Global) create an annotated input for the synthesis tool. The annotated input is then synthesized along with the technology library to generate an RTL code. The process is iterated in design space exploration many number of times to obtain an acceptable set of trade off designs (near Pareto-optimal designs). The selected optimal set of designs then undergo the steps of logic synthesis, technology mapping, and place and route.

II. QoR METRICS

HLS tools must report accurate Area and Performance after each synthesis run. Area reporting in the form of only the LUT usage [4], [5], [6] and comprehensive usage of LUTs and other blocks are fairly common in the literature. In this paper, we will refer to number of LUTs (A) only for reporting area resources which consistent with other published works [4], [5], [6]. Commercial HLS tools produce fairly correct estimates for the BRAM and DSP resources. Latency (L) in the form of clock cycles is an accepted metric for FPGA-based design flows, and a correct estimate of Latency is available after the HLS Synthesis stage. In this paper, we will report Latency and the post-route maximum clock frequency $f_{max}$. 

![Fig. 1: Conventional FPGA Design Flow and the Proposed Model](image-url)
The rest of the paper is organized as follows. Section IV gives an overview of the existing work. Section V defined the problem statement. The proposed post route QoR prediction model is described in Section VI. The experiments and results are presented in Section VII. Section VIII concludes the paper.

IV. RELATED WORKS

In a recent paper, COMBA [8], the authors presented a metrics guided design space exploration method where they study the effect of different pragmas on the latency of the design. The research produces impressively correct performance estimates for the behavioral models in a negligible amount of time. The comparison with Xilinx Vivado HLS toolset shows that COMBA provides approximately similar quality estimates compared to the output of HLS toolset. However, it is observed in [4] as well as [5] that the post-synthesis QoR, as reported by commercial tools like Xilinx Vivado HLS, is grossly different from the final post-route QoR for a given design. We have highlighted this difference through experiments in section IV as illustrated in Figure 2. Dai et al. [4] created a regression based machine learning model to estimate accurate post-route resource and timing of a design using features extracted from the post-synthesis log files. This work is more like calibration where resource and timing estimation error is fixed after a high-level synthesis stage. Both approaches in [4] and [5] require time consuming C-synthesis step before QoR estimates can be corrected. In another recent work, Ironman [6], the authors proposed post route resource and timing requirement of HLS designs using graph based learning methods. In order to do so, they used synthesized data flow graphs (DFG) generated from IR code as an input to their ML model.

While fairly accurate, the methods reported in [4] and [5] require a time-consuming synthesis step before QoR can be accurately estimated and [6] requires scheduled DFG graphs from synthesis stage. COMBA is a fast approach for estimation but the accuracy of estimates matches only with the post-C-synthesis results. In Table I, we have summarized the four relevant works described in [4], [5], [6] and [8], and compared them with our presented research. The research presented in this paper is comprehensive and predicts all the post route vital performance measuring parameters of a HLS design viz., clock period, latency and resource requirement together. It also eliminates the need for full C-synthesis.

V. PROBLEM DEFINITION

Given a synthesizable C/C++ based high-level code with synthesis directives in the form of pragma, and the desired global frequency of operation, create a machine learning based model which will predict the post-route clock period, latency and resource requirement of a design without synthesizing the design in real time.

We formulated the post route QoR prediction of HLS design as a machine learning based regression model. Fig. 1 shows the basic block diagram of our proposed methodology.
TABLE I: Comparison of the proposed work with the state of the art research

| Reference | Predicted Parameter | C-Synthesis Required | Feature Source | Reference Labels |
|-----------|---------------------|----------------------|----------------|------------------|
| Fast [1] | ✓ ✓ ✓ | ✓ | Synthesis Log Files | Post Route |
| Pyramid [5] | ✓ ✓ ✓ | ✓ | Synthesis Log Files | Post Route |
| Comma [8] | ◯ ✓ ✓ | No | Analytical | Post-C synthesis |
| Ironman [6] | ✓ ✓ ✓ | Scheduled DFG | Scheduled DFG | Post Route |
| This Work | ✓ ✓ ✓ | No | C++/LLVM IR | Post Route |

VI. QoR Metrics Prediction Framework

LLVM[10] is an open source compiler which is used to develop executable codes for multiple platforms. LLVM generates technology and processor independent assembly language code called Intermediate Representation (IR). There is an optimizer present in LLVM, which optimizes the IR code. The final optimized IR code is converted into Control and Dataflow Graphs (CDFGs) which are later used for scheduling and binding of the generated RTL code. The LLVM toolchain also generates callgraphs which represent the inter-function relationships in a C/C++ codes. These functions are later synthesized as individual modules in the generated RTL code.

We have analyzed the High Level C/C++ codes, Pragma optimized LLVM IR codes, Control and Dataflow Graphs, and Call-graphs to extract features that can help us in predicting final QoR metrics. We have used HLS benchmarks taken from CHStone[7] benchmark set. These benchmarks are very diverse in terms of code structure, applications as well as area and timing costs. These benchmarks represent many single-function and multi-function designs. We generate multiple versions from a single HLS design by changing the following six pragmas in the HLS codes: (i) Loop Unrolling, (ii) Loop Pipelining, (iii) Array Partitioning, (iv) Array Reshaping, (v) Function Inlining, and (vi) Function Instantiation.

For each benchmark shown in Table II we have generated 400 versions (data) of the design by varying the pragmas and desired target frequency. Table II shows the statistics of range of variation of Latency, Clock-Period, and the LUT usage for each benchmark versions when the designs are mapped on the Zynq 7000 device. Our methodology has also been verified using Xilinx VIRTEX and KINTEX series of devices also. It is clear from Table II that the data is very diverse and would support building robust training models.

TABLE II: Statistics of Training/Testing benchmarks

| Design Name | Latency Range | Clock Period Range (ns) | LUT Range |
|-------------|---------------|--------------------------|-----------|
| adpcm       | 3119-62536    | 2.078-8.462              | 56-410000 |
| matrix_mult | 36-274        | 3.48-6.849               | 667-7139  |
| sobel       | 13-38         | 1.46-3.14                | 33-121    |
| average     | 2-211         | 1.338-2.623              | 4-3265    |
| dfadd       | NA            | 3.908-6.081              | 3634-4891 |
| dsin        | NA            | 6.137-8.74               | 4348-8818 |
| ddiv        | NA            | 6.887                    | 3318-3472 |
| sha         | 45-1330       | 2.299-4.221              | 101-1889  |
| blowfish    | 23525-36386   | 4.321-9.371              | 3357-60537|
| aes         | 2697-2937     | 2.815-5.021              | 186-1839  |
| Overall     | 2-63536       | 1.436-9.371              | 4-60537   |

A. Feature Extraction

We have created an extensive set of features to create a robust prediction model. We extracted a total of 69 features from four different sources, examples of which are shown in Table III. The features are either numerical or categorical features. An example of a numerical feature is the length of the longest path in the data-flow graph, and an example of a categorical feature is data-type that can be 8-bit integer, 16-bit integer, or a double-precision floating point number. Table III lists some of the important features used for training the models. The extracted features from each of the four sources are briefly described here.

i. High Level Code: As shown in Table III we extract 13 features from the HLS code. These features include information about the pragmas. Features extracted from HLS code include information about the loop unrolling and loop pipelining. We extract unroll factor, pipeline initiation interval (II) and batch size of the loops. Based on the pragma arguments, we compute a batch_size for each loop. It is defined as a ratio between the loop-bound and the unrolling factor for a loop. While the unrolling factor represents the degree of parallelism, and the batch_size represents the depth of the computation.

ii. LLVM IR Code: LLVM IR code are made up of basic blocks (BB). Each BB is a set of continuous assembly instructions, which are branched at if-else conditions, function returns and loops. We analyzed each of the BB in detail, and calculated total, maximum and average number of instructions in each BB. There are 9 types of instructions in LLVM. From each BB, we calculate the maximum, total and average number math, sign/zero extension, memory and logic instruction and vector instructions from the LLVM

| Feature Source | Feature Examples | No. of Features |
|----------------|------------------|----------------|
| HLS Code       | Max and average unrolled factor | 13 |
|                | Max & Average Batch size of loops | |
|                | Max Pipelined Loop Name | |
|                | Max & Average Pipelined II | |
| LLVM IR Code   | Max, average total number of instructions per BB | 44 |
|                | Max, average total number of (math, sign ext, zero ext, logic, memory, vector, other) operations | |
| CDFG           | Total number of nodes | 6 |
|                | Max length of critical path | |
|                | Number of FCUs | |
|                | Max path length | |
|                | Max and average number of incoming/outgoing edges | |
| Callgraph      | Properties of child functions | 6 |
|                | Max, min (latency, CP, FCUs) | |
| Total          | | 69 |
IR code. Example features are shown in Table III. This is most exhaustive source of features, and we extract 44 features from the IR code.

iii. Control and Data Flow Graph: Control flow graphs describe the inter-function relationship in a code. Most of the HLS codes are complex multi_function designs. Each node in the callgraph represents a function in the HLS code. By analyzing the callgraph, characteristics of the child nodes like a number of FCUs, latency, minimum and maximum clock period of child functions and the datatype passed from one function to another are extracted and passed to the root (Top) function.

We passed all the features through a feature analysis tool, xgboost regression feature analysis tool [11] and plotted the results in Fig. 3. In Fig. 3 we have normalized the importance of each feature to a range of 0 to 100. Each bar in Fig. 3 represents the sum of all the features from a particular source. As it can be seen from the bar diagram, IR file features hold most importance, while callgraph features hold least importance for our regression model.

iv. Callgraph: Callgraphs describe the inter-function relationship in a code. Most of the HLS codes are complex multi_function designs. Each node in the callgraph represents a function in the HLS code. By analyzing the callgraph, characteristics of the child nodes like a number of FCUs, latency, minimum and maximum clock period of child functions and the datatype passed from one function to another are extracted and passed to the root (Top) function.

Fig. 3: Feature Importance Analysis

B. Model Creation

For each data element described in the section VII we extract features. The same designs are also routed using Vivado P & R tools to generate the target labels. We also observed that the labels can be generated after logic synthesis stage also, step (9) in Figure 1 when the accurate estimate of resources and a near-accurate estimate of clock frequency and latency is available to the designer. There is a small error for clock period, since the router adds the wire delay thereby increasing the post route clock period by a small amount- around 1.5 ns. Labels generated after logic synthesis will also provide same QoR but we will save substantial (almost 30%) place & route execution time for label creation. For this particular work, we used the labels generated after routing. The entire training and prediction flow is illustrated in Fig. 4 where the black dotted box represents the training part consisting of feature extraction, label generation, and training, and the solid box below represents the prediction flow.

In order to measure the correctness of QoR prediction, we have used the average of mean absolute percentage error (MAPE) for all the models. MAPE is calculated using the following formula:

$$MAPE = \frac{1}{N} \sum \frac{|y_{actual} - y_{predicted}|}{y_{actual}} \times 100$$

(1)

In equation 1, $y_{predicted}$ and $y_{actual}$ represents the predicted and actual value respectively while N represented the total number of designs being tested.

VII. Testing and Results

A. Experimental Setup

We have synthesized and implemented our HLS designs on Intel Xeon E5-2603 quadcore processor based workstation with 32 GB RAM. The synthesis and implementation software used for this work is Xilinx Vivado 2019.1, while the target hardware is Xilinx Zynq 7000 series FPGA device. Our methodology has also been verified using Xilinx VIRTEX and KINTEX series of devices and we will present to support

Fig. 4: Training and Prediction Flow

Fig. 5: Change in $R^2$ value with increase in training datasize
TABLE IV: MAPE for different models trained

| Model Used | CLK | Latency | LUT |
|------------|-----|---------|-----|
| HLS        | 100.45% | NA     | 592.23% |
| MLP        | 9.60%   | 16.58% | 44.14% |
| RF         | 7.98%   | 18.25% | 16.28% |
| XGB        | 6.29%   | 10.22% | 10.32% |

the versatility of our methodology. We have used state of the art ML libraries ScikitLearn 0.19.1[12] and xgboost 0.90[11] running on Nvidia GeForce GTX 1080 GPUs to train our models. We used cloud-based Comet.ml[13] for hyperparameter tuning tool.

B. Training of Models
As stated in section[11] we have used 400 versions of designs for each of the benchmarks. To study the effectiveness of a regression model, we have plotted how the value of R² increase with increase in training data size in Figure[5]. The x-axis represent the percentage of total design points used for training. An R² value in the range of 0.7 to 0.8 is considered to be good for a model. The plot in the Figure[5] shows that a well-trained model can be achieved using a small fraction (around 30%) of the total data for predicting LUT resources and the clock period. However, predicting for latency may require much larger training data set. Based on assertions presented in Figure[5], we trained the individual designs on the generated 120 versions and predicted on another 280 designs. The matrix_multiplier design was trained and tested on half of the total 1500 designs. This is because matrix_multiplier is highly customizable in terms of dimensions, pragmas and frequencies.

C. Analysis of Results
We have presented results using all of the ten benchmarks described in Table[III]. We have also conducted experiments to demonstrate the robustness of our models using one very large and diverse benchmark: adpcm. adpcm is a very complex benchmark consisting of 13 loops, 10 arrays and 11 different functions. We selected adpcm because it is the most diverse design in terms of resource and latency requirement among all the CHStone benchmarks. As shown in Table[III], the LUT utilization ranges from 56 to 410K LUTs, while flipflop utilization ranges from 83 to 237k units and latency ranges from 3119 to 62536 clock cycles.

We have trained our model using three different regression models viz. (i) Multi-layer Perceptron Regression (MLP); (ii) Random Forest (RF) (iii) Gradient Boost Regression (XGB). The average results for the 10 benchmarks using the three models are shown in Table[IV]. In Table[IV] we have shown the average MAPE for the clock, latency, and LUTs for the ten benchmarks using the three regression models. In the third row (HLS), average MAPE reported by Vivado HLS after C-synthesis stage is presented. Each error is computed against the actual post-route value. It can be observed that very high accuracy is achieved using ensemble methods like XGB and RF. We chose XGB as our preferred model for rest of the experiments.

Table[VI] shows the MAPE values for each of the ten benchmarks used for testing. These results are based on XGB regression model, where training is done on 120 versions of a design, and prediction is done on 280 versions. Vivado HLS estimates are shown in Column 3 and 6 in Table[VI]. The estimates produced by Vivado HLS are very inaccurate, and on an average, our prediction is very accurate and our framework promises to provide a good design guidance to the designer. The LUT resource usage error change is relatively higher when compared with the clock period and the latency of the design. This is because the spectrum of LUT usage is very wide from a minimum of 4 to a maximum of 65K LUTS. In Fig[6], we have show the actual vs predicted values of all the three predicted parameters for adpcm benchmark, running on Zynq 7000 FPGA device using 100MHz frequency. As it can be seen from the figure, our prediction highly correlates with the actual value.

Our model is able to capture the effect of the target global frequency on the overall design and resource usage. It is expected that the variation of desired global frequency will result in a change in scheduling during the high-level synthesis, and therefore will result in different architectures with varying resource usage, latency, and clock-period. We tested the model for adpcm benchmark. We tested the model on the baseline (no pragmas design for adpcm). During training, we generated labels using three target frequency selections, i.e., 100MHz, 150MHz, and 200MHz. During testing, we varied the global-desired-frequency constraint from 100MHz to 500MHz. After 500MHz, Xilinx Vivado returns the same best possible design. Normally, an HLS tool will schedule single computation step in multiple clock cycles when the desired target frequency is very high. Xilinx Vivado does not perform such mapping. Table[VI] illustrates the results. We can observe that our model results in very accurate estimates for the QoR metrics. It is worth mentioning here that we trained on 3 frequencies (100MHz, 150MHz and 200MHz), while the model is able to accurately predict on 8 frequencies, 5 of which are not part of the training dataset. In Table[VI] we have also shown the estimated values of Vivado HLS tool after C-synthesis.

We also demonstrate the robustness of our methodology on other devices from Xilinx, including the Virtex-7 and Kintex-7 series of FPGAs. We trained the models using labels when designs were mapped on the selected device. Table[VI] presents results when adpcm benchmark was mapped on Virtex, Kintex, Zynq devices. The test results in Table[VI] however, are based on 64 completely new (blind) versions of pragma inserted designs that were not part of the train and validation framework.

VIII. Conclusion
We have presented a comprehensive and robust classical machine learning based post-route timing and resource requirement prediction tool for FPGA based HLS designs. Unlike previous approaches[4], [5], [6], our methodology does not require time consuming C-synthesis step as we extract features right out of the high-level behavioral code. Our method improves the state of the art by producing better or comparable results using a model created prior to synthesis. We believe that this is first such attempt that models the entire design flow as a machine learning model,
TABLE V: Actual vs Predicted values of resource and timing. Frequency Sweep from 100MHz to 500 MHz

| Target Frequency (MHz) | Clock Period (ns) | Latency (clock cycles) | # of LUTs | Clock Period (ns) | Latency (clock cycles) | # of LUTs | Clock Period (ns) | Latency (clock cycles) | # of LUTs |
|------------------------|-------------------|------------------------|------------|-------------------|------------------------|------------|-------------------|------------------------|------------|
|                        | Actual            | Predicted              | Vivado HLS | Actual            | Predicted              | Vivado HLS | Actual            | Predicted              | Vivado HLS |
| 100                    | 7.74              | 7.44                   | 9.10       | 20104             | 21659                  | 3244       | 5038              |
| 125                    | 6.64              | 7.41                   | 8.30       | 23604             | 21677                  | 3244       | 5039              |
| 150                    | 6.64              | 6.29                   | 6.05       | 28254             | 26916                  | 3244       | 5852              |
| 175                    | 4.55              | 4.49                   | 5.55       | 34004             | 40351                  | 3244       | 5821              |
| 200                    | 4.55              | 4.60                   | 4.49       | 43154             | 41332                  | 3244       | 4487              |
| 225                    | 4.55              | 4.60                   | 3.83       | 43204             | 41332                  | 2636       | 4484              |
| 300                    | 3.00              | 3.11                   | 3.39       | 55954             | 43586                  | 2740       | 5030              |
| 500                    | 3.00              | 3.46                   | 3.39       | 111654            | 42881                  | 3343       | 5687              |

TABLE VI: Validation and Test MAPE on 64 unseen designs on 3 different FPGA devices

| Device | Clock Period | Latency | Resource |
|--------|--------------|---------|----------|
| Zynq 7000 | 5.55 | 7.75 | 198.09 |
| Virtex 7 | 4.11 | 6.50 | 152.66 |
| Kintex 7 | 5.51 | 5.06 | 82.6 |

TABLE VII: MAPE for benchmarks and Vivado Estimates

| Design Name | Clock Period | Latency | Resource |
|-------------|--------------|---------|----------|
| adpcm       | 7.75         | 198.09  | 17.54    |
| ave8        | 7.28         | 182.14  | 14.12    |
| matn        | 7.92         | 67.15   | 8.37     |
| sobel       | 0.6          | 163.23  | 1.76     |
| dflaag      | 6.33         | 87.88   | 4.35     |
| dfldiv      | 0.19         | 26.19   | NA       |
| dfpsin      | 2.78         | 39.39   | 3.78     |
| aes         | 9.44         | 103.46  | NA       |
| blowfish    | 14.35        | 36.57   | NA       |
| Average     | 6.29         | 100.45  | 10.22    |

Note: NA: Reference labels not reported by HLS tool.

Thereby totally eliminating the HLS and physical design tools from the flow.

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