Multi-Beam RF Aperture Using Multiplierless FFT Approximation

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Abstract

Multiple independent radio frequency (RF) beams find applications in communications, radio astronomy, radar, and microwave imaging. An N-point FFT applied spatially across an array of receiver antennas provides N-independent RF beams at $\frac{N}{2} \log_2 N$ multiplier complexity. Here, a low-complexity multiplierless approximation for the 8-point FFT is presented for RF beamforming, using only 26 additions. The algorithm provides eight beams that closely resemble the antenna array patterns of the traditional FFT-based beamformer albeit without using multipliers. The proposed FFT-like algorithm is useful for low-power RF multi-beam receivers; being synthesized in 45 nm CMOS technology at 1.1 V supply, and verified on-chip using a Xilinx Virtex-6 Lx240T FPGA device. The CMOS simulation and FPGA implementation indicate bandwidths of 588 MHz and 369 MHz, respectively, for each of the independent receive-mode RF beams.

1 Introduction

Antenna array based radio frequency (RF) applications such as radar, wireless communications, localization, remote sensing, signal intelligence, radio astronomy, search for extraterrestrial intelligence (SETI), and imaging requires the fundamental operation of receive mode beamforming. To wit, beamforming is precisely the directional enhancement of propagating electromagnetic planar-waves based on their directions of arrival (DOA), whilst suppressing undesired noise and interference that impinge on the antenna array. The ability to form multiple receiver beams is known as “multi-beamforming” [1] [2]. Multiple RF beams, each having a unique “look direction”—the direction of maximum sensitivity—is needed for multiple visibilities.

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Multiple simultaneous beams are also needed for search-and-track radar, which in volume-scan mode, continuously monitor airborne threats, such as aircraft, warheads and cruise missiles, across a given range of angles. From the standpoint of high-capacity wireless communications, simultaneous receiver beams are of importance to multi-input multi-output (MIMO) systems. The application of an $N$-point fast Fourier transform (FFT)—at each time sample—spatially, across a uniform linear array (ULA) of antennas, is a technique for achieving a plurality of independent RF beams\[1\, 2\]. The FFT efficiently computes the discrete Fourier transform (DFT) with $\frac{N^2}{2} \log_2 N$ multiplications. Fig. 1 shows an overview of a ULA-based multi-beamformer using a spatial FFT. For an $N$-element ULA, the spatial FFT beamformer provides $N$ beams, each uniformly spaced in the frequency domain by the interval $2\pi/N$. The signal is first sent through a low noise amplifier (LNA) and the real (I, in-phase, $v_{\text{real}}$) and the imaginary (Q, quadrature, $v_{\text{im}}$) parts are low-pass filtered and sampled using analog-to-digital converters (ADCs), before application of the DFT. The spatial angle $\psi$ is the independent variable used in the polar array beam-patterns.

RF aperture power consumption is directly proportional to circuit complexity and clock frequency. Because multiplier hardware dominates circuit complexity, the utilization of FFT hardware having as small a number of parallel multiplier circuits as possible is preferable in terms of reduction of overall circuit complexity and power consumption of the multi-beamformer. The proposed fast algorithm approximates the FFT computation without using any multipliers at all, making the corresponding digital architecture very simple to realize on-chip. Because the proposed fast algorithm only requires 26 addition operation, the corresponding architecture is of lower power consumption compared to usual FFT-based circuits having parallel multipliers to implement the twiddle factors.

\section*{2 Multiplier-Free DFT Approximation}

The DFT is a linear orthogonal transformation relating an $N$-point input vector $\mathbf{v} = [v_0 \ v_1 \ \ldots \ v_N]^\top$ to an output vector denoted by $\mathbf{V} = [V_0 \ V_1 \ \ldots \ V_N]^\top$ according to

$$V_k = \sum_{n=0}^{N-1} v_n \cdot \omega_N^{kn}, \quad k = 0, 1, \ldots, N - 1,$$

where $\omega_N = \exp\{-2\pi j/N\}$ is the $N$th root of unity.\[3\]
and \( j = \sqrt{-1} \). In matrix formalism, the above expression reduces to: \( V = F_N \cdot v \), where \( F_N \) is the DFT matrix, whose \((i,k)\)-th element is given by \( f_{i,k} = \omega_{nk}^i \), for \( i, k = 0, 1, \ldots, N - 1 \). The direct DFT computation requires \( N^2 \) complex multiplications and \( N \cdot (N - 1) \) additions. Thus, fast algorithms are necessary and are often able to reduce the computation cost of the DFT computation to \( O(N \cdot \log_2 N) \) multiplications [4].

We submitted the 8-point DFT matrix \( F_8 \) to the parametric-based optimization method described in [5] to derive a matrix approximation. Two major constraints were imposed on the sought DFT matrix, whose \((i,k)\)-th elements satisfy the following matrix approximations:

\[
\hat{F}_N = \frac{1}{2} \begin{bmatrix}
2 & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & -2j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & -j & -2j & 1 & \ldots & 2 & -j & -2j & 1 & \ldots & 2 \\
2 & 1 & \ldots & 2 & -j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & -j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & 1 & \ldots & 2 & -j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & -2j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 & -j & 1 & \ldots & 2 \\
2 & -j & -2j & 1 & \ldots & 2 & -j & -2j & 1 & \ldots & 2 & -j & -2j & 1 & \ldots & 2
\end{bmatrix}
\]

Compared to the exact DFT matrix, above approximation has a mean squared error of 0.686, which is considerably low. Although not exactly orthogonal, the proposed approximation is very close to orthogonality. Considering the deviation from orthogonality measure [6], the proposed transform displayed a deviation of 0.03; whereas, in comparison, the popular non-orthogonal DCT approximation SDCT [7] has a deviation from orthogonality of 0.20.

The proposed approximate matrix \( \hat{F}_8 \) preserves the symmetry of the DFT and has null multiplicative complexity. Still requiring 64 additions and 32 bit-shifting operations, a further reduction in the additive complexity can be obtained by means of a tailored fast algorithm. Let \( I_n \) be the identity matrix of order \( n \) and \( B_n = [1 \ -1] \otimes I_{n/2} \), where \( \otimes \) denotes the Kronecker product. Thus, employing the matrix factorization methods suggested in [4], there exists a fast algorithm:

\[
\hat{F}_8 = P \times \text{diag} \left( I_2, A_1, A_3 \right) \times D_2 \times \text{diag} \left( B_2, I_2, A_4 \right) \times D_1 \times \text{diag} \left( B_4, A_2 \right) \times B_8,
\]

where \( A_1 = \begin{bmatrix} 1 & -1 \\ 1 & -1 \end{bmatrix} \), \( A_2 = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & -1 \end{bmatrix} \), \( A_3 = \begin{bmatrix} 1 & -1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \), \( A_4 = \begin{bmatrix} 1 & 1 & -1 \\ 1 & 1 & -1 \end{bmatrix} \), \( D_1 = \text{diag} \left( 1, 1, 1, 1, 1/2, 1, 1/2 \right) \), \( D_2 = \text{diag} \left( 1, 1, 1, 1, 1, 1, 1, 1 \right) \), \( P = \begin{bmatrix} e_1 | e_2 | e_3 | e_4 | e_5 | e_6 | e_7 | e_8 \end{bmatrix} \) is a permutation matrix, and \( e_i \) is the 8-point column vector with element \( 1 \) at the \( i \)-th position and \( 0 \) elsewhere. Figure 2 depicts the signal flow graph of the introduced algorithm. The arithmetic complexity assessment in terms of real operations and comparisons is summarized in Table 1.

Each row \( i \) of matrix \( F_8 \) may be interpreted as the coefficients of a discrete filter whose transfer function is \( H_i(\omega; F_8) = \sum_{k=0}^{N-1} f_{i,k} \cdot \exp(-jk\omega), i = 0, 1, \ldots, 7 \), for \( \omega \in [-\pi, \pi] \) [3]. In the case of multi-beam forming, the exact or approximate DFT are applied spatially, across a ULA of
Figure 2: Signal flow graph for the factorization of $\hat{F}_8$. Input data $v_i$, $i = 0, 1, \ldots, 7$, relates to the output $V_k$, $k = 0, 1, \ldots, 7$. Dotted arrows represent multiplications by $-1$.

Table 1: Real operation assessment and comparison

| Method                        | Multiplications | Additions | Shifts |
|-------------------------------|-----------------|-----------|--------|
| Exact DFT                     | 256             | 240       | 0      |
| FFT (complex input) [3]       | 4               | 52        | 0      |
| FFT (real input) [3]          | 2               | 26        | 0      |
| Proposed (complex input)      | 0               | 52        | 4      |
| Proposed (real input)         | 0               | 26        | 2      |
antennas. Here, variable \( \omega \) is the spatial frequency across the ULA. Let the normalized temporal frequency of the incident plane wave be \( \omega_t \leq \pi \). From physics, we have that \( \omega = -\omega_t \sin \psi \), for \(-\pi/2 \leq \psi \leq \pi/2\), measured counter-clockwise from ULA broadside. We set \( \omega_t = \pi \), which corresponds to \( \psi \in [-\pi/2, \pi/2] \). Thus, the array patterns are given by:

\[
P_i(\psi; F_8) = \frac{|H_i(-\omega_t \sin(\psi); F_8)|}{\beta_i},
\]

where \( \beta_i = \max_{\psi} |H_i(-\omega_t \sin(\psi))| \), for \( i = 0, 1, \ldots, 7 \), is a normalization factor. \textit{Mutatis mutandis}, the array patterns based on the proposed approximation are denoted by \( P_i(\psi; \hat{F}_8) \), \( i = 0, 1, \ldots, 7 \).

Figure 3(a)–(b) shows the pattern arrays associated to each row of \( F_8 \) and \( \hat{F}_8 \). The eight independent beams are pointed at angles \( \psi_k = 0.00, \pm14.47, \pm30.00, \pm48.59, 90.00 \) in degrees measured from array broadside direction, as expected from the conventional DFT beamformer. To quantify the difference between corresponding array patterns, we considered the following error function:

\[
D_i(\psi) \triangleq \left| P_i(\psi; F_8) - P_i(\psi; \hat{F}_8) \right|, \quad i = 0, 1, \ldots, 7.
\]

In Figure 3(c), the polar plot of \( D_i(\psi) \) for all rows of \( \hat{F}_8 \) is displayed. The error energy can be obtained integrating \( D_i(\psi) \):

\[
\epsilon_i = \int_{-\pi/2}^{\pi/2} D_i^2(\psi) \, d\psi, \quad i = 0, 1, \ldots, 7.
\]

This computation furnished \( \epsilon_i = 1.08 \), for odd \( i \), and \( \epsilon_i = 0 \), for even \( i \). The total error energy is 4.32. For comparison, the approximate DCT described in [3] has a total error energy of 4.12.

## 3 FPGA Realization and ASIC Synthesis

The proposed multiplierless architecture was realized on digital hardware using an ML-605 Xilinx Virtex-6 field programmable gate array (FPGA) prototyping board. The design was built and tested for 16-bit inputs via JTAG interface. Moreover, it was pipelined to minimize the critical-path delay \( T_{cpd} \), which in turn offers the maximum frequency of operation and RF bandwidth. The on-FPGA measured results verified the performance of the proposed architecture. The FPGA resource consumption, including the number of slices, look-up tables (LUTs), and flip-flop (FF) count, is presented in Table 2. The percentage utilization of the available resources is also shown. The pipelined design offered a maximum frequency of 739 MHz corresponding to a maximum RF bandwidth of 369 MHz for each of the eight beams.

The FPGA-based digital design was imported to Cadence RTL compiler for application-specific integrated circuit (ASIC) synthesis using 45 nm complementary metal oxide semiconductor (CMOS) technology, for an operating voltage of 1.1 V at 27°C. Table 3 displays the area, power, critical path
Figure 3: Polar plots of $P_i(\psi; F_8), i = 0, 1, \ldots, 7, \psi \in [-\pi/2, \pi/2]$ at the frequency $\omega_t = \pi$ for the (a) exact transform $F_8$, (b) proposed approximate transform $\hat{F}_8$, and (c) error measure $D_i(\psi)$.

Table 2: FPGA resource consumption

| Resources          | Proposed |
|--------------------|----------|
| Slice Registers    | 3064 (1%)|
| Slice LUTs         | 2044 (1%)|
| Occupied Slices    | 620 (1%) |
| LUT-FF Pairs       | 2335 (1%)|
| Bonded IOBs        | 2 (1%)   |
| $T_{cpd}$ (ns)     | 1.353    |
| Max. Frequency (MHz)| 739.09   |
delay, and maximum frequency of operation, at synthesis stage. The area-time (AT) and area-time$^2$ (AT$^2$) complexities are reported. The CMOS synthesis shows an increase in the maximum clock frequency when compared to its FPGA implementation.

## 4 Conclusion

An 8-point multiplierless DFT approximation requiring 26 additions was proposed. Applications in receive mode RF multi-beamforming using a ULA of antennas include communication, radar, and radio astronomy. CMOS synthesis and FPGA implementations have indicated bandwidths of 588 MHz and 369 MHz, respectively. The approximation is suitable for eight digital RF-beams, at low power. The DFT approximation allows FFT-like performance without multiplier hardware.

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