A GaAs p-HEMT Distributed Drain Mixer with Low LO Drive Power, High Isolation, and Zero Power Consumption

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ABSTRACT This paper presents a balanced distributed drain mixer fabricated in a 0.25-μm GaAs p-HEMT technology. The balanced distributed mixer combines two single-ended distributed mixers with an on-chip RF balun and LO divider integrated for improving isolation performance. Each single-ended mixer is designed with three drain-mixing unit cells distributed along transmission lines for broadband operation. The transistor size, bias condition and transmission line lengths are analyzed and determined to improve the conversion gain, bandwidth and impedance matching. In addition, the LO drive power required for mixing operation is reduced by bias optimization and large-signal LO matching. The balanced distributed drain mixer exhibits measured conversion gain of -4.0 to -7.4 dB from 5.4 to 21.8 GHz. The LO drive power of the mixer is as low as 2 dBm. The LO-to-RF and LO-to-IF isolation are higher than 23.5 and 54.7 dB, respectively. The mixer consumes no dc power due to the passive drain-mixing topology.

INDEX TERMS Distributed mixer, GaAs, millimeter-wave, MMIC, wideband, zero dc power

I. INTRODUCTION

As the communication technology evolves, a need for broadband RF front-end supporting multiple frequency bands for various communication standards is increasing. Several types of mixers such as double-balanced mixers [1]-[5], passive mixers [6]-[10], distributed mixers [9]-[17] have been reported as a key component for frequency conversion in the RF front-end. Among them, the distributed topology is an attractive option for broadband down-conversion mixers due to its flat conversion gain over a wide bandwidth.

Several active distributed mixers based on GaAs or silicon technologies were reported. In [12] and [13], the isolation performance of the distributed mixer was improved by adopting a cascode or balanced structure as a mixing unit cell. However, those structures require a large number of transistors, resulting in high dc power consumption. In order to reduce or eliminate dc power consumption, low-power active or passive distributed mixers were proposed [9], [10], [14]-[17]. However, most of those mixers suffer from high LO drive power required for mixing operation or poor port isolation [9], [10], [14]. In [15] and [16], a balanced structure is adopted to improve the isolation, but it rather requires additional external components such as RF or LO baluns.

In this paper, we present a balanced distributed drain mixer that provides wideband conversion gain with zero dc power consumption. The balanced mixer integrates two single-ended mixers with on-chip RF balun and LO divider. This boosts the port isolation without using external RF or LO components. Furthermore, the LO drive power required for mixing operation is reduced by bias optimization and large-signal LO matching, thus compensating for a shortcoming of passive mixers.

This paper is organized as follows. In Section II, the analysis and design of the distributed drain mixer are described. The measurement results are presented in Section III, followed by the conclusion in Section IV.

II. DISTRIBUTED MIXER DESIGN

A. DRAIN-MIXER UNIT CELL

A unit cell of the drain mixer is shown in Fig. 1. The RF-to-IF conversion is fulfilled by transistor transconductance g_m, which is modulated by LO drive signal at the drain.
Therefore, the IF current at the drain $i_{d,IF}$ is proportional to $g_m'$ given by

$$i_{d,IF} \propto \frac{\partial g_m(v_{gs},v_{ds})}{\partial v_{ds}} \bigg|_{v_{gs}=V_{GS}, v_{ds}=V_{DS}} = g_m'(v_{gs},v_{ds})$$  \hspace{1cm} (1)$$

where $V_{GS}$ and $V_{DS}$ are the dc bias voltages at the gate and drain, respectively. To achieve high conversion gain with low LO drive power, the dc bias condition should be carefully determined, such that $g_m'$ is maximized. In Fig. 2, $g_m'$ of a 2×50-μm enhancement-mode transistor is plotted versus $V_{DS}$ at different values of $V_{GS}$. All simulations were performed using Keysight’s Advanced Design System. It is observed that $g_m'$ shows a peak of 0.273 S/V at $V_{DS} = 0.01$ V and $V_{GS} = 0.6$ V. Since a small dc voltage of 0.01 V at the drain can be easily obtained by LO drive signal, the dc bias condition is set to $V_{DS} = 0$ V and $V_{GS} = 0.6$ V.

The peak $g_m'$ and gate-to-source capacitance ($C_{gs}$) at the optimum dc bias condition are simulated at different transistor sizes in Fig. 3. As the transistor size increases, $g_m'$ increases accordingly and thus improves the conversion gain. However, $C_{gs}$ also increases with a larger transistor size. This limits the cut-off frequency ($f_c$) of artificial transmission line (T-line) of the distributed mixer, thus reducing the operation bandwidth. Therefore, the transistor size should be determined considering the trade-off between the conversion gain and bandwidth.

**B. BALANCED DISTRIBUTED DRAIN MIXER**

A schematic of the balanced distributed drain mixer is shown in Fig. 4. It consists of two single-ended distributed drain mixers, an on-chip LO divider and RF balun, and an off-chip IF balun. In the single-ended distributed drain mixer, three drain-mixer unit cells ($M_1$–$M_3$) are distributed along input T-lines ($TL_1$) and output T-lines ($TL_2$).

The input capacitance of each unit cell ($C_{in}$) is absorbed into $TL_1$, so that an artificial T-line is formed at the input. The characteristic impedance and cut-off frequency of the input artificial T-line are expressed as

$$Z_{0,in} = \sqrt{\frac{L_1}{C_1 + C_{in} / l_1}}$$  \hspace{1cm} (2)

$$f_{c,in} = \frac{1}{\pi l_1 \sqrt{L_1 (C_1 + C_{in} / l_1)}}$$  \hspace{1cm} (3)$$

respectively [18]. $l_1$ is the length of $TL_1$. $C_1$ and $L_1$ are the unit-length capacitance and inductance of $TL_1$, respectively, which are determined by the width of $TL_1$ ($w_1$). In this work, $w_1$ is set to a small value of 5 μm. Since $Z_{0,in}$ is lowered after absorbing $C_{in}$, a small value of $w_1$ helps $Z_{0,in}$ raised back to the RF port impedance, 50 Ω. $l_1$ and $C_{in}$ (which is determined by transistor size) are chosen to achieve low input VSWR and high $f_{c,in}$. According to (2), as $l_1$ increases, $Z_{0,in}$ increases accordingly and thus the input VSWR is reduced. However, $f_{c,in}$ drops with a higher $l_1$ according to (3). Therefore, there is an obvious trade-off between the input VSWR and $f_{c,in}$. In addition, as the transistor size decreases, $C_{in}$ is reduced accordingly, thus improving both the input VSWR and $f_{c,in}$.
FIGURE 4. A schematic of the balanced distributed drain mixer.

FIGURE 5. VSWR and cut-off frequency of the input (a) and output (b) artificial T-lines versus the T-line length at different transistor sizes. *i.e.* achieving a lower VSWR and higher $f_{c,in}$. However, a small transistor size reduces $g_{m}$, thus degrading the conversion gain as mentioned in Section II-A. Therefore, a trade-off among the VSWR, bandwidth, and conversion gain should be considered in choosing $l_1$ and transistor size. In Fig. 5(a), the input VSWR and $f_{c,in}$ versus $l_1$ are simulated at different transistor sizes. In this work, $l_1$ and the transistor size are finally set to 420 $\mu$m and 2x50 $\mu$m, respectively. This results in the input VSWR of 1.2 and $f_{c,in}$ of 32.6 GHz. The output artificial T-line consisting of TL2 and the transistor output capacitance ($C_{out}$) is designed in a similar way to the input counterpart. Since $C_{out}$ is commonly smaller than $C_m$, the length of TL2 ($l_2$) is set to 860 $\mu$m which is larger than $l_1$. This makes the cut-off frequency and group delay of the output artificial T-line close to those of the input artificial T-line. As shown in Fig. 5(b), the output VSWR is 1.05 and $f_{c,out}$ is 20.6 GHz when $l_2 = 860 \mu$m and the transistor size is 2x50 $\mu$m.

To reduce the LO drive power required for the mixing operation, a large-signal impedance matching is performed at the LO port. In Fig. 6, the simulated large-signal return loss is shown as the LO power ($P_{LO}$) varies from -15 to 0 dBm. The return loss is lower than -10 dB from 5.0 to 23.2 GHz at $P_{LO} = 0$ dBm. It also should be mentioned that the effective dc voltage at the drain of $M_1$–$M_2$ is 0.09V when $P_{LO} = 0$ dBm is applied to the transistor. This confirms a small dc drain voltage assumed in Section II-A.
The IF output is extracted from the drain terminal which is shared with the LO input. Thus, a low-pass filter (LPF) consisting of $L_{\text{LPF}}$ and $C_{\text{LPF}}$ is placed to suppress the LO signal at the IF port. The cut-off frequency of the LPF ($f_{c,\text{LPF}}$) is 1.8 GHz. The transistor drain is dc-grounded by $R_D$, so that no dc power is consumed. The design parameter values of the distributed drain mixer are summarized in Table I.

![Chip micrograph of the balanced distributed drain mixer.](image)

**TABLE I**

**Design Parameters of the Distributed Drain Mixer**

| Parameters | Values         | Parameters | Values         |
|------------|----------------|------------|----------------|
| $M_{RF}$-$M_I$ | 2 × 50 $\mu$m | $l_4$      | 50 $\mu$m     |
| $w_2$      | 5 $\mu$m      | $L_{\text{LPF}}$ | 3.3 nH        |
| $l_2$      | 420 $\mu$m    | $C_{\text{LPF}}$ | 2.4 pF        |
| $w_2$      | 10 $\mu$m     | $C_{\text{DC}}$ | 13.7 pF       |
| $l_2$      | 860 $\mu$m    | $C_{\text{mip}}$ | 13.7 pF       |
| $w_3$      | 5 $\mu$m      | $Z_{\text{term}}$ | 50 $\Omega$  |
| $l_1$      | 50 $\mu$m     | $R_D$      | 2.34 k$\Omega$ |
| $w_4$      | 5 $\mu$m      | $R_{\text{th}}$ | 51 $\Omega$  |

Although an LPF is inserted at the output of each single-ended mixer, the LO-to-IF isolation would be degraded as the LO frequency approaches $f_{c,\text{LPF}}$. To improve the isolation, a balanced structure with two single-ended mixers combined is employed in this work. The two single-ended mixers are driven by differential RF signals which are generated by an on-chip Marchand balun. The amplitude and phase imbalance of the balun are no more than 1 dB and 7°, respectively, from 5.4 to 21.8 GHz.

Contrary to the RF input, the LO input is divided into two in-phase signals by an on-chip current divider. The current divider presents return loss and amplitude imbalance of no more than -10.2 dB and 1.3 dB, respectively, from 5.4 to 21.8 GHz. Accordingly, the IF signals of the single-ended mixers are generated in a differential manner ($IF_{\text{out}}^+$ and $IF_{\text{out}}^-$) and then are combined by an off-chip IF balun. It is noted that the LO leakage at the differential IF ports are in-phase to each other and thus are spontaneously canceled out at the IF balun output. Therefore, the LO-to-IF isolation is significantly improved compared to a single-ended mixer.

The LO-to-RF isolation is also improved in the same manner.

**III. MEASUREMENT RESULTS**

The balanced distributed drain mixer is fabricated in WIN Semi’s 0.25- $\mu$m GaAs p-HEMT technology providing enhancement-mode transistors with $f_T$ = 75 GHz. The chip micrograph is shown in Fig. 7. The chip area is 2.0 × 3.2 mm² including probing pads.

The measured and simulated conversion gain of the balanced mixer versus RF frequency is shown in Fig. 8(a). The IF frequency and LO power are fixed to 0.4 GHz and 2 dBm, respectively. Even with such low LO power, the balanced mixer shows conversion gain of -4.0 to -7.4 dB over the RF frequency from 5.4 to 21.8 GHz. The higher bound of the bandwidth is limited by the on-chip RF balun integrated in the mixer. In Fig. 8(b), the conversion gain versus IF frequency is plotted when the LO frequency is fixed to 10 GHz. The 3-dB IF bandwidth of the mixer is 1.6 GHz.
The IF output power and conversion gain of the balanced drain mixer versus RF input power are shown in Fig. 9. For comparison purpose, a test cut of the single-ended drain mixer is separately measured and superimposed in Fig. 9. The RF and IF frequencies are fixed to 10.4 and 0.4 GHz, respectively. The input 1-dB compression power (IP_{1dB}) of the single-ended and balanced mixers are -12.2 and -8.2 dBm, respectively. By combining two single-ended mixers, the balanced mixer is supposed to exhibit a higher linearity than the single-ended mixer by 3 dB in principle.

The LO-to-IF and LO-to-RF isolation of the two mixers are compared in Fig. 10. The single-ended mixer shows isolation less than 29.2 and 15.3 dB, respectively, over the frequency from 5.4 to 21.8 GHz. On the other hand, the balanced mixer achieves higher isolation, no less than 54.7 and 23.5 dB, respectively, over the same frequency band. This is attributed to the spontaneous cancellation of LO signal at the IF and RF ports in the balanced mixer structure.

Table II summarizes and compares the performance of this work with previously published distributed mixers. Adopting a passive topology, this work consumes no dc power but achieves high conversion gain comparable to those of other mixers. Compared to other zero-dc mixers [9,10], the LO power (P_{LO}) of this work is substantially low, i.e., 2 dBm. This eliminates the need of an additional LO drive amplifier which would consume high dc power. Furthermore, by adopting a balanced structure integrating an on-chip RF balun and LO divider, this mixer achieves excellent isolation performance, particularly showing the highest RF-to-IF isolation (>54.7 dB).

### IV. CONCLUSION
In this paper, a balanced distributed drain mixer with zero dc power consumption is presented. The conversion gain, impedance matching, and bandwidth of the mixer are enhanced by optimizing the transistor size, bias and the distributed T-line length. A balanced distributed mixer combines two single-ended mixers with an on-chip RF balun and LO divider integrated for enhancing the LO isolation at the IF and RF ports. The balanced distributed drain mixer achieves high conversion gain at the lowest LO drive power compared to other distributed mixers while consuming no dc power. This would eliminate the need of an additional LO drive amplifier before the mixer. Hence, the mixer will be suitable for low-power and broadband receivers.

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