High Performance P-Type Perovskite LaGaO$_3$ Thin Film Field Effect Transistor Prepared by Solution-Processed

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Abstract. Metal oxide semiconductor (MOS) is essential to compose high-performance electronic devices, however, the investigation on p-type MOS is relatively rare compared with its n-type counterpart. In this work, LaGaO$_3$ thin films with superior p-type conductivity have been prepared via a facile solution process. Moreover, we have implemented Al$_2$O$_3$ and SiO$_2$ as the dielectric of the p-channel LaGaO$_3$ thin film transistors (TFTs) annealed at different temperatures. Particularly, the LaGaO$_3$/Al$_2$O$_3$ TFTs annealed at 700 °C exhibit an ultrahigh hole mobility of 12.4 cm$^2$V$^{-1}$s$^{-1}$. Under the same conditions, LaGaO$_3$/SiO$_2$ thin film transistor is two orders of magnitude higher than LaGaO$_3$/SiO$_2$ thin film transistor. The advanced p-type characteristics of the LaGaO$_3$ thin film, along with its facile low-cost fabrication process can shed new light on future design of high-performance complementary MOS circuit with other optimized facile-integrated dielectrics.

Keywords: Perovskite LaGaO$_3$ Thin Film, P-Type Semiconductor, Thin Film Transistor, Sol-Gel Method.

1. Introduction
Thin film transistors (TFTs) based on metal oxide semiconductor (MOS) have attracted remarkable attention due to the intrinsic merits of high optical transparency and excellent electrical properties.$^{[1,2]}$ In the past few years, great endeavors have been made in the investigation of n-channel TFT with excellent performance. However, the exploration on the p-type TFT is far beyond mature, the main obstacles for the rare research of p-type oxide are as follows: (1) there have been no efficient methods to synthesize high-quality p-type MOS; (2) the choices for p-channel MOS are limited, to the best of our knowledge, only Cu$_x$O$^{[3,4]}$, SnO$^{[5,6]}$, NiO$^{[7]}$, CuMO$_2$ (M = Al, Ga, or Cr)$^{[8-10]}$ and their mixtures$^{[11,12]}$ or laminates$^{[13]}$ have been reported to exhibit p-type conductivity. However, these reported p-type MOS based TFT exhibited unsatisfied electrical performance, usually with the mobility standing an order of magnitude behind their n-type counterparts. The factors responsible for the inferior carrier mobility of p-type oxide semiconductor have been proposed. Firstly, the p-type MOS based on Cu$_2$O and SnO, which is unstable in air, could easily convert into the corresponding CuO and SnO$_2$, deteriorating the hole transport$^{[11]}$. Secondly, the anisotropic and strongly localized oxygen 2p orbitals lead to a large electro-negativity in the valance band maximum (VBM), resulting in a large effective hole mass and hence a low mobility$^{[14]}$. These drawbacks inhibit p-type MOS being applied in complementary metal oxide semiconductor (CMOS) circuit, which is the essential component in the next-generation displays$^{[15]}$. In this regard, it still remains a great challenge to develop p-type MOS with high carrier mobility comparable to their n-type counterparts.
In recent years, perovskite-structured oxides LaCrO$_3$ as p-type materials have attracted considerable attention owing to their high hole concentration (~ $10^{21}$ cm$^{-3}$). LaGaO$_3$ as a semiconductor material with p-type properties, is also one of the potential materials for preparing p-type metal oxide thin film transistors. In the current research report, thin film transistors using LaGaO$_3$ thin film as semiconductor layer have not been studied. Recently, it has been reported that perovskite NdAlO$_3$ thin films with excellent properties have been successfully prepared by solution method, and the integrated devices show good p-type semiconductor properties, which is realized by vacancy engineering [16]. This inspired us to explore the possibility of using sol gel method to prepare LaGaO$_3$ thin films and integrate thin film transistors. In this report, LaGaO$_3$ thin films with perovskite structure were prepared by a low-cost solution method. It is found that the LaGaO$_3$ films annealed at various temperatures exhibit p-type characteristics, and p-channel TFTs based on LaGaO$_3$ films are integrated as channel layers. When high-k dielectric Al$_2$O$_3$ is introduced instead of SiO$_2$ as the dielectric layer, the electrical properties of LaGaO$_3$/Al$_2$O$_3$ based TFTs are significantly improved, indicating that LaGaO$_3$ has great potential in constructing new electronic devices into new p-type semiconductors.

2. Experiment

2.1 Precursor Solution Preparation
To prepare the precursor solution for LaGaO$_3$ thin films, La(NO$_3$)$_3$•6H$_2$O, 99.9%, Aladdin and aluminum nitrate nonahydrate (Ga(NO$_3$)$_3$•xH$_2$O, 99.99%, Aladdin) with a molar ratio of 1:1 were dissolved into 10 mL N,N-dimethylformamide (DMF, 99.5%, Aladdin). The precursor solution for Al$_2$O$_3$ dielectric was prepared by dissolving the Al(NO$_3$)$_3$•9H$_2$O into DMF and a uniform transparent solution with a concentration of 0.1 M was obtained. All the precursor solutions were stirred vigorously overnight at ambient environment to obtain homogenous solution.

2.2 Thin Film Fabrication and Device Integration
The resistivity of heavily doped silicon is 0.001 $\Omega$•cm as substrate, the substrate was cleaned in acetone solution, ethanol and deionized water, and then dried with N$_2$ gun, the treated Si wafer acts as the bottom gate electrode of the devices. A syringe with a diameter of 0.22 μm and a filter were used to filter the precursor solution, and then the solution was dropped onto the substrate for 3s at a speed of 500rpm and 15s at a speed of 5000rpm for spin coating. The substrate coated with precursor film was baked on hot plate for 10 minutes and then the films were treated with UV for 40 minutes, finally thermal annealing at 800°C for 2h to obtain the compact dielectric thin film.

Figure 1 shows the fabrication process of the LaGaO$_3$ thin films. In order to fabricate the p-channel TFTs based on LaGaO$_3$ thin films, the obtained LaGaO$_3$ precursor solution was spin-coated on the SiO$_2$/Si or Al$_2$O$_3$/Si substrates with a rotation speed of 5000 rpm for 20 s. The gel films were then treated in UV illumination for 40 minutes and a low-temperature baking at 150°C for 10 min. The pretreated gel films were then annealed in nitrogen ambient in a furnace at various annealing temperatures ranging from 400 to 800°C for 120 min. Finally, the nickel source/drain electrodes are deposited on the film by thermal evaporation using the shadow mask, and the channel length (L) is 100 μm. And width (W) is 1000 μm.

2.3 Device Characterization
The surface roughness of the films prepared by solution method was characterized by atomic force microscopy (AFM). X-ray diffractometer (XRD) with a Cu Kα1 radiation was utilized to characterize the crystal structures of LaGaO$_3$ thin films. The electrical properties of the fabricated TFTs were tested in a dark box with Keithley 2634b
3. Results and Discussion

![Figure 1. Schematic illustration of the TFT fabrication process](image)

Figure 1. Schematic illustration of the TFT fabrication process

Figure 2(a) shows the XRD pattern of the LaGaO$_3$ thin films annealed at various annealing temperatures. The amorphous peak located at around 28° is originated from the quartz substrate. It can be seen from the figure that the crystallinity of LaGaO$_3$ is sensitive to the annealing temperature. There is no obvious diffraction peak in LaGaO$_3$ films annealed below 700 °C, indicating the amorphous nature of LaGaO$_3$ films. When the annealing temperature reaches 800 °C, the annealing temperature is 22.8, 32.5, 40.2, 46.7, 48.2, 52.6, 57.9, 68.2 and 77.5 °C The diffraction peaks observed at (110), (112), (022), (004), (023), (310), (312), (400) and (420) 

\[17\] belong to the crystal orientations of LaGaO$_3$ (jcpds No. 24-1102) (110), (112), (022), (004), (023), (310), (312), (400) respectively. An additional second phase peak of La$_4$Ga$_2$O$_9$ was observed. As we all know, perovskite materials are generally thermodynamically stable, which leads to the need for relatively high annealing temperature (>700 °C) in the formation of crystalline phase. \[18\] High annealing temperature (800 °C) provides enough heat energy, and LaGaO$_3$ thin films transfer from amorphous state to polycrystalline state with a large number of grain boundaries \[19\]. The grain boundary is the defect and scattering center, which greatly affects the carrier transport \[16\].

![Figure 2. (a) XRD pattern of LaGaO$_3$ thin films annealed at different temperatures](image)

Figure 2. (a) XRD pattern of LaGaO$_3$ thin films annealed at different temperatures

Figure 3 (A-E) shows the surface morphology of LaGaO$_3$ films annealed under different annealing conditions. The root-mean square (RMS) roughnesses of LaGaO$_3$ films annealed at 400, 500, 600, 700 and 800 °C are 3.37, 2.43, 1.64, 0.427 and 0.382 nm, respectively. RMS roughness of LaGaO$_3$ films
increases with annealing time the temperature decreases monotonously (Fig. 3F), this is due to the increase of surface energy. As we all know, the surface roughness of thin films has a profound impact on the size of interface trap density and the quality of electrical contact, thus determining the electrical performance of its electronic devices [20]. Therefore, the smoother surface of the annealed LaGaO₃ films, the more favorable the charge carrier transport, which is very important for the application of transistors.

![AFM images of LaGaO₃ thin films annealed at various temperatures.](image)

**Figure 3.** AFM images of LaGaO₃ thin films annealed at various temperatures. (a)-(e) 400 °C- 800 °C. (f) RMS values of LaGaO₃ thin films

In order to verify the potential of LaGaO₃ thin films as channel materials, the transistors were integrated based on LaGaO₃ thin films annealed at different temperatures were prepared on Si/SiO₂. Figure 4 shows the transfer characteristic curve of TFT based on LaGaO₃ thin films annealed at different temperatures. It is clearly observed that the drain current is increased with the gate voltage sweeping from 0 to -60 V, which demonstrates the typical p-channel characteristics. The key electrical parameters of the TFTs, including field-effect mobility ($\mu_{FE}$) and threshold voltage ($V_{TH}$) are extracted and presented in Fig. 3(c). It can be seen from Fig. 3(a) and 3(c) that, with increasing the annealing temperature from 400 to 700 °C, both $\mu_{FE}$ and $I_{on}$ are increased significantly, and the $V_{TH}$ is observed to be increased positively from -53 V to -38V. The enhanced device performance is attributed to the improved morphology and interface quality. However, for the TFT annealed at 800 °C, the electrical performance of the device is apparently deteriorated, with a low $\mu_{FE}$ of $0.09 \times 10^2$ cm² V⁻¹ s⁻¹ and a small $I_{on}/I_{off}$ of $2 \times 10^4$. 
Figure 4. (a) Transfer curves of TFTs based on LaGaO$_3$ thin films annealed at different temperatures. (b, c) Corresponding electrical parameters of the LaGaO$_3$ TFTs.

Figure 5. (a) Negative bias voltage transfer curve of LaGaO$_3$/SiO$_2$ TFT at the optimal annealing temperature (700°C).

We further studied the bias voltage stability of the device, and performed a 2000s negative bias voltage ($V_{GS}=-30V$) stability test on LaGaO$_3$/SiO$_2$ TFTs annealed at 700°C. The result is shown in
Figure 5. The negative gate voltage of 2000s is continuously applied to the device. The result shows that there is a small threshold voltage shift ($\Delta V_{TH} = 0.64V$), and the slope of the sub-threshold voltage hardly changes. It can be seen from this result that the main factor causing the $V_{TH}$ shift is the charge trapping effect at the interface $^{21}$ When a continuous negative bias is applied to the device, it is found that extending the gate voltage application time makes the on-state current of the device is a small amount of attenuation. Compared with holes, the number of electrons in the P-channel semiconductor channel is negligible. Under the negative gate pressure, as the gate voltage time is extended, the interface state is gradually filled, and the trapped holes on the surface of the LaGaO$_3$ film may produce phonons or coulomb scattering, thereby suppressing the state current $^7$.

In order to improve the electrical performance and achieve the low-voltage operation of the device based on p-channel LaGaO$_3$, it is of great significance to integrate gate dielectrics with high permittivity into the TFTs. In the literature, a series of solution-processed high-k oxide dielectrics had been fabricated and were integrated into the TFTs so as to achieve the high-performance electronic devices $^{22-24}$. Among these reported high-k dielectric thin films, Al$_2$O$_3$ is regarded as one of the most promising candidates to replace traditional SiO$_2$ as dielectric, due to its proper permittivity (~9), high quality, good chemical stability and high crystallization temperature (~1000 °C) $^{23}$. In this work, Al$_2$O$_3$ dielectric thin film was prepared by spin-coating Al(NO$_3$)$_3$ on the Si substrate (Fig. 6a), and then annealed at 800 °C. The prepared Al$_2$O$_3$ dielectric thin film exhibits a large capacitance density ($C_i$) of about 97 nF cm$^{-2}$ at 20 Hz $^{16}$. The characteristic transfer curves of the TFTs based on LaGaO$_3$ thin films annealed at 400-800 °C with Al$_2$O$_3$ dielectrics are shown in Fig. 4(b), the electrical parameters extracted from the transfer curves are listed in Table 1. As can be seen that, compared with the TFTs fabricated on SiO$_2$/Si substrate, the TFTs with Al$_2$O$_3$ dielectric exhibit much improved electrical performance. TFT based on LaGaO$_3$ films annealed at 700 °C It shows the highest electrical performance, including 12.4 cm$^2$V$^{-1}$s$^{-1}$ ultra-high mobility, $V_{TH}$ of -0.2V, excellent of $I_{on}$/I$_{off}$ 9.8*10$^6$ and significantly reduced operating voltage 10V. For the LaGaO$_3$/Al$_2$O$_3$ based TFTs, due to the reduction of hole traps at the interface of LaGaO$_3$/Al$_2$O$_3$ and the improvement of the quality of LaGaO$_3$ thin films, $V_{TH}$ can be improved. It increases with annealing temperature. The significant enhancement of the electrical properties of TFTs can be attributed to the large area capacitance of Al$_2$O$_3$,It allows more carriers to accumulate to achieve low operating voltage and high electrical performance. It is realized in this work. The hole mobility of TFT is the first report of p-type oxide semiconductor based on solution process One of the highest values recorded.

Figure 6. (a) Schematic diagram of solution-processed Al$_2$O$_3$ high-k dielectric layer. (b) Transfer characteristics of LaGaO$_3$/Al$_2$O$_3$ TFT annealed at different temperatures
Table 1. Comparison of electrical parameters of the TFTs based on LaGaO₃ annealed at different temperatures with SiO₂ and Al₂O₃ dielectrics

| Dielectric | Temperature(°C) | μFE (cm²V⁻¹s⁻¹) | I_on/I_off | I_ON(A) | V_TH(V) |
|------------|----------------|-----------------|-----------|---------|---------|
| SiO₂       | 400            | 0.62*10⁻³        | 32        | 2.76*10⁻⁹ | -53    |
|            | 500            | 0.0053           | 467       | 4.26*10⁻⁸ | -50    |
|            | 600            | 0.17             | 5.7*10⁴   | 1.34*10⁻⁶ | -39    |
|            | 700            | 0.92             | 2*10⁵     | 3.75*10⁻⁵ | -38    |
|            | 800            | 0.09             | 2*10⁴     | 5.24*10⁻⁶ | -44    |
| Al₂O₃      | 400            | 0.16             | 3.97*10⁵  | 3.97*10⁻⁷ | -2.78  |
|            | 500            | 0.58             | 1.5*10⁴   | 2.56*10⁻⁶ | -2     |
|            | 600            | 7.89             | 4.7*10⁵   | 5.87*10⁻⁵ | -1.08  |
|            | 700            | 12.4             | 9.8*10⁸   | 1.38*10⁻⁴ | -0.2   |
|            | 800            | 0.76             | 6.39*10⁴  | 8*10⁻⁶   | -0.35  |

4. Conclusion

In summary, a facile and cost-effective solution process was employed to fabricate the perovskite-structured LaGaO₃ thin films, which exhibit excellent p-type conductivity. With the aim of investigating the electrical properties of the solution-processed LaGaO₃ thin films, the transistors based on LaGaO₃ annealed at different temperatures have been successfully fabricated on Si/SiO₂ substrate, and possess typical p-channel transistor behavior. When the high-k dielectric Al₂O₃ was integrated into the device, the electrical performance of the TFT has been enhanced dramatically. Surprisingly, under the same optimized anneal temperature (700 °C), the field-effect mobility increases from 0.92 (LaGaO₃/SiO₂ TFT) to 12.4 cm²/V s (LaGaO₃/Al₂O₃ TFT).

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