A generic FPGA-based detector readout and real-time image processing board

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ABSTRACT
For space-based astronomical observations, it is important to have a mechanism to capture the digital output from the standard detector for further on-board analysis and storage. We have developed a generic (application-wise) field-programmable gate array (FPGA) board to interface with an image sensor, a method to generate the clocks required to read the image data from the sensor, and a real-time image processor system (on-chip) which can be used for various image processing tasks. The FPGA board is applied as the image processor board in the Lunar Ultraviolet Cosmic Imager (LUCI) and a star sensor (StarSense) — instruments developed by our group. In this paper, we discuss the various design considerations for this board and its applications in the future balloon and possible space flights.

Keywords: Detector, FPGA Spartan-6Q, Image processing, CCD, CMOS, star sensor, Lunar Ultraviolet Cosmic Imager

1. INTRODUCTION
Data generated in astronomical payloads in space or high-altitude balloon is large in size. To download this data through the limited downlink capability available on a satellite or a high-altitude balloon, the on-board processing of the data is required to reduce its size. We have developed an FPGA-based generic board which can be used for this task, and this utility can be implemented in various digital interfaces without much change in the hardware.

For any image processing board, some of the basic required components are a controller for image acquisition from the detector, RAM for temporary storage of the images, a microprocessor for processing the image data, and a permanent memory for on-board storage. Our FPGA board combines all of these requirements. This board can be used to read the digital output from any standard semiconductor detector, e.g. CMOS or CCD. The acquired image is sent to RAM, and is processed by the microprocessor embedded in the FPGA. The processed image is stored in a long-term memory (SD card), and can be either transmitted to ground station from space, or retrieved in case of a balloon flight. In Section 2 we describe the steps followed to design the board. A brief description of the image sensors that can be used in conjunction with this board is given in Section 3, and a brief description of algorithms for different image processing tasks to pinpoint the processing capabilities of the board is presented in Section 5. The conclusions and future applications of this processing board are given in the Section 6.

2. FPGA BOARD DESIGN
2.1 Components of the FPGA board
This board was developed as a generic application with intentions to use it as an image processor board in the flight instruments developed by our group — Lunar Ultraviolet Cosmic Imager (LUCI)[1, 2] and a star sensor StarSense[3, 4]. The board is to be interfaced with the ultraviolet (UV) CCD on LUCI, and with a radiation-hardened CMOS sensor Star1000 on StarSense. The characteristics and readout sequences of these sensors are described later in Section 3.

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The main components of the FPGA board are shown in Table 1 and their layout is shown in Fig. 1. An FPGA is an integrated circuit designed to be configured by a programmer, or end user, to carry out a specific set of tasks. An FPGA contains programmable logic components called logic blocks, and a hierarchy of re-configurable interconnects that allow the blocks to be wired together to form different configurations. We have selected a MIL-grade Spartan-6Q FPGA from Xilinx* because of its wide operating temperature range. The program for the FPGA is written in a hardware description language called Verilog. We also implement a soft core microprocessor†, called microblaze, inside the FPGA. The program for microblaze is written in C. The Verilog code is synthesized and a configuration program is generated using the programming toolsuite ISE from Xilinx. The configuration program for the FPGA is known as a bitstream. The FPGA consists of configurable logic blocks where the configuration is volatile, that is the FPGA has to be reprogrammed at each power cycle. We have selected a Master Serial programming interface for the FPGA, wherein the FPGA reads its bitstream from a flash memory on its own using a serial transfer protocol, called serial peripheral interface (SPI), and configures itself. The size of the bitstream determines the size of the flash memory chip. In our case, for a Spartan-6Q FPGA device, the bitstream size is 4 MB. Other than the bitstream, the flash memory can be used to store data that should be permanently available to the FPGA e.g. a star catalog, some configuration parameters for the payload, etc. Therefore we have selected a flash memory chip of 8 MB. The image sensors which we use typically have a size of 1024 × 1024 pixels, each pixel with a 10-bit digital value. This corresponds to an image size of ~1.2 MB being processed by the FPGA every 100 ms. We have selected a 64 MB RAM, which is sufficient for image processing tasks on images from the selected detectors. For the permanent storage of processed data, we use an SD card of 32 GB. The FPGA board can be connected to the on-board computer (OBC) of a satellite, or a balloon payload, through the standard RS485 protocol. During the development cycle, the FPGA can be connected to a computer through a USB port.

![Figure 1. Block diagram of the FPGA board](image)

### 2.2 Voltage regulators

The FPGA board can be powered by an external computer (a laptop, a satellite/balloon OBC) through either a USB cable or through a DB-9 (9 pins) connector (Fig. 1). In addition to this, it can also be powered by a DC jack provided on the board. The FPGA needs 3 different voltages: 3.3 V, 2.5 V and 1.2 V. It needs 3.3 V for general-purpose input/output pins, image sensor interface, SD card, flash memory interface, and RS485 interface. Voltage of 2.5 V is needed to connect to the SDRAM. Finally, it needs 1.2 V for its internal functioning. All these voltages are generated from the unregulated 5 V input through the voltage regulators. The regulated

*http://www.xilinx.com
†http://www.xilinx.com/products/design_resources/proc_central/microblaze_faq.pdf
Table 1. Technical Specifications of the FPGA board

| Component                              | Specifications                     |
|----------------------------------------|------------------------------------|
| FPGA                                   | Spartan-6Q (XQ6SLX150T-2FGG484)    |
| Size (mm)                              | 65 × 65                            |
| Weight                                 | 50 gms                             |
| Power                                  | 3 W                                |
| RAM†                                   | 64 MB SDRAM (MT46V32M16)           |
| Flash memory†                          | 8 MB chip (N25Q064A)               |
| SD card                                | 32 GB                              |
| Connectivity to the On-Board Computer  | RS485 (MAX481), USB-to-UART (FT232) |

† Micron Technology, Inc., USA. [https://www.micron.com/](https://www.micron.com/)

The voltage output should be switched on in a sequence to ensure successful programming of the FPGA. The FPGA is set in master serial configuration mode, and therefore, the flash memory chip should be powered on and ready to accept memory read commands, before the FPGA starts sending them. Therefore, the voltage regulators are connected in a chain as shown in Fig. 2. The programmable soft-start feature of the voltage regulator ensures that the flash memory is powered on at least 3 ms prior to the FPGA, and is ready to accept read commands from the FPGA. The image sensors require a 5 V supply, which can be switched on or off in order to reduce power consumption, when not in use. We do not use the 5 V input directly, instead a boost regulator is used to increase the voltage from 3.3 to 5 V. Such configuration gives a more stable voltage for the image sensors, which are the critical part of the circuit.

![Figure 2. Power supply for the FPGA board](image)

3. IMAGE SENSORS

The image sensors in LUCI and *StarSense* are directly connected with the FPGA board. LUCI uses a CCD sensor (ICX407BLA) from Sony, which is sensitive in ultraviolet wavelengths, and *StarSense* uses a radiation-hardened CMOS sensor (NOIS1SM1000A) from ON Semiconductors. Details of these image sensors are given in the following subsection.

3.1 Ultraviolet CCD

The UV CCD is a diagonal 8 mm (type 1/2-inch) interline CCD solid-state image sensor with a square pixel array and 1.45 Megapixels (Mp). Its technical details are shown in Table 2. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images. The effective quantum efficiency of this detector in near-UV wavelengths (200 to 400 nm) is approximately 20%.
This camera has a stack of 3 PCBs. First PCB contains the UV CCD and the timing generator chip, which is required to generate reset clocks and transfer clocks required for the CCD (Fig. 3, Left and Middle). Second PCB contains the voltage regulators to provide various voltages for reset gate, vertical transfer and horizontal transfer clocks. Third PCB contains its own FPGA which transmits the digital data received from the CCD PCB to the computer through USB. This PCB does not store the image data on-board or process it. We have used the CCD PCB and the voltage regulator PCB as is and connected our FPGA board to them.

| Sensor                      | ICX407BLA UV CCD | NOIS1SM1000A Star1000 |
|-----------------------------|------------------|-----------------------|
| Array size (mm)             | 6.47 × 4.83      | 15 × 15               |
| Total number of pixels      | 1360 × 1024      | 1024 × 1024           |
| Pixel size (µm)             | 4.65 × 4.65      | 15 × 15               |
| Frame rate (fps)            | 12               | 11                    |
| Voltage                     | 5 V              | 5 V                   |
| Power consumption           | 2 W              | 0.4 W                 |

Figure 3. Left, Middle: Photos of the UV CCD PCB, front and back side, respectively. Right: A photo of the STAR1000 image sensor chip.

### 3.2 Star1000

A star sensor is a critical sensor in satellite or balloon missions. The image sensor is the only electronics part which is open to incident radiation. Degradation of the detector quality with exposure to intense radiation cannot be tolerated and therefore, a radiation-hardened CMOS image sensor STAR1000‡ was selected for this application (Fig. 3, Right). Its technical details are shown in Table 2. It can also support the readout of small windows of a whole image at much faster frame rates. The sensor features the on-chip fixed-pattern noise (FPN) correction, a programmable gain amplifier, and a 10-bit analog-to-digital converter (ADC). The registers, which contain X— and Y—addresses of the read out pixels, can be directly accessed by an external controller. This architecture provides flexible operation and allows different operation modes, such as (multiple) windowing, sub-sampling, and so on.

### 4. READOUT PROCESS

An image sensor is essentially an array of photodiodes (pixels) which measure the light intensity at each pixel. The output of each pixel is an analog voltage. Each pixel is connected to an output amplifier on the chip through digital circuitry. The clock signals control this digital circuitry and manage the sequence of connections. The analog voltage of the output amplifier is converted to a digital value by an ADC. The external FPGA, or a

‡ON Semiconductors, USA. [http://www.onsemi.com](http://www.onsemi.com).
controller, generates all the clock signals to control the digital circuit and ADC, and captures the digital output from the ADC. Figure 4 gives a general outline of this process. The process of collecting digital data (a measure of the light intensity on each pixel) is called the readout process. In this section, we describe how the readout process is implemented for both sensors.

![Figure 4. General schematics of a readout process.](image)

4.1 UV CCD

As mentioned in Section 3.1, there is a timing generator chip VSP01M01 along with the image sensor on the same PCB. The required timing for various clock signals are to be programmed on the chip when the circuit is switched on. This programming is done by the microblaze, implemented on the FPGA board using SPI protocol. The timing generator chip includes the digital circuitry to access the analog voltage from each pixel and an ADC. It also generates image synchronization driver signals (frame-valid, line-valid, and pixel clock) which are received by the FPGA board. The FPGA board captures digital value of each pixel and decodes the position of the pixel in the image using these signals. Figure 5 shows a layout of UV CCD readout circuit.

![Figure 5. A layout of the UV CCD readout circuit.](image)

4.2 Star 1000

The Star1000 image sensor does not have a timing generator chip like the UV CCD. Therefore, we have to generate the clock signals for various pins on the image sensor from the FPGA using Verilog code. The image sensor consists of 5 basic modules as shown in Fig. 6:

1. Pixel array.

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³Texas Instruments, USA. www.ti.com
2. X–Y-addressing logic.
3. Column amplifier.
4. Output amplifier.
5. Analog to Digital Converter (ADC).

The pixel array is the light-sensitive part of the image sensor. It consists of 1024 × 1024 pixels each of size 15 µm × 15 µm (Table 2). The pixel to be read out is selected using the address value given on the address bus and a proper signal to the $Ld_X$ and $Ld_Y$ pins (Fig. 6). The $X$– and $Y$– addressing logic decodes the location of the pixel from the address bus. The column amplifier samples the output voltage and the reset level of the pixel whose row is selected, and presents these voltage levels to the output amplifier. The output amplifier combines subtraction of pixel signal level from reset level with a programmable gain amplifier. Finally the ADC converts the analog output from the output amplifier to a digital value. It converts the analog value to a 10-bit digital value which can be sampled by the FPGA. The FPGA board is programmed to generate clock signals to control these modules. These clock signals control the image acquisition from the image sensor.

The image acquisition process is implemented into two separate processes: reset and readout. The reset process can be done row-wise and the readout process can be done pixel-wise. The readout process is done in two parts: row readout and pixel readout. The clock signals for reset process, row readout process, and pixel readout process are described below. A general sequence for the readout of the image sensor is shown in Fig. 7.

- Row reset sequence: A row in the image sensor can be reset by the following sequence (illustrated in Fig. 8):
  1. Place proper $Y$–address on address pins.
  2. Assert $Ld_Y$ and latch the address into the internal decoder circuitry.
3. Pulse the ‘Reset’ pin so that the internal decoder circuitry resets the \( Y \)–row in the image sensor.

- Row readout sequence: After reset process is done and after the integration time is elapsed, each row must be read. By this process, the outputs of the pixels in the row are connected to an array of column amplifiers. The signals required to achieve this are illustrated in Fig. 9:
1. Place proper \( Y \)-address on address bus.

2. Assert \( Ld \_Y \) and latch the \( Y \)-address into the internal decoder circuitry.

3. Pulse \( S \) signal which will sample values from all column pixels in the row into the column amplifier. This is the signal value after the integration time.

4. Pulse ‘Reset’ to reset the row in the pixel array.

5. Pulse \( R \) signal which will sample the reset values of all column pixels in the row into the column amplifier. Eventually the output amplifier takes the difference between the reset level and the signal level and sends the analog output.

- ‘Cal’ pulse to initialize the output amplifier: For every frame there at the first row readout, the ‘Cal’ signal should be pulsed (illustrated in Fig. 10). This gives the black reference (defined by the analog level at ‘Blackref’ pin) value as output and thus calibrates the complete frame readout. The position of ‘Cal’ pulse is with respect to the \( S \) pulse and can be checked in the datasheet.

![Figure 10. Timing diagram for Cal pulse in row readout process](image)

- Pixel Readout/Column readout sequence: This process connects each pixel sequentially to the output programmable gain amplifier and gives reset pulses for the ADC to start conversion. The timing diagram for this process is illustrated in Fig. 11.

5. REAL TIME IMAGE PROCESSING

The microblaze implemented on the FPGA can achieve a maximum performance of approximately 950 DMIPS, when operating at 100 MHz. This is sufficient to implement various image processing tasks for 1 Mp images captured by the sensors. Image processing tasks required in StarSense are explained in this section.

A star sensor is a wide-FOV camera with online image processing capabilities which reduces the image data to an attitude quaternion that describes the rotation of the sensor coordinate system with respect to the Earth-centered inertial (ECI) coordinate system. This is achieved by processing the images using multiple algorithms in sequence, implemented on the microblaze microprocessor. All stars are point sources for the star sensor optics. The PSF of the optics is spread over \( 4 \times 4 \) pixels on the detector. To pinpoint the location of a star, we use centroiding algorithm to calculate the position of the star images on the detector plane. Geometric voting algorithm compares the geometric patterns of the star centroids in the image with geometric patterns of stars in a catalog. In our case, the algorithm compares angles between all the pairs of stars in image with those in the catalog. A binary search method is used to find matches. After identifying the imaged stars, the quaternion of the rotation between the sensor coordinate system and ECI coordinate system is calculated by QUEST algorithm. These algorithms and their estimated performance are described in detail in a forthcoming paper (Ref. 6).
6. CONCLUSION AND FUTURE WORK

We have developed a generic (application-wise) FPGA board to be used as image processor board on any space-based image sensor. This board includes a method to generate the clocks required to read the image data, and a real-time image processor system which can be used for image processing tasks of different levels. Our immediate application is a UV telescope placed on the Moon (LUCI) and a star sensor StarSense for minisatellites such as e.g. CubeSats.

The interface of this FPGA board with the star sensor StarSense is complete, and calibration and testing is in progress. We have also completed the interface with the UV CCD on LUCI, and currently we are working on high-level data processing tasks implementation, such as, for example, obtaining light curves from time series data of astronomical objects and storing them on-board.

In future, we are planning to use this FPGA board to operate an MCP-based detector employed on astronomical instruments that are currently in development (UV telescope and UV spectrograph, see Ref. 7).

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REFERENCES

[1] M. Safonova, J. Mathew, and R. Mohan, “Prospect for uv observations from the moon,” ApSS 353, 329 (2014).
[2] J. Mathew, A. Prakash, M. Sarpotdar, et al., “Ultraviolet cosmic imager to study bright uv sources,” SPIE Astronomical Telescopes + Instrumentation, Space Telescopes and Instrumentation 9905-146 (2016).

[3] M. Sarpotdar, J. Mathew, A. Prakash, et al., “Design and development of a stars sensor - starsense,” ASI Meeting Srinagar (2016).

[4] M. Sarpotdar, J. Mathew, A. Sreejith, et al., “Design and development of a star sensor-cum-asteroid tracker,” SPIE Astronomical Telescopes + Instrumentation, Space Telescopes and Instrumentation (2016).

[5] O. Semiconductors, “Datasheet star1000 1 megapixel radiation hard cmos image sensor,” ON Semiconductors, Phoenix, Arizona, USA (January 2015).

[6] M. Sarpotdar, J. Mathew, A. Sreejith, et al., “Performance estimate of star sensor algorithms,” submitted to Experimental Astronomy (2016).

[7] A. Sreejith, J. Mathew, M. Sarpotdar, et al., “Balloon uv experiments for astronomical and atmospheric observations,” SPIE Astronomical Telescopes + Instrumentation (2016).