An ultra-low power, low temperature coefficient voltage reference generator used for nanowatt-level passive sensor systems is presented. The voltage reference configuration, based on a voltage reference generating circuit embedded in the feedback loop, realises an average reference voltage \( V_{ \text{REF} } \) of 837.2 mV and 40 \( \mu \)A maximum load current. The temperature coefficient of \( V_{ \text{REF} } \) is compensated by a saturated diode-connected the positive channel Metal Oxide Semiconductor (PMOS) and a proportional to absolute temperature current source and a voltage reference core. The start-up circuit is designed as a precautionary process consumes an average current of 10 nA at room temperature and achieves a minimum temperature coefficient of 8.1 ppm/°C from -40°C to 125°C. The mean line sensitivity is 0.17%/V and the coefficient of variation is 2.1%.

**Circuit Description:** The circuit of the proposed voltage reference is illustrated in Figure 1. This circuit has three parts: a start-up circuit, a proportional to absolute temperature (PTAT) current source and a voltage reference core. The start-up circuit is designed as a precautionary measure to ensure bias in the desired state.

The PTAT current source is a well-known beta multiplier current source configuration formed by M1–M4 and R1. With higher than 100 mV of the drain-to-source voltage \( V_{DS} \), the F-β characteristics of M1–M4 operating in sub-threshold region is given by [1, 2] as

\[
I_D = \mu_C W \frac{1}{L} (m - 1) V_F^2 e^{\frac{(q_n q_\phi)}{k m V_T}}.
\]

where \( \mu \) is the carrier mobility, \( C_{ox} \) is the gate oxide capacitance per unit area, \( W \) and \( L \) are the channel width and length, respectively, \( m \) is the sub-threshold slope parameter, typically having a value of 1.5–2, \( V_{TH} \) is the gate-to-source voltage, \( V_{th} \) is the threshold voltage of a MOSFET and \( V_T \) is the thermal voltage.

From Figure 1, there exist body effects in M3 and M6. The expression of \( V_{th} \) is given by [3] as

\[
V_{th} = V_{gs0} + \gamma \left( \sqrt{2 \phi_F + V_{SB}} - \sqrt{\phi_F} \right) \approx V_{gs0} + \left( m - 1 \right) V_{SB}.
\]

where \( V_{gs0} \) is the threshold voltage with zero body bias, \( \gamma \) is the body effect constant, \( V_{SB} \) is the source-to-bulk voltage of a MOSFET and \( \phi_F \) is the Fermi potential.

With the reduction in the reference current value, the size of \( R_1 \) increases. The value of \( R_1 \) is 21.4 MΩ and \( I_o \approx 0.94 \) nA in this letter, while \( R_1 \) is about 10 MΩ and the reference current is 3.6 nA in [1].

For the voltage reference core composed of M8, M9, MP, M6 and R2, it can be regarded as a common source amplifier with M9 as input connected with a common gate amplifier with M6 as input. M5 is biased by the LC. M6 works in sub-threshold region. Setting the aspect ratio of M7 and M8 is 1:1 and the aspect ratio of M4 and M5 is 1:1, while the proposed voltage reference is in the desired state.

As observed, \( V_{REF} \) in expression (8) has a specific value at a certain temperature with the parameters of the proposed voltage reference designed. Moreover, the value of \( V_{REF} \) is not affected by the load current while the proposed voltage reference is in the desired state. Ignoring the effects of temperature characteristics of \( R_1 \) and \( R_2 \) and taking a derivative with respect to temperature in expression (8), there is the following relation as

\[
\frac{\Delta V_{REF}}{\Delta T} = \frac{1 + \beta}{2} \times \left( \frac{k_2}{k_1} \times \frac{k_2}{k_m} \right) \times T^{\frac{1}{2}} + (k_1 - \eta).
\]
Table 1. Parameters of proposed voltage reference

|     | M1 | M2, M4, M5 | M3 | M6 |
|-----|----|-----------|----|----|
| 1 μm/4 μm | 2 × 1 μm/4 μm | 21 × 1 μm/4 μm |
| M7, M8 | M9 | MP |
| 1 μm/1 μm | 2 μm/0.3 μm | 1 μm/100 μm |
| M10, M11 | M12 | N₁, N₂ |
| 2 μm/0.5 μm | 4 μm/0.5 μm | 2.21 |
| R₁, R₂, V₉₉₉ (300 K) | C₁, C₂, C₃ |
| 2 × 10.7 MΩ, 10.7 MΩ, −596.4 mV | 50 fF/0.6 pF/8 pF |

![Small signal model diagram of the voltage reference core](Image)

FIG. 2 Small signal model diagram of the voltage reference core

From expression (10), if \((k₁ − \eta)\) is negative, zero TC of \(V_{REF}\) could be achieved at a certain temperature. In this letter, as a \(V_{REF}\) of 837.2 mV, \(\eta\) is 902.9 μV/K and \(k₁\) is set as 260 μV/K. In order to have a lower TC from −40°C to 125°C, the value of the expression for temperature in expression (10) should be closed to 642.9 μV/K by properly setting \(k\) and \(k₂\).

However, \(R₁\) and \(R₂\) are non-silicide P+ poly resistors with negative temperature sensitivity and the TC is about −247 ppm/°C. From expression (9), with temperature changes from −40°C to 125°C, the change rate of resistance is about 4% and the change rate of \(k₂\) is about 4%. The change rate of \(k₁\) is about 2%. From expression (10), the term of the temperature characteristic of \(R₁\) and \(R₂\) on the value of \(\Delta V_{REF}/\Delta T\) is about 13 μV/K. Hence, the value of \(k\) and \(k₂\) obtained from the expression (10) only need to be adjusted slightly to have a lower value of \(\Delta V_{REF}/\Delta T\). From expressions (8)−(10), \(N₁, N₂, R₁\), \(R₂\) and \(Wₚ/Eₚ\), listed in Table 1, are the most critical design parameters for the performance of the proposed voltage reference.

Considering the stability of the voltage reference core, the small signal model diagram of feedback loop is depicted in Figure 2. From Figure 2, with \(r_{mp} >> 1/gₚ₆\) \((r_{mp}\) is the small signal equivalent resistance of MP and \(gₚ₆\) is the transconductance of MP), the transfer function of open loop can be written as

\[
\text{LoopGain}(s) = -K_{Loops} \times \frac{(1 + \frac{r_{mp}}{r_{o6}})}{(1 + \frac{1}{r_{o6}})(1 + \frac{1}{r_{o8}})}. \tag{11}
\]

The expression of the low-frequency open loop gain \(K_{Loops}\), dominant pole \(\left(p₁\right)\), non-dominant pole \(\left(p₂\right)\), zero pole \(\left(z₁\right)\) and output pole \(\left(z₂\right)\) are obtained as

\[
K_{Loops} = g_{mp}(r_{o6}/r_{o8})×r_{o6} \left| r_{o6}\right| \tag{12}
\]

\[
z₁ = \frac{g_{mp}}{C_{mp}} × \frac{1}{r_{o6} \left| r_{o6}\right| g_{o6}(r_{o6}/R_L)C_C} \tag{13}
\]

\[
p₂ = \frac{1}{C_{mp} \left| R₂(1/g_{mp})\right|}, \quad p₁ = \frac{1}{C_L(1/\left| g_{mp}\right|)} \tag{14}
\]

where \(g_{mp}, g_{o6}\) are the transconductances of M6 and M9, respectively. \(C_{mp}\) is the equivalent capacitance of point A. The expression of \(p₁\) is \(1/(r_{o6}/r_{o8})\) \((g_{mp} (r_{o6}/RL)C_C + C_A))\). \(C_A\) is far less than \(g_{mp}(r_{o6}/r_{o8})\)\.

Simulation Results: The performance of the proposed voltage reference has been determined in 55 nm CMOS process. The temperature characteristic of resistance is considered in the simulation of temperature coefficient. Figure 3 depicts the temperature characteristic curves of \(V_{REF}\) at different supply voltages. For supply voltages ranging from 0.86 to 3 V, voltage reference achieves an minimum TC of 8.1 ppm/°C from −40°C to 125°C and a 0.17%/V mean line sensitivity, while the load current is 0.

The TC of voltage reference under different load currents is shown in Figure 4. This proposed voltage reference realises a TC less than 20 ppm/°C under the load currents ranging from 1 nA to 10 μA and achieves a TC between 20 ppm/°C and 35 ppm/°C under the load currents ranging from 10 to 40 μA. Figure 5 depicts the stability response simulation of voltage reference under the load currents ranging from 1 nA to 40 μA. The loop can provide a minimum 48 dB gain and a minimum phase margin about 64.2°.

The simulation result of power-up is shown in Figure 6. The supply voltage is set at 1.2 V and the load current is set at 10 nA. The PTAT current source and the voltage reference core reach the desired state at 5.77 ms while the power on time of supply voltage is 2 ms.

The process variation and device mismatch of all devices except the resistors of proposed voltage reference are simulated by Monte Carlo. Figure 7 shows the Monte Carlo simulation results from 1000 samples. The coefficient of variation \(\approx \sigma/\mu\), where \(\mu\) and \(\sigma\) are the mean value
and the standard deviation, respectively) of $V_{\text{REF}}$ is 2.1%. Moreover, the performance of the proposed voltage reference can be calibrated by trimming $R_1$, $R_2$ and $W_P$.

Table 1 shows the parameters in this voltage reference. Table 2 summarises the characteristics of the proposed voltage reference in comparison with prior arts. It can be noted that the proposed reference has the lowest TC, the maximum supply voltage range compared to [1, 4, 5] and consumes less power compared to [1, 5]. Meanwhile, this proposed voltage reference has the maximum load current of 40 $\mu$A, which makes it possible for directly supplying the low-power sensors without an extra power management circuit.

**Conclusion:** This Letter realises a novel ultra-low power voltage reference. The mean reference voltage is 837.2 mV and the capacity of load currents ranging from 0 to 40 $\mu$A. Accurate design ensures that this voltage reference generates a reliable voltage with a low TC about 8.1 ppm/°C, while it just consumes a current of 10 nA. The extremely low power and high precision features of proposed voltage reference with the capacity of load current make it attractive for passive sensor systems.

**Author Contributions:** Maodong Wang: conceptualisation, formal analysis, methodology, writing original draft and review and editing; Wenjie Xu: investigation, validation and visualisation; Na Yan: methodology, software, validation and writing original draft; Hao Min: project administration, writing original draft and review and editing.

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**References**

1. Mu, J. et al.: A 58-ppm/°C 40-nW BGR at supply from 0.5 V for energy harvesting IoT devices. IEEE Trans. Circuits Syst. II Express Briefs 64(7), 752–756 (2017)
2. Liu, Y., et al.: An ultralow power subthreshold CMOS voltage reference without requiring resistors or BJTs. IEEE Trans. Very Large Scale Integr. VLSI Syst. 26(1), 201–205 (2018)
3. Luo, H. et al.: Subthreshold CMOS voltage reference circuit with body bias compensation for process variation. IET Circuits Devices Syst. 6(3), 198–203 (2012)
4. Bialek, H., et al.: A 6-transistor ultra-low power CMOS voltage reference with 0.02%/V line sensitivity. 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, pp. 1–4 (2020)
5. Chi-Wa, U. et al.: A 0.5-V supply, 36 nW bandgap reference with 42 ppm/°C average temperature coefficient within −40°C to 120°C. IEEE Trans. Circuits Syst. I Regul. Pap. 67(11), 3656–3669 (2020)