NAX: Co-Designing Neural Network and Hardware Architecture for Memristive Xbar based Computing Systems

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Abstract—In-Memory Computing (IMC) hardware using Memristive Crossbar Arrays (MCAs) are gaining popularity to accelerate Deep Neural Networks (DNNs) since it alleviates the “memory wall” problem associated with von-Neumann architecture. The hardware efficiency (energy, latency and area) as well as application accuracy (considering device and circuit non-idealities) of DNNs mapped to such hardware are co-dependent on network parameters, such as kernel size, depth etc. and hardware architecture parameters such as crossbar size. However, co-optimization of both network and hardware parameters presents a challenging search space comprising of different kernel sizes mapped to varying crossbar sizes.

To that effect, we propose NAX – an efficient neural architecture search engine that co-designs neural network and IMC based hardware architecture. NAX explores the aforementioned search space to determine kernel and corresponding crossbar sizes for each DNN layer to achieve optimal tradeoffs between hardware efficiency and application accuracy. Our results from NAX show that the networks have heterogeneous crossbar sizes across different network layers, and achieves optimal hardware efficiency and accuracy considering the non-idealities in crossbars. On CIFAR-10 and Tiny ImageNet, our models achieve 0.8%, 0.2% higher accuracy, and 17%, 4% lower EDAP (energy-delay-area product) compared to a baseline ResNet-20 and ResNet-18 models, respectively.

Index Terms—Neural Architecture Search, In-Memory Computing, Memristive Crossbar Array, Deep Neural Network.

I. INTRODUCTION

Deep Neural Networks (DNNs) are widely used in a variety of applications like object detection/recognition, video analytics, natural language processing etc. However, the increase of model size to achieve higher accuracy has led to a growing interest in designing domain-specific accelerators like Google TPU [1], Microsoft BrainWave [2]. Intel Nervana NNP [3] which accelerate the key compute primitive – Matrix Vector Multiplication (MVM) [4] in the DNNs. One key aspect of these accelerators is to amortize the data-movement cost in von-Neumann architectures by bringing computation closer to memory. To that effect, researchers have explored Memristive Crossbar Array (MCA) [5] based In-Memory Computing (IMC) hardware [6][7][8] which performs analog computations inside the memory array itself. Owing to the high on-chip density of MCAs [9] and their ability to perform efficient in-situ MVM operations [10], MCA based IMC hardware can achieve higher energy-efficiency compared to digital hardwares.

MCA based IMC hardware offer tremendous potential to accelerate machine learning (ML) workloads [6] [7]. However, there are significant challenges to overcome [11]. In particular, MVM operations are performed in the analog domain and hence require analog-to-digital converters (ADCs) to communicate digital outputs across several MCAs. ADC’s contribute majorly to the energy, latency and area of IMC hardware [11]. Since ADC precision depends on the crossbar size [6], the hardware efficiency (energy, latency and area) of such hardwares has a strong dependence on the crossbar size. In addition, MCA also suffers from computational errors originating from device and circuit non-idealities such as: parasitic resistance, non-linearity from access transistors and I-V characteristics of NVM device [12]. The degree of error in computation also depends on crossbar size [12]. In large-scale DNNs, these computation errors can accumulate and result in severe degradation in classification accuracy. Consequently, efficient mapping of DNN model to MCA based IMC hardware requires careful consideration of hardware design parameter such as crossbar size.

The hardware efficiency and accuracy of DNN models primarily depends on its kernel and layer dimensions, when deployed on fixed hardware configurations (CPUs, GPUs, mobile devices [13][14][15]. However, in order to efficiently map DNNs to IMC hardware, we need to not only consider these DNN model parameters, but also the underlying hardware design parameter such as crossbar size. Intuitively, larger crossbars amortize peripheral (ADC) cost, which should

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lead to better hardware efficiency. However, for some layer
operations, this may not be the case. For instance, as shown in
Fig. 1 an operation (with O output channels) when mapped to
a crossbar of size NxN (N>O), can lead to under-utilization
of the crossbar. In such a case, a smaller crossbar of size
MxM (N>M=O) which the operation fully utilizes can achieve
better hardware efficiency for that particular operation. On the
other hand, the accuracy of the DNN reduces with increasing
crossbar size. This is because the effect of non-idealities is
higher in larger crossbars [12]. Therefore, in order to maximize
the hardware efficiency and accuracy of the DNN mapped
on analog IMC hardware, there is a need to perform co-
exploration of both DNN model parameters and hardware
design parameters. However, such a co-design presents a
challenging search space (as depicted in Fig. 1) consisting
of both DNN and hardware design parameters.

Neural Architecture Search (NAS) has been widely used to
explore over a large search space in order to design efficient
neural networks for various deep learning tasks [14, 16, 17].
More recently, there has been an increasing interest in utilizing
NAS frameworks to design neural networks catered towards
hardware platforms like mobile devices, GPUs etc. More recently, several works [13, 18, 19, 20, 21] have explored the co-design of DNNs and digital hardware accelerators using NAS-based frameworks. In contrary, the search space for analog IMC hardware is unique and complex as DNN model parameters and the underlying hardware
architecture affect both hardware efficiency and application
accuracy.

With regard to analog IMC hardwares, past literature has
been limited to optimization of DNN model parameters in
isolation [21, 22] without consideration of their co-dependence
with the underlying hardware architecture in determination of
the hardware efficiency and accuracy. Naturally, there remains
a need to perform a scaled co-exploration of DNN model pa-
rameters as well as hardware parameters such as crossbar size
to designing efficient DNNs for analog IMC hardwares. Our
proposal NAX is a NAS-based framework to co-design DNNs
as well as the underlying analog IMC hardware architecture
for optimal hardware efficiency and accuracy.

II. RELATED WORK

Past works have explored hardware-aware NAS [14, 15]
focused towards optimizing DNN model parameters for per-
formance and accuracy on target platforms like mobile devices,
GPUs etc. More recently, several works [13, 18, 19, 20, 21]
have explored the co-design of DNNs and digital hardware
accelerators using NAS-based frameworks. In contrary, the
search space for analog IMC hardware is unique and complex
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III. ANALYSIS OF CROSSBAR SIZE IN IMC HARDWARE

We have alluded to the point briefly that crossbar size is
an important parameter in analog IMC hardware because it
has significant implications on the hardware efficiency and
accuracy of the DNN, and these implications are dependent
on DNN model parameters. We perform extensive analysis

Fig. 2. Illustration of kernels of a DNN mapped to the MVMUs. MVMU is shown with a single crossbar for simplicity.
to study the co-dependence of DNN model parameters and crossbar size.

A. Implication of Crossbar Size on Hardware Efficiency

We study the implications of crossbar size on hardware efficiency of a typical spatial architecture, such as PUMA [6]. PUMA's spatial architecture is organized hierarchically into three-tiers: cores, tiles and nodes. The basic computation unit inside the deepest hierarchy, that is the core, is a Matrix-Vector Multiplication Unit (MVMU). MVMU consists of a certain number of analog crossbars that are used to perform matrix vector multiplication operation. Multiple cores are connected via shared memory to constitute a tile. Finally, multiple tiles are connected via an on-chip network to constitute a node.

A typical mapping of a DNN layer to PUMA’s architecture is shown in Fig. 2. Let’s say an input activation (IA) of dimension $H_i \times W_i \times I$ is convolved with a kernel (W) of dimension $K \times K \times I \times O$ to get an output activation (OA) of dimension $H_o \times W_o \times O$. First, the kernels are flattened and stored as columns of a 2D matrix and the input feature maps (FM) are flattened to get the input vectors to MVMUs. As the crossbar size is limited due to technology constraints, the 2D weight matrix is partitioned to map small chunks (of crossbar size) to MVMUs. This mapping results in some of the MVMUs being underutilized as illustrated in Fig. 2. Under-utilized crossbars still involve accesses to peripherals, despite not processing useful information. Thus under-utilization can lead to higher energy consumption and latency. The percentage of under-utilization in a crossbar depends on crossbar size and output channels. Hence, the hardware efficiency of different operations in a DNN depends on crossbar size they are mapped to as shown in Fig. 3.

We observe, in Fig. 3 (a) that the inference energy for different operations in a DNN have varying trends based on the crossbar size they are mapped to. For instance, the energy for operations where the number of output channels $O$ is low (say 16), decreases as we decrease the crossbar size from $128 \times 128$ to $32 \times 32$. This occurs due to the under-utilization of the larger crossbars resulting in additional accesses to peripherals. As the number of output channels increases (to 32 or 64), the effect of under-utilization decreases and the smaller crossbars start to consume more energy compared to larger crossbars. This is because, when a DNN layer operation fully utilizes the crossbar, a smaller crossbar size leads to requirement of more MVMUs and consequently more peripheral accesses to represent the same operation.

The inference latency (area normalized) for the operations mapped to different crossbar sizes is shown in Fig. 3 (b). To understand the dependence of latency (area normalized) on crossbar size, we need to understand the dependence of area and latency in isolation. For example, like energy, latency has similar trends with crossbar size, i.e., for DNN operations with less output channels, lower crossbar sizes ($16 \times 16$) result in lower latency, whereas, for operations with more output channels, higher crossbar size leads to lower latency. However, area consumed by the compute core follows a different trend. In general, as crossbar size increases, number of required MVMUs reduce, resulting in reduced peripheral area overhead. But as the number of MVMUs per tile can be limited in a spatial architecture such as PUMA, for operations requiring a high number of MVMUs (K:7 I:16 O:16 S:1), the mapping may exceed the boundary of a tile, and require multiple tiles. In such a case, a larger crossbar ($128 \times 128$ here) size may end up requiring more area.
B. Implication of Crossbar Size on Functionality of IMC Hardware

Next, we study the implications of crossbar size on the computational accuracy of IMC hardware. Fig. 4 describes the basic structure of an MCA. There are several sources of non-idealities in an MCA, such as the peripheral resistances ($R_{source}$, $R_{sink}$), parasitic resistances ($R_{wire}$) and non-linear device I-V characteristics. In order to perform an MVM operation in an MCA, the inputs are encoded as voltage ($V_i$) and the weights are encoded as conductance of the device ($G_{ij}$). The currents at the output of $j^{th}$ BL is $I_j = \sum V_i G_{ij}$. However, due to the aforementioned non-idealities, the output current in an MCA is represented as:

$$I = f(V, G(V), R_{source}, R_{sink}, R_{wire})$$ (1)

where the device non-linear I-V characteristics is expressed such that the conductance ($G(V)$) is a function of input voltage ($V$). Hence to estimate the accuracy drop in a DNN due to these non-idealities we use GENIEx [12] that models the non-idealities of real crossbars using a neural network.

To understand the implication of crossbar size on the accuracy drop of a DNN due to the non-idealities in MCA, we map ResNet-20 model to different crossbar sizes based IMC hardware and the accuracy drop is shown in Fig. 5. We make the following conclusions that can be made from this analysis:

- Large crossbars (128x128 here) incurs maximum drop in accuracy, due to longer metal lines resulting in higher $R_{wire}$ which leads to reduced effective resistance of the crossbar.
- As the crossbar size decreases the effect of non-idealities decreases, hence lower drop in accuracy. But when the crossbar size is lowered even more (16x16 here), the accuracy drop increases that occur due to the effect of non-linear non-idealities becoming more prominent compared to linear non-idealities.

Hence, both the hardware efficiency and accuracy for DNNs mapped to the IMC hardware depend on crossbar size as well as layer operations. The unique trends of energy and latency (area normalized) with different operations motivate their co-optimization to get low energy-delay-area product (EDAP). To that effect, we propose NAX, a NAS-based approach to explore the search space presented by the unique co-dependence of DNN model parameters and crossbar size in IMC hardwares. Hereafter, area-normalized latency is referred to as latency.

IV. PROPOSED APPROACH

In this section, we explain the methodology adopted by NAX. First, we introduce the search space for IMC hardwares and show how we consider the non-idealities in crossbar during the architecture search. Then, we show the latency and energy regularized loss function.

A. Building Super-Network for NAS

The proposed hardware-aware NAS framework, NAX, derives motivation from [14]. First, we start by describing an over-parameterized network to represent different types of operations. The over-parameterized network is denoted by $\mathcal{N}(e_1, ..., e_n)$ where $e_i$ represents a certain edge in the directed acyclic graph (DAG). Let $\mathcal{O} = \{\alpha_i\}$ denote the candidate space for the over-parameterized network. The edge $e_i$ in the super-network is set as a mixed operation that has $N$ parallel paths denoted as $m_{\alpha_i}$. Hence, the over-parameterized network can be expressed as $\mathcal{N}(e_1 = m_{\alpha_1}, ..., e_n = m_{\alpha_n})$.

As described in [14], we also adopt path-level pruning which force only one path per layer to be active at runtime. This path-level pruning helps to reduce the memory requirement by an order and helps to search directly on large-scale datasets. If we look at path binarization in terms of equations, corresponding to the N parallel paths in a edge there are N real-valued architecture parameters ($\alpha_i$) which are transformed to binary gates as shown in Eq. (2), where $p_i = \frac{\exp(\alpha_i)}{\sum_{j} \exp(\alpha_j)}$. For a given input $x$ the output of the mixed edge is defined as shown in Eq. (3). For more technical details, please refer to [14].

$$g = \text{binarize}(p_1, ..., p_N) = \begin{cases} [1, 0, ..., 0], & \text{w/ probability } p_1, \\ ... \\ [0, 0, ..., 1], & \text{w/ probability } p_N \end{cases}$$ (2)
Architecture Parameter
CONV
3x3
CONV
3x3
INPUT
OUTPUT
update
CONV
5x5
α𝑖 𝛽𝑖 … 𝛾𝑖 … 𝛿𝑖 … 𝜎𝑖
0 0 … 0 … 1 … ... fmap in memory
Binary Gate 0: prune, 1: keep
CONV
7x7
CONV
7x7
Crossbar (Non-ideal):
... Crossbar (Ideal):
[0x0] 𝛽 [0x0] 𝛽 [0x0] 𝛽 [0x0] 𝛽 [0x0]: 64x64 [0x0] … [0x0] 𝛾 [0x0] 𝜎 [0x0] … [0x0] … [0x0] … [0x0] … [0x0] 0 [0x0] 𝜎 [0x0] 0 [0x0]: 32x32 [0x0]: 64x64 [0x0] … [0x0] 𝜎 [0x0]: 16x16 [0x0] 0 [0x0]: 16x16
fmap in memory
1 … 0 … 0 … 0 … 0
binary gate 0: prune, 1: keep

Fig. 6. An overview of NAX approach (best viewed in color): (a) First considering the crossbars without non-idealities, weights are trained keeping architecture parameters constant. (b) Next the architecture parameters are trained keeping the weight parameters constant and considering crossbars with non-idealities.

\[ m_{Binary}^\{i\}(x) = \sum_{i=1}^{N} g_i o_i(x) = \begin{cases} 
  o_1(x), & \text{w/ probability } p_1, \\
  \ldots \\
  o_N(x), & \text{w/ probability } p_N 
\end{cases} \quad (3) \]

B. Building and Training Over-Parameterized Network for IMC Hardware

The over-parameterized network for an IMC hardware is unique due to the dependence of both accuracy and hardware efficiency on crossbar size as discussed in section III. Hence, the candidate space \( \mathcal{O} \) contains the operations mapped to different crossbar sizes and an extra zero operator that helps to find the depth of the neural network. A particular edge of the over-parameterized network is shown in Fig. 6.

The training procedure of the over-parameterized network involves two steps first training the weight parameters and then the architecture parameters. To train the weight parameters the architecture parameters are frozen and one path from all the edges of \( \mathcal{N} \) is stochastically sampled according to Eq. (2) and then the weight parameters are trained with standard gradient descent on the training set (Figure 6 (a)). Next, to train the architecture parameters the weight parameters are frozen, then the binary gates are reset and the architecture parameters are updated on validation set (Fig. 6 (b)). To consider the effect of non-idealities in crossbar on accuracy, the inference through the selected architecture during the “update architecture parameter” step is done through GENIEx [12]. These two steps are performed alternately for certain number of epochs. Finally, to get the final compact neural network from \( \mathcal{N} \), we select the path in each edge with the maximum architecture parameter value.

C. Hardware Efficiency Regularized Loss Function

Besides accuracy and latency, energy is an important parameter for spatial architectures. As shown in section III-A both latency and energy of different operations mapped to IMC hardware vary with crossbar size and their trend for different operations are unique. Hence, when designing efficient neural network architecture for IMC hardwares, considering both latency and energy as objectives in the loss function is important. We follow the differentiable approach proposed in [4] to optimize both latency and energy. The expected hardware efficiency (energy or latency) of \( i^{th} \) edge \( e_i \) of \( \mathcal{N} \) as a function of path weight \( p_j^i \) is shown in Eq. (4).

\[ E[\text{HWE}_{e_i}] = \sum_j p_j^i \times F(o_j^i) \quad (4) \]

where HWE can be latency or energy and \( F(.) \) denotes the hardware efficiency prediction model, which is a lookup table containing latency and energy for all the operations in the search space.

Therefore, the expected hardware efficiency for \( \mathcal{N} \) can be expressed by adding this expected hardware efficiency for all the layers of over-parameterized network:

\[ E[\text{HWE}] = \sum_i E[\text{HWE}_{e_i}] \quad (5) \]

Now we add the weighted latency and energy regularized terms to our loss function. The constants \( \lambda_1 \) and \( \lambda_2 \) controls the trade-off between accuracy, energy and latency. Hence the hardware efficiency regularized loss function can be expressed as:

\[ \text{Loss} = \text{Loss}_{CE} + \lambda_1 \|w\|^2 + \lambda_2 E[\text{latency}] + \lambda_3 E[\text{energy}] \quad (6) \]

where \( \text{Loss}_{CE} \) is cross-entropy loss and \( \lambda_1 \|w\|^2 \) denotes weight decay.

V. EXPERIMENTS

We perform experiments on CIFAR-10 and Tiny ImageNet datasets to demonstrate the effectiveness of NAX to co-design neural network and hardware architecture. In addition, by an ablation study on CIFAR-10 dataset we show the importance of energy and latency co-optimization for MCA based IMC hardware. The IMC hardware parameters used in the experiments are shown in Table I. All the experiments for NAX are conducted on four NVIDIA RTX 2080Ti GPUs.
Fig. 7. Neural network and crossbar size found on CIFAR-10 with i-search when optimizing (a) None of hardware efficiency parameter (b) Energy (c) Latency (d) Energy and Latency. RNC represents the basic block of ResNet-20 model with two convolution layers in series and a skip connection. Feature map size in bold represents an input to the layer with stride = 2 block.

### TABLE I
IMC Hardware Parameters, N is the number of rows in a crossbar.

| Parameter       | Value       |
|-----------------|-------------|
| Bit stream      | 1 bit       |
| Bit slice       | 2 bit       |
| ADC precision   | log₂(N × 3) |
| $R_{on}$        | 100 KΩ      |
| $R_{off}$       | 600 KΩ      |
| $V_{supply}$    | 0.25 V      |

### A. Experiments on CIFAR-10
For the CIFAR-10 experiments, we start with ResNet-20 as our backbone. To create the over-parameterized network we replace the convolution layers of basic block in ResNet-20 model with the mixed layer which consists of different kernel sizes {3x3, 5x5, 7x7} mapped to varying crossbar sizes ($XB_{size}$) {128x128, 64x64, 32x32, 16x16}.

### TABLE II
Ablation study on CIFAR-10 with mono/bi/multi-objective loss function.

| HWE Parameter Optimized | Energy (J) | Latency ($s \times mm^2$) | i-accuracy (%) |
|-------------------------|------------|---------------------------|----------------|
| None                    | 1.59       | 1.27                      | 93.18          |
| Energy                  | 0.34       | 1.08                      | 93.43          |
| Latency                 | 1.94       | 0.44                      | 93.00          |
| Latency & Energy        | 0.44       | 0.25                      | 93.05          |

Searching and training details: From the training set, we create a validation set by randomly sampling 5000 images. This subset is used to learn the architecture parameters using Adam optimizer with an initial learning rate of 0.006. We consider two search configuration in NAX: i) non-ideal search (ni-search), where the inference while training the architecture parameters is performed considering non-idealities in the crossbars, ii) ideal search (i-search), where we do not consider non-idealities in crossbars. The functional simulator in GENIE framework which gives bit-serial compute units to implement the MVM operation which is further used to create custom conv2d and linear layers operation libraries. Hence, inference during ni-search has high memory and time requirements. To address the high time requirement we provide tiling support for the output activations and multi-GPU support for the whole GENIE framework which gives ~5-6x speedup compared to the original version. The added tiling feature also helps to create a trade-off between batch size for inference (while training architecture parameters) and the tile size. Even with all the above speedups, the time for inference during ni-search is high hence at every iteration we randomly select 2 layers from the over-parameterized network mapped to crossbars with non-idealities; the first convolution layer and last fully-connected layer are always mapped to crossbars with non-idealities.

After the training process of the over-parameterized network is completed we select a compact network according to the architecture parameter values as discussed in section [IV-B]. Then we train this compact network with step learning rate schedule for 300 epochs with learning rate starting from 0.1 and divide by 10 at 100th and 150th epoch. We report the accuracy on test set considering non-idealities in crossbar (ni-
TABLE III
Accuracy and hardware efficiency on CIFAR-10. $X B_{size} =$ mixed implies varying crossbar size across the layers.

| Model (X B_{size}) | i-accuracy (%) | ni-accuracy (%) | Energy (mJ) | Latency ($s \times mm^2$) | EDAP*1e3 | Params (M) |
|---------------------|----------------|-----------------|-------------|---------------------------|-----------|-----------|
| ResNet-20 (128x128) | 92.93 | 50.21 | 2.04 | 0.32 | 0.65 | 0.27 |
| ResNet-20 (64x64) | 92.93 | 91.93 | 0.89 | 0.40 | 0.35 | 0.27 |
| ResNet-20 (32x32) | 92.93 | 91.34 | 0.49 | 2.14 | 1.03 | 0.27 |
| ResNet-20 (16x16) | 92.93 | 88.76 | 0.49 | 2.14 | 1.03 | 0.27 |
| NAX-i (mixed) | 93.05 | 92.13 | 0.44 | 0.25 | 0.11 | 1.25 |
| NAX-ni1 (mixed) | 93.39 | 92.92 | 0.82 | 0.40 | 0.33 | 1.25 |
| NAX-ni2 (mixed) | 93.15 | 92.70 | 0.78 | 0.38 | 0.29 | 1.25 |
| NAX-ni3 (mixed) | 93.45 | 92.22 | 0.51 | 0.38 | 0.19 | 0.94 |

Fig. 8. Neural network (NAX-ni2) and crossbar size (label same as Fig. 7) found on CIFAR-10 with ni-search when optimizing both energy and latency. RNC represents the basic block of ResNet-20 model with two convolution layers in series and a skip connection. Feature map size in bold represents an input to the layer with stride = 2 block.

accuracy) and without considering non-idealities in crossbar (i-accuracy).

**Ablation Study:** To motivate the co-optimization of energy and latency, we find neural network and hardware architecture configuration using i-search in NAX by optimizing: i) none of the hardware efficiency (HWE) parameter (none), ii) one of the hardware efficiency parameter (energy or latency), iii) both energy and latency. The result for the ablation study is tabulated in Table I and the findings are summarized below:

- When none of the hardware efficiency parameter is optimized, energy and latency values are high; the neural network and crossbar size found is shown in Fig. 7 (a).
- When energy/latency is considered in the loss function, only those parameters are optimized; the neural network and crossbar size found is shown in Fig. 7 (b) for the layer with stride = 2 block.
- When energy/latency is considered in the loss function, all the hardware efficiency parameters are optimized. To optimize all the neural network and crossbar size together for some of the layers the NAS algorithm selects zero operation from the search space which is depicted in Fig. 7 (d).

**Non-ideal search results:** We apply the proposed approach in section IV-B to find neural networks and crossbar size for different layers of the neural network. We compare the test accuracy and hardware efficiency results for the neural network architecture (NAX-ni) found by ni-search in NAX with the neural network (NAX-i) found by i-search in NAX and the baseline ResNet-20 model mapped to homogeneous crossbar sizes across all the layers. The results are tabulated in Table III and the neural network and crossbar size found using i-search and ni-search is shown in Fig. 7 (d) and Fig. 8 respectively. Compared to all the ResNet-20 models, both NAX-ni and NAX-i have better i-accuracy and ni-accuracy. The ni-accuracy for NAX-ni1-3 is better compared to NAX-i, which can be attributed to the GENIEx inference during the ni-search that helps to select operations and crossbar size from the candidate set having better ni-accuracy. The EDAP and accuracy for NAX-ni2 is 17% lower and 0.8% higher than the best ni-accuracy ResNet-20 model (ResNet-20 (64x64)). Further, the EDAP and accuracy for NAX-ni3 is 29.63% lower and 0.9% higher respectively than the best EDAP ResNet-20 model (ResNet-20 (32x32)). Also, both NAX-i and NAX-ni use more parameters compared to ResNet-20 model; however, the hardware efficiencies for the model found by NAX is much better compared to the baseline ResNet-20 models, which is due to the high utilization of crossbars in the architectures found by NAX. Moreover, this motivates optimizing hardware efficiency directly instead of proxy metric like number of parameters in the neural network.

The ni-accuracy difference between NAX-ni and NAX-i models is not high, because the crossbar size in the CIFAR-10 search space that have high ni-accuracy (64x64, 32x32) also results in high hardware efficiency. These hardware efficiency and ni-accuracy results demonstrate the importance of exploring the search space proposed in section IV-B to co-design neural network and hardware architecture for MCA based IMC hardware. The search cost for ni-search is ~32 GPU-hours and for i-search it is ~12 GPU-hours.

**B. Experiments on Tiny ImageNet**

For the Tiny ImageNet experiments, we start with ResNet-18 (max-pool layer after first convolution layer removed) as our backbone. Similar to CIFAR-10 experiments we build the super-network by replacing the convolution layers of basic blocks in ResNet-18 with the mixed layer that consists of

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- **TABLE III**

- **Fig. 8.** Neural network (NAX-ni2) and crossbar size (label same as Fig. 7) found on CIFAR-10 with ni-search when optimizing both energy and latency. RNC represents the basic block of ResNet-20 model with two convolution layers in series and a skip connection. Feature map size in bold represents an input to the layer with stride = 2 block.
different kernel sizes \{3x3, 5x5\} mapped to varying crossbar sizes \{128x128, 64x64\}.

**Searching and training details:** We randomly sample 5000 images from the training set as a validation set to train the architecture parameters using Adam optimizer with an initial learning rate of 0.003. Similar to CIFAR-10 experiments we consider two search configurations ni-search and i-search. While training the architecture parameters, the stride=2 blocks, first convolution layer and last fully-connected layer in the over-parameterized network are always mapped to crossbars with non-idealities and additionally we randomly map 4 layers from rest of the layers in the over-parameterized network to crossbars with non-idealities at every “update architecture parameter” iteration. The compact network from the over-parameterized network is selected similar to CIFAR-10 experiments. We train this compact network with step learning rate schedule for 90 epochs with learning rate starting from 0.1 and divide by 10 at 30th and 60th epoch.

**Non-ideal search results:** We apply the NAX approach proposed in section IV-B to find neural network and crossbar size on Tiny ImageNet dataset. The results are listed in Table IV and the neural networks and hardware architecture configuration found using i-search and ni-search are shown in Fig. 9. Compared to the best ni-accuracy ResNet-18 model (ResNet-18 (64x64)) NAX-ni2 has 0.2% better accuracy with 4.4% lower EDAP. Further, NAX-ni1 has 18.57% higher accuracy with 10.47% higher EDAP compared to best EDAP ResNet-18 model (ResNet-18 (128x128)).

Majority of the layers in Fig. 9(a) use 128x128 crossbars (hence high hardware efficiency) because larger crossbars are fully utilized due to the output channels more than 128 for the operations in the Tiny ImageNet search space. Unlike CIFAR-10 the ni-accuracy difference between NAX-ni1,2 and NAX-i models is high because the operations in the Tiny ImageNet search space that have high ni-accuracy results in low hardware efficiency. This shows the importance of inference through GENIEx during the “update architecture parameter” step to find the crossbar size with better ni-accuracy. The search cost for ni-search is \(\sim 350\) GPU-hours and for i-search it is \(\sim 5\) GPU-hours.

VI. CONCLUSION

The efficiency of DNNs are co-dependent on DNN model parameters and the underlying hardware architecture. This is particularly true for memristive crossbar based in-memory computing systems. On one hand, these systems suffer from the effect of device-circuit non-idealities which govern the accuracy of DNNs, and on the other hand, the hardware efficiency is dominated by the peripheral ADC cost. Incidentally, the impact of non-idealities on DNN accuracy as well as the implications of ADC cost on hardware efficiency, is a strong function of the size of crossbars in IMC hardware. In this work, we present NAX, a NAS framework to co-design neural network and the underlying hardware architecture through co-exploration of DNN model parameters and crossbar-size for optimal hardware efficiency and accuracy. First, we analyze the implications of crossbar size on hardware efficiency and accuracy (considering non-idealities in crossbars) for different

### Table IV Accuracies and Hardware Efficiency on Tiny ImageNet

| Model (\(X_{B_{size}}\)) | i-accuracy (%) | ni-accuracy (%) | Energy (mJ) | Latency (s * mm²) | EDAP\(\times 10^3\) (mJ \(\times ms * mm^2\)) |
|---------------------------|----------------|----------------|-------------|-------------------|------------------------------------------|
| ResNet-18 (128x128)       | 55.83          | 78.60          | 2.31        | 0.83              | 1.91                                     |
| ResNet-18 (64x64)         | 55.83          | 78.60          | 2.31        | 1.37              | 2.71                                     |
| NAX-i (mixed)             | 56.57          | 78.48          | 2.31        | 0.85              | 1.71                                     |
| NAX-ni1 (mixed)           | 56.58          | 78.60          | 2.05        | 1.03              | 2.11                                     |
| NAX-ni2 (mixed)           | 56.32          | 78.32          | 2.31        | 1.11              | 2.59                                     |
layers of the neural network comprising of different kernel sizes mapped to varying crossbar sizes. Further, we demonstrate the importance of co-optimization of accuracy, energy and latency to build neural networks with high accuracy and low EDAP for IMC hardware. Finally, we show that NAX can co-design neural network and IMC hardware to achieve 17%, 4% lower EDAP and 0.8%, 0.2% higher accuracy, respectively, on CIFAR-10 and Tiny ImageNet datasets with respect to baseline ResNet-20 and ResNet-18 networks.

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