Supplementary Materials for

A 619-pixel machine vision enhancement chip based on two-dimensional semiconductors

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This PDF file includes:

Sections SI to SVIII
Figs. S1 to S17
Table S1
References
1. **Synthesis of wafer-scale MoS$_2$ film and fabrication of the MoS$_2$ chip**

**A. Synthesis of wafer-Scale MoS$_2$**

A crucible with sulfur powder (Alfa Aesar 99.999%) was placed in Zone 1 with an appropriate amount of MoO$_3$ powder (Alfa Aesar 99.95%) set in Zone 2 (downstream of the flow in the tube). The distance between the two crucibles was 30 cm. A sapphire substrate was carefully cleaned with IPA and methanol and dried by N$_2$, and placed in Zone 2, face-down on the crucible containing the MoO$_3$ powder. During synthesis, the temperature in Zone 1 and Zone 2 was controlled at 180 °C and 650 °C, respectively. A continuous monolayer MoS$_2$ film was synthesized at atmospheric pressure with 300 sccm of Ar as the carrier gas after 10 min sulfuration time.

![Fig. S1. The synthesis of wafer-scale monolayer MoS$_2$ films. (A) Schematic diagram of the CVD growth equipment. (B) Photograph of a 2 in. sapphire wafer uniformly covered with CVD-grown monolayer MoS$_2$.](image)

**B. Fabrication of MoS$_2$ integrated circuits**

The MoS$_2$ FETs and circuits were fabricated on a wafer-scale MoS$_2$ monolayer film on the sapphire substrate, as illustrated above. First, the contact electrodes were patterned with laser direct writing (MicroWriter ML3), followed by the metal deposition using electron beam (E-beam) evaporation. Then a lift-off process was performed to form 35nm Au electrodes. The CF$_4$ plasma etching was performed to define the MoS$_2$ channel geometry. 2 nm SiO$_2$ was deposited as the seeding layer using E-beam evaporation, then a 20-nm-thick HfO$_2$ was subsequently grown by atomic layer deposition (ALD) as a dielectric layer. A cycle including lithography, metal deposition, and lift-off was performed again to form the top gate (35 nm Au), deposited by thermal evaporation. Finally, another lithography and SF$_6$ plasma etching were adopted to form the via holes through the dielectric layer to make MoS$_2$ circuits functional.
2. Level-62 SPICE model

A. Subthreshold Region

In the subthreshold region, the electrons accumulate in the MoS\(_2\) 2D channel under the gate voltage. Because the intrinsic carrier density is rather small, the channel conductivity is almost under an off-state. Thus, the drift of the carrier can be ignored, and the diffusion of the carrier plays the main role in the drain-source current, then the subthreshold current can be determined by the similar method of a bipolar transistor. The drain-source current is exponentially related to the gate bias voltage. The current expression of the model in the subthreshold region is as follows:

\[
I_s = M \cdot \frac{\varepsilon_i}{E_{OX}} \frac{W_{eff}}{L_{eff}} \cdot V_{th}^2 \cdot \exp \left( \frac{V_{gs}}{V_{sth}} \right) \cdot \left( 1 - \exp \left( -\frac{V_{DS}}{V_{th}} \right) \right) \tag{1}
\]

\[
V_{sth} = ETA \cdot \frac{kT}{q} \tag{2}
\]

The mobility of the subthreshold region was characterized by \(M\). \(\varepsilon_i\) is the dielectric constant and \(E_{OX}\) is the thickness of the gate oxide. \(W_{eff}, L_{eff}\) are the width and length of the transistor. \(V_{DS}\) is the drain voltage. \(ETA\) is a model parameter used to adjust the current slope in the subthreshold region of the transfer curve. With the increase of \(ETA\), the slope of the transfer characteristic curve in the subthreshold region decreases, and the swing of the curve in the subthreshold region increases. \(ETA\) has an influence on the output curve and the increase of \(ETA\) will reduce the slope of the output curve in the subthreshold region.

The subthreshold leakage current is the result of the hot electron field emitted by the carrier through the grain boundary trap. The expression of leakage current is as follows:

\[
I_{leak} = I_0 \cdot W_{eff} \left[ \exp \left( \frac{q \cdot BLK \cdot V_{DS}}{k \cdot T} \right) - 1 \right] \cdot [X_{TFE}(F) + X_{TE}] + I_{diode} \tag{3}
\]

\[
F = \frac{V_{DS}}{DD} - \frac{V_{GS} - V_{FB}}{DG} \tag{4}
\]

Where \(I_0\) is defined as leakage scaling constant, \(BLK\) characterizes the contribution of \(V_{DS}\). \(DD\) reflects the influence of drain voltage \(V_{DS}\) on the electric field distribution of drain. With the increase of \(DD\), the influence of the drain electric field on the carriers in the film is weakened. The effect of DG is like that of DD, which reflects that the gate voltage \(V_{GS}\) affects the electric field distribution of the gate. \(X_{TFE}(F)\) and \(X_{TE}\) are the emissivity and thermal emissivity of the carrier under the temperature and electric fields, respectively

\[
X_{TFE}(F) = \int_0^{W_c} \exp \left[ -W - \frac{F_0}{F} (W_c - W) \right] dW \tag{5}
\]

\[
X_{TE} = \exp \left( -\frac{E_c - E_t}{kT} \right) \tag{6}
\]

In this formula, \(E_c\) guides the band bottom energy, \(E_t\) refers to the energy level of the defect state.
\[ F_0 = \left(\frac{kT}{2}\right)^{\frac{3}{2}} \cdot \frac{4}{3} \cdot \frac{2\pi \sqrt{2m_e^*}}{qh} \]  

(7)

Where, \( m_e^* \) is the effective mass of the carrier electron in the channel, and \( h \) is the Planck constant. The reverse bias leakage current \( I_{\text{diode}} \) is:

\[ I_{\text{diode}} = I_{00} \cdot W_{\text{eff}} \cdot \exp\left(\frac{-E_B}{kT}\right) \cdot \left[1 - \exp\left(-\frac{qV_{DS}}{kT}\right)\right] \]  

(8)

From the above formula, the larger \( V_{DS} \) contributes the greater leakage current. \( I_{00} \) is defined as the reverse bias saturation current, with an initial value of 150A/m. The larger \( E_B \) induces the larger the barrier of carrier transport.

B. Linear and Saturated Regions

When \( V_{gs} > V_{teff} \), the channel current changes with the gate voltage and the source-drain voltage. In linear regions, the current can be expressed as

\[ I = \mu_{\text{FET}} \cdot C_{ox} \cdot \frac{W_{\text{eff}}}{L_{\text{eff}}} \cdot \left(V_{GTE} \cdot V_{DS} - \frac{V_{DS}^2}{2ASAT}\right) \]  

(9)

Where the parameter \( ASAT \) is introduced to adjust the relationship between drain saturation voltage \( V_{DSAT} \) and gate voltage \( V_{GTE} \). In saturated regions, the current can be expressed as

\[ I = \frac{\mu_{\text{FET}} \cdot C_{ox} \cdot W_{\text{eff}} \cdot V_{GTE}^2 \cdot ASAT}{2L_{\text{eff}}} \]  

(10)

\[ V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \frac{D A^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1\right)^2}{D A^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1\right)^2}\right] \]  

(11)

Where the parameter \( DA \) is introduced to adjust \( V_{GTE} \). In equation (10), the expression of mobility \( \mu_{\text{FET}} \) is as follows:

\[ \frac{1}{\mu_{\text{FET}}} = \frac{1}{MU0} + \frac{1}{MU1 \cdot \left(\frac{2 \cdot V_{GTE}}{V_{sth}}\right)^{MMU}} \]  

(12)

Where \( MU0 \) and \( MU1 \) are the mobility of MoS2 FETs under high and low electric fields, respectively. When the gate voltage is small, the mobility depends on the mobility \( MU1 \) in the low field, and when the gate voltage is large, the mobility \( MU0 \) in the high field. \( V_{GTE} \) is the effective gate voltage. \( MMU \) is the exponential factor in the dependence of the carrier on the effective gate voltage when a low electric field is applied to the gate. The \( \mu_{\text{FET}} \) in the above formula is defined as the mobility of the transistor. Based on the above equations, the SPICE 62 level model can now be utilized for simulation.
The verification of the output and transfer characteristic curves of MoS$_2$ FETs with an improved Level-62 SPICE model was shown in Figure S2. As shown in Figure S2, the accuracy is within 6%.

Fig. S2. Verification of Level-62 SPICE model. The verification of the MoS$_2$ FETs’ output and transfer characteristic curves with improved Level-62 SPICE model. The accuracy is within 6%.
3. Photoelectric characteristics and reliability measurement for TG MoS$_2$ FETs:

A. Setup for photoelectric measurement:

To obtain reliable photoelectrical signals, a thinner top gate (TG) is deposited (Supplementary Figure S3(A)) to allow the light to efficiently pass through the TG to reach the MoS$_2$ channel. The photoelectrical properties of as-fabricated MoS$_2$ FETs and circuits were measured with a probe station connected to a semiconductor analyzer (Agilent B1500A). The schematic diagram of photoelectric measurement is shown in Figure S3(B).

![Fig. S3. The photoelectric measurement of the TG MoS$_2$ FET. (A) The optical photograph of TG MoS$_2$ FET with a thinner top gate. (B) The schematic diagram of photoelectric measurement.](image)

B. Typical photoelectric characteristics:

![Fig. S4. The photoelectric performance of the TG MoS$_2$ FET. $I_D-V_{TG}$ curves for a TG MoS$_2$ FET in darkness and while illuminated with (A) different wavelengths and (B) different Pin values, at $V_{DS} = 1$ V.](image)

To characterize the photoelectric characteristics of as-fabricated MoS$_2$ FETs, we measured the transfer characteristics while the devices were illuminated with different wavelengths and power densities at $V_{DS} = 1$ V, as shown in Figure S4.
To demonstrate the stability of TG MoS\(_2\) FET, the samples were stored in the glove box for a period of time and measured again. The results in Figure S5 show that the device remained nearly the same.

![Figure S5](image)

**Fig. S5.** The time stability of the TG MoS\(_2\) FET. Transfer characteristics of TG MoS\(_2\) FET at different times after the fabrication of the device at \(V_{DS} = 0.2\) V.

Time-resolved measurement of \(I_D\) for the TG MoS\(_2\) FET is shown in Figure S6, where the characteristics were measured at \(V_{DS} = 0.5\) V and a frequency of 0.2 Hz. The amplitude of the waveform is stable after more than 20000 On-Off cycles.

![Figure S6](image)

**Fig. S6.** The response speed and stability of the TG MoS\(_2\) FET. Time-resolved \(I_D\) of the TG MoS\(_2\) FET with \(V_{DS} = 0.5\) V and frequency of 0.2 Hz.

A photoresponse performance comparison of our TG MoS\(_2\) phototransistors with other similar devices was shown in Table S1.
Table S1  Photoresponse performance comparison of our TG MoS$_2$ phototransistor with other reported results with similar device geometries

| Devices       | $R$ (A W$^{-1}$) | $t_{\text{rise}}$ (s) | $t_{\text{fall}}$ (s) | Ref |
|---------------|------------------|------------------------|------------------------|-----|
| MoS$_2$/WS$_2$| 2.3              | -                      | -                      | 49  |
| MoS$_2$/MoS$_2$| 0.03            | -                      | -                      | 50  |
| MoS$_2$       | $3.6 \times 10^5$| 6.7                    | 70.8                   | 46  |
| MoS$_2$       | 0.0075           | 0.05                   | 0.05                   | 29  |
| MoS$_2$       | $9.26 \times 10^4$| 0.02                   | 0.025                  | 28  |
| MoS$_2$       | $3.3 \times 10^4$| 0.001                  | 0.001                  | This work |
4. The working principle of the MoS$_2$ current mirror circuit

![Diagram of current mirror circuit]

**Fig. S7. Basic current mirror.** This structure is utilized in the MVE chip to improve the noise performance.

Figure S7 schematically shows our MoS$_2$ current mirror structure, where the input and output current can be obtained as:

\[ I_{\text{out}} = \frac{1}{2} \mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_1 (V_{TG1} - V_{TH})^2 \]  

(13)

\[ I_{\text{bias}} = \frac{1}{2} \mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_2 (V_{TG1} - V_{TH})^2 \]  

(14)

So,

\[ I_{\text{out}} = \frac{\left( \frac{W}{L} \right)_1}{\left( \frac{W}{L} \right)_2} I_{\text{bias}} \]  

(15)

The structure consisting of M$_1$ and M$_2$ in Figure S7 is so-called a “current mirror” structure. Combining (13) and (14) to obtain (15), we can see that $I_{\text{out}}$ merely involves the ratio of device dimensions and bias current $I_{\text{bias}}$, thus $I_{\text{out}}$ can be controlled with a reasonable accuracy.
5. The working principle of controlling output current $I_{D3}$

As shown in Figure S8, the transistor M1 and transistor M3 are connected in series. $V_{GS1}$ is the voltage between the gate and source of transistor M1, and $V_{DS1}$ is the voltage between the drain and source of transistor M1. $V_{TH-M1,3}$ are threshold voltages of the transistor M1 and transistor M3.

Firstly, we can obtain

$$V_{DS1} = V_{TG3} - V_{TH-M3}$$ \hspace{1cm} (16)

When $V_{GS1} < V_{TH-G1}$, The transistor M1 is in the cut-off region with a very small current output. When $V_{GS1} > V_{TH-G1}$ and $V_{DS1} < V_{GS1} - V_{TH-G1}$, transistor M1 is in the linear region. The current $I_{D3}$ by transistor M1 is expressed as follows:

$$I_{D3} = \frac{\mu_n \cdot C_{ox} \cdot W}{2L} \cdot [2(V_{GS1} - V_{TH-M1})V_{DS1} - V_{DS1}^2]$$ \hspace{1cm} (17)

where $\mu_n$ is the field-effect mobility, $C_{ox}$ is the gate capacitance per unit area, and $W$ and $L$ are the channel width and length, respectively. When $V_{DS1}$ in (17) is very small, the quadratic term $V_{DS1}^2$ can be ignored, and Eq. (17) can be simplified as follows:

$$I_{D3} = \frac{\mu_n \cdot C_{ox} \cdot W}{L} \cdot (V_{GS1} - V_{TH-M1})V_{DS1} \approx \frac{\mu_n \cdot C_{ox} \cdot W}{L} \cdot (V_{TG1} - V_{TH-M1})(V_{TG3} - V_{TH-M3})$$ \hspace{1cm} (18)

When $V_{GS1} > V_{TH-M1}$ and $V_{DS1} > V_{GS1} - V_{TH-M1}$, transistor M1 operates in the saturation region. The current $I_{D3}$ is now:

$$I_{D3} = \left(\frac{1}{2}\right)\frac{\mu_n C_{ox}}{L}(V_{GS1} - V_{TH-M1})^2 = \left(\frac{1}{2}\right)\frac{\mu_n C_{ox}}{L}(V_{TG1} - V_{TH-M1})^2$$ \hspace{1cm} (19)

Hence, the output current $I_{D3}$ is accurately controlled by voltages $V_{TG3}$ and $V_{TG1}$. 

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Fig. S8. The structure of the current output circuit. The schematic (A) and the simplified schematic diagram (B) of the $I_{D3}$ controlling circuit.
6. The working principle of DAC and its calibration

A digital-to-analog converter (DAC) is one of the key modules used for analog control signal voltage $V_w$. Its function is to convert a digital input to an analog signal, which is a linear conversion. When a digital code is connected to the input, the output is proportional to its analog value. As shown in Figure S9, the performance of a digital-to-analog converter is mainly characterized by its differential nonlinearity (DNL) and integral nonlinearity (INL).

For an N-bit DAC, the digital input range is 0 to $2^{N-1}$. When the digital input changes by “1”, the value of the analog output change is called the minimum quantized analog increment. The value is characterized by the Least Significant Bit (LSB). Assuming its maximum analog value is $X$, its ideal minimum quantized analog increment is:

$$1 \text{ LSB} = \frac{X}{2^N - 1}$$ \hfill (20)

Because of the non-linearity of the DAC, when the input digital quantity changes by "1", its output value may not be equal to 1 LSB. This error can be characterized by DNL. DNL refers to the ratio of the difference between two adjacent analog output values:

$$\text{DNL}_K = \frac{X_K - X_{K-1} - 1 \text{ LSB}}{1 \text{ LSB}}$$ \hfill (21)

where $X_k$ and $X_{K-1}$ are the analog outputs corresponding to input digital quantities $K$ and $K-1$, respectively. Differential nonlinearity shows the uniformity of the analog output from the digital-to-analog converter when the digital input changes. If the adjacent input digital codes changes and its corresponding analog output changes by 1 LSB, then the output of the digital-to-analog converter (DAC) is uniform. However, due to processing fluctuations and transistor uniformity, the DNL is usually larger than 1 LSB. Higher quality MoS$_2$ film, better fabrication recipes and
more matched design methods are required to reduce DNL. The smaller DNL, the better linearity of the DAC.

Due to the unavoidable nonlinearity of digital-to-analog conversion, there is a deviation between the ideal analog output and the actual analog output. This deviation is characterized in terms of INL. For example, when the digital quantity $K$ is input, the actual output is $X_K$, and the ideal output is $X_K' = \frac{X}{2^{N-1}} \times K$. Therefore,

$$INL_K = \frac{X_K - X_K'}{X_K'}$$  \hspace{1cm} (22)

The integral linear error is closely related to the differential linear error as follows:

$$INL_K = \frac{\sum_{i=1}^{K} DNL_i}{K}$$  \hspace{1cm} (23)

The error of DNL and INL mainly affects the weight update accuracy, which directly affects the convergence speed. Although the error caused by the fluctuations in the process cannot be completely overcome with a symmetric layout, the error in INL and DNL can be further overcome by using a calibrated current source. For example, when the actual output current is larger than the theoretical value, the output current can be set closer to the theoretical value by reducing the current from the current source.

![Fig. S10. The results of DAC with the calibration ON/OFF.](image)

**Fig. S10. The results of DAC with the calibration ON/OFF.** The results of DNL (A) and INL (B) with the calibration ON/OFF.

Figure S10 shows DNL and INL as a function of 256 levels. After the calibration, the DAC has enough 8-bit accuracy.
7. The refresh control of the MVE chip

A. The delay unit in an individual pixel

![Circuit Diagram](image)

**Fig. S11.** The circuit diagram of a basic delay unit.

Figure S11 schematically illustrates the circuit of a delay unit used in each pixel to realize timing control. The delay unit is composed of two-stage delay cells with each implemented by two MoS$_2$ transistors in series. M$_3$ is the input transistor of the first stage delay cells, and M$_1$ is the load transistor. Here the source of M$_1$ and the drain of M$_3$ are connected as an output port. Similarly, transistors M$_4$ and M$_2$ are the input and load transistors of the second stage delay cell. After the signal is transmitted by each delay cell, the output signal is reversed, and the output signal phase of the second stage is the same as the input signal. Because of the inverter transmission characteristics, it has a certain amount of delay. By controlling the voltage of VC$_{\text{delay1}}$ and VC$_{\text{delay2}}$, the load can be changed to control the delay time of the delay unit.

B. The working principle of realizing control voltage refresh

![Refresh Process Diagram](image)

**Fig. S12.** Schematic refresh process of control voltage $V_w$. 

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13
To demonstrate how time-division multiplexing is used to update each pixel in turn, Figure S12 schematically shows such a refresh process. First, each pixel has memory, sensing, and processing units. Signal $V_w$ is the bit line input to the memory for each pixel, and $V_w$ is the output of the DAC. The signal output port of the memory is connected with the $V_{TG3}$ for tuning the output current, which is also shown in Figure S13. The word line of the memory controls it to switch between the read and write states. Under the joint influence of illumination, current bias $I_{bias}$ and $V_W$ signal, each pixel realizes an independent current output.

**Fig. S13. Schematic of sensing and processing unit shown in Figure S12.** The $V_{TG3}$ comes from the output of the memory.

The memory’s bit line of each pixel is connected to the same DAC output port on the chip. Through time-division multiplexing, the DAC can control each pixel independently. The memory’s word line of all pixels is connected through delay units. There is a delay unit between every two neighboring memories’ word lines. The input $V_g$ signal will be delayed for a certain period after each delay unit to reach the memory’s word line of each pixel in turn.

As shown in Figure S12, the memory’s bit line of each pixel on the chip is connected with the DAC output port. The externally input memory control signal is a single pulse signal in a global refresh cycle. First, the externally input periodic single pulse signal reaches node $V_{g1}$ through port $V_g$. At this time, the word line $V_{g1}$ of pixel1 obtains a single pulse signal. When the signal $V_{g1}$ is a high-level from word line, the memory of pixel1 is under a write status, and the $V_W$ signal for pixel1 input by DAC is written into the memory of pixel1. At the same time, the word line voltage of the $V_{gi}$ ($2 \leq i \leq n$) for all other pixels remains 0 under the read status, and the output current is maintained at the value of the previous cycle. When the signal of $V_{g1}$ changes from a high level to 0, the memory of pixel1 changes from the write to a read status. Thus, pixel1 receives an updated $V_W$ from $V_{TG3}$ to realize independent control of the output current for pixel1.

Then immediately, the DAC switches the $V_W$ signal value from pixel1 to pixel2, and the single pulse signal of the input $V_g$ is delayed after passing through the on-chip delay unit. Then the memory word line node $V_{g2}$ of pixel2 receives a single pulse signal, similar to the cycle for pixel1. When the high-level signal comes, the memory changes to the write status, The $V_W$ signal for pixel2 input by the DAC is written into the memory of pixel2. In the meantime, the word line voltages of $V_{gi}$ and $V_{gi}$ ($3 \leq i \leq n$) of all other pixels are 0 under the storage state, and the output current remains the value of the previous state.
By repeating the above cycles, the $V_g$ single pulse control signal passes through every delay unit, and the memory storage unit of each pixel is set into the write status in turn, and the DAC sends the $V_w$ signal to the corresponding pixels in turn. When the last pixel is updated, a refresh cycle ends, and $V_g$ sends another high-level single pulse signal again to start a new refresh cycle.
8. The contrast enhancement and noise reduction of our MVE chip

As shown in Figure S14, in the process of visual enhancement, the output current value is obtained first, and then the actual output current value is compared with the ideal output current by the software in PC, such as Matlab. And the control voltage is adjusted to make the output current value close to the ideal value. From the test results, the output current range of different regions can meet the needs of the design by adjusting the control voltage.

![Image Display](image.png)

**Fig. S14. A test implementation of the MVE chip.** This test is completed through the combination of the MVE chip and software.

Moreover, for an electronic imaging system, to deal with the display scene with a large dynamic range, multiple photos are usually obtained by multiple exposures of different lengths of time or multiple lenses are exposed at the same time. The final HDR image is synthesized by using the LDR (low dynamic range) image corresponding to each exposure time, to retain the image details to the maximum extent. HDR processing, the amount of computation is very huge. To overcome this defect, the circuit proposed in this paper adopts the regulation method like retinal ganglion cells. The peripheral control circuit compares the average value of the output current in each region of the visual field and adjusts the weight of the large area of the current mean according to the average value, to ensure the realization of high dynamic range imaging and contrast enhancement.

Due to the material quality, manufacturing defects of the chip and other issues, it is difficult to ensure that the linearity of all pixels is exactly the same. One pixel may be rather different from others surrounding it, so that it is impossible to guarantee the same output current of all pixels under the same light intensity, and random noises occur with a certain percentage, which is so-called the effect of “pepper salt” (i.e. black and white noise spots, especially in flat areas). Its direct impact on the gray value of pixels is to increase or decrease the original gray value. Visually, there are many disharmonious black or white spots in the image, like “salt and pepper”.

Median filtering is a simple nonlinear smoothing technique, which uses the median value of all the values in the solid neighborhood to replace the point value. It is a non-linear processing digital signal technology based on sorting statistics theory, which can effectively suppress noise, and is very effective in eliminating salt and pepper noise. A median filtering algorithm with conditional judgment based on the standard median filter is used in this work. The standard median filter is a
classic type which is a two-dimensional median filter that uses the filtering window to filter the image. In the process of removing image noises using the standard median filter, the size of the filtering window can be set freely. Generally, an odd square window is used, such as $3 \times 3$, $5 \times 5$ square window. In this paper, a $3 \times 3$ filter window is selected. The standard median filter with a smaller filter window has lower hardware requirements and is easy to complete the noise reduction process quickly, to complete the refresh and noise reduction for pixels.

The peripheral control circuit uses a median filtering algorithm to process the data and estimates the real gray value of noise points by denoising algorithm, to adjust the weight of noise points, eliminate noise and complete clear imaging.

![Fig. S15. The 3 \times 3 square filter window of the median filtering algorithm. (A) The 8-neighborhood system. (B) Gray value of each element.](image)

In digital image processing, a neighborhood system can help to establish the relationship between pixels, to deal with digital image problems. Neighborhood refers to the set of adjacent multiple pixels of a certain pixel $P$, as shown in Figure S15(A), which is the 8-neighborhood system used in this paper. Among them, 8 white circles constitute the hollow neighborhood of black circle $P$, which is denoted as $NP^\circ$, 8 white circles and circle $P$ constitute the solid neighborhood of circle $P$, which is denoted as $NP$. Supplementary Figure S15(B) $X_i$ is the gray value corresponding to each solid neighborhood element.

This paper uses the median filtering algorithm which has been optimized specifically. Firstly, a $3 \times 3$ square filter window is selected as the neighborhood of pixels. The standard deviations of the solid neighborhood $NP$ and the hollow domain $NP^\circ$ are calculated respectively.

$$\sigma_{(NP)} = \sqrt{\frac{1}{8} \sum_{i=1}^{8} (x_i - \mu_{(NP)})^2 + (x_p - \mu_{(NP)})^2}$$  \hspace{1cm} (24)
\[ \sigma_{(N_p^\circ)} = \sqrt{\frac{1}{7} \sum_{i=1}^{8} (x_i - \mu_{(N_p^\circ)})^2} \]  

(25)

Where \( \mu_{(N_p)} \) and \( \mu_{(N_p^\circ)} \) are the average values of the solid neighborhood \( N_p \) and the hollow domain \( N_p^\circ \) respectively. Use the following formula to calculate the difference between the two standard deviations.

\[ D = \frac{|\sigma_{(N_p)} - \sigma_{(N_p^\circ)}|}{\sigma_{(N_p^\circ)}} \times 100\% \]  

(26)

When \( D > D_0 \), \( x_p = median_{(N_p^\circ)} \). When \( D \leq D_0 \), \( x_p \) does not change \( median_{(N_p)} \) is the median value of \( N_P \) in the solid neighborhood, and \( D_0 \) is the threshold value of reliable judgment standard after the detection. After processing a “P” point, the same operation is performed on the next “P” point, and the whole flow chart is shown in the supplementary Figure S16.

![Flow chart of the proposed denoising method](image_url)

**Fig. S16. Flow chart of the proposed denoising method.** In the whole process, each pixel is denoised in turn.
The traditional standard median filtering algorithm directly replaces $x_p$ with the median value of solid neighborhood $N_p$, which may replace the original data with information, resulting in a certain degree of distortion. Compared with the traditional algorithm, the median filtering algorithm proposed by this study is adding a judgment process to ensure denoising and avoiding the loss of original information.

Fig. S17. Comparison images before (A) and after (B) denoising the salt and pepper noise by using median filtering algorithm. The standard median filtering algorithm proposed in the paper has a good effect on salt and pepper noise removal.
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