Theoretical and Experimental Substractions of Device Temperature Determination Utilizing I-V Characterization Applied on AlGaN/GaN HEMT

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Abstract: A differential analysis of electrical attributes, including the temperature profile and trapping phenomena is introduced using a device analytical spatial electrical model. The resultant current difference caused by the applied voltage variation is divided into isothermal and thermal sections, corresponding to the instantaneous time- or temperature-dependent change. The average temperature relevance is explained in the theoretical section with respect to the thermal profile and major parameters of the device at the operating point. An ambient temperature variation method has been used to determine device average temperature under quasi-static state and pulse operation, was compared with respect to the threshold voltage shift of a high-electron-mobility transistor (HEMT). The experimental sections presents theoretical subtractions of average channel temperature determination including trapping phenomena adapted for the AlGaN/GaN HEMT. The theoretical results found using the analytical model, allow for the consolidation of specific methodologies for further research to determine the device temperature based on spatially distributed and averaged parameters.

Keywords: AlGaN; FET; GaN; HEMT; thermal current; temperature profile; average temperature

1. Introduction

The commercial wireless market requires more demanding microwave operation with higher requirements in terms of self-heating, high operating voltage and inherent processes and their impact on the device reliability in consumer electronics [1–3]. The presence of two-dimensional electron gas (2DEG) in a gallium nitride (GaN) based structure presents the potential to fabricate high electron mobility transistors (HEMTs) with Schottky diodes employed as excellent devices for application in the microwave and power conversion field. The suppression of the critical temperature increase, caused by high power density along the device active area, requires the utilization of high thermal conductance substrates e.g., silicon carbide (SiC) [4]. Since the devices are microscopic in size, the conventional methods lack the accuracy to estimate the device operating temperature.

Numerous experimental methods were developed to determine the temperature inside and nearby active device area such as Raman spectroscopy or interferometric mapping [5–7]. Additionally, various methods utilizing external heating, or a low-power operating regime were employed, taking advantage of specific electro-thermal device properties. However, these methods, that are widely applied to determine average temperature of HEMT operating in the saturation regime, suffer from a lack of accuracy due to the marginalization of the drain current increase caused by, e.g., gate length modulation or leakage effects [8–10]. Moreover, the current comparison at the defined operating point
to the peak current under short-pulsed operation at various ambient temperatures [11] in these devices does not account for time dependent isothermal phenomena caused processes such as by charge trapping.

Although device thermal simulations, based on non-linear equations, resolve thermal processes inside the structure [12], the combined integral and differential analysis of the resultant current and the separation of the isothermal and thermal sections are emphasized in this work. The complex theoretical considerations, utilizing thermal profile variation, were simplified and adapted for the practical purposes to acquire the average HEMT channel temperature. The theoretical and experimental results obtained are present the potential to improve and consolidate the already utilized methodologies described empirically for specific devices.

2. Theory

2.1. Electrical Model

The presented model is possible to be applied to an n-port device with applied voltage $V_n$ considering resultant current $I$ at one port and neglecting the other port current. Devices meeting these requirements are e.g., Schottky diode, ungated or gated transmission line model (TLM) structure such as field-effect transistor (FET) when neglecting the gate current.

The resultant current change $dI$ ($\Delta I$) consists of an isothermal section $dI_E$ ($\Delta I_E$) induced by applied voltage change $dV_n$ ($\Delta V_n$) and isothermal trapped charge variation $dQ_{TE}(X)$ ($\Delta Q_{TE}(X)$) and thermal section $dI_T$ ($\Delta I_T$) assigned to spatial temperature change $dT(X)$ ($\Delta T(X)$) and the thermal trapped charge variation $dQ_{TT}(X)$ ($\Delta Q_{TT}(X)$):

$$dI = dI_E + dI_T$$  \hspace{1cm} (1)

The current change is defined for the time interval $dt$ ($\Delta t$) considering the device area consisting of spatial elements $dX$ ($\Delta X$) and thermal profile $T(X)$. The resultant trapped charge $dQ_T(X)$ ($\Delta Q_T(X)$) is defined in a similar way, as follows:

$$dQ_T(X) = dQ_{TE}(X) + dQ_{TT}(X)$$  \hspace{1cm} (2)

In general, $dI_E$ is related to $dV_n$ and $dQ_{TE}(X)$ by time invariant coefficients $k_{Vn}$ and $k_Q(X)$, respectively, whereas $dI_T$ is related to $dT(X)$ and $dQ_{TT}(X)$ by time invariant coefficients $k_T(X)$ and $k_Q(X)$, respectively:

$$dI_E = k_{Vn}dV_n + \iiint_X k_Q(X)dQ_{TE}(X)dX$$  \hspace{1cm} (3)

$$dI_T = \iiint_X [k_T(X) + k_Q(X)k_{TT}(X)]dT(X)dX$$  \hspace{1cm} (4)

In (4) $k_{TT}(X) = dQ_{TT}(X)/dT(X)$ is time and state dependent variable. The coefficients $k_Q(X)$, $k_T(X)$, $k_{TT}(X)$ and $k_{Vn}$ at the operating point defined by $V_n$, $I$ and $T(X)$ at time $t$ can be obtained using an analytical solution or advanced simulation software calibrated by experimental results. Although the majority of commercially utilized simulation software allows for self-heating to be switched off/on [12] or DC measurements to be realized in a pulse or quasi-static state [13], it is impossible to turn self-heating on separately to obtain $T(X)$ and $I$ at a predefined operating point and to subsequently turn it off for $\Delta t$ and $\Delta V_n$ to separate $\Delta I_T$ and $\Delta I_E$.

It is recommended that the device current response of a stepping and rectangular pulse source is differentiated into time elements $\Delta t$ to find the particular $\Delta I_E$ and $\Delta I_T$ as shown in Figure 1a,b, respectively. The small parasitic capacitance, typical for GaN-based devices, and a short switching time of the stepping source in comparison with thermal and trapping time constants make it possible for $\Delta I_T$ to be obtained as the difference between $I$ acquired at $t_1 + \Delta t$ and at $t_1 + \Delta t$ in the case of a negligible $\Delta Q_{TE}(X)$. To reach an equilibrium
state during quasi-static stepping, the voltage source measurements shown in Figure 1a, \( \Delta I \) is utilized much higher than the thermal and trapping time constants. For the pulse voltage source measurements initialized at time \( t_0 \) depicted in Figure 1b, the temperature \( T(X) \approx T_0 \) is found along the active device area at \( t \approx t_1 \), that it is zero \( \Delta V_n \) at \( t > t_1 \) and a negligible \( \Delta Q_{TE}(X) \) results in \( \Delta I_T \approx \Delta I \). Otherwise, \( \Delta Q_{TE}(X) \) is required to be incorporated into \( \Delta I_E \) as illustrated below.

![Current time response I for (a) stepping \( V_n \) and (b) \( V_n \) pulse.](image)

**Figure 1.** Current time response \( I \) for (a) stepping \( V_n \) and (b) \( V_n \) pulse.

### 2.2. Average Temperature Definition

To avoid thermal gradient calculations, the average temperature contribution \( dT_A \) in the active device area \( X_A \) is defined by the substitution of \( k^I_T(X) = k_T(X) + k_Q(X)k_{TT}(X) \) and the spatially independent thermal coefficient \( k_T \) related to the operating point:

\[
dI_T = k_T(T_A, V_n, t)dT_A = \iiint_{X_A} k^I_T(X)dT(X)dX
\]

(5)

To eliminate the \( k^I_T(X) \) spatial determination, the approximation, demonstrated by an infinite thermal conductance for which the power density of \( X_A \) does not perform a function, is usually utilized to calculate average temperature \( T_A \) with trapping centers thermally excited by the same \( dT_A \). Therefore the \( k_T = \iiint_{X_A} k^I_T(X)dX \) as \( T_A, V_n \) and \( t \) dependent are used in the following way:

\[
dI_T = k_T(T_A, V_n, t)dT_A = \left[ \iiint_{X_A} k^I_T(X)dX \right]dT_A
\]

(6)

The deviation between (5) and (6) leads to a discrepancy in \( T_A \) determination, especially for different heat flux distributions caused by power dissipation, ambient temperature and time variation. For a spatially independent \( k_T(X), k_Q(X) \) or \( k_{TT}(X) \) in \( X_A \), (5) and (6) appear identical, resulting in \( k_T = k^I_T(X)X_A \) and subsequently \( dT_A \) as the thermodynamic average temperature contribution in \( X_A \):

\[
dT_A = X_A^{-1} \iiint_{X_A} dT(X)dX
\]

(7)
2.3. Ambient Temperature Variation

The average temperature determination method depicted in Figure 2a is based on the resultant current I comparison with an isothermal current IE at time t1 after the measurement initialization at time t0, where the maximum I and IE should be reached at time t0’. The trapping effects must be included in IE as illustrated below. In spite of the zero thermal contribution $$\int_{X} k^E_f(X) dT_E(X) dX$$ to IE, the variation of the isothermal temperature profile $$T_E(X)$$, together with a spatially dependent $$k^E_f(X)$$, results in a thermodynamic average temperature deviation from the initial temperature at t0, caused by the difference between (5) and (6). Therefore, this method is found to be sufficient for devices with a relatively small active area or negligible spatial $$k^E_f(X)$$ variation.

![Figure 2. Current time response comparison for various T_0 for (a) V_n pulse and (b) time interval Δt.](image)

Two identical measurements at distinct ambient temperatures, such that $$T_{01} \approx T_0$$ and $$T_{02} \approx T_0 + \Delta T^*$$ with a small temperature difference $$\Delta T^*$$ result in the current $$I_1$$ and $$I_2$$, temperature profiles $$T_1(X)$$ and $$T_2(X)$$, as depicted in Figure 2b, and exhibit the temperature profile difference $$\Delta T^*(X) = T_2(X, t_1) - T_1(X, t_1) \approx T_2(X, t_1 + \Delta t) - T_1(X, t_1 + \Delta t)$$, $$\Delta T(X) = T_1(X, t_1 + \Delta t) - T_1(X, t_1)$$ and the differential current $$\Delta I = I_1(t_1 + \Delta t) - I_1(t_1)$$, $$\Delta I^* = I_2(t_1) - I_1(t_1) \approx I_2(t_1 + \Delta t) - I_1(t_1 + \Delta t)$$. The assumption of a low $$\Delta t$$ means that the following formula is applicable for quasi-static and pulsed operations:

$$\Delta I^* = \int_{X} k^E_f(X) \Delta T^*(X) dX$$  \hspace{1cm} (8)

The substitution of $$\Delta T^*(X) = \Delta T(X) - \Delta T_E(X)$$ and $$\Delta T_E(X) = T_1(X, t_1 + \Delta t) - T_2(X, t_1)$$ in (8), utilized for the $$dI_T$$ comparison with $$\Delta I_T = \int_{X} k^E_f(X) \Delta T(X) dX$$ based on the comparison of difference and differential substitution $$dI_T / \Delta I_T = dT(X) / \Delta T(X)$$, results in:

$$\frac{dI_T}{\Delta I^*} = \frac{\int_{X} k^E_f(X) dT(X) dX}{\int_{X} k^E_f(X) \Delta T^*(X) dX}$$  \hspace{1cm} (9)

As a result, a $$T_A$$ definition utilizing (6) and substitution $$X \approx X_A$$, $$dI_T$$ and $$\Delta I^*$$ caused by $$\Delta V_n$$ and $$\Delta T_0$$ leading to $$dT_A$$ and $$\Delta T_A^*$$, respectively, leads (9) to the following relationship:

$$\frac{dI_T}{\Delta I^*} = \frac{dT_A}{\Delta T_A^*}$$  \hspace{1cm} (10)

However, despite the zero $$I_E$$ thermal current, a non-zero $$\Delta T_E(X)$$ variation results in a discrepancy between the definition of $$dT_A$$ and $$\Delta T_A^*$$ by (7) and the definition utilizing infinite thermal conductance of the device active area, on the other side. Nevertheless, the $$T_A$$ determination methods utilizing (10) are found to be sufficient for devices with a negligible spatial $$k^E_f(X)$$ variation or a relatively small active area.
Already known $\Delta T_A^*$ and $\Delta I_E$ time dependence allows to obtain $T_A$ as the sum of $dT_A$ calculated in (10) in the quasi-static or pulsed operating regime. Temperature dependent thermal resistance and thermal capacity result in a $\Delta T_A^*$ deviation from $\Delta T_0$. Quasi-static state methods, utilizing the $T_0$ variation, allows for the calculation of $dT_A$ and $\Delta T_A^*$ [9,14].

2.4. Trapping Effects Approximation in FET

We further consider the $T_A$ determination of the FET-neglecting parasitic gate, and its entire electric capacitance. Even a relative carrier velocity $v$ change, and pinchoff area formation are thought to have no impact on channel potential distribution along the channel [15,16].

The threshold voltage $V_{TH}$ shift is related to the time and temperature variation of energy barrier height, free charge concentration along the conductive channel as well as charge trapping, resulting in the additional virtual gate electrode. The gate voltage $V_{GS}$, drain voltage $V_{DS}$ and ambient temperature $T_0$ variation causes $dT_A$, with a direct impact on the $v$ and $V_{TH}$ change. These variations result from the isothermal section $dV_{THN}$, caused by an immediate band energy diagram and free charge concentration change. The isothermal section $dV_{TH}$, is a result of the trapping phenomena during the defined time and the thermal section $dV_{THT}$ originates from thermal carrier and trap center density change.

A widely utilized FET approximation [15] in the case of stepping $V_{DS}$ and/or $V_{GS}$ at a defined $T_0$ is as follows:

$$dl = g_{M0}(dV_{GS} - dV_{THE} - dV_{THT}) + g_{D0}dV_{DS} + dI_{TV}$$  \(\text{(11)}\)

It is possible to acquire the isothermal transconductance $g_{M0}$ and output conductance $g_{D0}$ via immediate isothermal $V_{DS}$ and $V_{GS}$ responses, including $dV_{THN}/dV_{DS}$ and $dV_{THN}/dV_{GS}$. The term $dI_{TV}$ represents the thermal change caused by $dV_{DS}$, $dV_{GS}$ and $dT_0$ and has a major impact on $v$, excluding $V_{TH}$. A substitution of $dl_0 = g_{M0}dV_{GS} + g_{D0}dV_{DS}$ and $dl = dl_E + dl_T$, as applied in (11), results in:

$$dl_E = dl_0 - g_{M0}dV_{THE}$$  \(\text{(12)}\)

$$dl_T = dl - dl_E = dl_{TV} - g_{M0}dV_{THT}$$  \(\text{(13)}\)

A common way to obtain $V_{TH}$ is pulsed and/or quasi-static transfer I-V characteristics utilization at defined $T_0$ and $V_{DS}$ assuming $V_{TH}$ independent on $V_{GS}$ as well as an approximation of isothermal and measured I-V characteristics pointing on the same $V_{TH}$ shift at $T_0$ in the operating range. Trapping phenomena and voltage drop in the source-to-gate and drain-to-source area have a partial influence on the $V_{TH}$ determination especially for low applied $V_{DS}$ or non-linear $V_{TH}$ vs. $V_{DS}$ dependence. The following ways of trapping effects incorporation in $T_A$ calculation coming out of $V_{TH}$ determination from transfer I-V characteristics are explained.

In the case of the quasi-static state operation $V_{TH}$ shift, resulting in $(dV_{THE} + dV_{THN})/dV_{DS}$ caused by $T_0$ and $V_{DS}$ variation, can be simply obtained from quasi-static I-V characteristics. Transfer I-V characteristics, measured by short-pulsed $V_{GS}$ and $V_{DS}$ offering trap influence separation, allow to get $dV_{THN}/dV_{DS}$ obtained from negative $V_{TH}$ shift caused by roll-off effect in short-channel FET [15,17]. Subsequently, the ratio $dV_{THE}/dV_{DS}$ dependent on $V_{DS}$ and $T_0$ acquired and utilized in (12), whereby $dl_0$ is acquired at the beginning of $V_{DS}$ and/or $V_{GS}$ step, a measured transconductance $g_M \gg |g_M - g_{M0}|$ is supposed. For a significant $g_{M0}dV_{THE}/dV_{DS}$ temperature variation in comparison with $dl_{TV}/dV_{DS}$ an iteration process is required for $T_A$ determination.

For $V_{DS}$ and/or $V_{GS}$ pulse responses, depicted in Figure 1b, the pulsed transfer I-V characteristics are measured utilizing $V_{GS}$ and/or $V_{DS}$ quiescent biasing and/or voltage pulses. At $T_0$ and the defined time $t_1$ after the increase of constant amplitude $V_{DS}$ and the sweeping amplitude $V_{GS}$, drain currents are acquired to extract the $V_{TH}$ as $t_1$ and $T_0$ functions. At the time interval $\Delta t$, during the pulse, $\Delta V_{THE} = V_{TH}(T_A, t_1 + \Delta t) -$
$V_{TH}(T_A, t_1)$ gives the opportunity to utilize $\Delta I_E = -g_{M0}\Delta V_{TH}$ for both a small $\Delta t$ and $\Delta V_{TH}$ corresponding to the virtual gate electrode potential shift, neglecting the $g_{M0}$ time variation. The maximum resultant current $I_E$ and $V_{TH}$ obtained immediately after $V_{GS}$ and/or $V_{DS}$ rising edges at $t_0$, provides the opportunity to plot the $I_E$ time dependence at $T_0$, depicted in Figure 2a:

$$I_E(t_1) = I_E(t_0) - g_{M0}[V_{TH}(t_1) - V_{TH}(t_0)]$$

In the considerations above a thermal gradient along the active device area that effects the trap spatial localization is truncated. Isothermal trapping phenomena and a voltage drop in the source-to-gate and the drain-to-source area having a partial influence on $V_{TH}$ shift are neglected as well. Despite this, an appropriate analytical approximation of the I-V characteristics provides an opportunity to predict the trapping phenomena in particular devices. An advantage of the $T_0$ variation method during the device operation is that the calibration of for $dI_{TV}/dT_A$ vs. $T_A$, $V_{DS}$ and $V_{GS}$ with an additional trapping phenomena analysis is not required.

2.5. Short Time Response Current Utilization

Many of the experimental methods that are widely utilized for the $T_A$ acquisition of FET in a saturation regime are based on a zero isothermal drain current change $dI_E/dV_{DS}$ at constant $V_{GS}$. The requirement of zero $dI_E$ in (12) is satisfied for a gate length modulation or a leakage current increase compensated by the trapping phenomena in the saturation regime, resulting in $dI_E \ll dI_T$. Long-channel FET excluding $V_{DS}$ such as $V_{GS}$ dependent charge trapping variation meets this condition therefore the methods to acquire $T_A$ in quasi-static operation coming out from temperature calibration of major electrical parameters [8,16] or ambient temperature variation [9,18] require standard DC measuring equipment. The $dI_E$ prediction at various ambient temperatures, using an analytical model or simulation software also makes such methods applicable for short-channel FET [17,18].

In general, the resultant current acquisition after a short period after the voltage step/pulse is required, to obtain the $dI_0$. The method depicted in Figure 2a is simply applicable for devices exhibiting relatively short time responses $t_0'$-$t_0$, operating in the quasi-static and dynamic state as well providing the opportunity to obtain an isothermal trapping effects approximation. However a switching time of $\sim 10^{-8}$ s is required for full load turning-on, which makes the experimental setup more expensive.

3. Experimental

3.1. Structure Design and Experimental Setup

The investigated Al$_{0.25}$Ga$_{0.75}$N/GaN HEMT structure, including 14 nm Al$_{0.25}$Ga$_{0.75}$N/1.5 nm AlN/1700 nm GaN/75 nm thermal boundary resistance layer (TBR) heterostructure was grown by MOVPE on a 70 µm thick 4H-SiC substrate, containing the backside Au contact, which was soldered to 1 mm thick CuMo leadframe using a 60 µm thick AuSn solder. The top ohmic drain/source and gate contacts were created via standard Au-based metallization. A gated transmission line model (GTLM) HEMT with a width of $w \approx 100$ µm, a gate with a length of $g_C \approx 0.15$ µm, asource to gate gap of length $d_{GS} \approx 0.75$ µm and the drain to gate gap of length $d_{CG} \approx 1.5$ µm was investigated [14]. The device is placed in an open package located on the Al thermal chuck and maintained at a constant temperature.

A semiconductor parameter analyzer Agilent 4155C and controlled thermal chuck were utilized to acquire the output characteristics at zero gate-source voltage $V_{GS}$ and the drain-source voltage $V_{DS}$ varied from 0 V up to 20 V. The chuck temperature was set in the range of 25–185 °C to demonstrate methods based on ambient temperature and threshold voltage variation. The device trapping level was reset via white LED illumination for one minute between quasi-static measurements. The 3D model incorporating device geometry, layout and thicknesses of individual layers was created using the 3D thermal FEM simulations performed by Synopsys TCAD Sentaurus [12]. The material thermal conductivity and capacity values were obtained from the previous work and calibrated.
utilizing the measurements provided [19,20]. The constant ambient temperature boundary condition was set to the structure backside, assuming an ideal heat transfer between leadframe and heatsink. The structure’s self-heating is simulated by three thermal contacts placed along 2DEG, between the drain and source, representing heat contribution from the drain to the source access region, under the gate electrode and the pinch-off region located at the drain side gate edge [19].

3.2. Average Channel Temperature Determination

The drain-source current $I_{DS}$ dependence on drain-source voltage $V_{DS}$ for gate-source voltage $V_{GS} = 0$ V at varying ambient temperature $T_0$ in the range of 25–105 °C was acquired during the $V_{DS}$ step, for a period of period ~1 s using the quasi-static operation as depicted in Figure 3. The maximum $I_{DS}$ obtained at the beginning of the extended $V_{DS}$ step $\Delta V_{DS} \approx 2$ V, and subtracted by $I_{DS}$ value, that were acquired under quasi-static operation from the previous $V_{DS}$ step, results in $\Delta I_{DS}$. Quasi-static and pulsed transfer I-V characteristics show soft $g_M$ and a $g_{M0}$ decrease with rising $V_{DS}$ and $T_0$ as illustrated in Figure 4. In particular, the $V_{TH}$ and $V_{THN}$ were obtained from square rooted transfer I-V characteristics resulting in constant $dV_{THE}/dV_{DS}$ for a defined $T_A$. Therefore $dV_{THE}/dV_{DS} \approx (dV_{TH} - dV_{THN})/dV_{DS}$ is approximately $dV_{THE}/dV_{DS} \approx k_{THE}(T_A - T_0) + k_{TH00}$, $T_0 \approx 25$ °C, $k_{THE} \approx 8.8 \times 10^{-6}$ K$^{-1}$ and $k_{TH00} \approx 1.97 \times 10^{-3}$ for $T_A$ (°C) in the saturation area. However, $T_A$ above $T_0 \approx 105$ °C was reached, which results in $g_MdV_{THE}/dV_{DS}$ being linearly approximated, exhibiting variations of $~8 \times 10^{-8}$ V/K in the range of 25–225 °C, corresponding to $~10\%$ of $dI_{DS}/dV_{DS}$. Interpolated thermal and isothermal parts of $dI_{DS}/dV_{DS}$ vs. $V_{DS}$ at $T_0 \approx 25$ °C are depicted in Figure 5. Moreover, the dissipated power contribution $dP^* = V_{DS}\Delta I^*$, caused by $dT_0$ for low $V_{DS}$ negligible in comparison with $dP = V_{DS}dI_{DS} + I_{DS}dV_{DS}$ caused by $dV_{DS}$, results in the simplified formula for differential thermal resistance $R_{A0}(T_0)$ calculation [14] utilizing (12):

$$R_{A0} = (dT_0^*/dP)(dI - dI_0 + g_MdV_{THE})/\Delta I^*$$ (15)

![Figure 3. Output I-V characteristics for $V_{GS}= 0$ V at various $T_0$.](image-url)
Figure 3. Output I-V characteristics for $V_{GS} = 0$ V at various $T_0$.

Figure 4. Transconductance $g_M, g_{M0}$ and threshold voltage $V_{TH}$ and $V_{THN}$ dependence on $V_{DS}$ at various $T_0$ required for trapping phenomena incorporation.

Figure 5. Interpolated thermal and isothermal difference current sections dependence on $V_{DS}$ at $T_0 \approx 25$ °C.

The linear approximation $T_A - T_0 \approx R_{A0} P$, utilized in the first $g_M dV_{THE}$ iteration step in (15), leads to a formula resulting in $R_{A0}(T_0)$ plot at different $T_0$ and $V_{DS}$ as shown in Figure 6:

$$R_{A0} = \frac{dI_{DS} - dI_0 + g_M[k_{THE}(T_0 - T_{00}) + k_{TH0}]dV_{DS}}{(\Delta P/dT_0) - (g_M k_{THE} V_{DS} I_{DS} dV_{DS})}$$  \hspace{1cm} (16)

Increasing $V_{DS}$ results in different $R_{A0}$ values at a defined $T_0$, which is partially caused by spatially distributed electrical parameters of the active device area such as the $g_M dV_{THE}/dV_{DS}$ variation. The approximation $R_{A0} \approx k_{RA}(T_0 - T_{00}) + R_{00}$, $T_{00} \approx 25$ °C, $k_{RA} \approx 0.2$ W$^{-1}$, $R_{00} \approx 57.0$ K/W at the defined $T_0$ was utilized to calculate $T_A$ in a recurrent way [14] as illustrated in Figure 7. In [8] the major contribution of the thermal $I_{DS}$ section is assigned to the serial source area resistance increase, caused by self-heating in a saturation regime for AlGaN/GaN HEMT. The simulated average channel temperature of the source to the gate area is in acceptable agreement in comparison to the calculated $T_A$. 
on an ambient temperature variation for a device under a quasi-static state and a device
avoid spatially distributed device parameters acquisition. The particular methods, based
pendence. This approximation is found to be sufficient, although further

Figure 6. Temperature dependence of normalized thermal resistance $R_{A0}$.

Figure 7. Average channel temperature $T_A$ vs. dissipated power $P$ in quasi-static state and $T_A$ time
dependence for applied $V_{DS}$ pulse.

For the $T_A$ investigation of HEMT in the pulse operation, $V_{GS}$ and $V_{DS}$ bias was
set to zero, superimposed by a $V_{DS} = 20$ V pulse of length $\sim 1$ s. In the case of non-zero
biasing, the initial condition of zero power dissipation is required to be satisfied. The
period of $\sim 5$ s between voltage pulses was found sufficient because of the absence of the
automated white LED illumination during the pulse breaks. The resultant current $I_{DS}$
acquired at $T_0$ and delay $t_1$ after the rising edge of constant amplitude $V_{DS} = 20$ V and
$V_{GS}$ amplitude sweeping from $-4$ V to $-2$ V at defined points, allowed us to plot the
transfer I-V characteristics and to subsequently obtain the $V_{TH}$ dependent on $t_1$ in the
logarithmic scale in the range of $10^{-7}$–$1$ s, where the $T_0$ step is set linearly in the range
of 25–185 °C. Experimentally acquired $I_{DS}$ in the range of 20–100 ns and 25–185 °C for
pulsed $V_{DS} = 20$ V and zero $V_{GS}$ are depicted in Figure 8. Setting the $V_{GS} = -0.5$ V allows
us to obtain the supposed $S_{M0}$ constant at the defined $T_0$ due to a small deviation under
isothermal conditions.
channel temperature determination. The calculations were a result of the isothermal and mental section, the theoretical subtractions were adapted for the AlGaN/GaN HEMT result of the FET threshold voltage shift that neglects electric capacitance. In the experimental under pulse operation, were compared by taking the trapping process into account as a cause by trapped and free carrier concentration, the band diagram variation in operating thermal current sections separation, by taking into account the threshold voltage shift.

4. Conclusions

The intersection of the measured $I_{DS}$ time dependence and $I_E$ at defined $T_0$ allows $T_A$ determination as depicted in Figures 7 and 8. The difference between the $T_A$ obtained by the quasi-static and the pulsed measurements at $t_1 \sim 1$ s can be explained by the partially compensated $I_{DS}$ during the rising time for the voltage pulse $\Delta V_{DS} \approx 20$ V and the uncompensated $I_{DS}$ during the rising time at the voltage step $\Delta V_{DS} \approx 2$ V, which were utilized in the quasi-static measurements. The difference of $\sim 20$ °C (13%) between simulated and experimental $T_A$ values is assigned to the different heat-flux distributions, resulting in the deviation between (5) and (6), as well as in the electric parameters from the source to the gate area, influencing $dI_T$ and $I_E$ approximation.

4. Conclusions

The average temperature significance was underlined in the theoretical section to avoid spatially distributed device parameters acquisition. The particular methods, based on an ambient temperature variation for a device under a quasi-static state and a device under pulse operation, were compared by taking the trapping process into account as a result of the FET threshold voltage shift that neglects electric capacitance. In the experimental section, the theoretical subtractions were adapted for the AlGaN/GaN HEMT channel temperature determination. The calculations were a result of the isothermal and thermal current sections separation, by taking into account the threshold voltage shift caused by trapped and free carrier concentration, the band diagram variation in operating temperatures and the applied voltage. The calculated and simulated average channel temperature $\sim 160$ °C of the source to the gate area for power dissipation $\sim 2$ W exhibits a difference of $\sim 20$ °C (13%). The considerations applied in the analytical model offer methodological consolidation for use in further research.

![Figure 8](https://example.com/image.png)

Figure 8. Measured $I_{DS}$ time dependence (full-dot) at $T_0 \approx 25$ °C and approximated isothermal $I_E$ time dependence (empty-dot) at various $T_0$ for applied $V_{DS}$ pulse.
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