SC Current Interruption Capability and Protection of SiC Based Solid State Circuit Breaker

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Abstract- This paper presents the short circuit (SC) current interruption capability of a 1.7 kV/72 A silicon carbide (SiC) MOSFET based solid state circuit breaker (SSCB). The interruption process of SSCB is introduced in detail. A test platform is built and the SSCB is tested and discussed at various DC-link voltage, fault inductance and junction temperature. Before the desaturation point ($V_{DS} = 200$ V), SSCB can successfully turn off the SC current. The saturation value of the SC current is positively correlated with $di/dt$, and the effect of junction temperature (50-150 °C) on saturation current is not significant. A SC protection circuit with a response time of 260 ns is proposed and is validated through the test platform.

1. INTRODUCTION
With the development of DC power distribution system, solid state circuit breaker becomes the critical equipment for DC power distribution systems to clear fault current quickly and reliably[1-2]. Power semiconductor devices in the SSCB such as gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), SiC junction filed-effect transistor (JFET), SiC MOSFET play the role of switch[3-6]. Compared with traditional Si devices, SiC MOSFET has higher breakdown voltage, thermal conductivity and lower on-state resistance[7], which is suitable for SSCB application. Understanding characteristics of the SiC MOSFET, including static and switching characteristics as well as SC performance, is essential for successful applying in SSCB condition. For DC power distribution systems, when a SC fault occurs, the SC current has no natural zero-crossing point and the SC current rises quickly, which brings severe challenges to the SC withstand capability of SiC MOSFET[8]. Unfortunately, its SC withstand time is shorter than IGBT, however, the DC system usually has a fault inductance which its value depends on the fault location in the DC power distribution system. Hence, the rising speed of the SC current will be limited by the fault inductance, which reduce the SC pressure on SiC MOSFET. The characterization and SC performance of SiC MOSFET have been presented with double pulse test (DPT)[9-10]. But the DPT condition is different from the SSCB condition due to the tiny loop inductance which causes the difference in SC characteristics. The SC characteristics of a 1.2 kV/115 A SiC MOSFET (C3M0016120D, Wolfspeed) is presented in SSCB condition with different fault inductance and gate resistance, but the influence of ambient temperature and DC-link voltages on SC characteristics has not been study[11]. There have literature studied a Gen3 10 kV/20 A SiC MOSFET (CREE) under different DC-link voltages and ambient temperatures in both HSF and FUL, but has not studied the SC failure[12].

This paper presents SC current interruption capability of a 1.7 kV/72 A SiC MOSFET (C2M0045170P, CREE) based SSCB with various DC-link voltage, fault inductances and junction...
temperature. Based on the SC characteristics, this paper proposed a SC protection scheme using desaturation mechanism and verified its effectiveness through experiments.

2. INTERRUPTION PROCESS OF SSCB
The SiC MOSFET based SSCB is shown in Fig. 1(a). It consists circuit fault inductor $L_{\text{fault}}$, RC snubber, power semiconductor device SiC MOSFET and Metal Oxide Varistor (MOV). RC snubber provides a continuation loop to suppress overvoltage when the SiC MOSFET is turned off and benefits the transient voltage balancing when used in series. MOVs absorb SC energy and clamp the overvoltage to make it lower than the rated voltage of the SiC MOSFET. Fig. 1(b) shows the waveforms of the interruption process of SSCB, it can be divided into four stages as follows.

2.1. Stage I: SC Current Rise Stage
From $t_1$ to $t_2$, SC current rises limited by $L_{\text{fault}}$. Meanwhile, buffer capacitor $C$ discharges through the SiC MOSFET loop as shown in Fig. 2(a). Since the stray capacitance of MOV is very small, its discharge current to SiC MOSFET can be ignored. An RC loop with parasitic inductance is shown in Fig. 3. The maximum pulse current of RC snubber is limited by $R$. In order to avoid excessive pulse current, the circuit should work under over-damped conditions. The circuit can be expressed as:

$$\frac{d^2 u_C}{dt^2} + \frac{R}{L_{\text{stray}}} \frac{du_C}{dt} + \frac{1}{L_{\text{stray}} C} u_C = 0$$

(1)

When $R$, $C$ and $L_{\text{stray}}$ satisfy the conditions of the following formula, the circuit works under over-damping.

$$\frac{R}{2L_{\text{stray}}} > \frac{1}{\sqrt{L_{\text{stray}} C}}$$

(2)
2.2. Stage II: DUT Turn-off Stage
At $t_2$, the SiC MOSFET is turned off, and the fault current is transferred to RC snubber as shown in Fig. 2(b), thereby reducing the turn-off loss of the SiC MOSFET. Capacitor $C$ suppresses the rising speed of the voltage. The SiC MOSFET is completely turned off at $t_3$. The voltage on DUT $V_{off}$ can be approximately expressed as:

$$V_{off} = \frac{I_m}{2C}(t_3 - t_2) + I_m R$$

(3)

2.3. Stage III: Current Commutation Stage
At $t_3$, the current on the SiC MOSFET is all transferred to the RC snubber. The current on $L_{fault}$ is approximately constant, it can be replaced by a current source as shown in Fig. 2(c). When the voltage across RC snubber meets the following conditions, the MOV starts to conduct.

$$V_{off} + \frac{I_m}{C}(t - t_3) \geq V_{1mA}$$

(4)

where $V_{1mA}$ is the opening voltage of MOV. At $t_4$, the current begins to transfer to MOV and the voltage across the SSCB rises sharply to meet the turn-on voltage of MOV. The volt-ampere characteristic of MOV quickly goes from leakage region to normal varistor operation region, its resistance decreases rapidly, which can be represented by a variable resistance $R_x$.

2.4. Stage VI: Energy Absorption Stage
At $t_5$, all SC current flows through the MOV. The MOV can be equivalent to the series connection of the parasitic inductance $L_{MOV}$, a resistor $R_{on}$ and a voltage source as shown in Fig. 2(d). In order to facilitate the calculation, the value of the voltage source is approximated as $V_{clamp}$. $V_{clamp}$ is higher than $V_{DC}$, forcing the SC current to drop. The SC current flowing on the MOV can be expressed as:

$$i_{MOV} = I_{abrupt} = \frac{V_{clamp} - V_{DC}}{L_{fault}}(t - t_3)$$

(6)

The energy absorbed on the MOV is:

$$W = \int_{t_4}^{t_5} V_{MOV}i_{MOV}dt = \frac{V_{clamp}L_{fault}I_{abrupt}^2}{2(V_{clamp} - V_{DC})}$$

(7)

3. SC CHARACTERIZATION TEST OF SSCB
Fig. 4 shows the schematic diagram and physical diagram of the SSCB short-circuit current breaking capacity test circuit. $C_{DC}$ is a DC-link capacitor charged by the high voltage DC power supply to maintain
the DC voltage constant during the SC. The device under test (DUT) is a 1700 kV/72 A SiC MOSFET (C2M0045170P, CERR). The MOVs are selected V420LA40BP, Littelfuse. FPGA control board and gate driver form the SiC MOSFET drive system. The current probe and the voltage differential probe respectively measure SC current \( I_s \), drain-source voltage \( V_{DS} \) and gate voltage \( V_{GS} \), there waveforms are displayed in the oscilloscope. The main test setup parameters are shown in Table I.

![Diagram of SC current interruption capability test platform of SSCB.](image)

Figure. 4. SC current interruption capability test platform of SSCB. (a) Schematic; (b) Picture.

The experiment steps are as follows: Firstly, close the switch \( S \) by the high-voltage DC power supply to charge the DC-link capacitor \( C_{DC} \). Secondly, FPGA controlled the gate-driver to turn on SiC MOSFET a few microseconds and then turn off. Program the FPGA to change the turn-on time until the SC current saturates.

### TABLE I PARAMETERS IN THE TEST

| Symbol | Value   | Descriptions                     |
|--------|---------|----------------------------------|
| \( V_{DC} \) | 200–400 V | DC-bus voltage                   |
| \( L_{fault} \) | 13/30/60/160 μH | fault inductor                  |
| \( DUT \) | 1.7 kV, 72 A | C2M0045170P from Wolfspeed   |
| \( R_{on} \) | 10 Ω   | gate resistor                    |
| \( R_{off} \) | 100 Ω  | gate resistor                    |
| \( R \) | 2 Ω     | resistor of RC snubber circuit    |
| \( C \) | 300nF   | capacitor of RC detection circuit |
| \( V_{G} \) | -5/+20 V | gate voltage                      |
| \( T \) | 50–150°C | junction temperature             |

3.1. **SSCB Failure Mode**

The turn-off failure of SSCB causes the SC current to continue rising rapidly, which seriously threatens the safety of the DC power distribution system and even causes the system to be destroyed. It’s important to clearly understand the failure mode of SSCB and avoid the occurrence of the failure. Using the test platform shown in Fig. 4 to conduct destructive experiments on SSCB. The DC-link voltage is 700V, the fault inductance is 160 μH.

The failure waveform of SSCB is shown in Fig. 5. SSCB failed after 119 μs of SC fault occurred, the SiC MOSFET loses control and the fault current runaway. Meanwhile drain-source voltage reduces to on-state voltage again, the gate-source is broken down and \( V_{G} \) is maintained at 5V. The SC energy loss is calculated as 1.92 J. The failure of the device is due to severe desaturation. The channel resistance of SiC MOSFET increases with the junction temperature, leading channel voltage \( V_{chan} \) ascends. When channel voltage \( V_{chan}>V_{GS}-V_{TH} \), the device current saturation and channel resistance rapid increase. Hence, high voltage and large current across SiC MOSFET generate great loss, which causes the junction temperature rising. The excessively high junction temperature causes the parasitic bipolar junction transistor (BJT) inside the device to be turned on and latch-up occurs[13], the gate loses control...
of the device. The accumulated junction temperature eventually makes the device breakdown. In the use of SSCB, it should be avoided to enter the severe desaturation zone to work.

![Image](image-url)

Figure 5. Failure mode waveforms for SiC MOSFET based SSCB

3.2. Various DC-link Voltage

The vD-Id curve provided by the data sheet of C2M0045170P is not sufficient to estimate the SC current interruption capability in SSCB conditions. Therefore, the SC test platform is used to test the SC performance at various DC-link voltage from 200 V to 400 V, the fault inductance is 60 μH. When VDS exceeds 200V, the desaturation of SiC MOSFET is more significant and the corresponding current is recorded as saturation current. The experimental waveforms are shown in Fig. 6.

As the DC-link voltage increases, the current rises approximately linearly from 320 A to 400A. In addition, the time for the device to appear desaturated is much earlier. From the experiments results, SiC MOSFET can safely turn off 4.5-5.7 times the rated current, which is much larger than the drain pulse current (2.2 times the rated current) given by the datasheet of C2M0045170P. Changing the DC-link voltage is essentially changing the SC current rise speed di/dt, the saturation current is positively correlated with di/dt. As for the turn-off overvoltage, it is equal to the rated maximum clamping voltage of the MOVs, which indicates that the MOVs have successfully clamped the overvoltage and prevented SSCB from being broken down by the overvoltage.

![Image](image-url)

Figure 6. Experimental results of saturation current and Drain-Source voltage at various DC-link voltage. (a) Saturation current. (b) Drain-Source voltage.

3.3. Various Fault Inductance

The DC power distribution system usually has a large inductance. When the SC fault point is far away from the SSCB, the fault inductance is larger and when the fault occurs at the outlet of the SSCB, the fault inductance is the smallest. The saturation current and the Drain-Source voltage at 400 V DC-link
voltage with various fault inductance are presented in Fig. 7. With a small inductance 13 μH, the saturation current of the device can even reach 500A. Under different di/dt, the saturation current has a significant difference. The SC loss and on-state resistance are calculated as shown in Fig. 8. As the fault inductance decreases, di/dt increases, the SC loss required to reach the desaturation point ($V_{DS}=200V$) is reduced. Meanwhile, the on-state resistance corresponding to the desaturation point is also reduced. The reason can be explained as follows.

\[
R_{CH} = \frac{L_{CH}W_{cell}}{1140C_{ox}(V_{G}-V_{th})} \left( \frac{T}{300} \right)^{2.7}
\]

where $V_{th}$ is the threshold voltage. $L_{CH}$ is the channel length. $W_{cell}$ is the cell width. $C_{ox}$ is the capacitance of the gate oxide. T is the junction temperature. From (8), $R_{CH}$ is proportional to temperature $T$. The thermal effect of the SC current increases the junction temperature of the device. The SC current can be expressed as:

\[
i_f = \frac{V_{DE}(t-t_f)}{L_{fault}}
\]

when the SC current and channel resistance meet the following relationship, the current is saturated.

\[
i_fR_{CH} > (V_G-V_{th})
\]
Smaller inductance or higher voltage makes di/dt larger, so the SC current rises quickly. Due to the large current, \((V_G-V_{TH})\) can be reached at a smaller \(R_{CH}\).

### 3.4. D. Various Junction Temperatures

SiC power semiconductor devices are sensitive to temperature. In order to more comprehensively evaluate the SC current breaking capacity of SSCB, the SSCB is tested at 400 V DC-link voltage, 60 μH fault inductance and various junction temperatures from 50 to 150 ℃. Before starting the experiment, heat the device at the specified temperature for 10 minutes to ensure that the junction temperature of the device is the same as the temperature of the heating plate. The experiment results are shown in Fig. 9. As the junction temperature increases, the current that the device reaches the desaturation point decreases. This phenomenon is consistent with Equation (8). The initial junction temperature of 150 ℃ compared to 50 ℃ reduces the saturation current by 40 A, make desaturation happen 10 μs earlier. Compared with di/dt, the effect of junction temperature on saturation current is not significant.

In conclusion, the rise of SC current increases the junction temperature of the device. A larger di/dt makes the current saturate at a lower junction temperature. Lower junction temperature means shorter junction temperature accumulation time, and the device desaturates earlier. When a SC fault occurs, the saturation current of the device is difficult to predict, and it can usually be measured by actual testing. In order to prevent the SSCB from being severely desaturated during use and testing and cannot be turned off, a protection scheme should be designed.

![Figure 9](image9.png)

**Figure 9.** Experimental results of saturation current and Drain-Source voltage at various junction temperatures. (a) Saturation current. (b) Drain-Source voltage.

![Figure 10](image10.png)

**Figure 10.** Waveform of \(dV_{DS}/dt\) at 400 V, 60μH
4. FPGA-BASED SHORT-CIRCUIT PROTECTION

Severe desaturation of power devices is a precursor to SSCB failure as shown in Fig. 5. Power semiconductor device desaturation is accompanied by a rapid rise in drain-source voltage $V_{DS}$. According to the experimental waveform, $dV_{DS}/dt$ versus $t$ curve can be calculated as shown in Fig. 10. As the SC current increases, the $dV_{DS}/dt$ slowly increases, and when the SC current reaches a certain point, the $dV_{DS}/dt$ increases sharply. According to this desaturation feature, a SC protection circuit can be designed by indirect monitoring the $dV_{DS}/dt$. The structure diagram of the FPGA-based SC protection circuit is shown in Fig. 11. The RC snubber is used to reflect the $dV_{DS}/dt$. The relationship between the voltage and current of the capacitor $C$ can be expressed as:

$$i_C=C \frac{dV_{DS}}{dt}$$

(11)

According to (3), the capacitor $C$ will generate the current $i_C$ flowing through the detection resistor $R_{sense}$. A voltage drop will occur across the resistor. By monitoring this voltage $V_{sense}$, the SC fault can be detected in time. The 0.01% high precision resistance $R_1, R_2, R_3, R_4$ and high-speed operational amplifier AD9631 form a differential amplifier circuit to amplified voltage signal $V_{sense}$, its magnification is 50 times. The high-speed comparator compares $V_a$ with the reference voltage $V_{ref}$. Set the threshold voltage of $V_{sense}$ for SC protection operating as 5mV and the reference voltage $V_{ref}$ is 0.25V. When $V_a$ is greater than the reference voltage, the comparator outputs a high level voltage, which is transmitted to FPGA through the optical fiber for logical comparison. FPGA controls Gate Driver to turn off SiC MOSFET. Zener diodes $Z_{d1}, Z_{d2}$ and $Z_{d3}, Z_{d4}$ protect AD9631 and TL3016 separately from being destroyed. Zener diodes $Z_{d1}$ and $Z_{d2}$ prevent the gate voltage from exceeding the safe range.

![Figure 11. Protection scheme of the FPGA-based SC protection](image)

Fig. 12. shows the proposed FPGA-based SC protection circuit picture. In order to verify its effectiveness, it was tested under the experimental conditions of 400 V DC-link voltage and 60 $\mu$H fault inductance. The RC values of the RC snubber circuit are selected as 2$\Omega$, 30nF. In order to eliminate the influence of voltage noise and system parasitic parameters on the protection, a 240ns time delay is set in FPGA. The experimental results are shown in Fig. 13. The protection acts when the SC current reaches 150A, and successfully turns off the SSCB, avoiding serious desaturation. The response time of protection is mainly determined by AD9631, TL3016 and FPGA delay program, about 260 ns. Due to the 7$\mu$s delay in the protection, the current-limiting reactor should be used when SSCB is turned on.
5. CONCLUSION
The SC current interruption capacity test platform is built for SiC MOSFET based SSCB. The test was carried out under various DC-link voltages, fault inductances and junction temperatures. SSCB can successfully turn off the SC current before the desaturation point ($V_{DS}=200$ V). The saturation current corresponding to the desaturation point is positively correlated with $di/dt$. When $di/dt$ is small, such as 2.5 A/μs, the saturation current is 340A. And when the $di/dt$ is relatively high, such as 30 A/μs, the saturation current is 500A. The failure mode of SiC MOSFET based SSCB is the sharp rise of the junction temperature after severe desaturation, which makes the parasitic BJT conduction and latch-up. The saturation current is difficult to predict. In order to avoid the occurrence of severe desaturation due to excessive SC current exceeding saturation current, a SC protection scheme is proposed. The SC protection circuit detects the fault when the SC current reaches 200A, which is much lower than saturation current 400A.

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