Low-Power Logic-in-Memory Complementary Inverter Based on p-WSe$_2$ and n-WS$_2$

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Transition metal dichalcogenides have been considered as candidate materials to construct logic-in-memory devices for realizing non-von-Neumann architecture. Thus, reducing the power consumption is extremely critical for their applications in big data and artificial intelligence. Here, a low-power logic-in-memory device is demonstrated by constructing complementary inverter with p-WSe$_2$ and n-WS$_2$ transistors. By engineering the interface states between WSe$_2$ (WS$_2$) and substrate artificially, non-volatile memory with resistance ratio of $10^4$ and $10^3$ after 500 s are achieved in individual WSe$_2$ and WS$_2$ transistors, respectively. Furthermore, a complementary inverter with a retention time longer than 500 s is realized by connecting p-WSe$_2$ and n-WS$_2$ transistors. More importantly, the static operating source-drain current $I_{ds}$ of this inverter is around 0.5/0.1 nA at low/high resistance states with source-drain voltage $V_{ds}$ = 5 V, and the hysteresis window is located around 0 V, both of which can reduce the energy consumption dramatically and leads to the low operation power. This work provides a convenient strategy to build a non-von-Neumann device toward post-Moore information processing technology.

1. Introduction

Over the past few decades, the data size and computation capability have experienced explosive growth.\[1\] The evolution of integration density and computation capacity could be described by Moore’s law. However, the Moore’s law cannot be continuously valid if the transistors are further scaled down to “quantum regime.”\[2\] The fabrication technique limit, tunneling carriers and severe heating issue render that the size of transistors will reach its absolute limit soon. To maintain the Moore’s law, alternative materials platform should be explored to overcome those challenges. Recently, it has been demonstrated that atomically thin 2D materials could be used as channel materials to scale down the transistor size dramatically.\[3\] Tunneling effects and heating problem can be relieved significantly in 2D materials based transistor due to their excellent electronic and thermal properties.\[4\] On the other hand, memory and data processing units are separated in conventional von Neumann architecture. The communication procedures between processor and memory limit the computation speed and result in high power consumption. To meet the requirement of today’s state-of-the-art technology such as big data, neuromorphic computing, and artificial intelligence, non-von Neumann architecture in which processor and memory are operating parallel has been proposed in several platforms. Importantly, 2D materials are proposed as a promising platform for integrated non-von Neumann chips.\[5\]

To sum up, 2D materials not only increase the integration density, but also can be used to realize non-von Neumann system. Transition metal dichalcogenides (TMDs) are a kind of important materials in 2D materials family and have been extensively studied due to their excellent physical properties and potential applications, including transistors,\[6\] lasers,\[7\] photodetectors,\[8\] memory,\[9\] spintronic,\[10\] and valley electronic devices. Moreover, logic and memory function could be achieved simultaneously in an individual TMDs transistor.\[12\] Although it can integrate the logic and memory function with an individual TMDs transistor, those devices are switching between high resistance state (HRS) and low resistance state (LRS). Thus, large current in LRS lead to high power consumption. Complementary inverter is a key element to construct TMDs based logic circuits and it also can reduce the power consumption.\[13\] Therefore, it is of great importance to develop complementary inverter with integration of logic and memory functions.

Here we report a low-power logic-in-memory complementary inverter with p-WSe$_2$ and n-WS$_2$ transistors. All the sample are prepared by dry transfer method to guarantee the high quality of TMDs flakes and good Au/TMDs contact.\[14\] Non-volatile memory is realized in individual WSe$_2$ and WS$_2$...
transistor, which is attributed to the charge traps at the interface. An inverter is realized by connecting WSe$_2$ and WS$_2$ transistor with complementary memory effect. Because WSe$_2$ and WS$_2$ are always operating at opposite resistance states, the static current of the inverter is at the order of nanoampere. In addition, the hysteresis window is located at 0 V, reducing the power consumption dramatically.

2. Results and Discussion

Figure 1a shows the schematic illustration of WSe$_2$/WS$_2$ inverter on Si substrate with a 300 nm SiO$_2$ serving as the dielectric layer. Silicon wafers were rinsed with isopropanol and deionized water, and subsequently cleaned by oxygen plasma. The oxygen plasma treatment can induce trap states at the interface between WSe$_2$(WS$_2$) and SiO$_2$, which is critical to realize the hysteresis as reported in our previous work.$^{[15]}$ WSe$_2$, WS$_2$ layers and electrodes were fabricated by dry transfer method (see details in Section 4).

We firstly investigate the electric properties of individual WSe$_2$ and WS$_2$ transistors. The output curves of WSe$_2$ and WS$_2$ are shown in Figure S1, Supporting Information. The symmetrical output curves in linear coordinates reveal the excellent contact between Au and WSe$_2$(WS$_2$). Figure 1b,c are the transfer characteristics of individual WSe$_2$ and WS$_2$ transistors under different $V_{ds}$, respectively. $I_{ds}$ continuously decreases (increases) for WSe$_2$ (WS$_2$) with the increased gate voltage $V_g$, suggesting WSe$_2$ (WS$_2$) is p-type (n-type) semiconductor. The opposite polarities of WSe$_2$ and WS$_2$ meet the basic requirement to build a complementary inverter.

Figure 2a,b are the transfer curves of the WSe$_2$ and WS$_2$ in logarithmic coordinates with $V_{ds} = 3$ V. The black and red arrows represent forward and backward $V_g$ sweep directions. Both curves have obvious hysteresis caused by interface states between WSe$_2$(WS$_2$) and SiO$_2$, and the mechanism will be discussed below.$^{[15,16]}$ Consequently, a memory can be achieved by using the hysteresis. The hysteresis window of WSe$_2$ and WS$_2$ are 0–30 V and -30–0 V, respectively. For $V_g = 0$ V in forward direction, WSe$_2$ is in high resistance cutoff state, while WS$_2$ is in low resistance conduction state. On the contrary, resistance states of WSe$_2$ and WS$_2$ are reversed in backward direction. It is worth to note that HRS and LRS always appear simultaneously in this inverter regardless of sweep direction, which is the main character of the complementary memory devices.

Furthermore, endurance and retention performance were investigated. Figure 2c,d (upper panel is source-drain current and lower panel is applied gate pulse) are endurance characteristics within 10 cycles by applying $V_g = \pm 50$ V pulses. The HRS and LRS current remain unchanged within 10 cycles, indicating the reliability of WSe$_2$ and WS$_2$ transistors. Figure 2e,f show the retention characteristics of the HRS and LRS for WSe$_2$ and WS$_2$ transistors, respectively. WSe$_2$ transistor exhibits HRS/LRS ratio of $10^4$ after 500 s, and WS$_2$ transistor also has a HRS/LRS ratio of $10^3$ after 500 s. It can be clearly seen that WSe$_2$ and WS$_2$ have opposite resistance states under the same pulse. Therefore, the output current is expected to be small if those two transistors are connected to form an inverter.
We then investigate the mechanism of resistance states evolution. The on (LRS) and off (HRS) states of WSe$_2$ and WS$_2$ under $\pm 50 \text{ V}$ pulses are schematically shown in Figure 3a. According to previous reports,$^{[17]}$ the oxygen plasma treatment of SiO$_2$ substrate would create hydroxyl-group (–OH) at the surface that would attract H$_2$O and O$_2$. Electron trapping and de-trapping within the interface states take place under +50 and −50 V gate pulses respectively, which corresponds to H$_2$O/O$_2$ redox as following equation:$^{[17c]}

$$\text{O}_2 + 2\text{H}_2\text{O} + 4e^{-} (\text{WSe}_2/\text{WS}_2) = 4\text{OH}^{-}$$ \hspace{1cm} (1)

When a positive $V_g$ is applied in Figure 3b, electrons are trapped in interface states. The oxidation reaction takes place and electrons in WSe$_2$/WS$_2$ transfer from H$_2$O/O$_2$ to form OH$^-$. As a result, hole concentration of p-type WSe$_2$ increases, while electrons concentration of n-type WS$_2$ decreases as illustrated in top panel in Figure 3a. Therefore, WSe$_2$ transists to LRS and WS$_2$ changes to HRS. The reversed reduction process takes place under a negative $V_g$ as shown in Figure 3c. The electrons de-trapping process will render WSe$_2$ to HRS and WS$_2$ to LRS. To understand how the carrier concentration varies with $V_g$ during electrons trapping and de-trapping process, we specifically measured the transfer curve of WSe$_2$ transistor when $V_g$ is changed gradually (Figure S2, Supporting Information). When the $V_g$ decrease gradually from +50 V with a triangle pulse, $I_{ds}$ declines first and then increase (Figure S2b,c, Supporting Information), which is corresponding to the electrons depletion and holes accumulation process (Figure S2d, Supporting Information). The memory characteristics are related to the hysteresis opening size of the transfer curve. To investigate the mechanism of hysteresis, WSe$_2$ and WS$_2$ transistor are prepared based on different interface states, which show marked difference in hysteresis (Figure S3, Supporting Information). The charge transfer occurs in interface states during the applying bias (Figure S3a, Supporting Information), which causes the hysteresis of the transfer curve of WSe$_2$ and WS$_2$ transistors (Figure S3c,e, Supporting Information). In contrast, an inhibition of interfacial charge transfer is observed once the silicon wafer is covered with h-BN layer (Figure S3b, Supporting Information). Accordingly, the hysteresis of WSe$_2$ and WS$_2$ transistors are almost negligible (Figure S3d,f, Supporting Information). At the same time, the transfer curves of WSe$_2$ transistor indicate different hysteresis opening sizes by varying the time of oxygen plasma treatment of silicon wafers (Figure S4, Supporting Information). As the time of oxygen plasma processing the silicon wafer increases, the hysteresis window increases, which demonstrates the correlation between hysteresis and oxygen plasma treatment of silicon wafers.

An inverter was experimentally constructed as shown in Figure 4a. Figure 4b is the corresponding optical image of as-fabricated device. After applying ±50 V pulses as input signal ($V_{in}$), the output signal ($V_{out}$) switches between high-level (≈5 V) and low-level (≈0.6 V) voltage in Figure 4c. The output signal almost remains unchanged after repeating tens of cycles, suggesting the reliability of the logic and memory device. The operating current $I_{ds}$ is presented in Figure S5, Supporting Information. Retention and endurance characteristic are shown in Figure 4d,e. The output voltage changes with $V_{ds}$ and remains constant for 500 s and remaining unchanged for 100 cycles as well, which further evidence the excellent performance of inverter based memory. More importantly, the static operating current $I_{ds}$ is around 0.5/0.1 nA at LRS/HRSs with $V_{ds} = 5 \text{ V}$ as shown in Figure S6, Supporting Information, which results in 0.25/0.5 nW for on/off states. The memory function is further evidenced by the hysteresis response of the inverter in

![Figure 2](image_url). a,b) The transfer curves of the WSe$_2$ and WS$_2$ transistors. The black and red arrows represent scanning direction. c,d) Resistance states evolution under $V_g = \pm 50 \text{ V}$ pulses for WSe$_2$ and WS$_2$ transistors. e,f) Retention times in different resistance states for WSe$_2$ and WS$_2$ transistors.
Figure 3. a) Schematic of the HRS and LRS of WSe2 and WS2 under $V_g = \pm 50$ V pulses, on and off represent LRS and HRS respectively. b) Electrons trapping under $+50$ V. c) Electrons de-trapping under $-50$ V.

Figure 4. a) Schematic structure of the inverter. The red arrow is the operating current of the inverter. b) Optical image of the device with scale bar of 10 µm. c) Dynamic memory properties of the inverter. d) Retention characteristic. The black/brown red/purple and blue/green curves correspond to $V_{ds} = 10$, 8, and 5 V (pulse $V_g = \pm 50$ V), respectively. e) Endurance characteristic. f) Hysteresis characteristic.
3. Conclusion

We demonstrated a complementary inverter with logic and memory function by integrating p-WSe₂ and n-WS₂ transistors together to break the von Neumann architecture. The memory function originates from the artificial engineering of the interface states. Because WSe₂ and WS₂ have opposite polarity, there always exist a high-resistance state and low-resistance state regardless of gate voltage. Consequently, the overall current can be reduced dramatically when they form an inverter. The static operating current $I_{DS}$ of the inverter is at the order of nanoampere and the hysteresis window is located at $V_{in} = 0$ V, both of which can reduce the power consumption. Our work demonstrates a convenient and effective strategy to design energy efficient logic and memory device with non von Neumann architecture. Considering the fact that the atomic thickness of TMDs materials also can increase the integration intensity, this kind of complementary inverter can be promising in the post-Moore information processing technology.

4. Experimental Section

**Device Fabrication:** WSe₂ and WS₂ thin flakes (10–40 nm) were obtained by mechanical exfoliation from bulk crystals and then transferred to the plasma cleaned silicon wafer by a dry transfer method. The thermal evaporation Au electrodes were peeled onto a polydimethylsiloxane and plasma cleaned silicon wafer by a dry transfer method. The thermal evaporation Au electrodes were peeled onto a polydimethylsiloxane and plasma cleaned silicon wafer by a dry transfer method. Finally, the device was annealed at 300 °C under Ar atmosphere in a tube furnace with flow rate of 100 sccm and pressure of 1 Torr (Lindberg/Blue MTFS035K1-1).

**Electrical Characterization:** The electrical measurements were performed in a probe station (Lakeshore, P500). Source/measurement unit (Keysight B2902A) was used to apply source-drain voltage and input signal. The nanovoltmeter (Keithley 2182A) was used to measure the output signal. All measurements were conducted under vacuum of 10⁻⁴ Torr at room temperature.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Data Availability Statement**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Keywords**

inverters, logic-in-memory, non-von Neumann, transition metal dichalcogenides
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