Research and Design of X-band Low Noise Amplifier Based on CMOS Process

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Abstract. Based on CMOS process, a low noise amplifier (LNA) operating at 7.4GHz ~11.4GHz was designed. The two-stage differential cascode structure is adopted. Transformer was used to achieve inter-stage matching. Balun was used to achieve input and output matching, which reduces the number of inductors used, effectively reduces the chip size while ensuring good gain and noise figure. The actual measurement results show that the power gain at the center frequency of 9.4GHz is 27dB, the maximum noise figure is less than 3.82dB, the output power 1dB compression point is greater than 8dBm, the chip area is only 0.41mm×0.83mm (excluding PAD).

1. Introduction

With the rapid development of silicon-based semiconductor technology, the characteristic size of transistor is constantly decreasing. At present, the most advanced process node has reached less than 5nm. Silicon-based process has the advantages of the low power consumption, high integration and easy integration with digital circuit [1], which can make up for the deficiency of compound semiconductor. In recent years, the research on silicon-based microwave amplifier has been gradually enriched in China, but there is still a widening gap between domestic and foreign research results. As the first active circuit in the RF receiver, the noise performance of LNA directly determines the noise characteristics of the whole RF receiver system. The silicon-based process has the disadvantages of large substrate noise and low gain, and the parasitic effect of the transistor itself will further deteriorate its gain and noise performance, which makes the design of LNA more difficult.

In this paper, based on CMOS process, a two-stage differential structure LNA working in 7.4GHz~11.4GHz is designed and manufactured. The transformer is used for inter-stage matching, and the input and output matching is realized by balun.

2. Circuit Design

2.1. LNA Design

Aiming at the problems of poor noise figure (NF) and low gain of silicon-based process amplifier, the LNA designed in this paper adopts differential cascade structure. Through the source cascading inductor, the amplifier stability is improved while the input matching is improved [2]. The resistive negative feedback improves the gain flatness and facilitates impedance matching. Transformer is used for inter-stage matching and reducing the circuit size.
Figure 1. Two-stage LNA schematic.

For LNA, the bias voltage will affect the gain, noise, power consumption and other aspects of the system. Gain, linearity, power consumption and other factors should be considered when selecting bias voltage. Through simulation of drain current changing curve with bias voltage, the bias voltage is selected from 0.5V to 0.9V, which ensures that the transistor operated in the saturated region, with good gain and linearity, while not consuming too much power. The change of maximum available gain (MAG) and noise figure (NF) of common source (CS) stage and common gate (CG) stage with bias voltage was simulated respectively. And the bias voltage of CS was 0.7V and the bias voltage of CG was 1.8V. This ensures that the amplifier has a low noise figure and sufficient gain.

In order to provide sufficient gain, the LNA designed in this paper adopts two-stage amplifier. The noise figure of the multi-level cascade circuit is expressed as:

$$NF = NF_1 + \frac{NF_{1-1}}{G_1} + \frac{NF_{2-1}}{G_1G_2} + \cdots + \frac{NF_{n-1}}{G_1G_2 \cdots G_{n-1}}$$

In this equation, $NF_n$ and $G_n$ represent the NF and gain of the $n$th stage circuit, respectively.

It can be seen that the NF of the first stage amplifier directly determines the noise performance of the whole amplifier. Therefore, NF needs to be taken into special consideration when designing the first stage amplifier. The second stage amplifier provides high gain as far as possible while satisfying the NF.

Figure 2. Small-signal equivalent circuit.

According to the small signal equivalent circuit of the differential cascade amplifier (Fig 2), the maximum voltage gain of the differential circuit is

$$\frac{V_{out}}{V_{in}}(j\omega_0) = \frac{g_mR - j\omega_0 R C_{gd}}{1 + Z_1 + jZ_2}$$

$$Z_1 = R(r_s + r_d)(\omega_0 C_{gd})$$

$$Z_2 = \omega_0(r_s + r_d)[C_{gs} + C_{gd}(1 + g_m R)]$$

According to the equation, the parasitic capacitance affects both the numerator and the denominator and significantly reduces the voltage gain of the transistor. Moreover, the negative component introduced by the parasitic capacitance in the input admittance will affect the circuit stability. Cascode
is a CS and CG cascade. On the basis of the CS stage with negative source feedback, the CG stage can not only improve gain, but also suppress the parasitic capacitance of the CS stage, which improves the noise performance and stability of the system.

2.2. Transformer Matching
The traditional matching method is LC matching. Impedance selection is carried out according to the equal noise circle and equal gain circle obtained by Smith chart.

In order to achieve better noise matching and input impedance matching, this design uses balun to replace the traditional LC network for input matching. As a passive device, balun can realize DC isolation, single-ended signal conversion to differential signal, impedance matching and other functions\(^3\). The matching network with LNA designed by balun can effectively reduce the number of inductors used, thus avoiding the loss caused by additional inductors, and greatly reducing the chip area. In addition, balun can replace the capacitor to achieve DC isolation, reducing the difficulty of layout design. This balun uses two layers of metal and is implemented in a planar structure. The main geometric parameters are microstrip line width, line spacing and external diameter. It is pretty difficult to design a balun with good noise matching and input impedance matching just by adjusting these parameters. Therefore, balun geometric parameters can be adjusted to a relatively reasonable value first, and then the capacitance or inductance can be connected outside the input end according to Smith chart to achieve noise matching and input impedance matching. So we choose a compromise method, in which the inner inductor of balun is connected, and the matching is further adjusted by adjusting the inner inductor to achieve good standing wave performance and noise performance.

2.3. Stability problem
As the first stage of the receiver, LNA needs to be stable in any frequency band, otherwise the gain peak will appear, and the poor linearity will cause the circuit system to fail to work normally.

A common way to improve the stability of a LNA is cascade the inductor between the source and the ground. But the negative feedback due to series inductance will lead to gain loss. Therefore, the value of the source feedback inductance is generally small and can be replaced by the microstrip line. Another approach is to generate feedback by a parallel resistor between the gate and drain. The resistor determines the depth of the feedback. A zero point and two poles far apart are introduced to improve the gain flatness and the stability of the LNA. In addition, there is a method of series attenuator at the end of the multistage LNA, but it will bring great loss to the gain. This circuit design adopts the method of combining the source cascade inductance and the parallel resistance between gate and drain. The small value of cascade inductance can improve stability without bringing too much gain loss. Feedback is introduced through the shunt resistor to improve gain flatness and facilitate impedance matching.

The necessary and sufficient conditions for the circuit to be unconditionally stable are as follows.

\[ |S_{11}| < 1 \]
As can be seen from the Fig4, $K_f$ is greater than 3.5 in the full frequency band, and the circuit is unconditionally stable.

2.4. Layout Design

The MOSFET with different the number of fingers and gate width is simulated by Cadence. After comparison, the MOSFET with single finger gate width of 3 um and the number of fingers of 24 is selected for circuit design to achieve the expected effect.

It is necessary to design the layout symmetrically when designing the layout of the LNA. The top metal layer is thicker than other metal layers, with smaller resistivity and smaller parasitic capacitance. Therefore, the top metal is selected for signal wiring, the bottom metal for bias wiring, and the middle layer metal for connecting the lower layer, which can effectively reduce the influence of crosstalk between wires. A certain distance should be maintained between the active device and the transformer to avoid magnetic interaction between them. Dummy resistor can be drawn when drawing the feedback resistor to improve the accuracy of physical graphics in subsequent circuit fabrication.

After the layout design is completed, the passive part of the layout is imported into ADS for EM simulation, and S parameters are extracted and imported into schematic through the nport component in Cadence for co-simulation with the transistor. After the simulation results meet the expected requirements, it is necessary to check the design rules and compare the layout with the schematic to ensure that the electrical properties are consistent. These are based on the DRC and LVS functions in the Calibre column in Cadence. The final design layout and the physical picture of the chip are shown in the Fig5, and the chip size is 0.41mm×0.83mm(excluding PAD).
3. Test Result

The S parameters, input-output standing wave ratio and noise figure of LNA were tested by microwave network analyzer. The comparison between the test results and the simulation results is shown in the Fig6.

![Figure 6](image)

**Figure 6.** Comparison of S parameter test results and simulation results of LNA.

According to the comparison curve between the test results and the simulation results, the measured results show that the gain of the LNA from 7.4GHz to 11.4GHz is (24.5±1.5dB), which basically coincidences with the simulation curve. According to the input-output standing wave comparison curve, the typical input standing wave ratio is 1.4:1, the typical output standing wave ratio is 2:1. The measured value of the input standing wave is basically consistent with the trend of the simulation curve with a slight deviation, while the measured value of the output standing wave is slightly worse than the simulated value, indicating that the measured data of the active device model is slightly different from the model data.

![Figure 7](image)

**Figure 7.** NF test curve.

According to the noise figure test curve(Fig7), the NF is less than 3.82dB from 7.4GHz to 11.4GHz. Because it is difficult to achieve ideal performance in all aspects when designing LNA. It is necessary to make a trade-off among NF, gain, frequency band, input and output standing wave. Therefore, the output standing wave is relatively poor. The simulation result of DC power consumption is 41.08mA, and the test result is 41mA. At 9.4GHz, the output 1dB gain compression power is 8.16dBm.
Table 1. The performance comparison between the LNA in this paper and the LNA based the same process in other recent literatures.

| Process         | 180nm CMOS | 65nm CMOS | 90nm CMOS | 180nm CMOS | This design |
|-----------------|------------|-----------|-----------|------------|-------------|
| Frequency (GHz) | 6.4~7.4    | 9.65~10.65| 8~12      | 15.1~16.6  | 7.4~11.4    |
| Gain (dB)       | 18         | 28        | 24        | 15.2       | 27          |
| NF (dB)         | 2.85(min)  | 1.8(min)  | 3.3~3.8   | 5(min)     | 3.2~3.82    |
| S11 (dB)        | -13        | -28.2     | <-10      | <-10       | <-12        |
| Area (mm²)      | 0.55       | 0.2       | 0.96      | 0.144      | 0.34        |

As shown in Table 1, by comparing the LNA performance based the same process in recent years, it can be seen that the LNA designed in this paper ensures good gain, noise and standing wave ratio while the chip size is relatively small.

4. Conclusion
In this paper, we use CMOS process to design a two-stage differential structure LNA working in 7.4GHz~11.4GHz. Transformer is used for the inter-stage matching. Input and output matching is realized by balun. The test results show that the LNA has a working frequency range of 7.4GHz~11.4GHz. Gain is (24.5±1.5dB), noise figure is less than 3.82dB, output 1dB compression point is greater than 8dBm. This verifies that the implementation of matching using balun and transformer can ensure good performance while effectively reducing the chip size.

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