A New MMC Sub-Module Topology with DC Fault Blocking Capability and Capacitor Voltage Self-Balancing Capability

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Abstract: A large number of modular multilevel converters (MMC) are connected to HVDC transmission systems nowadays. This paper aims at the short-circuit fault in the DC line of the HVDC transmission system and the problem of capacitor voltage imbalance in MMC, proposing a new type of MMC sub-module, which has both the DC fault self-clearing ability and the capacitor voltage self-balancing ability. This sub-module combines the topology of half bridge and full bridge. It uses the reverse capacitor voltage to forcibly turn off the conducting diode to block the fault current loop. At the same time, the two capacitances charge and discharge states are consistent by utilizing the operating mode of the sub-module. It is possible to directly achieve a self-balancing capacitor voltage without complex balancing voltage control. The MATLAB/Simulink simulation verifies the effectiveness of the DC fault blocking capability and capacitor voltage balance capability of the proposed sub-module.

Keywords: modular multilevel inverter; DC fault clearing ability; improved sub-module topology; voltage self-balancing ability

1. Introduction

The flexible DC transmission technology of MMC has the advantages of high modularity, low switching frequency and low harmonic content, which makes it widely used in the fields of HVDC transmission and power conversion [1,2]. When MMC is applied to HVDC transmission, the following two issues must be considered.

1) How to deal with the short-circuit fault of the DC side line. Once the DC system fails, the lower damping results in a higher rate of current rise, so that the current removal is more difficult than the AC system [3,4]. At present, AC circuit breakers, DC circuit breakers and improved sub-module topology are mainly used to block fault current.

As shown in Table 1, AC circuit breakers are widely used [5], but the AC circuit breaker fault removal time is usually between 45–150 ms. The power supply reliability and operating speed of AC circuit breakers are far from reaching the requirements of the DC grid [6]. The DC circuit breaker can quickly cut off the fault [7,8]. However, since DC does not have a natural zero-crossing point, problems such as difficulty in line arc extinguishing are caused, which brings great challenges to the technical research and investment costs of DC circuit breakers [9–11]. Therefore, it is the most effective method to absorb the fault current through the improvement of the converter topology and the cooperation with the control strategy to realize the rapid isolation of the fault. This method is controlled by pulse signals without mechanical switching [12,13]. The fault clearing time and the recovery time of the system after the fault are relatively fast, so it can adapt to the development requirements of high-voltage, large-capacity and long-distance power transmission.

The improved sub-module topology mainly includes symmetrical output type and asymmetrical output type. Symmetric output sub-module topology includes full-bridge sub-modules (FBSM) [14,15], enhanced self-blocking sub-module (SBSM) [16], three-level clamp...
sub-modules (CCSM) [17], five-level cross connected double sub-modules (CCDSM) [18] and serial connected double sub-modules (SCDSM) [19]. Asymmetric output sub-modules include clamp double sub-modules (CDSM) [20] and hybrid bridge sub-modules (HBSM) [21]. The improved topology DC fault blocking suppression has all or part of the sub-modules in the blocking or bypass state. After the fault is blocked, the sub-module power circuit may cause asymmetrical charging of the capacitor, which is not conducive to restarting the MMC.

Table 1. Comparison of methods to deal with a short circuit fault of a DC side line.

| Method                          | Advantages                                                                 | Disadvantages                                                                 |
|---------------------------------|---------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| AC circuit breaker (ACCB)       | ACCB is a straightforward solution with the good economic efficiency and the high technical maturity [5]. | ACCB operating speed is slow, and the recovery time is long after the fault is removed [6]. |
| DC circuit breaker (DCCB)       | DCCB offers very low conduction losses and can interrupt the DC fault current in a very short time [7,8]. | High-voltage and large-capacity DC circuit breakers are facing huge challenges in terms of technical research and investment costs [9–11]. |
| Improved topology               | Improved topology does not require mechanical switch action, so the fault clearing time and the system recovery time after the fault are relatively fast [12]. | The cost of improved topology increases, but it is lower than DCCB [13]. |

(2) How to solve the problem of capacitor voltage balance. The main research methods focus on the capacitor voltage equalization strategy, the voltage equalization algorithm and the voltage equalization topology research. Although the research on the capacitor voltage balance strategy and the voltage equalization algorithm can accurately regulate the capacitor voltage, the data collection pressure is large and the calculation is complicated [22,23]. There is no complicated calculation process in the research of the equalization topology, but the investment cost needs to be considered. Bai proposed the strategy of rotating the carrier to achieve the balance of capacitor voltage and simplify the modulation algorithm [24]. Ghazanfari proposed a strategy to evenly distribute the switching gate signals by using PCC (permutation cyclic coding), which balances the voltage of the submodule capacitors [25]. Wang proposed a new CPS-PWM (Carrier Phase Shift Pulse Width Modulation) scheme, allocating new drive signals with charging capability to the corresponding unbalanced sub-modules, which can balance the capacitor voltage [26]. Mora realized the balance of capacitor voltage by using model predictive control, aiming to solve the problem of optimal control [27]. Shu proposed a sub-module with two-way voltage self-balancing ability, which can suppress well the circulating current [28]. Tan proposed a topology using clamp diodes to connect D-FBSM and HBSM (half-bridge sub-modules), which eliminates the fault current through the single conductivity of the diode [29].

In view of the above problems, improving the sub-module topology is the most effective method. Most of the existing improved sub-modules can only solve one of the problems, but the proposed topology can solve two problems at the same time. By combining HBSM and FBSM, this paper proposes a new type of sub-module with the capability of fault current self-clearing and capacitor voltage self-balancing: Combined Half-Bridge Full-Bridge Sub-Module (CHBFBSM).

2. Topological Structure and Operation Mode of CHBFBSM

On the basis of HBSM and FBSM, this paper uses the combination method to derive a new type of sub-module CHBFBSM, which has both DC fault current blocking capability and capacitor voltage self-balancing capability. Then, the derivation process and operation mode of CHBFBSM are introduced.
2.1. Topological Structure

The topological structure of HBSM is shown in Figure 1a. The topological structure of FBSM is shown in Figure 1b. CHBFBSM combines HBSM and FBSM. By sharing a switch tube, the utilization rate of the device is improved. A diode is added to prevent the sub-module from being short-circuited after all IGBTs are blocked when a fault occurs. This article proposes a topology which combines HBSM and FBSM according to the method shown in Figure 1, and the specific structure is shown in Figure 2. The topological structure consists of five IGBTs $T_1$–$T_5$ and their anti-parallel diodes $D_1$–$D_5$, a single diode $D_6$ and two capacitors $C_1$ and $C_2$.

![Topological Structure of CHBFBSM](image)

**Figure 1.** CHBFBSM combination diagram: (a) HBSM; (b) FBSM.

2.2. Operating Mode

During normal operation, CHBFBSM works in the following five modes, by adjusting the on and off states of the switch tube.

- **Mode 1:** The switch tubes $T_1$ and $T_3$ are turned on. The capacitors $C_1$ and $C_2$ are bypassed. The output voltage of CHBFBSM is 0.
- **Mode 2:** The switch tubes $T_2$ and $T_3$ are turned on. The capacitor $C_1$ is input and $C_2$ is bypassed. The output voltage of CHBFBSM is $U_{c1}$.
- **Mode 3:** The switch tubes $T_1$ and $T_5$ are turned on. The capacitor $C_2$ is input and $C_1$ is bypassed. The output voltage of CHBFBSM is $U_{c2}$.
- **Mode 4:** The switch tubes $T_1$, $T_4$, and $T_5$ are turned on, resulting in two loops. Loop 1 circulates switches $C_1$, $T_4$, and $D_5$. Loop 2 circulates $D_6$, $T_1$, $C_2$, and $D_5$. The capacitors $C_1$ and $C_2$ are connected in parallel. The output voltage of CHBFBSM is $U_{c1}/U_{c2}$.
- **Mode 5:** The switch tubes $T_2$ and $T_5$ are turned on, generating loops $C_1$, $D_2$, $C_2$, and $D_5$. The capacitors $C_1$ and $C_2$ are connected in series, and the output voltage of CHBFBSM is $U_{c1} + U_{c2}$.
When a fault occurs on the DC line, all switching devices are in an off state. When the bridge arm current $i_{\text{arm}} > 0$, the current forms a loop through $C_1$, $D_2$, $C_2$, and $D_5$. When the bridge arm current $i_{\text{arm}} < 0$, the current forms a loop through $C_1$, $D_4$, $C_2$, and $D_3$. The current path formed by the freewheeling diode inside the sub-module is shown in Figure 3. The bridge arm current will drop rapidly as the reverse capacitor voltage in the loop increases.

![Figure 3. Current path when the fault is blocked: (a) $i_{\text{arm}} > 0$; (b) $i_{\text{arm}} < 0$.](image)

In summary, the operation mode of CHBFBSM can be divided into five normal modes and two blocking modes. The switch state of the device in each mode is shown in Table 2.

| Mode       | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | Output   |
|------------|-------|-------|-------|-------|-------|----------|
| normal operation | 1 | 1 | 0 | 1 | 0 | 0 $U_{C1}$ |
| normal operation | 2 | 0 | 1 | 1 | 0 | 0 $U_{C2}$ |
| normal operation | 3 | 1 | 0 | 0 | 0 | 1 $U_{C1}/U_{C2}$ |
| normal operation | 4 | 1 | 0 | 0 | 1 | 1 $U_{C1} + U_{C2}$ |
| normal operation | 5 | 0 | 1 | 0 | 0 | 1 $U_{C1} - U_{C2}$ |
| blocked $i_{\text{arm}} > 0$ | 0 | 0 | 0 | 0 | 0 | $U_{C1} + U_{C2}$ |
| blocked $i_{\text{arm}} < 0$ | 0 | 0 | 0 | 0 | 0 | $U_{C2} - U_{C1}$ |

3. Analysis of Self-Balancing Characteristics

Under normal operating conditions, CHBFBSM can run in five modes. CHBFBSM mainly operates in mode 1, mode 4 and mode 5, namely the capacitor bypass, capacitor parallel connection and capacitor series connection to balance the sub-module capacitor voltage. In an ideal situation, ignoring the capacitance difference, if CHBFBSM always runs in the above three modes, the charge and discharge of the two capacitors in the sub-module will be consistent, which can ensure the balance of the two capacitors voltage. Next, considering the capacitance difference, the self-balancing characteristics of CHBFBSM are further analyzed.

3.1. Analysis of Impulse Current

The voltage expression of the two capacitors in CHBFBSM is:

$$U_{Ck}(t) = U_0 + \frac{1}{C_k} \int_{t_0}^{t} i(\tau) d\tau$$

(1)

where $U_0$ is the capacitor voltage value at $t_0$; $C_k$ refers to the two capacitor values of the sub-module, $U_{Ck}(t)$ is the capacitor voltage value at time $t$ and $k = 1, 2$; $i$ is the capacitor charging current.
\[
\int_{t_0}^{t_1} i(\tau) d\tau = \Delta q, \text{ then there is:}
\]
\[
\Delta U = U_{C1}(t) - U_{C2}(t) = \frac{C_2 - C_1}{C_1 C_2} \Delta q
\]
where \(\Delta U\) is the voltage difference of the sub-module capacitance.

Considering the tolerance of the film capacitor within \(\pm 5\%\), when the CHBFBSM operates in mode 5, the capacitor is output in series. It can be seen from Equations (1) and (2) that even if the same loop current charges two capacitors with the same initial voltage, there will still be a certain voltage difference between the two capacitors.

Since the control period is very short, it can be approximately considered that the capacitor charging current is constant at \(I\) in a control period \(T_s\), then:
\[
\Delta q = \int_{t_0}^{t_1} i(\tau) d\tau = I(t - t_0) = IT_s
\]

When two capacitors are connected in parallel, the impulse current \(I_b\) can be expressed as:
\[
I_b = \frac{\Delta U}{R} = \frac{C_2 - C_1}{RC_2 C_1} IT_s
\]
where \(R\) is the on-state resistance of the IGBT.

Taking into account the most serious situation, \(C_1\) and \(C_2\) are taken as the largest difference, which can be expressed as:
\[
\begin{cases}
C_1 = (1 - 5\%) C \\
C_2 = (1 + 5\%) C
\end{cases}
\]
where \(C\) is the theoretical value of the module capacitance.

The relationship between \(I_b\) and \(I\) can be expressed as:
\[
\frac{I_b}{I} = \frac{\Delta U}{R} \approx \frac{0.1 T_s}{RC}
\]

It can be seen that the parallel impulse current is determined by the control period. When the control period is very short (usually in the microsecond level), capacitors with a certain difference will not generate excessive impulse current during the parallel connection process.

### 3.2. Energy Analysis

Regarding the IGBT as an ideal switch and the on-state resistance in series, the equivalent circuit of the switching process of CHBFBSM from mode 5 to mode 4 is shown in Figure 4. Mode 5 is a state where switches \(B_1\) and \(B_3\) are open, but \(B_3\) is off. Mode 4 is a state where switches \(B_1\) and \(B_2\) are off, but \(B_3\) is open.

![Figure 4. The equivalent circuit of the switching process.](image-url)
The charge quantity of the circuit before and after switching can be expressed as:

\[
\begin{align*}
Q_c(0^-) &= C_1U_1 + C_2U_2 = C_1U_0 + C_2U_0 + 2\Delta q \\
Q_c(0^+) &= C_1U_3 + C_2U_5
\end{align*}
\]

where \(Q_c(0^-)\) and \(Q_c(0^+)\) are the charges of the circuit before and after the switch; \(U_1\) and \(U_2\) are the voltages of capacitors \(C_1\) and \(C_2\) before switching, with the capacitors connected in series at this time; \(U_3\) is the voltage of capacitors \(C_1\) and \(C_2\) after switching, with the capacitors connected in parallel at this time.

According to the law of conservation of charge, the amount of charge in the circuit remains unchanged before and after switching. \(U_3\) can be expressed as:

\[U_3 = U_0 + \frac{IT_s}{C}\]

The energy \(E(0^-)\) before switching and the energy \(E(0^+)\) after switching can be expressed as:

\[
\begin{align*}
E(0^-) &= 0.5C_1U_1^2 + 0.5C_2U_2^2 \\
E(0^+) &= 0.5C_1U_3^2 + 0.5C_2U_5^2
\end{align*}
\]

The energy loss of the circuit before and after switching can be expressed as:

\[
\Delta E = E(0^-) - E(0^+) = \frac{0.25I^2T_s^2}{100C^2}
\]

Generally, \(IT_s\) is much smaller than \(C\), so the parallel loss is much smaller than 0.25%. Therefore, there will not be too much additional loss during the parallel connection. In addition, the circuit can be approximated as an \(RC\) circuit after switching, and the time constant \(\tau = RC\). Then, only the control period \(T_s > 3\tau\) is required, and the steady state can be reached after switching. The energy transfer is completed, so the voltage self-balance can be well realized.

The above analysis shows that when the capacitances are the same, the module has a complete self-balancing effect. When there are differences in capacitances, selecting an appropriate control period \(T_s\) to complete the self-balancing process will not produce a large impulse current and excessive additional loss. The sub-module voltage can be automatically balanced by mode switching. Therefore, only one capacitor of the sub-module needs to be detected to participate in the sorting calculation. Compared with the voltage sensors required by the traditional half-bridge MMC, the number of voltage sensors required by the proposed topology and the number of voltage signals involved in the control are both reduced by half. Therefore, the system hardware cost is reduced, the calculation burden of the controller is reduced.

4. Analysis of DC Fault Blocking Characteristics

When a DC side fault occurs in the CHBFBSM-MMC system, the capacitor discharges to the fault point. Energy is fed into the AC side, and the DC current quickly rises to a preset threshold. All IGBTs are blocked, and the blocking ability of CHBFBSM on the fault current is used to realize the elimination of the fault. The change of DC current can divide the CHBFBSM fault current clearing process into pre-blocking stage and post-blocking stage. The operation flowchart of the DC fault protection strategy is shown in Figure 5 [30].
4. Analysis of DC Fault Blocking Characteristics

When a DC side fault occurs in the CHBFBSM MMC system, the capacitor discharges approximately equally divided into two groups, and the two groups of sub-modules are discharged alternately in turn. The equivalent circuit of CHBFBSM-MMC is shown in Figure 6. The high system control frequency makes all the sub-modules are in the state of input or removal. According to the sorting algorithm, all sub-modules of each phase can be approximately equally divided into two groups, and the two groups of sub-modules are discharged alternately in turn. The equivalent circuit of CHBFBSM-MMC is shown in Figure 6. $L_{\text{arm}}$ is the inductance of the bridge arm and $R_{\text{arm}}$ is the resistance of the bridge arm; $L_{\text{dc}}$ is the DC line inductance; $R_{\text{dc}}$ is the DC line resistance; $R_f$ is the resistance of the fault point.

4.1. Pre-Blocking Stage

$N_p$ and $N_n$ are, respectively, the number of equivalent capacitors put into the upper and lower bridge arms. $N_c$ is the total number of input capacitors in the single-phase bridge arm. $N$ is the number of sub-modules of a single bridge arm, and the relationship can be expressed as:

\[
\begin{cases} 
N_p + N_n = N_c \\
N_c = 2N 
\end{cases} \tag{11}
\]

If the step wave $N_m$ is an odd number, let one sub-module operate in the capacitor parallel mode and $(N_c - 1)/2$ sub-modules operate in the capacitor series mode. The equivalent capacitance $C_{d1}$ of the bridge arm input can be expressed as:

\[
C_{d1} = C_p / C_n = \frac{C}{N_c - 1} \tag{12}
\]

If the step wave $N_m$ is an even number, all the sub-modules put in are operating in the capacitor series mode, and the equivalent capacitor $C_{d2}$ can be expressed as:

\[
C_{d2} = \frac{C}{N_c} \tag{13}
\]

The high system control frequency makes all the sub-modules are in the state of input or removal. According to the sorting algorithm, all sub-modules of each phase can be approximately equally divided into two groups, and the two groups of sub-modules are discharged alternately in turn. The equivalent circuit of CHBFBSM-MMC is shown in Figure 6. The operation flowchart of the DC side fault ride through protection strategy is shown in Figure 5.
The equivalent circuit shown in Figure 6 can be simplified as a second-order zero-input RLC series circuit. The differential equation and initial conditions can be expressed as:

\[
\begin{align*}
\frac{d^2 u_c(t)}{dt^2} + \frac{R_{eq}}{L_{eq}} \frac{du_c(t)}{dt} + \frac{1}{L_{eq}C_{eq}} u_c(t) &= 0 \\
u_c(0^-) &= 2N_c U_{c0} \\
\frac{du_c(0^-)}{dt} &= -\frac{1}{L_{eq}} I_{d0}\end{align*}
\]

where \(C_{eq} = 3C / N_c + 3C / (N_c - 1)\), where \(C_{eq}\) is the equivalent capacitance of the three-phase bridge arm; \(L_{eq} = L_{arm} / 3 + L_{dc}\), where \(L_{eq}\) is the sum of the equivalent inductance of the three-phase bridge arm and the DC line inductance; \(R_{eq} = R_{arm} / 3 + R_{dc} + R_f\), where \(R_{eq}\) is the sum of the equivalent resistance of the three-phase bridge arm, the DC line resistance and the short-circuit resistance; \(u_c(t)\) is the voltage across the equivalent capacitor \(C_{eq}\); \(u_c(0^-)\) is the initial voltage of the equivalent capacitor \(C_{eq}\); \(U_{c0}\) is the rated value of the sub-module capacitor voltage; \(I_{d0}\) is the steady-state value of the DC current during normal operation.

In the actual system, the equivalent resistance \(R_{eq}\) is much smaller than \(2R_{eq}/C_{eq}\), so the second-order circuit is an underdamped circuit. The solution of the differential Equation is:

\[
u_c(t) = Ke^{-\alpha t} \sin(\omega_d t + \varphi)
\]

where \(\omega_d = \sqrt{\omega_0^2 - \alpha^2}, \omega_0 = 1 / (R_{eq} C_{eq})\), \(\alpha = R_{eq} / (2L_{eq})\); \(\omega_d\) is the oscillation angular frequency; \(\omega_0\) is the resonance angular frequency; \(\alpha\) is the circuit attenuation coefficient; \(\varphi = \arctan(2U_{c0} \omega_d / (\alpha N_c U_{c0} - I_{d0} / C_{eq}))\); \(K = \sqrt{N_c^2 U_{c0}^2 + [(\alpha N_c U_{c0} - I_{d0} / C_{eq}) / \omega_d]^2}\).

The DC side current \(i_{dc}\) can be expressed as:

\[
i_{dc}(t) = KC_{eq} \omega_0 e^{-\alpha t} \sin(\omega_d t + \varphi - \arctan(\frac{\omega_d}{\alpha}))
\]

4.2. Blocking Stage

After the direct current rises rapidly and reaches more than ten times the rated value, it can be detected as a short-circuit fault. When MMC is blocked, the energy stored in the DC network is mainly divided into three parts: the network storage energy before failure, the sub-module capacitor discharge energy and the AC system feed energy. After the MMC is blocked, most of the energy will be fed back to the capacitors, except for a small part of the energy that is dissipated through the resistors. The two capacitors of CHBFBSM are connected in parallel to the fault circuit in reverse. The energy in the bridge arm inductance and the DC link is injected into the capacitor. The capacitor reduces the current in the bridge arm by providing a reverse voltage. At the same time, the AC side charges the
capacitor, and the capacitor voltage rises. Figure 7 shows the specific equivalent circuit. The DC line is simplified to fault point \( f \). \( R_f \) is the resistance where the fault occurs. \( U_a \), \( U_b \) and \( U_c \) are, respectively, the equivalent power supply voltages of \( a \)-phase, \( b \)-phase and \( c \)-phase on the source side. \( R_{\text{arm}} \) and \( L_{\text{arm}} \) are, respectively, the equivalent resistance and the equivalent inductance of the bridge arm. \( u_a \), \( u_b \) and \( u_c \) are, respectively, the equivalent capacitance voltages of the \( a \)-phase, \( b \)-phase and \( c \)-phase bridge arms. The subscripts \( p \) represents the upper bridge arms and \( n \) represents the lower bridge arms.

![CHBFBSM-MMC equivalent circuit when blocked.](image)

When the bridge arm current \( i_{SM} \) > 0, the current forms a loop through \( C_1 \), \( D_2 \), \( C_2 \) and \( D_5 \). At this time, the diode leads the sub-module capacitances into the bridge arm. The short-circuit fault current in the MMC flows through the diode, which charges the sub-module capacitances. The reverse capacitor voltage is used to forcibly turn off the conducting diode, thereby blocking the fault current loop.

\[
U_{ac} = 2N \cdot [U_{D2} + U_{DS} + U_c] - U_f \tag{17}
\]

where \( U_{ac} \) is the line voltage of the AC system between phase \( a \) and phase \( c \); \( U_{D2} \) is the voltage across the diode \( D_2 \); \( U_{DS} \) is the voltage across the diode \( D_5 \); \( U_f \) is the remaining voltage between the DC side poles after the fault; \( U_c \) is the average value of the capacitor voltage in the sub-module.

The capacitor voltage average value \( U_c \) can be expressed as:

\[
U_c = \frac{U_{dc}}{2N} \tag{18}
\]

Thus, the voltage of two diodes can be expressed as:

\[
U_{D2} + U_{DS} = \frac{U_{ac} - U_{dc} + U_f}{2N} \tag{19}
\]

The AC system line voltage meets \( U_{ac} < \sqrt{3}U_{dc}/2 \). Because \( U_{dc} \geq U_f \), the relationship of the diode voltage can be expressed as:

\[
U_{D2} + U_{DS} < 0 \tag{20}
\]
The diodes $D_2$ and $D_5$, which provide the reverse current path, will be turned off due to the reverse voltage, which can cut off the current path from the AC side to the DC side. The DC side cannot feed energy from the AC side, so the DC fault current can be completely eliminated.

When the current of bridge arm $i_{SM} < 0$, it forms a loop through $C_1$, $D_4$, $C_2$ and $D_3$, which can be expressed as:

$$U_{ca} = 2N \cdot [U_{D3} + U_{D4} + U_c] + U_r$$  \hspace{1cm} (21)

where $U_{ca}$ is the line voltage of the AC system between phase $c$ and phase $a$; $U_{D3}$ is the voltage across the diode $D_3$; $U_{D4}$ is the voltage across the diode $D_4$.

The voltage of the two diodes $D_3$ and $D_4$ can be expressed as:

$$U_{D3} + U_{D4} = \frac{U_{dc} - U_{dc} - U_r}{2N}$$  \hspace{1cm} (22)

The combination of the relationship between the amplitude of line voltage in AC system can be shown as:

$$U_{D3} + U_{D4} < 0$$  \hspace{1cm} (23)

It can be obtained that the diodes $D_3$ and $D_4$ are in the reverse cut-off state, which can cut off the fault current path, so as to achieve the purpose of clearing the fault current.

Regardless of the direction of the bridge arm current, the diode that is forcibly turned off will hinder the fault current. The switching device will not withstand the impulse voltage, which ensures the safety of the power device and improves the reliability of the fault current clearing.

5. Simulation Results

For the purpose of verifying the effectiveness of CHBFBSM's voltage self-balancing ability and the ability to clear DC faults, an 11-level MMC DC transmission system was built using the MATLAB/Simulink simulation platform as shown in Figure 8. The simulation model is shown in the Appendix A. The most serious bipolar short circuit fault among DC fault is studied. Specific electrical parameters are shown in Table 3.

![Figure 8. Simulation model structure diagram.](image)

Table 3. Simulation system parameters.

| Parameter                        | Value      |
|----------------------------------|------------|
| Number of bridge arm sub-modules | 5          |
| Sub-module capacitance value     | 5 mF       |
| Bridge arm inductance            | 10 mH      |
| Bridge arm resistance            | 0.02 Ω     |
| Sub-module capacitor voltage     | 1 kV       |
| DC side rated voltage            | 10 kV      |
| DC side line load                | 2 Ω + 5 mH |
| System rated capacity            | 12 MVA     |
| AC side rated line voltage       | 8.66 kV    |
| Inductance value                 | 3 mH       |
5.1. DC Blocking Capability Verification

In this paper, a bipolar short circuit fault occurs at 1 s. Figure 9 shows the working status of all switch tubes. The on–off conditions of all switching tubes are consistent with the theoretical analysis. Among them, the on–off conditions of $T_1$ and $T_2$ are opposite. After about 2 ms, all IGBTs are blocked.

Figure 9. Switch tubes conduction situation.

Figure 10 shows the waveform after the fault. Figure 10a shows the trend of the DC side current rising after a short-circuit fault occurs. In normal operation, the steady-state current of the DC side is about 400 A, and the fault current rises to about 1000 A. In the fault detection stage, the current rises quickly, which may cause serious harm to the power devices, so it is necessary to quickly block the switching devices. After about 2 ms, the fault current quickly drops to 0 after flowing through the capacitor with all IGBTs blocked. Figure 10b shows that the DC side voltage is about 10 kV during normal operation, and it drops to 0 after a fault occurs, so the sub-module has the fault current clearing capability.

Figure 10c shows that the AC side current is about 750 A during normal operation. When a fault occurs, energy will flow from the AC side to the DC side. The sum of the three-phase current is 0, so the feed energy on the AC side has little effect. After that, the AC side current drops to zero. The sub-module blocking will provide back electromotive force, which hinders the energy supply from the AC side to the DC side and plays a role in isolating the AC and DC. Figure 10d shows that the AC side voltage does not change much because the lockout was performed in time.

Figure 11 shows waveform of the bridge arm current. The current value of the bridge arm and the AC voltage at the moment of blocking affect the length of the decay time. After the fault occurs, the reverse voltage of the capacitor causes the diode to no longer have freewheeling capability, and the bridge arm current quickly drops to zero.
... capacitor causes the diode to no longer have freewheeling capability, and the bridge arm current quickly drops to zero.

**Figure 10.** Bipolar fault waveform on the DC side: (a) DC current; (b) DC voltage; (c) AC current; (d) AC voltage.

**Figure 11.** Bridge arm current waveform.
5.2. Capacitor Voltage Balance Ability Verification

According to the experimental conditions given in Table 2, the variation of the sub-module capacitor voltage is simulated and the voltage fluctuation is shown in Figure 12.

![Waveform diagram of sub-module capacitor voltage](image1)

**Figure 12.** $C_1 = C_2$, capacitor voltage of sub-module: (a) Waveform diagram of sub-module capacitor voltage; (b) Magnified diagram of capacitor voltage waveform after failure.

Figure 12a shows that the sub-module capacitor voltage fluctuates in the same trend during normal operation. The voltage fluctuation range between sub-modules is less than 5%. The capacitor voltage fluctuation of single sub-module is about 6%. The small fluctuation index proves that the capacitor voltage has a good balance effect. Therefore, only a single capacitor of the sub-module can be monitored, which automatically balances the capacitor voltage. Therefore, it can effectively reduce the use of measuring devices. The capacitor voltage also drops sharply since the fault occurs. Figure 12b shows the magnified diagram of capacitor voltage waveform after failure. Due to the voltage equalization characteristic, the capacitor voltage of the sub-module keeps falling synchronously when a fault occurs. After the switch tubes are blocked, the capacitor voltage is simultaneously charged to near the rated value. The fluctuation range of capacitor voltage is less than 2%.

The above analysis is based on the situation that the two capacitor values are equal, but the film capacitor has a tolerance within ±5%. When taking the maximum difference, $C_1$ is 4.75 mF and $C_2$ is 5.25 mF. The waveform of each sub module capacitor voltage is shown in Figure 13.
fluctuation index proves that the capacitor voltage has a good...voltage balance capability, which is conducive to the rapid restart of the MMC.

In summary, this sub-module has a good voltage balance capability, which is conducive to the rapid restart of the MMC.

It can be seen from Figure 13a that the fluctuation range between sub-modules is still less than 5%. The capacitor voltage fluctuation of single sub-module is about 7%. It can be seen from Figure 13b that after the IGBT is locked, the capacitor voltage can be stabilized at about 1.02 kV. The maximum unevenness of sub-modules is about 4%. Even if the capacitance values are not equal, the sub-modules are still in a voltage equalization state. In summary, this sub-module has a good voltage balance capability, which is conducive to the rapid restart of the MMC.

5.3. Investment Cost Analysis

The rated withstand voltage level of various power switching devices and the amount of the device determine the investment cost of the sub-module. In this paper, it is assumed that the rated voltages of all power devices in various topologies are the same. At this time, the models of IGBT and diode are the same, and the cost of different sub-modules is mainly reflected in the amount of devices. The specific investment cost is shown in Table 4.

Table 4. Comparison of investment costs.

| Sub-Module Topology | Number of Capacitors | Number of Sub-Modules | Number of IGBTs | Number of Diodes | DC Fault Clearing Capability |
|---------------------|----------------------|-----------------------|-----------------|-----------------|-----------------------------|
| HBSM                | N                    | 2N                    | 4N              | 4N              | No                          |
| FBSM                | N                    | 2N                    | 8N              | 8N              | Yes                         |
| CD6M                | N                    | N                     | 5N              | 7N              | Yes                         |
| SBSM                | N                    | 2N                    | 6N              | 8N              | Yes                         |
| CHBFBFSM            | N                    | N                     | 5N              | 6N              | Yes                         |
Table 4 shows that HBSM uses the fewest devices, but it is unable to clear DC faults. The number of IGBTs used in CHBFBSM is the same as that of CDASM, but less than FBSM and SBSM. However, the number of diodes used in CHBFBSM is smaller, and the required measurement device is only half of the remaining topologies. Therefore, CHBFBSM has the lowest investment cost and the highest economy.

6. Conclusions

This paper proposes a sub-module topology with DC fault clearing capability and internal capacitance self-balancing capability. This topology achieves multi-level output and DC fault blocking by combining HBSM and FBSM, using clamp circuits and switched capacitors. Moreover, no additional voltage balance control is required to automatically achieve the balance of the sub-module capacitor voltage. In addition, the number of measuring devices used can be reduced and the utilization rate of the device can be improved. Therefore, it has low investment cost and high economy. The simulation results show that the proposed sub-module can clear the fault current and realize the self-balance of the capacitor voltage. This sub-module increases the reliability of the system and eases the problem of heavy data collection pressure.

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Appendix A

Figure A1. Simulation model of the MMC DC transmission system.
Figure A2. Simulation model of CHBFBSM.

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