Impact of strained channel on electrical properties of Junctionless Double Gate MOSFET

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Abstract. Application of strained channel in Metal-oxide-semiconductor Field Effect Transistors (MOSFET) technology influences the electrical properties due to the significant changes in the energy band structure of silicon lattices. Thus, in this paper, a comprehensive analysis is conducted to investigate the impact of strained channel towards several electrical properties of junctionless double-gate MOSFET. The comparative analysis is carried out by simulating two different sets of device structure which are JLDGM device (without strain) and junctionless double-gate strained MOSFET (JLDGSM) device. The results show that the strained channel has improved the on-state current (I_{ON}), on-off ratio, transconductance (g_m) and transconductance generation factor (TGF) by approximately 58%, 98%, 98%, and 44% respectively. The significant improvement is mainly attributed to the presence of biaxial strain boosting the electron mobility in the channel. The intrinsic gate delay (τ_{int}) has significantly reduced by approximately 52% as the strained channel is applied. Since the variation of intrinsic gate capacitances (C_{int}) is very minimal (4%) as the strained channel is applied, the gate delay is dominantly governed by the drain current. However, the application of strain channel has increased the dynamic power dissipation (P_{dyn}) for approximately 19% mainly due to slightly increased intrinsic gate capacitances.

1. Introduction

MOSFET scaling has been the primary factor of rapid improvement in the integrated circuit (IC) industry over the past decades. Continuous improvement in MOSFET’s properties has been observed over the years in accordance with an aggressive scaling of the physical gate length (L_g) and the gate oxide thickness. One of the significant approaches to keep pace with Moore’s law prediction is to introduce the strained silicon (Si) in MOSFET channel. The strained channel has been proven to improve the MOSFET performance by a tremendous increase in electron mobility due to the alteration of the energy band structure [1,2]. Hence, the strained-Si technology can be regarded as an alternative solution for ultra-small scaled devices in achieving tolerable electrical properties. Ultra-thin body double-gate MOSFETs are non-conventional structures that exhibit excellent channel control and low leakage current compared to bulk planar MOSFETs. Thus, they can be regarded as the most promising device structure for realizing the continuity of MOSFET scaling. Furthermore, strain engineering can be conveniently applied to the non-conventional structures and is therefore compatible with the future and emerging MOSFET structures [3,4]. Hence, strain engineering is anticipated to be one of the types of
performance booster for complementary metal-oxide-semiconductor field effect transistors (CMOS) at ultra-scaled nanometer regime. The impact of strain towards transport properties in semiconductors has been thoroughly studied over half a century. It was first discovered in the year 1956 that the stress in silicon lattice might contribute a significant impact on the channel mobility [5]. Multiple reports have shown that the changes in electron mobility are caused by stress-induced energy shifts, depending on the applied level of stress [6–11]. The most common approaches to form strained Si which have been widely applied by chip manufacturers are uniaxial strain and biaxial strain. A uniaxial strain is a process-induced strain which the Si lattice is strained in one direction [12]. Meanwhile, the biaxial strain is a substrate-induced which makes the Si lattice strained in both x and y direction [13]. Technology Computer-Aided Design (TCAD) tools are indispensable for further investigation, development and optimization of future transistors and integrated circuits [14–16]. Therefore, TCAD tools are very crucial for predicting the multiple electrical properties of the silicon layer on multiple stress conditions. Advanced transport models are required to describe drain current (I_{ds}) improvement in the channel, including carrier quantization and carrier scattering mechanism. Although strain engineering is a mature technology to boost CMOS performance, it is still required to be studied, especially for non-planar MOSFET structures like Junctionless Double-gate MOSFET [17]. The impact of strained channel upon the electrical properties of Junctionless Double-gate MOSFET can be investigated via industrial-based software, Silvaco TCAD tools. Hence, this paper presents a comparative analysis of the impact of strained channel towards on-current (I_{ON}), off-current (I_{OFF}), on-off ratio, subthreshold swing (SS) and transconductance (g_m) of the JLDGM device. The organization of this work is conducted as follows: Section 2 describes the JLDGM device structure and simulation. Section 3 discusses the comparative analysis of the strain impact between JLDGM and JLDGSM in term of I_{ON}, I_{OFF}, on-off ratio, SS and g_m properties. Finally, the conclusions and future work are briefly summarized in section 4.

2. Schematic layout and device simulation

The schematic layout of the n-type JLDGSM is depicted in Figure 1. The silicon-germanium (SiGe) material (Ge<20%) is used as the initial substrate for the device. Strained silicon is formed by depositing Si layer at both the top and bottom part of the main substrate (SiGe). The Si layer becomes tensile stretched due to continuous attempt to align with SiGe atoms. The gate length (L_g) is scaled at 6 nm in accordance with ITRS 2013 prediction for future high performance (HP) logic technology requirements [18]. Titanium dioxide (TiO_2) is utilized as the gate insulator that isolates the gate region from source/drain regions as well as the conductive channel linking the source and drain region during the on-state condition. The application of TiO_2 as the gate dielectric allows much thicker insulator to be used, thereby mitigates the gate leakage, dopant penetration, depletion, defects and degradation [19,20].

![Figure 1. Schematic Layout for Junctionless Double-gate MOSFET device (a) n-type JLDGSM (with strain) (b) n-type JLDGM (without strain)](image-url)
One of the important criteria in designing the junctionless transistor is to ensure that both the channel and source/drain (S/D) region are doped with the identical type of dopant. In this case, the S/D region of the device is doped with \(1 \times 10^{13} \text{ cm}^{-3}\) of Arsenic dose (n-type), thereby forming the N N+ N configuration. Both device structures are reflected for complete 2-D structures as depicted in Figure 2. The design parameters used in the simulation for both types of device are tabulated in Table 1.

![Figure 2. 2-D Structure of Junctionless Double-gate MOSFET device (a) n-type JLDGSM (with strain) (b) n-type JLDGM device (without strain)](image)

| Design Parameters | Units | Value |
|-------------------|-------|-------|
| SiGe Thickness, \( T_{\text{SiGe}} \) | nm | 8 |
| Si Thickness, \( T_{\text{Si}} \) | nm | 1 |
| Body Thickness, \( T_{\text{Body}} \) | nm | 10 |
| TiO\(_2\) Thickness, \( T_{\text{TiO2}} \) | nm | 3 |
| Gate Length, \( L_g \) | nm | 6 |
| Channel doping, \( N_{\text{ch}} \) | cm\(^{-3}\) | 1.0E17 |
| S/D doping, \( N_{\text{sd}} \) | cm\(^{-3}\) | 1.0E13 |
| Metal work-function, \( WF \) | eV | 4.6 |

The investigated electrical characteristics of both n-JLDGSM and n-JLDGM are simulated via ATLAS Silvaco module. The device simulation includes all the aforementioned physical and mobility model in the previous section. Using Tonyplot feature, the \(I_{\text{ds}}-V_{\text{gs}}\) transfer characteristics can be clearly plotted in the graphical form. Thus, important device properties such as on-state current \(I_{\text{ON}}\), on-off ratio, transconductance \(g_m\), transconductance generation factor (TGF), intrinsic gate capacitances \(C_{\text{int}}\), intrinsic gate delay \(\tau_{\text{int}}\) and dynamic power dissipation \(P_{\text{dyn}}\) can be extracted and computed based on the generated \(I_{\text{ds}}-V_{\text{gs}}\) transfer characteristics.

3. Impact of the strained channel on the electrical properties of junctionless device

The impact of the strained channel on the electrical properties of Junctionless Double Gate MOSFET is extensively studied via 2-D Atlas simulation. This study would contribute a significant insight into the variation of the \(I_{\text{ON}}, I_{\text{OFF}}, \text{on-off ratio}, \text{SS}\) and \(g_m\) of the device due to the employment of the strained channel. Figure 3 depicts the merged transfer curve of \(I_{\text{ds}}-V_{\text{gs}}\) in linear and log scale at constant \(V_{\text{ds}} = 0.5\)
V for both n-type JLDGSM and n-type JLDGM device. For the purpose of comparative analysis, the $V_{TH}$ for both n-type JLDGSM and JLDGM device is fixed at 0.2 V in which the $I_{ds}$ is dramatically increased when the $V_{gs}$ is greater than $V_{TH}$. The extracted maximum $I_{ds}$ or on-state current ($I_{ON}$) for n-type JLDGSM and JLDGM device are 1951.3 µA/µm and 824.6 µA/µm respectively. It is found that the $I_{ON}$ can be tremendously boosted by approximately 58% as the strained channel is applied to the junctionless double-gate MOSFET. The significant improvement in the saturation current is mainly attributed to the presence of the SiGe layer which significantly improves the electron mobility in the tensile stretched silicon layer. As the thin silicon layer is grown at the top and bottom of a SiGe substrate, the channel would become tensely strain as a result of the lattice mismatch between Si and SiGe layer. The impact of strain on $I_{ON}$ improvement in the device is also in agreement with reports carried out by [21–24], in which the influence of interface states charge on electron transport has been significantly alleviated. Figure 4 depicts the bar graph indicating the level of on-off ratio for both devices. The on-off ratio for n-type JLDGSM and JLDGM device are measured at $2.5 \times 10^5$ and $0.04 \times 10^5$ accordingly. The application of strain engineering in junctionless double-gate MOSFET has significantly improved the on-off ratio for approximately 98%. Thus, it can be concluded that the presence of strain channel in the device has contributed a much larger on-off ratio, implying its reduced power consumption suitable for low power applications. Increasing the concentration of channel doping increases the threshold voltage ($V_{TH}$) but decreases the $I_{ds}$ and the $g_m$ of n-type devices. It is also important to observe the effect of strain silicon on the magnitude of transconductance ($g_m$) of the junctionless double-gate device. The $g_m$ is used to indicate the amount of $V_{gs}$ needed to boost the $I_{ds}$ of a MOSFET. The higher the $g_m$ is, the better the analog performance of the device will be. The magnitude of $g_m$ can be calculated as:

\[
g_m = \frac{\partial I_{ds}}{\partial V_{gs}}
\]

Apart from that, the transconductance generation factor (TGF) is also an important characteristic to measure the effectiveness of the $I_{ds}$ in getting a higher magnitude of $g_m$. Higher TGF would imply that the device is very suitable for amplifier designs. The TGF of a MOSFET can be measured as:

\[
TGF = \frac{g_m}{I_{ds}}
\]
Figure 4. Bar Graph of On-off ratio for n-type JLDGSM (with strain) and JLDGM (without strain)

Figure 5 shows the merged plot of the $TGF$ and $g_m$ as a function of $V_{gs}$ at a constant $V_{ds} = 0.5$ V for both n-type JLDGSM and JLDGM device. The plot shows that the $g_m$ extracted at a maximum $V_{gs}=1$V for n-type JLDGSM and JLDGM device are 3.56 mS/µm and 0.08 mS/µm correspondingly. The $g_m$ is tremendously increased by approximately 98% as the strain engineering is applied to the junctionless configuration of the double-gate MOSFET. The effect of stress is definitely significant with the presence of strain region that consequently results in much higher channel volume. The $g_m$, in this case, increases more than 3 times as the strain effect in the channel is considered. Evident of the improved magnitude of $g_m$ in strain channel is in agreement with the results presented by [25,26]. In term of $TGF$, the n-type JLDGSM (with strain) demonstrates approximately 44% higher than the n-type JLDGM (without strain). The magnitude of $TGF$ for n-type JLDGSM (with strain) and n-type JLDGM (without strain) are 128.4 V^{-1} and 72.5.5 V^{-1} respectively (note that the $TGF$ magnitude is measured during off-state condition). The ratio between $g_m$ and $I_{ds}$ is significantly prominent when it is measured at lower $V_{gs}$ (weak inversion regime). When the $V_{gs}$ is shifted to higher positive magnitude, the $TGF$ begins to degrade as increased $I_{ds}$ approaching the super-threshold region. For a transistor with higher $TGF$ is considered to be highly efficient when it operates at low supply voltage.

The variation in magnitude of $C_{gs}$ and $C_{gd}$ depends on the intrinsic capacitance model and the device geometry. Both $C_{gs}$ and $C_{gd}$ should be carefully considered in order to provide good accuracy of the RF model, especially over multiple bias regions. Figure 6 shows the plot of intrinsic capacitances as a function of $V_{gs}$ at a constant $V_{ds} = 0.5V$ for both devices. It is shown that the magnitude of $C_{int}$ for n-type JLDGSM and JLDGM device at maximum $V_{gs}$ are 3.15 fF/µm and 3.28 fF/µm respectively. A slight improvement of approximately 4% in $C_{int}$ magnitude is observed as the strained channel is applied to the junctionless device. At low frequencies, this intrinsic capacitances can be neglected, but not at high frequencies. Thus, the magnitude of $C_{int}$ should be minimized as low as possible in order to avoid parasitic coupling that might cause the crosstalk interferences in amplifier circuits. In saturation mode ($V_{gs} > V_{TH}$), the variation of $C_{int}$ becoming more prominent as the gate bias is increased towards its maximum magnitude. Normally, the magnitude of $C_{int}$ would keep rising as a higher potential is fed to the gate terminal. During saturation mode, any changes in $V_{ds}$ will not contribute significant changes in $C_{int}$ magnitude due to pinch-off event that causes the $I_{ds}$ saturates constantly. An extremely high intrinsic capacitance should be avoided because it could significantly delay the rise of $I_{ds}$ over the gate bias. The magnitude of $C_{int}$ is then used to determine the intrinsic gate delay ($\tau_{int}$) for both devices. The magnitude of intrinsic gate delay is relatively depended on the magnitude of $I_{ds}$ and $C_{int}$ which is denoted as:

$$\tau_{int} = \frac{C_{int} \times V_{DD}}{I_{ds}}$$

(3)
where $V_{DD}$ is the supplied drain voltage which is varied from 0V to 1V. To extract the intrinsic gate delay ($\tau_{\text{int}}$) for both transistors, the transfer characteristic is plotted as a function of drain-to-source voltage ($V_{ds}$). Figure 7 depicts the plot of $\tau_{\text{int}}$ - $V_{ds}$ transfer characteristic in which the $V_{gs}$ is set as a constant magnitude of 1V. The intrinsic gate delay of n-type JLDGSM (with strain) and n-type JLDGM (without strain) are measured at 1 ps and 2.1 ps respectively. It is observed the intrinsic gate delay of n-type JLDGSM device is approximately 52% lower than the n-type JLDGM device. The results imply that the strain channel has significantly reduced the time taken by the gate to induce the drain current after being supplied with a certain input voltage. The results also in agreement with the results reported by [27] in which the quantum incorporation of strain did reduce the intrinsic gate delay. The intrinsic gate delay for both devices is significantly influenced by the drain current. Since the drain current is inversely proportional with the delay, a large amount of drain current would greatly reduce the gate delay. The intrinsic gate capacitances, however, does not affect much on the gate delay due to marginally different magnitudes between both devices.

Dynamic power dissipation ($P_{\text{dyn}}$) is an important figure of merit to measure the reliability of a transistor. The impact of extremely high power dissipation would lead to a continuous rise in temperature of the microchips. As the temperature rises over time, off-state current or so-called leakage current would increases drastically that might cause the malfunction of the device. Normally, during switching transition between ‘ON’ and ‘OFF’ state or vice versa, the drain current is required for the process of charging and discharging the intrinsic capacitive load. The $P_{\text{dyn}}$ of a transistor can be measured by the following equation:

$$P_{\text{dyn}} = C_{\text{int}} V_{DD}^2 f$$

where $f$ is the operating frequency of the device and $V_{DD}$ is the supplied drain voltage. Figure 8 shows the plot of $P_{\text{dyn}}$ as a function of $V_{ds}$ at a constant $V_{gs}$ of 0.5V for both devices. The $P_{\text{dyn}}$ at $f = 1$ MHz and
V_{ds} = 1V for n-type JLDGSM (with strain) and n-type JLDGM (without strain) are measured at 2.1 nW/µm and 1.7 nW/µm respectively. There is a slight increase of approximately 19% in $P_{dyn}$ as the strain channel is applied to junctionless double-gate MOSFET. A slight increase in $P_{dyn}$ for n-type JLDGSM (with strain) is relationally due to slightly higher intrinsic capacitances, as shown in Figure 6. Reducing the operational frequency ($f$) is the most visible approach to minimize the dissipated power, but it could significantly affect the device performance. Another optional method is to reduce the intrinsic capacitances which require advanced channel engineering and system design. Thus, it can be concluded that the presence of strain channel did contribute a significant impact on most of the electrostatic and analog properties of the junctionless double-gate MOSFET. The incorporation of SiGe substrate with ultrathin silicon layers has changed the mechanical properties in the channel which tremendously stimulate the mobility enhancement due to substrate-induced strain.

4. Conclusion
The impact of strain channel on the electrical properties of the junctionless double-gate MOSFET have been studied via Silvaco TCAD tools technology in which the physical mechanisms such as substrate-induced mobility models are considered. The strain effect on the device properties such as on-state current, on-off ratio, transconductance, transconductance generation factor, intrinsic capacitance, intrinsic gate delay and dynamic power dissipation have been investigated. The simulation results show that the application of strain engineering has significantly improved the channel mobility, subsequently enhancing the on-state current, on-off ratio and transconductance. The strained device has also shown a significant reduction in intrinsic gate delay as the SiGe substrate is sandwiched with two ultrathin silicon layers. Since the strain channel has less impact on intrinsic capacitances, its impact on dynamic power consumption seems to be very marginal.

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