Design of a broadband high-efficiency Doherty power amplifier for 5G communication systems

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Abstract In this paper, a novel load modulation network structure is proposed by connecting a shunt $\lambda/2$ micro-strip line at the combiner of traditional DPA. A broadband high-efficiency Doherty power amplifier (DPA) is designed and fabricated for 5G mobile communication. Measurement results show that the saturated output power of the DPA is above 43 dBm in the range of 3.1 to 3.7 GHz, and the saturated drain efficiency is between 65% and 73.1%. Additionally, drain efficiency of the 8 dB power back-off is above 40%. And better than $-45.6$ dBc adjacent leak power ratio (ACLR) can be achieved with Digital Pre-Distortion (DPD) under 10 MHz LTE signal testing at 3.3 GHz.

Keywords: Doherty power amplifier, high efficiency, broadband, load modulation network

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

With the development of 5G wireless communication technology, there has been increasing demands for communication speed and capacity, which largely depend on the improvement in the bandwidth, efficiency, and linearity of power amplifiers (PAs) [1, 2, 3, 4, 5, 6]. To address these significant issues, Doherty power amplifier (DPA) has been widely used due to its high back-off efficiency, good linearity and simple structure in communication systems [7, 8, 9, 10, 11, 12]. However, designing wideband DPAs is still a challenge. One of the main factors is the load modulation network that largely limits the bandwidth of the DPA [13, 14, 15, 16]. According to the classical transmission line theory, there is a frequency dispersion effect on the $\lambda/4$ micro-strip line in the load modulation network [17, 18, 19, 20]. When the DPA operating frequency is shifted by the center frequency, the output impedance of the carrier PA becomes smaller. This phenomenon seriously affects the drain efficiency of DPA and limits the operating bandwidth of DPA. Therefore, many methods have presented to optimize the load modulation network for designing broadband and high efficiency DPAs [21, 22, 23, 24]. In [21], a new load modulation network is proposed to alleviate the degradation of efficiency by adjusting the transmission line characteristic impedances in the load modulation network. A 65% efficiency and 42 dBm output power is implemented by using a new output combining network and adopting more realizable elements than the standard DPA [22]. In [23], an x-type high-pass impedance transformer based on lumped components is used to modulate the load impedance for designing DPA. A DPA with 61%–71% of saturated drain efficiency and over 43 dBm of output power is proposed by optimizing its load modulation network [24].

In this paper, a novel load modulation network structure is proposed, which connects a shunt $\lambda/2$ micro-strip line at the combiner of traditional DPA. This network has less frequency dispersion and then the operating bandwidth of the DPA is improved. The theory behind it is analyzed in detail in this paper. Then a broadband high efficiency DPA is designed and fabricated to verify the validity of the proposed structure.

2. Theoretical analysis

Traditional DPA load modulation network is shown in Fig. 1(a), which consists of two $\lambda/4$ micro-strip lines with different characteristic impedances [25, 26]. The output impedance $Z_c$ of carrier PA at the power back-off is usually $2Z_0$, where $Z_0$ is the optimal impedance [27]. However, the $\lambda/4$ micro-strip line in the load modulation network has the frequency dispersion effect. The output impedance $Z_c$ of the carrier PA changes within the operating frequency. As a result, the $\lambda/4$ line could not transform the impedance of combiner $Z_{com}$ to the output impedance $Z_c$ of carrier PA precisely in a wideband frequency range. Therefore, the

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drain efficiency at power back-off of DPA decreases due to the bandwidth limitation of the $\lambda/4$ line.

As shown in the Fig. 1(a), the impedance of conventional combiner $Z_{\text{Com}}$ at the power back-off point can be expressed as

$$Z_{\text{Com}} = \frac{Z_0 + jZ_L \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)}{Z_L + jZ_0 \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)} \quad (1)$$

The output impedance $Z_C$ of carrier PA can be calculated as

$$Z_C = Z_T + jZ_T \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)$$
$$Z_L + jZ_{\text{Com}} \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)$$

Where $\tilde{f} = \Delta f/f_0$ is the normalized frequency.

According to Eq. (1) and (2), the real part of $Z_C$ can be given by:

$$\text{Re}[Z_C] = Z_0 + Z_T^2 Z_L^2 + 2Z_T Z_L B^2 + Z_T^2 Z_L^4$$
$$Z_T^2 Z_L^4 + AB^2 + Z_T^4 B^4$$

Where, $A = (Z_T + Z_L)^2 Z_0^2 - 2Z_T Z_L$ and $B = \tan(\tilde{f} \cdot \frac{\pi}{2})$.

According to Eq. (1), (2) and (3), the output impedance $Z_C$ of the carrier PA can reach its optimal value ($2Z_0$) only when the DPA operates at the center frequency. The output impedance $Z_C$ of the carrier PA decreases due to the operating frequency shifting from the center frequency. It causes the drain efficiency dropping at power back-off for a bandwidth design.

To address the frequency dispersion issue, a novel load modulation network structure is proposed as shown in Fig. 1(b). Compared with traditional structures, a shunt $\lambda/2$ micro-strip line is connected at the combining point. As shown in the Fig. 1(b), the impedance $Z_{H1}$ and $Z_{H2}$ can be calculated as

$$Z_{H1} = Z_L + jZ_0 \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right) \quad (4)$$

$$Z_{H2} = Z_S + Z_{\text{open}} + jZ_0 \tan(\tilde{f} \cdot \pi)$$
$$Z_L + jZ_{\text{Com}} \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)$$

Where, $Z_{\text{open}}$ represents the output impedance of the peak PA at the power back-off.

Then impedance $Z'_{\text{Com}}$ of combiner is expressed as

$$Y'_{\text{Com}} = \frac{1}{Z_{H1}} + \frac{1}{Z_{H2}}, \quad Z'_{\text{Com}} = 1/Y'_{\text{Com}} \quad (6)$$

The output impedance $Z_{CN}$ of carrier PA can be derived as

$$Z_{CN} = Z_T + jZ_T \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)$$
$$Z_T + jZ_{\text{Com}} \tan\left(\tilde{f} \cdot \frac{\pi}{2}\right)$$

At the power back-off stage, only the carrier PA is operated. According to Eq. (1)–(7), the real and imaginary parts of the impedances $Z_C$ and $Z_{CN}$ can be extracted individually. Fig. 2 shows the comparison of the carrier PA’s output impedance frequency response between the proposed and conventional networks at the power back-off point. The output impedance of conventional carrier PA at power back-off point is highly frequency-dependent, and therefore the bandwidth of the DPA is limited. The proposed load modulation network can provide relatively stable output impedances for carrier PA in a wide frequency range. Therefore, the proposed load modulation network in this paper is more suitable for a wideband DPA design.

3. Design, simulation and measurement results

For validation, a broadband high efficiency DPA is design using the Cree’s CGH40010F transistor based on the Rogers4350B substrate ($\varepsilon_r = 3.66$, $H = 30\,\text{mil}$). The carrier PA is biased at Class AB, with gate and drain voltages at $-2.7\,\text{V}$ and $28\,\text{V}$. The gate bias voltage of the peaking PA is set to $-5.5\,\text{V}$ and the drain supply voltage is set to $30\,\text{V}$, corresponding to the Class C. Asymmetric structure is adopted for increasing the range of power back-off. The completed circuit of the DPA is shown in Fig. 3. And the photograph of the fabricated DPA is shown in Fig. 4.

The simulated and measured results of the proposed broadband DPA and conventional DPA are shown in Fig. 5 and Fig. 6. The measurement results agree well with simulations. The DPA performances under continuous wave (CW) driven in terms of output powers, gains and saturated drain efficiency are shown in Fig. 5. Drain efficiency is above 65% from 3.1 to 3.7 GHz, and the maximum drain efficiency is up to 73.10% at 3.6 GHz. A minimum output power of 43 dBm is obtained, while the maximum power reaches 44.65 dBm at 3.2 GHz.
In the same frequency band, the simulated and measured results of output power, gain and drain efficiency at 8 dB power back-off are shown in Fig. 6. Measured drain efficiency is above 40.3% within the 3.1 to 3.7 GHz frequency band, and the gain is above 9 dB. Compared with the conventional DPA, the proposed DPA is superior in power and saturated, power back-off drain efficiency according to Fig. 5 and Fig. 6.

Fig. 7 shows the proposed and conventional DPA measured drain efficiency versus output powers at different frequencies. It should be noted that the traditional DPA and the new DPA have different output power and drain efficiency even at the center frequency of 3.4 GHz shown in Figs. 5, 6 and 7. This is because the $\lambda/2$ open micro-strip line connected at the combiner which makes the impedance of the auxiliary power amplifier closer to infinity. Therefore, the power of the main power amplifier is not easily leaked to the auxiliary power amplifier branches compared with the traditional DPA. So, the overall output power and drain efficiency of the new DPA can be improved compared with traditional DPA. The DPA has a gain compression phenomenon when DPA approaches saturation status, which seriously affects the linearity of DPA. Therefore, DPD (Digital Pre-Distortion) technology is applied to correct the adjacent channel leakage ratio (ACLR) of DPA. An LTE modulation signal with a bandwidth of 20 MHz and a peak-to-average power ratio (PAPR) of 7.5 dB is used for testing. The measured results are shown in Fig. 8, in which ACLR is $-23.4$ dBc without DPD and $-45.6$ dBc with DPD for the proposed DPA. The ACLR is $-20.21$ dBc without DPD and $-47.2$ dBc with DPD for the conventional DPA.

Performance comparison has been made between the proposed DPA and previously reported at similar frequency
43 dBm and saturated drain measurement results show a saturated output power above 43 dBm. The DPA is implemented for validating the proposed structure. Measurement results show a saturated output power above 43 dBm and saturated drain efficiency between 65%–73.1% from 3.1 to 3.7 GHz. At 8 dB power back-off, the drain efficiency is above 40%. And the ACLR is better than –45.6 dBc with DPD, which makes it suitable for 5G base station applications.

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