A Circuital Model of Switching Behaviour of 4H-SiC $p^+\text{-}n\text{-}n^+$ Diodes Valid at any Current and Temperature

S Bellone\textsuperscript{1}, F Della Corte\textsuperscript{2}, L Di Benedetto\textsuperscript{1} and G D Licciardo\textsuperscript{1}

\textsuperscript{1}University of Salerno, D. I. In.,
Via Giovanni Paolo II, 132, Fisciano Salerno, IT
\textsuperscript{2}Mediterranea University of Reggio Calabria, D.I.M.E.T.,
Via Graziella Feo di Vito, Reggio Calabria, IT

E-mail: sbellone@unisa.it

Abstract. A circuital model of 4H-SiC $p^+\text{-}n\text{-}n^+$ diodes is presented, which is able to describe the switching behaviour of the devices in a wide range of current, voltage and temperature, at an arbitrary instant, with comparable accuracy of numerical simulations. The model has been analytically derived under generic conditions and is capable to calculate also the dynamic spatial distribution of minority carriers in the epitaxial layer. The accuracy of the model is shown by comparison with numerical simulations and experimental measurements.

1. Introduction
Contrarily to unipolar devices in Silicon Carbide, which are already commercially available [1], bipolar devices are still under investigation because of the stronger sensitivity of their electrical behaviour to material properties [2,3] and fabrication process [4,5]. In this context, the temperature effects on the electrical behaviour of bipolar devices has not been sufficiently modelled so far, although a number of relevant dependencies have been observed. In the present paper, starting from previous works of the authors [6,7], where the combined effects of the apparent bandgap narrowing and incomplete ionization of doping on the steady-state behaviour of 4H-SiC $p\text{-}i\text{-}n$ diodes have been modelled, a circuital model of the devices is presented, which is able to describe their switching behaviour in a wide range of current, voltage and temperature. Although numerical simulation tools have reached an impressive degree of complexity in exploring the electrical characteristics of devices, physics-based models continue to assume an important role for a meaningful interpretations of the experimental behavior of devices and the development of compact models for circuit simulation programs. Currently, a large part of analytical models used for the static description of SiC diodes [8-10] are based on the Herlet’s model [11], which was originally proposed for very high current operation of silicon $p\text{-}i\text{-}n$ diodes, while the dynamic models are based on charge control equations [12]; both leave a large space in the literature to propose models capable of describing the characteristics of SiC diodes from the lowest to the highest injection regimes at different temperatures. The proposed model is also capable to calculate the dynamic spatial distribution of minority carriers in the base of diodes with an accuracy comparable to numerical simulations, avoiding any fitting parameters, which extends the model validity to wider domains if compared to compact models, and makes it a useful instrument for the study of bipolar devices in 4H-SiC and their applications.
2. Circuital Model
The proposed circuital model is schematized in figure 1. The $S_W$ switch positions, $S$ and $D$, select the static or dynamic behaviour of the diode. All the circuital components in figure 1 are determined once the minority carrier distribution in the epilayer, $p(x)$, has been calculated as in [13-15] by analytically solving the semiconductor diffusion equations. For brevity the solution is not reported and the authors remand to the above references for more details. In the following, the apex ‘0’ will denote static values of time-varying electrical quantities.

![Figure 1. Circuit schematic of the model.](image)

2.1. Static model
The static model [6,7] is composed of two parallel branches. The $J_{\text{EPI}}^0$ current generator accounts for three current components:

$$J_{\text{DIF}}^0 = J_{\text{NP}}^0 + J_{\text{PN}}^0 + J_{\text{EPI}}^0$$  \hspace{1cm} (1)

The first two components of equation (1) describe the minority currents injected in the anode and cathode regions, respectively:

$$J_{\text{NP}}^0 = qS_{\text{p}}(T)p^0(0^+) \left[1 + \frac{p^0(0^+)}{N_{\text{EPI}}} \right]$$  \hspace{1cm} (2)

and

$$J_{\text{PN}}^0 = qS_{\text{n}}(T)p^0(W_{\text{EPI}}) \left[1 + \frac{p^0(W_{\text{EPI}})}{N_{\text{EPI}}} \right]$$  \hspace{1cm} (3)

where $q$ is the elementary charge, $N_{\text{EPI}}$ is the epilayer doping concentration, $S_{\text{p}}$ and $S_{\text{n}}$ are the equivalent temperature-dependent recombination velocities of the $P^+$ and $N^-$ terminal regions, respectively, and $p^0(0^+)$ and $p^0(W_{\text{EPI}})$ are the hole densities at the epilayer side of the $P^+$-$n$ and $n-n^+$ junctions, respectively. The third component of equation (1) describes the recombination current in the epilayer:

$$J_{\text{EPI}}^0 = \frac{qL_a}{\tau_a} \cosh\left[\left(\frac{W_{\text{EPI}}}{L_a}\right) - 1\right] \left[p^0(0^+) - p^0(W_{\text{EPI}})\right]$$  \hspace{1cm} (4)
expressed in terms of the temperature-dependent ambipolar lifetime $\tau_a = \tau_p + \tau_n p^0 \left( \frac{P^0 + N_{EPI}}{P^0} \right)$ and ambipolar diffusion length $L_a$. The other branch accounts for the recombination current in the space charge region, $W_{SC}$,

$$J_{SC}^0 = q \frac{W_{SC} \sqrt{N_{EPI} p^0}}{2 \tau_{SC}} \quad (5)$$

where $\tau_{SC}$ is the carrier lifetime in the space charge region (SCR) and such current density is represented by the diode symbol in figure 1, to which the Dember voltage contribution is in series:

$$V_{DIFF}^0 = V_T \ln \left[ \frac{(b+1) p^0 (0^+) + b N_{EPI}}{(b+1) p^0 (W_{EPI})^+ + b N_{EPI}} \right]^{\frac{b-1}{b+1}} \quad (6)$$

where $b = \mu_n / \mu_p$ is the electron-hole mobility ratio. The series resistance, $R_0^0$, accounts for the constant resistances of the terminal regions, including the contacts, and the injection dependence resistance of epilayer [6]. The current–voltage relation of the static model is finally given by

$$V_D^0 = V_{PN}^0 + V_{DIFF}^0 + R_0^0 \left( J_{SC}^0 + J_{DIFF}^0 \right) \quad (7)$$

where the $p^-n$ junction voltage, $V_{PN}^0$, is calculated by the well-known junction law. In figure 2 the static analytical $J_D-V_D$ curves of a 10µm-thick epilayer are compared with those from Silvaco ATLAS simulations [16] in a wide range of current and temperature values. It is interesting to note that the curves at different temperatures never intersect, which indicates that the diode series resistance presents a negative temperature coefficient [17].

![Figure 2. Steady-state $J_D-V_D$ curves of 10-µm thick diode.](image)

2.2. Dynamic model

When the switch $S_D$ in figure 1 is positioned on $D$, the switch $S_{W2}$ remains closed until the minority carrier density at the epilayer border of the $p^-n$ junction reduces to $N_{EPI}$, namely until $V_{PN} > V_{REF} = 2V_T \ln \left( N_{EPI} / n_i \right) [15]$. During this storage interval ($t < t_s$), the current-voltage characteristic of the diode is determined by the same quantities introduced above for the static model,
expressed this time in terms of the time-varying hole concentration. After the storage ($t > t_S$), $S_{W2}$ opens and the diode turn–off phase is described by the charging of the time-varying junction capacitance

$$C_j = \frac{e}{W_{SC}} \left[ 1 + \frac{p(0,t_S) e^{-\frac{t-t_S}{\tau_s}}}{N_{EPI}} \right]$$

(8)

by means of the current density determined by the difference between the total diode current and $J^*$ given by $J_p(W_{SC},t) + J_{pc}(t)$. The first term represents the hole density variation in the epilayer due to $W_{SC}$ widening, given by:

$$J_p(W_{SC},t) = qD_p \frac{p(x_{MAX}(t_S),t_S)}{x_{MAX}(t_S) - W_{SC}(t_S)} \frac{1-t_S}{\tau_{p,EQ}}$$

(9)

where $x_{MAX}$ is the epilayer abscissa where the hole density assumes its maximum value $p_{MAX}$, and $\tau_{p,EQ}$ has been calculated in [18]. The second term represents the current flowing through the substrate (3), approximated with the cathode current related to the peak value as [6]:

$$J_{pc}(t) \approx qS_p p_{MAX}(t) \left[ 1 + \frac{P_{MAX}(t)}{N_{EPI}} \right]$$

(10)

The accuracy of the dynamic model is shown in figure 3 by comparing current and voltage transients, at different temperatures, with numerical simulations of the same 10–µm thick diode of figure 2, when it is forward biased at 100Acm$^{-2}$ and then switched on a resistive load with a power supply of −20V.

The proposed model is isothermal and does not account for self-heating effects. Its validity is essentially limited by the temperature dependences of the transport parameters involved in the model, among which the mobility is particularly critical. The validity of the implemented mobility model [6] has been experimentally verified for silicon carbide in [19] up to about 600K, while in [20] an electro-thermal model of a lateral SiC JFET, using the same mobility equations, has been verified up to 300°C by simulation comparisons. These results suggest that the proposed model can be successfully employed up to about 600K. In this range of temperature, the model reveals an useful instrument for the dimensioning of diodes in the design process of switching circuits, like power converters, where (4)-(6) and (8)-(10) allow one to accurately define the $p-n$ junction structure and the epilayer characteristics (thickness, doping and ambipolar carrier lifetime) to optimize the switching velocity and the dynamic power losses. Similarly for communication systems, the model can be used to calibrate the series resistance of diodes for RF power switches and attenuators to minimize the insertion losses.
In figure 4, the capability of the model to describe also the internal quantity distribution is shown by comparing the hole distribution transient with numerical simulation results, sampled at five instants of time and at three temperatures. Finally, a comparison of the model with simulations and experimental results taken on a 25 µm–thick diode are reported in figure 5 at two temperatures. The device under test is a 4H-SiC p-i-n vertical diode, whose anode contact has a circular geometry with a 350 µm diameter. The 3×10^{15} cm^{-3} doped base region is epitaxially grown on a 300 µm thick and 5×10^{19} cm^{-3} nitrogen-doped substrate. The anode region is Al implanted at a depth of 1.3µm with a peak doping of 6×10^{19} cm^{-3}. Deposition of Al/Ti and of Ni realizes the ohmic contacts for the anode and cathode regions, respectively. The switching curves are obtained by imposing a forward and reverse current densities of 60 Acm^{-2} and 115 Acm^{-2} with a HP 8114A Pulse Generator and are acquired with Tektronix DPO7254 digital oscilloscope.
**Figure 4.** Transients of hole distribution in the same switching conditions of figure 3.

**Figure 5.** Comparisons among experimental measurement, numerical simulations and model results of a 25-µm thick diode [9].
3. Conclusion
A circuit model of the static and switching behavior of 4H-SiC $p$-$i$-$n$ diodes has been proposed, which is able to describe the diode $I$-$V$ characteristics at the terminals as well as the spatial-temporal profiles of physical quantities, like hole concentration and electric field. Numerical simulations and measurements have been compared with the model to show its accuracy to describe the diode electric behavior at different temperatures. It can be conveniently used to design 4H-SiC $p$-$i$-$n$ diodes for power and RF power applications.

4. References
[1] Cree Inc. (http://www.cree.com).
[2] Bellone S Di Benedetto L 2014 A model of the $I_D$-$V_{GS}$ characteristics of normally-off 4H-SiC bipolar JFETs IEEE Trans. on Power Electron. 1 29 514 – 521
[3] Bellone S Di Benedetto Licciardo G D 2012 A Quasi One–Dimensional Model of the Potential Barrier and Carrier Density in the Channel of Si and 4H–SiC BSIT’s IEEE Trans. on Electron Devices 59 9 2546-2549
[4] Buono B Ghandi R Domeij M M Zetterling C-M Œstling M 2010 Modeling and characterization of current gain versus temperature in 4H-SiC power BJTs IEEE Trans. on Electr. Dev. 57 3 704-711
[5] Nipoti R Di Benedetto L Albonetti C Bellone S 2012 Al$^+$ Implanted Anode for 4H–SiC $p$–$i$–$n$ Diodes ECS Tans. On GaN and SiC Power Tech., 50 3 391–397.
[6] Bellone S Della Corte F G Albanese L F Pezzimenti F 2011 An analytical model of the forward $I$-$V$ characteristics of 4H-SiC $p$-$i$-$n$ diodes valid for a wide range of temperature and current IEEE Trans. on Power Electron. 26 10 2835-2843
[7] Bellone S Della Corte F G Di Benedetto L Albanese L F Licciardo G D 2010 A self–consistent model of the static and switching behavior of 4H-SiC Diodes IEEE International Semiconductor Conference
[8] Sheng K Zhang Y Yu L Su M Zhao JH 2009 High-frequency switching of SiC high-voltage LIFET IEEE Trans. Power Electron., 24 1 271–277
[9] Dyakonova NV Ivanov PA Koslov VA Levinstrin ME Palmour JW Rumyantsev SL Singh R 1999 Steady-State and transient forward current-voltage characteristics of 4 H Silicon Carbide 5.5.kV diodes at high and superhigh current densities IEEE Trans. Electron Devices, 46 11 2188–2194
[10] Abuishmais I Undeland TM 2010 Simplified models of forward conduction for SiC power pin and Schottky diodeswith temperature dependency in Proc. 5th IET Int. Conf. Power Electron., Mach. Drives 1-6.
[11] Herlet A 1968 The forward characteristic of silicon power rectifiers at high current densities Solid State Electron. 11 717–742
[12] Lauritzen PO Ma CL 1991 A simple diode model with reverse recovery IEEE Trans. on Power Electron., 6 2 188-191
[13] Bellone S Albanese L F Licciardo G D 2009 A self-consistent model of the OCVD behavior of Si and 4H-SiC $p$–$n$–$n$ diodes IEEE Trans. on Electr. Dev. 56 12 2902-2910
[14] Bellone S Albanese L F Licciardo G D 2009 Limitations of the open-circuit voltage decay technique applied to 4H-SiC diodes IEEE International Semiconductor Conference
[15] Bellone S Della Corte F G Di Benedetto L and Licciardo G D 2012 An analytical model of the switching behavior of 4H-SiC $p$+$n$–$n$+ diodes from arbitrary injection conditions IEEE Trans. on Power Electronics 27 3 1641-1652
[16] ATLAS User’s Manual 2005 SILVACO Int. Santa Clara, CA, USA, Ver.5.10R
[17] Satoh M, Nagata S, Nakamura T, Doi H and Shibagaki M 2009 Doping Level Dependence of Electrical Properties for p+n 4H-SiC Diode formed by Ion Implantation Materials Science Forum 615-617, 679-682.
[18] Bellone S, Neitzert HC and Licciardo GD 2004, Modeling and Characterization of the OCVD Response at an Arbitrary Time and Injection Level Solid State Electronics 48 7 1127-1131.

[19] Roschke M Schwierz F 2001 Electron mobility models for 4 H, 6 H, and 3 C SiC IEEE Trans. Electron Devices, 48 7 1442–1447

[20] Zhong X Wang T Guo Q Sheng K 2011 High Temperature Physical Modeling and Verification of 4H-SiC Lateral JFET Device in IEEE 2nd International Conference on Artificial Intelligence, Management Science and Electronic Commerce (AIMSEC), 4015-4018

Acknowledgments
The authors wish to thank Dr. Roberta Nipoti from CNR-IMM in Bologna, Italy, for manufacturing the 4H-SiC diodes.