DbOBS: dual buffered switch for variable optical bursts in future datacenters

Pronaya Bhattacharya1,2 · Arunendra Singh3 · Amod Kumar Tiwari4 · Vinay Kumar Pathak5 · Rajiv Srivastava6

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Abstract
Modern data-driven applications pose stringent requirements of high bandwidth, ultra-low-latency, low-powered, and scalable interconnections among switches and routers in data-centers. To address these demands, electronic switching is not a viable choice due to bandwidth and computing bottlenecks. Thus, researchers explored effective optical switch design principles for next-generation data-centers. In optical switches, data aggregates in the form of optical bursts (OB) at ultra-high speeds. In the case of OB contention, solutions are proposed by researchers to store OB as recirculating patterns in fiber delay lines (FDL) with induced optical delay. However, due to variable burst length, it is not possible to measure slot delay length, thus storage of contending bursts is not possible at intermediate core switches. Motivated from the aforementioned discussions, in this paper, we propose a switch design DbOBS, that is capable to store variable OB during contention slots. DbOBS estimates mean burst length, and possible deviation from mean length to minimize burst loss. The considered switch design is validated through parameters like-burst length estimation, over-reservation, and waiting time. For network-layer simulations, poison arrivals of data bursts are considered as packetized units. The packets are sent through Monte-Carlo arrivals and burst loss probability (BLP) is estimated at various input load conditions and buffer sizes. DbOBS achieves a BLP in order of $10^{-4}$ at load $\approx 0.8$, and buffer-size of 50, and burst length of $L = 5$, that outperforms the traditional switch designs.

Keywords Optical burst switching · Dual buffers · Optical switch · Variable burst estimation · Contention · Poisson arrivals · Future data centers

1 Introduction

In next-generation data-centers, the demand for internet traffic has exponentially increased due to the emergence of data-centric applications like Internet television, video-on-demand, and big-data enabled infrastructures. To cater to this increasing demand, modern data-centers have evolved themselves to efficiently leverage computing and hardware
resources to build massive hyper-scale components. Table 1 presents the list of abbreviations and their intended description.

However, traffic within the high-performance data-centers is aggregated at core routers and switches, which are mainly electrical in nature. These switches process information based on individual entries in the packet header, and form route decisions locally based on routing table entries. Alternatively, circuit-design patterns employ high-speed electronic switches, and efficiently manage bandwidth based on multiplexing strategies. However, electronic switches are limited by data-rate bottlenecks due to the electrical processing of signal elements that induce link-level losses through communication channels, thereby limiting the propagation rate of communication channels. This has motivated researchers to look for alternate solutions in the optical domain, that can process information as light pulses, and can propagate at high distances with low-or-negligible
channels loss Forencich et al. (2020). Also, optical channels employ low-powered components to form a highly responsive, robust, and scalable interconnection framework that supports massive interconnections in modern data centers.

Modern optical data-centers are supported through high-performance switches that connect billions of servers through efficient network topology and switching interconnections. The statistics of optical switch deployments for future data center requirements are presented in Fig. 1. By 2022, the core optical switches in modern data-centers are predicted to support \( \approx 15 \, \text{K ZB} \) internet traffic every year, with the end-user traffic close to 2.6 K ZB/year. This humongous traffic needs to be managed at a high core bandwidth of 400 peta-bytes/sec transfer rate, with round-trip time latency close to 1 nano-second Singh et al. (2020). The following is depicted in Fig. 1a. Optical data-centers need to support a wide range of diverse applications and QoS parameters, with low-power requirements of optical interconnections. It is predicted that close to 60 ZB traffic would be supported by 2025 by data centers, with less than 2kW for optical interconnections Shukla et al. (2018). A detailed discussion on traffic estimates in data-centers to meet users QoS requirements is presented in Fig. 1b.

In a similar direction, modern cloud-computing infrastructures have hyper-scaled to provide computing-as-a-service to different data-driven applications like search engine platforms, social networking, and large-scale server computing. To support these applications, the cloud-infrastructures are faced with stringent challenges of pervasive and ubiquitous computing, coupled with network orchestrations to leverage scalable, available, and resilient services. To support the agility of heterogeneous operating systems, hardware, disk, and I/O, cloud applications require high end-to-end throughput to provision the resource requirements of users at massive scales. Cloud servers also support infrastructure-as-a-service components in inter and intra data center networking, where the fixed electrical grids can be replaced through off-the-shelf optical racks and components Yin et al. (2017). Thus, optical networks can provision and support responsive cloud services through the development of scalable, high-port, and low latency interconnection switches that allows high-end throughput, and support effective load balancing at bottleneck servers. Figure 1c shows the impact of optical PDUs over electrical PDUs.

The statistics indicate that optical data passing through modern data-centers has increased significantly Shukla et al. (2019). Thus, the legacy backbone networks are deployed with FEONs to handle large volumes of data traffic from heterogeneous networked applications. FEONs allow high agility and fine-tuned granularity that orchestrates intelligent resource sharing among dense interconnections in optical data centers. However, to deploy FEONs, the switching schematics are required to support unified control plane operations through GMPLS due to simplified management of network connectivity and flexibility in control operations Jinno et al. (2009). Through GMPLS, a unified separation of control and data plane operations is possible, and it allows effective programming of routers and switches, via PXC. The network is logically partitioned into separate virtual networks, or VT, where every VT can support its own set of regulations and cloud-service policies. Thus, in data centers, effective logical peering, control, and management stacks are built, and the entire data traffic of a virtual path is abstracted from other virtual resources. The control functions are abstracted through high-level core switched networks, where the entire data from the different virtual optical networks are aggregated for bulk processing and control. Thus, through an intelligent mix of FEONs employed with GMPLS, future data-centers, and cloud services have transitioned themselves to simplified network resource handlers, that are managed as logical entities.
Future data-centers require to upgrade themselves from conventional electrical backbones towards low-latency optical backbones. Optical switching can multiplex low-bandwidth channels to form high-density fiber interconnections through DWDM. This makes the realization of around 160 Gbps transfer rate in single fiber sheath, based on appropriate tuning strategies at the receiver end. In the future, it is envisioned that TWCs would be employed for tuning input optical data to destined output ports. The delivery could be packetized, as in OPS, or could be aggregated at edge nodes through OBS.

As discussed above, to manage the large data traffic through optical data centers, optical switches are deployed in either ToR or EoR establishment consisting of servers as leaf nodes at Layer 0. The leaf nodes at Layer 0 are connected through hierarchical topologies like Clos. and Fat-Tree, which presents a three-level connection establishment Vahdat et al. (2011), Kachris and Tomkos (2012), Di Lucente et al. (2012). The details of the same are presented in Fig. 2. The client application data queries are aggregated through Layer 0 and passed to Layer 1, which consists of edge switches. The edge-switches provide low-latency for query resolutions, and if data is not present, is passed to aggregate switches. The aggregate switches are connected to core switches at Layer 2. At Layer 2, the bulk of data-traffic is presented and is forwarded to public networks. Due to high data-traffic at aggregate and core layers, in the design of next-generation data centers, the switches are replaced through optical switches to support high-bandwidth, low RTT latency, and high availability Di Lucente et al. (2012), Miao et al. (2014). The challenge lies in designing an efficient optical switch that can meet the dual requirements of low-optical power requirements, minimized average RTT delay, low physical layer cross-talk and noise signal impairments at the physical layer, and low packet loss rates at the network layer design Srivastava et al. (2009).

Several switch architectures are proposed and examined by researchers across the globe. In a similar direction, it is concluded that OCS-based 3D-MEMS switches proved to be highly scalable, with dense port-connectivity and requirements for large port expansion to hundreds of ports Basha et al. (2007). Although, 3D-MEMS OCS switches suffer from the limitations of milliseconds-scale switching operations. Owing to this, researchers investigated the combination of passive AWGRs and tunable lasers/wavelength converters, that have the inherent benefits of the cyclic property of wavelength assignment through AWG. Due to this, even with more I/O ports than the available channels, through AWGR, we

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**Fig. 2** Schematic of datacenter topology
can scale the excess I/O ports with help of switch architectures. The architectures propose a hybrid scheme of combining delivery-and-coupling switches through cascaded cyclic AWGRs Bhattacharya et al. (2020). Cyclic AWGRs deploys a tunable laser at every input line, that is strategically placed before the delivery-and-coupling switch. The switch employs a buffer-less contention resolution technique that takes every input to develop a centralized arbitration approach that ultimately establishes the required switch state. Another approach is through the design of the delivery-and-coupling switch that employs a simplified buffer-less broadcast-and-select architecture, with support of low-port requirements through cyclic connectivity of AWGRs. To support the design, researchers have employed SOA ON/OFF gates that allow particular sections of the switch to be activated based on preferred selections Srivastava and Singh (2011).

In broadcast-and-select architectures, there is a considerable downfall in the latency performance due to the presence of arbitrating collisions, as present in the case of a centralized control system. These collisions are the reason for the development of a resource lag that decreases the latency performance, due to the increase in the number of the port count. In optical switch designs, the latest developments are inclined towards the layout of efficient controllers that supports sub-μ seconds switching latency at dense connectivity, with a high switch radix. Distributed switches are proposed with context-based clusters in optical datacenters design. To transmit data with low-losses, SOA-based controllers are proposed in switches that support buffer-less architectures and wavelength support through a broadcast-and-select WDM leveraged architecture. The SOA-based switches employ a boolean control with simple ON/OFF keying functionality to simplify hardware and allow electronic edge buffering and retransmissions. The design is scaled to support 1024 × 1024 switch designs. However, with large broadcast-and-select architectures, scalability of design architectures is a critical concern and is an open area of research due to the high splitting ratio. With a high-splitting ratio, optical losses are compensated in the design, and therefore, OSNR needs to be reduced by an increase in the number of the switch port count. In the unlikely event of the unavailability of any intra-switch buffering stage, wavelength-based routing schemes for the switch at scheduling sections are proposed to support optical slots for contention packets. However, with low slot duration, the switch performance drastically reduces and network throughput reduces to ≈ 70 % for switch designs greater than 64 × 64 port layouts Samoud et al. (2015).

1.1 State-of-the art approaches

The section presents a tabular description of different proposed switch designs. Srivastava and Singh (2010) proposed an all-optical switch to support OPS at low packet losses through optical reflectors, and AWG-based wavelength design. The proposed architecture simplifies a routing pattern for AWG to simplify switch design and lowers switch costs. Xiaohui et al. (2010) proposed a optical switch design, named as DOS, that exploits an AWG-based switch fabric at low-latency and high-throughput. DOS supports cyclic-AWGR arbitrator and shows that switching latency is independent of input port size. Wang et al. (2010) proposed an optical circuit switch technology, named as c-Through, with the hybrid packet and circuit switches to support data centers, and lowers the complexity of rack designs. Proietti et al. (2012) proposed an all-optical negative acknowledgment (AO-NACK) scheme that handles contention and deflects contended packets through a reflector scheme to trigger NACK at the sender. Experimentally, the authors proposed an error-free operation at 10 and 40 Gbps, at a host-switch distance of ≈ 20 m and packet-length of
204.8 nano-seconds (ns). Authors in Yin et al. (2013) proposed an AWGR-based loop-back interconnect simulator testbed, called LIONS, to reduce the end-to-end latency. They extended the work of Proietti et al. to reduce the need for feedback loops. The experimental results validated that LIONS performed better than flattened butterfly electrical networks.

In dual-staged buffers, Rastegarfar et al. (2015) proposed an AWG-based flexible design router to support variable load balancing. The proposed design distributes the incoming traffic evenly in both space and time and improves congestion. The paper also addresses the cost of physical layer components and proposes a tradeoff between network layer gain and physical layer penalty in the multistage switched network. Shukla et al. (2016) formulated a routing scheme applicable to modern data centers to accomplish wavelength parallelism through TWC and AWGR. The work compared the designs of two AWG switches in terms of physical and network layer parameters from the proposed switch and formulates a cost-effective solution. Authors in Li and Wai (2008) propose optical switching for wireless infrastructures, with effective load balance at data-centers. Bhattacharya et al. (2019) formulated a two-staged switching buffer to support two sub-sections scheduling and switching subsection, and proposes energy-efficient physical layer computations, along with low packet losses at the physical layer. Table 2 presents the novelty presented in the proposed works, along with the merits/demerits in each case.

1.2 Novelty

As indicated in Sect. 1.1, to envision cost-effective optical switch designs, authors have considered physical, link-level and network layer parameters to include effects of non-linear noise, bit error rates, packet loss measurements, and improved end-to-end latency of users. As the proposed parameters require a tradeoff, hence a design of switch that conforms to all parameters is a critical problem of study. Based on application requirements, the more priority-based parameters are presented while designing the schematics of an effective switch. The article extends the work of Bhattacharya et al. (2019) to include estimation of variable bursts in OBS in the proposed dual-buffer switch design, named as DbOBS scheme, that addresses the limitations of sub-μs latencies for scalable switch designs through a dual-buffer based optical switch. The switch provides a very low information loss rate both in OPS and OBS. In earlier state-of-the-art approaches, the researchers have considered different switch designs, mainly proposed for OPS. In the proposed work, the authors have considered the case of OBS, in which optical buffering is not considered as a viable solution due to the variable burst size. To design the switch buffer, the authors have considered the mean burst length and possible deviation from the mean burst length. This minimizes the burst loss for high contention periods, which is not addressed in the earlier switch designs. For bursty data, at the intermediate or destination node, authors in Shukla et al. (2018) considers an optical network as a sub-network of the mesh network.

In the past, it is shown that for an 8-node network with factor α, defined as the ratio of the link in the considered design in a fully-connected mesh scheme. In this proposed design, the authors have factor α as {0.29, 0.43, 0.71, 1.0}. The proposed work shows that under the mesh degree from α = 0.71 to 1, not much performance improvement is observed even at low loading conditions. For α = 0.29–0.43 buffering does not improve results under higher loading conditions. When buffer overflows (high loading conditions), the only choice is the deflection of the contending burst. Finally, the considered switch design concludes that both buffering and deflection routing are essential in OBS systems.
| Authors                  | Year  | Novelty                                                                 | Merits/Demerits                                                                 |
|-------------------------|-------|-------------------------------------------------------------------------|--------------------------------------------------------------------------------|
| Srivastava and Singh (2010) | 2010  | WDM buffers to support wavelength parallelism with FDL for slot contention | Automated write to the buffer and read from the buffer without explicit control |
| Xiaohui et al. (2010)    | 2010  | Buffer supported with electronic components                              | Persistent storage but fetching latency is more                                 |
| Wang et al. (2010)       | 2011  | Switching in both electrical and optical domain                         | Supports cut-through switch mechanism                                          |
| Proietti et al. (2012)   | 2012  | Replaced buffer schemes through optically induced negative acknowledgment | Re-transmissions of dropped packets is possible but cost overhead at the sender and receiver antennas |
| Yin et al. (2013)        | 2012  | Buffer supports both electronic packets and optical switched packets     | Length of storage slot duration is a variable factor                           |
| Xi et al. (2013)         | 2012  | Buffer-less mechanism to support optical transmission                   | Hardware design is simplified but adds more re-transmissions                   |
| Samoud et al. (2015)     | 2015  | Established QoS parameters during transmission                          | A hybrid buffer scheme to support optical and electronic buffer with differentiated QoS for varied user requirements |
| Wu et al. (2015)         | 2015  | Wavelength multiplexed buffer-less design                               | Design clusters to group similar users and context that lowers latency suitable for data centers |
| Rastegarfar et al. (2015)| 2015  | Dual-stage router design with AWGR component                            | A tradeoff is established in balancing peak loads and supported routing packets through WDM |
| Wang et al. (2016)       | 2016  | Hybrid based buffer                                                     | Varied slots for storing different data packets                                |
| Jain and shukla (2016)   | 2016  | Physical layer analysis with low switch power requirements through switched WDM buffer | Through low powered components, BER is drastically reduced                    |
| Shukla et al. (2016)     | 2016  | Non-linear losses during transmission are compensated through Erbium-Doped Fiber Amplifiers | Very low BER, that induces low packet losses at network layer                  |
| Singh et al. (2018)      | 2018  | A hybrid based buffer with low-powered energy consumption               | Proposed energy computations and efficient buffer scheduling for constrained environments |
| Singh and Tiwari (2018)  | 2018  | Hybrid based buffer                                                     | At network layer, packet loss probability is simulated with earlier designs    |
| Li and Wai (2008)        | 2018  | Combined optical switching to supports wireless infrastructures         | The design is used to support data centers for effective load balancing at core switches |
| Bhattarcharya et al. (2019)| 2019 | Dual stage buffer with switching and scheduling section                  | Compared to early designs, the packet loss rate drops to near zero              |
| Singh et al. (2019)      | 2019  | Hybrid based buffer design                                              | Computational analysis of BER and packet loss probability at network layer      |
| Authors                  | Year | Novelty                                                                 | Merits/Demerits                                                                 |
|--------------------------|------|-------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| Nigam et al. (2018)      | 2019 | A recirculating buffer to control loss of contending packets            | Proposed an scheme with ASE that reduces non-linear noise accumulation in switch |
| Bhattacharya et al. (2020)| 2020 | FDL based AO-NACK scheme                                                | FDL-driven data center switch semantics with lower recirculation losses          |
| Chandra et al. (2020)    | 2020 | Multi-functionality contention resolution scheme with electronic and optical buffers | AO-NACK based FDL buffering scheme for multi-level data centers                  |
| Bhattacharya et al. (2020)| 2020 | Load balanced optical buffer-based contention switch                   | Monte-carlo simulated AO-NACK and FDL scheme for load-balanced buffers           |
| Proposed $DbOBS$         | 2021 | Dual-buffer based variable burst-estimation switch                     | Buffer-estimation based on mean buffer arrivals for variable OB                  |
1.3 Research contributions

The article has the following research contributions

1. A buffer-based estimation for OB is proposed for contention slots. For the same, conditions of over reservation are considered for mean deviation from the burst length estimation.
2. To address the buffer estimation for optical bursts in contention slots, a 2-stage $2N \times 2N$ optical switch design is considered with support for a variable buffer scheme that is strategically placed as storage for contending OB.
3. Extensive simulation results are presented based on variable OB for the bursty traffic model that assumes the arrival of bursts at the different input port of the considered switch design. The states are defined through Markov chains and network and physical layer characteristics are plotted for the considered switch design.

1.4 Layout

The paper is organized into five sections. Section 1 presents the introduction of OB switch designs. Section 2 presents the schematics of buffer estimation for OB. Section 3 presents the dual-buffer based variable OB switch model. Section 4 presents the performance analysis of the considered switch model in terms of link-level and network layer losses, and finally, Sect. 5 presents the concluding remarks and future scope of the article.

2 Schematics of optical burst switching and burst estimations

The section presents the analysis of OBS in different loading conditions related to schematics like burst length, assembly time, which is considered on two conditions-fixed timer-based, or fixed-length based, and the formulation and analysis of the burst length under varied conditions assembly times, slots. We also measure the impact of the burst length by analysis of CDF against burst length, where the condition of over-reservation is also considered. The details are now presented as follows.

2.1 Burst length estimation in OBS

In OBS, we consider that there are $w$ senders that generates data randomly, with a Poisson arrival distribution, as $\{D_1, D_2, \ldots, D_w\}$. The data is packetized randomly and is forwarded to the aggregate router $A_r$. At any given time interval $t_0$, we assume that $A_r$ receives packets as random traffic distribution, and thus, the exact number of packets in unknown to $A_r$. As the packet count is not known in advance, there might be a contention among forwarded packets. In case of contention, buffering of the contending packet is not considered a suitable choice, and is infeasible as the size of the burst depends on multiple factors like- arrival rate, burst assembly time, and inter-arrival rates. Thus, the estimation of burst length is a challenge in OBS-case scenarios. Figure 3 presents the analysis of burst length against the burst assembly time at $A_r$. It can be inferred that at high loads, more packets are collected at $A_r$, and thus burst length reaches a threshold limit before the expiration of the burst timer. However, at low load conditions, fewer packets are collected, and thus the burst length does not reach the threshold size and the timer expires.
To address the above issue, two mechanisms are deployed in the OBS-fixed timer-based algorithm and the fixed-length based algorithm. The algorithms are proposed by Shukla et al. (2018). The details are presented as follows.

1. **Fixed Timer based** In the fixed time-based assembly algorithm. In this scheme, the arriving packets are stored in a temporary buffer $T_b$ for a fixed assembly time, denoted as $T$. Once $T$ is reached, the packets are released from $T_b$ and are transmitted into the core network.

2. **Fixed Length based** The fixed-length based algorithm is based on the burst length $BL$. In this approach, the arriving packets are accumulated until the burst reaches the size of threshold $B_{th}$, and $T$ is not fixed.

However, as depicted in Fig. 3, both the proposed algorithms are not suitable for modeling the bursty traffic conditions at high loads, as $BL$ reaches $B_{th}$, before the timer $T$ expires. At low loads, there is an indefinite wait condition for the burst to gain $B_{th}$, and mostly the timer $T$ expires. Thus the end-aggregate latency increases at low-loads. Thus, in Fig. 3, for condition ($T_1, BL$), there will be higher waiting time with no over-reservation, while for condition ($T_3, BL$) there will not be any waiting time but burst formation time will be much larger than assembly time. Therefore, both the conditions ($T_1, BL$) and ($T_3, BL$) are not favourable. Overall the basic idea is to select burst assembly parameter such that burst length $BL$ just achieve before the timer expires.

To buffer bursts, the burst length $BL$ should be known in advance, and if $BL$ is known, FDL-based buffers are deployed to store the bursts. This makes the burst-length estimation an important problem of study. To formulate $BL$, we assume that arrival data $\{D_1, D_2, \ldots , D_w\}$ at $Ar$ distribution is Poisson with an arrival rate of $\lambda$. At any given time $t$, the total data arrival would be $\lambda t$. The burst length $BL$ is considered of $L$ units in a given time $t$ and can be formulated as gamma distribution with a probability distribution function (PDF) defined as follows Shukla et al. (2018)

$$f(L, \lambda) = \frac{\lambda^L t^{L-1} e^{-\lambda t}}{(L-1)!}, \quad t \geq 0$$

(1)
The mean and standard deviation $\sigma$ at time $\tau$ are depicted as follows.

$$E[\tau] = \frac{L-1}{\lambda}$$

$$\sigma[\tau] = \sqrt{\frac{L-1}{\lambda^2}}$$

(2)

As soon as the first packet arrives at $A_r$, the assembly time $T$ starts, and the probability that the aggregated burst contains $L$ packets is depicted as follows.

$$P(\tau < t) = \int_0^t \frac{\lambda^t t^{L-1}}{(L-1)!} e^{-\lambda t} dt = \frac{\gamma_{inc}(L, \lambda t)}{(L-1)!}$$

(3)

where $\gamma_{inc}$ is the incomplete gamma function. To avoid delays in the transmission and setting time of the intermediate/destination nodes, a control packet is released as soon as the first packet arrives in the assembly buffer. The control packet contains information about the estimated burst length. As the actual burst length is closer to the estimated length, thus, fixing the burst length is a critical problem, with a requirement of a variable-length buffer that stores the contending bursts. If the actual burst length is greater than the estimated burst length, then the extra buffer resource is termed as over-reservation.

**Scenario I: Over-reservation condition:** To formulate the over-reservation condition, let us assume that the actual burst length is $\hat{L}$, with the condition of over-reservation presented as $X = (L - \epsilon)$. The average value of over reservation is now presented as follows.

$$E[X] = \sum_{j=1}^{L} (L - J)(\lambda t)^{(L-J)}(L-J)! e^{-\lambda t}$$

(4)

We consider an asymptotic behavior for infinite packet arrivals, which is depicted as follows.

$$E[X] = \sum_{j=1}^{\infty} (L - J)(\lambda t)^{(L-J)}(L-J)! e^{-\lambda t} = L - \lambda t - 1$$

(5)

**Scenario II: Burst Waiting Time:** If the arrival rate $\lambda$ is high, the burst is created early. We consider the burst in created at time $\tau$ units, with the trivial condition of $\tau < t$. The bursts then waits for the time duration $(t - \tau)$, defined as the burst waiting time. As burst waiting time is random variable, the mean waiting time can be computed as follows.

$$E[t - \tau] = \int_0^t (t - \tau) \frac{\lambda^t (t-1)}{(L-1)!} e^{-\lambda \tau} d\tau$$

$$E[t - \tau] = \frac{t}{(L-1)!} \gamma_{inc} (\hat{L}, \lambda t) - \frac{1}{\lambda (L-1)!}$$

(6)

Under asymptotic conditions, we have

$$E[t - \tau] = \int_0^\infty (t - \tau) \frac{\lambda^t (t-1)}{(L-1)!} e^{-\lambda \tau} d\tau = t - \frac{L}{\lambda}$$

(7)
In the proposed scheme DbOBS, we try to propose the problem formulation as follows:

\[ R_1 : \min E[X] \]
\[ R_2 : \min E[t - \tau] \]

**Algorithm 1 Optimum Burst Length \( L_{opt} \) estimation**

**Input**: Data \( \{D_1, D_2, \ldots, D_6\} \) at \( A_r \), arrival rate \( \lambda \).

**Output**: BL estimate as \( L_{i} \), burst waiting time \( \beta \), and optimum burst length \( L_{opt} \).

**Initialization**: \( n = 1, i = 1, \ INF= 1000000 \)

1: **procedure** `POISSON_ARRIVAL(\( \lambda \))`
2: \( N \leftarrow e^{-\lambda} \)
3: Initialize Array \( U \)
4: \( U[0] \leftarrow \text{rand}() / \text{RAND\_MAX} \)
5: \( \text{while } (1) \text{ do} \)
6: \( n \leftarrow n + 1 \)
7: \( U[i] \leftarrow U[n-1] * \text{rand}() / \text{RAND\_MAX} \)
8: \( \text{if } U[n] \leq N \leq U[n-1] \text{ then} \)
9: \( \text{break} \)
10: \( \text{return } n \)
11: \( \text{end while} \)
12: **end procedure**
13: **procedure** `COMPUTE\_BURST\_LENGTH(\( \lambda, n, t \))`
14: Initialize \( t \)
15: Total arrival \( T_A \leftarrow \lambda t \)
16: Sample = normal(\( L \))
17: \( f \leftarrow \text{normal}(L, \lambda) \)
18: \( E[t] \leftarrow \text{mean}(f) \)
19: \( \sigma[t] \leftarrow \text{std}(f) \)
20: \( P \leftarrow \text{norm}(E[t], \sigma[t]) \)
21: Initialize \( L \leftarrow \epsilon \)
22: \( \text{while } (1) \text{ do} \)
23: \( \text{for } i \leftarrow 1 \text{ to } \tau \text{ do} \)
24: \( \text{for } j \leftarrow 1 \text{ to } \INF \text{ do} \)
25: \( \text{if } (\tau < t) \text{ then} \)
26: \( \beta \leftarrow t - \tau \)
27: \( P \leftarrow \text{norm}(E[t - \tau]) \)
28: \( E[t - \tau] \leftarrow \exp(\lambda, \tau) \)
29: Solve \( E[t - \tau] = 0 \)
30: \( L_{opt} = \lambda t + 1 \)
31: \( \text{plot}(L_{opt}, \text{error}=5) \)
32: \( \text{else} \)
33: \( L_{tot} \leftarrow X \)
34: Compute \( Q \leftarrow X - (L - \epsilon) \)
35: \( E[X] \leftarrow \exp(\lambda, \tau) \)
36: Solve \( E[X] = 0 \)
37: \( L_{opt} = \lambda t \)
38: \( \text{plot}(L_{opt}, \text{error}=5) \)
39: \( \text{end if} \)
40: \( \text{end for} \)
41: \( \text{end for} \)
42: \( \text{end while} \)
43: **end procedure**
By setting up Eqs. 5 and 7 as 0, we get, $L_{opt} = \lambda t$, and $L_{opt} = \lambda t + 1$, respectively. As the timer begins after the arrival of first packet, therefore, in the over over-reservation scenario expected value 1 needs to be added to get the optimum burst length under asymptotic conditions. The optimum burst length is $L_{opt} = \lambda t + 1$.

As depicted in Fig. 4, we consider different values of $L$ and three values for assembly time $t$. The PDF function is approximated as a Gaussian distribution function, which is based on central limit theorem. From the distribution, it can be inferred that 95% and 99.7% areas under the PDF is covered for the range of $m \pm 2\sigma$, and $m \pm 3\sigma$, respectively. As the packet arrives with a Poisson distribution, therefore, both the mean and the variance is $\lambda t$. Based on the above observation, it can be analyzed that $m \pm 2\sqrt{\lambda t}$, and $m \pm 3\sqrt{\lambda t}$, respectively. We next shift towards the measurements of expected buffer size with varying time values. The details are presented in Fig. 5. To simulate the same, we plot with error bars with the consideration of $\lambda = 5$. Now considering $t = 5$, the mean burst length is 25, with 95% of burst with lengths in between ranges of 15 to 35 and 99.7% burst length is between 10 to 40.

Algorithm 1 presents the algorithm for computation of $L_{opt}$. We have considered two sub-procedures in the algorithm. In the first sub-procedure, we initialize the traffic for random arrivals with a specified rate $\lambda$. In the second sub-procedure, we compute $L_{opt}$ and $\beta$, based on $n$, at a given time interval $t$. In the sub-procedure, we have considered both the over-reservation condition and burst waiting time condition based on $\lambda$. Based on the OBS burst estimation, we next propose the switch design to handle the variable length bursts.

3 Schematics of the switch design

The section proposes a dual-buffer based switch design that handles the variable length bursts, based on the estimations of traffic arrivals $\lambda$, and measured burst length $L$, as formulated in Sect. 2. The considered switch design is presented in Fig. 6. We consider a two-stage buffer switch is presented for storage of contenting bursts. A TWC is placed at each input port to either allow direct transfer or places the contending packets in the buffer. Packets that arrives at the various input ports can be send to a common output port based on WDM technology. To realize the same, the switch employs AWG to support wavelength routing. The packets that are multiplexed form different inputs to a common output uses distinct wavelengths, and as AWG supports unused wavelength reuse, $N$ input ports of the switch can be connected to $2N$ output ports via $2N$ wavelengths. At the outputs of $2N \times 2N$ AWG, maximum $N$ ports can be used for buffering and rest $N$ ports are used for direct or next stage transfer of bursts. For the shorter duration of storage $L$ to 9$L$ slots only stage one is used, while in case if the required delay is more than 9$L$, the second stage of the switch is activated for use for the buffering of contending bursts Bhattacharya et al. (2019). In the switch, either in case of buffer or direct transfer of bursts, one burst is received at each output in a single time slot. This is due to the fact that the bursts that leaves the particular loop of the buffer might arrive at incorrect port, due to wavelength routing nature of AWG. Therefore, TWC are placed at the output of the second stage of AWG to select correct output based on the routing pattern of the switching section of AWG.

The complete switch consists of two sections $S_1$ and $S_2$. In $S_1$ FDL of 0 to 9$L$ is chosen where $L$ denotes either the packet size or the minimum burst size, depending on whether the transfer switching is OPS and OBS-based. In the second stage $S_2$, FDL of 10$L$ to 100$L$ is chosen. The maximum length of the fiber in stage 1 is 9$L$ in and in stage 2 is 100$L$. Therefore, the
maximum possible delay is of \(109L\). Thus, in general, we can define the buffering capacity of the two stage switch as follows

\[
B_c^2 = (1 \times x + 10 \times y)L
\]  

(9)

where, \(1 \leq x \leq 9\), and \(1 \leq y \leq 10\). Scaling the switch design, the considered formulation of a three-stage buffer can be computed as follows.

\[
B_c^2 = (1 \times x + 10 \times y + 10^2 \times z)L
\]  

(10)

where, \(1 \leq x \leq 9\), \(1 \leq y \leq 9\), and \(1 \leq z \leq 10\). In general, to support higher order traffic in data-centers, we can extend the concept to a \(j\)-state buffer switch as follows.

\[
B_c^2 = (1 \times a + 10 \times b + 10^2 \times c + \cdots + 10^{j-1} \times j)L
\]  

(11)

where, \(1 \leq (a, b, c, \ldots, (j-1)) \leq 9\), and \(1 \leq j \leq 10\), respectively.

The burst length follows the desired condition.

\[
L = \frac{cB_n p}{nB_r} \geq \frac{cB_{min}}{nB_r}
\]  

(12)

Considering 99.7 % burst prediction accuracy, we have defined the simulation parameters in Table 3.

**Fig. 4** Burst length versus PDF
Fig. 5  Expected burst size versus assembly time

Fig. 6  DbOBS: schematics of the two-stage buffer switch Bhattacharya et al. (2019)
As depicted in Fig. 7, and based on Eq. (13), the minimum fiber length is found out to be 0.8422 km, and the maximum burst size fiber length is 2.88 km. For a dual-stage buffer switch, as depicted in 10, the maximum length of 100 corresponds to 314 km. We consider the fiber loss to be 0.2 dB/Km, then the second stage of buffer would attenuate the signal power considerably, and thus, SOA are placed strategically at the switch inputs to cope-up for the signal and power losses.

4 Performance evaluation

The section now presents the performance evaluation of the proposed scheme DbOBS. We first propose simulation results of burst length estimation. As depicted in Sect. 2, to estimate $BL$, we considered the Poisson arrival distributions of data at $A_r$, and computed PDF for $L$ units at given time interval $t$, denoted as assembly time of bursts. We proposed algorithm 1 to estimate the scenarios of over-reservation, and burst waiting time conditions, to obtain $L_{opt}$.

Then, we propose the simulation results of the $2N \times 2N$ AWG supported dual-switch buffer, as presented in Sect. 3. We considered two-stage switching section $S_1$ and $S_2$, and FDL is formulated for a $j$-stage buffer switch to compute the requirements of $L_{min}$ and $L_{max}$, respectively. The details are now presented as follows.

1. Burst Length Generation and over-reservation We present the conditions of the probability of burst length generation, and over-reservation results. Fig. 8 measures the probability of generation of a particular burst length in terms of CDF, for various values of $t$. To simulate, the assembly time is varied form 2 to 10 units while fixing the arrival rate $\lambda$ at 5. We compute the probability of generation of burst length for different $t$, against different values of $L$. For example, at $t = 6$, the probability of generation of burst of length 20 is 1, and for the burst length of 25 the probability is 0.85. For $L = 30$, the probability is 0.53, and at $L = 40$, the probability is 0.04. Similarly, if we consider $t = 10$, the probability of generation of burst of length 30 is 1, and for $L = 40$, the probability is 0.94, and for $L = 50$ the probability is 0.52. Thus, it can be inferred from the figure that for the smaller assembly time, probability of generation of large size burst is $\approx 0$. On the contrary, for larger assembly time, the probability of generation of larger size burst is close to 1.

Fig. 9 presents the over-reservation versus burst length loading conditions. As inferred, as the burst assembly time increases, the over reservation decreases due to the formation of large size bursts. For example, at $t = 6$, and based on the asymptotic analysis, at $L = 30$, the value of over-reservation is 1.70, whereas over-reservation is 0 for a burst length of 25.

2. Burst Waiting time and Burst Loss Probability Next, we present the analysis of burst waiting time, for different values of $t$, and then we focus on switch analysis through burst

$$L_{min} = \frac{c b (\lambda t - 3 \sqrt{\lambda t})}{n B_r}$$

$$L_{max} = \frac{c b (\lambda t + 3 \sqrt{\lambda t})}{n B_r}$$

(13)
loss probability (BLP) measure vs. load, for fixed and varying buffers. Fig. 10 depicts the waiting time vs. burst length. As evident, for shorter length bursts, the waiting time is more as compared to larger size bursts. For example, at $t = 6$, and using asymptotic analysis, and $L = 30$, the waiting time is 0.44. For $L = 40$, the waiting time is negligible, and is equal to 0.01.

We now present the simulation results for switch design. For the same, we measured the BLP based on a bursty traffic model at different input ports of the switch. We presented the simulation based on the Markov Chain model at network layer design, as proposed in Srivastava and Singh (2010). Figure 11 presents the plot of BLP vs. load for a switch design of $4 \times 4$. We consider a two-stage buffer and measured the impact on BLP at different $L$ values. From the figure, it is inferred that as the burst length increases the BLP increases, due to the lesser available buffer space for the storage of contending bursts. For example, at the load of 0.8, and for $L = 2$, the BLP is $10^{-4}$, whereas with $L = 25$, the value of BLP is $7.1 \times 10^{-2}$.

**Table 3** Parameters for measuring FDL Length for a given assembly time

| Parameters                        | Value        |
|----------------------------------|--------------|
| Assembly time ($t$)              | 1–10 units   |
| Speed of light ($c$)             | $3 \times 10^8$ |
| Refractive Index ($n$)           | 1.45         |
| Bit rate ($B_r$)                 | 40 Gbps      |
| Arrival rate ($\lambda$)         | 5            |
| Number of bits in a packet ($b$) | 1500 bytes   |

![Fig. 7 FDL length versus assembly time](image-url)
3. **Analysis of Burst Loss probability for varying buffer lengths** We now present the BLP analysis for different buffer lengths, for varying and fixed loads. In Fig. 12, BLP versus load is plotted for a switch of size $4 \times 4$ for a two-stage varying buffer and fixed burst of 20. It is inferred that as the buffer space increases the BLP decreases. Comparing the results at the load of 0.8 for $B = 100L$, the BLP is $6 \times 10^{-2}$, while in case of $B = 500L$, the BLP is $7 \times 10^{-4}$. Therefore, with an increase in the buffer space, or by carefully selecting a smaller burst size, the burst loss can be minimized.

Fig. 12 BLP versus load is plotted while considering switch of size $4 \times 4$ for a two-stage buffer and varying burst lengths. At load of 0.8, at $L = 5$, the BLP is $3.4 \times 10^{-4}$, while in case of $L = 50$, the BLP is $1.1 \times 10^{-1}$. Comparing Figs. 11 and 13, it is evident that as the switch size increases, the BLP increases due to more arrival of bursts. Also, as expected, the difference in BLP is negligible at low loading conditions, and as load increases, the difference in BLP becomes significant.

4. We have considered burst prediction accuracy up to 99.7%, therefore, there are chances that for 0.3%, the burst length crosses the predefined limit $L_{\text{max}}$. In such a case, it is not possible to store the contending burst, as the length overflows. Therefore, the overflow bursts would be deflected as proposed in OBS systems.

5 **Conclusions and future scope**

Future data-centers are faced with the dual challenge to process big-data applications, but at low power and switch cost. To address the latency concerns, optical switching is considered a viable option. In optical switching, OBS is a preferred choice as massive data can be aggregated at input switch ports, which are then processed based on optical headers, and forwarded to output ports. However, OBS is far from the reality due to the challenges
Fig. 9 Over reservation versus burst length ($L$)

Fig. 10 Waiting time versus burst length ($L$)
Fig. 11 BLP versus load (for fix buffer and varying burst length, \( N = 4 \))

Fig. 12 BLP versus load (for fix burst length and varying buffer)
of estimation of burst length for storage of contending bursts. To address the concern, the paper proposed a scheme \textit{DbOBS}, that proposes a variable burst estimation algorithm that estimates the mean burst length, and measures deviation from the mean length. The scheme ensures that through the measure of standard deviation, 99.7\% burst can be covered. Once burst length estimation is made, a switch design is considered that contains variable buffers with varying FDLs length options for storage of contending bursts. Thus, the bursty data is captured through FDL and is not lost, and thus fewer retransmissions are present at the sender. Through Monte Carlo simulations, BLP is measured under different loading conditions and varying buffer lengths. The obtained results propose significant improvement over earlier switch designs in terms of BLP at high loads. In the future, the authors would investigate the integration of considered optical switch design with integrated FEONs-based infrastructure services through hybrid integration of software-defined virtual switches and optical backhaul networking stack that can provide data and cloud services effectively among different subscribers in heterogeneous networked units.

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Authors and Affiliations

Pronaya Bhattacharya1,2 · Arunendra Singh3 · Amod Kumar Tiwari4 · Vinay Kumar Pathak5 · Rajiv Srivastava6

Arunendra Singh
arun.sachan@gmail.com
Amod Kumar Tiwari
amodtiwari@gmail.com
Vinay Kumar Pathak
vinay@vpathak.in
Rajiv Srivastava
rajivs18@gmail.com

1 Research Scholar, Computer Science and Engineering, Dr. A.P.J. Abdul Kalam Technical University, Lucknow, Uttar Pradesh, India
2 Department of Computer Science and Engineering, Institute of Technology, Nirma University, Ahmedabad, Gujarat, India
3 Department of Information Technology, Pranveer Singh Institute of Technology, Kanpur, Uttar Pradesh, India
4 Department of Computer Science and Engineering, Rajkiya Engineering College, Churk, Sonbhadra, Uttar Pradesh, India
5 Dr. A.P.J. Abdul Kalam Technical University, Lucknow, Uttar Pradesh, India
6 Ex-Faculty, Department of EE, Indian Institute of Technology, Jodhpur, Rajasthan, India