TEM analysis of Ge-on-Si MOSFET structures with HfO$_2$ dielectric for high performance PMOS device technology

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Abstract. In this paper, we present a (scanning) transmission electron microscopy analysis of novel Ge-on-Si MOSFETs which incorporate a high-k HfO$_2$ dielectric and TaN/TiN metal gate electrodes. A key feature of these devices is the incorporation of a very thin (~1nm) Si passivation layer on top of the Ge virtual substrate, which is partially oxidized to form SiO$_2$ (~0.5nm), before depositing the HfO$_2$ dielectric and TaN and TiN metal gate electrodes. Our results confirm the architecture of the device structures and the existence of Si passivation.

1. Introduction
In recent years, there has been an increased interest in using Ge as a higher charge carrier mobility alternative to Si, for advanced complementary metal-oxide-semiconductor (C-MOS) device applications, based on hole transport [1].

One consideration is the choice and type of substrate used. Rather than using a pure Ge substrate, it has been found that it is possible to grow a relaxed layer of pure Ge onto a (001) Si wafer thereby producing a Ge-on-Si virtual substrate (VS) on to which MOS field-effect-transistor (MOSFET) devices can be processed [2]. One of the issues associated with fabricating such Ge VS-based devices is the need to form, on its surface, a stable dielectric prior to fabricating the gate electrode. One of the drawbacks of Ge-based devices, however, relates to the poorer thermal oxide quality compared with that of Si, which has been found to give rise to a higher interface trap density [3]. Consequently, methods have been developed to reduce this through the use of Ge passivation [4]. One possible route for such passivation involves the deposition of an ultra-thin epitaxial-Si layer on the surface of the Ge.
substrate which is then partially oxidised, prior to the growth of a high-k gate dielectric [4]. There have been issues as to whether Ge segregation during growth of the epi-layer will affect the interface trap density ($N_{it}$); however, charge pumping measurements of fast traps in samples passivated at different temperatures have shown a significant reduction of $N_{it}$ from $\sim 1.5 \times 10^{11} \text{cm}^{-2}$ (at 500°C) to $\sim 5 \times 10^{10} \text{cm}^{-2}$ (at 350°C) [5].

In this paper, we present a TEM/STEM analysis of MOSFETs which are processed on a Ge-on-Si VS. Such devices incorporate a partially oxidised Si passivation layer onto which are deposited high-k HfO$_2$ and metal gate electrodes. The architecture and details of the dielectric region and various other components of the device are measured and verified.

2. Experimental Details

Ge p-MOSFETs were fabricated using a silicon-compatible process flow on (001) Si wafers with a thick (~2 µm) relaxed Ge layer grown on the surface. These were then chemo-mechanically polished (CMP) to remove any cross-hatch surface undulations. After the P well and channel implants, the Ge-on-Si wafer was passivated by growing a thin epi-Si layer (~1nm) which was then partially oxidised at 350°C; see [4]. To avoid further oxidation, a thin layer of HfO$_2$ (~4 nm) was then immediately deposited by atomic layer deposition on the SiO$_2$ before growing the TaN (~10 nm) and next the TiN (~70 nm) metal layers. The remaining processes, i.e. the dry metal gate etch, BF$_2$ extension implants, spacer definition, B implant, NiGe formation in source and drain regions and metal contact fabrication are all detailed elsewhere [6].

The processed wafers include a narrow region of device lines (26 µm wide – 5 mm long) of MOSFETs of various gate lengths which could be processed into TEM specimens. [110] cross-sectional specimens, for the TEM, were prepared in the usual manner with 3 mm disks thinned mechanically to ~30-40 µm followed by Ar$^+$ ion thinning to electron transparency. Finished specimens were then analysed using a JEOL 2010F field-emission gun instrument, operating at 197kV, and equipped with a GATAN imaging filter, Oxford ISIS X-ray detection system and STEM analysis using bright-field (BF) and high-angle annular dark-field (HAADF) detectors.

3. Results and Discussion

A low magnification image of the MOSFET device structures on top of the Ge-on-Si VS is shown in figure 1. One can see that the Ge VS surface (1.63 µm) is uniformly flat as a result of the CMP. These particular devices have a 325 nm gate length and are spaced ~160 nm apart. A high magnification BF STEM image is shown in figure 2, and shows the various components which make up the device structure. The dark layer at the base of the gate electrode is the heavy TaN layer (~14 nm) under which are the HfO$_2$ (3.6 nm) and SiO$_2$ (0.5 nm) gate dielectrics. On top of this is a TiN (~70 nm) metal
electrode (as indicated in figure 2) above which is a SiO$_2$ ‘hardmask’. In the source and in the drain regions, the NiGe (~12 nm) is clearly visible.

A higher magnification BF STEM image of the edge of a large device is provided in figure 3. Here, the Si$_3$N$_4$ side-wall-spacer (SWS) is visible (~40 nm wide and 140 nm high) and is attached to the side of the gate-electrode via 15-20 nm of SiO$_2$ which acts as a SWS adhesion layer. The purpose of the SWS is to prevent the Ni (for the germanidation of the source and drain regions), deposited after SWS formation, from reacting with the sides of the gate terminal. Upon annealing the Ni reacts with the Ge and not with Si$_3$N$_4$. Any residual unreacted Ni is etched away; however, there do appear to be some residual Ni globules decorating the side of the SWS. Under the SWS there is a dark extended HfO$_2$ layer (labelled X) which indicates that the dry etch for gate-electrode definition terminated earlier than intended; however, this is unlikely to impact greatly on device performance.

A further feature of the present device structures is the occasional presence of stacking fault defects at the edge of the gate into the Ge VS, and a lattice image of this is shown in figure 4. Such features appear to be more prevalent in larger gate-length devices (325 nm and greater). They suggest that the regions at the edge of the gate have a particularly high stress concentration giving rise to the nucleation and expansion of dislocation half-loops. The stacking fault is in the glide plane of such loops.

The dielectric region, of a shorter gate-length device, was imaged using planar illumination under high resolution TEM (HREM) conditions and is shown in figure 5(A). One feature of the present device structures is the incorporation of a Si passivation layer grown on top of the Ge VS. This is partially oxidised to form a very thin SiO$_2$ layer, which (from figure 5(A)) was measured to be 0.5±0.1 nm. However, it is difficult to confirm the presence of the residual unoxidised Si from such phase contrast images.

An attempt was made, therefore, to determine the presence of a residual Si layer by HAADF (Z-contrast) imaging, and such an image, in a similar region of the device structure, is shown in figure 5(B). One can see clearly the different brightnesses of the various layers of different mass, and the width of the dark region indicated corresponds to the sum of the

Figure 3. BF STEM image of the edge of larger gate-length (~15 µm) MOSFET device structure showing the architecture of the metal gate, side wall spacer (SWS) and Ni germanide.

Figure 4. Stacking fault at edge of gate.
thicknesses of the residual Si and SiO$_2$ layers (1.2±0.2 nm). Hence, a comparison of these images shows that the thickness of the residual Si passivation layer must be 0.7±0.3 nm.

A particularly important issue is whether there is any Ge present within the residual Si and SiO$_2$ layers. It is known that during growth, Ge may segregate from the surface of the Ge substrate through the epitaxially grown Si layer [7] and may be incorporated into the processed SiO$_2$ layer, or accumulate at the lower Si/SiO$_2$ boundary by ‘snowploughing’. Verifying this is quite a demanding challenge since the layers concerned are extremely narrow. Our images indicate the presence of a residual Si passivation layer, thus it is confirmed that the Ge distribution does diminish at the Ge/Si boundary before reaching the Si/SiO$_2$ interface. However, we cannot rule out small amounts of Ge in the ultra-thin Si passivation and SiO$_2$ layers. We have attempted EELS spectrum imaging to examine the Ge distribution; however, it is extremely difficult to obtain the necessary spatial resolution.

4. Conclusions

Ge-on-Si MOSFET structures have been analysed using TEM-based techniques. A feature of the present devices was the use of Si passivation to reduce interface trap density. This required a very thin epi-layer of Si (1nm) to be grown onto the surface of the Ge-on-Si wafer, which was then partially oxidized. After this a HfO$_2$ high-k dielectric was deposited, followed by TaN and TiN gate electrodes. Our results verified the architecture of the processed devices structures, and confirmed Si passivation. The residual Si passivation layer was found to be 0.7±0.3 nm, and the SiO$_2$ layer was 0.5±0.1 nm.

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