GaN nanowires/ p-Si interface passivation by hydrogen plasma treatment

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Abstract. The effect of hydrogen plasma treatment on the electrical and optical properties of GaN NWs / Si based vertical heterostructures synthesized by the method of plasma molecular beam epitaxy is studied. The effect of treatment has been carefully studied by variation of the passivation duration. Measurements of the electron beam-induced current (EBIC) technique showed the absence of potential barriers between the active parts of the diode and the contacts, which indicates the ohmic behavior of the latter. The current – voltage characteristics show that hydrogen can efficiently passivate recombination centers at the GaN NWs / Si heterointerface. It is established that the optimal passivation duration, providing improved electrical properties, is 10 minutes in the adopted passivation modes. It is shown that a longer treatment causes a deterioration in electrical properties.

1. Introduction

Semiconductor technologies rapid development causes inescapable necessity in semiconductor compound and material properties research to design novel devices and to perfect already existing electronic devices. One of the most promising material hereof would be gallium nitride (GaN) – direct wide bandgap (3.4eV) semiconductor with high thermal and chemical stability as well as radiational resistivity. Except light emitting diodes application, nowadays, GaN had not made its big entrance into the electronic industry yet, however, GaN device market grows by the year. Currently, list of GaN devices in development includes: power conversion transistors, LEDs, microwave integrated circuits, UV laser and photodiodes.

The GaN synthesis on silicon substrate is the most financially promising strategy. Nevertheless, high lattice mismatch with GaN (17%) [1], as well as the high coefficient of thermal expansion (CTE) difference (57%) lead to dangling bonds formation at the heterointerface, followed by the threading
dislocations (TDs) development in the epitaxially growth GaN material [2]. These defects produce trap energy levels (recombination centers) for both electron and hole charge carriers that creates leakage current in the space charge region negatively impacting the device performance. Thus, high crystalline quality planar GaN structure growth requires introduction of the buffer layer for Si-GaN lattice parameter mismatch compensation. However, even when using buffer layers high quality GaN thin film formation is challenging [3].

Alternative approach to the semiconductor devices design and synthesis would be the implementation of the hybrid dimensionality structures [4]. Particularly, there is a huge interest in quasi-1D/planar GaN nanowires (NWs)/Si structures [5,6]. The reason for that would be the unique GaN NWs geometry, which is characterized by the perfect crystalline structure, even in the case of the growth on the poorly lattice parameter matched substrates: in-plane mechanical stress is relaxed in the out-of-plane direction, on the NWs sidewalls surface. This surface relaxation phenomenon allows synthesis of GaN NWs on the large diameter foreign substrates with the high lattice parameter mismatch and the high CTE difference without any buffer layer implementation [7,8]. It can be noted that GaN is characterized by the low density of surface states, which normally act as a recombination centers with the energy states inside of the material bandgap. The growth mechanism is another vital feature of the GaN NWs: no catalyst dripping during the growth is necessary [9], which provides higher crystallinity, lower density of point defects, as well as the improved transport properties, in contrast to the foreign catalyst dripping synthesis method [10]. Thus, GaN NWs implementation reveals new technological opportunities for Si and III-V group materials integration into the device building.

In industrial GaN devices substrate doesn’t function as a charge carrier transport layer, it only supports the functional material and acts as a heat sink. Due to the geometrical features, in the GaN NWs array devices on the Si substrate, the substrate itself will participate in the charge carrier transport, and, as a consequence, the GaN NWs/Si interface will be engaged in it as well. We recently published the paper [11], where we demonstrate the high crystalline quality GaN NWs growth on the Si substrate, nonetheless, we note the high recombination rate at the n-GaN NWs/p-Si interface, which restrains the transport capabilities of our heterostructures.

Among ways to limit the heterointerface recombination rate, surface passivation, hydrogen passivation in particular, - is one of the most widely used method for the Si surface and bulk defect density reduction [12,13]. This method is widely used in microelectronics, for example for Si/SiO2 interface passivation in CMOS-structures, as well as in photovoltaics – for high power conversion coefficient devices production [12,14].

Despite active research, GaN integration with Si technologies and GaN semiconductor device fabrication are not developed to a sufficient degree. There is also a lack of GaN NWs/Si interface passivation process and method studies. The present report is dedicated to the study of the GaN NWs/Si heterointerface hydrogen passivation influence on the optoelectronic device performance.

2. Experimental details
The GaN NWs were synthesized through the plasma-assisted molecular beam epitaxy (PA-MBE) method on the Veeco GEN-III tool. The Si(111) wafers were prepared following the Shiraki method; the GaN NWs growth on the Si substrate was done without buffer layer introduction directly after silicon surface oxide thermal removal (see the detailed procedure in [11]). Figure 1(a) shows the GaN NWs/Si system cross-section SEM image.

The conventional way to evaluate the heterostructure parameters is to study the J-V curve of the interface diode structure. The p-n junction is the simplest example of a such a structure. The GaN NWs exhibit intrinsic electron conductivity [15,16]; in our project we used the p-type doped Si(111)
wafers to study the hydrogen passivation influence on the interface defect density. Therefore, there was a p-n junction formed between the p-Si wafer and the n-GaN NWs array.

Figure 1. SEM image of the GaN NWs/Si heterostructure (a) and SEM image of the encapsulated GaN NWs with ITO top electrode (b).

As mentioned above, the GaN NWs have a n-type conductivity. The additional doping of the NWs tips for the ohmic contact formation with the top electrode was performed through the introduction of the Si dopants into the growth chamber at the final stages of the NWs growth. The temperature of the dopant source was 1150°C, which, according to the work of [5], corresponds to the ~10^{19} cm^{-3} doping level. Thickness of the doped region was estimated to be ~60 nm. The formed structures were then subjected to postgrowth processing in order to form the diode device.

On the first stage of the diode formation, aluminum backside contact to p-Si wafer was formed through the thermal evaporation in the Boc Edwards tool vacuum chamber, which was then followed by the one-minute annealing in the nitrogen flow at 700°C in the JetFirst100 rapid thermal annealing tool. On the next stage, the structure frontside was subject to the HF 10% solution treatment for the oxide removal, followed by the frontside structure passivation in the hydrogen plasma in the plasma-enhanced chemical vapor deposition (PECVD) tool.

In order to passivate the sample surface we varied the structure frontside plasma treatment time: 1, 5, 10, 15 and 20 minutes, at the constant plasma power of 20W, constant pressure and constant process temperature of 350°C.

Directly after the plasma treatment the layer of dielectric material was centrifuged on top of the NWs array structure for the electric isolation of the Si wafer from the top electrode. The photocured epoxy resin SU-8 layer was used as the insulating material. On the next stage, the top layer of the epoxy resin film was etched away in the low-pressure plasma system V15-G to expose the GaN NWs tips for the top contact formation. The SU-8 etch away thickness control was performed through the SEM imaging after each etch iteration.

On the last processing stage, the device front contact was formed: the continuous 100 nm thick layer of transparent conducting indium tin oxide (ITO) material was magnetron sputtered through the metal mask on top of the GaN NWs array. As a result, the circular measuring pads of 2.5 mm in diameter were formed. In order to protect the ITO thin film from the probe contact damage the silver paste point contacts were placed at the edges of the ITO contact pads. Figure 1(b) shows the cross-sectional SEM image of the prototype ITO / n-GaN NWs / p-Si diode structure.
The current-voltage characteristics (J-V characteristics) were measured using a Keithley 2400 SourceMeter multimeter. Thermo-stabilized stage with maintained temperature of 25°C was also used during the measurements.

3. Results and Discussion
For the quality characterization and the correct interpretation of the n-GaN NWs/p-Si J-V curves the ohmic contact between ITO and n-GaN NWs, as well as the between p-Si and Al bottom contact is required. The EBIC technique was used to study the ohmic behavior of the formed contacts through the visualization of the built-in electric fields at the heterointerfaces, and, therefore, the determination of the potential barriers in the contact regions [17]. In the figure 2 you can see the SEM cross-sectional image of the ITO/GaN NWs/Si structure and the corresponding EBIC signal. It can be clearly seen, that there are no special features in the n-GaN NWs/ITO contact region, which indicates the pure ohmic behavior of the contact. On the contrary, in the n-Gan NWs/p-Si heterointerface region there is a bright region on the EBIC map, which signifies the existence of the depletion region in the Si material, more specifically there is a p-n junction at the n-Gan NWs/p-Si heterointerface.

In order to study the potential barrier between the bottom Al contact and the p-Si substrate, two aluminum contacts were formed on the one side of the wafer. The linear J-V curve dependence, in addition to the EBIC measurements (not presented in this report), supports the idea of the ohmic contact between Al and p-Si.

![Figure 2. Heterostructure SEM image (a) and corresponding EBIC map (b).](image)

To study the passivation influence on the charge carrier transport properties of the n-GaN NWs/p-Si J-V curves were measured. Figure 3 shows the evolution of the J-V curves as a function of the passivation time. The fast increment of the non-passivated sample reverse current, and, as a consequence, the low diode threshold voltage, indicates the significant leakage current in the space charge region at the n-GaN NWs / p-Si interface. That is, probably, related to the high defect density in the space charge region. Apparently, the interface defects energy levels sit inside of the bandgap, which allows the main charge carriers to leak through the p-n junction potential barrier at the bias lower than expected one, as well as at the reverse bias condition. The defect formation in the initial structure, as it was already mentioned above, could be associated with the large lattice mismatch between Si and GaN at the base of the nanowire, as well as with the interface defects and dangling bonds formation in the silicon material. It worth mentioning, that the possible scenario is the formation of the nitrides on the Si surface during the GaN NWs growth [18,19], this process can be accompanied
by the defect formation at the interface. Moreover, it is well-known, that there is a non-zero probability of defect formation in the silicon nitride gate layers (only a few nm), this phenomenon has been widely used for non-volatile RAM devices design and development [20].

For the hydrogen plasma treated structures, we can note that there is an increase in the diode threshold voltage, as well as a decrease in the leakage current at the reverse bias, we can link that to the lowering of an active defects’ density in the space charge region at the n-GaN NWs/p-Si heterojunction. The numerical J-V curve analysis allows us to determine the tendency of lowering the leakage current with increasing of the passivation time up to 10 minutes (see figure 3(b)). The further increment of the passivation time negatively impacts the device performance, increasing the leakage current.

![Figure 3](image_url)

Figure 3. The J-V curves for the samples passivated for different time periods (a) and corresponding reverse J-V branches (b). The graph legend is the same for both (a) and (b) parts.

From the EBIC data and known doping level of the Si substrate, we can conclude, that upon passivation the NWs charge carrier concentration should stay at the level no lower than $10^{17}$ cm$^{-3}$, since there was no signal at the NWs base on the EBIC map (see figure 2). In other words, the signal absence indicates a weak charge separation field, which is the case only when the NWs doping level is significantly higher than the Si substrate doping level. We also want to note, that according to our assessment, NWs array resistance under the contact pad is twice smaller than the whole structure series resistance. Therefore, the passivated structure unique J-V curve features are related to the n-GaN/p-Si heterointerface space charge region modification, but not to the NWs charge carriers transport properties change.

There is an explanation for such a dependence of reverse current from the passivation time. At the early stages of passivation hydrogen atoms while diffusing into the substrate passivate the defects and/or dangling bonds at the NWs/substrate interface, decreasing their concentration, which allows to decrease the charge carrier recombination rate in the space charge region. With the longer passivation times hydrogen concentration inside of the silicon substrate increases gradually. It is known, that during the prolonged hydrogen plasma treatment of silicon, hydrogen atoms form defects in the crystalline structure of the material [21–23], they also accumulate in the surface region with subsequent gas bubbles formation [24]. Therefore, the concentration of the hydrogen atoms diffusion induced defects, such as bubbles, increases, which causes the charge carrier recombination rate increase.
Thus, after a relatively short treatment (~10 minutes) time in the hydrogen plasma the passivation of the defects in the n-GaN NWs/p-Si diode’s space charge region can be observed, which improves the rectifying diode properties, and, as a consequence, leads to the diode current increase. With the further increment of the passivation time (>10 minutes) the opposite effect is displayed: degradation of the semiconductor structure through the hydrogen-induced defects.

4. Summary
The current report provides the insight into the n-GaN NWs/p-Si heterointerface characteristics’ dependence on the passivation time in the hydrogen plasma. The data analysis showed, that with no hydrogen plasma treatment there is a significant amount of leakage current in the structure, which is related to the high defect density in the space charge region. It has been shown, that the treatment in the hydrogen plasma effectively passivates the recombination centers in the space charge region and, therefore, improves the diode structure response. The optimal hydrogen passivation time was estimated to be 10 minutes at a hydrogen plasma power of 10W. With the further increase of the hydrogen plasma treatment time the degradation of the system starts to play a role due to the hydrogen induced defect formation in the Si substrate surface layer.

Acknowledgments
The authors acknowledge support from the Ministry of Science and Higher Education of the Russian Federation (RFMEFI61619X0115).

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