A 1.2 mV ripple, 4.5 V charge pump using controllable pumping current technology

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Abstract: This paper represents a 4.5 V regulated charge pump with extremely small ripple. The pump designed with Voltage Doubler (VD) significantly reduces the output ripple voltage. In addition, this circuit utilizes a controllable pumping current (CPC) technology, which achieves automatically adjusting output current by feedback mechanism and resizing transfer transistors. The proposed charge pump has been demonstrated in 0.32 $\mu$m 3D NAND periphery technology under 3 V power supply. Simulation results show that the output ripple voltage is 1.2 mV at 5 mA load current with 0.1 $\mu$F load capacitance. The maximum current drivability and power efficiency is 8 mA and 81\% respectively.

Keywords: charge pump, CPC, small ripple, flash memory

Classification: Integrated circuits

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1 Introduction

The higher capacity storage and lower cost NAND Flash memories are gaining more and more attention in this “Big Data” era. Since 3D NAND Flash has come to market in 2014 [1], the memory array size has been nearly doubled every year [2, 3, 4]. The increasing density of 3D NAND flash array causes the increasing parasitic capacitance of word lines (WLs). As a result, the design of charge pump in 3D NAND flash meets greater challenges [5]. First, ripple voltage on selected WL will bring greater impact on adjacent WLs due to capacitance coupling which could cause worse threshold voltage distribution. Second, load current of 3D NAND Flash is much larger than that of planner due to the enlarged capacitance. Thereby, achieving small ripple and strong current drivability play the most important role in the design of charge pump in 3D NAND Flash memories.

To tackle these issues, this paper proposes a regulated charge pump system based on VD [6] with small ripple voltage of 1.2 mV at 5 mA load current and a maximum current drivability of 8 mA. 1.2 mV ripple at 4.5 V output voltage can meet the requirement of 3D NAND Flash in the future. The system realizes adjustable pumping current and dramatically reduces ripple by using CPC Technology. These properties make this charge pump suitable to implement in 3D NAND Flash. Other characteristics of charge pump such as power efficiency and drivability are comprehensively analyzed and compared in this paper.

2 Novel charge pump with CPC technology

2.1 CPC technology

Feedback mechanism is widely used in charge pump system as shown in Fig. 1 [7]. Black part shows the conventional charge pump system which contains a feedback loop that can regulate the output voltage around a target value. However, it’s difficult to achieve small ripple for the conventional one due to the mismatch
The Output ripple voltage $\Delta V$ of charge pump is expressed in Eq. (1) [8]:

$$\Delta V = \frac{I_{\text{pump}} - I_{\text{load}}}{fC_{\text{load}}}$$  (1)

Where $I_{\text{pump}}$ is the pumping current supplied by charge pump, $I_{\text{load}}$ is the load current, $C_{\text{load}}$ is the output load capacitance and $f$ is the switching frequency between the pumping and blocking periods. According to Eq. (1), smaller mismatch brings smaller ripple and that’s where the key idea of CPC technology lies. For the purpose of utilizing CPC, one more feedback loop used for switch control is added as shown in blue of Fig. 1. What’s more, the intent of capacitor $C_f$ is to compensate the RC delay caused by $R_f$ and $C_f$ [9]. Architecture of VD which will be discussed in the following part is also updated.

The theoretical analysis upon CPC technology is presented in Fig. 2. Blue curves illustrate the operations of charge pump with CPC technology while the black show operations of conventional one. $T_D$ is the delay of feedback loop and the maximum output ripple voltage are marked as $V_{\text{prop}}$ and $V_{\text{conv}}$. Moreover, the ripple can be separated into two parts by 4.5 V voltage level: $V_{\text{ripple, rise}}$ and $V_{\text{ripple, fall}}$. In the regulation phase, pumping current with CPC is more close to load current than that of conventional. As a result, the output voltage ramps more slowly and $V_{\text{ripple, rise}}$ will be decreased. It should be mentioned that reversion leakage current is an inherent drawback of VD [10], CPC technology can also limit the reversion leakage current and $V_{\text{ripple, fall}}$ decreases as well. What’s more, another advantage of this structure is its slower switching frequency of EN which is helpful to decrease dynamic power consumption and noise.

One of the most important parts in CPC technology is the proposed VD. Fig. 3(a) shows the conventional structure. To lower ripple, adopting a clock driver...
with small drivability is a practical way [11]. On the other hand, using transfer transistors with proper size can also generate matched pumping current (See Fig. 3(b)). MN11, MN22, MP11 and MP22 are omitted for better description. When output voltage comes close to target value during the ramping up phase, the larger PMOS pairs (MP1L, MP2L) are turned off by PMOS Enable signal, so the output voltage will ramp more slowly. Once the output voltage reaches target value, the negative feedback loop of clock control is wakened up to regulate output voltage at target value. Because only two small PMOS are in use in regulation phase, pumping current is more matched with load current.

### 2.2 Calculation of ripple

To calculate the ripple of $V_{\text{conv}}$ and $V_{\text{prop}}$, assumes that the pumping current is $I_{\text{pump}}$, load current is $I_{\text{load}}$ and reversion leakage current is $I_{\text{leak}}$. $T_D$, $V_{\text{ripple,rise}}$ and $V_{\text{ripple,fall}}$ are shown in Fig. 2. The total ripple can be described as Eq. (2):

$$V_{\text{ripple}} = V_{\text{ripple,rise}} + V_{\text{ripple,fall}} = T_D(I_{\text{pump}} + I_{\text{leak}})/C_{\text{load}}$$

For better illustration, we bring in a factor $m$, $W$ and $L$ are size of transistors. The size of large and small PMOS are $(W/L)_{l}$ and $(W/L)_{s}$. Define that:

$$(W/L)_{l}/(W/L)_{s} = m$$

According to Eq. (3) and the saturate drain current of p-channel transistor:

$$\frac{I_{\text{pump-l}}}{I_{\text{pump-s}}} = \frac{I_{\text{leak-l}}}{I_{\text{leak-s}}} = \frac{1}{2}\mu_p C_{\text{ox}}(W/L)_l V_{\text{ov}}^2 = \frac{(W/L)_l}{(W/L)_s} = m$$

Where $\mu_p$ is mobility of carriers, $C_{\text{ox}}$ is gate oxide capacitance per unit area and $V_{\text{ov}}$ is the over-drive voltage. Symbol $l$ and $s$ stand for large and small PMOS.

From Eq. (2) and (4), the ripple ratio of ripple voltage is shown in Eq. (5):

$$\frac{V_{\text{prop}}}{V_{\text{conv}}} = \frac{T_D(I_{\text{pump-s}} + I_{\text{leak-s}})/C_{\text{load}}}{T_D(I_{\text{pump-l}} + I_{\text{leak-l}})/C_{\text{load}}} = \frac{(I_{\text{pump-s}} + I_{\text{leak-s}})/(I_{\text{pump-l}} + I_{\text{leak-l}})}{m}$$

We can conclude that compared to conventional charge pump, ripple of proposed charge pump decreases by the factor $m$. 

**Fig. 3.** (a) The circuit of conventional VD and (b) the proposed
3 Simulation results

The proposed charge pump is operating at 3 V supply voltage and uses 0.32-µm 3D NAND technology. Simulation results are obtained from Virtuoso. When load current is 5 mA, the ripple of the conventional charge pump and the proposed one are shown in Fig. 4(a). The factor \( m \) is 30.

![Fig. 4.](image)

Fig. 4. (a) The ripple voltage and (b) ramp-up of output voltage

The ripple of conventional charge pump and the proposed are 20 mV and 1.2 mV and switching frequency of EN is 33 MHz and 20 MHz respectively. Besides, Fig. 4(b) shows that it takes 3 µs to reach 90% of the target level. However, since the results are from pre-layout simulation, the actual measured ripple at 5 mA load current may be larger than 1.2 mV. But the effect of CPC is significant. Fig. 5 illustrates the relationships of average output voltage and ripple voltage between load current. Ripple voltage is almost constant with the large variation of load current from 0 mA to 8 mA.

![Fig. 5.](image)

Fig. 5. Ripple and average output voltage vs. load current

![Fig. 6.](image)

Fig. 6. Efficiency versus load current
Power efficiency is another important factor. It’s defined as (6) [12]:

\[
\text{Efficiency} = \frac{V_{\text{out}} \times I_{\text{out}}}{V_{\text{power}} \times I_{\text{power}}} \times 100\%
\]  

(6)

Where \(I_{\text{power}}\) is average current consumed from power supply and \(I_{\text{out}}\) is average output current. The curve of efficiency as load current varies is shown in Fig. 6. Maximum efficiency is 81% when load current is 3 mA.

With the help of Layout XL in Virtuoso, the estimated layout area is around 0.28 mm\(^2\) except for two 0.5 nF flying capacitors.

Characteristics of the proposed charge pump are shown in Table I. Table II shows the comparison of this work to [11] and [13].

### Table I. Characteristics of the proposed charge pump

| Parameters                  | Value                          |
|-----------------------------|-------------------------------|
| Supply Voltage              | 3 V                           |
| Technology                  | 0.32 \(\mu\)m 3D NAND periphery technology |
| Clock Frequency             | 10 MHz                        |
| Output Voltage              | 4.5 V                         |
| Load Capacitance            | 0.1 \(\mu\)F                  |
| Load Current                | 0 mA ~ 8 mA                   |
| Area                        | \(\approx\)0.28 mm\(^2\)       |
| Ripple                      | 0.85 mV ~ 1.30 mV             |
| Efficiency                  | 50% ~ 80%                     |

### Table II. Comparison of performance

| Parameters                  | [11]  | [13]  | This work          |
|-----------------------------|-------|-------|--------------------|
| Process                     | 0.13 \(\mu\)m | 0.5 \(\mu\)m | 0.32 \(\mu\)m |
| Supply Voltage              | 3.3 V | 2.6 V ~ 3.5 V | 3 V              |
| Output Voltage              | 4.5 V \~ 5 V | 4.5 V | 4.5 V          |
| Load Capacitance            | 2 \(\mu\)F | 1 \(\mu\)F | 0.1 \(\mu\)F |
| Clock Frequency             | 400 KHz ~ 600 KHz | 100 KHz | 10 MHz         |
| Area                        | 0.25 mm\(^2\) | 0.3 mm\(^2\) | \(\approx\)0.28 mm\(^2\) |
| Ripple @ 5 mA Load Current  | 21 mV | 8 mV  | 1.2 mV           |

### 4 Conclusion

This paper has presented a novel charge pump with CPC technology which significantly reduces the output ripple voltage under a large load current variation. The proposed charge pump operates at 3 V supply voltage and 0.32 \(\mu\)m technology. The pre-layout simulation results show that when output voltage is 4.5 V and load current is 5 mA, the ripple is 1.2 mV with 0.1 \(\mu\)F load capacitor.

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