Optimized Graphene Electrodes for contacting Graphene Nanoribbons

Oliver Braun, Jan Overbeck, Maria El Abbassi, Silvan Käser, Roman Furrer, Antonis Olziersky, Alexander Flasby, Gabriela Borin Barin, Rimah Darawish, Klaus Müllen, Pascal Ruffieux, Roman Fasel, Ivan Shorubalko, Mickael L. Perrin, and Michel Calame

a. Transport at Nanoscale Interfaces Laboratory, Empa, Swiss Federal Laboratories for Materials Science and Technology, 8600 Dübendorf, Switzerland
b. Department of Physics, University of Basel, 4056 Basel, Switzerland
c. Swiss Nanoscience Institute, University of Basel, 4056 Basel, Switzerland
d. Kavli Institute of Nanoscience, Delft University of Technology, 2628 CJ Delft, The Netherlands
e. Department of Chemistry, University of Basel, 4056 Basel, Switzerland
f. IBM Research – Zurich, 8803 Rüschlikon, Switzerland
g. nanotech@surfaces Laboratory, Empa, Swiss Federal Laboratories for Materials Science and Technology, 8600 Dübendorf, Switzerland
h. Department of Chemistry and Biochemistry, University of Bern, 3012 Bern, Switzerland
i. Max Planck Institute for Polymer Research, 55128 Mainz, Germany

Corresponding authors:

*E-Mail: mickael.perrin@empa.ch

**E-Mail: michel.calame@empa.ch

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Atomically precise graphene nanoribbons are a promising emerging class of designer quantum materials with electronic properties that are tunable by chemical design. However, many challenges remain in the device integration of these materials, especially regarding contacting strategies. We report on the device integration of uniaxially aligned and non-aligned 9-atom wide armchair graphene nanoribbons (9-AGNRs) in a field-effect transistor geometry using electron beam lithography-defined graphene electrodes. This approach yields controlled electrode geometries and enables higher fabrication throughput compared to previous approaches using an electrical breakdown technique. Thermal annealing is found to be a crucial step for successful device operation resulting in electronic transport characteristics showing a strong gate dependence. Raman spectroscopy confirms the integrity of the graphene electrodes after patterning and of the GNRs after device integration. Our results demonstrate the importance of the GNR-graphene electrode interface and pave the way for GNR device integration with structurally well-defined electrodes.

1 Introduction

New classes of electronic nanomaterials often require several years to decades of research to develop reliable electrical contacting approaches. For example, it took more than two decades to go from the first carbon nanotube (CNT) field-effect transistors to their successful integration into microprocessors.[1–5] Similar timescales were also needed to develop the field of semiconducting nanowires from the first reporting of Si-whiskers to their reliable use for quantum computing.[6–8] In the case of Si-nanowires, surface passivation of the contact area and thermal annealing were found to increase device performance significantly.[9] More recently, bottom-up synthesized atomically precise graphene nanoribbons (GNRs) have attracted a lot of attention as their electronic and magnetic properties can be tailored by bottom-up synthesis. However, contacting GNRs using top down fabrication processes turned out to be highly demanding, in particular, because of their nanoscale dimensions of around 1 nm in width and lengths reaching typical 5-50 nm.[10–15]

Standard electron beam lithography and metallization processes have been used by several groups for contacting GNRs.[12, 16, 17] However, these methods involve processing and metallization on top of transferred GNRs and can lead to the introduction of contaminants at the contact-GNR interface
and/or GNR damage. This approach is particularly problematic for GNRs with reactive and/or function-alized edges.[18–21] Alternatively, GNRs have also been transferred on top of predefined metal elec-

trodes.[22] This approach may be suitable for GNR films in which hopping of charge carriers over larger distances is the dominating effect on transport properties but may lead to ill-defined 3-dimen-
sional junction geometries when contacting a single GNR. Furthermore, metal electrodes in short-

channel devices lead to the formation of image charges and screen the applied electrostatic gate field used to tune the electronic transport, requiring advanced gating approaches such as ionic liquid gating for reaching a sufficient gating efficiency.[12, 23–25] Finally, we expect that the disorder of metallic electrodes at the atomic scale leads to uncontrolled local electrostatic potential surrounding the nano-
scale object, a problem that 2D covalent crystals have the potential to overcome.

The above-mentioned issues can be addressed by the use of graphene electrodes. Graphene, with its monoatomic thickness, allows for the GNRs to be transferred on top of the electrodes, without intro-

ducing significant bending of the GNRs bridging the source and drain electrodes. The π-π orbital over-

lap is widely used for contacting two-dimensional materials [26, 27] and the charge carrier density in the graphene leads can be tuned by electrostatic gating. Graphene electrodes fabricated using the well-established electrical breakdown procedure result in gaps separating the electrodes by a few nano-
meters and are a suitable way to contact graphene nanoribbons of various types.[11, 13, 28–31] However, inherent geometric variation in such electrodes requires particular care during data analysis. This is necessary to disentangle the signal of the material under study from the direct tunneling current contributions, potential localized lead states, and to exclude reconnected graphene electrodes or con-

nected graphene islands.[32–35] Moreover, the long fabrication time of each gap impacts the scalabil-

ity of this approach.

Here, we report on graphene electrodes fabricated by electron beam lithography (EBL) using the combi-
nation of an optimized etch mask and etching recipe, which results in electrode separations down to <15 nm. This clean and well-defined electrode geometry helps to overcome the challenges empha-
sized above and represents an appealing platform to contact GNRs with a length of length above 15 nm. Moreover, the availability of large-scale graphene produced by chemical vapor deposition (CVD) allows us to fabricate up to 1680 devices per chip.
We demonstrate the suitability of our nanofabrication approach by integrating atomically precise 9-AGNRs in a field-effect transistor (FET) device.[36] 9-AGNRs are the ideal testing material due to their long-term stability and their well-studied transport properties.[37, 38] In addition, we show that thermal annealing is an efficient way to enhance the electrical device properties leading to an increase in the on-state current of up to an order of magnitude at room temperature. Moreover, our gate-dependent electrical transport measurements show on-off ratios reaching values as high as $10^4$. The results obtained in this work open perspectives for the integration of different types of GNRs in more complex device geometries.

2 Experimental

2.1 Graphene growth and transfer

Polycrystalline graphene is synthesized via chemical vapor deposition (CVD) in a tube furnace (Three zone HZS, Carbolite). A 25 μm thick copper (Cu) foil (Foil 2017, No. 46365, Alfa Aesar) is prepared at room temperature by first cleaning in acetone (15 min), rinsing in isopropanol (IPA), immersion in de-ionized (DI) water (5 min), acetic acid (30 min), DI-water (20 min + 5 min in an ultrasonic bath), ethanol (1 min) and blown dry with N2 before a reduction annealing in an H2-rich atmosphere (20 sccm H2 in 200 sccm Ar) at 1000 °C and <1 mbar for 60 min. Before the growth, the pressure inside the tube is increased to 110 mbar by partially closing the downstream valve. Graphene growth is initiated by the addition of 0.04 sccm CH4 to the chamber for 22 min. The growth is terminated by stopping the CH4 flow, reducing the pressure by opening the downstream valve, opening the lid of the tube furnace, and circulating air with a fan to allow for an abrupt drop in temperature. The cool down procedure (to <100 °C) takes 45 min. The as-grown single-layer graphene is transferred onto a specially-developed substrate for device integration of GNRs (target substrate) using a wet transfer method.[39] Poly(methyl methacrylate) (PMMA) 50K (AR-P 632.12, Allresist GmbH) is spun onto the graphene-coated Cu foil and the backside graphene is etched using reactive ion etching (RIE). Cu is etched away using a copper etchant (PC COPPER ETCHANT-100, Transene) for 60 min leaving the graphene/PMMA film floating on top. The etchant is then replaced by DI-water in a stepwise dilution process. The DI-water is then replaced by a 10 % HCl solution for 5min. After a final rinsing in DI-water, the graphene/PMMA film is fished out with the target substrate. After settling under ambient conditions for 30 min, the target
substrate/graphene/PMMA stack is placed in an oven and heated to 80 °C for 1 h followed by a second heating step at 80 °C for at least 12 h under vacuum conditions (<1 mbar) to ensure good adhesion of the graphene to the target substrate. PMMA is removed in acetone for 10 min at room temperature, 60 min at 56 °C, followed by a 30 min cool down period. Finally, we perform an IPA rinsing step followed by N2 dry blowing. This process yields clean, single-layer graphene with low defect density on the target substrate, see Fig. S1.[40]

2.2 Graphene patterning

To define graphene electrodes, graphene on Si/SiO2 with predefined metal electrodes and optimized areas for Raman spectroscopy is patterned by EBL as detailed below. Two exposure steps (100 kV write mode, EBPG5200, Raith GmbH) are done, each followed by an RIE step.[39]. For the first exposure step, the sample with graphene is spin-coated with 160 nm thick PMMA 50K (AR-P 632.06, Allresist GmbH) and 90 nm thick PMMA 950K (AR-P 672.02, Allresist GmbH), each baked at 180 °C on a hotplate for 5 min. Following a first electron beam exposure, the resist is developed in Methyl-isobutylketone (MIBK):IPA (1:3) at room temperature for 60 seconds. RIE (15 sccm Ar, 30 sccm O2, 25 W, 18 mTorr) for 30 s is used to remove the accessible graphene. PMMA is removed using acetone, IPA, and N2 dry blow. After this pre-patterning of the graphene, a second EBL and RIE step (same etching plasma parameters as above, reduced time of 6 s) are carried out to separate the graphene electrodes.

Two different approaches for the fabrication of etch masks were investigated:

i) **CSAR mask**: In the first approach, a 60 nm thick CSAR resist (AR-P 6200.04, Allresist GmbH) is spin-coated. Following the second electron beam exposure, the resist is developed using a suitable developer (AR 600-546, Allresist GmbH) at room temperature for 1 min followed by an IPA rinse. After RIE, the etching mask is removed by immersing in 1-Methyl-2-pyrrolidinone (NMP) (Sigma Aldrich) at room temperature for 10 min followed by 60 min at 80 °C, cooled down for 30 min, rinsed with IPA, and blown dry with N2.

ii) **PMMA mask and cold development**: In the second approach, a 60 nm thick layer of PMMA 950K (AR-P 672.02, Allresist GmbH) diluted in anisole (1:1) is spin-coated. The development of the resist after electron beam exposure is done in MIBK:IPA (1:3) at 2 °C
for 45 s followed by an IPA rinse at 2 °C for 10 s. After RIE the etch mask is removed in the same way as after the first RIE step.

Both approaches yield clean and well-separated graphene electrodes with reproducible gap sizes (see Results and Supporting Information).

### 2.3 Graphene electrode separation

The separation of graphene electrodes (gap size) is assessed using scanning electron microscopy (SEM) (Helios 450, FEI) and atomic force microscopy (AFM) (Icon, Bruker) is employed to independently determine the electrode separation. The AFM is equipped with a sharp cantilever (tip radius = 2 nm) (SSS-NCHR-20, Nanosensors) operated in soft-tapping mode. The electrode separation by AFM is determined via a Python script, based on the nanoscope library.[41] Each line scan is smoothed individually using a Savitzy-Golay filter and the edges of the gap are determined by selecting the local maxima and minima in the first derivative on either side of the gap minimum. It was not possible to apply the same procedure to the SEM data due to the low contrast between the graphene and the SiO₂ of the target substrate and the small separation of the graphene electrodes. Therefore, the average and standard deviation are obtained from 20 manual measurements that are equally spaced along the gap.

### 2.4 Graphene quality after patterning

The patterned graphene electrodes are analyzed in air by 2D Raman mapping (Alpha300R, WITec) using a 488 nm incident laser beam at 1.5 mW and a 100x objective (NA = 0.9) with a pixel spacing of 100 nm.[39]

### 2.5 On-surface synthesis of 9-AGNRs and transfer to a device substrate

9-AGNRs were synthesized from 3’,6’-diiodo-1,1’:2’,1”-terphenyl (DITP).[10] Two types of GNRs, uniaxially aligned and randomly oriented, are transferred onto the sample. Using Au(788) as growth substrate results in uniaxially aligned 9-AGNRs (GNRs grown along the narrow (111) terraces) while using Au(111)/mica leads to non-aligned 9-AGNRs. [42, 43] In both cases, Au(788) single crystal (MaTeK,
Germany) or Au(111)/mica growth substrates (Phasis, Switzerland), are cleaned in ultrahigh vacuum by two sputtering/annealing cycles: 1 kV Ar⁺ for 10 min followed by annealing at 420 °C for Au(788) and 470 °C for Au(111)/mica for 10 min. Next, the precursor monomer DITP is sublimed onto the Au surface from a quartz crucible heated to 70 °C, with the growth substrate held at room temperature. After deposition of 1 monolayer DITP, the growth substrate is heated (0.5 K/s) to 200 °C with a 10 min holding time to activate the polymerization reaction, followed by annealing at 400 °C (0.5 K/s with a 10 min holding time) to form the GNRs via cyclodehydrogenation.

The average GNR length is between 40 and 45 nm.[10] 9-AGNRs are transferred from their growth substrate to the silicon-based target substrates with predefined graphene electrodes by two different transfer approaches. 9-AGNRs grown on Au(788) crystals are transferred by an electrochemical delamination method using PMMA as described previously.[39, 44, 45] 9-AGNRs grown on Au(111)/mica are transferred using a polymer-free method as described elsewhere.[16, 37, 46]

2.6 Electronic measurements

All electronic measurements are performed under vacuum conditions (<10⁻⁶ mbar) in two different probe stations. The FETs consisting of aligned GNRs using the polymer-assisted transfer are characterized in a custom-built probe station equipped with nanopores (miBot, Imina Technologies SA). A data acquisition board (USB-6289, National Instruments) is employed to apply the bias and gate voltages and read the voltage output of a custom-made I–V converter (Model SP983, Basel Precision Instruments GmbH). The FETs consisting of GNRs using the polymer-free transfer method are characterized in a commercially available probe station (Lake Shore Cryogenics, Model CRX-6.5K). A data acquisition board (ADwin-Gold II, Jäger Computergesteuerte Messtechnik GmbH) is employed to apply the bias and gate voltages and read the voltage output of the I–V converter (DDPCA-300, FEMTO Messtechnik GmbH).
3 Results and discussion

3.1 Graphene electrodes

The fabrication process yielding graphene electrodes for contacting graphene nanoribbons is illustrated in Fig. 1 and described in detail in the experimental section.

**FIG. 1.** Fabrication procedure and electrical measurement configuration. Three-dimensional illustration describing the fabrication steps of the EBL defined graphene electrodes. The resist regions exposed during electron beam lithography are marked with darker colors. Arrows indicate fabrication order. The electrical measurement configuration is schematically shown in the last, slightly larger, illustration. See main text for details.

We stress that for etching nanogaps into graphene the interplay of the used etch masks, their removal, as well as the chosen etching parameters, plays an even more crucial role in obtaining the wanted feature resolution than for evaporated features.

First, it is crucial to split the resist exposure by electron beam into two steps to ensure the proximity-effect while writing the coarse features does not affect the sensitive exposure of the nanogap. For the
second exposure, we use a beam step size of 5 nm and beam current of 3 nA resulting in a beam diameter of 5 nm. Second, for the first RIE step to pattern the coarse features, a double layer etch mask is employed that helps reduce contaminations on graphene by using a low molecular weight resist in direct contact with the graphene and a high molecular weight resist on top for high contrast and feature definition. We note that the undercut in the double layer resist does not pose a problem, as the feature sizes in this first RIE step are not critical. For the second RIE step, an undercut is unwanted since it would result in a larger electrode separation. The smallest graphene electrode separation (<15 nm) is achieved using CSAR resist, due to its excellent performance in terms of resolution, sensitivity, and etch resistance.[47]

Third, we emphasize that the duration of the second RIE step has to be short enough to avoid a sideways etching of the resist mask but long enough that the monolayer graphene is fully etched. This trade-off leads to a delicate balance between device yield and electrode separation. Last, the removal of the etch mask has to be done using processes that are sufficiently mild to preserve graphene’s quality but sufficiently harsh to leave little residues on the electrodes. We therefore, employed only acetone and NMP since their effects on graphene’s quality are well studied.[48–51]

Since the used GNR growth substrates do not exceed 5x5 mm in size, after fabrication the chip is broken into smaller pieces with 100-200 devices each before the GNRs to target substrate transfer.

3.2 Characterization of patterned graphene electrodes

Before the electrode separation is assessed, an optical inspection of the graphene electrodes is carried out. Graphene electrodes containing graphene folds in the central region or those damaged during thefabrication process are excluded from further investigation. A typical optical image of the graphene electrodes can be seen in Fig. 2(a).
FIG. 2. Electrode separation of devices fabricated using CSAR mask. (a) Optical image of a representative device. Of the central region of the same device is shown in (b) a SEM image and in (c) a height profile (AFM scan) including a line cut through the central region (red) showing the electrode separation. (d) Electrode separations measured by SEM and AFM for four devices with different gap sizes. (e) Raman intensity maps for D-, G- and 2D-bands in the area indicated with a black square in (a) and spectra extracted at representative positions.

The electrode separation is assessed by SEM and AFM and representative scans are shown in Fig. 2(b) and 2(c), respectively, with in Fig. 2(d) extracted gap sizes. We find that the graphene electrodes fabricated with the CSAR etch mask (see experimental section) are separated by <15 nm for the smallest designed geometry. The fabrication method using the PMMA etch mask yields a slightly larger electrode separation of around 27 nm in the smallest case (See Fig. S3). Hence, these electrodes are only used for the uniaxially aligned 9-AGNRs in order to have high device yields.
also shows that the measured electrode separation for the CSAR etch mask does not scale linearly with the width of the gap in the design. We attribute this behavior to the proximity-effect correction procedure that is applied for the exposure dose calculation.

For a successful device integration of GNRs, we consider it important to have graphene electrodes with little to no defects after patterning. Raman spectroscopy maps confirm the high quality of the graphene electrodes after processing (see Fig. 2(e)). The D-band intensity map shows in the pristine area neglectable intensity and an intensity increase at the edges and in the nanogap region. Raman spectroscopy further revealed a clear drop in the intensity of the G- and 2D- bands where the graphene electrodes are separated, indicating a lower amount of carbon and breaking of the crystal structure. The 488 nm excitation source was chosen to reach a minimal laser spot size for best spatial resolution. The high graphene quality was also confirmed by measuring the current versus applied gate voltage of a reference device that underwent the same fabrication procedure except for the 2nd RIE step, revealing field-effect mobilities of 2'500 cm²/Vs for electrons and 1'800 cm²/Vs for holes (see Fig. S3).

We optically assessed 91 devices for the two transfer methods based on which we excluded 24 devices. After the initial optical assessment and prior to the 9-AGNR transfer, each device is characterized electrically. A schematic illustration of the electronic wiring for the latter is depicted in Fig. 3(a). As shown in Fig. 3(b) a high yield of clearly separated graphene electrodes (>1 TΩ) of 79.1 % is found. The remaining 20.9 % of graphene electrodes are either weakly (<1 TΩ) or fully connected (<1 GΩ). Representative I-V characteristics for the three cases are shown in Fig. 3(c).
3.3 Electrical characterization and effect of annealing

After the initial characterization of the devices, 9-AGNRs were transferred on top of the graphene electrodes. Fig. S4 shows high resolution scanning tunneling microscope (STM) images of 9-AGNRs on
the growth substrates presenting their alignment. We note that the growth and transfer method were adapted to the gapsize. For the devices fabricated using the PMMA mask (gapsize \( \sim 28 \text{ nm} \)), uniaxially aligned GNRs were transferred oriented perpendicular to the gap to maximize the chance of bridging both electrodes. For the devices fabricated using the CSAR mask (gapsize <15 nm), based on geometrical considerations, we anticipate a higher probability of bridging that allows for investigating non-aligned 9-AGNRs transferred using a polymer-free method. In both cases, the integrity of the 9-AGNRs after the transfer process was confirmed by Raman spectroscopy (Fig. S5). In particular, the presence of the longitudinal compressive mode (LCM) is strong evidence for the high quality of the 9-AGNRs after the transfer process due to its high sensitivity to structural damage.[45] Fig. 4(a) shows typical I-V characteristics recorded at room temperature under vacuum conditions \(<10^{-6} \text{ mbar}\) on different devices fabricated using the two transfer methods. We observe highly nonlinear I-V curves with currents up to 0.5 nA at 1 V bias voltage. The inset presents a schematic of the device and the electrical characterization scheme.

To improve the maximum currents through the devices, we investigated the effect of thermal annealing. As the transfer of the 9-AGNRs onto the target substrate exposes the graphene to humidity and even water in the case of the polymer assisted transfer, the samples were heated to 150 °C for 30 minutes at \(10^{-6}\) mbar to remove water residues at the graphene/GNR interface. The heating also provides energy for local geometric rearrangements. To evaluate the benefit of this thermal treatment, the maximum currents observed at a gate voltage of 0 V and a bias voltage of 1 V are compared before (as transferred, \(I_{\text{transferred}}\)) and after thermal annealing (\(I_{\text{annealed}}\)). Fig. 4(b) shows a scatter plot of the ratio \(I_{\text{annealed}} / I_{\text{transferred}}\) for all devices. Over all samples, an increase by one order of magnitude or higher in 50 % of the devices is observed, with individual junctions showing an increase as high as a factor of 100.

During annealing, several processes can take place and affect the conductance of the junctions. By reducing the number of water adsorbates at the GNR-graphene interface, the two nanomaterials can go into a more intimate contact, which can lead to an increased electronic coupling similar to what has been observed for decoupled graphene monolayers.[52, 53] Water removal may also result in reduced doping of the GNRs, leading to a probing of the more intrinsic GNR transport properties, similar to
what has been reported for graphene FETs on SiO₂. Studies of molecules with planar anchor groups on graphene electrodes revealed that the binding energy to sliding and bending is around 0.01 eV, significantly lower than the energy $k_B T$ (~0.04 eV) provided during the thermal annealing process. Hence, this energy likely is sufficient to cause local displacement and geometrical rearrangements of the GNRs that can lead to both improved contact but also loss of GNRs within the junction and a decrease of overall conductance in multi-GNR junctions as can be seen by a conductance decrease in about 20% of the devices after annealing. We note that at the annealing temperature used, no lateral fusion of GNRs is expected.

FIG. 4. (a) I-V characteristics of four representative 9-AGNR devices for each of the two transfer methods before thermal annealing. (b) The main panel shows the ratio of current values measured before and after the annealing of the devices. Current increase and decrease are highlighted in green and red respectively. Histograms of $I_{\text{transferred}}$ and $I_{\text{annealed}} / I_{\text{transferred}}$ are shown in the outer panels on the top and the right respectively. Highlighted in blue are 50% of the devices. (c) I-V characteristics of device

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E recorded at different applied gate voltages after annealing. Inset shows the effect of annealing on the I-V characteristics. (d) Current – gate voltage dependence at fixed bias voltage for two devices. Arrows indicate the direction of the gate sweep. The blue dashed line indicates the noise floor of the I-V converter. The inset shows a histogram of the on-currents.

In Fig. 4(c), we measured current-voltage characteristics at various applied gate voltages. The plot indicates slightly asymmetric characteristics with a strong gate dependence. The presence of only little hysteresis effects between the up and down sweep of the applied bias voltage indicates high device stability. The observed hysteresis is attributed to the influence of trap states in the oxide.[60] Fig. 4(d) shows a measurement of the current as a function of gate voltage for two devices, recorded at a fixed applied bias voltage of 1 V (extended data see Fig. S6). The traces show a drastic increase of the conductance for negative gate voltages, pointing towards hole transport through the valence band (or highest occupied molecular orbital (HOMO)).[12] The gentle increase in conductance at positive gate voltages suggests the presence of another transport channel entering the bias window, presumably the conduction band (or lowest unoccupied molecular orbital (LUMO)). In the gate sweeps, we obtain maximal on-off ratios of up to $10^4$, with an on-current of 70 nA at a gate voltage of -100 V and an off-current of 5 pA at a gate voltage of +40 V for the black curve in Fig. 4(d). The maximum observed values for the on-off ratios is about a factor of 100 higher than reported by Martini et al. and El Abbassi et al. contacting 9-AGNRs using graphene electrodes fabricated by electrical breakdown, and about a factor 50 higher than reported by Jangid et al. for top-down fabricated GNRs.[11, 30, 61]

4 Conclusions

We successfully integrated 9-AGNRs in a FET geometry using graphene electrodes fabricated via optimized e-beam lithography and reactive ion etching resulting in electrode separations as small as <15 nm. Room-temperature electrical transport measurements revealed nonlinear current-voltage characteristics and a strong gate dependence. Furthermore, we find that thermal annealing improves the on-currents after annealing by at least one order of magnitude in 50% of the investigated devices. In addition, we performed gate sweeps revealing on-off ratios as high as $10^4$ with the highest on-currents of 70 nA at a bias voltage of 1 V.
The developed technology to fabricate graphene electrodes separated by <15 nm is a major step forward towards all-carbon electronics and offers encouraging prospects for room-temperature ambipolar 9-AGNR-FET behavior. The presented platform could also be applied for short channel FETs using two-dimensional materials as channel material, as reported for MoS$_2$ or phase-change memory devices.[62, 63] Importantly, this platform will allow for the integration of GNRs of different widths as well as different edge structures for exploring more exotic transport properties.[13, 64]

CRediT authorship contribution statement

**Oliver Braun:** Conceptualization, Methodology, Investigation, Writing – Original Draft, Writing – Review & Editing, Visualization, Project administration. **Jan Overbeck:** Conceptualization, Methodology, Investigation, Writing – Original Draft, Visualization. **Maria El Abbassi:** Investigation. **Silvan Käser:** Investigation. **Roman Furrer:** Resources. **Antonis Olziersky:** Investigation. **Alexander Flasby:** Software. **Gabriela Borin Barin:** Writing – Original Draft, Resources. **Rimah Darawish:** Resources. **Klaus Müllen:** Resources. **Pascal Ruffieux:** Supervision. **Roman Fasel:** Funding acquisition, Supervision. **Ivan Shorubalko:** Conceptualization, Methodology. **Mickael L. Perrin:** Writing – Original Draft, Writing – Review & Editing, Visualization, Supervision. **Michel Calame:** Conceptualization, Writing – Original Draft, Writing – Review & Editing, Visualization, Funding acquisition, Supervision

Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Appendix A. Supplementary information

Supplementary information to this article is available free of charge.
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