A 1.2 Gb/s Data Transmission Unit in CMOS 0.18 µm technology for the ALICE Inner Tracking System front-end ASIC

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ABSTRACT: The upgrade of the ALICE Inner Tracking System is based on a Monolithic Active Pixel Sensor and ASIC designed in a CMOS 0.18 µm process. In order to provide the required output bandwidth (1.2 Gb/s for the inner layers and 400 Mb/s for the outer ones) on a single high speed serial link, a custom Data Transmission Unit (DTU) has been developed in the same process. The DTU includes a clock multiplier PLL, a double data rate serializer and a pseudo-LVDS driver with pre-emphasis and is designed to be SEU tolerant.

KEYWORDS: Digital electronic circuits; Radiation-hard detectors; Front-end electronics for detector readout
1 The ALICE ITS upgrade

The upgrade of the Inner Tracking System of the ALICE experiment foresees the replacement of the existing 6 layers of silicon detectors, based on 3 different sensor technologies (namely Silicon Pixel, Drift and Strip detectors), with 7 layers all constructed with Monolithic Active Pixel Sensors (MAPS) [1]. The 7 layers can be divided into 3 inner barrel (IB) layers, 2 middle barrel (MB) layers and 2 outer barrel (OB) layers, as shown in figure 1.

![Figure 1](image)

Figure 1. The layout of the new ALICE ITS.

The sensor and front-end ASIC, named ALPIDE [2], is a 30 mm × 15 mm chip with a matrix of 1024 × 512 pixels. The size of each pixel is 28 µm × 28 µm. About 24000 chips will be required
to cover the \( \sim 10 \, \text{m}^2 \) active area of the full ITS, which gives a total of about 12.5 billion pixels. The ASICs are organized in modules; IB layers modules consist of 9 chips in a single row, while MB and OB layers are based on 14 chips modules on two rows.

In order to transmit the huge amount of data (of the order of 10 kevents/cm\(^2\) at 100 kHz interaction rate) generated by such a high detector granularity with the stringent space and material budget requirements typical of an inner tracker, a high speed serial interface is mandatory. The most critical layers are the IB ones, where a 1.2 Gb/s link per chip is required. As the chip occupancy decreases with the distance from the interaction point, a 400 Mb/s link per module is sufficient for the MB and OB layers. A custom block, named Data Transmission Unit (DTU) has thus been designed in order to provide the Alpide ASIC with the required output bandwidth. Table 1 summarizes the DTU requirements.

| Table 1. DTU serial link requirements. |
|----------------------------------------|
| Input clock                            | 40 MHz |
| Transmission clock                     | 600 MHz |
| Transmission type                      | Double Data Rate |
| Data encoding                          | 8b10b |
| Line/Data rate                         | 1.2/0.96 Gb/s (IB) |
| Line/Data rate                         | 400/320 Mb/s (MB and OB) |
| Electrical protocol                    | LVDS compatible |
| Technology                              | CIS 0.18 \( \mu \text{m} \) |
| TID (safety factor 5\( \times \) included) | 350 krad |

2 DTU design

The DTU schematic is shown in figure 2. It consists of three main components: a Double Data Rate (DDR) serializer, an output driver and a clock multiplication PLL. The DTU receives 3 data bytes every 25 ns which have already been encoded according to the 8b10b protocol (hence the 30 bits-wide input bus). The even and odd bits are loaded on two 15 bit serializers synchronized on the two phases of the 600 MHz clock. The two outputs are then fed to a multiplexer controlled by the same 600 MHz clock (in order to provide the DDR function) which is connected to the output driver. A second data path, delayed by half a clock cycle, drives a pre-emphasis driver connected in parallel to the main one. This second driver can provide extra current during bit transition in order to improve the switching time.

The 600 MHz clock is generated from the 40 MHz by a PLL. Albeit the two clocks are synchronous, the relative phase can potentially create metastability issues when the two shift registers are loaded. The load signal is thus generated from the 40 MHz clock with a programmable phase adjustment circuit, which allows to move the load signal in a position where the input data are stable.
2.1 PLL

The PLL, shown in figure 3, generates the 600 MHz clock from the 40 MHz master clock. It is based on the classical charge pump scheme [3]: the 40 MHz input clock is compared with an internally generated reference clock. The phase difference is used to control two switches connected to matched current sources. The current sources charge/discharge a main capacitor $C_1$. The voltage across the capacitor is used to control a Voltage Controlled Oscillator (VCO). The VCO output signal is divided by 15 and is used as reference clock to close the PLL loop. In lock condition, the input and the reference clock are forced to have the same frequency (40 MHz) and therefore the VCO frequency will be 15 times higher (i.e. 600 MHz).

![Figure 3. PLL simplified schematic.](image)

Resistor $R_1$ and capacitor $C_2$ are added for loop stability and VCO control voltage noise reduction, respectively.
The VCO is a ring oscillator based on the differential delay cell scheme proposed in [4]. The number of delay cells is programmable between 3 and 5, in order to compensate for PVT variations. The frequency divider is based on standard cells and is triplicated for Single Event Upset (SEU) protection.

2.2 Serializer

The serializer consists of two 15 bits standard cell based shift registers synchronized on the two 600 MHz clock edges, in order to obtain a 180° phase shift between the two serial data streams. An extra half clock cycle delay is added to drive the pre-emphasis driver.

The two registers load the input data every master clock period unless an enable signal is set to zero. It is possible to move the position of the load signal with respect to the 40 MHz clock in any of the 15 serializer clock pulses in the master clock period. If the load is disabled, the two shift registers provide a constant zero and a constant one value, respectively, thus resulting in a 600 MHz clock signal at the output. This feature can be useful to test the serial link.

All the registers are protected with Triple Modular Redundancy (TMR) in order to be tolerant to SEU.

2.3 Output driver

The output driver consists of two drivers: a main driver, with a current driving capability of 5 mA, and a pre-emphasis driver, with halved strength. The main driver, shown in figure 4, is based on a current source and a current sink with the same current, and 4 switches steering the current in one direction or the other through the external termination resistor. The output current can be changed between 0 and 5 mA in 312 μA steps via a 4 bit DAC.

![Driver schematic](image)

**Figure 4.** Driver schematic.

The output common mode is read via two probe resistors and compared with an internal common mode voltage reference. The difference is used to control a second current source for common mode voltage control [5]. The driver is compliant with the LVDS standard apart from the common mode voltage, which is set to 900 mV (i.e. half the supply voltage) to allow sufficient voltage headroom for the pMOS transistors.
The pre-emphasis driver is based on a similar scheme with halved current capabilities. The steering switches are 8 in order to implement an XOR logic function for the pre-emphasis [6]. Moreover, the common mode control loop is not present.

3 Test results

The DTU has been produced both as a test chip for standalone tests and integrated in the Alpide ASIC. Figure 5 shows the eye diagrams for a data rate of 1.25 Gb/s, an output current of 2.5 mA and a pre-emphasis of 0 and 50% obtained with an internally generated 30 bits fixed test pattern. The test pattern is set to Hex 35A58783 in order to have both short and long bit sequences and thus emulate a PRBS. The random and deterministic jitter are 11.4 ps and 48.8 ps in the first case and 10.9 ps and 52.8 ps in the second case. It can be observed that no bandwidth limitation comes from the output stage.

Figure 5. Eye diagram at 1.25 Gb/s and 2.5 mA output current. The pre-emphasis is set to 0 (left) and 1.25 mA (right). The eye widths (red arrows) are 0.822 (left) and 0.826 UI (right).

Figure 6 shows the DTU eye diagram at 1 Gb/s and 1.5 Gb/s. The deterministic jitter is 69.6 ps in the first case and 71.5 ps in the second one, while the random jitter is roughly the same as in previous case. Albeit the higher jitter, the eye diagram is still wide open. The degradation at higher rate is expected and it is clearly due to bandwidth limitation. On the other hand, the degradation at lower frequency is not fully understood but it is probably related to an increase of jitter in the PLL, since it can be observed also with a clock pattern as a test sequence.

Test results on the DTU integrated in the Alpide ASIC have shown similar performance of the high speed link when the Alpide is in idle mode. However, a significant increase in the noise (up to 5 times) has been observed when a large number of pixels are hit and read out. This has been correlated with a relatively weak power supply rejection of the PLL.

In the new ALPIDE chip (v4) the PLL supply has been separated from the digital one, skewing of the control signals has been introduced, and a few small modifications on the PLL itself have been implemented, which in general were aimed to improve the coupling between the node controlling the VCO and the power supply to improve the power supply rejection. These modifications include a filter capacitor on the VCO control line and better power routing, plus other minor layout changes. All this resulted in a significant improvement of the activity-induced jitter increase, which now only increases by a factor 2 instead of a factor 5 compared to the idle case. Further studies with external filtering capacitors closer to the DTU supply pads and with separate supply are ongoing.
Figure 6. Eye diagram at 2.5 mA output current with no pre-emphasis. The data rate is set to 1.063 Gb/s (left) and 1.5 Gb/s (right). The eye widths (red arrows) are 0.814 (left) and 0.789 UI (right).

4 Radiation test results

The DTU has been tested for radiation tolerance both with 30 MeV protons at NPI Prague and with a set of ions at INFN LNL, Legnaro.

In the proton test, the DTU test chip has been irradiated with a flux of $10^7$ protons cm$^{-2}$s$^{-1}$ for 1750 s. Neither PLL lock nor transmission error have been detected under these conditions. The flux has then been increased to $10^8$ protons cm$^{-2}$s$^{-1}$ for 6967 s, again without any error. The final dose after this first phase was 262 krads. The fluence and dose as a function of time are shown on the left part of figure 7.

Figure 7. Proton fluence and dose versus time for the proton test.

The flux has then been increased to $10^9$ protons cm$^{-2}$s$^{-1}$ for 7072 s, as shown on the right part of figure 7. In these conditions a Bit Error Rate (BER) of $1.4 \times 10^{-10}$ has been measured. However, only one PLL loss of lock has been observed, and the receiver was able to maintain the lock. A further increase of the flux to $10^{10}$ protons cm$^{-2}$s$^{-1}$ led to a chip failure. The final dose was 1.676 Mrad.
In order to disentangle the Total Ionizing Dose (TID) and SEU effects on the DTU performances a second test has been performed with ions. The DTU has thus been irradiated with 4 different ions at 3 angles, as described in table 2.

| Ion | Angle | LET [MeV cm$^2$/mg] |
|-----|-------|---------------------|
| 0   | 0°    | 2.88                |
| 0   | 20°   | 3.06                |
| 0   | 45°   | 4.07                |
| Si  | 0°    | 8.63                |
| Si  | 20°   | 9.18                |
| Si  | 45°   | 12.20               |
| Ni  | 0°    | 27.93               |
| Ni  | 20°   | 29.72               |
| Ni  | 45°   | 39.50               |
| Ag  | 0°    | 53.04               |

Table 2. List of used ions and angles.

Figure 8 left shows the SEU cross section for the PLL loss of lock as a function of the ion Linear Energy Transfer (LET), compared with the cross section for a standard D-type Flip Flop (DFF). A Weibull fit gives a LET$_{TH}$ of 3.9 MeV cm$^2$/mg for the DFF and ~ 9 MeV cm$^2$/mg for the PLL. This corresponds to an estimated loss of lock in the ITS layer 0 (108 DTUs) every 149 hours in the expected radiation levels foreseen for the ITS upgrade [7]. It should also be noted that only one of the 37 loss of lock events lead to a receiver synchronization failure. The PLL therefore shows an excellent SEU tolerance.

Figure 8 right shows the SEU cross section for the Bit Error Rate (BER) test. The Weibull fit give a LET$_{TH}$ of ~ 3 MeV cm$^2$/mg, which corresponds to a BER per link of $3.53 \times 10^{-14}$. This result is compatible with the result obtained with protons at low flux, which predicts a BER lower than $1.2 \times 10^{-13}$.

Figure 8. Ion irradiation results for the DTU prototype for DFF and PLL loss of lock (left) and for BER (right).
5 Conclusions

A 1.2 Gb/s Data Transmission Unit for the upgrade of the ALICE ITS has been designed in a CIS (CMOS Image Sensor) 0.18 $\mu$m technology and tested. The DTU consists of a PLL for clock multiplication, a DDR serializer and a pseudo-LVDS driver with pre-emphasis.

Electrical tests on the test chip show that the DTU fulfills the ITS upgrade requirement. Further tests on the full chip have shown a sensitivity of the DTU with respect to the chip activity. However, preliminary test results on a modified version show that with proper supply filtering the jitter can be kept under control.

Radiation tests shows a sufficient tolerance of the DTU for both total ionizing dose and single event upset aspects.

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