0.6 V, 116 nW Neural Spike Acquisition IC with Self-Biased Instrumentation Amplifier and Analog Spike Extraction

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Abstract: This paper presents an ultralow power 0.6 V 116 nW neural spike acquisition integrated circuit with analog spike extraction. To reduce power consumption, an ultralow power self-biased current-balanced instrumentation amplifier (IA) is proposed. The passive RC lowpass filter in the amplifier acts as both DC servo loop and self-bias circuit. The spike detector, based on an analog nonlinear energy operator consisting of a low-voltage open-loop differentiator and an open-loop gate-bulk input multiplier, is designed to emphasize the high frequency spike components nonlinearly. To reduce the spike detection error, the adjacent spike merger is also proposed. The proposed circuit achieves a low IA current consumption of 46.4 nA at 0.6 V, noise efficiency factor (NEF) of 1.81, the bandwidth from 102 Hz to 1.94 kHz, the input referred noise of 9.37 µVrms, and overall power consumption of 116 nW at 0.6 V. The proposed circuit can be used in the ultralow power spike pulses acquisition applications, including the neurofeedback systems on peripheral nerves with low neuron density.

Keywords: neural spike; instrumentation amplifier; analog nonlinear energy operator; spike detection

1. Introduction

Ultralow power consumption is highly required to avoid overheating surrounding tissues in many neuroprosthetic devices, as well as to operate the device for long term with limited power capacity under implanted condition [1]. In neural engineering of the central nervous system, using multi electrodes array, recording of the entire waveforms are required in order to classify the features from different neurons. However, in neurofeedback applications on peripheral nerves with low neuron density, the low supply voltage neural signal processing with only the spike features rather than dealing with the entire signal waveform can be a low power solution. The typical characteristics of the neural spikes are summarized in Table 1 [1–5].

The spikes are rare events in neural signal with 10–120 fires/s therefore, it is desirable to record only the spikes in order to reduce the power consumption while preserving the important information of the neuronal activities. To record the full waveform of the neurosignals, the amplifier with the acquisition bandwidth higher than the interested neural frequency range of typical 5–10 kHz is required. However, in the case of the spike extraction with the digital pulse train form, the required acquisition bandwidth can be reduced to near 1 kHz, considering the low firing rate of 10–120 fires/s. To record the low frequency neural signals, high power and area consumptions are required to reduce the flicker noises. In the spike pulse extraction, the required noise specifications also can be relaxed because the spike pulse information can be obtained with the high frequency components. The relaxed
noise and bandwidth specifications enables the ultralow power implementation of the neural spike extraction integrated circuit (IC).

| Interested Frequency Band | Typical Amplitude | Typical Firing Rate | Remark |
|--------------------------|-------------------|---------------------|--------|
| ASSCC 2014 [1]           | 300 Hz–10 kHz     | a few tens to several hundreds µV | 10–100 fires/s |
| TBCAS 2013 [2]           | 300 Hz–10 kHz     | 10 µV–1 mV          | - |
| EMBC 2013 [3]            | 300 Hz–5 kHz      | 50 µV–500 µV        | - |
| TNSRE 2009 [4]           | 100 Hz–10 kHz     | 50 µV–500 µV        | 10–120 fires/s | Duration of a few ms |
| JSSC 2007 [5]            | 300 Hz–5 kHz      | 50 µV–500 µV        | 10–100 fires/s | Duration of 250 µs |

Instrumentation amplifiers (IAs) are key building blocks of neural signal acquisition circuits. Specifically, the capacitively-coupled IA (CCIA) and current-balanced IA (CBIA) are widely used for low-power, and low-noise biopotential acquisition [6]. In addition, the CCIA has PVT-tolerant characteristics due to its feedback configuration, (i.e., the gain is determined by the ratio of input capacitors to feedback capacitors when the open-loop gain of the amplifier is sufficiently large). Although a recently proposed self-biased current-reuse scheme can reduce its power consumption [7], the inherent maximum bandwidth is limited by the frequency compensation for feedback stability. In contrast, the CBIA gain is mostly determined by the ratio of resistors and affected by the corner variations of the transistor parameters, including source and drain resistances. In addition, it has an open-loop operation, thus exhibiting a wider bandwidth without frequency compensation. We adopted the CBIA architecture to achieve the ultralow power consumption in the proposed IC.

The digital analysis of spike signals requires a high sampling rate of the analog-to-digital converter and presents a high-power consumption for signal processing. The typical action potentials have frequency components in the range from 100 Hz to 5 kHz, and appear up to 100 times per second. The minimum required sampling rate for these potentials is 10 kHz. Given that spikes appear sporadically in the time domain, this high-frequency sampling results in unnecessary power consumption. On the other hand, the nonlinear energy operator (NEO) is widely used to estimate the instantaneous frequency and amplitude of the signal, and it has been reported to be sensitive to signal discontinuity and superior to other energy estimators for detection in noisy signals [8–10]. In general, the NEO requires three analog building blocks, namely, a differentiator, a four-quadrant multiplier, and a difference amplifier. These building blocks allow to emphasize high-frequency components, such as spikes, and attenuates the low-frequency components. In addition, a threshold is usually applied on the nonlinearly emphasized output of the NEO, and the spike detection depends on threshold crossing. The threshold can be a scaled average of the NEO output using a lowpass filter (LPF). Given its simplicity, analog NEO-based spike extraction is a suitable and ultralow power solution [11].

In this paper, we propose an ultralow power neural spike acquisition IC with analog spike extraction supplied with 0.6 V. To reduce power consumption, we include a self-biased CBIA, which has a low current consumption and achieves a suitable noise efficiency factor (NEF). The passive RC LPF acts as both DC servo loop (DSL) and self-bias circuit. The ultralow power analog domain NEO composed of a low-voltage open-loop differentiator, and an open-loop gate-bulk input multiplier is designed to emphasize the high frequency spike components nonlinearly. The comparison threshold is generated by low-pass filtering the NEO output. To reduce the spike detection error by the NEO operation, the adjacent spike merger is also proposed. This paper is organized as follows: Section 2 details the design, operation principle, and circuit of the proposed ultralow power neural spike acquisition IC with analog spike extraction. Section 3 presents the fabricated IC and measurement results. Finally, conclusions and summary are described in Section 4.
2. Neural Spike Acquisition IC

Figure 1 shows the top-level block diagram of the proposed neural spike acquisition IC that is composed of input high pass filter (HPF), self-biased CBIA, analog NEO, comparator (CMP), and spike merger (SPIKE_MERGER) circuit. The neural input signal from electrodes, AINP and AINN, is high-pass filtered through pseudo-resistors with an adjustable corner frequency from 0.4 Hz to 115 Hz. To reduce power consumption, we designed the ultralow power IA (ULPIA) using two stage cascaded CBIA. In the CBIA, the RC LPF acts as DSL, and also provides self-biased operation.

The general continuous NEO is defined as

\[ \psi(x(t)) = \left( \frac{dx(t)}{dt} \right)^2 - x(t) \frac{d^2x(t)}{dt^2}, \]  

where \( x(t) \) is the input signal. Although the input HPF and DSL remove the low-frequency components, baseline fluctuations are still present in the output signal of the IA, between IA_OP and IA_ON. At the next stage, the analog NEO attenuates the low-frequency components and emphasizes the high-frequency spike-related components. Moreover, we designed the analog NEO to be reconfigurable into other energy operator schemes as shown in Figure 2.

The TH_GEN generates the threshold voltage for spike detection, whose level is compared with the NEO output at the comparator. The comparator output usually includes adjacent multiple pulses driven from the nonlinear operation of the NEO corresponding to one neural spike. Such multiple pulses cannot be eliminated perfectly by using a hysteresis comparator. Hysteresis can undermine the spike detection sensitivity. Therefore, we designed an adjacent spike merger circuit, which merges the adjacent spikes within a predefined time window. In the adjacent spike merger circuit, a counting clock with 6.75 kHz is used, and the merging window is programmable from 0.30 ms to 2.37 ms. Assuming the rare firing rate of typically less than 120 fires/s in neural spike activity, the merging window of the proposed spike merger circuit is shorter than the spike firing periods. Thus, the spiker merger can effectively reduce the detection error of the analog NEO.
2.1. Ultralow Power Self-Biased CBIA

The circuit diagram of proposed ultralow power self-biased CBIA is shown in Figure 3. The input signals are high-pass filtered using the input HPF, as shown in Figure 3a, and the filtered signals are amplified by the CBIA, as shown in Figure 3b. Figure 3c shows the implementation of the pseudo-resistors array. In Figure 3b, the input transistor pair, PM3 and PM4, constitutes source followers, and thus the voltage across \( R_{\text{LPF}} \) becomes the buffered copy of the differential input voltage between INP and INN. The CBIA is designed using the medium threshold voltage (Vth) transistors, which have lower Vth than the normal Vth transistors in typical 0.18 \( \mu \)m process. The PM3 and PM4 have the operation points of \(|V_{\text{GS}}| = 223 \text{ mV}, |V_{\text{th}}| = 132 \text{ mV}, |V_{\text{DS}}| = 250 \text{ mV}\), and are operated in the saturation region. The voltage difference across \( R_{\text{IN}} \) results in the current difference of PM3 and PM4. Therefore, the differential output voltage between OUTP and OUTN is determined by the multiplication of this current difference and output resistance \( R_{\text{OUT}} \), which is implemented using the adjustable pseudo-resistor. The gain of the IA is proportional to the ratio between resistors \( R_{\text{IN}} \) and \( R_{\text{OUT}} \). The central node between the two pseudo-resistors \( R_{\text{OUT}} \) is connected to gate of n-type metal oxide semiconductor (NMOS) loads NM1 and NM2 to form a resistive common-mode feedback.

Adjustable pseudo-resistors \( R_{\text{LPF}} \) and metal–insulator–metal (MIM) capacitors \( C_{\text{LPF}} \) form the passive LPF, whose output is connected to the gates of PMOS current sources PM1 and PM2. Therefore, the low-frequency components of the output signals are negatively returned using this feedback loop, and the IA can be operated in self-bias mode. In this system, the input HPF rejects the DC components of the input signal. The negative feedback of passive LPF using \( R_{\text{LPF}} \) and \( C_{\text{LPF}} \) forms DSL, and the additional HPF characteristics can be obtained. Given that the DC gain of the passive LPF is unity, the DC rejection performance of this DSL is worse than that using active Miller integrators. However, this DSL does not consume additional power. Moreover, the gate bias voltages of PM1 and PM2 are provided by the LPF, and the IA can be operated in the self-biased mode. The DC bias current of both NM1 and NM2 is 11.6 nA, and the IA current consumption is 23.2 nA with supply voltage of 0.6 V. To achieve adequate amplification gain, two IAs are cascaded. The design values of the CBIA are summarized in Table 2.
Figure 3. Ultralow-power self-biased current-balanced IA (CBIA): (a) Input passive HPF (programmable from 0.23 Hz to 185 Hz); (b) CBIA; (c) Pseudo resistors array.

Table 2. Design values of CBIA.

| Devices            | Value                                      |
|--------------------|--------------------------------------------|
| PM1, PM2           | W/L = 8 μ/10 μ                             |
| PM3, PM4           | W/L = 30 μ/5 μ                             |
| NM1, NM2           | W/L = 0.5 μ/30 μ                           |
| $R_{\text{IN}}$    | 35 kΩ                                      |
| $R_{\text{OUT}}$   | 4-bit binary-weighted (LSB unit: W/L = 4 μ/1 μ, approx. 20 MOhm) |
| $R_{\text{LPF}}$   | 2-bit binary-weighted (LSB unit: W/L = 0.5 μ/10 μ, approx. 900 MOhm) |
| $C_{\text{LPF}}$   | 17.9 pF                                    |
2.2. Analog NEO-Based Spike Extraction

The NEO is known to outperform other spike extraction methods in conditions such as low SNR [9–11]. Therefore, we implemented the spike detector based on the NEO using an open-loop differentiator and a subthreshold four-quadrant multiplier, also with supply voltage of 0.6 V. The open-loop configuration of the differentiator (differentiator (DIFF) in Figure 2) and the gate-bulk input scheme of the multiplier (multiplier (MUL) in Figure 2) are based on the design in [11]. The open-loop differentiator and its common-mode feedback circuit are illustrated in Figure 4a,b, respectively. The differentiator does not require an operational amplifier and can achieve a low current consumption of 53 nA including the feedback circuit. The differentiator gain can be expressed as

\[ A(s) = A_o \frac{sC_{DIFF}}{1 + sC_{DIFF} \left( \frac{r_{op4}}{r_{op6}} + \frac{1}{g_{mp5}} \right) \left( \frac{r_{on2}}{r_{op5}} \right) \left( \frac{1}{r_{oCS}} \right) \left( \frac{r_{op4}}{r_{op6}} \right)}, \]  

(2)

where

\[ A_o = g_{mn2} g_{mp6} \left( \frac{r_{on2}}{r_{op4}} \right) \left( \frac{1}{g_{mp5}} \right) \left( \frac{1}{r_{oCS}} \right) \left( \frac{r_{op4}}{r_{op6}} \right), \]  

(3)

and the \( r_{oCS} \) is the output resistance of the 5.8 nA current source. The zero of the transfer function is at the origin, and the input signal is differentiated before the dominant pole. The design values of the differentiator are summarized in Table 3.

Figure 4. Open-loop differentiator: (a) Core and (b) common-mode feedback.
Table 3. Design values of differentiator.

| Devices          | Value                          |
|------------------|--------------------------------|
| PM1, PM2, PM5, PM6 | W/L = 0.5 μ/10 μ              |
| PM3, PM4         | W/L = 0.5 μ/30 μ               |
| NM1, NM2         | W/L = 1 μ/10 μ                 |
| NM3, NM4         | W/L = 2 μ/30 μ                 |
| C_DIFF           | 8.95 pF                       |
| PM7, PM8         | W/L = 1 μ/10 μ                 |
| PM9              | W/L = 5 μ/10 μ                 |
| NM5, NM6, NM7, NM8 | W/L = 2 μ/5 μ                |

Figure 5 shows the design of the subthreshold four-quadrant multiplier that uses a crossed-coupled quad structure, where differential multiplication is obtained by driving the gate and bulk of the four PMOS transistors, PM1, PM2, PM3, and PM4, which operate in the subthreshold region, and whose output current can be approximated to a first-order equation given by

\[ I_{OUT} = (I_3 + I_4) - (I_1 + I_2) \propto V_1 \cdot V_2. \] (4)

The multiplier current consumption is 71.6 nA. The design values of the multiplier are summarized in Table 4.

Figure 5. Subthreshold four-quadrant multiplier using gate and bulk input.

Table 4. Design values of multiplier.

| Devices          | Value                          |
|------------------|--------------------------------|
| PM1, PM2, PM3, PM4 | W/L = 5 μ/10 μ                |
| PM5, PM6         | W/L = 1 μ/10 μ                 |
| NM1, NM2, NM3, NM4 | W/L = 0.5 μ/30 μ              |

The threshold voltage (COMP_TH) for the comparator input is generated in the TH_GEN block as shown in Figure 6. The threshold voltage can be selected among NEO_OUT_LPF, COMP_TH_UP, COMP_TH_DN, and COMP_TH_STATIC. The static threshold (COMP_TH_STATIC) is generated from the voltage digital-to-analog converter. The low pass filtered signal (NEO_OUT_LPF) from the NEO output (NEO_OUT) is fed to the analog level shifter (source follower). In the case of positive spike detection, the low pass filtered signal (NEO_OUT_LPF) should be down-shifted to COMP_TH_DN. In the case of negative spike detection, the low pass filtered signal (NEO_OUT_LPF) should be up-shifted to COMP_TH_UP.
The simulation results of the spike detection with typical neural input signals are shown in Figure 7. The neural inputs, between INP and INN, include the baseline components and the spike components. The baseline components are sinusoidal with the frequency of 40 Hz and the amplitude of 500 µVpk. The spike pulse components are triangular with the bottom pulse width of 100 µs, peak amplitude of 400 µV, and firing rate of 100 Hz. In the simulation, the full spike detection chain path from input HPF, ULPIA, NEO, and the TH_GEN is included. The transient noise simulation is performed with the noise bandwidth from 0.1 Hz to 100 kHz. The simulation results show that the typical neural spikes can be detected properly under baseline fluctuation.

![Threshold generator (TH_GEN) circuit diagram.](image)

**Figure 6.** Threshold generator (TH_GEN) circuit diagram.

![Transient noise simulation results of spike detection.](image)

**Figure 7.** Transient noise simulation results of spike detection.

The NEO output usually includes adjacent multiple spikes responsive to one neural spike input. In the proposed design, we remove such glitches by merging adjacent spikes within very short intervals that contain them. Figure 8a,b show the circuit diagram and typical timing diagram of the adjacent spike merger.
In the adjacent spike merger circuit, a counting clock (CLK) with 6.75 kHz is used, and the spike merging window can be programmable from 2 CLK to 16 CLK (0.30 ms to 2.37 ms). Assuming the rare firing rate of typically less than 120 fires/s in neural spike activity, the merging window of the proposed spike merger circuit is shorter than the spike firing periods. Thus, the spike merger can effectively reduce the detection error of the analog NEO. As shown in Figure 8b, the adjacent spike merger circuit maintains signal SPIKE_OUT at the high level during merging window length after the rising edge of comparator input COMP_IN. The adjacent spikes within typical 8 CLK periods (1.19 ms) are merged to eliminate glitches.

3. Measurement Results

The die photo of the proposed neural spike acquisition IC is shown in Figure 9. We fabricated the IC using the standard 0.18 μm complementary metal oxide semiconductor (CMOS) process, obtaining a chip of 470 μm × 2600 μm. The power breakdown of the IC is shown in Table 5. The supply current of the ULPIA using the 2-stage CBIA is 46.4 nA, and the total supply current of the IC is 193.3 nA with 0.6 V power supply.

Figure 8. Adjacent spike merger circuit: (a) Circuit diagram and (b) timing diagram illustrating spike merging.

Figure 9. Die photo of the proposed neural spike acquisition IC.
Table 5. Power consumption of IC.

| Sub-Block                      | Current (nA) |
|--------------------------------|--------------|
| ULPIA using 2-stage CBIA       | 23.2 × 2 = 46.4 |
| Differentiator                 | 53.0         |
| Multiplier                     | 71.6         |
| Threshold generator            | 7.2          |
| Comparator                     | 9.8          |
| etc                            | 5.3          |
| Total                          | 193.3        |

The measured transfer function and the input referred noise of the IA are shown in Figure 10a,b, respectively. The adjustable high-pass corner frequency from 0.23 Hz and 185 Hz exhibits a default gain of 48.2 dB, with a lowpass corner frequency of 1461 Hz. The input referred noise is 9.37 μVrms from 102 Hz to 1941 Hz. The current consumption of the IA is 46.4 nA at 0.6 V, and the NEF is 1.81.

![Figure 10a](image1)  
![Figure 10b](image2)

**Figure 10.** Instrumentation amplifier (IA) measurement results: (a) Transfer function with adjustable corner frequency and (b) input referred noise.
Figure 11a shows the spike detection results with an input spike amplitude of 400 $\mu$V$_{pk}$ and intervals at 100 Hz. The spikes are properly detected, and the successful operation of the spike merger circuit is illustrated in Figure 10b. The digital signals of COMP_OUT and SPIKE_OUT are level-shifted from 0.6 V to 1.8 V for the purpose of monitoring. The typical merging window of the spike merger circuit is 1.19 ms (=840 Hz), and the high-pass corner frequency of the IA is 1461 Hz. Therefore, the maximum detectable firing rate of the input spike is limited to 840 Hz by the spike merger circuit. Because the maximum detectable firing rate is higher than the typical firing rate 120 fires/s in neural spike activity, the typical spikes can be detected properly.

Figure 11. Processing of 400 $\mu$V and 100 Hz spikes: (a) Spike extraction and (b) glitch removal.
Table 6 shows a performance comparison of the proposed IC to previous developments [1,7,12–16]. The NEF is commonly used to evaluate the efficiency in the noise-power tradeoff, and is defined as [7]

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{total}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (5)$$

The IC shows the ultralow power consumption and good NEF and $NEF \cdot VDD^2$. To achieve the ultralow power consumption, the input referred noise and the highpass corner frequency are increased, and the low lowpass corner frequency is decreased. In the point of view of the full waveform neural recording, the noise and bandwidth performances of the IC are not sufficient. In the point of the spike extraction applications, this IC achieves the ultralow power spike pulses acquisition with sacrificing the noise and bandwidth performance.

Table 6. Performance comparison.

| Process (µm) | Supply voltage (V) | IA power (µW) | Total power/ channel (µW) | Highpass corner freq. (Hz) | Lowpass corner freq. (Hz) | IRN (µVrms) | NEF | NEF $\cdot VDD^2$ |
|------------|-------------------|---------------|--------------------------|---------------------------|--------------------------|-------------|-----|------------------|
| TBCAS 2009 12 | 0.18            | 1.2           | 23.6                     | 100                       | 9.2 k                    | 5.4      | 4.9  | 44.05            |
| TBCAS 2012 13 | 0.13            | 1.1           | 1.92                     | 11.5–167                  | 4.8–9.8 k                | 3.8      | 4.0  | 44.05            |
| EL 2012 14   | 0.18            | 0.8           | 0.8                      | 0.2–430                   | 5.8 k                    | 5.71     | 5.7  | 44.05            |
| TBCAS 2014 7  | 0.35            | 2.5           | 0.0825                   | 0.005–200                 | 0.1/10 k                 | 2.8      | 2.6  | 44.05            |
| ASSCC 2014 1  | 0.18            | 0.5           | 1.25                     | 102                       | 10k                      | 5.4      | 5.4  | 44.05            |
| TCAS-II 2016 15 | 0.18           | 1.25          | 56                      | 0.1/10 k                  | 7k                       | 4.5      | 4.5  | 44.05            |
| TBCAS 2017 16 | 0.18            | 0.6           | 0.116                    | 102 (programmable, 0.23/53.1/76.7/102/165) | 1.94 k                  | 4.57     | 4.57  | 44.05            |

4. Conclusions

This paper presents an ultralow power neural spike acquisition IC with analog spike extraction. We fabricated the IC using the standard 0.18 µm CMOS process, obtaining a circuit of 470 µm $\times$ 2600 µm. The passive RC LPF in the CBIA acts as both DSL and self-bias. The ULPIA is implemented using the cascaded two self-biased CBIA. The ULPIA has a low current consumption of 46.4 nA at 0.6 V, NEF of 1.81, the bandwidth from 102 Hz to 1.94 kHz, and the input referred noise of 9.37 µVrms. In addition, we integrated a spike detector based on an analog NEO using a low-voltage open-loop differentiator and a gate-bulk input multiplier, and removed erroneous glitches using the adjacent spike removal circuit. Overall, the proposed IC achieves the ultralow power spike detection performance.

Author Contributions: J.P.K. is the first author, implemented the circuit blocks and designed the top architecture of the IC. H.L. is the second author, designed the sub-blocks including digital blocks. H.K. is the corresponding author, and he designed the analog sub-blocks of the IC.

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References

1. Kim, S.; Liu, L.; Yao, L.; Goh, W.; Gao, Y.; Je, M. A 0.5-V sub-µW/channel neural recording IC with delta-modulation-based spike detection. In Proceedings of the 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), Kaohsiung, Taiwan, 10–12 November 2014; pp. 189–192.

2. Han, D.; Zheng, Y.; Rajkumar, R.; Dawe, G.; Je, M. A 0.45 V 100-Channel Neural-Recording IC with Sub-µW Channel Consumption in 0.18 µm CMOS. IEEE Trans. Biomed. Circuits Syst. 2013, 7, 735–746. [PubMed]

3. Liu, L.; Yao, L.; Zou, X.; Goh, W.; Je, M. Neural recording front-end IC using action potential detection and analog buffer with digital delay for data compression. In Proceedings of the 2013 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Osaka, Japan, 3–7 July 2013; pp. 747–750.

4. Gosselin, B.; Mohamad, S. An ultra low-power CMOS automatic action potential detector. IEEE Trans. Neural. Syst. Rehabil. Eng. 2009, 17, 346–353. [CrossRef] [PubMed]

5. Harrison, R.; Watkins, P.; Kier, R.; Lovejoy, R.; Black, D.; Greger, B.; Solzbacher, F. A low-power integrated circuit for a wireless 100-electrode neural recording system. IEEE J. Solid-State Circuits 2007, 42, 123–133. [CrossRef]

6. Van Helleputte, N.; Konijnenburg, M.; Pettine, J.; Jee, D.; Kim, H.; Morgado, A.; van Wegberg, R.; Torfs, T.; Mohan, R.; Breeschoten, A.; et al. A 345 µW multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction, and integrated DSP. IEEE J. Solid-State Circuits 2015, 50, 230–244. [CrossRef]

7. Wang, T.Y.; Lai, M.R.; Twigg, C.M.; Peng, S.Y. A fully reconfigurable low-noise biopotential sensing amplifier with 1.96 noise efficiency factor. IEEE Trans. Biomed. Circuits Syst. 2014, 8, 411–422. [CrossRef] [PubMed]

8. Yang, Y.; Boling, C.S.; Kamboh, A.M.; Mason, A.J. Adaptive threshold neural spike detector using stationary wavelet transform in CMOS. IEEE Trans. Neural Syst. Rehabil. Eng. 2015, 23, 946–995. [CrossRef] [PubMed]

9. Mukhopadhyay, S.; Ray, G.C. A new interpretation of nonlinear energy operator and its efficacy in spike detection. IEEE Trans. Biomed. Eng. 1998, 45, 180–187. [CrossRef] [PubMed]

10. Semmaoui, H.; Drolet, J.; Lakhssassi, A.; Sawan, M. Setting adaptive spike detection threshold for smoothed TEO based on robust statistics theory. IEEE Trans. Biomed. Eng. 2012, 59, 474–482. [CrossRef] [PubMed]

11. Cao, W.; Li, H. Ultra-low-power neural recording microsystem for implantable brain machine interface. In Proceedings of the IEEE International Conference on Green Computing and Communications and IEEE Internet of Things and IEEE Cyber, Physical and Social Computing, Beijing, China, 20–23 August 2013; pp. 1050–1053.

12. Gosselin, B.; Ayoub, A.E.; Roy, J.F.; Sawan, M.; Lepore, F.; Chaudhuri, A.; Guitton, D. A Mixed-Signal Multichip Neural Recording Interface with Bandwidth Reduction. IEEE Trans. Biomed. Circuits Syst. 2009, 3, 129–141. [CrossRef] [PubMed]

13. Rodriguez-Perez, A.; Ruiz-Amaya, J.; Delgado-Restituto, M.; Rodriguez-Vazquez, A. A Low-Power Programmable Neural Spike Detection Channel with Embedded Calibration and Data Compression. IEEE Trans. Biomed. Circuits Syst. 2012, 6, 87–100. [CrossRef] [PubMed]

14. Liu, L.; Zou, X.; Goh, W.L.; Ramamoorthy, R.; Dawe, G.; Je, M. 800 nW 43 nV/√Hz neural recording amplifier with enhanced noise efficiency factor. Electron. Lett. 2012, 48, 479–480. [CrossRef]

15. Wu, J.; Law, M.K.; Mak, P.I.; Martins, R.P. A 2-µW 45-nV/√Hz readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudofeedback DC servo loop. IEEE Trans. Circuits Syst. II Exp. Briefs 2016, 63, 351–355. [CrossRef]

16. Liu, X.; Zhang, M.; Richardson, A.G.; Lucas, T.H.; Van der Spiegel, J. Design of a closed-loop, bidirectional brain machine interface system with energy efficient neural feature extraction and PID control. IEEE Trans. Biomed. Circuits Syst. 2017, 11, 729–742. [CrossRef] [PubMed]