Gated silicon nanowire for thermo-electric power generation and temperature sensing

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Abstract
Gate-all-around Si FETs are predicted to be the future of integrated CMOS circuits (ICs). The reduction in size of the Si channel, surrounded by oxide and a gate causes increased self-heating effects due to a reduction in thermal conductivity of the Si channel. Although, this degrades performance, we demonstrate that this can be exploited for localized thermoelectric power generation and temperature sensing that help reduce energy waste and increase IC lifetime. We show, using Sentaurus TCAD simulations, that unbiased gated intrinsic Si nanowires (NWs) can generate 2.2 times higher output power than doped NWs by choosing the correct metal gate work function. In addition, the voltage on the gate of the NW can be used to sense the temperature at the hot-spot in gate-all-around ICs. Among the studied gated NWs, the double gated structure with 30 nm gate length shows higher sensitivity to the change of temperature.

Keywords: carrier modulation, thermo-electric power generation, temperature sensing, undoped thermo-electric material

(Some figures may appear in colour only in the online journal)

1. Introduction

Aggressive downscaling of the gate length of Si FETs has led to novel devices such as gate-all-around FETs [1–4] and nanosheet (NS) FETs [5–7]. Simultaneously, nano-structuration of Si bulk was shown to improve its thermoelectric characteristics [8–11]. The reduction in thermal conductivity in nanostructured Si leads to increased hot-spot temperatures (as high as 353 K) in nanowire (NW)-based FETs but also increased thermoelectric performance of Si NWs [12–14]. These seemingly conflicting findings can be exploited for heat sensing and thermal management in integrated circuits (ICs) that are based on NW/NS (NW/NS) devices. In thermo-electric materials (TEMs), the Seebeck effect is used for thermo-electric power generation [15] and temperature sensing [16–18]. The Seebeck coefficient, $S$ is defined as $S = \frac{\Delta V}{\Delta T}$ (1) with $\Delta T$ the temperature difference and $\Delta V$ the voltage due to $\Delta T$. Ideally, low thermal, $\kappa$ and high electrical, $\sigma$ conductivity are required to preserve $\Delta T$ and high conduction of carriers, respectively [15]. The figure of merit ($ZT$) evaluates the performance of TEMs by correlating thermal and electrical properties [21]:

$$ZT = \frac{\sigma S^2 T}{\kappa}. \quad (2)$$

As seen in equation (2), high $ZT$ can be achieved when the thermo-electric power factor ($\sigma S^2$) is high and thermal...
conductivity is low. In bulk TEMs, optimization of $ZT$ is challenging due to the Wiedemann–Franz law [19, 22]. Shrinking TEMs to nanoscale partially de-couples the electrical and thermal properties and resolves this bottleneck. $\kappa$ reduces significantly due to increasing boundary scattering and phonon confinement [8–10]. Conventionally, optimizing the doping concentration maximizes $\sigma S^2$ [23]. However, increased doping leads to increased impurity scattering [24]. Significant improvement in $\sigma S^2$ has been reported via modulation doping [24], applying a gate voltage on gated TEMs [25–29], or generation of a strong internal electric field ($E_{int}$) as the result of core/shell structures [30–33]. Reproducibility and precision of doping profiles become challenging as NWs are downscaled [34] while applying a gate voltage requires additional circuitry and power. Previously, $E_{int}$ at interfaces of i-Ge (core)/i-Si (shell) [33] and i-GaN (core)/i-AlN (shell)/i-Al GaN (shell) [32] structures have led to accumulation of holes and electrons in the core respectively, where $i$ stands for intrinsic. However, one has to find an approach to accumulate carriers on a dopant-free abundant material with low-cost fabrication processes, like Si [9]. In our previous work [35], the effect of gate length and applying gate voltage on thermo-electric properties of NiSi$_2$/n-Si/NiSi$_2$ core structure with Schottky–Ohmic and Ohmic–Ohmic contacts were studied. In the mentioned paper, carrier density optimisation is mainly achieved by applying a voltage to the Ti gate. In this work, we present an alternative method to optimize $\sigma S^2$ in Si NWs and evaluate its implementation for both power generation as well as temperature sensing. TCAD simulations [36] are conducted to study the effect of using an appropriate gate metal work function to modulate the carrier concentration across an intrinsic silicon NW. We use Sentaurus TCAD’s ability to simulate circuits around novel semiconductor device structures, together with its electrical and thermal simulation abilities.

2. Simulation models

Accurate modelling of the thermoelectric performance of nano-devices can be done by choosing appropriate models available in Sentaurus TCAD. The hydrodynamic model is used to simulate coupled thermo-electrical transport that allows carrier temperature to diverge from lattice temperature. In addition, we have used PhuMob, Enormal, and HighFieldSat models to simulate effects of lattice temperature, acceptor concentration, donor concentration, electron–hole scattering, acoustic phonon scattering, surface roughness scattering, and high field saturation on the overall mobility. The Boltzmann statistics for carrier density, and a lattice temperature-dependent model for the effective density of states are implemented [36]. The lattice thermal conductivity of Si ($\kappa_{Si}$) as a function of Si diameter ($d_{Si}$) is extracted from [10] and the thermal conductivity of SiO$_2$ is kept constant at $\kappa_{SiO2} = 0.014$ W (cm K)$^{-1}$ [37]. Carrier thermal conductivities are computed within the hydrodynamic model.

The hydrodynamic model was developed for studying electrical and thermal properties of sub-micron devices [36]. The equations were evaluated against experimental results [36, 38–41]. Their validity for thermo-electric simulations has been investigated in different contexts. For instance, Myeong et al [42] used the hydrodynamic model in Sentaurus TCAD to analyse self-heating effects in vertical FinFETs with a rectangular cross section of 6 nm $\times$ 46 nm. Comparison between simulations and measurements in [42] shows that the ‘Hydrodynamic model well describes the thermal characteristics in the current equation’. In addition, Weber et al [34] also demonstrate a good fit between simulation and experimental result of a NW with 20 nm Si thickness. Their simulation results show radial dependence of the mobility of a Si NW with 12 nm cross section. Weber et al [34] states ‘this confirms that mobility is highest in the centre of the NW’. In our study, we have used hydrodynamic model and different temperature dependent material modules to study thermoelectric properties of NWs with comparable dimensions as in these references. Therefore, we assume that the validity of the models used in this work can be seen in to [34, 42, 43].

3. Thermo-electric power generation

Carrier modulation and its effect on the generated power are studied by tuning the work function of the metal gate ($\phi_m$) wrapped around an undoped Si NW with circular cross section. This approach is similar to threshold voltage tuning in MOSFETs as the energy bands bend due to the work function difference between the metal gate and the Si, leading to accumulation/depletion of charges. The cross section of the structure and metal/SiO$_2$/Si band diagram is shown in figure 1. The Si NW length and the thickness of the SiO$_2$ wrapping ($d_{SiO2}$) are 220 nm and 8 nm, respectively, and are kept constant. The diameter of the Si NW ($d_{Si}$) varies in this investigation. The contacts are Al with work function $\phi_{Al} = 4.1$ eV, within the range of 4.06 eV–4.28 eV reported in [43]. The work function of the metal gate is varied between 3.7 eV $\leq \phi_m \leq 4.2$ eV. All metal layers are defined as surfaces without thickness. The temperature gradient ($\Delta T$) is imposed by having a hot source $T_h$ and cold sink $T_c = 300$ K as shown in figure 1.

Figure 2 shows the influence of $\phi_m$ on the carrier density and mobility. Figures 2(a) and (b) illustrate the non-homogeneous variation of these parameters in the cross section of the NW. This is different to homogenous doping and will lead to non-homogeneous power generation across the cross section of the NW. Therefore, equation (2) is no longer a representative quality factor for these structures.

Figures 2(c) and (d) give the variation of the carrier density and mobility as a function of $\phi_m$ as well as $d_{Si}$. As expected, increasing $\phi_m$ decreases the electron concentration at the interface and increases the mobility, while higher carrier concentration (lower mobility) is achieved for smaller $d_{Si}$. The mobility degradation is a consequence of the internal electric field perpendicular to the SiO$_2$ interface.
The non-homogeneous electron concentration ($n_e$) in the cross-sectional area of the NW (figure 2(c)) leads to a non-homogenous Seebeck coefficient ($S$) across the NW. $S$ is highest at the core (C), and reaches a minimum at the interface, showing the expected inverse proportionality between $n_e$ and $S$. This relation is also seen in the variation of the average value of $<n_e>$ and $<S>$ as a function of NW diameter and metal gate work function (see figure 3(a)). For smaller diameters the modulation effect increases $<n_e>$ and thus decreases $<S>$. This leads to a maximum in power factor (see figure 3(b)), especially apparent for the narrow NW. The voltage difference ($\Delta V$) and generated current ($I_g$) obtained for a temperature difference of $\Delta T = 15$ K shows a relationship consistent with the variation of $<S>$ and $<n_e>$ with NW diameter (see figure 3(c)).

The maximum output power, $P_{\text{max}}$, is simulated by varying the load resistance to determine the point where $R = R_L$. This point will be different for each GAA NW implementation as the variation of $\phi_m$ modulates both the carrier concentration as well as the mobility non-linearly. Simulations of power density as a function of $\phi_m$ are done for $T_H - T_C = \Delta T = 15$ K. Figure 4 shows the results for three values of $d_{Si}$: 12, 37 and 62 nm. To illustrate the impact of scattering processes, simulations are done with and without the mobility scattering model and are also compared to the performance of the doped NW with different doping levels. In figure 4(a) we investigate the influence of $\phi_m$ for $d_{Si} = 12$ nm and $d_{ox} = 8$ nm. This confirms an optimum is achieved at $\phi_m \approx 4.1$ eV. Comparison with the simulations without scattering degradation shows that the scattering processes decrease $P_{\text{max}}$ by 32%.

Power density for higher $d_{Si}$ is achieved for lower $\phi_m$, as the optimal carrier concentration is achieved for lower $\phi_m$ as shown in figure 3(b). Figure 4(b) shows that mobility degradation in doped NWs causes a decrease of power density by 74%, compared to gated NWs. The interface mobility of the gated structure with $\phi_m = 4.1$ eV ($n_e = 1.03 \times 10^{18}$ cm$^{-3}$ at the interface) is 2.44 times larger than the doped NW with similar concentration. Consequently, power density for gated NWs ($d_{Si} = 12$ nm) is 2.20 times larger than the doped structure ($d_{Si} = 12$ nm). Within the range of simulated NW diameters, we find that higher diameters lead to higher $P_{\text{max}}$ where of constant and steady temperature difference is present. However, at the instance (time = 0 s) that the heat source is lost, higher thermal conductivity of larger diameters, reduces the time that $\Delta T$ is preserved. Figure 5 shows the response of power and $\Delta T$ to complete heat source loss at time = 0 s, while $T_C$ is set to a fixed temperature ($=300$ K) in the simulation. Time taken for the gated thermo-electric power generator with $d_{Si} = 12$ nm to lose 14 K of temperature difference is 76% and 88% more than $d_{Si} = 37$ nm and 62 nm, respectively (figure 5(b)). Figure 5(a) shows longer energy harvesting time for NWs with lower diameter.

Figure 1. (a) Front view, and (b) cross section of a gate all around (GAA) thermoelectric power generator. (c) Schematic energy band diagram along the dashed line in (b) for $\phi_{Si} > \phi_m$ giving accumulation of electrons.

Figure 2. (a) Electron density ($n_e$) and (b) electron mobility ($\mu_e$) of an intrinsic GAA NW with $d_{Si} = 12$ nm and $d_{ox} = 8$ nm. Both for the cross section midway between the contacts. (c) Electron density, and (d) electron mobility as a function of metal work function ($\phi_m$) and NW diameter, $d_{Si}$, with $d_{ox} = 8$ nm. All at $\Delta T = 0$ K. Labelling: int refers to the interface and C to the middle of the NW.
Comparing the performance of a GAA to a \(\Omega\)-gated NW \[44\] for \(\phi_m = 4.1\) eV, \(d_{ox} = 8\) nm and \(\Delta T = 15\) K gives an output power for the \(\Omega\)-gated NW 0.09%, 3.47% and 4.30% smaller than that of the GAA NW with \(d_{Si} = 12\) nm, 37 nm, and 62 nm respectively. This is because the bottom part of the semi-covered channel in \(\Omega\)-gated NW is away from the metal gate.

The effect of interface trapped charge \((Q_i)\) and fixed charge \((Q_f)\) has been extensively studied in \[45–47\]. Amongst these two charges, \(Q_i\) has a considerable effect on carrier concentration across the NW. A typical density range is \(10^{10} < D_{it} < 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}\) \[45\]. Simulations (figure 6) show a sharp decrease in \(P_{\text{max}}\) for \(D_{it} \geq 2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}\). However, if a work function of \(\phi_m = 3.9\) eV is used rather than 4.1 eV, then the maximum output recovers at the value of \(D_{it} \approx 8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}\).
at this voltage results in equal output power to the case when
the optimized carrier concentration. The carrier concentration
is most sensitive to the meter of the most sensitive to
meter of $D_{\text{ox}}$ applying a gate voltage ($\Delta V_{\text{G}}$ is 4.1 eV and 3.9 eV work functions, respectively. $\Delta V_{\text{G}}$ is set to $\phi_m = 4.1$ eV and $D_{\text{it}} = 0$ cm$^{-2}$eV$^{-1}$ for all simulations in this section. The gap between the gates is 10 nm. $V_{\text{PG}} = 0$ V at all times, while $V_{\text{CG}}$ is varied. $T_h = \text{variable}$ and $T_c = 300$ K, setting up a variable temperature difference $\Delta T$. The simulations are set up in the same way as in section 2. The variation of the conduction band as a function of control gate lengths ($L_{\text{CG}}$) is shown in figure 7(b) for different values of $V_{\text{CG}}$. A potential barrier ($\phi_B$) is generated between the two Al contacts by the work function difference between the Si NW and the gate metal. Applying a $V_{\text{CG}}$ in DG (or SG) GAA NWs, tunes the height of $\phi_B$ and thus controls the current that can flow through the channel. Since the DG structure is conducting electrons at $V_{\text{CG}} = 0$ V, a negative $V_{\text{CG}}$ will decrease the electron flow as it increases the potential barrier. When $T_h$ is increasing, the density of carriers at energy levels higher than $\phi_B$ increases, increasing the current, $I_g$. Temperature, $T_h$ sensing can be done in either two steps for higher accuracy, or a single step. $T_h$ can be sensed by, (a) using the linear relation between $I_g$ and $T_h$ at $V_{\text{CG}} = 0$ V for DG (SG) (figure 8(a)), and (or) (b) by adapting $V_{\text{CG}}$ to keep $I_g$ constant and equal to $I_{\text{gref}}$ under changing $T_h$, where $I_{\text{gref}}$ is the constant reference current. The value of $V_{\text{CG}}$ to maintain $I_{\text{gref}}$ is then the reading of $T_h$, $I_{\text{gref}}$ is the generated current for the case in which $T_h = 301$ K and $T_c = 300$ K at zero gate bias ($V_{\text{CG}} = 0$ V).

Figure 8(a) shows a linear variation of the current, $I_g$ as a function of $T_h$ for SG NWs with different $d_{\text{Si}}$ at $V_{\text{CG}} = 0$ V. Since the gap between the gates of the DG is small ($< 10$ nm), $I_g$ as a function of $\Delta T$ for DG is similar to SG. The formula of $I_g$ as a function of $\Delta T$ (equation (3)) can be derived based on equations of current in [22, 48–50].

For completeness, we also study the influence of applying a gate voltage ($V_{\text{CG}}$) to optimise $P_{\text{max}}$ when $D_{\text{it}} = 10^{12}$ cm$^{-2}$ eV$^{-1}$ and $\phi_m = 4.1$ eV. A channel diameter of $d_{\text{Si}} = 12$ nm is chosen for this investigation as it is the most sensitive to $V_{\text{CG}}$. A $V_{\text{CG}} = 0.25$ V is required to reach the optimized carrier concentration. The carrier concentration at this voltage results in equal output power to the case when $\phi_m = 4.1$ eV and $D_{\text{it}} = 0$ cm$^{-2}$eV$^{-1}$ (ideal).

**Figure 5.** (a) Power-time, and (b) $\Delta T$-time. $\varphi_m$ is 4.1 eV, 3.9 eV, and 3.9 eV for $d_{\text{Si}} = 12$ nm, 37 nm, and 62 nm, respectively.

**Figure 6.** Maximum output power as a function of interface charge density for GAA with $d_{\text{ox}} = 8$ nm, $d_{\text{Si}} = 12$ nm, and two metal work function values at $\Delta T = 15$ K. The grey and black lines are for 4.1 eV and 3.9 eV work functions, respectively.

**Figure 7.** (a) Schematic of a DG temperature sensor with control gate (CG) and program gate (PG). (b) The conduction band $E_c$ along the length of the SG and DG GAA NW for $-0.4 \leq V_{\text{CG}} < 0$ V and CG lengths of 30 or 50 nm. $d_{\text{Si}} = 12$ nm and the NW length is 220 nm.

**4. Gated structure for temperature sensing**

Single gated (SG) (figure 1) and double gated (DG) (figure 7(a)) GAA NWs can also be used as hot spot temperature sensor. The core of the DG structures is an Al/i-Si/Al NW wrapped with 8 nm of SiO$_2$. In the DG configuration one gate controls the carrier density (CG) and the other programs (PG) the carrier type in the NW. The work function of the gates is set to $\phi_m = 4.1$ eV and $D_{\text{it}} = 0$ cm$^{-2}$eV$^{-1}$ for all simulations in this section. The gap between the gates is 10 nm. $V_{\text{PG}} = 0$ V at all times, while $V_{\text{CG}}$ is varied. $T_h = \text{variable}$ and $T_c = 300$ K, setting up a variable temperature difference $\Delta T$. The simulations are set up in the same way as in section 2. The variation of the conduction band as a function of control gate lengths ($L_{\text{CG}}$) is shown in figure 7(b) for different values of $V_{\text{CG}}$. A potential barrier ($\phi_B$) is generated between the two Al contacts by the work function difference between the Si NW and the gate metal. Applying a $V_{\text{CG}}$ in DG (or SG) GAA NWs, tunes the height of $\phi_B$ and thus controls the current that can flow through the channel. Since the DG structure is conducting electrons at $V_{\text{CG}} = 0$ V, a negative $V_{\text{CG}}$ will decrease the electron flow as it increases the potential barrier. When $T_h$ is increasing, the density of carriers at energy levels higher than $\phi_B$ increases, increasing the current, $I_g$. Temperature, $T_h$ sensing can be done in either two steps for higher accuracy, or a single step. $T_h$ can be sensed by, (a) using the linear relation between $I_g$ and $T_h$ at $V_{\text{CG}} = 0$ V for DG (SG) (figure 8(a)), and (or) (b) by adapting $V_{\text{CG}}$ to keep $I_g$ constant and equal to $I_{\text{gref}}$ under changing $T_h$, where $I_{\text{gref}}$ is the constant reference current. The value of $V_{\text{CG}}$ to maintain $I_{\text{gref}}$ is then the reading of $T_h$, $I_{\text{gref}}$ is the generated current for the case in which $T_h = 301$ K and $T_c = 300$ K at zero gate bias ($V_{\text{CG}} = 0$ V).
where $q$ is charge, $n$ is carrier density, $\mu$ is mobility, $x$ is cross sectional area of the channel, and $L$ (=220 nm) is length of the NW. As seen in equation (3), $n$, $\mu$, and area change the response of $I_g$ to $T_h$. $d_{Si}$ has significant impact on $I_g$, as it will affect $n$ and $\mu$ (figure 2) as well. $n$ reduces and $\mu$ increases as $d_{Si}$ increases.

The sensitivity ($\Delta I_{IK} = \frac{\Delta I_g}{\Delta T}$ with $\Delta T = 1$ K) of $I_g$ to $T_h$ depends on $d_{Si}$; $\Delta I_{IK} = 0.63$ nA K$^{-1}$, 3.40 nA K$^{-1}$, 7.22 nA K$^{-1}$ for $d_{Si} = 12$ nm, 37 nm, and 62 nm, respectively. Figure 8(b) gives the variation of $I_g$ as a function of $V_{CG}$ at $\Delta T = 1$ K for the SG structure and the DG structure with two different $L_{CG}$.

The $CG$ length ($L_{CG}$) has a strong influence on charge carrier flow since it controls the depletion width and $\phi_B$ at $V_{CG} < 0$ V (see figure 7(b)). The effect of $L_{CG}$ (30 nm and 50 nm) on temperature sensing is studied for $d_{Si} = 12$ nm, 37 nm, and 62 nm and compared to the SG structure with gate length equal to the NW length. The variation of $I_g$ as a function of $V_{CG}$ is exponential over a wide gate voltage range, similar to a FET in weak inversion. As in FETs, this characteristic can be expressed in terms of subthreshold swing [51]:

$$SS = \left( \frac{d\log(I_g)}{dV_{CG}} \right)^{-1}.$$  

SS is given in table 1. While in signal FETs, SS needs to be near 60 mV dec$^{-1}$ [52], SS for temperature sensing should be high. This is confirmed in figure 9 that gives the value of $V_{CG}$ for constant $I_g = I_{gref}$ for changing $T_h$. The slope of $V_{CG}$ versus $T_h$ is highest for the longest $SS$. $I_{gref}$ is different for different $d_{Si}$, namely 0.65 nA, 3.51 nA, and 7.51 nA for $d_{Si} = 12$ nm, 37 nm, and 62 nm, respectively.

In the two-step temperature sensing implementation, first $I_g$ in (i) can be used to find the required $V_{CG}$ in (ii) to maintain $I_g = I_{gref}$. In this approach, the device is pre-calibrated to apply a specific $V_{CG}$, based on generated $I_g$ as a function of $T_h$ in case (i). After applying the required $V_{CG}$, achieving $I_g = I_{gref}$ in

$$V_{CG} = \frac{ab + cP_1}{b + P_1^2}$$  

where $a$, $b$, and $c$ are constants that are dependent on gate length and $d_{Si}$. These parameters for the simulated structures are shown in table 2.

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**Figure 8.** (a) The generated current ($I_g$) as a function of hot side temperature ($T_h$) in the SG NW for $d_{Si} = 12$ nm, 37 nm, and 62 nm. (b) The variation of the sensor current as a function of the control voltage ($V_{CG}$) for the SG and DG NWs at a $\Delta T = 1$ K and $d_{Si} = 12$ nm.

**Table 1.** Subthreshold swing ($SS_{x,y}$) as a function of $\Delta T$ and $d_{Si}$. $x =$ SG, DG for single, double gate, respectively; $y =$ 30, 50 for the control gate length $L_{CG}$ in nm.

| $d_{Si}$ (nm) | $\Delta T$ (K) | $SS_{SG}$ (mV dec$^{-1}$) | $SS_{DG,50}$ (mV dec$^{-1}$) | $SS_{DG,30}$ (mV dec$^{-1}$) |
|--------------|--------------|----------------|----------------|----------------|
| 12           | 1            | 62             | 65             | 74             |
| 12           | 5            | 63             | 66             | 75             |
| 12           | 10           | 63             | 67             | 76             |
| 37           | 1            | 63             | 84             | 124            |
| 37           | 5            | 63             | 84             | 124            |
| 62           | 1            | 64             | 115            | 199            |

**Table 2.** Specific parameters for the simulated structures.

| $d_{Si}$ (nm) | $a$ | $b$ | $c$ |
|--------------|-----|-----|-----|
| 12           | 0.65| 3.51| 7.51|
| 30           | 0.65| 3.51| 7.51|
| 50           | 0.65| 3.51| 7.51|
5. Conclusion

In order to optimize the thermoelectric performance of GAA NWs, the metal gate work function ($\phi_m$) was used to modulate the carrier density of the intrinsic Si NWs for maximum output power. NWs with different diameters, $d_{Si}$: 12 nm, 37 nm, and 62 nm were studied, and it was found that the NW with $d_{Si} = 62$ nm generated the best output at a presence of constant and steady temperature difference ($\Delta T$). However, NWs with lower diameter show higher reliability in preserving $\Delta T$ when the heat source’s temperature varies, due to their lower thermal conductivity. It was shown that significant power degradation occurs due to interface roughness scattering and interface trapped charges. Using metals with lower $\phi_m$ can compensate for this. In addition, single and DG structures, can be used for temperature sensors by modulating the carrier concentration with a gate voltage. SG and DG structures show that the temperature sensor can operate in two different modes to insure the correctness of the detected temperature. It was shown that gated structures with higher diameters or smaller control gate length require higher operational voltage, if a two-step temperature sensing is implemented. The DG NW with $d_{Si} = 62$ nm and control gate length of 30 nm show higher sensitivity to temperature changes.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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