Design of MUX based Flash ADC for Reduction in Number of Comparators

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Abstract. This paper presents the design of multiplexer-based Flash ADC with a reduced number of comparators to achieve less area and less power consumption with increased resolution. As the number of bits increases, flash ADC needs a huge number of comparators which increases the area of the chip, and also the power consumption will increase. The conventional N-Bit Flash ADC requires a $2^N$ number of resistors and $2^N-1$ number of preamplifiers and comparators. Here the number of comparators is reduced by using multiplexers by providing reference voltage through multiplexers. And also, the encoder is designed using multiplexers. The 6-bit Flash ADC is designed utilizing multiplexers and a reduced number of comparators. The Simulation is done by using the proteus 8.9 design suite with 1v supply voltage.

Keywords: Comparators count, Flash ADC, Multiplexer, Power consumption.

1. Introduction

In all the digital systems data conversion is the main process that is done with the help of Analog to digital converter. There are many types of ADC’s available for this conversion but among those Flash ADCs are more advantageous because of their high speed. Flash ADC has a high speed due to the simultaneous conversion. The addition of the comparator delays and the logic delays (logic delays are negligible) gives the conversion speed of flash ADC. Flash ADC is provided with input voltage which needs to be converted and the unique reference voltage. The conventional flash ADC includes the resistor ladder network, preamplifiers, comparators, and priority encoder. The specified figure 1 exhibit the structure of conventional Flash ADC, For N-bit transformation, $2^N$ number of resistors and $2^N-1$ number of comparators and preamplifiers are needed [1]. Here reference voltage is provided by using a resistor ladder network for each comparator [2-3]. Each comparator is provided with a reference voltage of 1 LSB (least significant bit). The comparator yields logic “1” if the signal applied on the input line is more prominent than the reference voltage. Conversely, the comparator yields logic “0”, if the signal applied on the input line is smaller than the reference voltage and then all the comparators outputs are provided to the priority encoder for final conversion into digital output [4].

In conventional Flash ADC increase in resolution increases the number of comparators. we need to reduce the comparators without limiting the resolution of the flash ADC. To achieve less area and less power consumption.
The above figure 1 shows a 3bit conventional flash ADC with 7 comparators, 7 registers, and 1 (8 to 3) priority encoder. Here the input is given to one of the input lines of all the comparators and reference voltage to all the comparators is provided with register ladder network. The outputs from all the comparators are given to the priority encoder for the final conversion and the output of the priority encoder is the final digital output of the conversion.

The reference voltage is divided into steps and the step size is given by \( \frac{v_{\text{ref}}}{2^N} \). The resolution of Flash ADC is defined by the step size. The conventional Flash ADC has the disadvantage of limited resolution, larger area, and high power consumption so it can be improved by using multiplexers in the design of Flash ADC. The proposed design of Flash ADC has many benefits compared to conventional Flash ADC. In the proposed work Flash ADC needs only \( (2^{(N-2)} + 1) \) number of comparators, which is the need for high-resolution ADCs [5-6].

2. Literature Review

The flash ADC with low power and low resolution with different sampling rates is used in many versatile applications because of its effortlessness and quick activity. The flash ADCs also suffer from huge input-referred noise and comparator offsets. To remove these problems many strategies have been presented. Preamplifiers count can be reduced by using interpolation techniques [1-2]. For N-bit Flash ADC needs a \( 2^N \) number of registers and \( 2^{(N-1)} \) number of preamplifiers and comparators so the fabrication area on-chip will increase as the number of bits increases which also increases the power consumption due to a large number of components. So low power and low voltage comparators are designed like double tail CMOS comparator to reduce the power consumption [3-4]. The high speed and high-resolution comparators are designed by using BiCMOS and CMOS VLSI technologies. We will have the option to accomplish a higher goal and speed by keeping up low power, less information capacitance, and low intricacy. With 12-bit resolution and 10 MHz of comparison rates, the BiCOMS and CMOS comparators are designed [5]. comparator operation can also be improved by modifying the threshold of the comparator circuit. In this TIQ comparator can also be used to replace the resistor network but it suffers
from input frequency to overcome this improved CMOS inverter comparator is proposed to reduce area and power requirement. A flash ADC with a bit reference encoder can be designed for high-speed applications [6-18]. The Flash ADC can also be designed using domino CMOS logic for reducing power consumption and increasing the speed [7].

3. The architecture of Proposed Flash ADC

The proposed 6-bit MUX based flash ADC contains a resistor ladder network, a (2x1) multiplexer, 8 (4x1) multiplexers, 17 comparators, and a 6-bit thermometer to the binary encoder. The below figure 2 shows the optimized design of flash ADC using multiplexers.

The proposed Flash ADC is provided with an input signal which needs to be converted into a digital signal and the reference voltage. The first comparator (C1) compares the input signal with the reference voltage level 32/64 \text{vref}. The yield of this comparator C1 is taken as the digital outputs most significant bit (MSB) and provided as a control signal to the preceding multiplexers (M1-M9). Similarly, the same input signal is simultaneously given to the second comparator (C2) and compared with either 16/64 \text{vref} or 48/64 \text{vref} by using a 2x1 multiplexer [7-9]. The reference voltage for C2 is selected depending on the first comparator (C1) yield. The yield of the second comparator is again taken as the digital outputs second most significant bit (MSB). The two MSB’s of the digital output provided from comparators (C1 & C2) acts as the control signal to all 4x1 multiplexers to provide a reference voltage to all the other comparators. The output from all the comparators is fed to the thermometer to the binary encoder to convert the input signal into digital output [10].

![Figure 2. The architecture of 6-bit MUX based Flash ADC.](image)

In this work, the new low power, low offset CMOS comparator is introduced. With this comparator, the elimination of preamplifiers and track and hold circuit is achieved. Because comparators are the sampling devices here no need to have a track and hold circuit at the input side. The number of comparators is also reduced; therefore, less fabrication area and reduced power consumption are achieved.
Table 1. The total preamplifiers and comparators required.

| Resolution (Bit) | Flash ADC | Proposed Flash ADC |
|------------------|-----------|--------------------|
|                  | Pre-amp $2^N - 1$ | Comparators $2^N - 1$ | Pre-amp | Comparator $2^{N-2} + 1$ |
| 4                | 15        | 15                 | -       | 5                     |
| 6                | 63        | 63                 | -       | 17                   |
| 8                | 255       | 255                | -       | 65                   |
| 10               | 1023      | 1023               | -       | 257                  |
| 12               | 4095      | 4095               | -       | 1025                 |

Where $N$ denotes the Resolution.

Table 1 shows the comparators and preamplifiers count in the conventional and MUX based flash ADC with different resolutions. From the above table, we can observe that for 6-bit conventional flash ADC 63 comparators and preamplifiers are required whereas in proposed flash ADC only 17 comparators are required and preamplifiers are eliminated. Thus, we can observe that number of comparators has been subsequently reduced and due to a reduction in comparators count area and power consumption will be reduced. Also, the preamplifiers are eliminated. so, this can be used in the various applications where the power and area are of major interest [11].

4. Applications of MUX Based Flash ADC

These digital systems find applications in various high-speed devices that range from audio communications to medical applications. Numerous remote versatile applications require fast information converters with the high sign to commotion ratio, wide transmission capacity, and variable resolution with streamlined power and decreased expense. so, we need to redesign the ADC to meet prerequisites as indicated by developing advances. The digital signal processing is the robust and cost-effective way of signal processing in various applications the input and output signals will be in the analog form so conversion from analog to digital is required at interfaces. so, this flash ADC will act as the interface between the analog signal coming from the real world and the functional block of DSP. This flash ADC can be used in video-imaging systems and personal communication systems. The high speed and high-resolution flash ADCs can be used in wireless communication and image processing. It also finds applications in Radar detection, Wideband radio receivers, Electronic test equipment, optical communication links, Satellite communication, Sampling oscilloscope, High-density disk drivers, and universal DSP receivers, etc. [12-16].

5. Components in MUX Based Flash ADC

5.1 Comparator

The comparator is a very important component in Flash ADCs, here it acts as a quantizer in the ADCs. It is of 1 bit having two levels either a ‘1’ (implies VDD = +2.5) or ‘0’ (implies VSS = -2.5). Whenever input applied to the comparator is more prominent than the reference voltage at that point yield is 1 and whenever the contribution of input voltage of the comparator is not as much as the reference voltage at that point yield is 0. Here we have utilized two-stage CMOS OPAMP as a comparator to accomplish faster operation and low power utilization. The comparator comprises current mirrors, current sinks, active load, and constant current source. Transistors W/L proportions are chosen so that comparators give the exact and ideal outcomes. Parasitic impacts that influence the performance of the comparator are limited in this structure. This helps to get a low power and high-speed comparator [13-14].
The comparator sampling speed is obtained by its regeneration time constant which is contrarily proportional to the square of gate length for a CMOS technology [15]. Due to very low matching requirements, the comparator can be optimized for high speed, low power, and low area requirements. The generation of bubble errors is eliminated [16].

![Figure 3. Schematic of comparator.](image)

Figure 3 shows a schematic of the CMOS comparator made using a two-stage operational amplifier.

5.2 Thermometer to Binary Encoder

It is used to create binary data that can be processed in real-time. There are many ways to design the encoder but most of the designs have the disadvantages like less speed, high complexity, the occurrence of bubble error problem, high power consumption, and unbalanced signal paths so to avoid these all problems multiplexer based thermometer to the binary encoder is designed with lower bubble error suppression, less delay, lower critical path, and less area. Due to these all benefits this encoder can be used in many low power applications. Here we have designed an 8-to-3 MUX based thermometer to a binary encoder that has 7 OR gates and 4 (2X1) multiplexers as shown in figure 4. The outputs of all the comparators which is the thermometer code is fed to the OR gates and the OR gate outputs are provided to the multiplexer inputs. The mux gives the output according to the control signal provided to it. One output bit is taken directly from the OR gate and the other two bits are taken from the two Multiplexers makes the final digital output. This works like a priority encoder by selecting higher-order active inputs from comparators output and converts them into binary and ignores all other active inputs. Here multiplexers are used to correct the bubble errors that occurred due to mismatches in the comparator’s inputs. Table 2 denotes the 8 to 3 encoder truth table.
Figure 4. Block diagram of a 3-bit thermometer to a binary encoder.

Table 2. The 8 to 3 Encoder truth table.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | B2 | B1 | B0 |
|----|----|----|----|----|----|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | X  | 0  | 0  | 1  |
| 0  | 0  | 0  | 0  | 0  | 1  | X  | X  | 0  | 1  | 0  |
| 0  | 0  | 0  | 1  | X  | X  | X  | X  | 0  | 1  | 1  |
| 0  | 0  | 1  | X  | X  | X  | X  | 1  | 0  | 0  | 0  |
| 0  | 1  | X  | X  | X  | X  | X  | 1  | 0  | 1  | 0  |
| 1  | X  | X  | X  | X  | X  | X  | 1  | 1  | 0  | 0  |

Where X denotes don’t care.

Comparator simulations
The comparator design is simulated on the proteus 8.9 simulation tool with a power supply of +2.5v and -2.5v. The sinusoidal input signal of 1v with a frequency 5kHz is applied with a reference voltage of 0v, we get the output as 1v which refers to +2.5v and when the input signal with 0v is applied with 1v sinusoidal reference voltage we get the output as 0v which refers to -2.5v as shown in above waveforms. When the input signal is prominent compared to the reference signal then the positive half cycle of the input signal become visible at the output which represents +2.5v VDD supply and when the input signal is smaller than the reference signal the output we get as 0v because here we have used reference signal as 0v which represents the -2.5v VSS supply.

**Table 3. Comparison of flash ADC’s**

| Specification (unit) | [7] | [17] | [11] | This work |
|----------------------|-----|------|------|-----------|
| Publication title    | CICC |       | TENCON | -         |
| Technology (nm)      | 90  | 180  | 180   | 90        |
| Resolution (Bit)     | 6   | 4    | 6     | 6         |
| Supply voltage(v)    | 1.2 | 2.5  | 1     | 1         |
| Power (mw)           | 12  | bandwidth | 0.4  | 2.511E6 Hz |

6. Conclusion

In this paper, MUX based Flash ADC is designed by using Proteus 8.9 simulation tool. The number of comparators is reduced and the preamplifiers are eliminated. So, for the design of N-bit flash ADC, $2^N - 2 + 1$ number of comparators are required instead of $2^N - 1$. And in the 6-bit Flash ADC, the comparators are reduced by 73%. Hence, the proposed MUX based Flash ADC can have less area and less power consumption.

7. Future Scope

The proposed flash ADC has reduced the number of comparators from $2^N - 1$ to $2^{N-2} + 1$, further it can be reduced to increase the resolution. In the proposed design comparators are reduced by using multiplexers and designing low power, the high-speed comparator in the future can be reduced by using any other methods. In the present design, the encoder is designed by using multiplexers which convert the thermometer code into binary output, in future ADC with different encoders can be designed which can be used in high-frequency applications.
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