POWER OPTIMIZATION BY USING RECONFIGURABLE LFSR WITH GATED CLOCK

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Abstract

LFSR are the most commonly used test pattern generators due to its efficiency than any binary counters. This paper presents the design of a novel reconfigurable LFSR with clock gating for VLSI testing. The technology advancement in VLSI has increased the complexity of chip testing. This complexity in testing has made the Logic BIST (LBIST) more popular than Automatic Test Equipment. This helps the testing with an additional hardware added inside the circuit. ATE does not apply any test patterns but the test patterns are generated by the testing circuits which are inbuilt in the hardware. Thus the cost of testing is greatly reduced. In the LBIST, reconfigurable LFSR are used for the test pattern generation which improves the fault coverage in IC testing. This increases the generation of random test pattern. To increase the speed of testing and reduce the power required a clock gating is introduced in the reconfigurable LFSR. In traditional testing more transistors are required in the circuits resulting in consumption of more power than power required for the functioning of the circuit. Conventional clock circuit consumes 70% of the clock buffer. This reduces the number of switching activities in the BIST. The power consumption of the proposed reconfigurable LFSR with gated clocking is significantly reduced when compared with the conventional LFSR with clocking circuits.

Keywords : VLSI, BIST, reconfigurable LFSR, clock gating, low power, switching, FPGA

1. INTRODUCTION

The increasing complexity of Integrated Circuit (IC) designs has led to the increased difficulty in VLSI testing. Due to the technology advancement it has made VLSI testing for common faults like
bridging faults and Stuck-at-faults. This has made the way for the new testing technology among the technologist called Logic BIST. To ensure the durability and safety, the testing inside the circuit prefers Logic BIST which tests the quality and structural integrity of the chip.

A digital system, in numerous occasions is put for testing and is diagnosed. It is highly decisive to have a testing which is quick and highly fault coverage. In semi-conductor industries, the most common and widely adopted technique for IC chip testing ensures that the test is made as a part of system functionality and thus the test becomes a self-test. Designing a system without the feature of internal or integrates test policy for all levels starting from entire system down to the components is termed as system-foolish and chip-wise. Whereas a BIST offsets the added cost for the test hardware also ensuring the system testability, reliability with reduced system maintenance cost.

The objective of BIST is to design a circuit which is capable of self-test as “good” (fault-free) or “bad” (faulty) respectively. It requires an additional circuit which generates test patterns along with mechanisms to check whether the output responses under Circuit Under Test (CUT) matches to the patterns generated by a fault free circuit. The two key functions of BIST are generating the generators using Test Pattern generator (TPG) which is tested using CUT and analyzing the patterns as pass or fail using Output Response Analyzer (ORA).

BIST requires two more functions at the system level includes BIST test controller and an Input Isolation Circuitry (ISC). Also apart from the basic system I/O pins, BIST needs additional I/O pins to activate its sequence such as Start control signal, analyzing and indicating the output as Pass/Fail and an indication for the completion of BIST which is optional as “BIST Done” stating whether the BIST sequence is valid or not. The result shows whether the circuit is faulty or fault-free.

Section 2 presented the literature survey of the paper. The BIST architecture and the types of LFSR are describes in section 3. The section 4 deals with clock gating technique. The proposed LFSR architecture with gated clock is presented in section 5. The Simulation results and synthesized reports are given in section 6 and results are compared with the other types LFSR methods. The results are concluded in section 7.

2. LITERATURE SURVEY

Designing Logic BIST includes both board and on-chip circuitry to generate the test patterns and the output responses are analyzed. Logic BIST can perform internal testing which does not require any external circuit for testing. This internal in-circuitry testing decreases the size of the circuit for testing and any external equipment for testing. This reduces the testing cost and increases the speed of testing
This guarantees entire fault coverage and the chip area is reduced to about 15% of overall chip area. In LBIST, PRPG generates the test patterns and are fed as the input to CUT. MISR is used as the output analyzer. The corresponding outputs are compared with the golden signature through a comparator and the circuit is checked for fault-free or faulty [2][3].

Alternating variable Run-length coding is used to reduce the test data in LFSR [4]. MISR and Pseudo Random Pattern generator (PRPG) are the critical components in Logic BIST. LFSR is used for the implementation of PRPG and the test patterns generated are fed to CUT for testing [5][6]. Reconfigurable LFSR constitutes XOR gates, flip-flops and multiplexers. The linear function to LSB flip-flop is the input from the shift register. The linear functionality is provided by XOR gates. Many researchers work on reconfigurable LFSR [7],[8],[9]. Test pattern generation is the common application of LFSR [10]. By relaying the multiplexers, reconfiguring of LFSR is performed [11]. But this increases the complexity of the circuit and it requires n-1 XOR gate for an n-bit LFSR even though the feedback polynomial require onlly a decreased number of taps. LFSR has a wide range of applications.

3. BIST ARCHITECTURE

The hardware architecture of BIST is shown in Figure 1. In this work, the schematically represented architecture of BIST is followed for developing the IOP BIST module. In general, BIST architecture consists of a hardware pattern generator, test controller, input multiplexer and a CUT. In this work, CUT is the output response comparator and also the IOP. Optionally with BIST, the Read Only Memory (ROM) and a comparator is included. As shown in Figure 1, the test controller controls the test patterns and its generations in BIST mode. Pattern generator generates the patterns as input to the CUT.
Normally, extensive test patterns are generated by the pattern generator as input to the CUT in order to ensure high fault coverage. For instance, the number of inputs to the CUT is 10, and then the required number of test patterns is 1024. Primary inputs are fed as the input to CUT during the functional mode or in non-BIST mode. The selection of correct input to the CUT is done by the input multiplexer for different modes. During the BIST mode, the input is generated by the hardware pattern generator but during the functional mode, the primary inputs are fed as the input to the CUT. Output response compactor compacts the circuit responses in number to a manageable size so that it can be utilized as signature and is stored on ROM.

3.1. Types of LFSR

Basically there are four different types of LFSRs used in designing BIST architecture. They are discussed below.

a) Standard LFSR  
b) Modular LFSR 
c) Complete LFSR  
d) Hybrid LFSR

3.1.1 Standard LFSR
A standard LFSR is also called as external XOR LFSR or Fibonacci LFSR. XOR LFSR acts as the shift register in which XOR gates denote the tapping positions in the feedback polynomial. These polynomials are concatenated and a new output bit is generated. This newly generated single output bit is fed as the input to the final flip flop in the architecture. Figure 2 illustrates an n-bit Standard LFSR.

![Figure 2. Architecture of a Standard n-bit LFSR](image)

3.1.2 Modular LFSR

A Modular LFSR is also called as Galois, one-to-many, internal XORs. One-to-many LFSR is another form of conventional LFSR which generates the same test patterns similar to that of the conventional one. The only variation between a modular and a conventional LFSR lies in the connectivity of taps in its feedback polynomials. Based on the tap positions, connectivity of XOR gates with the flip flops are done. The output of one flip flop is immediately fed as the input to its next flip flop. Between any two flip flops there exist only one XOR gate on the critical path and this is the prominent advantage of a modular LFSR over a conventional LFSR. All XOR gates are included based on the number of taps. Hence, this feature increases the execution speed of a modular LFSR when compared with a conventional LFSR. Thus Galois LFSR is more efficient than an ordinary LFSR. Figure 3 illustrates the architecture of an n-bit modular LFSR.
Figure 3. Architecture of n-bit Modular LFSR

3.1.3 Complete LFSR

The objective of all types of LFSR is generation of a maximum length of test data sequence up to $2^n-1$ only. Architecture of a complete LFSR is shown in Figure 4. An all-zero condition can push the LFSR into an unfunctioning state called as locked-state condition. A complete LFSR is a modified form of a conventional LFSR which includes all-zero state. Hence, a complete LFSR type can be designed and developed from a conventional LFSR just by adding an XOR gate at the last stage of LFSR. Also, a NOR gate which has $n-1$ inputs is used for zero detection. Thus $2^n$ patterns are generated using a complete LFSR for a normal primitive polynomial feedback [18].
3.1.4 Hybrid LFSR

For illustration consider the polynomial \( f(x) = 1 + m(x) + q(x) \) and this polynomial is said to be fully decomposable only when \( m(x) \) and \( q(x) \) has no terms in common. An integer \( J \) exist such that \( q(x) = x^Jm(x) \) with the condition \( J > 1 \). Then its corresponding polynomial is expressed as follows.

\[
F(x) = 1 + m(x) + x^J m(x)
\]

From the above polynomial, a hybrid polynomial called as Top-bottom polynomial can also be constructed by using the below mentioned connection polynomial.

\[
P(x) = 1 + x^J + x^J m(x)
\]

Where \( \oplus x^J \) represent XOR gates with only one input. This input is the output of the \( j^{th} \) stage LFSR which is connected in the feedback path and LFSRs in between the stages are not considered. The great advantage of this hybrid LFSR over the other LFSRs is the reduction in the usage of XOR gates say from ‘\( m \)’ number of XORs to \( (m-1)/2 \) number of XORs in the Hybrid LFSR type. A modular LFSR uses the registers from \( (j-1)^{th} \) stage of registers.

Thus, Hybrid LFSR is highly efficient than other types of LFSRs in terms of reduced usage of circuit area with reduced number of XOR gates and increased speed. Figure 5 illustrates the architecture of a Hybrid LFSR.

4. CLOCK GATING
In the technology advancement in VLSI systems, power is found to be most predominant constraint in designing a VLSI system design. In fact, clock power plays a major contribution in the consumption of dynamic power in the chip. Since the clock is connected to the entire functional block set in any synchronous VLSI system. Another reason for more power consumption is the increased switching activity caused every time when the clocks switch at every cycle resulting in the generation of signals. The total power consumption of clock activity is almost 50-70% of the total power consumption of the chip. Hence to reduce this major power consumption, a technique called as clock gating is introduced [2]. Some of the other reasons for power dissipation with respect to the clocks are listed below.

- Power dissipation created in the clock network.
- Power dissipation due to clock buffers.
- Power dissipation caused by flip flops.

Cost, performance, power, area and cost are the major factors deciding the successful functioning of a VLSI design circuit. The increased power dissipation in a VLSI circuit can be reduced when the output is found to be same as the input and by the deactivation of its clock signal. Among the available techniques to reduce the power dissipation, clock gating is one of the most important and preferred technique. Total power dissipation caused in the clock network depends on two factors say data rate and clock frequency. Thus, the total power dissipation in a clock network can be computed as follows.

\[ P_{ck} = V_2d f_{ck} (C_{ck} + C_{ff,ck} + C_{ff,cd}) \] [2]

Where,

- \( f_{ck} \) – clock frequency.
- \( C_{ck} \) – total capacitance in the clock network
- \( C_{ff,ck} \) – capacitance observed by the flip flops on the path of the clock
- \( C_{ff,cd} \) – capacitance observed by flip flops on the data path

### 4.1 Gated Design in a N-Bit LFSR

To reduce the power consumption in digital systems, Dynamic power management is used. The objective of Dynamic Power management is to disable the functional modules which are found to be inactive or disabled for a particular time. This strategy of disabling the functional modules based on
their participation in the system function is termed as Gated Clock approach. The Gate Clock for an n-bit LFSR is illustrated in Figure 6 [4].

![Circuit design of a Gated clock in an n-bit LFSR](image)

**Figure 6. Circuit design of a Gated clock in an n-bit LFSR**

### 4.2 Look-Ahead clock gating (LACG)

Complete clock cycles are allotted to avoid the timing constraints occurring in DDCG and AGFF techniques. LACG achieves goals as disabling the clock pulse in its master latch and making it suitable for general clock designs when compared to AGFF. XOR output of auto-gated clock design is used for the generation of enabling signals for all other flip flops but is applicable only for the specified interval
\{t_{\text{setup}}, t_{\text{ccq}}\}, \text{where } t_{\text{setup}} \text{ is the setup time for FF and } t_{\text{ccq}} \text{ is the contamination delay from clock to its output. After the contamination delay, the output of XOR gate is automatically corrupted and its value becomes zero [11]. Hence, a latch is used to make the value of output valid throughout the positive cycle period. Figure 7 represent the general logic of LACG.}

![Figure 7. LACG of General logic](image)

In the Figure 7, FF1 is the source flip flop and FF2 is the destination flip flop. The destination FF depends on the value of \(k>1\) of the source FF without any external input from the block. The output set of XOR gates of the source flip flop FF1 is assumed as \(X(D2)\) and \(Q(D2)\) be their corresponding outputs. Since the flip flops in clock gating results in more power consumption and extensive overhead, the flip flop FF3 is gated as shown in Figure 7. As FF3 is clocked oppositely, the value of \(X3\) which is the signal to enable the clock is made negative. FF3 is quite a normal flip flop which has the internal XOR gate connected in between \(D3\) and \(Q3\).

5. PROPOSED LFSR ARCHITECTURE WITH GATED CLOCK

A reconfigurable LFSR with gated clock is proposed in this paper. A conventional LFSR can generate \(2^n-1\) states when the considered polynomial is primitive and the number of generated is less than \(2^n-1\) when the polynomial taken is non-primitive. A Programmable LFSR (PLFSR) can increase the randomness of the output. This PLFSR uses multiplexers, XOR gates and D-flip-flops. Figure 8 illustrate the proposed LFSR architecture. The required polynomial for the circuit design is given by the chain value. Based on the chain value, XOR gates are introduced between the flip flops. The value of PN
sequence available before repetition is determined by the type of taps used. This provides the PN sequence of the cycles. Multiplexers in the design make the LFSR as a reconfigurable LFSR. Either loading the flip flops or shifting the values in the register is decided by the select signal. If the value of the select signal is zero then LFSR is loaded with its initial value else the shifting operation is performed based on the selection of the feedback polynomial. Also, the length of LFSR is programmed to have the length as n-bit.

In this paper, types of LFSRs standard LFSR, modular LFSR, complete LFSR and Hybrid LFSR are designed as reprogrammable. The designs for complete and standard are same except the need of an additional circuit in complete LFSR.

Figure 8. Proposed LFSR with clock gating
The NOR gates in this circuit gets all the output of the flip-flops as its input and are passed to a XOR gate. Whereas XOR gate also get input from the designed feedback path of a standard LFSR. The output of XOR gate is fed as the feedback input to the reconfigurable LFSR. By performing the above process, 2^n exhaustive patterns are generated by LFSR and fault coverage is also improved. In the top-bottom HLFSR design, the XOR gates are reduced by using both Standard LFSR and Modular LFSR configurations in the circuit design. Figure 8 represent the architecture of the proposed reconfigurable LFSR with clock gating.

6. SIMULATION AND SYNTHESIS

The proposed reconfigurable LFSR design is described in Verilog HDL and simulation is performed in ModelSim 6.5 RTL and for FPGA synthesis Xilinx ISE is used. EDA tool is Encounter RTL.

6.1. Simulation results

Figure 9 shows the simulation result of a 16-bit Standard LFSR type generating 65535 patterns. The clock period is 20ns for 10 as the seed value [1].

![Figure 9. Simulation result of 16-bit R-LFSR](image)

6.2 Synthesis results using Xilinx ISE tool

Analysis of results was done after the synthesis for 16 bit and 32 bit LFSR with its varying configurations. From the analysis, it is found that Modular LFSR has the maximum operating frequency of 509 MHz when compared with SLFSR, CLFSR or HLFSR for any kind of bit configuration. CLFSR takes more time for execution as it has enormous number of gates being involved in critical path. HLFSR has more operating frequency when compared with SLFSR. Memory utilization is found to remain same
for all types of LFSRs. Figure 10 shows the synthesis result of Modular LFSR. Various literatures shows the synthesis results of different types of bits LFSR in a RTL compiler.

Figure 10. Synthesis of a 16-bit Modular R-LFSR

Figure 11 shows the synthesis results of a 16-bit reconfigurable LFSR with clock gating and Figure 12 shows the synthesis of 32-bit reconfigurable LFSR with clock gating. The analysis of the discussed work shows that, reconfigurable LFSR with clock gating is found to be more efficient in terms of power and speed than any other conventional and reconfigurable LFSR without clock gating.

Figure 11. Synthesis result of 16-bit reconfigurable LFSR with clock gating
7. CONCLUSION AND FUTURE WORK

In this paper, the architecture of Reconfigurable Logic BIST (RL-BIST) is proposed. All the components in the architecture were designed so that they are programmable. Thus self testing for various configuration of circuitry is designed. Re-configurability in MISR and PRPG is achieved by adding the multiplexers. Tap insertion inside the circuit is made flexible which determine the circuit’s feedback polynomial and test pattern generation. HLFSR achieves high speed when compared with SLFSR due to the utilization of reduced number of gates. Though complete and Modular LFSR generates 2n test patterns, it occupies more area and it is the main drawback of it. Comparison of various parameters like speed and power shows that reconfigurable LFSR with clock gating is more efficient than other LFSR types. The only drawback of the proposed method is large area utilization. As clock circuits are added to reconfigurable LFSRs the area of the circuit is more. Size of circuit reduction can be carried out as the future work.

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