1. Introduction

Two-dimensional materials (2DMs) have awakened the great interest of the nanotechnology community during the last decade [1]. Their striking physical properties, intrinsically different from their 3D counterparts, open a vast field of opportunities only partially exploited so far. Among these alternatives, 2DMs find a natural spot in electronics, where their monoatomic thickness makes them especially attractive to overcome the hurdles related to the transistor scaling-down [2].

Graphene is not only the pioneer, but also the most singular member of the 2DM family [3]. It is characterized by a gapless Dirac-cone bandstructure, where electrons and holes have symmetric dispersion relationships. The literature is abundant in Graphene Field-Effect Transistors (GFETs) [4–6], where this particular band structure is manifested in an ambipolar behaviour and a poor $I_{ON}/I_{OFF}$ ratio (direct consequence of the easiness to switch the carrier transport from electrons to holes and vice versa). This issue jeopardizes the use of GFETs in digital electronics, although a successful demonstration has been achieved in [7]. In radio-frequency (RF), however, graphene has revealed itself as an interesting candidate [8], and devices with cut-off frequencies of hundreds of GHz have already been demonstrated [9,10], even reaching wafer scale integration [11], or being applied for flexible electronics [12,13]. The main strategies to boost GFETs performance have consisted of the
scaling-down of the gate oxide thickness \[4,14\], the encapsulation in hexagonal boron nitride \[15\] or
the improvement in the quality of the graphene-insulator stack \[7,16\]. In particular, clean self-aligned
fabrication, based in pre-deposited gold, has been proposed in \[17\]; while the self-aligned transfer of
the gate stack (processed in a sacrificial substrate) has been detailed in \[18\].

The transfer characteristic of experimental GFETs is V-shaped, but very often shows an asymmetry
with respect to the Dirac voltage \[19\], usually associated with different electron and hole mobilities.
These mobility dissimilarities are the common path to handle the device response asymmetry,
leaving out of the spot the relevance of the gate underlapped areas \[15,20,21\]. These access regions
(intended to minimize the capacitance coupling between the gate and the source and drain) impact,
however, strongly on the GFET electrical behaviour, as they constitute a noticeable resistance pathway
for carrier transport. Partial attempts on the modelling of this issue have been discussed from an
analytical resistance-based perspective in \[20,22\], but a comprehensive study of their impact in the
GFET performance is still lacking \[18\]. In this work, we direct our attention to this asymmetric response
of GFETs and, by means of detailed numerical simulations, we explain such effect studying the impact
of the access regions in the transfer characteristic as well as in the RF performance of such devices.

The rest of the document is organized as follows. Section 2.1 presents the numerical model
employed for this study. To check and validate it we compare, in Section 2.2, the simulated transfer
response of two GFETs against the corresponding experimental measurements. Section 2.3 contains a
thorough analysis of the access resistances and a discussion of its influence on the cut-off frequency, \(f_T\).
Finally, the main conclusions are drawn in Section 3.

2. Results

2.1. Device Simulation

A schematic depiction of the physical structure of the simulated GFET is shown in Figure 1.
The graphene flake is sandwiched in between a top insulator layer, with thickness \(t_{\text{TOX}}\) and
dielectric permittivity \(\varepsilon_{\text{TOX}}\), and an insulating substrate, with thickness \(t_{\text{BOX}}\) and dielectric permittivity
\(\varepsilon_{\text{BOX}}\). Both oxides are assumed thick enough as to neglect any tunnelling current through them.
A four-terminal device is considered, with a front gate extending over a length \(L_{\text{Chn}}\) (the device
channel length), giving rise to two under-lapped regions of length \(L_{\text{Acc}}\) (the access region length) that
connect it with the source and drain terminals. The back gate, when considered, extends all along
the structure including the channel as well as the access regions. \(V_{\text{FG}}, V_{\text{BG}},\) and \(V_{\text{D}}\) stand for the front
gate, back gate, and drain terminal biases respectively, while the source terminal, \(V_{\text{S}}\), is assumed
to be grounded. The total resistance of this structure, \(R_T\), can be schematically split into the series
combination of three resistances corresponding to the source access region \((R_{S,\text{Acc}})\), the channel region
\((R_{\text{Chn}})\) and the drain access region \((R_{\text{D,Acc}})\).

To determine the \(I – V\) response of GFET devices, we have self-consistently solved the coupled
Poisson, Drift-Diffusion and continuity equations \[23,24\]. For the device modelling, we have
considered a longitudinal \(x – y\) section of the GFET, assuming invariance along the device width \((z)\).
The resulting 2D Poisson equation is given by:

\[
\nabla (\varepsilon (x,y) \nabla V(x,y)) = -\rho (x,y)
\]

where \(V\) is the electrostatic potential; \(\rho\) is the net charge density in the structure, that comprises the
mobile (electrons and holes) and fixed (dopants) charges; and \(\varepsilon\) is the dielectric permittivity.

The Drift-Diffusion transport equation is formulated in terms of the pseudo-Fermi level \((E_F)\) as
proposed in \[25\]:

\[
J(x) = q \left[ \mu_n n_{1D}(x) + \mu_p p_{1D}(x) \right] \frac{dV_{E_F}}{dx}
\]

where \(V_{E_F}\) is the potential associated with this level and \(n_{1D}\) \((p_{1D})\) is the graphene electron (hole) 1D
density profile. Here, \(\mu_n\) \((\mu_p)\) stands for the electron (hole) mobility. Due to the extreme confinement,
the carriers are supposed to move only along the transport direction ($x$). $J$ must comply with the continuity equation that, under steady-state conditions, is formulated as: $\nabla \cdot J = 0$. Ohmic contacts are assumed at the source and drain terminals, with the Fermi level at the source grounded, $E_{FS} = 0$, and at the drain given by $E_{FD} = -qV_{DS}$. The equation system is then iteratively solved for each set of terminal biases, until a convergence threshold is achieved for the potential and charge concentrations.

In addition to the mobile charge and dopants in the graphene layer, we account for the existence of puddles \[26,27\]. Their associated charge density, $N_p$, is assumed constant and added to both electron and hole charge densities \[28\]. In this way, puddles impact on the overall graphene layer conductivity while conserving a neutral net charge character.

\[\text{Figure 1. Schematic of the simulated GFET and the characteristic resistances of the device. The dashed and dotted rectangles indicate the regions used for the different simulations. While the dotted rectangle only encompasses the channel region, the dashed one includes the access regions.}\]

2.2. Validation

To assess the capability of the numerical simulator to reproduce and explain the experimental results, we have first validated it against the devices fabricated in \[29,30\]. Both are GFETs based on monolayer graphene embedded between a SiO$_2$ layer, which acts as a substrate, and a Y$_2$O$_3$ layer, which acts as a front gate dielectric. In both cases, this Y$_2$O$_3$ layer is 5 nm thick while the substrate is 300 nm thick in \[29\], and 286 nm thick in \[30\]. For the device presented in \[29\], the distance between the source and drain contacts is 1.5 $\mu$m and the front gate length is 600 nm, while in \[30\] the device is 8.2 $\mu$m long and its front gate is 7 $\mu$m long. In other words, in both experimental devices the gate contact does not cover the whole region between source and drain contacts, thus creating two symmetrical under-lapped regions at both channel edges; namely, the device access regions. To reproduce the data reported in \[29\], the same mobility is assumed for both types of carriers, electrons and holes ($\mu = \mu_n = \mu_p$) with a value of 90 cm$^2$/Vs, and a puddle charge density of $7 \cdot 10^{11}$ cm$^{-2}$ is considered. N-type chemical doping of $10^{12}$ cm$^{-2}$ is defined for the graphene layer. To account for the graphene-metal contact resistances, which are in series with the total resistance of the structure, $R_T$, we include two additional 100 nm long N-type doped regions ($5 \cdot 10^{10}$ cm$^{-2}$) in both source and drain ends \[31\]. The back gate is grounded and $V_{DS}$ is set to 0.1 V. To fit the data presented in \[30\], the values used are $\mu = 1091$ cm$^2$/Vs, $N_p = 8 \cdot 10^{11}$ cm$^{-2}$ and the graphene layer chemical doping is set to $10^{11}$ cm$^{-2}$. The back gate is also grounded and $V_{DS}$ is set to 0.05 V. The experimental and simulated transfer characteristics are shown in Figure 2a \[29\] and Figure 2b \[30\]. The simulated I-V characteristics match very accurately with the experimental results in the whole range of biases and are able to catch the transfer response of the electron and hole branches, especially in Figure 2b.
2.3. Access Region Analysis

As mentioned in Section 1, the existence of access regions and puddles is a very common scenario in the experimental realization of GFETs due to the difficulties to precisely control the fabrication process in this early stage of the technology. They modify the behaviour of the transistors, in many cases determining their performance, and therefore deserving a particular attention that is usually obliterated. Hence, once the numerical simulator has been validated, we now proceed to analyse the effect of the access regions.

2.3.1. Including the Access Regions

To begin with, we have considered a test structure where the front gate covers the whole device length (i.e., suppressing the access regions) and compared the results with those obtained later when access regions are included. These scenarios are illustrated in Figure 1 by the dotted and dashed frames respectively. The material stack comprises a monolayer graphene sandwiched between a 3 nm thick HfO$_2$ layer (front gate insulator) and a 27 nm thick SiO$_2$ layer (back gate insulator). The front gate, which determines the channel length ($L_{Chn}$), is 100 nm long and both access regions are 35 nm long ($L_{Acc}$). Electron and hole mobilities are equal ($\mu = 1500$ cm$^2$/Vs) and no chemical doping or puddle charge density is considered in the graphene layer.

The transfer characteristic of the device without access regions is depicted in Figure 3a for different values of $V_{DS}$. As can be observed, the device exhibits the ambipolar V-shaped $I - V$ response of an ideal GFET. The minimum of the $I - V$ curve defines the Dirac voltage ($V_{Dirac}$) that is shifted to larger $V_{FG}$ when $V_{DS}$ increases. The behaviour is perfectly symmetric with respect to $V_{Dirac}$, reflecting the symmetry between electron and hole properties.

Next, the GFET including the access regions is investigated. The resulting transfer characteristic is shown in Figure 3b. Comparing Figure 3b and Figure 3a, a marked variation of the GFET response is observed. First, there is a notable decrease in the values of $I_{DS}$, around a factor $\times 100$. Second, the transfer characteristic shows a saturation trend for high $|V_{FG}|$ which resembles much better the experimental response. Third, and more important, the $I - V$ characteristic is no longer symmetric with respect to $V_{Dirac}$, though the mobility is identical for both kinds of carriers.
To provide insights into these changes, the resistance of the different regions of the device are calculated. Figure 4 shows their values for $V_{DS} = -0.1$ V and $V_{DS} = -0.2$ V. Mirror symmetric behaviour is observed for positive $V_{DS}$. The access region resistances, $R_{S, Acc}$ and $R_{D, Acc}$, show values comparable with the channel resistance, $R_{Chn}$. At the Dirac voltage, where the channel resistivity is the highest, $R_{Chn}$ commands the series association, but still the access regions have a noticeable contribution. For $|V_{FG} - V_{Dirac}| > 0.1$ V the total resistance is mainly determined by $R_{S, Acc}$ and $R_{D, Acc}$. Consequently, the total resistance ($R_T$) is not controlled just by the channel conductivity and, therefore, by the gate terminal. The weak dependence of $R_{S, Acc}$ and $R_{D, Acc}$ on $V_{FG}$ is reflected in the $I_{DS}$ trend to saturation. As the values of $R_{S, Acc}$ and $R_{D, Acc}$ are higher than the channel resistance, a larger fraction of $V_{DS}$ drops in the access regions. This fact reduces the potential at the channel edges with respect to the no-access-regions scenario, reducing the output current. In addition, the $R_{Acc} - V_{FG}$ dependence is not symmetric, so neither are the access region potential drops, resulting into a non-symmetric reduction of the output current, that is, an asymmetric $I_{DS} - V_{FG}$ curve shown in Figure 3b. This lack of equivalence between the source and drain access regions is explored in detail in the following section.

### 2.3.2. Gate Misalignment

In the previous section, we assumed that the gate is perfectly aligned in the middle of the channel leading to identical source and drain access regions ($L_S = L_D = L_{Acc}$) at both ends. A more realistic scenario should consider the impact of having non-equal $L_S$ and $L_D$, enabling us to test the non-equivalent role of $R_{S, Acc}$ and $R_{D, Acc}$ on the GFET response. For this purpose, we have analysed GFETs where the top gate contact is not placed in the centre of the structure, resulting in access regions of different length. In particular, we have kept $L_S$ (or $L_D$) equal to 35 nm while $L_D$ (or $L_S$) is modified. Specifically, we considered four scenarios: (i) short source, (ii) short drain, (iii) long source and (iv) long drain. The length of the short and long regions is set to 17.5 nm and 70 nm,
respectively. The \( I_{DS} - V_{FG} \) curves, along with the resistances \( R_{S,Acc} \), \( R_{D,Acc} \) and \( R_{Chn} \) obtained in each case, are depicted in Figure 5.

![Figure 5](image_url)

**Figure 5.** Transfer response (**a,b**) and structure resistances (**c,d**) as a function of the gate bias. These results are obtained reducing the length of either the source (**a,c**, solid lines) or drain access region (**b,d**, dashed lines) down to 17.5 nm, and increasing the length of either the source (**a,c**, solid lines) or the drain access region (**b,d**, dashed lines) up to 70 nm.

As expected, there are significant differences between devices. Shortening either the source or the drain access regions results in a higher output current (Figure 5a) and reduces both its saturation and its asymmetry with respect to the elongated scenario (Figure 5b). When comparing the shorter regions (Figure 5a) it is clearly observable that the \( L_{S} = 17.5 \) nm device (solid lines) has a more symmetric response than the \( L_{D} = 17.5 \) nm (dashed lines). This is more evident for \( V_{DS} = 0.1 \) V and emphasizes the role of the source access region with respect to the drain access region. An equivalent conclusion can be achieved from the elongated devices (Figure 5b). The longer \( L_{S} \) results in an increased asymmetry between both branches. These results can be explained by analysing the resistances of the structure. Figure 5c,d show \( R_{S,Acc} \), \( R_{D,Acc} \) and \( R_{Chn} \) as a function of \( V_{FG} \) for \( V_{DS} = 0.1 \) V. When any access region is shortened (Figure 5c), its resistance is similar or lower than the channel resistance regardless \( V_{FG} \). The longer region resistance controls the total current (except for \( V_{FG} \) close to zero). When one of the regions is enlarged this effect is emphasized. The transfer responses in Figure 5b are clearly saturated due to the dominant role in the total conductivity of the longer access region.

2.3.3. Impact of Electrostatic Doping and Puddles

To reduce the impact of the access regions in the overall device performance, it is possible to increase their conductivity by means of an electrostatic doping using the back-gate terminal. In the following we analyse how the back gate influences the GFET behaviour. Figure 6 shows the transfer characteristic for three different values of \( V_{BG} \): \(-1 \) V, \( 0 \) V and \( 1 \) V (solid lines). For \( V_{BG} = 0 \) V the results are quite similar to the scenario without back gate. In the other two cases, depending on the polarity of \( V_{BG} \), electrons or holes are accumulated in the graphene layer. As a result, the P-type (N-type) branch
is enhanced for $V_{BG} = -1$ V ($V_{BG} = 1$ V), regardless the value of $V_{DS}$. As in the previous scenario, the origin of this behaviour can be traced back to the resistance associated with the access regions.

![Image](image_url)

**Figure 6.** $I_{DS} - V_{FG}$ characteristics of the complete structure when three different back gate potentials are used ($-1$ V (a), 0 V (b) and 1 V (c)). Solid lines correspond to the device without puddles and dashed lines to the device with $N_p = 10^{12}$ cm$^{-2}$.

Figure 7 depicts the device resistances for different $V_{BG}$ and $V_{DS} = -0.1$ V (without puddles, solid lines). For $|V_{BG}| = 1$ V the total resistance near the Dirac voltage is dominated by $R_{Chn}$. When $V_{FG}$ is increased above $V_{Dirac}$, the symmetry of $R_{Chn}$ is kept since it is mostly controlled by the front gate, while the asymmetry of $R_{S,Acc}$ and $R_{D,Acc}$ is exacerbated due to the electrostatic doping, giving rise to the large asymmetry observed in the transfer response, in Figure 6. In particular, the asymmetric step-like dependence of the access resistances on $V_{FG}$ (for $V_{BG} \neq 0$ V) is the result of the electrostatic competition between the front and back gates to control the access regions closer to the channel. When $V_{FG}$ and $V_{BG}$ have the same polarity, they add their electric forces to increase the carrier density in the aforementioned zones, increasing the conductivity and therefore lowering the whole access resistance. However, if $V_{FG}$ is opposite to $V_{BG}$, both gates compete to accumulate different types of charges, resulting in a depleted region close to the channel edges that decreases the conductivity and increases the overall access region resistances. An equivalent conclusion was achieved in [26] where a strong modulation of the total resistance by two additional gates is observed, as in Figure 7.

An additional aspect that cannot be overlooked is the effect of the presence of puddles in the graphene layer [27,32]. To shed light on this issue Figure 6 includes the $I_{DS} - V_{FG}$ response when a puddle charge density of $N_p = 10^{12}$ cm$^{-2}$ is considered (dashed lines). Two major changes are observed after including the puddles: (i) the total current is increased, and (ii) the asymmetry is clearly reduced. These changes derive from the equal contribution of puddles to the conductivity of both electrons and holes, and explain why the $I - V$ curves of some experimental devices are reasonably symmetric close to the Dirac voltage, where the conductivity of puddles is dominant. In this situation, the conductivity of the whole graphene layer is increased for electrons and holes, in contrast with the electrostatic doping generated by the back gate. This non-selective improvement of the conductivity is translated into the resistances of the device: Figure 7 includes the $R - V_{FC}$ relation for $N_p = 10^{12}$ cm$^{-2}$ (dashed lines). The step-like behaviour of $R_{S,Acc}$ and $R_{D,Acc}$ is softened when the puddles are included, resembling the $V_{BG} = 0$ V case.
2.3.4. RF Performance

Finally, to determine the impact of the access regions in the RF performance, we evaluate the cut-off frequency, $f_T$, as a RF figure of merit (FoM). The value of $f_T$ is calculated as in [33,34]:

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{fg}}$$

where $g_m$ is the transconductance and $C_{fg}$ the front gate capacitance.

Figure 8 shows $f_T$ as a function of $V_{FG}$ under two scenarios: no puddles (solid lines) and $N_p = 10^{12}$ cm$^{-2}$ (dash-dotted lines). To assess the impact of the access regions, the performance of the intrinsic device (structure indicated by the dotted rectangle in Figure 1) is depicted too (dashed lines). In addition, to evaluate the magnitude of the calculated values, the experimental measurements of $f_T$ reported in [35] and [36] are indicated by the arrows on the right side axis of Figure 8. Despite the device structure and the bias conditions are different, the channel lengths of these experimental devices are similar to the ones simulated here (144 nm [35] and 140 nm [36]), and therefore constitute a good reference. Importantly, a de-embedding procedure was carried out for the RF measurements of these experimental devices by using specific “short” and “open” structures with identical layouts in order to remove the effects of the parasitics associated with the pads and connections, but not the contact and access region resistances.
Figure 8. $f_T$ of the back-gated device with access regions under two scenarios: no puddles (solid lines) and $N_p = 10^{12}$ cm$^{-2}$ (dash-dotted lines). The values obtained for the intrinsic device are depicted by the purple dashed line. The arrows labelled by marks on the right side axis indicate the values of $f_T$ extracted from [35] (circle) and [36] (square and triangle). The yellow line indicates the physical limit for graphene $v_F/2\pi L$, determined by the transit time $L/v_F$, with the Fermi velocity $v_F \approx 10^8$ cm/s and $L = 100$ nm (squares).

Including the access regions results in a quite different response compared with the intrinsic device, as the associated parasitic resistances provoke a bias dependent decay of $f_T$. Considering the scenario without puddles, when the back gate is properly biased, $f_T$ is considerably improved. If we analyse Figure 8 in combination with Figure 7, those combinations of $V_{FG}$, $V_{BG}$ for which the $R_S - V_{FG}$ $(R_D - V_{FG})$ curve shows its minimum values, are those for which $f_T$ shows a greater improvement. When $R_S (R_D)$ is higher, $f_T$ is spoiled with respect to the $V_{BG} = 0$ V case. This relation between the access region conductivity and the improvement of the RF performance was experimentally observed in [21] where a higher $f_T$ was demonstrated when a GFET with two additional electrodes was properly biased to control such conductivity. When puddles are included, the channel conductivity increases, what reduces the control of the back-gate bias, and simultaneously results in a more symmetric $f_T - V_{FG}$ dependence.

3. Conclusions

GFETs have been thoroughly studied in order to assess the impact of the access regions in the device performance. The validation of our approach against two experimental devices spotlights the importance of these regions as well as the presence of puddles to reproduce the state-of-the-art technology. When the access regions are considered, the transfer response reveals a lower, saturated and asymmetric $I_{DS} - V_{FG}$ characteristic that is not observed in their absence. To explore the impact of a variable conductivity of these regions we have included a back gate in the structure able to introduce an electrostatic doping. The back gate increases the output current as well as the asymmetry of the transfer characteristic. The latter effect is explained in terms of the competition of the back and front gates that results in a depletion of the amount of carriers close to the channel edges when both biases have an opposite polarity. The influence of puddles is also theoretically investigated, observing that they reduce the asymmetry of $I_{DS} - V_{FG}$.

The analysis of the impact of the access regions and puddles have been extended to the prediction of the cut-off frequency to assess the properties of GFETs for potential RF applications. Our results reveal an important degradation of the $f_T - V_{FG}$ relation due to access regions. The application of an appropriate back gate bias can tune the access region conductivity generating a remarkable improvement in the RF performance. The presence of puddles also mitigates this degradation, but neglects the possibility of tuning the access regions conductivity.
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Abbreviations

The following abbreviations are used in this manuscript:

2DM Two-dimensional material
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor
GFET Graphene Field-Effect Transistors
RF Radio-Frequency

References

1. Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S.K.; Colombo, L. Electronics based on two-dimensional materials. *Nat. Nanotechnol.* 2014, 9, 768–779. [CrossRef] [PubMed]
2. Lee, S.; Zhong, Z. Nano electronic circuits based on two-dimensional atomic layer crystals. *Nanoscale* 2014, 6, 13283–13300. [CrossRef] [PubMed]
3. Neto, A.H.C.; Guinea, F.; Pereira, N.M.R.; Novoselov, K.S.; Geim, A.K. The electronic properties of graphene. *Rev. Mod. Phys.* 2009, 81, 109–162. [CrossRef]
4. Guerriero, E.; Pedrinazzi, P.; Mansouri, A.; Habibpour, O.; Winters, M.; Rorsman, N.; Behnam, A.; Carrión, E.A.; Pesquera, A.; Centeno, A.; et al. High-Gain Graphene Transistors with a Thin AlOx Top-Gate Oxide. *Sci. Rep.* 2017, 7, 2419. [CrossRef] [PubMed]
5. Lin, Y.M.; Jenkins, K.A.; Valdes-Garcia, A.; Small, J.P.; Farmer, D.B.; Avouris, P. Operation of Graphene Transistors at Gigahertz Frequencies. *Nano Lett.* 2009, 9, 422–426. [CrossRef] [PubMed]
6. Meric, I.; Han, M.Y.; Young, A.F.; Ozyilmaz, B.; Kim, P.; Shepard, K.L. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nat. Nanotechnol.* 2008, 3, 654–659. [CrossRef] [PubMed]
7. Rizzi, L.G.; Bianchi, M.; Behnam, A.; Carrión, E.; Guerriero, E.; Polloni, L.; Pop, E.; Sordan, R. Cascading Wafer-Scale Integrated Graphene Complementary Inverters under Ambient Conditions. *Nano Lett.* 2012, 12, 3948–3953. [CrossRef] [PubMed]
8. Pandey, H.; Shaygan, M.; Sawallich, S.; Kataria, S.; Wang, Z.; Noculak, A.; Otto, M.; Nagel, M.; Negra, R.; Neumaier, D.; et al. All CVD Boron Nitride Encapsulated Graphene FETs With CMOS Compatible Metal Edge Contacts. *IEEE Trans. Electron Devices* 2018, 65, 4129–4134. [CrossRef]
9. Wu, Y.; Zou, X.; Sun, M.; Cao, Z.; Wang, X.; Huo, S.; Zhou, J.; Yang, Y.; Yu, X.; Kong, Y.; et al. 200 GHz Maximum Oscillation Frequency in CVD Graphene Radio Frequency Transistors. *ACS Appl. Mater. Interfaces* 2016, 8, 25645–25649. [CrossRef]
10. Cheng, R.; Bai, J.; Liao, L.; Zhou, H.; Chen, Y.; Liu, L.; Lin, Y.C.; Jiang, S.; Huang, Y.; Duan, X. High-frequency self-aligned graphene transistors with transferred gate stacks. *Proc. Natl. Acad. Sci. USA* 2012, 109, 11588–11592. [CrossRef]
11. Lin, Y.M.; Dimitrakopoulos, C.; Jenkins, K.A.; Farmer, D.B.; Chiu, H.Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* 2010, 327, 662. [CrossRef] [PubMed]
12. Georgiou, T.; Jalil, R.; Belle, B.D.; Britnell, L.; Gorbachev, R.V.; Morozov, S.V.; Kim, Y.J.; Gholina, A.; Haigh, S.J.; Makarovsky, O.; et al. Vertical field-effect transistor based on graphene–WS2 heterostructures for flexible and transparent electronics. *Nat. Nanotechnol.* 2013, 8, 100–103. [CrossRef] [PubMed]
13. Wang, Z.; Uzlu, B.; Shaygan, M.; Otto, M.; Ribeiro, M.; Marin, E.G.; Iannaccone, G.; Fiori, G.; Elsayed, M.S.; Negra, R.; et al. Flexible One-Dimensional Metal–Insulator–Graphene Diode. *ACS Appl. Electron. Mater.* 2019, 1, 945–950. [CrossRef]
14. Liao, L.; Bai, J.; Cheng, R.; Lin, Y.C.; Jiang, S.; Huang, Y.; Duan, X. Top-Gated Graphene Nanoribbon Transistors with Ultrathin High-k Dielectrics. *Nano Lett.* 2010, 10, 1917–1921. [CrossRef] [PubMed]
15. Mayorov, A.S.; Gorbachev, R.V.; Morozov, S.V.; Britnell, L.; Jalil, R.; Ponomarenko, L.A.; Blake, P.; Novoselov, K.S.; Watanabe, K.; Taniguchi, T.; et al. Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature. *Nano Lett.* **2011**, *11*, 2396–2399. [CrossRef] [PubMed]

16. Farmer, D.B.; Lin, Y.M.; Avouris, P. Graphene field-effect transistors with self-aligned gates. *Appl. Phys. Lett.* **2010**, *97*, 013103. [CrossRef]

17. Feng, Z.; Yu, C.; Li, J.; Liu, Q.; He, Z.; Song, X.; Wang, J.; Cai, S. An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors. *Carbon* **2014**, *75*, 249–254. [CrossRef]

18. Fiori, G.; Iannaccone, G. Multiscale Modeling for Graphene-Based Nanoscale Transistors. *Proc. IEEE* **2013**, *101*, 1653–1669. [CrossRef]

19. Di Bartolomeo, A.; Giubileo, F.; Romeo, F.; Sabatino, P.; Carapella, G.; Iemmo, L.; Schroeder, T.; Lupina, G. Graphene field-effect transistors with niobium contacts and asymmetric transfer characteristics. *Nanotechnology* **2015**, *26*, 475202. [CrossRef]

20. Jain, S.; Dutta, A.K. Resistance-Based Approach for Drain Current Modeling in Graphene FETs. *IEEE Trans. Electron Devices* **2015**, *58*, 1523–1533. [CrossRef]

21. Ancona, M.G. Electron Transport in Graphene From a Diffusion-Drift Perspective. *IEEE Trans. Electron Devices* **2010**, *57*, 681–689. [CrossRef]

22. Curatola, G.; Doornbos, G.; Loo, J.; Ponomarev, Y.; Iannaccone, G. Detailed Modeling of Sub-100-nm MOSFETs Based on Schrödinger DD Per Subband and Experiments and Evaluation of the Performance Gap to Ballistic Transport. *IEEE Trans. Electron Devices* **2005**, *52*, 1851–1858. [CrossRef]

23. Ge, J.; Hwang, J.; Yu, C.; Wang, Z.; Chen, X.; Gao, J.; Liu, X.; Zou, W.; Peng, L.; Xie, T.; et al. Direct observation of spatial charge inhomogeneity in graphene field-effect transistor using current-voltage and capacitance-voltage measurements. *Appl. Phys. Lett.* **2012**, *101*, 213103. [CrossRef]

24. Venica, S.; Zanato, M.; Driussi, F.; Palestri, P.; Selmi, L. Modeling electrostatic doping and series resistance in graphene-FETs. In *Proceedings of the 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*; Nuremberg, Germany, 6–8 September 2016.
35. Liao, L.; Lin, Y.C.; Bao, M.; Cheng, R.; Bai, J.; Liu, Y.; Qu, Y.; Wang, K.L.; Huang, Y.; Duan, X. High-speed graphene transistors with a self-aligned nanowire gate. *Nature* 2010, 467, 305–308. [CrossRef]

36. Wu, Y.; Jenkins, K.A.; Valdes-Garcia, A.; Farmer, D.B.; Zhu, Y.; Bol, A.A.; Dimitrakopoulos, C.; Zhu, W.; Xia, F.; Avouris, P.; et al. State-of-the-Art Graphene High-Frequency Electronics. *Nano Lett.* 2012, 12, 3062–3067. [CrossRef]

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