A Highly Efficient and Linear mm-Wave CMOS Power Amplifier Using a Compact Symmetrical Parallel–Parallel Power Combiner With IMD3 Cancellation for 5G Applications

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ABSTRACT This paper presents a fully integrated linear power amplifier (PA) in a 65-nm CMOS process for mm-wave 5G applications. The proposed linear PA employs a compact symmetrical 4-way parallel–parallel power combiner with a third-order intermodulation distortion (IMD3) cancellation method to achieve high linear output power with a high power-added efficiency (PAE). An on-chip 4-way parallel–parallel power combiner, which combines the output power from 8-unit PAs, is designed with a compact footprint (241 µm × 241 µm). Conventional series power-combining transformer based power combiners have poor symmetrical performance for the amplitude and phase of the input impedance among unit PAs owing to the parasitic effects of the power combiners. However, the proposed parallel–parallel power combiner, which is based on parallel power-combining transformer structures, shows good symmetrical performances among unit PAs. Moreover, an IMD3 cancellation method using a parallel–parallel power combiner is proposed in this work. The proposed IMD3 cancellation method can support high-order modulation signals without increasing the complexity and reduce the dependence for digital predistortion (DPD). Consequently, the proposed linearization method obtains a high linear $P_{\text{OUT}}$ and PAE without DPD. The PA in 65-nm CMOS demonstrates a saturated output power ($P_{\text{SAT}}$) of 23.2 dBm, a 15.9-dB power gain, a 1-dB compressed output power ($P_{\text{O},1\text{dB}}$) of 22 dBm, and a peak power-added efficiency (PAE) of 33.5% at 28 GHz. The measured error vector magnitude with 100 Msym/s of 256/512-QAM is $-31.2/-32.1$ dB with average output power of $18.02/17.73$ dBm, average PAE of $17.6/16.1\%$, and adjacent channel power ratio (ACPR) of $-30/-33.1$ dBc without DPD. To the best of the authors' knowledge, the proposed PA demonstrates high output power with the highest PAE performance supporting 256/512-QAM compared to the recently published fully integrated mm-wave 5G CMOS PAs.

INDEX TERMS CMOS technology, mm-wave, 5G, power combiner, linearity, power amplifier, IMD3 cancellation, 65 nm.

I. INTRODUCTION

In the past several decades, the demands for high data rates, a massive Internet of Things, and ultra-reliable low-latency have driven the tremendous development of mobile technologies [1]–[11]. With the roll-out of the new generation of wireless communication technology, i.e., 5G applications, expected soon, various mm-wave bands range from 24 to 80 GHz have been considered and evaluated for 5G systems. According to the Federal Communications Commission (FCC), the 28 GHz band has emerged as one of the candidates among multiple mm-wave frequency bands for 5G system in most countries [12], [13].

To keep up with the needs, mm-wave transceivers integrated circuits (ICs) for 5G systems have been intensively studied. Moreover, to fulfill these demands, an orthogonal
Recently reported several PAs with linearization techniques can be required in increasing DPD complexity [41]–[44]. However, this technique and phase distortion by pre-distorting the input stimulus are frequently used in transmitters to correct the amplitude distortion technique of digital predistortion (DPD) loop-back is secondary winding. Parallel power-combining transformers (PCTs) are combined to improve imbalances in the unit PAs with a small size. Two parallel power combiner is proposed to mitigate these issues, a series (SCT)–parallel power combiner. Section III introduces the detailed design and analysis of the proposed PA are presented. Finally, this paper is concluded in Section VI.

II. ANALYSIS OF SYMMETRICAL PERFORMANCE FOR PROPOSED POWER COMBINER
Before delving into the proposed 4-way parallel–parallel power combiner, we review previously reported power combiner schemes. Fig. 1(a), (b), and (c) show conceptual diagrams of the transformer-based radial structures, SCTs, modified-SCTs. In addition, Fig. 1 includes the unwanted parasitic capacitance in the primary and secondary windings. Typically, to improve the linearity, the external linearization technique of digital predistortion (DPD) loop-back is frequently used in transmitters to correct the amplitude and phase distortion by pre-distorting the input stimulus with their inverse equivalents. However, this technique can be required in increasing DPD complexity [41]–[44]. Recently reported several PAs with linearization techniques (e.g., transformer-based amplitude-to-phase modulation (AM-PM) correction, inductive source degeneration, PMOS varactor AM-PM compensation, and second harmonic termination) for mm-wave 5G applications have been proposed [30]–[33], [46]. A transformer-based AM-PM correction technique provides optimum neutralization of the gate-drain capacitance (Cgd) in a common-source (CS) configuration by adopting a reconfigurable and tunable coupling-coefficient-based transformer [30]. An inductive source degeneration was proposed to improve and minimize the amplitude-to-amplitude modulation (AM-AM)/AM-PM response of the output stage [31]. An AM-PM compensation scheme with a PMOS varactor is used at the input of the amplifying stages to reduce the variation in the input capacitance [32]. One-stage differential structure PAs with harmonic control circuits is proposed to minimize the second harmonics produced by the CS amplifier at the drain and source [33], [46]. The AM-AM/AM-PM characteristics or inter-modulation (IM) distortions have been analyzed and improved in these works. Nevertheless, these PAs may increase design complexity or require additional circuits for a linearization technique. To improve linearity without adding design complexity, the IMD3 cancellation method using a parallel–parallel power combiner is proposed. This paper presents a fully integrated 28-GHz linear CMOS PA using a compact symmetrical 4-way parallel–parallel power combiner with an IMD3 cancellation method to obtain a high linear PoUT with a high PAE. The implemented PA delivers an output power of saturated output power (PsAT) of 23.5/23.2 dBm, power gain of 16.6/15.9 dB, and peak PAE of 35.5/33.5% at 27.3/28GHz, respectively.

This paper is an extension of [48]. In [48], the concept of a symmetrical 4-way parallel–parallel power combiner and the IMD3 cancellation method is introduced. In this paper, the detailed design and analysis of the proposed PA are presented. This paper is organized as follows. Section II covers a comparative analysis of the PCT-based proposed power combiner and SCT-based power combiner. Section III introduces the operation of the IMD3 cancellation method. In addition, the detailed architecture and implementation of the proposed linear PA are presented in Section III. In Section IV, the measurement results of the proposed mm-wave 5G CMOS PA are presented. Finally, this paper is concluded in Section VI.
intersection of the input and output lines may cause stability issues and a complex layout is required, the case of Fig. 1(a) is excluded in the analysis process.

For the dotted terminals between the primary and secondary windings in Fig. 1(b) and (c), the minus side of primary winding through the unwanted parasitic capacitors is connected to the middle point of the secondary winding, while the other minus side of the primary winding is directly connected to the ground. Thus, this configuration with unwanted parasitic capacitors causes an imbalance effect, resulting in an imbalance performance in the amplitude and phase of the input impedance at each primary winding. In particular, as the operating frequency increases, the parasitic capacitor dramatically affects the overall performance. The proposed 4-way parallel–parallel power combiner for mm-wave 5G applications is shown in Fig. 1(d). As shown in Fig. 1(d), the proposed power combiner employs PCTs and a parallel T-Line. For the proposed power combiner, two-unit PAs are connected to each primary winding of the two PCTs; i.e., the output powers from 8-unit PAs are combined by two PCTs to generate a high output power. In addition, the outputs of the two PCTs are summed by a parallel T-line combiner. In the contrast to the other combiners shown in Fig. 1(b) and (c), the configuration of each primary side is identical to the unwanted parasitic capacitors in this parallel–parallel power combining approach, resulting in the minimization of imbalances.

Additionally, the topologies shown in Fig. 1(b), (c), and (d) can be considered as two-stage power-combining topologies. As shown in Fig. 1, two-stage power-combining topologies comprise the 1st stage and 2nd stages. SCT is adopted in Fig. 1(b) and (c) for the 1st stage of the power-combining topology, while a PCT is used in the 1st stage of Fig. 1(d). In the 2nd stage of the power-combining topology shown in Fig. 1(b), two SCTs are connected in series at the secondary winding, resulting in a SCT topology with four primary windings. In contrast, for the 2nd stage of the power-combining topology in Fig. 1(c) and (d), two SCTs or two PCTs are connected in parallel. The parallel connection in the 2nd stage in the power-combining topology can be simply estimated, as this configuration does not cause an imbalance performance between two SCTs or PCTs, owing to the symmetrical physical geometry. Thus, only SCT and PCT configurations in the 1st stage of the power-combining topology are covered to analyze the input impedance of these structures. Many research works have been dedicated for the analysis of SCTs and PCTs [51]–[54]. However, these works were focused on characteristics of input impedance and passive efficiency especially at lower gigahertz frequencies. Thus, high frequency effects owing to parasitic capacitances were not considered. In this work, imbalance performances of the input impedances at each primary winding in the SCT and PCT are analyzed with the unwanted parasitic capacitors between the primary and secondary windings. Fig. 2 shows

FIGURE 1. Conceptual diagrams of the (a) transformer-based radial structure, (b) series power-combining transformers (SCTs), (c) modified-SCTs, and (d) the proposed parallel–parallel power combiner for combining 8-unit PAs.
the equivalent circuits for the single-ended cases of the PCT and SCT with the unwanted parasitic capacitors. Fig. 2 is modeled by the net inductance of $L_{1a}/L_{1b}$ and $L_{2a}/L_{2b}$ for the primary and secondary winding, including the equivalent series resistors $R_{1a}/R_{1b}$ and $R_{2a}/R_{2b}$. $M_{a}/M_{b}$ are the mutual inductance, and $C_{a}/C_{b}$ are the parasitic capacitor between the primary and secondary windings. In the case of a PCT with equivalent circuits, as shown in Fig. 2(a), if $V_{1a} = V_{1b} = V_1$, $I_{1a} = I_{1b} = I_1$, $I_{L1a} = I_{L1b} = I_{L1}$, $R_{1a} = R_{1b} = R_1$, $L_{1a} = L_{1b} = L_1$, and $M_a = M_b = M$, the input and output voltages are described as follows:

$$V_1 = (R_1 + j\omega L_1)I_{L1} + j\omega M I_{L2}$$  \hspace{1cm} (1)

$$V_2 = (R_2 + j\omega L_2)I_{L2} + 2j\omega M I_{L1}$$  \hspace{1cm} (2)

where $R_L$ is the output resistance, which is typically 50 Ω.

If $V_{ca} = V_{cb} = V_c$ and $C_a = C_b = C$, $I_C$ can be defined as

$$I_c = j\omega CV_c = j\omega C (V_1 - V_2)$$  \hspace{1cm} (3)

According to Kirchhoff’s current law (KCL) at the primary winding node in Fig. 2(a), $I_{L1}$ can be defined as

$$I_1 = I_{L1} + I_c,$$

$$I_{L1} = I_1 - j\omega C (V_1 - V_2)$$  \hspace{1cm} (4)

In addition, by considering KCL at the secondary winding node in Fig. 2(a), $I_{L2}$ can be defined as

$$2I_c = I_2 + I_{L2},$$

$$I_{L2} = 2j\omega C (V_1 - V_2) - I_2$$  \hspace{1cm} (5)

If $Z_{IN1} = Z_{IN1a} = Z_{IN1b}$, the input impedance ($Z_{IN1}$) in Fig. 2(a) can be expressed as

$$Z_{IN1} = \frac{V_1}{I_1} = R_{IN1} + jX_{IN1}$$  \hspace{1cm} (6)

where $R_{IN1}$ and $X_{IN1}$ is the real and imaginary parts of $Z_{IN1}$, respectively. The relationship between the voltages and currents for the PCT is given by (7), as shown at the bottom of the page. Because the derivation of the equation for $Z_{IN1}$ is too complex to obtain the summarized form (6), $Z_{IN1}$ is calculated and plotted using MATLAB by solving the linear matrix equation of (7) and $V_2 = R_L I_2$.

By considering $j\omega C_a V_{ca} = I_{ca}$ and $j\omega C_b V_{cb} = I_{cb}$, applying KCL to the nodes in Fig. 2(b) gives

$$I_{1a} = I_{L1a} + I_{ca}, \quad I_{ca} = I_2 + I_{L2a},$$

$$I_{1b} = I_{L1b} + I_{cb}, \quad I_{cb} + I_{L2b} = I_{L2b}$$  \hspace{1cm} (11)

$$\begin{bmatrix}
1 + 2\omega^2 MC + j\omega C (R_1 + j\omega L_1) \\
\omega^2 2MC + j2\omega C(R_2 + j\omega L_2)
\end{bmatrix}
\begin{bmatrix}
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
\end{bmatrix}
= \begin{bmatrix}
\begin{bmatrix}
R_1 + j\omega L_1 & -j\omega M \\
j\omega 2M & -(R_2 + j\omega L_2)
\end{bmatrix}
\end{bmatrix}
\begin{bmatrix}
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}
\end{bmatrix}$$  \hspace{1cm} (7)
Additionally, applying Kirchhoff’s voltage law (KVL) to each primary winding node in Fig. 2(b) gives
\[
V_{1a} = V_{ca} + V_2, \\
V_{1b} = V_{cb} + V_{2b} = V_{cb} + (R_{2b} + j\omega L_{2b}) I_{L2b} + j\omega M_2 I_{L1b}
\]
(12)

If \( I_{1a} = I_{1b} = I_1 \), \( R_{1a} = R_{1b} = R_1 \), \( R_{2a} = R_{2b} = R_2 \), \( L_{1a} = L_{1b} = L_1 \), \( L_{2a} = L_{2b} = L_2 \), \( M_a = M_b = M \), and \( C_a = C_b = C \), \( Z_{IN1a}/Z_{IN1b} \) of the Fig. 2(b) is expressed as
\[
Z_{IN1a} = \frac{V_{1a}}{I_1} = R_{IN1a} + j\omega X_{IN1a} \\
Z_{IN1b} = \frac{V_{1b}}{I_1} = R_{IN1b} + j\omega X_{IN1b}
\]
(13)

If \( Z_1 = R_1 + j\omega L_1 \) and \( Z_2 = R_2 + j\omega L_2 \), using (8), (9), and (10), \( V_{1a} \), \( V_{1b} \), and \( V_2 \) can be expressed as follows:
\[
\begin{bmatrix}
V_{1a} \\
V_{1b} \\
V_2
\end{bmatrix} = \begin{bmatrix}
Z_1 & j\omega M & 0 & 0 \\
0 & 0 & Z_1 & j\omega M \\
j\omega M & Z_2 & j\omega M & Z_2
\end{bmatrix} \cdot \begin{bmatrix}
I_{L1a} \\
I_{L2a} \\
I_{L1b} \\
I_{L2b}
\end{bmatrix}
\]
(15)

The currents \( I_1 \) and \( I_2 \) in the SCT are given by (16), as shown at the bottom of the page, which can be derived with \( I_{L1a}, I_{L2a}, I_{L1b}, \) and \( I_{L2b} \) by using (10) and (11). The relationship between the voltages and currents for the SCT is given by (17), as shown at the bottom of the page. Additionally, to obtain the calculated \( Z_{IN1a} \) and \( Z_{IN1b} \) in Fig. 2(b), (17) and \( V_2 = R_1 I_2 \) are also solved using MATLAB.

To plot the calculated \( Z_{IN1} \) and \( R_L \) are set as 50 ohm, and all lumped elements are determined by considering the physical layout geometries. In Fig. 2(a) and (b), if \( M_a = M_b = M \), the mutual inductance, \( M \), is set as \( M = k \sqrt{L_1 \cdot L_2} \) \((k = 0.80)\).

If \( L_{1a} = L_{1b} = L_1 \) and \( L_{2a} = L_{2b} = L_2 \), the self-inductances are selected as \( L_1 = 219 \text{ pH} \) and \( L_2 = 210 \text{ pH} \). Moreover, if \( R_{1a} = R_{1b} = R_1 \) and \( R_{2a} = R_{2b} = R_2 \), the parasitic resistances \( R_1 \) and \( R_2 \) are calculated using \( R_1 = \omega L_1/Q_1 \), \( R_2 = \omega L_2/Q_2 \), where \( Q_1 \) and \( Q_2 \) are 15 and 17. In addition, if \( C_a = C_b = C \), the parasitic capacitors between the primary and secondary windings are set as \( C = 60 \text{ fF} \).

To check the effect of the parasitic capacitor in PCT and SCT, the calculated input impedances of the PCT and SCT are plotted, as shown in Fig. 3 and 4. Here, the calculated real and imaginary parts of the input impedances for the PCT and SCT are obtained via (7) and (17) using MATLAB. For the PCT case, the input impedance of one PA is identical to that of the other PA over the frequency range of interest, which indicates that symmetrical performance among PAs can be achieved.

On the other hand, for the SCT, as the frequency ranges increase, the input impedance mismatch increase, leading to the input impedances being unequal from one PA to another PA and, depending on each other.

The proposed power combiner comprises two PCTs and a T-line parallel combiner, adding the \( P \) over the frequency range of interest, which indicates that symmetrical performance among PAs can be achieved. In addition, the spacing between AP and M8 is similar to the spacing between M7 and LI. However, the input impedances mismatch increase, leading to the input impedances being unequal from one PA to another PA and, depending on each other.
factor \( k \), one primary winding (Primary1) is located below the secondary winding, while the other primary winding (Primary2) is located above the secondary winding, resulting in a vertical geometry. Thus, this configuration can reduce the occupied die area. An additional T-line parallel combiner can be simply added, thus minimizing the additional combining loss. The size of the proposed power combiner is \( 241 \, \mu m \times 96 \, \mu m \), which is optimized by considering the frequency band of interest. An 8-\( \mu m \) metal width is chosen for each primary and secondary winding.

To evaluate the performance of the proposed power combiner, the electromagnetic (EM) simulation was performed. As shown in Fig. 6(a), the simulated self-inductances and \( Q \) factors of Primary1 and Primary2 are very close to each other. Additionally, the magnitudes of the transmission coefficients \( (S_{51}, S_{52}, S_{53}) \) and phase differences \( (|\angle S_{51} - \angle S_{52}|, |\angle S_{52} - \angle S_{53}|) \) are shown in Fig. 6(b). Typically, the imbalance of phase and magnitude in the combining networks degrades the power gain, output power, and PAE performance in the PA [48]. However, as shown in Fig. 6(a) and (b), the proposed combiner exhibits very little deviation from each other because of its symmetrical geometry. Thus, the application of the proposed power combiner to the design of the PA is expected to achieve high performances. The simulated \( k \) is approximately 0.8 both between Primary1 and secondary windings and between...
Primary 2 and the secondary winding, as shown in Fig. 6(c). A device parasitic capacitor ($C_P$) is added to the primary sides, as shown in Fig. 5. At 28 GHz, the simulated overall insertion loss of the 4-way parallel–parallel combiner is −0.70 dB, which proves that the proposed power combiner has a low passive loss while occupying a smaller die area. Thus, the proposed compact 4-way parallel–parallel power combiner adds the $P_{OUT}$ from multiple unit PAs with low loss and symmetrical phases/amplitudes. Fig. 7 presents the input impedances ($Z_{IN1}$, $Z_{IN2}$, $Z_{IN3}$, and $Z_{IN4}$) at each port of the proposed power combiner. As indicated in Fig. 7, the tendencies of the simulated results also exhibits small differences in each other. Thus, symmetrical performance of the proposed power combiner is verified by both the simulation and calculation results.

### III. mm-Wave CMOS PA with Proposed Linearization Method

#### A. IMD3 Linearization Method

5G mm-wave systems require highly linear PAs to satisfy the stringent requirements for the error vector magnitude (EVM) and adjacent channel power ratio (ACPR) [12], [13], [31]. In particular, third-order intermodulation distortion (IMD3) significantly affects the in-band linearity (EVM) and output-of-band linearity (ACPR or spectrum regrowth), when a complex modulated signal, high-order QAM, is used as the input.
signal for the transmitter [34]–[38], [41]. Thus, the properties of IMD3 have been analyzed and improved [34]–[38], [41].

For the study of nonlinearity, nonlinear outputs of a nonlinear system are usually analyzed, where a sinusoidal input signal can be assumed as

\[ v_{GS}(t) = V_{GS} + v_{gs}(t) = V_{GS} + A \cos \omega t \]  \hspace{1cm} (18)

In (18), \( A \), \( V_{GS} \), and \( \omega \) are the magnitudes of the input signal, gate–source voltage, and angular frequency, respectively. To obtained form of nonlinear, a nonlinear form can be obtained by applying the Taylor series to the drain current versus \( V_{GS} \):

\[
i_{ds(V_{GS}+v_{gs})} = i_{ds(V_{GS})} + g_{m1}(V_{GS})v_{gs} + g_{m2}(V_{GS})v_{gs}^2 \\
+ \frac{1}{2} \int_{0}^{v_{gs}} (v_{gs} - x)^2 g_{m3}(x + V_{GS})dx \hspace{1cm} (19)
\]

where \( g_{mn} \) is the nonlinearity coefficient of the nonlinear system output. In the last term of (19), \( g_{m3} \) is dominant contributor to IMD3 generation [34]–[38], [41]. With \( g_{m3} \) characteristics represented by impulses, the third-order products of \( i_{ds} \), i.e., \( i_{ds,3} \), can be expressed using the residual term in (19):

\[
i_{ds,3} = \frac{1}{2} A \cos \omega t \int_{0}^{A} (A \cos(\omega t) - x)^2 \\
\times \left( \sum_{i=1}^{N} K_i \delta(x - V_i) \right) dx \hspace{1cm} (20)
\]

where \( K_i \) and \( V_i \) are their magnitude and voltage positions of the impulses \( \delta(\cdot) \), respectively.

The multi-gated transistors (MGTRs) method is widely used to achieve IMD cancellation between MGTRs, which are biased in the class-AB/class-C region for one of the MGTRs/other MGTRs. Furthermore, IMD3 cancellation methods between unit PAs in power combining structures (e.g., SCT and single- and two-winding transformer) have been proposed and verified to improve the linearity [49], [50]. Additionally, if an expansion version of (18)–(20) is applied to the two stages, the input/output characteristics of the two
FIGURE 11. Simulated (a) IMD3 upper and (b) IMD3 lower sides of the power stage \(V_{\text{GCS}} = 0.5\ \text{V}\) with the DA under different DA bias voltages (two-tone signal with a 100-MHz spacing at 28 GHz).

FIGURE 12. Simulated (a) IMD3 upper and (b) IMD3 lower sides for different cases (two-tone signal with a 100-MHz spacing at 28 GHz).

stages, i.e., the driver stage (DA) and power stage in cascade, can be obtained. To improve the linearity in the two stages, an anti-phase method was proposed [38]–[40]. The anti-phase method cancels the nonlinearity of the power stage using the DA, which has a positive sign of \(g_{m3}\). However, to satisfy the stringent requirements for the high-order QAM and OFDM signals from low-output power regions to high-power output power regions, mm-wave 5G CMOS PA still requires an effective linearization method.

Fig. 8 shows the simulated transfer-function derivatives of the transistor (width of 42 \(\mu\text{m}\)) versus the gate-source voltage \(V_{\text{GS}}\). \(g_{mi}\) is \(i\)-th order transconductance. As shown in Fig. 8, the impulse of the \(g_{m3}\), which has either a positive or negative sign, is changed by the \(V_{\text{GS}}\). The \(g_{m3}\) near the \(V_{\text{GS}}\) of 0.3 V has a positive sign, whereas the \(g_{m3}\) near the \(V_{\text{GS}}\) of 0.45 V has a negative sign. Thus, \(g_{m3}\) is initially positive (below a \(V_{\text{GS}}\) of 0.38 V), and as the \(V_{\text{GS}}\) moves to the high-voltage region, \(g_{m3}\) becomes negative.

To improve linearity without adding design complexity, the IMD3 cancellation method is proposed, as shown in Fig. 9. The unit PAs connected to one PCT (PCT1) are biased to the class-AB region; thus, they with a two-tone signal result in a negative IMD3 current (\(I_{\text{1,IMD3}}\) and \(I_{\text{2,IMD3}}\)). In contrast, the unit PAs connected to the other PCT (PCT2) are biased closer to the class-C region, a positive IMD3 current (\(I_{\text{2,IMD3}}\)) is generated, as shown in Fig. 9. At the T-line parallel combiner, the fundamental currents (\(I_{\text{1,Fund}}\) and \(I_{\text{2,Fund}}\)) of PCT1 and PCT2 are added, while \(I_{\text{1,IMD3}}\) and \(I_{\text{2,IMD3}}\) are cancelled each other, resulting in good linearity. Additionally, to effectively cancel the nonlinearity coefficients in the two nonlinear stages (DA and power stages), the DAs are biased closer to the class-C region using the antiphase method; thus, positive IMD3 currents (\(I_{\text{PA,IMD3}}\)) are generated. Accordingly, the negative IMD3 currents generated by the PCTs in the power stage can be canceled using positive IMD3 currents from the DAs.

First, to validate the proposed linearization concept, a two-tone simulation was performed only for the power stage, at a center frequency of 28 GHz with a tone spacing of 100 MHz. Fig. 10 shows the simulated IMD3 characteristics versus the output power with various gate bias voltages of the power stage. In the simulation of the power stage, the proposed power combiner is included. The gate bias voltages of the power stage are swept from 0.25 to 0.65 V. As shown in Fig. 10, with a lower bias, the IMD3s in both the low and middle output power regions are high level, resulting in poor linearity performance. In contrast, for a higher bias, the IMD3s are maintained at a low level over most of the
TABLE 1. Classification of cases for bias voltages.

| Driver stage (DA) | Power stage |
|-------------------|-------------|
|                   | Unit PAs connected to | Unit PAs connected to |
|                   | PCT1         | PCT2         |
| Case 1            | 0.3 V        | 0.5 V        | 0.5 V        |
| Case 2            | 0.45 V       | 0.5 V        | 0.5 V        |
| Case 3            | 0.3 V        | 0.6 V        | 0.6 V        |
| Proposed case     | 0.3 V        | 0.35 V       | 0.55 V       |

output power. Thus, using a higher bias for the gate bias voltage of the power stage is expected to achieve better linearity performance. However, if the bias point is too high, achieving a high PAE of the PA is difficult. Thus, the selection of bias points is important with regard to the IMD3 and PAE. Additionally, sweet-spot generation and movement depending on the gate bias voltages are also observed in Fig. 10. As shown in Fig. 10, the sweet-spots are generated at approximately 0.35–0.5 V. Accordingly, we can estimate that the selected gate bias voltage for the power stage is approximately 0.35–0.5 V. The optimum gate bias voltage of the power stage is considered to maintain the IMD3s below −30 dBc versus an output power of 0–14 dBm. Hence, a gate bias voltage of 0.5 V for the power stage is selected to satisfy the specification of the IMD3 with output power. At the selected gate bias voltage of 0.5 V, IMD3s of −30 dBc are maintained well up to output power of 14 dBm.

Next, the simulated IMD3s of the two stages are plotted in Fig. 11. The simulated PA consists of a two-stage structure. The DA includes an inter-stage matching networks. The gate bias voltages of the DA are swept from 0.15 to 0.65 V, while the gate bias voltage of the power stage is fixed at 0.5 V. The simulation results indicate the cancellation effect of IMD3s from the power stage. For a selected gate bias voltage of 0.3 V for the DA, IMD3s are significantly suppressed in the output-power range of 0–14 dBm. The selected gate bias voltage of 0.5 V for the power stage is close to the class-AB region; thus, negative IMD3s are generated. Meanwhile, the obtained gate bias voltage of 0.3 V for the DA is in the class-C region, resulting in positive IMD3s. Thus, in the two cascaded nonlinear stages, the generated negative IMD3s from the power stage in the class-AB region are clearly canceled by the positive IMD3s from the DA in the class-C region [34]–[38], [41]. As mentioned previously, the cancellation effect in the anti-phase method is remarkably demonstrated through the simulation results of the two stages, as shown in Fig. 11.

The simulated IMD3 performances of the proposed CMOS PA for proof-of-concept IMD3 cancellation method with the four different cases are shown in Fig. 12. The four different
cases are classified by different bias conditions of the DAs and the unit PAs connected to two PCTs, as shown in Table 1. In case 1, the DAs are biased at 0.3 V, and the unit PAs connected to the two PCTs are biased at 0.5 V, which are acquired from the result of Fig. 11. In other words, to improve the IMD3 performance, case 1 is applied to the anti-phase method. In case 2, the DAs are biased at 0.45 V, while the unit PAs connected to the two PCTs are biased at 0.5 V. In case 3, compared to case 1, the gate bias voltage of the unit PAs connected to the two PCTs is slightly increased to close the class-A region. Finally, to improve the linearity over a wide range of $P_{\text{OUT}}$, the proposed IMD3 cancellation method with an anti-phase method is applied to the proposed case. With the proposed IMD3 cancellation method, DAs are biased at 0.3 V, which contributes to generating positive IMD3s. Additionally, the unit PAs connected to PCT1 is biased at 0.35 V; thus, positive IMD3s are generated, while other PCT2 is biased at 0.55 V, resulting in negative IMD3s, as shown in Fig. 8. As mentioned previously, in the proposed power-combiner structure, the nonlinearities of IMD3s from the unit PAs connected to PCTs are canceled each other. Additionally, the nonlinearities of the IMD3s in the two-stage PA can be canceled using the anti-phase method between the DAs and the power stage. As shown in Fig. 12, most cases satisfy the IMD3 of $-30$ dBc up to an output power of 10 dBm. However, to achieve a high linear output power up to 16 dBm, further improvements are required. In case 1, the IMD3s at output power of up to 15 dBm are effectively canceled. Nevertheless, the enhancement of IMD3s in the high-output power region is still needed to achieve high linearity at a higher output power. Compared with the other cases, the output power of the PA in the proposed case is improved from 12 to 19 dBm with an IMD3 performance of $-30$ dBc by using the proposed IMD3 cancellation method. The generated sweet spots in the proposed case can be pushed toward a high output power, resulting in good linearity. Hence, the proposed IMD3 cancellation is effective for achieving high linearity with a wide output-power range.
In addition, to evaluate the linearity improvement with the proposed IMD3 cancellation method, the phases of the IMD3 components for the output currents of the PCT1 and PCT2 in the proposed case are compared with those in the case 1, as shown in Fig. 13. The phases of the IMD3 components for the two output currents in the case 1 are similar and no cancellation at the T-line combiner occurs in the case 1. In contrast, the phase difference between the IMD3 components of the output currents of the PCT1 and PCT2 in the proposed case is approximately 180° from 16-dBm output power to 19-dBm output power. Thus, the IMD3 components for the output currents from the two PCTs are canceled each other. The proposed case demonstrates lower nonlinearity of IMD3 in a high output power region.

To test wideband performances, two-tone simulations with tone spacing of 200 MHz and 400 MHz were performed, as shown in Fig. 14 and 15. For the two-tone test with a tone spacing of 200 MHz, the simulated IMD3s of the proposed case are maintained less than approximately −30 dBc up to an output power of 17 dBm. For the case with a tone spacing of 400 MHz, the bias point of the proposed case is slightly tuned (PCT1: 0.37 V and PCT2: 0.58 V) for better performance. With the increase of a tone spacing, the IMD3 performances are slightly degraded. However, the trends from the simulated results with wider tone spacing agree with the trends from the simulated results with a tone spacing of 100 MHz.

Fig. 16(a) and (b) show comparisons between the power gain and PAE of the proposed IMD3 cancellation method and those of other cases. In Fig. 16(a), the power gain of the proposed case is slightly lower than those of the other cases. However, because the gate bias voltage of the DAs and power stage for the proposed techniques is lower than those of the other cases, the proposed IMD3 cancellation method exhibits excellent performance for improving the PAE, as shown in Fig. 16(b). With this method, the low bias voltage of the DAs and the power stages reduces the current consumption of the proposed PA, while power gain of the PA is sacrificed. As explained previously, the proposed PA using the IMD3 cancellation method demonstrates the superiority of the improved IMD3s and PAE under the determined bias condition. The simulated AM-PM results are shown in Fig. 16(c) for four different cases. Compared with the other cases, the AM-PM performance of the proposed case is more flat with the increase of the output power. Fig. 17 shows the load-pull simulation results for a cascode single-ended configuration with an input power of 5 dBm. The simulated output power and PAE contours are plotted with $V_{GS} = 0.35$ V and $V_{GS} = 0.55$ V, which is applied in the proposed case. The optimum performances for output power and PAE are slightly different for two cases. However, the optimum impedance with $V_{GS} = 0.35$ V is closed to that with $V_{GS} = 0.55$ V. Thus, the optimization of the output combiner considering different gate bias voltage was not considered in this design. If it is well optimized further, PAE and output power can be slightly improved.

B. DESIGN OF PROPOSED mm-WAVE POWER AMPLIFIER

Fig. 18 shows a detailed schematic of the proposed mm-wave two-stage power amplifier. The proposed mm-wave PA is composed of five functional blocks: the input-matching network, DA, inter-stage matching network, power stage, and output-matching network. For the single-ended input and output, input and output networks are required for both balun function and matching.

For the input-matching network, two input transformers are designed to generate two differential signals. The input transformer has a 1:1 turn ratio, and the widths of the primary and secondary windings are $8 \, \mu m$. The M8 and M7 layers are used for the primary and secondary windings in the design of the input-matching networks, respectively. The size of the input-matching network is $180 \, \mu m \times 72 \, \mu m$. The DA is designed using the CS topology for a 1.2-V supply voltage. Each differential DA drives two differential unit PAs, which have the same transistor size ($42 \, \mu m/65 \, nm$). Two 4-way inter-stage transformers are used to drive 8-unit PAs. Because the output impedance of the unit DA is typically higher than the input impedance of a unit PA, the topology of the series power divider is used for the 4-way inter-stage transformer. The size of the inter-stage matching network is $354 \, \mu m \times 65 \, \mu m$. For PA designs, a differential cascode configuration is adopted for a 2.4-V supply voltage to prevent source degeneration and breakdown of the transistor. The size
of the common-gate device is identical to that of the CS device, i.e., 128 µm/65 nm. In addition, the differential DA and CS in the PA include two neutralized capacitors (C_NS) for high reverse isolation. Because the increase of C_gd in the CS transistor will degrade the stability and power gain of the PA, the stability issues of the CS transistor can be solved by adding the C_N [44], [45].

To reduce the effect of bonding wires and create a solid ground plane, four VDD and six ground pads are placed on the chip. Additionally, the ground pads including input/output ground pads and ground plane are connected to each other, and the ground pads are bound by strips, which are composed of M8 and AP layers. The proposed power combiner was used for an output-matching network to combine the output power from the unit PAs and convert differential signals into a single-ended signal.

IV. MEASUREMENT RESULTS
The proposed mm-wave PA using a 4-way parallel–parallel combiner with IMD3 cancellation was implemented in 1P8M 65-nm CMOS technology that supports an ultra-thick metal (UTM) layer and an aluminum redistribution layer (RDL). Fig. 19 shows a chip photograph of the implemented PA, which has a size of 0.87 mm × 0.9 mm, including all pads. The chip incorporates the PA cores and input/output passive networks. Because all the matching circuits are integrated, there are no external matching components apart from the off-chip bypass capacitors. To validate the performance of the PA, the implemented PA is measured using on-wafer probing with a dc wire bond to an external FR4 printed circuit board (PCB), as shown in Fig. 19.

Fig. 20 shows the experimental setup for the s-parameter, large-signal continuous-wave (CW), and modulation measurements. The s-parameter is measured using an Anritsu 37369c vector network analyzer with an input power of −30 dBm. For large-signal CW and modulation measurements, the output power is measured with a Rohde & Schwarz (R&S) SMW200A signal generator and a R&S FSV A3030 spectrum analyzer. Fig. 21 shows the simulated and measured results for the s-parameters. There is little deviation between the simulated and measured results, and their trends are similar. The measured peak S21 is 16.6 dB, and the
−3 dB bandwidth is 3.2 GHz, centered at approximately $F_0 = 27.3$ GHz. The input return loss (S11), at $F_0$ is better than $-15$ dB and remains better than $-10$ dB over the range of 25–31.1 GHz. The PA is well designed for the target band.

Fig. 22(a) shows the measurement results for the CW power-sweep at 27.3/28 GHz. The PA delivers a saturated $P_{\text{OUT}}$ ($P_{\text{SAT}}$) of 23.5/23.2 dBm with a power gain of 16.6/15.9 dB while achieving a $\text{PAE}_{\text{SAT}}$ of 35.5/33.5% for 27.3/28 GHz. $P_{\text{SAT}}$ is defined as the $P_{\text{OUT}}$ at a 5-dB compression point. Additionally, the measured and simulated results at 28 GHz for a CW are plotted in Fig. 22(b).

The large-signal characteristic of the PA with frequency variation results are measured over the range of 25–30 GHz. As shown in Fig. 22(c), the peak CW signal performance is obtained at 27.3 GHz. For the frequency range of 26–28 GHz, the measured $P_{\text{SAT}}$ is $>22$ dBm with a PAE of 30%. Additionally, the measured 1 dB compressed output power ($P_{\text{O,1dB}}$) achieves above 20 dBm over the range of 26–28 GHz. The 3-dB bandwidths for both $P_{\text{SAT}}$ and $P_{\text{O,1dB}}$ are more
than 5 GHz. Because wideband matching methods were not applied in this work, the bandwidth performance can be improved by incorporating wideband matching methods in [55]–[57]. Comparisons of the measured the IMD3 are shown in Fig. 23 (a). The IMD3 characteristics are measured using a two-tone signal centered at 28 GHz with a tone spacing of 100 MHz in the four different cases including the proposed linearization bias point. Compared with other three cases, the proposed IMD3 cancellation method clearly produces less IMD3 for a wide range of $P_{\text{OUT}}$. The IMD3 of the PA is maintained under $-30$ dBc up to a $P_{\text{OUT}}$ of 19.0 dBm. This implies that the linear output power of the PA at an IMD3 of $-30$ dBc is improved by 6.5 dBm. The proposed PA achieves a high $P_{O,AVG}$ with a high PAE by employing the parallel–parallel power combiner with the IMD3 cancellation method.

Next, the PA is characterized using a 256/512-QAM signal (7.5-dB PAPR with a 100-MSym/s data rate owing to equipment limitations). Fig. 23 (b) shows the EVM, ACPR, average output power, and PAE with 256-QAM signals at 28 GHz. When tested with a 256-QAM 100-MSym/s signal, the proposed PA achieves a $P_{O,AVG}$ of 18.36/18.02 dBm at a PAE of 18.6/17.6% with an EVM of $-31.6/-31.2$ dB and an ACPR of $-30/-30$ dBc at 27.3/28 GHz. Additionally, when a 512-QAM 100-MSym/s signal is applied to the PA, it achieves a $P_{O,AVG}$ of 18.25/17.73 dBm at a PAE of
**TABLE 2.** Performance comparison with state-of-the-art mm-wave CMOS PAs for 5G application.

| Ref. | This work | [30] | [31] | [32] | [33] | [46] | [47] | [58] | [60] |
|------|-----------|------|------|------|------|------|------|------|------|
| Tech. | 65nm CMOS | 65nm CMOS | 28nm CMOS | 28nm CMOS | 28nm CMOS | 28nm CMOS | 28nm CMOS | 90nm CMOS | 130nm SiGe | 45nm SOI CMOS |
| Number of stages | 2 | 2 | 2 | 2 | 1 | 2 | 1 | 2 | 2 |
| Freq. (GHz) | 27.3 | 28 | 28 | 30 | 34 | 28 | 28 | 28 | 28 |
| Gain (dB) | 16.6 | 15.9 | 15.6 | 15.7 | 20.8 | 13.6 | 18.5 | 16.3 | 20.5 | 20.5 |
| P_{SAT} (dBm) | 23.5 | 23.2 | 15.5 | 14 | 16.6 | 19.8 | 18.9 | 26 | 28.3 | 20.4 |
| PAE_{SAT} (%) | 35.5 | 33.5 | 41 | 35.5 | 24.2 | 43.3 | 39.7 | 34.1 | 30.4 | 45.0 |
| P_{O, 5dB} | 22.2 | 22 | 13.9 | 13.2 | 13.4 | 18.6 | 18.5 | 23.2 | 26.8 | 19.1 |
| Modulation scheme | 256-QAM | 256-QAM | 64-QAM | 64-QAM | 64-QAM | 64-QAM | 64-QAM | 256-QAM | FR2 5G NR 64-QAM | FR2 5G NR 64-QAM |
| Data rate (Msym/s) | 100 | 100 | 340 | 250 MHz | 337 MHz | 80 MHz | 1200 MHz | 100 | 200 MHz | 800 MHz |
| EVM (dB) | -31.6 | -31.2 | -26.4 | -25 | -25 | -27.5 | -25.4 | -32 | -25.1 | -25.1 |
| ACPR (dBc) | -30 | -30 | -30 | -26.4 | -32.1 | NA | NA | -35+ | - | -25.6 |
| P_{O, AVG} (dBm) | 18.36 | 18.02 | 9.8 | 4.2 | 10.1 | 10.97 | 9.3 | 20 | 18.1 | 11.3 |
| PAE_{AVG} (%) | 18.6 | 17.6 | 18.2 | 9 | 5.8 | 17.3 | 10.3 | 8+ | 13.8 | 16.6 |
| Modulation scheme | 512-QAM | 512-QAM | 256-QAM | NA | NA | NA | 256-QAM | 256-QAM | FR2 5G NR 256-QAM |
| Data rate (Msym/s) | 100 | 100 | 60 | | | | 400 MHz | 500 | 400 MHz |
| EVM (dB) | -32.8 | -32.1 | -31.7 | | | | -31.77 | -30 | -30.5 |
| ACPR (dBc) | -31.8 | -33.1 | -28 | | | | NA | N/A | -34.7 |
| P_{O, AVG} (dBm) | 18.25 | 17.73 | 9.4 | | | | 6.6 | 16.2 | 11.1 |
| PAE_{AVG} (%) | 18.2 | 16.1 | 16.3 | | | | 5.6 | 6+ | 15.3 |
| PA core area (mm²) | 0.25 (0.78*) | 0.24 | 0.16 | 0.16 | 0.28 | 0.31* | 0.4* | 1.35 (4.19) | 0.21 (1.35) |
| Topology | 4-way parallel-parallel power combiner with IMD3 cancellation | Transformer based AM-PM correction | Inductive source degeneration | PMOS varactor AM-PM compensation | 2nd harmonic traps | Ladder-transformer with 2nd harmonic traps | Current-combining with inductance-based neutralization | Multi-Primary DAT-based Doherty | Compensated distributed balun |

*Including pads (total area), +graphically estimated

18.2/16.1% with an EVM of $-32.8/-32.1$ dB and an ACPR of $-31.8/-33.1$ dBc at 27.3/28 GHz. Fig. 24 depicts the constellation and the corresponding output-power spectrum with 256/512-QAM at 27.3/28 GHz.

Table 2 presents a comparison of the PA developed in this work with other state-of-the-art CMOS PAs for 5G applications. Among the PAs in the table, the proposed CMOS PA demonstrates the high linear $P_{OUT}$ with the highest PAE, supporting 256/512-QAM modulation without DPDs.

**V. CONCLUSION**

In this paper, a mm-wave CMOS PA based on a 4-way parallel-parallel power combiner with the IMD3 cancellation method using 65-nm CMOS technology is proposed for achieving a high linear output power and high PAE. To demonstrate the superiority of the proposed power combiner, two types of power-combining transformers, SCT and PCT, are comprehensively analyzed and compared with regard to their balance performances by considering the unwanted parasitic capacitors. Additionally, the proposed IMD3 linearization method can enhance the linear output power and PAE without a large back-off from the $P_{SAT}$. The proposed CMOS PA demonstrates a highly linear $P_{OUT}$ with the highest PAE, supporting 256/512-QAM modulation without DPD. This is achieved by adopting the mm-wave PA design for 5G applications, the proposed output-power combiner, and the linearity improvement method. To the best of the authors’ knowledge, the presented PA demonstrates...
the highest linear P_{OUT} with the high PAE, supporting 256/512-QAM among the recently published fully integrated mm-wave 5G CMOS PAs [48].

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