A Method for Building Low Loss Multi-Layer Wiring for Superconducting Microwave Devices

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Complex integrated circuits require multiple wiring layers. In complementary metal-oxide-semiconductor (CMOS) processing, these layers are robustly separated by amorphous dielectrics. These dielectrics would dominate energy loss in superconducting integrated circuits. Here we describe a procedure that capitalizes on the structural benefits of inter-layer dielectrics during fabrication and mitigates the added loss. We use deposited inter-layer dielectric throughout fabrication, then etch it away post-fabrication. This technique is compatible with foundry level processing and can be generalized to make many different forms of low-loss wiring. We use this technique to create freestanding aluminum vacuum gap crossovers (airbridges). We characterize the added capacitive loss of these airbridges by connecting ground planes over microwave frequency λ/4 coplanar waveguide resonators and measuring resonator loss. We measure a low power resonator loss of $\sim 3.9 \times 10^{-9}$ per bridge, which is 100 times lower than dielectric supported bridges. We further characterize these airbridges as crossovers, control line jumpers, and as part of a coupling network in gmn and fluxmon qubits. We measure qubit characteristic lifetimes ($T_1$’s) in excess of 30 $\mu$s in gmn devices.

Two dimensional superconducting qubit architectures will require multi-layer wiring.1–5 Multiple wiring layers are fundamental to standard integrated circuits to route signals past one another to individually address a two dimensional grid of elements. Multi-layer wiring has been developed for superconducting circuits.6,7 These wiring layers are separated by deposited dielectrics, and while these processes offer robust large scale control, the amorphous dielectrics used (typically SiO$_2$) are quite lossy, with loss tangents $\tan \delta \approx 10^{-3}$8,9. We limit participation of similar dielectrics ($p_i < 10^{-3}$) to achieve state-of-the-art qubit quality factors ($Q_i > 1 \times 10^{10}$)10,11. We have developed a method that benefits from the structural support of inter-layer dielectrics while mitigating the loss. We use deposited dielectrics only as a scaffold to separate and stabilize different metal layers through aggressive fabrication steps, and then etch it away at the end of fabrication. This process is compatible with standard CMOS processing, and provide an avenue toward scalable low-loss control wiring for a two dimensional grid of qubits. While this method is quite general and can be applied to many forms of multi-layer wiring we demonstrate this technique by fabricating the simplest forms of multi-layer wiring: crossovers.

Free standing metallic crossovers, known as airbridges, are widely used in low-loss microwave circuits12,13 as well as superconducting circuits.14–16 These airbridges are typically fabricated using re-flowed photoresist as a scaffold, which is removed immediately after bridge fabrication and prior to further processing. Released airbridges typically cannot withstand the sonication widely used to remove surface contaminants. Additionally, without dielectric support, the mechanical strength of freestanding airbridges relies on an arched shape. Airbridges with spans much larger than their arched height tend to bend under the pressure of resist spins and bakes. Thus, airbridges are made taller to span longer distances. Bridge height is limited by future processing, as standard high-resolution resists ($\sim 1-10 \mu$m thick) fail to protect taller airbridges from aggressive processing steps such as ion etching or lift-off. We use our dielectric scaffolding technique to create a different kind of airbridge. The dielectric scaffolding stabilizes these bridges through aggressive sonication and resist coating, thus decoupling the air bridges’ span from it’s height. Mechanical tests indicate these airbridges span distances of at least 70 $\mu$m reliably. The added capacitive loss per bridge is comparable to photoresist scaffolded airbridges and is $\sim 100 \times$ less lossy than conventional dielectric crossovers (bridges with the scaffolding left in tact, as in Fig. 1).

We fabricate these airbridges after defining aluminum basewiring on high resistivity (>10 kΩ-cm) intrinsic (100) plane silicon substrates. We optically pattern a tri-layer17 stack of resist as a lift-off mask and electron beam (e-beam) deposit 1 $\mu$m of SiO$_2$ to define our dielectric scaffold. Due to the growth conditions the SiO$_2$ sidewalls form an approximately 45° with the substrate (see Fig. 1(b)). Next, we reapply the same lift-off process to define the bridge itself, except prior to deposition, we use an in-situ 400 V, 0.8 mA/cm$^2$ argon ion mill to remove the exposed native aluminum oxide on the basewire. This mill allows DC electrical contact between base-wire aluminum and the 600 nm thick airbridge aluminum. After all further processing we use a dry VHF etcher (PRI-MAXX @VHF Etch Release Technology) to release the airbridges by removing the scaffolding SiO$_2$. The chamber is pumped low vacuum, and the die is heated to 45 Celcius on a 3 inch silicon carrier wafer. A mixture of
HF vapor, nitrogen, and ethanol is then bled into the chamber at a total pressure of 125 Torr (parameters in Table I). The scaffold SiO$_2$ and native oxide of the exposed silicon substrate are removed after 2 cycles of 15 seconds without breaking vacuum, as shown in Fig 1(c). Vapor phase release significantly reduces the mechanical strength required to overcome stiction, a common failure in microelectromechanical systems (MEMs) devices.$^{18,19}$ This process does not attack other materials used in qubit fabrication including aluminum, aluminum oxide, and silicon.

In our superconducting circuits these airbridges serve two main functions: ‘jumper airbridges’ which hop circuit elements over each other for stronger couplings, smaller footprints, and design flexibility. These SiO$_2$ scaffolded airbridges can be made with contact pads as small as 1 µm$^2$ and allow even micron width lines to hop over each other. Ground plane airbridges are commonly used to electrically connect ground planes to suppress parasitic microwave frequency slot line modes which modify couplings and act as qubit loss channels in coplanar waveguide (CPW) geometries.$^{20,21}$ These airbridges also route return currents to reduce unwanted cross-talk between control lines.

We measure the added capacitive loss from airbridges using $\lambda/4$ CPW resonators. To measure resonator loss, we cool down chips in a heavily filtered$^{22}$ adiabatic demagnetization refrigerator with a base temperature of 50 mK. We extract resonator internal quality factor (loss = $1/Q_i$) by measuring and fitting the microwave scattering parameters versus frequency near resonance.$^{23}$ Each chip has ten resonators capacitively coupled ($Q_e$ between $5 \times 10^5$ and $1 \times 10^6$) to a common feedline. These resonators have between zero and ninety-eight groundplane airbridges spanning their center trace. The airbridges are 3 µm wide and have a height above the center trace set by the original dielectric thickness of 1 µm. In Fig. 1(a) we show one such resonator resonator spanned by 12 ground plane airbridges equally spaced along the resonator after the coupling arm. All resonators have a 10 µm center trace and a 5 µm gap to ground on either side, and resonance frequencies near 6 GHz.

We compare loss between three styles of resonators: resonators spanned by scaffolded bridges (Fig. 1(b)), resonators spanned by airbridges (after VHF release, Fig. 1(c)), and purely CPW resonators with no crossovers of any kind (bare resonators). In Fig. 1(d) we display internal quality factor data for these three resonators. For clarity, we show only a single representative trace from each. The single photon loss limit approximately captures the physics of energy loss in superconducting qubits at the same frequency. The bare witness resonator has a low power internal quality factor of around $1.5 \times 10^6$ which is consistent with single layer fabrication resonators of the same geometry. We saw little to no difference in bare resonator quality factors between chips with or without the VHF process. When the SiO$_2$ is left intact, (as it would be in typical dielectric crossovers) the low power $Q_i$ drops to around $1 \times 10^4$. This is consistent with an amorphous SiO$_2$ loss tangent of $\tan \delta \approx 10^{-3}$ and a participation of 10% (roughly the added capacitance for twelve scaffolded bridges). After the VHF treatment, the $Q_i$ of resonators with twelve airbridges recovers to a factor of 2 lower than the bare resonators. We measure the

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|}
\hline
VHF Flow (SCCM) & N$_2$ Flow (SCCM) & Ethanol Flow (SCCM) \\
\hline
190 & 1425 & 210 \\
\hline
\end{tabular}
\caption{VHF etch parameters.}
\end{table}

Figure 1. (a) Optical micrograph of a CPW $\lambda/4$ resonator with 12 crossovers over the center trace capacitively coupled to a feed-line. (b) Crossover spanning the resonator before removing SiO$_2$ scaffold. (c) Freestanding airbridge crossover after VHF treatment. (d) Representative resonator $Q_i$ vs average photon excitation. Leaving the SiO$_2$ under the bridges greatly reduces the resonator’s quality, as would most deposited dielectrics. After removing the SiO$_2$ the resonator’s quality recovers to about a factor of two lower than bare witness resonators. The twelve evenly spaced airbridges only cover ~0.7% of the $\lambda/4$ resonator geometry. Resonators without bridges (bare resonators) show no substantial difference in quality with or without VHF treatment.
scaling of this residual loss with number of airbridges between zero and ninety-eight. The internal quality factor decreases with increasing number of airbridges and lines of best fit indicate added loss at low power of $3.9 \times 10^{-8}$ per bridge.\textsuperscript{17}

We use these low-loss airbridges as an integral part of gmon qubits. These qubits are transmon qubits\textsuperscript{24} with inductive taps placed between DC SQUID and ground plane to allow adjustable coupling to nearest neighbors.\textsuperscript{25} It is critical that any added loss from the airbridges does not compromise the qubit coherence. In Fig. 2(a) we display one such gmon qubit with its neighboring coupler network. We bias these qubits’ DC SQUID loop with maximum DC current of 2 mA. This current flows entirely through a jumper crossover in-line with the flux bias line (Fig. 2(b)) and shows no evidence of on-chip heating. In the qubit circuit, we use many ground plane airbridges as well as a set of jumper airbridges in-line with the coupler’s geometric inductor (Fig. 2(c)). This jumper airbridge allows a gradiometric turn which further reduces crosstalk. These jumper airbridges are only 1.5 $\mu$m wide, highlighting their small footprint. It is also important to note that these airbridges are fabricated prior to Josephson junction deposition, and are robust after all of the further processing, with yield limited by errors in lithography. In Fig. 2(d) we show qubit energy relaxation time ($T_1$) spectra over 3 GHz of tunable qubit frequency for four different qubits. The spectrum is well represented by a constant effective $Q_i \approx 6.5 \times 10^6$, with small sections where the $T_1$ drops dramatically. These spectra are consistent with qubit loss dominated by dielectric surface loss from the SQUID area.\textsuperscript{10} The airbridges themselves do not appear to greatly impact the qubit $T_1$ spectra.\textsuperscript{17}

Figure 2. (a) Scanning electron microscope image of a gmon qubit and it’s neighboring adjustable coupler network. (b) This qubit design utilizes both jumper airbridges (hopping SQUID bias lines over ground plane and qubit inductor lines) as well as ground plane airbridges (hopping ground plane over coupler and qubit inductor lines). (c) Jumper airbridges are also used in the coupler network to hop the coupler inductor over itself as well as qubit inductor lines creating a “figure 8” pattern. (d) Qubit $T_1$ measurements from four different gmon qubits, with an average around 20 $\mu$s.

We also use these airbridges as integral parts of our fluxmon\textsuperscript{26} flux qubit circuits, for both isolated and coupled qubits. The main inductance and capacitance of the fluxmon is distributed over a long CPW segment that is terminated with an electrical short to ground at one end and a DC SQUID shorted to ground at the other. We use both ground plane airbridges over the qubit’s CPW and jumper airbridges in-line with the qubit’s CPW and the couplers as well. We tested three variations of fluxmon qubits on the same chip: uncoupled, coupled with
jumper bridge, and coupled without jumper bridge. The uncoupled qubits only use ground plane airbridges. For the coupled qubits, the CPW center trace of one qubit jumps over the CPW center trace of the other qubit via an airbridge, as shown in Fig. 3(a), while the other qubit does not have any in-line jumper airbridges.

The resulting qubit $T_1$ vs. frequency at symmetric bias (zero tilt bias) is shown in Fig. 3(d) for the three qubit variations. The background dissipation is believed to come from 1/f flux noise at low frequencies$^{26,27}$ extrinsic to the airbridges, with some other inductive loss extrinsic to the airbridges dominating at high frequencies. We find no measurable difference in coherence between the two types of coupled qubits. This is consistent with a very high quality galvanic contact between the jumper bridge and the qubit’s CPW. Furthermore, we see no measurable difference in coherence between the coupled and uncoupled qubits, despite the fact that the coupled qubits are in very close proximity to a coupler circuit (the thin traces and ground plane pads in Fig. 3(c)) containing many crucial jumper and ground plane airbridges. This retained coherence is very important for scaling up fluxmon circuits with many jumper airbridges and couplers, in order to couple one qubit to many others at once for quantum annealing applications.

In summary, we have demonstrated a procedure that utilizes the structural benefits of inter-layer dielectrics commonly used in multi-layer wiring, while mitigating the capacitive loss. We use this process to fabricate low-loss airbridges that are robust during fabrication against strong sonication, other aggressive etches, and have a low profile. We measure the added loss per ground plane bridge over resonators to be $\sim 3.9 \times 10^{-8}$ at low power. We demonstrated these airbridges’ use in different superconducting qubit devices and measured little to no effect on the coherence of the qubits. These qubit designs fundamentally require a second layer of wiring, and here we have demonstrated a proof-of-principle method for rigidly scaffolding this second layer of wiring. Reapplication of the lift-off steps of SiO$_2$ and metal (prior to VHF release) would allow for further layers of wiring as well as further complexity.$^{17}$ By replacing the lift-off steps in the bridge fabrication with more standard blanket depositions and via etches, this technique is completely compatible with standard multi-layer CMOS processing.

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Supplementary Material for “A Method for Building Low Loss Multi-Layer Wiring for Superconducting Microwave Devices”

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We provide supplementary data and calculations.

I. RESONATOR LOSS PER BRIDGE

![Figure 1](image1)

Figure 1. Resonator loss ($1/Q_i$) cuts at low power (average photon population of $\sim 10^0$) and high power (average photon population of $\sim 10^6$) plotted against number of bridges. Lines of best fit give and 3.9 $\times$ 10$^{-8}$ per bridge at low (high) power.

Figure 2. CPW dimensions of aluminum resonators on a silicon substrate. The width of the bridge into the page is $l = 3 \mu$m.

Here we calculate the expected added low-power loss per bridge:

$$1/Q_{i, \text{bridge}} = \tan \delta \times p_{loss}$$

$$\approx \tan \delta \left( \frac{2t_{loss}}{h} \right) \left( \frac{1}{\epsilon_{r,loss}} \right) \left( \frac{C_{\text{bridge}}}{C_{\lambda/4}} \right)$$

$$= 1 \times 10^{-9} \text{loss per nm} \left( \frac{t_{loss}}{\epsilon_{r,loss}} \right)$$

Where the factor of 2 assumes that the lossy material is on both the top of the center conductor and bottom.

We design $\lambda/4$ coplanar waveguide (CPW) resonators with a variable number of ground plane airbridges to measure the added capacitive loss per bridge. We use the anhydrous hydrofluoric acid vapor (VHF) process detailed in the main paper to remove the SiO$_2$ scaffold prior to cooling down these resonators. We measure the scaling of the resonator loss with between 0 and 98 bridges spanning the center trace. In Fig. 1 (a) we display representative $Q_i$ vs average photon excitation for these resonators. The resonator internal quality factor decreases with increasing number of bridges. In Fig. 1 (b) we show cuts of loss ($1/Q_i$) vs number of bridges at low and high power. A line of best fit indicates an added loss at low power of 1.2 $\times$ 10$^{-7}$ per fF of added capacitance, or 3.9 $\times$ 10$^{-8}$ per bridge at low power. This is a factor of two higher loss per added capacitance of photoresist scaffolded airbridges (5.08 $\times$ 10$^{-8}$ per fF). It is also important to note that if either of these bridges were coupled to a lumped capacitor, they would display a factor of two more loss. Here we are protected from the full loss by the cosine voltage profile along the $\lambda/4$ resonator.

$$\mu m h = 1$$
$$\mu m t = 0.6$$
$$\mu m g = 5$$
$$\mu m w = 10$$

Figure 2: CPW dimensions of aluminum resonators on a silicon substrate. The width of the bridge into the page is $l = 3 \mu$m.


| Resist Type | Hot Plate Bake Temperature (°C) | Bake Time (minutes) | Approximate Thickness (nm) | Vertical Oxygen Barrel Ash Rate \(^a\) (nm/sec) | Vertical Oxygen Ash Rate in ICP \(^b\) (nm/sec) |
|-------------|---------------------------------|----------------------|-----------------------------|-----------------------------------------------|-----------------------------------------------|
| PMMA        | 160                             | 10                   | 240                         | 2.10                                          | 0.92                                          |
| SF5 (etch)  | 160                             | 5                    | 200                         | NA                                            | NA                                            |
| SF11 (liftoff) | 160                          | 5                    | 1300                        | NA                                            | NA                                            |
| SPR (955-0.9)| 90                              | 1.5                  | 900                         | 0.71                                          | 0.40                                          |

\(^a\) 0.3 torr O\(_2\), 100 watts RF bias power  
\(^b\) 0.015 torr O\(_2\), 100 watts ion power, 0 watts RF bias power

Table I. Parameters for resists used in tri-layer stack. All resists are spun on at 1500 rpm for 45 seconds. SF5 is used for etch processes while the thicker SF11 is used for liftoff processes. We use a 0.4 second exposure at \(\sim 420\) mW/cm\(^2\) at the wafer to expose the SPR, and do a post exposure bake on a 110 C hot plate for 90 seconds to improve resist contrast and development stability. Etch rates measured with blanket films of the corresponding resist types.

II. EFFECT OF OVER-ETCHING SiO\(_2\)

The etch rate of the SiO\(_2\) in VHF will depend on the amount of SiO\(_2\) present. This loading effect could lead to remnant SiO\(_2\) and therefore increased loss. Over-etching may also lead to excess loss, as VHF is known to leave residue from condensation under certain etch conditions.\(^4\) We cooled down resonators etched for longer in VHF, as well as resonators with a much more substantial VHF etch (parameters in Tab. II), to test the effects of over-etching.

| VHF Flow (SCCM) | N\(_2\) Flow (SCCM) | Ethanol Flow (SCCM) |
|-----------------|--------------------|---------------------|
| 880             | 325                | 720                 |

Table II. Heavy VHF etch parameters.

In Fig. 3 we plot \(Q_i\) vs average photon population in resonators that underwent the above processes. We note that there is a very small effect on the internal quality from over etching for up to 3 times the length required to remove the SiO\(_2\) (this variation in \(Q_i\) is expected for device-to-device variation). However, when we use the stronger etch parameters for a much longer time, resonator’s internal quality factor drops to around \(2 \times 10^5\).

III. FULL FABRICATION

The basewire deposition, lithography, and wet-etch (using Tetramethylammonium hydroxide (TMAH) based photo resist developer) are covered in detail in a previous publication.\(^5\) We use this tri-layer stack of resist, consisting of PMMA (Polymethylmethacrylate 4% in Anisole), SF series PMGI, and i-line positive photoresist (SPR 955-0.9) to protect the aluminum from developer etching during dry etch and lift-off steps (Tab. I). The top resist layer is a standard photoresist for defining features \(\sim 1\) µm in critical dimension. The middle layer of resist
allows for variable undercutting for reliable lift-off and and etching profiles. The bottom layer of resist is used to protect the aluminum layer during photo resist development, and is known to etch readily in oxygen plasmas.\textsuperscript{6,7} We use a GCA Auto-Stepper 200 to expose optical patterns. The topmost resist layer develops where exposed. The PMGI develops without being exposed, undercutting the SPR (Fig. 4 a-b). The PMMA is not etched by the TMAH based developer and thus protects the aluminum from being etched. We then oxygen ash the PMMA to remove it where exposed and slightly undercut the SPR (Fig. 4 c).

Figure 4. Example tri-layer lift-off process step through. (a) Cartoon profile of tri-layer stack of resists top-to-bottom SPR 955, PMGI, PMMA, then an etched 100 nm aluminum film on an intrinsic silicon substrate (not to scale). (b) After photo lithography we develop to remove SPR where exposed and the PMGI develops isotropically at a rate of \(\sim 2.4 \text{ \mu m/min.}\) (c) The PMMA is nearly directionally ashed (due to RF bias and low pressures) in an oxygen plasma. (d) The SiO\(_2\) is e-beam deposited in a high vacuum system. (e) The resist is stripped clean with the help of the undercut layers breaking up the lift-off film.

This tri-layer process is made compatible with both etching and lift-off processes by changing the PMGI thickness and PMMA ashing method. For etch steps, the oxygen ash is done prior to the aluminum etch in situ in an inductive coupled plasma (ICP) tool (Panasonic E626I) with 15 mT of oxygen and 200 W plasma power with no RF bias onto the devices. For lift-off steps we ash the PMMA in a barrel asher (Technics PEII) with 300 mT of oxygen with 300 W of RF power. The middle PMGI layer also serves as a buffer between the solvents in the SPR and the PMMA. Direct contact between SPR and PMMA leads to variable intermixing and unstable PMMA ash rates. We use a thicker layer of PMGI SF11 (\(\sim 1.1 \text{ \mu m}\)) to fabricate the SiO\(_2\) scaffolded airbridges bridges. We do one round of lithography and ashing, then load into a high vacuum electron beam deposition tool (base pressure \(\sim 1 \times 10^{-6} \text{ Torr}\)) and deposit 1 \text{ \mu m} of silicon oxide (Fig. 4 d). The resist is stripped using an N-Methyl-2-pyrrolidone (NMP) based resist stripper lifting off the excess silicon oxide (Fig. 4 e), and a second round of spins and photo-lithography defines the top metal. We load into another electron beam deposition tool (P\(_{\text{base}} = 2 \times 10^{-7} \text{ Torr}\)), do an in-situ argon ion mill to remove the oxide of the exposed aluminum. We use a 400 V, 0.8 mA/cm\(^2\) beam for 6 minutes with and continuous Argon flow of 3.6 sccm for this clean. We then deposit 600 nm of aluminum to form the bridge. We strip the resist as above to lift-off the excess metal.

We have greatly stabilized our lithography and processing by using this tri-layer stack of resists. Stripping resist after dry etch steps is more stable as all the resist in direct contact with the substrate and metal is shielded from the high energy ions needed to etch the aluminum oxide and subsequently the underlying aluminum. This allows solvents to get under hardened resist and reduces residues. This tri-layer of resist also greatly stabilizes lift-off processing. The undercut of the resist disconnects the lifted off film from the intended remnant material. This stack up also allows for an arbitrary number of lithography steps to be performed without worry of developer etching aluminum. This protection enables quick recovery from errors in lithography.

IV. OTHER STRUCTURES / SCALING TO MORE LAYERS

Figure 5. (a) Optical micrograph of CPW lines completely covered by a “tunnel” of metal. (b) The gaps between legs allow VHF to etch away the scaffolding SiO\(_2\).

We use the same dielectric scaffolding technique (detailed in the main paper) to create a “tunnel” structure displayed in Fig. 5. This almost completely shields CPW lines from one side by covering it in a continuous ground
plane. This structure is useful for reducing cross-talk in sensitive devices. It is perhaps easier to see that a third wiring layer could be fabricated on top of this tunnel. We expect that a 10 µm center trace resonator that is entirely encased by a tunnel would have a low (high) power $Q_i$ of roughly $2 \times 10^4$ ($5 \times 10^4$) by extrapolating the above loss per airbridge (Fig. 1 (b)). However, these tunnel resonators may have a higher $Q_i$ than this extrapolation predicts, as the continuous covering would have no edges or corners that concentrate the electric field. The $Q_i$ of these structures depends on the geometry. Specifically, we chose the height of the tunnel (or bridge) to optimize for high $Q$ as well as process stability for a single added layer. These heights could be modified to more easily allow further layers to be added on top.

It is important to note that the top metal layer is simply a re-application of the same lift-off steps as the scaffolding dielectric. Therefore nothing fundamentally limits this process to only a second layer. Furthermore, with planarization (a method commonly used in large layer stacks for CMOS processing\textsuperscript{8,9}), this process also generalizes to many multiple wiring layers. Ventilation holes are required however (as in Fig 5) to allow the VHF to attack the underlying SiO$_2$. While this constraint does add some complexity to the design layout, it is not prohibitive. If properly considered, this process allows for even more complex wiring.

V. GMON $T_1$ FREQUENCY DEPENDENCE

\[ C_q = 85 \text{ fF} \]
\[ L_{J,0} = 6.3 \text{ nH} \]
\[ L_g = 1.0 \text{ nH} \]

Figure 6. A simplified circuit of a lone gmon. The shaded resistor represents surface loss from the amorphous dielectrics near the thin geometric inductor lines.

All of the bridges in the gmon circuit are most strongly coupled to the qubit’s geometric inductor. Therefore, additional loss from these bridges would mostly add to that of the stray capacitance of the geometric inductor. The coherence of the gmon qubit is protected from capacitive loss in its thin inductor lines by a voltage divider between it’s SQUID inductance ($L_{J,0} \approx 6.3$ nH) and the linear geometric inductance ($L_g \approx 1.0$ nH). We flux tune this SQUID inductance larger to decrease the qubit’s frequency, thus the qubit energy relaxation time ($T_1$) would have a frequency dependence, as the ratio of SQUID to geometric inductance changes. Here we calculate the expected frequency dependence of this loss. It is often easier to think about loss in terms of an effective quality factor ($Q_i$). For this channel:

\[ Q_i = \frac{R_g}{Z_g} \left( \frac{V_g}{V_q} \right)^2 \]  

(1)

Where $Z_q \approx (L_J/C_q)^{1/2}$ is the qubit impedance, $R_g$ is the loss from surface amorphous dielectrics near the geometric inductor lines, $V_q$ is the voltage drop across the qubit capacitor ($C_q$), and $V_R$ is the voltage drop across the geometric inductor tail ($L_g$). We neglect the stray capacitance of the inductor tail as the qubit operates well below the resonance of the inductor circuit ($\sim 12$ GHz), and instead consider it only as a source of loss. We can calculate $V_g$ in terms of $V_q$ using the voltage divider:

\[ V_g = V_q \left( \frac{L_g}{L_J + L_g} \right) \approx V_q \left( \frac{L_g}{L_J} \right) \]  

(2)

we can also define $\omega_q = 1/(L_JC_q)^{1/2}$ and thus:

\[ Q_i \approx \frac{R_g}{C_qL_g^2} \left( \frac{1}{\omega_q} \right)^3 \]  

(3)

and to convert to an energy relaxation limit $T_1 = Q_i/\omega_q$ of the qubit:

\[ T_1 = \frac{R_g}{C_qL_g^2} \left( \frac{1}{\omega_q} \right)^4 \]  

(4)

We do not witness this strong frequency dependence in the qubit’s energy relaxation spectrum, indicating the qubit’s coherence is not limited by this loss channel. Another main loss channel for these qubits is due to surface dielectrics in the qubit capacitor. We fabricate witness resonators (etched at the same time as the qubit capacitor, but cooled down separately) to investigate this limit on qubit coherence. Witness resonators with a similar geometry have a much larger $Q_i \approx 3 \times 10^6$ indicating that the qubits’ $T_1$ is not limited by the capacitor itself. Most likely the gmon’s $T_1$ is limited by interfacial amorphous dielectrics near the Josephson junction electrodes.\textsuperscript{5}

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