Performance tests during the ATLAS IBL Stave Integration

J. Jentzsch on behalf of the ATLAS collaboration

CERN, PH Department,
Geneva, Switzerland
TU Dortmund, Physics Department,
Otto-Hahn-Str. 4, Dortmund, Germany

E-mail: jennifer.jentzsch@tu-dortmund.de

ABSTRACT: In preparation of the ATLAS Pixel Insertable B-Layer integration, detector components, so called staves, were mounted around the Beryllium ATLAS beam pipe and tested using production quality assurance measurements as well as dedicated data taking runs to validate a correct grounding and shielding schema. Each stave consists of 32 new generation readout chips which sum up to over 860k pixels per stave. The integration tests include verification that neither the silicon planar n⁺-in-n nor the silicon 3D sensors were damaged by mechanical stress, and that their readout chips, including their bump-bond and wire-bond connections, did not suffer from the integration process. Evolution of the detector performance during its integration will be discussed as well as its final performance before installation.

KEYWORDS: Detector design and construction technologies and materials; Hybrid detectors; Particle tracking detectors (Solid-state detectors)
1 The ATLAS Insertable B-Layer

An additional layer of pixel detectors, known as the Insertable B-Layer (IBL), has been installed in mid 2014 inside the existing 3-layer ATLAS Pixel Detector [1, 2] in order to improve tracking robustness, the tracks’ impact parameter reconstruction, vertexing and $b$ tagging performance for Run 2 and 3 of the LHC [3, 4]. This new layer of silicon pixel detectors is mounted around a new Beryllium beam-pipe at an average distance of 33.25 mm from the beam. It is more robust to the conditions expected for the upcoming runs, namely increased luminosity, radiation damage and pileup and thus will help compensate possible failures that may emerge over time in the existing pixel layers.

Considering the expected lifetime and the service capabilities of the ATLAS IBL, the sensors must have an inactive edge of at most 450 $\mu$m, show sufficient charge collection up to a fluence of $5 \cdot 10^{15}$ $n_{eq}$cm$^{-2}$ at a total ionizing dose of 250 MRad, be operational at a temperature of $-25$ °C, dissipate at maximum 200 mWcm$^{-2}$ power at a temperature of $-15$ °C and, furthermore, the required high voltage must not exceed 1000 V. Due to space constraints there can be no overlap of material in $z$ (along the beam direction), leaving a 205 $\mu$m gap between the sensors. Thus, two new sensor designs were implemented to minimize the inactive area: planar n$^+$-in-n sensors with slim edges, produced at CiS$^1$ and double sided 3D designs with a slim fence, produced at FBK$^2$ and CNM$^3$. Details on the specific IBL sensor designs can be found in [4]. An IBL module consists of either one planar sensor hosting two FE-I4 [5] chips or one 3D sensor bump bonded to one FE-I4 chip. With the FE-I4 generation the individual pixel size has been reduced from $50 \times 400 \mu$m$^2$ to $50 \times 250 \mu$m$^2$ which reduces the cross section and simultaneously increases the granularity of the detector. The pixels are organized in a 80 columns by 336 rows matrix. The chip’s physical size

---

1 Competence in Silicon, Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH (Erfurt, Germany).
2 Fondazione Bruno Kessler (Trento, Italy).
3 Centro Nacional de Microelectronic (Barcelona, Spain).
is 20.2 × 18.8 mm$^2$ with an active area of 20.2 × 16.8 mm$^2$ and a periphery of 20.2 × 2.0 mm$^2$, resulting in an active to inactive area fraction of about 90 %. The smaller feature size$^4$ leads to more radiation hardness due to thinner gate oxide transistors plus more digital complexity in less area. Each pixel holds internal calibration circuits as well as adjustable charge sensitive amplifiers and discriminators. The modules are glued to 64 cm long Parylene coated carbon foam support structures (staves), enabling charged track reconstruction up to a pseudo-rapidity$^5$ $|\eta| \leq 2.9$. 12 planar modules (24 FE-I4 chips long) cover the central part of the stave, and 4 3D modules (4 FE-I4 chips long) cover the regions of the both ends of a stave. In total 32 FE-I4 units are placed on a stave.

The IBL consists of 14 staves made of low density carbon foams mounted at a tilt angle of 14° (figure 1). The extremely light design structure of the IBL leads to a radiation length of 1.9 %. Inside the carbon foam support structure a titanium pipe carries CO$_2$ for cooling.

2 Module loading and results

Modules arriving at the stave loading site are dressed as seen in figure 2. Here, a planar module is shown. The electrical signals to and from the chips are transported via wire bonds through

$^4$130 nm CMOS process compared to 250 nm CMOS process in the 3-Layer ATLAS Pixel Detector.

$^5$\(\eta \equiv -\ln [\tan (\theta / 2)]\), where \(\theta\) is the angle between the particle three-momentum \(p\) and the positive direction of the beam axis.
a flexible PCB (module flex) glued on top of the sensor-chip assembly. The assemblies were mounted on an aluminum carrier, along with the full size module flex for mechanical support and a connector for handling and testing. This temporary connector was removed and the remaining module was glued onto a bare stave with high precision alignment. Then the wings, guiding the electrical connections from the stave flex underneath the stave to its face plate, were glued onto the module flexes. For monitoring the wire bonding process, four additional wire bonds every two readout chips were set and pulled afterwards. The average pull strength of the entire production was \( \sim 6.5 \pm 0.6 \) g while 5 g was the required minimum pull strength. The module alignment was verified in metrology measurements where fiducial marks on the sensors served as reference points. The module positions were verified along and across the stave to avoid mechanical contact between two modules. It was observed that no module deviated more than 150 \( \mu \)m from its nominal position. Thus, all staves fulfilled the mechanical IBL qualification. The subsequent module tests comprised verification of the electrical and logical functionality of the chips and their calibration of deposited charge threshold and time over threshold. If those steps were successfully passed, the staves were shipped to CERN where they were integrated into a dedicated test bench for full qualification. In case of failure, a module not satisfying the requirements was replaced on site, which occurred for 10 % of the production. In total 20 staves were loaded with 240 planar double chip, 88 3D CNM and 72 3D FBK modules.

3 The Stave QA bench and performance

The main part of the CERN ATLAS IBL Stave Quality Assurance (QA) bench located in SR1 laboratory comprises a \( \sim 2 \times 1 \times 1 \) m\(^3\) environmentally controlled, insulated aluminum box in which
two staves were placed, connected to a transportable CO\textsubscript{2} cooling system, equipped with a humidity and temperature interlock. Close to the setup there are second stage regulated LV power supplies, readout adapter cards as well as a crate for scintillator triggering in case of cosmic tests. Two radioactive sources, namely \textsuperscript{90}Sr and \textsuperscript{241}Am, were mounted onto a support structure connected to a linear motor and used for sensor qualification and disconnected bump studies.

To minimize the services inside the active area of the detector, four chips are powered in parallel forming a “DCS\textsuperscript{6} group”. Two chips share one command line and thus form one readout group. The data is sent out on individual lines. The naming convention (A and C side, counting modules from the interaction point to each end of stave) is in accordance with the ATLAS naming scheme. The modularity is shown in figure 3. In the Stave QA a highly modular system developed at SLAC, based on an ATCA\textsuperscript{7} crate was used as the IBL DAQ components [3] were not fully available by the time the QA measurements were performed. The RCE\textsuperscript{8} system is composed of three main parts: the RCE boards which generate commands, receive and chart the data, the CIMs\textsuperscript{9} which are the control units and communication interfaces, 96 channel 10 Gb/s ethernet switches, establishing connections between the DAQ computer and the corresponding RCEs and finally the HSIO\textsuperscript{10} boards which provide routing, buffering, multiplexing of commands and 8b/10b decoding of the FE-I4 data as well as generation of the clock and cyclic or external triggers. The calibration and data taking is executed by an operator via a dedicated DAQ panel (GUI) which collects module configuration files, runs scans and displays the results of each scan. The module configuration files are lists in plain text format that hold the readout chips’ register names and individual settings. The results were saved in the ROOT file format.

Four days were needed for each stave to be tested, including the time for installation, removal and optical inspections. The test flow comprised verification of the electrical and logical functionality of chips and sensors, calibration of all chips to the same (standard) settings, running of source scans for charge calibration, sensor functionality and disconnected bump bond studies and concludes in the determination of the total number of inoperable pixels based on the information from all previous scans. First, high resolution overview pictures were taken (as seen in figure 4(a)) followed by detailed inspection of all wire-bonds and critical electrical components. The inspector’s comments and pictures were stored in a dedicated QA database. If nothing suspicious was found during the optical inspection, the stave was integrated into the environmental box. The electrical functionalities were checked by running sense line checks, LV power cycle studies and measuring the sensors’ IV characteristics. Basic scans to check the logical parts included register read back

\textsuperscript{6}Detector Control System.
\textsuperscript{7}Advanced Telecommunications Computing Architecture.
\textsuperscript{8}Reconfigurable Cluster Element.
\textsuperscript{9}Cluster Interconnect Module.
\textsuperscript{10}High-Speed Input-Output.
tests, digital and analog tests as well as a threshold and time over threshold (ToT) scan. The digital test injects pulses in each pixel to an OR element right after the discriminator. Analog test hits are generated by a calibration voltage that charges the injection capacitors and are used to verify the functionality of the analog part of a pixel cell. A threshold scan injects various charges at a fixed step width and thus measures the discriminator activation curve. The time over threshold scan injects a fixed reference charge and evaluates the according length of the discriminator output signal.

These basic tests were performed at a module temperature of \( \sim 22^\circ C \) and mainly used for identifying major changes due to handling issues. All modules were calibrated to the desired threshold of 3000 e\(^-\) with a dispersion of less than 100 e\(^-\) with a time over threshold of 10 bunch crossings\(^{11}\) as a response to an injected reference charge of 16 000 e\(^-\). After calibration they were

\(^{11}\)25 ns bunch crossing rate at the LHC.
Figure 6. (a) Threshold, (b) threshold noise, (c) threshold over noise distributions per pixel at a module temperature of $-12 \degree C$ and (d) chip wise ToT (Time over Threshold) response for the 14 IBL staves at a module temperature of $20 \degree C$ and a threshold of 3000 e$^-$.\cite{6, 7}

Illuminated by a radioactive $^{90}$Sr source for 400 s to verify the sensor functionality and to identify disconnected bumps. The seemingly low efficiency regions seen in the 2D hit map in figure 4(b) correspond to the passive components mounted on the module flex (figure 4(a)). The increased number of hits in the outer column corresponds to longer pixels (see slim edge design in\cite{4}).

In order to mimic the conditions in the ATLAS Detector the most important operation was the calibration to a threshold of 1500 e$^-$ at a module temperature of $-12 \degree C$ while the time over threshold setting is held constant. The production of detector components lead to a successful construction of 20 staves from which 18 were considered production staves as two were damaged by accidental exposure to condensation\cite{6}. In figure 5 threshold and derived noise of the remaining 18 production staves as a function of chip position is shown. The error bars represent the RMS, the blue bars represent the minimum and maximum values found among the 18 staves. The central 24 entries correspond to FE-I4 chips connected to planar sensors, while the external 4+4 entries to 3D sensors. The slightly higher noise (figure 5(b)) on the 3D sensors is expected due to a higher sensor capacitance. The significantly increased noise on A8-2 comes from one module on a stave which was not chosen for the IBL. After a successful threshold calibration to 1500 e$^-$, three thermal cycles were performed with basic functionality checks (Digital, Analog, Threshold, ToT Scan) in-between...
to look for changes due to mechanical stress but none were observed. In figure 6 the IBL calibration performance before integration is summarized. Figure 6(a) shows the overall pixel thresholds for the different pixel types. All types peak at 1500 e\textsuperscript{−} threshold in a very narrow distribution with a dispersion of less than 50 e\textsuperscript{−}. Planar outer column and inter chip pixels are listed separately because of their longer size as can be seen in the derived noise plot (figure 6(b)). The threshold over noise is the key parameter in determining the quality of the IBL modules with respect to their operability at a given discriminator setting. The bigger this factor the less contamination of noise hits in the sample of physics hits recorded during collisions. The physics occupancy in the ATLAS Pixel Detector b-layer was $\sim 5 \cdot 10^{-4}$ hits per pixel per bunch crossing at the end of Run 1 while the expected physics occupancy for the IBL is $10^{-3}$ hits per pixel per bunch crossing in early operation and higher in later years. In both cases, pixels with a noise occupancy rate higher than $10^{-6}$ hits per pixel per bunch crossing are referred to as noisy pixels and are disabled from data taking to ensure noise contamination in physics hits from collisions to be less than 0.5%. A threshold over noise value higher than 5 would ensure that the noise contamination in physics hits from IBL would be less than 0.1%. This is achieved for the majority of all pixels, as can be seen in figure 6(c). The fraction of noisy IBL pixels is less than 0.03% for the 1500 e\textsuperscript{−} reference threshold calibration at $-12$ °C module temperature. The rate of noisy pixels in the 3-Layer Pixel Detector is twice as high at 0.06% for the 3500 e\textsuperscript{−} operational threshold at the same module temperature. In figure 6(d) the most probable values of the cluster time over threshold distributions per chip as responses to the electrons from the $^{90}$Sr source are presented. It shows a very homogeneous signal response over all chips in the detector.

The number of working pixels is the major criterium for choosing a stave for installation along with stave planarity and sensor IV stability. A production requirement for the IBL was to ensure a number of 99 % working pixels while all 18 staves show at least 99.7 % operable pixels. Figure 7(a) shows the average inoperable (bad) pixel fraction in blue for the installed 14 and in red for the 4 remaining staves as a function of $\eta$. It can be clearly seen that already in the step of mounting
modules onto staves the low $\eta$ regions were covered with the best modules available. The few defect channels are preferably distributed homogeneously in the $\eta$-$\phi$ plane. Thus, an $\eta$ weighted ranking was applied on all staves. The resulting picture of the operational fraction of pixels in the $\eta$-$\phi$ plane for the 14 installed staves is displayed in figure 7(b). The planarity is defined as the difference between the minimum and maximum height of a stave and did not exceed 340 $\mu$m in the IBL production which is within the envelope requirements of the IST, a carbon fiber tube inside the 3-Layer Pixel Detector. The applied classification of pixel failure modes, more detailed QA results and a selection of encountered issues during the production, namely double trigger responses, noise sensitivity on 3D sensors, charge calibration, weak differential driver output, oscillations on the low voltage supply lines and noise coupling on double chip sensors, can be found in [6].

4 Integration and current status

At the beginning of 2014, the stave QA finished and within one month 14 staves were integrated onto the IPT, a carbon fiber tube surrounding the beam pipe. The entire IBL package was fully assembled including all services one month later and was lowered into the ATLAS cavern beginning of May 2014. Once the detector was fully connected to all supplies, cooling and readout, it was re-calibrated stave by stave with a transportable version of the readout system used for the stave QA (see section 3). The QA configuration files were used as starting points. All chips were still operational and the calibration results, as shown in figure 8, are comparable to the ones obtained in the QA setup (not shown here, but available in [7]).

5 Towards bake out and operation

The next steps towards Run 2 of the LHC were the cold operation of the Inner Detector, the bake-out of the new beam pipe and combined cosmics data taking of all subsystems of the ATLAS detector.

---

12IBL Support Tube.
13IBL Positioning Tube.
Figure 9. (a) Photograph of the thermal mockup at CERN and (b) CFD simulations of the temperature distribution in IBL for the foreseen beam pipe bake out.

| Table 1. Comparison of CFD calculations and measurements performed with the thermal mock-up. |
|------------------------------------------------------------------------------------------|
| Measurements | CFD calculations |
|---------------|-----------------|
| Cooling lines  | $-19.2^\circ\text{C}$ | $-19.2^\circ\text{C}$ |
| Cold staves   | $-18.7^\circ\text{C}$ | $-17.7^\circ\text{C}$ |
| $T_{IP}$ at $Z_0$, north            | $+92.5^\circ\text{C}$ | $+92.7^\circ\text{C}$ |
| $T_{IST}$ at $Z_0$, north/south     | $+18.5^\circ\text{C}/+9.2^\circ\text{C}$ | $+13.4^\circ\text{C}/+5.3^\circ\text{C}$ |
| Central heater dissipation at $Z_0$  | 212 W/m | 154 W/m |

The new beam pipe which was integrated in the IBL package needed to be baked out to reduce thermal outgassing and to activate the Non Evaporable Getter (NEG) coating on the inside of the beam pipe. This is a crucial procedure for the targeted LHC vacuum. To understand the conditions during the beam pipe bake-out, CFD\textsuperscript{14} simulations were run (see figure 9(b)). In addition to those, a real size IBL thermal mock-up (figure 9(a)) was built and installed in CERN SR1 clean room. It was operated with a 1000 W CO\textsubscript{2} cooling plant connected to stainless steel pipes running in aluminum staves in the mock up. Various heaters as well as temperature and humidity sensors were largely distributed over the entire mockup. Only every second stave could be cooled in that setup. However, comparing the results from the cold staves to the CFD simulation during bake-out, one can see that they are in very good agreement (see table 1). The beam pipe bake-out was performed at $220^\circ\text{C}$. The stave temperatures, however, were not meant not exceed $+40^\circ\text{C}$ which resulted in a substantial temperature gradient over just a few mm. With the help of the simulations and the mock-up it could be shown that the detector will remain unharmed during the bake-out if the coolant is set to $-20^\circ\text{C}$.

6 Conclusion

The IBL is the fourth layer of silicon pixel detectors in ATLAS, foreseen to take data up to the high luminosity upgrade of the LHC. All components used for the ATLAS IBL were built and found to

\textsuperscript{14}Computational Fluid Dynamics.
meet the demanding requirements described above with respect to engineering constraints, operational stability, calibration performance and radiation hardness. Eventually the 14 best were chosen to build the IBL. All modules were functional after integration and 99.9% of the pixels were working. The installation into the ATLAS Detector was successful and no damages were observed. Also the beam pipe bake out left the detector unharmed and first cosmic data in combination with other ATLAS sub-detectors was taken. The DAQ integration into the existing ATLAS frame is ongoing.

Acknowledgments

Work supported by the Wolfgang-Gentner-Programme of the Bundesministerium für Bildung und Forschung (BMBF).

References

[1] ATLAS collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, 2008 JINST 3 S08003.
[2] G. Aad et al., ATLAS pixel detector electronics and sensors, 2008 JINST 3 P07007.
[3] ATLAS collaboration, ATLAS Insertable B-Layer technical design report, CERN-LHCC-2010-013 (2010) [ATLAS-TDR-019].
[4] ATLAS IBL collaboration, Prototype ATLAS IBL modules using the FE-I4A front-end readout chip, 2014 JINST 7 P11010.
[5] M. Garcia-Sciveres et al., The FE-I4 pixel readout integrated circuit, Nucl. Instrum. Meth. A 636 (2011) S155.
[6] ATLAS collaboration, ATLAS Pixel IBL: stave quality assurance, ATL-INDET-PUB-2014-006 (2014).
[7] ATLAS collaboration, https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsPixel (2014).