Using the PALS Architecture to Verify a Distributed Topology Control Protocol for Wireless Multi-Hop Networks in the Presence of Node Failures

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The PALS architecture reduces distributed, real-time asynchronous system design to the design of a synchronous system under reasonable requirements. Assuming logical synchrony leads to fewer system behaviors and provides a conceptually simpler paradigm for engineering purposes. One of the current limitations of the framework is that from a set of independent “synchronous machines”, one must compose the entire synchronous system by hand, which is tedious and error-prone. We use Maude’s meta-level to automatically generate a synchronous composition from user-provided component machines and a description of how the machines communicate with each other. We then use the new capabilities to verify the correctness of a distributed topology control protocol for wireless networks in the presence of nodes that may fail.

1 Introduction

The design and verification of a distributed embedded system (DES) such as those in avionics, cars, medical systems, and sensor networks, poses serious challenges for formal verification, particularly for model checking verification, for at least two reasons: (i) their real-time nature has to be taken into consideration in their modeling and verification, and this usually makes verification harder or may require restrictions such as the use of time-bounded properties; (ii) their distributed nature can easily cause an explosion in the size of the state space, making it infeasible for a model checker to verify a system.

The Physically Asynchronous but Logically Synchronous (PALS) architectural pattern [7, 6, 9, 8] has been recently introduced to greatly reduce the design, verification, and implementation efforts for a large class of DES systems, including many in avionics applications, which can be conceptually conceived to operate in a synchronous way, but which are in fact implemented as asynchronous systems. Up to now, the design of such systems has been very labor-intensive and error-prone, and their formal verification has been infeasible due to state space explosion even for modest-sized systems. The essence of the PALS idea is to allow the designer and formal verifier to specify the system as a synchronous composition of abstract machines, and to then automatically derive from this synchronous design a corresponding asynchronous version which is correct by construction.

Conceptually, PALS can be understood as a model transformation, which takes as arguments both the simpler synchronous design and a collection of performance-related upper bounds, such as the maximum clock skew in an underlying clock synchronization algorithm, the maximum network delay for message transmission between any two components, and the maximum computation time for an abstract machine to perform a one-step transition. The result of the PALS transformation is the corresponding
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asynchronous system that will correctly realize the synchronous design with a provable minimal time period of operation.

For model checking verification purposes, the great advantage of using PALS is that the two difficulties (i)–(ii) described above for DES model checking verification are greatly reduced. Difficulty (i), their real-time nature, completely goes away, since the synchronous system can be viewed as a single abstract machine obtained by composing the different machines connected together in the design. Such a single abstract machine, together with its environment specification, can then be treated as an ordinary Kripke structure with no explicit real-time features, and can therefore be reasoned about with standard model checkers. Difficulty (ii) is enormously reduced, because what in the synchronous model corresponds to a single state transition is achieved in its asynchronous version by possibly many transitions (at least one per distributed component), with possibly many interleavings. This means that the synchronous model will typically have many fewer states than the asynchronous one, so that it may be often possible to model check the synchronous model while it is infeasible to do so for its asynchronous version. Because of the semantic equivalence between a synchronous design and its PALS asynchronous transform, both systems satisfy the same temporal logic properties, so that it is enough to verify the much simpler synchronous design.

For the moment, the potential of PALS has not yet been fully exploited at the formal specification and verification levels in languages such as Maude and Real-Time Maude. For this to happen, two important theory transformations need to be supported and automated, namely:

1. the transformation performing the synchronous composition of a collection of abstract machines as specified by a wiring diagram connecting those machines; and

2. the PALS transformation itself, which takes the collection of such machines and their wiring together with the performance parameters and produces the equivalent asynchronous model.

Thanks to the reflective features of rewriting logic and their Maude support by its META-LEVEL module, transformations (1) and (2) can be specified within Maude as reflective module transformations. Note, however, that for model checking verification purposes, since only the synchronous model needs to be verified, only transformation (1) is needed.

This paper addresses this need for supporting PALS in Maude and Real-Time Maude and makes the following contributions:

- It provides a meta-level implementation in Maude of transformation (1) which is both parametric on the wiring diagram and generic on the actual abstract machines that may then be composed according to the specified diagram.

- It applies the PALS transformation for the first time to an application in the area of sensor networks, illustrating how it can be used to greatly simplify the formal verification of a topology control protocol (LMST) in the presence of failures, so that some of the nodes may fail.

- It illustrates by the LMST example a more general method by which real-time distributed object-based systems can be modeled in a much simpler synchronous way using the PALS architecture, provided that the objects in the system in question are supposed to only communicate with each other at pre-established times, and change their state at those times only as a result of the messages they then receive.

The remainder of the paper is organized as follows. Section 2 reviews the PALS framework, in particular the synchronous model of design. Section 3 then describes our generic implementation in Maude for combining many independent synchronous machines into one large machine, accomplishing transformation (1) above. In Section 4 we then describe the LMST topology control protocol, our modeling
of it in PALS using the methods of Section 3 and prove its correctness with respect to node failure using Maude’s LTL model checker. Finally, Section 5 contains some concluding remarks and discusses future work.

2 Background: The PALS Synchronous Model

To design a distributed, real-time system with the PALS architecture [7, 6, 9, 8], one starts with a synchronous model of the system; then, a very general transformation, formally specified in [7, 6], takes the synchronous model into an asynchronous one suitable for deployment. A certain kind of bisimulation between the two systems (see [7, 6]) allows one to reduce (a) verification of a property against the asynchronous machine to (b) verification of the property against the synchronous design; where the properties in question are given by temporal logic formulae. The synchronous machine typically has a much smaller state space and can therefore be model checked more efficiently.

In this paper we are concerned only with the synchronous model (for information on the asynchronous model and transformation, see [7, 6]), the key notions of which are synchronous machines, environment, and wiring diagram. Consider the small logic circuit given in Figure 1. In terms of the synchronous model, it is comprised of three synchronous machines, $M_1 - M_3$, an environment defined by the unconnected wires at the boundary box, and a wiring diagram specifying that the two xor gates get their inputs from the environment and send their outputs to the and gate, which finally outputs its result to the environment.

Formally, a component machine $M$ is defined as a four-tuple, $(D_i, S, D_o, \delta : D_i \times S \rightarrow S \times D_o)$, where $D_i = D_{i_1} \times \cdots \times D_{i_n}, n \geq 1$, specifies the inputs to the machine, $D_o = D_{o_1} \times \cdots \times D_{o_m}, m \geq 1$, specifies the outputs of the machine, $S$ is its internal state, and $\delta$ is its transition function, specifying how the state is updated and what outputs are produced from a given input and current state. Each of the component input types $D_{i_1}, \ldots, D_{i_n}$ and component output types $D_{o_1}, \ldots, D_{o_m}$ are assumed to be non-empty; for technical reasons, it is also assumed that $S \neq \emptyset$.

An environment is a pair $(D^e_i, D^e_o)$ with $D^e_i = D^e_{i_1} \times \cdots \times D^e_{i_{ne}}, ne \geq 1$, the set of inputs to the environment, and $D^e_o = D^e_{o_1} \times \cdots \times D^e_{o_{me}}, me \geq 1$, the output from the environment. Again, each of the $D^e_{i_1}, \ldots, D^e_{i_{ne}}$ and $D^e_{o_1}, \ldots, D^e_{o_{me}}$ are assumed to be non-empty.
Let \( \{M_j\}_{j \in J} \) be a \((J)\) indexed set of machines and \( E = (D^e_i, D^e_o) \) an environment. A wiring diagram for \( \{M_j\}_{j \in J} \) and \( E \) is a function \( \text{src} : I \rightarrow O \), where

\[
I = \{ (j, n) \in (J \cup \{e\}) \times \mathbb{N} \mid 1 \leq n \leq n_j \} \quad \text{and} \quad O = \{ (j, n) \in (J \cup \{e\}) \times \mathbb{N} \mid 1 \leq n \leq m_j \},
\]

that maps each input port to the output port, or source, from which it receives data. Ports exist as part of the component machines, \( \{M_j\}_{j \in J} \), or as part of the environment, \( E \).

Returning to the example in Figure 1, each of the machines \( M_1 \) – \( M_3 \) have as input set \( B^2 \), and as output set \( B \); they have no internal state, but because the \( S \) component is required to be non-empty we represent the internal state with the unit type, we we denote by \( \{\star\} \). The output part of their transition functions perform exclusive-or in the case of \( M_1 \) and \( M_2 \), and logical and in the case of \( M_3 \). The input type of the environment is \( B \), since there is one input to the environment, and output type \( B^4 \), since the environment furnishes four values to the machine. The wiring diagram, src, is given by

\[
(1, 1) \mapsto (e, 1), \quad (1, 2) \mapsto (e, 2), \quad (2, 1) \mapsto (e, 3),
\]

\[
(2, 2) \mapsto (e, 4), \quad (3, 1) \mapsto (1, 1), \quad (3, 2) \mapsto (2, 1),
\]

\[
(e, 1) \mapsto (3, 1).
\]

The composed machine operates just like the logic circuit, with values propagating through one level of logic gate per round. This could, for example, represent the time it takes for values to propagate through the logic elements to the output of the circuit.

### 3 Automatic Synchronous Composition

We now describe the infrastructure we have built in Maude to compose a set of synchronous machines into one larger machine, as illustrated above in Section 2 when we composed the three logic gates into a circuit. Given (a) for each machine \( M_j \), values \( n_j, m_j \) specifying the number of inputs and outputs, respectively, of \( M_j \), (b) values \( n_e, m_e \) for the number of inputs and outputs of the environment, and (c) a wiring diagram, we automatically generate a parameterized module [1, Ch. 10] corresponding to the synchronous composition of a set of abstract (\( \delta \) unspecified) machines composed according to the given wiring diagram. This is accomplished using Maude’s meta-level [1, Ch. 14]. The module has a fixed topology, but is generic in the operation of the individual synchronous machines. The discussion in this section assumes a firm understanding of parameterized and meta-level programming in Maude (see [1] for a review).

Parameterized programming in Maude uses the notions of “theories” and “views” (see [1, §8.3.1] and [1, §8.3.2]). Theories are used to specify a parameter’s interface, and views are used to instantiate an interface. Theories are like regular functional and system modules in Maude, except that they do not need to satisfy the same conditions for executability. In general, they also may omit constructors for defined sorts or equations defining the declared operators since these will be mapped to other sorts and functions later, using a view. However, they can state axioms that any instance of the symbols in the parameter theory must satisfy.

For (a) above, the user provides a term of sort Machines:

\[
\text{including MAP\{NzNat,IOSize\} * (sort Map\{NzNat,IOSize\} to Machines}).
\]
presumed to give a mapping from a prefix of the non-zero natural numbers, isomorphic to the index set \( J \), to pairs of numbers \((n_j, m_j)\), the number of inputs and outputs of \( M_j \), respectively. The sort for this pair of numbers is \( \text{IOSize} \), defined with the following constructor

\[
\text{op } _\#_ : \text{NzNat NzNat} \rightarrow \text{IOSize} \quad \text{[ctor]}
\]

With a term of sort \( \text{Machines} \), it is possible to generate the set of parameters for the \( \{ M_j \}_{j \in J} \). We simply iterate through the mappings, creating a new parameter for each \((n_j, m_j)\) pair requiring a view for a theory

\[
\text{op smParams : Machines NzNat} \rightarrow \text{ParameterDeclList}.
\]

\[
\text{eq smParams(MS, J) =}
\begin{array}{l}
\text{if } \$\text{hasMapping(MS, J)} \\
\quad \text{then index('M, J) :: mkP(MS[J])} \\
\quad \text{else nil fi} .
\end{array}
\]

\[
\text{op mkP : IOSize} \rightarrow \text{Qid}.
\]

\[
\text{eq mkP(N # M) = -index(-index('SM, N), M).}
\]

The functions \( \text{index} \) and \( \text{-index} \) take a \( \text{Qid} \) and a \( \text{Nat} \) and produce a new \( \text{Qid} \); for example, \( \text{index('M, 1)} = \text{'M1} \) and \( \text{-index('M, 1)} = \text{'M-1} \). The sort \( \text{ParameterDeclList} \) is pre-defined in the Maude prelude, in module \( \text{META-MODULE} \), using the following constructors which are syntactically similar to the source-level representation of parameters in a parameterized module

\[
\text{op } _::_ : \text{Sort ModuleExpression} \rightarrow \text{ParameterDecl}.
\]

\[
\text{op } _,_ : \text{ParameterDeclList ParameterDeclList} \\
\rightarrow \text{ParameterDeclList} \quad \text{[ctor assoc id: nil prec 121]}
\]

The operator \( \$\text{hasMapping} \) is pre-defined in the \( \text{MAP} \) module; it determines whether a given term has a mapping, and we use it to determine when we are finished iterating through the \(|J|\) modules.

We assume a set of theories, \( \{ \text{SM-}n_j-m_j \}_{j \in J} \), giving a general interface for a synchronous machine with \( n_j \) inputs and \( m_j \) outputs; the general form of \( \text{SM-}n_j-m_j \) is given in Figure 2, it specifies the component input and output sorts, product types for the input and output, projection functions, and a split transition function. Figure 3 shows how to instantiate a view of \( \text{SM-2-1} \) corresponding to a “synchronous machine” for the two xor gates given above in Figure 1. The \( \text{TUPLE} \) module operation provides a very general way to create product types (see [1, §18.3.1]); it only works in Full Maude [1, Part II], but by a slight abuse of notation we employ it in Figure 3 and throughout this document, as if it can be used in Core Maude [1, Part I]; also, we call the projection functions \( \text{p1, etc.} \) instead of \( \text{p1} \), which is used in [1, §18.3.1]. In addition, it is worth noting that while it would be nice to use the \( \text{TUPLE}[,] \) module operation in the \( \text{SM-n-m} \) theories, parameterized theories are not currently allowed in Maude.

Consider again the example of Figure 1. The corresponding \( \text{Machines} \) is given by

\[
1 \rightarrow 2 \ # \ 1, \ 2 \rightarrow 2 \ # \ 1, \ 3 \rightarrow 2 \ # \ 1
\]

and the value produced by \( \text{smParams} \) is

\[
\text{'M1 :: 'SM-2-1, 'M2 :: 'SM-2-1, 'M3 :: 'SM-2-1}
\]

The values \( n_e, m_e \), provided by the user and corresponding to (b) above, determine the interface of the \( \text{environment} \), just as the \( n_j, m_j \) determined the interface to the component synchronous machines. Similar to the \( \text{SM-n-m} \) theories, we assume theories \( \text{E-n-m} \) for the environments. These are exactly the same as the \( \text{SM-n-m} \) theories, except that they omit the sort \( S \) and the transition functions \( \text{delta1} \) and \( \text{delta2} \). Therefore, to generate the header for the module giving the synchronous composition of a set of machines we can simply use
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fth SM-\(n-m\) is
\[\text{sorts } Di \ Di-1 \ldots Di-n\]
\[\text{op } \langle\ldots, \ldots, \ldots \rangle : \text{Di-1} \ldots \text{Di-n } \rightarrow \text{Di} \text{ [ctor]} \]
\[\text{op pi1 : Di } \rightarrow \text{Di-1} \]
\[\text{eq pi1(( X1:Di-1, \ldots )) } = X1: \text{Di-1} \]
\[\ldots\]
\[\text{op pin : Di } \rightarrow \text{Di-n} \]
\[\text{eq pin(( \ldots, Xn:Di-n )) } = Xn: \text{Di-n} \]
\[\text{sort S} \]
\[\text{sorts Do Do-1 \ldots Do-m} \]
\[\text{op } \langle\ldots, \ldots, \ldots \rangle : \text{Do-1} \ldots \text{Do-m } \rightarrow \text{Do} \text{ [ctor]} \]
\[\text{op pi1 : Do } \rightarrow \text{Do-1} \]
\[\text{eq pi1(( X1:Do-1, \ldots )) } = X1: \text{Do-1} \]
\[\ldots\]
\[\text{op pin } : \text{Do } \rightarrow \text{Do-m} \]
\[\text{eq pin(( \ldots, Xm:Do-m )) } = Xm: \text{Do-m} \]
\[\text{op delta1 : Di S } \rightarrow \text{S} \]
\[\text{op delta2 : Di S } \rightarrow \text{Do} \]
endfth

Figure 2: The “functional theory” for a synchronous machine with \(n\) inputs and \(m\) outputs.

op scHeader : Machines IOSize -> Header .
\[\text{eq scHeader(MS, N # M) } = \]
\[\text{'SC } \{ \text{smParams(MS, 1), E :: -index(-index('E, N), M) } \} \text{ .}\]

The third component, (c) above, that we need to give is the wiring diagram. A wiring diagram is treated as a mapping between ports, where a port is defined as follows:

| sort MIdx . subsort NzNat < MIdx . |
| op e : -> MIdx [ctor] . |
| sort Port . |
| op \(\langle\ldots, \ldots\rangle : \text{MIdx NzNat } \rightarrow \text{Port [ctor]} \) . |

Then, a wiring diagram is just (with a view for ports instantiated in the obvious way)

\[
\text{including MAP(Port,Port) } \ast (\text{sort Map(Port,Port) to Wiring}) \text{ .}
\]

To generate a module for the synchronous composition of machines \(\{M_j\}_{j \in J}\), and environment \(E\), and a wiring diagram src, we have a function

\[\text{op gensc : Machines IOSize Wiring } \rightarrow \text{Module} .\]

where the arguments correspond to the three pieces of information, (a) – (c) respectively, above. The composed machine will be denoted by \(E\), following the notation of \(\text{[7]} \text{[6]}\).

The meta-level sort Module in META-MODULE contains the following constructor for functional modules

\[\text{op fmod_is_sorts_.____endfm : Header ImportList SortSet SubsortDeclSet OpDeclSet MembAxSet EquationSet } \rightarrow \text{Module [ctor} \ldots\] \text{].}\n
The function gensc is defined at the top level by instantiating each of the arguments of the above operator as explained below
fmod XOR2 is
  including BOOL .
  including UNIT .
  including TUPLE[2]{Bool,Bool} *
    (sort TUPLE[2]{Bool,Bool} to Bool^2) .
  including TUPLE[1]{Bool} *
    (sort TUPLE[1]{Bool} to Bool^1) .
var I : Bool^2 .
var S : Unit .
op delta1 : Bool^2 Unit -> Unit .
eq delta1(I, S) = .
op delta2 : Bool^2 Unit -> Bool^1 .
eq delta2(I, S) =
  ( pi1(I) xor pi2(I) ) .
endfm

(a) Synchronous machine for an xor gate.

view Xor2 from SM-2-1 to XOR2 is
  sort Di-1 to Bool .
  sort Di-2 to Bool .
  sort S to Unit .
  sort Do-1 to Bool .
endv

(b) View of the xor gate in the appropriate theory.

Figure 3: Instantiating a synchronous machine for the xor gate using a view.

eq gensc(MS, E, W) =
  fmod
    scHeader (MS, E, W) is
      nil
    sorts
      scSorts (MS, E, W) .
      scSubsorts(MS, E, W)
      scOpDecls (MS, E, W)
      none
    scEqs (MS, E, W)
  endfm .

The implementation of scHeader is given above (albeit with the third argument omitted, since it is unused and Wiring had not been introduced). For scSorts we simply need to give names for the relevant sorts of $E$: (1) the input type for the composed machine, $D_i^E$, (2) the state type, $S^E$, and (3) the output type, $D_o^E$.

op scSorts : Machines IOSize Wiring -> SortSet .
eq scSorts(MS, E, W) = 'Di^E ; 'Do^E ; 'S^E .

Let us jump ahead briefly to define the internal state of $E$, i.e., the constructor for sort $S^E$, since it requires the notion of internal node, which we will need when defining scSubsorts. Let

$$N^E = \{(j,m) \in J \times N \mid \exists (j',n) \in J \times N \text{ s.t. src}(j',n) = (j,m)\};$$

$N^E$ is called the set of internal nodes. Then, the state of $E$ is defined as

$$\prod_{j \in J} S_j \times \prod_{(j,m) \in N} D_{o_m}^j$$

where $D_{o_m}$ denotes the sort of the $m^{th}$ output of machine $M_j$. For example, the set of internal nodes for the circuit in Figure 1 is $\{(1,1),(2,1)\}$, the outputs of the xor gates; therefore we generate an OpDecl for the state constructor as follows (where the parameters are assumed to be the same as above).
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The general case is somewhat more tedious, but straightforward in the way described above; for details, see our implementation [2].

The component for subsorts, scSubsorts, is relatively simple to define, but fraught with a subtle difficulty. To start with, we generate subsort declarations for $Di^E$ and $Do^E$, the inputs and outputs of the composed module $E$, respectively;

\[
\begin{align*}
\text{(subsort 'E$Do < 'Di$E .) } \\
\text{(subsort 'E$Di < 'Do$E .)}
\end{align*}
\]

We also need to give subsort declarations for input-output port matchings, for example, to assert that the output sort of the xor gate $M_1$ is a subsort of the first input of the and gate $M_3$

\[
\text{(subsort 'M1$Do-1 < 'M3$Di-1 .)}
\]

The subtle difficulty is that in Maude the semantics of \textit{subsort} is that the sort on the left-hand side of the \textless symbol is a \textit{proper} subsort of the sort on the right-hand side. Therefore, when using this module for the circuit in Figure 1, one must guarantee that the input sorts to the and gate are strict supersorts of the inputs. To maintain the genericity of the parameterized module, this seems unavoidable, but one could go to a less generic solution where this problem would go away. In practice, we have just added unit (\texttt{⋆}) to the input type, e.g.,

\[
\text{sort Bool+ . op * : } \rightarrow \text{Bool+ [ctor] .}
\]

Finally, we must generate operators and equations for the transition function of $E$. The operator declarations are straightforward

\[
\begin{align*}
\text{(op 'delta1$E : 'Di$E 'S$E } \rightarrow \text{'S$E [none] .) } \\
\text{(op 'delta2$E : 'Di$E 'S$E } \rightarrow \text{'Do$E [none] .)}
\end{align*}
\]

The equational definition of the above functions follows the description given in [7] [6]. The details of the general case are too tedious to present here, but in Figure 4 is shown the result of applying gensc to the appropriate arguments for the circuit in Figure 1. For full details, see our implementation [2].

The last step is to instantiate the generated module with the appropriate views. For example, for the circuit in Figure 1 we use views like the one given in Figure 3.

\[
\text{fmod USE-SC is} \\
\text{including SC{Xor2,Xor2,And2,Env} .} \\
\text{endfm}
\]

One small difficulty in using the generated module is that it requires capturing it, saving to a file, and then instantiating it with appropriate views for the component machines and the environment. Of course, some small changes need to be made for this to work, such as removing the quotes from the quoted identifiers, but it is easy to write a small script for this purpose. It would of course be more elegant to do this entirely inside of Maude, but unfortunately the operations provided by \texttt{META-LEVEL} make this difficult. The essential problem is that because we are generating a \textit{parameterized} module at the meta-level, to use it we need to \textit{instantiate} it, and that requires generating a second meta-level module. However, meta-level functions such as

\[
\text{op metaReduce : Module Term } \rightarrow \text{ResultPair}
\]

take as an argument just a \textit{single} module, and not a module \textit{set}; which we would need to capture both the generated parameterized module and its instantiation. It may simply be better to generate a specialized, but non-parameterized module instead of the parameterized one.
fmod SC{M1 :: SM-2-1,M2 :: SM-2-1,M3 :: SM-2-1,E :: E-1-4} is
sorts Di^E Do^E S^E.
subsort E$Di < Do^E.
subsort E$Do < Di^E.
subsort E$Do-1 < M1$Di-1.
subsort E$Do-2 < M1$Di-2.
subsort E$Do-3 < M2$Di-1.
subsort E$Do-4 < M2$Di-2.
subsort M1$Do-1 < M3$Di-1.
subsort M2$Do-1 < M3$Di-2.
subsort M3$Do-1 < E$Di-1.
subsort M3$Do < E$Di.

op '(_', '_', '_', '_', '_') : M1$S M2$S M3$S M1$Do-1 M2$Do-1 -> S^E [ctor].
op pi1 : S^E -> M1$S.
op pi2 : S^E -> M2$S.
op pi3 : S^E -> M3$S.
op pi-1-1 : S^E -> M1$Do-1.
op pi-2-1 : S^E -> M2$Do-1.
op delta1^E : Di^E S^E -> S^E.
op delta2^E : Di^E S^E -> Do^E.

eq pi1 (((X1:M1$S,X2:M2$S,X3:M3$S,X4:M1$Do-1,X5:M2$Do-1))) = X1:M1$S.
eq pi2 (((X1:M1$S,X2:M2$S,X3:M3$S,X4:M1$Do-1,X5:M2$Do-1))) = X2:M2$S.
eq pi3 (((X1:M1$S,X2:M2$S,X3:M3$S,X4:M1$Do-1,X5:M2$Do-1))) = X3:M3$S.
eq pi-1-1(((X1:M1$S,X2:M2$S,X3:M3$S,X4:M1$Do-1,X5:M2$Do-1))) = X4:M1$Do-1.
eq pi-2-1(((X1:M1$S,X2:M2$S,X3:M3$S,X4:M1$Do-1,X5:M2$Do-1))) = X5:M2$Do-1.
eq delta1^E(X:Di^E,Y:S^E) =
  ( delta1((pi1(X:Di^E),pi2(X:Di^E)),pi1(Y:S^E))
  , delta1((pi3(X:Di^E),pi4(X:Di^E)),pi2(Y:S^E))
  , delta1((pi-1-1(Y:S^E),pi-2-1(Y:S^E)),pi3(Y:S^E))
  , pi1(delta2((pi1(X:Di^E),pi2(X:Di^E)),pi1(Y:S^E)))
  , pi1(delta2((pi3(X:Di^E),pi4(X:Di^E)),pi2(Y:S^E))))
).
eq delta2^E(X:Di^E,Y:S^E) =
  ( pi1(delta2((pi-1-1(Y:S^E),pi-2-1(Y:S^E)),pi3(Y:S^E))) )
.endfm

Figure 4: The parameterized module for the small circuit.
4 Verifying LMST in the Presence of Failures using PALS

We now utilize the infrastructure described above to verify the correct operation of the local minimum spanning tree protocol in the presence of node failures. We begin with a brief introduction to the protocol, what it aims to achieve and its basic operation, in Section 4.1. Then, we show how to verify the correctness of the LMST protocol with respect to node failure. This entails showing how each individual node is implemented as a synchronous machine of the kind described above (Section 4.2), composing the nodes, modeling the environment, and performing the final verification (Section 4.3).

4.1 The LMST Protocol

The purpose of a topology control protocol is to define which nodes in an ad-hoc wireless sensor network communicate with each other, and with what transmission power they communicate. The goal is to minimize power consumption, prolong network lifetime, and maximize data bandwidth while maintaining network connectivity.

In the case of the LMST protocol, a distributed, real-time algorithm is employed whereby each sensor node periodically updates its own local topology. The local topology of a node is the set of neighboring nodes to which it routes data. Each wireless node is a machine with internal quartz clock timers, a memory for buffering messages, and a wireless transmitter which is adjustable to different power levels.

The periodic, real-time nature of the protocol is governed by a global constant called the round time, denoted rd, and each node constantly employs one of its timers, called the round timer, to count the time between round boundaries. When the round timer indicates that a new round has started the node adjusts its local topology by changing its wireless transmission strength.

There are therefore two notions of a round, one global and one local. A global round is any real-world interval \([t, t + rd]\) where \(t\) is a multiple of \(rd\). A local round is an individual node’s perception of the global, and is defined as any interval between successive expirations of the node’s local round timer, which may not keep perfect time with respect to the real-world.

The protocol is then defined by what happens when the local round timer of a node expires:
1. The node first broadcasts a message, called a hello message, at maximum transmission strength. The hello message contains a unique identifier of the node and its current physical location. Hello messages are buffered by any visible neighbor, that is, any node within wireless transmission range.

2. The node reads from its message buffer all hello messages received during the previous round and distills from these a graph of its visible neighbors weighted by distance.

3. Taking the local graph of visible neighbors just distilled by the node, it then calculates the minimum spanning tree of that graph.

4. The nodes in the local minimum spanning tree which are directly connected (one-hop away) are selected to be the node’s new neighbors, meaning those to which it will transmit data during this local round. The node then scales its transmission power so that it can just reach the furthest of these neighbors.

5. The node resets its round timer for rd, and waits for the timer to expire.

As shown in [5], LMST has a number of advantageous properties, including low power usage, and a provably small number of neighbors for each node, which reduces medium contention and increases bandwidth. Furthermore, it is also shown that LMST satisfies the crucial property of maintaining network connectivity. That is, if the graph whose edges link the sensor nodes within wireless reach of each other is connected, then the considerably smaller subgraph computed by LMST is also connected.

However, as described the protocol is somewhat idealized; it does not take into account issues that must be faced in a real implementation such as medium contention and node mobility. For the purpose of this paper, we ignore such issues. For more information of formally analyzing the LMST protocol in a more realistic setting, see [3].

### 4.2 LMST Nodes as PALS Synchronous Machines

We now demonstrate an application of the PALS architecture to verify the correctness of the LMST protocol in the presence of node failure. To do this we use the infrastructure of Section [3] treating the wireless nodes as individual synchronous machines and the environment as the determiner of which nodes fail during a given step. Correctness is established by showing that disconnectedness can only occur during a round when a node has failed. This section treats just the construction of LMST nodes as synchronous machines, the modeling of the environment and formula we verify the system against are described in Section [4.3]. Assume that all of the definitions below go into a module LMST-NODE, which we will use when we instantiate the view associated with it at the end of this section.

For the sake of concreteness we consider a network with five nodes, $N_1, \ldots, N_5$, with an all-to-all topology. However, nodes will ignore any hello message when it is outside the maximum range of the sending node. Furthermore, nodes that fail will output a special token, nomsg, indicating that no message was broadcast.
Using PALS

\begin{verbatim}
pr TUPLE[3]{NzNat,Nat,Nat} *( sort Tuple{NzNat,Nat,Nat} to Msg
 , op pi1 to id
 , op pi2 to xcoord
 , op pi3 to ycoord
).

sort Msg+. subsort Msg < Msg+ .
op nomsg : -> Msg+ [ctor] .
\end{verbatim}

Given the all-to-all topology and the environment as described above, each node will have five inputs: four hello message lines, one each from each of the other nodes, and one from the environment determining if the node fails during the current round. The input type for $N_1, \ldots, N_5$ is therefore given by

\begin{verbatim}
pr TUPLE[5]{Msg+,Msg+,Msg+,Msg+,Status} *
 (sort Tuple{Msg+,Msg+,Msg+,Msg+,Status} to RealInput).

sort Di . subsort RealInput < Di .
op * : -> Di [ctor] .
\end{verbatim}

The additional constructor $\ast$ is necessary because of the semantics of subsort in Maude, as described above in Section 3. The sort (with corresponding view) Status contains two values associated with constants, fail and ok. Note the sort name Di corresponds to a sort assumed in each of the SM-$n$-$m$. This is convenient because it allows us to avoid an explicit mapping when we eventually define the views for each node $N_1, \ldots, N_5$.

For the state of each node, we again have to consider the two cases where the node is still running, or it has failed. If it is still running, it contains all of the information it needs to send a hello message plus its current routing table, which is a list of nodes to which it can route data through.

\begin{verbatim}
pr TUPLE[4]{NzNat,Nat,Nat,NzNatList} *
 (sort Tuple{NzNat,Nat,Nat,NzNatList} to NodeSt
 , op pi1 to id
 , op pi2 to xcoord
 , op pi3 to ycoord
 , op pi4 to routing
).

sort S . subsort NodeSt < S .
op failed : -> S [ctor] .
\end{verbatim}

Finally, the output type for each node just contains a single piece of information for the hello message broadcast.

\begin{verbatim}
pr TUPLE[1]{Msg+} *(sort Tuple{Msg+} to Do).
\end{verbatim}

Therefore, each of the nodes in the network will need to instantiate a view of SM-5-1, since each has five inputs and a single output.

We still need to define the transition function for each of the nodes $N_1, \ldots, N_5$. The transition function is exactly the same for each node.
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\[ \text{op } \Delta_1 : \text{Di } S \rightarrow S . \]
\[ \text{eq } \Delta_1(I, \text{failed}) = \text{failed} . \]
\[ \text{eq } \Delta_1(I, S) = \]
\[ \begin{cases} \text{failed} & \text{if } \pi_5(I) = \text{fail} \\ \text{id}(S), \text{xcoord}(S), \text{ycoord}(S), \text{routing}'(I, S) & \text{else} \end{cases} . \]

\[ \text{op } \Delta_2 : \text{Di } S \rightarrow \text{Do} . \]
\[ \text{eq } \Delta_2(I, \text{failed}) = (\text{nomsg}) . \]
\[ \text{eq } \Delta_2(I, S) = \]
\[ \begin{cases} (\text{nomsg}) & \text{if } \pi_5(I) = \text{fail} \\ ((\text{id}(S), \text{xcoord}(S), \text{ycoord}(S))) & \text{else} \end{cases} . \]

where \( \text{routing}' \) is defined according to the LMST algorithm given above in Section 4.1 and [5] (for implementation details with respect to our experiment, see [2]). Then, we can define a node simply by giving instantiating a view with the above sorts and functions as follows

\[ \text{view } \text{LMSTNode from SM-5-1 to LMST-NODE is} \]
\[ \text{endv} \]

The body is empty because the module LMST-NODE named its sorts and operators using the same names and with the same signature as the SM-5-1 theory.

4.3 Verification of LMST using PALS

With synchronous machines now for all of the nodes, we still must build the composed machine, model the environment, and write an appropriate correctness property. The first part is greatly eased by using the \text{gensc} function from Section 3 with an all-to-all wiring diagram, and an appropriate abstract environment, namely E-1-5. Taking the environment from something abstract to a concrete implementation is also straightforward, we essentially just need a rule for each subset of nodes that can fail during a round. To do this we first define an auxiliary function

\[ \text{op } \text{natToDi}^E : \text{Nat} \rightarrow \text{Di}^E . \]
\[ \text{eq } \text{natToDi}^E(X) = \]
\[ \begin{cases} \text{fail} & \text{if } (X \& (1 << 0)) > 0 \\ \text{ok} & \text{else} \end{cases} \]
\[ \text{if } (X \& (1 << 1)) > 0 \text{ then fail else ok fi} \]
\[ \text{if } (X \& (1 << 2)) > 0 \text{ then fail else ok fi} \]
\[ \text{if } (X \& (1 << 3)) > 0 \text{ then fail else ok fi} \]
\[ \text{if } (X \& (1 << 4)) > 0 \text{ then fail else ok fi} \]

Where \& is an operator for bit-wise and, and \text{<<} is left-shift. As an example, to generate an input where every node but the first one, \( M_1 \), fails, we simply use \text{natToDi}^E(1) which evaluates to

\[ (\text{ok}, \text{fail}, \text{fail}, \text{fail}) \]

The sort \( \text{Di}^E \) is just the automatically generated type via \text{gensc}, specifically (recalling from Section 3)

\[ \text{(subsort 'E$Do < 'Di}^E .) \]

which is just a 5-tuple with every component of sort \text{Status}, that is, exactly the information we expect from the environment. Then, we add a \text{rule} to non-deterministically generate any possible output from the environment (equivalently, \text{input} to the device) at each step
Using PALS

\[
\text{crl [fromEnv]} : S \Rightarrow \text{delta}^E(I, S) .
\]
\[
\text{if } I, IS := \text{possibleInputsSet}
\]

where possibleInputsSet is a set all possible values of sort Di^E. Using the function natToDi^E above, it is straightforward to generate

\[
\text{op genDi^EUpTo : Nat } \rightarrow \text{Set(Di^E)} .
\]
\[
\text{eq genDi^EUpTo}(0) = \text{natToDi^E}(0) .
\]
\[
\text{eq genDi^EUpTo}(s(X)) = \text{natToDi^E}(s(X)) , \text{genDi^EUpTo}(X) .
\]

\[
\text{op possibleInputsSet : } \rightarrow \text{Set(Di^E)} .
\]
\[
\text{eq possibleInputsSet} = \text{genDi^EUpTo}(31) .
\]

We still need to define a notion of correctness for LMST. At a high level we say that the protocol is correct if the network always stays connected whenever there are no new node failures during a round. The top-level LTL formula is given by

\[
\text{op correct? : } \rightarrow \text{Formula} .
\]
\[
\text{eq correct?} = O(\[
\text{no-new-failures?} \rightarrow (\text{connected?})\)) .
\]

which says, more precisely, that after the first time step it is always the case that whenever the set of failing nodes is \textit{stable}, then during the next round the network is \textit{connected}. The formula characterizing when there are no new node failures is defined as

\[
\text{op no-new-failures? : } \rightarrow \text{Formula} .
\]
\[
\text{eq no-new-failures?} =
\]
\[
\begin{align*}
\text{failed?(1) } &\leftrightarrow \text{0 failed?(1)} \land \\
\text{failed?(2) } &\leftrightarrow \text{0 failed?(2)} \land \\
\text{failed?(3) } &\leftrightarrow \text{0 failed?(3)} \land \\
\text{failed?(4) } &\leftrightarrow \text{0 failed?(4)} \land \\
\text{failed?(5) } &\leftrightarrow \text{0 failed?(5)}. \\
\end{align*}
\]
\[
\]
\[
\text{eq S |=} \text{failed?(1)} = \text{pi1(S) == failed} .
\]
\[
\text{eq S |=} \text{failed?(5)} = \text{pi5(S) == failed} .
\]

that is, that the failed proposition for each node is consistent between the current state and the next state for every node individually. The connected? formula is more complicated, but essentially it traverses the routing tables of all non-failed nodes to determine if there is a multi-hop route from each non-failed node to every other one (see [2] for details).

Finally, we can model check a 5 node system against correct? using Maude’s LTL model checker, showing that for the particular topology, LMST is correct in the presence of node failure. Therefore, any asynchronous implementation of the system had through the PALS transformation would satisfy the same notion of correctness.

Maude> red modelCheck(init, correct?) .
reduce in CHECK : modelCheck(init, correct?) .
rewrites: 317674 in 218ms cpu (226ms real) (1456678 rewrites/second)
result Bool: true
5 Conclusions

We have addressed the need to automatically support the synchronous composition of abstract machines within Maude so that the PALS architecture can be exploited for model checking purposes. This is accomplished via a meta-level module transformation in Maude that can automatically generate the single abstract machine which is the composition of an ensemble of abstract machines connected by a wiring diagram. The transformation makes it easy to verify a complex asynchronous DES system by model checking a much simpler synchronous version where the user is responsible only for the individual machine specifications and the wiring diagram.

We have then illustrated how this transformation can be applied to greatly simplify the formal verification of a key connectedness property in the LMST topology control protocol for sensor networks. As explained in the introduction, a sensor network protocol such as LMST is an example of a much broader class of distributed object-based DESs whose objects only communicate with each other at pre-established times, and which change their state at those times only as a result of the messages they then receive. It would be quite useful to identify other examples of systems within this category; also, the module transformation that we have presented could be specialized to object-based systems of this kind, so that it is not necessary to specify such objects explicitly as abstract machines.

Besides the extension of the present work just outlined, much work remains ahead. For example, what is called transformation (2) in the Introduction (passing from a synchronous model to its asynchronous PALS equivalent) should also be automated at the meta-level, not for verification purposes, but for purposes such as asynchronous design, code generation and also for system emulation in physical time, when Real-Time Maude specifications are transformed into actual real-time implementations.

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