Mechanism analysis of IGBT turn-on process

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Abstract. Based on the internal structure of IGBT, the characteristics of gate voltage, collector current and collector-emitter voltage of IGBT during its turn-on process are studied in this paper. The relationship between gate voltage and gate capacitance is given, and the rising process of gate voltage is described in detail. According to the characteristics of IGBT turn-on current, a quadratic function is proposed to fit the collector current waveform. The influence of the main circuit stray inductance on collector-emitter voltage waveform is also analyzed. Finally, the IGBT dynamic switch characteristic test platform is built, and the measurement results verify the correctness of the analysis.

1. Introduction

Insulated Gate Bipolar Transistor (IGBT) has the advantages of voltage control, fast switching speed and low on-state loss [1]. It is widely used in high-voltage large-capacity inverter, DC transmission and other fields [2-5]. In order to meet the application requirements, the IGBT package develops a high-power compression package combined the common advantages of IGBT and GTO [6, 7].

With the application of technologies such as carrier lifetime control, the IGBT turn-off loss has been significantly improved. On the other hand, the reverse recovery process of the internal freewheeling diode of the high-power IGBT device greatly increases the turn-on loss. Therefore, the turn-on process of IGBT has attracted much attention. The accurate IGBT turn-on model can evaluate the turn-on loss, tolerable electrical stress, and electromagnetic interference noise, so as to further improve the turn-on characteristics of IGBT [8, 9].

At present, the widely used IGBT switch models mainly include analytical model [10] and lumped charge model [11], both of which can be used for IGBT switch modeling, but the detailed analysis of IGBT turn-on mechanism is lacking. In view of the limitations of the above methods, the literature [12] considers the capacitive charging model of the drive circuit in the turn-on process, and analyzes the turn-on waveform of IGBT in stages, but does not explain the mechanism of miller plateau, and lack of the analysis of the interaction between gate voltage and collector-emitter voltage. The literature [13, 14] also analyze the relationship between collector current, collector-emitter voltage and gate voltage during the IGBT turn-on process, but all used the circuit method, lacking the analysis of the turn-on mechanism.

In this paper, the relationship between input capacitance and gate voltage is studied for the IGBT turn-on process under inductive load condition, and each phase of gate voltage during turn-on is described in detail. The rising characteristics of collector current and the falling characteristics of collector-emitter voltage of IGBT turn-on process are studied. The influence of the loop stray inductance on collector-emitter voltage is also revealed. Finally, the IGBT dynamic characteristic test
platform is built and the turn-on waveform of IGBT is obtained. The experimental results verify the correctness of the above analysis.

2. The internal structure of IGBT

The basic structure of cross section of IGBT chip is shown in Figure 1. P’ and N’ indicate that the collector and source regions are heavily doped, and N’ indicates that the base region has a lower doping concentration. Compared with MOSFET, IGBT has an extra layer of P+ substrate, which is the P+ collector region shown in Figure 1. Therefore, when IGBT flows through the current, both minority carriers and majority carriers participate in it. Due to the conductance modulation effect, the IGBT on-state voltage drop is much lower than that of the MOSFET with the same structure.

3. Analysis of the turn-on process

3.1. Analysis of gate voltage

First, to analyze the gate voltage of IGBT turn-on process, it is necessary to understand the composition of gate capacitance. For IGBT devices, the gate capacitance consists of four parts as shown in Figure 2. (a) gate-emitter metal capacitance $C_1$. (b) gate-N+ source oxide capacitance $C_2$. (c) gate-P base capacitance $C_{gp}$, which is composed of $C_3$ and $C_5$. (d) gate-collector capacitance $C_{gc}$, which is composed of $C_4$ and $C_6$. The gate-emitter capacitance (also called input capacitance) is $C_{ge}=C_1+C_2+C_{gp}$, and the gate-collector capacitance (also called reverse transmission capacitance or miller capacitance) is $C_{gc}$. In addition, $C_{gp}$ varies with the change of gate voltage, and $C_{gc}$ varies with the change of collector voltage.
As the voltage increases, the depletion region is gradually formed. In the depletion, the gate oxide capacitance is in series with the depletion layer capacitance. At this time, the unit area capacitance of the gate-P base region is

$$C_{gp} = \frac{C_3C_5}{C_3+C_5} = \frac{\varepsilon_{ox}}{t_{ox} + (\frac{\varepsilon_{ox}}{\varepsilon_s})x_d}$$  \hspace{1cm} (2)$$

The gate voltage continues to increase, and when the gate voltage is greater than the threshold voltage, the depletion width reaches its maximum and the inversion layer is gradually formed. Since the switching speed of IGBT is relatively slow, the inversion layer charge can keep up with the change of capacitor voltage. At this time, the unit area capacitance of the gate-P base region is

$$C_{gp} = C_3 = \frac{\varepsilon_{ox}}{t_{ox}}$$  \hspace{1cm} (3)$$

Where, $\varepsilon_{ox}$ is the dielectric constant of the gate oxide layer, $t_{ox}$ is the thickness of the gate oxide layer, $\varepsilon_s$ is the silicon dielectric constant, $x_d$ is the depletion region width.

According to the above analysis, the capacitance value of $C_{gp}$ decreases first with the increase of gate voltage, and then gradually increases and reaches a stable value with the further increase of gate voltage.

The different stages of gate voltage is analyzed in detail below. The process of gate voltage rising from zero to the threshold voltage is called the turn-on delay stage. The charging process in the turn-on delay stage is only for capacitors $C_1$, $C_2$ and $C_{gp}$. Therefore, in combination with the above analysis, the drive circuit is not charged to the constant capacitor during the turn-on delay stage. Figure 3 shows the rise process of gate voltage with variable capacitance, in which the solid line is the voltage curve for a constant capacitance, and the dashed line is the voltage curve considering the change of input capacitance.

![Figure 3 Gate voltage rising curve during opening delay](image)

When gate voltage rises to a certain value, there will be a stage in which gate voltage is maintained at a level, which is called the Miller plateau voltage. When gate voltage is greater than the threshold voltage, IGBT begins to flow through the forward current. When the collector current reaches the maximum current, the freewheeling diode is reverse biased, then $V_{ce}$ decreases rapidly. In this process, the drive circuit keeps charging the capacitance $C_{gc}$. Since $V_{ce}$ is decreasing, the gate voltage $V_g$ does not rise, which is also the direct cause of the formation of the Miller plateau.

After the Miller plateau stage, the drive circuit continues to charge both $C_{ps}$ and $C_{gc}$, and gate voltage begins to rise again. At this stage, gate voltage rises faster than the turn-on delay stage.

3.2. Analysis of collector current
Before gate voltage is lower than the threshold voltage, IGBT is in the turn-off state. Once gate voltage exceeds the threshold voltage, electrons in the N’ source region flow to the N’ base region through the MOS channel, and collector current begins to rise. At this time, collector current flowing through IGBT can be expressed as
$$I_C = K_n (V_{gs} - V_T)^2$$

(4)

Since the collector current rises extremely fast, gate voltage can be approximated as a linear increase in the short time. Therefore, IGBT collector current curve can be considered as a quadratic function curve before it reaches the load current,

$$I_C = at^2$$

(5)

Where, $a$ is determined by the chip parameters, power loop parameters, and drive loop parameters.

### 3.3. Analysis of collector-emitter voltage

Under ideal conditions, regardless of stray inductance and resistance, when the current of the freewheeling diode reaches the maximum reverse current, the diode begins to withstand the reverse voltage, and the voltage across the IGBT drops sharply. The IGBT collector-emitter voltage drop consists of two phases. The first phase is similar to the MOSFET turn-on mechanism. The depletion region quickly disappears and the voltage drops sharply, as shown in the $U_{CE,MOSFET}$ phase in Figure 4. The second phase is the process of excess carrier diffusion in the base region, conductance modulation region expansion, and neutral base region voltage drop reduction, as shown in $U_{CE,BJT}$ phase in Figure 4. Since the rate of carrier diffusion is much slower than the rate of depletion region disappears, the voltage attenuation at second phase is very slow.

$$I_{peak} V_{dc} I_{load} U_{CE,MOSFET} i_c U_{CE_BJT} V_{dc} L_s V_g$$

**Figure 4 Ideal turn-on voltage waveforms**  **Figure 5 Test circuit under inductive load condition**

The inductive load double-pulse test circuit is shown in Figure 5. The load inductance is large enough. Under ideal conditions, when the freewheeling diode is subjected to reverse voltage, the IGBT collector-emitter voltage begins to drop.

However, there is a certain stray inductance in the main circuit under actual working conditions. Therefore, in the process of collector current rising, the on-state voltage drop of the freewheeling diode can be neglected, so that the voltage equation of the power loop can be obtained as follows:

$$V_{ce} + L_s \frac{di_c}{dt} = V_{dc}$$

(6)

Where, $V_{ce}$ is collector-emitter voltage of IGBT device, $L_s$ is the main circuit stray inductance, $i_c$ is collector current, $V_{dc}$ is the DC bus voltage. Therefore, $V_{ce}$ is lower than the DC bus voltage from the moment the current rises. Combined with formula (5),

$$V_{ce} = V_{dc} - L_s \frac{di_c}{dt} = V_{dc} - 2aL_st$$

(7)

It can be seen from the above equation that, during the process of collector current rising, collector-emitter voltage drops approximately linearly. The larger the stray inductance is, the faster collector-emitter voltage falls.

### 4. Experimental verification

#### 4.1. The experiment platform
In order to verify the correctness of the analysis in this paper, based on the circuit principle shown in Figure 5, a testing platform for the dynamic parameters of Press Pack IGBT as shown in Figure 6 is built. The tested IGBT is T0600TB45A (4.5 kV/600 A) from WESTCODE, and the pressure applied to IGBT is 10kN. The freewheeling diode uses IGBT module DIM800NSM33-A00 from DYNEX. The experimental temperature is room temperature. Then, an oscilloscope TekTronix DPO4104B is used to record the voltage and current waveforms in the experiment, with the bandwidth of 1GHz and the sampling rate of 5 GS/s.

4.2. Test result and analysis

The turn-on waveform of IGBT is shown in Figure 7, which can be divided into five stages. Where, \( V_{G(off)} \) is the negative gate voltage of turn-off state, \( V_{G(on)} \) is the positive gate voltage of turn-on state, and \( V_{G(th)} \) is the IGBT turn-on threshold voltage. \( V_{DC} \) is the DC bus voltage, \( I_L \) is the load current, \( I_{RR} \) is the diode reverse recovery maximum current. \( V_{GE} \) is gate voltage, \( I_C \) is collector current, and \( V_{CE} \) is collector-emitter voltage of IGBT.

- Open delay phase. During this phase, the drive loop charges the input capacitor and gate voltage is gradually increased. It should be noted that gate voltage in the dotted circle in Figure 9 has a slop increasing process, which corresponds to the change of input capacitance during the rising of gate voltage.
- Current rise phase. During this phase, the MOSFET channel conducts and collector current of IGBT begins to rise rapidly. When \( I_C \) is less than the load current, \( I_C \) can be fitted with a quadratic function. At this time, collector-emitter voltage decreases linearly with the increase of collector current.
- Collector-emitter voltage drops rapidly phase. When collector current \( I_C \) is greater than the peak current, the freewheeling diode is subjected to the reverse voltage, and collector-emitter voltage of IGBT decreases rapidly.
- Gate voltage platform phase. The gate voltage at this phase is maintained at the Miller plateau. Due to the expansion of the conductance modulation region in IGBT, collector-emitter voltage \( V_{CE} \) continues to decrease.
- Gate voltage continuing rise phase. The drive circuit continues to charge the gate capacitance, the IGBT collector-emitter voltage basically reaches the steady on-state voltage drop, and collector current is equal to the load current.

5. Conclusion

In this paper, the relationship between gate voltage, collector current and collector-emitter voltage during IGBT turn-on is analyzed based on the physical mechanism of IGBT, and the following conclusions are obtained:

a) Before gate voltage reaches the threshold voltage, with the increase of gate voltage, the gate-emitter capacitance \( C_{ge} \) decreases first and then increases.
b) Collector current during the turn-on process can be fitted by quadratic function.

c) The larger the stray inductance of the main circuit, the faster the initial drop speed of collector-emitter voltage during collector current rising process, and the smaller the turn-on loss of IGBT.

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