Combined Implications of UV/O3 Interface Modulation with HfSiOx Surface Passivation on AlGaN/AlN/GaN MOS-HEMT

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Abstract: Surface passivation is critically important to improve the current collapse and the overall device performance in metal-oxide semiconductor high-electron mobility transistors (MOS-HEMTs) and, thus, their reliability. In this paper, we demonstrate the surface passivation effects in AlGaN/AlN/GaN-based MOS-HEMTs using ultraviolet-ozone (UV/O3) plasma treatment prior to SiO2-gate dielectric deposition. X-ray photoelectron spectroscopy (XPS) was used to verify the improved passivation of the GaN surface. The threshold voltage (VT) of the MOS-HEMT was shifted towards positive due to the band bending at the SiO2/GaN interface by UV/O3 surface treatment. In addition, the device performance, especially the current collapse, hysteresis, and 1/f characteristics, was further significantly improved with an additional 15 nm thick hafnium silicate (HfSiOx) passivation layer after the gate metallization. Due to combined effects of the UV/O3 plasma treatment and HfSiOx surface passivation, the magnitude of the interface trap density was effectively reduced, which further improved the current collapse significantly in SiO2-MOS-HEMT to 0.6% from 10%. The UV/O3-surface-modified, HfSiOx-passivated MOS-HEMT exhibited a decent performance, with IDMAX of 655 mA/mm, GMMAX of 116 mS/mm, higher ION/IOFF ratio of approximately 107, and subthreshold swing of 85 mV/dec with significantly reduced gate leakage current (IGC) of 9.1 × 10−10 mA/mm.

Keywords: AlGaN/AlN/GaN; gallium oxide; MOS-HEMT; HfSiOx; UV/O3; passivation; interface trap density; flicker noise

1. Introduction

In recent years, substantial research has been focused on AlGaN/GaN-based high electron mobility transistors (HEMTs) for high-power and radio-frequency applications due to the remarkable properties of III-nitrides such as high saturation velocity (~2 × 107 cm/s), wide band gap (~3.4 eV), high carrier density (~1013/cm2), and large breakdown electric field (~3 MV/cm) [1–3]. In particular, high-density and high-mobility two-dimensional electron gas (2DEG) generated at the AlGaN/GaN interface allows us to understand how power-switching transistors having low ON-resistance are applicable to next-generation power conversion systems [4]. However, observations confirm that the AlGaN/GaN HEMTs suffer from severe current collapse due to the presence of multiple surface states at source/drain (S/D) access region [5]. Various methods were introduced to improve the surface and interface states, such as wet cleaning [6], dry etching [6], interface passivation layers [7,8], and surface plasma treatment [9–11].

Among these methods, ultraviolet/ozone (UV/O3) surface plasma treatment is important due to its ability to screen the effects of polarization bound charges of GaN and to produce the Ga-O surface dielectric layer on GaN [12]. Eller et al. and Choi et al. reported that Gallium oxide (Ga-O) layer is useful as a surface dielectric layer in GaN-based electronic devices [6,13]. Notably, this method is much easier and simpler to apply than what was previously reported [14]. To date, UV/O3 is mainly used for cleaning. There are very
few available reports that are focused on the improvement of the interface quality of the GaN devices by the application of UV/O\textsubscript{3} surface plasma treatment [12,15,16]. Furthermore, previous reports have suggested that the current collapse phenomenon can be effectively mitigated by the reduction of surface states using the different surface passivation dielectrics [17]. Numerous dielectric materials have been used as a passivation layer along with various deposition technologies to improve the device performance, such as SiO\textsubscript{2}, SiN\textsubscript{x}, SiON, AlN, and HfO\textsubscript{2} [17–20]. However, previous investigation has revealed that each material has its own limitations, e.g., higher gate leakage currents or high interface state density have been observed after SiO\textsubscript{2}, SiN\textsubscript{x}, or HfO\textsubscript{2} passivation [17,21]. Recent studies have explored how the interface state density could be reduced effectively by the incorporation of Si into Al\textsubscript{2}O\textsubscript{3}, which subsequently improves the device performance [22]. In order to improve the dielectric properties of HfO\textsubscript{2}, the inclusion of Si into HfO\textsubscript{2} has been investigated. Due to the unique properties of hafnium silicate (HfSiO\textsubscript{x}), i.e., high dielectric constant (~16.8) [23], with comparatively large band-gap (~6 eV) [24] and lower interface trap density than HfO\textsubscript{2}, some research groups have previously used HfSiO\textsubscript{x} as gate dielectric [19]. To date, direct observation of the improvement of performance in SiO\textsubscript{2} metal oxide semiconductor high electron mobility transistor (MOS-HEMT), using the combined effects of UV/O\textsubscript{3} surface modification with HfSiO\textsubscript{x} passivation, has not yet been investigated.

With this aim in mind, in this work, the interface of the SiO\textsubscript{2} MOS-HEMTs was improved through UV/O\textsubscript{3} surface plasma treatment prior to gate oxide deposition. Dramatic reduction of the current collapse in the MOS-HEMT due to deposition of HfSiO\textsubscript{x} passivation layer after gate metallization was also examined. The UV/O\textsubscript{3} treatment might have screened the internal/external polarization charge and altered the band bending at the atomic layer deposition (ALD) SiO\textsubscript{2}/GaN interface through modifying the charged surface states, which resulted in positive shifting of the $V_{\text{TH}}$ in MOS-HEMT compared to conventional HEMT (C-HEMT). The threshold voltage of $-3 \text{ V}$, $I_{\text{D MAX}}$ of 655 mA/mm, subthreshold slope of 85 mV/dec, and $I_{\text{G}}$ of $9.1 \times 10^{-10}$ A/mm with a significant improvement of current degradation of 0.6% were achieved for UV/O\textsubscript{3} plasma modified SiO\textsubscript{2}-MOS-HEMT after HfSiO\textsubscript{x} surface passivation.

2. Materials and Methods

The AlGaN/AlN/GaN heterostructure was grown on a 6-inch p-type low-resistive Si substrate using metal organic-chemical vapour deposition (MOCVD) system. The heterostructure consisted of 5.5 μm GaN buffer layer, a 200 nm undoped GaN layer, 1 nm AlN, and a 25 nm Al\textsubscript{0.23}Ga\textsubscript{0.77}N as barrier layer, and a 2 nm GaN cap layer. The room temperature sheet carrier-density ($n_{\text{sh}}$) and mobility ($\mu$) were extracted from Hall measurements, which were approximately $8 \times 10^{12} \text{ cm}^2/\text{V s}$ and 1700 cm$^2$/V s, respectively.

Device processing began with mesa isolation using an inductive coupled plasma reactive ion etching (ICP-RIE) system under Cl\textsubscript{2}/BCl\textsubscript{3} environment. After that, source and drain regions were defined with UV photolithography and Ti/Al/Ni/Au (25/150/30/120 nm) metal stacks were deposited by using electron-beam (e-beam) evaporator. Then, the rapid thermal annealing (RTA) was done at 875 °C for 30 s under N\textsubscript{2} ambient to ensure good ohmic contact. The sheet resistance was found to be approximately 400 $\Omega/\square$. After that, the UV-ozone surface plasma treatment was done with 7 mg/L-O\textsubscript{3} dose and active wavelengths of 185 nm and 254 nm for 4 min, prior to gate oxide deposition. Then, 5 nm SiO\textsubscript{2} layer was deposited as gate dielectric using atomic layer deposition (ALD) system at 250 °C. Then, the gate region was defined by UV photolithography and Ni/Au (80/100 nm) metal stack was deposited by e-gun evaporator. Furthermore, to improve the device performance, a 15 nm thick HfSiO\textsubscript{x} passivation layer was deposited by ALD. As for the 15 nm HfSiO\textsubscript{x} deposition, one cycle reaction of bis-(diethylamino) silane (SAM-24) with ozone was inserted into HfO\textsubscript{2} after 4 cycles of HfO\textsubscript{2} to form ~1 nm HfSiO\textsubscript{x}. As a reference, to understand the effects of surface modification and passivation layer separately, C-HEMTs were fabricated with three different conditions, i.e., (i) without UV/O\textsubscript{3} treatment
and HfSiO$_X$ passivation, (ii) with UV/O$_3$ treatment and without HfSiO$_X$ passivation, and (iii) with UV/O$_3$ and HfSiO$_X$ passivation. In addition, to determine the HfSiO$_X$ passivation effects on MOS-HEMT, devices were fabricated (iv) with and (v) without HfSiO$_X$ passivation. The UV lithography and DC measurements were performed with the MJB3 Karl Suss Mask Aligner and B1500A Semiconductor Characterization system. Figure 1a shows the schematic diagram of UV/O$_3$ surface-modified HfSiO$_X$ passivated MOS-HEMT. All devices were made with the same gate length ($L_G = 2 \mu m$) and $L_{GD}/L_{SG}$ (2/2 $\mu m$) distances.

![Figure 1](image)

**Figure 1.** (a) Schematic illustration and (b) TEM image of ultraviolet-ozone (UV/O$_3$)-treated HfSiO$_X$ passivated metal-oxide semiconductor high-electron mobility transistors (MOS-HEMT). (c) EDX line scan of HfSiO$_X$. AFM image of MOS-HEMT (d) without UV/O$_3$, (e) with UV/O$_3$ treatment before passivation, and (f) with UV/O$_3$ treatment after passivation.

### 3. Results and Discussion

Figure 1b shows the transmission electron microscopy (TEM) image of the UV/O$_3$ surface-treated HfSiO$_X$-passivated MOS-HEMT. From TEM image, it can be understood that, due to the UV/O$_3$ surface treatment prior to gate dielectric deposition, a thin layer of GaO$_X$N$_Y$ was formed [25]. The energy dispersive X-ray (EDX) line scan of HfSiO$_X$ was shown in Figure 1c. Figure 1d,e shows the atomic force microscopy (AFM) images of the unpassivated sample with and without UV/O$_3$ plasma treatment, while the AFM image of the UV/O$_3$ modified HfSiO$_X$ passivated sample is shown in Figure 1f. The combined effects of UV/O$_3$ surface treatment and the deposition of HfSiO$_X$ passivation layer decreased the surface roughness significantly, which subsequently improved the device performance.

To analyse the improvement of device performance, X-ray photoelectron spectroscopy (XPS) was performed using K-Alpha X-ray photoelectron spectrometer to examine the change in the surface chemistry of the SiO$_2$/GaN interface after UV/O$_3$ plasma treatment. Figure 2a,b exhibit the change in atomic composition of GaN 3d core levels without and with UV/O$_3$ surface treatment, respectively. It can be seen that both spectra were de-convoluted into Ga-N and Ga-O peaks. The Ga-N peak de-convoluted at 19.7 eV and Ga-O peak appeared at 20.8 eV, considering spin orbital splitting [15]. The peak intensity ratio of Ga-O/Ga-N was improved to 75% from 38% after UV/O$_3$ plasma treatment, indicating an improved passivation. Since the standard Gibbs free energy of the Ga-O bond is negatively larger ($-285$ kJ/mol) than Ga-N bond ($-157$ kJ/mol), the Ga atoms in the Ga-O bond could come from the Ga-N bond [15].
The typical drain current-voltage characteristics of the UV/O\textsubscript{3} surface-treated MOS-HEMT and C-HEMT before and after HfSiO\textsubscript{X} passivation is shown in Figure 3. The maximum drain currents (I\textsubscript{DMAX}) (@ V\textsubscript{C} = 4 V) before/after passivation were found to be 655/620 mA/mm for MOS-HEMT and 542/504 mA/mm (@ V\textsubscript{C} = 1 V) for C-HEMT, respectively. Owing to the large gate leakage current, C-HEMT could not be biased with high V\textsubscript{G}. Henceforth, the reduction of I\textsubscript{DMAX} in C-HEMT was due to the large gate leakage current [26]. The improvement of the I\textsubscript{DMAX} after passivation was attributed to the increase in sheet electron concentration [27] and surface-controlled effect [28]. After passivation, the SiO\textsubscript{2} MOS-HEMT showed good pinch-off characteristics. In comparison, I\textsubscript{DMAX} was found approximately to be 415 mA/mm for C-HEMT without surface treatment and passivation. Henceforth, the reduction of I\textsubscript{DMAX} in C-HEMT was due to the large gate leakage current.

Comparison of drain current-voltage (I\textsubscript{D}-V\textsubscript{D}) characteristics of (a) conventional HEMT (C-HEMT) (before and after UV/O\textsubscript{3} treatment) and (b) MOS-HEMT with and without HfSiO\textsubscript{X} passivation.

To understand the gate controllability of UV/O\textsubscript{3} surface-modified MOS-HEMT and C-HEMT, the transfer characteristics were calibrated before and after passivation at V\textsubscript{D} = 4 V, as shown in Figure 4. The threshold voltage (V\textsubscript{TH}) is defined as the gate bias intercept point of the linear extrapolation of I\textsubscript{D} at peak transconductance (G\textsubscript{MMAX}) [29]. V\textsubscript{TH} of the MOS-HEMT after and before passivation were found to be −3.0 V and −2.65 V, respectively. For C-HEMT, V\textsubscript{TH} was found to be approximately −3.05 V before passivation, which is hardly a change after HfSiO\textsubscript{X} passivation. In previous literature, the negative shifting of V\textsubscript{TH} in MOS-HEMT compared to planar HEMT was observed due to the larger separation between the gate and the channel [30]. The threshold voltage can be expressed as [31]

\[
V_{th} = \phi_B - \Delta E_C - \phi_F - \frac{t_{ox}}{\varepsilon_b} (P_1 + P_2 + P_3 + qn_{GaN}/SiO_2) - \frac{t_{ox}}{\varepsilon_{ox}} (P_2 + P_3)
\]

(1)

where \( \phi_B \) is the metal barrier height; \( \phi_F \) is the energy difference \( E_C - E_F \) (\( E_F \) is the Fermi energy) in the GaN bulk; \( \Delta E_C \) is the conduction band offset between SiO\textsubscript{2} and GaN; \( t_b \) is the barrier thickness; \( t_{ox} \) is the SiO\textsubscript{2} thickness; \( \varepsilon_b \) is the permittivity of the barrier layer; \( \varepsilon_{ox} \)
is the permittivity of the SiO$_2$; $n_0$ is the oxide charge; $n_{GaN/SiO2}$ is the interface charge density at the SiO$_2$/GaN interface; and $P_1$, $P_2$, and $P_3$ are the total polarization sheet charges (sum of the spontaneous and piezoelectric polarization) at the GaN-cap surface, GaN-cap/AlGaN interface, and AlGaN/GaN buffer interface, respectively. The UV/O$_3$ treatment could screen internal/external polarization bound charges and form thin Ga$_2$O$_X$ layer on the GaN surface that could shift the $V_{TH}$ towards positive [16]. Another reason for the positive shifting of threshold voltage in the MOS-HEMT might be the band bending at the SiO$_2$/GaN interface, which changed the $\Delta E_C$ causing the UV-O$_3$ treatment [11]. After HfSiO$_X$ passivation, the sheet carrier concentration was increased in the channel, which effectively shifted the $V_{TH}$ in the negative direction [32].

\[ G_{\text{MMAX}} = \frac{n_G n_D}{\varepsilon_0 W d / \varepsilon_{\text{SiO2}}} \]

\[ V_{TH} = \frac{P_1 P_2 P_3}{n_G n_D n_{GaN/SiO2} W d / \varepsilon_{\text{SiO2}}} \]

\[ G_{\text{MMAX}} = \frac{n_G n_D}{\varepsilon_0 W d / \varepsilon_{\text{SiO2}}} \]

\[ V_{TH} = \frac{P_1 P_2 P_3}{n_G n_D n_{GaN/SiO2} W d / \varepsilon_{\text{SiO2}}} \]

\[ SS = \left( \frac{\partial \log I_{DS}}{\partial V_{GS}} \right)^{-1} \]

Figure 4. Comparison of transfer characteristics ($I_D$-$V_G$) (@ $V_D = 4$ V) of (a) C-HEMT (before and after UV/O$_3$ treatment) and (b) MOS-HEMT with and without HfSiO$_X$ passivation.

$G_{\text{MMAX}}$ was increased to 116 mS/mm after passivation from 90 mS/mm for MOS-HEMT, while for UV/O$_3$-treated C-HEMT, the $G_{\text{MMAX}}$ was increased to 138 mS/mm (129 mS/mm) after passivation (before passivation) treatment. To understand the linear behaviour of the devices, the gate voltage swing (GVS) was calculated for two devices. The GVS, defined as 10% drop from the $G_{\text{MMAX}}$, was increased to 2.53 V (1.55 V) from 1.60 V (1.15 V) for MOS-HEMT (C-HEMT) after passivation [30]. The largest GVS after passivation suggests a better linear behaviour for the UV/O$_3$ surface-treated MOS-HEMT compared with the C-HEMT, from which a smaller intermodular distortion, a smaller phase noise, and a larger dynamic range could be expected, thus making it desirable for practical amplifier applications [30]. The $G_{\text{MMAX}}$ and GVS were found to be 104 mS/mm and 0.87 V, respectively, for C-HEMT without UV/O$_3$ treatment as well as HfSiO$_X$ passivation.

Figure 5a shows the subthreshold characteristics as a function of gate voltage (@ $V_D = 4$ V) for UV/O$_3$ surface-treated MOS-HEMT and C-HEMT after passivation. It is clearly found that the subthreshold drain leakage current was decreased more than two orders of magnitude in UV/O$_3$ surface modified HfSiO$_X$ passivated MOS-HEMT than C-HEMT. The interface oxide (Ga$_{2}$O$_{X}$N$_{Y}$) on the GaN, formed by the UV/O$_3$ surface treatment, reduced the defect states at the metal–semiconductor interfaces resulting in the reduction of subthreshold drain leakage current and the reverse-biased gate leakage current in MOS-HEMT as shown in Figure 5a [15]. The subthreshold drain leakage current is dominated by the reverse-biased drain leakage current in the pinch-off region [33]. Since the reverse bias gate leakage current was suppressed in MOS-HEMT, the subthreshold drain leakage was decreased due to the improvement of the metal barrier height, as discussed later [34]. The subthreshold swing (SS) was also highly dependent on the reversed-bias gate leakage current [33]. The SS is defined as [35]
HEMT (before and after UV/O3 treatment) and MOS-HEMT with HfSiOX passivation. (a) Subthreshold characteristics of (@ VD = 6V) C-HEMT (before and after UV/O3 treatment) and MOS-HEMT with and without HfSiOX passivation. Figure 5.

Figure 5. Comparison of (a) subthreshold (@ VD = 4 V) and gate leakage (IG-VG) characteristics of C-HEMT (before and after UV/O3 treatment) and MOS-HEMT with HfSiOX passivation. (b) Hysteresis characteristics of (@ VD = 6 V) C-HEMT (before and after UV/O3 treatment) and MOS-HEMT with and without HfSiOX passivation.

To understand the gate controllability, the SS values of the MOS-HEMT and C-HEMT were calculated from Figure 5a. Plasma-treated MOS-HEMT after passivation exhibited much lower SS of 85 mV/dec than for C-HEMT (125 mV/dec). The ON/OFF ratio (ION/IOFF) for MOS-HEMT was found to be approximately 3.1 × 10^6, while for C-HEMT it was found to be 1.6 × 10^6. The SS and ION/IOFF were found to be 160 mV/dec and 4.8 × 10^5 for C-HEMT without UV/O3 treatment and HfSiOX passivation.

The reverse and forward gate leakage I-V characteristics of the surface-treated SiO2 MOS-HEMT and C-HEMT after passivation are shown in Figure 5a. It was clearly revealed that the reverse gate leakage current (IG) (@ VG = −15 V) of MOS-HEMT was 9.1 × 10^-10 A/mm, which was nearly two orders of magnitude less than C-HEMT (4.3 × 10^-8 A/mm). As expected, due to the increment of effective barrier height, causing the insertion of large band gap (~9 eV) ALD SiO2 as gate dielectric, the gate leakage current was reduced in MOS-HEMT compared to C-HEMT. The band alignment of Ni/SiO2/GaN Schottky interface with Ga-O interlayer due to UV/O3 surface treatment might be another reason for the noticeable reduction of IG [15].

The ideality factor (η) can be extracted by employing the standard thermionic equation as [36]

\[ \eta = \frac{q}{kT} \left( \frac{dV}{d(\ln I)} \right) \]

where T is the temperature, q is the electron charge, k is the Boltzmann constant, and V is the applied voltage.

The ideality factors of 2.5 and 3.2 were calculated for MOS-HEMT and C-HEMT, respectively. The UV/O3 surface plasma treatment prior to gate dielectric deposition reduced the interface state densities, which effectively improved the ideality factor of the MOS-HEMT. Furthermore, a higher turn on voltage (VT) was observed in C-HEMT with UV/O3 surface treatment and MOS-HEMT, as shown in the inset of Figure 5a. The shift of VT was associated with the formation of Ga-O interface oxide layer by UV/O3 surface treatment in C-HEMT [15].

Figure 5b shows the hysteresis characteristics for MOS-HEMT and C-HEMT before and after HfSiOX passivation (@ VD = 6 V). The MOS-HEMT exhibited less hysteresis than C-HEMT after HfSiOX passivation. The combined effects of UV/O3 surface treatment and HfSiOX passivation resulted in the significant reduction of hysteresis in SiO2-MOS-HEMT. Compared to C-HEMT, the MOS-HEMT exhibited almost low hysteresis of 0.11 V after passivation due to the effective neutralization of the surface caused by the Ga-O interface oxide passivation [15] and HfSiOX passivation layer [35]. Due to the presence of acceptor-like surface states on the device, counter-clockwise hysteresis was found [35].

To investigate the effectiveness of the HfSiOX surface passivation and UV/O3 surface treatment in the MOS-HEMT compared to C-HEMT, the gate lag measurements were employed. Figure 6a–d show the drain current response of the UV/O3-treated MOS-HEMT and C-HEMT before and after HfSiOX passivation. The pulse width and pulse period are
set to 500 µs and 50 ms, respectively. From observation, it was clearly revealed that with HfSiO\textsubscript{X} passivation the current collapse was improved significantly in MOS-HEMT over C-HEMT. The drain-source current collapse was significantly improved to 0.6% (7%) in MOS-HEMT (C-HEMT) after HfSiO\textsubscript{X} passivation, while before passivation it was found to be approximately 10% (13%) (@ V\textsubscript{D} = 8 V, V\textsubscript{G} = 0 V). Most of the surface traps presented in the S/D access regions might have been passivated by UV/O\textsubscript{3} surface modification and HfSiO\textsubscript{X} passivation, resulting in significant improvement in the current collapse. Without surface treatment and passivation, the current collapse was found in C-HEMT to be approximately 20% (not shown here). The formation of the thin Ga-O interface layer between gate metal and GaN cap, which serves as the passivation layer, resulted in the reduction of current collapse to 13% from 20% in C-HEMT [15,37].

Figure 6. Comparison of pulsed I\textsubscript{D}-V\textsubscript{D} characteristics of UV/O\textsubscript{3}-treated C-HEMT (a) after and (b) before HfSiO\textsubscript{X} passivation and MOS-HEMT (c) after and (d) before HfSiO\textsubscript{X} passivation.

In order to understand the reduction of trap states after the UV/O\textsubscript{3} surface treatment and HfSiO\textsubscript{X} passivation of the devices, capacitance-voltage (C-V) measurements of C-HEMT and MOS-HEMT were measured at 1 MHz, shown in Figure 7a,b. The interface state density (D\textsubscript{it}) for surface-treated MOS-HEMT can be extracted from the previously reported formula [38] to be 1.9 \times 10^{12} \text{eV}^{-1}\cdot\text{cm}^{-2} (4.1 \times 10^{12} \text{eV}^{-1}\cdot\text{cm}^{-2}) with HfSiO\textsubscript{X} passivation (without passivation). To realize the surface passivation effects on the reduction of interface state density, D\textsubscript{it} for C-HEMT were also estimated to be 9.7 \times 10^{12} \text{eV}^{-1}\cdot\text{cm}^{-2} (1.4 \times 10^{13} \text{eV}^{-1}\cdot\text{cm}^{-2}) after (before) HfSiO\textsubscript{X} surface passivation. A similar trend was found in the previous report [39]. Due to the combined effects of UV/O\textsubscript{3} surface treatment and HfSiO\textsubscript{X} passivation, the interface trap density was reduced approximately one order of magnitude in MOS-HEMT compared to C-HEMT.

Low-frequency noise, or 1/f measurement, is an effective method for studying electron-trapping and -de-trapping behaviour. Figure 7c shows the low-frequency characteristics, measured at V\textsubscript{DS} = 4 V, V\textsubscript{GS} = -1 V, and f = 10\textasciitilde10\textsuperscript{5} Hz, for MOS-HEMT before and after passivation, and C-HEMT. In 1/f-noise characteristics, the variation of noise current spectral density S\textsubscript{D} (A\textsuperscript{2}/Hz) with frequency was measured. This is directly related to the presence of electron traps and/or de-trapping between the 2 DEG channel and traps in the GaN buffer layer [34]. It was found that S\textsubscript{D} of the MOS-HEMT was one order lower after passivation than before passivation, as expected from the improved surface quality [34]. Table 1 shows the comparison of MOS-HEMT and C-HEMT before and after UV/O\textsubscript{3} modification and HfSiO\textsubscript{X} passivation.
C-HEMT and C-HEMT without any treatment. (c) Flicker noise characteristics of MOS-HEMT with and without HfSiO\textsubscript{X} passivation, and C-HEMT without any treatment.

| Parameters | C-HEMT | C-HEMT with UV/O\textsubscript{3} | C-HEMT with UV/O\textsubscript{3} and HfSiO\textsubscript{X} | MOS-HEMT with UV/O\textsubscript{3} | MOS-HEMT with UV/O\textsubscript{3} and HfSiO\textsubscript{X} |
|------------|--------|-----------------|-----------------|-------------------|-------------------|
| $I_{\text{DMAX}}$ (mA/mm) | 415    | 504             | 542             | 620               | 655               |
| $V_{\text{TH}}$ (V) | −3.1   | −3.05           | −3.05           | −2.65             | −3.0              |
| $G_{\text{MAX}}$ (mS/mm) | 104    | 129             | 138             | 90               | 116               |
| $SS$ (mV/dec) | 160    | 140             | 125             | 95               | 85                |
| $I_{\text{ON}}/I_{\text{OFF}}$ | $4.8 \times 10^{-5}$ | —               | $1.6 \times 10^{6}$ | —               | $3.1 \times 10^{7}$ |
| $I_{\text{G}}$ (A/mm) (@ $V_G = -15$ V) | $6.6 \times 10^{-8}$ | —               | $4.3 \times 10^{-8}$ | —               | $9.1 \times 10^{-10}$ |
| Current collapse (%) | 20     | 13              | 7               | 10               | 0.6               |
| $D_{\text{IT}}$ (eV\textsuperscript{-1}.cm\textsuperscript{-2}) | $2.1 \times 10^{13}$ | $1.4 \times 10^{13}$ | $9.7 \times 10^{12}$ | $4.1 \times 10^{12}$ | $1.9 \times 10^{12}$ |
| Hysteresis ($\Delta V$) (V) | 1.04   | 2.12            | 0.804           | 1.95             | 0.11              |
| GVS (V) | 0.87   | 1.15            | 1.55            | 1.60             | 2.53              |

4. Conclusions

In summary, we have demonstrated the combined effects of UV/O\textsubscript{3} plasma treatment and the surface passivation using ALD-grown HfSiO\textsubscript{X} on the DC performance of SiO\textsubscript{2}-MOS-HEMTs. A high-quality HfSiO\textsubscript{X} passivation layer significantly reduced the current degradation from 10% to 0.6% in MOS-HEMT compared to C-HEMT by decreasing the trapping phenomenon originating from the surface states. A significant enhancement of electrical characteristics in MOS-HEMT was observed after the combined treatment, compared to C-HEMT. The MOS-HEMT with surface plasma treatment after passivation exhibited $I_{\text{DMAX}}$ of 655 mA/mm, $G_{\text{MAX}}$ of 116 mS/mm, on-off ratio of $3.1 \times 10^{7}$ with subthreshold slope of 85 mV/dec, and $V_{\text{TH}}$ of −3 V. The combined effects of band bending at the SiO\textsubscript{2}/GaN interface and screening of internal/external-polarization-bound charges by the UV/O\textsubscript{3} surface treatment shifted the $V_{\text{TH}}$ in a positive direction in MOS-HEMT, compared to C-HEMT. The reversed gate leakage current of approximately $9.1 \times 10^{-10}$ A/mm was achieved. Furthermore, the aforementioned combined treatment decreased the interface trap states from $4.1 \times 10^{12}$ eV\textsuperscript{-1}.cm\textsuperscript{-2} to $1.9 \times 10^{12}$ eV\textsuperscript{-1}.cm\textsuperscript{-2} in UV/O\textsubscript{3}-treated MOS-HEMT after HfSiO\textsubscript{X} passivation, which resulted in the reduction of hysteresis and 1/f-noise characteristics, compared to C-HEMT. The experimental results are significant for the development of high-performance GaN-based MOS-HEMT.
Author Contributions: S.M. is responsible for the device preparation and characterization, data analysis, and paper writing. All authors analyzed the data and revised the manuscript. Y.-H.W. is the advisor to monitor the progress and paper editing. All authors have read and agreed to the published version of the manuscript.

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