Modular Multiplication without Carry Propagation

Algorithm Description

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Abstract—This paper describes a sufficiently simple modular multiplication algorithm, which uses only carry-save addition with bit inspection Boolean logic and without number comparison or carry propagation.

NOTE AND OPERATIONS

In this paper the following notation is used. Numbers represented as big letters, e.g. $A, B$. Their corresponding bits of binary expansion represented by small indexed letters, e.g. $a_0, b_i$. Index 0 specifies the least significant bit. Letters $n$ and $k$ are sizes of the numbers in bits. Bars $| \cdot |$ denote bit-length; so $|A| = n$ means that $A$ has exactly $n$ bits. Operation $\lfloor \cdot \rfloor_R$ is modular reduction by $R$ such that $A \equiv |A|_R \mod R$ and $|A|_R < R$. Operation $\lfloor \cdot \rfloor$ is floor function. Operations $(+,-)$ are arithmetic addition and subtraction. Arithmetic multiplication is implied between numbers, e.g. $AB$. Boolean multiplication, $\land$ gate, is implied between bits, e.g. $ab = \land(a, b)$. Other Boolean operations are explicit: $a \oplus b \equiv \text{XOR}(a, b)$ and $a \equiv b \equiv \text{OR}(a, b)$. Boolean negation is denoted with a bar: $\neg a \equiv \text{NOT}(a)$. Boolean operations can be used between numbers in parallel bit-to-bit manner. Explicit bit-by-bit Boolean $\land$ as $\land B$ can be used between numbers. Symmetric 2-out-of-3 function is denoted as:

$$(a, b, c)_2 = ab \parallel bc \parallel ac = ab \parallel c(a \parallel b)$$

Further in the text, terms top bit and most significant bit mean the same. The term top bits means several high order bits including the top bit.

I. INTRODUCTION

A. Background

Can we do modular multiplication of two numbers without number comparison, conventional arithmetic subtraction or addition; or any other elementary operations that depend on the size of the operands of multiplication? This paper describes one possible and sufficiently simple algorithm.

Carry propagation is necessary in normal arithmetic processing numbers. For example, in

$$15 + 1 = 1111_b + 1_b = 10000_b = 16$$

in binary representation the most significant bit of the result depends on the least significant bits of the arguments. In order to obtain the result, the addition algorithm must propagate the bit value through the whole length of the number; through 4 bit positions in the above example. Therefore, number bit-length affects the length of the computation sequence – it is impossible to get the result of the top bit without computing first all lower bit positions.

There are a few ways to rewrite a sum of two or three numbers:

$$A + B = (A \land B) + 2(A \land B)$$
$$A + B = (A \land B) + (A \land B)$$
$$A + B + C = (A \land B \land C) + (A, B, C)_2 + (A \land B \land C)$$
$$A + B + C = (A \land B \land C) + 2(A, B, C)_2$$

The first equation corresponds to carry propagation methods – the equation is applied in iterations until the last term $(A \land B)$ is zero. The second and the third equations are top-up, can be used to reorganize the sum so that the operands are sorted by value. This top-up operation is used further in the presented algorithm. The last equation is a carry-save addition with two useful properties: 1) bit operations can be done independently and in parallel for all bit positions; and 2) the sum of 3 numbers is reduced to a sum of 2 numbers. Hence, a long sequence of additions can be done more efficiently using this trick, since carry-save operation does not depend on the length of the operand numbers.

Normal (non modular) multiplication requires many additions. Carry-save addition can naturally be used, so carry propagated addition is done only once at the very end to obtain the result as one number. In modular multiplication it is not obvious how to use carry-save because it requires reduction operation, that requires comparison, and that, in turn, requires subtraction with carry propagation. The aim of this work is to perform modular multiplication while avoiding carry propagating addition, subtraction and number comparison.

B. Contribution

The algorithm\footnote{Internally called IM1C - Interleaved Modular 1-bit-Radix Carry-save.} for modular multiplication $[AB]_R$, where $R$ is modulus, outputs a pair of numbers $(P, Q)$ such that $P, Q < R$ and $P + Q \equiv AB \mod R$. The algorithm uses only carry-save adders and fixed Boolean logic operations of $O(1)$ complexity.

C. Limitations

Along with $A, B, R$ input the algorithm requires five precomputed values of $R$, e.g. $[2^{n+1}]_R$. Some of them are hard to compute in carry-save only mode in $O(1)$ number of steps. This makes the algorithm less efficient when $R$ is changing from one multiplication to another.
The algorithm outputs two numbers instead of one. At the time of writing, it is not known if producing the result as one final number is possible, given the constrains of using only carry-save addition, fixed Boolean logic of $O(1)$ complexity, and final reduction in $O(1)$ steps. If one number is necessary as the result, an extra addition with carry propagation is needed.

II. ALGORITHM OVERVIEW

A. Interleaved multiplication

The algorithm presented in this paper follows the idea of the classical interleaved modular multiplication [1], which is briefly described below. The expression, seen as Horner’s scheme in powers of 2 expansion:

$$AB = 2(2(\ldots(2( a_{k-1}B + a_{k-2}B) + \ldots + a_2B) + a_1B) + a_0B)$$

gives a direct way to multiply two numbers $A$ and $B$ modulo $R$, where $k$ is number of bits (binary digits) of each these three numbers. In each iteration the accumulator (holding the result value) is multiplied by 2; added $a_iB$; and reduced by $R$. In carry-save mode the reduction step is problematic because comparison between the accumulator and the modulus is impossible. The solution presented here is to drop high bits of the accumulator and compensate the accumulator by adding a specific value in such way that the result remains valid.

B. Conditions and notations

Let’s define the working size of the algorithm as $n$, that is the algorithm can do multiplications up to $n$-bit numbers. Let us call two values of the accumulator as $P$ and $Q$. The current version of the algorithm requires $P, Q$ to be 1 bit larger than the working size: $|P| = |Q| = n + 1$. Assume also $A, B < R, n > 2$ and $n \geq k$, where $k$ is determined by $2^{k-1} \leq R < 2^k$. Therefore, $|A| = |B| = |R| = k$. To simplify expressions in the future, denote $2^k$ as $\beta: \beta = 2^k$.

Input: $n, k, A, B, \{R\}$.

{$R$} is a set of $5$ precomputed values of $R$ and the bit next to the most significant bit of $R$:

\[ {R} = \{ R_n, R_m, R_s(i), R_{k-2} \} \]

\[ R_n = \lceil \beta \rceil_R \]

\[ R_m = \lceil 3\beta/4 \rceil_R \]

\[ R_1 = \lceil 2\beta \rceil_R \]

\[ R_2 = \lceil 4\beta \rceil_R \]

\[ R_3 = \lceil 6\beta \rceil_R \]

Output: $(P, Q)$ such that $P < R$ and $Q < R$, and $P + Q \equiv AB \mod R$.

C. Overall picture

Fig. 1 shows the algorithm overall diagram. **Main Loop**, **Shrink**, and **Squeeze** modules are three sequential steps performing computation. They work on the assumption that the most significant bit of $R$ is 1, i.e. $2^{n-1} \leq R < 2^n$ (note $n$ instead of $k$). To accommodate this condition we shift left (normally assuming the top bit to be in the leftmost position) by $n-k$ bit positions (same as multiply by $2^{n-k}$)

![Fig. 1. Overall diagram of the algorithm.](image)

Fig. 2. Loop module consists of two carry-save adders of size $n+1$. LCU (Loop Control Unit) and the Multiplexer. LCU takes 7 bits as input and outputs 2 bits. The Multiplexer selects one out four values: 0, $R_1$, $R_2$, $R_3$.

![Fig. 2. Loop module](image)

values $B, R, \{R\}$ in Shift-left step. Accordingly before the output we shift right (Shift-right) by the same number of bits (division by $2^{n-k}$) output values $P$ and $Q$.

Main loop module executes interleaved iterations over all bits of $A$ in $k$ cycles. Its output is a pair $(P, Q)$ of size $n+1$, hence, in ranges $0 \leq P < 2\beta$ and $0 \leq Q < 2\beta$. Shrink module reduces values $(P, Q)$ so that their sizes are $n$ and the ranges are $0 \leq P < \beta$ and $0 \leq Q < \beta$, and $P \neq Q<\beta/2$. Finally, Squeeze module does further reduction so the both values $P, Q < R$.

Loop module uses $A, B$, and $R_x$ values. Also it uses value $k$ as the number of iterations. Shrink module uses $R_1$ and $R_n$. Squeeze module uses $R_n$, $R_m$, and $R_{k-2}$.

III. MAIN LOOP MODULE

A. Computation flow

Loop module is the main and most critical part of the algorithm. It executes the iterations over all bits of $A$ starting from bit $k-1$ and going down to 0. This is the only place
where \( k \) is used. From now on it is assumed that \( k = n \) because Shift-left has been applied. Correspondingly \( \beta = 2^n \) in the text below.

As shown in Fig. 2 there are two additions (\( \Sigma \)), Loop Control Unit (LCU), and the multiplexer producing \( R_y \) reduction value. First addition adds to the accumulator, shifted left by 1 bit position, the next value of \( B \) and outputs a pair \((S, C)\):

\[
(S, C) = (2P, 2Q) + a_iB
\]

The second addition adds the reduction value \( R_y \)

\[
(P, Q) \leftarrow (P', Q') = (S, C) + R_y
\]

Note, that both additions are done in carry-save mode in \( n+1 \) sized registers discarding all overflowing bits. Discarded bits can be seen as subtraction of some number \( F \). Value \( R_y \) must match \( F \) to make it valid reduction by \( R \):

\[
R_y - 2\beta F = 0 \mod R
\]

In the above equation \( R_y \) is a value we arithmetically add. The second term \( 2\beta F \geq R_y \) is the value we arithmetically subtract from the accumulator, effectively making reduction.

B. Bit analysis in LCU

The value \( F \) has two important properties: 1) it does not depend on \( R_y \), i.e. \( R_y \) bits do not propagate to the overflow bits; and 2) \( F < 4 \), i.e. has only two bits \( f_1 \) and \( f_0 \): \( F = 2f_1 + f_0 \). The first property breaks the circular dependency; and the second makes the algorithm requirements and computation simple.

To understand why \( F \) has these properties consider the following example. Let \( n = 4 \). The additions can schematically be represented by the worksheet:

\[
\begin{array}{cccccccc}
& p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0 & 0 \\
q_4 & q_3 & q_2 & q_1 & q_0 & b_3 & b_2 & b_1 & b_0 \\
\hline
s_5 & s_4 & s_3 & s_2 & s_1 & s_0 \\
c_5 & c_4 & c_3 & c_2 & c_1 & c_0 & 0 \\
r_5 & r_4 & r_3 & r_2 & r_1 & r_0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{array}
\]

The first line is \( P \) and the second is \( Q \), both are left shifted by 1 bit. The third line represents \( a_iB \). The full result of the addition is all the bits \( s \) and \( c \) on the fourth and fifth lines. Their values are defined by expressions shown below in subsection C. Note, that the bits on the left side of the vertical line \( (p_3, q_3, s_3, \text{etc}) \) do not participate in computation because we use only 5-bit carry-save adder. After the lines with \( s \) and \( c \) bits, we add \( R_y \) value shown as four \( r \) bits resulting in new values of \( P \) and \( Q \), with bits \( p_5, p_6, q_5, \text{and } q_6 \), and \( q_6 \) being overflown. Finally, these overflown bits form the value \( F \).

First observation is that neither \( p_5 \) nor \( q_5 \) depend on \( r_3 \). The highest bit that depends on \( r_3 \) is \( q_4 \) and \( q_4 \) position remains within the \( n+1 \) bounds. Therefore \( F \) does not depend on value \( R_y \). Second observation is that \( s_5 c_5 = 0 \) and \( s_4 c_4 = 0 \), hence the resulting bits satisfy the following both conditions:

\[
\begin{align*}
p_6q_6 &= c_5 s_5 c_4 = 0 \\
p_5q_5(p_6 \parallel q_6) &= (s_5 \parallel c_4) s_4 c_3 (c_5 \parallel s_5 c_4) = 0
\end{align*}
\]

which imply no carry to the position above \( f_2 \) and therefore the sum of two numbers \( (2p_6 + p_7) \) and \( (2q_6 + q_7) \), which is equal to \( F \), has only 2 bits; hence, \( F < 4 \).

Direct derivation of bit values \( f_1 \) and \( f_0 \) gives the control logic for selecting \( R_y \):

\[
\begin{align*}
s_4 &= p_3 \oplus q_3 & s_5 &= p_4 \oplus q_4 \\
c_3 &= (p_2, q_2, b_3) & c_4 &= p_3 q_3 \\
c_5 &= p_4 q_4 & q_5 &= s_4 c_3 \\
f_0 &= q_5 \oplus s_5 \oplus c_4 & f_1 &= c_5 \oplus (s_5, c_4, q_5) \times 2
\end{align*}
\]

This logic is implemented in LCU. Finally, the multiplexer selects one correct value from the array of four: zero and three precomputed values \( (F = 1, 2, 3) \):

\[
R_y = R_x(F) = [2\beta F]_R
\]

In this way, when computing \( F \), LCU inspects 7 bits: the three highest bits of \( P \) and \( Q \) and the most significant bit of \( a_iB \). Then the multiplexer selects the appropriate reduction value \( R_y \).

C. Carry-save adder

Carry-save adder, used in this algorithm, of size \( m \) with three inputs \((X, Y, Z)\) and two outputs \((S, C)\) is a standard carry-save operation defined by the functions:

\[
S = X \oplus Y \ominus Z \\
C = 2(X, Y, Z)_2 \mod 2^m
\]

The reduction on the carry \( C \), erasing the top bit after the shift, is necessary for the correct behaviour of the algorithm.

IV. SHRINK MODULE

A. Components

Shrink module, schematically depicted in Fig. 3 performs the reduction of the accumulator by erasing the top bits of \( P \) and \( Q \) effectively shrinking their size by one bit from \( n+1 \) to \( n \); as well as ensuring that \( P, Q < \beta / 2 \). It runs in cycles up to three times following the logic:

1) Top-up moves top bits between \( P \) and \( Q \);
2) Shrink Control Unit (SCU) analyses a few top bits of \( P \) and \( Q \) and selects one of four rules to apply;
3) Each rule executes one carry-save summation, and clears some bits if necessary.

For the sake of simplicity and without losing generality let us use 4-based indices as shown in the example in Section III-B instead of \( n \)-based. So \( p_4 \) is \( p_{n-1} \), \( q_4 \) is \( q_{n-1} \) and so on.

Top-up operation consists of changing two top bits in \( Q \) to \( P \) as:

\[
\begin{align*}
p'_4 &= p_4 \parallel q_4 & q'_4 &= p_4 q_4 \\
p'_3 &= p_3 \parallel q_3 & q'_3 &= p_3 q_3
\end{align*}
\]
where prime symbol means new values for the corresponding bits. Basically each line swaps two bits if \( p_i = 0 \) and \( q_i = 1 \) and leaves unchanged in all other cases. This operation does not change the value \( P + Q \).

SCU computes ancillary bits (such as \( p_4 q_4, p_3 q_3 \)) and triggers a rule from the following logic:

```
if \((p_4 q_4)\):
  1: add \( R_1 \)
else if \((p_4 p_3 q_3)\):
  2: add \( R_1 \) \( p_4 = q_4 = 0 \)
else if \((p_4)\):
  3: add \( R_n \) \( p_4 = q_4 = 0 \)
else if \((p_3 q_3)\):
  4: add \( R_n \) \( q_4 = 0 \)
else done
```

First, \( p_4 q_4 \) is tested and if true rule 1 is triggered. Its action is to add \( R_1 \) to the accumulator. The addition is done in \( n+1 \) size carry-save adder. In this case discarded overflow is automatically balanced with the addition of \( R_1 \). If rule 1 is not triggered, the condition of rule 2 is tested and if triggered, \( R_1 \) is added and then bits \( p_4 \) and \( q_4 \) are cleared (set to zero). If not, we proceed to the next clause. Rules 3 and 4 work similarly. If any rule is triggered we cycle back to the beginning. Rule 1 or 2 can be triggered only in the first iteration because in the subsequent iterations \( q_4 \) and \( p_4 p_3 q_3 \) cannot be one.

The idea behind this logic is simple: we keep subtracting power of 2: \( \beta \) or \( 2\beta \), and compensate by adding \( R_n \) or \( R_1 \) until the accumulator value is reduced. Subtraction is done by either overflowing (rule 1) or directly clearing the bits after addition.

### B. Number of cycles

Number of Shrink cycles cannot be less than three because of the counterexample \( n = 8, A = 63, B = 121, R = 173 \). On the other hand it is obvious that the number is not greater than 7, since \( P + Q < 4\beta \) and every iteration subtracts a value greater than \( \beta/2 \). It turns out proving that the number of Shrink cycles is not greater than 4 is not too difficult.

**Proof:** Consider three possible cases:

1) One of the top bit of \( P \) or \( Q \) is zero;
2) Both top bits of \( P \) and \( Q \) are ones and \( R < R_c \); and
3) Both top bits of \( P \) and \( Q \) are ones and \( R > R_c \).

Here \( R_c \) is a critical value for \( R_1 \) \( (= [\beta R]) \) such that:

\[
\begin{align*}
R_1 &= 2\beta - 2R - \alpha R \\
\alpha &= 1 \quad \text{if} \quad R < R_c \\
\alpha &= 0 \quad \text{if} \quad R > R_c
\end{align*}
\]

Therefore

\[
R_c = \frac{2}{3}\beta
\]

Remember that \( \beta = 2^\alpha \). Note, that \( R \) is never equal to \( R_c \). The above three cases are exhaustive, thus it is sufficient to prove each case.

**Case 1:** Since one of the top bits of \( P \) or \( Q \) is zero, the total value is limited by \( P + Q < 3\beta \). Each cycle reduces the accumulator by \( \beta \) and adds \( R_n \). After four cycles the new accumulator values \( (P', Q') \) are

\[
P' + Q' = P + Q + 4(-\beta + R_n)
\]

Since \( R_n \equiv [\beta R] \) and \( R \geq \beta / 2 \), \( R_n \) can be either zero: \( R_n = 0 \) if \( R = \beta / 2 \), or if \( R > \beta / 2 \), then:

\[
R_n = \beta - R \quad \text{and} \quad R_n < \frac{1}{2}\beta
\]

\[
P' + Q' < 3\beta + 4(-\beta + \frac{1}{2}\beta) = \beta
\]

The final result is less than \( \beta \) \( (= 2^n) \). Hence both \( P' \) and \( Q' \) each less than \( \beta \), their top bits are zero \( p_4 = q_4 = 0 \) and \( p_3 q_3 = 0 \).

**Case 2:** If both top bits of \( P \) and \( Q \) are ones, then the first cycle reduces the accumulator by \( 2\beta \) and adds \( R_1 \); and the following three cycles do the same as in Case 1:

\[
P' + Q' = P + Q + (-2\beta + R_1) + 3(-\beta + R_n) = \]

\[
= P + Q - 5\beta + R_1 + 3R_n
\]

Since now \( P + Q < 4\beta \), it would be sufficient to prove that \( R_1 + 3R_n < 2\beta \). In Case 2 \( R < R_c \) and \( \alpha = 1 \), so

\[
R_1 + 3R_n = (2\beta - 3R_1) + 3(\beta - R) = \]

\[
5\beta - 6R < 5\beta - 6 \cdot \frac{2}{3} = 2\beta
\]

This proves that \( R_1 + 3R_n < 2\beta \), therefore \( P' + Q' < \beta \), hence \( p_4 = q_4 = 0 \) and \( p_3 q_3 = 0 \).

**Case 3:** When \( R > R_c \), the same logic follows as in Case 2 up to the derivation of \( R_1 + 3R_n \). This time, however, \( \alpha = 0 \) and \( R \) is bound by \( R_c = 2\beta / 3 \) from below:

\[
R_1 + 3R_n = (2\beta - 2R) + 3(\beta - R) = \]

\[
= 5\beta - 5R < 5\beta - 5 \cdot \frac{2}{3} = \frac{5}{3} \beta < 2\beta
\]

As above in Case 2 this proves that \( R_1 + 3R_n < 2\beta \), therefore \( P' + Q' < \beta \), hence \( p_4 = q_4 = 0 \) and \( p_3 q_3 = 0 \). □

In the three cases above it was assumed \( P + Q < 4\beta \) at the beginning. In reality the upper bound is lower, since there are dependencies between the bits of \( P \) and \( Q \). For example, \( P \)
and $Q$ cannot both be equal to $2\beta - 1$ upon the exit from the main loop. It is likely that the number of Shrink cycles is not greater than 3. Proving this statement is much harder. It might be possible to prove formally using symbolic execution or Binary Decision Diagrams. At the time of writing, the idea of the proof may go along the following arguments. The values $R_n$ have at least one zero in the top three bits. This is a result of binary expansions of $2/3$, $4/5$, and $6/7$ - some of the critical values for $R_1$, $R_2$, $R_3$. This causes, after the main loop, having at least one zero in the three top bits of $P$ and $Q$. The reduction in each cycle is done faster because $P+Q$ value is smaller and $\beta - R_n$ (and $2\beta - R_1$) is greater. The statement that 3 cycles are sufficient is left as a conjecture.

V. SQUEEZE MODULE

The output of Shrink module are $P$ and $Q$ value of size $n$ (i.e. $p_4=q_4=0$) and $p_1q_3=0$. Here again, as above, we use 4-based indices as in the example in Section III-B instead of $n$-based. Squeeze module, depicted in Fig. 4, reduces further the accumulator and makes decision on which rule to apply using the following logic:

\[
\begin{align*}
|P| = n \text{ and } |Q| = n - 1 \\
\begin{array}{ll}
\text{top-up} & \\
\text{QCU} & \text{rule 1} \\
& \text{rule 2} \\
& \ldots \\
& \text{rule 6} \\
\end{array}
\end{align*}
\]

\[
P < R \text{ and } Q < R
\]

Note, that the order of clearing bits and summation is opposite comparing to Shrink’s SCU. Along with accumulator bits QCU also inspects the second top bit of $R$, $r_2$. Depending on its value either rules (3, 4) or (5, 6) work.

Rule 1 says that if $p_3$ is zero, then we are done because $q_3$ is zero and $r_3$ is always one, ensuring the exit condition.

Rule 2 is triggered when $p_3$, $p_2$, $q_2$ bits are set. It subtracts $\beta$ by clearing these bits and compensates with $R_n$. Now if $R < 3\beta/4$ (i.e. $r_2 = 0$) rules 3 and 4 are active. Rule 3 makes $R_m$ reductions. And rule 4 does not reduce the accumulator. To ensure the exit condition, it subtracts $\beta/2$ from $P$ and adds $\beta/4$ to $P$ and $Q$, so $P+Q$ remains the same. Now $P < R$ because $r_3 = 1$ but $p_3 = 0$; same for $Q$. For rule 5 we are done, because $p_2 = 0$ implies $q_2 = 0$ but $r_2 = 1$. Rule 6 does the trick similar to rule 4: subtracting $\beta/4$ from $P$ and adding to $Q$. This works because here $R \geq 3\beta/4$ and, before the rule is executed, $P < \beta$ and $Q < \beta/4$. The conditions of these rules list all possible combinations of the accumulator values. The detailed inspection of each rule proves that the result satisfies the exit conditions. Note, that rules missing addition should not perform addition with zero because carry-save addition of $P$ and $Q$ (even with zero) changes their values and may change the top bits.

VI. ACKNOWLEDGEMENTS

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VII. FINAL REMARKS

The purpose of this paper is to present the mathematical solution to the problem. This work does not compare the performance to other algorithms (such as [2],[3]); and does not discuss applications or hardware implementation. Due to no carry propagation, the presented algorithm can be extended to process either long number operations or several shorter in parallel on the same hardware, i.e. reusing operational elements for different length of the operands. Also in chained computation, it can be extended to allow input in the form of $(P, Q)$. The idea can be extended to use 7-to-3 carry-save adders with higher Radix processing. The presented algorithm has been developed without awareness of the plethora of existing carry-save based algorithms. The next step will be to analyse and compare to the other modular multiplication algorithms and possibly extend and optimize it for specific applications.

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