An FPGA-based Direct Sampling and Digital Processing System for Wideband and Narrowband Radar Signal

Yingxiao Zhao¹, Hongliang You¹ and Yue Zhang²,*

¹Information Research Center of Military Science, Academy of Military Sciences, China
²College of Electronic Science, National University of Defense Technology, China

*Corresponding author email: zhangyue05@nudt.edu.cn

Abstract. This paper designs an integrated wideband and narrowband radar signal direct sampling and digital processing system based on FPGA. The system comprises a VPX case, a main board, a direct sampling board, a fiber board. It makes direct sampling of 1.8GHz-3.0GHz echo waves, with 3.2GHz sampling rate. The wideband and narrowband echo waves share the same ADC channel. After ADC sampling, both of wideband and narrowband data are exported to a mix-free digital quadrature demodulation module in FPGA. The narrowband data will be further processed by digital frequency down conversion. The wideband data will be further processed by digital de-chirp operation, with parallel DDS structure and multi-level decimation filters. Data rate of both the wideband and narrowband data after processing is decreased obviously. The designed sampling system cut down the analog radar signal processing operation, and decreases signal distortion. Besides, it integrated the reception, sampling and processing of wideband and narrowband signal, simplified the structure of radar system.

Keywords: Direct sampling; FPGA; Narrowband and wideband signal processing.

1. Introduction

With the development of radar systems, their signal bandwidth is continuously expanding. Radar signal can be divided into wideband signal (gigahertz level or higher) and narrowband signal (megahertz level or lower). The wideband signal has high distance resolution, usually used for target imaging [1, 2]. The narrowband signal has low data rate and high processing efficiency, usually used for target detection and tracking [3, 4]. In traditional radar systems, the narrowband echo will be sampled by ADC after analog frequency down conversion, and the wideband echo will be sampled after analog de-chirp processing. The above methods can reduce the sampling rate obviously, but require two receivers for wideband and narrowband signal respectively [5, 6], which increases the complexity of radar system. Besides, analog signal processing like frequency down conversion and de-chirp operation will bring signal distortion to the received echo and have a bad effect on subsequent digital signal processing[7, 8]. To solve the above problems, an integrated wideband and narrowband radar signal direct sampling and digital processing system is designed in this paper. The wideband or narrowband echo signals share the same analog receiving channel, and are directly sampled in a high ADC rate. In FPGA, the narrowband digital signal is processed through quadrature demodulation and frequency down conversion, and the wideband digital signal is processed through quadrature demodulation and digital de-chirp operation, after which the data rate is greatly reduced.
2. Structure of the System

The appearance of the system is shown in Figure 1. The system comprises a VPX case, a main board, a direct sampling board, a fiber board. The structure of the system is shown in Figure 2. The sampling board makes analog to digital conversion, which is done in an ADC circuit, and digital signal processing, which is done in an FPGA circuit. The fiber board receives the radar control signal and transfers data after processing through high-speed serial fiber channels. The device number of the ADC circuit is EV10AQ190, with 10bit quantization width. The device number of the FPGA is Xilinx XC6VS315t. As Figure 2 shows, the sampling rate is 3.2GHz with 1.6GHz sampling clock, and the frequency range of the echo wave signal is 1.8GHz-3.0GHz.

![Figure 1. Appearance of the System.](image)

We make a basic test of the sampling system, results of which is shown in Figure 3. The spurious free dynamic range (SFDR) is higher than 42dB in the working frequency range.

![Figure 3. SFDR of the system ADC sampling.](image)

The top-level module structure in FPGA is shown in Figure 4. The ADC module is connected with the ADC circuit and outputs the sampled data in 16 parallel channels. The QD module makes digital quadrature demodulation and output the complex I-Q signal in 8 parallel channels. The DDC module makes digital frequency down conversion for narrow band I-Q signal. The Dechirp module makes digital de-chirp operation for wideband I-Q signal. Fiber 1 and Fiber 2 module makes data transmission for processed narrowband and wideband data, respectively.
3. Implementation of Mix-free Digital Quadrature Demodulation

As shown in Figure 4, both of the sampled wideband and narrowband signal will be output to QD module for digital quadrature demodulation. The basic digital quadrature demodulation structure is shown in Figure 5. We multiply the sampled data $x(n)$ with two orthogonal sinusoidal signal $\cos(2\pi f_0/f_s)$ and $\sin(2\pi f_0/f_s)$ respectively to get the complex signal $I_0(n)$ and $Q_0(n)$, and extract the baseband component $I(n)$ and $Q(n)$ by a low pass filter $h(n)$. Then we make $D$ times decimation and get final complex signal $I'(n)$ and $Q'(n)$.

$$I_0(n) = x(n) \cos(2\pi f_0 / f_s) = x(n) \cos\left(\frac{3}{2} n\pi\right)$$ (1)

$$Q_0(n) = x(n) \sin(2\pi f_0 / f_s) = x(n) \sin\left(\frac{3}{2} n\pi\right)$$ (2)

$$I(n) = I_0(n) * h(n)$$ (3)

$$Q(n) = Q_0(n) * h(n)$$ (4)

$$I'(n) = I(2n) = I_0(2n) * h(2n) + I_0(2n-1) * h(2n+1)$$ (5)

In this platform, the sampling rate $f_s$ is 3.2GHz, the frequency range of sampled signal is from 1.8GHz to 3.0GHz, and the frequency of numerically controlled oscillator (NCO) $f_0$ is set to 2.4GHz. So, the frequency range of base band complex signal $I(n)$ and $Q(n)$ is -0.6GHz to 0.6GHz, whose spectrum won’t overlap with 2 times decimation ($D = 2$).

With the above parameter setting, we can conclude that,
\[ Q'(n) = Q(2n) = Q_0(2n) \ast h(2n) + Q_1(2n-1) \ast h(2n+1) \]  
(6)

From Eq. (1) to Eq. (6), we get the final expression of \( I'(n) \) and \( Q'(n) \),

\[ I'(n) = (x(2n)(-1)^n) \ast h(2n) \]  
(7)

\[ Q'(n) = (x(2n-1)(-1)^n) \ast h(2n+1) \]  
(8)

The mixing structure in Figure 5 is simplified as Eq. (7) and Eq. (8), which can save lots of multipliers. Because data after ADC module in Figure 4 is in 16 parallel channels, the final structure of digital quadrature demodulation in this platform is shown in Figure 6. The polyphase filtering structure is clearly elaborated in [9].

**Figure 6.** Final structure of digital quadrature demodulation.

4. Further Processing of Narrowband Echo Wave Signal

The whole flow of narrowband signal sampling and processing is shown in Figure 7. Let \( f_0 \) be the central frequency of the narrowband echo signal. After quadrature demodulation in Section 3, its central working frequency is converted to \( (f_n - f_0) \). Next, digital down conversion (DDC) should be further carried on to move the central working frequency to zero for lower data rate.

**Figure 7.** Whole flow of narrowband signal sampling and processing.

In Figure 7, DDC is realized by frequency mixing with point frequency complex exponential signal, which should be generated in FPGA.

Digital waveform generation can be realized in DDWS (Direct Digital Waveform Synthesis) mode or DDFS (Direct Digital Frequency Synthesis) mode. In DDWS mode, digital waveform is directly
acquired from RAM inside FPGA or memory circuits (DDR, QDR) outside FPGA. In DDFS mode, as shown in Figure 8, the value of sinusoidal function is stored in a look-up table, and digital waveform generation is controlled by phase offset and phase increment. Xilinx provides DDS IP core for DDFS waveform generation [10]. In this paper, we adopt DDFS mode for lower memory resource utilization and more flexible control.

**Figure 8.** Basic structure of DDFS.

For point frequency complex exponential signal used in frequency mixing in Figure 7, the phase offset and phase increment has a constant value in a radar cycle, which is set according to the central frequency of narrowband echo signal. And the whole structure of DDC realized in this paper is shown in Figure 9. Because the output data of QD module is in 8 parallel channels, 8 parallel DDS is instantiated. To ensure the coherence of signal processing in each radar cycle, the DDS should be reset at the beginning of every radar cycle. In Figure 9, narrowband data with different sampling rate is output after multi-stage decimation, which is applied for narrowband echo signal with different bandwidth, respectively. 8 times data decimation is realized by polyphase filtering structure, and other decimation is realized by single channel FIR decimation filter.

**Figure 9.** Structure of DDC and 8 times decimation in narrowband signal processing.
For function test, we recorded the narrowband data after processing of this system. The waveform in time domain and pulse compression result is shown in Figure 10, and Figure 11.

![Narrowband Signal Waveform](image1)

**Figure 10.** System output narrowband signal waveform in time domain.

![Narrowband Pulse Compression Result](image2)

**Figure 11.** Pulse compression result of narrowband signal.

5. **Further Processing of Wideband Echo Signal**

The maximum data rate of signal after digital quadrature demodulation is 6.4GB/s, with 1.6GHz sampling rate and 32bit data width. The bandwidth of wideband signal is 1.2GHz, so data decimation can’t be implemented directly. High data rate brings large pressure on subsequent data store and real-time processing. In this paper, we use digital de-chirp method, which is explicated in [8]. It can decrease signal bandwidth obviously with lower data rate and still ensure high range resolution of wideband signal.

The whole flow of wideband signal sampling and processing is shown in Figure 12. Digital Quadrature has been elaborated in Section 2. And digital de-chirp operation will be designed in this section.
Comparing Figure 7 and Figure 12, the flow of DDC for narrowband signal, and de-chirp operation for wideband signal are similar. And the main difference between them is the form of generated digital waveform which is multiplied with complex echo wave signal. So we adopt the similar structure as Figure 9 to realize de-chirp operation for wideband signal. Based on which we concentrate on the LFM reference signal generation.

Next, we will make derivation of the expression of phase increment and phase offset in each DDS. Let \( N \) the total number of reference LFM signal sampling point, \( n \) be the serial number of waveform sampling point, \( m \) the serial number of parallel channel (the total number of parallel channel is 8, as shown in Figure 9), \( k \) the serial number of waveform sampling point in each channel, and \( x \) the value of reference LFM signal, \( \mu \) and \( \Omega_0 \) the parameter of \( x \). We can conclude that,

\[
x = \exp\left(\frac{1}{2} \mu n^2 + \Omega_0 n\right), \quad n = 0,1,\ldots,N-1
\]

\[
n = 8k + m, \quad m = 0,1,\ldots,7, \quad k = 0,1,\ldots,N/8 - 1
\]

Let \( p(k, m) \) be the phase of LFM signal \( x \). From Eq. (9), Eq. (10), we can acquire the expression of phase offset and phase offset phase increment of DDS in each channel, as shown in Eq. (11), Eq. (12).

\[
p(0, m) = \frac{1}{2} \mu m^2 + \Omega_0 m \tag{11}
\]

\[
p(k + 1, m) - p(k, m) = 64 \mu k + 8 \mu m + 32 \mu + 8 \Omega_0 \tag{12}
\]

From Eq. (12), we can find that when generating LFM signal, the phase offset of DDS in each channel is in linear relationship with \( k \), so, we can generate the phase offset value by an accumulator. The relevant module structure for LFM signal generation is shown in Figure 13.
We make FPGA simulation for digital LFM signal generation using Modelsim tool. The waveform output from each DDS is shown in Figure 14.

![Figure 13. Structure for reference LFM signal generation in FPGA.](image)

![Figure 14. FPGA simulation for digital LFM signal generation.](image)

The realization of data decimation is similar to Figure 9. And sampling rate of de-chirp data includes 40MHz, 20MHz, 10MHz. Let $K$ be the linear frequency modulation rate of LFM signal, $B$ the bandwidth of LFM signal, and $r$ the distance range of target detection. The relationship between $r$ and $B$ can be derived as Equation (5). Suppose the band width and pulse width of the wideband LFM signal is 1.2GHz, 5ms, respectively, and oversampling rate of de-chirp signal is 1.3, we can use de-chirp data with 40MHz sampling rate for distance range of target detection less than 20km, and 20MHz for 10km, 10MHz for 5km.

\[
B = \frac{2K}{c} \cdot r
\]  (13)
6. Conclusion
This paper has designed and realized an integrated wideband and narrowband radar signal direct sampling and digital processing system based on FPGA. The sampling rate is 3.2Gbps, and the frequency range of echo is 1.8GHz-3.0GHz. The SFDR of ADC is higher than 40dB. The narrowband sampling data is processed by quadrature demodulation, frequency down conversion. The wideband sampling data is processed by quadrature demodulation, de-chirp operation. The output data rate is 40MHz, 20MHz, 10MHz, or 2MHz, according to bandwidth of signal for narrowband signal, or distance range of targets for wideband signal. By direct sampling of echo wave, signal distortion in analog channel is obviously overcome. By signal processing in FPGA, high data rate caused by high sampling rate is effectively reduced. By wideband and narrowband integrated sampling and processing, the structure of radar system is simplified.

References
[1] L. Zuo and B. Wang, “ISAR Imaging of Non-Uniform Rotating Targets Based on Optimized Matching Fourier Transform,” IEEE Access, vol. 8, pp. 64324-64330, 2020.
[2] T. Jin, H. Wang and H. Liu, “Design of a flexible high-performance real-time SAR signal processing system,” 2016 IEEE 13th International Conference on Signal Processing (ICSP) in Chengdu, 2016, pp. 513-517.
[3] K. Kim, M. Üney and B. Mulgrew, "Coherent track-before-detect with micro-Doppler signature estimation in array radars," IET Radar, Sonar & Navigation, vol. 14, no. 4, pp. 572-585, 2020.
[4] X. Rao, H. H. Tao, J. Su, X. L. Guo, “Axis rotation MTD algorithm for weak target detection,” Digital Signal Process, vol 26, no. 1, pp. 81-86, 2014.
[5] Y.X. Zhao, Y. Zhang, Q.Q. Lin, T. Li, and Z.P. Chen, “Design and Implementation of a High-speed, Large-capacity, Multi-type Data Recording System Used in Wideband Phased-array Radar,” PIERS(Progress in Electromagnetics Research Symposium) 2017 in St Petersburg, May, 2017, pp. 1-8.
[6] Y. X. Zhao, Y. Su, R. Huang, P. J. Hu, Z. P. Chen, “Design and Implementation of a Radar Waveform Playback System for Real-time Digital Signal Processing Test,” Asia-Pacific Conference on Antennas and Propagation (APCAP 2017) in Xi’an, China, October, 2017, pp. 1-3.
[7] Q. Q. Lin; Y. Zhang; P. F. Tang; Z. P. Chen, “Digital dechirp method based on wideband radar direct IF sampling” Yuhang Xuebao/Journal of Astronautics, vol.34, no. 3, pp. 402-409, March 2013.
[8] Q. Q. Lin, P. f. Tang, B. Yuan and Z. P. Chen, "A new dechirp method for wideband radar direct IF sampling signal," 2012 IEEE 11th International Conference on Signal Processing in Beijing, 2012, pp. 1920-1924.
[9] Richard G.Lyons. “Understanding Digital Signal Processing, Second Edition,” Prentice Hall PTR, 2004: 374-379.
[10] Xilinx, “LogiCORE IP DDS Compiler v5.0”, XAPP1052(v3.3), March 1, 2011,pp. 1-49.