Power dissipation is a fundamental issue for future chip-based electronics. As promising channel materials, two-dimensional semiconductors show excellent capabilities of scaling dimensions and reducing off-state currents. However, field-effect transistors based on two-dimensional materials are still confronted with the fundamental thermionic limitation of the subthreshold swing of 60 mV decade$^{-1}$ at room temperature. Here, we present an atomic threshold-switching field-effect transistor constructed by integrating a metal filamentary threshold switch with a two-dimensional MoS$_2$ channel, and obtain abrupt steepness in the turn-on characteristics and 4.5 mV decade$^{-1}$ subthreshold swing (over five decades). This is achieved by using the negative differential resistance effect from the threshold switch to induce an internal voltage amplification across the MoS$_2$ channel. Notably, in such devices, the simultaneous achievement of efficient electrostatics, very small sub-thermionic subthreshold swings, and ultralow leakage currents, would be highly desirable for next-generation energy-efficient integrated circuits and ultralow-power applications.
Scalability of complementary metal–oxide–semiconductor (CMOS) field-effect transistors (FETs) is a mainstream approach for reducing power dissipation in the rapidly developing field of information technology\(^{-1-4}\). However, CMOS technology still faces a great challenge of feature size (<5 nm, due to the degradation of the off-state leakage current induced by short-channel effects (i.e., direct source–drain punch through, and a loss of gate electrostatic control))\(^{-3,8}\). An efficient way to minimize power consumption is to achieve a steep subthreshold swing (SS) with a fast-switching rate at a reduced supply voltage\(^{-9}\). The emerging two-dimensional (2D) transition metal dichalcogenides\(^{10-12}\), e.g., atomically thin molybdenum disulfide (MoS\(_2\))\(^{13,14}\), are promising channel materials for future electronic chips with scaling dimensions and ultralow off-state currents, due to the high electron effective mass, low dielectric constant, and large bandgap\(^{10-13}\). Furthermore, the atomic-scale thickness and smoothness of MoS\(_2\) also significantly improve the electrostatic gate control capability according to its characteristic scaling length and can efficiently lower the supply voltage\(^{8,10}\). However, the electron in the source usually represents a usual Boltzmann distribution with a potential barrier, which restricts the gate modulation capacity to 60 mV decade\(^{-1}\), as determined by the thermal voltage \((kT/q)^{6,7}\). Hence, to break the “Boltzmann tyranny”, enabling atomic-scale FETs with steep subthreshold behavior and still maintaining high on/off current ratio, is critical for the development of ultralow-power electronics.

Several strategies have been proposed to obtain an SS of sub-60 mV decade\(^{-1}\), such as band-to-band tunneling\(^{8}\), impact ionization\(^{14}\), nanoelectromechanical switching\(^{15}\), Dirac-source\(^{16}\), negative capacitance (NC)\(^{17-20}\), and negative differential resistance (NDR)\(^{21,22}\). The demonstrated threshold-switching behavior acting as an internal amplifier offers a shortcut to conquer the Boltzmann limit and triggers the FET to switch with a sub-\(kT/q\) slope. In particular, the NDR effect in threshold-switching FET is highly predictable and quantifiable for constructing steeply switchable electronic devices with high performance\(^{9,21}\). When compared to a common insulator–metal–transition device (e.g., V\(_{OC}\))\(^{21,23}\), a new type of metal filamentary threshold switch (TS), which generally consists of Ag (or Cu) as an active electrode or dopant in a solid electrolyte, has been demonstrated a lower leakage current and much steeper switching characteristics\(^{24-27}\), and can contribute to suppressing the off-state leakage current of conventional FETs with an abrupt SS\(^{22,28}\). The seamless device architecture based on a 2D FET and TS may realize the simultaneous achievement of efficient electrostatic control, small sub-thermionic SS, and low leakage current, leading to efficiently minimizing power dissipation.

Here, we present an atomic threshold-switching MoS\(_2\) FET (ATS-FET) with sharp on/off switching properties and ultralow energy consumption. The ATS-FET is endowed with an abrupt amplification capacity via integrating an abrupt variable-resistance Ag atomic TS with an atomically thin MoS\(_2\) channel. The channel thickness and metal film at the atomic scale are critical to reducing the supply voltage. The common HfO\(_2\) insulator functions as the dielectric layer for the FET and the electrolyte for the TS, which is promising for future monolithic integration of the ATS-FET configurations with facile fabrication processes. The NDR effect according to the abrupt resistance transition of the TS induces an internal voltage amplification across the MoS\(_2\) channel, which enables the MoS\(_2\) FET to significantly overcome the fundamental thermionic limitation. According to the atomic thickness of the MoS\(_2\) channel and the Ag atomic conductive filament (Ag filament), the superior electrical performances, such as on/off current ratio >10\(^6\), ultralow cutoff current at \(1 \times 10^{-13} \text{ A} \mu \text{m}^{-1}\), an average SS (SS\(_{\text{average}}\)) of sub-5 mV decade\(^{-1}\) (median), and very small hysteresis, are achieved in the ATS-FET. We systematically investigate the influence of the NDR effect on the internal amplification phenomena and evaluate the improved electrical performance of the ATS-FET. The proposed ATS-FET has great potential to be extended to scalable and monolithic steep-slope transistor arrays and is of great significance in energy-efficient and high-performance electronic switches with ultralow-power dissipation.

**Results**

**ATS-FET design.** Figure 1a shows a schematic illustration of the ATS-FET by integrating an Ag atomic TS in series with a MoS\(_2\) FET. The FET shares the same HfO\(_2\) dielectric with the TS (acting as the electrolyte in the TS). Triangle-shaped MoS\(_2\) nanoflakes are first synthesized on a SiO\(_2\)/Si substrate by chemical vapor deposition (CVD). The source/drain electrodes (Cr/Au) top-contacted with the MoS\(_2\) are prepared via standard e-beam lithography (EBL), thermal evaporation, and lift-off process. The common HfO\(_2\) thin film is deposited with atomic layer deposition (ALD), functioning as both the dielectric layer of the FET and the electrolyte of the TS. The Ag atomic layer is patterned on HfO\(_2\) by a standard liftoff process. Top gate and drain contacts are defined at the desired position via EBL and metallization. The structural design of the common HfO\(_2\) layer simplifies the fabrication process, while ensuring a high-\(k\) dielectric performance for FET operation and good electrochemical kinetics for threshold switching. The fast formation and spontaneous rupture of the atomic Ag filament in the TS will lead to abrupt on/off switching in the ATS-FET with an ultralow SS (Fig. 1a).

Figure 1b depicts the equivalent circuit diagram of the ATS-FET, which can be considered as a baseline MoS\(_2\) FET in series with a TS device. The supply voltage (or drain-to-source voltage, \(V_D\)) drives the TS and the MoS\(_2\) channel, while the gate-to-source voltage (\(V_G\)) controls the switching characteristics of the ATS-FET. The supply voltage variably distributes between the TS and FET, corresponding to a voltage drop of \(V_T\) for the whole device and \(V_{DT}\) for the MoS\(_2\) FET, respectively. Based on the series TS configuration, \(V_G\) can tune the Fermi level of the MoS\(_2\) channel and lead to efficient control of the channel resistance, which dominantly determines the voltage drop between the FET and TS in the series configuration. The band diagrams of the ATS-FET for a typical \(V_G\) (compared with the threshold voltage, \(V_{TH}\)) are illustrated in Fig. 1c, d. The HfO\(_2\) electrolyte layer in the series TS can be considered as a variable barrier for electron transport according to the applied \(V_G\), which determines the voltage drop on the MoS\(_2\) channel and the TS component. For \(V_G < V_{TH}\), the Fermi level of MoS\(_2\) is slightly shifted downwards (the MoS\(_2\) channel resistance is maintained at a high level). The current across the TS is insufficient to trigger the bridging of the Ag filament. The HfO\(_2\) electrolyte layer acts as a large barrier to blocking the transport of electrons. When \(V_G > V_{TH}\), the MoS\(_2\) Fermi level is effectively shifted downwards (the MoS\(_2\) channel resistance transits to a low level). The current across the TS could induce the Ag filament formation, leading to an abrupt current increase (the mechanism will be discussed below in detail). An optical image of the ATS-FET device is shown in Fig. 1e. The TS stack (Au/Ag/HfO\(_2\)/Au) is connected in series to the FET, sharing its top electrode as the drain electrode of the ATS-FET. Figure 1f shows the Raman spectrum of a CVD synthesized MoS\(_2\) nanoflake excited with a 532 nm laser. The peaks of the in-plane \(E_{2g}\) and out-of-plane \(A_{1g}\) vibration modes at 386.2 and 406.6 cm\(^{-1}\), respectively, indicate that the as-grown MoS\(_2\) is a monolayer.

**ATS-FET versus the baseline FET.** The transfer characteristics (\(I_D–V_G\)) of the ATS-FET and the baseline MoS\(_2\) FET are presented...
ATS-FET under thermal equilibrium with the CVD synthesized MoS$_2$ nano
transition of the TS. The enhanced performance of the ATS-FET is essentially attributed to the abrupt switching transition of the TS. $V_D$ is the drain-to-source voltage across the TS and the MoS$_2$ FET. $V_G$ is the gate-to-source voltage across the MoS$_2$ FET. The equivalent circuit schematic of the ATS-FET, which can be considered as a baseline MoS$_2$ FET in series with a TS device. $V_D$ is the drain-to-source voltage across the TS and the MoS$_2$ FET. $V_G$ is the gate-to-source voltage across the MoS$_2$ FET. 

In the series combination, $V_D$ is divided between the MoS$_2$ channel and the TS corresponding to their individual resistances. The off-state (or leakage) current of ATS-FET is commonly determined by the ultrahigh resistance of the TS, leading to a further decrease of $I_D$ to a lower level of $1 \times 10^{-13}$ A $\mu$m$^{-1}$. Initially, at a low $V_G$, the $I_D$ flowing through the MoS$_2$ channel and TS is insufficient to induce the switching of TS. As $V_G$ increases (i.e., forward sweep), the MoS$_2$ channel resistance shows a gradual decrease until $I_D$ approaches a critical threshold ($I_{th,TS}$), which is capable to induce the switching on of TS (to low-resistance state, LRS). And consequently, the total resistance of the ATS-FET dramatically decreases and triggers an abrupt $I_D$ increase. On the contrary, as $V_G$ decreases (i.e., reverse sweep), the MoS$_2$ channel resistance shows a gradual increase until $I_D$ reduces to another critical threshold ($I_{hold,TS}$), which could reversely induce the switching off of TS (back to high-resistance state, HRS) and causes a rapid drop of $I_D$. Hence, hysteresis in the transfer curve can be found as a result of the difference in $V_G$ corresponding to the two critical thresholds (Fig. 2a). Different from that of the baseline FET (clockwise), the hysteresis of the ATS-FET resembles an anticlockwise transition that is caused by the series integration of the TS.

From the subthreshold region of the ATS-FET (in Fig. 2a), the extracted $SS_{min}$ in forward and reverse sweeps are 2.5 and 4.5 mV $\mu$m$^{-1}$, respectively, as shown in Fig. 2b. Besides, the ATS-FET has a large range of $I_D$ (over four decades) where the average SS ($SS_{average}$) is 3.0 mV $\mu$m$^{-1}$ in the forward sweep. It is considered that the NDR effect originating from the volatile threshold-switching behavior in the atomic Ag filament device induces an efficient internal voltage amplification across the atomically thick MoS$_2$ channel, and contributes to inducing a record and significantly reduced SS, which is much smaller than the values previously reported for a tunnel FET (TFET) at 31.1 mV $\mu$m$^{-1}$ (ref. 8), an NC-FET at 41.7 mV $\mu$m$^{-1}$ (ref. 19), a Dirac-source CNT FET (DS-FET) at 35 mV $\mu$m$^{-1}$ (ref. 16), and an ion liquid gating FET at 50 mV $\mu$m$^{-1}$ (ref. 29). Moreover, the subthreshold characteristics of various types of the steep-slope MoS$_2$ FETs are outlined in Supplementary Table 1. A record on $SS_{min}$ of 0.3 mV $\mu$m$^{-1}$ and $SS_{average}$ of 1.3 mV
decade\(^{-1}\) (over three decades) is also achieved in the ATS-FET at room temperature.

Both reductions in off-state current and SS in the ATS-FET. Power dissipation is a fundamental issue for advanced CMOS technology, which faces two severe challenges: the increasing difficulty for the supply voltage scaling, and the rising leakage currents causing on/off current ratio degradation. The energy efficiency of a logic operation can be estimated through the total switching energy \(E_{\text{total}}\) consisting of dynamic \((E_{\text{dynamic}})\) and static \((E_{\text{static}})\) parts, defined as:

\[
E_{\text{total}} = E_{\text{dynamic}} + E_{\text{static}} = a C_L V_D^2 + I_{\text{off}} V_D \tau_{\text{delay}},
\]

where \(C_L\) is the switched capacitance, \(\tau_{\text{delay}}\) is the delay time, \(a\) is the activity factor, and \(y\) is a fitting parameter. It can be inferred from the above equations that the steeper SS and a lower off-state current in FETs enable further scaling of the supply voltage and a corresponding reduction in total power dissipation. As shown in Fig. 2c (orange region), the integration of the TS with the baseline MoS\(_2\) FET helps to significantly suppress the on-state leakage currents by ~30 times, attributing to the ultrahigh resistance of the TS in the off-state (~1 T\(\Omega\)). Besides, \(S_{\text{off}}\) of the ATS-FET in forward and reverse sweeps have been demonstrated to greatly decrease to 2.5 and 4.5 mV decade\(^{-1}\), respectively. Both of them are far lower than the fundamental thermionic limitation and those of the baseline MoS\(_2\) FET (close to 50 times reduction, the cyan region of Fig. 2c).

**Electrical properties of the ATS-FET.** To exclude the effects of the \(V_G\) sweeping rate on the ultralow SS, the transfer characteristics \((I_D-V_G)\) of the ATS-FET are measured at slow and fast \(V_G\) sweep speeds of 3 and 30 mV s\(^{-1}\), respectively. As illustrated in Fig. 2d, identical steep-slope switching characteristics with high on/off current ratios over \(10^6\) are observed at different \(V_G\) sweep speeds. The SS, \(V_T\), off-state current, and on/off ratio are all independent of the \(V_G\) sweeping rate. In addition, the transfer characteristics \((I_D-V_G)\) of the ATS-FET at \(V_D=0.2\) and 0.3 V are shown in Fig. 2e. In the forward sweep, the SS\(_{\text{average}}\) at \(V_D=0.2\) and 0.3 V are characterized to be 4.5 mV decade\(^{-1}\) (over five decades) and 6.0 mV decade\(^{-1}\) (over four decades), respectively. Meanwhile, \(V_T\) of the ATS-FET shows a negative shift from ~1.14 to ~1.59 V, which is determined by the balances between the supply voltage and the relevant potential drops on the FET and TS during the \(V_G\) sweeping. At a higher \(V_D\), the TS favors a tendency for the turn on state; consequently, the abrupt resistance change is less efficient, and it is easier for the TS to be switched on at a lower \(V_G\). In the reverse sweep, the \(I_D\) of the ATS-FET decreases until it reaches the critical threshold \(I_{\text{hold-TS}}\) (<5 \(\times\) \(10^{-11}\) A m\(^{-2}\)), leading to the instantaneous switching off of the TS. And hence, the ATS-FET shows similar abrupt switching characteristics in the threshold region regardless of \(V_D\). The output characteristics \((I_D-V_G)\) of the ATS-FET for different \(V_D\) are characterized, as shown in Fig. 2f. The channel current \(I_D\)
increases from $6.7 \times 10^{-8}$ to $2.1 \times 10^{-6}$ A $\mu$m$^{-1}$ as $V_G$ increases from $-2$ to $2$ V in the linear/saturation region, showing an increase in the channel conductance with increasing $V_G$. Distin-
guishable on- and off-states are observed in different $V_D$ regions ($V_D < V_{th-TS}$ or $V_D \geq V_{th-TS}$ $V_{th-TS}$ is the threshold voltage of the TS), as shown in Fig. 2f. As $V_D$ increases, when $V_D < V_{th-TS}$ the conductance of the ATS-FET is primarily determined by the TS, even though the MoS$_2$ channel is in a LRS; when $V_D \geq V_{th-TS}$ the conductance of the ATS-FET is coordinated by the MoS$_2$ channel. Similarly, as $V_F$ decreases, the conductance of the ATS-FET shows a sudden reduction when $V_F \leq V_{hold-TS}$ ($V_{hold-TS}$ is the hold voltage of the TS). Moreover, the output characteristics of another ATS-FET and its baseline FET at different $V_G$ (from $-2$ to $2$ V) in linear scale are also demonstrated in Supplementary Fig. 1. It is clearly observed that the abrupt switching on/off behavior of TS contributes to causing the steep-slope phenomenon of the 2D FET.

**Ag atomic threshold switching.** The excellent subthreshold characteristics of the ATS-FET are attributed to the series integration of high-performance TS device. Therefore, it is critical to achieving a TS device with superior threshold-switching behavior. The typical $I$–$V$ characteristic of the as-fabricated TS device at a compliance current ($I_{cc}$) of 100 nA is shown in Fig. 3a. The TS exhibits volatile threshold-switching behavior with a small threshold voltage of the TS ($V_{th-TS} \sim -0.26$ V), an ultralow leakage current ($<1$ pA), and a high on/off current ratio ($>10^3$). The TS device switches from the off-state to the on-state at an applied voltage ($V_D$) larger than $V_{th-TS}$ (green curve in Fig. 3a), while it switches to the off-state at $V_D$ less than the hold voltage ($V_{hold-TS}$ grey curve in Fig. 3a). The TS device yields an extremely steep on/off switching slope $<0.5$ mV decade$^{-1}$, and $V_{th-TS}$ ranges between 0.205 and 0.265 V in the cyclic tests. Energy-dispersive X-ray spectroscopy (EDS) line profiles of the cross-sectional TS stack layers are shown in Fig. 3b. The inset is a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image. The sphere-shaped Ag layer, HfO$_2$ dielectric layer, and top/bottom electrode (TE/BE) layers can be clearly observed, with the Ag atomic-scale layer accumulated at the interface of TE/HfO$_2$.

To investigate the effect of the filament morphology on the switching dynamics, the formation and rupture of the Ag filament at a $V_D$ of 0.4 V are illustrated in Fig. 3c via a Monte Carlo simulation (the flow chart is shown in Supplementary Fig. 2). The on/off-state of the TS is determined by the formation/rupture of Ag filament with volatile threshold-switching behavior. The HfO$_2$ electrolyte layer of the TS can be considered as a variable barrier for electron transport. The Ag nanoparticles diffusion into HfO$_2$ matrix contributes to electrons transport along the nanoparticle chain (i.e., filament), and the adjacent Ag nanoparticles can act as electron traps for thermionic emission or tunneling$^{30}$. As shown in Supplementary Fig. 3, the Arrenius curve is used to explain the temperature dependence of the leakage current of a TS device. The charge transport of the TS at HRS is governed by a combination of Frenkel-Poole (F-P) emission and trap-assisted tunneling (TAT) process$^{31-33}$. Specifically, in the high-temperature region ($>200$ K), the current strongly depends on the temperature, indicating the F-P emission mechanism. In contrast, in the low-temperature region ($<200$ K), the current shows weak temperature-dependent behavior due to the existence of the TAT mechanism.

By applying a large voltage on the TS, the abrupt formation of the Ag filament commonly induces the NDR effect across the TS. The measured $I$–$V$ characteristics of the TS device in voltage-sweeping and current-sweeping modes are shown in Supplementary Fig. 4, indicating good performances for current-controlled (or S-type) NDR behavior. The NDR effect is further illustrated with a control sample (the TS connected with a resistor $R_L$, Supplementary Fig. 5a) to study the distribution of the voltage drops during the on/off switching process of the TS. The NDR effect induces an abruptly decreased voltage drop ($V_{TS} - \Delta V_{NDR}$) across the TS device, and consequently an amplified voltage drop ($V_L + \Delta V_{NDR}$) across the series resistor (Supplementary Fig. 5a). The decrease in the voltage drop ($-\Delta V_{NDR}$) across the TS device can be extracted from the AC $I$–$V$ characteristics (Supplementary Fig. 5b). According to the analysis of the control sample, it can be predicted that the NDR effect can induce a similar internal voltage amplification by replacing the resistor with a MoS$_2$ FET.

**Fig. 3 Ag atomic threshold-switching (Ag/HfO$_2$-based TS).** a) Typical $I$–$V$ characteristic of the TS device at a compliance current ($I_{cc}$) of 100 nA in forward (green)/reverse (grey) voltage sweeping, exhibiting ultralow leakage currents (<1 pA). b) Energy-dispersive X-ray spectroscopy (EDS) line profiles (including Ag, Hf, and O elements) of the TS stack layers along the red line shown in a cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image. Scale bar: 10 nm. c) Simulation for the formation and rupture procedures (on/off) of the atomic Ag filament in the TS device with an applied voltage of 0.4 V.

**Monitoring the internal amplification in the ATS-FET.** The equivalent circuit diagram of the ATS-FET can be considered as two variable resistors connected in series, as shown in Fig. 4a. We try to disclose the working mechanism of the ATS-FET by using mathematical derivation and simulation with a semi-quantitative model$^{34-36}$ and the simulation is illustrated in Supplementary Fig. 6 and Note 1. Taking the highly nonlinear $I$–$V$ characteristics both of TS and baseline MoS$_2$ FET into consideration, the node voltage ($V_{G}$) and the channel current ($I_D$) can be solved as the intersections of output characteristics ($I_D$–$V_{DS}$, black lines) of the baseline MoS$_2$ FET and the $I$–$V$ curve ($I_D$–$V_{DS}$, red line) of TS device for different $V_G$ (see Supplementary Fig. 6c). Impressively, the simulated transfer curves extracted from Supplementary Fig. 6c are in good agreement with the experimental data, as depicted in Fig. 4b. From a physical viewpoint, the steep SS phenomenon is caused by the NDR effect of TS, and it can be understood by a concept of internal amplification gain ($\beta = \frac{dV_D}{dV_G}$), which is defined to describe
the relationship between \( V_D' \) and \( V_G \). According to the definition of subthreshold swing, SS can be written as

\[
SS = \frac{\partial V_G}{\partial \log(I_D)} = \frac{\partial V_G}{\partial V_D'} \times \frac{\partial V_D'}{\partial \log(I_D)} = \frac{2.3kT}{q} \times \frac{\beta}{n} \times \frac{\exp \left( \frac{qV_D'}{kT} \right) - 1}{\exp \left( \frac{q\beta}{kT} \right) - 1}
\]

(2)

where \( V_D' \) is the output voltage at the internal node \( D' \), \( \beta \) is the internal amplification gain, \( n \) is the ideal factor, \( q \) is the basic electron charge, \( k \) is the Boltzmann constant, and \( T \) is the absolute temperature. Ideally, \( \beta \) is approximated to be infinity (i.e., \( \Delta V_G = 0 \)) in the forward switching process, and thus SS will be approximated to be zero. However, due to the inevitable limitation by the accuracy of the testing instrument, the measured SS is \( >0 \text{ mV decade}^{-1} \), when \( \beta \rightarrow \infty \).

To verify and further elaborate the internal amplification induced by the NDR, we monitor the output voltage at the internal node \( D' \) (\( V_D' \)) and analyze the voltammetry characteristics under current sweeping at two different \( I_D \). According to \( V_{th-TS} \) at \(-0.26 \text{ V} \), we reasonably select two typical \( V_D' \) values (0.2 and 0.3 \text{ V}, i.e., \( V_D' < V_{th-TS} \) and \( V_D' > V_{th-TS} \), respectively). As shown in Fig. 4c, the abrupt increases in \( V_D' \) are clearly observed under both \( V_D'(V_D < V_{th-TS} \) and \( V_D' > V_{th-TS} \)). As \( V_G \) sweeps over \( V_T \), the redistribution of the effective potential drops on the MoS\(_2\) channel and the TS pulls up (increases) \( V_D' \) according to the drain voltage superposition effect. The \( V_D' \) drop on the MoS\(_2\) channel is amplified according to the NDR effect caused by the TS transition from the off-state to the on-state. Notably, the trends of the variation in \( V_D' \) are obviously distinguishable for different \( V_D' \). \( V_D' \) at \( V_D = 0.3 \text{ V} \) shows an initial decrease with a subsequent increasing trend, while \( V_D' \) at \( V_D = 0.2 \text{ V} \) only shows an increase at the pull-up point. The pull-up \( V_G \) value also shifts from \(-1.45 \text{ to } -1.04 \text{ V} \) as \( V_D \) decreases from 0.3 to 0.2 \text{ V} (inset of Fig. 4c). The underlying reason is explained by the voltammetry characteristics under current sweeping. For \( I_D < I_{th-TS} \) (Fig. 4d), the TS is initially in the off-state at \( I_D = 1 \times 10^{-12} \text{ A} \mu\text{m}^{-1} \). To maintain a low current in the series circuit, \( V_D' \) is therefore kept at a low level to minimize the current in the MoS\(_2\) FET. As \( I_D \) increases, \( V_D' \) slightly increases. When \( I_D \) is large enough (exceeding \( 1.6 \times 10^{-12} \text{ A} \mu\text{m}^{-1} \)) to trigger the Ag filament formation in the TS, the resistance of the ATS-FET abruptly decreases with \( V_D' \) representing a steep increment (\( \Delta V_{NDR} \)). In contrast, \( V_D' \) is initially at a high level (0.263 \text{ V}) for \( V_D > V_{th-TS} \) (Fig. 4e). This may be because the supply voltage applied from the drain electrode is transiently imposed on the TS component and triggers the bridging of the Ag filament. The instantly increased device current results in a high \( V_D' \) at the beginning. Then, \( V_D' \) dramatically decreases with a subsequent slight increasing.
trend as $I_D$ sweeps. When $I_D$ exceeds $1.4 \times 10^{-12} \, \text{A} \, \mu\text{m}^{-1}$, $V_D$ represents a steep increment ($\Delta V_{NDR}$). As the supply voltage in Fig. 4e is larger than that in Fig. 4d, the trigger current for the Ag filament would be relatively smaller, which is consistent with the results in Fig. 4c.

Furthermore, the internal amplification gain ($\beta = \frac{\text{d}I_D}{\text{d}V_D}$) extracted from the abrupt switching region is $\sim 22.2$ for a low supply voltage at $V_D = 0.2$ V (the inset of Fig. 4f), corresponding to the $S_{\text{SS}}$ of 2.5 mV decade$^{-1}$ and the $S_{\text{average}}$ of 3.0 mV decade$^{-1}$ over four decades of $I_D$. As the internal amplification gain increases to 28.6, the $S_{\text{average}}$ can be further reduced to a record of 1.3 mV decade$^{-1}$ (Fig. 4f). The internal amplification gain is considered a significant parameter for designing steeper-slope FETs with lower energy consumption.

Based on the above discussion, the internal voltage amplification in the ATS-FET according to the voltage snapshot ($\Delta V_{\text{NDR}}$) induced by the NDR effect is directly observed in this work. From the point of view of charge carriers, the free electrons transported in the ATS-FET are blocked by the barrier of the HfO$_2$ electrolyte at the beginning ($V_G < V_T$). When $V_G$ reaches $V_T$, $I_D$ increases in an abrupt fashion as a result of the Ag filament formation. Hence, the ATS-FET can in principle overcome the fundamental thermionic limitation of 60 mV decade$^{-1}$ at room temperature.

**Improved ATS-FET with much-reduced hysteresis and SS.**

Hysteresis is commonly undesirable for transistors in logic applications. Technically, the achievable ATS-FET with small hysteresis (or hysteresis-free) and ultralow subthreshold characteristics is capable of offering the promising potential for ultralow-power logic circuit applications. However, the ATS-FET described above exhibits large hysteresis of 0.5–1 V (Fig. 2), which in essence needs to be greatly reduced. Some device optimization methods were used to reduce the hysteresis, such as annealing, and passivation, as previously reported. To suppress the hysteresis of the ATS-FET, we also present an effective approach of device optimization by using the TS device with highly ordered Ag nanodots, which could contribute to shrinking the switching window (e.g., reducing the difference between $V_{\text{th-TS}}$ and $V_{\text{hold-TS}}$) and improving $I_{\text{hold-TS}}$ of TS. The newly presented TS device is fabricated with a HfO$_2$ layer of 10 nm, an active electrode of highly ordered Ag nanodots, and followed by a process of rapid thermal annealing. It is critical to treat the atomic Ag layer with rapid thermal annealing to make the Ag atoms accumulate in a spherical shape, which is preferential for interstitial dopants in HfO$_2$ to guarantee the volatile threshold-switching behavior even at a high-compliance current. With the compliance currents ($I_{\text{cc}}$) defined from 10 nA to 50 $\mu$A, the TS device shows abrupt and volatile threshold-switching behavior (Supplementary Fig. 7a). And the TS device also exhibits good stability in the cyclic test (Fig. 5a), achieving a reduced switching window of 0.12–0.24 V and small variations both in $V_{\text{th-TS}}$ and $V_{\text{hold-TS}}$ (Supplementary Fig. 7b). Furthermore, by connecting such TS device to a MoS$_2$ FET, an improved ATS-FET is demonstrated to have much-reduced hysteresis and SS in a highly reproducible manner. The output characteristics ($I_D$ vs $V_D$) of the improved ATS-FET for different $V_G$ are shown in Supplementary Fig. 8.
Fifty continuous cycles of the output characteristics (at $V_G = 2$ V) in Fig. 5b can also verify the stable and repeatable operations of the ATS-FET. From the transfer characteristics in Fig. 5c, we can see that the improved ATS-FET shows reduced hysteresis of <0.15 V at different $V_D$ (ranging from 0.7 to 1.1 V). More impressively, the nearly negligible hysteresis (10 mV) is observed at the $V_D$ of 0.7 V, meanwhile the $SS_{\min}$ in forward and reverse sweeps are 2.6 and 12.5 mV decade$^{-1}$, respectively (Supplementary Fig. 9). Further extracting key parameters, including $SS_{\text{forward}}$, $SS_{\text{reverse}}$, hysteresis, and $V_T$, from three ATS-FETs are shown in Supplementary Fig. 10. The $SS_{\text{forward}}$, $SS_{\text{reverse}}$, and hysteresis are all independent of $V_D$, while the $V_T$ shows the negative shift with the increase of $V_D$ (consistent with that of Fig. 2e).

**Statistical analysis of ATS-FET and the device comparison.** To more clearly illustrate the reproducibility of the ATS-FET, we conduct the statistical analysis for the average SS (including $SS_{ \text{forward}}$ and $SS_{ \text{reverse}}$), and hysteresis in cycle-to-cycle (80 cycles) and device-to-device (50 devices) variations. Figure 5d shows the histograms and Gaussian fits for the $SS_{ \text{forward}}$, $SS_{ \text{reverse}}$, and hysteresis (4.8 and 4.6 mV decade$^{-1}$; 0.14 V) of the ATS-FET in 80 cycles. Besides, the abrupt switching behavior of the ATS-FET is free of device-to-device deviations. The Gaussian distributions of the $SS_{ \text{forward}}$, $SS_{ \text{reverse}}$, and hysteresis are plotted in Fig. 5e, showing that the statistical $SS_{ \text{forward}}$, $SS_{ \text{reverse}}$, and hysteresis mainly distribute at 5.3 mV decade$^{-1}$, 6.1 mV decade$^{-1}$, and 0.19 V, respectively.

According to the above-described Eq. (1), $V_D$ and SS synergistically contribute to the evaluation of power consumption in the FET device. And hence, it is recommended that both $V_D$ and SS are preferred to be minimized, in addition to the suppressed hysteresis in transfer curves. Compared with previous reports of different categories of steep-slope transistors, including the TFET$^{8,39,40}$, NC-FET$^{18-20,41-46}$, phase-FET$^{21,47,48}$, Ag (or Cu) filament TS-FET$^{22,28,49}$, resistive-switching FET$^{50,51}$, and DS-FET$^{16}$, the relations of SS–hysteresis and SS–$V_D$ are both summarized and depicted in Fig. 5f. Capable of achieving steeper SS, reducing hysteresis, and scaling $V_D$, the ATS-FETs show superior performances by using the atomic-scale geometry design with seamless integration of 2D FET and TS. Specifically, the achieved ATS-FET is nearly hysteresis free (10 mV), and has ultralow $SS_{\min}$ of <2.6 mV decade$^{-1}$, which can satisfy the ITRS requirement for the SS of 25 mV decade$^{-1}$ in the year of 2027 (ref.1), and will be promising for future electronics with ultralow-power consuming.

**Discussion**

In summary, we successfully demonstrate an ATS-FET that significantly overcomes the fundamental thermionic limitation of the SS. This ATS-FET achieves extremely abrupt steepness in the turn on characteristics with a typical $SS_{\text{average}}$ of 4.5 mV decade$^{-1}$ for more than five decades of $I_D$ at room temperature, and exhibits a significant off-state leakage current reduction to lower the power dissipation. According to the analysis of the $I$–$V$ dynamics in the ATS-FET both in experiment and simulation, the NDR effect from the TS transition can contribute to inducing an internal $V_D$ amplification across the MoS$_2$ channel, enabling the ATS-FET to break the “Boltzmann tyranny”.

As a benefit of the active materials in atomic scale (MoS$_2$ and Ag filament), the proposed ATS-FET permits the critical scaling of the supply voltage and exhibits superior electrical performances, as well as greatly suppressed off-state current (Supplementary Fig. 11). In addition, the $V_D$ can be readily scaled by reducing the HfO$_2$ thickness of TS, but the abrupt SS behavior can be maintained independent of the variable HfO$_2$ thickness (Supplementary Fig. 12). The geometry design with seamless integration of FET and TS is promising for the potential monolithic integration of the ATS-FET in wafer scale. In this work, the sharp on/off switching properties with ultralow SS in the ATS-FET is originated from the threshold-switching behavior with an internal voltage amplifier, which is universal and applicable to other emerging 2D semiconducting materials related FETs and even different types of transistor devices. To meet the practical applications of logic circuits (also illustrated in the ITRS), the ATS-FETs are available with additional optimization from technical aspects, e.g., further decreasing off current, SS and hysteresis, and improving on/off ratio and reliability. Based on the simulated analysis (Supplementary Fig. 13 and Note 2), the ATS-FET with hysteresis-free behavior is possible to be achieved. Alternatively, in the case of the steep-slope FETs with hysteresis, they could be potentially used as memory devices$^{52}$ or some specific logic circuits, e.g., Schmitt trigger$^{53}$. Looking forward, the achievement of an ultralow-power steep-slope ATS-FET would coordinate with the scientific research of short-channel devices to efficiently reduce power dissipation, which is highly desirable for next-generation energy-efficient integrated circuits and ultralow-power electronics.

**Methods**

**Device fabrication.** The MoS$_2$ nanoflakes were initially synthesized on highly p-doped rigid silicon (Si) substrates with a thermally grown 275 nm-thick SiO$_2$ layer through CVD. Copolymer and polymethyl methacrylate were spin-coated at 4000 r.p.m. and then baked on a hot plate at 150 °C. Subsequently, the source–drain electrodes of the MoS$_2$ transistor and the BEs of the TS were simultaneously defined with a standard EBL process, thermal evaporation of Cr/Au (10/40 nm), and lift-off process. A dielectric HfO$_2$ layer of 5–20 nm was fabricated via ALD (PICOSUN/SUNALE R-200) approach. A pre-deposited seed layer of 1 nm of Al via thermal evaporation could help to obtain a high-quality dielectric film. The top gate electrodes of the MoS$_2$ transistor were defined by a second EBL process and metallization of Cr/Au (10/40 nm). The top electrodes of the TS were defined by a third EBL process and metallization of Ag/Au (3/40 nm).

For the TS device with highly ordered Ag nanodots, an ultrathin AAO template was transferred onto the prepared layers after the step of ALD, and then patterned an Ag thin film (4 nm), and followed by a process of rapid thermal annealing (500 °C for 30 s) after the removal of AAO template. The bottom and top electrodes were fabricated following the above-described process. The as-fabricated TS device can be connected to a baseline FET (MoS$_2$, monolayer or multilayer) to construct the ATS-FET.

**Materials characterization and electrical measurements.** The Raman spectrum was measured by a HORIBA/LabRAM HR Evolution spectrophotograph with a 532 nm excitation laser. The cross-sectional HAADF-STEM image and EDS line profiles of the TS were obtained by STEM (FEI Tecnai F20). The SEM image was captured by a FEI Nova 450. And the EBL was performed by the FEI Nova 450 with a Raith B1500A in an ambient atmosphere at room temperature.

**Data availability**

All data supporting this study and its findings are available within the article and its Supplementary Information or from the corresponding author upon reasonable request.

**Code availability**

The codes that support the findings of this study are available from the corresponding author upon reasonable request.

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Additional information
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