Simulation Study of Single-Event Burnout for the 4H-SiC VDMOSFET with N+ Split Source

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Abstract. Silicon Carbide (SiC) power MOSFET is the next generation device in the supply system of spacecraft. However, the current degradation or catastrophic failure of the power device could be induced when a drain voltage exceeds critical condition. In this article, an improved VDMOSFET structure for the Single-Event Burnout (SEB) is demonstrated. The improved power VDMOSFET includes a P+ shielding region at the JFET region. Meanwhile, forming a CSL layer by ion-implantation at the JFET to reduce the specific on-resistance. The device is etched in both sides to form trench and then implanting N-type impurities at the side walls of the trench to form the N+ split source (SDS-VDMOSFET). The 2-D numerical simulator Silvaco Atlas was used to study the SEB performance for the 1.2 kV-rated SiC SDS-VDMOSFET in a high linear energy transfer (LET) value of 0.5 pC/μm. The simulation results show that the improved structure can effectively reduce the peak lattice temperature induced by heavy-ion and increase the SEB threshold voltage compared with the standard VDMOSFET. Furthermore, the improved structure also presents a lower specific on-resistance. As a result, the maximum temperature of the standard VDMOSFET has exceeded 3000 K at a drain voltage of 400 V. However, the maximum temperature of the improved VDMOSFET is only 2090 K at a drain voltage of 800 V.

1. Introduction

Silicon carbide (SiC) power MOSFETs have presented several compelling characteristics, such as, high thermal conductivity, high-power, and high critical breakdown voltage [1-3]. With the continuous development of the aerospace technology, especially for the deep space probe and other extreme conditions, the SiC MOSFETs are significantly suitable. However, many researchers have found that SiC power MOSFETs are susceptible to heavy-ion radiation in the space environment [4-6]. The high-energy heavy-ion can cause serious radiation damage in the SiC MOSFET even at the drain voltages below the breakdown voltage (BV). For example, the catastrophic Single-Event-Burnout (SEB) and the Single-Event Gate Rupture (SEGR) can be induced by the high-energy heavy-ion.

Catastrophic failure has been found to occur at about half the rated BV for the commercial VDMOSFET devices by the heavy-ion irradiation experiments [7-9]. So far, many researches have been carried out for the SiC VDMOSFET to investigate the mechanism of SEB event [5-9]. The most effective and common way to improve the anti-irradiation ability of the SiC MOSFET is adding a buffer layer between the epilayer and substrate to decrease the strong electric field and high impact ionization rate after an ion’s strike. The lattice temperature of the device after a heavy-ion’s impact could also be decreased further by optimizing the buff layer parameters. It has been proved by Lu et al.
[10] that the SEB threshold voltage could be effectively improved by adding an optimized buff layer. But it is inevitable that the on-resistance of the device would also increase.

In this article, a way to improve the SEB performance at high linear energy transfer (LET) value and decrease the specific on-resistance ($R_{on,sp}$) of the device is proposed. In the structure, a $N^+$ split source is proposed to introduce a horizontal electric field to make the distribution of hole current induced by heavy-ion become more uniform that the SEB performance can be improved. In addition, the multi-buffer layers are also added to modulate the strong electric field as mentioned above. Furthermore, the Current spreading Layer (CSL) is added to suppress the $R_{on,sp}$, and the $P^+$ shielding region at the JFET region is used to reduce the electric field of the gate oxide are both considered. As a result, the maximum lattice temperature is simulated at 2090 K with a LET value of 0.5 pC/μm when the drain voltage is 800V.

2. Description of Device Structure and SEB Mechanism
Figure 1(a) shows a cross-sectional view of the 4H-SiC Standard-VDMOSFET, and figure 1(b) shows a schematic cross section of the improved VDMOSFET. The total thickness of the optimized multi-buffer layers (four buffer layers) is 5.2 μm, and the thickness of each buffer layer is equal. The depth of $P$-region and $N^+$ split source is 1.6 and 1.0 μm, respectively. The trench will be filled with the metal to form the source electrode. The doping concentrations of the four buffer layers increase sequentially with the same multiplication factor. The CSL, drift, and substrate regions are all uniformly doped with the concentration of $1.0 \times 10^{17}$, $8.0 \times 10^{15}$, and $5 \times 10^{18}$ cm$^{-3}$. In the $P$- base region, the gauss doping profiles is used and the peak doping concentrations is $3.1 \times 10^{18}$ cm$^{-3}$ with a depth of 0.5 μm. The main parameters are demonstrated in the table 1.

![Figure 1. Cross-sectional view of 1.2-kV SiC power VDMOSFET.](image)

(a) Standard-VDMOSFET (b) SDS-VDMOSFET.

| Structure parameters | Standard-VDMOSFET | SDS-VDMOSFET |
|----------------------|------------------|--------------|
| Drift thickness(μm)  | 10.0             | 8.8          |
| CSL doping concentration(cm$^{-3}$) | --             | $1.0 \times 10^{17}$ |
| $P^+$ shielding doping concentration(cm$^{-3}$) | --             | $1.0 \times 10^{18}$ |
| $N^+$ split source Thickness(μm) | --             | 0.3          |
The fabrication process of the SDS-VDMOSFET is shown in figure 2 (a~h). Firstly, the desired epitaxial wafer is prepared by forming the multiple-buffer layers and drift layer with the chemical vapor deposition. Secondly, the ion implantation is used to form the P- base and the P+ shielding at the JFET region. Afterwards, the N+ Source is formed by the ion implantation. Next, the trench is formed by the etching process. Then, at the bottom and side wall of the trench, the P+ shielding region and N+ split source is obtained by the multiple-ion implantation. Finally, the trenches are filled with metal, and it is also deposited on the surface of the device to form the electrodes.

| N+ split source concentration(cm⁻³) | -- | 1.0×10¹⁸ |
|-------------------------------------|----|----------|
| P- base concentration(cm⁻³)         | -- | 5.0×10¹⁷ |

3. Numerical Simulation Results and Discussion
In this section, the simulation results of the Standard-VDMOSFET and SDS-VDMOSFET are comparatively investigated with a series of photographs and analysis.

3.1. Basic Electric Characteristic

![Figure 3](image-url) **Figure 3.** The breakdown voltage characteristics of structures.

![Figure 4](image-url) **Figure 4.** The ON-state characteristic curves of structures.
Figure 3 shows the BV characteristics of the two structures. The BVs of the Standard-VDMOSFET and SDS-VDMOSFET are 1220 and 1230 V, respectively. The threshold voltages of the two devices show different values of 3.8 and 4.6 V because of the different doping concentration in the P-base regions. However, there is a big gap in their Ron,sp, although the doping profiles in the drift regions are the same. Figure 4 shows the ON-state performance of the two devices. As a result, the Ron,sp of the Standard-VDMOSFET and SDS-VDMOSFET are 3.7 and 2.1 mΩ·cm² at Vgs=15 V.

3.2. SEB Characteristic

The SEB characteristics of the two structures were simulated by using the 2-D simulator Silvaco ATLAS. The simulation is based on some physical models which include the ANALYTIC model, the concentration dependent mobility (CONMOB) model, the parallel electric field dependent mobility (FLDMOB) model. A bandgap narrowing (BGN) model was needed due to the presence of highly doped regions. The recombination models include the SRH model with doping and temperature dependency and the AUGER model. The incomplete ionization model and the Selberherr model were used to calculate the impact ionization rate, as well as the lattice self-heating model (LAT.TEMP) to compute the device temperature.

The heavy ion model is described by (1), the track charge generation rate for a vertical track is the function of the spatial and temporal Gaussian. The parameters used in simulation are list in table 2.

\[
rate(x, y) = \frac{LET}{q\pi\omega_0T_c} \exp\left(-\frac{(x-x_0)^2}{\omega_0^2}\right) \cdot \exp\left(-\frac{(t-T_0)^2}{T_c^2}\right)
\]  

(1)

| LET (pC/μm) | Track Radius ω₀ (μm) | Initial Charge Generation Time T₀ (s) | Temporal Gaussian Function Width T_c (s) | Lateral Ion Striking Position x₀ (μm) |
|------------|-----------------------|--------------------------------------|----------------------------------------|--------------------------------------|
| 0.5        | 0.05                  | 4×10⁻¹²                              | 2×10⁻¹²                                | x₀                                   |

4. SEB Simulation Results and Discussion

4.1. Simulation Results for the Standard-VDMOSFET

In SiC power MOSFETs, the SiC material will directly sublimate rather than melt when the temperature is higher than 2100–2200 K. In order to find the most sensitive position of the Standard-VDMOSFET, as shown in figure 5, we have simulated the SEB characteristics of the device at different positions. At last, we found that the maximum temperature of the device has exceeded 4000 K which locates at the drift/substrate junction. The electric field in the oxide layer also far exceeds the critical value when the heavy-ion strikes in the center of the JFET region, as shown in this figure. This demonstrates that the SEB and SEGR events both occur in the Standard-VDMOSFET at Vds=300 V. So, the most sensitive position is in the P-base area of the Standard-VDMOSFET.
Figure 5. The maximum temperature of Standard-VDMOSFET at different position when $V_{ds}=300$ V LET=0.5 pC/μm.

Figure 6. The impact generation rate distribution at different times. (a) $t=0.1$ns (b) $t=0.5$ns (c) $t=1$ns (d) $t=10$ns.

The impact generation rate of the Standard-MOSFET after the heavy-ion strikes in the JFET region at $V_{ds}=300$ V is also illustrated in figure 6. From the figure, we can see the highest impact generation rate is located in the drift/substrate homogeneous junction due to the strong electric field which could also lead to the self-heating effect to make the device burnout.

4.2. SEB Performance for the SDS-VDMOSFET

The characteristics of a SEB has been studied with the different drain voltage while keeping the gate voltage constant at 0 V. The electric field at the drift/substrate homogeneous junction can be decreased by adding the multi-buffer layers. And the electric field of the oxide can also be reduced by forming the P+ shielding region in the JFET region. In the figure 7, the electric field distribution of the device is transformed to the upper region and gradually decrease. Eventually, the largest electric field is located in the P+ shielding which prevents the gate oxide from failure.

As shown in the figure 8, a part of hole current flows out of the device from the N+ split source region, which can make the distribution of the hole current induced by heavy-ion more uniform to suppress the operation of the parasitic BJT. The presence of the N+ split source region reduces the hole current flowing through the N+ source of the SDS-VDMOSFET and also suppresses the temperature in the N+ source region, as illustrated in the figure 8.
Figure 7. The electric field distribution along the ion track when the $V_{ds}=800$ V and LET=0.5 pC/μm at $x_0=4.5$ μm.

Figure 8. The hole current distribution of the SDS-VDMOSFET.

Figure 9. Lattice temperature distribution of the SDS-VDMOSFET at $V_{ds}=800$ V LET=0.5 pC/μm. (a) ion strikes position $x_0=2.0$ μm (b) ion strikes position $x_0=3.0$ μm.

In figure 9 (a), the maximum temperature of the device is 1962 K when the ion incidences in the source region. In the figure 9 (b), the maximum temperature is 2090 K which locates in the drift/buffer homojunction. The temperature of the electrode contact is only 1128 K at this condition, so it does not have a significant effect on the source contact metal.

5. Conclusion
In this article, the anti-irradiation performance of the 1.2-kV VDMOSFETs with the N+ split source and multi-buffer layers is studied. Numerical simulations are used to illustrate the SEB effect of the device. The final results demonstrate that the lattice temperature of the device could be reduced to 2090 K at $V_{ds}=800$ V with LET=0.5 pC/μm. This method not only increases the SEB threshold voltage, but also suppress the occurrence of the SEGR effect. At the same time, the $R_{on}$ is reduced to 2.1 mΩ·cm² by adding a CSL region. So, the proposed device could effectively reduce the energy loss of the system.
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