Analysis of ZVS Realization with Consideration of Secondary Parasitic Capacitance for High Frequency GaN-based LLC Resonant Converter under DCM Mode

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Abstract. LLC resonant converter can achieve zero voltage switching (ZVS) for primary side devices and zero current switching (ZCS) for secondary side rectifiers while operating in discontinuous conduction mode (DCM). However, the parasitic capacitance significantly affects the ZVS realization of primary side switches for high frequency GaN-based LLC converter. In order to reveal the influence, this paper analyses ZVS transition process with consideration of secondary parasitic capacitance in a high frequency GaN-based LLC resonant converter under DCM mode. Then, an accurate model during ZVS transition is derived. To verify the analysis and the derived model, a 250V rating input and 270V/6.6A rating output GaN-based LLC converter prototype operating at 500 kHz is built. The experimental results are consistent with the theoretical analysis.

1. Introduction
As a Wide Bandgap semiconductor device, Gallium Nitride High Electron Mobility Transistor (GaN transistor) has been widely used in high frequency converters such as CLLC resonant converter, Class Φ2 converter, totem-pole bridgeless PFC converter and LLC resonant converter in recent years owing to its advantages of fast switching speed, low switching loss and parasitic parameters [1-4]. CLLC resonant converter is usually applied in bidirectional on-board charger (OBC), the application of GaN transistors can significantly reduce its size and improve its power density [5]. Similar to CLLC resonant converter, LLC resonant converter can achieve both high frequency and efficiency, and the power level can be further improved by utilizing GaN transistors.

High frequency LLC resonant converter has the advantages of small size, light weight, high power density and easy modulization. However, as the frequency increases, it also faces some issues. Since the loss of traditional magnetic component increases with the increase of frequency, it is difficult to meet the requirement of efficiency. Therefore, many higher efficiency planar magnetic components are designed to address this problem [6, 7]. Compared with Si-based devices, GaN transistors are easier to drive. Its driving voltage is typically about 6V, while the threshold voltage of GaN transistors is also very low (generally around 1.5V), which makes GaN transistors easy to occur false turn-on due to the parasitics. Furthermore, since the reverse conduction of GaN transistors is realized by two-dimensional electron gas (2DEG), it has a higher reverse conduction voltage than that of Si-based devices, which can induce obvious losses [8]. Various solutions have been proposed to improve the gate drive reliability and reduce the reverse conduction loss of GaN transistors [9, 10].
Besides the above problems, the secondary parasitic capacitance cannot be ignored as the frequency increases, because it will affect the realization of the zero-voltage switching (ZVS) for LLC converter [11]. The ZVS is realized during the deadtime. For the primary side, when the upper switch of a bridge arm is turned off, the current will transfer to the lower switch and flow from the source electrode to drain electrode, and the charges stored by the \( C_{oss} \) in the previous switching cycle will be discharged. For the secondary side, the rectifier diodes or synchronous rectifier MOSFETs can realize zero-current switching (ZCS) while operating in discontinuous conduction mode (DCM), thus achieving a higher efficiency [12]. When the deadtime is selected appropriately, complete ZVS for primary GaN transistors can be realized. If the deadtime is set too long or too short, the primary side GaN transistors cannot completely realize ZVS. This paper firstly analyses the operation of high frequency GaN-based LLC resonant converter under DCM mode. Secondly, the time to achieve ZVS transition with consideration of secondary parasitic capacitance is analysed and derived. Finally, simulations and experiments are given to verify accuracy of the analysis.

2. Operation Analysis of high frequency LLC resonant converter under DCM mode
The topology of LLC resonant converter is shown in Figure 1. \( Q_1\sim Q_4 \) are enhancement mode GaN transistors, \( D_1\sim D_4 \) are SiC diodes, \( L_r, L_m \), and \( C_r \) are resonant inductor, magnetizing inductance, and resonant capacitor respectively. \( C_i \) is the input capacitor, \( C_o \) is the output capacitor, \( R_L \) is the load resistance, and the turns ratio of transformer is \( N:1 \).

![Figure 1. Topology of LLC resonant converter.](image1)

![Figure 2. Waveforms for high frequency LLC converter under DCM mode (\( f_i < f_r \)).](image2)
When operating in DCM mode, the key waveforms for high frequency LLC resonant converter are given in Figure 2. Analyses for different stages are given in the following:

a) $t_0~t_1$: ZVS realization stage. $Q_1$-$Q_4$ are turned off at time $t_0$, $Q_1$ and $Q_4$ achieve ZVS transition during this stage;

b) $t_1~t_2$: Deadtime resonance stage. During the deadtime, the primary side completes ZVS transition and re-enters the $L_r$-$C_r$ resonance, meanwhile $D_1$ and $D_4$ at the secondary side are turned on;

c) $t_2~t_3$: $L_r$-$C_r$ resonance stage. $Q_1$ and $Q_4$ are turned on at time $t_2$, the primary side is in $L_r$-$C_r$ resonance state;

d) $t_3~t_4$: Boost stage. $Q_1$ and $Q_4$ are turned on, $L_m$ participates in resonance, the resonant frequency decreases and the resonant current increases. Since the magnetizing inductance is short-circuited by the secondary side, $D_2$ and $D_3$ realizes ZCS;

e) $t_4~t_5$: ZVS realization stage. $Q_1$-$Q_4$ are turned off at time $t_4$, $Q_2$ and $Q_3$ achieve ZVS transition during this stage;

f) $t_5~t_6$: Repeat the process from $t_0$ to $t_5$.

2.1. $L_r$-$C_r$ resonance stage

According to the above analysis, the primary side is in $L_r$-$C_r$ resonance state during $t_1<t_3$. The resonant current during this period is given by

$$i_{L_r}(t) = A_1 \cos[\omega_r(t-t_1)] + A_2 \sin[\omega_r(t-t_1)]$$

(1)

where $\omega_r = \frac{1}{\sqrt{L_rC_r}}$ is the resonant frequency, $A_1$ and $A_2$ are undetermined coefficients. Furthermore, the resonant capacitor voltage is given by

$$V_{C_r}(t) = V_{in} - N V_a + Z_r A_1 \sin[\omega_r(t-t_1)] - Z_r A_2 \cos[\omega_r(t-t_1)]$$

(2)

where $Z_r = \omega_r L_r$. Assume the resonant current at $t_1$ is $I_{L_r1}$, then the coefficients are derived as

$$\begin{cases}
A_1 = I_{L_r1} \\
A_2 = \frac{V_{in} - N V_a - V_{C_r}(t_1)}{Z_r}
\end{cases}$$

(3)

According to Figure 2, the duration from $t_1$ to $t_3$ is given by

$$t_3 - t_1 = \frac{T_r}{2}$$

(4)

where $T_r$ is the cycle of $L_r$-$C_r$ resonance.

Based on (2) and (4), the resonant capacitor voltage at $t_3$ is

$$V_{C_r}(t_3) = 2(V_{in} - N V_a) - V_{C_r}(t_1)$$

(5)

Since the magnetizing inductance voltage is clamped by the secondary output voltage during $t_1<t_3$, the magnetizing current is given by

$$i_{L_m}(t) = -I_{L_m, \text{max}} + \frac{N V_a}{L_m} (t-t_1)$$

(6)

where $I_{L_m, \text{max}}$ is the maximum magnetizing current. Furthermore, the magnetizing current is equal to resonant current at $t_3$. Using the symmetry of the resonant current, the magnetizing current is derived as

$$i_{L_m}(t_3) = -I_{L_m, \text{max}} + \frac{N V_a T_r}{2L_m} = I_{L_r1} = -I_{L_r1}$$

(7)

Based on the power balance, the output current is approximately equal to $N$ times the average value of the resonant current from $t_1$ to $t_3$, (8) can be obtained

$$\frac{2N}{T_r} \int_{t_1}^{t_3} \left[ I_{L_r1} \cos[\omega_r(t-t_1)] + \frac{V_{in} - N V_a - V_{C_r}(t_1)}{Z_r} \sin[\omega_r(t-t_1)] - i_{L_m}(t) \right] dt \approx \frac{V_a}{R_o}$$

(8)

Substituting (6) into (8) yields
\[ \frac{4N[V_m - NV_s - V_C(t_1) + \frac{T_N}{T_s}I_{\text{Lm,max}} - \frac{N^2V_sT_s^2}{4L_mT_s}]}{T_c\omega Z_r} = \frac{V_o}{R_c} \]  

(9)

### 2.2. Boost stage

During \( t_3 < t < t_4 \), the magnetizing inductance of the transformer participates in resonance, and the resonant frequency becomes lower. The resonant current and resonant capacitor voltage during \( t_3 < t < t_4 \) are given by

\[
\begin{align*}
    i_{Lr}(t) &= A_1 \cos(\omega_r(t-t_3)) + A_2 \sin(\omega_r(t-t_3)) \\
    V_C(t) &= V_m + Z_s A_1 \sin(\omega_r(t-t_3)) - Z_r A_2 \cos(\omega_r(t-t_3))
\end{align*}
\]  

(10)

where

\[ \omega_r = \frac{1}{\sqrt{(L_r + L_m)C_r}} \]

and

\[ Z_s = \omega_r(L_r + L_m) \]

Substituting \( t = t_3 \) into (10) gives the coefficients, as shown in (11).

\[
\begin{align*}
    A_1 &= -\frac{V_m - V_C(t_3)}{Z_r} \\
    A_2 &= \frac{-I_{Lr1}}{Z_r}
\end{align*}
\]  

(11)

According to Figure 2, the duration from \( t_3 \) to \( t_4 \) is given by

\[
t_4 - t_3 = \left( \frac{T_c}{2} - t_o \right) - \left[ \frac{T_c}{2} - (t_o - t_{\text{ZVS}}) \right] = \frac{T_c}{2} - \frac{T_c}{2} - t_{\text{ZVS}}
\]  

(12)

where \( t_o = t_3 - t_0 \) is the deadtime and \( t_{\text{ZVS}} = t_4 - t_3 \) is the ZVS realization time. Since the resonant cycle is long and the time duration from \( t_3 \) to \( t_4 \) is relatively short, (12) is approximated as

\[ i_{Lr}(t) \approx -\frac{V_m - V_C(t_3)}{Z_r} \left[ \omega_r(t-t_3) \right] \]  

(13)

Furthermore, the resonant current and resonant capacitor voltage at \( t_4 \) are given by

\[
\begin{align*}
    i_{Lr}(t_4) &= i_{Lr}(t_3) = I_{\text{Lm,max}} = -\frac{V_m - V_C(t_3)}{Z_r} \left[ \omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} - t_{\text{ZVS}} \right) \right] \\
    V_C(t_4) &= V_m - Z_r I_{Lr1} \sin(\omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} - t_{\text{ZVS}} \right)) - [V_m - V_C(t_3)] \cos(\omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} - t_{\text{ZVS}} \right))
\end{align*}
\]  

(14)

### 2.3. ZVS realization stage

During \( t_4 < t < t_5 \), the ZVS realization time is very short due to the small parasitic capacitance of GaN transistor. The resonant capacitor voltage can be considered as unchanged, then resonant capacitor voltage is given by

\[ V_C(t_4) = V_C(t_5) = -V_C(t_3) \]  

(15)

Combining (14) and (15), the resonant capacitor voltage at \( t_1 \) is given by

\[
\begin{align*}
    V_C(t_1) &= -V_m + Z_s I_{Lr1} \sin \left[ \omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} \right) \right] + [V_m - V_C(t_3)] \cos \left[ \omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} \right) \right]
\end{align*}
\]  

(16)

Substituting (5) and (7) into (16) yields

\[
\begin{align*}
    V_m + Z_s \left( \frac{NV_s T_s}{2L_m} - I_{\text{Lm,max}} \right) \sin \left[ \omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} \right) \right] + V_C(t_1) + [2NV_o - V_m + V_C(t_1)] \cos \left[ \omega_r \left( \frac{T_c}{2} - \frac{T_c}{2} \right) \right] = 0
\end{align*}
\]  

(17)

From (9) and (17), the resonant capacitor voltage at \( t_1 \) and maximum resonant current is obtained
3. Analysis of ZVS realization

ZVS is realized during $t_4 < t < t_5$. In this stage, the drain to source voltage of $Q_2$ and $Q_3$ decrease from $V_{in}$ to $V_{sd}$. The charge and discharge state of primary and secondary parasitic capacitance is shown in Figure 3(a), where $C_{oss}$ is the drain to source junction capacitance of $Q_1$-$Q_4$ and $C_j$ is the junction capacitance of $D_1$-$D_4$. Figure 3(b) shows the equivalent circuit of Figure 3(a), where $C_{eq1}$ is the equivalent capacitance of $Q_1$-$Q_4$, $C_{eq2}$ is the equivalent capacitance of $D_1$-$D_4$.

![Figure 3. ZVS realization stage (a) Charge and discharge state of primary and secondary parasitic capacitance (b) Equivalent circuit model](image)

Since the resonant capacitor $C_r$ is much larger than the junction capacitance $C_{oss}$ of GaN transistor, and the duration from $t_4$ to $t_5$ is very short, it can be considered that the voltage across the resonant capacitor $C_r$ is constant at this stage. In addition, since the magnetizing inductance is much larger than the resonant inductance, the magnetizing current can also be considered as constant.

As shown in figure 3(b), $L_r$ resonate with the series equivalent capacitance of $C_{eq1}$ and $C_{eq2}$ during $t_4 < t < t_5$. The resonant current can be derived according to figure 3(b) as (19):

$$i_r(t) = A + B \cos(\omega(t-t_4)) + C \sin(\omega(t-t_4))$$

where $\omega = \frac{1}{\sqrt{C_{eq1}C_{eq2}-L_r}}$ is the resonant frequency in this stage. Through the boundary conditions, $A$, $B$ and $C$ can be derived as follows

$$A = \frac{C_{eq1}}{C_{eq1} + 2C_{eq2}} I_{L_{m\_max}}$$

$$B = I_{L_{m\_max}} - \frac{C_{eq1}}{C_{eq1} + 2C_{eq2}} I_{L_{m\_max}}$$

$$C = \frac{V_{in} - V_{C}(t_4) - NV_o}{\omega L_r}$$

Since $\omega(t-t_4)$ is very small, (20) can be further approximated as

$$i_r(t) \approx \frac{C_{eq1}}{C_{eq1} + 2C_{eq2}} I_{L_{m\_max}} + \frac{2C_{eq2}}{C_{eq1} + 2C_{eq2}} I_{L_{m\_max}} \cos(\omega_r(t-t_4))$$

The $V_{ds}$ of $Q_2$ and $Q_3$ can be calculated in the following:
\[ V_{ds}(t) = V_{in} - \frac{1}{C_{eq}} \int i_{Lr}(t) \, dt \]  

(22)

From the dc term in (19), it can be seen that the magnetizing current is shared by the primary side and secondary side for charging/discharging during ZVS transition. Besides, from the \( \omega \) in (19), it shows that \( L_r \) will resonate with all the capacitances reflected to the primary side during ZVS transition. From (22), it can be seen that the ZVS realization time \( t_{ZVS} \) is the time required for \( V_{ds} \) to drop from \( v_{in} \) to 0.

4. Simulation and experimental verification

According to the analyses in the previous sections, a GaN-based LLC converter prototype with 250V rating input and 270V/6.6A rating output is built to verify the analysis of ZVS realization with consideration of secondary parasitic capacitance, as shown in figure 4. The key parameters of the prototype are given in Table 1.

![GaN-based high frequency LLC converter prototype](image)

Figure 4. GaN-based high frequency LLC converter prototype

| Table 1. Main specifications of the prototype |
|---------------------------------------------|
| Resonant frequency                           | 660 kHz |
| Switching frequency                          | 500 kHz |
| Primary GaN transistors \( Q_1 \)–\( Q_4 \)  | GS66508T|
| Secondary diodes                             | C3D16060D|
| Transformer                                  | Turn ratio: 5:5 |
|                                              | \( L_m \): 11.32\( \mu \)H; \( L_R \): 0.98\( \mu \)H |
| Resonant \( L_r \) and \( C_r \)             | 0.98\( \mu \)H and 60nF |
| Parasitic capacitance                        | GS66508T: 88pF |
|                                              | C3D165065D: 32pF |

Since the secondary side rectifier diodes under DCM mode can achieve ZCS, in engineering practice, the LLC converter parameters are often designed to work in this mode. According to the analysis of Section 2 and Section 3, the variation of \( V_{ds} \) with time under different maximum magnetizing currents under DCM mode is shown in Figure 5. It can be seen from Figure 5 that under different maximum magnetizing currents, as the maximum magnetizing current decreases, the ZVS realization time increases gradually. The maximum magnetizing current in the LLC converter is influenced by the load, so the ZVS realization time varies with the load.
Figure 5. Variation of $V_{ds}$ with time under different maximum magnetizing currents.

Figure 6. Variation of $V_{ds}$ with time under different input voltages when maximum magnetizing current $I_{Lm_{max}}=5A$.

Figure 6 shows the variation of $V_{ds}$ with time at different input voltages under DCM mode. It can be seen that as the input voltage increases, the time to achieve ZVS is gradually increasing, which implies that the ZVS realization time changes continuously with input voltage and load.

In order to verify the previous analysis, the LLC converter with different input voltages and output powers is presented. Figure 7 and figure 8 show the LLC converter working under DCM (500 kHz) mode with the deadtime of 90ns. The experimental waveforms are consistent with the analysis in section 2. The experimental results show that the ZVS is fully realized for both conditions. The $t_{ZVS}$ for 250V input and 270V/6.6A output is shorter than that of 200V input and 220V/5.3A output because load increases and it has a higher maximum magnetizing current. Compared with figure 5 and figure 6, the time to achieve ZVS in the experiment is longer than that of theoretical analysis. This is because the parasitic capacitance varies nonlinearly with the voltage in practice, the equivalent parasitic capacitance is larger than that used in the theoretical analysis.

5. Conclusion
This paper examines the effect of secondary parasitic capacitance on the ZVS realization in high frequency GaN-based LLC resonant converter under DCM mode. With consideration of secondary parasitic capacitance, the ZVS realization is analysed and derived. A 250V rating input and 270V/6.6A rating output GaN-based LLC converter prototype operating at 500 kHz is built to verify the theoretical analysis.
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