Nonideality-Aware Training for Accurate and Robust
Low-Power Memristive Neural Networks

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Abstract

Recent years have seen a rapid rise of artificial neural networks being employed in a number of cognitive tasks. The ever-increasing computing requirements of these structures have contributed to a desire for novel technologies and paradigms, including memristor-based hardware accelerators. Solutions based on memristive crossbars and analog data processing promise to improve the overall energy efficiency. However, memristor nonidealities can lead to the degradation of neural network accuracy, while the attempts to mitigate these negative effects often introduce design trade-offs, such as those between power and reliability. In this work, we design nonideality-aware training of memristor-based neural networks capable of dealing with the most common device nonidealities. We demonstrate the feasibility of using high-resistance devices that exhibit high \( I-V \) nonlinearity—by analyzing experimental data and employing nonideality-aware training, we estimate that the energy efficiency of memristive vector-matrix multipliers is improved by three orders of magnitude (555 GOPs \( \rightarrow \) to 474 TOPs \( \rightarrow \) ) while maintaining similar accuracy. We show that associating the parameters of neural networks with individual memristors allows to bias these devices towards less conductive states through regularization of the corresponding optimization problem, while modifying the validation procedure leads to more reliable estimates of performance. We demonstrate the universality and robustness of our approach when dealing with a wide range of nonidealities.
1 Introduction

Artificial neural networks (ANNs) are now routinely used in machine learning tasks ranging from text generation [1] to autonomous driving [2]. However, rapidly increasing number of parameters in modern ANNs is making them time- and power-consuming during both training [3] and inference [4] stages. This makes it challenging to apply machine learning approaches in environments where resources are tightly constrained [5, 6].

One of the proposed solutions to improve the efficiency of ANNs has been to adopt different computer architectures. The need to transfer data between memory and computing units in the von Neumann architecture is the main bottleneck in modern computers [7]; this is especially evident in machine learning where large amounts of data are utilized. In this specific case, an alternative can be memristor-based ANNs, or memristive neural networks (MNNs). With this approach, memristive crossbar arrays are used to physically compute vector-matrix products which are one of the most fundamental operations in ANNs [8, 9]. This is done without the need to constantly move large amounts of data: matrix entries are encoded into memristor conductances, vector entries—into applied voltages, and the result of the operation is extracted from the output currents produced according to Ohm’s law and Kirchhoff’s current law [8].

Memristors—when used and programmed as analog devices—can encode values at much higher density, but at a cost of lower precision. A number of nonidealities may prevent from accurately programming device conductances or may cause deviations from intended electrical behavior. Such nonidealities include stuck devices, device-to-device (D2D) and cycle-to-cycle variability, drift in resistance states, line resistance, I-V nonlinearity, and others [10].

Potential solutions do exist but many of them introduce a number of trade-offs. For example, to ensure more linear I-V characteristics, one may use low-resistance devices [11]; however, this results in higher power consumption. Alternatively, the effects of I-V nonlinearities may be minimized by utilizing pulse-width modulation [12], but that comes at a cost of increased clock cycles for each encoded input [13].

Other techniques of dealing with memristor nonidealities include

- in-situ (re)training to recover from the effects of the nonidealities [14–18]
- modifying device structure [19–21]
- using additional circuitry [22, 23]

However, many of these approaches are technology-specific and thus difficult to apply to different types of devices.

When optimizing the performance of memristive systems (as opposed to individual devices), software approaches may be preferable because they are usually technology-agnostic. For general applications, mapping or redundancy schemes can be used to mitigate the effects of faulty-devices [24] or line resistance [25]. In the specific context of MNNs, multiple smaller nonideal networks may replace a large one and increase the accuracy in this way [26]. Alternatively, modifying ex-situ training has been proposed: altering the cost function [27] or injecting noise into the synaptic weights [28] can make MNNs more robust to the effects of nonidealities.

Memristor-oriented ex-situ training is indeed a very promising method of making MNNs feasible. However, it has been applied by considering only a limited number of nonidealities, while the robustness of this technique is not well understood. In this work, we propose a number of improvements to memristive ex-situ training that are summarized in Figure 1.

Firstly, our novel training technique addresses the problem of nonlinearity. Deviations from the linear relationship between inputs and outputs in crossbar arrays are a major obstacle, however none of the aforementioned methods directly address this issue. Although existing works often take conductance deviations into account during ex-situ training, crossbar arrays are still usually modeled as structures computing a product of a vector of voltages and a matrix of conductances. To reflect non-ohmic behavior of memristive devices (illustrated in Figure 1) during training, we propose incorporating nonlinearities into the node functions of MNNs. Our aim is to embrace memristor nonlinearity, so that the network can learn to be robust toward this nonideality—or even take advantage of it—during training based on stochastic gradient descent. Existing works attempting to take device variations into account during ex-situ training often result in potentially lower training accuracy [29]. Depending on the nature of the nonideality that MNNs are trained on, our method could potentially perform even better than conventional ANNs. For example, if nonlinear response of the device is sufficiently consistent, nonlinearities may increase the network capacity [30].

We also show how to improve nonideality-aware training by exposing conductances to the training process in a more direct way. By constraining MNN weights to be non-negative, they can be related to conductances in a linear way. This allows to

- minimize the effects of nonidealities in cases
their severity is dependent on the conductance values of the memristors

- employ regularization as a high-level tool for controlling power consumption of MNNs

Finally, we propose improving validation techniques applied during the training of MNNs. Most memristive nonidealities are stochastic in nature, therefore computing validation metrics only once at specified checkpoints may provide unreliable estimates of neural network performance, as illustrated in Figure 1. We propose computing validation metrics multiple times and using an aggregate value (like the median) to determine which version of the MNN to save for inference.

In this work, we explore how to make nonideality-aware training more effective. We employ experimental data from a SiO$_x$ memristor device and a 128 $\times$ 64 Ta/HfO$_2$ memristor crossbar array, and consider multiple nonidealities: $I$-$V$ nonlinearity, stuck devices, and D2D variability. We give special focus to $I$-$V$ nonlinearity because existing works often prefer low-resistance devices as they exhibit more linear $I$-$V$ behavior. We show that our proposed training function enables the use of the more power-efficient high-resistance memristors by minimizing the accuracy loss due to high nonlinearity and variability that typically manifest themselves in high-resistance devices [31]. We demonstrate how the proposed mapping between nonnegative weights and memristor conductances enables further power savings through $\ell_1$ regularization. We additionally show how MNN validation during training may be improved by taking the stochastic nature of many of the nonidealities into account. Finally, to assess the robustness of nonideality-aware training, we expose MNNs to different setups than they were trained for—we find that the networks employing this technique are much more robust than the networks trained using the previous, more conventional approaches.

2 Design

2.1 Nonlinearity-Aware Training

The main focus of this work is the design of a novel ex-situ MNN training scheme that could handle nonidealities characterized by the nonlinear relationship between inputs and outputs. Nonidealities like stuck devices, programming inaccuracies or random telegraph noise (RTN) can typically be represented with a change in conductance alone. They are thus more straightforward to take into consideration during ex-situ training because one can inject noise into the conductances to represent their effect. We refer to these nonidealities as linearity preserving. On the other hand, nonidealities like $I$-$V$ nonlinearity or
line resistance cannot be represented by simply disturbing the conductances. We refer to such nonidealities as **linearity nonpreserving**. In this work, we redefine the output operations of the synaptic layers to take the effect of linearity-nonpreserving nonidealities into account. To the best of our knowledge, this is the first time these nonidealities are addressed during ex-situ training.

Existing works usually model memristor crossbars as structures computing linear dot products, while only activation functions are assumed to introduce nonlinearity. Specifically, outputs \( y_j \in \mathbf{y} \in \mathbb{R}^{1 \times N} \) are calculated using inputs \( x_i \in \mathbf{x} \in \mathbb{R}^{1 \times M} \), weights \( w_{ij} \in \mathbf{w} \in \mathbb{R}^{M \times N} \), and a nonlinear activation function \( f \) as shown in Equation (1). During inference, \( \mathbf{x}, \mathbf{w} \) and \( \mathbf{y} \) are then mapped onto and from voltages, conductances and currents, respectively. However, this creates a discrepancy between the linear dot-product training nodes and memristor nonidealities that deviate from ohmic device behavior.

\[
y_j = f \left( \sum_{i=1}^{M} x_i w_{ij} \right) \tag{1}
\]

Therefore, we suggest modifying the output operation of the synaptic layers to reflect the nature of linearity-nonpreserving nonidealities. Specifically, in cases where the nonlinearity is limited to individual devices (i.e. where devices experience \( I-V \) nonlinearity), we propose replacing the approach in Equation (1) with the approach in Equation (2). That is, the activation function is unchanged but the product is replaced with a nonlinear function \( g \) which captures memristors’ non-ohmic \( I-V \) behavior.

\[
y_j = f \left( \sum_{i=1}^{M} g(x_i, w_{ij}) \right) \tag{2}
\]

The exact choice of \( g \) will depend on

- the mapping scheme, examples of which are explored in Section 2.2
- non-ohmic behavior model that might typically be determined by the devices used; in Section 2.4, we present one possibility motivated by experimental device data

### 2.2 Modified Weight Implementation

As mentioned previously, synaptic weights of MNNs are typically implemented using conductances of memristive devices. While weights can usually take any real value, conductances are nonnegative—this presents design challenges. In this work, we propose training double the number of weights\(^1\), but constrain them to be nonnegative and associate them with individual devices. This approach creates a more natural mapping between neural network parameters and conductances, as well as enables weight regularization to act as a method for decreasing the power consumption.

#### 2.2.1 Conventional approaches

In typical MNN implementations, both inputs \( \mathbf{x} \in \mathbf{x} \) and outputs \( \mathbf{y} \in \mathbf{y} \) are mapped onto voltages \( V \) and from currents \( I \), respectively, in a proportional way using scaling factors \( k_V \) and \( k_I \), as shown in Equation (3).

\[
\begin{align*}
V &= k_V x \
\end{align*}
\]

\[
\begin{align*}
y &= \frac{I}{k_I} \quad \text{where } k_I = k_V k_G \\
\end{align*}
\]

where \( k_G \) is the conductance scaling factor typically made equal to \( \frac{G_{on} - G_{off}}{\max(|\mathbf{w}|)} \) and \( k_V \) is determined before training.

To encode both positive and negative weights, pairs of conductances are employed. Conductances \( G_+ \) and \( G_- \) are introduced into “positive” and “negative” bit lines of crossbar arrays, where the output currents of the latter are subtracted from the output currents of the former; this is referred to as **differential pair architecture**. Each weight is typically made proportional to the difference of \( G_+ \) and \( G_- \) (with \( G_0 \) acting as the constant of proportionality) which enables to encode any real number within a finite interval. However, infinite conductance combinations will produce the same difference [32], thus the network designer may have to make an arbitrary choice of how to perform this mapping. For example, to encode weights \( w \in \mathbf{w} \), the two conductances may be picked symmetrically around the average value [32], as shown in Equation 4.

\[
G_{\pm} = G_{\text{avg}} \pm \frac{k_G w}{2} \tag{4}
\]

where \( G_{\text{avg}} = \frac{G_{off} + G_{on}}{2} \).

Although there might be advantages to using the mapping scheme like the one in Equation (4)\(^2\), the choice of mapping could be explicitly tied to certain objectives. For example, [22] points out that differential pair architecture with aware mapping can be advantageous for mitigating the effects of stuck devices. Alternatively, a mapping scheme which optimizes some metric (like power consumption) may be employed. Indeed, such a scheme is used

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\(^1\)The number of memristive devices remains the same as with conventional weight implementation schemes.

\(^2\)An argument could be made, for example, that such a mapping scheme would produce very few conductances with values near \( G_{off} \) or \( G_{on} \) that may be more difficult to achieve in real devices.
throughout this work for mapping the weights of conventionally trained ANNs onto conductances; we minimize power consumption by ensuring that at least one device in the pair is set to $G_{\text{off}}$, as demonstrated in Equation (5).

$$
G_+ = G_{\text{off}} + \max \{0, k_G w\}
$$

$$
G_- = G_{\text{off}} - \min \{0, k_G w\}
$$

(5)

However, choosing the optimal scheme manually is a low-level approach that requires understanding the physical characteristics of MNNs. Thus, even if training is done ex situ, network designer has to make choices about not only the conventional training hyperparameters (like learning rate), but also how the system will be implemented physically because that will affect MNN performance. We see this as an additional obstacle to making memristive implementations of ANNs feasible in the real world.

### 2.2.2 Our approach—double weights

In this work, instead of tweaking the mapping function, we decided to change the characteristics of the weights that are being trained. Specifically, we train two sets of nonnegative weights, $w^+_i \in w_+ \in \mathbb{R}_{\geq 0}^{M \times N}$ and $w^-_i \in w_- \in \mathbb{R}_{\geq 0}^{M \times N}$, that we refer to as double weights; similar approach has been explored in [33]. We map double weights onto conductances in the aforementioned “positive” and “negative” bit lines, respectively. Although all the weight parameters are nonnegative, the negative contribution of $i^{th}$ input on $j^{th}$ output can still be encoded because of the differential pair architecture in the physical system. Only the nonlinearity-aware ex-situ training function in Equation (2) has to be adjusted leading to the form in Equation (6).

$$y_j = f \left( \sum_{i=1}^{M} g \left( x_i, w^+_i \right) - g \left( x_i, w^-_i \right) \right)
$$

(6)

The adoption of double weights allows to relate every weight in $w \equiv \left[ w_+ \ w_- \right]$ to the corresponding conductance in the same way, i.e. $w_\pm \in \left[ 0, \max(w) \right]$ are linearly mapped onto $G_\pm \in \left[ G_{\text{off}}, G_{\text{on}} \right]$, as shown in Equation (7).

$$G_\pm = k_G w_\pm + G_{\text{off}}
$$

(7)

A clear advantage of our approach is that double weights allow for more direct optimization of MNN behavior. Exposing raw device characteristics—i.e. conductances—to the training algorithm, enables it to select the combination that has both the optimal performance (as defined by some metric like loss) and high robustness. For example, if a certain nonideality manifests itself to a greater degree at low conductances, the training algorithm would be able to push double weight pairs (and by extension, conductances) towards higher values. Because of the differential pair architecture setting $G_+$ and $G_-$ to 1.0 mS and 2.0 mS, respectively, will—at least in the case of linearity-preserving nonidealities—have the same effect as setting them to 3.0 mS and 4.0 mS, respectively. Therefore, with double weights, the training algorithm should be able to choose conductance combinations that minimize the negative influence of nonidealities.

Additionally, double weights allow regularization to act as a high-level tool for controlling the importance of power consumption. We propose training with the $\ell_1$ sparsification regularizer [34] which can not only improve training\(^3\), but also promote lower conductances because they are linearly related to weight parameters, as demonstrated in Equation (7). During backward propagation, the regularizer influences training loss, inducing conductance pairs to descend towards $G_{\text{off}}$. Instead of manually tweaking the mapping function, network designer can decide to what extent energy efficiency should be prioritized by simply adjusting, say, regularization factor in $\ell_1$ regularization. This can be incorporated into typical hyperparameter tuning process that is performed before deploying ANNs in practise.

### 2.3 Modified Validation

We also propose a modified model validation scheme more fit for MNNs. To determine when to stop the training (or which version of the network to use when the training takes a predetermined set of epochs), a validation dataset is commonly employed—a metric (like error or loss) is computed for this dataset at certain epochs and is used for picking the optimal version of the network [35]. However, many of memristor nonidealities are at least partly stochastic in nature, thus, say, validation accuracy at any given epoch may not be entirely representative of the model’s quality purely due to random chance. Because of this, we suggest computing the validation metric multiple times and using an aggregated value for higher reliability. Choices can be made about

- aggregate value that is used
- how frequently validation is performed
- how many times validation metric is computed at each checkpoint

In the simulations of this work, we computed validation error 20 times every 20 epochs and saved the model when-

\(^3\)This may manifest itself as avoiding overfitting, for example.
ever the median validation error decreased.

2.4 Nonidealities

In this work, we explore a wide range of memristor nonidealities and utilize experimental data. We use two different memristor technologies—SiO$_2$- and Ta/HfO$_2$-based resistive random-access memory (RRAM). More details on the two technologies can be found in Section 5 and our previous publications [10, 26].

2.4.1 I-V nonlinearity

In the context of memristive applications, we may define perfectly ohmic devices as those for which the ratio of current $I$ to voltage $V$ is always constant. In memristors, deviations from this behavior have usually been characterized by considering a pair of points on the I-V curve [36, 37]. For example, a nonlinearity parameter $\gamma$ may be defined by introducing reference voltage $V_{\text{ref}}$ [37], as shown in Equation (8).

$$\gamma \equiv \frac{h(2V_{\text{ref}})}{h(V_{\text{ref}})} \text{ where } I = h(V)$$ (8)

To construct an I-V curve from a given $\gamma$, one may assume that the equality in Equation (8) holds for all $V$, not just $V_{\text{ref}}$. This would produce a relationship between current and voltage shown in Equation (9).

$$I = V_{\text{ref}}G \left( \frac{V}{V_{\text{ref}}} \right)^{\log_2 \gamma}$$ (9)

In Equation (9), $G$ is the conductance parameter. It has a particular meaning in the context of $V_{\text{ref}}$—at this voltage the device produces the expected (ohmic) amount of current equal to $V_{\text{ref}}G$.

Experimental data from a SiO$_2$ RRAM device were used to extract nonlinearity parameters $\gamma$. SiO$_2$ devices can undergo resistance switching—typical I-V switching curve is shown in Figure S1 in the Supporting Information, while a more detailed analysis of resistance switching performance can be found in our previous study [31]. For the purposes of this work, to achieve a wide range of resistance states and to analyze I-V nonlinearity, incremental positive sweeps were used to gradually reset the device from the low-resistance state (LRS) to the high-resistance state (HRS). I-V curves of two subsets of all achieved states are shown in Figures 2a,b. Low-resistance discrete states (in Figure 2a) exhibit more linear behaviour and experience little variability in nonlinearity. On the other hand, high-resistance states (in Figure 2b) are more nonlinear and the nonlinearity is less predictable. This is supported by the numerical summary in Table 1.

| Figure | $R_{\text{on}}$ (Ω) | $R_{\text{off}}$ (Ω) | $m_\gamma$ | $s_\gamma$ |
|--------|---------------------|---------------------|-------------|-------------|
| 2a     | 284.6               | 1003                | 2.132       | 0.095       |
| 2b     | 366 200             | 1295 000            | 2.989       | 0.369       |

Table 1: Parameter summary of I-V curves in Figure 2. $R_{\text{on}}$ is the lowest resistance at 0.25 V of any curve, while $R_{\text{off}}$ if the highest. $m_\gamma$ is the mean of nonlinearity parameters of the curves, while $s_\gamma$ is the (sample) standard deviation.

To test the effects of I-V nonlinearity, we use two different resistance ranges from the SiO$_2$ RRAM device:

- low-resistance (and low-nonlinearity) device range using data from Figure 2a
- high-resistance (and high-nonlinearity) device range using data from Figure 2b

$V_{\text{ref}}$ from Equation (8) was set to 0.25 V (i.e. half of the minimum switching voltage). In each case, the devices could be set to any conductance between $G_{\text{off}} \equiv 1/R_{\text{off}}$ and $G_{\text{on}} \equiv 1/R_{\text{on}}$ (see Table 1). The states for the two groups were picked so that $G_{\text{on}}/G_{\text{off}}$ ratio for high-resistance devices would be slightly larger—this would ensure that possibly higher error rate in this group would be due to nonlinearity and its variability, and not due to limited dynamic range.

To ensure more robust modelling, we considered uncertainty in the amount of nonlinearity each device experiences. Although there is a general trend for high-resistance states to be more nonlinear, the exact amount of nonlinearity at any given resistance state may be difficult to predict, as suggested by the variability of the I-V curves shown in the experimental data in Figure 2b. Therefore, for each device in either of the groups, nonlinearity parameter $\gamma$ was drawn from a truncated normal distribution$^4$ with mean$^5$ $m_\gamma$ and standard deviation $s_\gamma$ (see Table 1). This also allowed to test whether nonideality-aware training works even when there is uncertainty in the device behavior in general.

Linearity-nonpreserving nonidealities like I-V nonlinearity cannot be simulated using conventional noise injection methods that simply disturb the conductance values. Instead, a forward propagation function must be defined reflecting the nonlinear relationship between inputs and outputs. In our proposed training function in Equation (6), we incorporate the aforementioned I-V nonlinearity into the function $g$ by combining Equations (3), (7)

$^4$The distribution was truncated for $\gamma$ values of less than 2 to ensure realistic device behavior and numerical stability of the simulations.

$^5$Both mean and standard deviation refer to the underlying normal distribution prior to truncation.
and (9) (using $k_V = 2V_{ref}$ because of the definition in Equation (8)) leading to the form in Equation (10) which we implement using TensorFlow.

$$g(x, w_{\pm}) = \frac{(k_G w_{\pm} + G_{off}) \times (2x)^{k_G \gamma_{\pm}}}{2k_G}$$

(10)

2.4.2 Stuck devices

Additionally, we explore linearity-preserving nonidealities that can be simulated using noise injection into the conductances. One of such nonidealities is devices stuck in a particular state which is a very common issue in memristors. The effect of stuck devices can be explored in isolation, but it also easily lends itself to being simulated along other nonidealities thus allowing to investigate the effectiveness of nonideality-aware training in more complex scenarios. In the modeling of this nonideality, we consider both real experimental data (where we draw the state in which devices may get stuck from a random distribution) and a simplified model (where we assume devices can get stuck in only one state).

Data from $128 \times 64$ Ta/HfO$_2$ memristor crossbar array
were analyzed for the purposes of modeling stuck devices’ behavior. Figure 2c shows 11 potentiating and depression cycles (each consisting of a 100 voltage pulses) for a fraction of the devices. By considering the minimum and maximum conductance values achieved by each of the 8192 devices over 11 cycles, $G_{\text{off}}$ and $G_{\text{on}}$ were chosen as the median of these minimum and maximum values, respectively. Devices whose maximum range was less than the median range (where median range had been defined as $G_{\text{on}} - G_{\text{off}}$) were classified as “stuck”.

Stuck devices were simulated using a probabilistic model. Using the aforementioned stuck devices’ definition, 10.1% of the devices were classified as such. To simplify modeling, these devices were simulated to be fully stuck, meaning their conductance could not be changed even by a small amount\(^6\). The average values of all stuck devices are denoted by markers on the $y$ axis of Figure 2d. The probability density function of these average values was constructed using kernel density estimation with truncated normal distributions. Scott’s rule \cite{38} was used for bandwidth estimation, while mirror reflections of the distributions were employed to correct for bias at the 0S clipping boundary\(^7\). When simulating the effect of the nonideality, each device could be set to any conductance state between $G_{\text{off}}$ and $G_{\text{on}}$; however, every device also had a 10.1% probability of getting stuck. When a device was classified as stuck, its conductance would be drawn from the probability distribution constructed using kernel density estimation in Figure 2d.

Additionally, a simple model of devices getting stuck in $G_{\text{off}}$ or $G_{\text{on}}$ was considered. This allowed to combine nonidealities together, specifically with SiO$_x$ $I$-$V$ nonlinearities. For both states, devices were simulated to have 5% probability of getting stuck. As with experimental stuck devices’ model, this was simulated as noise injection into the conductances. Both models of stuck device behavior were used to test the robustness of nonideality-aware training.

### 2.4.3 Device-to-device variability

We also consider D2D variability arising from inaccuracies during device programming. During mapping onto conductances, one may end up with different values than intended; in some memristors, these (resistance) deviations are modeled using lognormal distribution \cite{39}. As with stuck devices, this can be incorporated into training by disturbing the values in each iteration—in this case, by drawing from random lognormal distribution. We use this nonideality to explore

1. double weights (see Section 3.4)
2. memristive validation (see Section 3.5)

For the lognormal modeling, we linearly interpolate the standard deviation of the natural logarithm of resistances from the following values meant to represent different device behaviors:

- 0.25 for $R_{\text{off}}$ and $R_{\text{on}}$ (more uniform D2D variability)
- 0.5 for $R_{\text{off}}$ and 0.05 for $R_{\text{on}}$ (less uniform D2D variability)
- 0.5 for $R_{\text{off}}$ and $R_{\text{on}}$ (high-magnitude D2D variability)

### 3 Results and Discussion

#### 3.1 Nature of Training

Figure 3 contains training curves for MNNs trained on MNIST dataset and exposed to $I$-$V$ nonlinearities. Although not used to affect any aspect of the training process, error curves for the test subset\(^8\) are included as well. Testing on nonideal configuration during training can help understand the differences between standard and nonideality-aware training.

Figures 3a–c explore the effect of low $I$-$V$ nonlinearity. In Figure 3a, the validation curve (which is computed assuming digital implementation of the ANN) is closely coupled with the test curve (which assumes that nonideal effects are present)—this suggests negligible effect of low $I$-$V$ nonlinearity. Consequently, nonideality-aware training produces similar results on the test set both without (Figure 3b) and with (Figure 3c) regularization.

Figures 3d–f explore the effect of high $I$-$V$ nonlinearity. In Figure 3d, where the results of standard training are presented, we notice that validation and test curves are detached from one another. Not only that, but the global minimum of the test curve occurs rather early in the training, while the validation error keeps decreasing. This indicates that without taking nonidealities into account during training, a highly suboptimal version of the ANN may be chosen for inference stage with nonidealities. Nonideality-aware training without (Figure 3b) and with (Figure 3c) regularization is much more effective—the validation and test curves are closely coupled together and the test error decreases to lower values.

\(^6\)This assumption overestimates the effect of stuck devices, not underestimates it.

\(^7\)To ensure numerical stability, mirror reflections were only included if the area under the curve of the underlying normal distribution below 0S was more than $10^{-8}$

\(^8\)Test set errors at training checkpoints were computed in the same way as memristive validation curves, see Section 2.3.
3.2 Performance Improvement

Inference results for \(I-V\) nonlinearity simulations are summarized in Figure 4. Because the simulated memristors are nonlinear, power consumption was computed using \(P = IV\), instead of \(P = I^2R\), for each of the individual devices. Although, apart from crossbar arrays, MNN implementations require additional circuitry, [40] suggest power consumption due to passive elements dominates in the \(\mu\)S range and above (i.e. the conductance range of the device investigated in this work); only at lower conductances does the relative impact of other energy components become significant.

Box plots representing low-resistance (and, by extension, low-nonlinearity) devices are presented on the right side of Figure 4. With such devices, nonideality-aware training without regularization achieves median error of 4.4%. This is comparable to the error of (digital) ANNs of the same size trained using standard procedure—it is indicative of the small effect of low \(I-V\) nonlinearity. However, regularization not only decreases the power consumption by more than half, but also helps achieve median

![Figure 3: Training results for standard and nonideality-aware schemes when exposed to \(I-V\) nonlinearities. a–c) low \(I-V\) nonlinearity (data from Figure 2a), d–f) high \(I-V\) nonlinearity (data from Figure 2b); a, d) standard training (same training and validation curves), b, e) nonideality-aware training, c, f) nonideality-aware training with regularization. The panels show curves for one of five sets of trained networks. Networks were trained on MNIST dataset. Where error was computed multiple times, the curves show the median value, as well as the region bounded by the minimum and maximum values.

![Figure 4: Inference results of using nonideality-aware training to deal with \(I-V\) nonlinearities. The three box plots on the right refer to MNNs that used data from Figure 2a, and the three on the left—to MNNs that used data from Figure 2b. Networks were trained on MNIST dataset. The variability in power consumption for the data points of each group is small thus the average power consumption is used for the horizontal position of each box plot.](image-url)
error rate of 4.1%.

As shown on the left side of Figure 4, MNNs implemented using high-resistance devices achieve three orders of magnitude lower power consumption. However, MNNs trained using the standard procedure have median error of 11.7%. Adjusted training results in much lower error rate, while maintaining low power consumption (compared to low-nonlinearity devices). In the non-regularized case, the median error is 5.7%, and in regularized MNNs it is 4.8%. Thus, nonideality-aware training makes it feasible to use orders of magnitude more power-efficient high-resistance devices while maintaining error rates similar to those achieved with low-resistance devices.

One may also compare estimated absolute energy efficiency in both cases. By assuming the values used in [41]—read pulses of 50 ns, and 2 operations per synaptic weight (multiplication and accumulation)—one can calculate energy efficiency in OPs−1W−1 using Equation (11).

\[
\text{energy efficiency} = \frac{2 \times n}{50 \times 10^{-9} \times P_{\text{avg}}} \quad (11)
\]

where \(n\) is the number of synaptic weights and \(P_{\text{avg}}\) is the average power consumption.

Using these assumptions, standard training using low-resistance devices achieves energy efficiency of 555 GOPs−1W−1, while nonideality-aware training using high-resistance devices achieves energy efficiency of 256 TOPs−1W−1 in the nonregularized case and of 474 TOPs−1W−1 in the regularized case. As explained earlier, these estimates incorporate power consumption only on crossbar arrays.

### 3.3 More Complex Architectures and Datasets

To understand how well nonideality-aware training performs on more complex tasks, we employed CIFAR-10 dataset. For this, we trained convolutional neural networks (CNNs) assuming that their convolutional layers would be implemented digitally, and their fully connected layers—using memristive crossbar arrays suffering from high \(I-V\) nonlinearity. Standard training is explored in Figure 5a, and nonideality-aware training—in Figure 5b. As with MNNs trained on MNIST, there is a much greater coupling between validation and test curves when nonidealities are taken into account. As shown in Figure 5c, nonideality-aware approach reduces the median inference error from 26.1% to 21.3%.

### 3.4 Importance of Weight Implementation

Double weights can be advantageous because they expose conductances to the training process in a more direct way. To investigate the utility of this modified weight implementation, we utilized lognormal D2D variability of two kinds:

1. more uniform variability where the relative magnitude of deviations is the same throughout \([G_{\text{off}}, G_{\text{on}}]\)
2. less uniform variability where the relative magnitude of deviations is much greater near \(G_{\text{off}}\) compared to \(G_{\text{on}}\)—similar to what is experienced in real devices when trying to program them [39]
Figure 6: **Comparison of weight implementations.** Conductance distributions in the first synaptic layer of a memristive neural network that deals with more uniform device-to-device variability and utilizes a) conventional weights mapped symmetrically around average conductance, b) conventional weights mapped onto devices by preferring lowest total conductance, c) double weights, d) double weights with regularization; e–h) corresponding conductance distributions for a memristive neural network dealing with less uniform device-to-device variability. Scatter plots contain conductance data from 10% of the devices for one of five sets of networks. Inference error for different weight implementations of memristive neural networks that deal with i) more and j) less uniform device-to-device variability, where the box plot colors correspond to different weight implementations in a–d and e–h, respectively.

This allowed to

1. evaluate the performance of double weight implementation when the severity of nonideality does not depend on the conductance value
2. test whether double weight implementation would outperform standard weights when exposed to non-idealities whose severity depends on the conductance value

Both standard weights with different mapping schemes and double weights without and with regularization are investigated in Figure 6.

Firstly, we consider weight implementations in the context of D2D variability with relatively high uniformity across the conductance range. Figures 6a,b show conduc-
tances resulting from mapping conventional weights using rules in Equations (4) and (5), respectively. In both cases, the conductances are all mapped along either one or two line segments. In contrast, Figures 6c,d show double weights (obtained through training without and with regularization, respectively) mapped onto conductances. In the nonregularized case (Figure 6c), the conductances are distributed mostly around the diagonal, though they are spread out, unlike in Figure 6a. Regularization results in more data points in the lower left corner of the diagram representing low-conductance values, as shown in Figure 6d.

Figures 6e–h demonstrate the utility of double weights. Here, the MNNs were trained to deal with less uniform D2D variability where the disturbances are much greater at low-conductance values compared to high-conductance values. As demonstrated in Figure 6g, the training naturally results in most of the conductance pairs concentrated in the upper right corner at high values. Like before, regularization in Figure 6h results in conductances with lower values.

Figure 6i shows the inference error for various weight implementations of MNNs encountering more uniform D2D variability. Conventional weights with mapping rule in Equation (5) result in the lowest median error of 7.3%; in comparison, double weights achieve median error of 8.3% without regularization and median error of 7.7% with regularization. Conventional weights with mapping rule in Equation (4) achieve the highest median error of 8.8%, indicating the unpredictability of the performance of mapping methods. Even so, it is important to point out that double weights do not achieve optimal performance in this case. We hypothesize that in scenarios where the dependence of the severity of the nonideality on the conductance values is not strong, double weights might struggle to find optimal configuration—infinitely many pairs may result in the same behavior, making it a more computationally difficult problem.

Figure 6j shows the inference error for equivalent weight implementations of MNNs dealing with less uniform D2D variability. In this case, the advantage of double weights is much more apparent—the median error in nonregularized case is 6.3% compared to 7.4% and 9.0% resulting from conventional weights with mapping rules in Equations (4) and (5), respectively. When double weights are trained by employing regularization, they take on lower values thus decreasing power consumption but also increasing the error—in the case of this specific nonideality, there is a tradeoff between energy efficiency and accuracy. However, double weights together with regularization provide a straightforward way of specifying to what extent low power consumption should be prioritized at the expense of accuracy.

### 3.5 Memristive Validation

As explained in Section 2.3, many memristive nonidealities are nondeterministic, therefore it might be advantageous to compute an aggregate metric for use in validation. To evaluate this approach, we employed high-magnitude D2D variability and compared MNNs trained without and with memristive validation. Specifically, for any training instance, two versions of the network were saved by utilizing the two validation techniques: the results are presented in Figure 7. In Figure 7a, typical validation approach is employed—validation set error is computed once every epoch. Its variability from epoch to epoch is high; though it could potentially be due to training alone, test set error is computed 20 times every 20 epochs and there is a noticeable difference between the lowest and highest error values. This suggests that the validation error may, too, vary greatly at any given epoch (and not just between epochs). Indeed, this is confirmed by Figure 7b where memristive validation (with validation set error computed 20 times every 20 epochs) is used—there are large differences between the minima and maxima of not only the test error, but also the validation error.

The inference error for the two methods is compared in Figure 7c. Only a minimal improvement in median error is achieved when using memristive validation—it decreases from 18.9% to 18.8%. Although we hypothesize that in aggregate this method will achieve only marginally better performance, it should help avoid choosing a highly suboptimal version of the weights which might yield higher error in a small number of cases. In Figure 7c, the errors at the 99th, 99.5th and 99.9th percentiles are 21.6%, 21.8% and 22.4%, respectively, for standard validation and 21.3%, 21.4% and 21.8%, respectively, for memristive validation.

Of course, memristive validation parameters may have to be optimized individually for each training configuration. For example, in the memristive CNN training in Figure 5b, the variability of validation error is usually lower at any given checkpoint than between checkpoints. In that case, one may increase the frequency of checkpoints by either decreasing the number of repeats at each checkpoint (and thus increasing uncertainty) or keeping it the same (and thus increasing computation time).
Figure 7: Effectiveness of validation checkpoints designed for memristive neural networks. a) training with standard validation, b) training with memristive validation, c) inference error comparing the approaches in a and b. The networks were trained on MNIST dataset and exposed to high-magnitude device-to-device variability. Panels a and b show curves for one of a hundred trained networks.

3.6 Nonideality Agnosticism

Accurate modeling of nonidealities for nonideality-aware ex-situ training is a significant challenge. Firstly, the nature of nonidealities encountered in practice may be different than what was modeled for the purposes of training. For example, D2D variability of SiO$_x$ memristors might mean that the behavior of any individual device might not be perfectly representative of the nature of other devices. Therefore, to hedge against fitting the model to the behavior of any specific device, we assumed that nonlinearity parameter is drawn from a truncated normal distribution. Even so, in different devices, the mean and standard deviation of this distribution may be different.

Secondly, in the real world, one may encounter completely different types of nonidealities. If the training takes into account the effects of only, say, I-V nonlinearities, MNNs could still suffer from, for example, stuck devices when deployed. Therefore, it is important to find out how robust the MNNs employing nonideality-aware training are.

To investigate this, we utilized networks trained either by assuming no nonidealities or by being exposed to one of 8 different combinations of nonidealities. In the case of both types of I-V nonlinearity and two types of D2D variability, networks were additionally trained using regularization. During inference, each group of networks was then exposed to the

- setup that they were trained on
- setups of the other groups of networks

In total, this produced $(1 + 8 + 2 + 2) \times (1 + 8) = 117$ scenarios; median inference error for each is presented in the heatmap in Figure 8.

The heatmap shows that, in most cases, the lowest error for a given nonideality during inference is achieved by the network that was exposed to it during training. A notable exception are networks exposed to high I-V nonlinearity during training (without regularization)—when exposed to low I-V nonlinearity, they achieve lower median error of 4.2% compared to 4.4% of networks that were trained (without regularization) on it. This may suggest that, in some cases, it can be advantageous to overestimate the amount of uncertainty during training.

Importantly, Figure 8 demonstrates that nonideality-aware training makes networks robust to the effects a wide array of nonidealities. Except for the ideal case and low-severity nonidealities (low I-V nonlinearity and devices stuck at $G_{off}$) nonideality-aware training results in lower median error compared to conventional training for all MNN groups—even when the networks encounter different nonidealities during inference. The heatmap also suggests that the effect of regularization on robustness is not always the same. In the case of I-V nonlinearity, regularization usually results in higher error (compared to nonregularized case) when encountering different nonidealities. On the other hand, regularization in networks dealing with D2D variability produces more robust behavior—when encountering different nonidealities, they usually achieve lower error.
4 Conclusion

In this work, design a novel nonideality-aware training scheme that can improve the performance of MNNs. We demonstrate the importance of taking nonideal device behavior into account during training—without that, training performance may not be indicative of how well the networks will perform during inference. Importantly, we show the utility of nonideality-aware training in dealing with linearity-nonpreserving nonidealities, specifically \( I-V \) nonlinearity. Our simulations show that the dichotomy between stable device behavior and power efficiency can become less relevant if the training stage is adjusted. Indeed, if nonideality-aware training is used, high-nonlinearity devices may achieve similar error rate, while also having three orders of magnitude better energy efficiency of 474 TOPs\(^{-1}\)W\(^{-1}\) (with regularization) compared to 555 GOPs\(^{-1}\)W\(^{-1}\) with the conventional training scheme and low-resistance devices.

We additionally explore a number of adjacent factors that are worth considering when dealing with MNN training. For example, we explore the use of double weights as a way to control conductance values of MNNs more directly through methods like \( \ell_1 \) regularization. We show the need to consider how validation is performed during training when nonidealities are stochastic and thus the outputs of an MNN are nondeterministic. In contrast to many previous works, we also investigate how robust nonideality-aware training is—we find that, compared to conventional training, it can usually achieve much lower error when encountering nonidealities that it was not trained to deal with. Besides, nonideality-aware training can be applied not just to one single type of nonideality—it can deal with multiple nonidealities at once, for example \( I-V \) nonlinearity and stuck devices, as shown in Figure 8.

Nonideality-aware training schemes are critical to making memristor-based ANNs feasible. Such schemes are key to ensuring low error rate and high energy efficiency.
Using experimental data and several novel optimization techniques, we demonstrate that our training design deals with a wide range of nonidealities, importantly linearity-nonpreserving nonidealities that have not been addressed during ex-situ training before. Further, we demonstrate that high-resistance operational ranges can be used to reduce power consumption by three orders of magnitude without significant accuracy loss, despite the high level of associated nonidealities.

5 Experimental Section

5.1 Experiments

5.1.1 SiO$_x$

Fabrication:
SiO$_x$ RRAM devices were fabricated on a Si substrate with 1 µm of thermal oxide on top. A 100 nm of Mo was deposited on top of the Si/SiO$_2$ substrate which served as the bottom electrode. The SiO$_x$ layer was sandwiched between the bottom and top electrodes and was deposited by reactive sputtering. The top electrodes consisted of 5 nm Ti wetting layer followed by a 100 nm of Au; their pattern was defined using a shadow mask. The device sizes ranged from 200 µm × 200 µm to 800 µm × 800 µm.

Characterization:
Electrical characterization of a 400 µm × 400 µm device was performed using Keithley 4200A-SCS. The signals were applied to the top electrode (Au), while the bottom electrode (Mo) was connected to the ground. The device required an initial electroforming step before stable resistive switching could be achieved. The forming process was carried out by a negative voltage sweep which stopped when the current had reached the limit of 3 mA. Subsequently, 18 voltage sweeps were performed to guarantee proper device performance: the voltage was ramped from 0.0 V, to ±2.5 V, and back to 0.0 V using a 3 mA current compliance.

After this, to achieve a wide range of resistances, incremental positive sweeps were applied to the sample, starting from 0.5 V and increasing by 0.05 V in each run. This was being repeated until there was no further resistance change, i.e. the filament had returned to its initial (post-forming) state. The obtained $I$-$V$ curves are shown in Figure S2 in the Supporting Information, while a subset of curves utilized in this work are shown in Figures 2a,b.

5.1.2 Ta/HfO$_2$

Fabrication:
Ta/HfO$_2$ 1T1R array contains NMOS transistors (with feature size of 2 nm) and Pt/HfO$_2$/Ta RRAM devices. The bottom electrode was deposited by evaporating 20 nm Pt layer on top of a 2 nm Ta adhesive layer. A 5 nm HfO$_2$ switching layer was deposited by atomic layer deposition using water and tetrakis(dimethylamido)hafnium as precursors at 250 °C. 50 nm Ta sputtered layer followed by 10 nm Pd served as the top electrode [26]. Fabrication process is described in more detail in [42].

Characterization:
Device conductance was being increased using SET pulses (500 µs @ 2.5 V and gate voltage linearly increasing from 0.6 V to 1.6 V). After each 100-pulse cycle, RESET pulses (5 µs @ 0.9 V linearly increasing to 2.2 V and gate voltage of 5 V) were used to reduce the conductance.

5.2 Simulations

5.2.1 Training and inference particulars

The following architectures were employed:

- fully connected ANNs (trained on MNIST [43]) containing
  1. fully connected layer with 25 hidden neurons and logistic activation function
  2. fully connected layer with 10 output neurons and softmax activation function
- CNNs (trained on CIFAR-10 [44]) containing
  1. convolutional layer with 32 output filters, 3 × 3 kernel size and ReLU activation function
  2. pooling layer with 2 × 2 pool size
  3. convolutional layer with 64 output filters, 3 × 3 kernel size and ReLU activation function
  4. pooling layer with 2 × 2 pool size
  5. convolutional layer with 64 output filters, 3 × 3 kernel size and ReLU activation function with maximum value of 1
  6. fully connected layer with 25 hidden neurons and logistic activation function
  7. fully connected layer with 10 output neurons and softmax activation function

To account high variability of nonidealities (that were nondeterministic), 5 networks were trained for each configuration. Each trained network went through 25 inference runs, totaling 5 × 25 = 125 runs for each configuration. An exception is simulations in Section 3.5—a 100 (instead of 5) networks were trained in order to investigate the effectiveness of memristive validation. However, only the
first five networks were used for agnosticism simulations in Section 3.6.

Networks used 4 : 1 training-validation split. All networks were trained for a 1000 epochs with batch size of 64. Where $\ell_1$ regularization had been employed, regularization factor of $10^{-4}$ was used. To ensure double weights stayed nonnegative we utilized NonNeg weight constraint provided by the Keras machine learning library. For any given batch (whose size was 64 during training, as mentioned before, and 100 during inference), conductances were disturbed once in the case of linearity-preserving nonidealities and nonlinearity parameters associated with individual devices were drawn from a random distribution once in the case of $I$-$V$ nonlinearity.

5.3 Statistical Analysis

- In all box plots, the maximum whisker length is set to 1.5 $\times$ IQR.
- In Figure 3 and equivalent plots, curves with semi-transparent regions consist of two parts summarizing 20 inference repeats at certain epochs: opaque curve representing the median values, and semi-transparent region bounded by the minimum and maximum values.
- To avoid large file size, only a subset of all data points is presented in Figures 2 and 6; these subsets were chosen randomly using NumPy.

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Author Contributions

D.J. and E.W. contributed equally to this work, as did A.M. and G.A.C. Authors thank Professor Qiangfei Xia of University of Massachusetts Amherst for sharing data on the switching of Ta/HfO$_2$ devices.

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Conflict of Interest Statement

The authors declare no competing interests.

Data Availability Statement

The source code for all the simulations in the paper can be found at https://github.com/joksas/nonideality-aware-mnn-training/releases/tag/2021-12-13. Ta/HfO$_2$ data that support the findings of this study are available from D.J. upon request. SiO$_x$ data have been made publicly available [45]; file excelDataCombined.mat was utilized in the simulations of this work. All data generated by the simulations have been made publicly available [46].
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### Supporting Tables

| ID | Nonideality | $G_{\text{off}}$ (S) | $G_{\text{on}}$ (S) | Parameters |
|----|-------------|---------------------|---------------------|------------|
| 1  | Low I-V nonlinearity in SiO$_x$ | $9.72 \times 10^{-4}$ | $3.514 \times 10^{-3}$ | $m_\gamma = 2.132$, $s_\gamma = 0.095$ |
| 2  | High I-V nonlinearity in SiO$_x$ | $7.723 \times 10^{-7}$ | $2.731 \times 10^{-6}$ | $m_\gamma = 2.989$, $s_\gamma = 0.369$ |
| 3  | Stuck at $G_{\text{off}}$ | - | - | $P(\text{stuck}) = 0.05$ |
| 4  | Stuck at $G_{\text{on}}$ | - | - | $P(\text{stuck}) = 0.05$ |
| 5  | Stuck Ta/HfO$_2$ devices | $4.364 \times 10^{-5}$ | $9.782 \times 10^{-4}$ | $P(\text{stuck}) = 0.101$ |
| 6  | More uniform D2D variability | - | - | $\sigma_{|R=R_{\text{off}}|} = \sigma_{|R=R_{\text{on}}|} = 0.25$ |
| 7  | Less uniform D2D variability | - | - | $\sigma_{|R=R_{\text{off}}|} = 0.5$, $\sigma_{|R=R_{\text{on}}|} = 0.05$ |
| 8  | High-magnitude D2D variability | - | - | $\sigma_{|R=R_{\text{off}}|} = \sigma_{|R=R_{\text{on}}|} = 0.5$ |

Table S1: **All nonidealities utilized in the simulations.** For mappings onto crossbar arrays, $G_{\text{off}}$ and $G_{\text{on}}$ of the nonidealities were used. Where these values were not available (because the models did not use experimental data), they were borrowed from nonideality 2.

| ID | Nonideality IDs | Notes | Figures |
|----|----------------|-------|---------|
| 1  | -              | Mapping from Equation (5) and standard validation. | 3a,d, 4, 5a,c, 8 |
| 2  | 1              | -     | 3b, 4, 8 |
| 3  | 1              | Regularized. | 3c, 4, 8 |
| 4  | 2              | -     | 3e, 4, 5b,c, 8 |
| 5  | 2              | Regularized. | 3f, 4, 8 |
| 6  | 6              | Mapping from Equation (4). | 6a,i |
| 7  | 6              | Mapping from Equation (5). | 6b,i |
| 8  | 6              | -     | 6c,i, 8 |
| 9  | 6              | Regularized. | 6d,i, 8 |
| 10 | 7              | Mapping from Equation (4). | 6e,j |
| 11 | 7              | Mapping from Equation (5). | 6f,j |
| 12 | 7              | -     | 6g,j, 8 |
| 13 | 7              | Regularized. | 6h,j, 8 |
| 14 | 8              | Standard validation. | 7a,c |
| 15 | 8              | -     | 7b,c, 8 |
| 16 | 3              | -     | 8 |
| 17 | 5              | -     | 8 |
| 18 | 2, 4           | -     | 8 |

Table S2: **Training setups.** Unless stated otherwise, the networks used double weights, regularization was not applied and memristive validation was used.

| ID | Nonideality IDs | Notes | Figures |
|----|----------------|-------|---------|
| 1  | -              | Mapping from Equation (5). | 8 |
| 2  | 1              | -     | 3a–c, 4, 8 |
| 3  | 2              | -     | 3d–f, 4, 5, 8 |
| 4  | 6              | Mapping from Equation (4). | 6i |
| 5  | 6              | Mapping from Equation (5). | 6i |
| 6  | 6              | -     | 6i, 8 |
| 7  | 7              | Mapping from Equation (4). | 6j |
| 8  | 7              | Mapping from Equation (5). | 6j |
| 9  | 7              | -     | 6j, 8 |
| 10 | 8              | -     | 7, 8 |
| 11 | 3              | -     | 8 |
| 12 | 5              | -     | 8 |
| 13 | 2, 4           | -     | 8 |

Table S3: **Inference/test setups.** This includes both the figures where the networks were evaluated on the test set after they had been fully trained and the figures in which test set performance was evaluated during training. Unless stated otherwise, the networks used double weights.
| Name                                      | Training setup ID | Inference setup ID |
|-------------------------------------------|-------------------|--------------------|
| Ideal                                     | 1                 | 1                  |
| Low $I-V$ nonlin. [SiO$_x$]               | 2                 | 2                  |
| Low $I-V$ nonlin. [SiO$_x$] (reg.)        | 3                 | -                  |
| High $I-V$ nonlin. [SiO$_x$]              | 4                 | 3                  |
| High $I-V$ nonlin. [SiO$_x$] (reg.)       | 5                 | -                  |
| Stuck at $G_{\text{off}}$                | 16                | 11                 |
| Stuck [Ta/HfO$_2$]                        | 17                | 12                 |
| More uniform D2D var.                    | 8                 | 6                  |
| More uniform D2D var. (reg.)             | 9                 | -                  |
| Less uniform D2D var.                    | 12                | 9                  |
| Less uniform D2D var. (reg.)             | 13                | -                  |
| High $I-V$ nonlin. [SiO$_x$] + stuck at $G_{\text{on}}$ | 18                | 13                 |
| High D2D var.                            | 15                | 10                 |

Table S4: Training and inference setups used in Figure 8.
**Supporting Figures**

**Figure S1**: Typical resistance switching behavior of the SiO$_x$ device. One SET and one RESET sweep are shown.

**Figure S2**: All I-V sweeps of the SiO$_x$ device. Single sweeps are shown for 53 different states obtained by incrementing maximum voltage by 0.05 V. Every seventh state shares the same color.
Figure S3: Training results for standard and nonideality-aware schemes when exposed to $I-V$ nonlinearities. Panels include equivalent curves of Figure 3 for all five trained networks. a, d) Training setup 1, b) training setup 2, c) training setup 3, e) training setup 4, f) training setup 5; a–c) test setup 2, d–f) test setup 3. Curves of different networks are indicated by different line styles in each of the panels.

Figure S4: Training results for nonideality-aware scheme with conventional weight implementations when exposed to device-to-device variability. a) Training setup 6, test setup 4, b) training setup 7, test setup 5, c) training setup 10, test setup 7, d) training setup 11, test setup 8. Curves of different networks are indicated by different line styles in each of the panels.
Figure S5: Training results for standard and nonideality-aware schemes when exposed to device-to-device variability. a, d) Training setup 1, b) training setup 8, c) training setup 9, e) training setup 12, f) training setup 13; a–c) test setup 6, d–f) test setup 9. Curves of different networks are indicated by different line styles in each of the panels.

Figure S6: Training results for standard and nonideality-aware schemes when exposed to high-magnitude device-to-device variability. a) Training setup 1, b) training setup 14, c) training setup 15; test setup 10 was used in all three panels. Curves of different networks are indicated by different line styles in each of the panels.
Figure S7: Training results for standard and nonideality-aware schemes when exposed to devices getting stuck at $G_{\text{off}}$. a) Training setup 1, b) training setup 16; test setup 11 was used in both panels. Curves of different networks are indicated by different line styles in each of the panels.

Figure S8: Training results for standard and nonideality-aware schemes when exposed to high $I-V$ nonlinearity and devices getting stuck at $G_{\text{on}}$. a) Training setup 1, b) training setup 18; test setup 13 was used in both panels. Curves of different networks are indicated by different line styles in each of the panels.

Figure S9: Training results for standard and nonideality-aware schemes when exposed to devices getting stuck. a) Training setup 1, b) training setup 17; test setup 12 was used in both panels. Curves of different networks are indicated by different line styles in each of the panels.