ScaleQC: A Scalable Framework for Hybrid Computation on Quantum and Classical Processors*

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Abstract

Quantum processing unit (QPU) has to satisfy highly demanding quantity and quality requirements on its qubits to produce accurate results for problems at useful scales. Furthermore, classical simulations of quantum circuits generally do not scale. Instead, quantum circuit cutting techniques cut and distribute a large quantum circuit into multiple smaller subcircuits feasible for less powerful QPUs. However, the classical post-processing incurred from the cutting introduces runtime and memory bottlenecks. Our tool, called ScaleQC, addresses the bottlenecks by developing novel algorithmic techniques including (1) a quantum states merging framework that quickly locates the solution states of large quantum circuits; (2) an automatic solver that cuts complex quantum circuits to fit on less powerful QPUs; and (3) a tensor network based post-processing that minimizes the classical overhead. Our experiments demonstrate both QPU requirement advantages over the purely quantum platforms, and runtime advantages over the purely classical platforms for benchmarks up to 1000 qubits.

1 Introduction

Quantum Computing (QC) has been proposed as a promising counterpart to classical computing, but QPUs face demanding hardware requirements to operate at useful scales. Many quantum algorithms offer runtime advantages over the best known classical algorithms, such as unstructured database search [16] and integer factorization [34]. To solve a problem, researchers develop a quantum algorithm that is represented as a $n$ qubit quantum circuit. A QPU then executes the circuit and samples its probability output to find the “solution” states, indicated by their much higher quantum state amplitudes than the non-solution states. In order to even run the circuit at all, the QPU must have at least $n$ qubits. Furthermore, the QPU’s qubits must be accurate and robust enough to support the quantum workload without accumulating too much noise to produce quality solutions. However, these two requirements put a heavy toll on the hardware. As an example, the famous Shor’s integer factorization algorithm is expected to take millions of physical qubits in order to construct enough number of high quality logical qubits to run problems at practical scales [35].

Instead, the recent introduction of the quantum circuit cutting theory [30] and its early demonstrations [38, 37] hint at the potential to combine multiple less capable QPUs and classical post-processing into a hybrid architecture. Circuit cutting techniques divide a large quantum circuit into several smaller subcircuits, which can be executed in parallel on multiple QPUs with lower qubit quantity and quality requirements. Classical post-processing is then used to reconstruct the output from these small subcircuit outputs. This hybrid architecture is analogous to the classical parallel computing where a large workload is distributed among many computing nodes, which afford to be much less powerful, but at the expense of some communication cost to reconstruct the results.

Dividing a large quantum circuit into many smaller subcircuits introduces obvious advantages over relying on either quantum or classical platforms alone. The most important advantage comes from that the subcircuits usually have fewer quantum gates, potentially also have fewer qubits. This puts a much lower qubit quality requirement for QPUs to produce accurate results, as the shallower and less complicated subcircuits incur much less crosstalk [24], decoherence [20], gate errors [4] and control difficulties [1]. In addition, having fewer qubits directly reduces the strict size limit on QPUs. Specifically, [38] demonstrates that certain algorithms can be run with fewer than half the number of qubits. Furthermore, since QPUs operate much faster than the classical simulations of quantum circuits, such hybrid architecture offers significant runtime speedup. Overall, quantum circuit cutting techniques combine less powerful QPUs and classical computing to expand the computational

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reach for both.

Despite the obvious advantages, two key challenges remain to make quantum circuit cutting practical. First, the classical post-processing overhead grows quickly with the number of cuts and bottlenecks the end-to-end workflow, preventing its application to hard-to-cut circuits. Second, the memory overhead to store and compute the state space of quantum circuits still doubles with every additional qubit, preventing its application to large circuits.

This paper overcomes the fundamental runtime and memory scalability difficulties of quantum circuit cutting and makes the hybrid architecture practical. Via an iterative search framework called states merging, ScaleQC offers the ability to locate solution states for arbitrarily large quantum circuits, hence bypassing the classical memory limitations. Via an automatic cut solver, ScaleQC finds high quality cuts suitable for post-processing and generalizes to different benchmarks. Via the compute graph contraction algorithm, ScaleQC reduces the runtime overhead to enable the applications to complicated circuits.

To evaluate the performance, we ran several realistic quantum benchmark algorithms such as QAOA [32], AQFT [3], Maximum Independent Set [32], Supremacy [4] and BV [6]. We demonstrated running quantum circuits of up to 1000 qubits. Our contributions include the following:

1. **Reduce Memory**: Developed a states merging method to efficiently locate arbitrary solution states for large quantum circuits, thus overcoming the classical memory scalability obstacles.

2. **Reduce Runtime**: Developed a Mixed Integer Programming (MIP) solver that automatically finds cuts for large quantum circuits to allow easier classical post-processing, while constrained by user-specified available QPU resources.

3. **Reduce Runtime**: Developed a compute graph contraction algorithm to significantly reduce the classical runtime overhead.

## 2 Background

This section introduces the quantum circuit cutting theory, its use cases and identifies its key challenges.

### 2.1 Circuit Cutting Theory

While we refer the readers to [30] for a detailed derivation and proof of the physics theory, we provide an intuitive understanding of the cutting process in order to identify its key challenges.

Circuit cutting cuts between quantum gates and decomposes the qubit states into their Pauli bases. With a proper selection of the cutting points, a large quantum circuit can be divided into smaller isolated subcircuits. Figure 1a shows an example 5-qubit quantum circuit. Without cutting, this circuit requires a QPU with at least 5 good enough qubits to execute all the quantum gates before too many errors accumulate. Circuit cutting makes 1 cut and divides this quantum circuit into two smaller subcircuits, each with both fewer qubits and fewer gates. Figure 1b shows that each subcircuit needs to be measured and initialized in different bases according to the permutations of all the cuts. Now multiple less powerful 3-qubit QPUs can run these independent subcircuits in parallel. The quantum interactions among the subcircuits are substituted by classical post-processing, which are analogues to the communication cost paid in classical parallel computing.

In general, a n qubit quantum circuit undergoes K cuts to divide into nC completely separated subcircuits C = {C1, ..., CnC}. A complete reconstruction of the quantum interactions requires each cut to permute each of the {I, X, Y, Z} bases, for a total of 4^K assignments. Depending on the basis assigned to the cuts connecting each
subcircuit, it is initialized and measured slightly differently to produce a distinct entry. We use \( p_i(k) \) to represent the output of subcircuit \( i \) in the \( k \)th cuts assignment, where \( i \in \{1,\ldots,n_c\} \) and \( k \in \{1,\ldots,4^K\} \). The physics theory \([30]\) dictates that the output of the original circuit is given by

\[
P = \sum_{k=1}^{4^K} \otimes_{i=1}^{n_c} p_i(k) \in \mathbb{R}^{2^n}
\]

where \( \otimes \) is the outer product between two subcircuit output vectors. Note that each subcircuit only has a different entry when at least one cut connecting it in the compute graph changes basis. This means that many of the \( p_i(k) \) repeat in the various summation terms.

### 2.2 Circuit Cutting Use Cases

Several theory proposals \([9,30]\) first introduce the possibility of quantum circuit cutting. Many small-scale demonstrations exist for chemical molecule simulations \([12]\) and variational quantum solvers \([46]\). In addition, several quantum computing industry leaders such as IBM and Xanadu \([44]\) are actively developing quantum circuit cutting products. These efforts either apply the hybrid architecture to real-world problems, or aim at incorporating it into the existing quantum hardware and software stack. However, none of the current efforts addresses the scalability obstacles.

### 2.3 Circuit Cutting Challenges

The key challenges of applying quantum circuit cutting at useful scales lie with the classical post-processing. Equation 1 clearly shows the two challenges as the following:

1. The length of the full output of a \( n \)-qubit circuit is \( 2^n \). Large quantum circuits quickly bottleneck the classical memory as well as the runtime.
2. The classical post-processing scales exponentially with the number of cuts required \( K \) and hence bottlenecks the runtime.

This paper develops the states merging technique to bypass the memory challenge altogether while reducing the classical overhead. In addition, this paper proposes compute graph contraction to significantly reduce the runtime overhead.

### 3 Framework Overview

Algorithm 1 outlines the overall framework of ScaleQC. The input to the framework includes the quantum circuit itself and a list of hyperparameters:

**Algorithm 1: ScaleQC Framework**

**Input:** Quantum circuit \( C \). Max load factor \( \alpha \). Max number of probability bins allowed per recursion \( M \). Max number of recursions \( R \).

1. Initialize an empty list \( L \)
2. Recursion counter \( r \leftarrow 0 \)
3. Find cuts for \( C \) to satisfy the max load \( \alpha \) and produce the compute graph \( G \). // Section 5
4. \( n_i \leftarrow \) number of data qubits in subcircuit \( i \in \{1,\ldots,n_c\} \)
5. \( \text{while } r < R \text{ do} \)
6. \( \text{if } r > 0 \text{ and bin is None then} \)
7. \( \text{BREAK // All solution(s) are found} \)
8. Compute the bin assignments for each subcircuit \( \{p_i,k\} \)
9. \( \text{Contract the compute graph } G \text{ to reconstruct the probability sums for the bins} \)
10. \( \text{Append the } R \text{ largest bins not yet fully expanded to } L \)
11. \( \text{Sort and truncate } L \text{ to keep the largest } R \text{ bins} \)
12. \( \text{Pop bin from } L \)
13. \( r \leftarrow r + 1 \)

1. Max QPU load factor \( \alpha \): The maximum fraction of the two-qubit gates each QPU can handle. For example, \( \alpha = 0.5 \) for a quantum circuit with 100 two-qubit gates means ScaleQC needs to cut into subcircuits with at most 50 two-qubit gates.
2. Max per-recursion bins \( M \): The maximum number of probability bins each states merging recursion computes.
3. Max recursions \( R \): maximum number of states merging recursions to run.

The framework is mainly built around an iterative procedure called the states merging to locate the solution states for the input quantum circuit (the while loop in Algorithm 1). Section 4 discusses the iterative procedure in detail. On a high level, ScaleQC recursively evaluates the subcircuits with QPUs and searches the solution states with classical computing until all solution states are found, or the user-defined max recursion depth \( R \) is reached first. States merging narrows down to a range of possible states containing the solutions when the max recursion depth is reached.
The solution states hence have much higher probabilities than the others. The states merging method makes use of the fact that the individual probabilities of the non-solution states are not of interest. Hence, instead of keeping track of the individual probability for each quantum state, the states merging method merges multiple states into one bin and keeps track of their sum of probabilities. The bins containing the solution states hence have much higher probabilities than the other bins and can be easily identified. The while loop in the ScaleQC framework in Algorithm 1 shows the complete process.

Each recursion of the procedure first assigns the quantum states still under analysis into various bins. Algorithm 2 shows the assignment process. Lines 1-4 first calculate the current number of bins for each subcircuit. The first recursion uses a loop in line 5 to locate the subcircuit states contained in bin $i$, $l_i \leftarrow \#states_i$. Copy $l'_i \leftarrow l_i$. Initialize the total number of bins required $l \leftarrow \prod_i l'_i$. While $l > M$ do Pick the subcircuit $i$ with the largest $l'_i$ $l'_i \leftarrow \lfloor l'_i/2 \rfloor$ $l \leftarrow \prod_i l'_i$ for $i \in \{1, \ldots, n_C\}$ do Initialize $l'_i$ empty bins for $j = 1, \ldots, l_i$ do $k \leftarrow j \% l'_i$ Append the $j$th state of subcircuit $i$ to bin $k$ of subcircuit $i$ end end return Updated subcircuit bin assignment

Quantum algorithms can be loosely characterized as two groups based on the type of their output. The first type produces concentrated outputs, where a few solution states have much higher probability amplitudes than the others. The solution states should only occupy a very small part of the entire state space, which is the very reason that it is useful for the quantum algorithms to find them efficiently. This paper mainly focuses on demonstrating circuits of this type.

The second type of algorithms produces a certain probability distribution, where the probability amplitudes are much more distributed among the states. We argue that large size circuits of this type are not practical, since their probability distributions most likely require exponentially many shots to converge even with a large and reliable QPU. In addition, it is impossible to store or analyze the entire state space. As a result, they are usually limited at medium sizes. ScaleQC is able to produce the full state output for this type of circuits.

One major bottleneck of quantum circuit cutting is that the length of the probability output of a $n$-qubit quantum circuit is $2^n$. Hence, full state reconstruction for large circuits quickly increases both the memory requirements and runtime. As an alternative, states merging offers a scalable way to only locate the solution states for large circuits.

The states merging method makes use of the fact that the individual probabilities of the non-solution states are not of interest. Hence, instead of keeping track of the individual probability for each quantum state, the states merging method merges multiple states into one bin and keeps track of their sum of probabilities. The bins containing the solution states hence have much higher probabilities than the other bins and can be easily identified. The while loop in the ScaleQC framework in Algorithm 1 shows the complete process.

Each recursion of the procedure first assigns the quantum states still under analysis into various bins. Algorithm 2 shows the assignment process. Lines 1-4 first calculate the current number of bins for each subcircuit. The first recursion
sion starts with each quantum state in its own separate bin, hence each subcircuit has \( l_i = 2^n \) bins, where \( n_i \) is the number of data qubits in the subcircuit \( i \). Subsequent recursions seek to expand a particular selected bin, hence each subcircuit has the number of subcircuit states belonging to the selected bin.

Next, lines 6-11 calculate the target number of bins to use for the next recursion. We shrink the subcircuit with the most number of bins by 2. The shrinking steps repeat until the total number of bins required satisfies the given memory limit \( M \).

Finally, lines 12-18 evenly assign the quantum states under analysis into the number of bins calculated for the next recursion.

The max number of bins \( M \) enables a key trade-off for the states merging procedure. The states merging procedure is equivalent to a full state reconstruction if the max number of bins allowed \( M \) is larger than the size of the full state \( 2^n \). In this case, the states merging procedure simply locates all the solution states in one recursion. Any \( M \) smaller than \( 2^n \) essentially provides a trade-off of the size of the vectors to compute during each iteration versus the number of iterations required to locate all the solution states.

For the extreme case where the non-solution states have 0 probability, the states merging procedure is guaranteed to find all the solutions in at most \( mn/\log_2 M \) recursions for a \( n \)-qubit circuit. Where \( m \) is the number of solution states. Figure 2 visualizes an example for a 100-qubit circuit, assuming \( M = 20 \) bins, which is negligible as compared to the \( 2^{100} \) full states. Each recursion expands a bin for finer details of the quantum states contained. A max depth of \( \frac{100}{20} = 5 \) produces leaf bins with just 1 state. A solution state is found when a leaf bin with just 1 state and high probability is computed. The entire states merging process hence creates a search tree with a depth of \( n/\log_2 M \) and width of \( m \), representing total \( mn/\log_2 M \) recursions.

The procedure finds solutions more quickly if multiple solution states happen to be assigned into the same bin, which reduces the width of the search tree at some depth. Having larger \( M \) shortens the search tree but has diminishing returns, as doubling \( M \) only increases the denominator by 1. Furthermore, larger \( M \) means slower post-processing for each recursion. As a result, it is usually favored to use smaller \( M \) even if larger \( M \) fits in the memory.

In addition, larger quantum circuits (larger \( n \)) and more solution states (larger \( m \)) only increase the number of states merging recursions linearly. The method hence easily scales to large quantum circuits with more solution states.

Comparison with classical arbitrary state simulation methods: The state-of-the-art simulation work [22] only simulates an arbitrary subset of quantum states for large circuits to avoid the exponential number of quantum states. Our method easily achieves the same functionality if we just select an arbitrary subset of quantum states to run for a single recursion without merging into bins. However, such arbitrary selection methods will have virtually 0 chance to include any solution states in the sampled subset. To find any solution states, such methods will need to run almost \( 2^n \) times and thus do not scale. Instead, the states merging method strictly outperforms the existing methods via its iterative searches.

[38] proposed a Dynamic Definition search method that is similar in spirit with states merging. The method iteratively fixes the state of the individual qubits to search for the solution states. However, this method forces quantum states without common qubit states (such as \( |01\rangle \) and \( |10\rangle \)) to be in different bins, thus can only be located in separate recursions. States merging is hence more efficient as it allows any solution states to be located simultaneously.

## 5 Locate Cutting Points

With the overall framework in mind, this section discusses the first step in circuit cutting – determine the cutting points.

Figure 3a shows an example QAOA quantum circuit solving the maximum independent set problem for a random Erdos-Renyi graph with 5 qubits. Quantum circuits can also be represented as directed acyclic graphs (DAG), where the vertices are the gates and the edges are the qubit lines connecting the gates. Hence, locating the cutting points is equivalent to partitioning the quantum gates into certain number of subcircuits. Note that DAG partition problems only concern with the connection among the vertices, but the single qubit gates do not affect such connections. As a result, the single qubit gates are ignored during cuts finding, and are simply attributed to the same subcircuit as their closest two-qubit gate neighbor.

Figure 3b shows its corresponding DAG representation after removing the single-qubit gates. The input (green) and output (red) qubit vertices are illustrated for a clearer correspondence with Figure 3a. However, there is no reason to partition any I/O vertices solely by themselves. Therefore, the I/O vertices are also safely ignored during cuts finding.

### 5.1 MIP Model

Figure 5a shows the DAG graph to partition, which only includes the two-qubit quantum gates. We adapt from [38] to encode the DAG for our MIP solver. We denote the \( n_C \) subcircuits as \( \{C_1, \ldots , C_{n_C}\} \), all the qubit lines as edges in \( E \), and all the quantum gates as vertices in \( V \). Furthermore,
we define the edge and vertex variables as

\[ x_{e,c} = \begin{cases} 1 & \text{if edge } e \text{ is cut by subcircuit } c \\ 0 & \text{otherwise} \end{cases} \]

\[ y_{v,c} = \begin{cases} 1 & \text{if vertex } v \text{ is in subcircuit } c \\ 0 & \text{otherwise} \end{cases} \]

\[ \forall e \in E, \forall v \in V, \forall c \in \{1 \ldots n_C\} \]

The numbers of incoming and outgoing cut edges to a subcircuit are modeled as

\[ I_c = \sum_{e \in E} x_{e,c} \times y_{e[1],c} \]

\[ O_c = \sum_{e \in E} x_{e,c} \times y_{e[0],c} \]

The number of quantum gates in each subcircuit is modeled as

\[ S_c = \sum_{v \in V} y_{v,c} \]
5.2 MIP Constraints and Objective

Figure 5 shows the subcircuit abstraction obtained after applying some cuts to the DAG. We call this abstraction the compute graph, where each subcircuit is a vertex and the edges are the cuts selected. Each subcircuit is also connected with some output qubit vertices. We limit the max subcircuit size based on the load factor $\alpha$ and demand that

$$S_c \leq \alpha |V|, \forall c \in C$$  \hspace{1cm} (2)

In addition, the MIP model contains the corresponding constraints to help define the edge and vertex variables.

Our efficient post-processing algorithms escape the seemingly exponential cost suggested by Equation 1 but they also make the exact post-processing cost of quantum circuit cutting much nuanced and depend on many factors. We defer the detailed discussions of post-processing the compute graph to Section 6.2. Let us accept for now that the computation complexity is closely related with the compute graph degree, which serves as an indirect measure of the computation overhead. The compute graph degree is just the max number of cuts on any subcircuit, which is simply the sum of the incoming and outgoing cut edges. Therefore, our MIP solver seeks to minimize

$$L \equiv \max_{c \in \{1, \ldots, n_C\}} \{I_c + O_c\}$$ \hspace{1cm} (3)

Furthermore, the number of subcircuits $n_C$ to partition into cannot be captured as part of the optimization model. Instead, we run our solver for up to $n$ subcircuits for a $n$-qubit benchmark to obtain several possible solutions. Results from Section 6 then allow us to predict the exact post-processing cost for each. The cutting solution with the lowest computation cost is eventually selected.

Overall, the cut search problem is transformed as an integer programming model. However, this constrained graph partition problem is conjectured to have no efficient solutions in polynomial time \cite{12}. Instead, we utilized the commercial solver Gurobi \cite{17} to implement our model. We limit the runtime to 30 seconds for each candidate $n_C$ for an approximate solution if an optimal solution is not found within the time.

6 Compute Graph Contraction

This section introduces compute graph contraction for an efficient post-processing. According to Equation 1, the final reconstruction of the output of the uncut circuit requires permutating the $\{I, X, Y, Z\}$ indices for the $K$ cut edges, taking the outer products among the subcircuits, and sum over all the $4^K$ terms. The naive computation of Equation 1 quickly becomes the bottleneck for complicated circuits as it incurs many redundant computations. This is because subcircuits in general do not connect with all the edges and hence remain unchanged across many different edge bases. In addition, it is preferable to group many outer products as matrix products, as GPUs usually compute matrix products much faster than the explicit iterations over the rows and columns. Compute graph contraction hence seeks to eliminate the redundant computations and exploit the more efficient compute kernels.

6.1 Relation with Tensor Network Contraction

Post-processing the compute graph is in fact equivalent to tensor network contractions, which have been widely used in classical simulations of quantum systems \cite{41, 42, 33, 40}. Figure 4 establishes the equivalence of a pairwise tensor contraction with a compute graph contraction containing two subcircuits.

Figure 4a shows contracting a pair of tensors means taking the sum over their common index (indices).
their last dimensions as however many bins each subcircuit
circuits beyond classical memory, the beginning tensors have
has different number of cuts and number of qubits, hence
compute graph contraction is exactly a tensor contraction.
traction is a single tensor of dimension
into a single vertex. The final output of compute graph con-
tion process finishes when all the vertices are contracted
qubits in each tensor for brevity. The dashed edges are the
dashed. Each output qubit has a dimension of
Figure 6: Slicing one cut edge to express the compute graph
as a summation of smaller compute graphs.

6.2 Memory Requirement and Compute Cost

The memory requirement of the post-processing comes
from two parts. First, we need to store the input subcircuit
tensors. The tensor of subcircuit $i$ has $4^\text{#cuts}_i \times 2^\text{#qubits}_i$
(4^#cuts$_i \times$ #bins$_i$) floats when employing full state (states
merging). Second, we need to store all the intermediate ten-
 sor products during the contraction.

The compute cost of the post-processing can be cap-
tured by the floating point multiplications required in all
the contraction steps. The number of multiplications of a
pair of contraction is simply the product of all the dimen-
sions involved. For example, Figure 4a requires $\dim(i) \times
\dim(j) \times \dim(k)$ multiplications. Similarly, Figure 4b
requires $2^1 \times 4^\text{#cuts} \times 2^1$ multiplications.

Now we can easily predict the memory and compute
overhead of a compute graph without actually perform-
ing the computations. The input subcircuit tensors for
the example contraction step in Figure 5a require total
$4^3 \times 2^4 + 4^2 \times 2^0 + 4^3 \times 2^4 = 1168$ float numbers
and $(2^2 \times 2^4) \times (2^4) \times (2^1)$ multiplications. The con-
traction step in Figure 5b requires $4^3 \times 2^4 + 4^2 \times 2^0 = 1152$
float numbers and $2^4 \times 4^4 \times 2^4 = 2048$ multiplications.

In contrast, the naive computation of Figure 5a based on
Equation 1 requires $4^4 \times (2^1 \times 2^0 + 2^1 \times 2^1) = 8704$
multiplications, a 3.4× extra overhead.

It is now clear that both the memory and compute cost
of compute graph contraction are positively correlated with
the number of cuts on each subcircuit during every con-
traction step. This explains our MIP solver objective choice in
Equation 3. In order to keep the post-processing runtimes
reasonable, we limit the compute graph degree to be 15.

6.3 Two Level Index Slicing

It is possible that complicated compute graphs with
many cuts require input subcircuit tensors too large to fit in
the memory. Hence we implement an index slicing strategy

Figure 5: Contracting the compute graph example from Fig-
ure [3d] The output qubits are abbreviated as the number of
qubits in each tensor for brevity. The dashed edges are the
traction edges in each step. The sub-figures show the
best contraction order obtained from Section 6.4.

is simply the matrix product $C = AB$.

Figure 4b shows a hypothetical example of contracting
a compute graph with two subcircuits. Each subcircuit is
a tensor, the cut edges are the common indices to be con-
tracted, and the output qubits are the output indices. Each
cut edge has a dimension of 4 because of the $\{I, X, Y, Z\}$
labels to permute. Each output qubit has a dimension of
2 because of the $|0\rangle$, $|1\rangle$ bases. Explicitly writing out the
output indices based off Equation 1 clearly shows that the
compute graph contraction is exactly a tensor contraction.

Figure 5 shows the contraction process for the compute
graph in Figure 3d as tensor contractions. Each subcircuit
has different number of cuts and number of qubits, hence
different dimensions of tensors at the beginning. Each step
contracts two vertices in the compute graph. The con-
traction process finishes when all the vertices are contracted
into a single vertex. The final output of compute graph con-
taxtion is a single tensor of dimension $\{2^n\}$ for a $n$-qubit
circuit when using full state reconstruction.

Furthermore, when we apply states merging to large cir-
cuits beyond classical memory, the beginning tensors have
their last dimensions as however many bins each subcircuit

(c) Contraction process finishes. The output is a single
tensor of dimension $\{2^3\}$, as expected from a 5-qubit input

circuit.
prior to their contraction to reduce the input tensor sizes. Index slicing is to explicitly write out certain indices and express the full tensor network as a summation of smaller tensor networks. In the context of compute graph, it is to explicitly write out certain cut edges. For example, slicing one edge in Figure 6 reduces the input subcircuit tensor sizes to $4^2 \times 2^1 + 4^2 \times 2^1 = 304$ float numbers but produces 4 smaller compute graphs to contract. Our heuristics keep slicing the index that reduces the overall tensor sizes the most, until the overall sizes fit in the memory specified. The heuristics hence produce a set of smaller compute graphs that we explicitly iterate over.

In addition, the intermediate tensor products during contractions may also exceed memory. We further applied the index slicing algorithm from the CoTenGra software [15] to each sub compute graph generated from the first level of slicing.

6.4 Determine Contraction Order

In tensor network contractions, different contraction orders significantly affect the overhead, sometimes even introduce orders of magnitude differences. In circuit cutting, the contraction order of the subcircuits only affects the reconstruction up to a permutation of the qubit order, and has no effect on the quantum state probability accuracy. However, finding the optimal contraction order for general compute graphs is hard. In fact, it is an active area of research and of broader interest across many disciplines [31, 23, 28]. We used the CoTenGra software [15] to compile the contraction order for each sub compute graph.

7 Methodology

This section introduces the various backends, benchmarks, and metrics.

7.1 Backends

The following three backends are involved in the experiments:

1. Quantum: Direct evaluation of quantum circuits on a powerful enough QPU without circuit cutting;
2. Cut: The standard ScaleQC framework in full state;
3. Cut\_M: Cut with states merging. This is equivalent to full state evaluation when states merging runs to completion. We run the max number of $mn / \log_2 M$ recursions to guarantee completion.

Large circuits tend to have larger subcircuits as well, but the Noisy Intermediate Scale Quantum (NISQ) devices nowadays are still too small and noisy for any meaningful experiments at even medium sizes. Hence we use random numbers as the subcircuit output. Although it does not produce any useful circuit outputs, it does not affect the post-processing runtime results of the experiments. We expect more reliable QPUs to enable a full implementation of the ScaleQC framework.

We use a single compute node with 64 CPUs equipped with a single Nvidia A100 GPU for all the cuts finding and classical post-processing.

7.2 Benchmarks

We used the following circuits as benchmarks:

1. $BV$: Bernstein-Vazirani circuit [6] solves the hidden substring problem. Has 1 solution state.
2. $Regular$: Quantum Approximate Optimization Algorithm solves the maximum independent set problem for random 3-regular graphs [32]. With the proper hyperparameters, this circuit produces 1 solution state. However, the full QAOA training process to solve the hyperparameters is beyond the scope of this paper. We use random hyperparameters with the same circuit structure.
3. $Erdos$: The same algorithm as $Regular$ but for random Erdos-Renyi graphs.
4. $Supremacy$: Random quantum circuits adapted from [7]. Deeper versions of the circuit was used by Google to demonstrate quantum advantage [4]. Our paper uses depth $(1 + 8 + 1)$ at various sizes. As it does not have well-defined solution states, we run $mn / \log_2 M$ recursions to produce more samples.
5. $AQFT$: Approximate Quantum Fourier Transform [5] that is expected to outperform the standard QFT circuit under noise.

All of our benchmarks are examples of circuits and routines that are expected to demonstrate quantum advantage over classical computing on the Quantum backend. ScaleQC aims to demonstrate the middle ground where the overall runtime is slower than Quantum but still beyond the classical reach, while the quantum and classical computing resources requirements are much lower.

7.3 Metrics

There are two key metrics this paper looks at, namely runtime and quantum resources.

**Runtime, faster is better:** For Quantum, it is the end-to-end runtime on a standalone QPU, which is the best runtime possible. The Cut and Cut\_M backends are slower.
The ScaleQC runtime is the end-to-end runtime except time spent on QPUs in Algorithm 1. The NISQ QPUs nowadays are small, slow and too noisy for any practical purposes. As we expect the practical ScaleQC applications to be used with medium sized reliable QPUs in the near future, it is irrelevant to profile the NISQ QPU runtime now. Furthermore, multiple small QPUs can be used in parallel to reduce the runtime. In addition, the runtime advantage of QPUs over CPUs will be even more significant for larger circuits. We expect the framework to offer more significant advantages over classical methods as larger and more reliable QPUs become available.

Quantum Area, smaller is better: The quantum resources requirement is loosely defined as the product of the circuit width and depth, called the ‘quantum area’. Classical simulations require 0 quantum area as it does not use QPUs at all. For Quantum, it is simply the product of the number of qubits and the circuit depth of the input quantum circuit. For the various ScaleQC backends, it is defined for the largest subcircuit produced from cutting. The rationale is that QPUs must be able to support the workloads with a certain quantum area at high accuracy to produce accurate results. While many hardware and software factors affect the QPUs’ ability to support quantum workloads, a smaller quantum area generally puts less burden on the quantum resources.

8 Experiment Results

8.1 Runtime

When the size of the Hilbert space of the quantum circuits is still within the memory limit, it is possible to perform full state evaluation. This cutoff depends on the particular classical backend available to the users. We use 30 qubits as the cutoff in this paper, which is roughly $10^9$ states. However, since each qubit doubles the memory requirement, there is little value in pushing this cutoff point to the extreme.

Figure 7 plots the benchmark circuits $20 \rightarrow 30$ qubits, subject to a max load of $\alpha = 0.4$. We observe that the majority of the runtime is spent on searching the cuts. For example, the runtime breakdown of the AQFT benchmarks shows that nearly all of the postprocessing runtime comes from the cut searching. This pre-processing overhead can be significant for medium sized benchmarks due to their short overall runtime. As a result, it might not be worth the overhead to use circuit cutting for medium circuits. Admittedly, classical simulators operate relatively fast and are usually adequate for such small benchmarks. As a reference, the widely used Qiskit [3] simulator takes about $30 \rightarrow 50$ seconds to run the 30-qubit benchmarks on the same classical backend. ScaleQC is able to produce comparable runtime even for the small benchmarks where classical simulation excels.

While finding the optimal cut solution can be difficult for large circuits, our experiments capped the solver runtime to produce high quality solutions. The cut searching step can hence be viewed as a nearly constant pre-processing overhead for large benchmarks. In fact, ScaleQC has more significant runtime advantages for larger circuits, where the cut searching overhead no longer bottlenecks the framework. Furthermore, ScaleQC with states merging becomes necessary to deal with the exponentially increasing state space.

Figure 8 plots the runtime scalability for large benchmarks, subject to a max load of $\alpha = 0.8$ for the two QAOA benchmarks and $\alpha = 0.5$ for the rest. We set $M = 2^{20}$ bins. Each experiment runs $n/\log_2 M$ recursions to find at least
M requires QPUs to support at most about \( M \) as the percentage over Quantum since it just needs to support the smaller subcircuits. Figure 9 plots the quantum areas of Cut_M as the percentage of Quantum for the same experiments in Figure 8. Figure 11 similarly plots the quantum areas of the large BV benchmarks in Figure 9. Quantum simply requires the area of the input benchmark circuit. Cut_M requires QPUs to support the quantum area of the largest subcircuit from cutting. With \( \alpha = 0.5(0.8) \), Cut_M requires QPUs to support at most about 57%(83%) of the quantum area to run the various benchmarks, at the expense of the postprocessing runtimes in Figures 8 and 9.

Lower quantum area requirements translate to the ability to tolerate smaller and noisier NISQ devices. Furthermore, in the fault tolerant regime, lower quantum areas translate to a looser requirement on the logical qubit error rate. Depending on different quantum error correction solutions, this implies much reduced physical qubit counts and error threshold requirements. In addition, compiling and decoding the smaller subcircuits are also much easier than larger circuits, which put much less burden on the quantum software development.

### 8.3 Compare Against Classical Simulation

There are lots of purely classical simulation works \([43, 10, 18, 22]\). The state-of-the-art tensor network based method \([22]\) slices a deeper 100-qubit \textit{Supremacy} circuit into \(32^6\) “subtasks” to fit onto almost 42 million cores on the Sunway supercomputer. As a comparison, our shallower benchmark will be sliced into \(2^6\) such “subtasks” by the same metric.

Figure 12 shows a qualitative comparison for the most related benchmark circuit. To maintain their 300 seconds runtime, we estimate \([22]\) to require \(42 \times 10^6 \times \frac{2^6}{32^6} \approx 2.5\) cores for 1 million samples at \(< 1\%\) fidelity, or \(2.5 \times 5 \times 100 = 1250\) cores for 5 million samples at the same perfect postprocessing fidelity as ScaleQC shows in Figure 8.

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**Figure 9**: States merging for large BV circuits. Max load \( \alpha = 0.5 \). Max bins \( M = 2^{20} \). Each data point is the average of 5 trials. Cut_M runs \( n/\log_2 M \) recursions (i.e. 50 for the 1000-qubit benchmark) to find the unique solution. The runtime will be the same to reconstruct \( Mn/\log_2 M \) states for the \textit{Supremacy} benchmark, which is about 7 million states for the 144(12 × 12)-qubit circuit. Instead, states merging obtains more information about the entire state space under the same time.

**Figure 10**: Quantum areas comparisons for the same experiments in Figure 8. The numbers in the legends indicate the average quantum area of Cut_M as a percentage over Quantum. Cut_M requires QPUs to support at most 83% of the quantum area at the expense of the classical runtimes in Figure 8.

**Figure 11**: Quantum areas comparisons for the same experiments in Figure 9. Cut_M requires QPUs to support about 25% of the quantum area at the expense of the runtimes in Figure 9.

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**8.2 Resources Estimations**

ScaleQC also requires much less powerful QPUs than Quantum since it just needs to support the smaller subcircuits. Figure 8.5 plots the runtime scalability for the BV benchmark up to 1000 qubits, subject to a max load of \( \alpha = 0.5 \) and \( M = 2^{20} \) bins. Each experiment runs to completion to find the unique hidden string solution.

The various benchmarks scale well as circuits get larger. The \textit{Erdos} benchmark appears to be the hardest and no solutions were found above 80 qubits for the maximum of 15 compute graph degree.

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**Figure 8**: Time (s) vs Circuit Sizes for BV benchmark. Lower is Better.
Table: Method Comparison

| Method | Supremacy Benchmark | Backend | Runtime | Result |
|--------|---------------------|---------|---------|--------|
| ScaleQC | 10\times10^6(1 + 8 + 1) #subtasks = 2^8 | 1 Nvidia A100 GPU on 1 core. | 50 seconds | About 5 million states at perfect classical post-processing fidelity. Overall fidelity depends on GPUs. |
| Liu et al. | 10\times10^6(1 + 40 + 1) #subtasks = 32^6 | 42 million cores on the Sunway supercomputer | 304 seconds | About 1 million states at < 1% fidelity. |

Figure 12: Compare against [22]. We estimate [22] requires $42 \times 10^6 \times 2^6 \times 100 \times 5 \approx 1250$ cores and 300 seconds for our benchmark. Each recursion of ScaleQC produces 1 million more states at minimal extra runtime cost. However, [22] requires the same time for each 1 million more states.

Figure 13: Running the Supremacy benchmark for varying number of recursions. Max load $\alpha = 0.5$, max bins $M = 2^{20}$. Since each states merging recursion is fast, adding more recursions do not increase the runtime too much.

We can easily modify the states merging framework to instead produce 1 million arbitrary states in each recursion. Figure 13 runs various Supremacy benchmarks for 10, 50, 100 recursions. Specifically, 5 recursions of the 100-qubit Supremacy benchmark takes about 50 seconds in Figure 8. Meanwhile, 100 recursions of the same benchmark only takes about 160 seconds in Figure 13. The little runtime increase for more recursions shows that the majority of the runtime is the one-time initial cut searching. Furthermore, the cut searching allows our method to generalize to any benchmarks.

In contrast, [22] manually pre-determines the slicing strategy specifically but only for the Supremacy benchmark. It also needs to spend the same runtime for every 1 million more samples calculated.

Deeper and more complicated benchmarks are going to require more than a single GPU. ScaleQC relies on the continued developments of HPC techniques to port to scalable parallel computing backends.

9 Related Work

Many quantum compiler works exist to improve the performance of standalone QPUs to evaluate quantum circuits [27][36][25][11][26]. Quantum error correction is the key to build reliable QPUs [14][8][19][45][21]. QAOA uses classical computing to tune quantum circuit hyper-parameters to solve optimization problems [13][39]. However, they still rely entirely on QPUs to compute the quantum circuits.

Prior circuit cutting implementations [38][37] rely on parallelization techniques for faster compute while performing direct reconstruction of Equation 1 with high overhead. The various post-processing algorithms proposed in this paper go beyond what is possible from such techniques and reduce the overhead itself.

10 Conclusion

This paper overcomes the classical runtime and memory scalability challenges for hybrid computation via novel post-processing algorithms and develops the corresponding cuts searching algorithm. By distributing large quantum workloads to quantum and classical processors, we demonstrate up to 1000-qubit quantum circuits running on both QPUs and GPUs, which is significantly beyond the reach of either platform alone and previous hybrid workflows. As ScaleQC bridges the classical and the quantum technologies and paves the way for hybrid computations, its future developments naturally benefit from advancements on both sides.

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