Work function variations on electrostatic and RF performances of JLSDGM Device

K K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, Ameer F. Roslan, I. Ahmad

1,2,3,4MiNE, CeTRI, Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka, Malaysia
1Faculty of Engineering and Built Environment, Lincoln University College, Malaysia
5College of Engineering (CoE), Universiti Tenaga Nasional (UNITEN), Malaysia

ABSTRACT

This paper offers a systematic analysis on the impact of work function (WF) variations on electrostatic and radio frequency (RF) performances of n-channel junctionless strained double gate (n-JLSDGM) metal oxide semiconductor field effect transistor (MOSFET). The study has been performed under other constant level of design parameters that operates in saturation as a transconductance amplifier, considering the dependence of electrostatic and RF performance on the variation of WF. Furthermore, this paper aims to provide physical insight into the improved electrostatic and RF performances of the proposed n-JLSDGM device. The device layout and characteristics were designed and extracted respectively via a comprehensive 2-D simulation. Device performances such as on-state current (I_{ON}), off-state current (I_{OFF}), on-off current ratio, subthreshold swing (SS), intrinsic capacitances, dynamic power dissipation (P_{dyn}), cut-off frequency (f_{T}), and maximum oscillation frequency (f_{max}) are intensively investigated in conjunction with WF variations.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Fauziyah Salehuddin
Micro and Nano Electronics (MiNE), Centre for Telecommunication Research and Innovation (CeTRI)
Faculty of Electronics and Computer Engineering (FKEKK)
Universiti Teknikal Malaysia Melaka
Hang Tuah Jaya, Durian Tunggal, 76100 Melaka, Malaysia
Email: fauziyah@utem.edu.my

Nomenclatures

- C_{gd}: Gate-to-drain capacitance
- C_{gg}: Gate-to-gate/parasitic capacitance
- C_{gs}: Gate-to-source capacitance
- I_{max}: Maximum oscillation frequency
- f_{r}: Cut-off frequency
- g_{m}: Transconductance
- I_{OFF}: Off-state current
- I_{ON}: On-state current
- L_{ch}: Channel length

Abbreviations

- SCE: Short channel effect
- SS: Subthreshold swing
- WF: Metal work function

Journal homepage: http://ijeecs.iaescore.com
1. INTRODUCTION

Over the past decade, the transistor’s layouts heavily rely on the formation of junctions. The presence of junctions become extremely important for blocking and allowing the current to flow as the gate bias is applied. Those junctions are commonly patterned based on the location of two opposite polarity’s regions that placed besides one another, known as the p-n junction. However, as the transistor dimension is further shrinking, the fabrication process of the junction transistors is becoming quite complicated due to the requirement of extremely low thermal budget processing. The low thermal budget processing is required to form a junction with high doping gradient, while avoiding the dopant redistribution which could affect the transistor performance [1]-[3]. Therefore, junctionless configuration is introduced as an alternative transistor structure that would avoid such intricate fabrication process. Khorramrouz, et al. has mentioned that the process variation in junctionless transistors might be avoidable but the uncertainties caused by the insulating thickness could alter the shape of the energy band diagram [3].

The first patent of junctionless transistor have been invented by the Austrian-Hungarian physicist, Julius Edgar Lilienfield on 22 October 1925 [4]. The transistor invented by Lilienfield consists of a thin semiconductor film, deposited on a thin layer of insulator protected by a metal electrode. The metal electrode functions as a gate which controls the conducting channel. The working principle is mainly based on the currents flow in the resistors between two metal electrodes, similar to the modern metal oxide semiconductor field effect transistor (MOSFET) device in which the drain current flows between source and drain regions. The Lilienfield’s transistor simply behaves as a resistor that allows the thin semiconductor layer to be depleted as certain gate bias is applied, thus modulating its carriers. The key feature of the junctionless transistor is the creation of an ultra-thin silicon (Si) body that allows complete depletion of most carriers in the channel as the device is turned on [5], [6]. Also, the ultrathin Si body has to be heavily doped for allowing an adequate amount of current flow to turn the device on. Junctionless configuration has been found to be applied to most of fully depleted devices such SOI MOSFET, FinFETs, Multigate FETs, π-gate FETs, Ω-gate FETs and Gate-all-Around FETs, vertical MOSFETs and nanowire devices [7]-[11].

There have been some significant problems with aggressive transistor scaling, such as short channel effects (SCE), impact ionizations, and gate leakage [12]-[14]. Therefore, numerous channel engineering approaches have been proposed to counter these issues [15]-[17]. High-k-metal-gate (HKMG) stack technology is one the common approach to control the gate leakage current [18]-[20]. The HKMG integration offers an alternative option in minimizing the gate leakage without having to reduce the thickness of the insulator for same intrinsic capacitances [21]. Rezeli et al. have stated that parameter dependencies should be carefully considered in HKMG based transistor due to inconsistent atom configuration at the surface material [15].

Besides HKMG, strained engineering is also an effective approach to overcome the limit of transistor’s scaling [22]. It has been proven to provide a significant boost in the transistor’s electrostatic and radio frequency (RF) performance by integrating silicon-germanium (SiGe) on silicon layer (strained channel), while keeping the compatibility with complementary metal oxide semiconductor (CMOS) technology [23]. The placement of HKMG layers on the top of the strained channel could further enhance the carriers mobility while maintaining acceptable leakage current (I_{ON}) [24], [25] have emphasized that strain-engineered SiGe-based channel improved the transistor performance but the variability impact on ultra-scale nanowire resulting in strong V_{th} variations should be seriously looked into [26].

The impact of work function (WF) engineering towards electrostatic and RF performances of a transistor is very crucial, especially with tremendous growth in the RF wireless technologies and the demand for low-cost high-speed RF applications. The WF engineering of CMOS technology requires the integration of different HKMG materials for NMOS and PMOS. Tuning the appropriate WF that match the HKMG properties becomes a crucial factor in achieving a better electrostatic and RF performances of a transistor [27]-[29].

In our recent works, the impact of gate length variations on the n-channel Junctionless Strained DG-MOSFET (n-JLSDGM) performances have been studied and analyzed [11]. The results have showed excellent device properties where both I_{ON} and g_{m(max)} were estimated at 1680 μA/μm and 2.79 mS/μm respectively. Another published work emphasized on the impact of strain channel on n-JLSDGM properties [25]. The results reveal the adoption of strain effect has tremendously enhanced the channel mobility, on-state current, on-off ratio and transconductance of the device. However, this paper focuses on a systematic analysis of the impact of WF variation on the electrostatic and RF outputs of the n-JLSDGM device.

The paper is structured as follows: section 2 explains the n-JLSDGM’s dimension and the 2-D simulation via Silvaco Athena and Atlas respectively. Section 3 provides a comprehensive study of the impact of WF variation on the electrostatic and RF performances in the n-JLSDGM device. Finally, the conclusions and future work are briefly discussed in section 4.
2. DEVICE DIMENSION AND SIMULATION

Figures 1 and 2, respectively, display the simulation flow and cross-section layout for n-JLSDGM device. The main substrate of this device was based on SiGe material (Ge<20%) with a thickness of 8nm, mainly opted due to its larger lattice constant than Si [30]. The ultrathin Si layer (1 nm) was then deposited on the top of the main SiGe layer, thus forming a strained Si layer. The strained effect on the Si layer was fundamentally caused by the stretched Si atoms as its majority trying to coordinate with the atoms of SiGe.

Next, the strained SiGe and Si layers were heavily doped with $1 \times 10^{17} \text{cm}^{-3}$ of Arsenic dose (n-type). Tungsten silicide (WSi$_2$) layer was opted for the gate material due to its superior tunable WF [31]-[33]. The top and bottom gate configuration was intended to boost the gate controllability over the strained channel, thereby improving the carrier’s mobility. The length of the gate ($L_g$) of the proposed device was scaled to approximately 6 nm. The WSi$_2$ layer was then placed on the high-k dielectric layer to avoid potential defects at the insulator/gate boundaries that would cause the threshold voltage ($V_{th}$) pinning.

Due to its high dielectric allowability (~85eV), titanium dioxide (TiO$_2$) was chosen as a gate dielectric (insulator). The utilization of TiO$_2$ as the gate dielectric opened the possibility to apply thicker insulator for the metal-gate. The TiO$_2$ layer (~85 eV) could be scaled approximately 21 times thicker than the silicon dioxide, SiO$_2$ (3.9 eV), thereby minimizing the leakage while keeping the same capacitance as SiO$_2$ layer. Equivalent oxide thickness (EOT) is a merit figure to indicate the necessary SiO$_2$ layer thickness that would have an effect close to that of a certain high-k dielectric material. Hence, the EOT for the n-JLSDGM device can be computed as:

$$EOT = \left( \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} \right) T_{high-k}$$

(1)

where $\varepsilon_{SiO_2}$ is the permittivity of SiO$_2$ (3.9 eV), $\varepsilon_{high-k}$ is the permittivity of high-k dielectric and $T_{high-k}$ is the physical thickness of high-k dielectric. Since the TiO$_2$ (~85 eV) with 3nm of thickness was employed as the gate insulator, the EOT of the insulator for the n-JLSDGM device was computed to be 0.138 nm.

The next process was source/drain (S/D) doping in which the S/D regions were infused with the similar dopant type used in channel doping process (Arsenic). This process was performed in order to shape the N N+ N configuration, so that no junctions were created between channel and S/D regions (Junctionless). Due to junctionless configuration, the strained channel was significantly depended on the high doping concentration to insure a large drive current. The metallization process was then carried out by depositing the aluminum layer on the entire surface of the device structure. Both contacts and electrodes were formed by etching the unwanted aluminum layer. Lastly, the structure was mirrored in both x and y axis to form a complete n-JLSDGM. The design parameters used for simulating the device are listed in Table 1.
3. IMPACT OF THE WORK FUNCTION VARIATIONS ON JLSDGM’S PERFORMANCE

Work function (WF) of transistors can be tuned in many ways such as molecular doping, stacking bi-metal layer, and chemical vapor deposition control. In this study, work function (WF) has been tuned by doping TiSi2/WSi2 stack with different arsenic concentration, ranging from 4.6 eV to 4.8 eV. To explicitly investigate on the impact of work function (WF) variations towards the n-JLSDGM’s performances, the simulation results have been divided into two different categories which are electrostatic performance and RF performance. Despite of having different structure, the definition and graphical extraction of the n-JLSDGM device are still similar with the conventional double-gate MOSFET.

3.1. Electrostatic performances

The combined plot of $I_{ds}$-$V_{gs}$ transfer characteristics at a constant $V_{ds}$=0.5 V with different WF in both linear and log scales for n-JLSDGM device are shown in Figure 3. It shows the impact of different WF on $I_{ds}$-$V_{gs}$ transfer characteristics at a constant $V_{ds}$=0.5 V, shifting the curves from 0 V to 1 V. It is observed that the $I_{ds}$ of n-JLSDGM is inversely proportional with the WF variation in which the $I_{ds}$ increases as the WF decreases.
This implies that higher WF yields higher threshold voltage ($V_{th}$) which definitely reduces the rate of $I_{ds}$ improvement over the increased gate bias. With lower WF, the electron mobility in the depleted channel becomes increased due to reduced electric field, thereby increasing the on-state current ($I_{ON}$) as shown in Figure 4. It is observed that the $I_{ON}$ is increased by approximately 35% as the WF is reduced from 4.8 eV to 4.6 eV.

Since the value of $I_{ON}$ is totally depended on the $V_{th}$, the $V_{th}$ value must be carefully adjusted by tuning the correct metal WF. As for n-JLSDGM device, decreasing the WF would contribute to lower $V_{th}$, thus increasing the $I_{ON}$. This is in agreement with the results reported by [21], [29], [35]. Based on the results, the highest recorded $I_{ON}$ is demonstrated by the n-JLSDGM device with $WF=4.6$ which is measured at approximately 1951 $\mu$A/µm. From the leakage perspective, the off-state current ($I_{OFF}$) exhibits a constant value until the WF is reduced to 4.6 eV as depicted in Figure 5. The plot clearly shows that the $I_{OFF}$ is increased by approximately 56% as the WF of the n-JLSDGM device is further reduced below 4.7 eV. The result implies that a lower WF would contribute to much larger leakage current which eventually deteriorating the n-JLSDGM’s performance. Such behavior is mainly due to lesser barriers in the channel which might fail to prevent the excessive electrons from being leaked as the WF is further reduced.

![Figure 4. Plot of on-state current ($I_{ON}$) versus work function (WF)](image)

![Figure 5. Plot of off-state current ($I_{OFF}$) versus work function (WF)](image)

The effect of WF variation towards on-off ratio of the n-JLSDGM device is also shown in Figure 6. It is shown that the n-JLSDGM device exhibits random pattern of variation in on-off ratio as the WF is reduced from 4.8 eV to 4.6 eV. This is predominantly due to the unpredictable leakage behavior towards the WF variation. The highest on-off ratio is demonstrated by the n-JLSDGM device with 4.7 eV which is measured at 4.7x10$^{-5}$. Higher on-off ratio is always desirable for attaining much lower static power dissipation especially in digital circuit designs.

Subthreshold swing (SS) is another electrical characteristic that are crucial for analyzing the short channel behaviors in n-JLSDGM device. It is used to indicate how much the $V_{gs}$ required increasing the $I_{ds}$ by one decade. It also implies how effective the current flow can be halted as the $V_{gs}$ is reduced below $V_{th}$. A transistor with smaller SS value normally demonstrates much faster switching capability since less $V_{gs}$ is needed to change the device condition from its on-state to off-state or vice versa. The SS of the n-JLSDGM device is mathematically described as:

$$SS = \frac{dV_{gs}}{d(log_{10} I_{ds})}$$

The impact of WF variations on the SS for n-JLSDGM device is shown in Figure 7. As the WF ranges from 4.6 eV to 4.8 eV, it is observed that the n-JLSDGM shows a constant SS value. Therefore, it can be assumed that no shift in the SS value is caused by the difference in WF. The SS is estimated at 84.8 mV/decade for all the investigated WF ranges. Smaller SS denotes an increased immunity from short-channel effects (SCE) and thus an improved channel gate access. The extracted and calculated magnitude of $V_{th}$, $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$ ratio and SS for n-JLSDGM device are tabulated in Table 2. In the next sub-section, the effect of WF variations on RF performances is addressed.

| Table 2 | Value |
|---|---|
| $V_{th}$ | 4.7 eV |
| $I_{ON}$ | 1951 $\mu$A/µm |
| $I_{OFF}$ | 4.7x10$^{-5}$ |
| $I_{ON}/I_{OFF}$ ratio | 35% |
| SS | 84.8 mV/decade |

Indonesian J Elec Eng & Comp Sci, Vol. 23, No. 1, July 2021: 150 - 161
3.2. RF Performances

Gate-to-source capacitance ($C_{gs}$), gate-to-drain capacitance ($C_{gd}$), parasitic capacitance ($C_{gg}$), intrinsic gate delay ($\tau_{int}$), dynamic power dissipation ($P_{dyn}$), cut-off frequency ($f_{T}$) and maximum oscillation frequency ($f_{m}$) are all quite important parameters to be examined from the RF design perspective. After post-processing DC analysis, AC small signal analysis is then performed in order to extract intrinsic capacitances ($C_{gs}$ & $C_{gd}$) and parasitic capacitance ($C_{gg}$). Capacitances between regions is determined by a single $1\, \text{MHz}$ AC input frequency ($f$), as the $V_{gs}$ are shifted from $0\, \text{V}$ to $1\, \text{V}$ at a constant step of $0.01\, \text{V}$.

The combined plot for the intrinsic capacitances ($C_{gs}$ & $C_{gd}$) as a function of $V_{gs}$ for multiple $WF$ values is shown at Figure 8. The n-JLSDGM device exhibits very small variation in the $C_{gs}$ upon $WF$ adjustment. The $C_{gs}$ values of the device for all the investigated $WF$ begin to deliberately increase as they reach the corresponding $V_{Th}$. The lowest $C_{gs}$ value is observed to be $1.12\, \text{fF}/\mu\text{m}$, exhibited by the device with $WF=4.8\, \text{eV}$. Apart from that, the $C_{gd}$ values of the device for all the investigated $WF$ show an almost constant value until they reach a higher level of $V_{gs}$. At maximum $V_{gs}$, the $C_{gd}$ of the n-JLSDGM has been increased by around $57\%$ as the $WF$ has been decreased from $4.8\, \text{eV}$ to $4.6\, \text{eV}$. The n-JLSDGM with $WF=4.8$ indicates the lowest $C_{gd}$ estimated at $0.87\, \text{fF}/\mu\text{m}$.

These intrinsic capacitances might not be mutual. In fact, considering the n-JLSDGM device in the saturation mode, any variation of the $V_{ds}$ would not contribute any significant variation in the $I_{ds}$ and the intrinsic capacitances due to pinch off phenomenon. However, when the $V_{gs}$ is varied, a variation in $I_{ds}$ would happen, consequently inducing variation in $C_{gd}$. In other words, a higher potential is applied to the gate, a higher $C_{gd}$ would be induced. In RF and high frequency circuits, very large $C_{gd}$ is not desirable, because this could cause a substantial delay on the $I_{ds}$ to rise during on-state condition and to fall during the off-state condition. Another essential feature to test RF output is the gate-to-gate capacitance ($C_{gg}$). $C_{gg}$ is also known as a parasitic gate capacitance used to calculate the intrinsic gate delay ($\tau_{int}$).

The plot for $C_{gs}$ as a $V_{gs}$ function with a constant $V_{ds}=0.5\, \text{V}$ for multiple $WF$ ranges is shown in Figure 9. The $C_{gs}$ of n-JLSDGM rises by about $37\%$, with the $WF$ reduced to $4.6\, \text{eV}$ from $4.8\, \text{eV}$. The lowest $C_{gg}$ has been demonstrated by the device with $WF=4.8\, \text{eV}$, measured at $1.98\, \text{fF}/\mu\text{m}$. Thus, lower $WF$ can give a better control of the channel depletion area in the ultra-thin fully depleted body, subsequently reducing SCEs and parasitic capacitances.

A substantial decrease in $C_{gs}$ would result in much less intrinsic delay at the gate and dynamic power dissipation. For determining frequency limits of JLSDGM, the intrinsic gate delay ($\tau_{int}$) is very important to be considered. The $\tau_{int}$ in JLSDGM device is significantly related to the magnitude of $C_{ss}$ and $I_{ds}$, mathematically defined as:

![Figure 6. Plot of on-off current ratio versus work function (WF)](image)

![Figure 7. Plot of subthreshold swing (SS) versus work function (WF)](image)

Table 2. Electrostatic Performances of n-JLSDGM Device at different $WF$

| $WF$ (eV) | $I_{on}$ (µA/µm) | $I_{off}$ (µA/µm) | $I_{on}/I_{off}$ ratio (x10$^3$) | $SS$ (mV/dec) |
|----------|-----------------|------------------|-------------------------------|-------------|
| 4.6      | 1951            | 7.8              | 2.5                           | 84.8        |
| 4.7      | 1595            | 3.4              | 4.7                           | 84.8        |
| 4.8      | 1275            | 3.4              | 3.8                           | 84.8        |
\[ \tau_{\text{int}} = \frac{C_{gs} \times V_{DD}}{I_{ds}} \]  

(3)

where \( \tau_{\text{int}} \) is the intrinsic gate delay and \( V_{DD} \) is the supply drain voltage. Plot for \( \tau_{\text{int}} \) as a \( V_{ds} \) function at constant \( V_{gs} = 0.5V \) for multiple \( WF \) ranges is represented in Figure 10.

Figure 11 indicates a small improvement in \( P_{\text{dyn}} \) by around 7% as the \( WF \) decreases from 4.8 eV to 4.6 eV. Thus, it can be said that the \( WF \) variation does not greatly affect the power dissipation of the device. The device with \( WF=4.8 \) eV, measured at 1.78 nW/\( \mu \)m, shows the lowest \( P_{\text{dyn}} \). Definitively, lower \( C_{gg} \) would minimize the \( P_{\text{dyn}} \) of the device. Remarkable n-JLSDGM’s features such as ultrathin and fully depleted body would minimize the parasitic capacitances between regions. Hence, it is crucial to ensure the magnitude of \( C_{gg} \) as well as \( P_{\text{dyn}} \) to be as low as possible in maintaining an ideal temperature for the RF circuits [36]. Any significant rise in temperature could deteriorate the device performance either in on-state or off-state.

The \( \tau_{\text{int}} \) of the n-JLSDGM is considerably lowered, with the reduction of \( WF \) from 4.8 eV to 4.6 eV, by around 89%. The lowest \( \tau_{\text{int}} \) is shown by the device with \( WF=4.6 \) eV measured at 4.8 ps. Although the device with \( WF=4.6 \) eV has the highest \( C_{gs} \), it still exhibits the lowest propagation delay. Such occurrence is mainly due to the shorter path of electron flows between source and drain region which is dominantly governed by the \( WF \). As the \( WF \) is reduced, the electron density inside the strained channel would be significantly increased, eventually contributing to much higher \( I_{ds} \). Besides that, the impact of \( WF \) variation on \( C_{gs} \) is pretty weak, thus any \( WF \) adjustments do not have an important effect on the \( \tau_{\text{int}} \). For this reason, the \( I_{ds} \) is regarded as a dominant control factor to decide the \( \tau_{\text{int}} \) for n-JLSDGM device.
In transient analysis, the dynamic power dissipation ($P_{\text{dyn}}$) is also an integral feature of the AC. As the frequency ($f$) is continuously delivered at 1 MHz, $C_{gs}$ has a critical role to play in evaluating the $P_{\text{dyn}}$. The dynamic power dissipation ($P_{\text{dyn}}$) is mathematically expressed as:

$$P_{\text{dyn}} = C_{\text{int}} V_{DD}^2 f$$

(4)

where $f$ is the operating frequency and $P_{\text{dyn}}$ is the dynamic power dissipation. Plot $P_{\text{dyn}}$ as the $V_{ds}$ function at constant $V_{gs}=0.5V$ for multiple WF ranges is shown in Figure 13.

A significant characteristic in the analysis of RF output of the n-JLSDGM device is the cut-off frequency ($f_T$). It is defined as the frequency of transition at which the small signal current gains into unity. In other words, $f_T$ is the frequency when the current gain is unity which can be measured by:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

(5)

The plot of $f_T$ as a function of $V_{gs}$ at constant $V_{ds}=0.5V$ for the multiple WF ranges is represented in Figure 12. The highest $f_T$ is observed to be 236 GHz, demonstrated by the n-JLSDGM device with WF=4.8 eV. As the WF drop from 4.8 eV to 4.6 eV, the $f_T$ is decreased by roughly 24%. This clearly indicates that the $f_T$ is significantly governed by the value of the intrinsic capacitances ($C_{gs}$ & $C_{gd}$). A lower value of intrinsic capacitances is always desired to generate much higher $f_T$, especially for high frequency RF CMOS designs. It is also shown that the $f_T$ of n-JLSDGM device is inversely proportional with the $g_m$ in which the maximum $f_T$ is measured at minimum $g_m$ value. The $f_T$ is shown to be substantially decreased for all WF ranges when the gate bias exceeding 0.8V.

The $f_T$ is definitely an excellent indicator for low-current forward transit time. However, the impact of gate resistance ($R_g$), that is crucial to estimate the transient response of the n-JLSDGM device, is entirely disregarded for the performance indicator. Therefore, an indicator, known as the maximum oscillation frequency ($f_{\text{max}}$), which takes $R_g$ into account is proposed. The $f_{\text{max}}$ is the frequency where the unilateral acquisition of power becomes unity. In other words, it is the highest frequency from which the power gain can be drawn out of the transistor. The $f_{\text{max}}$ for the n-JLSDGM device can be mathematically calculated by:

$$f_{\text{max}} = \sqrt{\frac{f_T}{8\pi R_g C_{gd}}}$$

(6)

where,

$$R_g = \frac{1}{2\pi f_T (C_{gs} + C_{gd})}$$

(7)

Figure 12. Plot of $f_T$ as a function of $V_{gs}$

Figure 13. Plot of $f_{\text{max}}$ as a function of $V_{gs}$

Work function variations on electrostatic and RF performances of JLSDGM Device (K K. E. Kaharudin)
The plot of $f_{\text{max}}$ as a $V_{gs}$ function with constant $V_{ds}=0.5$ V for the multiple WF ranges is shown in Figure 13. The $f_{\text{max}}$ is decreased by about 43% with the WF lowered from 4.8 eV to 4.6 eV. The n-JLSDGM device with $WF=4.8$ eV, measured at 3294 GHz, shows the maximum $f_{\text{max}}$. Due to the WF variation, the value of $f_{\text{max}}$ is mainly governed by the $R_s$ value. The increased WF would reduce parasitic capacitances of the device, thus increasing the $f_T$. As a result, $R_s$ is further decreased with $f_T$ continuing to rise, subsequently increasing the maximum oscillation frequency of the device. With such remarkable $f_T$ and $f_{\text{max}}$ properties, n-JLSDGM can be utilized as the future low-power high frequency transistor configuration. For a JLSDGM device with multiple WF ranges, the extracted and estimated magnitude of $C_{gs}$, $C_{gs}$, $\tau_{\text{on}}$, $P_{\text{dyn}}$, $R_T$ and $f_{\text{max}}$ are listed in Table 3.

| WF (eV) | $C_{gs}$ (fF/µm) | $C_{gd}$ (fF/µm) | $C_{gd}$ (fF/µm) | $\tau_{\text{on}}$ (ps) | $P_{\text{dyn}}$ (nW/µm) | $R_T$ (GHz) | $f_{\text{max}}$ (GHz) |
|---------|----------------|----------------|----------------|----------------|----------------|-------------|----------------|
| 4.6     | 1.15           | 2              | 3.15           | 4.8            | 1.92           | 180         | 1890          |
| 4.7     | 1.16           | 1.03           | 2.19           | 9.9            | 1.87           | 233         | 3007          |
| 4.8     | 1.12           | 0.87           | 1.98           | 45.7           | 1.78           | 236         | 3294          |

The $f_T/L_d$ ratio of the JLSDGM device have been compared to different structures of transistor from recent studies as shown in Table 4. Since some of the transistor structures have utilized various gate length ($L_d$), the comparative performance of $f_T$ has to be done based on $f_T/L_d$ ratio. Based on Table 4, it is observed that JLSDGM device has demonstrated the highest $f_T/L_d$ ratio compared to others. The $f_T/L_d$ ratio of JLSDGM device is estimated at 39.3 while moderate doped drain dual-channel single gate junctionless field-effect transistor (MDD-DCJLT), heavy doped drain dual-channel single gate junctionless field-effect transistor (HDD-DCJLT), overlap composite channel double gate MOSFET (CCDGM) and overlap CCDGM are estimated at 20.7, 28.4, 30.8 and 23.4 respectively [28, 37].

| Parameter            | JLSDGM (This work) | MDD-DCJLT [28] | HDD-DCJLT [28] | Underlap CCDGM [37] | Overlap CCDGM [37] |
|----------------------|---------------------|----------------|----------------|---------------------|---------------------|
| Gate Length, $L_d$ (nm) | 6                   | 20             | 20             | 12                  | 12                  |
| $f_T$ (GHz)          | 236                 | 413            | 568            | 369                 | 281                 |
| $f_T/L_d$ ratio      | 39.3                | 20.7           | 28.4           | 30.8                | 23.4                |

Based on the overall results, WF variation is very sensitive to the output of n-JLSDGM device in electrostatic and RF terms. Some of the investigated properties indicate incoherence due to slight WF alteration. WF variation is not the only factor influencing random output fluctuations. Other input parameters such as channel doping, source/drain doping, high-k dielectric constant and body thickness should be included for detailed analysis [38]-[41]. In view of the effect of other input parameters besides work function, statistical-based and AI-based optimization approaches [42]-[44] will be applied in the future work in order to reduce the output variance that may further improves the device's electrostatic and RF performances.

4. CONCLUSION

In summary, the impact of work function variations upon electrostatic and RF performance of n-channel junctionless strained DG-MOSFET (n-JLSDGM) has been comprehensively studied using industrial based 2-D process (Silvaco Athena) and device simulator (Silvaco Atlas). The characteristics of the device used in measuring electrostatic and RF performances are thoroughly investigated, including on-state current, off-state current, on-off ratio, subthreshold swing, intrinsic gate delay, dynamic power dissipation, intrinsic capacitances, cut-off frequency and maximum oscillation frequency. The final results suggest the 35% rise in state-current ($I_{\text{on}}$) when the WF dropped from 4.8 eV to 4.6 eV. From the perspective of radio frequency (RF) performance, the cut-off frequency ($f_T$) and oscillation frequency ($f_{\text{max}}$) of the n-JLSDGM device decrease by ~24%, and ~43% respectively, with the WF reduced from 4.8 eV to 4.6 eV. The overall results of the study prove that the variation in metal work function has contributed significant influences on the overall n-JLSDGM’s performances. The JLSDGM device demonstrates outstanding electrical properties, such as a high on-state current, high transconductance, a lower consumption of power, high cut-off frequency which can be regarded as a potential MOSFET structure for future high-frequency RF applications.
ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE, CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

REFERENCES

[1] D. A. J. Millar, X. Li, U. Peralagu, and M. J. Steer, “High Aspect Ratio Junctionless InGaAs FinFETS Fabricated Using a Top-Down Approach,” 2018 76th Device Research Conference (DRC), no. September, pp. 1–2, 2018, doi: 10.1109/DRC.2018.8442150.

[2] S. C. Wagaj, S. Patil, and Y. V. Chavan, “Performance analysis of shielded channel double-gate junctionless and junction MOS transistor,” International Journal of Electronics Letters, vol. 6, no. 4, pp. 192–203, 2018, doi: 10.1080/21681724.2017.1335785.

[3] F. Khorramrouz, S. A. S. Ziaibari, and A. Heydari, “Analysis and study of geometrical variability on the performance of junctionless tunneling field effect transistors: Advantage or deficiency?,” International Journal of Nano Dimension, vol. 9, no. 3, pp. 260–272, 2018.

[4] J. P. Colinge, C. W. Lee, A. Alzalian, and N. D. Akhavan, “Nonwire transistors without junctions,” Nature Nanotechnology, vol. 5, no. 3, pp. 225–229, 2010, doi: 10.1038/nnano.2010.15.

[5] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, and A. F. Roslan, “Effect of Channel Length Variation on Analog and RF Performance of Junctionless Double Gate Vertical MOSFET,” Journal of Engineering Science and Technology, vol. 14, no. 4, pp. 2410–2430, 2019.

[6] D. H. Son, Y. Jo, J. H. Seo, and C. H. Won, “Low voltage operation of GaN vertical nanowire MOSFET,” Solid-State Electronics, vol. 145, pp. 1–7, 2018, doi: 10.1016/j.sse.2018.03.001.

[7] S. R. Mulmame, S. C. Wagaj, and N. U. Chaudhari, “Simulation of Nanoscale Fully Depleted EJ- SOI Junctionless MOSFET for High Performance,” International Journal of Industrial Electronics and Electrical Engineering, vol. 4, no. 6, pp. 34–37, 2016.

[8] M. A. Riyadi, I. D. Sukawati, T. Prakoso, and Darjat, “Influence of gate material and process on junctionless FET subthreshold performance,” International Journal of Electrical and Computer Engineering, vol. 6, no. 2, pp. 895–900, 2016, doi: 10.11591/ijece.v6i2.407.

[9] S. Archana, G. Vallathan, and M. A. Kumar, “Analytical Modeling of Dual Material Junctionless Surrounding Gate MOSFET,” SSSR International Journal of Electronics and Communication Engineering, vol. 4, no. 3, pp. 40–43, 2017.

[10] R. Ambika and R. Srinivasan, “Impact of structural process variation on junctionless silicon nanotube FET,” Advances in Natural Sciences: Nanoscience and Nanotechnology, vol. 9, no. 3, pp. 1–7, 2018, doi: 10.1088/2043-6254/aadd33.

[11] K. E. Kaharudin, A. F. Roslan, F. Salehuddin, Z. A. F. M. Napiah, and A. S. M. Zain, “Design Consideration and Impact of Gate Length Variation on Junctionless Strained Double Gate MOSFET,” International Journal of Recent Technology and Engineering, vol. 8, no. 256, pp. 783–791, 2019, doi: 10.3940/jirte.B1146.0782S619.

[12] M. Vadizadeh, “Characteristics of GaAs/GaSb tunnel field-effect transistors without doping junctions: numerical studies,” Journal of Computational Electronics, vol. 17, no. 2, pp. 745–755, 2018, doi: 10.1007/s10825-018-1136-6.

[13] K. A. Gupta, D. K. Anvekar, and V. V., “Modeling of Short Channel MOSFET Devices and Analysis of Design Aspects for Power Optimisation,” International Journal of Modeling and Optimization, vol. 3, no. 3, pp. 266–271, 2013, doi: 10.7763/IJMO.2013.V3.279.

[14] K. Biswas, A. Sarkar, and C. K. Sarkar, “Fin shape influence on analog and RF performance of junctionless accumulation-mode bulk FinFETs,” Microsystem Technologies, vol. 24, no. 5, pp. 2317–2324, 2018.

[15] F. A. Rezahi, M. Mazhar, N. Aida, F. Othman, and S. W. Muhamad, “Performance and device design based on geometry and process considerations for 14/16 - nm FinFETs stress engineering,” IEEE Transactions on Electron Devices, vol. 63, no. 3, pp. 974–981, 2016, doi: 10.1109/TED.2016.2520583.

[16] C. Nanmeni Bondja, Z. Geng, R. Granzner, and J. Pezoldt, “Simulation of 50-nm Gate Graphene Nanoribbon Transistors,” Electronics, vol. 5, no. 3, 2016, doi: 10.3390/electronics5010003.

[17] A. Kumar, M. M. Tripathi, and R. Chaujar, “Comprehensive analysis of sub-20 nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications,” Supramolecules and Microstructures, vol. 116, no. February, pp. 171–180, 2018, doi: 10.1016/j.spmi.2018.02.018.

[18] Y. Chai, S. Su, D. Yan, M. Ozkan, R. Lake, and C. S. Ozkan, “Strain Gated Bilayer Molybdenum Disulfide Field Effect Transistor with Edge Contacts,” Scientific Reports, vol. 7, no. December 2016, pp. 1–9, 2017, doi: 10.1038/srep41593.

[19] W. Chakraborty, K. Ni, S. Dutta, B. Grisafe, J. Smith, and S. Datta, “Cryogenic Response of HKMG MOSFETs for Quantum Computing Systems,” in Device Research Conference - Conference Digest, DRC, 2019, June, no. 1, 2019, pp. 115–116, doi: 10.1109/DRC49490.2019.9046346.

[20] H. H. Radamson, Z. Huilong, Z. Wu, and X. He, “State of the art and future perspectives in advanced CMOS technology,” Nanomaterials, vol. 10, no. 8, pp. 1–86, 2020, doi: 10.3390/nano10081555.

[21] G. Dhim and R. Pourush, “Analysis of Variations of Metal Gate Work Function on Junctionless Double Gate MOSFET with High-k Spacers,” in International Conference on Emerging Trends in Communication, Control and Computing, 2020, pp. 1–4, doi: 10.1109/ICONC345789.2020.9117425.
[22] S. Krivec, M. Poljak, and T. Suligoj, “The Physical Mechanisms Behind the Strain-Induced Electron Mobility Increase in InGaAs-On-InP MOSFETs,” IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 2784–2789, 2018, doi: 10.1109/TED.2018.2838681.

[23] A. Varshney, “Analytical study of strained soi mosfet,” International Journal of Research in Engineering and Technology, vol. 5, no. 12, pp. 47–52, 2016, doi: 10.1562/IRET.2016.0512009.

[24] T. K. Sharma and S. Kumar, “A comparative study of above-and sub-threshold characteristics of strained and unstrained Si GAA MOSFETs,” in 2018 International Symposium on Devices, Circuits and Systems (ISDCS), 2018, pp. 1–6, doi: 10.1109/ISDCS.2018.8379655.

[25] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, A. F. Roslan, and I. Ahmad, “Impact of strained channel on electrical properties of Junctionless Double Gate MOSFET,” Journal of Physics: Conference Series, vol. 1502, 2020, doi: 10.1088/1742-6596/1502/1/012045.

[26] T. P. Dash, S. Dey, S. Das, E. Mohapatra, J. Jena, and C. K. Maiti, “Strain-engineering in nanowire field-effect transistors at 3 nm technology node,” Physica E: Low-Dimensional Systems and Nanostructures, vol. 118, no. September 2019, p. 113964, 2020, doi: 10.1016/j.physe.2020.113964.

[27] R. Saha, B. Bhowmick, and S. Baishya, “Impact of work function on analog/RF and linearity parameters in step-FinFET,” Indian Journal of Physics, no. October, pp. 1–6, 2020.

[28] A. Garg, Y. Singh, and B. Singh, “Dual-Channel Junctionless FETs for Improved Analog/RF Performance,” Silicon, no. June, pp. 1–9, 2020.

[29] Y. Harpara and R. Saha, “Analysis on DC and RF/Analog Performance in Multifin-FinFET for Wide Variation in Work Function of Metal Gate,” Silicon, vol. 133, no. 2, pp. 1–5, 2020, doi: 10.1007/s12633-020-00408-2.

[30] S. R. Saddapalli and B. R. Nistala, “The analog/RF performance of a strained-Si graded-channel dual-material double-gate MOSFET with interface charges,” Journal of Computational Electronics, no. September, pp. 1–11, 2020.

[31] Z. Hong, A. Bodkhe, and S. Tzeng, “Method for Forming A Low Resistivity Tungsten Silicide Layer for Metal Gate Stack Applications,” 2014.

[32] S. K. Mah, I. Ahmad, P. J. Ker, and Z. A. Noor Faizah, “High-k Dielectric Thickness and Halo Implant on Threshold Voltage Control,” Journal of Telecommunication, Electronic and Computer Engineering, vol. 10, no. 2, pp. 1–5, 2018.

[33] K. E. Kaharudin, Z. A. F. M. Napiah, F. Salehuddin, and A. S. M. Zain, “Performance analysis of ultrathin junctionless double gate vertical MOSFETs,” Bulletin of Electrical Engineering and Informatics, vol. 8, no. 4, pp. 1268–1278, 2019, doi: 10.11591/eei.v8i4.1615.

[34] Silvaco, “Silvaco ATLAS manual Device Simulation Software,” 2006.

[35] F. Ana and Najeeb-ud-din, “Gate Workfunction Engineering for Deep Sub-Micron MOSFET’s: Motivation, Features and Challenges,” International Journal of Electronics & Communication Technology, vol. 2, no. 4, pp. 29–35, 2011.

[36] H. Awasthi, N. Kumar, V. Purwar, and R. Gupta, “Impact of Temperature on Analog/RF Performance of Dielectric Pocket Gate-all-around (DPGAA) MOSFETs,” Silicon, no. July, pp. 1–5, 2020, doi: 10.1007/s12633-020-00610-2.

[37] J. Ajayan, D. Nirmal, K. Dheena, and P. Mohankumar, “Investigation of impact of gate underlap/overlap on the analog/RF performance of composite channel double gate MOSFETs,” Journal of Vacuum Science & Technology B, vol. 37, no. 6, p. 062201, 2019, doi: 10.1116/1.5116199.

[38] C. K. Pandey, D. Dash, and S. Chaudhury, “Improvement in analog/RF performances of SOI TFET using dielectric pocket,” International Journal of Electronics, vol. 107, no. 11, pp. 1844–1860, 2020, doi: 10.1080/00207217.2020.1756439.

[39] P. K. Verma and S. K. Gupta, “An Improved Analog/RF and Linearity Performances with Small-Signal Parameter Extraction of Virtually Doped Recessed Source/Drain Dopingless Junctionless Transistor for Radio-Frequency Applications,” Silicon, no. June, pp. 1–21, 2020, doi: 10.1007/s12633-020-00518-x.

[40] N. Yadava and R. K. Chauhan, “Impact of Different Gate Metals on the RF Performance of Gallium Oxide MOSFET,” ECS Journal of Solid State Science and Technology, vol. 9, no. 5, pp. 055011, 2020.

[41] C. Sahu and J. S. Pamar, “Analog/RF Performance Comparison of Junctionless and Dopingless Field Effect Transistor,” in International Conference on Computer, Communications and Electronics, 2017, pp. 606–611, doi: 10.1109/COMPELIX.2017.8004041.

[42] F. Salehuddin, K. E. Kaharudin, A. S. M. Zain, A. K. M. Yamin, and I. Ahmad, “Analysis of process parameter effect on DIBL in n-channel MOSFET device using L27 orthogonal array,” International Conferences on Fundamental and Applied Sciences, AIP Conf. Proc., vol. 1621, no. 1, 2014, pp. 322–328, doi: 10.1063/1.4898486.

[43] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, and A. F. Roslan, “Optimal design of junctionless double gate vertical MOSFET using hybrid Taguchi-GRA with ANN prediction,” Journal of Mechanical Engineering and Sciences, vol. 13, no. 3, pp. 5455–5479, 2019, doi: 10.15282/jmes.13.3.2019.16.0442.

[44] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, and A. F. Roslan, “Predictive Analytics of CIGS Solar Cell using a Combinational GRA-MLR-GA Model,” Journal of Engineering Science and Technology, vol. 15, no. 4, pp. 2823–2840, 2020.
BIOGRAPHIES OF AUTHORS

K. E. Kaharudin received Ph.D in Electronic Engineering and M. Eng degree in Computer Engineering from Technical University of Malaysia Melaka (UTeM), in 2017 and 2013 respectively. His Ph.D project focused on the process optimization of vertical double gate MOSFET. His research’s interests include CMOS design, microelectronics, semiconductors, engineering optimization and artificial intelligence. Recently, his efforts emphasize on modeling of Junctionless MOSFET, silicon-on-insulator (SOI) MOSFET, high-k/metal-gate stack technology, solar cells, design of experiment (DoE) and AI-based optimization approaches.

F. Salehuddin received the B.Sc. degree in electrical engineering (Communication) from Universiti Teknologi Mara (UiTM), Malaysia in 2001 and the M.Sc. degree in Electrical, Electronic and System Engineering from Universiti Kebangsaan Malaysia, in 2003. She received the Ph.D. degree in Microelectronics Engineering from Universiti Tenaga Nasional (UNITEN), Malaysia in 2012. She joined Universiti Teknikal Malaysia Melaka (UTeM) in December 2001 as a tutor and is currently a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), UTeM. Her research interest includes process and device simulation of nanoscale MOSFET devices, advanced CMOS design and optimization approach (DOE).

A. S. M. Zain received the B.Eng degree in electrical, Electronic and System engineering and M. Sc in Microelectronics from National University of Malaysia (UKM), Malaysia. She received the Ph.D. degree in Nanoelectronics Engineering from University of Glasgow, UK in 2013. She is currently working as a senior lecturer at Faculty of Electronic and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM). Her research interest includes Nanoscale Device Design and Simulation, Variability and Reliability of Emerging Technology Devices, IC Design for Biomedical Applications.

Ameer F. Roslan received the B.Sc. Degree in Telecommunication Engineering from Technical University of Malaysia Melaka (UTeM), in 2017. He is currently pursuing his M.Sc. degree in electronics and doing research on the DG-FinFET device at Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Technical University of Malaysia Melaka (UTeM). His research interest includes the DG-FinFET architecture and statistical optimization.

I. Ahmad received the B.Sc. degree in Physics in 1980 from Universiti Kebangsaan Malaysia (UKM). He received the M.Sc. degree in Nuclear Science and Analytical Physics from UKM and University of Wales respectively, in year of 1991 and 1992. He received the Ph.D. degree in Electrical, Electronic and System Engineering from UKM in 2007. He joins the Department of Electrical, Electronic and System Engineering, UKM as a lecturer in 1997 to 2002, and as Associate Professor from 2002 to 2007. He involved in several management and technical positions with MINT, MIMOS and UKM. He is currently a Professor with the Department of Electronics and Communication Engineering, Universiti Tenaga Nasional, Malaysia. He is a senior member of the Institute of Electrical and Electronics Engineers (Senior MIEEE).