Compensation of dynamic nonlinear mismatches in time-interleaved analog-to-digital converter

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Abstract This paper introduces a structure for Compensation of dynamic nonlinear mismatches in time-interleaved analog-to-digital converter (TIADC). The basic idea of the proposed compensation structure is to reconstruct error signal and then subtract the reconstructed error from the output signal of TIADC. The compensation performance can be improved progressively by cascading compensation structure. We also proposed the real-valued compensation structure, which is suitable for implementation in hardware.

Keywords: time-interleaved analog-to-digital converter, dynamic nonlinear mismatches, Volterra series, compensation, real-valued

Classification: Circuits and modules for electronic instrumentation

1. Introduction

In recent years, the general trend in modern telecommunication and radar is pushing the analog-to-digital converter (ADC) to higher sampling rate [1, 2, 3]. To increase the sampling rate of an ADC beyond a certain process technology limit, time-interleaved ADC (TIADC) is proposed to meet the fast growing requirements for these applications [4, 5]. However, TIADC is sensitive to mismatches among sub-ADCs, which can significantly degrade the system performance [5, 6].

During the last few decades, much effort has been devoted to offset, gain, time and frequency mismatches in TIADC system [4, 5, 6, 7, 8, 9, 10, 11, 12]. The effects of these mismatches have been investigated extensively by researchers [6, 7, 8, 9]. Numerous estimation and compensation methods for these mismatches have been proposed in the literature [8, 9, 10, 11, 12]. In recent years, there has been an increasing interest in nonlinear mismatch problems in TIADC system [13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24] since nonlinear behaviors are becoming serious as the input frequency increases [25]. The nonlinear distortions in TIADC system are originated from switch-induced charge injection and input signal dependent switch on-resistance [25].

However, most existing studies are focused on static nonlinear errors of TIADC [13, 14, 15, 16, 17, 18, 19] and there are few papers address dynamic nonlinearities in TIADC [19, 20, 21, 22, 23, 24]. In [21], a joint blind compensation method is proposed to calibrate dynamic nonlinear mismatches in TIADC, which uses normalized least-mean square algorithm to estimate and compensate for nonlinear mismatch errors. The price paid for this background method is the requirements for the input signal bandwidth and this requirements can not always be satisfied in practical situations. A polyphase nonlinear equalizer based on Volterra series is proposed in [20], which is capable of simultaneously mitigating linear and nonlinear mismatch errors. However, the calibration involves numerous complex number computations, which consumes large amounts of hardware resources.

In this paper, a behavioral model based on Volterra series is proposed to model the dynamic nonlinearities in TIADC system. Volterra series is one of the most well-established model in nonlinear modeling problem and is gaining widespread popularity in many fields [26, 27, 28, 29, 30].

We introduce a digital post compensation structure for the proposed model to compensate dynamic nonlinear mismatches in TIADC. The basic idea of the proposed compensation structure is to reconstruct error signal and then subtract the reconstructed error from the output signal of TIADC. The major advantage of the proposed compensation structure is that the compensation performance would be progressively improved by cascading compensation structure. Then we propose the real-valued compensation structure, which avoids the computation of complex numbers. Thus the proposed compensation structure is suitable for implementation in hardware, which is capable of utilizing filters in FPGA (Field Programmable Gate Array) directly.

The rest of this paper is structured as follows. In section 2, the nonlinear behavioral model of TIADC based on Volterra series is established. In section 3, the compensation structure of dynamic nonlinearities in TIADC system is proposed. Section 4 introduces the real-valued compensation structure. The simulation results is provide in section 5. Finally, Section 6 concludes the paper.

2. Nonlinearity mismatches in time-interleaved ADCs

Fig. 1 shows a simplified block diagram of an M channel time-interleaved ADC. Each channel converts analog input signal $x(t)$ every $MT_s$ with sampling clocks $CLK_0$-$CLK_{M-1}$ generated by clock management unit. The digital streams from M sub-ADCs are multiplexed to form the final digital output with a sampling rate of $f_s$, ($f_s = 1/T_s$).
Suppose that $x(t)$ is a band-limited signal, which fulfills

$$X(j\Omega) = 0, \quad 0 \leq \Omega_0 \leq |\Omega|, \quad \Omega_0 \leq \frac{\pi}{T_s} \quad (1)$$

Then we can establish a discrete-time model for TIADC system based on Volterra series [23, 24]. An $M$ channel TIADC nonlinear behavioral model with Volterra series is depicted in Fig. 2(a). The input signal $x(n)$ passes through the $m$th channel discrete-time Volterra series $V_m[\cdot]$ followed by a multiplication by an impulse train $s_m(n)$ to get the output $y_m(n)$ ($m = 0, \ldots, M - 1$), which is given by

$$y_m(n) = V_m[x(n)] \cdot s_m(n) \quad (2)$$

with

$$s_m(n) = \sum_{k=-\infty}^{\infty} \delta(n - m - kM), \quad m = 0, \ldots, M - 1 \quad (3)$$

where $\delta(n)$ is the Dirac-delta function.

The expression for $m$th channel discrete-time Volterra series $V_m[x(n)]$ is

$$V_m[x(n)] = \sum_{p=0}^{P} \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} h_{m,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} x(n - k_i) \quad (4)$$

where $P$ is the order of the nonlinear system, and $h_{m,p}(k_1, \ldots, k_p)$ is the $p$th order Volterra kernel for $m$th channel sub-ADC. It can be assumed that Volterra kernels are symmetric without any loss of generality, that is, $h_{m,p}(k_1, \ldots, k_p)$ remains unchanged when permuting the order of $k_1, \ldots, k_p$ [27].

Then the final digital output $y(n)$ can be obtained by adding the outputs of $M$ channels, which is given by

$$y(n) = \sum_{m=0}^{M-1} y_m(n) \quad (5)$$

The Dirac-delta function in (3) can be transformed using Poisson summation formula. The Poisson summation formula is expressed as [31]

$$\sum_{k=-\infty}^{\infty} \delta(n - kM) = \frac{1}{M} \sum_{k=-\infty}^{\infty} e^{j2\pi kn/M} \quad (6)$$

By substituting $n$ for $n - m - kM$, (3) can be expressed as

$$s_m(n) = \sum_{k=-\infty}^{\infty} \delta(n - m - kM) = \frac{1}{M} \sum_{k=0}^{M-1} e^{j2\pi k(n-m)/M} \quad (7)$$

Then we obtain the discrete-time equivalent model of TIADC as Fig. 2(b). The output of TIADC is thus expressed as

$$y(n) = \sum_{m=0}^{M-1} y_m(n) = \frac{1}{M} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} e^{j2\pi k(n-m)/M} V_m[x(n)]$$

$$= \frac{1}{M} \frac{M-1}{M-1} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} \sum_{p=0}^{P} \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} e^{j2\pi k(n-m)/M}$$

$$\cdot h_{m,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} x(n - k_i) \quad (8)$$

### 3. Compensation structure

In this section, the digital post compensation structure is proposed to calibrate nonlinear distortions in TIADC system. By dividing TIADC output into two parts, (8) can be rewritten as

$$y(n) = x(n) + e(n) \quad (9)$$
where \( e(n) \) is the error signal caused by nonlinear behaviors in TIADC system, which is given by

\[
e(n) = \frac{1}{M} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} e^{j2\pi k(n-m)/M} G_m[x(n)]
\]

\[
= \frac{1}{M} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} \sum_{p=0}^{\infty} \sum_{k_1=-\infty}^{\infty} \ldots \sum_{k_p=-\infty}^{\infty} e^{j2\pi k(n-m)/M} \\
\cdot f_{m,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} x(n-k_i)
\]

with

\[
f_{m,p}(k_1, \ldots, k_p) = \begin{cases} 
   h_{m,p}(k_1, \ldots, k_p) - 1, & p = 1, k_p = 0 \\
   h_{m,p}(k_1, \ldots, k_p), & \text{otherwise}
\end{cases}
\]

and

\[
G_m[x(n)] = \sum_{p=0}^{\infty} \sum_{k_1=-\infty}^{\infty} \ldots \sum_{k_p=-\infty}^{\infty} f_{m,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} x(n-k_i)
\]

The basic idea of compensation structure is to reconstruct the error signal \( e(n) \), and then subtracts the reconstructed error signal \( \hat{e}(n) \) from TIADC output \( y(n) \) to get the calibrated output \( \hat{y}(n) \).

For explanation, we begin by assuming that input signal \( x(n) \) is known. If \( x(n) \) is known, the reconstructed error \( \hat{e}(n) \) is equal to \( e(n) \) as given in (10). Then the calibrated output \( \hat{y}(n) \) is equal to \( x(n) \). However, knowing \( x(n) \) would not require a reconstruction system and in practice only the TIADC output \( y(n) \) is available. Thus, the compensation structure uses \( y(n) \) to replace \( x(n) \) to get the reconstructed signal \( \hat{e}(n) \), which is given by

\[
\hat{e}(n) = \frac{1}{M} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} e^{j2\pi k(n-m)/M} G_m[y(n)]
\]

\[
= \frac{1}{M} \sum_{m=0}^{M-1} \sum_{k=0}^{M-1} \sum_{p=0}^{\infty} \sum_{k_1=-\infty}^{\infty} \ldots \sum_{k_p=-\infty}^{\infty} e^{j2\pi k(n-m)/M} \\
\cdot f_{m,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} [x(n-k_i) + e(n-k_i)]
\]

Then the calibrated output \( \hat{y}(n) \) can be obtained by

\[
\hat{y}(n) = y(n) - \hat{e}(n)
\]

The compensation structure is shown in Fig. 3. Since we use \( y(n) \) as the input of compensation structure, the calibrated output \( \hat{y}(n) \) would be slightly different from the input signal \( x(n) \). For a reasonably designed and implemented TIADC, the energy of \( e(n) \) is much lower than the input signal, which guarantees the effectiveness of the proposed compensation structure.

We can further improve the calibration performance by cascading the compensation structure as in Fig. 4. In the first stage, the input to the compensation structure is \( y(n) \) and we get the first stage calibrated output \( \hat{y}_1(n) \). Since the energy of \( e(n) \) is much lower than input signal, \( \hat{y}_1(n) \) is a better approximation of \( x(n) \) compared to \( y(n) \). The \( \hat{y}_1(n) \) is thus selected as the input to the second stage of the same compensation structure to get the second stage calibrated output \( \hat{y}_2(n) \), and so on. By cascading compensation structure, the compensation performance would be progressively improved, which is a major advantage of the proposed method.

4. Real-valued compensation structure

Although compensation structure proposed in section 3 can compensate nonlinear and nonlinear mismatch errors in TIADC system, it is not suitable for practical situations. The digital compensation structures for TIADC system are generally implemented in FPGA (Field-Programmable Gate Array), which can only deal with real-valued number. Even though the input \( y(n) \) and output \( \hat{y}(n) \) are real-valued signal, the complex \( e^{j2\pi k(n-m)/M} \) would introduce computation of complex numbers. Thus, in this section, we propose the real-valued compensation structure.

By changing the summation order \( k \) and \( m \) in (13), the reconstructed signal can be re-expressed as

\[
\hat{e}(n) = \sum_{k=0}^{M-1} e^{j2\pi k/n/M} \sum_{p=0}^{\infty} \sum_{k_1=-\infty}^{\infty} \ldots \sum_{k_p=-\infty}^{\infty} \\
F_{k,p}(k_1, \ldots, k_p) \prod_{i=1}^{p} y(n-k_i)
\]

where

\[
F_{k,p}(k_1, \ldots, k_p) = \frac{1}{M} \sum_{m=0}^{M-1} f_{m,p}(k_1, \ldots, k_p) e^{j2\pi k/m/M}
\]
It can be seen from (15) that $F_k$ is the discrete Fourier transform (DFT) of the compensation parameters $f_m,k(1,\cdots,k_p)$. Then, $F_{M-k}$ can be expressed as

$$F_{M-k}(k_1,\cdots,k_p) = \frac{1}{M} \sum_{m=0}^{M-1} f_m,k(1,\cdots,k_p)e^{j2\pi m/kM}. \quad (17)$$

Since the compensation parameters $f_m,k(1,\cdots,k_p)$ are real-valued number according to (11), we can obtain

$$F_{k,p}(k_1,\cdots,k_p) = F_{M-k}(k_1,\cdots,k_p) \quad (18)$$

where $x^*$ denotes the complex conjugation of $x$.

Splitting $F_{k,p}(k_1,\cdots,k_p)$ into the real and imaginary part as

$$F_{k,p}(k_1,\cdots,k_p) = F_{k,p}^R(k_1,\cdots,k_p) + jF_{k,p}^I(k_1,\cdots,k_p) \quad (19)$$

Assume $M$ is an even number, we can rewrite (14) as

$$\hat{e}(n) = \sum_{p=0}^{M/2-1} \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} \left\{ F_{0,p}^R(k_1,\cdots,k_p) \prod_{p=1}^{p} y(n-k_i) ight\} + \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} \left\{ F_{0,p}^I(k_1,\cdots,k_p) \prod_{p=1}^{p} y(n-k_i) \cos(2\pi kn/M) \right\}$$

$$+ \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} \left\{ F_{0,p}^I(k_1,\cdots,k_p) \prod_{p=1}^{p} y(n-k_i) \sin(2\pi kn/M) \right\}$$

$$+ \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} \left\{ F_{0,p}^R(k_1,\cdots,k_p) \prod_{p=1}^{p} y(n-k_i) (-1)^p \right\}$$

Then the calibrated output $\hat{y}(n)$ can be obtained by subtracting $\hat{e}(n)$ from TIADC output $y(n)$ as

$$\hat{y}(n) = y(n) - \hat{e}(n) \quad (20)$$

Define

$$Q_m^R[x(n)] = \sum_{p=0}^{M/2-1} \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} F_{0,p}^R(k_1,\cdots,k_p) \prod_{p=1}^{p} x(n-k_i) \quad (21)$$

$$Q_m^I[x(n)] = \sum_{p=0}^{M/2-1} \sum_{k_1=-\infty}^{\infty} \cdots \sum_{k_p=-\infty}^{\infty} F_{0,p}^I(k_1,\cdots,k_p) \prod_{p=1}^{p} x(n-k_i) \quad (22)$$

for $m = 0,\cdots,M/2$. For $m = 0$ and $M = M/2$, $Q_m^R[x(n)] = Q_m^I[x(n)]$, which denotes as $Q_0[x(n)]$ and $Q_2[x(n)]$.

The diagram of the real-valued compensation structure is shown in Fig. 5. The performance of real-valued compensation structure can also be improved by cascading more stage as in Fig. 4.

5. Simulation results

To verify the effectiveness of the proposed compensation structure, the numerical simulations with MATLAB is performed in this section. We use a four channel TIADC model based on Volterra series to model the dynamic nonlinearities in TIADC system. For a reasonably designed TIADC, the second and third order terms are the dominant nonlinear distortions. Thus, we use third order Volterra series with memory two to represent the nonlinearities in TIADC system. The sampling rate of the TIADC is set as 1GSPS.

Define $m$th channel Volterra kernel vectors as $h_m = [h_{m,0}^T,\cdots,h_{m,3}^T]^T$, where $h_{m,0}$ corresponds to the coefficients associated with the $p$th order Volterra kernel of $m$th channel sub-ADC. The coefficients for four channel are defined as $h_0 = [-0.021, 0.096, 0.006, 0.022, 0.014, -0.006, -0.033, 0.015, -0.003, 0.006]^T$, $h_1 = [-0.032, 1.033, 0.013, 0.021, 0.012, -0.005, -0.035, 0.018, 0.003, -0.010]^T$, $h_2 = [0.025, 1.012, -0.011, 0.018, 0.008, -0.012, -0.025, -0.003, -0.011, 0.005]^T$, $h_3 = [0.010, 0.983, -0.005, 0.023, 0.005, -0.008, -0.028, 0.013, 0.005, -0.011]^T$, respectively. We have considered the symmetric property of Volterra kernels.

5.1 Example 1

In example 1, we adopt a sinusoidal signal with frequency 110 MHz as the input signal. The spectra of the TIADC output without compensation is shown in Fig. 6. As can be seen from the spectrum, there are numerous spurious tones in the TIADC output apart from input signal. The SFDR (spurious-free dynamic range) before calibration is only 33.14 dB.

Fig. 7 shows the spectrum of the calibrated output signal with one, two and three stages using the proposed real-valued compensation structure. It can be seen from the spectrum, the performance of the compensation structure can be progressively improved by cascading more stage. The SFDR of the calibrated signal after one, two and three stages are 54.90 dB, 74.88 dB and 94.13 dB, respectively. Thus, it can be concluded that the proposed compensation structure is effective for narrow-band signal.
5.2 Example 2

The TIADC model used in the simulation is a dynamic nonlinear model based on Volterra series. Compared with static model, the fundamental difference is that the system is dependent on frequency. Thus, in example 2, we use a wide band signal to testify the validity of the proposed compensation structure. We adopt a multi-tone signal as the input of the TIADC system, which is composed of 21 sinusoids with uniform amplitude and equal space frequencies from DC to $0.8\pi$.

The spectrum of input and output signal of TIADC is shown in Fig. 8. It can be seen from the spectrum that the nonlinearities of TIADC degrade the performance of the system significantly, which is much more serious than single sinusoids in example 1. The SFDR before compensation is 27.24 dB for multi-tone signal.

The spectrum of the output signal after calibration is shown in Fig. 9. The SFDR after compensation are increased to 58.12 dB, 81.84 dB and 95.67 dB after applying one, two and three stage real-valued compensation structure. It can be seen that the proposed compensation structure is also applicable for wide-band signal, which shows the generality of our proposed compensation structure.

6. Conclusion

In this paper, we present the compensation method for dynamic nonlinear mismatches in TIADC. The real-valued compensation structure is suitable for implementation in hardware, which is capable of utilizing filters in FPGA directly. Simulation results verify the effectiveness of the proposed algorithm for both narrow-band signal and wide-band signal.

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