Silicon Drift Detector Readout Electronics for a Compton Camera

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Abstract

A prototype detector for Compton camera imaging is under development. A monolithic array of 19 channel Silicon drift detector with on-chip electronics is going to be used as a scatter detector for the prototype system. Custom designed analog and digital readout electronics for this detector was first tested by using a single cell Silicon drift detector. This paper describes the readout architecture and presents the results of the measurement.

Key words: Compton Camera, Silicon Drift Detector, emitter follower, readout electronics, data acquisition

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1 Introduction

Since the introduction of the Compton imaging principle [1], Compton cameras found a number of applications [2],[3],[4] and several prototype detectors have

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been produced. The prototype system under development which is discussed here [5] is going to be used for studying the application in medical imaging.

The principal idea of the Compton camera is to replace the mechanical collimator of an Anger camera with an electronic collimator. The Compton camera consists of two detector components: the so called scatter detector and the absorption detector. A photon emitted from a source undergoes Compton scattering at the scatter detector where the recoil electron is absorbed and its energy and the location of interaction are determined. The scattered photon leaves the scatter detector and is absorbed in the second detector where the energy and impact position are determined. From this information the source of the incident photon is found to be on the surface of a cone; the so called backprojected cone.

Silicon was found to be the best material for the scatter detector [6] considering its high Compton to total interaction ratio at the gamma energy of interest (several hundred keV). The prototype will consist of a Silicon Drift Detector (SDD)[7] as the scatter detector and an Anger camera without lead collimator as the absorption detector. The Silicon detector is a monolithic array of 19 cells with an on-chip JFET for the first amplification in every cell. It has been produced by the Max Planck Institute semiconductor laboratory (MPI/HLL). This paper presents the fast frontend and readout electronics designed for this detector and the test results which were obtained with a single cell detector of the same type.

2 Setup Overview

The single cell detector has an area of 5 mm$^2$ and it has a circular shape. The thickness of the wafer is 300 µm. The mounting of the detector on a ceramic support and the bonding were done at MPI/HLL. The detector leakage current was around 100 pA. The operational principle of this detector has been explained in several publications elsewhere [8]. The most significant feature of this detector is the on-chip integrated JFET which serves to reduce the stray capacitance and therefore provides a better noise performance compared to other Silicon detectors. This detector type has been used for several applications such as a scintillator based gamma-camera [9], holography [10], and spectrometry [11]. Our prototype Compton camera will exploit the new possible application field for it.
2.1 Readout Architecture

The standard readout architecture for the SDD consists of a source follower with a source load of a constant current supply and the detector signal is amplified at a voltage-sensitive preamplifier, and then further filtered with a shaper. The transconductance ($g_m$) of an n channel on-chip JFET is about 0.3 mS and the time constant $\tau = \frac{1}{g_m} \cdot C_{total}$ produces a rise time of $2.2 \cdot \tau$ which is of the order of 300 ns. For the Compton camera application it is important to have fast trigger signals from the first detector. This can be done by a readout of the back side of the detector which is under research at MPI. Our implementation of the readout architecture is shown in Fig 1. Emitter followers were used for gas proportional counters as low noise preamplifiers [12]. In addition to the source-follower at the SDD chip, an emitter follower provided certain advantages. First of all, the signal after the emitter-follower stage becomes more immune to additional stray capacitances. The readout electronics can be placed further away from the detector, provided that the emitter-follower is as near as possible to the detector. Furthermore, the rise time of the preamplified signal decreases considerably, which makes the use of a short shaping time ($<100$ ns) possible. The driver transistor for the emitter follower was chosen to be a bipolar junction transistor. The selection of this transistor is based on a dynamic range, a noise contribution and an input capacitance. Fig 2 shows the preamplifier output with and without emitter follower between the detector and the preamplifier. The detector was irradiated by a $^{55}$Fe source. The rise time of the signal reduces almost by a factor of 5 with the emitter follower.
2.2 Preamplifier

The preamplifier is a modified version of a preamplifier which was used for one of the first prototype SDDs [13]. The gain of the preamplifier is approximately the ratio between the injection capacitor at the input and the feedback capacitor. The voltage step at the output of the preamplifier decays with a time constant of $R_f \cdot C_f = 100\mu s$.

10 channels of the preamplifier have been implemented on a hybrid board by using a thick film technology. (fig 3). The power consumption per channel is around 130$mW$ according to the SPICE simulations. The deviation from linearity of the preamplifier for one channel is shown in Fig 4a. The measurement was done by applying a voltage step at the input of the preamplifier and measuring the output of it. The average voltage gain is around 15. In Fig 4b the equivalent noise charge (ENC) of the preamplifier as a function of a shaping time is shown. The preamplifier output was connected to a spectroscopy amplifier (model 1413) for performing the noise measurements. The ENC was calculated for an input capacitance of 1 pF. The peak noise voltage of the preamplifier/shaper system was measured with an analog oscilloscope recording the peak-to-peak amplitude at a very low trigger rate ($\leq 100Hz$) and this level corresponds to four to five standard deviations. The re-
results obtained by this method were also confirmed with a digital oscilloscope’s (LeCroy 9362) standard deviation measurement. The ENC values are given in rms electron/pF units which translate into 2-4 rms electrons for 300 fF of detector capacitance. So, the noise contribution of this low noise preamplifier to the whole detector and readout system is expected to be very small.

Fig. 4. a) Percent deviation from linearity for the first preamplifier channel b) Noise figure for the preamplifier channels

2.3 Shaper

An in house developed hybrid shaper was used for the measurements. The shaper is a CR-RC shaper with adjustable pole-zero cancellation and gain. The hybrid board has two shaper channels and 10 of these boards will be used for the 19-cell SDD setup.

Fig. 5. Block diagram of the shaper

The block diagram of the shaper is shown in Fig 5. There is a differential amplifier with variable gain(g) at the first stage. It is followed by a pole-zero(pz) filter and an integrator(int). The waveforms from the shaper, as shown in Fig 6, demonstrate reasonably symmetrical differential outputs on a load of 50 Ω.
Fig. 6. Shaper output with SDD irradiated by $^{55}\text{Fe}$. The upper waveforms are the positive and the negative outputs. Below is the resulting waveform when the difference is taken.

Certain aspects were taken into account when choosing the appropriate shaping time. The rise time of the preamplified signal is about 60 ns. The shaping time should not be much shorter than this value in order to avoid ballistic deficit. The sampling rate of the ADC system is 66 MHz and at least 4 samples should be taken at the region of highest signal to noise ratio. The leakage current of this detector is not the dominating factor, therefore the energy resolution improves with an increasing shaping time. However, it can not be made very long, since we need fast signals. Considering these constraints a peaking time of 100 ns was chosen.

### 2.4 Data Acquisition System

A custom-designed data acquisition (DAQ) system has been developed for the Compton camera prototype [14], [15]. It consists of channel processors, an event builder and a bus which transfers the data between the channels processors and the event builder. Only one channel of one of the channel processor cards is used for the measurements done with one-cell SDD. The channel processor card is connected to a parallel port interface card and the data are transferred to a computer via this interface. The architecture of the channel processor is shown in Fig 7.

The signals arrive first at the channel processor which has both analog and
Fig. 7. Data Acquisition for the SDD
digital sections. The analog part receives the differential signals, sends them
to an ADC and the digitized signals are processed by a Xilinx FPGA. At
the FPGA necessary operations such as peak finding, integration and time
 stamping are applied. The ADCs have as mentioned, 66 MHz of sampling
rate and 12 Bit resolution. System performance tests show that the effective
resolution is around 11 Bit. Each processed signal reaches the interface board
and is transferred to a PC.

3 Spectroscopic Measurements

The spectroscopic measurements were done by using the analog and digital
readout electronics described at the previous chapters. The differential shaper
output is connected to one channel of the single channel processor card. The
channel processor is connected to an interface card and the digitized signal is
transferred to a PC via parallel port connection. Several bias voltages needed
for the SDD are supplied by a custom-designed power supply.

The first measurements were done by using a $^{55}$Fe source. The spectrum is
shown in Fig. 8a, where both Mn K$_\alpha$ and K$_\beta$ peaks can be seen clearly. The
equivalent noise charge (ENC) is about 33 rms electrons which includes noise
contributions from the detector and the electronics. Fig 8b shows the energy
resolution at 5.9 keV as a function of a shaping time. The FWHM value is
about 250 eV at a shaping time of 250 ns and increases with longer shaping
times.

The aim of the Compton camera project is to be able to use high energetic
radionuclides, preferably at least few hundred keV and more. Therefore, it
is interesting to study the performance of the SDD with a radioactive source
emitting higher energetic photons. The spectraus obtained with $^{109}$Cd and
Fig. 8. a) $^{55}$Fe spectrum b) Energy resolution as a function of a shaping time

$^{133}$Ba sources are shown in Fig. 9. The counts are multiplied by 10 for energies above 35 keV in order to see the peaks more clearly.

Fig. 9. $^{109}$Cd and $^{133}$Ba spectrums obtained with SDD
4 Conclusion

A multi-channel silicon drift detector is going to be used as a scatter detector of a Compton camera prototype. The complete chain of analog and digital readout electronics for the SDD has been tested by using a single cell SDD. Faster readout has been obtained by using an emitter follower stage immediately after the on-chip FET of the detector. A low noise hybrid voltage preamplifier and a CR-RC hybrid shaper have been used. The data acquisition was done by using a custom-designed FPGA based readout system. An ENC of 33 rms electron of the overall system has been measured by using a shaper with a rise time of 100 ns.

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