Understanding the Input Signal Frequency Effects on the Resistive Window of Memristors

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Abstract—As theoretically predicted by Prof. Chua, the input signal frequency has a major impact on the electrical behavior of memristors. According to one of the so-called fingerprints of such devices, the resistive window, i.e., the difference between the low and high resistance states, shrinks as the frequency increases for a given input signal amplitude. Physically, this effect stems from the incapability of ions/vacancies to follow the external electrical stimulus. In terms of the electrical behavior, the collapse of the resistive window can be ascribed to the shift of the set/reset voltages toward higher values. Moreover, for a given frequency, the resistance window increases with the signal amplitude. In this letter, we show that both phenomena are the two sides of the same coin and that can be consistently explained after considering the snapback effect and a balance model equation for the device memory state.

Index Terms—memristor, resistive switching, frequency.

I. INTRODUCTION

According to [1] and [2], a memristive device exhibits three major fingerprints: i) a pinched hysteresis loop in the current-voltage (I-V) plane, ii) the decrease of the hysteresis lobe area as the input signal frequency increases, and iii) the shrinking of the pinched hysteresis loop to a single-valued function when the frequency tends to infinite. In terms of the resistive switching (RS) mechanism, the latter two points can be understood as the mutual approach of the low (LRS) and high (HRS) resistance states as the frequency increases. Not only the signal frequency takes part in this problem but also its amplitude needs to be considered. As is well known, for a fixed frequency, the magnitude of the hysteretic current-voltage (I-V) loop increases as the signal amplitude increases (see Fig. 1(a)). In practice, the transitions occur at two voltage levels often referred to as the set ($V_S$) and reset ($V_R$) voltages which are regarded as fixed values [3]. Similarly, the I-V loop increases as the signal frequency decreases (see Fig. 1(b)) and for a very high frequency, the I-V curve collapses to a purely resistive behavior. The ratio between the LRS and HRS currents measured at a low fixed bias is referred to as the resistive window of the device and when properly normalized to unity as its memory state window. Then, one can talk about the collapse of the memory window when the input signal amplitude is decreased and the frequency increased [3]-[5]. It is clear that both aspects of the phenomenon have the same root, i.e., the ion/vacancy displacements within the insulating layer and the formation and rupture of an atomic-size conducting bridge in between the electrodes [6]-[8]. Physically, the collapse of the memory window can be attributed to the incapability of ions/vacancies to follow the input signal [9],[10]. Electrically, the effect is linked to the shift of the transition voltages, $V_{TS}$ and $V_{TR}$, toward higher values. These issues have been thoroughly investigated in the past for constant and ramped voltage input signals [11]-[14] but a theoretical approach able to deal with arbitrary input signals is still an almost unexplored terrain.

In this letter, the effects of the input signal frequency and amplitude on the hysteretic I-V curves of memristive devices are investigated. The memory window collapse is demonstrated for HfO$_2$-based MIM structures. On the basis of Chua’s theory, a simple phenomenological memristor model formed by two coupled equations is proposed. The model takes into account the snapback effect in the I-V characteristic and assumes a dynamic balance-type equation for the memory state of the device. We show that the proposed approach provides a consistent framework for understanding the role played by the signal frequency and amplitude applied to memristors.

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II. DEVICES AND EXPERIMENTAL DETAILS

The devices used in this work are Ti:N(200m)/Ti(10m)/HfO$_2$(10nm)/W(200nm) structures with area 5×5μm$^2$. The input signal was applied to the top electrode with the bottom electrode grounded. Details about the device fabrication and electroforming processes can be found in [12], [13]. Two kinds of ramped voltage experiments were carried out varying specific parameters in each case. In the first experiment (see Fig. 1(c)), the maximum positive voltage amplitude was ranged from 0.4V to 1.1V (RR-0.3V/s) while the maximum negative amplitude was fixed to -1.5V (RR-0.4V/s) in order to induce the complete reset of the device after each cycle. RR is the ramp rate. In the second experiment (see Fig. 1(d)), RR was varied from 1V/s to 10V/s keeping the positive and negative maximum voltage amplitudes fixed to 1.1V and -1.4V, respectively. As illustrated in Figs. 2(a) and 3(a), the median of the I-V curves shown in Figs. 1(c) and 1(d) were corrected for the snapback and snapforward effects (V-I-R$_S$) using a series resistance R$_S$ [15]-[17]. Figure 2(b) shows the dependence of V$_{TR}$ on R$_S$ for the different applied signals. The crossover point indicates the optimum value for R$_S$. Regardless of the signal amplitude, the transition voltages are approximately the same (V$_{TS}$=V$_{TR}$=0.5V) for R$_S$=450Ω. Figure 2(c) shows the progressive increase of the memory window with the signal amplitude. In case of the frequency variation, V$_{TS,TR}$ are no longer constant (see Fig. 2(a)) and the cycle-to-cycle variability (C2C) must be taken into account. Figure 3(b) shows the weibits for the individual V$_T$ and V$_{TR}$ values. Remarkably, both data sets can be fitted using the Burr’s XII (also called clustering) distribution [18]:

$$F(V) = 1 - \left( 1 + \frac{1}{\alpha_{SR}} \left( \frac{V}{V_{TS,TR}} \right)^{\beta_{SR}} \right)^{-\alpha_{SR}} \quad (1)$$

where $F$ is the cumulative distribution function, $\alpha_{SR}$ the clustering, $\beta_{SR}$ the shape, and $V_{TS,TR}$ the scale (transition voltages) parameters for set and reset, respectively. The obtained fitting parameter values are $\beta_{SR}=75$ with $0.35<\alpha_{SR}<2.0$ and $\beta_{SR}=65$ with $0.45<\alpha_{SR}<1.3$. While $\beta$ takes into account the intrinsic C2C variability, $\alpha$ is related to the extrinsic one (different initial conditions for HRS and LRS). Notice that for $\alpha \to \infty$, (1) yields the Weibull distribution. Figures 3(c) and 3(d) show, respectively, that V$_{TS,TR}$ and R$_S$ linearly increase with ln(RR). While the first result is a well-known experimental observation [19], [20], the second one points out that R$_S$ is similarly affected by RR. This is not surprising since both behaviors are ultimately ruled by the same mechanism, i.e. the ion/vacancy displacements [21]. This indicates that R$_S$ or at least part of R$_S$ is associated with the filamentary structure itself [16] and should not be regarded as a completely external artifact [15]. Finally, Fig. 3(e) shows the collapse of the resistive window with RR as predicted by Chua. Notice the asymmetric reduction of the resistive window largely caused by the $R_S$ effect on the LRS current. As it will be discussed next, both effects shown in Figs. 2 and 3 can be interpreted as the two sides of the same coin.

III. MODEL DESCRIPTION AND DISCUSSION

In this Section, a simple phenomenological model which contains all the ingredients necessary to understand the collapse of the resistive window is presented. The first equation, which is related to the electron transport and which accounts for the snapback/snapforward effect discussed above, is expressed as:

$$I(V) = G_C(g)V_C = G_C(g)[V - I(V)/R_S] \quad (2)$$

where $G_C(g)$ is the conduction of the memory state, $V_C$ the voltage drop across this constriction, $V$ the applied voltage, and $g_{min}$ and $g_{max}$ fitting parameters for the minimum and maximum conductances, respectively. From (2), the I-V curve reads:

$$I(V) = \frac{G_C(g)}{1 + G_C(g)R_S/V} \quad (3)$$

(3) expresses that the behavior of the I-V characteristic is dictated by two frequency-dependent factors, $G_C$ and $R_S$. The second equation deals with the memory state of the device [22] and is expressed in terms of the low voltage-normalized conductance $g$ as a symmetric balance model:

$$\frac{dg}{dt} = \frac{V}{\tau_S(V_C)} - \frac{V}{\tau_R(V_C)} \quad (4)$$

where $\tau_S$ and $\tau_R$ are characteristic times associated with the set and
For the sake of simplicity, equation (4) can be represented by the equivalent circuit model shown in Fig. 4(a), where \( g \) is the current flowing through the circuit. The memory state, \( g \), is represented by the current flowing through the RL circuit. Memory state for a sinusoidal signal with increasing amplitude \((f=1\text{Hz})\) and frequency \((V_{\text{AMP}}=1\text{V})\) (c). Typical simulated intrinsic I-V curves (d) for different ramped voltage amplitudes and (e) for different \( RR \). \( f \) Evolution of the memory window, \( \Delta g \), as a function of \( f \) and \( V_{\text{AMP}} \).

reset transitions. Assuming ion/vacancy hopping transport \([23, 24]\):

\[
\tau_{S,R}(V_C) = \tau_{0S,0R} \exp \left( -\frac{|V_C|}{V_{0S,0R}} \right)
\]

where \( \tau_{0S,0R} \) and \( V_{0S,0R} \) are fitting parameters of the model. Remarkably, (4) can be represented by the equivalent circuit model shown in Fig. 4(a), where \( g \) is the current flowing through the circuit. For the sake of simplicity, in what follows, identical \( \tau_{S,R} \) parameters will be considered for both positive and negative biases. Figures 4(b) and 4(c) show the hysteretic behavior of \( g \) for sinusoidal signals with different amplitude and frequency. Notice how the resulting hysterons or memory loops agree with the experimental results reported in Section II. More in detail, Figs. 4(d) and 4(e) illustrate simulated I-V curves using (3) and (4).

Importantly, to our knowledge, analytic results for a time-varying signal in (4) can only be found for the case of a linearly increasing or decreasing positive and negative ramps. Again, for the sake of simplicity, let's consider only the set region of the device. Solving (4) for \( V_C=RRt \), yields the double exponential expression:

\[
g(t) = g_0 - \frac{1}{2} \exp \left( -\frac{V_{0S}}{RR \tau_{0S}} \left[ \exp \left( \frac{RRt}{V_{0S}} \right) - 1 \right] \right) + \frac{1}{2}
\]

where \( g_0=g(t=0) \) is the initial memory condition. Considering the inflection point of (6), \( d^2g/dV_C^2=0 \), as the reference transition voltage, we obtain:

\[
V_{TS} = V_{0S} \ln(RR) + V_{0S} \ln \left( \frac{\tau_{0S}}{\tau_{0S}} \right)
\]

which provides the linear relationship shown in Fig. 3(c). For our devices (HfO\(_2\)), \( V_{0S}=1.3\cdot10^{-2}\text{V} \) and \( \tau_{0S}=2.97\cdot10^7\text{s} \) are obtained. Moreover, for a cycled ramped voltage signal with maximum amplitude \( V_{\text{AMP}} \) and frequency \( f \), \( V_C=V_{\text{AMP}}f-t \), so that from (6) we can look for the initial condition \( g_0 \) required for a stationary loop as \( g(1/4f)=0 \). This simple exercise provides the amplitude of the memory window \( \Delta g \) as a function of \( V_{\text{AMP}} \) and \( f \) (see Fig. 4(f)):

\[
\Delta g = 2g_0 \exp \left\{ \frac{V_{0S}}{4V_{\text{AMP}}f \tau_{0S}} \left[ \exp \left( \frac{V_{\text{AMP}}}{V_{0S}} \right) - 1 \right] \right\} - 1
\]

which, again, is in total agreement with the expected phenomenology for memristive devices.

**IV. CONCLUSIONS**

In this letter, the dependence of the memory state (resistance) window on the input signal amplitude and frequency was investigated. It was shown that the behavior of the I-V characteristic of HfO\(_2\)-based memristors can be understood as the combined action of two frequency-dependent factors, i.e. a series resistance effect and a phase lag effect in the diffusive movement of ions/vacancies.
REFERENCES

[1] L. Chua, “Resistance switching memories are memristors,” Appl. Phys. A, vol. 102, pp. 765-783, Jan. 2011, doi: 10.1007/s00339-011-6264-9.

[2] P. S. Adhikari, M. P. Sah, H. Kim, and L. O. Chua, “Three fingerprints of memristor,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 11, pp. 3008-3021, Jun. 2013, doi: 10.1109/TCSI.2013.2256171.

[3] T. D. Dongale, K. V. Khot, S. V. Mohite, N. D. Desai, S. S. Shinde, V. L. Patil, S. A. Vanalkar, A. V. Moholkar, K. Y. Rajpuro, P. N. Bhosale, P. S. Patil, P. K. Gaikwad, and R. K. Kamat, “Effect of write voltage and frequency on the reliability aspects of memristor-based RRAM,” Int. Nano Lett. vol. 7, pp. 209-216, Aug. 2017, doi: 10.1007/s40089-017-0217-z.

[4] T. Dongale, P. Patil, P. Gaikwad, R. Kamat, “Investigating conduction mechanism and frequency dependency of nanoscale memristor device,” Mat. Sci. Semi. Proc., vol. 38, pp. 228-233, May. 2015, doi: 10.1016/j.mssp.2015.04.033.

[5] J. Eshraghian, S. Kang, S. Baek, G. Orchard, H. Iu, W. Lei, “Analog weights in ReRAM DNN accelerators,” IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), Hsinchu, Taiwan, Taiwan, Mar. 2019, pp. 267-271, doi: 10.1109/AICAS.2019.9078550.

[6] R. Waser, R. Dittmann, G. Saitov and K. Sotz, “Redox-based resistive switching memories-Nanoionics mechanisms, prospects, and challenges,” Adv. Mater. vol. 21, pp. 2632-2663, Jul. 2009, doi: 10.1002/adma.200900375.

[7] S. Larentis, F. Nardi, S. Balatti, D. Ielmini, D.C. Gilmer, “Bipolar- Switching model of RRAM by field- and temperature-activated ion migration,” IEEE International Memory Workshop, Milan, Italy, May. 2012, pp. 1-4, doi: 10.1109/IMW.2012.6236468.

[8] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, G. Bersuker, “Microscopic modeling of HfO2 RRAM operations: From forming to switching,” IEEE Trans. Elec. Dev., vol. 62, no. 6, pp. 1998-2006, Jun. 2015, doi: 10.1109/TED.2015.2418114.

[9] M. Sah, H. Kim, L. Chua, “Brains are made of memristors,” IEEE Circuits and Systems Magazine, vol. 14, no. 1, pp. 12-36, Feb. 2014, doi: 10.1109/mcas.2013.2296414.

[10] K. Campbell, K. Drake, E. Barney Smith, “Pulse shape and timing dependence on the spike-timing dependent plasticity response of ion conducting memristors as synapses,” Front. Bioeng. Biotechnol., vol. 4, pp. 1-11, Dec. 2016, doi: 10.3389/fbioe.2016.00097.

[11] M. Maestro, J. Martin-Martinez, J. Diaz, A. Crespo-Yepes, M. B. Gonzalez, R. Rodriguez, F. Campabadal, M. Nafría, and X. Aymerich, “Analysis of set and reset mechanisms in Ni/HfO2-based RRAM with fast ramped voltages,” Micro. Eng., vol. 147, pp. 176-179, Nov. 2015, doi: 10.1016/j.mee.2015.04.057.

[12] M. Maestro-Izquierdo, M.B. Gonzalez, F. Campabadal, “Mimicking the spike-timing dependent plasticity in HfO2-based memristors at multiple time scales,” Micro. Eng., vol. 215, pp. 111014/1-5, Jul. 2019, doi: 10.1109/mee.2019.111014.

[13] S. Poblador, M.B. Gonzalez, F. Campabadal, “Investigation of the multilevel capability of TiN/Ti/HfO2/W resistive switching devices by sweep and pulse programming,” Micro. Eng., vol. 187-188, pp. 148-153, Feb. 2017, doi: 10.1016/j.mee.2017.11.007.

[14] M. B. Gonzalez, M. Maestro-Izquierdo, F. Campabadal, S. Aldana, F. Jiménez-Molinos, J. B. Roldán, “Impact of intrinsic series resistance on the reversible dielectric breakdown kinetics in HfO2 memristors,” IEEE International Reliability Physics Symposium (IRPS), Dalla, TX, USA, Apr. 2020, pp. 1-4, doi: 10.1109/IRPS45951.2020.9128961.

[15] A. Fantini, J. Wouters, R. Degraeve, L. Goux, L. Pantisano, G. Kar, Y.-Y. Chen, B. Govoreanu, J. A. Kitti, L. Altimime, and M. Jurczak, “Intrinsic switching behavior in HfO2 RRAM by fast electrical measurements on novel 2R test structures,” IEEE 4th International Memory Workshop (IMW), Milan, Italy, May. 2012, pp. 1-4, doi: 10.1109/IMW.2012.623646.

[16] A. Hardtdegen, C. L. Torre, H. Zhang, C. Funck, S. Menzel, R. Waiser, and S. Hoffmann-Effert, “Internal cell resistance as the origin of abrupt reset behavior in HfO2-based devices determined from current compliance series,” IEEE 8th International Memory Workshop (IMW), Paris, France, May. 2016, pp. 1-4, doi: 10.1109/IMW.2016.7495280.

[17] A. Hardtdegen, C. L. Torre, F. Clppers, S. Menzel, R. Waiser, and S. Hoffmann-Effert, “Improved switching stability and the effect of an internal series resistor in HfO2/TiOx bilayer ReRAM cells,” IEEE Trans. Electron Devices, vol. 65, no. 8, pp. 3229-3236, Aug. 2018, doi: 10.1109/TED.2018.2849872.

[18] E. Y. Wu, B. Li, and J. H. Stathis, “Modeling of time-dependent non-uniform dielectric breakdown using a clustering statistical approach,” IEEE Trans. Electron Devices, vol. 103, no. 15, pp. 152907, Oct. 2013, doi: 10.1063/1.4824035.

[19] C. Cagli, D. Ielmini, F. Nardi, and A. L. Lacaita, “Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retractions and disturb prediction,” IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, Dec. 2008, pp. 1-4, doi: 10.1109/IEDM.2008.4796678.

[20] D. Ielmini, “Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth,” IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4309-4317, Dec. 2011, doi: 10.1109/TED.2011.2167513.

[21] S. Ambrogio, S. Balatti, D. C. Gilmer, and D. Ielmini, “Analytical Modeling of Oxide-Based Bipolar Resistive Memories and Complementary Resistive Switches,” IEEE Trans. Elec. Dev., vol. 61, no. 7, pp. 2378-2386, Jul. 2014, doi: 10.1109/TED.2014.2325531.

[22] E. Miranda and J. Suñe, “Memristive State Equation for Bipolar Resistive Switching Devices Based on a Dynamic Balance Model and Its Equivalent Circuit Representation,” IEEE Trans. Nanotechnol., vol. 19, pp. 837-840, Nov. 2020, doi: 10.1109/TNANO.2020.3039391.

[23] C. Cagli, F. Nardi, and D. Ielmini, “Modeling of Set/Reset Operations in NiO-Based Resistive-Switching Memory Devices,” IEEE Trans. Dev. Elec., vol. 56, no. 8, pp. 1712-1720, Aug. 2009, doi: 10.1109/TED.2009.2024046.

[24] E. W. Lim and R. Ismail, “Conduction mechanism of valence change resistive switching memory: A survey,” Electronics, vol. 4, no. 3, pp. 586-613, Sept. 2015, doi: 10.3390/electronics4030586.