Edges vs Circuits: a Hierarchy of Diameters in Polyhedra

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Abstract

The study of the graph diameter of polytopes is a classical open problem in polyhedral geometry and the theory of linear optimization. In this paper we continue the investigation initiated in [4] by introducing a vast hierarchy of generalizations to the notion of graph diameter. This hierarchy provides some interesting lower bounds for the usual graph diameter. After explaining the structure of the hierarchy and discussing these bounds, we focus on clearly explaining the differences and similarities among the many diameter notions of our hierarchy. Finally, we fully characterize the hierarchy in dimension two. It collapses into fewer categories, for which we exhibit the ranges of values that can be realized as diameters.

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1 Introduction

Dantzig’s Simplex method from 1947 and its variations are the most common algorithms for solving linear programs. It can be viewed as a family of combinatorial local search algorithms on the graph of a convex polyhedron. More precisely, the search is done over the graph of the polyhedron, which is composed of the zero- and one-dimensional faces of the feasible region (called vertices and edges). The search moves from a vertex of the graph to a better neighboring vertex joined by an edge.

The (graph) diameter (or combinatorial diameter) of a polyhedron is the diameter of its graph, the length of the longest shortest path among all possible pairs of vertices. Despite great effort of analysis, it remains open whether there is always a polynomial bound on the shortest path between two vertices in the graph (see for example [8]). While trying to understand this well-known problem, the authors of [4] introduced a very natural generalization of the notion of diameter. Here we continue their work by introducing a hierarchy of possible diameter definitions. We will see that the hierarchy includes the traditional graph diameter and the circuit diameter introduced in [4].

In the following we will consider polyhedra of the general form \( P(b, d) = \{ z \in \mathbb{R}^n : Az = b, Bz \leq d \} \) for matrices \( A \in \mathbb{Z}^{m_A \times n}, B \in \mathbb{Z}^{m_B \times n} \). Note that the matrix \( B \) should have full row rank \( n \) for the polyhedron to have vertices and edges. The circuits or elementary vectors associated with matrices \( A \) and \( B \) are those vectors \( g \in \ker(A) \setminus \{0\} \), for which \( Bg \) is support-minimal in the set \( \{ Bz : z \in \ker(A) \setminus \{0\} \} \). The vectors \( g \) are always normalized to have coprime integer components and thus, there are only finitely many such vectors. It can be shown that the set of circuits consists exactly of all edge directions of \( P(b, d) \) for varying \( b \) and \( d \). In particular the circuits provide augmenting directions to any non-optimal solution of \( \min \{ c^Tz : Az = b, Bz \leq d \} \) for any choice of \( b \), \( d \) and \( c \). It should be noted that the circuits are as expected related to the matroid of linear dependences of the matrix \( \begin{pmatrix} A & O \\ B & I \end{pmatrix} \).

Thus by using the circuits as measurement steps for a distance we are allowing for bounds in a family of parametric polyhedra that result from translation of defining hyperplanes.

We remark that circuits have already played a fundamental role in various aspects of the theory of linear optimization (see e.g., [1, 2, 5, 6, 9]). Note also that for a linear program, augmentation along circuit directions is a generalization of the Simplex method: While in the Simplex method one walks only along the graph (so in particular on the boundary) of one polyhedron for fixed \( b, d \), the circuit steps could go through the interior of the polyhedron (but along potential edge directions of other polyhedra in the same parametric family).
Let us now define a very general notion of distance based on circuits. Let \( P \) be a polyhedron and let \( \mathcal{C} \) be the set of circuits for the associated matrices \( A \) and \( B \). For a pair of two vertices \( \mathbf{v}^{(1)}, \mathbf{v}^{(2)} \) of \( P \), we call a sequence \( \mathbf{v}^{(1)} = y^{(0)}, \ldots, y^{(k)} = \mathbf{v}^{(2)} \) a circuit walk of length \( k \) if for all \( i = 0, \ldots, k-1 \) we have \( y^{(i+1)} - y^{(i)} = \alpha_i \mathbf{g}_i \) for some circuit \( \mathbf{g}_i \) and some \( \alpha_i > 0 \). Note that because we are allowing the \( \alpha_i \) to be arbitrary real non-negative numbers there are walks that can be infinite, but we restrict our attention to those that are finite and we can define: The circuit distance from \( \mathbf{v}^{(1)} \) to \( \mathbf{v}^{(2)} \) is the minimum length of a circuit walk from \( \mathbf{v}^{(1)} \) to \( \mathbf{v}^{(2)} \).

We call a circuit walk that realizes the circuit distance a shortest or optimal walk. The circuit diameter of \( P \) is the maximum circuit distance between any two vertices of \( P \).

Our hierarchy will include different notions of circuit distances which arise by considering circuit walks that satisfy additional properties. We write \( P \) for \( P(b, d) \) for fixed \( b \) and \( d \):

- (e) If \( y^{(i)} \) and \( y^{(i+1)} \) are neighboring vertices in the graph of the polyhedron for all \( i = 0, \ldots, k-1 \), we call the walk an edge walk. This is the term that corresponds to the classical graph diameter of a polytope.

- (f) If \( y^{(i)} \in P \) for all \( i = 0, \ldots, k-1 \), then we say the circuit walk is feasible.

- (m) If the extension multipliers \( \alpha_i \) are maximal, i.e. if \( y^{(i)} + \alpha \mathbf{g}_i \) is infeasible (i.e., lies outside \( P \)) for all \( \alpha > \alpha_i \), we say that the walk is of maximum extension length or simply maximal.

- (r) If no circuit is repeated, then we say the walk is non-repetitive.

- (s) If no pair of circuits \( \mathbf{g}_i, -\mathbf{g}_j \) is used, then we say the walk is non-backwards.

In what follows, we consider circuit distances restricted to different combinations of these properties and relate them to each other. A prime example would be the following: In the Simplex method one is limiting augmentation directions to actual edge directions at the current vertex and always choosing maximal augmentations to another vertex. In particular one ensures that the next point on the walk is feasible. Hence such walks satisfy the properties (e), (f) and (m). For several of the distance concepts we present, we liberate ourselves from some of these restrictions: We try to go from \( \mathbf{v}^{(1)} \) to \( \mathbf{v}^{(2)} \) more efficiently by possibly going through the interior of the polyhedron along linear combinations of circuits. We are even willing to leave the feasible region if that may yield fewer steps. Figure 1 depicts some walks for different combinations of these properties.

Figure 1: An edge walk and a feasible maximal walk (first row). A feasible (repetitive) walk and an unrestricted walk (second row).

We now introduce a uniform notation for our discussion. We use \( \mathcal{CD} \) to refer to the circuit distance from \( \mathbf{v}^{(1)} \) to \( \mathbf{v}^{(2)} \) with no further restrictions. When considering only circuit walks
on which we impose some of the above restrictions, we denote these restrictions by small subscript letters as used in the above list of properties. For example $CD_{f,s}$ refers to the feasible sign-compatible circuit distance, where the corresponding walk is feasible and sign-compatible, while $CD_{f,m,r}$ means we have to use a feasible, maximal and non-repetitive walk. To have a simple wording, we call, for example, $CD_{f,m}$ the feasible maximal circuit distance and do the same for all other circuit distances. In addition, we here give explicit names to the four circuit distances that will form the core of our hierarchy:

Note that $CD_{f,m}$ is the classical graph distance in the polytope $P$, while $CD_{f,m}$ corresponds to the original circuit distance as introduced in [4]. Further, we call $CD_f$ the weak circuit distance and $CD$ the soft circuit distance. As we often have to carefully distinguish different types of circuit distance, we stick to identifying them by their properties in many cases, but these four distances are the most fundamental in our work (see Theorem 1 and the central column of Figure 2).

Why are these distances interesting? First, note the graph diameter is bounded (below) by diameters that have much weaker properties and that therefore may be much easier to bound or to compute. Second, we will show the different diameters shed some light on bounding the graph diameter. For some polytopes the differences are large but in others they are not (e.g., in [5] we show there are only small differences for transportation polytopes). Many pairs of these circuit distances have easy-to-verify relationships to each other. For two given vertices, e.g. the weak circuit distance $CD_f$ is at least as large as the soft circuit distance $CD$ because we are just imposing an additional constraint. We denote this $CD_f \geq CD$. If there are polyhedra with vertices such that these two values differ, we write $CD_f > CD$. Sometimes we will consider several such combinations at the same time. We then e.g. use $CD_{f,m,s} > CD_{f,m,s}$ to refer to both $CD_f > CD$ and $CD_{f,m} > CD_{s,m}$. Note that this notation is transitive: Clearly $CD_{f,m} \geq CD_f \geq CD$ implies $CD_{f,m} \geq CD$ and $CD_{f,m} > CD_f \geq CD$ implies $CD_{f,m} > CD$. The main goal of this paper is to prove inequalities between the different distances, show how they strictly or weakly bound each other, and show how they differ.

Some general comments are in order before we list our results. First, as we will see later, some of optimal walks are commutative in the sense that it does not matter in which order we apply the steps. This happens for the diameters $CD$ and $CD_{f,s}$. Such commutative walks can be interpreted simply as linear combinations of circuits of the form $v^{(2)} - v^{(1)} = \sum_{i=1}^{k} \alpha_i g^i$. All other types of circuit walks have to be regarded as ordered sequences of vectors. In this way, the distance $CD$ is just a linear algebra bound of the graph diameter that equals the size of a minimal support of a linear combination of circuits.

Second, it is important to note that reversing the walk from $v^{(1)}$ to $v^{(2)}$ (by taking the negatives of circuits) gives a walk from $v^{(2)}$ to $v^{(1)}$, but this new walk may not necessarily satisfy the same properties. See [4] for a simple counterexample with respect to $CD_{f,m}$. However, fortunately all of the distance concepts besides $CD_{f,m,b(r)}$, are symmetric in the sense that the reversed walk satisfies the conditions the original walk did and thus the distance from $v^{(2)}$ to $v^{(1)}$ is the same as the distance from $v^{(1)}$ to $v^{(2)}$. Finally, sign-compatible walks may not be obviously natural for the non-expert, but it was shown in [7] they play a significant role in showing that there is a selection strategy such that only polynomially many circuit greedy-like augmentation steps that respect sign-compatibility are needed to reach an optimal linear programming solution (a fact that is still unresolved for the Simplex method). However, it is still an open problem how to implement this greedy-type augmentation oracle in polynomial time.

Our Contributions

Our main result is the following

**Theorem 1.** The circuit distances satisfy a hierarchy as depicted in Figure 3. The sign $\geq$, denotes that for any given pair of vertices one type of circuit distance always upper bounds the other. Respectively, $>$ means that one diameter strictly upper bounds the other and that there exists a polyhedron with a pair of vertices for which the two distances strictly differ.

Section 2 first presents some general properties and observations on our distances. We explain why the hierarchy contains precisely the depicted notions of circuit distances and why they satisfy the respective “weak inequalities”. One key result of this discussion is
Figure 2: A hierarchy of circuit distances.
Theorem 2. Let \( P = \{ z \in \mathbb{R}^n : Az = b, Bz \leq d \} \) with \( A \in \mathbb{Z}^{m \times n}, B \in \mathbb{Z}^{m \times n} \). be a polyhedron in \( \mathbb{R}^n \). For all pairs of vertices of \( P \) the distances \( CD_f, CD_{fb}, CD_{fr}, CD_{fbr} \), and \( CD \) are bounded above by the distance \( CD_{fs} \). Moreover, all these distances are smaller or equal to \( \min \{ n - \text{rank}(A), \text{rank}(A) - n + m_B \} \).

We then perform the core part of the proof of Theorem 1. We exhibit polytopes with pairs of vertices \( v^{(1)}, v^{(2)} \) for which the length of optimal walks with the respective properties differ. We prove that almost all circuit distances in the hierarchy are indeed distinct and thus viable. Observe that the results on the circuit distances transfer to statements about the diameters of polyhedra being different too.

In Section 3 we discuss the hierarchy for dimension \( n = 2 \), denoting the circuit distances by \( CD^2 \). We show that many different distance notions collapse into only a few distinct distances. The resulting hierarchy is depicted in Figure 3 and proved in the following theorem, together with the possible distances of vertices in (two-dimensional) polygons.

Theorem 3. For \( n = 2 \) the circuit hierarchy collapses as depicted in Figure 3.

More precisely, for a polygon on \( k \) vertices we obtain

\[
CD^2_{efmb} \in \{1, \ldots, k-3\} \quad (k \geq 5)
\]

\[
CD^2_{efm} = CD^2_{efmr} \in \left\{1, \ldots, \left\lfloor \frac{k}{2} \right\rfloor \right\}
\]

\[
CD^2_{fm(b)}(r) \in \left\{1, \ldots, \left\lfloor \frac{k}{2} \right\rfloor \right\}
\]

\[
CD^2_f = CD^2_{fb} = CD^2_{fr} = CD^2_{fbr} = CD^2_{fs} = CD^2 \in \{1, 2\}
\]

Further there are polygons with pairs of vertices that attain the maximal distances in the ranges claimed above.

2 Proof of Theorem 1

Before we start with the technical details of the proof of Theorem 1, there are a few comments to make. Figure 2 depicts a total of 12 different notions of circuit distance. For sake of having a clear layout the lower left and lower right parts refer to the same classes.

The very first horizontal layer of the table contains edge walks, which we group by a small surrounding box. An edge walk always is both feasible and maximal, so there are only combinations that contain all of these properties at the same time. We distinguish between \( CD_{e fm} \) and \( CD_{e fmb}, CD_{e fmr} \). By imposing an additional constraint we directly have \( CD_{e fmb} \geq \)}
We want to perform circuit walks from all possible edge directions \( g \) length at most \( \min \{ \mathbf{v} \} \) of two of its vertices. Then there is a feasible sign-compatible circuit walk from \( \mathbf{v} \). So in particular \( \mathbf{v} \) holds for all feasible maximal circuit walks, which are listed in the second layer.

**Lemma 1.** For \( n = 2 \), there is a polytope with a pair of vertices such that there is no feasible maximal sign-compatible circuit walk from one vertex to the other one. In particular there is no feasible maximal sign-compatible edge walk.

**Proof.** Consider the polytope

\[
P = \{ \mathbf{x} \in \mathbb{R}^2 : 1 \leq \mathbf{Bx} \leq \mathbf{u} \}
\]

defined by

\[
\mathbf{B} = \begin{pmatrix}
1 & 0 \\
1 & 1 \\
1 & -1 \\
1 & -2
\end{pmatrix},
1 = \begin{pmatrix}
0 \\
-1 \\
-3
\end{pmatrix},
\mathbf{u} = \begin{pmatrix}
\infty \\
4 \\
\infty
\end{pmatrix}.
\]

All possible edge directions \( \mathbf{g} \) of \( P \) are given by

\[
\pm \begin{pmatrix}
0 \\
1
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
-1
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
1
\end{pmatrix}, \pm \begin{pmatrix}
2 \\
1
\end{pmatrix},
\]

and the corresponding vectors \( \mathbf{Bg} \) are

\[
\pm \begin{pmatrix}
0 \\
1 \\
-1 \\
-2
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
0 \\
2 \\
3
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
2 \\
0 \\
-1
\end{pmatrix}, \pm \begin{pmatrix}
2 \\
3 \\
1 \\
0
\end{pmatrix}.
\]

We want to perform circuit walks from \( \mathbf{v}^{(1)} = (2, -2)^T \) to \( \mathbf{v}^{(2)} = (1, 2)^T \). We have \( \mathbf{B} \) \( \mathbf{v}^{(2)} - \mathbf{v}^{(1)} = (-1, 3, -5, -6)^T \). The only sign-compatible circuits are \( (0, 1)^T \) (as \( \mathbf{B}(0, 1)^T = (0, 1, -1, -2)^T \)) and \( (-1, 1)^T \) (as \( \mathbf{B}(-1, 1)^T = (-1, 0, 2, 3)^T \)). But choosing direction \( (0, 1)^T \) as well as choosing \( (-1, 1)^T \) for a first feasible maximal circuit step at \( \mathbf{v}^{(1)} \) yields points from which we cannot reach \( \mathbf{v}^{(2)} \) with circuits that are sign-compatible with \( \mathbf{v}^{(2)} - \mathbf{v}^{(1)} \).

![Figure 4: All feasible maximal circuit steps at \( \mathbf{v}^{(1)} \) that are sign-compatible with \( \mathbf{v}^{(2)} - \mathbf{v}^{(1)} \).](image)

In contrast, one can show that two vertices of a polyhedron \( P = \{ \mathbf{z} \in \mathbb{R}^n : \mathbf{Az} = \mathbf{b}, \mathbf{Bz} \leq \mathbf{d} \} \), are – in our wording – connected by a feasible sign-compatible circuit walk of boundable length. So in particular \( \mathcal{CD}_{f4} \) is well-defined.

**Lemma 2.** Let \( P = \{ \mathbf{z} \in \mathbb{R}^n : \mathbf{Az} = \mathbf{b}, \mathbf{Bz} \leq \mathbf{d} \} \) be a polyhedron in \( \mathbb{R}^n \) and let \( \mathbf{v}^{(1)}, \mathbf{v}^{(2)} \) be two of its vertices. Then there is a feasible sign-compatible circuit walk from \( \mathbf{v}^{(1)} \) to \( \mathbf{v}^{(2)} \) of length at most \( \min \{ \text{rank}(\mathbf{A}) - n + m_B, n - \text{rank}(\mathbf{A}) \} \).
Proof. It suffices to consider the case \( \operatorname{rank} \left( \begin{pmatrix} A \\ B \end{pmatrix} \right) = \operatorname{rank}(A) + \operatorname{rank}(B) \). Otherwise the representation of \( P \) has redundant rows in the matrix \( B \) and the bound derived below may only become lower.

Let \( \sim \in \{=, \leq , \geq \}^m \) such that its \( i \)-th component \( \sim_i \) is defined as

\[
\sim_i = \begin{cases} 
\leq & \text{if } (B(v^{(2)} - v^{(1)}))_i < 0 \\
\ = & \text{if } (B(v^{(2)} - v^{(1)}))_i = 0 \\
\geq & \text{if } (B(v^{(2)} - v^{(1)}))_i > 0
\end{cases}
\]

Then \( v^{(2)} - v^{(1)} \in \{ x \in \mathbb{R}^n : Bx \sim 0 \} =: C_{\sim} \). This is a polyhedral rational cone in which all elements are pairwise sign-compatible. Observe that \( Bv^{(i)} \leq d \) and at least \( n \) (linearly independent) inequalities of this kind are tight. Hence \( (B(v^{(2)} - v^{(1)}))_i = 0 \) for at least \( 2(n - \operatorname{rank}(A)) - m_B \) (linearly independent) inequalities if \( m_B \leq 2(n - \operatorname{rank}(A)) \) (and possibly for none if \( m_B \geq 2(n - \operatorname{rank}(A)) \)). This forces \( C_{\sim} \) to be of dimension at most \( (2(n - \operatorname{rank}(A)) - m_B) \). Hence \( C_{\sim} \) has dimension at most \( n \), and we conjecture that these weak inequalities are strict as well. In Lemma 14, we explain why a polytope proving this conjecture has to be of dimension five or higher.

Let \( H_\sim \) be the unique minimal generating set of \( C_{\sim} \cap \ker(A) \) over \( \mathbb{R} \), where the components of each vector in \( H_\sim \) are scaled to integers with greatest common divisor one. Then all elements in \( H_\sim \) are circuits. Note that \( \dim(C_{\sim} \cap \ker(A)) = \dim(C_{\sim}) - \operatorname{rank}(A) \) due to \( \operatorname{rank} \left( \begin{pmatrix} A \\ B \end{pmatrix} \right) = \operatorname{rank}(A) + \operatorname{rank}(B) \) and hence \( \dim(C_{\sim} \cap \ker(A)) = \dim(C_{\sim}) = \operatorname{rank}(A) + \operatorname{rank}(B) \) (and \( \dim(C_{\sim} \cap \ker(A)) \leq \dim(C_{\sim}) \)). By Caratheodory’s Theorem \( v^{(2)} - v^{(1)} \in C_{\sim} \cap \ker(A) \) can thus be written as a combination of at most \( \operatorname{rank}(A) \) (respectively \( n \)) of the generators contained in \( H_\sim \).

By transitivity of the inequalities in the hierarchy, this upper bound on \( CD_{fB} \) transfers to many of the distances. This proves Theorem 2.

Let us add what the given bound looks like for two widely-used types of polyhedra in whose description the matrix \( A \), respectively \( B \) does not appear.

Corollary 1. Let \( P = \{ z \in \mathbb{R}^n : Az = b, z \geq 0 \} \) be a polyhedron in \( \mathbb{R}^n \) and let \( v^{(1)}, v^{(2)} \) be two of its vertices. Then there is a feasible sign-compatible circuit walk from \( v^{(1)} \) to \( v^{(2)} \) of length at most \( \min \{ \operatorname{rank}(A), n - \operatorname{rank}(A) \} \).

Proof. Note that \( B = -I_n \). The claim then follows from Lemma 2 by using \( m_B = n \).

Corollary 2. Let \( P = \{ z \in \mathbb{R}^n : Bz \leq d \} \) be a polyhedron in \( \mathbb{R}^n \) and let \( v^{(1)}, v^{(2)} \) be two of its vertices. Then there is a feasible sign-compatible circuit walk from \( v^{(1)} \) to \( v^{(2)} \) of length at most \( \min \{ m_B - n, n \} \).

Proof. There is no matrix \( A \) in the description of the polyhedron, so the claim follows from Lemma 2 by using \( \operatorname{rank}(A) = 0 \).

We now relax the constraint (e) and allow circuit walks through the interior of the polyhedron. For feasible maximal circuit walks we again distinguish between \( CD_{fmb}, CD_{fmr} \) and we prove that these concepts do not coincide in Lemmas 9 and 10 that is, \( CD_{fmb} < CD_{fmr} \). Additionally, we show that the second layer connects to the first one not only by the obvious weak inequalities, but by \( CD_{efmb(b)(r)} \) and \( CD_{efmr(b)(r)} \) in Lemma 4 using a polytope from [4].

In the third and lower layers of the table, we drop the maximality condition. This may again reduce the distance of vertices, which we show in Lemma 3. We further prove that requiring a non-repetitive walk may increase the distance of a feasible walk, i.e. \( CD_{fr} > CD_{f} \) and \( CD_{fmr} > CD_{fb} \) by constructing a special four-dimensional polytope in Lemma 12. In contrast we only know \( CD_{fb} \geq CD_{f} \) and \( CD_{fmr} \geq CD_{fr} \) when the non-backwards restriction is dropped. These are the only weak inequalities in the hierarchy, and we conjecture that these are strict as well. In Lemma 13 we explain why a polytope proving this conjecture has to be of dimension five or higher.

We conclude the feasible circuit walks with sign-compatible ones, i.e. \( CD_{fj} \). Unlike the many combinations where a weak inequality is clear from imposing additional or less constraints, it is not obvious for \( CD_{fj} \geq CD_{fbr} \).

Lemma 3. Any optimal sign-compatible circuit walk is in fact feasible, non-backwards and non-repetitive.
Proof. It follows immediately from the definition of sign-compatible walks, that these are feasible. In fact, the steps of a sign-compatible circuit walk can be applied in arbitrary order, yielding feasible sign-compatible walks again. Hence by reordering, we can assume that all steps that use a circuit $\pm g^*$ are applied consecutively. Thus these multiple steps could be combined into a single circuit step which yields a shorter circuit walk.

Later we will prove in Lemma 13 that even $CD_{fs} > CD_{fb}$ holds.

In the final part of the hierarchy, shown in the lowest horizontal layer of the table, we do not even require feasibility. This can indeed be an advantage as demonstrated in Lemma 6. Here we only have to consider $CD$. Lemma 6 tells us that every optimal sign-compatible walk is feasible, hence $CD_s = CD_{fs}$, and similar arguments show that optimal soft circuit walks are non-repetitive and non-backwards, that is $CD = CD_s = CD_b$.

Let us point out that there are classes of polyhedra for which the whole hierarchy ‘collapses’. For example, in simplices all pairs of vertices are connected by an edge, so all circuit diameters equal one. For any $n$-dimensional zonotope, all circuit diameters are equal to $n$; the $n$-dimensional cube is a particularly simple special case. Recall that a zonotope is point-symmetric with respect to its center of gravity. Vertices that correspond to each other with respect to the point symmetry are connected by an edge walk of length exactly $n$. Using any set of circuits and no restrictions on the walk we cannot do any better, as the circuits here correspond to the actual, existing edge directions.

Finally we turn to the proofs for the ‘strict inequalities’ in our hierarchy. We begin with the relation of edge walks and feasible maximal circuit walks.

**Lemma 4** ($CD_{efm}(r) > CD_{fm}(r)$). For $n = 2$, there is a polytope with a pair of vertices for which every optimal feasible maximal circuit walk is not an edge walk, and there is such a walk that is non-repetitive and non-backwards. Hence the distances $CD_{efm}$ and $CD_{fm}$, the distances $CD_{efmb}$ and $CD_{fmnb}$, and the distances $CD_{efmr}$ and $CD_{fmr}$ differ in this case.

**Proof.** In the polytope below, an optimal edge walk from $v^{(1)}$ to $v^{(2)}$ along the edges has length three, while there is a feasible maximal non-repetitive non-backwards circuit walk of length two.

![Diagram](image1.png)

Figure 5: An optimal edge walk and an optimal feasible maximal walk.

Next we turn to dropping maximality of a feasible circuit walk.

**Lemma 5** ($CD_{fm(b)(r)} > CD_{f(b)(r)}$). For $n = 2$, there is a polytope with a pair of vertices for which every optimal feasible circuit walk is not maximal, and there is such a walk that is non-repetitive and non-backwards. Hence the distances $CD_{fm}$ and $CD_{f}$, the distances $CD_{fmnb}$ and $CD_{fnb}$, and the distances $CD_{fmr}$ and $CD_{fr}$ differ in this case.

**Proof.** In the polytope below, an optimal feasible maximal walk from $v^{(2)}$ to $v^{(1)}$ has length at least three: No matter which circuit direction we apply at $v^{(2)}$ with maximum length, we cannot get to $v^{(1)}$ in just one additional step.
On the other hand, there is a feasible non-repetitive non-backwards circuit walk of length two.

We now show that a soft circuit walk may be shorter than an optimal feasible circuit walk.

**Lemma 6** ($CD_f > CD$). For $n = 3$, there is a polytope with a pair of vertices for which no optimal circuit walk with respect to $CD$ is feasible, and there is such an optimal walk that is sign-compatible. Hence the distance $CD_f$ and $CD$ differ in this case.

**Proof.** The polytope below is obtained from a cube by cutting off six of its vertices using three pairs of hyperplanes, and keeping an opposite pair $v^{(1)}, v^{(2)}$ of vertices as depicted. Assume the center of gravity of the cube is 0. Then the normals of these hyperplanes are equal to the coordinates of the vertices cut off. The ‘depth’ of the cuts is arbitrarily small.

Any feasible circuit walk from $v^{(1)}$ to $v^{(2)}$ has length at least three: To see this we illustrate the directions of all possible first steps at $v^{(1)}$ (red) and all possible last steps to $v^{(2)}$ (green) of a feasible circuit walk. Note that these steps are not necessarily maximal.
Clearly there is no point that (a) can be reached in a single step from $v^{(1)}$ and (b) from which one can reach $v^{(2)}$ in a single step. Hence any feasible circuit walk from $v^{(1)}$ to $v^{(2)}$ has length at least three.

On the other hand, there is a soft circuit walk of length two from $v^{(1)}$ to $v^{(2)}$.

![Figure 9: A soft circuit walk of length two.](image)

The following two lemmas explain why allowing the use of edge directions both $g^i$ and $-g^i$ or the repeated use of an edge direction $g^i$ can yield a shorter edge walk.

**Lemma 7** ($CD_{efmb} > CD_{efm}$). For $n = 2$, there is a polytope with a pair of vertices for which the unique optimal edge walk is backwards. Hence the distances $CD_{efmb}$ and $CD_{efm}$ differ in this case.

**Proof.** In the polytope below, the unique non-backwards edge walk from $v^{(1)}$ to $v^{(2)}$ has length four, while there is an edge walk of length three that uses edges in opposite directions.

![Figure 10: An optimal non-backwards edge walk and a backwards edge walk.](image)

**Lemma 8** ($CD_{efmr} > CD_{efm}$). For $n = 3$, there is a polytope with a pair of vertices for which the unique optimal edge walk is repetitive. Hence the distances $CD_{efmr}$ and $CD_{efm}$ differ in this case.

**Proof.** We construct a polytope with the claimed property by cutting off vertices of a three-dimensional cube as illustrated in the following figures:
We obtain the polytope below, in which there is a repetitive edge walk from $v^{(1)}$ to $v^{(2)}$ of length four. It is easy to check that any other edge walk from $v^{(1)}$ to $v^{(2)}$ has length at least five.

Backwards or repetitive circuit walks also can be shorter than their respective counterparts. First we exhibit a polytope to see this for backwards walks.

**Lemma 9** \( (CD_{fmb} > CD_{fm}) \). For \( n = 2 \), there is a polytope with a pair of vertices for which every optimal feasible maximal circuit walk is backwards. Hence the distances $CD_{fmb}$ and $CD_{fm}$ differ in this case.

**Proof.** We consider the polytope on 11 vertices depicted in Figure 13, the lower subfigure is a zoomed-in view on the right part of the polygon. The edge directions are given by

\[
\begin{align*}
(1, 1), (1, 0), (-1, 1), (3, -10), (2, -10), (1, 10), (2, 10), (3, 10).
\end{align*}
\]

There is a feasible maximal circuit walk of length three from $v^{(1)}$ to $v^{(5)}$ that is backwards.
Figure 13: A polytope with a feasible maximal backwards circuit walk of length three.

Every other feasible maximal circuit walk from \( v^{(1)} \) to \( v^{(5)} \) has length at least four. To see this, we illustrate all possible combination of first (dashed) and second feasible maximal circuit steps in Figure 14. From none of these second step points we can reach \( v^{(5)} \) in only one additional step, except from the point \( v^{(10)} \) in the top left picture. But this is the backwards circuit walk as depicted in Figure 13. Observe that all second steps that end in the edge \((v^{(11)}, v^{(1)})\) have coordinates \((x, 9)^T\) for an integral \(x\), in particular we cannot go to \(v^{(5)} = (27 \frac{27}{100}, 0)^T\) by applying the circuit \((-1, 1)^T\) at these points. The final sketch is a zoomed-in view on the bottom right picture. It illustrates all possible second steps after applying \((-1, 1)^T\) at \(v^{(1)}\).
Figure 14: Possible combinations of first and second feasible maximal circuit steps from $v^{(1)}$.

Similarly, one may obtain a shorter circuit walk by allowing oneself to use a repeated circuit.

**Lemma 10** ($CD_{fmr} > CD_{fm}$). For $n = 2$, there is a polytope with a pair of vertices for which every optimal feasible maximal circuit walk is repetitive. Hence the distances $CD_{fmr}$ and $CD_{fm}$ differ in this case.

**Proof.** We consider the following polytope on nine vertices depicted in Figure 15. Note that there are two edges $e_0$ and $e_7$ with direction $(1, 0)^T$, an edge $e_1$ with direction $(1, -1)^T$, an edge $e_6$ with direction $(1, 1)^T$ and the edge $e_8$ with direction $(0, 1)^T$. Further, in the right part there are four steeper edges: $e_2$ with direction $(1, -4)^T$, $e_3$ with direction $(1, -5)^T$, $e_4$ with direction $(1, 5)^T$, $e_5$ with direction $(1, 4)^T$.

There is a feasible maximal circuit walk of length three from $v^{(1)}$ to $v^{(5)}$ that is repetitive.

Figure 15: The polytope for the proof of Lemma 10.

Figure 16: A feasible maximal repetitive circuit walk of length three.
Every other circuit walk from $v^{(1)}$ to $v^{(5)}$ has length at least four. Therefore we illustrate all possible combinations of first (dashed) and second steps in Figure 17. From none of these second step points we can reach $v^{(5)}$ in only one additional step, except from the point $(0,0)$ in the first picture. But this is the repetitive circuit walk as in Figure 16. For those points for which it might not be immediately obvious that we cannot get to $v^{(5)}$ in only one more step, we added the coordinates for a convenient verification that we cannot reach $v^{(5)} = (19\frac{3}{2}, 0)$ with any edge direction.

Figure 17: Possible combinations of first and second feasible maximal circuit steps from $v^{(1)}$.

The following lemma tells us that for an example for $CD_{fr} > CD_f$ we need a polytope in dimension at least four. In Lemma 12 we show that such a polytope indeed exists.

**Lemma 11.** For $n \leq 3$, every optimal feasible circuit walk is non-repetitive. Hence the distances $CD_f$ and $CD_{fr}$ coincide in this case.

**Proof.** Clearly repetitive circuit walks have length at least three. In case any optimal circuit walk between two vertices is repetitive, any feasible non-repetitive circuit walk must have length at least four. But in dimension $\leq 3$ there always is a such a circuit walk of length at most three by Lemmas 2 and 3.

**Lemma 12 ($CD_{fr}(b) > CD_f(b)$).** For $n = 4$, there is a polytope with a pair of vertices for which every optimal feasible circuit walk is repetitive (but non-backwards). Hence the distances $CD_f$ and $CD_{fr}$, and the distances $CD_{ffr}$ and $CD_{frb}$ differ in this case.

**Proof.** Let the polytope

$$P = \{ x \in \mathbb{R}^4 : l \leq Ax \leq u \}$$

be defined by

$$A = \begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
1 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 \\
1 & 0 & 0 & 1 \\
\end{pmatrix}, \quad l = \begin{pmatrix}
0 \\
0 \\
0 \\
-\infty \\
-\infty \\
-\infty \\
-\infty \\
\end{pmatrix}, \quad u = \begin{pmatrix}
3/2 \\
1 \\
1 \\
1 \\
2 \\
2 \\
2 \\
\end{pmatrix}.$$

The rows of the matrix $A$ define directions of 11 hyperplanes bounding the polytope.
The vertices are the intersections of four of these hyperplanes, in case this intersection is a single point that is contained in $P$. A simple computation shows that we have 23 vertices $((0,1)^3 \cup \{(1,0,0,0)^T\}) \cup \left(\left\{\frac{1}{2}\right\} \times \{0,\frac{1}{2}\}\right)^3$. In particular $v^{(1)} := (0,0,0,0)^T$ and $v^{(2)} := (1,1,1,1)^T$ are vertices of $P$.

The circuits are the potential edge directions for varying $l$ and $u$, that is, they are given by the intersection of three hyperplanes, in case this intersection is 1-dimensional. Again it is not hard to compute that these directions are $\pm e^i$ (where $e^i$ is the $i$th unit vector) and $\pm \{(1) \times (0,[-1]^3)\}$ and hence constitute the set of circuits.

**Claim:** Every feasible circuit walk from $v^{(1)} = (0,0,0,0)^T$ to $v^{(2)} = (1,1,1,1)^T$ of length at most three is repetitive.

**Proof of claim:** We investigate how we can reach $v^{(2)} = (1,1,1,1)^T$ in at most three feasible circuit steps. Observe that in particular we cannot apply circuits that violate the lower bounds of 0 or the upper bounds of $\frac{1}{2}$ (respectively 1). Hence as a first feasible circuit step, we can only apply $e^1$ or w.l.o.g. $e^2$.

Applying $e^2$ yields a point $(x_1,x_2,0,0)^T$ with $x_2 \leq 1$. In the second step we can either apply w.l.o.g. $e^3$, giving $(0,x_2,x_3,0)^T$ with $x_2, x_3 \leq 1$, or we apply $e^2$ or $(1,-1,0,0)^T$ giving $(x_1,x_2,0,0)^T$ with $x_1 \leq \frac{1}{2}$. Hence to reach to $v^{(2)} = (1,1,1,1)^T$ with one more circuit step: We cannot increase the first and the last component at the same time, nor increase the last two components by one simultaneously without decreasing the first component to $\leq \frac{1}{2}$.

Applying $e^1$ as a first step yields a point $(x_1,0,0,0)^T$ with $x_1 \leq \frac{1}{2}$. In the next step we can either increase only one component w.l.o.g. only the second one (by applying $e^2$ or $(-1,1,0,0)^T$), giving $(x_1,x_2,0,0)^T$ with $x_1 \leq \frac{1}{2}$, $x_2 \leq 1$, but as before we cannot reach $v^{(2)}$ in one more circuit step. Otherwise in the second step we increase at least two components (by applying $(-1,1,1,1)^T$ or w.l.o.g. $(-1,1,1,0)^T$, giving $(x_1,x_2,x_3,x_4)^T$ with $x_1+x_2 = x_1+x_3 = x_1+x_4 \leq \frac{1}{2}$, $x_2,x_3 \leq 1$ (respectively $(x_1,x_2,x_3,0)^T$ with $x_1+x_2 = x_1+x_3 \leq \frac{1}{2}$, $x_2 \leq 1$). In particular we know that $x_2 = x_3 < 1$ or $x_1 < 1$. Hence to reach to $v^{(2)} = (1,1,1,1)^T$ in one more step, we have to increase the second and third component simultaneously to 1 (which decreases the first component to $\leq \frac{1}{2}$), or we have to increase the first one without decreasing any other component (that is, we apply $e^1$ again). This proves our claim.

On the other hand, applying the circuits $e^1$, $(-1,1,1,1)^T$ and $e^1$ with step length one each is indeed a feasible non-backwards circuit walk of length three from $v^{(1)}$ to $v^{(2)}$.

**Lemma 13 ($CD_{fs} > CD_{fbr}$).** For $n = 3$, there is a polytope with a pair of vertices for which every optimal feasible circuit walk is not sign-compatible, and there is such a walk that is non-repetitive and non-backwards. Hence the distance $CD_{fs}$ differs from $CD_{fbr}$, $CD_{fr}$, $CD_{fb}$, and $CD_f$.

**Proof.** Consider the polytope

$$P = \{ x \in \mathbb{R}^3 : 1 \leq Bx \leq u \}$$

defined by

$$B = \begin{pmatrix}
1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1 \\
1 & 1 & 0 \\
1 & 0 & 1 \\
\end{pmatrix}, \quad 1 = \begin{pmatrix}
0 \\
0 \\
-\infty \\
-\infty \\
\end{pmatrix}, \quad u = \begin{pmatrix}
\infty \\
1 \\
2 \\
2 \\
\end{pmatrix}. $$

All possible edge directions $g$ of $P$ are given by

$$\pm \begin{pmatrix}
1 \\
0 \\
0 \\
0 \\
1 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
1 \\
0 \\
1 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
0 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
0 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
0 \\
1 \\
1 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
1 \\
1 \\
0 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
1 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, \pm \begin{pmatrix}
1 \\
1 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, $$

and the corresponding vectors $Bg$ are

$$\pm \begin{pmatrix}
1 \\
0 \\
1 \\
1 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
1 \\
0 \\
1 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
1 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
1 \\
0 \\
0 \\
-1 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
0 \\
1 \\
1 \\
0 \\
\end{pmatrix}, \pm \begin{pmatrix}
0 \\
0 \\
1 \\
1 \\
0 \\
\end{pmatrix}. $$
We want to perform circuit walks from $v^{(1)} = (0, 0, 0)^T$ to $v^{(2)} = (1, 1, 1)^T$. We have $B (v^{(2)} - v^{(1)}) = (1, 1, 1, 2, 2)^T$. Hence only the unit vectors $e^1, e^2$ and $e^3$ can be applied in sign-compatible walks. Thus an optimal feasible sign-compatible walk from $v^{(1)} = (0, 0, 0)^T$ to $v^{(2)} = (1, 1, 1)^T$ has length at least three, as we have to apply all three unit vectors.

![Figure 18: A feasible sign-compatible circuit walk of length three.](image)

On the other hand, there is a feasible non-repetitive non-backwards circuit walk of length two that is not sign-compatible.

![Figure 19: A feasible not sign-compatible circuit walk of length two.](image)

The following lemma tells us that for an example for $CD_{fb} > CD_f$ we need a polytope in dimension at least five.

**Lemma 14.** For $n \leq 4$, every optimal feasible circuit walk is non-backwards. Hence the distances $CD_f$ and $CD_{fb}$ coincide in this case.

**Proof.** We first show that if an optimal feasible circuit walk is backwards then it has length at least four. Clearly it has length at least three. Assume there is a polytope with vertices $v^{(1)}$ and $v^{(2)}$ that are connected by a feasible circuit walk

$$v^{(1)} = y^{(0)}, \quad y^{(1)} = y^{(0)} + \alpha_1 g^1, \quad y^{(2)} = y^{(1)} + \alpha_2 g^2, \quad y^{(3)} = y^{(2)} + \alpha_3 (-g^1) = v^{(2)}$$

that is, the walk is backwards. But then there is a feasible circuit walk from $v^{(1)}$ to $v^{(2)}$ of length two,

$$v^{(1)} = y^{(0)}, \quad \tilde{y}^{(1)} = y^{(0)} + (\alpha_1 - \alpha_3) g^1, \quad \tilde{y}^{(2)} = \tilde{y}^{(1)} + \alpha_2 g^2$$

if $\alpha_1 \geq \alpha_3$ , respectively

$$v^{(1)} = y^{(0)}, \quad y^{(1)} = y^{(0)} + \alpha_2 g^2, \quad \tilde{y}^{(2)} = \tilde{y}^{(1)} + (\alpha_3 - \alpha_1) (-g^1)$$

if $\alpha_1 < \alpha_3$ .

Clearly these circuit walks satisfy $\tilde{y}^{(2)} = v^{(2)}$ and are indeed feasible by convexity of the polytope. Therefore a feasible backwards circuit walk of length three cannot be optimal.

Now in case any optimal circuit walk between two vertices is backwards, any feasible non-backwards circuit walk must have length at least five. But Lemmas 2 and 3 imply that for $n \leq 4$ there always is a feasible non-backwards circuit walk of length at most four. \qed
3 Diameter hierarchy in dimension two

We conclude this paper with a discussion of the different notions of circuit distances in dimension \( n = 2 \). It is easy to see that in this situation the graph diameter is given by \( \left\lfloor \frac{k}{2} \right\rfloor \), where \( k \) is the number of vertices of the polygon. In particular this number tells us which values \( \text{CD}_{efm}^2 \) can take. In this section we prove Theorem 3 that states the possible ranges of all the notions of circuit distances, and tells us which distance categories coincide for \( n = 2 \) and which remain different. Finally, we will exhibit that \( \text{CD}_{efm(b)(r)}^2 \) and \( \text{CD}_{fm(b)(r)}^2 \) can differ significantly in Lemma 10.

Proof of Theorem 3. Note that Lemma 4, Lemma 5, Lemma 6 and Lemma 10 show the inequality of the corresponding circuit distances in dimension two and hence also prove the strict inequalities in the circuit hierarchy in Figure 3. Again the numbers near the inequality symbols refer to these lemmas.

A polygon on \( k \) vertices and a pair of vertices with \( \text{CD}_{efm}^2 (v^{(i)}, v^{(i)}) = k - 3 \) is readily derived from the one given in Figure 10 in Lemma 7 by putting \( k - 4 \) vertices ‘to the left’ of \( v^{(i)} \) and \( v^{(i)} \).

In dimension two there are no repetitive edge walks and hence \( \text{CD}_{efm}^2 = \text{CD}_{fm}^2 \). The claimed range of values for distances of vertices is obvious.

For \( \text{CD}_{fm(b)(r)}^2 \) we only have to show that there are indeed vertices with feasible maximal circuit distance \( \left\lfloor \frac{k}{2} \right\rfloor \). Lemma 15 proves this for even \( k \) and can easily be extended to odd \( k \) by adding another vertex.

For

\[
\text{CD}_{f}^2 = \text{CD}_{f r}^2 = \text{CD}_{fr}^2 = \text{CD}_{fs}^2 = \text{CD}^2 \in \{1, 2\}
\]

it is enough to recall Lemma 2. \( \square \)

To complete the proof of Theorem 3 we still have to show that there are polygons with vertices that have feasible maximal circuit distance \( \left\lfloor \frac{k}{2} \right\rfloor \). For the sake of a clean presentation, we provide the proof for \( k \) even. It can readily be extended to the general case.

Lemma 15. Let \( k \) be even. Then there is a polygon on \( k \) vertices with diameter \( \frac{k}{2} \) with respect to \( \text{CD}_{fm}^2 \).

Proof. Let \( k \) even be given. We construct a polygon on vertices \( v^{(0)}, \ldots, v^{(k-1)} \) with edges \( \langle v^{(i)}, v^{(i+1)} \rangle = e_i \) for \( i = 0, \ldots, k - 1 \) (where \( v^{(k)} := v^{(0)} \)) such that \( \text{CD}_{fm}^2 (v^{(0)}, v^{(k)}) = \frac{k}{2} \). The corresponding edge walk will be an optimal maximal circuit walk.

Note that for \( n = 2 \), the edges are the facets of the polygon. Thus there is a direct correspondence of the circuits and the edges as ‘edge directions’. We will exploit this for a simpler wording in the following, talking about ‘walking along edges’ or ‘in direction of an edge’.

First of all we fix the edge directions and hence the set of circuits associated with \( P \). To this end choose \( \frac{k}{2} \) slopes \( 0 > s_0 > s_1 > s_2 > \ldots > s_{\frac{k}{2}-1} \) arbitrarily. In the upcoming construction we assign edge \( e_0 \) slope \(-s_0\); edge \( e_{\frac{k}{2}-1} \) slope \(-s_{\frac{k}{2}-1} \), and for \( i = 1, \ldots, \frac{k}{2} - 1 \) we assign \( e_i \) slope \( s_i \) and \( e_{\frac{k}{2}+1-i} \) slope \(-s_i \). This will produce a polygon of shape as depicted in Figure 20. Observe that the slopes of the edges on an edge walk from \( v^{(1)} \) to \( v^{(\frac{k}{2})} \) iteratively become less, just as the slopes of the edges from \( v^{(k-1)} \) to \( v^{(\frac{k}{2})} \) become steeper. Further the polygon is symmetric with respect to the first coordinate axis (which we call \( x_1 \)-axis from now on).

It remains to arrange the vertices. We do this iteratively, fixing a pair of vertices \( v^{(i)}, v^{(k-i)} \) in each step such that in \( P \) the following property (*) is satisfied:

\( (*) \) Every maximal feasible circuit walk starting at \( v^{(0)} \) of length at most \( \frac{k}{2} \) that contains a point \( v' \) with larger \( x_1 \)-coordinate than \( v^{(i)} \) or \( v^{(k-i)} \) (or equivalently, that hits an edge \( e_j \) with \( i \leq j \leq k - 1 - j \)) must contain \( v^{(i)} \) or \( v^{(k-i)} \).

This will immediately imply that the circuit distance \( \text{CD}_{fm}^2 \) from \( v^{(0)} \) to \( v^{(\frac{k}{2})} \) is \( \frac{k}{2} \): Every circuit walk of length at most \( \frac{k}{2} \) from \( v^{(0)} \) to \( v^{(\frac{k}{2})} \) does reach a \( v' \) with larger \( x_1 \)-coordinate than every \( v^{(i)} \) for all \( i = 1, \ldots, \frac{k}{2} - 1 \). (We will informally call this ‘going beyond \( v^{(0)} \) from now on.’) Hence by (*), any such circuit walk must contain a vertex from each of these \( \frac{k}{2} - 1 \) pairs of vertices. This takes at least \( \frac{k}{2} - 1 \) steps, and it takes one additional step to reach the target vertex \( v^{(\frac{k}{2})} \).
Construction of initial vertices: Fix $v^{(0)} = (0, 0)$. Let edges $e_0$, respectively $e_{k-1}$, start at $v^{(0)}$ and end in a $v^{(1)}$ on $e_0$ and a $v^{(k-1)}$ on $e_{k-1}$ such that $v^{(1)}$ and $v^{(k-1)}$ have identical $x_1$-coordinates.

(*) holds for the pair $v^{(1)}, v^{(k-1)}$: At $v^{(0)}$ we can only apply circuit steps with directions $e_0$ or $e_{k-1}$ (any other direction is too steep). As we apply maximal steps, the second point of any circuit walk is either $v^{(1)}$ or $v^{(k-1)}$.

Construction of a pair of vertices: Let the vertices $v^{(0)}, v^{(1)}, \ldots, v^{(i)}, v^{(k-i)}, \ldots, v^{(k-1)}$, $i < \frac{k}{2} - 1$, be constructed and satisfy (*). We now construct the vertices $v^{(i+1)}, v^{(k-i-1)}$ together with the incident edges $e_i, e_{k-1-i}$.

1. Let edges with directions $e_i$ (respectively $e_{k-1-i}$) start at $v^{(i)}$ (respectively $v^{(k-i)}$). Let $w^{(i)}$ be their intersection (which has $x_2$-coordinate 0). This defines a polygon $P_i$.

2. In $P_i$ consider all feasible maximal circuit walks of length at most $\frac{k}{2}$ that begin at $v^{(0)}$ and do not walk along the (actual) edge $e_j$ (respectively $e_{k-1-i}$) to the vertex $w^{(i)}$. Then none of these walks contains $w^{(i)}$: A step that hits $w^{(i)}$ is not allowed to go along the edges we just inserted by definition and we cannot reach $w^{(i)}$ from $e_0$ (respectively $e_{k-1}$) in one circuit step by construction. Hence it must start at an edge $e_j$ with w.l.o.g. $0 < j < i$. But then there would have been a feasible maximal circuit walk of length at most $\frac{k}{2}$ in $P_j$ that goes beyond $v^{(j)}$ which contradicts the definition of $v^{(j)}$ in $P_j$.

3. Among all points contained in all of these circuit walks, there are points that have a largest $x_1$-value. These points lie on the edges $e_i$ (respectively $e_{k-1-i}$) by construction.
We now set $v^{(i+1)}$ to be such a point on $e_i$ (respectively $v^{(k-1-i)}$ on $e_{k-1-i}$). This yields a pair of vertices $v^{(i+1)}, v^{(k-1-i)}$ of identical $x_1$-value and with $v^{(i+1)}, v^{(k-1-i)} \neq w^{(i)}$ (with the same arguments as before).

We have to show that $v^{(i+1)}$ and $v^{(k-1-i)}$ satisfy (*) in $P$. Therefore, consider a maximal feasible circuit walk in $P$ starting at $v^{(0)}$ and of length at most $\frac{k}{2}$ that goes beyond $v^{(i+1)}$. This walk in $P$ translates to a walk in $P_t$ and clearly these walks in $P$ and $P_t$ coincide until they go beyond $v^{(i+1)}$ (in both $P$ and $P_t$) by applying some circuit $g^j$ at some point $y^{(j)}$ in the respective circuit walks. Let $y^{(j+1)}$ be the subsequent point in the circuit walk in $P$, respectively $y^{(j+1)}$ in $P_t$. In particular these $y^{(j+1)}$ and $y^{(j+1)}$ have a larger $x_1$-value than $v^{(i+1)}$. By construction of $v^{(i+1)}$ we can only go beyond $v^{(i+1)}$ in at most $\frac{k}{2}$ circuit steps in $P_t$ when going along the (actual) edge w.l.o.g. $e_i$. Hence w.l.o.g. $g^j$ is the edge direction $e_i$ and $y^{(j)} \in e_i$. Thus we have $y^{(j)} = v^{(i+1)}$ as we apply maximal steps, in particular the vertex $v^{(i+1)}$ is contained in the circuit walk in $P$.

Construction of target vertex: Set $v^{(i)} := w^{(i)}$ for $i = \frac{k}{2} - 1$. This concludes the construction of a polygon $P$ with property (*).

Theorem 3 tells us that $CD^2_{fmb(r,s)}$ is constant always one or two, while the other distances can be linear in the number of vertices, in particular $CD^2_{fmb}$. It remains to investigate how $CD^2_{efm(r)}$ and $CD^2_{fmb(r)}$ are related to each other. We conclude by demonstrating that there are polygons for which the former grows linear in the number of vertices while the latter remains constant.

Lemma 16. Let $P$ be a regular polygon on $k$ vertices. Then the diameter with respect to $CD^2_{efm(r)}$ is given by $\frac{k-1}{2}$ if $k$ odd, and the diameter with respect to $CD^2_{fmb(r)}$ is given by $\begin{cases} 1 & \text{if } k \text{ odd} \\ 2 & \text{if } k \text{ even} \end{cases}$

Proof. For $CD^2_{efm(r)}$ the claim is obvious.

To determine the circuit distances $CD_{fmb(r)}$, let $v^{(1)}, \ldots, v^{(k)}$ ($v^{(k+1)} := v^{(1)}$) be the vertices of the polygon and (v(t), v(t+1)) its edges. Let $k$ be odd. It suffices to show that from $v^{(1)}$ we can reach any other vertex in just a single circuit step. For this, it is enough to see $v^{(2)} = v^{(1)} + \alpha \cdot (v^{(1)} - v^{(1)})$ for some $\alpha$ and $v^{(2k+1)} = v^{(1)} + \alpha' \cdot (v^{(2k+1)} - v^{(2k+1)})$ for some $\alpha'$.

Figure 22: A circuit step from $v^{(1)}$ to $v^{(3)}$ and the edge of corresponding direction.

Now let $k$ be even. First observe that there are always two collinear edges and hence not all pairs of vertices are connected by a single circuit step, i.e. the diameter cannot be equal to one. As before, we have $v^{(2k)} = v^{(1)} + \alpha \cdot (v^{(1)} - v^{(1)})$ for some $\alpha$. In case we want to walk from $v^{(1)}$ to $v^{(2k+1)}$ we first go to $v^{(2k)}$ and then along edge $(v^{(2k)}, v^{(2k+1)})$, as depicted in the walk from $v^{(1)}$ to $v^{(5)}$ in Figure 3. Hence the regular $k$-polygon for $k$ even has diameter 2 with respect to $CD^2_{fmb(r)}$.
Figure 23: Optimal circuit walks from $v^{(1)}$ to $v^{(4)}$ and $v^{(5)}$ and edges of corresponding direction.

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