Hardware Circuit Design and Implementation of Digital IF Receiver

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Abstract. At present, most of the digital IF receivers have bottlenecks in the acquisition and analysis of ultra-high frequency bandwidth signals. At the same time, they have the disadvantages of low resolution and low input bandwidth, which cannot meet the needs of ultra-high frequency signal measurement. In this paper, a high-resolution, high-bandwidth digital IF receiver hardware system is designed based on ADC + FPGA architecture. The front-end analog signal is discretized by two high-speed ADC chips and sent to FPGA to decode the sampling data, and the FFT IP core is called to calculate the power spectrum of the signal. The spectrum data are sent to the host computer through RS485 module and Ethernet chip to display the spectrum image of the original signal in real time, so as to analyze the temperature profile of the target atmosphere.

1. Introduction
With the development of human production activities, how to understand global climate change quickly and in real time has gradually been put on the agenda\cite{1}. The analog input signal bandwidth of the digital signal receiver system designed in this paper is greater than 2GHz, the system resolution is not less than 6.8 bits, and supports the simultaneous sampling of two channels. Compared with the general digital signal receiver system, the system can process and analyze the electromagnetic radiation signal in the super band and wide frequency band in real time, and has high measurement resolution. In the process of retrieving the temperature and humidity profile, the receiver system has the advantages of high precision, large range and low delay\cite{2}. It plays an important role in predicting the weather change trend of natural disasters such as typhoon and tropical storm\cite{3}.

2. Overall design of digital IF receiver system
The digital IF receiver system can digitize the preprocessed low IF analog signal, and calculate the spectrum information of the original signal through FFT\cite{4}. This paper uses ADC and FPGA as the core architecture of digital IF receiver. Figure 1 shows the system architecture of digital IF receiver, which is mainly divided into four parts: ADC signal acquisition, high-speed clock, FPGA chip and data transfer module. The analog signal is sampled and quantized by ADC to obtain the discrete digital signal, which is sent to the data receiving unit in FPGA through the high-speed data link, and the module control unit controls the data processing unit to complete the spectrum calculation of the signal. Finally, the spectrum information is sent to the host computer through the data transfer module to obtain the spectrum image of atmospheric radiation and retrieve the atmospheric temperature profile.
3. Hardware design of core system of digital IF receiver

3.1. Overall hardware architecture

The overall structure diagram of receiver system hardware circuit is shown in figure 2.

The hardware of the digital IF receiver system can be divided into three parts: data acquisition circuit, data cache and processing circuit and interface circuit. The data acquisition circuit includes two RF Transformers TCM2-43X+, two high-speed ADC sampling chips ADC12DJ2700 and a clock chip LMK04828. The data cache and processing circuit consists of two DDR3 memories and a FPGA chip. The interface circuit includes two RS485 modules, two RS422 modules, a LVDS Chip, a Gigabit Ethernet controller and a USB 3.0 chip. The bus end of each interface chip is connected to the CPCI interface and connected with the host computer through the physical socket on the backplane.
The overall hardware idea of the receiver system is: two independent signals with a bandwidth of 2GHz are respectively sent to the RF transformer of the data acquisition circuit to be converted into differential signals, which are sampled by an ADC with sampling rate of 5GSPS to obtain digital sampling data. The data is output to the back-end data cache and processing circuit through JESD204B high-speed serial interface. The FPGA in the data cache and processing circuit decode the data stream containing sampling points according to JESD204B transmission protocol to obtain sequential sampling points. The frequency domain data of the signal is obtained after FFT calculation, and finally sent to the host computer through the data interface circuit to display the spectrum information of the original signal in real time.

Because this design requires the system to sample the signal in real time and store the spectrum data of the signal for a period of time. Therefore, on the basis of the original receiver, two DDR3 memory modules are added as external storage modules to cache spectrum data. At the same time, the system uses low speed RS485 and RS422 modules, and the middle speed LVDS module, high-speed Gigabit Ethernet controller and USB3.0 chip, and connect them to the backplane through the physical slot of the CPCI interface, thus realizing data transmission matching of different interface types.

3.2. Power supply scheme design

3.2.1. Power supply scheme for FPGA, DDR3 memory and their peripheral interfaces

For digital devices similar to FPGA, because they are insensitive to external noise and have strong anti-interference ability, BUCK circuit is directly used for power supply, as shown in figure 3. The power supply of each power track is listed in detail below: (1) Core voltage is 1.0V, chip internal block memory voltage is 1.0V and high-speed transceiver port power supply voltage is 1.0V. (2) Terminal voltage of high-speed transceiver is 1.2V. (3) Common IO port voltage is 1.5V. (4) Auxiliary function voltage is 1.8V, auxiliary function IO port voltage is 1.8V. (5) DDR3 memory supply voltage is 1.50v, DDR3 memory reference voltage is 0.75V, RS485 and RS422 supply voltage is 3.3V, USB 3.0 chip supply voltage is 3.3V, and Gigabit Ethernet and LVDS chip supply voltage is 2.5V.

3.2.2. Power supply scheme of ADC and clock chip

For analog devices such as ADC and clock chip, in order to keep the output voltage ripple at a low level, we use the BUCK and LDO (Low Dropout Regulator) scheme for power supply design, as shown in figure 4. ADC power supply demand: (1) 1.1V analog voltage. (2) 1.9V analog voltage. (3) 1.1V digital voltage. Power supply demand of clock chip: (1) 3.3V analog voltage. (2) 3.3V digital voltage.

3.3. Design of high speed clock network

FPGA uses the differential clock with frequency of 200MHz as the global clock for on-chip logic design. The maximum line rate of DDR3 memory module can reach 1600Mbps, using 200MHz differential clock as input. Because the working clock frequencies of FPGA and DDR3 are the same, we can consider using the same clock source as the clock network. So the project uses a 200MHz active crystal oscillator and clock buffer as the core of the clock circuit. The circuit schematic diagram is shown in figure 5.
The overall architecture of ADC clock network is shown in Figure 6. When the chip works, it will output two channels of 2.5GHz DCLK clock (device clock) and two channels of 1.953125MHz SYSREF clock (system reference clock) to two ADCs, and output four channels of 125MHz refclk clock (reference clock) and two channels of 1.953125MHz SYSREF clock to FPGA.

3.4. ADC acquisition circuit design

3.4.1. Analog input circuit
RF transformer is used for coupling input. The circuit structure is shown in Figure 7. The circuit uses a transmission line type RF transformer TCM2-43+ as the core device of the single ended to differential circuit. The input frequency range of the transformer is 10MHz-4000MHz and the maximum insertion loss is 1.8dB. Pin PRI DOT is connected with single ended input and pin PRI is tied to ground; The secondary pins SEC and SEC DOT are used as the positive phase and reverse phase ends of the differential signal, and a bypass capacitor of 0.5pf is connected at both ends. This design has two functions: firstly, prevent the high-frequency noise in the input signal from entering the ADC to cause frequency aliasing and affect the system measurement results; The second function is to use a transformer to isolate the path between the back-end ADC and the front-end signal source, so as to prevent the internal circuit of ADC from causing electromagnetic interference to the front-end signal source during analog-to-digital conversion.

3.4.2. Data output circuit
The ADC chip data interface protocol used in this design is JESD204B transmission protocol, and the interface level type is CML (current mode logic). The ADC output interface adopts AC coupling, and a
0.1μF capacitor is connected in series on each differential transmission line to eliminate the common mode component, as shown in figure 8.

4. System function verification

Figure 9 shows the hardware platform of the digital IF receiver system. The function of the receiver system will be verified below.

Use RF signal source to send a sine wave signal (frequency: 500MHz, amplitude: 1Vp-p) to the system, and the sampling points output by ADC are processed in MATLAB to obtain the waveform image of the sampling signal, as shown in figure 10.

Use RF signal source to send a sine wave signal (frequency: 488.28125MHz, power: -3dBm) to the system. Import the data captured by the logic analyzer into Matlab for FFT calculation, and draw the power spectrum image of the signal, as shown in figure 11.

5. Conclusions

In this paper, a hardware system of digital IF receiver is designed to realize the sampling and spectrum analysis of dual channel signals. Compared with the general digital IF receiver system, the system can process and analyze the electromagnetic radiation signals in the ultra-high signal bandwidth in real time,
and has great advantages for real-time prediction of typhoon and other natural disaster weather. However, according to the development trend of digital IF receiver in the future, the receiver designed in this paper still has room to improve the input signal bandwidth and signal resolution. It is expected that the design of the next version will adopt time alternating sampling technology to improve the measurement frequency bandwidth and system resolution.

References

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