On the Impact of Network Delays on Time-to-Live Caching

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Abstract

We consider Time-to-Live (TTL) caches that tag every object in cache with a specific (and possibly renewable) expiration time. State-of-the-art models for TTL caches assume zero object fetch delay, i.e., the time required to fetch a requested object that is not in cache from a different cache or the origin server. Particularly, in cache hierarchies this delay has a significant impact on performance metrics such as the object hit probability. Recent work suggests that the impact of the object fetch delay on the cache performance will continue to increase due to the scaling mismatch between shrinking inter-request times (due to higher data center link rates) in contrast to processing and memory access times.

In this paper, we analyze tree-based cache hierarchies with random object fetch delays and provide an exact analysis of the corresponding object hit probability. Our analysis allows understanding the impact of random delays and TTLs on cache metrics for a wide class of request stream models characterized through Markov arrival processes. This is expressed through a metric that we denote delay impairment of the hit probability. In addition, we analyze and extend state-of-the-art approximations of the hit probability to take the delay into account. We provide numerical and trace-based simulation-based evaluation results showing that larger TTLs do not efficiently compensate the detrimental effect of object fetch delays. Our evaluations also show that unlike our exact model the state-of-the-art approximations do not capture the impact of the object fetch delay well especially for cache hierarchies. Surprisingly, we show that the impact of this delay on the hit probability is not monotonic but depends on the request stream properties, as well as, the TTL.

1 Introduction

Content orientation is the raison d’être for a wide scale of caching infrastructures in the Internet [1–3] in addition to being a foundation for new Internet architectures [4]. Recently, a renewed interest in a class of caching systems, namely Time-to-Live (TTL) caches, triggered a line of analytical work on the performance evaluation of such systems [5–10]. A remarkable property of TTL caches is that some of their performance measures are equivalent to their counterparts for classical caching algorithms such as Least Recently Used (LRU) under mild conditions [8, 9, 11].

The analysis of large-scale, interconnected TTL caching systems is a difficult task that does not simply allow for exact results. This difficulty stems from the calculation of the forwarded object request stream of each cache, i.e., the cache miss process, and the aggregation of multiple of such processes as input to parent caches. To this end, related work derives approximations that may deviate significantly from the caching system behavior [7]. A significant contribution to the analysis of TTL cache is provided by [7] through an exact formulation for hierarchies under the assumption of zero object fetch delay. We note that in general TTL-based caches are often analyzed under idealized communication assumptions such as negligible latency, no packet loss, no network dynamics, and no capacity constraints [6–9, 11–14].

Observations show, however, that particularly in cache hierarchies the object fetch delay may have a significant adverse effect on the cache performance especially in the tail. The importance of modeling the object fetch delay was pointed at in a recent work [15] that has shown that there is a growing mismatch between data center link rates, thus the ever shrinking request inter-arrival times, and the processing/memory access times in caching systems [16]. This is reflected in form of empirically observed request waiting behavior and service batching [15]. This suggests that the impact of the delay on the cache performance will continue to increase due to this scaling mismatch.
In this paper, we analyze tree-based TTL cache hierarchies under random delays and provide an exact model extending the previous approaches to a joint consideration of caching and communication. Our analysis provides the object hit probability under link-based delays allowing to understand the impact of random network delays and TTLs on cache metrics for a wide class of request stream models. To incorporate the object fetch delays in our proposed model we provide a recursive algorithm to construct a Markov Arrival Process (MAP) description of the output of a given caching hierarchy, i.e., its miss process. To relate the impact of the delay to the object hit probability we coin the metric delay impairment.

In addition to the exact analysis of TTL cache hierarchies under random link delays we analyze state-of-the-art approximations of the object hit probability that aim to encompass these delays. Our numerical as well as trace-based evaluation results shows that unlike our exact model the state-of-the-art approximations do not capture the object fetch delays well. Moreover, we show that larger TTLs are not efficient in compensating for the object fetch delay especially in caching hierarchies. Interestingly, for request processes that approach a periodic behavior it can be shown that the hit probability is not monotonically decreasing in the delay. To reduce the computational complexity of the calculation of performance measures for TTL caching trees we provide an analytical approach to state lumpability that takes advantage of symmetric sub-trees of caches within a hierarchy.

Our contributions can be summarized as follows:

- We provide an exact analysis of TTL cache hierarchies under non-zero object fetch delay. In addition, we generalize the existing models to Phase-type distributed inter-request times, TTLs, and delays.
- We analyze the computation complexity of the exact performance model and provide a rigorous computational speedup method for calculating exact cache performance metrics based on a MAP lumpability argument taking into account cache tree symmetry and recursion.
- We provide numerical and trace-driven simulation results that show the significant detrimental impact of network delays on cache hierarchy performance, as well as, the accuracy of our model. Further results also show the non-trivial approximation error due to state-of-the art approximation methods.

The remainder of the paper is structured as follows: We first provide an overview of related work on modeling and analyzing TTL caches in Sect. 2 before describing the system model and the problem statement in Sect. 3. In Sect. 4 we analyze cache hierarchies under object fetch delays. In Sect. 5 we derive performance metric approximations for single caches and for cache hierarchies and in Sect. 6 we provide a model-based approach to speed up the numerical calculation of cache hierarchy performance metrics. Finally, in Sect. 7 we show numerical and trace-based simulation results before concluding the paper in Sect. 8.

2 Background and Related work

Time-to-Live caches decouple the management of objects in the cache. The inclusion and removal of an object from the cache is based solely on the request process for that object and its TTL, i.e., the validity timestamp assigned to the object. An object request generates either a hit if the object is present in the cache's local memory, or a miss if not. In the case of a hit, the object is delivered to the request source immediately. In the case of a miss, the object is requested from another cache in the cache hierarchy (or finally the origin server) according to a specified routing algorithm. Upon receiving the object the cache that generated the miss in the first place forwards the object to the request source and adds it to local storage with a validity timestamp, the TTL. Objects are removed from local storage upon TTL expiry. TTL can be regenerative or fixed, i.e., renewing upon an object hit or not, respectively. TTLs can also set deterministically or randomly with a given distribution. Different methods exist for selecting and optimizing TTLs \[7, 17\] to optimize the cache performance. The work in \[9\] shows that the number of TTL cached objects in one cache follows a concentrated distribution. Further work shows how parameterization rules for TTLs lead to statistically equivalent cache performance when compared to some classical caching algorithms such as LRU. An established argument for this relates the expected cache occupancy to cache capacity \[6, 7, 18–20\].

2.1 Single Cache Analysis

State-of-the-art analytical models of TTL caches usually assume idealized communication such as negligible object fetch latency, no losses, no network dynamics, and no link capacity constraints \[6–9, 11–13\]. Fur-
Considering a single cache as depicted in Fig. 1 (left), the standard analysis assumes a renewal request process for any given object as depicted in Fig. 2. The inter-request time is given by the independent and identically distributed (IID) random variables $X_i \sim X$. The IID random variables $T_i \sim T$ denote the TTLs, whereas the object fetch delay is zero (i.e. $\Delta = 0$ in Fig. 2) and $Y$ represents the inter-miss time. Given this model, a cache hit occurs when the inter-request time is less than the TTL and the object hit probability $P_h$ is [6]

$$P_h = \mathbb{P}(X < T) = \int_0^\infty (1 - F_T(t))dF_X(t),$$

where $F_T(t)$ and $F_X(t)$ are the CDFs of the TTL and the inter-request time, respectively. Hence, the Laplace-Stieltjes Transform (LST) $F_Y^*(s)$ of the inter-miss time with CDF $F_Y(t)$ is given by [6]

$$F_Y^*(s) = \frac{F_X^*(s) - L^*(s)}{1 - L^*(s)},$$

(1)

where $F_X^*(s)$ is the LST of the inter-request time and $L^*(s)$ is the LST of $L(t) = \int_0^t (1 - F_T(t))dF_X(t)$.

### 2.2 Analysis of TTL Cache Hierarchies

At the core of the analysis of cache hierarchies lies the problem of describing the superposition of miss processes coming from different child caches as input to one parent cache. The standard approximation for this superposition is given by the assumption that the miss process of any cache follows a Poisson process parameterized with the cache miss probability. This approximation, however, deviates significantly from the exact miss process, especially when there are multiple levels of caching within the hierarchy [7]. The work in [6] provides an exact expression for the miss process of a single cache under zero fetch delay as a function of a renewal input process and the TTL, however, this exact approach is not extended to hierarchies. Relaxing the Poisson assumption of the request process to renewal processes allows to model a large class of request processes [6, 8, 14, 24], but due to the superposition properties of renewal processes, assuming that the multiplexed miss process is renewal leads to significant approximation errors in the analysis of caching hierarchies.
The authors of [7] provide an exact analysis of caching hierarchies under zero fetch delay including miss process superposition using Markov arrival processes (MAPs). A MAP is defined using two transition matrices \((D_0,D_1)\) of same size that contain hidden and active transitions, respectively. The matrix \(D_0\) controls a background Markov process \(J(t)\) while \(D_1\) controls \(N(t)\), as well as, a counting process \(N(t)\) (for an introduction see [25]). For example, for a given cache with Poisson request process with rate \(\lambda\) and exponentially distributed TTL with parameter \(\lambda_T\) the state for one object is shown in Fig. 1 (right). The elegant modelling using MAPs in [7] allows to exactly express the superposition of miss-processes using the Kronecker sum and Kronecker multiplication operations on the corresponding MAPs. The object hit probability is given thus as [7]

\[
P_h = 1 - \frac{\pi D_1 1}{\pi(t) D_1^{(t)} 1^{(t)}},
\]

where \(D_1\) is the active matrix of the caching system MAP and \(\pi\) is the vector of the corresponding steady state probabilities. The active matrix \(D_1^{(t)}\) and the probability vector \(\pi^{(t)}\) are similarly defined for the MAP representing the input process of requests arriving to the caching system. The vectors \(1\) and \(1^{(t)}\) are all ones.

Taking the object fetch delay into account, the approach in [10] showed first analytical results to incorporate the communication latency for a single TTL cache into the exact analysis. However, to extend this analysis to hierarchies the work [10] resorts to the inaccurate Poisson multiplexing approximation, i.e., assuming that the miss process of every cache is Poisson. Recall that this assumption has been shown to produce significant errors (even in the zero object fetch delay regime) [7]. Further work that considers the download delay time for objects in single LRU caches includes [26,27], where the authors propose variants of the LRU algorithm that work better under non-zero delay by jointly analyzing single LRU caching and pending interest table (PIT) that contain object requests that are not yet fetched. The authors of [28] consider the object download delay and propose an algorithm based on q-LRU to optimize the average latency based on the popularity of the object and its size.

On a different note, approaches that optimize TTL caching hierarchies, e.g., using utility functions can be found in [29,30]. Starting from a formulation as an optimization problem, TTL values that maximize the hit probability are sought in [17,30,31]. This problem is solved for heavy-tailed arrivals in [31]. In [32], a caching optimization problem with linear cost functions is proposed and solved. In [33], a utility-based approach is proposed to model the caching problem as a Nash bargaining game, where in [34], a utility-based approach to cache partitioning is proposed for cache resource allocation. Other related caching algorithms, but not TTL specific [35,36], attempt to minimize the average cost of misses, where the cost of an object is given by, for example, the variability in latency or computation cost. Other approaches that consider cache optimization such as [37–41], attempt to optimize given cache utility offline. This is different from the approach of the paper at hand as we model caching under non-zero random object fetching delays.

How our contributions differ from [7,10,26–28]: While [10] analyzes cache hierarchies under non-zero object fetch delays using approximations, our work differs significantly as we exactly analyze the caching hierarchies under non-zero delay. In Sect.5 and in the evaluations in Sect. 7 we discuss and show the significant approximation error for cache hierarchies. Note that the work in [10] is exact in case of a single cache. Further, our work is different from [26–28] due to the same technical reasons, as well as, the fact that we consider a fundamentally different caching algorithm (TTL instead of LRU). Our contributions also differ from the work in [7] which assumes zero object fetch delay and focuses on the derivation of cache performance metrics. Calculating the performance metrics as in the work [7] suffers from high computational complexity due to state explosion of the Markovian model. In contrast we generalize the exact model here to non-zero object fetch delays and analyze the cache performance metrics under the effects of network delays. To tackle the problem of the exploding computational complexity of the calculation of exact cache performance metrics we derive a model-based exact speed-up method that is based on lumpable partitions and automorphisms in the corresponding MAP. Finally, we include numerical and trace-based evaluation results to show the accuracy of our model as well as the impact of the network delays on the cache performance.

3 System Model and Problem Statement

When cache hierarchies are formed on-top of (or within) communication networks, cache misses require some random latency until the sought objects are retrieved from other caches or from the origin server. This
latency results from processing and forwarding miss requests and objects, along predefined routing paths between leaf and parent caches.

Fig. 2 shows one cycle of the miss process where, without loss of generality, the first request comes at time $t = 0$ and the object is initially not in cache. The figure shows that the object is admitted after some random object fetch delay $\Delta$ and is evicted when the TTL expires. We also depict regenerative TTL that is refreshed upon each hit (black arrow). We count requests that arrive during the object fetch delay (dashed arrows) as misses as the object is not fetched yet. The excess lifetime of the renewal request process at time $\Delta$ is $\Gamma_{\Delta}$.

Essentially, the shift towards relatively large request latencies in comparison to inter-request times that has been reported recently in [15] implies that the impact of the delay on the cache performance is significant and increasing. This shift is due to extremely fast data center communication compared to memory access, processing and forwarding of miss requests [16]. Recent empirical approaches [15] attempt to incorporate this behavior in a problem description based on a minimum-cost multi-commodity flow formulation. This motivates our approach to an exact model of TTL cache hierarchies under non-negligible object fetch delays.

The work in [10] calculates the object hit probability at a single cache under non-zero delay as
\[
P_h = \frac{E[N]}{1 + E[m(\Delta)] + E[N]},
\]
where $N$ is a counting random variable representing the number of hits between two misses and $m(\Delta)$ is the expected number of requests within the delay $\Delta$. Moreover, the work in [10] specifies the inter-miss distribution as
\[
F_Y(y) = \int_0^{y} \left[ H_0^\delta(y) P(N = 0|\Delta = \delta) + \sum_{n=1}^{\infty} \left( H_1^\delta \ast L_2 \ast L_1^{(n-1)}(y) \right) P(N = n|\Delta = \delta) \right] dF_\Delta(\delta),
\]
with $F_\Delta(\delta)$ being the CDF of the delay, and $H_0^\delta(\cdot)$ is the distribution of the excess lifetime $\Gamma_{\Delta}$ given no hits in one cycle. Similarly, $H_1^\delta(\cdot)$ is the distribution of the excess lifetime given at least one hit in the cycle. Further, $L_1$ and $L_2$ denote the conditional distribution of the inter-request time $X$ given that it is less or it is larger than the TTL $T$, respectively. To obtain an exact analysis for cache hierarchies, a closed-form expression is needed for the superposition of request processes at a cache under random object fetch delays. These request processes may themselves be the miss processes of children caches. While [10] provides an expression for the miss process under random fetch delay at a single cache, it is notoriously difficult to extend this expression towards the exact superposition of miss processes. The analysis in [10] hence resorts to approximating the aggregation of miss processes as a renewal process to analyze cache hierarchies. Similarly, in [42] the cache hierarchy analysis under non-zero fetch delay is based on the assumption of Poisson miss processes.

### 4 Exact Cache model with Object Fetch Delays

In this section, we use a technique based on Markov arrival processes to model TTL caching hierarchies when random object fetch delays are present. We first show how the object fetch delay is incorporated into the MAP representation of a single cache before expanding to tree-like caching hierarchies. To introduce our approach, we first consider exponentially distributed inter-request times, TTLs and delays. In resemblance to Kendall’s notation we call such a system M/M/M caching system (in the order inter-request times at the system input, TTLs, delays). Consequently, we generalize the approach to caching systems under Phase-type (PH) distributions that describe the request process as well as the delays. We choose PH distributions as these are dense in the class of distributions describing requests and delays. At the end of this section we discuss the computational complexity of our approach.

#### 4.1 Single M/M/M Cache

As TTL caches decouple objects it is sufficient to analyze the caching process for one object [6]. First, we show how to incorporate the object fetch delay into the MAP representation of a single cache. Fig. 4a shows
Figure 3: Construction of the hierarchy MAP through iteration of level and line superposition.

Figure 4: Basic MAPs of different caching setups: \textit{State 1, State $F$ and State 0 denote object in cache, object being fetched or object out of cache respectively.} Combination of States depends on the semantics of the hierarchy, i.e. whether the MAP is for a combination of leaf caches or child/parent caches.

The MAP for one object at a single M/M/M cache. Here, the MAP has three states capturing the life cycle of the object in the system.

When an object request arrives to the cache, it can find the object in cache (State 1) or being fetched from the origin (State $F$) or the object is neither in cache nor being fetched which we denote “out of cache” (State 0). We define a \textit{cache miss} as a request arriving when the object is not in cache. Hence, the active \textit{transitions} in the MAP denote misses that happen when a request arrives in states 0 or $F$. In contrast to the classical cache analysis the object is not instantaneously admitted upon a miss due to the fetching delay between the cache and the origin server. In this first step we consider exponentially distributed fetch times with parameter $\lambda_{\Delta}$. We generalize the delay model in the following sections. Hence, the hidden and active matrices of the MAP are

$$
D_0 = \begin{bmatrix}
-\lambda & 0 & 0 \\
\lambda_T & -\lambda_T & 0 \\
0 & \lambda_{\Delta} & -\lambda_{\Delta} - \lambda
\end{bmatrix}, \quad D_1 = \begin{bmatrix}
0 & 0 & \lambda \\
0 & 0 & 0 \\
0 & 0 & \lambda
\end{bmatrix},
$$

where $\lambda$ is the request arrival rate, $1/\lambda_T$ is the mean TTL and $1/\lambda_{\Delta}$ is the mean fetch delay.

4.2 Construction and Analysis of Cache Hierarchies

We first consider one object that is contained in a tree caching hierarchy as depicted in Fig. 3. The figure shows an “algorithmic” overview of the steps of our approach for the incorporation of the delay into the MAP model of the cache hierarchy. First, caches on the same level, i.e., having the same parent, are grouped together through an operation that we denote \textit{level superposition}. In the next step, parent and child caches are grouped through an operation denoted \textit{line superposition}. Now we can build the overall MAP from the MAPs of the single caches starting from the leaf nodes until the root. Level and line superposition correspond to non-trivial compounding of the MAPs of the single caches. We expand the definition of a
miss to caching hierarchies to denote object requests where the object is not fetched from caches within the hierarchy but from the origin server.

4.2.1 Level superposition (Φ)

The level superposition forms a MAP from two separate sub-trees connected directly to the same parent node. The level superposition for caches under the zero-delay assumption was shown first in [7]. Here, the MAP (M) resulting from the superposition is formed by the Kronecker sum ⊕ of the two MAPs (M₁, M₂) of the two sub-trees as

\[ M = M_1 \oplus M_2 \]

\[ (D_0, D_1) = (D_0^{(1)}, D_1^{(1)}) \oplus (D_0^{(2)}, D_1^{(2)}) \]

where \(D_0^{(i)}\) and \(D_1^{(i)}\) are the hidden and active transition matrices of \(M_i\), respectively. As the two sub-trees receive independent request streams, the Kronecker sum produces the exact states with the right transitions between them. A basic example of the level superposition is of two separate caches described each by (5) that are connected to a parent cache. Applying the Kronecker sum we obtain the MAP in Fig. 4b.

4.2.2 Line superposition (Ψ)

Line superposition involves constructing the MAP for a parent node and the sub-tree below it. In contrast to level superposition, the caches considered in line superposition are dependent. We carry out the line superposition using the following four steps:

Kronecker sum As the parent cache is not associated with a direct request stream the active transition matrix of the MAP representing the added parent is given by \(D_2^{(2)} = 0\) where the superscript denotes the cache id along the line. Performing the Kronecker sum on the MAP of the parent cache and the existing MAP of the sub-tree of children results in all state combinations. Due to the dependency between the parent cache and the children sub-tree connected to it, not all possible state combinations are valid and need to be removed. We consider in the following two caches in line for simplicity, however, the MAP of the child cache can well be a superposed caching sub-tree. Note that the result of the Kronecker sum exactly represents the overall MAP only when dealing with two independent MAPs where the transitions are given by

\[ M^{(ij \rightarrow i'j')} = \begin{cases} 
M_1^{(i \rightarrow i')} & \text{when } j = j' \\
M_2^{(j \rightarrow j')} & \text{when } i = i' 
\end{cases} \]

(6)

where \(M^{(ij \rightarrow i'j')}\) represents the transition in the resulting MAP \(M\) from state \(ij\) to \(i'j'\) where \(ij\) represents the state superposition of state \(i\) from \(M_1\) and state \(j\) from \(M_2\).

Fig. 4c describes the MAP of two caches in line. This example is used in the following to illustrate the changes required after the Kronecker sum to produce a MAP that exactly represents the combined behavior of the caches after line superposition.

Removal of invalid states and transitions Observe that when comparing the MAP resulting from the Kronecker sum in Fig. 4b to the final MAP in Fig. 4c there are two removed invalid states when dealing with two caches in line which are 0F and 1F. State 0F denotes that the object is out of the child cache and is being fetched by its parent which contradicts our assumption that objects are fetched by the parent based on a request by the child cache. Further, the state 1F denotes that the object is in cache at the child while being fetched by the parent which obviously violates causality. Based on this observation, the hidden and active matrices are updated by removing the rows and columns of the invalid states.

Applying this idea to tree hierarchies, we build the MAP for the hierarchy with line superposition applied when \(M_2\) represents the parent MAP and \(M_1\) represents the superposition of all of its children. Note that in this case the invalid states set \(I\) is defined by

\[ I = \bigcap_{k=1}^{n_{ch}} I_k \]

(7)
where $I_k$ is the invalid states set of an added parent cache and its child $k$ as given by the two node example and $n_{ch}$ is the number of children caches.

Further, the hidden transition in the Kronecker sum given by $M^{(FF \rightarrow 1F)}$ is invalid and removed as the object is admitted in the parent cache before the child. Note that in the two cache case, this transition is obsolete as the state $1F$ is removed as stated above, however, in general for a parent cache and a child sub-tree this type of transition is generally removed.

**Accounting for system hits by moving transitions from $D_1$ to $D_0$** Since the active transitions are related to requests which induce misses, when performing line superposition some of the requests no longer generate a system miss as the object is contained in the parent cache. Hence, the Kronecker sum of the active matrices is adapted to account for that fact. The following active transitions are moved from $D_1$ to $D_0$:

$$M^{(ij \rightarrow i'j)} \text{ for } i, i' \in S_1 \text{ and } j \neq F,$$

where $S_1$ represents the set of the states of the MAP $M_1$ of the connected sub-tree. To illustrate this, we first consider the case of two caches in line (Fig. 4c). Now it is obvious that the transition $M^{(01 \rightarrow F1)}$ is hidden as it does not denote a system miss. Moreover, this argument also holds for the self transitions $M^{(F1 \rightarrow F1)}$ and $M^{(F0 \rightarrow F0)}$. Note that we do not draw the hidden self transitions in Fig. 4c.

**Updating $D_0$ and $D_1$ for system misses** Finally, a single transition of the Kronecker sum is adapted to express the system miss. Considering first the line superposition of a child and a parent cache we observe that when a request generates a system miss, i.e., when the two caches are in state 0, the child cache fetches the object from its parent and the parent fetches the object from the origin server. Thus the transition obtained by the Kronecker sum as $M^{(00 \rightarrow F0)}$ in $D_1$ is replaced by the corresponding transition $M^{(00 \rightarrow FF)}$.

The four preceding steps to calculate the overall system MAP for a general tree cache hierarchy with one parent/root and $l-1$ children are given in Algorithm 1. Here, the caches are labeled from 1 to $l$ such that 1 and $l$ represent the first leaf cache and the root, respectively. The function children($i$) returns the indices of the children of cache $i$. $M_i$ represents the MAP of a single cache $i$ while $M_{l,i}$ represents the MAP of the sub-tree with root $i$. The functions $\Phi$ and $\Psi$ represent the level and line superposition, respectively. $M_{vl}$ represents the MAP obtained from the level superposition $\Phi$. Note that $\Phi(0) = 0$ and $\Psi(M_{i}, 0) = M_{i}.$

**Algorithm 1: Calculation of the combined MAP for a tree caching topology**

| Input: $M_i$ $i \in \{1, \ldots, l\}$. |
| Result: $M_{l,1}$ |
| Initialization: $i = 1$, $M_{t,i} = 0 \forall i \text{ s.t } \text{children}(i) = 0$; |
| while $i \leq l$ do |
| $M_{vl} = \Phi(M_{t, \text{children}(i)});$ |
| $M_{t,i} = \Psi(M_{i}, M_{vl});$ |
| end |

**4.3 M/M/PH Caching System**

Next, we generalize the approach illustrated above to M/M/PH caching systems where the delay is PH distributed. Recall that the PH distribution is dense in the class of positive-valued distributions making it a good approximate for trace-based evaluations.

In case of PH distributed delay, the fetching process is given by a multiple state MAP $M_F$ with states $F_\alpha$ where $\alpha \in \{1, 2, \ldots, f\}$ and $f$ represents the number of the phases. Without loss of generality, we use here an Erlang $E_f$ delay distributions with $f$ states to illustrate our approach. For a single M/M/PH cache we provide the MAP in Fig. 5 highlighting the $E_f$ fetching process.
The corresponding transition matrices of the single cache MAP are given as

\[
D_0 = \begin{bmatrix}
-\lambda & 0 & 0 & 0 & 0 \\
\lambda_T & -\lambda_T & 0 & 0 & 0 \\
0 & \lambda_\Delta & (-\lambda_\Delta - \lambda) & 0 & 0 \\
0 & 0 & \ddots & \ddots & 0 \\
0 & 0 & 0 & \lambda_\Delta & (-\lambda_\Delta - \lambda)
\end{bmatrix}, \\
D_1 = \begin{bmatrix}
0 & 0 & 0 & 0 & \lambda \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & \lambda & 0 & 0 \\
0 & 0 & 0 & \ddots & 0 \\
0 & 0 & 0 & 0 & \lambda
\end{bmatrix}.
\]

Similar to the derivation of the MAP for M/M/M caching hierarchies we apply the same operations of level and line superposition for the M/M/PH caching hierarchy. To this end, we essentially define the line superposition in a general manner to capture PH delay distributions.

We show how to generalize the four main steps given in Sect. 4.2.2 for PH delay distributions. The Kronecker sum in the first step is applied without changes. The second step represented by removing the invalid states is generalized next. As the fetching process is represented by multiple states, the invalid states are defined for all state combinations. Note that in case of exponential delay distribution, the invalid states are defined by the two states 0\(F\) and 1\(F\). For PH delay distribution, the invalid states due to a child cache \(k\) represented by multiple states \(F_\alpha\) are given as

\[
I_k = \{0 F_\alpha, 1 F_\alpha, F_\beta F_\alpha\}
\]

\(\alpha \in \{1,...,f\}, \beta \in \{1,...,f-1\}\).

The first two state combination sets 0\(F_\alpha\) and 1\(F_\alpha\) are analogous to the case of exponential delay distribution. However, given PH distributed delays the invalid state combinations \(F_\beta F_\alpha\) when \(\alpha \in \{1,...,f\}\) and \(\beta \in \{1,...,f-1\}\) arise. This comes from causality, i.e., object fetching ends at the parent cache before starting at the child. The third step in Sect. 4.2.2 representing the transitions to be changed from active to hidden is extended such that self transitions include all the fetching states. Hence, the states changed from active to hidden are given by

\[
M^{(i \to i')}_j \quad \text{for } i, i' \in S_1 \text{ and } j \neq F_\alpha \forall \alpha.
\]

The final step is analogous to the case of the exponential distribution, i.e. changing the transition \(M^{(00 \to F_0)}\) to \(M^{(00 \to F_0 F_0)}\).

### 4.4 PH/M/M/M Caching System

Next, we generalize the Poisson request processes to show how to form the MAP of a caching hierarchy for PH distributed inter-arrival times. First, considering a single PH/M/M cache we show two required steps to form the MAP. We regard two separate MAPs; one representing the arrival process which we denote as \(M_A\) and the other representing the TTL and the fetching processes denoted by \(M_{FD}\). We form the MAP by (i) applying the superposition between \(M_A\) and \(M_{FD}\) and (ii) changing the transitions resulting in misses. For illustration the MAPs \(M_A\) and \(M_{FD}\) for an E2/M/M system are shown in Fig. 6. \(M_A\) can be shown to have transition matrices

\[
D_0 = \begin{bmatrix}
-\lambda_1 & \lambda_1 \\
0 & -\lambda_2
\end{bmatrix}, \\
D_1 = \begin{bmatrix}
0 & 0 \\
\lambda_2 & 0
\end{bmatrix}.
\]
while $M_{FD}$ is represented by

$$D_0 = \begin{bmatrix} 0 & 0 & 0 \\ \lambda^T & -\lambda^T & 0 \\ 0 & \lambda_\Delta & -\lambda_\Delta \end{bmatrix}, \quad D_1 = 0.$$  

The second step, i.e. changing the transitions that result in misses, requires the modification of the two active transitions $M^{(0A_2\rightarrow 0A_1)}$ and $M^{(1A_2\rightarrow 1A_1)}$. The first represents an arrival when the object is not in the cache, therefore the transition is changed as $M^{(0A_2\rightarrow FA_1)}$. The latter transition should not be an active transition as the object is not in the cache. The resulting MAP of the superposition before the modification of the two active transitions is shown in Fig. 7.

The MAP formation of the caching system requires performing level and line superposition according to the topology. Note that the previously discussed MAP extension depends on the delay MAP. Changing the request input process influences the MAP formation as in that every transition or state to be changed exists a number of times as many as the states of the input process. We do not show the derivation of PH/M/PH as it is straightforward given the analysis in this section.

### 4.5 Computational Complexity Discussion

In this subsection, we discuss the computational complexity of our MAP approach for caching trees. Further, we show the computational complexity for calculating the hit probability.

Our MAP approach is based on the level superposition and the line superposition operations. First, the computational complexity of the level superposition operation is that of the Kronecker sum. The Kronecker sum of two square matrices of size $m_1$ and $m_2$ results in a square matrix of size $m_1m_2$. The only operation involved between the elements of both matrices are addition operations. Thus, the level superposition affects first the memory requirement and assignment.

On the other hand, the computational complexity of line superposition operation is that of its four steps. Except for the first step (Kronecker sum), the three other steps have a complexity of a search function in the state set. For example, the identification of the invalid states requires a search through the state set. Let the first step be a Kronecker sum between the MAP of a parent cache with $m_p$ number of states and the MAP of the children sub-trees with size $m_{ch}$ number of states. The computational complexity of the Line superposition, i.e., the search in the state set with size $m_p m_{ch}$ in a tree is $O(\log(m_p m_{ch}))$. Here, $m_p = m_c$, i.e. the number of states of a single cache MAP which is given for a defined caching system with stationary stochastic parameters (input, TTL and delay). The complexity of our MAP approach is then determined by the search complexity $O(\log(m_p m_{ch}))$ in the number of states. At each step of constructing the system MAP starting from the leaves to the root, $m_{ch}$ increases exponentially depending on the number of caches.
n represented. Therefore, we know for $m_{ch}$ that

$$m_{ch} \sim O(m_c^n).$$

Although each step of our approach has a complexity corresponding to the number of the caches involved, overall we find the complexity of system MAP construction to be $O(\log(m_c^{nc})) = O(n_c \log(m_c))$, where $n_c$ denotes the total number of caches of the hierarchy. Therefore, the complexity of constructing the overall MAP grows linearly with the number of caches in the system. For example, a binary M/M/M tree with $L$ levels has a complexity of $O(2^{L-1} \log(3))$.

The calculation of the hit probability depends on the steady state probability of the states denoted $\pi$ in (2). The calculation of the steady state vector has a complexity of solving a system of $m_{cn}$ linear equations. Thus, it has a time complexity of $O(m_c^{5n_c})$ with $\xi \in (2.4, 3]$ [43].

5 Approximation for single caches and cache hierarchies under non-zero delay

5.1 Approximation for single caches under non-zero delay

Motivated by the high computational complexity of the calculation of the CDF of the inter-miss times for a single cache in (3)-(4) we provide a computable approximation for the Laplace-Stieltjes transform (LST) of the inter-miss times $F_Y(s)$ that also permits calculating the hit probability given renewal inter-request times, and arbitrary distributions of the TTL and the delay $T$. Note that (4) contains iterative convolutions making it practically only computable for simple inter-arrival time distributions such as the exponential distribution. In contrast to (3)-(4) the following approximation can readily be incorporated in analytical methods to model entire caching hierarchies. Our approximation is based on the following:

Assumption 1. Given a miss there exists a request arrival at the instant the object is admitted to the cache, i.e., exactly at the end of the object fetch delay duration.

Proposition 1. Under Assumption 1 and given the object fetch delay LST $F_{\Delta}^X(s)$, the LST of the renewal inter-request time $F^X_s(s)$ and the LST of the joint probability $L^*(s)$ from Sect. 2.1 at a single cache, the LST of the inter-miss time is

$$F_Y^*(s) = \frac{F_{\Delta}^X(s)[F^X_s(s) - L^*(s)]}{1 - L^*(s)}. \quad (8)$$

Proof. We calculate the probability that the inter-miss time $Y < t$ for inter-request time $X > T$ as $P(X + \Delta < t)$. Hence, the CDF of the inter-miss times is given by

$$F_Y(t) = P(T < X < t - \Delta) + P(Y < t, X < t, X < T),$$

We manipulate the terms as

$$P(T < X < t - \Delta) = P(X < t - \Delta) - P(X < T, X < t - \Delta) = E[F_X(t - \Delta)] - E\left[\int_0^{t-\Delta} (1 - F_T(x))dF_X(x)\right],$$

$$P(Y < t, X < t, X < T) = E[F_Y(t) 1_{X<t,X<T}] = \int_0^t F_Y(t)(1-F_T(x))dF_X(x),$$

to express $F_Y(t)$ in terms of the PDFs and CDFs of the TTL and the inter-request time as

$$F_Y(t) = E[F_X(t - \Delta)] - E\left[\int_0^{t-\Delta} (1 - F_T(x))dF_X(x)\right] + \int_0^t F_Y(t)(1 - F_T(x))dF_X(x), \quad (9)$$

1 as long as the corresponding Laplace transform exists.
Note that we marginalized here over the random variable $\Delta$. Using $L(t)$ from Sect. 2.1 and by substitution in (9) as well as expressing the CDF of the inter-miss times in terms of the delay we obtain

$$F_Y(t) = \int_0^\infty F_X(t-\delta) dF_\Delta(\delta) - \int_0^\infty L(t-\delta) dF_\Delta(\delta) + \int_0^t F_Y(t-x) dL(x).$$ (10)

Note that $F_Y(t)$ is replaced with $F_Y(t-x)$ in the last term since $F_Y(t) = F_Y(t-x)$. This is a property of the renewal process [44]. As a result, $F_Y(t)$ is expressed in a recursive form. Taking the LSTs we obtain

$$F^*_Y(s) = F^*_X(s)F^*_\Delta(s) - L^*(s)F^*_\Delta(s) + F^*_Y(s)L^*(s),$$

which completes the proof. 

We observe that the closed form above is similar to the result of the zero delay expression in (1). Both can be further related by $F^*_Y(s) = F^*_\Delta(s)F^*_Y(s|\Delta = 0)$. This is intuitive in light of Assumption 1. Next, we use Assumption 1 to approximate the object hit probability. Note that the probability of the number of hits $N$ between two misses being $n$ can be represented by

$$P(N = n) = \begin{cases} P(X > T) & \text{for } n = 0 \\ P(X < T)^n P(X > T) & \text{for } n > 0. \end{cases}$$

Letting $q = P(X < T)$, $E(N)$ is given from the geometric distribution as

$$E(N) = \frac{q}{1-q}. \quad (11)$$

Next we compare the hit probability given non-zero object fetch delay to that under the zero delay assumption. To this end, we use the following definition:

**Definition 1.** The delay impairment $\eta$ under random delay $\Delta$ is defined as

$$\eta := 1 - \frac{P_h|\Delta \geq 0}{P_h|\Delta = 0}, \quad (12)$$

with $P_h$ denoting the object hit probability.

This ratio $\eta \in [0, 1]$ describes the reduction of the hit probability due to the object fetch delay, i.e., for $\eta = 0$ there is no reduction in the hit probability, whereas $\eta = 1$ denotes that the hit probability under delay is reduced to 0.

**Lemma 1.** Given Assumption 1 the delay impairment for a single M/M/M cache is

$$\eta = \frac{\bar{\tau}_\Delta}{\bar{\tau}_T + \bar{\tau}_\Delta + 1}. \quad (13)$$

Here, the ratio of the expected delay $E[\Delta]$ to the expected inter-request time $E[X]$ is defined as $\bar{\tau}_\Delta := E[\Delta]/E[X]$. Further, the ratio of the expected TTL $E[T]$ to the expected inter-request time is defined as $\bar{\tau}_T := E[T]/E[X]$. Obviously, the delay impairment $\eta$ in (13) increases monotonically from 0 to 1 as $\bar{\tau}_\Delta$ increases from 0 to $\infty$. In addition, we observe that the delay impairment $\eta$ decreases with the expected TTL which suggests that the reduction in hit probability due to larger delays can be compensated by larger TTL. However, considering the rate of change of the delay impairment with respect to the expected TTL $\frac{\partial \eta}{\partial \bar{\tau}_T} = \frac{\bar{\tau}_\Delta^2}{(\bar{\tau}_T + \bar{\tau}_\Delta + 1)^2}$ we conclude that compensating the object fetch delays using longer TTLs is disproportionately expensive.
5.2 Approximations for caching hierarchies under non-zero delay

Next, we extend the approximate caching hierarchy model in [6] to consider random object fetching delays. We will compare this approximation to our exact MAP based model in the following evaluation section.

Similar to the level superposition and line superposition operations defined in the context of MAPs in Sect. 4, the two main operations required in [6] to model a caching system are (i) Input-output operation and (ii) Superposition of the miss process of multiple caches. Assuming zero delay, the input-output operation is used to exactly calculate the miss process of a given cache given the input process according to (1). Further, [6] approximates the superposition of renewal miss processes as a renewal process. Finally, the input request rate into each parent cache in the system is calculated recursively as the sum of input rates to the children caches each weighted by their respective miss probabilities.

Here, we extend this approximation to incorporate non-zero random object fetch delay. We use our approximation from Proposition 1 to carry out the input-output operation according to (8) instead of (1). In addition, we calculate the hit probability of each cache according to (3) and (11) using \( m(\Delta) \) from [10]. Note that the superposition operation as defined by [6] remains unaffected by the delay. Now, a challenge facing the straightforward extension of the model from [6] to incorporate the object fetch delay, is that this model lacks a metric for calculating the system hit probability. There the system hit probability is not proposed nor used to evaluate the cache hierarchy. We opt here to use the classical method from [20] to calculate the system hit probability, i.e.,

\[
P_{h,sys} = 1 - \frac{M_{r,out}}{\sum_{i=1}^{K} \lambda_i},
\]

where \( M_{r,out} \) is the output miss rate, i.e the miss rate of the root cache and \( \lambda_i \) represents the input rate to the leaf cache \( i \) while \( K \) denotes the number of leaf caches in the system. Here, the system miss probability is obtained as the ratio of the output to the input rate of the cache hierarchy.

6 Computable performance metrics for large Cache hierarchies through MAP Lumping

In this section, we show how to reduce the state set size of the caching tree MAP to reduce the computational complexity of the cache performance metric computation. Here, we use graph automorphisms to define equivalent states which are then lumped together and denoted as a lumpable partition.

The equivalent states within a MAP are the states that have the same description of the object status within the caching system. To illustrate this, we use the example of a cache system consisting of two leaf caches as represented by the MAP in Fig. 4b. For example, state "10" in Fig. 4b denotes that the object is stored in the first cache only while state "01" denotes that the object is stored in the second cache only. If the two caches are symmetric in terms of the request processes, the TTL and the delay distributions, the order of the caches having the object is irrelevant and the system description is identical when having the object in either of the caches. Here, it is clear that states "01" and "10" are hence equivalent states and can be lumped together. In general, we denote each group of equivalent states within a MAP as a lumpable partition while the number of lumpable partitions is given by \( N_p \). To reduce the state set of a given MAP, we find all lumpable partitions and represent each of them using only one of their states, thus we only use \( N_p \) states for the final performance metric computation.

We observe that the problem of finding lumpable partitions within a MAP that represents a caching tree is equivalent to first finding the automorphisms of a graph featuring the caching tree. Then, we can let the automorphism group act on the states set \([45, 46]\). We focus in the following on finding the lumpable partitions.

Given a caching hierarchy with depth \( L \) (denoted the number of levels) and defining the set \([L] = \{1, \ldots, L\}\). We call a caching tree homogeneous when the caches on the same level have the same input, TTL and delay distributions, i.e.,

\[
F_{X_{i,j}}(t) = F_{X_{i,k(t)}}, F_{T_{i,j}}(t) = F_{T_{i,k(t)}}, F_{\Delta_{i,j}}(t) = F_{\Delta_{i,k(t)}}, k \in [n_i], j \in [L],
\]
where $F_{X_{i,j}}(t)$, $F_{T_{i,j}}(t)$ and $F_{\Delta_{i,j}}(t)$ are respectively the input (inter-request time), TTL and delay distribution of the $j$th cache in the $i$th level. Here $n_i$ is the number of caches in level $i$ and $[n_i] := \{1, \ldots, n_i\}$.

We represent the homogenous cache tree with a graph $G(V, E)$ whose vertices $V \in [n_c]$ are the caches, where $n_c$ is the total number of caches in the hierarchy, and the edges in $E$ denote their connections.

**Definition 2.** A bijection $f : V \rightarrow V$ is an automorphism of $G$ if for $(i,j) \in E$ $(f(i), f(j)) \in E \forall i, j \in V$, i.e., it is a permutation of the graph vertices that retains the edges. The set of all the automorphisms $f$ that are defined on the graph $G$ forms a group $\text{Aut}(G)$ under function composition [47].

Given the set of states of a MAP of a single cache $\gamma$, as depicted for example for an M/M/M or an M/M/E/$c$ cache in Fig. 4a or Fig. 5, respectively. In order to find the lumpable partitions, we let $\text{Aut}(G)$ act on $\gamma^{n_c} - I$ where $I$ is the set of the invalid states defined in (7). Note that for a state $u \in \gamma^{n_c}$, $u_i \in \gamma$ for $i \in [n_c]$. For example, for Fig. 4b we have $u \in \gamma^{2}$ with $u_i \in \{0,1,F\}$, i.e. when $u = (1,F)$ (that is the depicted state $1F$ in the figure) then $u_1 = 1, u_2 = F$. The group action is a map $\text{Aut}(G) \times \gamma^{n_c} - I \rightarrow \gamma^{n_c} - I$ defined by

$$f.u = v \leftrightarrow u_i = v_{f(i)} \forall i \in [n_c], \forall f \in \text{Aut}(G), u \text{ and } v \in \gamma^{n_c} - I,$$

(14)

using the equivalence relation $\leftrightarrow$. This group action on $u$ is the permutation of the elements of $u$ each representing a state of one of the tree caches according to $f$. Using this concept, we define next the equivalence between two states $u, v$ in $\gamma^{n_c} - I$.

**Definition 3.** States $u, v \in \gamma^{n_c} - I$ are equivalent if and only if there exist $f \in \text{Aut}(G) : f.u = v$ .

### 6.1 Iterative state lumping

In this subsection, we describe our approach to reducing the state set using lumpability first by a solution to the problem of finding automorphisms then by iteratively lumping the state set. The problem of finding the automorphisms of any graph is NP complete and can be solved using McKay’s algorithm [48]. However, given the symmetric and recursive structure of the tree graph and based on Def. 2, we define the automorphisms in a caching tree graph using Theorem 2.

**Lemma 2.** A permutation of a tree graph is an automorphism if it is a composition of permutations between sibling sub-trees that are symmetric.

**Proof.** This lemma imposes three conditions on a permutation to be identified as an automorphism. We prove these conditions in the following: First, only siblings can be permuted such that it preserves the vertex-edge connectivity. Let $i, j$ represent the indices of two leaf nodes in a tree graph and $i_p, j_p$ represent the corresponding parent. As a result $(i, i_p)$ as well as $(j, j_p) \in E$. A permutation between $i$ and $j$ is an automorphism if and only if $(i, j_p)$ and $(j, i_p) \in E$. This is only true if $j_p = i_p$ thus $i$ and $j$ are siblings. The second condition is that the permutation of non-leaf nodes requires that of their entire sub-trees. Hence, let $i, j$ represent the indices of two non-leaf nodes in a tree graph and $i_c, j_c$ represent the indices of one of their corresponding children. As a result $(i, i_c)$ as well as $(j, j_c) \in E$. A permutation between $i$ and $j$ is an automorphism if and only if $(i, j_c)$ and $(j, i_c) \in E$ which is impossible to happen. Hence, the simultaneous permutation of the vertes and their corresponding children is indispensable to keep the same vertex-edge connectivity. The third condition is that the sibling sub-trees must be symmetric. We define two sub-trees to be symmetric if, for each vertex of a sub-tree, there exists a corresponding symmetric one in the other located in the same level and has the same number of children. This condition is a straightforward result to the second condition.

Note that the lemma above implies that a composition between two permutations that fulfill the three conditions is also an automorphism. This is due to the fact that the set of all automorphisms forms a group $\text{Aut}(G)$ under the function composition. Graphically, this can be seen from the recursive structure of the tree where one of the permutable sub-trees can contain permutable sub-trees.

Recall that in our MAP approach in Sect. 4, we build the MAP of the caching tree iteratively by applying the level superposition operation on MAPs modelling the sibling cache sub-trees in each level starting from the leaves followed by the line superposition operation between the parent caches and their superposed
Theorem 1. The number of lumpable partitions within the MAP representing the level superposition of $m$-trees corresponds to the number of all possible values of $\nu$.

As a result of Corollary 1, the number of the states of $M_{\text{lvl}}$ resulting from the level superposition of $n$ permutable subtrees is $m_S^n$ where $m_S$ is the number of the states of the MAP modelling any of the subtrees. Let the state of a subtree be defined as $S = (S_1, S_2, \ldots, S_n) \in S^n$, i.e. it represents a state in $M_{\text{lvl}}$ such that $S_j \in S \forall j \in [n]$ where $S$ denotes the set of states of the MAP of one subtree. In a lumpable partition $\rho$, we denote the frequency of the presence of a state $s^{(i)} \in S$ as an element in a state $S$ by $\nu_i$ where $i \in [m_S]$. For example, for three binary M/M/M sub-trees each of one parent and two child caches we have for $S = (001, 10F, 001)$ and $s^{(i)} = (001)$ the frequency $\nu_i = 2$. We represent $\nu_i$ by

$$\nu_i = \sum_{j \in [n]} 1_{S_j = s^{(i)}} ,$$

where $1_{(\cdot)}$ is the indicator function. According to Lem. 2, the states in each lumpable partition are considered permutations with respect to their elements $S_j$. This is exactly the result of the action of the automorphisms of $G$ that include only the permutations of the intended subtrees on the state set $S^n$. As a result, the frequency $\nu_i$ of all the states in one partition is the same. Hence, each lumpable partition has a unique frequency vector $\nu$ of length $m_S$ which defines the different lumpable partitions in $M_{\text{lvl}}$. Since the length of $S$ with respect to its elements $S_i$ is $n$, we have

$$\sum_{b=1}^{m_S} \nu_b = n .$$

Theorem 1. The number of lumpable partitions within the MAP representing the level superposition of $n$ symmetric subtrees with refined individual MAPs is

$$N_p = \left( \frac{n + m_S - 1}{m_S - 1} \right) \leq m_S^n \quad m_S \geq 3, n \geq 1 .$$

where $m_S$ is the number of the states of the MAP of one sub-tree. We denote a MAP as refined if there exists no equivalence between its states. Note that this is the case after lumping. The number of the lumpable partitions corresponds to the number of all possible values of $\nu$. Therefore, the number of lumpable partitions is the number of $m_S$-tuples of non-negative integers whose sum is $n$. According to the “stars and bars” theorem in [49], the number of tuples is given by $\binom{n + m_S - 1}{m_S - 1}$. The proof of the relation in Theorem 1 is given in the appendix 9.1.
The reduced state set size due to lumpability grows significantly slower (polynomially) for an increasing number of sub-trees compared to the original MAP that grows exponentially in $n$. Lumping the states of inner caches (permutation between leaves) shows an additional improvement compared to only lumping with respect to the permutations between the sub-trees.

Corollary 2. The number of partitions $N_p$ is bounded by a polynomial function of $n$

$$N_p \sim O(n^{ms})$$

The proof of Cor. 2 is in the appendix in Sect. 9.2. Essentially, Cor. 2 states that the growth of the number of states with the number of symmetric sub-trees in the cache hierarchy is broken down from originally an exponential growth (see the right hand side of Theorem 1) to a polynomial one under the lumpability approach.

We show in Fig. 8 the significant effect of the lumpability on the number of the states of the MAP representing $n \in \{1, \ldots, 10\}$ 2-lvl M/M/M symmetric binary sub-trees. We compare the size of the state set for three cases: the original MAP, the MAP after applying the lumpability approach with respect to the sub-tree permutations only (Lump) and the MAP applying lumpability approach with respect to all the possible automorphisms (Lump+). Here we use 2-lvl binary sub-trees as an example, but the qualitative behavior of Fig. 8 remains unchanged when having more levels or different number of children per node. As described above, the figure shows that applying the lumpability approach results in a remarkable decrease in the growth of the number of states with the number of symmetric sub-trees, i.e., from an originally exponential growth to a polynomial one. In addition, lumping all the possible states taking into account not only the sub-trees permutations but also the inner nodes permutations leads to an additional reduction in the state set size (Lump+).

### 6.3 MAP Lumpability

In this subsection, we prove that the MAP within each level superposition operation is lumpable with respect to the lumpable partitions $\rho = \{\rho_1, \rho_2, \ldots, \rho_N\}$ formed according to the equivalence relation between the states based on Def. 3.

**Definition 4.** We define $Q = D_0 + D_1$ as the total transition matrix of the MAP resulting from the level superposition of $n$ symmetric sub-trees. Elements of $Q$, i.e., $Q_{A,B}$ denote the transition rate from state $A$ to state $B$. In addition, we define $q$ as the total transition matrix of each of the $n$ symmetric sub-trees. Elements of $q$, i.e., $q_{a,b}$ denote the transition rate from state $a$ to state $b$.

**Lemma 3.** There exists no transition from a state $A$ to a state $B$ in the MAP $M_{1\text{lvl}}$ resulting from the level superposition of the MAPs $M_j$ of $n$ symmetric trees if $A_j \neq B_j$ for more than one element $j \in [n]$.

$$Q_{A,B} = 0 \text{ if } \sum_{j \in [n]} 1_{A_j \neq B_j} > 1, \ A, B \in S^n$$
Proof. We note that only one event (active or hidden transition) takes place at a time. The level superposition is applied on MAPs of independent trees, i.e. a transition between different states in one MAP is independent of any other transitions in other MAPs. Therefore, having two states A and B that have a difference of at least two pairs of the corresponding superposed states A_2 and B_2 implies the occurrence of at least two independent events. For these events no single transition exists.

Given a MAP $M_{bl}$ resulting from the level superposition of $n$ independent symmetric sub-trees in a graph $G_{bl}$, we consider states $A, B$ with non-zero transition rates $Q_{A,B}$ as defined by Lem. 3. Now we can represent the transition rate $Q_{A,B}$ as the sum of the corresponding sub-tree transition rates as

$$Q_{A,B} = \sum_{j=1}^{n} q_{A_j,B_j} |_{A_j \neq B_j}, \quad A \neq B. \quad (15)$$

Note that for $Q_{A,B} \neq 0$ there is only one value of $j$ for which $A_j \neq B_j$.

Now, we show that under the equivalence relation from Def. 3 for an automorphism $f \in \text{Aut}(G_{bl})$, i.e. a permutation of the $n$ symmetric sub-trees, the total transition rates between states in different lumpable partitions remain unchanged.

**Lemma 4.**

$$Q_{A^*,B^*} = Q_{A,B} :$$

$$\forall f \in \text{Aut}(G_{bl}).$$

The proof of Lem. 4 is given in the appendix in Sect. 9.3. In the following, based on the equivalence relation from Def. 3 we obtain lumpable partitions of the MAP of the level superposition.

**Theorem 2.** The MAP $M_{bl}$ resulting from the level superposition of $n$ independent symmetric sub-trees is lumpable with respect to the partitions $\rho = \{\rho_1, \rho_2, ..., \rho_{N_p}\}$ formed based on the equivalence relation between the states according to Def. 3.

Proof. A necessary and sufficient condition for a MAP to be lumpable with respect to $\rho$ is that for every pair of partition sets $\rho_i$ and $\rho_j$, $Q_{A,\rho_i} := \sum_{B \in \rho_j} Q_{A,B}$ remains unchanged $\forall A \in \rho_i$ [50]. From Lem. 4 we know that any pair of states $A, A^*$ from one partition $\rho_i$ has the same transition rate to a state $B$ in another partition $\rho_j$ and its permutation $B^*$ in the same partition respectively. This implies that $Q_{A,\rho_i} = Q_{A^*,\rho_i} \forall A, A^* \in \rho_i$ and $j \in [N_p] \setminus i$. The only remaining task is to prove that $Q_{A,\rho_i} = Q_{A^*,\rho_i} \forall A, A^* \in \rho_i$, i.e., the sum of the transition rates from one state to its equivalent ones remains constant for all the states in the same partition. As every two states $A, A^*$ within the same partition are permutations, the corresponding sub-tree states $A_j, A^*_j$ are not equal for at least two values of $j \in [n]$. Therefore, by Lem. 3 there exists no transition between $A$ and $A^* \forall A, A^* \in \rho_i : A \neq A^*$, i.e. there exist no transitions between states from the same partition. Therefore, the condition in [50] holds for partitions defined under the equivalence relation Def. 3.

Note that the transition matrix of the lumped MAP is an $N_p \times N_p$ matrix with elements representing the transition rate from one partition to another, i.e., an element $Q_{\rho_i,\rho_j} := \sum_{B \in \rho_j} Q_{A,B}$ where $A$ is any of the states in $\rho_i$ since they all have the same value of the sum.

### 7 Evaluations

In this section, we show analytical, as well as, simulation-based evaluation results for TTL cache hierarchies under object fetch delays. We first show the impact of non-zero fetch delay on the object hit probability using the M/M/M caching system before validating the MAP approach from Sect. 4 using simulation results. We then evaluate the accuracy of the approximations from Sect. 5 compared to the MAP approach from Sect. 4.
Delay to inter-request time ratio $\bar{\tau}_\Delta$ Object hit probability $P_h$

Figure 9: Single M/M/M Cache: Object hit probability $P_h$ for increasing ratio $\bar{\tau}_\Delta$ of the expected delay to the expected inter-request time. Note that the MAP approach from Sect. 4 exactly matches the simulation. The analytical approximation for a single cache is accurate.

TTL to inter-request time ratio $\bar{\tau}_T$ Delay impairment $\eta$

Figure 10: Single M/M/M cache: The delay impairment $\eta \in [0, 1]$ for different TTL to inter-request time ratios $\bar{\tau}_T$. Note that compensating the impact of the delay on the hit probability using increased object TTL has diminishing returns.

7.1 Impact of network delays on the object hit probability

If not stated otherwise, we use in the following full binary tree caching hierarchies of $L$ levels with $L \in \{1, 2, 3\}$, i.e. the hierarchies possess $2^L - 1$ caches. Note that the provided analytical methods hold for any tree caching hierarchy. For the illustration of the following results we repeat the definitions from Sect.5.1 of the ratio of the expected delay $E[\Delta]$ to the expected inter-request time $E[X]$, i.e., $\bar{\tau}_\Delta := E[\Delta]/E[X]$, as well as, the the ratio of the expected TTL $E[T]$ to $E[X]$ defined as $\bar{\tau}_T := E[T]/E[X]$.

Fig. 9 shows a comparison of the object hit probability $P_h$ at an M/M/M single cache from simulations, the MAP as well as the approximations (8-11). The object hit probability declines with increasing delay for a given expected inter-request time. The ratio of the TTL to the inter-request time is fixed to $\bar{\tau}_T = 2$. The figure shows that our MAP approach, as well as, the analytical approximation coincide with the simulation. Moreover, an increasing fetch delay (even of the order of the expected inter-request time $E[X]$) is shown to significantly decrease the hit probability.
Delay to inter-request time ratio $\bar{\tau}_\Delta$

Figure 11: Two level M/M/M binary caching tree: The object hit probability $P_h$ of the MAP approach and the simulation coincide. State-of-the-art approximations deviate significantly under object fetch delays.

$\bar{\tau}_\Delta$

Object hit probability $P_h$

0 2 4 6 8 10

Delay to inter-request time ratio $\bar{\tau}_\Delta$

Figure 12: Binary M/M/E\_2 caching trees with $2^L-1$ caches: Increasing the depth $L$ of the caching tree under the same TTL budget compensates for large delays. For zero or small delays the TTL overlap is, however, detrimental.

In Lem. 1 we showed that the TTL can counteract the delay impairment, however, at a diminishing impact. Fig. 10 illustrates this for a single M/M/M cache for given expected delays. Note that for a given expected TTL doubling the expected delay leads to an over-proportional increase in delay impairment $\eta$.

Fig. 11 depicts the decrease in object hit probability with increasing object fetch delay for a two level binary tree cache hierarchy under the M/M/M setting. The figure shows results obtained by simulation that match our MAP approach in comparison to the renewal approximation. We set the expected TTL as $\bar{\tau}_T=2$ for the first level containing the leaf caches and $\bar{\tau}_T=4$ for the root cache. In contrast to Fig. 9 this result shows that the approximation deteriorates quickly for hierarchies.

Fig. 12 illustrates the gain of adding one level of leaf caches to a hierarchy in terms of the object hit probability. We compare an $L=2$-level caching binary tree with an $L=3$-level binary tree. We keep the aggregate input request process to the system fixed for comparison. Obviously, increasing the TTL budget proportionally to the additional level of caches results in a hit probability curve ($L=3$-proportional in Fig. 12) that dominates the $L=2$ curve. More interestingly, is how the behavior shifts when we keep the overall system TTL budget fixed and distribute it evenly. As delays are per link random variables an additional level of caches stochastically increases the object fetch delay. In Fig. 12 we observe that an extra level of leaf caches compensates for relatively large object fetch delays (albeit the fixed system TTL budget). For zero or small delays under fixed system TTL budget the added layer of caches is detrimental as the (per cache) smaller TTLs overlap between children and parent caches.

Fig. 13a shows the object hit probability $P_h$ using $\bar{\tau}_T=2$ for increasing delay for an E\_20/M/M cache in comparison to an M/M/M cache. Here, we sample the input inter-request times from an Erlang E\_k

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prepare the trace data to ensure its consistency. We remove statistical outliers based on the density function \( \hat{\text{MAP}} \) as in Fig. 6. Hence, in the first step we fit the inter-request times in the trace to a corresponding on our MAP approach.

Next, we use trace data from a production system [51] as input to a caching scenario with a single cache. In addition, that is simulated to show the impact of different average delays on the object hit probabilities. In addition, objects requested with a delay, which is more significant for small TTLs.

Interestingly, the figure also shows the ratio \( \kappa \) of the hit probability for zero delay to \( \kappa \) at the optimum delay is depicted as \( \kappa \) showing that for small expected TTL the hit probability is significantly increased in presence of delays. It can be shown that this is due to the nearly periodic behavior of the request stream.

Distribution with a fixed mean such that for larger \( k \) the request process becomes periodic.\(^2\) Interestingly, the function shows that for request streams approaching periodic there is a non-trivial optimum of the object hit probability at an expected delay denoted \( \tau_{\Delta}^* \). To give an intuition for this behavior, consider deterministic inter-arrival time \( x \), delay \( \delta \) and TTL \( t \). In case of zero delay and if \( x > t \) each request results in a miss thus zero hit probability. Having a delay that shifts the TTL start such that \( \delta < x < \delta + t \) results in a positive hit probability. Fig. 16 illustrates this in the appendix.

For the case of periodic arrivals we prove in the appendix (Sect. 9.4) that there exists an upper bound \( \tau_{\Delta}^* \) on the expected delay to inter-request ratio \( \tau_{\Delta}^* \) as a function of the expected delay \( \tau_{\Delta}^* \) to inter-request ratio \( \tau_{\Delta}^* \) below which the object hit probability is higher than the zero delay case (For example see \( \tau_{\Delta}^* \) in Fig. 13a).

Accordingly, Fig. 13b shows for varying expected TTL \( \tau_{\Delta}^* \) the corresponding expected delay \( \tau_{\Delta}^* \), which maximizes the hit probability \( P_h \). The figure also shows the ratio \( \kappa \) of the hit probability for zero delay to the maximum hit probability at \( \Delta = \delta^* \), i.e., \( \kappa \) denotes the number of standard deviations a sample deviates from the mean of the trace data. Here \( \mu \) and \( \sigma \) are the mean and the standard deviation of the trace data, respectively. In this work we use a cutoff value of 2 and a power transform to map our trace data such that we can calculate the z-score.

\(^2\)A special case of \( \Gamma(\alpha, \alpha\beta) \) distributed inter-request times with \( \alpha \to \infty \).

## 7.2 Trace-based simulation results

Next, we use trace data from a production system [51] as input to a caching scenario with a single cache that is simulated to show the impact of different average delays on the object hit probabilities. In addition, we compare the simulation results to analytical results obtained from modelling the caching system based on our MAP approach.

Given the MAP model of the input to a single cache, in addition to the TTL and delay, we form a cache MAP as in Fig. 6. Hence, in the first step we fit the inter-request times in the trace to a corresponding density function \( f_X(t) \) that is represented by a MAP. To optimize the estimation of the density, we first prepare the trace data to ensure its consistency. We remove statistical outliers based on the z-score of the samples [52], where the z-score \( z = \frac{x - \mu}{\sigma} \) denotes the number of standard deviations a sample deviates from the mean of the trace data. Here \( \mu \) and \( \sigma \) are the mean and the standard deviation of the trace data, respectively. In this work we use a cutoff value of 2 and a power transform to map our trace data such that we can calculate the z-score.
Figure 14: Trace data probability density function estimation: The estimated PDF using PH8 distribution after removing the outliers is very close to the histogram of the trace data.

We carry out a parametric estimation of the density that best represents the trace. Here, we represent the parameters of the density by $\theta$. We formulate the parameter estimation problem as a maximum likelihood optimization problem of the form

$$\hat{\theta} = \arg \max_{\theta} f_{\Theta}(\theta | T) ,$$

where $\hat{\theta}$ represents the estimate of the density parameters, $T$ represents the trace data and $f_{\Theta}$ is the conditional density of the parameters given the trace. We apply the expectation maximization (EM) algorithm to solve this optimization problem [53]. We use a PH Coxian distribution PH$_k$ for the PDF estimation of the trace data. The Coxian distribution is a generalization of the Erlang distribution where the transition to the absorption state is not limited to the last state $k$, however, it can be reached from any other state [54]. The larger the number of states used, the more degrees of freedom are available, thus we achieve a better estimation. On the other hand, the increase in the states comes at the expense of the computational complexity and overfitting. Several approaches exist to determine the minimum number of phases required for fitting the data [55]. One approach is to use distant metrics such as AIC (Akaike information criterion) [56] and BIC (Bayesian information criterion) [57] to quantify the distance between the estimation and the data. Based on these metrics, the minimum number of phases is determined by a tolerance value. Fig. 14 shows the result of the density estimation of the trace data where PH$_8$ is used. Although, the histogram of the trace is shown to be non-monotonic, using PH$_8$ allows for capturing such a behavior. Here we find 8 phases enough to capture the statistical characteristics of the data.

Fig. 15 shows the result of our MAP approach using a PH$_8$/M/M model in comparison to the trace simulation. Observe that the MAP approach provides a very close result to the trace simulation. As expected, the object hit probability declines with increasing delay. The figure shows that if the average delay is in the order of the inter-request times the loss in object hit probability compared to the classical and idealized ”no-delay” model is substantial.

8 Conclusions

In this paper, we provided an exact model for TTL caches under non-zero object fetch delays. We considered tree-based cache hierarchies with random fetch delays, as well as, a wide class of object request processes. Our analysis provides the object hit probability under delays and allows understanding the impact of delays and TTLs on cache performance. We provided a rigorous computational speedup method for calculating exact cache performance metrics based on MAP lumpability. We also show shortcomings of state-of-the-art approximations of the hit probability given object fetch delays. We provided numerical and trace-based evaluation results validating the accuracy of our model and quantifying the delay impairment, as well as, the benefit of adding caches to a hierarchy under delay constraints. We also discuss the diminishing return of using TTLs as means to compensate object fetch delays.
Figure 15: Trace-driven simulation of a single cache system with delay: The MAP model accurately provides the object hit probability $P_h$ under varying expected delays.

9 Appendix

9.1 Proof of Theorem 1

Here, we prove the proposition in Theorem 1 that is $m_S^n \geq N_p$ for which we use the shorthand notation $P(m_S, n)$. The proof goes by induction which involves three steps.

Proof. First, we show that the proposition $P(3, 1)$ holds: \( \binom{3}{2} = 3 \). Then we show that $P(m_S, 1)$ implies $P(m_S + 1, 1)$.

\[
P(m_S + 1, 1) : m_S + 1 \geq \binom{m_S + 1}{m_S}
\]

\[
m_S + 1 = m_S + 1
\]

The last step is to show that $P(m_S, n)$ implies $P(m_S, n + 1)$

\[
P(m_S, n + 1) : m_S^{n+1} \geq \binom{m_S + n}{m_S - 1}
\]

\[
m_S^{n+1} \geq \frac{(m_S + n)!}{(m_S - 1)!(n + 1)!}
\]

\[
m_S^{n+1} \geq \frac{(m_S + n)(m_S + n - 1)!}{(m_S - 1)!(n + 1)n!}
\]

Given $P(m_S, n) : m_S^n \geq \frac{(m_S + n - 1)!}{(m_S - 1)!n!}$, $P(m_S, n + 1)$ exists if $m_S \geq \frac{m_S + n}{n + 1}$, i.e.,

\[
(n + 1)m_S \geq m_S + n
\]

\[
m_S \geq 1
\]

9.2 Proof of Cor. 2

Proof. Next, we prove that the number of lumpable partitions grows polynomially with the number of symmetric sub-trees $n$ for a given number of states $m_S$ of any of the sub-trees. From Theorem 1 we know
that

\[
N_p = \binom{n + mS - 1}{mS - 1} = \frac{(n + mS - 1)!}{(mS - 1)! n!} = \frac{(n + mS - 1)(n + mS - 2)\ldots(n + 1)n!}{(mS - 1)! n!} = \prod_{k=0}^{mS - 2} \frac{(n + mS - 1 - k)}{(mS - 1)!}.
\]

Since \((n + mS - 1) \geq (n + mS - 1 - k) \forall k \in \mathbb{N},

\[
N_p = \prod_{k=0}^{mS - 2} \frac{(n + mS - 1 - k)}{(mS - 1)!} \leq \frac{(n + mS - 1)^{mS - 1}}{(mS - 1)!}.
\]

\[\square\]

### 9.3 Proof of Lem. 4

Proof. Using (15) we can write

\[
Q_{A,B} = \sum_{j=1}^{n} q_{A_j,B_j} \Big|_{A_j \neq B_j},
\]

\[
Q_{A^*,B^*} = \sum_{j=1}^{n} q_{A^*_j,B^*_j} \Big|_{A^*_j \neq B^*_j}.
\]

Together with (14) we have

\[
Q_{A^*,B^*} = \sum_{j=1}^{n} q_{A_{f^{-1}(j)},B_{f^{-1}(j)}} \Big|_{A_{f^{-1}(j)} \neq B_{f^{-1}(j)}}.
\]

Given that \(f\) is any permutation of the \(n\) sub-trees, \(A^*\) is a permutation of the elements \(A_j\) of \(A\) according to \(f\). Therefore, \(\sum_{j=1}^{n} \Upsilon(A_j, B_j) = \sum_{j=1}^{n} \Upsilon(A_{f^{-1}(j)}, B_{f^{-1}(j)})\) where \(\Upsilon\) represents any non-random test function. Using that in (16) we obtain

\[
Q_{A^*,B^*} = \sum_{j=1}^{n} q_{A_j,B_j} \Big|_{A_j \neq B_j} = Q_{A,B}.
\]

\[\square\]

### 9.4 Derivation of improved hit probability under delays

In this part, we derive a bound on the network delay that improves the hit probability for a periodic request process with inter-request times \(x\) and exponentially distributed TTL and exponentially distributed delay with parameters \(\lambda_T, \lambda_\Delta\), respectively. In this case, the hit probability improves if for \(x > T = t\) the delay shifts the TTL such that \(\delta < x < \delta + t\). The hit probability then improves as

\[
P(\Delta < x < \Delta + T) \geq P(x < T),
\]

with \(P(\Delta < x < \Delta + T) = F_\Delta(x) - F_{\Delta + T}(x), P(T > x) = 1 - F_T(x),\) and finally \(F_{\Delta + T}(x) = \int_0^x f_\Delta(t) * f_T(t) \, dt\).

Now we can compute for the model at hand

\[
P(\Delta < x < \Delta + T) = \frac{\lambda_\Delta}{\lambda_\Delta - \lambda_T} (e^{-x\lambda_T} - e^{-x\lambda_\Delta})
\]

and \(P(x < T) = e^{-x\lambda_T}\). Substituting in (17) we obtain

\[
\frac{\lambda_\Delta}{\lambda_\Delta - \lambda_T} e^{-x\lambda_\Delta} \leq \frac{\lambda_T}{\lambda_\Delta - \lambda_T} e^{-x\lambda_T}
\]

(18)
Based on $\lambda_\Delta - \lambda_T$, we derive a bound on $\lambda_\Delta$ in two cases:

**Case 1**: $\bar{\tau}_\Delta < \bar{\tau}_T$, i.e., $\lambda_\Delta > \lambda_T$ we have

$$-\frac{1}{\bar{\tau}_\Delta} e^{-1/\bar{\tau}_\Delta} \geq -\frac{1}{\bar{\tau}_T} e^{-1/\bar{\tau}_T}$$

(19)

In order to derive the delay interval that satisfies the inequality, we first solve the equation $-\frac{1}{\bar{\tau}_\Delta} e^{-1/\bar{\tau}_\Delta} = -\frac{1}{\bar{\tau}_T} e^{-1/\bar{\tau}_T}$. Let $u = -\frac{1}{\bar{\tau}_\Delta}$ and $h = -\frac{1}{\bar{\tau}_T} e^{-1/\bar{\tau}_T}$. For the transcendental equation $ue^u = h$ we know that

$$u = \begin{cases} \bar{W}_1(h), W_0(h) & -1/e \leq h < 0 \\ W_0(h) & h \geq 0 \end{cases}$$

(20)

where $\bar{W}_a(.)$ is the a-th branch of the Lambert-$W$ function. Note that the possible solutions of (20) depend on the value of $h$. We know that $h = -\frac{1}{\bar{\tau}_T} e^{-1/\bar{\tau}_T}$ is a convex function over $\bar{\tau}_T \in [0, \infty]$ where $-1/e \leq h < 0$. Therefore, the solution to the (20) is $u = \bar{W}_-1(h), W_0(h)$.

Given that $ue^u$ is decreasing on $u \leq -1$ and $\bar{W}_-1(h) < -1$ the inequality (19) holds for

$$u \leq W_1(h).$$

(21)

Recall that $\bar{\tau}_\Delta < \bar{\tau}_T$, i.e., $u < -1/\bar{\tau}_T$. For the interval of $-1 < u < -1/\bar{\tau}_T$, $ue^u$ is an increasing function such that $-1/e < ue^u < h$. As a result, (19) does not hold for $-1 < u < -1/\bar{\tau}_T$. Now, from (21) we finally obtain,

$$\bar{\tau}_\Delta \leq -1/W_1(-1/\bar{\tau}_T) \text{ if } \bar{\tau}_\Delta \leq \bar{\tau}_T$$

**Case 2**: $\bar{\tau}_\Delta \geq \bar{\tau}_T$, i.e., $\lambda_\Delta \leq \lambda_T$

From (18) we have

$$-\frac{1}{\bar{\tau}_\Delta} e^{-1/\bar{\tau}_\Delta} \leq -\frac{1}{\bar{\tau}_T} e^{-1/\bar{\tau}_T}$$

Analogous to the first case the solution to the inequality is

$$W_1(h) \leq u < -1, \ -1 \leq u \leq W_0(h)$$

$$W_1(h) \leq u \leq W_0(h)$$

Note that the following solution is only valid if $\bar{\tau}_\Delta \geq \bar{\tau}_T$.

$$-1/W_1(-1/\bar{\tau}_T) \leq \bar{\tau}_\Delta \leq -1/W_0(-1/\bar{\tau}_T)$$

(22)

Since

$$W_0(-1/\bar{\tau}_T) \begin{cases} = -1/\bar{\tau}_T, \text{ for } \bar{\tau}_T \geq 1 \\ > -1/\bar{\tau}_T, \text{ otherwise } \end{cases}$$

using that in (21) and (22), we represent bounds for the expected delay for both cases depending on $\bar{\tau}_\Delta$ as $\bar{\tau}_\Delta \leq \bar{\tau}_\Delta^+$.

$$\bar{\tau}_\Delta^+ = \begin{cases} -1/W_1(-1/\bar{\tau}_T), \text{ for } \bar{\tau}_T \geq 1 \\ -1/W_0(-1/\bar{\tau}_T), \text{ otherwise } \end{cases}$$

Now, for the considered caching system when the expected network delays lie below these bounds this results in an object hit probability that is larger or equal to the object hit probability at zero delay. We conclude that there exist at least one delay value $\bar{\tau}_\Delta$ that maximizes the hit probability. For example, recall that in Fig. 13a we use a nearly periodic $E_{20}$ input and $\bar{\tau}_T = 2$. The figure shows that the hit probability for $\bar{\tau}_\Delta \leq -1/W_1(-1/\bar{\tau}_T) = \bar{\tau}_\Delta^+$ is larger or equal to the hit probability under zero delay. Moreover, we can show from the equation that as $\bar{\tau}_T \to \infty, \bar{\tau}_\Delta^+ \to 0$, thus $\bar{\tau}_\Delta \to 0$ (see Fig. 13b). An additional remark is that for small values of $\bar{\tau}_T$ ($\bar{\tau}_T < 1$), the bound on the delay that improves the hit probability exceeds the TTL $\bar{\tau}_\Delta^+ > \bar{\tau}_T$.  

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9.5 Illustration: Intuition behind the positive impact of the delay on the hit probability for periodic requests

Figure 16: Assuming constant TTL and delay. (a) Zero delay case: Zero hit probability. (b) Non-zero delay: Positive hit probability.

References

[1] K. Andreev, B. M. Maggs, A. Meyerson, and R. K. Sitaraman, “Designing overlay multicast networks for streaming,” in Proc. of ACM Symposium on Parallelism in Algorithms and Architectures SPAA, 2003, pp. 149–158.

[2] W. Jiang, S. Ioannidis, L. Massoulié, and F. Picconi, “Orchestrating massively distributed CDNs,” in Proc. of the Conference on Emerging Networking Experiments and Technologies, CoNEXT, 2012, p. 133–144.

[3] D. Bhat, A. Rizk, M. Zink, and R. Steinmetz, “SABR: Network-Assisted Content Distribution for QoE-Driven ABR Video Streaming,” ACM Trans. Multimedia Comput. Commun. Appl., vol. 14, no. 2s, apr 2018.

[4] G. Zhang, Y. Li, and T. Lin, “Caching in information centric networking: A survey,” Computer Networks, vol. 57, no. 16, pp. 1389–1286, 2013.

[5] N. Choungmo Fofack and S. Alouf, “Modeling modern DNS caches,” in Performance Evaluation Methodologies and Tools, 2013, pp. 184–193.

[6] N. Choungmo Fofack, P. Nain, G. Neglia, and D. Towsley, “Performance evaluation of hierarchical ttl-based cache networks,” Computer Networks, vol. 65, pp. 212 – 231, 2014.

[7] D. S. Berger, P. Gland, S. Singla, and F. Ciucu, “Exact analysis of TTL cache networks,” Performance Evaluation, vol. 79, pp. 2 – 23, 2014.

[8] V. Martina, M. Garetto, and E. Leonardi, “A unified approach to the performance analysis of caching systems,” in Proc. of IEEE Conference on Computer Communications, INFOCOM, April 2014, pp. 2040–2048.

[9] C. Fricker, P. Robert, and J. Roberts, “A versatile and accurate approximation for lru cache performance,” in Proc. of the Teletraffic Congress (ITC), 2012, pp. 1–8.

[10] M. Dehghan, B. Jiang, A. Dabirmoghaddam, and D. Towsley, “On the analysis of caches with pending interest tables,” in Proc. of ACM Conference on Information-Centric Networking, 2015, p. 69–78.

[11] H. Che, Y. Tung, and Z. Wang, “Hierarchical web caching systems: modeling, design and experimental results,” IEEE JSAC, vol. 20, no. 7, pp. 1305–1314, Sep 2002.

[12] K. Schomp, O. Bhardwaj, E. Kurtoglu, M. Muhaimen, and R. K. Sitaraman, “Akamai DNS: Providing Authoritative Answers to the World’s Queries,” in Proc. of ACM SIGCOMM, 2020, p. 465–478.

[13] E. J. Rosensweig, D. S. Menasche, and J. Kurose, “On the steady-state of cache networks,” in Proc. of IEEE Conference on Computer Communications, INFOCOM, 2013, pp. 863–871.
[14] A. Rizk, M. Zink, and R. Sitaraman, “Model-based design and analysis of cache hierarchies,” in *IFIP Networking Conference (IFIP Networking) and Workshops*, 2017, pp. 1–9.

[15] N. Atre, J. Sherry, W. Wang, and D. S. Berger, “Caching with delayed hits,” in *Proc. of ACM SIGCOMM*, 2020, pp. 495–513.

[16] S. Li, D. Reddy, and B. L. Jacob, “A performance & power comparison of modern high-speed DRAM architectures,” in *Proc. of the International Symposium on Memory Systems, MEMSYS*, 2018, pp. 341–353.

[17] A. Ferragut, I. Rodriguez, and F. Paganini, “Optimal timer-based caching policies for general arrival processes,” *Queueing Syst. Theory Appl.*, vol. 88, no. 3-4, pp. 207–241, 2018.

[18] B. Jiang, P. Nain, and D. Towsley, “On the convergence of the TTL approximation for an LRU cache under independent stationary request processes,” *ACM Trans. Model. Perform. Evaluation Comput. Syst.*, vol. 3, no. 4, pp. 20:1–20:31, 2018.

[19] E. Gelenbe, “A unified approach to the evaluation of a class of replacement algorithms,” *IEEE Trans. Computers*, vol. 22, no. 6, pp. 611–618, 1973.

[20] Hao Che, Ye Tung, and Zhijun Wang, “Hierarchical web caching systems: modeling, design and experimental results,” *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 7, pp. 1305–1314, 2002.

[21] S. Müller, O. Atan, M. van der Schaar, and A. Klein, “Context-aware proactive content caching with service differentiation in wireless networks,” *IEEE Trans. Wirel. Commun.*, vol. 16, no. 2, pp. 1024–1036, 2017.

[22] S. Maghsoudi and M. van der Schaar, “A non-stationary bandit-learning approach to energy-efficient femto-caching with rateless-coded transmission,” *IEEE Trans. Wirel. Commun.*, vol. 19, no. 7, pp. 5040–5056, 2020.

[23] M. Ji, G. Caire, and A. F. Molisch, “Fundamental Limits of Caching in Wireless D2D Networks,” *IEEE Transactions on Information Theory*, vol. 62, no. 2, pp. 849–869, 2016.

[24] N. Melazzi, G. Bianchi, A. Caponi, and A. Detti, “A general, tractable and accurate model for a cascade of LRU caches,” *IEEE Communications Letters*, vol. 18, no. 5, pp. 877–880, May 2014.

[25] S. Asmussen, *Applied Probability and Queues*, ser. Stochastic Modelling and Applied Probability. Springer New York, 2008.

[26] H. Dai, B. Liu, H. Yuan, P. Crowley, and J. Lu, “Analysis of tandem pit and cs with non-zero download delay,” in *IEEE Conference on Computer Communications, INFOCOM*, 2017, pp. 1–9.

[27] M. Ahmadi, J. Roberts, E. Leonardi, and A. Movaghar, “On the effectiveness of the pit in reducing upstream demand in an ndn router,” *Performance Evaluation*, vol. 138, p. 102081, 2020.

[28] G. Neglia, D. Carra, M. Feng, V. Janardhan, P. Michiardi, and D. Tsigkari, “Access-time-aware cache algorithms,” *ACM Trans. Model. Perform. Eval. Comput. Syst.*, vol. 2, no. 4, nov 2017.

[29] M. Dehghan, B. Jiang, A. Seetharam, T. He, T. Salonidis, J. Kurose, D. Towsley, and R. K. Sitaraman, “On the complexity of optimal request routing and content caching in heterogeneous cache networks,” *IEEE/ACM Trans. Netw.*, vol. 25, no. 3, pp. 1635–1648, 2017.

[30] M. Dehghan, L. Massoulíé, D. Towsley, D. S. Menasché, and Y. C. Tay, “A utility optimization approach to network cache design,” *IEEE/ACM Trans. Netw.*, vol. 27, no. 3, pp. 1013–1027, 2019.

[31] A. Ferragut, I. Rodriguez, and F. Paganini, “Optimizing TTL caches under heavy-tailed demands,” in *Proc. of ACM SIGMETRICS*, 2016, pp. 101–112.
[32] G. Neglia, D. Carra, and P. Michiardi, “Cache policies for linear utility maximization,” *IEEE/ACM Trans. Netw.*, vol. 26, no. 1, pp. 302–313, 2018.

[33] L. Wang, G. Tyson, J. Kangasharju, and J. Crowcroft, “Faircache: Introducing fairness to ICN caching,” in *Proc. of IEEE International Conference on Network Protocols, ICNP*, 2016, pp. 1–10.

[34] W. Chu, M. Dehghan, D. Towsley, and Z. Zhang, “On allocating cache resources to content providers,” in *Proc. of the ACM Conference on Information-Centric Networking, ICN*, 2016, pp. 154–159.

[35] C. Li and A. L. Cox, “Gd-wheel: a cost-aware replacement policy for key-value stores,” in *Proc. of the European Conference on Computer Systems, EuroSys*, 2015, pp. 5:1–5:15.

[36] J. Du, C. Jiang, E. Gelenbe, H. Zhang, Y. Ren, and T. Q. S. Quek, “Double auction mechanism design for video caching in heterogeneous ultra-dense networks,” *IEEE Trans. Wirel. Commun.*, vol. 18, no. 3, pp. 1669–1683, 2019.

[37] N. Beckmann, P. B. Gibbons, B. Haeupler, and C. McGuffey, “Writeback-aware caching,” in *Symposium on Algorithmic Principles of Computer Systems, APOCS*. SIAM, 2020, pp. 1–15.

[38] Y. Cheng, F. Douglis, P. Shilane, G. Wallace, P. Desnoyers, and K. Li, “Erasing belady’s limitations: In search of flash cache offline optimality,” in *Proc. of USENIX Annual Technical Conference*, 2016, pp. 379–392.

[39] J. Wang, B. Berg, D. S. Berger, and S. Sen, “Maximizing page-level cache hit ratios in large web services,” *SIGMETRICS Perform. Evaluation Rev.*, vol. 46, no. 2, pp. 91–92, 2018.

[40] C. Koch, J. Pfannmüller, A. Rizk, D. Hausheer, and R. Steinmetz, “Category-Aware Hierarchical Caching for Video-on-Demand Content on Youtube,” in *Proceedings of the 9th ACM Multimedia Systems Conference*, 2018, p. 89–100.

[41] C. Koch, S. Werner, A. Rizk, and R. Steinmetz, “MIRA: Proactive Music Video Caching Using ConvNet-Based Classification and Multivariate Popularity Prediction,” in *IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS)*, 2018, pp. 109–115.

[42] A. Dabirmoghaddam, M. Dehghan, and J. J. Garcia-Luna-Aceves, “Characterizing interest aggregation in content-centric networks,” in *Proc. of IFIP Networking Conference*, 2016, pp. 449–457.

[43] D. Coppersmith and S. Winograd, “Matrix multiplication via arithmetic progressions,” *Journal of Symbolic Computation*, vol. 9, no. 3, pp. 251–280, 1990, computational algebraic complexity editorial.

[44] E. Cinlar, *Introduction to Stochastic Processes*. Dover Publications, 2013.

[45] W. R. KhudaBukhsh, A. Auddy, Y. Disser, and H. Koepl, “Approximate lumpability for markovian agent-based models using local symmetries,” *Journal of Applied Probability*, vol. 56, no. 3, p. 647–671, 2019.

[46] P. Simon, M. Taylor, and I. Kiss, “Exact epidemic models on graphs using graph-automorphism driven lumping,” *Journal of mathematical biology*, vol. 62, pp. 479–508, 04 2011.

[47] C. D. Godsil and G. F. Royle, *Algebraic graph theory*. Springer, 2010.

[48] B. D. McKay and A. Piperno, “Practical graph isomorphism, II,” *Journal of Symbolic Computation*, vol. 60, pp. 94–112, 2014.

[49] P. Ehrenfest and H. K. Onnes, “Simplified deduction of the formula from the theory of combinations which planck uses as the basis of his radiation theory,” *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science*, vol. 29, no. 170, pp. 297–301, 1915.

[50] J. G. Kemeny and J. L. Snell, *Finite Markov chains with a new app. ”Generalization of a fundamental matrix”*. Springer, 1983.
[51] SNIA IOTTA, “Microsoft production server traces,” 2011.

[52] D. Cousineau and S. Chartier, “Outliers detection and treatment: A review,” International Journal of Psychological Research, vol. 3, 06 2010.

[53] P. Buchholz, J. Kriege, and I. Felko, Input modeling with phase-type distributions and Markov models: theory and applications. Springer, 2014.

[54] M. Bladt, “A review on phase-type distributions and their use in risk theory,” Astin Bulletin, vol. 35, pp. 145–161, 05 2005.

[55] H. Okamura and T. Dohi, Fitting Phase-Type Distributions and Markovian Arrival Processes: Algorithms and Tools, 04 2016, pp. 49–75.

[56] H. Akaike, Information Theory and an Extension of the Maximum Likelihood Principle. New York, NY: Springer New York, 1998, pp. 199–213.

[57] G. Schwarz, “Estimating the dimension of a model,” The Annals of Statistics, vol. 6, no. 2, pp. 461–464, 1978.
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