A CNRZ-7 Based Wireline Transceiver With High-Bandwidth-Density, Low-Power for D2D Communication

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ABSTRACT A novel high-speed transceiver based on 7 bit correlated non-return-to-zero(CNRZ-7) with high-bandwidth-density(bandwidth per unit length) and low-power for Die-to-Die(D2D) communication is proposed. In order to further improve the SNR and the bandwidth of the CNRZ-5 in D2D communication, a CNRZ-7 based transmitter matrix and receiver matrix are proposed firstly, which are derived from Walsh Hadamard(W-H) transform and inverse transformation. In addition, to reduce the power consumption of the transmitter, the encoding driver based on CNRZ-7 transmitter matrix is designed with source series terminated drivers(SST). To further improve the SNR of the receiver, the decoding circuit based on CNRZ-7 receiver matrix is designed with a special multi-input comparators(MIC), which contain equalizer circuits. This transceiver is designed with a 28nm CMOS technology and the core area is $0.66\text{mm}^2$. The post-simulation results show that this transceiver can operate at 280 Gb/s, and the data rate is 35 Gb/s/wire. The worst width of the receiver’s eye-diagrams is 0.45UI when the transceiver operates at a 50 mm PCB channel with a 10dB@20GHz insertion loss, and the total BER is less than 1E-15. The power consumption is 1.1pJ/b under a normal corner.

INDEX TERMS Wireline transceiver, correlated non-return-to-zero (CNRZ), Walsh Hadamard, SST, MIC, D2D communication, pin efficiency.

I. INTRODUCTION

To drive the demand for higher bandwidth from high-performance computers and data centers, the data exchange rate of chips is growing rapidly. With the increasing functions of high performance chip, the area of monolithic SoC reaches the upper limit of lithography mask size, which makes the yield rate of SoC(system-on-chip) decrease sharply. With the increasing complexities of high performance chip, the design cycle of monolithic SoC increases exponentially. Large lithography masks with advanced technology are expensive, and the development cost of monolithic SoC increases sharply. Chiplet technology is the best solution to solve the current slow development of high performance chip [1]. The technology adopts an efficient DIE-to-DIE (D2D) communication technology in the package, which integrates multiple chips with different technologies and functions into the same package to achieve higher performance chips, as shown in Fig. 1. The key technology of chiplet is to develop D2D communication with high bandwidth density, low power consumption, and low BER [2]. To solve the problems of bandwidth, power consumption, and BER of D2D communication transceivers, previous generations have also proposed a variety of solutions.
A. In order to solve the problem of low bandwidth in D2D interconnection, higher order modulation transmission is adopted, but this method faces the problems of high power consumption and high BER.

B. In order to solve the problems of high BER and high power consumption, differential parallel NRZ transmission is adopted, but it is difficult to improve the bandwidth density.

C. In order to solve the problem of bandwidth density, single-ended parallel NRZ transmission is used, but its anti-jamming capabilities are weak. And this transmission depends more on advanced packaging technology, resulting in a sharp increase in cost.

D. In order to solve the problems encountered by ABC, chord encoding transmission is used, but it still has the problem of bandwidth improvement. Now these four ways are introduced and analyzed as follow.

![FIGURE 1. Chips interconnection of different technologies.](image_url)

**A. HIGHER ORDER MODULATION TRANSMISSION**

To address the high bandwidth requirements of D2D communication, the previous researchers used the high-order modulation technology PAM4(4 pulse amplitude modulation) [3]. Compared with NRZ (nonreturn-to-zero) signal transmission technology, PAM4 increases number of pulse amplitude modulation levels to achieve high-speed SerDes. Because of its high bandwidth characteristics, it has been widely used in the industry [4]. Simultaneously, the differential transmission technology is used to avoid the disadvantages of single-ended signal transmission, such as large common-mode-noise(CMN), large switching-synchronization-noise(SSN), and serious crosstalk(XTALK) between channels. However, the SNR of PAM4 signal is very low. In order to improve the SNR, it is necessary to introduce DFE at the receiver. In addition, when the rate reaches 112 Gbps, the timing on the DEF feedback path is very tense, and only a few taps of DFE can be designed. So the equalization ability is limited, and the error code can only reach 10E-5 [5], [6], [7], [8]. Although the D2D communication with high-order modulation technology can achieve high-bandwidth data transmission in organic substrate, the technology still has limitations in bandwidth density, power consumption and BER in practical applications.

**B. DIFFERENTIAL PARALLEL NRZ TRANSMISSION**

The parallel interface of a single-ended transmission has weak equalization capabilities. In the standard package, the total bandwidth of the D2D communication port is limited by the channel transmission distance [9]. With frequency of the signal is getting higher, the change of the signal edge is getting faster. The bandwidth of the single-ended transmission line cannot gradually meet the needs of D2D communication, so the traditional D2D communication port adopts differential parallel NRZ transmission. However, the parallel interface pin efficiency of differential transmission is half the efficiency of single-ended transmission parallel interface pins, so its bandwidth density is much lower than that of single-ended data transmission. The aggregate bandwidth is promoted by increasing the number of channels, so the pin efficiency of the chip becomes the primary reason for the low bandwidth density of the D2D communication port.

**C. SINGLE-ENDED PARALLEL NRZ TRANSMISSION**

In advanced packaging, the advantages of single-ended parallel transmission are high bandwidth density, low power consumption and low error rate. In 2019, Intel introduced AIB 1.2 protocol. As shown in Table 1, the protocol uses EMIB advanced packaging technology to achieve up to 24 single-ended data transmissions with a maximum single-channel rate of 2Gb/s and the bandwidth density is up to 150Gb/s/mm [10]. In 2020, TSMC and ARM collaborated to launch the LIPINCON protocol. The protocol uses EMIB and CoWoS technologies in advanced packaging technologies to achieve single-ended data transmission in a silicon intermediary using CoWoS packaging technology with a single channel maximum rate of 8Gb/s and the bandwidth density is up to 600 Gb/s/mm [11]. In February 2022, Intel, TSMC, Samsung, AMD, ARM, and Qualcomm jointly launched the UCIe protocol. The protocol uses EMIB and CoWoS technologies in advanced packaging technologies to achieve single-ended data transmission of up to 64 channels in silicon intermediaries with single-channel rates of 32 Gb/s and the bandwidth density is up to 1317 Gbs/mm [12]. However, with the increase of data rate, the anti-interference ability of single-ended signal becomes weaker, so the signal transmission is more dependent on advanced packaging technology, resulting in a high cost. Therefore, it is still a technical problem to apply single-ended signal to standard packaging for D2D communication.

**D. CHORD CODING TRANSMISSION**

To effectively increase the bandwidth density, high-pin-efficiency D2D communication interface technology with
chord coding has been used [13], [14]. This technology takes advantage of the interconnectivity of transmitted signals in multiple channels to transmit N bits in N+1 wires. The advantages of its method are high bandwidth density, low power consumption, and low BER. ENRZ transceiver technology is introduced by the international CEI organization, which improves pin efficiency compared to the traditional NRZ technology by transmitting 3 bits data in 4 wires [15], [16]. Kandou proposed the CNRZ-5 chord-coded data transceiver technology, which further improves the pin efficiency of data transmission by transmitting 5 bits data in 6 wires [17], [18]. The advantage of [18] is that through SST direct encoding and MIC direct decoding, the CNRZ-5 matrix can evenly distribute 5 bits of energy to each channel, ensuring that the binary codes decoded by the receiver are the same (eye height and eye width), as this helps the bathtub curves of the five eye diagrams to be similar, making the worst eye opening width wider than [17]. However, compared with ENRZ, the CNRZ-5 encoded signal has an asymmetric waveform in the output of the transmission. Therefore, it results in a low SNR of the receiver signal and the data rate is promoted difficultly.

In order to further improve the SNR and the bandwidth of the CNRZ-5 in D2D communication, a CNRZ-7 based transmitter matrix and receiver matrix are proposed firstly, which are derived from Walsh Hadamard(W-H) transform and inverse transformation. In addition, to reduce the power consumption of the transmitter, the encoding driver based on CNRZ-7 transmitter matrix is designed with source series terminated drivers(SST). To further improve the SNR of the receiver, the decoding circuit based on CNRZ-7 receiver matrix is designed with a special multi-input comparators(MIC), which contain equalizer circuits. The complete CNRZ-7 transceiver is designed by using forward clock architecture.

The structure of this study is as follows: The second chapter analyzes the high SNR and high bandwidth CNRZ-7 transceiver matrix algorithm. Chapter 3 details the system architecture and the circuit design, including encoding circuit, decoding circuit, and the clock of the CNRZ-7 transceiver. Chapter 4 describes the simulation results of CNRZ-7 and a comparison of the related literature.

II. CNRZ-7 TRANSCEIVER MATRIX ALGORITHM
The chapter focuses on the CNRZ-7 transceiver matrix algorithm and how it achieves high bandwidth and high SNR.

A. D2D COMMUNICATION PORT
As the performance requirements of high performance computers for computing and network chips increase dramatically, SoC technology for large chip design faces the problem of yield and power consumption. As shown in Fig.1, a better way to optimize SoC yield is to divide the SoC into two or more equivalent homogeneous chips and use D2D communication. Therefore, in order for smaller multiple chips to behave consistently with a single chip, higher requirements must be placed on the D2D communication. It has higher bandwidth density, lower power consumption, and lower BER(1E-15).

B. CHORD CODING
As mentioned above, due to higher bandwidth requirements, D2D communication use differential signal transmission methods. But the pin efficiency of differential parallel NRZ transmission is half of the single-ended one, so its natural properties determine that it is extremely difficult to increase the bandwidth density for differential parallel NRZ transmission. Chord coding solved the problem well.

To further explain the pin efficiency of signal transmission and chord coding, we introduced the Walsh function, which is composed of a square wave signal and is very convenient for computer calculations [19]. It takes the following form (1).

$$\text{wal}(i, t) = \prod_{k=0}^{p-1} \{R(k + 1, t)\}^{g(i)_k}$$  

(1)

$$R(k+1,t)$$ is the arbitrary Rademacher function, $$g(i)$$ is the gray code of $$i$$, and $$g(i)_k$$ is the $$k$$th digit of this gray code which is either 1 or -1. And P is a positive integer. This transformation has been applied in digital circuits, such as switched-capacitor realization [20] and DSP [21], but in this work, we apply it to analog design of string-coding circuit. When P=1, (2) and (3) are sampled to obtain. The second-order orthogonal matrix(4) is obtained.

$$\text{wal}(0, t) = 1, \ldots, \{1 - 1\}$$  

(2)

$$\text{wal}(1, t) = R(1, t) \ldots \{1 - 1\}$$  

(3)

$$W(0) = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$  

(4)

As shown in the matrix (4), Walsh’s matrix is orthogonal, and the first column is all 1. We summarize the differential signal transmission to the matrix transformation. Fig.2 shows that the common-mode voltage $$V_{CM}$$ is the first column of the matrix, and the signal is encoded up and down the common-mode point. Thus, the differential signal transmission method is the simplest chord coding and it is a way to solve the SSN problem, because differential transmission can eliminate the common mode noise(CMN) and greatly provide signal quality.

![FIGURE 2. Transfer Coding for DS.](image)

It can be observed that in the case of a certain bandwidth, the pin efficiency is only 50% relative to the single-ended signal transmission. Therefore, while maintaining the advantages of differential signal transmission at high
speed, improving pin efficiency has become a technical key. When \( P=2 \), the first four \( \text{Wal}(i,t) \) values are sampled. Four \( \text{Wal} \)-groups \([5], (6), (7), \) and \( (8)\) \) are enumerated to form a fourth-order orthogonal matrix \( (9) \).

\[
\text{wal}(0, t) = 1, \ldots, \{1 1 1 1\} \quad (5)
\]

\[
\text{wal}(1, t) = R(1, t) \ldots \{1 1 -1 -1\} \quad (6)
\]

\[
\text{wal}(2, t) = R(1, t) \cdot R(2, t) \ldots \{1 -1 1 1\} \quad (7)
\]

\[
\text{wal}(3, t) = R(2, t) \ldots \{1 -1 1 -1\} \quad (8)
\]

\[
W(0) = 
\begin{bmatrix}
1 & 1 & 1 & 1 \\
1 & 1 & -1 & -1 \\
1 & -1 & 1 & 1 \\
1 & -1 & -1 & -1
\end{bmatrix}
\quad (9)
\]

Walsh functions arranged by Hadama are derived from a 2nd-order Hadama matrix. \( 2n \)-order Hadamard matrix has the symbol change rule of each row, which corresponds to the symbol change rule of a Walsh function in the orthogonal interval. Each 2nd-order Hadama matrix corresponds to a discrete Walsh function. It can be summarized as equation \( (10) \).

\[
H_N = H_{2^n} = H_2H_{2^{n-1}} = 
\begin{bmatrix}
H_{2^{n-1}} & H_{2^{n-1}} \\
H_{2^{n-1}} & -H_{2^{n-1}}
\end{bmatrix}
\]

\quad \text{and} \quad H(0) = W(0) = [1], \quad H(1) = W(1) = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}
\end{equation}

\[(10)\]

and \( H(0) = W(0) = [1], H(1) = W(1) = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \) in equation \( (10) \). Using this related properties can produce any order Hadama matrix. Therefore, the orthogonal matrix \( (11) \) is obtained from matrix \( (4) \) through equation \( (10) \).

\[
H(2) = 
\begin{bmatrix}
1 & 1 & 1 & 1 \\
1 & -1 & 1 & 1 \\
1 & -1 & -1 & 1 \\
1 & 1 & -1 & -1
\end{bmatrix}
\quad (11)
\]

The matrix was proposed in 2013 and applied to ENRZ (3bits/4wires), which increased the pin efficiency of D2D communication from 50% to 75%. At the transmitter, binary data of 3 bits are encoded on 4 wires and one of the output eye diagrams on wires has four levels of equal height. And then through the channel, the decoding circuit recover the binary data in receiver. The emergence of the chord coding transmission significantly improves the pin efficiency on differential parallel NRZ transmission as shown in Fig.3. After a review of the literature, there is no theoretical process of matrix, so we carried out the analysis and derived circuit verification.

In 2016, Shokrollahi et al. proposed the CNRZ-5 transceiver technology [17], but there is inconsistent of five binary eye diagrams in the receiver. In order to solve the problems, [18] adopted a new matrix (as shown in Fig.4) and SST design and decrease the BER. But in [18], the eye-height in channel is inconsistent and the SNR is low.

C. CNRZ-7

As shown in Fig.3, when ENRZ coding method is used and the matrix \( (11) \) is completely symmetrical, the eye diagram of the four transmitter terminals are identical. The coding method can work at higher rates and higher insertion loss (20dB). However, as can be seen from Fig.5, when the CNRZ-5 coding method is used, the encoding matrix and decoding matrix are asymmetrical. The multi-level signal at the transmitting end will appear as two kinds of unequal height eye diagrams. SNR in CNRZ-5 of the transmitting signal is lower than ENRZ encoding, limiting the rate increase of D2D communication. Although the transmission method of CNRZ-5 has higher pin efficiency, it sacrifices a certain SNR.

According to equation \( (12) \), WH matrix \( H_T \) based on the 8th order is derived. D2D communication of the 8-channel transmission of 7 bits data is designed, which improves the pin efficiency to 87.5%. The eye diagram after encoding and decoding is shown in Fig.6. This scheme avoids the unequal height eye diagram of CNRZ-5, but the problem of low SNR still exists while improving pin efficiency. As the signal rate increases, the BER also increases. Therefore, in order to solve this problem, the matrix \( A \) is used for row transformation \( (13) \) which significantly improves the SNR when the information...
of the signal is not lost.

$$H_H = \begin{bmatrix}
H(2) & H(2) \\
H(2) & -H(2)
\end{bmatrix}$$

(12)

$$A = \begin{bmatrix}
1/2 & 0 & 0 & 0 & 0 & 1/4 & 0 & 0 \\
-1/2 & 1/4 & 1/4 & 0 & 0 & 0 & -1/4 & 0 \\
1/2 & 0 & 0 & 1/2 & -1/2 & 1/4 & 0 & 0 \\
1/2 & 0 & 0 & 1/4 & 0 & 0 & 0 & 1/4 \\
1/2 & 0 & 0 & 0 & 0 & -1/4 & 0 & 0 \\
1/2 & 1/4 & 1/4 & 0 & 0 & 0 & -1/4 & 0 \\
-1/2 & 0 & 0 & 1/2 & 1/2 & -1/4 & 0 & 0 \\
-1/2 & 1/4 & -1/4 & 0 & 0 & 0 & 0 & -1/4 \\
\end{bmatrix}$$

(13)

$$H_{CNRZ-7} = H_H \otimes A$$

Fig.7 shows the calculation method for the transmission matrix of this design and the electrical signal. $H_{CNRZ-7}$ matrix is composed of $-1$, $0$, and $1$. In the encoding process shown in Fig.7, the 7 bits signal is reasonably allocated to the eight corresponding channels according to the transmitter matrix. As shown in the post-simulation result in Fig.21, the number of levels transmitted on each channel is four. Using the transmitter matrix in Fig.7, 7 bits signal can be transmitted on 8 wires. Compared with the transmission scheme of CNRZ-5 (5bits/6wires), it not only improves the problem of the low SNR of CNRZ-5, but also further improves pin efficiency.

$$SNR = 20 \log(Q)$$

(14)

$$Q = \frac{P_t - P_b}{\sigma_1 + \sigma_0}$$

(15)

To further illustrate the advantages of CNRZ-7, a factor $Q$ is introduced, which represents the SNR parameter of the eye diagram [22]. The relationship between $Q$ and SNR given by (14), and the calculation method is (15). $P_t$ represents the average value of the logic high level of the signal and $P_b$ represents the average value of the logic low level. The rms value $\sigma_1$ of high level signal noise and the rms value $\sigma_0$ of low level signal noise, the sum of which is the rms value of signal noise. The $Q$ factor is the ratio of the signal amplitude to the noise amplitude.

We selected four kinds of signals (NRZ, ENRZ, CNRZ-5, and CNRZ-7) for comparison, and selected the worst eye at the transmitting end to analyze the $Q$ factor. As shown in the Fig.8(a), the simulation results indicate that:

(1) As the Nyquist-frequency($F_N$) increases, the overall SNR of the signal decreases. The SNR of CNRZ-7 is comparable to that of ENRZ.

(2) As the $F_N$ is 5G-10G, the SNR of CNRZ-7 is 2 times that of CNRZ-5. But as the frequency reaches 25G, the SNR of CNRZ-7 is 3.5 times that of CNRZ-5.

(3) At the same $F_N$, the total bandwidth of CNRZ-7 is 7 times that of NRZ, 2.3 times that of ENRZ, and 1.4 times that of CNRZ-5.

The quality of the SNR in transmitter determines the quality of the decoded binary eye diagram at the receiver. Fig.8(b) shows the receiver eye opening widths of four signals when BER is less than 1E-15 under different insertion loss($F_N$). It can be seen that at 10dB@20G, CNRZ-7 still maintains an eye width of 0.45UI when BER is less than 1E-15.

Therefore, CNRZ-7 not only address the problem of the low SNR on CNRZ-5, but also further improves pin efficiency and bandwidth.
D. Architecture

The architecture of the entire system is shown in Fig.9. The overall structure includes two transmitters, two receivers and a shared clock path. One of the transmitters combines seven groups of 64UI (1UI=25ps) low-speed parallel data streams into seven groups of 1UI high-speed one byMUXs(multiplexer). And then the driver transmits them through eight groups of SST based precoding circuits. The receiver decodes the high-speed data by seven MIC-CTLE (continuous-time linear equalizer) based decoding circuits. Then, the sampler and decomposer convert the serial data into the transmitter’s parallel data. Transmitter and receiver each have a MINI-PLL, including PFD, CP, Filter, VCO. The same is that both of them adopt a type-II PLL and ring oscillator structure. The difference is that TX-MINIPLL is low-power processing and outputs 4 phase clocks, while RX-MINIPLL of the receiver is combined with the forward clock and outputs eight orthogonal clocks. The clock data adjustment(CDA) circuit transmits the phase message to the phase interpolator (PI) in the PLL. Finally, the clock generated by the phase-locked loop is sampled to the best position of the data.

III. IMPLEMENTATION AND DESIGN

This transmitter consists of MUX, SST based precoding circuit and clock. The MUX consists of two parts: a low-speed MUX and a high-speed. Low-speed MUX is responsible for synthesizing 64 bits parallel low-speed data into 4 bits medium-speed data. High-speed one part is responsible for combining the 4 bits medium-speed data of 4UI into high-speed 1UI data. The SST based precoding circuit realizes the precoding and driving of the signal. The clock adopts the forwarded clock to provide clock reference for RX-MINIPLL, which is used to recover the high frequency clock for receiver.

A. Encoding Circuit

Each column in Fig.7 represents an encoder (SST driver: w0 \* w7), and each row describes a decoder (also called a subchannel) of the receiver. As shown in Fig.10, in each unit interval (UI), the transmitter adopts the driving method of voltage mode, which is also encoded and sent out while driving. And then 7 bits data (D0~D6) are encoded to 8 wires (w0~w7). Fig.11 shows the circuit design of the encoding circuit. The 8 groups of SST use the same circuit, and the input and output of the signal are performed according to Fig.7. Corresponding to each wire (each column of \( H_{CNRZ-7} \) matrix), the input bit will be encoded and the output driver are decoded correctly. The combined signal is placed on the corresponding wire with the target output impedance.

\[ R_{out} = \frac{(R_0 + R_1)}{3} \square / R_2 \]  

(16)

With the ever-increasing power consumption requirements of high-speed cable transceivers, SST (source-series terminated) is widely used due to its low power consumption and good linearity compared to traditional current-mode (CM)
drivers. The characteristic impedance \( Z_0 \) of this channel is 50Ω. According to the impedance matching principle, the output resistance of the driver should also be 50Ω. The output resistance of the driver is given by (16).

\[ V_{(w0)} = (3V_{CM} + V_{(D0)} + V_{(D2)} + V_{(D3)}) \times A \]  

(17)

\[ V_{(w1)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(18)

\[ V_{(w2)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(19)

\[ V_{(w3)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(20)

\[ V_{(w4)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(21)

\[ V_{(w5)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(22)

\[ V_{(w6)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(23)

\[ V_{(w7)} = (3V_{CM} + V_{(D1)} + V_{(D2)} + V_{(D3)}) \times A \]  

(24)

To ensure the matching impedance and prevent the influence of reflection on the circuit signal, four pairs of NMOS and PMOS are introduced, using the resistance characteristics of the MOS transistor to form a matching impedance circuit. Four pairs of digitally controlled NMOS, PMOS, and SST are used for matching and adjustment. The formed variable resistance is controlled by a pair of opposite \( R < 0.3 > \) and \( R_0 < 0.3 \). The logical expression for the SST circuit is given by (17). \( A(A=1/3) \) is the amplification factor of the drive circuit. \( W_1 \rightarrow W_7 \) links are presented in the form of equation (18), (19), (20), (21), (22), (23) and (24).

B. Decoding Circuit

The eight SST circuits are used for decoding and driving of the circuit design, encoding the signal on eight lines. The receiving end also includes seven decoding circuits-MIC, as shown in Fig.12, which uses a differential structure to decode the encoded 4-level signal into two-levels, as shown in Fig.13. The eight wires are connected to seven MIC circuits according to the decoding matrix shown in Fig.7. The circuit expression corresponding to the last line of the decoding matrix \([1 1 1 1 -1 -1 -1] \) is (25), which decodes the D6 signal. The input stage of each MIC performs an inverse linear transformation (linear combination), which results in seven binary data by correlation operation (25), (26), (27), (28), (29), (30), and (31).

\[ V_{OUT,6} = [w_0+w_1 + w_2 + w_3-w_4-w_5+w_6-w_7] \times g_mR \]  

(25)

\[ V_{OUT,0} = [w_0-w_1] \times g_mR \]  

(26)

\[ V_{OUT,1} = [w_1-w_2] \times g_mR \]  

(27)

\[ V_{OUT,3} = [w_0+w_1-w_2] \times g_mR \]  

(28)

\[ V_{OUT,3} = [w_6+w_7-w_4-w_5] \times g_mR \]  

(29)

\[ V_{OUT,4} = [w_5-w_4] \times g_mR \]  

(30)

\[ V_{OUT,5} = [w_6-w_7] \times g_mR \]  

(31)

Fig.13(a) shows an improvement in the traditional equalizer, and the transfer function is (32). Fig.14 shows the channel S12 parameters used for the simulation in this study. The parameters of this channel are extracted from a real 50mm long organic substrate channel. At the 20GHz Nyquist
FIGURE 9. Design framework for CNRZ-7.

FIGURE 10. Voltage-mode output driver combined with CNRZ-7 encoder for w0.

FIGURE 11. SST circuit for w0.

FIGURE 12. Multiple input comparator logic for D6.

frequency, the channel has 10dB attenuation as shown in Fig.14(a). We simulated the transfer function of the MIC and CTLE based decoding circuit mentioned above, as shown in Fig.14(b), to meet the channel requirement of 10dB loss at a 20GHz Nyquist sampling frequency.

\[
A(s) = \frac{g_m R/3}{1 + g_m R S/2} \left(1 + s \cdot \frac{C_s R_s}{1 + s \cdot \frac{C_s R_s}{3R_C}}\right) \left(1 + s \cdot \frac{1}{3R_C}\right)
\]  

(32)

By changing the W/L of the input PMOS in Fig.13(a), MIC is formed as shown in Fig.13(b). The circuit structure can not only decode binary signal, but also play a role of equalization.

C. RX-MINIPLL

The RX-PLL shown in Fig.15 adopts a divide-by-four structure. The output of the ring oscillator (number of ring oscillations, N=4) comprises eight phases to improve the rotation accuracy of the PI. Clock and data alignment (CDA) is used
to detect 8 bits edge information, and after thermometer coding, 3 phase codes and 32 thermometer codes are generated, as shown in Fig.15. When the clock generated by the phase-locked loop is sampled to the best position of the data, it is locked and the output clock jitter is 3.2ps.

\( R_1 \) and \( R_2 \) are the load resistors with equal resistance values. Each differential-pair transistor is a parallel current source controlled by 32 switches, \( P<3> \), \( P<2> \), and \( P<1> \) are used to generate the gray code of the control quadrant to avoid competitive risk in Fig.16(c), which is generated by the high 3 bits of the 8 bits control code and Bit0-Bit31 is a thermometer code with 32 control phases, generated by the lower 5 bits of an 8 bits control code to effectively detect data along the information in Fig.16(a). After logical operation, the control bits of the current path controlling the current source are finally generated as SWITCH_0, SWITCH_45, SWITCH_90, SWITCH_135, SWITCH_180, SWITCH_225, SWITCH_270, and SWITCH_315, as shown in Fig.16(b).

\[ V_{out} = A_1 \sin(\omega t) + A_2 \sin(\omega t + \varphi_d) \]
\[ \varphi_{out} = \arctan\left( \frac{A_2 \sin \varphi_d}{A_1 + A_2 \cos \varphi_d} \right) \] (33)

From Formula (33), the output phase is a function of \( A_1 \), \( A_2 \), and \( \varphi_d \). The sizes of \( A_1 \) and \( A_2 \) are determined using the control code \( n \). In the case of different phase differences, the output phase changes when the weight coefficient \( A_2 \) changes from 0 to 1.

Fig.17 shows the equivalent current-source phase interpolator structure. The input transistors M1-M8 have the same size, the loads R1 and R2 are equal R. The input is an 8-phase clock, the phase difference of which is 45°. V0 and V4, V1 and V5, V2 and V6, V3 and V7 form four differential pairs.

**Fig. 14.** Insertion Loss and Equalization Compensation. (a) is the insertion loss, (b) is the equalization compensation.

**Fig. 15.** Design of PI based Phase-Locked Loop.

The PI outputs the clocks of different phases through a linear combination of the input clocks under different weights to realize the phase interpolation function. The output signal of the phase interpolator is expressed as (33).

**Fig. 16.** TEM-CODE block. Binary code (P3, P2, P1, A5, A4, A3, A2, A1) to thermometer code. (a) is the lower five bits coding to thermometer codes, (b) is the higher three bits coding to P<2:0>, (c) is the phase variation design.
Fig. 23 shows the eye diagrams of 7 bits from the output of the MIC with 10 dB CTLE. There are seven clear and consistent eye diagrams in Fig. 23. The worst eye diagram of seven still keep a higher quality (eye-height = 200 mV, eye-width = 20 ps).

Table 2 lists the energy consumption and the proportion of the transceiver. The power consumptions of the transmitter (TX) and receiver (RX) are 320 mW and 271.04 mW (52% and 44%) respectively. The transmitter and receiver are comprised of three modules: digital, analog, and PLL. In the transmitter, the power consumption of digital is 49.28 mW (24.64%), mainly used for 64:16 MUX and 16:4 MUX. TX-MINIPLL power consumption is 61.6 mW (10%). The transmitter analog power consumption is 209.44 mW (30.8%).
of which 162mW is used for the SST drive circuit. In the receiver, the power consumption of the analog part is 184.8mW (30%) for MIC decoding circuit, 1/4 sampler circuit and PI. The power consumption of the digital part mainly includes 4:16 DMUX and 16:64 DMUX, and the total power consumption is 61.6mW (10%). The RX-MINIPLL adopts the forward clock structure, and the power consumption is only 24.65mW (4%). The remaining power consumption (4%) is used to generate the bias circuit. As shown in Fig.24, analog power consumption accounts for 64% of the overall design. At 125°C temperature and tt corner, the power consumption of the simulated transceiver is measured to be 1.1pJ/b.

**TABLE 2.** Power consumption and percentage.

| MOD  | TX | RX | Others |
|------|----|----|--------|
| ENG  | mW | PLL| Ana | Dig| PLL| Ana | Others |
| PLL  | 49 | 62 | 209 | 62 | 25 | 185 | 30.8 |
| PLL  | 8  | 10 | 34  | 10 | 4  | 30  | 4     |

**TABLE 3.** Performance comparison.

| Reference | Unit | [24] | [17] | [18] | This work |
|-----------|------|------|------|------|-----------|
| Year      |      | 2018 | 2016 | 2020 | 2022      |
| Signaling | Gb/s | 25   | 20.83| 20.83| 35        |
| Date Rate | b/s  | 8.5  | 3    | 6    | 8         |
| Insertion loss | dB | 16 | 28 | 16 | 28 |
| Technology | pJ/b | 1.17 | 0.94 | 1.02 | 1.1 |
| Energy Efficiency | b/b | 1E-15 | 1E-15 | 1E-15 | 1E-15 |
| Core area(RX+TX) | mm² | 0.75 | 1.5 | 2.4 | 0.66 |
| Throughput(RX+TX) | Gb/s | 200 | 250 | 1000 | 360 |
| Density of BW | Gb/s/mm² | 266.7 | 166.3 | 416.7 | 844 |

Table 3 shows the performance of the previous work compared to this one. There is a decrease in the area relative to [17], [18], [24], and a slight decrease in power consumption relative to [24]. This work increases bandwidth density up to 848 Gb/s/mm, which can support an effective throughput of 35 Gb/s/wire for D2D communication. Compared to [17], [18], CNRZ-7 exhibits greater advantages on bandwidth density. With better encoding, it can support a higher insertion loss(10dB) and lower BER.

Fig.25(a) shows the BER for 7 bits of data without the layout parasitic. The worst eyes eye-opening is 14ps(0.56UI) at BER=1E-15. But due to the limited time and data quantity of simulation, the bathtub curve can only be simulated to 1E-11.
after extracting the layout parasitic, as shown in Fig. 25(b). The worst one in Fig. 25(b) is 11.2 ps(0.45 UI) at BER = 1E-15 by fitting and forecasting from Fig. 25(a).

**V. CONCLUSION**

Traditional D2D communication use differential signal transmission methods. When the aggregate bandwidth is increased by increasing the number of channels, the pin efficiency of the chip will become the main reason for the low bandwidth density of the D2D communication ports. In this study, system analysis and modeling of chord coding theory are performed, and the design provides a solution to this problem. The bandwidth density of the D2D communication is increased by reducing the number of pins without reducing the total bandwidth. By using CNRZ-7 transceiver technology, the transmission bandwidth is increased to 35 Gb/s/wire, and the total bandwidth is 560 Gb/s.

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