SnO$_2$ Nanowire Arrays and Electrical Properties Synthesized by Fast Heating a Mixture of SnO$_2$ and CNTs Waste Soot

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Abstract SnO$_2$ nanowire arrays were synthesized by fast heating a mixture of SnO$_2$ and the carbon nanotubes waste soot by high-frequency induction heating. The resultant SnO$_2$ nanowires possess diameters from 50 to 100 nm and lengths up to tens of micrometers. The field-effect transistors based on single SnO$_2$ nanowire exhibit that as-synthesized nanowires have better transistor performance in terms of transconductance and on/off ratio. This work demonstrates a simple technique to the growth of nanomaterials for application in future nanoelectronic devices.

Keywords SnO$_2$ nanowires · Semiconducting · Field-effect transistor

Introduction

One-dimensional semiconductor nanowires and nanotubes have stimulated increasing attention in the last few years and are expected to lead to novel device application due to their intriguing properties and potential applications in constructing nanoscaled electronic and optoelectronic devices [1–12]. Among semiconductor oxide nanostructure, SnO$_2$ nanowires, nanobelts, and nanowires are very important n-type semiconductors for applications as transparent conducting electrodes [12], gas sensors [13], and lithium-ion batteries [14], which utilize the unique characteristics of SnO$_2$ nanostructures including a wide band gap ($E_g = 3.6$ eV at 300 K) and large surface-to-volume ratios. A precondition for SnO$_2$ nanostructures based on the applications is an easy and large-scale synthesis of SnO$_2$ nanostructures. Several methods have been reported for the synthesis of SnO$_2$ nanowires/nanobelts, including thermal decomposition [15], electrospinning [16, 17], solution-based crystal growth [18, 19], laser ablation, and template-based approaches [20]. However, those methods always required long time for heating and cooling, which hinder the mass production of SnO$_2$ nanostructures. Due to its versatility and simplicity, the synthesis method of SnO$_2$ nanowires is still investigated [21].

The electrical properties of SnO$_2$ nanowires and nanobelts are also reported [22, 23]. Field-effect transistors (FETs) based on single carbon nanotube, Si nanowire, ZnO nanowire and others are with excellent properties superior to their bulk counterparts [24, 25]. SnO$_2$ nanowires are one of the potential semiconducting materials for nanoelectronic devices due to their excellent electronic properties. In the present study, we report a novel method to synthesize aligned SnO$_2$ nanowires by using high-frequency inductive heating furnace. A mixture of SnO$_2$ and the carbon nanotubes (CNTs) waste soot which was a main by-product in the production of CNTs by arc-discharge. The electrical properties including application in FETs of SnO$_2$ nanowires were also studied.
Experimental

The fabrication of nanowires was carried out in a high-frequency introduction furnace. The schematic diagram of the apparatus is shown in Fig. 1. The SnO$_2$ nanowires were synthesized on a silicon substrate by heating pure SnO$_2$ powders (50 wt.%) and CNTs waste soot (50 wt.%) which was a main by-product in the production of CNTs at 1,027 K in the quartz tube. An appropriate amount of source powders (about 1 g) and the silicon substrate separated by 10 cm were put in the center of the quartz tube. The silicon (100) substrate patterned with Au using conventional photolithographic method was located downstream of the source powders. The precursor was loaded in a graphite boat and located in a high-purity graphite tube. As a heating crucible, the graphite tube was placed in a horizontal quartz tube and heated in a high-frequency induction furnace. The quartz tube was first evacuated at $10^{-2}$ Torr by a vacuum pump. After heated up to the desired temperature (1,027 K), an Ar gas flow at a rate of 20 SCCM was introduced, and the growth was initiated and maintained for less than 3 min. When the system was cooled to room temperature, many white products were formed on the surface of the substrate.

![Fig. 1 Schematic diagram of the apparatus for synthesis of SnO$_2$ nanowires](image)

The as-grown SnO$_2$ nanowires were characterized by scanning electron microscopy (SEM, FEI SIRION 200) equipped with energy-dispersive X-ray spectroscopy (EDX, INCA OXFORD) and transmission electron microscopy (TEM, JEM-2010). The electronic measurements were made using an Agilent 4156C semiconductor characterization system under an ambient condition at room temperature.

Results and Discussions

Figure 2 is the morphology of as-synthesized nanowires. Figure 2a and b show two typical SEM images of the

![Fig. 2 a, b The typical SEM images of as-synthesized aligned SnO$_2$ nanowires, c low-magnification TEM, and d HRTEM image of single SnO$_2$ nanowire](image)
as-grown SnO₂ ordered nanowire arrays deposited on the silicon substrate. It can be observed that large quantities of nanowires were grown vertically on the silicon substrate and formed the SnO₂ nanowire arrays with the length of tens of micrometers, and the surfaces of the nanowires are uniform and smooth. Structural properties of the nanowires were further studied with TEM. Figure 2c shows a low-magnification TEM image of single SnO₂ nanowire with diameters ranging from ~20 nm. It can be seen that the SnO₂ nanowire is very smooth, straight, and uniform, and the geometrical shape is structurally perfect. The crystallography of the nanowires was investigated by select area electron diffraction (SAED) pattern. High-resolution TEM (HRTEM) (Fig. 2d) shows that the as-synthesized SnO₂ nanowire is single crystalline. The interplanar spacing is about 0.334 nm, which is corresponding to the (110) plane of rutile crystalline SnO₂.

Figure 3 shows X-ray diffraction (XRD) patterns of SnO₂ nanowires. All the diffraction peaks can be indexed to the tetragonal rutile structure of SnO₂. The SnO₂ lattice constants obtained by refinement of XRD data are $a = 4.737 \, \text{Å}$, $c = 3.185 \, \text{Å}$, which are consistent with bulk rutile SnO₂ tetragonal structure [26]. It indicates that SnO₂ nanowires are in excellent accordance with a rutile structure. To study the composition of single as-prepared nanowire, EDS measurements (Fig. 4) have been performed on individual nanowire. All the resultant nanowires are mainly composed of Sn, O, and C (come from CNTs).

Figure 5 shows the FT-IR spectrum in the range of 1,000–4,000 cm$^{-1}$ of as-synthesized SnO₂ nanowires. It shows dominant peaks at 1,635, 2,377, 2,925, 3,467, and 3,865 cm$^{-1}$ which corresponds to Si–O, Sn–O, C–O, CNT, H–O–H, and C–Hx, respectively [27, 28]. The peak near 1,635 cm$^{-1}$ can be assigned to the vibration of O–Sn–O that corresponds to the $A_{2u}$ mode [29]. The peaks near 2,370 cm$^{-1}$ agreed with stretching vibrations of Sn–O bonds [30].

These peaks confirm that SnO₂ nanowires possess the crystalline structure of the tetragonal rutile structure, which is corresponding to the results of XRD.

The growth mechanism of these aligned SnO₂ nanowires follows the conventional vapor–liquid–solid during the experiment. In terms of this mechanism [31], there exist three processes. First, SnO₂ powders react with CNTs waste soot powder, which results in the formation of SnO gas under high temperature. Subsequently, SnO gas will decompose to Sn and O₂ at a temperature higher than 1,027 K. Some Sn droplets reacted with the Au particles and formed Au–Sn alloyed droplets. These alloyed droplets can provide the energetically favored sites for formation of SnO₂ nanowires. Finally, aligned SnO₂ nanowires were produced by the reaction with Sn and O₂ during the process of transporting the Sn to the substrate by carrier gas. Moreover, the temperature is reached in several short seconds during high-frequency induction heating process.
which results in eliminating the dimensional growth of the Au species present on the surface, so it gives rise to the formation of SnO$_2$ nanowires, while other nanostructure products can not be formed. The following chemical reaction equations are proposed to explain the growth mechanism:

\begin{align*}
\text{SnO}_2(s) + C(s) & = \text{SnO}(g) + \text{CO}_2(g) \quad (1) \\
2\text{SnO}(g) & = 2\text{Sn}(l) + \text{O}_2(g) \quad (2) \\
\text{Sn}(l) + \text{O}_2(g) & = \text{SnO}_2(l) \quad (3)
\end{align*}

After growth, the SnO$_2$ nanowires were transferred from silicon substrates, and a number of FETs device structures were fabricated. Devices were fabricated by thermally growing SiO$_2$ film with 500 nm thickness on the top of n-type Si wafers, followed by deposition of an Au layer with sputtering and standard photolithography. Parallel Au electrode pairs, with \( \sim 1 \) \( \mu \)m in length and 80 nm in thickness, were patterned. The parallel Au electrodes will be used as source and drain electrodes. An n-type silicon layer serves as the back gate. The as-prepared SnO$_2$ nanowires were sonicated into a suspension in ethanol, followed by solution casting the slightly dispersed SnO$_2$ nanowires between the drain and the source of Au electrodes to form a single SnO$_2$ nanowire FET (SnO$_2$-FET). The SnO$_2$-FET samples were quickly transferred to a stove to anneal in Ar at 973 K for 5 min in order to improve the quality of Au–SnO$_2$ contacts. The inset in Fig. 3 is the SEM image of the as-fabricated single SnO$_2$ nanowire with a channel width of \( \sim 200 \) nm.

The current–voltage of drain and source \( (I_{ds}–V_{ds}) \) data of the device are shown in Fig. 6. The gate voltages were applied from 0 to 9 V and the drain voltages were from \(-1.0\) to 1.0 V for room temperature samples. It is very clearly shown that we have demonstrated that the conductance increased with the increase of the back gate voltage, which indicates an n-type property for the SnO$_2$ nanowire. The possible reason is due to oxygen vacancies and extra gallium interstitial atoms in the lattice during the synthesis process [32]. An on/off current ratio \( (I_{on}/I_{off}) \) of more than $10^5$ has been achieved at \( V_{gs} \) from \(-1 \) to 1 V with \( V_{ds} \) of 0.2 V. The FETs based on single SnO$_2$ nanowire exhibited better electrical properties, which affected both on/off current ratio and threshold voltage of the devices. Figure 6. shows a typical \( I_{DS}–V_{DS} \) characteristic of single SnO$_2$ nanowire FETs. The mobility can be calculated from the following formula [33–35]

\[ \mu_e = \frac{g_m L^2}{CV_{DS}} \]  
(4)

\[ g_m = \frac{dI_{DS}}{dV_g} \]  
(5)

\[ C = \frac{2\pi\varepsilon_0\varepsilon}{h(2h/r)} \]  
(6)

where \( g_m \) is the transconductance, \( C \) is the capacitance and \( L \) is the channel length, \( \varepsilon \), \( h \), and \( r \) are the dielectric constant, the thickness, and the radius of silicon dioxide, respectively. Using \( \varepsilon = 3.9 \), \( h = 500 \) nm, \( L = 1.5 \) \( \mu \)m, and \( r = 15 \) nm, it can be calculated \( \mu_e = 169 \) cm/V s at \( V_{DS} = 0.3 \) V. This value is consistent with those obtained in planar single-crystalline SnO$_2$ nanowire and other metal oxide nanowires. The performance of SnO$_2$-FET devices depends to a large extent on the source and drain contacts. In our cases, we find that it is effective to improve the quality of Au–SnO$_2$ contacts by annealing the SnO$_2$-FET devices in Ar at 973 K for 5 min. Therefore, the value of effective mobility, transconductance, and on/off ratio has also been significantly improved.

**Conclusions**

We present a simple, fast, and a low-cost method to synthesize SnO$_2$ nanowire arrays by using fast heating furnace. A ball-milled mixture of SnO$_2$ and CNTs waste soot was used as source materials. SEM and TEM images show nanowire diameters of 50–100 nm and lengths up to tenths of micrometers. The electrical properties of the as-synthesized single SnO$_2$ nanowire in FETs devices show that the n-type SnO$_2$ nanowires have larger on/off ratio (>10$^5$) and higher carrier mobility at room temperature. This method provides a promising candidate for large-scale preparation of SnO$_2$ nanostructures.

![Fig. 6](image-url)  
*Fig. 6* Transistor characteristic of back-gated single SnO$_2$ nanowire FET devices on silicon substrates: \( I_{ds}–V_{ds} \) curves for gate voltages with \( V_{gs} = 9 \) V to 0 in \(-3 \) V steps from top to bottom. The inset is the SEM image of the as-fabricated single SnO$_2$ nanowire.
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