Reliability-Aware SPICE Compatible Compact Modeling of IGZO Inverters on a Flexible Substrate

Je-Hyuk Kim 1,†, Youngjin Seo 1,†, Jun Tae Jang 1, Shinyoung Park 1, Dongyeon Kang 1, Jaewon Park 2, Moonsup Han 3, Changwook Kim 4, Dong-Wook Park 2,* and Dae Hwan Kim 1,4,*

1 School of Electrical Engineering, Kookmin University, Seoul 02707, Korea; jhyuck93@kookmin.ac.kr (J.-H.K.); ssoocw1535@kookmin.ac.kr (Y.S.); jjang@kookmin.ac.kr (J.T.J.); shinyoung94@kookmin.ac.kr (S.P.); orega715@kookmin.ac.kr (D.K.)
2 School of Electrical and Computer Engineering, University of Seoul, Seoul 02504, Korea; wpqsk2@naver.com
3 Department of Physics, University of Seoul, Seoul 02504, Korea; mhan@uos.ac.kr
4 Circadian ICT Research Center, Kookmin University, Seoul 02707, Korea; ncwkim@kookmin.ac.kr
* Correspondence: dwpark3l@uos.ac.kr (D.-W.P.); drlife@kookmin.ac.kr (D.H.K.)
† These authors are co-first authors.

Abstract: Accurate circuit simulation reflecting physical and electrical stress is of importance in indium gallium zinc oxide (IGZO)-based flexible electronics. In particular, appropriate modeling of threshold voltage ($V_T$) changes in different bias and bending conditions is required for reliability-aware simulation in both device and circuit levels. Here, we present SPICE compatible compact modeling of IGZO transistors and inverters having an atomic layer deposition (ALD) Al$_2$O$_3$ gate insulator on a polyethylene terephthalate (PET) substrate. Specifically, the modeling was performed to predict the behavior of the circuit using stretched exponential function (SEF) in a bending radius of 10 mm and operating voltages ranging between 4 and 8 V. The simulation results of the IGZO circuits matched well with the measured values in various operating conditions. It is expected that the proposed method can be applied to process improvement or circuit design by predicting the direct current (DC) and alternating current (AC) responses of flexible IGZO circuits.

Keywords: indium gallium zinc oxide; IGZO TFT; SPICE simulation; flexible device; inverter; compact modeling; reliability-aware simulation; PET substrate

1. Introduction

Recently, amorphous indium gallium zinc oxide (a-IGZO) has drawn much attention as an active channel material for thin-film transistors (TFTs) because of its relatively high mobility, low off-current, high $I_{on}/I_{off}$ ratio, and low-temperature process [1–5]. In particular, IGZO TFTs can be fabricated on a flexible substrate, such as polyethylene terephthalate (PET) and polyimide (PI), through a low-temperature process, and they have been applied to rollable and foldable electronics [6–8]. However, the inherent performance degradation caused by bending conditions and bias stress is problematic in flexible IGZO systems. Therefore, a systemic study about the effect of mechanical and electrical stress on long-term reliability should be performed at both device and circuit levels. It is necessary to predict the circuit operation in alternating current (AC) driving conditions through simulations that reflect analysis results. Until now, there has been much research on direct current (DC) stress [9–17], even though most circuits are driven in AC conditions. Hence, it is very important to analyze the instability characteristics of IGZO devices and circuits in various AC conditions so that compact modeling can be drawn for the reliability-aware SPICE (Simulation Program with Integrated Circuit Emphasis) simulation.

Generally, a positive gate bias stress (+$V_G$) on IGZO TFTs results in a positive shift of threshold voltage ($V_T$). This is due to electron-trapping inside the gate insulator and on the interface trap. However, when the gate insulator is aluminum oxide (Al$_2$O$_3$) deposited...
by atomic layer deposition (ALD) at low temperatures, in addition to electron-trapping that generates positive $\Delta V_T$, there is also a hydrogen migration mechanism that generates negative $\Delta V_T$ [18–23]. Cho et al. investigated the static and dynamic bias stress-induced charge trapping and de-trapping in IGZO TFTs [18]. On et al. examined the impact of channel length on the performance of IGZO TFTs with self-aligned structures [19]. Although these studies investigated the mechanism of $V_T$ shift in various conditions, the studies were performed at the transistor level, which has a limitation in circuit-level AC simulation.

In this paper, we analyzed the performance of IGZO TFTs and inverters based on the aforementioned degradation mechanisms, while mechanical stress (bending) and electrical stress (AC stress) were applied simultaneously. The NMOS-only inverters were fabricated on a flexible PET substrate consisting of a low-temperature processed a-IGZO and an ALD Al$_2$O$_3$ gate insulator. The electrical stress and recovery on the driver and load transistor of the inverters were analyzed under AC bias conditions. Multiple bending tests were also performed for the mechanical stress test. Parameters such as $\tau(V)$, $\beta$, and $\Delta V_{T0}(V)$ were obtained by applying the stretched exponential function (SEF) to the instability characteristics that appeared in each stress condition [24,25]. These parameters were loaded into HSPICE so that the simulation could reflect the $\Delta V_T$ in real-time, while AC bias was applied. This work can be a useful approach for a reliability-aware simulation of flexible IGZO circuits, enabling a circuit operation prediction based on compact modeling.

2. Fabrication and Measurement

In this study, a-IGZO was processed on a flexible PET substrate by taking advantage of its low-temperature process. The 3-dimensional (3D) structure and circuit diagram of the NMOS-only inverter are shown in Figure 1a,b. Copper (Cu) gate metal with a thickness of 20 nm was deposited using an electron-beam (e-beam) evaporator. The 40 nm Al$_2$O$_3$ gate insulator was deposited using an ALD system at 80 °C. In detail, an ALD Al$_2$O$_3$ film was formed using Al(CH$_3$)$_3$ (trimethylaluminum; TMA) and H$_2$O.

![Figure 1](image_url)

Figure 1. (a) 3-dimensional (3D) structure and (b) circuit diagram of an NMOS-only indium gallium zinc oxide (IGZO) inverter. (c) Top view of the fabricated IGZO inverter. (d) Schematic of bending test tool and bending measurement using the fabricated flexible device.

Thereafter, a target with the ratio of In$_2$O$_3$:Ga$_2$O$_3$:ZnO = 1:1:1 mol% was radio frequency (RF) sputtered to form a 35 nm IGZO channel under the condition of Ar:O$_2$ = 3:0.1 sccm. Source and drain electrodes (40 nm Cu) were also deposited using an e-beam evaporator. The gate insulator was wet-etched using buffer oxide etchant (BOE) for metal
interconnection, followed by a metallization performed with 60 nm Cu to connect the inverter circuit. A top view of the fabricated device for which inverter manufacturing has been completed is shown in Figure 1c.

The mechanical stress to the IGZO inverters was applied with a bending radius of 10 mm, and the electrical stress was tested by applying DC/AC stress to $V_{GS}$ and $V_{DS}$ using Keithley 4200. The schematics of the bending test, bending tool, and bending measurement of the fabricated flexible device are shown in Figure 1d. It should be noted that some local surfaces with small dimensions might experience negligible bending stress.

3. Result and Discussion

3.1. Analysis Process

The analysis process for the inverter simulation is shown in Figure 2. The load and driving transistors will be under electrical stress depending on the driving condition of the device. The two types of electrical stress that can be applied to each transistor (Figure 2a) are current stress (CS) and positive bias stress (PBS). The electrical stress will affect $V_T$, and the $V_T$ change will result in the voltage transfer curve (VTC) of the inverter. In general, when the gate insulator is composed of SiO$_2$, the cause of the positive $V_T$ shift due to the PBS condition can be explained by electron trapping (Figure 2b,c) [24-27]. However, when Al$_2$O$_3$ is deposited by low-temperature ALD, the AlO-H bonding tends to have weak bonding that can lead to a negative $V_T$ shift. This is known as a hydrogen migration phenomenon as a result of the movement of H$^+$ ions (Figure 2b,c) [18-23]. The movement of electrons and hydrogens when the positive voltage is applied to the gate electrode is represented in Figure 2b.

![Figure 2](image_url)

**Figure 2.** Analysis process for the inverter simulation. (a) Two types of electrical stress can be applied to load and driver transistors: positive bias stress (PBS) and current stress (CS). (b) Schematic of electron trapping and hydrogen migration in an IGZO transistor. (c) Threshold voltage shift ($\Delta V_T$) upon electron trapping and hydrogen migration. (d) Concept of AC inverter simulation based on a compact model of $\Delta V_T$ in load and driver transistors.

In this experiment, the effects of electrical stress were measured and analyzed in accordance with the physical states of flat and bending conditions. The results showed that negative and positive shifts of $V_T$ were mixed because of the aforementioned electron trapping and hydrogen migration phenomena. In particular, in the case of AC driving, where the stress/recovery situation is repeated, the parameters $\Delta V_T$ and $\tau$ were extracted using the SEF Equation (1). The compact model was mounted on HSPICE, and the load/driver transistors for AC simulation and its consistency were verified for the change of $V_T$, as shown in Figure 2d.

$$V_T = \Delta V_{TD} \left(1 - e^{-\left(\frac{t}{\beta}\right)^\rho}\right)$$  (1)
3.2. SPICE Compatible Compact Modeling

To analyze the reliability of the inverter operation, compact modeling of the load/driver transistors during the DC and AC bias should be studied. From the inverter schematic in Figure 2a, it is known that the CS condition dominates for the load transistor in which $V_{GS}$ and $V_{DS}$ are simultaneously applied, while the PBS condition dominates for the driver transistor. To implement experimentally the CS/PBS stress and recovery conditions, the change of the transfer curve was observed for up to 1800 s in each case. The width ($W$) and length ($L$) of the load transistor were designed as $W/L = 50/5 \mu m$ and of the driver transistor were designed as $W/L = 50/5 \mu m$. Additionally, different $V_{GS}$ and $V_{DS}$ bias conditions ranging from 4 V to 8 V were applied to see the change of device characteristics in accordance with the applied voltage. The transfer curve change over time when 4 V and 7 V of $V_{GS}$ and $V_{DS}$ were applied (i.e., CS condition) to the load transistor in a flat state is shown in Figure 3a, respectively. The threshold voltage shift ($\Delta V_T$) depending on the stress and recovery time is summarized in Figure 3c. Meanwhile, the transfer curve changes and the summarized $\Delta V_T$ when the load transistor was in a bending condition are shown in Figure 3d–f.

![Graphs showing threshold voltage shift in flat and bending conditions.](image)

Figure 3. Threshold voltage shift ($\Delta V_T$) of load transistors in flat and bending conditions. (a) Transfer curve change in flat conditions when $V_{GS} = V_{DS} = 4$ V and (b) when $V_{GS} = V_{DS} = 7$ V. (c) Summarized $\Delta V_T$ of flat load transistors depending on the stress and recovery time. (d) Transfer curve change in bending radius of 10 mm when $V_{GS} = V_{DS} = 4$ V, and (e) when $V_{GS} = V_{DS} = 7$ V. (f) Summarized $\Delta V_T$ of bending load transistors depending on the stress and recovery time.

From the measurement results, it can be seen that a positive $\Delta V_T$ and a negative $\Delta V_T$ were mixed under stress and recovery conditions, and the trend changed for various voltages. In general, when electron trapping occurs in the gate insulator, a positive $\Delta V_T$ occurs because more gate bias is required for the same channel charge, and the opposite phenomenon occurs when de-trapping takes place. As mentioned above and in other studies [18–23], the hydrogen migration takes place opposite to the electron trapping by $H^+$.
cations, which results in a negative $\Delta V_T$ for the hydrogen migration and a positive $\Delta V_T$ for the recovery of hydrogen migration. For the flat load transistors, as shown in Figure 3c, the largest positive $\Delta V_T$ was observed in low-voltage stress, which is attributed to the dominant electron trapping. In the recovery condition, the total amount of charge contributed by the recovery of hydrogen migration is dominant, which results in a positive $\Delta V_T$. The measurement results in the bending condition were similar, as shown in Figure 3d–f. The larger $\Delta V_T$ range is attributed to the increased oxygen vacancy during the tensile stress along the channel direction, which can increase the hydrogen migration [28,29].

The $\Delta V_T$ over time for the driver transistors in the PBS stress/recovery conditions is shown in Figure 4. The biggest difference from the result of the load transistor in Figure 3 is that, because there is no drain bias, electrons and hydrogens move only with gate bias. This could enhance the effect of $V_{GS}$ bias throughout the entire channel region. The driver transistors in the flat state are shown in Figure 4a–c, while those for the bending condition are shown in Figure 4d–f. Overall, the negative $\Delta V_T$ component increased, which is attributed to the larger hydrogen migration effect caused by greater charge movement throughout the channel.

As shown above, the physical and electrical stresses can cause various $\Delta V_T$ trends, which could affect the operation of the complex circuit. Therefore, based on the DC characteristics of a single device and its appropriate modeling, the $V_T$ instability of the load and driver transistors was predicted for an accurate transient simulation. In detail, the beta ($\beta$) and tau ($\tau$) were extracted using the measured $\Delta V_T$ and Equation (1). A more
detailed SEF model is presented in the below Equation (2), which reflects both negative and positive $\Delta V_T$ cases.

$$V_T = \Delta V_{T0positive}(V_{OVpositive}) \left(1 - e^{-\left(\frac{t}{\beta_{positive}(V_{OVpositive})}\right)}\right) + \Delta V_{T0negative}(V_{OVnegative}) \left(1 - e^{-\left(\frac{t}{\beta_{negative}(V_{OVnegative})}\right)}\right)$$

The extracted $\Delta V_{T0}$ and $\tau$ for various conditions are shown in Figure 5. The $\tau$, $\Delta V_{T0}$, and $\beta$ functions for every physical and electrical stress condition are summarized in Table 1. Reflecting the repeated stress/recovery in AC bias, a real-time $\Delta V_T$ was successfully applied in the inverter simulation. In detail, each function presented in Table 1 was entered into the $V_T$ parameters in the analytical I-V model of Verilog-A [30]. After configuring an IGZO NMOS-only inverter in HSPICE, the SEF model and the extracted parameters were used for both device simulation and transient AC simulation.

![Figure 5](image-url)

**Figure 5.** (a) Extracted $\Delta V_{T0}$ and (b) $\tau$ for load transistors in different electrical and physical stress conditions. (c) Extracted $\Delta V_{T0}$ and (d) $\tau$ for driver transistors in different electrical and physical stress conditions.

The measured values and simulation results of the load/driver transistors in a flat condition are shown in Figure 6a,b. The measured values and simulation results of voltage transfer curves (VTC) of a flat inverter are shown in Figure 6c. Similarly, the measured values and simulation results of the transistor and inverter in the bending condition are shown in Figure 6d–f. As shown in these figures, it was demonstrated that the simulation results fit very well with the measured values.
Table 1. Extracted parameters for compact SPICE modeling.

| Bending Condition | Bias Condition      | $\tau$ (s)        | $\Delta V_{Tq}$ (V) | $\beta$ |
|-------------------|---------------------|-------------------|---------------------|---------|
| Flat              | Driver positive stress | $4 \times 10^2 e^{-\frac{V}{V_{ov}}} \times 1.8 \times 10^{-1} e^{\frac{V}{V_{ov}}}$ | 0.2     |
|                   | Driver negative stress | $2.5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 4.8 \times 10^{-2} e^{\frac{V}{V_{ov}}}$ | 0.3     |
|                   | Driver recovery      | $3 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 1.7 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.2     |
|                   | Load positive stress | $1.4 \times 10^3 e^{-\frac{V}{V_{ov}}} \times 2.2 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.45    |
|                   | Load negative stress | $4.5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 0.12 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.3     |
|                   | Load recovery        | $5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 1.6 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.6     |
| Bending           | Driver positive stress | $1.5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 3.0 \times 10^{-1} e^{\frac{V}{V_{ov}}}$ | 0.2     |
|                   | Driver negative stress | $1.6 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 5.5 \times 10^{-2} e^{\frac{V}{V_{ov}}}$ | 0.3     |
|                   | Driver recovery      | $9 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 2.3 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.2     |
|                   | Load positive stress | $3 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 3.5 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.45    |
|                   | Load negative stress | $4.5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 0.003 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.12    |
|                   | Load recovery        | $5 \times 10^4 e^{-\frac{V}{V_{ov}}} \times 4.5 \times 10^1 e^{\frac{V}{V_{ov}}}$ | 0.5     |

Figure 6. Measured values and simulation results of (a) a load transistor, (b) a driver transistor, and (c) a voltage transfer curve (VTC) of an inverter in a flat condition. Similar results for (d) a bending load transistor, (e) a bending driver transistor, and (f) a VTC of a bending inverter.
3.3. Inverter AC Driving Simulation

Inverter AC driving simulation was performed by applying the DC stress-based positive and negative SEF model. The detailed AC driving condition was as follows: 3 V to 7 V range of $V_{OV} = (V_{in} - V_T)$, a duty of 50%, cycle of 10 ms or 20 ms, and toggle number of up to 10,000 times. The measured values and simulation results when $V_{OV}$ was 3 V or 5 V in a flat inverter are shown in Figure 7a–d. Similarly, the measured values and simulation results when $V_{OV}$ was 3 V or 7 V under the bending condition are shown in Figure 7e–h. In this simulation, the initial curve was matched with the measurement data, followed by a long-term simulation of 10,000-toggle. The degree of device/circuit deterioration is relatively small in AC driving because the bias time under which the device is stressed is 50% shorter, as compared with DC bias. It can be seen that the proposed compact modeling reflected the inverter’s physical and electrical stress effects well, as the matching degree between the measured value and the simulation result was high. We expect that the proposed reliability-aware SPICE simulation will help predict the circuit operation of flexible a-IGZO TFTs.

![Figure 7. Measured values and simulation results for flat inverters when (a) $V_{OV} = 3$ V and toggle number = 10, (b) $V_{OV} = 3$ V and toggle number = 10,000, (c) $V_{OV} = 5$ V and toggle number = 10, (d) $V_{OV} = 5$ V and toggle number = 10,000. Similar results for bending inverters when (e) $V_{OV} = 3$ V and toggle number = 10, (f) $V_{OV} = 3$ V and toggle number = 10,000, (g) $V_{OV} = 7$ V and toggle number = 10, and (h) $V_{OV} = 7$ V and toggle number = 10,000.](image)

4. Conclusions

In this study, both DC and AC bias-induced instability characteristics of flexible a-IGZO transistors and inverters were analyzed under electrical and mechanical stress. In particular, the electron trapping and hydrogen migration mechanisms that can occur in the IGZO transistors were analyzed and modeled under PBS/CS stress conditions. In this compact modeling, simulation parameters were extracted from both positive and negative $\Delta V_T$ by applying the SEF model. When performing DC and AC simulation by loading the extracted parameter in HSPICE, real-time dependent $\Delta V_T$ was successfully reflected, showing a high consistency of measurement values and simulation results.

The proposed method enables a reliability-aware circuit simulation so that the operation of the flexible IGZO transistor and circuit can be predicted with high accuracy.
Future studies with various operating conditions, such as different duty, voltage, and toggle numbers, will bring more accurate predictions of the flexible IGZO circuit operation.

**Author Contributions:** Conceptualization, J.-H.K., Y.S., D.-W.P. and D.H.K.; methodology, J.-H.K., Y.S.; validation, J.-H.K., Y.S., J.T.J., S.P., D.K., J.P., M.H. and C.K.; writing—original draft preparation, J.-H.K., Y.S., D.-W.P. and D.H.K.; writing—review and editing, J.-H.K., Y.S., D.-W.P. and D.H.K.; supervision, D.-W.P. and D.H.K.; project administration, D.-W.P. and D.H.K.; funding acquisition, M.H., C.K., D.-W.P. and D.H.K. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (MSIT) of Korea under Grant (2016R1A5A1012966 and 2020R1A2B5B01001979). D. Park and M. Han acknowledge support from the Basic Study and Interdisciplinary R&D Foundation Fund of the University of Seoul (2019).

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** The raw/processed data required to reproduce these findings will be shared upon request from the corresponding author.

**Acknowledgments:** The CAD software was supported by SILVACO and IDEC.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Kamiya, T.; Nomura, K.; Hosono, H. Present status of amorphous In–Ga–Zn–O thin-film transistors. *Sci. Technol. Adv. Mater.* 2010, 11, 1–23. [CrossRef]
2. Kamiya, T.; Hiramatsu, H.; Nomura, K.; Hosono, H. Device applications of transparent oxide semiconductors: Excitonic blue LED and transparent flexible TFT. *J. Electroceram.* 2006, 17, 267–275. [CrossRef]
3. Lin, C.-L.; Chang, W.-Y.; Hung, C.-C. Compensating Pixel Circuit Driving AMOLED Display With a-IGZO TFTs. *IEEE Electron Device Lett.* 2013, 34, 1166–1168. [CrossRef]
4. Nomura, K.; Takagi, A.; Kamiya, T.; Ohta, H.; Hirano, M.; Hosono, H. Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film Transistors. *Jpn. J. Appl. Phys.* 2006, 45, 4303–4308. [CrossRef]
5. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* 2004, 432, 488–492. [CrossRef] [PubMed]
6. Lee, C.-Y.; Chang, C.; Shih, W.-P.; Dai, C.-L. Wet etching rates of InGaZnO for fabrication of transparent thin-film transistors on plastic substrates. *Thin Solid Films* 2010, 518, 3992–3998. [CrossRef]
7. Münzenrieder, N.; Pettì, L.; Zysset, C.; Salvatore, G.A.; Kinkeldei, T.; Perumal, C.; Carta, C.; Ellinger, F.; Tröster, G. Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm. In Proceedings of the 2012 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012; pp. 96–99.
8. Münzenrieder, N.; Zysset, C.; Pettì, L.; Kinkeldei, T.; Salvatore, G.A.; Tröster, G. Flexible double gate a-IGZO TFT fabricated on free standing polyimide foil. *Solid-State Electron.* 2013, 84, 198–204. [CrossRef]
9. Kim, J.-H.; Jang, J.T.; Bae, J.-H.; Choi, S.-J.; Kim, D.; Kim, C.; Kim, Y.; Kim, D.H. Analysis of threshold voltage shift for full VGS/VDS/Oxygen-content span under positive bias stress in bottom-gate amorphous InGaZnO thin-film transistors. *Micromachines* 2021, 12, 327. [CrossRef]
10. Takahashi, T.; Miyanaga, R.; Fuji, M.N.; Tanaka, J.; Takechi, K.; Tanabe, H.; Bermudo, J.P.; Ishikawa, Y.; Uraoka, Y. Hot carrier effects in InGaZnO thin-film transistor. *Appl. Phys. Express* 2019, 12, 094007. [CrossRef]
11. Kim, J.; Choi, S.; Jang, J.; Jang, J.T.; Kim, J.; Choi, S.-J.; Kim, D.M.; Kim, D.H. Analysis of instability mechanism under simultaneous positive gate and drain bias stress in self-aligned top- gate Amorphous Indium-Zinc-Oxide Thin-Film. *J. Semicond. Technol. Sci.* 2015, 15, 526–531. [CrossRef]
12. Abe, K.; Takahashi, K.; Sato, A.; Kumomi, H.; Nomura, K.; Kamiya, T.; Kanicki, J.; Hosono, H. Amorphous In–Ga–Zn–O Dual-Gate TFTs: Current-voltage characteristics and electrical stress instabilities. *IEEE Trans. Electron Devices* 2012, 59, 1336–1339. [CrossRef]
13. On, N.; Kim, K.; Lee, S.; Kim, E.H.; Lim, J.H.; Jeong, I.K. Hot carrier effect in self-aligned in–Ga–Zn–O Thin-film transistors with short channel length. *IEEE Trans. Electron Devices* 2020, 67, 5544–5551. [CrossRef]
14. Choi, S.; Kim, H.; Jo, C.; Kim, H.-S.; Choi, S.-J.; Kim, D.M.; Park, J.; Kim, D.H. The Effect of gate and drain fields on the competition between donor-like state creation and local electron trapping in In–Ga–Zn–O thin film transistors under current stress. *IEEE Electron Device Lett.* 2015, 36, 1336–1339. [CrossRef]
15. Lin, D.; Su, W.-C.; Chang, T.-C.; Chen, H.-C.; Tu, Y.-F.; Zhou, K.-J.; Hung, Y.-H.; Yang, J.; Lu, I.-N.; Tsai, T.-M.; et al. Degradation Behavior of Etch-Stopper-Layer Structured a-InGaZnO Thin-Film Transistors under Hot-Carrier Stress and Illumination. IEEE Trans. Electron Devices 2021, 68, 556–559. [CrossRef]

16. Yen, C.-C.; Tai, A.-H.; Liu, Y.-U.; Chen, T.-L.; Chou, C.-H.; Liu, C.W. Oxygen-Related Reliability of Amorphous InGaZnO Thin Film Transistors. IEEE J. Electron Devices Soc. 2020, 8, 540–544. [CrossRef]

17. Lee, D.; Jeong, C.-Y.; Song, S.-H.; Xiao-Shi, J.; Kim, J.I.; Lee, J.-H.; Kwon, H.-I. Asymmetrical degradation behaviors in amorphous InGaZnO thin-film transistors under various gate and drain bias stresses. J. Vac. Sci. Technol. B 2014, 33, 011202. [CrossRef]

18. Chang, Y.-H.; Yu, M.-J.; Lin, R.-P.; Hsu, C.-P.; Hou, T.-H. Abnormal positive bias stress instability of In-Ga-Zn-O thin-film transistors with low-temperature Al2O3 gate dielectric. Appl. Phys. Lett. 2016, 108, 033502. [CrossRef]

19. Oh, S.-I.; Woo, J.-M.; Jang, J.-H. Comparative Studies of Long-Term Ambiance and Electrical Stress Stability of IGZO Thin-Film Transistors Annealed Under Hydrogen and Nitrogen Ambiance. IEEE Trans. Electron Devices 2016, 63, 1910–1915. [CrossRef]

20. Noh, H.-K.; Park, J.-S.; Chang, K.J. Effect of hydrogen incorporation on the negative bias illumination stress instability in amorphous In-Ga-Zn-O thin-film-transistors. J. Appl. Phys. 2013, 113, 063712. [CrossRef]

21. Kang, Y.; Ahn, B.D.; Song, J.H.; Mo, Y.G.; Nham, H.-H.; Han, S.; Jeong, J.K. Hydrogen Bistability as the Origin of Phoro-Bias-Thermal Instabilities in Amorphous Oxide Semiconductors. Adv. Electron. Mater. 2015, 1, 1400006. [CrossRef]

22. Jeon, Y.W.; Hur, I.; Kim, Y.; Bae, M.; Jung, H.K.; Kong, D.; Kim, W.; Kim, J.; Jang, J.; Kim, D.M.; et al. Physics-Based SPICE Model of a-InGaZnO Thin-Film Transistor Using Verilog-A. J. Semicond. Technol. Sci. 2011, 11, 153–161. [CrossRef]