Characterization and modeling of the reverse behavior of a vertical power MOSFET

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Abstract
In this work, the static and dynamic reverse behavior of a vertical structure Si power MOSFET is characterized. The BSIM3 model is adopted and extended to describe the channel current considering asymmetric channel behavior caused by the vertical structure. The diffusion capacitance of the body diode is analyzed, which is critical for the reverse recovery behavior but currently not precisely defined in power MOSFET models. To accurately depict the reverse recovery current, two diode models with diffusion capacitance definitions based on the solution of different methods are built into the MOSFET model and their performance is compared. The result shows that to describe the reverse recovery of the body diode for smaller current range simulation, the stored charge model is recommended, but when scalability is necessary, the carrier distribution model is more suitable.

KEYWORDS
power MOSFET, characterization, modeling, reverse recovery

1 | INTRODUCTION

The vertical power MOSFET is commonly used in resonant power supplies and inverter circuits. In these applications, current can flow in reverse direction through the transistor during freewheeling. The reverse current can flow through the body diode of the power MOSFET, and it is also possible to induce higher drain current via the channel at lower negative drain bias voltages by applying a gate bias.\(^1\) This operation is referred to as the synchronous rectification mode, because the MOSFET is behaving like a rectifier by selectively applying the gate bias when the drain to source voltage is negative during circuit operation.

The body diode of the MOSFETs can be relied upon for normal circuit operation, but it also exhibits considerable loss, because of the simultaneous presence of high current and voltage during reverse recovery, that is, while it switches from the forward-biased state to the reverse-biased state. Moreover, the peak reverse recovery current also flows through the power transistor controlling the switching event, which also increases the power loss in the transistor.

However, currently these reverse behaviors are not precisely described in the power MOSFETs models provided by the device vendors, in which the MOSFET channel is simply symmetrically defined for forward and reverse operation and the body diode is defined using the Spice diode model. The inaccurate model definition may cause that the exact power loss and some EMI problems cannot be correctly estimated in the simulation. Therefore, a precise model to describe the reverse conducting mode of the power MOSFET is quite necessary to estimate the behavior of the device in switching mode application.

2 | DEVICE CHARACTERIZATION

2.1 | Static reverse behavior

In most of the conventional power MOSFET models the channels are defined as symmetric for forward and reverse current, that is, in the simulation before gate-source voltage \(V_{gs}\) arrives at the threshold voltage, there is only current going through the body-diode in the reverse case. However, it is observed that the vertical structure can also cause an asymmetric channel behavior. In the measurement of the reverse static current with Keysight B1505A, it is observed that before the reverse voltage \(V_{ds}\) arrives at the threshold voltage of the diode and before the gate voltage \(V_{gs}\) arrives at the forward threshold voltage of the channel, there exists a high current going through the device.

Figure 1 shows the waveform of the measurement in B1505A when \(V_{gs}\) is set at different voltages. In Figure 1A, \(V_{gs}\) is set at negative value \(-2\) V and in the reverse case, that
is, $V_{ds}$ is negative, we check here the waveform of $V_{gd}$ instead of $V_{gs}$. It shows that the reverse current going through the device is not influenced by the changing $V_{gd}$, as the current in this case only flows through the body diode. Figure 1C shows the waveform when $V_{gs}$ is set at 6 V. In this case the channel is in the strong inversion state and in the waveform $I_d$ appears an additional increase with the increasing $V_{gd}$ and the voltage across the device $V_{ds}$ begins to decrease, because of the onset of channel conduction.

Figure 1B displays the waveform when $V_{gs}$ is set at 2 V. It is observed that when $V_{gd}$ increased to some certain value, the voltage across the device $V_{ds}$ begins to decrease and $I_d$ appears an additional increase. It is very similar as the waveform shown in Figure 1C, which means that with negative $V_{ds}$, the channel is already turned to on-state, although the $V_{gd}$ is much lower than the threshold voltage in the forward $V_{ds}$ bias case.

This asymmetric channel behavior is caused by the shorted source and bulk structure of the vertical power MOSFETs. The channel can “open up” either on the source side or on the drain side, depending on the local potential under the gate. But in the reverse operation, the relatively higher potential on the source terminal can cause a potential influence through bulk toward gate, which cause the decrease of threshold voltage. However, to the best of the authors’ knowledge, this phenomenon is currently not described in any vendor models for power MOSFETs.

In this work, the body effect parameters defined in BSIM3 are used to describe the asymmetric channel behavior and details are explained in Section 3. The measurement and the simulation results of the IV characteristic is shown in Section 4.

### 2.2 Transient reverse behavior

For transient performance, a double pulse test (DPT) is carried out to characterize the process of reverse recovery of the body diode. Due to the fast current change during the transient time, the Fraunhofer IZM inductive current shunt is used as the current sensor to measure the reverse recovery current. The sketch of the custom DPT set up is shown in Figure 2A, and the waveform of the double pulse test is shown in Figure 2B. The populated PCB for the custom DPT measurement is shown in Figure 3.

The inductor L acts as a current source when the low-side device is turned off at some certain current level as shown in Figure 2B. During the off-time of the low-side device, the constant current flows through the body diode of the high-side device. When the low-side device is switched on and the current begins to flow through the low-side device, the body diode of the high-side device is reverse biased. During this switching process there appears a large current flowing through the diode in the reverse direction. This transient is characterized as reverse recovery of the body diode. The reverse recovery current can be directly measured with the high-side current sensor as shown in Figure 2A or obtained from the low-side current sensor plus the inductor current. Both methods are used in this work and the measurement results of these two methods are consistent.

The reverse recovery is caused by the stored minority carriers, which come from both the depletion capacitance and diffusion capacitance of the junction. The depletion capacitance accounts for most of the junction capacitance when the junction is reverse biased, that is, the MOSFET is forward biased. When the junction is forward biased, there is an additional contribution to junction capacitance from the rearrangement of the stored charges in the neutral region, which is the diffusion capacitance. These two capacitances together induce the reverse recovery phenomenon.

The behavior of the two capacitances is separately analyzed. As the depletion capacitance dominates the forward $C_{ds}$ of a vertical MOSFET, the depletion capacitance is characterized with forward bias in a 2-Port S-parameter measurement with forward $V_{ds}$ bias.

The conventional definition in the SPICE model for diode capacitance is as:

$$C_D = \begin{cases} \frac{C_{J0}}{(1-V_{bi}/V_{bi})^{M_j}} & V_D < F_C \cdot V_{bi} \\ \frac{C_{J0}}{(1-F_C)^{M_J}} \left[ 1 - F_C \cdot \left(1 + M_J \right) + M_J \cdot \frac{V_D}{V_{bi}} \right] & \text{else} \end{cases}$$

where $V_D$ is the voltage drop across the diode, $F_C$ is the forward-bias depletion capacitance coefficient, $C_{J0}$ is the zero-bias p-n capacitance, $M_j$ is the junction grading

![Figure 1](https://example.com/figure1.png)  
Reverse current measurement waveform in B1505A (A) $V_{gs}$ is set at $-2$ V (B) $V_{gs}$ is set at 2 V, (C) $V_{gs}$ is set at 6 V [Color figure can be viewed at wileyonlinelibrary.com]
coefficient and $V_{bi}$ is the junction built-in potential. With this definition, the reverse recovery at relatively low current level can be fitted; however, as shown in Figure 4, when the current level becomes high, an obvious deviation appears between the simulation and measurement of the reverse recovery, as in the high injection case the Equation 1 is not able to describe the diffusion capacitance correctly.

Therefore, to precisely describe the reverse recovery behavior a more accurate model that can correctly predict the charge behavior during the transient especially for the diffusion capacitance is required.

The oscillation at the end of the reverse recovery is not only caused by the intrinsic parasitics of the device but also largely influenced by the parasitic coming from the measurement setup. Therefore, an EM simulation for the double pulse test PCB board is also carried out to figure out the parasitic influence coming from the measurement setup. The ANSYS Q3D is used to analyze the parasitic inductance of the PCB board. Figure 5 shows the current loop in the DPT setup. The EM simulation result can be completed as a Spice model describing the parasitic influence between each node contacting all the components in the loop. This model is also inserted into the DPT simulation to consider the parasitic influence coming from the PCB setup.

### 3 | MODEL DESCRIPTION

In vertical power MOSFETs the source electrode is connected to the P base region to suppress the parasitic N-P-N transistor. Consequently, the P- base layer, the N- drift layer, and the N+ substrate form a PiN diode between the drain and source electrodes, as shown in Figure 6, which acts as an intrinsic body diode. In our previous work, an extended BSIM3v3 model is successfully adopted to describe the forward DC-IV characteristics of the vertical power MOSFET.6

#### 3.1 | Reverse IV model

Considering the structure of vertical power MOSFETs, in which bulk and source are shorted, all the parameters related with $V_{bs}$ are deactivated in the previous modeling of forward DC-IV. However, as explained in the Section 2.1 the shorted bulk and source caused a potential effect to the channel similar as the body effect, which influences the channel asymmetrical behavior in the reverse case.
Therefore, the body effect parameters including $K_1$ and $K_2$ defined in BSIM3 model as shown in Equation 2 are activated to describe the asymmetrical reverse channel behavior.

$$V_{th} = V_{th0} + K_1 \left( \sqrt{\Phi_S} - V_{bs} - \sqrt{\Phi_S} \right) - K_2 V_{bs} \quad (2)$$

When $V_{ds}$ turned to be negative, the $V_{bs}$ is replaced by $V_{bd}$ in the BSIM3 expression, and the influence coming from the relatively higher potential bulk is introduced to the definition of threshold voltage.

### 3.2 Transient model

To describe the reverse recovery of power diodes, several models have been proposed based on lumped-charge theory or ambipolar diffusion equation and solved by different methods. However, there is still few work describing the plasma caused reverse recovery of the body diode in power MOSFETs.

In this work, two different methods based on different theories are chosen to be implemented and their performance is compared. These two models are the dynamic stored charge model and the carrier distribution profile model.

#### 3.2.1 Stored charged model

The dynamic stored charged model is defined based on the fundamental charge control equation for P-N junction, and the excess charge $Q$ definition is modified as a function of its rate of change to describe its dynamic behavior. The charge equation is shown in Equation 3.

$$Q = \tau \left[ I_d - \nu \frac{dQ}{dt} \right] \quad (3)$$

In this equation, $I_d$ is the diode current, $\tau$ is the excess minority lifetime, $\nu$ is the parameter to describe the viscosity of the minority carrier charge, which is related to the geometrical width of the N-drift region.

In this model all the stored charge is considered as a lumped unit. Therefore, it is relatively simple as there are only two parameters involved in describing the charge changing transient.

#### 3.2.2 Charge distribution model

In the stored charge model the excess charge is defined as lumped charge without spatial distribution. To describe the behavior of the charge stored in the drift region under transient operation, with both time and position, a more physics-based model that is determined by the solution of
the ambipolar diffusion equation (ADE) Equation 4 through the finite difference method (FDM)\textsuperscript{10} is tried to analyze the carrier concentration distribution during reverse recovery.

\[
\frac{\partial p}{\partial t} = D_a \frac{\partial^2 p}{\partial x^2} - \frac{p}{\tau_{HL}} \tag{4}
\]

The \( p \) in Equation 4 is the carrier concentration, the \( D_a \) is the ambipolar diffusion coefficient, \( x \) is the length of the point from the P-N junction, and \( \tau_{HL} \) is the high level lifetime of free carriers.

In the FDM solution, the whole drift region is divided into \( N \) elements of unit length \( \Delta x \). Exploiting the central difference approximations of the partial derivatives at each \( i^{th} \) node as in Equations 5 and 6, the ADE can be expressed as in Equation 7

\[
\frac{\partial p}{\partial t} \bigg|_{i} = \frac{p_{i+1} - p_{i-1}}{2\Delta x} \tag{5}
\]

\[
\frac{\partial^2 p}{\partial x^2} \bigg|_{i} = \frac{p_{i+1} - 2p_i + p_{i-1}}{\Delta x^2} \tag{6}
\]

With the boundary current, a symmetric system of \( N + 1 \) ordinary differential equations (ODEs) is obtained as Equation 8.

\[
[C] \frac{\partial p}{\partial t} + [G] [p] + [f] = 0 \tag{8}
\]

This ODE set can be implemented through a nonlinear RC network, and the solved voltage drop at each node of the network represents the carrier concentration at certain position \( x \). The RC network can be built as an auxiliary circuit in the Spice model, and in the Verilog-A model the ODEs can directly built as equations and solved by the simulator.

This model provides the carrier dynamic behavior in the drift region during the switching transient. The obtained carrier concentration is related to the body diode voltage and ohmic law under forward bias and Poisson equation for reverse operation.\textsuperscript{10} Then a current controlled voltage source is built as the equivalent circuit for the body diode.

\section*{4 | PARAMETER EXTRACTION}

The extended model is implemented using Verilog-A and simulated in the Keysight Advanced Design System (ADS). According to the result in our previous work,\textsuperscript{6} the parameters for the channel are extracted based on the measurement of the forward output characteristics. Figure 7 shows the parameter extraction result.

The simulation result of the extended BSIM3 model for the reverse IV characteristic compared with the measurement is presented in Figure 8. It is observed that, when the channel is defined symmetric for forward and reverse current, the bulk potential effect that cause the change of the threshold voltage cannot be described, as shown in Figure 8A. When the body effect parameters \( K_1 \) and \( K_2 \) defined in Equation 2 are activated and the channel is defined as asymmetric, the reverse output characteristic is able to be described...
accurately, as shown in Figure 8B. As $K_1$ also influence the forward channel IV expression through bulk charge effect, $K_1$ is set as 1 and the asymmetric threshold voltage is mainly described by $K_2$ which is set to 3.6.

For the reverse recovery models, the parameters of the stored charge model and the charge distribution model are extracted based on the measurement at 3.2A, 9.8A, 18A, and 21A forward current. The parameter extraction results are compared and shown in Figure 9. According to the parameter extraction, the parameter for carrier lifetime $tau$ in both models are set to around 80 ns, which is much smaller than the carrier lifetime value in Si devices, and it is inferred that some lifetime killers are added to the drift region of the device for high switching speed.
5 | CONCLUSIONS

This article presents the characterization and modeling of the static and transient reverse behavior of a vertical power MOSFET. A double pulse test measurement is carried out to analyze the reverse recovery behavior of the device body diode. The channel current model is built based on the BSIM3 expression, and two charge diffusion capacitance models used to describe the body diode are presented and compared. The parameters are extracted based on the characterization result. The simulation results show that the proposed model can depict the reverse behavior of the device precisely, and the two transient model for body diode reverse recovery are separately recommended to use under different simulation requirements.

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