Si and SiGe Nanowire for Micro-Thermoelectric Generator: A Review of the Current State of the Art

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In our environment, the large availability of wasted heat has motivated the search for methods to harvest heat. As a reliable way to supply energy, SiGe has been used for thermoelectric generators (TEGs) in space missions for decades. Recently, micro-thermoelectric generators (µTEG) have been shown to be a promising way to supply energy for the Internet of Things (IoT) by using daily waste heat. Combining the predominant CMOS compatibility with high electric conductivity and low thermal conductivity performance, Si nanowire and SiGe nanowire have been a candidate for µTEG. This review gives a comprehensive introduction of the Si, SiGe nanowires, and their possibility for µTEG. The basic thermoelectric principles, materials, structures, fabrication, measurements, and applications are discussed in depth.

Keywords: Si, SiGe, nanowire, thermoelectric generator, ZT, heat

INTRODUCTION

Global warming has become a significant problem in today’s world, and environmental awareness is stronger than it ever has been before (Moss et al., 2010). Researchers have long been focused on locating new carbon-free and environmentally friendly energy alternatives (Radousky and Liang, 2012). The waste heat from engines was considered to be a low-grade energy in the past century but is now seen as a fantastic energy source for the near future. Most of the energy that we consume is wasted in the form of heat. Thermal energy scavenging or harvesting, achieved by a thermoelectric generator (TEG), has the strength of stable components, high reliability, long service life, no maintenance, and direct energy conversion (Yan et al., 2018). Because of this, TEGs have become the most promising device with core materials for harvesting wasted heat, as a result of a temperature difference.

The first generation of TEGs was manufactured from semiconductors e.g., bismuth telluride (Bi2Te3), lead telluride (PbTe), and silicon germanium (SiGe). Except for Bi2Te3, those materials have been used in deep-space missions, like NASA’s Voyager, Pioneer, Ulysses, and Cassini space ships using radioisotope thermoelectric generators (RTGs) (June and Zakrajsek, 2017). Radioisotope thermoelectric generators can supply enough power for electronic devices in space probes and satellites using the thermal energy from nuclear fission (Yang and Caillat, 2011). Some of those devices have operated for more than 30 years, showing their reliability and efficiency. One of the main drawbacks of TEG is the low efficiency compared with other types of power generators. This low efficiency problem has made it difficult to use TEGs for an ecological niche in the past decades.
In recent years, different research groups have fabricated micro-thermoelectric generators (μ-TEGs) which are much smaller than the traditional TEGs (Gadea et al., 2018b; Noyana et al., 2019). Micro-thermoelectric generators fabrication apply the NW techniques commonly used in CMOS technology or microelectromechanical systems (MEMS) (Radamson et al., 2017, 2019).

This also reduces the cost by using micro-patterning which can be integrated with other microfabricated devices (Gadea et al., 2018a). Over the past decades, figure-of-merit (ZT) was increased slowly with existing materials and structures, with the realized value in the vicinity of 1, thus little attention has been paid to the thermoelectric (TE) field. Though slowly, the TE industry has developed steadily by finding its niches for space exploration and laboratory and medical applications, where the availability and reliability of energy is more overwhelming than the cost and efficiency (Radamson et al., 2019).

Recently, scientists have experimented with many nanostructured materials to make a high performance μ-TEG. Besides the elementary substances like bismuth (Kim et al., 2015) and silicon (Li et al., 2003b), a large number of composite materials, including clathrates (Kleinke, 2010; Takabatake et al., 2014), skutterudites (Nolas et al., 1999; Rogl et al., 2014), metal oxides (Koumoto et al., 2010; Ishibe et al., 2018), tellurides (Heremans et al., 2008; Poudel et al., 2008; Goldsmid, 2014), and intermetallics (Zeyer et al., 2016), have been investigated for their TE performance. A key issue for this TE research is to find a high-performance TE material with low thermal conductivity and high electric conductivity. More possible solutions have been put forward and verified; one of the most promising materials is silicon. Silicon and its Group IV binary or ternary alloys have potential to be used to form a TEG in commercial application for several reasons. They would be Si-based CMOS technology compatible, the source of the Group IV materials is much cheaper than the traditional TE materials, and rather than poisonous materials like Bi₂Te₃, the Group IV materials are environment-friendly and safe for civil use.

However, despite its high thermal conductivity, Si bulk is unideal for TEG. Because of the popularization of Si electronics, research on Si TE devices are expanding (Ni et al., 1995). Two promising roads have been researched to improve the TE performance. The former is the alloying effect, which introduces other extended group IV materials with the same lattice structure, the typical one being SiGe. Compared to pristine Si, the experiment results show a distinct decrease in thermal conductivity. Interest has also been given to nanostructures, with quantum confinement applied. The development in nanoengineering makes it possible for nanostructures in Si-based TEG. The low-dimensional structures exhibit a significantly reduced lattice thermal conductivity compared to their bulk counterparts owing to the enhanced phonon scattering at the interfaces, and nanowires (NWs) have been proven with high ZT (Dresselhaus et al., 2007).

The two methods could be combined fabricate TEG with Si and SiGe NWs. Specifically, the Si and SiGe NWs have exhibited higher TE performances related to their bulk crystal counterparts both in experimental and theoretical studies since the early 1990s (Li et al., 2003a,b; Hochbaum et al., 2008). Different explorations of the elements that affect TE have been put forward by several groups like alloy, surface roughness, doping, etc., Silicon (Si) NWs exhibited a ZT of 0.6 at 300 K (∼0.01 for bulk Si) without degeneration of the Seebeck coefficient and electrical conductivity (Hochbaum et al., 2008). Moreover, the thermal conductivity is further reduced in SiGe NWs (Li et al., 2003a). The longer SiGe NW arrays gives a higher Seebeck coefficient and the thermal conductivity decreases with increasing Ge content and NW length (Li et al., 2012).

Nowadays, with further research, Si-based CMOS technology shows its potential to make a high-performance μ-TEG (Gadea et al., 2018b). Meanwhile, the scaling down in the fabrication of CMOS makes it possible to grow extremely thin Si and SiGe NWs. In general, two approaches have been adopted for the fabrication of different NWs: top-down or bottom-up (Akbari-Saatlu et al., 2020). In most of the research we have investigated, the bottom-up approach is preferred with the popular vapor-liquid-solid chemical vapor deposition (VLS-CVD) used (Calaza et al., 2015); others are achieved using the top-down approach with an etching process, for example, metal-assisted wet chemical etching (MaCE) or reactive ion etching (RIE) (Wolffsteller et al., 2010; Sandu et al., 2019; Radamson et al., 2020). Some relevant measurements of the TE properties have also been developed during the study of NWs (Rojo et al., 2013; Borup et al., 2015; Liu et al., 2016). The typical methods for the Seebeck coefficient measure are mesoscopic or microfabricated suspended devices and thermocouples. The microfabricated suspended devices have also been used in the measurement of thermal conductivity. The other methods commonly used are the 3ω methods and scanning thermal microscope (SThM) technique (Grauby et al., 2013). Micro-thermoelectric generators has a great variety of potential applications, including business electronics, bio-medical devices, and internet of things (IoT) devices. Internet of things devices are the most promising prospect for the μ-TEG with a steady μW-mW level energy supply (Haras and Skotnicki, 2018; Zhang et al., 2018).

In this review article, we examine the past and existing research into TEG and μ-TEG, especially based on the Si and SiGe NWs. The basic TE principles and theories are introduced and the factors that may influence the TE performance of Si and SiGe NWs are discussed. The superiority of the group IV material-based NWs as TE materials are detailed with feasible structures while their fabrication methods and TE measurements are also reviewed. Finally, the existing Si and SiGe NW μ-TEGs are discussed for their potential applications and the feasible applications are illustrated.

THEORY AND PRINCIPLE

Based on the three fundamental TE principles, the Seebeck effect, the Peltier effect, and the Thomson effect, TE devices such as TEGs and TE coolers have been fabricated (Figure 1). To detail the mechanisms in TEGs fabricated using materials like Si and other group IV NWs, researchers have proposed some theories based on the semiconductor physics model to explain it.
**ZT and Energy Conversion Efficiency**

To measure the TE energy conversion efficiency of TEG, researchers adopted the parameter called dimensionless figure of merit, denoted as ZT, which is defined as (Rowe, 1995):

\[ ZT = \frac{\sigma S^2}{\kappa} T \]

where \( S \) is the Seebeck coefficient, \( \sigma \) the electrical conductivity, \( T \) the operating temperature, and \( \kappa \) the thermal conductivity. In some cases, when \( \kappa \) is unavailable for ZT calculation, the parameter which is defined as TE power factor:

\[ PF = \sigma S^2 \]

can be an indicator (Rowe, 1995). To improve the TE property of TEG, two approaches have been considered: (1) improve the power factor \( S^2/\sigma \), (2) decrease the thermal conductivity \( \kappa \). Since electron scattering in a semiconductor is negligible, interest has been focusing on the method to lower the thermal conductivity.

For the conventional TEG, ZT is defined as (Rowe, 1995):

\[ ZT = \frac{(S_p - S_n)^2 \cdot T}{\left( \sqrt{\frac{\sigma_p}{\sigma_n}} + \sqrt{\frac{\sigma_n}{\sigma_p}} \right)^2} \]

where the subscripts \( p \) and \( n \) denote the P-type and N-type legs, respectively.

The maximum conversion efficiency is defined by (Rowe, 1995):

\[ \eta_{\text{max}} = \eta_0 \cdot \frac{\sqrt{1 + ZT_{\text{avg}}} - 1}{\sqrt{1 + ZT_{\text{avg}}} + \frac{T_c}{T_h}} \]

where \( \eta_0 = (T_h - T_c)/T_h \) is the Carnot ideal cycle efficiency. Here, the \( T_h \) is the hot junction temperature, \( T_c \) for the cold side. \( ZT_{\text{avg}} \) is the average value of ZT from \( T_c \) to \( T_h \). The certain relations between \( T_h, \ ZT_{\text{avg}}, \) and \( \eta \) are shown in Figure 2 (Yu et al., 2019). Like other types of heat power generation, \( \eta \) increases with temperature difference and is confined to the Carnot limit (Gadea et al., 2018a). Conversion efficiency of different types of energy sources for electric generations like geothermal, solar, nuclear, and coal are also presented in Figure 2, which can be a comparison.

The highest ZT has achieved more than 2 for some materials (Kumar et al., 2020), and there are some calculations and models which speculated that there is still potential for ZT. But it is noteworthy that for different temperatures, the ZT varies widely; the most valuable temperature is 300 K, which is the device’s normal operate temperature. For Si, \( ZT = 0.2 \) is achieved at 620 K with the optimized contact in a recent work (Gadea Diez et al., 2020).

**Thermal Conductivity**

Fourier’s law is defined as: \( j = -\kappa \nabla T \), where thermal conductivity \( \kappa \) is the ratio of heat flux \( j \) that passes through unit area per unit time to temperature gradient \( \nabla T \) (Swinkels and Zardo, 2018). In a semiconductor, \( \kappa = \kappa_{\text{ph}} + \kappa_e \) is the sum of two main parts, dominating phonon thermal conductivity and negligible electron thermal conductivity \( \kappa_e \). Phonon thermal conductivity \( \kappa_{\text{ph}} = L_{\text{ph}} v_s C_v/3 \) is related to heating transport through phonons, depending on the phonon’s mean free path of certain materials (MFP, \( L_{\text{ph}} = v_s \tau \) is the phonon mean free path, with \( \tau \) phonon lifetime), sound velocity \( (v_s) \), and heat capacity \( (C_v) \). Electron thermal conductivity is calculated by the Wiedemann-Franz law \( \kappa_e = L \sigma T \) where \( L \approx 2.45 \times 10^{-8} \ V^2 \ K^{-2} \) is the Lorentz constant for degenerately doped silicon (Minnich et al., 2009), representing heat propagation with charged carriers, \( \sigma \) the electrical conductivity, and \( T \) the average temperature between the cold and hot side. Molecular dynamics (MD) and first principle calculation techniques have been used in several studies to calculate the theoretical value of the thermal conductivity of Si.
Phonon Thermal Conductivity

Thermal conductivity is actually related to the lattice thermal conductivity, and it consists of different kinds of phonon scattering. This is caused by defects or dopants with disorganized lattice periodicity; the scatterings reduce the MFP to a large extent. Other particles and quasiparticles, like electrons, can also produce scattering using the energy and momentum exchange. These scattering mechanisms have been formulated by the Matthiessen's rule (Gadea et al., 2018a):

\[
\frac{1}{\tau_{p,i}} = \frac{1}{\tau_{pN,i}} + \frac{1}{\tau_{pR,i}}
\]

\[
\frac{1}{\tau_{pR,i}} = \frac{1}{\tau_{pU,i}} + \frac{1}{\tau_{pA,i}} + \frac{1}{\tau_{pB,i}} + \frac{1}{\tau_{pC,i}} + \frac{1}{\tau_{pE,i}}
\]

In the above formula, the phonon relaxation time is comprised of multiple phonons scattering events including phonon–phonon normal scattering, phonon–phonon Umklapp scattering, phonon alloy scattering, phonon boundary scattering, phonon cluster scattering, and phonon electron scattering (Yi and Yu, 2015).

Mainly, researchers focused on the most important parts like phonon-boundary scattering and phonon alloy scattering. Although phonon boundary scattering is frequency independent, it is mainly influenced by the low frequency phonons with long wavelength (Kim, 2013). Phonon boundary scattering is caused by the grain boundary and it is dominant where the dimension of the structure is much smaller than the phonon MFP. Therefore, the phonon thermal conductivity is strongly depressed and the heat flux through the system is limited by the thermal boundary Kapitza resistance (Cahill et al., 2003). For silicon NW, its phonon mean free path is \(~300\) nm while its electron mean free path is \(~110\) nm with heavy doping (Ju and Goodson, 1999). Considering this, the diameter of a Si NW should be thinner than 300 nm but more than 110 nm. Then the \(\kappa\) will be reduced for that \(\kappa_{ph} = L_{ph}v_{ph}C_v/3\), so the thermal conductivity of a single Si NW decreases when the diameter decreases.

When we discuss the influence of phonon boundary scattering on the \(\kappa\), the surface roughness of the NWs is an important issue. Thermal conductivity reduction caused by surface roughness has been observed in several experimental works (Hochbaum et al., 2008; Kim et al., 2011; Feser et al., 2012; Malhotra and Maldovan, 2016); \(\kappa\) was reported with a value down to few \(W\ m^{-1} K^{-1}\) in NWs with a diameter of several tens of nms, much lower than the bulk Si (\(~150\) \(W\ m^{-1} K^{-1}\)). By theoretical prediction, the \(\kappa\) in Si NWs with a diameter <100 nm was proportional to \((D/\Delta)^2\), where \(D\) was diameter and \(\Delta\) the surface roughness. An analysis shows that the experimental data fits well with the calculation data, indicating the dependence between \(D\) and \(\kappa\) (Figure 3).

Other mechanisms, like point defect scattering in Si\(_{1-x}\)Ge\(_x\) alloy, also result in the reduction of \(\lambda_{ph}\). Figure 3 shows the \(\kappa\) behavior of Si\(_{1-x}\)Ge\(_x\) NWs with Ge concentration \(x\) = 0.004, 0.04, and 0.09. The figure reveals that the alloy scattering is aggravated by the increased Ge content. At the same Ge concentration, the thermal conductivity is decreased with a smaller diameter, which has been confirmed in previous research (Li et al., 2003b). In principle, alloy scattering causes a severe suppression of high-frequency phonons in Si\(_{1-x}\)Ge\(_x\), thus the low frequency phonons became the dominant ones (Xie et al., 2014). Meanwhile, compared with Si NWs, a stronger length dependence, weaker diameter, and surface roughness dependence have been shown to occur in Si\(_{1-x}\)Ge\(_x\) NWs thermal conductivity (Xie et al., 2014).
### Electron Thermal Conductivity

Besides the reduction of phonon thermal conductivity, there is also an alternative approach which is based on tailoring the electronic transport properties. Electron thermal conductivity $\kappa_e = L_0 \sigma T$ depends on the density and mobility of the carriers in $L_0$, and it is strictly related to the electrical conductivity $\sigma$. Electronic thermal conductivity is high in metal materials but much lower in semiconductors due to their different thermal conduction mechanism. It is noteworthy that once the $\kappa_{ph}$ is largely suppressed by effective phonon scatterings in bulk nanostructure, $\kappa_e$ become dominant and the $ZT$ can be simplified to $ZT = S^2 \sigma / \kappa_e T$, making it totally electronic.

Using the electron energy filtering effect, the thermal conduction from the carrier density is reduced, and thus $\kappa_e$ is largely reduced. Meanwhile, the filtering causes a decrease of the Lorenz number, which further reduces the $\kappa_e$ and makes the $\kappa_{ph}$ dominant one (Bahk et al., 2013). The energy filtering effect has been researched in the bulk nanostructured Si, SiGe, and PbTe (Martin et al., 2009; Minnich et al., 2009; Narducci et al., 2015), and it has also been demonstrated in the Si NW (Bennett et al., 2015). The energy filtering is also important for PF, which we will discuss in the next section.

### Power Factor

In addition to reducing thermal conductivity, the enhancement of power factor is another approach for the TE performance improvement. PF = $\sigma S^2$ is related to the electronic transport, and it is better to simultaneously improve both the electrical conductivity and the Seebeck coefficient for the optimal PF (Mehdizadeh Dehkordi et al., 2015). For the optimal TE performance, the ideal doping concentration is between $10^{19}$ and $10^{21}$ cm$^{-3}$, which depends on the electronic band structure.
of materials (Tritt, 2011; Schierning, 2014). The relations between the TE parameters and doping concentration for the alloy Si₉₀Ge₃₀ are shown in Figure 4: $\kappa$, $\sigma$, $S$, and $ZT$ vary with the doping concentration in different tendency (Minnich et al., 2009).

A simulation has studied the optimal power factor in Si NW with different sizes, and the relation of $S$, $\sigma$, and PF vs. the cross-section area (area) and carrier concentration ($n$) are shown in Figure 5 (Shi et al., 2009). The thinner Si NW will have larger $S$ and smaller $\sigma$, and thus slightly increase the PF, and proper carrier concentration is needed for the optimal PF.

The research studies about the TE power factor enhancement are based on the nanostructures of different materials to a great extent (Mehdizadeh Dehkordi et al., 2015); here we only give a brief introduction of the mechanism of electrical conductivity and Seebeck coefficient.

**Electrical Conductivity**

The electrical conductivity is always an important parameter for electronic devices as well as for TE ones. This parameter is mainly dependent on Kelvin temperature and the electronic relaxation time in a material. In principle, the carriers can interact with different scattering centers e.g., impurities or phonons, and the relaxation time may be affected. More specifically, the scattering centers are categorized by ionized and neutral impurities ($I$ and $N$) and deformation potential ($D$) created by phonons. These scatterings mostly occur simultaneously, therefore, the total relaxation time is written by Matthiessen’s rule (Yi and Yu, 2015).

$$\frac{1}{\tau_e} = \frac{1}{\tau_D} + \frac{1}{\tau_I} + \frac{1}{\tau_N}$$

The deformation potential is governed by electronic carriers scattering through the acoustic vibration of atoms in the crystal lattice and intervalley scattering caused by optical phonons (Yi and Yu, 2015). The modulation-doping is remarkable for the ionized impurity scattering which is dominant at a low temperature (Mehdizadeh Dehkordi et al., 2015).

**Seebeck Coefficient**

Based on the Seebeck effect (Figure 1A) found in 1821, Seebeck voltage $V$ is proportional to the temperature difference $\Delta T$ and Seebeck coefficient $S$ (also thermopower) (Gadea et al., 2018a):

$$S = \frac{V}{\Delta T}$$

The Seebeck coefficient for semiconductors is typically on the order of 100 $\mu$V/K (Goktas et al., 2018). Conversely, this process can operate in reverse to make TE cooler (the Peltier effect, Figure 1B). In P-type semiconductors, $S$ is a positive value (negative in N-type semiconductor). In the fabrication of a TEG, both N-type and P-type are applied to achieve a larger potential difference.

For metals and degenerate semiconductors, the Seebeck coefficient is defined as (Snyder and Toberer, 2008):

$$S = \frac{8\pi^2 k_B^2}{9e} m^* T \left( \frac{\pi}{2n} \right)^2$$

where $n$ is the charge carrier concentration, $m^*$ is the effective mass of the charge carrier, $h$ is the Planck’s constant, $k_B$ is the Boltzmann constant, and $e$ is the carrier charge. $S$ is strongly influenced by the charge carrier energy distribution, and in particular it increases when the average difference between the carrier energies and the Fermi energy increases (Pennelli, 2014).

Dopants, defects, and interfaces can act as energy barriers. The caused energy filtering effect will suppress the low energy electrons in the transport, and thus increase the $S$ and PF in a semiconductor (Schierning, 2014). Hicks and Dresselhaus (1993a) have presented a study about the effect of electron quantum confinement on TE properties of NWs. The results show that interfaces cause energy barriers as energy filtering for low energy electrons which are not active in the transport, resulting in an enhancement of PF (Martin et al., 2009). The enhancement of PF in combination with the reduction of the $\kappa$ are the two benefits for quantum dot and quantum well structures where density of electronic states is modified and phonon modes are frozen. The TE properties of quantum dots and quantum wells are both theoretically foreseen (Hicks and Dresselhaus, 1993b) and experimentally demonstrated (Harman et al., 2002).

The longer SiGe NW arrays provide higher $S$ and then $\kappa$ is decreased by increasing Ge content and NW length (Li et al., 2012). A TEG with short planar Si NWs have demonstrated a dramatic enhancement in the TE power density, attributing to the increase in $S$ (Tomita et al., 2018a). This was explained by the enhanced phonon drag effect, since the frequent surface scattering in longer Si NWs will weaken this effect (Figure 6).

**ADVANCED GROUP IV MATERIALS**

Since the electric conductivity of a TEG was decreased as a result of pursuing the high thermal conductivity, the better choice is an ideal material which integrates the opposite properties of low thermal conductivity and high electric conductivity ($\sigma$), with an as high as possible Seebeck coefficient ($S$). Therefore, the concept called phonon glass-electron crystal (PGEC) has been put forward which involves limiting the minimum electron scattering (small electron mean free path), like the crystalline material, and high phonons scattering (large phonon mean free path), like the amorphous material.

Bismuth telluride ($\text{Bi}_2\text{Te}_3$) and its ($\text{Bi}_{1-x}\text{Sb}_x\text{Se}_{1-y}\text{Te}_y$)$_3$ alloy family are the most used TE materials because of their high TE conversion efficiency at room temperature. Also, their easy deposition in thin film makes the module flexible (Siddique et al., 2017). However, the process price of these traditional foundation materials is also an important issue. A review of the material price of the TE is listed as: Lead (Pb $\sim$2.50$/\text{kg}$), Bismuth (Bi $\sim$10.55$/\text{kg}$), Antimony (Sb $\sim$9$/\text{kg}$), Selenium (Se $\sim$24$/\text{kg}$), or Tellurium (Te $\sim$36$/\text{kg}$) (Haras and Skotnicki, 2018). As a comparison, the pristine silicon is much cheaper as a TE material due to the increase in photovoltaic power generation (Si $\sim$1.5$/\text{kg}$). Silicon also has the advantage of being low cost with the CMOS-compatible processing. Furthermore, when counting other recessive and dominant costs, like environment friendliness
Si NWs

With the diamond structure (Fd-3m), silicon conducts heat largely by phonon rather than the charge carrier (electron or hole). At 300 K, thermal conductivity of pure silicon is \( \sim 150 \text{ W m}^{-1} \text{ K}^{-1} \) (Glassbrenner and Slack, 1964). With doping, the thermal conductivity can be further reduced due to phonon impurity scattering (Slack, 1964). Silicon NW has shown its priority in TE application. Compared with bulk Si, an extreme reduction of thermal conductivity (1.6 W m\(^{-1}\) K\(^{-1}\)) has been demonstrated for Si NWs with a 50 nm diameter without the detriment of Seebeck coefficient and electrical resistivity values (Hochbaum et al., 2008). The strong diameter dependence of Si NWs thermal conductivity has been demonstrated, which is attributed to the enhanced phonon-boundary scattering and phonon spectrum modulation (Li et al., 2003b). The similar reduction of thermal conductivity from bulk to NWs has also been reported in Ge-based TE research. A sub-30 nm diameter Ge NWs was measured with a thermal conductivity of \( \sim 1.5-2.3 \text{ W m}^{-1} \text{ K}^{-1} \) at 300 K (Wingert et al., 2011), dramatically decreased from Ge bulk (\( \sim 56 \text{ W m}^{-1} \text{ K}^{-1} \)) (Glassbrenner and Slack, 1964). Also, we can see a decrease of thermal conductivity compared to the Si NWs mentioned above, and the difference is explained by the heavier atomic mass and decreased phonon velocities of Ge with respect to Si (Wingert et al., 2011).

Si NW arrays, which are largely parallel Si NWs, have been fabricated on Si substrate with metal-assisted chemical etching (MaCE) in order to make a TEG. With an amount larger than \( \times 10^2 \) in several mm\(^2\), a 0.5 mm thick sample chip, and NWs diameter between 60 and 120 nm, the thermal conductivity was measured at \( \sim 4.6 \text{ W m}^{-1} \text{ K}^{-1} \) (Pennelli et al., 2018).

Isotope doping can be a feasible way to reduce thermal conductivity. Isotope effect on the thermal conductivity of Si NWs has been researched theoretically based on the nonequilibrium molecular dynamics (NEMD) method (Yang et al., 2008). Random isotope doping Si NWs and isotopic-superlattice Si NWs are built in this research, the minimum thermal conductivity is 0.4 W m\(^{-1}\) K\(^{-1}\) is shown in \( ^{28} \text{Si}_{0.5}^{12} \text{Si}_{0.5} \) NWs with cross sections of 1.6 × 1.6 nm\(^2\). Furthermore, a curve of thermal conductivity vs. the concentration of doping isotope atom (x) is exhibited, which shows a similar tendency with \( ^{28} \text{Si}_{1-x}^{12} \text{Si}_x \) and a plateau at 0.2 < x < 0.8 (We will discuss this tendency in the next section). More simulations have been conducted for the isotope effect on thermal conductivity, like the isotopic core-shell Si NWs (Hattori and Uno, 2013) and isotope radial distribution (Royo and Rurali, 2016). The fabrication of Si isotope NWs is demonstrated in Mukherjee et al. (2015) using the VLS method and a 30% decrease of thermal conductivity is shown in isotopically mixed \( ^{28} \text{Si}_{x}^{12} \text{Si}_{1-x} \) NWs compared with isotopically pure \( ^{28} \text{Si} \). This is in agreement with the aforementioned simulation.

Si\(_{1-x}\)Ge\(_x\) Alloy NWs

Starting in the 1970s, SiGe alloys have been applied in RTGs for the power systems in NASA space missions (with \( ZT \sim 0.5 \) for P-type and \( \sim 0.9 \) for N-type at 1,073 K; Rowe, 1995). Later improvements were realized in nanostructured bulk SiGe with \( ZT \sim 1.3 \) at 1,173 K for N-type (Wang et al., 2008a) and \( ZT \sim 0.95 \) at 1,073 K for P-type (Joshi et al., 2008). A recent study has fabricated \( Si_{0.8}Ge_{0.2}B_0.5 \) bulk alloy with the maximum \( ZT \) of 0.71 at 1,073 K using melt spinning (MS) combined with spark plasma sintering (SPS) (Wongprakarn et al., 2018).

Like Si NWs, SiGe alloy NWs exhibited excellent enhancement as a result of the phonon boundary scattering. Individual P-type SiGe alloy NW was reported with thermal conductivity \( \sim 1.1 \text{ W m}^{-1} \text{ K}^{-1} \) and \( ZT \sim 0.18 \) at 300 K experimentally (Martinez et al., 2011). In a typical TE modeling of SiGe NWs, the optimized \( ZT \) is 1.3 at 800 K for the \( Si_{0.73}Ge_{0.27} \) NW with 26 nm diameter where the ionized impurity concentration should be about 1.0 × 10\(^{20} \) cm\(^{-3} \) (Yi and Yu, 2015). In principle, the \( ZT \) of SiGe at different temperatures can be further enhanced by the diameter reduction and doping concentration optimization. The reduction in SiGe alloy NWs came from the phonon alloy scattering which scatters short wavelength phonons with high frequency, while low frequency phonons are scattered by the phonon boundary scattering (Li et al., 2003a).

Several studies have investigated the effect of Ge fraction (x) on the thermal conductivity (\( \kappa \)) in Si\(_{1-x}\)Ge\(_x\) NWs both theoretically and experimentally (Wang and Mingo, 2010; Li et al., 2012; Yi and Yu, 2015). In an MD simulation, with x = 0.05, the \( \kappa \) of SiGe NW was decreased to half of that of the intrinsic Si NW, and the minimum thermal conductivity was shown at x = 0.5, which is reduced to only 18% (Chen et al., 2009). With a similar tendency found in bulk SiGe alloy, it has been shown that a dramatic reduction of thermal conductivity happens when the Ge concentration increases in a small scale less than x = 0.005 (Wang and Mingo, 2010). The further increasing of Ge content will decrease the thermal conductivity to approach the lower limit which is achieved at
A study on the surface doping effect shows different types of alloying of SiGe, and Ge are used in a small fraction as a dopant on the surface of Si NWs with a facile fabrication (Pan et al., 2015). Compared to pristine Si NW, the Ge-coated Si vertical NW arrays show a 23% reduction in thermal conductivity at 300 K, and such a decrease can be enhanced to 44% by annealing. Analyzed by X-ray photoelectron spectroscopy (XPS), the interaction between Ge surface doping and Si NWs is
enhanced by the binding energy shifting of Si-2p and Ge-3d after annealing treatment. Moreover, simulated results by MD method shows the SiGe composition has to be graded in order to effectively optimize the thermal conductivity. Compared to the SiGe with abrupt interfaces, a 57% reduction of thermal conductivity was reported for the graded SiGe NW (Zhang et al., 2017).

Besides Ge fraction, diameter (D), and length of SiGe NWs are also important issues for the TE properties (Li et al., 2003b; Wang and Mingo, 2010). The thin NWs show a reduction of thermal conductivity when compared with the thick ones. A thorough study has been designed to find the certain trend (Shi et al., 2009), and the result is that thermal conductivity is proportional to D when D is small. However, this dependence becomes continually weaker with increasing D. Combined with the Ge constituent effect, the group found the linear trend slowed down with a higher Ge content, up to x = 0.5. The same situation happens with the increasing Si in Ge. This is because of the coexistence of alloy and boundary scattering. SiGe NW arrays with a longer length exhibit a higher Seebeck coefficient while the thermal conductivity decreases with increasing Ge concentration and NW length (Li et al., 2012).

When it comes to doping type, N-type SiGe NWs are reported to have remarkably higher ZT and power factor compared to P-type SiGe NWs at 300 K (Shi et al., 2010). With a cross section area of 2.3 nm², the ZT of N-type Si$_1-x$Ge$_x$ NWs was theoretically calculated to be ~4.3 (Shi et al., 2010). In Noroozi et al. (2017a), the peak of Seebeck coefficient for N-type and P-type Si$_{0.53}$Ge$_{0.47}$ are 8 and 1.8 mV/K at 315 K, which can be explained by the temperature dependence of the interaction of defects. With the same diffusion process applied, the carrier mobility in N-type SiGe NWs is higher than P-type, which results in a much higher Seebeck coefficient in N-type SiGe NWs than P-type. Also, the measured maximum power factor of N-type is two times higher than P-type.

**Other Promising Group IV Materials**

With the prosperity of silicon-based technology, other Group IV materials have also been studied as composite materials. They have similar crystal textures, so they have lower processing costs and high compatibility. With the publications of theoretical and experimental research, it was discovered that carbides and tin compounds with silicon and germanium have excellent TE properties.

**SiC**

As the recognized third generation semiconductor material, SiC has become a promising material for power electronics. Different advanced growth methods have been applied to improve the crystal quality (Pecz et al., 1999; Yakimova et al., 2011). SiC has also been applied to other semiconductor devices including composites, field emitters, supercapacitors, field-effect transistors, nanoelectromechanical devices, photocatalysts, sensors, microwave absorbers, and super-hydrophobic coating (Zekentes and Rogdakis, 2011; Wu et al., 2015; Chen et al., 2019). A lot of studies have presented the performances of SiC. Under those investigations, SiC exhibits excellent mechanical properties, exceptional chemical stability, high power, high frequency, thermal stability, and low thermal conductivity (Zekentes and Rogdakis, 2011; Wu et al., 2015; Chen et al., 2019). Some people have investigated its TE properties to seek for the possibility of SiC as a TE material (Choi et al., 2011). The revealed characteristics demonstrated the possibility for SiC as a superb TEG material which can work in harsh ambiances like high-power/high-temperature/high-voltage.

Both theoretical and experimental studies have been carried out for the thermal properties of SiC NWs. NEMD simulations were used on the lattice thermal conductivity of bulk β-SiC and NWs (Papanikolaou, 2008). Like Si and SiGe, a dramatically reduced thermal conductivity has been shown in SiC NWs compared to the bulk SiC, similarly owing to the boundary scattering and size confinement of phonons in nanostructures. In another piece of research based on NEMD, the thermal conductivity of SiC NWs with modulated diameters and polytypes were predicted, and it was also found that the increase of both the diameter and length can enhance the thermal conductivity of SiC NWs with the similar tendency of Si NWs (Termentzidis et al., 2013). A repeatable method involved placing the individual or double β-SiC NWs on pre-patterned electrodes via a nanomanipulator combined with focused ion beam (Lee et al., 2010), and the 300K method measured thermal conductivities of the individual and double NWs were, respectively, 82 ± 6 and 73 ± 5 W m$^{-1}$ K$^{-1}$. Likewise, the thermal conductivity, electrical conductivity, and Seebeck coefficient of SiC NWs were reported as a function of temperature for the SiC NWs from 190 to 370 K (Valentin et al., 2013). The Seebeck coefficient was measured varying from −17 to −68 μV/K with the temperature range, and at 300 K the S varied from −22 to −56 μV/K, for N-type doped SiC (Valentin et al., 2013). A simulation study demonstrates that the thermal conductivity ranged from 4 to 12 W m$^{-1}$.
Si-Ge-Sn Binary and Ternary Alloys

Compared to C, Si, and Ge, Sn has a larger atomic mass and bigger atom diameter. The size difference has a large impact on TE performance. A variety of studies have demonstrated their alloy effects significantly decrease thermal conductivity.

Theoretically, a group investigated the Sn alloying effect to SiGe on the thermal conductivity ($\kappa$) of SiGeSn alloys using NEMD simulations with optimized Stillinger–Weber parameters (Lee and Hwang, 2017). The afore-mentioned broad plateau in SiGe alloy also appeared in the ternary alloys. With a realizable content range in $0 \leq x \leq 0.2$, the $\kappa$ of Si$_{0.8}$Ge$_{0.2}$Sn$_x$ alloy was much lower than the SiGe and Ge alloys. The predicted minimum of $\kappa$ occurred at $x = 0.1$ with a ~40% reduction compared to those of Si$_{0.2}$Ge$_{0.8}$ and Ge$_{0.2}$Sn$_{0.8}$. This reduction is produced by the increased mass disorder scattering of phonons similar to SiGe. Another theoretical study with phonon Boltzmann transport formalisms have simulated the phonon thermal conductivity of SiSn, GeSn, and SiGe-Sn alloys and their corresponding thin films (Khatami and Aksamija, 2016). They showed that the minimum thermal conductivity of Si$_{1-x}$Sn$_x$ alloys was 3 $W\ m^{-1}\ K^{-1}$ with $x = 0.5$ and 5.86 $W\ m^{-1}\ K^{-1}$ for the Ge$_{1-y}$Sn$_y$ with $y = 0.61$, which can be the lowest of the three alloys, twice as low as SiGe. In contrast, their simulation of the 20 nm SiGe, SiSn, and GeSn thin films offer a further decrease in $\kappa$ with a value of 1.71 $W\ m^{-1}\ K^{-1}$ for the Si$_{0.51}$Ge$_{0.49}$, 0.91 $W\ m^{-1}\ K^{-1}$ for the Si$_{0.41}$Sn$_{0.59}$, 1.53 $W\ m^{-1}\ K^{-1}$ for the Ge$_{0.45}$Sn$_{0.55}$, and 1.11 $W\ m^{-1}\ K^{-1}$ for the Si$_{0.36}$Ge$_{0.32}$Sn$_{0.32}$ which are near the conductivity of amorphous SiO$_2$ (Khatami and Aksamija, 2016). Both pieces of research theoretically show the TE potential of Sn incorporated with SiGe.

Experimentally, phosphorous-doped Ge$_{0.97}$Sn$_{0.029}$ NWs is fabricated using RPCVD and its electrical conductivity and Seebeck coefficient data is compared to the Si and Ge NWs at 250 K for NWs with cross-sectional area of 700 $\times$ 50 nm and length 22 $\mu$m. The GeSn is measured with electrical conductivity ~550 $\Omega^{-1}\ cm^{-1}$, which is much higher than Si (231 $\Omega^{-1}\ cm^{-1}$) but less than Ge (653 $\Omega^{-1}\ cm^{-1}$), and Seebeck coefficient ~67 $\mu$V/$K$, larger than Si (42 $\mu$V/$K$) or Ge (47 $\mu$V/$K$). The calculated power factor is 0.24 $m^2 W^{-1} K^{-2}$, superior to Si (0.041 $m^2 W^{-1} K^{-2}$) and Ge (0.14 $m^2 W^{-1} K^{-2}$) (Noroozi et al., 2014). The electronic properties of Ge$_{0.81}$Sn$_{0.19}$ NWs were studied in the temperature range of 10–298 K, and resistivity of Ge$_{0.81}$Sn$_{0.19}$ NW ($\sim 1 \times 10^{-4}\ \Omega\ m$) was 100 times lower than the pure Ge ($\sim 9 \times 10^{-3}\ \Omega\ m$) at room temperature (Sistani et al., 2018). The difficulty for the high Sn content in SiSn alloy fabrication (and, to a lesser extent, Ge-Sn) comes from the 19.5% lattice mismatch between Si and α-Sn, and Sn has a low solid solubility (~5 $x\ 10^{19}\ cm^{-3}$) in Si (Min and Atwater, 1998). No experimental data of Si$_{x}$Sn$_{1-x}$ and Ge$_{y}$Sn$_{1-y}$ NWs has been found for the thermal conductivity yet, which may be a sally port for TE material research.

ADVANCED STRUCTURES

The effective TE performance modulation by diameter and alloying have been proven theoretically and experimentally. New atomic-scale designs and surface structure as toolkits for thermal conductivity control are also under investigation (Özden et al., 2015). To reduce the time and cost of the experiments, several calculation models have been proposed to simulate new nanostructures. These structures affect the TE performance by modulating various scattering events we mentioned in Chapter 2 such as phonon normal scattering, phonon boundary scattering, and phonon Umklapp scattering.

Many possible structures have been considered on the foundation of SiGe alloy NW $\mu$TEGs with high TE performance in the past decades, like core-shell (C-S) (Hu et al., 2011; Markussen, 2012), superlattice (SL) (Lee et al., 1997; Huxtable et al., 2002; Li et al., 2003a), etc. Compared with the pure NWs, these structures further suppress the thermal conductivity by enhancing various phonon scattering owing to the lattice mismatch of ~4% between Si and Ge.

In a recent theoretical work, pristine, core-shell, holey, superlattice, sawtooth, and superlattice sawtooth Si/SiGe NWs with identical structural parameters were investigated (Özden et al., 2015). A comprehensive comparison of thermal conductivity in those different nanostructures was performed by using equilibrium molecular dynamics (EMD) simulations with Green-Kubo method at room temperature. The results demonstrated that thermal conductivity can be minimized by varying the specific parameters e.g., the core diameter and monolayer separation for Core-Shell (C-S), holey, and sawtooth structures. However, for SL structures, the thermal conductivity is independent of the above-mentioned parameters. The lowest thermal conductivity in these structures has been demonstrated for the sawtooth superlattice NW, with $\kappa < 2\ W \ m^{-1} K^{-1}$ (Özden et al., 2015).

Core-Shell (C-S)

The SiGe C-S structure is a radial heterostructure of Si and Ge. SiGe alloys have been used in many electronic devices, such as stressor and high mobility channel materials, for years. Both Ge or SiGe layers could be grown selectively in trenches or around SiNWs as core layer (Grahn et al., 2000; Hällstedt et al., 2008b; Radamson and Kolahdouz, 2015). The interface between core and shell reduces thermal conductivity by phonon scattering. A successful synthesis of Ge–Si core–shell NWs with no branch has been reported recently and the synthesis processes were elaborated in detail (Noguchi et al., 2016).

Wingert et al. has synthesized sub-20 nm diameters Ge and Ge–Si C-S NWs by VLS-CVD method (shown in Figure 7; Wingert et al., 2011). Particularly, $\kappa$ of the C-S NWs at 388 K is 1.1–2.5 $W\ m^{-1}\ K^{-1}$, remarkably reduced from the Ge NWs (2.3–3.9 $W\ m^{-1}\ K^{-1}$).

Some theoretical works have applied first-principle calculations and Boltzmann transport theory to model the
TE performance of Ge/Si or Si/Ge core-shell NWs (Wingert et al., 2011; Yang et al., 2015; David et al., 2017). In a study (Chen et al., 2010), with the optimal carrier concentration of $2.64 \times 10^{25}$ m$^{-3}$, the achieved maximum $ZT$ value reached $0.85$ at $300$ K in Ge/Si C-S NWs with P-type doping, significantly larger than 0.36 in pure Si NWs. Moreover, they verified the chances for the further improvement of the C-S NWs by optimized core/shell radius ratio, NW sizes, doping, orientation, and surface structure (Chen et al., 2010). Several factors, such as the core/shell radius ratio, may influence the C-S thermal conductivity (Lü, 2009): (1) The C-S structures have a weaker length dependence compared to pristine NWs due to the diffusion dominant phonon transport, and the thermal conductivity of C-S is even low for the long NWs; (2) The thermal conductivity of C-S structure is practically independent of the temperature in the range of 50–600 K, which shows a confinement of the core by the shell; and (3) Unlike the monotonic impact on the thermal conductivity of pure NWs, the increasing diameter of the core-shell NWs first reduced the thermal conductivity to a minimum then boosted it because of the contrast from core center vs. shell surface.

**Superlattice (SL)**

Semiconductor SLs are attractive for their potential as TE materials (Li et al., 2003a). The traditional 2D SL is the multilayer thin films of different materials that are alternately periodically stacked, and 1D NW SL is the axial heterostructure NW of different materials which can be seen as a series of interlaced nanodots of these different materials (Chen et al., 2011). Due to the periodic modulation of energy gaps by the adjacent nanodots, the TE properties can be improved. The different scattering mechanisms are demonstrated in Dames and Chen (2004), which can be explained by Figure 8. In SLs, heat transport is modulated by various phonon scattering phenomena (Li et al., 2003a): alloy scattering, interface scattering caused by the mismatch in acoustic impedance, and scattering by lattice mismatch from imperfections. The energy filtering mechanism is also effective in the research of superlattices (Thesberg et al., 2016).

Lee et al. (1997) have fabricated 2D Si/Ge SL with SL periods from 30 to 300Å, the thermal conductivity was measured at $<5$ W m$^{-1}$ K$^{-1}$. Monocrystalline Si/SiGe superlattice NWs were synthesized block-by-block based on hybrid pulsed laser ablation/chemical vapor deposition (PLA-CVD) method in 2002 by Wu et al. (2002). Later, the thermal conductivity of Si/SiGe SL NWs with 58 and 83 nm diameter was measured from 20 to 320 K. The value varied from 1 to 7 W m$^{-1}$ K$^{-1}$, lower than the SiGe alloy film, 2D Si/SiGe SL film, and intrinsic Si NWs at the same temperature (Li et al., 2003a). Among different research groups, Si/Ge SL NWs with a diameter below 20 nm were reported by using metal-assisted etching (Geyer et al., 2009).

Owing to the difficulty in the SL fabrication, more recent research about superlattice are based on simulations (Xiong et al., 2014; Mu et al., 2015; Hijazi and Kazan, 2016; Qu and Gu, 2020). The MD simulation of Si/Ge SL NWs have reported a 95% reduction by the periodic Si/Ge defects, while amorphization and roughening of the NW surface are utilized (Mu et al., 2015). They concluded that periodicity perturbation can be a useful method for the reduction of SL thermal conductivity by impairing the formation of phonon coherence (Mu et al., 2015).

**Other Origin Structures**

Sawtooth Si NWs have been fabricated with periodic sawtooth faceting by VLS (Ross et al., 2005). Later, a Monte Carlo simulation demonstrated that the sawtooth roughness caused a thermal conductivity suppression below the limit of diffuse surface by introducing phonon backscattering (Moore et al., 2008). Such surface faceting dependence of thermal conductivity in Si NWs was demonstrated by direct MD simulations and the Si sawtooth NWs with $\kappa \sim 16$ W m$^{-1}$ K$^{-1}$ was reported (Sansoz, 2011).

Recently, a novel structure, called fishbone NWs, has been synthesized and studied, which is intrinsic silicon NWs with periodic wings (Shown in Figure 9) and the $\kappa$ of those fishbone NWs were reported between 30 and 50 W m$^{-1}$ K$^{-1}$ (Maire et al., 2018). The researchers investigated the heat conduction of this structure through experiments and found that the cross-section of fishbone NWs also controlled the $\kappa$, as in pristine NWs, and further reduction was caused by the periodic wings. The increasing wing depth exhibited a significant decrease of $\kappa$ (this decrease was intensified in narrower NWs) while the wing...
width only had a slight influence, and these effects were explained by modeling.

There is a study on the TE properties about a gate-all-around (GAA) structure Si NWs (Curtin and Bowers, 2014). Using multi-subband Boltzmann transport formulation and relaxation time approximation, a GAA Si NW with a cross-sectional area between $4 \times 4 \text{ nm}$ and $12 \times 12 \text{ nm}$ was simulated and compared with experiment. With the charge carriers induced with the electrical gate, no ionized impurity scattering was discovered; meanwhile, the mobility and electrical conductivity were increased compared to the doped materials. The smaller cross-section of the Si NWs showed stronger quantum confinement, which means an improvement of the Seebeck coefficient. This also exhibited an enhanced electrical conductivity in a smaller cross-section. The maximum power factor of the $6 \times 6 \text{ nm}$ Si NWs achieved $6.8 \times 10^{-3} \text{ W m}^{-1} \text{ K}^{-2}$ (Curtin and Bowers, 2014).

Though many Si/Ge/SiGe-based novel structures have been simulated to study the TE properties, few have been achieved in the experiments. Even fabricated, they are not applied in the TE field. Further experiments are indispensable for those structures to be used in TE devices.

**MATERIAL GROWTH AND FABRICATION OF µTEG**

Si NWs can be fabricated only in the $<100>$, $<111>$, $<110>$, or $<112>$ directions depending on their diameter and the substrate (Wang et al., 2008b). For industrial manufacturing, the (100) Si wafer are the most common substrates, and the vertical Si $<100>$ NWs can be easily utilized by the etching process (Wolfsteller et al., 2010). Meanwhile, the $<100>$ crystal orientation also exhibits better TE performance than the $<111>$ in SiGe bulks and NWs (Kandemir et al., 2017). Besides the conventional Si substrate, the most used substrate for Si and SiGe NWs is the $<100>$ SOI wafer for its fabrication convenience and good electrical properties (Barraud et al., 2019). A research group prepared a SiGeOI wafer for the fabrication of SiGe NWs (Noroozi et al., 2017b). The SiGe nanowires operated as an FET transistor with back-gate configuration.

In order to achieve the NWs structure, several fabrication technologies have been proposed and applied. They are classified into two methods: “Bottom-up” and “Top-down.” Bottom-up fabrication is a somewhat easier way to achieve NW growth compared to the Top-down, and it also has the advantages of low cost and massive fabrication. However, more complex processes are necessary for the contacts and connection with NWs. Meanwhile, the top-down method, though expensive, is CMOS-MEMS compatible and allow the fabrication of NWs together with contacts, connections, and control gates. In practical process, the vertical NWs can be easily synthesized by the bottom-up methods for material research, while NWs with both vertical and horizontal orientation are suitable to be fabricated and integrated into the device like TEG with top-down approaches (Ray et al., 2017). Wolfsteller et al. have fabricated the Si/Ge NW heterostructures in both bottom-up and top-down approaches, and the diameter of the NWs are down to tens of nm; the differences between the two approaches have been compared (Wolfsteller et al., 2010). Another approach to form NWs is Sidewall transfer lithography where a sacrificial layer is deposited oxide and later etched to form residuals on both sides of the oxide. The oxide is removed, and the remaining residuals are used as a mask to form the NWs. In this way, very narrow NWs with widths of 20 nm can be synthesized (Hällstedt et al., 2008a).

### Bottom-Up

One of the most popular methods for the fabrication of Si NWs in bottom-up approaches is the vapor–liquid–solid (VLS) mechanism (Wagner and Ellis, 1964). With an Au droplet as catalyst, several approaches have been applied to the bottom-up growth of Si, Ge, and SiGe NWs based on the VLS mechanism like chemical vapor deposition (CVD), molecular beam epitaxy, and laser ablation (Ray et al., 2017). The typical process of VLS is illustrated in Figure 10, which follows three different steps: (1) source gas like silane ($\text{SiH}_4$) or tetrachlorosilane ($\text{SiCl}_4$) is decomposed at the vapor–liquid interface under a high temperature, (2) Si atoms diffuse through Au-Si eutectic, and (3) the Si NWs crystallize at the growing liquid-solid interface (Hällstedt et al., 2008a). The diameter is modulated by the droplet diameter while the length is regulated by the growth time (Kim, 2013).

Based on the VLS methods, a variation named vapor-solid-solid (VSS) was put forward. In this method, the NWs are fabricated at lower temperature than in VLS, which is available for the mass production of devices since it is more compatible with standard industrial processes. There is a report that Si/Ge heterojunction NWs with abrupt interfaces have been grown by VSS (Chou et al., 2012).

The problem for the VLS growth mechanism may lie in the potential inclusion of the metal catalyst during the growth of NWs, because metal catalysts like Au are a detriment to the electrical properties of the Si-based electronics which produce deep-level, carrier recombination centers or cause unintentional doping. Though such problems can be neglected for current

![FIGURE 8 | Dominating scattering mechanisms in superlattice NWs (A) diameter limited; (B) superlattice limited; (C) bulk limited. Reprint from Dames and Chen (2004).](Image)
Si NWs, it is better to avoid the problem for better device performance. Several analytical technologies, like high-angle annular dark-field scanning transmission electron microscopy (Oh et al., 2008) and secondary ion mass spectroscopy, at the nanoscale are applied for the detection of Au atoms inside Si NWs (Putnam et al., 2008).

**Top-Down**

The top-down fabrication approach is based on the Si CMOS technology like lithography, etching, and oxidation. The highly anisotropic etching (wet, plasma, and metal assisted) is key to the Si NWs fabrication. Different types of etching are applied in different research, such as silicon alkaline etching, RIE, and MaCE.

Silicon alkaline etching is a cheap and convenient way for etching, and typically uses KOH (potassium hydroxide) or TMAH (tetramethylammonium hydroxide). Based on the anisotropic etching properties of alkaline solution, the etching rate of $<111>$ direction is much slower than other directions like $<100>$; more than 1/100 between $<111>$ and $<100>$ directions have been shown in a typical 35% KOH aqueous solution at 43°C (Pennelli, 2015).

Using chemical reactive plasma as an etchant, RIE can be applied for the fabrication of Si NWs (Peng et al., 2015). High-energy plasma ions etch the wafer surface and cause surface damage, then the outer atoms are removed from the surface. Suitable materials with high selectivity for the mask are the precondition to fabricate structures on the substrates. The commonly used masks are polymers, SiO$_2$, Si$_3$N$_4$, patterned metal film, or metal nano-particles like Au, Ag, Ni, Al, and W (Ray et al., 2017). Inductively coupled plasma-reactive ion etching (ICP-RIE) has been applied based on RIE while an RF powered electric field is used to generate the plasma, but the ion has a low energy compared to the conventional RIE. Research about the fabrication of CMOS-MEMS $\mu$-TEG has been reported using RIE; CHF$_3$/O$_2$ is used for the oxide layer while XeF$_2$ is used for the Si substrate (Kao et al., 2010).

MaCE is an electrochemical technique which has been widely used for its low-cost and high yield. Figure 11 has illustrated the procedures of MaCE of silicon NWs under 100 nm and the
The measurements of NW arrays are somewhat simpler than the single NW. It is easier to prepare NWs array samples, and the oxidation of NWs can be decreased in the processing which show a large deviation when measuring in single NW (Swinkels and Zardo, 2018). Surface oxidation complicates the electrical contacts and aggravates the measurement difficulties, therefore, it is important to design a suitable measurement configuration. The high-density arrays can reduce the radial thermal conductivity, and thus the measurement can be focused on the axial direction (Gadea et al., 2018a). However, some drawbacks still exist for the growth of orderly arrays and achievement of the low thermal or electrical contact resistances by depositing a metal layer on top NWs.

Based on the principles of measurement, several groups have researched the TE measuring techniques in different aspects. A group have divided the equipment into electrical-based, which is SPM-based, and optical-based equipment (Rojo et al., 2013). In electrical-based analysis, the single NW is fabricated on the µ-chip in suspended or non-suspended substrate. In SPM-based research, the measuring process is based on a series of characterization techniques that use tips like Kelvin Probe Microscopy (KPM), Scanning Tunneling Microscopy (STM), Atomic Force Microscope (AFM), and SThM. Different in the optical-based part, the measurements are non-invasive by adapting photo-acoustic or photo-thermal techniques.

Thermal conductivity measurement of such non-contact methods are further investigated and summarized in Abad et al. (2017) and Liu et al. (2019). A review about the nanostructure measurement has concluded twelve techniques for thermal conductivity and five methods for Seebeck coefficient (Liu et al., 2016).

A typical way for measurement is the 4-point contacts method, which is shown in Figure 12 (Boukai et al., 2008; Yanagisawa et al., 2020). Electrical conductivity is the relatively easy part in the measurement, which can be achieved by measuring the I-V characteristics with the known NW dimensions (area A, length L). With a preassembled heat source as a heater and a thermometry measurement, the temperature difference between the hot side and cold side of the NWs can be measured for the determination of thermal conductivity. Finally, the Seebeck coefficient can be measured from $S = AV/\Delta T$ by applying an open voltage on the sample with a temperature difference. With the three parameters, $ZT$ can be calculated. Similar techniques, like the 2-point method, have also been used in some research. However, the 4-point method is more accurate for the direct measurement of thermal conductivity rather than the estimation in the 2-point method (Rojo et al., 2013). With respect to the 2-point-probe technique, the 4-point probe can eliminate the resistance of NWs outside the substrate and minimize the contact contribution (Shi et al., 2010).

The $3\omega$ method has been described for thermal conductivity measurement of bulk crystal and thin films in 1990 (Cahill, 1990), then it is applied to the Si NWs (Stranz et al., 2011). With an alternating current at frequency $\omega$ passing through the heater, the generated Joule heating is at a frequency of $2\omega$ ($P = I^2 R$), accompanied by temperature oscillation at the same $2\omega$ frequency. Meanwhile, with temperature increasing,
the resistance is increased by a $2\omega$ oscillation. Thus, there is a $3\omega$ oscillation component of the voltage ($V = IR$) across the heater, and the thermal conductivity can be calculated by measuring this component (Lu et al., 2001). A similar $2\omega$ technique combined four-probe microchip has been put forward so that the Seebeck coefficient can also be attained by the equation $S = \Delta V(2\omega)/\Delta T(2\omega)$, while the $\Delta V(2\omega)$ is the Seebeck voltage induced by the temperature difference from the ac current at frequency $\omega$ through a micro-heater (Kirihara et al., 2011).

An alternative method for TE properties is the SPM. In this kind of technique, probes or tips are used for scanning the NWs with nanometric resolution. The surface topography of samples can be imaged by the probe. With high spatial resolution, SPM are utilized for measurements of both electrical and thermal conductivities. For NWs electrical conductivity measurement, the AFM and STM are typically used, while SThM combined with the $3\omega$ method can be used for thermal conductivity measurement (Grauby et al., 2013), shown in Figure 13.

**TE Properties for NWs and TEG**

The first measured thermal conductivity of silicon NWs was achieved in 2003, and found a small value of $\kappa$ down to 7–8 W m$^{-1}$ K$^{-1}$ for NWs 22 nm wide with the VLS method (Li et al., 2003b). Compared to 20 nm thickness Si film with thermal conductivity $\sim$ 22 W m$^{-1}$ K$^{-1}$, a reduction of around two-thirds of the thermal conductivity was observed, and the value becomes smaller than measured suspended films down to a thickness of $\sim$10 nm with thermal conductivity $\sim$10 W m$^{-1}$ K$^{-1}$. For the measurement, they used microfabricated suspended plates for the positioning of the individual NW, where Pt resistors were integrated in the TEG as electrodes, heater, and thermometer; this method has been adopted in many studies. Following, Hochbaum et al. used 50 nm NWs fabricated by MaCE and demonstrated a very small $\kappa$ of 1.6 W m$^{-1}$ K$^{-1}$ where the phonon thermal conductivity $\kappa_{\text{ph}}$ was estimated about 1 W m$^{-1}$ K$^{-1}$. This is 5–8 times lower than the corresponding Si NWs synthesized by the VLS method (Hochbaum et al., 2008). The reduction was explained by the phonon surface scattering effect, since MaCE NWs exhibited a rougher surface compared to VLS NWs (Pennelli, 2015). Later, more research reports about Si NWs have reported the thermal conductivity based on different equipment. A TE module based on vertical rough Si NWs with 200 nm diameter showed the lowest thermal conductivity between 10.1 and 14.8 W m$^{-1}$ K$^{-1}$ with boron- and phosphorus-doped, and the $P_{\text{max}}$ was 3.74 W/cm$^2$ with temperature difference $\Delta T = 180$ K (Lee et al., 2019). For different fabrications and measurement techniques, the precision in data varies according to the literature. And the experiment conditions are constantly changing and errors may exist. When measuring the samples, it is crucial to select appropriate measurements for accuracy.

For the fabricated $\mu$TEG in research, there are several experimental data of generated output. A vertical Si NW structure is demonstrated by RIE with a TE power of 29.3 $\mu$W at $\Delta T = 56$ K under 50 $\times$ 50 $\mu$m chip area; spin-on glass thin film is applied for the support of Si NW (Curtin et al., 2012). An output power density of 9 $\mu$W/cm$^2$ is measured at $\Delta T = 27$ K cross the Si NWs $\mu$TEG fabricated by the CVD-VLS methods (Dávila et al., 2012). By standard CMOS processing, 20 thin Si membranes generated an output power density of 4.5 $\mu$W/cm$^2$ under $\Delta T = 5$ K by using 20 thin Si membranes made $\mu$TEG with area of 50 $\times$ 150 $\mu$m on the chip (Perez-Marín et al., 2014). More recently, Donmez et al. have measured the maximum power densities of Si NWs, SiGe NWs, and Si micro-beam-based $\mu$TEG with values of 41.2, 45.2, and 34.5 $\mu$W/cm$^2$, respectively, at a hot plate temperature of 100ºC (Donmez Noyan et al., 2019). A two-leg $\mu$TEG has been fabricated based on vertical Si NW forest where the achieved power output is 0.25–0.5 $\mu$W/(cm$^2$ºK) with the NW length from 25 to 6.5 $\mu$m (Elyamny et al., 2020). By shortening Si NW to sub-$\mu$m length, a planar $\mu$TEG achieved the power density of 12 $\mu$W/cm$^2$ with $\Delta T = 5$ K (Tomita et al., 2018b).

Simulations and analytic models based on the finite element method (FEM) have been applied for the risk/cost reduction in fabrication, and the data are compared with the experimental results (Tomita et al., 2018b; Donmez Noyan et al., 2019; Elyamny et al., 2020). In a recent study, with the 3-D FEM device simulation software COMSOL Multiphysics, a research group has analyzed the thermal distribution and power generation of Si NWs TEG with varied parameters (Zhang et al., 2018). An extreme high-power density of 4.2 and 425 mW/cm$^2$ was achieved in the simulation at 0.1 $\times$ 0.1 $\mu$m Si NWs, respectively, under $\Delta T = 5$ and 57 K. With the model, maximum power generation density is speculated to be proportional to $\Delta T^2$.

**Thermal and Electrical Contact Resistance**

The electrical and thermal contact resistance of the metal electrodes are special issues for measurement which have severe impacts on the nanodevice performance which mean that ohmic contacts are necessary. Following the scaling of IC-technology, different metal electrodes have been experimented on for the contact resistance with the tendency of TiSi$_2$ $\rightarrow$ CoSi$_2$ $\rightarrow$ Ni(Pt)Si in planar structures (Lavoie et al., 2017). For the fabrication of $\mu$TEG integrated with a heater, Pt is a good choice for both electrodes and heaters due to its thermal-independence.
and low electrical/thermal contact resistance (Noroozi et al., 2017b). NiSi has also been a good choice for electrodes for those μTEG heated from the outside (Zhan et al., 2018). AlN films are adopted as thermally conductive layers for TEG with 300/500 nm thickness and the respective thermal conductivity is 4 and 11 W m⁻¹ K⁻¹. Other metals or multi-metals have been adopted, like tungsten (W) (Gadea Díez et al., 2020), Ti/W (Noyana et al., 2019), Ti/Pt (Boukai et al., 2008), and so forth. Recent research has reported the effect of thermal boundary resistance in the contact layer, and several metal/adhesion/dielectric materials have been compared for their thermal conduct property. The contact layer with the Al/Ti/SiO₂ (300/10/10 nm) structure turns out to have the best TE performance compared to the counterpart Cu/Cr/AlN (Zhan et al., 2020). Furthermore, a study found that it is effective in reducing the heat loss across the interfaces by utilizing Ag foil as electrodes and exerting pressure on it (Xu et al., 2013). They also found that, by applying spin-on-doping (SOD) on the Si wafers before the NW arrays are etched, the electrical contact resistance can be reduced by the heavily doped top of NWs. By searching for the optimal power output, an original zigzag arrangement has been implemented for metal supports which allows aligned membranes with arbitrary length. Due to the enhanced metal/window area ratio, such a structure can provide decreased internal resistances (Calaza et al., 2016).

Other than Si NW metallic contact, researchers have also investigated the contact for SiGe. Cobalt has been used to form the CoSi₂ on the SiGe layer (Nur et al., 1994, 1995). Nickel has been applied to the SiGe with carbon doping and the thermal stability of Ni(SiGeC) is improved compared with Ni(SiGe) (Hällstedt et al., 2004). A similar thermal stability enhancement by carbon doping has also been observed in Ni(Ge) and Ni(GeSn) (Liu et al., 2014, 2015). Moreover, instead of traditional TiSi₂, TiSi₃, and TiSi₃Geₓ are used for the Ti-based ohmic contacts (Mao et al., 2017; Mao and Luo, 2019).

Ideal contact materials should have the following characteristics: (1) higher electrical and thermal conductivity than TE material, (2) the coefficient of thermal expansion (CTE) of the material is matched with the TE elements, (3) the deposited layer can be very thin for the reduction of contact resistances, (4) low interface resistance, (5) high stability for the working temperature, (6) stronger yield strength at operating temperature, and (7) good mechanical bonding with the TE layer (Liu W. et al., 2015; He et al., 2018).

**DESIGN AND APPLICATION OF μTEG**

**μTEG Design**

Unlike the traditional TEG with a large size, μTEG commonly works at small temperature differences for its small dimension and severer parasitic electrical/thermal resistances. These should be considered in the design of μTEG and its packaging. According to the different structures, the μTEG was classified into three types as follows (Yan et al., 2018).

Type 1—vertical structure (out-of-plane): μTEG with both vertical heat and current flow in Figure 14A.
Type 2—lateral structure (in-plane/planar): μTEG with both lateral heat and current flow in Figure 14B.
Type 3—hybrid structure: TEG with vertical heat and lateral current flow in Figure 14C.

Fabricated with sandwich structure, the vertical TEG was the traditional structure of μTEG and widely utilized in commercial TE devices. Recently, a series of vertical Si NWs modules and TEGs have been fabricated (Curtin et al., 2012; Tomita et al., 2018a; Lee et al., 2019). Generally, μTEGs with this structure are easy to design, and they have large output power and high conversion efficiency. However, the defects come from the difficult and expensive fabrication process, like the deep-etching in the top-down methods, or the well-controlled NW
FIGURE 14 | Three types of μTEG. (A) Vertical structure; (B) lateral structure; (C) hybrid structure. Reprint with permission from Yan et al. (2018).

synthesis and metal electrodes integration in the bottom-up methods (Zhan et al., 2018). The lateral structure μTEG, which is compatible with the CMOS process, is relatively easy to fabricate (Xie et al., 2010; Yu et al., 2012, 2015; Noroozi et al., 2017b). But the drawbacks lie in the comparatively low efficiency owing to high parasitic heat flux and low temperature difference. For that reason, the lateral structure is unable to be utilized in power generation and often applied in different sensors. As a compromise of the abovementioned two structures, the hybrid structure shows integrated advantages. In the hybrid structure, the heat flux from ambient flows vertically in a planar direction, and is ejected vertically from another side (Xie et al., 2010). Therefore, the hybrid structure μTEG is desirable to satisfy particular applications and the key for the optimization is the design of a heat flux path.

Moreover, the substrates are etched away to form thermally isolated Si NWs for high efficacy, resulting in a vulnerable structure and expensive fabrication cost. Generally, the high conversion efficiency is essential when the expensive specified heat source is applied, such as RTG, while power generation density is crucial for the heat source which is cheap or free, like waste heat (Zhan et al., 2018).

Performance and Application

In fact, the first generation of TEG, the radioisotope TEG, has been used during the last four decades for power supply by converting the thermal power generated by a radioisotope heat source to electricity for many planetary exploration missions. Unlike a solar power generator, the RTG can operate without sunlight. That advantage fits well with long (more than 10 years) and far-distanced missions (O’Brien et al., 2008).

The μTEGs are a terrific power source for existing and coming electronics considering their ubiquity, magnitude of heat dissipation, and the direct, stable, and non-pollutive energy conversion. The aim of μTEG research is to supply steady electricity power for those miniature electronic instruments. A comparison of the existing microgenerators and applications has been exhibited in Figure 15 (Iannacci, 2019). After the research into TEG and boom of electrical technology, μTEGs have come to be utilized in many fields, like business electronics, health electronics, and IoT (Haras and Skotnicki, 2018; Tomita et al., 2018a). For business electronics, the milestone application of μTEG was a TE watch named Thermatron which was introduced by Bulova in 1980; however it failed due to its unreliable battery and high price (Adams, 2019). A recent smart watch named Matrix Powerwatch II, which is powered by body temperature, has the like calorie counting, sleep tracker, and step counting (Powerwatch, 2020).

Heat dissipation from the human body has been considered as an excellent source of heat energy. As the skin on the wrist has a relatively constant temperature of 36.5°C, it would be possible to utilize this heat for wearable TEGs (Lv et al., 2016). Meanwhile, the temperature difference between the skin and the internal body can reach a maximum of 8°C, sufficient to generate a microwatt level of electricity with μTEG (Ben Amar et al., 2015). It can serve as an alternative power supply compared to other
conventional power sources in many wearable devices, especially with implant medical devices like pacemakers (Siddique et al., 2017). For IMD, the difficulty is the permanent operation or standby of the electronics with no secondary removal; body heat is a perfect endless source for those devices like pacemakers.

The increase of research into IoT has also promoted the application of µTEG. The IoT calls for smart, integrated, miniaturized, and low-energy wireless nodes, powered by non-renewable batteries in most cases. The most important part of IoT is the discrete wireless sensor networks (WSNs) which are distributed in different fields like intelligent buildings, medical treatment, monitoring, and security (Ghayvat et al., 2015). The low power dissipation (10–10⁴ µW/cm²) corresponds with the power supplied by µTEG (Noyana et al., 2019). A TE energy harvesting system for WSN has been designed with an input power of 84 µW (Guan et al., 2017). Designed for building energy management (BEM), a TEG-powered WSNs module has been built and characterized in a recent study, which shows the possibility for further application of µTEG for WSNs (Wang et al., 2013).

Some problems limited the application for µTEG and need better solutions. Above all, the conversion efficiency of energy is around 5–10% owing to the low ZT of TE materials (mostly <1), which is much lower than traditional generators and has no market competitiveness. Secondly, it is difficult to attain high temperature differences in daily life; for a wearable TEG, the typical ΔT is 5–15°C. Finally, a suitable external load is needed for load matching and power matching (Siddique et al., 2017).
More requirements of TEG can be illustrated by Figure 16, which is also essential for μTEG. A good TE power system should possess all three demands as a minimum: efficiency, effectiveness, and reliability (Liu W. et al., 2015). More detailed requirements should be considered like strong device bonding strength, excellent thermal stability, and chemical stability.

SUMMARY AND PROSPECT

In this review article, we have explored the basic conceptions in the fabrication of Si-based NW μTEG. The μTEG has a bright future as an efficient method for power supply in wireless microelectronic devices due to its energy recycle and convenience. However, there are still many problems that must be addressed before proceeding to large-scale application. Among those TE properties that influence $ZT$, thermal conductivity $\kappa$ is the most important parameter in the consideration for the design of μTEG with Si and SiGe NWs. Most research is focusing on the tuning of phonon thermal conductivity, which is dominant in semiconductors. Then the novel potential materials in Group IV have been stated; specifically we explain the superiority of Si and SiGe NWs as a candidate for TEs. Simple examples for the novel structure in the SiGe NWs e.g., superlattice (SL), core-shell (C-S), etc., have been presented for their possibility to further enhance the TE properties. The methods for fabrication are also introduced in this article, with the top-down and bottom-up methods illustrated and the detailed process generalized like MBE, RIE, and STL. After the process, the analysis and characterization of TE in different articles about the TE parameters are reviewed here, the commonly used 4-point probing for the electrical properties with I-V characteristic curve described and 3ω method for the thermal conductivity. Finally, we describe the existing and prospective applications for TEG-sourced devices, which are likely to be an enormous market in the near future. For the utilization of μTEG, IoT is a good carrier due to its miniature energy consumption. Also, flexible wearable devices and implantable medical devices are promising directions.

We believe more research is necessary to further enhance the TE properties and lower the cost of processing and power generating. From this research, Si and SiGe NW μTEGs have the potential to find their niche in daily life and in more complicated application scenarios.

AUTHOR CONTRIBUTIONS

YL and HR conceived and designed the manuscript. YL wrote the article. GW, MA-S, MP, and HR revised it. All authors contributed to the article and approved the submitted version.

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Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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