Abstract—In comparison to the conventional complementary pull-up and pull-down logic structure, the pass transistor logic (PTL) family reduces the number of transistors required to perform logic functions, thereby reducing both area and power consumption. However, this logic family requires inter-stage inverters to ensure signal integrity in cascaded logic circuits, and inverters must be used to provide each logical input signal in its complementary form. These inverters and complementary signals increase the device count and significantly degrade overall system efficiency.

Dual-gate ambipolar field-effect transistors natively provide a single-transistor XNOR operation and permit highly-efficient and compact circuits due to their ambipolar capabilities. Similar to PTL, logic circuits based on ambipolar field-effect transistors require complementary signals. Therefore, numerous inverters are required, with significant energy and area costs.

Ambipolar field-effect transistors are a natural match for PTL, as hybrid ambipolar-PTL circuits can simultaneously use these inverters to satisfy their necessity in both PTL and ambipolar circuits. We therefore propose a new hybrid ambipolar-PTL logic family that exploits the compact logic of PTL and the ambipolar capabilities of ambipolar field-effect transistors. Novel hybrid ambipolar-PTL circuits were designed and simulated in SPICE, demonstrating strong signal integrity along with the efficiency advantages of using the required inverters to simultaneously satisfy the requirements of PTL and ambipolar circuits. In comparison to the ambipolar field-effect transistors in the conventional CMOS logic structure, our hybrid full adder circuit can reduce propagation delay by 47%, energy consumption by 88%, energy-delay product by a factor of 9, and area-energy-delay product by a factor of 20.

Index Terms—Ambipolarity, Transmission Gate Logic, Pass Transistor Logic (PTL), Carbon Nanotube, Ambipolar Logic

I. INTRODUCTION

As technology scaling becomes increasingly challenging and expensive, novel device switching phenomena have the potential to revolutionize computing beyond conventional unipolar field-effect transistors (FETs) with a fixed charge polarity. In particular, dual-gate ambipolar FETs (DG-A-FETs) enable efficient computing through dynamic switching between $n$- and $p$-type [1]–[9]. Such DG-A-FETs can be implemented with a variety of materials that exhibit ambipolar transport, including carbon nanotubes (CNTs), silicon nanowires, graphene nanoribbons, and transition metal dichalcogenides [10]–[15]. Though this paper considers circuits designed with DG-A-FETs with CNTs (DG-A-CNTFETs) due to the existence of an effective SPICE-compatible device model, the general conclusions are expected to also apply to DG-A-FETs based on other ambipolar materials.

As illustrated in Fig. 1, the polarity gate (PG) voltage in a DG-A-FET determines the dominant carrier polarity while the control gate (CG) voltage modulates the current. Ambipolar transistors have been used in circuits based on the conventional complementary pull-up and pull-down logic family, enabling increased logical expressivity in compact circuits [12], [13]. In particular, the conventional complementary pull-up and pull-down logic family enables XOR and XNOR gates with only four transistors. However, these gates require complementary input signals, necessitating the use of a two-transistor inverter for each input. These additional inverters significantly increase the area and energy consumption, thereby reducing the benefits of using ambipolar transistors.

Pass transistor logic (PTL) is a well-established logic family that is designed to reduce the energy and area of logical computing systems by reducing the number of transistors required to perform logical functions [19]–[21]. However, its broad application in large-scale circuits is limited by the need for inverters to provide the external power required for signal integrity [22].

As both DG-A-FET logic and the PTL family require additional inverters for proper operation, this paper proposes a hybrid A-PTL family that simultaneously uses the inverters to satisfy the requirements for both PTL and DG-A-FET-based circuits. As the inverters provide both complementary signals and external power for signal integrity, their dual-purpose use makes PTL extremely well-suited for use with DG-A-FETs in compact and efficient logic circuits. This paper therefore describes the A-PTL family and explores the A-PTL design space to propose and analyze three A-PTL structures with distinct trade-offs in terms of area, speed, and energy. These A-PTL variants are shown to provide propagation delay reduction of up to 47% and energy savings of up to 88% in comparison to the conventional CMOS-like logic family with the same A-FETs, leading to a 9x reduction in EDP and 20x reduction in area-energy-delay product (AEDP).

II. BACKGROUND

In order to appreciate the potential benefits of using DG-A-FETs within the PTL family for large-scale computing systems, it is important to understand the potential and unique characteristics of these unconventional devices and of the PTL family.

A. Dual-Gate Ambipolar Carbon Nanotube Field-Effect Transistor

Though the high current density and tunable bandgap of low-dimensional materials such as CNTs have attracted significant attention, the presence of ambipolar transport has impeded attempts to use them to replace Si in unipolar FETs. However, this ambipolarity creates new opportunities for circuit design, as DG-A-FETs can be dynamically switched between $n$-type and $p$-type polarity.

In the device of Fig. 1 the PG voltage determines the channel polarity while the CG voltage modulates current flow through the channel. This ability to switch the transistor between electron and hole conduction by the dual independent gate control allows the transistor to have more expressive power, reducing the number of
devices required to perform logical operations [17]. In particular, the DG-A-FET of Fig. 2(a) natively provides a single-transistor XNOR operation and enables high-efficiency logical and neuromorphic computing systems [23].

B. Complementary Ambipolar Field-Effect Transistor Logic

When DG-A-FETs are used to implement logic circuits within a conventional complementary pull-up and pull-down logic structure, as in [17], transmission gates (TGs) with complementary inputs are used in the pull-up and pull-down networks to prevent $V_T$-drops [4]. For example, although a single DG-A-FET is able to implement the XNOR function, four DG-A-FETs are used to ensure signal integrity and fan-out as in Fig. 2(b). The requirement of the complementary transistor pair significantly increases the device count and hence the area cost and power consumption. Furthermore, since each transistor pair requires its input signal to be provided in a complementary form (both A and its complement are needed for A XNOR B), the overhead circuits and interconnects required to generate the complementary signal further reduce the benefits derived from utilizing transistor ambipolarity.

Compared to conventional CMOS logic with unipolar transistors, DG-A-FETs within a conventional complementary pull-up and pull-down logic structure implement complex logic functions with higher logical expressivity. However, both the extra transistors used for ambipolar TG pairs and the inverters required for generating complementary signals decrease the efficiency of using A-FETs in the conventional CMOS logic architecture. It is therefore worthwhile to explore other logic styles that are well-suited to logic with DG-A-FETs.

C. Pass Transistor Logic

PTL is a logic family designed to minimize the number of transistors required to implement any given logic function, thereby reducing area and power consumption. However, as there is no connection to a power supply, the energy for each PTL gate comes from its input, therefore necessitating the use of inverters to ensure signal integrity in cascaded circuits [19], [24]. Furthermore, as traditional PTL uses only NMOS transistors, there is a threshold voltage drop whenever a high voltage signal is transmitted; an additional PMOS transistor is therefore frequently added to provide a full voltage swing using TGs in complementary PTL (CPL), which further necessitates inverters to provide each logical input signal in its complementary form. This heavy use of inverters and the need to use complementary transistors drastically increases the device count, delay, and energy consumption of PTL circuits, inhibiting the development of computing systems based entirely on PTL.

PTL and CPL are therefore often used for specific logic functions within systems based primarily on the conventional complementary pull-up and pull-down logic structure. For example, multiplexing is particularly efficient with PTL, and PTL multiplexers are therefore frequently found within an otherwise conventional CMOS logic architecture. In that vein, previous work has proposed PTL and CPL multiplexers with DG-A-CNTFETs [25] as well as a PTL full adder with ambipolar silicon nanowire FETs [26]. These logic circuits, however, face the same challenges that have plagued other A-FETs and PTL: complementary input signals are required for functionality, requiring the heavy use of additional inverters. The area and energy costs of these inverters drastically decrease the efficiency, limiting the use of such circuits to particular logic functions within systems based primarily on the conventional complementary pull-up and pull-down logic structure. While previous DG-A-FET and PTL/CPL circuits are efficient for particular individual functions, novel approaches are required to enable a scalable logic family.

III. HYBRID AMBIPOLAR PASS TRANSISTOR LOGIC

The challenges facing both PTL and DG-A-FETs can be resolved by incorporating DG-A-FETs into a hybrid A-PTL family that can be scaled to large circuits and systems. In the proposed hybrid A-PTL family, the inverters required for complementary inputs and signal integrity simultaneously satisfy the needs of both DG-A-FETs and PTL, thereby amortizing the costs of these inverters across the benefits provided by both DG-A-FETs and PTL. Various hybrid A-PTL circuit styles are optimized for particular figures of merit, providing distinct advantages in large-scale circuits implemented entirely with hybrid A-PTL.

A. Basic Hybrid A-PTL Structure (Type I)

As illustrated in Fig. 3, the core concept of the proposed hybrid A-PTL family is the alternation between PTL-based computational circuits and buffering inverters. The entire system is composed solely of DG-A-FETs, with CPL-based computations performed by ambipolar transmission gate cores (A-TGCs) followed by two CMOS-style DG-A-FET inverters. The A-TGC performs logical operations based on the input data, and is succeeded by two inverters that ensure signal integrity and provide the complementary output signals for cascading stages. These buffering inverters provide energy from the power supply (rather than from the input as in PTL), thereby

![Fig. 2: Transistor-level schematic of XNOR gate with (a) single transistor, and (b) four transistors.](image)

![Fig. 3: Block diagram of the Type I hybrid A-PTL architecture illustrating the alternation between A-TGCs and buffering inverters.](image)
Fig. 4: Transistor-level schematic of the Type I hybrid-A-PTL one-bit full adder.

Fig. 5: (a) Block diagram of the Type II hybrid A-PTL style. (b) Transistor-level schematic of a Type II hybrid-A-PTL one-bit full adder, showing A-TGCs replaced by A-PTCs.

TABLE I: One-Bit Full Adder Area Comparison with Hybrid A-PTL Architecture

| Architecture | Device Count | Estimated Area Reduction |
|--------------|--------------|--------------------------|
| CMOS-like    | 28           | baseline                 |
| Type I       | 16           | 43%                      |
| Type II      | 12           | 57%                      |
| Type III     | 12           | 57%                      |

Boosting the fan-out and enabling large cascaded circuits without signal degradation. Furthermore, using DG-A-FETs to reduce the number of transistors in the PTL-style logic circuits reduces area, delay, and energy in comparison to PTL.

An example hybrid A-PTL circuit is illustrated in the schematic of Fig. 4, which will henceforth be referred to as the Type I cascading style. This one-bit requires eight transistors in the A-TGC and an additional eight transistors in the four inverters, for a total of 16. In comparison to the 28 DG-A-FETs required for a one-bit full adder in the conventional CMOS architecture, this represents a 43% reduction in area. Furthermore, as demonstrated in the simulations of section IV, this hybrid A-PTL full adder structure exhibits significant reductions in delay and energy consumption.

B. Alternative Hybrid A-PTL Structures (Types II & III)

Beyond the proposed Type I hybrid A-PTL style, the transistor count can be minimized further by reducing complementarity in either the A-TGC or buffering inverters. These two alternative logic styles make the following modifications:

- Type II: one transistor is removed from each TG pair within the A-TGC.

- Type III: one buffering inverter is removed following each A-TGC.

Each of these modifications directly causes a significant decrease in the circuit area, while also drastically impacting energy consumption and delay.

The Type II style is illustrated in Fig. 5(a) with each TG pair in the A-TGC replaced by an ambipolar pass transistor core (A-PTC) with a single pass transistor to reduce device count. As a single pass transistor cannot always provide a full voltage swing, the logical complexity of the Type II A-PTL is limited by the DG-A-FET threshold voltage drops from propagating a ‘1’ (‘0’) when the DG-A-FET has an n-type (p-type) channel. As demonstrated in section IV, the area reduction in this Type II structure therefore comes at the cost of increased delay, limiting its overall efficiency.

The Type III structure shown in Fig. 5(b) uses the same A-TGC structure as Type I, but one buffering inverter is removed. Therefore, the non-inverted output signals (Sum and $C_{OUT}$ in the full adder) drive cascaded stages directly, without passing through a buffering inverter. Like conventional CPL, this may prevent long chains of cascaded circuits because the energy of the entire CPL block comes from the initial input signals. Whereas the Type II style compromises signal integrity by having an asymmetric signal swing at the output of the A-PTC, the Type III style has reduced signal integrity due to the lack of isolation/buffering inverters between the input and output. As demonstrated in section IV, the removal of an inverter from the critical path gives the Type III style the lowest delays for circuits without high fan-out.

Table I summarizes the transistor count of one-bit full adders in each of the three styles. Compared to the CMOS-like one-bit full adder baseline, the proposed Type I style reduces the area by 43%, while Types II and III reduce the area by 57%. The reduced circuit symmetry with both Types II and III decreases the output slew rate, increasing the delay. However, this is compensating to varying degrees by reductions in the parasitic capacitances and, for Type III, the removal of an inverter from the critical path.

IV. Computational Performance & Efficiency

To evaluate the performance and efficiency of the proposed hybrid A-PTL styles, SPICE simulations have been performed to compare the various styles to the conventional complementary pull-up and
A. Comparison of One-Bit Full Adders

Fig. 7 shows the transient simulation waveforms of one-bit full adder circuits in the three hybrid A-PTL styles. To provide a reference that enables apples-to-apples comparisons of the circuit structures, the conventional CMOS-like 28-transistor one-bit full adder of [4] serves as a baseline. As shown in Figs. 4-6, the output of the A-TGC or A-PTC is fed to the CGs of the DG-A-FETs in the buffering inverters; the PGs of the DG-A-FETs in the inverters are connected to power supplies for DC biasing. Figs. 7(b) and (c) zoom in on transitions of both the Sum and $C_{OUT}$ output signals. These simulations clearly reveal that the Type III style provides the shortest delay, significantly faster than the baseline. The Type I and II styles have varying delays in each case, though the Type II style is clearly quite slow for computing $C_{OUT}$.

B. Control Gate vs. Polarity Gate Cascading

In all of the circuits that have thus far been discussed, the output of the A-TGC or A-PTC has been fed to the CGs of the DG-A-FETs within the inverters. With this CG cascading, the polarity of each DG-A-FET within the inverters is constant. Alternatively, this signal could be used to drive the PGs within the inverter DG-A-FETs, as shown in Fig. 8, thus broadening the design space. In the case of PG cascading, the polarity of the DG-A-FETs within the inverters is modulated by the outputs of the A-TGC or A-PTC while the CG input remains constant.

To directly compare CG and PG cascading, the transient waveforms with both CG and PG cascading are plotted together for the Type III hybrid A-PTL full adder in Fig. 10. As the non-inverted Sum and $C_{OUT}$ signals have not passed through an inverter, there is no difference between CG and PG cascading. For the inverted output...
Fig. 11: Transistor-level schematic of the hybrid A-PTL four-bit ripple-carry adder using the Type III style and PG cascading.

Fig. 12: Selected simulation waveforms of the Type III hybrid A-PTL four-bit ripple-carry adder with PG cascading.

signals, this comparison clearly shows that CG cascading provides shorter delay than PG cascading due to an earlier transition. However, the PG cascading has a higher output slew rate, leading to lower energy consumption.

C. Medium-Scale Circuit Analysis

To enable analysis more predictive of a large-scale system, four-bit hybrid A-PTL ripple-carry adders have been simulated with all three styles and both cascading approaches, for a total of six distinct circuits. As an example, the four-bit hybrid A-PTL ripple-carry adder using the Type III style with PG cascading is shown in Fig. 11. To broadly characterize the behavior across input combinations, a sequence of 1,000 operations was randomly generated and used as input signals.

A selection of the transient simulation waveforms is shown in Fig. 12. This four-bit full adder circuit has an additional carry-in bit such that it is composed of four one-bit full adders rather than three one-bit full adders and a half adder. As can be seen in the figure, the missing inverter from the Type III style leads to a propagation delay dependent on the input combination.

The performance and efficiency of all three hybrid A-PTL styles and both cascading approaches are analyzed in Fig. 13 based on the results for the four-bit full adder circuits. These results are compared to the conventional CMOS-style DG-A-FET circuit as a baseline in terms of average delay, energy consumption, EDP, and AEDP across the 1,000 input combinations. As can clearly be observed in the figure, the Type III hybrid A-PTL style is superior to the conventional baseline structure for all metrics.

The asymmetry between the CG and PG of the DG-A-FET devices leads to a trade-off between speed and energy consumption. For all three hybrid A-PTL styles, CG cascading is always faster than PG cascading; however, the circuits with PG cascading consume less energy and therefore result in a lower EDP and AEDP. Therefore, CG cascading is preferred when speed is critical, while PG cascading is more suitable to low-power system design.

While the delay of the Type I and III styles can be significantly less than the baseline, the type II style is significantly slower. The Type I and III styles also provide enormous reductions in energy consumption, with the Type III style providing an 8x reduction when using PG cascading. The energy consumption of the Type II style strongly depends on the cascading approach, with PG cascading producing an energy consumption 4x less than CG cascading. The lack of complementary transistors in the Type II A-PTC results in lower signal integrity than with the A-TGC used in Types I and III, leading to increased EDP and AEDP for Type II.

Hybrid A-PTL drastically improves the overall computing efficiency, with the Type III style with PG cascading providing a 9x
improvement in EDP and a 20x improvement in AEDP. These figures of merit leverage the slightly improved delay and massively improved energy consumption, with the AEDP further incorporating the 57% reduction in area (Table I). While the Type I style is also promising, the reduced transistor count and simplified circuit structure provide the Type III style the greatest potential for compact and efficient circuits.

V. CONCLUSIONS

DG-A-FETs are naturally compatible with PTL, and the proposed hybrid A-PTL family leverages the advantages of both DG-A-FETs and PTL by applying their required inverters in a manner that efficiently amortizes their costs. This A-PTL family enables device count to be reduced by half, and increases energy-efficiency by an order of magnitude. Comparisons among the three hybrid A-PTL styles proposed in this work indicate that the Type III style is superior, thanks to the complementarity of the A-TGC and the removal of the second inverter. Furthermore, CG cascading is shown to be faster than PG cascading, while PG cascading is shown to be more energy-efficient than CG cascading. By comparing a medium-scale hybrid A-PTL circuit to one realized with DG-A-FETs in the conventional CMOS-like logic style, the hybrid A-PTL system is shown to provide up to 47% decrease in delay, 57% reduction in area, 88% reduction in energy consumption, 9x reduction in EDP, and 20x reduction in AEDP. These results therefore greatly advance the already-promising prospects for efficient computing systems with ambipolar transistors.

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Fig. 13: Performance and efficiency comparison of the proposed hybrid A-PTL styles to the conventional CMOS-style baseline. These results are based on simulations of the four cascaded full adders.
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