PORTING A SPARSE LINEAR ALGEBRA MATH LIBRARY TO INTEL GPUs

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ABSTRACT

With the announcement that the Aurora Supercomputer will be composed of general purpose Intel CPUs complemented by discrete high performance Intel GPUs, and the deployment of the oneAPI ecosystem, Intel has committed to enter the arena of discrete high performance GPUs. A central requirement for the scientific computing community is the availability of production-ready software stacks and a glimpse of the performance they can expect to see on Intel high performance GPUs. In this paper, we present the first platform-portable open source math library supporting Intel GPUs via the DPC++ programming environment. We also benchmark some of the developed sparse linear algebra functionality on different Intel GPUs to assess the efficiency of the DPC++ programming ecosystem to translate raw performance into application performance. Aside from quantifying the efficiency within the hardware-specific roofline model, we also compare against routines providing the same functionality that ship with Intel’s oneMKL vendor library.

Keywords  Sparse Matrix Vector Product · Krylov Solvers · GPUs · Intel · oneAPI · DPC++

1 Introduction

For a long time, Intel GPUs were almost exclusively available as integrated component of Intel CPU architectures. However, at latest with the announcement that the Aurora Supercomputer will be composed of general purpose Intel CPUs complemented by discrete Intel GPUs and the deployment of the oneAPI ecosystem in cooperation with CodePlay, Intel has committed to enter the arena of discrete high performance GPUs. Other than integrated GPUs, discrete GPUs are usually not exclusively intended to accelerate graphics, but they are designed to also deliver computational power that can be used, e.g., for scientific computations. On the software side, the oneAPI ecosystem promoted by Intel intends to provide a platform for C++ developers to develop code in the DPC++ language that can be executed on any Intel device, including CPUs, GPUs, and FPGAs.

In 2020, Intel released the Intel generation 12 Intel® Iris® Xe Graphics GPU codename DG1, an architecture more powerful than the Intel generation 9 integrated GPU deployed in many systems, and with full support of the oneAPI ecosystem. As this GPU may be spearheading the development of Intel’s discrete GPU line, we assess the performance this GPU can achieve in numerical calculations. Specifically, we develop a DPC++ backend for the GINKGO open source math library, and benchmark the developed functionality on different Intel GPU architectures. As GINKGO’S main focus is on sparse linear algebra, we assess the performance of the sparse matrix vector product (SPMV) and iterative Krylov solvers within the hardware-specific performance limits imposed by arithmetic peak performance and memory bandwidth. We consider both double precision and single precision computations and compare against Intel’s vendor library oneMKL designed for the oneAPI ecosystem.
Up to our knowledge, we are the first to present the functionality and performance of an open source math library on Intel discrete GPUs. We structure the paper into the following sections: In Section 2 we introduce the GINKGO open source library and its design for platform portability. In Section 3 we introduce the oneAPI ecosystem and the DPC++ programming environment. In Section 4 we discuss some aspects of adding a DPC++ backend to GINKGO for portability to Intel GPUs. For convenience, we briefly recall in Section 5 the functionality and some key aspects of the algorithms we utilize in our experimental evaluation. This performance evaluation is presented in Section 6: we initially benchmark the both the Intel generation 9 and 12 GPUs in terms of feasible bandwidth and peak performance to derive a roofline model, then evaluate the performance of GINKGO’S SpMV kernels (also in comparison to the SpMV routine available in the oneMKL vendor library), and finally assess the performance of GINKGO’S Krylov solvers. For completeness, we include performance results using GINKGO’S other backends on high-end AMD and NVIDIA hardware to demonstrate the (performance) portability of the GINKGO library. We conclude with a summary of the porting and performance experiences on the first discrete Intel GPU in Section 7.

2 GINKGO design

GINKGO is a GPU-focused cross-platform linear operator library focusing on sparse linear algebra [3, 2]. The library design is guided by combining ecosystem extensibility with heavy, architecture-specific kernel optimization using the platform-native languages CUDA (NVIDIA GPUs), HIP (AMD GPUs), or OpenMP (Intel/AMD/ARM multicore) [4]. The software development cycle ensures production-quality code by featuring unit testing, automated configuration and installation, Doxygen code documentation, as well as a continuous integration and continuous benchmarking framework [1]. GINKGO provides a comprehensive set of sparse BLAS operations, iterative solvers including many Krylov methods, standard and advanced preconditioning techniques, and cutting-edge mixed precision methods [6].

A high-level overview of GINKGO’s software architecture is visualized in Figure 1. The library design collects all classes and generic algorithm skeletons in the “core” library which, however, is useless without the driver kernels available in the “omp”, “cuda”, “hip”, and “reference” backends. We note that “reference” contains sequential CPU kernels used to validate the correctness of the algorithms and as reference implementation for the unit tests realized using the googletest [7] framework. We note that the “cuda” and “hip” backends are very similar in kernel design, and we therefore have “shared” kernels that are identical for the NVIDIA and AMD GPUs up to kernel configuration parameters [14]. Extending GINKGO’s scope to support Intel GPUs via the DPC++ language, we add the “dpcpp” backend containing the kernels in the DPC++ language.

To reduce the effort of adding a DPC++ backend, we use the same base components of GINKGO like config, binding, executor, types and operations, which we only extend and adapt to support DPC++.

- **config**: hardware-specific information like warp size, lane_mask_type, etc.;
- **binding**: the C++ style overloaded interface to vendors’ BLAS and sparse BLAS library and the exception calls of the kernels not implemented;

![Figure 1: The GINKGO library design overview.](image)
• executor: the “handle” controlling the kernel execution, all form of interactions with the hardware such as memory allocations and the ability to switch the execution space (hardware backend);
• types: the type of kernel variables and the conversion between library variables and kernel variables;
• operations: a class aggregating all the possible kernel implementations such as reference, omp, cuda, hip, and dpc++, which allows to switch between implementations at runtime when changing the executor type used.

3 The oneAPI Programming Ecosystem

oneAPI is an open and free programming ecosystem which aims at providing portability across a wide range of hardware platforms from different architecture generations and vendors. The oneAPI software stack is structured with the new DPC++ programming language at its core, accompanied by several libraries to ease parallel application programming.

DPC++ is a community-driven (open-source) language based on the ISO C++ and Khronos’ SYCL standards. The concept of DPC++ is to enhance the SYCL ecosystem with several additions that aim at improving the performance on modern hardware, improving usability, and simplifying the porting of classical CUDA code to the DPC++ language. Compared to SYCL, two relevant features of the DPC++ ecosystem are: 1) DPC++ introduces a new subgroup concept which can be used inside kernels. This concept is equivalent to CUDA subwarps (or SIMD on CPUs) and allows optimized routines such as subgroup based shuffles. In the GINKGO library, we make extensive use of this capability to boost the performance. 2) DPC++ adds a new Unified Shared Memory (USM) model which provides new malloc_host and malloc_device operations to allocate memory which can either be accessed both by host or device, or respectively accessed by a device only. Additionally, the new SYCL queue extensions facilitate the porting of CUDA code as well as memory control. Indeed, in pure SYCL, memory copies are entirely asynchronous and hidden from the user, since the SYCL programming model is based on tasking with automatic discovery of task dependencies.

Another important aspect of oneAPI and DPC++ is that they adopt platform portability as the central design concept. Already the fact that DPC++ is based on SYCL (which leverages the OpenCL’s runtime and SPIRV’s intermediate kernel representation) provides portability to a variety of hardware. On top of this, DPC++ develops a plugin API which allows to develop new backends and switch dynamically between them. Currently, DPC++ supports the standard OpenCL backend, a new Level Zero backend which is the backend of choice for Intel hardware, and an experimental CUDA backend for targeting CUDA-enabled GPUs. As our goal is to provide high performance sparse linear algebra functionality on Intel GPUs, we focus on the Intel Level Zero backend of DPC++.

In Listing 1, we show a minimal example of a SYCL/DPC++ code in a classical use case. In line 10-11, previously declared data is wrapped into a `sycl::buffer` to enable automatic memory management. In this example, the `sycl::queue` declared in line 14 automatically selects the execution hardware. In general, the hardware selection can also be controlled explicitly. In line 17-28, the submission of a kernel is controlled through a command group handler. This allows to define accessors for the data in lines 19 and 20. These accessors declare the data access policy of the previous buffers and allow the runtime to automatically infer which data transfers (host/device) are required. Lines 22-27 contain the actual kernel declaration. The accessors are used to write to the previous buffers. Taking the C++ principles, at the end of the kernel, DPC++ automatically transfers the buffers back to the vectors A, B, destroys the buffers and synchronizes the queue. As a result, after kernel completion, the (modified) vectors A and B can again be accessed transparently, see lines 31-34.

4 Porting to the DPC++ ecosystem

Porting CUDA code to the DPC++ ecosystem requires to acknowledge that the SYCL-based DPC++ ecosystem is expressing algorithms in terms of tasks and their dependencies, which requires a fundamentally-different code structure. For the porting process, Intel provides the “DPC++ Compatibility Tool” (DPCT) that is designed to migrate CUDA code into compilable DPC++ code. DPCT is not expected to automatically generate a DPC++ “production-ready” executable code, but “ready-to-compilation” and it requires the developer’s attention and effort in fixing converting issues and tuning it to reach performance goals. However, with oneAPI still being in its early stages, DPCT still has

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[1] https://spec.one Api.com/versions/latest/index.html
[2] Both extensions are now also part of the SYCL 2020 Provisional Specification: https://www.khronos.org/news/press/khronos-releases-sycl-2020-provisional-specification
[3] https://intel.github.io/llvm-docs/PluginInterface.html
[4] https://spec.one Api.com/level-zero/latest/core/INTRO.html

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some flaws and failures, and we develop a customized porting workflow using the DPC++ Compatibility Tool at its core, but embedding it into a framework that weakens some DPCT prerequisites and prevents incorrect code conversion. In general, DPCT requires not only knowledge of the functionality of a to-be-converted kernel, but also knowledge of the complete library and its design. This requirement is hard to fulfill in practice, as for complex libraries, the dependency analysis may exceed the DPCT capabilities. Additionally, many libraries do not aim at converting all code to DPC++, but only a subset to enable the dedicated execution of specific kernels on DPC++-enabled accelerators. In Section 4.1, we demonstrate how we isolate kernels to be converted by DPCT from the rest of the library. Another flaw of the early version of the DPCT is that it typically fails to convert CUDA code making use of atomic operations or the cooperative group functionality. As GINKGO implementations aim at executing close to the hardware-induced limits, we make heavy use of atomic- and cooperative group operations. In Section 4.2 we demonstrate how we prevent DPCT from executing an incorrect conversion of these operations such that we can convert them using a customized script. To simplify the maintenance of the platform-portable GINKGO library, our customized porting workflow also uses some abstraction to make the DPC++ code in this first version look more similar to CUDA/HIP code. We note that this design choice is reflecting that the developers of GINKGO are currently used to designing GPU kernels in CUDA, but it may not be preferred by developers used to programming in task-based languages. We elaborate on how we preserve much of the CUDA/HIP code style in Section 4.3.

4.1 Isolated Modification

Unfortunately, DPCT needs to know the definition of all functions related to the target file. Otherwise, when running into a function without definition in the target file, DPCT returns an error message. Furthermore, DPCT by default converts all files related to the target file containing any CUDA code that are located in the same folder like the target file. To prevent DPCT from converting files that we do not want to be converted, we have to artificially restrict the conversion to the target files. We achieve this by copying the target files into a temporary folder and considering the rest of the GINKGO software as a system library. After the successful conversion of the target file, we copy the file back to the correct destination in the new DPC++ submodule.

By isolating the target files, we indeed avoid additional changes and unexpected errors, but we also lose the DPCT ability to transform CUDA kernel indexing into the DPC++ `nd_item<3>` equivalent. As a workaround, we copy simple headers to the working directory containing the thread_id computation helper functions of the CUDA code such that DPCT can recognize them and transform them into the DPC++ equivalent. Unfortunately, this workaround works well

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5 Also files in subfolders are automatically converted by DPCT if they contain CUDA code.
only if DPCT converts all code correctly. If DPCT fails to convert some files or function definitions live outside the
target files, we need to add a fake interface. Examples where the DPCT conversion does not meet our requirements
are our custom DPC++ cooperative group interface and the DPC++ CUDA-like dim3 interface which allows to use
CUDA-like block and grid kernel instantiation instead of the DPC++ nd_range. For those, we prevent DPCT from
applying any conversion steps but keep DPCT’s functionality to add the nd_item<3> launch parameters.

4.2 Workaround for Atomic Operations and Cooperative Groups

DPC++ provides a subgroup interface featuring shuffle operations. However, this interface is different from CUDA’s
cooporative group design as it requires the subgroup size as a function attribute and does not allow for different subgroup
sizes in the same global group. Based on the DPC++ subgroup interface, we implement our own DPC++ cooperative
group interface. Specifically, to remove the need for an additional function attribute, we add the item_ct1 function
argument into the group constructor. As the remaining function arguments are identical to the CUDA cooperative group
function arguments, we therewith achieve a high level of interface similarity.

A notable difference to CUDA is that DPC++ does not support subgroup vote functions like “ballot”, “any”, or other
group operations yet. To emulate this functionality, we need to use a subgroup reduction or some algorithms provided
by the oneAPi groups to emulate these vote functions in a subgroup setting. This lack of native support may affect the
performance of kernels relying on these subgroup operations. We visualize the workflow we use to port code making
use of the cooperative group functionality in Figure 2. This workflow composes four steps:

1. Origin: We need to prepare an alias to the cooperative group function such that DPCT does not catch the
keyword. We create this alias in a fake cooperative group header we only use during the porting process.

2. Adding Interface: As explained in Section 4.1, we need to isolate the files to prevent DPCT from changing
other files. During this process we add the simple interface including threadIdx.x and make use of the alias
function. Note that for the conversion to succeed, it is required to return the same type as the original CUDA
type, which we need to extract from the CUDA cooperative group function this_thread_block.

3. DPCT: Apply DPCT on the previously prepared files. As we add the threadIdx.x indexing to the function,
DPCT will automatically generate the nd_item<3> indexing for us.

4. Recovering: During this step, we change the related cooperative group functions and headers to the actual
DPC++ equivalent. We implement a complete header file which ports all the cooperative group functionality
to DPC++.

We show in Figure 2 the final result of the porting workflow on a toy example featuring the use of cooperative groups.
For the small example code in Figure 2a, if we do not isolate the code, DPCT will throw an error like Figure 2b once
encountering the cooperative group keyword. A manual implementation of the cooperative group equivalent kernel
is shown in Figure 2c. Our porting workflow generates the code shown in Figure 2d which is almost identical to the
original CUDA code Figure 2a.

The conversion of CUDA atomics to DPC++ atomics is challenging as the conversion needs to recognize the data
location and decide whether the DPC++ atomics operate on local or global memory. DPCT generally succeeds in this
automated memory detection, however, there are two aspects that require us to create a workaround: 1) at the time of
writing, DPCT fails to correctly convert atomic operations on local memory and 2) DPC++ does not provide atomics
for complex floating point numbers. We prevent DPCT from applying any conversion of atomic operations and add a
customized conversion to our preprocessing script. For this to work, we manually ported the atomic functions from
CUDA to DPC++ in a specific header file which is properly added during the postprocessing step.

4.3 Workaround for Code Similarity

GINKGO was originally designed as a GPU-centric sparse linear algebra library using the CUDA programming language
and CUDA design patterns for implementing GPU kernels. The GINKGO HIP backend for targeting AMD GPUs was
deployed for production in early 2020. The next step is to support Intel GPUs via a DPC++ backend. Thus, for historic
reasons and simplified maintenance, we prefer to keep the coding style of the initial version of the DPC++ backend of
GINKGO similar to the CUDA coding style. We acknowledge that this design choice may narrow down the tasking
power of the SYCL language, but consider this design choice as acceptable since task-based algorithms are currently
outside the focus of the GINKGO library at the backend level. However, the GINKGO library design allows to move
closer to the SYCL programming style at a later point if the algorithm properties favor this. For now, we aim for a

6We reported this issue to the Intel Development Team and they are working on a bugfix.
7Atomic operations on complex numbers is correct only if a single modification is applied at a time.
Figure 2: Summary of the workflow used to port the cooperative groups functionality and isolating effort such that we get the correct converted DPC++ codes.

(a) CUDA small cooperative group example
(b) DPCT conversion fails and reports error
(c) Manual DPC++ subgroup implementation. The orange boxes are the main difference from CUDA
(d) The result converted by our porting script

Figure 3: The cooperative group example
high level of code similarity by not only adding the customized cooperative group interface as discussed in Section 4.2, but also adding a dim3 implementation layer for DPC++ kernel launches that uses the same parameters and parameter order like CUDA and HIP. The interface layer simply reverses the launch parameter order in a library-private member function.

Despite adding a dim3 helper to use the grid and block notation from CUDA, several differences are left when calling CUDA and DPC++ kernels as in Figure 4. One fundamental difference between the CUDA/HIP ecosystem and DPC++ is that the latter handle the static/dynamic memory allocation in the main component. CUDA and HIP handle the allocation of static shared memory inside the kernel and the allocation of dynamic shared memory in the kernel launch parameters. Another issue is that widely different syntax are used to call CUDA and DPC++ kernels, since DPC++ relies on a hierarchy of calls first to a queue, then a parallel instantiation. For consistency, we add another layer that abstracts the combination of DPC++ memory allocation and DPC++ kernel invocation away from the user. This enables a similar interface for CUDA, HIP, and DPC++ kernels for the main component, and shared memory allocations can be perceived as a kernel feature, see Figure 5. The purple block (additional_layer_call) in Figure 5 has the same structure as the gray block (cuda_kernel_call) in the left side of Figure 4. Our script will convert the code from the left side of Figure 4 to the right side of Figure 5 by adding the corresponding additional layer automatically.

Figure 4: Hierarchical view of usual CUDA (left) and DPC++ (right) kernel call and parameters.

5 Central Sparse Linear Algebra Functionality

An important routine in sparse linear algebra is the sparse matrix product (SpMV). This kernel reflects how a discretized linear operator acts on a vector, and therewith plays the central role in the iterative solution of linear problems and eigenvalue problems. Popular methods based on the repetitive application of the SpMV kernel are Krylov subspace solver such as Conjugate Gradient (CG), GMRES, or BiCGSTAB, and the PageRank algorithm based on the Power Iteration. The SpMV kernel is also a key routine in graph analytics as it can be used to identify all immediate neighbors of a node or a set of nodes.

The sparse data format used to store the discretized matrix and the kernel processing scheme of an SpMV kernel are usually optimized to the hardware characteristics and the matrix properties. In particular on SIMD-parallel architectures like GPUs, the optimization balances between minimization of the matrix memory footprint and efficient parallel processing. In the performance evaluation in this paper, we consider two sparse matrix formats: 1) the “coordinate format” (COO) that stores all nonzero entries (and only those) of the matrix along with their column-indices and row-indices, and the “compressed sparse row” (CSR) format that reduces the memory footprint of the COO format further by replacing the explicit row-indices with pointers to the first element in each row of a row-sorted COO matrix. We focus on these popular matrix formats not only because of their widespread use, but also because Intel’s oneMKL library provides a heavily-optimized CSR-SpMV routine for Intel GPUs. For a theoretical analysis of the arithmetic intensity of the sparse data formats, one usually simplifies the CSR memory footprint as 1 floating point value + 1 index value per nonzero entry (8 Byte for single precision CSR, 12 Byte for double precision CSR) and the COO memory...
footprint as 1 floating point value + 2 index values per nonzero entry (12 Byte for single precision CSR, 16 Byte for double precision CSR).

Aside from the SpMV kernel which forms the backbone of many algorithms, in the present performance evaluation we also consider iterative sparse linear system solvers that are popular in scientific computing. Specifically, we consider the Krylov solvers CG, BiCGSTAB, CGS, and GMRES. All these solvers are based on the principle of successively building up a Krylov search space and approximating the solution in the Krylov subspace. While the generation of the Krylov search directions is specific to the distinct solvers and realized via a combination of orthogonalizations and vector updates, all solvers heavily rely on the SpMV kernel. All solvers except the GMRES solver are based on short recurrences, that is, the new Krylov search direction is only orthogonalized against the previous search direction [12]. Conversely, GMRES stores all search directions, and each new search direction is orthogonalized against all previous search direction [11]. Therefore, the orthogonalization plays a more important role in the GMRES algorithm. Another difference is that all algorithms except the CG algorithm are designed to solve general linear problems, while the CG algorithm is designed to solve symmetric positive definite problems. For a more comprehensive background on the Krylov solvers we consider, we refer the reader to [12].

6 Experimental Performance Assessment

6.1 Experiment Setup

In this paper, we consider two Intel GPUs: the generation 9 (GEN9) integrated GPU UHD Graphics P630 with a theoretical bandwidth of 41.6 GB/s and the generation 12 Intel® Iris® Xe Max discrete GPU (GEN12), which features 96 execution units and a theoretical bandwidth of 68 GB/s. To better assess the performance of either GPUs, we include in our analysis the performance we can achieve in bandwidth tests, performance tests, and sparse linear algebra kernels.

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https://ark.intel.com/content/www/us/en/ark/products/211013/intel-iris-xe-max-graphics-96-eu.html
We note that the GEN12 architecture lacks native support for IEEE 754 double precision arithmetic, and can only emulate double precision arithmetic. Obviously, emulating double precision arithmetic provides significantly lower performance. Given that native support for double precision arithmetic is expected for future Intel GPUs and using the double precision emulation would artificially degrade the performance results while not providing insight whether GINKGO’s algorithms are suitable for Intel GPUs, we use single precision arithmetic in the performance evaluation on the GEN12 architecture. The DPC++ version we use in all experiments is Intel oneAPI DPC++ Compiler 2021.1 (2020.10.0.1113). All experiments were conducted on hardware that is part of the Intel DevCloud.

Figure 6: Performance evaluation of the Intel GPUs using the BabelStream benchmark. The bandwidth analysis on the GEN9 architecture (left) uses IEEE 754 double precision values, the bandwidth analysis on the GEN12 architecture (right) uses IEEE 754 single precision values.

Figure 7: Experimental performance roofline of the Intel GPUs using the mixbench benchmark for the GEN9 (left) and GEN12 (right) GPUs.

6.2 Bandwidth Tests and Roofline Performance Model

Initially, we evaluate the two GPUs in terms of architecture-specific performance bounds. For that purpose, we use the BabelStream [5] benchmark to evaluate the peak bandwidth, and the mixbench [9] benchmark to evaluate the arithmetic performance in different precision formats and derive a roofline model [16]. In Figure 6 we visualize the bandwidth we achieve for different memory-intense operations. On both architectures, the DOT kernel requiring a global synchronization achieves lower bandwidth than the other kernels. We furthermore note that the GEN12 architecture achieves for large array sizes about 58 GB/s, which is about 1.6 × the GEN9 bandwidth (37 GB/s).

In Figure 7 we visualize the experimental performance roofline for the two GPU architectures. The GEN9 architecture achieves about 105 GFLOP/s, 430 GFLOP/s, and 810 GFLOP/s for IEEE double precision, single precision, and half precision arithmetic, respectively. The GEN12 architecture does not provide native support for IEEE double precision and the double precision emulation achieves only 8 GFLOP/s, which is significantly below the GEN9 performance. On the other hand, the GEN12 architecture achieves 2.2 TFLOP/s and 4.0 TFLOP/s for single precision and half precision floating point operations.

GINKGO is designed to compile for IEEE 754 double precision arithmetic, single precision arithmetic, double precision complex arithmetic, and single precision complex arithmetic.
6.3 SpMV Performance Analysis

Next, we turn to evaluating the performance of numerical functionality on the Intel GPUs. All SpMV experimental performance data we report reflects the average of 10 kernel repetitions after 2 warmup kernel launches. In Figure 8, we visualize the performance of the CSR and COO SpMV kernels of the GINKGO library along with the performance of the CSR SpMV kernel from the oneAPI library. Each dot represents the performance for one of the test matrices of the Suite Sparse Matrix Collection [13]. On the GEN9 GPU, we run these benchmarks using IEEE 754 double precision arithmetic. GINKGO’s CSR SpMV kernel and the CSR SpMV kernel of Intel’s oneMKL library achieve similar performance, while GINKGO’s COO SpMV generally achieves lower performance. Assuming an arithmetic intensity of 1/6 (2 FLOP / 12 Byte) for the double precision CSR SpMV and 1/8 (2 FLOP / 16 Byte) for the double precision COO SpMV, we can derive for the GEN9 architecture (experimental peak bandwidth 37 GB/s) an upper bound for SpMV performance of 6 and 4.6 GFLOP/s respectively. This theoretical upper bound does neither account for the row-pointer overhead in the CSR format nor for the read and write access to the vector. Hence, the experimental performance achieving 5.1 GFLOP/s (CSR) and 3.8 GFLOP/s (COO) indicate the high efficiency of the SpMV kernel implementations.

Given the lack of native IEEE 754 double precision support, we use IEEE 754 single precision in the performance evaluation on the GEN12 architecture. Ignoring the access to the vectors and the CSR row-pointer, the arithmetic intensity of the SpMV routines becomes 1/4 (2 FLOP / 8 Byte) for the single precision CSR SpMV and 1/6 (2 FLOP / 12 Byte) for the single precision COO SpMV. With the experimental bandwidth peak of 58 GB/s, we derive the
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| Matrix       | Origin                  | Size (n) | Nonzeros (nz) |
|--------------|-------------------------|----------|---------------|
| rajat31      | Circuit Simulation Problem | 4,690,002 | 20,316,253    |
| atmosmodj    | CFD Problem             | 1,270,432 | 8,814,880     |
| nlpkkt160    | Nonlinear Programming Problem | 8,345,600 | 225,422,112   |
| thermal2     | Unstructured FEM        | 1,228,045 | 8,580,313     |
| CurlCurl_4   | 2nd order Maxwell       | 2,380,515 | 26,515,867    |
| Bump_2911    | 3D Geomechanical Simulation | 2,911,419 | 127,729,899   |
| Cube_Coup_dt0| 3D Consolidation Problem | 2,164,760 | 124,406,070   |
| StocF-1456   | Flow in Porous Medium   | 1,465,137 | 21,005,389    |
| circuit5M    | Circuit Simulation Problem | 5,558,326 | 59,524,291    |
| FullChip     | Circuit Simulation Problem | 2,987,012 | 26,621,990    |

Table 1: Test matrix along with key characteristics.

Theoretical performance limits of 14.5 GFLOP/s and 9.7 GFLOP/s for the single precision CSR and COO SpMV kernels, respectively. The experimental data presented in Figure 8b reveals that both the CSR and COO SpMV routines from GINKGO and the CSR SpMV kernel shipping with Intel’s oneAPI library achieve performance close to this theoretical performance limit.

![Figure 9: Performance evaluation of GINKGO’s Krylov solvers on the Intel GPUs.](image)

10 At the point of writing, oneMKL CSR can only operate on shared memory on the GEN12 architecture and oneMKL does not support the COO SpMV operation yet.
6.4 Krylov Solver Performance Analysis

We now turn to complete linear solver applications as they are typical for scientific simulation codes. We run the solver experiment for 1,000 solver iterations after a warm-up phase. The iterative Krylov solvers we consider all have the SpMV kernel as central building block, and we use GINKGO’s COO SpMV kernel in the solver performance assessment. For this experiment, we select a set of test matrices from the Suite Sparse Matrix Collection that are orthogonal in their characteristics and origin, see Table 1. The upper graph in Figure 9 visualizes the performance for the Krylov solvers on the GEN9 architecture. All solvers achieve between 1.5 GFLOP/s and 2.5 GFLOP/s depending on the test matrix. We notice that the performance differences in-between the solvers are quite small compared to the performance differences for the distinct problems. The lower graph in Figure 9 visualizes the performance for the Krylov solvers on the GEN12 architecture. We recall that GEN12 does not provide native support for IEEE double precision computations, and we therefore run the solver benchmarks in IEEE single precision. Overall, in this experiment, the GINKGO solvers achieve between 5 GFLOP/s and 9 GFLOP/s for the distinct systems. We note that all Krylov solvers based on short recurrences are very similar in terms of performance, while the performance of the GMRES solver is usually significantly lower. This may be due to the fact that the GMRES algorithm requires solving the Hessenberg system, and some needed functionality not yet being supported on the GEN12 architecture by oneAPI. The developed workaround occurs to achieve lower performance.

6.5 Platform Portability

Finally, we want to take a look at the platform portability of GINKGO’s functionality, and see whether the “dpcpp” backend can provide the same efficiency like the “cuda” and “hip” backends. For that, we do not focus on the absolute performance the functionality achieves on GPUs from AMD, NVIDIA, and Intel, but the relative performance taking the theoretical performance limits reported in the GPU specifications as baseline. This approach reflects the aspect that the GPUs differ significantly in their performance characteristics, and that Intel’s OneAPI ecosystem and Intel’s high performance GPU architectures still being under active development and not yet having reached the maturity level of other GPU computing ecosystems. At the same time, reporting the performance relative to the theoretical limits allows to quantify the suitability of GINKGO’s algorithms and efficiency of GINKGO’s kernel implementations for the distinct GPU architectures. It may also indicate the performance we can expect for GINKGO’s functionality when scaling up the GPU performance. In Figure 10 we report the relative performance of different SpMV kernels on the AMD Radeon VII (“hip” backend), the NVIDIA V100 (“cuda” backend), and the Intel GEN9 and Intel GEN12 GPUs (both “dpcpp” backend).

As expected, the achieved bandwidth heavily depends on the SpMV kernel and the characteristics of the test matrix. Overall, the performance figures indicate that the SpMV kernels achieve about 90% of peak bandwidth on A100 and GEN12, but about 60-70% of peak bandwidth on Radeon VII and GEN9. At the same time, we notice that on the GEN12, the performance of the oneMKL CSR SpMV to be inconsistent, largely outperforming GINKGO’s SpMV kernels for some cases, but underperforming for others. Overall, GINKGO’s SpMV kernels are on all platforms competitive to the vendor libraries, indicating the validity of the library design and demonstrating good performance portability.

7 Summary and Outlook

In this paper, we have presented an open source math library featuring a DPC++ backend to execute on Intel GPUs. We elaborated on the porting effort and the workarounds we implemented to enable DPC++ support. We also evaluated the raw performance of different Intel GPU generations and investigated how this raw performance translates into the developed basic sparse linear algebra operations and sparse iterative solvers. The performance analysis revealed that DPC++ allows to achieve high efficiency in terms of translating raw performance into mathematical algorithms. The portability analysis shows GINKGO’s performance portability on modern HPC platforms. Future work will focus on running the platform-portable DPC++ kernels on AMD GPUs and NVIDIA GPUs and compare the kernel performance with the performance of kernels written in the vendor-specific programming languages HIP and CUDA, respectively. We failed to include the work in this paper as at the time of writing, platform portability of DPC++ is not yet enabled.
Figure 10: SpMV kernel bandwidth relative to the peak bandwidth for SpMV kernels available in the Ginkgo open source library and vendor libraries on the AMD, NVIDIA, and Intel GPUs.

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