Memristor-Based Neural Network Circuit of Delay and Simultaneous Conditioning

XINYU XU, WEILIN XU, BAOLIN WEI, AND FANGRONG HU

Guangxi Key Laboratory of Precision Navigation Technology and Application, Guilin University of Electronic Technology, Guilin 541004, China

Corresponding author: Weilin Xu (xwl@guet.edu.cn)

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ABSTRACT Most conventional memristor-based Pavlov associative memory neural network circuits have been working on realizing the learning and forgetting functions of simultaneous conditioning. However, the time interval between unconditional stimulus and conditional stimulus is a critical variable in classical conditioning. Different unconditional and conditional stimulus intervals evoke associative memory of brains with different rates. For example, learning in simultaneous conditioning is less effective than delay conditioning. Therefore, a memristor-based neural network circuit of delay and simultaneous conditioning is designed. The proposed circuit consists of learning states detection module, voltage control module, and synapse module. Many functions, such as short-delay conditioning learning, long-delay conditioning learning, simultaneous conditioning learning, experience learning, and two types of forgetting are implemented by the circuit. In particular, the so-called experience learning is that learning the forgotten knowledge will be faster than before and learning again will forget more slowly. This function is more bionic. The correctness of the design is demonstrated through simulations using PSPICE.

INDEX TERMS Associative memory, memristive neural network circuit, memristor, delay conditioning.

I. INTRODUCTION

Human brain, the most intelligent existence, suggests a great source of inspiration for a non-conventional information processing paradigm to deal with the lapse of Moore’s law and break the Von Neumann bottlenecks. The current main research idea is to use micro Nano devices to imitate the information processing and transmission of neurons and synapses according to the known brain structure [1]–[3]. It is expected to closely mimic the operating principles of the human brain at the device and architecture levels. Since Professor Chua published a famous paper about memristor in 1971 [4] and TiO$_2$ memristor was physically produced in 2008 by HP lab [5], it has drawn a lot of attention from researchers [6]–[10]. The variability, nonvolatility, and low power consumption of memristors are very similar to the characteristics of synapses in biological neural networks, which makes people see the dawn of directly simulating human brain functions at the hardware level. Many scholars have put efforts to build neural networks with memristive synapses [11]–[15].

Associative memory is an important way for intelligent organisms to recognize the world. In associative learning, classical conditioning is the best-known and typical, which is related to important neuronal behaviors and has been extensively studied and simulated. Since Pershin and Di Ventra [16] first implemented Pavlov associative memory by using a microcontroller and memristor-based synapses, the memristor-based neural network has been bringing about many discussions [17]–[26]. Zhang et al. [17] realized some advanced neural activities in the light of spike-rate-dependent plasticity (SRDP) rules, including learning, associative memory, and forgetting. A memristor-CMOS hybrid circuit presented by Liu and Zeng [18] can perform the learning activity and two types of forgetting activities. Because different polarities of voltages are applied to adjust memristance in most memristive circuits, Yang et al. [19] proposed a memristance changing circuit to perform the Pavlov associative memory only by positive voltage. In addition, work in [20] not only achieved Pavlov associative memory,
but also accomplished experience learning. Sun et al. [21] put forward a Pavlov associative memory neural network to realize associative memory, experience learning, and trace conditioning. Zhang and Long [22] proposed a learning experience memristor for using as synapse. Based on all input feedback law, the associative neural network circuit incorporates learning experience behavior, forgetting, and threshold functions. Sun et al. [23] designed a Pavlov associative memory circuit with dual-mode switching that is auditory mode and visual mode. Furthermore, a memristive network for associative learning was constructed by Wang et al. [24] with associative learning, backward conditioning, and forgetting functions. In addition to learning and forgetting, Pavlov’s theory of associative memory also includes stimulus generalization and discrimination [27]. Shang and Wang [25] designed a circuit to implement generalization and discrimination. Wang and Zou [26] demonstrated a new emotion model of associative memory neural network and a Ag/AgInSeTe/Ta memristor were employed. Different emotions can be recognized through associative memory when different news is received. However, deficiencies also exist in previous works. The work in [16] does not have a forgetting function. In [17], the “food” neuron can still be activated by the “ring” neuron in a low frequency even if the synaptic weight between the “ring” neuron and the “salivation” neuron is rather minimal. Work in [18] and [19] do not contain experience learning. The control circuit in work [20] and [23] are too complicated if covering all of the learning functions. The learning functions in Work [21] are more comprehensive, but also do not include other learning procedures. What’s more, most of the works discussed above [16]–[20], [22], [23], [25], [26] are dedicating to build simultaneous conditioning. It strictly requires that unconditional stimulus and conditional stimulus appear simultaneously and are repeated several times to generate associative memory.

In Pavlov associative memory, a crucial variable in classical conditioning is the time interval between conditioned stimulus and unconditioned stimulus [30], [31]. Actually, in classical conditioning, the delay conditioning is more effective than the simultaneous conditioning [32]. And there is a general tendency for long-delay conditioning to emerge more slowly than short-delay conditioning [32]–[35].

Compared with previous works, this work has the following advantages: besides simultaneous conditioning, the delay conditioning, including short-delay conditioning and long-delay conditioning, is also accomplished; the effect of time-specific between conditioned stimulus and unconditioned stimulus is reflected by the circuit; experience learning is also implanted, which the learning and forgetting rates are variable; with no false learning.

The remainder of this paper is organized as follows. Section II introduces the theoretical basis of the proposed circuit, namely the memristor model. Section III introduces the basic theory of delay and simultaneous conditioning and overall design ideas. In Section IV, each module of the circuit is discussed and the complete circuit is presented. In Section V, the simulation results of the associative memory are explained in detail. All simulations in this paper are carried out using PSPICE. Finally, Section VI concludes the paper.

II. THE SPICE MODEL OF MEMRISTOR

A memristor is a type of dynamic resistor that can memorize the history of previous electrical inputs. The memristance (resistor of the memristor) changes only if the amount of electric charge flows through it that varies. Based on work [5], the structure of the HP memristor is shown in Fig.1 and the memristance is defined as

\[
M(t) = x(t)R_{ON} + [1 - x(t)]R_{OFF}, \tag{1}
\]

\[
x(t) = \frac{w(t)}{D} \in [0, 1], \tag{2}
\]

where \(R_{ON}\) is the lowest resistance state, \(R_{OFF}\) is the highest resistance state, \(w(t)\) is the width of the doped region, \(D\) is the width of the total region, and \(x(t)\) is the internal state variable and its dynamic equation is defined as

\[
\frac{dx}{dt} = k_i(t)f(x), \tag{3}
\]

\[
k = \frac{\mu V_i R_F}{D^2}, \tag{4}
\]

where \(\mu\) is the average ion mobility, \(i(t)\) is the current flowing through memristor, \(f(x)\) is the window function, and \(k\) is the proportional factor between the changing speed of \(x(t)\) and \(i(t)\).

However, the ideal memristor mentioned above cannot describe the threshold characteristics of an actual memristor device. Therefore, in this article, we adopt an HP memristor with a hard threshold voltage in our design and simulations. The so-called hard threshold-type switching is that the device states change only if \(|V_M| > V_{TH}\) (see Fig.2), where \(V_{TH}\) is the threshold voltage and \(V_M\) is the voltage across the memristor. The Biolek window function [28] is employed as follows:

\[
f(x) = 1 - \left(x - stp(-i)^2p\right). \tag{5}
\]

The threshold function is in the following form:

\[
f(x, p) = stp (abs(V(x) - V_{TH})), \tag{6}
\]

where the window parameter \(p\) is a positive integer.
From the viewpoint of [29], different smoothing functions are used for equations (5) and (6), which can weaken the mathematical convergence problem of the memristor model owing to the absolute value function and the step function.

The step function is smoothed as

\[ stp_s(x) = \frac{1}{1 + e^{-x/b}}. \]  

The absolute value function can be smoothed as

\[ abs_s(x) = x (stp_s(x) - stp_s(-x)). \]  

The accuracy and robustness of the model can be increased by adjusting the value of b. In this article, the value of b is determined to be $4.5 \times 10^{-6}$.

When a positive voltage greater than $V_{T+}$ (positive threshold voltage) is applied to the memristor, it tends to broaden the doped region and descend the memristance. Conversely, a negative voltage less than $V_{T-}$ (negative threshold voltage) is applied to the memristor, which causes a decrease of doped region and an increase of the memristance. Three different memristors ($M_1$, $M_2$, and $M_3$) are employed in this article. The relevant parameter configurations of all three memristors are presented in Table 1, where $R_{INT}$ is the initial resistance of the memristor. The Fig.3 demonstrates the memristance response when different voltages are applied to these memristors. As shown in Fig.3(a), for $M_1$, since $V_{T+}$ is 5.1 V, when $V_M = 5V$, $M_1$ still remains at the initial resistance state of 100 $\Omega$. When $V_M = 5.5V$, $M_1$ quickly switches to 200 $\Omega$. Likewise, $M_2$ has similar characteristics to $M_1$, as presented in Fig.3(b), but they have different $\mu_V$ values. In this article, the greater $|V_M|$ is, the faster the memristance changes. In Fig.3(C), the external voltage applied to $M_3$ within 0−9 s is 5 V (grey line) or 10 V (blue line). The voltage applied within 9−18 s is −5V (red line) or −10V (green line). Obviously, $M_3$ drops faster at a voltage of 10V and rises slower when the voltage is −5V.

III. THE PAVLOV ASSOCIATIVE MEMORY OF DELAY CONDITIONING AND SIMULTANEOUS CONDITIONING

Classical conditioning refers to a learning procedure that occurs unconsciously. Pavlov repeatedly paired the bell with the food. After repeated presentations of the bell and the food, the dogs will salivate once they hear the bell. The bell predicts the food, which means that dogs have an associative memory between the food and the bell. In this case, food is an unconditioned stimulus (US), the sound of the bell is a conditioned stimulus (CS), instinctive salivation in response to the food is an unconditioned response (UR), and the salivation can be triggered by the sound of the bell, which is a conditioned response (CR). A number of CS-US pairings are necessary to yield the CR on a test. The gradual acquisition of CR is a learning process in associative memory. The gradual extinction of CR is the so-called the forgetting process in associative memory. In particular, after a complete training cycle of learning and forgetting, further study will be more skillful. In other words, the rate of acquisition will be faster than before, and the extinction will be slower. This is called experience learning.

The synapse is the junction between neurons. Synapse weight refers to the connection strength of the presynaptic neuron to the postsynaptic neuron, which is variable. Such dynamic changes that occur at synapses depend on whether they’re active or inactive. This is called synaptic plasticity which is a critical characteristic in human brains. Therefore, the memristor-based synapse module demonstrates synaptic weight updates and connects the pre-neuron and post-neuron. As shown in Fig.4, $W_{US}$ represents the synaptic weight between the $N_{US}$ (US neuron) and $N_R$ (Response neuron) and it should be a constant and strong connection.

### Table 1. The parameters of memristors in this paper.

| Parameters | M1(\(\Omega\)) | M2(\(\Omega\)) | M3(\(\Omega\)) |
|-----------|----------------|----------------|----------------|
| $D_{INJ}$ | 10             | 10             | 10             |
| $R_{ER}(\Omega)$ | 100           | 100            | 100            |
| $R_{ER}(\Omega)$ | 2000           | 2000           | 5000           |
| $V_T(V)$  | 5.1            | 2.1            | 0.13           |
| $V_T(V)$  | -5.1           | -2.1           | -0.13          |
| $\mu_V(\text{m}^2 \text{s}^{-2})$ | 1e-16          | 0.8e-19        | 1e-16          |
| $\sigma_p$ | 2              | 2              | 2              |

![FIGURE 2. Hard threshold voltage memristor.](image2)

![FIGURE 3. Curves of memristance when M1, M2, and M3 are applied by different voltages. (a) $V_M = 5.5V$ (red line) and $V_M = 5V$ (blue line); (b) $V_M = 2.15V$ (blue line) and $V_M = 2V$ (red line); (c) $V_M = 5V$ (grey line), $V_M = -5V$ (red line), $V_M = 10V$ (blue line), and $V_M = -10V$ (green line).](image3)
FIGURE 4. The brief diagram of the Pavlov associative memory neural network. N\textsubscript{US} and N\textsubscript{CS} are pre-neurons, which represent US neuron and CS neuron respectively; N\textsubscript{R} represents respond neuron and it is a post-neuron; Two lines connecting the afferent and efferent neurons are synapses. W\textsubscript{US} and W\textsubscript{CS} represent the synaptic weights.

FIGURE 5. Illustration of the time-specific of CS-US pairings. Process ① has only CS signal; Process ② has only US signal; Process ③ is short-delay conditioning; Process ④ is long-delay conditioning; Process ⑤ is simultaneous conditioning.

In Fig.5, in process ①, since there is only a CS signal, the subject will have no response. In process ②, if only the US signal is given to the subject, the UR will occur physically. In delay conditioning, CS is paired with the US, which typically overlaps and terminates at the same time. If the interstimulus interval (ISI) between CS and US is short, as presented in process ③, it is the short-delay conditioning. If the ISI is longer, as presented in process ④, it is a long-delay conditioning. After the CS-US pairing is repeated several times in process ③, the CR can be measured. In process ④, it needs more repeated times than that of process ③ to elicit CR because learning in process ③ is much faster than process ④. When the CS and US signals are contemporaneous, as shown in process ⑤, it is known as simultaneous conditioning. Process ⑥ has a relatively weak reflection. Process ③, process ④, and process ⑤ are learning processes.

Moreover, if the association between US and CS is not periodically reinforced by such pairing as described above, the CR undergoes extinction. Thus, process ① and process ② also represent two types of forgetting.

IV. THE CIRCUIT DESIGN

Based on the above theory, a block diagram of the overall circuit design is shown in Fig.6. In part A, N\textsubscript{US} and N\textsubscript{CS} represent two excited neurons after receiving the US and CS signals, respectively. The proposed circuit includes a learning states detection module, a voltage control module, and a synapse module. The learning states detection module is mainly used to detect the time interval of CS-US pairing, and then determines the learning states of training. According to different learning states, the voltage control module outputs different learning and forgetting voltages to control the synapse module. Part B is a major part of the synapse module. Ma is a memristor, Va is a DC voltage, Rb is a resistor, ABM is a mathematical operation device whose output is equal to $-V_{IN1}/V_{IN2}$, and OPa and OPb are operational amplifiers. When $V_{ABM}$ is less than Va, it implies a strong connection between the afferent and efferent neurons and the afferent neuron is excited. When the test is in process ⑤, the output of the voltage control module is set as 5V. This will cause a decrease in Ma and an increase in synaptic weights. Similarly, when the test is in process ⑥, the output of voltage control module is 2.5V that will also make Ma smaller. But its memristance goes down slower than that of process ③. Because the conditioned response established by process ⑤ is relatively weak, a voltage of 0.15V is used to characterize it. In particular, the output of the voltage control module is greater than or equal to $-2V$ in the forgetting process, which is not a fixed value, indicating that forgetting rate can be varied. Then, Ma will gradually increase which means the synaptic weight decreases. According to the characteristics of the memristor, in experience learning, we hope that the learning voltage will be larger and the forgetting voltage will be smaller so that each learning will be more efficient than the previous one. Thus, with the help of the learned response signal from the synapse module, the learning voltage in
process \( \pi \) and process \( \rho \) becomes 10V and 5V, respectively, and the forgetting voltage will decrease after each learning.

As stated above, \( W_{US} \) is constant. Therefore, it is represented by a fixed resistance \( R_a \) that is equal to 100\( \Omega \). Once the US signal is a high-level voltage, the UR of the subjects can be triggered. Then, \( N_R \) is a high-level voltage.

### A. THE LEARNING STATES DETECTION MODULE

The learning states detection module mainly consists of a decimal counter 74160 (C1), three T flip-flop (T1–T3) with asynchronous set and reset, and some gates (G1–G30) as shown in Fig.7. The CLK input of the counter and T flip-flop is active on the rising edge with a frequency of 1Hz and a duty cycle of 50\%. The pulse width of US signal is 500ms. When C1 outputs “0000”, the pulse width of the CS signal is 500ms. It can be a state of simultaneous conditioning or forgetting. When C1 outputs “0000–0100”, the pulse width of CS signal is 2–5s. If the CS signal occurs with the overlap of the US signal at the end, it is a learning state in short-delay conditioning. When C1 outputs “0101–1001” or overflows, the pulse width of CS signal is greater than 6s. Then the test is in long-delay conditioning if the US signal also occurs later and ends together with the CS signal. Table 2 summarizes these processes.

![Fig.7: Learning states detection module.](image)

![Table 2: Signal detection and learning states.](image)

| Counter output \( (Q_0\bar{Q}_0\bar{Q}_1\bar{Q}_1) \) | Process                        |
|---------------------------------|--------------------------------|
| 0000–0100                       | Short-delay conditioning (Process \( \pi \)) |
| \( \geq 0101 \)                 | Long-delay conditioning (Process \( \rho \)) |
| 0000                            | Simultaneous conditioning (Process \( \varphi \)) or forgetting (Process \( \omega \) and Process \( \zeta \)) |

C1 has an asynchronous reset input \( R_D \), a parallel enable input \( L_D \), and two enables inputs ENT and ENP. When \( \bar{R}_D = L_D = ENP = ENT = 1 \), C1 is in the counting state. When \( \bar{R}_D = L_D = 1 \) and \( ENP \cdot ENT = 0 \), regardless of the CLK state, C1 has the previous value. In particular, when \( ENP = 0 \) and \( ENT = 1 \), the carry output RCO also maintains its state. Based on the above working principles, set data input as “0000”, \( \bar{R}_D, L_D \), and ENT are connected together to \( N_{CS} \), and RCO signal is transmitted to ENP via a inverter G10, so as to ensure that C1 is in counting state once CS signal is high. Moreover, when RCO = 1, the counting output and RCO will hold the previous value.

Ground the inputs of flip-flops T1, T2, and T3, and reset all of their initial states to 0. If C1 outputs “0001”, the T2S will be pulsed high. Then, T2Q will be pulsed high. If C1 outputs “0101”, T3S will be pulsed high. Then, T3Q will be held high and T2 is reset. When the US signal is high and T2S is high (short-delay signal is high), AND gate G28 output will be high, which indicates that short-delay conditioning signal is high and the test is in process \( \pi \). Likewise, if the US signal is high and T3Q is held high (long-delay signal is high), then the AND gate G29 output is high, indicating that long-delay conditioning signal is high and the test comes into process \( \rho \). In addition, if T2Q and T3Q are all low while the CS and US signals appear simultaneously, then the test is in process \( \varphi \).

T2S and T3S are connected to T1S via OR gate G11 and T1R is connected to the NUS. According to Fig.5, there is an ISI between the US and CS signals in delay conditioning. When the US signal has not arrived and the count output of C1 is greater than “0000”, T1Q is held high, otherwise it is low. Based on that, the count output state “0000” and T1Q are connected via AND gate G22 to T2R and T3R. If the count output of C1 is greater than “0000” and T1R has no US signal to reset, then G22, G27, and G23 will be high and T2 and T3 will be reset, indicating that the delay conditioning is over.

Specific examples are shown in Fig.8 and Fig.9, where the pulse widths of CS signals are 3s and 9s, respectively.

![Fig.8: Short-delay signal.](image)

In addition, when the associative is formed, the U2 signal from the synapse module is high. Then, a feedback signal is generated. If only the CS or US signal is presented, G24 has signal. That is to say, a forgetting signal is produced.
The simultaneous conditioning signal occurs (G25 has signal) when the stimuli are presented simultaneously.

**B. VOLTAGE CONTROL MODULE**

Based on [21], the voltage control module is modified, as shown in Fig.10. S1−S7 are voltage-controlled switches with a threshold voltage that is 2V. \( V_1 = V_2 = 5V, V_3 = 0.5V, V_4 = 2V, V_5 = 0.15V, R_2 = 100\Omega, R_3 = 200\Omega, \) and \( R_4 = R_5 = R_6 = R_7 = R_8 = 1k\Omega. \) SUM1, SUM2, and SUM3 are the sum components. \( V_{SUM1} = V_1 + V_3, V_{SUM2} = V_2 + V_3, \) and \( V_{SUM3} = V_4 + V_5. \) M1 and M2 are memristors, ABS is a mathematical component to obtain the absolute value of the input voltage, and A1 is an operational amplifier. U3 is output control voltage of this module. M1 and M2 are applied to adjust the amplitude of the control voltage. They are both placed in reverse. And the negative threshold voltage of M1 is −5.1V to ensure that the memristance can be altered only if the input voltage received by M1 is greater than 5.1V. M2 works in the same way as M1 and its negative threshold voltage is −2.1V. For M1, the \( R_{OFF} \) is 2k\Omega and \( R_{ON} \) is 100\Omega.

Associative memory occurs only after the subject has been trained for a period of time. At first, the subject has no response to CS signal. There is no feedback signal. If the short-delay conditioning signal is received (G28 has signal), S1 and S7 are closed and S2, S3, S4, S5, and S6 are opened. The output voltage of A1 is \( -(M_1/M_2) \times V_1 = -5V. \) Thus, the voltage of −5V becomes 5V through ABS. Then, this learning voltage is sent to the synapse module, and the learning of process ③ starts. If there is a long-delay conditioning signal (G29 has signal), S2 and S7 are closed and S1, S3, S4, S5, and S6 are opened. The output voltage of A1 is \( -(M_1/R_2) \times V_1 = -5V. \) Via ABS, the voltage of −5V turns to 2.5V. This learning voltage is also sent to the synapse module, and the learning of process ④ begins. If the \( N_{US} \) and \( N_{CS} \) are activated simultaneously, it is the learning state of simultaneous conditioning. In process ⑤, S5 and S7 are closed and S1, S2, S3, S4, and S6 are opened. The output voltage of A1 is \( -(M_1/M_2) \times V_4 = -0.15V. \) Which becomes 0.15V through ABS and the learning begins. In addition, if only \( N_{US} \) or \( N_{CS} \) is excited, S4 and S6 will be closed, and S1, S2, S3, S5, and S7 will be opened. Then, the output voltage of A1 is \( -(M_1/M_2) \times V_4 = -2V. \) This voltage is directly sent to the synapse module without through ABS and the forgetting process begins.

When associative memory is formed (U2 signal is high) and the test is still in process ③, G20 has signal (see Fig7). A feedback signal is generated, then S3 is closed. \( V_{SUM1} \) equals \( V_1 + V_3, \) that is 5.5V. It is greater than the threshold voltage of M1, which will switch the memristance of M1 from 100\Omega to 200\Omega. Subsequently, the learning voltage in process ③ will become \( |-(M_1/R_2) \times V_1| = 10V \) next time. Obviously, learning at 10V will be much faster. Similarly, if the test is still in process ④, with the help of the feedback signal, M1 is switched from low resistance to high resistance. In the new learning process, the learning voltage turns to \( |-(M_1/R_3) \times V_2| = 5V. \) This learning voltage is also twice that of the first-time learning. In particular, when the associative memory comes into being, in virtue of the feedback signal, G24 and G25 have signals (see Fig.7). And voltages of V4 and V5 are exerted to make M2 gradually increase. This is because \( V_{SUM3} = V_4 + V_5 = 2.15V \) is greater than the threshold voltage of M2. When the subject begins to forget, the forgetting voltage U3 is equal

![FIGURE 9. Long-delay signal.](image)

![FIGURE 10. Voltage control module.](image)

![FIGURE 11. Synapse module.](image)
to $-(M1/M2) \times V4$. Because of the fast switching of M1 (from the low resistance state to high resistance state), the forgetting rate mainly depends on M2. The forgetting voltage will be bigger than that of the last time. Hence, the forgetting rate will be smaller in further leaning, which means the memory will be much deeper. Moreover, the longer it learns, the deeper it remembers. The more it learns, the slower it forgets. Finally, it may develop into long-term memory. Compared to work [21], this feature is more bionic.

C. SYNAPSE MODULE

Synapses are neuronal junctions. Synaptic plasticity is the neurobiological basis of brain learning and memory. The synapse circuit module adopts the design of the work [21], as shown in Fig.11. The U3 signal is the voltage output of the voltage control module. The high-level voltage of the U2 signal on behalf of the acquisition of CR and the high-level voltage of the U1 signal represents the occurrence of UR. Since the US always makes the subject produce UR, a small resistor $R1 (R1 = 100\Omega)$ is applied to imitate the synapse between the NUS and NR. M3 is a memristor, $R9 = 1k\Omega$, $V6 = 2V$, A1 and A2 are operational amplifiers, and ABM is a mathematical operation device whose output is $V_{ABM} = -V_{IN1}/V_{IN2}$.

The core of the synapse module is M3. When a voltage above the threshold voltage is applied to M3, its memristance changes. The memristance of M3 can be adjusted by the voltage of U3. The output voltage of A2 is equal to $-(R9/M3) \times U3$, thus the output of the ABM is $V_{ABM} = M3/R9 = M3/1000$. The inverting input node of A3 receives the signal from SUM4 which indicates synaptic strength. When its value is less than $V6 (M3 < 2k\Omega)$, A3 outputs a high-level voltage. In other words, there is a strong connection between the NCS and NR and CR is acquired. When $V_{SUM4} \geq 2V$, the output of A3 is low. The NOT gate G13 is controlled by NCS. Therefore, when there is no CS signal, the inverting input node of A3 is always greater than 2V and a low level voltage is produced by A3. The above analyses indicate that the Pavlov associative memory can be realized by controlling the input voltage of M3, and different rates of memristance change demonstrate different learning and forgetting rates.

The complete circuit is illustrated in Fig.12. It includes learning state detection (in red box), voltage control module (in blue box), and synapse module (in orange box). CLK is a clock signal. The subject will respond once a US signal occurs or CR is established. Thus, the relationship between two of them can be demonstrated by an OR gate G31, where NR is the response neuron.

V. SIMULATION RESULTS

A. LONG-DELAY CONDITIONING

According to the above we mentioned, as the count output surpasses “0101”, the pulse of the CS signal will exceed 6s and $T_{3Q}$ is held high. When US signal is also high, G29 outputs high and long-delay conditioning signal is high. As shown in Fig.13, the associative memory has not been built at the beginning of the test. The subject is only given the US signal, so U1 is high and UR emerges. Only the CS signal, the subject has no response and U2 signal is low.
The \( U3 = -2V \), which means that the forgetting voltage is \(-2V\) in both cases, as shown in Fig.15.

From 28.5s, the pulse width of the CS signal is 7s and the test is in long-delay conditioning at the very first time. The learning voltage \( U3 \) equals \(|-(M1/R3) \times V2|\), that is \(|-(100/200) \times 5V|\) or 2.5V. Until 294.5 s, the subject has been through the repetition of CS-US pairing for 19 times. M3 drops below 2k\( \Omega \) and CR starts to be acquired (U2 signal is high), as shown in Fig.16(c) and Fig.14 respectively. Then, memory continues to be reinforced by almost 3 CS-US pairings (i.e. 42s) that makes the subject learn more deeply. The strong connection between \( N_{CS} \) and \( N_{US} \) is sustained which ensures the feedback signal is high. Therefore, M1 and M2 are up to 200\( \Omega \) and 303.8\( \Omega \) respectively, as shown in Fig.16(a) and Fig.16(b). When the US signal is gone, the long-delay conditioning is over. From 343.5s, the CS signal is presented repeatedly in the absence of the US signal and \( U3 \) turns to \(|-(M1/M2) \times V4|\) that is \(|-(200/303.8) \times 2V|\) or \(-1.32 V\). M3 gradually ascends, which implies that the connection between \( N_{CS} \) and \( N_{US} \) descends. The CR disappears after 6s.

**B. SHORT-DELAY CONDITIONING**

When pulse width of the CS signal is 3s and CS signal is overlapped by the presentation of US signal at the end, it is a test in short-delay conditioning, as shown in Fig.17.
After the US and CS signals appear 10 times, i.e. 60s, the associative memory is formed and U2 signal starts to be high, as shown in Fig.18. It is obvious that the learning here is faster than the previous learning in Fig.13. In Fig.23, we can
see that the learning voltage $U_3$ equals $|-(M_1/R_2) \times V_1|$, that is $|-(100/100) \times 5V|$ or $5V$ at first. Furthermore, the US and CS signals also continue to repeat almost 3 times (i.e. 18s) to enhance the memory. $M_1$ also increased from
100Ω to 200Ω as shown in Fig. 24(a). When the US signal disappears, the short-delay conditioning comes to the end. After that, the subject is given to only CS signal (from 84.5s to 126s) or US signal (from 126.5s to 160s), as shown in
Fig.17 and Fig.19. This causes a reduction in CR to CS. M3 becomes larger and the CS signal eventually stops eliciting CR after 7s.

Learned it then forgot it. After experiencing this process once, usually the learning rate rises and the forgetting rate falls. As illustrated in Fig.19, from 160.5s, the test enters short-delay conditioning again. The learning voltage U3 is $|-(M1/R2) \times V1|$ which is $|-(200/100) \times 5V|$ or 10V, as shown in Fig.23, that is twice as large as the original. The subject gets down to respond to the CS signal (see Fig.20), following 5 times CS-US pairings (i.e. 30s). Then, 3 times CS-US pairings (i.e. 18s) continue to be exerted to the subject. Afterwords, in Fig.19 and Fig.21, there is only the CS signal (from 206.5s to 279s) or the US signal (from 279.5s to 304s). The subject forgets after 9s. It follows that the second-time learning is much faster and the forgetting is slower than that of the first-time learning in Fig.17.
TABLE 3. Simulation results of the proposed circuit.

| Simulations | $N_{CS}$ | $N_{CS}$ | $N_{R}$ | $M_1(\Omega)$ | $M_2(\Omega)$ | $M_3(\Omega)$ | $U1$ | $U2$ | $U3(V)$ | Rate | Reference |
|-------------|---------|---------|---------|--------------|--------------|--------------|------|------|--------|-------|-----------|
| The long-delay conditioning | 0 | 1 | 1 | 100 | 100 | 4.9kΩ | 1 | 0 | -2 | / | Process ⊗: US → UR |
| | 1 | 0 | 0 | 100 | 100 | 4.9kΩ | 0 | 0 | -2 | / | Process ⊗: US → No response |
| | 1 | 1 | 1 | 100 | 100 | 1kΩ | 1 | 0 | 2.5 | 19 times | Process ⊗: US-CS pairs → No response (learning) |
| | 1 | 1 | 1 | 100 | 100 | 200 | 1 | 1 | 5.5V | 3 times | Process ⊗: US-CS pairs → CR (learned to response) |
| | 1 | 0 | 1 | 200 | 303.8 | 2kΩ | 0 | 1 | -1.32 | 6s | Process ⊗: US → CR (forgetting) |
| | 1 | 0 | 0 | 200 | 303.8 | 2kΩ | 0 | 0 | -1.32 | / | Process ⊗: US → No response (forgotten) |
| The short-delay conditioning and experience learning | 1 | 1 | 1 | 100 | 100 | 4.9kΩ | 1 | 0 | 5 | 10 times | Process ⊗: US-CS pairs → No response (learning) |
| | 1 | 1 | 1 | 100 | 100 | 351.3 | 2kΩ | 1 | 1 | 5.5V | 3 times | Process ⊗: US-CS pairs → CR (learned to response) |
| | 1 | 0 | 1 | 200 | 351.3 | 1kΩ | 0 | 1 | -1.14 | 7s | Process ⊗: US → CR (forgetting) |
| | 1 | 0 | 0 | 200 | 351.3 | 2kΩ | 0 | 0 | -1.14 | / | Process ⊗: US → No response (forgotten) |
| | 0 | 1 | 1 | 200 | 351.3 | 1kΩ | 1 | 0 | -1.14 | / | Process ⊗: US → UR (forgotten) |
| | 1 | 1 | 1 | 200 | 351.3 | 2kΩ | 1 | 0 | 10 | 5 times | Process ⊗: US-CS pairs → No response (learning) |
| | 1 | 0 | 1 | 200 | 464.5 | 2kΩ | 0 | 1 | -0.86 | 9s | Process ⊗: US-CS pairs → CR (learned to response) |
| | 1 | 0 | 0 | 200 | 464.5 | 2kΩ | 0 | 0 | -0.86 | / | Process ⊗: US → CR (forgetting) |
| | 0 | 1 | 1 | 200 | 464.5 | 1kΩ | 1 | 0 | -0.86 | / | Process ⊗: US → No response (forgotten) |
| | 1 | 1 | 1 | 200 | 464.5 | 1kΩ | 1 | 0 | 5 | 8 times | Process ⊗: US-CS pairs → No response (learning) |
| | 1 | 1 | 1 | 200 | 464.5 | 2kΩ | 1 | 1 | 5.5V | 3 times | Process ⊗: US-CS pairs → CR (learned to response) |
| | 1 | 0 | 1 | 200 | 556 | 1kΩ | 0 | 1 | -0.72 | 11s | Process ⊗: US → CR (forgetting) |
| | 1 | 0 | 0 | 200 | 556 | 2kΩ | 0 | 0 | -0.72 | / | Process ⊗: US → No response (forgotten) |

1 The “↓” behind $M_3$ indicates that the memristance of $M_3$ is decreasing.
2 The “↑” behind $M_3$ or $U_3$ indicates that the memristance of $M_3$ or the voltage value of $U_3$ is increasing.
3 The “→” between two chosen voltages indicates that the voltage applied to M1 or M2 is switched from the former to the latter.

With the experience of the first two learning, the long-delay conditioning comes at 308.5s, as shown in Fig.21. The pulse width of the CS signal is also 7s just like the first long-delay conditioning in Fig.13. The learning voltage $U_3$ equals $|-(M_1/R_3) \times V_2|$, that is $|-(200/200) \times 5V|$ or 5V, as shown in Fig.23. This is a double voltage compared to the first long-delay conditioning. A strong connection between $N_{CS}$ and $N_{R}$ is produced (see Fig.22) after past 112s, i.e. 8 CS-US pairings. Then, the learning is maintained for 3 CS-US pairings, which is taken 42s. In the end, the CR fades away after 11s as the US signal vanishes. It is evident that the learning in this time is more than twice as fast as that of the last time in Fig.13, and the forgetting is also relatively slower.

The change in the memristance of M2 is shown in Fig.24(b). M2 is trained three times. For the first time, M2 increases from the initial value to 351.3Ω. For the second time, M2 increases to 464.5Ω. Finally, M2 is 556Ω. Thus the forgetting voltage switches from $-1.14V$ to $-0.86V$ and then to $-0.72V$. This means that the knowledge learned will be forgotten more slowly each time. In other words, the acquisition will last much longer when each time one actually learned again. In the above processes, the curve of the M3 memristance is shown in Fig.24(c).

C. SIMULTANEOUS CONDITIONING

In simultaneous conditioning, the CS signal is repeatedly paired with the US signal simultaneously as shown in Fig.25.
The simultaneous conditioning does not work well, so the learning voltage is designed to be 0.15 V as shown in Fig. 27. As shown in Fig. 26, the U2 signal becomes high at 294s. This means that two paired input signals are about to be repeated 294 times in 294s to evoke the learned response. The subject continues to learn for 56s so that M3 declines continuously. US signal ends at 350s. The learned response lasts 3s without the presence of US signal, which means that the formed memory is quite shallow. The forgetting voltage U3 is equal to \(-\frac{(100/100) \times 2V}{100} = -2V\), as shown in Fig. 27. The changes in M3 are plotted in Fig. 28.

**VI. CONCLUSION**

In this paper, a memristor-based neural network circuit of delay and simultaneous conditioning is presented, where short-delay conditioning, long-delay conditioning, simultaneous conditioning, experience learning, and two types of forgetting are implemented, according to the time-specific of CS-US pairs. Unlike the previous Pavlov associative memory, the proposed circuit can realize the associative memory even if the US and CS signals do not appear at the same time. The circuit also reflects that the ability of short-delay conditioning to induce associative memory is usually better than long-delay conditioning and simultaneous conditioning typically works poorly. Moreover, the learning and forgetting rates are variable when the associative memory is formed. Further studies will focus on more efficient associative learning network circuits and large-scale integrated circuits to mimic the human brain intelligence.

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Xinyu Xu received the B.E. degree with the School of Opto-Electronic and Communication Engineering, Xiamen University of Technology, Xiamen, China, in 2019. She is currently pursuing the M.E. degree with the School of Information and Communication, Guilin University of Electronic Technology, Guilin, China. Her interest includes memristor-based artificial neural networks.

Weilin Xu was born in Hunan, China, in 1976. He received the Ph.D. degree in micro-electronics and solid-state electronics from Wuhan University, Wuhan, China, in 2011. In 2005, he joined the Guilin University of Electronic Technology, Guilin, China, where he is currently a Professor. From February 2019 to February 2020, he was a Visiting Scholar with the Electrical and Computer Engineering Department, Southern Illinois University Carbondale, IL, USA. His current research interests include memristors and CMOS mixed-signal integrated circuits for biomedical applications.

Fangrong Hu was born in Hunan, China, in 1973. He received the Ph.D. degree in optics engineering from the Chinese Academy of Science, Beijing, China, in 2010. In 2005, he joined the Guilin University of Electronic Technology, Guilin, China. His current research interests include metamaterials, novel terahertz functional devices, microelectromechanical systems, and laser technology.

Baolin Wei received the B.S. and M.S. degrees, in 1999 and 2002, respectively, and the Ph.D. degree from Nankai University, Tianjin, China, in 2010. From February 2017 to February 2018, he was a Visiting Scholar with the Electrical and Computer Engineering Department, Southern Illinois University Carbondale, IL, USA. He is currently a Professor with the School of Information and Communication, Guilin University of Electronic Technology, Guilin, China. His research interests include analog, and RF IC design, and integrated circuit design for emerging transistors.