THE FAILURE RISK ANALYSIS OF DIGITAL CIRCUITS

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Abstract – To analyze the failure risk of asynchronous digital circuits the time-parameter is introduced into the Boolean algebra replacing the arithmetic operations by logical operations. There considered an example of construction of signals passing through the logical elements, using the described below mathematical apparatus.

Keywords: failure risks, Boolean algebra, the Heaviside function.

AMS: 94C05, 06E25, 06E30.

1. INTRODUCTION

In Boolean algebra that is used for simulation of digital circuits, the transition time (or inertia) of logical elements (eg, ”and”, ”or”) from one state to another (eg, from 0 to 1) does not take into account. In cases when the signal propagation time inside the element is sufficiently small the switching delay can be ignored. But with increasing frequency of changes of the input signals in real circuits the time influence starts to affect the signal propagation inside its elements. Such delays may cause the unstable devices work (i.e. there appeared a transitions, called failures in the signals after serial passage through the nodes of the circuit unaccounted by the circuit model). Many manufacturers of modern CPUs kept in secret how they struggle with failures posed by the delays at frequencies of the order of GHz. In fact a common conductor with many bends close to the board is converted into inductance in this operation mode.

To analyze the most simple failure risk scheme there usually used the time diagrams method [1–3], which has already become a classic. The signals at each node are drawn strictly under each other: an artificial delay is produced in transition from one state to another where it necessary, and then the output signals are constructed according to Boolean representation. Given method is not very good because it requires work with graphics that can make an error in the received signals. We need to know whether there is a failure, and what will it look like. That is why, in this article this procedure is
transformed from graphical representation to mathematical representation.  
At that we introduce a time-parameter into Boolean algebra replacing the  
logic operations by arithmetic. To simplify the analysis there considered  
asynchronous circuit, i.e. uncontrolled by external (synchronizing or pulsing)  
signal digital circuit.

2. THE TRANSITION FROM THE LOGICAL REPRESENTATION TO  
ARITHMETIC REPRESENTATION OF BOOLEAN FUNCTIONS

Let us consider set of numbers $M = \{0; 1\}$. It defined the operations  
of negation, conjunction, disjunction, and their products (e.g. implication,  
disjunction, and other alternative). Let us express these logical operations  
through the arithmetical on a set $M$:

$$
\begin{align*}
\overline{x} &= 1 - x, \\
x \land y &= x \cdot y, \\
x \lor y &= x + y - x \cdot y. 
\end{align*}
\tag{1}
$$

Let us show the validity of law of De Morgan $x \land y = \overline{x \lor y}$:

$$
\overline{x \lor y} = 1 - (1 - x + 1 - y - (1 - x) \cdot (1 - y)) = x \cdot y = x \land y.
$$

For expression (1) let us add a rule

$$
x^m = x
$$

for all natural values $m$, which validity is obvious.

The expression for a Boolean function $f$, which is a function of input sig- 
nals of circuit can now be simplified by the laws of arithmetical operations  
and rule (2). After some simplifications move back – to Boolean representa- 
tion. At that the minimization process can be automated by using symbolic  
calculations.

3. THE INJECTION OF TIME-PARAMETER INTO BOOLEAN  
ALGEBRA

As it is known the unit step function or Heaviside function is defined on  
the area of real numbers and returns the number that belongs to the set $M$:

$$
h(t) = \begin{cases} 
1, & t \geq 0, \\
0, & t < 0.
\end{cases}
$$
Let us denote the current time by $t$. Notice that function $h$ is also called the turn off function. The following statement is obvious: any signal in the logic circuit, comprising a transition from one logical state to another can be represented as the sum of the difference of Heaviside functions, combined with an appropriate argument.

For function $h$ there is the rule

$$\prod_{i=1}^{n} h(t - \tau_i) = h\left(t - \max_{i=1,n} \tau_i\right), \quad (3)$$

where $\tau_i$ – time moment when there is a change in the signal. Let us add a formula (3) to (1) and (2).

Now, knowing the analytical expression for the input signals of logical circuit, there can be found a function form of the output signal.

4. DELAYS IN LOGIC CIRCUIT ELEMENTS

It is convenient to model a signal delay in the logic element as the difference between the argument of the Heaviside function and the duration of the delay (so as for existing logical elements, commonly, the delays along the front (transition from 0 to 1) and recession (transition from 1 to 0) are approximately equal). Thus, any real logical element of the circuit can be modeled as a series connection of element of a pure delay [4] for each input and the ideal logic element (here the delay is equal to the duration of delay). For example, the output signal equation of conjunctor delay $\tau$ on the input takes the form:

$$y_c = f_1(t - \tau) \cdot f_2(t - \tau),$$

where $f_1(t)$ and $f_2(t)$ – functions that describe the corresponding input signals.

5. THE SEARCH ALGORITHM OF FAILURE CONDITIONS

The proposed search algorithm of failure states is similar to time diagram method; advantage of this method is that we work with graphical images signals, and their analytical expressions (in this case it is possible to assess the temporal characteristics of an analytical failure):

1. Let the investigated scheme operates in accordance with a logical expression given by disjunctive-normal form;
2. Defined by functions of input signals that represent transitions in the truth table, expressed in terms of the Heaviside function;

3. Go along the path of signals in the logic circuit in order to find expressions for the output circuit, applying the rules of (1) and (3);

4. If the resulting expression contains the difference between the Heaviside function, then we have a static failure, if there is a Heaviside function with delaying argument, then failure is dynamic.

6. AN EXAMPLE OF LOGICAL SCHEME ANALYSIS

Let us investigate the transition from the set 1111 to the set 1001 (15 → 9) of truth table for the circuit, that is shown at fig. 1. Let us represent the

Figure 1: Circuit that realize the Boolean function $Y = X_1X_2 \lor \overline{X_3}X_4$.

input signals as follows (for simplicity, let us consider the change of condition at the time moment, equal to 5 sec.).

\[
\begin{align*}
X_1 &= 1, \\
X_2(t) &= 1 - h(t - 5), \\
X_3(t) &= 1 - h(t - 5), \\
X_4 &= 1.
\end{align*}
\]
Assume that all elements have the same delay, equal to $\tau$. Then

$$X^*_1(t) = 1 - (1 - h(t - 5 - \tau)) = h(t - 5 - \tau),$$
$$X^*_2(t) = 1 \cdot (1 - h(t - 5 - \tau)) = 1 - h(t - 5 - \tau),$$
$$X^*_3(t) = X^*_1(t - \tau) \cdot 1 = h(t - 5 - 2\tau),$$
$$Y(t) = X^*_2(t - \tau) + X^*_3(t - \tau) - X^*_2(t - \tau) \cdot X^*_3(t - \tau) = 1 - h(t - 5 - 2\tau) + h(t - 5 - 3\tau) - (1 - h(t - 5 - 2\tau)) \cdot h(t - 5 - 3\tau) = 1 - h(t - (5 + 2\tau)) + h(t - (5 + 3\tau)).$$

Thus, we have a static crash – the difference of Heaviside functions is in the resulting expression (fig. 2).

![Figure 2: Signal diagram $Y(t)$](image)

### 7. CONCLUSION

In this work there was considered the method of failure risk analysis of digital circuits using an analytic representation of signals within the circuit. At that logical operations had to be replaced by arithmetic operations. The transitions from one signal state to another is described by the Heaviside function. The advantage of the described modification of the time diagrams method is the possibility of analytical analysis of the characteristics of failure.

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