A Single-Cycle MLP Classifier Using Analog MRAM-based Neurons and Synapses

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Abstract—In this paper, spin-orbit torque (SOT) magnetoresistive random-access memory (MRAM) devices are leveraged to realize sigmoidal neurons and binarized synapses for a single-cycle analog in-memory computing (IMC) architecture. First, an analog SOT-MRAM based neuron bitcell is proposed which achieves 12× reduction in power-area-product compared to the previous most power- and area-efficient analog sigmoidal neuron design. Next, proposed neuron and synapse bitcells are used within memory subarrays to form an analog IMC-based multilayer perceptron (MLP) architecture for the MNIST pattern recognition application. The architecture-level results exhibit that our analog IMC architecture achieves at least two and four orders of magnitude performance improvement compared to a mixed-signal analog/digital IMC architecture and a digital GPU implementation, respectively, while realizing a comparable classification accuracy.

Index Terms—Analog computing, in-memory computing, magnetic random access memory (MRAM), multi-layer perceptron (MLP), sigmoidal neuron, spin orbit torque (SOT).

I. INTRODUCTION

In-memory computing (IMC) has attracted considerable attention in recent years as a hardware accelerator for artificial neural networks (ANNs) [1], [2]. The main objective of the IMC architectures as alternatives for von-Neumann architectures is avoiding the processor-memory bottleneck to realize an energy-efficient and area-sparing computation. To achieve this goal, various techniques have been investigated from using 3D integration technology [3] to leveraging beyond-CMOS memristive devices [4]. Recently, various resistive technologies have been proposed to be used within IMC architectures such as resistive random access memory (ReRAM) [4], phase-change memory (PCM) [5], and magnetoresistive random-access memory (MRAM) [1].

Most of the previous IMC approaches operate in the digital domain [1], [6], meaning that they leverage resistive memory crossbars to implement Boolean logic operations such as XNOR/XOR within memory subarrays, which can be utilized to implement multiplication operation in binarized neural networks [7]. While digital IMC approaches provide important energy and area benefits, they are not fully leveraging the true potential of resistive memory devices that can be realized in the analog domain. On the other hand, mixed-signal analog/digital IMC architectures [5], [8] leverage the resistive crossbars to compute multiply and accumulation (MAC) operation in O(1) time complexity, however, they still require transferring data to digital processors to compute activation functions. Thus, in addition to the energy that is consumed to transfer data between processor and memory, signal conversion blocks are required to convert data from analog to digital domain and vice versa, which can lead to considerable energy overheads. In this paper, we use spin-orbit torque (SOT)-MRAM technology to implement both synapses and neurons within analog IMC subarrays that can be concatenated to form a multilayer perceptron (MLP) classifier that operates in a single clock cycle.

II. SOT-MRAM BASED NEURONS AND SYNAPSES

Fig. 1 shows a simplified structure of a SOT-MRAM cell including a magnetic tunnel junction (MTJ) with two ferromagnetic (FM) layers, which are separated by a thin oxide layer. MTJ has two different resistance levels, which are determined according to the angle (θ) between the magnetization orientation of the FM layers. The resistance of the MTJ in parallel (P) and antiparallel (AP) magnetization configurations can be obtained using the following equations [9]:

\[
R(\theta) = \frac{2R_{MTJ}(1 + TMR)}{2 + TMR(1 + \cos \theta)}
\]

\[
R_P = R_{MTJ}, \quad \theta = 0
\]

\[
R_{AP} = R_{MTJ}(1 + TMR), \quad \theta = \pi
\]

\[
TMR(T, V_b) = \frac{TMR_0/100}{1 + (\frac{V_b}{V_0})^2}
\]

where \(R_{MTJ} = \frac{RA}{AV_{CG}}\), in which the resistance-area product (RA) value of the MTJ depends on the material composition of its layers. TMR is the tunneling magnetoresistance, which relies on temperature (T) and bias voltage (V_b). \(V_0\) is a fitting parameter, and \(TMR_0\) is a material-dependent constant.

In the MTJ structure, the magnetization direction of electrons in one of the FM layers is fixed (pinned layer), while the electrons’ directions in the other FM layer (free layer) can be
TABLE I
PARAMETERS OF THE SHE-MRAM DEVICE [9].

| Parameter       | Description          | Value       |
|-----------------|----------------------|-------------|
| MTJArea         | $l_{MTJ} \times w_{MTJ} \times t_{MTJ}$ | $50nm \times 30nm \times 8nm$ |
| $H_{MTJ}$       | $H_{MTJ} \times w_{HMTJ} \times t_{HMTJ}$ | $100nm \times 50nm \times 3nm$ |
| RA              | Resistance-area product | 10 Ω·μm² |
| $V_0$           | Fitting parameter    | 0.65        |
| $TMR_{10}$      | Tunneling magnetoresistance | 100        |

Fig. 2 (a) shows the bitcell structure of the proposed neuron, which includes two SOT-MRAM cells and a CMOS-based inverter. The magnetization configurations of SOT-MRAM1 and SOT-MRAM2 devices should be in $P$ and $AP$ states, respectively. The SOT-MRAMs in the neuron’s circuit create a voltage divider, which reduces the slope of the linear operating region in the inverter’s voltage transfer characteristic (VTC) curve. The reduction in the slope of the linear region in the CMOS inverter creates a smooth high-to-low output voltage transition, which enables the realization of a sigmoid activation function. Fig. 2 (b) shows the SPICE circuit simulation results of the proposed SOT-MRAM based neuron using $V_{DD} = 0.8V$ and $V_{SS} = 0V$. The results verify that the neuron can approximate a $sigmoid(-x)$ activation function that is biased around $b = \frac{1}{2}(V_{DD} - V_{SS})$ voltage. The non-zero bias voltage can be canceled at both circuit- and algorithm-level, as described in the next sections.

B. SOT-MRAM Based Synapse

SOT-MRAM cells are capable of realizing two resistive levels, i.e., $R_P$ and $R_{AP}$. The combination of two SOT-MRAM cells and a differential amplifier can produce the positive and negative weights required for the implementation of a binary synapse. Fig. 3 shows a neuron with $Y_i = X_i \times W_i$ as its input, in which $X_i$ is the input signal and $W_i$ is a binarized weight. The corresponding circuit implementation is also shown in the figure, which includes two SOT-MRAM cells and a differential amplifier as the synapse. The output of the differential amplifier ($Y_i$) is proportional to $(I^+ - I^-)$, where $I^+ = X_iG_{AP}^i$ and $I^- = X_iG_{AP}^i$. Thus, $Y_i \propto X_i(G_{AP}^+ - G_{AP}^-)$, in which $G_{AP}^+$ and $G_{AP}^-$ are the conductance of SOT-MRAM1 and SOT-MRAM2, respectively. The conductance of SOT-MRAMs can be adjusted to realize negative and positive weights in a binary synapse. For instance, for $W_i = -1$, SOT-MRAM1 and SOT-MRAM2 should be in $P$ and $AP$ states, respectively. According to Eq. (1) $R_{AP} > R_P$, which means $G_{AP} < G_P$ since $G = 1/R$, therefore $G_{AP}^+ < G_{AP}^-$ and $Y_i < 0$.

III. PROPOSED SOT-MRAM BASED MLP ARCHITECTURE

Fig. 4 exhibit the training and inference paths of a proposed $n \times m$ SOT-MRAM based single layer perceptron, which are shown separately for simplicity. The synaptic connections are designed in the form of a crossbar architecture, in which the number of columns and rows are defined based on the number of nodes in input and output layers, respectively. During the training phase, the resistance of the SOT-MRAM based synapses will be tuned using the bit-lines (BLs) and source-lines (SLs) which are shared among different rows, as shown in Fig. 4 (a). The write word line (WWL) control signals will only activate one row in each clock cycle, thus the entire array can be updated using $j$ clock cycles, where $j$ is equal to the number of neurons in the output layer. Moreover, to tune the states of the SOT-MRAMs in the neurons according to requirements mentioned Section II.A, the BL and SL control signals for the neuron are set to VDD and VSS, respectively, as shown in Fig. 4 (a).

In the inference phase, the BL and SL control signals are in high-impedance (Hi-Z) state, and read word line (RWL) and WWL control signals are connected to VDD and GND, respectively. This will stop the write operation in synapses,
and generate $I^+$ and $I^-$ currents shown in Fig. 4 (b). The amplitude of produced currents depends on the input ($I^N$) signals and the resistances of SOT-MRAM synapses. Each row includes a shared differential amplifier, which generates an output voltage proportional to $\sum_i (I^+_{i,n} - I^-_{i,n})$ for the $n$th row, where $i$ is the total number of nodes in the input layer. Finally, the outputs of the differential amplifiers are connected to the SOT-MRAM based sigmoidal neurons. The entire inference operation occurs in parallel and in a single clock cycle. The required signaling to control the training and inference operations is listed in Table II. One of the main advantages of the proposed SOT-MRAM based perceptron architecture is that it can be readily concatenated to form an MLP classifier, which can still operate in a single clock cycle as it will be shown in Section V.

### IV. Hardware-Aware Learning Mechanism

To train the proposed SOT-MRAM based MLP classifier, a hardware-aware learning mechanism should be developed which incorporates the characteristics and limitations of our SOT-MRAM based neurons and synapses. Herein, we use a two-stage teacher-student approach, in which both teacher and student networks have identical topologies. Table III provides the notations and descriptions for teacher and student networks, in which $x$ is the input of the network and $y_i$ and $o_i$ are the input and output of the $i$th neuron, respectively.

To incorporate the features of the SOT-MRAM based synapses and neurons within our training mechanism, we have made two modifications to the approaches previously used for training binarized neural networks [7], [13]. First, we have used binarized biases in the student networks instead of real-valued biases. Second, since our SOT-MRAM neuron realizes real-valued sigmoidal activation function ($\text{sigmoid}(-x)$) without any computation overheads, we could avoid binarizing the activation functions and reduce the possible information loss in the teacher or student networks [7]. Herein, after each weight update in the teacher network we clip the real-valued weights within the $[-1, 1]$ interval, and then use the below deterministic binarization approach to binarize the weights:

$$ W_{ij} = \begin{cases} +1, & w_{ij} \geq \Delta_B \\ -1, & w_{ij} < \Delta_B \end{cases} \quad (3) $$

where $\Delta_B = 0$ is threshold parameters for binarized weights. Finally, once all the binarized weights are trained we will use a mapping mechanism to convert them to resistive states in SOT-MRAM based synapses according to Section II.B. It is worth noting that, the stochastic binarization [13] scheme can also be used to quantize the weights and biases. However, the stochastic rounding approach exhibits its advantages in deeper neural networks which are not the focus of this paper. In fact, we initially leveraged stochastic rounding in our simulations and while the training times were approximately 10-fold longer, the obtained accuracy values were comparable to those realized by the deterministic rounding approach.

### V. Simulation Results

#### A. Circuit-Level Simulation of SOT-MRAM based Neuron

Herein, we used the SPICE circuit simulator to measure the power consumption of our proposed SOT-MRAM based sigmoid neuron. The results obtained show the average power consumption of 64 $\mu$W for the SOT-MRAM based sigmoid neuron. Moreover, the layout design of the proposed neuron
circuit shows an area consumption of $13\lambda \times 30\lambda$, in which $\lambda$ is a technology-dependent parameter. Herein, we used the 14nm FinFET technology, which leads to the approximate area consumption of 0.02$\mu m^2$. Table IV provides a comparison between our SOT-MRAM based sigmoidal neuron and previous power- and area-efficient analog neurons [14], [15].

To provide a fair comparison in terms of area and power dissipation, we have utilized the general scaling method [16] to normalize the power dissipation and area of the designs listed in Table IV. Voltage and area scale at different rates of $U = \frac{0.78}{\sqrt{DD_x}}$ and $S = \frac{14nm}{tech - node}$, respectively, where $VDD_x$ and $tech - node$ are the nominal voltage and technology node used in the studied neuron designs. It shall be noted that we used 0.8 (V) nominal voltage and 14nm FinFET technology in our design. Moreover, power and area consumption values are scaled with respect to $1/U^2$ and $1/S^2$, respectively [16]. The results obtained exhibit that the proposed SOT-MRAM based neuron achieves significant area reduction, while realizing comparable power consumption compared to the existing power- and area-efficient analog neuron implementations. This leads to a $74\times$ and $12\times$ reduction in power-area product compared to the designs introduced in [14] and [15], respectively.

### B. Architecture-level Simulation

Herein, we developed a Python-based simulation framework based on [17] to realize the SPICE implementation of our SOT-MRAM based MLP classifier. Fig. 5(a) depicts the circuit realization of a $784 \times 16 \times 10$ SOT-MRAM based MLP classifier. A comparison between the MNIST [18] classification accuracy of SOT-MRAM MLP classifier and conventional real-valued and binarized MLP architectures is shown in Fig. 5 (b). The results show a comparable maximum classification accuracy of 86.54% and 85.56% in the first 10 epochs for binarized and SOT-MRAM based MLP classifiers, respectively.

Moreover, Table V provides a comparison between the analog IMC-based MLP classifier proposed herein and various hardware implementations of a $784 \times 16 \times 10$ binarized MLP architecture. As listed in the table, our analog MLP classifier completes the recognition task in a single clock cycle, while a highly-parallel digital implementation on GPU and a high-performance mixed-signal IMC architecture require at least $10^5$ and $10^2$ clock cycles, respectively, to complete the similar task. It is worth noting that digital CPU or GPU implementations can support higher clock frequencies as listed in the table. However, the difference between total clock cycles is so large that our analog IMC realization can still achieve at least four and five orders of magnitude performance improvement compared to GPU and CPU implementation, respectively.

### VI. Conclusion

In this paper, we proposed a power- and area-efficient SOT-MRAM based sigmoidal neuron, which was leveraged along-with SOT-MRAM based binary synapses to construct an analog IMC architecture for MLP classifiers. The developed neuron and synapse bitcells could be implemented within the same memory subarray, enabling a single-cycle operation for the analog IMC-based MLP architecture while removing the need for signal conversion units. We implemented a $784 \times 16 \times 10$ SOT-MRAM based MLP using the SPICE circuit simulator and compared its performance with various hardware realizations of an MLP classifier. The results exhibited at least two orders of magnitude increase in the processing speed of our analog IMC architecture compared to the highest performance MLP classifier implemented on a mixed-signal analog/digital IMC architecture.
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