A study on modeling and simulation of Multiple-Gate MOSFETs

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Abstract. Endless scaling of planar MOSFET over the past four decades has delivered proliferating transistor density and performance to integrated circuits (ICs) at the cost of increase in short channel effects (SCEs). As a result of narrow channel lengths in deeply scaled MOSFETs, off-state leakage current happens to increase the power requirement of device by forcing drain potential to lose its leverage over the electrostatics of channel. Multigate devices (Double Gate FET, FinFET) promise better immunity to SCEs by concealing the issues caused by scaling of planar technology, and also exhibits better scalability with increased level of integration. In this paper, a study on modeling and simulation of multiple-gate MOSFETs is presented. This paper describes the development in semiconductor technology from planar to non-planar devices, benefits of multigate MOSFETs over previous technologies. Effects of varying different parameters (such as Fin thickness, Fin height, use of different gate material etc.) in multigate (specially FinFET) devices is also described. Improvement in device physics models along with technology, and importance of computational physics for efficient modeling of nanoscale devices is presented.

1. Introduction
As the semiconductor technology moves towards nanoscale length, complexity to design and fabricate devices has increased to achieve desired accuracy and results. Endless scaling of bulk CMOS resulted in SCEs, leakage current, power consumption and threshold voltage roll-off. Several alternatives to CMOS scaling were used to move forward with scaling, are as follows: i) use of strained silicon to increase mobility whereby enhancing drive current, ii) high-K materials are being used to achieve same level of results without compromising drive current, iii) Silicon on Insulator (SOI) emerged as one of the best alternative prior to multigate technology to reduce power consumption, leakage, with better isolation, high reliability and speed. Multigate transistors emerged as the new hope for semiconductor technology, extending development beyond nanometer length with better control over channel, eliminating SCEs and threshold voltage roll-off. Among multigate devices FinFET shows promising results with variation in various parameters such as Fin thickness, Fin height and use of different gate materials.

Even with recent advancement in technology, it is hard to model and simulate nanoscale devices because of the level of physics involved at this structural complexity. Device modeling has moved from classical to quantum models in order to incorporate physical phenomenon involved in short channel devices. Complexity in device modeling and simulation further increases as we include quantum models for nano length devices. Parallel processing of simulation environment...
with graphical processing units and other accelerators have shown improvement in accuracy and speed for device simulation.

This paper is organized as follows. In Section 2, shift from planar to non-planar technology, multigate technology and its benefits over previous technology is described along with variations in different parameters of FinFET device and models used for modeling of multigate devices are described. In Section 3, improvement in device physics models along with technology and importance of computational physics for better study of nanoscale devices is described. Section IV concludes the paper along with discussion of the work presented in this paper.

2. Beyond Planar CMOS Technology

Planar CMOS scaling was limited by SCEs, leakage current, power consumption and threshold voltage roll-off. Several advanced techniques are discussed here to reduce the drawbacks of CMOS scaling.

2.1. Strained Si

As the device size shrinks, mobility decreases, in order to enhance mobility silicon is strained, resulting in higher drive current ($I_{ON}$) under the same conditions i.e. with lower supply voltage and thick gate oxide. Trade-off can be achieved among current drive, short channel effects and power consumption. In strained silicon, atoms are stretched beyond their atomic distance as shown in the figure 1, which is achieved by developing a thin layer of Si epitaxially on material with higher lattice constant. Strained Si have significant disadvantage in the form of self-heating effects due to lower thermal conductivity and dislocation effects in epitaxial layer [1]. Self-heating effects can be overcome by reducing the thickness of epitaxial layer in the device structure. The remarkable advantage of strained Si is improved mobility even at high effective fields, resulting in approximate $70\%$ increment in mobility with $30\%$ of speed improvement [2].

![Figure 1. Strained Silicon.](image1)

![Figure 2. High K Metal Gate transistor.](image2)

2.2. High K material

With constant scaling of device size into nanoscale technology, scaled gate oxide results in exponential increase of gate leakage current. With the number of transistors on a single chip growing exponentially, power dissipation becomes a big problem. To reduce the gate leakage current in ultra-small devices without adjusting the ON state current of MOS device, reduced electrical oxide thickness (EOT) of gate dielectric are required. High K material in case of fully depleted silicon on insulator (FD-SOI) or thin film (e.g. FinFET) has improved short channel effects and thus loosens up the requirements for EOT scaling. Direct interface between high-K dielectric and poly-silicon gate has some limitation such as photon scattering which degrades the carrier mobility, thermal instability and a direct shoot up in threshold voltage value. To eliminate these limitations, metal gate electrode is used with the high-K gate insulator as shown in figure 2.
2.3. Silicon on Insulator (SOI)

SOI structure is similar to the conventional bulk structure except the presence of buried layer which is grown by the oxygen ions in the Si as shown in figure 3, which provides full dielectric isolation to active Si layer from the main substrate with the help of buried oxide layer, that allows the use of relatively high resistivity main substrate, causing a significant reduction in parasitic [3] and leakage current in substrate. Contrary to bulk Si transistor, SOI technology has become attractive way for the fabrication of advanced CMOS ICs because of low supply voltage, minimum power consumption features [4], higher drive current, excellent device isolated structure, high reliability and high speed due to elimination of vertical as well as sidewall capacitances. SOI CMOS transistors suffers from self heating effect which appears only when the transistor is in conduction mode. But this effect certainly will not eliminate the global usage of SOI for CMOS ICs.

![Figure 3. Silicon on insulator.](image)

![Figure 4. (A) Bulk MOSFET (B) Double-gate MOSFET (C) FinFET (Trigate MOSFET)](image)

2.4. Multigate transistors

With so many alternative after the bulk MOS transistor, a more promising device structure or alternative was required to extend the growing semiconductor technology to overcome short channel effects such as drain induced barrier lowering (DIBL), threshold voltage roll off and to get the precise control over channel current. Multigate transistor emerged as the promising candidate for enhancing the performance and scaling properties of device, among multigate transistors dual-gate MOSFET (DG-MOSFET) as shown in figure 4 with aligned planar gate structure provides improved channel control but its fabrication process is more challenging. With ease of fabrication, FinFET and Trigate FETs have emerged as the dominant structure. FinFET has an advantage to be fabricated on bulk as well as on SOI, obtained by etching thin silicon strip called fins with gate electrodes occupying the sidewalls of silicon strips. SOI FinFETs have better isolation as they are isolated by very shallow trench isolation than bulk FinFETs which have common substrate for isolation.

Thickness and height of Fin are the two important parameter which are used to control short channel effects [5]. Thinner Fin has much better control over short channel effects [6] than that of thick Fin, as in later case channel barrier is lowered by drain electric field due to the reduction in source/Fin and drain/Fin capacitances. Fin thickness plays an important role to overpower short channel effects, as DIBL is increased with the increment in Fin thickness. Drive current capability of FinFET is mainly controlled by Fin height, as noticed in[7] increment in Fin height degrades off-state leakage current. In case of tri-gate MOSFET, use of different gate material shows significantly improved performance[8] in terms of surface potential, electric field and carrier velocity distribution over double or single material gate.

Modelling of multigate device started with double gate MOSFET. Two models are discussed here which have the major contribution among multigate device modelling.
- **Taur Models**: Taur [9] solved the Poisson equation for the case of intrinsic doping concentration as follows, neglecting fixed charges:

\[
\frac{d^2 \varphi}{dx^2} = \frac{q n_i e^{-\varphi/V}}{\epsilon_s} \tag{1}
\]

where:

- \( \varphi \) changes across the thickness of the film and \( V \) changes along the channel.
- \( q \) is electrostatic charge, \( n_i \) is intrinsic carrier density, \( T \) is temperature in Kelvin and \( \epsilon_s \) is dielectric permittivity.

After two integration, the surface potential \( \varphi_s \) along the channel is obtained as function of a constant intermediate calculation parameter \( \beta \):

\[
\varphi_s(x) = V - 2\varphi_f \ln \left( \frac{t_s}{2\beta L_{Di}} \cos \left( \frac{2\beta}{t_s} x \right) \right) \tag{2}
\]

where \( t_s \) is the silicon layer thickness, \( L_{Di} \) is the intrinsic Debye length and \( \varphi_f \) is the thermal voltage \( kT/q \).

- **BSIM-MG Model**: In 2012 the BSIM-MG model [10] was adopted as industry standard. Two cases were considered mainly to formulate models: symmetric or common gate (CMG) and asymmetric gates (IMG). This model already considers the silicon layer doping concentration and short-channel effects. In the case of symmetric gates and doped silicon layer, Poisson's equation is solved using the perturbation method approach. The general equation has two terms: the first term attributed to inversion charges only and second term attributed to body doping \( N_a \), where \( \varphi_f \) is the Fermi potential:

\[
\frac{d^2 \varphi}{dx^2} = \frac{q n_i e^{-\varphi/V}}{\epsilon_s} + \frac{q N_a}{\epsilon_s} \tag{3}
\]

This solution has two terms, \( \varphi_1 \) considering only the first term, and \( \varphi_1 \) solving the second term as a perturbation. After defining a function of \( \beta \), the sequence of calculation is the following:

\[
f(\beta) = \ln(\beta) - \ln(\cos(\beta)) - \frac{V_{gfb} - V}{2\varphi_T} - \ln \left[ \frac{t_s}{2} \sqrt{ \frac{q n_i^2}{2\epsilon_s \varphi_T N_a} + M(\beta) } \right] = 0 \tag{4}
\]

where:

\[
M(\beta) = \frac{2C_s}{C_{ox}} \beta^2 \left[ \frac{e^{\varphi_T}}{\cos \beta^2} - 1 \right] + \frac{\varphi_f}{\varphi_T^2} (\varphi_f - 2\varphi_T \ln[\cos(\beta)]) \tag{5}
\]

and

\[
V_{gfb} = V_{gs} - V_{fb} - V \tag{6}
\]

Solution of equation 4 can be obtained by: 1) Newton-Raphson method; 2) table look approach; 3) analytical approximation with good initial solution \( \beta_0 \) and corrections of 3rd order h.
3. Development in device Modeling

As the device size shrinks, physics involved in device and its understanding became very important and so does the physical phenomenon used to describe device characteristic. Earlier for long channel devices, Drift Diffusion model was used to define the device physics [11], since it could not deal with hot carrier effects and it was good for gate length greater than 500nm. To overcome the hot carrier effects for shorter channel devices (upto 100nm of gate length) Hydrodynamic models [12] were used to describe the device physics. Hydrodynamic models have become a practice in industry for describing device physics with certain variation in different parameters (e.g. impact ionization coefficient, mobility, etc.). However for ultra-small devices these models do not have exact predictive power, for that some of the approximations [13] need to be relaxed and Quantum transport models should be considered with inclusion of quantum effects, small-geometry effects and SCEs to overcome quantum mechanical restraints along channel, as shown in the hierarchical map [14] of transport models.

| Model                          | Improvements                      |
|-------------------------------|-----------------------------------|
| Compact models                | Appropriate for circuit design    |
| Drift-Diffusion equations     | Good for device down to 0.5µm     |
| Hydrodynamics equations       | Velocity overshoot effect can be treated properly |
| Boltzmann transport equation  | Accurate up to classical limits   |
| Monte Carlo/CA methods       | Keep all classical hydrodynamics features + quantum corrections |
| Quantum Hydrodynamics         | Keep all classical hydrodynamics features + quantum corrections |
| Quantum Monte Carlo/CA methods| Keep all classical features + quantum corrections |
| Quantum-Kinetic equations     | Accurate up to single particle description |
| (Liouville, Wigner-Boltzmann) |                                   |
| Green’s function method       | Includes correlation in both space and time domain |
| Direct solution of the n-body Schrodinger equation | Can be solved only for small number of particles |

**Figure 5.** Hierarchy in Device Modeling[14].

Even with recent advancement in technology, the present technology [15] is unable to tackle new challenges in scaling of semiconductor devices from classical down to quantum scale devices as shown in figure 5. Classical models based on drift-diffusion model equations are certainly inadequate for device length below 200nm, even typical Hydrodynamic model do not provide exact description of device physics as they neglect some important contribution in the channel region. Computational changes results in limited performance of emerging device technology as self-consistent solution of coupled transport-field equation is required and also both the transport and the Poisson’s equations are needed to be solved over 3D domain, requiring highly accurate algorithms with high-end computational platform. It is very challenging to both computationally and from device physics perspective to solve for appropriate level of accuracy required to describe and calculate the device characteristic.
4. Conclusion
A study of progress in semiconductor technology is presented with improvements among various technologies. Multigate transistors have better control over channel thus gives better performance to previous technologies. Multigate devices emerged to extend semiconductor technology beyond nano meter of channel length. With variation in certain parameters of multigate device better results were found. Device modeling and simulation plays important role in scaling. To develop a new device and test its functionality, exact modeling of device is required to understand the physics involved. To get the faster and accurate results on simulation environment, parallel processing of simulation is required on graphical processing units. Several method to fasten the solving algorithms and to get accurate results are used, such as use of finite element method (FEM) for complex geometries over finite difference method (FDM). Study in this paper provides a huge scope in development of new tools for device modeling and simulation.

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