Gating of high-mobility InAs metamorphic heterostructures

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We investigate the performance of gate-defined devices fabricated on high mobility InAs heterostructures. The magnetotransport properties of these structures strongly depend on the surface states. Heterostructures terminated in In\(_{0.75}\)Ga\(_{0.25}\)As are found to host a conductive sheet of electrons depending on details of epitaxial growth or deposition of the dielectric material and limit the performance of gate-defined devices. However, In\(_{0.75}\)Al\(_{0.25}\)As capped heterostructures show a robust gating behavior suitable for fabrication of gate-defined mesoscopic devices.

Narrow band gap semiconductors such as InAs are of fundamental interest for next generation high-speed electronics due to their unique material properties of small effective mass, large dielectric constant and high room temperature mobility \(^1\)\(^2\). In addition, they possess strong spin orbit interaction and large g-factor which make them an ideal platform for spintronics applications \(^3\)\(^4\). Recently, two-dimensional electron systems (2DESs) confined to InAs layers have become the focus of renewed theoretical and experimental attention partly because of their potential applications in quantum computation \(^5\)\(^7\). However, all these applications require precise control of electrostatic potentials and carrier densities using nano-fabricated metallic gates. Unlike widely used GaAs systems, reliable gating has proven difficult in InAs systems due to gate leakage and hysteretic behavior. Charge traps and surface Fermi level pinning could drastically affect the device performance. Controlling surface states in In\(_x\)Ga\(_{1-x}\)As material has played a crucial role in achieving high quality interfaces for metal oxide semiconductor field effect transistors (MOSFETs) \(^2\). The capping layer material and its surface states will also influence the gating efficiency of buried quantum wells.

The Fermi level pinning at semiconductor surfaces has been the subject of numerous theoretical and experimental studies \(^8\). In most semiconductors, such as GaAs, the Fermi level is pinned in the band gap \(^10\). It is well known that the surface states in case of InAs (100) can result in a two dimensional electron system \(^8\). The electron accumulation is due to pinning of the Fermi level above the conduction band minimum. The position of the pinning level sensitively depends on the material and the surface treatments \(^11\). In the case of high indium content InGaAs, the situation is similar to InAs. Experiments on In\(_x\)Ga\(_{1-x}\)As predicts Schottky barrier height becomes negative, exhibiting an ohmic behavior, for \(x > 0.85\) \(^12\). In this work, we grow two structures under different growth conditions with In\(_{0.75}\)Ga\(_{0.25}\)As capping layers. On the same structures we remove the capping layer with wet chemical etching terminating the surface with In\(_{0.75}\)Al\(_{0.25}\)As. We study the gating properties of these structures and conclude the In\(_{0.75}\)Al\(_{0.25}\)As capping layers yield stable gate-defined devices.

The samples were grown on a semi-insulating InP (100) substrate, using a modified VG-V80H molecular beam epitaxy system. After oxide desorption under an As\(_4\) overpressure at 520 °C the substrate temperature is lowered to 480 °C where we grow a superlattice of InGaAs/InAlAs lattice matched to InP. The Substrate temperature is further lowered to 300 °C for growth of the In\(_{0.75}\)Ga\(_{0.25}\)As buffer layer. This lower temperature buffer growth is necessary to reduce and minimize the influence of dislocations forming due to the lattice mismatch of the active region to the InP substrate. The indium content is step graded from \(x = 0.52\) to 0.85 \(^12\)\(^13\). We lower the indium content to \(x = 0.75\) while increasing the substrate temperature to \(T_{sub} \sim 460\)°C with As\(_4\) beam equivalent pressure (BEP) to 2.5×10\(^{-5}\) for sample A and \(T_{sub} \sim 490\)°C and with 2.0×10\(^{-5}\) BEP for sample B. The quantum well consists of 4 nm InAs layer sandwiched by In\(_{0.75}\)Ga\(_{0.25}\)As layers for both samples. A In\(_{x}\)Al\(_{1-x}\)As

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
Layer & Description \\
\hline
In\(_{1-x}\)Ga\(_x\)As (10 nm) & Sample A \\
In\(_{1-x}\)Al\(_x\)As (120nm) & Sample A \\
In\(_{1-x}\)Ga\(_x\)As (10.5 nm) & \\
In\(_{1-x}\)Al\(_x\)As (10.5 nm) & \\
In\(_{1-x}\)Al\(_x\)As & Low temperature step graded buffer (\(\sim 1\)μm) \\
S.I. InP substrate (100) & \\
\hline
\end{tabular}
\caption{Layer thickness for InAs/GaAs/InAlAs quantum well.
\label{tab:layer_thickness}}
\end{table}

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig1.png}
\caption{(Color online) (a) schematic of the quantum well containing InAs layer. (b) Hall and (c) longitudinal magnetotransport for InGaAs capped heterostructure (sample A) shown in (a).
\label{fig:fig1}}
\end{figure}

FIG. 1: (Color online) (a) schematic of the quantum well containing InAs layer. (b) Hall and (c) longitudinal magnetotransport for InGaAs capped heterostructure (sample A) shown in (a).
(120 nm) top barrier layer is grown next as shown in Fig. 1(a). Finally, the structures are capped with a 10 nm In$_{0.75}$Ga$_{0.25}$As layer. The structures are nominally undoped but the deep levels in InAlAs donate carriers to the quantum well.

Figure 1(b) and (c) show Hall, $R_{xy}$, and longitudinal, $R_{xx}$, magnetotransport measurements on sample A in a Hall bar geometry at $T = 2$ K. The $R_{xx}$ shows a positive slope magnetoresistance and very weak Shubnikov de-Haas oscillations. The Hall data also shows two slopes with $R_{xx}$ mixing. Both sets of data suggest a multi-carrier transport with the simplest case being a two-carrier transport consisting of an extra conductive sheet of electrons in addition to our quantum well. We can fit both $R_{xx}$ and the Hall data reasonably well with one layer having a high mobility $> 10^5$ cm$^2$/Vs and low density $\sim 4 \times 10^{11}$ cm$^{-2}$ carriers which matches well with our quantum well and the other layer having high density $4 \times 10^{12}$ cm$^{-2}$ and low mobility $4 \times 10^{5}$ cm$^2$/Vs mobility. The fits to $R_{xx}$ and $R_{xy}$ are shown in Fig. 1(b) and (c) as dashed red curves. We believe that this high density, low mobility parallel conduction channel arises from the surface states which could pin the Fermi level above the conduction band minimum in the InGaAs, capping layer. Gated-Hall bars fabricated on sample A with InGaAs capping layers did not show significant response to gating, probably due to shielding of the electric field by the surface charges. By removing the InGaAs capping layer of the same wafer in a H$_3$PO$_4$·H$_2$O$_2$·H$_2$O solution the magneto-transport is drastically modified. Figure 2(a) shows the measured longitudinal and Hall data of the InAlAs surface terminated Hall bar. $R_{xx}$ shows integer quantum Hall states with corresponding quantization of Hall data. We measure a density of $3 \times 10^{11}$ cm$^{-2}$ with a mobility of $3 \times 10^5$ cm$^2$/Vs. We fabricated a gated-Hall bar by deposition of 100 nm SiO$_2$ at a substrate temperature of 250°C using plasma enhanced chemical vapor deposition (PECVD) and a subsequent 100 nm Ti/Au as a metallic gate. Carrier densities could be tuned over a wide range of densities with InAlAs cap as shown in Fig. 2(b).

Sample B, which is grown under lower As overpressure and higher substrate temperature compared to sample A, shows no sign of significant two-carrier transport. Figure 3(a) shows $R_{xx}$ data for sample B capped with InGaAs. Clearly growth condition could affect the surface states.
(dangling bonds) and the corresponding Fermi level pinning position at the surface. There has been a great deal of experimental and theoretical studies carried out in the field of III-V MOSFET transistors where Fermi level pinning has been studied at the semiconductor-oxide interface [8]. The number of trap states largely varies depending on the dielectric material and technique used for deposition. Here we fabricate a gated-Hall bar using PECVD grown SiO₂ similar to sample A. The density of carriers, n, does not change as top gate voltage, Vg, is decreased (green squares in Fig. 3(d)). This poor efficiency in gating carrier density suggests formation of surface charge most likely due to defect states at the semiconductor-oxide interface. These states are schematically shown in Fig. 3(b).

We introduce here a technique to measure the density of this surface charge. At room temperature we apply a positive bias, Vp, and start cooling down the device to 2 K. At room temperature under a positive bias the surface states are filled by mobile electrons from the InGaAs surface cap layer. As the temperature is lowered, many of these electrons are frozen in place, even when the bias is turned off, leading to a lower number of free carriers in the surface as shown in Fig. 3c. This technique has been successfully used in GaAs material system for showing surface charge most likely due to defect states at the semiconductor-oxide interface. These states are schematically shown in Fig. 3(b).

When the InGaAs capping layer is removed using wet chemical etching, we do not observe a drastic change in the quality of the magnetotransport, however, the gating properties changes dramatically. Figure 4(a) shows the gate bias dependence of the density for an InAlAs capped device. The device is cooled down under no bias. The density could be varied in a wide range. The measured mobility as a function of density at 2 K for both samples A and B are well-fitted by \( \mu \sim n^\alpha \), with \( \alpha = 0.8 \) at high density range \( n > 2 \times 10^{11} \text{ cm}^{-2} \). A value of \( \alpha \sim 0.8 \) signifies that the mobility is limited by scattering from nearby background charged impurities [10].


culated quantum devices using these heterostructures such as quantum point contacts (QPCs) show no gate leakage and no hysteretic behavior. Figure 4(b) shows the plot of conductance as a function of side-gate bias shows quantization at 0.7 and 1 in units of \( 2e^2/h \).

In conclusion, we have studied the effect of surface states on gating performance of InAs heterostructures. We find that the surface of InGaAs is prone to Fermi level pinning due to details of epitaxial growth or deposition of the dielectric material. However, InAlAs surfaces show a robust gating behavior and allow fabrication of reliable gate-defined mesoscopic devices.

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