Laconic Deep Learning Computing

Sayeh Sharify, Mostafa Mahmoud, Alberto Delmas Lascorz, Milos Nikolic, Andreas Moshovos
Electrical and Computer Engineering, University of Toronto
{sayeh, delmasl1, moshovos}@ece.utoronto.ca,
{mostafa.mahmoud, milos.nikolic}@mail.utoronto.ca

ABSTRACT

We motivate a method for transparently identifying ineffec-
tual computations in unmodified Deep Learning models and
without affecting accuracy. Specifically, we show that if we
decompose multiplications down to the bit level the amount
of work performed during inference for image classification
models can be consistently reduced by two orders of magni-
tude. In the best case studied of a sparse variant of AlexNet,
this approach can ideally reduce computation work by more
than 500×. We present Laconic a hardware accelerator that
implements this approach to improve execution time, and
energy efficiency for inference with Deep Learning Networks.
Laconic judiciously gives up some of the work reduction po-
tential to yield a low-cost, simple, and energy efficient de-
sign that outperforms other state-of-the-art accelerators. For
elementary, Laconic configuration that uses a weight memory
interface with just 128 wires outperforms a conventional ac-
celerator with a 2K-wire weight memory interface by 2.3×
on average while being 2.13× more energy efficient on av-
average. A Laconic configuration that uses a 1K-wire weight
memory interface, outperforms the 2K-wire conventional ac-
celerator by 15.4× and is 1.95× more energy efficient. La-
conic does not require but rewards advances in model design
such as a reduction in precision, the use of alternate numeric
representations that reduce the number of bits that are “1”,
or an increase in weight or activation sparsity.

1. MOTIVATION

Modern computing hardware is energy-constrained and
thus developing techniques that reduce the amount of energy
required to perform the computation is essential for im-
proving performance. The bulk of the work performed by con-
volutional neural networks during inference is due to 2D con-
volutions (see Section 2). In turn, these convolutions entail
numerous multiply-accumulate operations were most of the
work is due to the multiplication of an activation \textit{A} and a
weight \textit{W}. In order to improve energy efficiency a hardware
accelerator can thus strive to perform only those multiplica-
tions that are effectual which will also lead to fewer addi-
tions. We can approach a \textit{A} \times \textit{W} multiplication as a mono-
lithic action which can be either performed or avoided in
its entirety. Alternatively, we can decompose it into a col-
lection of simpler operations. For example, if \textit{A} and \textit{W}
are 16b fixed-point numbers \textit{A} \times \textit{W} can be approached as 256
1b \times 1b multiplications or 16 16b \times 1b ones.

Figure 1 reports the potential reduction in work for sev-
eral ineffectual work avoidance policies. The “A” policy
avoids multiplications where the activation is zero. This is
representative of the first generation of value-based accel-
erators that were motivated by the relatively large fraction of
zero activations that occur in convolutional neural networks,
e.g., Cnvlutin [1]. The “A+W” skips those multiplications
where either the activation or the weight are zero and is rep-
resentative of accelerators that target sparse models where
a significant fraction of synaptic connections has been pruned,
e.g., SCNN [2]. The “Ap” (e.g., Stripes [3] or Dynamic
Stripes [4]) and “Ap+Wp” (e.g., Loom [5]) policies target
precision for the activations alone or for the activations and
the weights respectively. It has been found that neural net-
works exhibit variable per layer precision requirements. All
aforementioned measurements corroborate past work on ac-
celerator designs that exploited the respective properties.

However, we show that further potential for work reduc-
tion exists if we decompose the multiplications at the bit
level. Specifically, for our discussion we can assume with-
out loss of generality that these multiplications operate on
16b fixed-point values. The multiplication itself is given by:

\[
A \times W = \sum_{i=0}^{15} \sum_{j=0}^{15} A_i \text{ AND } W_j \quad (1)
\]

where \(A_i\) and \(W_j\) are bits of \textit{A} and \textit{W} respectively. When
decomposed down to the individual 256 single bit multipli-
cations one can observe that it is only those multiplica-
tions where both \(A_i\) and \(W_j\) are non-zero that are effectual. Accord-
ingly, the “Ab” (e.g., Pragmatic [6]) and “Ab+Wb” measure-
ments show the potential reduction in work that is possible if
we skip those single bit multiplications where the activation
bit is zero or whether either the activation or the weight bits
are zero respectively. The results show that the potential is
far greater than the policies discussed thus far.

Further to our discussion, rather than representing \textit{A} and
\textit{W} as bit vectors, we can instead Booth-encode them as a
series of signed powers of two, or terms (higher-radix Booth
encoding is also possible). In this case the multiplication is
given by:

\[
A \times W = \sum_{i=0}^{15} \sum_{j=0}^{15} A_i \text{ \text{BOOTH-}\ AND } W_j \quad (2)
\]
Figure 1: Performance improvement potential for: 1) skipping zero activations [1], 2) skipping zero activations and weights, 3) using static precision for activations [3], 4) using static precision for activations and weights, 5) skipping zero bits of activations [6], 6) skipping zero bits of activations and weights, 7) skipping zero bits of activations using booth encoding [6], 8) skipping zero bits of activations and weights using booth encoding (logarithmic scale).

\[ A \times W = \sum_{i=0}^{A_{\text{terms}}} \sum_{j=0}^{W_{\text{terms}}} A_{ti} \times W_{tj} \]  

where \( A_{ti} \) and \( W_{tj} \) are of the form \( \pm 2^x \). As with the positional representation, it is only those products where both \( A_{ti} \) and \( W_{tj} \) are non-zero that are effectual. Accordingly, the figure shows the potential reduction in work with “At” where we skip the ineffectual terms for a Booth-encoded activation (e.g., Pragmatic [6]), and with “At+Wt” where we calculate only those products where both the activation and the weight terms are non-zero. The results show that the reduction in work (and equivalently the performance improvement potential) with “At+Wt” is in most cases two orders of magnitude higher than the zero value or the precision based approaches. Based on these results, our goal is to develop a hardware accelerator that computes only the effectual terms. No other accelerator to date has exploited this potential. Moreover,
by targeting "At+Wt" we can also exploit "Ab+Wb" where the inputs are represented in a plain positional representation and are not Booth-encoded.

2. BACKGROUND

This section provides the required background information as follows: Section 2.1 reviews operation of a Convolutional Neural Network and Section 2.2 goes through our baseline system.

2.1 Convolutional Layers

Convolutional Neural Networks (CNNs) usually consist of several Convolutional layers (CVLs) followed by a few fully-connected layers (FCLs). In many image-related CNNs most of the operation time is spent on processing CVLs in which a 3D convolution operation is applied to the input activations producing output activations. Figure 2 illustrates a CVL with a $c \times x \times y$ input activation block and $N c \times h \times k$ filters. The layer dot products each of these $N$ filters (denoted $f^0, f^1, ..., f^{N-1}$) by a $c \times h \times k$ subarray of input activation, called window, to generate a single $o_h \times o_k$ output activation. In total convolving $N$ filters and an activation window results in $N o_h \times o_k$ outputs which will be passed to the input of the next layer. The convolution of activation windows and filters takes place in a sliding window fashion with a constant stride $S$.

Fully-connected layers can be implemented as convolutional layers in which filters and input activations have the same dimensions, i.e., $x = h$ and $y = k$.

2.2 Baseline system

Our baseline design (BASE) is a data-parallel engine inspired by the DaDianNao accelerator which uses 16-bit fixed-point activations and weights. Our baseline configuration has 8 inner product units (IPs) each accepting 16 input activations and 16 weights as inputs. The 16 input activations are broadcast to all 8 IPs; however, each IP has its own 16 weights. Every cycle each IP multiplies 16 input activations by their 16 corresponding weights and reduces them into a single partial output activation using a 16 32-bit input adder tree. The partial results are accumulated over the multiple cycles to generate the final output activation. An activation memory provides the activations and a weight memory provides the weights. Other memory configurations are possible.

3. Laconic: A SIMPLIFIED EXAMPLE

This section illustrates the key concepts behind Laconic via an example using 4-bit activations and weights.

Bit-Parallel Processing: Figure 3a shows a bit-parallel engine multiplying two 4-bit activation and weight pairs, generating a single 4-bit output activation per cycle. Its throughput is two $4b \times 4b$ products per cycle.

Bit-Serial Processing: Figure 3b shows an equivalent bit-serial engine which is representative of Loom (LM) [5]. To match the bit-parallel engine’s throughput, LM processes 8 input activations and 8 weights every cycle producing 32 $1b \times 1b$ products. Since LM processes both activations and weights bit-serially, it produces 16 output activations in $P_a \times P_w$ cycles where $P_a$ and $P_w$ are the activation and weight precisions, respectively. Thus, LM outperforms the bit-parallel engine by $\frac{16}{P_a \times P_w}$. In this example, since both activations and weights can be represented in three bits, the speedup of LM over the bit-parallel engine is $1.78 \times$. However, LM still processes some ineffectual terms. For example, in the first cycle 27 of the 32 $1b \times 1b$ products are zero and thus ineffectual and can be removed.

Laconic: Figure 3c illustrates a simplified Laconic engine in which both the activations and weights are represented as vectors of essential powers of two, or one-offsets. For example, $A_0 = (110)$ is represented as a vector of its one-offsets $A_0 = (2, 1)$. Every cycle each PE accepts a 4-bit one-offset of an input activation and a 4-bit one-offset of a weight and adds them up to produce the power of the corresponding product term in the output activation. Since Laconic processes activation and weight “term”-serially, it takes $t_a \times t_w$ cycles for each PE to complete producing the product terms of an output activation, where $t_a$ and $t_w$ are the number of one-offsets in the corresponding input activation and weight. The engine processes the next set of activation and weight one-offsets after $T$ cycles, where $T$ is the maximum $t_a \times t_w$ among all the PEs. In this example, the maximum $T$ is 6 corresponding to the pair of $A_0 = (2, 1)$ and $W_0 = (2, 1, 0)$ from $PE(1, 0)$. Thus, the engine can start processing the next set of activations and weights after 6 cycles achieving $2.67 \times$ speedup over the bit-parallel engine.

4. Laconic

This section presents the Laconic architecture by explaining its processing approach, processing elements structure, and its high-level organization.

4.1 Approach

Laconic’s goal is to minimize the required computation for producing the products of input activations and weights by processing only the essential bits of both the input activations and weights. To do so, $LAC$ converts, on-the-fly, the input activations and weights into a representation which contains only the essential bits, and processes per cycle one pair of essential bits one from an activation and another from a weight. The rest of this section is organized as follows: Section 4.1.1 describes the activation and weight representations in $LAC$ and Section 4.1.2 explains how $LAC$ calculates the product terms.

4.1.1 Activation and Weight Representation
For clarity we present a LAC implementation that processes the one-offsets, that is the non-zero signed powers of two in a Booth-encoded representation of the activations and weights (however, LAC could be adjusted to process a regular positional representation or adapted to process representations other than fixed-point). LAC represent each activation or weight as a list \((o_n, \ldots, o_0)\) of its one-offsets. Each one-offset is represented as \((\text{sign}, \text{magnitude})\) pair. For example, an activation \(A = -2(10) = 1110(2)\) with a Booth-encoding of 0010(2) would be represented as \((-1, 1)\) and a \(A = 7(10) = 0111(2)\) will be presented as \((+3), (-0))\). The sign can be encoded using a single bit, with, for example, 0 representing “+” and 1 representing “-”.

### 4.1.2 Calculating a Product Term

LAC calculates the product of a weight \(W = (W_{\text{terms}})\) and an input activation \(A = (A_{\text{terms}})\) where each term is a \((\text{sign}, \text{magnitude}) = (s_i, t_i)\) as follows:

\[
W \times A = \sum_{\forall(s, t) \in W_{\text{terms}}} (-1)^s 2^t \times \sum_{\forall(s', t') \in A_{\text{terms}}} (-1)^{s'} 2^{t'}
\]

\[
= ((-1)^s 2^{t_0} + (-1)^s 2^{t_1} + \cdots + (-1)^s 2^{t_n}) \times
((-1)^{s'} 2^{t'_0} + (-1)^{s'} 2^{t'_1} + \cdots + (-1)^{s'} 2^{t'_m})
\]

\[
= ((-1)^s (-1)^s 2^{t_0} 2^{t'_0} + \cdots + ((-1)^s (-1)^s 2^{t_0} 2^{t'_m}) + \cdots + ((-1)^s (-1)^s 2^{t_n} 2^{t'_0}) + \cdots + ((-1)^s (-1)^s 2^{t_n} 2^{t'_m}))
\]

\[
= ((-1)^{s+s'} 2^{t_0+t'_0} + \cdots + (-1)^{s+s'} 2^{t_0+t'_m}) + \cdots + ((-1)^{s+s'} 2^{t_n+t'_0} + \cdots + (-1)^{s+s'} 2^{t_n+t'_m})
\]

That is, instead of processing the full \(A \times W\) product in a single cycle, LAC processes each product of a single \(t\) term of the input activation \(A\) and of a single \(t\) term of the weight.
$W$ individually. Since these terms are powers of two so will be their product. Accordingly, LAC can first add the corresponding exponents $t'+t$. If a single product is processed per cycle, the $2^{t'+t}$ final value can be calculated via a decoder. In the more likely configuration where more than one term pairs are processed per cycle, LAC can use one decoder per term pair to calculate the individual $2^{t'+t}$ products and then an efficient adder tree to accumulate all. This is described in more detail in the next section.

### 4.2 Processing Element

Figure 4 illustrates how the LAC Processing Element (PE) calculates the product of a set of weights and their corresponding input activations. Without loss of generality we assume that each PE multiplies 16 weights, $W_0,...,W_{15}$, by 16 input activations, $A_0,...,A_{15}$. The PE calculates the 16 products in 6 steps:

**Step 1**: The PE accepts 16 4-bit weight one-offsets, $t_0,...,t_{15}$ and their 16 corresponding sign bits $s_0,...,s_{15}$, along with 16 4-bit activation one-offsets, $i_0,...,i_{15}$ and their signs $s'_0,...,s'_{15}$, and calculates 16 one-offset pair products. Since all one-offsets are powers of two, their products will also be powers of two. Accordingly, to multiply 16 activations by their corresponding weights LAC adds their one-offsets to generate the 5-bit exponents $(t_0+i_0),...,t_{15}+i_{15}$ and uses 16 XOR gates to determine the signs of the products.

**Step 2**: For the $i^{th}$ pair of activation and weight, where $i \in \{0,...,15\}$, the PE calculates $2^{t_i+i_i}$ via a 5b-to-32b decoder which converts the 5-bit exponent result $(t_i+i_i)$ into its corresponding one-hot format, i.e., a 32-bit number with one “1” bit and 31 “0” bits. The single “1” bit in the $i^{th}$ position of a decoder output corresponds to a value of either $2^1$ or $-2^1$ depending on the sign of the corresponding product ($E_i \cdot \text{sign}$ on the figure).

**Step 3**: The PE generates the equivalent of a histogram of the decoder output values. Specifically, the PE accumulates the 16 32-bit numbers from Step 2 into 32 buckets, $N_0,...,N_{31}$, corresponding to the values of $2^0,2^1,...,2^{31}$ as there are 32 powers of two. The signs of these numbers $E_i \cdot \text{sign}$ from Step 1 are also taken into account. At the end of this step, each “bucket” contains the count of the number of inputs that had the corresponding value. Since each bucket has 16 signed inputs the resulting count would be in a value in $[-16,...,16]$ and thus is represented by 6 bits in 2’s complement.

**Step 4**: Naively reducing the 32 6-bit counts into the final output would require first “shifting” the counts according to their weight converting all to $31+6=37b$ and then using a 32-input adder tree as shown in Figure 4(b). Instead LAC reduces costs and energy by exploiting the relative weight of each count by grouping and concatenating them in this stage as shown in Figure 4(c). For example, rather than adding $N_0$ and $N_0$ we can simply concatenate them as they are guaranteed to have no overlapping bits that are “1”. This is explained in more detail in Section 4.2.1.

**Step 5**: As Section 4.2.1 explains in more detail, the concatenated values from Step 4.1 are added via a 6-input adder tree as shown in Figure 4(d) producing a 38b partial sum.

**Step 6**: The partial sum from the previous step is accumulated with the partial sum held in an accumulator. This way, the complete $A \times W$ product can be calculated over multiple cycles, one effectual pair of one-offsets per cycle.

The aforementioned steps are not meant to be interpreted as pipeline stages. They can be merged or split as desired.

#### 4.2.1 Enhanced Adder Tree

Step 5 of Figure 4(b) has to add 32 6b counts each weights by the corresponding power of 2. This section presents an alternate design that replaces Steps 4 and 5. Specifically, it presents an equivalent more area and energy efficient “adder tree” which takes advantage of the fact that the outputs of Step 4 contain groups of numbers that have no overlapping bits that are “1”. For example, in relation to the naïve adder tree of Figure 4(a) consider adding the $6^h$ 6-bit input $(N^6_0,...,N^6_{15})$ with the $0^h$ 6-bit input $(N^0_0,...,N^0_{15})$. We have to first shift $N^6_0$ by 6 bits which amounts to adding 6 zeros as the 6 least significant bits of the result. In this case, there will be no bit position in which both $N^6_0\neq 6$ and $N^0_0=0$ will have a bit that is 1. Accordingly, adding $(N^6\preceq 6)$ and $N^0_0$ is equivalent to concatenating either $N^6_0$ and $N^0_0$ or $(N^6_0\preceq 1)$ and $N^0_0$ based on the sign bit of $N^0_0$ (Figure 5):

$$N^6_0 \times 2^6 + N^0_0 = (N^6_0 = <6) + N^0_0$$

1) if $s^6_0$ is zero:

$$= n^6_000000000000000000000000000000$$

2) else if $s^6_0$ is one:

$$= (n^6_0 + 1)(n^6_0 + 1)(n^6_1 + 1)(n^6_1 + 1)(n^6_1 + 1)(n^6_1 + 1) + n^6_000000000000000000000000$$

$$= \{(n^6_1 = 1), N^0_0\}$$

(4)

Accordingly, this process can be applied recursively, by grouping those $N^0_0$ where $(i \bmod 6) = 0$ is equal. That is the $i^{th}$ input would be concatenated with $(i + 6)^{th}$, $(i + 12)^{th}$, and so on. Figure 5 shows an example unit for those $N^0_0$ inputs where $(i \bmod 6) = 0$. While the figure shows the concatenation done as stack, other arrangements are possible.

For the 16 product unit described here the above process yields the following six groups:

$$G_0 = \{N^{30,34,N^{18}}, N^{12}, N^6, N^0\}$$

$$G_1 = \{N^{33}, N^{35}, N^{19}, N^{13}, N^7, N^1\}$$

$$G_2 = \{N^{26}, N^{20}, N^{14}, N^8, N^2\}$$

$$G_3 = \{N^{22}, N^{23}, N^{15}, N^7, N^1\}$$

$$G_4 = \{N^{28}, N^{22}, N^{16}, N^{10}, N^4\}$$

$$G_5 = \{N^{29}, N^{23}, N^{17}, N^{11}, N^5\}$$

(5)

The final partial sum is then given by the following:

$$psum = \sum_{i=0}^{5} (G_i = <i)$$

(6)
4.3 Tile Organization

Figure 6 illustrates LAC tile which comprises a 2D array of PEs processing 16 windows of input activations and \( K = 8 \) filters every cycle. PEs along the same column share the same input activations and PEs along the same row receive the same weights. Every cycle PE\((i,j)\) receives the next one-offset from each input activation from the \( j^{th} \) window and multiplies it by a one-offset of the corresponding weight from the \( j^{th} \) filter. The tile starts processing the next set of activations and weights when all the PEs are finished with processing the terms of the current set of 16 activations and their corresponding weights.

Since LAC processes both activations and weights term-serially, to match our BASE configuration it requires to process more filters or more windows concurrently. Here we consider implementations that process more filters. In the worst case each activation and weight possesses 16 terms, thus LAC tile should process \( 8 \times 16 = 128 \) filters in parallel to always match the peak compute bandwidth of BASE. However, as shown in Figure 1 with \( 16 \times \) more filters, LAC’s potential performance improvement over the baseline is more than two orders of magnitude. Thus, we can trade-off some of this potential by using fewer filters.

To read weights from the WM BASE requires 16 wires per weight while LAC requires only one wire per weight as it process weights term-serially. Thus, with the same number of filters LAC requires \( 16 \times \) less wires. In this study we limit our attention to a BASE configuration with 8 filters, 16 weights per filter, and thus 2K weight wires (BASE\(_{2K}\)), and to LAC configurations with 8, 16, 32, and 64 filters, and 128, 256, 512, and 1K weight wires. In all designs, the number of activation wires is set to 256 (Figure 7). Alternatively, we could fix the number of filters and accordingly number of weight wires and add more parallelism to the design by increasing the number of activation windows. The evaluation of such a design is not reported in this document.

5. EVALUATION

This section evaluates LAC’s performance, energy and area and explores different configurations of LAC comparing to BASE\(_{2K}\). This section considers LAC\(_{128}\), LAC\(_{256}\), LAC\(_{512}\), and LAC\(_{1K}\) configurations which require 128, 256, 512, and 1K weight wires, respectively (Figure 7).

5.1 Methodology

Execution time is modeled via a custom cycle-accurate simulator and energy and area results are reported based on post layout simulations of the designs. Synopsys Design Compiler \(^8\) was used to synthesize the designs with TSMC 65nm library. Layouts were produced with Cadence Innovus \(^9\) using synthesis results. Intel PSG ModelSim is used to generate data-driven activity factors to report the power numbers. The clock frequency of all designs is set to 1GHz. The ABin and ABout SRAM buffers were modeled with CACTI \(^10\) and AM and WM were modeled as eDRAM with Destiny \(^11\).

5.2 Performance

Figure 8 shows the performance of LAC configurations relative to BASE\(_{2K}\) for convolutional layers with the 100% relative TOP-1 accuracy precision profiles of Table 1. LAC targets both dense and sparse networks and improves the performance by processing only the essential terms; however, the sparse networks would benefit more as they posses more ineffectual terms. On average, LAC\(_{128}\) outperforms BASE\(_{2K}\) by more than \( 2 \times \) while for AlexNet-Sparse LAC\(_{128}\) achieves a speedup of \( 3 \times \) over the baseline. Figure 8 shows how average performance on convolutional layers over all networks scales for different configurations.
Table 1: Activation and weight precision profiles in bits for the convolutional layers.

| Network             | Convolutional Layers | 100% Accuracy |
|---------------------|----------------------|---------------|
|                     | Activation Precision Per Layer | Weight Precision Per Network |
| AlexNet             | 9-8-5-5/-            | 11            |
| GoogLeNet           | 10-8-10-9-8-10-9-8-9-10/- | 11            |
| VGG                | /-8-9/-9            | 12            |
| VGGM               | /-/-/8/-            | 12            |
| AlexNet-Sparse [12] | 8-9-9-9-8           | 7             |
| ResNet50-Sparse [13] | 10-8-6-6-5-7-6-6-7-6-7-6-8-7-6-8-5-8 | 13            |

![Graph showing LAC performance relative to BASE2K](image)

Figure 8: Laconic performance relative to BASE2K

Table 2: Laconic energy efficiency relative to BASE2K.

| Network    | LAC128 | LAC256 | LAC512 | LAC1K |
|------------|--------|--------|--------|-------|
| AlexNet    | 2.03   | 2.44   | 2.92   | 1.88  |
| GoogLeNet  | 1.84   | 2.32   | 2.76   | 1.75  |
| VGG_S      | 2.43   | 3.04   | 3.63   | 2.31  |
| VGG_M      | 2.18   | 2.73   | 3.26   | 2.02  |
| AlexNet-Sparse | 2.81   | 2.91   | 3.49   | 2.19  |
| ResNet50-Sparse | 1.09   | 2.02   | 2.41   | 1.61  |
| Geomean    | 2.13   | 2.35   | 3.05   | 1.95  |

with different number of weight wires. LAC256, LAC512, and LAC1K achieve speedups of 4.0×, 8.1×, and 15.4× over BASE2K, respectively.

5.3 Energy Efficiency

Table 2 summarizes the energy efficiency of various LAC configurations over BASE2K. On average over all networks LAC128, LAC256, LAC512, and LAC1K are 2.13×, 2.55×, 3.05×, and 1.95× more energy efficient than BASE2K.

5.4 Area

Post layout measurements were used to measure the area of BASE and LAC. The LAC128, LAC256, and LAC512 configurations require 0.75×, 0.82×, and 0.96× less area than BASE2K, respectively while outperforming BASE2K by 2.3×, 4.0×, and 8.1×. The area overhead for LAC1K is 1.36× while its execution time improvement over the baseline is 15.4×. Thus LAC exhibits better performance vs. area scaling than BASE.

5.5 Scalability

Thus far we considered designs with up to 1K wire weight memory connections. For one of the most recent network studied here, GoogleNet we also experimented with 2K and 4K wire configurations. Their relative performance improvements were 20.4× and 27.0×. Similarly to other accelerators performance improves sublinearly. This is primarily due to inter-filter imbalance which is aggravated as in these experiments we considered only increasing the number of filters when scaling up. Alternate designs may consider increasing the number of simultaneously processed activations instead. In such configurations, minimal buffering across activation columns as in Pragmatic [6] can also combat cross-activation imbalance which we expect will worsen as we increase the number of concurrently processed activations.

6. CONCLUSION

We have shown that compared to conventional bit-parallel processing, aiming to process only the non-zero bits (or terms in a booth-encoded format) of the activations and weights has the potential to reduce work and thus improve performance by two orders of magnitude. We presented the first practical design, Laconic that takes advantage of this approach leading to best-of-class performance improvements. Laconic is naturally compatible with the compression approach of Delmas et al. [14] and thus as per their study we expect to perform well with practical off-chip memory configurations and interfaces.

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