Fast Successive-Cancellation List Flip Decoding of Polar Codes

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ABSTRACT This work presents a fast successive-cancellation list flip (Fast-SCLF) decoding algorithm for polar codes that addresses the high latency issue associated with the successive-cancellation list flip (SCLF) decoding algorithm. We first propose a bit-flipping strategy tailored to the state-of-the-art fast successive-cancellation list (FSCL) decoding that avoids tree-traversal in the binary tree representation of SCLF, thus reducing the latency of the decoding process. We then derive a parameterized path selection error model to accurately estimate the bit index at which the correct decoding path is eliminated from the initial FSCL decoding. The trainable parameter is optimized online based on an efficient supervised learning framework. Simulation results show that for a polar code of length 512 with 256 information bits, with similar error-correction performance and memory consumption, the proposed Fast-SCLF decoder reduces up to 73.4% of the average decoding latency of the SCLF decoder with the same list size at the frame error rate of $10^{-4}$, while incurring a maximum computational complexity overhead of 27.6%. For the same polar code of length 512 with 256 information bits and at practical signal-to-noise ratios, the proposed decoder with list size 4 reduces 89.3% and 43.7% of the average complexity and decoding latency of the FSCL decoder with list size 32 (FSCL-32), respectively, while also reducing 83.2% of the memory consumption of FSCL-32. The significant improvements of the proposed decoder come at the cost of 0.07 dB error-correction performance degradation compared with FSCL-32.

INDEX TERMS 5G, polar codes, list decoding, bit flipping, machine learning.

I. INTRODUCTION

POLAR codes are the first class of error-correcting codes that is proven to achieve the channel capacity of any binary symmetric channel under the low-complexity successive-cancellation (SC) decoding algorithm [1]. Recently, polar codes are selected for use in the enhanced mobile broadband (eMBB) control channel of the fifth generation of cellular communications (5G) standard, where codes with short to moderate block lengths are used [2]. The error-correction performance of short to moderate-length polar codes under SC decoding does not satisfy the requirements of the 5G standard. SC list (SCL) decoding was introduced in [3]–[5] to improve the error-correction performance of SC decoding by keeping a list of candidate message words at each decoding step. In addition, it was observed that under SCL decoding, the error-correction performance is significantly improved when the polar code is concatenated with a cyclic redundancy check (CRC) [3], [4]. Furthermore, SC-based decoding of polar code can be represented as a binary tree traversing problem [6] and it was shown that the decoders in [1], [3]–[5] experience a high decoding latency as they require a full binary tree traversal. Several fast decoding techniques were introduced to improve the decoding latency of the conventional SC and SCL decoding algorithms [7]–[11]. In particular, the decoding operations of special constituent codes under the fast SCL (FSCL) decoding algorithms proposed in [8]–[11] can be carried out at the parent node level, thus reducing the decoding latency caused by the tree traversal.

As the memory requirement of SCL decoding grows linearly with the list size [12], it is of great interest to improve the decoding performance of SCL decoding with a small list size. To address this issue, various bit-flipping algorithms of the SC-based decoders were proposed to significantly improve the error-correction performance of SC and SCL decoding with the same list size [13]–[23]. In [19], given that the initial SCL decoding attempt does not satisfy the CRC verification, the authors proposed an algorithm that
flips the first erroneous bit of the best decoding path in the next decoding attempt and the error position is estimated using a correlation matrix. The SCL-Flip (SCLF) decoder proposed in [20] estimates the bit index at which the correct path is discarded from the initial SCL decoding, then in the next decoding attempt all the paths that were discarded at the estimated error position are selected to continue the decoding. It was observed that the decoder in [20] provides a better error-correction performance when compared with the decoder proposed in [19]. In [21], an improved SCLF decoding algorithm is proposed which addresses the high-order errors of SCL decoding. By utilizing a complex path selection error model and with the same number of additional decoding attempts, the decoder in [21] provides a slight error-correction performance improvement when compared with the SCL decoder [20]. It is worth to note that all the bit-flipping algorithms of SCL decoding introduced in [19]–[22] suffer from a variable decoding latency, which is caused by the sequential nature of the bit-flipping operations. In addition, all the decoders in [19]–[22] fully traverse the polar code decoding tree as required by SCL decoding, thus resulting in a high decoding latency. The authors in [23] proposed a simplified node-based bit-flipping algorithm to improve the decoding latency of SCLF decoding, which is referred as SSCLF decoding in this paper. Specifically, a low-complexity bit-flipping metric based on the path metrics is utilized in [23] to select the first error position of FSCL decoding. However, when applied to an FSCL decoder with the list sizes of 2 and 4, the simplified path-selection scheme of [23] results in a significant FER performance degradation when compared with SCLF decoding [20].

In this paper, a fast SCLF (Fast-SCLF) decoding algorithm is proposed to tackle the underlying high-decoding latency of the SCLF decoder [20]. In particular, a bit-flipping strategy tailored to FSCL decoding of polar codes is first introduced. Then, a path selection error metric is derived for the proposed bit-flipping strategy. The proposed path selection error metric utilizes a trainable parameter to improve the estimation accuracy of the error position, which is optimized online using an efficient supervised learning framework. By utilizing online training, the proposed path selection error-model does not require the parameter to be optimized offline at various signal-to-noise ratios (SNRs). Instead, the parameter is automatically optimized at the operating SNR of the decoder, which obviates the need for pilot signals. Our simulation results illustrate that for a polar code of length 512 with 256 information bits at the frame error rate (FER) of $10^{-4}$, with similar error-correction performance and memory consumption, the proposed Fast-SCLF decoder reduces up to 73.4% of the average decoding latency of the SCLF decoder with the same list size, while incurring a maximum computational overhead of 27.6%. For the same polar code of length 512 with 256 information bits and at practical SNR values, the proposed decoder with list size 4 reduces 89.3% and 43.7% of the average complexity and decoding latency of FSCL-32, respectively, while also reducing 83.2% of the memory consumption of FSCL-32. Note that the significant complexity reductions only come at the cost of less than 0.07 dB error-correction performance degradation. For the same polar code of length 512 with 256 information bits, when compared with the SSCLF decoder with list size 4 at the target FER of $10^{-4}$, an FER performance gain of 0.2 dB is obtained for the proposed Fast-SCLF decoder at the cost of 8.3% computational complexity overheads, while the average decoding latency and memory consumption of the Fast-SCLF decoder are relatively similar to those of the SSCLF decoder.

The remainder of this paper is organized as follows. Section II provides the background on polar codes and their decoding algorithms. Section III proposes the Fast-SCLF decoding algorithm. Simulation results are reported in Section IV followed by concluding remarks drawn in Section V.

II. PRELIMINARIES

We start this section by first introducing notations. Throughout this paper boldface letters indicate vectors and matrices, while unless otherwise specified non-boldface letters indicate either binary, integer or real numbers. In addition, by $a_{i_{\text{max}}}^{i_{\text{min}}} = \{a_{i_{\text{min}}}, \ldots, a_{i_{\text{max}}}\}$ we denote a vector of size $i_{\text{max}} - i_{\text{min}} + 1$ containing the $a$ elements from index $i_{\text{min}}$ to $i_{\text{max}}$ (i.e., $i_{\text{min}} < i_{\text{max}}$). Sets are denoted by blackboard bold letters, e.g., $\mathbb{R}$ is the set containing real numbers. Finally, $I_{X}$ is an indicator function where $I_{X} = 1$ if the condition $X$ is true, and $I_{X} = 0$ otherwise.

A. POLAR ENCODING

A polar code $\mathcal{P}(N,K)$ of length $N$ with $K$ information bits is constructed by applying a linear transformation to the binary message word $u = \{u_{1}, \ldots, u_{N}\}$ as $x = uG^\otimes n$ where $x = \{x_{1}, \ldots, x_{N}\}$ is the codeword, $G^\otimes m$ is the $m$-th Kronecker power of the polarizing matrix $G = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$, and $n = \log_{2}N$. The vector $u$ contains a set $\mathbb{I}$ of $K$ information bit indices and a set $\mathbb{I}^{c}$ of $N - K$ frozen bit indices, with $\mathbb{I}$ and $\mathbb{I}^{c}$ are known to the encoder and the decoder. The values of all the frozen bits are set to 0, while the values of the information bits are independent and identically distributed (i.i.d.). The codeword $x$ is then modulated and sent through the channel. In this paper, binary phase-shift keying (BPSK) modulation and additive white Gaussian noise (AWGN) channel model are considered. Therefore, the soft vector of the transmitted codeword received by the decoder is given as $y = (1 - 2x) + z$, where $1$ is an all-one vector of size $N$, and $z$ is a Gaussian noise vector of size $N$ with variance $\sigma^2$ and zero mean. In the log-likelihood ratio (LLR) domain, the LLR vector of the transmitted codeword is given as $\alpha_n = \ln \left( \frac{P[r=x=0|y]}{P[r=x=1|y]} \right) = \frac{2y}{\sigma^2}$.

B. SUCCESSIVE-CANCELLATION AND SUCCESSIVE-CANCELLATION LIST DECODING

An example of a factor-graph representation for $\mathcal{P}(16,8)$ is depicted in Fig. I(a) with the frozen set $\mathbb{I}^{c} = \{1, 2, 3, 4, 5, 9, 10, 11\}$. To obtain the message word under SC decoding, the soft LLR values and the hard bit estimations
are propagated through all the processing elements (PEs), which are depicted in Fig. 1(b). The PE in Fig. 1(b) performs the computations:

\[ \alpha_{s,i}, \beta_{s,i} = f(\alpha_{s,i+1}, \beta_{s,i+1}) \]

and

\[ \alpha_{s,i+2}, \beta_{s,i+2} = g(\alpha_{s,i+1}, \beta_{s,i+1}) \]

where \( f(\cdot) \) and \( g(\cdot) \) are the soft LLR value and the hard-bit estimation at the \( s \)-th stage and the \( i \)-th bit, respectively, and the minimum approximation formulations of \( f \) and \( g \) are

\[ f(a, b) = \min(\alpha_i, \beta_i) \text{sgn}(a) \text{sgn}(b), \]

and

\[ g(a, b, c) = b + (1 - 2c)a. \]

The soft LLR values at the \( n \)-th stage are initialized to \( \alpha_0 \) and the hard-bit estimation of an information bit at the 0-th stage is obtained as

\[ \hat{u}_i = \beta_{0,i} = \frac{1 - \text{sgn}(\alpha_{0,i})}{2}, \quad \forall i \in \mathbb{I}. \]

Given

\[ \beta_{s,i}, \beta_{s,i+1}, \text{ and } \beta_{s,i+1,2} \]

are then computed as

\[ \beta_{s,i+1} = \beta_{s,i}\beta_{s,i+2}, \quad \text{and} \quad \beta_{s,i+1,2} = \beta_{s,i,2}. \]

SCL decoding was introduced to significantly improve the error-correction performance of SC decoding [3]–[5]. Under SCL decoding, the estimation of an information bit \( \hat{u}_i \) at the \( (s+1) \)-th stage is obtained as

\[ \hat{u}_i = \beta_{0,i} = \frac{1 - \text{sgn}(\alpha_{0,i})}{2}, \quad \forall i \in \mathbb{I}. \]

Given

\[ \beta_{s,i}, \beta_{s,i+1}, \beta_{s,i+1,2}, \quad \text{and} \quad \beta_{s,i+1,2} \]

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\[ \beta_{s,i+1} = \beta_{s,i}\beta_{s,i+2}, \quad \text{and} \quad \beta_{s,i+1,2} = \beta_{s,i,2}. \]
algorithm \[9\]. The definitions and decoding operations of each special node under FSCL decoding are given as follows.

1) Rate-0 node
All the leaf nodes of a Rate-0 node are frozen bits. Therefore, all the hard values associated with the parent node are set to 0 and the path metric of the \( l \)-th path is given as \[9\]

\[
PM_l = PM_t + \sum_{i=\text{min}_v}^{\text{max}_v} |\alpha_{s,i}| - \alpha_{s,i} \frac{2}{i_{\text{max}_v}}. \tag{3}
\]

2) REP node
All the leaf nodes of a REP node are frozen bits, except for \( \beta_{0,\text{min}_v} \). The path metric of the \( l \)-th decoding path is calculated as \[9\]

\[
PM_l = PM_t + \sum_{i=\text{min}_v}^{\text{max}_v} |\alpha_{s,i}| - (1 - 2\beta_{s,i}) \alpha_{s,i} \frac{2}{i_{\text{max}_v}}, \tag{4}
\]

where \( \beta_{s,i} \) denotes the bit estimate of the information bit of the REP node.

3) Rate-1 node
All the leaf nodes of a Rate-1 node are information bits. FSCL decoding performs \( \tau \) path splittings, where \( \tau = \min(L - 1, N_v) \) \[9\]. The path metric of the \( l \)-th decoding path for a Rate-1 node is calculated as \[9\]

\[
PM_l = PM_t + \sum_{i=\text{min}_v}^{\text{max}_v} |\alpha_{s,i}| - (1 - 2\beta_{s,i}) \alpha_{s,i} \frac{2}{i_{\text{max}_v}}, \tag{5}
\]

where \( \beta_{s,i} \) denotes the bit estimate of the \( i \)-th bit of \( v \).

4) SPC node
All the leaf nodes of an SPC node are information bits, except for \( \beta_{0,\text{min}_v} \). The parity check sum of the \( l \)-th path is first obtained as \[9\]

\[
\hat{p}_l = \bigoplus_{i=\text{min}_v}^{\text{min}\nu_{l}} 1 - \frac{1}{2} \text{sgn}(\alpha_{s,i}). \tag{6}
\]

The path metric is then updated as \[9\]

\[
PM_l = PM_t + \hat{p}_l |\alpha_{s,i*_{\text{min}_v}}|. \tag{7}
\]

The decoding continues with \( \tau \) path splittings, where \( \tau = \min(L - 1, N_v - 1) \) \[9\]. In each new path splitting at the \( i \)-th index, the path metric is updated as \[9\]

\[
PM_l = \begin{cases} 
PM_t + |\alpha_{s,i}| + (1 - 2\hat{p}_l) |\alpha_{s,i*_{\text{min}_v}}| & \text{if } 1 - 2\beta_{s,i} \neq \text{sgn}(\alpha_{s,i}), \\
PM_t & \text{otherwise,}
\end{cases} \tag{8}
\]

then the parity check sum is updated as \[10\]

\[
\hat{p}_l = \begin{cases} 
1 & \text{if } 1 - 2\beta_{s,i} \neq \text{sgn}(\alpha_{s,i}), \\
\hat{p}_l & \text{otherwise.}
\end{cases} \tag{9}
\]

where \( i \) is selected by following the bit indices of the sorted absolute LLR values in \[9\]. When all the bits are estimated, the hard decision of the least reliable bit is updated to maintain the parity check condition of the SPC node \[9\]

\[
\beta_{s,i*_{\text{min}_v}} = \bigoplus_{i=\text{min}_v}^{\text{min}\nu_{l}} \beta_{s,i}. \tag{10}
\]

The memory requirements of SCL and FSCL decoding algorithms with list size \( L \) in terms of the number of memory bits are given as \[5\], \[9\]

\[
M_{\text{SCL}} = M_{\text{FSCL}} = N(L + 1)b_f + 2LN. \tag{11}
\]

where \( b_f \) is the number of bits used to quantize a floating-point number.

D. SUCCESSIVE-CANCELLATION FLIP AND DYNAMIC SUCCESSIVE-CANCELLATION FLIP DECODING
SC-Flip (SCF) decoding algorithm was proposed in \[13\] to improve the error-correction performance of SC decoding for short to moderate block lengths. Specifically, if the estimated message word \( \hat{u} \) does not satisfy the CRC test after the initial SC decoding attempt, an additional SC decoding attempt is made by flipping the estimation of an information bit in \( \hat{u} \) that is most likely to be the first error bit. In the rest of this paper, as we only need to locate the error decision occurred when an information bit is decoded under SC-based decoding, the bit indices are referred to as information bits and are indexed from 1 to \( K + C \). In \[13\], the most erroneous position is estimated as \( \tau = \arg \min_{1 \leq \tau \leq K + C} |\alpha_{0,\tau}|. \)

A problem associated with SCF decoding is its poor estimation accuracy of the actual error position \[14\]. To address this issue, the authors in \[14\] propose the Dynamic SC-Flip (DSCF) decoding algorithm that utilizes a conditional probability model to accurately estimate the error position, which is given as \( \tau = \arg \min_{1 \leq \tau \leq K + C} Q_\tau \), where \( Q_\tau \) is the error metric of the \( \tau \)-th information bit under SC decoding:

\[
Q_\tau = |\alpha_{0,\tau}| + \sum_{1 \leq j \leq L} \lambda \ln[1 + \exp(-\lambda|\alpha_{0,j}|)]. \tag{12}
\]

The parameter \( \lambda \in \mathbb{R}^+ \) is a perturbation parameter that is optimized offline \[14\]. In \[10\]–\[18\], fast decoding schemes are proposed to reduce the decoding latency of SCF and DSCF decoding. However, it was observed in \[14\], \[15\] that the maximum number of decoding attempts required by the DSCF-based decoders to obtain a comparable FER performance of SCL decoding with list size 16 is significantly large. This problem prevents the DSCF-based decoders to be practical for applications with a stringent worst-case latency.
E. SUCCESSIVE-CANCELLATION LIST FLIP DECODING

SCLF decoding also relies on a CRC verification to indicate whether the initial SCL decoding attempt is successful or not. If the first SCL decoding attempt does not satisfy the CRC verification, the SCLF decoding algorithm tries to identify the first information bit index \( i \), at which the correct path is discarded from the list of the \( L \) most probable decoding paths \[20\]. Given that the \( i \)-th bit index is correctly identified, in the next decoding attempt and after the path splitting occurred at the \( i \)-th bit index, the erroneous path selection is reversed where the \( L \) decoding paths that have the highest (worst) path metrics are selected to continue the decoding \[20\]. This reversed path selection scheme recovers the correct decoding path, which was discarded at the initial SCL decoding at the \( i \)-th bit index, to the list of the active decoding paths. SCLF decoding then performs conventional SCL decoding operations for all the bit indices following \( i \).

Given that at the \( i \)-th information bit under SCL decoding, there are \( L \) active decoding paths denoted as \( l \), \( l \in \{1, 2L\} \). After the path splitting of the current \( L \) active paths, the path metrics of the new \( 2L \) paths are computed and sorted. Let \( l' \) be the index of a discarded decoding path after the path metric sorting, i.e., the path metric corresponding to \( l' \) is among the \( L \) largest path metric values. The probability that the path with index \( l' \) is the correct decoding path is \[14\]

\[
Pr(\hat{u}^{l'}_{j_{i'}} = u^{l'}_{i} | \alpha_n) = \prod_{1 \leq j < i' \atop \forall j \in \mathcal{A}'_{l'}} Pr(\hat{u}_{j_{i'}} = u_{j} | \alpha_n, \hat{u}^{j_{i'}}_{l'\lambda} = u^{j_{i'}}_{1}),
\]

\[
\times \prod_{1 \leq j < i \atop \forall j \in \mathcal{A}'_{l'}} \left[1 - Pr(\hat{u}_{j_{i'}} = u_{j} | \alpha_n, \hat{u}^{j_{i'}}_{l'\lambda} = u^{j_{i'}}_{1})\right],
\]

(13)

where \( Pr(\hat{u}^{l'}_{j_{i'}} = u^{l'}_{i} | \alpha_n) = Pr(\hat{u}_{1_{l'}} = u_1, \ldots, \hat{u}_{i-1_{l'}} = u_{i-1,\lambda_1}) \). \( \mathcal{A}'_{l'} \) is the set of information bit indices where their hard decisions follow the sign of the corresponding LLR values, while \( \mathcal{A}'_{l'} \) is the set of information bit indices whose hard decisions do not follow the sign of the LLR values \[20\].

Note that \( Pr(\hat{u}_{j_{i'}} = u_{j} | \alpha_n, \hat{u}^{j_{i'}}_{l'\lambda} = u^{j_{i'}}_{1}) \) is not available during the course of decoding as \( u \) is unknown, thus it is approximated as \[14, 20\]

\[
Pr(\hat{u}_{j_{i'}} = u_{j} | \alpha_n, \hat{u}^{j_{i'}}_{l'\lambda} = u^{j_{i'}}_{1}) \approx \frac{1}{1 + \exp(-\lambda |\alpha_{0,j_{i'}}|)},
\]

(14)

where \( \lambda \in \mathbb{R}^+ \) is a perturbation parameter that is optimized offline to improve the approximation accuracy of \[14\]. The flipping metric \( Q_i \) under the approximation provided in \[18\] is then given as \[15, 20\]

\[
Q_i \approx \min_{\forall l'} \left[ \sum_{\forall j \in \mathcal{A}'_{l'}} |\alpha_{0,j_{i'}}| - \theta + \sum_{1 \leq j \leq i} \text{ReLU} \left( \theta - |\alpha_{0,j_{i'}}| \right) \right],
\]

(19)

where \( \text{ReLU}(a) = a \) if \( a > 0 \) and \( \text{ReLU}(a) = 0 \) otherwise. The most probable information bit index where the correct path is discarded is then estimated as \( i = \arg\max_{\log_2 L < i \leq K+C} P_i \). \[20\].

In this paper, we implement the hardware-friendly SCLF decoder using \[19\] as it only requires the optimization of \( \theta \).

Unlike DSCF decoding, SCLF decoding can achieve the FER performance of SCL decoding with a large list size using a reasonable number of maximum decoding attempts \[20\]. A critical problem associated with SCLF decoding is that it fully traverses the polar binary tree as required by SCL decoding, which results in a high decoding latency. The SSCLF decoder was proposed in \[23\] to improve the decoding latency of SCLF decoding by introducing a reversed path selection scheme to FSCL decoding. However, the proposed scheme in \[23\] is only applied to the decoding steps that perform path splitting and path metric sorting, thus it does not apply to the decoding steps that occur after the \( \tau \) path-splittings for the SPC and Rate-1 nodes. As a consequent, SSCLF decoding with a small list size (\( L \in \{2, 4\} \)) incurs a significant FER performance degradation when compared to SCLF decoding with the same list size.
III. FAST SUCCESSIVE-CANCELLATION LIST FLIP DECODING

A. BIT-FLIPPING SCHEME FOR FSCL DECODING

We first introduce the bit-flipping scheme tailored to FSCL decoding by illustrating the proposed scheme under various examples. We consider the case where an all-zero codeword of $\mathcal{P}(16, 8)$ is transmitted through the channel, whose binary tree representation is depicted in Fig. 2(a). Similar to SCL-based decoding, under FSCL-based decoding, we denote by $l$ the path index corresponding to the current $L$ active decoding paths, while $\bar{l}$ is used to indicate the indices of the paths that are forked from $l$. Finally, $l'$ indicates the path indices of the decoding paths that are discarded due to their high path metric values. Note that $l, \bar{l}, l' \in [1, 2L]$.

1) Bit-Flipping Scheme for SPC Nodes

Table 1 shows an example of FSCL decoding when applied to the SPC node of $\mathcal{P}(16, 8)$ with $L = 4$. The decoding order is first determined by sorting the magnitude of the LLR values associated with the SPC node in the increasing order.

In this example, the following decoding order is considered: $\{\beta_{2,8_1}, \beta_{2,5}, \beta_{2,7_1}, \beta_{2,6_2}\}$. Thus, $\beta_{2,8}$ is selected as the parity bit of the SPC node for all the active decoding paths. The path splittings at $\beta_{2,6_1}$ are considered in this example, and the paths with indices $l \in \{5, 6, 7, 8\}$ are forked from the paths with indices $l \in \{1, 2, 3, 4\}$ at $\beta_{2,6_2}$, respectively, followed by the path metric sorting operations. The most likely decoding paths with indices $l \in \{1, 2, 3, 4\}$ are then selected to continue the decoding, while the paths with indices $l' \in \{5, 6, 7, 8\}$ are discarded as illustrated in Table 1.

At this stage, the parity bit $\beta_{2,8}$ of the SPC node is not yet decoded. As an all-zero codeword is considered, the correct decoding path is $l' = 5$, which is discarded after $\beta_{2,6_1}$ is decoded, i.e., after the third path-splitting index. Given that this erroneous decision in the initial FSCL decoding is detected by a CRC verification, this erroneous path selection is reversed in the next decoding attempt by swapping the path indices of $l'$ and $l$ after the path splittings at $\beta_{2,6_1}$ for all the decoding paths. The decoding continues by setting the values of the parity bit $\beta_{2,8}$ with respect to (10) to maintain the parity constraint for all the corrected paths. Similar to the bit-flipping schemes introduced in [17], [23], in the proposed scheme, the bit-flipping operation is not applicable to the parity bits of the SPC nodes. This is due to the fact that the parity bits are determined after the all the other bits are calculated to ensure the parity check is satisfied. Therefore, if all the other bits of the SPC node are correctly decoded, the parity bit of this decoding path is also correctly decoded. As a result, the proposed algorithm only considers a maximum of $N_v - 1$ possibilities to identify a bit flip that occurs in an SPC node. This is significantly smaller than the maximum search space of size $\binom{N_v}{2}$ required to flip a pair of bits to maintain the parity check constraint, especially as $N_v$ increases [19].

Note that in this example, the minimum number of path splittings required by the SPC node to preserve the SCL decoding performance is $\tau = \min\{L - 1, N_v - 1\} = \min\{3, 3\} = 3$, where $\nu$ indicates the SPC node of size 4. Under the proposed bit-flipping scheme for SPC nodes, if a decision error occurs at the path-splitting index after the minimum number of $\tau$ path splittings are obtained, in the next decoding attempt, the hard values at the estimated error index are flipped for all the active paths. The path metrics PM of the surviving paths are then updated by following (8), using the LLR value corresponding to the flipped position and the current parity checksum $\nu$.

2) Bit-Flipping Scheme for REP Nodes

Since the soft and hard estimate of the information bit associated with a REP node can be directly obtained at the parent node level under FSCL decoding, the path splitting operation under FSCL decoding applied to the information bit of a REP node is similar to that of SCL decoding when applied to an information bit at the leaf node level. Therefore, in this paper, the reversed path selection scheme used in SCLF decoding is directly applied to the information bit associated with a REP node or to an information bit at the leaf-node level under FSCL decoding [17], [23].

3) Bit-Flipping Scheme for Rate-1 Nodes

Table 2 shows an example of FSCL decoding on the Rate-1 node of $\mathcal{P}(16, 8)$ at the fifth path-splitting index with $L = 2$. In Table 2 the hard estimates of the discarded paths with indices $l' \in \{2, 4\}$ are indicated, while the hard estimates of the surviving paths with indices $l' \in \{1, 3\}$ are omitted. It can be observed that the decoding path with index $l' = 2$ is the correct path as all the estimated bits are 0, which is discarded after bit $\beta_{2,13_2}$ is decoded. Therefore, in the next decoding attempt, the decoding paths with indices $l' \in \{2, 4\}$ will be selected to continue the decoding instead of the paths with indices $l' \in \{1, 3\}$ [17], [23]. Similar to the case of SPC nodes, after $\tau$ path splittings, if the hard decision of a bit of the Rate-1 node results in the elimination of the correct path, this erroneous decision is reversed in the next FSCL decoding attempt by flipping the hard estimates of all the active paths at that erroneous index. The path metrics of the active paths are then added with the corresponding absolute LLR values of the flipping indices. In this example, the minimum number of path splittings is $\tau = \min\{L - 1, N_v\} = \min\{1, 4\} = 1$, which is obtained at the fifth path-splitting index. Therefore, under FSCL decoding, the hard values of all the active
decoding paths following the fifth path-splitting index are set to follow the signs of their LLR values. Similar to SCLF decoding, the proposed scheme only aims at correcting the first erroneous decision in the initial FSCL decoding attempt. Fig. 3 shows the ideal FER of the proposed bit-flipping scheme where the first erroneous path selection is always accurately corrected. In Fig. 3, we use the 5G polar codes $\mathcal{P}(512, 256)$ and $\mathcal{P}(512, 384)$ concatenated with a 24-bit CRC. Note that the positions of the first erroneous decoding decision can be obtained by comparing the discarded paths with the correct path after each path splitting. The FER performance of the ideal SCLF [20] and SSCLF [23] decoders and the FSCL decoder with list size 32 is also plotted for comparison. In Fig. 3, the ideal SCLF, SSCLF, and Fast-SCLF decoders with list size $L$ are denoted as I-SCLF-$L$, I-SSCLF-$L$ and I-Fast-SCLF-$L$, respectively, with $L \in \{2, 4, 8, 16, 32\}$.

As seen from Fig. 3, I-Fast-SCLF-$L$ obtains a slight FER performance gain over I-SCLF-$L$. In addition, as the reversed path-selection scheme of [23] is not applied to the decoding steps that occur after the minimum number of path-splittings is obtained for the Rate-1 and SPC nodes, this simplified bit-flipping scheme of [23] introduces FER performance degradation when compared with the ideal SCLF and Fast-SCLF decoders, especially when the list size is small, ($L \in \{2, 4\}$). For $L = 4$ and at the target FER of $10^{-4}$, the error-correction performance degradations of 0.2 dB and 0.3 dB are recorded for the ideal SSCLF decoder when compared to the ideal Fast-SCLF decoder for $\mathcal{P}(512, 256)$ and $\mathcal{P}(512, 384)$, respectively. Also note that the FER performance of the ideal SSCLF decoder with $L \in \{2, 4\}$ degrades quickly as the SNR increases.

We now explain the slight improvement in the error-correction performance of I-Fast-SCLF-$L$ over that of I-SCLF-$L$ as observed in Fig. 3. The error-correction performance of I-Fast-SCLF-$L$ and I-SCLF-$L$ are identical for REP nodes. Therefore, we empirically show that I-Fast-SCLF-$L$ outperforms I-SCLF-$L$ when applied to the same channel LLR vectors for Rate-1 and SPC nodes, where the LLR vectors contain an exact number of $c_e$ ($c_e > 0$) channel errors. A similar study was conducted in [24] for the case of fast SCF decoding.

We first consider the error event where only a single error is present in the LLR vector of the Rate-1 and SPC nodes ($c_e = 1$), which causes an unsuccessful CRC verification in the first FSCL and SCL decoding attempt. After the correct decoding path is recovered in the second FSCL decoding attempt of I-Fast-SCLF-$L$, FSCL decoding operations, e.g., path forking and path metric sorting, are applied to the $L$ recovered paths. Then, all the hard decisions of the correct path are set to follow the signs of the corresponding LLR values to maintain its path metric. Therefore, the path metric is equal to the absolute LLR value of the flipped bit. Recall that the FER values of the Rate-1 and SPC nodes are sorted in accordance with [2]. Thus, at the subsequent decoding steps after the flipped position, any new candidate path with at least a hard decision not following its corresponding LLR value will contain a higher path metric compared to that of the correct decoding path. Therefore, with $c_e = 1$, the correct decoding path is always found in the list of the best paths after the second FSCL decoding attempt of I-Fast-SCLF-$L$.

Note that a single error at the parent node level can translate into multiple errors at the leaf node level. This phenomenon is illustrated in Fig. 4 for an all-zero polar code of length $N = 64$, where the number of error bits at the leaf node level is provided with respect to the position of the single error bit at the parent node level. Consequently, there are cases that I-SCLF-$L$ has to perform the reserved path selection schemes multiple times to maintain the correct codeword in the list of the best paths, while I-Fast-SCLF-$L$ only requires a single reserved path selection. Thus with $c_e = 1$, the error correction performance of I-Fast-SCLF-$L$ is improved when compared to I-SCLF-$L$. As $c_e$ increases ($c_e > 2$), due to the complicated error patterns caused by multiple error bits, we expect that both I-Fast-SCLF-$L$ and I-SCLF-$L$ almost equally discard the correct path in the second decoding attempt, causing a wrong estimation of the transmitted codeword. Also note that when the channel reliability is improved at the high SNR regimes and given that $c_e > 0$, the performance gain of I-Fast-SCLF-$L$ over I-SCLF-$L$ is mainly obtained from the case of $c_e = 1$, as the LLR vectors are more likely to contain a single error than multiple ones ($c_e > 1$). On the other hand, at the low SNR regimes, it is more likely to have multiple errors at the parent node level, thus the error-correction performance gain of I-Fast-SCLF-$L$ is incremental when compared to that of I-SCLF-$L$. This phenomenon can also be observed from Fig. 5.

In Fig. 5b, we plot the FER curves of I-Fast-SCLF-32 and I-SCLF-32 for the polar codes of lengths 64 and 128 concatenated with a 16-bit CRC used in the 5G standard, the values of $K$ are selected to form the Rate-1 and SPC nodes, respectively. The simulations are carried out at $E_b/N_0 = 3$ dB and the FER values of the decoders in Fig. 5b are only obtained for the channel LLR vectors that contain exactly $c_e \in \{1, 2, 3, 4, 5, 6\}$ errors. It can be confirmed from Fig. 5b.

## Table 2: An example of FSCL decoding applied to a Rate-1 node of size 4 with $L = 2$, where the decoding is at the 6-th path splitting. $l' \in \{2, 4\}$ are the indices of the discarded paths.

| Node type | Path splitting index | $l' = 2$ | $l' = 4$ |
|-----------|----------------------|---------|---------|
| SPC       | $\beta_{2, 8_2} = 0$ | $\beta_{2, 8_4} = 0$ |         |
|           | $\beta_{2, 3_2} = 0$ | $\beta_{2, 3_4} = 0$ |         |
|           | $\beta_{2, 7_2} = 0$ | $\beta_{2, 7_4} = 0$ |         |
|           | $\beta_{2, 8_2} = 0$ | $\beta_{2, 8_4} = 0$ |         |
| REP       | $\beta_{0, 12_2} = 0$ | $\beta_{0, 12_4} = 0$ |         |
| Rate-1    | $\beta_{2, 13_2} = 0$ | $\beta_{2, 15_4} = 1$ |         |
|           | $\beta_{2, 15_2} = n/a$ | $\beta_{2, 16_4} = n/a$ |         |
|           | $\beta_{2, 16_2} = n/a$ | $\beta_{2, 14_4} = n/a$ |         |
|           | $\beta_{2, 14_2} = n/a$ | $\beta_{2, 13_4} = n/a$ |         |

1 We use the 24-bit CRC specified as 24C in the 5G standard.
that with \( c_e = 1 \), I-Fast-SCLF-32 has a significant FER performance improvement when compared to I-SCLF-32. In addition, the error-correction performance gains of I-Fast-SCLF-32 with respect to I-SCLF-32 quickly reduce as \( c_e \) increases, with the error probabilities of both decoders approaching 1 when \( c_e \geq 4 \).

Note that the error-correction performance degradation of I-Fast-SCLF-32 is also caused by the imperfect error detection of the CRC, where a wrong estimate of the correct codeword that satisfies the CRC is selected as the decoding output. As shown in Fig. 4b, if the CRC verification is replaced by a genie selection scheme, the FER values of I-SCLF-32 and I-Fast-SCLF-32 are relatively unchanged, except for the case of I-Fast-SCLF-32 with \( c_e = 1 \), where an FER of 0 is obtained. This confirms that after the second FSCL decoding attempt of I-Fast-SCLF-32, the correct codeword is always present in the list of the best decoding paths for \( c_e = 1 \).

In the next section, a path selection error model is derived to accurately estimate the index of the path splitting that causes the elimination of the correct path at the initial FSCL decoding. Therefore, the error-correction performance of the I-Fast-SCLF-\( L \) decoder provided in Fig. 3 serves as the empirical lower bound of the proposed decoding algorithm.

### B. PATH SELECTION ERROR MODEL FOR FSCL DECODING

We use the methods introduced in [14], [20] to estimate the erroneous path-splitting index, which predicts the error position using the LLR values associated with each discarded decoding path. Thus, the proposed path selection error model relies on the construction of the LLR vectors obtained at each path splitting under FSCL decoding.

Consider that the first FSCL decoding attempt does not pass the CRC verification and \( \nu \) is a node located at the \( s \)-th stage of the binary tree, that is visited by FSCL decoding. Let \( k \in \{1, K + C\} \) be the path-splitting index that occurs during the decoding of \( \nu \). Let \( \gamma_{\nu} = \gamma_{\nu}^{k} \) be an LLR vector of a discarded decoding path \( \nu^\prime \), which contains \( k \) LLR values corresponding to the hard estimates of the discarded path \( \nu^\prime \). After each information bit is decoded, \( \gamma_{\nu} \) is constructed progressively up to the \( k \)-th path splitting. Formally, \( \gamma_{\nu} \) is obtained using the following procedure:

- If \( \nu \) is a leaf node that contains an information bit:
  \[
  \gamma_{\nu} = \text{concat}(\gamma_{\nu}^{k}, \alpha_{0, i_{\min}^{k}}).
  \]
  \[
  (20)
  \]
- If \( \nu \) is a REP node:
  \[
  \gamma_{\nu} = \text{concat}(\gamma_{\nu}^{k}, \sum_{j = i_{\min}^{k}}^{i_{\max}^{k}} \alpha_{s,j}).
  \]
  \[
  (21)
  \]
- If \( \nu \) is a Rate-1 node: Updating \( \gamma_{\nu} \) using the following function after each path splitting at the \( j \)-th bit:
  \[
  \gamma_{\nu}^{j} = \text{concat}(\gamma_{\nu}^{j}, \alpha_{s,j}),
  \]
  \[
  (22)
  \]
where \( j \in \{i_{\min}^{k}, \ldots, i_{\max}^{k}\} \) is selected by following the indices of the sorted absolute LLR values in (2).

- If \( \nu \) is an SPC node: Updating \( \gamma_{\nu} \) using the following function after each path splitting at the \( j \)-th bit:
  \[
  \gamma_{\nu}^{j} = \text{concat}(\gamma_{\nu}^{j}, \alpha_{s,j}),
  \]
  \[
  (23)
  \]
where \( j \in \{i_{\min}^{k}, \ldots, i_{\max}^{k}\} \setminus i_{\min}^{k} \) is selected by following the order of the sorted absolute LLR values in (2). Note that \( i_{\min}^{k} \) is the bit index of the parity bit.

---

\(^3\)We exclude the FER of I-Fast-SCLF-32 with \( c_e = 1 \) from Fig. 4b as an FER of 0 cannot be plotted in the logarithmic scale.
whose LLR value is ignored when constructing $\gamma_{v'}$. $\text{concat}(\gamma_{v'}, a)$ is a function that concatenates $a \in \mathbb{R}$ to the end of $\gamma_{v'}$ and initially $\gamma_{v'} = \emptyset$. In addition, $\gamma_{v'}$ is not altered if $\nu$ does not satisfy any of the above conditions. For example, the LLR vector $\gamma_{v'}$ obtained after the fifth path-splitting index in Table 2 for $l' = 2$ is $\gamma_2 = \gamma_2^{52} = \{\alpha_{2,52}, \alpha_{2,72}, \alpha_{2,62}, \alpha_{0,122}, \alpha_{2,132}\}$. We now define the hard estimates of $\gamma_{v'}$ as $\eta_{v'} = \hat{\eta}_{v'}^{k_{v'}}$, and the correct hard values associated with $\gamma_{v'}$ as $\eta_{v'} = \eta_{v'}$. For instance, $\eta_2 = \hat{\eta}_2^{52} = \{\beta_{2,52}, \beta_{2,72}, \beta_{2,62}, \beta_{0,122}, \beta_{2,132}\}$ is the discarded decoding path obtained after the fifth path-splitting index in Table 2 with $l' = 2$, and $\eta_2 = \eta_2 = \{0, 0, 0, 0, 0\}$. It is worth to note that by not considering the bit-flipping operations for the parity bits of the SPC nodes, the search space of the first error path selection for FSCCL decoding contains $K + C$ possible positions, which is equal to that of the SCLF decoder.

Unlike SCLF decoding, at the same path splitting index the hard estimates and LLR values of $\eta_{v'}$ and $\gamma_{v'}$ of different path indices $l'$ can correspond to different bit indices of the polar binary tree. However, similar to SCLF decoding, each instance of the hard estimates and LLR values of $\hat{\eta}_{v'}$ and $\gamma_{v'}$ are obtained sequentially by following the course of FSCCL decoding. Therefore, in this paper we utilize the conditional error probability model considered in [14], [15], [20] to estimate the erroneous decision occurred at the $k$-th path splitting index of FSCCL decoding. Specifically, the probability that the discarded path $l'$ at the $k$-th path splitting index under FSCCL decoding is the correct path is

$$
Pr(\eta_{v'}^{k_{v'}} = \eta_{v'}^{k_{v'}} | \alpha_n) = \prod_{1 \leq j < k} \prod_{j \in A_{v'}} \left[ 1 - Pr(\hat{\eta}_{j_{v'}} = \eta_{j_{v'}} | \alpha_n, \hat{\eta}_{j_{v'}}^{-1} = \eta_{j_{v'}}^{-1}) \right],
$$

(24)

where $A_{v'}$ is the set of bit indices $j$ in which the hard estimates $\hat{\eta}_{j_{v'}}$ follow the sign of $\gamma_{j_{v'}}$, and $A_{v'}^c$ is the set of bit indices $j$ in which the hard estimates $\hat{\eta}_{j_{v'}}$ do not follow the sign of $\gamma_{j_{v'}}$.

Similar to $u$, $\eta_{v'}$ is also not available during the decoding process, and thus we use the approximation introduced in [15] to calculate $Pr(\hat{\eta}_{j_{v'}} = \eta_j | \alpha_n, \hat{\eta}_{j_{v'}}^{-1} = \eta_{j_{v'}}^{-1})$ as

$$
Pr(\hat{\eta}_{j_{v'}} = \eta_j | \alpha_n, \hat{\eta}_{j_{v'}}^{-1} = \eta_{j_{v'}}^{-1}) \approx \frac{1}{1 + \exp(\theta - |\gamma_{j_{v'}}|)}
$$

(25)

The path selection error metric obtained at the $k$-th path splitting based on (24) and (25) can be obtained as

$$
Q_k = - \ln \left[ \sum_{v'} Pr(\hat{\eta}_{v'}^{k_{v'}} = \eta_{v'}^{k_{v'}} | \alpha_n) \right]
$$

$$
\approx - \ln \left[ \max_{v'} Pr(\hat{\eta}_{v'}^{k_{v'}} = \eta_{v'}^{k_{v'}} | \alpha_n) \right]
$$

$$
\approx \min_{v'} \left[ \sum_{1 \leq j < k} (|\gamma_{j_{v'}} - \theta|) + \sum_{1 \leq j < k} \text{ReLU}(\theta - |\gamma_{j_{v'}}|) \right]
$$

(26)

Consequently, the most probable erroneous position $l$ is obtained as

$$
l = \arg \min_{l_1, \ldots, l_{K+C}} Q_k.
$$

(27)

The error metric described in (26) can be progressively calculated during the course of decoding, allowing for an efficient implementation of the proposed decoder. In particular, for each active decoding path $l$ we denote by $q_{l-1}$, the path-error metric at the $(k-1)$-th path splitting index of $l$, which

![Figure 4](image-url)
is given as
\[ q_{k-1} = \sum_{1 \leq j \leq k-1} \left( |\gamma_j| - \theta \right) + \sum_{1 \leq j \leq k-1} \text{ReLU} \left( \theta - |\gamma_j| \right) \] (28)
if \( k > 1 \) and \( q_0 = 0 \ \forall l \). Thus, the path-error metric of the path \( l \) at the \( k \)-th path splitting index can be calculated from \( q_{k-1} \) as
\[ q_{ki} = q_{k-1} + \text{ReLU} \left( \theta - |\gamma_{ki}| \right). \] (29)

The path-error metric of the forked path with index \( \tilde{l} \) originating from \( l \), whose hard value at the \( k \)-th path splitting index does not follow the sign of its LLR value, is calculated as
\[ q_{ki} = q_{k} + \gamma_{ki} - \theta. \] (30)

(29) and (30) are used to compute the path-error metrics of all the \( 2L \) paths associated with the current \( L \) active paths and the \( L \) forked paths progressively. Next, the path metric sorting is carried out and a list of discarded paths with indices \( l' \) is determined. The flipping metric in (26) is obtained as
\[ Q_k = q_{k_{l_{\text{min}}}}, \] (31)
where \( l_{\text{min}} = \arg\min_{l'} q_{kl} \). Therefore, under a practical implementation one only needs to maintain the path-error metrics \( q \) corresponding to the most probable paths to progressively calculate the path selection error metric \( Q_k \).

In this paper, we tackle the disadvantage of Monte-Carlo simulation which optimizes the single parameter \( \theta \) offline [14], [18], [20]. This is because in practice, e.g., in the 5G standard, there is a vast number of polar code configurations with different code lengths and rates, and the parameter also requires to be optimized at various SNR values. Thus, optimizing the parameter for each specific configuration is a time-consuming task as adequate training data samples need to be collected for each code configuration. Therefore, we propose an efficient online supervised learning approach to directly optimize the parameter at the operating SNR of the decoder, while obviating the need of pilot signals.

In particular, let \( \mathcal{D} \) be a data batch that contains \( B = |\mathcal{D}| \) instances of the path selection error metrics \( Q = Q_1^{K+C} \), where the corresponding message word estimated by the initial FSCL decoding algorithm does not satisfy the CRC test. Under supervised learning, we need to obtain the incorrect path-splitting index \( \hat{\tau}_e \) to train \( \theta \). Note that in a practical scenario, the proposed decoder often requires a maximum number of \( m \) additional FSCL decoding attempts where a different estimated error index is associated with each additional decoding attempt. By assuming that a correct codeword is obtained if the CRC verification is successful, the error index \( \hat{\tau}_e \) can be obtained when a secondary FSCL decoding attempt passes the CRC verification. Let \( o \) be a one-hot encoded vector of size \( K + C \) that indicates the error bit index \( \tau_e \) as
\[ o_k = \begin{cases} 1 & \text{if } k = \tau_e, \\ 0 & \text{otherwise}. \end{cases} \] (32)

A data sample \( d \in \mathcal{D} \) contains a pair of the input \( Q \) and its corresponding encoded output \( o \), i.e., \( d \triangleq \{Q, o\} \).

Given a data sample \( d \), the path selection error metric introduced in Section III-B provides an estimate of \( \hat{\tau}_e \) as \( \tau \) by selecting the index corresponding to the smallest element of \( Q \) (see (27)). To enable training, the error metrics are converted to the probability domain using the following softmax conversion:
\[ \hat{o}_k = \frac{\exp(-Q_k)}{\sum_{j=1}^{K+C} \exp(-Q_j)}, \] (33)
where \( Q_k \) is manually set to \( \infty \) for \( k \in [1, \log_2 L] \) as the correct decoding path is always present in the first \( \log_2 L \) path splittings. It can be seen from (26) and (33) that the bit index that has the smallest error metric is also the bit index that has the highest probability to be in error. In this paper, we use the binary cross entropy (BCE) loss function to quantify the dissimilarity between the target output \( o \) and the estimated output \( \hat{o} \) as
\[ \text{Loss} = -\sum_{k=1}^{K+C} \left[ o_k \ln \hat{o}_k + (1 - o_k) \ln(1 - \hat{o}_k) \right]. \] (34)

The parameter \( \theta \) can then be trained to minimize the loss function by using the stochastic gradient descent (SGD) technique or one of its variants. An update step is given as
\[ \theta = \theta - \frac{\mathcal{E}}{B} \sum_{d \in \mathcal{D}} \frac{\partial\text{Loss}}{\partial\theta}, \] (35)
where \( \mathcal{E} \in \mathbb{R}^+ \) is the learning rate and \( \frac{1}{B} \sum_{d \in \mathcal{D}} \frac{\partial\text{Loss}}{\partial\theta} \) is the estimation of the true gradient obtained from a data set that contains an infinite number of data samples. By using the chain rule and simple algebraic manipulations, given an instance \( Q \) of a data sample \( d \), \( \frac{\partial\text{Loss}}{\partial\theta} \) can be calculated as
\[ \frac{\partial\text{Loss}}{\partial\theta} = \sum_{k=1}^{K+C} \hat{o}_k - o_k \left[ \frac{\partial\phi_k}{\partial\theta} - \hat{o}_k \sum_{j=1}^{K+C} \frac{\partial\phi_j}{\partial\theta} \right], \] (36)
where \( \phi_k = \exp(-Q_k) \) and \( \frac{\partial\phi_k}{\partial\theta} = -\exp(-Q_k) \frac{\partial Q_k}{\partial\theta} \).

It can be observed that the computation of \( \frac{\partial\text{Loss}}{\partial\theta} \) requires the computation of \( \frac{\partial Q_k}{\partial\theta} \). Similar to \( Q_k \), \( \frac{\partial Q_k}{\partial\theta} \) can also be progressively calculated during the course of decoding. In particular, from (29) and (30) we obtain
\[ \frac{\partial q_{ki}}{\partial\theta} = \frac{\partial q_{k-1}}{\partial\theta} + \frac{\partial \text{ReLU}(\theta - |\gamma_{ki}|)}{\partial\theta} = \frac{\partial q_{k-1}}{\partial\theta} + \mathbb{I}_{\theta > \gamma_{ki}}, \] (37)
and
\[ \frac{\partial q_{ki}}{\partial\theta} = \frac{\partial q_{ki}}{\partial\theta} - 1, \] (38)
respectively, and \( \frac{\partial \theta}{\partial\theta} = 0 \ \forall l \). Since the values of \( \frac{\partial q_{ki}}{\partial\theta} \) and \( \frac{\partial q_{k-1}}{\partial\theta} \) are available for all the current active decoding paths with indices \( l \) and the forked paths with indices \( \tilde{l} \), after the
Algorithm 1: Fast-SCLF Decoding Algorithm

Input : $y, L, m, B$
Output: $\hat{u}$

1. $\theta \sim (0, 1)$ // Initialize $\theta$
2. $u_{init}, Q, \frac{\partial Q}{\partial \theta} \leftarrow \text{InitialFSCL}(y, \theta, L)$
   /* Perform FSCL decoding with the
   reserved path selection scheme */
3. if $\hat{u}_{init}$ passes CRC then
   return $\hat{u}_{init}$
4. else
   $\{i_1, \ldots, i_m\} \leftarrow \text{Sort}(Q)$
5. for $i \leftarrow 1$ to $m$ do
6.   $u_{flip} \leftarrow \text{FSCL}(y, i_i^*, L)$
7.   if $\hat{u}$ passes CRC then
8.     Construct $o$ using (32) given $i_c = i_i^*$
9.     $\theta \leftarrow \text{OptimizeTheta}(\theta, o, Q, \frac{\partial Q}{\partial \theta})$
10. return $\hat{u}_{flip}$
11. return $\hat{u}_{init}$

The inputs of Algorithm 1 contain the channel vector $y$, the list size $L$, the maximum number of additional FSCL decoding attempts $m$, and the size of the data batch $B$, denoted as $B$. The parameter $\theta$ is first randomly initialized from $(0, 1)$. Given a channel output vector $y$, the initial FSCL decoding is carried out in the InitialFSCL() function described in Algorithm 2 which performs the conventional FC decoding operations to obtain the decoded message word $\hat{u}_{init}$. In addition, at each path splitting, with index $k$, of the initial FSCL decoding attempt, the path-error metrics $\{q_k, q_{k+1}\}$ and the derivatives $\{\frac{\partial q_k}{\partial \theta}, \frac{\partial q_{k+1}}{\partial \theta}\}$ of all the paths with indices $l$ and $\bar{l}$ are progressively calculated (line 3-4, Algorithm 2), followed by the computations of $Q_k$ and $\frac{\partial Q_k}{\partial \theta}$ (line 5-6, Algorithm 2). Note that $\frac{\partial Q_k}{\partial \theta}$ is set to 0 and $Q_k$ is set to $\infty$ for all the path splittings with index $k \in [1, \log_2 L]$.

In Algorithm 1, we outline the proposed Fast-SCLF decoding algorithm integrated with the online training framework.

\[ \frac{\partial Q_k}{\partial \theta} = \frac{\partial q_{k \min}}{\partial \theta}. \]  
Note that $\frac{\partial q_{k \min}}{\partial \theta}$ contains integer values and $\frac{\partial Q_k}{\partial \theta} \in [-(K + C), K + C]$. To reduce the computational complexity of the training process, we use the method in [25] to implement the $\exp(\cdot)$ function as required in (33) and (36). Specifically, the Taylor series are utilized to approximate the $\exp(\cdot)$ function, which is given as [25]

\[ \exp(x) \approx \max\{0, \sum_{t=0}^{T} \frac{x^t}{t!}\}, \]  
where $x \in \mathbb{R}$, $T \geq 0$ is an integer number, and the approximation is exact if $T = \infty$ [26].

In Algorithm 1, we outline the proposed Fast-SCLF decoding algorithm integrated with the online training framework.

At the end of the InitialFSCL() function, the first estimate of the message word $\hat{u}_{init}$, the path selection error metrics $Q$, and their derivatives $\frac{\partial Q}{\partial \theta}$ are returned to the main decoding algorithm.

In the next step, if $\hat{u}_{init}$ satisfies the CRC test, the Fast-SCLF decoder then outputs $\hat{u}_{init}$ and terminates. Otherwise, the path selection error metrics $Q$ are sorted in the increasing order such that $Q_{i_1} \leq \ldots \leq Q_{i_{k+c}}$, and the path-splitting indices corresponding to the $m$ smallest elements of $Q$ are selected for the secondary FSCL decoding attempts, i.e., $\{i_1, \ldots, i_m\}$. The Fast-SCLF decoder then performs a maximum number of $m$ additional FSCL decoding attempts (line 8, Algorithm 1) with each attempt performs the reversed path selection scheme at a different path-flipping index $i_i^*$. If one of the secondary FSCL decoding attempts results in a successful CRC verification, the optimization process

Algorithm 2: Initial FSCL Decoding Algorithm

Input : $y, \theta, L$
Output: $\hat{u}_{init}, Q, \frac{\partial Q}{\partial \theta}$

1. Function InitialFSCL($y, \theta, L$):
2. for each path-splitting with index $k \in [1, K + C]$ do
3.   Compute $q_k$ and $q_{k+1}$ based on (29) and (30)
4.   for all the paths $l$ and $\bar{l}$
5.   Compute $\frac{\partial q_k}{\partial \theta}$ and $\frac{\partial q_{k+1}}{\partial \theta}$ based on (37) and (38)
6.   Compute $Q_k$ based on (31)
7.   Compute $\frac{\partial Q_k}{\partial \theta}$ based on (39)
8. for $k \leftarrow 1$ to $\log_2 L$ do
9.   $Q_k \leftarrow \infty$
10. $\frac{\partial Q_k}{\partial \theta} \leftarrow 0$
11. Obtain $\hat{u}_{init}$ from the first FSCL decoding attempt
12. return $\hat{u}_{init}, Q, \frac{\partial Q}{\partial \theta}$

Algorithm 3: Parameter optimization

Input : $\theta, Q, \frac{\partial Q}{\partial \theta}$
Output: $\theta$

1. $c \leftarrow 0$ // The number of data samples
2. $\Delta \leftarrow 0$ // The accumulated gradient
3. Function OptimizeTheta($\theta, Q, \frac{\partial Q}{\partial \theta}$):
4. $c \leftarrow c + 1$
5. Compute $\frac{\partial \text{loss}}{\partial \theta}$ using (36)
6. $\Delta \leftarrow \Delta + \frac{\partial \text{loss}}{\partial \theta}$
7. /* Update $\theta$ and reset the accumulated gradient */
8. if $c \text{ mod } B == 0$ then
9.   $\theta \leftarrow \theta - \frac{\Delta}{B}$
10. $\Delta \leftarrow 0$
11. return $\theta$
of \( \theta \) implemented in the \text{OptimizeTheta}() function is queried, which performs the proposed optimization process based on supervised learning. The details of the function \text{OptimizeTheta}() are provided in Algorithm 3. To reduce the memory consumption required to store the data batch \( \mathcal{D} \) for each parameter update, we use a variable \( \Delta \) in Algorithm 3 to store the accumulated gradients \( \sum_{\forall d \in \mathcal{D}} \frac{\partial \text{Loss}}{\partial \theta} \) as shown in (25). In addition, each data sample \( d \) is completely different from the others due to the presence of channel noise. Therefore, the proposed training framework can prevent overfitting without the need of a separate validation set, which also reduces the memory consumption of the parameter optimization.

Finally, if the resulting estimated message word \( \hat{u}_{\text{flip}} \) obtained from one of the additional FSCL decoding attempts satisfies the CRC test, \( \hat{u}_{\text{flip}} \) is returned as the final decoding output. On the other hand, if none of the additional FSCL decoding attempt can provide a message word that passes the CRC verification, the estimated message word \( \hat{u}_{\text{init}} \) of the initial FSCL decoding is returned as the final output of the decoding process.

C. QUANTITATIVE COMPLEXITY ANALYSIS

To quantify the computational complexity of the decoders considered in this paper, we compute a weighted complexity of the performed floating-point additions/subtractions, comparisons, multiplications, and divisions. The complexity of a floating-point addition/subtraction or a floating point comparison is considered to be one unit of complexity, a multiplication requires 24 units of complexity [27]. In this paper, we use the merge sort algorithm to sort a vector with \( N \) elements, which requires a worst cost of \( N \lfloor \log_2 N \rfloor - 2^{\lfloor \log_2 N \rfloor} + 1 \) floating-point comparisons if \( N \) is not a power of 2, otherwise the number of comparisons needed is \( N \log_2 N \) [28] Chapter 2. We compute the decoding latency of the SCL-based decoders by using the method considered in [9], [10]. In particular, we count the number of time steps for various decoding operations with the following assumptions. First, the hard decisions obtained from the LLR values and binary operations are computed instantaneously [5], [9], [10]. Second, we consider the time steps required by a merge sort algorithm to sort a vector of size \( N \) is \( \lfloor \log_2 N \rfloor \) [28] Chapter 2. In addition, we also measure the average runtime in seconds required to decode a frame of all the decoders considered in this paper. The runtime is measured based on a single-core C++ implementation of the considered decoders on a similar Linux system, with an AMD Ryzen 5 CPU and a DRAM memory of 16 GBytes.

Note that the \text{OptimizeTheta}() function can be executed in parallel with the decoding process presented in Algorithm 1 and the decoding latency in time steps of the \text{OptimizeTheta}() function is significantly smaller than the time steps required by an FSCL decoding attempt. Therefore, we do not include the number of time steps needed by the \text{OptimizeTheta}() function in the time steps of the proposed algorithm. However, to enable a fair comparison with other decoders that do not require parameter optimization during the course of decoding, we include the runtime of the \text{OptimizeTheta}() function when computing the runtime of the proposed decoder. Furthermore, the computational complexity and memory requirement of the \text{OptimizeTheta}() function are also considered when computing those of the proposed decoder. The memory consumption of the proposed decoder with list size \( L \) can be calculated as

\[
\mathcal{M}_{\text{Fast-SCLF}} = \mathcal{M}_{\text{FSCL}} + b_f + L b_f + L b_i + (K + C) b_f + (K + C) b_i + 5 b_f + b_f + \frac{\partial Q}{\partial \theta} \text{-memory} + \frac{\partial Q}{\partial \theta} \text{-memory} + \Delta \text{-memory}
\]

where \( b_i \) is the number of memory bits used to quantize the integer values of \( \frac{\partial Q}{\partial \theta} \) and \( \frac{\partial Q}{\partial \theta} \). We consider that \( \frac{\partial \text{Loss}}{\partial \theta} \) is progressively calculated, thus \( 4 b_f \) memory bits are used to store the temporal values of \( \sum_{j=1}^{K+C} \exp(-Q_j) \), \( \exp(-Q_k) \), \( \text{exp}(Q_k) \), and \( \sum_{j=1}^{K+C} \frac{\partial Q_j}{\partial \theta} \), and \( 5 b_f \) memory bits are used to store \( \frac{\partial \text{Loss}}{\partial \theta} \), whose value is progressively summed over \( K + C \) indices.

IV. EVALUATION

A. OPTIMIZED PARAMETER AND ERROR-CORRECTION PERFORMANCE

We measure the accuracy of the proposed training framework by calculating the probability that the most probable error index \( \hat{e} \) derived from (27) is the actual error index, denoted as \( \tau_e \), given that the initial FSCL decoding attempt does not satisfy the CRC test. Note that the error index \( \hat{e} \) used as the training label can be different from \( \tau_e \). This is because satisfying the CRC test after performing the reserved path selection scheme at the \( \tau_e \)-th path-splitting index does not warrant that the estimated codeword is the sent codeword. Therefore, the training accuracy is quantified as

\[
E[Pr(i = \tau_e | \mathbf{y})] \approx \frac{\sum_{\text{training samples}} 1_{i = \tau_e}}{\text{Number of training samples}} \tag{42}
\]

In this paper, we use the conventional SGD algorithm to optimize \( \theta \) with \( E = 2^{-4} \) and \( B = 32 \), thus \( \frac{\partial E}{\partial \theta} \) is fixed to \( 2^{-9} \) and a multiplication with \( \frac{\partial E}{\partial \theta} \) can be implemented as a shift operation. We set \( b_f = 32 \) for both the training and decoding processes as single-precision floating-point format is used to quantize a floating-point number. In addition, an integer number \( a \) is quantized using the sign-magnitude representation, which requires \( \lfloor \log_2(|a|) \rfloor + 1 \) memory bits.

Fig. 5 illustrates the learning curves of \( \theta \) for \( P(512, 256) \) and \( P(512, 384) \) with \( m = 80 \), \( L = 32 \), \( b_i \in \mathbb{N} \).
Training accuracy with $\theta$ and $\log_2(K + C)$ with list size $32$ is denoted as Fast-SCLF. 

OptimizeTheta proposed framework. In this paper, we stop querying the computational complexity and memory accesses of the function OptimizeTheta. 

In Table 3, we summarize the average computational complexities ($C$) and the average decoding latency in time steps ($L$) of all the SCLF-based decoders considered in Fig. 6. The $E_b/N_0$ values in Table 3 are selected from Fig. 6 where the simulated FER values of the proposed decoder are closest to the target FER of $10^{-4}$. 

The effectiveness of the proposed decoder is confirmed in Table 3 as the decoding latency of the SCLF decoding algorithm is significantly higher than that of the Fast-SCLF decoder with the same list size. However, with the list size increases the Fast-SCLF decoder imposes a more significant computational complexity overhead when compared to that of the SCLF decoder. This is due to the complexity devoted for sorting the LLR values associated with the special SPC and Rate-1 nodes, which significantly increases with the increase of the list size under FSCL decoding. From Table 3 it is observed that the proposed Fast-SCLF decoder reduces up to $73.4\%$ of the average decoding latency of the SCLF decoder with the same list size at the FER of $10^{-4}$, while

\begin{align*}
\{ \lfloor \log_2(K + C) \rfloor + 1, 2 \}, \text{ and } T \in \{\infty, 3\}. \text{ With } b_i = \lfloor \log_2(K + C) \rfloor + 1 \text{ the maximum and minimum values of the derivatives } \frac{\partial Q}{\partial b} \text{ and } \frac{\partial q}{\partial b} \text{ are exactly represented under the sign-magnitude quantization scheme. On the other hand with } b_i = 2, \frac{\partial Q}{\partial b} \text{ and } \frac{\partial q}{\partial b} \text{ are constrained to } \{-1, 0, 1\}. \text{ As observed from Fig. 5 for } T = 3, \text{ constraining } \frac{\partial Q}{\partial b} \text{ and } \frac{\partial q}{\partial b} \text{ with the ternary values of } \{-1, 0, 1\} \text{ does not significantly degrade the estimation accuracy of the proposed error model compared to the configuration using } T = \infty \text{ and } b_i = \lfloor \log_2(K + C) \rfloor + 1. \text{ Therefore, in the rest of this paper, we set } b_i = 2 \text{ and } T = 3 \text{ for the proposed decoder as the computational complexity and memory consumption are significantly reduced by using a small value of } T \text{ and } b_i, \text{ which can be observed from } (40) \text{ and } (41), \text{ respectively. Note that the spikes in the early part of the training accuracy are caused by the small number of the training samples, which makes the calculation of the training accuracy unreliable at the initial phases of the parameter optimization. As also observed from Fig. 5 the value of } \theta \text{ becomes relatively stable as the number of parameter updates increases. Thus, in practice the function OptimizeTheta() can be skipped after a predefined number of parameter updates to further reduce the computational complexity and memory accesses of the proposed framework. In this paper, we stop querying the OptimizeTheta() function after 50 parameter updates to further reduce the computational complexity of the proposed decoder.}

\begin{align*}
\text{FIGURE 5: Training curves of the parameter } \theta \text{ for } P(512, 256) \text{ and } P(512, 384) \text{ with } L = 32 \text{ and } m = 80. \text{ A 24-bit CRC used in 5G is concatenated with the polar codes.}
\end{align*}
incurred a maximum computational overhead of 27.3%. As also seen from Table 3 and Fig. 6 when compared with the SSCLF decoder with \( L \in \{2, 4\} \), the proposed decoder with the same list size only incurs negligible overheads in the computational complexity while achieving significantly error-correction performance improvements and maintaining relatively similar decoding latency in time steps. On the other hand, with \( L \in \{8, 16, 32\} \), a maximum complexity overhead of 13.3% is recorded for the proposed decoder when compared with SSCLF decoding with the same list size, while obtaining relatively similar error-correction performance and decoding latency.

Note that the path selection error metric of SCLF decoding can be progressively calculated using a similar approach as described in (29) and (30). Therefore, the memory consumption of the SCLF decoder with list size \( L \) is calculated as

\[
M_{\text{SCLF}} = M_{\text{SCL}} + b_{f} + Lb_{f} + (K + C)b_{f} 
\]

\[
= M_{\text{SCL}} + (K + C + L + 1)b_{f}. 
\]

In addition, the memory consumption of the SSCLF decoder only requires an addition of \((K + C)b_{f}\) memory bits to store the path-selection error metric when compared with that of the FSCL decoder with the same list size [23]. The memory consumption of the SSCLF decoder with list size \( L \) is given as

\[
M_{\text{SSCLF}} = M_{\text{FSCL}} + (K + C)b_{f}. 
\]

In Table 4, we summarize the memory consumption in KBits of all the SCL-based decoders considered in this paper.

We illustrate the average complexity, average decoding latency in time steps, and average runtime of the Fast-SCLF-
TABLE 4: Memory requirement in KBits of all the SCL-based decoders considered in this paper.

| $P(512, 256)$ | $L$ | 2 | 4 | 8 | 16 | 32  |
|----------------|-----|---|---|---|----|-----|
| FSCL [9]       | 50.0| 84.0|152.0|288.0|560.0|
| SCLF [20]      | 58.8| 92.9|161.0|297.3|569.8|
| SSCLF [23]     | 58.7| 92.7|160.7|295.7|568.7|
| Fast-SCLF      | 60.1| 94.2|162.3|298.6|571.1|

| $P(512, 384)$ | $L$ | 2 | 4 | 8 | 16 | 32  |
|----------------|-----|---|---|---|----|-----|
| FSCL [9]       | 50.0| 84.0|152.0|288.0|560.0|
| SCLF [20]      | 62.8| 97.0|165.0|301.3|573.8|
| SSCLF [23]     | 62.7| 96.7|164.7|300.7|572.7|
| Fast-SCLF      | 64.6| 98.7|166.8|303.1|575.6|

FIGURE 7: Average computational complexity and latency in terms of time steps and runtime of the SCLF-based decoders with list size 4.

As seen from Fig. 7, the proposed decoder requires a relatively similar decoding complexity when compared with the SCLF, while the SSCLF decoder has the lowest average computational complexity among all the SCLF-based decoders. In addition, the SSCLF and Fast-SCLF decoding algorithms require significantly smaller average decoding latency both in terms of time steps and runtime when compared with those of the SCLF decoder.

In Table 5, we summarize the average computational complexity, memory requirement, and average decoding latency in terms of time steps and runtime of the SCLF-based decoders with $L = 4$, $m = 50$, and those of the FSCL-32 decoder. The error-correction performance degradation of the SCLF-based decoders when compared to FSCL-32 is also provided in Table 5. The $E_b/N_0$ values are selected to allow an FER performance close to the target FER of $10^{-4}$ for all the considered decoders. In particular, for $P(512, 256)$, the average complexity and average latency in time steps of Fast-SCLF-4-50 account for approximately 10.7% and 56.3% of the complexity and time steps of FSCL-32, respectively. For $P(512, 384)$, Fast-SCLF-4-50 reduces 84.0% of the average complexity and 27.2% of the average time steps in comparison with FSCL-32. In addition, the proposed decoder with list size 4 requires around 17% of the memory requirement of FSCL-32, while having an FER degradation of less than 0.07 dB. When compared with the SSCLF decoder, the proposed decoder obtains the FER performance gains of 0.2 dB and 0.3 dB at the cost of 8.3% and 12.0% computational complexity overhead for $P(512, 256)$ and $P(512, 384)$, respectively, while the average decoding latency and memory consumption are relatively preserved at the target FER of $10^{-4}$. Note that due to its high complexity, the average runtime of FSCL-32 is significantly higher than those of all the SCLF-based decoders with list size 4.

In Fig. 8 we study the effects of the $\theta$ parameter on the error-correction performance of the proposed decoder when online training is considered. Specifically, we illustrate the FER values obtained at the first 200000 frames of Fast-SCLF-4-50 with and without online learning. In addition, the FER values of the ideal Fast-SCLF-4 decoder are also plotted for reference. It can be observed that the proposed online learning scheme effectively optimizes the $\theta$ parameter, allowing the FER of the proposed decoder to quickly approach its ideal FER performance. On the other hand, when online training is not considered, using the proposed decoder with the initialized value of $\theta$ results in a poor error-correction performance.
TABLE 5: The average computational complexity, average decoding latency, memory consumption, and error-correction performance degradation of the Fast-SCLF, SCLF, and SSCLF decoders with $L = 4$ and $m = 50$ in comparison with those of the FSCL-32 decoder.

|                         | \(P(512, 256) - C24\) | \(P(512, 384) - C24\) |
|-------------------------|-------------------------|-------------------------|
| **Fast-SCLF-4** @2.75 dB| 2.60E+4                 | 3.26E+4                 |
| **SCLF-4** @2.75 dB     | 2.69E+4                 | 3.18E+4                 |
| **SSCLF-4** @3.0 dB     | 2.40E+4                 | 2.91E+4                 |
| **FSCL-32**             | 2.05E-3                 | 1.36E+3                 |
| **Fast-SCLF-4** @4.0 dB | 3.26E+4                 | 3.18E+4                 |
| **SCLF-4** @4.0 dB      | 2.40E+4                 | 9.78E+02                |
| **SSCLF-4** @4.25 dB    | 2.91E+04                | 1.36E+3                 |
| **FSCL-32**             | 2.12E+5                 | 560.0                   |

**FER** (weighted complexity)
- \(\mathcal{L}\) (time steps)
- \(\mathcal{M}\) (KBits)
- Avg. Runtime (seconds/frame)
- FER Degradation (dB)

**FIGURE 8**: Effects of online training on the error-correction performance of the Fast-SCLF-4-50 decoder.

**V. CONCLUSION**

In this paper, we proposed a bit-flipping scheme tailored to the state-of-the-art fast successive-cancellation list (FSCL) decoding, forming the fast successive-cancellation list flip decoder (Fast-SCLF). We then derived a parameterized path selection error metric that estimates the erroneous path-splitting index at which the correct decoding path is eliminated from the initial FSCL decoding. The trainable parameter of the proposed error model is optimized using online supervised learning, which directly trains the parameter at the operating signal-to-noise ratio of the decoder without the need of pilot signals. We numerically evaluated the proposed decoding algorithm and compared its error-correction performance, average computational complexity, average decoding latency, and memory requirement with those of the state-of-the-art FSCL decoder, the successive-cancellation list flip (SCLF) decoder, and the simplified SCLF (SSCLF) decoder. The simulation results confirm the effectiveness of the proposed decoder when compared with the FSCL and the SCLF decoders for different polar codes and various list sizes. As also observed from the simulation results, the error-correction performance of the Fast-SCLF decoder significantly outperforms that of the SSCLF decoder with small list sizes (2 and 4), at the cost of negligible computational complexity overhead, while maintaining relatively similar memory consumption and decoding latency also compared to SSCLF decoding. Future research includes designing and implementing a hardware architecture of the proposed decoder, where the bit-flipping scheme is extended to other special nodes of polar codes.

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