A Wideband Sliding Correlator-Based Channel Sounder with Synchronization in 65 nm CMOS

Ting Wu, Theodore S. Rappaport, Michael E. Knox, Davood Shahrjerdi
NYU WIRELESS, NYU Tandon School of Engineering, New York University, Brooklyn, NY, 11201
Email:{tw1059, tsr, mek407, davood}@nyu.edu

Abstract—A programmable ultra-wideband sliding correlator-based channel sounder with high temporal and spatial resolution is designed in standard 65 nm CMOS. The baseband chip can be configured either as a baseband transmitter to generate a pseudo-random spread spectrum signal with flexible sequence lengths, or as a baseband receiver with sliding correlator having an absolute timing reference to obtain power delay profiles of the multipath components of the wireless channel. The sequence achieved a chip rate of one Giga-bit-per-second, resulting in a multipath delay resolution of 1 ns. The baseband chip occupies an area of 0.66 mm x 1 mm with a power dissipation of 6 mA at 1.1 V in 65 nm CMOS. The sliding correlator-based channel sounder in this work is a critical block for future low-cost, miniaturized channel sounding systems used in accurate and efficient channel propagation measurements at millimeter-wave frequencies.

Index Terms—Sliding correlator channel sounder, on-chip baseband, multipath delay, pseudo-random sequence

I. INTRODUCTION

Advances in manufacturing of silicon integrated circuits have enabled wideband wireless communications networks that operate at millimeter-wave frequencies [1], [2]. These higher frequency bands have massive amounts of raw bandwidth, thereby allowing remarkably high data rates (tens of Giga-bit-per-second, (Gbps)) in spectrum bandwidths that are several hundreds of MHz to a few GHz. A critical step towards the implementation of these emerging wireless technologies is the development of accurate channel propagation models for the frequency bands of interest.

The sliding correlation measurement technique has provided a gold standard for accurate modeling of channel propagation. This direct sequence spread spectrum technique, pioneered by Don Cox of Bell Telephone Labs [3], performs channel propagation measurements in the time domain by transmitting an RF carrier modulated with a high chip rate pseudo-random code and correlating the received signal with a replica of this PN code at the receiver. The output from the correlator represents the power delay profile (PDP) of the wireless channel. Past research has successfully demonstrated the utility of this technique for characterizing radio channels with RF carrier operating at millimeter-wave frequencies up to 73 GHz [4]–[15]. Despite the progress for making propagation measurements at such high frequencies, the increase of the RF bandwidth has remained a difficult task as the pseudo-random sequence requires very high chip rates in order to achieve high resolution in the PDP. Given the short wavelength of the signal at these high carrier frequencies, the signal would experience significant scattering [17]. Therefore, to improve the accuracy of the propagation channel models, it is essential to increase the RF bandwidth. The RF bandwidth of the most current measurement systems is still below 1 GHz [8], [14], [15]. The aim of our paper is to report a chip design that overcomes this limit using low-cost CMOS technology.

The hardware implementation of most sliding correlators reported in the literature have relied on commercial off-the-shelf (COTS) electronic components [8], [12], [14]–[16]. However, the use of COTS for implementing a practical high resolution measurement systems has a few shortcomings. First, the limitation in the maximum chip rate of the baseband electronics reduces the resolution in the power delay profile. Second, COTS-based implementations are often complex and relatively bulky, hindering the ability to make measurements in tight spaces, including crowded offices, inside vehicles and carried by an individual. Third, as massive multiple-input-multiple-out (massive MIMO) is becoming a key research subject for next-generation cellular networks, there is also a need for multiple transmitting and receiving channels that work in parallel to provide a short measurement time. However, COTS hinders the implementation of multiple sounding and receiving channels [18]. Lastly, it increases the overall cost of the implementation, which may be prohibitively expensive for many research entities.

To mitigate the aforementioned problems, we present a low-cost, ultra-wideband, programmable channel sounder with synchronization capability, implemented in a 65 nm standard CMOS process. We anticipate that our wideband channel sounder baseband integrated circuit (IC) will improve the efficiency and accuracy of the channel propagation measurements at millimeter-wave frequencies.

II. ON-CHIP WIDEBAND SLIDING CORRELATOR CHANNEL SOUNDER BASEBAND DESIGN

A. Principles of sliding correlator channel sounder

Fig. [1]a and (b) shows a simplified block diagram of the transmitter (TX) and receiver (RX) of a typical sliding correlator channel sounder. At the TX, the baseband pseudo-random sequence generator (PNSG) generates a PN sequence, $s(t)$, operating at the fast clock rate of $\alpha$. The maximum chip rate of the PNSG is an important parameter since it relates to the multipath delay resolution of $1/\alpha$. Referring to Fig.[1]a, the PN sequence, $s(t)$, is modulated at the intermediate frequency (IF) and then upconverted to the RF carrier frequency, $f_c$. 

The hardware implementation of most sliding correlators reported in the literature have relied on commercial off-the-shelf (COTS) electronic components [8], [12], [14]–[16]. However, the use of COTS for implementing a practical high resolution measurement systems has a few shortcomings. First, the limitation in the maximum chip rate of the baseband electronics reduces the resolution in the power delay profile. Second, COTS-based implementations are often complex and relatively bulky, hindering the ability to make measurements in tight spaces, including crowded offices, inside vehicles and carried by an individual. Third, as massive multiple-input-multiple-out (massive MIMO) is becoming a key research subject for next-generation cellular networks, there is also a need for multiple transmitting and receiving channels that work in parallel to provide a short measurement time. However, COTS hinders the implementation of multiple sounding and receiving channels [18]. Lastly, it increases the overall cost of the implementation, which may be prohibitively expensive for many research entities.

To mitigate the aforementioned problems, we present a low-cost, ultra-wideband, programmable channel sounder with synchronization capability, implemented in a 65 nm standard CMOS process. We anticipate that our wideband channel sounder baseband integrated circuit (IC) will improve the efficiency and accuracy of the channel propagation measurements at millimeter-wave frequencies.
and transmitted into the wireless channel. As the wideband transmit signal propagates through the wireless channel, it experiences reflection, scattering and diffraction effects from the environment. These “multipath” components arrive at the RX with different propagation delays.

At the RX, the propagation delays of the sounding signal are detected by sliding correlating using the same PNSG, but operating with a slightly lower chip rate $\beta$, as shown in Fig. 1(b). The PNSG output is referred as $r(t)$. This sliding correlation can be expressed by [19]

$$ R_s(\tau) = \int_0^T r(t)s(t-t_0-\tau)dt \tag{1} $$

The above expression can be implemented by a pair of mixers followed by two low pass filters. The correlated output, $R_s(\tau)$, is the power delay profile (PDP), representing the time-domain response of the measured wireless channel. The sliding correlation dilates the time scale of the channel response measured at the receiver by a sliding factor $\gamma$, defined as [19]

$$ \gamma = \frac{\alpha}{\alpha - \beta} \tag{2} $$

When examining the received signal in the frequency domain, the bandwidth is compressed, thus easing the hardware design for analog-to-digital converters.

C. Digital D-flip-flop

Edge triggered D flip-flop (DFF) is an important building block in a PN sequence generator. In high-speed and low-power digital VLSI designs, DFFs are often implemented using dynamic logic circuits, such as clocked CMOS (C2MOS), Nora dynamic CMOS, and True single-phase-clock (TSPC).
TSPC DFF is an efficient and simple technique for modern communication circuit design, because it uses a single-phase clock. The TSPC DFF of Yuan and Svensson [21] is constructed by a P-C2MOS stage, an N-precharge stage, and an N-C2MOS stage. Fig. 2 shows the schematic of the TSPC DFF with low-level effective SET, used in this work.

D. PN sequence generator

A PN sequence can be generated using a maximal linear feedback shift register, and the generated sequence is determined by the number of stages in the shift register and a specific combinations of feedback taps [22]. Two types of shift register generators are commonly used: simple shift register generator (SSRG) and modular shift register generator (MSRG). In MSRG, the feedback state from the last stage is added to modulo-2 adders between each stage, and the total delay is less than that of a single-tap sequence generator. Thus, when more than one feedback connections are used, MSRG is preferable than SSRG in terms of speed [23].

The proposed PN sequence generator based on MSRG configuration is shown in Fig. 3. A 3-bit digital words \( S(2 : 0) \) selects the input of the multiplexer to the output, thus determining the number of stages, while \( SW(12 : 1) \) controls the feedback taps. Digital words \( SW(12 : 1) \) should be carefully selected to generate a PN code.

To avoid the “all-zero” condition, the initial state of each DFF is set to one by a low-level effective SET signal (/SET) after power up. The thermal and shot noise can cause the time of the rising edge (or the falling edge) of the binary sequences to vary, adding jitter to the signal, which can accumulate through the propagation of the signal [24]. In order to minimize the jitter, the generated PN sequence from the last stage is followed by a synchronization DFF (Sync-DFF in Fig. 3). The Sync-DFF has the same clock signal as the other DFFs in the shift register, thus the rising edge of the signal is synchronized with the rising edge of the main clock signal CLK. This way, the jitter will be minimized because only one DFF contributes to the jitter.

E. Gilbert cell double-balanced mixer

In order to achieve better signal-to-noise ratio in the sliding correlator channel sounder system, the receiver front-end architecture should provide differential signaling including the mixers. In this design, the mixing in the sliding correlator IC was realized using a Gilbert cell double-balanced mixer shown in Fig. 4. M1 and M2 convert RF input voltage to current. The other four transistors are driven by the LO signal to switch the polarity of the RF current. To improve the mixer performance, sufficient drive from the LO and appropriate biasing must be supplied in order to make the four LO transistors behave as close as possible to ideal switches.

III. Measurement Results

The programmable spread spectrum channel sounder baseband IC was fabricated in a standard 65 nm CMOS process and powered using a 1.1 V power supply. Fig. 5 shows the chip photograph. The chip occupies an area of 0.66 mm × 1 mm.

In order to test the chip, a 4-layer PCB using a FR4 substrate was fabricated and the chip was attached to the board and wire bonded for the signal inputs and outputs. Passive low-pass...
TABLE I
A SUMMARY OF SPECIFICATIONS OF OUR ON-CHIP BASEBAND DESIGN FOR WIDEBAND SLIDING CORRELATOR CHANNEL SOUNDER.

| Item                     | Specification                          |
|--------------------------|----------------------------------------|
| Technology               | 65 nm CMOS                             |
| Maximum chip rate        | 1 Gbps                                 |
| Multipath delay resolution | 1 ns                                   |
| Null-to-null RF bandwidth | 2 GHz                                  |
| PN code length           | $2^N - 1$ (N is programmable from 5 to 12) |
| Area                     | 0.66 mm $\times$ 1 mm                  |
| Synchronization          | Supported                              |

filters with cut-off bandwidths of 100 kHz, were also soldered to the appropriate chip outputs.

Fig. 6(a) shows the time-domain measurement result from PNSG 1 (Mode_control = 0, TX mode). The PN sequence is generated by an 11-stage shift register with a 1 GHz clock. Controls $S(2 : 0) = \text{“110”}$, and $SW(12 : 1) = \text{“00010010010”}$, result in feedback taps of [11,8,5,2]. In order to validate that the measured sequence was a maximal sequence (m-sequence), we first recover the measured analog signal (black) to a binary sequence (blue). Then we count the number of various run-lengths for both “ones” and “zeros” groups (One run is defined as a series of “ones” or “zeros” grouped consecutively), shown in Fig. 6(b). The measured PN sequence has only one run containing eleven “ones” and only one run containing ten “zeros” and equal number of “ones” and “zeros” for the other run-lengths, confirming it is an m-sequence code [23]. The measured spectrum for this PN sequence operating with a clock frequency of 1 GHz is shown in Fig. 6(c). This baseband chip has the capability to program the number of shift register stages in the m-sequence PN code. Fig. 6(d) and (e) shows the measured spectrum for a 5-stage and 8-stage PN code clocked at 1 GHz. Fig. 6(f) shows the spectrum for the 11-stage PN code operating with a 400 MHz clock. This measurement confirms that our baseband IC is flexible and can achieve a maximum clock rate of 1 GHz while also providing programmability in output sequence.

Fig. 7 shows the measurement results of the synchronization signal generated when Mode_control = 1 (RX mode). Two identical 11-stage PN sequences, clocked at 1 GHz and 999.95 MHz respectively, are correlated together to generate the required synchronization signal. Since the length of PN sequence is 2047 chips, the synchronization signal repeats every 40.94 ms. The amplitude of the measured synchronization signal is about 100 mV, which could be further increased if the passive low-pass filters are replaced with active filters.

Table I is a summary of key specifications of the channel sounder baseband chip.

IV. CONCLUSION

In this paper, we presented an on-chip ultra-wideband spread spectrum sliding correlator-based channel sounder with high spatiotemporal resolution. This work is the first known report to achieve a 1 Gbps baseband operation using low-cost CMOS technology. The versatility of this channel sounder provides researchers with the capability to choose the most suitable system parameters when conducting propagation measurements with high accuracy and efficiency. The miniaturized baseband chip can be used for accurate spatiotemporal channel propagation measurements, to identify absolute multipath delays, in system utilizing massive MIMO technology at millimeter-wave carrier frequencies.

ACKNOWLEDGEMENT

The authors acknowledge United Microelectronics Corporation (UMC) for manufacturing the chip. This research is supported by the NYU WIRELESS Industrial Affiliates Program.
REFERENCES

[1] H. Hashemi and S. Raman, *mm-Wave Silicon Power Amplifiers and Transmitters*. Cambridge University Press, 2016.

[2] T. S. Rappaport, R. W. Heath Jr., R. C. Daniels, and J. N. Murdock, *Millimeter wave wireless communications*. Pearson Education, 2014.

[3] D. Cox, “Delay doppler characteristics of multipath propagation at 910 MHz in a suburban mobile radio environment,” *IEEE Trans. Antennas Propag.*, vol. 20, no. 5, pp. 625–635, Sept. 1972.

[4] T. S. Rappaport, S. Sun, R. Mayuzs, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. K. Samimi, and F. Gutierrez, Jr., “Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!” *IEEE Access*, vol. 1, pp. 335–349, May 2013.

[5] T. Zwick, T. Beukema, and H. Nam, “Wideband channel sounder with measurements and model for the 60 GHz indoor radio channel,” *IEEE Trans. Veh. Technol.*, vol. 54, no. 4, July 2005.

[6] T. S. Rappaport, G. R. MacCartney, M. K. Samimi, and S. Sun, “Wideband millimeter-wave propagation measurements and channel models for future wireless communication system design,” *IEEE Trans. on Commun.*, vol. 63, no. 9, pp. 3029–3056, 2015.

[7] M. K. Samimi, G. R. MacCartney, S. Sun, and T. S. Rappaport, “28 GHz millimeter-wave ultrawideband small-scale fading models in wireless channels,” in *Proc. IEEE 83rd Veh. Technol. Conf.*, 2016, pp. 1–6.

[8] G. R. MacCartney, H. Yan, S. Sun, and T. S. Rappaport, “A flexible wideband millimeter-wave channel sounder with local area and NLOS to LOS transition measurements,” in *IEEE Int. Conf. Commun.*, 2017, pp. 1–7.

[9] E. Ben-Dor, T. S. Rappaport, Y. Qiao, and S. J. Lauffenburger, “Millimeter-wave 60 GHz outdoor and vehicle AOA propagation measurements using a broadband channel sounder,” in *IEEE Global Telecommun. Conf.*, 2011, pp. 1–6.

[10] T. S. Rappaport, F. Gutierrez, E. Ben-Dor, J. N. Murdock, Y. Qiao, and J. I. Tamir, “Broadband millimeter-wave propagation measurements and models using adaptive-beam antennas for outdoor urban cellular communications,” *IEEE Trans. Antennas Propag.*, vol. 61, no. 4, pp. 1850–1859, 2013.

[11] T. S. Rappaport, E. Ben-Dor, J. Murdock, and Y. Qiao, “38 GHz and 60 GHz angle-dependent propagation for cellular & peer-to-peer wireless communications,” in *IEEE Int. Conf. Commun.*, 2012, pp. 4568–4573.

[12] C. R. Anderson, T. S. Rappaport, K. Bae, A. Verstak, N. Ramakrishnan, W. H. Tranter, C. A. Shaffer, and L. T. Watson, “In-building wideband multipath characteristics at 2.5 and 60 GHz,” in *Proc. IEEE 56th Veh. Technol. Conf.*, 2002, vol. 1, 2002, pp. 97–101.

[13] S. Hur, Y.-J. Cho, J. Lee, N.-G. Kang, J. Park, and H. Benn, “Synchronous channel sounder using horn antenna and indoor measurements on 28 GHz,” in *Proc. IEEE Int. Black Sea Conf. Commun. Netw. (BlackSeaCom)*, 2014, pp. 83–87.

[14] J. Lee, J. Liang, J.-J. Park, and M.-D. Kim, “Directional path loss characteristics of large indoor environments with 28 GHz measurements,” in *Proc. IEEE 26th Annu. Int. Symp. Pers., Indoor, Mobile Radio Commun. (PIMRC)*, 2015, pp. 2204–2208.

[15] R. Miao, L. Tian, Y. Zheng, P. Tang, F. Huang, and J. Zhang, “Indoor office channel measurements and analysis of propagation characteristics at 14 GHz,” in *Proc. IEEE 26th Annu. Int. Symp. Pers., Indoor, Mobile Radio Commun. (PIMRC)*, 2015, pp. 2199–2203.

[16] G. R. MacCartney and T. S. Rappaport, “A flexible millimeter-wave channel sounder with absolute timing,” *IEEE J. Sel. Areas Commun.*, vol. 35, no. 6, pp. 1402–1418, June 2017.

[17] S. Ju et al., “Scattering Mechanisms and Modeling for Terahertz Wireless Communications,” in *IEEE Int. Conf. Commun.*, May 2019, pp. 1–7.

[18] S. Sun, T. S. Rappaport, R. W. Heath, A. Nix, and S. Rangan, “MIMO for millimeter-wave wireless communications: Beamforming, spatial multiplexing, or both?” *IEEE Commun. Mag.*, vol. 52, no. 12, pp. 110–121, 2014.

[19] T. S. Rappaport et al., *Wireless communications: principles and practice*. New Jersey: prentice hall PTR, 1996, vol. 2.

[20] M. K. Samimi and T. S. Rappaport, “3-D millimeter-wave statistical channel model for 5G wireless system design,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2207–2225, July 2016.

[21] J. Yuan and C. Svensson, “High-Speed CMOS Circuit Technique,” *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–69, Feb. 1989.

[22] R. J. Pirkl and G. D. Durgin, “Optimal sliding correlator channel sounder design,” *IEEE Trans. Wireless Commun.*, vol. 7, no. 9, 2008.

[23] R. C. Dixon, *Spread Spectrum Systems with Commercial Applications, 3rd edition*. John Wiley & Sons, Inc., 2016.

[24] A. Sahafi, J. Sobhi, M. Sahafi, O. Farhanieh, and Z. D. Koozehkanani, “Ultra low power frequency divider for 2.45 GHz ZigBee frequency synthesizer,” *Analog Integr. Circuits Signal Process*, vol. 74, no. 1, pp. 97–103, 2013.