Revitalizing Copybacks in Modern SSDs: Why and How

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ABSTRACT
For modern flash-based SSDs, the performance overhead of internal data migrations is dominated by the data transfer time, not by the flash program time as in old SSDs. In order to mitigate the performance impact of data migrations, we propose rcopyback, a restricted version of copyback. Rcopyback works like the original copyback except that only \( n \) consecutive copybacks are allowed. By limiting the number of successive copybacks, it guarantees that no data reliability problem occurs when data is internally migrated using rcopyback. In order to take a full advantage of rcopyback, we developed a rcopyback-aware FTL, \( rcFTL \), which intelligently decides whether rcopyback should be used or not by exploiting varying host workloads. Our evaluation results show that \( rcFTL \) can improve the overall I/O throughput by 54% on average over an existing FTL which does not use copybacks.

KEYWORDS
Copyback, NAND flash memory, FTL, Storage system

1 INTRODUCTION
Flash-based SSDs move a large amount of data internally for supporting various SSD management tasks such as garbage collection (GC), wear leveling and reliability enhancement. For example, because of the erase-before-write constraint in the NAND flash memory, GC is required to reclaim invalid pages for future writes. During GC, valid pages of a GC victim block should be migrated to a new target block with free pages. Since these internal data copy operations directly interfere with I/O requests from user applications, how to efficiently handle internal data migrations is a key challenge for designing a high-performance SSD.

Although there have been extensive investigations (e.g., [6, 8, 9, 12]) to mitigate the impact of internal data migrations on the SSD performance, most existing techniques do not adequately handle a new performance bottleneck of copy operations in modern SSDs. Unlike old SSDs where the copy cost was dominated by the flash program time \( t_{PROG} \), in recent high-end SSDs, the data transfer time \( t_{DMA} \) between flash cells and off-chip DRAM takes a large portion of the copy cost. This shift in the performance bottleneck is due to two recent flash/SSD technology changes: 1) innovations in the flash cell design (which reduced \( t_{PROG} \)) [11] and 2) a high degree of the internal parallelism in high-end SSDs (which results in frequent access collisions on a shared medium (e.g., a channel bus or a serial DRAM bus) between flash cells and off-chip DRAM.)

In order to minimize \( t_{DMA} \), copyback operations [2] are the most effective solution because the copyback operation can move pages within an SSD without off-chip data transfers, thus eliminating \( t_{DMA} \) completely. However, copyback operations are rarely used in modern SSDs because they cause a fatal reliability problem. When pages are migrated using copyback operations, they bypass an off-chip error-correction code (ECC) module and bit errors occurred during copyback operations are accumulated. If the number of the accumulated bit errors exceeds the correction capacity of the ECC module, the stored data in the copybacked page becomes unreadable. Furthermore, since \( t_{PROG} \) was responsible for a large portion of the data migration time in old SSDs, the performance improvement from copyback operations was marginal. In this paper, however, we argue that it is time to revitalize old copyback operations for modern SSDs.

We revisit copyback operations in the context of modern high-density flash memory and propose a restricted version of copyback, called rcopyback, which works like the original copyback except that data migrated by \( n \) successive rcopyback operations must be error-corrected by an off-chip ECC module. The proposed rcopyback technique is based on a simple observation on the error propagation characteristics of successive copyback operations. From our characterization study with recent 1x nm-node NAND chips, we observed that if we properly limit the number of consecutive copyback operations, accumulated bit errors can be within the error correction capability of a common ECC scheme. Furthermore, we observed that the overhead of internal data migrations is significantly reduced even when only a small number of copyback operations can be successively used. For example, when only two consecutive copyback operations are possible, \( t_{DMA} \) is effectively reduced by 1/3.

Based on the rcopyback model from a detailed characterization study using 1x nm-node NAND MLC chips, we designed a new FTL, called \( rcFTL \), which takes advantage of rcopyback for data migrations. In addition to basic extensions for supporting rcopyback, \( rcFTL \) implements an intelligent data-migration mode selector for maximizing the effect of rcopyback on the SSD performance. The mode selector decides whether rcopyback or an off-chip copy operation is used for a given data migration. For light-load intervals, \( rcFTL \) uses the off-chip copy mode, which increases the number of future rcopyback-eligible blocks. On the other hand, for heavy-load intervals, \( rcFTL \) maximally utilizes rcopyback for higher I/O performance.

We have evaluated \( rcFTL \) using various benchmarks on our SSD emulation environment [7]. Our experimental results show that \( rcFTL \) can improve the overall I/O throughput by 54% on average over a conventional FTL without copyback support. We also show that the proposed migration mode selector is effective in maximizing the efficient use of rcopyback under varying workload requirements.
2 MOTIVATIONS

A typical data migration in SSDs is performed by an off-chip data copy as shown in the left dotted box of Fig. 1. An SSD firmware reads data from a source page and transfers the data to a DRAM buffer through a channel bus. Before the data are sent to the DRAM buffer, errors are corrected by the ECC module of the flash memory controller (FMC). In the program phase, in order to move the data back to the target page, the SSD firmware takes a reverse data path from the DRAM buffer to the target page. When no contention occurs along the off-chip copy data path, the data copy latency $t_{COPY}$ can be expressed as follows: $t_{COPY} = t_{R} + t_{DMA_{out}} + t_{DMA_{in}} + t_{PROG}$ where $t_{R}$, $t_{DMA_{out}}$ and $t_{DMA_{in}}$ are a data transfer time from NAND cells to a per-plane register and a DMA out/in time between the register and DRAM buffer, respectively.

However, in a modern SSD which consists of multiple channels and multiple NAND dies per channel, a large number of data migrations may occur at the same time. A high degree of the parallelism in data migrations may significantly increase $t_{DMA_{in}}$ and $t_{DMA_{out}}$ because of contentions on the channel level as well as the serial bus to/from the DRAM buffer. For example, when eight data migrations are concurrently requested by the SSD firmware, if all eight migrations had both the source page and destination page on the same channel, $t_{DMA_{in}}$ and $t_{DMA_{out}}$ may increase by eight times because all data transfers should be serialized.

On the other hand, when a copyback command is supported by a NAND flash chip, a data migration can be performed without requiring neither $t_{DMA_{out}}$ nor $t_{DMA_{in}}$ as shown in the right dotted box of Fig. 1. The SSD firmware can read data from the source page to the per-plane local register and directly write back to the destination page from the per-plane local register. Since the copyback command transfers data within a given plane, even when multiple data migrations occur at the same time, if they can be supported by the copyback command, all data migrations can complete by $(t_{R} + t_{PROG})$. Thus, if the copyback command can be supported, it can significantly reduce the overhead from SSD-internal data migrations. Unfortunately, however, the copyback command is rarely used in modern SSDs because it accumulates all the bit errors occurred to a page during its migrations. Since, in older NAND flash memory, $t_{PROG}$, which is much larger than $t_{DMA}$, dominated $t_{COPY}$, little effort was made to overcome the error propagation problem of the copyback command.

In order to develop an effective solution to revitalize the copyback for modern SSDs, our proposed technique is motivated by an observation on internal data migration characteristics of storage workloads: most pages migrate internally just a few times. For example, Fig. 2 shows a probability distribution of internal data migrations in RocksDB under the append-random workload of db_bench. 77% of pages migrate less than five times. Therefore, if we could support 4 consecutive copybacks without causing any flash reliability problem, about 86% of off-chip data migrations can be avoided in this workload.

3 RCOPYBACK: COPYBACK WITH A THRESHOLD

3.1 Copyback Error-Propagation Characteristics

In order to manage the flash reliability problem caused by successive copyback operations, it is important to understand the error propagation characteristics when the same page experiences consecutive copyback operations without the ECC module’s involvement. Using 1x nm-node MLC NAND chips, we conducted experiments using a total of 81,920 pages out of 20 NAND chips. First, we confirmed that, in our tested MLC NAND blocks, which consist of 64 word lines (WLs, each of which can store two pages, the MSB page and LSB page), MSB pages of WL 62 were the most unreliable because the outer WLs, the more vulnerable to noise (e.g., hot-carrier effects and gate-induced drain leakage (GIDL)) and the more disturbed from Vpass. Since we are interested in finding a safe bound on the number of consecutive copybacks over all the possible data migrations, we focus on understanding the error propagation characteristics when both the source and destination pages are in WL 62, which is the worst combination from the bit-error rate (BER) perspective.

As with other NAND flash reliability evaluations, we used the NAND retention BER as our measurement metric. The NAND retention BER is based on the number $N(x, t)$ of bit errors after $t$-month retention time at 30°C for $x$ pre-cycled NAND cells [10]. For a given upper limit on the number of consecutive copyback operations, we measured $N(x, t)$ values while changing both $x$’s (i.e., P/E cycles) and $t$’s (i.e., retention times). Fig. 3(a) shows how retention BER’s change as the number of successive copybacks increases. Retention BER values were normalized over $N(0, 0)$. For example, $N(3K, 1 year)$ values increase almost linearly over the number of consecutive copybacks. When a block is erased by 3,000...
3.2 RcCopyback Operation Model

From our characterization study on the copyback error propagation, we constructed a table of copyback threshold \( CT(x,t) \) values for \( x \) P/E-cycled NAND blocks with \( t \)-month retention requirement. The \( CT(x,t) \) value indicates the maximum number of consecutive copyback operations that does not cause any reliability problem for \( x \) P/E-cycled blocks when \( t \)-month data retention is required. Fig. 3(b) shows how copyback threshold values change under varying P/E cycles and different retention time requirements for our evaluated MLC NAND chips. As the retention time requirement increases, the copyback threshold decreases for the same P/E cycle. For the same retention time requirement, as expected, the number of P/E cycles strongly affects the copyback threshold. For the 1-year data retention requirement at 30°C (which is the JEDEC client class retention requirement), the copyback threshold value decreases from 5 to 2 as the P/E cycle increases from 0 to 3,000. That is, after 3K P/E cycles, the copyback command can be consecutively used only twice. If the third data migration is required on the same page, the page must be migrated using an off-chip data copy, thus the accumulated bit errors can be corrected by the ECC engine of the FMC. Table 1 summarizes our proposed \( \text{rc} \)copyback operation model with the 1-year data retention requirement based on the copyback threshold values described in Fig. 3(b).

### Table 1: Rcopyback operation model.

| P/E cycle | \( 1-1000 \) | \( 1001-2000 \) | \( 2001-3000 \) |
|-----------|-------------|-------------|-------------|
| Copyback Threshold | 4 | 3 | 2 |

Figure 3: The effect of successive copybacks on the reliability.

Figure 4: An organizational overview of \( \text{rc} \)FTL.

4.1 Error Propagation Management

The main function of the EPM module is to monitor the cumulative number of successive copyback operations for each page so that no page can be \( \text{rc} \)opybacked more than the copyback threshold. A simple approach to keep track of the cumulative count is to maintain a per-page counter which is incremented whenever \( \text{rc} \)opyback is used for the page. However, for recent high-capacity NAND flash memory, the space overhead of per-page counting is quite high. For example, 1.4-GB memory is needed for supporting a 3-bit per-page counter for a 16-TB SSD. In addition, in highly-optimized commercial SSDs, updating the per-page counter (in slower DRAM memory) can incur a significant CPU cycle overhead as well because memory accesses are optimized to occur in SRAM memory for higher performance. In order to avoid the overhead of per-page counting, the EPM module employs a per-block counting approach. That is, the cumulative number of \( \text{rc} \)opyback operations is manged at the block level, not at the page level. Since the number of counters for the per-blocking counting is at least two orders of magnitude smaller than that for the per-page counting, the per-block counting technique significantly reduces the memory footprint for maintaining counters and minimizes the computing overhead of bookkeeping operations to a negligible level.

Since all the pages in a block are assumed to have been migrated by the same number of \( \text{rc} \)opyback operations in the per-block counting scheme, when a source page \( p \) in a block \( b(c) \) with the counter value \( c \) is migrated by \( \text{rc} \)opyback, the page \( p \) should be moved to a page in a block \( b(c’) \) where \( c’ = c + 1 \). In order to efficiently support this additional constraint, the EPM module manages multiple active blocks at the same time. If the maximum copyback threshold value is given by \( M_{\text{cpb}} \), the EPM module maintains \( (M_{\text{cpb}} + 1) \) active blocks, \( b_0, \ldots, b_{M_{\text{cpb}}} \), where \( b_i \) indicates a block with its counter value \( i \). Fig. 5 shows an example of how data migrations are performed using \( \text{rc} \)opyback operations in the per-block counting scheme. For example, when the block \( vb(1) \)
is selected as a GC victim block, its valid pages, C and D, are moved to the active block b(2) when they are migrated using rcopyback operations. When the block v(b(M_p)) is selected as a GC victim block, its valid pages are moved using off-chip copies to the active block b(0).

**4.2 Data Migration Mode Selection**

Since the copyback threshold is rather small, using rcopyback in a greedy fashion may not be the most effective use of it from an overall I/O throughput perspective. For example, when no high I/O throughput is required, it does not make sense to use rcopyback for data migrations. Doing so may prevent more effective future use of rcopyback when high I/O throughput is needed. Furthermore, when the high I/O bandwidth is not necessary, using off-chip data migrations enables more future data migrations to be supported by rcopyback.

In order to take full advantages of rcopyback, the DMMS module intelligently chooses when to use rcopyback operation over a normal off-chip copy depending on the write buffer utilization ratio u. When u is low, which indicates that the current host I/O workload is not intensive, the DMMS module selects the off-chip copy mode so that more future data migrations can be supported by rcopyback. On the other hand, when u is high, the DMMS module chooses the rcopyback mode for higher performance. In our current implementation, the utilization threshold ratio for the mode selection was set to 50% (That is, if u is higher than 50%, the rcopyback mode is used for data migrations.) Since rcFTL employs the per-block counting scheme and most data migration decisions are made in a block granularity, the DMMS module makes its mode selection decisions in a per-block level as well. When a data migration decision is made (e.g., by a foreground GC task), the DMMS module selects a proper mode based on the current u value. In order to filter out abrupt noise-like changes in u, the DMMS module makes its mode selection based on a t-second moving average of u. In the current implementation, t is set to an average block write time.

In rcFTL, both the garbage collector and wear leveler operate in an rcopyback-aware fashion. For urgent management tasks (such as a foreground GC task), the rcopyback mode is actively used regardless of the current u ratio value. On the other hand, when background management tasks (such as a background GC task) are invoked, the DMMS module decides proper modes as explained above.

**5 EXPERIMENTAL RESULTS**

**5.1 Experimental Setup**

In order to evaluate the effectiveness of the proposed rcFTL technique, we implemented rcFTL as a host-level FTL on a custom flash storage system [7]. For our evaluation, we configured our flash storage system to support a 64-GB storage capacity only for efficient experimental evaluations. Our emulated storage system was configured to have eight channels with eight NAND flash chips per channel. Each NAND flash chip has 1024 blocks which are composed of 64 16-KB pages. The average tPROG was set to 640 us and the size of the write buffer was set to 10 MB. We evaluated rcFTL using four I/O traces generated from Sysbench [3] and Filebench [1]. As shown in Table 2, each workload has different ratios between read and write and different WAF values. Using these workloads, we evaluated the overall I/O throughput for three different rcFTL versions, rcFTL2, rcFTL3, and rcFTL4, where rcFTLn indicates that the maximum copyback threshold was set to n. All measurements were normalized over a page-level mapping FTL which always migrates data using the off-chip copy.

**5.2 Evaluation Results**

Fig. 6(a) shows normalized I/O throughputs of different rcFTL versions. As the copyback threshold increases, the I/O throughput increases accordingly because more data migrations are supported by rcopyback. The overall I/O throughput was improved on average by 54% in rcFTL4 over the baseline FTL. Even rcFTL2, which can use rcopyback only twice in a row, outperforms the baseline by 41% on average. As the maximum copyback threshold increases, the I/O throughput of NTRX quickly increases over other traces. This difference comes from the difference in update patterns of each trace. In general, when data are updated sequentially (as in Varmail), it is less likely that data are moved multiple times, thus
making rcFTL with a higher maximum copyback threshold less efficient.

In order to understand how the mode selector proposed in rcFTL performs, we compared the performance of rcFTL with rcFTL- (which uses rcopyback in a greedy fashion). Fig. 6(b) shows how these two rcFTL versions compare under varying I/O intensity cases. In order to generate workload fluctuations, which are needed to properly evaluate the DMMS module, we generated three synthetic workloads, High, Mid and Low, using Fio. In High, 70% of I/O requests were issued without inter-request idle times while 30% were issued with some idle times. For Mid and Low, the ratio between two requests is 50:50 and 30:70, respectively. When the I/O intensity is lower, since the off-chip copy mode is more likely to be used in rcFTL, rcopyback-eligible blocks tend to increase over rcFTL—because the per-block counters of more blocks are reset. The increased number of rcopyback-eligible blocks, in turn, improves the I/O throughput when the I/O intensity is high. In Fig. 6(b), rcFTL2 outperforms rcFTL- by this effect. In particular, for the Low case, rcFTL2 improves the I/O throughput by 17% over rcFTL-.

6 RELATED WORK

There have been several studies to improve the performance of flash-based storage systems with the copyback operation. However, many existing techniques [4, 13, 14] are not applicable for modern NAND flash memory because they assumed an ideal SLC NAND flash memory where no error propagation occurs from successive copyback commands. Other studies such as Jang et al. [5] considered the error propagation problem in their techniques. However, their solutions was to bring data out to the ECC module to check the validity of data, thus minimizing the potential benefit of using copyback. Our technique is different from existing techniques in that the error propagation problem is fully controlled while maximizing the potential benefit of copyback.

7 CONCLUSIONS

We have presented rcopyback to minimize performance degradations from internal data migrations in modern highly-parallel SSDs. From an experimental characterization study, we developed a rcopyback operation model that takes as the key input the P/E cycle and data retention requirement. Based on the rcopyback operation model, we have implemented a rcopyback-aware FTL, rcFTL, which intelligently manages when to use rcopyback for a given I/O workload requirement. Our experimental results show that rcFTL can improve the overall I/O throughput by 54% on average over an existing FTL with no copyback supported.

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