Negative Capacitance Double-Gate Junctionless FETs: A Charge-based Modeling Investigation of Swing, Overdrive and Short Channel Effect

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Abstract—In this paper, an analytical predictive model of the negative capacitance (NC) effect in symmetric long channel double-gate junctionless transistor is proposed based on a charge-based model. In particular, we have investigated the effect of the thickness of the ferroelectric material on the I-V characteristics. Importantly, for the first time, our model predicts that the negative capacitance minimizes short channel effects and enhances current overdrive, enabling both low power operation and more efficient transistor size scaling, while the effect on reducing subthreshold slope shows systematic improvement, with subthermionic subthreshold slope values at high current levels (0.1 µA/µm). Our predictive results in a long channel junctionless with NC show an improvement in ON current by a factor of 6 in comparison to junctionless FET. The set of equations can be used as a basis to explore how such a technology booster and its scaling will impact the main figures of merit of the device in terms of power performance and gives a clear understanding of the device physics. The validity of the analytical model is confirmed by extensive comparisons with numerical TCAD simulations in all regions of operation, from deep depletion to accumulation and from linear to saturation.

Index Terms—Negative capacitance, charge-based model, double-gate junctionless FET, Short channel effect.

I. INTRODUCTION

ADVANCED aggressive scaling of conventional metal-oxide-semiconductor field-effect transistors (MOSFET) requires the use of advanced processing with multiple additive technology boosters, such as strain, high-k dielectrics with metal gate stacks, shallow junctions and the replacement of the silicon channel with materials having higher carrier mobility [1], [2]. Even more sophisticated techniques for locally controlling the strain have been proposed in various research works [3]. Significant efforts are needed for the junction and contact engineering in such advanced MOSFETs. A lot of effort has been recently dedicated to the so-called steep-slope transistors [4] but their maturity is still far from being adopted by the nanoelectronics industry. In an attempt to remove all the limitations related to the junction engineering at nanoscale, the concept of junctionless field-effect transistors (JLFET) has been proposed, where the conduction in a very thin, highly doped semiconductor film is controlled by a gate field effect. Because of the absence of source and drain junctions, junctionless transistors are free from steps to create ultra-steeep junctions and high thermal annealing for S/D dopant activation, which is a big advantage for scaling and cost reduction at nanoscale [5].

However, the scaling of MOS devices must cope with issues such as increased power consumption and degraded off-state current [6] upon reduction of the power supply to mitigate power consumption. The main parameter limiting the power supply voltage scaling in MOS devices is the intrinsic limit of 60 mV/dec at 300 K of the subthreshold swing (SS). To overcome this, it was proposed to add to the conventional insulator of the gate oxide a ferroelectric material of a given thickness that will create an effective negative capacitance, resulting in a reduction of the transistor body factor below unity. This would lead to SS values lower than 60 mV/dec [7]–[13]. Having negative capacitance means that a given charge density in the channel can be achieved with a lower gate voltage. In [10] the use of a ferroelectric gate with voltage amplification has been proposed for the first time to be used to boost Tunnel FET characteristics, with the possibility to achieve near-zero hysteresis in NC devices. In the original paper by Sallahudin and Datta [9], the negative capacitance amplifies the gate voltage and as a result, the subthreshold slope is reduced. More recently, EPFL has highlighted and demonstrated for the first time by experiments that negative capacitance can play a significant role to improve the ON current and/or improve the overdrive in an enhancement-mode MOSFET [12], [13]. This is setting a very interesting direction for the efforts of both academic and industrial research in the field, as the negative capacitance can be considered an ultimate technology booster at the nanoscale. In this work, we investigated by calibrated modeling and simulations, for the first time the effect of negative on the characteristics of junctionless transistors. The phenomena of a ferroelectric material have been modeled by Ginzburg and Devonshire which is based on the Landau theory of phase transitions [14]. Landau theory can predict the behavior of ferroelectric material. To the best of our knowledge, it is the most common approach to the study negative capacitance effect with ferroelectrics [9]–[16]. The negative capacitance in the conventional MOSFETs is still under investigation and modeling of a ferroelectric junctionless transistor was attempted in [17]. Still, the model in [17] it is not a charge based model and there is no evidence of an instability in the simulations, nor the effect of negative capacitance on short channel effects is discussed.
Thus, in order to take account the ferroelectric in junctionless transistors in a simple and compact model approach, in this work we propose analytical and explicit relationships taking into account the negative capacitance effect in Double-Gate JLFET (NCDG JLFET) and evidences for the first time an amplification of the current-voltage dependence with respect to the ferroelectric thickness. This model relies on the charge-based approach developed in [18]–[23]. This approach will be validated with technology computer-aided design (TCAD) simulations in all regions of operation from deep depletion to accumulation and linear to saturation. The effect of the negative capacitance on DIBL (Drain Induced Barrier Lowering) based on the 2D Poisson-Boltzmann relationship is also addressed.

II. MODELING APPROACH

Three-dimensional schematic of the structure of the symmetric double-gate junctionless transistor with the ferroelectric layer is shown in Fig. 1(a). In this structure, an intermediate metallic layer is considered between the insulator and the ferroelectric material. This ferroelectric gate stack architecture in the MOSFET [16], imposes a uniform electric field in the ferroelectric [8]. As such, it will simplify the model derivation at aim in this work.

We call the potential of this inner metal layer \( V_{\text{gate\,(eff)}} \) and the potential of the real gate, \( V_{\text{gate}} \). Hence the potential across the ferroelectric can be expressed as

\[
V_f = V_{\text{gate}} - V_{\text{gate\,(eff)}}.
\]

(1)

According to the Landau theory, the Gibbs free energy \( F \) of the ferroelectric material, respect to the polarization \( P \) is

\[
F = \alpha P^2 + \beta P^4 + \gamma P^6 - \bar{E} \cdot \bar{P},
\]

(2)

where \( \alpha, \beta, \gamma \) are ferroelectric material constants and \( \bar{E} \) is the electric field in the ferroelectric. The \( F-P \) curve has two minima as shown in Fig. 1(b). These represent the two counter stable states in the ferroelectric material (\( \pm P \)) which can be switched by applying an external electric field (note that since the electric field and polarisation are uniform and aligned with the y-axis, we will consider them as scalars). Then we have \( Q=\bar{P} \) and \( V_f=Et_f \) [9], where \( Q \) is the charge density of the ferroelectric (per unit area) and \( t_f \) is the ferroelectric thickness. The derivation of \( F \) with respect to \( Q \) gives (see Fig. 1(c))

\[
\frac{\partial F}{\partial P} = \frac{\partial F}{\partial Q} = 2\alpha Q + 4\beta Q^3 + 6\gamma Q^5 - V_f/t_f,
\]

(3)

The capacitance is related to the slope of the \( P-E \) curve as follows (see the Appendix)

\[
C = \frac{1}{t_f} \left( \epsilon_0 + \frac{dP}{dE} \right),
\]

(4)

thus, as illustrated in Fig. 1(b) and c, there is a region where the capacitance in negative (red rectangular). The domain is normally unstable but can be stabilized when combined with a capacitor in series [9]. The stable state corresponds to a minimum in the Gibbs free energy, which is obtained when (3) is zero. This happens for a specific \( Q-V_f \) relationship

\[
V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5.
\]

(5)

From the charge-based model in [18], [19], what we know is the relationship between the \( V_{\text{gate\,(eff)}} \) and the charge density in the channel. In addition, from (1) and (5), we also know how \( V_{\text{gate}} \) and \( V_{\text{gate\,(eff)}} \) are interrelated. These set of relations will be now combined to simulate the device characteristics with respect to the external voltages (gate, source and drain).

A. Recalling JLFET Core Equations

We consider an n-type long-channel symmetric double-gate JLFET with ferroelectric material (as shown in Fig. 1(a)) with a doping density \( N_D \), a channel length, thickness and width \( L_p, T_{sc} \), and \( W \) respectively. Gate oxide and ferroelectric film thicknesses are \( t_{ox} \) and \( t_f \). Device and ferroelectric material parameters are listed in Table I and Table II respectively. When the JLT is in depletion mode, the channel becomes depleted of majority carriers and results in negligible current conduction (See A in Fig. 1(d)). By increasing the gate voltage carriers can pass through the channel and the electron concentration

Fig. 1: (a) 3-D Schematic view of a double-gate JLFET with negative capacitance. (b) The double-well free energy in ferroelectric versus the electric polarization (\( P \)) from the Landau theory of ferroelectrics. (c) Polarization of ferroelectric as a function of the electric field. The red rectangular in (b) and (c) denotes the region of negative capacitance. (d) Drain current versus the applied gate voltage and electron concentration corresponds to depletion, accumulation and hybrid channel mode of a junctionless transistor at \( V_{DS} = 1 \text{ V} \).
increases which is called hybrid channel (See B in Fig. 1d). Finally, when the JLT is in accumulation, a high electron concentration in the channel appears, facilitating current conduction between source and drain (See C in Fig. 1d).

According to the derivation of the charge-based model for double-gate symmetric JLFETs developed in [18]–[20], we have the two following relationships which link the surface potential \( \psi_s \) and the center potential \( \psi_0 \)

\[
E_s^2 = \frac{2qn_i U_T}{\epsilon_{si}} \left[ \exp \left( \frac{\psi_s - V_{ch}}{U_T} \right) - \exp \left( \frac{\psi_0 - V_{ch}}{U_T} \right) \right]
- \frac{N_D}{n_i} \left( \frac{\psi_s - \psi_0}{U_T} \right)^{2},
\]

(6)

where \( n_i \) is the intrinsic carrier concentration, \( \epsilon_{si} \) is the permittivity of silicon, \( V_{ch} \) is the quasi Fermi potential, \( U_T = k_B T / q \) is the thermal voltage, other symbols having their usual meaning. Since \( E_s \) is the surface electric field and is equal \( Q_{sc} / 2 \epsilon_{si} \), the semiconductor (total) charge density \( Q_{sc} \) is linked to the surface and center potentials

\[
\frac{Q_{sc}}{2 \epsilon_{si}} = \frac{2qn_i U_T}{\epsilon_{si}} \left[ \exp \left( \frac{\psi_0 - V_{ch}}{U_T} \right) - 1 \right] - \frac{N_D}{n_i} \left( \frac{\psi_s - \psi_0}{U_T} \right)^{2}.
\]

(8)

The total charge in the semiconductor, \( Q_{sc} \), is also related to the potential which drops across the gate capacitor

\[
Q_{sc} = -2C_{ox} \left( V_{gate(eff)} - \Delta \phi_{ms} - \psi_s \right),
\]

(9)

where \( C_{ox} \) is the capacitance of the insulator and \( \Delta \phi_{ms} \) denotes the difference between the work function of metal and the work function of the intrinsic semiconductor.

1) Depletion Mode: In depletion mode, the potential at the center of the semiconductor channel is higher than the surface potential, and the net charge density in the semiconductor is positive (\( Q_{sc} \geq 0 \)). Therefore, the exponential term in (8) is negligible than the second term and thus relation (8) can be simplified to

\[
\frac{Q_{sc}}{2 \epsilon_{si}} = \frac{2qn_i U_T}{\epsilon_{si}} \left( \psi_0 - \psi_s \right).
\]

(10)

By introducing (7) in (10) and then in (9), the effective gate potential in the depletion mode with respect to the total charge density is as follows

\[
V_{gate(eff)} = \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln \left( \frac{N_D}{n_i} \right)
+ U_T \ln \left[ 1 - \left( \frac{Q_{sc}}{Q_{f}} \right)^{2} \right] - \frac{Q_{sc}^{2}}{8C_{sc}Q_{f}},
\]

(11)

where \( Q_{f} = qN_D T_{sc} \) is the fixed charge in the channel and \( C_{sc} = \epsilon_{si} / T_{sc} \).

2) Accumulation Mode: Under accumulation mode, the last term in (8) is always smaller than the exponential term, which leads to a negative charge density in the semiconductor \( (Q_{sc} \leq 0) \). In addition, in accumulation, the center potential remains close to the value it takes at the flat-band condition \( \psi_0 \approx V_{ch} + U_T \ln (N_D / n_i) \) [18]. Therefore, relation (8) can be approximated with

\[
\frac{Q_{sc}}{2 \epsilon_{si}} = \frac{2qn_i U_T}{\epsilon_{si}} \left[ \exp \left( \frac{\psi_s - V_{ch}}{U_T} \right) - \frac{N_D}{n_i} \right].
\]

(12)

Substituting (9) in (12), the effective gate voltage in accumulation mode becomes

\[
V_{gate(eff)} = \Delta \phi_{ms} + V_{ch} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln \left( \frac{N_D}{n_i} \right)
+ U_T \ln \left( 1 + \frac{Q_{sc}^{2}}{\theta} \right),
\]

(13)

where \( \theta = 8\epsilon_{si} qN_D U_T \).

3) Drain Current: The relationships derived previously [11] and [13] for depletion and accumulation modes give rise to explicit relationships for the channel current [18]. The drain current in depletion is given by

\[
I_{D_{dep}} = \mu \frac{W}{L} \left[ \frac{1}{8C_{sc}} - \frac{1}{4C_{ox}} \right] Q_{sc}^{2} - \frac{Q_{sc}^{3}}{12Q_{f}C_{sc}}.
\]

(14)

and in accumulation we have

\[
I_{D_{acc}} = \mu \frac{W}{L} \left[ \frac{Q_{f}}{2C_{ox}} + 2U_T \right] Q_{sc} - \frac{1}{4C_{ox}} \frac{Q_{sc}^{2}}{8Q_{f}C_{sc}U_{T}}
- 2U_{T} \ln \left( 1 + \frac{Q_{sc}^{2}}{8Q_{f}C_{sc}U_{T}} \right) \frac{Q_{sc}}{\sqrt{8Q_{f}C_{sc}U_{T}}}.
\]

(15)

where \( \mu \) is the free carrier mobility assumed constant along the channel in this work. Also, for gate voltages where the an hybrid channel takes place [18], i.e. part of the channel (near the source) in accumulation and the rest in depletion, the drain current becomes \( I_{hyb} = I_{D_{acc}} + I_{D_{dep}} \).

B. Merging JLFET with Ferroelectric

1) Landau Equation: In this section, we will merge the model of the JLFET described above with the core relation governing the ferroelectric layer.

2) Total Charge Density: To obtain \( V_f \) from (3) the total charge density in the ferroelectric material \( Q \) must be known. This is obtained by calculating the integral of the semiconductor charge density over the channel length

\[
W L_g \times 2Q = - \int_{0}^{L_g} W Q_{sc} dx.
\]

(16)

The total charge density is the sum of fixed and mobile charges \( Q_{sc} = Q_{f} + Q_{m} \). Hence, we can write

\[
L_g \times 2Q = -Q_{f} L_g - \int_{0}^{L_g} Q_{m} dx.
\]

(17)
Although we do not know how \( Q_m \) is related to \( x \), we know the relation between \( Q_m \) and \( V_{ch} \) from (11) and (13) in depletion and accumulation modes respectively. In addition, from the drain current \( I_{ds} \) relationship, we \( dx \) and \( V_{ch} \) are linked as follows:

\[
dx = -\frac{\mu Q_m}{I_{ds}} dV_{ch}. \tag{18}
\]

By substituting (13) in (17) the integral in space turns into an integral over the potential of the channel from the source (S) to the drain (D):

\[
Q = \frac{-Q_f}{2} + \frac{\mu}{2L_g I_{ds}} \int_{S}^{D} Q_m^2 dV_{ch}. \tag{19}
\]

In depletion mode, \( dV_{ch} \) is obtained from (11) as follows:

\[
dV_{ch} = \left( \frac{1}{2C_{ox}} + \frac{2U_T Q_{sc}^2}{Q_f} + \frac{Q_{sc}}{4C_{sc}^2 Q_f} \right) dQ_{sc}. \tag{20}
\]

Since \( dQ_{sc} = dQ_m \), we introduce (20) in (19) and \( Q \) becomes:

\[
Q = \frac{-Q_f}{2} + \frac{\mu}{2L_g I_{ds}} \int_{S}^{D} \left( \frac{Q_m^2}{2C_{ox}} + \frac{2U_T Q_{sc} Q_m}{Q_f} + \frac{Q_{sc}^2 Q_m}{4C_{sc} Q_f} \right) dQ_m. \tag{21}
\]

After solving the integral, an analytical and explicit relation for the total charge in the ferroelectric is obtained (in depletion mode):

\[
Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}} \left\{ \frac{Q_m^3}{6C_{ox}} + 2U_T \left[ Q_m Q_f - \frac{Q_m^2}{2} - 2Q_f^2 \ln(2Q_f + Q_m) \right] \right\}. \tag{22}
\]

In accumulation, we have

\[
dV_{ch} = \left( \frac{1}{2C_{ox}} + \frac{2U_T Q_{sc}}{Q_f^2} + \theta \right) dQ_{sc}. \tag{23}
\]

Substituting (23) in (19) gives:

\[
Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}} \int_{S}^{D} \left( \frac{Q_m^3}{2C_{ox}} + \frac{2U_T Q_{sc}^2 Q_m}{Q_f^2 + \theta} \right) dQ_m. \tag{24}
\]

Solving (24) gives an analytical and explicit relationship for the total charge density of the ferroelectric when the whole device is biased in accumulation:

\[
Q = -\frac{Q_f}{2} + \frac{\mu}{2L_g I_{ds}} \left\{ \frac{Q_m^3}{6C_{ox}} + 2U_T \left[ \frac{Q_m^2}{2} + \frac{Q_f^2 - \theta}{2} \ln(Q_{sc} + \theta) - Q_m Q_f \right] \right\}. \tag{25}
\]

The way charges and voltages have been calculated is now explained: for a given effective gate voltage \( V_{gate(ef)} \), the total charge density of ferroelectric \( Q \) is known either from
Next, introducing $Q$ in (5) and using equation (1), the applied gate voltage $V_{gate}$ is finally obtained.

Proceeding through this sequence greatly simplifies the way plots are obtained, avoiding cumbersome self-consistent calculations, and providing a clear and simple understanding of the imbrication of the different parts of the model.

To confirm the validity of the model, we performed simulations with TCAD software. The simulation result of NCDG JLFET is numerically calculated by combining SILVACO TCAD software with a MATLAB script to include the Landau calculations, and providing a clear and simple understanding of the fabrication of the different parts of the model.

For extracting the coefficients in relation (5), we rely on the data published in literature [15] where authors used an HZO film as a ferroelectric material with a remanent polarization $P_r$ of about $17 \mu C/cm^2$ and a coercive field $E_c$ of about $1.2 MV/cm$. By using the experimental data of remanent polarization and coercive field and based on the approach presented in [24], we extracted the Landau coefficients.

Next, we consider a double gate JLFET with $1 \mu m$ channel length and width, and with $10 nm$ of silicon thickness. The doping density and oxide thickness were set respectively to $N_D = 10^{19} cm^{-3}$ and $1 nm$ (see Table I).

Fig. 2a and b show the applied gate voltage versus the effective gate voltage for various thickness of the ferroelectric ranging from $2 nm$ to $12 nm$, both at low and high $V_{DS}$ respectively. Lines and blue circles have been used for the analytical model and TCAD simulations, respectively. The analytical model at both low and high $V_{DS}$ demonstrates a full agreement with TCAD simulations. It can be seen that increasing the thickness of ferroelectric layer increases the voltage amplification, which is the signature of the negative capacitance effect.

The total charge density of the ferroelectric versus the applied gate voltage at $V_{DS} = 10 mV$ and $V_{DS} = 1 V$ obtained from TCAD simulations and from the model is plotted in Fig. 2c and Fig. 2d.

To summarize, the total charge density of ferroelectric is now known in all regions of operation from depletion (22) to accumulation (25), resulting in a relationship between $V_{gate_{eff}}$ and $V_{gate}$. Furthermore, we know the link between $V_{gate_{eff}}$ and the mobile charge density in the channel, and so the relationship between $V_{gate}$ and $Q_m$, giving finally the expected $I_D - V_{gate}$ dependence.

Fig. 3e and f illustrate the drain current versus the applied gate voltage at $V_{DS} = 10 mV$ and $V_{DS} = 1 V$ for ferroelectric thicknesses from $8 nm$ to $12 nm$. Increasing the thickness of ferroelectric causes a shift to the higher voltage in the subthreshold region, because in subthreshold the amount of fixed charge in the channel dominates over the mobile charge ($-Q_f/2$ in equation (22)). This makes a constant background of charge density regarding to the $t_f$ in the Landau equation. Beyond a threshold voltage, the slope increases and above a critical thickness $t_{cr}$ a snaps back due to the hysteresis effect of a ferroelectric layer is observed. These regions are unstable which are depicted with a rectangular in Fig. 2e and f. In order to have a non-hysteretic operation, the total gate capacitance should be positive in the whole range of the gate voltage [16]. Fig. 3a shows SS versus the drain current in different thicknesses of ferroelectric at low and high $V_{DS}$. It illustrates that NC systematically reduces the slope, even if not sub-60 mV/dec in all regimes. Subthermionics values down to sub 10 mV/dec are achieved at moderate drain currents and low $V_{DS}$ (see Fig. 3b). It means that NC still causes a significant improvement in the overdrive voltage. On the other hand, by using a negative capacitance, we gain a remarkable increase in ON current as illustrated in Fig. 3c. Fig. 3c shows the percentage of increment of ON current versus applied gate voltage in different thicknesses of the ferroelectric layer.

Our results are conceptually in agreement with the experimental and simulation works [12], [16]. But it worth to note that these are different from previous work on modeling and simulation of a junctionless transistor with ferroelectric [17] where no such behavior was evidenced.

III. SHORT CHANNEL EFFECT

In this section, we investigate how negative capacitance can affect the DIBL short channel effect. To this purpose, we need to solve the two dimensional Poisson-Boltzmann relationship in the channel in subthreshold. This was done for a regular JLFET in [25].

The potential distribution obtained from the 2D Poisson-Boltzmann relation is expressed as follows [25]:

$$\psi(x, y) = \psi_s(x) \left[ 1 + y \left( 1 - \frac{y}{T_{sc}} \right) \frac{C_{ox}}{\epsilon_{si}} \right]$$

+ $(\Delta \phi_{ms} - V_{gate_{eff}}) y (1 - \frac{y}{T_{sc}}) \frac{C_{ox}}{\epsilon_{si}}$, (26)
where $\psi_s(x)$ is the surface potential at $y = 0$ and $y = T.sc$ which is defined as follows

$$\psi_s(x) = \eta \exp(\delta x) + \zeta \exp(-\delta x) + \lambda,$$  \hspace{1cm} (27)

$$\delta = \sqrt{\frac{2C_{ox}}{\epsilon_s T.sc}},$$  \hspace{1cm} (28)

$$\lambda = V_{gate(eff)} - \Delta \phi_{ms} + \frac{qN_D}{\delta^2 \epsilon_s},$$  \hspace{1cm} (29)

$$\zeta = -\lambda \frac{\exp(\delta L_g) - 1}{2 \sinh(\delta L_g)},$$  \hspace{1cm} (30)

$$\eta = -\zeta - \lambda,$$  \hspace{1cm} (31)

By introducing the surface potential from equation (27) in (9), the total charge density in the channel (which is a function of $V_{DS}$) becomes

$$Q_{sc} = -2C_{ox} \left\{ V_{gate(eff)} - \Delta \phi_{ms} ight. - \left\{ \eta \exp(\delta x) + \zeta \exp(-\delta x) + \lambda \right\},$$  \hspace{1cm} (32)

Finally, the total charge density in the ferroelectric can be obtained by substituting (32) in (16) and calculating the integral along the lateral direction of the channel from 0 to $L_g$:

$$Q = \frac{C_{ox}}{L_g} \left\{ V_{gate(eff)} - \Delta \phi_{ms} - \lambda \right\} L_g$$

$$- \left\{ \eta \frac{\exp(\delta L_g)}{\delta} - \frac{\zeta}{\delta} \exp(-\delta L_g) + \frac{\zeta - \eta}{\delta} \right\},$$  \hspace{1cm} (33)

Since $Q$ is a function of the drain voltage, we can estimate how much $V_{DS}$ affects the charge density of ferroelectric. Therefore, we define $\Delta Q = Q_h - Q_l$ as the difference in the charge density of ferroelectric between high and low $V_{DS}$:

$$\Delta Q = \frac{-2C_{ox} \Delta V_{DS}}{2L_g \delta \sinh(\delta L_g)} \left[ \cosh(\delta L_g) \right],$$  \hspace{1cm} (34)

where $\Delta V_{DS} = V_{DS(high)} - V_{DS(low)}$.

To find $\Delta V_f$, the difference of the electrostatic potential across the ferroelectric at high and low $V_{DS}$, we neglect the coefficient $\gamma$. Hence, $\Delta V_f$ becomes

$$\Delta V_f = (2\alpha f Q_h + 4\beta f Q_h^3) - (2\alpha f Q_l + 4\beta f Q_l^3),$$  \hspace{1cm} (35)

which can be further simplified

$$\Delta V_f = 2\alpha f \Delta Q + 4\beta f \Delta Q^3 + 12\beta f \Delta Q^3 Q_h Q_l.$$  \hspace{1cm} (36)

It happens that $Q_h$ and $Q_l$ are the only contributions to $\Delta V_f$ that depend on the applied gate voltage. Still, it happens that the last term in (36) containing these quantities is negligible, meaning that we can approximate $\Delta V_f$ as follows

$$\Delta V_f \approx 2\alpha f \Delta Q + 4\beta f \Delta Q^3.$$  \hspace{1cm} (37)

Fig. 4 depicts $\Delta V_f$ and $\Delta Q$ versus the channel length on the left and right axis respectively. We see that the absolute value of $\Delta Q$ increases by going to the shorter channel lengths, and as a result, $\Delta V_f$ increases as well. This is an advantage because it predicts that negative capacitance mitigates short channel effect at high $V_{DS}$. Actually $\Delta V_f$ represents somehow $\Delta V_G$, i.e. the difference of $V_G$ between high and low $V_{DS}$.

The schematic drawing in the inset of Fig. 4 illustrates this improvement. It compares the I-V characteristic of a regular double gate JLFET and a double gate JLFET with negative capacitance. As we mentioned in the previous section, a negative capacitance causes a potential amplification as much as $V_f$. Although $V_f$ is almost the same for high and low $V_{DS}$ for the long channel device, it becomes less effective at low $V_{DS}$ in regard to high $V_{DS}$ for a short channel device. In fact, in presence of short channel effect, the I-V characteristic that shifts towards high $V_{DS}$ is compensated by $\Delta V_f$ in NCDG JLFET, thus improves short channel effect in presence of negative capacitance. Although the model is developed for long channels, it is scalable to below 50 nm as it appears from Fig. 4.

IV. CONCLUSION

An analytical charge-based model for symmetric double-gate junctionless FETs with negative capacitance was developed. The model incorporates the impact of the negative capacitance of ferroelectric on DC electrical characteristics of double gate JLFETs by proposing an analytical and explicit equation for the total charge density of ferroelectric in depletion and accumulation modes. The model confirms that using the negative capacitance in junctionless transistors means that the gate overdrive voltage decreases, which can be interpreted as lower energy consumption. The model also shows that the subthreshold slope almost remains constant in NCDG JLFET, but an improvement of swing for above the threshold causes a significant enhancement in ON current. Actually, in junctionless with NC, we gain ON current improvement by a factor of 6 in comparison to junctionless FET. In addition, an analysis on the short channel effect predicts an improvement when negative capacitance is observed. The model has been compared to TCAD simulations with an excellent agreement in all regions of operation from deep depletion to accumulation and linear to saturation.
V. APPENDIX

The total polarization $P$ can be expressed as the sum of a linear and switching dipole $P_D$ contributions as follows [26]

$$P = \varepsilon_0 \chi E + P_D. \quad (38)$$

Hence, the surface charge density $\sigma$ of ferroelectric becomes

$$\sigma = V \frac{\varepsilon_f}{t_f} + P_D, \quad (39)$$

where $\varepsilon_f = \varepsilon_0 (1 + \chi)$. Thus the capacitance becomes

$$C = \frac{d\sigma}{dV} = \frac{1}{t_f} \left( \varepsilon_f + t_f \frac{dP_D}{dE} \right). \quad (40)$$

We can replace $dV$ with $t_f dE$ and then $dP_D/dE = dP/dE - \varepsilon_0 \chi$. Therefore, the capacitance is related to the slope of the $P$-E curve as expressed in (4).

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