A Fresh Perspective on DNN Accelerators by Performing Holistic Analysis Across Paradigms

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ABSTRACT

Traditional computers with von Neumann architecture are unable to meet the latency and scalability challenges of Deep Neural Network (DNN) workloads. Various DNN accelerators based on Conventional compute Hardware Accelerator (CHA), Near-Data-Processing (NDP) and Processing-in-Memory (PIM) paradigms have been proposed to meet these challenges. Our goal in this work is to perform a rigorous comparison among the state-of-the-art accelerators from DNN accelerator paradigms, we have used unique layers from MobileNet, ResNet, BERT, and DLRM of MLPerf Inference benchmark for our analysis. The detailed models are based on hardware-realized state-of-the-art designs. We observe that for memory-intensive Fully Connected Layer (FCL) DNNs, NDP based accelerator is $10.6 \times$ faster than the state-of-the-art CHA and $39.9 \times$ faster than PIM based accelerator for inferencing. For compute-intensive image classification and object detection DNNs, the state-of-the-art CHA is $\sim 10 \times$ faster than NDP and $\sim 2000 \times$ faster than the PIM-based accelerator for inferencing. PIM-based accelerators are suitable for DNN applications where energy is a constraint ($\sim 2.7 \times$ and $\sim 21 \times$ lower energy for CNN and FCL applications, respectively, than conventional ASIC systems). Further, we identify architectural changes (such as increasing memory bandwidth, buffer reorganization) that can increase throughput (up to linear increase) and lower energy (up to linear decrease) for ML applications with a detailed sensitivity analysis of relevant components in CHA, NDP and PIM based accelerators.

Keywords neural networks, hardware accelerators, processing-in-memory

1 Introduction

Deep Neural Networks (DNN) have evolved to do image classification, object detection, language processing, and recommendation tasks in mobile, edge, and datacenter applications [1]. These applications have specific latency and energy constraints based on the scenarios where these applications are deployed [2]. Since traditional computers with von Neumann architecture are not suitable for meeting these constraints, various DNN accelerator architecture paradigms have been proposed [3,4,5,6,7,8]. As shown in Fig. 1, they can be broadly classified into Conventional Hardware Accelerators (CHA) [6,7], Near Data Processors (NDP) [5,7], and Processing in Memory (PIM) Accelerators [4,8]. Application-specific integrated circuit (ASIC) based CHA DNN accelerators are designed to provide fast compute capability with the help of operation specific circuits but are limited by DRAM interface bandwidth due to limited pin out count [7]. Simba [6], as shown in Fig. 1a is a hardware realized example of CHA. An alternative to CHA, PIM-based accelerators are proposed to overcome the memory bandwidth bottleneck. Commercial PIM based accelerators use 2D DRAM process to fabricate compute elements on the same chip as memory. However, they are limited to simple core designs without dedicated single cycle hardware multipliers due to the DRAM fabrication process [7,8]. Fig. 1e shows UpMem [4], a state-of-the-art PIM based accelerator. NDP-based DNN accelerator architectures, which reduce data movement costs by placing compute capability close to memory, are a middle ground between the other two
architectures [7]. NDP accelerators based on 3D-stacked memory integrate DRAM layers with a logic layer which consists of processing elements. Still, the logic layer has area and thermal constraints, limiting the capabilities of processing components. Tetris [5], shown in Fig. 1c, is such an NDP architecture. While such a varying range of architectures exist, there is no works which performs in-depth comparisons among these three architectural paradigms. Traditionally the existing works have limit the comparison of DNN accelerators against CPUs and GPUs.

To the best of our knowledge this is the first work where in-depth analysis and comparison has been done among these three paradigms. We identify the DNN architectural paradigm suitable for different ML workloads by detailed architectural analysis, for different scenarios where latency, throughput, or energy efficiency are essential. Further, we identify changes that can be made to the components of each architectural paradigm to improve latency and energy efficiency for ML workloads by carrying out sensitivity analysis. We also identify the upper limits of performance for each of these architectural paradigms to identify possible future designs. The leading five aspects of this novel work that compared multiple paradigms are as follows.

First, we model representative architectures based on state-of-the-art Simba, Tetris and UpMem architectures to represent CHA, NDP and PIM DNN accelerator paradigms based on a survey of each paradigm space, respectively. Second, we use the latency, bandwidth and energy measurements of components from realized hardware architectures as inputs to the model, for a realistic comparison. This helps account for form factors and fabrication process limitations associated with each paradigm. Third, we use DNN layers from MLPerf [1] to benchmark and identify the suitability of each architecture for different real-world applications under their respective latency and energy constraints. Fourth, a detailed architectural cost model (based on Simba, Tetris, and UpMem) is used for each architecture, which considers the spatial and temporal data flow constraints between each component of the accelerator and its energy consumption. Further, the optimum mapping of the DNN to the detailed model, for least latency and energy consumption, is used for comparison. Fifth, we perform sensitivity analysis on the detailed model to find architectural changes that benefit each application.

The main contributions of this work are:

- We provide the first realistic and detailed comparison of state-of-the-art conventional, NDP and PIM DNN accelerator paradigms for their suitability for processing DNN applications. The models used in this work are based on hardware-realized designs.
- Data-Reuse (DR) of a DNN layer represents the number of times a word of input data participates in multiply-accumulate (MAC) operations. We show that for DNN applications with low data reuse, such as language and recommendation tasks, NDP architecture is \( \sim 10 \times \) and \( \sim 39 \times \) faster for inferencing than CHA and PIM architectures, respectively.
- CHA has \( \sim 10 \times \) and \( \sim 2000 \times \) lower latency than NDP and PIM architectures, respectively, for inferencing DNN applications with high DR (\( \sim 100 \) MACs/word) such as object detection and image classification. Because CHA architecture can supply required data to a vast number of fast MAC units from its internal buffer without being affected by the narrow bandwidth between the accelerator and memory for such applications.
- For applications with constraints on energy, such as mobile applications, PIM paradigm is better as it consumes the least energy (\( \sim 2.7 \times \) and \( \sim 21 \times \) less than CHA for Convolutional Neural Networks (CNN) and Fully Connected Layer (FCL) applications respectively) for DNNs. This is because energy for data transfer from memory to MAC units is significantly less than other considered architectures.
- We identify architectural changes that can increase throughput, decrease latency and lower energy for ML applications with sensitivity analysis. Batching is universally beneficial for CHA in terms of throughput and energy, at the cost of slightly increased latency. However, we identify that batching can adversely affect BERT and DLRM in NDP architectures.
and PIM systems. An increase in last-level-memory bandwidth can decrease the latency of CHA by 20% for CNN applications and linearly increase performance for FCL applications.

- Further, by sensitivity analysis, the following observations are made. (i) NDP can be redesigned to be 3× faster than CHA for CNN applications, thus making it the fastest paradigm for both CNN and FCL workloads. (ii) PIM is not suitable for CNN workloads when latency is the primary concern. (iii) PIM, with design changes, is more suitable for FCL workloads than CHA.

2 Background: Software for DNNs

Deep Neural Networks (DNNs) can be broadly classified into artificial neural networks and spiking neural networks. These DNNs usually have two phases, namely training and inference. In this work we analyze the design of accelerators used during the inference phase of the artificial neural networks. We have focused on inference as training, in general, is done infrequently. Inference, on the other hand, is done every time the application needs to perform a task. Also, latency, throughput energy, or power constraints are usually tighter for inference application scenarios than training, which require specialized hardware accelerators [3]. The background related to the design of DNNs and the accelerators for these DNNs are discussed in the next sections.

2.1 Inference

In DNNs, inference is performed by passing a high-dimensional input through a parameterized function. This parameterized function can be represented as a stack of neural network layers as shown in Eq. 1.

\[ f(x) = f_{l-1} \circ f_{l-2} \circ \ldots \circ f_2 \circ f_1(x) \]  

(1)

Here \( x \) represents the high dimensional input. Each of the functions \( (f_1, f_2, \ldots, f_{l-1}) \) form a layer, and the output of each layer is passed only to the next layer in a uni-directional manner forming a network. Processing these layers on a traditional computer with general purpose CPU based on von Neumann architecture involves huge volumes of data transfer between the processor and the off-chip memory due to large network size and high number of memory accesses [3]. This limits the system’s performance and increases the energy consumption during inference, making traditional systems highly inefficient for performing inference using DNNs. Furthermore, traditional systems suffer from two physical limitations as follows. (i) Due to the existing memory wall [9], where the processor’s latency being much lower and internal bandwidth being higher than memory’s latency, memory is unable to transfer sufficient data in time to the processing units. Hence the processing unit’s utilization is significantly reduced, leading to lower performance. (ii) Traditional systems have complicated sub-units (modules of out-of-order core) which lead to significant power consumption, making them inefficient at processing DNNs. High power dissipation due to the power wall [10], i.e., comparable leakage and dynamic power in lower technology nodes, further put a limit on the performance of these processing units. These limitations have led to the shift away from traditional systems to the development of accelerators tailored toward DNNs [3]. These accelerators have orders-of-magnitude higher performance and power efficiency as compared to traditional computer systems [6]. They mitigate the issues related to bottlenecks of traditional systems and also successfully exploit the deterministic flow of data in DNNs [11].

DNNs can have different types of layers such as Fully Connected Layer (FCL), Convolutional Layer (CL), ReLU, sigmoid, max pooling, and batch normalization layers. In state-of-the-art DNNs, FCL and CL account for over 90% of the operations [3]. Hence, most DNN accelerator designs are targeted towards accelerating these layers [3]. In this work, we have also focused on FCL and the CL of the DNNs.

\[ \text{out}_{b,o} = \sum_{i,c=0}^{L-1} \text{in}_{b,i,c} \times \text{weight}_{i,c,o} \]  

(2)

A FCL performs matrix multiplication and can be represented as Eq. 2 and Fig. 2a where \( I, O, \) and \( B \) denote the number of input channels, number of output channels, and batch size (number of separate inputs that are being processed together), respectively. Further, in the equation, \( i, o, \) and \( b \) denote the index of input channels, output channels, and batch, respectively. Similarly, a CL can be represented by the Eq. 3 and Fig. 2b where \( F_h \) and \( F_w \) are the height and width of the filter, \( i \) and \( j \) represent the row and column index of an element in the filter, \( x \) and \( y \) represent the index of an element in the feature map. Contrary to FCL, in CL, the filter is slid across the input and element-wise multiplied and accumulated to generate the output, as shown in Fig. 2b. For CL and FCL, the inputs are reused for all output channels, and weights are reused for all input batches. This data reuse is also an important property that is exploited in the DNN accelerator designs to make them efficient.
2.2 Inference Benchmark

There are a number of DNNs that have been proposed in the past decade. To effectively capture the state-of-the-art DNNs, the benchmark networks adopted in MLPerf Inference benchmark have been used in this work. MLPerf Inference benchmark is a benchmark suite made up of workloads that are reflective of real-world applications [1]. Since our goal in this work is to perform a rigorous comparison among the state-of-the-art accelerators, we have used unique layers from MobileNet [12], ResNet [13], BERT [14], and DLRM [15] of MLPerf Inference benchmark for our analysis.

MobileNet (MN) is designed for mobile and embedded vision applications and is designed for energy efficiency. ResNet (RN) is designed to be efficient when training with a deeper number of layers by alleviating the issues related to vanishing gradients using skip connections [13]. ResNet has improved object detection accuracy due to its extreme deep representations. BERT is a language representation model with applications in various tasks such as question answering and language inference. DLRM is used for recommendation tasks. The 27 unique layers have been taken from these networks as shown in Table 1. The index numbers and corresponding layers belonging to each NN used in this work are also shown. The table also shows the reuse potential of input and filter data words. DNN accelerators heavily exploit this data reuse by caching operands to reduce bottlenecks due to memory wall and improve energy efficiency [3]. Further, layer volume provides the minimum number of words of the NN layer that have to be moved between main memory and the compute units when the NN is processed in a layer by layer manner. In a pipelined setup with multiple tiled regions for compute, layer volume is the number of words that needs to transferred to the next region [6]. Minimum data transfer is achieved when using data-stationary approaches where either the entire input, filter, or output is kept on-chip during the computation being done by a layer. Input volume and Filter volume of a layer denote the minimum required size of the on-chip buffers to implement input and filter stationary approaches of computing, respectively. In the following section, the design of different accelerator types and details related to data reuse have been explained.
Table 1: Index of unique layers of MobileNet, ResNet, BERT and DLRM

| Index | Input shape | Filter shape | Input word | Filter word | Layer word | Input volume | Filter volume |
|-------|-------------|--------------|------------|-------------|-------------|--------------|--------------|
|       |             |              | reuse      | reuse       | (words)     | (words)      | (words)      |
|       |             |              | count      | count       |             |              |              |

**MobileNet (Convolutional layers)**

| Layer | Volume | Input volume | Filter volume |
|-------|--------|--------------|---------------|
| 1     | 224x224x3 | 3x3, 32 | 72 | 12544 | 552800 | 150528 | 864 |
| 2     | 112x112x32 | 1x1, 64 | 64 | 12544 | 1206272 | 401408 | 2048 |
| 3     | 56x56x64 | 1x1, 128 | 128 | 3136 | 610304 | 200704 | 8192 |
| 4     | 56x56x128 | 1x1, 128 | 128 | 3136 | 819200 | 401408 | 16384 |
| 5     | 28x28x128 | 1x1, 256 | 256 | 784 | 333824 | 100352 | 32768 |
| 6     | 28x28x256 | 1x1, 256 | 256 | 784 | 466944 | 200704 | 65536 |
| 7     | 14x14x256 | 1x1, 512 | 512 | 196 | 281600 | 50176 | 131072 |
| 8     | 14x14x512 | 1x1, 512 | 512 | 196 | 462848 | 100352 | 262144 |
| 9     | 7x7x512 | 1x1, 1024 | 1024 | 49 | 599552 | 25088 | 524288 |
| 10    | 7x7x1024 | 1x1, 1024 | 1024 | 49 | 1148928 | 50176 | 1048576 |

**ResNet (Convolutional layers)**

| Layer | Volume | Input volume | Filter volume |
|-------|--------|--------------|---------------|
| 1     | 224x224x3 | 7x7, 64 | 784 | 12544 | 962752 | 150528 | 9408 |
| 2     | 56x56x256 | 1x1, 64 | 64 | 3136 | 1019904 | 802816 | 16384 |
| 3     | 56x56x64 | 3x3, 64 | 576 | 3136 | 438272 | 200704 | 36864 |
| 4     | 56x56x64 | 1x1, 128 | 128 | 3136 | 1019904 | 200704 | 16384 |
| 5     | 28x28x512 | 1x1, 128 | 128 | 784 | 567296 | 401408 | 65536 |
| 6     | 28x28x128 | 3x3, 128 | 1152 | 784 | 348160 | 100352 | 147456 |
| 7     | 28x28x128 | 1x1, 512 | 512 | 784 | 567296 | 100352 | 65536 |
| 8     | 14x14x1024 | 1x1, 256 | 256 | 196 | 513024 | 200704 | 262144 |
| 9     | 14x14x256 | 3x3, 256 | 2304 | 196 | 690176 | 50176 | 589824 |
| 10    | 14x14x256 | 1x1, 1024 | 1024 | 196 | 513024 | 50176 | 262144 |
| 11    | 7x7x2048 | 1x1, 512 | 512 | 49 | 1174016 | 100352 | 1048576 |
| 12    | 7x7x512 | 3x3, 512 | 4608 | 49 | 2409472 | 25088 | 2359296 |
| 13    | 7x7x512 | 1x1, 2048 | 2048 | 49 | 1174016 | 25088 | 1048576 |

**BERT (Fully connected layers)**

| Layer | Volume | Input volume | Filter volume |
|-------|--------|--------------|---------------|
| 1     | 1024x1 | 1024x1024 | 1024 | 1 | 1049600 | 1024 | 1048576 |
| 2     | 4096x1 | 4096x4096 | 1024 | 1 | 4198400 | 4096 | 4194304 |
| 3     | 1024x1 | 4096x1024 | 4096 | 1 | 4195328 | 1024 | 4194304 |

**DLRM (Fully connected layer)**

| Layer | Volume | Input volume | Filter volume |
|-------|--------|--------------|---------------|
| 1     | 256x1 | 512x256 | 512 | 1 | 131328 | 256 | 131072 |
3 Background: Hardware for DNNs

Traditional von Neumann computers have limits on system performance and energy efficiency when processing DNN applications. Also, most DNN applications have strict latency requirements, and traditional von Neumann computers cannot meet these requirements [3]. Further, traditional von Neumann computers are made up of separate processor and off-chip memory components [16]. Because of this separation, it takes \( \sim 200 \times \) more energy to transport operands of an instruction from memory to the processor than the actual computation [16][4]. These limits have led to the development of computing platforms dedicated to processing DNN applications.

Contemporary DNNs have 10 to 200 million compute operations per layer, as seen in Table 1. A large fraction of these compute operations can be performed in parallel due to minimal data dependency between the output data words. This idea is heavily exploited in the design of DNN accelerators. Over the years, many accelerators designs have been proposed for DNNs. Early designs [17][18] were on-chip co-processors with limited compute capabilities. Conventional standalone DNN accelerators [19][6] are being designed with an understanding of the workloads where data flow is analyzed and utilized to reduce off-chip accesses and increase system performance and efficiency. We classify these as Conventional Hardware Accelerators (CHA). CHAs have massively parallel compute units that allow hundreds of Multiply-Accumulation (MAC) operations per cycle [6]. However, these CHAs still suffer from the limitation of fetching data from off-chip memory, which is an energy-intensive operation.

To overcome these limitations, accelerators have been proposed which perform computations either near or in-memory, i.e., the computations are closely coupled to memory, alleviating the issue of off-chip memory accesses. We classify these accelerators as non-conventional hardware accelerators (NHAs) [5][4]. NHAs are further subdivided into two categories.

The first type, such as [4] employs digital compute circuitry near the row buffers of 2D memory to minimize data movement. However, this architecture is limited to simple logic designs owing to the limited number of metal layers available in the process [20]. The second type, such as [5], exploits vertical integration of DRAM, and logic dies of 3D memories by placing the compute elements in logic dies. Accelerators, such as [21][22], utilize memory cells to perform computations using analog properties. In this work, we limit ourselves to the first two categories, namely CHAs and NHAs based on 2D and 3D memory.

3.1 Conventional Accelerators

Conventional hardware accelerators are either standalone systems or part of a general-purpose host system. In either case, the Last-Level-Memory (LLM) used is the traditional DDR DRAM, and the chips housing the MAC units are designed specifically for a set of DNN applications. Hence, these systems are primarily bottlenecked due to the memory wall [3]. For these systems, it is essential to exploit the data reuse potential of NN applications to reduce off-chip data transfers. As shown in Fig. 3, these systems use large on-chip buffers to hold the inputs, intermediate outputs, and filters while fast processing elements (PEs) perform computations using these data. A Network-on-chip (NoC) helps data transfer among PEs. Techniques such as multi-casting are used to deliver required data to all the PEs in parallel if needed [16][6]. PEs have local buffers to reduce traffic on NoCs and also have specialized Multiply-Accumulate (MAC) structures to perform operations in DNN. The spatial arrangement of PEs allows for the splitting of the these operations by input and output channels across different PEs. While there are a number of CHAs [23][11][16][24][25][26][27][28], in this work, we have used the state-of-the-art, hardware realized Simba accelerator as a representative architecture for CHAs.

3.1.1 SIMBA

Simba [6] is a highly scalable chipset-based architecture with the baseline system consisting of one chiplet. The chiplet consists of resources for inter-chiplet communication, a Global Buffer, an array of 16 PEs connected together using an NoC and a RISC-V processor (RVP) to co-ordinate the compute tasks, as shown in Fig. 3. Each PE has a router interface, and buffers for weights (filters), input, and output (Accumulation Buffer). Further, each PE has eight vector MACs, and each vector MAC is capable of Multiplying and accumulating eight input words with eight weight words to form a single output word. The Accumulation Buffer, with the help of separate accumulators, accumulates current results with previous partial results stored in the Accumulation Buffer. Results transferred from other PEs over the NoC can also be accumulated. The generated output is then post-processed (ReLU, Pooling, Scaling) or directly transferred out of the PE via the NoC.
3.2 Non Conventional Hardware Accelerators

Conventional applications have dynamic paths for execution and require techniques such as branch predictors and
prefetchers to improve performance. However, most DNN applications have a pre-determined fixed pattern for
computing. The DNN applications can be decomposed into simple parallel operations that can be performed using
simple compute units in a deterministic manner \[^2\]. Further, the throughput can be increased by performing these
simple compute operations in parallel. However, a DNN accelerator system having separate off-chip memory and
compute units still introduces scalability challenges due low bandwidth and high data access energy of off-chip memory.
Hence NHAs were introduced to overcome this limitation. In most NHAs, the memory and the compute units are
tightly integrated, alleviating the issue of memory wall due to the high internal bandwidth. NHAs can further be
sub-categorized into two categories:
3.2.1 3D Memory - NDP

Fig. 1c shows Tetris [5], a state-of-the-art 3D memory-based DNN accelerator. In Tetris, the memory dies of the Hybrid-Memory-Cube (HMC) are stacked on top of the logic layer. The dies are spatially split into sixteen parts, as shown in the figure, and the parts that are stacked on top of each other are connected via through-silicon vias (TSVs) to form a vault. Each vault operates independently and contains a separate memory controller on the logic die. In an HMC, each vault has $3.5 \text{ mm}^2$ of unused area in the logic layer, this area is utilized for dedicated compute units and associated resources such as buffers for performing DNN acceleration in Tetris. As shown in Fig. 4a, each vault has a single instance of an accelerator with its own global buffer and PE array. The data stored in the same vault is fetched with the help of the memory controller, while data stored in another vault has to be fetched over the inter-vault router. Since the computation is performed separately to memory die and the compute sites are near where data resides, this paradigm is known as Near-Data-Processing (NDP).

This category of NHA uses 3D memory, and for this work, we have used Tetris [5], which is the state-of-art 3D memory-based accelerator for DNNs, for our analysis.

3.2.2 2D Memory - PIM

Fig. 1e shows an abstract hardware model of UpMem, a state-of-the-art 2D memory-based DNN accelerator. UpMem is designed to work alongside a host system where the UpMem DIMMs act as both regular memory and compute accelerators. The DIMMs are constructed of PIM chips, as shown in Fig. 4b. Each PIM chip has memory arrays that are connected to the host via a standard DDR interface. Further, each PIM chip has a small local buffer and dedicated compute units with access to memory arrays over DMA. This arrangement provides large bandwidth to the compute units. However, inter-chip communication still relies on the standard DDR interface and is costly in terms of latency and energy.

To get insights into the different accelerators, we will compare Simba, Tetris, and UpMem. A detailed and quantified comparison of the architectural parameters for each of these is given in Section 6. In the next section, we discuss the evaluation setup used to compare the architectures.

4 Representative models for DNN accelerator paradigms

A fine-grained analysis of all DNN accelerators belonging to CHA, NDP, and PIM is beyond the scope of this work. Hence we construct representative models for each paradigm with the best in class parameters from data-agnostic works. In data-agnostic processing of NN, the actual value of inputs do not change the inference time. Further, the parameters are measured only from hardware-based works. Furthermore, for the spatial organization of the components representing each paradigm, we use Simba, Tetris and UpMem for CHA, NDP and PIM. They are state-of-the-art hardware-based designs, and hence the architectural parameters inscribing the aspects are constrained by the real-world characteristics of each paradigm. Further, Simba, Tetris and UpMem are data-agnostic designs with the most best in class parameters as compared to other relevant works in each paradigm, as shown in Table 2 hence are good representatives of the paradigm space.

### Table 2: Representative hardware accelerators and relevant related works from each paradigm

| Representative Accelerator | Simba [6] (CHA) | Tetris [5] (NDP) | UpMem [4] (PIM) |
|----------------------------|----------------|-----------------|----------------|
| Related works              | [23,11,16,24,25,26,27,28] | [29,30,31,32,33] | [34,35,7,36,37,38,39] |

4.1 Architectural parameters

For an accurate evaluation of DNN architectures, Oliveira et al. [7] and Gómez-Luna et al. [8] have shown that data storage and data movement bottlenecks must be modeled along with the compute capabilities of the DNN accelerators. Parashar et al. [2] and Wu et al. [40] have shown that mapping a DNN to the DNN accelerator has to be optimized, based on the accelerator’s structure and based on latency and energy aspects of the individual components of the accelerator, to achieve the lowest latency and energy for execution. In this work, the mapping is optimized for least latency followed by least energy, and such a mapping is referred to as optimal mapping. Hence the relevant parameters are as follows. (i) Count and latency of MAC units. (ii) Working memory size (iii) Data bandwidth: bandwidth between different PEs, bandwidth between working memory and PEs, and bandwidth between DRAM and working memory. (iv) MAC compute energy (v) Data access and data transfer energies from each data storage level. The specific values of parameters and their relationships are explained in Section 6.
5 Tools used for Analysis and Experimental Setup

Table 3: Summary of Experiments

| Experiment | Figures |
|------------|---------|
| Baseline – Inference of MobileNet, ResNet, BERT and DLRM | 5a, 5b, 6, 7, 8a, 8b, 9a, 9b |
| Batching – The workload inputs are batched at 1×, 2×, 4× and 8×. | 10a, 10b, 11a, 11b, 12a, 12b, 13a, 13b |
| Last level memory bandwidth – The last level memory bandwidth is increased by 1×, 2× and 4×. | 14a, 14b, 15a, 15b |
| Maximum usable MAC units- The total count of MAC units for each system is increased to 100 thousand. | 19a, 19b, 20 |
| Buffer size and layout- The buffer size of each system is increased to 1×, 2× and 4×. | 16, 17, 18 |

Note: The metrics for comparison are obtained for each experiment where mapping is optimized for least latency followed by least energy for Simba-like, Tetris-like and UpMem-like systems.

The detailed models of the accelerators are implemented based on the designs described in Section 3 and the parameters in Section 6 Timeloop [2], Accelergy [40], and Cacti [41] are used to perform detailed analysis. The per-layer optimal mapping of DNN to hardware is found using Timeloop.

Accelergy and Cacti are used to obtain the area and energy of PEs, SRAM buffers, and DRAM using the 45nm model. When calculating the total energy of DRAM, only the access energy of DRAM is considered for all three models. Based on DNN’s mapping and usage, timing, and energy associated with each accelerator component, the execution time and energy consumption are obtained. The summary of experiments carried out is shown in Table 3.

Timeloop

It allows the modeling of DNN accelerators and finds the optimal mapping of the workload to the accelerator based on user specified optimization criteria such as least latency or energy. The tool provides abstractions for defining compute units, memories across various levels, and communication links. Further, dataflow constraints, bandwidth limitations, and utilization constraints can be placed upon these three elements. The main usage of Timeloop in this work is to provide optimal mappings of DNN layers to architectural models. Timeloop’s mapper constructs mapspace and evaluates the quality of each mapping with the cost model provided by Accelergy. The optimal mapping is obtained using an iterative search in the mapspace based on optimization criteria. The mappings are optimized for least latency followed by least energy in this work [2].

Accelergy

It allows fast and accurate cost modeling, in terms of latency, area and energy, of each of the units present in DNN accelerator hardware. Similar to Timeloop, Accelergy provides abstractions to define compute units and various memory levels. Upon instantiating these abstractions, the corresponding area and energy values are obtained by Accelergy and are used by Timeloop for model mapping. In this work, Accelergy uses external plugins (Cacti and Aladdin[42]) to determine the area and energy of buffers and MACs.

Cacti and Aladdin

Cacti is a tool for modeling the dynamic power, access time, area, and leakage power of caches and other memories. Cacti is used to model the area and energy of buffers and memories in our work, with access time constraints. In this work, the 45 nm model is used and buffer size is based on values from Table 4.

Aladdin allows for specifying scalable compute energy cost per bit.

In the next section, we discuss detailed architectural parameters that have been used for modeling of accelerators.

6 Detailed Architectural Parameters

The values of architectural parameters used in this work are given in Table 4. Dependent energy values are derived from CACTI based on values in Table 4.
Table 4: Summary of architectural constraints

| Metric/Constraint | CHA | NDP | PIM |
|-------------------|-----|-----|-----|
| MAC units         | 1024 [6] | 256 [6, 7] | 128 [4, 8] |
| MAC latency       | 1 ns [6] | 2 ns [5] | 40 ns [4, 8] |
| MAC compute energy| 0.2 pJ/bit [4] | 0.2 pJ/bit [5] | 0.4 pJ/bit [4] |
| Inter-PE bandwidth| 70 GB/s [6] | 16 GB/s [4, 5] | 12.8 GB/s [8] |
| Working memory size| 3 MB [7] | 2 MB [5] | 512 KB [8] |
| Working memory bandwidth| 70 GB/s [6] | 6.4 GB/s [5] | 800 MB/s [8] |
| DRAM-Compute bandwidth| 25.6 GB/s [45] | 16 GB/s per vault [5] | 102 GB/s [8] |
| DRAM-Compute data access energy| 46 pJ/bit [4] | 4.2 pJ/bit [5] | 2.3 pJ/bit [4] |

MAC Unit

The MAC unit consists of circuits used to perform MAC operations and a register file with 16 entries. CHA architecture that we have considered in this study has 1024 MAC units, with each unit operating with a latency of 1 ns. Further, the compute energy is 0.2 pJ/bit. In NDP, MAC units drop to 256, and the latency doubles to 2 ns due to a stricter thermal constraint of 10W and area constraint of 3.5 $mm^2$ per vault. Further, the energy cost per bit of computing is 0.2 pJ/bit. CHA and NDP have similar energy costs for computing regardless of their difference in operating speed as state-of-the-art CHA have fused vector MACs that reduce writes. PIM system has only 128 MAC units across 16 PIM chips, with each MAC operating at a latency of 40 ns. The extreme slowdown is due to the DRAM process used for the MACs. Further, energy cost per bit also doubled to 0.4 pJ/bit due to the same reason. In CHA, the MAC count is limited by the available memory bandwidth, while in NDP and PIM, thermal, area, and process constraints limit the MAC count.

Working Memory

All three paradigms have working memory to avoid redundant data fetches to the LLM. In CHA, the working memory is formed by the global buffer and the local buffers at each PE. However, due to relatively smaller configuration, NDP and PIM have only one buffer acting as the working memory between MAC units and the last-level-memory. Due to its memory bandwidth constraint and relaxed area constraints, CHA systems have large buffers (3 MB combined) to exploit the data-reuse potential of the workload. On the other hand, NDP and PIM systems have smaller buffers (2 MB and 512 KB, respectively) due to high bandwidth and relatively low access energy at the last-level memory.

7 Metrics for Evaluation

Architectures for ML inference operate under different operational scenarios and can be compared using various metrics. Real-time ML applications operate in a single-stream scenario where each input needs to be processed, and decisions based on it need to be taken before processing the following input. In multi-stream scenario, the objective is to handle as many parallel streams as possible without breaking the latency constraints required by the application. Surveillance cameras and sensor data processing in autonomous vehicles are excellent examples of this scenario. In the offline scenario, the throughput of processing inputs is more important than the latency constraint and assumes that all the inputs are available from the start. Hence in this scenario, power is more important than energy. Server scenario assumes the server setting where inputs arrive for inference at various rates. Therefore, the requests for processing the inputs will come at different times, creating a hybrid scenario between multi-stream and offline. Here the requests follow a Poisson distribution.

MLPerf utilizes mainly three metrics for performance comparison. (i) Latency: It measures the time it takes for an input to be fully inferenced. In our work, we measure the latency of each unique layer in different ML workloads in wall clock time (ns). Layer-wise measurement helps increase the coverage of ML workloads in MLPerf, as they are constructed of these unique layers in various combinations. The latency of each workload can be calculated by adding up the individual layer latencies. (ii) Throughput: it is measured as layers per second in this work as batching is performed at layer level [6]. Measuring throughput is especially important for offline settings when multiple inputs are
available for processing in parallel. (iii) Energy: MLPerf uses system energy per stream as a metric for comparing energy efficiency of systems. Latency and energy can be used to derive power values.

Apart from these metrics, ML accelerator designers are interested in the utilization ratio of all available MACs. This ratio informs the designer to understand compute resource requirements when processing each layer and how the architecture can be modified to suit the application better.

8 Evaluation Results

In this section we discuss the detailed analysis and comparisons across the three different architectures. The layer shapes respective to the index used in the Figures are given in Table 1.

8.1 Convolutional Neural Network (CNN)

In Fig. 5a, the average time taken by various architectures to process each layer of MobileNet (MN) and ResNet (RN) is shown. On average, CHA is $11 \times$ and $2029 \times$ faster as compared to NDP and PIM for MobileNet. Also, CHA is $13 \times$ and $2272 \times$ faster as compared to NDP and PIM for ResNet. For latency-sensitive ML vision applications that use CNN, CHA is preferable over NDP and PIM. This makes CHA ideal for use in the single stream scenario where queries are generated sequentially and the 90\(^{th}\) percentile latency is the biggest concern. It also makes it suitable for use in multi stream scenario as it can incorporate more streams for a given latency bound. This performance gap further increases for the initial and the final layers. CHA becomes $21 \times$ and $5600 \times$ faster as compared to NDP and PIM for these layers. This variance is due to the skewed shape of these initial and final layers, making it less optimal to map the layers to the distributed architecture of NHAs. The performance gap can be attributed to three main factors. (i) Latency and the number of parallel MAC operations - CHA and NDP can complete 320 and 40 MAC operations in the time PIM performs 1 MAC operation. (ii) CHA has only $1/10^{10}$th bandwidth of the NHAs, but data reuse in CHA is better.
exploited using the large on-chip buffer to compensate for the limited bandwidth, as shown in Section 9.4. (iii) Due to the monolithic spatial architecture of CHA, it allows for higher utilization even with a batch size of one. As compared to NDP and PIM, CHA is able to better utilize its MAC units by 4% and 17% respectively, as shown in Fig. 5b.

Fig. 6 shows the total energy consumed in each layer of MobileNet and ResNet, respectively. Fig. 7 show the split of energy consumed by individual parts of the system per computation. PIM is the most energy-efficient among all designs. This can be largely attributed to no off-chip communication required for PIM. PIM consumes 1.7× and 3.6× lower energy than NDP and CHA for MobileNet. In CHA and NDP architectures, the data access to the LLM accounts for 73% and 60% of the total compute energy, while LLM access energy is only 27% of the total energy per compute in PIM. CHA consumes the highest energy due to off-chip memory accesses. In NDP, the last level memory access energy is 2× more than that of PIM. This can be attributed to the TSVs used in NDP which are not present in PIM.

For ResNet, the difference in energy per compute for CHA and NDP narrows to 1.6× and 1.9×, respectively, compared to PIM. For CHA, due to the higher reuse potential of ResNet compared to MobileNet, as shown in Table 1, the number of LLM access is halved. Irrespective of this, the buffer energy consumption is quite large. NDP is not able to translate the higher data reuse potential of ResNet due to smaller buffers and distributed architecture, leading to higher energy consumption.

In the next section, we discuss the analysis done for fully connected networks.

8.2 Fully Connected Layers (FCL)

Fig. 8a shows the time taken by each FCL of BERT and DLRM, and Fig. 8b shows the MAC utilization of CHA, NDP and PIM for BERT and DLRM. For FCL layers, NDP is 11× and 40× faster than CHA and PIM. Unlike CNN, the data reuse potential is negligible, i.e., 1 compute/data word for FCL - leading to a severe LLM bandwidth bottleneck in CHA. This leads to only 1% MAC utilization as shown in Fig. 8b. Contrary to CHA, in NDP, the utilization is 100% as each vault has sufficient bandwidth to supply the required data to compute logic. Even though each MAC in NDP is working at half the frequency of CHA - the higher number of MACs working together compensates for the lower frequency leading to better performance compared to CHA. PIM has 100% utilization same as NDP, but PIM is 20× slower because the logic in PIM is built using DRAM process, which is inherently slow, as explained in Section 3. Also, for the given area, PIM has only half the number of MACs as compared to NDP due to area constraints determined by the DRAM technology [4, 8]. Thus, for ML applications involving latency-sensitive language and recommendation tasks, NDP has at least 10× speedup than other architectures.

Fig. 9a shows the total energy per layer for BERT and DLRM, and Fig. 9b shows the split up of average energy per compute of BERT and DLRM. PIM is the most efficient among the three architectures in terms of energy. PIM consumes 1.7× and 21× lesser energy as compared to NDP and CHA. CHA consumes 20× more energy to bring data
from main memory to compute units than PIM during inference of FCL. This, along with the higher buffer energy, leads to the $21 \times$ higher energy expenditure in CHA compared to PIM. In PIM, the energy consumed by the MAC unit is twice that of NDP due to the DRAM process. However, the energy to access data from LLM is half compared to NDP. Thus, PIM is at least 40% more energy efficient than other architectures for CNN and FCL ML workloads.

9 Sensitivity Analysis Results

In this section we dive deeper into the individual components of each of these architectures to study their effect on the overall system. This analysis helps us to better understand the resource requirements for designing DNN accelerators. It will also help designers to identify components that need to be improved depending upon the requirements of the accelerator by reducing the design space. The results presented in this section are obtained by averaging the observed values of all the layer of respective workloads.

9.1 Batching of workload for CNN

Batching is a common technique used in many application scenarios within the ML domain where higher throughput is needed. When batched, multiple inputs are processed in parallel rather than sequentially. This parallel processing increases the average latency of processing each layer, however allows for the reuse of weights across multiple inputs. Batching becomes very important for the offline scenario in MLPerf. Offline scenario is for applications where all the data is readily available and there is no strict constraint on latency for single inference. Batching is also important for multi-stream and server applications where throughput is important with additional constraints on latency. Though batching increases throughput, the benefits are not uniform across architectures.

Fig. 10 shows relative latency for inference and relative MAC utilization of CHA, NDP and PIM for MobileNet and ResNet for batch sizes 1, 2, 4, and 8, respectively. We see that as the batch sizes increase by $2 \times$, $4 \times$, and $8 \times$, the
Figure 9: Energy consumed in inferencing BERT and DLRM

(a) Energy consumed by each layer

(b) Breakup of energy per compute

Figure 10: Relative latency of MobileNet and ResNet for batch size of $1 \times$, $2 \times$, $4 \times$ and $8 \times$ on CHA, NDP and PIM

(b) Relative utilization of MAC
latency on average, increases by $1.7 \times$, $3.5 \times$, and $6.8 \times$ as shown in Fig. 10a. However, when doubling the batch size, throughput increases by $13\%$, $8\%$ and $1\%$ for CHA, NDP and PIM, respectively, for MobileNet. Further, ResNet’s throughput increases by $13\%$, $25\%$ and $28\%$ for CHA, NDP and PIM, respectively, when batch size is doubled. This variation across paradigm and workload is due to the following reasons. (i) When examining the shape of layers of CNN workloads, we observe that in MobileNet, $60\%$ of the layers lead to an increase in the number of output channels, while in ResNet, only $30\%$ of the layers lead to an increase in the number of output channels, as shown in Table 1. Hence, ResNet is more symmetric across layers as compared to MobileNet, which leads to better resource utilization, and is, therefore, more suitable for batching, as shown in Fig. 10b. (ii) The distributed architecture of NDP and PIM is not suitable for batching due to variations in sizes across layers.

Further, we observed particular batch sizes work better than others for each paradigm. CHA and PIM have better throughput improvement at a batch size of 8 due to higher utilization of MACs for MobileNet and ResNet as MACs are spatially arranged with 8 MACs on one row and column, which leads to better parallelization. With its 4x4 arrangement, NDP has a better throughput for batch sizes of 4 and 8.

Fig. 11a shows the relative energy when batching MobileNet and ResNet workloads on the accelerators. Further, Fig. 11b shows the split of energy per compute for Fig. 11a. For MobileNet using CHA, batching causes reduction in energy per layer by $10\%$, $10\%$, and $20\%$ for $2 \times$, $4 \times$, and $8 \times$ batching respectively, compared to $12 \times$. For ResNet using CHA, it is $15\%$, $15\%$, and $35\%$ for $2 \times$, $4 \times$, and $8 \times$ batching respectively. The decrease in energy is attributed to decreased last-level memory accesses in CHA due to data reuse.

Contrary to CHA, in NDP and PIM, batching increases the number of memory accesses leading to increase in energy consumption. In the worst case for PIM, the energy consumption can increase up to $2.5 \times$. Hence, for CNN, batching is beneficial for CHA, increasing throughput and decreasing overall energy. But NDP and PIM need to be redesigned with better support for batching as the current buffer to PE ratio leads to larger number of memory access with increase in batch sizes.
9.2 Batching of workload for FCL

When FCL workloads are batched, inputs are processed in parallel, compared to processing them one after the other. In this parallel processing, the weight matrix is reused for each vector input. Figures 12a and 12b show the average latency for inference per layer and the relative MAC utilization, respectively, for BERT and DLRM when batching at 1×, 2×, 4×, and 8×. For FCL layers, there is no improvement in throughput for NDP and PIM as they are already at 100% utilization at 1×, as seen in Fig. 8b. But for CHA, on average, the throughput and utilization increase by 2×, 3.3×, and 5.3× for a batch size of 2×, 4×, and 8×. This is because NDP and PIM have no last-level memory bandwidth bottleneck, whereas CHA is limited by LLM bandwidth bottleneck for FCL. Thus, as data reuse potential increases with batching, CHA can reuse the data across multiple MACs while keeping the number of memory accesses the same, increasing throughput.

Figures 13a and 13b show the relative energy and split up of energy per compute when batching BERT and DLRM workloads on the accelerators. Batching reduces energy requirement per layer by 0.8× and 2× at a batch size of 2× and 4× compared to processing them sequentially for all the architectures. This reduction is due to the amortization of memory access energy across the layers. However, for CHA, at 8× batching, the energy consumption per layer is 7× lower than 1× batch size, but for NDP and PIM, the energy consumption per layer is only 2.7× lower compared to 1× batch size. This is because the optimal mapping for latency bypasses the global buffer in NDP and PIM. At the same time, the registers in the PE are not able to hold all the input and output words till all the operations associated with those words are finished leading to an increase in the number of LLM access. Hence for FCL layers, it is beneficial to batch the inputs for all three accelerators as it considerably decreases energy consumption.

9.3 Last-level-memory bandwidth for CNN and FCL

Figures 14a and 14b show the relative latency and MAC utilization for MobileNet and ResNet workloads with respect to a 2× and 4× increase in the LLM bandwidth, respectively. The baseline LLM bandwidth of each accelerator paradigm is given by the DRAM-Compute bandwidth entry in Table 4. For NDP and PIM, increasing the LLM bandwidth does not improve performance as their performance is not limited by memory bandwidth. For CHA, latency decreases by 20% for MobileNet and 10% for ResNet when the bandwidth is doubled. CHA is able to provide more data for MAC
9.4 Working memory size

Fig. 16b shows the split of energy per compute for CNN workloads when working memory size is increased 2× and 4×, compared to baseline designs. In CHA and NDP, global buffer represents the working memory, as seen in Fig. 1. The working memory of PIM is shown in Fig. 4b. It is observed that increasing working memory size of CHA, NDP, and PIM leads to a negligible change in latency and utilization of MAC, as shown in Fig. 15. However, as the access energy of the buffers has increased, the energy per compute increases. Hence, minimizing the buffer size to the required application will reduce energy requirement.

9.5 Buffer layout

CHAs usually have at least two levels of buffers, one at the global level and one at the PE level (local buffer). The global buffer helps establish chip-level stationary approaches, and local buffers help in partitioning the workload. Some of the workload data is replicated across the PEs based on mapping to facilitate PE level computation. In this analysis, the total buffer size is 3MB, and we partition it across global and local buffers. Fig. 18 shows energy per compute of
Figure 14: Latency and MAC utilization of MobileNet and ResNet for LLM bandwidth = 1×, 2× and 4x

Figure 15: Latency and MAC utilization of BERT and DLRM for LLM bandwidth = 1×, 2× and 4x
MobileNet and ResNet, respectively, on CHA with different buffer partition ratios. For example, in 1:1 configuration 1.5 MB is allocated to both the global buffer and the local buffer distributed across 16 PEs.

We observe that the latency, as shown in Fig. 17, remains same for all configurations except for layer 11 of ResNet. It is observed that the energy value is highest for 2:1 followed by 1:1 and lowest for 1:2 configurations. These changes are due to resultant optimal mapping of the layer to PEs and buffers, reducing the number of reads and writes to the global buffer where the read and write energy is higher.

Fig. 18 shows that the total buffer energy per compute reduces by 10% and 23% for 1:1 and 1:2 configurations compared to 2:1 configurations. This is because the increase in access energy of local buffer compared to the decrease in access energy of global buffer is much smaller. However, the global buffer size to local buffer size ratio cannot be skewed too much, as seen in layer 11 of ResNet. In this layer, there is diminished energy saving for 1:2 configuration compared to other configurations due to more accesses to the local buffer.

9.6 Limits of performance for architecture paradigms.

In this experiment, we relax the area and thermal constraints by increasing the resources available within the DNN accelerator models to gain insight into the impact of resources on various metrics. The LLM bandwidth is kept the same as the baseline design. To identify the maximum number of MACs that can be used per layer, the number of PEs are increased from the baseline such that the total number of MAC units is 100 thousand in the MAX variants of CHA, NDP, and PIM. Fig. 19a shows the maximum MAC units used per layer of MobileNet and ResNet on CHA, NDP, and PIM, while Fig. 19b shows the same data for BERT and DLRM workloads. For MobileNet, half of the layers can use more than 1024 MACs (Baseline), while in ResNet, only 8 out of the 13 layers can use more than baseline. For NDP and PIM, all CNN layers can use more MACs than their respective baselines. The average MACs required per layer for MobileNet during inference are 1100, 6300, 2300 for CHA, NDP, and PIM, respectively. Due to its higher data reuse potential, ResNet has 1777, 8500, and 2100 average MACs per layer requirements for CHA, NDP, and PIM, respectively. This shows that NDP and PIM are extremely compute bottlenecked for CNN-based ML applications, and improving the number of MACs can potentially improve the performance of NDP and PIM.

Figure 16: Latency and Energy of CNN workloads when Global Buffer is increased 1×, 2× and 4x
Figure 17: Latency and energy of MobileNet and BERT on CHA when 3MB of buffer is distributed between global buffer and local buffer.

Figure 18: Per compute energy of MobileNet and BERT on CHA when 3MB of buffer is distributed between global buffer and local buffer.
For FCL layers, with optimal mapping, the total count of MAC units that can be used is limited to 12, 256 and 2100 with the available LLM bandwidth. Hence, for FCL layers, CHA is not compute bottlenecked but is severely LLM bandwidth limited. In NDP, the LLM bandwidth balances the compute requirement in the baseline design for FCL workloads. Hence, additional PEs in the MAX variant are not used. An increase in the average number of MAC units used per layer in the MAX variant of PIM shows that baseline PIM is compute bottlenecked, and future designs should have $16 \times$ more MACs in the PIM chip to balance compute and bandwidth for FCL workloads.

Further, we consider the resultant latency if all compute bottleneck is removed. Fig. 20 shows the latency of baseline design and the MAX variant with the MAC count increased to 100 thousand. There are several key observations. (i) There is no significant increase in performance for MAX CHA as compared to baseline CHA for both CNN and FCL workloads due to LLM bandwidth bottleneck. (ii) For CNN workloads, there is a $50 \times$ speedup for MAX NDP due to high data reuse. Whereas in FCL workloads, there is no latency improvement due to no data reuse. (iii) MAX NDP has $3 \times$ lower latency than MAX CHA, making it the fastest across both workloads. (iv) Compared to baseline PIM, MAX PIM has $120 \times$ and $15 \times$ speedup for CNN and FCL workloads, respectively. The significant difference in speedup is

Figure 19: Maximum MAC units used per layer of CNN and FCL workloads

Figure 20: Comparison of time taken to compute by baseline systems against corresponding MAX variant systems with 100 thousand MAC units for MobileNet, ResNet, BERT and DLRM
due to higher MAC utilization in MAX PIM in CNN because of data reuse. (v) We also observe that MAX PIM has lower latency per layer than MAX CHA for FCL workloads, hence could be a better paradigm for FCL workloads. However, MAX PIM is not better than baseline CHA for CNN workloads.

10 Inferences from the Experiments

In this section, we summarize the significant qualitative findings from the detailed comparison of representative architectures from the three DNN accelerator paradigms when inferencing CNN and FCL workloads. We observe the following. (i) CHA has the least latency per layer for CNN workloads. (ii) NDP has the least latency per layer for FCL workloads. (iii) PIM consumes the least energy for CNN and FCL workloads.

Further, in order to identify how latency and energy characteristics can be improved for each workload on these representative architectures, we performed sensitivity analysis on significant components of the accelerator and found the following. (i) Batching of CNN and FCL workloads can decrease inference energy on CHA, NDP, and PIM. However, NDP and PIM should be redesigned to support larger batch sizes. Otherwise, this could lead to higher energy with larger batch sizes. (ii) Batching of FCL workloads in CHA leads to a linear increase in throughput at a negligible increase in latency of processing each layer as it heavily benefits from data reuse. (iii) Batching FCL workloads on NDP and PIM can be detrimental for latency-sensitive applications because with the increase in batching the latency of the network also increases. (iv) Increasing LLM bandwidth for CHA can linearly decrease latency for FCL applications and would be highly beneficial for latency bound single-stream applications. (v) Total on-chip buffer size can be redistributed, based on workload, between the different buffer hierarchies in CHA to reduce on-chip energy. Further, an increase in on-chip buffer size beyond data reuse requirements leads to higher on-chip energy with no additional benefits.

Additionally, we identified the limits of each paradigm for CNN and FCL workloads to identify future possibilities and found the following. (i) NDP can be redesigned to be the fastest for CNN and FCL workloads by balancing the count of MAC units to the available memory bandwidth. PIM is not suitable for CNN workloads. PIM is more suitable than CHA for FCL workloads.

11 Conclusion

We perform an in-depth analysis of representative state-of-the-art DNN hardware accelerators from Conventional Hardware Accelerator (CHA), Near-Data Processing (NDP), and Processing-in-Memory (PIM) architecture paradigms to identify the fastest and the most energy efficient architecture paradigm for different ML workloads from MLPerf benchmark suite. We identified that CHA, on average, has 7× and 2000× speedup than NDP and PIM for CNN workloads. In comparison, NDP has, on average 10× and 40× speedup than CHA and PIM for workloads with Fully Connected Layers (FCL) such as BERT and DLRM. This inversion is due to the high data reuse potential in CNN workloads, and negligible data reuse potential in FCL, along with the limited bandwidth of the last-level memory. PIM is the most efficient paradigm and consumes 21× and 2.7× lower energy than CHA for CNN and FCL. PIM is also 1.7× more energy efficient than NDP for all DNN workloads. Further, we identified architectural changes that could be made to these representative architectures to make them faster and more energy-efficient by component-wise sensitivity analysis. In these sensitivity analyses, we have identified conditions for a linear increase in throughput with no loss of latency for FCL workloads for CHAs and a near-linear increase in energy efficiency at no loss of throughput for NDP and PIM paradigms. Further, we have quantitatively established that PIM can not be better than CHA for CNN workloads in terms of latency, while PIM could be better for FCL workloads than CHA.

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