Approach to the design of monitoring buffer for read-out ASICs

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Abstract. The paper describes the approach to designing built-in monitoring buffers for the purpose of checking the functionality of ASICs as parts of test printed boards. A figure of merit (FOM), based on that analysis is suggested. Features of the FOM, applied to particle physics experiments, are the speed, power consumption, load driving capability and occupied chip area.

As an example, illustrating the choice of buffer according to the proposed FOM, there are presented the results of designing a buffer version as part of an ASIC for the CBM MUCH(http://www.fair-center.eu/for-users/experiments/cbm.html).

1. Introduction
The important building blocks in the design of both analog and mixed-signal multichannel ASICs for particle physics experiments are the close to rail-to-rail class-AB buffers (voltage followers), having low power consumption, and occupying small area on the chip.

The buffers may be split into two groups according to their destination:
1) internal ones, working on a high resistance and low capacitance load;
2) interface or monitoring ones, working on a low resistance and/or high capacitance external load.

Figure 1. Schematic of presented buffer.
The specificity of the first group is lesser power consumption. Nevertheless greater difficulties for ASIC designers are set by interface buffer, since they require a more thoroughly circuits development in the large signal mode. Namely they are the subject of the given report.

As result of an analysis of literature on low-power high-speed buffers there have been selected and compared the most popular ones. The classical AB-class buffer was used as the reference one (figure 1, 2).

![Figure 2. Layout implementation of the proposed buffer.](image)

2. Figures of merit

Particle physics experiments impose a specific set of requirements for buffer amplifiers, implemented by CMOS of the 180-90 nm levels. The standard requirements, as well as specific ones, are as follows:

1) **Small signal speed** (rise/fall time, settling time at specified accuracy) - nanosecond range
2) **Speed the large signal mode** (slew rate) - not less than 100 mV / ns
3) **Power consumption** - no more than units of milliwatts
4) **Load driving capability** - up to 50 ohm and / or 10 pF (conditions of chip mounting on the read-out board)
5) **Processing at amplitudes**, cover almost the full supply voltage range (rail-to-rail function)
6) **Small area occupied** on ASIC (dictated by channel multiplicity in the created ASIC)

According to standard requirements, the quality of buffer amplifiers may be estimated by the following FOM factors:

1) Actual energy efficiency may be evaluated by the factor

\[
FoM_1 = \frac{I_{\text{imp}}}{I_{\text{supply}}},
\]

where \(I_{\text{imp}}\) - the maximum pulse current through load and \(I_{\text{supply}}\) - the maximum current consumption of the whole buffer.

2) Dynamic performance in the modes of both small and large signals may be evaluated by the factor

\[
FoM_2 = \frac{SRdV}{T_s},
\]
where \( SR \) - slew rate, \( dV \) - the maximum output signal amplitude, at a non-linearity not exceeding a specified level (for example 5 percent), and \( T_s \) - time of settling in the specified tolerance (for example 1 percent).

3) The area efficiency of buffer may be evaluated by the factor

\[
FoM_3 = \frac{C_l}{S},
\]

where \( C_l \) - capacitive load, and \( S \) - area occupied by the buffer on the chip. This factor should be considered at designing the buffers of first group due to the channel multiplicity of ASIC.

As an example, the FoMs calculated for the proposed read-out buffer (Fig.1, Fig.2) are:

1) \( FoM_1 = 31.9 \)
2) \( FoM_2 = 150 \text{ mV} \)
3) \( FoM_3 = 2.3 \text{ nF/m} \)

3. Proposed buffer

The integrated buffer circuit which is designed proceeding from the proposed FoMs is shows on figure 1, 2. This buffer is a part of the ASIC for the CBM MUCH. Simulation results (Transfer function, Rise Time and Power consumption for 3 sets of input signals) taking into account the extraction of both internal and external parasitic elements are presented in figure 3.

All simulations were performed in the CAD Cadence Virtuoso IC 6.1.7 using such tools, as ADE Assembler/Explorer, Layout GXL, and Calibre of Mentor Graphics.

Figure 3. Simulation results: (a) – transfer function, (b) – rise time, (c) – power consumption.
4. Conclusion
Paper describes the approach to creating built-in monitoring buffers for functional checking of ASICs as parts of test PCBs. The new figure of merit is presented. Finally, as an example, the results of designing a buffer version as part of the ASIC for the CBM MUCH are presented.

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