Reversible Logic Circuit Complexity Analysis via Functional Decomposition

Anupam Chattopadhyay and Anubhab Baksi

School of Computer Engineering, Nanyang Technological University, Singapore

Abstract—Reversible computation is gaining increasing relevance in the context of several post-CMOS technologies, the most prominent of those being Quantum computing. One of the key theoretical problem pertaining to reversible logic synthesis is the upper bound of the gate count. Compared to the known bounds, the results obtained by optimal synthesis methods are significantly less. In this paper, we connect this problem with the multiplicative complexity analysis of classical Boolean functions. We explore the possibility of relaxing the ancilla-free synthesis methods by using transformations and by starting from an Exclusive Sum-of-Product (ESOP) formulation remain, theoretically, the synthesis methods for achieving least gate count for the cases where the number of variables \( n \) is less than 8 and otherwise, respectively.

1. INTRODUCTION

A Boolean function \( f \) is of the form \( f : \{0,1\}^n \to \{0,1\} \) (or equivalently \( f : \mathbb{V}_2^n \to \mathbb{V}_2 \)). The output of the Boolean function \( f \) can be represented as a string of ones and zeros. It can also be represented as a multivariate polynomial over \( GF(2) \). This polynomial can be expressed as an exclusive disjunction (\( \oplus \)) of a constant \( a_0 \) and one or more conjunctions of the function argument. This is called the Exclusive Sum-Of-Product (ESOP) representation. An alternative representation of the ESOP form is known as the Algebraic Normal Form (ANF). The general ANF for a function \( f(x_1, \ldots, x_n) \) over \( n \)-variables can be written as,

\[
f(x_1, \ldots, x_n) = a_0 + a_1 x_1 + \cdots + a_i x_i + \cdots + a_n x_n + \cdots + a_{1,2,\ldots,n} x_1 x_2 \cdots x_n
\]

Reversible and Irreversible Boolean functions: An \( n \)-variable vectorial Boolean function is termed reversible if all its output patterns map uniquely to an input pattern and vice-versa. It can be expressed as an \( n \)-input, \( n \)-output bijection or alternatively, as a Boolean permutation function over the truth value set \( \{0,1,\ldots,2^{n-1}\} \). An irreversible Boolean function \( f_{irr} : \{0,1\}^n \to \{0,1\}^m \) with \( n \neq m \) can also be made reversible with the help of additional output lines, which adds distinguishing patterns to the irreversible output. Correspondingly, additional inputs are added. If an input line is constant-initialized and the constant is recovered after the circuit execution then, it is termed as ancilla. Otherwise, it is termed as garbage.

A. Reversible Logic Synthesis

Reversible Boolean logic synthesis is achieved with the help of reversible logic gates. The gates are characterized by their implementation cost in quantum technologies, which is denoted as the Quantum Cost (QC). A reversible gate library is a complete set of reversible gates which can be used to implement any reversible circuit. For example the set of NOT, CNOT, controlled-V and Controlled-V+, known as NCV, is a reversible gate library widely used in the literature. Recently, there has been a significant research activity towards the realization of quantum circuits using Clifford+T gates, considering the importance of fault tolerance in quantum computing. Efficient synthesis for NCV circuits \(^1\), Clifford+T circuits \(^2\) and mapping of NCV circuits to Clifford+T gates \(^3\) have been proposed in the literature. Few gates from these libraries are outlined below. For detailed discussion on primitive quantum gates and their universality, readers may refer to \(^4\), \(^5\).

- **NOT gate**: This is represented using the matrix \( \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \).
- **CNOT gate**: CNOT(a,b)\=\( (a, a \oplus b) \). This gate can be generalized with Tof\(_n\) gate, where first \( n-1 \) variables are used as control lines. Generalized Toffoli gates form an universal reversible logic gate library, termed as MCT.
- **Hadamard gate**: The unitary transformation for Hadamard gate is, \( \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \).
- **T gate**: The unitary transformation for this gate is, \( \begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{pmatrix} \).
- **Phase gate**: Also denoted by \( S \) and performs the unitary transformation of \( \begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{pmatrix} \). NOT, CNOT, Hadamard, S and \( S^+ \) gates together form the Clifford gate family.
- **Toffoli gate/CCNOT gate**: The gate flips the target if both the control lines are set: Tof(a,b,c)\=\( (a, b, c \oplus ab) \).

B. Cost Models

For evaluating the performance of the synthesis tools and benchmark circuit implementations, different cost models have been proposed in the literature. The most basic cost model is the number of reversible logic gates needed for the implementation. These logic gates could be, with rather large number of control lines, such as, for Multiple-Control Toffoli gates (MCT) or Mixed-Polarity Multiple Control Toffoli (MPMCT) gates. To closely reflect the cost in terms of quantum gates, the QC value is computed for each of these gates, which is nothing but the number of 2-qubit gates \( 2 \) needed to implement these circuits. In recent fault-tolerant Quantum circuit implementations, the cost is estimated in terms of T-count, corresponding to the Clifford+T realization. Logical depth or T-depth.
Finally, considering the cost and difficulty of implementing large number of qubits, one performance indicator is the total number of lines or ancilla/garbage count. It is well-known that there exists a trade-off between gate count/QC and ancilla count [7], [8]. It is trivial to show that with increasing ancilla count, MCT gates with smaller control lines can be realized, thereby establishing a clear trade-off between QC and ancilla. However, it not clear if such a trade-off exists for gate count vs ancilla.

2. BACKGROUND

For theoretical as well as practical interests, several researchers worked towards establishing the bounds on the gate count for reversible circuits. For selective classes of Boolean functions, much lower upper bound compared to generic Boolean functions has been reported in [9]. For reversible circuits of practical interest, e.g., modulo-exponentiation, addition, reversible circuit implementation with parameterized upper bounds have been established [10], [11]. We outline the major results in the gate count upper bound for different synthesis methods.

A. Upper Bound for Transformation-based Synthesis Methods

The gate cost upper bound for transformation-based synthesis methods, for \( n \)-variable reversible logic circuits, have been reported as following for two different gate libraries.

**Lemma 2.1:** The upper bound of gate count for MMD [12] using MPMCT library is \( (n-1)2^{n}+1 \) [13], [1].

**Lemma 2.2:** The upper bound of gate count for MMD [12] using MPMCT(+Fredkin gate) library is \( (n-2)2^{n}+2+n \) [1].

B. Upper Bound for BDD-based Synthesis Methods

The Binary Decision Diagram (BDD)-based synthesis method, originally proposed in [14], observed an gate count upper bound of 3.2\( n \). Note that this method generates high number of ancilla, which is in the order of \( O(2^n) \). By utilizing a bi-conditional decomposition, for selective Boolean functions, a tighter upper bound is proposed in [15], however, the worst-case upper bound remains the same for generic Boolean functions. Ancilla-free reversible logic synthesis for BDDs has been proposed recently [16], which does not report any theoretical bounds so far.

C. Upper Bound for ESOP-based Synthesis Methods

The tightest upper bound for reversible circuits have been reported in [17] following a mix of Young subgroups and Exclusive Sum-Of-Products (ESOP)-based synthesis approach. In the first phase of the synthesis with young subgroups, it is established that an \( n \)-variable reversible function can be implemented with a circuit of \((2n-1)\) single target gates. Further, it was shown that, an \( n \)-variable single target gate can be realized with at most \( 29 \cdot 2^{n-8} \) MPMCT gates, if \( n \geq 8 \).

Therefore, the gate count upper bound for the reversible circuit is \( 29 \cdot 2^{n-8} \cdot (2n-1) \) MPMCT gates, if \( n \geq 8 \). The upper bound of the single target gate implementation is established by using a result from [13]. Note that this method does not require any ancilla line.

For the rest of the paper, we will closely follow the above synthesis method and focus on the complexity of a single-output Boolean function. We will assume the single target distribution obtained from Young subgroup method [17] and concentrate on the functional decomposition approach of Boyar et al [19] to check for potential improvements.

D. Multiplicative Complexity

In parallel with the efforts for enumerating the reversible circuit complexity, progress in the analysis of classical Boolean functions in terms of multiplicative complexity is reported [19]. The primary application for this analysis has been towards the design of cryptographic primitives, though.

**Definition 2.3:** The multiplicative complexity \( C_{m}(f) \) of a Boolean function is the minimum number of multiplications (AND-gates) that are sufficient to evaluate the function over the basis \((\land, \lor, \neg)\).

It has been established that the multiplicative complexity of functions having degree \( d \) is at least \( d-1 \) [20] and the multiplicative complexity of a randomly selected \( n \)-variable Boolean function is at most \( 2^{d+1} - n/2 - 2 \) (\( n \) even) [19].

Intuitively, multiplicative complexity of a Boolean function has some correspondence with the Toffoli gate. The number of AND gates in a single term of ESOP expression represents the number of control lines in a Toffoli gate. In the following sections, we follow the same approach of the derivation of multiplicative complexity and explore if it reduces the theoretical upper bound of gate count compared to the currently known bounds.

3. UPPER BOUNDS VIA MULTIPlicative COMPLEXITY ANALYSIS

In this section, we first revisit the function decomposition approach used in [17] Section 4 from a mathematical perspective. We show that their work can be described as solving a linear recurrence of the form:

\[
f(n) = 2f(n-1) + 2
\]

with the initial conditions \( f(5) = 10, f(4) = 4 \).

The reason for adopting the recurrence relation, \( f(n) = 2f(n-1) + 2 \) is described in second paragraph of the proof of [17] Theorem 1, so we skip that part. The case for \( f(5) \) is described in [21], which is cited in [17].

Now, assume that, we want to solve: \( f(n) = 2f(n-1) + 2 \). We substitute \( n \) by \( n+1 \) to yield, \( f(n+1) = 2f(n)+2 \). Now, subtracting, we get \( f(n+1) - f(n) = 2f(n) - 2f(n-1) \)

\[
\implies f(n+1) = 3f(n) - 2f(n-1)
\]

Hence, the characteristic equation is: \( x^2 = 3x-2 \Rightarrow (x-1)(x-2) = 0 \Rightarrow x = 1, 2 \), and hence, \( f(n) = \alpha \cdot 1^n + \beta \cdot 2^n \), where \( \alpha, \beta \) are constants to be determined from the initial conditions.

Now, given that, \( f(5) = 10, f(4) = 4 \), we generate the linear equations: \( f(5) = \alpha + 32\beta = 10, f(4) = \alpha + 16\beta = 4 \), which gives, \( \alpha = -2, \beta = \frac{3}{8} = 3 \cdot 2^{-3} \).

Therefore, \( f(n) = -2 + 3 \cdot 2^{-3} \cdot 2^n = 3 \cdot 2^{n-3} - 2 \).
A. Based on Function Decomposition

A recursive decomposition procedure can be used for systematic implementation of reversible Boolean functions. From a given ESOP form, three following functional decompositions can be applied.

\[ f = \overline{x_1} \cdot f_{x_1=0} + x_1 \cdot f_{x_1=1} \]  
(1)

\[ f = f_{x_1=0} \oplus x_1 \cdot f_{x_1=2} \]  
(2)

\[ f = f_{x_1=1} \oplus \overline{x_1} \cdot f_{x_1=2} \]  
(3)

where \( f_{x_1=2} = f_{x_1=0} \oplus f_{x_1=1} \). These are known as Shannon, positive Davio and negative Davio decompositions respectively. Here, we adopt the positive Davio decomposition. The Shannon decomposition leads to a \(2^n\) gates. However, if we assume that computing each function, we need to look into the complete set of all possible minterms can also be implemented with \(2^n\) gates. Further, the positive Davio and negative Davio decompositions respectively. Here, we adopt the positive Davio decomposition. The Shannon set of all possible minterms can also be implemented with \(2^n\) gates. Further, the positive Davio and negative Davio decompositions respectively. Here, we adopt the positive Davio decomposition.

In [19, Lemma 5], it was proved that it requires at most \(2^n - n - 1\) AND (\(\land\) and \(\lor\) gates) for realizing all the positive minterms of \(n\) Boolean variables. In that, authors proposed a circuit of alternating \(\land\) and \(\lor\) gates. It is evident that this set of all possible minterms can also be implemented with only MCT gates, when \(0\)-initialized ancilla lines are used. A representative implementation is shown in the following Fig. 1. This requires \(2^n - n - 1\) MCT gates and total \(2^n - 1\) lines.

We start with an idea similar to [19 Theorem 6]. Following positive Davio decomposition, \(\forall f : \mathbb{F}_2^n \rightarrow \mathbb{F}_2\), it is possible to find \(f_1, f_0 : \mathbb{F}_2^{n-1} \rightarrow \mathbb{F}_2\) such that,

\[ f(x_1, x_2, \ldots, x_n) = x_1 f_1(x_2, \ldots, x_n) \oplus f_0(x_2, \ldots, x_n). \]

Alternatively, it can be stated that, \(f\) is divided by \(x_1\), with \(f_1\) being the quotient and \(f_0\) being the remainder. For example, if \(f(x_1, x_2, x_3) = x_1 x_2 x_3 \oplus x_1 x_2 \oplus x_2 x_3 \oplus x_1 \oplus x_2 \oplus 1\), then \(f_1(x_2, x_3) = x_2 x_3 \oplus x_2 \oplus 1\) and \(f_0(x_2, x_3) = x_2 x_3 \oplus x_2 \oplus 1\). Also, notice that both \(f_0, f_1\) are of (at most) \(n - 1\) variables.

Note that, if we can implement \(f_1\) and \(f_0\), then we can readily implement \(f\) just by using one MCT gate (using \(x_1, f_1\) as the control lines and \(f_0\) as the target line, as depicted in Fig. 2).

Thus, we make the following observation:

\[ \mathcal{M}(f) \leq 1 + \mathcal{M}([f_1, f_0]), \]

where \(\mathcal{M}([f_1, f_0])\) denotes the MCT gate complexity of \(f_1, f_0\) combined. Therefore, we can express the MCT gate complexity of an \(n\)-input function \(f\) in terms functions of lower numbers of input variables. We can recursively use this decomposition:

\[ f = x_1 f_1 \oplus f_0 = x_1 (x_2 f_{11} \oplus f_{10}) \oplus x_2 f_{01} \oplus f_{00} = x_1 (x_2 f_{11} \oplus f_{10}) \oplus x_3 f_{101} \oplus f_{100} \oplus (x_2 f_{011} \oplus f_{010}) \oplus x_3 f_{001} \oplus f_{000} \]

In the above decomposition, at \(k\)-th step, we require \(2^k - 1\) additional MCT gates other than the ones needed by the new functions of lower input variables. Thus, after \(k\)-th step, we can write:

\[ \mathcal{M}(f) \leq 1 + \mathcal{M}([f_1, f_0]) \leq 3 + \mathcal{M}([f_{11}, f_{10}, f_{01}, f_{00}]) \]

\[ \vdots \]

\[ \leq (2^k - 1) + \mathcal{M}([f_{i_1, i_2, \ldots, i_k} | i_1, i_2, \ldots, i_k \in \{0, 1\}^k]) \]

Note that, all functions \([f_{i_1, i_2, \ldots, i_k} | i_1, i_2, \ldots, i_k \in \{0, 1\}^k]\) are (at most) of \(n - k\) variables, hence, \([f_{i_1, i_2, \ldots, i_k} | i_1, i_2, \ldots, i_k \in \{0, 1\}^k]\) denotes some circuit with \(n - k\) variables.

\[ \text{Fig. 1. Implementation of Minterms} \]

\[ \text{Fig. 2. Implementation of } f \text{ from } f_1 \text{ and } f_0 \text{ as inputs} \]
Therefore, using the lemma 3.1 (here, \( r = 2^k \)) and the MCT gate count for the minterm constructions, in equation 4, we can write

\[
\mathcal{M}(f) \leq (2^k - 1) + \mathcal{M}\{\{f_{i_1}, i_2, \ldots, i_k \mid i_1, i_2, \ldots, i_k \in \{0, 1\}^k\}
\]

\[
\leq (2^k - 1) + \{2^{n-k} - (n-k) - 1\} + 2^k \left(\frac{2^{n-k} - 1}{2} - 1\right)
\]

\[
\leq (2^k - 1) + \{2^{n-k} - (n-k) - 1\} + 2^{n-1} - 3 \cdot 2^{n-k}
\]

(5)

Assuming \( k = n/2 \) to be the point, where we stop the functional decomposition and construct the functions from the available positive minterms, we obtain

\[
\mathcal{M}(f) \leq 2^{n-1} + 2^{n-2} - n/2 - 2
\]

(6)

This leads to an overall MCT gate complexity of

\[
(2n - 1)(2^{n-1} + 2^{n-2} - n/2 - 2)
\]

(7)

by following the Young subgroup decomposition. Corresponding bound for the garbage count is \( O(2^{n/2}) \), which is introduced for the minterm construction and for the realization of the functions once the decomposition procedure is stopped.

---

**B. Discussion**

It can be noted that the MCT gate complexity, derived through the approach of [19] is worse compared to that of the transformation-based method (for \( n < 8 \)) and the ESOP-based method (for \( n \geq 8 \)) (see Fig. 3). This leads to the conclusion that introducing ancilla/garbage lines does not lead to any reduction in the gate count complexity, if functional decomposition approach is followed. On the other hand, different complexity bounds in different synthesis approaches indicate that it might be beneficial to adopt a hybrid synthesis approach for reversible circuit realization.

**REFERENCES**

[1] M. Soeken and A. Chattopadhyay, “Fredkin-enabled transformation-based reversible logic synthesis,” in *Multiple-Valued Logic (ISMVL), 2015 IEEE International Symposium on*, May 2015, pp. 60–65.

[2] M. Amy, D. Maslov, M. Mosca, and M. Roetteler, “A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits,” *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 32, no. 6, pp. 818–830, June 2013.

[3] D. Miller, M. Soeken, and R. Drechsler, “Mapping ncir circuits to optimized Clifford+T circuits,” in *Reversible Computation, ser. Lecture Notes in Computer Science*, S. Yamashita and S.-i. Minato, Eds. Springer International Publishing, 2014, vol. 8507, pp. 163–175. [Online]. Available: http://dx.doi.org/10.1007/978-3-319-08494-7_13

[4] A. Barenco, C. H. Bennett, R. Cleve, D. F. DiVincenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter, “Elementary gates for quantum computation,” *Phys. Rev. A*, vol. 52, pp. 3457–3467, Nov 1995. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevA.52.3457

[5] A. Barenco, “A universal two-bit gate for quantum computation,” *Proceedings: Mathematical and Physical Sciences*, vol. 449, no. 1937, pp. 679–683, 1995.

[6] “Reversible Logic Synthesis Benchmarks Page,” howpublished = http://webhome.cs.uvic.ca/~dmaslov/, note = Accessed: 2015-10-19.

[7] R. Wille, M. Soeken, D. M. Miller, and R. Drechsler, “Trading off circuit lines and gate costs in the synthesis of reversible logic,” *Integration, the VLSI Journal*, vol. 47, no. 2, pp. 284 – 294, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0378568813000436

[8] A. Chattopadhyay, N. Pal, and S. Majumder, “Ancilla-quantum cost trade-off during reversible logic synthesis using exclusive sum-of-products,” *CoRR*, vol. abs/1405.6073, 2014. [Online]. Available: http://arxiv.org/abs/1405.6073

[9] A. Chattopadhyay, S. Majumder, C. Chandak, and N. Chowdhury, “Constructive reversible logic synthesis for boolean functions with special properties,” in *Reversible Computation*, ser. Lecture Notes in Computer Science, S. Yamashita and S.-i. Minato, Eds. Springer International Publishing, 2014, vol. 8507, pp. 95–110. [Online]. Available: http://dx.doi.org/10.1007/978-3-319-08494-7_8

[10] Y. Takahashi, S. Tani, and N. Kumihoro, “Quantum addition circuits and unbounded fan-out,” *Quantum Inf. Comput.*, vol. 10, no. 9, pp. 872–890, Sep 2010. [Online]. Available: http://dl.acm.org/citation.cfm?id=2011464.2011476

[11] M. Saeedi and I. L. Markov, “Synthesis and optimization of reversible circuits-a survey,” *ACM Comput. Surv.*, vol. 45, no. 2, pp. 21:1–21:34, Mar. 2013.

[12] D. Miller, D. Maslov, and G. Dueck, “A transformation based algorithm for reversible logic synthesis,” in *Design Automation Conference*, 2003, pp. 318–323.

[13] D. Maslov, G. Dueck, and D. Miller, “Toffoli network synthesis with templates,” Computer-Aided Design of Integrated Circuits and Systems, *IEEE Transactions on*, vol. 24, no. 6, pp. 807–817, June 2005.

[14] R. Wille and R. Drechsler, “BDD-based Synthesis of Reversible Logic for Large Functions,” in *Proceedings of the 46th Annual Design Automation Conference*, ser. DAC ’09, 2009, pp. 270–275.

[15] A. Chattopadhyay, A. Littarru, L. Amaru, P.-E. Guillardon, and G. De Micheli, “Reversible logic synthesis via biconditional binary decision diagrams,” in *Multiple-Valued Logic (ISMVL), 2015 IEEE International Symposium on*, May 2015, pp. 2–7.

[16] M. Soeken, L. Tague, G. W. Dueck, and R. Drechsler, “Ancilla-free synthesis of large reversible functions using binary decision diagrams,” *J. Symb. Comput.*, vol. 73, pp. 1–26, 2016. [Online]. Available: http://dx.doi.org/10.1016/j.jsc.2015.03.002

[17] N. Abdessaied, M. Soeken, M. K. Thomesen, and R. Drechsler, “Upper bounds for reversible circuits based on young subgroups,” *Information Processing Letters*, vol. 114, no. 6, pp. 282–286, 2014.

[18] A. Gaidukov, “Algorithm to derive minimal esop for 6-variable function,” in *International Workshop on Boolean Problems*, 2002, pp. 141–148.

[19] I. Boyar, René Peralta, Denis Pouchue, “On the multiplicative complexity of Boolean functions over the basis \( \{\wedge, \oplus\} \),” *Theor. Comput. Sci.*, vol. 235, no. 1, pp. 43–57, 2000. [Online]. Available: http://dx.doi.org/10.1016/S0304-3975(99)00182-6

[20] C.-P. Schnorr, “The multiplicative complexity of boolean functions,” in *Proceedings of the 6th International Conference, on Applied Algebra, Algebraic Algorithms and Error-Correcting Codes*, ser. AAECC-6, London, UK, UK: Springer-Verlag, 1989, pp. 45–58. [Online]. Available: http://dl.acm.org/citation.cfm?id=6646025.676419

[21] D. Grosse, R. Wille, G. Dueck, and R. Drechsler, “Exact multiple-control toffoli network synthesis with sat techniques,” *Computer-Aided Design*
of Integrated Circuits and Systems, IEEE Transactions on, vol. 28, no. 5, pp. 703–715, May 2009.