ESSOP: Efficient and Scalable Stochastic Outer Product Architecture for Deep Learning

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Abstract—Deep neural networks (DNNs) have surpassed human-level accuracy in a variety of cognitive tasks but at the cost of significant memory/time requirements in DNN training. This limits their deployment in energy and memory limited applications that require real-time learning. Matrix-vector multiplications (MVM) and vector-vector outer product (VVOP) are the two most expensive operations associated with training of DNNs. Strategies to improve the efficiency of MVM computation in hardware have been demonstrated with minimal impact on training accuracy. However, the VVOP computation remains a relatively less explored bottleneck even with the aforementioned strategies. Stochastic computing (SC) has been proposed to improve the efficiency of VVOP computation but on relatively shallow networks with bounded activation functions and floating-point (FP) scaling of activation gradients. In this paper, we propose ESSOP, an efficient and scalable stochastic outer product architecture based on the SC paradigm. We introduce efficient techniques to generalize SC for weight update computation in DNNs with the unbounded activation functions (e.g., ReLU), required by many state-of-the-art networks. Our architecture reduces the computational cost by re-using random numbers and replacing certain FP multiplication operations by bit shift scaling. We show that the ResNet-32 network with 33 convolution layers and a fully-connected layer can be trained with ESSOP on the CIFAR-10 dataset to achieve baseline comparable accuracy.

I. INTRODUCTION

Research on developing accelerators for training deep neural networks (DNNs) has attracted significant interest. Several potential applications such as autonomous navigation, health care, and mobile devices require learning in-the-field while adhering to strict memory and energy budgets. DNN training demands significant time and compute/memory. The two most expensive computations in DNNs are the matrix-vector multiplications (MVM) and vector-vector outer product (VVOP) and both require \( O(N^2) \) multiplications for a layer with a weight matrix of the size \( N \times N \). Several strategies to improve efficiency of MVM computation have been proposed with minimal impact on the training accuracy. These strategies leverage either low precision digital representation \([1], [2]\) or crossbar architectures \([3], [4], [5], [6]\). Less precise implementations of MVM are shown to perform sufficiently well for DNN training \([1], [2], [7], [8], [9], [10]\).

For improving the efficiency of VVOP computation to calculate the weight updates, the algorithmic ideas that have been proposed so far require expensive multiplier circuits \([11], [12], [13]\). Stochastic computing (SC) has been suggested as an efficient alternative to floating point (FP) multiplications, given that operands are real numbers in \([0, 1]\). This poses challenges for DNN training as operations such as ReLu, batchnorm, etc. have unbounded outputs. Moreover, small error gradients are often quantized to 0 due to the limited precision in the range \([0,1]\).

The main contributions of this paper are the following: (1) We propose an SC-based efficient architecture ESSOP for computing weight updates for DNN training. (2) We introduce efficient schemes to generalize SC-based multiplier to unbounded activation functions (e.g. ReLU) that are essential for DNN training \([14], [15], [16]\). (3) We show that these improvements have minimal effect on training accuracy of a deep convolution neural network (CNN). (4) Post place and route results at 14nm CMOS show that ESSOP design is 82.2% and 93.7% better in energy and area efficiency respectively, compared to a highly pipelined FP16 multiplier design for outer product computation.

II. BACKGROUND AND MOTIVATION

A. Neural Network Training

DNN training proceeds in three phases, namely (1) forward propagation, (2) backpropagation and (3) weight update. As shown in Fig. 1 MVM operation is essential in forward and backpropagation while during the weight update phase, the VVOP is computed between the error gradient \( \Delta \) of that layer and the output activations of the previous layer \( X \) to calculate the weight update matrix \( \delta W \) (see Eq. (1)). Note that this \( \delta W \) calculation, in general, applies to both fully-connected and convolution layers as well \([7]\).

\[
\delta W = \Delta \times X^T
\]  

(1)
B. Stochastic Computing (SC)

SC is a method of computing arithmetic operations using the stochastic representation of real numbers constrained to the interval \([0, 1]\), instead of using real valued operands [18], [19], [20]. For notational convenience, we denote scalars by lowercase letters (e.g. \(x \in \mathbb{R}\)) and vectors by uppercase letters (e.g. \(X \in \mathbb{R}^N\)). To compute the stochastic representation \(\Psi_r \in \{0, 1\}^M\) of a real number \(r\), where \(r \in [0, 1]\), a Bernoulli sequence with \(M\) binary bits is computed such that the probability that any one of these bits being 1 is equal to \(r\), i.e., \(P(\Psi^k_r = 1) = r \forall k = 1, 2, \ldots, M\).

Using this representation, the product of two real numbers \(c = r \times b\), where \(b \in [0, 1]\), can be computed using the bit-wise AND operation on the Bernoulli sequences as

\[
P(\Psi^k_c = 1) = P(\Psi^k_r = 1) \wedge P(\Psi^k_b = 1) \quad \forall k = 1 : M \quad (2)
\]

and

\[
c \sim E[\Psi_c] = E[\Psi_r \wedge \Psi_b] \quad (3)
\]

Equation (3) thus replaces the expensive floating point multiplications with bitwise AND operations and subsequent summation operations. However, the range of numbers being multiplied in DNNs is usually not confined to \([0, 1]\). Equations (2) and (3) can be generalized to numbers of arbitrary range; we illustrate this assuming \(X\) and \(\Delta\) both have \(N\) elements and weight update is determined using VVOP computation as given by equation (1). Assuming that the vector \(X\) lies in the range of \([-x_{\text{max}}, x_{\text{max}}]\) and similarly the error gradient \(\Delta\) lies in the range \([-\delta_{\text{max}}, \delta_{\text{max}}]\), we first normalize both \(X\) and \(\Delta\) vectors to constrain their values to \([-1, 1]\) as,

\[
\bar{X} = \frac{X}{x_{\text{max}}} \quad \bar{\Delta} = \frac{\Delta}{\delta_{\text{max}}} \quad (4)
\]

Next, we denote the stochastic representation of all elements in a vector \(X\) as \(\Psi_X \in \{0, 1\}^{N \times M}\). For computing the Bernoulli sequences of \(\Psi_X\) and \(\Psi_{\Delta}\) in hardware, we can implement a random number generator (RNG) to sample from the uniform distribution of \([0, 1]\) and compare the normalized real number with the sampled random number:

\[
\Psi^{i,k}_\zeta = \begin{cases} 1 & \text{if } RNG^k_\zeta \geq \bar{X}^i \\text{else } 0 \end{cases} \quad \forall k = 1 : M \quad (5)
\]

In [5], \(\Psi^{i,k}_\zeta\) is the \(i^{th}\) Bernoulli event of the \(i^{th}\) element of \(\zeta\) obtained by comparing \(i^{th}\) element of \(\zeta\) with \(k^{th}\) sample from corresponding random number generator \(RNG^k_\zeta\), where \(\zeta \in X\) or \(\Delta\). We can approximate the product in equation (1) using SC as,

\[
\delta W^{ji} = \text{sign}(\delta W^{ji}) \times F_{\text{scale}} \times \sum_{k=1:M} \Psi^{i,k}_\Delta \wedge \Psi^{i,k}_X \quad (6)
\]

where the parameter \(F_{\text{scale}}\) is defined as \((x_{\text{max}} \times \delta_{\text{max}})/M\).

From equations (4)-(6), it is clear that a SC-based multiplier implementation for VVOP calculation presents the following challenges: (i) determination of the maximum elements \(x_{\text{max}}\) and \(\delta_{\text{max}}\) of the vectors \(X\) and \(\Delta\) respectively in equation (4), requiring \(O(N)\) floating point comparisons; (ii) floating point division for normalization in equation (4) that requires \(O(N)\) floating point division operations; (iii) computation in equation (5) requires \(O(MN)\) random number generations; and (iv) scaling by \(F_{\text{scale}}\) in equation (6) requires \(O(N^2)\) FP multiplication operations. We now discuss several techniques to address these challenges.

III. OPTIMIZATION OF THE SC-BASED MULTIPLIER FOR THE DESIGN OF ESSOP ARCHITECTURE

A. Eliminating the normalization operations

As discussed above, the normalization operation introduces \(O(N)\) floating point divisions. This can be addressed by the following improvement. Consider a number \(z\) that lies in the range \([0, 1]\) and another real number \(y\) that is obtained by using a constant positive scaling factor \(y_{\text{max}}\) as \(y = z \times y_{\text{max}}\). A Bernoulli representation \(\Psi_z^k\) of \(z\) is obtained as \(z \geq RNG^k_z, \forall k = 1 : M\) and that of \(y\) is,

\[
\Psi_y^k = \begin{cases} 1 & \text{if } y \geq y_{\text{max}} \times RNG^k_z \\text{else } 0 \end{cases} \quad \forall k = 1 : M \quad (7)
\]

In equation (7), RNG can be realized by using a linear feedback shift register (LFSR) circuit to generate \(p\)-bit pseudo-random numbers. Notably, the hardware realization of equation (7) does not require a multiplication with \(y_{\text{max}}\) and can be realized by sampling few bits from the LFSR. For example, in a floating point representation, \(2^{p}\)th power in \(y_{\text{max}}\) can be used as an exponent and \(RNG^k_z\) as mantissa to compute \(y_{\text{max}} \times RNG^k_z\) without any floating point multiplications. Alternatively, in a fixed point representation, only a fraction of the bits generated from the LFSR need to be used to eliminate the fixed point multiplications in equation (7). For instance, if \(y_{\text{max}}\) requires only 8-bits in the fixed point representation, 8-bits could be sampled from the \(p\)-bit LFSR to compute \(y_{\text{max}} \times RNG^k_z\). This eliminates the need for \(O(N)\) expensive divisions irrespective of the numerical representation of \(y\).

B. Reusing the generated random numbers

The next hurdle for a SC-based multiplier is the requirement to create \(O(MN)\) uniformly distributed \(p\)-bit random numbers. In order to efficiently utilize the generated random numbers, we propose to reuse the random numbers, for the computations in equation (5). \(N\) times by generating only \(M\) random numbers. Hence, we generate only \(2M\) random numbers in equation (5) instead of \(MN\). This allows us to store only \(2M\) random numbers in memory, which is significantly less than the \(MN\) required in traditional methods.

Fig. 1. Illustration of the two bottleneck operations in DNN training. Each of the illustrated operations require \(O(N^2)\) multiplications. Unlike MVM, VVOP is a relatively less explored problem that eventually becomes the bottleneck even when MVM is efficiently implemented in hardware. The ESSOP architecture addresses this problem to enable efficient hardware implementation of DNN training.
numbers from the LFSR instead of $2NM$ random numbers for the $2N$ elements in $X$ and $\Delta$ combined. The first $M$ random numbers are used to generate the Bernoulli sequences of all the elements in the vector $X$ and the remaining $M$ random numbers are used to generate the Bernoulli sequences of all the elements in the vector $\Delta$. For example, to generate 8-bit long Bernoulli sequences corresponding to 256-element long vectors $X$ and $\Delta$, only 16 random numbers are generated. The first 8 random numbers will be used to generate the Bernoulli sequence of all elements in the vector $X$ and the remaining 8 for that of vector $\Delta$. With this modification, random number generation complexity is reduced to $O(M)$, making it independent of the dimensions of the weight matrix. As our detailed network simulations indicate, unintended correlations are not introduced by reusing random numbers, as the two Bernoulli sequences in equation (6) are uncorrelated.

### C. Approximating the scaling operations

Scaling the result of the AND operation in equation (6) with $F_{\text{scale}}$ is an $O(N^2)$ operation involving full-precision multiplications. To efficiently realize this scaling operation in hardware, we propose to use the closest $2^{th}$ power of the number $F_{\text{scale}}$ obtained as shown below,

$$F_{\text{scale}} = 2^\lfloor \log_2(F_{\text{scale}}) \rfloor$$

where $\lfloor x \rfloor$ denotes the largest integer smaller than $x$. Using $F_{\text{scale}}$ instead of $F_{\text{scale}}$ makes the computations in equation (6) straightforward as only bit shift operations are required. Usually, $F_{\text{scale}}$ in DNNs will be smaller than 1 and hence such a bit-shift operation will mostly be a right shift operation. In the case of stochastic gradient descent optimizer, note that the learning rate can also be accommodated in the $F_{\text{scale}}$ computation.

### IV. THE ESSOP ARCHITECTURE

#### A. Unit cell design

We leverage innovations from Section III to develop the architecture of a single SC-based multiplier that we refer to as an ESSOP unit cell, shown in Fig. 2(a). At the periphery of the unit cell, $M$-bit stochastic sequences $\psi^X$ and $\psi^\Delta$ are computed for two input real numbers $X$ and $\Delta$ respectively. The unit cell receives two inputs each with 2 bits representation, with the first bit representing the stochastic representation of a real number and the second bit is the sign of the real number. The sign of the final product is computed using a 1-bit XOR on the sign bits of two real numbers. In our design, we assume a simple 2-input AND gate that is used $M$ times to compute the $M$-bit representation of SC-based multiplication. For each cycle out of $M$ cycles, the output of the AND gate is fed to a counter that counts the number of 1s in the resulting sequence. In the periphery of the unit cell, $F_{\text{scale}}$ is computed, which is used by the shift logic circuit to scale the output of the counter to a desired range. Shift logic will depend on the digital representation used for the input real numbers. For example, for a floating point representation as shown in Fig. 2(b), shift logic is as simple as copying the output of the XOR to the sign bit position, the counter output to the mantissa position and $F_{\text{scale}}$ value to the exponent position. Finally, the result of the shift logic circuit is stored in a latch (or in a desired memory location) for the weight update. Note that the SC-based multiplier requires only $M$ clock cycles to compute one product.

#### B. The multi-cell architecture of ESSOP

To compute all the elements of an outer product matrix, either a unit cell can be multiplexed or multiple unit cells can be used simultaneously. The proposed ESSOP architecture has multiple unit cells stacked in a single row. The high-level architecture of ESSOP is shown in Fig. 3, and has $N$ unit cells (U) arranged in a row. At the periphery of the unit cells, all inputs have their corresponding comparator (C). Each comparator receives two inputs, one from either an element of an activation vector ($X$) or error gradient vector ($\Delta$), second from a corresponding random number generator (R). The comparator generates one stochastic bit by comparing two
inputs at a time. In the M-bit implementation of the ESSOP, several such random numbers could be fed to the comparator circuit to compute M comparisons in total, resulting in an M-bit long stochastic sequence. As discussed in Section III-B, there are exactly two RNGs, one for X and another for ∆, that generate M random numbers each for every outer product.

V. NUMERICAL VALIDATION

We train the ResNet-32 network on CIFAR-10 dataset to validate the ESSOP architecture. We use ESSOP to compute weight updates in all the 33 convolution layers and in the final layer of the ResNet-32 network. The CIFAR-10 dataset has 50K images in the training set and 10K images in the test set. Each image in the dataset has a resolution of 32 × 32 pixels and three channels and belongs one of the ten classes. We preprocess CIFAR-10 images by implementing the commonly used image processing steps for the family of residual networks as reported in [22]. The simulation was performed with FP16 precision for data and computation, with a mini-batch size of 100 images for 200 epochs. We used initial learning rate (LR) of 0.1 with LR evolution (LRE) for baseline as in [14]; LRE is tuned for better accuracy in ESSOP implementation. The categorical cross-entropy loss function is minimized using stochastic gradient descent with momentum of 0.9. In our results, we denote ESSOP16(M) to indicate FP16 precision for input operands (X and ∆) represented using M-bit Bernoulli sequences. Fig. 4 shows the accuracy of ResNet-32 as a function of ESSOP16 sequence length. The test accuracy drop with ESSOP16(16) is only 0.25% compared to the baseline. Experiments on different sequence lengths indicate that 16-bits is sufficient to achieve close to baseline accuracy with FP16 outer product. ESSOP16(16) shows an average of 0.73% drop in the test accuracy compared to the baseline accuracy. ESSOP16(8) has on an average of 1.13% drop in test accuracy compared to the baseline. Remarkably, ESSOP16(2) has on an average of only 2.6% drop in the test accuracy compared to the baseline. It is important to note that with a sequence length of 2-bits, it is possible to compute the weight update in just 2 clock cycles.

VI. POST LAYOUT RESULTS

In this section, we present the details of hardware implementation of ESSOP16 and compare its post route layout performance with that of a highly pipelined FP16 multiplier design after place and route. FP16 design is an array of N = 64 FP16 multipliers (from Samsung’s Low Power Plus (LPP) library) that compute 64 FP16 multiplications in parallel. Similarly, ESSOP16 design has 64 unit cells (U1 to U4k) to compute 64 elements of an outer product matrix in parallel, as illustrated in Fig. 5. Inputs X and ∆, which are in FP16 precision, are fed to the corresponding comparator circuit (C1 to C4k). Two RNGs R_X and R_∆ corresponding to X and ∆ generate M random numbers each. Each RNG generates only mantissa part of the random number, exponent (E_X or E_∆) is derived from the absolute maximum number in the vector X or ∆ and sign bit is derived from another input of a corresponding comparator. Configuration parameters such as Bernoulli sequence length is stored in configuration register G. Post place and route results at 14 nm using Samsung LPP libraries are shown in Fig. 5. These results indicate ESSOP16(16) design, even though sequential and not pipelined, operates at 1.9× higher frequency and achieves 82.2% and 93.7% better energy and area efficiency respectively, compared to the FP16 multiplier array for outer product computation.

VII. CONCLUSION

We proposed an efficient hardware architecture ESSOP that facilitates training of deep neural networks. The central idea is to efficiently implement the vector-vector outer product calculation associated with the weight updates using stochastic computing. We proposed efficient schemes to implement the stochastic computing-based multipliers that can generalize to operands with unbounded magnitude and significantly reduce the computational cost by re-using random numbers. This addresses a significant performance bottleneck for training DNNs in hardware, particularly for applications with stringent constraints on area and energy. ESSOP complements architectures that accelerate matrix-vector multiply operations associated with the forward and backpropagations where weights are represented in low precision or stored in computational memory based crossbar array architectures. We evaluated ESSOP on a 32-layer deep CNN that achieves baseline comparable accuracy for a sequence length of 16-bits. 14 nm place and route of the ESSOP architecture compared with FP16 design shows 82.2% and 93.7% improvement in energy and area efficiency respectively for outer product computation.
