mpiQulacs: A Distributed Quantum Computer Simulator for A64FX-based Cluster Systems

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Abstract—Quantum computer simulators running on classical computers are essential for developing real quantum computers and emerging quantum applications. In particular, state vector simulators, which store a full state vector in memory and update it in every quantum operation, are available to simulate an arbitrary form of quantum circuits, debug quantum applications, and validate future quantum computers. However, the time and space complexity grows exponentially with the number of qubits and easily exceeds the capability of a single machine.

Therefore, we develop a distributed state vector simulator, mpiQulacs, that is optimized for large-scale simulation on A64FX-based cluster systems. A64FX is an ARM-based CPU that is also equipped in the world’s top Fugaku supercomputer. We evaluate weak and strong scaling of mpiQulacs with up to 36 qubits on a new 64-node A64FX-based cluster system named Todoroki. By comparing mpiQulacs with existing distributed state vector simulators, we show that mpiQulacs achieves the highest performance for large-scale simulation on tens of nodes while sustaining a nearly ideal scalability. Besides, we define a new metric, quantum B/F ratio, and use it to demonstrate that mpiQulacs running on Todoroki fits the requirements of distributed state vector simulation rather than the existing simulators running on general purpose CPU-based or GPU-based cluster systems.

Index Terms—quantum computing, quantum computer simulator, distributed computing, cluster system

I. INTRODUCTION

Quantum computing is attracting a lot of attention both in industry and academia owing to the potential of exponential computing power. However, since it is still at the dawn, further innovation and development both in quantum hardware and software are necessary for the practical usage of quantum computing. Quantum computer simulators running on classical computers are essential for this purpose, because they can simulate the behaviors of future quantum computers and accelerate the development of emerging quantum applications.

State vector simulators are one of the representative quantum computer simulators, which store a full state vector in memory and update it in every quantum operation. They can be used to simulate an arbitrary form of quantum circuits, debug quantum applications, and validate real quantum computers. Although tensor network simulators have also been developed to simulate large-scale quantum circuits with up to 100 qubits [1], they can only simulate circuits with low depth and do not effectively support intermediate measurement for quantum software debugging [2]. We aim to accelerate the development of emerging quantum applications and thus target state vector simulators in this work.

The major challenge of state vector simulators is time and space complexity which grows exponentially with the number of qubits of a given quantum circuit. When a state vector is represented in double precision, an n-qubit circuit requires $2^{n+1}$ bytes of memory space. For instance, a 36-qubit circuit requires 1 TiB of memory space. Although such a memory space can be allocated on a single high-end server having terabytes of memory, its computational power is not sufficient for the 36-qubit simulation in a practical time. On the other hand, high-performance computing devices such as GPUs are necessary for fast simulation, but the memory capacity of such devices is still limited to tens of gigabytes. Therefore, distributed state vector simulators have been developed for fast and large-scale simulation on cluster systems [3]–[6].

In this work, we develop a distributed state vector simulator, mpiQulacs, that is based on Qulacs [7] and optimized for A64FX-based cluster systems. Qulacs is one of the fastest state vector simulator running on a single machine and supports general quantum operations to meet popular demands in quantum computing research. We extend Qulacs with message passing interface (MPI) to support distributed simulation on multiple computing nodes. mpiQulacs is optimized to fully utilize the high memory bandwidth of an A64FX CPU. It is a 48-core ARM-based CPU having high-bandwidth memory (HBM2) and also used in the world’s top Fugaku supercomputer. In addition, we implement a fused-swap gate in mpiQulacs based on the idea discussed in [8] to minimize MPI communication for distributed simulation.

We construct a new 64-node A64FX-based cluster system named Todoroki and use it to evaluate weak and strong scaling of mpiQulacs with up to 36 qubits. By comparing the results of mpiQulacs with those of existing distributed state vector simulators reported in corresponding papers, we show that mpiQulacs achieves the highest performance for large-scale simulation on tens of nodes while sustaining nearly ideal weak and strong scaling. Moreover, we define a novel metric, quantum B/F ratio (QBF), that indicates the execution efficiency of state vector simulators running on cluster systems. The QBF evaluation demonstrates that mpiQulacs running on Todoroki fits the requirements of distributed state vector simulation rather than the existing simulators running on general purpose CPU-based or GPU-based cluster systems. The rest of the paper is organized as follows. Section II introduces the basis of state vector simulation and four existing
A quantum circuit is a computational routine consisting of a random sequence of gates with up to 38 qubits on the ARCUS and ARCHER supercomputers.

**JUQCS-G** is a GPU-accelerated version of **JUQCS** [6]. JUQCS is a distributed state vector simulator that was used for Google’s quantum supremacy demonstration. JUQCS-G supports distributed simulation with multiple GPUs on multiple nodes. It is parallelized with MPI and optimized to reduce the amount of MPI communication by relabeling global and local qubits after a global qubit operation. The weak and strong scaling of JUQCS-G has been evaluated using a random circuit consisting of a random sequence of gates with up to 38 qubits on the JUWELS Booster supercomputer. In addition, JUQCS-G is used to study the relationship between quantum annealing and QAOA. Note that it is not an open-source simulator.

**Qiskit Aer** is a set of open-source simulators with realistic noise models for Qiskit. Qiskit is an open-source framework for working with noisy quantum computers. Qiskit Aer supports multiple types of simulator backends such as state vector and density matrix. In this work, we use the distributed state vector backend of Qiskit Aer that supports MPI-based distributed simulation with multiple GPUs on multiple nodes [5]. It applies a cache blocking technique to divide an state vector into small blocks and distribute them across multiple GPUs and multiple nodes. It is also optimized to reduce the amount of MPI communication by appropriately inserting swap gates when a given quantum circuit is transpiled. The weak and strong scaling of this implementation has been evaluated using a Quantum Volume model circuit (see Section IV-E for the detail) with up to 34 qubits on a 16-node IBM cluster system.

### III. mpiQulacs

We develop a distributed state vector simulator, mpiQulacs, that is optimized to fully utilize the high memory bandwidth of ARM-based A64FX CPUs and achieve a nearly ideal
scalability to larger-scale quantum circuits. As it is based on Qulacs [7], we first introduce Qulacs and then explain the three unique features of mpiQulacs in this section.

A. Qulacs

Qulacs is one of the fastest state vector simulators running on a single machine [7]. It has four main features to accelerate quantum computing research: (1) It is optimized to achieve fast simulation by fully utilizing the capability of multi-core CPUs and GPUs. (2) It is designed to minimize the overhead of pre- and post-processing for fast simulation of small-scale circuits. (3) It is available on several operating systems such as Linux, Windows, and MAC OS with the interfaces for Python and C++ languages. (4) It meets popular demands in quantum computing research by supporting general quantum operations.

However, the scale of quantum circuits Qulacs can simulate is limited by the capability of a single machine, because the original version of Qulacs does not support distributed simulation on multiple computing nodes. In this work, we target A64FX-based cluster systems and extend Qulacs for distributed simulation on them.

B. MPI parallelization

We apply a similar MPI approach as Intel-QS [3] to extend Qulacs for distributed simulation. With $2^n$ MPI processes, the $2^n$ probability amplitudes in an $n$-qubit state vector are evenly distributed to all the processes. In other words, each process stores $2^m \ (m = n - p)$ amplitudes. All quantum operations on the first $m$ qubits require no MPI communication, while it is required when performing operations on the last $p \ (= n - m)$ qubits. Therefore, the qubits with index $0 \leq q < m$ and ones with index $m \leq q < n$ are called local qubits and global qubits, respectively.

Fig. 1 illustrates an operation scheme of mpiQulacs on a global qubit. Each process divides the $2^m$ probability amplitudes into fixed-size $c$ chunks and reserves a local temporal buffer to temporarily store one chunk to be exchanged. At the step 1, a pair of a process $k$ and process $k + 2^n - m$ exchange the first chunks with each other and store them in their temporal buffers. At the step 2, each process updates the first local chunk with the chunk stored in the temporal buffer. These steps are repeated until all of the $c$ chunks are updated. As this operation scheme is performed by all pairs of corresponding processes, $2^{n+4}$-byte MPI communication is performed in total if probability amplitudes are double precision.

C. Vectorization for A64FX CPU

Since we target A64FX CPUs to run mpiQulacs, one of keys for achieving fast simulation is to fully exploit the potential of each A64FX CPU. It is an ARM-based CPU having a 512-bit Scalable Vector Extension (SVE) engine [9] and 32 GB high-bandwidth memory (HBM2). Thus, we optimize the gate operations of mpiQulacs using this engine to fully utilize the high memory bandwidth of the A64FX CPU.

The gate operations of mpiQulacs are represented as repetitive matrix-vector multiplications as shown in Equation 4. We therefore extend them using 512-bit SVE instructions through the ARM C Language Extension (ACLE) [10]. Since a state vector is represented as an array of double-precision floating point values (i.e., 64-bit values), we optimize each gate operation so that eight values are loaded, processed, and stored simultaneously by an SVE instruction. Consequently, the number of instructions executed in each gate operation is reduced by a factor of eight, and the effective memory bandwidth of each A64FX CPU exceeds 80% of the peak theoretical bandwidth of HBM2 (see Fig. 12 for the detail).

D. Fused-Swap Gate

A key for achieving a high scalability to larger-scale distributed simulation on tens or hundreds of nodes is to minimize the amount of MPI communication required for global qubit operations as shown in Fig. 1, because the inter-node network bandwidth is a bottleneck. One of the straightforward approaches for this goal is to apply gates on as many local qubits as possible by inserting swap gates to a given circuit. A swap gate represented as swap($i$, $j$) is a gate to exchange the probability amplitudes between the $i$-th qubit and $j$-th qubit. If both the qubits are local qubits, the swap operation is performed locally in one process. Otherwise (i.e., if either of them is a global qubit), MPI communication is required.

Fig. 2 shows examples of inserting swap gates to a 4-qubit circuit. We here assume that the original circuit applies Hadamard and RX gates on each qubit and the two higher qubits are global qubits, as shown in the left part of this figure. Since a global qubit operation in an $n$-qubit circuit requires $2^{n+4}$-byte MPI communication, the total communication amount for the original circuit including four global qubit operations is 1,024 ($= 2^{4+4} \times 4$) bytes. Alternatively, we can apply the eight gates on the two local qubits by inserting four swap gates, as shown in the middle part of Fig. 2. As each swap gate involving a global qubit requires
\[ \frac{2^{n+4}}{2} \times \text{byte} \] MPI communication, the four swap gates cause 512-byte \( (\approx \frac{2^{n+4}}{2} \times 4) \) MPI communication in total. In this case, the swapped circuit halves the total amount of MPI communication compared to the original circuit. The distributed implementation of Qiskit Aer introduced in Section II-B applies this approach [5]. However, an important note is that the total amount of MPI communication is \( \frac{2^{n+4}}{2} \times \#\text{swap\_gates} \) bytes in general, which increases linearly as the number of swap gates is increased.

In order to further reduce the amount of MPI communication, we implement a fused-swap gate in mpiQulacs that collectively performs multiple swap operations as one swap operation. It is based on the idea discussed in [8] and designed to fully utilize the bandwidth of InfiniBand. Provided that \( s \) is the number of swap operations to be fused, a fused-swap operation behaves in a similar way to the following code:

```c
fused_swap(p, q, s) {
    for (i = 0; i < s; i++) {
        swap(p+i, q+i);
    }
}
```

Listing 1. Fused-swap behavior

As shown in this code, the fused-swap gate contiguously performs \( s \) swap operations from the \( p \)-th and \( q \)-th qubits. As it does not allow the two operation ranges \( [p : p + s] \) and \( [q : q + s] \) to overlap, each swap operation can be performed independently.

A fused-swap operation exchanges the probability amplitudes within the two operation ranges in a state vector between two corresponding processes at three steps: (1) A gather operation gathers a block of amplitudes into the send buffer of a source process. (2) The block stored in the send buffer is sent to the receive buffer of a target process with MPI, while the receive buffer of the source process receives a block sent from the send buffer of the target process. (3) A scatter operation scatters the amplitudes stored in the receive buffer to appropriate positions in a state vector. These three steps are repeated until all of the amplitudes within the two operation ranges are exchanged with all corresponding target processes.

The total amount of MPI communication in a circuit including fused-swap gates is \( 2^{n+4} \times (1 - \frac{1}{2^n}) \times \#\text{fused\_swap\_gates} \) bytes. The right part of Fig. 2 shows an example of inserting two fused-swap gates to the 4-qubit circuit, where the total amount of MPI communication is 384 bytes \( (\approx 2^{n+4} \times (1 - \frac{1}{2^n}) \times 2) \). It is 25% lower than that of the swapped circuit. Although the examples in Fig. 2 are tiny, the benefit of the fused-swap gate is more significant for larger-scale circuits. If \( s \) is large (e.g., 4 or more) and a fused-swap gate fuses \( s \) swap gates, we can bound the total amount of MPI communication to \( \approx 2^{n+4} \times \frac{\#\text{swap\_gates}}{s} \) bytes.

### E. Double Buffering for Fused-Swap

A naïve implementation of a fused-swap operation sequentially performs the procedure of a gather operation, MPI communication, and a scatter operation, as shown in the upper part of Fig. 3. To reduce the processing time of a fused-swap operation, we apply double buffering, which is a well-known optimization technique to overlap computation and communication. The lower part of Fig. 3 illustrates our double buffering implementation. We prepare two pairs of send/receive buffers and overlap the \((j-1)\)-th scatter operation and the \((j+1)\)-th gather operation with \( j \)-th MPI communication. In addition, we also overlap the last scatter operation of the \( i \)-th target process and the first MPI communication of the \((i+1)\)-th target process. Consequently, the double buffering implementation reduces the processing time of a fused-swap operation by hiding the processing times of gather and scatter operations.

### IV. Evaluation

In this section, we evaluate the performance of mpiQulacs on our 64-node A64FX-based cluster system named Todoroki and compare the results with those of Intel-QS, JUQCS-G, and Qiskit Aer reported in corresponding papers. Moreover, we evaluate the performance of three open-source distributed simulators (Intel-QS, QuEST, and Qiskit Aer) by ourself on the ABCI supercomputer and compare those results with that of mpiQulacs evaluated on Todoroki. We first explain the configuration of Todoroki and evaluation metrics and then show the comparison results.

#### A. Todoroki: 64-node A64FX-based cluster system

We construct a new 64-node A64FX-based cluster system named Todoroki to evaluate mpiQulacs. TABLE I summarizes its configuration. It consists of 64 PRIMEHPC FX700 servers, each of which has a 48-core ARM-based A64FX CPU. This CPU is also used in the world’s top Fugaku supercomputer. The noticeable feature of this CPU is 32 GB high-bandwidth memory (HBM2), whose theoretical peak bandwidth is 1,024 GB/s. This is an order of magnitude higher than that of widely used DDR4 DRAM. All of the 64 nodes are interconnected with InfiniBand EDR in a fat tree topology.

#### B. Evaluation Metrics

To compare mpiQulacs with other existing distributed simulators, we measure the execution times of several quantum benchmark circuits. Note that each circuit is executed six times and we report the average execution time of the last five runs.
(i.e., the first run is omitted). The detail of each circuit is described in each of the following sections.

In addition, we define a novel metric, quantum Q/F ratio (QBF), that indicates the execution efficiency of state vector simulation running on cluster systems and use it to compare mpiQulacs running on Todoroki and the existing simulators running on HPC systems. It is defined as

$$QBF = \frac{2^n \times \text{gates}}{\text{exetime} \times \text{totalFLOPS}}$$

where \( n \), \( \text{gates} \), and \( \text{exetime} \) are the number of qubits, the number of gates, and the execution time of a given quantum circuit, respectively. \( \text{totalFLOPS} \) is the total theoretical peak FLOPS of all computing units (i.e., CPUs or GPUs) used to execute the circuit. According to [11], \( 2^n \) represents the amount of memory traffic in bytes to read and write an entire state vector in one gate operation. Thus, the product of \( 2^n \) and \( \text{gates} \) corresponds to the total amount of memory traffic in bytes for the circuit. On the other hand, the product of \( \text{exetime} \) and \( \text{totalFLOPS} \) corresponds to the estimated number of double-precision floating point operations executed by CPUs or GPUs for the target circuit. The QBF is inspired by Q/F ratio, which is a metric widely used for HPC systems, but has a different meaning. A higher QBF means that a large-scale quantum circuit can be simulated in a shorter time with less computational hardware resource.

C. Comparison with Intel-QS

We measure the processing time of a 1-qubit gate of mpiQulacs and compare it with that of Intel-QS reported in [3]. The weak and strong scaling of Intel-QS has been evaluated on the 6,480-node SuperMUC-NG HPC system. TABLE II summarizes the configuration of this system. Each node has two sockets of Xeon® Platinum 8174 processors and 96 GB DDR4 DRAM. We calculate the theoretical peak FLOPS of each CPU by dividing the total theoretical peak FLOPS of the entire system by the total number of CPUs (= 26.3 PFLOPS / 12,960 CPUs). Moreover, we calculate the theoretical peak memory bandwidth based on the memory type and the number of memory channels supported by the CPU (= 2666 MHz \( \times 8 \) bytes \( \times 6 \) channels).

The 1-qubit gate time of Intel-QS has been measured using a 1-qubit gate defined by a random 2x2 matrix [3]. We therefore measure the processing time of an RX-gate, which is also defined by a 2x2 matrix, with mpiQulacs running on Todoroki. Fig. 4 plots the 1-qubit gate time when applied on each qubit of mpiQulacs running on Todoroki and Intel-QS running on SuperMUC-NG.

Fig. 4a shows the weak scaling results of both the simulators, where the number of qubits is set to 30 per CPU and incremented with doubling the number of CPUs. Both mpiQulacs and Intel-QS achieve ideal weak scaling because the 1-qubit gate time is not changed (three blue and orange
D. Comparison with JUQCS-G

We then compare mpiQulacs with JUQCS-G evaluated on the JUWELS Booster supercomputer. TABLE III summarizes the configuration of the system. It consists of 936 nodes, each of which has two sockets of AMD EPYC™ 7402 processors with 512 GB DDR4 DRAM and four NVIDIA A100 GPUs. This GPU contains 40 GB HBM2 as well as the A64FX CPU, and its theoretical peak memory bandwidth is 1,555 GB/s. The major difference of the GPU from the A64FX CPU is over 6x higher FLOPS.

![Fig. 5. Quantum B/F ratio based on the strong scaling results of mpiQulacs running on Todoroki and Intel-QS running on SuperMUC-NG.](image)

The weak and strong scaling of JUQCS-G has been evaluated using an Hadamard benchmark circuit [6], where eleven Hadamard gates are repeatedly applied on each qubit. Thus, we also implement it for mpiQulacs. Fig. 6 plots the computation time and communication time for this circuit with mpiQulacs running on Todoroki and JUQCS-G running on JUWELS Booster. We obtain the results of JUQCS-G from [6], where the normalized execution time with respect to the number of gates in the 32-qubit circuit is reported. We therefore calculate the absolute execution time by multiplying the normalized time by a corresponding normalization factor and plot it in Fig. 6. For instance, the normalization factor of the 36-qubit circuit is $1.125 (=\frac{36 \times 11}{32 \times 11})$. For mpiQulacs, we insert fused-swap gates that involves all global qubits (i.e., $s = \#\text{global qubits}$) in the circuit so that the amount of MPI communication is minimized and the final state vector is consistent to the original circuit. Note that the communication time of mpiQulacs includes the processing time of fused-swap gates in addition to the MPI communication time.

![Fig. 6a shows the weak scaling results of both the simulators. The maximum numbers of qubits on one A64FX CPU and one A100 GPU are 30 and 31, respectively. We therefore start at 32 qubits with four A64FX CPUs for mpiQulacs and with two A100 GPUs for JUQCS-G and increment the number of qubits up to 36 while doubling the number of CPUs or GPUs. TABLE IV summarizes the configurations of Todoroki and JUWELS Booster when the number of qubits is 36 and shows that the theoretical performance of Todoroki is not significantly different from that of JUWELS Booster.](image)

| # of nodes | 936 |
|------------|-----|
| CPU        | AMD EPYC™ 7402 |
| # of CPUs per node | 2 |
| # of cores per CPU | 24 |
| CPU memory | 512 GB DDR4 DRAM |
| GPU        | NVIDIA A100 |
| # of GPUs per node | 4 |
| GPU memory | 40 GB HBM2 |
| Theoretical peak FLOPS per GPU | 19.5 TFLOPS |
| Theoretical peak memory BW per GPU | 1,555 GB/s |
| GPU interconnect | NVLink® 3 |
| Interconnect | InfiniBand HDR |
| # of HCAs per node | 4 |
| Theoretical peak network BW per node | 100 GB/s |
| OS         | CentOS |

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Fig. 6. The execution time of Hadamard benchmark circuit with mpiQulacs running on Todoroki and JUQCS-G running on JUWELS Booster.

TABLE IV
THE CONFIGURATIONS OF TODOROKI AND JUWELS BOOSTER FOR THE 36-QUBIT HADAMARD BENCHMARK CIRCUIT

|                        | Todoroki | JUWELS Booster |
|------------------------|----------|-----------------|
| # of nodes             | 64       | 8               |
| # of CPUs or GPUs      | 64 CPUs  | 32 GPUs         |
| Total theoretical FLOPS| 198 TFLOPS| 624 TFLOPS (x3.15) |
| Total theoretical memory BW | 64 TB/s | 49 TB/s (x0.76) |
| Total theoretical network BW | 800 GB/s | 800 GB/s (x1.00) |

* The values in ( ) indicates the related values to Todoroki.

Fig. 7. Quantum B/F ratio based on the strong scaling results of mpiQulacs running on Todoroki and JUQCS-G running on JUWELS Booster.

The computation time of mpiQulacs is almost half of that of JUQCS-G even though the total FLOPS for mpiQulacs is 3.15x lower than that for JUQCS-G. This result implies that state vector simulation is memory bound, and the high memory bandwidth of the A64FX fits this requirement.

Fig. 6 shows the strong scaling results, where the number of CPUs or GPUs is increased from 16 to 64 with fixed 34 qubits. The computation time of mpiQulacs is comparable to that of JUQCS-G when the numbers of CPUs and GPUs are same. This result again demonstrates that high memory bandwidth is a key for fast state vector simulation.

Fig. 7 plots the QBF of both the simulators based on the strong scaling results shown in Fig. 6b. mpiQulacs achieves an order of magnitude higher QBF than JUQCS-G. This is because the FLOPS of one A64FX CPU is over 6x lower than that of one A100 GPU, whereas the execution time is comparable. This result means that the FLOPS of the A64FX CPU is sufficient for state vector simulation. The QBF of both the simulators is almost constant because the execution time is halved by doubling the number of CPUs or GPUs.

Summary of comparison with JUQCS-G: mpiQulacs outperforms JUQCS-G especially for large-scale simulation by minimizing MPI communication. In addition, mpiQulacs enables one A64FX CPU to achieve comparable performance to one A100 GPU, leading to an order of magnitude higher QBF.

E. Comparison with Qiskit Aer

Next, we compare mpiQulacs with the distributed state vector backend of Qiskit Aer that supports distributed simulation with multiple GPUs on multiple nodes [5] as introduced in Section II-B. The weak and strong scaling of this backend has been evaluated on a 16-node IBM GPU cluster system. TABLE V summarizes its configuration. Each node has two sockets of Power9 processors with 512 GB DDR4 DRAM and six NVIDIA V100 GPUs. This GPU contains 16 GB HBM2, whose theoretical peak bandwidth is 900 GB/s.

A Quantum Volume model circuit has been used for the evaluation of Qiskit Aer [5]. Quantum Volume (QV) is a

except the x3.15 lower total FLOPS. We can see in Fig. 6a that mpiQulacs outperforms JUQCS-G consistently across the varied number of qubits. Interestingly, the performance difference between them gets more significant as the number of qubits is increased and reaches to over twice with 36 qubits. The fused-swap gates of mpiQulacs mainly contribute to this result by minimizing the amount of MPI communication. In fact, the communication time of mpiQulacs does not increase linearly with the increased number of qubits. On the other hand, since JUQCS-G requires MPI communication for all global qubit operations, its communication time increases linearly. The computation time of mpiQulacs is almost half of that of JUQCS-G even though the total FLOPS for mpiQulacs is 3.15x lower than that for JUQCS-G. This result implies that state vector simulation is memory bound, and the high memory bandwidth of the A64FX fits this requirement.

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A Quantum Volume model circuit has been used for the evaluation of Qiskit Aer [5]. Quantum Volume (QV) is a
TABLE V

| Cluster node                     | IBM Power System AC922 |
|----------------------------------|-------------------------|
| # of nodes                       | 16                      |

| CPU                              | POWER9                  |
|----------------------------------|-------------------------|
| # of CPUs per node               | 2                       |
| # of cores per CPU               | 21                      |
| CPU memory                       | 512 GB DDR4 DRAM        |

| GPU                              | NVIDIA V100             |
|----------------------------------|-------------------------|
| # of GPUs per node               | 6                       |
| GPU memory                       | 16 GB HBM2              |
| Theoretical peak FLOPS per GPU   | 7.0 TFLOPS               |
| Theoretical peak memory BW per GPU| 900 GB/s                |
| GPU interconnect                 | NVLink® 2               |

| Interconnect                     | InfiniBand EDR          |
|----------------------------------|-------------------------|
| Theoretical peak network BW per node | 12.5 GB/s               |

| OS                               | RHEL Server 7.6         |
|----------------------------------|-------------------------|
| Compiler                         | GCC 8.3.0                |
| CUDA Toolkit                     | CUDA 10.1                |
| MPI                              | IBM Spectrum MPI 10.3.1  |

Single-number metric to measure the performance of near-term quantum computers [12]. The model circuit for QV measurement consists of multiple layers of random permutations of qubit labels, followed by random 2-qubit dense-matrix gates. We implement this circuit for mpiQulacs according to the source code on Github [13] and insert fused-swap gates that involves all global qubits (i.e., \( s = \# \text{global qubits} \)) so that MPI communication is minimized. The depth (i.e., the number of layers) of the model circuit is set to 10. Fig. 8 plots the execution time of the QV model circuit with mpiQulacs running on Todoroki and Qiskit Aer running on the GPU cluster system. The results of Qiskit Aer is obtained from [5].

Fig. 8a shows the weak scaling results of both the simulators. We here set the number of qubits to 30 per node and increment it with doubling the number of nodes. Qiskit Aer outperforms mpiQulacs when the 30-qubit circuit is executed on a single node. This is because Qiskit Aer uses six GPUs while mpiQulacs uses only one CPU. On the other hand, mpiQulacs significantly outperforms Qiskit Aer with more than 31 qubits. mpiQulacs achieves a high weak scalability to the number of qubits by reducing MPI communication with the fused swap gates. In contrast, Qiskit Aer increases the execution time linearly as the number of qubits is increased.

Fig. 8b shows the strong scaling results, where the number of nodes is varied from 1 to 64 with fixed 30 qubits. Note that Qiskit Aer uses six GPUs for the single-node simulation but only one GPU per node for the multi-node simulation. This graph shows that mpiQulacs outperforms Qiskit Aer when the numbers of A64FX CPUs and V100 GPUs are same (i.e., on two or more nodes). In particular, mpiQulacs achieves over 2x higher performance when the number of node is 16.

Fig. 9 plots the QBF of both the simulators based on the strong scaling results shown in Fig. 8b. mpiQulacs achieves higher QBF than Qiskit Aer consistently across the varied number of nodes. The difference between them is especially significant (8x) when the number of node is one, because a single A64FX CPU (3.1 TFLOPS) achieves the 60% performance of six GPUs (42.0 TFLOPS in total).

**Summary of comparison with Qiskit Aer:** mpiQulacs achieves a high weak/strong scalability by minimizing MPI communication and outperforms Qiskit Aer significantly for large-scale simulation on multiple nodes. The QBF of mpiQulacs running on Todoroki is much higher than that of Qiskit Aer running on the GPU cluster system.

F. Evaluation using Quantum Software Benchmark

Finally, we evaluate three existing open-source distributed simulators (Intel-QS, QuEST, and Qiskit Aer) by ourself on the AI Bridging Cloud Infrastructure (ABCI) supercomputer and compare the results with that of mpiQulacs evaluated on Todoroki. We run QuEST only with CPUs because it does not support the distributed simulation using multiple GPUs. Unfortunately, we cannot evaluate JUQCS-G by ourself because it is not an open-source simulator.

ABCI is an open supercomputer operated by National Institute of Advanced Industrial Science and Technology (AIST). Although two types of computing nodes called V-node and A-
node are available on it, we only use the A-nodes because they have more high-end hardware resources than the V-nodes. TABLE VI summarizes the configuration of the A-nodes. There are 120 A-nodes, each of which has two sockets of Xeon® Platinum 8360Y processors with 512 GB DDR4 DRAM and eight NVIDIA A100 GPUs. The specification of the A100 GPU is identical to that equipped on JUWELS Booster, except the GPU counts per node. We calculate the theoretical peak FLOPS of each CPU by subtracting the total FLOPS of eight A100 GPUs per node from the total FLOPS of each node and dividing the difference by the number of CPUs per node (= (160.8 TFLOPS - 19.5 TFLOPS × 8) / 2) [14]. In addition, we calculate the theoretical peak bandwidth of DDR4 DRAM based on the memory type and the number of memory channels supported by the CPU (= 3200 MHz × 8 bytes × 8 channels).

To compare mpiQulacs with the three existing simulators, we use the Quantum Software Benchmark (QSB) circuit [15], which is reviewed by the developers of representative simulators such as Qiskit and Cirq and used for the evaluation of the original version of Qulacs [7]. This circuit consists of ten sets of a rotation layer and a CNOT layer, followed by one more rotation layer. In a rotation layer, random RZ, RX, and RZ gates are applied on each qubit. In a CNOT layer, CNOT gates are applied on the \(i\)-th target qubit and the \((i + 1 \mod n)\)-th control qubit for \((0 \leq i < n)\) where \(n\) is the number of qubits. For mpiQulacs, we insert fused-swap gates that involves all global qubits (i.e., \(s = \#\text{global qubits}\)) in the circuits so that the amount of MPI communication is minimized and the final state vector is consistent to the original circuit.

Fig. 10 plots the execution time of the QSB circuit with mpiQulacs running on Todoroki and Intel-QS, QuEST, and Qiskit Aer running on ABCI.

Fig. 10a shows the weak scaling results of the four simulators. We set the number of qubits to 30 per CPU and 31 per GPU and increment it with doubling the number of CPUs or GPUs. The performance of Intel-QS and QuEST is comparable because they use only CPUs. They increase the execution time linearly along with the number of qubits due to the increase in the amount of MPI communication. In contrast, Qiskit Aer
that is accelerated with GPUs significantly outperforms Intel-QS and QuEST. It achieves nearly ideal weak scaling with up to 34 qubits because eight GPUs on a single node are fully utilized. However, it steeply increases the execution time with 35 and 36 qubits due to inter-node MPI communication. In these cases, we run Qiskit Aer on 16 nodes and 32 nodes with a single GPU per node because the multi-node simulation with multiple GPUs per node is much slower. Interestingly, mpiQulacs achieves the comparable performance to Qiskit Aer with up to 34 qubits and sustains nearly ideal weak scaling with 35 qubits or more. The vectorization for A64FX CPUs and fused-swap gates of mpiQulacs contribute to this result.

Fig. 10b shows the strong scaling results of the four simulators with the log-scaled y-axis. We here fix the number of qubits to 30 and vary the numbers of CPUs and GPUs from 2 to 64. mpiQulacs, Intel-QS, and QuEST achieve nearly ideal strong scaling, and mpiQulacs outperforms Intel-QS and QuEST significantly. Qiskit Aer outperforms mpiQulacs with up to eight GPUs, because Qiskit Aer uses multiple GPUs on a single node while mpiQulacs uses multiple nodes. In contrast, mpiQulacs outperforms Qiskit Aer when inter-node MPI communication is required.

Fig. 11 shows the QBF of the four simulators based on the strong scaling results shown in Fig. 10b. Interestingly, the QBF of GPU-accelerated Qiskit Aer is comparable or lower compared to that of CPU-based Intel-QS and QuEST. This is because the total FLOPS of GPUs used by Qiskit Aer is much higher than that of CPUs used by Intel-QS and QuEST, although Qiskit Aer significantly outperforms Intel-QS and QuEST as shown in Fig. 10b. In contrast, mpiQulacs achieves much higher QBF than the other three simulators owing to the comparable performance to Qiskit-Aer and the comparable total FLOPS to Intel-QS and QuEST. This result means that mpiQulacs running on A64FX-based Todoroki fits the requirements of distributed state vector simulation.

To analyze the benefit of the vectorization for the A64FX CPU of mpiQulacs, we execute the 30-qubit QSB circuit in three ways: Intel-QS with a single Xeon CPU on ABCI, Intel-QS with a single A64FX CPU on Todoroki, and mpiQulacs with a single A64FX CPU on Todoroki. Fig. 12 shows the execution time of the QSB circuit on the left y-axis and the effective memory bandwidth on the right y-axis. The effective memory bandwidth is calculated by dividing the total amount of memory traffic in bytes (\(= 2^{30+5 \times \# \text{gates}}\)) by the execution time. We can see in this figure that the performance of Intel-QS with the Xeon CPU is limited by the bandwidth of DDR4 DRAM. Thus, Intel-QS with the A64FX CPU reduces the execution time by 37% by utilizing the high bandwidth of HBM2. However, in this case, the effective memory bandwidth is far from the theoretical peak bandwidth of HBM2. In contrast, mpiQulacs with the A64FX CPU achieves over 80% of the theoretical peak bandwidth of HBM2 and thus further reduces the execution time by 69%. This result demonstrates that mpiQulacs brings out the potential of the A64FX CPU.

Summary of evaluation using QSB: mpiQulacs running on Todoroki achieves nearly ideal weak/strong scaling and significantly outperforms Intel-QS, QuEST, and Qiskit Aer running on ABCI for large-scale simulation on multiple nodes. The QBF evaluation shows that mpiQulacs running on Todoroki fits the requirements of distributed state vector simulation. Moreover, we demonstrate that mpiQulacs fully utilizes the high memory bandwidth of the A64FX CPU.

V. CONCLUSION AND FUTURE WORK

We develop mpiQulacs that is a fast and scalable distributed state vector simulator to accelerate the development of emerging quantum applications. It is optimized to fully utilize the high memory bandwidth of A64FX CPUs and supports a fused-swap gate to minimize the amount of MPI communication. We evaluate weak and strong scaling of mpiQulacs on the 64-node A64FX-based Todoroki cluster system using several quantum benchmark circuits. By comparing mpiQulacs with existing distributed state vector simulators, we show that mpiQulacs outperforms them for large-scale simulation on tens of nodes and achieves nearly ideal weak and strong scaling. Moreover, the evaluation in terms of quantum B/F ratio (QBF) demonstrates that mpiQulacs running on Todoroki fits the requirements of distributed state vector simulation.
We are currently constructing another 1024-node A64FX-based cluster system, where mpiQulacs can simulate up to 40-qubit quantum circuits. We will use it to conduct research on quantum applications and further accelerate the development of real quantum applications. The nearly ideal scalability of mpiQulacs to larger-scale simulation will be more remarkable on this system. We also believe that the high QBF of mpiQulacs will contribute to lower energy consumption and/or lower system cost for such large-scale state vector simulation.

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