The Improvement Switching Technique for High Step-Up DC-DC Boost Converter

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Abstract: This paper proposes the non-isolated DC-DC converter with high boost ratios and efficiency. We suggest boosting methods including voltage multiplier cells or coupled inductors. However, both techniques have a limited constant voltage multiplier coefficient according to the fixed configuration. Therefore, in the proposed method, we change the multiplier factor (as the number of activity levels) and combine it with the turn of the appropriate duty cycle; these factors are considered at the same time in order to increase the energy conversion efficiency and expand the control area of the duty cycle. A mathematical analysis of the losses of the components in operation modes shows that the boost ratio and efficiency are functions of the number of activity levels and duty cycle. Therefore, this paper proposes an algorithm for tracking the activity levels and duty cycle in order to obtain the maximum efficiency. The simulations produced with the Powersim-PSIM software, and the experiments with load capacities of 250 W, 500 W and 1000 W, boosting the ratio by more than ten times, were conducted in order to clarify the capabilities of the proposed configuration.

Keywords: DC-DC converter; boost ratio; activity levels; duty cycle; efficiency

1. Introduction

High step-up DC-DC converters have various applications, such as uninterrupted power supply-UPS, renewable energy systems, fuel cell systems, and hybrid electric vehicles [1–9]. They can be classified into two types: isolation and non-isolation converters [10–12]. Isolated DC-DC converters have some disadvantages, such as high eddy current and voltage stress on the output diode [12]. When applications do not have the required isolation, non-isolated DC-DC converters offer a more straightforward and flexible solution for boosting [10,11].

Conventional DC-DC converters include an inductor, a switch and a diode, as shown in Figure 1a. For a high boost ratio, it operates at an extreme duty cycle $D$ (to units). The boost ratio may be higher if more conventional boost converters cascade, as shown in Figure 1b,c. Theoretically, these cascading converters are another technique for obtaining a higher boost ratio and lower conductive losses without an extreme duty cycle. However, these converters still suffer from high voltage stress and the significant input current ripple of DC power [13].

To reduce the input current ripple, a two-phase interleaved boost converter with parallel inputs and parallel boosters is proposed, as shown in in Figure 1d. The switches $S_1$ and $S_2$ in Figure 1d are activated alternately so that the input current’s ripple is lower [14].
In recent years, studies of high step-up DC-DC converters have been published with improved topologies to reduce the input ripple current (voltage lift cell (VLC) and interleaved input), incorporating voltage multiplier cells or coupled inductors [15–17], as shown in Figure 1e, Figure 2a,b. Although it has the advantages of high voltage gain, the configuration shown in Figure 1e has a larger size and weight [18]. Another improved technique which uses a voltage multiplier circuit is illustrated in Figure 2a,b.

The voltage multiplier has some of the diodes and capacitors. Theoretically, it is possible to use more capacitors and diodes in order to obtain a larger voltage boost ratio. Therefore, this circuit can increase the output boost at a low duty cycle. According to [16], the boost ratio can be determined as

$$B = \frac{U_L}{E} = \frac{2N}{1 - D}$$

Another improved configuration, as shown in Figure 2b, with the voltage lift cell (VLC) includes two inductors L1, L2, two diodes D1, D2 and a capacitor C1, replacing the interleaved input. In this
structure, not only is the number of switches reduced, but the voltage boost ratio is also twice as high, as shown in the formula (2).

\[ B = \frac{U_L}{E} = \frac{4N}{1 - D} \] (2)

With Cockcroft–Walton cells, the energy is transferred between the capacitors (for example, from \( C_3 \) to \( C_2 \) Figure 2b) in a short period of time so that the power loss on the capacitor is high while the conversion efficiency reduces.

Using VLCs reduces the number of switches but increases the current that passes through them. Therefore, the loss of the switch with the VLC is greater than the interleaved input.

Now, the improved converters with a high boost ratio and a low ripple current are shown in Table 1.

| No. | Configuration                        | Switches | Capacitors | Diodes | Boost               |
|-----|--------------------------------------|----------|------------|--------|---------------------|
| 1   | interleaved input and coupled inductor | 2        | 4          | 4      | \( \frac{2(N + 1)}{1 - D} \) |
| 2   | interleaved input and multiplier cell | 2        | 5          | 5      | \( \frac{2N}{1 - D} \) |
| 3   | VLC input and multiplier cell         | 1        | 4          | 5      | \( \frac{4N}{1 - D} \) |

This shows that the voltage multiplier ratio \( N \) is not changed in operation. Thus, the only way to change the boost ratio is to regulate the duty cycle \( D \). As a result of this limitation, there are not many flexibilities of control and implementation optimizations.

Thus, this paper proposes an improved DC-DC converter topology with an interleaved input, high boost ratio and flexible control according to the optimized functions and fewer multipliers. The two parameters that can be regulated to achieve the desired voltage boost are the duty cycle \( D \) and the voltage multiplier \( N \).

2. The Improvement Switching Technique

This paper proposes an improved DC-DC converter that uses the cascaded traditional boost circuit, with a high voltage boost ratio, wide control range and optimal control. Moreover, a new control method is shown with an almost linear and stable output voltage. The control technique is flexible because of the wide control range with two variants of the duty cycle \( D \) and the voltage multiplier \( N \).

Figure 3 shows that the proposed converter has some of the basic cascaded levels such as an inductor, MOSFET, diode and capacitor. The inductor is the energy store that is magnetized during turn-on time and demagnetized during turn-off time; the diode is used to direct the currents, and the capacitor acts to charge and discharge the energy.

2.1. Principles

Set \( N_{\text{max}} \) is the number of levels in the configuration, which means that \( N_{\text{max}} \) will be four with the converter, as shown in Figure 3a. The three stages of the converter are described in Figure 3b–d. Figure 4 shows the waveform of the voltage and current on switches, inductors and capacitors in the switching cycle. The first level always acts while the other might be active or not, depending on the status of the switches. There are four operation modes in the converter, as shown in Table 2.
### Table 2. Active switches involved in the modes of the converter.

| Mode | 1          | 2          | 3          | 4          |
|------|------------|------------|------------|------------|
| PWM signals | S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, S<sub>4</sub> | S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub> | S<sub>1</sub>, S<sub>2</sub> | S<sub>1</sub> |
| Turn off switch | None | S<sub>4</sub> | S<sub>3</sub> to S<sub>4</sub> | S<sub>2</sub> to S<sub>4</sub> |

**Figure 3.** Proposed converter (a), the operating states: 1 (b), 2 (c) and 3 (d).
Figure 4. The waveform of the gate voltages (a), the voltage and current on switches (c-f), inductors (b), and capacitors (g).

This section analyzes the first mode with full activity levels. Figure 4 shows the established waveforms in the switching cycle of the converter in the first mode. In this case, all of the levels operate together. The control cycle of S1 is the same as S3 and the phase shifts by 180° between S2 and S4. In the first mode, there are three operating states, which are shown in Table 3.

Table 3. The operation states of the circuit when all of the levels are active.

| Stage | Switch on | Switch off | Time  | Result |
|-------|-----------|------------|-------|--------|
| 1     | S1, S2, S3, S4 | D1, D2, D3, D4 | t1–t2 | All inductors store energy. Capacitor C4 discharges to the load |
| 2     | S2, S3, D1, D3 | S1, S4, D2, D4 | t2–t3 | Capacitors C1 and C3 charged, capacitor C2 discharged |
| 3     | S1, S3, D2, D4 | S2, S4, D1, D5 | t3–t4 | Capacitors C2 and C3 charged, capacitors C1 and C5 discharged |

In stage 1, from t1 to t2, the MOSFETs turn on, the diodes turn off and four inductors are magnetized by the input source (Figure 3b). Therefore, the current that is charged into the inductor linearly increases and can be calculated using the following formula (3, 4). The output capacitor (C4) supplies energy to the load.

\[
i_{L1}(t) = I_{L1}(t_0) + \frac{V_{\text{in}}}{L_1} (t - t_0) \quad \text{and} \quad i_{L3}(t) = I_{L3}(t_0) + \frac{V_{\text{in}}}{L_3} (t - t_0) \tag{3}
\]

\[
i_{L2}(t) = I_{L2}(t_0) + \frac{V_{\text{in}}}{L_2} (t - t_0) \quad \text{and} \quad i_{L4}(t) = I_{L4}(t_0) + \frac{V_{\text{in}}}{L_4} (t - t_0) \tag{4}
\]

State 2 [t2–t3]: the two switches S1 and S3 turn off while the remaining switches (S2, S4) still turn on (Figure 3c). The capacitor C1 is charged by the energy stored in L1 and the power source, similar to the C3 in level 3. The inductor in levels 2 and 4 still magnetizes so that the current that passes
through $S_2$ and $S_3$ is the sum of the inductor’s magnetized current and the capacitor’s charging current. The output capacitor ($C_4$) supplies energy to the load:

$$V_{C1} = V_{S1} = V_{S3} = \frac{V_{in}}{1 - D}$$

$$V_{C3} = V_{C2} + \frac{V_{in}}{1 - D} = 3 \frac{V_{in}}{1 - D}$$

State 3 [$t_3$–$t_1$]: this state is the same as state 2 with the status of switches and capacitors on the reverse. Both capacitors $C_1$ and $C_3$ transfer energy to capacitors $C_2$ and $C_4$, respectively. The output capacitor $C_4$ still supplies the load. In this state, the $S_1$ current is only the $L_1$’s magnetized current.

$$V_{S2} = V_{S4} = \frac{V_{in}}{1 - D}$$

$$V_{C2} = 2 \frac{V_{in}}{1 - D}$$

$$V_{C4} = V_{C3} + \frac{V_{in}}{1 - D} = 4 \frac{V_{in}}{1 - D}$$

Consequently, the voltage boost factor depends on the activity levels ($N$). The ideal voltage boost ratio $B^*$ can be determined by the formula (10),

$$B^* = \frac{V_{C0}}{V_{in}} = \frac{N}{1 - D} \frac{I_{in}}{I_o} \text{ where } N = 1, 2, ..., N_{max}$$

The switch voltage stress (at the current level) is:

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = \frac{V_{in}}{1 - D}$$

The voltage across on the diode can be calculated based on the analysis of stage 2 and stage 3:

$$\begin{cases} 
V_{D1} = \frac{V_{in}}{1 - D} \\
V_{Di} = iV_{in} \frac{1}{1 - D} \text{ khi } i < N \\
V_{Di} = 0 \text{ khi } i > N 
\end{cases}$$

2.2. Power Loss Analysis

The resistors $R_D$, $R_L$, $R_S$ can be described as the resistance of the turn-on diode, the inductor and the turned-on switch.

2.2.1. Power Loss in Diode:

All diodes are turned on in the $(1 - D)T$ period with the current the same as the level current at the corresponding stage. Therefore, the conductive losses on the diode can be calculated by:

$$\Delta P_D = N(1 - D)R_D I_o^2 = NR_D \frac{I_o^2}{1 - D}$$

where $N$ is the number of the activity levels and $I_o$ is the load current.

2.2.2. Power Loss in Inductor:

The power losses in the inductors consist of two main losses: copper and core losses. The sum of the two losses can be represented by a resistor. The currents that pass through the inductor in all stages can be presented as the mean current on the level. Therefore, the losses in the $N$ inductors can be calculated as:
\[ \Delta P_L = N R_L I_L^2 = N R_L \frac{I_o^2}{(1-D)^2} \]  \hspace{1cm} (14)

2.2.3. Power Loss in the Switch:

The power loss in switch \( S_1 \) can be calculated similarly to the traditional boost circuit using the formula (15).

\[ \Delta P_{S1} = D R_S I_{S1}^2 = D R_S \frac{I_o^2}{(1-D)^2} \]  \hspace{1cm} (15)

At levels 2 to 4, the current on the turned-on switch is also the current on the inductor in stage 1. Consequently,

\[ \Delta P_{S(i,(S1))} = (2D - 1)R_S I_{S(i,(S1))} = (2D - 1)R_S \frac{I_o^2}{(1-D)^2}, i = 2 \ldots 4 \]  \hspace{1cm} (16)

However, in stages 2 and 3, during \((1-D)T\), the switch current is the magnetization and charge of the front level capacitor (Figure 4). Therefore, the power losses in the switches in these stages can be calculated, respectively, as:

\[ \Delta P_{S(i,(S2,3))} = (1-D)R_S I_{S(i,(S2,3))} = (1-D)R_S \frac{4I_o^2}{(1-D)^2} = R_S \frac{4I_o^2}{(1-D)}, i = 2 \ldots 4 \]  \hspace{1cm} (17)

Consequently, the total loss in a switch \((S_2, S_3 \text{ or } S_4)\) in a cycle is:

\[ \Delta P_{S(i)} = (3 - 2D)R_S \frac{I_o^2}{(1-D)^2} \]  \hspace{1cm} (18)

2.2.4. Power Loss in the Output Capacitor

The output capacitor \( (C_4) \) serves not only to store energy but also to supply it to the load. The output capacitor current has two components, namely the charge and discharge currents. The \( C_4 \) discharge current is the load current, and the charge current is the difference between the last level and the output current. Therefore, this can be calculated as (19):

\[ \Delta P_{C_4} = D R_C \frac{I_o^2}{1-D} \]  \hspace{1cm} (19)

2.2.5. Losses in the Level Capacitor:

The level capacitors \((C_1 \text{ to } C_3)\) operate in stages 2 and 3 only. Both the charge and discharge currents of them are involved in the inductor current sequence. Thus, the power losses to the level capacitor can be calculated as (20)

\[ \Delta P_{C_l} = 2R_C \frac{I_o^2}{1-D} \]  \hspace{1cm} (20)

According to [19], conductive losses are low when switching frequencies below 100 kHz, which can lead to the switching losses being ignored. Consequently, the total power loss in the proposed circuit can be calculated by the following:

\[ \Delta P = \Delta P_L + \Delta P_S + \Delta P_D + \Delta P_C \]

\[ = \frac{N R_L}{(1-D)^2} I_o^2 + \frac{D + (N-1)(3-2D)R_S}{(1-D)^2} I_o^2 + \frac{N_{max} R_D}{1-D} I_o^2 + \frac{D + 2(N-1)R_C}{1-D} I_o^2 \]  \hspace{1cm} (21)

2.3. Control Technology to Minimize Power Loss
In order to maximize the conversion efficiency, it is necessary to determine the correct values of \( N \) and \( D \) for minimizing the power losses defined by the formula (21) on the conditions in (22).

\[
\begin{align*}
1 \leq N & \leq N_{\text{max}} (N \in \mathbb{N}) \\
0.1 \leq D & \leq 0.8 \text{ if } N = 1 \\
0.5 \leq D & \leq 0.8 \text{ if } N > 1
\end{align*}
\]  

The formula (21) is rewritten as below.

\[
\Delta P = I_0^2 \left( \frac{N R_L}{(1-D)^2} + \frac{D + (N-1)(3-2D)R_S}{(1-D)^2} + \frac{N_{\text{max}} R_D}{1-D} + \frac{D + 2(N-1)R_C}{1-D} \right)
\]  

If set up internal resistance:

\[
r_o = \frac{N R_L}{(1-D)^2} + \frac{D + (N-1)(3-2D)R_S}{(1-D)^2} + \frac{N_{\text{max}} R_D}{1-D} + \frac{D + 2(N-1)R_C}{1-D}
\]  

Thus:

\[
\Delta P = I_0^2 r_o
\]  

Alternatively:

\[
\Delta P = I_0^2 r_o = \left( \frac{P_o}{V_o} \right)^2 r_o = \left( \frac{V_o}{R_{\text{Load}}} \right)^2 r_o
\]  

Therefore, with the required output power \( P_o \) and output voltage \( V_o \) (respectively \( I_o \) and \( R_{\text{Load}} \)), the choice of working levels \( N \) and duty cycle \( D \) to minimize power losses is, in fact, essentially minimum internal resistance \( r_o \). The efficiency of the circuit can be calculated according to equation (27). \( B^* \) is the ideal voltage boost ratio in (10), and the internal resistance \( r_o \) is zero. The efficiency can be calculated by

\[
\eta = \frac{P_o}{P_{in}} = \frac{V_o I_o}{V_{in} I_{in}} = \frac{V_o I_o}{V_{in} B^*} = \frac{V_o}{V_{in} B^*}
\]  

The real voltage boost \( B = \frac{V_o}{V_{in}} \) is set up, then

\[
B = \frac{V_o}{V_{in}} = \eta B^*
\]  

The input power \( P_{in} \) and output voltage \( V_o \) are also calculated as follows:

\[
P_{in} = P_0 + \Delta P
\]  

\[
V_o = V_{in} B^*(N, D) - I_o r_o
\]  

This paper proposes using a graph method to determine \( N \) and \( D \) for minimum \( \Delta P \) (or minimum internal resistance \( r_o \)). The value of \( r_o \) as calculated in formula (24) with the parameters \( R_s, R_L, R_C \) is given in Table 5. The values \( D \) and \( N \) satisfy the constraint (22). The real voltage boost \( B \) can be calculated by formula (28) for each value of \( N, D, \) and \( r_o \).

The load resistor \( R_{\text{Load}} \) can be calculated from the required output voltage and power of the DC-DC converter in equation (31). We select \( R_{\text{Load}} = 250 \) Ohm, which is suitable for \( V_o \) from 400 V to 600 V and \( P_o \) from 250 W to 1000 W.

\[
R_{\text{Load}} = \frac{V_o^2}{P_o}
\]  

The efficiency and boost ratio graphs according to the activity levels \( N \) and duty cycle \( D \) are indicated by the flowchart in Figure 5, and Figure 6 shows the results of this.
Thus, using the figures in Table 4, it is possible to quickly determine the number of working levels of $N$ and the appropriate range of $D$ so that the conversion efficiency is the highest.
Table 4. The appropriate selection of D and N (RLoad = 250 Ohm).

| B   | 1.1 ≤ B ≤ 4.0 | 4.0 < B ≤ 6.0 | 6.0 < B ≤ 7.9 | 7.9 < B ≤ 20 |
|-----|---------------|---------------|---------------|--------------|
| Nset| 1             | 2             | 3             | 4            |
| D(N)| 0.1 ≤ D(1)< 0.75 | 0.5≤ D(2) < 0.67 | 0.5≤ D(3) < 0.62 | 0.5 ≤ D(4) ≤ 0.8 |
| Dset| 0.55          | 0.55          | 0.55          | 0.55         |
| Dmax| 0.75          | 0.67          | 0.62          | 0.8          |

3. Simulation and Experimental Results

3.1. Experimental Model and Results

The experimental model in Figure 7a has a design capacity of 1000 W and a maximum input voltage of 70 V at four levels. Table 5 shows the circuit parameters. Practical experiments were conducted with various different loads. Figure 7b shows the current and voltage values measured by the oscilloscope in the boost ratio $B = 9$ and the load changes from 600 W to 900 W. In Figure 7b, the orange and blue lines are the input voltage and current while the green and violet lines are the output current and voltage sequence. The measurement results are shown in Table 6. The efficiencies calculated from the measurement data are 95.5% and 94.4% at the 600 W and 900 W sequences.

Table 5. The parameters of the circuit.

| Elements   | Type and parameter                                   |
|------------|------------------------------------------------------|
| FET        | FQP38N30 (300 V, 38 A, $R_S = 0.07$)                 |
| Diode      | MUR1640CT, (400 V, 16 A, $V_F = 0.6$ V, $R_D = 0.08 \Omega$) |
| Capacitor  | $2 \times 22 \mu F$, $R_C = 0.2 \Omega$             |
| Inductor   | $L = 180 \mu H$, $R_L = 0.15 \Omega$                |

Figure 7. Experimental model (a), the input/output voltage and current in the experiment, (b) input voltage: orange, output voltage: violet, input current: cyan and output current: green.
Table 6. Measurement results and the effectiveness of the experiment shown in Figure 7b.

| $P_o$ (W) | Parameters | Value | Unit | Efficiency |
|-----------|------------|-------|------|------------|
| 600       | $V_{in}$   | 49.5  | V    |            |
|           | $I_{in}$   | 13.3  | A    |            |
|           | $P_{in}$   | 658.35| W    | 95.5%      |
|           | $V_o$      | 449.0 | V    |            |
|           | $I_o$      | 1.4   | A    |            |
|           | $P_o$      | 628.6 | W    |            |
| 900       | $V_{in}$   | 48.8  | V    |            |
|           | $I_{in}$   | 19.4  | A    |            |
|           | $P_{in}$   | 946.72| W    | 94.4%      |
|           | $V_o$      | 447   | V    |            |
|           | $I_o$      | 2.0   | A    |            |
|           | $P_o$      | 894   | W    |            |

The three loads that were measured in the simulation and experiment were 1000 W, 500 W and 250 W. We performed some experimental and simulated tests to verify the findings, including the following:

Test 1: Determine the duty cycle ($D$) and the number of activity levels ($N$) while changing the boost ratio $B$. This test shows the benefits of flexibility when combining the duty cycle and the number of activity levels. The duty cycle is always in the controllable area (in Table 5) by increasing or decreasing working levels. Then, it is easy to control the stable output voltage under the changing of the load or the input voltage.

Test 2: Determine the conversion efficiency $\eta$ according to the voltage boost ratio $B$. This test shows that an advantage of the proposed technique is its ability to possibly increase the conversion efficiency if the duty cycle and the number of activity levels are determined appropriately. The selection of the largest number of activity levels, if possible, will reduce the current through the components, thus helping to increase the conversion efficiency.

3.2. Analysis of the Results of Tests 1 and 2 with the Load of 500 W

Figure 8a shows four characteristics of the boost ratio $B$ with four values of $N$ ($N = 1 \ldots 4$) and the duty cycle $D$ with a 500 W load. Figure 8b shows the efficiency curves that were calculated based on the flowchart in Figure 5 and simulated using the PSIM software. Figure 8c shows the experiment’s performance results using the model. The test results show that there were no significant differences between the theoretical calculations and the simulated and experimental results.
Figure 8. Boost ratio $B$ (a), Efficiency $\eta$ in calculated - simulation (b), and experiment (c) at $P_o = 500$ W.
The results in Figure 8 indicate that the boost ratio $B$ can be continuously controlled, ranging from 1 to 18 with an efficiency range of 93% to 99% in theory. Experimentally, the values were $B$ from 2 to 13, with an efficiency range of 91% to 96.6%. Generally, these results indicate that the quality of the proposed converter is high compared to the circuits presented in [20,21] with the same power and boost ratio.

The observations in Figure 8a show that the duty cycle $D$ was allowed to operate from 0.1 to 0.8 with $N = 1$ and $D = (0.5$ to $0.8)$ with $N = 2$ to 4. With the specific boost ratio $B = 4$ to 5, there are two options: $N = 1$ and $N = 2$. If $N$ is 1, and $B$ equals 5, then $D$ is 0.8, so the output voltage is difficult to keep stable when the load changes suddenly. On the contrary, if $N = 2$ is selected, with $B = 5$, it is quite easy to keep the output stable due to the adjustment of $D$ within $0.5 \leq D \leq 0.8$ (specifically $D = 0.52$). The same is true for higher boost ratios. For example, if $6 \leq B \leq 8$, you can choose $N = 2$ or $N = 3$. If $N = 3$ and $0.5 \leq D \leq 0.65$, it will be easier to adjust the output voltage than with $N = 2$ and $0.65 \leq D \leq 0.78$. Alternatively, if $8 \leq B \leq 13$, with selective active levels $N = 4$ and a $D$ value in the range of 0.5 to 0.72, it will be easier to control than choosing $N = 3$ and $0.65 \leq D \leq 0.8$.

Figure 8b describes the relationship between the conversion efficiency and the boost ratio of the proposed converter. The boost ratio $B$ is the function of working levels $N$ and the duty cycle $D$. It can be easy to see with a $B$ range of 1 to 5 when $N$ is 1, the appropriate duty cycle $D$ is from 0.1 to 0.8 (at $D = 0.8$, as shown in formula (24), and the value of the boost ratio can still reach $B = 5$). However, when the boost ratio $B$ is 4 to 5, the conversion efficiency with only one activity level ($N = 1$) will be lower than that with two ($N = 2$). Specifically, when the boost ratio was $B = 4.5$, the efficiency improved from 98% ($N = 1$) to 98.3% ($N = 2$).

Similarly, when $B$ is a range of 4 to 7.9, the efficiency with three activity levels is higher than with two. Specifically, when the expected boost ratio $B$ is 7.5, the efficiency is improved from 97% to 97.5% when changing $N$ from 2 to 3. Moreover, when the boost ratio $B$ is larger than 7.9, for the operation in four activity levels ($N = 4$), the performance is significantly improved. With $B = 9$, the efficiency ($\eta$) increases from 96.2% ($N = 2$) up to 97.3% if changing the activity levels from $N = 2$ to $N = 4$.

For the experiments with 250 W and 1000 W loads, the boost ratio $B$ and the efficiency curves are shown in Figures 9 and 10. The analysis and evaluation of these characteristics yield similar results as in the 500W load. In the load of 1000W, it is only possible to conduct the experiment if the activity levels are more than two. With the number of level $N = 1$, the too-large input current can destroy the MOSFET switch (S1).
Figure 9. Boost ratio $B$ (a), Efficiency $\eta$ in calculated - simulation (b), and experiment (c) at $P_o = 250$ W.
Figure 10. Boost ratio $B$ (a), Efficiency $\eta$ in calculated - simulation (b) and experiment (c) at $P_o = 1000$ W.
Generally, the duty cycle $D$ and activity level $N$ determines the base of the flowchart in Figure 11, and these are the best ways to improve control and voltage stability. With the specific boost ratio, choosing the highest activity levels $N$ and the appropriate duty cycle $D$ will easily be able to stabilize the voltage under a fluctuating load. Due to the fact that the duty cycle $D$ always has the smallest value, increasing the number of active levels $N$ to the highest possible value and tracking the appropriate duty cycle $D$ will divide the input current through the $N$ switches, inductors and capacitors, which increases the efficiency of the circuit. The analysis, simulation and experiment conducted in this paper have proven this.

3.3. Control the Proposed Converter as in the Flowchart in Figure 11

The experiments based on the flowchart in Figure 11 track the activity levels $N$ and duty cycle $D$ when the boost ratio $B$ changes, with the goal of achieving the highest efficiency. Figure 12 shows the comparison of efficiencies (simulation) between the proposed converter and the others in Figure 2a,b with the parameters in Table 5 for power loads of 250 W, 500 W and 1000 W. When the power load or the boost factor $B$ increases, the efficiency of the proposed converter is better. Especially with a high boost ratio, the activity level is higher, so that dividing the input current between the switches results in a significant reduction in power loss in the switches.

![Flowchart](image-url)

**Figure 11.** Flowchart for determination of $N$ and $D$. 
Figure 12. The comparison of efficiency between the proposed converter and the others in Figure 2a,b with $P_o = 250$ W (a), 500 W (b), and 1000 W (c).

Similarly, Figure 13 shows a comparison of the results of the boost ratio $B$ (according to the duty cycle $D$) between the proposed converter and the others shown in Figure 2 for the different loads. At a low boost ratio ($B < 4$), the proposed configuration still operates normally with a duty cycle $D$ in the range of 0.1 to 0.75, but the others do not. With $B$ ranging from 4 to 8, the proposed converter works for values of 0.5 to 0.75 of $D$, but the converter [16] does not, and the converter in Figure 2b works when $D < 0.5$, so this is due to the high ripple of the input current [22].

Figure 13. The comparison of boost ratio $B$ with $P_o = 250$ W (a), 500 W (b), 1000 W (c).

Figure 14a,b represent a comparison of the voltage stress on the switches and diodes of the converters. The voltage stress in the proposed converter is lower than that of the VLC converter and the same goes for the interleaved converter.

Figure 14. The comparison of voltage stress on switches (a) and diodes (b).

Figure 15a,b depict the gate voltage, the voltage stress on the MOSFETs and the duty cycle $D$ in the boost ratio $B = 8$, when the number of working levels is $N = 3$ (Figure 15a) and $N = 4$. (Figure 15b). These results show that the efficiency increases from 93.8% ($N = 3$) to 95% ($N = 4$), and the voltage stress on the MOSFET switches decreases from 134 V down to 100 V.
4. Conclusions

This paper proposes the non-isolated DC-DC converter with the highest boost ratio and efficiency. The boost ratio can change due to the wide range of the changing activity levels. The change in the number of activity levels and the appropriate duty cycle can increase the efficiency and the stability of the output voltage when the load suddenly changes.

The experimental results show that the efficiency of the proposed converter was higher than 90%, and the maximum efficiency was 98.3% for loads ranging from 250 W to 1000 W. In addition, the boost ratio can be controlled for the range of 1.25 to 13 when $0.25 \leq D \leq 0.7$ and activity levels range from 1 to 4 ($N_{\text{max}}$).

The paper clearly explains the operation sequence of the proposed converter and the mathematical formulas for the power loss in the components.

With the physical descriptions, the mode of operations and the mathematical formulas, the boost ratio and the efficiency represent the functions of the activity levels and duty cycle. Therefore, this paper proposes an algorithm for tracking the activity levels and duty cycle in order to achieve the maximum efficiency. In addition, the simulations produced using the PSIM software and the experiments that were conducted verify the proposed advantages.

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