A wideband blocker-resilient direct delta sigma receiver with selective input-impedance matching

Faizan Ul Haq1 · Mikko Englund3 · Kim B. Östman4 · Kari Stadius2 · Marko Kosunen2 · Kimmo Koli3 · Jussi Rynänen2

Received: 8 April 2019 / Revised: 28 January 2020 / Accepted: 26 February 2020 / Published online: 17 March 2020
© The Author(s) 2020

Abstract
This paper presents a wideband blocker-tolerant direct ΔΣ receiver (DDSR). Blockers are attenuated through selective input impedance matching and reduced gain design. The selective input impedance profile provides a low impedance at blocker frequencies enabling blocker attenuation, while the in-band impedance is boosted to matched condition through an up-converted positive feedback from the DDSR output. In addition, with the help of reduced gain design, near band blocker gain is minimized, further improving the blocker resilience. The receiver is designed for configurable operation from 0.7–2.7 GHz and a baseband bandwidth of 10 MHz. Simulated in a 28 nm technology, the DDSR demonstrates a maximum noise figure of 6.2 dB, and achieves a peak SNDR of 53 dB with an out-of-band 1 dB input compression point of −11 dBm at a 100 MHz offset.

Keywords  Blocker tolerance · Selective impedance matching · Tunable bandpass filtering · Low noise amplifier · Direct delta sigma receiver

1 Introduction

Wireless receivers for emerging radio access standards such as 5G and LTE-A demand a reconfigurable operation on multiple frequency bands and across a wireless spectrum of several GHz. To meet this required reconfigurability, several digital intensive architectures have been envisioned [1–4]. Among these, one showing promising performance is the direct-ΔΣ-receiver (DDSR). The architecture was first presented in [5] and investigated further in [6–10].

The wideband DDSR architecture differs from conventional direct conversion receivers by embedding RF front-end units as part of a delta-sigma-modulator (DSM) loop-filter. As shown in Fig. 1, the DDSR brings the outermost loop of the feedback type ΔΣ modulator to the output of a low noise amplifier (LNA). In this way, signal discretization already begins at RF and the DSM loop filter performs the functions of both baseband filtering and quantization noise shaping.

Inherently, such wideband receivers are exposed to high power out-of-band (OB) blockers. If not attenuated, these blockers may completely saturate the receiver and make reception non-linear. Traditionally, OB blocker resilience has been achieved by utilizing external off-chip filtering. However, as external filters are generally non-tunable and bulky, multiple filters are required to cover wide range of receiver bands. Two widely used on-chip alternatives for improving blocker resilience in wideband receivers are: (1) applying N-path filtering at the LNA output and (2) low-noise transconductance amplifier/mixer first arrangements [2, 6, 9, 11–16]. However, as will be explained later, these techniques have certain blocker rejection limitations such as not addressing the OB linearity degradation due to receiver input transconductor swing range limitation.

In this paper we propose a blocker resilient DDSR which attenuates blockers at both the input and output...
nodes of LNA. The additional bandpass filtering at LNA input is achieved through design of a low-intrinsic input impedance LNA, which provides OB voltage attenuation when driven by source impedance higher than LNA input impedance. On the other hand, at the desired signal frequency, input impedance is boosted to matched condition by implementation of positive upconverted feedback from the DDSR output. Additionally, we follow an approach of reduced receiver gain design which results in an improved near-band compression point. Evaluated with detailed simulations in a 28 nm technology, the proposed selective input impedance matching and reduced gain design approach demonstrates state-of-the-art blocker tolerance, when compared with recently published DDSRs.

The paper is organized as follows. Section 2 describes the limitations of blocker rejection with basic N-path filtering and how rejection can be improved with our proposed solution of selective input impedance and reduced gain design. Section 3 details the design method for the proposed DDSR while Sect. 4 covers its transistor level implementation details. We finalize the discussion with performance evaluation results in Sect. 5 and conclusions in Sect. 6.

2 Blocker rejection for a DDSR

2.1 Blocker rejection at the DDSR input

In DDSRs blocker rejection is usually achieved by implementing N-path filtering technique at the LNA output [5, 6]. However, there are two limitations with this approach. First, the gain/loss of far-away blockers is limited by the N-path mixer switch resistance ($R_{SW}$) and the LNA transconductance ($g_{m,LNA}$) which should both be minimized. These parameters cannot be reduced indefinitely due to limitations on local oscillator (LO) drive power consumption and LNA noise contribution. Second, filtering is implemented only at LNA output, neglecting the filtering requirement at the input. Without input filtering and provided the low blocker gain at the LNA output due to filtering, the LNA transconductor input swing range limits can reach earlier than its output. Therefore, an optimum design should ideally filter the OB blockers already at the LNA input.

In order to provide on-chip bandpass filtering at the DDSR input, the input impedance ($R_{IN}$) needs to be frequency dependent and lower than source impedance ($R_S$). The relative blocker voltage attenuation is proportional to the ratio between $R_S$ and $R_{IN}$ at blocker frequencies. Such an input impedance profile has been demonstrated earlier in [17, 18] for LNA-first receivers and in [19] for mixer-first receivers. However, in both LNA-first and mixer-first designs, the selected input impedance profile was chosen to reduce the noise contribution of the front-end. The authors did not report the possibility of blocker attenuation through optimizing the input impedance profile. In this paper, we utilize this impedance profile to provide additional blocker voltage attenuation already at the DDSR input.

2.2 Blocker rejection through optimized gain design

In a typical down-conversion receiver, gain is needed for two reasons: First, it suppresses noise contributions from the later stages of the receiver. From this point of view, implementing gain more than the minimum required to suppress the noise contribution of later stages does not bring any benefit from noise perspective. Second, gain is needed so that the weakest input signal appearing at the analog-to-digital converter (ADC) input is sufficiently greater than the quantization noise of the ADC. For DDSRs, however, this ADC input range requirement is different and needs further explanation.

Figure 2 presents a comparison of the typical output spectrum for a Nyquist-rate ADC based receiver and that of a DDSR. Typically, a Nyquist-rate ADC for a receiver is designed to meet certain signal-to-noise and distortion ratio (SINR) requirement dictated by the communication standard. The maximum SINR achieved by the ADC is limited on upper side by full-scale linear voltage swing range ($V_{FS}$) and on the lower side by the noise floor. A typical ADC design process starts from $V_{FS}$ and the required SINR is achieved by pushing the ADC’s quantization noise floor down by increasing the ADC resolution. After defining this resolution, sufficient gain needs to be applied in the receiver chain so that the amplified receiver thermal noise level at the ADC input is higher than the quantization noise floor. This ensures that the quantization noise does not contribute significantly to the overall receiver noise. Analytically we can calculate the minimum gain (G) requirement for Nyquist-ADC based receivers as:

$$G = P_{FS} - SNR_{tar} - SNR_{min} + 174 - 10\log(f_{BW})$$

where $P_{FS}$ is the ADC full-scale power in dBm, $SNR_{tar}$ is the required SNR for a given specification, $SNR_{min}$ is the...
minimum acceptable SNR for an acceptable reception, and \( f_{BW} \) is the required channel bandwidth.

In contrast, the DDSR design begins from the in-band thermal noise floor level at the input of the receiver. The amount of gain that is applied in the DDSR is selected solely based on what is needed to ensure that the LNA is the most significant noise contributor. The resolution of the quantizer and the loop filter order are then designed so that the in-band quantization noise is sufficiently lower than the amplified thermal noise. This ensures that the minimum amount of gain is applied in the receiver.

Now let us consider how the lower gain helps to achieve optimized blocker rejection in DDSR design. High power blockers can make the receiver operation non-linear if they are strong enough to reach the swing range limitations of the designed RF and BB amplifiers. Any additional gain for blockers will result in amplifier swing range limitations being reached earlier. Therefore, whenever gain is applied in the receiver, it should be selective so that only desired signals are amplified and blockers are attenuated. Usually this is done in receivers through RF and/or BB filtering. However, filtering profiles for a single stage are generally limited to first-order roll-off after the cut-off frequency.

This means that any near-band blockers will not be suppressed adequately by a single filtering stage. A higher number of filtering stages with partitioned gain can be employed for reasonable suppression of near-band blocker signals. However, after a certain limit, increasing the number of stages becomes impractical due to increased power consumption. Another way to solve this problem is to implement higher-order filtering schemes such as in [15]. However, higher-order filtering still provides limited near-band blocker attenuation. Considering this limited roll-off of RF and BB filters, we propose to suppress the near-band blocker signals with minimum possible gain. This is easy to achieve in DDSRs, as the absolute power of DSM quantization noise is much lower than thermal noise floor due to the inherent noise shaping of DDSR.

Based on the aforementioned discussion, our proposed DDSR consists of optimized receiver gain design together with tunable bandpass filtering at the RF input. We now detail the design of proposed the DDSR.

### 3 DDSR design

Figure 3 shows the block diagram of the proposed DDSR. In comparison to the traditional DDSR architecture, the proposed architecture differs in the front-end design. We intentionally design the intrinsic input impedance \( R_{INT} \) of the front-end to be lower than the antenna source impedance \( R_S \) while at the desired frequency this \( R_{INT} \) is boosted to matched conditions by the application of up-converted positive feedback from the DDSR output (Fig. 5). As explained earlier, lower \( R_{IN} \) at blocker frequencies helps to reduce blocker voltage gain already at the DDSR input.

Apart from attenuating the blockers from selective impedance profile, the proposed DDSR is designed with only the minimum closed loop gain \( A_{CL} \) required to suppress the noise contribution of later stages. The \( A_{CL} \) gain is defined from the LNA input to DDSR output including the input impedance mismatch effects. As explained earlier, this reduced gain helps to achieve better near-band blocker rejection. An \( A_{CL} \) of 20 dB is selected in this case which will suppress the noise contribution from later stages to about 10 \( \times \). This means that later DDSR stages can be designed with much lower current. For such a case, combined noise factor \( F_{tot} \) of stages after the LNA can be derived as:

\[
F_{tot} = 1 + (F_{RX} - F_{LNA})A_{CL}
\]

Here \( A_{CL} \) should be put on linear scale, and \( F_{RX} \) is the target NF of receiver. To achieve such \( F_{tot} \), we can...
approximate the later stage minimum required transconductance as:

\[
g_m \approx \frac{\eta}{R_S(F_{\text{tot}} - 1)}
\]  

(3)

where \(\eta\) is process and channel-length dependent constant.

After the selection of \(A_{\text{CL}}\), and referring to Fig. 4 for parameter definitions, the DDSR design is split into four steps: (1) the value of the positive feedback factor \((\beta_{\text{req}})\) and the DDSR open loop gain without the positive feedback \((A_{\text{OL}})\) are solved which provide the desired impedance match and \(A_{\text{CL}}\). (2) The loop-filter is designed with the calculated \(A_{\text{OL}}\) specification. (3) We take into account the non-idealities of the N-path filter and demonstrate how the DSM coefficients are implemented in the circuit. Finally, in (4) positive feedback is implemented with a value of required feedback factor \((\beta_{\text{req}})\) from step one that matches \(R_{\text{IN}}\) to \(R_S\) and raises \(A_{\text{OL}}\) to \(A_{\text{CL}}\) (Fig. 5). In the

Fig. 3 (Top) Block level representation of the proposed receiver, and (bottom) implementation of the proposed wide-band DDSR architecture. Blockers are attenuated through low LNA input impedance

Fig. 4 Simplified small signal model of positive feedback loop excluding the mixer upconversion effects (top) voltage mode DAC implementation (bottom) Current steering DAC implementation
As explained, the positive feedback loop boosts $R_{IN}$ to matched conditions. However, the implementation of positive feedback also increases the gain of the DDSR and consequently reduces the bandwidth. Therefore, the initial open loop gain of DDSR without positive feedback ($A_{OL}$) should be designed to be lower than target $A_{CL} = 20 \text{ dB}$.

In order to find the starting $A_{OL}$ and the required value of positive feedback factor $\beta_{req}$ that gives the matched input impedance and $A_{CL} = 20 \text{ dB}$, the small-single model presented in Fig. 4 can be used. The presented model does not consider passive mixer upconversion losses, therefore, some deviation of analytical results from simulated response is expected. Nevertheless, for quadrature passive mixers with 25% duty-cycle, the difference is not large and results can be used with reasonable accuracy. For the presented model, a simple shunt-shunt positive feedback analysis with DAC gain ($G_{DAC}$) of unity provides [20]:

$$\beta_{req} \approx \frac{R_{IN}R_{S} - R_{S}(R_{S}|R_{DES}|) - (R_{S}|R_{DES}|)R_{IN}}{(R_{S}|R_{DES}|)R_{IN}R_{S} - A_{CL}R_{IN}R_{S}^2}, \quad (4)$$

where $R_{IN}$ is the intrinsic input impedance of the DDSR front-end and $R_{DES}$ is the desired $R_{IN}$ for a matched case. In addition, $A_{CL}$ should be put on linear scale in all derived equations of the presented model. Provided that the calculated $\beta_{req}$ is lower than the maximum theoretical $\beta_{req} < 1/A_{OL}$, a stable implementation of $\beta_{req}$ is possible. The positive feedback factor $\beta$ can be implemented by design as:

$$\beta \approx \frac{1}{R_{POS} + R_{SW} + r_o}, \quad (5)$$

where $R_{SW}$ is the passive mixer switch resistance and $r_o$ is the output impedance of DAC. This means that $\beta_{req}$ can be achieved by controlling the value of $R_{POS}$ in the positive feedback loop.

Based on $\beta_{req}$, we can calculate the starting open-loop gain $A_{OL}$ that will result in $A_{CL} = 20 \text{ dB}$ after the implementation of positive feedback.

$$A_{OL} \approx \frac{A_{CL}R_{S}}{(1 + A_{CL}R_{S}\beta_{req})(R_{S}|R_{DES}|)|1/\beta_{req}|}, \quad (6)$$

where the calculated $A_{OL}$ is in linear scale. As a design example we select $R_{IN} = 15 \Omega$, $R_{DES} = 50 \Omega$, $G_{ADC} = 1$ and $R_{S} = 50 \Omega$. These values are extracted from the implemented circuits in DDSR and represent what can be practically be achieved. For example, reducing $R_{IN}$ to be lower than 15 $\Omega$ will increase the power consumption of LNA substantially. Based on the chosen parameters, the required feedback factor from Eq. ?? is $\beta_{req} \approx 0.005$. In other words, $R_{POS} + R_{SW} + r_o$ of 200 $\Omega$ is required. Based on the calculated $\beta_{req}$, Eq. 4 suggests $A_{OL} = 13.3 \text{ dB}$.

### 3.1.2 Case-II, IDAC implementation

As presented in Fig. 4, the IDAC implementation in the positive feedback path can be modeled with a voltage controlled current source having a transconductance $g_{m,IDAC}$ and output resistance $r_o$. Following a simple shunt-shunt feedback analysis, we can solve the value of positive feedback factor $\beta$ that gives the required input impedance match and closed loop gain $A_{CL}$.

$$\beta_{req} \approx \frac{(R_{S}|R_{DES}|)(1/(r_o + R_{SW}) + 1/R_{INT} + 1/R_{S}) - 1}{A_{CL}R_{S}}, \quad (7)$$

Provided that $\beta_{req}$ is lower than the maximum theoretical $\beta_{req} < 1/A_{OL}$, a stable implementation of $\beta_{req}$ is possible.
The positive feedback factor $\beta$ can be implemented by design as:

$$\beta \approx \frac{r_o}{r_o + R_{POS} + R_{SW}} g_{m,IDAC},$$

(8)

This means that the required value of feedback factor can be achieved by controlling $g_{m,IDAC}$ and $R_{POS}$ (Fig. 4).

Based on $\beta_{req}$, we can calculate the starting open-loop gain $A_{OL}$ that will result in $A_{CL} = 20$ dB after the implementation of positive feedback as:

$$A_{OL} \approx \frac{A_{CL} R_S}{(1 + A_{CL} R_S \beta_{req}) (R_S||R_{INT}) (R_S + R_{POS} + r_o)}.$$  

(9)

where the calculated $A_{OL}$ is in linear scale. As a practical design example, we select, $R_{INT} = 15 \, \Omega$, $R_{DES} = 50 \, \Omega$, $R_s = 50 \, \Omega$, $R_{SW} = 32 \, \Omega$, $r_o = 2 \, k\Omega$ and $R_{POS} = 200 \, \Omega$. These values are extracted from the implemented circuits in proposed DDSR and represent what can be practically be achieved. In implementation section, we will elaborate more the reason to choose these parameters values. Based on the chosen parameters, the required feedback factor from Eq. 5 is $\beta_{req} \approx 0.005$. In other words, $g_{m,IDAC}$ of 5.5 mS is required. Based on calculated $\beta_{req}$ Eq. 7 suggests $A_{OL} = 13.3$ dB.

Both, DAC and IDAC feedback structures are valid choice for positive feedback implementation. However, in order to be consistent with other baseband IDAC based feedbacks in proposed DDSR, we choose an IDAC-based positive feedback implementation.

### 3.2 Loop-filter design

Based on the calculated value of $A_{OL}$, the next step is to design the DDSR loop-filter. As has been focus of the discussion, blockers are the main concern when designing a DDSR. Thus, it is also natural that we emphasize the signal transfer function (STF) in the loop-filter design. The cascade of integrators in feedback topology (CIFB) is well suited for a DDSR thanks to its well-defined and non-peaking STF. The poles of the low-pass STF and high-pass noise transfer function (NTF) are identical, meaning that we can choose to design either the STF or NTF, which then fixes the other. We choose to design the STF, while keeping in mind the requirements for quantization noise shaping. Gain needs to be applied in the first stage, so that the noise performance requirement of the later stages can be relaxed. Based on the previous section, we select $A_{OL} = 13.3$ dB gain in this case. For the out-of-band, we want to keep the applied gain to a minimum and therefore the first pole of the STF needs to be at channel bandwidth ($f_{BW}$).

Next, we need to calculate the number of additional noise shaping stages after the LNA required for fulfilling the quantization noise shaping requirement. The number of these stages can be calculated to be [6]:

$$n = \log_2 \left( \frac{\Delta^2}{f_{BW} \cdot A_{req}} \right)$$

(10)

where $\Delta$ is the quantizer step size, $f_s$ is the sampling frequency, $k$ is Boltzmann constant, $T$ is the temperature in Kelvins ($T = 300$ K is used), $A_{CL}$ is the required receiver power gain after the implementation of positive feedback, $F_{RX}$ is the noise factor of the receiver excluding quantization noise, $f_{BW}$ is BB bandwidth cutoff frequency, and $f_{NSP}$ is the combined noise shaping pole cutoff frequency. The closed loop gain of the receiver was targeted to be $A_{CL} = 20$ dB, while the parameters $\Delta$, $F_{RX}$, $f_s$ and $f_{NSP}$ still remain undefined.

In order to keep the focus of the paper on the positive feedback, we utilize an ideal 4-bit quantization and feedback with a clock delay added to emulate the required time for buffering and transistor switching. The differential input range for the quantizer is selected to be 600 mV, so that it is not the limiting factor for receiver linearity and thus we can calculate that $\Delta = 40$ mV. Noise factor $F_{RX}$ is set by the device noise of amplifiers and the mixers, dominated by the noise of the first amplifier in the chain. For calculating the number of noise shaping stages, we use $NF = 5$ dB i.e. $F_{RX} = 3.1623$, which is based on steady-state AC simulations when the discrete feedback is replaced by ideal continuous-time feedback.

The selection of the sampling frequency $f_s$ is critical in a DDSR. This is because the loop-filter contains mixers, that need to operate across the receiver frequency range. If no additional filtering is implemented for the feedback signal that is fed to the mixer nodes, LO frequencies that are not multiples of $f_s/2$ will cause the quantization noise to fold to the in-band and potentially desensitize the receiver [5]. The severity of this effect is dependent on the absolute level of the quantization noise at LO frequency and its harmonics. In order to avoid this issue, we have locked the $f_s$ to LO frequency ($f_{LO}$). The $f_s$ will thus vary between 0.7–2.7 GHz.

A parameter that still remains undefined is the combined noise shaping pole cutoff frequency $f_{NSP}$. In addition to being the key factor in determining the required number of stages, $f_{NSP}$ also affects the stability of the loop. The lower limit for $f_{NSP}$ is $f_{BW}$ as the number of stages increases to infinity. As a first order analysis, we can reason that the upper limit is $f_s/4$, as the quantization noise removed from below this frequency has to fit between $f_s/4$ and $f_s/2$, leading to the stability criteria of 3 dB out-of-band gain for...
the NTF. As we approach the upper limit, the high-frequency gain of the NTF increases [21]. A high NTF gain will decrease feedback loop resilience against non-idealities, such as the excess-loop delay or clock jitter [22]. To navigate this trade-off, we select f_{NSP} to be 10 times f_{BW}, or 100 MHz, which is 1/7–1/27 of the f_c.

Calculating the number of noise shaping stages from Eq. 10 with the chosen parameters gives n = 2.44–2.73 i.e. 3 stages. The resulting loop filter has a total of four stages where the first one provides gain and filtering and the following three ensure that the inband quantization noise is shaped below the thermal noise level. Next, the loop-filter coefficients need to be determined. Implementing an A_{OL} = 13.3 dB and the chosen bandwidth requires that when normalized to f_{BW}, a_1 = 9.25 and b_1 = 1. In order to avoid peaking, Butterworth coefficients are used in the noise shaping stages. The initial coefficients of the noise shaping stages are first normalized to f_{BW} and then scaled so that a_k = G_k b_k, where G_k is the gain of respective DSM filter stage. This results in dynamic range scaling, setting the dc gain of each noise shaping stage to unity. The initial and the scaled coefficients are listed in Table 1.

Based on above calculated coefficients, the STF of the proposed DDSR can be derived as:

\[
H_{\text{STF}} = \frac{a_3 a_4 h_{fb} H_{\text{I}}^2}{1/H_{\text{I}} + a_2 a_3 a_4 h_{fb} H_{\text{I}}^2 + a_3 a_4 b_2 H_{\text{I}}^2 + a_4 b_3 H_{\text{I}}^2 + b_4 H_{\text{I}}^2},
\]

where H_{\text{I}} is the integrator transfer function. For an ideal integrator it is 1/s.

### 3.3 Loop filter implementation

Figure 3 shows the block diagram of the proposed DDSR. The first integration stage consists of the LNA, down-converting passive mixers and integration capacitances at the baseband, which form an N-path filter. The second, third and fourth stage are implemented as g_mC integrators. The noise performance of each stage is dependent on their transconductance g_m, and thus the LNA and the g_m stages are designed first. The LNA performance sets the noise figure to be roughly 5 dB, while the later stages are designed so that their contribution is minimal. Based on the designed g_m of the stages, we can calculate the capacitances C_{1-4} of the DSM loop filter and the feedback transconductances g_{m, fb,1-4} as [10, 23]:

\[
C_1 = \frac{\sqrt{2} g_m \text{LNA}}{\pi g_m \text{LNA} H_{\text{I}} + R_{LNA} R_{SW}} \tag{12}
\]

\[
C_2-4 = \frac{g_m 2^{-4}}{2 \pi a_2 a_4 f_{BW}} \tag{13}
\]

\[
g_{m, fb,2-4} = \frac{g_m 2^{-4}}{G_{2-4}} \tag{14}
\]

\[
g_{m, fb,1} = \frac{h_{RF} / (2A_{OL} - 1)}{h_{fb}} \tag{15}
\]

\[
h_{RF} = \frac{\sqrt{2} g_m \text{LNA} R_{LNA} R_{BB} R_{SH}}{4 R_{BB} (R_{LNA} + R_{SH} + R_{SW}) + \pi^2 R_{SH} (R_{LNA} + R_{SW})} \tag{16}
\]

\[
h_{fb} = \frac{4 R_{BB} (R_{LNA} + R_{SW})}{2 R_{LNA} + 2 R_{SW} + R_{BB}} \tag{17}
\]

\[
R_{SH} = \left( \sum_{n=3,7,11}^{\infty} \frac{1}{n^2 R_3^2 (n f_{LO})} + \sum_{n=5,9,13}^{\infty} \frac{1}{n^2 R_5^2 (n f_{LO})} \right)^{-1} \tag{18}
\]

where R_{LNA} is the output impedance of LNA, R_{BB} is the parallel combination of C_1 impedance and input impedance of first BB amplifier, G_{2-4} is the gain of respective DSM stages, h_{RF} is the transfer function from the LNA input to the first BB output, h_{fb} is the transfer function for the negative DSM feedback from DDSR output to first BB input and R_{SH} represents the virtual shunt impedance representing the power dissipation due to baseband signal upconversion.

The final values of the circuit parameters are provided in Table 2.

| Table 1 Loop-filter coefficients |
|---------------------------------|
| Coefficient | a_1 | a_2 | a_3 | a_4 | b_1 | b_2 | b_3 | b_4 |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Initial      | 9.25| 1   | 1   | 1   | 1   | 2   | 2   |     |
| Scaled       | 9.25| 5   | 10  | 20  | 1   | 5   | 10  | 20  |

| Table 2 Circuit parameters |
|-----------------------------|
| Parameter | Value |
|------------|-------|
| g_mLNA [mS] | 80 |
| g_m2 [mS] | 23 |
| g_m3 [mS] | 2.6 |
| g_m4 [mS] | 2.6 |
| C_1 [pF] | 28 |
| C_2 [pF] | 73.2 |
| C_3 [pF] | 4.14 |
| C_4 [pF] | 2.07 |
| g_mfb,1 [mS] | 2.6 |
| g_mfb,2 [mS] | 23 |
| g_mfb,3 [mS] | 2.6 |
| g_mfb,4 [mS] | 2.6 |
3.4 Positive feedback implementation

Finally, positive feedback is implemented across the designed DDSR loop-filter. The required feedback factor $\beta_{\text{req}}$ is implemented by selecting a proper value for $g_{\text{m,IDAC}}$ and $R_{\text{POS}}$. The resulting closed loop gain is equal to the required $A_{\text{CL}} = 20$ dB and the input matched. However, the implementation of positive feedback reduces the bandwidth of the proposed DDSR. In order to circumvent the problem, the N-path capacitance $C_1$ needs to be scaled with a scaling factor of $A_{\text{OL}}/A_{\text{CL}}$ to match the desired bandwidth. The final value of $C_1$ can be found as:

$$C_{1,\text{scaled}} \approx C_1 \frac{A_{\text{OL}}}{A_{\text{CL}}}$$  \hspace{1cm} (19)

where $A_{\text{OL}}$ and $A_{\text{CL}}$ are open and closed-loop gains on linear scale.

Based on the system model and design equations presented earlier, Fig. 6 plots the required analytical transfer function for the proposed receiver.

4 System implementation

The DDSR is designed for an receiver gain of 20 dB. The RF front-end consists of a transconductor implementation with a parallel combination of common-gate CG and push-pull common-source CS amplifiers [16]. A common-gate amplifier is a valid choice as the input impedance can be easily controlled through common-gate transconductance. Figure 7(a) shows the circuit diagram of the designed transconductor. The parallel CG and CS combination increases the transconductor gain, and the push-pull configuration helps to achieve better large signal linearity. To maximize output voltage swing range of the transconductor, the output common-mode voltage is set to half of the supply voltage by implementing a common-mode feedback loop. Blocker filtering at the transconductor input is achieved by designing a low intrinsic input impedance.

Ideally, the intrinsic input impedance of the LNA should be 0 $\Omega$. However, due to practical limitations of LNA transistor power consumption, differential intrinsic input impedance is designed to be 30 $\Omega$. This intrinsic impedance is then boosted to matched condition by the positive feedback from the DDSR output to RF nodes through passive quadrature mixers. The amount of positive feedback can be controlled through positive feedback IDAC’s transconductance $g_{\text{m,IDAC}}$ and series resistance $R_{\text{POS}}$. Based on the analytical derivations from previous sections, we choose a $g_{\text{m,IDAC}} = 5.3$ mS. As implementation of positive feedback is prone to instability, process corner simulations were carried out, for the chosen $g_{\text{m,IDAC}}$, to ensure the stability of the system in all process corners.

Downconversion mixers in the main signal path were implemented as quadrature passive mixers driven with 25% duty cycle LO waveforms. Transistors with a large aspect-ratio of 48/0.03 $\mu$m are implemented in the main path downconversion mixers. This ensured a small switch resistance of 8 $\Omega$ for better attenuation at far away offsets from $f_{\text{LO}}$. As there was no such requirement of smaller $R_{\text{SW}}$ for the positive feedback mixers, their aspect ratio was
The later integrators were implemented with consecutively higher noise contribution. This is because once the gain is implemented in the system, later stages noise contribution is reduced by the amount of added gain. Therefore, there is no need for the later stage noise contribution to be low. Figure 7(b) shows the implemented dynamically-biased BB transconductors. All baseband amplifiers are designed with the same configuration as shown in Fig. 7(b) with the small exception of designing the first baseband transconductor with a transconductance of 23 mS and bias current of 3.8 mA. This is about 10 × higher than the bias currents of later baseband stages to ensure reduced noise contribution from the first baseband amplifier. Capacitors C1–C4 implement the required BB bandwidth cutoff frequency (fBW) and noise shaping pole cutoff frequency (fNSP) in the DSM loop filter. Their values were selected based on the calculations from the previous section and are provided in Table 2.

The quantizer and feedback DACs were implemented as behavioral models. Nevertheless, the most important non-idealities of quantizer and feedback DAC such as clock delay between DAC and quantizer and noise of DAC transistors were added to closely match the simulated behavior with real circuits.

5 Performance evaluation

The proposed DDSR was evaluated in a 28 nm fully-depleted silicon-on-insulator (FD-SOI) process through transient and steady-state AC simulations. The DDSR is reconfigurable from 0.7–2.7 GHz with a fBW of 10 MHz. Further, based on our previous implementation [6], we added estimated values I/O pad capacitances, bondwire inductances, s-parameter models of 20 nH off-chip RF-choke, and clock delay between the quantizer and IDACs in order to match the simulated results more closely to the real scenario.

The spectrum of the DDSR output bit stream for an input signal and blocker power of −43 dBm is shown in Fig. 8. A few key points can be observed. First, the desired in-band signal is amplified with about ACL = 20 dB of receiver gain. Second, the blocker at 73 MHz offset from fLO is filtered by the baseband filtering response, and third, the quantization noise is shaped by the DDSR feedback loop such that the in-band quantization noise is lower than thermal noise floor.

Figure 9 shows the simulated steady-state AC analysis results of DDSR gain and S11. As desired, ACL = 20 dB is observed within the 20 MHz RF bandwidth. Further, a differential out-of-band input impedance of 30 Ω can be seen needed for blocker attenuation at LNA input.

Figures 10 show the receiver SNDR versus input signal and blocker powers. The receiver achieves a maximum SNDR of 53 dB at PIN of −43 dBm. Further, we observe a decrease in SNDR from at blocker input powers greater than −35 dBm for an input signal power of −80 dBm. At low signal powers, the difference between ideal and simulated SNDRs is approximately equal to receiver NF.
Figure 11 presents a comparison of the simulated SNDR for cases when \( f_S = 1.5 \) GHz and \( f_S = f_{LO} \). It can be seen that for a constant \( f_S = 1.5 \) GHz, SNDR degrades from its maximum value for \( f_{LO} \neq nf_S/2 \), where \( n \) is an integer number. This degradation occurs due to the quantization noise upconversion effect inherent in DDSR architectures [5]. However, in the proposed structure, the degradation of SNDR due to quantization noise upconversion is much more severe than in a traditional DDSR. This is due to bringing the DDSR feedback to the input of receiver rather than to the LNA output. As there is no preceding gain stage before this input, the upconverted quantization noise effect is more severe on achieved SNDR. The problem was solved in the final design by choosing \( f_{LO} = f_S \) for the entire band of operation. As can be seen in Fig. 11, this ensures that the degradation of SNDR due to quantization noise upconversion effects is minimal.

Figure 12 presents the SNDR versus clock delay for two different sampling frequencies of \( f_S = 0.7 \) GHz and \( 1.5 \) GHz. The clock delay is defined from the rising edge \( f_S \) to the instant when output of IDAC begins to change. It can be seen that the DDSR loop is able to handle about 70 ps of delay, in the worst case \( f_S = 0.7 \) GHz, before the SNDR begins to degrade rapidly. At higher sampling frequencies, DSM loop is able to handle much longer delays than 70 ps. This is because a higher sampling frequency brings the response more close to a continuous time filter with more resilience towards clock delay. While the delay of 70 ps is still implementable in the given process, the process variations can increase the delay to be higher than 70 ps. Therefore, a better solution for worst case scenario of \( f_S = 0.7 \) GHz will be to lock \( f_S = 2f_{LO} \). Locking \( f_S = 2f_{LO} \) for the worst case scenario minimizes SNDR degradation due to quantization noise upconversion.

In addition to clock delay, the supply noise can also affect the maximum SNDR of the receiver. Figure 13
shows the performance of receiver SNDR under the presence of supply noise.

Figures 14 and 15 show the simulated NF, receiver gain and blocker input compression point (BCP). The receiver achieves a BCP of $-11.5 \text{ dBm}$ at 100 MHz offset from $f_{\text{LO}}$ with a maximum integrated receiver NF of 6.2 dB. When compared with BCP results collected into Table 3, the proposed approach is able to promising blocker tolerance even with its lower supply voltage.

### 6 Conclusion

We have proposed a blocker resilient DDSR with a low intrinsic input impedance front-end. It reduces blocker gain already at the LNA input by creating an on-chip tunable bandpass response. Furthermore, we proposed a reduced receiver gain design that helps to minimize near-band blocker gain. This ensures that the voltage swing limits are pushed towards much stronger blockers. The simulated results demonstrate an OB blocker compression point of $-11.5 \text{ dBm}$ and OB-IIP3 of 0 dBm at 100 MHz offset from the desired received frequency, with a maximum SNDR of 53 dB and a maximum NF of 6.2 dB. The results collected into Table 3 indicate that the proposed approach is able to achieve state-of-the art blocker tolerance even with its lower supply voltage.

**Acknowledgements** Open access funding provided by Aalto University. This research was supported by the Academy of Finland.

**Open Access** This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article’s Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article’s Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit http://creativecommons.org/licenses/by/4.0/.

### References

1. Martens, E., Bourdoux, A., Couvreur, A., Fasthuber, R., Wesmeael, P. V., der Plas, G. V., et al. (2012). RF-to-baseband digitization in 40 nm CMOS with RF bandpass $\Delta E$ modulator and polyphase decimation filter. *IEEE Journal of Solid-State Circuits, 47*(4), 990–1002.
2. Wu, C., Alon, E., & Nikolic, B. (2014). A wideband 400 MHz-to-4 GHz direct RF-to-digital multimode delta sigma receiver. *IEEE Journal of Solid-State Circuits, 49*(7), 1639–1652.
3. Shibata, H., Schreier, R., Yang, W., Shaikh, A., Paterson, D., Caldwell, T. C., et al. (2012). A DC-to-1 GHz tunable RF delta sigma ADC achieving $DR = 74$ dB and $BW = 150$ MHz at $fo = 450$ MHz using 550 mW. *IEEE Journal of Solid-State Circuits, 47*(12), 2888–2897.
4. Andersson, M., Anderson, M., Sundström, L., Mattisson, S., & Andreani, P. (2014). A filtering delta sigma ADC for LTE and beyond. *IEEE Journal of Solid-State Circuits, 49*(7), 1535–1547.
5. Koli, K., Jussila, J., Sivonen, P., Kallioinen, S., & Pärssinen, A. (2010). A 900MHz direct delta-sigma receiver in 65nm CMOS. In: 2010 IEEE international solid-state circuits conference—(ISSCC), Feb (pp. 64–65).
6. Englund, M., Östman, K., Viitala, O., Kaltiokallio, M., Stadius, K., Koli, K., et al. (2015). A programmable 0.7–2.7 GHz direct ΔΣ receiver in 40 nm CMOS. *IEEE Journal of Solid-State Circuits*, 50(3), 644–655.

7. Nguyen, M. T., Jabbour, C., Homayouni, S. M., Duperray, D., Triaire, P., & Nguyen, V. T. (2016). System design for direct RF-to-digital ΔΣ receiver. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 63(10), 1758–1770.

8. Englund, M., Östman, K., Viitala, O., Kaltiokallio, M., Stadius, K., Ryyränen, J., & Koli, K. (2014). A 2.5-GHz 4.2-dB NF direct delta sigma receiver with a frequency-translation integrator. In *European Solid State Circuits Conference*, Sept (pp. 371–374).

9. Nejdel, A., Liu, X., Palm, M., Sundström, L., Törnänen, M., Sjöland, H., & Andreani, P. (2015). A 0.6–3.0GHz 65 nm CMOS radio receiver with ΔΣ based A/D-converting channel-select filters. In *41st European Solid-State Circuits Conference (ESSCIR)* (ESSCIRC 2015), Sept (pp. 299–302).

10. Östman, K. B., Englund, M., Viitala, O., Stadius, K., Koli, K., & Ryyränen, J. (2015). Next-generation RF front-end design methods for direct delta sigm receivers. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 5(4), 514–524.

11. Lin, Z., Mak, P. I., & Martins, R. P. (2015). A 0.028mm2 11mW single-mixing blocker-tolerant receiver with double-RF N-path filtering, S11 centering, +13 dBm OB-IIP3 and 1.5-to-2.9 dB NF. In 2015 IEEE international solid-state circuits conference (ISSCC) digest of technical papers, Feb 2015 (pp. 1–3).

12. Ghaffari, A., Klumperink, E. A. M., & Nauta, B. (2010). A differential 4-path highly linear widely tunable on-chip band-pass filter. In *2010 IEEE radio frequency integrated circuits symposium*, May (pp. 299–302).

13. Mirzaei, A., Darabi, H., Yazdi, A., Zhou, Z., Chang, E., & Suri, P. (2011). A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE. *IEEE Journal of Solid-State Circuits*, 46(4), 950–964.

14. Borremans, J., Mandal, G., Giannini, V., Debaillie, B., Ingels, M., Sano, T., et al. (2011). A 40 nm CMOS 0.4-6 GHz receiver resilient to out-of-band blockers. *IEEE Journal of Solid-State Circuits*, 46(7), 1659–1671.

15. Chen, R., & Hashemi, H. (2015). Reconfigurable SDR receiver with enhanced front-end frequency selectivity suitable for intra-band and inter-band carrier aggregation. In *2015 IEEE international solid-state circuits conference (ISSCC) digest of technical papers*, Feb (pp. 1–3).

16. Ru, Z., Moseley, N. A., Klumperink, E. A. M., & Nauta, B. (2009). Digitally enhanced software-defined radio receiver robust to out-of-band interference. *IEEE Journal of Solid-State Circuits*, 44(12), 3359–3375.

17. Park, J., Kim, S. N., Roh, Y. S., & Yoo, C. (2010). A direct-conversion CMOS RF receiver reconfigurable from 2 to 6 GHz. *IEEE Transactions on Microwave Theory and Techniques*, 58(9), 2326–2333.

18. Rossi, P., Liscidini, A., Brandolini, M., & Svelto, F. (2005). A variable gain RF front-end, based on a voltage-voltage feedback LNA, for multistandard applications. *IEEE Journal of Solid-State Circuits*, 40(3), 690–697.

19. Nejdel, A., Abdulaziz, M., Törnänen, M., & Sjöland, H. (2015). A positive feedback passive mixer-first receiver front-end. In *Radio frequency integrated circuits symposium (RFIC)*, May 2015 (pp. 79–82). IEEE.

20. Sedra, A. S., & Smith, K. C. (2010). *Microelectronics circuits* (6th ed.). Oxford: Oxford University Press.

21. Norsworthy, S. R., Schreier, R., & Temes, G. C. (1996). *Delta-Sigma data converters*. Piscataway: IEEE Press.

22. Cherry, J. A., & Snelgrove, W. M. (1999). Excess loop delay in continuous-time delta-sigma modulators. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 46(4), 376–389.

23. Andrews, C., & Molnar, A. C. (2010). Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(12), 3092–3103.

**Publisher’s Note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Faizan Ul Haq received his M.Sc. and Ph.D. degrees in electrical engineering from Tampere university Finland and Aalto University Finland in 2012 and 2019. From 2012–2014 he was working as a research intern in Nokia research center, Finland. He is currently working as a senior design engineer at CoreHW Finland. His research interests include RF/analog communication circuits and power management circuits such as dc–dc converters.

Mikko Englund was born in Espoo, Finland, in 1985. He received the M.Sc. and Ph.D. degrees in electrical engineering from Aalto University School of Electrical Engineering, Espoo, Finland in 2013 and 2018. He is currently working as a senior RFIC design engineer at Huawei technologies Finland. His research interests include filters and high-speed analog-to-digital converters in digital-intensive receivers.

Kim B Östman received the M.Sc. (with distinction) and Lic. Tech. degrees from Tampere University of Technology, Tampere, Finland, in 2005 and 2012, respectively, and the D.Sc. (with honors) degree from Aalto University, Espoo, Finland, in 2014. He also holds the Ph.D. degree in the humanities from Åbo Akademi University, Turku, Finland. He was with the Department of Communications Engineering at Tampere University of Technology from 2002 to 2010, and with the Department of Micro- and Nanosciences at Aalto University School of Electrical Engineering from 2011 to 2014. From 2014 to 2015, he was with Nokia Technologies, and is now with Nordic Semiconductor as a Senior R & D Engineer. His research interests include highly linear wireless CMOS receivers, with a
Analog Integrated Circuits and Signal Processing (2020) 103:195–207

particular emphasis on digital-intensive solutions, along with frequency synthesizers and fully integrated DC–DC conversion.

Kari Stadius received the M.Sc., Lic. Tech., and Doctor of Science degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1994, 1997, and 2010, respectively. He is currently working as a staff scientist at the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering. His research interests include the design and analysis of RF transceiver blocks with special emphasis on frequency synthesis, and for analog and mixed-mode circuit design and new emerging RF technologies such as graphene. He has authored or coauthored over 70 refereed journal and conference papers in the areas of analog and RF circuit design.

Marko Kosunen received his M.Sc, L.Sc. and D.Sc. (with honors) degrees from Helsinki University of Technology, Espoo, Finland, in 1998, 2001 and 2006, respectively. He is currently a Senior Researcher at Aalto University, Department of Electronics and Nanoengineering. His research interests include the design and analysis of RF transceiver blocks with special emphasis on frequency synthesis, and for analog and mixed-mode circuit design and new emerging RF technologies such as graphene. He has authored and co-authored more than 80 journal and conference papers and holds several patents. His current research interests include programmatic circuit design methodologies, digital intensive and time-based transceiver circuits, and medical sensor electronics.

Kimmo Koli was born in Karuna, Finland, in 1964. He received the M.Sc., Lic. Tech., and D.Sc. degrees in electrical engineering from the Helsinki University of Technology, Helsinki, Finland, in 1991, 1995, and 2000, respectively. From 1989 to 2000, he was a Research Engineer in Electronic Circuit Design Laboratory at the Helsinki University of Technology. From 2000 to 2014, he joined STMicroelectronics (later ST-NXP Wireless, ST-Ericsson, and Ericsson) and is currently with HiSilicon at Huawei Technologies Oy (Finland) Co. Ltd., Helsinki, Finland, focusing on RF design blocks for wireless applications. He has authored or coauthored over 40 journal articles and conference papers and holds over 10 patents. Dr. Koli served as a member of the technical program committee of IEEE International Solid-State Circuits Conference from 2011 to 2014 and IEEE European Solid-State Circuits Conference since 2011.

Jussi Rynänen was born in Ilmajoki, Finland, in 1973. He received his Master of Science, Licentiate of Science, and Doctor of Science degrees in electrical engineering from Helsinki University of Technology (HUT), Helsinki, Finland, in 1998, 2001, and 2004, respectively. He is currently working as an associate professor at the Department of Electronics and Nanoengineering, Aalto University School of Electrical Engineering. His main research interests are integrated transceiver circuits for wireless applications. He has authored or coauthored over 100 refereed journal and conference papers in the areas of analog and RF circuit design. He holds six patents on RF circuits.