Comments on the parallelization efficiency of the Sunway TaihuLight supercomputer

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Abstract

In the world of supercomputers, the large number of processors requires to minimize the inefficiencies of parallelization, which appear as a sequential part of the program from the point of view of Amdahl’s law. The recently suggested new figure of merit is applied to the recently presented supercomputer, and the timeline of ”Top 500” supercomputers is scrutinized using the metric. It is demonstrated, that in addition to the computing performance and power consumption, the new supercomputer is also excellent in the efficiency of parallelization. Based on the suggested merit, a ”Moore-law” like observation is derived for the timeline of parallelization efficacy of supercomputers.

Keywords: supercomputer, parallelization, performance, scaling, figure of merit

1. Introduction

Supercomputers are ranked (TOP500.org (2016)) according to their parameter ”Rmax (TFlop/s)”, which parameter depends of two factors: how many processors are comprised and how effectively they are put together. Increasing the number of processors only is useless, as pointed out early by Amdahl: [Amdahl, G. M. (1967)] the effort expended on achieving high parallel processing rates is wasted unless it is accompanied by achievements in sequential processing rates of very nearly the same magnitude”.

Most of the users of supercomputers are not using all available processors, they are rather interested in the efficiency of parallelization of their program.
To find a proper merit was always subject of serious debates (see Sun and Gustafson (1991)). It looks like the recently introduced figure of merit (see Végh et al. (2016)), the effective parallelization, is a good merit not only to characterize the effectivity of parallelizing software execution, but also to characterize the engineering ingenuity of parallelizing the hardware operation, and so allows to characterize the timeline of supercomputer development itself.

2. THE MERIT $\alpha_{EFF}$

According to Amdahl (Amdahl, G. M. (1967)), the speedup can be expressed as

$$S^{-1} = (1 - \alpha) + \alpha/k$$  \hspace{1cm} (1)

where $k$ is the number of parallelized processors, $\alpha$ is the ratio of the parallelizable part to the total sequential part, $S$ is the measurable speedup. The same relation can be expressed (see Végh et al. (2016)) also in the form

$$\alpha_{eff} = \frac{k}{k-1} \frac{S - 1}{S}$$  \hspace{1cm} (2)

The first form is an architectural view, the second one is empirical: no matter, what causes the (apparently) sequential part, $(1 - \alpha)$ part decreases the parallelism, and so can be used to quantitize the goodness of the implementation of parallelisation.

In general, the efficiency (in the case of supercomputers: $\frac{R_{\text{max}}}{R_{\text{peak}}}$) is used, which cannot be used as a single parameter to describe the efficacy of the implementation. When using several processors, one of them makes the sequential calculation, the others are waiting (use the same amount of time). So, when calculating the speedup, one calculates

$$S = \frac{(1 - \alpha) + \alpha}{(1 - \alpha) + \alpha/k} = \frac{k}{k(1 - \alpha) + \alpha}$$  \hspace{1cm} (3)

hence the efficiency

$$R = \frac{S}{k} = \frac{1}{k(1 - \alpha) + \alpha}$$  \hspace{1cm} (4)

This explains the behavior of diagram $\frac{S}{k}$ in function of $k$: the more processors, the lower efficiency, and the larger $(1 - \alpha)$, the lower is the reachable speedup.
At this point one can notice that $\frac{1}{R}$ is a linear function of the number of the processors, and its slope equals to $(1 - \alpha)$, i.e. from the speedup data one can estimate value of $\alpha$ even for the individual regions, i.e. without knowing the execution time on 1 processor (from technical reasons, it is the usual case in the case of supercomputers).

Notice also that through using Equ. (4), $\frac{S}{k}$ can be equally good for describing the efficiency of parallelization efficiency of a setup, if the number of processors is also known. From Equ. (4)

$$\alpha_R = \frac{Rk - 1}{R(k - 1)}$$

Figure 1: Comparing efficiency, efficiency slope and $\alpha_{eff}$ for different communication strategies when running two minimization task on SoC by de Macedo Mourelle et al. (2016)
Figure 2: \((1 - \alpha_{\text{eff}})\) values for running benchmark Linpack on Sunway TaihuLight supercomputer and supercomputers 25 years ago, with different number of parallel processors. Karp and Flatt (1990)

This quantity of course assumes that \(\alpha\) is independent from the number of the processors. Its numerical value equals to the value calculated using differences over the full range of processors, and so is not displayed in Fig. 1. The supercomputer technology, according to the need mentioned above, is focusing on decreasing the (apparently) sequential part \((1 - \alpha)\), so this quantity is shown on the diagrams rather than \(\alpha\) itself.

3. Characterizing effect of communication method in SOC

As mentioned, in the Amdahl’s model there are only two categories: everything which does not make useful computational work, but needs time, contributes to the sequential part. Such contribution is the internal communication between cores inside a chip. In their work de Macedo Mourelle et al. (2016) compare the effect of using different internal communication methods. From their speedup results, the diagrams shown in Fig. 1 were derived. The diagrams show \((1 - \alpha)\), and for comparison, the slope of \(\frac{1}{\alpha}\) is also displayed. It looks like within the limits of the experimental precision, both methods provide the same numerical value. Also displayed for comparison the diagram \((1 - \frac{S}{N})\), which is traditionally used to describe the performance of multi-processor systems. As shown, for very low number of processors,
Figure 3: Supercomputer parallelization efficiency, in function of time and ranking

The diagram practically provides the same numerical value, so it is as good for describing multiprocessor efficiency, as \((1 - \alpha)\). However, \((1 - \frac{S}{k})\) steadily raises with increasing the processor numbers; in the region typical for supercomputers, is not usable any more.

4. Characterizing supercomputer architecture

In supercomputers, the "sequential part" is technically of different origin, but has the same effect on \((1 - \alpha_{eff})\). The recent Chinese supercomputer (Fu et al. (2016)) provided also performance data, from which diagrams on Fig 2 were derived. Compare these values (and consider the different scales!) to the former supercomputer data (Karp and Flatt (1990)) shown in Fig 2; the change is imposing. The new Chinese supercomputer is not only good in energy consumption, and the raw computing power, but also the coordination of the parallel work is excellently organized (the scale is the same as in Fig 1 where inside-chip organization takes place, although there the benchmark is different).
5. Characterizing the supercomputer timeline

When comparing the performance scales one sees an imposant change in the performance. There are (not fully detailed) data available on site TOP500.org (2016), covering the "supercomputer age", so using the data $R_{max}$ and $R_{peak}$, and using Equ. (5), $(1 - \alpha)$ can be calculated in function of time and ranking, see Fig. 3. It looks like $(1 - \alpha)$ changes in an exponential-like way, both with the time and the ranking in a given year. To establish a more quantitative description, it is worth to derive a timeline for the past 24 years. In Fig. 4, the $(1 - \alpha)$ values are displayed, for the top 3 supercomputers, in function of the time. The figure also contains the diagram of the best $(1 - \alpha)$ in the year, which confirms that high computing performance strongly correlates with the efficiency of parallelization. It looks like this development path (independently of technology, manufacturer, number and type of processors) shows a semi-logarithmic behavior, and only part of the tendency is caused by the Moore-observation. It is able to forecast the expected behavior of performance in the coming years, and its validity can provoke debates like the Moore observation does.

Figure 4: Timeline of supercomputer parallelism
6. Conclusions

The recently introduced figure of merit "effective parallelization" can excellently used to characterize the quality of hardware implementation, too. In addition to qualifying manual or compiler optimized parallelization, it can qualify the effect of method of inter-core communication in SoC, can characterize "goodness" of supercomputer implementation. Since a single figure of merit describing their performance can be attached to the supercomputers, the timeline of the development of supercomputing technology can be described. Interestingly enough, the timeline of the introduced parameters follow a tendency, similar to the Moore "law".

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