Multiple-Fault-Tolerant Strategy for Three-Phase Hybrid Active Neutral Point Clamped Converters Using Enhanced Space Vector Modulation Technique

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ABSTRACT In recent decades, renewable energy has become an important part of the power generation field. In any renewable energy system, power converters form the dominant part, owing to their important role. However, such converters are exposed to the danger of single and/or multiple open- and short-circuit faults. This paper proposes a creative control strategy for tolerating the faults by generating a new switching sequence and reference signals in hybrid active natural point clamped (ANPC) converters. The hybrid ANPC converters are exposed to consequent short- or open-circuit faults simultaneously for each kind of faults. In these regards, the operation under multi-short-circuit and multi-open-circuit faults are analyzed and described. Correspondingly, the control strategy with the selection of new vectors under the faulty conditions is explained and clarified in detail. Furthermore, the proposed strategy does not require installing any additional devices or changing the original topology, and it can be applied to hybrid ANPC converters without any special requirements to withstand high voltage levels. The effectiveness of the proposed control strategy is verified and confirmed by simulation results and experimentally tested using a 15-kW hybrid ANPC prototype converter.

INDEX TERMS Fault tolerance, multiple faults, open circuit, short circuit, hybrid ANPC.

I. INTRODUCTION
Among all types of energy, renewable energy has the widest applicability in electricity generation. It provides reliable energy with less or even no harmful greenhouse gases (GHG) at a suitable cost; this results in more utilization of such systems. Therefore, the recent developments in energy systems requested improvements in the quality of power converting systems, which is considered one of the most important parts of the generation system. Such systems with a wide range of power converters can withstand medium and high-power ranges. Among the various topologies, three-level neutral point clamped (NPC) converters have received increased attention in recent decades. Nevertheless, NPC converters have the main drawback in that the distribution of the losses is uneven; thus, two additional switches were added to form active NPC (ANPC) converters to solve the uneven loss distribution. ANPC and NPC converters have been compared to verify the reliability of ANPC converters over NPC converters [1], the crucial results of which proved the high reliability of ANPC converters over the conventional NPC converters. ANPC converters were further improved by using a hybrid combination of two Si–IGBTs and SiC-MOSFETs, which resulted in a higher ability to work under higher switching frequency with lower switching losses, as reported in [2].

Some studies proposed to find new multi-level topologies for medium and high-power applications that could use the minimum number of switching devices with the highest
possible efficiency [3]–[5]. In these regards, in any power
conversion system, the switching devices are vulnerable to
failure due to different reasons such as high voltage, current,
and physical-manufacturing limitations. The rate of failure
exceeds 30% and may reach 50%, including the gate-drive
faults [6]. When a fault occurs in any device (i.e., switching
device), the voltage stress on the other devices may increase
and cause an imbalance in the output. Moreover, the reliabil-
ity and safety of the system will be affected [6]. The faults are
mainly classified into two categories: open and short circuit
faults [7]. Fault detection plays a crucial role in the field
of energy systems. Most of the fault detection methods can
detect the fault by analyzing the output current waveform
by observing the distortion in the current using methods
such as Park’s transformation and slope [8]. Other methods
have been established based on learning technology to detect
open-circuit faults in three-level inverters as reported in [9].
In recent years, the topic of diagnosis and detection of faults
has been widely discussed and studied [10]–[14]. Faults have
significant effects either on time or even frequency domains,
to accurately realize the fault diagnostic actions [10].

The algorithms employing time-domain analyses are domi-
nant in fault diagnosis. Commonly selected diagnostic vari-
ables are the derivative of the inverter input current [11],
circulating current with/without the output voltage [12], [13],
and the associated diode voltages [14]. Most of these meth-
ods have been proposed and employed extensively for dif-
ferent multi-level inverter topologies. Hence, many studies
have been developed to solve the problems associated with
the faults of different topologies, as reported in [15]–[20].
In these studies, the authors proposed a method for open
fault tolerance in T-type inverters by considering the turn-on
time. Similarly, another study proposed the dwelling time to
tolerate the open fault in T-type inverters by considering
the turn-on and turn-off time scheme [15]. Some studies
introduced the diagnosis of short circuits faults (SCFs) in
dc-dc converters, as reported in [16], which can detect the
fault and identify the fault location with a short response
time of up to less than one cycle. Another study discussed
the fault detection and tolerance for a grid-connected T-type
converter using space vector modulation (SVM) under open
fault conditions [18], [19], while the fault is detected within
a period of current. The usage of additional hardware was
presented in [20]. In general, most studies have focused on
 tolerance of faults by adding new parts to the main topol-
yogy [21]. Therefore, the need for fault tolerance and the capa-
bility of re-operating the power system adequately and safely
has drawn considerable interest during the past decade [22].

As a consequence, enhancing the performance of the power
electronics systems by performing a proper control strategy
to effectively handle the faulty conditions without any inter-
ruption is regarded as an important measurement for a wide
range of power electronics applications [23]. The usage of
additional hardware was presented in [24]. The application of
an additional leg (fourth leg) is proposed to maintain healthy
operation under the fault conditions. Similarly, the usage of
a redundant leg for SiC devices of ANPC converters has also
been proposed [25]. In the same manner, fault tolerance
strategies were used to perform the healthy operation for other
topologies as shown in [20], [26]–[29]. The main purpose
is to recover a healthy operation during the fault. In gen-
eral, the addition of extra devices to the original topology
balances the neutral point voltage and obtains the output for
continuous operation. In contrast, the extra switching devices
would result in complex combinations in addition to increas-
ing the weight and cost of the system. Consequently, many
fault tolerance methods were proposed in the literature for
NPC and T-type topologies. Some benchmark studies such
as [30], consider using the carrier-based control strategy
to tolerate open-circuit faults in a three-level T-type rectifier in
a grid-connected system. The purpose is to consider the reduc-
tion of the loss and balancing the neutral point voltages at the
same time. In this paper, the authors divided the time intervals
of the fault into two main categories; normal time interval
(NTI), and abnormal time interval (ATI). While during the
first-time interval NTI, within the switching period, a time
offset is set to reduce the loss and balance the neutral point
voltage. Whereas, in the second time interval ATI, the fault
is divided into two conditions; the faulty condition of half-
bridge switches, and neutral point switches. Moreover, the
simulation and experimental works considered a wide range
of the AC voltage (75 – 150) V, resistance (50 – 75) Ω, and
modulation index (0.435 – 0.87) at 300 DC link voltage.
The outcomes of this paper result in establishing a healthy
operation by balancing the neutral point voltages and reduce
the associated losses. Some papers focused on tolerating the
faults by inserting additional hardware parts to the basic
topology which results in increasing the system cost which
could be regarded as a huge drawback as shown in [31]–[33].
However, these control schemes do not completely remove
the current distortion when an open circuit fault occurs. Also,
they could not be applied to other topologies such as hybrid
ANPC due to the differences in the topology configuration
and working principle. Besides, none of these studies is devel-
oped to tolerate the effects of multi open/short circuit faults
among the same phase leg and maintain healthy operation
under the faulty conditions. As multi open/short faults could
have more serious effects on the system performance and may
lead to damage at different parts of the inverter. Sequentially,
in terms of the different basic topologies between the NPC,
T-type, and the hybrid ANPC in addition to their switching
sequences and topologies performance. It could be concluded
that in the case of the fault at different switches the fault
tolerance which is applied to conventional NPC and T-type
could not be applied to the hybrid ANPC. These topologies
are based on the optimum switching concerning four IGBT
switches in each phase leg, while in the case of hybrid ANPC
there six switches which generate additional issues mainly in
the case of faults, thus the need of finding a method that can
be applied on the hybrid ANPC is highly needed. Therefore,
this paper proposed a creative method that can be applied
to the hybrid ANPC to recover the healthy operation and
eliminate the fault effects on the system and is necessary to improve the reliability of its applications. Besides, the proposed topology can eliminate the output distortion and works on balancing the DC links voltages and thus enhance the system performance under the multi open/short faults without the need of using any additional parts. The hybrid ANPC converters are exposed to consequent short- or open-circuit faults simultaneously for each kind of faults. In these regards, the operation under multi-short-circuit and multi-open-circuit faults are analyzed and described. These could be established by adding new voltage references, and voltage offset to the original waveforms. Moreover, finding new switching sequences under the faulty conditions, deep explanations are shown in the following sections.

Open/short circuit faults have a direct influence on the system and are hence regarded as the most common faults in power converters. Therefore, this paper proposes an effective fault tolerance control strategy to retain healthy operation under multiple faults, including multi-open- and multi-short-circuit faults for hybrid ANPC converters by changing the vector mapping, creating new switching sequences, generating new voltage references, and calculating the regenerated voltage offsets for the proposed system. The proposed strategy in this paper provides an effective technique to operate under multi-open- or multi-short-circuit faults simultaneously without the need of using any additional devices or changing the system configuration.

The rest of the paper is organized as follows. Section II includes the modeling configuration of hybrid ANPC converters. In section III, a detailed description of faults occurring in the converter is presented. Section IV presents an analysis of the proposed fault tolerance strategy. Section V contains the main simulation results supported by experimental verification. Finally, the conclusion is presented in section VI.

II. MODELING CONFIGURATION OF HYBRID ANPC CONVERTERS

The basic topology of the hybrid ANPC converter is shown in Fig. 1. The basic configuration consists of four Si-IGBT (Sx1/Dx1 to Sx4/Dx4) and two SiC-MOSFET (Qx1/DQx1 and Qx2/DQx2) switches and the associated diodes in each phase’s leg, for a total of 12 Si-IGBT and 6 SiC-MOSFET switches, to offer all necessary explanations as well as focused on Sx1/Dx1, Sx2/Dx2, and Qx1/DQx1 to describe the fault cases and the proposed method, as symmetrical behavior was found for other phases and switching devices. Meanwhile, it is worth noting that the topologies of conventional three-level ANPC, NPC, and T-Type converters are different from the hybrid ANPC topology, and to explain the differences, the switching behavior should be clarified. Where the proposed fault tolerance methods for the conventional ANPC, NPC, and the T-Type converters are different from the hybrid ANPC topology, and to explain the differences, the switching behavior should be clarified. Where the proposed fault tolerance methods for the conventional ANPC, NPC, and the T-Type converters are different from the hybrid ANPC topology, and to explain the differences, the switching behavior should be clarified.

In this study, we considered A phase to offer all necessary explanations as well as focused on Sx1/Dx1, Sx2/Dx2, and Qx1/DQx1 to describe the fault cases and the proposed method, as symmetrical behavior was found for other phases and switching devices. Meanwhile, it is worth noting that the topologies of conventional three-level ANPC, NPC, and T-Type converters are different from the hybrid ANPC topology, and to explain the differences, the switching behavior should be clarified. Where the proposed fault tolerance methods for the conventional ANPC, NPC, and the T-Type converters are different from the hybrid ANPC topology, and to explain the differences, the switching behavior should be clarified.

In the conventional topologies, four switching devices are employing Si-IGBT switches with the associated diodes in each switching device. Two additional active diodes and two active switches are added to the NPC and ANPC converters, respectively, to balance the uneven loss distribution of the NPC converter, as shown in Fig. 2. In T-Type converters, two switching devices work as half-bridge and another two as neutral point IGBTs. Similarly, NPC and ANPC inverters use two switches connected in series to block the full DC-link voltage compared to one switch in T-Type inverters. For these topologies, there are two loops for commutation paths.

| Switching states | Sx1 | Sx2 | Sx3 | Sx4 | Qx1 | Qx2 |
|------------------|-----|-----|-----|-----|-----|-----|
| P                | 1   | 0   | 1   | 0   | 1   | 0   |
| O+               | 1   | 0   | 1   | 0   | 0   | 1   |
| O−               | 0   | 1   | 0   | 1   | 0   |
| N                | 0   | 1   | 0   | 1   | 0   | 1   |

| TABLE 1. Normal switching sequence for hybrid ANPC converters. |

FIGURE 1. Basic circuit configuration of hybrid ANPC inverters.
The first path includes the inner loop, which starts when the current flows through the clamping diode \((D_{a6})\) with the outer switch \((S_{a4})\), whereas the second loop starts when the inner switch \((S_{a2})\) with either the inner diode \((D_{a3})\) or the outer diode \((D_{a4})\) based on the modulation scheme. Owing to the symmetrical structure of the top and bottom of these loops, it can be reflected in the remaining commutation loops. The ANPC converters followed the same switching scheme but with additional complementary switching of \((S_{a4}/S_{a5})\) and \((S_{a1}/S_{a6})\). Similarly, in T-Type converters, two main loops are active: the first comprises the current passing through the upper switch \((S_{a1})\) and inner switch \((S_{a2})\), and the other loop comprises the current passing through the lower switch \((S_{a4})\) and inner switch \((S_{a3})\), depending on the modulation scheme.

III. MULTI FAULT ANALYSIS

There are several studies on fault detection [3]–[6]; however, fault tolerance is considered only in this work, where the fault is assumed to have occurred and detected at a specific time. Under the healthy conditions, the inverter is operating according to the switching sequence summarized in Table 1. Under multiple faults, the system would behave in different ways as shown in Fig. 3. It is clear that in the case of an open circuit fault in \(S_{a2}/D_{a2}\) and \(Q_{a1}/D_{Qa1}\), the state \(O^-\) would be impossible to achieve when the current is the negative direction \((i_d < 0; \text{blue lines in the figure})\). Moreover, the state \(P\) would also be lost when the current is in the positive direction \((i_d > 0; \text{red lines in the figure})\) as shown in Fig. 3a. Another case of multiple open faults at \(Q_{a1}/D_{Qa1}\) and \(Q_{a2}/D_{Qa2}\) is shown in Fig. 3b; in this case, both states \(O^-\) and \(O^+\) are impossible to achieve in both cases when the current is positive and negative as well. The multiple-short case is shown in Fig. 3c; in this case, the main issue is the system continuously having the \(O^-\) and \(O^+\) states owing to the short case in \(S_{a2}/D_{a2}\) and \(S_{a3}/D_{a3}\). The faults prevent the system from achieving the requested voltage level. Fig. 3d shows the effects of multiple open faults in the upper MOSFET \(Q_{a1}/D_{Qa1}\) and lower IGBT \(S_{a4}/D_{a4}\). In this case, achieving the \(O^-\) state and \(N\) state is impossible owing to the open circuit in these devices. Furthermore, more fault cases are shown in Fig. 4. When multiple short faults occur at \(S_{a1}/D_{a4}\) and \(Q_{a2}/D_{Qa2}\), it is impossible to lose the \(P\) state and/or the \(O^+\) state because the short circuit opens the path from the upper part of the inverter at \(S_{a1}/D_{a1}\) down to the lower part at \(S_{a4}/D_{a4}\). Thus, it is not possible to realize complementary switching sequences as under healthy conditions. We now consider multiple faults in the lower part of the inverter, as shown in Fig. 4b, where an open fault occurs at the clamped end of the lower IGBT at \(S_{a3}/D_{a3}\) and \(S_{a4}/D_{a4}\). In this case, the \(O^+\) and \(N\) states are impossible to achieve owing to the open circuit faults. Consequently, multiple short faults in the upper part of the inverter at \(S_{a2}/D_{a2}\) and the upper MOSFET \(Q_{a1}/D_{Qa1}\) are shown in Fig. 4c. Due to the short circuit, the \(O^-\) state occurred continuously, following the normal switching sequence. Another important short fault may occur.
Safe and continuous operation are the main aims of any fault tolerance technique. Moreover, it is also important to enhance the reliability of the system under faulty conditions. It should be noted that most fault tolerance techniques have been proposed for conventional topologies and are limited to only those topologies. Besides, most techniques are limited to single open or short faults and use additional parts in the main topologies. Thus, although these strategies can recover healthy operation, they suffer from the above-mentioned drawbacks. Adding additional devices and/or changing the topology of the converter would increase the system control complexity as well as its cost. Moreover, the hybrid ANPC system is considered as a new topology different from ANPC and NPC topologies with a unique topology configuration and working principle. In this regard, this paper proposes an efficient fault tolerance strategy that does not require making any changes to the system configuration or any additional devices.

Under the faulty conditions, some current paths became inapplicable due to the loss of the control capability of the switching devices. The fault affects the switches in both cases open and short thus, the conventional switching strategy that is shown in Table 1 could not establish a healthy operation. Therefore, under the faulty conditions, the system needs to be controlled by a suitable control strategy that allows the system to handle the new working conditions. For example, when a multi open fault occurred at \( S_{a2}/D_{a2} \) and \( Q_{a1}/D_{Qa1} \), it’s impossible to control the aforementioned devices. Therefore, it’s necessary to find a suitable replacement for the current paths so that the system would recover the healthy operation. In these regards, the new switching sequences are shown in Table 2, which indicates the switching sequences at different states under the faulty condition which include multi open and short circuit failures. The switching sequence is applied to the faulty leg only, while the other legs continue working normally without the need for further modifications. In addition to the proposed sequence, a new voltage reference should be applied to the faulty phase leg as well as the other legs. The pole reference voltages to be applied to the hybrid ANPC are described as follows:

\[
\begin{align*}
V_a &= MI \cdot \sin(\omega t) \\
V_b &= MI \cdot \sin(\omega t - \frac{2\pi}{3}) \\
V_c &= MI \cdot \sin(\omega t + \frac{2\pi}{3})
\end{align*}
\]  

(1)

For instance, the faulty leg is assumed to be in the A-phase with zero voltage as a reference, while other new references are applied at the B- and C- phases with a 120° phase shift. Hence, the new voltage references can be calculated as follows.

\[
\begin{align*}
V_a &= 0 \\
V_b &= MI \cdot \sqrt{3} \cdot \sin(\omega t + \frac{2\pi}{3}) \\
V_c &= MI \cdot \sqrt{3} \cdot \sin(\omega t - \frac{2\pi}{3})
\end{align*}
\]  

(2)

Here, \( V_a, V_b, \) and \( V_c \) are the voltage references for the A-, B-, and C- phases, respectively; \( t \) is the time, \( \omega \) is the fundamental frequency; and \( MI \) is the modulation index. As it is clear that \( MI \) is reduced by a ratio of 0.577 to avoid overmodulation. The effects of the new switching sequence are clearly shown in the new vector sequence. As an example, for the case of multiple open circuit faults at \( Q_{a1}/D_{Qa1} \) and \( S_{a2}/D_{a2} \), the original vector sequence under healthy conditions and the new sequence after applying the proposed switching, voltage references, and voltage offset are shown in Table 3. Taking sector 3(i) as an example, the original sequence is \( NON, NPN, OPN, OPO, OPI, \) and \( NON \), and when the proposed method was applied, the sequence became \( OON, \)
TABLE 2. New switching sequence under multi open/short circuit faults.

| Faulty device | Switching status |
|---------------|------------------|
|              | \( S_{M1} \) | \( S_{M2} \) | \( S_{M3} \) | \( S_{M4} \) | \( Q_{M1} \) | \( Q_{M2} \) |
| \( S_{M2}/D_{M2} \) and \( Q_{M2}/D_{Q2} \) | 0 | Open Fault | 0 | 0 | Open Fault | 1 |
| \( Q_{M2}/D_{Q2} \) and \( Q_{M2}/D_{Q2} \) | 1 | 0 | 1 | 0 | 0 | Open Fault |
| \( S_{M2}/D_{M2} \) and \( S_{M3}/D_{M3} \) | 0 | Short Fault | 0 | 1 | 0 | 0/1 |
| \( S_{M3}/D_{M3} \) and \( S_{M4}/D_{M4} \) | 0 | 0 | 0 | 0 | 0 | Short Fault |
| \( S_{M5}/D_{M5} \) and \( Q_{M5}/D_{Q5} \) | 0 | Short Fault | 0 | 1 | 0 | 0/1 |
| \( S_{M5}/D_{M5} \) and \( Q_{M5}/D_{Q5} \) | 0 | 0 | 0 | 0 | 0 | Short Fault |
| \( S_{M6}/D_{M6} \) and \( Q_{M6}/D_{Q6} \) | 0 | Short Fault | 1 | 0 | 0 | 0/1 |

ONN, OON, OOO, OON, ONN, and OON. Fig. 5 illustrates the proposed vector sequences under both normal and post-fault conditions. The new sequence indicates that the \( P \) and \( N \) vectors in the faulty phase (A-phase) cannot be achieved as per the proposed switching sequences in Table 2.

Moreover, the proposed method was calculated as a new voltage offset (\( V_{sn} \)). This voltage offset has the advantage of maintaining the hybrid switching of the SiC-MOSFET devices as required. The calculated method is shown in Fig. 6; it is clear that the new offset is recalculated by considering the new voltage references and then by comparing these references to determine the maximum, minimum, and medium values. Finally, based on the obtained values, the new \( V_{sn} \) can be calculated. This process should be carried out at each switching cycle. Here, \( V_{max} \) and \( V_{min} \) are the maximum and minimum reference voltages, respectively. It is also necessary to modify the new \( V_{sn} \) so that it has the same frequency as the fundamental frequency (i.e., 50 Hz).

TABLE 3. Normal and proposed switching vectors for hybrid ANPC.

| Sector | Normal switching | Proposed switching |
|--------|-----------------|--------------------|
| Sector 1(i) | POO, PNO, PNN, ONN | OOP, ONO, OOP, ONO |
| Sector 1(ii) | OON, PNN, PNO, PPO | ONO, ONO, ONO, ONO |
| Sector 2(i) | OON, PON, PPO, PNO | NOO, ONO, ONO, ONO |
| Sector 2(ii) | OON, OPO, PPO, ONO | NOO, OOO, OOO, OOO |
| Sector 3(i) | NON, NPN, PNO, OPO | OOO, OOO, OOO, OOO |
| Sector 3(ii) | NNO, NOO, NPO, OPO | OOO, OOO, OOO, OOO |
| Sector 4(i) | NOO, NPO, OPN, OPO | OPN, OOO, OOO, OOO |
| Sector 4(ii) | NOP, OPO, NOP, NOO | OPO, OPO, OPO, OPO |
| Sector 5(i) | NOP, NPP, NNO, NPP, NPO | OPO, OPO, OPO, OPO |
| Sector 5(ii) | NNO, NNP, ONP, OOP, OPO | OPO, OPO, OPO, OPO |
| Sector 6(i) | POP, NPN, ONP, OPO | OPO, OPO, OPO, OPO |
| Sector 6(ii) | POP, NPN, ONP, OPO | OPO, OPO, OPO, OPO |

FIGURE 5. Vector sequence in case of multi open fault at \( Q_{a1}/D_{Qa1} \) and \( S_{a1}/D_{Qa1} \): (a) healthy conditions and (b) after applying the proposed method.
instead of a frequency that is three times more than the fundamental frequency under normal operating conditions (i.e., 150 Hz). The most important part is to include all the voltage references, including the new faulty phase reference, when calculating the new voltage offset \( V_{sn} \). Only applying the new voltage offset would be insufficient in achieving the goal of maintaining a healthy operation. Therefore, following the switching sequences shown in Table 2 for both MOSFET and IGBT switching devices considering the new voltage reference, we clarify vector selection for each fault case for multiple open and multiple short circuit faults.

V. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

To verify the effectiveness of the proposed method for short circuit fault tolerance in hybrid ANPC converters, this section analyzed a part of the simulation results. Fig. 7 shows the results of different multiple open circuit faults. Fig. 6a shows the effects of open faults at \( S_{a2}/D_{a2} \) and \( Q_{a1}/D_{a1} \). In this figure, the line-to-line voltage \( (V_{ab}) \), pole voltage \( (V_{an}) \), load current \( (I_a) \), and the DC capacitor voltages \( (V_{C1} \text{ and } V_{C2}) \) of the A-phase before and after the fault occurs are shown. Meanwhile, as fault detection is not a focus of this study, the fault is assumed to occur and be detected at \( t = 0.05 \text{ s} \).

In the same manner, the results shown in Fig. 7b to Fig. 7d indicates the effects on \( V_{ab} \), \( V_{an} \), \( I_a \), \( V_{C1} \), and \( V_{C2} \) after an open fault at \( S_{a4}/D_{a4} \), \( Q_{a1}/D_{a1} \), \( S_{a3}/D_{a3} \), \( S_{a4}/D_{a4} \), \( S_{a2}/D_{a2} \), and the...
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FIGURE 9. Line-to-line voltage between A-phase and B-phase, pole voltage for A-phase, load current for A-phase, and capacitor voltages of the DC-link under healthy and faulty conditions with multiple short faults at (a) $S_{a2}/D_{a2}-S_{a3}/D_{a3}$, (b) $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, (c) $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, and (d) $S_{a2}/D_{a2}-Q_{a2}/D_{Qa2}$.

FIGURE 10. Line-to-line voltage between A-phase and B-phase, pole voltage for A-phase, load current for A-phase, and capacitor voltages of the DC-link under healthy conditions and after applying the proposed method with multiple short faults at (a) $S_{a2}/D_{a2}-S_{a3}/D_{a3}$, (b) $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, (c) $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, and (d) $S_{a2}/D_{a2}-Q_{a2}/D_{Qa2}$.

It is clear that each fault has different effects on system performance. Therefore, it is important to suitably select a vector for each fault as explained in the previous section. This selection should be based on the new switching sequence shown in Table 2, the new reference voltages, and the new voltage offset. The effect of applying the proposed method on the system is shown in Fig. 8. Meanwhile, the hybrid switching frequency (50 Hz for IGBT and 30 kHz for MOSFET) should be set, as presented in Table 2; thus, the inverter can continue to balance the losses. Additionally, the DC-link balancing capability of the hybrid ANPC converter should be satisfied, to some extent, concerning the location of the fault. This is verified in Fig. 8a to Fig. 8d. Consequently, Fig. 9 shows the effects of multiple short circuit faults. Fig. 9a presents the effects on $V_{ab}$, $V_{an}$, $I_a$, $V_{C1}$, and $V_{C2}$ after multiple short circuit faults at $S_{a2}/D_{a2}-S_{a3}/D_{a3}$. Fig. 9b to Fig. 9d show the result of faults at $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, $S_{a2}/D_{a2}-Q_{a1}/D_{Qa1}$, and $S_{a2}/D_{a2}-Q_{a2}/D_{Qa2}$, respectively. The proposed method is applied to the inverter while using the proposed switching sequences, as explained in the previous sections. Multiple short circuit faults have more serious effects because of the dependence on the MOSFET switches in the hybrid ANPC inverter, as shown in Table 1. Moreover, the instant and fast discharge of the DC link capacitors can result in an extremely high current (i.e., in the order of kA), which can severely damage the system components. However, by using the proposed method of including new voltage references and suitably selecting new vectors by following the new switching sequences, the system performance can be improved and healthy operation can be recovered.

B. EXPERIMENTAL RESULTS

To verify the proposed fault tolerance method, a 15 kW HANPC inverter prototype is used. Fig. 11 shows the experimental setup of this study. The main experimental
parameters are the same as those shown in Table 4. The power devices used are SEMIKRON-SK75GBB066T (Si IGBT) and CREE–C2M0040120D (SiC MOSFET) modules along with a TMS320F28335 digital signal processor (DSP) control board manufactured by Texas Instruments (TI).

TABLE 4. Simulation parameters.

| Parameter                  | Value   |
|----------------------------|---------|
| Inductance                 | 1 mH    |
| Resistance                 | 10 Ω    |
| Fundamental frequency      | 50 Hz   |
| IGBT switching frequency   | 50 Hz   |
| MOSFET switching frequency | 30 kHz  |

The normal operation of the three-level hybrid ANPC converter is shown in Fig. 12a, which indicates the line-to-line voltage ($V_{ab}$), pole voltage ($V_{an}$), three-phase load currents, and the DC link voltages ($V_{C1}$ and $V_{C2}$) of the A-phase under normal operation before the fault occurs while the modulation index is at its peak value of 1. Fig. 12b shows the result of applying the proposed method after multiple open faults occur at $Q_{a1}/D_{Qa1}$-$Q_{a2}/D_{Qa2}$. The proposed method improves the system performance with the modulation index reduced to 0.577 compared to its original value under healthy operation (i.e., 1), as explained in the previous sections. Meanwhile, the experimental verification of multiple open
circuit faults at $\frac{S_{d1}/D_{d1}}{Q_{a1}/D_{Qa1}}$ is shown in Fig. 12c. The proposed method can improve the reliability in different multiple open fault cases. Fig. 8d confirms the effectiveness of the proposed control strategy in balancing the DC link voltages for all cases of multiple open faults. Meanwhile, Fig. 12d presents the balanced DC link voltages ($V_{C1}$ and $V_{C2}$) after applying the proposed control scheme.

The result of applying the proposed algorithm on multiple short circuit faults is shown in Fig. 13. The normal operation of the system is the same as that shown in Fig. 12a. The result of a short circuit fault at $\frac{S_{d2}/D_{d2}}{S_{a2}/D_{a2}}$ and $\frac{S_{d2}/D_{d2}}{Q_{a1}/D_{Qa1}}$ are shown in Fig. 13a and Fig. 13b, respectively. Where the line-to-line voltage ($V_{dl}$) and pole voltage ($V_{an}$) after applying the proposed fault tolerance strategy are shown. The results confirm the capability of the proposed method in maintaining healthy operation under multiple short circuit faults. Meanwhile, Fig. 13c presents the balanced DC link voltages ($V_{C1}$ and $V_{C2}$) after applying the proposed control scheme. Owing to the limitation of the experimental setup and because of the general safety requirements when dealing with high short circuit currents, as explained in section III and Section IV, the fault is assumed to occur and be detected after a certain time, and the system performance results are shown after the proposed algorithm is applied.

The results confirmed the capability of the proposed method in recovering the healthy operation of the system under multiple open and short circuit faults. It also balanced the DC-link voltages ($V_{C1}$ and $V_{C2}$) with a reduced MI.

VI. CONCLUSION
An effective control method for realizing the healthy operation of hybrid ANPC converters under multiple open and short circuit faults was proposed in this paper. The avoidance of open/short circuit loops by creating new switching sequences and new voltage references were clarified. The faults were assumed to occur within multiple switches of the converter owing to the different effects of the fault with reference to the faulty switch. The faults and their effects were illustrated and explained. The selection of new vectors under faulty conditions was clarified in detail. Moreover, open/short faults at different locations were thoroughly investigated. Additionally, the associated effects of each fault were highlighted and illustrated. The proposed method was explained in terms of the mathematical and theoretical calculation of the new voltage references and the new offset voltage; the proposed switching sequences were clarified in detail. Finally, the effectiveness of the proposed method was demonstrated through simulation and experimental verification for all cases of short circuit faults. The proposed method was verified theoretically by the simulation results and experimentally by using a 15-kW prototype inverter setup.

REFERENCES
[1] J. Li, S. Englebretson, and A. Q. Huang, “Reliability comparison for 3L-NPC and 3L-ANPC converters for drives application,” in Proc. IEEE Int. Electr. Mach. Drives Conf. (IEMDC), Niagara Falls, ON, Canada, May 2011, pp. 271–276.
[2] Q. Guan, C. Li, Y. Zhang, W. Shuai, and D. Xu, “An extreme high efficient three-level active neutral-point-clamped converter comprising SiC & Si hybrid power stage,” IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8341–8352, Oct. 2018.
[3] M. D. Siddique, S. Mekhlief, N. M. Shah, A. Sarwar, A. Iqbal, M. Tayyab, and M. K. Ansari, “Impact of switching frequency based asymmetrical multilevel inverter topology with reduced switch count,” IEEE Access, vol. 7, pp. 86374–86383, 2019.
[4] M. D. Siddique, S. Mekhlief, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, “A new multilevel inverter topology with reduce switch count,” IEEE Access, vol. 7, pp. 58584–58594, 2019.
[5] B. Chokkalingam, M. S. Bhaskar, S. Padmanaban, V. K. Ramachandaramurthy, and A. Iqbal, “Investigations of multi-carrier pulse width modulation schemes for dual active neutral point clamped multilevel inverters,” J. Power Electron., vol. 19, no. 3, pp. 702–713, May 2019.
[6] B. Lu and S. K. Sharma, “A literature review of IGBT fault diagnostic and protection methods for power inverters,” IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1770–1777, Jul. 2009.
[7] Y. Song and B. Wang, “Survey on reliability of power electronic systems,” IEEE Trans. Power Electron., vol. 28, no. 1, pp. 591–604, Jan. 2013.
[8] J.-S. Lee, K.-B. Lee, and F. Blaabjerg, “Open-switch fault detection method of a Back-to-Back converter using NPC topology for wind turbine systems,” IEEE Trans. Ind. Appl., vol. 51, no. 1, pp. 325–335, Jan. 2015.
[9] S.-H. Kim, D.-Y. Yoo, S.-W. An, Y.-S. Park, J.-W. Lee, and K.-B. Lee, “Fault detection method using a convolution neural network for hybrid active neutral-point clamped inverters,” IEEE Access, vol. 8, pp. 140632–140642, Jul. 2020.
[10] F. Bento and A. J. Marques Cardoso, “Open-circuit fault diagnosis and fault-tolerant operation of interleaved DC–DC boost converters for homes and offices,” IEEE Trans. Ind. Appl., vol. 55, no. 5, pp. 4855–4864, Sep. 2019.
[11] E. Ribeiro, A. J. M. Cardoso, and C. Boccaletti, “Open-circuit fault diagnosis in interleaved DC–DC converters,” IEEE Trans. Power Electron., vol. 29, no. 6, pp. 3091–3102, Jun. 2014.
[12] A. Ghazanfari and Y.-A.-R.-I. Mohamed, “A resilient framework for fault-tolerant operation of modular multilevel converters,” IEEE Trans. Ind. Electron., vol. 63, no. 5, pp. 2669–2678, May 2016.
[13] K. Bi, Q. An, J. Duan, L. Sun, and K. Gai, “Fast diagnostic method of open circuit fault for modular multilevel DC/DC converter applied in energy storage system,” IEEE Trans. Power Electron., vol. 32, no. 5, pp. 3292–3296, May 2017.
[14] H. Givi, E. Farjah, and T. Ghanbari, “Switch and diode fault diagnosis in nonisolated DC–DC converters,” IEEE Trans. Power Electron., vol. 30, no. 5, pp. 2517–2533, May 2015.
[15] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, “Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy,” IEEE Trans. Power Electron., vol. 30, no. 5, pp. 2660–2673, May 2015.
[16] U.-M. Choi, K.-B. Lee, and F. Blaabjerg, “Diagnosis and tolerance strategy of an open-switch fault for T-type three-level inverter systems,” IEEE Trans. Ind. Appl., vol. 50, no. 1, pp. 495–508, Jan. 2014.
[17] J.-S. Lee and K.-B. Lee, “An open-switch fault detection method and tolerant controls based on SVM in a grid-connected T-type rectifier with unity power factor,” IEEE Trans. Ind. Appl., vol. 56, no. 2, pp. 1606–1615, Feb. 2018.
[18] K.-B. Lee and J.-S. Lee, “Reliability Improvement Technology for Power Converters,” Cham, Switzerland: Springer, 2017.
[19] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, “Study and handling methods of power IGBT module failures in power electronic converter systems,” IEEE Trans. Power Electron., vol. 30, no. 5, pp. 4613–4623, Oct. 2017.
[20] W. Zhang, D. Xu, P. N. Enjeti, H. Li, T. J. Hawke, and H. S. Krishnamoorthy, “Survey on fault-tolerant techniques for power electronic converters,” IEEE Trans. Power Electron., vol. 29, no. 12, pp. 6319–6331, Dec. 2014.
[21] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardneau, “Survey on fault operation on multilevel inverters,” IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2207–2218, Jul. 2010.
[24] E. Pazouki, J. A. De Abreu-Garcia, and Y. Sozer, “Short circuit fault diagnosis for interleaved DC-DC converter using DC-link current emulator,” in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Tampa, FL, USA, Mar. 2017, pp. 230–236.

[25] R. Katebi, J. He, and N. Weise, “An advanced three-level active neutral-point-clamped converter with improved fault-tolerant capabilities,” IEEE Trans. Power Electron., vol. 33, no. 8, pp. 6897–6909, Aug. 2018.

[26] U.-M. Choi, J.-S. Lee, F. Blaabjerg, and K.-B. Lee, “Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter,” IEEE Trans. Power Electron., vol. 31, no. 10, pp. 7234–7247, Oct. 2016.

[27] B. H. Kwon, S.-H. Kim, S.-M. Kim, and K.-B. Lee, “Fault diagnosis of open-switch failure in a grid-connected three-level Si/SiC hybrid ANPC inverter,” Electronics, vol. 9, no. 3, p. 399, Feb. 2020.

[28] H.-K. Ku, J.-H. Jung, J.-W. Park, J.-M. Kim, and Y.-D. Son, “Fault-tolerant control strategy for open-circuit fault of two-parallel-connected three-phase AC-DC two-level PWM converter,” J. Power Electron., vol. 20, pp. 1–12, May 2020.

[29] X.-X. Zheng and P. Peng, “Fault diagnosis of wind power converters based on compressed sensing theory and weight constrained Adaboost-SVM,” J. Power Electron., vol. 19, no. 2, pp. 443–453, 2019.

[30] J. Chen, C. Zhang, X. Xing, and A. Chen, “A fault-tolerant control strategy for T-type three-level rectifier with neutral point voltage balance and loss reduction,” IEEE Trans. Power Electron., vol. 35, no. 7, pp. 7492–7505, Jul. 2020.

[31] B. Wang, Z. Li, Z. Bai, P. T. Krein, and H. Ma, “A redundant unit to form T-type three-level inverters tolerant of IGBT open-circuit faults in multiple legs,” IEEE Trans. Power Electron., vol. 35, no. 1, pp. 924–939, Jan. 2020.

[32] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, “Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives,” IEEE Trans. Power Electron., vol. 27, no. 2, pp. 519–533, Feb. 2012.

[33] S.-Z. Xu, C.-J. Wang, and Y. Wang, “An improved fault-tolerant control strategy for high-power ANPC three-level inverter under short-circuit fault of power devices,” IEEE Access, vol. 7, pp. 55443–55457, 2019.

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