COMPARATIVE ANALYSIS OF MC-SPWM AND MSVPWM FOR SEVEN LEVEL DIODE CLAMPED MULTILEVEL INVERTER

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Abstract

Multilevel inverters are superior to the two-level inverters to meet medium and high-power applications. A seven-level diode-clamped multilevel topology (7L-DCMT) proposed, and compare the advantages and disadvantages of various control strategies such as multilevel space vector pulse width modulation (MSVPWM) with multicarrier sinusoidal pulse width modulations (MCSPWM) named as level shift and phase shift PWM based on the position of carriers at certain frequency. In level shift is further divided and compare the Inphase disposition sinusoidal pulse width modulation (IPD-SPWM), phase opposition and disposition-sinusoidal pulse width modulation (POD-SPWM), alternate phase opposition and disposition-sinusoidal pulse width modulation (APOD-SPWM) and carrier phase displacement sinusoidal pulse width modulation (CPD-SPWM). The 7L-DCMT designed with MATLAB/SIMULINK and the performance can analyses based on the observing total harmonic distortion (THD) at different control strategies.

Keywords: Seven level diode-clamped multilevel inverter, Multicarrier sinusoidal pulse width modulation, level shift, phase shift, Multilevel Space vector pulse width modulation.

I. Introduction

Conventionally, two-level (TL) inverters used in DC-AC power conversion[VI],[VII],[XXI] and its output becomes a square wave in nature. These TL inverters are used in applications of high - voltage DC transmission, adjustable
speed drives, integration of renewable energy, switch-mode power supply, traction drives. However, TL inverters are suffering from a few downsides such as low output waveform quality, high filter requirement values, consistently high total harmonic distortion (THD), more upper switching stress, lower efficiency and higher electromagnetic emission (EMI) [IX],[X],[XIV],[XXIV]. The above drawbacks overcome by preferring the sustainable structure of inverter called multilevel (ML) inverters with the high quality of waveform and ability[VIII].

ML inverters are indeed too classified as three types: Diode clamped ML inverters (DC-MLI), flying capacitor ML inverters (FC-MLI) and cascaded H-bridge ML inverters (CHB-MLI)[XVII]. Among these structures, DC-MLI extensively used in industry because of its simple switch control and a low - complexity protective circuit. Due to the fact that the ML inverter output voltage is a modulated staircase, the output waveform consists of a series of non-essential elements, known as harmonic compositions[XI],[XXIII]. To measure the harmonic content of any waveform total harmonic distortion (THD) is described. The amplitude of harmonics will increase THD and thus the resulting quality of output decreases. The THD output approaches zero with increasing the number of inverter output stairs [I], [XVI], [XVIII].

The ML inverter performance depends on the type of modulation control strategies used for switching them[XX]. The most precise methods used in MLIs are multicarrier pulse width modulation (MCPWM), and multilevel space vector pulse width modulations (MSVPWM) operated with high switching frequency[II], [XXII]. The SVPWM is famous as it produces a small harmonic distortion, higher flexible in the choosing of the switching process and a satisfactory digital execution. The SVPWM approach, however, involves extensive, tedious computations such as identification of sector/subsector, calculation of switching times, and optimal selection of vectors[III],[V],[XII],[XIII],[XV],[XIX]. The operation of seven level diode clamped multilevel inverter (7L-DCMLI) describes in section II. In section III discuss the results of 7L-DCMLI with various control strategies with FFT spectrum and finally concluded with best PWM and is adopted for further work.

II. 7 Level Diode Clamped Multilevel Inverter

The 7L-DCMLI as shown in Fig. 1. In DC-MLI, employs diode clamps and connected cascaded capacitors to generate multilevel ac voltage waveforms. The circuit represents, six bulk capacitors as C1, C2, C3, C4, C5, and C6 are connected in a pattern for splitting the dc bus voltage \( V_{dc} \) with a same voltage across of \( V_{dc}/6 \) and generates the seven stepped output phase voltage waveform. The midpoint of each two capacitors can be described as the neutral point N.

In Figure 1, the numbering
order of the 6 positive group switches are IA1, IA2, IA3, IA4, IA5, IA6 and other are form negative group such as IA1’,IA2’,IA3’,IA4’,IA5’ and IA6’ per each leg. The phase voltage levels are \( V_{dc}/2, V_{dc}/3, V_{dc}/6,0,-V_{dc}/6,-V_{dc}/3,-V_{dc}/2 \) as shown in Fig. 2. and levels of line voltage as \( V_{dc}, 5V_{dc}/6, 2V_{dc}/3, V_{dc}/2, V_{dc}/3, V_{dc}/6, 0, -V_{dc}/6, -V_{dc}/3, -V_{dc}/2, -2V_{dc}/3, -5V_{dc}/6, -V_{dc} \) as shown in Fig. 3.

The switching states of 7L-DCMLI as shown in Table-1, “1” stands for ON and “0” for OFF of the device.

![Diagram](image1)

**Fig. 1.** 7 level Diode Clamped Inverter Configuration

![Graph](image2)

**Fig. 2.** Phase Voltage of 7 level DC-MLI output voltage

![Graph](image3)

**Fig. 3.** Line Voltage of 7 level DC-MLI output voltage
Table 1: Switching States for Phase A of 7L-DCMLI

| Phase Voltage | Line to Line Voltage | Device Switching States of Phase A leg |
|---------------|----------------------|----------------------------------------|
| IA1 | IA2 | IA3 | IA4 | IA5 | IA6 | IA1' | IA2' | IA3' | IA4' | IA5' | IA6' |
| + Vdc/2 | Vdc | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| + Vdc/3 | 5Vdc/6 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| + Vdc/6 | 2Vdc/3 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | Vdc/2 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| - Vdc/6 | Vdc/2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| - Vdc/3 | Vdc/6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| - Vdc/2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

The multi-stepped phase voltage synthesized by taking the neutral N as the reference point. For \( V_{AN} = +V_{dc}/2 \), the positive group of switches \( I_{A1}-I_{A6} \) are turned on, for \(+V_{dc}/3\) switched on \( I_{A2}-I_{A6} \) from the positive group and switched on \( I_{A1}' \) from the negative group. For voltage level, \(+V_{dc}/6\) obtained from turn on the switches of \( I_{A3}-I_{A6} \) from positive and switched on \( I_{A1}'-I_{A3}' \) from the negative group. For \( V_{AN}=0 \), to turn on the equal switches \( I_{A4}-I_{A6} \) from the positive and \( I_{A1}'-I_{A3}' \) negative group. To obtain the negative alternation majorly conduction of negative group switches and minor from positive group switches, as shown in Table-1. At any time for 7 level inverter, a set of six switches are on. The main features of the DC-MLI inverter are High voltage rating for blocking diodes, Unequal switching device rating, and capacitor voltage unbalance.

In general, for “p” number of levels, the components required and levels of output phase and line voltage for DC-MLI as shown in Table-2.

Table 2: Components requirement, levels of Phase and Line voltage for p-level & 7L-DCMLI

| Devices | p-level DC-MLI | 7-level DC-MLI |
|---------|----------------|----------------|
| Main Switching Devices & Diodes | \(2(p-1)\) | 12 |
| Clamping Diodes | \((p-1) \times (p-2)\) | 30 |
| Capacitors in DC Link | \(p-1\) | 6 |
| No.of output phase voltage levels | \(p\) | 7 |
| No.of output line voltage levels | \((2p-1)\) | 13 |
| Voltage withstand by each switching device | \(V_{dc}/(p-1)\) | \(V_{dc}/6\) |
| Voltage across of each DC link capacitor | \(V_{dc}/(p-1)\) | \(V_{dc}/6\) |
III. PWM Control Strategies

Modulation of pulse width control strategies used in a conventional inverter can be modified and to be used in multilevel inverters, these are extensions from the standardized two-level inverters. Based on the advantages of the multilevel inverter PWM control strategies can be categorized based on switching frequency, as shown in Fig. 4.

![PWM Control Strategies for Multilevel Inverters](image)

In this work, high switching frequency PWM is proposed; among these, the preferable PWM control strategies are multicarrier-based sinusoidal PWM (MCSPWM) and Multilevel Space Vector PWM (MSVPWM).

**Multicarrier Sinusoidal Pulse Width Modulation (MCSPWM)**

In MCSPWM, a sinusoidal signal with fundamental frequency is compared with high-frequency carrier signal to generated required control pulses. MCSPWM mainly divided into two types based on the placements of multicarrier are, level shifted modulation and phase-shifted modulation.

**Level Shifted MC-SPWM**

In this control strategy, p-level DC-MLI requires (p-1) level-shifted triangular carriers with the same frequency and amplitude. The (p-1) triangular carriers are placed vertically such that the bands they occupy are contiguous.

The frequency modulation index,

\[ m_f = \frac{f_c}{f_m} \]  

(1)

Where \( f_c \) = frequency of carrier signals and \( f_m \) = frequency of modulated wave

Modulation Amplitude index,

\[ m_a = \frac{V_m}{V_{cr(p-1)}} \]  

for \( 0 \leq m_a \leq 1 \)  

(2)

Where \( V_m \) = maximum magnitude of modulated signal, \( V_{cr} \) = maximum magnitude of each carrier wave

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Level shifted control strategies are further categorized into in-phase disposition PWM (IPD-PWM), phase opposition and disposition PWM (POD-PWM), and alternative phase opposite and disposition (APOD-PWM).

**In-Phase Disposition Sinusoidal PWM (IPD-SPWM)**

In this IPD-PWM, all the triangular carrier signals are in-phase and as level shifted, as shown in Fig.5. For the generation of control pulses, high-frequency carrier signals are $C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5},$ and $C_{r6}$ comparing with fundamental three phase sinusoidal signals $V_R, V_Y, V_B$. The generated control signals are applied to corresponding switches of each phase leg of the proposed inverter.

**Phase Opposition Disposition Sinusoidal PWM (POD-SPWM)**

In this POD-SPWM, the triangular carrier signals are in-phase above zero reference line and below the same reference carrier signals are in the same phase, as shown in Fig.6. But the triangular carriers signals below and above the zero reference line are out of phase by 180°. For the generation of control pulses, high-frequency carrier signals are $C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5},$ and $C_{r6}$ comparing with fundamental three-phase sinusoidal signals $V_R, V_Y, V_B$. The generated control signals are applied to corresponding switches of each phase leg of the proposed inverter.

**Alternative Phase Opposition Disposition Sinusoidal PWM (APOD-SPWM)**

In this APOD-SPWM, the triangular carrier signals are alternatively out of phase by 180°, as shown in Fig.7. For the generation of control pulses, high-frequency carrier signals are $C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5},$ and $C_{r6}$ comparing with fundamental three-phase...
sinusoidal signals $V_R$, $V_Y$, $V_B$. The generated control signals are applied to corresponding switches of each phase leg of the proposed inverter.

**Carrier Phase Displaced Sinusoidal PWM (CPD-SPWM)**

In CPD-SPWM, the triangular carrier signals are vertically placed with same frequency and magnitude but are phase displaced by each other by 60 degrees, as shown in Fig.8. For the generation of control pulses, high-frequency carrier signals are $C_{r1}$, $C_{r2}$, $C_{r3}$, $C_{r4}$, $C_{r5}$, and $C_{r6}$ comparing with fundamental three-phase sinusoidal signals $V_R$, $V_Y$, $V_B$. The generated control signals are applied to corresponding switches of each phase leg of the proposed inverter.

The phase angle is calculated by,

$$\theta_{cr} = \frac{360^\circ}{(p - 1)}$$

**Phase Shifted MCSPWM**

In Phase shifted MCSPWM for p-level DC-MLI, $(p-1)$ triangular carrier signals are needed but each signal phase shift by $360^\circ/(p-1)$ by each other. Here 7L-DCMLI proposed, the necessary high frequency triangular signals are 6 from $C_{r1}$ to $C_{r6}$, and phase-shifted by each other by 60 degrees apart as shown Fig. 9. These carrier signals have the same frequency and same peak to peak amplitude. This signals are compared with fundamental modulated three-phase signals $V_R$, $V_Y$, $V_B$ to generate the control pulses and are applied for appropriate switches in DC-MLIs.
Multilevel Space Vector PWM (MSVPWM) for 7L-DCMLI

Multilevel Space vector pulse width modulation (MSVPWM) is more advent than multicarrier PWM due to highly appropriate for implementing digital signal processing, enhanced the use of the DC bus, reduced total harmonic distortion (THD), the fundamental output voltage become higher, higher effective performance. In this work, the generalized n-level SVPWM is used and is to be proposed for the implementation of 7L-DCMLI. In MSVPWM, for a p-level inverter, switching states are $p^3$ and a number of triangles are $(6(p-1))^2$ in space vector diagram. In MSVPWM, pulses can be generated directly from the reference instantaneous phase voltage and triangular approach without using a lookup table. To obtain switching vectors with its actual associate vector by the principle of mapping by suitable switching sequence for an MLI from a two-level algorithm.

The principle procedure for generation of MSVPWM pulses as follows,

1. Layer and Center Identification are held with the tip of the reference space vector.
2. Mapping the space vector reference to an inner sub-hexagon sector.
3. To determine the changing switching vector duration and adequate switching sequence by using two-level algorithm.
4. By adding the vector at the center of subhexagon to generating required switching vectors for DC-MLI.

To identify the operating level of a p-level inverter can be driven by control of the modulation index (MI) between two to “p” and tip of the revolving reference vector $V_r$. Two-level to seven level layers in MSVPWM spectrum, as shown in the Fig.10, represented from $l = 2$ to $l = 7$. The equation (4) can identify the operating level of 7L-DCMLI,

$$l = \text{int} \left( \frac{V_{\text{ref}}}{MI} \right) + 2$$

(4)

Where,

$$MI = \frac{V_{dc}}{(p-1)}$$

(5)

The magnitude of the reference vector is, 

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The supporting vector can be evaluated by using the following, consider \((x_1, y_1, z_1)\) and \((x_2, y_2, z_2)\) are the end vectors of the center hexagon and for level "l" be \((x_{l1}, y_{l1}, z_{l1})\) and \((x_{l2}, y_{l2}, z_{l2})\) are inner side of end vectors. Hence, the each state of the supporting vectors are generated as by using equation (5) & (6). The complete switching states as shown in Fig.11.

\[
V_s = \sqrt{V_{d1}^2 + V_{d2}^2} 
\]

(6)

\[
(x_{l1}, y_{l1}, z_{l1}) = (l - 1) \ast (x_1, y_1, z_1) + (m - 1) \ast \delta
\]

(7)

\[
(x_{l2}, y_{l2}, z_{l2}) = (l - 1) \ast (x_2, y_2, z_2) + (m - 1) \ast \delta
\]

(8)

Where,

\[
\delta = difference \ vector \ = (x_2, y_2, z_2) - (x_1, y_1, z_1)
\]

(9)

and

\[
m = supporting \ vector \ in \ each \ state = l - 1
\]

Substitute equation (10) in equation (7) & (8),

Therefore, \(x_{l1}, y_{l1}, z_{l1}\) = \(m \ast (x_1, y_1, z_1) + (m - 1) \ast \delta\) \hspace{1cm} (11)

Next, to identify the closest vector to the tip of the reference space vector \(V_s\) can be done by measuring the distance "\(d_j\)" of each supporting vector from \(V_s\).

\[
d_j = |V_{d1} - V_{dsv}| + |V_{d2} - V_{dsv}|
\]

(13)

Where \((V_{d1}, V_{d2})\) and \((V_{dsv}, V_{dsv})\) are the coordinates of the reference vector \(V_s\) and supporting vectors respectively.

To find space states of the higher level of SUBHEXAGON by reverse mapping by using the following relation,

\[
(x_0, y_0, z_0) = (x_0, y_0, z_0) + (x_c, y_c, z_c)
\]

(14)

Where \((x_0, y_0, z_0)\) and \((x_c, y_c, z_c)\) are the switching states of two level inverter and center of the outer subhexagon. For example the state vector (5,4,0) obtained by...
adding the center of SUBHEXAGON-I to SUBHEXAGON-II. Therefore vector (5,4,0) = (0,0,0)+(5,4,0).
In this proposed method, the inverter output voltages are generated automatically without using any lookup tables and need not require to identify the tip of reference vector $V_r$ for MLIs.

![Fig11.7L-DCMLI Space vector plane](image)

**IV. Results & Discussion**

The performance of three-phase 7-level DC-MLI has been studied by comparing the line voltage THDs at linear modulation index (LMI) for a level shift, phase shift and multilevel space vector PWM (MSVPWM) and finally concluded with best. The n-1 capacitors are used for n-level MLIs, capacitors are used to distribute the applied voltage depending on the capacitance value. For 7L-DCMLI, voltage across each capacitor is $V_{dc}/(7-1)$. Each switching unit has to block a voltage an amount of $V_{dc}/(7-1)$, but the clamping diodes need to block distinct voltage depending on their switching states. The 7L-DCMLI analyzed on and displayed results are based on open loop scenario.

**Level Shift PWM:**
**In Phase Disposition PWM (IPDPWM)**

In this IPDPWM, the modulation index (MI) is 0.866 at the switching frequency of 5000Hz. Fig.12(a) shows the phase voltage of one leg, (b) for one leg of line voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 300 V and THD of 13.24% for 7L-DCMLI.
In this PODPWM, the modulation index (MI) is 0.866 at the switching frequency of 5000Hz. Fig.13(a) shows the phase voltage of one leg, (b) for one leg of line voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 300 V and THD of 21.64% for 7L-DCMLI.
Fig 13. (a) Phase Voltage (b) Line Voltage of single leg (c) Three phase line voltage & (d) Line Voltage FFT spectrum of PODPWM for 7L-DCMLI.

Alternative Phase Opposition Disposition PWM (AODPWM)

In this AODPWM, the modulation index (MI) is 0.866 at the switching frequency of 5000Hz. Fig.14(a) shows the phase voltage of one leg, (b) for one leg of line voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 300.1 V and THD of 18.92% for 7L-DCMLI.

Fig 14. (a) Phase Voltage (b) Line Voltage of single leg (c) Three phase line voltage & (d) Line Voltage FFT spectrum of AODPWM for 7L-DCMLI.

Carrier Phase Displaced Sinusoidal PWM (CPD-SPWM)

In CPD-SPWM, the modulation index (MI) is 0.866 at the switching frequency of 5000Hz. Figure 15(a) shows the phase voltage of one leg, (b) for one leg of line

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voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 300.1 V and THD of 21.21% for 7L-DCMLI.

Fig 15.(a) Phase Voltage (b) Line Voltage of single leg (c) Three phase line voltage & (d) Line Voltage FFT spectrum of CPDSPWM for 7L-DCMLI.

Phase Shift PWM (PSPWM)
In PSPWM, the modulation index (MI) is 0.866 at the switching frequency of 5000Hz. Fig.16(a) shows the phase voltage of one leg, (b) for one leg of line voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 299.7 V and THD of 18.82% for 7L-DCMLI.
Multilevel Space Vector PWM (MSVPWM)

In MSVPWM, the MI is 0.866 at the switching frequency of 5000Hz. Fig. 17(a) shows the phase voltage of one leg, (b) for one leg of line voltage (c) for three phase line voltage (d) indicates that line voltage FFT spectrum with fundamental voltage of 383 V and THD of 12.16% for 7L-DCMLI.

The simulated AC output voltage for 7 level DC-MLI as shown in the above figure and is operated with different control strategies. The comparison of THD and fundamental voltage is tabulated in below Table 3.
Table 3. Comparison of Control Strategies

| PWM Technique | Fundamental Voltage | THD (%) |
|---------------|---------------------|---------|
| IPD           | 300                 | 13.24   |
| POD           | 300                 | 21.64   |
| APOD          | 300.1               | 18.92   |
| CPD           | 300.1               | 21.12   |
| PS            | 299.7               | 18.80   |
| SVPWM         | 383                 | 12.16   |

V. Conclusion

The DC-MLI is a simplest topology and circuit configuration have less complexity, due to its advantages it is more popular in recent applications mainly in an interfacing of grid connected renewable energy sources and speed adjustable drives. In this work, 7 level DC-MLI is simulated using different control strategies with multi carrier sinusoidal PWM (MC-SPWM) and Multilevel Space Vector PWM (MSVPWM). In this comparative analysis, the proposed MSVPWM technique achieved low THD and better fundamental voltage. Due to the better performance of MSVPWM technique with DC-MLI, is extensively used in future work of single stage grid connected Photovoltaic system.

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