A 14bit 500MS/s 85.62dBc SFDR 66.29dB SNDR SHA-less pipelined ADC with a stable and high-linearity input buffer and aperture-error calibration in 40nm CMOS

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Abstract This paper presents a 14bit 500MS/s SHA-less pipelined analog-to-digital converter (ADC) implemented in 40nm CMOS. A high-linearity pseudo-differential push-pull input buffer with an anti-oscillation technique and a nonlinear parasitism eliminate technique is proposed to stably drive the pipelined stages while keeping low distortion. Moreover, a digital controlled aperture-error calibration is also employed with offset of comparators compensated in advance. Measurement results show that the ADC achieves a signal-to-noise-and-distortion-ratio (SNDR) of 66.29dB and a spurious-free-dynamic-range (SFDR) of 85.62dBc at 80.1MHz input.

Keywords: pipelined ADC, push-pull, input buffer, offset compensated, aperture-error calibration

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the rapid development of wireless communication systems and measurement instruments, the demands for high-speed and high-resolution analog-to-digital converters (ADCs) are increasing [1]. Among the variety of ADC architectures, such as flash [2, 3, 4], folding [5, 6, 7], successive approximation register (SAR) [8, 9, 10] sigma-delta (ΣΔ) [11, 12, 13] and so on, the pipelined ADC offers a balance between sampling rate and resolution [14, 15]. Due to the requirement of high performance and low power consumption, it is preferred to eliminate the power-hungry front-end sample-and-hold amplifier (SHA) [16], which is usually called as SHA-less. And in such a SHA-less ADC architecture, a high-linearity input buffer is usually employed to make the ADC core easier to drive, and to reduce the kick-back noise from the sampling network [17]. However, the input buffer in front of the pipelined stages should be linear enough to reduce the impact on the whole ADC performance. Besides, due to the timing skew and bandwidth mismatch between two sampling networks, the input signal sampled by the multiplying digital-to-analog converter (MDAC) and sub-ADC of the first pipelined stage can be different after removing the front-end SHA, which is called as aperture-error, may also deteriorate the performance of the pipelined ADC [18].

In this paper, a high-linearity push-pull input buffer with an anti-oscillation technique and a nonlinear parasitism eliminate technique is proposed to drive the pipelined stages with high stability and low distortion. The aperture-error is calibrated with digital-analog mixed technique. With similar deterioration results, the aperture-error is difficult to recognize from comparators’ offset in digital circuits, so an aperture-error calibration with offset of comparators compensated is employed in advance.

This paper is organized as follows: Section 2 introduces the ADC topologies, the detail designs of the input buffer, and the calibration technique. Section 3 reports the measured results and the conclusion is drawn in Section 4.

2. Topologies and implementation

A top-level block diagram of the ADC is depicted in Fig. 1, which shows a SHA-less pipelined architecture with an input buffer, six 2.5bit pipelined stages and a 2bit back-end flash sub-ADC. The input buffer is designed to reduce the kick-back noise from the sampling capacitors and directly drive a 500MS/s MDAC resolving 2.5bit. The input buffer and the MDAC amplifiers are designed at a 2.5V supply, while the clocks, switches and comparators use a 0.8/1.7V supply domain.

To deal with the capacitor mismatches between sampling capacitors and feedback capacitors, a digital capacitor-mismatch calibration is employed [19] for both stage1 and stage2 of the ADC. The schematic diagram of stage1 is shown in Fig. 2. The extra capacitor \( C_{aux} \) is added to avoid the ADC working out of the range during calibrating. The mismatch of each sampling capacitor is quantified by the back-end ADC, and the pseudorandom noise (PN) series are used to get a statistical result and the mismatch is compensated in digital circuits.

![Fig. 1 Top-level block diagram of the ADC](image-url)
2.1 Input buffer

It is necessary for a high-speed high-resolution pipelined ADC to employ a low-distortion and power-efficient input buffer to achieve high performance. The input buffer usually has a high input impedance and low output impedance and can protect the input signal from the kick-back noise of sampling capacitances and charge injection [20].

Conventionally, the input buffer composed of an NMOS source follower is usually applied [21, 22, 23], which is shown in Fig. 3. The input impedance is given as [24]

\[ Z_{in} = \frac{1}{sC_{GS}} + \left(1 + \frac{g_m}{sC_{GS}}\right) \frac{1}{g_{mb} + sC_L} \]  

(1)

If the input frequency is low enough, then \( g_{mb} \gg |sC_L| \), and \( Z_{in} \approx \frac{1}{sC_{GS}} \left(1 + \frac{g_m}{g_{mb}}\right) \frac{1}{g_{mb}} \). However, when the frequency arises high enough, \( g_{mb} \ll |sC_L| \), and for a given \( s = j\omega \), the input impedance consists of the series combination of capacitors and a negative resistance equal to \( -\frac{g_m}{sC_{GS}C_L} \), which may cause instability. The circuit can oscillate at \( \omega = \frac{g_m}{C_{GS}C_L} \).

Beside the instability, the buffer shown in Fig. 4 also suffers from severe non-linearity, such as current and drain-source voltage (\( V_{DS} \)) variation of \( M_1 \), body effect if the bulk of the \( M_1 \) is connected to VSS, et al. A common approach to eliminate the body effect is just tying the bulk terminal to the source of \( M_1 \), as shown in Fig. 5. However, though the body effect has been eliminated, the nonlinear parasitic capacitor between the PW and DNW (\( C_{d1n} \)) and the parasitic capacitor between DNW and P-sub (\( C_{d2n} \)) would introduce a low-impedance path from the source of \( M_1 \) to VSS, especially at high frequencies. Similar effects would occur if \( M_1 \) is implemented in PMOS [17].

In this paper, a high-linearity low-power input buffer is proposed, which employs an anti-oscillation technique to eliminate the instability problem and a nonlinear parasitism elimination technique to reduce buffer performance degradation caused by layout nonlinear parasitism. Fig. 6 shows the simplified single-ended schematic of the proposed input buffer. It employs a complementary push-pull structure [25] to achieve low power consumption, which almost doubles the trans-conductance. The input signal \( V_{in} \) drives the input P-well to generate the independent potential. So, \( M_1 \) is usually fabricated in the isolated P-well (PW) to connect its source to bulk, as shown in Fig. 5. However, though the body effect has been eliminated, the nonlinear parasitic capacitor between the PW and DNW (\( C_{d1n} \)) and the parasitic capacitor between DNW and P-sub (\( C_{d2n} \)) would introduce a low-impedance path from the source of \( M_1 \) to VSS, especially at high frequencies. Similar effects would occur if \( M_1 \) is implemented in PMOS [17].
devices (M₂, M₃) by the level shift capacitors. And the cascode devices (M₁, M₄) is further level shift, which boost the drain voltages of M₂/M₃ to reduce the $V_{DS}$ variation [17]. A 2.5V power supply is taken for the input buffer. M₁~M₄ are biased by resistors ladder to ensure they are all in the saturation region.

To protect the circuits from oscillation because of the negative resistance mentioned above, an anti-oscillation technique is employed. Shown in Fig. 6, the small resistor $R_3$ is connected between the gate of M₁ and the level shift capacitor C₁, which is the same for the small resistor $R_4$. With the $R_3/R_4$ added, which are parallel connected with the negative resistance, the equivalent input impedance shown in Eq. (2) becomes positive. Thus, the input buffer could drive the back-end circuits stably.

$$Z'_m = \frac{R_n R_3}{R_n + R_3} > 0 \tag{2}$$

where $R_n = \frac{g_m}{\omega^2 C_{GS} C_L}$ is the negative resistance, and $R_3 \ll |R_n|$, in this work, $R_3 = R_4 = 1\ \Omega$.

As mentioned above, the drain voltage of M₂ would be deteriorated due to the nonlinear parasitic capacitors C₁₂n and C₉₂n. Based on the approach, the bulk voltage follows the source of M₁ shown in Fig. 4, thus a nonlinear parasitism eliminate technique is proposed. The large resistor ($R_1$) is added between the source and bulk of the M₁. Then the impedance seen from the source of M₁ can be expressed as $Z_S = R_1 + \frac{1}{j\omega C_{DS}} + \frac{1}{j\omega C_{GS}} \approx R_1$, in this work, $R_1 = R_2 = 1k\ \Omega$, the low-impedance path could be eliminated by $R_1$. Meanwhile, the $R_1$ provides M₁ with a steady source-bulk voltage, which would not be affected by the nonlinear parasitic capacitors and hence improves the linearity. For the same purpose, a large resistor ($R_2$) is also inserted between the bulk and source of M₄.

As shown in Fig. 7 a), with the resistances $R_3$&$R_4$, the output voltage of buffer strive to a final potential more quickly after sampling, the resistances help the input buffer to eliminate the instability problem. Fig. 7 b) shows that the resistances $R_1$&$R_2$ improve the overall SFDR performance of the ADC.

### 2.2 Comparator and aperture-error calibration

Comparator is a key module for sub-ADCs [26]. Fig. 8 shows the adopted structure of the comparators and the non-overlap clock. In the amplification phase $\Phi_2$, the reference voltage is connected to the bottom plate of the capacitor and the top plate is connected with common voltage. In the sampling phase $\Phi_1$, the input signal is sampled and the compared signal is directly amplified by the pre-amplifier. In the phase $\Phi_1n$ rather than the phase $\Phi_2$ the latch generates the output codes. By this approach, the codes for DACs’ switches are already prepared when the MDAC begins to work in the amplification phase $\Phi_2$. Therefore, it spares more time for the amplifier of MDAC, which relaxes the unit bandwidth requirement of the operational amplifier in the MDAC.

However, due to the separated sampling network, bandwidth mismatch and sampling timing skew between the MDAC and sub-ADC in the first pipelined stage, probably causes aperture error and deteriorates the performance of the whole ADC at a high-frequency large-swing input [27]. Moreover, as for the adopted comparator structure, the signal goes through the pre-amplifier introducing an extra-large delay $\Delta T_{pre}$. And for a sinusoidal input, this error can be approximated as:
\[ \Delta V_{err} = A \cdot 2\pi f_{in} \cdot (\Delta T_S + \Delta T_B + \Delta T_{pre}) \] (3)

Where \( A \) is the peak amplitude and \( f_{in} \) is the frequency of the input signal, \( \Delta T_S \) is timing skew, \( \Delta T_B \) is caused by the bandwidth mismatches between the two networks and \( \Delta T_{pre} \) is the delay introduced by the pre-amplifier.

Aperture-error calibration is needed especially for a large-amplitude and high-frequency input according to Eq. (3). The calibration algorithm in [28] would reduce the aperture-error caused by timing skew and the bandwidth mismatch. However, with similar deterioration results, the aperture-error is difficult to recognize from comparators’ offset in digital circuits, thus it is necessary to compensate the comparator offset before dealing with the aperture-error. Besides, when solving the aperture-error, the contribution of the pre-amplifier delay as a main factor needs to be focused, which does not mention in reported works [29].

In this work, an aperture-error calibration algorithm with comparator offset compensating in advance is applied. In the offset compensation technique, the input of the pre-amplifier is shorted with each other and a 6bit current steering DAC in SAR algorithm is employed to correct the offset, which is controlled digitally.

Directly correlative with the aperture-error, the statistic number of over-range points in a given period can be used as a judgment to overcome the aperture-error. Comparing the current number with the former one, the digital module controls the delay time of the sampling clock of switches between the pre-amplifier and latch until the number is alike. This calibration is almost achieved in digital domain except a simple delay line, which costs little.

3. Measurement results

The 14bit pipelined ADC is fabricated in a 40nm CMOS technology. Fig. 9 illustrated the layout and micrograph of the ADC. The occupied area of the proposed ADC is 1.05mm².

The measurement results are shown in Fig. 10. The ADC achieves an SFDR of 85.62dBc and an SNDR of 66.29dB at 80.1MHz input signal under 500MS/s with 2.5V supply and consumes only 270mW.

Table I [30, 31, 32] shows the comparisons of state-of-the-art ADCs with sampling rate in excess of 120MHz and resolution over 12bit. The figure of merit (FOM) is calculated with the following expression.

\[ FOM = \frac{Power}{2^{ENOB} \cdot f_s} \] (4)

4. Conclusion

In this paper, a 14bit 500MS/s SHA-less pipeline ADC is presented. A high-linearity pseudo-differential push-pull input buffer with an anti-oscillation technique and a nonlinear parasitism eliminate technique is proposed to drive the pipelined stages stably and eliminate the nonlinearity of layout. The ADC employs a digital controlled calibration to correct the aperture-error. And to eliminate the distribution of the comparator offsets on the aperture-error reorganization, the comparator offset is compensated in advance in the adopted aperture-error calibration. As the input signal is 80.1MHz, the ADC reaches 85.62dBc SFDR and 66.29dB SNDR with the power consumption of 270mW.
References

[1] Y. Chen, et al.: “A wide-band input buffer for 3GS/s 12bit time-interleaved ADC,” IEEE International Conference on Solid-State and Integrated Circuit Technology (2016) (DOI: 10.1109/ICSCIT.2016.798771).

[2] P.C. Scholten, et al.: “A 6-b 1.6-Gsample/s flash ADC in 0.18-μm CMOS using averaging termination,” IEEE J. Solid-State Circuits 37 (2002) 1599 (DOI: 10.1109/JSSC.2002.804334).

[3] C.-Y. Chen, et al.: “A low power 6-bit flash ADC with reference voltage and common-mode calibration,” IEEE J. Solid-State Circuits 44 (2009) 1041 (DOI: 10.1109/JSSC.2009.201709).

[4] S. Shahramian, et al.: “A 35-GS/s, 4-bit flash ADC with active data and clock distribution trees,” IEEE J. Solid-State Circuits 44 (2009) 1709 (DOI: 10.1109/JSSC.2009.202067).

[5] A.G.W. Venes, et al.: “An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing,” IEEE J. Solid-State Circuits 31 (1996) 1846 (DOI: 10.1109/4.545804).

[6] R.C.Taft, et al.: “A 1.8 V 1.0 GS/s 10b self-calibrating unified-folded-interpolation ADC with 91 ENOB at Nyquist frequency,” IEEE J. Solid-State Circuits 44 (2009) 3294 (DOI: 10.1109/JSSC.2009.2032634).

[7] J.V. Valburg, et al.: “An 8-b 650-MHz folding ADC,” IEEE J. Solid-State Circuits 27 (1992) 1662-1666 (DOI: 10.1109/4.173091).

[8] K. Doris, et al.: “A 480 mW 2.6 GS/s 10b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS,” IEEE J. Solid-State Circuits 46 (2011) 2821 (DOI: 10.1109/JSSC.2011.2164961).

[9] T. Miki, et al.: “A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC with SNR and SFDR enhancement techniques,” IEEE J. Solid-State Circuits 50 (2015) 1372 (DOI: 10.1109/JSSC.2015.2417803).

[10] J. Fang, et al.: “A 5-GS/s 10-b 76-mW time-interleaved SAR ADC in 28 nm CMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers 64 (2017) 1673 (DOI: 10.1109/TCSI.2017.2661481).

[11] C.C. Lee, et al.: “A 14b 23MS/s 48mW resetting ΣΔ ADC with 87dB SFDR 11.7b ENOB & 0.5mm2 area,” IEEE Symposium on VLSI Circuits (2008) (DOI: 10.1109/VLSIC.2008.4585999).

[12] J. Ryckhaert, et al.: “A 2.4GHz 40mW 40dB SNDR/62dB SFDR 60MHz bandwidth mirrored-image RF bandpass ΣΔ ADC in 90nm CMOS,” IEEE Asian Solid-State Circuits Conference (2008) (DOI: 10.1109/ASSCC.2008.4708802).

[13] G. Mitteregger, et al.: “A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB,” IEEE J. Solid-State Circuits 41 (2006) 2641 (DOI: 10.1109/JSSC.2006.884332).

[14] W. Ke, et al.: “A 14-bit 100 MS/s SHA-less pipelined ADC with 89 dB SFDR and 74.5 dB SNR,” IEICE Electron. Express 12 (2015) 20150070 (DOI: 10.1587/exel.12.20150070).

[15] A. Panigada, et al.: “A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction,” IEEE J. Solid-State Circuits 44 (2009) 3314 (DOI: 10.1109/JSSC.2009.2032637).

[16] C.-Y. Chen, et al.: “A 12-bit 3 GS/s pipeline ADC with 0.4 mm2 and 500 mW in 40 nm digital CMOS,” IEEE J. Solid-State Circuits 47 (2012) 1013 (DOI: 10.1109/JSSC.2012.2185192).

[17] Y. Zhang, et al.: “A 14-bit 500-MS/s SHA-less pipelined ADC in 65nm CMOS technology for wireless receiver,” International Conference on Circuits, System and Simulation (2018) (DOI: 10.1109/CIRSYSIM.2018.8525871).

[18] D. James et al.: “Mitigating aperture error in pipelined ADCs without a front-end sample-and-hold amplifier,” International Conference on VLSI Design and International Conference on Embedded Systems (2018) (DOI: 10.1109/VLSID.2018.29).

[19] A.N. Karanicolas, et al.: “A 15-b 1-Msample/s digitally self-calibrated pipeline ADC,” IEEE J. Solid-State Circuits 28 (1993) 1207 (DOI: 10.1109/94.261994).

[20] Z. Wu, et al.: “An ADC input buffer with optimized linearity,” IEEE International Conference on Solid-State and Integrated Circuit Technology (2018) (DOI: 10.1109/ICSCIT.2018.8564827).

[21] K. Hadidi, et al.: “A highly linear cascade-driver CMOS source-follower buffer,” IEEE International Conference on Electronics, Circuits, and Systems (1996) (DOI: 10.1109/ICECS.1996.584657).

[22] I. Ahmed, et al.: “A capacitive charge pump based low power pipelined ADC,” Analog Circuits & Signal Processing (2010) 163 (DOI: 10.1007/978-90-481-6652-5_9).

[23] W.-C. Song, et al.: “A 10-b 20-Msample/s low-power CMOS ADC,” IEEE J. Solid-State Circuits 30 (1995) 514 (DOI: 10.1109/3.84164).

[24] B. Razavi: “Design of Analog CMOS Integrated Circuits” (McGraw-Hill, New York, 2017) 2nd ed. 173.

[25] B. Hershberg, et al.: “A 3.2GS/s 10 ENOB 61mW ringamp ADC in 16nm with background monitoring of distortion,” IEEE International Solid-State-Circuits Conference (2019) (DOI: 10.1109/JSSC.2019.8862290).

[26] A.M.A. Ali, et al.: “A 14 bit 1 GS/s RF sampling pipelined ADC with background calibration,” IEEE J. Solid-State Circuits 49 (2014) 2857 (DOI: 10.1109/JSSC.2014.2361339).

[27] C. Wang, et al.: “A 14-bit 250MS/s low-power pipeline ADC with aperture error eliminating technique,” IEEE International Symposium on Circuits and Systems (2018) (DOI: 10.1109/ISCAS.2018.8351100).

[28] S. Devarajan, et al.: “A 12-b 10-GS/s interleaved pipeline ADC in 28-nm CMOS technology,” IEEE J. Solid-State Circuits 52 (2017) 3204 (DOI: 10.1109/JSSC.2017.2747758).

[29] M. Brandolini, et al.: “A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS,” IEEE J. Solid-State Circuits 50 (2015) 2922 (DOI: 10.1109/JSSC.2015.2464684).

[30] M. Ni, et al.: “A 12bit 800MS/s time-interleaving pipeline ADC in 65nm CMOS,” IEEE International Conference on Electron Devices and Solid-State Circuits Digest of Technical Papers (2016) (DOI: 10.1109/EDSSC.2016.7785290).

[31] Z.K. Zhou, et al.: “A 12 bit 120 MS/s SHA-less pipeline ADC with capacitor mismatch error calibration,” IEICE Electron. Express 15 (2018) 20180481 (DOI: 10.1587/eelex.15.20180481).

[32] X.B. Chen, et al.: “A 14 bit 500 MS/s SHA-less pipeline ADC with a high linear input buffer and power-efficient supply voltage domain arrangement in 40 nm CMOS,” IEICE Electron. Express 16 (2019) 20190197 (DOI: 10.1587/eelex.16.20190197).

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