A Time-domain Analog Weighted-sum Calculation Model for Extremely Low Power VLSI Implementation of Multi-layer Neural Networks

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Abstract. A time-domain analog weighted-sum calculation model is proposed based on an integrate-and-fire-type spiking neuron model. The proposed calculation model is applied to multi-layer feedforward networks, in which weighted summations with positive and negative weights are separately performed in each layer and summation results are then fed into the next layers without their subtraction operation. We also propose very large-scale integrated (VLSI) circuits to implement the proposed model. Unlike the conventional analog voltage or current mode circuits, the time-domain analog circuits use transient operation in charging/discharging processes to capacitors. Since the circuits can be designed without operational amplifiers, they can operate with extremely low power consumption. However, they have to use very high resistance devices on the order of GΩ. We designed a proof-of-concept (PoC) CMOS VLSI chip to verify weighted-sum operation with the same weights and evaluated it by post-layout circuit simulation using 250-nm fabrication technology. High resistance operation was realized by using the sub-threshold operation region of MOS transistors. Simulation results showed that energy efficiency for the weighted-sum calculation was 290 TOPS/W, more than one order of magnitude higher than that in state-of-the-art digital AI processors, even though the minimum width of interconnection used in the PoC chip was several times larger than that in such digital processors. If state-of-the-art VLSI technology is used to implement the proposed model, an energy efficiency of more than 1,000 TOPS/W will be possible. For practical applications, development of emerging analog memory devices such as ferroelectric-gate FETs is necessary.

Keywords: time-domain analog computing, weighted sum, spike-based computing, deep neural networks, multi-layer perceptron, artificial intelligence hardware, AI processor

1 Introduction

Artificial neural networks (ANNs), such as convolutional deep neural networks (CNNs) [15] and fully-connected multi-layer perceptrons (MLPs) [2], have shown
excellent performance on various tasks including image recognition [21,31,30]. However, computation in ANNs is very heavy, which leads to high power consumption in current digital computers, and even in highly parallel coprocessors such as graphics processing units (GPUs). In order to implement ANNs at edge devices such as mobile phones and personal service robots, very low power consumption operation is required.

In ANN models, weighted summation, or multiply-and-accumulate (MAC) operation, is an essential and heavy calculation task, and dedicated complementary metal-oxide-semiconductor (CMOS) very-large-scale integration (VLSI) processors have been developed to accomplish it [29,31,28,11]. As an implementation approach other than digital processors, use of analog operation in CMOS VLSI circuits is a promising method for achieving an extremely low power consumption operation of such a calculation task [31,22,21]. Although the calculation precision is limited due to the non-idealities of analog operation such as noise and device mismatches, the neural network models and circuits can be designed to be robust to such non-idealities [24,10,7]. On the other hand, in the research field of ANN models, low-precision neural networks have been proposed and their comparable performance has been demonstrated, mainly in applications of image recognition [30]. These models facilitate the development of energy-efficient hardware implementations [22].

The time-domain weighted-sum calculation model was originally proposed based on mathematical spiking neuron models inspired by biological neuron behavior [18,19]. We have simplified and expanded this calculation model under the assumption of operation in analog circuits with transient states, and call its VLSI implementation approach “Time-domain Analog Computing with Transient states (TACT).” In contrast to conventional weighted-sum operation in analog voltage or current modes, the TACT approach is suitable for much lower power consumption operation in CMOS VLSI implementation of ANNs.

We have already proposed a device and circuit that performs time-domain weighted-sum calculation [26,31,25]. The proposed circuit consists of plural input resistive elements and a capacitor (RC circuit), which can achieve extremely low-power operation. The energy consumption could be lowered to the order of 1 fJ per operation, which is almost comparable to the calculation efficiency in the brain. We also proposed a circuit architecture to implement a weighted-sum calculation with different-signed weights with two set of RC circuits, one of which calculates positively weighted-sums while the other calculates negatively weighted-sums [32].

In this paper, we formulate the weighted-sum calculation model based on the TACT approach, and propose its applications to ANNs such as MLPs and CNNs. We also show simulation results of ANNs using the MNIST database in which the calculation results by the proposed model are compared with the ordinary numerical calculation results, and verify the usefulness of our model. We then evaluate the energy consumption of the proposed circuit by conducting post-layout circuit simulation of a CMOS circuit designed equivalently to the RC
A simple spiking neuron model, also known as an integrate-and-fire-type (IF) neuron model, is shown in Fig. 1[20]. In this model, a neuron receives spike pulses via synapses. A spike pulse only indicates the input timing, and its pulse width and amplitude do not affect the following processing. A spike generates a temporal voltage change, which is called a post-synaptic potential (PSP), and the internal potential of the $n$-th neuron, $V_n(t)$, is equal to the spatiotemporal summation of all PSPs. When $V_n(t)$ reaches the firing threshold $\theta$, the neuron outputs a spike, and $V_n(t)$ then settles back to the steady state.

Based on the model proposed in [13], a simplified weighted-sum operation model using IF neurons is proposed. Time span $T_{in}$ is defined, during which only one spike is fed from each neuron, and it is assumed that a PSP generated by a spike from neuron $i$ increases linearly with slope $k_i$ from the timing of the spike input, $t_i$, as shown in Fig. 1[11].
A required weighted-sum operation is that normalized variables \( x_i \) (\( 0 \leq x_i \leq 1 \), \( i = 1, 2, \ldots, N \)) is multiplied by weight coefficients \( a_i \), and the multiplication results are summed regarding \( i \), where \( N \) is the number of inputs. This weighted-sum operation can be performed using the rise timing of PSPs in the IF neuron model. Input spike timing \( t_i \) is determined based on \( x_i \) using the following relation:

\[
\begin{align*}
t_i &= T_{in}(1 - x_i), \\
x_i &= (1 - \frac{t_i}{T_{in}}).
\end{align*}
\]

(1) \hspace{2cm} (2)

Coefficients \( a_i \) are transformed into the PSPs’ slopes \( k_i \);

\[
k_i = \lambda a_i,
\]

(3)

where \( \lambda \) is a positive constant. If the firing time of the neuron is defined as \( t_\nu \), the following equation is easily obtained:

\[
\sum_{i=1}^{N} k_i (t_\nu - t_i) = \theta.
\]

(4)

If we define the following parameters:

\[
\beta = \sum_{i=1}^{N} a_i,
\]

(5)

we obtain

\[
\sum_{i=1}^{N} a_i \cdot x_i = \frac{\theta/\lambda + \beta(T_{in} - t_\nu)}{T_{in}},
\]

(6)

\[
= \frac{\theta}{\lambda T_{in}} + \beta(1 - \frac{t_\nu}{T_{in}}).
\]

(7)

Here, we assume that all the weights in the calculation have the same sign; i.e., \( a_i \geq 0 \) or \( a_i \leq 0 \) for all \( i \). When all inputs are minimum (\( \forall i \ x_i = 0 \)), the left side of Eq. (6) is zero. Then, the output timing \( t_\nu \) is given by

\[
t_{\nu}^{min} = \frac{\theta}{\lambda \beta} + T_{in}.
\]

(8)

On the other hand, when all inputs are maximum (\( \forall i \ x_i = 1 \)), the left side of Eq. (6) is \( \beta \), and the output timing \( t_\nu \) is given by

\[
t_{\nu}^{max} = \frac{\theta}{\lambda \beta}.
\]

(9)

The time span during which \( t_\nu \) can be output is \( [t_{\nu}^{max}, t_{\nu}^{min}] \), and its interval is

\[
T_{out} \equiv t_{\nu}^{min} - t_{\nu}^{max} = T_{in}.
\]

(10)
Thus, the time span of output spikes is the same as that of input spikes, $T_{in}$.

In this model, since the normalization of the sum of $a_i$ ($\beta = 1$) is not required (unlike in our previous work [18,19,31]), the calculation process becomes much simpler. When implementing the time-domain weighted-sum operation, setting the threshold potential $\theta$ properly is the key to making the operation work appropriately. As shown in Fig. 1, the earliest output spike timing has to be later than the latest input spiking timing $T_{in}$; that is, $t_{\nu}^{\text{max}} \geq T_{in}$. Thus,

$$\theta \geq \lambda \beta T_{in}. \quad (11)$$

Also, we can rewrite Eq. (11) as

$$\theta = \lambda \beta T_{in} + \delta, \quad (12)$$
$$\delta = \epsilon (\lambda \beta T_{in}), \quad (13)$$

where $\epsilon \geq 0$ is an arbitrarily small value. By substituting Eqs. (12) and (13) into Eqs. (8) and (9), we obtain

$$t_{\nu}^{\text{min}} = (2 + \epsilon)T_{in}, \quad (14)$$
$$t_{\nu}^{\text{max}} = (1 + \epsilon)T_{in}, \quad (15)$$

where $\epsilon T_{in}$ is considered as a time slot between input and output timing spans, as shown in Fig. 1 and $\epsilon$ determines the length of the slot. Also, the weighted summation expressed by Eq. (6) is rewritten as follows:

$$\sum_{i=1}^{N} a_i \cdot x_i = \beta [2 + \epsilon - \frac{t_{\nu}}{T_{in}}], \quad (16)$$

2.2 Time-domain Weighted-sum Calculation with Different-Signed Weights

We have proposed a time-domain weighted-sum calculation model with two spiking neurons, one of which is for all the positive weights and the other for all the negative ones [32]. We apply Eq. (6) to each neuron, and the two results are summed as the final result of the original weighted-sum. Here, we show the details of the model.

Let $a^+_i$ and $a^-_i$ indicate the positive and negative weights, respectively. We define

$$\beta^+ = \sum_{i=1}^{N^+} a^+_i \geq 0, \quad (17)$$
$$\beta^- = \sum_{i=1}^{N^-} a^-_i \leq 0. \quad (18)$$
where \( N^+ \) and \( N^- \) are the numbers of positive and negative weights, respectively;

\[
N = N^+ + N^-,
\]

\[
\sum_{i=1}^{N} a_i = \sum_{i=1}^{N^+} a_i^+ + \sum_{i=1}^{N^-} a_i^-,
\]

\[
\beta = \beta^+ + \beta^-.
\]

Thus, assuming \( \lambda = 1 \), Eq. (4) is rewritten for the positive and negative weighted-sum operations as follows:

\[
\sum_{i=1}^{N^+} a_i^+ (t_i^+ - t_i) = \theta^+ + \beta T_{in} - t_i^+ + \nu
\]

\[
\sum_{i=1}^{N^-} a_i^- (t_i^- - t_i) = \theta^- + \beta T_{in} - t_i^- - \nu
\]

where \( \theta^+ (> 0), \theta^- (< 0), and t\) indicate the threshold values and output timing for the positively and negatively weighted-sum operation, respectively. Then we obtain

\[
\sum_{i=1}^{N^+} a_i^+ \cdot x_i = \frac{\theta^+ + \beta T_{in} - t_i^+}{T_{in}}
\]

\[
\sum_{i=1}^{N^-} a_i^- \cdot x_i = \frac{\theta^- + \beta T_{in} - t_i^-}{T_{in}}
\]

Therefore, we can obtain the original weighted-sum result:

\[
\sum_{i=1}^{N} a_i \cdot x_i = \frac{\sum_{i=1}^{N^+} a_i^+ \cdot x_i + \sum_{i=1}^{N^-} a_i^- \cdot x_i}{T_{in}}
\]

\[
= \frac{\theta^+ + \theta^- + \beta T_{in} - (\beta t_i^+ + \beta t_i^-)}{T_{in}}
\]

Let us define a dummy weight \( a_0 \) as the difference between both absolute values of \( \beta \):

\[
a_0 = -(\beta^+ + \beta^-).
\]

If \( \beta^+ \geq -\beta^- \), then \( a_0 \leq 0 \) and this dummy weight is incorporated into the negative weight group, and vice versa. This dummy weight is related to a zero input, \( x_0 = 0 \), which means \( t_0 = T_{in} \). By using the dummy weight, we can make the absolute values of \( \beta \) identical (\( \beta = 0 \), and we define

\[
\beta_o = \beta^+ = -\beta^-.
\]
Fig. 2. Neuron model: (a) typical neuron model; (b) neuron model for time-domain weighted-sum operation with a dummy weight, \( w_{n+1} \); (c) neuron model for time-domain weighted-sum operation in which each synapse has two sets of inputs and weights. One is \((x_i, w_i)\) and the other is \((0, -w_i)\) or \((t_i, w_i)\) and \((T_{in}, -w_i)\) according to Eq. (2).

Also, according to Eqs. (12) and (13), the absolute values of \( \theta^+ \) and \( \theta^- \) can be the same, and \( \theta^+ + \theta^- = 0 \). Therefore, Eq. (27) can be rewritten as

\[
\sum_{i=1}^{N} a_i \cdot x_i = \beta (t^- - t^+) \frac{T_{in}}{T_{in}}. \tag{30}
\]

3 Spiking Neural Network model

3.1 Neuron Model

The typical neuron model of artificial neural networks is shown in Fig. 2(a), which has \( N \) inputs \( x_i \) with weights \( w_i \) and a bias \( b \):

\[
y = f \left( \sum_{i=1}^{N} w_i \cdot x_i + b \right), \tag{31}
\]

where \( y \) is the output of the neuron, and \( f \) is an activation function. We can consider the bias as a weight whose input is always unity. Therefore, our time-domain weighted-sum calculation model with the dummy weight can be applied to this neuron model, as shown in Fig. 2(b). According to Eq. (30),

\[
\sum_{i=1}^{N} w_i \cdot x_i + b = \beta (t^- - t^+) \frac{T_{in}}{T_{in}}. \tag{32}
\]
Based on Eq. (32), we propose another model, shown in Fig. 2(c), in which each synapse has two sets of inputs and weights; one is \((x_i, w_i)\) and the other is \((0, -w_i)\). In this model, it is not necessary to add a dummy weight because the summation of positive weights is \(\beta = \sum_{i=0}^{N} |w_i|\) and that of negative ones is \(\beta = -\sum_{i=0}^{N} |w_i|\), which means that the absolute values of both summations are equal.

As the activation function \(f\), we often use the rectified linear unit called “ReLU” [6,8], which is defined as follows:

\[
    f(x) = \text{ReLU}(x) = \begin{cases} 
        x & \text{if } x \geq 0, \\
        0 & \text{otherwise}.
    \end{cases} \tag{33}
\]

We can implement the ReLU function by comparing the output timings \(t_{(n)}^{(n)} - t_{(n)+}^{(n)}\) and \(t_{(n)}^{(n)+} - t_{(n)}^{(n)-}\) in the time-domain weighted-sum calculation. If \(t_{(n)}^{(n)-} \geq t_{(n)}^{(n)+}\), the difference between two timing values is regarded as the output transferred to neurons in the next layer. On the other hand, if \(t_{(n)}^{(n)-} < t_{(n)}^{(n)+}\), the output is

\[
\]
3.2 Neural Network Model

In this section, we show an application of our time-domain weighted-sum model to the MLPs shown in Fig. 3 as an example that has one hidden layer and two sets of input and weight for each neuron. In this application, after we calculate a weighted sum using Eq. (32), the result is given to the activation function \( f \), and the output is fed into the next layer.

According to Eq. (32), the weighted-sum result of the \( j \)-th neuron in the layer labeled \( n \) in Fig. 3 can be

\[
\sum_{i=0}^{N} w_{ij}^{(n)} \cdot x_i = \frac{\beta_j^{(n)}}{T_{in}} (t_{v_j}^{(n)} - t_{v_j}^{(n)+}).
\]  

(34)

where \( w_{0j}^{(n)} \) is the bias of the \( j \)-th neuron in the \( n \)-th layer. The output of the \( k \)-th neuron in the layer labeled \( p(=n+1) \) in Fig. 3 is

\[
\sum_{j=1}^{N} w_{jk}^{(p)} \cdot f(\sum_{i=0}^{N} w_{ij}^{(n)} \cdot x_i) + b_k^{(p)} = \sum_{j=1}^{N} w_{jk}^{(p)} \cdot f\left(\frac{\beta_j^{(n)}}{T_{in}} (t_{v_j}^{(n)} - t_{v_j}^{(n)+})\right) + b_k^{(p)}. 
\]

(35)

Here, substituting the activation function with ReLU, we can obtain

\[
ReLU\left(\frac{\beta_j^{(n)}}{T_{in}} (t_{v_j}^{(n)} - t_{v_j}^{(n)+})\right) = \frac{\beta_j^{(n)}}{T_{in}} (t_{v_j}^{(n)} - t_{v_j}^{(n)+}),
\]

(36)

where if \( t_{v_j}^{(n)} < t_{v_j}^{(n)+} \), then let \( t_{v_j}^{(n)} = t_{v_j}^{(n)+} \). Thus, Eq. (35) can be rewritten as

\[
\sum_{j=1}^{N} w_{jk}^{(p)} \cdot \text{ReLU}\left(\sum_{i=0}^{N} w_{ij}^{(n)} \cdot x_i\right) + b_k^{(p)} = \sum_{j=1}^{N} w_{jk}^{(p)} \frac{\beta_j^{(n)}}{T_{in}} (t_{v_j}^{(n)} - t_{v_j}^{(n)+}) + b_k^{(p)}. 
\]

(37)

In the MLP shown in Fig. 3 we transfer the output timings \( t_{v_j}^{(n)+} \) and \( t_{v_j}^{(n)} \) generated in layer \( n \) to neurons in layer \( p \) and perform the time-domain weighted-sum operation. In layer \( n \), we assume that timing \( t_{v_j}^{(n)+} \) is related to weight \( w_{jk}^{(p)} \) and \( t_{v_j}^{(n)} \) is related to \( -w_{jk}^{(p)} \). We also assume here \( j = 3 \), and that \( w_{1k}^{(p)} \geq 0, w_{2k}^{(p)} \leq 0, b_k^{(p)} \geq 0, \) and \( \theta_k^{(p)+} = -\theta_k^{(p)-} \), where \( \theta_k^{(p)+} \) and \( \theta_k^{(p)-} \) are the threshold values for positively and negatively weighted-sum operations, respectively. Thus, according to Eq. (34), we can obtain

\[
\begin{align*}
(w_{1k}^{(p)} t_{v_k}^{(p)+} - t_{v_1}^{(n)+}) + (w_{2k}^{(p)} t_{v_k}^{(p)+} - t_{v_2}^{(n)+}) + (w_{3k}^{(p)} t_{v_k}^{(p)+} - t_{v_3}^{(n)+}) + b_k^{(p)} (t_{v_k}^{(p)+} - t_{v_0}^{(n)+}) = \theta_k^{(p)+} \\
(w_{1k}^{(p)} t_{v_k}^{(p)-} - t_{v_1}^{(n)+}) + (w_{2k}^{(p)} t_{v_k}^{(p)-} - t_{v_2}^{(n)+}) + (w_{3k}^{(p)} t_{v_k}^{(p)-} - t_{v_3}^{(n)+}) + b_k^{(p)} (t_{v_k}^{(p)-} - t_{v_0}^{(n)+}) = \theta_k^{(p)-}
\end{align*}
\]

(38)
By adding Eq. (38) to Eq. (39), the following relationship is obtained:

\[ w_{1k}^{(p)} (t_{vk}^{(p)} - t_{v1}^{(n)}) + (-w_{1k}^{(p)}) (t_{vk}^{(p)} - t_{v0}^{(n)}) + w_{2k}^{(p)} (t_{vk}^{(p)} - t_{v2}^{(n)}) + (-w_{2k}^{(p)}) (t_{vk}^{(p)} - t_{v3}^{(n)}) + k_k^{(p)} (t_{vk}^{(p)} - t_{v0}^{(n)}) + (-b_k^{(p)}) (t_{vk}^{(p)} - t_{v0}^{(n)}) = t_{vk}^{(p)} - t_{v0}^{(n)} \]

where \( w_{0k}^{(p)} = b_k^{(p)} \). Thus, we can obtain the following simple expression:

\[ w_{jk}^{(p)} (t_{vk}^{(p)} - t_{vj}^{(n)}) + \sum_{j=0}^{N-3} w_{jk}^{(p)} (t_{vj}^{(n)} - t_{v0}^{(n)}) = 0, \quad k = 0, 1, \ldots, N-3 \]

Therefore, we can have the more general expression as follows:

\[ \sum_{j=0}^{N} w_{jk}^{(p)} (t_{vk}^{(p)} - t_{vj}^{(n)}) = (t_{vk}^{(p)} - t_{v0}^{(n)}) \cdot \sum_{j=0}^{N} w_{jk}^{(p)}. \]

Then, we can obtain the following formula:

\[ \sum_{j=0}^{N} w_{jk}^{(p)} \cdot \frac{\beta_j^{(n)}}{T_{in}} \cdot (t_{vj}^{(n)} - t_{vj}^{(n)+}) = (t_{vk}^{(p)} - t_{v0}^{(n)}) \cdot \sum_{j=0}^{N} w_{jk}^{(p)} \cdot \frac{\beta_j^{(n)}}{T_{in}} \]

where \( w_{0k}^{(p)} = b_k^{(p)} \), \( t_{v0}^{(n)} = T_{in} \), and \( t_{v0}^{(n)+} = 0 \). Because there is no input to the bias \( b_k^{(p)} \), we let \( \beta_0^{(n)} = 1 \). Therefore, Eq. (41) becomes

\[ \sum_{j=1}^{N} w_{jk}^{(p)} \cdot \frac{\beta_j^{(n)}}{T_{in}} \cdot (t_{vj}^{(n)} - t_{vj}^{(n)+}) = b_k^{(p)} = \beta_0^{(n)} w_{0k}^{(p)} \cdot \frac{\beta_0^{(n)}}{T_{in}} \]

where \( \beta_0^{(n)} = 1 \) on the right side. Therefore, Eq. (43) can be modified as

\[ \sum_{j=1}^{N} w_{jk}^{(p)} \cdot ReLU \left( \sum_{i=0}^{N} w_{ij}^{(n)} \cdot x_i \right) + b_k^{(p)} = (t_{vk}^{(p)} - t_{v0}^{(n)}) \cdot \sum_{j=0}^{N} w_{jk}^{(p)} \cdot \frac{\beta_j^{(n)}}{T_{in}} \]
As a result, for neurons in the hidden layer $n$, we apply the time-domain weighted-sum operation to generate the timing $t_{vj}^{(n)+}$ and $t_{vj}^{(n)-}$ for the positively and negatively weighted-sum calculation from the input layer, respectively. Then, these timings are directly transferred to neurons in the next layer $p$, and timing $t_{vj}^{(p)+}$ and $t_{vj}^{(p)-}$ are obtained. Finally, we calculate the final outputs of the MLP using Eq. (46). Note that intermediate weighted-sum results with different-signed weights are not calculated in the middle layers.

For CNNs, weighted-sum calculations of convolutions can be performed in the same way. In addition to the convolutions, max pooling operations can also be implemented simply by considering the difference between positive and negative timing values, as follows:

$$y_{\text{maxpooling}} = (t_{vk}^{(l)-}, t_{vk}^{(l)+}),$$

where

$$k = \arg \max_i (t_{v1}^{(l)-} - t_{v1}^{(l)+}, \cdots, t_{vi}^{(l)-} - t_{vi}^{(l)+}).$$

### 3.3 Numerical Simulations of Neural Networks

We performed numerical simulations to verify our weighted-sum calculation model. First, in order to verify our model for weighted-sum calculation with different-signed weights, we conducted a simulation to perform a weighted-sum calculation with 501 pairs of inputs and weights that consisted of 249 positive and 252 negative weights. We added a dummy weight to make the sum of positive weights equal to the absolute sum of the negative ones. Figure 4 shows the simulation results of time-domain weighted-sum calculation with a dummy weight $w_{n+1}$. The results show that the weighted-summation can be calculated correctly with different negative and positive firing timing inputs each set of which are multiplied by the corresponding signed weights.

Then, we applied our model to a four-layer MLP (784-100-100-10) and a CNN known as LeNet5 [15] to classify the MNIST digit character set. We trained these two ANNs, and then performed inference according to Eq. (46) with the obtained weights, which were either binary [3] or analog values. As described above, output spike timing at each neuron in the previous layer was directly conveyed to the neurons in the next layer without obtaining the subtraction of the signed weighted-sum results. We founded that we obtained the same weighted-sum calculation results in the last layer, and also the same recognition precisions in both NNs as in the numerically calculated ones.

### 4 Circuits and Architectures for TACT-based Neural Networks

As an implementation for our weighted-sum calculation based on our TACT approach, we have proposed an RC circuit in which a capacitor is connected
Fig. 4. Simulation results for the time-domain weighted-sum calculation model: (a) PSP of positively weighted-sum operation with 249 inputs in which $T_{in} = 1$, $\lambda = 1$, $\beta^+ = 24.01$, and $\theta^+ = 26.41$. The output spike timing is $t^+_o = 1.7256$. (b) PSP of negatively weighted-sum operation with 253 inputs in which $w_0 = -0.06$, $w_{n+1} = -2.819$, $T_{in} = 1$, $\lambda = 1$, $\beta^- = -24.01$, and $\theta^- = -26.41$. The output spike timing is $t^-_o = 1.9221$. Thus, the result of weighted-sum calculation is $|\beta^\pm| (t^\pm - t^\mp) / T_{in} = 4.718$.

by plural resistors, as shown in Fig. 5(a). Theoretical estimations have indicated that this circuit can perform weighted-sum calculations with extremely low energy consumption [31,32]. In CMOS VLSI implementation, resistance $R$ can be replaced by a p-type MOS field-effect transistor (pMOSFET), as shown in Fig. 5(b). The approximately linear slope $k$ is generated by capacitance $C$ and ON resistance of a pMOSFET with a step voltage input $V_{in}$, where we use step voltages instead of spike pulses as inputs. Each resistance should have a rectification function to prevent an inverse current.

The rectification function is automatically realized by the FET operation as follows. When a pMOSFET receives a step-voltage input, the terminal voltage of the input is higher than that at $C$, and therefore the input-side terminal of the pMOSFET is “source”, and the capacitor-side terminal is “drain.” In this state, if the gate-source voltage of the pMOSFET is set to exceed its threshold voltage, the pMOSFET turns on, and $C$ is charged up. On the other hand, when
a pMOSFET receives no input, the terminal voltage of the input is lower than that at \( C \), and therefore the source-drain position in the pMOSFET is reversed; i.e., the input-side terminal of the pMOSFET is “drain”, and the capacitor-side terminal is “source.” In this state, if the gate-source voltage of the pMOSFET is set not to exceed its threshold voltage, the pMOSFET turns off, and charges stored at \( C \) does not flow back to the input side.

In order to evaluate the energy consumption of this circuit, we designed a CMOS circuit equivalent to the RC circuit. It is obviously difficult to change the ON resistance of each pMOSFET independently, because different analog voltages have to be given as the gate voltages of the pMOSFETs. Therefore, in the PoC circuit, all MOSFETs have the same ON resistance with the same gate voltage. To realize different analog weights, it is necessary to use analog memory devices such as resistance-change memory \([27,12]\), ferroelectric-gate FETs \([17]\), and floating-gate flash memory \([1]\).

We designed a crossbar synapse circuit array to perform the weighted-sum calculation shown in Fig. 1 with a one-layer MLP model, as shown in Fig. 6. In the array, the horizontal and vertical lines are referred to as “axons” of the previous neurons and “dendrites” of the post neurons, respectively; each axon line has \( M \) synapse circuits, and each dendrite line receives \( N \) synapse outputs. An input voltage charges up the parasitic capacitance of the axon line, \( C_{al} \), and then charges up the capacitance, which includes the parasitic capacitance of the dendrite lines, \( C_{dl} \), and the input capacitance of the post neuron, \( C_i \), via synapse blocks, each of which consists of a pMOSFET.
We designed two single-layer neural network circuits, which have 500 inputs and 20 outputs \((N = 500, M = 20)\), and 500 inputs and 100 outputs \((N = 500, M = 100)\), respectively. The layout result and post layout simulation results are shown in Fig. 7. The fabrication technology of TSMC 250-nm were used, and both the gate length and width of pMOSFETs were 0.6 \(\mu\)m. The simulation results show a correct weighted-sum operation, where \(T_{in} = 1\ \mu\)s, and \(\theta = 0\) V. 3 V.

We extracted the parasitic capacitance of the dendrite and axon lines per synapse, \(c_{dl} = C_{dl}/N\) and \(c_{al} = C_{al}/M\), which were 1.76 fF and 1.78 fF, respectively. It is assumed that the input capacitance of pMOSFETs is included in this capacitance. Therefore, the energy consumption of line charge/discharge operation per synapse, \(E_{syn}\), is expressed by \(E_{syn} = (c_{dl} + c_{al})V_{dd}^2\), and it was 3.54 fJ, where \(V_{dd} = 1 \) V. We note that the above estimation does not include the energy consumption related to charging/discharging of the input capacitance \(C_i\) of post-neuron circuits; this, however, would be negligible compared to the dendrite line capacitance under 250-nm technology.

As for the neuron part, which consists of a comparator and the output buffer, the energy consumption was about 1.67 pJ, which means 3.34 fJ per synapse operation. As a result, overall energy consumption was 6.88 fJ per synapse operation, which consists of two operations, multiply and accumulate. This implies that the energy efficiency is 290 TOPS/W (Tera-Operations Per Second per
This efficiency is more than one order of magnitude higher than that of state-of-the-art digital AI processors [11].

For sufficient calculation precision, we expect the time constant of RC circuits to be much more than 1 µs to guarantee a time resolution of 7 bits, assuming a resolved time step of 10 ns. To obtain this time constant, $R$ should be more than 1 GΩ, which means that the current flowing through each resistance is less than 1 nA. Such high resistance can be achieved by using the subthreshold operation of MOSFET, and we set all the gate-source voltages of the pMOSFETs at -0.37V.

We propose the circuit architecture of a neural network suitable for our TACT approach, in which the weights may be both positive and negative as described above. The architecture is shown in Fig. 8 and is composed of synapses acting as resistive elements, the neuron part functioning as thresholding, the ReLU part denoting the activation, and the configuration part controlling synapses.

There are two inputs for each synapse circuit, which are $t_i$ as signal input and $T_{in}$ as a dummy input in the first layer, and $t_{i+}^+$ and $t_{i-}^+$ at the subsequent layers. Pairs of positive and negative timing are directly connected to the next layer without calculating subtraction between positively and negatively signed weighted results. The synapse part is designed with two resistive elements and two pairs of switches. A set of two identical resistances represents the weight value. We can assume that the upper-side axon is for $t_{i+}^+$ and the other is for $t_{i-}^+$, and the left-side dendrite is for a positive weight connection while the other is for a negative one. The two switches are exclusively controlled according the corresponding sign of weights, which is controlled by the weight control circuit.

The neuron part includes a comparator. The ReLU activation function can easily be implemented by logic gates, as shown in Fig. 9. When $t_{i+}^+ > t_{i-}^+$, we set both timing at $t_{i+}^+$ as shown in Fig. 9. With such circuits, the output spike timings at each neuron in the previous layer are directly transferred into the neurons in the next layer, while the nonlinear activation function ReLU can be implemented with low energy consumption operation.

5 Conclusions

In this paper, we proposed a time-domain weighted-sum calculation model based on the spiking neuron model, and formulated the calculation model to implement MLPs with an activation function of ReLU. In the proposed model, weighted-sum results with different-signed weights are not calculated in intermediate layers. We also proposed VLSI circuits based on the TACT approach to implement the calculation model with extremely low energy consumption. We demonstrated the high energy efficiency of the circuit using 250-nm CMOS VLSI technology. If we use a more advanced VLSI fabrication technology, able to achieve lower parasitic capacitance, the energy efficiency will be much improved over 1 POPS/W (Peta-operations Per Second per Watt).

However, there are some issues to be overcome toward developing practical AI processors using our TACT approach. In terms of synapse circuits, the designed
PoC CMOS VLSI chip provided no memory function. In order to construct neural network systems, it is necessary to introduce analog memory devices with high resistance in synapse circuits. As for the neuron parts, the results of post-layout simulations suggest that the energy consumption of this part is comparable to that of the whole synapse part with 500 inputs. It will be necessary to design a comparator with much lower power consumption to improve the energy efficiency of the whole weighted-sum calculation circuit.

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Fig. 9. ReLU circuit.

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