Research on high robustness 4.5kV FRD chip

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Abstract. A robustness 4500V/100A FRD with was designed by simulation and verified by experiment. The chip composed with optimized carrier density cell area and ruggedness terminal area. The cell area composed of P-body/N-sub/N+ layers, has good static and dynamic trade off characteristics by carefully design. The simulation show that there was no difference between conventional multi-deep P-ring terminal and multi-deep P-ring plus inner field plate terminal. Both terminals have the same width and almost the same breakdown voltage, low electric field and etc.by simulation. The experiment show that different terminal chips have almost the same trade off characters but different in reliability test, the inner field plate terminal pass 1000H HTRB test while the conventional multi-deep P-ring terminal failed at 168H HTRB test.

1. Introduction
Fast Recovery Diodes (FRD) is usually used as free-wheeling diode in anti-parallel to the IGBTs, which is an effective solution for easier controlled in the field of power systems. The FRD is usually used in a high-voltage, high-frequency environment. This puts higher requirements on the diode. The diode need to have faster reverse recovery time, lower leakage current and softer reverse recovery characteristics, good surge-current capability and high reliability.

During the past two decades, a lot of studies have been done in the field of FRDs. It has been demonstrated that several concepts (such as CIBH, FCE) offer a significantly improved on-state, reverse recovery and softness characteristics [1-6]. However, it is difficult to optimize the reliability. In this paper, FRD with different terminal structures were proposed. After using the inner field plate terminal structure, the FRD chip has low conduction loss, soft reverse recovery, large safe operation area and also high robustness and reliability.

2. Structure Design
The 4.5kV/100A diode cell structure diagram are shown in Fig.1. It is composed of P-body/N-sub/N+ layers, the P-body contact with the anode electrode, and the N+ contact with the cathode electrode.

The three layer thickness/doping concentration/profile need careful consideration to get low loss, high ruggedness and good surge-current capability. The N-sub doping concentration is about 1E13/cm3, 430ohm.cm, and the thickness is 500μm. The optimized P-body peak concentration is 2E17/cm3 and the depth is about 10μm. The N+ peak concentration is near 1E20/cm3 and the depth is about 40μm.
The 4.5kV/100A diode terminal structure diagrams are shown in Fig.2 and Fig.3. Fig.2 was the conventional multi-deep P-ring terminal. Fig.3 was the multi-deep P-ring with inner field plate terminal. The inner field plate was located in the ring and does not occupy the terminal area. The inner field plate was different with the conventional field plate, the conventional field plate extend outside the p-ring and occupy the terminal area. The total dimension of both terminals were the same and less than 2.3mm.

3. Result and discussion

3.1 Simulation Results

Fig.4 shows the breakdown voltage of the terminal with and without inner field plate. There was no significant difference between the of two terminal breakdown voltages. The breakdown voltage was above 6000V.
Figure 4. The breakdown voltage of different terminals.

Fig. 5-Fig. 7 show the electric field of both terminals at breakdown voltage, the peak electric field is located in the curve of ring rather than silicon-oxide interface. The electric field profile is insensitive to mobile charge and result in ruggedness and high reliability.

Figure 5. The simulated electric field profile of terminal without inner plate.

Figure 6. The simulated electric field profile of terminal with inner plate.

Figure 7. The simulated electric field of different terminals (cut-line of junction curve).

Fig. 8 shows the depletion profile at breakdown voltage, the depletion boundary of both terminals were far away from last stop ring. The large margin of depletion boundary result in ruggedness and high reliability.
3.2 Experiment Results

The 4500V/100A FRD chips were fabricated base on the simulation. The chips have the same cell areas with the different terminals. Chip1 terminal was only composed of multi-deep P-ring , but chip2 terminal was composed of multi-deep P-ring plus inner field plate.

The static and dynamic characteristics test result show no significant difference. The test details are shown in Table 1 and Table 2.

The static and dynamic characteristics was mainly depend on the cell area, and the cell area of The two chips was not different.

| Characteristics | $V_f/V$ | $I_R/uA$ | $I_{le}/mA$ |
|-----------------|---------|----------|-------------|
| Bias            | 100A    | 4500V    |             |
| Temperature/℃   | 25      | 125      | 25          |
| Design chip1    | 2.25    | 2.55     | 3           |
| Design chip2    | 2.23    | 2.58     | 2           |

Table 2. Dynamic characteristics of design chip.

| Characteristics | $I_{RM}/A$ | $Q_{rr}/μC$ | $T_{rr}/μs$ | $E_{rec}/mJ$ |
|-----------------|------------|-------------|-------------|--------------|
| Bias $V_G=2800V, V_G=+/−15V$ |            |             |             |              |
| Temperature/℃   | 25         | 125         | 25          | 25           |
| Design chip1    | 180        | 200         | 60          | 0.52         |
| Design chip2    | 185        | 205         | 65          | 0.55         |

Figure 8. The simulated depletion profile of different terminals

The inner plate terminal and conventional terminal show almost the same performance, including the breakdown voltage, the electric field profile, the depletion boundary and etc.

Figure 9. Chip2 reverse recovery curve at small current.

(Conditions: $V_R=2.8kV$, $I_F=3A$, $R_g=330\,Ω$, $T_j=25\,℃$).
The chip1/2 also has soft reverse recovery behavior and a large safe operation area. Both chips turn off less than 1/10 and 2 times rated current successfully at home and high temperature.

Fig.9 shows design chip2 turn off curve of small current at home temperature.

Fig.10 shows design chip2 turn off curve of 2 times rated currents at high temperature.

![Figure 10. Chip2 reverse recovery curve at 2 times rated currents.](Conditions: VR=2.8kV, IF=200A, Rg=330Ω, Tj=125℃).

The design chip1/2 also do 168H HTRB(high temperature reverse bias) test, the chips show difference performances. Chip1 show large leakage after the test, and chip2 pass the test. The test details are shown in Table3, the test temperature was 25℃.Chip2 was more ruggedness and has high reliability.

| Characteristics/Chip | Design chip1 | Design chip2 |
|----------------------|-------------|--------------|
| Before HTRB          |             |              |
| $V_f/\text{V} @100A$ | 2.264       | 2.252        |
| $I_{\text{leak}}/\mu\text{A} @4500\text{V}$ | 4           | 3            |
| After HTRB           |             |              |
| $V_f/\text{V} @100A$ | 2.268       | 2.256        |
| $I_{\text{leak}}/\mu\text{A} @4500\text{V}$ | 9000        | 9980         |

Chip2 also pass 1000H HTRB test, the leakage was about 5uA after 1000H HTRB test.

Fig.11 shows the inline leakage curves of 16 chip2 samples at 1000H HTRB test, the inline leakage was less than 2mA at the stable period, the test condition was VR=3600V, Tj=125℃.

![Figure 11. The inline leakage curve during HTRB test of chip2.](Conditions: VR=3600V, Tj=125℃).

4. Conclusion

This paper introduces the 4500V100A FRD chip design with different terminals. Multi-deep P-ring structure terminal with and without inner field plate were compared using simulation and verified by
experiment. The different terminals have the same width and show almost the same performance by simulation. Chip1 and chip2 with the same cell area but the different terminals were fabricated, chip1 terminal was only composed of multi-deep P-ring, but chip2 terminal was composed of multi-deep P-ring plus inner field plate. The test results show that the different chips have the same static, dynamic characteristics, and both have large safe operation area. But show difference result in reliability test, the chip2 pass 1000H HTRB test while the chip1 without field plate failed the test. The terminal with inner field plate terminal show more robustness and high reliability.

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