A Direct Mapped Method for Accurate Modeling and Real-Time Simulation of High Switching Frequency Resonant Converters

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Abstract—This paper presents a Direct Mapped Method (DMM) for real-time simulation of high switching frequency resonant converters. The DMM links state variables to diode statuses and provides an exact and noniterative solution to network equations. The proposed method is implemented on FPGA to simulate an LLC converter with switching frequencies ranging up to 500 kHz. The best reported implementations of DMM achieve a 25 ns simulation time-step for a wide range of clock frequencies, ranging from 40 MHz to 320 MHz.

Index Terms—Real-time simulation, FPGA, high switching frequency converters, resonant converters, power electronic converter modeling.

I. INTRODUCTION

Advances in semiconductor technology allow the increase of the efficiency and power density of modern power electronic converters (PECs) by operating them at higher switching frequencies (>50 kHz). Resonant converters are particularly of interest and renowned for their higher power density with typically small L/C components [1], [2]. These converters are typically operated using soft switching techniques to preclude switching losses, reduce filtering requirements, and to mitigate electromagnetic interference (EMI) [3], [4]. Among various resonant topologies [5], the LLC converter has drawn attention for its unique characteristics such as low voltage stress on the secondary rectifier and high efficiency at high input voltages [6], [7].

These technology advancements are however very challenging for the realm of FPGA-based Hardware-In-the-Loop (HIL) real-time simulation (RTS). HIL simulation is a prototyping technique used to assess the performance of control/protection systems in the design or installation stages. FPGAs are programmable devices that have played a pivotal role during the last decade in the RTS of PECs for HIL applications [8]–[10]. The main challenges faced by the FPGA-based HIL of high switching frequency (HSF) converters come from the limited memory resources and the heavy processing requirements given the small calculation time-step.

Two main modeling approaches are typically employed in FPGA-based RTS to model switching devices: i) The Associate Discrete Circuit (ADC); and ii) The Resistive Switch Model (RSM). The ADC switch model was introduced in the 90s [11] and has been since extensively utilized for RTS applications, provided that the simulation time-step $(\Delta t)$ is sufficiently small [8]–[10]. However, ADC is prone to fictitious oscillations that can alter the behavior of a PEC model in particular when dealing with HSF. Various techniques exist to alleviate these drawbacks [12]–[15], but are unpractical for resonant converters because the adopted switch model affects the resonant tank behaviour. The RSM on the other hand uses a two-valued resistance for the switch $(R_{on} \approx 0$ and $R_{off} \gg 0$) [16]–[20]. RSM produces more accurate results compared to ADC when modeling PECs, but has the drawbacks of a variable admittance matrix and heavier computations in real-time.

To circumvent the heavy computational burden of RSM, the inverse of the nodal matrix for all possible switch combinations can be precomputed. This approach, however, considerably limits the number of switches due to FPGA memory requirement limitations. The Sherman-Morrison-Woodbury formula has been utilized to compute the updated inverse matrix on the fly [18], but the method is unpractical for HSF PECs, and neglects the iterations needed to determine the state of natural commutation devices such as diodes. Methods for handling the RTS of diodes can be found in [16], [17], [19], [20]. In [16], unrealistic parasitic elements are augmented in parallel with switches that may alter the behavior of the converter, more so when resonant converters are considered. The method proposed in [17] results in large time-steps and as such is inadequate for the simulation of HSF PECs. A predictor-corrector algorithm has been used in [19] to decouple the switches from the circuit elements and to simulate them simultaneously. However, due to the stability concerns, very short time-steps should be selected which results in increased hardware resources when dealing with large circuits. More recently, the RSM has been used to simulate low-frequency PECs [20]. This method, however, uses an iterative solver to deal with switches, which makes it unpractical for the simulation of HSF PECs.
The RTS of HSF converters is more challenging since it requires very small time-steps which can be restrictive for the iterative solver. To obviate the iterative procedure while adopting the RSM, some specific simplifications are often made for the determination of switch states. In [21], a commercial RTS method has been used to simulate an LLC, with the switching frequency of 20 kHz which is relatively low. The simulation of an LLC converter with a switching frequency of 60 kHz has been presented in [22], where the LLC model is built by breaking down the converter into interconnected modules. This approach relies on intra-module delays which can cause erroneous results. In [23], an LLC converter with a resonance frequency of 160 kHz has been simulated using FPGA. The simulations have been done by making use of Forward Euler (FE) method where a time-step of 15 ns has been achieved. The FE is not however a generic approach and might not work for certain LLC parameters. This will be discussed for the first time in this paper.

This paper proposes a Direct Mapped Method (DMM) for accurate RSM-based simulation of HSF resonant converters. The method offers higher computational performance while providing the same level of accuracy compared to iterative solutions. The DMM proceeds by constructing a mapping function that relates the state variables of the circuit to switch states. The mapping function is then used to directly determine switch states during the simulation. In this paper, the DMM is used to implement an FPGA-based LLC simulator with parameters taken from the literature. It is demonstrated that the method is successful in the accurate simulation of LLC converters with switching frequencies ranging up to 500 kHz.

The remainder of this paper is organized as follows. The theoretical background of resonant and LLC converters are briefly presented in Section II. In Section III, the DMM is elaborately presented while its application for an LLC converter is discussed. Section IV presents the FPGA implementation of the DMM and discusses experimental results.

II. DC-DC RESONANT CONVERTER

A typical DC-DC resonant converter is comprised of three stages: an inverter, a 2- or 3-element resonant tank, and a rectifier. The inverter consists of a MOSFET half-bridge or full-bridge, operated with a fixed 50% duty cycle. The power flow of the converter is controlled by modulating the frequency of the square wave with respect to the tank’s resonant frequency. The rectifier stage converts its AC input to a DC output voltage which is filtered by a capacitor. A transformer is often used in the rectification stage for scaling and isolation purposes.

The resonant tank modulates the voltage using L-C elements such as series LC, parallel LC, LLC, etc. These resonant tanks are selected depending on the converter application [24]. In this work, we will focus on the LLC converter topology which is comprised of a full-bridge inverter and a full-bridge rectifier, see Fig. 1. The LLC converter is used in many applications such as power electronic-based distributed generation, electric vehicles, computer and communication systems [25]–[28]. The proposed DMM is, however, applicable to other resonant topologies as well.

A. Overview of the LLC Resonant Converter

The LLC converter is a multi-resonant converter with resonant frequencies \( f_r = f_{r1} = 1/(2\pi \sqrt{L_r C_r}) \) and \( f_{r2} = 1/(2\pi \sqrt{(L_r + L_m) C_r}) \). With reference to Fig. 1, \( L_m \) is embodied in the magnetizing inductance of the transformer which helps to reduce the size and the cost of the the converter [26]. LLC resonant tank gain, \( G(F) \), is defined as the magnitude of its input/output voltage transfer function. Typical voltage gains of the LLC tank for different normalized switching frequencies \( F = f_s/f_r, (f_s \text{ being the switching frequency}) \) are obtained from [29]:

\[
G(F) = \frac{(m - 1) F^2}{\sqrt{(m F^2 - 1)^2 + (m - 1)^2 F^2 (F^2 - 1)^2 Q^2}}, \tag{1}
\]

where \( Q \) is the quality factor, and \( m \) is the inductance ratio:

\[
Q = \left( \sqrt{L_r/C_r} \right)/R_{ac} \\
m = \left( L_r + L_m \right)/L_r \\
R_{ac} = 8n^2/\pi^2 R_L.
\tag{2}
\]

\( R_{ac} \) denotes the reflected load resistance \( R_L \), seen from the resonant tank side, and \( n \) is the turn ratio of the isolation transformer.

B. LLC Operation

Fig. 2 depicts the LLC voltage gain for different values of quality factor \( Q \), which are used for the analysis and design of the resonant converter. \( f_{r2} \) delimits the capacitive and the inductive regions of the resonant tank, which are associated
with the Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS) regions, respectively. The MOSFET-based LLC converters are preferably operated in the ZVS region, i.e., \( f_x > f_{r_2} \), since it significantly mitigates the switching losses [5]. When LLC is working with \( f_{r_2} < f_x < f_{r_1} \), at the end of one half resonant cycle, during a certain time interval no power is delivered to the load and the whole resonant current passes through the magnetizing inductance. During this time interval, the rectifier is said to be in blocking mode \( (i_{\text{rec}} = n_i - i_m) \approx 0 \). The region where \( f_x > f_{r_1} \) refers to an operational mode of the LLC where a resonant half cycle is not completed and interrupted by the switching of other MOSFET.

### C. LLC Simulation

In this paper, the LLC converter of Fig. 1 is considered for which two sets of parameters are chosen from the literature as listed in Table I. In this table, LLC with Parameter Set #1 [23] and Parameter Set #2 [30] has the resonant frequency of 160 kHz, 500 kHz, respectively. We will show in this section why an iterative solution is needed to accurately simulate the LLC converter.

As proposed in [19] and [23], an explicit integration method such as FE can be used to avoid the iterative process. This however necessitates adopting a sufficiently small simulation time-step. For the sake of clarity, let us recall that FE offers a recursive solution to \( x(t) = f(x(t)) \) in the following form:

\[
x(t) = x(t - \Delta t) + \Delta t f(x(t - \Delta t)).
\]

By applying Eq. (3) to the resonant inductors of the resonant tank of the LLC, an explicit expression for the rectifier’s input current is obtained (see Fig. 1):

\[
i_{\text{rec}}(t) = n_i(t) - i_m(t)
\]

\[
= n_i(t, t - \Delta t) + \frac{1}{n} v_L(t, t - \Delta t) - i_m(t, t - \Delta t) - \frac{\Delta t}{L_m} v_L(t, t - \Delta t).
\]

It is proposed in [23] to use Eq. (4) to determine the mode of the full-bridge rectifier; positive mode when \( i_{\text{rec}}(t) \geq 0 \), \( \{d_1, d_2, d_3, d_4\} = (1, 0, 0, 1) \), and negative mode otherwise — \( \{d_1, d_2, d_3, d_4\} = (0, 1, 1, 0) \). However, such an approach may lead to either inaccurate results or instability, even for very small time-steps. This behavior is partly due to the fact that this method completely ignores the blocking mode of the converter.

Fig. 3a gives the resonant current, \( i_r \), for LLC with Parameter Set #1 (see Table I), calculated by either making use of FE or backward Euler (BE) methods, and assuming a time-step of 15 ns. It is noted that BE method is applied completely ignores the blocking mode of the converter. The zoomed view of resonant current during the blocking mode is shown in Fig. 3b. It is seen from this figure that in contrast with BE method, the current \( i_r \) calculated by the method proposed in [23] is oscillatory during the blocking mode period. The blocking mode is in fact disregarded during the simulation i.e., only positive and negative modes are considered, and the model alternates between the two modes during the blocking period.

The effects of ignoring the blocking mode for LLC with Parameter Set #2 (see Table I) are observed in Fig. 4. Similar to the previous case, \( i_r \) is calculated by either BE or FE with the same 15 ns time-step. It is seen from Fig. 4 that \( i_r \) calculated by FE is oscillatory during the blocking mode. It is also seen from Fig. 4 that, as opposed to LLC with Parameter Set #1, the results of FE and BE are quite different for LLC.
with Parameter Set #2. This indicates that the accuracy of the method proposed in [23] can be affected by circuit parameters.

During our simulations, it was also observed that the resonant current calculated by FE method becomes unstable for ∆t ≥ 30 ns. It is also worth noting that another possible mode of the rectifier stage of the LLC circuit of Fig. 1 is the short circuit mode, i.e. (d₁, d₂, d₃, d₄) = (1, 1, 1, 1) which is also disregarded by explicit methods such as [19], [23].

III. DIRECT MAPPED METHOD

A. DMM Analysis of the LLC

Without losing any generality, we consider the circuit of Fig. 5, which represents the rectifying stage of the LLC. Both AC and DC side circuits are replaced by a Norton equivalent circuit comprised of a conductance in parallel with a time-dependent current source. The Norton equivalents result from the BE discretization.

The following systems of equations associate network equations of the circuit of Fig. 5 using a classical nodal analysis:

\[ \mathbf{Y}^{\sigma_{rec}} \mathbf{v}_n = \mathbf{i}, \]

\[ \mathbf{Y}^{\sigma_{rec}} = \begin{bmatrix} g_1 + g_d + g_d & -g_1 & -g_1 & -g_{d_1} \\ -g_1 & g_1 + g_d + g_d & -g_1 & -g_{d_2} \\ -g_1 & -g_1 & g_1 + g_d + g_d & -g_{d_3} \\ -g_{d_1} & -g_{d_2} & -g_{d_3} & g_2 + g_d + g_d \end{bmatrix}, \]

\[ \mathbf{i} = \begin{bmatrix} i^h_1 \\ -i^h_1 \\ i^h_2 \\ -i^h_2 \end{bmatrix}^T, \]

where \( \mathbf{Y}^{\sigma_{rec}} \) is the admittance matrix, \( \sigma_{rec} \in \{0, 1, ..., 15\} \) refers to the 16 diodes status combinations, \( \mathbf{v}_n = [v_1, v_2, v_3]^T \) is the unknown nodes voltage and \( \mathbf{i} \) is the current injection vector. \( g_{d_i} = 1/R_{d_i}, i \in \{1, 2, 3, 4\} \) are the conductances associated with the diodes \( (g_{d_1} = g_{on} \ or \ g_{off}) \) with respect to the diode status combination \( \sigma_{rec} \).

Eq. (5) can be rewritten as:

\[ \mathbf{Y}^{\sigma_{rec}} \mathbf{v}_n = \mathbf{B} \mathbf{i}^h, \]

\[ \mathbf{B} = \begin{bmatrix} +1 & 0 \\ -1 & 0 \\ 0 & +1 \end{bmatrix}, \]

\[ \mathbf{i}^h = \begin{bmatrix} i^h_1 \\ i^h_2 \end{bmatrix}^T, \]

In addition, diodes voltages can be defined using a connectivity matrix, \( \mathbf{T} \), as:

\[ \mathbf{v}_d = \mathbf{T} \mathbf{v}_n, \]

\[ \mathbf{T} = \begin{bmatrix} +1 & 0 & -1 \\ -1 & 0 & 0 \\ 0 & +1 & -1 \\ 0 & -1 & 0 \end{bmatrix}, \]

where \( \mathbf{v}_d \) is the vector of diode voltages: \( \mathbf{v}_d = [v_{d_1}, v_{d_2}, v_{d_3}, v_{d_4}]^T \). From (8) and (11), \( \mathbf{v}_d \) can be obtained as follows:

\[ \mathbf{v}_d = \mathbf{T} (\mathbf{Y}^{\sigma_{rec}})^{-1} \mathbf{B} \mathbf{i}^h. \]  

The RSM requires the correct state of each diode (ON/OFF) at each time-point. This is done by checking whether the sign of the diode’s voltage or its current \( (v_{d_i} = R_{d_i} i_{d_i}, R_{d_i} > 0) \) is positive or negative. However, from (13), one can find that diode \( d_i \) conducts whenever \( \vartheta_{d_i} > 0, i \in \{1, 2, 3, 4\} \):

\[ \vartheta_{d_1} = \begin{cases} + (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_1 \\ - (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_2 \end{cases}, \]

\[ \vartheta_{d_2} = \begin{cases} - (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_1 \\ + (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_2 \end{cases}, \]

\[ \vartheta_{d_3} = \begin{cases} - (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_1 \\ + (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_2 \end{cases}, \]

\[ \vartheta_{d_4} = \begin{cases} + (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_1 \\ - (g_{d_1} g_{d_3} + g_{d_3} g_{d_1} + g_{d_3} g_2 + g_{d_3} g_2) i^h_2 \end{cases}. \]

Hence, for each combination \( \sigma_{rec} \), a system of inequalities combining (14)-(17) is obtained, and the Fourier-Motzkin elimination [31] is used to evaluate its feasibility.

The feasibility check reveals that only 4 feasible diode combinations exist, those for which \( d_1 = d_4 \) and \( d_2 = d_3 \). A mapping function \( f(i^h_1, i^h_2) \) linking the state variables to diode states, \( (i^h_1, i^h_2) \rightarrow \sigma_{rec} \equiv (d_1, d_2, d_3, d_4) \), can be obtained. Fig. 6 demonstrates this mapping function in the \( i^h_1, i^h_2 \)-plane with four half lines dividing the plane into four feasible regions: \( (0, 0, 0, 0) \) = Blocked, \( (1, 0, 0, 1) \) = Positive, \( (0, 1, 1, 0) \) = Negative and \( (1, 1, 1, 1) \) = Shorted. The half
lines start at the origin and have slopes of \( \pm m_1 \) and \( \pm m_2 \), as illustrated in Fig. 6. The slopes \( m_1 \) and \( m_2 \) are given by:

\[
\begin{align*}
   m_1 &= \frac{g_{off}g_{off} + g_{off}g_{off} + g_{off}g_{2}}{g_{off}g_{off} + g_{off}g_{off} + g_{off}g_{2}}, \\
   m_2 &= \frac{g_{on}g_{on} + g_{on}g_{on} + g_{on}g_{2}}{g_{on}g_{on} + g_{on}g_{on} + g_{on}g_{2}}. 
\end{align*}
\]

Eqs. (18) and (19) reduce to:

\[
\begin{align*}
   m_1 &= \frac{g_{off} + g_{2}}{g_{off} + g_{1}}, \\
   m_2 &= \frac{g_{on} + g_{2}}{g_{on} + g_{1}}.
\end{align*}
\]

Assuming \( g_{off} \approx 0 \), slope \( m_1 \) is approximated by:

\[
m_1 \approx \frac{g_{2}}{g_{1}}.
\]

From (22), one can observe that the slope \( m_1 \) (which delimits the Blocked from the Positive and Negative states) is approximately independent of diode conductances and is a function of both AC and DC side parameters. It also appears from Eq. (22) that explicit solvers such as those used in [19], [23] — which substitute the Norton equivalent of the AC side by a pure current source \((g_1 = 0)\) — discard the Blocked mode of the rectifier because they force \( m_1 \) to infinity. Such an approximation is not problematic if the slope \( m_1 \) is very large such as for Parameter Set #1, but can considerably degrade the simulation results for other parameters, such as those of Parameter Set #2.

B. Simulation Algorithm

The aim of this section is to develop a simulation algorithm for the LLC converter of Fig. 1. The inverter is operated in controlled mode, and DMM is used to determine the diode states. Network equations for the LLC converter of Fig. 1 are formulated using the Modified Augmented Nodal Analysis (MANA) [32] after discretizing all elements using BE rule:

\[
A^\sigma x(t) = B \left[ u(t), i_{\text{in}(t)}, i_{\text{hat}(t)} \right]^T.
\]

where \( A^\sigma \) is the MANA matrix for switch combination \( \sigma \), \( B \) is the incidence matrix, \( x(t) \) is the vector of unknown variables. \( u(t) = v_{dc}(t) \) is the input DC voltage, \( i_{\text{in}(t)} \) and \( i_{\text{hat}(t)} \) are ac and dc side history vectors, respectively: \( x(t) \) is comprised of node voltages \((v_n(t))\), the current entering the DC voltage source \((i_{dc}(t))\) and the current entering the secondary port of the transformer \((i_{\text{DB}}(t) = -i_{\text{in}(t)})\):

\[
x(t) = [v_n(t), i_{dc}(t), i_{\text{DB}}(t)].
\]

The history vectors are comprised of history currents that result from the backward discretization of the L/C components in the circuits: \( i_{\text{in}(t)} = [i_{\text{in}(t)}, i_{\text{in}(t)}, i_{\text{in}(t)}] \), and \( i_{\text{hat}(t)} = [i_{\text{hat}(t)}, i_{\text{hat}(t)}, i_{\text{hat}(t)}] \). More on the use of MANA for the simulation of power electronic circuits can be found in [17], [33].

To reduce the computational burden of solving Eq. (23) at each time-point of the simulation, the following formulation is used:

\[
\begin{bmatrix}
   i_{\text{in}}(t + \Delta t) \\
   i_{\text{in}}(t + \Delta t) \\
   y(t)
\end{bmatrix}
 =
\begin{bmatrix}
   H_{\text{in},u}(t) & H_{\text{in},w}(t) & H_{\text{in},f}(t) \\
   H_{\text{in},u}(t) & H_{\text{in},w}(t) & H_{\text{in},f}(t) \\
   y_{\text{in}},u(t) & y_{\text{in}},w(t) & y_{\text{in}},f(t)
\end{bmatrix}
\begin{bmatrix}
   u(t) \\
   v_{\text{in}}(t) \\
   y_{\text{in}}(t)
\end{bmatrix},
\]

where \( H_{\text{in}}(t) \) are precomputed matrices obtained from simple algebraic manipulations of \( B \) and inverse of \( A^\sigma \). \( y(t) \) is a vector comprised of desired output variables, \( y(t) = [v_{\text{in}}(t), i_r(t), i_m(t)] \). Similar rewrites are used to determine the history currents associated with the Norton equivalents of the ac and dc sides:

\[
\begin{align*}
   i_{\text{in}}(t) &= H_{\text{in},u}(t) u(t) + H_{\text{in},w}(t) i_{\text{in}}(t), \\
   \sigma_{\text{in}}(t) &= H_{\text{in},f}(t) y_{\text{in}}(t).
\end{align*}
\]

where \( \sigma_{\text{in}}(t) \) is the switch combination associated with the inverter's state, which is defined as a function of the gating signal \( c(t) \) driving \( S_1 \) and \( S_2 \) (see Fig. 1), given the controlled operation of the inverter:

\[
\sigma_{\text{in}}(c(t)) = \begin{cases} 
   6, & \text{if } c(t) = 0 \\
   9, & \text{if } c(t) = 1.
\end{cases}
\]

The DMM function is used to determine \( \sigma_{\text{rec}} \) and \( \sigma \):

\[
\sigma_{\text{rec}}(t) = f(i_{\text{in}}(t), i_{\text{hat}}(t)), \sigma_{\text{rec}}(t) \in \{0, 6, 9, 15\},
\]

\[
\sigma(t) = 16 \cdot \sigma_{\text{in}}(c(t)) + \sigma_{\text{rec}}(t).
\]

DMM consists mainly in solving the following (see Fig. 6):

\[
\begin{bmatrix}
   p_1(t) \\
   p_2(t) \\
   p_3(t) \\
   p_4(t)
\end{bmatrix}
 =
\begin{bmatrix}
   -m_1 & 1 \\
   +m_1 & 1 \\
   -m_2 & 1 \\
   +m_2 & 1
\end{bmatrix}
\begin{bmatrix}
   i_{\text{in}}(t) \\
   i_{\text{hat}}(t)
\end{bmatrix},
\]

where \( \text{sgn}(\cdot) \) is the sign function. The DMM function reads henceforth as follows:

\[
\begin{align*}
   \{p_1(t), p_2(t)\} &= +(1, +1) \Rightarrow \sigma_{\text{rec}}(t) = 0, \\
   \{p_2(t), p_3(t)\} &= -(1, +1) \Rightarrow \sigma_{\text{rec}}(t) = 6, \\
   \{p_3(t), p_4(t)\} &= +(1, -1) \Rightarrow \sigma_{\text{rec}}(t) = 9, \\
   \{p_3(t), p_4(t)\} &= -(1, -1) \Rightarrow \sigma_{\text{rec}}(t) = 15.
\end{align*}
\]

From the mathematical formulation given above, the following algorithm is used at each time-point to simulate the LLC:

1) Determine \( \sigma_{\text{rec}}(t) \) using Eqs. (25), (29), and (30);
2) Determine \( \sigma(t) \) using Eqs. (26) and (28);
3) Compute the output vector \( y \) as well as the history vectors \( i_{\text{in}} \) and \( i_{\text{hat}} \) for the next time-point using Eq. (24).

This algorithm is referred to as the Two-Stage Algorithm because it involves two Matrix-Vector Multiplications (MVMs): Step 1) is performed by combining Eqs. (25), (29) into a single MVM following which Eq. (30) is used to determine \( \sigma_{\text{rec}} \). Step 2) is a simple binary word concatenation and is therefore instantaneous. Step 3) constitutes the second stage MVM of the algorithm.
hinders reaching to a small time-step. The only limitation of this approach is that two consecutive simulation steps are needed to produce the output vector \( y(t) \). Section IV will demonstrate that the hardware implementation of the Single-Stage results in an input-output latency of two time-steps, but that it is legitimate since the simulation time-step is halved compared to the Two-Stage version of the algorithm.

### IV. FPGA IMPLEMENTATION

#### A. Hardware Implementation

A hardware implementation of the Single-Stage DMM algorithm datapath is shown in Fig. 8. The architecture is almost a one-to-one map of the dataflow diagram of Fig. 7.b, and consists of two main computing units: a) The first unit is devoted to updating history terms and computing outputs of interest, i.e. Eq. (24); b) The second unit evaluates the DMM function, i.e. Eqs. (28)-(31). Eq. (24) is implemented by a dedicated MVM module; Eqs. (29) and (31) are combined and implemented by a dedicated MVM module as well. Eqs. (30) is a simple lookup table. Eq. (28) consists of a bit string concatenation and comes at no hardware cost.

Each MVM module from Fig. 8 is shown in Fig. 9. The architecture is composed of \( N \times m \) ROMs and \( m \) Input DP units.

![Dataflow Diagram for the Two-Stage Algorithm](attachment:fig7a.png)

(a) Dataflow Diagram for the Two-Stage Algorithm

![Dataflow Diagram for the Single-Stage Algorithm](attachment:fig7b.png)

(b) Dataflow Diagram for the Single-Stage Algorithm

Fig. 7. Dataflow Diagram: (a) Two-Stage Algorithm; (b) Single-Stage Algorithm.

### C. Low-latency Implementation of the DMM

Fig. 7.a illustrates a dataflow diagram for the Two-Stage Algorithm, and shows the data dependency of the two stages (through \( \sigma(t) \)) that forces their serial execution. Moreover, each stage involves matrix vector multiplications (MVMs) that hinders reaching to a small time-step.

It is possible to reduce the time-step if one rewrites Eqs. (25) in the following form:

\[
\begin{align*}
i_1^h(t) &= H_{L, u}^{\sigma_u(c(t))} u(t) + H_{L, ac}^{\sigma_u(c(t))} H_{dc, u}^{\sigma(t-h)} u(t-h) + H_{ac, u}^{\sigma_u(c(t))} H_{dc, u}^{\sigma(t-h)} i_{hist}^{dc}(t-h) + H_{ac, u}^{\sigma_u(c(t))} H_{dc, u}^{\sigma(t-h)} i_{hist}^{ac}(t-h).
\end{align*}
\]

Hence, knowing \( u(t-h), \sigma(t-h), i_{hist}^{dc}(t-h), i_{hist}^{ac}(t-h), u(t), \) and \( c(t) \) would suffice to determine \( \sigma(t) \). Fig. 7.b illustrates how this rewriting yields a Single-Stage Algorithm version of the DMM by breaking the data dependency. The only limitation of this approach is that two consecutive simulation steps are needed to produce the output vector \( y(t) \). Section IV will demonstrate that the hardware implementation of the Single-Stage results in an input-output latency of two time-steps, but that it is legitimate since the simulation time-step is halved compared to the Two-Stage version of the algorithm.

![Datapath of the hardware implementation of the LLC simulator using Single-Stage DMM Algorithm](attachment:fig8.png)

Fig. 8. Datapath of the hardware implementation of the LLC simulator using Single-Stage DMM Algorithm.

![The \((N, m)\) MVM module used in the proposed LLC simulator](attachment:fig9.png)

Fig. 9. The \((N, m)\) MVM module used in the proposed LLC simulator: The module is composed of \( N \times m \) ROMs and \( m \) Input DP units.
is presented to discuss the impact of parameters \( N_1 \) and \( N_2 \) on area occupation, and simulation time-step.

### B. Number Format

An FPGA can handle real arithmetic using either fixed-point (FXP) or floating-point (FP) format. The FXP format uses less hardware and yields a datapath of lower latency, but has a limited dynamic range. The FP number format allows for a larger dynamic range, but its hardware arithmetic operators are costly in terms of FPGA resource consumption, and require deeper pipelines than their FXP counterparts. Due to latency considerations, this paper considers solely the FXP number format. The limited dynamic range issue of the FXP format is addressed by normalizing matrix entries using a per-unit scale.

The targeted FPGA, a Kintex K325T from Xilinx, uses an asymmetric multiplication block (25 × 18 signed). Hence, the selected number format used by the LLC simulator will be different whether we are dealing with a vector (FXP 25.23) or a matrix (FXP 35.29) in order to offer a good precision to the precomputed matrices and good computation accuracy, while reducing the area footprint of the simulator. A similar idea was presented in [16] and is adopted here.

### C. Design Space Exploration

This section presents a design space exploration whose purpose is to evaluate the impact of parameters \( N_1 \) and \( N_2 \) on area occupation, and simulation time-step. Two implementations are considered in this design exploration, the first approach consists in a Fully Parallel Implementation (FPI) that sets \( N_1 = n_1 = 7 \), and \( N_2 = n_2 = 4 \); whereas the second approach will resort to a Hardware Reuse Technique (HRT) that consists in setting \( N_1 < n_1 \) and \( N_2 < n_2 \), thus time-multiplexing the computations. In this paper, the adopter HRT approach sets \( N_1 = 1 \) and \( N_2 = 1 \).

Also considered is the effect of the FPGP clock frequency on the timing performance and simulation time-step. Various clock frequencies are investigated, namely 40 MHz, 200 MHz and 320 MHz. The timing closure is met by varying the pipelining depth of the DP Unit accordingly. When the 40 MHz clock frequency is targeted, the DP Unit is purely combinational.

### D. Computational Accuracy

The computational accuracy of the hardware LLC simulator (200 MHz FPI) is assessed through a test sequence lasting 0.6s. Parameter Set #2 in Table I is considered. During the test sequence, the input voltage is kept constant at 400 V. The FPGA simulation results are validated against an offline iterative solution, as shown in Fig. 10, where the output voltage \( v_o \) and the switching frequency \( f_s \) are shown. The test sequence comprises the following steps:

1) \( t = 0 \text{s}-0.1 \text{s} \): Operation of the inverter at \( f_s = 312.5 \text{kHz} \).
2) \( t = 0.1 \text{s}-0.13 \text{s} \): Load is shorted (fault); \( f_s = 312.5 \text{kHz} \).

Table II presents the design exploration results for the Kintex K325T for each design approach and each target frequency. It shows that the smallest simulation time-steps (25 ns) are obtained when a FPI approach is adopted. FPI is however the most expensive approach in terms of hardware consumption. The HRT trades simulation time-step for area footprint. Hence, this approach allows considerable saving in hardware utilization (up to 4 folds), with a very acceptable impact on the simulation time-steps, which are less or equal to 100 ns. For HRT, smaller time-steps are achieved by increasing the clock frequency, with the smallest time-step (34.375 ns) obtained for the highest clock frequency (320 MHz). The 200 MHz implementations are the most balanced options for both FPI and HRT approaches.

That being said, all reported implementations are characterized by a very low hardware utilization, a small simulation time-step (\( \leq 100 \) ns), and an input-output (In-Out) latency of two-time-steps. These notable results are more obvious from Table III, which lists from the literature works dealing with the real-time simulation of high-frequency converters, i.e. \( \geq 50 \text{ kHz} \). As one can see from Table III, where the 200 MHz FPI and HRT results have been reproduced, the proposed implementations have indeed a very small footprint and offer one of the smallest time-steps ever reported in the literature. It is noteworthy that, thanks to the proposed DMM, these outcomes are obtained using an implicit solver, without decoupling any part of the circuit, and while using a simultaneous and exact switch state solution.
Table III

Comparison with the existing work on the FPGA-based real-time simulation of resonant converters.

| Power Electronic Circuit | FPGA | Clock (MHz) | Number Formats | LUTs | RAM | DSP Blocks |
|--------------------------|------|-------------|----------------|------|-----|------------|
| LLC                      | K7-325 | 100        | K-329          | 1000 | 100 | 100        |
| K7-410                   | K7-410 | 200        | 200            | 200  | 200 | 200        |
| V7-485                   | V7-485 | 50         | V-35          | 50   | 50  | 50         |
| V5-50                    | V5-50  | 100        | V-35          | 100  | 100 | 100        |

Table IV

LLC with Parameter Set #2 [30]: 2-Norm Relative Errors

| Sequence     | $v_o$ | $t_f$ | $\Delta t$ |
|--------------|-------|-------|------------|
| 0.00s-0.10s  | 0.024%| 0.383%| 0.120%     |
| 0.10s-0.13s  | 0.001%| 0.001%| 0.016%     |
| 0.13s-0.25s  | 0.021%| 0.338%| 0.131%     |
| 0.25s-0.48s  | 0.006%| 0.391%| 0.131%     |
| 0.48s-0.60s  | 0.023%| 0.499%| 0.048%     |
| 0.00s-0.60s  | 0.018%| 0.336%| 0.124%     |

To further assess the accuracy of the FPGA result, each signal is compared to its offline reference. The 2-norm relative error is used as a measure of accuracy [37]:

$$e = \frac{||f_r - f_o||_2}{||f_r||_2}$$

where $f_o$ and $f_r$ are FPGA results and offline reference, respectively. Table IV reports the 2-norm errors for the FPGA results for each sub-sequence as well as for the entire test sequence. All the reported errors are below 0.5% and show the very good performance of the FPGA implementation in different operating mode and condition of the LLC.

V. Conclusion

This paper presented a direct mapped method for the accurate real-time simulation of high switching frequency resonant converters. The method obviates the need for iterations while providing accurate simulation results. The benefits of the proposed method was demonstrated through the implementation
of an FPGA-based LLC real-time simulator capable of achieving a time-step of 25 ns while offering a very small hardware footprint. A design space exploration was proposed to discuss the opportunity of further reducing the area occupation by reusing parts of the computational datapath. It was shown that such an approach can result in considerable savings for higher clock frequencies. The LLC simulator performance has been evaluated for the case of a 500 kHz LLC converter. It has been shown that the DMM real-time results are in excellent agreement with those obtained by offline iterative solution. A 2-norm relative error of less than 0.5% for various operating modes has been reported, which was also shown to hold true in the presence of a fault.

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