PySchedCL: Leveraging Concurrency in Heterogeneous Data-Parallel Systems

Anirban Ghose, Siddharth Singh, Vivek Kulaharia, Lokesh Dokara, Srijeta Maity and Soumyajit Dey

Abstract—In the past decade, high performance compute capabilities exhibited by heterogeneous GPGPU platforms have led to the popularity of data parallel programming languages such as CUDA and OpenCL. Such languages, however, involve a steep learning curve as well as developing an extensive understanding of the underlying architecture of the compute devices in heterogeneous platforms. This has led to the emergence of several High Performance Computing frameworks which provide high-level abstractions for easing the development of data-parallel applications on heterogeneous platforms. However, the scheduling decisions undertaken by such frameworks only exploit coarse-grained concurrency in data parallel applications. In this paper, we propose PySchedCL, a framework which explores fine-grained concurrency aware scheduling decisions that harness the power of heterogeneous CPU/GPU architectures efficiently. We showcase the efficacy of such scheduling mechanisms over existing coarse-grained dynamic scheduling schemes by conducting extensive experimental evaluations for a Machine Learning based inferencing application.

1 INTRODUCTION

The rise of data parallel programming languages like OpenCL [1] and CUDA [2] have paved the way for high throughput application development on big data clusters as well as embedded platforms comprising multiple CPU and GPU cores. Such frameworks support asynchronous event driven programming models that enable both data parallel and task parallel paradigms of computation for implementing high performance parallel applications. The OpenCL runtime system additionally has provision for program portability across different types of devices i.e. the same computational kernel source code can be compiled into device specific binaries for execution on different devices.

Given heterogeneous platforms comprising multiple devices of varying computational power, determining efficient architecture-to-application mapping decisions require extensive domain knowledge of platform level characteristics as well as precedence constraints enforced by the application which is typically represented as a directed acyclic graph (DAG) of tasks. As an illustrative example, let us consider a simple fork-join DAG in Fig. 1.

We consider a heterogeneous platform comprising a single CPU and a single GPU along with a DMA copy engine responsible for transferring data across the PCI-Express bus from the CPU to the GPU and back. The fork-join graph comprises four tasks, each representing some computational kernel which takes as input two input buffers and produces one output buffer. In Fig. 1 the rectangular nodes represent input and output buffers and the circular nodes represent kernels. We use this convention throughout the paper. The edges between a buffer and task represents the precedence constraints between tasks as well. Given a heterogeneous compute platform comprising a single CPU and a single GPU there can exist a total of 16 task-device mappings for this DAG where task(s) are either mapped to a CPU device or a GPU device. In Fig. 1 we explore one of the 16 possible mappings where $k_0$ and $k_3$ are mapped to a CPU device, $k_1$ and $k_2$ are mapped to a GPU device.

Scheduling decisions for general application DAGs are coarse-grained in the sense that each task is mapped to a single device at a time and the associated kernel execution, buffer reads and writes are finished completely before proceeding to execute successors of the kernels. In Fig. 1 for kernel $k_2$ to start execution, $k_1$ must finish and the copy engine should copy the resultant buffer $b_5$ to the host. After that the required input buffer $b_4$ has to be copied to the GPU device. The scheduling decisions are achieved by designing complex host programs that orchestrate the
process of mapping individual kernels to target devices of the heterogeneous platform while maintaining precedence constraints. Alternatively, there exist several frameworks proposed in the recent past that alleviate the burden of implementing such complex orchestrators for undertaking coarse-grained scheduling decisions. The frameworks can be classified into two broad categories. The first category of frameworks [3], [4] provide a top-level API as well as additional programming constructs using which a designer can explicitly specify the mapping and scheduling of OpenCL kernels without writing a complex host program. The second category of frameworks (StarPU, MultiCL) [5], [6] provide scheduling engines optimized for heterogeneous clusters with support for custom scheduling heuristics. These frameworks require as input the DAG specification and a scheduling heuristic for mapping OpenCL kernels optimally on a heterogeneous platform. Both styles rely on deriving coarse-grained scheduling decisions for application DAGs.

In contrast, we believe scheduling decisions should be more fine-grained in nature allowing execution of multiple tasks in the same device and interleaving copy operations with execute operations. This is exemplified in the right hand side scheduling option of Fig. 1. In the figure we show the execution timings of kernels in CPU and GPU along with the data transfers scheduled in the available copy engine in the GPU platform. We can observe for kernel $k_1$, the two input buffers $b_2$ and $b_3$ can be transferred by the copy engine in parallel. Also while kernel $k_1$ is executed, $b_1$ can be transferred asynchronously to the GPU device. The kernel $k_2$ executes in parallel with $k_1$ while sharing the same GPU resource. As a result, we observe that the individual times of $k_1$ and $k_2$ increase. However, the overall time to finish DAG execution decreases.

Implementing such fine-grained scheduling requires designing an even more complex host program capable of i) asynchronously interleaving data transfers as and when required and ii) clustering multiple tasks to the same device as and when feasible. These scheduling decisions can be achieved by setting up multiple worker queues per device and asynchronously enqueueing commands for executing multiple kernels on the same device. For the CUDA runtime system, these worker queues are referred as CUDA streams. For the OpenCL runtime these are referred as command queues. Naturally, the end user has to consider the computational capability of the device and the individual computational requirements of each concurrent kernel before dispatch.

We propose PySchedCL, a platform agnostic programming framework which is possibly the first computer-aided design solution that is capable of automating the process of deriving both coarse-grained and fine-grained scheduling decisions for efficient collaborative execution of application DAGs on heterogeneous multicore comprising CPU and GPU devices. The proposed framework supports reduction of considerable implementation overhead and automatically outputs scheduling decisions that exploit concurrency, requiring minimal intervention from the programmer. The framework is built using the widely used PyOpenCL API [2] and facilitates rapid development and deployment of OpenCL applications. We choose OpenCL, since it offers device portability, thus supporting a myriad of compute devices such as CPU, GPUs, FPGAs, DSPs etc. Our framework enables the user to concentrate only on developing OpenCL kernels and perform minimum manual intervention that would help in finally determining near optimal runtime scheduling decisions for data parallel applications on a target heterogeneous CPU-GPU platform. We note the optimizations proposed are generic and the ideas can be leveraged for any data parallel heterogeneous setting. The salient features of the proposed framework are enumerated as follows.

1) The framework eases development of data parallel applications through specification files, thus completely bypassing the requirement of manually implementing orchestrator host programs. As a representative example, one can implement the host code of a Transformer Neural Network based inference pipeline [8] which takes $\approx 130$ lines of vanilla OpenCL code using a specification file of 25 lines in our framework.

2) The framework comprises a customizable scheduling backend optimized for automatically extracting fine-grained concurrency in applications executing on heterogeneous compute platforms. The backend also enables programmable scheduling with its rich API support, thereby allowing users to design, experiment and validate both coarse-grained and fine-grained scheduling policies on top of the default strategies in the framework.

3) While the usability of the framework is evident in terms of programming effort, we also observe the efficacy of its automated fine-grained scheduling schemes through extensive experimentation for AI workloads such as transformer networks. We have observed considerable speedups in the range of $1.4 - 3.4 \times$ for such applications compared to existing coarse-grained scheduling approaches supported in frameworks such as StarPU [5], SOCL [4] etc.

The remainder of the paper is organized as follows. In Section 2, we present necessary background on OpenCL runtime and the inadequacy of existing OpenCL based high-level scheduling frameworks, thus motivating the requirement of our proposed framework. This is followed by problem formulation in Section 3 and the software architecture of the framework in Section 4. We perform extensive experimentation and provide a comparative evaluation in Section 5. We present a comprehensive list of related work in Section 6 and finally conclude the paper in Section 7.

2 Background and Motivation

Any OpenCL application typically comprises two distinct program entities - i) the host which is a single threaded sequential program executing on one CPU core that orchestrates the entire process of managing data and issuing directives for parallel execution, and ii) kernel(s) which execute on devices with support for vector processing (CPU, GPU, FPGA, DSP etc). For every computational kernel, the single-threaded host program leverages command queues supported by the OpenCL API to issue commands for performing the following operations - i) copying the data from host to input buffers resident on device memory (Host to Device or H2D transfer), ii) launching multiple instances
of the same kernel to process the data copied to the device and iii) copying back the data stored in output buffers in the device back to the host memory after the kernel has finished processing (Device to Host or D2H transfer).

As an illustrative example, we consider a simple OpenCL application DAG depicted in the top left of Fig. 2 where kernel $k_0$ performs a vector addition operation ($vadd$) and kernel $k_1$ performs a simple element-wise trigonometric sine operation ($vsin$) on the output of $k_0$. The kernel $k_0$ takes as input two input buffers ($b_0$ and $b_1$), performs element-wise addition and produces an output buffer ($b_2$). The kernel $k_1$ takes one buffer ($b_3$) and performs an in-place element-wise sine operation. The corresponding kernel codes of $k_0$ and $k_1$ are depicted in the functions $vadd$ and $vsin$ respectively in the top right subfigure of Fig. 2.

Considering a heterogeneous platform comprising two GPU devices $GPU_0$ and $GPU_1$, it may be observed in the bottom right subfigure of Fig. 2 that two command queues are setup, one for each GPU device. Kernel $k_0$ executes on $GPU_0$ and kernel $k_1$ executes on $GPU_1$. Each command queue consists of a sequence of commands for H2D transfers, kernel execution and D2H transfers pertaining to each kernel. The associated host program depicted in the bottom left of Fig. 2 illustrates how the command queues are populated.

For $GPU_0$, the host first issues two write commands ($\text{clEnqueueWrite()}$) for copying data from the host to the buffers $b_0$ and $b_1$. This is followed by a barrier directive ($\text{clEnqueueBarrier()}$). The barrier command in general ensures that all commands enqueued previously finish before proceeding to execute commands enqueued after the barrier. In this case, it is ensured that the write commands are finished before processing the next command in the queue. The host next enqueues a kernel execution command or $ndrange$ command using the function $\text{clEnqueueNDRangeKernel()}$ which spawns a collection of threads referred as work items where each work item executes the function bodies depicted in the top right of Fig. 2. The execution command is followed by a barrier directive and finally one read command ($\text{clEnqueueReadBuffer()}$). In a similar fashion, for the command queue of device $GPU_1$, the host issues a write command (for buffer $b_3$), an execute command for $vsin$ kernel and read command (for buffer $b_3$). We note that barriers in general incur synchronization overhead. For the remainder of the paper we assume that barriers are not enqueued and that command queues follow inorder execution i.e. commands are executed in the order which they are enqueued and each command cannot start until the previous command has finished completely.

The OpenCL runtime system uses event objects for enforcing dependencies across multiple commands resident in same or different queues. In Fig. 2 the $i^{th}$ write for the H2D transfers (highlighted by red edges in the OpenCL DAG) are associated with event $w_i$. In a similar fashion, the $i^{th}$ $ndrange$ command for kernels and $i^{th}$ read command for D2H transfers (highlighted by red edges in the OpenCL DAG) are associated with events $e_i$ and $r_i$ respectively. These are labelled in the OpenCL DAG. The associated event for a command is specified in the last argument of a function call with the $\text{clEnqueue}$ prefix in the host program. The second last argument of each such function represents events on which the event associated with command $c$ is dependent for execution. For our representative example, from the OpenCL DAG it may be observed that the event $w_3$ is dependent on $r_1$, i.e. the write command corresponding to $w_3$ should take place only when the read command corresponding to $r_1$ is complete. This is specified in the $\text{clEnqueueWriteBuffer}$ command for buffer $w_3$.

Finally, for the event $r_2$ associated with the last read command (‘read for $b_3$’), a callback function $cb$ is setup using the $\text{clSetEventCallback()}$ API call. A callback function $cb$ in general is registered with any event $ev$. The object to the event along with data to be accessed by the callback function once it starts execution is specified in user_args. The callback function is spawned on a separate thread in parallel with the host program once the event $ev$ (denoting computation/data transfer) has achieved some status (any one of enqueued / submitted / complete) as specified in the argument status and is implemented typically to notify the host. In Fig. 2 $cb$ notifies the host, once $r_2$ has achieved complete status i.e. ‘read for $b_3$’ has finished. We note the $\text{clEnqueue}$ OpenCL functions enqueue operations to each command queue for the devices, i.e. after enqueuing the commands, the host is free to execute something else while those command executions are executed on the target device. 

#### 2.1 Motivation

We consider a transformer application [8] which is a popular Deep Learning Neural Network pipeline for Natural Language Processing (NLP) tasks. The application exhibits ample scopes for exploiting concurrency with the possibility of executing multiple instances of standard General Matrix Multiply (GEMM) kernels in parallel. A sample DAG comprising 8 kernels for one layer of the transformer network is presented in Fig. 3.

As per our earlier convention, the rectangular nodes represent input and output buffers and the circular nodes represent kernels. Each kernel is labeled with the corresponding level number starting from 1. Initially there is a copy operation which copies the same buffer to each of the kernels at level 1. Each of the kernels in levels 1, 4, 5, 6 represent

![Fig. 2: OpenCL Execution](image-url)

![Fig. 3: Sample DAG](image-url)
General Matrix Multiply (GEMM) kernels where each kernel takes as input two buffers and produces one output buffer. The kernels in level 2 and level 3 represent transpose and softmax operations respectively, each processing one input buffer to produce one output buffer. The edges between rectangular nodes, i.e. buffers, represent data dependencies for the DAG. For enforcing precedence constraints between any pair of kernels \((k_i, k_j)\), a programmer shall set event dependencies between read commands for output buffers of \(k_i\) and write commands for input buffers of \(k_j\), as was observed in Fig. 2. For our transformer DAG depicted in Fig. 3 we assume that the entire DAG is mapped to a single GPU device. This implies that the output buffers of kernels at level \(i\) to be processed as input buffers of kernels at level \(i+1\), \(i = [1, 5]\) are already resident in GPU memory. Thus explicit reads and writes for dependent buffers between kernels in levels 1-5 are not required. In this scenario, the programmer needs to set up event dependencies between \textit{ndrange} commands of kernels in levels \(i\) and \(i+1\) as depicted in the event dependency graph. One can observe from Fig. 3 that the actual H2D and D2H transfers (red edges) occur only for kernels at level 1 and level 6 while the remaining black edges reflect the input-output buffer dependencies between kernels in the DAG.

**Fig. 3: Event Dependencies for DAG**

In the left hand side of Fig 3, we label each kernel \(k\) of the DAG with event \(e_k\) associated with the corresponding \textit{ndrange} command for that kernel. Apart from this, we have a \textit{write} command \(w_0\) responsible for copying one common buffer to be used for each GEMM kernel in level 1. We also have \textit{write} commands \(w_1, w_2, w_3\) for each of the remaining buffers required by GEMM kernels in level 1 and a \textit{write} command \(w_4\) for a buffer required by GEMM kernel in level 6. Finally we have a \textit{read} command \(r\) for the output buffer of the GEMM kernel in level 6. The dependencies between these events are depicted in the corresponding event dependency graph in the right hand side of Fig. 3. The end designer is burdened with the task of manually writing a host program that will capture the event dependencies illustrated in this dependency graph for ensuring that precedence relations of the DAG are met during execution. This is achieved by using the complex programming constructs for OpenCL events and callback functions as discussed earlier. Existing heterogeneous programming frameworks like StarPU [3], SOCL [4] and MultiCL [6] all impose this same level of programming complexity. We next examine how coarse-grained and fine-grained scheduling decisions are made for mapping this DAG onto a single GPU device with the help of Figs. 4 and 5 respectively.

We execute the DAG on a heterogeneous platform comprising an NVIDIA GTX-970 GPU device and a Quadcore Intel i5-4690K CPU device. Coarse-grained scheduling is achieved by setting up a single command queue on the GPU device as depicted in the right hand side of Fig. 4. As a consequence, all \textit{read}, \textit{write} and \textit{ndrange} commands for each of the 8 kernels as labelled by the events used in Fig. 3 execute serially on the GPU device. In the left hand side of Fig 4, we plot a Gantt chart representing the time taken by the commands. It is evident from the Gantt chart that such serialized execution of commands on the GPU device result in an execution time of 105ms.

**Fig. 4: Coarse-grained Scheduling**

In contrast, if we set up multiple command queues, there is a possibility of leveraging fine-grained scheduling decisions that can i) interleave data transfers with \textit{ndrange} operations and can ii) execute multiple \textit{ndrange} operations concurrently. In the right hand side of Fig. 5, we setup 3 command queues for achieving this. As a result of enqueuing the operations using multiple command queues,
we observe from the corresponding Gantt chart in the left hand side of Fig. 3 several write and ndrange commands are interleaved thus resulting in an 8% decrease in overall execution time with the DAG finishing in 95ms. On closer inspection, one can observe from the Gantt chart that while the ndrange command associated with e1 is executing, the buffer associated with w2 can be copied simultaneously. This is because w2 and e1 belong to separate command queues in the right hand side of Fig. 3. In a similar vein, w3 can also be copied while e1 and e2 are executing. Additionally, it can be seen that all kernels in level 1 i.e. ndrange commands associated with events e1, e2 and e3 are executing concurrently on the same device. We can observe something similar happening for the events e5, e6 and w4 in the Gantt chart as well. However, there are commands that despite belonging to different command queues are not able to execute simultaneously due to the precedence relationships enforced by the event dependency graph illustrated in of Fig. 3. These dependencies being part of the actual command queue setup, are represented by inter-queue edges between events in the command queue structure in the right hand side of Fig. 3. For example, since e4 is dependent upon e2, it can start execution only after e2 has finished. But e4 can still overlap with e3. Another interesting observation would be that the individual execution times for each kernel increases slightly as a result of interleaving. This is due to the fact, that different work groups of different kernels that have been concurrently dispatched are scheduled in a round robin fashion to the compute units of the device, thus causing resource contention 9. However, the total time for finishing kernels concurrently is lesser than the case when they are dispatched in sequence. We note that both the cases represented in Figs. 3 and 5 depict one of the possible command queue configurations and multiple such possibilities exist both for coarse-grained and fine-grained scheduling respectively.

The Gantt charts for the execution of DAG highlighted in Fig. 3 thus reveal that fine-grained scheduling has potential performance benefits over coarse-grained scheduling in the context of data parallel programming models used for GPGPU systems.

3 Problem Formulation

Let us consider a heterogeneous platform P depicted in Fig. 4 which comprises a CPU device and a GPU device connected via a PCI-Express bus. Each device has support for executing multiple kernels simultaneously. The OpenCL standard supports device fission for CPU devices i.e. a single CPU device can be partitioned into multiple subdevices, thereby enabling concurrent execution for the same. We consider as GPU an NVIDIA device with Hyper-Q support 4. Hyper-Q offers a solution that allows the CPU host to dispatch multiple kernels simultaneously on the GPU device with the help of hardware managed work queues.

Let us represent an OpenCL application as a directed acyclic graph (DAG) \( G = ((K, B), (E_1, E_0, E)) \) where \( K \) denotes the set of OpenCL kernels, \( B = B_1 \cup B_0 \) represents the set of buffers for all \( k \in K \). The set \( B_1 \) denotes the set of input buffers and the set \( B_0 \) denotes the set of output buffers. The set \( E_1 \subseteq B_1 \times K \) denotes the set of edge dependencies between each input buffer and kernel, \( E_0 \subseteq K \times B_0 \) denotes the set of edge dependencies between each kernel and output buffer. The set \( E \subseteq B_0 \times B_1 \) denotes the set of input output buffer dependencies across kernels in the DAG. For the remainder of the paper, we shall use this notation for representing DAGs. Command queues are typically setup per device, depending on which kernels are mapped to which devices.

Fig. 6: Platform and DAG Model

Given an OpenCL DAG \( G \), we denote a task component \( T \) as a subset of kernels \( K' \subseteq K \) where each kernel \( k \) is mapped to a device of the same type say \( \text{dev} \). In our case, \( \text{dev} = \{ \text{cpu, gpu} \} \). In Fig. 6, \( T = \{ k_0, k_1, k_2, k_3, k_4 \} \). For a given task component we define the following terminology.

**Definition 1.** Given a task component \( T \) pertaining to some OpenCL DAG \( G \), we define \( \text{FRONT}(T) \) as the set of kernels where each kernel \( k \) has input buffer dependencies \( (b_i, k) \in E_1 \) such that for \( b_i \), if there exists an immediate successor \( b_j \) where \((b_j, b_i) \in E \) and \((k', b_j) \in E_0 \), then the kernel \( k' \) belongs to a different task component \( T_{a'} \).

In Fig. 6, we observe that \( \text{FRONT}(T) = \{ k_0 \} \), since both input buffers \( b2 \) and \( b3 \) have predecessors pertaining to kernels belonging in a different task component.

**Definition 2.** Given a task component \( T \) pertaining to some OpenCL DAG \( G \), we define \( \text{END}(T) \) as the set of kernels where each kernel \( k \) has output buffer dependencies \( (k, b_i) \in E_0 \) such that for \( b_i \), if there exists an immediate successor \( b_j \) where \((b_i, b_j) \in E \) and \((b_j, k') \in E_1 \) then kernel \( k' \) belongs to a different task component \( T' \).

In Fig. 6, we can observe that \( \text{END}(T) = \{ k_3, k_4 \} \).

**Definition 3.** Given a task component \( T \) pertaining to some OpenCL DAG \( G \), we define \( \text{IN}(T) \) as the set of kernels where each kernel \( k \in T \), \( k \notin \text{FRONT}(T) \), \( k \notin \text{END}(T) \).

In Fig. 6, we can observe that \( \text{IN}(T) = \{ k_1, k_2 \} \). We classify buffer edge dependencies \((b_i, b_j) \in E \) into two categories -i) intra edge, ii) inter edge. Given a task component \( T \) pertaining to a DAG \( G \), an edge \((b_i, b_j) \) for kernels \( k_i, k_j \) such that \((k_i, b_i) \in E_0 \), \((b_j, k_j) \in E_1 \) represents an intra edge if \( k_i \) and \( k_j \) belong to the same component and inter edge if they belong to different task components.
we can observe that \((b_4, b_6), (b_4, b_7), (b_9, b_{11})\) and 
\((b_1, b_{12})\) are intra edges, while \((b_0, b_2), (b_1, b_3), (b_{13}, b_{15})\) 
and \((b_{14}, b_{16})\) are inter edges.

We classify kernel-buffer dependencies in \(E_I\) and \(E_O\) into two categories - i) isolated copy and ii) dependent copy. 
Given any kernel \(k_i\), an edge \((b_i, k_i) \in E_I\) represents an 
isolated copy (write) if for every \(b_k \in B\), \((b_k, b_i) \notin E\). 
The same edge can represent a dependent copy if there exists 
some buffer \(b_k \in B\) such that \((b_k, b_i) \in E\). In a similar 
fashion, an edge \((k_i, b_j) \in E_O\) represents an isolated copy (read) if 
for every \(b_k \in B\), \((b_j, b_k) \notin E\) respectively and a dependent 
copy (read) if there existed some \(b_k \) such that \((b_j, b_k) \in E\).

In Fig.\[5\] the edges \((b_5, k_1)\) and \((b_8, k_2)\) represent isolated 
writes while every other kernel-buffer dependency represents 
dependent copies.

**Definition 4.** Given a task component \(T\) of an application DAG 
\(G\) mapped to a device \(d\) with \(r\) command queues, we define the 
command queue data structure \(Q = (Q, ENQ)\) as follows. 
\(Q = \{q_1, q_2, \ldots, q_r\}\) is the set of command queues, each 
command queue \(q_i\) is a list such that every location \(q_i[j] \in \{write, nrange, read\}\) contains 
young three of any these command queues pertaining to some kernel belonging to \(T\). 
Each element of \(E_O\) is a precedence constraint of the form \(\langle q_i[j], q_i[r] \rangle\),  
\(1 \leq s \neq t \leq r\) which enforces that the \(s\)-th command enqueued in \(q_s\) 
must finish execution before the \(t\)-th command enqueued in \(q_t\) can start.

A precedence constraint \(\langle q_i[s], q_i[t] \rangle \in E_O\) exists if any 
of the following is true - i) \(q_i[s]\) is an isolated/dependent 
write \((b_k, q_i)\) and \(q_i[t]\) is an nrange operation for kernel 
\(k_m\), ii) \(q_i[s]\) is an nrange operation for kernel \(k_m\) and 
\(q_i[t]\) is a dependent/isolated read \((k_n, b_l)\), iii) both \(q_i[s]\) and \(q_i[t]\) 
are nrange operations for kernels \(k_m\) and \(k_n\) respectively such 
that there exists edges \((k_m, b_l) \in E_O\), \((k_n, b_m) \in E_I\) 
and \((b_l, b_n) \in E\) where \((b_l, b_n)\) is an intra edge. In Fig.\[6\] 
\((b_3, k_0)\) corresponds to a dependent write for kernel \(k_0\) thus 
requiring a dependency between associated operations \(w_2\) 
and \(e_1\) in \(Q\). The edge \((e_1, e_2)\) represents the dependency 
between kernels \(k_0\) and \(k_2\) arising due to the dependencies 
\((k_0, b_2)(b_5, b_7)(b_7, k_2)\) where \((b_5, b_7)\) is an intra edge. 
The operations of a kernel \(k_i\) in \(T\) that are to be enqueued to 
some queue \(q_s \in Q\) of \(Q\) are determined by the framework 
using an enqueue procedure \(enq(k_i, q_s)\) and is described as 
follows.

i) If \(k_i \in FRONT(T)\), \(enq(k_i, q_s)\) enqueues all dependent 
write commands for buffers \(b_m\) corresponding to dependent 
writes \((b_m, k_i) \in E_I\) followed by nrange command for \(k_i\) 
to \(q_s\).

ii) If \(k_i \in END(T)\), \(enq(k_i, q_s)\) enqueues nrange command 
for \(k_i\) followed by all dependent reads \((k_i, b_m) \in E_O\) 
for \(b_m\) to \(q_s\).

iii) If \(k_i \in IN(T)\), \(enq(k_i, q_s)\) only enqueues nrange for \(k_i\) 
to \(q_s\).

Note, a kernel may belong to any combination of the three 
sets discussed above. One can observe that since all kernels in 
\(T\) are mapped to the same device, the \(enq\) procedure 
using the rule set above ensures that redundant dependent 
reads from \(FRONT(T)\), redundant dependent writes and 
reads from \(IN(T)\) and redundant dependent writes from 
\(END(T)\) are avoided from being enqueued. Apart from 
these enqueue operations, for every kernel \(k_i\), irrespective 
of which set it belongs to, \(enq(k_i, q_s)\) enqueues to \(q_s\) - (i) 
all isolated writes \((b_m, k_i) \in E_I\) for input buffers \(b_m\) before 
enqueuing the nrange command for \(k_i\) and (ii) all isolated 
reads \((k_i, b_n) \in E_O\) for output buffers \(b_n\) after enqueuing 
the nrange command for \(k_i\).

Note that the above rules for \(enq\) when applied to individual 
kernels in a task component \(T\) need not generate a unique 
command queue structure \(Q\) for a device. This, coupled 
with different possible task component partitions based on 
device mapping decisions of the overall DAG lead to multi-
ple possible dispatch orderings, i.e. scheduling decisions 
for the kernels.

**Definition 5.** Consider a DAG \(G = ((K, B), (E_I, E_O, E))\), 
with a set of task components \(T = \{T_1, T_2, \ldots, T_M\}\) such that 
\(\bigcup_i T_i = K\), a heterogeneous CPU-GPU multicore target platform 
\(P = \{d_1, d_2, \ldots, d_p\}\) containing \(p\) devices, and the number 
of command queues for each device \(\{q_1, q_2, \ldots, q_N\}\) as given. 
Consider, the set of all command queues \(Q = \{q_1, q_2, \ldots, q_N\}\) 
where \(N = \sum_r r\). For such an application-architecture pair, 
a (valid) schedule \(\sigma\) is a collection of enqueue procedures 
\(\langle \text{enq}(k_i, q_j) \rangle | k_i \in K, q_j \in Q \rangle\) such that each kernel \(k_i \in K\) 
is dispatched in a topologically sorted fashion with respect to the 
ordering of \(k_i\)'s enforced by the edges in \(G\).

Our framework facilitates automated creation of such 
correct-by-construction valid schedules, both coarse-grained 
and fine-grained.

### 4 Software Architecture

An overview of the software architecture for PySchedCL is 
shown in Fig.\[7\]. The framework comprises two distinct 
modules, the functionalities of which are elaborated below.

**A. Design Frontend:** The input to the scheduling 
framework is an OpenCL application represented in the form 
of an OpenCL DAG as discussed earlier. The proposed 
framework supports a specification file using which pro-
grammers can easily design an OpenCL application for 
execution on a heterogeneous platform. The specification 
file contains necessary buffer-kernel dependency information 
for an OpenCL DAG, along with necessary attribute 
information such as input/output buffers, variables passed 
as arguments for each constituent kernel. The file uses 
Javascript Object Notation (JSON) format. Let us consider 
an example DAG comprising three kernels as depicted in 
Fig.\[8\] Each kernel in \(\text{dag.json}\) file as shown in top-left 
box of Fig.\[8\] is designated with i) a unique identifier 
field called \(\text{id}\), ii) a \(\text{name}\) field depicting the name of kernel 
function, iii) a device field \(\text{dev}\) indicating the device type 
to which the kernel should be mapped (‘cpu’ or ‘gpu’). The 
task component partitioning \(T = \{T_1, T_2, \ldots, T_M\}\) for the 
DAG is specified as a list \(tc = \{\{\ldots\}, \{\ldots\}\}\) with 
each sub-list \(i\) being an enumeration of the kernel \(id-s\) in 
\(T_i\). All kernels mapped to a task component must be given 
the same device type. In Fig.\[8\] the list \(tc = \{\{0, 2\}, \{1\}\}\)
specifies that the kernels with ids 0 and 2 are mapped as a task component with both constituent kernels having ‘gpu’ device preference while kernel with id 1 is the other task component having ‘cpu’ device preference. The number of command queues to be setup for the platform is specified in the list cq where each element \( r_i : n \) denotes that device \( d_i \in \mathcal{P} \) has \( r_i = n \) command queues. Assuming a target platform for 4 devices, we can observe from Fig. 8 that \( cq = \{ r_1 : 4, r_2 : 2, r_3 : 2, r_4 : 4 \} \). The framework uses this information to automatically set up \( \mathcal{Q} \) data-structure for each task component. The dependency information of the DAG is specified as a set of edges of the form \( k_i, b_r \rightarrow k_j, b_s \), where \( k_i, j \) represent kernel ids that are dependent, \( b_r \) is an output buffer of \( k_i \) and \( b_s \) is an input buffer of \( k_j \) i.e. \( (k_i, b_r) \in E_{O}, (b_s, k_j) \in E_I \) and \( b_r, b_s \in E \). The ids for the buffers \( b_r \) and \( b_s \) are represented by their corresponding argument positions in the function call for the kernels. For example, consider the entry 0, 2 \( \rightarrow \) 2, 0 in the dag.json file of Fig. 8. This implies that the output buffer specified in argument 2 of kernel 0 will be used as input buffer specified in argument 0 of kernel 2. Note in the bottom-left box of Fig. 8 the tag "outputBuffers" for the matmul kernel (which is kernel ‘0’). The argument position pos for this buffer is indicated as 2 in the specification.

Fig. 8: JSON Specification File for DAG

Kernel information includes i) the name of the function (matmul), ii) the filepath of the required source file (gemm.cl), iii) the kernel dimensionality in workDimension and iv) the total number of work items (globalWorkSize) to be launched for this kernel. The variable globalWorkSize is a three element list where each element refers to the number of work items along a particular dimension. Buffer information for each kernel constitutes information for three buffer lists - i) inputBuffers reserved for input buffers, ii) outputBuffers reserved for output buffers and iii) ioBuffers reserved for buffers which are treated as both input and output by the kernel. Each buffer is characterized by the tuple \( (type, size, pos) \) where type denotes the data type for each element in the buffer, size denotes the total number of elements in the buffer, and pos denotes the index position of the buffer argument in the actual function call of the kernel. Variable argument information for every kernel is denoted by the tuple \( (type, pos, value) \) with type, pos meaning same as earlier and value denoting the argument variable.

The required attribute information comprising information specific to the kernel implementation, buffers and variable arguments for the matmul kernel is depicted in Fig. 8. The matmul kernel takes as input two matrices \( A, B \) of dimensions \( M \times K, K \times N \) respectively and produces an output matrix \( C \) of dimension \( M \times N \). For this, a total of \( M \times N \) work items is launched. In Fig. 8, the three variable arguments are \( M, N, K \) for matmul and globalWorkSize = \( [M, N, 1] \). In Fig. 8 the value of size for the output buffer is set as the symbolic expression \( M \times N \). Guidance parameters specified as symbolic expressions aid in depicting the relationship between number of work items launched and the dataspaces to be processed. The values of the symbolic variables \( M, N, K \) can be configured by the user as command line parameters before dispatching the kernel. In general, guidance parameters can be specified both as compile time constants or using expressions containing symbolic variables as exemplified.

We have implemented an LLVM [10] based compiler pass with the help of the library reported in [11] that i) parses the abstract syntax tree of each OpenCL kernel and automatically generates necessary attribute information for each kernel, ii) infers the dimensionality, types and positions of variables and buffers used for each kernel, 3) classifies buffers as input/output buffers by understanding whether it is treated as l-values or r-values in the body of the function. This pass thus automatically generates most fields of the JSON file by analysing the individual kernels. After this, the user is only required to specify guidance parameters which include - i) the size of the buffers ii) the number of work items iii) the values of the variable arguments.

B. Scheduling Backend: As depicted in Fig. 7, the scheduling backend processes the specification file of an application DAG and takes care of setting up OpenCL command queues for mapping kernels across devices of a heterogeneous CPU/GPU platform. We explain the working principle of the backend with the help of the procedure schedule highlighted in Algorithm 1.

Algorithm 1: Scheduling in PySchedCL

Initialization: The procedure executes on the host device, and first parses the input specification (for the application graph \( G \) along with the set of devices in the target platform \( \mathcal{P} \)) and populates the centralized task queue \( \mathcal{F} \) with task components that are ready for dispatch using \( ready_task_components() \) (line 2). Here, a task component \( T \) is added to \( \mathcal{F} \) if for every kernel \( k_i \in \mathcal{F}(T) \), there exists no predecessor. The task queue \( \mathcal{F} \) is implemented
as a priority queue, where the user can specify custom ranking measures for enforcing an ordering among task components to be selected from $P$. The set $A$ represents the set of available devices and is initialized to all the devices contained in $P$ (line 2).

**Primary Scheduling Loop:** The procedure $schedule$ runs the routines inside the while loop (line 3-6) and continues until all kernels of the DAG have not finished execution. In any scheduling iteration where the frontier $F$ and the set $A$ are non-empty (line 4), the $select$ routine inspects task components in $F$ and returns $T$ and $d$ (line 5) if an available device $d \in A$ is found that matches the device preferences of all the constituent kernels of some task component $T \in F$. We note that the $select$ routine is a blocking call i.e. if a task component $T$ or a matching device $d$ is not immediately available, the routine blocks further execution of the $schedule$ routine until a suitable match is found. In the meantime, kernels already dispatched continue executing on their respective devices. Once $T$ and a matching device $d \in A$ is obtained using $select$(line 5), the framework spawns a separate child thread responsible for running $setup_cq()$ and $dispatch()$ functions for mapping $T$ to $d$ (line 5). This ensures that on the host device i) the master thread running $schedule$ continues to search for existing task components that are free to execute on matching devices that are available using $select$ (lines 3-5) and ii) the subsequent operations for setting up command queue data structures (once a match is found) and dispatching each task component (line 5) are performed in parallel using separate child threads. In the event, if one of $F$ or $A$ is empty, the $schedule$ procedure remains idle using $sleep_till_cb_update()$ (line 6). The data structures $F$ and $A$ are updated by callback functions with new task components and devices, once they are available again. This happens following the procedure outlined in $cb$ (lines 13-17). We note such callback functions when initiated operate in a parallel thread w.r.t. $schedule$, executing on the host device. Once one of these data structures are updated by respective callbacks, the $schedule$ routine resumes the scheduling loop (lines 3-5) if any kernel of $G$ remained unfinished.

**Command Queue Setup:** In each child thread, the $setup_cq$ procedure is used to set up the command queue structure $Q$ (line 5) for a given $T$ and $d$. The data structure $Q = (Q, E_Q)$ is first initialized using the init routine (line 9) such that $E_Q = \{\}$ and $Q = \{q_0, q_1, \ldots, q_D\}$ where $D$ represents the number of command queues to be setup as specified by $r_i \in cq$ for that device $d$ in the JSON file. We shall explain how $setup_cq$ finishes setting up $Q$ with the help of an illustrative example depicted in Fig. 9 where we map the task component $T = \{k_0, k_1, k_2, k_3, k_4\}$ to a GPU device using a total of 3 command queues i.e. $Q = \{q_0, q_1, q_2\}$. After init(), the procedure next initializes the set unprocessed with kernels belonging to FRONT($T$) (line 8) and keeps on updating $Q$ until all kernels of $T$ have been processed (lines 9-12). A kernel $k$ is said to be processed once all read, write and nrange operations pertaining to it have been enqueued to a queue, otherwise it is unprocessed. Initially, unprocessed = \{ $k_0$ \} for the task component $T$ in Fig. 9. Next, in each iteration of the while loop (lines 10-12) a kernel $k$ is first selected from unprocessed (line 10). A queue $q$ is selected in a round robin fashion from $Q$ of $q$ using $sel_r.(Q)$ (line 10). Following the rules outlined in Section 3, the $enq(k,q)$ function enqueues relevant read, write and nrange commands of kernel $k$ to $q$ (line 10). In Fig. 9, we observe that $k_0$ and $q_0$ are first selected and $enq(k_0,q_0)$ pushes write commands $w_1$ and $w_2$ to $q_0$ followed by the nrange command $e_1$. The write commands correspond to the two inter edges (b0, b2) and (b1, b3). The $setup_cq$ function next sets up dependencies between relevant operations i.e. synthesizes $E_Q$ of $Q$ using $set_dependencies()$ (line 11). For kernel $k_0$, we have no dependencies to set. Once this is done, the list unprocessed is updated with the successors of $k$ that have not been processed using update (line 11).

The sequence of $enq$ calls and step by step construction of the set $E_Q$ by $setup_cq$ are highlighted in Fig. 9. For kernel $k_1$ belonging to $IN(T)$, $enq(k_1,q_1)$ pushes the isolated write operation $w_3$ and the nrange operation $e_2$ to $q_1$. The $set_dependencies()$ function populates $E_Q$ with the dependency $(e_1,e_2)$. One may observe that despite there being a dependency between $k_0$ and $k_1$, the round-robin selection of queues ensures that write commands $w_1$ and $w_2$ enqueued to $q_0$ can be interleaved with the write command $w_3$ enqueued to $q_1$. In a similar fashion, as depicted in Fig. 9, the $enq$ function pushes operations for kernels $k_2$, $k_3$ and $k_4$ to $q_2$, $q_0$ and $q_1$ respectively while the $set_dependencies()$ function sets up $E_Q$. One can also observe that since nrange operations $e_2$ and $e_3$ belong to different command queues with no dependencies, they can also execute in parallel. We note that while setting up $Q$, the framework uses low-level OpenCL API calls with the clEnqueue prefix for i) enqueuing commands in each $q \in Q$ ii) associating event objects with each such command and iii) enforcing dependencies in $E_Q$ using these event objects as discussed in Section 2.

**Callback Assignment:** In addition to constructing $Q$, $setup_cq$ uses the setcallbacks function (line 12) to investigate already enqueued operations pertaining to each kernel $k \in END(T)$ in $Q$ and register multiple instances of the callback procedure $cb$ (lines 13-17). This is done by registering an instance of $cb$ using $clSetEventCallback()$ (refer Section 2) for every event ev associated with certain commands for all kernels $k \in END(T)$ in $Q$, depending on the device $d$ where $T$ gets mapped to.

1) If $d$ is a GPU device, callback is registered for events associated with every dependent read command pertaining to an inter edge $b_i, b_j \in E$ such that $k, b_i \in E_Q$. In Fig. 9, callbacks are registered for events associated with the
read commands \( r_1 \) and \( r_2 \) pertaining to kernels \( k_3 \) and \( k_4 \) belonging to \( \text{END}(T) \).

2) If \( d \) is a CPU device sharing the same memory space as that of the host, callback is registered for the event pertaining to the \( \text{ndrange} \) operation of \( k \) if \( b_i, b_j \in E_D \) and there exists an inter edge \( b_i, b_j \in E \). If \( T \) had been mapped to a CPU device in Fig. 3, the callbacks would have been registered with events associated with the \( \text{ndrange} \) commands \( e_4 \) and \( e_5 \).

While registering each callback instance, the routine \( \text{set callbacks()} \) also ensures to specify the associated event \( ev \), task component \( T \), device \( d \) and global task queue \( F \) and device set \( A \) in \( \text{user args} \) argument of \( \text{clSetEventCallback()} \) so that they are accessible once the callback instance starts execution.

### Thread safe Callback Procedure

Each instance of the callback function registered using \( \text{set callbacks()} \) is spawned at runtime when the associated event completes and follows the functionality outlined in procedure \( cb \) (lines 13-17). The associated data \( ev, T, d, F \) and \( A \) as discussed above are first obtained using \( \text{get user args()} \) (line 14). Next, the routine \( \text{update status()} \) (line 15) is used to update based on \( ev \) which kernel \( k_i \) has completely finished execution in \( \text{END}(T) \). We say that a kernel \( k_i \) has finished execution if i) \( k_i \) was mapped to a CPU and \( ev \) pertained to an \( \text{ndrange} \) command or ii) \( k_i \) was mapped to a GPU and every event other than \( ev \) pertaining to dependent \( \text{read} \) commands have also completed. This indicates that the output buffers produced by \( k_i \) are available in the host memory space. Depending on which kernel \( k_i \) has finished, task components \( T' \notin F \) containing kernels \( k_j \in \text{FRONT}(T') \) which are successors of \( k_i \), are next investigated if they are ready for dispatch in the function \( \text{get ready suc}() \) (line 15). If it is observed that all predecessors of every kernel in \( \text{FRONT}(T') \), have finished execution, then \( T' \) is ready for dispatch. All such ready task components are populated in the set \( T' \) and are added to \( F \) using \( \text{update task queue()} \) (line 16). Finally, if all kernels of \( \text{END}(T) \) have finished execution i.e. all kernels in \( T \) have completed, the device \( d \) is returned back to \( A \) using the \( \text{return device()} \) function (line 17). One may further note that the routines \( \text{return device()} \) and \( \text{update task queue()} \) are rendered thread safe using the \text{lock()} and \text{unlock()} functions. As discussed earlier, callback functions are initiated in separate threads and thus execute in parallel with the host thread running \( \text{schedule} \) while potentially modifying \( F \) and \( A \). Furthermore, as described above multiple callbacks can be registered for the same task component and can potentially execute simultaneously. It is therefore imperative that atomic updates are applied to the shared data structures \( F \) and \( A \) by the callback functions to ensure correctness.

### Final Dispatch

Once the callback functions are set, the \( \text{dispatch()} \) function (line 8) is called which executes the \( \text{clFlush()} \) function once for each command queue in \( Q \) to ensure that the commands are submitted to the device. Once this call is made, the associated command queues are locked i.e. they cannot be used by other task components that are ready for dispatch.

The algorithm \( \text{schedule} \) highlights a generic scheduling framework which allows for specifying the task component partitioning \( T \) and overriding the implementation of the \text{select} routine for choosing \( T \in T \) and \( d \in A \) with different scheduling policies. We note that the design principles of \text{PySchedCL} extend beyond OpenCL and holds in general for any heterogeneous CPU/GPU platform that supports SIMD style programming and a runtime system that supports some abstraction of worker queues for enqueuing operations on compute devices. One can thus incorporate the methodologies highlighted in this paper by implementing \text{schedule} in CUDA (using \text{streams}) or modern frameworks such as DPC++ (using SYCL queues) \cite{12}. The focal point of our work lies in investigating fine-grained scheduling techniques as opposed to traditional coarse-grained policies and presenting a generic design workflow for achieving the same.

### 5 Experimental Results

The Transformer Neural Network \cite{8} has proven to be a viable alternative to Recurrent Neural Networks \cite{13}, in Natural Language Processing (NLP) tasks such as Named Entity Recognition and Neural Machine Translation. The transformer architecture is based on the standard encoder-decoder architecture used in sequential learning tasks, and is depicted in Fig. 7. The input to the transformer is a sentence matrix \( X = [w_1, w_2, w_3, \ldots, w_n] \) where \( w_i \in \mathbb{R}^d \) represents an embedding vector for each word in the sentence. The matrix \( X \) undergoes transformations through each layer in the encoder and decoder before yielding the target vector \( Y \). An attention mechanism is used to assign scores indicating the importance of each word in yielding the sentence. This is achieved by a series of matrix transformations through a mechanism called multi-headed attention. Each layer in the transformer comprises multiple heads operating in parallel where each head \( h \) represents a series of linear algebra operations on the sentence matrix \( X \) for generating a contextual embedding matrix \( Z_h \) comprising contextual embedding vectors for each of the \( n \) words in the sentence. Each head \( h \) is characterized by four parameter weight matrices \( W_h, W_h, W_h, W_h \) and \( W_h \). The computation involved in each head \( h \) is represented by the DAG on the right hand side of Fig. 10 (the same DAG used in the motivation example in Section 2). It can be observed that the sentence vector \( X \) typically undergoes 3 parallel GEMM transformations with the weight matrices \( W_h^Q, W_h^K, W_h^V \) to generate Query \( Q \), Key \( K \) and Value \( V \) matrices respectively. Using \( Q \) and \( K \), as depicted in Fig. 10 the matrices \( A = QK^T \) followed by \( B = \text{Softmax}(A) \) are computed where \( \text{Softmax} \) represents a normalized exponential function \cite{14}. The contextual embedding matrix \( C = [h_1^T, h_2^T, \ldots, h_n^T] \) is computed as \( C = BV \). Finally, the output \( Z_h \) is obtained by the GEMM operation \( CW_h \). The outputs of each of these heads are concatenated to produce the final contextual embeddings for the sentence. The output of each layer is passed as input to the following layer similar to any neural network pipeline.

In contrast to RNNs, the transformer architecture offers ample scope for parallelization. A single transformer layer typically comprises, 8 or 16 heads and thus a maximum of \( 16 \times 3 = 48 \) matrix computations can execute in parallel given sufficient hardware resources. Since the operations in each of the layers are similar in nature, we validate our
We execute the clustering scheme for each of the transformer DAGs by varying the number of command queues $q_{cpu} \in [0, 5]$ and $q_{gpu} \in [0, 5]$ for our target platform and by varying the number of task components mapped to the CPU, $h_{cpu} \in [0, H]$. The remaining $H - h_{cpu}$ task components are mapped to the GPU device. Given this, let us denote an architecture mapping configuration for the clustering scheme as $mc = (q_{gpu}, q_{cpu}, h_{cpu})$. We have observed from our experimental results that increasing beyond 5 command queues for the CPU and GPU device does not improve execution time. This may be attributed to the overhead of managing multiple command queues by the OpenCL runtime system. The clustering scheme can also emulate static coarse-grained scheduling decisions if the entire DAG is mapped to the GPU device using a single command queue i.e. $mc = (1, 0, 0)$. We consider clustering with this architecture-mapping configuration to be the default coarse-grained scheduling scheme against which we shall compare how fine-grained decisions fare for the same task component partitioning $T$.

For each DAG distinguished by the number of heads $H$, the best mapping configuration for clustering is the one which gives the best speedup with respect to time taken by the DAG to execute in its default configuration. We profile a total of $(H + 1) \times q_{cpu} \times q_{gpu}$ such mapping configurations for each transformer DAG with $H$ heads and highlight our observations in Fig. 11. The x-axis denotes the total number of heads for the transformer. The y-axis represents the speedups obtained for the best configuration for each DAG over the default configuration. Each point is labeled by the $q_{gpu}, q_{cpu}$ tuple corresponding to the best configuration. We further note that for DAGs with number of heads upto 10 (region to the left of the dotted line), $h_{cpu}$ is 0. For DAGs having number of heads greater than 10 (region to the right of the dotted line), we have $h_{cpu} = 1$.

Thus, for DAGs with $H \in [1, 10]$, we observe that the best configuration only differs from the default configuration with respect to the $q_{gpu}$ parameter. All the task components of the DAGs are scheduled to the GPU with the only difference being the number of command queues assigned to each component. The key observation in this region is that the transformer shows a clear speedup of about $15\% - 17\%$, if fine-grained scheduling is enabled leveraging multiple command queues. This highlights the effectiveness of automated fine-grained scheduling which our framework offers.

For $H \in [11, 16]$, we observe that scheduling one of the task components of the DAG to the CPU device yields the maximum speedups. We also observe a jump in the relative speedup values as compared to the DAGs with $H <= 10$. This is because apart from taking fine-grained scheduling decisions for the GPU device, we are also undertaking certain fine-grained scheduling decisions for the CPU device as well. This results in better extraction of application level-parallelism since mapping a task component to the CPU results in lesser contention for the GPU device. However we
observe with $H > 10$, it is meaningful to migrate only one head to the CPU device for further speedups. This makes sense since i) the GPU has an order of magnitude number of processing elements greater than the CPU under consideration, ii) the kernels selected are optimized for GPUs rather than CPUs and iii) the CPU device is heavily engaged in setting up command queues and issuing directives to the devices in the heterogeneous platform. Mapping more than 1 head for execution on the CPU actually takes more time to execute than that of mapping the remaining heads to the GPU device.

The current experiment highlighted how the clustering scheme has been envisaged for the transformer DAG by considering specific DAG head mappings along with a choice of command queues and devices. Our next two categories of experiments consider comparing our static scheme with traditional implementations of coarse-grained heterogeneous scheduling policies like Eager and HEFT available in the StarPU framework [5] which are inherently dynamic in nature i.e. kernel-device mappings are decided only at runtime.

**Experiment 2: Clustering vs Eager Execution:** We have implemented a simplistic eager execution based scheduling algorithm in our framework inspired from StarPU. In this strategy, we specify every kernel in the DAG as a separate task component and each device to use only one command queue. The select routine is modified to i) choose task components based on the bottom level ranks discussed earlier and ii) select any device $d$ that is available at runtime irrespective of the individual device preferences of the kernel. The eager scheduling scheme supports only coarse-grained scheduling since it implements single command queue per device. Furthermore, since each task component is a kernel here, an explicit callback is required for every kernel to notify the host that it has finished execution.

For a comparative evaluation of this dynamic scheme with clustering, we generate a set of input DAGs by keeping the number of heads $H$ fixed to 16 and by varying the size parameter $\beta$ from 64 to 512 in powers of 2. We profile each such input DAG, using both eager scheduling and clustering schemes for all possible mapping configurations. We compute the speedups of execution times taken by clustering based scheduling for the best mapping configuration over that of eager and highlight them in Figure 12(a). The x-axis represents the size of the transformer head ($\beta$) for each DAG and the y-axis represents the speedup values. Each point in the plot is again labelled by the tuple $g_{cpu}, g_{gpu}$ used by the best mapping configuration for the clustering scheme. The third element of the best configuration $h_{cpu}$ was found to be 1 for each $\beta$. It can be observed that clustering outperforms eager by a considerable margin. The comparison in Fig. 12 brings out the advantage of static fine-grained scheduling as supported by our framework.

**Experiment 3: Clustering vs HEFT:** Our final experiment considers the standard Heterogeneous Earliest Finishing Time First algorithm [16] heft. Similar to eager, the scheduling heuristic heft assumes each task component to represent one kernel and sets up one command queue for each device. The select routine is modified to i) choose the kernel $k$ with the maximum bottom level rank and for ii) choose the device $d$ on which $k$ can execute with the earliest finishing time (EFT). Assuming execution times for kernels are available via prior profiling, EFT of $k$ executing on a device $d$ is computed as the sum of its execution time and the execution time of a kernel $k'$ currently executing on $d$. Considering the same set of input DAGs used in Experiment 2, we plot the speedups of the best configurations of the clustering scheme over the heft scheme in Fig. 12(b). As expected, heft performs better than eager due to the added knowledge of earliest finishing times for each task. However, heft being implemented as a dynamic coarse-grained scheduling scheme is short sighted and fails to exploit concurrency aware scheduling decisions undertaken by clustering.

**Comparative Evaluation:** One can also observe from the speedup values from Experiments 1, 2 and 3 that both heft and eager perform poorly when compared to both coarse-grained and fine-grained versions of static clustering. We explain the reasons behind this by performing a deeper analysis of the scheduling decisions taken for a DAG with $H = 16$ and $\beta = 512$ using the Gantt charts for eager heft and clustering depicted in Fig. 13. The primary reason for the poor performance of eager maybe attributed to the greedy selection of devices based on runtime availability rather than kernel preference. As a consequence, one can observe from Fig. 13(a), that multiple GEMM kernels have been scheduled on the CPU, thereby taking a significantly larger amount of time. Even though GPU bound GEMM kernels take less time, the execution of the callbacks are delayed since the CPU is being heavily used for the GEMM computation. This is evident from the gaps between the kernels scheduled on the CPU device. Since the callback function is initiated using a separate thread for notifying the host, it might happen that either i) the master thread running the schedule routine is swapped out of main memory at that point of time or ii) there are not enough resources to spawn the thread for running the callback function. As a result, the read callbacks wait before updating $F$ and $A$ to allow progress. In contrast, we observe there are little to no gaps between kernels scheduled on the CPU device. This indicates that once the ndrange callback for a kernel executing on the CPU device finishes, it immediately updates $A$. Consequently, the scheduling algorithm continues to dispatch kernels to the available CPU, thus causing starvation of the GPU resource.

In contrast to eager scheduling, it may be observed from Fig. 13 that heft exclusively uses the GPU for the GEMM kernels and is thus approximately $2A \times$ faster than eager. But, heft fundamentally being a dynamic coarse-grained scheduling policy like eager still relies on read callbacks for dispatch decisions for every kernel. The successive gaps introduced between each kernel execution in the DAG results...
in a considerable slowdown.

Fig. 13: Gantt charts for different scheduling algorithms

For our clustering scheme we may observe from Fig. 13 (c), that kernels start executing much later when compared to kernels being scheduled in the other schemes. This may be attributed to the fact, that our framework sets up the command queues first with operations pertaining to all kernels in a task component before actually dispatching the kernels to their respective devices. Another interesting observation in Fig. 13 (c) is as follows. Since, the task component partitioning $T$ ensures that there exists no inter edge buffers in $END(T)$ for each task component $T$ in the clustering scheme, there is no explicit requirement of callbacks which was the primary bottleneck in the other dynamic schemes. As a result, there exists no gaps between the execution of any two successive kernels in the DAG in Fig 13. This holds true for the default coarse-grained configuration of clustering as well, since the task component partitioning set $T$ is same as that of the fine-grained configuration. The definition of $T$ coupled with intelligent use of command queues by the framework for clustering helps in avoiding these runtime delays and results in a considerable speedup when compared to dynamic scheduling decisions employed by eager and heft. The framework has been open-sourced in Github with scripts for running all the experiments.

6 RELATED WORK

Given the rich API support of CUDA and OpenCL, several frameworks have emerged over the last few years with the objective of providing user friendly solutions for development of data parallel applications. Frameworks based on CUDA include OpenACC [17] and HiCUDA [18] which supports a directive based programming model where relevant annotations in sequential C programs generate data parallel CUDA code for execution on the GPU. Frameworks such as GMAC [19] ease programming by not requiring explicit memory operations while designing CUDA applications. Several OpenCL based frameworks have also been envisioned in the past decade for general purpose heterogeneous programming. The most notable framework in this regard is SkelCL [20] which offers support for designing algorithmic skeletons (higher order functions such as map, reduce, scan etc) which can be leveraged for implementing data parallel kernels. Note, the primary approach of this work is complementary in the sense that they focus on rapid kernel development, while our work focuses on scheduling optimizations on target heterogeneous architectures. The most recent work reported in [3] proposes a novel set of APIs for specifying dependencies of a DAG thus easing application development, but does not have explicit algorithm support for scheduling. The VirtCL framework [21] provides an abstraction layer between the programmer and the OpenCL runtime system acting as a hypervisor for scheduling multiple OpenCL applications. The abstraction framework leverages a profile driven history based scheduling scheme for dispatching OpenCL kernels on multiple devices. However, a major limitation for VirtCL is that it cannot operate with devices belonging to different platforms. Our framework in contrast is suited to work with different OpenCL platforms and supports both static and dynamic scheduling approaches for mapping OpenCL kernels. There also exists frameworks such as SnUCL [22], VOCL [23], MultiCL [6] etc. that extend upon the OpenCL runtime API which allows OpenCL applications to leverage devices belonging to heterogeneous clusters. While SnUCL and VOCL have no explicit algorithm support for scheduling, MultiCL relies on coarse-grained scheduling decisions with a focus on data partitioning across multiple devices. Also, since these APIs are extensions of OpenCL, one cannot bypass the requirement of complex host program development for implementing data parallel applications.

StarPU [5], [24] is a unified scheduling framework allowing users to design and experiment scheduling policies for both CUDA and OpenCL applications. The work reported in [4] presents an unified OpenCL implementation called SOCL which directly extends StarPU for exclusively supporting execution of OpenCL workloads across multiple devices. Both SOCL and StarPU rely on prior profiling information for each task on each device for constructing a performance model to be used for scheduling decisions and have algorithm support for coarse-grained scheduling decisions. In contrast, to the best of our knowledge, our framework is possibly the first to present an automated mechanism for enforcing fine-grained scheduling decisions which are relatively more adept in exploiting concurrency in OpenCL applications.

7 CONCLUSION

We propose a platform agnostic scheduling framework that not only enables users to design HPC applications with ease, but also performs optimized scheduling decisions that exploit both application-level and platform-level concurrency. For an application with ample scope for concurrency, we have observed that rather than relying on traditional coarse-grained scheduling decisions, implementing fine-grained scheduling policies using PySchedCL where the user specifies an intuitive task component partitioning $T$ after examining the structure of a DAG application results

1. https://github.com/anighose25/pyschedcl-concurrent
in significantly better execution times. Future work entails investigating sophisticated low-level scheduling approaches such as sub-kernel partitioning \[9\], \[25\] at the work-item level for effective interleaving of concurrent kernels. Such approaches coupled with Machine Learning assisted control theoretic scheduling solutions \[26\] shall be used to develop an auto-tuning framework on top of \textit{PySchedCL} which would automatically determine given an application-architecture pair, the optimal allocation of command queues across devices in the platform.

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