Development of a Reliable High-Performance WLP for a SAW Device

Zuohuan Chen and Daquan Yu *

School of Electronic Science and Engineering, Xiamen University, Xiamen 361005, China; xmuuchenzh@stu.xmu.edu.cn
* Correspondence: yudaquan@xmu.edu.cn

Abstract: In this paper, we present wafer-level packaging technology for surface acoustic wave (SAW) filters with higher long-term reliability and better electrical performance. This article focuses on the package structure, fabrication processes, and reliability for the SAW filter wafer-level package (WLP). The key processes, including cavity wall (CW) dam formation through non-photosensitive film vias development using a laser drilling process, a redistribution layer (RDL), and ball-grid array formation are developed. In addition, a numerical study based on the finite element model has been conducted to analyze the stress distribution of Cu RDL traces. In addition, the CW dam and the roof layer are covered with polymer, which solves the delamination problem between the CW dam and the substrate. Meanwhile, after practical verification, the SAW filter WLP was resistant to encapsulating pressure using a high elastic modulus capping material, which solved the collapse problem. Additionally, a comparison of the RF filter package's electrical performance following the preconditional level 3 and unbiased highly accelerated stress test revealed no differences in insertion attenuation across the passband (<0.2 dB, standard value: 1 dB). The final packages passed the reliability tests in the field of consumer electronics.

Keywords: surface acoustic wave filter; wafer-level packaging; laser drilling; finite element model; reliability

1. Introduction

The recent advent of 5G networks has necessitated the assistance of acoustic wave device volume creation. Acoustic wave devices, such as surface acoustic wave (SAW) and bulk acoustic wave (BAW), are primarily utilized in the front ends of current mobile transceiver systems to filter out desirable frequencies. Many specialists have worked to reduce the size or number of SAW/BAW devices or to eliminate them entirely through design or packaging changes [1–3]. However, there are currently no competitive devices that offer the same performance at the same size and price. According to Qorvo’s estimates, the market for radio frequency (RF) filters in mobile phones is worth USD 12.83 billion. This unlikely to decrease. This paper aims to capture the rationales behind these approaches to new packaging approaches, such as novel topologies, new materials, and enhanced simulation modeling achieving a higher performance and lower cost of SAW devices [4–6]. A series of evaluations and investigations into the development of high-performance wafer-level packaging (WLP) for SAW devices are offered in order to achieve this goal.

1.1. Historical View of SAW Device Package

SAW device packaging began with a hefty ceramic container that was unsuitable for mobile radios. SAW packages were primarily wire-bonded ceramic, metal, and plastic containers until 2001. Then, EPCOS introduced the chip-sized SAW package (CSSP) [2,3]. Flip-chip technology was employed to replace wire bonding in this package form. The
flip-chip technique connects the chips to a high-temperature confirmed multilayer ceramic (HTCC) substrate, which is then coated by polymer lamination, which is a characteristic packaging method utilized only in low-frequency devices [2,3].

WLP is the next step in miniaturization and cost reduction [7–14]. In WLP, one or two organic or inorganic layers on top of the piezoelectric crystal, such as a lithium (LiTaO$_3$, LT) piezoelectric substrate, form cavities above the active portions of the chip, which can protect the susceptible SAW device structure from probable injuries, such as dust or corrosion. Different processes, such as the production of polymer caps utilizing a sacrificial layer or dry film resist lamination techniques, are used to create these hollow structures [9–11]. The SAW devices are also sealed with a stiff cap structure using wafer-to-wafer or chip-to-wafer bonding technologies. The cap layer made of glass or polymer film with via interconnects were formed to contact the external circuits and the chip’s pads [15,16]. Partially limiting the interdigital transducer (IDT) regions while leaving the SAW devices’ IOs available is more cost-effective. A self-packaged SAW device using a boundary acoustic wave, which does not require cavities or a particular processing approach for making sturdy packages, is even better from a functional standpoint. However, because it uses Au interdigital transducers deposited on LiNbO$_3$ substrates, which has a greater cost, this filter is not advantageous in terms of cost and filter qualities. Typically, these devices operate in the mobile environment at frequencies ranging from 1040 to 1120 MHz, which do not match the high-frequency requirement.

Because the range of existing technologies is so broad, there is no perfect solution in terms of key evaluating indicators such as low cost, process risk, reliability performance, degree of miniaturization, and compatibility with various microelectromechanical systems (MEMS) and complementary metal oxide semiconductor (CMOS) technologies on a wafer [17,18]. We aimed to create a reliable high-performance WLP for SAW device processing flow in this study, with a particular focus on keeping the low cost and post-wafer-level process flow as short as possible to reduce the chance of process failure. The process of developing a dependable high-performance SAW device WLP is described in the following paragraphs. We employed devices developed for the B41 band application with operation frequencies ranging from 2.496 GHz to 2.690 GHz as SAW filter test devices. SAC solder balls were used in the final SAW device packaging, which was mounted to external circuitry, like a circuit board; it was flipped over, so that its top side faced down and its pads were aligned with matching pads on the external circuit; then, the solder was reflowed to complete the interconnect. In Section 1, we present an overview of packaging technologies and propose various SAW filter WLP configurations to fit various application scenarios. Section 2 describes the WLP process flow and common failure mechanisms, which include interfacial delamination and redistribution layer (RDL) fracture. Section 3 builds a wafer-level and a single-die simplified finite element (FE) model for von Mises stress and collapse prediction. Both FE models were shown to be accurate through theoretical calculations and actual experimental results’ comparison. We presented an in-depth look at the creation and reliability enhancement of the wafer-level molded package based on the proposed packaging models for the diverse structural design of the SAW device. The packages were tested for reliability, as detailed in Section 4, and all of them passed. Finally, in Section 5, some observations are made.

1.2. SAW Device Package Design

In this paper, the SAW filter with a size of 1.58 mm $\times$ 1.18 mm was packaged. There were eight pads on the front side, and each pad had a size of 70 $\mu$m $\times$ 70 $\mu$m. The WLP structure of the SAW device is presented in Figure 1.

As shown in Figure 1, the SAW filter package consisted of a SAW filter substrate with IDTs and pads, a CW dam (also called a wall layer), non-photosensitive dry film capping (also called a roof layer), an RDL, and solder ball. There were three metal layers in the package; the first layer was metal 1 (M1), the second layer was the through film vias (TFV), used to connect the top and bottom metal, and the third layer was M2. The
top and bottom diameters of the CW dam and roof layer were 50 and 70 μm (dimensional tolerance: ±3 μm), respectively. The thickness of the CW dam was 15 μm, while the non-photosensitive dry film layer was 20 μm thick. The solder balls were 110 μm in diameter and 70 μm in height, respectively. Meanwhile, cavities with a size of 980 μm × 320 μm in a thin-film capping acoustic package were designed.

![Diagram of SAW filter WLP structure](image)

**Figure 1.** (a) The schematic of the cross-sectional SAW filter WLP structure; (b) the 3D WLP SAW filter’s top view following BGA creation.

2. Process Flow of the SAW Device’s WLP and the Typical Failure Mode

This WLP technique is a real chip-scale packaging method that enables packages to maintain the same size as a die. A new efficient WLP technique created a gas-filled cavity structure for SAW filter packages, using non-photosensitive film lamination technology, with high strength and a high elastic modulus [7–14,19].

2.1. Process Flow of SAW Device WLP

The process flow of the SAW device WLP is depicted in Figure 2, and the details are listed as follows: (1) we prepared a 220 μm SAW filter substrate wafer with IDTs and an M1 layer and used the lithography process to make a CW dam layer. (2) A non-photosensitive dry film was laminated on the CW dam layer using a roller lamination method to make an individual cap for each IDT. As shown in Figure 3, we used laser drilling to drill TFVs with different diameters [20,21]. Meanwhile, no delamination of the roof layer in the top of the CW dam layer was found from scanning electron microscopy (SEM). The non-photosensitive dry film was a non-hermetic material; the inside of the microcavity had the same pressure as the outside of the device after forming the cavity wall. (3) Physical vapor deposition (PVD) and the RDL process was used to fill Cu into TFVs and form the M2 layer. (4) The solder balls were dropped on the M2 layer by stencil printing and a reflow process. The diameter and height of the solder ball were 110 μm and 70 μm, respectively. The wafer was diced into individual packages after the final solder-balling procedure.

2.2. The Experimental Results of Typical Failure Mode

The reliability of the SAW filter package is a major concern for the RF front-end passive devices. Many types of failures may happen during assembly, qualification tests, and operation. Typical failure modes are shown in Figures 4 and 5, such as an RDL crack in the TC test and capping layer collapse of the package. Meanwhile, the RDL structure may affect the thermomechanical performance of the solder joints or SAW devices, in severe cases, thus causing the entire device structure to be destroyed. All of these failures will cause pollution or damage to the IDTs.
2.2. The Experimental Results of Typical Failure Mode

The reliability of the SAW filter package is a major concern for the RF front-end passive devices. Many types of failures may happen during assembly, qualification tests, and operation. Typical failure modes are shown in Figure 4 and 5, such as an RDL crack in the TC test and capping layer collapse of the package. Meanwhile, the RDL structure may affect the thermomechanical performance of the solder joints or SAW devices, in severe cases, thus causing the entire device structure to be destroyed. All of these failures will cause pollution or damage to the IDTs.

3. FE Model of a SAW Filter’s WLP

3.1. Single-Die FE Model to Solve the RDL Crack Failure Mode

To investigate the stress distribution of Cu RDL traces, an FE model was constructed to calculate the maximum primary stress at each phase of the manufacturing process flows, focusing on the different Cu thicknesses of the vias sidewall at the steady-state cooling process (temperature conditions varied from 260 °C to 22 °C) to achieve high dependability [22,23]. The package structure model was developed and simplified into four parts in this model, as illustrated in Figure 6, comprising the RDL, roof layer, CW dam layer, and SAW device substrate (from top to bottom), and the material properties are listed in Table 1.

Figure 2. The process flow of the 3D WLP package.

Figure 3. Top view of the opening size of the CW dam and roof layer.

Figure 4. SAW filter package failure mode. (This refers to an RDL crack).
In general, a mismatch in the coefficient of thermal expansion (CTE) between different materials in a WLCSP structure can induce high thermal stress. Because the performance of the package may be impacted by the design structure and material characteristics, such as the thickness of the vias sidewall Cu plating and material properties of both the CW dam and roof layer, it is necessary to investigate the impact of these aspects.

To ensure reliability, for a SAW filter WLP, it was necessary for us to investigate the causes of typical failure models and optimize the package structure to meet the reliability requirements of consumer electronics.

3. FE Model of a SAW Filter’s WLP

3.1. Single-Die FE Model to Solve the RDL Crack Failure Mode

To investigate the stress distribution of Cu RDL traces, an FE model was constructed to calculate the maximum primary stress at each phase of the manufacturing process flows, focusing on the different Cu thicknesses of the vias sidewall at the steady-state cooling process (temperature conditions varied from 260 °C to 22 °C) to achieve high dependability [22,23]. The package structure model was developed and simplified into four parts in this model, as illustrated in Figure 6, comprising the RDL, roof layer, CW dam layer, and SAW device substrate (from top to bottom), and the material properties are listed in Table 1.

Figure 5. Collapse of the SAW WLP package.

Figure 6. The single-die FE modeling.
Table 1. Material properties of the two single-die models.

| Items              | Young Modulus | Poisson Ratio | CTE            |
|--------------------|----------------|---------------|----------------|
| SAW device substrate | 230 Gpa        | 0.22          | 16.1 ppm/°C    |
|                    |                |               | 4.1 ppm/°C     |
| Cavity wall layer  | 4.4 Gpa        | 0.34          | 65 ppm/°C      |
| Roof layer         | 9 Gpa          | 0.34          | CTE1: 18 ppm/°C (25–150 °C) |
|                    |                |               | CTE2: 45 ppm/°C (150–240 °C) |
| Cu                 | 119 Gpa        | 0.326         | 17.5 ppm/°C    |

The Cu thickness of the via sidewall was adjusted to 2 µm, 8 µm, and filled in the simulation setting. Temperature conditions were varied from 260 °C to 22 °C. Then, 260 °C was chosen as the reference temperature. Figure 7 depicts the stress distribution. The max stresses for the via sidewall Cu thickness at 2 µm, 8 µm, and filled were 416.07 MPa, 363.84 MPa, and 350.45 MPa, respectively, which means the stress decreased as the Cu thickness of the via sidewall increased, as presented in Figure 7 and Table 2. In a followup design structure, the full-via Cu electroplating process was performed.

Figure 7. Stress distribution of the thickness of the Cu plating at 8 µm during the cooling-down stage of the curing process.

Table 2. Statistics of the stress value during the different thicknesses of Cu plating.

| Cu Thickness | Stress Point (MPa) | Ratio |
|--------------|--------------------|-------|
| 2 µm         | 416.07             | 1.00  |
| 8 µm         | 363.84             | 1.14  |
| filled via   | 350.45             | 1.19  |

3.2. Effect of Geometric Parameters on Stress Distribution

It is essential to thoroughly research the geometric characteristics and material parameters, since they might have an impact on the dependability of the SAW filter package. In Figure 8, we show the typical wall-layer delamination in the bottom of the pad after the temperature cycling test (TCT). The performance of high-temperature composites can be significantly affected by the presence of residual stresses. These stresses arise during the cooling processes from fabrication to room temperature due to a mismatch in the CTE of the various materials. This will cause wall delamination and an RDL crack.
After the cavity actors in depth. We find that the maximum equivalent stress appears at the bottom edge of the wall layer. Meanwhile, we compared the unimproved and improved SAW filter WLP, and the equivalent (von Mises) stresses were 154.06 MPa and 74.487 MPa, respectively (the maximal stress is marked in Figure 10), which means the maximum stress value decreased by 51.65% on average.

Figure 8. SAW filter package failure modes after TC test. (The arrow, in this Figure, refers to a magnified image of the delamination between the wall layer and substrate).

A greater comprehension of the adhesion processes will accelerate the development of microelectronic and SAW filters in order to increase the dependability performance. As a typical wall-layer delamination can be influenced by geometric parameters, it is necessary to investigate those factors in depth. Figure 9 shows the cross-sectional structure of the improved SAW filter WLP. The most significant feature is that polymer materials were added to the SAW device to give extra protection to the exposed bard wall and roof layer on the sidewall. In this way, smaller peeling stress between the wall layer and SAW filter substrate was obtained without wall layer delamination.

Figure 9. Structural comparison of (a) top-side molded WLP with (b) typical fan in SAW device package.

Figure 10 shows the maximal equivalent stress value distribution on the bottom surface of the wall layer. We find that the maximum equivalent stress appears at the bottom edge of the wall layer. Meanwhile, we compared the unimproved and improved SAW filter WLP, and the equivalent (von Mises) stresses were 154.06 MPa and 74.487 MPa, respectively (the maximal stress is marked in Figure 10), which means the maximum stress value decreased by 51.65% on average.
After the cavity was created, epoxy molding compound (EMC) was applied to the whole device, and then a consistent load was placed on top of the EMC.

3.3. Deflection Prediction of Different Cavity Sizes

In the case of the package capping layer collapse, a non-photosensitive film with high strength and high elastic modulus has become more and more attractive for the wafer-level SAW filter packages because it exhibits excellent pressure capability.

We developed a deflection prediction model to simulate the collapse of the package capping layer in order to forecast the cavity deflection under pressure [5,24]. A single SAW filter WLP collapse model and its boundary conditions are shown in Figure 11. The restrained surface was stationary (it means that \( y = 0 \)). After the cavity was created, epoxy molding compound (EMC) was applied to the whole device, and then a consistent load was placed on top of the EMC.

![Collapse model and boundary conditions.](image)

**Figure 11.** Collapse model and boundary conditions.

Through discussion of the WLP structure of the SAW filter, the maximum collapse of the cavity with a size of 980 \( \mu m \times 320 \mu m \) in the device was simulated. This was performed by studying the collapse calculation of the device using the finite element simulation model. Following simulation validation, Figure 12 shows that the quantity of collapse at a higher mold pressure of 6.2 MPa was approximately 1.32 \( \mu m \). After practical verification, the highest amount of collapse in the center of the cavity was estimated to be around 5.4 \( \mu m \) at the mold pressure of 6.2 MPa, as shown in Figure 13. At this point, the cavity’s height was 9.6 \( \mu m \).
Figure 12. The collapse result after the roof layer process obtained by applying 6.2 MPa pressure to the FE model.

Figure 13. Experimental results of collapse test by applying 6.2 MPa pressure. (a) Schematic of molding pressure test; (b) indicates the SEM image of the SAW device molding pressure test; (c–e) indicate the degree of collapse of the cavity at the left, middle and right positions, respectively.

The difference between the measured and simulated results was small. In the actual test of the cavity collapse resisting molding pressure, there were also factors such as the error of measurement (tolerance range: ±2 μm) and substrate warpage, which could not be simulated in the simulation software, and the simulation results were only used as a directional guide. The collapse issue brought on by the SAW filter WLP’s encapsulation pressure was resolved by using a non-photosensitive dry film with a high modulus of elasticity as a capping layer, which also lowered the failure risk of devices and modules.

4. Reliability Evaluation

SAW filters and BAW filters are examples of electronic and RF equipment that are used in a variety of mechanically and thermally demanding environments. We carried out typical reliability testing to certify the SAW filter’s WLP, as shown in Table 2. Before reliability testing, preconditioning was conducted to simulate the effects of the board assembly. The samples went through a 192-h soak procedure at 30 °C and 60% relative
humidity, as well as a 24-h baking process at 125 °C. The samples were then reflowed three times by a temperature profile with a 260 °C peak. The unbiased highly accelerated stress test (uHAST) temperature storage test at 130 °C for 96 h was carried out for reliability evaluation with the goal of evaluating dependability. The Joint Electron Device Engineering Council (JEDEC) standards were referenced in the test circumstances.

Each reliability test used 30 samples. In Table 3, the dependability findings are summarized. There was no variation in the insertion attenuation across the passband (<0.2 dB) for the SAW filter package following the uHAST test, as shown in Figure 14 [3]. The chosen samples were characterized and cross-sectioned by SEM after the reliability test and the subsequent electrical testing, as shown in Figure 15. No delamination was found between the wall layer and the SAW filter substrate after uHAST 96-h. There was no crack at the interface between the bottom of the via and the Al pad, and the RDL profile was normal, as it had been before the reliability test.

Table 3. Items and results of reliability test.

| Items    | Conditions                | Failure Rate (%) | Result |
|----------|---------------------------|------------------|--------|
| Pre-Con L3 | Bake 125 °C/24 H          | 0.00             | Pass   |
|          | Soak 30 °C/60%/192 H      | 0.00             | Pass   |
|          | Reflow 260 °C (+5/−0) 3×  | 0.00             | Pass   |
| uHAST    | 130 °C/85% RH, 96 H       | 0.00             | Pass   |

Figure 14. Measurement results of frequency response before and after reliability test.
Figure 15. SEM image of the RDL of a single package after uHAST 96 h. (a) Cross-sectional picture of the SAW Device WLP with solder ball. (b) Interconnection structure of the chip’s pad and the solder ball by TFV. (c,d) indicate the interconnection structure on the left and right side of the chip’s pad, respectively.

5. Conclusions

In this paper, a construction procedure for a 3D WLP for a SAW filter using non-photosensitive dry film lamination and laser drilling technologies was presented. Due to its effective packaging process, it can provide a low-cost alternative to a conventional packaging method for smaller SAW filter applications. The main conclusions are described as follows.

1) A wafer-level lamination process was conducted on the SAW filter substrate with the CW dam layer together before the electrical interconnection process. Laser drilling was used to form the connection vias, which was characterized by a gradual increase in diameter from the bottom to the top of the TFVs, and the side walls were smooth without steps.

2) Parameters, such as material properties and geometry, affect the maximum stress of the package significantly. Following practical verification, the cavity collapse amount was projected to be about 6.6 µm at a larger size of 980 µm × 320 µm, resolving the collapse problem caused by the encapsulating pressure of the SAW filter WLP. In terms of the effect of the geometric parameters on stress distribution, by comparing the top-side molded with the conventional SAW filter WLP, the maximum von Mises values were 74.487 MPa and 154.06 MPa, respectively, with a 51.65% reduction.

3) After Pre Con L3 and uHAST 96-h, no electrical breakdown was seen during the reliability tests. The results show that the proposed SAW filter package based on 3D WLP technology is reliable for large-scale industrial manufacture. We infer from this that our technique can significantly enhance the development and use of consumer market band applications.

6. Patents

Zuohuan Chen, Daquan Yu, Jiang Feng, et al. A Wafer-level packaging structure and method for filter. CN Patent 202210528805.8. 16 May 2022.
Author Contributions: Conceptualization and patent, Z.C. and D.Y.; investigation, Z.C.; package structure design and fabrication, Z.C. and D.Y.; reliability analysis, Z.C.; writing—original draft preparation, Z.C.; writing—review and editing, D.Y.; supervision, D.Y.; project administration, D.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the National Natural Science Foundation of China (Grant No. 61974121) and the Science and Technology Major Project of Xiamen City (Grant No. 3502Z20201004).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to thank Xiamen Sky Semiconductor Technology Co., Ltd. for their strong support. They would also like to thank Wenbiao Ruan, Feng Jiang, Mingchuan Zhang, Heng Wu, and Jiqin Zhang for their constructive contributions.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Watanabe, A.O.; Ali, M.; Sayeed, S.Y.B.; Tummala, R.R.; Pulugurtha, M.R. A Review of 5G Front-End Systems Package Integration. IEEE Trans. Compon. Packag. Manuf. Technol. 2021, 11, 118–133. [CrossRef]
2. Gong, S.; Lu, R.; Yang, Y.; Gao, L.; Hassanien, A.E. Microwave Acoustic Devices: Recent Advances and Outlook. IEEE J. Microw. 2021, 1, 601–609. [CrossRef]
3. Hagelauer, A.; Fattinger, G.; Ruppel, C.C.W.; Ueda, M.; Hashimoto, K.-Y.; Tag, A. Microwave Acoustic Wave Devices: Recent Advances on Architectures, Modeling, Materials, and Packaging. IEEE Trans. Microw. Theory Tech. 2018, 66, 4548–4562. [CrossRef]
4. Chen, Z.; Yu, D.; Zhang, M.; Jiang, F. Development and Reliability Study of 3-D Wafer Level Packaging for SAW Filter Using Thin Film Capping. IEEE Trans. Compon. Packag. Manuf. Technol. 2021, 11, 1047–1054. [CrossRef]
5. Chen, Z.; Yu, D.; Jiang, F. Development of 3-D Wafer Level Packaging for SAW Filters Using Thin Glass Capping Technology. IEEE Trans. Compon. Packag. Manuf. Technol. 2022, 12, 375–381. [CrossRef]
6. Chen, Z.; Yu, D.; Jiang, F. A Wafer-Level Packaging Structure and Method for Filter. CN Patent 202210528805.8, 16 May 2022.
7. Lim, J.-H.; Hwang, J.-S.; Kwon, J.; Ham, S.-J.; Kim, T.H.; Jeung, W.K.; Yang, S.J.; Choi, S.M.; Park, J.H.; Kim, W. 6B-6 An Ultra Small SAW RF Filter using Wafer Level Packaging Technology. In Proceedings of the 2006 IEEE Ultrasymposium Symposium, Vancouver, BC, Canada, 3–6 October 2006; pp. 196–199. [CrossRef]
8. Zoschke, K.; Wegner, M.; Lopper, C.; Klein, M.; Gruenwald, R.; Schoenbein, C.; Lang, K.-D. LiTaO$_3$ Capping Technology for Wafer Level Chip Size Packaging of SAW Filters. In Proceedings of the 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 31 May–3 June 2016; pp. 889–896. [CrossRef]
9. Kim, T.H.; Jeung, W.K.; Yang, S.J.; Choi, S.M.; Park, S.W.; Kim, H.H.; Ha, J.; Park, M.J.; Kao, S.; Hong, J.; et al. Miniaturization and Optimization of RF SAW Filter Using Wafer Level Packaging Technology. In Proceedings of the 57th Electronic Components and Technology Conference, Las Vegas, NV, USA, 29 May–1 June 2007; pp. 574–579. [CrossRef]
10. Pitschi, E.; Bauer, C.; Koch, R.D.; Wagner, K.C. Approaches to wafer level packaging for SAW components. In Proceedings of the 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, WA, USA, 2–7 June 2013; pp. 1–3. [CrossRef]
11. Ham, S.-J.; Jeong, B.-G.; Lim, J.-H.; Jung, K.-D.; Baek, K.-D.; Kim, W.-B.; Moon, C.-Y. Characterization and Reliability Verification of Wafer-Level Hermetic Package with Nano-Liter Cavity for RF-MEMS Applications. In Proceedings of the 57th Electronic Components and Technology Conference, Sparks, NV, USA, 29 May 2007–1 June 2007; pp. 1127–1134. [CrossRef]
12. Park, S.W.; Hong, J.P.; Kim, T.H.; Yang, S.J.; Ha, J.; Park, S.W.; Kweon, Y.D.; Yi, S. Fabrication and optimization of wafer level SAW filter package using laser via drilling. In Proceedings of the 2nd Electronics System-Integration Technology Conference, Oulu, Finland, 17–20 June 2007; pp. 1–5. [CrossRef]
13. Feiertag, G.; Krüger, H.; Bauer, C. Surface acoustic wave component packaging. In Proceedings of the European Microelectronics and Packaging Conference, Oulu, Finland, 17–20 June 2007; pp. 1–5.
14. Mandal, D.; Banerjee, S. Surface Acoustic Wave (SAW) Sensors: Physics, Materials, and Applications. Sensors 2022, 22, 820. [CrossRef]
15. Savornin, B.; Baillin, X.; Blanquet, E.; Nuta, I.; Patrice, D.S.; Nicolas, P.; Charvet, P.L.; Pornin, J.L. Outgassing characterization of MEMS thin film packaging materials. In Proceedings of the IEEE 63rd Electronic Components and Technology Conference, Las Vegas, NV, USA, 28–31 May 2013; pp. 1514–1518. [CrossRef]
16. Zhou, T.; Ma, S.; Yu, D.; Li, M.; Hang, T. Development of Reliable, High Performance WLCSP for BSI CMOS Image Sensor for Automotive Application. Sensors 2020, 20, 4077. [CrossRef]
18. Fukano, T.; Okubo, Y.; Nishii, J.; Obara, I. 2E-2 0806 SAW Filters Using Wafer Level Packaging Technology. In Proceedings of the IEEE Ultrasonics Symposium, New York, NY, USA, 28–31 October 2007; pp. 68–71. [CrossRef]

19. Qin, F.; Zhao, S.; Dai, Y.; Yang, M.; Xiang, M.; Yu, D. Study of Warpage Evolution and Control for Six-Side Molded WLCSP in Different Packaging Processes. IEEE Trans. Compon. Packag. Manuf. Technol. 2020, 10, 730–738. [CrossRef]

20. Hsiao, H.-Y.; Ho, D.S.W.; Chong, S.C.; Chai, T.C.; Schutzberger, D.; Oz, Y.; Amrani, G. Through Mold Via Development Using Laser Drilling Process for 3D Fan-out Wafer Level Package. In Proceedings of the IEEE 23rd Electronics Packaging Technology Conference (EPTC), Virtual, 1–3 December 2021; pp. 253–257. [CrossRef]

21. Hsiao, H.-Y.; Ho, D.S.W.; Lim, K.C.S.; Chong, S.C.; Chai, T.C.; Schutzberger, D.; Oz, Y.; Amrani, G.; Zhao, J.; Toh, J. Laser drilling and Plasma Cleaning Process for Blind Via Through Mold Interconnect. In Proceedings of the IEEE 22nd Electronics Packaging Technology Conference (EPTC), Singapore, 2–4 December 2020; pp. 14–18. [CrossRef]

22. Zhao, J.; Li, W.; Zhong, Y.; Yu, D.; Qin, F. Stress Issues in 3D Interconnect Technology Using Through Glass Vias. J. Mech. Eng. 2022, 58, 246–258. [CrossRef]

23. Zhao, J.; Qin, F.; Yu, D.; Chen, Z.; Zhao, S. Warpage Characteristic of Glass Interposer with Different CTE’s and Thickness. In Proceedings of the 22nd International Conference on Electronic Packaging Technology (ICEPT), Xiamen, China, 11–14 August 2021; pp. 1–4. [CrossRef]

24. Li, Q.; Goosen, H.; Van Keulen, F.; Van Beek, J.; Zhang, G. Assessment of testing methodologies for thin-film vacuum MEMS packages. Microsyst. Technol. 2009, 15, 161–168.