Truncating Wide Networks using Binary Tree Architectures

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Abstract

Recent study shows that a wide deep network can obtain accuracy comparable to a deeper but narrower network. Compared to narrower and deeper networks, wide networks employ relatively less number of layers and have various important benefits, such that they have less running time on parallel computing devices, and they are less affected by gradient vanishing problems. However, the parameter size of a wide network can be very large due to use of large width of each layer in the network. In order to keep the benefits of wide networks meanwhile improve the parameter size and accuracy trade-off of wide networks, we propose a binary tree architecture to truncate architecture of wide networks by reducing the width of the networks. More precisely, in the proposed architecture, the width is continuously reduced from lower layers to higher layers in order to increase the expressive capacity of network with a less increase on parameter size. Also, to ease the gradient vanishing problem, features obtained at different layers are concatenated to form the output of our architecture. By employing the proposed architecture on a baseline wide network, we can construct and train a new network with same depth but considerably less number of parameters. In our experimental analyses, we observe that the proposed architecture enables us to obtain better parameter size and accuracy trade-off compared to baseline networks using various benchmark image classification datasets. The results show that our model can decrease the classification error of baseline from 20.43% to 19.22% on Cifar-100 using only 28% of parameters that baseline has. Code is available at https://github.com/ZhangVision/bitnet

1. Introduction

Recently, Deep Neural Networks (DNNs) have achieved impressive results for many image classification tasks \cite{cifar10,imagenet,resnet,squeezenet,vgg}. Various architectures of DNNs have been proposed in order to improve classification accuracy. One approach used to improve accuracy of a DNN is to widen each layer while keeping the depth unchanged. For instance, it is empirically shown in \cite{wide} that a wide but relatively shallow DNN can obtain accuracy comparable to a narrow but relatively deep DNN on several classification tasks. There are two crucial benefits of wide-shallow DNNs. First, it usually runs faster than narrow-deep DNNs on parallel computing devices, e.g. GPUs, as illustrated in \cite{wide}. Also, a deep DNN with many layers may suffer from a gradient vanishing problem. Reducing the depth can ease this problem as shown in \cite{vanishing}. However, parameter size of DNNs may significantly increase with respect to improvement of accuracy by widening each layer.

In this paper, we address a problem of improvement of the parameter size and accuracy trade-off of the aforementioned wide-shallow DNNs. Specifically, given a baseline wide-shallow DNN, we aim to construct and train a new DNN equipped with the following two desirable properties.

- The new DNN has a depth not greater than the baseline wide-shallow DNN so that it can keep the aforementioned two benefits.
- The new DNN can achieve comparable accuracy using

![Figure 1. Left: A conventional architecture \cite{6}. Right: Proposed binary tree architecture. Arrows indicate data flow. The numbers depicted in the rectangle denote the width of the layer. Both architectures have depth 3 and output width 256. Our architecture has considerably less number of parameters.](https://github.com/ZhangVision/bitnet)
relatively less number of parameters compared to the baseline DNN, or can achieve better accuracy by using the same number of parameters as baseline DNN.

Toward this end, we propose a binary tree architecture for implementation of DNNs with a better trade-off. An illustrative comparison of our proposed binary tree architecture and conventional architectures [6, 28] is given in Figure 1. In conventional architectures, layers having same width (number of channels) are sequentially stacked. In the proposed binary tree architecture, the width of the \( k^{th} \) layer is \( \frac{D}{2^{k-1}} \), where \( D \) is the width of the first layer (\( k = 1 \)) (input layer). Additionally, connections between layers of the proposed architecture are established as connections used in an asymmetric binary tree. At each \( k^{th} \) layer of a binary tree architecture, we have \( C_k = \frac{D}{2^{k-1}} \) channels. Then, \( \frac{C_k}{2} \) of channels are connected to the channels of the \( k + 1^{st} \) layer. In addition, the remaining \( \frac{C_k}{2} \) channels are directly concatenated to form the output of the architecture. Note that our binary tree architecture can be generalized to fully connected layers in which the width becomes the number of neurons used at the layer.

Our motivation for employment of the proposed binary tree architecture is twofold. First, we intend to increase the expressive capacity of DNNs with a relatively small increase of parameter size. In this paper, we use the definition of expressive capacity proposed in the previous work [20, 13], where it is defined to be the maximal number of linear regions of (decision) functions computable by the given DNN. As shown in [20, 13], it reflects the complexity of class decision boundary computable by the DNN. Their results state that the maximal number of linear regions of a fully connected feed forward neural network endowed with ReLU [19] activation functions grows exponentially with respect to the depth of the network, and polynomially with respect to the width of the network (i.e., the number of neurons used at each layer of the network). Following this theoretical result, one can increase the expressive capacity with a small increase of the parameter size by simply stacking more layers with small width. This leads to the first characteristic structure of our binary tree architecture, which is obtained by continuous decrease of the width from input layer to higher layers by a factor of \( 2^{-1} \). With this specific structure, the expressive capacity grows with small increase of the parameter size. In our experiments, a binary tree used at convolutional layers of a DNN can increase classification accuracy with a small increase of parameter size of the DNN.

The second motivation for employment of our binary tree architecture is to ease a vanishing gradient problem observed in DNNs. While training DNNs, the magnitude of gradient can be cumulatively reduced when it is propagated from higher layers to lower layers. Therefore, the more layers are used for propagation, the weaker gradient will be obtained at the lower layers, which makes it difficult to train a DNN with many layers [11, 4]. Consequently, the gradient vanishing problem suggests reduction of the depth of a DNN, while increasing the depth may lead to efficient improvement of the expressive capacity as mentioned above. Thus, we need to trade-off between easing the gradient vanishing problem and increasing the expressive capacity, which motivates our second characteristic structure of our proposed binary tree architecture that is obtained by concatenation of features obtained at different layers. With this specific structure, gradients can propagate through short path to lower layers. An illustration is given in Figure 1 where flow of gradient propagation during backpropagation is depicted by red dash line. For a better illustration of vanishing gradients, we use thicker red line to show stronger gradient. Our empirical analyses in Section 4.4 show that concatenation of features at lower layers can ease the gradient vanishing problem.

Our contributions are summarized as follows.

1) We propose a binary tree architecture to improve the trade-off between parameter size and classification accuracy of given baseline wide-shallow DNNs. Meanwhile, the depth of baseline wide-shallow DNNs is not increased to keep the benefit of running speed on parallel computing devices.

2) Our experimental results show that, on the Cifar datasets, one can construct a DNN using the proposed binary tree architecture to achieve better accuracy but using considerably less number of parameters. On the Cifar-100 dataset, our models can outperform corresponding baselines by using only approximately 50% of baseline’s parameter size. One of our models decreases the classification error of baseline from 20.43% to 19.22% by using only 28% of parameters that baseline has. On ILSVRC12 task, we construct and train two DNNs using the proposed binary tree architecture which also provide better parameter size and classification accuracy trade-off than baseline models.

3) We also provide a theoretical analysis of the expressive capacity of DNNs endowed with our proposed binary tree architecture as a function of its depth and width. The theoretical results indicate that expressive capacity of DNNs endowed with our proposed binary tree architecture can grow with small increase of the parameter size.

The rest of this paper is organized as follows. The second section provides the related work. In Section 3, we introduce our binary tree architecture. Experimental results and analyses are given in Section 4. Section 5 concludes the paper.

2. Related Work

Recently, various architectures of convolutional neural networks (CNNs) have been proposed [14, 17, 26, 22, 27, 23]. In [10], connections between random forest [2] and
CNNs are investigated. Inspired by random forest, they embedded routing functions to CNNs and obtain Conditional CNNs. As shown in their experiments, Conditional CNNs with highly branched tree architectures can improve the accuracy-efficiency trade-off. Conditional CNNs can be considered as symmetric full tree architectures. On the other hand, we use an asymmetric tree architecture and concatenate features from different layers. Another related work, a fractal architecture used by FractalNet was proposed in [15]. Fractal architecture can also be considered as a tree architecture. Fractal architecture is different from ours in several aspects. First, the output of a fractal architecture is element-wise mean of features obtained at different layers. Also, all convolutional layers used in fractal architecture use the same width, which may result in a large parameter size if the width is large.

As shown in [12, 29], the parameter size of a trained CNN can be reduced by constructing a new CNN with less redundancy of weights. However, these methods may cause a drop on accuracy after a compression of model. With our architecture, we can boost the accuracy with less number of parameters. In [6], a residual architecture is proposed to construct CNNs (ResNets). ResNets enable us to train considerably deeper CNNs. The deepest ResNets employed for classification using the ILSVRC12 [21] and Cifar datasets have 200 and 1000 layers, respectively [6,7], and achieved impressive performance. However, a deep ResNet with many layers may suffer from two problems. First, the running speed on parallel computing devices may be slow compared to the speed of shallower ones. Thus, it takes more time to train a very deep ResNet. Also, the gradient vanishing problem [1,4] may also be observed on a very deep ResNet with many layers. To address these problems, a novel training procedure called stochastic depth is introduced in [9]. It enables one to train shallow ResNets during training and use deep ResNets for testing. Shallow ResNets can ease the gradient vanishing problem during training, and reduce the training time. Their experimental results show that their proposed training procedure can improve the test accuracy of baseline ResNets with constant depth. This indicates easing the gradient vanishing problem is crucial to train a very deep ResNet. However, during the test time, the depth of ResNets is the same as the depth of baseline which makes inference speed slower.

Intuitively, a simpler way to avoid gradient vanishing problem and accelerate the running speed during training and inference is to use a shallow network. In [28], Zagoruyko and Komodakis use a shallow ResNet, and increase the width to make the expressive capacity comparable with narrow-deep ones. Interestingly, they observe that wide-shallow CNNs can outperform its deeper-narrower peer CNNs which have the same parameter size on the Cifar-10/100 classification datasets. On the ILSVRC12 classification task, wide ResNets can also obtain comparable accuracy with smaller depth. Their results draw our attention to consider the wide-shallow DNNs. In their method, the width of each layer is symmetrically increased by the same factor. This will significantly increase the parameter size. Therefore, in this work, the proposed binary architecture truncate architecture of wide networks by reducing width of the networks considering their parameter size and accuracy trade-off. Our motivation for employment of binary tree architecture also considers gradient vanishing problem, which has been shown to be crucial for training DNNs in [9].

3. Binary Tree Architecture

In this section, we give an overview of conventional blocks used in previous works [6,28], and introduce our proposed binary tree architecture. Then, we theoretically analyze expressive capacity and parameter size of our proposed binary tree architecture considering its depth and width.

3.1. Conventional Blocks

In some CNNs [22, 6, 7, 28], a block is constructed by a stack of $K$ convolutional layers. At each $k^{th}$ layer, $k = 1, 2, \ldots, K$, we compute

$$X_k = f_k(X_{k-1}; W_k),$$

where $X_0 := X \in \mathbb{R}^{w \times h \times c}$. $X$ is an input tensor of features given to the block, $X_k \in \mathbb{R}^{\frac{w}{2^k} \times \frac{h}{2^k} \times D}$ is the tensor of features obtained at the output of $k^{th}$ layer, $c$ is the number of channels, $w$ is the width and $h$ is the height of a feature map. We assume that the number of convolutional filters used at each layer is $D$, and down-sampling is performed at the first convolutional layer by stride $s$. $f_k(X_k; W_k)$ is computed by a composition of a convolution operation, batch normalization [11] and nonlinear function $\sigma$, where $W_k$ denotes a set of trainable parameters used at the $k^{th}$ layer, e.g. the filter weights. The output feature tensor of the block is obtained at the last layer $Y := X_K \in \mathbb{R}^{\frac{w}{2^K} \times \frac{h}{2^K} \times D}$. In [1], we omit shortcut connection and element-wise addition used in [6] to simplify the notation. We refer to the block defined in [1] as a conventional block (ConvenBlock) with width $D$ and depth $K$ in the following sections. An illustration of ConvenBlock with width 256 and depth 3 is given in Figure 1(left).

3.2. Binary Tree Blocks

We define a binary tree block (BitBlock) by a binary tree $\mathcal{T} = (\mathcal{V}, \mathcal{E})$, where $\mathcal{V}$ is the set of nodes residing in the block, and $\mathcal{E}$ is the set of edges that connect the nodes. The architecture of a BitBlock is determined by its width $D$ and
depth $K$, where $D$ is the channel number, i.e. number of feature tensors provided by the BitBlock at the output, and $K$ is the depth of the binary tree $T$, as follows.

- At the root of a BitBlock $T$ denoted by $v_0 \in V$, we have a feature tensor denoted by $X_{0,t} := X \in \mathbb{R}^{w \times h \times c}$, where $X$ is given as an input to the block.
- At each $k^{th}$ layer (level) of a BitBlock, we apply two mapping functions $f_{k,l}$ and $f_{k,r}$ to the input feature tensor $X_{k-1,t}$. Then, we compute a feature tensor $X_{k,l}$ having $\frac{D}{2}$ channels on a left child node of $v_{k-1}$, and a feature tensor $X_{k,r}$ having $\frac{D}{2}$ channels on a right child node of $v_{k-1}$ at the $k^{th}$ layer of $T$. The feature tensor $X_{k,t}$ is further fed to the next $k + 1^{st}$ layer. More precisely, at each $k^{th}$ level, we compute

$$\begin{align*}
X_{k,l} &= f_{k,l}(X_{k-1,l}; W_{k,l}), \\
X_{k,r} &= f_{k,r}(X_{k-1,l}; W_{k,r}).
\end{align*}$$

- Finally, feature tensors computed at all right child nodes at each $k^{th}$ level of $T$, and the feature tensors computed at the left child node at the last $K^{th}$ level of $T$ are concatenated across channels to construct the output feature tensor of the BitBlock by

$$Y = \text{concat}(X_{1,l} \bullet X_{2,l} \cdots \bullet X_{K,l} \bullet X_{K,r}).$$

The size of concatenated tensor $Y$ is $(\frac{n}{s} \times \frac{h}{s} \times D)$. In the case of down-sampling, we apply a stride $s$ at the first layer as utilized in ConvenBlocks.

We note that $D$ is divided by $2^K$. Moreover, if $K = 1$, then the BitBlock $T$ reduces to a single convolution layer. Our BitBlocks can also be applied to fully connected layers using a feature tensor $X \in \mathbb{R}^{1 \times 1 \times c}$. We denote it by fully connected BitBlock. An illustration of proposed BitBlock with width 256 and depth 3 is given in Figure 1 (right). We can construct a DNN by stacking multiple BitBlocks. A DNN endowed with BitBlocks is called as a BitNet in this paper.

### 3.3. A Theoretical Analyses of Expressive Capacity of Binary Tree Blocks

In this section, we theoretically analyze expressive capacity and parameter size of the proposed binary tree block with respect to its depth and width when it is used at fully connected layers. We use the definition of expressive capacity proposed in the previous work [20][13]. Precisely, expressive capacity of a DNN is defined by the maximal number of linear regions of (decision) functions computable by the given DNN. The formal definition of linear regions of a function is given as follows.

**Definition 3.1 (Linear Region).** Given a function $f(\cdot)$ with $n$-dimensional input space $\mathbb{R}^n$, a linear region $\mathbb{R}^n$ of $f(\cdot)$ is a subspace of its input space, such that $f(\cdot)$ computes a linear mapping on that linear region, i.e. $\forall x \in \mathbb{R}^n$, $f(x) := w^T x + b$, and $\forall x \notin \mathbb{R}^n$, $f(x) 
eq w^T x + b$.

Consider a decision function $f(\cdot)$ computed by a DNN, then the more number of linear regions $f(\cdot)$ has, the more complex input-output mapping the DNN can compute. In other words, the DNN can compute more complex decision boundary and solve more complex classification tasks. A multilayer perceptron network implementing a linear activation function computes a linear mapping between input and output. Thus, it only has 1 linear region, i.e. the whole input space.

We provide the following two theoretical results regarding i) computation of the parameter size, and ii) computation of the maximal number of linear regions of functions computable by a fully connected conventional network and a BitNet. Proofs of the theorems are given in the supplemental material. We first provide the results for conventional networks that can be easily derived using the results given in [13].

**Corollary 3.2.** Suppose that we are given a fully connected neural network stacked by $L$ fully connected ConvenBlocks each having width $D$ and depth $K$. The parameter size of the given network is $O(LKD^2)$. The maximal number of linear regions of functions that can be computed by the given network in an $n$-dimensional ($D \geq n$) input space is lower bounded by $O((\frac{L}{n})^{nKD})$. ■

The expressive capacity of our proposed BitNet is given as follows.

**Proposition 3.3.** Suppose that we are given a BitNet stacked by $L$ fully connected BitBlocks each having width $D$ and depth $K$. The parameter size of the given BitNet is $O\left(\frac{L}{2} \left(1 - \frac{1}{2^K}\right) D^2\right)$. The maximal number of linear regions of functions that can be computed by the given BitNet in an $n$-dimensional ($D \geq 2^K n$) input space is lower bounded by $O((\frac{D}{2n})^{nKL})$. ■

As we observe from these results, when $D$ and $L$ are fixed, as $K$ increases, the expressive capacity of BitNets can grow with a small increase of the parameter size. Although the expressive capacity of a fully connected conventional network can grow faster as $K$ increases, its parameter size also grows faster than that of a BitNet. Although these theoretical results are obtained for fully connected layers, our experimental observations reflect that the results can be applied also for the convolutional layers. In our experiments, a binary tree used at convolutional layers of a DNN can increase classification accuracy with a small increase of parameter size of the DNN.
4. Experimental Results

We empirically analyze the proposed binary tree architecture using various baseline ResNets and several benchmark image classification datasets. We also analyze the gradient vanishing problem of the proposed binary tree architecture. In the implementation of BitNets, given a baseline ResNet, we can construct a BitNet of the same depth and the same block width with considerably fewer parameters compared to the baseline (ResNet). We can also increase the block width but keep the depth of baseline model by the proposed binary tree architecture and obtain a BitNet with a similar number of parameters. The configuration details of BitNets are given for each classification task.

4.1. Cifar-10 and Cifar-100

Cifar-10 and Cifar-100 [13] are image datasets consisting of 50,000 training images and 10,000 test images. The spatial size of each image is $32 \times 32$. Cifar-10 and Cifar-100 consist of 10 and 100 categories, respectively. The architectures of BitNets and ResNets used to perform analyses on the Cifar datasets are given in Table 1. As we can see from the table, the depth of a net is determined by the number of blocks in each group, i.e. $n$, and the depth of each block, i.e. $k$. The width of each block is determined by $d$.

We first compare performance of our proposed BitNets and that of Wide ResNets [28] by constructing nets with same depth and block width. Specifically, given a Wide ResNet with fixed value of $d$, $k$, and $n$, we use the same block width $d$ for BitNet. Then, we set values of $k$ and $n$ for BitNet, such that the total depth of BitNet equals to the total depth of the given Wide ResNet. We can use different value combinations of $k$ and $n$ for BitNet as long as $k \times n$ value for BitNet equals $k \times n$ value for the given Wide ResNet. For example, given a 38-layer Wide ResNet with $(d = 4, k = 2, n = 6)$, we can construct a BitNet with $(d = 4, k = 3, n = 4)$ or a BitNet with $(d = 4, k = 4, n = 3)$, both implying 38 layers.

For fair comparison with Wide ResNets, we use the same training and testing setting as employed in [28]. Specifically, for data augmentation, we use a common method used in previous works [5, 17, 6, 28]. More precisely, 4 pixels with zero values are padded on each side of the original image to make a $40 \times 40$ image, from which a $32 \times 32$ patch is randomly cropped and randomly flipped horizontally. For testing, the original $32 \times 32$ image is used. Batch size is 128 that is split on two GPUs. The initial learning rate is 0.1, and is reduced by 0.2 on the 60th, 120th and 160th epoch. The training is finished at the 200th epoch.

Table 2 provides the comparative results for several Wide ResNets and BitNets, which are designed with the same width and depth. As we can see from the results, using the same depth and width, BitNet has considerably less number of parameters and FLOPs. Moreover, BitNets can outperform Wide ResNets using considerably less number of parameters. We compare BitNets with four baseline Wide ResNets. In the analyses, we obtained the following results:

1) A Wide ResNet having $(d = 4, k = 2, n = 6)$ is the deepest and narrowest architecture among four baseline architectures. The BitNet $(d = 4, k = 4, n = 3)$ and the BitNet $(d = 4, k = 3, n = 4)$ can obtain comparable performance with this baseline and the parameter size is only 30% and 41% of that of baseline, respectively. The BitNet $(d = 4, k = 2, n = 6)$ is constructed by using more number of blocks but reduce the depth of each block. As shown in Section 4.4, this BitNet suffers from a gradient vanishing problem during the training due to use of small $k$ and a large $n$. As a result, the performance slightly degrades. BitNet $(d = 4, k = 6, n = 2)$ has least parameter size, i.e. only 19% of baseline’s parameter size. However, it also performs worst.

2) Compared with first baseline ResNet $(d = 4, k = 2, n = 6)$, the baseline ResNet $(d = 10, k = 2, n = 2)$ is wider and shallower. The BitNet $(d = 10, k = 2, n = 2)$ outperforms it by 1% in the Cifar100 task by using approximately 56% of baseline ResNet’s parameter size. Another configuration of BitNet $(d = 10, k = 4, n = 1)$ uses only one BitBlock at each group, resulting in only 23% of baseline’s parameter size. However, the performance is also degraded by more than 1% using the Cifar-100 dataset. For the Cifar-10 dataset, both BitNets obtain similar performance compared to the baseline.

3) For the Wide ResNet $(d = 10, k = 2, n = 3)$, both BitNets obtain more than 1% performance boost using the Cifar-100 dataset. For the Cifar-10 dataset, the performance boost is more than 0.5%. Notably, the parameter size of the BitNet $(d = 10, k = 3, n = 2)$ is only 38% of the parameter size of the baseline.

| Group Name | Configuration | Output Size |
|------------|---------------|-------------|
| conv1      | conv, 16 channels | $32 \times 32$ |
| conv2      | block$(d \times 16, k) \times n$ | $32 \times 32$ |
| conv3↓     | block$(d \times 32, k) \times n$ | $16 \times 16$ |
| conv4↓     | block$(d \times 64, k) \times n$ | $8 \times 8$ |
| gap        | global average pooling | $1 \times 1$ |
| fc         | 10 or 100-way softmax | |

Table 1. The CNN architecture employed for classification using the Cifar-10 and Cifar-100. BitNets use BitBlock as block type, and ResNets use ConvenBlock with residual connection. $k$ denotes the depth of each block (for all ResNets used in this paper). $d$ determines the width of each block. $n$ denotes a stack of $n$ blocks. All convolutional layers use filters of size $3 \times 3$. Batch Normalization is used at every convolutional layer before ReLU. Down-sampling is performed by applying pooling at the first convolutional layer of the first block in Group conv3 and conv4.
Table 2. Classification error (%) of CNNs for the Cifar-10/100 datasets. Using the same depth and block width, our BitNets can outperform Wide ResNets with considerably less number of parameter size. Underlined numbers indicate the best performance among models having the same depth and same block width. Bold numbers denote the best performance obtained for all models. Definition of \( d \), \( k \) and \( n \) are given in Table 1. All of Wide ResNets and our BitNets are trained using data augmentation and without using dropout.

(4) The Wide ResNet \( (d = 12, k = 2, n = 4) \) has the largest parameter size among four baseline models. Our two BitNets both outperform the baseline by more than 1% accuracy. Note that the parameter size of the BitNet \( (d = 12, k = 4, n = 2) \) is only 28% of that of the baseline.

We emphasize that the performance of baseline Wide ResNets are already close to the state-of-the-art. Thus more than 1% boost of the accuracy is obtained. To summarize, most of our BitNets can achieve better or approximately equal accuracy using less number of parameters, which indicates that our binary tree architecture can improve the parameter size and accuracy trade-off of baseline Wide ResNets. There are two BitNets whose accuracy are roughly 1% lower than that of their baselines. This is possibly because they use too less number of BitBlocks causing insufficient expressive capacity. The rest of BitNets obtain sufficient expressive capacity with a relatively less number of parameter size. Compared with other previous models such as Stochastic Depth ResNet [9] and FractalNet [15], our BitNets can outperform them using less number of parameter size.

4.2. ILSVRC12

To evaluate the proposed architecture on a large scale image classification task, we also use the training and validation dataset of ILSVRC12 [21], which consists of 1.3M training images and 50,000 validation images belonging to 1000 categories. During training, data augmentation and image preprocessing methods are used as follows. The input images are mean subtracted and variance normalized on each RGB channel. The color distortion methods proposed in [14] and [8] are both used. For validation, the image is resized such that its shorter side is 256, and a center crop of 224 \( \times \) 224 are used to test. Batch size is 256 split on 8 GPUs. The initial learning rate is 0.1 and is reduced by \( 10^{-1} \) at each 30 epoch. The training is finished at the 90th epoch. Following [6], stochastic gradient descent (SGD) with momentum 0.9 is used as our optimizer and the weight decay is set as 0.0001. Batch Normalization is used in every convolutional layer before ReLU. We didn’t use dropout [24] in any BitNet.
In this task, we construct two BitNets (BitNet-26 and BitNet-34) in order to compare their performance with that of ResNet-34 [6]. The details of models are given in Table 3. The classification results are given in Table 4. The results show that our BitNets have better parameter size and accuracy trade-off than ResNets. Specifically, BitNet-34 outperforms ResNet-34 B by 1% using same parameter size, while their depth is the same. Another smaller BitNet-26 obtains 1% higher error compared to ResNet-34 B. However it is shallower and the parameter size is approximately 50% of ResNet-34 B. Compared to model FractalNet-34, BitNet-34 also outperforms it. BitNet-26 outperforms ResNet-18 B by approximately 2% accuracy using the same number of parameters. Increasing the width of ResNet-18 by methods in [28] can improve the accuracy. However the cost for the improvement is also huge. BitNet-26 and ResNet-18 B width × 2 have comparable accuracy, but the parameter size of our BitNet is almost two times smaller than that of ResNet. Similarly, the parameter size of BitNet-34 is only 50% of ResNet-18 width × 3.

### 4.3. Experimental Analyses of Depth of BitBlock

Also, we observe that using the same width d and same number of BitBlocks n, BitBlocks having different depth may provide different performance (see BitNet \((d = 10, k = 3, n = 2)\) and BitNet \((d = 10, k = 2, n = 2)\) in Table 2). Thus, we further analyze how performance of BitNets changes with respect to the depth of BitBlocks. Specifically, we evaluate BitNet \((d = 4, k, n = 4)\) (a deep-narrow one) and BitNet \((d = 12, k, n = 2)\) (a relatively shallower-wider one) by setting different values to \(k\). The results are given in Table 5. As illustrated in the table, as \(k\) increases, both BitNets gain a performance boost due to an increase on the expressive capacity. Note that for the BitNet \((d = 12, k, n = 2)\) employed using the Cifar-100, there is almost a 4% performance boost from \(k = 1\) to \(k = 2\) with a 33% increase of parameter size. We observe that the performance boosts further as \(k\) increases. These observations match our theoretical analyses provided in Section 3.3 which states that as \(d\) and \(n\) are fixed, increasing \(k\) can increase the expressive capacity of a BitNet with a small increase of parameter size. However, the boosting trend tends to be saturated after \(k \geq 3\), and the increase of parameter size is also negligible. This can be explained as follows. As \(k\) increases, the width of convolutional layer also decreases in the binary tree architecture resulting in a saturated expressive capacity. Additionally, we also observe that wider BitNets \((d = 12)\) gain more performance boost than a narrower Bitnet \((d = 4)\) with the same increase on \(k\). This is simply because the increased layers in the wider BitNet are wider than narrower one, thus it can increase more expressive capacity.

| Group | BitNet-26 | BitNet-34 | Output Size |
|-------|-----------|-----------|-------------|
| conv  | conv 7 × 7, 64 channels, stride 2 | 112 × 112 |
| conv2 | max pooling 3 × 3, stride 2 | 56 × 56 |
| conv3 | \(b(128, 3) \times 2\) | \(b(256, 4) \times 2\) |
| conv4 | \(b(192, 3) \times 1\) | \(b(384, 4) \times 2\) |
| conv5 | \(b(512, 3) \times 1\) | \(b(768, 4) \times 2\) |
| gap   | global average pooling | 1 × 1 |
| fc    | 1000-way softmax | |
| Param. | 12.79M | 22.99M |
| FLOP  | \(2.8 \times 10^9\) | \(7.8 \times 10^9\) |
| Depth | 26 | 34 |

Table 3. Structure of BitNets used for ILSVRC12 classification task. \(b(d, k) \times n\) refers to a stack of \(n\) BitBlocks with width \(d\) and depth \(k\). All convolutional layers employed in each BitBlock use filters of size 3 × 3. The output size is reduced by applying stride 2 at the first convolutional layer of first block in some Groups.

| Model | Single Crop | Ten Crop | Param |
|-------|-------------|----------|-------|
| ResNet-18 B [6] | 30.43 | 28.22 | 13.1M |
| Width ×2 [28] | 27.06 | – | 25.9M |
| Width ×3 [28] | 25.58 | – | 45.6M |
| FractalNet-34 [15] | – | 24.12 | – |
| ResNet-34 B [6] | 26.73 | 24.76 | 23.2M |
| Width ×2 [28] | 24.5 | – | 48.6M |
| BitNet-26 | 27.74 | 25.83 | 12.8M |
| BitNet-34 | 25.46 | 23.77 | 23.0M |

Table 4. Single model, Top-1 classification error (%) obtained using ILSVRC12 validation dataset.

| \(k\) | BitNet \((d = 4, k, n = 4)\) | BitNet \((d = 12, k, n = 2)\) |
|-------|-----------------|-----------------|
| \(k = 1\) | 2.7M 4.98/23.54 | 10.3M 6.02/23.80 |
| \(k = 2\) | 3.5M 4.68/22.72 | 13.8M 4.02/19.86 |
| \(k = 3\) | 3.7M 4.82/22.19 | 14.7M 3.98/18.97 |
| \(k = 4\) | 3.7M 4.69/22.65 | 14.9M 4.11/19.22 |
| \(k = 5\) | 3.7M 4.69/22.86 | 15.0M 4.09/18.95 |
| \(k = 6\) | 3.7M 4.77/22.69 | 15.0M 4.19/19.51 |

Table 5. Cifar-10/100 classification error (%) of two BitNets with respect to \(k\). Definition of \(d, n, \) and \(k\) are given in Table 1.
4.4. Experimental Analyses of Gradient Vanishing Problem

In this section, we analyze our BitNets considering the gradient vanishing problem. Specifically, during the training of a BitNet or Wide ResNet employed using the Cifar-100, we compute the mean magnitude (L2-norm) of gradient obtained at the first convolutional layer per epoch. The results are given in Figure 2. We analyze 9 models having different depth but same width $d = 4$. In the figure, wide resnet-38 refers to the Wide ResNet $(d = 4, k = 2, n = 6)$ having 38 layers and plainnet-38 is the one designed without using residual shortcut connections. Models denoted by $b(d, k, n) - m$ are proposed BitNets and $m$ is the total depth.

As we can see from the figure, for all models having 38 layers, our BitNet $b(4, 6, 2) - 38$ shows the strongest magnitude, even stronger than wide resnet-38. This results indicates that using concatenation in the proposed binary tree architecture can ease the gradient vanishing problem. We also observe that gradient becomes weaker as the number of blocks $n$ is increased and the depth $k$ of each BitBlock is reduced. For instance, for all 38 layers BitNets, the magnitude can be roughly sorted by $b(4, 2, 6) - 38$ weaker than $b(4, 3, 4) - 38$ weaker than $b(4, 4, 3) - 38$ weaker than $b(4, 6, 2) - 38$ according to the strength of the magnitude. This observation reflects that as $n$ increases and $k$ decreases, features obtained at less number of lower layers are concatenated to form the output of each BitBlock. In general, the gradients propagate more layers to reach lower layers.

We also analyze how the gradient magnitude changes with respect to BitBlock’s depth $k$ if $d$ and $n$ are fixed. As we can see, $b(4, 1, 2) - 8$ shows the strongest magnitude of gradient among all nine models as expected because it is the shallowest model. By increasing $k$, we observe that for BitNet $b(4, 4, 2) - 26$ and $b(4, 4, 2) - 38$, the magnitude is decreased because more layers are used to propagate gradient in BitBlocks.

The errors obtained for nine models are given in Table 6. Although $b(4, 1, 2) - 8$ and $b(4, 2, 2) - 14$ show stronger gradient magnitude than wide resnet-38, they provide higher classification errors. This is mainly because the depth of these two BitNets is too small resulting in insufficient expressive capacity. BitNet $b(4, 4, 3) - 38$ obtains comparable classification performance by using larger depth. The gradient magnitude of BitNet $b(4, 4, 3) - 38$ is also comparable with that of resnet, which benefits from the proposed binary tree architecture. Without using binary tree architecture, the gradient magnitude of plainnet-38 is weaker than that of resnet-38 and the final classification error is larger.

5. Conclusions

In this paper, we introduce and analyze a binary tree architecture to truncate architecture of wide networks considering their parameter size and accuracy trade-off. In the proposed architecture, the width at each layer is continuously reduced from lower layers to higher layers. Also, features obtained at different layers are concatenated to form the output of our architecture. In our experiments, the networks which are designed using the proposed architecture, called BitNets, can obtain better parameter size and accuracy trade-off on several benchmark datasets compared to baseline networks endowed with conventional architectures. Additionally, in our experimental analyses, we observe that the concatenation structure can ease the gradient vanishing problem. We also provide a theoretical analyses of the expressive capacity of BitNets. In our future work, we plan to use BitNets for object detection tasks.
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Supplemental Material

In the supplemental material, we provide the proofs of Corollary 3.2 and Proposition 3.3 in Section 3.3 in the main paper. We also show training errors of proposed BitNets used in our experiments.

A. Proofs

Proof of Corollary 3.2. The total depth of the given network is $L K$. Thus, the parameter size is $O(L K D^2)$. Also, according to Corollary 5 of [18], the maximal number of linear region of functions that can be computed by the given network in an $n$-dimensional $(D > n)$ input space is lower bounded by $O(\left(\frac{D}{n}\right)^n K L - 1) D^n$, which can be simplified by a looser bound $O(\left(\frac{D}{n}\right)^n K L)$ and resulting in our corollary.

Proof of Proposition 3.3. According to the definition of BitBlock, the width of $k^{th}$ layer in a BitBlock is $D^{2(k-1)}$. Thus, the parameter size of the given BitBlock can be computed by,

$$
\sum_{k=1}^{K} \left(\frac{D}{2^{(k-1)}}\right)^2 = \frac{4}{3} \left(1 - \frac{1}{4^K}\right) D^2
$$

Thus, the parameter size of $L$ stacked BitBlocks is $O\left(\frac{4}{3} L (1 - \frac{1}{4^K}) D^2\right)$. According to Theorem 4 of [18], the maximal number of linear regions of functions that can be computed by a given BitBlock in an $n$-dimensional $(D \geq 2^K n)$ input space is lower bounded by

$$
\prod_{k=1}^{K} \left(\frac{D}{n}\right)^n = \left(\frac{D}{n}\right)^{n K} 2^{n(1+K)K} > \left(\frac{D}{n}\right)^{n K} 2^{-n K K} = \left(\frac{D}{2^K n}\right)^{n K}.
$$

As a result, with $L$ BitBlocks, the maximal number of linear region is bounded by $O\left(\left(\frac{D}{2^K n}\right)^{n K L}\right)$.

B. Training Errors

Training and testing errors of BitNets used in our experiments for Cifar-100 classification task are given in Table 7. As shown in [20, 18], the expressive capacity reflects

| Model                           | Param. | Test Err. | Train Err. |
|---------------------------------|--------|-----------|------------|
| Wide ResNet (d=4,k=2,n=6)      | 8.9M   | 22.89     | 0.018      |
| BitNet (d=4,k=3,n=4)           | 3.7M   | 22.19     | 0.018      |
| BitNet (d=4,k=4,n=3)           | 2.7M   | 22.60     | 0.022      |
| BitNet (d=4,k=2,n=6)           | 5.4M   | 23.22     | 0.026      |
| BitNet (d=4,k=6,n=2)           | 1.7M   | 23.87     | 0.028      |
| Wide ResNet (d=10,k=2,n=2)     | 17.1M  | 21.59     | 0.018      |
| BitNet (d=10,k=2,n=2)          | 9.6M   | 20.48     | 0.018      |
| BitNet (d=10,k=4,n=1)          | 3.9M   | 23.88     | 0.020      |
| Wide ResNet (d=10,k=2,n=3)     | 26.8M  | 20.75     | 0.018      |
| BitNet (d=10,k=2,n=3)          | 15.6M  | 19.29     | 0.018      |
| BitNet (d=10,k=3,n=2)          | 10.2M  | 19.37     | 0.018      |
| Wide ResNet (d=12,k=2,n=4)     | 52.5M  | 20.43     | 0.018      |
| BitNet (d=12,k=2,n=4)          | 31.2M  | 19.06     | 0.018      |
| BitNet (d=12,k=4,n=2)          | 14.9M  | 19.22     | 0.018      |

Table 7. Cifar-100 classification error (%) of the BitNets and Wide ResNets used in our experiments.