Efficient Ab-Initio Molecular Dynamic Simulations by Offloading Fast Fourier Transformations to FPGAs

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Abstract—A large share of today’s HPC workloads is used for Ab-Initio Molecular Dynamics (AIMD) simulations, where the interatomic forces are computed on-the-fly by means of accurate electronic structure calculations. They are computationally intensive and thus constitute an interesting application class for energy-efficient hardware accelerators such as FPGAs. In this paper, we investigate the potential of offloading 3D Fast Fourier Transformations (FFTs) as a critical routine of plane-wave-based AIMD paper, we investigate the potential of offloading 3D Fast Fourier Transformations (FFTs) as a critical routine of plane-wave-based electronic structure calculations to FPGA and in conjunction demonstrate the tolerance of these simulations to lower precision computations.

I. INTRODUCTION

AIMD simulations are one of the most computationally intensive scientific simulations in current high performance cluster systems. These simulations involve computing interatomic forces using accurate electronic structure calculations to simulate the motion of atoms. Accelerating these simulations has led to massively parallel computations using multicore processors and hardware accelerators. Popular AIMD simulation software packages such as Quantum Espresso[1] and CP2K[2] offer CUDA implementations to offload specific routines to GPUs. This scale of processing has led to maximizing performance through efficient computation.

One of the approaches to improve efficiency involves sacrificing accuracy in computations using lower precision arithmetic units, a strategy denoted as Approximate Computing (AC). Techniques such as half-precision floating point arithmetic are used in hardware accelerators, specifically in recent Nvidia GPUs to support applications that tolerate approximation. Field Programmable Gate Arrays (FPGAs) are becoming increasingly relevant in this regard, mainly due to the flexibility in building custom data paths and arbitrary widths/precision fixed or floating point units.

In AIMD, a key kernel on the critical path of plane-wave-based density functional theory (DFT) calculations are 3D FFTs, which are exploited for an efficient evaluation of the quantum-mechanical operators. Accelerating this routine involves optimizing execution in ranges of microseconds. In the context of classical force-field-based Molecular Dynamics (MD) simulations, Humphries et al. implement high performance 3D FFT with single precision floating point accuracy by fitting the entire data set in the FPGA and by using vendor-specific 1D FFT IP blocks. Their evaluation focuses on the performance of the 3D FFT design, but does not evaluate the impact of reduced precision on the MD application in question. This raises the question whether acceleration of specific routines with reduced precision can be tolerated by MD simulations. Recently, Rengaraj et al. have shown that errors introduced by low precisions computing can be modeled as noise and can be perfectly corrected at the algorithmic level by means of a modified Langevin equation[5].

In this paper, the resilience of AIMD simulations to approximation from lower precision floating point arithmetic is investigated by offloading 3D FFT computations to FPGAs. This is demonstrated by designing an Open Computing Language (OpenCL) based 3D FFT design for Intel FPGAs that uses single precision instead of double precision floating points for computations. This is compared with FFTW for performance and evaluated for AIMD simulations by creating an interface in the CP2K framework. As an initial contribution, this interface has already been adopted as part of CP2K 7.1 release[4].

II. APPROACH

3D FFT is an efficient algorithm to compute a 3D discrete Fourier transform (DFT) as defined in Equation [1], where

\[ F(k_x, k_y, k_z) = \sum_{z=0}^{N-1} f(x, y, z) W_z^{k_x} W_y^{k_y} W_z^{k_z} \]

To compute the 3D FFT of \(N^3\) points, the computation can be decomposed into 1D FFTs in \(x\)-dimension followed by the same in the \(y\)-dimension and then the \(z\)-dimension.

The platform to offload this routine is the Nallatech 520N board that houses a Stratix 10 GX2800 FPGA along with four 8 GB banks of DDR4 memory. It is connected to the host CPU using an 8-lane Gen3 PCIe bus. Developing an OpenCL 3D FFT kernel design targeting this board requires transferring \(N^3\) points from the host CPU to the DDR (global) memory via the PCIe bus, transforming the data and finally, transferring the results back to the host CPU. The transformation step involves fetching data from the global memory followed by

[1] https://github.com/cp2k/cp2k/releases/tag/v7.1.0
The 3D FFT design described above is implemented for Intel’s Stratix 10 FPGAs. It uses single precision floating point digital signal processing (DSP) blocks in 1D FFT computations. The code is available as an open source project\(^2\)\footnote{https://github.com/pc2/fft3d-fpga}. The FPGA kernel code is synthesized using Intel OpenCL SDK 19.3 for Nallatech 520N board. The host code, which is compiled using GCC v8.3, measures the total wall clock time of PCIe data transfers between the host and the DDR memory as well as the time taken for kernel execution that includes FPGA and DDR memory communication. This is measured over an average of a hundred iterations of non-batched executions.

Here, the performance of the Stratix 10 implementation is compared with the single precision floating point variant of FFTW v3.3.8. The FFTW application is linked using GCC v8.3 and executed on a node with two Intel Xeon Skylake Gold 6148 CPUs, each featuring 20 cores with hyperthreading disabled operating at 2.4 GHz. Performance is measured by scaling the number of threads from 1 to 40 threads pinned to the 40 cores available for an average of hundred iterations each, using all four planning heuristics; the best runtime obtained among the different multithreaded executions is used for comparison, as shown in Table I.

Table I. Comparison of runtimes in milliseconds of different 3D FFT sizes between FFTW and FPGA 3D FFT along with the latency of PCIe data transfers between host and DDR memory

| N\(^3\) | FFTW Kernel Execution | PCIe Data Transfer |
|-------|-----------------------|-------------------|
| 16\(^2\) | 0.01                  | 0.11              |
| 32\(^2\) | 0.03                  | 0.22              |
| 64\(^2\) | 0.14                  | 0.74              |

The performance of the FPGA is promising considering the evaluation compares highly optimized libraries utilizing 40 core server CPUs. The latency of the FPGA implementation can be reduced by overcoming the bottleneck with the 3D transpose step. PCIe data transfer latency can be overcome using larger transforms, making use of the available bandwidth.

In order to evaluate the resiliency of AIMD simulations to approximate floating point arithmetic, an interface to the FPGA 3D FFT implementation is integrated into the CP2K framework. This is then compared with the default double precision CPU execution of 3D FFT using FFTW3\(^4\). The application chosen for evaluation uses the Gaussian and plane wave DFT method to compute the molecular orbitals of a single H\(_2\)O molecule in the gas phase\(^7\). By restricting the plane-wave density cutoff, the application is evaluated for the specific 3D FFT sizes that matches the FPGA implementation. Both experiments converge to nearly identical total energies, leading to similar nuclear forces, thus showing that the AIMD simulations are tolerant to approximations in floating point arithmetic.

With these initial accomplishments, further work can be focused on efficient acceleration of AIMD simulations by developing a competitive 3D FFT design for FPGAs that scales to larger FFT sizes, where FPGAs should have a significant advantage. Moreover, investigating the tolerance of AIMD simulations towards further approximation using custom precision floating point units in FPGAs could help achieve higher computational efficiency.

\(^2\)https://github.com/pc2/fft3d-fpga

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