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To cite this article: Liyue Yuan et al 2018 IOP Conf. Ser.: Mater. Sci. Eng. 394 042012

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Research on Power Grid Imbalance and Harmonics Based on Improved Phase-Locked Loop

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Abstract. In the new energy grid connected power generation system, accurately extracting the grid synchronization signals such as frequency, phase and amplitude of the grid voltage is the basis for effective control. A new design method of phase-locked loop (PLL) in static coordinate system is proposed for the demand of synchronous signal detection under unbalanced and harmonic conditions. This method uses the resonator to extract and filter the high frequency harmonics in the grid voltage, and combines the adaptive trap (ANF) and the positive and negative sequence elimination loop (PNSC) to complete the voltage positive and negative sequence separation, and then accurately extracts the synchronous information of the positive sequence voltage of the power grid. The simulation and experimental results show that under the conditions of unbalanced and harmonic grid, the designed PLL can quickly and accurately lock the property of the grid voltage, and has the advantages of high detection precision and strong robustness to frequency fluctuation. It can provide reliable reference signal for the new energy grid connected power generation control.

1. Introduction

In view of the phase-locked loop technology under the harmonic grid, the multi frequency trap [1], the first order low pass filter [2] and the multi frequency decoupling [3] are applied to the design of the new phase locked loop, and many advanced phase locked loops are put forward. In document [4], a multi frequency phase locked loop technology is proposed, which combines Nikai Hiyoshi integrator and Frequency-Locked Loop (FLL) to design high frequency harmonic elimination network to eliminate the influence of harmonic. In document [5], by analyzing the small signal model of the existing PLL, an improved Type-3 phase locked loop is proposed. By designing a high order loop filter, the frequency information of the power grid can be extracted without the high frequency filter network. In document [6], an adaptive vector filter (Multiple Adaptive Vectorial Filter-PLL, MAVF-PLL) is proposed to extract the positive, negative and high frequency signals. Literature [7] analyses the shortcomings of SOGI, and proposes a pre filter MSOGI-FLL (Multiple SOGI-FLL with Prefilter, MSOGI-FLL-WPF) technology to enhance the ability to suppress harmonics.

According to the research status of PLL, this paper proposes an improved phase-locked loop technology for unbalanced power grid and harmonic. The phase locked loop first designs the high-frequency harmonic elimination module through the resonator to eliminate the influence of the high
frequency harmonic. Then the two orthogonal signals output by the ANF are used to eliminate the positive and negative sequence of the voltage. The voltage synchronization signal is detected by the αβPLL. Through simulation and experimental verification, the proposed phase-locked loop can separate the positive, negative and high-frequency harmonic signals under the condition of unbalanced and harmonic waves, and accurately track the frequency information of the positive sequence voltage, which has the characteristics of frequency adaptive, fast response and strong robustness.

2. improved phase locked loop structure

According to the formula (1), under the condition of unbalanced and harmonic power of the power grid, the influence of various harmonics can be eliminated by the design of multiple harmonic elimination modules based on the frequency n of the power grid, and then the improved phase locked loop under the unbalance condition of the power grid is applied to track the same step signal of the positive sequence voltage of the power grid in real time, and it is suitable for the imbalance of the power grid. The block diagram of the improved PLL under harmonic conditions is shown in Figure 1.

\[
V_i = V^p \cos\left(\omega t + \phi^p - k_i \frac{2\pi}{3}\right) + V^n \cos\left(-\omega t + \phi^n - k_i \frac{2\pi}{3}\right) + \sum_{n=5,7,\ldots} V^n \cos\left(n\omega t + \phi^n - k_i \frac{2\pi}{3}\right) i = a, b, c
\]

(1)

**Figure 1.** Structure diagram of improved PLL

2.1. Filtering characteristic and parameter design of harmonic elimination module

In order to eliminate the harmonics of 5, 7 and 11 harmonics in the power grid, in order to better eliminate the influence of high frequency harmonics, the cascade filter structure and the small signal model of harmonic elimination are shown in Figure 2.

**Figure 2.** Small-signal model of harmonic cancellation

According to Fig. 6, the transfer function of the harmonic elimination module can be obtained.

\[
G_{oi}(s) = \prod_{n=5,7,11,13,\ldots}^N \frac{s^2 + (n\omega_i)^2}{s^2 + 2\omega_i s + (n\omega_i)^2}
\]

(2)
In the form, $\omega_3$ is the fundamental frequency of the power grid. When the filter module passes the H sub harmonics, the filter gain is obtained.

$$G_{o1}(j\omega_3) = \prod_{n=5,7,11,13,...}^{N} \left(1 + \frac{1}{\sqrt{1 + \left[\frac{2h\omega_{cn}}{(n^2 - h^2)\omega_{cn}}\right]^2}}\right)$$

(3)

When the harmonic frequency is equal to a certain resonant frequency that needs to be eliminated, such as $h=5$, the relationship exists.

$$G_{o1}(j5\omega_3) \approx 0 \prod_{n=5,7,11,13,...}^{N} \left(1 + \frac{1}{\sqrt{1 + \left[\frac{2h\omega_{cn}}{(n^2 - 5^2)\omega_{cn}}\right]^2}}\right) = 0$$

(4)

According to the transfer function of formula (2), the response time of filtering can be obtained.

$$t_s \approx \frac{3}{\omega_{cn}}$$

(5)

$$t_{sd} \approx \frac{4}{\zeta \omega_0}$$

(6)

The response time is 0.05s, and the harmonic attenuation effect of the filter is considered. The cut-off frequency is 60rad/s. The above analysis can be verified by the filter Bode diagram of Figure 3, which has a good attenuation effect for high frequency harmonics of a specific frequency, with good frequency effect for low frequency harmonics and no phase shift. The excellent high-frequency harmonic attenuation effect shows that the resonator has a good extraction ability for high frequency harmonic components.

Figure 3. Bode diagram of harmonic cancellation
2.2. Parameter design and stability analysis of unbalanced phase locked loop

According to the ANF transfer function of formula (5), it can be concluded that the response time $A$ of the output signal tracking input signal is related to the system parameter $A$ and the input signal frequency.

In the case of a certain input signal frequency, the response time of the system is mainly influenced by the value of the parameter $\zeta$. Considering that the phase locked loop needs a rapid response process, the parameter $\zeta$ is usually valued at 0.707.

The block diagram in Figure 1 is simplified as a small signal model, as shown in Figure 4.

![Figure 4. Small-signal model of $\alpha\beta$PLL](image)

According to Fig. 4, the $\alpha\beta$ PLL’s closed loop transfer function for phase is

$$G_c(s) = \frac{\dot{\theta}(s)}{\theta(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i}$$

(7)

The characteristic polynomial of $\alpha\beta$PLL is

$$s^2 + k_p s + k_i = 0$$

(8)

To obtain the relevant information of the high frequency harmonic components, the Park transformation of the high order harmonic components can be designed on the basis of the existing PLL, and the form of the subsequent control process can be obtained.

3. Experimental verification

In order to further verify the phase-locked loop performance of the phase-locked loop under the condition of unbalanced and harmonic power grid, a hardware platform based on DSP is built for experimental verification. The experimental equipment, in the experiment, the TMS320F28335 DSP chip of TI company is used as the main control chip to carry out the signal acquisition, operation and processing. By sampling the voltage of the three-phase balance grid, the negative sequence and high frequency signal produced in the DSP are superimposed, and the state of the power grid is simulated. The phase-locked loop program is discrete mining.

The sentence execution frequency is 120MHz, the sampling and program running frequency is 10 kHz; the data of the program running process is transmitted to the host computer software for display and data storage by CAN communication at the rate of 1Mbit/s, and the real waveform is obtained by using the Matlab software. The grid fault condition in the experiment is the same as that in the simulation. The waveform of the fault grid and the experimental results are shown in figures 5 to 10.
According to figure 5, it can be seen that the improved phase locked loop can be stable in a shorter time when the frequency mutation occurs under unbalanced and harmonic conditions. Compared with
MAVF-PLL and MSOGI-FLL, it has faster response speed, and there is no frequency fluctuation in the traditional $\alpha\beta$PLL, which is in agreement with the simulation results.

Compared with the experimental results of three phase locked loops in Figure 6 to 9, the improved phase locked loop can quickly and smoothly separate the positive and negative sequence and harmonic components in the frequency mutation. Because the frequency information of MSOGI-FLL extraction is relatively slow, the separation speed of positive and negative sequence voltage components is significantly lower than the other two phase locked loops. The extraction of high frequency signals from MAVF-PLL and MSOGI- FLL has small fluctuation, and the extraction process of the improved phase locked loop is smooth, so it has excellent dynamic and static performance.

According to the experimental results of the voltage phase shift of power grid in Figure 10, the improved phase locked loop can reach the power grid frequency in 0.05s, and the actual phase of the power grid can be traced, so it has a faster response speed.

According to the experimental results of power grid imbalance and harmonic, the improved phase-locked loop can accurately extract high frequency harmonic, separate the positive and negative voltage of the power grid, and accurately track the synchronous information of the power grid. The experimental results are in good agreement with the simulation results, and the dynamic and static performance of the improved PLL is verified again.

4. Conclusion
In this paper, an improved phase-locked loop (PLL) technique for power grid imbalance and harmonics is proposed, which can quickly and accurately track the frequency, phase and amplitude of the positive sequence voltage of the power grid. This method uses the resonator to design the high-frequency harmonic elimination module to eliminate the influence of the high frequency harmonics in the power grid, and uses ANF and PNSC to complete the positive and negative sequence separation in the two phase stationary coordinate system, and the positive sequence voltage component can track the synchronous signal of the power grid in real time through the $\alpha\beta$PLL. The proposed phase-locked loop is simple and easy to expand. Through a simple further design, the amplitude and phase of the negative sequence and harmonic wave components can be obtained, so as to meet the requirements of the different controllers for the synchronous signals of the power grid. The simulation and experimental results show that the improved phase locked loop can quickly and accurately track the synchronous signal of the power grid under the condition of unbalanced and harmonic power grid. It has good dynamic and static performance, and has frequency self-adaptability. It can provide accurate control datum for new energy grid connected power generation.

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