Testing station for fast screening of through silicon via-enabled application-specific integrated circuits for hard x-ray imaging detectors

Daniel P. Violette,*,† Branden Allen, Jaesub Hong, Hiromasa Miyasaka, and Jonathan Grindlay

*Center for Astrophysics | Harvard & Smithsonian, Cambridge, Massachusetts, United States
†NASA FINESST fellow.

Abstract. Application-specific integrated circuits (ASICs) are used in space-borne instruments for signal processing and detector readout. The electrical interface of these ASICs to frontend printed circuit boards is commonly accomplished with wire bonds. Through silicon via (TSV) technology has been proposed as an alternative interconnect technique that will reduce assembly complexity of ASIC packaging by replacing wire bonding with flip-chip bonding. TSV technology is advantageous in large detector arrays where TSVs enable close detector tiling on all sides. Wafer-level probe card testing of TSV ASICs is frustrated by solder balls introduced onto the ASIC surface for flip-chip bonding that hamper alignment. Therefore, we developed the ASIC test stand (ATS) to enable rapid screening and characterization of individual ASIC die. We successfully demonstrated ATS operation on ASICs originally developed for CdZnTe detectors on the Nuclear Spectroscopic and Telescope Array (NuSTAR) mission that were later modified with TSVs in a via-last process. We tested both backside blind-TSVs and frontside through-TSVs, with results from internal test pulser measurements that demonstrate performance equal to or exceeding the probe card wafer-level testing data. The ATS can easily be expanded or duplicated to parallelize ASIC screening for large area imaging detectors of future space programs. © 2022 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: 10.1117/1.JATIS.8.3.036001]

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1 Introduction and Motivation

Wide-field coded aperture hard x-ray telescopes enable the discovery and characterization of the most energetic and transient astrophysical phenomena in the universe, including gamma-ray bursts, outbursts from supermassive black holes with jets (blazars), black hole and neutron star binary mergers, and outbursts from black hole and neutron star x-ray binaries. A next-generation instrument under development is the High-Resolution Energetic X-ray Imager (HREXI). HREXI is a CdZnTe (CZT) imaging hard x-ray (3 to 300 keV) detector designed to identify and localize transient astrophysical events. Drawing on heritage technology developed during the ProtoEXIST I & 2 balloon-borne x-ray telescope experiments, spinoff HREXI is composed of a modular array of 256 closely tiled pixellated 19.9 × 19.9 mm², 3-mm-thick CZT detectors. Each CZT detector, with an example shown in Fig. 1(a), is bonded to an individual application-specific integrated circuit (ASIC) with gold studded conductive-epoxy. Previously developed and flown on the the NuSTAR mission, the NuSTAR ASIC (NuASIC) readout enables tiling of large detector area assemblies for coded aperture imaging, which is depicted in Fig. 1(b). While NuSTAR operates eight individual detectors (2 × 2 for each of the two focusing telescopes), a coded aperture x-ray telescope requires orders of magnitude more detectors to achieve...
the desired sensitivities over a larger field of view. Fabrication, testing, and assembly of hundreds of CZT and NuASIC detectors will be labor intensive and every improvement to the integration process will result in large reductions to schedule time and cost. To overcome this challenge, the HREXI program plans to replace NuASIC wire bonds with through silicon vias (TSVs). In this paper, we detail efforts to streamline screening and testing of TSV NuASICs before bonding to CZT.

Wire bonding is a standard space-qualified technique for connecting integrated circuits with other electronics that are commonly used for detector and sensor integration. Wire bonds are thin gold wires attached to pads on the NuASIC’s surface, which are each connected to staggered pads on a frontend electronics board beneath. The use of exposed wire bonds has a number of drawbacks, including vulnerability to damage, that complicate the safe integration of large detector planes. Attempting to protect wire bonds through encapsulation will add additional processing and integration time for each detector unit. Furthermore, the frontend board must be larger than the NuASIC to provide room for bonding, creating gaps between individual NuASICs, which quickly scales the size of large detector arrays. The necessary gaps between detectors also introduce spatial nonuniformity in the instrument background by allowing x-rays to penetrate the detectors through the side walls of the CZT crystals. Wire bonds may also act as a source of electrical noise pickup during detector operation. Due to these disadvantages, we explore an alternative interconnect solution for large area tiled detector arrays.

TSVs offer an alternative to wire bonds for connecting each NuASIC to the readout electronics system. TSVs are metallized vias that connect the wire bond pads on the top surface of the NuASIC with a double row of flip-chip bond pads on the bottom surface. These TSVs are depicted in a NuASIC in Fig. 2. These new pads can then be easily flip-chip solder-bonded to a frontend.

![Fig. 1](image1.png)

(a) A single detector crystal unit (DCU) of a CZT crystal bonded with conductive epoxy to a NuASIC. The NuASIC is wire bonded to a frontend PCB to power and control the detector. (b) Computer aided design model of the HREXI coded aperture instrument, composed of tiled arrays of 2 x 2 DCUs. Flip-chip bonding TSV NuASICs allows for tightly packed detector spacing.

![Fig. 2](image2.png)

A depiction of backside blind-TSVs that connect the single row of wire bond pads on the NuASIC’s top surface with a double row of flip-chip bond pads on the NuASIC’s bottom surface. The flip-chip bond pads are offset to prevent the attached solder balls from merging together during attachment.
board below the NuASIC, removing the need for wire bonds entirely. This eliminates the handling and tiling concerns introduced by the wire bond contacts. In a “via-last” approach, the NuASIC’s 8-in. silicon wafers are mounted to a carrier wafer for mechanical stability before thinning, etching, and metallization, as described in Ref. 7. After TSV implementation, traces and pads are plated to the back side of the NuASIC before lead solder balls are deposited on the NuASIC pads for later flip-chip bonding. Finally, the carrier wafer is detached and the new TSV NuASICS are diced into 49 individual devices. The additional TSV processing will likely reduce the overall yield of NuASICS per wafer. Further testing of the functionality of each TSV NuASIC must therefore be performed prior to detector bonding to a frontend printed circuit boards (PCB) and CZT.

For NuSTAR, testing of NuASICS was performed at the wafer level by carefully aligning a probe card over the 87 (225 μm pitch) wire bond pads for the power, command, and signal lines of a single NuASIC. After confirming successful NuASIC operation, a diagnostic test was performed with an internal test pulser to probe the functionality and resolution of each of the device’s 1024 pixel channels. Testing NuASICS on the wafer sequentially required the time-consuming realignment of the test probe card over each device. This testing process was suitable for the NuSTAR mission, which ultimately selected the eight best candidate NuASIC/CZT detectors, but is untenable for wide-field coded aperture detector arrays like HREXI. The difficulties with probe card testing are exacerbated by the addition of solder balls for flip-chip bonding on the backside of the NuASIC. The rounded surface and uneven heights of solder balls disrupts probe placement and creates uncertainties in alignment. Considering the reduced NuASIC yield from the via-last TSV insertion process, the disadvantages of traditional probe card testing, and the benefits of testing individual TSV NuASICS prior to bonding, we designed and produced the ASIC test stand (ATS).

2 NuASICS Testing Requirements and ATS Design

The ATS is designed to support rapid testing of unattached TSV NuASICS. TSV NuASICS have a single row of 87 wire bond pads for command, data, and power on the top surface. Conductive TSVs connect these pads to two staggered rows of traces along an edge on the bottom surface of the NuASIC for flip-chip bonding. The bottom surface of the NuASIC along with the device’s flip-chip bonding pads can be seen in Fig. 3. These two offset rows of contacts have a 450 μm pitch (225 μm trace pitch) and a 138 μm × 230 μm pad size. In addition, a grid of 16 × 16

![Fig. 3 Bottom-side view of the TSV NuASIC. 87 power, readout, and commanding traces and pads are arrayed in two staggered rows across the top edge of the NuASIC with a 450 μm pitch between adjacent pads in a row. 16 × 16 “dummy pads” (no connections) fill out the remaining area with a 1.209-mm pitch and are used for flip-chip bonding to the readout board.](image)
(1.209 mm pitch) 188 \( \mu m \times 188 \mu m \) unconnected “dummy” pads used in the flip-chip bonding process are distributed across the bottom surface of the NuASIC. Each of the 87 operating lines and 256 dummy pads have attached solder balls. The solder balls settle at different heights (with a \( \sim 12 \, \mu m \) tolerance) on the operational pads and dummy pads due to the difference in pad sizes affecting the solder spread. The variance in solder ball height and tight pitch requirements of the NuASICs necessitates a specialized fixture for rapid testing. Finally, the wafer dicing process introduces die-to-die variance (estimated at 50 \( \mu m \)) in NuASIC dimensions. Any designed test fixture must be adjustable to account for these NuASIC shape irregularities.

The ATS utilizes a micropogo probe test socket to meet the testing requirements imposed by the TSV NuASIC. Micropogo probe testing fixtures have been used for ASIC testing across many architectures. Micropogo probes are conductive, spring-loaded contacts that make temporary connections to the NuASIC. The test socket is composed of the micropogo probes and a probe guide, which are depicted in Fig. 4. Each micropogo probe compresses independently to accommodate the variance in solder ball height and curvature. A micropogo probe guide encapsulates the spring structure of the probe, fixing the alignment to match the NuASIC pitch requirement while also limiting transverse deflection of the probes during vertical compression. The micropogo probes selected for the ATS were designed and produced by AlphaTest Corp., which specializes in fine-pitch test sockets. The micropogo probes have crowned 140 \( \mu m \) diameter heads that cup directly onto the NuASIC solder balls, whereas the flat 203 \( \mu m \) diameter ends of the pins are mounted onto pads on the ATS’ readout board. Long 5.1-mm micropogo probes were selected to offset the TSV NuASIC from the surface of the ATS test board, allowing a gap between ASIC and test board for edge-on monitoring of alignment and compression with USB microscopes as shown in Fig. 5(b). Each micropogo spring can maximally travel 700 \( \mu m \) but the probe guide limits compression to 350 \( \mu m \) to preserve spring health and limit force on the

![Fig. 4](image-url) (a) Diagram of the AlphaTest micropogo probe S200 series with crown-tip. (b) An array of 6 \( \times \) 6 micropogo probes at 1.2 mm pitch encapsulated in the micro-pogo probe guide (orange) and mounted to an ATS test board. (c) Image of several micropogo probes of the 87 needed for NuASIC readout. These 140 \( \mu m \) diameter micropogo probes can compress up to 350 \( \mu m \). (d) Diagram of a micropogo probe within the probe guide structure. The probe guide encapsulates the probe spring while allowing the tip of the probe to make contact with the NuASIC and compress.
NuASIC. In addition to an array of 87 micropogo probes for the TSV NuASIC readout, two arrays of 6 × 6 probes make contact with dummy pads at the opposite edge of the TSV NuASIC. This distributes the compression force across the TSV NuASIC surface preventing the device from shifting. The variety of micropogo probes available from AlphaTest Corp. has also allowed the construction of a secondary micropogo test socket with pointed probes. This allows for testing NuASICs without solder balls in the event another integration mechanism is chosen instead of flip-chip bonding.

The ATS is a mechanical fixture designed to control the alignment and contact force of the micropogo probe test socket with the TSV NuASIC under test. Figure 5(a) contains an image of the ATS and its components. The TSV NuASIC is placed flat on an electrostatically dissipative (Semitron ESD-225) surface. An L-bracket is machined into the surface, which assists with TSV NuASIC alignment. In addition, the placement of the TSV NuASIC can be secured by a vacuum chuck located below the ESD-225 plate and routed through holes to the ASIC. In practice, the use of vacuum to secure the TSV NuASIC has not been required. The alignment of the micropogo probe test socket is adjusted relative to the TSV NuASIC’s position by a micrometer-controlled two-dimensional horizontal translation stage and a rotational stage. To guide and confirm alignment, two USB microscopes were used to allow us to observe the solder ball and micropogo probes edge-on as the test socket is lowered by a vertical micrometer stage. One microscope confirms alignment of the 87 solder balls while the second is used along the adjacent edge to adjust the micropogo probes relative to the two offset solder ball columns and dummy pads. Top-down USB endoscopes are incorporated into the design to align the ATS with fiducial points on the surface of the TSV NuASIC. These endoscopes typically are only used when solder balls are not present on the TSV NuASIC surface, which makes edge-on alignment confirmation difficult. The TSV NuASIC test procedure is sensitive to light and other electromagnetic interference, so exposure is prevented by a light-tight grounded aluminum cover that is put in place after TSV NuASIC alignment and compression. Once the NuASIC is in contact with the micropogo pin test socket and has been covered, testing is controlled through the ATS test board.

The ATS test board in Fig. 6 is composed of the micropogo probe test structure, a complex programmable logic device (CPLD) and passive components that form a low-pass power filter for both the CPLD and NuASIC. The CPLD handles low-level NuASIC signaling and passes user commands to the NuASIC from a commercial-off-the-shelf field programmable gate array (FPGA) that sits behind a power isolation barrier on a secondary board. Data from the NuASIC are passed through the CPLD off the ATS test board to the FPGA board where it is buffered. The FPGA handles the event data packaging for the final data product and passes both data and
commands serially over USB with a user-controlled computer. Test pins on the ATS test board allow for confirmation of proper connection with the TSV NuASIC by confirming low resistivity measurements between the CPLD and TSV NuASIC ground planes.

On the ATS, the test board drives TSV NuASIC evaluation via an internal test pulser. During testing, the NuASIC test pulser injects charge into selectable contiguous arrays of the 1024 NuASIC pixels. This injected charge mimics the charge collection pathway of a NuASIC bonded to CZT when exposed to an x-ray event. The current induced by the injection of this charge is copied sequentially to a series of 16 capacitors on the NuASIC. The collected charge on each capacitor is digitized in an on-chip digital-to-analog converter and read out by the detector control system. In the most stable testing configuration, $4 \times 4$ pixel regions on the TSV NuASIC are stimulated sequentially with the test pulser for several minutes. All 1024 NuASIC pixels can be well-characterized within 30 min, and the data can be used to produce a report of individual pixel health status, resolution, and gain.

3 Performance of NuASICs Tested through the ATS

We have successfully used the ATS to test TSV NuASICs modified by both backside blind TSVs and frontside through TSVs incorporated through via-last processes. Backside TSVs are implemented from the bottom of the NuASIC by inserting a single 100 $\mu$m diameter by 300 $\mu$m deep tapered cylindrical TSV that touches down directly onto the back of each of the wire-bond pads on the top surface. Figure 7 displays a full internal pulser scan of a backside TSV NuASIC performed by sweeping the internal pulser across the $32 \times 32$ NuASIC pixels in a $4 \times 4$ grid and collecting data from the triggered channels. “Hot” (noisy) pixels or unresponsive pixels are filtered out from the image to determine the overall number of functioning pixel channels in the device, resulting in 1022 active pixels out of 1024 for the device under test. The scan also reports the mean analog-to-digital unit (ADU) value of each pixel channel with an ADU value of 1230 corresponding approximately to a 130-keV x-ray event. The resolution of each pixel as a full-width at half-maximum (FWHM) percentage of the ADU is also mapped in Fig. 7. A histogram of gain-corrected FWHM resolutions of the 1022 active pixels from the backside TSV NuASIC is shown in Fig. 8(a). We find an average gain-corrected resolution of (0.54% FWHM) in the ATS tested backside TSV NuASIC. Performing an identical analysis on a smaller set of data from NuASIC internal pulser testing with a traditional wafer-level probe card station yielded a
gain-corrected FWHM of 2.69% with the supporting histogram found in Fig. 8(b). The comparison of the two data sets is limited by the relatively small amount of pixels tested with the wafer-level probe card while performing rapid testing across multiple NuASIC devices, but these results indicate that the testing performance of the ATS is stable and a capable replacement to traditional probe card testing.

Challenges with implementing the backside TSVs successfully\textsuperscript{7} led to the exploration of a frontside through TSV design with Micross Advanced Interconnect Technology.\textsuperscript{13} In this process, three 20 μm diameter TSVs are etched adjacent to each of the wire bond pads, then revealed on the backside of the NuASICs through a polishing and etching process before backside traces are deposited. The first run of the frontside TSV NuASICs tested with the ATS produced a functioning device yield of ~30%. While these devices returned high resolution pulser spectra at first, the functionality of the frontside TSV NuASICs degraded quickly with increasing current draws, becoming unresponsive in ~10 min of operation time.\textsuperscript{7} We suspect that the degradation in device performance is caused by insufficient insulation layer thickness within the NuASIC TSVs, leading to electrical shorting. This performance degradation has been observed both with the ATS and with probe card testing at the wafer level and is currently being further studied.

While this degradation prevented a full ATS scan of a frontside TSV NuASIC, we performed limited testing on regions of pixels without pixel-by-pixel gain calibration and with the aggregate gain-corrected FWHM of 2.69% with the supporting histogram found in Fig. 8(b). The comparison of the two data sets is limited by the relatively small amount of pixels tested with the wafer-level probe card while performing rapid testing across multiple NuASIC devices, but these results indicate that the testing performance of the ATS is stable and a capable replacement to traditional probe card testing.

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spectral resolution of the internal pulser reported in Fig. 9. These selected pixel patches were two $8 \times 8$ pixel regions on opposite corners of the frontside TSV NuASIC and were chosen to include a similar number of pixels to the pixel patches reported in Ref. 7 for comparison of gain-uncorrected results. The mean 1120 ADU value reported in pixel patch 1 would correspond to $\sim 118$ keV event for a bonded detector. Between pixel patch tests, we observed a shift in peak ADU value of $\sim 30$ ADU, which may be a result of the device’s changing performance. The pixel patches’ gain-uncorrected spectral resolution yielded 1.7% FWHM and 1.4% FWHM, respectively, similar to the 2.6% FWHM and 3.2% FWHM resolution results from wafer-level testing performed and reported in Ref. 7. Due to the degradation of the devices under test, no frontside TSV NuASICs were successfully examined with both wafer-level probe card testing and die-level ATS testing. The differences in reported gain-uncorrected pixel patch FWHM resolution can be explained by independent NuASIC device and pixel channel variance.

TSV NuASICs were inspected before and after testing with the ATS to determine if the compression forces from using an array of micropogo probes could damage the devices. Of particular concern were the frontside through TSV NuASICs, as the TSV implementation process results in additional thinning of the devices to expose the vias. However, no damage to the TSV NuASICs silicon was observed, whereas repeated compression on both TSV NuASICs pads and solder balls only resulted in slight indentations. We previously confirmed while operating the micropogo pin test socket and ATS that a limited probe compression of 50 to 100 $\mu$m is necessary to achieve sufficient probe contact with the TSV NuASIC, reducing the compression force necessary for testing.9

4 Summary and Future Development

We have successfully designed, constructed, and tested the functionality of a die-level test stand that will allow for the rapid screening of individual TSV NuASICs. This assures that low-noise NuASICs can be selected for integration into HREXI’s closely tiled CZT/TSV NuASIC $16 \times 16$ imaging detector array for a wide-field coded aperture x-ray telescope at lower cost, risk, and complexity than previous wire bonds designs. The ATS allows for rapid pixel-to-pixel channel calibration of the $32 \times 32$ pixels of each TSV NuASIC. The ATS will be valuable as the development of the frontside through TSV NuASIC process continues, offering rapid testing of NuASIC die to determine wafer yield and functionality. In addition, a secondary operating mode available on the NuASIC allows the detector to achieve greater spectral resolution at low (3 to 5 keV) x-ray energies at the cost of leakage current sensitivity. This secondary operating mode, currently used...
on the NuSTAR mission, has tunable parameters that must be adjusted for improved operation prior to launch. The ATS will serve as an integral testbench for the parameter adjustments necessary to operate the TSV NuASICs in this mode.

HREXI will require the evaluation of more CZT/NuASIC detectors than any previously launched instrument. While the ATS successfully minimizes the necessary human resources for testing via rapid alignment capabilities, the NuASIC testing duration is dominated by the pixel pulser scan, which can take up to 30 min to achieve reasonable spectral resolution statistics. For HREXI’s proposed 256 unit CZT/TSV NuASIC detector array, the testing of all individual NuASICs will take nearly a week. To accommodate this, the ATS can be duplicated to allow for parallel testing of multiple NuASICs.

The development of a future SmallSat Constellation capable of full-sky hard x-ray monitoring will further expand detector testing requirements. Continued ATS development will fine-tune micropogo probe test fixtures with smaller probe diameters and finer pitch for testing successor ASICs with 2x finer spatial resolution (64 × 64 pixels). These advances in ATS development will promote generalization of the test stand to future, higher resolution ASICs that will be used in next-generation instrument designs.

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Daniel P. Violette is a graduate student at Harvard University working with the High-Resolution Energetic X-ray Imager (HREXI) team, with interests in high-energy time domain astrophysics and instrumentation. He is supported by the Future Investigators in NASA Earth and Space Science and Technology (FINESST) Fellowship to further develop HREXI detector sensitivity at low energy thresholds.

Branden Allen received his PhD in physics from U.C. Irvine in 2007 and is currently a senior research scientist at Harvard University with over 20 years of experience in the development, deployment, and operation of ground- and space-based telescopes for high-energy X/γ-ray astronomy and planetary science. His current research is focused on the development and deployment of next-generation detector systems and telescopes to probe high energy astrophysical phenomena and for future planetary exploration.

Jaesub Hong is a senior research scientist at Harvard University. He has nearly 20 years of experience in development of x-ray telescopes for high energy astrophysics and planetary science. His current focus is the development of advanced hard x-ray detectors for next-generation wide-field hard x-ray telescopes for time-domain astrophysics and the miniature lightweight x-ray optics for planetary science. He received his PhD in physics from Columbia University. He has (co)authored over 40 publications.

Hiromasa Miyasaka is a staff scientist at California Institute of Technology. He received his PhD in physics (2000) from Saitama University in Japan. He has over 20 years of experience in development of particles and x-ray detectors for the cosmic ray and high-energy astrophysics. Since 2006, his work has focused on CdZnTe and CdTe detectors and readout ASIC development. He is one of the primary detector scientists for the NuSTAR mission.

Jonathan Grindlay is the Robert Treat Paine professor of astronomy at Harvard. He received his BA degree in physics from Dartmouth (1966) and his PhD in astrophysics from Harvard (1971). He joined the faculty in 1976 and chaired the Department in 1985 to 1991 and 2001 to 2003. His primary interest is black hole time variability, accretion physics, accreting black hole (both stellar and supermassive) populations, and formation as measured with wide-field coded aperture imaging x-ray telescopes (ultimately full-sky) and optical/IR imaging/spectroscopy. He has over 434 refereed journal papers.