Survey of key technologies on millimeter-wave CMOS integrated circuits

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Abstract. In order to provide guidance for the development of high performance millimeter-wave complementary metal oxide semiconductor (MMW-CMOS) integrated circuits (IC), this paper provides a survey of key technologies on MMW-CMOS IC. Technical background of MMW wireless communications is described. Then the recent development of the critical technologies of the MMW-CMOS IC are introduced in detail and compared. A summarization is given, and the development prospects on MMW-CMOS IC are also discussed.

1. Introduction

Millimeter-wave (MMW) is an electromagnetic wave between the microwave and the far-infrared wave, the millimeter-wave band is 30-300 GHz. MMW has great significance in communication, radar, navigation, remote sensing, radio astronomy, and biomedical spectroscopy. With the rapid development of microelectronics technology and the growth of military demand, millimeter-wave monolithic integrated circuit (MMIC) became a new type of integrated circuit that integrates multiple field-effect transistors and other components on a single chip. In order to meet the requirements of high-speed wireless applications, such as high-speed wireless personal area network, vehicular radar, Gigabit point to point link connection [1] etc. The 60 GHz band have been opened despite without international non-license, such as 59-66 GHz in Japan and 57-64 GHz in the United States. For III-V semiconductor technology, such as GaAs and InP, although it has high electron mobility, resistivity and superior performance, the silica-based complementary metal oxide semiconductor (CMOS) has mature progress with low power consumption and low cost. The maximum oscillation frequency fmax and the characteristic frequency ft has been improved with the CMOS process size decreasing, which make the application of CMOS process of the millimeter wave turn possible [2] According to the International Semiconductor Technology Blueprint (ITRS) that give the RF/Analog CMOS evolution route, the characteristic frequency of the CMOS process exceeded the InP in 2009, exceeding the SiGe in 2014 [3], as shown in Figure 1. With the CMOS technology characteristics of the size of the shrinking and working frequency improved, making the millimeter-wave CMOS integrated circuit technology continues to upgrade, it has become a hot spot in the field of MMIC.
The key technology to research the design of MMW-CMOS integrated circuits is to establish accurate and effective CMOS active and passive device models. The ordinary device model will inaccurate when the working frequency of the CMOS process enters the millimeter wave band. The modeling of MMW-CMOS IC mainly includes CMOS field-effect transistor modeling and transmission line modeling which include microstrip line and coplanar waveguide (CPW) modeling etc. This paper summarized key technologies of MMW-CMOS IC, introducing wireless communication technology in the field of millimeter wave, and describing several key techniques for MMW-CMOS IC, and then, the key technologies of MMW-CMOS IC are introduced and compared in detail, furthermore, the future researching direction of the MMW-CMOS IC is prospected and the goal of the MMW-CMOS IC is reviewed.

2. Research on key technologies of MMW-CMOS IC

2.1. Research on de-embedding method in microwave measurement

In the microwave circuit, it is necessary for us to accurate measurement of related devices. In order to get accurate measurement results, it is important that design accurate fixture, meanwhile, the parameters of the device must be deducted from the fixture parameters, which can be called to de-embedding. Using the equivalent circuit to characterize the fixture parameters, this embedding method is point at production of millimeter-wave integrated circuit that base on Inpand GaAs process. With the operating frequency of the integrated circuit reaching the microwave frequency band, a variety of parasitic parameters and skin effect become obvious, thus, it is difficult to use a simple equivalent circuit structure to accurately characterize fixture parameters [4], especially for CMOS integrated circuits, the traditional de-embedding method cannot accurately reflect the microwave characteristics of silicon-based devices, we need to improve the method in the relevant device modeling.

The method of de-embedding including Line-Reflect-Line (LRL) [4], Short-Open-Load-Reciprocal (SOLR) [5], Thru-Reflect-Line (TRL) [6], Line-Reflect-Match (LRM) [7], with the rapid development of CMOS technology, the traditional method of de-embedding is no longer suitable. In 2000, Kolding [8] introduced four-step CMOS device de-embedding, it takes into account substrate loss and contact effects. Using simple texting structure to complete four steps containing open circuit, simple short circuit, open circuit, and short circuit, we can get accurate result. Rosales et al. [9] proposed a de-embedding method based on on-chip spiral inductor modeling, the method employ open, left-short, right-short and penetrated four virtual structures to achieve function, and finally using 0.25 μm CMOS process to verify its accuracy. Niu et al. [10] compared the four-port de-embedding and verifying it in the frequency range of 2-110 GHz with a CMOS process, and using the NMOS as a DUT to test, as shown in Figure 2. Issakov et al. [11] used a new two-port de-embedding technique for differential device modeling and fabricate 2:1 differential transformers and on-chip Thru-Line (TL) with 0.13 μm CMOS process, Thru-Line-Reflect (TLR) virtual structure, and then used the de-embedding of TL and
TLR to test the transformer S parameters. South Korea's Samsung Electronics related researchers [12] proposed a five-step de-embedding (Pad, Pad-Short, Pad-Open, Short, Open), the five virtual structures were verified by gate electrode resistance and input capacitance of transistor based on 45 nm CMOS process, the results show that the five optimized virtual structures can eliminate the parasitic parameters which generated by pad and metal traces.

![Diagram](image1)

**Figure 2.** The proposed four-port de-embedding method in Ref. [9].

2.2. Research on modeling method of MOS field effect

The traditional CMOS model provides accurate simulation results in low frequency bands, such as BSIM3 (developed by the University of California, Berkeley Device Research Group), and MOS9 [1] (developed at the Philips Research Laboratory in the Netherlands). However, these CMOS transistor model simulation results appear to large error when the frequency reach to the millimeter-wave band, so how to apply them to the millimeter-wave band what is a very big challenge [2]. It has been theoretically analyzed that $f_{\text{max}}$ is independent with the fingers number of multi-finger transistor, so the maximum operating frequency $f_{\text{max}}$ of the transistor can be optimized with a single-finger transistor, the layout as shown in Figure 3. A series of resistance and inductive parasitic parameters will become more important when the operating frequency in the microwave frequency band, therefore, these parasitic parameters should be considered in the transistor modeling, the impact of capacitance also cannot be ignored. In the microwave frequency band, the transistor model working is generally divided into the external parameter part and the part of kernel, the external parameter part is the parasitic parameter generated at the high frequency, the part of kernel is the traditional transistor model, as shown in Figure 4. After the model is established, the parameters of the CMOS transistor are extracted by Agilent IC-CAP [13] and Agilent ADS Momentum electromagnetic simulation [14]. The accuracy of the former is higher than the latter owing to necessarily testing transistor layout. The latter parameters need to be extracted directly from the measured data, but the bias conditions are limited.

![Diagram](image2)

**Figure 3.** The single-finger physical model of NMOS devices.
At present, people have made a relatively rich research on the CMOS transistor modeling, as early as 2001, Hsu et al. [15] optimized the layout of CMOS and introduced deep wells, which make and of 0.18 μm CMOS process transistor respectively reach to 70 GHz and 58 GHz. In 2007, Zhu et al. [16] directly extracted the values of the parasitic elements from the physical map of the MOSFET, and the layout was designed by using the NMOS field-effect transistor of 0.18 μm CMOS process. The simulation shows that the model can achieve high-frequency performance of NMOS from 100 MHz to 40 GHz, Dr. Liang and Professor Razavi [17] proposed a folding transistor of physical model, as shown in Figure 5 (a), the model describes the metal capacitance between the transistor stages, as
shown in Figure 5 (b), through the new layout technology to reduce these capacitors which can improve the performance of the circuit.

2.3. Research on modeling transmission line
In the millimeter-wave CMOS integrated circuit, the main structure of the transmission line is the microstrip line (MSL) and Coplanar Waveguide (CPW). Since the traditional transmission lines are primarily modeled on processes such as GaAs, the principle of propagation will be different from the CMOS process. Therefore, it is particularly important to model the standard CMOS process (the substrate is silicon) transmission line, which will be described in detail. After model is completed, it is necessary to establish the equivalent model of RLG parasitic parameters, and finally use the electromagnetic simulation software (ADS or HFSS) to extract the parameters, the characteristic impedance range, quality factor Q and other parameters.

2.3.1. Research on modeling method of MSL.
MSL is a planar transmission line. Compared with CPW, it has wider band, higher reliability, smaller size, light weight and lower manufacturing costs, however, the capacity of power is smaller and larger power consumption. Si-based microstrip line use the underlying metal as the ground plane and the top metal as a signal line, substrate has a SiO₂ passivation layer protection. The MSL was manufactured by standard CMOS process which have biggest drawback the signal line is close with the ground surface, it makes the distributed inductance turn small and reducing the inductance Q. When the Si-based CMOS process achieve active and passive devices, due to the high loss of silicon substrate between the interaction of electromagnetic field, resulting a large number of substrate losses, to improve it, the relatively thin electrolyte passivation layer was used to modify the traditional transmission line (usually using SiO₂), and other also can be used such as benzo cyclobutene (BCB) and polyimide etc. Wu et al. [18] improved the traditional thin film transmission line by placing the Si substrate under the ground, and put four pads on the dielectric layer (passivation layer) for measuring. In order to research the lumped parameters of the relevant TFML, they use less than 1V voltage to measuring and get accurate parameter values. Lee et al. [19] proposed an external processing method based on Magnetorheological Fluid, which can achieve lower loss of high frequency transmission lines. This paper proposed two transmission lines with 20 μm polyimide dielectric layer by magnetorheological surface processing method, which can effectively reduce the loss but raising processing expense. Chiang et al. [20] designed a Quasi-TEM transmission line by using a 0.18 μm 1P6M CMOS process, which was called a Complementary-conducting-strip transmission line (CCS TL). The CCS TL unit consisted by six layers of metal and one layer of dielectric (MD), and then used a number of CCS TL units to form a comprehensive zigzag CCS TL. The simulation showed that the transmission line can obtain wide impedance range (8.62-104.0 Ω), the maximum value of slow wave factor was 4.79, the transmission line area and the quality factor Q ratio was constant when the transmission line length was determined. In 2015, Sang et al. [21] proposed a compass transmission line, which characterized with a multi-metallization 65 nm CMOS process, the model, achieving 50 Ω characteristic impedance, getting coefficient of about -27 dB up to 80 GHz and reducing lower insertion loss. In 2017, Zhu [22] introduced an arrowed dielectric microstrip line which put concentrate a dielectric transmission line that consisted by three dielectric substrate layers. Its excellent performance such as ease of fabrication, and low loss make it become suitable for MMW applications.

2.3.2. Research on modeling method of CPW
CPW, all conductors are connected in the same plane, easily realizing the connect with active and passive device. Its propagation mode belongs to quasi-horizontal electromagnetic mode (Q-TEM), CPW has no cut-off frequency, the impedance characteristics is independence of dielectric layer, which is determined by the ratio of the signal line width to the seam widthso that you can freely design its size, compared with microstrip line, it has many advantages such as the smaller dispersion, less loss, higher efficiency. Based on the optimized slot-type floating shields technology of which slow-wave CPW structure is proposed by TSMC and related researchers in Taiwan Jiaotong University with 45 nm CMOS process [23], as shown in Figure 6 (a). The first study shows that the propagation
wavelength, attenuation loss and characteristic impedance of CPW can be adjusted by changing the protective layer length (SL), band spacing (SS) and protective layer metal type. The measurement results show that the CPW with the gap-type floating protection structure can reduce the silicon-based area by 67%, compared with the traditional structure, there are more than 9 effective dielectric constants and the quality factor more than 6. In order to obtain a higher quality factor, Kaddour et al. [24] simplified the slow-wave CPW structure with gap-type floating protection, as shown in Figure 6 (b), removing the dielectric layer and using a 0.35 μm CMOS process to realize simple structure, small size, good performance and so on. The effective dielectric constant up to 48 and the quality factor reaches 20-40 in range 10 GHz from to 40 GHz.

2.4. Research on modeling method of inductance
In the MMW-CMOS IC, inductors are widely used in low-noise amplifier (LNA), mixer, voltage-controlled oscillator (VCO), filter and other devices. With the development of CMOS technology and shrinking area of chip, requiring the inductance turn smaller, external inductors or active inductors are difficult to be realized. Because the traditional spiral inductor has big area and higher power consumption, which affect the performance of the various components of the integrated circuit, so the designing high self-resonant frequency (SRF) and high-quality factor Q inductance become essential task. Cao et al. [25] developed a differential circular helix inductance based on the traditional spiral inductor structure by using a 0.13 μm CMOS process, as shown in Figure 7, using M1 and POLY to make graphics shield (PGS) and adjusting diameter D to get different inductance and Q value. With development of BiCMOS process, has attract great attention, in 2017, Dickson et al. [26] proposed usage stacked inductor with compact inductor model. Measured results of the first dc to 50 GHz broad-band mixer and 40 GHz VCO with integrated inductors verifies the applicability of spiral structures and the Gilbert cell employed in the broad-band mixer demonstrates for the first time the benefits of a true BiCMOS topology for high-linearity, low-noise, and low-power millimeter-wave circuits.

Figure 6. (a) Slow-wave CPW structure with gap-type floating protection, (b) Simplified form.

Figure 7. Differential circular spiral inductor structure.
3. Discussion and conclusion
In summary, the current MMW-CMOS IC technology still has the following key issues:
First, in the aspect of modeling to establish the de-embedding research. As the operating frequency of integrated circuit devices constantly increase, it is difficult to accurately characterize fixture parameters with simple equivalent circuit structures. In the modeling of MMW-CMOS IC, the traditional de-embedding method should be improved to accommodate the new MMW-CMOS IC structure.
Second, the traditional CMOS reduced model is only suitable for low frequency, when the operating frequency reaches the millimeter wave frequency, the simulation will appear to big error. In the modeling, we must first consider the CMOS parasitic parameters under high-frequency, and then researching model, using the software to extract the parameters of the CMOS transistor, finally complete layout to verify the design.
Third, in the aspect of researching transmission line. Because the traditional modeling principles and CMOS process have different feature, it is obviously initial that utilize standard CMOS process (substrate for the silicon) transmission line modeling. At present, the research on transmission line modeling is mainly aimed at transmission line and CPW research. Although it has the characteristics of small size and high frequency bandwidth, its substrate loss is considerable, the researchers proposed a passivation layer with a thin film transmission line and it reduce substrate loss, however, which increased the difficulty of process, cost and Q value. Due to the CPW easily connecting active or passive devices, this can achieve high Q values that widely used in millimeter-wave integrated circuits. The optimization of CPW modeling is mainly based on the gap-type floating protection technology and propagation wavelength, attenuation loss and characteristic impedance of CPW can be adjust by changing the length of the protective layer, the belt spacing and the protective layer. How we reduce the loss, the complexity of design and improve the Q value still is the focus of the research.
With the size of CMOS process constantly decreasing, the operating frequency of CMOS integrated circuit continues to be improved, MMW-CMOS IC will be moving towards the chip system and MMIC development, making the millimeter-wave baseband processor, transceiver and other modules integrated in a chip be possible. Although there are still many problems with the key technologies of MMW-CMOS IC, the related researching is not yet perfect and CMOS modeling techniques for active and passive devices need to be improve. With the continuous improvement of some key technologies and nanometer CMOS technology is turning mature, we always believe that the CMOS integrated circuit transceiver used in millimeter-wave wireless communication will be developed.

4. Acknowledgment
This work was supported by the National Natural Science Foundation of China under Grants 61504013 and 61702052, and by the Scientific Research Fund of Hunan Provincial Education Department under Grant 15C0033, and the Open Research Fund of Hunan Provincial Key Laboratory of Intelligent Processing of Big Data on Transportation, China.

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