Ultra-Thin SiO2/Si Interface Quality In-Line Monitoring Using Multiwavelength Room Temperature Photoluminescence and Raman Spectroscopy

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Multiwavelength room temperature photoluminescence (RTPL) and Raman spectroscopy were proposed as in-line monitoring techniques for characterizing the dielectric/Si interface. As an application example, ∼7.0 nm thick ultra-thin SiO2 films on 300 mm Si wafers, prepared by various oxidation techniques and conditions, were characterized using multiwavelength RTPL and Raman spectroscopy. Specifically, overall quality of the ultra-thin SiO2/Si interface (including passivation characteristics) and Si lattice stress beneath SiO2 films are investigated. The overall SiO2/Si interface quality was seen to be very dependent on oxidation technique and process conditions. Within wafer and wafer-to-wafer variations of SiO2/Si interface quality were successfully characterized by RTPL and Raman spectra measurements. For electrical analysis of SiO2/Si-based structures, non-contact corona charge-based, in-line (capacitance-voltage (C-V) and stress induced leakage current (SILC)) measurements were performed and compared with RTPL and Raman characterization results. Surprisingly, significant variations in RTPL intensity at and near the corona charge-based measurement sites, indicated that the corona-based electrical measurement technique, though non-contact, was indeed invasive. The effect of corona-charge based electrical measurements on SiO2/Si interface was permanent and even clearly visible from the back side of the wafer. RTPL intensity variations at and near the measurement sites remained, even after a forming gas anneal.

As devices scale to smaller size and complexity of device structures increase, the importance of proper understanding and control of the dielectric/Si interface is increasing. Advanced metal-oxide-semiconductor (MOS) and metal-insulator-semiconductor (MIS) devices employ ultra thin dielectric gate layers. The physical dimensions are in the range of single digit to double digit nanometers. The effective oxide thickness (EOT) is significantly less than 10 nm. Pure SiO2 or combinations of SiO2 and SiN layers are typically used as gate dielectrics. Materials with high dielectric constant (high-k dielectrics) and metal gates are also frequently used, depending on chip design.

Conventional interface characterization techniques, such as high resolution cross-sectional transmission electron microscopy (HRXTEM), Auger electron spectroscopy (AES), secondary ion mass spectrometry (SIMS), X-ray photoelectron spectroscopy (XPS) and non-contact electrical measurement tools (for example, I-V, C-V and carrier life-time measurements) are either destructive or invasive (including methods which are non-contact, but impact dielectric/Si interface quality).1-3 The purpose of all these characterization techniques is to gain useful insights into dielectric/Si in various dimensions or aspects. While the conventional characterization techniques provide very useful information on many properties of the dielectric/Si interface, they appear unable to provide additional clues to some puzzling dielectric/Si interface problems. For example, Si lattice stress (or Si bond length) at or near the dielectric/Si interface, and overall quality of the dielectric/Si interface, including passivation characteristics which strongly affect electronic carrier behaviors at or near the active layer of devices, deserve to be carefully investigated as they can provide technical insights which can meaningfully improve performance and yields from current levels.4,5

Physical dimensions of dielectric layer(s) are typically measured using ellipsometry and high resolution cross-section transmission microscopy (HRXTEM). Electrical characteristics are typically characterized using either contact or non-contact C-V and I-V measurements tools. Non-contact characterization techniques are generally preferred for in-line monitoring applications. However, spatial resolution of non-contact C-V and I-V measurement techniques is in the range of a few millimeters, which is 3 to 4 orders of magnitude larger than typical dimensions of actual devices.6 High spatial resolution, non-contact dielectric/Si interface quality characterization techniques are strongly desired.

In this paper, ultra thin (∼7.0 nm) SiO2 films on Si wafers were prepared by various oxidation techniques and conditions. Dielectric/Si interface quality was characterized by room temperature photoluminescence (RTPL) and Raman measurements. The RTPL and Raman intensity and spectra from Si were measured under different excitation wavelengths, which have different probing depths. Oxidation technique and condition dependency of multiwavelength RTPL and Raman spectra were investigated and examined as a potential non-contact dielectric/Si interface characterization technique with high spatial resolution and the capability of virtual depth profiling of electrically active defects.

Experimental

Ultra thin (target thickness of ∼7.0 nm) gate oxide (SiO2) films were either grown or deposited on prime 300 mm p−Si (100) wafers by a number of different oxidation techniques in a commercial vertical batch furnace and a single wafer processing system in the temperature range of 850 ∼ 950 C. Oxidation temperature, oxygen source, oxidation sequence and wafer temperature ramp rate were varied to investigate the effect of the oxidation conditions on the SiO2/Si interface quality.

Oxide thickness mapping was performed at 225 points per wafer using ellipsometry under a He-Ne laser (633 nm) beam excitation. RTPL intensities and spectra from the dielectric/Si wafers in the wavelength range of 900 ∼ 1400 nm were measured to investigate the effect of oxidation techniques and conditions on the SiO2/Si interface quality. A WaferMasters’ MPL-300 system was used, with three excitation wavelengths (532, 650 and 827 nm) which have different penetration depths (∼1.5, ∼4.0 and ∼10 μm).3,4,10 Penetration depth is a measure of how deep excitation light can penetrate into Si. It is defined as the depth at which the intensity of the excitation light inside the material falls to 1/e (about 37%) of its original value as it propagates into the SiO2/Si interface. For detailed wafer mapping, 15,101 points per wafer per excitation wavelength were measured in 2 mm intervals in both x- and y-directions. Fine pitch x- and y-line scans across the wafer were also done at 559 points in 500 μm intervals. The excitation laser beam spot size was in the range of 50 μm.

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The SiO₂/Si wafers were also characterized by high spectral resolution Raman spectroscopy under various excitation wavelengths using three different visible excitation wavelengths (457.9, 488.0 and 514.5 nm). A WaferMasters’ MRS-300 system was used. The details of the system and its applications can be found in previous publications. Measurements were done in a 180° backscattering geometry under an optical microscope. The excitation laser beam spot size was in the range of ~0.5 μm in diameter. The laser power at the wafer surface was 5 mW to 20 mW. Exposure time was varied from 5 s to 20 s per measurement site, depending on the Raman signal intensity under the specific excitation wavelengths. Ninety-three (93)-point wafer mapping was done under the three excitation wavelengths, for all wafers.

Non-contact, corona charge-based measurements of interface state density (Dᵢₛ) and stress induced leakage current (SILC) were performed on all SiO₂/Si wafers using a corona charge-based electrical measurement tool (FaAST from SDI). The Dᵢₛ was measured at five points, one at the center and four points near the (left, right, top and bottom) edges of the wafer. The SILC was measured at one point near the (bottom left) edge of the wafer. For Dᵢₛ measurements, the contact potential difference between the corona charge deposited electrode and the Si wafer was measured in the dark and under illumination with a light intensity high enough to make surface band bending disappear under illumination. Surface band bending is obtained as the difference between the measurements of the contact potential difference in the dark and under illumination, as a function of the charge deposited at the oxide surface (Qₓ). SILC and gate oxide integrity (GOI) defects on ultra-thin SiO₂/Si were measured under several constant voltage stress levels. The typical bias voltage for the C-V measurement and current density for SILC measurements were 40 mV and 1.0 × 10⁻⁸ A/cm², respectively.

After the routine, in-line, non-contact electrical metrology, RTPL spectra were measured again to investigate whether there was any change in the SiO₂/Si interface characteristics, from an optical characterization point of view.

Results and Discussion

Ultra-thin oxide film growth.— Two identical sets of twelve (12) ultra thin SiO₂ films were either grown or deposited by various oxidation techniques and conditions to ensure the repeatability of the experimental data. The second set of 12 wafers was prepared two weeks after the preparation of the first set of wafers, as a part of process repeatability tests. Oxidation technique, oxidation sequence, oxidation temperature, wafer temperature ramp rate and average oxide thickness of the first set of 12 wafers (measured using ellipsometry) were summarized in Table 1. The second set of wafers showed almost identical oxide thickness and physical properties. Thus, the discussions are based on the first set of 12 ultra thin SiO₂/Si wafers. The thickness of the ultra thin SiO₂ films was in the range of 6.8~∼9.2 nm. Except for wafer L (plasma oxidation followed by in-situ steam generation (ISSG) oxidation in the single wafer processing system), thickness of all SiO₂ films is 7.0 ± 0.2 nm. The oxide film thickness uniformity of 225 point measurements with 10 nm edge exclusion (E.E. = 10 nm) was <1.0% (1σ) in all wafers. The oxidation temperature is defined as the highest temperature set point during oxidation in a commercial vertical batch furnace. The load size was 15 wafers. Wafers A ~ D and I ~ K (7 wafers) were loaded at a lower temperature (~300°C) and heated to the oxidation temperature shown. Wafers E ~ H (4 wafers) were loaded at higher temperatures (600~∼700°C). Wafer L was loaded at room temperature. All wafers were unloaded at the temperature range of 400~∼500°C.

Room temperature photoluminescence (RTPL).— Room temperature photoluminescence intensity is very sensitive to the quality of passivation characteristics of SiO₂/Si. Effective (non-radiative) surface recombination is higher (i.e. minor carrier life-time near the surface is shorter) for SiO₂/Si with poor passivation characteristics and RTPL intensity is weaker as a result. For SiO₂/Si with excellent passivation characteristics, the effective (non-radiative) surface recombination is very low (i.e. minor carrier life-time near the surface is long) and RTPL intensity becomes very strong. The effective lifetime of high quality SiO₂/Si often exceeds 1 ms and photo-generated carriers can travel up to a few millimeters in the in-plane and depth directions. Thus, the RTPL characterization techniques with optical techniques with 1.5 ~ 10 μm probing depths can still be used for in-line monitoring and screening of the dielectric/Si interface quality. The effectiveness of RTPL for monitoring the dielectric/Si interface quality were examined and demonstrated. Details of design concepts and Si and dielectric/Si characterization application examples of the multiwavelength RTPL system used in this study can be found in previous publications.

To gain insights into electronic carrier behavioral properties as an SiO₂/Si interface (passivation) quality factor, RTPL intensity and spectra mapping of the two sets of SiO₂/Si wafers was done under 532, 650 and 827 nm excitation. Figure 1a and 1b show RTPL spectra measured from the center of the first set of SiO₂/Si wafers under 650 and 827 nm excitation. Since the trends of RTPL intensity under 532 nm excitation was more or less the same as 650 nm excitation results and 827 nm excitation. Since the trends of RTPL intensity under 532 nm excitation was more or less the same as 650 nm excitation results and 827 nm excitation results with poor signal-to-noise (S/N) ratios, they are not shown in this paper. Estimated probing depths for Si, under 532, 650 and 827 nm, are ~1.5, ~4.0 and ~10.0 μm, respectively (Fig. 1c). Significant RTPL intensity variations were measured between wafers. Almost no RTPL signal was measured from the wafers A ~ D and I ~ L under 650 nm excitation. The strong RTPL spectra from wafers E ~ H show typical RTPL spectra from a lightly doped Si wafer with high quality surface passivation properties. They generally can be deconvoluted into an

~ 100 μm in diameter. The details of the system and its applications have been published elsewhere. No measurable RTPL signal was observed from most of SiO₂/Si wafers under 532 nm excitation. For 650 nm excitation, the laser power at the wafer surface was 20 mW and exposure time was 1.0 s per point. For 827 nm excitation, the laser power at the wafer surface was 50 mW and exposure time was 50 ms per point.

| Wafer ID | Oxidation Techniques and Sequences | Oxidation Temperature | Loading Temperature | Oxide Thickness |
|---------|-----------------------------------|-----------------------|---------------------|-----------------|
| A       | Radical                           | 850°C                 | Low                 | 7.1 nm          |
| B       | Radical                           | 950°C                 | Low                 | 7.0 nm          |
| C       | Dry + Radical                     | 850°C                 | Low                 | 7.1 nm          |
| D       | Dry + Radical                     | 950°C                 | Low                 | 6.9 nm          |
| E       | Dry                               | 850°C                 | High                | 7.0 nm          |
| F       | Wet                               | 850°C                 | High                | 7.0 nm          |
| G       | Radical + Wet                     | 850°C                 | High                | 6.8 nm          |
| H       | Thermal CVD (SiH₄ based)          | 850°C                 | High                | 6.9 nm          |
| I       | Radical                           | 850°C                 | Low                 | 7.2 nm          |
| J       | Radical + H₂ Bake                 | 850°C                 | Low                 | 7.1 nm          |
| K       | Radical + H₂ Bake                 | 850°C                 | Low                 | 7.1 nm          |
| L       | Plasma Ox. + ISSG Ox.             | 850°C                 | Low                 | 9.2 nm          |
asymmetric band-to-band transition RTPL peak centered $\sim 1140$ nm and a small band tail RTPL peak extended to $\sim 1270$ nm. When the RTPL intensity from SiO$_2$/Si wafers are similar, detailed analysis including deconvolution of RTPL spectra is necessary to identify the possible cause of the difference. For the SiO$_2$/Si wafers with large wafer-to-wafer RTPL intensity variations, simple maximum RTPL intensity comparisons can provide the first order probable cause of wafer-to-wafer variations.

Three dimensional (3D) graphs of RTPL spectra are very useful for understanding spectral change and qualitative comparisons between spectra. However, they make quantitative comparisons somewhat difficult. For easier quantitative RTPL peak intensity comparisons, the RTPL intensity bar graphs are plotted in Fig. 2. The figure shows (a) linear scale and (b) log scale for RTPL peak intensity under 650 and 827 nm excitations, and (c) RTPL intensity ratio ($I_{650}/I_{827}$: 650 nm excitation RTPL peak intensity to 827 nm excitation RTPL peak intensity).

Four ($E \sim H$) out of 12 wafers showed very strong RTPL intensity under both 650 and 827 nm excitation. They are 30 $\sim$ 50 times stronger than the other 8 wafers ($A \sim D$ and $I \sim L$). The 4 wafers $E \sim H$ with higher RTPL intensity were all oxidized by various techniques at 850 $^\circ$C with a higher loading temperature (600 $\sim$ 700 $^\circ$C). The other eight wafers ($A \sim D$ and $I \sim L$) were oxidized by various techniques at either 850 $^\circ$C or 950 $^\circ$C with a lower loading temperature ($\sim 300$ $^\circ$C for batch furnace and room temperature for single wafer chamber). Wafer B and D were oxidized at 950 $^\circ$C (100 $^\circ$C higher than all other wafers). Wafer L had a thicker oxide (9.2 nm as compared to 6.8 $\sim$ 7.2 nm for other wafers) even though the oxidation temperature (850 $^\circ$C) was the same as the other wafers. The higher oxidation temperature and thicker oxide film seem to enhance RTPL intensity, but not as much as the initial oxidation temperature. The higher loading temperature (i.e. higher initial oxidation temperature) seems to be the primary factor for yielding stronger RTPL intensity. The strong RTPL intensity variations (up to 50-fold) for SiO$_2$ films of identical thickness, on prime p$^-$-Si wafers, is quite remarkable. Exactly the same RTPL characterization results were achieved from the second set of 12 wafers prepared under the same oxidation conditions two weeks later. The oxidation results and properties of SiO$_2$/Si interface were almost identical between the first set and the second set of 12 wafers.

The strong RTPL peak intensity variations among wafers strongly suggest that SiO$_2$/Si interface quality plays a very important role in electronic carrier transport properties (mainly minority carrier lifetime and the ratio between radiative and non-radiative recombination of carriers due to the oxidation condition dependency of the passivation characteristics).

An SiO$_2$/Si interface with lower interface state density, interface trap density and good passivation characteristics would yield relatively stronger RTPL intensity. Shorter wavelength excitation RTPL measurements, with shallower probing depth, are more sensitive to SiO$_2$/Si interface quality since the majority of electron-hole pairs are generated near the surface, within the probing depth, and the minority carriers seek (either radiative or non-radiative) recombination partners in the diffusion path. The ratio between RTPL intensities under different excitation wavelengths, with different probing depths, can suggest the degree of SiO$_2$/Si interface quality, bulk crystal quality, and relative location of electrically active sites (such as traps, mid-gap states) as a function of depth from the surface at the measurement site.

The excitation wavelength and initial oxidation temperature dependency of RTPL intensity and spectra suggests significant variations in SiO$_2$/Si integrity and interface quality between the furnace based thermal oxidation conditions. Different initial oxidation temperatures resulted in up to 50-fold RTPL intensity variations under all excitation wavelengths. The SiO$_2$/Si interface quality was significantly influenced by the initial oxidation temperature.
Raman spectroscopy.— Raman spectroscopy can provide crystallinity, lattice stress/strain-related material property information of crystalline solids as a form of inelastic light scattering with phonons. In a 180° backscattering geometry, only one sharp symmetrical Raman peak corresponding to the longitudinal optical (LO) phonon is measured at $\sim 520.3 \text{ cm}^{-1}$ from stress-free Si (100) single crystal. Probing depth of Raman spectroscopy depends on the absorption coefficient ($\alpha$) of Si at a specific excitation wavelength.\textsuperscript{11,12} The Raman signal contains the weighted average of Si lattice condition within the probing depth. The probing depth deepens as the excitation wavelength increases. For ultraviolet (UV) excitation below 400 nm, the probing depth in Si is 50 nm or shallower. The probing depth under visible (VIS) excitation wavelengths (400 – 700 nm) is in the range of 50 nm – 3 $\mu$m. The effect of oxidation conditions on Si lattice properties underneath the thin oxide layer can be investigated using Raman spectroscopy under different excitation wavelengths.

To investigate the effect of loading temperature of the oxidation process, which has caused significant RTPL intensity variations, up to 50-fold, 93-point Raman wafer mapping was done using high resolution, multiwavelength Raman spectroscopy (MRS-300) system under 457.9, 488.0 and 514.5 nm excitation.\textsuperscript{11,12} Probing depths of the three excitation wavelengths in Si (100) wafers with ultra thin (6.8 $\sim$ 9.2 nm) oxide films are illustrated in Fig. 3a. The Raman spectra measured from the center of 12 Si wafers with ultra thin oxide films (A $\sim$ L) under 457.9 nm excitation were plotted in Fig. 3b. All measured Raman spectra were fitted to Lorentzian curves using least square approximation. Intensity, Raman shift and full-width-at-half-maximum (FWHM) values were extracted from the fitted Lorentzian curves. Average intensity and FWHM values of 93-point wafer mapping measurements under the three excitation wavelengths were plotted in Fig. 3c and 3d.

As seen in Fig. 3b, Raman peak shifts (the center of Raman spectra) measured under 457.9 nm excitation were almost identical within the resolution and repeatability of the Raman system (0.01 cm$^{-1}$). The Raman shift values measured from 488.0 and 514.5 nm stayed the same. This implies that the average lattice stress of Si within probing depths of three different excitation wavelengths were almost identical, among all 12 wafers regardless of oxidation conditions. However, the intensity and FWHM values of five Si wafers (E $\sim$ H and L) with ultra thin oxide films measured under 488.0 and 514.5 nm excitation, were statistically different from the rest. The four wafers (E $\sim$ H) have higher loading temperature (600 $\sim$ 700°C) compared to the rest ($\sim$300°C). The wafer L has the highest oxide film thickness (9.2 nm) of all other wafers (6.8 $\sim$ 7.2 nm). It has $\sim$ 28% thicker oxide film than the other wafers. The five wafers (E $\sim$ H and L) with slightly weaker Raman intensity showed broadening of FWHM. Atrial (integrated) Raman intensity of the five wafers may have been almost identical to the other wafers. The broadening of the Raman peak (i.e. FWHM) is responsible for the weakening of Raman intensity (maximum value) of the peak. Since the change of intensity and FWHM were only measured under longer excitation wavelengths (488.0 and 514.5 nm) with deeper probing depths, it is reasonable to assume that the Si lattice stress in bulk Si may have been altered during the ultra thin film oxidation by either high loading temperature and plasma oxidation prior to ISSG oxidation. Only four wafers (E $\sim$ H), loaded at higher temperatures, significantly reduced non-radiative recombination centers and yielded very strong RTPL signal. This strongly suggests the significant increase of SiO$_2$/Si interface quality and/or minority carrier life-time in bulk Si. Raman results showed perfect correlation with RTPL measurement results and provided clear evidence of RTPL intensity enhancement in the four wafers with higher loading temperature.

Performance of electronic devices is strongly related to the important material properties, including minority carrier life-time and mobility. However, there were no direct and convenient in-line material characterization techniques. RTPL and multiwavelength Raman spectroscopy can be very valuable in-line material characterization techniques for identifying hidden property and material property variations.

Non-contact electrical measurements.— To characterize the electrical properties of ultra thin oxide films, non-contact, corona
charge-based measurements of interface state density ($D_{it}$) and stress induced leakage current (SILC) were done on all SiO$_2$/Si wafers using a corona charge-based electrical measurement tool (FAaST from SDI). Non-contact electrical characterization methods make use of corona charging in air to deposit ionic species [positive charged (H$_2$O)$_n$H$^+$ or negative charged CO$_3$$^{2-}$] onto the SiO$_2$ surface. The method can generate oxide fields within a typical range of +7 or −14 MV/cm by controlling the applied corona voltage. The value of $n$ for (H$_2$O)$_n$H$^+$ depends on relative humidity and may range from 2 to 5 for usual conditions.  

Corona charge-based, electrical metrology tools have been in use since the mid 1990’s. They became popular for their convenience (no requirement for sample preparation), reduced metrology cost, and fast feedback. 

In corona charge-based metrology, the deposited ions are thermalized by their long passage in 1 atm air. The corona charging is believed to be a nearly ideal non-destructive (non-destructive and non-invasive) biasing method with no impact on the intrinsic properties of the samples under investigation. 

The $D_{it}$ was measured at five points, one at the center and four points (left, right, top and bottom) mm from the edges of the wafer. The SILC measurements were done at one point near the (bottom left) edge of the wafer. The contact potential difference between the corona charge deposited electrode and the Si wafer was measured for $D_{it}$ characterization both in the dark and under illumination, with a light intensity high enough to mask the surface band bending. The surface band bending is obtained as the difference between the measurements of the contact potential difference in the dark, and under illumination, as a function of the charge deposited at the oxide surface ($Q_{ox}$) by corona discharge. SILC and GOI defects on ultra-thin SiO$_2$/Si were measured under several constant voltage stress levels. The bias voltage of 40 mV and current density of $1.0 \times 10^{-8}$ A/cm$^2$ were used for the C-V measurement and SILC measurements, respectively. Identical $D_{it}$ and SILC characterization results were obtained from all 12 wafers with ultra-thin oxide films grown under different conditions. Corona charge-based C-V and SILC measurements were not able to distinguish the difference in electrical properties of ultra-thin oxide films, regardless of oxidation conditions. 

While corona charge-based electrical measurements are generally believed to be non-destructive and non-invasive, there are a few electron spin resonance (ESR) studies which show the destructive nature of these measurement techniques under high electrical field measurement conditions. For ultra thin oxide films, the electrical field across the films can reach very high values, and may reach a sufficiently critical electrical field strength to affect the as-deposited properties of the SiO$_2$/Si structure. Since the positive corona charging involves hydrogenic species ([H$_2$O)$_n$H$^+$] which are known to interact with the SiO$_2$/Si structure, it could result in modification of the intrinsic properties of the SiO$_2$/Si structure from the as-prepared states.

Side effects of non-contact electrical measurements.— To investigate the effect of Corona charge-based non-contact electrical measurements, RTPL spectra were measured after the routine (in-line and non-contact) electrical metrology, under three excitation wavelengths in the wavelength range of 900 nm ~ 1400 nm (532, 650 and 827 nm) which have different penetration depths (~1.5, ~4.0 and ~10 μm). 

For detailed wafer mapping, 15,101 points per wafer for each excitation wavelength were measured in 2 mm intervals in both x- and y-directions. Fine pitch x- and y-line scans across the wafer were also done at 559 points, at 500 μm intervals. RTPL mapping of all SiO$_2$/Si wafers revealed destructive side effects of the corona charge-based electrical metrology. Either significant RTPL intensity enhancement or deterioration was observed at the corona charge-based non-contact electrical C-V and SILC measurement sites. Average RTPL intensity varied from wafer-to-wafer depending on the oxide film growth techniques and conditions. Figure 4 summarizes auto-scale 2D and 3D RTPL wafer maps and line scan RTPL spectra, in the x-direction, across an 850°C grown, ultra-thin (~7.0 nm thick) dry SiO$_2$/Si wafer under 650 and 827 nm excitation. RTPL measurements were done from both front and back sides of the wafer. Prior non-contact electrical measurement sites were easily recognized from both sides of the wafer. Figure 5 shows the schematic illustration of C-V and SILC measurement sites on the wafer. The back side RTPL maps are mirror images of the front side RTPL maps.
Figure 4. Summary of multiwavelength (650 and 827 nm) RTPL mapping and line scan results of ∼7.0 nm thick dry thermal SiO₂/Si wafer after corona charge-based, non-contact, in-line electrical characterization. RTPL mapping (15,101 points in 2 mm intervals in x and y directions) was done from both front and back sides of the SiO₂/Si wafer. Electrical characterization was performed from the front side only.

The concentric rings in the RTPL maps are due to variations in interstitial oxygen concentration (Oi), oxygen precipitates and/or weak thermal donors in Czochralski Si (Cz-Si) wafers. The ring-like weak RTPL region corresponds to recombination-active regions with shorter effective carrier lifetimes. Since these are bulk effects, 827 nm excitation RTPL measurements, with deeper penetration depths, resulted in clearer signatures on the wafer maps.

The C-V measurement sites were always characterized by a pair of doughnut-shaped enhanced RTPL ring patterns and a small dot with significantly deteriorated RTPL intensity. The inside of the doughnut-shaped RTPL ring pattern showed significant deterioration of RTPL intensity under 827 nm excitation from the front side measurements and all wavelength excitation frequencies from the back side measurements. The doughnut-shaped ring pattern and neighboring dot pattern correspond to the corona-confining ring and reference electrode of the measurement probe. The polarity of corona charge biasing is responsible for the RTPL intensity change at the C-V measurement sites. The SILC measurement site only shows a doughnut-shaped ring pattern at the bottom left in the front side RTPL maps and the bottom right in the back side RTPL maps. RTPL intensity variations at the C-V and SILC measurement sites are higher under 650 nm excitation (penetration depth: ∼4 μm) than 827 nm excitation (penetration depth: ∼10 μm) as seen in the auto-scale 2-D RTPL intensity range (maximum intensity – minimum intensity) maps, fixed scale 3-D RTPL intensity maps and fixed scale RTPL spectra line scans displayed in Fig. 2. This strongly suggests that the C-V and SILC measurements had more impact near the SiO₂/Si interface than in the Si bulk material. Even though C-V and SILC measurements were only done from the front side of the wafer, all measurement sites were clearly visible from the RTPL maps measured from the back side, as well.

Figure 5. Schematic illustration of corona charge-based, non-contact, in-line electrical measurement sites (five C-V measurements and one SILC measurement from the front side of the SiO₂/Si wafer) and its mirror image from the back side. 15,101 point RTPL wafer mapping was done from both sides of the wafer under 650 and 827 nm excitation. 559 point horizontal RTPL line scans across the wafer were done in 500 μm intervals.
RTPL line scan spectra show the Si band-to-band recombination with a center wavelength of ∼1140 nm and weak band tail recombination extended to ∼1260 nm. The RTPL spectra at the C-V and SILC measurement sites showed very large intensity variations while keeping similar spectral distributions as those from the rest of the wafer.

Recombination occurs in the bulk Si as well as on both surfaces of the Si wafers (interfaces of the SiO2/Si wafers). The measured life-time is, in fact, an effective life-time (τeff) which depends on the bulk life-time (τb) and the surface life-time (τs) determined by the recombination velocity S of the Si surfaces (or SiO2/Si interfaces). The effective life-time is given as:

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}
\]

(1)

For a Si wafer with a thickness of W, the surface life-time (τs) can be approximated as follows based on the surface recombination velocity boundary conditions:

\[
\tau_s = \frac{1}{D} \left( \frac{W}{\pi} \right)^2 \quad \text{(for both surfaces with high recombination velocity)},
\]

(2)

\[
\tau_s = \frac{4}{D} \left( \frac{W}{\pi} \right)^2 \quad \text{(for one surface with high recombination and one surface with low recombination velocity)},
\]

(3)

where D is the minority carrier diffusivity.\textsuperscript{21} When the surface passivation quality of at least one side is deteriorated, for any reason, the surface life-time (τs) and the effective life-time (τeff) become shorter.

The life-time for a Si wafer strongly depends on the source material purification method, crystal growth method, crystallinity, dopant and surface passivation quality. It can vary by several orders of magnitude. A good quality, device production grade p<sub>-</sub>Si wafer, with good passivation quality, typically gives an effective life-time >1 ms.\textsuperscript{22,23} In the p<sub>-</sub>Si wafers, carriers can travel up to a few millimeters (more than the thickness (∼775 µm) of a 300 mm Si wafer) without recombination.\textsuperscript{24} Thus, it is not surprising to see the impact of the C-V and SILC measurements at the front of the SiO2/Si interface for the back side RTPL measurements. Since the back side RTPL intensity is affected by many factors, other than the front side SiO2/Si interface quality, the signature of the C-V and SILC measurement sites from the front side is clear.

A lower surface recombination velocity of a high SiO2/Si interface quality makes the effective life-time longer and radiative recombination (i.e. RTPL) probability higher. Thus, the longer effective life-time corresponds to a higher RTPL intensity.

Variation in RTPL intensity at corona charge-based measurement sites is very clear evidence of the impact of the measurements on the intrinsic properties of SiO2/Si structures (the invasive nature of the corona charge-based metrology). The recombination velocity S of the Si surface (or SiO2/Si interface) (τs) in equation 1 was significantly affected by corona charge-based measurements and resulted in effective life-time (τeff) change.

Discussion.— Physical aspects of SiO2/Si wafers (such as SiO2 thickness) can be easily monitored and controlled by optimizing typical oxidation process variables. However, electronic carrier transport properties are typically strongly influenced by subtle differences in various material parameters, besides physical dimensions. Crystalline defects, interface states, fixed and/or mobile charges, dangling bonds, band bending, strain/stress, dopant density and dopant uniformity are a partial list of important variables which can be difficult to describe or characterize, even with state-of-the-art characterization techniques. All aspects of material properties must be closely monitored and controlled to establish robust manufacturing process and quality control procedures.

It is important to note that the typical in-line C-V and SILC measurements for SiO2/Si quality control significantly modified SiO2/Si interface properties in this study and the measured characteristics are significantly different from the intrinsic properties of the as-prepared SiO2/Si. The corona charge-based, non-contact electrical metrology performed is not non-invasive, as is generally assumed. In Corona charging experiments in SiO2/SiN<sub>x</sub> stack passivated Si solar cells, it was found that the positive fields enhance RTPL intensity, while negative fields reduce RTPL intensity. RTPL intensity change is proportional to the applied filed and polarity of the SiO2/SiN<sub>x</sub> stack passivated Si solar cells. Field effect correlation with RTPL intensity has been found.\textsuperscript{25} For these reasons, analysis of the corona charge-based electrical property measurement data should be done very carefully to draw meaningful conclusions, since the measurement itself significantly influenced the electrical properties of interest that were being measured.

To better understand the dynamics of these complex semiconductor systems it is helpful to use several analytical disciplines together. Raman and photoluminescence spectroscopy are two such disciplines. We suspect that Si lattice stress beneath ultra thin SiO2 layers and the quality of the SiO2 network (bond structure, interface states, fixed and/or mobile charges, dangling bonds, band bending etc.) must be playing a very significant role in RTPL peak intensity variations in ultra thin SiO2/Si with substantially similar physical dimensions. Multiwavelength Raman spectroscopy studies of SiO2/Si, with various probing depths, indicates Si lattice stress or deformation beneath the ultra thin SiO2 films. Low temperature annealing (<850°C, lower than oxidation temperature) of all wafers in forming gas (containing H<sub>2</sub>) can reveal the role of dangling bonds at the SiO2/Si interface affecting RTPL intensity (the ratio of radiative recombination to non-radiative recombination). Multi-wavelength Raman characterization results indicate differences in Si lattice homogeneity beneath the ultra thin SiO2 layers among ultra-thin SiO2 films on Si wafers grown under different conditions (i.e. growth temperature, loading temperature, growing techniques, chemistry).

Multiwavelength spectroscopic RTPL is a very powerful non-contact and non-invasive optical characterization technique for analyzing electronic carrier transport properties.\textsuperscript{7-12} Many apparent or hidden factors which can influence electronic carrier transport properties, such as metal contamination, fixed/mobile charges, interface states, defects, mid-gap states, dangling bonds, band bending, dopant concentration etc., can be traced by carefully analyzing multiwavelength RTPL spectra with other material characterization results. Together, with multiwavelength Raman spectroscopy, change of lattice stress before and after oxidation processes and differences among wafers can be investigated.

The invasive nature of corona charge-based electrical metrology, used for SiO2/Si characterization in the semiconductor industry, was analysed by using multiwavelength RTPL wafer mapping and line scan measurements. Subsequent forming gas anneals and RTPL measurements revealed that the large portion of corona charged induced damage in SiO2/Si structures is permanent. More attention needs to be paid in characterizing and analyzing measurement data from corona charge-based electrical metrology tools. The conclusion must be that corona charge-based electrical metrology is invasive in nature.

In photovoltaics, SiO2 layers are typically used as a surface passivation layer to reduce surface recombination and thus improve the effectiveness of solar cells. The SiO2/Si interface states can capture photogenerated carriers and deteriorate passivation over time. Deposition of charge on the oxide surface can help suppress surface recombination at the SiO2/Si interface and enhance passivation. The charge deposited on the SiO2 surface changes the surface potential and produces an electric field across the SiO2 film. If the electric field is too large, it can induce damage and thus deteriorate the passivation. The optimum electrical threshold for positive passivation effect needs to be analysed to determine the optimum parameters of a low cost, corona charge-based passivation for Si photovoltaic applications.\textsuperscript{26}
Electric field dependency of the structure damage and passivation degradation of the 164 nm-thick thermal SiO2/Si, induced by corona charging, has been studied by varying corona charging voltage and time. At lower oxide electric fields (≤3.23 MV/cm), corona charging is demonstrated to be safe and reliable, and causes no obvious damage to the SiO2/Si structure. At medium oxide electric field (between 3.33 MV/cm and 3.96 MV/cm), corona charging causes little damage to the SiO2/Si structure, but still showed improved passivation effects. For higher oxide electric field (≥3.96 MV/cm), corona charging is destructive for both structure and passivation.26

For ultra-thin films used as gate oxides in advanced devices, a small bias voltage (40 mV) through deposited corona charges can build up significant electric field in SiO2/Si structures and induce damage, as demonstrated in the multiwavelength RTPL maps and line-scan results shown in Fig. 4. The typical bias voltage (40 mV) for the C-V measurement is equivalent to 4.3 ~ 5.7 MV/cm for the SiO2/Si wafers tested in this study. All SiO2/Si wafers showed the C-V and SILC measurement marks. Thus, the lowest electric field exhibiting damage in the SiO2/Si interface in this study was 4.3 MV/cm. The threshold electric field strength for the onset of SiO2/Si interface damage is possibly even smaller than 4.3 MV/cm.

Corona charging can induce damage to the SiO2/Si interface, demonstrated by an increase in interface defect density (from C-V measurements), and an increase in Si surface recombination velocity (from life-time measurements). This results in modification of surface passivation and surface recombination characteristics.14,15,27,28 A post corona charging anneal in nitrogen at 400 °C effectively reduces the defect density generated by corona charging. Annealing in forming gas has the effect of further reducing the damage. However, some of the damage is permanent and cannot be reversed by thermal anneals.27,28

Since atomic hydrogen (H+) generated in positive corona charging can passivate and depassivate silicon dangling bonds at the SiO2/Si interface, the role of hydrogen during corona charging and forming gas anneal is often discussed to explain passivation and depassivation mechanisms.22,24,29

To investigate whether the corona charging damage can be reduced, the SiO2/Si wafers were annealed in forming gas (N2 96% + H2 4%) at 400 and 800 °C for 10 min and additional RTPL measurements were performed. As forming gas annealing temperature increased, the average RTPL intensity was increased due to enhancement of the SiO2/Si passivation effect. However, the trace of corona charge-based electrical measurements was still clearly visible. A significant portion of corona charge induced damage in SiO2/Si structures was permanent. Applications of corona charge-based electrical measurements are common in device wafer characterizations. Since the corona charge-based electrical measurements modifies the electrical properties of as-prepared SiO2/Si, and possibly measures the modified state of electrical properties during the measurements, data from the potentially invasive measurements must be carefully analysed before drawing conclusions.

Summary

As complimentary in-line monitoring techniques for characterizing the dielectric/Si interface, in addition to the conventional physical thickness and electrical measurement techniques, multiwavelength room temperature photoluminescence (RTPL) and Raman spectroscopy were proposed Ultra-thin (6.8 ~ 9.2 mm thick) SiO2 films on 300 mm Si wafers prepared by various oxidation techniques and conditions were characterized using multiwavelength RTPL and Raman spectroscopy. Overall quality of the ultra-thin SiO2/Si interface (including passivation characteristics) and Si lattice stress beneath SiO2 films are investigated and compared with corona charge-based electrical characterization results.

While the corona charge-based electrical measurements cannot distinguish differences between ultra-thin (6.8 ~ 9.2 mm thick) SiO2 films on 300 mm Si wafers regardless of oxidation techniques and conditions, significant differences in RTPL and Raman characterization results were observed. The RTPL and Raman characterization results from the ultra-thin SiO2/Si wafers were dependent on the oxidation technique and process conditions. The RTPL and Raman results were well correlated. This suggested that the Si lattice condition beneath the ultra-thin SiO2 films was strongly influenced by initial oxidation temperature (loading temperature). Within wafer and wafer-to-wafer variations of SiO2/Si interface quality were characterized by RTPL and Raman spectra measurement. RTPL and Raman wafer mapping measurements under different excitation wavelengths were done to visualize the uniformity and repeatability of oxidation process.

RTPL wafer mapping and line scans revealed that the corona charge-based, non-contact, in-line characterization (capacitance-voltage (C-V) and stress induced leakage current (SILC) measurements) leave permanent measurement marks on wafers. This suggests that the characteristics of corona charge-based electrical measurements, generally assumed to be non-destructive, is no longer a valid assumption for ultra-thin oxide films. The impact of corona-charge based electrical measurements on SiO2/Si interface was permanent, and even clearly visible from the back side of the wafer. RTPL intensity variations at and near the measurement sites remained even after an additional forming gas anneal. There is a great possibility that the corona charge-based electrical measurement results may be “contaminated” by the destructive nature of measurements for ultra thin oxide films under high voltage corona charging.

For characterizing ultra-thin SiO2/Si interface quality, multiwavelength RTPL and Raman spectroscopy can provide additional insights into electrical and crystallographic properties in microscopic resolution without special sample preparation. They can be used as very useful complimentary in-line SiO2/Si interface quality characterization techniques combined with other, conventional characterization techniques.

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