PR-CIM: a Variation-Aware Binary-Neural-Network Framework for Process-Resilient Computation-in-memory

Minh-Son Le sonlm@khu.ac.kr
Thi-Nhan Pham nhanpt@khu.ac.kr
Thanh-Dat Nguyen datnt@khu.ac.kr
Ik-Joon Chang ichang@khu.ac.kr

Abstract—Binary neural networks (BNNs) that use 1-bit weights and activations have garnered interest as extreme quantization provides low power dissipation. By implementing BNNs as computing-in-memory (CIM), which computes multiplication and accumulations on memory arrays in an analog fashion, namely analog CIM, we can further improve the energy efficiency to process neural networks. However, analog CIMs suffer from the potential problem that process variation degrades the accuracy of BNNs. Our Monte-Carlo simulations show that in an SRAM-based analog CIM of VGG-9, the classification accuracy of CIFAR-10 is degraded even below 20% under process variations of 65nm CMOS. To overcome this problem, we present a variation-aware BNN framework. The proposed framework is developed for SRAM-based BNN CIMs since SRAM is most widely used as on-chip memory, however easily extensible to BNN CIMs based on other memories. Our extensive experimental results show that under process variation of 65nm CMOS, our framework significantly improves the CIFAR-10 accuracies of SRAM-based BNN CIMs, from 10% and 10.1% to 87.76% and 77.74% for VGG-9 and RESNET-18 respectively.

Index Terms—BNN, Deep Neural Network, Computation-in-memory, SRAM, Polar Neural Network

I. INTRODUCTION

Deep neural networks (DNNs) have shown outstanding performance to surpass human-level accuracy in many applications such as image processing, voice recognition, and language translation. Many researchers have made hard efforts to deploy the inference of DNNs at resource-constraint edge devices, still challenging due to the following reasons. It is well-known that DNNs accompany myriad parameters, and hence, a large memory size is indispensable to operate DNNs efficiently. At resource-constraint edge devices, it is not easy to increase the size of embedded memories above a certain level, leading to many DRAM footprints. In addition, the computational overhead of DNNs is considerable as well. These result in substantial energy dissipation, the major hurdle of edge devices.

Recently, some researches have shown the possibility to clear the hurdle. One of the most representative researches is a binary neural network (BNN), where all weights and activations are binarized. Despite the extreme 1-bit quantization, BNN delivers reasonably good accuracy [6]–[8]. Due to the aggressive quantization, BNNs have a small model size and can be processed with small-sized embedded memories, ensuring low energy dissipation. The energy efficiency of BNNs is further improved by directly computing BNNs in embedded memories such as SRAM, e-FLASH, and STT-MRAM, namely computation-in-memory (CIM) [1]–[5]. Most BNN CIM hardware computes multiplication and accumulations by using the concept of analog computing, so-called analog CIM, further enhancing energy efficiency. However, in reality, we should consider the potential problem that process variation significantly degrades the accuracy of BNNs to operate on analog CIM platforms. The low-resolution weights of BNNs tend to make BNNs prone to errors due to process variations, strongly motivating techniques to alleviate this problem.

This work presents a variation-aware BNN framework to deliver accurate analog CIM operations even under process variations of scaled technologies, based on the conventional 6T-SRAM. Recently, many emerging non-volatile memories (eNVM) based CIMs have gathered interest because of their high density and low standby power [4], [5], [9], [10], [16], [18]. However, the eNVM-based CIMs face many challenges in manufacturing actual hardware, while SRAM has advantages in terms of the actual design perspective and hence, plays a dominant role in the CIM design. Considering such a situation, we develop the variation-aware BNN framework on the SRAM-based CIM. However, we can easily extend the developed framework for the CIMs of other memories.

The contribution of this paper can be summarized as follows.

- We derive mathematical models related to the effect of process variations on the SRAM-based BNN CIM circuit. In the CIM circuit, an SRAM cell current represents the multiplication results of the weight and activation corresponding to the SRAM cell. Due to parametric process variations, the SRAM cell current is varied, affecting analog computation. Our model regards such a situation as the weight variation of BNNs. We extracted the models of the weight variations by using Monte-Carlo (MC) simulations in 65nm CMOS.
- Based on the derived model, we present the variation-aware BNN training framework to produce variation-resilient training results. During the training, BNNs are considered bi-polar neural networks due to the weight variations aforementioned. We demonstrate the efficacy of the developed framework through extensive simulations.
| Network     | Dataset  | Full precision | BNN (+1/-1) | BNN (1/0) | Split BNN (+1/-1) | Split BNN (1/0) |
|------------|----------|----------------|-------------|-----------|------------------|----------------|
| VGG-9      | CIFAR-10 | 93.71          | 89.77       | 91.36     | 88.51            | 88.70          |
| RESNET-18  | CIFAR-10 | 91.17          | 82.82       | 83.06     | 78.30            | 81.08          |

- We optimize biasing voltages of bit-lines (BLs) and word-lines (WLs) of SRAM, further improving the accuracy of the SRAM-based CIM.

The remaining part of this paper is organized as follows. In section II, we explain the background regarding BNN, the architecture of SRAM-based CIM, how DNNs can be mapped onto SRAM-based CIM arrays, and in-memory batch normalization. In section III, we present the variation-aware framework and optimization methodology for biasing voltages of BLs and WLs of SRAM. Section IV validates the efficacy of our framework. Lastly, we conclude the paper in section V.

II. PRELIMINARIES

A. Binary Neural Network

In BNN, all weights and activations are binarized, significantly enhancing the DNN inference energy efficiency. Many researchers have shown that despite such a low precision format, BNN delivers good inference accuracy [6]–[8]. The firstly introduced BNN [6] uses the sign function for the binarization of both weight and activation, where all weights and activations become ‘+1’ or ‘-1’. However, some state-of-the-art (SOTA) works improved the accuracy of BNN by using the activations of ‘0’ or ‘1’ [8] while they still employ the sign function for the binarization of weights. Considering such a trend, we use the following activation function.

$$BinAct(X) = \begin{cases} 
1, & X \geq \text{thresh} \\
0, & X < \text{thresh} 
\end{cases}$$

where \( \text{thresh} \) is the activation threshold. Our experiment results, where \( \text{thresh} \) is assumed as ‘0.5’, are shown in Table I showing the similar trend to SOTA works [8] as well. Since we use the activation function of (1), activations have the values of ‘0’ or ‘1’.

B. The Architecture of SRAM-based CIM

Fig. 1 shows the most widely used 6T-SRAM based CIM architecture and cell configuration for the BNN computation, which refers to the design of Rui Liu et al. [2]. We consider such an architecture for our proposed BNN framework, discussed in section III.

In Fig. I weights of BNNs are stored to 6T-SRAM cells, and the bitwise multiplications between weights and input activations of the network are directly computed with an analog fashion inside the SRAM array. Let us assume that the weight of ‘+1’ is represented by \( Q = 1 \), \( QB = 0 \), and the weight of ‘-1’ as the inverted cell. When we operate a BNN on the given configuration, the input activations of a certain BNN layer become the digital values of WLs, since the activation function of (1) is considered in this work, as mentioned in section II-A. When the inference is executed, all WLs are biased upon the input activations and then, the product of the \( i^{th} \) weight and the \( i^{th} \) activation becomes the difference between the \( bl \) and \( blb \) cell currents, \( i_{cell_{bl_i}} - i_{cell_{blb_i}} \), in Fig. I. All cell currents are accumulated to the currents of BL and BLB, implying that ‘\( I_{BL} - I_{BLB} \)’ becomes the multiply-and-accumulation (MAC).
TABLE II: Number of split groups for VGG-9

| Layer | Input count per output | Number of groups (Input size = 256) |
|-------|------------------------|-------------------------------------|
| 1     | 3x3x3                  | -                                   |
| 2     | 3x3x128                | 6                                   |
| 3     | 3x3x128                | 6                                   |
| 4     | 3x3x256                | 9                                   |
| 5     | 3x3x256                | 9                                   |
| 6     | 3x3x512                | 18                                  |
| 7     | 8192                   | 32                                  |
| 8     | 1024                   | 4                                   |
| 9     | 1024                   | -                                   |

TABLE III: Number of split groups for RESNET-18

| Layer | Input count per output | Number of groups (Input size = 256) |
|-------|------------------------|-------------------------------------|
| 1     | 3x3x3                  | -                                   |
| 2→7   | 3x3x16                 | 1                                   |
| 8→13  | 3x3x32                 | 2                                   |
| 14→19 | 3x3x64                 | 3                                   |
| 20    | 64                     | -                                   |

TABLE IV: Software to hardware conversion of \( BnBinAct() \)

| Software implementation | Hardware implementation |
|-------------------------|-------------------------|
| \( BnBinAct(X) = \begin{cases} 1, & X \geq X_{ih} \\ 0, & X < X_{ih} \end{cases} \) | \( \text{Output}(Y) = \begin{cases} 1, & Y \geq X_{ih} \\ 0, & Y < X_{ih} \end{cases} \) |
| where \( Y = I_{BL} - I_{BLB} \) | |

C. Mapping DNNs onto SRAM-based CIM arrays

1) Input Splitting: In the CIM architecture of Fig. 1, we store weights to SRAM and control the potentials of WL upon the input activations. Then, SRAM directly computes the matrix multiplications of convolution and fully-connected (FC) layers by using analog computing techniques. In such a scheme, the maximum matrix size that SRAM can calculate at once is dependent on the SRAM array size, which relies on the physical design constraints. Unfortunately, the computed matrix size often exceeds the SRAM array size. Fig. 3 shows such a situation well. Here, some convolution layers have 4-dimensional weights. We can regard a convolution layer with 4-dimensional weights as a 2-dimensional matrix with the size of \( (\text{kernell size} \times \text{kernel size} \times \text{input channel size}) \times (\text{output channel size}) \). For instance, in Fig. 3 the 4-dimensional convolution layer whose kernel, input channel, and output channel sizes are 3, 128, and 256, respectively, is considered as the 1152 \( (= 3 \times 3 \times 128 \times 256) \) matrix. To compute the matrix on the circuit of Fig. 1, we need 1152 memory rows. Since it is challenging to implement the SRAM array with 1152 rows, we need to properly split the matrix by considering the SRAM array size. Under such a circumstance, an SRAM CIM circuit can deal with one split part of the matrix and produces the corresponding partial sum. All partial sums delivered by the SRAM CIM circuits should be accumulated to complete the matrix computation. SOTA works showed that the precision of the partial sums significantly affects the accuracy of the computed BNNs \([2],[10],[11],[16]\). To obtain multi-bit partial sums in the SRAM CIM circuits, we need ADCs to produce multi-bit outputs, incurring large area and energy overhead.

To address this problem, the authors of \([11]\) developed an input splitting technique, which we employed in this work. A large convolution or FC layer is reconstructed into several smaller groups, as shown in Fig. 3 whose input number should be smaller or equal to the number of rows in an SRAM array. Hence, the SRAM array of Fig. 1 computes the weighted-sums of each group, and the CSAs produce their own 1-bit outputs. Then, the outputs of all groups are merged to fit the input size of the following BNN layer, which is done by digital machines to obtain accurate merging without the effect of process variations.

The accuracy based on the input splitting technique is compared with the accuracy of the baseline as shown in Table IV. We assume a typical SRAM array size, \( 256 \times 256 \). The first layer of the BNN that processes the input image and the last layer of the BNN that computes the score of each class are excluded from the input splitting, computed by digital machines. Such an approach follows SOTA works \([6]–[8], [10], [11]\) related to BNN. The split BNN accuracies of Table IV are considered as the baselines when our techniques are evaluated. For reference, we summarized the number of groups per BNN layer after input splitting on Table II and Table III for VGG-9 and RESNET-18 networks respectively.

2) Mapping: We make more detailed discussions regarding the mapping between convolution layers of BNNs and SRAM-based CIM arrays, shown in Fig. 3. As aforementioned, convolution layers are split to ensure that their size is equal to or less than the number of rows in the SRAM array. As shown in Table II the number of split groups of the layer is six \( (= \lceil 1152/256 \rceil + 1) \), and the input channels per group are 21 \( (= 128/6) \) in VGG-9. Hence, the input size of each group is 189 \( (= 3 \times 3 \times 21) \), which is smaller than the number of rows in the SRAM array. Consequently, each group can be regarded as a 2-dimensional matrix with the size of \( (3 \times 3 \times 21) \times (256) \). Under this circumstance, we can have the mapping strategy that all weights corresponding to each output channel are stored on one column of the SRAM array. The outputs of each group, which is binary ‘0’ or ‘1’, are obtained from the macros. We can manage FC layers with the above mapping strategy as well.

D. In-memory batch normalization

Batch normalization (BN) is the technique to stabilize the learning process, significantly reducing the number of training
epochs. In BNNs, BN highly affects the training accuracy [19], more critical. BN can be described by the following equation.

\[ Y = \gamma \frac{X - \mu}{\sigma^2 + \epsilon} + \beta \]  

where \( X \) and \( Y \) are the input and the output of BN, and \( \gamma, \beta, \mu, \sigma, \) and \( \epsilon \) are a weight, a bias, a mean, a standard deviation, and a sufficiently small constant, respectively. During the back propagation of the training, these four parameters are updated and used to normalize the output of the current batch. In the inference, these parameters become constant, and hence, BN can be regarded as a linear transformation function. As shown in Fig. 4, in the inference, the output of the BN layer becomes the input of the activation function (1). In this work, we merge (1) and (2), whose function is named as \( BnBinAct() \). The merged function can be expressed by

\[ BnBinAct(X) = \begin{cases} 1, & X \geq X_{th} \\ 0, & X < X_{th} \end{cases} \]  

, where \( X \) is the output of weighted-sum layer, and

\[ X_{th} = \frac{(\text{thresh} - \beta)}{\gamma} \left( \sqrt{\sigma^2 + \epsilon} \right) + \mu. \]  

Most previous works assume that BN is computed by software [1], [2], [9], [10]. In such a scenario, ADCs should convert accumulated BL currents to high-precision digital values, which are fed to digital processors, not suitable for edge devices due to large energy overhead. To address this problem, in [15] BN is implemented as additional cells. In this work, we simply handle the problem by implementing the merged function as the variable current biasing embedded to the differential CSA, shown in Fig. 2. The biasing current values can be derived from the conversion rule of Table IV. Two current biasing, \( I_{\text{Thres}_\text{Neg}} \) and \( I_{\text{Thres}_\text{Pos}} \), are necessary to deal with both positive and negative \( X_{th} \) cases. Since the major contribution of this work is to present a variation-aware framework, the detailed discussion regarding the operation of the CSA is not discussed.

III. A VARIATION-AWARE BINARY NEURAL NETWORK FRAMEWORK

A. Variation-aware Models for SRAM-based BNN CIM

In this section, we present a variation-aware BNN framework to enhance the reliability of CIM under process variations. The framework assumes SRAM-based CIM, whose configuration is discussed in section II-B. To develop such a BNN framework, firstly, variation-aware models are investigated and derived as follows.

In the given configuration (Fig. 1), as discussed, the MAC output is defined by ‘\( I_{BL} - I_{BLB} \)’, which described as

\[ I_{BL} - I_{BLB} = \sum_{i=0}^{N-1} (i_{\text{cell}_{BL}i} - i_{\text{cell}_{BLB}i}) \times W_{Li} \]

\[ = \sum_{i=0}^{N-1} ((W_i) \times IM) \times W_{Li} \]

, where \( W_i \) is the \( i^{th} \) weight stored in the SRAM array (i.e., \( W_i \) is ‘+1’ or ‘-1’), \( W_{Li} \) is the \( i^{th} \) word-line (WL) status (ON or OFF), which corresponds to activation values (‘1’ or ‘0’), and \( IM \) is the current margin that is absolute value of difference current between BL and BLB for one cell (i.e., one bitwise-multiply operation), where no process variations are assumed. In reality, both ‘\( i_{\text{cell}_{BL}i} \)’ and ‘\( i_{\text{cell}_{BLB}i} \)’ experiences process variations, which can be regarded as the variation of \( W_i \) in (5). Let us model the weight variation as \( \Delta(W_i) \). Consequently, the product of the \( i^{th} \) weight and the \( i^{th} \) activation, ‘\( i_{\text{cell}_{BL}i} - i_{\text{cell}_{BLB}i} \)’, can be redefined as

\[ i_{\text{cell}_{BL}i} - i_{\text{cell}_{BLB}i} = (W_i + \Delta(W_i)) \times IM. \]  

In this work, the analysis of process variations was performed through 10,000 MC simulations using statistical models from 65nm CMOS. Without the loss of generality, for one cell configuration as in Fig. 1 we investigate the case that stored...
weight as ‘+1’ (i.e., \( Q = 1 \) and \( Q_B = 0 \)). Therefore, when \( WL \) is ON (i.e., \( \text{input neuron is 1} \)), under process variations, the \( bl \) and the \( blb \) cell currents have the log-normal distributions of \( LN(\mu_{bl}, \sigma^2_{bl}) \) and \( LN(\mu_{blb}, \sigma^2_{blb}) \) as shown in Fig. 5. Then, we can sequentially derive the following equations.

\[
\begin{align*}
\Delta(W_i) &= \begin{cases} 
\frac{\Delta_{(+1)}}{1} = \frac{1}{1+\Delta_{(+1)}} \times (i_{cell_{bl, i}} - i_{cell_{blb, i}}) - 1 \\
\frac{\Delta_{(-1)}}{1} = \frac{1}{1+\Delta_{(-1)}} \times (i_{cell_{blb, i}} - i_{cell_{bl, i}}) + 1
\end{cases} 
\end{align*}
\]

Based on (7) and the models that is taken from Fig. 5 we obtain the weight distribution under process variations, illustrated in Fig. 6. This shows that under process variations of the given CIM configuration, binary weights (-1/+1) are transformed to analog weights \((-1 + \Delta_{(-1)})/1 + 1 + \Delta_{(+1)}\) of a BNN, whose distributions are log-normal.

**B. Variation-aware Framework for Bi-polar Neural Networks**

The discussion of section III-A shows that with the effect of process variations, each weight stored in memory array experience process variations with the weight variation as \( \Delta(W_i) \). Then, the weight stored in each SRAM cell is not an exact digital value of +1 or -1 but can be redefined as

\[
\text{Polarize}(W_i) = \begin{cases} 
+1 + \Delta_{(+1)}, & \text{when } W_i = +1 \\
-1 + \Delta_{(-1)}, & \text{when } W_i = -1
\end{cases}
\]

where \( W_i \) is a binarized weight, and \( \Delta_{(+1)} \) and \( \Delta_{(-1)} \) are random stochastic parameters to express the effect of process variations.
Algorithm 1 Training a reconstructed L-layer BNN with variation-aware weights and activations. C is the cost function for minibatch, \( \lambda \) - the learning rate decay factor and L the number of layers. \( \circ \) indicates element-wise multiplication. The function \( \text{Sign}() \) specifies how to polarize the weights. \( \text{Polarize}() \) is used for estimating gradients for (1) as in [6]. Split() and previous learning rate \( \eta \)

Require: a minibatch of inputs and target \((a_0, a^*)\), previous weights W, previous BatchNorm parameters \((\gamma, \beta)\), \( \text{ArraySize} \), weights initialization coefficients from [22] \( \alpha \), and previous learning rate \( \eta \).

Ensure: updated weights \( W^{t+1} \), updated BatchNorm parameters \((\gamma^{t+1}, \beta^{t+1})\) and updated learning rate \( \eta^{t+1} \).

1. Computing the parameters gradients:

   1.1 Forward propagation:
   
   for \( k = 1 \) to \( L \) do
   
   // Input size per array
   \( \text{InputSize} = \text{Kernel} \times \text{Kernel} \times \text{InputChannels} \)
   
   // Number of groups
   \( nGroups = \lceil \text{InputSize}/\text{ArraySize} \rceil \)
   
   while \( \text{InputSize} \% nGroups \neq 0 \) do
   
   \( \text{nGroups} = \text{nGroups} + 1 \)
   
   end while
   
   // Input splitting
   \( a_{k-1}^b \leftarrow \text{Split}(a_{k-1}^b, nGroups) \)
   
   \( W_k \leftarrow \text{Split}(W_k, nGroups) \)
   
   for \( i = 1 \) to \( nGroups \) do
   
   \( W_{k}^i[i] \leftarrow \text{Sign}(W_k[i]) \)
   
   \( W_{k}^i[i] \leftarrow \text{Polarize}(W_k[i]) \)
   
   \( s_k[i] \leftarrow a_{k-1}^b[i] W_{k}^i[i] \)
   
   end for
   
   \( a_k \leftarrow \text{BatchNorm}(s_k, \gamma_k, \beta_k) \)
   
   if \( k < L \) then
   
   \( a_k \leftarrow \text{Clip}(a_k, 0, 1) \)
   
   \( a_k^b \leftarrow \text{StoQuantize}(a_k) \)
   
   \( a_k^b \leftarrow \text{Merge}(a_k^b, nGroups) \)
   
   \( a_k^b \leftarrow \text{BinAct}(a_k^b) \)
   
   end if
   
   end for

\[
\begin{align*}
\text{StoQuantize}(X) &= \begin{cases} 
1, & X \geq (\text{thresh} + \Delta_{\text{act}}) \\
0, & X < (\text{thresh} + \Delta_{\text{act}}) 
\end{cases} \quad (9)
\end{align*}
\]

Algorithm 1 (Continued)

1.2 Backward propagation:

Compute \( g_{a_k} = \frac{\partial C}{\partial a_k} \) knowing \( a_L \) and \( a^* \)

for \( k = L \) to 1 do

if \( k < L \) then

\( g_a \leftarrow g_{a_k} \circ 1_{0 \leq a_k \leq \text{thresh}} \) (STE)

end if

\( (g_{s_k}, g_{\gamma_k}, g_{\beta_k}) \leftarrow \text{BackBatchNorm}(g_{a_k}, s_k, \gamma_k, \beta_k) \)

for \( i = 1 \) to \( nGroups \) do

\( g_{a_k}^{b-1}[i] \leftarrow g_{s_k} g_{W_k}^i[i] \)

\( g_{W_k}^{b+1}[i] \leftarrow g_{s_k}^T g_{b}^{a_k-1}[i] \)

end for

end for

2. Accumulating the parameters gradients:

for \( k = 1 \) to \( L \) do

\( \gamma_{k+1} \leftarrow U\text{Update}(\gamma_k, \eta, g_{\gamma_k}) \)

\( \beta_{k+1} \leftarrow U\text{Update}(\beta_k, \eta, g_{\beta_k}) \)

for \( i = 1 \) to \( nGroups \) do

\( W_{k+1}^{b+1}[i] \leftarrow U\text{Update}(W_k[i], \alpha_k[i] \eta, g_{W_k}^{b+1}[i]) \)

end for

end for

end for

end while

\( \eta^{t+1} \leftarrow \lambda \eta \)

end for

end for

variations, whose distributions are obtained from (7). Our training framework is described as Algorithm 1, where the function of (8) is exploited. In the variation-aware training, we train BNNs based on Algorithm 1 from scratch.

Please note that due to process variations of CSA, the activation threshold of (1) can be varied. By taking into consideration this, in Algorithm 1 we employ the stochastic activation function, whose equation is given by (9), instead of the deterministic activation function of (1).

\[
\Delta_{\text{act}} \sim N(0, \text{stddev}) \quad (10)
\]

, where the standard deviation of \( \Delta_{\text{act}} \) is properly assumed. When the training step is completed, only binarized weights are left for the inference and the SRAM-based CIM. However, in the inference, the quantized weights need to be polarized again to evaluate the effect of process variation. Since the stochastic function of (8) is used in the variation-aware inference, we executed the inference 100 times, whose distribution is observed.

C. Optimization of Biasing Voltages

In this section, we propose the optimization methodology for biasing voltages of WLs and BLs of SRAM, respectively expressed as \( V_{WL} \) and \( V_{BL} \), which is shown in Fig. 7. This methodology provides steps to find the optimal biasing voltages, which delivers the best accuracy. Firstly, the \( V_{WL} \) and \( V_{BL} \) configuration is set to run MC circuit simulations of the SRAM cell. If a cell flipping occurs, the \( V_{WL} \) and \( V_{BL} \) configuration is discarded to ensure the accuracy for BNNs. If a cell flipping does not happen, mean and variance of \( i_{cell_{WL}} \) and \( i_{cell_{BL}} \) distributions are fed to the variation-aware BNN framework (Section III-B). After conducting the variation-aware training and variation-aware inferences, the
average accuracy is collected and compared with those of other $V_{WL}$ and $V_{BL}$ configurations.

D. Modeling of IR-drop

The resistance of the power lines in an SRAM array causes IR-drop, causing the drop of supply voltages. Such an effect is not considered in our experiments. However, we can easily model the drop effect by applying lower supply voltages in our MC simulations.

IV. VALIDATION OF OUR FRAMEWORK

A. Experimental Setting

We evaluate the efficacy of our proposed framework with different biasing voltages of BLs and WLs in 6T-SRAM. Under process variations of 65nm CMOS, we estimate the average inference accuracies before and after variation-aware training of RESNET-18 and VGG-9 with CIFAR-10.

In training, the loss is minimized with the algorithm of [20], the initial learning rate is set to 0.01, and the maximum number of epochs is 150 for VGG-9 and 250 for RESNET-18. We decay the learning rate by 0.31 when scalar statistics of validation accuracy do not change enough. The variation-aware inferences are 100 times executed with the batch size of 1 for 50000 validation images, whose accuracies are averaged.

In (10), the standard deviation is assumed as 10% of $\text{thresh}$ in (1) and (9).

For the baseline, we do not consider the effect of process variation while the input splitting technique, mentioned in section II-C2, is used. For RESNET-18, we assume that shortcuts have the data format of full-precision. Many SOTA works [8] employed such an approach since the accuracy of RESNETs is sensitive to the quantization errors of shortcuts, which is followed in this work.

B. Results and Discussion

The average inference accuracy before applying variation-aware training of both RESNET-18 and VGG-9, shown in Fig. 8 and 9, clearly show that in SRAM-based analog CIMs, the classification accuracy of CIFAR-10 is severely degraded by process variations, even below 20% for all $V_{WL}$ and $V_{BL}$ voltage configurations under consideration.

Our variation-aware training framework addresses this problem. Fig. 10 shows the inference accuracies of RESNET-18 after using the variation-aware training, where the effect of process variations is considered for the inference as well. The results demonstrate that our variation-aware training
framework significantly improves the accuracy under process variations. For instance, when $V_{WL}=0.9V$ and $V_{BL}=0.4V$, the accuracy was 10% under process variations of 65nm CMOS (Fig. 8). Our variation-aware training framework provides a quantum leap for the accuracy of this $V_{WL}$ and $V_{BL}$ biasing condition, to 77.74%.

We have similar results in VGG-9. Our variation-aware training framework supports remarkable accuracy improvement under the effect of process variations. For instance, in Fig. 9 the accuracies are 10% for two biasing cases of $V_{WL}=0.4V/BL=0.3$, and $V_{WL}=0.9V/BL=0.4$ while, in Fig. 11 the accuracies corresponding to the above two cases become 74.51% and 87.76%. This well validates the efficacy of our variation-aware training framework.

As illustrated in Fig. 10 and 11 the accuracy under process variations tends to increase as $V_{WL}$ increases. It is since cell currents are larger with the higher $V_{WL}$ providing better immunity to process variations. However, when $V_{WL}$ is above a certain level, some SRAM cells are flipped due to a negative read static noise margin [21] (In Fig. 8, 9, 10 and 11 the biasing case with the SRAM cell flipping is marked with “Flipped”). It significantly degrades the accuracy. Considering this factor, we decide the optimal biasing point of $V_{WL}$ and $V_{BL}$, which is the case that $V_{WL}=0.9V$ and $V_{BL}=0.4V$. At this point, the CIFAR-10 accuracies of RESNET-18 and VGG-9 are 77.74% and 87.76%, respectively.

V. CONCLUSION

By directly computing BNNs in embedded memories, namely computation-in-memory (CIM), we can obtain the utmost energy efficiency for edge devices. However, such an approach suffers from considerable accuracy degradation due to process variation. We present a variation-aware BNN framework on a configuration of SRAM-based CIM, whose efficacy is validated by extensive simulations.

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