Abstract—Due to their capacity-achieving property, polar codes have become one of the most attractive channel codes. To date, the successive cancellation list (SCL) decoding algorithm is the primary approach that can guarantee outstanding error-correcting performance of polar codes. However, the hardware designs of the original SCL decoder have large silicon area and long decoding latency. Although some recent efforts can reduce either the area or latency of SCL decoders, these two metrics still cannot be optimized at the same time. This paper, for the first time, proposes a general log-likelihood-ratio (LLR)-based SCL decoding algorithm with multi-bit decision. This new algorithm, referred as LLR-2^Kb-SCL, can determine 2^K bits simultaneously for arbitrary K with the use of LLR messages. In addition, a reduced-data-width scheme is presented to reduce the critical path of the sorting block. Then, based on the proposed algorithm, a VLSI architecture of the new SCL decoder is developed. Synthesis results show that for an example (1024, 512) polar code with list size 4, the proposed LLR-2^Kb-SCL decoders achieve significant reduction in both area and latency as compared to prior works. As a result, the hardware efficiency of the proposed designs with K=2 and 3 are 2.33 times and 3.32 times of that of the state-of-the-art works, respectively.

Index Terms— polar codes, successive-cancellation, VLSI, log-likelihood-ratio (LLR), multi-bit decision

I. INTRODUCTION

POLAR codes [1] have emerged as one of the most attractive forward error correction (FEC) codes in recent years. Due to their unique capacity-achieving property, polar codes provide outstanding error-correcting capability that would be very useful for digital transmission.

However, to date polar codes suffer from inferior finite length error-correcting performance. In particular, in the region of short or medium code length, polar codes are not comparable to the LDPC codes in terms of coding gain. To solve this problem, successive-cancellation list (SCL) decoding algorithm was proposed in [2] to improve the coding gain of the polar codes. In [2], it was shown that with the use of SCL algorithm, polar codes can outperform the WiMAX LDPC codes even for a shorter code-length.

Although SCL algorithm can help polar codes achieve beyond-LDPC performance, this approach suffers from high complexity and long latency. Recently, some efforts were proposed to address these problems. An LLR-based SCL algorithm was proposed in [3-4] to reduce the amount of combinational logic and memory. In [5-6][11], low-latency SCL algorithms were presented to reduce the required number of decoding cycles. However, these prior works only focused on either reducing area or latency, but not on optimizing these two metrics at the same time.

This paper, for the first time, proposes a general reduced-latency LLR-based SCL decoding algorithm. This new algorithm, namely LLR-2^Kb-SCL, can determine 2^K bits in one cycle for arbitrary K with the use of LLR messages. As a result, it can achieve both low complexity and short latency. In addition, a reduced-data-width scheme is presented to reduce the critical path of the sorting block. Based on the proposed algorithm, a VLSI architecture of the new SCL decoder is developed. Synthesis results show that for an example (1024, 512) polar code with list size 4, the proposed LLR-2^Kb-SCL decoder achieves great reduction in both area and latency as compared to the prior works, respectively. As a result, the hardware efficiency of the proposed designs with K=2 and 3 are 2.33 times and 3.32 times of that of the state-of-the-art works, respectively. Notice that this paper is a generalized version of our prior work [10].

The rest of the paper is organized as below. Section II gives a brief review of polar codes. The proposed LLR-2^Kb-SCL algorithm and the reduced-bit-width scheme for sorting block are presented in Section III. Section IV develops the hardware architecture of the new algorithm. Hardware performance is analyzed and discussed in Section V. Section VI draws the conclusions.

II. REVIEW OF POLAR CODES

A. Encoding of Polar Codes

The encoding procedure of (n, p) polar codes consists of two steps. First, the p-bit source message is extended to an n-bit message w=(u_1, u_2…u_n) with padding n-p “0” bits. Here those padded “0” bits are referred as frozen bits and their positions over the u, namely frozen positions, are known to both the transmitter and receiver. Then, u is multiplied with an n-by-n generator matrix G to obtain the transmitted codeword x=(x_1, x_2…x_n)=uG. Fig. 1 shows the example of an n=4 polar code encoder. For details on encoding of polar codes, the reader is referred to [1].
is defined as \((y_1, y_2, \ldots, y_n)\). An LLR-based successive-cancellation (SC) decoder can be used to recover \(u\) from \(y\). Fig. 2 shows an example SC decoding procedure for \(n=4\) polar codes. It can be seen that the SC decoder consists of two types of computation units, namely \(f\) and \(g\), respectively. Here each \(f\) or \(g\) unit is labelled with a number, which indicates the time index when the corresponding unit is activated for computation. It can be seen that at clock cycle 2, 3, 5 and 6, the \(f\) or \(g\) unit in the last stage (stage 2 in this example) sends its LLR output to the hard-decision \(h\) unit to determine the decoded bit. Notice that the example SC decoder is based on LLR form. In this case, the function of \(f\) and \(g\) units can be approximated as (1) and (2):

\[
\begin{align*}
\hat{a}(a, b) &= \text{sign}(a) \text{sign}(b) \min(|a|, |b|) \\
\hat{g}(a, b) &= a(-1)^{\sum_{u} a} + b
\end{align*}
\]

In Fig. 2, the example process of \(n=4\) is shown, cited from [7].

### C. Successive-Cancellation List (SCL) Algorithm

The decoding process of polar codes can also be interpreted from the view of code tree. Fig. 3 shows an example code tree for \(n=4\) polar codes. Here each level represents a decoded bit. The value that is associated with each node represents the probability (metric) of the corresponding decoding path. For example, 0.23 at level 4 represents the probability for the length-4 path (1000) is \(P_r(i_1=1, i_2=0, i_3=0, i_4=0) = 0.23\). Based on this representation, the objective of a successful decoding procedure is to find the length-4 path that is the correct codeword. To achieve this goal, the SC decoder first visits the children nodes that are associated with the current survival path at each level. Then it selects the new path that has the larger metric as the updated survival path. Because this searching strategy is only locally optimal, the performance of the SC decoder is limited.

Different from the SC decoder that only selects a single path, the \(L\)-size SCL algorithm utilizes \(L\) different searching paths. Therefore, it is more likely for the SCL algorithm to find the desired path than the SC algorithm. For example, SCL decoder with \(L=2\) is able to trace the valid path (1000) in Fig. 3 while the SC decoder fails to find it.

### III. THE PROPOSED LLR-BASED MULTI-BIT DECODING

This subsection presents an LLR-based SCL decoding algorithm with \(2^K\) bits decision, namely LLR-2^Kb-SCL. Notice that [5] also proposed a reduced-latency decoder that can determine multiple bits in one cycle. However, the SCL decoder in [5] is based on the likelihood form while the design in this paper is based on the LLR form. This difference in the fundamental representation of the proposed algorithm leads to much less computation complexity than the approach in [5].

Next, we show how to determine each successive \(2^K\) bits as \(u_{2^K-1}, \ldots, u_1\), at the same time in the LLR form. From the view of code tree (see Fig. 3), this means the SCL decoder is able to directly calculate the metrics of length-\((2^K)\) paths from the metrics of length-\((2^{K-1})\) paths. In general, such direct computation is performed by an LLR-based metric computation unit (MCU), which replaces the original last \(K\) stages of each LLR-based SC decoder (see Fig. 2). In the following paragraph, we show how to derive the function of the LLR-based MCU.

Assume that the previously decoded \(2^K\) bits \(u_{K-1}, \ldots, u_1\) are \(z_{K-1}, \ldots, z_1\), respectively. This event is denoted as \(z_{2^K-1} = z_{2^{K-1}}\). Therefore, in the logarithmic domain the length-\((2^K)\) path metric can be represented as:

\[
M(a_{2^K-1}, a_{2^{K-1}}, \ldots, a_1) = \ln(P_r(u_{2^K-1} = a_{2^K-1}, u_{2^{K-1}} = a_{2^{K-1}}, \ldots, u_1 = a_1)),
\]

where \(a_{2^K-1} \ldots a_1\) is defined as \((u_{2^K-1}, \ldots, u_1)\) that is the set of the current \(2^K\) decoded bits. In addition, \(a_i\) is defined as \((a_i)\) whose elements are the binary values.
contains the probabilistic information of the current $2^K$ decoded bits, which is unknown during the decoding procedure. To address this problem, we need to further represent the logarithmic path metrics with the LLR messages that are input to the MCU. Such reformulation is based on the fact that the polar decoding procedure is inherently “guided” by its encoding procedure [8]. Simultaneous right-to-left decoding procedure of the successive $2^K$ bits (see Fig. 4(a)) involves the estimation of the left-to-right encoding procedure (see Fig. 4(b)). Hence if $\bar{u}^{i}_{j}$ is estimated to be $a^{i}_{j}$, then $\bar{u}^{i}_{j}$ should be the estimation of $a^{i}_{j}$, where $U$ is the $2^d$-by-$2^k$ generator matrix. As a result, (3) can be further re-written as:

$$M(a_{i...a_{K}}, z_{i}^{2^{K-i}(i)}) = \ln(Pr(\bar{u}^{i}_{j} = a_{i}^{j} u^{j}_{i}, u^{j}_{i} = z_{i}^{2^{K-i}(i)}))$$  

(4)

Consider $\ln(1+e^x) \approx x$ for large $x$; otherwise 0 for small $x$. (7) can be further approximated as below:

$$M(a_{i...a_{K}}, z_{i}^{2^{K-i}(i)}) = \sum_{j=1}^{2^d} (s_j (1-a^{j}_{K} u(j)) - \delta(s_j)) + M(z_{i}^{2^{K-i}(i)}),$$  

(8)

where $\delta(s_j)=s_j$ if $s_j \geq 0$; otherwise 0.

(8) shows how to directly calculate the metric of length-$2^{i}$ paths from the metric of length-$2^{i-1}$ paths. With the use of this update principle, we can develop the LLR-based SCL decoding algorithm with $2^K$ bits decision as Scheme-A. In general, an L-size LLR-2^{b}-SCL decoder consists of L copies of LLR-based SC decoder. To decode every $2^K$ successive bits, each SC component decoder first performs the regular SC decoding procedure till the last-(m-K) stage (see Fig. 2), where $m=\log n$. At this time, the (m-K) stage outputs $2^K$ LLR messages $s_j (j=1, 2,..., 2^K)$ to the MCU block. Then, the MCU block in each SC component decoder calculates the new path metrics with the use of (8). After that, all of the updated path metrics from the L SC component decoders are compared and L largest are selected as the survival paths metrics. The above entire procedure is repeated for every $2^K$ bits until all the $n$ bits are determined. Note that similar to [5], a simple zero-forcing unit (ZFU) is needed after the computation of (8), which helps to drop the unqualified paths that violate the frozen conditions.

**Scheme A:** $L$-size LLR-$2^b$-SCL Algorithm for $(n, k)$ polar codes

1: **Input:** Log-Likelihood ratios of each bit in the received codeword
2: **Initialization:** Path metric $M_{i}=0$ for each survival path
3: For $i=1$ to $n/2^b$
4: For each length-$2^i$ survival path $z_{i}^{2^{K-i}(i)}$
5: SC component decoding:
6: Activate stage-1 to stage-(m-K) of LLR-based SC decoder
7: Stage-(m-K) output $2^b$ LLR-based message $s_j (j=1, 2,..., 2^K)$
8: Path Expansion:
9: Expand survival path $z_{i}^{2^{K-i}(i)}$ to $2^b$ candidate paths $u_{i}^{j}$ ($a_{i}^{j} = z_{i}^{2^{K-i}(i)}$)
10: $1$ length-(2^{i-1}(i)) path $\Rightarrow$ $2^{b}$ length-(2^{i}(i)) paths
11: Metric Computation:
12: Calculate $2^b$ actual path metrics $M(a_{i...a_{K}}, z_{i}^{2^{K-i}(i)})$ by (8)
13: Forcing Zero:
14: $M(a_{i...a_{K}}, z_{i}^{2^{K-i}(i)})$ for path $u^{j}_{i}$ ($a^{j}_{K} = z_{i}^{2^{K-i}(i)}$)
15: $u_{i}^{j}$ is frozen $\Rightarrow$ all $M(a_{i...a_{K}}, 0a^{j}_{K}...)=\inf$
16: End for
17: Compare and Prune:
18: Compare $M(a_{i...a_{K}}, z_{i}^{2^{K-i}(i)})$ for all the $2^{b}$ length-(2^{i}(i)) candidate paths
19: Select $L$ paths with the L largest metrics as the new survival paths
20: End for
21: **Output:** Choose the length-$n$ survival path with the largest metric

**B. Reduced-Data-Width Scheme for Sorting Block**

Typically, $Q=6$ bit quantization scheme is sufficient for the fixed-point implementations of LLR-based SCL decoder. However, as indicated in [3], the representation of path metrics needs more bits since the path metrics have larger data range than the propagated LLR messages. In [3], it showed that $M=8$ bit for path metrics can avoid significant performance degradation in terms of frame error rate (FER). Since the overall critical path of the SCL decoder is in the sorting block that sorts those path metrics [3][5], the escalating data-width of
path metrics inevitably causes significant increase in critical path delay. To address this challenge, we propose a reduced-bit-width scheme for sorting block. The key idea is to only utilize $S=M-1$ bits to represent the path metrics for sorting, while the representations of path metrics for updating and storing are still based on $M$ bits. This approach is derived from the following observation: In SCL decoder the sorting block does not require as high precision as MCUs, since the function of the sorting block is just to rank the path metrics without changing their values, while the MCUs have to adopt larger data-width to guarantee accurate calculation. Therefore, a reduced-data-width for sorting block does not cause significant performance degradation but enables reduction in critical path delay. Fig. 5 shows the fixed-point simulation results for the proposed LLR-2b-SCL algorithm with reduced-data-with for sorting block. Here the simulation environment is AWGN channel with BPSK modulation and the code parameters are $n=1024$, $r=0.5$. From the figure it can be seen that, compared to the original scheme using $S=8$ bits for sorting the path metric, the proposed scheme with $S=7$ bits only has negligible performance loss for different values of $K$ and $L$.

Notice that since ZFU can be easily implemented with multiplexers; the analysis of this block is omitted as well.

![Fig. 6. Overall architecture of the LLR-2b-SCL decoder.](image)

**IV. HARDWARE ARCHITECTURE**

**A. Overall Architecture**

Fig. 6 shows the overall hardware architecture of the proposed $L$-size LLR-2b-SCL algorithm decoder. The data path of the entire decoder contains $L$ LLR-based SC decoders plus a metric sorting block. For each SC component decoder, it is reformulated from the LLR-based decoder in [8], which retains the $(m-K)$ stages but the last $K$ stages are replaced by the LLR-based MCU and ZFU. In addition, the required memory resource of the entire decoder consists of register arrays, bulk memory and buffer for survival paths, path metrics, propagating LLR messages and channel outputs, respectively.

In this section, the hardware design of the sorting path is very straightforward and similar to the approaches in [3] [5]. The only difference is that the data-width of comparators is reduced from $M$ bits to $M-1$ bits and the least significant bits (LSBs) of all the input path metrics are dropped to be consistent with the data-width of comparators. Therefore, in this section we focus on other parts of the data path and memory resource.

![Fig. 7. Architecture of MCU for $K=3$.](image)

**B. LLR-based Metric Computation Unit (MCU)**

In Section III (8) describes the function of MCU. Since this function depends on $K$, the hardware design of MCU varies with different choices of $K$. Fig. 7 illustrates the inner architecture of MCU for $K=3$. Here $\delta(*)$ block can be simply implemented with a multiplexer. In addition, StoC and CtoS blocks represent the components that perform the conversion between sign-magnitude and 2’s complement forms.

![Fig. 8. Architecture of PE.](image)

**C. LLR-based Processing Element (PE)**

As shown in line 5 – line 7 in Scheme-A, the input LLR messages of MCU are calculated from the first $(m-K)$ stages of LLR-based SC decoder in [8]. In general, these stages consist of $f$ and $g$ nodes in Fig. 2, which can be implemented in hardware as the following processing element (PE) in Fig. 8. Notice here the addition and subtraction in (2) is designed as a unified adder and subtractor to save area.

**D. Memory Resource**

For the proposed decoder, different types of memory resource are needed for different types of data. Because the $L$ survival paths and their metrics need to be updated simultaneously each
time, they are stored in registers. In addition, for the propagating LLR messages that are processed in the PEs, L bulk memory banks are used to store the corresponding messages in the L different SC component decoders. This memory partition approach can also avoid the potential memory access conflict. Besides, a specific buffer is used to store the initial LLR inputs to the decoder.

V. PERFORMANCE AND DISCUSSION

A. Hardware Performance Comparison

Table I shows the hardware performance of different SCL decoders with list size \(L=4\) for the same (1024, 512) polar codes. For the designs with different technology libraries, the results on area and frequency are scaled to the same 90nm node. From this table it can be seen that; the proposed design with \(K=3\) can achieve much higher throughput than the same design with \(K=2\) with a slight increase in area and critical path delay (lower clock frequency). As a result, the hardware efficiency of the design with \(K=3\) can achieve 572Mbps/mm\(^2\), which is the highest among the listed works.

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Design} & \text{This work}^1 & [3] & [5] & [9]^1 \\
\hline
\text{Message form} & \text{LLR} & \text{LLR} & \text{LL} & \text{LL} \\
\hline
\# of PE/path & 64 & 64 & 1025 & 64 \\
\hline
\text{Multi-bit decision} & \text{Yes} & \text{No} & \text{Yes} & \text{No} \\
\hline
\text{Tech.(nm)} & 65 & 90 & 65 & 90 \\
\hline
\text{Quantization.} & 6-bit & 6-bit & \text{Dynamic} & \text{Dynamic} \\
\hline
\text{A} & 2 & 65 & 1.8 & 4.10 \\
\hline
\text{N/A} & 3 & 1.18 & 794 & 288 \\
\hline
\text{Area (mm\(^2\))} & 0.94^1 & 1.78 & 2590 & 492 \\
\hline
\text{Freq. (MHz)} & 390 & 288 & 94 & 2520 \\
\hline
\text{Latency (Clock cycle)} & 1056 & 546 & 2648 & 1022 \\
\hline
\text{Throughput (Mbps)} & 387 & 675 & 307 & 288 \\
\hline
\text{Efficiency (Mbps/mm\(^2\))} & 402 & 572 & 172 & 70 \\
\hline
\end{array}
\]

\(^1\) The results have been scaled to 90nm.
\(^1\) Re-synthesis results for 64PE of each path are cited from [3].
\(^1\) The compensation operation for permutation matrix \(B\) has been embedded in the design of the proposed decoders.

Compared with the LL-based designs [5] and [9], the proposed design with \(K=3\) has 71% and 52% less area, respectively. In addition, its low decoding latency leads to 31% and 94.8% increase in throughput, respectively.

Compared with the LLR-SCL decoder in [3], the proposed design with \(K=3\) has 79.3% shorter latency, which translates to 133% increase in decoding throughput. It should be noted that the proposed works with \(K=2\) and 3 adopt data path balancing technique in [5] to reduce the critical path delay. If advanced technique, such as optimized sorting block in [3] is utilized, the clock frequency of the proposed designs will be further improved, thereby leading to even higher throughput and hardware efficiency.

B. Discussion on relevant works

In [3], a LLR-based SCL decoder was proposed. The derivation for the LLR representation in [3] was similar to the work in [4] with slight difference on the sign of path metrics. However, the bit-decision in [3][4] is serial, thereby causing low throughput. Different from these works, this paper enables the simultaneous decision of each \(2^k\) bits with the LLR representation; hence it can achieve much higher throughput and lower latency. For instance, as seen in Table I, the proposed design with \(K=3\) achieves 133% increase in data rate than [3].

In [9], a channel message compression scheme was proposed to reduce the memory requirement. However, because [9] is only an LL-based decoder, its silicon area is at least two times of the proposed design. Interestingly, because the area-optimizing techniques in [9] and this paper are performed at different levels, they can be jointly used to develop a more area-efficient decoder.

To address the long latency problem, multi-bit decision, or so-called parallel output was proposed in [5-6][11]. These literatures describe the reduced-latency technique in different manners, but all utilize the special recursive property of polar codes. However, different from those prior LL-based works, the proposed approach successfully enables multi-bit decision with LLR-based messages, thereby leading to great reduction in both computation complexity and memory requirement, which are very important for application of polar codes.

VI. CONCLUSION

In this paper we present LLR-2\(^k\)-b-SCL algorithm for polar codes decoding. The proposed algorithm can reduce complexity and decoding latency at the same time without performance loss. Then, based on the proposed algorithm, we develop the corresponding VLSI architecture. Hardware analysis shows that the proposed SCL decoders have significant reduction in area and decoding latency.

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