Design of Programmable Filter Based on MAX262

Yan-xi LI, Shun-kai XIANG, Ying-zhang LI, Yong YAN and Tao ZHANG

Wuhan University of Science and Technology, Institution of Information Science and Engineering, People’s Republic of China

Keywords: MAX262, Programmable filter, MSP430, DDS, MCU.

Abstract. A design scheme of programmable filter based on programmable filter chip MAX262 and MSP430F5529 is introduced in the paper. As a candidate in active filters, the function of switching between high pass and low pass mode and 1Khz step adjustment on cut-off frequency at -3dB from 1Khz at 20Khz in both modes could be performed. The overall design principle is expounded in the paper. Parameters of filter were designed and realized by means of software. To tackle the problem of providing with accurate clock frequency, this system used DDS signal generator as clock source. A small input is allowed because of the design of front amplifier section. Compared with the common active filter, the system solves the problem of parameter selection difficulty and equipped with a more stable ability in filtering.

Introduction

Traditional active filter is usually composed of operation amplification device and RC components. It has high requirements for the parameters of components and is difficult to test at the time of design. The programmable filter chip MAX262 produced by MAXIM is able to set up various parameters by software, so as to process a certain range of low frequency signal in low pass, high pass, band pass and band stop mode [1]. The system could also set up filter characteristic parameters such as filter quality factor and central frequency by programming in order to realize the change of filter performance.

System Design

This system is a program-controlled filter using MSP430F5529 ultra low power MCU from TI company as the control core. It includes program-controlled amplifier section and program-controlled filter section. The program-controlled amplifier section consists of a 20dB pre-amplifier section which is composed of a precision operational amplifier OPA227, a -40dB-20dB voltage amplification section composed of a voltage-controlled amplifier VCA810, and a 20dB post stage amplifier section composed of OPA227. The overall gain of the program-controlled amplifier is from 0dB - 60dB, with 10dB step adjustable. The VCA810 control voltage is provided by 12-bit dual channel digital to analog converter DAC7612 and OP07 inverter in serial input mode, so as to achieve the function of VCA810. Programmable filter section is composed of programmable filter chip MAX262 and digital-controlled analog switch CD4053, both of which are controlled directly by the MSP430 microcontroller. The mode selection as well as the settings of frequency and quality factor are made by software, to achieve cut-off frequency at -3dB equipped with 1kHz step adjustment in 1kHz ~ 20kHz range. CD4053 makes the two internal 2 twice-order filters cascaded to form a fourth-order filter for more reliable filtering performance. The clock of MAX262 is provided by the square wave output of the AD9850 - DDS section to get a more accurate cut-off frequency. The overall design block diagram is shown in Figure 1.
Hardware Design

Program-controlled Amplifying Circuit. As shown in Figure 2, the gain range of the voltage-controlled amplifier VCA810 is -40dB to 40dB, and the control voltage is from -2V to 0V. To ensure that the amplifier is in good linear state, the system use the part of -40dB to 20dB of voltage gain range, with the control voltage of 0V to -1.5V given by the DAC section [2]. In order to make the system expand the gain range, a front and a back stage amplifiers with a fixed gain of 20dB are added, so that the whole system is in the gain range of 0-60dB.

The front and the back amplifier circuit are set up by OPA227. Considering the influence of the practical error, the $R_l$ of the pre-amplifier is a variable resistor, so that the pre-amplifier is in an adjustable state to accurately meet the gain requirement, and the post amplification is fixed at 10 times. The control voltage of VCA810 is provided by the digital analog conversion chip DAC7612, using its serial input mode. It outputs voltage at the range of 0-1.5V according to the demand, with 0.25V step adjustment. Then an inverter composed of OP07 is used to make the final output voltage reach the range of 0V to -1.5V so as to meet VCA810's demand for control voltage. The program-controlled amplifying circuit is shown in Figure 3.
Program-controlled Filter Circuit. Programmable filter chip MAX262 internal is integrated with A, B two filters, which could make low pass and high pass mode selection. In order to meet the requirements of bandwidth and filter performance, the system use analog switch CD4053 to cascade two filters of MAX262, forming a fourth-order filter and achieving filter channel selection function. The cut-off frequency and quality factor of the filter are controlled by the program. The MAX262 mode 2 is low pass mode, the calculation of clock frequency and central frequency is shown in Eq. 1, and the calculation of the quality factor is shown in Eq. 2.

\[
\frac{f_{\text{clk}}}{f_0} = 1.11072(26+N) \tag{1}
\]

\[
Q = 90.51/(128-N) \tag{2}
\]

Mode 3 is high pass mode, the calculation of clock frequency and central frequency is shown in Eq. 3, and the calculation of quality factor is shown in Eq. 4. The N is the control word of the MAX262[3].

\[
\frac{f_{\text{clk}}}{f_0} = (26+N) \pi/2 \tag{3}
\]

\[
Q = 64/(128-N) \tag{4}
\]

In order to simplify the calculation, the control words are set as follows: AF=9, AQ=79, BF=9 and BQ=9. The function of step adjustment is realized by changing the \(f_{\text{clk}}\) to change the central frequency. The relation between the central frequency and the cut-off frequency of the low pass and the high pass mode are shown in Eq.5 and Eq.6.

\[
f_c = f_o \sqrt{(1 - \frac{1}{2Q^2}) + \sqrt{(1 - \frac{1}{2Q^2})^2 + 1}} \tag{5}
\]

\[
f_c = f_o \sqrt{(1 - \frac{1}{2Q^2}) + \sqrt{(1 - \frac{1}{2Q^2})^2 + 1}} \tag{6}
\]
In order to meet the requirements of the system, the system needs 40 different clock frequency values to change the central frequency of the system. Because of the difficulty and inaccuracy of realizing this kind of demand with the internal clock of MSP430, the system uses DDS chip AD9850 to output 40 different clock pulses in serial mode, providing MAX262 with different clock frequencies, which makes center frequency more accurate, so that to achieve better performance of filter function.

AD9850 clock pulse output is actually obtained through the built-in high-speed comparator of sine wave. The reference voltage comparator determines the duty cycle of the square wave at the same time. Using a special voltage regulator chip as the reference voltage, the reference voltage is more stable, so the stability of the square wave output is also higher. The program-controlled filter circuit is shown in Figure 4, and the circuit of AD9850 is shown in Figure 5.
Software Design

**Programming Method of MAX262.** The writing operation of MAX262 can make the address, data and control into the memory so that the system works, and its internal program address is assigned as shown in Table 1. The choices of central frequency and quality factor are determined by $D_0-D_1$ data bits and $A_0-A_1$ address bits. The type of data is determined by the address bits, and the data bits provide with the exact value of the written data [4]. The data value could be obtained by the relationship between the central frequency $F_0-F_5$ and $t$ the relationship between the quality factor $Q_0-Q_7$ from the datasheet.

| DATA BIT | ADDRESS | LOCATION |
|----------|---------|----------|
| D0       | D1      | A3       | A2 | A1 | A0 | FILTER A  |
| M0_A     | M1_A    | 0        | 0  | 0  | 1  | 0          |
| F0_A     | F1_A    | 0        | 0  | 0  | 0  | 1          |
| F2_A     | F3_A    | 0        | 0  | 1  | 0  | 2          |
| F4_A     | F5_A    | 0        | 0  | 1  | 1  | 3          |
| Q0_A     | Q1_A    | 0        | 1  | 0  | 0  | 4          |
| Q2_A     | Q3_A    | 0        | 1  | 0  | 0  | 5          |
| Q4_A     | Q5_A    | 0        | 1  | 1  | 0  | 6          |
| Q6_A     |         |          |    |    |    | 7          |
| FILTER B  |         |          |    |    |    |            |
| M0_B     | M1_B    | 1        | 0  | 0  | 0  | 8          |
| F0_B     | F1_B    | 1        | 0  | 0  | 1  | 9          |
| F2_B     | F3_B    | 1        | 0  | 0  | 1  | 10         |
| F4_B     | F5_B    | 1        | 0  | 0  | 1  | 11         |
| Q0_B     | Q1_B    | 1        | 1  | 0  | 0  | 12         |
| Q2_B     | Q3_B    | 1        | 1  | 0  | 0  | 13         |
| Q4_B     | Q5_B    | 1        | 1  | 1  | 0  | 14         |
| Q6_B     |         |          |    |    |    | 15         |

**Program Design.** The program flow chart of the system is shown in Figure 6. First, the controlled sections are initialized, including the DAC7612, the DDS chip AD9850, the keys and display screen LCD12864, MAX262. Once the key press is detected, it goes to the interrupt and determines which key is pressed. Key 1 is responsible for the gain selection of the amplifier voltage, and Key 2 is responsible for the selection of high pass mode cut-off frequency and Key 3 is responsible for the selection of low pass mode cut-off frequency. The final selection will be reflected by the display screen.
System Test

**Amplifier Test.** Use a sine wave with 20mVpp, 1Khz as the input signal and observe the results of different gains on the oscilloscope. The function of amplifier is stable, with the 1.59% error rate in average.

**Filter Test.** Use a sine wave with 10mVpp, 1KHz as the input signal of the whole system and observe the results of filtering performance of different cut-off frequencies and modes. The error rate of the system is controlled under 1.5%.

Summary

This system could accomplish the function of programmable filter for both low pass and high pass mode. Because of the design in amplifier, a small signal could be used as input. This kind of filter is easy to manage and operate with its stable performance and low energy cost. To improve the accuracy, the design approaches a DDS chip as the clock source, which is also a characteristic in this system.

References

[1] Ni Xiangdong. Design of dual channel active filter based on SCM[J]. Application of Electronic Technique, 2002, (1):16-18. DOI: 10.3969/j.issn.0258-7998.2002.01.005.
[2] Texas Instruments.VCA810 Datasheet.
[3] Texas Instruments.MAX262 Datasheet.
[4] Qian Yingjing, Li Feng. Design of program-controlled filter based on MAX262[J]. Journal of Huaihua University, 2008, (11):45-47. DOI: 10.3969/j.issn.1671-9743.2008.11.014.