FATAL+: A Self-Stabilizing Byzantine Fault-tolerant Clocking Scheme for SoCs

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Abstract—We present concept and implementation of a self-stabilizing Byzantine fault-tolerant distributed clock generation scheme for multi-synchronous GALS architectures in critical applications. It combines a variant of a recently introduced self-stabilizing algorithm for generating low-frequency, low-accuracy synchronized pulses with a simple non-stabilizing high-frequency, high-accuracy clock synchronization algorithm. We provide thorough correctness proofs and a performance analysis, which use methods from fault-tolerant distributed computing research but also addresses hardware-related issues like metastability. The algorithm, which consists of several concurrent communicating asynchronous state machines, has been implemented in VHDL using Petrify in conjunction with some extensions, and synthesized for an Altera Cyclone FPGA. An experimental validation of this prototype has been carried out to confirm the skew and clock frequency bounds predicted by the theoretical analysis, as well as the very short stabilization times (required for recovering after excessively many transient failures) achievable in practice.

I. INTRODUCTION

To circumvent the cumbersome clock tree engineering issue [1], [2], [3], [4], systems-on-chip (SoC) are nowadays increasingly designed globally asynchronous locally synchronous (GALS) [5]. Using independent and hence unsynchronized clock domains requires asynchronous cross-domain communication mechanisms or synchronizers [6], [7], [8], however, which inevitably create the potential for metastability [9]. This problem can be circumvented by means of multi-synchronous clocking [10], [11], which guarantees a certain degree of synchrony between clock domains. Multi-synchronous GALS is particularly beneficial from a designer’s point of view, since it combines the convenient local synchrony of a GALS system with a global time base across the whole chip, including the ability for metastability-free high-speed communication across clock domains [12].

The decreasing feature sizes of deep submicron VLSI technology also resulted in an increased likelihood of chip components failing during operation: Reduced voltage swings and smaller critical charges make circuits more susceptible to ionized particle hits, crosstalk, and electromagnetic interference [13], [14], [15], [16], [17], [18]. Fault-tolerance hence becomes an increasingly pressing issue also for chip design. Unfortunately, faulty components may behave non-benign in many ways: They may perform signal transitions at arbitrary times and even convey inconsistent information to their successor components if their outputs are affected by a failure. Well-known theory on fault-tolerant agreement and synchronization shows that this behaviour is the key feature of unrestricted, i.e., Byzantine faults [19]. This forces to model faulty components as Byzantine if a high fault coverage is to be guaranteed.

Unfortunately, lower-bound results [19], [20] reveal that, in order to cope with some maximum number $f$ of Byzantine faulty components (say, processors) throughout an execution of a system, $n \geq 3f + 1$ components are required. Given the typically transient nature of failures in digital circuits, these bounds reveal that even a Byzantine fault-tolerant system cannot be expected to recover from a situation where more than $f$ components became faulty transiently, since their state may be corrupted. Dealing with this problem is in the realm of self-stabilizing algorithms [21], which are guaranteed to recover even if each and every component of the system fails arbitrarily, but later on works according to its specification again: in that case the system resumes correct operation after some stabilization time following the instant when no more failures occur. Byzantine-tolerant self-stabilizing algorithms [22], [23], [24], [25], [26], [27], [28] combine the best of both worlds, by guaranteeing both correct operation and self-stabilization in the presence of up to $f$ Byzantine faulty components in the system.

This paper presents concept and prototype implementation of a novel approach, termed FATAL+, for multi-synchronous clocking in GALS systems. It relies on a self-stabilizing and Byzantine fault-tolerant distributed algorithm, consisting of $n$ identical instances (called nodes), which generate $n$ local clock signals (one for each clock domain) with the following properties: Bounded skew, i.e., bounded maximum time
between the \( k \)-th clock transitions of any two clock signals of correct nodes, and bounded accuracy (i.e., frequency), i.e., bounded minimum and maximum time between the occurrence of any two successive clock transitions of the clock signal at any correct node. At most \( f < n/3 \) nodes may behave Byzantine faulty, in which case their clock signals may be arbitrary. The whole algorithm can be directly implemented in hardware, without quartz oscillators, using standard asynchronous logic gates only.

FATAL\(^+\) self-stabilizes within \( O(kn) \) time with probability \( 1 - 2^{-k(n-f)} \) (with constant expectation in typical settings), and is metastability-free by construction after stabilization in failure-free runs.\(^1\) If the number of faults is not overwhelming, i.e., a majority of at least \( n-f \) nodes continues to execute the protocol in an orderly fashion, recovering nodes and late joiners (re)synchronize deterministically in constant time.

**Detailed contributions:** (1) In Sections \(^1\)[II][V] we present concept and theoretical analysis of FATAL\(^+\), which is based on a variant of the randomized self-stabilizing Byzantine-tolerant pulse synchronization algorithm \(^2\)[28] we recently proposed. It eventually generates synchronized periodic pulses with moderate skew and low frequency, and improves upon the results from \(^2\)[28] in that it tolerates arbitrarily large clock drifts and allows late joiners or nodes recovering from transient faults to deterministically resynchronize within constant time. The formal proof of these properties builds upon and extends the analysis in \(^2\)[30]. In Section VI, this algorithm is integrated with a Byzantine-tolerant but non-self-stabilizing tick generation algorithm based on Srikanth & Toueg's clock synchronization algorithm \(^3\)[31], operating in a control loop: The latter, referred to as the quick cycle algorithm, generates clock ticks with high frequency and small skew, which also (weakly) affect pulse generation. On the other hand, quick cycle uses pulses to monitor its ticks in order to detect the need for stabilization.

(2) In Section VII we present the major ingredients of an Altera Cyclone IV FPGA prototype implementation of FATAL\(^+\). It primarily consists of multiple hybrid (asynchronous + synchronous) state machines, which have been generated semi-automatically from the specification of the algorithms using Petriy \(^4\)[32]. Non-standard extensions were needed for ensuring deadlock-free communication despite arbitrarily many desynchronized nodes, some of which could be Byzantine faulty, which e.g. forced us to use state-based communication instead of handshake-based communication. Special care had also to be exercised for ensuring self-stabilizing elementary building blocks and metastability-freedom in normal operation (after stabilization).

(3) In Section VIII we provide some results of the experimental evaluation of our prototype implementation. They demonstrate the feasibility of FATAL\(^+\) and confirm the results of our theoretical analysis, in particular, a tight skew bound, in the presence of Byzantine faulty nodes. Special emphasis has been put on experiments validating the predictions related to stabilization time, which revealed that the system indeed stabilizes in very short time from any initial/error state.

Section IX eventually concludes our paper.

**Related work:** The work \(^3\)[33], \(^3\)[34], \(^3\)[35], \(^3\)[36] on distributed clock generation in VLSI circuits is essentially based on (distributed) ring oscillators, formed by regular structures (rings, meshes) of multiple inverter loops. Since clock synchronization theory \(^5\)[20] reveals that high connectivity is required for bounded synchronization tightness in the presence of failures, these approaches are fundamentally restricted in that they can overcome at most a small constant number of Byzantine failures.

The only exception we are aware of is the DARTS fault-tolerant clock generation approach \(^3\)[37], \(^3\)[38], which also addresses multi-synchronous clocking in GALS systems. Like FATAL\(^+\), DARTS is based on a fault-tolerant distributed algorithm \(^3\)[39] implemented in asynchronous digital logic. Although it shares many features with FATAL\(^+\), including Byzantine fault-tolerance, it is not self-stabilizing: If more than \( f \) nodes ever become faulty, the system will not recover even if all nodes work correctly thereafter. Moreover, in DARTS, simple transient faults such as radiation- or crosstalk-induced additional (or omitted) clock ticks accumulate over time to arbitrarily large skews in an otherwise benign execution. Despite not suffering from these drawbacks, FATAL\(^+\) offers similar guarantees in terms of area consumption, clock skew, and amortized frequency as DARTS.

Furthermore, a number of Byzantine-tolerant self-stabilizing clock synchronization protocols \(^3\)[23], \(^3\)[24], \(^3\)[24], \(^3\)[25], \(^3\)[26], \(^3\)[27] have been devised by the distributed systems community. Beyond optimal resilience, an attractive feature of most of these protocols is a small stabilization time. However, all of them exhibit deficiencies rendering them unsuitable in the VLSI context. This motivated to devise an improved variant of which forms the basis of FATAL\(^+\).

**II. Model**

In this section we introduce our system model. Our formal framework will be tied to the peculiarities of hardware designs, which consist of modules that continuously compute their output signals based on their input signals.

\(^1\) It is easy to see that, metastable upsets cannot be ruled out in executions involving Byzantine faulty. However, they can be made as unlikely as desired by using synchronizers or elastic pipelines acting as metastability filters [29].

\(^2\) In sharp contrast to classic distributed computing models, there is no computationally complex discrete zero-time state-transition here.
Signals

Following [40, 41], we define (the trace of) a signal to be a timed event trace over a finite alphabet \( S \) of possible signal states: Formally, signal \( \sigma \in S \times \mathbb{R}_0^+ \). All times and time intervals refer to a global reference time taken from \( \mathbb{R}_0^+ \), that is, signals reflect the system’s state from time 0 on. The elements of \( \sigma \) are called events, and for each event \((s, t)\) we call \( s \) the state of event \((s, t)\) and \( t \) the time of event \((s, t)\). In general, a signal \( \sigma \) is required to fulfill the following conditions: (i) for each time interval \([t^-, t^+]\) \( \subseteq \mathbb{R}_0^+ \) of finite length, the number of events in \( \sigma \) with times within \([t^-, t^+]\) is finite, (ii) from \( s \in \mathbb{R}_0^+ \), \( \sigma \) is required to be a timed event trace over a finite alphabet \( S \). 

Note that our definition allows for events \((s, t)\) and \((s', t')\) \( \in \sigma \), where \( t < t' \), without having an event \((s', t')\) \( \in \sigma \) with \( s' \neq s \) and \( t < t' < t' \). In this case, we call event \((s, t')\) idempotent. Two signals \( \sigma \) and \( \sigma' \) are equivalent, if \( \sigma \) and \( \sigma' \) differ in idempotent events only. We identify all signals of an equivalence class, as they describe the same physical signal. Each equivalence class \([\sigma]\) of signals contains a unique signal \( \sigma_0 \) having no idempotent events. We say that \( \sigma \) switches to \( s \) at time \( t \) iff event \((s, t)\) \( \in \sigma_0 \).

The state of signal \( \sigma \) at time \( t \in \mathbb{R}_0^+ \), denoted by \( \sigma(t) \), is given by the state of the event with the maximum time not greater than \( t \). Because of (i), (ii) and (iii), \( \sigma(t) \) is well defined for each time \( t \in \mathbb{R}_0^+ \). Note that \( \sigma \)’s state function in fact depends on \([\sigma]\) only, i.e., we may add or remove idempotent events at will without changing the state function.

Distributed System

On the topmost level of abstraction, we see the system as a set of \( V = \{1, \ldots, n\} \) physically remote nodes that communicate by means of channels. In the context of a VLSI circuit, “physically remote” actually refers to quite small distances (centimeters or even less). However, at gigahertz frequencies, a local state transition will not be observed remotely within a time that is negligible compared to clock speeds. We stress this point, since it is crucial that different clocks (and their attached logic) are not placed too close to each other, as otherwise they might fail due to the same event such as a particle hit. This would render it pointless to devise a system that is resilient to a certain fraction of the nodes failing.

Each node \( i \) comprises a number of input ports, namely \( S_{i,j} \) for each node \( j \), an output port \( S_i \), and a set of local ports, introduced later on. An execution of the distributed system assigns to each port of each node a signal. For convenience of notation, for any port \( p \), we refer to the signal assigned to port \( p \) simply by signal \( p \). We say that node \( i \) is in state \( s \) at time \( t \) iff \( S_i(t) = s \). We further say that node \( i \) switches to state \( s \) at time \( t \) iff signal \( S_i \) switches to \( s \) at time \( t \).

Nodes exchange their states via the channels between them: for each pair of nodes \( i, j \), output port \( S_i \) is connected to input port \( S_{j,i} \) by a FIFO channel from \( i \) to \( j \). Note that this includes a channel from \( i \) to \( i \) itself. Intuitively, \( S_i \) being connected to \( S_{j,i} \) by a (non-faulty) channel means that \( S_{j,i} \) should mimic \( S_i \), however, with a slight delay accounting for the time it takes the channel to propagate events. In contrast to an asynchronous system, this delay is bounded by the maximum delay \( d > 0 \).

Formally we define: The channel from node \( i \) to \( j \) is said to be correct during \([t^-, t^+]\) iff there exists a function \( \tau_{i,j} : \mathbb{R}_0^+ \rightarrow \mathbb{R}_0^+ \), called the channel’s delay function, such that: (i) \( \tau_{i,j} \) is continuous and strictly increasing, (ii) \( \forall t \in [\max(t^-, \tau_{i,j}(0)), t^+]: 0 < t - \tau_{i,j}^{-1}(t) < d \), and (iii) for each \( t \in [\max(t^-, \tau_{i,j}(0)), t^+] \), \((s, t) \in S_{j,i} \Leftrightarrow (s, \tau_{i,j}^{-1}(t)) \in S_i \), and for each \( t \in [t^-, \tau_{i,j}(0)) \), \((s, t) \in S_{j,i} \Rightarrow s = S_i(0) \). Note that because of (i), \( \tau_{i,j}^{-1} \) exists in the domain \([\tau_{i,j}(0), \infty)\), and thus (ii) and (iii) are well defined. We say that node \( i \) observes node \( j \) in state \( s \) at time \( t \) if \( S_{j,i}(t) = s \).

Clocks and Timeouts

Nodes are never aware of the current reference time and we also do not require the reference time to resemble Newtonian “real” time. Rather we allow for physical clocks that run arbitrarily fast or slow as long as their speeds are close to each other in comparison. One may hence think of the reference time as progressing at the speed of the currently slowest correct clock. In this framework, nodes essentially make use of bounded clocks with bounded drift.

Formally, clock rates are within \([1, \vartheta]\) (with respect to reference time), where \( \vartheta > 1 \) is constant and \( \vartheta - 1 \) is the (maximum) clock drift. A clock \( C \) is a continuous, strictly increasing function \( C : \mathbb{R}_0^+ \rightarrow \mathbb{R}_0^+ \) mapping reference time to some local time. Clock \( C \) is said to be correct during \([t^-, t^+] \subseteq \mathbb{R}_0^+ \) iff we have for any \( t, t' \in [t^-, t^+] \), \( t < t' \), that \( t' - t \leq C(t') - C(t) \leq \vartheta(t' - t) \). Each node comprises a set of clocks assigned to it, which allow the node to estimate the progress of reference time.

Instead of directly accessing the value of their clocks, nodes have access to so-called timeout ports of watchdog timers. A timeout is a triple \((T, s, C)\), where \( T \in \mathbb{R}_0^+ \) is a duration, \( s \in S \) is a state, and \( C \) is some local clock (there may be several), say of node \( i \). Each timeout \((T, s, C)\) has a corresponding timeout port \( \text{Time}_{T,s,C} \), being part of node \( i \)'s local ports. Signal \( \text{Time}_{T,s,C} \) is Boolean, that is, its possible states are from the set \([0, 1]\). We say that timeout \((T, s, C)\)
is correct during \([t^-, t^+] \subseteq \mathbb{R}_+^\ast\) iff clock \(C\) is correct during \([t^-, t^+]\) and the following holds:

1) For each time \(t_s \in [t^-, t^+]\) when node \(i\) switches to state \(s\), there is a time \(t \in [t_s, \tau_{i, i}(t_s)]\) such that \((T, s, C)\) is reset, i.e., \((0, t) \in \text{Time}_{T, s, C}\). This is a one-to-one correspondence, i.e., \((T, s, C)\) is not reset at any other times.

2) For a time \(t \in [t^-, t^+]\), denote by \(t_0\) the supremum of all times from \([t^-, t]\) when \((T, s, C)\) is reset. Then it holds that \((1, t) \in \text{Time}_{T, s, C}\) iff \(C(t) - C(t_0) = T\). Again, this is a one-to-one correspondence.

We say that timeout \((T, s, C)\) expires at time \(t\) iff \(\text{Time}_{T, s, C}\) switches to 1 at time \(t\), and it is expired at time \(t\) iff \(\text{Time}_{T, s, C}(t) = 1\). For notational convenience, we will omit the clock \(C\) and simply write \((T, s)\) for both the timeout and its signal.

A randomized timeout is a triple \((D, s, C)\), where \(D\) is a bounded random distribution on \(\mathbb{R}_0^\ast\), \(s \in \mathbb{S}\) is a state, and \(C\) is a clock. Its corresponding timeout port \(\text{Time}_{D, s, C}\) behaves very similar to the one of an ordinary timeout, except that whenever it is reset, the local time that passes until it expires next—provided that it is not reset again before that happens—follows the distribution \(D\). Formally, \((D, s, C)\) is correct during \([t^-, t^+] \subseteq \mathbb{R}_0^+\), if \(C\) is correct during \([t^-, t^+]\) and the following holds:

1) For each time \(t_s \in [t^-, t^+]\) when node \(i\) switches to state \(s\), there is a time \(t \in [t_s, \tau_{i, i}(t_s)]\) such that \((D, s, C)\) is reset, i.e., \((0, t) \in \text{Time}_{D, s, C}\). This is a one-to-one correspondence, i.e., \((D, s, C)\) is not reset at any other times.

2) For a time \(t \in [t^-, t^+]\), denote by \(t_0\) the supremum of all times from \([t^-, t]\) when \((D, s, C)\) is reset. Let \(\mu : \mathbb{R}_0^+ \rightarrow \mathbb{R}_0^+\) denote the density of \(D\). Then \((1, t) \in \text{Time}_{D, s, C}\) “with probability \(\mu(C(t) - C(t_0))\)” and we require that the probability of \((1, t) \in \text{Time}_{D, s, C}\)—conditional to \(t_0\) and \(C\) on \([0, t]\) being given—is independent of the system’s state at times smaller than \(t\). More precisely, if \(E\) identifies variables in execution \(E\) and \(t_0\) is the infimum of all times from \((t_0, t]\) when node \(i\) switches to state \(s\), then we demand for any \([\tau^-, \tau^+] \subseteq [t_0, t]\) that

\[
P \left( \exists t' \in [\tau^-, \tau^+] : (1, t') \in \text{Time}_{D, s, C} \right)
= \int_{\tau^-}^{\tau^+} \mu(C(\tau) - C(t_0)) d\tau,
\]

independently of \(E\) if \(t < t_0\).

We will apply the same notational conventions to randomized timeouts as we do for regular timeouts.

Note that, strictly speaking, this definition does not induce a random variable describing the time \(t' \in [t_0, t'_0]\) satisfying

\[
(1, t') \in \text{Time}_{D, s, C}.
\]

However, for the state of the timeout port, we get the meaningful statement that for any \(t' \in [t_0, t'_0]\),

\[
P[\text{Time}_{D, s, C} \text{ switches to } 1 \text{ during } [t_0, t']] = \int_{t_0}^{t'} \mu(C(\tau) - C(t_0)) d\tau.
\]

The reason for phrasing the definition in the above more cumbersome way is that we want to guarantee that an adversary knowing the full present state of the system and memorizing its whole history cannot reliably predict when the timeout will expire.

We remark that these definitions allow for different timeouts to be driven by the same clock, implying that an adversary may derive some information on the state of a randomized timeout before it expires from the node’s behavior, even if it cannot directly access the values of the clock driving the timeout. This is crucial for implementability, as it might be very difficult to guarantee that the behavior of a dedicated clock that drives a randomized timeout is indeed independent of the execution of the algorithm.

Memory Flags

Besides timeout and randomized timeout ports, another kind of node \(i\)’s local ports are memory flags. For each state \(s \in \mathbb{S}\) and each node \(j \in V\), \(\text{Mem}_{i, j, s}\) is a local port of node \(i\). It is used to memorize whether node \(i\) has observed node \(j\) in state \(s\) since the last reset of the flag. We say that node \(i\) memorizes node \(j\) in state \(s\) at time \(t\) if \(\text{Mem}_{i, j, s}(t) = 1\). Formally, we require that signal \(\text{Mem}_{i, j, s}\) switches to 1 at time \(t\) iff node \(i\) observes node \(j\) in state \(s\) at time \(t\) and \(\text{Mem}_{i, j, s}\) is not already in state 1. The times \(t\) when \(\text{Mem}_{i, j, s}\) switches to 1, i.e., \((0, t) \in \text{Mem}_{i, j, s}\), are specified by node \(i\)’s state machine, which is introduced next.

State Machine

It remains to specify how nodes switch states and when they reset memory flags. We do this by means of state machines that may attain states from the finite alphabet \(\mathbb{S}\). A node’s state machine is specified by (i) the set \(\mathbb{S}\), (ii) a function \(tr\), called the transition function, from \(T \subseteq \mathbb{S}^2\) to the set of Boolean predicates on the alphabet consisting of expressions “\(p = s\)” (used for expressing guards), where \(p\) is from the node’s input and local ports and \(s\) is from the set of possible states of signal \(p\), and (iii) a function \(re\), called the reset function, from \(T\) to the power set of the node’s memory flags.

Intuitively, the transition function specifies the conditions (guards) under which a node switches states, and the reset

\[\text{This is a non-trivial property. For instance nodes could just determine, by drawing from the desired random distribution at time } t_0, \text{ at which local clock value the timeout shall expire next. This would, however, essentially reveal when the timeout will expire prematurely, greatly reducing the power of randomization!}\]
function determines which memory flags to reset upon the state change. Formally, let \( P \) be a predicate on node \( i \)'s input and local ports. We define \( P \) holds at time \( t \) by structural induction: If \( P \) is equal to \( p = s \), where \( p \) is one of node \( i \)'s input and local ports and \( s \) is one of the states signal \( \tau_1 \), then \( P \text{ holds at time } t \text{ iff } p(t) = s. \) Otherwise, if \( P \) is of the form \( \neg P_1, P_2 \land P_2, \) or \( P_1 \lor P_2 \), we define \( P \text{ holds at time } t \) in the straightforward manner.

We say node \( i \) follows its state machine during \([t^-, t^+]\) iff the following holds: Assume node \( i \) observes itself in state \( s \in S \) at time \( t \in [t^-, t^+] \), i.e., \( S_{i,t}(t) = s \). Then, for each \((s, s') \in T\), both:

1) Node \( i \) switches to state \( s' \) at time \( t \) iff \( tr(s, s') \) holds at time \( t \) and \( i \) is not already in state \( s' \). (In case more than one guard \( tr(s, s') \) can be true at the same time, we assume that an arbitrary tie-breaking ordering exists among the transition guards that specifies to which state to switch.)

2) Node \( i \) resets memory flag \( m \) at some time in the interval \([t, t_{\tau_i}(t)]\) iff \( m \in re(s, s') \) and \( i \) switches from state \( s \) to state \( s' \) at time \( t \). This correspondence is one-to-one.

A node is defined to be non-faulty during \([t^-, t^+]\) if all its timeouts and randomized timeouts are correct and it follows its state machine. If it employs multiple state machines (see below), it needs to follow all of them.

In contrast, a faulty node may change states arbitrarily. Note that while a faulty node may be forced to send consistent output state signals to all other nodes if its channels remain correct, there is no way to guarantee that this still holds true if channels are faulty.

Metastability

While the presented model does not fully capture propagation and decay of metastable upsets, i.e., the propagation of intermediate values through combinational circuit elements, and the probability distributions on the decay of metastable upsets, it allows to capture its generation. An algorithm is inherently susceptible to metastability by the lacking capability of state machines to instantaneously take on new states: Node \( i \) decides on state transitions based on the delayed status of port \( S_{i,2} \) instead of its "true" current state \( S_i \). Consider the following example: Node \( i \) is in state \( s \) at some time \( t \), but since it switched to \( s \) only very recently, it still observes itself in state \( s' \neq s \) at time \( t \). A metastable upset might occur at time \( t \) (i) if the guard \( tr(s', s) \) falls back to false at time \( t \), or (ii) if there is another transition \((s', s'')\) in \( T \) whose guard becomes true at time \( t \). The treatment of scenario (i) is postponed to Section VII where it is discussed together with the implementation of a node's components. Scenario (ii) is accounted for in the following definition:

Definition 2.1 (Metastability-Freedom): We denote state machine \( M \) of node \( i \) as being metastability-free during \([t^-, t^+]\), iff for each time \( t \in [t^-, t^+] \) when \( M \) switches from some state \( s \in S \) to another state \( s' \in S \), it holds that \( \tau_{i,t}(t) < t' \), where \( t' \) is the infimum of all times in \([t, t^+]\) when \( M \) switches to some state \( s'' \).

Multiple State Machines

In some situations the previous definitions are too stringent, as there might be different "components" of a node's state machine that act concurrently and independently, mostly relying on signals from disjoint input ports or orthogonal components of a signal. We model this by permitting that nodes run several state machines in parallel. All these state machines share the input and local ports of the respective node and are required to have disjoint state spaces. If node \( i \) runs state machines \( M_1, \ldots, M_k \), node \( i \)'s output signal is the product of the output signals of the individual machines. Formally we define: Each of the state machines \( M_j, 1 \leq j \leq k \), has an additional own output port \( s_j \). The state of node \( i \)'s output port \( S_i \) at any time \( t \) is given by \( S_i(t) := (s_1(t), \ldots, s_k(t)) \), where the signals of ports \( s_1, \ldots, s_k \) are defined analogously to the signals of the output ports of state machines in the single state machine case. Note that by this definition, the only (local) means for node \( i \)'s state machines to interact with each other is by reading the delayed state signal \( S_{i,2} \).

We say that node \( i \)'s state machine \( M_j \) is in state \( s \) at time \( t \) iff \( s_j(t) = s \), where \( s_j(t) = (s_1(t), \ldots, s_k(t)) \), and that node \( i \)'s state machine \( M_j \) switches to state \( s' \) at time \( t \) iff \( s_j \) switches to \( s' \) at time \( t \). Since the state spaces of the machines \( M_j \) are disjoint, we will omit the phrase "state machine \( M_j \)" from the notation, i.e., we write "node \( i \) is in state \( s'' \)" or "node \( i \) switched to state \( s'' \), respectively.

Recall that the various state machines of node \( i \) are as loosely coupled as remote nodes, namely via the delayed status signal on channel \( S_{i,2} \). Therefore, it makes sense to consider them independently also when it comes to metastability.

Definition 2.2 (Metastability-Freedom—Multiple SM's): We denote state machine \( M \) of node \( i \in V \) as metastability-free during \([t^-, t^+]\), iff for each time \( t \in [t^-, t^+] \) when \( M \) switches from some state \( s \in S \) to another state \( s' \in S \), it holds that \( \tau_{i,t}(t) < t' \), where \( t' \) is the infimum of all times in \([t, t^+]\) when \( M \) switches to some state \( s'' \in S \). Note that by this definition the different state machines may switch states concurrently without suffering from...
metastability. It is even possible that some state machine suffers metastability, while another is not affected by this at all.

**Problem Statement**

The purpose of the pulse synchronization protocol is that nodes generate synchronized, well-separated pulses by switching to a distinguished state accept. Self-stabilization requires that it starts to do so within a bounded time, for any possible initial state. However, as our protocol makes use of randomization, there are executions where this does not happen at all; instead, we will show that the protocol stabilizes with probability one in finite time. To give a precise meaning to this statement, we need to define appropriate probability spaces.

**Definition 2.3 (Adversarial Spaces):** Denote for \( i \in V \) by \( C_i = (C_{i,1}, \ldots, C_{i,n}) \) the tuple of clocks of node \( i \). An adversarial space is a probabilistic space that is defined by subsets of nodes and channels \( W \subseteq V \) and \( E \subseteq V^2 \), a time interval \([t^-, t^+]\), a protocol \( \mathcal{P} \) (nodes’ ports, state machines, etc.) as previously defined, tuple of all clocks \( (C_{i,1}, \ldots, C_{i,n}) \), a function \( \Theta \) assigning each \((i,j) \in V^2\) a delay \( \tau_{i,j} : \mathbb{R}^+_0 \rightarrow \mathbb{R}^+_0 \), an initial state \( \mathcal{E}_0 \) of all ports, and an adversarial function \( \mathcal{A} \). Here \( \mathcal{A} \) is a function that maps a partial execution \( \mathcal{E}[(0,0)] \) until time \( t \) (i.e., all ports’ values until time \( t \)), \( W, E, [t^-, t^+] \), \( \mathcal{P}, \mathcal{C}, \) and \( \Theta \) to the states of all faulty ports during the time interval \((t, t')\), where \( t' \) is the infimum of all times greater than \( t \) when a non-faulty node or channel switches states.

The adversarial space \( \mathcal{A} \mathcal{S}(W, E, [t^-, t^+], \mathcal{P}, \mathcal{C}, \Theta, \mathcal{E}_0, \mathcal{A}) \) is now defined on the set of all executions \( \mathcal{E} \) satisfying that (i) the initial state of all ports is given by \( \mathcal{E}[(0,0)] = \mathcal{E}_0 \), (ii) for all \( i \in V \) and \( k \in \{1, \ldots, c_i\} : C_{i,k}^E = C_{i,k} \), (iii) for all \((i,j) \in V^2\) and \( \tau_{i,j}^E = \tau_{i,j} \), (iv) non-faulty during \([t^-, t^+]\) with respect to the protocol \( \mathcal{P} \), (v) all channels in \( E \) are correct during \([t^-, t^+]\), and (vi) given \( \mathcal{E}[(0,0)] \) for any time \( t, \mathcal{E}[(t,t')] \) is given by \( \mathcal{A} \), where \( t' \) is the infimum of times greater than \( t \) when a non-faulty node switches states. Thus, except for when randomized timeouts expire, \( \mathcal{E} \) is fully predetermined by the parameters of \( \mathcal{A} \mathcal{S} \).

The probability measure on \( \mathcal{A} \mathcal{S} \) is induced by the random distributions of the randomized timeouts specified by \( \mathcal{P} \).

To avoid confusion, observe that if the clock functions and delays do not follow the model constraints during \([t^-, t^+]\), the respective adversarial space is empty and thus of no concern. This cumbersome definition provides the means to formalize a notion of stabilization that accounts for worst-case drifts and delays and an adversary that knows the full state of the system up to the current time.

We are now in the position to formally state the pulse synchronization problem in our framework. Intuitively, the goal is that after transient faults cease, nodes should with probability one eventually start to issue well-separated, synchronized pulses by switching to a dedicated state accept. Thus, as the initial state of the system is arbitrary, specifying an algorithm is equivalent to defining the state machines that run at each node, one of which has a state accept.

**Definition 2.4 (Self-Stabilizing Pulse Synchronization):** Given a set of nodes \( W \subseteq V \) and a set \( E \subseteq V \times V \) of channels, we say that protocol \( \mathcal{P} \) is a \((W, E)\)-stabilizing pulse synchronization protocol with skew \( \Sigma \) and accuracy bounds \( T^- > \Sigma \) and \( T^+ \) that stabilizes within time \( T \) with probability \( p \) iff the following holds. Choose any time interval \([t^-, t^+] \supseteq [t^-, t^+ + T + \Sigma]\) and any adversarial space \( \mathcal{A} \mathcal{S}(W, E, [t^-, t^+], \mathcal{P}, \mathcal{C}, \Theta, \mathcal{E}_0, \mathcal{A}) \) (i.e., \( \mathcal{C}, \mathcal{P}, \mathcal{E}_0 \), and \( \mathcal{A} \) are arbitrary). Then executions from \( \mathcal{A} \mathcal{S} \) satisfy with probability at least \( p \) that there exists a time \( t_s \in [t^-, t^+ + T] \) so that, denoting by \( t_s(k) \) the time when node \( i \in W \) switches to a distinguished state accept for the \( k \)-th time after \( t_s \), \( t_s(k) = \infty \) if no such time exists, (i) \( t_s(1) \in (t_s, t_s + \Sigma) \), (ii) \( |t_s(k) - t_j(k)| \leq \Sigma \) if max\{\( t_i(k), t_j(k) \)\} \( \leq t^+ \), and (iii) \( T^- \leq |t_s(k + 1) - t_s(k)| \leq T^+ \) if \( t_s(k) + T^+ \leq t^+ \).

Note that the fact that \( \mathcal{A} \) is a deterministic function and, more generally, that we consider each space \( \mathcal{A} \mathcal{S} \) individually, is no restriction: As \( \mathcal{P} \) succeeds for any adversarial space with probability at least \( p \) in achieving stabilization, the same holds true for randomized adversarial strategies \( \mathcal{A} \) and worst-case drifts and delays.

### III. The FATAL Pulse Synchronization Protocol

In this section, we present our self-stabilizing pulse generation algorithm. In order to be suitable for implementation in hardware, it needs to utilize very simple rules only. It is stated in terms of state machines as introduced in the previous section.

Since the ultimate goal of the pulse generation algorithm is to interact with an application layer, we introduce a possibility for a coupling with such a layer in the pulse generation algorithm itself: for each node \( i \), we add a further port \( \text{NEXT}_i \), which can be driven by node \( i \)'s application layer. As for other state signals, its output raises flag...
Mem_{i,NEXT}, to which for simplicity we refer to as NEXT, as well. The purpose of the port is to allow the application layer to influence the time between two of node i’s successively generated pulses within a range that does not prevent the pulse generation algorithm to stabilize correctly.

In Section VI we give an example for an application layer: The quick cycle completing the FATAL is a non-self-stabilizing clock synchronization routine which relies on the pulse generation algorithm for self-stabilization. Since we will show that the pulse algorithm stabilizes independently of the behavior of the NEXT signal, and the clock synchronization routine presented in Section VI is designed such that it will stabilize once the pulse generation algorithm did so, we can partition the analysis of the compound algorithm into two parts. When proving the correctness of the pulse generation algorithm in Section IV we thus assume that for each node i, NEXT, is arbitrary.

A. Basic Cycle

The full pulse generation algorithm makes use of a rather involved interplay between conditions on timeouts, states, and thresholds to converge to a safe state despite a limited number of faulty components. As our approach is thus complicated to present in bulk, we break it down into pieces. Moreover, to facilitate giving intuition about the key ideas of the algorithm, in this subsection we assume that there are never more than $f < n/3$ faulty nodes, i.e., the remaining $n-f$ nodes are non-faulty within $[0, \infty)$. We further assume that channels between non-faulty nodes (including loopback channels) are correct within $[0, \infty)$. We start by presenting the basic cycle that is repeated every pulse once a safe configuration is reached (see Figure 1).

We employ graphical representations of the state machine of each node $i \in V$. States are represented by circles containing their names, while transition $(s, s') \in T$ is depicted as an arrow from $s$ to $s'$. The guard $tr(s, s')$ is written as a label next to the arrow, and the reset function’s value $re(s, s')$ is depicted in a rectangular box on the arrow. To keep labels more simple we make use of some abbreviations. Recall that in the notation of timeouts $(T, s, C)$ the driving clock $C$ is omitted. We write $T$ instead of $(T, s)$ if $s$ is the same state which node $i$ leaves if the condition involving $(T, s)$ is satisfied. Threshold conditions like “$\geq f + 1$ s”, where $s \in S$, abbreviate Boolean predicates that reach over all of node i’s memory flags $\text{Mem}_{i,j,s}$, where $j \in V$, and are defined in a straightforward manner. If in such an expression we connect two states by “or”, e.g., “$\geq n-f$ s or $s'$” for $s, s' \in S$, the summation considers flags of both types $s$ and $s'$. Thus, such an expression is equivalent to $\sum_{j \in V} \max\{\text{Mem}_{i,j,s}, \text{Mem}_{i,j,s'}\} \geq f + 1$. For any state $s \in S$, the condition $s_{i,1} = s$, (respectively, $\neg(s_{i,1} = s)$) is written in short as “in s” (respectively, “not in s”). We write “true” instead of a condition that is always true (like e.g. “(in s) or (not in s)” for an arbitrary state $s \in S$). Finally, $re(\cdot, \cdot)$ always requires to reset all memory flags of certain types, hence we write e.g. $\text{propose}$ if all flags $\text{Mem}_{i,j,\text{propose}}$ are to be reset.

We now briefly introduce the basic flow of the algorithm once it stabilizes, i.e., once all $n-f$ non-faulty nodes are well-synchronized. Recall that the remaining up to $f < n/3$ faulty nodes may produce arbitrary signals on their outgoing channels. A pulse is locally triggered by switching to state accept. Thus, assume that at some time all non-faulty nodes switch to state accept within a time window of $2d$, i.e., a pulses are generated by non-faulty nodes within a time interval of size $2d$. Supposing that $T_3 \geq 3\delta d$, these nodes will observe, and thus memorize, each other and themselves in state accept within a time interval of size $3\delta d$ and thus before $T_3$ expires at any non-faulty node. This makes timeout $T_3$ the critical condition for switching to state sleep. From state sleep, they will switch to states sleep → waking, waking, and finally ready, where the timeout $(T_3, \text{accept})$ is determining the time this takes, as it is considerably larger than $\delta (2\delta + 2)T_3$. The intermediate states serve the purpose of achieving stabilization, hence we leave them out for the moment.

Note that upon switching to state ready, nodes reset their propose flags and NEXT. Thus, they essentially ignore these signals between the most recent time they switched to propose before switching to accept and the subsequent time when they switch to ready. Since nodes already reset their accept flags upon switching to waking, this ensures that nodes do not take into account outdated information for the decision when to switch to state propose.

Hence, it is guaranteed that the first node switching from state ready to state propose again does so because $T_3$ expired or because $T_3$ expired and its NEXT memory flag is true. The constraint $\min\{T_3, T_4\} \geq \delta (T_2 + 4d)$ ensures that all non-faulty nodes observe themselves in state ready before the first one switches to propose. Hence, no node deletes information about nodes that switch to propose again after the previous pulse.

The first non-faulty node that switches to state accept again cannot do so before it memorizes at least $n-f$ nodes in state propose, as the accept flags have been reset upon switching to state waking. Therefore, at this time at least $n-2f \geq f+1$ non-faulty nodes are in state propose. Hence, the rule that nodes switch to propose if they memorize $f+1$ nodes in states propose will take effect, i.e., the remaining non-faulty nodes in state ready switch to propose after less than $d$ time. Another $d$ time later all non-faulty nodes in state propose will have become aware of this and switch to state accept as well, as the threshold of $n-f$ nodes in states propose or accept is reached. Thus the cycle is complete and the reasoning can be repeated inductively.

Clearly, for this line of argumentation to be valid, the algorithm could be simpler than stated in Figure 1. We already mentioned that the motivation of having three in-
termediate states between accept and ready is to facilitate stabilization. Similarly, there is no need to make use of the accept flags in the basic cycle at all; in fact, it adversely affects the constraints the timeouts need to satisfy for the above reasoning to be valid. However, the accept flags are much better suited for diagnostic purposes than the propose flags, since nodes are expected to switch to accept in a small time window and remain in state accept for a small period of time only (for all our results, it is sufficient if \( T_1 = 4\vartheta d \)). Moreover, two different timeout conditions for switching from ready to propose are unnecessary for correct operation of the pulse synchronization routine. As discussed before, they are introduced in order to allow for a seamless coupling to the application layer.

B. Main Algorithm

We proceed by describing the main routine of the pulse algorithm in full. Alongside the main routine, several other state machines run concurrently and provide additional information to be used during recovery, as we detail later.

The main routine is graphically presented in Figure 2. Except for the states recover and join and additional resets of memory flags, the main routine is identical to the basic cycle. The purpose of the two additional states is the following: Nodes switch to state recover once they detect that something is wrong, that is, non-faulty nodes do not execute the basic cycle as outlined in Section III-A. This way, non-faulty nodes will not continue to confuse others by sending for example state signals propose or accept despite clearly being out-of-sync. There are various consistency checks that nodes perform during each execution of the basic cycle. The first one is that in order to switch from state accept to state sleep, non-faulty nodes need to memorize at least \( n - f \) nodes in state accept. If this does not happen within \( 4d \leq T_1 / \vartheta \) time after switching to state accept, by the arguments given in Section III-A the nodes could not have entered state accept within \( 2d \) of each other. Therefore, something must be wrong and it is feasible to switch to state recover. Next, whenever a non-faulty node is in state waking, there should be no non-faulty nodes in states accept or recover. Considering that the node resets its accept and recover flags upon switching to waking, it should not memorize \( f + 1 \) or more nodes in states accept or recover at a time when it observes itself in state waking. If it does, however, it again switches to state recover.

Last but not least, during a synchronized execution of the basic cycle, no non-faulty node may be in state propose for more than a certain amount of time before switching to state accept. Therefore, nodes will switch from propose to recover when timeout \( T_b \) expires.

![Figure 1. Basic cycle of node i once the algorithm has stabilized.](image)
Figure 2. Overview of the core routine of node $i$’s self-stabilizing pulse algorithm.

On the other hand, it is crucial that this happens in a sufficiently well-synchronized manner, as otherwise nodes could drop out of the basic cycle again because the various checks of consistency detect an erroneous execution of the basic cycle.

In part, this issue is solved by an additional agreement step. In order to enter the basic cycle again, nodes need to memorize $n - f$ nodes in states $join$ (the respective nodes detected an inconsistency), $propose$ (these nodes continued to execute the basic cycle), or $accept$ (there are executions where nodes reset their $propose$ flags because of switching to $join$ when other nodes already switched to $accept$). The threshold conditions of $f + 1$ nodes memorized in state $join$ or $f + 1$ nodes memorized in state $propose$ for leaving state $recover$, all nodes will follow the first one switching from $join$ to $propose$ quickly, just as with the switch from $propose$ to $accept$ in an ordinary execution of the basic cycle. However, it is decisive that all nodes are in states that permit to participate in this agreement step in order to guarantee success of this approach.

As a result, still a certain degree of synchronization needs to be established beforehand both among nodes that still execute the basic cycle and those that do not. For instance, if at the point in time when a majority of nodes and channels become non-faulty, some nodes already memorize nodes in $join$ that are not, they may switch to state $join$ and subsequently $propose$ prematurely, causing others to have inconsistent memory flags as well. Byzantine faults may sustain such amiss configuration of the system indefinitely.

So why did we put so much effort in “shifting” the focus to this part of the algorithm? The key advantage is that nodes outside the basic cycle may take into account less reliable information for stabilization purposes. They may take the risk of metastable upsets (as we know it is impossible to avoid these during the stabilization process, anyway) and make use of randomization.

In fact, to make the above scheme work, it is sufficient that all non-faulty nodes agree on a so-called resynchronization point (cf. Definitions 3.1 and 3.2), that is, a point in time at which nodes reset the memory flags for states $join$ and $sleep \rightarrow waking$ as well as certain timeouts, while guaranteeing that no node is in these states close to the respective reset times. Except for state $sleep \rightarrow waking$, all of these timeouts, memory flags, etc. are not part of the basic cycle at all, thus nodes may enforce consistent values for them easily when agreeing on such a resynchronization point.

Conveniently, the use of randomization also ensures that
it is quite unlikely that nodes are in state $sleep \rightarrow waking$ close to a resynchronization point, as the consistency check of having to memorize $n - f$ nodes in state $accept$ in order to switch to state $sleep$ guarantees that the time windows during which non-faulty nodes may switch to $sleep$ make up a small fraction of all times only.

Consequently, the remaining components of the algorithm deal with agreeing on resynchronization points and utilizing this information in an appropriate way to ensure stabilization of the main routine. We describe this connection to the main routine first. It is done by another, quite simple state machine, which runs in parallel alongside the core routine. It is depicted in Figure 3.

Its purpose is to reset memory flags in a consistent way and to determine when a node is permitted to switch to $join$. In general, a resynchronization point (locally observed by switching to state $resync$, which is introduced later) triggers the reset of the $join$ and $sleep \rightarrow waking$ flags. If there are still nodes executing the basic cycle, a node may become aware of it by observing $f + 1$ nodes in state $sleep \rightarrow waking$ at some time. In this case it switches from the state $passive$, which it entered at the point in time when it locally observed the resynchronization point, to the state $active$. Subsequently, once timeout $T_{R}$ expires, the node will switch to state, in which it is more susceptible to switching to state $join$. This is expressed by the rather involved transition rule $tr'(recover, join)$ (in Figure 2). $T_{R}$ is much smaller than $T_{7}$, but $T_{R}$ is of no concern until the node switches to state $active$ and resets $T_{R}$. The condition that $Mem_{i,s,join} = 0$ simply means that nodes should not already have attempted to stabilize by switching to $join$ since the most recent transition to $passive$. This avoids interfering too much with the second stabilization mechanism (switching from $recover$ to $accept$), as it might take significantly longer than the time required for this “immediate” recovery to stabilize by means of agreeing on a resynchronization point.

It remains to explain how resynchronization points are generated.

C. Resynchronization Algorithm

The resynchronization routine is specified in Figure 4. Similarly to the extension of the core routine, it is a lower layer that the core routine uses for stabilization purposes only. It provides some synchronization that is akin to that of a pulse, except that such “weak pulses” occur at random times, and may be generated inconsistently even after the algorithm as a whole has stabilized. Since the main routine operates independently of the resynchronization routine once the system has stabilized, we can afford the weaker guarantees of the routine: If it succeeds in generating a “good” resynchronization point merely once, the main routine will stabilize deterministically.

Definition 3.1 (Resynchronization Points): Given $W \subseteq V$, time $t$ is a $W$-resynchronization point iff each node in $W$ switches to state $supp \rightarrow resync$ in the time interval $(t, t + 2d)$.

Definition 3.2 (Good Resynchronization Points): A $W$-resynchronization point is called good iff no node from $W$ switches to state $sleep$ during $(t - \Delta_{g}, t)$, where $\Delta_{g} := \langle 2d + 3 \rangle T_{1}$, and no node is in state $join$ during $t - T_{1} - d, t + 4d$.

In order to clarify that despite having a linear number of states ($supp_{1}, \ldots, supp_{n}$), this part of the algorithm can be implemented using 2-bit communication channels between state machines only, we generalize our description of state machines as follows. If a state is depicted as a circle separated into an upper and a lower part, the upper part denotes the local state, while the lower part indicates the signal state to which it is mapped. A node’s memory flags then store the respective signal states only, i.e., remote nodes do not distinguish between states that share the same signal. Clearly, such a machine can be simulated by a machine as introduced in the model section. The advantage is that such a mapping can be used to reduce the number of transmitted state bits; for the resynchronization routine given in Figure 4 we merely need two bits (init/wait and none/supp) instead of $\lceil \log(n + 3) \rceil + 1$ bits.

The basic idea behind the resynchronization algorithm is the following: Every now and then, nodes will try to initiate agreement on a resynchronization point. This is the purpose of the small state machine on the left in Figure 4. Recalling that the transition condition “true” simply means that the node switches to state $wait$ again as soon as it observes itself in state $init$, it is easy to see that it does nothing else than creating an $init$ signal as soon as $R_{3}$ expires and resetting $R_{3}$ again as quickly as possible. As the time when a node switches to $init$ is determined by the randomized timeout $R_{3}$ distributed over a large interval (cf. Equality [11]) only,
resync

none

wait

true

init

supp

\[ (R_1, \text{supp} \rightarrow \text{resync}) \]

\[ 2\vartheta d \]

\[ \geq n - f \text{ supp} \]

\[ 4\vartheta d \]

\[ \ast (S_{i,j} = \text{init and } (R_2, \text{supp } j)) \]

\[ \ast (S_{i,k} = \text{init and } (R_2, \text{supp } k)) \]

\[ \vartheta d \]

\[ \geq n - f \text{ supp} \]

\[ \text{supp } j \]

\[ \text{supp } \]

\[ \geq n - f \text{ supp} \]

\[ \text{resync} \]

\[ \text{none} \]

Figure 4. Resynchronization algorithm, comprising two state machines executed in parallel at node i.

therefore it is impossible to predict when it will expire, even with full knowledge of the execution up to the current point in time. Note that the complete independence of this part of node i’s state from the remaining protocol implies that faulty nodes are not able to influence the respective times by any means.

Consider now the state machine displayed on the right of Figure 4. To illustrate how the routine is intended to work, assume that at the time t when a non-faulty node i switches to state init, all non-faulty nodes are not in any of the states supp, resync, or supp i, and at all non-faulty nodes the timeout \((R_2, \text{supp } i)\) has expired. Then, no matter what the signals from faulty nodes or on faulty channels are, each non-faulty node will be in one of the states supp, \(j, j \in V\), or supp \(\rightarrow\) resync at time \(t + d\). Hence, they will observe each other (and themselves) in one of these states at some time smaller than \(t + 2d\). These statements follow from the various timeout conditions of at least \(2\vartheta d\) and the fact that observing node i in state init will make nodes switch to state supp i if in none or supp \(j, j \neq i\). Hence, all of them will switch to state supp \(\rightarrow\) resync during \((t, t + 2d)\), i.e., \(t\) is a resynchronization point. Since \(t\) follows a random distribution that is independent of the remaining algorithm and, as mentioned earlier, most of the times nodes do not switch to state sleep and it is easy to deal with the condition on join states, there is a large probability that \(t\) is a good resynchronization point. Note that timeout \(R_1\) makes sure that no non-faulty node will switch to supp \(\rightarrow\) resync again anytime soon, leaving sufficient time for the main routine to stabilize.

The scenario we just described relies on the fact that at time \(t\) no node is in state supp \(\rightarrow\) resync or state resync. We will choose \(R_2 \gg R_1\), implying that \(R_2 + 3d\) time after a node switched to state init all nodes have “forgotten” about this, i.e., \((R_2, \text{supp } i)\) is expired and they switched back to state none (unless other init signals interfered). Thus, in the absence of Byzantine faults, the above requirement is easily achieved with a large probability by choosing \(R_3\) as a uniform distribution over some interval \([R_2 + 3d, R_2 + \Theta(nR_1)]\); Other nodes will switch to init \(O(n)\) times during this interval, each time “blocking” other nodes for at most \(O(R_1)\) time. If the random choice picks any other point in time during this interval, a resynchronization point occurs. Even if the clock speed of the clock driving \(R_3\) is manipulated in a worst-case manner (affecting the density of the probability distribution with respect to real time by a factor of at most \(\vartheta\)), we can just increase the size of the interval to account for this.

However, what happens if only some of the nodes receive an init signal due to faulty channels or nodes? If the same holds for some of the subsequent supp signals, it might happen that only a fraction of the nodes reaches the threshold for switching to state supp \(\rightarrow\) resync, resulting in an inconsistent reset of flags and timeouts across the system.
Until the respective nodes switch to state \textit{none} again, they will not support a resynchronization point again, i.e., about \( R_1 \) time is “lost”. This issue is the reason for the agreement step and the timeouts \((R_2, \text{supp } j)\). In order for any node to switch to state \textit{supp} \rightarrow \textit{resync}, there must be at least \( n-2f \geq f+1 \) non-faulty nodes supporting this. Hence, all of these nodes recently switched to a state \textit{supp} \( j \) for some \( j \in V \), resetting \((R_2, \text{supp } j)\). Until these timeouts expire, \( f+1 \in \Omega(n) \) non-faulty nodes will ignore \textit{init} signals on the respective channels. Since there are \( \mathcal{O}(n^2) \) channels, it is possible to choose \( R_2 \in \mathcal{O}(nR_3) \) such that this may happen at most \( \mathcal{O}(n) \) times in \( \mathcal{O}(n) \) time. Playing with constants, we can pick \( R_3 \in \Omega(n) \) maintaining that still a constant fraction of the times are “good” in the sense that \( R_3 \) expiring at a non-faulty node will result in a good resynchronization point.

**D. Timeout Constraints**

**Condition 3.3** summarizes the constraints we require on the timeouts for the core routine and the resynchronization algorithm to act and interact as intended.

**Condition 3.3 (Timeout Constraints):** Recall that \( \vartheta > 1 \) and \( \Delta_g := (2\vartheta + 3)T_1 \). Define

\[
\lambda := \sqrt{\frac{25\vartheta - 9}{25\vartheta}} \in \left[\frac{4}{5}, 1\right].
\]

The timeouts need to satisfy the constraints

\[
\begin{align*}
T_1 &\geq 4\vartheta d \\
T_2 &\geq 3\vartheta \Delta_g + 7\vartheta d \\
T_3 &\geq (2\vartheta^2 + 4\vartheta)T_1 + 9\vartheta d \\
T_4 &\geq (\vartheta - 1)T_2 + 6\vartheta d \\
T_5 &\geq \max\{ (\vartheta - 1)T_2 - T_3 + \vartheta T_4 + 7\vartheta d, \\
&\quad (\vartheta - 1)T_1 + \vartheta (T_2 + T_3) - T_6 \} \\
T_6 &\geq \vartheta T_2 - 2\vartheta T_1 - 2\vartheta d \\
T_7 &\geq (2\vartheta^2 + 3\vartheta - 1)T_1 + 7\vartheta d \\
T_8 &\geq (2\vartheta^2 + 3\vartheta - 2)T_1 + \vartheta (T_2 + T_4 + T_5) + T_6 \\
R_1 &\geq \max\{ \vartheta T_7 + (4\vartheta^2 + 8\vartheta)d, \\
&\quad \vartheta (2T_2 + 2T_3 + 7d) - 2T_1 \} \\
R_2 &\geq \frac{2\vartheta (R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d)(n - f)}{1 - \lambda} \\
R_3 &= \text{uniformly distributed random variable on} \\
&\quad [\vartheta (R_2 + 3d), \vartheta (R_2 + 3d) + 8(1 - \lambda)R_2] \\
\lambda &\leq \frac{T_2 - 2\vartheta \Delta_g - (\vartheta - 1)T_1 - 4\vartheta d}{T_2 - (\vartheta - 1)T_1 - \vartheta d}.
\end{align*}
\]

We need to show that this system can always be solved. Furthermore, we would like to allow to couple the pulse generation algorithm to an application algorithm with any possible drift. To this end, we would like to be able to make the ratio \( (T_2 + T_4)/(\vartheta(T_2 + T_3 + 4d)) \) arbitrarily large: Thereby, \((T_2 + T_4)\) is the minimal gap between successive pulses generated at each node, provided that the states of all the \textit{NEXT} signals are constantly zero, and \( \vartheta(T_2 + T_3 + 4d) \) is the maximal time it takes nodes to observe themselves in state \textit{ready} with \( T_3 \) expired after the last generated pulse (as then they will respond to \textit{NEXT}i switching to one).

**Lemma 3.4:** For any \( d, \vartheta \in \mathcal{O}(1) \), \textbf{Condition 3.3} can be satisfied with \( T_1, \ldots, T_7, R_1, R_2 \in \mathcal{O}(1) \) and \( R_2 \in \mathcal{O}(n) \), where

\[
\alpha := \frac{(T_2 + T_4)/\vartheta}{T_2 + T_3 + 4d}
\]

may be chosen to be an arbitrarily large constant.

**Proof:** First, observe that if \textbf{inequality (3)} holds, the denominator in the right hand side of \textbf{inequality (12)} is positive. Thus, we can equivalently state \textbf{inequality (12)} as

\[
T_2 \geq \frac{2\vartheta \Delta_g + (1 - \lambda)(\vartheta - 1)T_1 + (4 - \lambda)d}{1 - \lambda}.
\]

Since \( \lambda \in (4/5, 1) \), this inequality clearly imposes a stronger constraint than \textbf{inequality (5)}; hence we can replace Inequalities \textbf{(3)} and \textbf{(12)} with this one and obtain an equivalent system. The requirement of \((T_2 + T_4)/(\vartheta(T_2 + T_3 + 4d)) = \alpha \) can be rephrased as

\[
T_4 \geq (\alpha \vartheta - 1)T_2 + \alpha \vartheta (T_3 + 4d).
\]

Again, clearly this constraint is stronger than \textbf{inequality (5)}; hence we drop \textbf{inequality (5)} in favor of \textbf{inequality (14)}.

We satisfy the inequalities by iteratively defining the values of the left hand sides in accordance with the respective constraint, in the order \textbf{(2), (13), (7), (4), (14), (6), (8), (9)}, and finally \textbf{(10)}. Note that this is feasible, as in any step the right hand side of the current inequality is an expression in \( d, \vartheta, \alpha \), and, in case of \textbf{inequality (10)} \( n - f \).

\footnote{For simplicity, we refrain from demanding equality and drop terms in order to get more condensed expressions. For \( \vartheta \leq 1.2 \), for example, the increase in the bounds is not significant.}
the solution
\[
T_1 := 4\vartheta d
\]
\[
T_2 := \frac{46\vartheta^3 d}{1 - \lambda}
\]
\[
T_6 := \frac{46\vartheta^4 d}{1 - \lambda}
\]
\[
T_3 := \frac{(\vartheta^2 - 1)46\vartheta^3 d}{1 - \lambda} + 31\vartheta^3 d
\]
\[
T_4 := \frac{46\vartheta^4(\alpha\vartheta^3 - 1)d}{1 - \lambda} + 35\alpha\vartheta^4 d
\]
\[
T_5 := \frac{46\vartheta^4(\alpha\vartheta^3 - 1)d}{1 - \lambda} + 39\alpha\vartheta^5 d
\]
\[
T_7 := \frac{92\alpha\vartheta^6 d + 78\alpha\vartheta^5 d}{1 - \lambda}
\]
\[
R_1 := \frac{46\vartheta^6(3\alpha\vartheta^3 - 1)d}{1 - \lambda} + 109\alpha\vartheta^6 d
\]
\[
R_2 := \frac{(92\vartheta^7(3\alpha\vartheta^3 - 1)(n - f)d}{(1 - \lambda)^2}
\]
\[+ \frac{(218\alpha\vartheta^7 + 108\alpha^2)(n - f)d}{1 - \lambda}.
\]
As $\alpha \in O(1)$ was arbitrary, $d$ and $\vartheta$ are constants, and $\lambda \in (4/5,1)$ depends on $\vartheta$ only and is thus a constant as well, these values satisfy the asymptotic bounds stated in the lemma, concluding the proof.

IV. ANALYSIS

In this section we derive skew bounds $\Sigma$, as well as accuracy bounds $T^-, T^+$, such that the presented protocol is a $(W,E)$-stabilizing pulse synchronization protocol, for proper choices of the set of nodes $W$ and the set of channels $E$, with skew $\Sigma$ and accuracy bounds $T^-, T^+$ that stabilizes within time $T(k) \in O(kn)$ with probability $1 - 2^{-k(n-f)}$, for any $k \in \mathbb{N}$. This analysis follows the lines of [20], with minor adjustments due to the changes made to the FATAL protocol. Moreover, we show that if a set of at least $n - f$ nodes fires pulses regularly, then other non-faulty nodes synchronize within $O(R_1)$ time deterministically. This stabilization mechanism is much simpler; the main challenge here is to avoid interference with the other approach.

A. Basic Statements

To start our analysis, we need to define the basic requirements for stabilization. Essentially, we need that a majority of nodes is non-faulty and the channels between them are correct. However, the first part of the stabilization process is simply that nodes “forget” about past events that are captured by their timeouts. Therefore, we demand that these nodes indeed have been non-faulty for a time period that is sufficiently large to ensure that all timeouts have been reset at least once after the considered set of nodes became non-faulty.

Definition 4.1 (Coherent Nodes): A subset of nodes $W \subseteq V$ is called coherent during the time interval $[t^-, t^+]$, iff during $[t^- - (\vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2 + d, t^+]$ all nodes $i \in W$ are non-faulty, and all channels $S_{i,j}$, $i,j \in W$, are correct.

We will show that if a coherent set of at least $n - f$ nodes fires a pulse, i.e., switches to accept in a tight synchrony, this set will generate pulses deterministically and with controlled frequency, as long the set remains coherent. This motivates the following definitions.

Definition 4.2 (Stabilization Points): We call time $t$ a $W$-stabilization point (quasi-stabilization point) iff all nodes $i \in W$ switch to accept during $[t, t + 2d]$ ($[t, t + 3d]$).

Throughout this section, we assume the set of coherent nodes $W$ with $|W| \geq n - f$ to be fixed and consider all nodes in and channels originating from $V \setminus W$ as (potentially) faulty. As all our statements refer to nodes in $W$, we will typically omit the word “non-faulty” when referring to the behavior or states of nodes in $W$, and “all nodes” is short for “all nodes in $W$”. Note, however, that we will still clearly distinguish between channels originating at faulty and non-faulty nodes, respectively, to nodes in $W$.

As a first step, we observe that at times when $W$ is coherent, indeed all nodes reset their timeouts, basing the respective state transition on proper perception of nodes in $W$.

Lemma 4.3: If $W$ is coherent during the time interval $[t^-, t^+]$, with $t^- \geq \vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2 + d$, any (randomized) timeout $(T, s)$ of any node $i \in W$ expiring at a time $t \in [t^-, t^+]$ has been reset at least once since time $t^- - (\vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2)$.

Proof: According to [Condition 3.3], the largest possible value of any (randomized) timeout is $\vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2$. Hence, any timeout that is in state 1 at a time smaller than $t^- - (\vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2) \geq 0$ expires before time $t^-$ or is reset at least once. As by the definition of coherency all nodes in $W$ are non-faulty and all channels between such nodes are correct during $[t^- - (\vartheta(R_2 + 3d) + 8(1 - \lambda)\vartheta^2), t^+]$, this implies the statement of the lemma.

Phrased informally, any corruption of timeout and channel states eventually ceases, as correct timeouts expire and correct links remember no events that lie $d$ or more time in the past. Proper clearing of the memory flags is more complicated and will be explained further down the road.

Throughout this section, we will assume for the sake of simplicity that the set $W$ is coherent at all times and use this lemma implicitly, e.g. we will always assume that nodes from $W$ will observe all other nodes from $W$ in states that they indeed had less than $d$ time ago, expiring of randomized timeouts at non-faulty nodes cannot be predicted accurately, etc. We will discuss more general settings in Section V.
We proceed by showing that once all nodes in $W$ switch to accept in a short period of time, i.e., a $W$-quasi-stabilization point is reached, the algorithm guarantees that synchronized pulses are generated deterministically with a frequency that is bounded both from above and below.

Theorem 4.4: Suppose $t$ is a $W$-quasi-stabilization point. Then

(i) all nodes in $W$ switch to accept exactly once within $[t, t + 3d)$, and do not leave accept until $t + 4d$; and

(ii) there will be a $W$-stabilization point $t' \in (t + (T_2 + T_3)/\vartheta, t + T_2 + T_4 + 5d)$ satisfying that no node in $W$ switches to accept in the time interval $[t + 3d, t')$, and that

(iii) each node $i$’s, $i \in W$, core state machine [Figure 1] is metastability-free during $[t + 3d, t' + 3d]$.

Proof. Proof of (i): Due to Inequality (2), a node does not leave the state accept earlier than $T_1/\vartheta \geq 4d$ time after switching to it. Thus, no node can switch to accept twice during $[t, t + 3d]$. By definition of a quasi-stabilization point, every node does switch to accept in the interval $[t, t + 3d) \subset [t, t + T_1/\vartheta]$. This proves Statement (i).

Proof of (ii): For each $i \in W$, let $t_i \in [t, t + 3d)$ be the time when $i$ switches to accept. By (i) $t_i$ is well-defined. Further let $t'_i$ be the infimum of times in $(t_i, \infty)$ when $i$ switches to recover or propose. In the following, denote by $i \in W$ a node with minimal $t'_i$.

We will show that all nodes switch to propose via states sleep, sleep $\rightarrow$ waking, waking, and ready in the presented order. By (i) nodes do not leave accept before $t + 4d$. Thus at time $t + 4d$, each node in $W$ is in state accept and observes each other node in $W$ in accept. Hence, each node in $W$ memorizes each other node in $W$ in accept at time $t + 4d$. For each node $j \in W$, let $t_j$ be the time node $j$’s timeout $T_j$ expires first after $t_j$. Then $t_j \in (t_j + T_1/\vartheta, t_j + T_1 + d)$. Since $|W| \geq n - f$, each node $j$ switches to sleep at time $t_j$. Hence, by time $t + T_1 + 4d$, no node will be observed in state accept anymore (until the time when it switches to accept again).

When a node $j \in W$ switches to state waking at the minimal time $t_w$ larger than $t_j$, it does not do so earlier than at time $t + T_1/\vartheta + (2 + 1/\vartheta)T_1 = t + (2 + 2/\vartheta)T_1 > t + T_1 + 4d$. This implies that all nodes in $W$ have already left accept at least $d$ time ago, since they switched to it at their respective times $t_j < t + T_1 + 3d$. Moreover, they cannot switch to accept again until $t'_i$ as it is minimal and nodes need to switch to propose or recover before switching to accept. Hence, nodes in $W$ are not observed in state accept during $(t + T_1 + 4d, t'_i)$, in particular not by node $j$. Furthermore, nodes in $W$ are not observed in state recover during $(t_w - d, t'_i)$. As it resets its accept and recover flags upon switching to waking, $j$ will hence neither switch from waking to recover nor from ready to propose during $(t_w, t'_i)$.

Now consider node $i$. By the previous observation, it will not switch from waking to recover, but to ready, following the basic cycle. Consequently, it must wait for timeout $T_2$ to expire, i.e., cannot switch to ready earlier than at time $t + T_2/\vartheta$. By definition of $t'_i$, node $i$ thus switches to propose at time $t'_i$. As it is the first node that does so, this cannot happen before timeouts $T_3$ or $T_4$ expire, i.e., before time

$$t + \frac{T_2}{\vartheta} + \frac{\min\{T_3, T_4\}}{\vartheta} \geq t + T_2 + T_3  \geq t + T_2 + T_4 + 5d. \quad (15)$$

All other nodes in $W$ will switch to waking, and for the first time after $t_j$, observe themselves in state waking at a time within $(t + T_1 + 4d, t + T_1(2 + \vartheta) + 7d)$. Recall that unless they memorize at least $f + 1$ nodes in accept or recover while being in state waking, they will all switch to state ready by time

$$\max\{t + T_2 + 4d, t + (2\vartheta + 2)T_1 + 7d\} \geq t + T_2 + 4d. \quad (16)$$

As we just showed that $t'_i > t + T_2 + 5d$, this implies that at time $t + T_2 + 5d$ all nodes are observed in state ready, and none of them leaves before time $t'_i$.

Now choose $t'$ to be the infimum of times from $(t + (T_2 + T_3)/\vartheta, t + T_2 + T_4 + 4d)$ when a node in $W$ switches to state accept. Because of Inequality (15), node $j$ cannot switch to propose within $[t_j, t + (T_2 + T_3)/\vartheta)$. Thus, (after time $t + 3d$) node $j$ does not switch to accept again earlier than time $t'$, and timeout $T_5$ cannot expire at $j$ until time

$$t + \frac{T_2 + T_3 + T_5}{\vartheta} \geq t + T_2 + T_4 + 7d \geq t' + 3d, \quad (17)$$

making it impossible for $j$ to switch from propose to recover at a time within $[t_j, t' + 3d]$. What is more, a node from $W$ that switches to accept must stay there for at least $T_1/\vartheta > 3d$ time. Thus, by definition of $t'$, no node $j \in W$ can switch from accept to recover at a time within $[t_j, t' + 3d]$. Hence, no node $j \in W$ can switch to state recover after $t_j$, but earlier than time $t' + 2d$. It follows that no node in $W$ can switch to other states than propose or accept during $[t + T_2 + 4d, t' + 2d]$. In particular, no node in $W$ resets its propose flags during $(t + T_2 + 4d, t' + 2d)$. Moreover, there cannot be any node in $W$ that switches to state accept $n - 2f \geq f + 1$ of its propose flags corresponding to nodes in $W$ are true, i.e., all correspond to a flag holding 1. As the node resets its propose flags at the most recent time when it switched to ready and no nodes in $W$ have been observed in propose between this time and $t'_i$, it holds that $f + 1$ nodes in $W$ switched to state propose during $[t'_i, t')$. Since we established that no node resets its propose flags during $[t'_i, t' + 2d]$, it follows that all nodes are in state propose by time $t' + d$.

Footnotes:

16. Note that we follow the convention that $\inf \emptyset = \infty$ if the infimum is taken with respect to a (from above) unbounded subset of $\mathbb{R}_0^+$.  
17. The upper bound comprises an additive term of $d$ since $T_1$ is reset at some time from $(t_j, t_j + d)$.  
18. Note that since we take the infimum on $(t + (T_2 + T_3)/\vartheta, t + T_2 + T_4 + 4d)$, we have that $t' \leq t + T_2 + T_4 + 4d$. 

Consequently, all nodes in \( W \) will observe all nodes in \( W \) in state \( \text{propose} \) before time \( t' + 2d \) and switch to \( \text{accept} \), i.e., \( t' \in (t + (T_2 + T_3))/\vartheta, t + T_2 + T_4 + 4d \) is a \( W \)-stabilization point. Statement (ii) follows.

On the other hand, if at time \( t' \) no node in \( W \) switches to state \( \text{accept} \), it follows that \( t' = t + T_2 + T_4 + 4d \). As all nodes observe themselves in state \( \text{ready} \) by time \( t + T_2 + 5d \), they switch to \( \text{propose} \) before time \( t + T_2 + T_4 + 5d = t' + d \) because \( T_4 \) expired. By the same reasoning as in the previous case, they switch to \( \text{accept} \) before time \( t' + 2d \), i.e., Statement (ii) holds as well.

Proof of (iii): We have shown that within \( [t_j, t_j' + 3d] \), any node \( j \) in \( W \) switches to states along the basic cycle only. Note that Condition (ii) in the definition of metastability-freedom is satisfied by definition for state transitions along the basic cycle, as the conditions involve memory flags and timeouts (that are not associated with the states the nodes switch to) only. To show the correctness of Statement (iii), it is thus sufficient to prove that, whenever \( j \) switches from state \( s \) of the basic cycle to \( s' \) of the basic cycle during time \( [t_j, t_j' + 3d] \), the transition from \( s \) to \( \text{recover} \) is disabled from the time it switches to \( s' \) until it observes itself in this state. We consider transitions \( tr(\text{accept}, \text{recover}), tr(\text{waking}, \text{recover}) \), and \( tr(\text{propose}, \text{recover}) \) one after the other:

1) \( tr(\text{accept}, \text{recover}) \): We showed that node \( j \)'s condition \( tr(\text{accept}, \text{sleep}) \) is satisfied before time \( t + 4d \leq t + T_1/\vartheta \), i.e., before \( tr(\text{accept}, \text{recover}) \) can hold, and no node resets its \text{accept} flags less than \( d \) time after switching to state \text{sleep}. When \( j \) switches to state \text{accept} again at or after time \( t' \), \( T_1 \) will not expire earlier than time \( t' + 4d \).

2) \( tr(\text{waking}, \text{recover}) \): As part of the reasoning about Statement (ii), we derived that \( tr(\text{waking}, \text{recover}) \) does not hold at nodes from \( W \) observing themselves in state \text{waking}.

3) \( tr(\text{propose}, \text{recover}) \): The additional slack of \( d \) in Inequality (17) ensures that \( T_5 \) does not expire at any node in \( W \) switching to state \text{accept} during \( (t', t' + 2d) \) earlier than \( t' + 3d \).

Since \( [t_j, t_j' + 3d] \supset [t + 3d, t' + 3d] \), Statement (iii) follows.

Inductive application of Theorem 4.4 shows that by construction of our algorithm, nodes in \( W \) provably do not suffer from metastability upsets once a \( W \)-quasi-stabilization point is reached, as long as all nodes in \( W \) remain non-fauly and the channels connecting them correct. Unfortunately, it can be shown that it is impossible to ensure this property during the stabilization period, thus rendering a formal treatment infeasible. This is not a peculiarity of our system model, but a threat to any model that allows for the possibility of metastable upsets as encountered in physical chip designs. However, it was shown that, by proper chip design, the probability of metastable upsets can be made arbitrarily small. In the remainder of this work, we will therefore assume that all non-faulty nodes are metastability-free in all executions.

The next lemma reveals a very basic property of the main algorithm that is satisfied if no nodes may switch to state \text{join} in a given period of time. It states that if a non-faulty node switches to state \text{sleep}, other non-faulty nodes cannot remain too far ahead or behind in their execution of the basic cycle.

Lemma 4.5: Assume that at time \( t_{\text{sleep}} \), some node from \( W \) switches to state \text{sleep} and no node from \( W \) is in state \text{join} during \( [t_{\text{sleep}} - T_1 - d, t_{\text{sleep}} + 2T_1 + 3d] \). Then

1) at time \( t_{\text{sleep}} + 2T_1 + 3d \), any node is in one of the states \text{sleep}, \text{sleep} \rightarrow \text{waking}, \text{waking}, or \text{recover};
2) any node in states \text{sleep}, \text{sleep} \rightarrow \text{waking}, or \text{waking} reset its timeout \( T_2 \) at some time from \( (t_{\text{sleep}} - \Delta_g - 4d, t_{\text{sleep}} + (2 - 1/\vartheta)T_1 + 3d) \); and
3) no node switches from \text{recover} to \text{accept} during \( [t_{\text{sleep}} + T_1 + 2d, t_a] \), where \( t_a > t_{\text{sleep}} + 2T_1 + 3d \) denotes the infimum of times larger than \( t_{\text{sleep}} + T_1 + 2d \) when a node switches to state \text{accept}.

Proof: We claim that there is a subset \( A \subseteq \{W \) of at least \( n - 2f \) nodes such that each node from \( A \) has been in state \text{accept} at some time in the interval \( (t_{\text{sleep}} - T_1 - d, t_{\text{sleep}}) \). To see this, observe that if a node switches to state \text{sleep} at time \( t_{\text{sleep}} \), it must have observed \( n - 2f \) non-faulty nodes in state \text{accept} at times from \( (t_{\text{sleep}} - T_1, t_{\text{sleep}}) \), since it resets its \text{accept} flags at the time \( t_a \geq t_{\text{sleep}} - T_1 \) (that is minimal with this property) when it switched to state \text{accept}. Each of these nodes must have been in state \text{accept} at some time from \( (t_{\text{sleep}} - T_1 - d, t_{\text{sleep}}) \), showing the existence of a set \( A \subseteq \{W \) as claimed.

During

\[
\begin{align*}
\left[ t_{\text{sleep}} + T_1 + 2d, t_{\text{sleep}} - T_1 - d + \min \left\{ \frac{\vartheta(2T_1 + 3d)}{\vartheta}, T_2 \right\} \right]
\end{align*}
\]

\[
\left[ t_{\text{sleep}} + T_1 + 2d, t_{\text{sleep}} + T_1 + 2d \right]
\]

no node from \( A \) is observed in state \text{accept}, as following the basic cycle requires \( T_2 \) to expire, no node switches to \text{join}, and in order to switch directly from \text{recover} to \text{accept}, a timeout of \( \vartheta(2T_1 + 3d) \) needs to expire first. Since this also applies to the nodes from \( A \) and no node is in state \text{join} until

Note that it is feasible to incorporate this issue into the model by means of the probability space, as it is beyond control of “reasonable” adversaries to control signals on faulty channels (or ones that originate at non-faulty nodes) precisely enough to ensure more than a small probability of a metastable upsets. However, since it is (at best) impractical to consider metastable states of the system in our theoretical framework, essentially this approach boils down to counting the number of state transitions during stabilization where a non-faulty node is in danger of becoming metastable and control this risk by means of the union bound.
time $t_{\text{sleep}} + 2T_1 + 3d$, the only way to do so is by following the basic cycle via states $\text{sleep}$, $\text{sleep} \rightarrow \text{waking}$, $\text{waking}$, ready, and propose. However, this takes at least until time $t_{\text{sleep}} + \frac{T_2}{\vartheta} \geq t_{\text{sleep}} + 2T_1 + 3d$

as well. This shows Statement (iii) of the lemma.

Now consider any node that observes itself in one of the states $\text{waking}$, ready, or propose at time $t_{\text{sleep}} - T_1 - d$. By time $t_{\text{sleep}} + d$, it will memorize all nodes from $A$ in accept (provided that it did not switch to accept in the meantime). Hence, it satisfies $tr(\text{waking}, \text{recover})$, $tr(\text{ready}, \text{propose})$, and $tr(\text{propose}, \text{accept})$ until it switches to either recover or accept. It follows that any such node must have switched to recover or accept by time $t_s + 3d < t_s + T_1 + 2d$. On the other hand, nodes that do not observe themselves in state $\text{waking}$ at time $t_{\text{sleep}} - T_1 - d$ but are in one of the states $\text{sleep}$, $\text{sleep} \rightarrow \text{waking}$, or waking at this time or switch to sleep during time $(t_{\text{sleep}} - T_1 - d, t_{\text{sleep}} + 2T_1 + 3d]$ must have reset their timeout $T_2$ at some time from

$$\left(t_{\text{sleep}} - (2\vartheta + 3)T_1 - 4d, t_{\text{sleep}} + \left(2 - \frac{1}{\vartheta}\right)T_1 + 3d\right),$$
i.e., Statement (ii) holds. To infer Statement (i), it remains to show that none of the latter nodes may switch to ready until time $t_{\text{sleep}} + 2T_1 + 3d$. As no nodes from $W$ are in state $\text{join}$ during $[t_{\text{sleep}} - T_1 - d, t_{\text{sleep}} + 2T_1 + 3d]$ by assumption, the statement follows immediately from Statement (ii), as

$$t_{\text{sleep}} - (2\vartheta + 3)T_1 + \frac{T_2}{\vartheta} - 4d \geq t_{\text{sleep}} + 2T_1 + 3d.$$ 

The lemma follows.

Granting that nodes are not in state $\text{join}$ for sufficiently long, this implies that nodes will switch to $\text{sleep}$ in rough synchrony with others or drop out of the basic cycle and switch to recover.

Corollary 4.6: Assume that at time $t_{\text{sleep}}$, a node from $W$ switches to $\text{sleep}$, no node is in state $\text{join}$ during $[t_{\text{sleep}} - T_1 - d, t_{\text{sleep}} + 2T_1 + 4d]$, and also that during $(t_{\text{sleep}} - \Delta_g, t_{\text{sleep}}) = (t_{\text{sleep}} - (2\vartheta + 3)T_1, t_{\text{sleep}})$ no node in $W$ is in state $\text{sleep}$. Then at time $t_{\text{sleep}} + 2T_1 + 4d$, any node from $W$ is either in one of the states $\text{sleep}$ or $\text{sleep} \rightarrow \text{waking}$ and observed in $\text{sleep}$, or it is and is observed in state $\text{recover}$.

Proof: We apply Lemma 4.5 to see that at time $t_{\text{sleep}} + 2T_1 + 3d$, all nodes are in one of the states $\text{sleep}$, $\text{sleep} \rightarrow \text{waking}$, $\text{waking}$, or recover. As nodes remain in $\text{sleep}$ for a timeout of duration $(2\vartheta + 1)T_1 \geq \vartheta(2T_1 + 4d)$, the statement of the corollary follows immediately provided that we can show that any node that does not switch to state $\text{sleep}$ during $[t_{\text{sleep}}, t_{\text{sleep}} + T_1 + 3d]$ is not in state $\text{waking}$ at time $t_{\text{sleep}} + T_1 + 3d$. Consider such a node. If there is a time from $(t_{\text{sleep}} - \Delta_g, t_{\text{sleep}} + T_1 + 3d]$ when the node is not in one of the states $\text{sleep}$, $\text{sleep} \rightarrow \text{waking}$, or $\text{waking}$, it cannot be in state $\text{waking}$ at time $t_{\text{sleep}} + 2T_1 + 5d$, since it could not have switched to $\text{sleep}$ again in order to get there. Assume w.l.o.g. that the node switches to $\text{sleep}$ exactly at time $t_{\text{sleep}} - \Delta_g$. Thus, it must have previously reset its timeout $T_2$ no later than

$$t_{\text{sleep}} - \Delta_g - \frac{T_2}{\vartheta} \leq t_{\text{sleep}} - \Delta_g - 4d.$$

Hence we conclude by Lemma 4.5 that the node is in state $\text{recover}$ at time $t_{\text{sleep}} + 2T_1 + 5d$, finishing the proof.

B. Resynchronization Points

In this section, we derive that within linear time, it is very likely that good resynchronization points occur. As a first step, we infer from Lemma 4.5 that whenever nodes may not enter state $\text{join}$, the time windows during which nodes may switch to $\text{sleep}$ occur infrequently.

Lemma 4.7: Suppose no node is in state $\text{join}$ during $[t-, t^+]$. Then the volume of times $t \in [t^- + T_1 + d, t^+]$ satisfying that no node is in state $\text{sleep}$ during $(t - \Delta_g, t)$ is at least

$$\left(\frac{T_2 - 2\vartheta \Delta_g - (\vartheta - 1)T_1 - 4d}{T_2 - (\vartheta - 1)T_1 - \vartheta d}\right) (t^+ - t^-) - 4\Delta_g + T_1 + 7d).$$

Proof: Denote by $t_0$ the infimum of times from $[t^- + T_1 + d, t^+]$ when a node switches to $\text{sleep}$. Thus, by definition any time $t \in [t^- + \Delta_g + T_1 + d, t_0]$ satisfies that no node is in state $\text{sleep}$ during $(t - \Delta_g, t)$. We proceed by induction over increasing times $t_i \in (t_0, t^+)$, $i \in \{1, \ldots, i_{\text{max}}\}$. The induction halts at index $i_{\text{max}} \in \mathbb{N}$ iff $t_{i_{\text{max}}} > t^+ - T_2 / \vartheta + (1 - 1/\vartheta)T_1 + d$. We claim that, for each $i$, the volume of times $t \in [t^- + T_1 + d, t_i]$ such that no node is in state $\text{sleep}$ during $(t, t - \Delta_g)$ is at least

$$t_i - t^- - (T_1 + d) - i(2\Delta_g + 3d)$$

and that

$$t_i \geq t^- - (2\vartheta + 1 + 1/\vartheta)T_1 - 2d$$

$$\quad + i\left(\frac{T_2}{\vartheta} - \left(1 - \frac{1}{\vartheta}\right)T_1 - d\right).$$

In fact, we will show these bounds by establishing that no node is in state $\text{sleep}$ during

$$(t_{i-1} + (2\vartheta + 3)T_1 + 3d, t_i) = (t_{i-1} + \Delta_g + 3d, t_i)$$

and that

$$t_i \geq t_{i-1} + \frac{T_2}{\vartheta} - \Delta_g - 4d \geq t_{i-1} + 2\Delta_g + 3d$$

for all $i \in \{1, \ldots, i_{\text{max}}\}$.

We first establish these bounds for $t_1$. By Lemma 4.5 every node not switching to state $\text{recover}$ until time $t_0 + T_1 + 3d$ resets $T_2$ at some time from $(t_0 - \Delta_g - 4d, t_0 + 3d)$ and is in one of the states $\text{sleep}$, $\text{sleep} \rightarrow \text{waking}$, or $\text{waking}$ at time $t_0 + T_1 + 3d$. Hence, such nodes do not switch to
state \textit{ready} and subsequently to \textit{propose}, \textit{accept}, and \textit{sleep} again until \( t_0 + T_2/\vartheta - \Delta_y - 4d \leq t^+ \), giving
\[
t_1 \geq t_0 + \frac{T_2}{\vartheta} - \Delta_y - 4d.
\]
Moreover, the lemma implies that no node is in state \textit{sleep} during \([t_0 + (2\vartheta + 3)T_1 + 3d, t_1]\), as any node in state \textit{sleep} at time \( t_0 + 2T_1 + 3d \) will leave after a timeout of \((2\vartheta + 1)T_1\) expires. Hence, the volume of times \( t \in [t^- + T_1 + d, t_1] \) such that no node is in state \textit{sleep} during \((t, t - \Delta_y)\) is at least
\[
t_0 - (t^- + T_1 + d + \Delta_y) + t_1 - (t_0 + \Delta_y + 3d),
\]
showing the claim for \( i = 1 \).

We now perform the induction step from \( i < i_{\text{max}} \) to \( i+1 \). By (20), no node is in state \textit{sleep} during
\[
(t_{i-1} + \Delta_y + 3d, t_i) \supseteq (t_i - \Delta_y, t_i).
\]
Hence we can apply Corollary 4.6 to see that nodes not observing themselves in state \textit{Hence we can apply Corollary 4.6 to see that nodes not observing themselves in state \textit{ready} such nodes do not switch to state \textit{ready}\). By (20), no node is in state \textit{sleep} during \((t, t - \Delta_y)\) is at least
\[
t_0 - (t^- + T_1 + d + \Delta_y) + t_1 - (t_0 + \Delta_y + 3d),
\]
showing the claim for \( i = 1 \).

We now perform the induction step from \( i < i_{\text{max}} \) to \( i+1 \). By (20), no node is in state \textit{sleep} during
\[
(t_{i-1} + \Delta_y + 3d, t_i) \supseteq (t_i - \Delta_y, t_i).
\]
Hence we can apply Corollary 4.6 to see that nodes not observing themselves in state \textit{sleep} during \((t, t - \Delta_y)\) is at least
\[
st_1 \geq t_i + \frac{T_2}{\vartheta} - (1 - \frac{1}{\vartheta})T_1 - d.
\]
Moreover, no node is in state \textit{sleep} during \([t_{i+1} + (2\vartheta + 3)T_1 + 3d, t_{i+1}]\). These two statements show Corollary 4.6 and Inequality (21) for \( i+1 \), and by means of the induction hypothesis directly imply Inequality (18) and Inequality (19) for \( i+1 \) as well, i.e., the induction succeeds.

From Inequality (19) we have that
\[
i_{\text{max}} \leq \frac{t^+ - t^- + (2\vartheta + 1 + 1/\vartheta)T_1 + 2d}{T_2/\vartheta - (1 - 1/\vartheta)T_1 - d} + 1.
\]
Observe that the same reasoning as above shows that no node switches to \textit{sleep} during \([t_{i_{\text{max}}} + \Delta_y + 3d, t^+]\) since
\[
t_{i_{\text{max}}} \geq t^+ - (T_2/\vartheta - (1 - 1/\vartheta)T_1 - d).\]
Thus, inserting \( i = i_{\text{max}} \) into Inequality (18) we infer that the volume of times \( t \in [t^- + T_1 + d, t^+] \) such that no node is in state \textit{sleep} during \((t, t - \Delta_y)\) is at least
\[
t^+ + t^- - (T_1 + d) - (i_{\text{max}} + 1)(2\Delta_y + 3d)
\[
\geq \left( T_2 - 2\vartheta(\Delta_y - \vartheta - 1)T_1 - 4\vartheta d \right) (t^+ - t^-)
\]
concluding the proof. ■

We are now ready to advance to proving that good resynchronization points are likely to occur within bounded time, no matter what the strategy of the adversary is. To this end, we first establish that in any execution, at most of the times a node switching to state \textit{init} will result in a good resynchronization point. This is formalized by the following definition.

\textbf{Definition 4.8 (Good Times):} Given an execution \( E \) of the system, denote by \( E' \) any execution satisfying that \( E'|_{[0,t)} = E|_{[0,t)} \), where at time \( t \) a node \( i \in W \) switches to state \textit{init} in \( E' \). Time \( t \) is \textit{good in} \( E \) with respect to \( W \) provided that for any such \( E' \) it holds that \( t \) is a good \( W \)-resynchronization point in \( E' \).

The previous statement thus boils down to showing that in any execution, the majority of the times is good.

\textbf{Lemma 4.9:} Given any execution \( E \) and any time interval \([t^-, t^+]\), the volume of good times in \( E \) during \([t^-, t^+]\) is at least
\[
\lambda^2 (t^+ - t^-) - \frac{11(1 - \lambda)R_2}{10\vartheta}.
\]

\textbf{Proof:} Assume w.l.o.g. that \(|W| = n - f\) (otherwise consider a subset of size \( n - f \)) and abbreviate
\[
N:= \left( \frac{\vartheta (t^+ - t^-)}{R_2} + \frac{1}{10} \right) (n - f)
\]
\[
\geq \left[ \frac{\vartheta (t^+ - t^-) + R_2/10}{R_2} \right] (n - f)
\]
\[
\geq \left[ \frac{\vartheta (t^+ - t^-) + (R_1 + 4\Delta_y + T_1 + 10d)/(5(1 - \lambda))}{R_2} \right] (n - f).
\]
The proof is in two steps: First we construct a measurable subset of \([t^-, t^+]\) that comprises good times only. In a second step a lower bound on the volume of this set is derived.

\textbf{Constructing the set:} Consider an arbitrary time \( t \in [t^-, t^+] \), and assume a node \( i \in W \) switches to state \textit{init} at time \( t \). When it does so, its timeout \( R_3 \) expires. By Lemma 4.3 all timeouts of node \( i \) that expire at times within \([t^-, t^+]\), have been reset at least once until time \( t^- \). Let \( t_{R_3} \) be the maximum time not later than \( t \) when \( R_3 \) was reset. Due to the distribution of \( R_3 \) we know that
\[
t_{R_3} \leq t - (R_2 + 3d).
\]
Thus, node \( i \) is not in state \textit{init} during time \([t - (R_2 + 2d), t] \), and no node \( j \in W \) observes \( i \) in state \textit{init} during time \([t - (R_2 + d), t] \). Thereby any node \( j \)'s, \( j \in W \), timeout \((R_2, \text{supp } i)\) corresponding to node \( i \) is expired at time \( t \).

We claim that the condition that no node from \( W \) is in or observed in one of the states \textit{resync} or \textit{supp} \( \rightarrow \text{resync} \) at time
is sufficient for $t$ being a $W$-resynchronization point. To see this, assume that the condition is satisfied. Thus all nodes $j \in W$ are in states none or supp $k$ for some $k \in \{1, \ldots, n\}$ at time $t$. By the algorithm, they all will switch to state supp $i$ or state supp $\rightarrow$ resync during $(t, t + d)$. It might happen that they subsequently switch to another state supp $k'$ for some $k' \in V$, but all of them will be in one of the states with signal supp during $(t + d, t + 2d]$. Consequently, all nodes will observe at least $n - f$ nodes in state supp during $(t', t + 2d)$ for some time $t' < t + 2d$. Hence, those nodes in $W$ that were still in state supp $i$ (or supp $k'$ for some $k'$) at time $t + d$ switch to state supp $\rightarrow$ resync before time $t + 2d$, i.e., $t$ is a $W$-resynchronization point.

We proceed by analyzing under which conditions $t$ is a good $W$-resynchronization point. Recall that in order for $t$ to be good, it has to hold that no node from $W$ switches to state sleep during $(t - \Delta_g, t)$ or is in state join during $(t - T_1 - d, t + 4d)$.

We begin by characterizing subsets of good times within $(t_r, t'_r) \subseteq [t^-, t^+]$, where $t_r$ and $t'_r$ are times such that during $(t_r, t'_r)$ no node from $W$ switches to state supp $\rightarrow$ resync. Due to timeout

$$ R_1 \geq (4\vartheta + 2)d, $$

we know that during $(t_r + R_1 + 2d, t'_r)$, no node from $W$ will be in, or be observed in, states supp $\rightarrow$ resync or resync. Thus, if a node from $W$ switches to init at a time within $(t_r + R_1 + 2d, t'_r)$, it is a $W$-resynchronization point. Further, all nodes in $W$ will be in state dormant during $(t_r + R_1 + 2d, t'_r + 4d)$. Thus all nodes in $W$ will be observed to be in state dormant during $(t_r + R_1 + 3d, t'_r + 4d)$, implying that they are not in state join during $(t_r + R_1 + 3d, t'_r + 4d)$. In particular, any time $t \in (t_r + R_1 + T_1 + d, t'_r)$ satisfies that no node in $W$ is in state join during $(t - T_1 - d, t + 4d)$.

Applying [Corollary 4.7] we infer that the total volume of times from $(t_r, t'_r)$ that is good is at least

$$\left(\frac{T_2 - 2\vartheta\Delta_g - (\vartheta - 1)T_1 - 4\vartheta d}{T_2 - (\vartheta - 1)T_1 - \vartheta d}\right)(t^+ - t^-) - (4\Delta_g + T_1 + 10d).$$

(24)

In other words, up to a constant loss in each interval $(t_r, t'_r)$, a constant fraction of the times are good.

**Volume of the set:** In order to infer a lower bound on the volume of good times during $[t^-, t^+]$, we subtract from $t^+ - t^-$ the volume of some intervals during which we cannot exclude that a node switches to supp $\rightarrow$ resync, increased by the constant term $R_1 + 4\Delta_g + T_1 + 10d$ from [Inequality (24)]. The inequality then yields that at least a fraction of $\left(\frac{T_2 - 2\vartheta\Delta_g - (\vartheta - 1)T_1 - 4\vartheta d}{T_2 - (\vartheta - 1)T_1 - \vartheta d}\right)$ of the remaining volume of times is good. Note that we also need to account for the fact that nodes may already be in state supp $\rightarrow$ resync at time $t^-$, which we account for by also covering events prior to $t^-$ when nodes switch to supp $\rightarrow$ resync. Formally, we define

$$\bar{G} = \bigcup_{t \in [t^-, t^+] \setminus \bar{G}} [t_r, t_r + R_1 + 4\Delta_g + T_1 + 10d]\bigcup_{\exists t \in W: t \text{ switches to supp} \rightarrow \text{resync} \text{ at } t_r}\\text{and strive for a lower bound on the volume of } [t^-, t^+] \setminus \bar{G}.\text{ In order to lower bound the good times in } [t^-, t^+], \text{ it is thus sufficient to cover all times when a node switches to supp} \rightarrow \text{resync during } [t^+ - (R_1 + 4\Delta_g + T_1 + 10d), t^+].\text{ By } 2N - 1 \text{ intervals of volume at most } V \text{ and then infer a lower bound of } t^+ - t^- - 2N(\mathcal{V} + R_1 + 4\Delta_g + T_1 + 10d) \text{ on the volume of } [t^-, t^+] \setminus \bar{G}.\text{ The remainder of the proof hence is concerned with deriving such a cover of the times when nodes may switch to supp} \rightarrow \text{resync during } [t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+].$$

Observe that any node in $W$ does not switch to state init more than

$$\frac{t^+ - t^- + R_1 + 4\Delta_g + T_1 + 10d}{R_3} \leq \frac{t^+ - t^- + R_1 + 4\Delta_g + T_1 + 10d}{R_2 + d} \leq \frac{N}{n - f}$$

(25)

times during $[t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+]$.

Now consider the case that a node in $W$ switches to state supp $\rightarrow$ resync at a time $t$ satisfying that no node in $W$ switched to state init during $(t - (8\vartheta + 6)d, t)$. This necessitates that this node observes $n - f$ of its channels in state supp during $(t - (2\vartheta + 1)d, t)$, at least $n - 2f + 1$ of which originate from nodes in $W$. As no node from $W$ switched to init during $(t - (8\vartheta + 6)d, t)$, every node that has not observed a node $i \in V \setminus W$ in state init at a time from $(t - (8\vartheta + 4)d, t)$ when $(R_2, \text{supp } i)$ is expired must be in a state whose signal is none during $(t - (2\vartheta + 2)d, t)$ due to timeouts. Therefore its outgoing channels are not in state supp during $(t - (2\vartheta + 1)d, t)$. By means of contradiction, it thus follows that for each node $j$ of the at least $f + 1$ nodes (which are all from $W$), there exists a node $\bar{i} \in V \setminus W$ such that node $j$ resets timeout $(R_2, \text{supp } \bar{i})$ during the time interval $(t - (8\vartheta + 4)d, t)$.

The same reasoning applies to any time $t' \notin (t - (8\vartheta + 6)d, t)$ satisfying that some node in $W$ switches to state supp $\rightarrow$ resync at time $t'$ and no node in $W$ switched to state init during $(t' - (8\vartheta + 6)d, t')$. Note that the set of the respective at least $f + 1$ events (corresponding to the at least $f + 1$ nodes from $W$) where timeouts $(R_2, \text{supp } i)$ with $i \in V \setminus W$ are reset and the set of the events corresponding to $t$ are disjoint. However, the total number of events where such a timeout can be reset during $[t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+]$
is upper bounded by
\[ |V \setminus W||W| \left( t^+ - t^- + R_1 + 4\Delta_g + T_1 + 10d \right) R_2/\vartheta \]
\[ \leq (f + 1)N, \tag{26} \]
i.e., the total number of channels from nodes not in \( W \) \((|V \setminus W| \text{ many})\) to nodes in \( W \) multiplied by the number of times an associated timeout can expire at a receiving node in \( W \) during \([t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+]\).

With the help of inequalities (25) and (26), we can show that \( G \) can be covered by less than \( 2N \) intervals of size \((R_1 + 4\Delta_g + T_1 + 10d) + (8\vartheta + 6)d\) each. By \textbf{Inequality (25)} there are no more than \( N \) times \( t \in [t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+] \) when one of the \(|W| = n - f\) many non-faulty nodes switches to \textit{init} and thus may cause others to switch to \textit{state supp \rightarrow resync} at times in \([t, t + (8\vartheta + 6)d]\). Similarly, \textbf{Inequality (26)} shows that the channels from \( V \setminus W \) to \( W \) may cause at most \( N \) such times \( t \in [t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+] \), since any such time requires the existence of at least \( f + 1 \) events where timeouts \((R_2, \text{supp } i), i \in V \setminus W, \) are reset at nodes in \( W, \) and the respective events are disjoint. Thus, all times \( t_r \in [t^- - (R_1 + 4\Delta_g + T_1 + 10d), t^+] \) when some node \( i \in W \) switches to \textit{supp \rightarrow resync} are covered by at most \( 2N - 1 \) intervals of length \((8\vartheta + 6)d\).

This results in a cover \( G' \supseteq G \) consisting of at most \( 2N - 1 \) intervals that satisfies
\[ \text{vol}(G) \leq \text{vol}(G') < 2N(R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d). \]

As argued previously, summing over the at most \( 2N \) intervals that remain in \([t^- , t^+] \setminus G'\) and using \textbf{Inequality (24)} it follows that the volume of good times during \([t^- , t^+]\) is at least
\[ T_2 - 2\vartheta\Delta_g - ((\vartheta - 1)T_1 - 4\vartheta d) \]
\[ = \frac{\lambda(t^+ - t^- - 2N(R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d))}{T_2 - (\vartheta - 1)T_1 - \vartheta d} \]
\[ \geq \frac{\lambda(t^+ - t^- - 2N(R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d))}{T_2 - (\vartheta - 1)T_1 - \vartheta d} \]
\[ = \frac{\lambda(t^+ - t^- - 2N(R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d))}{R_2} \]
\[ \geq \frac{\lambda(t^+ - t^- - 11\lambda(R_1 + 4\Delta_g + T_1 + (8\vartheta + 16)d)(n - f)}{5} \]
\[ \geq \lambda^2(t^+ - t^-) - \frac{11(1 - \lambda)R_2}{10\vartheta}, \]
as claimed. The lemma follows. \( \blacksquare \)

We are now in the position to prove our second main theorem, which states that a good resynchronization point occurs within \( O(R_2) \) time with overwhelming probability.

\textbf{Theorem 4.10:} Denote by \( \hat{E}_3 := \vartheta(R_2 + 3d) + 8(1 - \lambda)R_2 + d \) the maximal value the distribution \( R_3 \) can attain plus the at most \( d \) time until \( R_3 \) is reset whenever it expires. For any \( k \in \mathbb{N} \) and any time \( t, \) with probability at least \( 1 - (1/2)^{k(n - f)}\) there will be a good \( W\)-resynchronization point during \([t, t + (k + 1)\hat{E}_3]\).

\textbf{Proof:} Assume w.l.o.g. that \(|W| = n - f\) (otherwise consider a subset of size \( n - f\)). Fix some node \( i \in W \) and denote by \( t_0 \) the infimum of times from \([t, t + (k + 1)\hat{E}_3]\) when node \( i \) switches to \textit{init}. We have that \( t_0 < t + \hat{E}_3. \) By induction, it follows that node \( i \) will switch to state \textit{init} at least another \( k \) times during \([t, t + (k + 1)\hat{E}_3]\) at the times \( t_1 < t_2 < \ldots < t_k. \) We claim that each such time \( t_1, j \in \{1, \ldots, k\}, \) has an independently by \( 1/2 \) lower bounded probability of being good and therefore being a good \( W\)-resynchronization point.

We prove this by induction on \( j: \) As induction hypothesis, suppose for some \( j \in \{1, \ldots, k - 1\}, \) we showed the statement for \( j' \in \{1, \ldots, j - 1\} \) and the execution of the system is fixed until time \( t_{j-1}, \) i.e., \( E_{[0,t_{j-1}]} \) is given. Now consider the set of executions that are extensions of \( E_{[0,t_{j-1}]} \) and have the same clock functions as \( E. \) For each such execution \( E' \) it holds that \( E'_{[0,t_{j-1}]} = E_{[0,t_{j-1}]} \), and all nodes' clocks make progress in \( E' \) as in \( E. \) Clearly each such \( E' \) has its own time \( t_j < t + (j + 1)\hat{E}_3 \) when \( R_3 \) expires next after \( t_{j-1} \) at node \( i, \) and \( i \) switches to \textit{init}. We next characterize the distribution of the times \( t_j. \)

As the rate of the clock driving node \( i \)'s \( R_3 \) is between \( 1 \) and \( \vartheta, t_j > t_{j-1} \) is within an interval, call it \([t^-, t^+]\), of size at most
\[ t^+ - t^- \leq 8(1 - \lambda)R_2, \]
regardless of the progress that \( i \)'s clock \( C \) makes in any execution \( E'. \)

Certainly we can apply \textbf{Lemma 4.9} also to each of the \( E' \), showing that the volume of times from \([t^-, t^+]\) that are not good in \( E' \) is at most
\[ (1 - \lambda^2)(t^+ - t^-) + \frac{11(1 - \lambda)R_2}{10\vartheta}. \]

Since clock \( C \) can make progress not faster than at rate \( \vartheta \) and the probability density of \( R_3 \) is constantly \( 1/(8(1 - \lambda)R_2) \) (with respect to the clock function \( C \)), we obtain that the probability of \( t_j \) not being a good time is upper bounded by
\[ \frac{(1 - \lambda^2)(t^+ - t^-) + 11(1 - \lambda)R_2/(10\vartheta)}{8(1 - \lambda)R_2/\vartheta} \leq \frac{\vartheta(1 - \lambda^2) + \frac{11}{80}}{\frac{9}{25\vartheta} + \frac{7}{50}} = \frac{1}{2}. \]

Here we use that the time when \( R_3 \) expires is independent of \( E'_{[0,t_{j-1}]} \).
We complete our reasoning as follows. Given $E_{[0,t_{j-1}]}$, we permit an adversary to choose $E'$, including random bits of all nodes and full knowledge of the future, with the exception that we deny it control or knowledge of the time $t_j$ when $R_3$ expires at node $i$, i.e., $E'$ is an imaginary execution in which $R_3$ does not expire at $i$ at any time greater than $t_{j-1}$. Note that for the good $W$-resynchronization points we considered, the choice of $E'$ does not affect the probability that $t_1, \ldots, t_{j-1}$ are good $W$-resynchronization points: The conditions referring to times greater than a $W$-resynchronization point $t$, i.e., that all nodes in $W$ switch to state $supp \rightarrow resync$ during $(t, t+2d)$ and no node in $W$ shall be in state $join$ during $(t-T_1-d, t+4d)$, are already fully determined by the history of the system until time $t$. As we fixed $E'$, the behavior of the clock driving $R_3$ is fixed as well. Next, we determine the time $t_j$ when $R_3$ expires according to its distribution, given the behavior of node $i$’s clock. The above reasoning shows that time $t_j$ is good in $E'$ with probability at least $1/2$, independently of $E_{[0,t_{j-1}]} = E_{[0,t_{j-1}]}$. We define that $E_{[0,t_j]} = E'(0,t_j)$ and in $E$ node $i$ switches to state $init$ (because $R_3$ expired). As—conditional to the clock driving $R_3$ and $t_{j-1}$ being specified—$t_j$ is independent of $E_{[0,t_j]}$, $E$ is indistinguishable from $E'$ until time $t_j$. Because $t_j$ is good with probability at least $1/2$ independently of $E_{[0,t_{j-1}]}$, so it is in $E$. Hence, in $E$ $t_j$ is a good $W$-resynchronization point with probability $1/2$, independently of $E_{[0,t_{j-1}]}$. Since $E'$ was chosen in an adversarial manner, this completes the induction step.

In summary, we showed that for any node in $W$ and any execution (in which we do not manipulate the times when $R_3$ expires at the respective node), starting from the second time during $[t, t+(k+1)E_3]$ when $R_3$ expires at the respective node, there is a probability of at least $1/2$ that the respective time is a good $W$-resynchronization point. Since we assumed that $|W| = n - f$ and there are at least $k$ such times for each node in $W$, this implies that having no good $W$-resynchronization point during $[t, t+(k+1)E_3]$ is as least as unlikely as $k(n-f)$ unbiased and independent coin flips all showing tail, i.e., $(1/2)^{k(n-f)}$. This concludes the proof.

C. Stabilization via Good Resynchronization Points

Having established that eventually a good $W$-resynchronization point $t_g$ will occur, we turn to proving the convergence of the main routine. We start with a few helper statements wrapping up that a good resynchronization point guarantees proper reset of flags and timeouts involved in the stabilization process of the main routine.

Lemma 4.11: Suppose $t_g$ is a good $W$-resynchronization point. Then

(i) Each node $i \in W$ switches to $passive$ at a time $t_i \in (t_g + 4d, t_g + (4\bar{d} + 3)d)$ and observes itself in state $dormant$ during $[t_g + 4d, \tau_{\bar{t}_i}(t_i))$,

(ii) $\text{Mem}_{i,j,\text{join}}[\tau_{\bar{t}_i}(t_i), t_{\text{sw}}] \equiv 0$ for all $i, j \in W$, where $t_{\text{join}} \geq t_g + 4d$ is the infimum of all times greater than $t_g - T_1 - d$ when a node from $W$ switches to $join$,

(iii) $\text{Mem}_{i,j,\text{sleep} \rightarrow \text{waking}}[\tau_{\bar{t}_i}(t_i), t_i] \equiv 0$ for all $i, j \in W$, where $t_s \geq t_g + (1 + 1/\bar{d})T_1$ is the infimum of all times greater or equal to $t_g$ when a node from $W$ switches to $sleep \rightarrow \text{waking}$,

(iv) No node from $W$ resets its $sleep \rightarrow \text{waking}$ flags during $[t_g + (1 + 1/\bar{d})T_1, t_g + R_1/\bar{d})$, and

(v) No node from $W$ resets its $join$ flags due to switching to $passive$ during $[t_g + (1 + 1/\bar{d})T_1, t_g + R_1/\bar{d})$.

Proof: All nodes in $W$ switch to state $supp \rightarrow resync$ during $(t_g, t_g + 2d)$ and switch to state $resync$ when their timeout of $\bar{d}4d$ expires, which does not happen until time $t_g + 4d$. Once this timeout expired, they switch to state $passive$ as soon as they observe themselves in state $resync$, i.e., by time $t_g + (4\bar{d} + 3)d$. Hence, every node $i \in W$ does not observe itself in state $resync$ within $[t_g + 3d, \tau_{\bar{t}_i}(t_i)]$, and therefore is in state $dormant$ during $[t_g + 3d, \tau_{\bar{t}_i}(t_i)]$. This implies that it observes itself in state $dormant$ during $[t_g + 4d, \tau_{\bar{t}_i}(t_i)]$, completing the proof of Statement (i).

Moreover, from the definition of a good $W$-resynchronization point we have that no nodes from $W$ are in state $join$ at times in $[t_g - T_1 - d, t_{\text{join}})$. Statement (ii) follows, as every node from $W$ resets its $join$ flags upon switching to state $passive$ at time $t_i$.

Regarding Statement (iii), observe first that no nodes from $W$ are in state $sleep \rightarrow \text{waking}$ during $(t_g - d, t_g + (1 + 1/\bar{d})T_1)$ for the following reason: By definition of a good $W$-resynchronization point no node from $W$ switches to sleep during $(t_g - \Delta_g, t_g) \supset (t_g - (2\bar{d} + 1)T_1 - 3d, t_g)$. Any node in $W$ that is in states $sleep$ or $sleep \rightarrow \text{waking}$ at time $t_g - (2\bar{d} + 1)T_1 - 3d$ switches to state $waking$ before time $t_g - d$ due to timeouts. Finally, any node in $W$ switching to $sleep$ at or after time $t_g$ will not switch to state $sleep \rightarrow \text{waking}$ before time $t_g + (1 + 1/\bar{d})T_1$. The observation follows.

Since nodes in $W$ reset their $sleep \rightarrow \text{waking}$ flags at some time from

$$[t_i, \tau_{\bar{t}_i}(t_i)] \subset (t_g + 3d, t_g + (4\bar{d} + 4)d) \supseteq (t_g + 3d, t_g + (1 + 1/\bar{d})T_1),$$

Statement (iii) follows.

Statements (iv) and (v) follow from the fact that all nodes in $W$ switch to state $passive$ until time

$$t_g + (3 + 4\bar{d})d \leq t_g + (1 + 1/\bar{d})T_1 - d,$$

while timeout $(R_1, supp \rightarrow resync)$ must expire first in order to switch to $dormant$ and subsequently $passive$ again.
Before we proceed with our third main statement showing eventual stabilization, we make a few more basic observations. Firstly, if nodes do not make progress on the basic cycle, they must eventually switch to recover, i.e., the timeout conditions ensure detection of deadlocks.

**Lemma 4.12:** For any time $t^-$ and any node it holds that it must be in state recover or join or switch to sleep at some time from $[t^-, t^- + (1 - 1/\vartheta)T_1 + T_2 + T_4 + T_5 + 4d]$.  

**Proof:** Suppose a node is never in state recover or join during $[t^-, t^- + (1 - 1/\vartheta)T_1 + T_2 + T_4 + T_5 + 4d]$. Thus it may follow transitions along the basic cycle only. Assume w.l.o.g. that the node switched to sleep right before time $t^-$. Thus, it switched to state accept beforehand, no later than time $t^- - T_1/\vartheta$. Due to timeouts, either switch to recover at some point in time or switch to sleep, sleep $\rightarrow$ waking, waking, ready, propose, accept, and finally sleep again. At each state, it takes less than $d$ time until a respective timeout is started and it observes itself in the respective state. Hence, the node switches to recover or sleep before time

$$t^- - \frac{T_1}{\vartheta} + \max\{(2\vartheta + 2)T_1 + 3d, T_2\} + T_4 + T_5 + 4d,$$

proving the claim of the lemma. ■

Secondly, after a good $W$-resynchronization point $t_g$, no node from $W$ will switch to state join until either time $t_g + T_7/\vartheta + 4d$ or $T_6/\vartheta$ time after the first non-faulty node switched to sleep $\rightarrow$ waking again after $t_g$. By proper choice of $T_7 > T_6$ and $T_6$, this will guarantee that nodes from $W$ do not switch to join prematurely during the final steps of the stabilization process.

**Lemma 4.13:** Suppose $t_g$ is a good $W$-resynchronization point. Denote by $t_s$ the infimum of times greater than $t_g$ when a node in $W$ switches to state sleep $\rightarrow$ waking and by $t_{\text{join}}$ the infimum of times greater than $t_g - T_1 - d$ when a node in $W$ switches to state join. Then, starting from time $t_g + 4d$, $tr(\text{recover, join})$ is not satisfied at any node in $W$ until time

$$\min\left\{ t_g + \frac{T_7}{\vartheta} + 4d, t_s + \frac{T_6}{\vartheta} \right\} > t_{\text{join}}.$$

**Proof:** By Statements (ii) and (iii) of Lemma 4.11 and Inequality 2 we have that $t_s \geq t_g + T_4 + 4d \geq t_g + (4\vartheta + 4)d$ and $t_{\text{join}} \geq t_g + 4d$. Consider a node $i \in W$ not observing itself in state dormant at some time $t \in (t_g + 4d, t_{\text{join}}]$. According to Statements (i) and (ii) of Lemma 4.11, the threshold condition of $f + 1$ nodes memorized in state join cannot be satisfied at such a node. By statements (i) and (iii) of the lemma, the threshold condition of $f + 1$ nodes memorized in state sleep $\rightarrow$ waking cannot be satisfied unless $t > t_s$. Hence, if at time $t$ a node from $W$ satisfies that it observes itself in state active, we have that $T_5$ expired after being reset after time $t_s$, i.e., $t > t_s + T_6/\vartheta$. Moreover, by Statement (i) of Lemma 4.11 we have that if $T_7$ is expired at any node in $W$ at time $t$, it holds that $t > t_g + T_7/\vartheta + 4d$. Altogether, we conclude that $tr(\text{recover, join})$ is not satisfied at any node in $W$ during

$$\left[ t_g + 4d, \min\left\{ t_g + \frac{T_7}{\vartheta} + 4d, t_s + \frac{T_6}{\vartheta} \right\} \right].$$

In particular, $t_{\text{join}}$ must be larger than the upper boundary of this interval, concluding the proof. ■

Thirdly, after a good $W$-resynchronization point, any node in $W$ switches to recover or to sleep $\rightarrow$ waking within bounded time, and all nodes in $W$ doing the latter will do so in rough synchrony. Using the previous lemmas, we can show that this happens before the transition to join is enabled for any node.

**Lemma 4.14:** Suppose $t_g$ is a good $W$-resynchronization point and use the notation of Lemma 4.13. Define $t^+ := t_g - T_1/\vartheta + T_2 + T_4 + T_5 + 3d$ and denote by $t_{\text{sleep}}$ the infimum of all times greater than $t_g - \Delta_g$ when a node in $W$ switches to sleep. Then $t_{\text{sleep}} \geq t_g$ and either (i) $t_{\text{sleep}} < t^+$ and at time $t_{\text{sleep}} + 2T_1 + 4d$, any node in $W$ is either in one of the states sleep or sleep $\rightarrow$ waking and observed in sleep or is in recover and also observed in recover, or (ii) all nodes in $W$ are observed in state recover at time $t^+ + 2T_1 + 4d$.

**Proof:** By definition of a good resynchronization point, no node switches to sleep during $(t_g - \Delta_g, t_g)$, giving that $t_{\text{sleep}} \geq t_g$. If $t_{\text{sleep}} < t^+$, Lemma 4.13 yields that

$$t_{\text{join}} > \min\left\{ t_g + \frac{T_7}{\vartheta} + 4d, t_{\text{sleep}} + \frac{T_6}{\vartheta} \right\} \geq \min\left\{ t^+ + 2T_1 + 4d, t_{\text{sleep}} + \frac{T_6}{\vartheta} \right\} \geq t_{\text{sleep}} + 2T_1 + 4d.$$

Therefore, by definition of a good resynchronization point, no nodes are in state join during $(t_g - T_1 - d, t_{\text{join}}) \supset (t_g - T_1 - d, t_{\text{sleep}} + T_1 + 4d)$. Recalling that during $(t_g - \Delta_g, t_{\text{sleep}})$, no node is in state sleep, the preconditions of Corollary 4.7 hold, implying Statement (i).

If $t_{\text{sleep}} \geq t^+$, by definition of a good resynchronization point no node switched to sleep during $(t_g - \Delta_g, t^+) \supset (t_g - T_1 - d, t^+)$ and no node is in state join during $(t_g - T_1 - d, t_{\text{join}})$. By Lemma 4.13

$$t_{\text{join}} > \min\left\{ t_g + \frac{T_7}{\vartheta} + 4d, t_{\text{sleep}} + \frac{T_6}{\vartheta} \right\} \geq \min\left\{ t^+ + 2T_1 + 4d, t^+ + \frac{T_6}{\vartheta} \right\} \geq t^+ + 2T_1 + 4d.$$
Hence, Lemma 4.12 states that every node must be in state $\text{recover}$ at some time in $(t_g - T_1 - d, t^+)$. Since nodes do not leave state $\text{recover}$ during $(t_g - T_1 - d, t_{\text{join}})$, Statement (ii) follows.

We have everything in place for proving that a good resynchronization point leads to stabilization within $R_1/\vartheta - 3d$ time.

**Theorem 4.15:** Suppose $t_g$ is a good $W$-resynchronization point. Then there is a quasi-stabilization point during $(t_g, t_g + R_1/\vartheta - 3d]$.

Proof: For simplicity, assume during this proof that $R_1 = \infty$, i.e., by Statement (i) of Lemma 4.11 all nodes in $W$ observe themselves in states passive or active at times greater or equal to $t_g + (4\vartheta + 4)d$. We will establish the existence of a quasi-stabilization point at a time larger than $t_g$ and show that it is upper bounded by $t_g + R_1/\vartheta - 3d$.

Hence this assumption can be made w.l.o.g., as the existence of the quasi-stabilization point depends on the execution up to time $t_g + R_1/\vartheta$ only, and $R_1$ cannot expire before this time at any node in $W$. Moreover, by Statements (i) and (ii) of Lemma 4.11 every node satisfies $\text{Mem}_{i,j,\text{join}} \equiv 0$ on $[t_g + (4\vartheta + 4)d, t_{\text{join}})$, where $t_{\text{join}}$ denotes the infimum of all times greater or equal to $t_g + (4\vartheta + 4)d$ when node $i$ switches to $\text{join}$. During the time span considered in this proof, every node switches at most once to $\text{join}$, thus we may w.l.o.g. assume that $\text{Mem}_{i,j,\text{join}} = 0$ always is satisfied in the following. We use the notation of Lemmas 4.13 and 4.14. By Statements (ii) of Lemma 4.11 and Inequality (2) we have that $t_s \geq t_g + (1 - 1/\vartheta)T_1 \geq t_g + (4\vartheta + 4)d$.

According to Lemma 4.11 all nodes in $W$ switch to state passive during $(t_g + 4d, t_g + (3 + 4\vartheta)d)$, implying that at any node in $W$, $T_2$ will expire at some time from

$$(t_g + T_2/\vartheta + 4d, t_g + T_7 + (4\vartheta + 4)d)$$

By Lemma 4.13 thus $t_{\text{join}} > t_g + (1 + 1/\vartheta)T_1$, and by Statement (v) of Lemma 4.11 no node resets its $\text{join}$ flags after $t_g + (1 + 1/\vartheta)T_1$ again (before $R_1$ expires).

**Case 1:** Assume $t_{\text{sleep}} \geq t^+$. Thus, Statement (ii) of Lemma 4.14 applies, i.e., all nodes are observed in state $\text{recover}$ by time $t^+ + 2T_1 + 4d$. Any node from $W$ will switch to state $\text{join}$ before time $t_g + T_2 + (4\vartheta + 4)d$ because $T_7$ expires no later than that. Subsequently, it will switch to $\text{propose}$ as soon as it memorizes all non-faulty nodes in state $\text{join}$. Denote by $t_{\text{propose}} \in (t_g + T_2/\vartheta + 4d, t_g + T_7 + (4\vartheta + 5)d)$ the minimal time when a node from $W$ switches from $\text{join}$ to $\text{propose}$. Certainly, nodes in $W$ do not switch from $\text{waking}$ to $\text{ready}$ during $(t_{\text{propose}}, t_{\text{propose}} + 3d)$ and therefore also not reset their $\text{join}$ flags before time $t_{\text{propose}} + 3d$. As nodes in $W$ reset their $\text{propose}$ and $\text{accept}$ flags upon switching to $\text{join}$, some node in $W$ must memorize $n - 2f \geq f + 1$ non-faulty nodes in state $\text{join}$ at time $t_{\text{propose}}$. According to Statement (ii) of Lemma 4.11 these nodes must have switched to state $\text{join}$ at or after time $t_{\text{join}}$. Hence, all nodes in $W$ will memorize them in state $\text{join}$ by time $t_{\text{propose}} + d$ and thus have switched to state $\text{join}$. Hence, all nodes in $W$ will switch to state $\text{propose}$ before time $t_{\text{propose}} + 2d$ and subsequently to state $\text{accept}$ before time $t_{\text{propose}} + 3d$, i.e., $t_{\text{propose}} \leq t_g + T_2 + (4\vartheta + 5)d$ is a quasi-stabilization point.

**Case 2:** Assume $t_{\text{sleep}} < t^+$. By Statement (i) of Lemma 4.14 all nodes are observed in either $\text{sleep}$ or $\text{recover}$ at time $t_{\text{sleep}} + 2T_1 + 4d$. The nodes observed in state $\text{sleep}$ will have been observed in state $\text{sleep} \rightarrow \text{waking}$ and switched to waking by time $t_{\text{sleep}} + (2\vartheta + 3)T_1 + 5d$.

**Case 2a:** Suppose $f + 1$ nodes in $W$ are observed in state $\text{sleep}$ at time $t_{\text{sleep}} + 2T_1 + 4d$, i.e., $\geq n - 2f \geq f + 1$ non-faulty nodes are observed in state $\text{recover}$. By Lemma 4.13 we have that

$$t_{\text{sleep}} + (2\vartheta + 3)T_1 + 7d$$

$$\leq t_s + \left(2\vartheta + 3 - \frac{1}{\vartheta}\right)T_1 + 7d$$

$$\leq \min \left\{ t_s + T_6 \vartheta, t^+ + \left(2\vartheta + 3 - \frac{1}{\vartheta}\right)T_1 + 7d \right\}$$

$$\leq \min \left\{ t_s + T_6 \vartheta, t_{\text{sleep}} + T_7 + \vartheta, t_{\text{sleep}} + \vartheta \right\} < t_{\text{join}}.$$

Hence, any node observing itself in state $\text{waking}$ at some time $t \in (t_{\text{sleep}} + 2T_1 + 4d, t_{\text{sleep}} + (2\vartheta + 3)T_1 + 6d)$ will also observe at least $f + 1$ nodes in state $\text{recover}$ and switch to $\text{recover}$. As any node in $\text{sleep}$ or $\text{sleep} \rightarrow \text{waking}$ at time $t_{\text{sleep}} + 2T_1 + 4d$ will observe itself in state $\text{waking}$ no later than time $t_{\text{sleep}} + (2\vartheta + 3)T_1 + 6d$, by time $t_{\text{sleep}} + (2\vartheta + 3)T_1 + 7d < t_{\text{join}}$, all nodes observe themselves in state $\text{recover}$. From here we can argue analogously to the first case, i.e., there exists a quasi-stabilization point $t_{\text{propose}} \leq t_g + T_2 + (4\vartheta + 5)d$.

**Case 2b:** Suppose $\geq f + 1$ nodes in $W$ are observed in state $\text{sleep}$ at time $t_{\text{sleep}} + 2T_1 + 4d$. These nodes will switch to $\text{waking}$ and subsequently $\text{ready}$ until time

$$\max \left\{ t_{\text{sleep}} + (2\vartheta + 3)T_1 + 6d, t_{\text{sleep}} - \frac{T_1}{\vartheta} + T_2 + d \right\}$$

$$t_{\text{sleep}} = \frac{T_1}{\vartheta} + T_2 + d$$

(27)

due to $T_2$ being expired while observing themselves in $\text{waking}$ unless they switch from $\text{waking} \rightarrow \text{recover}$. Note that these nodes reset their $\text{accept}$ flags upon switching to $\text{waking}$. Denote by $t_{\text{propose}}$ and $t_{\text{accept}}$ the infima of times greater than $t_{\text{sleep}} + 2T_1 + 4d$ when a node switches to $\text{propose}$ or $\text{accept}$, respectively. Recall that any node switching from $\text{recover}$ to $\text{join}$ resets its $\text{propose}$ and $\text{accept}$ flags, and any node switching from $\text{waking}$ to $\text{ready}$ resets its $\text{propose}$ flags.

Hence, we have for all $i, j \in W$ that

(i) $\text{Mem}_{i,j,\text{propose}}(t) = 0$ at any time $t \in [t_{\text{sleep}} + 2T_1 + 4d, t_{\text{propose}}]$ when $i$ observes itself in $\text{ready}$ or $\text{join}$, and
By Statements (ii) and (iv) of Lemma 4.11, no node from $W$ resets its sleep → waking flags at or after time $t_\sigma \geq t_g + (1 + 1/\vartheta)T_1$. As $t_\sigma \geq t_{\text{sleep}} + 2T_1 + 4d$ and all nodes observed in sleep at time $t_{\text{sleep}} + 2T_1 + 4d$ will be observed in sleep → waking by time $t_{\text{sleep}} + (2\vartheta + 3)T_1 + 5d$, Statement (i) of the lemma implies that all nodes in $W$ switch to active at some time from $(t_\sigma, t_{\text{sleep}} + (2\vartheta + 3)T_1 + 5d) \subseteq (t_{\text{sleep}} + 2T_1 + 6d, t_{\text{sleep}} + (2\vartheta + 3)T_1 + 5d)$. As, by the Statements (i) and (ii) from above, the first node switching to state propose must do so because of an expiring timeout, Lemma 4.13 yields that

$$t_{\text{propose}} \geq \min \left\{ t_{\text{join}}, t_{\text{sleep}} - T_1 - d + \frac{T_2}{\vartheta} \right\}$$

$$\geq \min \left\{ t_g + \frac{T_7}{\vartheta} + 4d, t_\sigma + \frac{T_6}{\vartheta} \right\},$$

$$t_{\text{sleep}} - T_1 - d + \frac{T_2 + \min(T_3, T_4)}{\vartheta},$$

$$\geq \min \left\{ t_{\text{sleep}} - t^* + t_g, t_{\text{sleep}} + \left(2 - \frac{1}{\vartheta}\right)T_1 + \frac{T_6}{\vartheta} \right\},$$

$$t_{\text{sleep}} - T_1 - d + \frac{T_2 + T_3}{\vartheta},$$

$$t_{\text{sleep}} + \left(2 - \frac{1}{\vartheta}\right)T_1 + \frac{T_6}{\vartheta}.$$ 

By Inequality (27) we conclude that at time $t_{\text{sleep}} - T_1/\vartheta + T_2 + 2d < t_{\text{propose}}$, any node from $W$ observes itself in one of the states ready, recover, or join.

Continuing Case 2b: Next, we claim that any node is in states propose or join by time $t_{\text{sleep}} - T_1/\vartheta + T_2 + 2d$. To see this, observe that any node following the basic cycle must switch from ready to propose by this time due to timeouts. On the other hand, according to Inequality (29) all nodes in state recover switch to join by time

$$t_{\text{sleep}} - T_1 - d + \frac{T_2 + T_3}{\vartheta} \leq t_{\text{sleep}} - T_1/\vartheta + T_2 + T_3 + 2d,$$

showing the claim.

In summary, we showed the following points:

(i) At time $t_{\text{propose}} + d$, all nodes are observed in states ready, join, propose, or accept.

(ii) All nodes switch to states propose or join during $[\min\{t_{\text{join}}, t_{\text{propose}}\}, t_{\text{sleep}} - T_1/\vartheta + T_2 + T_3 + 2d]$.

(iii) No node resets its propose or accept flags at or after time $t_{\text{propose}} + d$ unless switching to accept first.

(iv) No node memorizes nodes in state propose or accept that have not been in that state at or after time $t_{\text{propose}}$.

We claim that the infimum $t_q$ of all times from

$$\left[ t_{\text{propose}}, t_{\text{sleep}} - T_1/\vartheta + T_2 + T_3 + d \right]$$

when a node switches to accept is a quasi-stabilization point. Note that because

$$t_{\text{sleep}} - T_1/\vartheta + T_2 + T_3 + d \leq t_{\text{sleep}} + T_4 + 4d,$$

no node will switch from propose to recover before time $t_q + 3d$.

Again, we distinguish two cases. First assume that $t_q < t_{\text{sleep}} - T_1/\vartheta + T_2 + T_3 + 2d$, i.e., at time $t_q$ indeed a node switches to state accept. Due to Statement (iv) from the above list and the minimality of $t_q$, it follows that the respective node memorizes $n - 2f \geq f + 1$ nodes from $W$ in state propose that switched to propose at or after time $t_q$. These nodes must be in one of the states propose or accept during $[t_q, t_q + 3d]$. According to Statement (i) from above, thus all nodes still in ready will switch to propose by time $t_q + d$. By time $t_q + 2d$, all nodes in join will observe the at
least \(n-f\) nodes from \(W\) in one of the states \(\text{join}, \text{propropose}, \text{or accept}\), and hence switch to \(\text{propose}\). Another \(d\) time later, all nodes will have switched to \(\text{accept}\), i.e., \(t_q\) is indeed a quasi-stabilization point.

On the other hand, if \(t_q = t_{\text{sleep}} - T_1/\vartheta + T_2 + T_4 + 2d\), Statement (ii) from the above list gives that all nodes from \(W\) are in one of the states \(\text{join}, \text{propose}, \text{or accept}\) during \([t_q + d, t_q + 3d]\). Therefore, nodes will switch from \(\text{join} \) to \(\text{propose}\) and subsequently from \(\text{propose} \) to \(\text{accept}\) until time \(t_q + 3d\) as well.

It remains to check that in all cases, the obtained quasi-synchronization point \(t_q\) occurs no later than time \(t_g + R_1/\vartheta - 3d\). In Cases 1 and 2a, we have that

\[
t_q = t_{\text{propose}} \leq t_g + T + (4d + 5)d \leq t_g + \frac{R_1}{\vartheta} - 3d.
\]

In Case 2b, it holds that

\[
t_q \leq t_{\text{sleep}} - \frac{T_1}{\vartheta} + T_2 + T_4 + d \\
\leq t^+ - \frac{T_1}{\vartheta} + T_2 + T_4 + d \\
= t_g - \frac{2T_1}{\vartheta} + 2T_2 + 2T_4 + T_5 + 4d \\
\leq t_g + \frac{R_1}{\vartheta} - 3d.
\]

We conclude that indeed all nodes in \(W\) switch to \(\text{accept}\) within a window of less than 3\(d\) time before, at any node in \(W\), \(R_1\) expires and it leaves state \(\text{resync}\), concluding the proof.

Finally, putting together the established main theorems and Lemma 3.4 we deduce that the system will stabilize from an arbitrary initial state provided that a subset of \(n-f\) nodes remains coherent for a sufficiently large period of time.

**Corollary 4.16:** Let \(W \subseteq V\), where \(|W| \geq n-f\), and define for any \(k \in \mathbb{N}\)

\[
T(k) := (k+2)(\vartheta(R_2 + 3d) + 8(1 - \lambda)R_2 + d) + R_1/\vartheta.
\]

Then, for any \(k \in \mathbb{N}\), the proposed algorithm is a \((W, W^2)\)-stabilizing pulse synchronization protocol with skew 2\(d\) and accuracy bounds \((T_2 + T_3)/\vartheta - 2d\) and \(T_2 + T_4 + 7d\) stabilizing within time \(T(k)\) with probability at least \(1 - 2^{-k(n-f)}\). It is feasible to pick timeouts such that \(T(k) \in \mathcal{O}(kn)\) and \(T_2 + T_4 + 7d \in \mathcal{O}(1)\).

**Proof:** The satisfiability of Condition 3.3 with \(T(k) \in \mathcal{O}(kn)\) and \(T_2 + T_4 + 7d \in \mathcal{O}(1)\) follows from Lemma 3.4. Assume that \(t^+\) is sufficiently large for \([t^- + T(k) + 2d, t^+]\) to be non-empty, as otherwise nothing is to show. By definition, \(W\) will be coherent during \([t^- + T(k) + 2d, t^+]\) with \(t^- = t^- + \vartheta(R_2 + 3d) + 8(1 - \lambda)R_2 + d\). According to Theorem 4.10, there will be some good \(W\)-resynchronization point \(t_g \in [t^- + T(k) + (k+1)(\vartheta(R_2 + 3d) + 8(1 - \lambda)R_2 + d)]\) with probability at least \(1 - 2^{k(n-f)}\). If this is the case, Theorem 4.15 shows that there is a \(W\)-stabilization point \(t \in [t_g, t^- + T(k)]\). Applying Theorem 4.4, inductively, we derive that the algorithm is a \((W, W^2)\)-stabilizing pulse synchronization protocol with the bounds as stated in the corollary that stabilizes within time \(T(k)\) with probability at least \(1 - 1/2^{2k(n-f)}\).

**D. Late Joining and Fast Recovery**

An important aspect of combining self-stabilization with Byzantine fault-tolerance is that the system can remain operational when facing a limited number of transient faults. If the affected components stabilize quickly enough, this can prevent future faults from causing system failure. In an environment where transient faults occur according to a random distribution that is not too far from being uniform (i.e., one deals not primarily with bursts), the mean time until failure is therefore determined by the time it takes to recover from transient faults. Thus, it is of significant interest that a node that starts functioning according to the specifications again synchronizes as fast as possible to an existing subset of correct nodes. Moreover, it is of interest that a node that has been shut down temporarily, e.g. for maintenance, can join the operational system again quickly.

**Theorem 4.17:** Suppose there exists a node \(i\) in \(V\) and a set \(W \subseteq V\), \(|W| \geq n-f\), such that there is a \(W\)-stabilization point at some time \(t^-\) and \(W \cup \{i\}\) is coherent during \([t^-, t^- + (1 + 5/(2\vartheta))R_1]\). Then there is a \((W \cup \{i\})\)-stabilization point at some time \(t \in [t^-, t^- + (1 + 5/(2\vartheta))R_1]\).

**Proof:** Again, the proof is executed by distinguishing cases. W.l.o.g., we assume for the moment that \(W \cup \{i\}\) is coherent during \([t^-, \infty)\) and later show that indeed \(t \leq t^- + (1 + 5/(2\vartheta))R_1\).

**Case 1:** Node \(i\) does not switch to \(\text{supp} \rightarrow \text{resync}\) during \([t^-, t^- + R_1 + (1-1)T_1 + 2T_2 + 2T_4 + 18d]\). Thus, after \(R_1\) expires at the latest by time \(t^- + R_1 + d\), it will observe itself in \(\text{dormant}\) during \([t^- + R_1 + 2d, t^- + R_1 + (1-1)T_1 + 2T_2 + 2T_4 + 18d]\) and therefore not be (or observe itself) in state \(\text{join}\) during \([t^- + R_1 + 3d, t^- + R_1 + (1-1)T_1 + 2T_2 + 2T_4 + 18d]\). By Theorem 4.4, there is a \(W\)-stabilization point \(t_W \in [t^- + R_1 + (1-1)T_1 + 4d, t^- + R_1 + (1-1)T_1 + T_2 + T_4 + 9d]\). Subsequently, the nodes in \(W\) will switch to \(\text{sleep}\) during \([t_W + T_1/\vartheta, t_W + T_1 + 5d]\). Denote by \(t_{\text{sleep}}\) the minimum of the respective times. We apply Lemma 4.5 to \(W \cup \{i\}\). Thus, at time \(t_{\text{sleep}} + 2T_1 + 3d\), node \(i\) is either in \(\text{state recover}\) and will not leave until the next \(W\)-stabilization point (or it switches to \(\text{join}\)), or it is in state \(\text{sleep}\) and reset its timeout \(T_2\) at some time from \([t_W - \Delta_g + T_1/\vartheta - 4d, t_W + (3-1/\vartheta)T_1 + 8d]\).

**Case 1a:** Node \(i\) is in \(\text{recover}\) at time \(t_{\text{sleep}} + 2T_1 + 3d\). As it cannot switch to \(\text{join}\) until time \(t^- + R_1 + (1-1)T_1 + 2T_2 + 2T_4 + 18d\), it will stay in \(\text{recover}\) until the subsequent \(W\)-stabilization point \(t_W \in [t_W + (T_2 + T_3)/\vartheta, t^- + R_1 + (1-1)T_1 + 2T_2 + 2T_4 + 14d]\) (existing according to Theorem 4.4). By time \(t_W\), clearly timeout \((\text{recover}, \vartheta(2T_1 + 3d))\) has
expired at the node, as
\[ t'_W \geq t_W + \frac{T_2 + T_3}{\vartheta} > t_{\text{sleep}} + (\vartheta + 1)(2T_1 + 3d). \]

Because \( T_1/\vartheta \geq 4d \), i will observe all nodes from W in accept during \([t'_W + 3d, t_W + 4d]\). Hence it will switch to accept by time \( t'_W + 3d \), i.e., \( t'_W \) is a \( W \cup \{i\} \) quasi-stabilization point.

**Case 1b:** Node i is in sleep at time \( t_{\text{sleep}} + 2T_1 + 3d \). Denote by \( t'_W \) the W-stabilization point subsequently to \( t_W \) as in the previous case. As no node from W is observed in state accept or recover during \([t_s + 2T_1 + 3d, t'_W] \), and i resets its timeout \( T_2 \) no earlier than time \( t_W - \Delta_g + T_1/\vartheta - 4d \), it will not switch to recover before time \( \min\{t_W, t_W - \Delta_g + (T_1 + T_2 + T_3 + T_5)/\vartheta - 4d\} \) unless it switches to accept first. However, as it resets its propose and accept flags before switching to ready, it cannot switch to accept before at least \( f \) nodes from W switched to propose (unless switching to recover first). Moreover, by time \( t'_W \), it will already have switched to ready since
\[ t'_W \geq t_W + \frac{T_2 + T_3}{\vartheta} \geq t_W + \left(3 - \frac{1}{\vartheta}\right)T_1 + \frac{T_2}{\vartheta} + 8d. \]

Hence, reasoning analogously to the proof of Theorem 4.4, \( t'_W \) is in fact a \( W \cup \{i\} \)-stabilization point provided that i switches to accept instead of recover first. This in turn follows from the bound
\[
\begin{align*}
& t_W - \Delta_g + \frac{T_1 + T_2 + T_3 + T_5}{\vartheta} - 4d \\
& \geq t_W - \Delta_g + (T_1 + T_2 + T_4 + \frac{T_2 + T_3 - T_5}{\vartheta} - 4d \\
& \geq t_W - \Delta_g + (2\vartheta + 5)T_1 + 2T_2 + T_4 + 3d \\
& > t_W + T_2 + T_4 + 7d \\
& > t'_W + 2d,
\end{align*}
\]

where in the last step we used that \( t'_W < t_W + 2T_2 + T_4 + 5d \) according to Theorem 4.4. This shows that \( T_5 \) does not expire at i while it is in propose before time \( t'_W + 2d \). Hence, \( t'_W \) is a \( W \cup \{i\} \)-stabilization point.

**Case 2:** Node i switches to supp \( \rightarrow \) resync at a time \( t' \in [t^-, t + R_1 + (\vartheta - 1)T_1 + 2T_2 + 2T_3 + 18d] \). Denote by \( t_W \) and \( t'_W \) the maximal W-stabilization point smaller than \( t' \) and the minimal W-stabilization point larger than \( \max\{t', t_W + 2d\} \), which exist by Theorem 4.4. Denote by \( t_{\text{sleep}} \) the minimal time larger than \( t_W \) when a node from W switches to sleep. Analogously to Case 1b, \( t'_W \) is a \( W \cup \{i\} \)-stabilization point if i is in state sleep at time \( t_{\text{sleep}} + 2T_1 + 3d \). Hence, assume w.l.o.g. that i is in state recover or already switched to join by this time. Analogously to Case 1a, \( t'_W \) will be a \( W \cup \{i\} \)-quasi-stabilization point if it stays in recover until time \( t_W + 3d \). Therefore, w.l.o.g., i switches to join at some time during \((t', t'_W + 3d)\), implying that it will leave the state no later than time \( t'_W + 4d \) and switch to state accept by time \( t'_W + 5d \).

Now either i continues to execute the basic cycle and thus will, analogously to Case 1b, participate in the minimal W-stabilization point \( t'_W > t_W + 2d \), or it will switch to recover again. In the latter case, it cannot switch back to join until at least time \( t' + R_1/\vartheta \) because it needs to reset its join flags first, which happens upon switching to passive only. As we have that
\[
\begin{align*}
t' + R_1/\vartheta &\geq t' - \frac{2T_1}{\vartheta} + 2T_2 + 2T_3 + T_5 + 7d \\
&> t' - \frac{2T_1}{\vartheta} + 3T_2 + 3T_3 - T_6 + 7d \\
&> t' + 2T_2 + 2T_4 + 14d \\
&\geq t'_W + 4d,
\end{align*}
\]
i cannot leave state recover through join again before time \( t'_W + 4d \). Therefore, \( t'_W \) is a \( W \cup \{i\} \)-quasi-stabilization point, analogously to Case 1a.

We have shown that there is some \( W \cup \{i\} \)-quasi-stabilization at the latest by time
\[
t'_W \leq t' + 2T_2 + 2T_4 + 10d \\
\leq t^- + R_1 + (\vartheta - 1)T_1 + 4T_2 + 2T_4 + 28d
\]
in Case 2, while in Case 1 there is a quasi-stabilization point no later than time \( t^- + R_1 + (\vartheta - 1)T_1 + 2T_2 + 2T_4 + 18d \). By Theorem 4.4 this implies a \( W \cup \{i\} \)-stabilization point by time
\[
t^- + R_1 + (\vartheta - 1)T_1 + 5T_2 + 2T_4 + 23d < t^- + (1 + 5/2\vartheta)R_1,
\]
where the estimate is obtained analogously to the bound \( t' + R_1/\vartheta > t'_W + 4d \) shown above. This concludes the proof, as indeed there is a \( W \cup \{i\} \)-stabilization point no later than time \( t^- + (1 + 5/2\vartheta)R_1 \).

**V. Generalizations**

This section provides a few extensions of the core results derived in the previous section. In particular, we show that it is not necessary to map faulty channels to, for example, faulty nodes (thus rendering a non-faulty node effectively faulty in terms of results), that the algorithm can tolerate an even stronger adversary than defined in Section II without significant change of stabilization time, and that in many reasonable setting stabilization takes \( O(R_1) \) time only, even if there is no majority of non-faulty nodes that is already synchronized. With the exception of Corollary 5.6, we again follow [30] during this section.
A. Synchronization Despite Faulty Channels

Theorem 4.15 and our notion of coherency require that all involved nodes are connected by correct channels only. However, it is desirable that non-faulty nodes synchronize even if they are not connected by correct channels. To capture this, the notions of coherency and stability can be generalized as follows.

Definition 5.1 (Weak Coherency): We call the set $C \subseteq V$ weakly coherent during $[t^-, t^+]$, iff for any node $i \in C$ there is a subset $C_i \subseteq C$ that contains $i$, has size $n - f$, and is coherent during $[t^-, t^+]$.

In particular, if there are in total at most $f$ nodes that are faulty or have faulty outgoing channels, then the set of non-faulty nodes is (after some amount of time) weakly coherent.

Corollary 5.2: For each $k \in \mathbb{N}$ let $T^+(k) := T(k) - ((\lambda)(R_2 + 3d) + 8(1 - \lambda)R_2 + 4d)$, where $T(k)$ is defined as in Corollary 4.16. Suppose the subset of nodes $C \subseteq V$ is weakly coherent during the time interval $[t^-, t^+]$ then, with probability at least $1 - (f + 1)/2^{k(n - f)}$, there is a $C$-quasi-stabilization point $t \leq t^- + T^+(k) + T_2 + 4d + 5d$ such that the system is weakly $C$-coherent during $[t, t^+]$.

Proof: By the definition of weak coherency, every node in $C$ is in some coherent set $C_i \subseteq C$ of size $n - f$. Hence, for any such $C_i$ it holds that we can cover all nodes in $C$ by at most $1 + V_1 \setminus C_i \leq f + 1$ coherent sets $C_1, \ldots, C_{f + 1} \subseteq C$. By Corollary 4.16 and the union bound, with probability at least $1 - (f + 1)/2^{k(n - f)}$, for each of these sets there will be at least one stabilization point during $[t^-, t^- + T^+(k) - (T_2 + T_2 + 4d + 5d)]$. Assuming that this is indeed true, denote by $t_{i_0} \in [t^-, t^- + T^+(k) - (T_2 + T_2 + 4d + 5d)]$ the time

$$
\max_{i \in \{1, \ldots, f + 1\}} \{ \max \{ t \leq t^- + T^+(k) - (T_2 + T_2 + 4d + 5d) \} \mid t \text{ is a } C_i \text{-stabilization point} \},
$$

where $i_0 \in \{1, \ldots, f + 1\}$ is an index for which the first maximum is attained and $t_{i_0}$ is the respective maximal time, i.e., $t_{i_0}$ is a $C_{i_0}$-stabilization point.

Define $t_{i_0}^j \in (t_{i_0} + 2d, T^- + T^+(k))$ to be minimal such that it is another $C_{i_0}$-stabilization point. Such a time must exist by Theorem 4.4. Since the theorem also states that no node from $C_{i_0}$ switches to state accept between $[t_{i_0} + 2d, t_{i_0}^j)$ and $C_{i_0} \cap C_i \neq \emptyset$, there can be no $C_i$-stabilization point during $(t_{i_0} + 2d, t_{i_0}^j - 2d)$ for any $i \in \{1, \ldots, f + 1\}$. Applying the theorem once more, we see that there are also no $C_i$-stabilization points during $(t_{i_0}^j + 2d, t_{i_0}^j + (T_2 + T_2 + 4d)/2 - 2d$ for any $i \in \{1, \ldots, f + 1\}$. On the other hand, the maximality of $t_{i_0}$ implies that every $C_i$ had a stabilization point by time $t_{i_0}$. Applying Theorem 4.4 to the latest stabilization point until time $t_{i_0} + T_2 + T_2 + 4d$. We have that

$$
2(T_2 + T_3) - 2d \geq T_2 + T_3 + T_5 \geq T_2 + T_2 + 5d,
$$

i.e., all $C_i$ have stabilization points within a short time interval of $(t_{i_0}^j - 2d, t_{i_0}^j + 2d)$. Arguing analogously about the previous stabilization points of the sets $C_i$ (which exist because $t_{i_0}$ is maximal), we infer that all $C_i$ had their previous stabilization point during $(t_{i_0} - 2d, t_{i_0} + 2d)$.

Now suppose $t_a$ is the minimal time in $(t_{i_0} - 2d, t_{i_0} + 2d)$ when a node from $C$ switches to accept and this node is in set $C_i$ for some $i \in \{1, \ldots, f + 1\}$. As usual, there must be at least $f + 1$ non-faulty nodes from $C_i$ in state propose at time $t_a$ and by time $t_a + d$, all nodes from $C_i$ will be observed in either of the states propose or accept. As $|C_i \cap C_j| \geq f + 1$ for any $j \in \{1, \ldots, f + 1\}$, all nodes in $C_j$ will observe at least $f + 1$ non-faulty nodes in states propose or accept at times in $(t_a, t_a + 2d)$. We have that $t_a \geq t_{i_0} + (T_2 + T_3)/d - 2d$ according to Theorem 4.4. As no nodes switched to state accept during $(t_{i_0} + 2d, t_a)$ and none of them switch to state recover (cf. Theorem 4.4), for any $j$ we can bound

$$
t_a + d \geq t_j + d + \frac{T_2 + T_3}{d} \geq t_j - 3d + \frac{T_2 + T_3}{d} \geq t_j + 2d + 3d.
$$

that all nodes from $C_j$ are in one of the states ready, propose, or accept at time $t_a + d$. Hence, they will switch from ready to propose if they still are in ready before time $t_a + 2d$. Less than $d$ time later, all nodes in $C_j$ will memorize all nodes in $C_j$ in state propose and therefore switch to accept if not done so yet. Since $j$ was arbitrary, it follows that $t_a$ is a $C$-quasi-stabilization point.

Corollary 5.3: Suppose $C \subseteq V$ is weakly coherent during $[t^-, t^+]$ and $t \in [t^-, t^- + (T_2 + T_2 + 4d)]$ is a $C$-quasi-stabilization point. Then

(i) all nodes from $C$ switch to accept exactly once within $[t, t + 3d]$;

(ii) there will be a $C$-quasi-stabilization point $t' \in [t + (T_2 + T_3)/d, t + T_2 + T_2 + 4d]$ satisfying that no nodes switch to accept in the time interval $[t, t + 3d]$;

(iii) and each node s’s, $i \in C$, main state machine (Figure 1) is metastability-free during $[t + 4d, t' + 4d]$.

Proof: Analogously to the proofs of Theorem 4.4 and Corollary 5.2.

We point out that one cannot get stronger results by the proposed technique. Even if there are merely $f + 1$ failing channels, this can e.g. effectively render a node faulty (as it may never see $n - f$ nodes in states propose or accept) or exclude the existence of a coherent set of size $n - f$ (if the channels connect $f + 1$ disjoint pairs of nodes, there can be no subset of $n - f$ nodes whose induced subgraph contains correct channels only). Stronger resilience
to channel faults would necessitate to propagate information over several hops in a fault-tolerant manner, imposing larger bounds on timeouts and weaker synchronization guarantees.

Combination of Corollary 5.2 and Corollary 5.3 finally yields:

**Corollary 5.4:** Let \( C \subseteq V \) be such that, for each \( i \in C \), there is a set \( C_i \subseteq C \) with \( |C_i| = n - f \), and let \( E = \bigcup_{i \in C} C_i \). Then, for any \( k \in \mathbb{N} \), the proposed algorithm is a \((C, E)\)-stabilizing pulse synchronization protocol with skew 3d and accuracy bounds \( (T_2 + T_3)/\vartheta - 3d \) and \( T_2 + T_4 + 8d \) stabilizing within time \( T(k) + T_2 + T_4 + 5d \) with probability at least \( 1 - (f + 1)/2^{k(n-f)} \).

**Proof:** Analogously to the proof of Corollary 4.10. ■

**B. Stronger Adversary**

So far, our analysis considered a fixed set \( C \) of coherent (or weakly coherent) nodes. But what happens if whether a node becomes faulty or not is not determined upfront, but depends on the execution? Phrased differently, does the algorithm still stabilize quickly with a large probability if an adversary may “corrupt” up to \( f \) nodes, but may decide on its choices as time progresses, fully aware of what happened so far? Since we operate in a system where all operations take positive time, it might even be the case that a node might fail just when it is about to perform a certain state transition, and would not have done so if the execution had proceeded differently. Due to the way we use randomization, this however makes little difference for the stabilization properties of the algorithm.

**Corollary 5.5:** Suppose at every time \( t \), an adversary has full knowledge of the state of the system up to and including time \( t \), and it might decide on in total up to \( f \) nodes (or all channels originating from a node) becoming faulty at arbitrary times. If it picks a node at time \( t \), it fully controls its actions after and including time \( t \). Furthermore, it controls delays and clock drifts of non-faulty components within the system specifications, and it initializes the system in an arbitrary state at time 0. For any \( k \in \mathbb{N} \), define \( t_k \) as

\[
(k+3)(\vartheta(R_2+3d)+8(1-\lambda)(R_2+d)+R_1/\vartheta+T_2+T_4+5d).
\]

Then the set of all nodes that remain non-faulty until time \( t_k \) reaches a quasi-stabilization point during \([\hat{E}_3, t_k]\) with probability at least

\[
1 - (f + 1)e^{-k(n-f)/2}.
\]

Moreover, at any time \( t \geq \hat{E}_3 \), the set of nodes that are non-faulty at time \( t \) is coherent.

**Proof:** The last statement of the corollary holds by definition.

We need to show that Theorem 4.10 holds for the modified time interval \([\hat{E}_3, (k+3)\hat{E}_3]\) with the modified probability of at least \( 1 - e^{-k(n-f)/2} \). If this is the case, we can proceed as in Corollaries 5.2 and 5.3.

We start to track the execution from time \( \hat{E}_3 \). Whenever a non-faulty node switches to state \( \text{init} \) at a good time, the adversary must corrupt it in order to prevent subsequent deterministic stabilization. In the proof of Theorem 4.10 we showed that for any non-faulty node, there are at least \( k+1 \) different times during \([\hat{E}_3, (k+3)\hat{E}_3]\) when it switches to \( \text{init} \) that have an independently by 1/2 lower bounded probability to be good. Since Lemma 4.9 holds for any execution where we have at most \( f \) faults, the adversary corrupting some node at time \( t \) affects the current and future trials of that node only, while the statement still holds true for the non-corrupted nodes. Thus, the probability that the adversary may prevent the system from stabilizing until time \( t_k \) is upper bounded by the probability that \((k+1)(n-f)\) independent and unbiased coin flips show \( f \) or less times tail.

Chernoff’s bounds states for the random variable \( X \) counting the number of tails in this random experiment that for any \( \delta \in (0, 1) \),

\[
P[X < (1 - \delta)|E[X]] < \left(\frac{e^{-\delta}}{(1 - \delta)^{1-\delta}}\right)^{E[X]} < e^{-\delta E[X]}.
\]

Inserting \( \delta = k/(k+1) \) and \( E[X] = (k+1)(n-f)/2 \), we see that the probability that

\[
P[X \leq f] \leq P[X < (n-f)/2] < e^{-k(n-f)/2},
\]

as claimed. ■

**C. Constant-Time Stabilization**

Up to now, we considered worst-case scenarios only. In practice, it is likely that faulty nodes show not entirely arbitrary behavior. In particular, they might still be partially following the protocol, not exhibit a level of coordination that could only be achieved by a powerful central instance, or not be fully aware of non-faulty nodes states. Moreover, it is unlikely that at the time when a majority of the nodes becomes non-faulty, all their timeouts \( R_2 \) and \( R_3 \) have been reset recently. In such settings, stabilization will be much easier and therefore be achieved in constant time with a large probability. It is difficult, however, to name simple conditions that cover most reasonable cases. Generally speaking, once (randomized) timeouts of duration \( R_2 \) or \( R_3 \) are not “ messed up” at non-faulty nodes anymore, faulty channels and nodes need to collaborate in an organized manner in order to prevent stabilization for a large time period. We give a few examples in the following corollary.

**Corollary 5.6:** Suppose \( W \subseteq V \), where \(|W| \geq n - f \), satisfies that for each \( i \in W \), all (randomized) timeouts of duration \( R_2 \) or \( R_3 \) are correct during \([t^- , t^+], \) and the node is non-faulty during \([t^- + \vartheta(3(R_2 + 3d) + (2(8(1 - \lambda)R_2 + d)), t^+], \)

Moreover, channels between nodes in \( W \) are correct during \([t^- + \vartheta(3(R_2 + 3d) + (2(8(1 - \lambda)R_2 + d)), t^+], \)

and did not insert \( \text{init} \) signals that have not been sent during \([t^- , t^+ + \vartheta(3(R_2 + 3d) + (2(8(1 - \lambda)R_2 + d))] \) or delay them by more than \( R_1 \) time. Define \( \hat{t}^- := t^- + \vartheta(3(R_2 + 3d) + \)
2(8(1 − λ)R_2 + d)) + R_1 + d. Moreover, assume that one of the following statements holds during \([\hat{t}^-, \hat{t}^+]\).

(i) Nodes in \(V \setminus W\) switch to \(init\) at times that are independently distributed with probability density at most \(\mathcal{O}(1/(R_1n^2))\), and channels from \(V \setminus W\) to \(W\) do not generate \(init\) signals on their own (or delay \(init\) signals from before \(\hat{t}^-\) more than \(R_1\) time).

(ii) Channels from \(V \setminus W\) to \(W\) switch to \(init\) at times that are independently distributed with probability density at most \(\mathcal{O}(1/(R_1n^2))\).

(iii) Channels from \(V \setminus W\) to \(W\) switch to \(init\) obliviously of the history of signals originating at nodes in \(W\) and do not know the time \(\hat{t}^-\).

If \(t^+ \in \hat{t}^- + \Omega(kR_1), k \in \mathbb{N}\), then there is a \(W\)-stabilization point during \([\hat{t}^-, \hat{t}^- + \mathcal{O}(kR_1)]\) with probability at least \(1 - 2^{-O(k)}\).

**Proof:** In Theorems 4.4 and 4.15 we showed that stabilization is deterministic once a good resynchronization point occurs. The notion of coherency essentially states that at non-faulty nodes, each timeout expired at least once and has not been reset again because of incorrect observations on other non-faulty nodes’ states until the set is considered coherent (cf. Lemma 4.3). Subsequently, the respective nodes are non-faulty and the channels connecting them correct. This is true by the prerequisites of the corollary, which essentially state respective conditions on timeouts \(R_2\) and \(R_3\) explicitly, while rephrasing the conditions for coherency for the remaining timeouts (note that \(R_1\) is the largest timeout except for \(R_2\) and \(R_3\)).

Moreover, the time span during which \(R_2\) and \(R_3\) behave and are observed regularly is large enough for \(R_3\) to expire twice and additional \(R_2 + 3d\) time to pass. This accounts for the fact that in the proof of Theorem 4.10 we essentially first wait until \(R_3\) expires once (so the adversary has no useful information on the timeout at the respective node anymore) and then consider the subsequent time(s) when it expire(s). The proof then exploits that non-faulty nodes timeout \(R_3\) will expire at roughly independently uniformly distributed points in time. Therefore, unless faulty nodes or channels interfere, the statement of the corollary holds.

Hence, we need to show that for any of the three conditions, there is not too much meddling from outside \(W\). For Conditions (i) or (ii), we see that the probability that there are no \(init\) signals on channels from \(V \setminus W\) to \(W\) at all for any time span of length \(\mathcal{O}(R_3)\) is at least constant, regardless of the time interval considered. Regarding Condition (iii), recall that Theorem 4.10 essentially shows that whatever the strategy of the adversary, the expected number of good \(W\)-resynchronization points during a fixed time interval (where \(W\) is coherent) is linear in the size of the interval divided by \(R_3\) if the interval is sufficiently large. Since the adversary is oblivious of the current time in relation to \(\hat{t}^+\) and the state of \(W\), the statement that for any strategy of the adversary the amortized number of good stabilization points per \(R_1\) time is constant yields the claim of the lemma.

We remark that this observation is particularly interesting as the core routine of the algorithm is independent of the resynchronization routine after stabilization. If at some time \(W\) becomes subject to a large number of faults resulting in loss of synchronization, however the resynchronization routine still works properly, it is very likely that \(W\) will recover within \(\mathcal{O}(1)\) time (provided \(R_1 \in \mathcal{O}(1)\)). On the other hand, if the resynchronization routine fails in the sense that a majority of the nodes suffers from faulty timeouts \(R_2\) or \(R_3\), or communication is faulty between too many nodes, this will not affect the core routine unless too many components related to it fail as well.

**VI. The FATAL\(^+\) Protocol**

The synchronized pulses established by the FATAL pulse synchronization algorithm could in principle serve as the local clock signals provided to the application layer of the SoC\(^{21}\). However, just using the FATAL protocol in this way would result in a very low clock frequency: Despite the fact that the time between pulses is \(\Theta(d)\) (if the timeouts are chosen accordingly) and thus asymptotically optimal, the actual clock speed would be several orders of magnitude below the upper bound resulting from \([42]\), due to the large implied constants. Moreover, the system model introduced in Section II assumes that delays may vary arbitrarily between 0 and \(d\), with \(d\) also covering the fairly complex implementation of communicating the main algorithm’s states (see Section VII-B). By contrast, pure wire delays of the communication channels between different nodes are much smaller and also vary within a smaller range.

This section contains an extension of FATAL, termed FATAL\(^+\), which overcomes these limitations. In a nutshell, it consists of adding a fast non-self-stabilizing, Byzantine-tolerant algorithm termed quick cycle to FATAL, which generates exactly \(M > 1\) fast clock ticks between any two pulses at a correct node after stabilization.

**The Quick Cycle Algorithm**

Consider a system of \(n\) nodes, each of which runs the FATAL pulse synchronization protocol. Additionally, each node is equipped with an instance of the quick cycle state machine depicted in Figure 5. The interface between the quick cycle algorithm and the underlying FATAL pulse synchronization protocol is by means of two signals only, one for each direction of the communication: (i) The quick cycle state machine generates the NEXT signal by which it (weakly) influences the time between two successive

\(^{21}\)In order to establish a consistent global tick numbering (needed for establishing a global notion of time across different clock domains) of arbitrarily large bounded clocks, a self-stabilizing digital clock synchronization algorithm like the one from [25] can be employed. Implementing such algorithms in SoCs is part of our future work and thus outside the scope of this paper, however.
pulses generated by FATAL, and (ii) it observes the state of the \((T_2^+, \text{accept})\) signal, which signals the expiration of an additional timer added to the FATAL protocol. The timer is coupled to the state \text{accept} of FATAL, in which the pulse synchronization algorithm generates a new pulse. The signal’s purpose is to enforce a consistent reset of the quick cycle state machine once FATAL has stabilized.

Essentially, the quick cycle state machine is a copy of the outer cycle of Figure 2 that is stripped down to the minimum. However, an additional mechanism is introduced in order to ensure stabilization, namely, some coupling to the \text{accept} state of the main algorithm: Whenever a pulse is generated by FATAL, we require that all nodes switch to the \text{accept} state unless they already occupy that state. This is easily achieved by incorporating the state of the expiration signal of the additional FATAL timer \((T_2^+, \text{accept})\) in the guards of Figure 5. Since pulses are synchronized up to the skew \(\Sigma\) of the pulse synchronization routine, it follows that all nodes switch to \text{accept} within a time window of \(\Sigma + 2d\). Subsequently, all nodes will switch to state \text{ready} before the first one switches to \text{propose} provided that \(T_3^+\) is sufficiently large, and the condition that \(f + 1\) \text{propose} signals trigger switching to \text{propose} guarantees that all nodes switch to \text{accept} in a tightly synchronized fashion.

One element that is not depicted explicitly in Figure 5 is that nodes increase an integer cycle counter by one whenever they switch to \text{accept}. The counter is reset to zero whenever \((T_2^+, \text{accept})\) expires, i.e., shortly after a pulse generated by the underlying pulse synchronization algorithm. The algorithm makes sure that, once the compound algorithm stabilized, these resets never happen when the counter holds a non-zero value. The counter operates mod \(M \in \mathbb{N}\), where \(M\) is large enough so that at least roughly \(T_2 + T_3\) and at most \((T_2 + T_3)/\vartheta\) time passed since the most recent pulse when it reaches \(M \equiv 0\) again. Whenever the counter is set to 0, node \(i \in V\) will set its \text{NEXT} signal to 1 and switch it back to 0 at once (thus raising the respective \text{NEXT} memory flag of the main algorithm). Thus, by actively triggering the next pulse, we ensure that a pulse does not occur at an inconvenient point in time: When the system has stabilized, exactly \(M\) switches to \text{accept} of the quick cycle algorithm occur between any two consecutive pulses at a correct node. As these switches occur also synchronously at different nodes, it is apparent that the quick cycle state machine in fact implements a bounded-size synchronized clock.

To derive accurate bounds on the skew of the protocol, we need to state the involved delays more carefully.

**Definition 6.1 (Refined Delay Bounds):** The state of the quick cycle algorithm is communicated via separate channels \(S_{i,j}^+\), with \(i, j \in V\), whose delays vary within \(d_{\min}^+\) and \(d_{\max}^+\) in order to be considered correct during \([t^-, t^+]\). State transitions of the quick cycle state machine, resets of its timeouts, and clearance of its memory flags take at most \(d_{\max}^+\) time.

Setting \(\Sigma^+ := 2d_{\max}^+ - d_{\min}^+\), we assume that the following timing constraints hold:

\[
T_1^+ \geq \vartheta(T_2^+ + \Sigma^+ + 3d + d_{\max}^+) \\
T_2^+ \geq \vartheta(3d + 3d_{\max}) \\
T_3^+ \geq \vartheta(T_1^+ + d_{\max}^+) \\
M \in \left[\frac{\vartheta(T_2 + T_3 + 3d + d_{\max}^+)}{\vartheta}, \frac{T_2 + T_3 + 3d + d_{\max}^+}{\vartheta} \right]
\]

It follows from Lemma 3.4 that it is always possible to pick appropriate values for the timeouts and \(M\). Note, however, that choosing \(M \in \omega(1)\) requires that \(T_2 + T_3 \in \omega(1)\), resulting in a superlinear stabilization time. More precisely, the stabilization time of FATAL is, given \(M\) and minimizing the timeouts under this constraint, in \(O(Mn)\). As mentioned previously, this limitation can be overcome by employing a digital clock synchronization such as [22].

We now prove the correctness of the FATAL protocol.

**Theorem 6.2:** Let \(W \subseteq V\), where \(|W| \geq n - f\), and define \(T(k)\), for \(k \in \mathbb{N}\), as in Corollary 4.16. Then, for any \(k \in \mathbb{N}\), the FATAL protocol is a \((W, W^2)\)-stabilizing pulse synchronization protocol (where \text{accept} is the “pulse” state) with skew \(\Sigma^+\) and accuracy bounds \((T_1^+ + T_3^+) / \vartheta - \Sigma^+\) and \(T_1^+ + T_3^+ + \Sigma^+ + 3d_{\max}^+\). It stabilizes within time \(T(k) + T_1^+ + T_3^+ + \Sigma^+ + 3d + 3d_{\max}^+\) with probability at least \(1 - 2^{-k(n-f)}\). Moreover, the cycle counters increase by exactly one mod \(M\) at each pulse, within a time window of \(\Sigma^+\), and both the quick cycle state machine and the cycle counters are metastability-free once the protocol stabilized and remains fault-free in \(W\).

**Proof:** Assume that nodes in \(W \subseteq V\), where \(|W| \geq n - f\), are non-faulty and channels between them are correct during \([t^-, t^+]\), where \(t^+ \geq t^- + T(k) + T_1^+ + T_3^+ + \Sigma^+ + 3d + 3d_{\max}^+\). According to Corollary 4.16 with probability at least \(1 - 2^{-k(n-f)}\), there exists a time \(t_0 \in [t^-, t^- + T(k)]\) such that all nodes in \(W\) switch to \text{accept} within \([t_0, t_0 + 2d]\), and they will continue to switch to \text{accept} regularly in a synchronized fashion until at least \(t^+\). For the remainder of the proof, we assume that such a time \(t_0\) is given; from here we reason deterministically.
The skew bound is shown by induction on the $k$-th consecutive quick cycle pulse, where $k \in \mathbb{N}$, generated after the stabilization time $t_0$ of the FATAL algorithm. Note that the time for which we are going to establish that the compound algorithm stabilizes is $t_1 > t_0$; here we denote for $k \geq 1$ by $t_k$ the time when the first node from $W$ switches to accept$^+$ for the $k$th time after $t_0 + 3d$, i.e., the beginning of the $k$th pulse of FATAL$^+$ that we prove correct. W.l.o.g. we assume that $t^+ = \infty$; otherwise, all statements will be satisfied until $t^+$ only (which is sufficient).

To prove the theorem, we are going to show by induction on $k \in \mathbb{N}$ that

(i) $t_1 \in [t_0 + (T_2^+ + T_3^+) / \vartheta, t_0 + T_1^+ + T_3^+ + \Sigma^+ + 3d + 3d_{\text{max}}]$,

(ii) if $k \geq 2$, $t_k \leq t_{k-1} + T_1^+ + T_3^+ + \Sigma^+ + 3d_{\text{max}}$,

(iii) if $k \geq 2$, $t_k \geq t_{k-1} + (T_1^+ + T_3^+) / \vartheta$,

(iv) \( \forall i \in W : \) i switches to accept$^+$ for the $k$th time after \( t_0 + 3d \) during \( [t_{k-1}, t_k + \Sigma^+] \),

(v) if $k \geq M$, for \( l := [k/M] \), \( \forall i \in W : \) i switches to accept$^+$ for the $l$th time after $t_0 + 3d$ during \( [t_{Ml}, t_{Ml} + \Sigma^+ + 3d] \),

(vi) \( \forall i \in W : \) node $i$'s cycle counter switches from $k - 1 \mod M$ to $k \mod M$ at some time from \( [t_{lk}, t_k + \Sigma^+] \), and

(vii) if $k \geq 2, \forall i \in W : \) node $i$'s cycle counter changes its state exactly once during \( [t_{lk-1}, t_{lk}] \).

In particular, the protocol is a pulse synchronization protocol with the claimed bounds on skew, accuracy, and stabilization time. Proving these properties will also reveal that quick cycle is metastability-free after time $t_1$.

To anchor the induction at $k = 1$, we need to establish Statement (i) as well as Statements (iv) and (vi) for $k = 1$; the remaining statements are empty for $k = 1$.

Recall that any node $i \in W$ switches to accept during \([t_0, t_0 + 2d]\). Hence, during

\[
\left[ t_0 + 3d, t_0 + \frac{T_2^+}{\vartheta} \right] \subseteq \left[ t_0 + 3d, t_0 + 3d + 3d_{\text{max}}^+ \right],
\]

at no node in $W$, \((T_2^+, \text{accept})\) is expired, implying that all nodes in $W$ are in state accept$^+$ during \([t_0 + 3d + 2d_{\text{max}}^+, t_0 + 3d + 3d_{\text{max}}^+]\). Note that each node will reset its cycle counter to 0 when \((T_2^+, \text{accept})\) expires, i.e., after having completed its transition to accept$^+$.

The above bound shows that at the minimal time after $t_0 + 3d$ when a node in $W$ switches to ready$^+$, it is guaranteed that no node is observed in propose$^+$ until the minimal time $t_p \geq t_0 + 3d$ when a node in $W$ switches to propose$^+$. Moreover, at any node switching to state ready$^+$ timeout \((T_2^+, \text{accept})\) must be expired, implying that the node may not switch from ready$^+$ to propose$^+$ due to this signal until it switches to accept$^+$ again. Recall that nodes set their NEXT signals to 1 only briefly when their cycle counters are set to 0. Hence, for each such node in $W$, this signal is observed in state 0 from the time when \((T_2^+, \text{accept})\) expires until (a) at least time $t_M$ or (b) the time the node is forced by a switch to accept to set its counter to 0, whatever is earlier. Examining the main state machine, it thus can be easily verified that no node in $W$ may switch from ready$^+$ to propose$^+$ because \((T_2^+, \text{accept})\) = 0 before (a) time $t_M$ or (b) time

\[
t_0 + \frac{T_2^+ + T_4}{\vartheta} \geq t_0 + M(T_1^+ + T_3^+ + 3d_{\text{max}}^+) + 3d
\]

is reached. We obtain:

(P1) No node in $W$ observes \((T_2^+, \text{accept})(t) = 0\) at some time $t \in [t_0 + 3d, \min\{t_M, t_0 + M(T_1^+ + T_3^+ + 3d_{\text{max}}^+) + 3d\}]$ when it is not in state accept$^+$.

Considering that any node $i \in W$ will switch to ready$^+$ once both $T_1^+$ and $T_2^+$ expired and subsequently to propose$^+$ at the latest when $T_3^+$ expires (provided that it does not switch back to accept$^+$ first), it follows that by time

\[
t_0 + 3d + \max\{T_1^+ + d_{\text{max}}^+, T_3^+\} + T_3^+ + 2d_{\text{max}}^+ \geq t_0 + T_1^+ + T_3^+ + 3d_{\text{max}}^+ + 3d
\]

each node in $W$ must have been observed in propose$^+$ at least once. On the other hand, as we established that nodes do not observe nodes in $W$ in state propose$^+$ when switching to ready$^+$ at or after time $t + 3d$ before the first node in $W$ switches to propose$^+$, it follows that until time

\[
t_0 + \frac{T_2^+ + T_3^+}{\vartheta} \geq t_0 + 3d + T_1^+ + 2d_{\text{max}}^+
\]

nodes in $W$ will have at most $|V \setminus W| \leq f$ of their propose$^+$ flags in state 1, and their timeout $T_3^+$ did not expire yet. Thus, by (P1), the first node in $W$ that switches to propose$^+$ after $t_0 + 3d$ must do so at time $t_p \geq t_0 + 3d + T_1^+ + 2d_{\text{max}}^+$.

Recall that $t_1$ is the minimal time larger than $t_0 + 3d$ when a node in $W$ switches to state accept$^+$. By (35) and since $|W| \geq n - f$, we have that each node in $W$ observes at least $n - f$ nodes in propose$^+$ by time $t_0 + T_1^+ + T_3^+ + 3d + 3d_{\text{max}}^+$, and thus

\[
t_1 \leq t_0 + T_1^+ + T_3^+ + 3d + 3d_{\text{max}}^+
\]

Moreover, we can trivially bound

\[
t_1 \geq t_p \geq t_0 + (T_2^+ + T_3^+)/\vartheta
\]

From (38) and (39) it follows that $t_1$ satisfies Statement (i) of the claim.

Since at time $t_1$ there is a node $i \in W$ switching from propose$^+$ to accept$^+$, (P1) implies that it must memorize at least $n - 2f \geq f + 1$ nodes in $W$ in state propose$^+$, which must have switched to this state during \([t_p, t_1 - d_{\text{min}}^+]\). By the above considerations regarding the reset of the propose$^+$ flags, this yields that all nodes in $W$ will memorize at least $f + 1$ nodes in state propose$^+$ by time $t_1 + d_{\text{max}}^+ - d_{\text{min}}^+$ and
thus switch to $propose^+$ (if they have not done so yet). It follows that by time $t_1 + 2d_{max}^+ - d_{min}^+$, all nodes in $W$ memorize at least $|W| \geq n - f$ nodes in $propose^+$ and therefore switched to $accept^+$. Hence, we successfully established Statement (iv) of the claim for $k = 1$. Statement (vi) follows for $k = 1$, as the cycle counters have been reset to zero at the expiration of $(T_2^+, accept)$ and are increased upon the subsequent state transition to $accept^+$. Note that Statements (ii), (iii), (v), and (vii) trivially hold.

We now perform the induction step from $k \in \mathbb{N}$ to $k + 1$. Assume that Statements (ii) to (vii) hold for all values smaller or equal to $k$; Statement (i) only applies to $k = 1$ and was already shown. Define $l := \lfloor k/M \rfloor \geq 0$. Thus, if we can show Statement (ii) for $k + 1$, we may infer that

$$t_{k+1}^{(i),(ii)} \leq t_{MI} + (k + 1 - M)(T_1^+ + T_3^+ + \Sigma^+ + 3d_{max}^+) + 3d \leq t_{MI} + M(T_1^+ + T_3^+ + \Sigma^+ + 3d_{max}^+) + 3d \leq t_{MI} + \frac{T_2 + T_4}{\vartheta}. \quad (40)$$

In case $l = 0$, it holds that $k < M$ and we may deduce (P1) by the same arguments as in the induction basis.

In case $l \geq 1$, we use Statement (v) for value $k$, and, by analogous arguments as in the induction basis, deduce that at no node in $W$, $(T_2^+, accept)$ is expired during $[t_{MI} + 3d, t_{MI} + 3d + 2d_{max}^+)$, implying that all nodes in $W$ are in $accept^+$ during that time. Repeating the reasoning of the induction basis before (P1) with $l_0$ replaced by $t_{MI}$, $t_1$ replaced by $t_{MI}$, and $T_{MI+1}$ replaced by $T_{MI+M}$ shows that:

(PI'). No node in $W$ observes $(T_2^+, accept)(t) = 0$ at some time $t \in [t_{MI} + 3d, \min\{t_{MI+1}, t_{MI} + M(T_1^+ + T_3^+ + 3d_{max}^+) + 3d\})$ when it is not in state $accept^+$.

Since further $t_{MI+M} \geq t_{k+1}$ by definition of $l$, we obtain from (PI') that no node $i \in W$ will memorize $next_i = 1$ earlier than time $\min\{t_{k+1}, t_{MI} + M(T_1^+ + T_3^+ + 3d_{max}^+) + 3d\}$ again by reasoning analogously to the induction base.

By Statement (iv) for the value $k$, we know that each node $i \in W$ switches to $accept^+$ during $[t_k, t_k + \Sigma^+]$. In particular, $i$ will increase its cycle counter at the respective time, i.e., Statement (vi) for $k + 1$ follows at once if we establish Statement (vii) for $k + 1$. As Statement (iv) for the value $k$ together with Statement (ii) for $k + 1$ imply that each node switches to $accept^+$ exactly once during $[t_k, t_{k+1})$, Statement (vii) for $k + 1$ follows, provided that we can exclude that the counter is reset to 0, due to $(T_2^+, accept)$ expiring, at a time when it holds a non-zero value.

We now show that this never happens. By Statement (v) for value $k$ each node $i \in W$ switches to $accept$ during

$$[t_{MI}, t_{MI} + \Sigma^+ + 2d) \quad (42)$$

and this time is unique during $[t_{MI}, t_{k+1})$ due to (40).

Because of (42), a node in $W$ will reset its timeout $(T_2^+, accept)$ during

$$[t_{MI}, t_{MI} + \Sigma^+ + 2d), \quad (43)$$

and $(T_2^+, accept)$ will expire within

$$[t_{MI} + T_2^+/\vartheta, t_{MI} + T_2^+ + \Sigma^+ + 3d_{max}^+]$$

Thus, no node in $W$ leaves state $accept^+$ after switching there for the $(M)_th$ time after $t_0 + 3d$ before observing that $(T_2^+, accept)$ is reset and expires again. In particular, this shows that the counters are only reset to 0 at times when they are 0 anyway. Granted that Statement (ii) holds for $k + 1$, Statement (vii) for $k + 1$ follows.

Next, we establish Statements (ii) to (iv) for $k + 1$. We reason analogously to the case of $k = 1$, except that we have to revisit the conditions under which state $accept^+$ is left. As we have just seen, nodes switch from $accept^+$ to $ready^+$ upon $T_1^+$ expiring. Thus, as all nodes in $W$ switch to $accept^+$ during $[t_k, t_k + \Sigma^+]$, they switch to $ready^+$ within the time window $[t_k + T_1^+ / \vartheta, t_k + T_1^+ + \Sigma^+ + d_{max}^+]$. By time

$$t_k + T_1^+/\vartheta \geq t_k + \Sigma^+ + d_{max}^+,$$

all nodes in $W$ will be observed in $accept^+$ (and therefore not in $propose^+$), together with (P1') preventing that the first node in $W$ that (directly) switches from $ready^+$ to $propose^+$ afterwards does so without $T_1^+$ expiring first.

More precisely, according to (P1') no node in $W$ observes $(T_2^+, accept)$ to be zero until time $\min\{t_{k+1}, t_{MI} + M(T_1^+ + T_3^+ + 3d_{max}^+) + 3d\}$. As showing Statement (ii) for $k + 1$ will imply inequality (42), we can w.l.o.g. disregard the case that $t_{MI} + M(T_1^+ + T_3^+ + 3d_{max}^+) + 3d < t_{k+1}$ in the following. Thus, each node $i \in W$ will be observed in state $propose^+$ no later than time $t_k + T_1^+ + T_3^+ + \Sigma^+ + d_{max}^+$. As argued for $k = 1$, it follows that indeed $t_{k+1} \leq t_k + T_1^+ + T_3^+ + \Sigma^+ + 3d_{max}^+$, i.e., Statement (ii) for $k + 1$ holds. Further each node $i$ switches to $accept^+$ for the $(k + 1)th$ time after $t_0 + 3d$ during time $[t_{k+1}, t_{k+1} + \Sigma^+]$, i.e., Statements (iv) for $k + 1$ holds. Statement (iii) for $k + 1$ is deduced from the fact that it takes at least $(T_1^+ + T_3^+)/\vartheta$ time until the first node from $W$ switching to $propose^+$ after $t_k + \Sigma^+$ does so, since timeouts $T_1^+$ and $T_3^+$ need to be reset and expire first, one after the other.

Finally, we need to establish Statement (v) for $k + 1$. If $M$ does not divide $k + 1$, Statement (v) for $k + 1$ follows from Statement (v) for $k$. Otherwise $M$ does divide $k + 1$
and we can bound\(^{22}\)
\[
(i),(ii)\quad t_{k+1} + \Sigma^+ + d \\
\geq t_{MI} + \frac{M(T_1^+ + T_3^+)}{\vartheta} - T_1^+ + T_2^+ + \Sigma^+ + d \\
\geq t_{MI} + T_2 + T_3 + \Sigma^+ + 4d .
\]
As by Statement (v) for \(k\) all nodes in \(W\) switched to accept during \([t_{MI}, t_{MI} + \Sigma^+ + 2d)\), we conclude\(^{23}\) from the main state machines’ description that all nodes in \(W\) are observed in state ready with timeout \(T_3\) being expired (or already switched to propose or even accept) by time \(t_{MI} + 2T_2 + T_3 + \Sigma^+ + 4d\). Because all their NEXT signals switch to one during \([t_{k+1}, t_{k+1} + \Sigma^+)\), all nodes in \(W\) must therefore have switched to propose by time \(t_{k+1} + \Sigma^+ + d\). Consequently\(^{24}\) as we stated that w.l.o.g. they do not switch to accept again before time \(t_{k+1}\), they do so at times in \([t_{k+1}, t_{k+1} + \Sigma^+ + 2d)\) as claimed.

This completes the induction. According to Statement (i), \(t_1\) satisfies the claimed bound on the stabilization time. With respect to this time, Statement (iv) provides the skew bound, and combining it with Statements (ii) and (iii), respectively, yields the stated accuracy bounds. Statements (vi) and (vii) show the properties of the counters. Metastability-freedom of the state machine is trivially guaranteed by the fact that each state has a unique successor state. For the counter, we can infer metastability-freedom after stabilization from the observation made in the proof that for times \(t \geq t_1\), \((T_2, \text{accept})(t) = 0\) at a non-faulty node implies that it is in state \(\text{accept}^+\) with its cycle counter equal to zero. This completes the proof.

For some applications, one might require an even higher operational frequency than provided by the quick cycle state machine. It turns out that there is a simple solution to this issue.

**Increasing the Frequency Further**

Given any pulse synchronization protocol, one can derive clocks operating at an arbitrarily large frequency as follows. Whenever a pulse is triggered locally, the nodes start to increase a local integer counter modulo some value \(m \in \mathbb{N}\) at a speed of \(\phi \in \mathbb{R}^+\) times that of a local clock, starting from 0. Denote by \(T^-\) the accuracy lower bound of the protocol and suppose that the local clock controlling the counter runs at a speed between 1 and \(\rho \in (1, \vartheta]\), i.e., its maximum drift is \(\rho - 1\)\(^{25}\). Once the counter reaches the value \(m - 1\), it is halted until the next pulse. We demand that
\[
m \leq \phi T^- .
\]
This approach is similar to the one presented in [23], enriched by addressing the problem of metastability.

In the context of the FATAL\(^+\) protocol, we get the following result.

**Corollary 6.3:** Adding a counter as described above to the FATAL\(^+\) protocol and concatenating the counter values of the two counters at node \(i \in V\) yields a bounded logical clock \(L_i \in \{0, \ldots, mM - 1\}\). At any time \(t\) when the protocol has stabilized on some set \(W\) (according to Theorem 6.2), it holds for any two nodes \(i, j \in W\) that
\[
|L_i(t) - L_j(t)| \mod mM \leq \left\lfloor \phi \Sigma^+ + \left(1 - \frac{1}{\rho}\right) m \right\rfloor .
\]
Once stabilized, these clocks do not “jump”, i.e., they always increase by exactly one mod \(mM\), with at least \(1/\rho\) time between any two consecutive “ticks”.

The amortized clock frequency is within the bounds \(m/(T_1^+ + T_3^+ + \Sigma^+ + 3d_{\text{max}})\) and \(\vartheta m/(T_1^+ + T_3^+ - \Sigma^+)\). Viewed as a state machine in our model, the clocks \(L_i\), where \(i \in W\), are metastability-free after stabilization.

**Proof:** Observe that it takes at least \(m/(\phi \rho)\) time for one of the new counters to increase from 0 to \(m\). Since the counters are restarted at pulses, which are triggered locally at most \(\Sigma^+\) time apart, at the time when a “fast” node arrives at the value \(m\), a “slow” node will have increased its clock by at least \([m/\rho - \phi \Sigma^+]\). According to [inequality (43)], slow nodes will be able to increase their counters to \(m\) before the next pulse. The claimed bound on the clock skew and the facts that clock increases are one by one and at most every \(1/\rho\) time follow.

The bound on the amortized clock frequency follows by considering the minimal and maximal times \(M\) iterations of the quick cycle may require.

The metastability-freedom of the clock is deduced from the metastability-freedom of the individual counters. For the new counter this is guaranteed by [inequality (44)] since the counter is always halted at 0 before it is reset due to a new quick cycle pulse.

We remark that in an implementation, one would probably utilize the better clock source, if available, to drive \(T_1^+\) and \(T_3^+\) as well.\(^{26}\) Maximizing \(m\) with respect to [inequality (44)] and choosing \(T_1^+ + T_3^+\) sufficiently large will thus result in clocks whose amortized drift is arbitrarily close to \(\rho\), the drift of the underlying local clock source.

**VII. IMPLEMENTATION**

In this section, we provide an overview of our FPGA prototype implementation of the FATAL\(^+\) protocol. The...
purposes of this implementation are (i) to serve as a proof of concept, (ii) to validate the predictions of the theoretical analysis, and (iii) to form a basis for the future development of protocol variants and engineering improvements. Rather than striving for optimizing performance, area or power efficiency, our primary goal is hence to essentially provide a direct mapping of the algorithmic description to hardware, and to evaluate its properties in various operating scenarios.

Our implementation does not follow the usual design practice, for several reasons:

Asynchrony: Targeting ultra-reliable clock generation in SoCs, the implementation of FATAL$^+$ itself cannot rely on the availability of a synchronous clock. Moreover, some performance-critical guards, like the one of the transition from propose to accept in Figure 2 are purely asynchronous and should hence not be synchronized to a local clock. Even worse, testing for activated guards synchronized to a local clock source bears the risk to generate metastability, as remote signals originate in different clock domains. On the other hand, conventional asynchronous state machines (ASM) are not well-suited for implementing Figure 2. Figure 3 due to the possibility of choice of successor states and continuously enabled (i.e., non-alternating) guards. Our prototype relies on hybrid state machines (HSM) that combine an ASM with synchronous transition state machines (TSM) that are started on demand only.

Fault tolerance: The presence of Byzantine faulty nodes forced us to abandon the classic “wait for all” paradigm traditionally used for enforcing the indication principle in asynchronous designs: Failures may easily inhibit the completion of the request/acknowledge cycles typically used for transition-based flow control. Timing constraints, established by our theoretical analysis, in conjunction with state-based communication are resorted to in order to establish event ordering and synchronized executions in FATAL$^+$.

Self-Stabilization: In sharp contrast to non-stabilizing algorithms, which can always assume that there is a (substantial) number of non-faulty nodes that run approximately synchronously and hence adhere to certain timing constraints, self-stabilizing algorithms cannot even assume this. Although FATAL$^+$ guarantees that non-faulty nodes will eventually execute synchronously, even when started from an arbitrary state, the violation of timing constraints and hence metastability cannot be avoided during stabilization. For example, state accept in Figure 2 has two successors sleep and recover, the guards of which could become true arbitrarily close to each other in certain stabilizing scenarios. This is acceptable, though, as long as such problematic events are neither systematic nor frequent, which is ensured by the design and implementation of FATAL$^+$ (see Section VII-A).

Inspecting Figure 2 reveals that the state transitions of the FATAL$^+$ state machines are triggered by AND/OR combinations of the following different types of conditions:

1. A watchdog timer expires [“(T2, accept)”].
2. The state machines of a certain number ($1, \geq f + 1, or \geq n - f$) of nodes reached a particular (subset of) state(s) at least once since the reset of the corresponding memory flags [“$\geq n - f$ accept”].
3. The state machines of a certain number ($1, \geq f + 1, or \geq n - f$) of nodes are currently in (one of) a particular (subset of) state(s) [“in resync”].
4. Always [“true”].

The above requirements reveal the need for the following major building blocks:

- Concurrent HSMs, implementing the states and transitions specified in the protocol.
- Communication infrastructure between those state machines, continuously conveying the state information.
- Watchdog timers (also with random timeouts) for implementing type (1) guards.
- Threshold modules and memory flags for implementing type (2) and type (3) guards.

Obviously, all these building blocks require implementations that match the assumptions of the formal model in Section II. Apart from maintaining timing assumptions like an end-to-end communication delay bound $t - \tau_{ij}^{-1}(t) < d$, this also includes the need to implement all stateful components in a self-stabilizing way: They must be able to eventually recover from an arbitrary erroneous internal state, including metastability, when operating in the specified environment.

Before we proceed with a description of the implementations of these components, we discuss how FATAL$^+$ deals with the threat of metastability arising from our extreme fault scenarios.

A. Metastability issues

Reducing the potential for both metastability generation and metastability propagation are important goals in the design and implementation of FATAL$^+$. Although it is impossible to completely rule out metastability generation in the presence of Byzantine faulty nodes (which may issue signal transitions at arbitrary times) and during self-stabilization (where all nodes may be completely asynchronous), we nevertheless achieved the following properties:

(I) Guaranteed metastability-freedom in fault-free executions after stabilization.

(II) Non-faulty nodes are safeguarded against “attacks” by faulty nodes that aim at inducing metastability, in particular once the system has stabilized.

(III) Metastable upsets at non-faulty nodes are rare during stabilization, therefore delaying stabilization as little as possible.

(IV) Very small windows of vulnerability and the possibility to incorporate additional measures for decreasing the upset probability further.
The following approaches have been used in FATAL+ to accomplish these goals (additional details will be given in the subsequent sections):

(I) is guaranteed by our proofs of metastability-freedom, which exploit the fact that all non-faulty nodes run approximately synchronously after stabilization. It is hence relatively straightforward to ensure, via timing constraints, that some data from remote ASMs does not change while it is used.

(II) is accomplished by several means, which make it very difficult (albeit not impossible) for a faulty node to generate/propagate metastability. Besides avoiding any explicit control flow between ASMs by communicating states only, which greatly reduces the dependency of a non-faulty receiver node from a faulty sender, several forms of logical masking of metastability are employed. One example is the combination of memory flags and threshold gates, which ensure that possibly upset memory flags are always overruled quickly by correct ones at the threshold output. A different form of logical masking occurs due to the fact that, after stabilization, all non-faulty nodes execute the outer cycle of the main state machine (Figure 2) only: Since the outer cycle does not involve any type (3) guard once stabilization is achieved, any metastability originating from the (less metastability-safe) resynchronization algorithm (Figure 4) and its extension (Figure 3) is completely masked.

To accomplish (III), the measures outlined in (2) are complemented by adding time masking using randomization: The resynchronization routine (Figure 4) tries to initialize recovery from arbitrary states at random, sufficiently sparse points in time. It is hence very unlikely that non-faulty nodes are kept from stabilizing due to metastable upsets. Moreover, if at the beginning of the stabilization process \( f' < f < n/3 \) nodes are faulty, up to \( f - f' \) metastable upsets can be tolerated without keeping the remaining nodes from stabilizing; the nodes that became subject to newly arising transient faults will stabilize quickly once \( n - f \) nodes established synchronization (cf. Theorem 4.17).

Finally, (IV) is achieved by implementing all building blocks that are susceptible to metastable upsets, like memory flags, in a way that minimizes the window of vulnerability. Moreover, elastic pipelines acting as metastability filters [29] or synchronizers can be added easily to further protect such elements.

**B. State machine communication**

According to our system model, an HSM must be able to continuously communicate its current state system-wide: It is requested that every receiver is informed of the sender’s current state within \( d \) time (resp. within \( d_{\text{min}} \) and \( d_{\text{max}} \) for the quick cycle algorithm). For simplicity, we use parallel communication, by means of a suitably sized data bus, in our implementation.\(^{27}\) Since a node treats itself like any other node in type (2) and type (3) guards with thresholds, it comprises a complete receiver as described below for every node in the system (including itself).

Figure 6 shows the circuitry used for communicating the current state of the main algorithm in Figure 2. The sender consists of a simple array of flip-flops, which drive the parallel data bus that thus continuously reflects the current state of the sender’s HSM. In sharp contrast to handshake-based communication, reading at the receiver occurs without any coupling to the sender here. As argued in Section VII-A, the synchrony between non-faulty nodes guaranteed by the FATAL+ protocol guarantees that the sender state data will always be stable when read after stabilization. For the stabilization phase, we cannot give such a guarantee but take some (acceptable) risk of metastability.

To avoid the unacceptable risk of reading and capturing false intermediate sender states due to different delays on the wires of the data bus, delay-insensitive [43] state coding must be used. We have chosen the following encoding for the main state machine in Figure 2.

\(^{27}\)It is, however, reasonably easy to replace parallel communication by serial communication, e.g., by extending the (synchronous) TSM appropriately.
propose 0000 accept 1001
sleep 1011 sleep → waking 0011
waking 0101 ready 0110
recover 1100 join 1010

For the other state machines making up FATAL⁺, it suffices to communicate only a single bit of state information (supp or none in Figure 3, init or wait in Figure 4, and propose⁺ or none⁺ in Figure 5). Hence, every bus consists of a single wire here, and the decoder in the receiver becomes trivial.

The receiver consists of a simple combinational decoder consisting of AND gates, which generate a 1-out-of-\( m \) encoding of the binary representation of the state communicated via the data bus. The decoded signals correspond to a single sender state each. This information is directly used for type (3) guards, and fed into memory flags for type (2) guards. Every memory flag is just an SR-latch with dominant reset, whose functional equivalents are also included in Figure 6. Note that a memory flag is set depending on the state communicated by the sender, but (dominantly) cleared under the receiver’s control.

A memory flag may become metastable when the inputs change during stabilization of its feedback loop, which can occur due to (a) input glitches and/or (b) simultaneous falling transitions on both inputs. However, for correct receivers, (a) can only occur in case of a faulty sender, and (b) is again only possible during stabilization: Once non-faulty nodes execute the outer cycle of Figure 2, it is guaranteed that e.g. all non-faulty nodes enter accept before the first one leaves. The probability of an upset is thus very small, and could be further reduced by means of an elastic pipeline acting as metastability filter (which must be accounted for in the delay bounds).

The most straightforward implementation of the threshold modules used for generating the \( \geq f + 1 \) and \( \geq n - f \) thresholds in type (2) and type (3) guards is a simple sum-of-product network, which just builds the OR of all AND combinations of \( f + 1 \) resp. \( n - f \) inputs. In our FPGA implementation, a threshold module is built by means of lookup-tables (LUT); some dedicated experiments confirmed that they work glitch-free for monotonic inputs (as provided by the memory flags).

C. Hybrid state machines

Our prototype implementation of FATAL⁺ relies on hybrid state machines (HSM): An ASM is used for determining, by asynchronously evaluating the guards, the points in time when a state transition shall occur. Our ASMs have been built by deriving a state transition graph (STG) specification directly from Figures 2–5 and generating the delay-insensitive implementation via Petrify [32]. The actual state transition of an HSM is governed by an underlying synchronous transition state machine (TSM). The TSM resolves a possibly non-deterministic choice of the successor state and then performs the required transition actions:

1. Reset of memory flags and watchdog timers
2. Communication of the new state
3. Actual transition to the new state (i.e., enabling of further transitions of the ASM)

The TSM is driven by a pausable clock (see Section VII-D), which is started dynamically by the ASM before the transition. Note that this avoids the need for synchronization with a free-running clock and hence preserves the ASMs continuous time scale.

The TSM works as follows (see Figure 7): Assume that the ASM is in state \( A \), and that the guard \( G \) for the transition from \( A \) to \( B \) becomes true. In the absence of an inhibit signal (indicating that another transition is currently being taken, see below), the TSM clock is started. With every rising edge of TSMClock, the TSM unconditionally moves through a sequence of three states: synchronize (Syn), commit (Cmt), and terminate (Trm) shown in the rectangular box in Figure 7. In Syn, the inhibit signal is activated to prevent other choices from being executed in case of more than one guard becoming true. Whereas any ambiguity can easily be resolved via some priority rule, metastability due to (a) enabled guards that become immediately disabled again or (b) new guards that are enabled close to transition time cannot be ruled out in general here. However, as argued in Section VII-A (a) could only do harm to FATAL⁺ during stabilization, due to type (3) guards; recall that type (1) and type (2) guards are always monotonic, with the reset (of watchdog timers and memory flags) being under the control of the local state machine. Similarly, our proofs reveal that upsets due to (b) are fully masked after stabilization. Thus, after stabilization, metastability of the TSM can only occur due to unstable inputs, i.e., upsets in memory flags. Given the small window of vulnerability of the synchronizing stage for Syn, the resulting very low probability of a metastable upset is considered acceptable.

Once the TSM has reached Syn, it has decided to actually take the transition to \( B \) and hence moves on to state Cmt. Here the watchdog timer associated with \( B \) and possibly

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Note that the STG specification had to be extended slightly in order to transform our possibly non-alternating guards (which might be continuously enabled in some cycle, in particular during stabilization) into strictly alternating ones.
some memory flags are cleared according to the FATAL+ state machine, and the new state B is captured by the output flip-flops driving the state communication data bus (recall Section VII-B). Note that the resulting delay must be accounted for in the communication delay bounds $d$, $d_{\text{min}}^+$ and $d_{\text{min}}^-$. Finally, the TSM moves on to state $Trm$, in which the reset signals are inactivated again and the TSM clock is halted. The inhibit signal is also cleared here, which effectively moves the ASM to state $B$. It is only now that guards pertaining to state $B$ may become true.

D. Pausible oscillator

The TSM clock is an asynchronously startable and synchronously stoppable ring oscillator, which provides a clock signal $TSMClock$ that is LOW when the clock is stopped via an input signal $TSMCStop$. Note that copies of this oscillator are used for driving the watchdog timers presented in Section VII-E.

The operation of the TSM clock circuit shown in Figure 8 is straightforward: In its initial state, $TSMCStop$=HIGH and the Muller C-gate has HIGH at its output, such that $TSMClock$=LOW. Note that the circuit also stabilizes to this state if the Muller C-gate was erroneously initialized to LOW, as the ring oscillator would eventually generate $TSMClock$=HIGH, enforcing the correct initial value HIGH of the C-gate.

When the ASM requests a state transition, at some arbitrary time when a transition guard became true, it just sets $TSMCStop$=LOW. This starts the TSM clock and produces the first rising edge of $TSMClock$ half a clock cycle time later. As long as $TSMCStop$ remains LOW, the ring oscillator runs freely.

The frequency of the ring oscillator is primarily determined by the (odd) number of inverters in the feedback loop. It varies heavily with the operating conditions, in particular with supply voltage and temperature: The resulting (two-sided) clock drift $\xi$ is typically in the range of 7% . . . 9% for uncompensated ring oscillators like ours; in ASICs, it could be lowered down to 1% . . . 2% by special compensation techniques. Note that the two-sided clock drifts map to $\vartheta = (1 + \xi)/(1 - \xi)$ bounds of 1.15 . . . 1.19 and 1.02 . . . 1.04, respectively.

The stopping of $TSMClock$ is regularly initiated by the TSM itself: With the rising edge of $TSMClock$ that moves the TSM into $Trm$, $TSMCStop$ is set to HIGH. Since $TSMClock$ is also HIGH after the rising edge $30$ the C-gate output is also forced to HIGH. Hence, after having finished the half period of this final clock cycle, the feedback loop is frozen and $TSMClock$ remains LOW.

For metastability-free operation of the C-gate in Figure 8 (a) the falling transition of $TSMCStop$ must not occur simultaneously with a rising edge of $TSMClock$, and (b) the rising transition of $TSMCStop$ must not occur simultaneously with the falling edge of $TSMClock$. (a) is guaranteed by stopping the clock in state $Trm$ of the TSM, since the output of the C-gate is permanently forced to HIGH on this occasion; $TSMClock$ cannot hence generate a rising transition before $TSMCStop$ goes to LOW again. Whereas this synchronous stopping normally also ensures (b), we cannot always rule out the possibility of getting $TSMCStop$=HIGH close to the first rising edge of $TSMClock$: (b) could thus occur due to prematurely disabled type (3) guards, which we discussed already with respect to their potential to create metastability in the TSM, recall Section VII-C. Besides being a rare event, this can only do harm during stabilization, however.

E. Watchdog Timers

Recall that every ASM state, except for $accept$ in Figure 2 is associated with at most one watchdog timer required for type (1) guards; $accept$ is associated with three timers (for $T_1$ and $T_2$ as well as for $T_2^+$ in Figure 5). A timer is reset by the TSM when its associated state is entered.

According to Figure 9, every watchdog timer consists of a synchronous resettable up-counter that is clocked by some oscillator, and a timeout register that holds the timeout value. A comparator raises an output signal if the counter value is greater or equal to the register value. An SR latch with dominant reset memorizes this expired condition until the timer is re-triggered.

Like the TSM, timers are driven by pausible oscillators, which are started by the TSM after resetting the timer and stopped synchronously upon timer expiration. Note that every timer (except for the multiple $accept$ timers, which share a common oscillator that is stopped when the largest timeout expires) is provided with a dedicated oscillator in our implementation for simplicity. This not only avoids

$29$ In our FPGA implementation, the oscillator frequency is so high that we also employ a frequency divider at the output.

$30$ Obviously, we only have to take care in the timing analysis that setting $TSMCStop$=HIGH occurs well within the first half period.
Quantization errors in the continuous timing of the ASM state transitions, but is also mandatory for avoiding the potential of metastability due to timer resets colliding with the transitions of a free-running clock. In our implementation, the timer reset takes place in TSM state \( Cnt \), while the oscillator is started in state \( Trm \). This well ordered sequence rules out all metastability issues.

As for the watchdog timer with random timeout \( R_t \) in Figure 4, our implementation uses an *linear feedback shift register* (LFSR) clocked by a dedicated oscillator: A uniformly distributed random value, sampled from the LFSR, is loaded into the timeout register whenever the watchdog timer is re-triggered. Note that for many settings, it is reasonable to assume that the new random value remains a secret until the timeout expires, as it is not read or in any other way considered by the node until then. As our prototype implementation is not meant for studying security issues, this simple implementation is thus sufficient.

**VIII. Experimental Evaluation**

Our prototype implementation has been written in VHDL and compiled for an Altera Cyclone IV FPGA using the Quartus tool.

Apart from standard functional and timing verification via Modelsim, we conducted some preliminary experiments for verifying the assumed properties (glitch-freeness, monotonicity, etc.) of the synthesized implementations of our core building blocks: Since FPGAs do not natively provide the basic elements required for asynchronous designs, and we have no control over the actual mapping of functions to the available LUTs (e.g. our threshold modules are implemented via LUT instead of the intended combinational AND-OR networks), we had to make sure that properties that hold naturally in "real" asynchronous implementations also hold here. Backed up by the (positive) results of these experiments, a complete system consisting of \( n = 4 \) resp. \( n = 8 \) nodes (tolerating at most \( f = 1 \) resp. \( f = 2 \) Byzantine faulty nodes) has been built and verified to work as expected; overall, they consume 23000 resp. 55000 logic blocks. Note however, that both designs include the test environments which makes up a significant part of the designs.

To facilitate systematic experiments, we also developed a custom test bench that provides the following functionality:

1. Measurement of pulse frequency and skew at different nodes.
2. Continuous monitoring of the potential of non-deterministic HSM state transitions.
3. Starting the entire system from an arbitrary state (including memory flags and timers), both deterministically and randomly chosen.
4. Resetting a single node to some initial state, at arbitrary times.
5. Varying the clock frequency of any oscillator, at arbitrary times.
6. Varying the communication delay between any pairs of sender and receiver, at arbitrary times.

All these experiments can be done with and without up to \( f \) (actually, \( f + 1 \) to also include excessively many) Byzantine nodes. To this end, the HSMs of at most \( f + 1 = 3 \) nodes can be replaced by special devices that allow to (possibly inconsistently) communicate, via the communication data buses, any HSM state to any receiver HSM at any time.

1. is accomplished using standard measurement equipment (logic analyzer, oscilloscope, frequency counter) attached to the appropriate signals routed via output pins. (2) is implemented by memorizing any event where more than one guard is enabled when the TSM performs its first state transition, in a flag that can be externally monitored.

3. is realized by adding a scan-chain to the implementation, which allows to serially shift-in arbitrary initial system states at run-time. Repeated random experiments are controlled via a Python script executed at a PC workstation, which is connected via USB to an ATMega 16 microcontroller (uC) that acts as a scan-controller towards the FPGA. The uC takes a bit-stream representing an initial configuration, sends it to the FPGA via the serial scan-chain interface, and signals the FPGA to start execution of FATAL\(^+\). When the system has stabilized, the uC informs the Python script which records the stabilization time and proceeds with sending the next initial configuration.

To enable (4)–(6), the testbench provides a global high-resolution clock that can be used for triggering mode changes. To ensure its synchrony w.r.t. the various node clocks, all start/stoppable ring oscillators are replaced by start/stoppable oscillators that derive their output from the global clock signal. (4) is achieved by just forcing a node to reset to its initial state for this run at any time during the current execution. In order to facilitate (5), dividers combined with clock multipliers (PLLs) are used: For any oscillator, it is possible to choose one of five different frequencies (0, excessively slow, slow, fast, excessively fast) at any time. For (6), a variable delay line implemented as a synchronous shift register of length \( X \in [0, 15] \), driven by the global clock, can be inserted in any data bus connecting different HSMs individually.

In order to exercise also complex test scenarios in a reproducible way, a dedicated *testbed execution state machine* (TESM), driven by the global clock, is used to control the times and nodes when and where clock speeds, transmission delays and communicated fault states are changed and when a single node is reset throughout an execution of the system. Transition guards may involve global time and any combinatorial expression of signals used in the implementation of FATAL\(^+\), i.e., any predicate on the current system state\(^{31}\).

\(^{31}\)To decrease the experiment setup time (after all, changing the TESM requires recompilation of the entire system), the TESM is gradually changed to also incorporate additional parameters and configuration information downloaded at run-time via the uC.
Figure 10. FATAL and FATAL+ clocks: $\text{MainAlgState}[i]=1$ iff $i$ is in accept, and $\text{FATAL+CLK}[i]$ is $i$’s FATAL+ signal.

Figure 11. Worst-case skew scenario for FATAL clocks.

Using our testbench, it was not too difficult to get our FATAL+ up and running. As expected, we spotted several hidden design errors that showed up during our experiments, but also some errors (like a missing factor of $\vartheta$ in one of our timeouts due to a typo) in the initial version of our theoretical analysis, which caused deviations of the measured w.r.t. the predicted performance.

Finally, using the implementation parameters $\vartheta = 1.3$, $d = 13T$, $d_{\text{min}}^+ = d_{\text{max}}^+ = 3T$, where $T$ is the experimental clock period $T = 400$ ns, and minimal timeouts according to the constraints, we conducted the following experiments, observing the behavior of both, the FATAL+ as well as the underlying FATAL system:

(A) Maximum skew scenarios, including effects of excessively small/fast clocks and message delays: The experimental results confirmed the analytic predictions as being tight: As shown in Figure 10 pulses of the 8 node FATAL resp. FATAL+ system occur at a frequency of about 62Hz resp. 10kHz. Note that the quite low values for the frequency stem from the fact that we were intentionally slowing down the system in order to carry out our worst-case experiments.

The figure further clearly demonstrates the capability of FATAL+ to generate pulses with significantly less skew ($1\mu$s) on top of the FATAL pulses.

Further experiments, involving $f = 2$ Byzantine nodes, were used to produce a worst-case scenario for the FATAL skew ($6\mu$s). The resulting waveform is depicted in Figure 11.

(B) Scenarios leading to the potential of non-deterministic HSM state transitions in the absence of Byzantine nodes (which would invalidate our proof of metastability-freedom if happening after stabilization): We run 17000 experiments, in each of which the 8 node system was set up with randomly chosen message delays between nodes and random clock speeds and stabilized from random initial states. Within 10 seconds from stabilization on, not a single upset was encountered in any instance.

(C) Stabilization of an 8-node system from random initial states, with randomly chosen clock speeds and message delays (without Byzantine nodes). Over 4000 runs have been performed. A considerable fraction of the setups stabilizes within less than 0.035 seconds, which can be credited to the fast stabilization mechanism intended for individual nodes resynchronizing to a running system (see Figure 12 and Figure 13). The remaining runs stabilize, supported by the resynchronization routine, in less than 10 seconds, which is less than the system’s upper bound on $T(1)$. Note that the stabilization time is inversely proportional to the frequency, i.e., in a system that is not slowed down stabilization is orders of magnitude faster.

IX. CONCLUSIONS

We conclude with a few considerations regarding the asymptotic complexity of implementations of FATAL+ and future work. The algorithm has the favorable property that nodes broadcast a constant number of bits in constant time, which clearly is optimal. While it would be beneficial to reduce node degrees, this must come at the price of reducing the resilience to faults [19], [20]. In terms of the number of Byzantine faults the algorithm can sustain in relation to node degrees, the algorithm is asymptotically optimal as well. It is subject to future work to extend the algorithm to be applicable to networks of lower degree in a way preserving resilience to a (local) number of faults that is optimal in terms of connectivity.

Furthermore, it is not difficult to see that except for the threshold modules, each node comprises a number of basic components that is linear in $n$ (cf. [37], where similar building blocks were used). In an ASIC implementation,
one could implement the threshold modules by sorting networks, resulting in a latency of $O(\log n)$ and a gate complexity of $O(n \log n)$ [45]. Clearly, it is necessary to have conditions involving more than $f$ nodes in order to overcome $f$ Byzantine faults. Hence, assuming constant fan-in of the gates, both the current and envisioned solutions are asymptotically optimal with respect to latency. Optimality of an implementation relying on sorting networks with respect to gate complexity is not immediate, however there is at most a logarithmic gap to the trivial lower bound of $\Omega(n)$.

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