Enhanced all-optical Y-shaped plasmonic OR, NOR and NAND gate models, analyses, and simulation for high speed computations

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Abstract
In this digital era, all-optical logic gates (OLGs) proved its effectiveness in execution of high-speed computations. A unique construction of an all-optical OR, NOR, and NAND gates based on the notion of power combiner employing metal–insulator-metal (MIM) waveguide in the Y-shape with a minimal imprint of 6.2 µm × 3 µm is presented and the structure is evaluated by finite-difference time-domain (FDTD) technique. The insertion loss (IL) and extinction ratio (ER) for proposed model are 6 dB and 27.76 dB for NAND gate, 2 dB and 20.35 dB for NOR gate and 6 dB and 24.10 dB for OR respectively. The simplified model is used in the construction of complex circuits to achieve greater efficiency, which contributes to the emergence of a new technique for designing plasmonic integrated circuits.

Keywords All-optical logic gate · MIM waveguide · Plasmonic waveguide · Y-power combiner · Finite-difference time-domain (FDTD)

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1 Introduction

The semiconductor trade has achieved tremendous advancement over the last several decades, despite the limitations of restricted bandwidth, high input power, short switching time, high power dissipation, and communication delays. Optical communication was developed as a solution to address these issues since it substituted electrons with photons as a technique to transmit information (Swarnakar et al. 2021a; Hussain et al. 2018). Optics surpasses electronic systems in terms of operating bandwidth, minimum electromagnetic interference, speed, and large data transfer capacity. Since optical circuits may offer potential solutions for signal transmission and processing, they are considered as bright prospects (Rao et al. 2021).

The modern technology aims for rapid communication devices that can surpass the diffraction limit of photonic devices, and plasmonics have shown to be a viable option in this regard (Pal et al. 2021; Cotter et al. 1999; Rezaei et al. 2018). It is the science that focuses on generating, optical signal detecting and processing at metal–dielectric interface (Sorger et al. 2012). Plasmonic waveguides may be used to address the main disadvantages in a plasmonic circuit, such as restricted propagation time, rise in temperature and difficulty in changing the signal direction. In recent years, researchers have examined different plasmonic waveguides including MIM, IMI, and dielectric-loaded surface plasmon polaritons (DLSPP) (Moradi et al. 2019). Compared to insulating waveguides, plasmonic MIM waveguides enable greater confinement and therefore been presented as a potential option for nanoscale optical circuits (Chen et al. 2009; Singh et al. 2017; Dolatabady and Granpayeh 2012; Sadeghi et al. 2019; Sharma et al. 2020). Noble metals like silver and gold have surface plasmons at visible and near-infrared wavelength. For optical devices, plasmonic nanoparticles are excellent rivals because of their unique features such as absorption, coupling, and scattering (Nozhat et al. 2017). Logic gates are essential components in all optical circuit design and a numerous optical equipments, like directional coupler (DC), Mach–Zehnder Interferometer (MZI), power couplers, and power dividers are utilized to realise logic gates such as AND (Kumar and Singh 2016; Ghomashi et al. 2021), OR (Sharma et al. 2020; Ghomashi et al. 2021), XOR (Nozhat et al. 2017; Raja et al. 2021), NOT (Fakhruldeen and Mansour 2018; Raja et al. 2021; Wu et al. 2013) and XNOR (Rao et al. 2020a), along with universal gates such as NAND (Nozhat et al. 2017; Kumar and Singh 2016; Ghomashi et al. 2021; Fakhrudeen and Mansour 2018; Raja et al. 2021; Wu et al. 2013; Rao et al. 2020a) and NOR (Rao et al. 2020a, 2020b). As a result, these all-OLGs may be utilised to construct any combinational circuit including multiplexers, demultiplexers, parity generator, adders and subtractors, and code translators (Meymand et al. 2020; Kumar et al. 2017; Swarnakar et al. 2020). Conventional OLGs give cut-off states and interference effects, but plasmonic logic gates greatly minimize size and signal losses; it can also lower signal thresholds of logic operations and offer rapid switching in optical devices (D’souza and Mathew 2016; Singh et al. 2019; Anguluri et al. 2021; Swarnakar et al. 2021b).

Two-dimensional (2D) MIM waveguides are selected for this logic device implementation because of their simple configuration and ability to confine light at the nanoscale, reasonable propagation distances, and low crosstalk making them ideal candidates for various ultra-compact devices as well as other characteristics (Al-Musawi et al. 2020; Dolatabady and Granpayeh 2017; Li et al. 2020; Safinezhad et al. 2021). Many logic operations may be performed with the MIM device without changing the phase of input signals in subsequent implementations (Singh et al. 2021; Choudhary and Kumar 2021; Jasim et al. 2021).
The framework of the suggested paper presents a simplified all-optical OR, NOR and NAND gate design with power coupling concept employing a Y-shaped waveguide and analysed using FDTD method. The Y-power coupler plasmonic OR, NOR and NAND gate design is reported in Sect. 2. Section 3 presents the simulation findings. Section 4 has a result analysis, in which the current study is also compared to prior published studies, and Sect. 5 concludes the paper.

2 The all-optical plasmonic OR, NOR, and NAND gate structure employing Y-power combiner

A miniaturized all-optical plasmonic OR, NOR, and NAND gate is modelled by arranging S-bend and linear waveguides of equal width (W) using power combiner concept. The presented design is obtained in a wafer size of 6.2 μm × 3 μm by arranging two parallel S-bend waveguides of equal length along XZ axis in Y shape separated by a distance, D and joined to single end of a linear waveguide whose structure is shown in Fig. 1. An external change in the phase controls the inputs supplied to both ends of the power combiner.

The final minimized structure is achieved by varying the Y-combiner parameters such as the length of S-bend waveguide (L_s), separation gap between inputs (D), and length of linear waveguide (L). By altering the L_s and maintaining D as 2.5 μm, different factors like the highest output power when turned ON and OFF and also ER may be determined, as shown in Table 1. The ER is estimated by comparing the peak output power in ON (P_{out|ON}) with peak output power in OFF (P_{out|OFF}) states and is represented as

\[
\text{Extinction ratio (ER)} = 10 \log_{10} \left( \frac{P_{out|ON}}{P_{out|OFF}} \right)
\]  

| Sl. no | Length of S-bend waveguide (μm) | P_{ON} (W) | P_{OFF} (W) | Extinction ratio (dB) |
|--------|-------------------------------|------------|-------------|-----------------------|
| 1      | 3.1                           | 4.26       | 0.009       | 26.75                 |
| 2      | 3.2                           | 4.31       | 0.008       | 27.31                 |
| 3      | 3.3                           | 4.36       | 0.008       | 27.36                 |
| 4      | 3.4                           | 4.37       | 0.008       | 27.37                 |
| 5      | 3.5                           | 4.32       | 0.008       | 27.32                 |
| 6      | 3.6                           | 4.18       | 0.007       | 27.76                 |
| 7      | 3.7                           | 4.28       | 0.011       | 25.90                 |
whereas the Insertion loss (IL) is defined as the ratio of total input power ($P_{\text{in}}$) to the total output power ($P_{\text{out}}$) is given as

$$IL = 10\log_{10}\left(\frac{P_{\text{in}}}{P_{\text{out}}}\right)$$

(2)

The output findings are used to determine the performance metrics such as IL and ER. It is observed that for $L_s$ of 3.6 µm, the obtained ER value is 27.76 dB that is higher compared to the rest. The $L_s$ versus ER plot is depicted in Fig. 2.

Similarly, all parameters indicated are indeed computed by changing the value of $D$ by maintaining $L_s$ at 3.6 µm, the results are tabulated in Table 2. It is observed that ER is more for a separation between waveguide of 2.6 µm resulting in 27.76 dB. The separation between waveguides versus ER is plotted and displayed in Fig. 3.

The $L_s$ and D are maintained constant at 3.6 µm and 2.6 µm, correspondingly, whereas L is adjusted to get the highest ER. Table 3 presents the ER for various linear lengths of waveguide. The higher ER of 26.87 dB is reported for L with 2.5 µm. L versus ER plot is depicted in Fig. 4 and the final dimensions of the Y-power coupler plasmonic OR, NOR, NAND gate with the highest ER are tabulated in Table 4.

From Tables 1, 2, 3 it is observed that $L_s$ with 3.6 µm, D and $L_L$ as 2.6 µm and 2.8 µm has got the best ER. So, the footmark of the designed structure is fixed in the dimension of 6.2 µm × 3.0 µm. By considering the minimized structure’s footmark the OR and NOR gates are also verified.
The Y-power combiner plasmonic gate design and FDTD simulation results

The optimized all-optical OR, NOR, NAND gate design contains plasmonic waveguide of refractive index (n) as 2.1 with Boron Nitride material and continuous-waveform (CW) in transverse electric (TE) mode, with wavelength (λ) of 1.55 µm provided at both inputs. The power at input is 0.7e9 W/m and 3e9 W/m for low and high intensity optical signals,
respectively. The presented structure is analysed using the FDTD technique and the Figs. 5, 6, 7 shows and explain the simulation outcomes realized for all 2-input combinations.

According to the theory of wave optics, constructive interference occurs when the phase difference between two optical waves is greater than 2n, where n = 0, 1, 2… It will have an extremely high power level, which is consistent with the logic state "1" when this happens. If the phase difference is (2n + 1) π, destructive interference occurs, resulting in logic zero at the output port (D’souza and Mathew 2016). All the input states of two-input OR, NOR, NAND are provided with the change in phase of the inputs with either 0° or 180° to satisfy the gate’s output. Table 4 shows the parameters of the simulation for the design proposed.

### Table 4 The Y-shaped plasmonic OR, NOR, NAND gate Simulation parameters

| Simulation parameters | Considered value |
|----------------------|------------------|
| Power at less intensity | $0.7 \times 10^9$ W/m |
| Power at high intensity | $3 \times 10^9$ W/m |
| Size of X mesh (μm) | 0.0114 |
| Size of Z mesh (μm) | 0.0114 |
| X mesh cells | 349 |
| Z mesh cells | 603 |
| Transverse input field | Gaussian |

3.1 OR gate

Based on truth table of OR logic gate, when both inputs are low, the output is low; otherwise, it generates a high output. The explanation that follows gives details of different

![Propagation of light across the suggested Y shaped plasmonic OR gate power combiner for various instances using FDTD method](image-url)
inputs and phase changes done to the Y-shape combiner to make it work with the OR outputs. In this instance, both the Y-combiner inputs are provided a signal of less-power intensity 0.7e9 W/m. According to the OR gate truth table, the output power is noted to be low. varied phase of 180° and 0° is given to both input signals resulting in destructive interference and the OR gate output is observed to be low (Y = 0) as shown in Fig. 5(a). For next case, the upper end of combiner is given less- power intensity (0.7e9 W/m) in contrast the lower end of combiner is provided a signal of greater-power intensity (3e9 W/m). A same phase of 180° or 0° is allowed in both inputs resulting in constructive interference thereby the OR gate’s output is high (Y = 1), as illustrated in Fig. 5(b). In contrast to the preceding instance, the upper end of combiner is given a greater intensity (3e9 W/m) whereas the below end is provided a signal of less-intensity power (0.7e9 W/m). Due to constructive interference, high output of OR gate (Y = 1) is achieved as depicted in Fig. 5(c). Finally, the two inputs of power coupler are provided
a high intensity power signal (3e9 W/m), same phase of 180° or 0° is provided resulting in constructive interference with high output (Y = 1) as shown in Fig. 5(d).

### 3.2 NOR logic gate

According to the truth table of NOR logic gate, when both inputs are low, the NOR logic gate creates a high output; but provides low output for the rest. The explanation that follows goes into detail into the various inputs and phase shifts used by the Y-shape combiner to meet the NOR output’s requirements. In the first instance, both the Y-combiner inputs are provided a signal of less-power intensity 0.7e9 W/m. Same phase of 180° or 0° is given to both input signals resulting in constructive interference and the NOR gate output is observed to be higher (Y = 1) as shown in Fig. 6a. In the next case, upper end of combiner is given less-power intensity (0.7e9 W/m) in contrast the lower end of combiner is provided a signal of greater-power intensity (3e9 W/m). As in the preceding example, destructive interference will arise, reducing the strength of the output signal. As a result, the NOR gate’s output is low (Y = 0), as illustrated in Fig. 6b. In contrast to the preceding case, the upper end of combiner is given a greater intensity (3e9 W/m) whereas the below end is provided a signal of less-intensity power (0.7e9 W/m). Due to destructive interference, resulting in low output of NOR gate (Y = 0) as depicted in Fig. 6c. Finally, the two inputs of power coupler are provided a high intensity power signal (3e9 W/m), The phase for one input is 180° and the other is 0° resulting in destructive interference resulting in low output intensity (Y = 0) as shown in Fig. 6d.

### 3.3 NAND logic gate

When both inputs are high in a NAND logic gate, the output is low; otherwise, the output is high. An explanation of how the NAND output alters with phase in a Y-shape combiner can be found below. Figure 7 depicts the propagation of light along the proposed NAND gate for the specified input signal pairings using the FDTD method. In the initial state, both the Y-combiner inputs are provided a signal of less-power intensity 0.7e9 W/m. According to the NAND gate truth table, the output power is noted to be high. Same phase of 180° or 0° is given to both input signals resulting in constructive interference and the NAND gate output is observed to be higher (Y = 1) as shown in Fig. 7a. While in the next case, the upper end of combiner is given less-power intensity (0.7e9 W/m) and in contrast the lower end of combiner is provided a signal of greater-power intensity (3e9 W/m). A same phase of 180° or 0° is allowed in both inputs. As in the preceding example, destructive interference will arise, reducing the strength of the output signal. As a result, the NAND gate’s output is high (Y = 1), as illustrated in Fig. 7b. In contrast to the preceding instance, the upper end of combiner is given a greater intensity (3e9 W/m) whereas the below end is provided a signal of less-intensity power (0.7e9 W/m). Thereby, due to the same phase, constructive interference will arise, resulting in high output of NAND gate (Y = 1) as depicted in Fig. 7c. Finally, the two inputs of power coupler are provided a high intensity power signal (3e9 W/m) The phase for one input is 180° and the other is 0° resulting in destructive interference resulting in low output intensity (Y = 0) as shown in Fig. 7d.
Performance analyses

The design has a minimal footprint of 6.2 μm × 3 μm compared to the structures in previous works (Raja et al. 2021; Singh et al. 2019, 2021; Anguluri et al. 2021; Swarnakar et al. 2021b; Al-Musawi et al. 2020; Dolatabady and Granpayeh 2017; Li et al. 2020; Safinezhad et al. 2021). The performance of proposed design has been examined using simulated parameters such as ER, IL, response time, and speed. So, the proposed design obtained IL and ER of 6 dB and 27.76 dB. The other parameters like response time of 32 fs and bit rate of 31.25 THz is observed. Table 5 displays the $P_{out}$ observations for various input power intensities and phases for the Y-shaped MIM waveguide.

A comparison of the proposed structure with previous published works is made and tabulated in Table 6. The proposed logic device is constructed using -MIM waveguide due to its simple configuration, ability to confine light at the nanoscale, low crosstalk and reasonable propagation distance, which made them ideal competitors for various ultra-compact devices. Only MIMs are capable of confining light to deep sub-wavelengths and routing it at the nanoscale (Choudhary and Kumar 2021; Jasim et al. 2021). From Table 6, it is clear that the MIM waveguides results in highest extinction ratio compared to that of ring resonators and IMI waveguides. With the same structure OR, NOR and NAND gates were designed and also all the simulated parameters were calculated resulted in highest ER and transmission efficiency with less insertion loss shown in this design structure. More over for the same structure response time and speed are also calculated.

Conclusion

The suggested Y-shaped MIM waveguide concept is utilised to construct an all-optical OR, NOR, and NAND logic gate. The structure has a surface area of 6.2 μm × 3 μm, which is less than earlier efforts. In this study, the IL and ER calculated are key factors that are determined to be 6 dB and 27.76 dB, respectively and response time of 32 fs and bit rate of 31.25 THz are also observed. The length of S-bend waveguide, input separation, and linear length of waveguide are designed to provide the highest ER while minimising waveguide losses. The Y-combiner-based NAND gate, with its simple construction and controllability, can provide a novel approach for implementing digital...

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### Table 5 Output power ($P_{out}$) observations for OR, NOR and NAND gate

| Sl. No | Inputs | OR gate | NOR gate | NAND gate |
|--------|--------|---------|----------|-----------|
|        | $I_1$  | $I_2$   | Phase angle | Output power ($P_{out}$) | Phase angle | Output power ($P_{out}$) | Phase angle | Output power ($P_{out}$) |
|        | $\phi_{I_1}$ | $\phi_{I_2}$ | $\phi_{I_1}$ | $\phi_{I_2}$ | $\phi_{I_1}$ | $\phi_{I_2}$ | $\phi_{I_1}$ | $\phi_{I_2}$ | $\phi_{I_1}$ | $\phi_{I_2}$ |
| 1      | 0      | 0      | 0° 180° | 0.01 | 0° 0° | 1.73 | 0° 0° | 1.78 |
| 2      | 0      | 1      | 0° 0°  | 4.11 | 0° 180° | 0.35 | 0° 0° | 4.21 |
| 3      | 1      | 0      | 0° 0°  | 1.95 | 0° 180° | 0.12 | 0° 0° | 0.97 |
| 4      | 1      | 1      | 0° 0°  | 1.73 | 0° 180° | 0.01 | 0° 180° | 0.01 |
| Structure                        | Material used            | Extinction ratio (dB) | Footprint          | Refractive index | Low intensity      | High intensity     | Ref. No                  |
|---------------------------------|--------------------------|-----------------------|--------------------|------------------|--------------------|---------------------|--------------------------|
| SOA                             | Dual semiconductor       | 25                    | 800 µm             | n.r\(^a\)        | n.r\(^a\)          | n.r\(^a\)           | Raja et al. (2021)       |
| MZI                             | Plasmonic MIM waveguide  | 10.25                 | 40×7.5 µm\(^2\)    | 2.01             | 0.7e9 W/m          | 3e9 W/m            | Singh et al. (2019)      |
| Y shaped power combiner         | Plasmonic MIM waveguide  | 14.11                 | 7×4 µm\(^2\)       | 2.1              | 2e9 W/m            | 3e9 W/m            | Anguluri et al. (2021)   |
| Two non-linear MZI              | Plasmonic MIM waveguide  | 10.55                 | 36×8 µm\(^2\)      | 2.01             | 0.7e9 W/m          | 3e9 W/m            | Swarnakar et al. (2021b) |
| Nanorings resonators            | Plasmonic IMI waveguide  | 20                    | 400 nm×380 nm      | 1.375            | n.r\(^a\)          | n.r\(^a\)           | Al-Musawi et al. (2020)  |
| Nanoslot cavity resonators      | Plasmonic MIM waveguide  | 25                    | 5 nm×5 nm          | 1                | n.r\(^a\)          | n.r\(^a\)           | Dolatabady and Granpayeh (2017) |
| MZI                             | Plasmonic MIM waveguide  | 10.57                 | 62 µm×9 µm         | n.r\(^a\)        | n.r\(^a\)          | n.r\(^a\)           | Li et al. (2020)         |
| 2D PhC                          | PhC waveguide            | 14.2                  | 192 µm\(^2\)       | n.r\(^a\)        | n.r\(^a\)          | n.r\(^a\)           | Safinezhad et al. (2021) |
| Microring resonator             | Graphene                 | 15.31                 | 3 µm               | n.r\(^a\)        | 0.45 eV            | 0.50 eV             | Singh et al. (2021)      |
| Y shaped power combiner         | Plasmonic MIM waveguide  | 27.76                 | 6.2×3 µm\(^2\)     | 2.1              | 0.7e9 W/m          | 3e9 W/m            | This work                |

n.r\(^a\): not reported
logic functions in electronics. The presented design has a simplified structure that might be utilized to develop ultra-compact devices for rapid optical computing in the future.

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Data availability The authors can provide the data on request.

Code availability No source code is available for this manuscript.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

Consent to participate For this type of study formal consent is not required.

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