Bypass anode lateral IGBT on SOI for snapback suppression

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Abstract: In this letter a novel lateral insulated gate bipolar transistor with a three dimensional (3D) bypass anode design on silicon-on-insulator (SOI) is proposed and discussed. The 3D bypass anode concept makes it more effectively not only suppress the snapback effect in conducting state, but also improve the switching speed as a fast electron extraction path during turnoff without wasting the anode area. Numerical simulation results show that the proposed LIGBT structure has a 1.12 V forward voltage drop and 400 ns turnoff time at current density of 100 A/cm\textsuperscript{2}. The proposed LIGBT saves the cell area by above 30\% compared with the conventional no snapback SA-LIGBT and has about 61\% reduction in turnoff time compared with the conventional LIGBT, respectively. Mostly, the proposed LIGBT can be fabricated by the conventional SOI smart power IC process without an additional process step and mask.

Keywords: LIGBT, snapback effect, turnoff time, SOI

Classification: Electron devices, circuits, and systems

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1 Introduction

The lateral insulated gate bipolar transistor (LIGBT) on silicon-on-insulator (SOI) has been widely used in off-line power conversion, lamp ballasts, PDP scan driver, and other smart power integrated circuits (SPICs) because of its high input impedance, low on-resistance, high current handling capability, and compatibility with CMOS technologies [1]. One key development is to improve the switching performance of the LIGBT. The shorted anode structure has been proved to offer the simplest solution in many efforts [2, 3, 4]. However, the SA-LIGBT inherently exhibits the snapback effect which results from the abrupt transition between the two different operation modes (LDMOS and LIGBT modes) [5]. A very long anode geometry is thus required to suppress the snapback and it would increase the device area considerably [6]. Nowadays, various approaches have been reported to achieve fast switching speed without increasing device cell pitch, such as NPN controlled LIGBT [7], 3-D n-region-controlled anode LIGBT [8], and insulated trench collector SA-LTIGBT [9], etc. But these structures caused increasing manufacturing process complexity: triple diffusion process or additional etching process.

The aim of this letter is to present a novel three dimensional (3D) bypass SA-LIGBT on SOI to suppress the snapback effect without increasing process step and device cell pitch. The fabrication of proposed LIGBT is fully compatible with the conventional SOI power ICs process.

2 Device structure and analysis

The schematic 3D and top view of the proposed LIGBT structure on SOI is shown in Fig. 1(a) and (b), respectively. Fig. 1(c) shows its equivalent circuit in the conduction. Compared to the conventional SA-LIGBT, the proposed structure features a special anode part design along the z-direction. The p+ anode region folds the y-direction p+ region to the z-direction, resulting in a reduced cell pitch. When operating in the LDMOS mode, the flow of electron carriers bypasses the p+ anode region. This bypass path can be also designed to act as an electron extraction path during the turnoff process.

When the anode PN junction of the PNP transistor is approximately 0.7 V at 300 K then the transistor begins to conduct and the device switches from the LDMOS mode to the LIGBT mode. Thus, during the on-state, a simple expression of the turnover voltage of the snapback is given as

\[
V_F = \left(1 + \frac{R_d + R_{ch}}{R_{nb} + R_{bypass}}\right) \times V_S
\]

where \(V_F\) is the total forward voltage drop across the device, \(R_d\) is the resistance of the n-drift region, \(R_{ch}\) is the resistance of the MOSFET channel, \(R_{nb}\) is the resistance of the n-buffer region near the anode, \(R_{bypass}\) is the resistance of the bypass path to the p+ anode around the p+ anode, and \(V_S\) is the PN junction (p+/n-buffer) voltage drop (approximately 0.7 V). When the device starts to shift from LDMOS mode to LIGBT mode, \(V_F\) develops in a turnover voltage of the snapback. In the limiting case of \(V_F \rightarrow V_S\), there is no snapback effect. Hence, the extent of the snapback is determined by the ratio
of the \( (R_d + R_{ch})/(R_{nb} + R_{bypass}) \) before the transition of the operation mode. For appointed material and process condition for a special blocking voltage, \( R_d \) and \( R_{ch} \) are hard to be smaller. According to equation (1), it is therefore favorable to increase the \( R_{bypass} \) to suppress the snapback effect when the doping of the n-buffer region is fixed.

3 Results and discussion

In order to gain deeper insight into the characteristics of the proposed LIGBT, 3D numerical simulations were performed by using SILVACO [10]. Physical mechanisms included in the simulation models were Shockley-Read-Hall recombination model (SRH), auger recombination model accounting for high level injection effects (AUGER), analytic concentration dependent mobility model (ANALYTIC), lateral electric field dependent mobility model (FLDMOB), surface mobility degradation model (SURFMOB), bandgap narrowing model (BGN), and the Selberherr impact ionization model (IMPACT SELB). Carrier lifetimes were assumed to be: \( \tau_n = \tau_p = 1 \mu s \) for electrons and holes. The cell length \( L_C \) in the x-direction and the cell width \( L_Z \) in the z-direction are 35 \( \mu m \) and 10 \( \mu m \), respectively. The doping concentration of the n-drift is set to be \( 2 \times 10^{15} \) cm\(^{-3} \) for a blocking capability of 250 V. Room temperature of 300 K is used in the simulation and some other important parameters are listed in Table I.

Fig. 2 shows a comparison of the I-V characteristics of the conventional LIGBT, the conventional SA-LIGBT, and the proposed SA-LIGBT. For ease
of comparison studies, we set the all three structure cell length to be the same 35 µm in the x-direction. For the conventional SA-LIGBT and the proposed SA-LIGBT, they have the same \( l_{px} \) (3 µm) and the same \( l_{nx} \) (1 µm) in the x-direction. It is particularly worth noting that the proposed structure suppressed the snapback effect completely. But even when the current density in on-state is nearly 90 A/cm\(^2\) for the conventional SA-LIGBT, the LIGBT mode still do not start to operate and the snapback voltage is up to 11.5 V. From the Eq. (1) we know that it can suppress the snapback effect by increasing the \( R_{bypass} \). Thus, the width of the p+ anode in the z-direction is an important parameter to be designed for proper optimization.

Fig. 2. Comparison of the I-V characteristics.

![Fig. 2. Comparison of the I-V characteristics.](image)

Table I. Key parameters in device simulations

| Parameters                     | Proposed LIGBT |
|--------------------------------|----------------|
| cell length, \( L_C \)         | 35 µm          |
| cell width, \( L_Z \)          | 10 µm          |
| SOI layer thickness, \( T_{SOI} \) | 2 µm          |
| buried oxide thickness, \( B_{OX} \) | 5 µm          |
| n-drift doping, \( N_D \)      | \( 2 \times 10^{15} \) cm\(^{-3}\) |
| n-buffer doping, \( N_B \)      | \( 2 \times 10^{16} \) cm\(^{-3}\) |
| p-well doping, \( N_{PW} \)     | \( 1 \times 10^{17} \) cm\(^{-3}\) |
| p+ anode length, \( l_{px} \)  | 3 µm           |
| p+ anode width, \( d_{pz} \)   | 3–9 µm         |
| n+ anode length, \( l_{nx} \)  | 1 µm           |
| n+ anode width, \( d_{pz} \)   | 1 µm           |

Fig. 3(a) shows the influences of \( d_{pz} \) on the snapbacks. The forward voltage drop \( V_F = 1.12 \) V at 100 A/cm\(^2\) is obtained for the proposed LIGBT with no snapback. The results clearly show that the suppression of the snapback in the on-state can be effectively improved as the width of \( d_{pz} \) is increased. When \( d_{pz} = 9 \) µm, the snapback basically disappears. That is because of the increased resistance of \( R_{bypass} \) in the LDMOS conduction.
Define $\Delta V = V_{SB} - V_H$. $V_{SB}$ is the turnover voltage of snapback. $V_H$ is the minimum anode voltage after snapback. The optimized $\Delta V_s$ dependent on the p+ anode parameters in the x-direction are shown in Fig. 3(b). For the conventional SA-LIGBT design, it must increase the p+ anode length to suppress the snapback, and it still has a snapback ($\Delta V = 0.96$ V) even under the p+ anode length of 18 µm [cell length $L_C = 50$ µm shown in Fig. 3(b)]. The p+ anode length $l_{px}$ of the proposed LIGBT is keep to be 3 µm (cell length $L_C = 35$ µm) and the method of suppression snapback is just by changing the p+ anode width $d_{pz}$ in the z-direction. This makes the device more area efficient because of their small n-drift length particularly for the low-middle voltage power devices (less than 300 V). So it can be concluded from Fig. 3(b) that the proposed LIGBT saves the cell area by above 30% compared with the conventional SA-LIGBT. The degree of anode process difficulty, breakdown voltage, and Figure-of-Merits (FOM) for the proposed SA-IGBT and some new IGBTs cited are given in Table II for better comparisons.

**Table II. Key parameters in device simulations**

| Device structures                      | anode process     | breakdown voltage (V) | FOM (MW/cm²) |
|----------------------------------------|-------------------|-----------------------|--------------|
| Proposed LIGBT                         | simple            | 250                   | 5.6          |
| Conventional SA-LIGBT                  | simple            | 250                   | 0.6          |
| NPN controlled anode LIGBT [7]         | complex (triple diffusion) | 360                   | 6.0          |
| Insulated trench collector SA-LTIGBT [9] | complex (etching) | 140                   | 1.96         |

The turnover current waveforms comparison for the proposed LIGBT and the conventional LIGBT with a resistive load is shown in Fig. 4(a). The proposed LIGBT and the conventional LIGBT exhibit the turnover times of 400 ns and 940 ns, respectively. It can be concluded that the turnover time of
the proposed LIGBT is decreased by 61% compared to that of the conventional LIGBT. The bypass path around the p+ anode provides the fast extraction for electron carriers during the turnoff process. This is thus attributed to the 3D shorted anode design in the z-direction. The tradeoff performances between the forward voltage drop $V_F$ and turnoff loss $E_{\text{off}}$ obtained by varying the doping concentrations of the p+ anode are comparatively illustrated in Fig. 4(b). It is obvious that the tradeoff curve of the proposed LIGBT lies below that of the conventional LIGBT. So it shows a better tradeoff performance and lower turnoff loss.

Therefore, this new structure has advantages in terms of size scaling, reduced snap-back voltage, and improving the turnoff speed without degrading the other electrical characteristics.

4 Conclusion

A novel three dimensional (3D) bypass SA-LIGBT on SOI has been presented and investigated by numerical simulations. A snapback-free LIGBT on SOI with 35 µm cell length, 3 µm-length and 9 µm-width p+ anode, 1.12 V forward voltage drop, and 400 ns turnoff time at 100 A/cm$^2$ is obtained. As simulations show, the proposed LIGBT eliminates the snapback, saves the cell area, and shows a better tradeoff between $V_F$ and $E_{\text{off}}$ without sacrificing the other characteristics. It is thus a promising power device used in SPICs.

Acknowledgments

This work is supported by the National Science and Technology Major Project (2011ZX02706-003) and the Fundamental Research Funds for the Central Universities (ZYGX2013J043).