Small Signal Parameter Extraction and DC Simulation of Asymmetric Dual Channel AlGaN/GaN Heterojunction Field Effect Transistor

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Abstract

Objectives: This article reports extraction of small signal parameters and analysis of dc behavior of enhanced dual channel (DC) AlGaN/GaN HFET first time. Enhanced device for which small signal model proposed incorporates double channels, field plate and nucleation layer as additional feature for better reliability. Methods/Analysis: Direct method for small signal parameter extraction is employed using cold FET pinch off biasing at lower and upper frequency band. Lower frequency band for analysis is chosen to ensure extraction accuracy for parasitic capacitive elements of our proposed small signal model parameters. Also TCAD simulation environment is utilized for extensive analysis and characterization of device for dc and small signal performance. Findings: The small signal extrinsic and intrinsic parameters are extracted for the proposed device structure that can predict physical as well as RF performance correctly. Simulation results support clear insight about dc performance and functional reliability of device. Novelty/Improvements: Proposed model takes in to consideration most of the important parasitic as well as intrinsic components of device for extraction purpose. The method employed for model is capable for providing higher accuracy in comparison of other approaches. The extracted model and simulation results give clear insight about enhanced device performance in higher frequency range. The reported results are compared with latest published data and found to be in good agreement.

Keywords: Dual Channel AlGaIn/GaN HEMT, Double Channel HFET, RF Parameter Extraction, Small Signal Modeling

1. Introduction

GaN material is extensively studied as wide band compound semiconductor material and preferred for fabrication of high frequency, high temperature and high power microwave semiconductor devices due its unique material properties. These properties include higher sheet-charge density due to inherent polarization effects, better saturation velocity, good thermal conductivity and high temperature sustainability. In present era AlGaN/GaN HEMTs are highly researched compound semiconductor devices as this device can address the need for future generation microwave circuits. An accurate modeling of electrical parameters, of GaN transistor always remained a requirement of design engineers. Apart from the active device characteristics, there is an additional requirement to model the high-frequency intrinsic and extrinsic elements of devices. Parasitic elements include layout inductances, resistances skin and proximity effects. These parasitic elements can be packaging dependent and difficult to be modeled readily within a generic GaN transistor model. Specific device structures may need, not only an accurate model of the active elements, but also, a high frequency model that may include all the parasitic interconnect elements of devices. Accuracy of the extracted parameter will depend on complexity of model and approach used by the scientist.
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Recently dual channel dual material gate AlGaN/GaN HEMT model has been analyzed for potential and electric field distribution. An improved T-Shaped gate double heterojunction AlGaN/GaN/InGaN/GaN HEMT based LNA has been fabricated and analyzed for small signal parameters. The one of the detailed approach for small signal model extraction using cold FET was also proposed. Many other researchers have also explored techniques based on AlGaN/GaN and AlGaAs/GaAs material system and devices. Mainly modeling approaches can be classified in to three important types as (a) all parameters optimization method, (b) partial optimization method and (c) direct extraction method. Since extraction accuracy of the parameter optimization method is heavily dependent on the assumed initial values of model and further the method of optimization. At narrow frequency band of measurement this technique may give large variations in measured and modeled parameters. This inaccuracy problem at lower frequency ranges was resolved by direct determination method successfully and has been suggested first time by Minasian that was later modified and in. In our proposed article the direct extraction method is applied for parameter extraction of DC AlGaN/GaN HFET due its inherent advantages.

2. Model Description

2.1 Device Structure

Dual channel dual material gate Al$_{0.3}$Ga$_{0.7}$N/ GaN HFET schematic structure is shown in Figure 1. Schottky junction between gate metal and UID Al$_{0.3}$Ga$_{0.7}$N cap layer of 3nm thickness is formed. A 15nm thick n-Al$_{0.3}$Ga$_{0.7}$N barrier layer is used to form hetero-interface with the cap layer. Barrier layer forms hetero-junction with 4nm UID Al$_{0.3}$Ga$_{0.7}$N spacer layer and used to reduce impurity scattering. Under spacer layer 6nm thick UID GaN upper channel layer is formed that follows 21 nm n-Al$_{0.3}$Ga$_{0.7}$N layer in which Al mole fraction grading (m) is applied from 3 to 6 percent from bottom to top. Under this graded layer a 2.5µm UID GaN lower channel layer formed followed by 3nm thick nucleation layer. These all epitaxial layers are laid on sapphire substrate that can withstand higher temperature of device. A nucleation layer is sandwiched between sapphire substrate and GaN layer to obtain good matching between GaN lattice profiles. Field plate provides better distribution of field and enhances device reliability.

Figure 1. Cross sectional schematic of asymmetric DC Al$_{0.3}$Ga$_{0.7}$N/GaN HFET incorporating single finger 1X100 square micrometer area.

2.2 Small Signal Model Formulation

Figure 2 represents small signal equivalent model of device. $R_g$, $R_s$ and $R_d$ represent parasitic resistances of gate, source and drain respectively. $L_s$, $L_d$, $L_g$ represent source, drain, gate electrodes inductances respectively. $C_{pd}$ and $C_{pg}$ and $C_{pgd}$ represent device contact pad capacitances between drain-source, gate-source and gate-drain respectively. $g_{ds}$ and $g_m$ represent drain conductance and transconductance of device. $V_{gs}$ in small signal model represent current generator in the output circuit, where $V_{gs}$ represents as gate to source voltage. Gate capacitances with a phase shift of $e^{-j\omega \tau}$ represent transit time ($\tau$) through the velocity saturated regions of the 2DEG-channels. The $\omega$ is angular frequency in rad/sec of the applied small RF signal at gate terminal.
Figure 2. Small signal equivalent circuit model of DC AlGaN/GaN HFET.

Figure 3. On wafer small signal equivalent circuit representation.
2.3 Parameters Extraction Method

For parameter extraction, the direct method is used as suggested\textsuperscript{24} and later on modified\textsuperscript{16}. Initially S-parameter extraction is carried out for shunt and series extrinsic elements of device under pinch off mode of biasing keeping frequency with in 5GHz range. These measured s-parameters are further transformed into Y-parameters and then into Z-parameters successfully in order to obtain values of all the series and shunt parasitic elements. On de-embedding of all the parasitic elements, the intrinsic Y-parameters are determined for device. After this all the intrinsic elements are derived by separating real and imaginary parts of intrinsic Y-parameters and then putting values in model expressions.

Figure 3 demonstrates on wafer visualization of small signal equivalent circuit. A physical device analogy is used demonstrated by the figure to represent basic circuit elements on wafer. Figure 4 shows block diagram of test circuit for extraction of s-parameters. This figure depicts a two port matching lossless output and input network for accurate extraction of parameters. In the circuit $E_s$ and $Z_s$ represents source potential and source impedance respectively. $Z_L$ represents load impedance terminated through matching output network. $P_A$, $P_i$, $P_o$ and $P_L$ represent available power, input power, output power and load power respectively.

\begin{align}
\text{Im}(Y_{11}) &= j\omega(C_{pg} + C_{gd0} + C_{gd} + C_{pgd}) \\
\text{Im}(Y_{12}) &= \text{Im}(Y_{21}) = -j\omega(C_{gd0} + C_{pgd}) \\
\text{Im}(Y_{22}) &= j\omega(C_{ds0} + C_{pd} + C_{gd0} + C_{pgd})
\end{align}

Figure 5. Small signal equivalent circuit as cold FET under pinch off biasing.

Figure 6. Imaginary Y-parameters vs. frequency graph.

2.4 Extraction of Extrinsic Parameters

The extrinsic elements are extracted carefully from imaginary Y-parameters under pinch-off condition called $V_{\text{pinch-off}}$ (means keeping $V_{gs} < -V_p$ and $V_{ds}=0V$). Now under pinch of biasing, the equivalent voltage controlled current source, forming intrinsic part of device, is disabled for extraction of parasitic elements purposely. Low frequency in the range of 5 GHz is selected so that the whole circuit under pinch off behaves as a capacitive network shown in Figure 5. Under stated condition following equations appropriately describe the relationship between extrinsic capacitances as imaginary parts of the Y-parameters.

\begin{align}
\text{Im}(Y_{11}) &= j\omega(C_{pg} + C_{gd0} + C_{gd} + C_{pgd}) \\
\text{Im}(Y_{12}) &= \text{Im}(Y_{21}) = -j\omega(C_{gd0} + C_{pgd}) \\
\text{Im}(Y_{22}) &= j\omega(C_{ds0} + C_{pd} + C_{gd0} + C_{pgd})
\end{align}
\[ C_{ds0} = 12C_{pd} \] (4)

The proposed device is asymmetric as gate is closer to source than drain in the ratio of 1:1.5. This kind of device structure supports better functionality and reliability option\(^2\). Hence

\[ C_{gs0} = 1.5C_{gd0} \] (5)

It is simplifying feature to consider shape of all pad connections similar for our model. This gives

\[ C_{pg} = C_{pd} = C_{pgd} \] (6)

Figure 7. Small signal circuit under pinch-off biasing at normal frequency.

At zero \( V_{ds} \) with gate forward biased \( (V_{gs} \geq 0V) \), small signal equivalent circuit is reduced as in Figure 7. In this condition gate leakage current \( (I_g) \) flows and internal device capacitances are shunted with conductance open circuited. The following simplified equations of Z-parameters are valid.

\[ Z_{\omega} = \frac{R_c + \frac{1}{1+c} + \frac{K}{qL_s} + j\omega(L_s + L_y)}{C_{gs} + j\omega C_{gsf}} + \frac{1}{j\omega C_{gsf}} \] (7)

\[ Z_{\omega 2} = Z_{\omega 1} + \frac{R_c}{c} + j\omega L_s + \frac{1}{j\omega C_{gsf}} \] (8)

\[ Z_{\omega 3} = Z_{\omega 2} + \frac{R_c}{c} + j\omega(L_s + L_y) + \frac{1}{j\omega C_{gsf}} + \frac{1}{j\omega C_{gsf}} \] (9)

Where \( R_c \) represents channel resistance and ‘c’ determines ratio of channel resistance between gate to drain and gate to source i.e \( (c=R_{cd}/R_{cg}) \). Due to proposed asymmetric device structure as in Figure 1 the value of \( c \) is 1.5 and it is based on ratio of source-gate and drain-gate separation. \( C_{df} \), \( C_{gf} \) and \( C_{sf} \) in Figure 7 represent fringing capacitances resulting at drain, gate and source terminals respectively in cold FET high frequency equivalent circuit. Also \( \eta kT/qL_s \) in equation gives the differential resistance of the Schottky diode. In this expression \( \eta \), \( K \) and \( T \) represent ideality factor of diode, Boltzmann constant and absolute ambient temperature respectively. Now by transforming Y-parameters to Z-parameters, \( R_g \), \( R_s \) and \( R_d \) can be extracted safely from the \( \text{Re}(Z_{ij}) \) expressions.

By multiplying \( \omega \) by imaginary parts of impedances, following expressions are obtained

\[ \text{Im}(\omega Z_{\omega 1}) = \omega^{2}(L_s + L_y) - \frac{1}{C_{gsf}} - \frac{1}{C_{gsf}} \] (10)

\[ \text{Im}(\omega Z_{\omega 2}) = \omega^{2}L_s - \frac{1}{C_{gsf}} \] (11)

\[ \text{Im}(\omega Z_{\omega 3}) = \omega^{2}(L_s + L_y) - \frac{1}{C_{gsf}} + \frac{1}{C_{gsf}} \] (12)

Figure 8. Variation of \( \omega \text{Im}(Z_{\omega}) \) with \( \omega^2 \).

The \( \omega \text{Im}(Z_{\omega}) \) versus \( \omega^2 \) plot is shown in Figure 8. Slope of these curves can be used to extract values of \( L_g \), \( L_d \) and \( L_s \) accurately. The imaginary part of the Z-parameters increases linearly with frequency but real part is independent from frequency variations. The value of \( R_c \) is determined by forming following equations

\[ \text{Re}(Z_{\omega 2}^{pinch-off}) = R_c + R_d \] (13)

Analyzing equation it is clear that

\[ \text{Re}(Z_{\omega 2}) = R_c + R_d + R_c \] (14)
\[ R_c = \text{Re}(Z_{22}) - \text{Re}(Z_{22\text{pinch-off}}) \]  

### 2.5 Intrinsic Parameters Extraction

The intrinsic part of device represent virtual circuit that can be described by the following Y-parameters

\[ Y_{11\text{int}} = \frac{\omega^2 C_{gd}^2 R_{gd} A}{B} + \frac{\omega^2 C_{gs}^2 R_{gd}}{B} + j\omega \left( \frac{C_{gs} + C_{gd}}{A} \right) \]  

\[ Y_{12\text{int}} = -\frac{\omega^2 C_{gd}^2 R_{gd}}{B} - j\omega \frac{C_{gd}}{B} \]  

\[ Y_{21\text{int}} = g_am e^{-j\omega} - \frac{\omega^2 C_{gs}^2 R_{gd}}{B} - j\omega \frac{C_{gd}}{B} \]  

\[ Y_{22\text{int}} = g_{ds} + \frac{\omega^2 C_{gd}^2 R_{gd}}{B} + j\omega \left( C_{ds} + \frac{C_{gd}}{B} \right) \]  

where \( A = 1 + l^2 \)  

\( l = \omega C_{gs} R_{gd} \)  

\( B = 1 + m^2 \)  

\( m = \omega C_{gs} R_{gd} \)  

Therefore, the value of individual intrinsic parameter can be derived from equation to by separating real and imaginary parts of \( Y_{11\text{int}}, Y_{12\text{int}}, Y_{21\text{int}} \) and \( Y_{22\text{int}} \) and using following expressions

\[ C_{gd} = -(1-m^2) \frac{\text{Im}(Y_{12\text{int}})}{\omega} \]  

\[ R_{gd} = \frac{v}{(1+m^2)\text{Im}(Y_{12\text{int}})} \]  

\[ C_{gs} = (1+l^2) \frac{\text{Im}(Y_{11\text{int}}) + \text{Im}(Y_{12\text{int}})}{\omega} \]  

\[ R_{gs} = \frac{l-1-l^2}{1-l^2} \text{Im}(Y_{11\text{int}} + Y_{12\text{int}}) \]  

\[ g_m = |Y_{21\text{int}} - Y_{12\text{int}}| \]  

\[ r = -\frac{1}{\omega} \arctan \left( \frac{\text{Im}(Y_{21\text{int}} - Y_{12\text{int}})}{\text{Re}(Y_{21\text{int}} - Y_{12\text{int}})} \right) \]  

\[ C_{ds} = \frac{\text{Im}(Y_{22\text{int}} + Y_{12\text{int}})}{\omega} \]  

\[ g_{ds} = \text{Re}(Y_{22\text{int}} + Y_{12\text{int}}) \]

These extracted parameters are listed separately in following Table 1 and Table 2.

#### Table 1. Extracted Intrinsic Parameters at \( V_{gs}=-1V \) and \( V_{ds}=10V \)

| Parameter | Value |
|-----------|-------|
| \( C_{gd} \) | 1.82fF |
| \( C_{gs} \) | 23.56fF |
| \( C_{ds} \) | 4.18fF |
| \( R_{gd} \) | 440Ω |
| \( R_{gs} \) | 15Ω |
| \( R_{ds} \) | 9mS |
| \( g_m \) | 380mS/mm |
| \( r \) | 0.51pS |

#### Table 2. Extracted extrinsic parameters at \( V_{gs}=-1V \) and \( V_{ds}=10V \)

| Parameter | Value |
|-----------|-------|
| \( L_g \) | 40pH |
| \( L_s \) | 49pH |
| \( L_d \) | 6pH |
| \( R_g \) | 15Ω |
| \( R_s \) | 21Ω |
| \( R_d \) | 38.6Ω |
| \( C_{pg} \) | 21fF |
| \( C_{pd} \) | 25fF |
| \( C_{pgd} \) | 3fF |
| \( C_o \) | 26fF |
| \( C_i \) | 23fF |

### 2.6 Derivation of R F Performance Metrics

The important figure of merits for RF performance evaluation are power gain, maximum power gain, transducer power gain, stability factor, cutoff frequency and maximum oscillation frequency. These performance metrics can be derived from scattering parameters using following equations directly.

**Transducer power gain (\( G_T \))**

\[ G_T = 10 \log \left( \frac{P_L}{P_A} \right) \text{dB} \]  

**Unilateral transducer power gain (\( G_{TU} \))**:

\[ G_{TU} = 10 \log \left( \frac{P_L}{P_A S_{21}=0} \right) \text{dB} \]  

(32)  

(33)
Maximum unilateral transducer power gain ($G_{TUM}$): For unconditional stability it is represented as

$$G_{TUM} = 10 \log \left( \frac{|S_{21}|^2}{1 - |S_{11}|^2(1 - |S_{22}|^2)} \right) \text{dB} \quad (34)$$

Maximum unilateral power gain ($G_{UM}$): It is largest of all gains and represented as

$$G_{UM} = 10 \log \left( \frac{1}{k} \left( \frac{S_{21}}{S_{12}} \right)^2 \left( \frac{k \pm \sqrt{k^2 - 1}}{k \pm \sqrt{k^2 - 1}} \right)^2 \right) \text{dB} \quad (35)$$

Available power gain ($G_A$): 

$$G_A = 10 \log \left( \frac{P_{d}}{P_{a}} \right) \text{dB} \quad (36)$$

Maximum available gain ($G_M$): 

$$G_M = 10 \log \left( \frac{S_{21}}{S_{12}} \left( k \pm \sqrt{k^2 - 1} \right) \right) \text{dB} \quad (37)$$

where $k$ represents stability factor as 

$$k = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{21}|^2 - |S_{22}|^2}{2|S_{12}|} \quad (38)$$

Maximum stable gain ($G_{MS}$): 

$$G_{MS} = 10 \log \left( \frac{|S_{21}|}{|S_{12}|} \right) \text{dB} \quad \text{for } k=1 \quad (39)$$

Current gain [$H_{21}$]: It is represented as

$$|H_{21}| = 10 \log \left( \frac{2S_{12}}{|(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}|} \right) \text{dB} \quad (40)$$

Cut off frequency ($f_c$): Frequency at which current gain rolls off to 0 dB is represented as

$$f_c = \frac{g_m}{2\pi(C_{gs} + C_{gd})(1 + (R_s + R_d)g_{ds}) + \frac{g_m}{2}\frac{R_s + R_d}{g_{ds} + 2\pi f_c C_{gd}R_s}} \quad (41)$$

Maximum oscillation frequency ($f_{max}$): It is represented as

$$f_{max} = \frac{f_c}{2\pi((R_s + R_d)g_{ds} + 2\pi f_c C_{gd}R_s)} \quad (42)$$

3. Results and Discussions

After modeling small signal equivalent circuit for parameter extraction, an extensive simulation of enhanced device structure is carried out using ATLAS TCAD device simulation tool\textsuperscript{29,30}. The simulation results shown in following Figure 9, Figure 10, Figure 11 and Figure 12 represent logarithmic electric field contour, potential contour, electron concentration contour and epitaxial structure contour of device respectively. These contour provide various internal parameters of device such as electric field distribution, potential distribution using color representation and very useful for analysis.

The output current voltage ($I_d$ vs. $V_{ds}$) characteristics of simulated device and experimental\textsuperscript{12} device for four set of gate-to-source voltages ($V_{gs}$) are shown and com-

![Figure 9. Simulated electric field contour at 10 volts $V_{ds}$.](image-url)
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Figure 10. Simulated device potential contour at 10 volts $V_{ds}$.

Figure 11. Simulated device electron concentration contour at 10 volts $V_{ds}$.

Figure 12. Simulated structure contour at 10 volts $V_{ds}$. 
pared in Figure 13 and Figure 14. It is clearly shown that device provides saturation current of 900mA/mm up to 12 volts range (approx) for +1V \( V_{gs} \) under enhancement mode of operation. Current reduces proportionately with application of lower gate to source biases \( (V_{gs}) \) in the step of -1 V. Experimental device also follow closely to simulated results. The device works in depletion mode when gate bias is reduced below zero volt. The result shows that device is capable to withstand higher current carrying capability due to its dual channel structure as evident in the plot. Figure 14 shows simulated as well as experimental results for input or transfer characteristics of device. Gate voltage has good control over drain current is clearly visible in the characteristic plot. Device has a threshold voltage of -5.5 V. The initial current at smaller \( V_{gs} \) is comparatively more contributed by lower channel but, at higher \( V_{gs} \) upper channel is switched on and start contributing additional current to the device.

The DC AlGaN/GaN HFET device stability analysis has been done with the help of polar plot and smith charts. Figure 15 shows simulated scattering parameter plot where parameters follow their respective capacitive and inductive loops hence showing that device is stable for microwave frequency range up to 90 GHz. The model and experimental \( S_{11} \) plot is shown in Figure 16. It give good conformity and consistency with experimental results of similar devices32. Similarly \( S_{22} \) model and experimental smith chart is compared in Figure 17 giving good match with experimental counterpart.

Figure 13. Current voltage \( (I_d \text{ vs. } V_{ds}) \) characteristics simulated (lines) experimental (symbol).

Figure 14. Transfer \( (I_d \text{ vs. } V_{gs}) \) characteristics and transconductance \( (g_m \text{ vs. } V_{gs}) \) plot simulated (line) experimental (symbol).

Figure 15. Simulated polar plot of \( S_{11}, S_{22}, S_{12} \) and \( S_{21} \) at 10 V \( V_{ds} \) and -1 V \( V_{gs} \), sweep frequency \( f_{\text{start}}=1\text{GHz} \) and \( f_{\text{stop}}=90\text{GHz} \).

The input and output reflection coefficient \( (S_{11} \text{ and } S_{22}) \) are plotted at a gate voltage of -1 V and frequencies range from 1GHz to 90 GHz. It is evident in the plots that the input and output impedances of the two-port network based device proposed in the manuscript, are capacitive in nature. At the lowest input frequency the input reflection coefficient is \( S_{11}=+1 \). It further represents maximum
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Figure 16. Scattering parameter ($S_{11}$) on smith chart model (red symbols) and experimental (black symbols) at 10 V $V_{ds}$ and -1 V $V_{gs}$, sweep frequency $f_{\text{start}}=1\,\text{GHz}$ and $f_{\text{stop}}=90\,\text{GHz}$.

Figure 17. Scattering parameter ($S_{22}$) on smith chart model (red symbols) experimental (black symbols) at at 10 V $V_{ds}$ and -1 V $V_{gs}$, sweep frequency $f_{\text{start}}=1\,\text{GHz}$ and $f_{\text{stop}}=90\,\text{GHz}$.

Figure 18. Scattering parameter ($S_{12}$) on smith chart model (red symbols) and experimental (black symbols) at at 10 V $V_{ds}$ and -1 V $V_{gs}$, sweep frequency $f_{\text{start}}=1\,\text{GHz}$ and $f_{\text{stop}}=90\,\text{GHz}$.

Figure 19. Scattering parameter ($S_{21}$) on smith chart model (red symbols) and experimental (black symbols) at at 10 V $V_{ds}$ and -1 V $V_{gs}$, sweep frequency $f_{\text{start}}=1\,\text{GHz}$ and $f_{\text{stop}}=90\,\text{GHz}$.

In Figure 18 and Figure 19, we have plotted and compared the model and measured values of the transmission coefficients ($S_{21}$) and ($S_{12}$) for a gate bias of -1 V and fre-
quencies between 1GHz and 90 GHz. Analysis shows that the transmission coefficients \( S_{11} \) and \( S_{21} \) both move towards clockwise direction in the circle of inductances and follow the inductive loops with rise in frequency on Smith chart. This proves the stability of device up to 90 GHz of frequency. On comparison the model values are found to be within the permissible range hence shows accuracy in prediction. The device important gains are plotted as a function of frequency at a gate bias of \( V_{gs} = -0.5\text{V} \) in Figure 20. The device unilateral transducer gain, maximum unilateral transducer gain, maximum stable gain and current gain are compared in Figure 20. The gains obtained from the proposed device model are also compared with simulated gains and experimental results\(^2\) and found to be within the limit of tolerance (±.5%). It is clearly depicted in plot that the gains decrease with the rise in frequency and the cut-off frequency \( (f_c) \) occurs at 34 GHz when current gain roll off to zero dB. Also maximum oscillation frequency is obtained at 88GHz when transducer unilateral power gain rolls off up to zero dB point which is obtained by extrapolation of trend line in the plot.

![Figure 20. Gains vs. frequency graph model (lines) simulated (symbols).](image)

### 4. Conclusions

The derived model as discussed above gives maximum oscillation frequency \( (f_{\text{max}}) \) of 88 GHz and cut-off frequency \( (f_c) \) of 34 GHz. Important RF performance metrics studied from the model include current gain \( |H_{21}| \), transducer power gain \( G_{11} \), available power gain \( G_{21} \), unilateral transducer power gain \( G_{1U} \), maximum stable gain \( G_{MS} \), transconductance \( g_m \), output conductance \( g_{ds} \), Stern stability factor \( (k) \) and time delay \( (\tau) \) for the proposed device structure. On the basis of above results and discussions it can be concluded that extracted small signal parameters and dc simulation results for enhanced device structure are consistent with physical behavior of device. Important figure of merits derived from the model parameters are found to be accurate and in close conformity with recently published experimental data.

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