Nonlinear distortion signal generation and THD measuring device

Jiaming Zhang*
School of Information Engineering, Wuhan University of Technology, Wuhan, China

*Corresponding author e-mail: giraffe@whut.edu.cn

Abstract. In order to generate nonlinear distortion when the amplifiers work in the nonlinear region, the system uses the transistor amplifiers to combine the analog switch and MCU to realize nonlinear distortion signal generation and THD (Total Harmonic Distortion) measurement device. The system is mainly composed of fixed gain amplifier circuit, multi-type signal selection circuit, class A and B complementary symmetric circuit, analog switch and microcontroller. The input signal is fixed as a 1KHz, 20mVp-p sinusoidal signal. Based on the influence of quiescent operation point on the common emitter amplifier circuit and the characteristics of Type B push-pull circuit, the analog switch is turned on or off by pressing the button of MCU to adjust the static working point and circuit structure to realize output of different types of signals. THD was calculated by sampling ADC inside MCU and FFT processing. The experimental results show that the system can successfully output sinusoidal signals and four kinds of nonlinear distortion signals (top distortion, bottom distortion, bidirectional distortion and cross-over distortion), and the peak-to-peak values are all greater than 2Vp-p. THD measurement error is less than 0.6%, which can achieve a more accurate measurement of total harmonic distortion.

Keywords: Nonlinear distortion, Total Harmonic Distortion, FFT.

1. System scheme design
The system provides a fixed gain by the front amplifier circuit; then it enters a multi-type signal selection circuit, controls the interruption of analog switch by key operation STM32, and enables the common emitter circuit to connect resistors of different resistance values to change the static working point and amplification multiples, and outputs different types of signals. Finally, through class A and B complementary symmetric circuit output, the circuit chooses whether the bias of the base is access or short circuit by analog switch to determine whether the output signal has cross-distortion. In the total harmonic distortion measurement, because the voltage sampled by ADC is not more than 3.3V positive voltage, the signal amplitude of the front output is large and there is a negative voltage to meet the requirements of peak output signal. Therefore, the pre-processing is carried out by the follower combined with the bias of the divider circuit, and the results of calculation are displayed. The entire system design is shown in figure 1.
2. Theoretical analysis and calculation

2.1. Fixed gain amplifier circuit

According to the design requirements, the input signal of 20mVp-p and the output signal of 2Vp-p are required, so the system needs at least 100 times gain. In order to obtain sufficient gain and reduce the influence of noise, a two-stage circuit is selected. The first stage provides about 14 times gain for a fixed gain amplifier circuit, the second stage is a multi-type selection circuit, and the second stage is designed with more than 23 times the gain for all types of signal circuits. The first level structure is shown in figure 2.

Among them, T1 tube is a common emitter amplifier circuit, and T2 transistor is an emitter follower circuit. The purpose is to reduce the output impedance and gain loss. The gain calculation is shown in formula 1.

$$A_v \approx \frac{R_c}{R_{g1}}$$  \hspace{1cm} (1)

2.2. Theoretical analysis and calculation of top distortion

As shown in (a) in figure 3, the waveform diagram when the cut-off distortion occurs. It can be seen that the voltage waveform distortion of the output signal appears at the top due to the common emitter circuit of NPN type transistor.

The circuit is designed as a base divider common emitter amplifier, and its structure is shown in figure 2. In order to keep the output signal undistorted, the triode needs to work in the amplification area, that is to find a suitable static working point to meet the conditions shown in formula (2)-(3)
On the contrary, to output the distorted signal, the signal can be distorted actively by selecting a specific static working point. The parameters of static working point $Q$ are calculated by formula (4)-(6)

$$\begin{align*}
V_{BQ} & \approx \frac{R_{b2}}{R_{b1} + R_{b2}} V_{CC} \\
I_{CQ} & \approx \frac{V_{BQ} - V_{BEQ}}{R_e} \quad (V_{BEQ} = 0.6 \sim 0.7V) \\
V_{CEQ} & = V_{CC} - I_{CQ} \left( R_e + R_v \right)
\end{align*}$$

According to formula (4)-(6), $I_{CQ}$ and $V_{CEQ}$ have negative and positive correlation with $R_{b1}/R_{b2}$ respectively. Therefore, the static operating point can be reduced by increasing $R_{b1}$. Due to the selection of lower static operating point $Q$, $V_{BEQ}$ and $I_{BQ}$ are too low, that is, transistors will enter the cut-off region in part of the time near the peak value of the positive half cycle of the AC signal, resulting in the top distortion.

2.3. Theoretical analysis and calculation of bottom distortion

"Bottom distortion" is the saturation distortion of NPN type transistor common emitter circuit. The saturation distortion waveform is shown in figure 3 (b). By reducing $R_{b1}$ and selecting a higher static operating point $Q$, $V_{BEQ}$ and $I_{BQ}$ are too high, that is, transistors will enter the cut-off region in the peak part of the negative half cycle of the AC signal, causing waveform distortion, that is saturation distortion ("bottom distortion").

2.4. Theoretical analysis and calculation of Bidirectional distortion

For the input signal amplitude has been determined, in order to make the triode produce bidirectional distortion signal, we can adjust the circuit to make the transistor work in the amplification area, reduce $R_e$ and increase the circuit magnification. The amplitude of the amplified signal increases to the peak

$$(a) \quad \text{Top distortion waveform} \quad (b) \quad \text{Bottom distortion waveform}$$

**Figure 3.** Two kinds of waveform distortion
value, which exceeds the amplification region of the transistor output characteristic curve, enters the saturation region and the cut-off region, so the bidirectional distortion occurs.

2.5. Theoretical analysis and calculation of Crossover distortion

Crossover distortion is a special distortion of class B push-pull amplifier. Since the circuit has no base bias, the base voltage of the two triodes is equal. When $V_i$ is between $\pm 0.7V$, T1 and T2 are in the cut-off state. In the transition between positive and negative half cycle, about 1.4V input signal is not amplified ($0.7V$ for positive and negative half cycle), and the output is the sum of the transmitting junction voltages of the two transistors, namely crossover distortion.

2.6. THD analysis and calculation of Crossover distortion

THD (Total Harmonic Distortion) represents the degree of harmonic distortion of the input signal, that is, when the input and output characteristics of the circuit are nonlinear, harmonic components will be generated. Formula (7) shows the calculation formula of THD:

$$\text{THD} = \left( \frac{D_2^2 + D_3^2 + \ldots + D_n^2}{D_1} \right) \times 100\%$$

Among them, D1 is the amplitude of the fundamental component, D2 is the amplitude of the second harmonic component, D3 is the amplitude of the third harmonic component, and Dn is the amplitude of the Nth harmonic component.

3. Hardware circuit design

The circuit diagram of each part of the system is shown in figure 4.

![Circuit Diagram](image)

(a) Fixed gain amplifier

The fixed gain amplifier circuit is designed as shown in figure 4 (a). There will be at least 1.4V voltage loss due to crossover distortion. In order to make the peak value of system output signal not less than $2V_{p-p}$, 8V single power supply is selected as the power supply. According to the design principle, R6 and R7 are selected as $23K$ and $8K$ respectively to stabilize the static operating point. R10 and R8 provide about 15 times gain for 3K and 200Ω respectively. Q3 and R11 are designed to reduce the output impedance and gain loss.

(b) Multi type signal selection circuit
According to the selection scheme, the circuit is shown in figure 4 (b). Based on the common emitter circuit, perform the following operations:
(1) Access R12, R13, R16, output no distortion waveform, gain of 23 times;
(2) When RB1 is increased and R14 is connected, the static working point is reduced, and the output signal produces cut-off distortion (top distortion);
(3) When RB1 is reduced and R15 is connected, the static working point is increased, and the output signal produces saturation distortion (bottom distortion);
(4) Increase the magnification, that is, access R12, R19, this stage will produce 63 times of gain, the output signal bidirectional distortion.
(c) Crossover distortion generation circuit
According to the scheme, the circuit for generating crossover distortion is shown in figure 4 (c). Based on the push-pull circuit of class A and B, the emitter junction of two triodes is short circuited, which is equivalent to the diode as the base bias to overcome the crossover distortion. When it is necessary to output crossover distortion, the analog switch is closed. At this time, the circuit is a push-pull circuit of class B, which outputs the crossover distortion signal. In order to ensure that the circuit can produce crossover distortion, the internal resistance of the selected analog switch should be small, so that the voltage at both ends is less than 1.4V.

4. Software design
The program flow chart is shown in figure 5. After the system turns on the power supply, it initializes each module first; according to the selected key to control the analog switch, the hardware is connected to the corresponding circuit; the ADC sampling timer is turned on for DMA data transmission; the FFT function in DSP library provided by arm is used to extract the amplitude of each harmonic component; the harmonic component is calculated by formula (7); a new round of sampling is conducted and the measurement results are displayed.

![Program flow chart](image)

**Figure 5.** Program flow chart

5. Test result
The total harmonic distortion of sinusoidal signal is 2.81% and no obvious distortion is observed. Other signal distortion shapes conform to the theory. According to the test results, the amplitudes of the five kinds of measurement signals are all greater than 2Vp-p, which meets the design requirements;
the total harmonic distortion error of all kinds of signals measured by the system is less than 0.6%, and the highest is 0.14%. This is because the professional instrument measures the 50th harmonic, while the system only measures the 5th harmonic. The overall performance of the system is excellent. The test results are shown in Table 1.

Table 1. Test results

|                        | Sinusoidal | Top distortion | Bottom distortion | Bidirectional distortion | Crossover distortion |
|------------------------|------------|----------------|-------------------|--------------------------|----------------------|
| peak-to-peak value (Vp-p) | 3.56       | 2.56           | 2.80              | 7.04                     | 2.10                 |
| THD of System (%)      | 2.80       | 14.16          | 18.98             | 30.12                    | 19.05                |
| THD of Instrument (%)  | 2.81       | 14.18          | 19.09             | 30.29                    | 19.08                |
| THD Error (%)          | 0.35       | 0.14           | 0.58              | 0.56                     | 0.16                 |

6. Conclusion

The system consists of fixed gain amplifier circuit, multi type signal selection circuit, class A and B complementary symmetrical circuit, analog switch and microcontroller, which constitute the nonlinear distortion signal generation and THD measurement device. The core principle of changing the signal is to change the static operating point and the amplification factor to actively affect the working area of the transistor. Finally, the required five kinds of signals are successfully output, and the error is less than 0.6% under the premise that the system measures the fifth harmonic.

References

[1] Kasinski K, Zubrzycka W. Overview of microelectronic circuits designed at agh university for the cbm experiment [C]. Acta Physica Polonica B, 2020, 13(4):885-891.
[2] Yang L, Song K. Research on Recovery of Clipping and HPA Nonlinear Distortion Based on Compressive Sensing in OFDM Systems[J]. Tien Tzu Hsueh Pao/Acta Electronica Sinica, 2018, 46(5):1078-1083.
[3] Zhao S, Wang C, Bian X. Research on harmonic detection based on wavelet threshold and FFT algorithm[J]. Systems Science and Control Engineering, 2018, 6(3):339-345.
[4] Ingale R. Harmonic analysis using FFT and STFT[J]. International Journal of Signal Processing, Image Processing and Pattern Recognition, 2014, 7(4):345-362.
[5] Umehira M, Tanabe M. Performance analysis of overlap FFT filter-bank for dynamic spectrum access applications[C]. 2010 16th Asia-Pacific Conference on Communications. APCC, 2010:424-428.
[6] Cerdeira A, Aleman MA, Estrada M, et al. Integral function method for determination of nonlinear harmonic distortion[J]. Solid-State Electronics, 2004, 48(12):2225-2234.
[7] Sefa I, Battal F. A harmonic analysis using parallel computing[C]. 2015 23rd Signal Processing and Communications Applications Conference. IEEE, 2015:1965-1968.