A complete analytical potential based solution for a 4H-SiC MOSFET in nanoscale

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Abstract
Analytical modeling with a verified simulation setup of surface potential, threshold voltage and electric field for a 4H-SiC MOSFET is presented to make enquiries about the short channel effects. The two-dimensional (2D) Poisson equation is used to achieve the model for surface potential. The 2D position equations have been solved by using four boundary conditions. The detail of the model is appraised by the various MOSFET parameters such as silicon carbide thickness, body doping concentration, and gate oxide influencing the electric field, channel potential and threshold voltage. The outcome shows that this model can reduce the short channel effects, drain induced barrier lowering and advance the sub-threshold fulfillment in nanoelectronic applications as compared to silicon MOSFETs. By comparing the model results with the 2D device simulations the veracity of the suggested 2D analytical model is proven.

Keywords: MOSFET, 4H-SiC, short channel effects, 2-dimensional modeling

Classification numbers: 2.07, 3.02, 5.01, 6.01

1. Introduction
Silicon carbide (SiC) was accidentally discovered in 1890 by E G Acheson, an assistant to Thomas Edison [1]. SiC is a compound semiconductor and is a mixture of silicon and carbon with the chemical formula SiC. Silicon is covalently bonded with carbon. In 4H-SiC, 4H is written in the Ramsdell classification scheme where the number indicates the layer and the letter indicates the Bravais lattice [2]. That means in a 4H-SiC structure four hexagonal layers of SiC are present. SiC exists in a kind of polymorphic crystalline building known as a polytype, e.g. 3C-SiC, 4H-SiC, 6H-SiC [2]. Presently 4H-SiC is usually preferred in power device manufacturing. SiC is a wider band-gap (Eg) material with Eg = 3.3 eV [3] as compared to silicon (Eg = 1.1 eV). Hence SiC has a band-gap three times higher than silicon. Due to its large bandgap, it has higher blocking voltage [3]. SiC is the most rising substrate for power MOSFETs and other power devices due to its high blocking voltage, great operating temperature, and admirable thermal conductivity. 4H-SiC MOSFETs are the power MOSFETs devices that have low switching losses and that can deliver low conduction with high breakdown voltages [4]. At the present time, SiC power MOSFETs with breakdown voltages from 500–1500 V [3] are readily available. SiC devices can also be made to have a much thinner drift layer, and greater doping concentration, i.e. the breakdown area for SiC is 2.4 MV cm\(^{-1}\) compared to silicon that has a breakdown discipline of 0.25 MV cm\(^{-1}\) [3]. That means the breakdown field for silicon is ten times less than SiC [4]. Electron mobility (\(\mu\)) for SiC is 950 cm\(^2\) V\(^{-1}\) s\(^{-1}\) [4] compared to silicon, \(\mu = 1400\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) [5]. This analogy shows that electron mobility for SiC is significantly less as compared to silicon. The continuous shrinkage of the device may require the attainment of excessive packing density and higher efficiency. However, the devaluation of the device dimensions in all forms decreases the performance that increases the high short channel effects. Compressing the bulk MOSFET into a nanometer MOSFET causes compelling challenges and difficulties with the control of the short channel effects [6–8]. According to our knowledge of concern, till now there is no analytical model on hand within the literature for the threshold voltage and surface potential of a nanoscale 4H-SiC MOSFET. The model presents the threshold voltage and surface potential of a nanoscale 4H-SiC MOSFET using the two-dimensional (2D) Poisson equation.
The 2D Poisson equation may be solved by using the four boundary condition in the SiC region, and analyzing the behaviour of the threshold voltage [9, 10], surface potential, and electric field with varying device parameters like gate oxide thickness \( t_{ox} \), 4H-SiC thin layer thickness \( t_{4H-SiC} \), channel length \( L \), and body doping \( N_A \). The intention is to study a physics centered 2D model for a 4H-SiC MOSFET with the aid of solving the 2D Poisson equation [9]. Note that this model can be utilized as a useful tool for the characterization and design of high-efficiency 4H-SiC nanoscale MOSFETs together with the short channel peculiarities by varying various physical parameters. The validity of the model is checked by matching the model results with the 2D simulation results gathered utilizing T-CAD [11, 12].

2. Two-dimensional structure of a 4H-SiC MOSFET

The structure of the 4H-SiC MOSFET is shown in figure 1. When compared to a silicon MOSFET, the 4H-SiC MOSFET structure is especially helpful for device scaling. In this structure a 4H-SiC epilayer is grown on a silicon substrate. The epilayer is doped with the boron concentration of \( 1 \times 10^{17} \text{ cm}^{-3} \) [9]. The phosphorus concentration of \( 2 \times 10^{30} \text{ cm}^{-3} \) [9] is used for source and drain region doping. The silicon dioxide layer is maintained between the gate metal and the 4H-SiC layer and the thickness of the gate oxide layer is \( t_{ox} \). All the device design parameters with specific values are tabulated in table 1. The compact model will be used for the characterization and design of high-efficiency nanoscale 4H-SiC MOSFETs.

2.1. Surface potential and electric field model

Before access of inversion let us write the 2D Poisson equation in the SiC thin film of a 4H-SiC MOSFET, presented in figure 1 as follows [9, 11, 13]

\[
\frac{d^2 \phi(x, y)}{dx^2} + \frac{d^2 \phi(x, y)}{dy^2} = \frac{qN_A}{\varepsilon_{SiC}} \quad \text{for } 0 \leq x \leq L, \quad 0 \leq y \leq t_{SiC}. \tag{1}
\]

The surface potential profile in the SiC film will also be approximated by a parabolic function, as carried out in \cite{9, 11, 13}, i.e.

\[
\phi(x, y) = \phi_{S}(x) + b_1(x)y + b_2(x)y^2 \quad \text{for } 0 \leq x \leq L, \quad 0 \leq y \leq t_{SiC}. \tag{2}
\]

where the coefficients \( b_1(x) \) and \( b_2(x) \) are functions of variable \( x \). Equation (1) may be solved by using the following four boundary conditions [9, 11, 13]:

(a) At the source side the surface potential is

\[
\phi(0, 0) = \phi_S(0) = V_{bs, SiC}, \tag{3}
\]

with

\[
V_{bs, SiC} = \frac{E_{g, SiC}}{2q} + \phi_{F, SiC},
\]

where \( \phi_{F, SiC} \) is the Fermi potential in SiC.

Table 1. List of symbols and their description.

| Symbol     | Confession                                      | Numeric value |
|------------|-------------------------------------------------|---------------|
| \( L \)    | channel length                                   | 100 nm        |
| \( E_{g, SiC} \) | energy band gap of SiC                            | 3.25 eV       |
| \( K \)    | Boltzmann constant                               | \( 1.38 \times 10^{-23} \) |
| \( V_T \)  | the thermal voltage                              | 0.026 V       |
| \( E_{g, Si} \) | band gap in Si                                   | 1.1 eV        |
| \( q \)    | electron charge                                  | 4.35 eV       |
| \( t_{ox} \) | gate oxide dielectric constant                  | 20            |
| \( t_{Si} \) | silicon film thickness                           | 100 nm        |
| \( t_{4H-SiC} \) | SiC thin film thickness                         | 30 nm         |
| \( t_{ox} \) | thickness of gate oxide layer                    | 5 nm          |
| \( \Phi_m \) | surface potential in thin film                   | unknown       |
| \( V_{GS} \) | gate to source voltage                           | 0.1 V         |
| \( V_{sub} \) | the substrate bias                               | 0 V           |
| \( V_{DS} \) | drain to source voltage                          | 0.5 V         |
| \( T \)    | Temperature                                      | 300 K         |

Table 1 includes the list of symbols and their description.
(b) At the drain side the surface potential is
\[
\phi(L, 0) = \phi_S(L) = V_{th, SiC} + V_{DS}.
\] (4)

(c) Electric field at the interface of the gate oxide and SiC film is continuous, i.e.
\[
\left[ \frac{d\phi(x, y)}{dy} \right]_{y=0} = \frac{\varepsilon_{SiC}}{\varepsilon_{SiC}} \left( \frac{\phi_S(x) - V_{GS}}{t_{ox}} \right).
\] (5)

(d) The electric field at the interface of SiC and the silicon substrate is
\[
\left[ \frac{d\phi(x, y)}{dy} \right]_{y=Sat} = \frac{\varepsilon_{Si}}{\varepsilon_{SiC}} \left( \frac{V_{sub} - \phi(x, t_{Si})}{t_{Si}} \right).
\] (6)

By using the boundary conditions (5) and (6), we can obtain the coefficients \(b_1(x)\) and \(b_2(x)\). Then by substituting these coefficients into the expression for \(\phi(x, y)\) and setting \(y = 0\), we obtain
\[
\frac{d^2\phi_0(x)}{dx^2} - \alpha \phi_0(x) = \beta,
\] (7)

where
\[
\alpha = \frac{2(1 + C_{as} + C_{sa})}{t_{SiC}^2(1 + 2C_{as}/C_{sa})},
\] (8)
\[
\beta = \frac{\frac{qN_A}{t_{SiC}} - \frac{2V_{GS}}{t_{SiC}} \left( \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{SiC}} \right) - \frac{2V_{sub}}{t_{SiC}} \left( 1 + 2C_{as}/C_{Sa} \right)}{t_{SiC}^2(1 + 2C_{as}/C_{sa})}.
\] (9)

where \(C_{ox}, C_{Si}\) and \(C_{SiC}\), are the capacitances per unit area for the gate oxide layer, silicon layer and 4H-SiC film, respectively
\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}} \quad \text{and} \quad C_{SiC} = \frac{\varepsilon_{SiC}}{t_{SiC}}.
\]

The solution of equation (7) must satisfy the boundary conditions
\[
\phi_0(0) = \phi_{b, SiC},
\] (10)
and
\[
\phi_0(L) = \phi_{b, SiC} + V_{DS}.
\] (11)

Let us set \(\lambda = \sqrt{\alpha}\) and \(\sigma = \beta/\alpha\). The second order inhomogeneous differential equation (7) with a constant coefficient has the following solution
\[
\phi_0(x) = Ae^{\lambda x} + Be^{-\lambda x} - \sigma,
\] (12)

where
\[
A = \frac{(V_{th, SiC} + \sigma + V_{DS}) - (V_{th, SiC} + \sigma)e^{-\lambda L}}{1 - e^{-2\lambda L}},
\] (13)
\[
B = \frac{(V_{th, SiC} + \sigma + V_{DS})e^{-\lambda L} - (V_{th, SiC} + \sigma)}{1 - e^{-2\lambda L}}.
\] (14)

2.2. Electric field model

By differentiating equation (12) we obtain the electric field
\[
e = \frac{d\phi_0(x)}{dx} = A\lambda e^{\lambda x} - B\lambda e^{-\lambda x}.
\] (15)

2.3. Threshold voltage model

The threshold voltage model can be obtained by calculating the minima of the surface potential (12). From the condition
\[
\frac{d\phi_0(x)}{dx} = 0
\]
we obtain
\[
\phi_{th, min} = 2\sqrt{AB} - \sigma.
\] (16)

The threshold voltage is the minimum value of gate to source voltage \(V_{GS}\) at which a channel is established by the gate oxide at the surface of the 4H-SiC MOSFET. Therefore, in a 4H-SiC MOSFET, the threshold voltage is taken to be that value of \(V_{GS}\) for which the surface potential is equal to twice the difference between the intrinsic and extrinsic Fermi level \(\phi_{F, Si}\) [9, 10, 12–15]:
\[
\phi_{th, min} = 2\phi_{F, SiC} = \phi_{th}.
\] (17)

Here \(\phi_{th}\) is the value of the surface potential at which the inversion electron charge density in the 4H-SiC device is the same as the doping concentration. As a consequence, the threshold voltage is defined as the value of \(V_{GS}\) at which the minimum surface potential \(\phi_{th, min}\) is equal to \(\phi_{th}\). Hence, accordingly, we will assess the value of the threshold voltage by substituting expression (16) into equation (17) and solving for equation (16) by putting the expressions of \(\alpha, \beta, \lambda, \sigma, A\) and \(B\)
\[
V_{th} = \frac{-K_1 + \sqrt{K_1^2 - 4K_1K_3}}{2K_1},
\] (18)
where

\[
K_1 = b^2 [4(N - N^2) - 1],
\]

\[
K_2 = b \{4(N + M + M - 2MN) - 2\phi_{th} \}
+ 2ab [4(N - N^2) - 1],
\]

\[
K_3 = a \{4(N + M + M - 2MN) - 2\phi_{th} \}
- \phi_{th}^2 - 4(M^2 - MV_{th, SiC}) + a^2 \{4(N - N^2) - 1\},
\]

\[
M = \frac{1 - e^{-2b \phi_{th, SiC} + V_{DS}}}{2 \sinh x},
\]

\[
N = \frac{1 - e^{-2b \phi_{th, SiC} + V_{DS}}}{2 \sinh x},
\]

\[
a = \frac{1}{\alpha} \left\{ g_{Na} + \frac{1}{t_{SiC} \epsilon_{SiC}} \left[ C_{ox} \left(1 + \frac{C_{Si}}{2C_{SiC} + C_{Si}}\right) \right. \right. \\
- C_{Si} \left(1 - \frac{C_{Si}}{2C_{SiC} + C_{Si}}\right) V_{sub} \left. \right\},
\]

\[
b = -\frac{1}{\alpha} \frac{C_{ox}}{t_{SiC} \epsilon_{SiC}} \left\{ 1 + \frac{C_{Si}}{2C_{SiC} + C_{Si}} \right\}.
\]

Figure 2. Graph for surface potential versus channel length for \(V_{DS} = 0.5 \text{ V}, V_{DS} = 1.0 \text{ V}, V_{DS} = 1.5 \text{ V} \) and \(V_{DS} = 2.0 \text{ V}\). The device parameters are used as follows: \(V_{sub} = 0 \text{ V}, V_{GS} = 0.1 \text{ V} \), \(N_a = 1 \times 10^{20} \text{ cm}^{-3}, N = 2 \times 10^{20} \text{ cm}^{-3}, t_{SiC} = 30 \text{ nm}, t_{ox} = 5 \text{ nm}, t_{Si} = 100 \text{ nm} \) and \(\phi_M = 4.35 \text{ eV}\).

\(t_{ox} = 3 \text{ nm}, t_{ox} = 6 \text{ nm}, t_{ox} = 9 \text{ nm}\). The device parameters are used as follows: \(V_{GGS} = 0 \text{ V}, V_{DS} = 0.5 \text{ V}, V_{GS} = 0.1 \text{ V} \), \(N_a = 1 \times 10^{20} \text{ cm}^{-3}, N = 2 \times 10^{20} \text{ cm}^{-3}, t_{SiC} = 30 \text{ nm}, t_{ox} = 5 \text{ nm}, t_{Si} = 100 \text{ nm} \) and \(\phi_M = 4.35 \text{ eV}\).

Figure 3. Graph for surface potential versus channel length for \(t_{ox} = 3 \text{ nm}, t_{ox} = 6 \text{ nm}, t_{ox} = 9 \text{ nm}\). The device parameters are used as follows: \(V_{GGS} = 0 \text{ V}, V_{DS} = 0.5 \text{ V}, V_{GS} = 0.1 \text{ V} \), \(N_a = 1 \times 10^{20} \text{ cm}^{-3}, N = 2 \times 10^{20} \text{ cm}^{-3}, t_{SiC} = 30 \text{ nm}, t_{ox} = 5 \text{ nm}, t_{Si} = 100 \text{ nm} \) and \(\phi_M = 4.35 \text{ eV}\).

3. Results and discussion

3.1. Surface potential

To validate the suggested analytical model, the 2D device simulator T-CAD [17] is used for the simulation of the surface potential distribution within the SiC layer and the threshold voltage \(V_{th}\) variation and the results are compared with the analytical model. Figure 2 shows the surface potential variation along the channel length for distinct values of drain voltages. It is understood from figure 2 that there is no powerful change in the potential at the source side and a very infinitesimal change at the drain side. As a final result, \(V_{DS}\) has a very small effect on \(I_D\) after saturation and it is visible from the figure that there is a negligible shift within the factor of the minimum surface potential regardless of the applied drain bias voltage. For this reason, drain-induced barrier lowering is substantially reduced for the 4H-SiC comparable to silicon. The model results and the simulation results [16] are correlated with each other to prove the accuracy of our suggested analytical model.
Figure 3 shows the surface potential variation along the channel for various values of oxide thickness. When the gate oxide thickness increased, the electric field decreased. Therefore, due to the fact that the decrement of electric field impact ionization also reduced, the rate of the generation of carriers was low. So, the controllability of the gate over the channel potential increases and it is less prominent to SCEs. Therefore, oxide thickness cannot be scaled right down to very small values due to the fact that the results of tunneling via the thin oxide and hot-carrier end up prominent.

Figure 4 shows the surface potential variation along the channel for various values of gate voltages. It may be observed from the figure that as the gate voltage increases, there is quite an increment in the height of the barrier at the source side and drain side. Therefore the surface potential increases in the channel region. Consequently, drain induced barrier lowering (DIBL) decreases and the immunity to manage the short channel effects (SCEs) is enhanced.

3.2. Electric field

Figure 5 shows the electric field distribution variation along the channel for distinct values of gate oxide thickness. It may be observed from the figure that at the drain side, with an increase in the gate oxide value, the electric field substantially reduces. Hence, the reduction of the electric field experienced by the carriers in the channel may be understood because of the reduction of the hot-carrier effect.

3.3. Threshold voltage

Figure 6 shows the variation of the threshold voltage along the channel for distinct doping concentration. As proven within the figure, the threshold voltage increases with improved body doping concentration. Hence, the scaling of the device can go to a further extent without any further increase in SCEs by increasing the body doping concentration. The threshold voltage obtained from the model correlates very well with the simulation result.

Figure 7 shows the threshold voltage variation alongside the channel for distinct values of gate oxide thickness. When the gate oxide thickness is diminished, the threshold voltage can also be diminished which is the requirement for a faster device. However, oxide thickness cannot be scaled all the way down to very small values because tunneling via the thin oxide layer and hot-carrier effects becomes prominent. It is clear that there is a
close match between the analytical outcome and the 2D simulation outcome.

4. Conclusion

Analytical modelling of the electric field, surface potential and threshold voltage for a 4H-SiC MOSFET is developed based on the 2D physical model. The influence of quite a lot of device parameters like gate length scaling, body doping, SiC thickness, gate oxide thickness on the electric field, the surface potential, and the threshold voltage are analyzed. The results envisioned by the model are compared with the 2D simulations performed by using a commercially available device simulator Sentaurus™. There is a large drop in the threshold voltage with the decrease in channel length. The use of 4H-SiC material instead of silicon increases the device performance regarding reduced short channel effects. The compact model adequately predicts the threshold voltage over a gigantic variety of device parameters and can also be conveniently used to characterize and design the nanoscale 4H-SiC MOSFETs with the desired performance.

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Figure 7. Graph for threshold voltage versus channel length for $t_{ox} = 3$ nm, $t_{ox} = 6$ nm, $t_{ox} = 9$ nm. The device parameters are used as follows: $V_{sub} = 0$ V, $V_{DS} = 0.5$ V, $V_{GS} = 0.1$ V, $t_{SiC} = 30$ nm, $t_{Si} = 100$ nm and $\phi_M = 4.35$ eV.

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