Low Power Sub-threshold Domino AND Gate

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Abstract. A high performance digital system is the need of an hour, in the current scenario not only the area but the leakage power holds the key for the future devices. The development of handheld devices often gets restricted due to the limited power resources available in these devices. The conventional structure performs badly for these devices hence multiple design schemes like domino have surface for recent devices. The Domino logic circuits provide high speed operations in comparison to conventional structure. The problem of charge sharing, charge leakage in domino circuits results in improper output level which can be eliminated using Keeper and Pre-charge internal node technique. For achieving very low power all PMOS and NMOS transistors are conducted in sub threshold region. This paper has implemented ultra-low power Domino AND gate. Simulations has been done using Tanner 13 using 18u CMOS technology. A comparison has been carried out with different approaches available in literature and keeper circuit-based domino logic reveals least power consumption which makes it is suitable for ultra-low power devices.

Keywords: Domino logic, power, charge leakage, charge sharing.

1. Introduction
Static CMOS circuits are used to build digital circuits. But it suffers from requirement of larger area and short circuit power dissipation. In this category, another logic style pseudo nmos consumes more static power as contrast to conventional static CMOS and suffers from poor noise immunity. These limitations can be eliminated by using dynamic logic. The dynamic logic requires N+2 transistors as compared to 2N in static logic, where N is the number of transistors [1]. It is beneficial to operate transistor in sub-threshold regime to save power. So, the sub-threshold circuits are considered which operates under the threshold voltage. These circuits are ether said to in off state or in nearly on state like situation. Domino logic style is preferred over to dynamic circuit to avoid cascading problem. Sub-threshold domino circuits as like Domino circuits work in two phases, one is pre-charge phase and other one is evaluation phase. During the pre-charge phase output node is charged to supply voltage (VDD) and while during evaluate phase inputs applied at gate takes into effect at the output. But it is affected by charge sharing and leakage [2]. The problem of charge sharing, and charge leakage is eliminated using Keeper and pre-charge internal node and combining both techniques.
together. These problems need to get eliminated for proper functionality of the logic implemented with the domino topology. However, these circuits are very prone to noise and dependent on circuit topologies. These problems are discussed below. However, while attain low power, delay comparatively increases for these circuits [3].

The dynamic value stored on the capacitor decides the operation of a dynamic gate. Ideally, the output should remain at the pre-charged phase of VDD if the pull-down network is off. However, due to presence of leakage currents, causes reduction in charge gradually [4]. The prime aspects of leakage are conduction in sub-threshold region and reverse biased junction present in both of PMOS and NMOS networks. Leakage currents mitigates the charge stored on load capacitance (CL). The output level is below than the power supply due to charge leakage. The leakage current is produced during evaluate mode due to high impedance state of the output node [5]. The bleeder transistor is integrated with output node to lower the output impedance to reduce the leakage current [6] which is mainly due to prevention of undesirable discharging. The aspect ratio of bleeder transistor is kept low to compensate for the charge lost.

Charge sharing is other imperative factor in dynamic logic. Fig 1[7] is showing charge sharing problem in Dynamic NAND gate circuit. The output node is pre-charged to VDD for the pre-charge phase. Initially, all set of inputs are 0 and Ca is discharged. Further, A changes from 0 to 1 which makes Ma on and B is set to 0 during evaluation. The charge stored on CL is divide between CL and Ca. This causes a drop in the output voltage, which cannot be recovered due to the dynamic nature of the circuit [8-10]. The most common and effective approach to deal with the charge redistribution is to pre-charge critical internal nodes [11-12]. This solution obviously comes at the cost of increased area and capacitance.

![Fig 1: Dynamic Circuit showing charge sharing problem](image)

**2. Results and discussion**

The Circuits are implemented on Tanner13. Figure 2, 3, 4 and 5 showing the subthreshold Domino AND gate, Domino AND gate With Keeper, Pre-charge Internal nodes, Combined pre-charge internal node and keeper technique, respectively. PMOS transistor used for keeper and pre-charge internal node is having long length and narrow width. High skew inverter at the output of Dynamic gate is used for favoring the rising output transitions.
Fig 2: Domino AND Gate

Fig 3: Domino AND Gate with pre-charging internal nodes Technique
Fig 4: Domino AND Gate with Keeper Technique

Simulations were performed with Tanner 13, 180 nm CMOS technology using 0.3V supply clock frequency is kept in KHz. Subthreshold circuits result in very low power dissipation as compared to strong inversion-based Domino Circuits. Table 1 represents the comparison based on power among various techniques which are discussed for removing the problem of charge sharing and charge leakage. Fig 6 showing the waveform for simulated Domino AND Gate. The traditional keeper, internal node pre-charging, and their combination are found to be effective in mitigating the effects of charge-sharing and leakage. The results reveal that Keeper technique is having least power consumption for low frequency operations. Keeper circuit based logic consumes 361 nW power dissipation as compared to Foot Driven Stack Transistor Domino Logic which consumes 0.5152 µW [13]. The keeper circuit shows higher degree of improvement in power as compared to comparator-based Domino logic (1 nW)[14] and Lector based foot driven stacked transistor domino logic (2.155 mW) respectively [15].
3. Conclusion

In this paper, key issues related to dynamic logic circuits are addressed. Domino AND gate with keeper, pre-charge internal node and combination of two methods has been implemented for low power using Tanner EDA tool. A comparison has been carried out and result reveals that Domino AND gate with keeper circuit offers low power. This is beneficial for designing of future dynamics circuits for ultra-low power consumption.

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