A highly linear 10 Gb/s MOS current mode logic driver with large output voltage swing based on an active inductor

Tengjia Wang¹, Min Zhou¹, a), Jiarui Liu¹, ², Zhiyu Wang¹, ², Jiongjiong Mo¹, ², Hua Chen¹, ², and Faxin Yu¹, ²

Abstract This letter proposes a MOS-current-mode-logic (MCML) driver with an active inductor structure to provide large voltage swing with linear response. This design is implemented in 45 nm CMOS with 1.2V supply. Compared with conventional active-inductor-based circuits, this topology enlarges the available single-ended output voltage swing from less than 350 mV to 600 mV. The MCML driver occupies a chip area of 0.0264 mm². Operating at 10 Gb/s over a channel with 3.5 dB loss at 5 GHz, the eye height is measured as 351 mV with 600 mV single-ended voltage swing, and the peak-to-peak jitter is 14.9 ps (0.149 UI). Keywords: active inductor, large voltage swing, linear, MCML driver

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the operating speed of I/O circuitry approaching microwave frequency range [1], the parasitic capacitances of wires, ESD devices, and bond pads become the major bandwidth-limiting factors. The reduction of bandwidth worsens the eye diagram at the receiver, and results in BER [2, 3]. Hence the bandwidth of the I/O output drivers needs to be extended. Inductive termination is useful in providing bandwidth enhancement [4], and CMOS on-chip spiral passive inductors are widely used as the inductive load of driver [5, 6]. However the spiral inductor is not only difficult to keep its self-resonance frequency higher than operating frequency in larger inductance, but also occupies huge area [7, 8, 9, 10, 11].

Many researchers have examined that active inductor is a more area-efficient alternative to realize an on-chip inductor [12, 13, 14, 15]. The active inductors are often used in MCML circuits due to the low-Q requirement, and both its area and resonant frequency scale with technology [16, 17]. Despite these advantages, active inductors impose some design challenges [18, 19]. Active inductors are built using transistors, so the voltage swing is lower than that of passive inductor due to the large voltage headroom required by the transistors. And the nonlinear characteristics of the transistors make the inductive impedance of active inductor vary with the bias point [20]. When the active inductor operates in relatively large voltage swing, the variation of output impedance is large. To increase the output voltage swing, some other works are done [21, 22, 23]. They overcome the limitations of threshold voltage, so the required voltage headroom is reduced, but the effect of the nonlinearity of transistors still exists. In order to make the impedance variation acceptable, they only provide limited increase on the output voltage swing.

In this letter, we propose an MCML driver with an active inductor structure to operate under large voltage swing with linear response. A PMOS based active inductor with a gate voltage level shifter and a drain series resistor is introduced to allow large output voltage swing and high linearity of the output impedance. The presented design can be widely used to achieve large eye height and low BER at the receiver.

2. Active inductor structures

The active inductor based driver transmits data across a channel to the receiver [24], the diagram of which is shown in Fig. 1. In this diagram, C_l represents the total parasitic capacitance seen at the output node of the driver, Z_T is the output impedance of the driver (with active inductor termination) and Z_0 is the characteristic impedance of the channel which is generally 50 Ω.

The fundamental active inductor circuit is shown in Fig. 2(a) [25]. It consists of an NMOS load transistor, M1 with a resistor, R connected between the gate of M1 and VDD. The C_GS of M1 and the resistor R provides high impedance at high frequency. However, due to the limitation of the output voltage, V_{out} < VDD-V_{th}, it cannot be used in low supply voltage applications [26].

[27, 28] used a folded active inductor as shown in Fig. 2(b). The folded NMOS transistor allows higher Vout. [21] proposed a PMOS based active inductor. However, these structures are strongly bias dependent. In order to exhibit 50 Ω output resistance and large output voltage swing, the bias currents and the override voltages of transistors should be large. And the equivalent output impedances

---

¹ School of Aeronautics and Astronautics, Zhejiang University, Hangzhou, 310000, China
² ZJU-Hangzhou Global Scientific and Technological Innovation Center, Hangzhou, 310000, China
a) zhoumin@zju.edu.cn

DOI: 10.1587/elex.17.20200160
Received April 23, 2020
Accepted May 18, 2020
Publicized May 28, 2020
Copyedited June 10, 2020

Copyright © 2020 The Institute of Electronics, Information and Communication Engineers
change as $V_{\text{out}}$ varies with time. Both of them limit the output voltage swings in these structures.

As shown in Fig. 2(c), this work proposes a highly linear active inductor structure, with which the designed MCML driver can operate under large voltage swing and provide less variation of impedance. The proposed structure uses a PMOS transistor M1 and a resistor $R_1$ connected between the gate of M3 and the drain of M1 (node B). NMOS transistors M3 and M2 form a level shifter which allows lower bias voltage for the gate of M1. A drain series resistor $R_S$ is introduced to reduce the override voltage of transistors under large output voltage swing and $50 \Omega$ output resistance, and also reduce the variation of $V_B$ (the voltage of node B) when $V_{\text{out}}$ changes.

3. Circuit analysis and design

Fig. 3 shows the full schematic of the presented MCML driver. The driver is designed as a fully differential structure, in which two proposed active inductors are used as the differential load. $R_{\text{end}}$ is for electrostatic discharge protection. $V_{\text{op}}$ and $V_{\text{on}}$ are the differential output nodes of the driver, and $I_{SS}$ is the tail current.

3.1 Small-signal analysis

In order to achieve the concrete design, the small-signal impedance of the active inductor is analyzed at the common mode bias point of the MCML driver. Due to the symmetry of the driver, the analysis is done on the left active inductor in Fig. 3, of which $V_{\text{op}}$ is the output voltage and the bias current is $I_{SS}/2$.

Assuming the level shifter has a unity AC gain, and simplifying the model of M1 with $g_m$ and $C_{gs}$, the small-signal equivalent circuit of the active inductor is shown in Fig. 4(a). The equivalent impedance $Z_T$ can be computed as Eq. (1):

$$Z_T = \frac{1 + g_m R_S + j \omega C_{gs} (R_1 + R_S)}{g_m + j \omega (1 + g_m R_S) C_L + C_{gs}} - \omega^2 C_L C_{gs} (R_1 + R_S)$$  \hspace{1cm} (1)

$C_L$ is the total parasitic capacitance of output node, which satisfies $C_L \gg C_{gs}$. Ignoring $C_{gs}$ in the second term in the denominator of $Z_T$, we achieve a passive equivalent circuit as shown in Fig. 4(b). The values of $R_0$, $L$, $C_P$ are given by Eq. (2), Eq. (3) and Eq. (4).

$$L = \frac{C_{gs} (R_1 + R_S)}{g_m}$$ \hspace{1cm} (2)

$$C_P = C_L$$ \hspace{1cm} (3)

$$R_0 = \frac{1 + g_m R_S}{g_m}$$ \hspace{1cm} (4)

in which the values of $C_{gs}$ and $g_m$ scale with technology. This work is designed in 45 nm CMOS technology with 1.2 V power supply. As a rule of thumb, the value of $C_L$ is about 400 fF in this technology. And $R_0$ should be 50Ω to realize the impedance matching. According to [29, 30], $L = R^2 C/m$, and the circuit has maximum bandwidth when $m = \sqrt{2}$. However, considering the channel loss, the value of $m$ should be tuned to provide a flat total gain within the range of concerned frequency [31]. This work is designed to operate with 10 Gb/s bit rate, so the concerned frequency band is below 5 GHz, and the channel loss shown in Fig. 5 is the measurement result of the real channel provided by our users. We sweep m from 0.5 to 2 to have expected gain at the end of the channel. The simulation results are shown in Fig. 5. From the results, the gain is flat below 5 GHz when $m = 1$, therefore, $m$ is set to be 1, and $L$ is designed to be 1 nH.

3.2 Large-signal operation

As shown in Fig. 3, when the MCML driver operates with a large voltage swing, the tail current is steered through the pair of the proposed active inductors, to transmit the digital
data.

When the driver is connected with an impedance matched load, the single-ended output \( V_{pp} \) (peak-to-peak voltage at \( V_{op} \) or \( V_{on} \)) is determined by \( R_0 I_{SS}/2 \) (half of the open load \( V_{pp} \)), where \( R_0 = 50 \Omega \) and \( I_{SS} \) is the tail current. The output DC level is \( (VDD - R_0 I_{SS})/2 \), so the output voltage ranges from \( (VDD - 3R_0 I_{SS})/4 \) to \( (VDD - R_0 I_{SS})/4 \).

With 1.2 V supply, the possible maximum \( V_{pp} \) with impedance matched load (\( V_{max} \)) is about 600 mV. In order to reach \( V_{max} \), the bias current \( I_{SS} \) should be 24 mA. Operating with the large bias current, the gate voltage of M1 needs to be very low. In 45 nm CMOS technology and with 1.2 V supply, the saturation voltage \( V_{dsat} \) of M1 cannot be higher than 377 mV. Assisted by the empirical equation in 45 nm CMOS, we have \( I_{SS} = 2 g_m V_{dsat} \) to estimate the maximum \( I_{SS} \) of M1 with given \( g_m \).

According to Eq. (4), big \( R_S \) allows bigger \( g_m \) when the output impedance exhibits 50 \( \Omega \). Combined with Eq. (4), \( V_{max} \) can be estimated as Eq. (5). The values of \( V_{max} \) versus \( R_S \) are plotted in Fig. 6. \( V_{max} \) cannot be lower than 600 mV when \( R_S \) is smaller than 18.6 \( \Omega \). Therefore, we can draw that with 1.2 V supply, conventional active inductors without \( R_S \) (\( R_S = 0 \)) cannot operate at \( V_{pp} = 600 \Omega \).

\[
V_{max} = \frac{R_0}{(R_0 - R_S)} V_{dsat} \tag{5}
\]

The impedance of an active inductor is highly related to the bias point of the transistors. The drain series resistor \( R_S \) can reduce the voltage variation of node B by a factor of \( (R_0 - R_S)/R_0 \) during large voltage swing. Although \( R_S \) can enlarge the output voltage swing to 600mV (when \( R_S = 18.6 \Omega \)), which is almost the maximum swing with 1.2 V supply, and allow the active inductor to have linear response under large voltage swing, additional costs introduced by large \( R_S \) need to be mentioned. According to Eq. (2) and Eq. (4), in order to exhibit 50 \( \Omega \) \( R_0 \), the value of \( 1/g_m \) turns to be very small when \( R_S \) goes far beyond 18.6 \( \Omega \). With small \( 1/g_m \), large \( C_{gs} \) and \( R_1 \) are needed to achieve the expected inductance \( L \), which costs large area and introduces large noise. Therefore, \( R_S \) is finally set to be 18.6 \( \Omega \) to achieve 1nH inductance and 50 \( \Omega \) resistance.

Fig. 7 shows the impedance of the active inductor and the passive equivalent circuit which is shown in Fig. 2(b), and the equivalent \( L = 1 \) nH, \( C_p = 400 \) fF, \( R_0 = 50 \Omega \).  

### 3.3 Simulation results

As discussed earlier, the proposed active inductor with MCML driver is designed to have 600 mV single-ended \( V_{pp} \) and a nominal output DC level of 600 mV in 45 nm CMOS with 1.2 V supply. In this case, the bias current \( I_{SS} \) is 24 mA. Fig. 8(a) shows the simulation results of the variation of the equivalent \( L \) of proposed active inductor versus frequency with 300 mV to 900 mV output voltage (at \( V_{op} \) or \( V_{on} \)). To have a comparison with the conventional active inductor, Fig. 8(b) shows the simulation results of the equivalent \( L \) of conventional active inductor in [21]. The voltage swing of the conventional active inductor is 300 mV, so the DC level is 900 mV and the output voltage ranges from 750 mV to 1.05 V. The inductances of \( L \) at each common mode DC level are both 1 nH. Below 5 GHz, the inductance of \( L \) (proposed) varies from 700 pH to 1500 pH under 600mV voltage swing while the inductance of \( L \) (conventional) varies from 350 pH to 1700 pH under 300 mV voltage swing. These results demonstrate that, even with a much larger voltage swing, the proposed active inductor shows higher linearity than the conventional structure.

Fig. 9 shows the simulated single-ended eye diagram transmitted by the proposed MCML driver through the channel (shown in Fig. 4) at the receiver. The data is a 10Gb/s
2^32-1 pseudo-random binary sequence. Under 600mV single-ended voltage swing, the eye height is 400mV and the peak-to-peak jitter is 11 ps.

4. Experimental results

Fig. 10 shows the chip micrograph and layout of the proposed MCML driver used in a SERDES transmitter lane fabricated in 45 nm CMOS technology with an area of 0.0264 mm^2. The circuit draws a total DC current of 24 mA from a 1.2 V supply.

A 2-m long MICABLE T26-01-01-2M cable is used as the channel to demonstrate the voltage swing that the proposed MCML driver can provide. The loss of the 2-m cable with SMA connectors is about 3.5 dB at 5 GHz.

Fig. 11 shows the S11 of the proposed MCML driver measured by Agilent N5230C network analyzer. S11 is less than 10 dB from DC to 5 GHz.

Fig. 12 shows the eye diagrams when 10 Gb/s 2^32-1 PRBS data patterns are transmitted by the driver with active inductors off (use 50 Ω resistor instead) in Fig. 12(a) and with active inductors on in Fig. 12(b) through the same cable channel to a KEYSIGHT DSAZ254A digital signal analyzer. The single-ended voltage swings are both 600mV, and the eye heights in Fig. 12(a) and Fig. 12(b) are 157mV and 351mV with the peak-to-peak jitters of 41.4 ps (0.414UI) and 14.9 ps (0.149UI). The proposed driver with active inductor increases the eye height by a factor of 2.2 and reduces peak-to-peak jitter by about 65%.

There is a performance degradation between the simulation results shown in Fig. 9 and the measurement results shown in Fig. 12(b). The eye height reduces because the channel in measurement introduces higher channel loss in low frequency, though it has similar channel loss with the channel in simulation at 5 GHz. And the proposed driver is used in a SERDES transmitter lane. Many blocks such as multiplexer, sampler and PLL are integrated on the same chip, therefore the measured peak-to-peak jitter performance is worsened by the power noises introduced by these blocks.

The circuit performance is summarized in Table I. with the comparison of previously published works with active inductors. Compared with others, the proposed design achieves a larger voltage swing when the data rate is relatively high.
This page presents a MCML driver with a proposed active inductor structure to provide large voltage swing with highly linear response. The driver with active inductor is designed in 45 nm CMOS with 1.2 V power supply. By using an 18.6 Ω passive resistor in series between the transistors and the output node, the driver can provide 600 mV peak-to-peak single-ended output voltage in 1.2 V supply, and the active inductor operates with high linearity. The measurement result demonstrates that the MCML driver can work well under large voltage swing. The measured eye height is 351 mV with a single-ended output swing of 600mVp-p and the measured peak-to-peak jitter is 14.9 ps. The output swing is much larger in this work than in conventional structures. Therefore, the presented design can be widely used to achieve large eye height and low BER at the receiver.

5. Conclusion

This letter presents an MCML driver with a proposed active inductor structure to provide large voltage swing with highly linear response. The driver with active inductor is designed in 45 nm CMOS with 1.2 V power supply. By using an 18.6 Ω passive resistor in series between the transistors and the output node, the driver can provide 600 mV peak-to-peak single-ended output voltage in 1.2 V supply, and the active inductor operates with high linearity. The measurement result demonstrates that the MCML driver can work well under large voltage swing. The measured eye height is 351 mV with a single-ended output swing of 600mVp-p and the measured peak-to-peak jitter is 14.9 ps. The output swing is much larger in this work than in conventional structures. Therefore, the presented design can be widely used to achieve large eye height and low BER at the receiver.

References

[1] C.-C. Lee, et al.: “A low-power miniature 20 Gb/s passive/active hybrid equalizer in 90 nm CMOS,” IEEE Microw. Wireless Compon. Lett. 25 (2015) 699 (DOI: 10.1109/LMWC.2015.2453322).
[2] W. Kim and W. Choi: “A 10-Gb/s low-power adaptive continuous-time linear equalizer using asynchronous under-sampling histogram,” IEICE Electron. Express 10 (2013) 20130330 (DOI: 10.1587/elex.20130330).
[3] G. de Street, et al.: “SleepTalker: a ULV 802.15.4a IR-UWB transmitter SoC in 28-nm FDSOI achieving 14 pJ/bit at 27 MHz with channel selection based on adaptive FBB and digitally programmable pulse shaping,” IEEE J. Solid-State Circuits 52 (2017) 1163 (DOI: 10.1109/JSSC.2016.2545607).
[4] S. Mohan, et al.: “Bandwidth extension in CMOS with optimized on-chip integrators,” IEEE J. Solid-State Circuits 35 (2000) 346 (DOI: 10.1109/6.826816).
[5] J. Kim, et al.: “Circuit techniques for a 40Gb/s transmitter in 0.13μm CMOS,” IEEE International Solid-State Circuits Conference Dig. Tech. Papers (2005) 150 (DOI: 10.1109/ISSCC.2005.1493913).
[6] G. Zhang, et al.: “An amplifier-doubler chain with conversion gain improvement techniques,” IEICE Electron. Express 15 (2018) 20171118 (DOI: 10.1587/elex.15.20171118).
[7] A. Thanhachayanan: “CMOS transistor-only active inductor for IF/RF applications,” IEEE International Conference on Industrial Technology (2002) 1209 (DOI: 10.1109/ICIT.2002.1189346).
[8] S. Xie, et al.: “An inductorless CMOS limiting amplifier with stream-mode active feedback,” IEICE Electron. Express 15 (2018) 20180860 (DOI: 10.1587/elex.15.20180860).
[9] O. Farouk, et al.: “Comparative analysis and simulation of active inductors for RF applications in 90 nm CMOS,” International Conference on Electrical Information and Communication Technology (2017) 978 (DOI: 10.1109/EICT.2017.8275233).
[10] L. Pantoli, et al.: “Design considerations and effects of class-AB polarization in active filters realized by means of active inductors,” European Microwave Conference (EuMC) Dig. Tech. Papers (2017) 37 (DOI: 10.23919/EuMC.2017.8230793).
[11] K. Ture, et al.: “Area and power efficient ultra-wideband transmitter based on active inductor,” IEEE Trans. Circuits Syst. II, Exp. Briefs 65 (2018) 1325 (DOI: 10.1109/TCSII.2018.2853190).
[12] S.H. Elahi and A. Nabavi: “A UWB LNA with interference rejection using enhanced-Q active inductor,” IEICE Electron. Express 6 (2009) 335 (DOI: 10.1587/elex.6.335).
[13] B. Shammugusamy, et al.: “A 24mW, 5Gb/s fully balanced differential output trans-impedance amplifier with active inductor and capacitive degeneration techniques in 0.18μm CMOS technology,” IEICE Electron. Express 7 (2010) 308 (DOI: 10.1587/elex.7.308).
[14] K.-H. Cheng, et al.: “A 0.9–8 GHz VCO with a differential active inductor for multistandard wireline SerDes,” IEEE Trans. Circuits Syst. II, Exp. Briefs 61 (2014) 559 (DOI: 10.1109/TCSII.2014.2327451).
[15] H.T. Bui and Y. Savaria: “Shunt-peaking of MCML gates using active inductors,” The 2nd Annual IEEE Northeast Workshop on Circuits and Systems (NEWCAS) Dig. Tech. Papers (2004) 361 (DOI: 10.1109/NEWCAS.2004.1359107).
[16] K. Gupta, et al.: “A novel active shunt-peaked MCML-based high speed four-bit Ripple-Carry adder,” ICCCT Dig. Tech. Papers (2010) 285 (DOI: 10.1109/ICCCT.2010.5640516).
[17] M.-S. Kao, et al.: “A 10-Gb/s CML I/O circuit for backplane interconnection in 0.18μm CMOS technology,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 17 (2009) 688 (DOI: 10.1109/TVLSI.2009.2016726).
[18] C.-L. Lee, et al.: “CMOS active inductor linearity improvement using feed-forward current source technique,” IEEE Microw. Theory Techn. 5.7 (2009) 1915 (DOI: 10.1109/MTT.2009.2025426).
[19] H.G. Momen, et al.: “CMOS high-performance UWB active inductor circuit,” Conference on Ph.D. Research in Microelectronics and Electronics (2016) 493 (DOI: 10.1109/PRIME.2016.7519552).
[20] R. Bhattacharya, et al.: “A highly linear CMOS active inductor and its application in filters and power dividers,” IEEE Microw. Wireless Compon. Lett. 25 (2015) 715 (DOI: 10.1109/LMWC.2015.2479718).
[21] Y.-S. M. Lee, et al.: “A 10Gb/s active-inductor structure with peaking control in 90nm CMOS,” IEEE Asian Solid-State Circuits Conference Dig. Tech. Papers (2008) 229 (DOI: 10.1109/ASSCC.2008.4708770).
[22] A. Saberkari, et al.: “Design and comparison of flapped active inductors with high quality factors,” Electron. Lett. 50 (2014) 925 (DOI: 10.1049/el.2014.0388).
[23] A. Worapishet and M. Thamsiriamunt: “An NMOs inductive loading technique for extended operating frequency CMOS ring oscillators,” Midwest Symposium on Circuits and Systems (2002) 116 (DOI: 10.1109/MWSCAS.2002.1187170).
[24] P. Payandehnia, et al.: “A 12.5Gb/s active-inductor based transmitter for I/O applications,” European Conference on Circuit Theory and Design (ECCTD) Dig. Tech. Papers (2011) 186 (DOI: 10.1109/ECCTD.2011.6043313).
[25] E. Sackinger and W.C. Fischer: “A 3-GHz 32-db CMOS limiting amplifier for SONET OC-48 receivers” IEEE J. Solid-State Circuits 35 (2000) 1884 (DOI: 10.1109/94.890301).
[26] H. Kimura, et al.: “2.1 2Gb/s 560mW multi-standard SerDes with single-stage analog front-end and 14-bit decision-feedback equalizer in 28nm CMOS,” IEEE International Solid-State Circuits Conference Dig. Tech. Papers (2014) 38 (DOI: 10.1109/ISSCC.2014.6757327).
[27] C.-H. Wu, et al.: “A 1V 4.2mW fully integrated 2.5Gb/s CMOS limiting amplifier using folded active inductors,” IEEE International Symposium on Circuits and Systems (2004) 1044 (DOI: 10.1109/ISCAS.2004.1328377).
[28] J. Chen, et al.: “Electrical backplane equalization using programmable analog zeros and folded active inductors,” IEEE Trans. Microw. Theory Techn. 55 (2007) 1459 (DOI: 10.1109/MTT.2007.900342).
[29] T.H. Lee: “The Design of CMOS Radio-Frequency Integrated Circuits” (Cambridge University Press, Cambridge, 2004) 2nd ed. 273.
the shunt-peaking inductor(s) in CMOS trans-impedance amplifier system by placement of poles and zeros,” IEEE International Conference on Electronics, Circuits, and Systems Dig. Tech. Papers (2011) 17 (DOI: 10.1109/ICECS.2011.6122203).

[31] J. Han, et al.: “A 60Gb/s 288mW NRZ transceiver with adaptive equalization and baud-rate clock and data recovery in 65nm CMOS technology,” IEEE International Solid-State Circuits Conference Dig. Tech. Papers (2017) 112 (DOI: 10.1109/ISSCC.2017.7870286).