ZrS$_2$ symmetrical-ambipolar FETs with near-midgap TiN film for both top-gate electrode and Schottky-barrier contact

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ZrS$_2$ ambipolar MISFETs are obtained in operations with both electrons and holes. A layered polycrystalline ZrS$_2$ thin film was formed by sputtering and sulfur-vapor annealing on a whole surface of a 2.4 cm $\times$ 2.4 cm SiO$_2$/Si substrate. The ZrS$_2$ FETs have Al$_2$O$_3$ gate insulator and TiN film for both the top-gate electrode and Schottky-barrier contact, which show symmetrical $I$–$V$ curves with a $V_{ds}$ of 0.4 V contributed by the TiN film with midgap work function to the sputtered ZrS$_2$ film. Notably, ambipolar FET operations because of both electrons and holes were successfully observed with an on/off current ratio of 250. This is an important step to realize n/p-type unipolar ZrS$_2$ FETs.

1. Introduction

The scaling of silicon FETs has currently reached down to 5 nm technology node. Although new FET structures such as nanosheet, forksheet and n/p-stacked complementary FETs have been proposed for the sub-3 nm technology node, it is very difficult for these structures to maintain device performances due to the mobility degradation caused by scattering mechanisms in a channel with a thickness of only a few nano-meters. Therefore, adoption of new materials with high mobilities even at the atomically thin thickness has been considered. Two-dimensional (2D) semiconductors have attracted intense attention because of their excellent electrical properties. In particular, 2D transition metal dichalcogenide films have unique electrical and physical properties, such as a high mobility and a steady band gap despite an atomically-thin thickness. A Zirconium disulfide (ZrS$_2$) film has reported to perform high mobilities of more than 1000 cm$^2$ V$^{-1}$ s$^{-1}$ and sulfur vapor annealing. Although a chemical vapor deposition (CVD) method for the synthesis of ZrS$_2$ film has been reported, a large area formation of this film has not been demonstrated yet. On the other hand, there has been a different attempt to use the sputtering method that achieves a uniform thickness with less contamination, and also fabrication of FETs has been demonstrated with this method. It has been reported that a large-area film of layered-polycrystalline ZrS$_2$ with a high Hall-effect electron mobility of 1250 cm$^2$ V$^{-1}$ s$^{-1}$ was achieved by sputtering and sulfur-vapor annealing. To realize CMOS logic circuits based on ZrS$_2$ films, both p- and n-type transistors are required. Although electron conduction has been observed in ZrS$_2$ films, hole conduction of a ZrS$_2$ film has not been demonstrated yet. For both electron and hole conductions, an intrinsic ZrS$_2$ channel film, low resistance contacts to the channel and appropriate gate metals for the channel are necessary. ZrS$_2$ MISFETs with both electron and hole conductions were preliminary demonstrated by using only a near-midgap TiN film for both the top-gate electrode and the Schottky-barrier contact.

2. Experimental methods

TiN source and drain (S/D) electrodes with a thickness of 80 nm formed on an SiO$_2$/Si substrate by sputtering and subsequent wet etching. A ZrS$_2$ film was formed using an ultra-high-vacuum radio frequency magnetron sputtering tool and a ZrS$_2$ target of 99%. Then, sulfur-vapor annealing was carried out for sulfur compensation in which sulfur powder was evaporated at 250 °C for 60 min, and wafers were heated at 700 °C for 60 min in Ar flow under 100 Pa. A 20 nm Al$_2$O$_3$ gate insulator was deposited by atomic layer deposition (ALD) at 300 °C using trimethyl aluminum and H$_2$O precursors. Then, an active area was defined by photolithography and reactive ion etching (RIE). After those, a 60 nm SiN sidewall beside the active area was formed by sputtering and lift-off method, as shown in Figs. 1 and 2. A top-gate of the TiN film was also formed by sputtering and wet etching. Then, S/D contact through the Al$_2$O$_3$ gate insulator were fabricated by RIE and sputtering. Finally, forming gas (F.G.) annealing was conducted at 300 °C for 10 min.

3. Results and discussion

Figure 3 shows the $I_d$–$V_{ds}$ characteristics of the ZrS$_2$ MISFETs obtained with and without F.G. annealing for the $V_{ds}$ of 0.05 and 1.0 V. It is observed that different threshold
Voltages are obtained with and without F.G. annealing at a high $V_{ds}$. Especially with F.G. annealing, ambipolar transfer characteristics at $V_{ds}$ of 1.0 V are confirmed.

To confirm the insulation property of the Al$_2$O$_3$ film, the $I_d$, $I_s$, and $I_g-V_{gs}$ characteristics of the ZrS$_2$ MISFETs obtained with and without F.G. annealing are shown in Figs. 4(a) and 4(b). Since the $I_d$ directly corresponds to the $I_s$ value at high $V_{gs}$ and the $I_g$ is sufficiently suppressed, the ALD Al$_2$O$_3$ film shows good insulation behavior even on the ZrS$_2$ film. The $I_g$ appears to be independent of the gate voltage because of a floating channel voltage with a semiconductor-on-insulator structure of the ZrS$_2$ MISFET.\(^{41,22}\)

To elucidate the origin of the $V_{th}$ shift, the $I_d-V_{gs}$ characteristics in forward and backward sweeps for the ZrS$_2$ MISFETs obtained with and without F.G. annealing are shown in Figs. 5(a) and 5(b). Regardless of the F.G. annealing, only a small $V_{th}$ shift is observed for a relatively high gate voltage range. It is speculated that the density of interface states between the Al$_2$O$_3$ and the ZrS$_2$ films are very low despite the polycrystallinity of the sputtered ZrS$_2$ film. Therefore, it is considered that fixed charges in the Al$_2$O$_3$ film play the dominant role in the $V_{th}$ shift. This indicates that positive fixed charges are reduced by the F.G. annealing resulting in the positive $V_{th}$ shift. In addition, the reduction of the off-current after F.G. annealing is considered to be because of the termination of an edge of the ZrS$_2$ channel by hydrogen.

To evaluate the drive current on F.G. annealing, the $I_d$ and $I_g-(V_{gs} - V_{off})$ characteristics of the ZrS$_2$ MISFETs obtained with and without F.G. annealing are shown in Fig. 6, where $V_{off}$ is extracted at the minimum $I_d$. The $I_d$ values at high positive $V_{gs} - V_{off}$ with and without the F.G. annealing are almost identical.

To confirm the saturation characteristics at negative and positive gate voltage ranges, the $I_d-V_{ds}$ characteristics of the ZrS$_2$ MISFETs obtained with F.G. annealing are shown in Figs. 7(a) and 7(b), respectively. The Schottky-like $I_d$ curves are observed at the negative gate voltage, while at the positive one, $I_d$ shows Ohmic-like curves. Since a parasitic resistance at the negative gate voltage is larger than that at the positive one, it is speculated that a TiN work function approximately locates above the intrinsic energy level of the ZrS$_2$ film.

Ambipolar transfer characteristics, as discussed above, can be explained by the Schottky-barrier FET model,\(^{13}\) as shown in Fig. 8. According to this model, the Schottky barriers for electrons and holes are controlled by the gate voltage. At a positive gate voltage, electrons mainly contribute to the current at a positive $V_{ds}$. By contrast, at a negative gate voltage, holes mainly contribute to the current at the positive $V_{ds}$. As discussed
with both Figs. 3 and 8, symmetrical $I_d-V_{gs}$ curves to $V_{off}$ of 0.4 V suggest that the Fermi energy level of the sputtered ZrS$_2$ film is located approximately in the middle of the band gap, because of the low carrier density of the ZrS$_2$ film.

To discuss the configuration of the band gap for the sputtered ZrS$_2$ film, the band diagrams are shown in Fig. 9. Since the TiN work function is located in the middle of the Si band gap, it is predicted that the bandgap of the sputtered ZrS$_2$ film is surprisingly located at a shallower level than calculated one with a large electron affinity of 5.71. Furthermore, it is speculated that the intrinsic level of the ZrS$_2$ locates a lower level than the TiN work function, which is consistent with the discussion on the gate stack above. These suggest that it is convenient to design the ZrS$_2$ FETs, comprehensively.

To evaluate the intrinsic drivability in the operation of electrons, parasitic resistances are extracted from the $R_{total}$ of the ZrS$_2$ MISFETs as a function of $L_{ch}$ at the $V_{ds}$ of 1.0 V, as shown in Fig. 10. An $R_{ext}$ of 0.038 GΩ cm and $2\Delta L$ of $-1.5 \mu m$ were calculated with the Terada method.

To compare the difference in the conductivity between the holes and electrons, the $g_{m}(V_{gs} - V_{off})$ characteristics without parasitic resistance of the ZrS$_2$ MISFETs are shown in Fig. 11. Here $R_{ext}$ and $2\Delta L$ of electrons are applied even for hole operation. It is observed that the electron mobility is higher than that of the hole one, because the $I_d$ value at the positive $V_{gs} - V_{off}$ is larger than that at negative one. This is consistent with that electron mass is approximately a half of hole one. From these $g_{m}$ values, an electron field-effect mobility of approximately 0.001 cm$^2$ V$^{-1}$ s$^{-1}$ is calculated, which does not meet the previous report. It is because that the Al$_2$O$_3$ gate insulator film influences transport properties of the ZrS$_2$ channel as well as other reports, and also the mobility can be deteriorated by the interface roughness between the ZrS$_2$ and Al$_2$O$_3$ films which might be unfortunately enhanced by SiO$_2$ surface roughness during the bottom TiN-electrode formation.

Table I shows the benchmarks of the ZrS$_2$ MISFETs obtained using different formation methods.
that our FET is superior to other FETs in terms of a small $V_{\text{off}}$ of 0.4 V and a high on/off current ratio of 250, because the contact TiN work function is near the middle of the bandgap of the sputtered ZrS$_2$ channel. Most importantly, conductions of both holes and electrons are performed, because of the higher quality of ZrS$_2$ film and integrated processes to fabricate the MISFETs.

### 4. Conclusions

Chip-level-integrated ambipolar-ZrS$_2$ MISFETs were successfully achieved by sputtering and sulfur-vapor annealing. In particular, the FETs performed both electron and hole conductions with a smaller $V_{\text{off}}$ of 0.4 V. In addition, the bandgap of the sputtered ZrS$_2$ films was predicted to be at a shallower level than the calculated value, which is advantageous for the engineering of the gate and contact metals. This study is an important milestone for the realization of n/p-type unipolar ZrS$_2$ FETs, and it is expected the more discussions to satisfy to precisely control the device operation.

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**Table I.** Benchmark of characteristics for reported ZrS$_2$ FETs obtained using different film formation methods.

| ZrS$_2$ film formation method | Sputtering in this work | CVD$^{[2]}$ | CVD$^{[3]}$ |
|--------------------------------|-------------------------|-----------|-----------|
| Precursors                     | ZrS$_2$ and sulfur       | ZrCl$_2$ and sulfur | ZrCl$_2$ and sulfur |
| Temperature [°C]               | 700                     | 760          | 950        |
| Thickness [nm]                 | ~5                      | 0.71         | A few layers |
| Gate configuration             | Top                     | Bottom      | Bottom     |
| Operation                      | Ambipolar               | Unipolar (e) | Unipolar (e) |
| $V_{\text{off}}$ [V]           | 0.4 (e/h both)          | ~40          | ~10        |
| $R_{\text{on/off}}$            | ~250                    | ~15          | ~25        |
| Mobility                       | 0.0001                  | 0.1–0.8      | ~0.1       |

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