Compact silicon double and triple dots realized with only two gates.

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We report electronic transport on silicon double and triple dots created with the optimized number of two gates. Using silicon nitride spacers two dots in series are created below two top gates overlapping a silicon nanowire. Coupling between dots is controlled by gate voltages. A third dot is created either by combined action of gate voltages or local doping depending on the spacers length. The main characteristics of the triple dot stability diagram are quantitatively fitted.

Semiconducting quantum dots are usually made with three gates: one plunger gate to control the density of carriers and two gates to control the in and out tunneling rates. A recent achievement is a controlled silicon Single Electron Transistor (SET) using only one gate. This MOS-SET departs from the usual MOSFET by a specific design of channel junctions to source and drain. Tunnel barriers are formed by undoped silicon segments and a quantum dot is created by accumulation of carriers below the gate. The undoped silicon barriers sit below spacers which are used as a mask during source and drain implantation.

In this work we show that the association of two MOS-SETs in series — the most natural extension of the single MOS-SET — yields both a well controlled double dot with tunable inter-coupling and a triple dot. Within other technologies triple dots usually require many gates. Triple dots have been realized in 2DEG and in silicon using top and side gates. The advantage of a single gate design becomes crucial when compact arrangements of multiple quantum dots are required, for instance to create high fidelity electron pumps, latching switches, quantum cellular automata, single-electron-parametron devices, non-local interacting qubits, or rectifier devices.

Recently silicon quantum dot molecules, i.e. a double dot with tunable coupling, have been built with one larger upper gate plus four side gates or three top gates. Reducing further the number of gates has been possible at the cost of stochasticity: a coupled quantum dot was obtained with two top and one upper gate by relying on the static disordered potential arising from the Si/SiO₂ buried oxide interface rugosity. One advantage of our technology is that our double and triple dots are smaller and/or simpler than previously reported.

Our samples are produced on 200 mm silicon-on-insulator (SOI) wafers in a CMOS platform. A 200 nm long, 20 nm thick and W = 20–60 nm wide silicon nanowire is etched and covered by two L₉ = 30–60 nm long polysilicon gates isolated by 5 nm thick SiO₂ gate oxide (Fig. 1). The spacing between gates is L₉₉ = 30–60 nm. 15 or 40 nm thick silicon nitride spacers are deposited on both sides of the gates. Therefore for samples with long (40 nm) spacers (samples 1 and 2) the silicon region between the gates is undoped as it is masked during the heavy As implantation of the source and drain. On the contrary it is doped for samples with short (15 nm) spacers (sample 3). Samples with thinner SOI (10 nm)

FIG. 1. schematic layout of the coupled MOS-SETs: a) long silicon nitride spacers protecting the central region of SOI during source-drain implantation (samples 1 and 2). b) with short spacers a dot is created by implanted arsenic donors in the central region (sample 3). Below each case the schematic profiles of the bottom of the conduction band are drawn for various gate voltages. The horizontal line is the Fermi energy fixed by the source and drain. c) SEM micrograph of a typical sample before spacers deposition. The gate length is 60 nm and the spacing between gate 30 nm. d) Equivalent circuit for the triple dot system. The capacitance values corresponding to sample 2 are given in aF.
have also been studied and the increase of the period of Coulomb blockade oscillations (CBO) shows that the size of each MOS-SET is further reduced (not shown). The typical charging energy of our MOS-SETs is 2 meV.

Figure 2 shows the drain-source current versus gate voltages applied on each gate at $T = 1$ K in a device with 40 nm long spacers. Two nominally identical MOS-SETs appear below the two gates, with CBO periods very constant in gate voltages. Similar CBO periods and threshold voltages are observed for the two MOS-SETs, illustrating the reproducibility of the fabrication process. At low ($V_{g1}, V_{g2}$) the two dots are decoupled and the 2D plot exhibits the expected square lattice pattern (not shown). At intermediate ($V_{g1}, V_{g2}$) the dots are capacitively coupled and the 2D plot shows the so-called honeycomb pattern (Fig. 2 left panel). The gate capacitances $C_{g1}, C_{g2}$ and the interdot capacitance $C_{12}$ are estimated to 40 aF, 40 aF and 20 aF respectively. At large ($V_{g1}, V_{g2}$) the tunnel coupling becomes non negligible and the 2D plot exhibits characteristic wandering anti-diagonals (Fig. 2 central panel). At even larger gate voltages the two dots merge into a single island (Fig. 2 right panel). In that case the period along the diagonal in ($V_{g1}, V_{g2}$) plot is half that of the two separated dots, as expected since the gate capacitance is approximately twice larger for the single merged dot. This evolution, similar to the ones reported in Ref. 14 and 15, shows that a tunable double dot is obtained with only two gates. The absence of independent control on the carrier’s number and interdot coupling is compensated by the compacity and simplicity of our devices.

The transition from two independent dots towards a single island is realized by increasing simultaneously the two gate voltages which both control the potential of the undoped silicon nanowire segment separating the two MOS-SETs. This evolution is not monotonic. A periodic antidiagonal (i.e. constant $V_{g1} + V_{g2}$ value) pattern is superimposed (see Fig. 3). This period results from Coulomb blockade on a third intermediate dot created in the silicon nanowire, at equal distance from both gates. It arises from the combined action of the two unscreened gate potentials in samples with long spacers (see Fig. 1). The whole system then behaves as three dots in series controlled by two gate voltages. In order to model this triple dot we consider the electrostatic configuration depicted in Fig. 3. The conductance is simulated within the orthodox model of Coulomb blockade without cotunneling. Cotunneling through dot 3 is nevertheless taken into account as a direct tunnel coupling between dots 1 and 2. For the sake of simplicity the five tunnel junctions tunneling rates are taken equal. The capacitance values indicated in Fig. 3 give the best fit for the periods measured in sample 2. These values also describe well sample 1. We note that these tunnel capacitances are larger than their simple planar geometrical approximations ($C_{12} = 20$ aF instead of 3 aF for instance). This effect is attributed to the large polarizability of electrons in the tunnel barriers with small energy height.

The tunnel coupling between the two MOS-SETs as well as the occurrence of the third dot can also be tuned by doping. Indeed in samples with small spacers (sample 3) the central region of the SOI nanowire is not protected and is therefore n-doped (see Fig. 3). Thus at zero gate voltages the central region contains electrons. This doped architecture is reminiscent of the locally implanted silicon quantum dots. The voltage at which source-drain current is detected at low temperature is $V_{g1} = V_{g2} \simeq -0.1$ V in short spacers samples, whereas it is detected at larger values (+0.2 V) in long spacers samples. The honeycomb pattern for both kind of samples exhibit similar periods, showing that the characteristics of each MOS-SET is not affected by the central doping. On the contrary the central dot is strongly modified: the period of the anti-diagonals is reduced by a factor 2.5, which indicates a bigger central dot more capacitively coupled to gates (see Fig. 3b).

On Fig. 3a a detail of the diagram is shown at lower temperature ($T = 1$ K) in sample 2 for one of these anti-diagonals. The corresponding simulation shown in Fig. 3b reproduces the distorted honeycomb pattern experimentally observed, except for lines joining the triple points which are a consequence of cotunneling. The number of electrons ($N_1, N_2, N_3$) on each dot is indicated in Fig. 3b. $N_1 \simeq 60, N_2 \simeq 60, N_3 \simeq 20$ are determined by dividing $V_g$ counted from the threshold (+0.2 V) by the CBO period and the figure is periodic in $N_1, N_2, N_3$ (see Fig. 3b). Far from the degeneracy ($N_3 \leftrightarrow N_3 + 1$) of dot 3 one recovers the honeycomb pattern for the double dot system. Near degeneracy we observe an alternance of pentagones and diamonds. Up to eight triple points per cell are predicted for a triple dot. In case of high symmetry and perfect matching between the capacitances these eight points can reduce to four quadruple points, as observed in both our simulation and data (see Fig. 3c).

In conclusion we have shown that the MOS-SET
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