The Effects of Carbon on the Bidirectional Threshold Voltage Instabilities Induced by Negative Gate Bias Stress in GaN MIS-HEMTs

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ABSTRACT

In this paper, numerical device simulations are used to point out the possible contributions of Carbon doping to the threshold voltage instabilities induced by negative gate bias stress in AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistors (MIS-HEMTs). It is suggested that Carbon can have a role in both negative and positive threshold voltage shifts, as a result of the changes in the total negative charge stored in the Carbon-related acceptor traps in the GaN buffer as well as the attraction of Carbon-related free holes to the device surface and their capture into interface traps or recombination with gate-injected electrons. For a proper device optimization of Carbon-doped MIS-HEMTs, it is therefore important to take these mechanisms into account, in addition to those related to defects in the gate dielectric volume and interface which are conventionally held responsible for threshold voltage instabilities.

KEYWORDS

GaN Power Devices; Threshold Voltage Instability; Negative Gate Bias Stress; NBTI; Carbon Doping.

1. INTRODUCTION

GaN technology has eventually found its way to the power electronics market [1, 2], thanks to the lower total losses at higher breakdown voltage and higher switching frequency allowed by GaN-based transistors compared to Si power devices [3]. While normally-off devices, either based on the junction-gated High-Electron Mobility Transistor (HEMT) (aka p-GaN HEMT) or the fully recessed gate Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) concepts are intensively being developed at both research and industry level [1, 2], the two-chip cascade connection of a low-voltage Si MOSFET with a high-voltage, normally-on AlGaN/GaN Metal Insulator Semiconductor High Electron Mobility Transistor (MIS-HEMT) still represents a commonly adopted solution mainly for its compatibility with Si drivers [1]. Concerning the substrate material for the GaN device, a large-area Si wafer is the solution of choice for cost competitiveness [1, 2].

Given the insulated-gate structure of the MIS-HEMT, threshold-voltage ($V_T$) stability is a major concern critically impacting yield [4]. For normally-on devices with negative threshold voltages of several volts, $V_T$ stability after the application of a large and negative gate bias is, in particular, a key aspect that needs careful evaluation during technology development. Assessing the $V_T$ stability under negative gate bias is important also for normally-off devices, as negative gate bias can be applied to prevent false turn-on and ensure safe operation against the voltage spike on the gate [5]. These considerations have actually been the rationale for several recent research works on both normally-on MIS-HEMT and fully-recessed MOSFETs [5–13]. These works can be divided into three categories depending on the sign of the observed $V_T$ shifts: 1) works showing a negative $V_T$ shift (i.e. $V_T$ becoming more negative) [6–8], 2) those illustrating a positive $V_T$ shift (i.e. $V_T$ becoming less negative) [5, 9–11], 3) the ones demonstrating $V_T$ shifts of both sign, depending on device type or stress conditions [12, 13].

In the above published works, the physical mechanism that is held responsible for the negative $V_T$ shifts is: A) electron emission from interface and/or border traps [6, 7,
In GaN power devices, Carbon (C) is widely adopted as compensation doping to suppress the unintentional conductivity in the GaN buffer and transition layers underlying the MIS-HEMT channel and to avoid premature breakdown related to source-to-drain punch-through [1, 14, 15]. The possible contributions of C doping to $V_T$ instabilities are however generally disregarded with the exception of [8], despite (i) C related acceptor traps are of course not only present in the gate-drain access region (where they are held responsible for dynamic on-resistance, $R_{ON}$, degradation after off-state stress [16, 17]) but also under the gate (where they could impact $V_T$ stability after negative gate bias stress), (ii) C-doped GaN is a weakly p-type semiconductor [16] and, in response to large and negative gate voltages, free holes can in principle drift to the surface and accumulate/recombine under the gate at the dielectric/barrier interface.

The aim of this paper is to investigate the possible role(s) played by C doping within the complex picture of negative gate bias $V_T$ instabilities in AlGaN/GaN MIS-HEMTs. This has been pursued by means of device simulations, allowing the effects of C doping to be isolated from mechanisms A)-E) above, that however remain likely to play a role and whose impact depends on the specific device and the sign of the $V_T$ shift observed experimentally.

The paper is organized as follows. In Section 2, the modeling framework is illustrated, including analyzed device structures and relevant physical models. Results are shown and discussed in Section 3. Conclusions are eventually drawn in Section 4.

2. MODELING FRAMEWORK

The two-dimensional (2D) numerical device simulations were carried out with the SDevice simulator (Synopsys Inc.) [18]. The analyzed structures are sketched in Fig. 1(a) and (b), resembling a typical power AlGaN/GaN MIS-HEMT and AlGaN/GaN Schottky-gate HEMT, respectively. While the focus of this paper is on AlGaN/GaN MIS-HEMTs for power switching applications, an AlGaN/GaN HEMT sharing the same epitaxial structure is also simulated and adopted as a useful, comparison case. What we are proposing here is a “simulated experiment”, allowing us to decouple $V_T$ instability effects related to Carbon from those connected to the gate dielectric. This will be done by considering the latter completely ideal or affected by defects and leakage currents and by even removing it so as to obtain a Schottky gate HEMT with the same epitaxy as the MIS-HEMT. Both structures have a grounded, p-type Si substrate, a C-doped GaN buffer (1.5 µm), an unintentionally doped (UID) GaN channel (150 nm), an $Al_{0.25}Ga_{0.75}N$ barrier (25 nm) and a Si$_3$N$_4$ passivation layer over the two access regions (150 nm). The MIS-HEMT features also a gate dielectric $Al_2O_3$ layer (15 nm) that is added to the structure after partially recessing the barrier and leaving 4 nm of residual AlGaN under the gate.

Charge transport was modelled by means of the drift-diffusion model. Electron mobility in the undoped and doped GaN layers were set to 1800 cm$^2$/V·s [19] and 900 cm$^2$/V·s [20], respectively. The latter value was taken as representative of a highly compensated GaN layer [20]. For easier simulation convergence, a silicon-like, monotonic velocity-field curve was assumed, with an electron saturation velocity of 1.5x$10^7$ cm/s [19]. Table 1 collects the most relevant geometrical and model parameters of the simulated structures. Hole mobility and saturation velocity were left to their default values. All other material-specific parameters, including mobilities in materials other than GaN, dielectric constants, SRH and Auger recombination parameters, were left to the simulator’s default values for the respective material. Impact ionization and self-heating were neglected. Piezoelectric polarization was included by using the default strain model of the simulator. Note that at the passivation/barrier and gate insulator/barrier interfaces the polarization model was deactivated. This approach is equivalent to assume that the polarization charge is completely compensated by a positive fixed surface charge [21].

As far as the trap model is concerned, a fully dynamic approach was adopted, with one SRH trap-balance equation...
different GaN power HEMTs yielding an acceptable accuracy description of dielectric transport mechanisms like adopted leaky dielectric model is simplified, it allows us to point out the possible interplay between interface traps and holes. The actual energy position of donor traps, if sufficiently shallow, has little influence on simulation results. C-related donors could actually be moved even closer to $E_C$ or be modelled as completely ionized dopants [34], in agreement with recent hybrid-functional Density Functional Theory (DFT) calculations [35, 36], without significant changes on simulation results. On the other hand, assuming that only acceptor levels are introduced with concentrations in the order of the nominal C density ($10^{18}-10^{19}$ cm$^{-3}$) resulted in all our previous works in a very large overestimation of current-collapse effects [27–30]. An experimental indication that C doping introduces also donor levels (besides dominant acceptor ones) can be found in [37]. The capability of the acceptor-donor model for C doping to reproduce source-drain leakage currents and off-state breakdown is demonstrated in [38].

### 3. RESULTS AND DISCUSSION

Simulated drain-current per 1-mm device width ($I_D$) vs gate-source-voltage ($V_{GS}$) characteristics at a drain-source voltage ($V_{DS}$) of 0.5 V of “fresh” and “stressed” devices are shown in Figure 2(a)-(d) for the following four cases: (I) the MIS-HEMT with ideal gate dielectric and without $D_{IT}$, (II) the MIS-HEMT with ideal gate dielectric but with $D_{IT}$, (III) the MIS-HEMT with both conductive gate dielectric and $D_{IT}$, (IV) the Schottky-gate HEMT. The four different cases are labelled I-IV and are collected in Tab. 2 for easier reference to the readers. Note that “Fresh” device here means that the simulation of the transfer curve was carried out starting from a ($V_{GS}, V_{DS}$) = (0 V, 0 V) equilibrium bias point by applying short $V_{DS}$ and $V_{GS}$ sweeps. “Stressed” device means that the same simulation was carried out (with the same short sweep times) immediately after application of a 100-s negative gate.

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**Table 1. Geometrical and model parameters of the simulated MIS-HEMT.**

| Geometrical Parameters (µm) | Model Parameters |
|----------------------------|------------------|
| Si$_3$N$_4$ Passivation Thickness | 0.15 | 2DEG Low-field mobility $\mu_{0a}$ (cm$^2$/V·s) | 1800 |
| Al$_2$O$_3$ Gate Insulator Thickness | 0.015 | Buffer Low-field mobility $\mu_{0b}$ (cm$^2$/V·s) | 900 |
| AlGaN Barrier Thickness | 0.025 | Saturation velocity $v_{sat}$ (cm/s) | 1.5x10$^7$ |
| Residual Barrier Thickness (Under the Gate) | 0.004 | Al molar fraction x (AlGaN:x-N) | 0.25 |
| GaN:UID Channel Thickness | 0.150 | UID Doping (cm$^3$) | 1x10$^{15}$ |
| GaN:C Buffer Thickness | 1.5 | Deep Acceptor Conc. $N_{CA}$ (cm$^3$) | 8x10$^{17}$ |
| Gate-to-Source Length $L_{GS}$ | 1 | Deep Donor Level $E_{CA} - EV$ (eV) | 0.9 |
| Gate-to-Drain Length $L_{GD}$ | 10 | Deep Donor Conc. $N_{CD}$ (cm$^3$) | 4x10$^{17}$ |
| Gate Length $L_G$ | 0.7 | Deep Donor Level $E_C - E_{CD}$ (eV) | 0.11 |

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**Table 2. Simulated devices for the different cases in Figures 2-6.**

| Case | Device |
|------|--------|
| I    | MIS-HEMT with Ideal Insulator and without $D_{IT}$ |
| II   | MIS-HEMT with Ideal Insulator but with $D_{IT}$ |
| III  | MIS-HEMT with Conductive Insulator and $D_{IT}$ |
| IV   | HEMT |

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In Case II, in our simulations despite the absence of interface/border is induced by further increasing shift up to $V_{GS,STR} = 10$ V, while a very small additional shift is induced by further increasing $V_{GS,STR}$. This effect is present in our simulations despite the absence of interface/border traps at the dielectric/barrier interface and can be considered as the contribution of C-related traps to the negative $V_T$ shift. In Case II, $D_{IT}$ is added to the simulated device, yielding a larger negative $V_T$ shift compared to Case I for the same $V_{GS,STR}$. In this case, the negative $V_T$ shift significantly increases at increasing $V_{GS,STR}$ over the entire $V_{GS,STR}$ range considered. The extra negative $V_T$ shift compared to Case I can be attributed to the $D_{IT}$. A bidirectional $V_T$ instability is instead present in Case III, with $V_T$ shifting negatively for $V_{GS,STR}$ values up to 10 V, going back about to the “fresh” value for $V_{GS,STR}= 15$ V, and eventually exceeding the initial
value for the largest \( V_{GS,STR} \) of 20 V. This is the combined effect of C doping and gate electron injection. Interestingly (but not surprisingly), Case IV shows a similar trend to that of Case III, suggesting that a Schottky gate has a similar impact on the \( V_T \) instability as an insulated one if the gate insulator conductivity is non-negligible.

The physical mechanisms underlying the different \( V_T \) shifts can be understood with the aid of Figs. 4-6, showing the gate stress bias dependence of the 2D integrals under the gate of the following quantities: the negatively ionized C-related acceptor trap concentration \( (N_C^-) \), the free hole density \( (p) \), and the positively ionized interface trap density \( (N_{IT}^+) \). All of the three integrals are extended to the device region under the gate footprint from the gate dielectric/barrier interface (MIS-HEMT) or the Schottky contact (HEMT) to the buffer/nucleation layer interface.

The \( N_C^- \) integral features a non-monotonic dependence on \( V_{GS,STR} \) for all the four Cases I-IV above, see Fig. 4. This results from the presence of two opposite processes taking place during the 100-s stress phase at negative gate bias and dominating at small and large \( V_{GS,STR} \), respectively: 1) the drifting of holes from the two access regions towards the gate region of the GaN buffer and the consequent hole capture increase into the C-related acceptor traps, leading to the decrease in the \( N_C^- \) integral under the gate; 2) the attraction of free holes from the GaN buffer region to the device surface and consequent enhanced hole emission from C-related acceptor traps, this instead leading to the increase in the \( N_C^- \) integral under the gate. This non-monotonic dependence of the \( N_C^- \) integral translates to bidirectional \( V_T \) shifts in cases III and IV, whereas other phenomena are at play in cases I

\[ \int_{x}^{y} N_C^- \, \text{d}x \text{d}y \]

\[ \int_{x}^{y} p \, \text{d}x \text{d}y \]

\[ \int_{x}^{y} N_{IT}^+ \, \text{d}x \text{d}y \]
and II compensating the increase in the \( N_C^- \) integral at large \( V_{GS,STR} \) and thus making \( \Delta V_T \) always negative.

The \( p \) integral becomes significant at sufficiently large \( V_{GS,STR} \) for Case I and II, i.e., for the MIS-HEMT device with ideal gate dielectric, whereas it is always zero in Case III and IV, i.e., for the MIS-HEMT with conductive gate dielectric and the Schottky-gate HEMT, see Fig. 5. This results from the accumulation of free holes at the dielectric/barrier interface that can take place only in the MIS-HEMT structure with ideal gate dielectric (Case I and II). This accumulated positive charge contributes to making the \( V_T \) shifts always negative even at large \( V_{GS,STR} \). On the other hand, holes attracted at the surface recombine with gate-injected electrons in the MIS-HEMT with conductive gate dielectric (Case III) or leak out from the device at the Schottky-gate contact in the HEMT (Case IV), explaining why the \( p \) integral is zero in these two cases.

Figures 6 and 7 show the 2-D contour plots of the \( N_C^- \) and \( p \) distributions in the device near the gate region for Case II and III, respectively. These figures better illustrate the difference between the above cases in terms of obtained \( \Delta V_T \) trends. In Case II, the accumulation of free holes at the gate/insulator interface is much higher than in Case III leading to negative \( \Delta V_T \) only. In the latter scenario, Case III, the holes emitted from C-related acceptors recombine with the electrons injected from the gate. Thus, the increase in the negative ionized charge in the buffer prevails determining the positive \( \Delta V_T \).

As can be seen in Fig. 8, the \( N_C^- \) integral is obviously always zero in Case I and IV where no \( D_{IT} \) is present. It can become significant for Case II, i.e., for the MIS-HEMT device with \( D_{IT} \) but with ideal gate dielectric, as a result of the concurrent effect of electron emission and hole capture into
interface traps. These effects explain the large, negative $V_T$ shifts obtained for case II. It is finally non-zero but saturates at large $V_{GS, STR}$ for Case III, i.e. for the MIS-HEMT device with $D_{IT}$ and conductive gate dielectric as a consequence of the competing effect of the trapping of gate-injected electrons into the interface traps and/or electron-hole recombination at the interface.

The contribution of the $D_{IT}$ to the $V_T$ instability is further analysed in Fig. 9, where $\Delta V_T$ is plotted against the stress voltage for case III for two different $D_{IT}$ values. As can be noted, a higher $D_{IT}$ results in a larger negative $V_T$ shift. In devices with large $D_{IT}$, the effect of C doping on the $V_T$ instabilities can therefore be masked. On the contrary, if/when the quality of the gate insulator/barrier interface is optimized and interface defects are reduced, $V_T$ instabilities still occur as a result of Carbon doping in the buffer.

The impact of temperature is illustrated by Fig. 10, showing $\Delta V_T$ as a function of stress time for different temperatures. The analysed device is the MIS-HEMT with leaky dielectric (case III) featuring the more complex behaviour among those shown in Fig. 3, i.e. a bidirectional $V_T$ instability. From Fig. 10, it can be noted that (i) a bidirectional $V_T$ instability can be present not only depending on stress bias at room temperature (see Fig. 3) but also on increasing stress time for a given stress bias, (ii) increasing temperature shifts the $\Delta V_T$ curves to the left, this being a result of the shortened hole emission processes from C-related traps. This behaviour is similar to that reported for GaN MOSFETs in [13].

4. CONCLUSIONS

We have analyzed by means of numerical device simulations the possible role played by Carbon doping in the negative gate bias $V_T$ instabilities in AlGaN/GaN MIS-HEMTs. Bidirectional threshold voltage shifts can at least in part be related to C doping, as a result of the modulation of the negative charge trapped into the C-related acceptors as well as the accumulation/recombination at the device surface of free holes generated by C doping.

More specifically, our simulation results point out that negative $V_T$ shifts can be the result of:

1) the increase in the positive interface charge due to electron emission from interface traps,
2) the decrease in the total negative charge stored in the C-related acceptors in the GaN buffer,
3) the increase in the positive interface charge due to hole capture into interface traps, where holes are provided by the C doping and not necessarily by a high-field electron-hole generation mechanism.

Process 1) is the one that is conventionally assumed and can be present also in devices without C doping. Processes 2) and 3) are consequences of the C doping.

On the other hand, positive $V_T$ shifts can be the result of:

1) the increase in the negative charge stored in the insulator due to electron injection from the gate (in our simulations oxide traps are concentrated at the insulator/barrier interface),
2) the recombination of holes provided by the C doping (and attracted to the device surface) with electrons injected from the gate.

Process 1) is the one that is conventionally assumed and can be present also in devices without C doping. Process 2) is an effect of C doping.

In actual devices, the role of Carbon in $V_T$ shifts can be masked by or, as mentioned above, have an interplay with other effects. Nevertheless, it is important for the technologist not to neglect it when interpreting $V_T$ instability experiments during the device optimization loop. Moreover, our analysis points out that, even in devices with optimized gate dielectric and interface, residual $V_T$ instabilities, related to Carbon doping, can still be present. These detrimental effects should ultimately be traded off with breakdown voltage similarly to what is done for Carbon-induced dynamic Ron degradation.

As a guideline for technologists, our results also suggest that negative-only $V_T$ shifts at varying negative gate bias stresses are typical of MIS-HEMTs with negligible gate dielectric conductivity, whereas bidirectional, or even positive-only $V_T$ shifts can be associated with non-negligible gate electron injection and leakage current through the gate dielectric.

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