Voltage Source Converters Connected to Very Weak Grids: Accurate Dynamic Modeling, Small-Signal Analysis, and Stability Improvement

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ABSTRACT The interfacing of the vector-controlled voltage-source converters (VSCs) into weak grid (WG) systems can induce severe instabilities. This is attributed to interactions between the vector control of the VSCs and the high impedance of the WG. The weak connection limits the amount of active power that can be injected by the VSC to the WG. In this work, the small-signal analysis is used to derive; first, a transfer function that helps to design the controller of the VSC output voltage based on the VSC-WG accurate dynamics; second, the full-order state-space model of the VSC-WG system. A modal analysis is then conducted to develop the participation factors to characterize the influencing states on the dominant modes of the system, followed by a sensitivity analysis to evaluate the influence of the vector control gains and other parameters on the dominant modes. The results of the modal analysis confirm that instabilities at the nominal power are inevitable for VSCs connected to very weak grids (VWGs). Inspired by this shortcoming, a novel compensation method is proposed to mitigate the dynamic instability of VSCs connected to VWGs. Finally, several offline time-domain simulations and hardware-in-the-loop (HIL) real-time experiments are conducted to verify the validity of small-signal analysis, validate the effectiveness of the proposed compensation method; and investigate the performance of the system under challenging scenarios such as sudden variations in the phase angle of the grid.

INDEX TERMS Active compensation, stability analysis, short circuit ratio (SCR), small-signal analysis, voltage source converter, weak grid.

I. INTRODUCTION
The growth of energy demand, environmental and economic problems related to fossil fuels, power grid limitations, and economic incentives rising from electricity market are among the reasons behind the adoption of the distributed generation (DG) systems to support and eventually replace the conventional power plants [1]–[3]. DG units often utilize clean energy sources such as fuel-cells and renewable energy resources (RESs) such as hydro, wind, and solar energy. Therefore, they can provide clean energy for remote or dispersed areas and locations [1], [3].

The two-level three-phase voltage source converters (VSCs) are the state-of-the-art technology to interface DGs into the power grid due to the high switching frequency capability and the ability to regulate bidirectional active and reactive powers independently [1]–[4]. In the context of grid-connected VSCs, the conventional control method which is widely accepted in the industry is the vector control (VC) [1]–[4]. Conventionally, the VC scheme is implemented in the direct-quadrature reference frame (dq-RF) which is synchronous with the phase angle of the point of common
coupling (PCC) voltage, and hence a phased-locked loop (PLL) is employed to generate the synchronization angle [1], [4]. If the equivalent impedance between the power grid and the PCC is negligible, the PCC voltage magnitude and frequency can be assumed to be constant, and hence the control of the VSC can be designed independent of the grid parameters. In this situation, the grid is known as a stiff grid (SG). However, if the equivalent impedance is not small enough, the previous assumption is not valid anymore as the PCC voltage exhibits fluctuations, especially during transient conditions. Moreover, the VSC and the grid dynamics become undesirably coupled [5]. In this case, the grid is known as a weak grid (WG). The grid impedance is mainly dictated by the long transmission lines and low power transformers [7]. Since wind farms and photovoltaic units are installed in locations far from the load centers [8], [9], the integration of DGs usually occurs in a WG infrastructure. Moreover, the WG impedance might have a wide range of variations due to faults, loading conditions, and grid reconfigurations by the operator [7], [9]–[11]. To quantify the grid strength or stiffness, the short circuit ratio (SCR) is utilized which is defined as the ratio of the grid short circuit level at the PCC to the rated dc power of the VSC [11]. A grid is considered a very weak grid (VWG) when the SCR is 1. However, the control design requires the maximum available power capacity of the VSC. However, this method often limits the transient response of the system [19]. Moreover, SCR = 1.25 is the maximum stable condition which is obtained for the VSC-WG system in previous works. However, the instability problem of the VSC-WG systems at SCR = 1, which is the worst-case scenario [24], does still exist.

The second method, as addressed in [7], [19]–[22], is to change the magnitude or phase angle of the VSC output impedance by adding auxiliary feedforward loop(s) to the current control path of the VC. However, the minimum SCR level studied in all these cases equals two. Another common feature in most of these methods is that they change the steady-state response of the VSC by modifying the VSC output impedance as an attempt to enhance the stability of the VSC-WG system.

The third method, as discussed in [8], [9], [23], is to eliminate the conventional PLL instead of dealing with its negative effect on the system stability by replacing the VC method by the power synchronization control (PSC). The PSC is a new concept in controlling the VSC output power in grid-connected applications, where the VSC is controlled to imitate the characteristics of a synchronous machine. The paramount advantage of the PSC method is that the VSC does not face any limitation to inject the active power into the VWGs. However, as the ac current is not controlled directly in the PSC, the performance under fault conditions is compromised. Therefore, there is still a great interest to improve the conventional VC method to adapt to the VWGs and maintain the direct current regulation.

Another variant of the VC method is introduced in [5] where the inner current control (CC) of the VSC is replaced by a voltage controller while the PLL is preserved in the control structure. In this case, the active and reactive power controls are the outer loops of the overall control system. However, similar to the PSC, there is no direct control on the VSC current. Moreover, the stability of the system under study has been verified at SCR = 3 which is not close enough to the worst-case scenario. An improved version of the VC strategy is proposed in [24], where the classic outer loop is modified by additional four decoupling gains based on the gain-scheduling technique. The VSC shows a stable performance at SCR = 1. However, the control design requires lookup tables to schedule eight control parameters following the operating point variation. Therefore, there is still a need for a simpler VC-based method to improve the VSC-WG system stability in the VWG conditions [25].

Inspired by the shortcoming of the previous works to present a simple method to mitigate the instability problem of the VC-based VSC in the VWG conditions, a simple active compensation method is proposed in this work that can be easily integrated with the existing VC scheme. The proposed method does not require any change in the VSC control parameters. Also, upon using the compensation method, the steady-state measures of the VSC remain unchanged. Moreover, it is shown that the stability region of the VSC-WG system is increased to SCR = 1 which is the worst-case scenario. The contributions out of this work are summarized as follows.

- Implementation of the compensated VSC-WG system to achieve a stable performance at SCR = 1, i.e., the VWG condition.
- Derivation of an accurate analytical transfer function of the PCC dynamics, which can be used for designing the PCC control system using single-input-single-output (SISO) control tools.
- Derivation of the small-signal state-space full-order model of the vector controlled VSC-WG system augmented with the compensation method where the influence of the ac voltage control (AVC), the PLL, the CC, and the dc-link voltage control (DVC) is considered.
• Performance comparison of the VSC-WG systems with and without the proposed active compensation method in terms of the dynamic response, the steady-state response, and the small-signal stability.

The rest of the paper is organized as follows. In Section II, the mathematical model of the VSC-WG system and the controllers are introduced; followed by a discussion of the tuning of the controllers parameters. Section III presents the small-signal model of the VSC-WG system followed by extensive modal analysis under the VWG conditions. In Section IV, the modeling and design of the proposed active compensation method are discussed. Section V provides the large-signal simulation results. The experimental verification of the proposed method is presented in Section VI. Conclusions are presented in Section VII.

II. DYNAMIC MODELING OF THE VSC-WG SYSTEM

Fig. 1(a) shows the VSC-WG system which includes a VSC with the nominal dc power \( P_n \) and an LC filter at the ac-side with a series resistance \( r_d \) as a passive damping [33]. The VSC is connected to an ideal voltage source, which emulates the power grid, at the PCC via a step-up power transformer and the grid impedance. A generic dc source, modeled as a dc current source, in parallel with a dc capacitor is interfaced by the VSC at the dc-link. The grid is assumed strong enough so that it can be modeled by a voltage source with a constant magnitude \( V_g \) and a constant frequency \( \omega_g \). It follows from the definition of \( SCR \) that

\[
SCR = \frac{V_g^2}{P_n (r_g + j\omega_g L_g)} \tag{1}
\]

where \( r_g \) and \( L_g \) are respectively the grid resistance and inductance. The complete system parameters are depicted in Appendix A.

The VSC is controlled by the VC scheme. The VSC control system is developed in the dq reference frame (dq-RF) which rotates synchronously with the converter angle \( \theta_{vsc} \). As shown in Fig. 1(b), the PLL provides the required angle \( \theta_{vsc} \) for the VSC control system by synchronizing the VSC to the PCC voltage. The equations describing the VSC-WG system in the following parts are written in the dq-RF. All equations are expressed in the frequency domain, wherein \( s \) represents the Laplace operator. The dynamics of the VSC, CC, PLL, DVC, and AVC are modeled in the following subsections.

A. MATHEMATICAL MODEL OF THE POWER CIRCUIT

Based on Fig. 1(a), the mathematical models of the grid impedance and the LC filter are given as

\[
\begin{align*}
\frac{v_{dq}}{v_{eq}} &= \frac{v_{od}}{v_{oq}} = \frac{Z_f(s)}{Z_g(s) + \omega_{vsc} L_f} \left[ i_{fd} - \frac{i_{qf}}{i_{fd}} \right] \\
\frac{v_{od}}{v_{oq}} &= \frac{v_{gd}}{v_{gg}} = \frac{Z_g(s)}{Z_g(s) + \omega_{vsc} L_f} \left[ i_{od} - \frac{i_{qo}}{i_{od}} \right] \\
\frac{i_{fd}}{i_{qf}} &= i_{od} + sC_f \frac{v_{cd}}{v_{cq}} + \omega_{vsc} C_f \left[ -v_{eq} \right] \frac{v_{cd}}{v_{cq}} \tag{4}
\end{align*}
\]

where \( Z_f(s) = r_f + s\omega_f L_f \) and \( Z_g(s) = r_g + s\omega_g L_g \) are the impedances of the filter inductor and grid impedance, respectively.

B. CURRENT CONTROL

The block diagram of the CC loops, which is the innermost control loop, is shown in Fig. 2. As shown, a pair of similar proportional-and-integral (PI) compensators, denoted by \( G_i(s) = K_{pc} + K_{ic} s^{-1} \), regulate the currents \( i_{fd} \) and \( i_{qf} \) to the corresponding reference values \( i_{ref} \) and \( i_{qref} \), that are assigned by the outer control loops; the DVC and AVC, respectively. Therefore, the following holds.

\[
\begin{bmatrix}
u_{cd} \\
u_{eq}
\end{bmatrix} = \left[ \begin{bmatrix} v_{od} \\
v_{oq}
\end{bmatrix} - r_d \left[ \begin{bmatrix} i_{fd} - i_{od} \\
i_{qf} - i_{qo}
\end{bmatrix} \right] \right]
\tag{5}
\]

where \( Z_f(s) = r_f + s\omega_f L_f \) and \( Z_g(s) = r_g + s\omega_g L_g \) are the impedances of the filter inductor and grid impedance, respectively.
disturbances, i.e., $v_{ad}$ and $v_{aq}$ [4]. If the PWM dynamics are neglected and the fundamental components of the terminal voltage is considered, the following holds [4].

$$
\begin{bmatrix}
    v_{id} \\
    v_{iq}
\end{bmatrix} = \begin{bmatrix} m_d & m_q \\ m_q & m_d \end{bmatrix} \frac{v_{ref}}{2} \begin{bmatrix} 1 \\ -1 \end{bmatrix}
$$

(8)

Applying (6)–(8) into (2) results in the following transfer function for the CC loops.

$$
T_c(s) = \frac{i_{fd}}{v_{ref}} = \frac{i_{fd}}{v_{ref}} = \frac{K_{pc}s + K_{ic}}{L_d s^2 + (r_f + K_{pc})s + K_{ic}}.
$$

(9)

C. DC-LINK VOLTAGE CONTROL

Neglecting the power losses in the VSC switches, the dc power $P_{dc}$ is equal to the instantaneous active power at the VSC terminals in Fig 1(a), which in turn, is the sum of the instantaneous power corresponding to the LC filter and the active power of the VSC injected to the grid, $P_{ac}$. Therefore, the following can be written [4].

$$
v_{dc}i_{dc} = \frac{1}{2} C_{dc}v_{dc}^2 + \frac{3}{4} L_f s (i_{fd}^2 + i_{fq}^2) + \frac{3}{2} r_f (i_{fd}^2 + i_{fq}^2) + \frac{3}{2} (v_{ad}i_{fd} + v_{aq}i_{fq}).
$$

(10)

Fig. 3(a) shows the block diagram of the DVC control loop. (a) Large-signal model. (b) Small-signal model.

FIGURE 3. Block diagram of the DVC control loop. (a) Large-signal model. (b) Small-signal model.

to $v_{ref}$ and the output of the compensator $i_{fd}^{ref}$ is given to the CC block. Also, a negative gain is added to the forward path to preserve the closed-loop stability. According to Fig. 3, the following relation between $v_{dc}$ and $i_{fd}$ exists.

$$
i_{fd} = G_d(s)(v_{dc} - v_{dc}^{ref}).
$$

(14)

D. PHASE-LOCKED LOOP MODEL

The PLL, shown in Fig. 4(a), is based on tracking the angle of the PCC voltage by regulating $v_{aq}$ to zero as given by

$$
\omega_{vsc} = \omega_{PLL}v_{aq}
$$

(15)

$$
\delta = \omega_{PLL} - \omega_{vsc} = (\omega_g - \omega_{vsc})s^{-1}
$$

(16)

where $\omega_{vsc}$ and $\omega_{PLL}$ are the VSC frequency and phase angle generated by the PLL, respectively; $\omega_g$ and $\omega_{PLL}$ are the grid frequency and the phase angle of the grid voltage, respectively; $\delta$ is the phase angle difference; and $G_{PLL}(s) = K_{p\theta} + K_{i\theta}s^{-1}$ is the PI compensator. The grid voltage $v_g$ can then be decomposed into $dq$ components on the $dq$-RF as

$$
v_{gd} = \hat{v}_g \cos(\delta)
$$

(17)

$$
v_{gq} = \hat{v}_g \sin(\delta)
$$

(18)

where $\hat{v}_g$ is the magnitude of the grid voltage. Substituting for $v_{aq}$ in (15) from (3) and then substituting for $v_{eq}$ from (18) in the result gives the nonlinear dynamics of the PLL as

$$
\omega_{vsc} = s\theta_{vsc} = G_{PLL}(s) (\hat{v}_g \sin(\delta) + (Z_{d}v_{eq} + \omega_{vsc}L_{q,ld})
$$

(19)

where the second term in the right-hand side shows the effect of the grid impedance on the PLL dynamics. If the grid impedance is small, i.e., $Z_d(s) \approx 0$, then $v_{aq} \approx v_{gd} \approx \theta$ and $\delta \approx 0$ in the steady state. If the grid frequency is constant, then (19) can be linearized as

$$
\tilde{\omega}_{vsc} = s\tilde{\theta}_{vsc} = G_{PLL}(s) (\hat{v}_g \cos(\delta)\tilde{\theta}_{vsc} + \Gamma_2(s))
$$

(20)

where $\Gamma_2(s)$ is a linear function showing the effect of the disturbances $\omega_{vsc}, i_{ld},$ and $i_{dq}$, which are yielded from the nonzero grid impedance. Ignoring the disturbances in (20), the small-signal dynamics of the PLL control can be obtained as shown in Fig. 4(b). However, the overall dynamics of the $\tilde{\theta}_{vsc}$ is significantly affected by the grid disturbances under the WG condition.

FIGURE 4. Block diagram of the PLL control loop. (a) Large-signal model. (b) Small-signal model.

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E. INFLUENCE OF THE CONVERTER MODELING ON THE AC VOLTAGE CONTROL

1) ACCURATE MODELING

In grid-connected applications, in addition to injecting the active power to the grid, the VSC is usually responsible for either injecting the reactive power or regulating the PCC voltage magnitude. When connected to the WG, the latter application is more common [9], [24]. Since \( v_{od} \) is regulated to zero by the PLL, the regulation of the PCC voltage is limited to \( v_{od} \). Similar to the CC loop in Part B, an AVC loop is shown in [3] where the feedforward terms are introduced to reject the output current disturbances, i.e., \( i_{od} \) and \( i_{od} \) in (4), and derive the decoupled SISO outer control loops in the dq-RF. However, this method cannot be applied to the VSC-WG system since the DVC block regulates the value of \( v_{od} \). Also, \( v_{od} \) is set to zero by the PLL. Therefore, a different method is adopted here for the AVC, which is originally used to control the PCC voltage in the STATCOM applications [4], as follows. Linearizing (3) results in

\[
\begin{align*}
\begin{bmatrix} \tilde{v}_{od} \\ \tilde{v}_{eq} \end{bmatrix} &= \begin{bmatrix} \tilde{v}_{gd} \\ \tilde{v}_{gq} \end{bmatrix} + Z_g(s) \begin{bmatrix} \tilde{i}_{od} \\ \tilde{i}_{eq} \end{bmatrix} + \omega_{vsc}L_g \begin{bmatrix} -\tilde{\theta}_{od} \\ -\tilde{\theta}_{eq} \end{bmatrix} \\
&\quad + L_g\tilde{\omega}_{vsc} \begin{bmatrix} -\tilde{\omega}_{eq} \\ -\tilde{\omega}_{eq} \end{bmatrix}
\end{align*}
\]  

where \( \tilde{v}_{od} \) and \( \tilde{v}_{eq} \) are obtained by replacing \( \delta \) in (17) and (18) from (16) and linearizing the results; and \( \tilde{\omega}_{vsc} \) and \( \tilde{\theta}_{vsc} \) are given in terms of \( \tilde{\omega}_{vsc} \) by perturbing (15). Moreover, considering the current of the ac filter capacitor \( i_f \) [34], then \( \tilde{i}_{fd} \approx i_{od} \) and \( \tilde{i}_{fd} \approx i_{od} \). After some mathematical manipulations, \( \tilde{v}_{od} \) and \( \tilde{v}_{eq} \) are obtained as functions of \( \tilde{i}_{fd} \) and \( \tilde{i}_{fq} \) from (21) in the following.

\[
\begin{align*}
\tilde{v}_{od} &= \left(G_1(s)G_2^{-1}(s) + 1\right) Z_g(s)\tilde{i}_{fd} + \left(G_1(s)G_2^{-1}(s) - 1\right) \\
&\quad \times \omega_{vsc}L_g\tilde{i}_{fq} \\
\tilde{v}_{eq} &= G_2^{-1}(s)\left(Z_g(s)\tilde{i}_{fd} + \omega_{vsc}L_g\tilde{i}_{eq}\right)
\end{align*}
\]

where

\[
\begin{align*}
G_1(s) &= G_{pl}(s)\left(\tilde{v}_g \sin(\delta)s^{-1} - L_g\tilde{i}_{fq}\right) \\
G_2(s) &= 1 + G_{pl}(s)\left(\tilde{v}_g \cos(\delta)s^{-1} - L_g\tilde{i}_{fd}\right).
\end{align*}
\]

In [4], \( \tilde{i}_{fd} \) is neglected because the VSC injects zero active power to the grid in the STATCOM applications. Therefore, further treatment is needed to include the effect of \( i_{fd} \) in this work. Perturbing (14) and rewriting the equation in terms of \( \tilde{i}_{fd} \) yields

\[
\tilde{v}_{dc} = G_{dc}^{-1}(s)\tilde{i}_{fd}
\]

The AVC is designed to have a much smaller bandwidth compared with the CC loop. Therefore, \( \tilde{i}_{fd} \approx \tilde{i}_{fd} \) in the time scale of the voltage dynamics. Thus, \( \tilde{v}_{dc} \) in (11) can be replaced by its equivalent in (26) as a function of \( \tilde{i}_{fd} \).

\[
\begin{align*}
\begin{bmatrix} \tilde{v}_{od} \\ \tilde{v}_{eq} \end{bmatrix} &= Z_g \begin{bmatrix} \tilde{i}_{fd} \\ \tilde{i}_{fq} \end{bmatrix} + \omega_{vsc}L_g \begin{bmatrix} -\tilde{\omega}_{eq} \\ -\tilde{\omega}_{eq} \end{bmatrix}
\end{align*}
\]

2) APPROXIMATED MODELING

According to (20), \( \tilde{\theta}_{vsc} \) and \( \tilde{\omega}_{vsc} \) are functions of \( \tilde{\omega}_{od} \) and \( \tilde{\omega}_{eq} \). Therefore, their transient excursion can be ignored if \( \tilde{i}_{od} \) and \( \tilde{i}_{eq} \) change with a sufficiently slow rate [4]. This means that \( \tilde{\omega}_{vsc} \approx \tilde{\theta}_{vsc} \approx 0 \) and, since the grid frequency is assumed fixed, \( \tilde{\delta} \approx 0 \). Consequently, \( \tilde{v}_{od} \approx \tilde{v}_{eq} \approx 0 \) according to (17) and (18). This condition holds assuming the AVC and DVC dynamics are considerably slower than the CC dynamics. With these assumptions in place, (21) simplifies into:

\[
\begin{align*}
\begin{bmatrix} \tilde{v}_{od} \\ \tilde{v}_{eq} \end{bmatrix} &= Z_g \begin{bmatrix} \tilde{i}_{fd} \\ \tilde{i}_{fq} \end{bmatrix} + \omega_{vsc}L_g \begin{bmatrix} -\tilde{\omega}_{eq} \\ -\tilde{\omega}_{eq} \end{bmatrix}
\end{align*}
\]

Fig. 5 shows the control block diagram of the PCC voltage, where, \( G_v(s) = K_{pv} + Ki_s s^{-1} \) is the PI compensator employed to regulate \( v_{od} \); and \( u_{cp} \) is a compensating signal that is discussed in Section IV. As shown, a negative gain is added to the forward path to preserve the closed-loop stability. According to Fig. 5, the AVC set the value of \( \tilde{i}_{dq} \) such that

\[
\tilde{i}_{dq} = G_v(s)(\tilde{i}_{od} - v_{od}).
\]
Repeating the same procedure in (22)–(32) results in the following.

\[ \tilde{i}_{fd} = \frac{N_2(s)}{D_2(s)} \tilde{i}_{fq} \]  
\[ T_{iv}^{\infty}(s) = Z_g(s) \frac{N_2(s)}{D_2(s)} - \omega_{vsc} L_g \]

where

\[ N_2(s) \approx -\omega_{vsc} L_g + G_3(s)\tilde{i}_{fq} Z_g(s) - \tilde{i}_{fq} G_3(s)(Z_f(s) + r_f) \]

\[ D_2(s) \approx G_3(s) - Z_g(s)\tilde{i}_{fd}^2 - G_3(s)\omega_{vsc} L_g \tilde{i}_{fd}. \]

It is shown in Section V that using the accurate modeling of the PCC voltage dynamics results in small-signal voltage responses that closely match the large-signal transient responses of PCC voltage at different values of the PLL bandwidth. On the contrary, the small-signal responses yielded from the approximate model, which is widely used in the literature for the AVC design [4], [24], [29], shows a discernable discrepancy between the small- and large-signal transient responses and this difference increases by increasing the PLL bandwidth. Therefore, it is important to obtain an accurate SISO transfer function for the PCC voltage dynamics if the control design optimization is the objective.

F. DESIGN OF THE VSC CONTROLLERS

As suggested by [4], the bandwidth of the CC loop \( T_c(s) \) is 10% to 20% of the converter switching frequency. The AVC and DVC loops are also considerably slower than the current loop. To this end, the corresponding control gains are selected to assign a bandwidth equal to 17% of the switching frequency to the CC loop and bandwidths equal to 14% and 12% of the CC bandwidth to the DVC and AVC loops, respectively. In the latter, the stability of the closed-loop system imposes the maximum permissible degree. The closed-loop bandwidth of the PLL is a trade-off between the filtering characteristics and fast responses [35]. In order to meet a fast tracking and filtering characteristics, the bandwidth of PLL is usually in the range of few tens of Hz [36]. Further, the PLL bandwidth in the grid-connected applications should be smaller than the grid nominal frequency to reject the second and sixth order harmonics [4]. However, it should not be too small so that the PLL tracks fast changes in the PCC voltage following the output power or the grid impedance variations [4].

III. SMALL-SIGNAL STABILITY ASSESSMENT OF THE VSC-WG SYSTEM WITHOUT ACTIVE COMPENSATION

A small-signal model of the VSC-WG system without active compensation (i.e., \( u_{cp} = 0 \) in Fig. 5) is developed in the form of the state-space equations by linearizing (2)–(8), (10), (14)–(16), and (33) about an equilibrium point which corresponds to the operation of the VSC-WG at the nominal condition according to Appendix A. The state-space representation is given by

\[ \frac{d}{dt} \tilde{X}_{uc} = A_{uc} \tilde{X}_{uc} \]

where “\( \sim \)” denotes a small deviation in variables and \( \tilde{X}_{uc} \) is the state vector as given by

\[ \tilde{X}_{uc} = \begin{bmatrix} \tilde{d} & \tilde{v}_{cd} & \tilde{v}_{cq} & \tilde{i}_{fd} & \tilde{i}_{fq} & \tilde{v}_{cd} & \tilde{v}_{cq} & \tilde{i}_{fd} & \tilde{i}_{fq} & \tilde{v}_{cd} \\ \tilde{v}_{cq} & \tilde{v}_{cd} & \tilde{v}_{cd} & \tilde{l}_{et} & \tilde{l}_{eq} & \tilde{v}_{cd} & \tilde{v}_{cq} & \tilde{l}_{et} & \tilde{l}_{eq} & \tilde{v}_{cd} \end{bmatrix}^{T}, \]

and \( A_{uc} \) is the state matrix as given in Appendix B.

A. PARTICIPATION ANALYSIS

The relative participation of different states in the dominant eigenvalues (modes) of the \( A_{uc} \) matrix in (39) is evaluated using the participation factor (PF) measure [37]. The relative PFs of the states are calculated for two cases of connection to a SG at \( SCR = 10 \), and a connection to a VWG at \( SCR = 1 \). The PF results are summarized in Table 1.

As shown, in the case of the SG, there are two real stable eigenvalues, \( \lambda_1 \) and \( \lambda_2 \), which mainly corresponds to the PLL and control states of the PCC voltage, respectively. However, in the case of the WG, there are two real stable eigenvalues, \( \lambda_1 \) and \( \lambda_4 \), which are mainly affected by the states of the PLL and the DVC, respectively. Also, there is a pair of unstable complex eigenvalues, \( \lambda_3 \sim \lambda_4 \), which corresponds to the states of the grid impedance, PLL, DVC, and AVC. This shows that the cross-coupling between the states of the VSC control system and the WG impedance is the primary source of instability in the VSC-WG system. In addition, there is a pair of stable complex eigenvalues, \( \lambda_5 \sim \lambda_6 \), which correspond to the states of the PLL, dc-link, and the grid impedance similar to \( \lambda_3 \sim \lambda_4 \). As will be shown, this pair can induce significant progress toward the imaginary axis following variations in the control.
gains. Therefore, they can be responsible for introducing oscillatory unstable modes to the system dynamics.

**B. SENSITIVITY ANALYSIS**

1) **INFLUENCE OF THE VSC POWER LEVEL**

Fig. 6 shows the location of the dominant eigenvalues of $A_{uc}$ under different values of $P_{ac}$. As shown, by changing $P_{ac}$ from 0.35 to 1 pu, $\lambda_{3-4}$ have considerable progress toward the imaginary axis while $\lambda_1$ does not show any noticeable change and $\lambda_2$ departs slightly from the imaginary axis. Therefore, the stability of the VSC-WG system decreases as the value of $P_{ac}$ increases. Moreover, the VSC-WG system is not stable for $P_{ac} > 0.84$ per-unit (pu.), which corresponds to $SCR < 1.2$.

2) **INFLUENCE OF THE LC FILTER DAMPING**

Fig. 7 shows the trajectory of the dominant eigenvalues when the LC filter damping resistance $r_d$ changes from 0 to 0.6 $\Omega$ under the nominal power condition, i.e., $SCR = 1$. By increasing the passive damping, it is possible to shift $\lambda_{5-6}$ to the stable region. However, $\lambda_{3-4}$ is almost unaffected by the passive damping resistance and hence it is not possible to stabilize the system at the nominal power level. Clearly, the origin of the instability is not the ac filter resonance.

3) **INFLUENCE OF THE PLL CONTROLLER**

The effect of changing the PLL control gains on the dominant eigenvalues is shown in Fig. 8. As shown, $\lambda_3$ and $\lambda_4$ are initially real with positive values. Then, by multiplying $(K_{ppl}, K_{ipl})$ by a gain of 0.28 to 1.23, the eigenvalues relocate slightly from the imaginary axis. Therefore, for a PLL with extremely limited bandwidth, the VSC-WG system can be stable. However, limited bandwidth of PLL hinders the excursion of the frequency during transients [4] which, in turn, slows down the response time of the VSC to the variations in the grid power that are typically fast. This effect is also in agreement with the PF values given in Table 1 where the PF values given in Table 1 for $\delta$ and $\delta_{eq}$ are the states related to PLL. Therefore, there is a trade-off between the VSC-WG system stability and the fast dynamic response.

4) **INFLUENCE OF THE DC-LINK VOLTAGE CONTROLLER**

The effect of changing the DVC gains on the dominant eigenvalues is depicted in Fig. 9. As shown, $\lambda_3$ and $\lambda_4$ are initially real with positive values. Then, by multiplying $(K_{pidc}, K_{idc})$ by a gain of 0.28 to 1.23, the eigenvalues relocate when $(K_{pdc}, K_{idc})$ change by a gain of 1 to 10 under $P_{ac} = 1$ pu condition. Therefore, for a PLL with extremely limited bandwidth, the VSC-WG system can be stable. However, limited bandwidth of PLL hinders the excursion of the frequency during transients [4] which, in turn, slows down the response time of the VSC to the variations in the grid power that are typically fast. This effect is also in agreement with the PF values given in Table 1 for $\lambda_{3-4}$ where $\delta$ and $\delta_{eq}$ are the states related to PLL. Therefore, there is a trade-off between the VSC-WG system stability and the fast dynamic response.

5) **INFLUENCE OF THE AC VOLTAGE CONTROLLER**

The effect of changing the AVC gains on the dominant eigenvalues is depicted in Fig. 10. According to Fig. 10(a), similar to changing DVC gains, $\lambda_3$ and $\lambda_4$ are initially real
values and, by multiplying \((K_{pv}, K_{pu})\) by a gain of 0.08 to 1.05, a relatively large relocation occurs before merging and turning into a complex pair \(\lambda_{3-4}\), yet, still in the unstable region. This observation is also in agreement with the PF values given in Table 1. Further, the bandwidth of the PCC closed-loop system \((\omega_{pcc})\) increases from 0.6 to 6.6 Hz and so \(\lambda_{5-6}\) progress extensively toward the unstable region as shown in Fig. 10(b).

IV. PROPOSED ACTIVE COMPENSATION OF VSC-WG

From Section III, it is concluded that without compromising the PLL closed-loop bandwidth, i.e., having the PLL with slow response time, it is not possible to preserve the stability of the VSC-WG system under the worst-case scenario at \(SCR = 1\). Therefore, a novel method is proposed in this work to stabilize the VSC-WG system under the same conditions and increase the damping of the system responses under lower levels of \(SCR\).

Fig. 5 shows a new feedforward compensation loop (in red) where a compensation signal \(u_{cp}\) is added to the forward path of the PCC closed-loop control system with a negative sign. Based on this augmentation, the equation for the \(q\)-axis component of the current reference can be rewritten as

\[
\tilde{I}_{fq}^{ref} = -G_i(s)(v_{od}^{ref} - v_{od}) - u_{cp}(s) \tag{41}
\]

where

\[
u_{cp}(s) = K_{cp} \frac{\omega_{cp}}{s + \omega_{cp}} v_{oq} \tag{42}
\]

in which, \(K_{cp}\) and \(\omega_{cp}\) are the dc gain and the cut-off frequency of the low-pass filter. In (42), \(v_{oq}\) is used for the active compensation because; first, according to Table 1, \(v_{oq}\) is the input of the PLL which corresponds to the instability of the dominant modes \(\lambda_{3-4}\), second, \(v_{oq}\) is zero in the steady-state stable conditions, therefore, \(u_{cp}\) has a zero influence on the steady-state operation of the VSC.

A. SMALL-SIGNAL MODEL OF THE ACTIVELY COMPENSATED VSC-WG SYSTEM

To represent the small-signal model of the compensated system, (2)–(8), (10), (14)–(16), (41), and (42) are linearized to give the state-space representation as

\[
\frac{d}{dt} \tilde{X}_{cp} = A_{cp} \tilde{X}_{cp} \tag{43}
\]

where the state vector \(\tilde{X}_{cp}\) is given by

\[
\tilde{X}_{cp} = [\tilde{x}_{uc} \ x_{cp}]^T \tag{44}
\]

where, \(x_{cp}\) is the new state variable corresponding to the low-pass filter in (42); and the state matrix \(A_{cp}\) is given in Appendix B.

B. STABILITY ASSESSMENT AND DESIGN

According to (42), there are two degrees of freedom to design the active compensator. Fig. 11 shows the eigenvalue spectrum of \(A_{cp}\) under the nominal conditions when \(K_{cp}\) increases at three different values of the cut-off frequency, \(\omega_{cp} = (15, 20, 25)\) rad/s. As shown, with the different values of \(\omega_{cp}\), the dominant eigenvalues \(\lambda_{3-4}\) migrate from the unstable to the stable region as \(K_{cp}\) increases. Note that \(\lambda_{3-4}\) move back toward the imaginary axis at higher values of \(K_{cp}\). Fig. 11 also shows that with a smaller value of \(\omega_{cp}\), more improvement in the dynamic stability is obtained. As shown in Appendix A, the parameters of the active compensation are designed to provide the maximum enhancement in the stability of the VSC-WG system at \(SCR = 1\).

Fig. 12 shows the location of the dominant eigenvalues of \(A_{cp}\) when \(P_{ac}\) increases from 0.35 to 1 pu. As shown, \(\lambda_{3-4}\) progress toward the imaginary axis while \(\lambda_1\) does not show a visible change whereas \(\lambda_2\) departs slightly away from the imaginary axis. Unlike the uncompensated system in Fig. 6, it is clear that the dominant eigenvalues are in the stable region for \(0.84 < P_{ac} < 1\) pu. The proposed active compensation loop successfully achieves the full integration of the VSC at \(SCR = 1\). Fig. 12 also shows the progress of a pair of complex eigenvalues, denoted by \(\lambda_{cp1-2}\), which corresponds to the active compensation state. As shown, by increasing \(P_{ac}\),
\[ \lambda_{cp1-2} \text{ depart slightly from the imaginary axis which does not compromise the system stability.} \]

V. SIMULATION RESULTS

To validate the developed dynamic models, the small-signal analysis, and the effectiveness of the proposed compensation method, nonlinear time-domain simulations are conducted in MATLAB/Simulink for the system shown in Fig. 1 and the parameters given in Appendix A. The average model of the VSC is used for the purpose of dynamic simulation [4].

A. INFLUENCE OF THE AC VOLTAGE CONTROL

The dynamic response of the PCC voltage corresponding to the VSC-WG system is presented in this section. The small-signal model is based on the closed-loop system in Fig. 5 whereas \( T_{iv}^{ac}(s) \) is evaluated using (32) and (36) as given in Appendix C for the accurate and approximate small-signal models, respectively. Fig. 13 shows the step response of \( v_{od} \) following a 1% step in \( v_{od}^{ref} \) at \( t = 0.5 \) s when \( P_{ac} = 0.84 \) pu with and without the proposed active compensation. As shown in Fig. 13(a), where the PLL is slow with a bandwidth of 3.2 Hz, the approximate model is close to a first-order exponential signal whereas the accurate model shows a second-order underdamped behavior with a noticeable overshoot before reaching the steady state. Moreover, the response of the nonlinear large-signal model is shown which closely matches the response of the accurate small-signal model.

Fig. 13(b) shows the dynamic responses of the models under the same scenario when a faster PLL with a bandwidth of 25 Hz is implemented. As shown, the response of the approximate model is the same as the case of the slow PLL since the effect of PLL is ignored. However, the responses of the accurate and the large-signal models show a poorly damped oscillatory behavior. Further, the responses of the accurate and large-signal models are closely matched which verifies the development of the small-signal model in (21)–(33). It is clear that the approximate model fails to reflect the entire dynamics of the system. On the other hand, the accurate model derived in this work closely follows the large-signal dynamics of the PCC voltage. This allows designing an optimized PCC controller for the VSC-WG systems according to the SISO model in Fig. 5. It is also worth noting that the slow PLL bandwidth of 3.2 Hz is implemented for the sake of evaluation only whereas a fast PLL is adopted in this work.

The capability of the accurate model in reflecting the PCC voltage dynamics is tested for the VSC-WG system with active compensation under the same scenario as the uncompensated model. Fig. 14 shows the response of the accurate small-signal model as compared to the response of the nonlinear large-signal model. As shown, both responses coincide closely. Moreover, the responses exhibit much less oscillatory behavior as compared to the response of the uncompensated model in Fig. 13 because the feedforward compensation is included in the control loop of the PCC voltage.

B. INFLUENCE OF THE ACTIVE POWER LEVEL

The performance of the VSC-WG system under different active power levels is investigated in Fig. 15. A small step change in the active power at \( t = 0.5 \) s under different levels of power is applied. As shown in Figs. 15(a)–(c), for \( P_{ac} \leq 0.6 \) pu, the responses are similar. However, as shown in Fig. 15(d), the uncompensated system is oscillatory as the active power increases. These oscillations are related to the relocation of \( \lambda_{3-4} \) with the change in the power according to Fig. 6. The unstable oscillatory behavior of the uncompensated system is clear at \( P_{ac} = 0.86 \) pu as shown in Fig. 15(e).
Note that the frequency of oscillations in Figs. 15(d)–(e) are 12.8 and 12.7 Hz, respectively, which closely matches the frequency of the corresponding mode $\lambda_{3-4}$ in Fig. 6. More importantly, the compensated system exhibits a stable response under the full range of the active power injection including the worst-case scenario at $SCR = 1$ as shown in Figs. 15(a)–(f).

C. INFLUENCE OF THE GRID ANGLE VARIATION

In this part, another advantage of using the proposed active compensation method is demonstrated. The capability of the compensated VSC-WG system to preserve the stability following a sudden change in the phase angle of the grid voltage $\theta_g$ is investigated. As an extremely challenging condition, Figs. 16(a)–(b) show the responses of $P_{ac}$ and $v_{ac}$ following a step change of 70° while its value relative to the grid angle $\theta_g$ (not shown here) is not changed. The same condition is applied to the uncompensated system. As shown in Figs. 16(a)–(b), the uncompensated system fails to reach a stable operating point. Figs. 17(a)–(b) show the active power and angle responses to a 20° increase in $\theta_g$ between $t = 1$ s and $t = 1.5$ s at $P_{ac} = 1$ pu. As shown, the compensated system stability is preserved under the nominal power condition.

D. INFLUENCE OF THE GRID IMPEDANCE VARIATION

Depending on the flow of power, especially in WGs where DGs are integrated, the grid impedance is not constant and might be subject to uncertainties [21], [39]. Online identification methods are suggested to find the real-time values of impedance for the stability assessment [40]. The stability analysis that is conducted in Part IV-B considers the nominal power which corresponds to the worst-case scenario at $SCR = 1$, where the suggested active compensation in (41) guarantees the system stability. However, according to (1), the $SCR$ level is a function of the VSC nominal dc power and the grid impedance. Therefore, in this part, the operation of the VSC-WG system is tested under the nominal power condition and a wide variation range in the grid impedance $Z_g$.

Figs. 18(a)–(b) show the response of the VSC reactive power $Q_{ac}$ and the magnitude of the phase difference, i.e., $|\delta|$, to the increase in the grid impedance (while the angle of $Z_g$ is fixed). Since the rate of the change in the grid impedance is not $a$ priori knowledge, the simulation is repeated for two periods of 0.3 s and 1 s during which, the grid impedance is changed to assess the effect of the impedance variation on the VSC-WG performance with fast and slow rates, respectively. As shown, the system is initially in the steady-state stable condition at $SCR = 3$, i.e., the WG condition, where the grid impedance $Z_g$ is one-third of the nominal value given in Appendix A. Then, at $t = 0.25$ s, $Z_g$ increases linearly until it reaches the nominal value at $SCR = 1$, i.e., the VWG condition. In the meantime, according to Fig. 18(a), $Q_{ac}$ increases to partially compensate for the reactive power absorbed by the grid reactance. Since the injected active power is fixed at 1 pu, $|\delta|$ increases as the grid reactance increases according to Fig. 18(b). This agrees with the steady-state real power flow equation in inductive lines [37]. Fig. 18 also shows that there are overshoots and undershoots in the responses corresponding to the fast rate of changes in the grid impedance while
they are considerably lessened in the responses of the slow rate of changes. However, the stable operation of the system is maintained during both impedance changes. Therefore, the VSC-WG system with the suggested active compensation method is immune to a wide range of changes in the grid impedance with slow and fast rates.

**E. INTERACTIONS WITH VSC PRIMARY CONTROLLERS**

In this part, the dynamic interactions of the proposed compensation method with the primary controllers of the VSC-WG system are investigated at $P_{ac} = 0.75$ pu by comparing the compensated and uncompensated responses. Fig. 19(a) shows the frequency tracking responses of the PLL subsequent to a 1 Hz step change in the frequency of the grid. It is clear that the active compensation loop has an insignificant effect on the PLL bandwidth. Fig. 19(b) shows the responses of $i_{gd}$ following a 5% step in the active power at $t = 0.5$ s. The proposed active compensation method manages to significantly decrease the overshoots and suppress the oscillations before reaching the steady-state operating point.

Fig 19(c) shows the variations of the PCC voltage magnitude $|v_o|$ following a 5% step change in the voltage reference at $t = 0.5$ s. As shown, the proposed active compensation does not have any noticeable influence on the dynamics of the PCC voltage as compared to the uncompensated system. Generally, the design of the VSC controllers is not compromised by the proposed active compensation method.

**VI. HIL EXPERIMENTAL VERIFICATION**

The feasibility of the proposed compensation method is verified by an FPGA-based HIL platform, as shown in Fig. 20, where the VSC-WG model is emulated with the same specifications as in Appendix A. The circuit model of VSC-WG is developed in the single-FPGA NI-PXIe-7846R real-time simulator with 1 $\mu$s time step which is interfaced to the host computer by StarSim HIL software. Also, the control model is implemented in the double-FPGA NI-PXIe-7868R simulator which is interfaced to the host computer by StarSim RCP software. The connections between NI-PXIe chassis are realized through three I/O interface boxes.

A series of experiments is performed during which the VSC dc power $P_{dc}$ increases according to the profile given by $P_{dc} = [0.4, 0.6, 0.8, 0.9, 0.95, 1]$ pu at $t = [0, 1, 2, 3, 4, 5]$ s, respectively. Fig. 21(a) shows the VSC responses $v_o$, $i_o$, and the dc-link voltage difference from the nominal value $\Delta v_{dc}$. As shown, both $v_o$ and $i_o$ are well-damped and regulated under all conditions. Moreover, since $v_{dc}$ is regulated by the DVC, $\Delta v_{dc}$ is zero in the steady state as shown in the figure. There are small overshoots in the waveform at the beginning of each step that are less than 0.15 pu at the start-up and less than 0.1 pu for the next steps. Fig. 21(b) shows a closer view
of \( v_p \) and \( i_p \) in the steady state. It should be noted that \( v_p \) has a total harmonic distortion of 5% which is in compliance with the IEEE standard 519 [38].

Fig. 22(a) shows the increases in the active power injected by the VSC \( P_{ac} \) subjected to the steps in \( P_{dc} \). There are small overshoots during each step. This regime continues until \( P_{ac} \) reaches the nominal value at \( t > 5 \) s. According to Fig. 22(b), the magnitude of the phase angle difference \( |\delta| \) between the PCC and grid phase voltages increases after each step in \( P_{dc} \). Fig. 22(c) shows the variations of the proposed compensation signal \( u_{cp} \). As shown, the compensation signal is only activated during the transient conditions to mitigate the potential instabilities and has no impact at the steady-state conditions.

VII. CONCLUSION

In this work, the integration of VSCs into the VWG systems has been investigated, and the associated instabilities have been mitigated effectively under the worst-case scenario at \( SCR = 1 \). The proposed compensator injects a modified version of \( v_{ao} \) into the \( q \)-axis reference of the CC. It is shown that the proposed method contributes successfully to the relocation of the unstable modes into more damped locations on the complex plane. In addition to the stabilization of the compensated system under the VWG conditions, the stability of the system under the grid angle deviations has been improved significantly with the proposed compensator. The effectiveness of the proposed compensator has been verified analytically using the small-signal analysis followed by large-signal simulations in MATLAB/SIMULINK and real-time HIL experiments. The proposed compensator has the following features:

1. It is simple and can be easily designed using the linear analysis tools;
2. It does not interact with the steady-state performance of the VSC; and
3. It has a minimal influence on the existing vector control structure and so it can be designed independently. Time-domain simulations and experiments of the VSC-WG system are carried out to verify:

- The superiority of the accurate small-signal modeling derived in this work over the conventional approximate modeling in reflecting the PCC voltage dynamics;
- The stability of the VSC-WG system with the proposed compensation method under VWG condition at \( SCR = 1 \) and its improved damping property at \( SCR > 1 \); and
- The enhanced capability of the VSC-WG system to withstand sudden grid angle deviations and wide range of variations in the grid impedance.

APPENDIX A

Parameters of VSC-WG system are provided in Table 2.

APPENDIX B

The state matrices introduced in the main body of the paper are provided in detail. \( A_{up} = A_{cp}(i,j) \) for \( 1 \leq i,j \leq 13 \) and \( A_{cp} \) is shown at the bottom of the next page. The corresponding parameters are:

- \( \Lambda_1 = r_{fd}^0 + K_p K_{pv} r_{fj}^0 \), \( \Lambda_2 = -v_{fd}^0 + (K_{pc} - r_d) i_{fj}^0 - (L_f \omega_g + K_{pc} K_{pv} r_{fj}^0) i_{fj}^0 \), \( \Lambda_3 = -v_{fj}^0 + (K_{pc} - r_d) i_{fj}^0 + L_f \omega_g i_{fj}^0 \), \( \Lambda_4 = K_{pv} r_{fod} - (r_d + r_p) i_{g}^0 \), \( \Lambda_5 = K_{pc} K_{pv} r_{f} L_f^{-1} + \omega_g - \omega_{f}^0 \), \( \Lambda_6 = \omega_{f}^0 - \omega_g + K_{pv} r_{fj}^0 \), \( \Lambda_7 = -r_d + K_{pc} r_{f} L_f^{-1} - K_{pv} r_{fj}^0 \), \( \Lambda_8 = (\gamma f_i^0)_{dc} - K_{pc} K_{pd} r_{j}^0 \), \( \Lambda_9 = \omega_{vsc} - K_{pv} r_{f} L_f^{-1} - K_{pv} r_{j}^0 \), \( \Lambda_{10} = K_{pv} r_{f} L_f^{-1} - C_f^{-1} \), \( \Lambda_{11} = r_d(L_g^{-1} - K_{pv} r_{fod}) \), \( \Lambda_{12} = L_g^{-1} - K_{pv} r_{fod} \), \( \Lambda_{13} = \omega_{vsc} + K_{pv} r_{vsc} \), \( \sigma = \gamma f_i^0 (C_{dc} v_{dc}^{-1})^{-1} \).
\[ A_{cp} = \begin{bmatrix} 0 & 0 & -K_{pc} & 0 & 0 & 0 & 0 & 0 & K_{pfc,d} & 0 & -K_{pfc,d} & 0 & -K_{pdc} & 0 \\ 0 & 0 & 0 & 0 & 0 & r_c & 0 & -r_c & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -r_c & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -K_{dc} & 0 & 0 & -K_{dc} & 0 & 0 & -1 & 0 & 0 & 0 & K_{pdc} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ v_{ps} & L_{ig} & 0 & K_{ic} \bar{v}_{eq} & 0 & 0 & 0 & -r_c + r_c & \lambda_0 & r_c & \frac{K_{pdc} \bar{v}_{eq}}{L_g} & \frac{1}{L_g} & \frac{K_{pdc} \bar{v}_{eq}}{L_g} & 0 \\ \frac{v_{ps}}{L_g} & 0 & -K_{ic} \bar{v}_{eq} & 0 & 0 & 0 & 0 & -\omega_{ps} \lambda_0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} . \]

**APPENDIX C**

In the PCC accurate modeling \( T_{ivc}(s) = \frac{N_1(s)}{M_{ij}(s)} \), where

\[
N_1(s) = 8.8 \times 10^{-3} s^{10} + 83.3 s^9 + 53.9 \times 10^3 s^8 - 3.9 \times 10^5 s^7 - 8.5 \times 10^{11} s^6 + 7.1 \times 10^{14} s^5 - 2.9 \times 10^{17} s^4 - 5.6 \times 10^{19} s^3 - 5.6 \times 10^{21} s^2 - 2.3 \times 10^{23} s - 1 \times 10^{24};
\]

\[
D_1(s) = s^{10} + 7.5 \times 10^3 s^9 + 2.2 \times 10^7 s^8 + 3.5 \times 10^{10} s^7 + 3.2 \times 10^{13} s^6 + 1.7 \times 10^{16} s^5 + 4.9 \times 10^{18} s^4 + 6.1 \times 10^{20} s^3 + 7 \times 10^{21} s^2 + 3 \times 10^{23} s^1 + 1.8 \times 10^{24}.
\]

In the PCC approximated modeling \( T_{ivc}(s) = \frac{N_2(s)}{M_{ij}(s)} \), where

\[
N_2(s) = -0.05 s^6 - 153.5 s^5 - 2.6 \times 10^5 s^4 - 2.6 \times 10^8 s^3 - 1.2 \times 10^{11} s^2 - 1.3 \times 10^{13} s^1 - 8 \times 10^{14};
\]

\[
D_2(s) = s^6 + 5.9 \times 10^3 s^5 + 1.2 \times 10^7 s^4 + 1.1 \times 10^{10} s^3 + 3.9 \times 10^{12} s^2 + 3.7 \times 10^{14} s^1 + 1.9 \times 10^{16}.
\]

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