Transient liquid phase bonding of silicon and direct bond copper via electroplating of tin-copper interlayers for power device applications

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Abstract

Joining technology of silicon semiconductors devices to direct bond copper (DBC) substrates in high-temperature power electronics packages is of utmost importance today. In this study, Sn–Cu solder was prepared by electroplating on a direct bonded copper (DBC) substrate. The electroplated DBC system thus prepared was TLP bonded with Si chip at 250 °C for 10 min under a vacuum atmosphere. The effect of electrical charge used for plating Sn–Cu solder, void fraction in the joint, Sn–Cu solder composition on the joining characteristics, and shear strength of the Si-DBC system were analyzed. The experimental results showed that the plating thickness increased almost linearly with plating time and electrical charge. A sound Sn–Cu solder plating thickness was obtained at 40 mA cm$^{-2}$, 11 C cm$^{-2}$, 20 min with 20 at% Cu in the deposit. Furthermore, the plated Sn–Cu solder layer transformed to Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>3</sub>Sn after joining at 250 °C for 10 min. The shear bonding strength of the Si/DBC joint increased with Cu content in the Sn–Cu solder until 20 at% in the Sn–Cu interlayer.

1. Introduction

Due to the 4th industrial revolution, electric and autonomous vehicles are in the spotlight. The continuous need for durable, high-performance and cost-effective electronic components to be used therein impose serious issues in microelectronic packaging manufacturers [1]. The bonding methods used in high-temperature power electronics packages employ Ag die attach sintering and low temperature TLP bonding technologies based on low-temperature Sn-based solders. Although Ag powder used for bonding of Si-chips and DBC substrate shows excellent reliability yet it has several drawbacks associated with it. For instance, longer bonding time, application of pressure, high cost of Ag in the international market [2, 3]. The most popular Sn–Ag and Sn–Ag–Cu alloy used in power semiconductor packaging are not reliable for high density and high-temperature power Si semiconductors [4, 5]. Ag-based solders have their limitations of Ag$_3$Sn intermetallic compounds (IMCs) needles at the solder/Cu joints which may lead to crack propagated failure of the entire device [6, 7]. Accordingly, Ag bearing solders are sensitive to high temperature creep deformation, buildup of plastic strain, and severe cracking at the solder/Cu interface [8]. A thick IMC formed at the solder/Cu interface degrades the joint reliability of solder/Cu owing to their high brittleness and tendency to enhance IMCs formation that also results in the brittle failure of the joints [9]. Therefore, such issues require an immediate solution for the mass production of power electronic packages and devices.

To address these challenges, several alternatives are already available in literature. The examples include the use of Ag free solders, such as Sn–Ni, Sn–Cu, Sn–Bi, Sn–Zn, etc which are relatively cheaper, and hence the material cost is not a concern [10–15]. Conductive epoxy pastes are also available as a viable option but unfortunately, it melts and causes outgas defects at elevated temperatures [16]. Similarly, advanced nano-reinforced composite solders are also not suitable for the joining of high power semiconductors at high-temperature [4, 6, 16, 17]. Recent literature shows that low-temperature TLP bonding via Ag free solders is a potential die-attach methodology [2–5]. In TLP bonding, the Sn layer is completely consumed and the final
bonding interface consists of Cu₅Sn₅ IMCs with residual Cu. The process is also relatively easier, with no-pressure or little pressure, shorter bonding time compared to the aforementioned processes. TLP bonding has various advantages over soldering such as rapid densification, lower bonding temperatures, least microstructural coarsening, and reduced void fraction and cost due to the absence of expensive pre-alloyed powders. However, there is an issue of the brittleness of the Sn-based TLP joints due to the IMCs like Cu₅Sn₅, Cu₃Sn, Ni₃Sn₄, Ag₃Sn, etc. Ironically, these troublesome IMCs have higher melting points than the solder matrix, which is beneficial to improve the thermal properties at elevated temperatures [3].

Among binary solders of interest, Sn–Cu seems to be highly promising over Sn–Ni, Sn–Zn, Sn–Bi based solder alloys. Sn–Bi is associated with the presence of the brittle Bi-phase while Sn–Zn has oxidation issues at elevated temperatures [2–4]. Most of these metal matrix composite fillers employ methods like casting, high-energy milling, powder metallurgy, or electrochemical deposition. Each method has its own merits and demerits [2–4, 17–19]. Compared to other methods, electrochemical deposition is a simple and easy process [20], while other methods include high temperature, ambient environments, and time-consuming.

Therefore, in this work, Sn–Cu solder was electroplated for the TLP bonding of Si-DBC system. In electroplating of Sn–Cu solder, the desired composition of Sn–Cu solder was obtained by varying the electrical charge density and plating time. The electroplated Sn–Cu interlayers was used for the TLP bonding of Si-DBC system. Further, the electroplated Sn–Cu solder characteristics such as, thickness, void fraction, morphology, and the joint shear strength of the Si-DBC were evaluated.

## 2. Experimental

### 2.1. Deposit preparation

The electrolytic plating solution for manufacturing the Sn–Cu binary bonding material was prepared from the plating bath shown in table 1. The major bath components CuSO₄·5H₂O, SnCl₂·2H₂O and an additive are shown in table 1. For electro-plating, DBC (Direct Bonded Copper, 99.999%, Sigma Aldrich, USA) was used as the cathode, and the Pt plate was used as the insoluble counter electrode. The DBC and Pt plate were covered with insulating polyimide tapes. The desired plating surface was exposed for plating. The plating cell was fixed to 3 cm. The pH of the plating solution was maintained to 3.8 ± 0.2, and the temperature of the plating bath was maintained at 25–30 °C. For uniform dispersion of metal salts at room temperature, the plating bath was stirred at 300 rpm using a magnetic stirrer. The number of moles of the [Cu²⁺] ions in the bath was around 0.004 mol 1⁻¹. The electroplating current density (J) and plating time (t) were varied. The amount of charge (Q) passed through the electrolyte was also tabulated in table 2.

| S. No. | t (min) | J (mA cm⁻²) | Moles of [Cu²⁺] | Q (C/m²) | Sn (at%) | Cu (at%) |
|-------|---------|-------------|-----------------|----------|----------|----------|
| 1     | 20 min  | Sn: 40      | 0.004/L         | 14.7     | 90       | 10       |
| 2     |         | Cu: 3       |                 | 12.5     | 85       | 15       |
| 3     |         |             |                 | 11.0     | 80       | 20       |
| 4     |         |             |                 | 8.5      | 75       | 25       |

\[
Q = \frac{Z \Delta m \cdot F}{M}
\]

Here, \(Q\) = amount of charge in coulombs, \(\Delta m\) = the amount of mass change, \(Z\) = number of electrons, \(F = 96,500 \text{ C mol}^{-1}\), and \(M\) = average value of the molar mass of the deposited alloy. A direct electric current (DC) electric power supply (EPP-4000, France, Biologic) supplied by Princeton Applied Research Company was used to carry out the plating experiments. The electrodeposition was carried out in potentiostatic mode. The various components in the plating setup were (1) Counter electrode (platinum foil (Pt)), (2) plating bath, (3) DBC substrate, (4) magnetic stirrer, and (5) power supply terminal (to three electrode geometry). The third saturated calomel electrode was used as a reference which was immersed deep in the plating bath (not shown). The deposition potential was around \(-0.65\text{ V}\).
2.2. Bonding specimen preparation

DBC substrate and a commercial Si-chip (Semi-Powerex Co., Korea) metallized with a Ti (0.1 μm)/Ni (0.2 μm)/Ag (1.0 μm) thin-film were selected as bonding specimens. Here, Ti, Ni and Ag were used as adhesion layer, diffusion barrier layer, and wetting layer on the substrates. Sputter coater (108 Auto, Cressington Scientific Instruments, UK) was used to deposit 10–15 nm thick Au film on Ni/Ti layer. The sputtering chamber was set to 0.1 mbar before deposition. The sputtering current and time were 20 mA and 60 s respectively. Au film coating enhanced the wettability of TLP coating on Si-die. After that, the Si-chip with a size of 2 × 2 × 0.3 mm³ was placed on the Sn–Cu plated bonding layer and subjected to high-temperature treatment under vacuum (1.0 × 10⁻⁴ torr) for the Si/Sn–Cu solder/DBC system using a vacuum furnace. The bonding temperature was 250 °C at a heating rate of 10 °C min⁻¹ and a holding time of 10 min. The temperature was measured using a Pyrex glass fiber thermocouple inside the furnace with IR transparent ZnS glass. The schematic diagram of the bonding specimen and the power module is shown in figure 1.

![Figure 1. Bonding specimen fabrication.](image)

![Figure 2. Cross-section SEM images of plated Sn–Cu solder and their bulk EDS compositional analyses at different amount of electrical charge for 20 min (a) 8.5, (b) 11.0, (c) 12.5, (d) 14.7 C cm⁻², and (e) thickness of Sn–Cu solder as a function of charge density. Peak current density = 40 mA cm⁻², [Cu²⁺] = 0.004 mole, plating time 20 min.](image)
2.3. Microstructure, void fraction, and shear strength analysis

For microstructure analysis, the bonded sample of Si/Sn–Cu solder/DBC was cold mounted using an epoxy followed by polishing with different grades of sandpapers (#800, #1200, #2000) and alumina suspension with 0.1 μm. The morphology of the electroplated Sn–Cu solder, thickness, and chemical compositions were examined using a scanning electron microscope (SEM, model JSM-6010PLUS/LA) and EDS (Energy Dispersive Spectrometer, INCA Oxford). The XRD analysis was performed using Brukers D8 Advance x-ray diffractometer at a slow-scanning rate of 1°/min. The void fraction across the joint was analyzed from SEM images using ImageJ Version 1.49 g. The void fraction was determined at 3 different areas of the deposit cross-section by image binarization using a threshold of 0.6. The area of pores and the fraction was determined after proper thresholding procedure. The bonding strength was evaluated by shear test using a shear tester (PTR-1102 Bond Tester, Rhesca, Japan). Shear stress was applied until the complete breakdown of the Si-chip or the Si/Sn–Cu/DBC joint occurred. The bonding pressure was around 4 MPa. The height of the shear tip was set to 10 μm away from the DBC substrate, and the shear rate was 0.7 mm s⁻¹. The shear strength was tested on 10 samples plated at a fixed charge density and the average value was reported for better accuracy.

3. Results and discussion

3.1. Effect of amount of electric charge on Sn–Cu solder deposition

The cross-section SEM images and compositional analyses of Sn–Cu electroplated layers at different charge densities for 20 min are shown in figures 2(a)–(d). The thickness of the plated Sn–Cu solder is shown in figure 2(e). The Sn–Cu thickness continuously increased with electrical charge density. Specifically, thickness increased from 7.2 to 10.4 μm by increasing electrical charge density from 8.5 to 14.7 C cm⁻². Initially, at 8.5 C cm⁻², the thickness of the Sn–Cu layer was very small (≈7.2 μm). Due to a low electrical charge density, an insufficient number of copper ions were reduced and deposited onto the substrate. The plated surfaces were relatively flat at these conditions. The thickness increased linearly with the electrical charge until a charge density of 12.5 C cm⁻². However, the rate of thickness increase was slower at 14.7 C cm⁻² due to the rapid evolution of hydrogen gases at higher charge density per unit area [21–24]. The EDS analysis of the Sn–Cu layers is illustrated in figure 2. The composition of Cu in the Sn–Cu coating was found to decrease with increasing electrical charge density. The Sn/Cu atomic ratio was varied approximately from 75/25, 80/20, 85/15, and 90/10 for electrical charge densities varying from 8.5 C m⁻², 11.0 C m⁻², 12.5 C m⁻², and 14.7 C m⁻², respectively.

The composition of copper in Sn–Cu solder at various charge densities was measured by bulk EDS analysis across the interface as shown in table 2. It was noticed that the copper content gradually decreased with an increase in the charge density. Recently, a similar observation was observed by Sharma et al. while electroplating Sn–Cu solder from a stannate bath [22]. This can be explained due to a large gap in the standard electrode potentials of Cu²⁺ (+0.34 V) and Sn²⁺ (−0.14 V) [22].

3.2. Effect of plating time on Sn–Cu deposition

The cross-section SEM images of Sn–Cu solder plated at different times is shown in figures 3(a)–(d). As expected, the average thickness of the Sn–Cu layer increased with plating time. Initially, the morphology of
Sn–Cu plated for 10 and 20 min was flat and smooth while the coating morphology turned rough when the plating time was 40 min. The increase in the thickness of Sn–Cu coatings with time was plotted in figure 3(e). The plated thickness of Sn–Cu solder increased linearly from 4.7 μm to 16.3 μm when the plating time increased from 10 to 40 min. Specifically, the average thickness of Sn–Cu increased was 4.7 μm for 10 min, 8.4 μm for 20 min, 16.3 μm for 30 min, and 13.5 μm for 40 min. The metal ions will be continuously deposited at their preferred growth sites leading to the accumulation of ions and poor deposition at the further sites [25]. Meanwhile, hydrogen evolution will be prominent at longer durations due to the limited concentration of metal ions near the electrode surface leading to a porous and rough deposits [24, 25].
The maximum room temperature interstitial diffusivity of Cu in Sn is reported to be 1.23 but Cu does not. Therefore, Cu3Sn layer was formed between the Cu6Sn5 layer and the Cu layer by the following reaction:

\[
5\text{Sn} + 6\text{Cu} \rightarrow \text{Cu}_6\text{Sn}_5
\]

According to the binary Cu–Sn phase diagram as shown in figure 5, Sn exists in equilibrium with Cu6Sn5 but Cu does not. Therefore, Cu3Sn layer was formed between the Cu6Sn5 layer and the Cu layer by the following reaction:

\[
\text{Cu}_6\text{Sn}_5 + 9\text{Cu} \rightarrow 5\text{Cu}_6\text{Sn}
\]

The maximum room temperature interstitial diffusivity of Cu in Sn is reported to be 1.23 \( \times 10^{-7} \text{ m}^2 \text{ s}^{-1} \) with an activation energy of 32.8 kJ mol\(^{-1}\). The energy of activation for grain boundary diffusion of Sn in Cu is 75.3 kJ mol\(^{-1}\). In equilibrium, the Cu–Sn system contains several phases. The interdiffusion in the Cu–Sn system is consistent with those of the binary phase diagram. The IMCs like Cu6Sn5 were formed close to the Sn–Cu substrate of the DBC substrate after joining (figure 4). The Cu6Sn5 IMCs were formed in a limited amount due to the higher amount of Sn due to an insufficient amount of Cu in the Sn–10Cu deposit. However, in solder joints prepared with a higher amount of Cu, i.e., Sn–(15–25)Cu (as-deposited state), a large amount of Cu6Sn5 IMCs is noticed. After bonding of the joints at 250 °C for 10 min, in addition to Cu6Sn5, Cu3Sn was also found in all the joints. Besides, all Sn peaks were disappeared because of the reaction of Sn with Cu and transformation of Cu6Sn5 and Cu3Sn according to the following reaction:

\[
5\text{Sn} + 6\text{Cu} \rightarrow \text{Cu}_6\text{Sn}_5
\]

The cross-section SEM images of the Si/Sn–Cu/DBC bonded joint with different Sn–Cu solders are shown in figure 6. The joint prepared with Sn–10Cu (as-deposited state) exhibited mostly Cu and Sn with a small amount of Cu6Sn5 IMC. An intense peak of Cu was obtained due to the strong signal from the Cu substrate of the DBC substrate after joining (figure 4). The Cu6Sn5 IMCs were formed in a limited amount due to the higher amount of Sn due to an insufficient amount of Cu in the Sn–10Cu deposit. However, in solder joints prepared with a higher amount of Cu, i.e., Sn–(15–25)Cu (as-deposited state), a large amount of Cu6Sn5 IMCs is noticed. After bonding of the joints at 250 °C for 10 min, in addition to Cu6Sn5, Cu3Sn was also found in all the joints. Besides, all Sn peaks were disappeared because of the reaction of Sn with Cu and transformation of Cu6Sn5 and Cu3Sn according to the following reaction:

\[
5\text{Sn} + 6\text{Cu} \rightarrow \text{Cu}_6\text{Sn}_5
\]

The joint microstructure of the bonded joint is shown in figures 6(a)–(d). The fine Ni5Si4 layer was on the top and bright areas were Ag3Sn IMCs layer. Two IMCs layers were visible in all the joints irrespective of the Sn–Cu compositions. The Cu6Sn5 IMC had a slight gray contrast relative to Cu6Sn5 IMC due to its smaller Sn content. The void fraction was maximum in joint formed from Sn–10Cu solder. After bonding with the Sn–10Cu interlayer, Sn did not react with Cu during bonding and the Sn-rich phase remains. Besides, large shrinkage voids remained at the joint, adversely affecting the bonding strength. Additionally, the void fraction was decreased with increasing Cu content of the Sn–Cu interlayer used for TLP bonding (figures 6(b)–(d)). When the joint was made with Sn–15Cu solder, four IMC layers were formed, i.e., Ni5Si4 from Si side (with trace amounts of Ag), Ag3Sn, Cu6Sn5 and Cu3Sn. The Ni–Ag–Cu–Sn and Ag–Sn–Cu IMCs were formed in the

3.3. Phases evolution of Si/Sn–Cu/DBC joint

The XRD patterns of the TLP bonded Si/Sn–Cu/DBC joints are shown in figure 4. The joint prepared with Sn–10Cu (as-deposited state) exhibited mostly Cu and Sn with a small amount of Cu6Sn5 IMC. An intense peak of Cu was obtained due to the strong signal from the Cu substrate of the DBC substrate after joining (figure 4). The Cu6Sn5 IMCs were formed in a limited amount due to the higher amount of Sn due to an insufficient amount of Cu in the Sn–10Cu deposit. However, in solder joints prepared with a higher amount of Cu, i.e., Sn–(15–25)Cu (as-deposited state), a large amount of Cu6Sn5 IMCs is noticed. After bonding of the joints at 250 °C for 10 min, in addition to Cu6Sn5, Cu3Sn was also found in all the joints. Besides, all Sn peaks were disappeared because of the reaction of Sn with Cu and transformation of Cu6Sn5 and Cu3Sn according to the following reaction:

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The maximum room temperature interstitial diffusivity of Cu in Sn is reported to be 1.23 \( \times 10^{-7} \text{ m}^2 \text{ s}^{-1} \) with an activation energy of 32.8 kJ mol\(^{-1}\). The energy of activation for grain boundary diffusion of Sn in Cu is 75.3 kJ mol\(^{-1}\). In equilibrium, the Cu–Sn system contains several phases. The interdiffusion in the Cu–Sn system is consistent with those of the binary phase diagram. The IMCs like Cu6Sn5 were formed close to the Cu–DBC layer. Bonding at 250 °C for 10 min led to the formation of the Cu3Sn. Therefore, the key factor in the formation of various phases in plated thin films was the interdiffusion and mixing of the depositing atoms. Initially, at a lower charge density, due to poor cathode coverage, the intermixing of Cu and Sn atoms was weak. A strong peak of Cu was noticed with a small amount of non-equilibrium phases. With an increase in the charge density, the amount and extent of the non-equilibrium phases were enhanced due to sufficient mobility of Cu and Sn atoms to allow the complete atomic rearrangements needed for equilibrium phases. Therefore, the movement of Cu atoms of the DBC to the Sn–Cu solder was predominant and controlling the parameter of Cu6Sn5 formation at room temperature. The Cu6Sn5 is pseudohexagonal in structure and forms without any appreciable change in the Sn structure. Besides, Cu6Sn5 IMCs were nucleated first when the composition was nearest to the lowest eutectic temperature compared to others, e.g., Cu3Sn and Cu10Sn3, and Cu41Sn11.

3.4. Joint microstructure

The cross-section morphology of Si/(10–25)Cu/DBC joint is shown in figures 6(a)–(d). The fine Ni5Si4 layer was on the top and bright areas were Ag3Sn IMCs layer. Two IMCs layers were visible in all the joints irrespective of the Sn–Cu compositions. The Cu6Sn5 IMC had a slight gray contrast relative to Cu6Sn5 IMC due to its smaller Sn content. The void fraction was maximum in joint formed from Sn–10Cu solder. After bonding with the Sn–10Cu interlayer, Sn did not react with Cu during bonding and the Sn-rich phase remains. Besides, large shrinkage voids remained at the joint, adversely affecting the bonding strength. Additionally, the void fraction was decreased with increasing Cu content of the Sn–Cu interlayer used for TLP bonding (figures 6(b)–(d)). When the joint was made with Sn–15Cu solder, four IMC layers were formed, i.e., Ni5Si4 from Si side (with trace amounts of Ag), Ag3Sn, Cu6Sn5 and Cu3Sn. The Ni–Ag–Cu–Sn and Ag–Sn–Cu IMCs were formed in the

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**Figure 6.** Cross-section SEM images of the Si/Sn–Cu/DBC bonded joint with different Sn–Cu solders. (a) Sn–10Cu, (b) Sn–15Cu, (c) Sn–20 Cu, and (d) Sn–25Cu. (e) EDS mapping analysis of various IMCs across the bonded joint using the Sn–15Cu interlayer.
Ni/Ag metallization of Si after reaction with Sn–Cu interlayers and accelerating the void formation, most of which were between the Ag-Sn–Cu and Cu₆Sn₅ IMCs. The compositions of various phases and IMCs across the interface for Sn–15Cu solder obtained from figure 6(e) are given in table 3. Figure 6(e) shows the EDS mapping for the Sn–25Cu solder joint. Here, Ni and Ag coated layers on a Si chip were observed. The various IMCs formed across the Si/Sn–Cu/DBC joint were identified.

### 3.5. Void fraction analysis

The void fraction was calculated and plotted in figure 7. The pore fraction of 2.29% was observed for the Sn–10Cu bonding material. Similarly, pore fractions of 0.48% for Sn–15Cu, 0.14% for Sn–20Cu and 0.01% for Sn–25Cu were noted. The void fraction was highest at a charge density of 12.5 C m⁻² in the Sn–15Cu sample.
which formed after the liquid reaction during bonding. Several studies are available on the formation of various IMCs, such as Cu$_3$Sn and Cu$_6$Sn$_5$ Cu–Sn couple and Ni$_3$Sn$_4$ or (Cu, Ni)$_6$Sn$_5$ IMCs in contact with nickel underlayer. Ni$_3$Sn$_4$ is formed after a solid state reaction of Ni and Sn in the absence of Cu. Cu$_6$Sn$_5$ forms with some Ni as impurity [4–7, 9]. Cu atoms are dominant diffusing species as compared to Sn atoms [30]. Due to a higher diffusivity of Cu over Sn, Cu atoms are diffused towards the Cu$_6$Sn$_5$–Sn keeping Cu$_6$Sn$_5$ to grow towards the Sn. Meanwhile, the Cu atoms could diffuse through the thin Cu$_3$Sn faster as compared to thicker Cu$_6$Sn$_5$ because of the longer diffusion path.

The shrinkage porosity was resulted from isothermal solidification of the solder melt in two phase region which could serve as weaker points for joint cracks. As shown in figure 6, as the Cu content exceeded 15 at%, Sn-rich phase disappeared, thereby reducing the shrinkage voids and defects to 1% or less. The void fractions were reduced further to 0.1% or less for bonded joint with Sn–25Cu interlayer.

3.6. Joint shear strength

The Si–Sn–Cu/DBC joint shear strength was tested for the joints bonded with different Sn–Cu solder interlayers (figure 8(a)). The shear strength was also plotted as a function of plated charge densities used to prepare the Sn–Cu interlayers (figure 8(b)). The shrinkage porosity defects in the Cu$_6$Sn$_5$–Si/Cu$_3$Sn/Cu layer are the major cause of poor joint strength [31, 32]. The bonding strength was increased as Cu the content in the Sn–Cu layer increased a shown in figure 8(a). Specifically, the bonding strength of each Sn–Cu interlayer was 23.32, 29.32, 34.34, and 35.57 MPa for Sn–10Cu, Sn–15Cu, Sn–20Cu, and Sn–25Cu, respectively. The reason for the increase in the bonding strength was attributed to the smaller void fraction in Sn–20Cu and Sn–25Cu interlayers. As shown in figures 8(a), (b), the Sn content in the Sn–Cu interlayers was also increased with the increase in the electrical charge density. The porosity was the main cause of lowering the joint shear strength of Si/Sn–Cu/DBC system. The fracture surface images of the sample with maximum void (Sn–10Cu) after shear tests was also analyzed (figure 9). Various types of IMCs (Cu$_6$Sn$_5$, Cu$_3$Sn) were detected mainly at the solder fracture sites. The black areas were the Si-chip while the grey areas were Ti/Ni layer. Ni$_3$Sn$_4$ was also detected across the fractured joint. Ag was not detected as it was not directly related to the fracture sites. The fracture mechanism was related to the collapse of shrinkage voids between Cu$_3$Sn IMCs and Cu substrate under tension. Therefore, the optimum composition of Sn–(20–25)Cu interlayer can be suggested for a robust bonding joint.

4. Conclusions

Sn–Cu solder was electroplated to bond the Si chip and DBC substrate. The Si chip–DBC system was bonded at 250 °C for 10 min under a vacuum atmosphere. The major conclusions are as follows:

Figure 9. Bonded fracture surface after shear test in Sn–10Cu sample. (a) SEM cross-section image of the Si/Sn–Cu/DBC joint, (b) high-resolution image showing fracture site, and (d) EDS mapping images recorded from (b).
1. The plated thickness of Sn–Cu solder was increased linearly with plating time until due to enhancement in the electroplating reaction with time.

2. The thickness of Sn–Cu solder was increased with electrical charge density while the Cu content decreased. This may be due to a large electrode potential gap between Cu and Sn ions in the electrolyte at higher charge densities. Specifically, thickness was increased from 6.2 to 10.5 μm by increasing electrical charge density from 8.5 to 14.7 C cm⁻².

3. The Sn–Cu solder in as-deposited state exhibited Sn, Cu₆Sn₅, Cu₃Sn, and Cu. The Cu was detected from the DBC substrate. After joining at 250 °C for 10 min, the interdiffusion of Sn and Cu was occurred leading to an increased amount of Cu₆Sn₅ and Cu₃Sn IMCs.

4. The void fraction in the bonding material was decreased with Cu content in Sn–Cu solder plated at a lower electrical charge density. The void fractions were 2.29% and 0.01% for the Sn–10Cu and Sn–25Cu, respectively.

5. The shear bonding strength of the Si/DBC joint was increased with Cu content in the solder, the shear strengths were 23.32 MPa and 35.57 MPa for Sn–10Cu and Sn–25Cu, respectively. The major mechanism of failure of the solder was through the fracture of Cu₆Sn₅ and Cu₃Sn IMCs.

6. It can be concluded that the shrinkage voids can be controlled and hence the life of power devices can be prolonged by optimizing the plating charge density and composition of the Sn–Cu interlayer.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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