Reuse Distance-based Copy-backs of Clean Cache Lines to Lower-level Caches

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Abstract—Cache plays a critical role in reducing the performance gap between CPU and main memory. A modern multi-core CPU generally employs a multi-level hierarchy of caches, through which the most recently and frequently used data are maintained in each core’s local private caches while all cores share the last-level cache (LLC). For inclusive caches, clean cache lines replaced in higher-level caches are not necessarily copied back to lower levels, as the inclusiveness implies their existences in lower levels. For exclusive and non-inclusive caches that are widely utilized by Intel, AMD, and ARM today, either indiscriminately copying all or none of replaced clean cache lines to lower levels raises no violation to exclusiveness and non-inclusiveness definitions.

We have conducted a quantitative study and found that, copying back all or none of clean cache lines to lower-level cache of exclusive caches entails suboptimal performance. The reason is that only a part of cache lines would be reused and others turn to be dead in a long run. This observation motivates us to selectively copy back some clean cache lines to LLC in an architecture of exclusive or non-inclusive caches. We revisit the concept of reuse distance of cache lines. In a nutshell, a clean cache line with a shorter reuse distance is copied back to lower-level cache as it is likely to be re-referenced in the near future, while cache lines with much longer reuse distances would be discarded or sent to memory if they are dirty. We have implemented and evaluated our proposal with non-volatile (STT-MRAM) LLC. Experimental results with gem5 and SPEC CPU 2017 benchmarks show that on average our proposal yields up to 12.8% higher throughput of IPC (instructions per cycle) than the least-recently-used (LRU) replacement policy with copying back all clean cache lines for STT-MRAM LLC.

Index Terms—Multi-level caches, clean cache lines, copy-back

I. INTRODUCTION

Cache is a critical component of CPU. It is employed to reduce the performance gap between CPU and main memory. Modern CPUs generally contain a multi-level hierarchy of caches. Each CPU core has its private local caches that hold the most recently and frequently used data for itself while all cores share a larger last-level cache (LLC) that maintains data with less access recency and frequency. There are three inclusion policies between multi-level caches. For inclusive caches, cache lines in a higher-level cache are surely included in lower levels. In other words, a higher level is a subset of lower level. In stark contrast, there is no intersection between multi-level exclusive caches. Non-inclusive caches do not enforce either aforementioned restriction and a cache line may or may not be found in any level. Non-inclusive and exclusive caches are more preferred by manufacturers such as Intel, AMD, and ARM, because inclusive caches introduce a wastage of space to redundantly keep duplicate copies of the same cache line in multiple levels. [1][2].

Owing to the limited capacity of cache, from time to time, some cache lines have to be selected as victims and replaced to make room for ones that are to be referenced. Although emerging non-volatile memory (NVM) technologies such as STT-MRAM are supposed to provide much denser media for building larger CPU caches in the near future [3][2][4][5], cache replacement is still essential and imperative. An ineffectual replacement policy yet badly impairs performance. Assuming that a cache line would be reused soon but erroneously replaced, the next reference to it causes a cache miss and incurs a penalty of loading data from memory with considerable access time. Multi-level caches help to reduce such penalties as lower levels can accept cache lines evicted from high levels, especially for dirty cache lines with modified data. Mainstream multi-level caches mostly write back a dirty cache line into an immediately lower-level cache upon replacement rather than write it through multi-level caches and main memory.

Writing back dirty cache lines upon replacement is common in all inclusive, exclusive, and non-inclusive caches, but how to handle replaced clean cache lines is not deterministic. One straightforward way is to discard all such clean cache lines, which does not violate the definitions of inclusiveness, exclusiveness, and non-inclusiveness. Nevertheless, some of them may be reused soon, and discarding all is likely to incur cache misses with significant penalties. On the other hand, exclusive caches in some CPUs simply copy back any clean cache line upon replacement to the immediately lower-level cache [6].

Factually, only a part of clean cache lines would be reused soon and other clean cache lines, as well as many dirty cache lines, turn to be unused in a long run (known as dead cache lines [4][7][8]). It is obvious that copying back all clean cache lines or none upon replacement is suboptimal, because the former underutilizes the lower-level cache while the latter may

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1We use ‘copy back’ for clean cache lines instead of ‘write back’ because ‘write back’ is conventionally used in literature to describe asynchronously updating dirty cache lines to lower levels of memory hierarchy. The latter is a contrast to the synchronous write-through strategy.
incurs cache misses. We have done a quantitative study with exclusive caches for proof-of-concept, and found that, with the knowledge of future, selectively copying back cache lines that would be soon reused outperforms either copying all or none.

In the real world, predicting the future is mainly achieved by learning from the history. We have considered an important historical record, i.e., the reuse distance, one that has been used to develop replacement policies, to predict whether a cache line would be reused soon. Cache lines with the longest reuse distances would be victims for replacement, but a clean cache line with a shorter reuse distance can be copied back into lower-level cache for a potential cache hit. To summarize, we make following contributions in this paper.

- We have conducted a quantitative study which indicates that, for exclusive or non-inclusive caches, copying back all clean cache lines or none yields inferior performance than partly copying back ones that would be reused soon.
- We measure the reuse distances of cache lines in the higher-level cache at runtime and predict whether to copy back a clean one into lower-level cache upon replacement.
- We confirm that dead cache lines exist in a larger lower-level cache. They are perfect victims to be replaced for placing copied-back clean cache lines.

We have done evaluation with gem5 simulator [9] by configuring two-level exclusive caches with non-volatile (STT-MRAM) LLC. Experimental results show that our proposal significantly improves performance compared to conventional LRU replacement with copying back all clean cache lines. For example, with SPEC CPU® 2017 benchmarks [10] run over a 1MB STT-MRAM L2 cache, our proposal yields up to 12.8% higher throughput of IPC (instructions per cycle) on average.

The remainder of the paper is as follows. Section II outlines the background and the motivation of this paper, showing why we aim at copy-back prediction. Section III presents our design CBP and its hardware implementation. Section IV talks about the evaluation of our work on STT-MRAM L2 caches. Section V concludes this paper.

II. BACKGROUND AND MOTIVATION
A. Overview of Multi-level Caches

Cache provides data buffering between CPUs and memory. It contains a multi-level hierarchy in modern CPUs. L1 cache is an on-core cache composed of instruction cache (ICache) and data cache (DCache). Lower-level caches hold more data with larger capacity. The LLC, with the largest capacity, is usually shared by multi-cores to main data that are less frequently accessed than ones in each core’s L1 cache.

Multi-level caches can be either inclusive, exclusive, or non-inclusive. The inclusive cache duplicates the cache line of the inner level, which helps coherence flows, but it reduces usable cache capacity. For exclusive caches, it is a benefit for capacity because no duplicate cache line exists between levels [1]. Non-inclusiveness is much more flexible compared to the former two and allows a cache line to stay at any level. As a result, exclusive and non-inclusive caches are striding into mainstream CPUs and gradually substitute inclusive caches as the de facto configuration today [11][12].

No matter what inclusion policies a particular cache hierarchy uses, achieving effective cache utilization is an objective of primary importance. Prior studies [13][14] found that an efficient organization and management of data in the cache may cause many clean cache lines, as well as many dirty lines, to become unused for a long time. They are known as dead cache lines and underutilize the valuable resource provided by the cache, thereby leading to performance degradation.

Because of the limited capacity of caches, replacements are frequently triggered to make room for cache lines that are to be accessed but missed. In a set-associative cache, the least-recently-used (LRU) cache line, such as the aforementioned dead one, is usually the victim to be replaced from the cache set. Cache replacements happening at a higher level entail interactions with its immediate lower level. Upon replacement, clean cache lines differentiate from dirty ones regarding the fact of no change ever performed. For inclusive caches, both clean and dirty cache lines in a higher level are surely existing in lower ones, so there is no need to push them back. As to exclusive and non-inclusive caches, clean cache lines to be replaced from high-level caches can be either discarded at all, or fully copied back into the lower level, as neither violates the definitions of exclusiveness and non-inclusiveness [1][15].

B. A Motivational Study on Copy-backs

We have conducted a study on the impact of copying back all or none of clean cache lines replaced at high levels of a multi-level exclusive or non-inclusive cache hierarchy. Hereafter we would use two-level exclusive caches for illustration unless otherwise stated. Similar observations are obtainable with more levels or non-inclusive caches.

Observation 1: Copying back all replaced clean cache lines into lower-level cache yields higher performance than discarding all of them. We have first done a quantitative experiment with gem5 simulator in order to illustrate the effect of various copy-back policies. We chose four representative benchmarks from the prevalent SPEC CPU® 2017 test suite. The configurations of L1 DCache and L1 ICache were both 8-way set-associative with 32KB capacity. We set a 16-way set-associative L2 cache in 1MB STT-MRAM as the LLC. We applied the classic LRU algorithm for cache replacement. By default, replaced dirty cache lines from L1 cache are filled into L2 cache. As to replaced cache cache lines from L1 cache, we considered one of four following copy-back policies at runtime.

1) Copying back clean cache line lines from both L1 DCache and ICache to L2 cache.
2) Copying back none of clean cache lines from both L1 DCache and L1 ICache.
3) Copying back clean lines of L1 ICache only to L2 cache.
4) Copying back clean lines of L1 DCache only to L2 cache.

Fig. 1 indicates the throughputs (instructions per second, IPC) of four copy-back policies, normalized against a policy
In this section, we would present our design of leveraging the reuse distance to select clean cache lines to be copied back from a high-level cache to a low-level one upon replacement. The reuse distance has been widely used to develop cache history of L1 ICache and DCache and calculated the reuse distance of each cache line. We define the reuse distance of a cache line as the number of misses over all cache lines in the cache between two consecutive accesses to the specified one. For example, the reuse distance of a cache line is five if globally five misses have happened before the next revisit of the cache line. We deem a cache line to be dead if it is with a reuse distance greater than one thousand. In Fig. 3, both L1 ICache and DCache hold a number of dead cache lines, i.e., 16.0% and 36.0%, respectively. Hence, copying back all clean cache lines, with dead ones included, yields inferior performance, because dead cache lines are unlikely to be accessed again but the cost of copying them back and replacing existing ones in L2 cache for space is inevitable. In fact, Fig. 3 shows that copying back all clean cache lines from L1 DCache entails much lower IPC than doing so with clean cache lines from L1 ICache. The two bars of Fig. 3 explain the reason: L1 ICache contains fewer dead cache lines than DCache, since instructions are more frequently reused.

Observation 3: Selectively copying back some clean cache lines from higher level to lower level improves performance.

Let us take a simplified two-level exclusive cache hierarchy in Fig. 2 to do a qualitative analysis. The upper part of Fig. 2 shows the initial state of two levels exclusively holding six cache lines, i.e., \{X, Y\} in L1 and \{A, B, C, D\} in L2. We assume both X and Y are clean and they are successively evicted from L1 cache. Later CPU intends to access Y and B. The lower part of Fig. 2 illustrates three possible situations with regard to copying back both X and Y, copying back neither X nor Y, and selectively copying back Y only. It is evident that selectively copying back Y incurs fewer cache misses and in turn higher performance. The answer to the question on what clean cache lines to be selected for copying back is the core of this paper.

### C. STT-MRAM as LLC

In the last decade, multiple NVM technologies have been investigated. Some NVM technologies, such as STT-MRAM, are promising to substitute SRAM for CPU caching, particularly as the LLC. With higher density than SRAM, STT-MRAM offers a large capacity cache design. Nonetheless, STT-MRAM suffers from longer write latency as well as higher write energy compared to SRAM. The long write latency of STT-MRAM leads to congestions on the request queues of LLC and can even stall CPU cores [5]. The avoidance of copying back clean cache lines that are dead to STT-MRAM LLC shall relieve the congestions for STT-MRAM, thereby improving the performance of STT-MRAM LLC.

### III. DESIGN AND IMPLEMENTATION

#### A. Design Decisions

In this section, we would present our design of leveraging the reuse distance to select clean cache lines to be copied back from a high-level cache to a low-level one upon replacement. The reuse distance has been widely used to develop cache replacement policies. We find that the reuse distance is an appropriate indicator that foresees future access to a cache line. In the current high-level cache, cache line with much...
longer reuse distances are victims for replacement, but not all of them have a very long reuse distance and would not be re-accessed in the near future. Therefore, we embed our copy-back selection scheme in the replacement process and set a threshold to filter out cache lines that are likely to be re-referenced from ones that shall be discarded.

As mentioned, dead cache lines exist in all levels of a cache hierarchy. Clean cache lines predicted to be reused soon can replace dead cache lines in the lower level. This may cause write-backs to main memory, but the gain in reducing future cache misses through selectively copying back cache lines offsets such penalties. There are research works utilizing the program counter (PC) to find out dead cache lines mainly for LLC [13][15][14][17]. Researchers also proposed PC-based replacement policies [18][19]. However, the involvement of PC in deciding whether to evict a cache line or declare the death of it is unfavorable in practice, because a pipe forwarding the PC from CPU’s front end to the memory hierarchy is hard to be designed, implemented, and verified. As a result, we have considered integrating a non-PC-based replacement policy with the copy-back prediction for both high performance and verifiable hardware expenses.

B. Design of CBP

Overview: A state-of-the-art study [20] on cache behaviors using the reinforcement learning reveals that characteristics of a cache line, such as its data type (prefetched or loaded on cache miss), access frequency, and reuse distance, are essentially contributive to performance. This inspires us of developing a copy-back predictor (CBP) based on these characteristics, especially on the reuse distance. During the replacement process, our CBP closely collaborates with the replacement policy to determine what cache lines to be replaced as victims and what victims shall be copied back. We assign different cache lines with different priorities. In particular, three types of cache lines have a higher priority to be replaced: one with longer reuse distance, one with lower hit frequency and one containing prefetched data. For a clean cache line with a priority exceeding a predefined threshold, it is not copied back to the immediate lower-level cache.

Private and Shared Reuse Distances: We maintain two types of reuse distances for CBP. One is a private reuse distance for each valid cache line, initialized as zero when the cache line is loaded into the high-level cache. We use $rd$ to denote it. $rd$ is incremented by one every time a cache miss occurs to any arbitrary cache line, and reset to be zero once a cache hit happens to the cache line. $RD$ stands for the other reuse distance, an average reuse distance for all valid cache lines in a cache set over time. In implementation, we use 4-bit saturating counter for both $rd$ and $RD$ (0 to 15). Algorithm 1 shows how to compute the priority of each cache line upon a replacement request among a cache set (Line 2 to Line 15). At the very beginning, each one has a priority of zero (Line 3). A prefetched cache line, or a cache line with a higher hit frequency, would have its priority incremented by one, respectively. Next, the comparison between private $rd$ and the average $RD$ may give credit to the cache line (Line 10 to Line 14). More important, a greater $rd$ would entitle more credits (Line 11 and Line 13) as the cache line has not been accessed for a longer time. We note that, due to the importance of reuse distance, the weight assigned to it is much higher than the other two factors.

Then, a cache line with the highest priority is the victim

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**Algorithm 1** Calculation of $rd$ and $RD$

1: procedure **CALCULATE Rd**
2: if it is a cache miss then
3: for each valid cache line $cl$ in the set do
4:  $cl.rd ← cl.rd + 1$
5: end for
6: else
7:  $RDsum ← RDsum + hit_{cl.rd}$
8:  $hit_{cl.rd} ← 0$
9:  $RDcounter ← RDcounter + 1$
10: if $RDcounter = 8$ then
11:  $RD ← RDsum / 8$
12:  $RDsum ← 0$
13:  $RDcounter ← 0$
14: end if
15: end if
16: end procedure
Algorithm 2 The replacement with CBP in a cache set

1: procedure CBP
2: for each valid cache line cl in the set do
3:   cl.priority ← 0
4: if IsPrefecthed(cl) = True then
5:   cl.priority ← cl.priority + 1
6: end if
7: if HitCounter(cl) ≤ 1 then
8:   cl.priority ← cl.priority + 1
9: end if
10: if 2 × RD ≤ cl.rd ≤ 3 × RD then
11:   cl.priority ← cl.priority + 4
12: else if 3 × RD < cl.rd then
13:   cl.priority ← cl.priority + 8
14: end if
15: end for
16: victims ← findHighestPriorityCL()
17: if victims.priority < 9 or IsDirty(victims) = True then
18:   copyback(victims)
19: end if
20: evict(victims)
21: end procedure

Fig. 4. A comparison on IPC between LRU and CBP

C. Hardware Cost

For our proposal, we have added 7 bits (rd) for each cache line and a dozen of bits (RD, counter, etc.) per cache set. The common size of a cache line is 64B in modern commercial CPUs. By calculation, the additional storage costs about 1.3% of the total area. More important, the PC is not taken into consideration in our design, so the area cost as well as the design and verification expenses are insignificant.

IV. EVALUATION

A. Methodology

We implemented and evaluated the proposed replacement policy with CBP in the gem5 simulator on the aforementioned two-level exclusive cache hierarchy. Table I shows the detailed configuration of the CPU we simulated. We applied our proposed replacement policy with CBP onto the L1 DCache. In particular, we experimented with STT-MRAM as the shared L2 cache (LLC). We selected nine workloads from the SPEC CPU® 2017 benchmark suite, because these benchmarks have high MPKI and are sensitive to varying cache organizations.

The main metric to measure performance is the instructions per cycle (IPC). IPC reveals the efficiency and fluency of program execution. A higher IPC means a higher throughput. We compared our proposal (denoted as CBP) to the classic LRU replacement policy with copying back all clean cache lines (denoted as LRU). For a clear illustration, all results of CBP are normalized against ones obtained with LRU unless otherwise stated.

B. Performance Evaluation

We ran both CBP and LRU on STT-MRAM L2 cache to investigate their effects. Fig. 5 shows the IPC improvement of CBP against LRU. It is evident that CBP significantly outperforms LRU with generally much higher IPC. For example, with 521.wrf_r, CBP yields as much as 12.8% more IPC than LRU. On average, the improvement of IPC achieved by CBP is 2.5% compared to LRU over all nine benchmarks. In addition, Fig. 6 shows the miss rate reduction of L1 DCache with both CBP and LRU. We can obtain a similar observation between Fig. 5 and Fig. 6 and the miss rate is dramatically reduced by CBP. These results state that the idea of CBP, i.e., leveraging the reuse distance and other factors to filter out clean cache lines that are going to be re-accessed and put them into L2 cache, is effectual.

We have recorded the numbers of copy-backs of both CBP and LRU after running each benchmark. Table II presents them. We note that LRU copies back all while CBP selectively copies back some cache lines in accordance with Algorithm 2. A joint investigation of Table II and Fig. 4 tells that fewer copy-backs lead to higher throughput. On average, CBP copies back 2.9% fewer cache lines than LRU. For 521.wrf_r, the reduction between CBP and LRU is 14.6%. Selectively copying back some clean cache lines, rather than all of them like LRU,
avoids keeping dead cache lines in lower-level cache, thereby improving the cache utilization.

In addition, from Fig. 4 we can find that, on the benchmark 548.exchange2_r, CBP is inferior compared to LRU. The numbers of copy-backs of CBP and LRU for this benchmark in Table II explain the reason. Compared to other benchmarks that would cause millions of or even tens of millions of copy-backs, both CBP and LRU only did with about 5,800 cache lines, which is less in multiple orders of magnitude. Such insignificant copy-backs hinder CBP from outperforming LRU.

V. CONCLUSION

Exclusive and non-inclusive caches are becoming the mainstream configurations for a multi-level cache hierarchy in commercial CPUs. On the other hand, NVM technologies such as STT-MRAM are promising candidates to be used as LLC. To make the most of multi-level caches, we have studied the problem of efficiently handling clean cache lines replaced from higher-level caches. By leveraging the reuse distance and other factors, we have proposed a new replacement policy with a selective copy-back scheme for clean cache lines. Experimental results confirm that our proposal is able to substantially outperform the state-of-the-art with up to 12.8% higher throughput.

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TABLE II
A COMPARISON ON THE COPY-BACKS BETWEEN CBP AND LRU

| # of copy-backs for L1 DCache | 507.cactuBSSN_r | 521.wrf_s | 538.imagick_r | 548.exchange2_r | 557.xz_r | 600.perbench_s | 620.gcc_s | 623.xalancbmk_s | 631.deepjeng_s |
|-----------------------------|----------------|----------|---------------|----------------|---------|----------------|---------|----------------|--------------|
| LRU                         | 16,023,511     | 6,032,447| 328,764       | 5,833          | 2,050,938| 1,980,125      | 2,051,612| 2,052,208      | 1,945,706    |
| CBP                         | 14,646,325     | 5,261,716| 329,265       | 5,832          | 2,051,812| 1,945,708      | 2,052,208| 1,945,708      | 1,945,706    |

Fig. 5. The reduction of miss rate by CBP over LRU.

No. of copy-backs

CBP and LRU