Microsecond Pulse I–V Approach to Understanding Defects in High Mobility Bi-layer Oxide Semiconductor Transistor

Hyunsuk Woo & Sanghun Jeon

The carrier transport and device instability of amorphous oxide semiconductor devices are influenced by defects that are exponentially distributed in energy, because of amorphous phase channels and front/back interfaces with a large number of sub-gap states. Thus, understanding defects and charge trapping in oxide semiconductor transistors is required for being core device element in reliable production lines. In this paper, we present the transient charging effect, the charge trapping mechanism, and the dynamic charge transport of high-mobility bilayer oxide semiconductor transistors. To this end, we exploited microsecond ramps, pulse ID–VG, transient current, and discharge current analysis methods. The mobility enhancement rate of single HfInZnO (HIZO) and bilayer HfInZnO-InZnO (HIZO-IZO) were 173.8 and 28.8%, respectively, in the charge-trapping-free environment. Transient charge trapping can be classified to temperature insensitive fast charging and thermally activated slow charging with two different trap energies. Insignificant fast transient charging of a bilayer-oxide high-mobility thin film transistor (TFT) can be explained by the low density of sub-gap states in the oxide semiconductor. Understanding defects and transient charging in the oxide semiconductor helps to determine the origin of device instability of oxide TFTs, and finally, to solve this problem.
mobility in an environment with minimal charge trapping42–46. To this end, we employed microsecond fast ramp
I–V (μs-FIV), pulse I–V (PIV), the transient current method, and discharge current analysis (DCA). The μs-FIV
and PIV methods permit relatively fast sweeping and measurement times on the order of μs, unlike the conven-
tional DC I–V method47–54. Thus, because we employ μs-FIV measurement, the charge trapping phenomena
induced by the defects can be minimized during measurement, enabling us to extract near-intrinsic transistor
parameters. In addition, we extracted the sub-gap states of amorphous oxide TFTs with quantified parameters
using the DCA method, which is a modified charge pumping method55, 56. In the DCA measurement method, we
applied a periodic pulse to the gate at a controlled frequency and measured the discharge current, thereby extract-
ing the sub-gap states that are exponentially distributed in energy in the oxide TFT57–59. DCA result shows that
the bilayer HIZO-IZO oxide TFT has lower sub-gap states in the oxide TFT, then in the single-layer HIZO oxide
TFT. We also discuss the model of charging phenomena of single-layer HIZO and bilayer HIZO-IZO oxide TFTs
using the transient current measurement method with varying temperature56, 51, 52. We observed fast and slow
charge-trapping phenomena for both devices and provide a possible model following temperature-insensitive fast
charging and thermally activated slow charging at two different trap energies. The various pulsed I–V techniques
described in this paper are expected to help accurately extract the sub-gap density of states and the transistor
parameters, and improve understanding of the impact of charging on oxide TFTs.

Results

As seen in Fig. 1(a), the cross-sectional high-resolution scanning transmission electron microscopy image shows
the Mo bottom gate TFT with a top-contact Mo source/drain and passivation layer structure. An inverted stag-
ered bottom-gate oxide TFTs were fabricated using a standard semiconductor fabrication process technology.
For all of the electrode, Mo electrode was deposited by radio frequency (RF) sputtering using O₂/Ar gas and
subsequently growing a gate insulator of SiO₂ by the plasma-enhanced chemical vapor deposition (PECVD).
As an active channel, four different type of semiconductor layer configurations, such as HIZO (40 nm), HIZO
(20 nm)-IZO (20 nm), HIZO (20 nm)-IZO (40 nm) and IZO (60 nm) channel, were employed. Each active
channel was deposited at room temperature by RF magnetron sputtering method. Subsequently, source/drain
electrodes were sputtered at room temperature, followed by patterning process. Then PECVD SiO₂, passivation
layer was formed and contact hole was patterned. The detail of fabrication can be found in the Methods (Device
Fabrication). The transmission electron diffraction pattern images of the bilayer semiconductors, top IZO, and
bottom HIZO, in the right part of Fig. 1(a), show tiny dots and characteristics lines in the hazy background
image, implying that both semiconductor layers are composed of the nano-crystalline phase in an amorphous
medium4. The energy dispersive spectroscopy data in Fig. 1(b) verifies that top and bottom layers are made of IZO
and HIZO, respectively. For composition analysis, the concentrations of Hf, In, and Zn were determined from
different HIZO and IZO samples using inductively coupled plasma atomic emission spectrometry (ICP-AES) on
a Shimadzu ICPS-8100 sequential spectrometer. We found that for IZO, Zn/(In + Zn) and In/(In + Zn) are 0.51
and 0.49, respectively. For HIZO, Zn/(Hf + In + Zn), In/(Hf + In + Zn), and Hf/(Hf + In + Zn) are 0.4, 0.53, and
0.07. For electrical analysis on both samples, the Hall mobility and carrier concentration of HIZO and IZO were
determined using Hall effect measurement (HIZO: μ: 17.2 cm²/V·s, n_{minor}: 2.71 × 10^{15} cm⁻³ and IZO: μ: 48.4 cm²/
V·s, n_{minor}: 9.93 × 10^{18} cm⁻³), as shown in Fig. 1(c). In our study, the front HIZO semiconductor layer adjusts the
threshold voltage and the back IZO semiconductor layer was designed as a high-mobility channel56, 60, 61. A sche-
matic of the bilayer oxide TFT is presented in Fig. 2(a). For μs-FIV, PIV, and DCA measurements, we designed
the device such that it minimized the overlap capacitances among the gate, source, and drain. Thus, all electrodes
were patterned using conventional lithography and dry etching methods. A schematic of the μs-FIV/PIV mea-
surement is shown in Fig. 2(b). For fast-pulse electrical testing, we used the waveform generator/fast measurement
unit (WGFMU) module in the B1500A semiconductor parameter analyzer. For the DC I–V measurements, the
voltage sweep rate was 1 V/s; for μs-FIV and PIV measurements, a single pulse (rise time and fall time 10μs, pulse
width 2 ms) was used. DCA was performed using a high-speed pulse generator (Agilent 81104 A) and a source
meter (Keithley 2401) to obtain the quantitative parameters of the number of sub-gap states in the oxide TFT.

Figure 2(c) shows a typical DC I–V curve of four TFTs with active layers of HIZO (40 nm), HIZO (20 nm)-IZO
(20 nm), HIZO (20 nm)-IZO (40 nm) and IZO (60 nm). When a relatively thick IZO layer is used, the drain
current level is increased because of both the high carrier concentration and the high mobility of IZO as the IZO thickness increases\(^6\),\(^7\). The DC \(I-V\) measurement method has a relatively long sweep/measurement time, and thus, the tested device experiences significant electrical stresses, thereby leading to significant charge trapping, mobility degradation, and device instability\(^4\). Therefore, we employed a fast \(I-V\) measurement method to minimize the fast trapping effect, thereby improving drain current and mobility. Properties were measured at a relatively rapid rise rate of several microseconds, as compared to conventional DC \(I-V\). As shown in the inset in Fig. 2(c), the fast \(I-V\) measurement technique for the HIZO TFT compensates for the fast trapping effects, showing a higher drain current than the DC technique. Figure 2(d) shows the mobility versus voltage ramping time (i.e., 10\(\mu\)s, 100\(\mu\)s, 300\(\mu\)s, and 500\(\mu\)s). As expected, with shorter voltage ramping times, there is higher drain current because of minor charge trapping. Charge trapping depends on gate voltage ramping time. Slow voltage ramping results in high charge trapping. Such a microsecond short sweeping and measurement time can avoid and minimize some channel carriers to be trapped in the shallow-level defects placed in the semiconductor with a certain level of sub-gap states also gate insulator film or at the interface. Therefore, a fast \(I-V\) measurement method has been employed to minimize the effect of fast charging, leading to evaluate the near-intrinsic mobility. Various mobility values of the four devices are presented. Results show that the highest mobility was achieved with bilayer HIZO-IZO devices with relatively thick IZO layers. In addition, the mobility increase rates (\(\mu_{\text{fast}}/\mu_{\text{DC}}\)) for HIZO (40 nm), HIZO (20 nm)-IZO (20 nm), HIZO (20 nm)-IZO (40 nm) and IZO (60 nm) TFTs were 173.8%, 38.5%, 28.8% and 23.8% respectively, indicating that bilayer devices with relatively thick IZO layers have fewer defects. As will be discussed below in detail, this phenomenon occurs because HIZO has a relatively large number

| Active Channel | S.S. (V/dec) | Hysteresis (V) | \(\mu_{\text{DC}}\) (cm\(^2\)/V\(\cdot\)s) | \(\mu_{\text{Fast}}\) (cm\(^2\)/V\(\cdot\)s) |
|----------------|--------------|----------------|--------------------------------|--------------------------------|
| HIZO (40 nm)   | 0.43         | 1.01           | 6.68                         | 18.29                        |
| HIZO (20 nm)-IZO (20 nm) | 0.14     | 0.38           | 30.86                        | 40.75                        |
| HIZO (20 nm)-IZO (40 nm) | 0.12     | 0.10           | 38.25                        | 49.57                        |
| IZO (60 nm)    | 0.10         | 0.07           | 42.26                        | 52.32                        |

Figure 2. (a) Basic schematics of bilayer oxide TFT with bottom gate, top contact, and passivation layer. (b) schematic of \(\mu\)-FIV/PIV system setup. (c) DC \(I-V\) characteristics of various oxide TFTs. Inset shows representative fast \(I-V\) and DC \(I-V\) data for HIZO TFT. (d) Extracted mobility versus voltage ramping time for various oxide TFTs. (e) Sub-threshold slope, hysteresis, and mobility extracted from DC \(I-V\) and fast \(I-V\) measurement methods for four different active oxide semiconductor transistors.
of acceptor-like sub-gap states, causing charge trapping and device instability. To further analyze the transient charging effect, we performed single-pulse $I-V$ measurements. The voltage ramping profile for this measurement is shown in Fig. 3(a). In the single-pulse $I-V$ measurement setup, we started to apply a relatively negative bias to the gate. During this stage, residual charges, which might be trapped in defects, are discharged. In the first stage, we ramp the gate voltage from 0 V to the transistor turn-on voltage during a rise time of 10 $\mu$s and simultaneously measure the drain current. In the second step, the transistor is turned on and some of the majority channel carriers might be trapped in the defects, causing a shift of the threshold voltage toward the positive gate bias direction and reducing the drain current level, because we applied the pulse for 2 ms and the drain current was gradually reduced during this time because of charge trapping. In the third phase of single-pulse measurement, we ramped down the gate voltage from the transistor turn-on voltage to 0 V during a fall time of 10 $\mu$s while measuring the drain current. For the three steps, the measured drain current versus gate voltage plots for four devices during rising and falling times ($T_R$ and $T_F$, respectively) are presented in the left part of Fig. 3(b). During single-pulse measurement (composed of three phases), the transient drain current versus pulse time for four devices was measured; results are plotted in the right part of Fig. 3(b). When we performed single-pulse measurement at various voltage rising times (i.e., 1 $\mu$s, 10 $\mu$s, 100 $\mu$s, 300 $\mu$s, and 500 $\mu$s), the transient drain current during the pulse time gradually becomes saturated after 0.5 ms, as seen in Fig. 3(c–f), following typical charge trapping behavior. The reduction of drain current during the pulse indicates charge trapping, and that transient charging behavior is significant for a single-layer HIZO TFT, but less so for a bilayer oxide TFT with relatively thin IZO, and insignificant for bilayer oxide TFT with relatively thick IZO, which is consistent with the result presented in Fig. 2. Transient charging behavior for four devices match the three-trap model with three trap time constants, as given by Eq. (1).
The above equation gives the number of events. The trapping time constants for the four oxide TFT devices are shown in Fig. 3(g). A short capture time constant (τ_A) and a long capture time constant (τ_B and τ_C) were extracted from Fig. 3(c–f) by applying the above equation. This result reveals that with quantified constants, charge trapping phenomena during charge transport through the channel are significantly affected by the active structure. Generally, carrier transport and charge trapping are thought to occur mainly between the channel and the insulator, or injected into the insulator from the channel. However, in this study, we found that the effect of the IZO back channel is pronounced in TFTs with the same front channel (HIZO) and the same front interface (SiO₂-HIZO). Because the back channel IZO layer has high mobility and high carrier concentration, this layer is attributed to the main charge transport layer in the HIZO-IZO stacked oxide TFTs. When charge transport occurs via an IZO layer with relatively low sub-gap states, charge trapping phenomena occur less often.

To extract the sub-gap states of the oxide TFT of four different channel structures, we exploited a DCA method modified by the charge pumping method. Figure 4(a) shows the measurement diagram of the DCA method. The pulse generator (Agilent 81104 A) and the source meter (Keithley 2401) were controlled using the Lab-view program. We applied a periodic voltage pulse to the gate while the end nodes of source and drain were grounded, enabling us to modulate the carrier concentration. Figure 4(b) shows the gate pulse shape and corresponding discharge current versus the measurement frequency. When we ramp up the gate voltage, the interface and the bulk channel (with and without sub-gap states) are charged. Upon ramping down the gate voltage, the majority carriers in the channel are quickly discharged via source and drain. Thereafter, charges trapped in the interface and the channel with sub-gap states are slowly discharged. At a certain read time, we measured this discharge current at the drain using the source meter. Therefore, the tail part of the discharge current, δI, is related to the carriers discharged from the interface and the bulk channel with sub-gap states. The details of the measurement method and related physics are found in previous work. As we measure the discharge current as a function of measurement frequency for the oxide TFT Fig. 4(b and c), the discharge current level varies with measurement frequency. At measurement frequency changes from 10 kHz to 1 MHz (from the 1st to the 3rd step), the discharge current linearly increases. Then, above 1 MHz, the value becomes saturated. For extracting the number of defects,
we measured the discharge current of the device at a measurement frequency of 100–500 kHz. The number of charging sites is extracted from the slope, \( \delta I / \delta f \), using Eq. (2),

\[
N_{\text{Defect sites}} \left[ \# / \text{cm}^2 \right] = \frac{2}{k} \cdot \frac{\delta I / \delta f \left[ \text{V} / \text{s} \right]}{V \cdot q \left[ \text{cm}^2 \cdot \text{C} \right]} \cdot \left( C / t \right)
\]

(2)

where \( N_{\text{Defect sites}} \) is the density of defects (sub-gap states), \( k \) is the charge loss factor, and \( V \) is the active volume. Additionally, we measure the measurement-frequency-dependent discharge current as a function of gate pulse amplitude \((V_{G,\text{amp}} = V_G - V_{FB})\). As shown in Fig. 4(d–g), the discharge current and the slope, \( \delta I / \delta f \), of the single-layer HIZO TFT is sharp, but is relatively lower for the bilayer oxide TFT with increasing IZO thickness. As shown in Fig. 4(h–i), from the slope, \( \delta I / \delta f \), of the oxide TFTs, the density of the sub-gap states was extracted.

The energy distribution of \( N_{\text{Defect sites}} \left[ N_{\text{Defect sites}} \left( E \right) \right] \) is obtained by calculating the surface potential \( \phi_s \) (or \( E \)) as a function of \( V_G \) using Eq. (3).

\[
\phi_s(V_G) = \int_{V_F}^{V_G} \left( 1 - \frac{C_G(V_G)}{C_i} \right) dV_G
\]

(3)

Figure 4(i) presents the sub-gap density profile of exponentially distributed in energy. The density of the sub-gap states in the four oxide devices, namely, HIZO (40 nm), HIZO (20 nm)-IZO (20 nm), HIZO (20 nm)-IZO (40 nm) and IZO (60 nm) TFTs are 1.2 \( \times \) 10^{18}, 3.7 \( \times \) 10^{17}, 1.6 \( \times \) 10^{17}, 8.6 \( \times \) 10^{17}/cm^2, respectively. Table 1 summarizes the parameters of the sub-gap density profile from the model \( g(E) = N_{DA} \cdot \exp((E - E_C)/kT_{DA}) + N_{TA} \cdot \exp((E - E_C)/kT_{TA}) \), where \( N_{DA} \) is the acceptor-like deep state density, \( kT_{DA} \) is the acceptor-like deep state characteristic energy, \( N_{TA} \) is the acceptor-like tail state density, and \( kT_{TA} \) is the acceptor-like tail state characteristic energy.

| Active channel                  | \( N_{\text{TA}} \) (cm^{-2} eV^{-1}) | \( kT_{TA} \) (eV) | \( N_{\text{DA}} \) (cm^{-2} eV^{-1}) | \( kT_{DA} \) (eV) |
|-------------------------------|--------------------------------------|-------------------|--------------------------------------|-------------------|
| HIZO (40 nm)                   | 6.1 \( \times \) 10^{14}             | 0.09              | 7.4 \( \times \) 10^{17}             | 0.5               |
| HIZO (20 nm)-IZO (20 nm)       | 2.3 \( \times \) 10^{14}             | 0.11              | 3.5 \( \times \) 10^{17}             | 0.6               |
| HIZO (20 nm)-IZO (40 nm)       | 1.2 \( \times \) 10^{14}             | 0.12              | 1.1 \( \times \) 10^{17}             | 0.6               |
| IZO (60 nm)                    | 8.5 \( \times \) 10^{17}             | 0.14              | 1.0 \( \times \) 10^{17}             | 0.6               |

Table 1. Parameters of sub-gap density of states extracted using the discharging current analysis method.

To further understand the transient charge trapping phenomena, the transient drain current versus pulse time plots for representative single-layer HIZO and bilayer HIZO-IZO TFTs were measured with different measurement temperatures, as shown in Fig. 5. We used the model of G. Bersuker in which the existing sub-gap states are filled via two processes, as shown in Fig. 5(a). As we apply a positive gate voltage, electrons drifting toward the front active channel are charged or trapped by acceptor-like sub-gap states. This step is called the charging process, which is a dominant process in the fast-transient charge trapping mechanism. Then, when electrons have sufficient thermal energy, the charged or trapped electrons are activated to overcome the barrier, then move via the trap (process \( P_f \)). On the other hand, \( P_f \) is a secondary (and slow) transient electron trapping process based on electrons having sufficient thermal energy. In this model, the equation for the kinetics of electron trapping can be expressed as follows.

\[
n = N_s(1 - e^{-P_f})
\]

(4)

Here, \( n \) is the number of the occupied defect-sites, \( N_s \) is the total available trap number, \( p \) is the electron-trapping probability, and \( t \) is the time for the process. Figure 5(b and c) show the transient drain current of HIZO and HIZO-IZO layers versus measurement temperature. By fitting equation (4) to \( \Delta I_f \) during the short charging time (initial 50 \( \mu \)s), we analyzed fast electron trapping characteristics, which indicate that fast charging is not dependent on measurement temperature. For single-layer HIZO and bilayer HIZO-IZO TFTs, the extracted \( N_s \) values are on the order of 8.4 \( \times \) 10^{13} and 2.2 \( \times \) 10^{12} cm^{-2}, respectively.

To probe the slow transient charge trapping phenomena, the transient drain current versus time was obtained during the long stress time (approximately 1000 ms), as depicted in Fig. 5(e,f), because slow transient charging follows a thermally activated process from trap to trap via activation energy. According to this model including the thermal activation process, the kinetics of the charging process can be expressed by Eq. (5).

\[
I_f(i) = n \frac{1}{\tau} \exp \left( \frac{-E_i}{kT} \right)
\]

(5)

where \( f \) is the current density, \( \tau \) is the de-trapping time constant, \( E_i \) is the trap energy, \( k \) is the Boltzmann constant, and \( T \) is temperature. Then, the slow transient charge trapping process with time is given by Eq. (6).

\[
N = N_s \sum_i (1 - e^{-P_f})
\]

(6)

In our study, we used two terms in Eq. (6) based on fitting for all measurement temperatures. Figure 5(g and h) show measured (symbol) and fitting (line) \( \Delta I_f \) data for the slow transient charging model for two devices, respectively. The relation of \( \ln(P_f) \) versus \( 1/kT \) generates \( E_f \) and \( E_s \), which represent trap energy barriers for slow transient charge flux: \( E_f = 0.24 \) eV, \( E_s = 0.30 \) eV (single-layer HIZO) and \( E_f = 0.22 \) eV, \( E_s = 0.27 \) eV (bilayer
HIZO-IZO), respectively, as shown in Fig. 5(i). This result indicates that the single-layer HIZO TFT has a larger number of defects and is more vulnerable to transient charge trapping, relative to the bilayer HIZO-IZO TFT.

Discussion
In summary, we evaluated the transient charge trapping effect, the charge trapping mechanism, and the dynamic charge transport of single-layer HIZO and high-mobility bilayer HIZO-IZO oxide TFTs. In our study, we carried out μs-FIV, PIV, transient current, and DCA analysis methods. The results indicate that the mobility enhancement rate of single-layer HIZO and bilayer HIZO-IZO is closely related to the charge trapping effect. The charge trapping mechanism follows the three-trap model with three different trapping time constants. The transient charge trapping model for both TFTs follows temperature-insensitive fast-transient charging and thermally activated slow transient charging with shallow and deep trap energies. For single-layer HIZO and bilayer HIZO-IZO TFTs, the extracted $N_0$ values are on the order of $8.4 \times 10^{13}$ and $2.2 \times 10^{12}$ cm$^{-2}$, respectively. Insignificant fast-transient charging of the bilayer HIZO-IZO TFT can be explained by the low density of sub-gap states in oxide TFTs. Various trap analysis methods allow us to evaluate defects; transient charge trapping study of oxide semiconductors improves understanding of the device instability and contributes to solving this problem.

Methods
Device Fabrication. We fabricated a bilayer oxide semiconductor TFT using an inverted staggered structure, as shown in Fig. 2(a). The integration of metal oxide semiconductor bilayer TFTs was done by sputter deposition of 100-nm thick Mo electrode at room temperature and subsequently growing a gate insulator of 100-nm thick...
SiO₂ by the plasma-enhanced chemical vapor deposition (PECVD). As an active channel, four different type of semiconductor layer configurations (such as HIZO (40 nm), HIZO (20 nm)-IZO (20 nm), HIZO (20 nm)-IZO (40 nm) and IZO (60 nm) channel) were employed. The films were deposited at room temperature by radio frequency (RF) magnetron sputtering method using separate 4-inch diameter target of In₂O₃, ZnO, and HfO₂. The RF power supplied to each of the targets was adjusted to control the composition of HIZO and IZO. The composition of the channel was determined by the duty cycle of the pulse (50%) at a given frequency; the rising/falling time was fixed at 80 ns.

23. Choi, H.

21. Munzenrieder, N.

26. Ghaffarzadeh, K.

28. Kim, M.-G., Kanatzidis, M. G., Facchetti, A. & Marks, T. J. Low-temperature fabrication of high-performance metal oxide thin-film semiconductors. Nat. Nanotechnol. 7, 798–805 (2012).

24. Lee, S.

20. Park, J. C.

15. Choi, H.-S. & Jeon, S. Thickness dependent low-frequency noise characteristics of a-InZnO thin-film transistors under light illumination. Appl. Phys. Lett. 100, 013503 (2012).

13. Ahn, S. et al. Phosphorescent of an oxide semiconductor photosensor. J. Vac. Sci. Technol. B 33, 031205 (2015).

12. Jeon, S. et al. Short channel device performance of a-InGaZnO thin film transistor. Appl. Phys. Lett. 99, 082104 (2011).

11. Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. Adv. Mater. 24, 2945–2986 (2012).

10. Choi, H.-S. & Jeon, S. Anomalous high photoconductivity in short channel indium-zinc-oxide photo-transistors. Appl. Phys. Lett. 106, 013503 (2015).

9. Yu, X. et al. A synergistic approach to high-performance oxide thin film transistors using a bilayer channel architecture. ACS Appl. Mater. Interfaces 5, 7983–7988 (2013).

8. Park, J. C. et al. Highly Stable Transparent Amorphous Oxide Semiconductor Thin-film Transistors Having Double-stacked Active Layer. Adv. Mater. 22, 5512–5516 (2010).

7. Jeong, J. K. Photo-bias Instability of Metal Oxide Thin Film Transistors for Advanced Active Matrix Displays. J. Mater. Res. 28, 1071–1084 (2013).

6. Lee, S., Jeon, S., Chaji, R. & Nathan, A. Transparent Conducting Oxide Technology for Touch Free Interactive Flexible Display. J. Display Technol. 10, 917–927 (2014).

5. Ghaffarzadeh, K. et al. Persistent photoconductivity in Hf-In-Zn-O thin film transistors. Sci. Rep. 2, 2945–2986 (2012).

4. Jeon, S. et al. Persistent photoconductivity in Hf-In-Zn-O thin film transistors. Appl. Phys. Lett. 97, 143510 (2010).

3. Jeon, S. et al. Nanometer-scale oxide Thin Film Transistor with Potential for High Density Image Sensor Applications. ACS Appl. Mater. Interfaces 3, 1–6 (2011).

2. Munzenrieder, N. et al. Verification of Interface State Properties of a-InGaZnO Thin Film Transistors with SiNx/SiO2 gate dielectrics. IEEE Trans. Electron Devices 58, 1038–1045 (2011).

1. Kim, S. et al. Nanocrystalline ZnON; High mobility and low band gap semiconductor material for high performance switch dielectrics. J. Vac. Sci. Technol. B 30, 031205 (2012).

References

1. Kwon, J. Y. et al. Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors. Semicond. Sci. Technol. 30, 024002 (2015).

2. Nomura, K. et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature 432, 488–492 (2004).

3. Jeong, J. K. Photo-bias Instability of Metal Oxide Thin Film Transistors for Advanced Active Matrix Displays. J. Mater. Res. 28, 1071–1084 (2013).

4. Jeon, S. et al. Origin of High Photoconductive Gain in Fully Transparent Heterojunction Nano-crystalline Oxide Image Sensors and Interconnects. Adv. Mater. 26, 7102–7109 (2014).

5. Nathan, A., Lee, S., Jeon, S. & Robertson, J. Amorphous Oxide Semiconductor TFTs for Displays and Imaging. J. of Display Technology 10, 917–927 (2014).

6. Lee, S., Jeon, S., Chaji, R. & Nathan, A. Transparent Semiconductor Technology for Touch-Free Interactive Flexible Display. Proc. IEEE 103, 644–64 (2015).

7. Jeong, J. K. et al. Origin of Threshold voltage instability in Indium-Gallium-Zinc-Oxide Thin Film Transistors. Appl. Phys. Lett. 93, 123508 (2008).

8. Park, J.-S. et al. Novel ZnInZnO Thin-film Transistor with Excellent Stability. Adv. Materials 21, 329–333 (2008).

9. Van de Walle, C. G. Hydrogen as a cause of doping in zinc oxide. Phys. Rev. Lett. 85, 1012–1015 (2000).

10. Choi, H.-S. et al. Influence of HF contents on interface state properties in a-HfInZnO thin-film transistors with SiNx/SiO2 gate dielectrics. Appl. Phys. Lett. 99, 183502 (2011).

11. Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. Adv. Mater. 24, 2945–2986 (2012).

12. Choi, H.-S. & Jeon, S. Anomalous high photoconductivity in short channel indium-zinc-oxide photo-transistors. Appl. Phys. Lett. 106, 013503 (2015).

13. Ahn, S. et al. Phosphorescence of an oxide semiconductor photosensor. J. Vac. Sci. Technol. B 33, 031205 (2015).

14. Lee, E. et al. Nanocrystalline ZnON; High mobility and low band gap semiconductor material for high performance switch transistors and image sensor applications. Sci. Rep. 4, 4948 (2014).

15. Choi, H.-S. & Jeon, S. Thickness dependent low-frequency noise characteristics of a-InZnO thin-film transistors under light illumination. Appl. Phys. Lett. 104, 023505 (2014).

16. Choi, H.-S. & Jeon, S. Instability in threshold voltage and sub-threshold behavior in Hf-In-Zn-O thin film transistors induced by bias- and light-Stress. Appl. Phys. Lett. 97, 113504 (2010).

17. Kim, M.-G., Kanatzidis, M. G., Facchetti, A. & Marks, T. J. Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing. Nature Materials 10, 382–388 (2011).

18. Jeon, S. et al. Nanometer-scale oxide Thin Film Transistor with Potential for High Density Image Sensor Applications. ACS Appl. Mater. Interfaces 3, 1–6 (2011).
31. Seo, D. et al. Fully transparent InGaZnO thin film transistors using indium tin oxide/graphene multilayer as source/drain electrodes. 

32. Choi, H.-S. & Jeon, S. Field-induced macroscopic barrier model for persistent photoconductivity in nanocrystalline oxide thin-film transistors. Appl. Phys. Lett. 97, 172106 (2010).

33. Jeon, S. et al. Low-frequency Noise Performance of a bilayer InZnO-InGaZnO Thin Film Transistor for Analog Device Applications. IEEE Electron Device Lett 31, 1128–1130 (2010).

34. Choi, H. et al. Verification of interface state properties of a-InGaZnO thin-film transistors with and gate dielectrics by low frequency noise measurements. IEEE Electron Device Lett. 32, 1083–1085 (2011).

35. Cheong, W. S. et al. Current stress induced electrical instability in transparent zinc tin oxide thin-film transistors. J. Nanosci. Nanotechnology 12, 3421–3424 (2012).

36. Bersuker, G. et al. Mechanism of Electron Trapping and Characteristics of Traps in HfO2 Gate Stacks. IEEE Trans. Dev. Mat. Reliability 7, 138–145 (2007).

37. Young, C. D. et al. Pulsed–methodology and its application to electron trapping characterization and defect density profiling. IEEE Trans. Electron. Device Lett. 56, 1322–1329 (2009).

38. Ahn, S. et al. High-performance nanowire oxide photo-thin film transistor. Advanced Materials 25, 5549–5554 (2013).

39. Park, J. C., Kim, S. W., Kim, C. J. & Lee, H.-N. The Effects of Gadolinium Incorporation Into Indium–Zinc–Oxide Thin-Film Transistors. IEEE Electron Device Letters 33, 809–811 (2012).

40. Barquinha, P., Pimental, A., Marques, A., Pereira, L., Martins, R. & Fortunato, E. Influence of the semiconductor on the electrical properties of transparent TFTs based on Indium Zinc Oxide. J. Non-Cryst. Solids 352, 1749–1752 (2006).

41. Itagaki, N. et al. Zn-In-O based Thin-Film Transistors-compositional dependence. Phys. Status solidi A 205, 1915–1919 (2008).

42. Lee, E. et al. Ultra-short pulse current–voltage characterization of the intrinsic characteristics of high-k devices. Japan. J. Appl. Phys. 44, 2437–2440 (2005).

43. Lee, Y. et al. Fast transient charging at the Graphene/SiOx interface causing hysteretic device characteristics. Appl. Phys. Lett. 98, 183508 (2011).

44. Shen, C. et al. A fast measurement technique of MOSFET Id–Vg characteristics. IEEE Electron Device Lett. 27, 55–56 (2006).

45. Lee, Y. et al. Quantitative analysis of hysteretic reaction at the interface of Graphene and SiOx using the short pulse I-V method. Carbon. 60, 453–460 (2013).

46. Young, C. D. et al. The pulsed Id–Vg methodology and its application to the electron trapping characterization of high-k gate dielectrics. J. Semicond. Technol. Sci. 10, 79–90 (2010).

47. Kim, T. et al. Effect of hydrogen on dynamic charge transport in amorphous oxide thin film transistors. Nanotechnology 27, 325203 (2016).

48. Kim, T. et al. High mobility and high stability glassy metal-oxynitride materials and devices. Sci. Rep. 6, 23940 (2016).

49. Kim, T. et al. Fast transient charging behavior of HfInZnO thin-film transistor. Appl. Phys. Lett. 107, 093503 (2015).

50. Heh, D., Young, C. D. & Bersuker, G. Experimental evidence of the fast and slow charge trapping/detrapping processes in high-k dielectrics subjected to RTI stress. IEEE Electron Device Lett. 29, 180–182 (2008).

51. Heh, D., Choi, R., Young, C. D. & Bersuker, G. Fast and slow charge trapping/detrapping processes in high-κ nMOSFETs. In Proc. IEEE IRW Final Report 120–124 (2006).

52. Kim, T. et al. The influence of interfacial defects on fast charge trapping in Nano-crystalline oxide semiconductor thin film transistor. Semicond. Sci. Technol. 31, 055014 (2016).

53. Kim, T. et al. Influence of fast charging on accuracy of mobility in a-InHfZnO Thin film transistor. IEEE Electron Device Lett. 38, 203–206 (2017).

54. Paulsen, R. E. & White, M. H. Theory and application of charge pumping for the characterization of Si-SiO2 interface and near-interface oxide traps. IEEE Trans. Electron. Device 41, 1213–1216 (1994).

55. Groeseneken, G., Maes, H. E., Beltran, N. & De Keersmaecker, R. F. Reliable approach to charge-pumping measurements in MOS transistors. IEEE Trans. Electron Device ED-31, 42–53 (1984).

56. Jung, U. et al. Quantitatively estimating defects in graphene device using discharge current analysis method. Sci. Rep. 4, 4886 (2014).

57. Jung, U. et al. Quantitative analysis of interfacial reaction at a graphene/SiO2 interface using the discharging current analysis method. Appl. Physic. Lett. 104, 151604 (2014).

58. Jung, U. et al. Extraction of the interface state density of top-gate graphene field-effect transistor. IEEE Electron Device Lett. 36, 408–410 (2015).

59. Choi, H. The impact of active layer thickness on low-frequency noise characteristics in InZnO thin-film transistors with high mobility. Appl. Phys. Lett. 100, 173501 (2012).

60. Barquinha, P., Goncalves, G., Pereira, L., Martins, R. & Fortunato, E. Effect of annealing temperature on the properties of IZO films and IZO based transparent TFTs. Thin Solid Films 515, 8450–8454 (2007).

61. Kim, T. et al. Pulse I-V characterization of a Nano-crystalline oxide device with sub-gap density of states. Nanotechnology 27, 325203 (2016).

62. Lee, S. et al. Extraction of sub-gap density of states in amorphous InGaZnO thin-film transistors by using multifrequency capacitance–voltage characteristics. IEEE Electron Device Letters 31, 231–233 (2010).

63. Chen, C., Abe, K., Kumomi, H. & Kanicki, J. Density of states of a-InGaZnO from temperature-dependent field-effect studies. IEEE Trans. Electron Devices 56, 1177–1183 (2009).

64. Jeon, Y. W. et al. Sub-gap density of state based amorphous oxide thin film transistor simulator (DeAOTS). IEEE Trans. Electron. Device, 57, 2988–2999 (2010).

65. Lee, S. et al. Oxygen defect-induced metastability in amorphous semiconductors probed by gate pulse spectroscopy. Sci. Rep. 5, 14902 (2015).

66. Lee, E. et al. Ar plasma treated ZnO thin film transistor for future thin film electronics. Appl. Physic. Lett. 107, 122105 (2015).

67. Ao, L. et al. High-performance InZnO thin-film transistors deposited by magnetron sputtering. Chin. Phys. Lett. 30, 127301 (2013).

68. Kim, T. et al. The influence of Hydrogen on defects of In-Ga-Zn-O semiconductor thin-film transistors with atomic-layer deposition of Al2O3. IEEE Electron Device Letters 37, 1131–1134 (2016).

Acknowledgements

This work was supported by a Korea University Grant.

Author Contributions

H.W. and S.J. contributed equally to this work. S.J. designed this work. S.J. carried out the HIZO & HIZO-IZO TFTs fabrication and H.W. performed electrical measurement and data analysis. S.J. wrote the main manuscript. All authors reviewed the results and implications and commented on the manuscript at all stages. The project was guided by S.J.
Additional Information

Competing Interests: The authors declare that they have no competing interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article’s Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article’s Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2017