Effect of NBTI on the Electrical Characteristics and Trap States of Low Temperature Poly-silicon Thin Film Transistor

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ABSTRACT: Polysilicon thin film transistors have broad application prospects in high-performance flat panel displays and flexible wearable devices due to their high carrier mobility and good stability. However, due to process conditions and other reasons, there are traps inside, and under some electrical stress conditions, its electrical properties will degrade. Here we report the changes in electrical characteristics of p-type polysilicon thin film transistors with stress time at a negative gate voltage of -20V and a temperature of 60°C. It is obtained that the transfer characteristics of the p-type polysilicon thin film transistor move in the negative direction with the increase of Negative Bias Temperature Instability time, and with the increase of SS degradation, and the total trap state inside it is calculated by SS, which provides a theoretical basis for improving the reliability of the device.

1. Introduction
The flat panel display industry is one of the pillar industries in the modern electronic information industry. With the rapid development of the information industry, the flat panel display industry has maintained rapid growth [1]. Thin film transistors are the core devices in the flat panel display industry. TFT is an insulated gate field effect transistor. Its conduction principle is similar to that of a MOSFET. It is also a gate control device with a semiconductor active layer film as the channel region. At present, thin film transistors are mainly divided into traditional amorphous silicon thin film transistors (a-Si:H TFT), Amorphous Indium Gallium Zinc Oxide, a-IGZO TFT and Low Temperature Poly-Si TFT. Compared with amorphous silicon thin film transistors and indium gallium zinc oxide TFTs, polysilicon thin film transistors have higher carrier mobility and higher stability, and at the same time overcome bias stress instabilities of a-Si TFTs [2].

This article mainly chooses LTPS TFT for research, characterizes the basic electrical characteristics of flexible LTPS TFT, and studies the degradation of LTPS TFT under negative bias temperature instability stress at the same time, the basic electrical characteristic parameters of LTPS-TFT and the changes of the total trap concentration before and after the DC gate stress degradation are analyzed. It provides important guidance for improving the reliability of LTPS TFT.

2. experimental details
The Figure 1.shows the schematic of LTPS TFT. LTPS-TFT is grown on a polyimide substrate, the buffer layer is composed of 300nm SiO2 and 100nm SiNx, the active layer is a 50nm polysilicon film, the gate insulating layer is composed of 120nm SiO2, and the surface of the device is passivated with 2um polyimide for protection. Device characteristics are measured to prevent surface oxidation and degradation. The gate
Electrode material is Mo, and the source and drain electrode materials are Ti/Al/Ti. In the experiment, the electrical characteristic curve of the device is measured using the B1500A semiconductor parameter analyzer.

![Schematic of LTPS TFT](image)

### 3. Results and Discussion

The Figure 2.(a)(b) shows the transfer curve and output curve characteristic diagram of LTPS TFT. It shows typical p-type transistor behavior, $V_{GS}$, $V_{DS}$, $I_{DS}$ represent the gate-source voltage, source-drain voltage, and source-drain current, respectively. The output curve was measured by changing $V_{GS}$ from -1V to -5V, and all the curves showed channel pinch-off and channel current saturation.

When the absolute value of $V_{GS}$ is greater than the absolute value of $V_{th}$ and satisfies $|V_{GS}-V_{th}| \geq |V_{DS}|$, holes accumulate to generate a conductive channel, and a channel current $I_{DS}$ is generated. At this time, the LTPS TFT is in the linear region, and its voltage-current characteristic satisfies the following formula(1)[5]:

$$I_{DS} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} [2(V_{SG} + V_{TH})V_{SD} - V_{DS}^2]$$

In this formula, $\mu_p$ is the hole field effect mobility, and $C_{ox}$ is the gate oxide capacitance per unit area. When the absolute value of the gate-source voltage is further increased, the absolute value of the gate-source voltage $|V_{GS}|$ is much larger than the absolute value of the source-drain voltage $|V_{DS}|$, and $|V_{DS}| \ll 2|V_{GS} - V_{th}|$, the device is in the deep in the linear region, the source-drain current $I_{DS}$ and the gate-source voltage $V_{GS}$ are in a strictly linear proportional change, so the $1/2V_{DS}^2$ term in the above formula can be ignored, and the formula(1) is simplified to the following formula(2)[5]:

$$I_{DS} = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} + V_{TH})V_{SD}$$

Based on this formula, the first-order partial derivative of the abscissa gate-source voltage is obtained through the transfer characteristic curve, and the first-order partial derivative is crossed with the abscissa gate-source voltage by linear fitting and extrapolation, and the crossing point is the threshold voltage $V_{th}$[3]. Calculate the threshold voltage of the device $V_{th}$=0.89V. In addition, when $V_{GS}$ is less than $V_{th}$, but close to $V_{th}$, the device is not completely turned off. At this time, there will be a weak inversion layer at the gate oxide layer and the channel interface, and a small channel current will exist. This phenomenon is sub-threshold conduction. The definition of the sub-threshold swing is the change in the gate-source voltage $V_{GS}$ corresponding to an order of magnitude change in the channel current $I_{DS}$ in the sub-
threshold region. The definition formula of the sub-threshold swing is shown in the following formula (3)[5], and the sub-threshold swing of the device is obtained as 0.73V/dec.

\[
SS = \frac{dV_{GS}}{d(logI_{DS})}
\]  

(3)

In addition, this article studies the degradation of LTPS-TFT under DC gate stress. Since LTPS TFT is a p-type device, NBTI is applied to the device. The electrical stress is applied as shown in the Figure 3. The DC negative gate stress is applied to the device on the gate, both the source and drain are grounded. The specific stress conditions are T=60°C and VGS=-20V. The figure 4. shows the transfer characteristic curve of LTPS TFT in the initial state, 2 hours after NBTI and 8 hours after NBTI. It can be seen that the transfer characteristic curve of the device shifts to the left as the time of NBTI time increases. The degradation of NBTI is manifested as the threshold voltage shift, and the threshold voltage \( V_{th} \) continues to drift in the negative direction. The threshold voltage after 2 hours of NBTI is -5.5V, and the threshold voltage after 8 hours of NBTI is -6.6V. At the same time, with the degradation of the sub-threshold swing SS, the sub-threshold swing SS after 2 hours of NBTI is 0.84V/dec, and the sub-threshold swing SS after 8 hours of NBTI is 0.99V/dec. The subthreshold swing is slightly degraded with NBTI.

According to reports, in polysilicon thin film transistors, the degradation mechanism of NBTI mainly follows the React-Diffusion (RD) model. When a negative bias voltage is applied to the gate for a long time, the weaker Si-H bond interacts with holes and the H atoms are released. After the reaction, H atoms diffuse into the gate insulating layer to form a positive oxide charge, so the threshold voltage moves in the negative direction. [4]

The power law between logarithmic stress time and logarithmic \( V_{th} \) shift can be calculated, and the factor \( n \) (slope) can be extracted, as shown in Figure 5. The horizontal axis time is plotted on a logarithmic scale.

\[
N_T = N_{bulk} + N_{it} = \left( \frac{SS_{log(e)}}{kT/q} - 1 \right) \frac{c_{ax}}{q}
\]

(4)

In addition, the subthreshold swing SS is closely related to the trap state density. The total trap state \( N_T \) is composed of the bulk trap state density \( N_{bulk} \) and the SiO\(_2\)/channel interface state density. The total trap state \( N_T \) and the subthreshold swing SS follow the relationship of the following formula (4)[6]:

![Figure 3. Application mode of electric stress](image)

![Figure 4. The transfer curve of Initial state, NBTI 2 hours, NBTI 8 hours](image)

![Figure 5. The power-law relationship between threshold voltage and stress time.](image)
Among them, e is Euler's number, k is Boltzmann's constant, T is the thermodynamic temperature, \( C_{ox} \) is the gate oxide capacitance per unit area, and q is the amount of charge. \( C_{ox} = 2.876 \times 10^{-8} \text{F/cm}^2 \). According to the above formula, the initial state, total trap states after 2 hours of NBTI and 8 hours after NBTI are extracted to be \( 2.01 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1} \), \( 2.34 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1} \), \( 2.79 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1} \). This is because the NBTI causes the Si-H bond to break, and H diffuses into the gate oxide or Si bulk, leaving interface traps. The increase of interface traps is equivalent to changing the interface state, thereby affecting the total trap state density.

4. conclusion

This paper mainly describes the influence of the negative bias temperature instability applied for different time on the polysilicon thin film transistor. The electrical characteristics of the polysilicon thin film transistor show that the threshold voltage \( V_{th} \) moves in the negative direction as the negative bias temperature instability experiment is applied for a longer period of time. The sub-threshold swing becomes larger, and the calculated total trap state density of the device becomes larger, and the device performance is slightly degraded. The reason is that NBTI increases the interface state, which affects the total trap state density.

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