Drawing Inductor Layout with a Reinforcement Learning Agent: Method and Application for VCO Inductors

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Design of Voltage-Controlled Oscillator (VCO) inductors is a laborious and time-consuming task that is conventionally done manually by human experts. In this paper, we propose a framework for automating the design of VCO inductors, using Reinforcement Learning (RL). We formulate the problem as a sequential procedure, where wire segments are drawn one after another, until a complete inductor is created. We then employ an RL agent to learn to draw inductors that meet certain target specifications. In light of the need to tweak the target specifications throughout the circuit design cycle, we also develop a variant in which the agent can learn to quickly adapt to draw new inductors for moderately different target specifications. Our empirical results show that the proposed framework is successful at automatically generating VCO inductors that meet or exceed the target specification.

1 INTRODUCTION

Voltage Controlled Oscillators (VCOs) are circuits that generate an oscillating signal whose frequency is controlled by an input voltage. As such, VCOs are widely used in Radio Frequency (RF) applications where there is a need to tune the device within a certain range of frequencies. A common form of VCO, which we focus on in this paper, is the Inductance Capacitance VCO that uses the coupling between an inductor and a capacitor to generate the oscillating signal. In this case, the capacitor is tuned by a voltage input to modify the frequency. To achieve a wide tuning range with a VCO, the effective resistance of the inductor should remain low, the Self-Resonance Frequency (SRF) should be high, and most importantly, the inductance should stay close to a target value.

Since the shape of an inductor determines its effective inductance and resistance, it is important to design it in such a way that the resulting inductor meets the performance requirements (i.e., desired specifications such as the effective inductance, resistance, etc.). There are, however, clear and strict design requirements (e.g., maximum available area, no crossing wires, wire turn angle constraints, etc.) that are imposed by manufacturing considerations.

Conventionally, the layout of an inductor is designed manually by human experts (see for example, Figure 1); however, this is a complex and time-consuming task. It involves an iterative process with two major steps: a human expert first designs/modify an inductor layout to meet a certain target specification, and analyzes the simulation performance of the inductor in a larger circuit. In this work, we formulate the task as an optimization problem that takes into account the above-mentioned design and performance requirements while generating inductor layouts. Our algorithm can come up with a variety of layout shapes, all of which can meet or exceed the target specifications. This is beneficial for cases where the canvas shape is irregular for example. Moreover, some of produced layouts might take a smaller area than what the human designers have come up with, which is desirable.

Fig. 1. Canvas properties of an example inductor layout.
We formulate the design framework for VCO inductors as a drawing task. Specifically, it is formulated as a Markov Decision Process (MDP) [14], where an agent draws a single wire segment on the canvas at each time step. Hence the framework is much more flexible compared to the template-based methods (elaborated in the Related Works section) in terms of the variety of shapes it can generate.

Moreover, our framework allows for several optimization techniques to be used to generate candidate layouts. Here, we focus on using Reinforcement Learning (RL) [15]. We show that the RL agent is able to generate candidate designs with performance matching the target specifications. We also develop a variant that adapts faster than the alternative optimization methods when the target performance requirements are [mildly] shifted.3

2 RELATED WORKS

Note that the goal for VCO inductor design is to find the best geometry that can even exceed the target specifications. This goal is different from the majority of literature on optimizing passive designs since they are often focused on only meeting the target specifications with the minimum number of simulations. VCO inductors are special because there are usually only a few of them on a chip, so finding the optimal one is quite important.

Existing methods related to the automated layout design for VCO inductors are summarized in Table 1, where the characteristics of each method is compared to the proposed approach. Description of each existing method follows.

2.1 Template Optimization

Current Electronic Design Automation (EDA) tools for inductor design formulate their solution as optimizing only a certain set of parameters of a fixed template layout. That is, the shape of the layout is pre-determined (e.g., a spiral), and the optimization procedure searches through the valid values of the layout’s parameters (e.g., number of turns, wire width, wire spacing, etc.) in order to find inductors that meet the target specification. Various optimization approaches have been used in the literature: Genetic Algorithm (GA) [2, 9], Heuristic Techniques [4], Bayesian Optimization (BO) [16], Evolutionary Computation and Gaussian-Process Surrogate Modeling [13], and Corner-Aware Optimization [12].

The problem with the template optimization approach is two-fold: (i) the rigidity of the pre-determined layout that hugely limits the search space for valid inductors, which in turn results in designing sub-optimal layouts; and (ii) inability to quickly come up with a new design that meets a moderately different target specification (i.e., the entire algorithm must be re-run and no knowledge transfer is possible from previously learned models).

2.2 Evolved Antenna

Hornby et al. [5] converted the problem of antenna design into a 3D drawing problem. Their proposed algorithm applies GA to open-ended sequences of line segments, where the mutations include:

- (i) adding to the length of each line segment; and (ii) rotating each line segment along x, y, and z axes.

To the best of our knowledge, such a step-by-step method that involves drawing has not been used to tackle VCO inductor design; and it is not trivial how to convert the antenna design to a VCO inductor design problem either. This is because the former requires evaluation of an incomplete antenna at each time step while the VCO inductor does not require that. The inductor must be completed (i.e., the input port is wired to the output port) before its performance is evaluated through simulations (this is beneficial since queries to the simulator are quite time-consuming). Moreover, similar to the template optimization methods, this approach is not able to quickly come up with a new design that meets a moderately different altered performance requirements than the original one.

3 VCO INDUCTOR DESIGN AS A DRAWING TASK

In our formulation of the VCO inductor design process, an inductor is described by a sequence of segments, where at each step, knowledge of the past steps is used to determine the placement of a new segment. Each segment contains information on its wire length, width, angle relative to the previous segment, and the metal layers on the chip which will contain this segment. This information is sufficient in order to manufacture a designed layout as an on-chip inductor. The first segment is always initiated at the input port (the location is determined by some parameters of the circuit), and each subsequent segments are relative to the one before them. A design is considered invalid if wire collision has happened or some portion of the inductor extends outside the maximum available area. Designs are considered complete when a segment has reached the output port for non-symmetric designs or the vertical mid-line for symmetric designs.

The action space corresponds to the information required for placing each segment. To constrain the huge search space and keep the experiments simple, the designs were enforced to have a fixed wire width across all segments and the length of each segment was fixed. As such, the action space was reduced to covering only the angle of the segment relative to the previous one. To comply with the design requirements, the angles are discretized, with actions 0°, 22.5°, 45°, 67.5°, 90°, 112.5°, 135°, 157.5°, and 180°.

As such, our method is quite flexible with the layouts that it can generate. Thus, we can design a valid inductor even when our available space is not evenly shaped (e.g., a perfectly square canvas) with a non-symmetric design. Conventionally, however, symmetric designs are preferred in practice to preserve symmetry in the overall circuit. Hence in our paper, we focus on symmetric cases without loss of generality. In this case, the drawing task terminates when it reaches the vertical mid-line between the input and output ports, and the segments are mirrored to complete the inductor.

6Although the wire width could be added to the action space (as a dimension), for our setting, we found the respective improvement to be empirically insignificant.

7Note that this is a manufacturing constraint that we embedded into our method. Our formulation is general and the actions can use finer discretizations of the angles based on the need and requirements.
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| Methods                   | Reliance on Expert Knowledge | Sample Efficiency | Design Space               | Transfer to Different Targets |
|---------------------------|-----------------------------|-------------------|----------------------------|-------------------------------|
| Template Optimization     | High                        | High              | Highly Constrained         | Hard                          |
| Evolved Antenna           | ?                           | ?                 | Less Constrained           | Hard                          |
| Our Proposed Solution     | Low                         | High              | Less Constrained           | Easy                          |

Table 1. Comparison of the proposed method and the existing approaches.

This formulation can be applied to arbitrary sequential optimization techniques by (i) providing the technique with some representation of the current segments, and (ii) receiving from the technique the parameters for drawing the next segment. For non-sequential baseline methods that operate on a fixed set of parameters, a fixed number of segments can be used as the optimization target, considering only as many segments from the result as are needed to create an inductor design and discarding the rest.

To summarize, the proposed framework is comprised of the following four modules (see also Figure 2), which all interact with each other to produce the overall solution:

1. The **inductor drawer** module is in charge of producing the inductor designs. It creates an inductor by adding line segments (each describing a segment of wire that can be realized) to the canvas, starting from a specified input position and appending each segment onto the previous one. These segments are each drawn using several parameters provided by the optimizer module.

2. The **optimizer** module is in charge of ensuring that the performance of the produced inductors will be improving with respect to their target specifications. Feedback is given to the optimizer in terms of how well designs met the target specifications or how badly they violated the design constraints. This feedback allows the optimizer to improve its model, such that it suggests parameters that result in designing more optimal layouts.

3. The **cache** module records all valid inductor designs that have been generated as well as their evaluated performance. The cache is used for fast retrieval of the performance measures of already seen layouts so that the number of queries to the [slow] simulator is minimized.

4. The **simulator** module takes the newly produced inductor designs from cache, evaluates them, and returns their performance specifications — i.e., L (inductance), R (resistance), SRF, Q (quality factor), etc. to be recorded in the cache. Processing each query to the simulator is often the bottle-neck in the procedure.

4 REINFORCEMENT LEARNING FOR OPTIMIZATION

We use RL to solve the drawing task by serving as the optimizer module of the proposed framework. For that, we formulate the optimizer module’s task as an MDP, denoted by a tuple $\langle S, A, R, P, \rho, \gamma \rangle$, where $S$ and $A$ are the finite state space and finite action space respectively; $R: S \times A \rightarrow \mathbb{R}$ is the reward function; $P(s, a, s')$ is the transition probabilities; $\rho$ is the state distribution of the initial state $s_0$ which is deterministic in our task (i.e., the first wire segment always starts at the input port); and $\gamma \in [0, 1]$ is the discount factor.

The goal of the design task is to maximize the expected sum of discounted rewards (i.e., the return) $J_\pi = \mathbb{E}_\pi \left[ \sum_{t=0}^{T} \gamma^t R(s_t, a_t) \right]$ where $s_t$ and $a_t = \pi(s_t)$ are the state and action at time step $t$ and policy $\pi(\cdot)$ is a function that maps a state to an action. $T$ is the termination time step of the episode. We set discount factor $\gamma = 1$.
since this is an episodic problem with sparse rewards where the reward is non-zero only at terminal states and zero elsewhere.\(^{10}\)

In our formulation, an episode corresponds to one attempt at drawing an inductor, whether the resulting inductor is valid or not. A valid inductor is one whose input port is successfully connected to its output port, without any wire collisions. In order to maximize efficiency, we added a masking mechanism in which the action(s) that result in colliding to another wire are eliminated from the agent's search space. This helps preserving what the agent has drawn so far and attempt to learn on top of that.

To ensure that the inductors are being optimized for the performance requirements, we design our reward signal accordingly. The reward is zero for non-terminal states (i.e., no feedback is given to an incomplete inductor). As soon as an episode is terminated (i.e., either when wires collision or area perimeter collision is inevitable; or the input and output ports are successfully connected) a reward is given. If the former was true, i.e., the generated layout was an invalid design, a small penalty is given; otherwise the reward is determined from how well the designed inductor’s specifications meets the performance requirements. The reward function for a complete inductor is defined as:

\[
1 - \frac{\omega_L \times C_L + \omega_R \times C_R + \omega_{\text{SRF}} \times C_{\text{SRF}} + \omega_{\text{Area}} \times C_{\text{Area}}}{\omega_L + \omega_R + \omega_{\text{SRF}} + \omega_{\text{Area}}}
\]  

(1)

where \(C_L\), \(C_R\), \(C_{\text{SRF}}\), and \(C_{\text{Area}}\) stand for the cost of inductance, resistance, SRF, and area respectively; and \(\omega_L\), \(\omega_R\), \(\omega_{\text{SRF}}\), and \(\omega_{\text{Area}}\) stand for the weights of each respective cost.

The cost values are computed as follows:

\[
C_L = \begin{cases} E_L & E_L < 0.05 \\ 2E_L - 0.05 & E_L \geq 0.05 \end{cases}
\]

\[
C_R = \begin{cases} 0 & E_R < 0 \ & E_L \geq 0.05 \\ E_R < 0 & E_L < 0.05 \ & \text{min}(2E_R, 1) \ & E_R \geq 0 \end{cases}
\]

\[
C_{\text{SRF}} = \begin{cases} 0 & E_{\text{SRF}} < 0 \ & E_L \geq 0.05 \\ \text{max}(2E_{\text{SRF}}, -1) & E_{\text{SRF}} < 0 \ & E_L < 0.05 \\ \text{min}(2E_{\text{SRF}}, 1) & E_{\text{SRF}} \geq 0 \end{cases}
\]

\[
C_{\text{Area}} = \begin{cases} 0 & E_{\text{Area}} < 0.05 \\ E_{\text{Area}} & E_{\text{Area}} \leq 0.05 \end{cases}
\]

where \(E_L = \frac{1}{L_T} - 1\), \(E_R = \frac{R}{R_T} - 1\), \(E_{\text{SRF}} = 1 - \frac{\text{SRF}}{\text{SRF}_T}\), \(E_{\text{Area}} = \frac{\text{Area}_{\text{MAX}}}{\text{Area}} - 1\), and \(L_T\), \(R_T\), \(\text{SRF}_T\) are the target specifications and \(\text{Area}_{\text{MAX}}\) is the maximum area available for the canvas.

The reward function is a linear combination of the cost for each performance requirement (i.e., inductance, resistance, SRF, and area). Each individual cost component as shown above is a piece-wise linear function of the error (‘\(E\)’ terms in the equations) for the corresponding requirement that is designed in consultation with the human experts. For example, the experts mentioned that 5% is an acceptable range for error in inductance. That is the reason for 0.05 being the breaking point in the sub-domains in the respective piece-wise function for the inductance cost. The penalty increases faster when the inductance is outside the 5% acceptable range. Similar rules are applied to the rest of parameters.

Due to the inherently spatial nature of the design problem, the state of the drawing is represented as a Boolean image where pixels are true for locations that are covered by an inductor segment and false for locations that are not. We train a Deep Q-Network (DQN) \([10]\) agent to solve this task. DQN takes advantage of Deep Learning (DL) \([3]\), specifically Convolutional Neural network (CNN) architecture \([8]\), in order to learn useful feature representations from the raw image states. DQN follows a conventional algorithm in RL, namely Q-learning \([17]\), to learn the action-values from those learned representations. The action-value function is then used to learn optimal policies for drawing inductors that meet the target specifications.

4.1 Transfer Learning

Once trained, the RL agent described in the previous section can draw inductor layouts that meet a certain, pre-determined target specification. However, such an ad hoc agent is not capable of producing layouts that meet new, moderately tweaked targets. However, due to circuit limitations uncovered throughout the circuit design cycle, the targets need to be tweaked throughout. To address this necessity, we modified the implementation of the RL agent so that it would take less time to produce new candidate VCO inductors when the target is changed during the design process. We do so by expanding the state observation such that it includes the desired target specifications (L, R, and SRF) as input. The respective neural network architecture for these features is a fully connected network.

To facilitate transfer learning for the RL agent, we divide the training into two stages. First, we pre-train the agent on an initial distribution of targets around the reference target. The distribution is centered on the reference target and only covers a small range around it (e.g., 20% above and below the reference target). An agent is trained on targets sampled from this distribution to the full. Then, once a new target is introduced, we fine-tune the trained agent for this new target. We empirically show that fine-tuning an agent that is pre-trained on different (yet close) targets is much faster than training a separate agent from scratch for each new target — see the Results and Discussions section.

5 EXPERIMENTS

5.1 Setup

In our experiments, we used an area of 100 m x 100 m (i.e., canvas) with the input and output ports located at the bottom of the allotted area at 40 m and 60 m respectively (see Figure 1). We fixed the length of the segments that can be drawn such that the ends of each segment land on a 10 m x 10 m grid (i.e., steps in the four cardinal directions had a length of 10 m and diagonal steps had a length of \(\sqrt{2} \times 10 m\)). We also fixed the width of all segments to 5 m and kept all segments on a single metal layer.

Figure 1 illustrates a commonly used expert design for a VCO inductor following the above-mentioned restrictions. With slightly relaxed requirements on resistance and SRF, this design yields a
desired inductor performance of $L = 116.5$ pH, $R \leq 0.925 \Omega$, and $SRF \geq 155$ GHz, at 15 GHz operating frequency. To determine the performance of the generated designs, we used ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) [11], which is an open source simulator for on-chip RF components. Cadence® Virtuoso® [1] and EMX [6, 7] were used for layout and simulation of chosen inductors as an additional validation step to ensure consistent results.

5.2 Results and Discussions

5.2.1 Symmetry. We chose primarily to focus on generating symmetric designs. To validate the claim that we do not lose any performance, we compared the training performance of a DQN agent producing symmetric designs with one using non-symmetric designs. From Figure 3, we can see that while we get some very minor performance gain in terms of the upper bound of return from using non-symmetric designs, it comes at the cost of much longer training time as well as high variance. In contrast, when using symmetric designs, we converge to an optimal design with far fewer interactions with the environment. Figures 4 (a) and (b) illustrate the top 5 layouts for symmetric and non-symmetric settings respectively.

5.2.2 Comparison to Baseline Methods. In this work, we use DQN (RL agent) as the optimization module to design the inductors in a sequential manner. However, there is some precedent to use a one-shot method to produce inductors. Therefore, we compared the results of DQN to that of GA as the optimization module (see Figure 2). Using GA, we optimize a sequence of 15 segments at once to create the inductors, disregarding any trailing segments that come after the segment has reached the output port. The sequence length was chosen to be 15 since it is larger than the length of the top performing designed inductors, giving the algorithm the opportunity to create designs as good as the ones that the RL agent could produce. We also compared our DQN agent with a baseline random agent that generated layouts in the same sequential manner as RL where it selected a random action at each step.

From Figure 5, we can see that DQN and GA significantly outperform the random agent in terms of number of simulations, meaning that they require far fewer queries to the simulator to converge to a good agent that is able to draw inductors meeting the performance requirements. Moreover, although GA achieves higher rewards at first, DQN surpasses GA at higher number of simulations. We can also see that DQN exhibits less variance than GA. Since we desire that our method to consistently produce the best inductor possible for a given specification, the DQN agent is preferred. Figures 4 (c) and (d) illustrates the top 5 layouts generated by the GA and random agents respectively.

Figure 6 illustrates the growth of number of simulations versus steps for all three agents. Although the random agent keeps generating novel inductors as the number of steps increases, it does not improve the achieved rewards as much as GA and DQN (Fig. 5). The GA agent, on the other hand, produces many duplicate inductors, failing to properly explore the space of valid inductors. Part of the reason is that some mutations only happened in the trailing segments after the layout was finished which did not generate new inductors. It explains its smaller mean and standard deviation compared to the other methods. The DQN agent, however, seems to have reached a good balance in terms of exploration of novel inductors and exploitation of the inductors that it has already generated.

Recall that we only send the novel inductors to the simulator for evaluation. We cache the evaluated inductors in order to reduce the time spent in the simulator bottle-neck.

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5.2.3 Transfer Learning. Here, the task is to generate inductors for a new target specification. There are two ways to do this: (i) train from scratch; and (ii) fine-tune a pre-trained model on similar targets (i.e., transfer). To facilitate transfer learning for the RL agent, we divide the training into two stages. First, we pre-train the agent on an initial distribution of targets around the reference target. An agent is trained on targets sampled from this distribution to the full. Then, once a new target is introduced, we fine-tune the trained agent for this new target. Figure 7 illustrates the performance for an agent that is trained from scratch (in blue) and transfer (in orange) and we show the results for when the new target is set to $L = 0.95$ (top) and $L = 1.05$ (bottom). In both cases, we can see that training from scratch to achieve the new target takes much longer to generate a top performing layout than the transferred model.

6 CONCLUSION

We proposed and implemented an Electronic Design Automation (EDA) tool that automates the design of Voltage-Controlled Oscillator (VCO) inductors. This tool can (i) generate several valid VCO inductors designs (a valid design being one which obeys the design constraints and meets the target specifications); and (ii) quickly produce new candidate inductors when the target specifications are moderately tweaked. We formulated the task as a drawing problem and solved it using Reinforcement Learning (RL) as the core optimization technique. We empirically showed that our tool can match or exceed the performance of the simpler human designs.

The current framework is focused solely on the design of VCO inductors, however, it could be more broadly applied to the design of general inductors (e.g., multi-layer architecture). This framework can also be applied to the design of more complex VCO inductors; for instance, to a switchable VCO inductor design involving multiple distinct coils, each drawn in the same manner as we draw a single coil here. These are left to future work.

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