Optimized step-stacked-routing ESD diode and its effects on LNA minimum noise figure

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Abstract. Low capacitance loading is a continuous demand and challenge for ESD device design. In this research, an inter-digital ESD diode realized in TSMC 0.18μm process is optimized and verified. The diode is capable of passing 7kV HBM with 190fF capacitance loading for dual diode protection scheme. Using the novel Step-Stacked-Routing technique, the capacitance is reduced by 18%. The effect on LNA minimum noise figure of this diode is analyzed and simulated with the extracted small signal model.

1. Introduction
High operating frequency and low power is becoming the future of IC industry. This strong demand is driven by mobile computation and communication. When consumers request more functionality on a slim hand-held device, more challenges are posed for IC designers, one of which is ESD protection design. For logic ASIC, higher operating frequency and lower power encourage IC designers to use the most advanced technologies available, namely, narrower length for CMOS. Many methods to increase ESD capability of transistors are proposed [1-3]. Some aim to improve the ESD reliability of the transistors [1], while others strive for better ESD protection devices [2, 3]. However, the driving force on RFIC design to accept advanced technologies may not necessarily be as strong as logic ASIC. Although narrower length transistors will certainly increase the gain-bandwidth frequency and reduce the noise figure, but headroom is normally lower as a result. Furthermore the area shrinkage in RFIC may not be as apparent as that in logic ASIC, since most areas are occupied by passive components in RFIC. Cost will also be higher without a question.

Both logic ASIC and RFIC applications have the same requirement for ESD devices – low capacitance. For logic ASIC, lower capacitance loading can greatly diminish the driving current of the previous stage, which saves power and prolongs battery life. On the other hand, it was suggested the requirement of ESD devices for RFIC to have minimum capacitance and zero resistance [4]. The reason behind it is that LNA should have minimum noise possible. Zero resistance is definitely true since it simply reduces noise. But minimum capacitance is a consequential result when the resistance of the ESD device is fixed. In this article, this study investigates the optimization of a simple inter-digital diode and a novel Step-Stacked-Routing technique, which diminishes the capacitance loading as shown in Figure 1. The ESD diode effect on LNA minimum noise figure is also studied and simulated.
2. Optimization

For an inter-digital ESD diode, as shown in Figure 1, there are a total of 6 variables critical to the ESD performance. These variables are I/O contact columns, power contact columns, I/O fingers, finger length, outer via columns and metal layers. In order to achieve maximum usage of capacitance, a series of optimization tests to determine the influence of each variable are performed. It is clear that increasing the diffusion area will significantly increase the ESD protection capability and the capacitance. Variables that affect diffusion area are I/O contacts columns, I/O fingers and finger length. On the other hand, power contact columns, outer via columns and metal layers used for routing may not increase the capacitance dramatically but they certainly contribute to on ESD capability. The optimization experiments are performed with the variation of a standard diode in both P-type (diodes in N-well) and N-type (diodes in P-sub.) The standard diode shown in Figure 1(a) has two I/O fingers (connected to I/O pads), three power fingers (connected to power lines), one I/O contact row (row of

![Figure 1. Standard inter-digital ESD diode layout (a) top view, (b) side view of regular routing (left) and Step-Stacked-Routing (right)](image)

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![Figure 2. Optimization test results (a) ESD voltage vs. finger length, (b) ESD voltage vs. I/O contact rows, power contact rows and outer via columns (c) ESD voltage vs. finger number, (d) ESD voltage vs. metal layers](image)
I/O finger contacts), one power row (row of power finger contacts), 6μm finger length, two columns of outer vias (columns of vias connected to second metal layer for routing), and one metal layer for diode finger connection. The effect of each variable is tested and the results are given below.

The results show that ESD capability does not necessarily increase linearly with larger diffusion area. Due to the high frequency behavior of ESD event, saturation could be observed from experiment with different diode finger length and contact rows. As the I/O contact rows and finger length was increased, the ESD capability did not increase linearly as shown in Figure 2(a) and Figure 2(b). When this technology was applied, it was obvious that 6μm finger length and three contact rows was an optimal choice before entering saturation zone. For other variables, they seemed to have minor ESD improvement. However, it is beneficial to increase power contact columns and outer via columns as long as the area consumption is acceptable since doing so will not increase the capacitance. Figure 2(c) and Figure 2(d) show that ESD capability was proportional to the increase of fingers, which confirmed early prediction. Increasing the routing metal layer was also very helpful, since the turn-on serial resistance was reduced by using more metal layers. However increasing the routing metal layer will also increase the routing capacitance as well. This triggered the novel Step-Stacked-Routing technique. The detail of this technique is discussed in the following section.

3. Step-Stacked-Routing

It is quite common and intuitive to reduce capacitance through routing technique. One example showed routing technique has been used on bond pads to reduce capacitance [5]. To maintain low turn-on resistance while keeping routing capacitance low, a novel Step-Stacked-Routing technique is proposed. As shown in Figure 1(b), the metal layers are not stacked directly on top of each other, but with a recess for higher stacked layer. With this technique, the routing capacitance can be greatly reduced while the turn-on resistance remained almost unaffected. Based on the optimization discussed in the previous section, the test structure is designed with optimized finger length of 6μm, three rows of I/O contacts, four rows of power contacts, three columns of outer vias and three layers of metal for routing.

From the comparison of regular routing and Step-Stacked-Routing as shown in Figure 3, it can be seen that the ESD capability is almost unaffected. In order to determine the reduction of capacitance, a one-port de-embedding technique is used to extract the real model of ESD diode. The equivalent small signal model of the one port pad and the one port pad photograph are shown in Figure 4. The pad model can be extracted with a dummy pad without diode by converting the measured S-parameter data to Y-parameter. The real diode model can be extracted by measuring dummy pad and pad with diode, and then subtracting Y-parameter of dummy pad from pad with diode. This is called the de-embedding technique. After de-embedding, the diode equivalent small signal model can be represented as shown in Figure 5. Since the difference between regular and Step-Stacked-Routing diodes is the routing capacitance, the capacitance can be extracted through the subtraction of these two Y-parameters. For

![Figure 3](image3.png)  
**Figure 3.** ESD voltage vs. regular routing and Step-Stacked-Routing

![Figure 4](image4.png)  
**Figure 4.** One port pad photograph (left) and small signal model (right)
Y2 representing regular diode Y-parameter and Y1 representing Step-Stacked-Routing diode Y-parameter, the capacitance difference can be expressed as follows:

\[
(Cr2 - Cr1) = \text{imag}(Y2 - Y1) / \sigma 
\]  

(1)

The extracted capacitance difference at different frequency is plotted in Figure 6. As we can observe in the figure, the capacitance reduction is around 19fF to 23fF within the frequency range of 1GHz to 20GHz for both N type and P type diodes. The only difference between N type and P type is their diode. The routing capacitance should be the same for both types, which is consistent with the result where the capacitance differences of both types almost overlap each other.

4. Effects of ESD on Nfmin

Besides low capacitance, it is also critical to keep the voltage drop as low as possible assuming that the classical protection scheme shown in Figure 7 is used. In Figure 8 below/above, I/V curve of ESD diodes with different finger numbers are compared with each other. Although each of the design can pass 2kV HBM, the voltage across the diode is quite different. Compromise between capacitance loading and voltage drop must be made. However another issue of noise figure consideration emerges for RF applications, especially LNA input protection. Considering a very simplified commonly used, inductively source degenerated common source amplifier shown in Figure 9, the only two noise sources are channel current noise in the nMOS and the thermal noise generated by the resistance in ESD diode. Since the routing capacitance in the ESD diode can be absorbed into the matching network, its effect is ignored in the analysis. Referring all the noise contribution to the drain noise current (id\text{drain}) at the nMOS, the noise current can be expressed as follows:

Figure 5. Diode equivalent small signal model

Figure 6. Extracted capacitance difference of regular routing and Step-Stacked-Routing

Figure 7. Classical dual diode ESD protection scheme

Figure 8. I/V curve of ESD diodes with different I/O finger numbers
Where \( g_{ds} \) is the transconductance of source-drain at \( V_{DS} = 0 \), \( k \) is Plank constant, \( T \) is absolute temperature, and \( \gamma \) is channel length correction coefficient (2/3 for long channel). It is clear from equation (2) that if we want to reduce the overall drain noise current, the diode resistance and capacitance must be reduced. This derivation is equivalent to the two port minimum noise figure representation depicted in [6]. After elaboration, the expression for minimum noise figure \( (F_{\text{min}}) \) is given:

\[
F_{\text{min}} = 1 + 2R_n(G_{\text{opt}} + G_c)
\]

\[
R_n = \frac{id}{4kTgm|Z|}
\]

\[
G_c = \left( \frac{1}{|Z|} + \frac{R_d}{R_d^2 - 1/C_d^2 \sigma^2} \right)
\]

\[
G_{\text{opt}} = \left( \frac{R_d}{R_d^2 - 1/C_d^2 \sigma^2} \right) \left( \frac{1}{|Z|^2} + \frac{R_d gm|Z|V_{nz}}{(R_d^2 - 1/C_d^2 \sigma^2) id} \right)
\]

\[
G_m = \frac{R_d V_{nz}}{4kT(R_d^2 - 1/C_d^2 \sigma^2)}
\]

\[
|Z| = \frac{L_s}{C_{gs}} - L_d \sigma^2
\]

Equation (6) suggests the same tendency of reducing the diode resistance and capacitance.

A cascode, inductively source degenerated, single-ended common source LNA, the schematic shown in Figure 10, is simulated with the extracted ESD diode model. The parametric analysis shows the minimum noise figure decreases with the diode resistance and capacitance as shown in Figure 11. Another simulation shows the routing capacitance has no effect on minimum noise figure at all. Other
than target ESD capability, the choice of ESD device for LNA is dominated by its resistance and capacitance. Sometimes the lowest capacitance loading ESD device is not necessarily the best choice for minimizing noise figure since it normally entails higher resistance. However, choosing the highest capacitance loading available may not result in the lowest minimum noise figure, since the minimum noise figure matching point may be far away from acceptable return loss. It may be the best choice to consider the ESD device as part of the LNA circuit and to make some compromise among gain, return loss and noise figure.

5. Conclusions
In this study, an optimized ESD diode with novel Step-Stacked-Routing aimed to further reduce capacitance loading is proposed. When tested, the ESD diode is able to pass 7kV HBM with 190fF capacitance loading for dual diode protection scheme. The novel routing technique is verified to be able to reduce around 18% total capacitance. Analysis and simulation is also discussed in this article. The minimum noise figure for LNA design should incorporate the ESD device as part of the circuit and make compromise among gain, return loss and noise figure at the same time. The ESD voltage in this article is calculated according to the TLP test with Barth Pulse Curve Tracer, Model 4002 TLP. The RF measurement is performed with HP8510C, and SOLT calibration is used with Cascade ACP100 probes.

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Figure 11. Simulated NFmin for (a) NFmin vs. Cd, (b) NFmin vs. Rd