TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2013, 23–27 SEPTEMBER 2013, PERUGIA, ITALY

Hybrid circuit prototypes for the CMS Tracker upgrade front-end electronics

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ABSTRACT: New high-density interconnect hybrid circuits are under development for the CMS tracker modules at the HL-LHC. These hybrids will provide module connectivity between flip-chip front-end ASICs, strip sensors and a service board for the data transmission and powering. Rigid organic-based substrate prototypes and also a flexible hybrid design have been built, containing up to eight front-end flip chip ASICs. A description of the function of the hybrid circuit in the tracker, the first prototype designs, results of some electrical and mechanical properties from the prototypes, and examples of the integration of the hybrids into detector modules are presented.

KEYWORDS: Detector design and construction technologies and materials; Front-end electronics for detector readout

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1 The CMS tracker upgrade for the HL-LHC

The increased luminosity planned for the High Luminosity LHC (HL-LHC) requires a major upgrade of the CMS tracker detector in order to cope with the new physics requirements and radiation tolerance constraints. The upgrade will require new modules that feature higher granularity and lower mass, as well as the ability to correlate locally the signals from two silicon sensors, enabling the rejection of low momentum tracks, and introducing at the same time a new level 1 (L1) track-triggering functionality to reduce the L1 trigger rate [1, 3].

The new front-end ASICs that are being developed for these new modules adopt flip-chip technology, replacing the traditional wire bonding connectivity to the printed circuit board (PCB) substrate. This will bring significant advantages in terms of size reduction of the front-end systems, but it imposes the use of high-density connectivity and signal routing on the PCBs. This paper presents the module types being considered today for the CMS tracker upgrade, focusing specifically on the outer barrel module design that uses the CBC ASIC [4]. The high-density connectivity requirements for the front-end ASIC are shown for both rigid and flexible substrate materials.

2 Tracker module types

The upgrade configuration for CMS tracker uses a barrel and endcap geometry, with different module types for the inner and outer regions (figure 1). The outer tracker modules shown in red are based on a pair of strip sensors and are called “2S” for strip-strip. The inner tracker modules shown in blue are based on one strip sensor and one pixel sensor and are called “PS” for pixel-strip.
The 2S modules are based on two overlaying strip sensors with parallel strips, with a sensor separation in the range from 1 to 4 mm depending on their radial position. A central service hybrid PCB provides the GBT optical link interface [5] and a power converter to supply the readout chips (figure 1).

The sensors contains 1016 strips with 90 $\mu$m pitch and strip length of 50 mm on both left and right hand sides, resulting in a sensor area of about $10 \times 10$ cm$^2$. Each read-out hybrid PCB will collect the strip signals from the nearby half of each of the upper and lower sensor by means of wire bonds between the sensor and hybrid PCB. This implies wire bond pads on the hybrid PCB on both the top and bottom sides (figure 10, figure 12). The strip signals are then processed by eight front-end readout ASICs. The front-end chips store the raw strip data into a memory buffer for retrieval upon receipt of a level 1 trigger readout request, and at the same time identify hits compatible with high transverse momentum tracks (stubs) which are forwarded synchronously to the back-end to contribute to the L1 trigger decision (figure 2) [2, 3]. This digital information (stubs and level 1 triggered data) is collected by a concentrator chip that interfaces to the GBT transmitter.

The PS modules will provide additional Z-axis information for the track triggering functionality [2, 3]. To achieve this the pair of sensors comprises a silicon strip sensor on the outer side with 25mm
long strips on 100\,\mu m pitch, resulting in a sensor area of about 5 \times 10 \, cm^2, coupled to a pixelated strip sensor on the bottom side (figure 3). Each pixel from the pixelated strip sensor is 1.5 \, mm long with pitch of 100 \, \mu m. The pixelated strip sensor is bump bonded to sixteen Macro-Pixel readout ASICs (MPA), each covering an array of 120 \times 16 macro-pixels.

The strip sensor signals are connected via wire bonds to two hybrid circuits on the left and right hand sides, and are read out by a simplified version of the 2S module front-end ASIC that will perform signal amplification and discrimination. The resulting binary signals from every strip are pushed to the macro-pixel readout ASICs on the pixelated strip sensor side: the macro pixel ASIC will perform the stub identification and transmission to the back-end level 1 trigger processing, whose decision is fed back to the front-end for extracting the raw strip and macro pixels data.

Both modules rely on flip-chip connectivity, however since the PS module covers half the area of the 2S modules, the service hybrid will have to be split in two pieces: one will provide the powering circuitry with its DC-DC converter, while the other will host the GBT circuitry and its corresponding optical module.

The results presented in this paper relates to the hybrid for the 2S module, which has been the focus of R&D activities so far.

3 \hspace{1em} \textbf{Flip-chip connectivity}

The 2S module electronics is based on the CBC2 (CMS Binary Chip), a full-scale prototype front-end readout ASIC which has been used for the development of the first 2S hybrids and to investigate the flip-chip interconnection [4]. The CBC2 pads are designed for C4 flip-chip bonding with a

\begin{figure}[h]
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\includegraphics[width=\textwidth]{fig3.png}
\caption{2S module readout architecture.}
\end{figure}

\begin{figure}[h]
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\includegraphics[width=\textwidth]{fig4.png}
\caption{Inner barrel strip and pixelated strip sensor module (PS).}
\end{figure}
250µm pitch. This technology was chosen to exploit low-risk commercial assembly for the large-scale production of the modules and to remove the need for pitch-adapting wire bonding. The bumped connection provides a less inductive path, which is of particular interest for the power distribution into the ASIC. The functionality of the assembled hybrids can also be fully tested without any wire bonding operation.

The CBC2 flip chip contains 771 C4 bumps made of Pb97Sn3 high lead material, for a total area of $11.025 \times 4.725 \text{mm}^2$. Figure 4 shows the footprint of the CBC2: the inputs pads are located on the first six rows of the die, this enables an optimal routing to the sensor wire bond pads using only two routing layers with minimum-separation tracks. Digital I/Os are confined to the opposite side of the ASIC to avoid noise injection. The two remaining sides contain the inter-chip communication lines, to allow the identification of stubs crossing two adjacent chip boundaries. The last row of pads on the back-end of the chip is reserved for probing the wafer without damaging the bumps. The central area of the chip and all the other unreserved pads are used for grounding.

Flip-chip connectivity translates into high-density interconnection requirements for the design of the printed circuit board. The copper pad that will receive the bump from the chip on the hybrid should ideally be of the same diameter as the under bump metallization (UBM) pad on the chip. The C4 bumps of the CBC2 ASIC have an outer diameter of 146 µm sitting on an UBM of 125 µm. The mating pad can be defined by the pad width itself, in which case the soldermask protection is completely removed (accounting for its alignment tolerance), or it can be soldermask-defined, so that the metal pad diameter is increased by twice the soldermask alignment tolerance and then covered by soldermask (figure 5). This latter implementation is the preferred one in the industry because it provides a self-aligning array for the placement of the chip, and provides better mechanical adhesion of the bump pad on the printed circuit.

The minimum separation and width for tracks in the rigid and flex technologies allow for only two tracks to be routed on the same layer between the pads. For non-peripheral pads across the chip footprint it is therefore necessary to use additional internal layers and vias. Regular pin escapes
are located in the center between four flip chip pads: typical drill diameters as small as 50 \( \mu \text{m} \) are used on pad apertures of a diameter as small as 110 \( \mu \text{m} \) (figure 6, figure 7). In some cases the flip chip pad diameter is too large and then the via-in-pad structure is used: the flip chip landing pad is drilled in its center and copper filled, so that the connection is made directly to the inner layer from the pad (figure 7). Different manufacturers will recommend one option or the other depending on their preferred technology.

The microvias required to escape the flip-chip array are laser-drilled between two adjacent layers. Hence the manufacturing of the hybrid circuit is produced sequentially: a central core structure is first produced, using regular mechanically-drilled vias and with standard width and spacing rules, after which additional layers are added on the top and bottom sides, carrying this time much narrower tracks and the laser-drilled vias. Additional layers can be added afterwards, always using laser microvias and tracks’ width and spacing as narrow as 25 \( \mu \text{m} \), to form a hybrid circuit construction known as build-up substrate (figure 8).

A typical cross section of a 6 layers rigid substrate produced to test the CBC2 chips is shown (figure 8), representing the flip chip pad and its solder material before assembly, the neighboring microvias of the pin escape structure, and an internal mechanical drill through the liquid crystal polymer (LCP) core.

The other critical interconnecting area is located on the sensor wire bonding arrays (figure 9). The strips’ pads are wire bonded to the hybrid circuit, matching the 90 \( \mu \text{m} \) pitch on the sensor. To accommodate the aluminum wire bond foot, the sensor pads were arranged in two rows with a pitch of 180 \( \mu \text{m} \) and with a pad width of 80 \( \mu \text{m} \), leaving a gap of 100 \( \mu \text{m} \) to route the connecting track in between. Hence, tracks width and spacing rules as low as 33 \( \mu \text{m} \) are required at this level.

High density interconnection technologies with track widths and spacing rules as low as 25 \( \mu \text{m} \), using microvias down to 30 \( \mu \text{m} \) of diameter on multilayer build-up structures are today available on rigid materials but also on flexible polyimide products. These are commonly used...
for today’s consumer electronics that require a high packaging density [6]. The same technology can be exploited for the development of new low mass and high-density hybrid circuits for physics experiments.

4 Rigid hybrids

Rigid build-up high-density interconnecting substrates have been used by the electronics packaging industry for many years [6]. This solution was selected to develop the first prototype for testing the CBC2 front-end ASIC (figure 11). The prototype featured two CBC2 chips [4], to enable the inter-chip links to be tested, and can be also connected to two strip sensors in a “mini” 2S module setup representative of the 2S module final application. The substrate design (figure 8) is made of a four-layer core made of a LCP central dielectric and two FR4 resin laminate external layers. Two additional copper layers were added for the high-density connections, resulting in a total thickness of 265 µm. The prototype also features a test connector to provide input signals for bench testing.

The prototype circuit was successfully tested in May 2013 [4]; after which the bonding of two strip sensors to the module highlighted some assembly difficulties. The small thickness of the rigid
material makes it insufficiently stiff for wire bonding the sensor without supporting the substrate from the opposite side directly behind the bond pads. To remedy this problem, the bottom sensor bond pad array should be offset from the top one, such that the opposite side of the substrate can always be supported during the wire bonding. The offset will result in longer wires for one of the sensors (figure 10). It should also be noted that the wires need to bridge the vertical gap that results from the sensors separation of up to 4 mm. Large height differences in the ends of bond wires typically result in reduced reliability.

The thermal expansion coefficient (CTE) of the rigid substrate is typically around 17 ppm/°C, mismatching the CTE of silicon (3 ppm/C) and also of the underfill material (typically around 10 ppm/C). This can result in board warpage after its reflow or underfilling process, as observed on a rigid hybrid mechanical sample prototype containing eight dummy ASICs (figure 11).

The prototype connected to two sensors was successfully tested with an Sr90 source [4].

5 Flexible hybrids

Flexible circuits based on polyimide offer an alternative integration option for the 2S module assembly. This technology is today offering high density connecting capabilities, mostly used for medical devices and high-end consumer electronics; it has also already found applications in physics front-end systems [7]. Carbon fiber stiffeners can be used to reinforce the areas requiring wire bonding and component assembly, providing at the same time a good cooling path for heat generated by the CBC2 chips (figure 12).

Moreover, the inclusion of stiffeners could provide a solution for the wiring of the sensors to the hybrid: an arrangement like the one presented in figure 12, but with the flexible hybrid folded around thicker stiffeners, would require shorter wire bonds and would remove the need to offset the two sets of pads on the hybrid, possibly resulting in a narrower design if the front end chips can

![Figure 11. Dual-CBC2 rigid substrate prototype.](image)
be brought closer to the sensors. Still, in some cases, the flexible circuit needs to be sharply folded on the sensor side with a radius as small as 0.5 mm.

At the moment of writing, a four-layer prototype, 145 $\mu$m thick, is in production featuring the full 2S hybrid geometry, with a size of $125 \times 20$ mm$^2$ and with an extension test connector for laboratory tests (figure 15). This circuit uses a via-in-pad flip chip array, with soldermask-defined pads and tracks of 30 $\mu$m. The laser microvias have a drill diameter of 25 $\mu$m.
6 Cooling

The integration of the hybrid circuits into full modules is driven by thermal constraints: the heat emitted by the sensors and by the hybrids needs to be extracted to keep the module elements at the allowable working temperature. The module integration and corresponding thermal studies were made on the basis of the flexible hybrids option (figure 16).

The two sensors are supported by two bridges made of Aluminum-Carbon Fiber composite that provides the thermal conductivity of Aluminum close to 230 W/m.K together with the carbon fiber thermal expansion coefficient of 4 ppm/°C and a Young modulus (for stiffness) of almost 100 GPa. The heat of the sensors is collected at the edges of these thermal bridges by means of two cooling pipes that circulate a CO\textsubscript{2} fluid at -28°C, maintaining the sensors temperature around -20 degrees with a temperature gradient of 3.5°C for all the sensors surface.

The flexible hybrids are reinforced by carbon fiber stiffeners that bring stiffness and a low thermal expansion coefficient. These stiffeners carry the heat to Al-C composite standoffs directly linked to the cooling pipe circuit. The service board is assembled in a similar way, with an additional Al-C support in the center.

Thermal simulations have been performed for the sensors; similar studies will be made in the near future for the front-end and service hybrids.

7 Conclusion

CMS is considering today two types of modules for the high-luminosity upgrade of the strip tracker: a strip-strip module using the CMS Binary Chip as front-end readout, and a strip-pixelated strip module that will use a strip readout chip and a macro-pixel readout chip. Both modules use flip-chip technology that requires substrates with high-density interconnection capabilities. Rigid and flexible substrates are both suitable for the CMS tracker application.

Prototypes using the CBC2 front-end ASIC for the 2S modules development have been tested and are currently in production. Regarding the rigid substrate technology, the flip-chip assembly appeared to be functional, however technical difficulties were identified for the module assembly, in particular for the wire bonding constraints and thermal expansion mismatches. A flexible prototype
matching the final size of the 2S module hybrid is now in production: despite requiring the addition of stiffeners it has clear advantages in terms of ease of assembly and cooling performance.

Future developments will see the production of the new flexible prototype and further experience with the ongoing assembly activities with the rigid hybrids for the 2S module, but also for the PS modules hybrids, with the aim to identify and consolidate a technology of choice for the CMS tracker upgrade.

References

[1] D. Abbaneo, Upgrade of the CMS Tracker with tracking trigger, 2011 JINST 6 C12065.
[2] N. Pozzobon, Development of a Level 1 Track Trigger for the CMS Experiment at the High-Luminosity LHC, Nucl. Instrum. Meth. A732 (2013) 151.
[3] D. Abbaneo and A. Marchioro, A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC, 2009 JINST 7 C09001.
[4] D. Braga et al., Characterization of the CBC2 readout ASIC for the CMS strip-tracker high-luminosity upgrade, in Topical Workshop on Electronics for Particle Physics 2013, September 23–27, Perugia, Italy (2013).
[5] D. Felici, A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments, in Topical Workshop on Electronics for Particle Physics 2013, September 23–27, Perugia, Italy (2013).
[6] K. Yamanaka et al., Materials, processes, and performance of high-wiring density buildup substrate with ultralow-coefficient of thermal expansion, IEEE T. Compon. Pack. T. 33 (2010) 453.
[7] M. Friedl et al., The Belle II Silicon Vertex detector, Phys. Procedia 37 (2012) 867.