Article

PWM Strategy to Alleviate Common-Mode Voltage with Minimized Output Harmonic Distortion for Five-Level Cascaded H-Bridge Converters

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Abstract: High-frequency components of common-mode voltage (CMV) induce the shaft voltage and bearing current, which lead to premature failures in motors. In addition, due to non-zero average CMV, the low-frequency components of CMV, particularly the third-order harmonic component, have been reported to cause difficulties in common-mode filter design. Furthermore, the utilization of distant voltage vectors in the pulse-width modulation (PWM) with reduced CMV magnitudes gives rise to high output harmonic distortion compared to PWM ones without CMV reduction. In an attempt to solve the aforementioned issues, this article presents a PWM strategy that features reduced CMV magnitudes, zero average CMV, and improved output harmonic distortion for a five-level cascaded H-bridge (CHB) converter. In addition, the carrier rotation technique based on the phase-leg redundancy of the CHB topology is also combined with the proposed scheme to achieve equal power loss distribution among power switching devices. Both simulation and experimental results confirm that the proposed strategy produces better output harmonic distortion than that of POD-SPWM and APOD-SPWM under the condition of reduced CMV magnitudes, zero average CMV, and equal power loss distribution.

Keywords: common-mode voltage; pulse-width modulation; harmonic distortion; cascaded H-bridge converter; zero average CMV

1. Introduction

Multilevel converters have found themselves in many industrial motor-drive applications. Several advantages, when compared to two-level ones, include lower harmonic distortion, higher blocking voltage, a more significant number of redundant switching states, lower electromagnetic interference (EMI), and lower dv/dt [1]. Some prominent multilevel converter topologies are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) converters. Among them, CHB converter topologies have been widely used in industrial applications, especially for the number of levels being greater than or equal to 5 (n ≥ 5). Aside from inheriting all the strengths of multilevel converters, they also possess some other merits such as a modular structure [2], a smaller number of switching devices as opposed to NPC converter topologies for the same number of levels [3]. With regard to the DC-link voltage levels among different cells in the same phase leg, the CHB converters can be classified as asymmetric and symmetric ones. The asymmetric CHB topologies aim at reducing the number of isolated DC-link voltages...
required for a given number of voltage levels [4]. The ratio of DC-link voltage levels among different cells in the same phase leg can be binary [5] or trinary [6]. In the binary asymmetric CHB topology [5], the research work further reduces the number of isolated DC-link voltages in a phase leg to one while the remaining DC-link voltages of other cells in the same phase leg are floating and are balanced by a technique called level doubling network. Similarly, the work in [6] proposed a modulation scheme for a trinary asymmetric CHB topology to balance the floating capacitor voltages of the remaining cells by utilizing the redundancies available in the trinary space vector diagram. In general, the unequal DC-link voltages in the asymmetric CHB topologies lead to complicated modulation schemes and uneven power-sharing among different cells. On the contrary, the power loss balance among switching devices can be achieved thanks to phase-leg redundancy in the symmetric CHB converters. This unique feature in the symmetric CHB converters manifests itself in the form of carrier rotation in which numerous research works [7–10] have utilized to equally distribute power loss among switching devices for a whole modulation range. The underlying principle of the carrier rotation is to rotate the carrier in a cyclic manner, which could be a fundamental modulating cycle [7], a full carrier cycle [8], a half carrier cycle [9], or a quarter of carrier cycle [10]. The choice of carrier-rotation cycle depends upon the modulation schemes and the total time required to achieve power balance [9,10]. In contrast, due to the lack of phase-leg redundancy of an NPC converter, the power loss balance cannot be realized, thereby reducing its reliability in the long run [11]. Moreover, the DC-link capacitor voltage balancing control in the NPC converter is relatively complex for five levels or above (n ≥ 5), rendering it unattractive for industrial applications as opposed to the CHB counterpart. The research work in [12] proposed a carrier-overlapped PWM for neutral-point (NP) voltage balancing in a five-level NPC inverter. Despite successfully balancing the NP voltage in a five-level NPC converter, the total harmonic distortion given by the proposed strategy is even inferior to that of the three-level NPC inverter for the modulation range of m ≥ 0.6 while using twice the number of switching devices in comparison to the three-level NPC one. The research work in [13] extends the one in [12] for n-level NPC inverters. However, the proposed scheme was applied to a five-level NPC inverter in both simulation and experiment, and the output harmonic distortion is once again higher than that of a three-level NPC one for m ≥ 0.6, albeit being capable of balancing the NP voltage.

Despite having the merits mentioned above, CMV still occurs in CHB converters. Large magnitudes and high-frequency components of CMV give rise to shaft voltage and bearing current, thereby leading to premature failures in motors as indicated in [14]. Moreover, in medium-voltage motor-drive applications, high CMV magnitude leads to the destruction of motor insulation [15]. Hence, the magnitude of which must be reduced. Aside from the high-frequency components of CMV, its low-frequency components, especially the third-order harmonic component of CMV, have been reported to cause difficulties in filter design, as well as heated CM inductors as reported in [16]. In an attempt to solve this problem, the zero-average CMV in a sampling period is, therefore, introduced in [16] to suppress the third-order harmonic component of CMV in a two-level converter. In practice, long cables, connected between the converter and the motor, would exacerbate undesired phenomena associated with CMV, as previously mentioned [17]. Therefore, CMV magnitude reduction and zero average CMV in one sampling period must be ensured.

In terms of solutions for CMV reduction, they can be classified as hardware and software solutions. On the hardware front, the research work in [18] proposed a CM filter to attenuate the conducted EMI generated by CMV. In [19], the researchers proposed a passive EMI filter for eliminating bearing current and ground leakage current. In [20], an integrated AC choke, which combines a common-mode and a differential-mode filter, was presented to suppress the adverse effects caused by CMV. However, the hardware solutions increase the cost and volume of a system. On the contrary, software methods only
involve modifying PWM strategies. Hence, they are more preferred over the hardware ones.

From the perspective of CMV alleviation, PWM methods can be classified as fully-eliminated-CMV PWM, partially-eliminated-CMV PWM, and non-eliminated-CMV strategies. Under the fully-eliminated-CMV PWM schemes, CMV can be theoretically eliminated to zero by avoiding all switching states that generate CMV magnitudes. Due to having no zero-CMV-magnitude vectors in the two-level space-vector diagram, the complete CMV elimination cannot be achieved in a conventional two-level converter [21] and is only feasible for odd n-level converters. As a result, the research work in [22] proposed a fully-eliminated-CMV strategy in conjunction with switching loss reduction under different power factor conditions for odd n-level converters. The switching loss reduction is realized based on the redundancies of implementation of zero-CMV switching sequences in a carrier period, in which the sequence with double switching commutations is assigned to one of the three phases with maximum absolute current magnitude. However, the total harmonic distortion of the proposed strategy in [22] is significantly higher than that of in-phase disposition sinusoidal PWM (IPD-SPWM) due to the use of distant zero-CMV vectors. The fully-eliminated-CMV scheme proposed in [23] aims to solve the deficiency of high harmonic distortion in [22] by once again utilizing the redundancies of implementation of zero-CMV switching sequences. The analytical harmonic distortion factor then determines which redundancy that leads to minimum harmonic distortion. The research work in [24] further improves the harmonic distortion produced in [23] by modifying the switching sequence in a carrier period. In [25], a marginal improvement of harmonic distortion is observed for a fully-eliminated-CMV PWM strategy with the use of a sawtooth carrier over the one in [24]. Even though the CMV magnitude is theoretically eliminated to zero, the CMV spike still occurs due to the deadtime effect. As a result, the work in [26] was presented to reduce the CMV spike. Nevertheless, the CMV spike is reduced at the expense of high switching loss. Although significant efforts have been made to reduce the harmonic distortion and switching loss in the fully-eliminated-CMV PWM strategies, both harmonic distortion and switching loss are still significantly higher than those of partially-eliminated-CMV PWM and non-eliminated-CMV PWM ones [27], thereby raising the torque pulsation in motors and reducing the overall efficiency of a system. The partially-eliminated-CMV schemes offer a nice balance among the CMV magnitude reduction, the THD of outputs, and the switching loss by neglecting switching states that generate high CMV magnitudes. In the conventional two-level converters, owing to the nonexistence of zero-CMV voltage vectors, significant attention has been paid to reduce the CMV magnitudes by avoiding the two zero voltage vectors. Several PWM strategies include remote state PWM (RSPWM) [28], active zero-state PWM (AZPWM) [29], and near state PWM (NSPWM) [30]. A comparative analysis of harmonic distortion for the above-mentioned PWM strategies is included in [31]. As demonstrated in [31], a common drawback of these strategies is the deteriorated output quality compared to the non-eliminated-CMV strategy such as SPWM. Therefore, the demand for both CMV-magnitude reduction and improved output quality gives rise to the adoption of multilevel converters. Owing to the complex control of NP voltage balancing for n ≥ 5 and uneven power loss distribution in an NPC converter, a CHB converter topology is generally preferred.

The partially-eliminated-CMV PWM strategy typically used in a CHB converter is phase opposition disposition SPWM (POD-SPWM), whereas the non-eliminated-CMV-PWM ones are IPD-SPWM and alternate phase opposition disposition SPWM (APOD-SPWM). Regarding the output quality, as demonstrated in [32], IPD-SPWM produces the best output harmonic distortion performance compared to APOD-SPWM and POD-SPWM due to the use of three nearest vectors. Unfortunately, the CMV magnitude given by IPD-SPWM is twice as high as that of POD-SPWM. Although the CMV magnitude reduction is achieved in POD-SPWM, its total harmonic distortion is noticeably higher than IPD-SPWM, as indicated in [32].
As a result, this article presents a PWM strategy with reduced CMV magnitude and zero average CMV in conjunction with minimized output harmonic distortion for a five-level CHB converter. The key contributions of the article include:

1. A PWM strategy featuring reduced CMV magnitudes, zero average CMV, and minimum output harmonic distortion is extended from a three-level NPC [33] to a five-level CHB converter;
2. A carrier-rotation technique [7] is combined with the proposed scheme for even power loss distribution in a five-level CHB converter, thereby enhancing the efficiency and reliability over the long term compared to a five-level NPC one;
3. A power loss analysis conducted in a PLECS thermal module is presented to confirm the even distribution of power loss, and to establish the condition of equivalent switching loss power under which the harmonic distortion of different PWM strategies is fairly compared against one another;
4. A detailed comparative analysis of output harmonic distortion on the basis of comparable switching loss power is conducted in both simulation and experiment for the proposed strategy, POD-SPWM, APOD-SPWM, and IPD-SPWM.

Finally, the article is organized as follows: Section 2.1 presents a mathematical model of a five-level CHB converter for a seamless extension of the proposed PWM strategy. Section 2.2 further enhances the performance of the proposed one by employing the carrier-rotation technique unique to a CHB topology for even power loss distribution. Section 3 illustrates some fundamental performance criteria for evaluating any PWM strategy, such as power loss (conduction and switching loss), total harmonic distortion, weighted total harmonic distortion, and RMS value of phase current ripple. Section 4 details a comparative analysis of output harmonic distortion, CMV magnitudes, and power loss in the simulation for the proposed one, POD-SPWM, APOD-SPWM, and IPD-SPWM. Section 5 demonstrates a comparative analysis of harmonic distortion in the experiment for the strategies mentioned above. Section 6 includes key remarks on the performance of the proposed scheme over POD-SPWM, APOD-SPWM, and IPD-SPWM.

2. PWM Strategy to Alleviate CMV with Improved Output Harmonic Distortion and Equal Loss Distribution

2.1. With CMV Alleviation and Improved Output Harmonic Distortion

This section presents a PWM method for CMV alleviation, which can be achieved by reducing CMV magnitudes and maintaining zero average CMV in one sampling period. In addition, the output harmonic distortion is also minimized, thereby enhancing the overall efficiency of a system.

The PWM strategy for a 5-level CHB converter is derived based upon the equal DC-link voltage condition, which can be obtained by multi-pulse diode rectifiers [1]. Hence, the instantaneous pole voltages of phase leg A \( V_{A0} \), phase leg B \( V_{B0} \), and phase leg C \( V_{C0} \) as shown in Figure 1a can be expressed as:

\[
V_{A0} = (S_{1A} + S_{2A} + S_{3A} + S_{4A}) \times V_{dc} - 2V_{dc} \quad (1)
\]

\[
V_{B0} = (S_{1B} + S_{2B} + S_{3B} + S_{4B}) \times V_{dc} - 2V_{dc} \quad (2)
\]

\[
V_{C0} = (S_{1C} + S_{2C} + S_{3C} + S_{4C}) \times V_{dc} - 2V_{dc} \quad (3)
\]

where \( S_{ix}, i \in \{1,2,3,4\} x \in \{A,B,C\} \) is regarded as a switching state of SWix, which assumes a value of 0 or 1.

The virtual instantaneous normalized switching voltage of phase leg A \( V_{AN} \), phase leg B \( V_{BN} \), and phase leg C \( V_{CN} \) can then be written as:

\[
V_{AN} = (S_{1A} + S_{2A} + S_{3A} + S_{4A}), 0 \leq V_{AN} \leq 4 \quad (4)
\]

\[
V_{BN} = (S_{1B} + S_{2B} + S_{3B} + S_{4B}), 0 \leq V_{BN} \leq 4 \quad (5)
\]
\[ V_{CN} = (S_{1C} + S_{2C} + S_{3C} + S_{4C}), 0 \leq V_{CN} \leq 4 \]  \quad (6)

As for 5-level NPC converters, there is a restriction over the switching states constituting the normalized switching voltage \( V_{xN} \), i.e., \( S_{1x} \leq S_{2x} \leq S_{3x} \leq S_{4x} \) [22]. However, there is no such restriction in 5-level CHB converters. This characteristic is referred to as phase-leg redundancy on which the carrier-rotation techniques [7–10] are based to distribute the power loss among switching devices equally.

The instantaneous normalized switching voltage of phase leg A \( (V_{AN}) \) in (4), phase leg B \( (V_{BN}) \) in (5), and phase leg C \( (V_{CN}) \) in (6) can be decoupled into 2 components.

\[ V_{AN} = s_A + L_A \]  \quad (7)
\[ V_{BN} = s_B + L_B \]  \quad (8)
\[ V_{CN} = s_C + L_C \]  \quad (9)

where \( s_x \) is the active switching state of phase leg \( x \in \{A, B, C\} \) which takes a value of 0 or 1. \( L_x \) is the base voltage of phase leg \( x \in \{A, B, C\} \).

The instantaneous CMV can be defined as [22–26]:

\[ V_{CM} = \frac{(V_{AN} + V_{BN} + V_{CN})}{3} = \frac{(V_{AN} + V_{BN} + V_{CN} - 6V_{dc})}{3} \]  \quad (10)
The average value of $V_{AN}$, $V_{BN}$, $V_{CN}$ in one sampling period can be written as:

$$\overline{V_{AN}} = v'_{\text{Aref}} = v_{\text{Aref}} + v_{\text{off}} = \xi_A + L_A$$

(11)

$$\overline{V_{BN}} = v'_{\text{Bref}} = v_{\text{Bref}} + v_{\text{off}} = \xi_B + L_B$$

(12)

$$\overline{V_{CN}} = v'_{\text{Cref}} = v_{\text{Cref}} + v_{\text{off}} = \xi_C + L_C$$

(13)

where $v'_{\text{xref}}$ is the reference voltage signal of phase $x \in \{A, B, C\}$.

$v_{\text{off}}$ is the offset voltage.

$\xi_x$ is the average active switching state of phase $x \in \{A, B, C\}$.

$L_x$ is the base voltage of phase $x \in \{A, B, C\}$ and $\text{Int}(v'_{\text{xref}})$ returns the smallest integer value of $v'_{\text{xref}}$.

For ease of understanding, the instantaneous, and average voltage models of three-phase legs are illustrated in Figure 2.

The average CMV in one sampling period can be then written as:

$$\overline{V_{CM}} = v_{\text{CM}} = \frac{(v_{\text{A0}} + v_{\text{B0}} + v_{\text{C0}})}{3} = \frac{(v_{\text{Aref}} + v_{\text{Bref}} + v_{\text{Cref}} + 3v_{\text{off}} - 6v_{\text{dc}})}{3}$$

(17)

The three-phase reference voltage signals in (5) can be expressed as:

$$v_{\text{Aref}} = \frac{2m}{\sqrt{3}} \times \cos(\omega t)$$

(18)

$$v_{\text{Bref}} = \frac{2m}{\sqrt{3}} \times \cos(\omega t - 2\pi/3)$$

(19)

$$v_{\text{Cref}} = \frac{2m}{\sqrt{3}} \times \cos(\omega t - 4\pi/3)$$

(20)

The condition of zero average CMV dictates the limit of linear modulation region, i.e., $0 \leq m \leq \sqrt{3}/2$. This condition also leads to $v_{\text{off}}$ in (17) being equal to 2.

Let us define $F_T$, $F_e$, and $F_L$ as total switching voltage, total average active switching voltage, and total base voltage, respectively.

$$F_T = F_e + F_L$$

(21)

$$F_e = \xi_A + \xi_B + \xi_C$$

(22)

$$F_L = L_A + L_B + L_C$$

(23)
The zero average CMV in one sampling period results in $F_I = 6$ in (21). Figure 1b shows that the red-line hexagon is the region where the average CMV is zero. This region consists of six sub-regions corresponding to two cases of $F_L = 4$ and $F_L = 5$, as shown in Figure 3. The reference vector $\mathbf{v}_{ref}$ in the five-level space vector diagram can be synthesized by $\mathbf{ξ}_{ref}$ in the two-level one with the aid of the base voltage vector $L$, as illustrated in Figure 1b. Under the condition of zero average CMV and reduced CMV magnitude, three possible switching sequences can be used to synthesize $\mathbf{ξ}_{ref}$, as shown in Figure 3b, for $F_L = 4$ and $\mathbf{ξ}_{ref}$ in the area (1). Among these, there is only one switching sequence that yields the best output harmonic distortion, i.e., $011 \rightarrow 111 \rightarrow 110 \rightarrow 100 \rightarrow 110 \rightarrow 111 \rightarrow 011$ [33]. The dwell time calculation of which is also shown in Figure 4b, along with the flowchart featuring switching sequences for the areas (1)–(6) which also gives the minimum output harmonic distortion. In this article, they are referred to as RCMV1-PWM.

![Diagram](image-url)

**Figure 3.** (a) Two-level space vector diagrams for $F_L = 4$ and $F_L = 5$, (b) The synthesis of $\mathbf{ξ}_{ref}$ for $F_L = 4$ and $\mathbf{ξ}_{ref}$ in the area (1) [33] by using three switching sequences.
\( v_{xref}, x \in \{A, B, C\} \) (Eq. 5, 8 – 9)

\[
\begin{align*}
L_A, L_B, L_C (Eq. 6) & \quad 1 \\
\xi_A, \xi_B, \xi_C (Eq. 5) & \quad 2 \\
F_e = 1 & \quad 3 \\
F_e = 0 & \quad 000 \\
\text{Switching Sequence } s_A s_B s_C \\
\text{Pulse Generator}
\end{align*}
\]

\[
\begin{align*}
001 \rightarrow 000 \rightarrow 100 \rightarrow 110 & \quad \text{Yes} \\
010 \rightarrow 000 \rightarrow 100 \rightarrow 110 & \quad \text{Yes} \\
001 \rightarrow 000 \rightarrow 110 \rightarrow 111 & \quad \text{Yes} \\
100 \rightarrow 000 \rightarrow 110 \rightarrow 111 & \quad \text{Yes} \\
\end{align*}
\]

\[
\begin{align*}
\text{Switching Sequence } s_A s_B s_C \\
\text{Pulse Generator}
\end{align*}
\]

\[
\begin{align*}
\xi_B & \quad \xi_C \\
1 - \xi_A & \\
T_1 = (1 - \xi_A) \left( \frac{T_s}{2} \right) \\
T_2 = (1 - \xi_B) \left( \frac{T_s}{2} \right) \\
T_3 = (\xi_B - \xi_C) \left( \frac{T_s}{2} \right) \\
T_4 = (1 - \xi_B) \left( \frac{T_s}{2} \right)
\end{align*}
\]

\[
\begin{align*}
V_{CM} & \\
+V_{dct}/3 & \\
0 & \\
-\frac{V_{dct}}{3}
\end{align*}
\]
2.2. With Equal Loss Distribution

The presented RCMV1-PWM strategy ensures the zero average CMV, reduced CMV magnitude, and minimum output harmonic distortion. In addition to those, equal power loss distribution among switching devices is also realized by cyclically changing the switching states after a fundamental period of $T_0$ as per Table 1. In the latter section, RCMV1-PWM is evaluated thoroughly against other methods to confirm the equal distribution of power loss indicated in this section.

Table 1. Pulse generator of RMCV1-PWM with equal power loss distribution.

| $s_x + L_x$ | $0 \leq t \leq T_0$ | $T_0 \leq t \leq 2T_0$ | $2T_0 \leq t \leq 3T_0$ | $3T_0 \leq t \leq 4T_0$ |
|-------------|---------------------|---------------------|---------------------|---------------------|
| 0           | $s_1x = s_2x = s_3x = s_4x = 0$ | $s_1x = 0; s_2x = 1$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ |
| 1           | $s_1x = 1; s_2x = 0$ | $s_1x = 0; s_2x = 1$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ |
| 2           | $s_1x = 1; s_2x = 1$ | $s_1x = 0; s_2x = 1$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ |
| 3           | $s_1x = 1; s_2x = 1$ | $s_1x = 0; s_2x = 1$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ |
| 4           | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ | $s_1x = 0; s_2x = 0$ |

3. Performance Criteria for Evaluation

This section presents two important criteria, including the power loss and the harmonic distortion, to evaluate PWM strategies. The power loss estimation is used to verify the power loss balance of the proposed strategy among switching devices, as mentioned in the previous section. In addition, it establishes the condition of comparable power loss on which the harmonic distortion calculation is based to fairly compare across different PWM strategies.

3.1. Power Loss

The power loss, which typically consists of the conduction and switching loss, can be readily estimated by the thermal module in the PLECS simulation program [34]. The principle of power loss calculation is explained in detail in [35]. The power switching devices (IGBTs) with an antiparallel diode used in the five-level CHB inverter are IKW15N120H3, of which the thermal characteristics can be obtained from the manufacturer’s website [36] and imported into the thermal module. For comparison, the power loss distribution of a five-level NPC inverter is also included. The power switching devices IGBTs used in the five-level NPC topology are the same as those in the five-level CHB one and the clamping diode type is IDP30E120, of which the datasheet and thermal characteristics can be found in [37]. For easy reference, some main parameters of IGBT IKW15N120H3 and clamping diode IPD30E120 are tabulated in Tables 2 and 3.

Table 2. IGBT IKW15N120H3 specification [36].

| Parameters                              | Symbols | Value   |
|-----------------------------------------|---------|---------|
| Maximum Collector-Emitter Voltage      | $V_{ce\text{-max}}$ | 1200 V  |
| Maximum Continuous Collector Current at $T_j = 25 \, ^\circ\text{C}$ | $I_{c\text{-max}}$ | 30 A    |
| Maximum Continuous Collector Current at $T_j = 100 \, ^\circ\text{C}$ | $I_{c\text{-max}}$ | 15 A    |
| Maximum Junction Temperature           | $T_{j\text{-max}}$ | 175 °C  |
| Gate Emitter Voltage                   | $V_{GE}$ | $\pm 20 \, \text{V}$ |
| Collector-Emitter Saturation Voltage at $T_j = 25 \, ^\circ\text{C}$ | $V_{CE\text{sat}}$ | 2.05 V  |
| Turn-On Delay Time at $T_j = 25 \, ^\circ\text{C}$ | $t_{\text{on}}$ | 21 ns   |
Turn-Off Delay Time at Tj = 25 °C \( t_{d(off)} \) 260 ns
Turn-On Energy at Tj = 25 °C \( E_{on} \) 1.10 mJ
Turn-Off Energy at Tj = 25 °C \( E_{off} \) 0.45 mJ
Diode Forward Voltage at Tj = 25 °C, \( I_R = 15 \) A \( V_F \) 2.4 V
Diode Forward Current at Tj = 25 °C \( I_F \) 15 A
Diode Reverse Recovery Time at Tj = 25 °C \( t_{rr} \) 260 ns
Diode Reverse Recovery Charge at Tj = 25 °C \( Q_{rr} \) 0.80 \( \mu \)C
Diode Peak Reverse Recovery Current at Tj = 25 °C \( I_{rnm} \) 7.7 A

Table 3. Clamping diode IDP30E120 specification [37].

| Parameters                                      | Symbols | Value   |
|------------------------------------------------|---------|---------|
| Peak Reverse Voltage                           | \( V_{RBM} \) | 1200 V  |
| Maximum Continuous Collector Current at Tj = 25 °C | \( I_{F-max} \) | 50 A    |
| Maximum Continuous Collector Current at Tj = 90 °C | \( I_{F-max} \) | 30 A    |
| Maximum Junction Temperature                   | \( T_{j-max} \) | 150 °C  |
| Forward Voltage Drop at \( I_F = 30 \) A, Tj = 25 °C | \( V_f \) | 1.65 V  |
| Reverse Recovery Time at Tj = 25 °C            | \( t_{rr} \) | 243 ns  |
| Reverse Recovery Charge at Tj = 25 °C          | \( Q_{rr} \) | 2630 nC |
| Peak Reverse Recovery Current at Tj = 25 °C     | \( I_{rnm} \) | 23.7 A  |

3.2. Harmonic Distortion

The harmonic distortion performance of each PWM strategy is evaluated by the THD of the voltage and current outputs, the weighted THD (WTHD) of the voltage output, and the root mean square (RMS) of current ripple in Ampere. The formulas of these performance metrics are given as follows [33]:

\[
THD_{V_L} = \frac{1}{V_{ml}} \sqrt{\sum_{n=2}^{\infty} V_{nl}^2}
\] (24)

\[
WTHD_{V_L} = \frac{1}{V_{ml}} \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{nl}}{V_{n}}\right)^2}
\] (25)

\[
THD_I = \frac{1}{I_m} \sqrt{\sum_{n=2}^{\infty} I_n^2}
\] (26)

RMS current ripple = \[ \sqrt{\frac{1}{T_0} \int_0^{T_0} (i_{mes} - i_{fund})^2 dt} \]

where: \( V_{ml} \) and \( V_{nl} \) are the fundamental magnitude and the \( n^{th} \) harmonic magnitude of line voltage output, respectively. \( I_m \) and \( I_n \) are the fundamental magnitude and the \( n^{th} \) harmonic magnitude of phase current output, respectively. \( I_{mes} \) and \( I_{fund} \) are the measured and the fundamental component of phase current, respectively.

4. Simulation Results

The simulation is conducted in MATLAB/Simulink environment under the condition of \( V_{dc} = 200 \) V, \( f_0 = 50 \) Hz, \( f_{carrier} = 5 \) KHz, \( R_a = R_b = R_c = 33.3 \) Ω, \( L_a = L_b = L_c = 2.7 \) mH, \( C = 4700 \) μF for a five-level CHB converter. The comparative analysis of RCMV1-PWM will be conducted against POD-SPWM, APOD-SPWM, and IPD-SPWM in terms of the performance criteria presented in the previous section.

4.1. Harmonic Distortion Evaluation

On the basis of the comparable power loss set forth in Section 4.2, the output harmonic distortion performance of RCMV1-PWM is compared against that of other methods. The THD and WTHD of voltage and the THD of current, as well as the RMS value of current ripple, are evaluated with regard to the modulation index for four
strategies. Figures 5 and 6 shows that the IPD-SPWM gives the best output quality for a whole modulation range due to the three nearest vectors principle. However, the magnitude of CMV is twice as high as that of other strategies, as illustrated in Figure 7a. Hence, it is unfavorable in motor-drive applications due to adverse effects of high CMV magnitude, as mentioned earlier. As demonstrated in Figures 5 and 6, the proposed RCMV1-PWM produces better output harmonic performance than the POD-SPWM over a whole modulation range. For example, at \( m = 0.3 \), the THD values of voltage and current outputs are 61.78% and 22.19%, respectively, for RCMV1-PWM as opposed to 73.55% and 26.65%, respectively, for POD-SPWM. This translates to a more than 10% improvement of THD of voltage output and a more than 4% improvement of THD of current output. Likewise, at \( m = 0.3 \), the WTHD of voltage output, and the RMS value of phase current ripple, are 0.61% and 0.13 A, respectively, for RCMV1-PWM in comparison to 0.73% and 0.16 A, respectively, for POD-SPWM. Both RCMV1-PWM and POD-SPWM produce a reduced magnitude of CMV of \( V_{dc}/3 \) for a whole modulation range, as shown in Figure 7a. As a result, under the reduced-CMV-magnitude condition, RCMV1-PWM is more favorable than POD-SPWM in motor-drive applications due to the lower output harmonic distortion. As for APOD-SPWM, its THD and WTHD of both voltage and current outputs, as well as RMS value of current ripple, are inferior to those of RCMV1-PWM for \( m \leq 0.45 \) and \( m \geq 0.7 \). For these two modulation ranges, both APOD-SPWM and RCMV1-PWM obtain a reduced CMV magnitude of \( V_{dc}/3 \) as demonstrated in Figure 7a. For \( 0.45 \leq m \leq 0.7 \), the output harmonic performance of APOD-SPWM is better than that of RCMV1-PWM. However, the CMV magnitude of APOD-SPWM in this modulation range is the same as that of IPD-SPWM, i.e., \( 2V_{dc}/3 \) as shown in Figure 7a. Hence, the better output harmonic performance of APOD-SPWM is achieved at the expense of higher CMV magnitude. Therefore, under the reduced-CMV-magnitude condition, the proposed RCMV1-PWM gives the most optimum output harmonic performance.

![Diagram](image-url)
Figure 5. Comparative analysis of (a) THD and (b) WTHD of line voltage output for different PWM strategies with respect to modulation index.
Figure 6. Comparative analysis of (a) THD and (b) RMS ripple of current ripple for different PWM strategies with respect to modulation index.

The frequency spectrum of CMV for RCMV1-PWM is also shown in Figure 7b. As can be observed from this figure, the third harmonic component of the CMV \( f_0 = 150 \text{ Hz} \) is virtually nonexistent, which indicates the zero average CMV in one sampling period is maintained.
Figure 7. (a) Comparison of CMV magnitudes for RCMV1-PWM, POD-SPWM, APOD-SPWM, and IPD-SPWM at $V_{dc} = 400$ V, (b) frequency spectrum of CMV for RCMV1-PWM at $m = 0.623$.

4.2. Power Loss Comparison

The conduction and switching loss of eight IGBTs of the phase leg A for RCMV1-PWM at $m = 0.3$ and $m = 0.8$ under the power factor of 0.99 in the five-level CHB inverter are shown in Figure 8. As shown in Figure 8, the equal power loss distribution among switching devices is achieved for the proposed strategy, as indicated in Section 2.
Figure 8. Comparison of (a) conduction loss and (b) switching loss of the eight IGBTs of the phase leg A in a five-level CHB converter for RCMV1-PWM at PF = 0.99.

By contrast, the NPC converter, which has the issue of unequal power loss distribution [11] illustrated in Figure 9 for a five-level NPC inverter, possibly leads to failures in some switching devices that have to experience a considerable amount of power loss over a long-term operation, thereby reducing the efficiency and reliability of a system, as well as the overall switch utilization [11]. The active neutral point clamped (ANPC) converter was proposed in [11] to resolve this issue. However, the increase in the number of switching devices results in higher power loss, and the control strategy is more complicated when compared to the CHB converter at the same number of levels. Therefore, the CHB converter topology with the proposed strategy featuring lower CMV magnitude, zero average CMV, and improved output harmonic distortion, as well as equal power loss distribution among switching devices, becomes a topology of choice due to higher efficiency and reliability over a long-term operation as opposed to the NPC one for the number of levels being greater than or equal to 5 ($n \geq 5$).
In order to further evaluate the power loss performance of RCMV1-PWM, the comparison of its power loss is made against that of POD-SPWM, APOD-SPWM, and IPD-SPWM at $m = 0.2$, $0.5$, and $0.8$, as illustrated in Figure 10. As can be seen from Figure 10, both the total switching loss and the total conduction loss of RCMV1-PWM are equivalent to those of other strategies at three modulation indices.
Figure 10. Comparison of (a) total conduction loss and (b) total switching loss for RCMV1-PWM, POD-SPWM, APOD-SPWM, and IPD-SPWM at 3 different modulation indices in a five-level CHB converter under PF = 0.99.

5. Experimental Results

The experiment is conducted on a five-level CHB converter with a no-load three-phase induction motor under the condition of $V_{dc} = 50 \text{ V}$, $C = 4700 \text{ μF}$, $f_{carrier} = 5 \text{ KHz}$, $f_0 = 50 \text{ Hz}$, deadtime = 2 μs. The parameters of the three-phase induction motor are as follows: 1.49 KW, 380 $V_{rms}$, 50 Hz, Y-connected, $R_s = 8.68 \Omega$, $R_r = 8.3 \Omega$, $L_{ir} = 17.5 \text{ mH}$, $L_{dr} = 17.5 \text{ mH}$, $L_m = 0.862 \text{ H}$. The V/f control is used such that the maximum linear modulation index $m = 0.866$ corresponds to the rated frequency of 50 Hz. The microcontroller, TMS320F28377D, has been used to fire the gating signals for the switching devices in the five-level CHB converter.

The experimental line voltage and the phase current, as well as the common-mode voltage waveforms, are shown in Figure 11a–c, respectively, for RCMV1-PWM, POD-SPWM, and APOD-SPWM at $f_0 = 36 \text{ Hz}$ ($m = 0.623$) under the no-load condition. In addition, to demonstrate the output harmonic distortion performance, the experimental THD of line voltage, and the phase current, as well as the RMS values of phase current ripple of RCMV1-PWM, are compared against those of other strategies. As can be observed from Figure 12a, the THD of line voltage of RCMV1-PWM is better than that of POD-SPWM for a whole fundamental frequency range. This is consistent with the simulated one, as shown in Figure 8a. The most noticeable reduction in THD of voltage happens at $f_0 = 14 \text{ Hz}$, at which it is 88.9% for RCMV1-PWM, as opposed to 106.1% for POD-SPWM. These results in an 18.87% improvement of THD of voltage for RCMV1-PWM over POD-SPWM. The frequency spectra of line voltage at $f_0 = 36 \text{ Hz}$ are shown in Figure 13a,b to further illustrate the THD reduction in line voltage of RCMV1-PWM over POD-SPWM. As can be observed from Figure 13a,b, the harmonic components around the switching frequency ($f = 5 \text{ KHz}$) of RCMV1-PWM are significantly less than those of POD-SPWM. In particular, they are less than 14 V in RCMV1-PWM as opposed to more than 25 V in POD-SPWM. With regard to APOD-SPWM, the THD of voltage of RCMV1-PWM is lower than that of APOD-SPWM for $f_0 < 26 \text{ Hz}$ ($m < 0.45$) and $f_0 > 40 \text{ Hz}$ ($m > 0.69$). The most significant improvement of the THD of line voltage happens at $f_0 = 10 \text{ Hz}$, at which it is 127.59% for RCMV1-PWM compared to 147.32% for APOD-SPWM. This translates to a 19.72% improvement of the THD of the voltage of RCMV1-PWM over APOD-SPWM. For $26 \text{ Hz} \leq f_0 \leq 40 \text{ Hz}$, the THD value of the voltage of APOD-SPWM is better than that of RCMV1-PWM. However, this frequency range $26 \text{ Hz} \leq f_0 \leq 40 \text{ Hz}$ ($0.45 \leq m \leq 0.69$) coincides with the higher CMV magnitude ($2V_{dc}/3$) of APOD-SPWM than that ($V_{dc}/3$) of RCMV1-PWM and POD-SPWM,
as demonstrated in Figure 10a. As can be observed from Figure 12a, IPD-SPWM still produces the best output harmonic distortion. However, its magnitude of CMV is twice as high as that of RCMV1-PWM and POD-SPWM for a whole frequency range and is the same as that of APOD-SPWM for $f_0 \geq 26$ Hz ($m \geq 0.45$).

Figure 11. Top trace: line voltage waveform; Middle trace: CMV waveform; Bottom trace: phase current waveform of (a) RCMV1-PWM, (b) POD-SPWM, (c) APOD-SPWM for $f_0 = 36$ Hz ($m = 0.623$) under no-load condition.
With regard to the current, the THD of current and the RMS values of current ripple of RCMV1-PWM are consistently better than those of POD-SPWM for a whole fundamental frequency range, as illustrated in Figure 12b,c, respectively. This is further supported by the frequency spectra of current of both RCMV1-PWM and POD-SPWM as shown in Figure 14a,b at $f_0 = 36$ Hz. As can be observed from Figure 14a,b, the harmonic components around the switching frequency ($f = 5$ KHz) are significantly less than 6 mA in RCMV1-PWM, as opposed to more than 10 mA in POD-SPWM. Similar to the THD of voltage, the THD of current and the RMS values of current ripple of APOD-SPWM are lower than those of RCMV1-PWM for $26$ Hz $\leq f_0 \leq 36$ Hz ($0.45 \leq m \leq 0.62$), which corresponds to a higher CMV magnitude of APOD-SPWM. As for $f_0 < 26$ Hz ($m < 0.45$) and $f_0 > 36$ Hz ($m > 0.62$), the THD of current, as well as the RMS value of current ripple of APOD-SPWM are worse than those of RCMV1-PWM, as evidenced in Figure 12b,c. The harmonic distortion calculations, including THD and WTHD in both simulation and experiment, are calculated up to the 200th harmonic of the fundamental frequency.

As for the CMV reduction performance, both RCMV1-PWM and POD-SPWM produce a reduced magnitude of CMV of $V_{dc}/3$ for a whole fundamental frequency range. In particular, the CMV waveforms and their frequency spectra are shown in Figure 11a,b and 15a,b, respectively, at $f_0 = 36$ Hz ($m = 0.623$). The CMV reduction performance is demonstrated by the reduction in the magnitude of CMV components around the switching frequency ($f = 5$ KHz). Specifically, they are less than 5 V for both RCMV1-PWM and POD-SPWM compared to more than 10 V for APOD-SPWM at $f_0 = 36$ Hz ($m = 0.623$), as shown in Figure 15. Moreover, the 3rd harmonic component of CMV, as shown in Figure 15, is well less than 1 V, which accounts for less than 2% of $V_{dc}$ ($V_{dc} = 50$ V), thereby ensuring the zero average CMV in one sampling period for RCMV1-PWM. Therefore, under the condition of the reduced magnitude of CMV, the zero average CMV, and the equal distribution of power loss, the proposed strategy produces the most optimum output harmonic performance when compared to POD-SPWM, and APOD-SPWM.
Figure 12. Experimental comparative analysis of (a) THD of voltage, (b) THD of current, (c) RMS current ripple for RCMV1-PWM, POD-SPWM, APOD-SPWM, and IPD-SPWM.
Figure 13. Experimental frequency spectra of voltage for (a) RCMV1-PWM, (b) POD-SPWM, (c) APOD-SPWM at \( f_0 = 36 \) Hz (\( m = 0.623 \)).
Figure 14. Experimental frequency spectra of current for (a) RCMV1-PWM, (b) POD-SPWM, (c) APOD-SPWM at \( f_0 = 36 \) Hz (\( m = 0.623 \)).
6. Conclusions

This article presents a reduced-CMV PWM strategy with zero average CMV and minimum output harmonic distortion for a five-level CHB converter. The CMV magnitude reduction aims to alleviate the shaft voltage and bearing current problems that lead to premature failures in motors while the zero average CMV is maintained to avoid the complications in CM filter design. The switching loss analysis conducted in the PLECS thermal module confirms that the proposed strategy, namely RCMV1-PWM, gives the comparable switching loss to that of POD-SPWM, APOD-SPWM, and IPD-SPWM. On the basis of equal switching loss power, the CMV reduction and the output harmonic distortion are compared for different PWM strategies. In terms of the CMV magnitude reduction, both RCMV1-PWM and POD-SPWM produce the same reduced CMV magnitude while the CMV magnitude of IPD-SPWM is twice as high as that of RCMV1-PWM and POD-SPWM over a whole range of modulation. Concerning output harmonic distortion, RCMV1-PWM gives better output harmonic distortion than that of POD-SPWM over a whole range of modulation under the condition of the reduced CMV magnitude. Moreover, in the modulation range that the CMV magnitude of APOD-SPWM is the same as that of RCMV1-PWM and POD-SPWM, the output harmonic distortion of APOD-SPWM is
inferior to that of RCMV1-PWM. Therefore, under the condition of the equivalent switching loss power, the reduced CMV magnitude, and the zero average CMV, the proposed scheme, namely RCMV1-PWM, gives the most optimum harmonic distortion as opposed to that of POD-SPWM and APOD-SPWM, thereby reducing the torque vibration attributed to high harmonic distortion, as well as adverse effects caused by the high CMV magnitude in motor-drive applications. Finally, thanks to equal power loss distribution, the proposed strategy, when applied to a five-level CHB converter, yields higher efficiency and reliability than a five-level NPC counterpart.

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