Implementation of a distributed Stand Alone Merging Unit

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Abstract. Smart substations for smart grids must be safe and reliable. In order to enable the development of smart substations, according to IEC61850 standards, a new stand alone merging unit based on STM32F7 arm microcontroller is proposed in this paper. The time synchronization is obtained by means of an Oscillator Disciplined by Global Positioning System (GPSDO); a high-precision Analog-to-Digital Converter (ADC) samples and converts voltage and current signals. The microcontroller coordinates the various parts of the system, implements the synchronization of merging unit and ethernet communication.

1. Introduction

The increasing development of smart grids ([1–9]) increases, in turns, the interest in smart substation development [10]. According to IEC61850 [11] Merging Units (MUs) play a crucial role in the design of substations communication and automation systems.

MUs sample alternating current and/or voltage of one or multiple phases, they convert these analog voltage and current signals to digital values and transmit the sampled values (SVs) to protection relays (PRs) and bay controllers (BCs) through either Ethernet or optical communication channels based on the IEC 61850-9-2 protocol. MUs could provide real-time data for current, voltage and status of power grids; and therefore, they can play a key role in real-time monitoring, protection and control of the grids. However, MU data exchange, sharing and interoperability can pose major challenges for the power industry. With the standardization of MU data formats, interfaces and communication protocols, it is hopeful that data interoperability of MUs can be achieved via the IEC 61850-9-2 standard. Nevertheless, MUs and PRs produced by different vendors may not be interoperable.

However Stand Alone Merging Units (SAMU) can be installed without impacting existing protection, metering and supervision equipment, thus allowing a smooth transition to digital smart grid data processing capabilities. Special care has to be taken for accurate time synchronization between units. In the following, Section 2 presents the proposed SAMU signal conditioning stage and hardware implementation, which is specifically designed for the application at hand; Section 3, instead, describes the firmware development.

2. Proposed SAMU

2.1. Signal Conditioning stage

In order to build up a complete SAMU, a combined voltage and current transducers has been realized. In figure 1 the electric scheme of the proposed combined transducer and conditioning
For both the transducers, three main sections can be found: an input stage, an insulation stage and an output stage. The input stage of the current transducer is composed of a shunt, with resistance equal to 2.5 mΩ, and a differential amplifier with gain equal to 1.8. For the voltage transducer, the input stage is an active compensated divider. It has been obtained by two operational amplifiers: one is mounted in current-pump configuration, while the other realizes a transimpedance amplifier [12].

It is necessary to insulate the transducer to preserve the safety of workers and the integrity of instrumentations. The common mode voltage between inputs of voltage transducers and ground may be very dangerous. In order to avoid this, an optical insulation stage has been introduced after the input stage. It consists of a modulator optically coupled to a demodulator. It is the integrated circuit HCPL7840, produced by Agilent. It guarantees insulation up to 2500 V with an upper bound on usable bandwidth at approximately 100 kHz.

As the insulation stages, also the output stages are identical for the two transducers. The insulation stage receives input signals in the range of ±200 mV and its output is the reproduction of the input but amplified with a scaling factor of 8 and with a common mode voltage of about 2.5 V. In order to eliminate this common mode voltage, a differential amplifier has been used. It has a unity gain and adds an offset equal to 1.65 V to the input voltage. So, the output is in the range of 0 ÷ 3.3 V and it is compatible with the range of STM32F7 analog input.

2.2. Hardware Implementation
The proposed SAMU is based on STM32F767ZI, a high performance microcontroller ARM Cortex-M7 with 2 Mbytes Flash, 216 MHz of clock frequency, L1 cache, 512 Kbytes of SRAM, DSP with FPU, art accelerator. The microcontroller unit has been interfaced with an external
ADC MAX11960 20-bit, sampling frequency of 1 MHz, fully differential Successive Approximation Register (SAR), 99dB of Signal to Noise Ratio, 123dB total harmonic distortion, ±1 LSB of differential non-linearity. The time synchronization is achieved through a Connor-Winfield FTS125-CTV-010.0 MHz GPSDO. It is a combination of a GPS receiver and a high-quality stable oscillator. UART interface is interconnected to read the GPS timestamp. The GPSDO produces a 1-PPS signal and a 10 MHz square wave, both synchronous with absolute time reference from GPS. It can also use external synchronization signal.

The 1-PPS signal is used to start acquisition and to maintain all the sample referenced to the corresponding 1-second-frame.

The 10 MHz reference clock is used as external trigger input for the STM32F767ZI’s timer. This peripheral is configured to control the Pulse Width Modulation (PWM) output with 50% duty cycle. The output signal is supplied as clock to ADC, its frequency is obtained by dividing the 10 MHz reference clock and is fixed to 12.8 kHz according to IEC61850; therefore, 256 samples per nominal line cycle (50 Hz) are produced.

STM32F767ZI integrates an EMAC RMII (Reduced Media Independent Interface) controller, with dedicated Direct Memory Access (DMA) that has been opportunely interfaced with physical layer (PHY). In figure 2 a block scheme of the proposed SAMU is shown.

3. Embedded Measurement Firmware
The microcontroller has been programmed using Standard C Language. The adopted design pattern is the classical foreground-background approach. The firmware implements the opportune drivers for all the above described hardware devices and performs their coordination.

The timebase for the ADC is built up adopting the internal timer peripheral. As mentioned before, the 10 MHz clock reference signal from GPSDO has been used as external trigger for the timer and this acts as divider, automatically controlling external PWM line with 50% duty cycle. This line is used to clock the ADC. To maintain a high level of accuracy the timer is configured to work in hardware without Interrupt Service Routine (ISR) latency.

The microcontroller firmware also receives and parses National Marine Electronics Association (NMEA) sentences from GPS receiver to obtain time stamp. Since SAMU must associate timestamps to each sample, an hard realtime mechanism has been implemented to identify the precise moment in which a 1-second-frame starts, using PPS signal external interrupt.

Figure 2. System Description.
The sampled data are collected via Serial Peripheral Interface (SPI) interface and put in relation with time stamp. Both voltage and current transducer responses has been characterized and systematic error has been compensated [13] through digital filter executed using the integrated Digital Signal Processor (DSP). The microcontroller firmware is responsible for IEC61850-9-2 communication via Ethernet, too. To fulfill this task, integration between well known Lightweight Internet Protocol (LwIP) stack and libiec61850 (an open source implementation of standard [14]) has been realized. This integration has been conducted through Berkeley Software Distribution (BSD) socket interface in LwIP stack.

IEC 61850-9-2 is the international standard protocol defined to ensure interoperability within Substation Automation System (SAS) by standardizing the abstract data models and services to support SAS communications.

4. Conclusion
In this paper a concept design of a distributed Stand Alone Merging Unit has been presented. It is based on a GPSDO, a 20-bit ADC, a STM32F7 ARM microcontroller and a specifically designed and realized electronic input stage. It can be directly applied to the output of instrument transformers both inductive or low-power.

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