High Efficiency and Voltage Conversion Ratio Bidirectional Isolated DC-DC Converter for Energy Storage System

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ABSTRACT This paper proposes a high efficiency and conversion ratio bidirectional isolated DC-DC converter with three-winding coupled inductor, which can fulfill storage system charging and discharging. The proposed topology is improved from traditional Buck-Boost converter. By integrating coupled inductor and switched-capacitor into power stage, the proposed converter can achieve the merits of isolation and bidirectional power flow. The proposed topology has only four switches and a common core coupled inductor, which greatly reduces design costs and achieves high step-up/step-down voltage gain without excessive duty cycles or high turns ratios. In addition, the proposed also has the function of leakage inductance energy recovery, which can recover all the energy stored in the leakage inductance to improve efficiency, and the main switches has a zero voltage switching (ZVS) feature. This paper implements a 500 W converter to verify the feasibility of the proposed topology through software simulation and experiment results, and conducts theoretical analysis, formula derivation, operation principle analysis, and non-ideal analysis. Finally, the experimental results show that the highest efficiency of the step-up and step-down modes are 96.8% and 96.4%, respectively.

INDEX TERMS Bidirectional DC-DC converter; zero voltage switching; three-winding coupled inductor.

I. INTRODUCTION

Since the industrial revolution, power generation driven by petrochemicals, coal and liquefied natural gas has caused a series of damage to the environment. Therefore, in recent years, countries around the world have also realized the importance of renewable energy and vigorously advocated renewable energy [1]-[3]. Renewable energy is natural energy, such as solar energy, wind energy, tidal energy, geothermal energy, hydroelectric power and biogas. However, due to irresistible factors, such as weather, environment, etc., the aforementioned renewable energy sources will become unstable. In order to make up for the power shortage in the process of green energy power generation, an energy storage system needs to be added to make the entire system more complete. When the production of green energy is too much, the excess electric energy will be stored in the energy storage system, and when the peak electricity is used, the energy storage system will be activated to distribute the overall electric energy. Therefore, as shown in Fig.1, a distributed generation system [4]-[6] is needed to assist the renewable energy system. The distributed power generation system plays an important role in the Micro-grid system, reducing the excessive consumption of traditional energy.

With the development of green energy, the demand for converters has increased. Compared with the traditional converters in the past, converters nowadays have more complexity and functional requirements; furthermore, the application level is more extensive. Bidirectional converters are indispensable in green energy system. Besides power supply applications for green energy system, bidirectional converters are also widely used in electric vehicle (EV), hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), uninterruptible power system (UPS), battery energy storage system (BESS) and renewable energy systems, etc., the importance of bidirectional converters can
be seen from the above, it can effectively reduce the number of components, increase the power density and reduce production costs. The common non-isolated bidirectional converter is to transform Boost, Buck-Boost, SEPIC and other unidirectional converters, which has the advantages of low cost, high circuit stability, and strong practicability. However, they are limited by the duty cycle, and traditional non-isolated converters cannot provide a higher voltage conversion ratio.

The increased auxiliary power supply terminal makes the converter uses a three-switch topology on the low-voltage side to replace the full-bridge structure. It can save the cost of the drive circuit, and can better ensure the stability of the entire system.

II. CIRCUIT ARCHITECTURE AND OPERATIONAL PRINCIPLES

The proposed isolated bidirectional DC-DC converter in this paper, as shown in Fig. 2(a). The components are defined as follows. \( V_I \) and \( V_M \) are the low-side and high-side power ports, respectively. The \( S_I \) to \( S_E \) are power switches, where \( D_S1 \) to \( D_S4 \) and \( C_S1 \) to \( C_S4 \) represent the body diodes and parasitic capacitances of the switches, respectively. The capacitors \( C_I \) to \( C_d \), three-winding coupled inductor are also part of the proposed topology. The coupled inductor is composed of leakage inductance \( L_{k1}, L_{k2} \) and \( L_{k3} \), magnetizing inductance \( L_{m1} \) and turns ratio \( n \).

![Diagram of diversified generation system with energy storage system.](image)

![Diagram of the proposed bidirectional DC-DC converter topology.](image)

Figure 2. The proposed topology: (a) diagram of the bidirectional isolated DC–DC converter and (b) the definitions for the equivalent circuit diagram.
The operation principle of the proposed converter in step-up mode and step-down mode is analyzed. The corresponding components, voltage polarity and current direction of the converter are shown in Fig. 2(b). The magnetic components operate in CCM mode. In order to describe and simplify the operation of the converter, assume the following:

1) The capacitance C1, C2, C3 and C4 values are assumed to be large enough.
2) All switches are assumed to be ideal, and body diodes and parasitic capacitance are considered.
3) The values of the leakage inductance Llk1, Llk2 and Llk3 are much smaller than magnetizing inductance Lm1.
4) The turns of N1 is equal to N2 but less than N3, and the ratio of N3 / N1 and N2 / N1 are defined as n.

A. Step-Up Mode

In the step-up mode, the switches S1 and S2 are complementary signals Vgs1 and Vgs2, and the signals of S3 and S4 are OFF state. The key waveforms of the step-up mode are shown in Fig. 3. This operation can be divided into five modes in an operating cycle, and the modes are shown in Fig. 4(a)-(e).

1. Mode 1 [t0–t1]

This mode starts at time t = t0, all switch signals are in OFF state. The leakage inductance Llk1 extracts the energy from the parasitic capacitance C5 of the switch S1 to achieve ZVS. The parasitic capacitances C5 of the switches S1 storage energy until the switches S1 is in OFF state. The low voltage side Vl supplies energy to the high voltage side Vh, while the current of the body diode Ds3 on switch S3 drops to zero. The equivalent circuit of Mode 1 shown as Fig. 4(a).

2. Mode 2 [t1–t2]

This modes begins as switch S1 is turned ON at t = t1, the switch signal Vgs1 is in ON state and the switch signal Vgs2 is in OFF state. The low voltage side Vl supplies energy to magnetizing inductance Lm1 and leakage inductance Llk1 and is also transmitted to the high voltage side Vh. The capacitor C3 through the coupled inductor and via the body diode Ds3 of the switch S3, while the low voltage side Vl and the capacitor C1 provide energy to the capacitor C2 and the leakage inductance Llk2. At the same time, the capacitor C4 starts to release energy to high voltage side Vh. Mode 2 ends while switch S1 is turned OFF. The equivalent circuit of Mode 2 is shown as Fig. 4(b).

3. Mode 3 [t2–t3]

At the beginning of this mode at the time t = t2, all switch signals are in OFF state. The leakage inductance Llk2 extracts the energy from the parasitic capacitance C5 of the switch S2 to achieve ZVS. The parasitic capacitances C5 of the switches S1 storage energy until the switches S1 is in OFF state. The low voltage side Vl continuously transmits energy to the high voltage side Vh, while the current of the body diode Ds3 on switch S3 drops to zero. The equivalent circuit of Mode 3 is shown as Fig. 4(c).

4. Mode 4 [t3–t4]

In Mode 4, the time starts from t = t3, the switch signal Vgs2 is in ON state and the switch signal Vgs1 is in OFF state. The magnetizing inductance Lm1 and the capacitor C2 releases energy to the high voltage side Vh. The capacitor C2 through the coupled inductor and via the body diode Ds4 of the switch S4. Meanwhile, the capacitor C3 starts to release energy to high voltage side Vh. The leakage inductance Llk1 releases energy to the capacitor C1 through the switch S1 until the current in S1 is zero, and the Mode 4 ends. The equivalent circuit of Mode 4 is shown as Fig. 4(d).

5. Mode 5 [t4–t5]

Mode 5 at time t = t4, the switch signals is consistent with the previous mode. The capacitor C1 continues to charge but capacitor C2 continues to discharge. Mode 5 ends while switch S2 is turned OFF. The equivalent circuit of Mode 5 is shown as Fig. 4(e).
The energy of capacitor C1 is stored by the leakage inductance L_{lk1}. The inductor L1 releases energy to the low voltage side V_L. While the switch signals V_{gs1}, V_{gs4} and V_{gs5} are in ON state, Mode 1 ends. The equivalent circuit of Mode 1 is shown as Fig. 6(a).

2. Mode 2 [t1–t2]

This stage begins as switch S1 and S3 are turned ON and switch S2 and S4 are turned OFF at t = t1, the switch signal V_{gs2} and V_{gs4} are in ON state and the switch signal V_{gs1} and V_{gs4} are in OFF state. The energy of the magnetizing inductance L_{m1} is continuously transmitted to the low voltage side V_L. The capacitor C1 continues to discharge, while the current of the leakage inductance L_{lk2} drops to zero, Mode 2 ends. And the equivalent circuit of Mode 2 is shown as Fig. 6(b).

3. Mode 3 [t2–t3]

At the beginning of this mode at the time t = t2, the switch signals is consistent with the previous mode. The capacitor C3 releases energy to the low voltage side V_L through the coupled inductor, while the capacitor C2 provides energy to the low voltage side V_L and the capacitor C1. At the same time, the high voltage side V_H starts to charge the capacitor C4. Mode 3 ends while all switches are turned OFF. The equivalent circuit of Mode 3 is shown as Fig. 6(c).

4. Mode 4 [t3–t4]

In Mode 4, the time starts from t = t3, all switch signals are in OFF state. The high voltage side VH charges the parasitic capacitance C_{S4} of the switch S3 until the switch S3 extracts the energy from the parasitic capacitance C_{S4} of the switch S4 to.

**Figure 5. Key waveforms of proposed topology in step-up mode.**
achieve ZVS. The energy of the magnetizing inductance $L_{m1}$ starts to store energy. Meanwhile, the leakage inductance $L_{lk1}$ and $L_{lk2}$ are released to the low voltage side $V_L$ via the body diode $D_{S1}$ of the switch $S1$, while $C_{S3}$ reaches the voltage of $V_{H}$. Mode 4 ends. The equivalent circuit of Mode 4 shown as Fig. 6(d).

Figure 6. Equivalent circuit diagram of in step-down mode, (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, and (g) Mode 7.

5. Mode 5 [t4→t5]

At time $t = t4$, the switch signals $V_{gs1}$ and $V_{gs2}$ are in OFF state and the switch signals $V_{gs2}$ and $V_{gs4}$ are in ON state. The capacitor $C1$ supplies energy to magnetizing inductance $L_{m1}$ and leakage inductance $L_{lk1}$ but capacitor $C2$ continues to release energy to leakage inductance $L_{lk2}$. The capacitors $C3$ continues discharged until the current of switch $S4$ drops to zero, Mode 5 ends. The equivalent circuit of Mode 5 is shown as Fig. 6(e).

6. Mode 6 [t5→t6]

At time $t = t5$, the switch signals is consistent with the previous mode. The capacitor $C1$ continues to supply energy to magnetizing inductance $L_{m1}$ and leakage inductance $L_{lk1}$. While the current of the switch $S2$ drops to zero, Mode 6 ends. The equivalent circuit of Mode 6 is shown as Fig. 6(f).

7. Mode 7 [t6→t7]

At the beginning of this mode at the time $t = t6$. The leakage inductance $L_{lk2}$ starts to provide energy to the capacitor $C2$. While all switches are turned OFF, Mode 7
ends. And the equivalent circuit of Mode 7 is shown as Fig. 6(g).

III. STEADY-STATE ANALYSIS

While analyzing the circuit, the analysis is operated in CCM. The switching period is TS, the signals \( V_{gs1} \) and \( V_{gs2} \) are turned ON for time \( D1TS \) and turned OFF for time \( 1-D1/TS \), in step-up mode. In step-down mode, the signals \( V_{gs1} \) and \( V_{gs3} \) are turned ON for time \( D3TS \) and turned OFF for time \( 1-D3TS \), the while switching period is TS. The following assumptions need to be made when the proposed topology is analyzed:

1) All components are ideal, regardless of internal resistance and parasitic effects.
2) The capacitance of all capacitors is large enough, making the voltage of capacitors constant.
3) The leakage inductance of the coupled inductor is ignored.
4) Ignore the circuit operation mode in the dead time.
5) The ideal turns ratio is represented by \( n = N3 / N1 = N3 / N2 \) and \( n \) is defined as coupled inductor turns ratio.

A. Step-Up Mode

1. Voltage Gain Analysis

The \( V_H \) is the sum of the voltages of \( V_{C3} \) and \( V_{C4} \), it can be expressed as

\[
V_H = V_{C3} + V_{C4}
\]

(1)

In order to derive the high voltage side \( VH \), the relationship between \( V_{C1}, V_{C2}, V_{C3}, V_{C4} \) and low voltage side \( V_t \) must be derived respectively.

During \( D1TS \), the switch signals is turned ON by \( V_{gs1} \), as shown in the equivalent circuit in Fig. 4(b). According to Kirchhoff's voltage law (KVL), the voltage at \( L_{m1} \) can be expressed as

\[
V_{L1} = V_L + V_{C1} - V_{C2} = \frac{V_{C3}}{n} L_{m1} \frac{n\Delta i_{Lm1, on}}{D1TS}
\]

(2)

During \( (1-D1)TS \), the switch signals \( V_{gs1} \) is turned OFF and the equivalent circuit is shown in Fig. 4(e). According to KVL, the voltage at \( L_{m1} \) can be expressed as

\[
V_{L1} = V_{c1} = V_{c2} = \frac{V_{C4}}{n} L_{m1} \frac{n\Delta i_{Lm1, off}}{(1-D1)TS}
\]

(3)

According to the voltage-second balance of the inductor, the amount of current change in the steady-state during switching must be zero, expressed as

\[
\Delta i_{Lm1, on} = \Delta i_{Lm1, off}
\]

(4)

Substituting (2) and (3) into (4), the voltage of capacitors \( C1, C2, C3 \) and \( C4 \) can be obtained as

\[
V_{C1} = \frac{D1}{1-D1} V_L
\]

(5)

\[
V_{C2} = \frac{D1}{1-D1} V_L
\]

(6)

\[
V_{C3} = nV_L
\]

(7)

Finally, substituting (7) and (8) into (1), the voltage gain in step-up mode \( G_{step-up} \) can be derived as

\[
G_{step-up} = \frac{V_H}{V_L} = \frac{n}{1-D1}
\]

(9)

According to (9), the voltage gain in the step-up mode \( G_{step-up} \), the relationship between the duty cycle \( D1 \) and the turns ratio \( n \) is shown in Fig. 7.

Figure 7. Voltage gain of the proposed topology in step-up mode.

2. Voltage and Current Stresses Analysis of Components

According to the switching sequence in step-up mode, the voltage stress relative to \( S1, S2, S3 \) and \( S4 \) can be expressed as

\[
V_{ds1, stress} = \frac{1}{1-D1} V_L = \frac{1}{n} V_H
\]

(10)

\[
V_{ds2, stress} = \frac{1}{1-D1} V_L = \frac{1}{n} V_H
\]

(11)

\[
V_{ds3, stress} = V_H = nV_L
\]

(12)

\[
V_{ds4, stress} = V_H = nV_L
\]

(13)

According to Kirchhoff's current law (KCL) and ampere-second balance, the peak current relative to \( S1, S2, S3 \) and \( S4 \) can be expressed as

\[
I_{ds1, peak} = \frac{n}{(1-D1)D1} I_H + \frac{(1-D1)D1}{2L_{m1}f_n} V_H
\]

(14)

\[
I_{ds2, peak} = \frac{nD1}{(1-D1)^2} I_H + \frac{(1-D1)D1}{2L_{m1}f_n} V_H
\]

(15)

\[
I_{ds3, peak} = \frac{2}{D1} I_H
\]

(16)

\[
I_{ds4, peak} = \frac{2}{1-D1} I_H
\]

(17)

3. Magnetic Components Design

The magnetic components of the proposed topology are designed in CCM, the maximum and minimum current of the magnetic components \( L_{m1} \) can be calculated by
The capacitor ripple voltage can be expressed as
\[ \Delta V_C = \frac{\Delta Q}{C} = \frac{i_{m} \Delta t}{C} \] (24)

The voltage ripple of each capacitor is \( \Delta V_{C1}/V_{C1} \), \( \Delta V_{C2}/V_{C2} \), \( \Delta V_{C3}/V_{C3} \) and \( \Delta V_{C4}/V_{C4} \), and each capacitance value can be obtained as
\[ C_i = \frac{(1-D_i)}{2D_i^2\Delta V_{C_i}/f_s} \frac{I_H}{V_H} \] (25)

B. Step-Down Mode

1. Voltage Gain Analysis

The low voltage side \( V_L \) is the voltage of the magnetizing inductance \( L_{m1} \), it can be expressed as
\[ V_L = V_\text{L}_{m1} \] (29)

During D3TS, the switch signals \( V_{gs1} \) and \( V_{gs3} \) are turned ON, as shown in the equivalent circuit in Fig. 6(c). According to KVL, the voltage at \( L_{m1} \) can be expressed as
\[ V_{L_{m1}} = \frac{V_{C3}}{n} = V_L + V_{C1} - V_{C2} = L_{m1} \frac{\Delta i_{L_{m1,\text{off}}}}{n(1-D_3)T_s} \] (30)

During (1-D3)TS, the switch signals \( V_{gs1} \) and \( V_{gs3} \) are turned OFF, and the equivalent circuit is shown in Fig. 6(f). According to KVL, the voltage at \( L_{m1} \) can be obtained as
\[ V_{L_{m1}} = \frac{V_{C4}}{n} = V_L + V_{C3} - V_{C2} = L_{m1} \frac{\Delta i_{L_{m1,\text{on}}}}{n(1-D_3)T_s} \] (31)

Substituting (30) and (31) into (4), the voltage of capacitors \( C_1, C_2, C_3 \) and \( C_4 \) can be obtained as
\[ V_{C1} = (1-D_1)V_H \] (32)
\[ V_{C4} = D_3V_H \] (33)
\[ V_{C1} = D_3V_L \] (34)
\[ V_{C2} = D_3V_L \] (35)

The voltage of \( L_{m1} \) is equal to the voltage of \( V_{C3} \) divided by \( n \). Finally, substituting (32) into (29), the voltage gain in step-down mode \( G_{\text{step-down}} \) can be derived as
\[ G_{\text{step-down}} = \frac{V_L}{V_H} = \frac{1-D_3}{n} \] (36)

Figure 8. The curve of \( L_{m1,\text{BCM}} \) in step-up mode.

The peak-to-peak value of the capacitor ripple can be calculated by using the inflow and outflow capacitor current. The capacitor ripple voltage can be expressed as
\[ \Delta V_c = \frac{\Delta Q}{C} = \frac{i_{m} \Delta t}{C} \] (24)

The voltage ripple of each capacitor is \( \Delta V_{C1}/V_{C1} \), \( \Delta V_{C2}/V_{C2} \), \( \Delta V_{C3}/V_{C3} \) and \( \Delta V_{C4}/V_{C4} \), and each capacitance value can be obtained as
\[ C_i = \frac{(1-D_i)}{2D_i^2\Delta V_{C_i}/f_s} \frac{I_H}{V_H} \] (25)
According to (36), the voltage gain in the step-down mode \( G_{\text{step-down}} \), the relationship between the duty cycle \( D_3 \) and the turns ratio \( n \) is shown in Fig. 9.

2. Voltage Stress Analysis of Components

According to the switching sequence in step-down mode, the voltage stress relative to S1, S2, S3 and S4 can be expressed as

\[
V_{\text{stress,peak,S1}} = V_H - \frac{n}{1-D_1} V_L
\]

\[
V_{\text{stress,peak,S2}} = V_H - \frac{n}{1-D_1} V_L
\]

\[
V_{\text{stress,peak,S3}} = \frac{1}{1-D_3} V_L = \frac{1}{n} V_H
\]

\[
V_{\text{stress,peak,S4}} = \frac{1}{1-D_4} V_L = \frac{1}{n} V_H
\]

(37) (38) (39) (40)

According to Kirchhoff’s current law (KCL) and ampere-second balance, the peak current relative to S1, S2, S3 and S4 can be expressed as

\[
I_{d1,\text{peak}} = \frac{2}{D_3} I_L
\]

\[
I_{d2,\text{peak}} = \frac{D_3}{1-D_3} I_L + \frac{D_3}{2L_{n1}} f_s V_L
\]

\[
I_{d3,\text{peak}} = \frac{2-D_3}{nD_3} I_L
\]

\[
I_{d4,\text{peak}} = \frac{1}{n(1-D_4)} I_L
\]

(41) (42) (43) (44)

3. Magnetic Components Design

The maximum and minimum current of the magnetic components \( L_{n1} \) can be calculated by

\[
i_{L_{n1,\text{max}}} = i_{L_{n1,\text{avg}}} + \frac{\Delta i_{L_{n1}}}{2}
\]

And

\[
i_{L_{n1,\text{min}}} = i_{L_{n1,\text{avg}}} - \frac{\Delta i_{L_{n1}}}{2}
\]

(45) (46)

The ripple current and average current of \( L_{n1} \) can be determined by

\[
\Delta i_{L_{n1}} = \frac{V_{L_{n1}}}{L_{n1}} DT_s = \frac{(1-D_1)D_1}{L_{n1}} f_s n V_H
\]

And

\[
i_{L_{n1,\text{avg}}} = \frac{n}{2(1-D_1)D_1} I_H
\]

(47) (48)

When the current \( i_{L_{n1,\text{min}}} \) is equal to zero, the magnetic components are operated in boundary conduction mode (BCM). Substituting (47) and (48) into (46), the current \( i_{L_{n1,\text{min}}} \) can be expressed as

\[
i_{L_{n1,\text{min}}} = 0 = \frac{n}{2(1-D_1)D_1} I_H - \frac{(1-D_1)D_1}{2L_{n1}} f_s n V_H
\]

And

\[
L_{n1,\text{BCM}} = \frac{(1-D_1)^2 D_1^2}{n^2 f_s n} V_H
\]

(50)

Under this conditions of the high voltage side is 400 V, the current of high voltage side \( I_{H,\text{BCM}} \) is 0.1875 A, the switching frequency \( f_s \) is 40 kHz and the turns ratio \( n \) is 4, the result of substituting (50) is shown in Fig. 10. When the value of \( L_{n1} \) is greater than the BCM curve, \( L_{n1} \) is operated in CCM; otherwise, it is operated in DCM.

![Figure 10. The curve of \( L_{n1,\text{BCM}} \) in step-down mode.](image)

4. Efficiency Analysis of Components

The total power losses of the proposed converter can be expressed as

\[
P_{\text{Loss}} = P_{L_{1,\text{loss}}} + P_{L_{2,\text{loss}}} + P_{L_{3,\text{loss}}} + P_{L_{4,\text{loss}}} + P_{C_{1,\text{loss}}} + P_{C_{2,\text{loss}}}
\]

\[
+ P_{C_{3,\text{loss}}} + P_{C_{4,\text{loss}}} + P_{C_{1,\text{loss}}} + P_{C_{2,\text{loss}}} + P_{C_{3,\text{loss}}} + P_{C_{4,\text{loss}}}
\]

(51)

The non-ideal conversion efficiency \( \eta_{\text{step-up}} \) and \( \eta_{\text{step-down}} \) can be determined by

\[
\eta_{\text{step-up}} = \frac{P_H}{P_L + P_{\text{Loss}}}
\]

And

\[
\eta_{\text{step-down}} = \frac{P_L}{P_L + P_{\text{Loss}}}
\]

(52) (53)

And the non-ideal voltage gain of the converter can be calculated as

\[
G_{\text{step-up}} = \eta_{\text{step-up}} \times \frac{n}{1-D_1}
\]

And

\[
G_{\text{step-down}} = \eta_{\text{step-down}} \times \frac{1-D_3}{n}
\]

(54) (55)

As shown in Fig. 11(a)-(d), substituting the conduction losses of the component into (52)-(55), it can be concluded that when the load increases, the non-ideal voltage gain and non-ideal efficiency will continue to decrease. The specifications of the proposed converter used in these figures have been assumed to be \( V_L = 48 \text{ V}, V_H = 400 \text{ V}, n = 4, r_{d1} = r_{d2} = 5.9 \text{ m\Omega}, r_{d3} = r_{d4} = 190 \text{ m\Omega}, r_{C1} = r_{C2} = 50 \text{ m\Omega}, r_{C3} = r_{C4} = 500 \text{ m\Omega} \) and \( r_{L1} = r_{L2} = r_{L3} = 50 \text{ m\Omega} \).
IV. EXPERIMENTAL DESIGN AND RESULTS

The common battery voltage is about 48V, and the DC bus voltage is about 400V. Therefore, the recommended converter design parameters are 48V for the low-side voltage $V_L$ and 400V for the high-side voltage $V_H$. The magnetic component is designed to be 15% of the full load of the BCM, where $I_H = 0.1875\text{A}$ and $I_L = 1.5624\text{A}$. The maximum allowable voltage ripple of $C_1$ and $C_2$ is 10% generally, and the high-side capacitors $C_3$ and $C_4$ are 1%. In addition, the electrical specifications of the recommended topology are shown in TABLE I. The photograph of the proposed bidirectional converter is shown in Fig. 12. The microcontroller is dsPIC30F4011 and the type of controller is PI controller.

![Figure 12. Photograph of the proposed topology, (a) main circuit, and (b) control circuit.](image)

| Parameter                  | Specification |
|----------------------------|---------------|
| High-side power $P_H$      | 500 W         |
| Low-side power $P_L$       | 500 W         |
| High-side voltage $V_H$    | 400 V         |
| Low-side voltage $V_L$     | 48 V          |
| Switching frequency $f_s$ | 40 kHz        |
| Power switches $S_1$ and $S_2$ | IRFP4568PbF |
| Power switches $S_3$ and $S_4$ | NTHL190N65S3HF |
| Magnetizing inductance $L_{m1}$ | 208 $\mu$H |
| Leakage inductance $L_{k1}$ and $L_{k2}$ | 2 $\mu$H |
| Capacitor $C_1$ and $C_2$  | 100 $\mu$F    |
| Capacitor $C_3$ and $C_4$  | 47 $\mu$F     |
| Turns ratio $n$            | 4             |

![Figure 11. Non-ideal of the proposed topology in step-up mode (a) voltage gain and (b) efficiency, and non-ideal of the proposed topology in step-down mode (c) voltage gain and (d) efficiency.](image)
Figure 13. Experimental results of proposed topology in the step-up mode at full load of 500 W. (a) Waveforms of \( V_{gs1}, V_{gs2}, i_{ds1} \) and \( i_{ds2} \), (b) \( V_{ds} \) and \( i_{ds} \) of S1 and S2, (c) \( V_{ds} \) and \( i_{ds} \) of S3 and S4, and (d) Voltage of C1, C2, C3 and C4, (e) \( V_{ds} \) and \( i_{ds} \) of S1 and S2 in one switching cycle.

In Fig. 13(a)-(e), the key waveforms measured in the step-up mode at a full load of 500 W. Fig. 13(a) is the complementary signal of \( V_{gs1} \) and \( V_{gs2} \), and the measured waveforms of leakage inductance \( L_{ds1} \) and \( L_{ds2} \). The measured waveforms of \( V_{ds} \) and \( i_{ds} \) of switches S1 and S2 are shown in Figure 13(b). The measured current waveforms \( i_{ds1} \) and \( i_{ds2} \) show that the voltage stress of switches S1 and S2 have ZVS in the step-up mode. In Fig. 13(c), there are measured waveforms of \( V_{ds} \) and \( i_{ds} \) of switches S3 and S4. The measured current waveforms \( i_{ds3} \) and \( i_{ds4} \) show that the voltage stress of switches S3 and S4 is the high-side voltage \( V_{ds} \) 400V. Fig. 13(d) shows the measured waveforms of the voltages of capacitors C1, C2, C3, and C4 in the proposed topology. It can be known that the sum of the voltages of C3 and C4 is the high-side voltage \( V_{ds} \) 400 V. In Fig. 13(e), shows the soft switching measurement waveforms of \( V_{ds} \) and \( i_{ds} \) of S1 and S2 in one switching cycle.

S2 are shown in Fig. 14(b). The measured current waveforms \( V_{ds1} \) and \( V_{ds2} \) show that the voltage stress of switches S1 and S2 is equal to 100 V. In Fig. 14(c), there are measured waveforms of \( v_{ds} \) and ids of switches S3 and S4. The measured current waveforms \( i_{ds3} \) and \( i_{ds4} \) show that switches S3 and S4 have ZVS in the step-down mode. Fig. 14(d) shows the voltage measurement waveforms of capacitors C1, C2, C3, and C4 in the proposed topology. It can be seen that all capacitor voltages are constant. In Fig. 14(e), shows the soft switching measurement waveforms of \( V_{ds} \) and ids of S3 and S4 in one switching cycle.

The conversion efficiency of step-up mode and step-down mode are shown in Fig. 15, respectively. In the step-up mode, the highest conversion efficiency point is 96.8% operated under 100 W-150 W. In the step-down mode, the highest conversion efficiency point is 96.2% operated under 100 W-200 W.

Figure 15. Efficiency of the proposed converter in step-up and step-down mode.

In addition, calculate the conduction losses of each component according to the equations in (52)-(55). Fig. 16(a) and Fig. 16(b) shows the losses in step-up mode and step-down mode at full load of 500 W, respectively. It can be known that in the step-up mode, the high-side voltage switches cause larger conduction losses due to the forward voltage of the body diode. In the step-down mode, the conduction losses of the switches are greatly reduced due to the use of synchronous rectification technology.

Figure 16. Conduction losses distribution (a) in step-up mode, and (b) in step-down mode.

To verify the performance and understand the advantages and disadvantages of the proposed topology, compare the number of components of a different...
bidirectional converters, the complexity of the PWM signal and the voltage gain, etc. In TABLE II, a comparison with other bidirectional converters [7], [8], [20] and [21] is summarized.

Table II. The Comparison of Related Literatures on Bidirectional Converters

| Item / Ref. | [7] | [8] | [20] | [21] | Proposed Converter |
|-------------|-----|-----|------|------|--------------------|
| $G_{\text{step-up}} (V_H/V_L)$ | $\frac{2 + D}{1 + D}$ | $\frac{3}{1 + D}$ | $nD$ | $\frac{2nD}{1 - D}$ | $\frac{n}{1 + D}$ |
| $G_{\text{step-down}} (V_L/V_H)$ | $\frac{D}{1 - D}$ | $\frac{D}{3}$ | $\frac{D}{n(1 - D)}$ | $\frac{D}{2n(1 - D)}$ | $\frac{1 - D}{n}$ |
| MOSFETs | 5 | 8 | 4 | 4 | 4 |
| Magnetic components | 2 | 3 | 2 | 3 | 1 |
| Capacitors | 6 | 6 | 2 | 4 | 4 |
| Diodes | 0 | 0 | 1 | 6 | 0 |
| PWM Control | Normal | Complex | Complex | Normal | Normal |
| Output power | 400 W | 800 W | 600 W | 400 W | 500 W |
| Isolated | No | No | Yes | Yes | Yes |

Figure 17. Comparison of the voltage gain (a) in step-up mode, and (b) in step-down mode.

The conversion efficiency of the proposed topology and the topology proposed in [7], [8], [20] and [21] are compared in the step-up mode and the step-down mode, respectively, as shown in Fig. 18(a) and Fig. 18(b). In [7] and [8], in order to increase the voltage gain ratio, excessive component losses are caused and the conversion efficiency is reduced. The best topology is [20], which has higher conversion efficiency in step-down mode, but its disadvantage is the low voltage gain ratio. The highest overall voltage gain ratio is [21], but the circuit components are also the most, so higher conversion efficiency cannot be achieved. Overall, the conversion efficiency of the converter proposed in this thesis has good performance in step-up mode and the step-down mode, respectively, and the proposed topology has a higher voltage gain ratio.

Figure 18. Comparison of efficiency (a) in step-up mode, and (b) in step-down mode.

In Fig. 19(a) and (b) shows the step variation of output load of proposed topology in step-up mode and step-down mode. The $V_L$ is 48 V and the $V_H$ is 400 V. While the output load is step changed between half load and full load. It can be seen that the output voltage ($V_H/V_L$) is very stable and is not greatly affected by load changes.
This paper proposes a novel bidirectional isolated DC-DC converter. The proposed topology has the following advantages: (1) high voltage gain ratio and galvanic isolation; can be widely used in energy storage systems; (2) bidirectional energy transfer, the leakage inductance energy can be effectively recovered, and the main switch of the proposed topology has ZVS; (3) fewer components, greatly reducing development and design costs; (4) high conversion efficiency, which can reduce power conversion losses.

The topology proposed in this paper can be confirmed its feasibility and correctness through theoretical analysis, simulation and experimental results. In the implementation, it is concluded that the highest efficiency of the step-up mode or step-down mode are 96.8% and 96.4%, respectively.

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**Figure 20.** The input and output current ripple operated under load variation, (a) input current ripple, and (b) output current ripple.

**V. CONCLUSION**

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