Hardware Implementation of Fano Decoder for Polarization-adjusted Convolutional (PAC) Codes

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Abstract—This brief proposes a hardware implementation architecture for Fano decoding of polarization-adjusted convolutional (PAC) codes. This architecture uses a novel branch metric unit specific to PAC codes. The proposed decoder is tested on FPGA, and its performance is evaluated on ASIC using TSMC 28 nm 0.72 V library. The decoder can be clocked at 500 MHz and reach an average information throughput of 38 Mb/s at 3.5 dB signal-to-noise ratio for a block length of 128 and a code rate of 1/2.

Index Terms—PAC codes, sequential decoding, Fano, polar coding, VLSI.

I. INTRODUCTION

This brief presents a hardware implementation study of Fano decoding for polarization-adjusted convolutional (PAC) codes, which are a new class of error-correcting codes introduced in [1]. PAC codes combine ideas from polar coding [2] and convolutional coding and have been shown to perform near the dispersion approximation [3] in certain cases [1]. Fano decoding [4] is a depth-first tree search algorithm which was originally developed for convolutional codes. PAC codes can be decoded using any tree search algorithm such as depth-first, breadth-first, and beam (constrained breadth-first) search algorithms.

Depth-first search decoders for convolutional codes are in general known as sequential decoding [5] algorithms. Two well-known sequential decoders are Fano and stack algorithms [6], [7]. Compared to stack algorithm, Fano decoder requires a smaller memory size and is more suitable for hardware implementations. For this reason, in this brief, we focus on the Fano version of sequential decoding. Various architectures for hardware implementation of sequential decoding of convolutional codes have been reported in the literature [8]–[11], but to the best of the author’s knowledge, the suitability of sequential decoding for PAC codes has never been studied from a hardware implementation perspective. Motivated by this, we implement a Fano decoder for PAC codes by introducing a new hardware-friendly variant of Fano algorithm for PAC codes and designing a novel branch metric unit capable of calculating the current and previous branch metrics without requiring any storage element or comparator.

Despite its near-optimal performance, PAC codes under sequential decoding exhibit variable time complexity, resulting in variable decoding latency. Although the depth-first search algorithms have variable search complexity, their average search complexity is low at a high signal-to-noise ratio (SNR) regime. On the other hand, breadth-first search algorithms have fixed but higher search complexity. List decoding [12] of PAC codes is an example of beam search decoder. However, the list decoder requires a large list size to achieve the error-correction performance of the PAC sequential decoder.

Throughout this brief, we denote vectors by boldface letters. For any set $A \subseteq \{0, 1, \ldots, N-1\}$, we denote its complement by $A^c = \{i : i \notin A\}$. For any vector $y$ and set $A$, $y_A$ denotes the sub-vector $(y_i : i \in A)$. For any vector $y$, $y^j = (y_0, y_2, \ldots, y_j)$. We define a sign function $s(l)$ such that $s(l) = 0$ if $l \geq 0$ and $s(l) = 1$, otherwise.

The rest of this brief is organized as follows. Section II gives a brief discussion of PAC codes. Section III introduces a new variant of Fano decoder for PAC codes. In Section IV we introduce a hardware architecture for Fano decoding of PAC codes. Implementation results of the proposed PAC Fano decoder are presented in Section V. Section VI concludes this brief.

II. PAC CODES

Fig. 1 shows a block diagram of PAC coding scheme. The data insertion block receives a source word $d$ of length $K$ and inserts it into a data carrier word $v$ of length $N$ in accordance with a data index set $A$ such that $v_A = d$ and $v_{A^c} = 0$. The bits fixed to zero are called frozen, whereas all the other bits are called non-frozen. The data carrier word $v$ goes through a convolution block with generator matrix $G$ which is a Toeplitz matrix whose first row is $c$ (the generator polynomial). The resulting word $u$ goes through a polar mapper and the overall encoding process of PAC codes can be expressed by $x = vGF^{\otimes n}$, where $F^{\otimes n}$ is the generator matrix of polar codes with $F^{\otimes n}$ being the $n$-th Kronecker product of the kernel matrix $F = [1]$.

At the receiver side, the PAC decoder receives the channel output $y$ and generates an estimate $\hat{v}$ of $v$. Then, a data extractor extracts an estimate $\hat{d}$ of $d$ from $\hat{v}$ using $\hat{d} = v_A$. The performance of the system is measured by the probability of frame error $P_e = P(d \neq \hat{d})$. A PAC sequential decoder

Fig. 1. PAC coding scheme.

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consists of two blocks: polar demapper and sequential decoder. The polar demapper receives the channel output $y$ and calculates a log-likelihood ratio (LLR) vector $l$. Then, based on the prior bit-estimates $\hat{u}^{i-1}$ received from sequential decoder, it generates the demapped LLR value $z_i \triangleq \ln \frac{P(y,u^{i-1}|u_i=0)}{P(y,u^{i-1}|u_i=1)}$ of $i$th bit. Polar demapper operates similar to successive cancellation (SC) decoder of polar codes with a difference that the polar demapper does not generate any bit-estimate output $\hat{u}_i$. Instead, it receives the prior bit-estimates $\hat{u}^{i-1}$ from the sequential decoder and passes back the soft value of $z_i$. The sequential decoder uses $z_i$ to calculate a path metric which helps the decoder to generate an estimate $\hat{v}$ of $v$.

### III. Fano Algorithm for PAC Codes

Fano algorithm uses a path metric and a metric threshold $T$ to identify the correct path in the code tree. The threshold can only take integer multiples of threshold spacing $\Delta$. If the path metric grows along a given path, the algorithm considers it as a correct path and continues to search further along it. But if the metric drops significantly, the algorithm moves back (backtracks) and searches other paths. Upon a backward move, if the currently reached node is frozen or all of its children are examined, the decoder moves back one more. An extensive study of the Fano decoder may be found in [13].

Fig. 2 shows a local node diagram of the Fano decoding tree. Assume that $N1$ is the current node, $N2$ is the most likely node (with larger metric), $N3$ is the least likely node (with smaller metric), and $N4$ is the previous node. $M2$ and $M3$ denote the metrics of branches from current node to $N2$ and $N3$, respectively, and $M1$ is the metric of the branch from previous node to the current node. To avoid branch metric overflow, we use relative branch metric computation instead of absolute branch metric value [8]. Adopting this method lets the current node’s branch metric be zero and all other branch metrics relative to the current node’s metric.

We modify the conventional Fano algorithm to make it suitable for decoding PAC codes and state it as the following set of rules. We define a variable $\Psi$ such that $\Psi = 1$ when the Fano decoder backtracks to a frozen node or to a node whose both children are examined; otherwise, $\Psi = 0$. $N23$ is a node that corresponds to $N2$ when the most likely node is being examined or $N3$ when the least likely node is being examined. Similarly, $M23$ corresponds to $M2$ when $N2$ is being examined or $M3$ when $N3$ is being examined. A node is considered as a new node if it is being visited for the first time.

- **Rule 0**
  
  **Conditions:** $\Psi = 0$, $N23$ is new node, $M23 \geq T$.

- **Rule 1**
  
  **Conditions:** $\Psi = 0$, $N23$ is old node, $M23 \geq T$.
  
  **Actions:** Move to $N23$, update $T$ to $T + \Delta - M23$, examine the most likely node leading from $N23$ at the next step.

- **Rule 2**
  
  **Conditions:** $\Psi = 0$, $M23 < T$, $N1$ is root node; or $\Psi = 0$, $M23 < T$, $N1$ is not root node, $M1 + T > 0$; or $\Psi = 1$, $N1$ is root node; or $\Psi = 1$, $N1$ is not root node, $M1 + T > 0$
  
  **Actions:** Make no move, update $T$ to $T - \Delta$, assign $\Psi = 0$, examine $N2$ again at the next step.

- **Rule 3**
  
  **Conditions:** $\Psi = 0$, $M23 < T$, $N1$ is not root node, $M1 + T \leq 0$, $N4$ is not frozen, $N1$ is the most likely node leading from $N4$; or $\Psi = 1$, $N1$ is root node, $N4$ is frozen, $N1$ is the most likely node leading from $N4$.
  
  **Actions:** Move to $N4$, update $T$ to $T + M1$, assign $\Psi = 0$, examine the lateral node of $N1$ at the next step.

- **Rule 4**
  
  **Conditions:** $\Psi = 0$, $M23 < T$, $N1$ is not root node, $M1 + T \leq 0$, $N4$ is frozen or $N1$ is the least likely node leading from $N4$; or $\Psi = 1$, $N1$ is root node, $N4$ is frozen or $N1$ is the most likely node leading from $N4$.
  
  **Actions:** Move to $N4$, update $T$ to $T + M1$, assign $\Psi = 1$, perform backward check at the next step.

Fig. 3 shows the corresponding flowchart of the Fano decoder. Note that whenever $\Psi = 1$, the Fano algorithm performs a backward check and does not require any new $z_i$ value. Thus, by storing the previously generated $z_i$ values, we can avoid activating the polar demapper when $\Psi = 1$ and significantly reduce the decoder’s latency (especially at low SNR regime).

### IV. Architecture of Fano Decoder for PAC Codes

Fig. 4 shows the hardware architecture of the proposed PAC Fano decoder. The input buffer stores the channel output LLR values, and the output buffer stores the final estimate $\hat{v}$ of $v$. The Fano control unit (FCU) implements the flowchart of Fig. 3. The branch metric unit (BMU) is responsible for providing the FCU with the current branch metric $M23$ and previous branch metric $M1$. Vreg is a bidirectional shift register used to store the prior convolution input estimates $\hat{v}$. Whenever the Fano decoder moves forward, the current

![Fig. 2. Fano decoding tree, reproduced from [8].](image-url)

![Fig. 3. Flowchart of Fano rules.](image-url)
convolution input estimate \( \hat{v}_i \) is stored in Vreg. To allow a maximum backtracking depth of \( N \), the size of Vreg is chosen to be \( N + h \), where \( h \) is the memory size of the convolution. The first \( h \) part of Vreg provides the convolution state (CS) for the BMU. The Ureg register is used to store the prior convolution output estimates \( \hat{u} \). When the Fano decoder moves forward, depending on the proceeding branch, the corresponding \( \hat{u}_i \) is stored in the Ureg. A clock cycle (CC) counter is used to count the number of clock cycles consumed for decoding a single codeword. The decoding of a codeword is terminated whenever the value of the CC counter exceeds a predefined maximum cycle (MC). In this case, a timeout (TO) is terminated whenever the value of the CC counter exceeds a maximum backtracking depth of \( N \) and corresponding registers and implement the bit-estimates \( \gamma_i \) and \( \gamma_i (0) \) for decoding a single codeword. The decoding of a codeword \( \hat{u} \) moves forward, depending on the proceeding branch, the prior convolution output estimates \( \hat{u}_i \), \( \hat{u}_i = 1 \) for non-frozen nodes (\( i \in A' \)) and \( a_i = 1 \) for frozen nodes (\( i \in A \)).

To implement the polar demapper (PD), we adopt the FFT-like architecture of [14] and apply the following modifications to make it operate as a polar demapper: 1) We remove the decision unit and pass the soft values of LLR vector \( z \) to the output; 2) We remove the bit-estimates update unit and corresponding registers and implement the bit-estimates update network using a combinational circuit that receives \( \hat{u} \) from Ureg and updates the intermediate bit-estimates; 3) We modify the bit-reversal architecture of [14] to output the LLR values in a natural order. Despite the similarity in architecture, the timing schedule of PD is different from the one of SC decoder. Once the PD generates the LLR value of a node \( z_i \), it remains idle until another node LLR value is requested. Note that the next LLR value request may be for the immediate forward node or any other backward node. Hence, the PD must be able to follow the Fano algorithm whenever it backtracks. To fulfill this requirement, all the intermediate LLR values are required to be stored and kept until the end of each decoding session. The FFT-like architecture of [14] uses distributed registers to stores the intermediate LLR values. Any SC decoder that is capable of storing the intermediate LLR values can be used as a polar demapper.

The BMU block is a fundamental block which makes the Fano decoding of PAC codes different from Fano decoding of convolutional codes. The metric function that BMU of PAC Fano decoder uses must be compatible with the polarized channel (created by the polar mapper and demapper) seen by the convolution block of PAC codes. For PAC codes, the well-known branch metric function of Fano [4], [15] becomes

\[ \gamma_i(\hat{u}_i) = \log_2 \frac{P(y, \hat{u}^{i-1}|\hat{u}_i) + b_i}{P(y, \hat{u}^{i-1}|\hat{u}_i = 1)} - b_i, \]  

where \( P(y, \hat{u}^{i-1}|\hat{u}_i) \) and \( P(y, \hat{u}^{i-1}) \) are transition and output probabilities of the \( i \)th bit-channel, respectively, and \( b_i \) is a bias term. For a binary input channel with uniform input distribution, we have

\[ P(y, \hat{u}^{i-1}) = \frac{1}{2} \left[ P(y, \hat{u}^{i-1}|\hat{u}_i = 0) + P(y, \hat{u}^{i-1}|\hat{u}_i = 1) \right]. \]  

By using (2) and dividing the numerator and denominator of the fractional part of (1) by \( P(y, \hat{u}^{i-1}|\hat{u}_i) \), after some calculus, we obtain

\[ \gamma_i(\hat{u}_i) = 1 - \log_2 (1 + e^{-1 - 2\gamma_i} |z_i|) - b_i, \]  

where \( z_i \) is the output of PD. To obtain a hardware-friendly version of (3), we apply the approximation \( \log_2 (1 + e^{-1 - 2\gamma_i} |z_i|) \approx 0 \), if \( \hat{u}_i = s(z_i) \), and \( \log_2 (1 + e^{-1 - 2\gamma_i} |z_i|) \approx |z_i| \), otherwise, and obtain

\[ \gamma_i(\hat{u}_i) = \begin{cases} 1 - b_i, & \text{if } \hat{u}_i = s(z_i), \\ 1 - |z_i| - b_i, & \text{otherwise}. \end{cases} \]  

To simplify (4) further, we assume \( b_i \) can take only binary values. As a result, we can tabulate \( \gamma_i(0) \) and \( \gamma_i(1) \) for all the possible values of \( b_i \) and \( s(z_i) \) in Table I.

| \( s(z_i) \) | \( b_i \) | \( \gamma_i(0) \) | \( \gamma_i(1) \) |
|---|---|---|---|
| 0 | 0 | 1 | 1 - |z_i|
| 0 | 1 | 0 | |z_i|
| 1 | 0 | 1 - |z_i| |z_i|
| 1 | 1 | -|z_i| |z_i|

We can implement this table using two 4-to-1 multiplexers and one adder. Fig. 5 shows the hardware implementation of Table I (metric calculator). The number of quantization bits for LLRs is denoted by \( Q \). The metric calculator receives \( z_i \) and \( b_i \) and generates the branch metric \( \gamma_i(\hat{u}_i) \) for the two possible values of \( \hat{u}_i = 0 \) and \( \hat{u}_i = 1 \). The constant ’0’ and ’1’ inputs to the adder and multiplexers are padded with zeros to have \( Q \)-bit width (not shown in the figure for clarity).

Fig. 5 shows the hardware diagram of BMU, which uses two metric calculator blocks to generate the current and previous branch metrics. With a careful observation of Table I, we realize that \( \gamma_i(0) \geq \gamma_i(1) \) when \( s(z_i) = 0 \) and \( \gamma_i(0) \leq \gamma_i(1) \) when \( s(z_i) = 1 \). Hence, the most likely branch can be
Fig. 6. Hardware diagram of branch metric unit (BMU).

distinguished from the least likely branch without using an actual comparator. The input $t_i$ is provided by FCU and is used to request the most likely branch metric (M2) when $t_i = 0$ or the least likely branch metric (M3) when $t_i = 1$ from BMU. Additionally, when the current node N1 is frozen (i.e., $a_i = 0$) the BMU is forced to output the branch metric which corresponds to $\hat{v}_i = 0$. We use a convolutional encoder to generate $u_{i,0}$ which is the convolution output for the assumption $\hat{v}_i = 0$. In addition to M1 and M23 metrics, the BMU block provides FCU with the selected branch $\hat{v}_i$ and its corresponding convolution output $\hat{u}_i$.

V. IMPLEMENTATION RESULTS

In this section, FPGA and ASIC implementation results of the proposed PAC Fano decoder are presented for block length $N = 128$ and message length $K = 64$. We use $Q = 7$, $\Delta = 2$, $e = (1, 0, 1, 1, 0, 1, 1)$, and choose $A$ according to the Reed-Muller scoring rule as explained in [1]. We use the hard quantized (1-bit quantization) values of bit-channel capacities [16] as the bias vector $b$. The channel output LLR values are calculated at $E_b/N_0 = 3.5$ dB.

A. FPGA Implementation Results

The proposed PAC Fano decoder is successfully implemented onto Xilinx Nexys 4 Artix®-7 (28 nm) FPGA. The place-and-route results show that the decoder uses 16443 lookup tables (LUTs) and 8306 registers. To evaluate the FER performance and measure the search complexity of the PAC Fano decoder, using MATLAB® software, pseudorandom messages are generated, encoded, modulated using a binary phase-shift keying (BPSK) modulator, and transmitted to FPGA after white Gaussian noise is added. The decoded carrier word $\hat{v}$ is received from FPGA, $d$ is extracted from $\hat{v}$ using $d = \mathbf{v}_A$, and compared with the actual transmitted message $d$. Also transmitted by the FPGA is the number of clock cycles consumed to decode each codeword which is measured by the CC counter.

Fig. 7 (left) plots the FER performance of the proposed PAC Fano decoder for different MC values. The FER performance of software implementation of original PAC codes reported in [1] and the dispersion approximation are also plotted in this figure. As expected, increasing the value of MC allows the Fano algorithm to perform more searches and maintain better FER performance. With MC = 2^18, the proposed PAC Fano decoder obtains a FER performance close to the FER performance of software implementation at high SNR regime; At $E_b/N_0 = 3.5$ dB the decoder achieves FER = $1.6 \times 10^{-5}$. The performance loss is majorly due to the quantization of LLRs and approximation of the Fano metric. In low SNR regime, the metric approximation error is large since the term $\log_2(1 + e^{-1-2a_i})$ diverges from $|z_i|$ as SNR decreases. But as SNR increases, this error becomes negligible.

Fig. 7 (right) shows the average number of clock cycles consumed by the decoder for decoding a single codeword for different MC values. The effect of MC value on average CC is significant at low SNR regime; as SNR increases, this effect fades out. This is due to the Pareto distribution of Fano decoder’s search complexity such that for high SNR values, only a small fraction of codewords require a very large search complexity [17]. With MC = 2^14, the average number of CCs per codeword drops by 51% at $E_b/N_0 = 1$ dB at a cost of FER performance drop at high SNR values (significantly at $E_b/N_0 = 3.5$ dB). At $E_b/N_0 = 3.5$, regardless of MC value, the decoder consumes an average of approximately 840 CCs to decode a single codeword. It is worth mentioning that for a noise-free channel (when no backtracking is done), the proposed PAC Fano decoder consumes 638 CCs which corresponds to $5N - 2$ CCs, of which $2N - 2$, $2N$, and $N$ is consumed by PD, FCU, and BMU, respectively.

B. Post-Synthesis Results

Table I lists the post-synthesis results of the proposed PAC Fano decoder using Cadence® Innovus™ Implementation System with TSMC 28 nm 0.72 V library. We present the results for the PAC Fano decoder with MC = 2^18. The decoder occupies an area of 0.059 mm^2 and can operate at 500 MHz consuming 3.85 mW power. The power value is estimated with Cadence® Voltus™ IC Power Integrity Solution using 10^4 pseudorandom input vectors. The performance values are reported at $E_b/N_0 = 3.5$ dB, and the average values are
calculated from $10^7$ decoding trials. The average information throughput (TP) of the decoder is estimated using $TP = (f_{clk}/\text{ACC}) \times K$, where $f_{clk}$ is the operating frequency and ACC is the average number of CCs consumed for decoding a frame and is obtained from Fig. 7. The worst-case (W.-C.) latency of the decoder is determined by the value of MC. The proposed PAC Fano decoder reaches an average information throughput of 38.1 Mb/s with an average latency of 839 CCs (1.68 µs).

### Table II

| Technology          | 28 nm |
|---------------------|-------|
| N                   | 128   |
| K                   | 64    |
| Supply Voltage (V)  | 0.72  |

| Frequency (MHz)     | 500   |
|---------------------|-------|
| Area (mm²)          | 0.059 |
| Power (mW)          | 3.85  |

| Avg. Info. TP† (Mb/s) | 38.1  |
|-----------------------|-------|
| W.-C. Info. TP* (Mb/s)| 0.12  |
| Avg. Latency† (µs)    | 1.68  |
| Avg. Latency (CCs)    | 839   |
| W.-C. Latency (µs)    | 524   |
| W.-C. Latency (CCs)   | 218   |

| Area Efficiency† (Mb/s/mm²) | 646 |
|----------------------------|-----|
| Power Density (W/mm²)      | 0.065 |
| Energy Efficiency† (PJ/bit)| 101 |

†Average value at $E_b/K_0 = 3.5$ dB.

### VI. Conclusion

In this brief, we proposed a hardware architecture for Fano decoding of PAC codes. We introduced a new variant of Fano algorithm suitable for decoding PAC codes. We also introduced a novel branch metric unit specific to PAC codes that can be implemented using simple logic gates. Post-synthesis results showed that the decoder could provide an average information throughput of approximately 38 Mb/s at 3.5 dB with a power consumption of 3.85 mW and an area of 0.059 mm² for a block length of 128 and a code rate of 1/2. Due to its backtracking feature, the PAC Fano decoder has lower throughput than the state-of-the-art polar decoders (such as decoders of [18]), but it exhibits better FER performance. Because of their excellent FER performance at short block lengths and low encoding complexity, one of the potential use cases of PAC codes could be the Internet of Things (IoT), for which reliable communication is of great interest and low throughput and high decoding latency is tolerable.

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