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CRM PFC Converter with New Valley Detection Method for Improving Power System Quality

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Abstract: High efficiency and the power factor of power converters are very important factors which can improve power system quality. In particular, research on improving low efficiency and the power factor at light-load conditions is essential. A boost power factor correction (PFC) is most commonly used in home appliances, with several operations being at light-loads; the critical conduction mode (CRM) control, fixed ON-time control, and valley detection technique are mainly applied to PFC control. However, these control schemes have the following problems: (1) low efficiency, due to sudden increase in switching frequency at light-loads; and (2) low power factor, due to switching ON-time limitation. This paper presents a new valley detection method that can actively extend the fixed ON-time to overcome these problems. Furthermore, a new valley point detection circuit and an ON-time extension signal generation circuit are proposed and described in detail. The superiority of the proposed method is demonstrated via comparison with two existing CRM PFC control methods, namely fixed ON-time (conventional#1) and existing valley detection (conventional#2) methods. Experimental results at 20% load demonstrate that the proposed method shows an efficiency improvement of 2.1%, compared with the fixed ON-time strategy; and a power factor improvement of 34.9%, compared with the existing valley detection strategy.

Keywords: power quality; valley detection; PFC; CRM; efficiency; power factor; light-load

1. Introduction

Nowadays, conventional TVs are being replaced with smart TVs, and the usage of TVs has expanded from merely viewing purposes, to becoming media equipment. Smart TVs have built-in smart home hubs, that can monitor and control other Internet-of-things devices with existing TV functions. In other words, smart TVs have become a multiscreen to be connected to and operated with various devices, e.g., PCs, mobile phones, USBs, HDDs, Internet, etc., and watching is not necessitated. This means that a smart TV consumes more power than standby power, even if it is not operated as a conventional TV. In addition, owing to the rapid expansion of smart TVs, the efficiency and power factor at light-load can deteriorate the power system quality. Therefore, it is important to enhance the efficiency and power factor not only in heavy-load conditions, but also in light-load conditions for improving the power system quality.

In general, a 55-inch smart TV adopts a switch-mode power supply (SMPS) of approximately 200 W in consideration of power consumption, and the critical mode (CRM) boost power factor correction (PFC) topology is primarily adopted [1–3]. The CRM boost PFC can be implemented simply. However, the power conversion efficiency in relatively light-load conditions degrade, because the switching frequency increases in inverse proportion to the peak current level, which is decided by input voltage and load current [4–6].
To reduce switching loss in light-load and low-input-voltage conditions, the switching frequency is typically limited. The fixed ON-time method and switching frequency limit (SFL) method were suggested [7–9] to reduce switching loss under light-loads and low-input-voltages. The light-load efficiency can be improved to a certain level by limiting switching frequency. However, the power factor decreases due to the large current distortion that occurs when switching frequency is limited in light-load and low-input-voltage conditions. Additionally, a valley switching strategy has been proposed to improve the efficiency and power factor [10–16]. The existing valley switching strategy can reduce the switching loss by switching at the valley point generated during inductance and capacitance (LC) resonance, in contrast to the CRM method of switching when the diode current becomes zero. This is mainly implemented by setting the zero current detection time \( T_{zc} \) for the SFL. However, though maximizing the efficiency, this method inevitably causes an error in the accurate calculation of the switching point, i.e., the valley point, owing to the change in the LC resonance frequency. In addition, it is difficult to obtain a high power factor using this method because the switching frequency is limited in light-load and low-input-voltage conditions, such as SFL. Previous works [17–19] have analyzed interleaving CRM boost PFC and CRM Totem-Pole PFC. The interleaving method has an advantage, as it allows the efficiency to be improved to some degree in the full-load range. However, switching losses increase because the switching frequency increases rapidly in the light-load condition. Therefore, problems such as metal oxide semiconductor field effect transistors (MOSFETs) being damaged relatively frequently, have been reported. Furthermore, the cost increases, because more switches, gate drivers, and controllers are required due to the parallel structure. For this reason, the industry considers interleaving CRM PFC above 300 W, but it is common to use a single CRM PFC that can be implemented with low cost under 300 W.

Therefore, a new valley detection method including ON-time extension is presented herein to overcome the problems of the existing valley switching technique. The proposed new valley detection method detects the polarity crossing moment of the inductor current without an additional circuit. In addition, it senses the moment that the differentiation of the divided voltage “\( V_{VAL} \)” changes from negative to positive, to enable an error-free valley point detection. Furthermore, based on the collected information, the reference signal for the ON-time extension is then generated in the current signal generator. Consequently, the proposed method can reduce the switching loss by suppressing the increase in the switching frequency, and can improve the reduced power factor due to the fixed ON-time, using the extended ON-time strategy at light-load conditions. In addition, the problem of MOSFETs getting damaged in light-load conditions can be addressed by turning the gate on at zero current voltage using a timer, in this method. The actual circuit with the proposed strategy was implemented and tested on a 240 W SMPS for a 55-inch smart TV. In order to prove the superiority of the new valley detection method using the proposed ON-time extension technique, the two existing methods, i.e., fixed ON-time method, denoted “conventional\#1” [20]; and existing valley detection method, denoted “conventional\#2” [21], were selected as the comparison group. The experimental results were then derived, based on the comparison. Experimental results demonstrated an efficiency improvement of 2.1%, compared with the conventional CRM PFC; and a power factor improvement of 34.9%, compared with the switching frequency limiting strategy under a 20% load condition.

The remainder of the paper is organized as follows: Section 2 describes the existing CRM boost PFC and conventional valley detection methods in detail; Section 3 describes the new valley detection strategy proposed in detail; Section 4 introduces the implementation and design considerations of the proposed circuit; and Section 5 demonstrates the feasibility of the proposed strategy through simulation and experimental results.

2. Description for Conventional CRM boost PFC

The conventional PFC converter, as shown in Figure 1, is widely employed in the power supplies of TV systems, which converts an AC voltage to a DC voltage. The CRM is a method to control a PFC converter without sensing the input voltage \( V_{in} \), where the switch ON-time \( T_{on} \) is a constant
value to retain the output voltage \(V_{\text{out}}\) at a target value, and the average value of the inductor current \(I_L\) in a switching cycle, i.e., the input current of the PFC converter is proportional to \(V_{\text{in}}\), as shown in Figure 2 [20–24]. It was observed that the CRM boost PFC shows a reduced power conversion efficiency, because the switching frequency was increased significantly at the low-input-voltage or light-load condition.

![Basic topological structure of boost power factor correction (PFC) converter.](image1)

**Figure 1.** Basic topological structure of boost power factor correction (PFC) converter.

2.1. Switching Frequency Limit Method

To reduce switching loss in light-load and low-input-voltage conditions, i.e., short \(T_{\text{on}}\), it is typical to limit the switching frequency, as shown in Figure 3. The timing to turn the switch ON is delayed until a predetermined time passes from the previous point when the switch is turned ON, even though \(I_L\) returns to zero [5,25]. In this method, switching is reduced, but the average \(I_L\) in a period also changes with the switching frequency. Therefore, it is difficult to reduce the limit of the switching frequency without degrading the power factor. Furthermore, switching with a low peak of \(I_L\) is reduced, but still occurs when \(V_{\text{in}}\) is low. Such switching only consumes energy without contributing any energy transfer from the input to the output, as the energy stored in the inductor is insufficient to change the parasitic capacitance of the drain of the switch or to conduct the diode.

![Typical inductor current waveform of critical conduction mode (CRM) boost PFC control.](image2)

**Figure 2.** Typical inductor current waveform of critical conduction mode (CRM) boost PFC control.

![Inductor current waveform of CRM boost PFC control with constant frequency limit.](image3)

**Figure 3.** Inductor current waveform of CRM boost PFC control with constant frequency limit.
2.2. Existing Valley Switching Method

Additionally, the existing valley switching scheme, as shown in Figure 4, is widely known for reducing switching loss. After $I_L$ returns to zero, the drain–source voltage of the switch ($V_{ds}$) starts to decrease due to the resonance between the inductance of the inductor ($L$) and the drain–source parasitic capacitance of the switch ($C_{oss}$). Therefore, turning the switch ON at a valley of $V_{ds}$ is better than when $I_L$ returns to zero after a current through the diode stops, for efficiency.

![Figure 4. Drain–Source voltage waveform of CRM PFC control with existing valley detection method.](image)

To achieve this, a timer to measure a time equal to half the resonant frequency from when point $I_L$ reaches zero is widely used. The timer must be set depending on the resonant frequency from one converter to another; therefore, a pin for the setting is often assigned when such controllers are fabricated in ICs. However, the resonant frequency changes even in a converter, depending on the input voltage of the converter, because $C_{oss}$ contains the parasitic capacitance of a P–N junction in the MOSFET switch, which depends on the voltage applied to it. Furthermore, if we realize valley switching using the timer, even when a frequency limit function delays the timing for the switch to turn ON again, as shown in Figure 3, the timing of the valley must be estimated from the moment $I_L$ returns to zero after the current through the diode stops. The error of the timer against the resonant frequency accumulates. Therefore, this method is not practical when the number of valleys to be skipped before the switch turns ON is large.

3. Proposed Valley Detection Strategies with ON-Time Extension

In detail, this section describes the proposed valley detection strategies that can overcome the problems that arose with the CRM boost PFC converter that applied the existing valley detection method, as mentioned in Section 2. Figure 5 shows the inductor current applied to the proposed valley detection method. The detailed inductor current waveform at a light-load is compared with the conventional method, and is shown in Figure 6.

![Figure 5. Inductor current waveform of CRM boost PFC control with the proposed method.](image)
3.1. Realization of Proposed Method

To prevent switching without transferring energy from the input to the output, the ON-time of the switch is extended if the inductor current does not exceed a predetermined level. Simultaneously, the OFF-time should be extended when the average current in the cycle is the same as that when the ON-time is not extended; that is, when the switching period (T_{sw}) satisfies Equation (1).

\[
\int_{0}^{T_{sw}} I_L dt / T_{sw} = T_{ono} \times V_{in} / 2L
\]

where \(I_L\) is the inductor current, \(T_{sw}\) is the switching period, \(T_{ono}\) is the ON-time before it is extended, \(V_{in}\) is the input voltage, and \(L\) is the inductance.

A circuit to realize this control is shown in Figure 7. A ramp generator generates a ramp signal voltage \(V_{ramp}\), which begins to increase at the moment the switch turns ON. An error amplifier amplifies the difference between the voltage feedback signal from the PFC converter \(V_{FB}\) and a predetermined reference voltage \(V_{ref}\), and generates an output voltage \(V_{ea}\). \(V_{ramp}\) is compared with \(V_{ea}\), and the current sense signal from the PFC converter \(V_{CS}\) is compared with a voltage corresponding to the predetermined minimum level of the inductor current \(V_{csmin}\). An OFF trigger signal to turn the switch OFF is generated if \(V_{CS}\) is larger than \(V_{csmin}\) when \(V_{ramp}\) reaches \(V_{ea}\), similar to conventional CRM boost PFC converters.

![Figure 7. Circuit diagram of PFC control with proposed valley detection method with ON-time extension.](image-url)
first; this signal should be defined by each section, according to the levels of $V_{\text{ramp}}$ and $V_{\text{ea}}$, as shown in Figure 8. $I_{\text{int}}$ for each mode in Figure 8 is described as follows:

$$\text{Mode I (}0 \sim T_{\text{on}}\text{)}: I_{\text{int}} = 2K \cdot V_{\text{ramp}} - K \cdot V_{\text{ea}}$$  \hspace{1cm} (2)$$

$$\text{Mode II (}T_{\text{on}} \sim T_{\text{zcd}}\text{)}: I_{\text{int}} = K \cdot V_{\text{ramp}} - K \cdot V_{\text{ea}}$$  \hspace{1cm} (3)$$

$$\text{Mode III (}T_{\text{zcd}} - T_{\text{sw}}\text{)}: I_{\text{int}} = -K \cdot V_{\text{ea}}$$  \hspace{1cm} (4)$$

where $I_{\text{int}}$ is the output current generated by the current signal generator, $K$ is constant value which can be selected for easy circuit implementation, $V_{\text{ramp}}$ is ramp signal voltage, $V_{\text{ea}}$ is the generated output voltage, $T_{\text{zcd}}$ is the time when the inductor current returns to zero, and $T_{\text{sw}}$ is switching period. Here, for brevity, it is assumed that the ramp signal starts at 0 V.

![Figure 8. Detailed inductor current waveform for ON-time extension.](image-url)

3.2. Description of ON-Time Extension

At the moment when the switch turns ON, the reset switch discharges the capacitor. Subsequently, the capacitor generates a voltage corresponding to the integration of $I_{\text{int}}$. When the ON-time is extended, the voltage stored in the capacitor is larger than zero at the moment when the switch turns OFF, and is reduced by $I_{\text{int}} (-K \cdot V_{\text{ea}})$ subsequently. Finally, it reaches zero, and the comparator generates the ON trigger signal.

Figure 8 illustrates the waveforms when the ON-time is extended. During the ON-time, $I_L$ and $V_{\text{ramp}}$ continue increasing. Simultaneously, the capacitor integrates $I_{\text{int}}$, which is proportional to twice that of the difference between $V_{\text{ramp}}$ and $V_{\text{ea}}$. The switch is turned off when $I_L$ reaches a predetermined level ($I_{\text{Lmin}}$). Subsequently, $I_L$ decreases and returns to zero. During that time, the value of $V_{\text{ramp}}$ remains the previous value at the moment the switch turns OFF, and $I_{\text{int}}$ is proportional to the difference between $V_{\text{ramp}}$ and $V_{\text{ea}}$. After $I_L$ reaches zero (in fact, $I_L$ remains in resonance with a small amplitude, owing to the parasitic capacitance in this region; however, it is omitted for a simple illustration), the capacitor is discharged by $I_{\text{int}}$, which is a constant value depending on $V_{\text{ea}}$. When the voltage stored in the capacitor reaches zero, the switch is turned ON again, and the same operation in the previous period repeats. Here, it can be confirmed that the length of a period ($T_{\text{sw}}$) decided by integrating $I_{\text{int}}$ satisfies Equation (1), which describes a desirable operation. Additionally, the voltage between
the switches remain in resonance in the time period when $I_L$ remains in resonance; and $T_{sw}$ can be adjusted within a range of cycles of resonant frequency, by combining techniques typically employed in conventional PFC converters. For minimizing loss, it is better to delay the timing to turn ON the switch from $T_{sw}$, as calculated by Equation (1), to the next valley of $V_d$, where the loss from turning the switch ON is the smallest.

4. Circuit Implementations and Design Considerations

In this section, two methods of detecting the valley of $V_d$ in detail are examined, and the actual implementation circuitry for each method is described.

4.1. Proposed Valley Detect Method with Current Sense Voltage

One of the methods, involves the detection of the moment $V_{CS}$ crosses zero, from positive to negative. In this case, no additional external component is necessary, but the $V_{CS}$ in the resonant region of $V_d$ is typically small, and noise should be considered. Figure 9a shows a circuit to detect the zero-cross of $V_{CS}$, where an offset cancel topology is employed to avoid the effect transistor mismatch in detecting small voltages. When valley detection is not required, the switches controlled by $DET_b$ turn ON, and the voltage corresponding to the condition $V_{CS} = 0$ is stored to the capacitor $C_{hold}$. In detecting the valley, the switch controlled by $DET$ turns ON, and the voltage depending on $V_{CS}$ is compared with the voltage stored in $C_{hold}$. We can adjust the gain from $V_{CS}$ to the voltage for the comparison, with resistors $R_{csin}$ and $R_{csat}$. By verifying the moment that the comparator output changes from high to low during the detection, we can detect the moment that $V_{CS}$ crosses zero, from positive to negative.

![Figure 9. The proposed valley detection circuit: (a) current sense voltage circuit; (b) divided drain voltage circuit.](image)

4.2. Proposed Valley Detect Method with Divided Drain Voltage

The other method is to divide $V_d$ using two capacitors, i.e., $C1$ and $C2$, as shown in Figure 10, and to sense the moment that the differentiation of the divided voltage $V_{VAL}$ changes from negative to positive. One of the two capacitors ($C2$) is often used in practical applications to reduce EMI noise, and only one low-voltage capacitor ($C1$) is necessary in this case. The value of the capacitors for the divided voltage should not exceed the input range of the circuit receiving it. Figure 9b shows a valley detection circuit with the divided voltage of $V_d$. Part of the circuit is the same as that shown in Figure 9a, and a differentiator is additionally included. Owing to the capacitor $C_{div}$ connected between the input and the node with near constant voltage maintained by the source-follower transistors, the current proportional to $dV_{VAL}/dt$ is generated, and converted to the voltage fed to the comparator. When valley detection is not required, the switches controlled by $DET_b$ turn ON; the voltage corresponding to when the current proportional to $dV_{VAL}/dt$ is equal to zero is stored in capacitor $C_{hold}$. In detecting the valley, the switch controlled by $DET$ turns ON, and the current–voltage proportional to $dV_{VAL}/dt$ is compared with the voltage stored in $C_{hold}$. By verifying the moment when the comparator output changes from
low to high during the detection, we can detect the moment when the differentiation of VAL changes from negative to positive.

![Figure 10. PFC Converter with valley detection capacitors.](image1)

### 5. Simulation and Experimental Results

#### 5.1. Simulation Results

The two valley detection methods described in Sections 3 and 4 were verified by computer simulations with the circuit shown in Figure 11. Moreover, the parameters used in the simulations are detailed in the schematic. Acquiring accurate data is very important for accurate valley detection and ON-time calculation [26]. Therefore, properly designed low-pass filters were used in the sensing stage, such as ‘Vcs’ and ‘VVAL’.

![Figure 11. Simulation circuit.](image2)

Figures 12 and 13 show the operating waveforms in different $V_{in}$ conditions, i.e., 300 and 100 V, in a light-load condition. To verify the effect of delay for the current detection, the low-pass filters for $V_{cs}$ is changed in the ranges of 50 $\Omega$—47 pF and 39 $\Omega$—5 nF. The simulation results in Figures 12 and 13 correspond to the valley detection circuits with $V_{cs}$ and $V_{VAL}$, respectively.

When the low-pass filter is 50 $\Omega$—47 pF, the delay caused by it is negligible, the peak value of $I_L$ is almost the same even if $V_{in}$ decreases from 300 V to 100 V, and only switching frequency decreases; from which we can confirm that the proposed control method in light-load conditions operates properly. Moreover, we can confirm that the switch always turns ON near the valley of $V_d$ in both valley detection circuits.

When the low-pass filter is 39 $\Omega$—5 nF, the dependency of the peak value of $I_L$ on $V_{in}$ increases, because slope of $I_L$ depends on $V_{in}$, and a larger slope results in a larger extension owing to the delay of the low-pass filter. When the peak value of $I_L$ increases, owing to delay of the low-pass filter, the switching frequency decreases to cancel its effect.
valley detection circuit with \( V \) Electronics  low-pass filter, when a valley detection circuit with \( V \) Electronics  \( = v \) voltage (LPF = \( v \) voltage (\( \text{LPF} = \text{voltage (} V \) LPF = \( \text{voltage (} V \) Val \)

The timing for when the switch turns ON deviates significantly from the valley of \( V_{\text{ds}} \), when a valley detection circuit with \( V_{\text{cs}} \) is employed; however, it does not change, owing to the delay of the low-pass filter, when a valley detection circuit with \( V_{\text{VAL}} \) is employed.

Figure 12. Simulation results of valley detection from current sense voltage (\( V_{\text{CS}} \)): (a) inductor current and drain–source voltage (\( \text{Vin} = 300 \text{ V}, \text{LPF} = 30 \Omega \times 5 \text{ nF} \)); (b) inductor current and drain–source voltage (\( \text{Vin} = 100 \text{ V}, \text{LPF} = 50 \Omega \times 47 \text{ pF} \)); (c) inductor current and drain–source voltage (\( \text{Vin} = 300 \text{ V}, \text{LPF} = 39 \Omega \times 5 \text{ nF} \)); (d) inductor current and drain–source voltage (\( \text{Vin} = 100 \text{ V}, \text{LPF} = 39 \Omega \times 5 \text{ nF} \)).

Figure 13. Simulation results of valley detection from divided drain voltage (\( V_{\text{VAL}} \)): (a) inductor current and drain–source voltage (\( \text{Vin} = 300 \text{ V}, \text{LPF} = 50 \Omega \times 47 \text{ pF} \)); (b) inductor current and drain–source voltage (\( \text{Vin} = 100 \text{ V}, \text{LPF} = 50 \Omega \times 47 \text{ pF} \)); (c) inductor current and drain–source voltage (\( \text{Vin} = 300 \text{ V}, \text{LPF} = 39 \Omega \times 5 \text{ nF} \)); (d) inductor current and drain–source voltage (\( \text{Vin} = 100 \text{ V}, \text{LPF} = 39 \Omega \times 5 \text{ nF} \)).
5.2. Experimental Results

Figure 14a shows an actual IC picture of the proposed valley detection circuit using the TowerJazz 0.18 µm 5 V/42 V CMOS process (TS035), and Figure 14b shows the experimental setup using the fabricated IC. This IC is designed as an output power in a full-load condition of approximately 240 W; however, the experimental results are focused on light-load conditions within a 40 W load, which is approximately 20% of the rated output power, to verify the improvement in power factor and efficiency under light-load conditions.

![Measurement setup](image)

Figure 14. Measurement setup: (a) realized valley detection CRM PFC IC; (b) test setup.

Figure 15 shows a key waveform under an input voltage of 220 V\(_{ac}\) and an output power of 40 W (400 V/0.1 A). Figure 15a shows the time-extended inductor current waveform shown in Figure 8, with the current sense voltage valley detection circuit shown in Figure 9a. As shown, the delay in switching ON is calculated by calculating \(t_{sw}\), satisfying Equation (1). Figure 15b shows the inductor current of the existing CRM boost PFC. The switching frequency in the zero-crossing region at a 40 W load is 130 kHz and shows a typical CRM boost PFC inductor current waveform, similar to that shown in Figure 2. Figure 15c shows the inductor current when the proposed valley switching technique is applied. The switching frequency is reduced to 76 kHz through the new valley detector method and the ON-time is extended, as shown in Figures 6 and 8, even under the same load condition.

Figure 16a–c show the comparison results of the light-load efficiency and power factor, between the existing CRM boost PFC method and the new valley detection method. Two commercial ICs were selected as the comparison group, and their performance was compared with that of the proposed method, to confirm the superiority of the proposed method more accurately. For the first comparison group (conventional#1), the SPC7011F manufactured by Fuji, with a fixed ON-time, and SFL of 500 kHz was used [20]. The second comparison group (conventional#2) had an existing valley detection method that was limited to 150 kHz at light-loads, and the On Semi’s NPC1602 was used for this [21]. The comparison result between the proposed method and conventional#1 shows an efficiency difference of 2.1% in the 40 W load condition; moreover, it shows an efficiency difference of up to 13% in the 1 W condition. This is due to the switching loss, caused by the increase of switching frequency to 500 kHz in the light-load or low-input-voltage condition. Furthermore, the MOSFET is turned on at a high \(V_{ds}\) voltage while resonating, which may reduce the efficiency. In terms of power factor, due to its fast switching in light-load and low-input-voltage conditions, the conventional#1 method achieves a higher power factor than the conventional#2 method. As a result, the power factor of the conventional#1 method was measured at 0.85 and 0.93 at 5 W and 40 W, respectively, while that of the proposed method was 0.95 and 0.985 under the same conditions, respectively. All the test conditions were controlled identically, and the comparison experiment was conducted after changing only the conventional#1 method to conventional#2 method. The efficiency of the conventional#2 method was 97% at 40 W and 48% at 1 W, which was 0.7% and 4% lower than that of the proposed method, respectively. However, this indicates that the conventional#2 method is relatively better than the conventional#1 method, in terms of efficiency. This result is because of the reduction in switching losses due to the limited switching frequency of 150 kHz, especially in light-load and low-input-voltage conditions. Compared
with the proposed method, the efficiency drop in the conventional#2 method increases as the load decreases. The analysis indicates that the reason for this result is the switching ON time limit of the conventional#2 method at light-loads and low-input-voltages. Compared with the proposed method, the power factor of the conventional#2 method shows a significantly larger difference under an 80 W load; moreover, a power factor difference of 0.581 is observed at 1 W. These results can be attributed to the large current distortion caused by the switching limitation of the conventional#2 controller in light-load and low-input-voltage conditions.

Figure 15. Key experimental waveform: (a) ON-time extended inductor current with new valley detection from current sense voltage ($V_{CS}$); (b) inductor current and drain–source voltage with conventional method; (c) inductor current and drain–source voltage with proposed valley detection method.

Figure 16. Cont.
which turned the switch ON at that moment, was included. Experimental results demonstrated that
were presented and explained in detail. A circuit for achieving the control method was designed in a

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Abbreviations

| Abbreviation | Description                                      |
|--------------|--------------------------------------------------|
| $C_{oss}$    | Drain–source parasitic capacitance of the switch |
| CRM          | Critical mode                                    |
| $I_L$        | Inductor current                                 |
| $I_{int}$    | Signal generator generates an output current     |
| $K$          | Constant value                                   |
| LC           | Inductance and capacitance                       |
| MOSFET       | Metal oxide semiconductor field effect transistor|
| PFC          | Power factor correction                          |
| SMPS         | Switch mode power supply                         |
\( T_{on} \)  
\( T_{ono} \)  
\( T_{sw} \)  
\( T_{zcd} \)  
\( V_{cs} \)  
\( V_{cmin} \)  
\( V_{ds} \)  
\( V_{FB} \)  
\( V_{in} \)  
\( V_{out} \)  
\( V_{ramp} \)  
\( V_{ref} \)  
\( V_{VAL} \)

Switch ON-time
ON-time before it is extended
Switching period
Inductor current returns to zero
Current sense voltage
Minimum level of the inductor current
Drain–source voltage of the switch
Generates an output voltage
Voltage feedback signal
Input voltage
Output voltage
Ramp signal voltage
Reference voltage
Differentiation of the divided voltage

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