A channel multiplexing digital calibration technique for timing mismatch of time-interleaved ADCs

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Abstract This paper presents an all-digital calibration technique for time-interleaved ADC (TIADC) timing mismatch. The calibration architecture is based on a channel multiplexing architecture. For a M-channel TIADC, only one centralized calibration module is needed. Timing mismatches between channels are estimated by correlating the adjacent channel’s outputs and a compensation algorithm based on the one-order five-point differentiator is employed to suppress the mismatches. Compared with conventional parallel calibration architecture, the proposed calibration architecture works well in higher Nyquist bands (NB) with high-scalability. The hardware consumption does not increase linearly with the number of sub-ADCs.

key words: time-interleaved ADC, timing mismatch, channel multiplexing, wide bandwidth
Classification: Integrated circuits

1. Introduction

The rapid growth in some areas, such as radar, communication and medical equipment, places a hard burden on the analog-to-digital converters (ADCs), and lead to an urgent need for energy-efficient ADCs in the GHz sampling frequency with moderate effective resolution. The time interleaved architecture of ADC that parallels several accurate sub-ADCs is an efficient solution [1]. However, the mismatch between channels will degrade the resolution of TIADC system seriously [2]. Particularly, the timing mismatch, which is nonlinear and sensitive to input signal, is challenging to estimate and compensate. In comparison, the offset and gain mismatch are much easier to handle [3]-[4].

Timing mismatch in TIADC can be calibrated through analog or mixed-signal techniques [5]-[9], but the calibration precision in analog domain is limited by the process. All-digital calibration technique, by contrast, seems to be a more promising and robust solution under various processes [10]. Some technologies have been developed in digital domain for timing mismatch calibration. However, most of these techniques [11]-[16] are derived assuming that the input signal is limited to the first Nyquist band (NB), and cannot be directly employed in the under-sampling TIADCs that are capable of sampling input signal located in the higher NB. Although some technologies can work for higher NB input, various problems still exist. The polyphase filters with under-sampling technique have been proposed in [17], but the lookup table for polyphase filters requires large hardware resources. Ref. [18] utilizes zero-crossing in the compensated signal and image signal, which is heavily dependent on statistics input. Ref. [19] needed an additional reference ADC and ref. [20] had to generate a pilot input signal, which also increases hardware consumption. In addition, ref. [21] employed Mitchell’s logarithmic multiplier with hardware reusing mechanism to reduce the complexity; however, the output suffered the inaccuracy effects that introduced by the logarithmic multiplier. Ref. [22] utilized Hilbert filter, but it was only suited to 2 channel or 4 channels systems.

In this work, an all-digital calibration architecture based on channel multiplexing technique for timing mismatch is presented. The timing mismatch is estimated by means of the correlation of adjacent channels’ outputs and a five-point derivative-based filter is employed to suppress the mismatch. Some improvements to the LMS and the Average modules are made to solve the problem of timing confusion existing in the serial architecture. The proposed multiplexing technique makes it possible for the calibration to be adapted to higher NB signal.
2. Channel Multiplexing Architecture

Most of the timing mismatch calibration techniques for TIADC [7], [12], [14], [16], [21], [22] using parallel timing mismatch calibration structure is shown in Fig. 1(a). A multi-phase clock synchronizes \( M \) \((M \geq 2)\) sub-ADCs with sampling rate \( f_{sam}=f_s/M \). Under the deployment of multiplexer, the TIADC system could achieve the overall sampling rate \( f_s \). \( y_{mn} \) denotes the \( n \)th sampling point of the \( m \)th channel and \( \tilde{y}_n \) denotes the \( n \)th calibrated output. The calibration timing diagram is shown in Fig. 1(b), where the hatched part indicates that the calibration module is in idle. In other words, assuming that the calibration can be accomplished in time, calibration modules are not fully utilized in a whole duty cycle. Besides, there are still two critical problems in the traditional calibration structure. Firstly, \( M \) calibration modules are needed for an \( M \)-channel TIADC, [7], [16], [22] or if the first channel is set as the reference ADC, at least \( M-1 \) channel is required [12], [14], [21], hence the hardware complexity increases with the number of sub-channels. More importantly, calibration based on this parallel architecture limits the input signal to the first Nyquist Band of sub-ADC.

In this work, a calibration architecture based on channel multiplexing is proposed as shown in Fig. 2(a) where only one centralized serial-calibration module is employed. The respective timing diagram is shown in Fig.2(b). Calibration is executed in a multiplexing mode.

One main advantage of the proposed architecture is that the calibration range is broadened in frequency domain. In conventional calibration architecture, the effective bandwidth is limited to Nyquist frequency of sub-ADCs. The calibration would be invalid when the input frequency is higher than this Nyquist frequency, because the aliasing will mislead the direction of estimation. Some techniques using serial architecture are proposed in ref. [23], [24], but the calibration range is also limited to first Nyquist frequency. In this work, the calibration is executed using the multiplexed data \( y_{mn} \). The estimation and compensation stages are executed in the same direction; hence the effective input frequency could be expanded far beyond the Nyquist frequency of entire TIADC system without extra hardware overhead.

Also, this multiplexing structure can solve the problem that hardware complexity will increase with the number of sub-channels. For a \( M \)-channel TIADC, only one module is used to calibrate the mismatches existing in all channels. In addition, centralized calibration module which works in higher frequency results in more power consumption. But we eliminate the power consumption generated from extra calibration modules compared with [7], [12], [14], [16], [21], [22], which is more suitable for advanced manufacture nodes.

3. Timing Mismatch Calibration

The calibration architecture based on channel multiplexing consists of two parts, which are depicted as estimation and compensation process. To analyze the timing mismatch calibration, the offset mismatch and gain mismatch, which could deal with common approaches are not considered here.

3.1 Timing mismatch estimation

The estimation method proposed here is based on cross-correlation for the merit of low complexity. The output of \( i \)th channel is given by [25]

\[
y_{i}[n] = \sin(w(nM + iT_s + \Delta t_i)) + \beta
\]  

(1)

Where \( w \) is the input angular frequency, \( \Delta t_i \) models the
timing mismatch, the \( \beta \) represents the aggregate noise.

For a small \( \Delta t \), the expectation of the first-order small quantity is related with the timing error [17], [23] which can be written as

\[
E[y[n] \times y'[n]] = \frac{1}{2} \left[ E[y[n] \times y_{i+1}[n]] - E[y[n] \times y_{i}[n]] \right] \\
= \frac{1}{2} \left[ \cos(w(1-\Delta t)) - \cos(w(1+\Delta t)) \right]
\]

(2)

Where \( y_{i}[n] \), \( y[n] \), \( y_{i+1}[n] \) are the digital outputs of adjacent channels. According to the formula (1), if there is no timing error \( \Delta t \), the expectation of the \( y[n] \times y'[n] \) will equal to zero; when timing error changes, the expectation value will change. Thus, we use the time correlation \( y_{i}[n] \times y'[n] \) as a related error in the LMS iterative algorithm to get the actual timing error as follows

\[
\Delta t(n+1) = \Delta t(n) + E[y[n] \times y'[n]] \times \eta_i
\]

(3)

where \( \eta_i \) is the iteration step, and the specific estimation scheme is shown in Fig. 3.

3.2 Timing mismatch compensation

The compensation techniques for timing mismatch usually include variable delay line [7], [8], [12], Farrow structure filter [26], [27], Taylor series expansion compensation [28], and adaptive calibration algorithm [29], [30]. In this work, a compensation algorithm based on five-point differentiator is proposed here. The signal output is the sum of the ideal signal and the signal derivative and the error term, which is proportional to its derivative [14], [23]. Thus, subtracting the product of error term and signal derivative can get the corrected output. The compensation principle is shown in Fig. 4. The corrected output is

\[
\hat{y} \approx y - \Delta t \times \frac{dy}{dt}
\]

(4)

where \( dy/dt \) can be implemented by a five-point derivative based on Lagrange interpolation, which can be written as

\[
f(x) = \sum_{k=-n}^{n} f(x_k) L_{N,k}(x) + \frac{(x-x_0) \cdots (x-x_n)}{(N+1)!} f^{(N+1)}(\xi(x))
\]

(5)

The sampling nodes are given as \( (x_0, f(x_0)), (x_1, f(x_1)), \ldots, (x_N, f(x_N)) \) and the discrete waveform with derivative shown in Fig. 4 (a). Plus, a tradeoff is considered here to choose the appropriate derivative order and number of sampling points. In general, using high order derivative method could achieve higher precision than first order derivative, but the hardware complexity will increase greatly, and the compensation bandwidth will be limited. However, using first order derivative with only two or three sampling points will degrade the accuracy of derivative. Thus, a one-order five-point midpoint derivative is employed. Taking the \( N=5 \) into formula (5), the corresponding midpoint formula coefficients are given by

\[
\frac{dy}{dt} \approx \frac{1}{12T_s} \times (y_{i-2} - 8y_{i-1} + 8y_{i+1} - y_{i+2})
\]

(6)

where \( y_{i-2}, y_{i-1}, y_i, y_{i+1} \) and \( y_{i+2} \) are five adjacent samples that outputted from the adjacent sub-ADCs. If the compensation aims to specific frequency application, the propriate coefficients of the differentiator could be further calculated [31], [24].

3.3 Customized LMS and Average

In the proposed serial calibration architecture, not all of the modules can indiscriminately process the assembled serial data stream. Some modules, such as LMS and Average need to process not only the current data but also the feedback historical data. Therefore, traditional LMS and Average that get feedback cycle by cycle will destroy the normal timing sequence required to convergence. To avoid timing disorder, some delay units are added to return the feedback data right to its own sub-channel. For a \( M \)-channel TIADC system, \( (M-1)T_s \) delay is added to both LMS and Average modules presented in Fig. 5(b), named serial-LMS and serial-Average.
The data stream comparison between conventional LMS and the serial-LMS in a 4-channel TIADC is illustrated in Fig. 6. To analyze the timing order briefly, the magnified factor is not considered here. For the conventional LMS unit, the data from previous cycle is directly fed back to the current input. In the end of first 4-cycle calibration shown in Fig. 6(a), the output includes $y_{11}$, $y_{12}$, $y_{13}$, $y_{14}$ from all 4 channels. We could not extract the useful information for single channel. Consequently, the data corruption lead to invalid calibration.

Therefore, some delay units are added to the serial-LMS to change the timing order shown in Fig. 6(b). In the first three cycle, the output remains 0; in the 4th cycle, the output is $y_{11}$ and the input is $y_{21}$, which both from the first channel; Then, $y_{12}$, $y_{13}$, $y_{14}$ also add to $y_{22}$, $y_{23}$, $y_{24}$, respectively. In the 12th cycle, when the data accumulate, the output $y_{11}$, $y_{21}$, $y_{31}$ could still fed back to $y_{41}$, which are all the sampling information from the first channel. During this iteration process, we rearrange the corresponding order of input and feedback output to reach the goal that feedback data comes from the same channel with current input.

Based on above analysis, the complete block diagram for the channel multiplexing calibration structure is proposed in Fig. 7.

### 4. Simulation Results

The proposed calibration architecture was modeled and verified at behavioral level based on MATLAB. A 4-channel 8-bit TIADC is employed here, with 1 GS/s system frequency. The iterative step $\mu$ both in serial-Average and serial-LMS module are set to $2^{-10}$.

The output spectrum of the 4-channel TIADC with signal frequency normalized at 0.15$\text{f}_s$ is shown in Fig. 8. After calibration, the spurs due to the timing mismatch has been greatly minimized and the SNDR rises from 32.9 dB to 48.4 dB. The spectrum with normalized frequency 0.45$\text{f}_s$ is shown in Fig. 9, and the SNDR rises to 48.2 dB.

The simulation results above show that the proposed calibration technique is effective throughout the entire Nyquist band of the TIADC.
Fig. 11 shows the output spectrum of 4-channel TIADC with 45-tone input signal that located in the second NB of TIADC, from \( y_l=0.5f_s + 0.135f_s \) to \( y_H=0.5f_s + 0.355f_s \). It can be observed that spurs due to timing mismatch are suppressed significantly by the proposed calibration technique, and the SNDR improvement approximately reach 14 dB.

Table 1 compares the main features of calibration techniques proposed in previous reported work. It can be shown that this work has advantages in the calibration bandwidth, hardware complexity and scalability.

### Table 1 Comparison with the state-of-art techniques.

| Reference | [14] | [22] | [12] | [24] | This work |
|-----------|------|------|------|------|-----------|
| Fully Digital | Yes | Yes | No | No | Yes |
| Serial Calibration Architecture | No | No | No | Yes | Yes |
| Input in higher NBs | No | Yes | No | No | Yes |
| Ref. channel | Yes | No | Yes | Yes | No |
| M (# of channels) | 12 | 4 | 4 | 4 | Arbitrary |
| Hardware consumption (channels) | Yes | Yes | Yes | Yes | No |
| Resolution | 9 Bit | 11 Bit | 8 Bit | 10 Bit | 8 Bit |

5. Conclusion

In this paper, a timing mismatch calibration technique based on the “serialization through multiplexing” is presented for TIADC. This technique takes effect in high input frequency range over Nyquist band, and consumes less hardware resources by means of high-scalability. The 4-channel and 8-channel TIADCs with 8-bit resolution are modeled and simulated. The simulation result shows that the proposed technique is effective to reduce the distortion caused by timing mismatch and can improve the SNDR and SFDR significantly.
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