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Design and performance of the TIGER front-end ASIC for the BESIII Cylindrical Gas Electron Multiplier detector

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Abstract—We present the design and characterization of TIGER (Turin Integrated Gem Electronics for Readout), a 64-channel ASIC developed for the readout of the CGEM (Cylindrical Gas Electron Multiplier) detector, the proposed inner tracker for the 2018 upgrade of the BESIII experiment, carried out at BEPCII in Beijing.

Each ASIC channel features a charge sensitive amplifier coupled to a dual-branch shaper stage, optimized for timing and charge measurement, followed by a mixed-mode back-end that extracts and digitizes the timestamp and charge of the input signals. The time-of-arrival is provided by a set of low-power TDCs, based on analogue interpolation techniques, while the charge measurement is obtained either from the Time-over-Threshold information or with a sample-and-hold circuit.

The ASIC has been fabricated in a 110 nm CMOS technology and designed to operate with a 1.2 V power supply, an input capacitance of about 100 pF, an input dynamic range between 3 and 50 fC, a power consumption of about 12 mW/channel and a sustained event rate of 60 kHz/channel. The design and test results of TIGER first prototype are presented showing its full functionality.

Index Terms—front-end ASIC, mixed-signal design, ASIC characterization, BESIII, GEM

I. INTRODUCTION

BESIII (BEijing Spectrometer III) is a multipurpose detector to study the collisions provided by the Beijing Electron-Positron Collider II (BEPCII), hosted at the IHEP (Institute of High Energy Physics) laboratory [1]. The Inner Tracker is showing aging effects due to the high radiation absorbed and since BESIII will run at least until 2022, it is foreseen to upgrade the Inner Tracker with a new detector. The proposed new inner tracker comprises three layers of Cylindrical Gas Electron Multiplier (CGEM) detector [2], [3]. Each layer consists of a cathode, three GEMs foils and the readout anode, which is segmented with 650 µm pitch XV-patterned strips. In order to achieve the required spacial resolution (130 µm), an analogue readout has been chosen since it allows to employ charge centroid and micro-TPC (Time Projection Chamber) algorithms to reduce the total number of channels to about 10,000 [4].

In this context, a dedicated front-end readout ASIC delivering the time and charge information for each fired strip has been developed.

II. ASIC ARCHITECTURE

TIGER (Turin Integrated Gem Electronics for Readout) is a mixed-signal ASIC for the readout of the CGEM detector. The ASIC architecture is shown in Fig. 2 and consists of 64 channels, references and bias generators, an internal test pulse calibration circuitry and a digital global controller. It has been designed in a 110 nm CMOS technology with a die area of 5x5 mm² and a low voltage operation of 1.2 V. The digital back-end is an SEU-upgraded version, i.e. protected against Single Event Upset using Hamming encoding and Triple Modular Redundancy, of the TOFPET2 ASIC [5], [6].

The architecture and parameters of the ASIC have been driven by the requirements of the CGEM detector, i.e. 100...
Entries 64
Mean 30.73
RMS 0.5828
time resolution [ps]
29 30 31 32 33
N
0
2
4
6
8
10
12
14

Fig. 2. TIGER ASIC.

The channel controller, a digital logic block working at 160 MHz clock frequency, generates the trigger signals for the channel operations. The time and charge information is provided by two low-power TDCs based on analogue interpolation and a sample-and-hold circuit (S/H). Each TDC is composed of a set of four time-to-analogue converters (TAC) and a Wilkinson ADC, and delivers a 50 ps time binning at 160 MHz clock frequency [7]. The S/H circuit samples the output signal of the E-branch shaper within a time window, generated by the digital logic and configurable by the user. The sampled signal is digitized with the same Wilkinson ADC used for the TDC operation, therefore both TAC and S/H circuits employ a quad-buffer scheme to de-randomize the input event rate and lessen the issue of the inherently high conversion time of this method. The flexibility of this multiple readout scheme allows to extract the charge measurement either from the Time-over-Threshold (ToT) or the S/H circuit digitized value.

The readout scheme features a trigger-less mode in which each input signal above the threshold is digitized and sent to the global controller which manages the data transmission to an FPGA board through 2 LVDS links, using 8B/10B encoding. The ASIC configuration is handled by the FPGA through a 10 MHz SPI like interface and allows to send a test pulse (TP) signal either to the front-end to test the whole readout chain or directly to the channel controller to calibrate the TDCs and assess the functionality of the digital logic of the chip. The analogue TP is generated by an internal calibration circuitry with a user-configurable amplitude, allowing to test the ASIC for the whole input dynamic range.

III. Test Results

The first prototype was produced in a Multi-Project Wafer (MPW) run and received in October 2016. The ASIC electrical characterization started in November 2016. As a first step, the back-end electronics was tested and found fully functional: Read/Write operations of channel/global configuration registers, data transmission and decoding, TDC operation and fine calibration are working properly. The TDCs performance have been evaluated by sending a digital test pulse at their inputs and sweeping the TP phase along one clock cycle. A look-up-table (LUT) is generated to store the gain and offset correction for all the channels. After the calibration, the TDC quantization error, shown in Fig. 4, is lower than 50 ps r.m.s for both branches and for all the channels.
This implies that the system time resolution is affected only by the sensor and the analogue front-end response. The jitter of the T-branch has been evaluated using the internal calibration circuitry to generate signals of fixed charge (3 fC) which are fed at the preamplifier input. The measured time jitter is below 5 ns r.m.s., allowing for efficient time-tag.

Threshold scans have been performed for thresholds equalization and noise measurement. In this method, the s-curve produced by the threshold scan is fitted with a sigmoid function in which the 50% value corresponds to the baseline level and the sigma provides the noise. A look-up-table allows to correct the mismatches between the channels by adjusting their effective threshold. Fig. 5 shows the s-curves for the 64 channels before and after thresholds equalization.

The noise has been evaluated for different input capacitances and the results are displayed in Fig. 6. The equivalent noise charge (ENC) measured at the output of the E-branch shaper for a 100 pF input capacitance is about 2100 electrons, which is slightly higher than the value expected from simulations. Despite the fact that the measured performance are already adequate for our application, more dedicated tests are currently ongoing in order to reduce the noise.

IV. OUTLOOK AND CONCLUSIONS

A 64-channel ASIC, named TIGER, has been developed to readout the signals coming from the BESIII CGEM detector. The results from the first prototype electrical characterization are in good agreement with the expected values, except for the noise, and the performance meet the requirements set by the experiment. Tests with the detector are currently ongoing using cosmic rays and radioactive sources, in order to fully qualify the ASIC with the sensor. A new version has been submitted in August 2017, with minor design revisions, to fully equip the detector for the installation which is scheduled for Summer 2018.

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