Common-Mode Voltage Suppression Strategy Based on Fast MPC for a Five-Level Nested Neutral Point Piloted Converter

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ABSTRACT This paper, regarding a five-level nested neutral point piloted (NNPP) converter as the research object, analyzes the working mechanism of an NNPP five-level converter and determines the switching commutation circuit and switching principles. To solve the problem of common-mode voltage (CMV) in NNPP five-level converters, a control strategy based on fast model predictive control (MPC) is proposed to effectively suppress common-mode voltage. The control method proposed in this paper is divided into two main parts. First, 19 zero common-mode voltage (ZCMV) vectors are selected from 125 voltage vectors, and 19 ZCMV vectors are optimized to select the best ZCMV vector. Next, according to the switching principles, the effective switching combinations are selected as the effective candidate control set, and proper switching combinations of the optimal ZCMV vector are determined. The effectiveness and validity of the proposed suppression strategy based on fast MPC in terms of the steady state and dynamic performance is confirmed by simulation and experimental results of the five-level NNPP converter.

INDEX TERMS Three-phase five-level converter, nested neutral point piloted, common-mode voltage suppression, model predictive control, switching principle.

I. INTRODUCTION Multilevel converters have been widely used in high-voltage high-power and alternating current speed control systems. However, limited by the withstand voltage level of power devices, three-level converters based on diode clamping will be limited in practical industrial applications. Therefore, higher-level converters are needed to improve the output voltage. Five-level converters have become a research hotspot in multilevel converters due to their advantages of multiple topologies, fewer components and higher cost performance. The traditional five-level topologies include neutral-point clamped five-level (NPC-5L) converters [1], flying-capacitor five-level (FC-5L) converters [2], [3] and cascaded H-bridge five-level (CHB-5L) converters [4].

The existence of common-mode voltage (CMV) in the multilevel converters will produce high amplitude shaft voltages and bearing currents, which will shorten the service life of the motor. In addition, the CMV can also produce high-order harmonics, increase the active and reactive power losses, and affect the power quality [5]. In the literature, various filters for eliminating the CMV of the inverter have been reported, which can produce a CMV with the same amplitude and opposite phase as the output voltage to suppress the CMV [6], [7]. For the CMV of multilevel inverters, various methods of using multiple space vector pulse width modulation to reduce the CMV can be found in many references [8]–[15]. In [8], a near-state pulse width modulation method was proposed to reduce the CMV of a three-phase pulse width modulation (PWM) inverter. Compared with traditional PWM modulation, the proposed the large vectors, medium vectors, and zero large vectors technology through large, medium and zero vectors can reduce the CMV that causes leakage current [9]. The modulation method of eliminating CMV for multilevel inverters is generally based on the principle of three-zero CMV. Compared with the existing PWM, a method based on carrier pulse width modulation for optimal output current ripple can effectively reduce the current ripple.
Phase-shifted sinusoidal pulse width modulation can significantly reduce CMV compared with traditional SPWM [11]. Aiming at the problem of common-mode spikes in CMV reduction PWM, a method of the injected zero-sequence voltage is proposed to eliminate CMV spikes [12]. A CMV reduction PWM, which can limit the CMV of the three-level neutral point clamped to less than one-sixth of the dc-link voltage, is researched in reference [13]. For the CMV of three-level converters, a double modulation wave carrier-based PWM strategy is proposed in [14]. The work reports a modified T-structured three-level inverter that can eliminate CMV, which is considered in [15]. In reference [16], the PWM scheme is adopted to eliminate the CMV of the five-level inverter, and the method has been improved in [17]. In reference [18], a novel SVPWM algorithm based on line voltage coordinates are proposed to address the shortcomings of the traditional algorithm, and the CMV of the five-level active neutral-point-clamped inverter is suppressed by selecting the appropriate switching state. Furthermore, ZCMV vectors can be used to eliminate CMV, presenting a space vector pulse width modulation (SVPWM) technique, which eliminates the CMV of a five-level active neutral-point clamped inverter by using the ZCMV vectors in [19]. However, considering that the above PWM methods are applied to multilevel inverters above three levels, the complexity and computational amount are increased due to the sharp increase in the number of space voltage vectors.

In recent years, the model predictive control (MPC) [20], [21] provides a new solution to the CMV problem due to its advantages such as simple structure, flexible control and multi-objective control. At present, MPC has been used to suppress CMV in some references [22]–[26]. References [22] and [23] propose an improved MPC strategy that can significantly reduce the CMV for voltage-source converters but increase the THD of the switching loss and current waveform. In the MPC strategy proposed in [24], four nonzero vectors are used for optimization in each cycle to suppress the CMV and reduce the switching frequency and calculation amount. Reference [25] proposes a double-vector MPC strategy to reduce CMV and current ripples for a three-level T-type converter. Reference [26] uses a model predictive control method combined with ZCMV vectors to eliminate the CMV of a five-level active neutral-point clamped inverter. When the output level of the inverter increases, the amount of calculation increases, which increases the operating burden of the MPC method. Therefore, it is necessary to reduce the candidate control set of MPC and reduce the amount of system calculation.

Recently, a nested neutral point piloted five-level (NNPP-5L) converter is derived from the three-level neutral-point piloted (NPP) topology. The NPP converter does not need extensive clamping devices, and the power switching voltage stress is equal and has the characteristics of high-power density and high efficiency [27]. There is no MPC research on CMV suppression in five-level NNPP converters at present. This paper proposes a fast MPC control algorithm based on the switching principles. The contributions of this paper are as follows:

1) In order to reduce the CMV, 19 space voltage vectors are selected from 125 space voltage vectors, and all switch combinations corresponding to the 19 voltage vectors are the candidate control set.
2) In order to further reduce the candidate control set of the switch combinations, a two-step prediction is adopted for the fast MPC control strategy based on the switching principles.
3) According to the control strategy, the cost function is designed in two steps, which reduces the number of weighting factors to a certain extent.

This paper is organized as follows. Section II presents the operating principle and switching combination principles of the five-level converter. The conclusion that switching principle at different time is obtained. In Section III, the selection of zero CMV and determination of the control set are obtained. Section IV proposes a fast MPC algorithm based on the switching principles to reduce the common-mode voltage. In Section V, the simulation and experimental results are presented. Finally, Section VI concludes this paper.

**II. OPERATING PRINCIPLE AND SWITCHING PRINCIPLE OF THE FIVE-LEVEL NNPP CONVERTER**

**A. ANALYSIS OF OPERATING PRINCIPLE**

The main circuit topology of the three-phase five-level NNPP converter is shown in Fig. 1.

Taking the single-phase topology as an example, $i_{s0}$, $i_{sf1}$, $i_{sf2}$ and $i_s$ are the neutral point currents on the dc-link, two flying capacitor currents and the output phase current. If the total voltage on the dc-link bus is $4E$, the voltages of dc-link capacitors $C_1$ and $C_2$ are $2E$, and the voltages of flying capacitors $C_{f1}$ and $C_{f2}$ are both $E$. Taking the neutral point of the dc-link as a reference, the five levels are -2E, -E, 0, E, 2E, which are represented by numbers 0, 1, 2, 3 and 4. There are nine different switch combinations for the five levels, which can be expressed as $(S_{11} S_{21} S_{13} S_{14} S_{23} S_{24} S_{15} S_{25})$, where $x$ represents different phases ($x = a, b, c$). The switches $S_{11}$, $S_{12}$, $S_{15}$ and $S_{16}$, $S_{21}$, $S_{22}$, $S_{25}$ and $S_{26}$ cannot be turned on at the same time, and the switches $S_{11}$ ($S_{12}$) and $S_{14}$, $S_{15}$ ($S_{16}$) and $S_{13}$, $S_{21}$($S_{22}$) and $S_{24}$, $S_{25}$

**FIGURE 1.** The main circuit topology of the three-phase five-level NNPP converter.
(S_{26}) and S_{23} are complementary, respectively. The specific switch combinations are shown in Table 1 [28], [29], where 1 and 0 indicate the turn-on and off states, respectively.

As Table 1 shows, when the output level is E, there are two switch combinations A2 and A3, which have the opposite effects on the higher flying capacitor voltage. Among these combinations, the effect of switch combination A3 on the higher flying capacitor voltage and the neutral point voltage of the dc-link is the same. When the output level is 0, there are three switch combinations A4, A5 and A6, among which switch combinations A4 and A6 have opposite influences on the upper and lower flying capacitor voltages, while switch combination A5 only works on the neutral point voltage of the dc-link.

When the output level is -E, corresponding to switch combinations A2 and A8, the effect of switch combinations A7 and A8 on the lower flying capacitor voltage is opposite, and the function of A8 on lower flying capacitor voltage and the neutral point voltage of the dc-link is different. Therefore, even if the output level is the same, the charging and discharging characteristics of the switch device are different when different switch combinations are selected.

Assuming that the output current i_x is positive, when the output level is -E, switch combination A7 discharges the lower flying capacitor voltage, while A8 charges the lower flying capacitor voltage and discharges the neutral point voltage of the dc-link. Similarly, when the output level is 0, switch combination A4 charges the upper and lower flying capacitor voltages, switch A6 discharges the voltage of the upper and lower flying capacitors, and A5 discharges only the neutral point voltage of the dc-link. Therefore, considering that there are many switching states in the five-level converter, a switch combination may affect both the voltage of the flying capacitor and the neutral point voltage of the dc-link, so there is coupling between the voltage of the flying capacitor and the neutral point voltage of the dc-link, which makes the balance of the capacitor voltage more difficult to control.

In addition, the switching between different switch combinations will produce different levels. To avoid unreasonable level jumps, it is necessary to select the switch between adjacent levels corresponding to the switching principle. Taking the switching between the 0 and -E levels as an example, there are three redundant switch combinations in the 0 level and two redundant switch combinations in the -E level, so there are six switching modes between 0 and -E. If switch combinations A4 and A8 are selected as circuit mappings for the 0 level and -E level, respectively, switch combinations A4 and A8 are selected, and a certain dead zone is added. When i_x >0, the mapping circuit is 10100101(0) switched to 00110101(-E) through 00100101(-E), as shown in loop F1, switch S_{13} is normally on, and switches S_{14} and S_{25}(S_{26}) flow through the antiparallel diode. When i_x <0, the mapping circuit is 10100101(0) switched to 00110101(-E) through 00100101(0), as shown in loop F2, switches S_{25}(S_{26}) are normally on, and switches S_{11}(S_{12}) flow through the antiparallel diode. According to the above analysis, when combinations A4 and A8 are switched, there is no level jump, and the level is limited between 0 and -E. However, if the 0 level and -E level, respectively, select combinations A6 and A8 as circuit mapping, that is, switch between combinations A6 and A8, and add a certain dead zone. When i_x >0, the mapping circuit is 01011010(0) switched to 00110101(-E) through 00010000(-2E), as shown in loop F3, and switches S_{15}(S_{16}) and S_{25}(S_{26}) both flow through the antiparallel diode. When i_x <0, the mapping circuit is 01011010(0) switched to 00110101(-E) through 00010000(2E), as shown in loop F4, switch S_{14} normally conducts, and switches S_{11} and S_{21}(S_{22}) flow through the antiparallel diode. When switching between combinations A6 and A8, there is a jump between level 0 and -2E or E to -E. The specific switching loop is represented in Fig. 2.

### B. PRINCIPLES OF SWITCHING COMBINATION

The analysis method of Fig. 2 is used to analyze the remaining switching circuits. For example, when switching between

| Level | S_{11} | S_{21} | S_{13} | S_{14} | S_{23} | S_{24} | S_{15} | S_{25} | A_4 | A_5 | A_6 | V_{sw} | i_p | i_q | i_r | i_s |
|-------|--------|--------|--------|--------|--------|--------|--------|--------|-----|-----|-----|--------|----|----|----|----|
| 4     | 1      | 1      | 0      | 1      | 0      | 1      | 0      | 0      | A_2 | -E  |    |        |    |    |    |    |
| 3     | 0      | 1      | 1      | 1      | 0      | 0      | A_3    | i_x   |    | i_x |    |        | i_x|    |    |    |
| 2     | 0      | 0      | 1      | 1      | 1      | 0      | A_4    | i_x   |    | i_x |    |        |    | 0  |    |    |
| 1     | 0      | 0      | 0      | 1      | 1      | 1      | A_5    | i_x   |    | i_x |    |        |    | 0  |    |    |
| 0     | 0      | 0      | 0      | 0      | 0      | 0      | A_6    | i_x   |    | i_x |    |        |    | 0  |    |    |
TABLE 2. Switching principle at different time.

| k       | k+1         |
|---------|-------------|
| A_1     | A_1 A_2 A_3 |
| A_2     | A_1 A_2 A_4 |
| A_3     | A_1 A_3 A_6 |
| A_4     | A_2 A_3 A_5 |
| A_5     | A_2 A_4 A_7 |
| A_6     | A_3 A_5 A_7 |
| A_7     | A_3 A_6 A_9 |
| A_8     | A_4 A_5 A_9 |
| A_9     | A_5 A_6 A_8 |

level E and level 0, there are six switching modes. When the switch combination is A_2 and A_4, A_2 and A_5, A_3 and A_5, A_3 and A_6, a total of four kinds of switching modes, at this time, there is no level jump between level E and level 0. However, when switching between A_2 and A_6 or between A_3 and A_4, there is a -E or 2E level jump between the two modes. The voltage stress of the switching device will be increased if the switching levels jump. To avoid the level jump and reduce the loss of switching devices, in the case of meeting the switching principle, that is, in the process of switching, the switch is on and off only once.

The switching mode between adjacent levels in the switch combination can be analyzed, and the switching principles of the switch combinations for a single-phase five-level NNPP converter can be derived, as shown in Table 2. Here, the effective switch combinations corresponding to switch combination A_5 are defined as A_2 A_4 A_5 A_7, so the maximum number of effective switch combinations for each phase is not more than 4 and the maximum number of three-phase effective switch combinations does not exceed 64.

III. SELECTION OF ZCMV AND DETERMINATION OF THE CONTROL SET
The five-level NNPP converter has five level states for each phase, which are represented by 0, 1, 2, 3, and 4, so there are 125 level states in the three phases. The spatial voltage vector distribution composed of 125 level states is shown in Fig. 3. Meanwhile, since the five level states of each phase correspond to nine switch combinations and a total of 729 switch combinations for three phases, there are 729 different mapping types when the switch states are mapped to the hardware circuit. If the traditional MPC is used, the difficulty of selecting the switch state and switch combination is greatly increased.

A. SELECTION OF ZERO COMMON MODE VOLTAGE VECTOR
To solve the problem of common mode voltage in a five-level NNPP inverter, the optimal ZCMV vectors are selected based on the traditional space voltage vectors. According to the fast MPC control strategy proposed in this paper, namely, according to the switching principle, all possible switch combinations corresponding to the optimal ZCMV vector are taken as the control set and output the optimal switch combination according to the cost function. This method can realize the balance of dc-link capacitance and flying capacitor voltage and curb the common mode voltage. The method does not need extensive function calculations, which reduces the number of iterations and is easy to implement flexibly.

From the NNPP main circuit topology in Fig. 1, the three-phase five-level output voltage can be expressed as:

\[
\begin{align*}
V_{an} &= V_{ao} - V_{no} = Ld_{ia}/dt + R_{ia} \\
V_{bn} &= V_{bo} - V_{no} = Ld_{ib}/dt + R_{ib} \\
V_{cn} &= V_{co} - V_{no} = Ld_{ic}/dt + R_{ic}
\end{align*}
\]

where the common-mode voltage \(V_{no}\) is the voltage between the load neutral point and reference point potential, can be described as:

\[
V_{no} = (V_{ao} + V_{bo} + V_{co})/3
\]

where \(V_{ao}, V_{bo}\) and \(V_{co}\) are the three-phase output voltages of the inverter.

Assuming that the dc-link voltage is \(V_{dc}\), the switch state is marked as \(S_x(x = a, b, c)\). The five level states of the three-phase output can be expressed as follows:

\[
\begin{align*}
V_{ao} &= -V_{dc}/2 & \text{if } S_x &= 0 \\
V_{xo} &= -V_{dc}/4 & \text{if } S_x &= 1 \\
V_{so} &= 0 & \text{if } S_x &= 2 \\
V_{vo} &= V_{dc}/4 & \text{if } S_x &= 3 \\
V_{vo} &= V_{dc}/2 & \text{if } S_x &= 4
\end{align*}
\]

According to (3), the relationship between the three-phase output voltage and the switching state can be deduced as:

\[
V_{xo} = V_{dc}(S_x - 2)/4
\]

Therefore, combining (2) and (4) can obtain the relationship between the common mode voltage and switching states:

\[
V_{no} = V_{dc}(S_a + S_b + S_c - 6)/12
\]
The five-level NNPP inverter output voltage is expressed by the DC-link voltage, which can output five levels: $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$, and $V_{dc}/2$. To suppress the common-mode voltage, space voltage vectors with ZCMV can be applied in the control. By substituting all possible switching states of the three phases into formula (5), 19 ZCMV vectors can be obtained. As shown in Fig. 4, 19 ZCMV vectors are selected from 125 space voltage vectors to suppress common-mode voltage, greatly reducing the number of control vectors.

**B. CONTROL SET BASED ON SWITCHING PRINCIPLE**

The five-level NNPP inverter has many switching states. Because the five level states of the three-phase output correspond to 729 switch combinations, the traditional MPC will make the calculation more complicated. Based on the principle of switch combination, a fast MPC control strategy is proposed to reduce the computational burden and avoid unnecessary level jumps. As seen from Table 2, if the switch combination corresponding to the output level at $k$ is known, all possible switch combinations at $k + 1$ can be obtained. There are nine possible switch combinations at $k$, and the maximum number of switch combinations corresponding to each switch combination at $k + 1$ is not more than 4. To further reduce the number of switch combinations at $k + 1$, based on the switch combination corresponding to the known optimal ZCMV vector and combined with the principle of switching transitions, the number of switch combinations can be further reduced. Taking the ZCMV vector $V_5(123)$ as an example, the actual corresponding switch combinations are shown in Fig. 5.

If the switching principle is considered, as shown in Fig. 6, suppose at time $k$, the switch combinations of phase $a$ are $A_4$, those of phase $b$ are $A_2$, and those of phase $c$ are $A_8$. Table 2 shows that the switch combinations of phase $a$ should be $A_2$, $A_4$, $A_5$, and $A_8$ at time $k + 1$. Similarly, the switch combinations of phase $b$ should be $A_1$, $A_2$, $A_4$, and $A_5$ at time $k + 1$ and those of phase $c$ should be $A_4$, $A_5$, $A_8$, and $A_9$ at time $k + 1$. Fig. 5 shows that the actual switch combinations of phase $a$ for the ZCMV vector are $A_7$ and $A_8$, the actual switch combinations of phase $b$ are $A_4$, $A_5$ and $A_6$, and the actual switch combinations of phase $c$ are $A_2$ and $A_3$. According to the above analysis, switch combination $A_8$ not only satisfies the switching principle of phase $a$ but also satisfies the actual switch combination, so $A_8$ is regarded as the effective switch combination of phase $a$ at time $k + 1$. Similarly, $A_4$ and $A_5$ satisfy both the switching principle of phase $b$ and the actual switch combinations, so $A_4$ and $A_5$ are regarded as the effective switch combinations of phase $b$ at time $k + 1$. In particular, $A_2$ and $A_3$ do not satisfy the switching principle but are the actual switch combinations of ZCMV vector $V_5(123)$ in phase $c$. In this case, the actual switch combinations $A_2$ and $A_3$ are selected as the effective switch combinations of phase $c$ at time $k + 1$. According to the above derivation process, the effective switch combinations of the ZCMV vector $V_5(123)$ under all circumstances at time $k + 1$ can be obtained, as shown in Table 3. These effective switch combinations will be used as a candidate control set to participate in MPC control, and the optimal switch combination will be output. Table 3 shows that at time $k + 1$, phase $a$ has 1 or 2 switch combinations, phase $b$ has 2 or 3 switch combinations, and phase $c$ has 1 or 2 switch combinations. Therefore, there are at most 12 switch combinations and at least 2 switch combinations for three phases, compared with Table 2, which reduces the control set of MPC to a certain extent and reduces the amount of calculation.

**IV. FAST MPC BASED ON SWITCHING PRINCIPLE**

**A. MATHEMATICAL MODEL OF PREDICTIVE CONTROL**

Aiming at eliminating common-mode voltage, keeping capacitor voltage balance and reducing the calculation burden
of the five-level NNPP inverter, a fast MPC control strategy based on the switching principle is proposed, that is, according to the switching principles at \( k + 1 \), to select effective switch combinations of the ZCMV vector as the candidate control set and output the optimal switch combination that minimizes the cost function.

According to the topology of the five-level converter, the relationship between the phase voltage and the switching states is as follows:

\[
V_{\alpha} = (S_{21} - S_{11}) V_{cfx1} + (S_{23} - S_{13}) V_{cfx2} + S_{11} V_{c1} + (S_{13} - 1) V_{c2}
\]

(6)

From the balance mechanism of the flying capacitor and the dc-link capacitor voltage, substituting \( V_{c1} = 2E, V_{c2} = 2E, V_{cfx1} = E, \) and \( V_{cfx2} = E \) into (6), the following equation can be obtained:

\[
V_{\alpha} = (S_{11} + S_{21} + S_{13} + S_{23} - 2) E
\]

(7)

Under RL load, continuous-time model of load current is

\[
V_{in} (t) = V_{\alpha} (t) - V_{no} (t) = R i(t) + L \frac{d i(t)}{dt}
\]

(8)

Introduce the sampling period \( T_s \) into (8) and adopt the forward Euler approximation:

\[
d i(t) / dt = (i(k+1) - i(k))/T_s
\]

(9)

The discrete-time model of the output currents in the \( \alpha \beta \) coordinate system is

\[
\begin{align*}
i_{\alpha} (k+1) &= (T_s V_{in} (k) + (L - RT_s) i_{\alpha} (k))/L \\
i_{\beta} (k+1) &= (T_s V_{in} (k) + (L - RT_s) i_{\beta} (k))/L
\end{align*}
\]

(10)

Similarly, the continuous-time models of the flying capacitor voltage and the dc-link capacitor voltage are (11) and (12), respectively:

\[
\begin{align*}
i_{cfx1} (t) &= (S_{21} - S_{11}) i_{\alpha} (t) - C_{fx1} d V_{cfx1} (t)/dt \\
i_{cfx2} (t) &= (S_{23} - S_{13}) i_{\alpha} (t) - C_{fx2} d V_{cfx2} (t)/dt \\
i_o (t) &= \sum_{x=a,b,c} [(S_{13} - S_{11}) i_{x} (t)] = 2C_1 d V_{c1} (t)/dt
\end{align*}
\]

(11)

\[
\begin{align*}
i_o (t) &= \sum_{x=a,b,c} [(S_{13} - S_{11}) i_{x} (t)] = 2C_2 d V_{c2} (t)/dt
\end{align*}
\]

(12)

Using the forward Euler approximation for (11) and (12) and introducing the sampling time \( T_s \), the discrete-time models of the flying capacitor voltage and the dc-link capacitor voltage can be predicted as (13) and (14):

\[
\begin{align*}
V_{cfx1} (k+1) &= -T_s i_{cfx1} (k)/C_{fx1} + V_{cfx1} (k) \\
V_{cfx2} (k+1) &= -T_s i_{cfx2} (k)/C_{fx2} + V_{cfx2} (k) \\
V_{c1} (k+1) &= T_s i_o (k)/2C_1 + V_{c1} (k) \\
V_{c2} (k+1) &= -T_s i_o (k)/2C_2 + V_{c2} (k)
\end{align*}
\]

(13)

(14)

Particularly, there may be a one-beat delay in the predictive control when the algorithm is implemented. To solve this problem, two-step prediction can be adopted to compensate for which value of \( k+1 \) is taken as the feedback value of \( k+2 \), and the value of \( k+2 \) is substituted into the cost function to obtain the optimal switch combination.

The reference current \( i^*_{\alpha} \) at \( k + 2 \) can be estimated as

\[
i^*_{\alpha} (k + 2) = 6i^*_{\alpha} (k) - 8i^*_{\alpha} (k - 1) + 3i^*_{\alpha} (k - 2)
\]

(15)

where \( i^*_{\alpha}(k+2), i^*_{\alpha}(k), i^*_{\alpha}(k-1), \) and \( i^*_{\alpha}(k-2) \) are the current reference values at \( k + 2, k + 1, \) and \( k - 2, \) respectively. In the \( \alpha \beta \) coordinate system, the discrete-time model of the output current at instant \( k + 2 \) is as follows:

\[
\begin{align*}
i_{\alpha} (k+2) &= \frac{T_s}{L} V_{\alpha} (k+1) + \frac{L - RT_s}{L} i_{\alpha} (k+1) \\
i_{\beta} (k+2) &= \frac{T_s}{L} V_{\beta} (k+1) + \frac{L - RT_s}{L} i_{\beta} (k+1)
\end{align*}
\]

(16)

At instant \( k + 1 \), the current passing through the flying capacitors and the dc-link capacitors can be expressed as

\[
\begin{align*}
i_{cfx1} (k+1) &= (S_{21} (k+1) - S_{11} (k+1)) i_{\alpha} (k+1) \\
i_{cfx2} (k+1) &= (S_{23} (k+1) - S_{13} (k+1)) i_{\alpha} (k+1)
\end{align*}
\]

(17)

\[
i_o (k+1) = \sum_{x=a,b,c} [(S_{13} (k+1) - S_{11} (k+1))] i_{x} (k+1)
\]

(18)

The discrete-time models of the flying capacitor voltage and the dc-link capacitor voltage at instant \( k + 2 \) are expressed as

\[
\begin{align*}
V_{cfx1} (k+2) &= -\frac{T_s}{C_{fx1}} i_{cfx1} (k+1) + V_{cfx1} (k+1) \\
V_{cfx2} (k+2) &= -\frac{T_s}{C_{fx2}} i_{cfx2} (k+1) + V_{cfx2} (k+1) \\
V_{c1} (k+2) &= \frac{T_s}{2C_1} i_o (k+1) + V_{c1} (k+1) \\
V_{c2} (k+2) &= -\frac{T_s}{2C_2} i_o (k+1) + V_{c2} (k+1)
\end{align*}
\]

(19)

(20)

B. THE DESIGN OF THE COST FUNCTION

The weight coefficients in the cost function require repeated trial and error, which is relatively cumbersome. In traditional current prediction control, it is necessary to achieve current tracking and balance the dc-link capacitor voltage and flying
capacitor voltage at the same time. Therefore, the cost function is usually.

$$g = \left| i^*_\alpha (k+2) - i_\alpha (k+2) \right| + \left| i^*_\beta (k+2) - i_\beta (k+2) \right|$$

$$+ \lambda_1 \sum_{x=a,b,c} \sum_{i=1,2} \left| V_{cfxi} (k+2) - V_{cref} \right|$$

where $i^*_\alpha (k+2)$ and $i^*_\beta (k+2)$ are the values of the reference current located in the $\alpha\beta$ coordinate at moment $k+2$. $\lambda_1$ and $\lambda_2$ are the weight coefficients of the dc-link capacitor voltage and flying capacitor voltage in the cost function, respectively. The reference value $V_{cref}$ of the flying capacitor voltage for each phase is $V_{dc}/4$.

To reduce the number of weight coefficients in the cost function, the MPC control strategy based on the switching principle proposed in this paper can be divided into two stages. The first stage is in the current predictive control. Nineteen ZCMV vectors need to be substituted into the cost function $g_1$ for optimization in each sampling period, and the candidate voltage vector with the minimum value of the cost function $g_1$ is selected as the optimal voltage vector to realize fast current tracking. Therefore, the cost function $g_1$ can be designed as:

$$g_1 = \left| i^*_\alpha (k+2) - i_\alpha (k+2) \right| + \left| i^*_\beta (k+2) - i_\beta (k+2) \right|$$

To make the system have good dynamic and steady-state performance, while considering the balance of the flying capacitor voltage and the dc-link capacitor voltage, all the switch combinations of the optimal voltage vector are substituted into the cost function $g_2$ in the second stage, and the switch combination with the minimum cost function $g_2$ is output, reducing the number of weighting coefficients in the
cost function to a certain extent. The cost function $g_2$ can be designed as

$$g_2 = |V_{c1}(k+2) - V_{c2}(k+2)| + \lambda \sum_{x=a,b,c} \sum_{i=1,2} |V_{cfxi}(k+2) - V_{cref}|$$  \hspace{1cm} (23)

where the weight coefficient $\lambda$ is 0.5, and the reference value of the flying capacitor voltage for each phase is $V_{dc}/4$.

C. IMPLEMENTATION STEPS

The implementation process of the fast MPC strategy proposed in this paper to suppress common-mode voltage is divided into two main stages, as shown in Fig. 7.

In the first stage, the instant reference currents $i^*_\alpha(k+2)$ and $i^*_\beta(k+2)$ are predicted by using Lagrange extrapolation. Second, the load current and ZCMV vectors at $k+1$ are predicted, and load currents $i_\alpha(k+2)$ and $i_\beta(k+2)$ are predicted in two steps. Then, the optimal ZCMV vector can be obtained from the cost function $g_1$. In the second stage, the candidate control set of switch combinations is obtained by combining the optimal voltage vector with Tables 2 and 3, the predicted values at $k+2$ of the dc-link capacitor voltage and flying capacitor voltage are predicted in two steps, and the optimal output switch combinations are obtained by the cost function $g_2$. The flow chart of the control algorithm is shown in Fig. 8.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION PARAMETERS

To verify the feasibility of the theory and control strategy proposed above, the simulation of a five-level NNPP inverter was built according to the circuit structure in Fig. 1. The main parameters of the simulation are shown in Table 4.

B. STEADY-STATE ANALYSIS

Fig. 9 and Fig. 10 show the simulation results of the dc-link capacitor voltage, flying capacitor voltage and common-mode voltage when the load resistance is 10 $\Omega$. The traditional MPC control without reducing the common-mode voltage and the fast MPC control with common-mode voltage...
suppression proposed in this paper are compared in the steady state.

By comparing the line voltage and phase voltage of traditional MPC control strategy, the line voltage and phase voltage proposed in this paper have also been effectively improved. As shown in Fig. 10(a) and (b), the waveforms of the line voltage and phase voltage are smoother and higher in quality. Traditional MPC and the MPC strategy proposed in this paper stabilize the upper and lower capacitor voltage of the dc-link at approximately 260 V (\(V_{dc}/2\)), but the fluctuation range of the dc-link capacitor voltage in Fig. 10(d) is within 0.5 V. Compared with the fluctuation range of 2 V in Fig. 9(d), the proposed control strategy can better suppress the fluctuation of the bus capacitance voltage. Likewise, the three-phase five-level NNPP inverter has upper and lower flying capacitors, which can be charged and discharged frequently during the control period. As shown in Fig. 9(e) and Fig. 10(e), the voltage of the upper and lower flying capacitors is stable at approximately 130 V (\(V_{dc}/4\)).

In addition, by comparing the waveforms of the common-mode voltage in Fig. 9(f) and Fig. 10(f), Fig. 9(f) shows that when the traditional MPC is adopted, the system has a larger common-mode voltage, with a maximum amplitude of up to 173 V (\(V_{dc}/3\)). Fig. 10(f) shows that the fast MPC proposed in this paper can effectively suppress the common-mode voltage of the system, and the common-mode

FIGURE 10. Simulation waveforms of fast MPC under steady-state operation.

TABLE 4. Main parameters of five-level NNPP converter.

| Parameters          | Notation | Simulation |
|---------------------|----------|------------|
| dc-link voltage     | \(V_{dc}\) | 520 V      |
| dc-link capacitors  | \(C_1, C_2\) | 13500 μF  |
| Flying capacitors   | \(C_{e1}, C_{e2}\) | 6600 μF  |
| Fundamental frequency | \(f\) | 50 Hz     |
| Sampling frequency  | \(f_s\) | 10 kHz    |
| Load resistance     | \(R\) | 10 Ω      |
| Load inductance     | \(L\) | 5 mH      |
FIGURE 11. Simulation waveforms with the 40% overestimated inductance and the correct resistance under steady-state operation. (a) traditional MPC. (b) fast MPC.

FIGURE 12. Simulation waveforms with the 40% underestimated inductance and the correct resistance under steady-state operation. (a) traditional MPC. (b) fast MPC.

FIGURE 13. Simulation waveforms when the load currents changing based on traditional MPC.

Voltage can be suppressed within the range of upper and lower 3 V.

In order to verify the robustness and stability of the proposed control strategy under steady-state, the output currents simulation waveforms with the 40% overestimated and 40% underestimated inductance as well as the correct resistance are shown in Fig. 11 and Fig. 12, respectively. It can be obtained that the three-phase output current fluctuations under the two control strategies are small when the inductance changes, and the robustness and stability of the proposed control strategy are verified. In addition, comparing with the traditional MPC control strategy, the proposed fast MPC in this paper not only has good robustness and stability, but also reduces the control candidate set and suppresses the common-mode voltage.
C. DYNAMIC -STATE ANALYSIS

The dynamic response test is carried out to further verify the effectiveness of the proposed control strategy, the simulation waveforms of the system are shown in Fig. 13 and Fig. 14.

Under the different control strategies and load conditions, both control strategies stabilize the capacitor voltage on the dc-link at 260 V ($V_{dc}/2$). After the current amplitude increases at $t = 0.05$ s, the capacitor voltage can be kept stable, and the neutral-point potential can be balanced. At the same time, the conventional MPC control strategy maintains a large fluctuation range of common-mode voltage with a maximum amplitude of 175 V under different load conditions. However, the proposed fast MPC strategy maintains the common-mode voltage within the range of upper and lower 3 V under different load conditions, as shown in Fig. 14(d), indicating that the CMV is well suppressed.
D. EXPERIMENTAL RESULTS

In order to verify the robustness and stability of the proposed control strategy under dynamic-state, the output currents simulation waveforms with the 40% overestimated and 40% underestimated inductance as well as the correct resistance are shown in Fig. 15 and Fig. 16. The proposed control strategy still has good robustness and stability under dynamic-state, comparing the three-phase output current fluctuations under the two MPC strategies.

The steady-state experimental waveforms of traditional MPC and fast MPC are shown in Figs. 17 and 18, respectively. The reference frequency is 50Hz, the dc-link voltage is 200V and the load resistance is 10Ω. It can be obtained that the experimental waveforms generated by two strategies coincide with the simulation results. No matter the traditional MPC control or the fast MPC control, the voltages of flying capacitor and the dc-link capacitor are balanced. The flying capacitor voltage are well controlled around the value 50 V. The dc-link capacitor voltages are well controlled around the value 100 V. Furthermore, the common-mode voltage of the fast MPC strategy is obviously less than that of the traditional MPC strategy. The common-mode voltage of the traditional MPC strategy is about 50V, but the common-mode voltage of the fast MPC strategy is lower than 5V. It can be summarized from the steady-state experimental results shown in Figs. 17 and 18 that the proposed fast MPC algorithm has good steady-state performance and capacity in reducing the CMV.

Figs. 19 and 20 show the dynamic experimental results of the load currents changing suddenly. Fig. 19(a) and Fig. 20(a) are the experimental waveforms of common-mode voltage, phase voltage, phase-a and phase-b output currents under the two control strategies, respectively. Fig. 19(b) and Fig. 20(b) are the experimental waveforms of the flying capacitor array (XC6SLX16). The main experimental parameters are shown in Table 5. The experimental results of steady and dynamic processes are shown in Figs. 17, 18, 19 and 20.

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voltage, dc-link capacitor voltages and line voltage under the two control strategies. Fig. 19 and Fig. 20 show that, the phase currents of the two control strategies track well before and after the load mutation. The voltage of the flying capacitor is maintained at 130V, the voltage of the dc-link capacitor is maintained at 260V, and the voltages of the flying capacitor and the dc-link capacitor are balanced. However, the common-mode voltage in Fig. 19 fluctuates between up and down 50V before and after the load mutation, while the common-mode voltage in Fig. 20 does not exceed 1V before the load mutation, and remains within 2V after the load mutation. Similarly, before and after the sudden change of load, the waveform quality of the phase voltage and line voltage in Fig. 20 is obviously better than that of phase voltage and line voltage in Fig. 19.

According to the experimental results of the two control strategies, the fast MPC method based on the switching principle can keep the dc-link capacitor voltages and flying capacitor voltages stable, and has good performance with almost no change in the common-mode voltage under the steady-state and dynamic-state.

VI. CONCLUSION

A fast MPC method based on the switching principle is proposed to solve the problem of the common-mode voltage of the 5 L-NNPP inverter and realize the balance of the dc-link capacitor voltage and flying capacitor voltage. The working mechanism, switching states and switching transitions of the converter are given. The common-mode voltage is suppressed by selecting 19 ZCMV vectors, and the fast MPC candidate control set is reduced according to the switching principle, which greatly reduces the computational burden. In addition, the fast MPC strategy based on the switching principle adopts two-step control, which can reduce the number of weight coefficients and simultaneously realize that the voltage ripples of the common-mode voltage, dc-link capacitor voltage and flying capacitor voltage are controlled very well within a small range.

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**W. Luo et al.** | **CMV Suppression Strategy Based on Fast MPC for Five-Level NNPP Converter** | *IEEE Access* | **142059**

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