VLSI Technology for Cognitive Radio

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Abstract: One of the most challenging tasks of cognitive radio is the efficiency in the spectrum sensing scheme to overcome the spectrum scarcity problem. The popular and widely used spectrum sensing technique is the energy detection scheme as it is very simple and doesn’t require any previous information related to the signal. We propose one such approach which is an optimised spectrum sensing scheme with reduced filter structure. The optimisation is done in terms of area and power performance of the spectrum. The simulations of the VLSI structure of the optimised flexible spectrum is done using verilog coding by using the XILINX ISE software. Our method produces performance with 13% reduction in area and 66% reduction in power consumption in comparison to the flexible spectrum sensing scheme. All the results are tabulated and comparisons are made. A new scheme for optimised and effective spectrum sensing opens up with our model.

Keywords: Optimized flexible sensing, Energy detection, Cognitive radio (CR)

1. INTRODUCTION

Electromagnetic radio spectrum plays an important role in the wireless communication. At present, because of the advent of the development of new wireless technologies, the radio spectrum is being used extensively and has become limited. As a result spectrum sharing has become a challenging task to meet all the emerging technologies. Government agencies have been regulating the task of spectrum allocation and their policy of static spectrum allocation is also adding to the spectrum scarcity problem. To tackle the problem of spectrum sharing, radio spectrum is licensed by several regulatory bodies for various applications. When a certain bandwidth of spectrum is allocated to the primary user, the primary user will not use the complete spectrum, rather some regions are left unused. These unused spectrum locations are called Spectrum holes or White spaces. A secondary user who does not have access to this spectrum tries to make use of these white spaces which are unused by the primary user without interfering with the primary user.

To overcome the problems of spectrum allocation, Cognitive Radio (CR) technology has been proposed as a solution. The main aim of CR is to increase utilization of spectrum by identifying unused as well as under-utilized spectrum in both normal and rapidly changing environmental conditions. Traditionally, four techniques are being mostly used for spectrum sensing. They are matched filter detection, energy detection, waveform based sensing and cyclostationary feature detection. Energy detection is the most extensively used method
because of its simplicity as it do not require any prior knowledge about the input signal. Energy detection technique is used in this paper for reduced complexity

This paper is organized in the following way: Section II shows an optimized flexible spectrum sensing scheme to decrease the complexity of previous structures and gives a description about the whole process involved in this spectrum sensing method. The VLSI architecture of an RDDC and its down converting process are explained in Section III. The output from RDDC is given to the FIR filter one by one and its operation is explained in section IV. Section V gives a detailed explanation about the process sensing the data using energy detection and The VLSI implementation of energy calculation of the signal is given. Experimental results are shown in section VI and finally followed by conclusions.

2. OPTIMIZED FLEXIBLE SPECTRUM SENSING SCHEME

![Optimized flexible spectrum sensing scheme](image)

This consists of an RDDC, a simple FIR filter and energy detection based sensing scheme which is shown in Fig.1. The basic operation of the whole scheme is to first sense the given input into sub parts by down converting them using a RDDC. Then each down converted output is filtered using FIR filter. The filter output is finally given to the energy detection and the energy of the given data is obtained. If this energy value is zero then it is said that the signal is absent and it some energy value is observed then the signal is said to be present.

This scheme consists of the following steps:
1. RDDC is given with the required step input which represents the digital form of the signal.
2. The filter is fixed with predefined filter coefficients.
3. The down converted outputs are then given to FIR filter one by one.
4. The obtained filter output is then given to energy detection for the calculation of energy of the given data.

3. VLSI ARCHITECTURE FOR RDDC

The basic reconfigurable block for a Cognitive Radio implementation is the Digital down converter (DDC). The required frequency band of interest can be shifted down the spectrum with the help of a digital down converter. Due to this the reduction of sample rate can be done and further processing of the required signal of interest may become realizable more easily. Thus by using a DDC, the required band can be selected and its frequency can be converted down to the baseband frequency. The output of the digital down converter will retain all the information regarding our required frequency band of interest but will move it down to baseband and hence the sample frequency can be greatly reduced.
Fig. 2. VLSI architecture of RDDC.

Fig. 2 shows the architecture of the RDDC. RDDC comprises of a counter-AND gate-multiplexer arrangement for setting/changing the reference frequency, two accumulator units (Acc 1 and Acc 2), and a ROM for storing the sine or cosine terms.

4. IMPLEMENTATION OF FIR FILTER

Even though the main functional blocks in the spectrum sensing are down converter for dividing the sub bands and converting it to base band signal and the detection block to detect the actual presence of signal, the filtering operation also requires a complicated architecture to filter the required band and give it to the detection block. So simple filter architecture is used to optimize the area and power constrains to a significant level.

Digital filters are commonly used as an essential element of everyday electronics. FIR filters are one of most important types of digital filters used in Digital Signal Processing. Any type of frequency response can be implemented digitally by using an FIR filter. It is usually implemented with the help of D flip flops, multipliers and adders to obtain the filter output. The basic block diagram of modified FIR filter is as shown in the figure below. The D flip flop acts as a delay element which results in the operation on the prior input signals. The h values are the coefficient values. These are used in the multiplication process so that the output at a particular time will be the sum of all the delayed samples multiplied by their corresponding coefficient values. The process involved in selecting the length of the filter and the coefficient values is known as filter design. The main aim of the filter is to set these parameters in such a way that the desired pass band and stop band parameters are obtained after the operation of the filter.

Depending upon the length, filter response can be improved. That means by using the filter structure with more number of taps, more finely tuned response can be obtained. With predefined length and coefficients, the design of the filter is very straightforward.

Fig. 3. Implementation of FIR Filter.
The modified filter consists of the following steps:

1) Sample the input signal obtained from the RDDC.
2) Insert the newest sample into the circular buffer where the old sample is overwritten here with the new one.
3) Multiply all the previous samples with their appropriate coefficient values. Now their sum becomes the current output.
4) Repeat the above process for all stages and the output of the filter is obtained at the final stage.

Thus the above filter produces a weighted average of its most recent input samples. The key logic of the filter lies in the coefficient values, which dedicate the actual output for a given pattern of input samples. Here the filter is implemented for seven stages. Because of avoiding the usage of multiplexer, the complexity of the filter as well as the area occupied is reduced to a greater extent.

5. ENERGY DETECTION
Energy detection is a simple signal detection method which is referred as radiometry. Practically, energy detector is suitable for wide band spectrum sensing when sufficient information about the PU signal cannot be gathered by the cognitive radio. Energy detection is the mostly suited detection technique because in most of the cases information about the primary user is not known.

5.1 Implementation of energy detection in time domain
A multiplier, adder and followed by a scaling unit can be used to implement the above Eqn. 3 in digital form. To get the squared value of each sample, the received signal samples are given as input to the multiplier. These squared samples are accumulated resulting in summation of squared values. A control signal count is maintained in the accumulator which produces the number of squared samples getting accumulated i.e. the accumulator internally consists of a counter so that the count of number of the samples gets generated. Finally for the process of averaging, the sum of the squared values is passed through scaling unit. Thus the output of scaling unit is the energy of the input digital signal. The energy detector block diagram is shown in Fig. 4.

![Fig. 4. Block diagram of Energy detection.](image)

The first VLSI architecture of energy detector is shown below in Fig. 5. To get the squared values, the input samples are given to a multiplier. The adder and register setup functions as an accumulator. The accumulator keeps on adding its inputs until the register receives a control signal from the counter. The counter and bit wise AND gate outputs logic high when the count of the samples reaches the desired value. This control signal is given to the reset of the accumulator i.e. the accumulator starts from zero when the desired counts of samples are accumulated. Thus the energy detector can output the energy periodically where the period is the time taken to accumulate desire number of samples. Hence, the above energy detector is suitable for real time applications.
6. EXPERIMENTAL RESULTS

The proposed optimized flexible spectrum sensing scheme is implemented in XILINX ISE simulator using verilog coding. The simulation for all the blocks is done separately and the whole scheme is collectively implemented. A step input of 128 bit is given to represent the full cycle of the signal in digital form. The filter is implemented for seven stages and eight input samples were given as address to the ROM in RDDC. These addresses decide the output of the DDC. Finally energy detector gives the energy value of the signal which determines the presence or absence of the signal.

Fig. 6. Simulation results of RDDC

The DDC operation is performed as shown in Fig. 6 and 128 bit step input is divided into eight different 16 bit down converted outputs. Thus the address given decides the output of DDC. The output obtained from the RDDC is fed to the filter one by one. Here the filter is designed for seven stages and the output is obtained by averaging all the previous stage outputs. The final output of filter is shown in Fig.7. Thus the averaged output is a 32 bit output and is an efficient filter output.

Fig. 7. Simulation results of FIR filter
The filter output obtained is given to the energy detection. It squares the input and then scaling is done using a multiply and accumulate arrangement. Finally because of this arrangement, the energy value of the signal is obtained. The energy detection block calculates the energy of the given input as shown in the Fig. 8. If the energy value is 0, then the signal is said to be absent. If any energy value is obtained for the signal, then it is said that the signal is present.

![Fig. 8. Simulation results of energy detector](image)

The above individual blocks are implemented collectively. The final output of the optimized flexible spectrum sensing scheme is shown in Fig. 9. In Fig. 9, the energy value of the data is zero for some time and some energy value is obtained at other time. Zero value indicates the absence of the signal and energy value indicates the presence of the signal. Thus when a digital step input is given to the sensing scheme, depending upon the address selected, it calculates the energy of the signal and tells the presence of signal.

The analysis of the result, power, data path delay and area are calculated for both flexible sensing scheme [3] and optimized flexible sensing schemes and comparisons are done between both the schemes. The comparisons are shown in the Table I below.

The power analysis is observed in the Xpower Analyzer using Xilinx tool. The power consumed by the optimized flexible sensing scheme is reduced when compared to the flexible sensing scheme. The area occupied by LUT’s, IOB’s and number of slices used is observed from the design summary. The data path delay is noted from the synthesis report. The above results prove that the optimized flexible sensing scheme offers better performance with 13% reduced area and 66% reduction in power.

### Table I

| Parameters                  | Flexible sensing scheme | Optimized flexible sensing scheme |
|-----------------------------|-------------------------|----------------------------------|
| Power(W)                    | 0.100                   | 0.034                            |
| Number of slice registers   | 558                     | 522                              |
| Number of slice LUT’s       | 1496                    | 1271                             |
| Number of fully used LUT-FF pairs | 425                      | 328                              |
| Number of bonded IOB’s      | 170                     | 167                              |
| Number of BUFG/BUFGCTRLs   | 5                       | 5                                |
| Number of DSP48E1s          | 12                      | 7                                |
| Total Area                  | 2666                    | 2300                             |
| Delay(ns)                   | 25.136                  | 25.075                           |
| Memory usage(KB)            | 172228                  | 171332                           |
CONCLUSIONS

This paper presents a new optimized flexible sensing scheme to reduce the area and complexity by considering a simple filter structure using D flip flops, multipliers and adders. The area, power and delay constraints are observed using XILINX ISE simulator. The optimized flexible sensing scheme offers better performance with a reduced area when compared to the flexible spectrum sensing technique thus making it a more simple and efficient structure. In the future, the work can be extended by implementing this technique using cooperative spectrum sensing. This sensing scheme can also be implemented using other novel detection techniques like Eigen value based detection to obtain better performance at low signal to noise ratio (SNR).

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