Characterization of various Si-photodiode junction combinations and layout specialities in 0.18µm CMOS and HV-CMOS technologies

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Abstract. With the ongoing miniaturization of CMOS technologies the need for integrated optical sensors on smaller scale CMOS nodes arises. In this paper we report on the development and implementation of different optical sensor concepts in high performance 0.18µm CMOS and high voltage (HV) CMOS technologies on three different substrate materials. The integration process is such that complete modularity of the CMOS processes remains untouched and no additional masks or ion implantation steps are necessary for the sensor integration. The investigated processes support 1.8V and 3V standard CMOS functionality as well as HV transistors capable of operating voltages of 20V and 50V. These processes intrinsically offer a wide variety of junction combinations, which can be exploited for optical sensing purposes. The availability of junction depths from submicron to several microns enables the selection of spectral range from blue to infrared wavelengths. By appropriate layout the contributions of photo-generated carriers outside the target spectral range can be kept to a minimum. Furthermore by making use of other features intrinsically available in 0.18µm CMOS and HV-CMOS processes dark current rates of optoelectronic devices can be minimized. We present TCAD simulations as well as spectral responsivity, dark current and capacitance data measured for various photodiode layouts and the influence of different EPI and Bulk substrate materials thereon. We show examples of spectral responsivity of junction combinations optimized for peak sensitivity in the ranges of 400-500nm, 550-650nm and 700-900nm. Appropriate junction combination enables good spectral resolution for colour sensing applications even without any additional filter implementation. We also show that by appropriate use of shallow trenches dark current values of photodiodes can further be reduced.

1. Introduction
The selection of Si as the starting material for photodiode (PD) fabrication, gives the possibility to monolithically integrate the sensor with the reading circuitry, lowering device costs, and enhancing the sensor capabilities [1]. With the ongoing miniaturization of CMOS technologies the need for integrated optical sensors on smaller scale CMOS nodes arises. In this paper we report on the development and implementation of different optical sensor concepts in high performance 0.18µm CMOS and HV-CMOS technologies. The 0.18µm CMOS and HV-CMOS process technologies offer several junctions with different doping levels and depths which have been investigated as single junction and double junction PDs and have been characterized with respect to their electrical and optical performance.
2. Structures and Measurements
In this section PD layouts and measurement setup are described. Test chips containing various junction combinations were processed in the 0.18µm CMOS and HV-CMOS process options of ams AG [2]. Only standard process steps were used. The only modification was the opening of the passivation nitride layer on top of the PDs in order to minimize multiple reflections and interferences in the illumination path in the dielectric layer stack between top wafer surface and the silicon based diodes.

2.1. Layouts
Figure 1 shows schematics of the single junction PDs processed and measured in the course of this work. For the electrical contact, an anode (A) and a cathode (C) contact are used as indicated in Figure 1a. For the cathode, a contact with the active area of the PD is established by an n+ source/drain doped region. The anode contact is build-up of a p+ source/drain-doping in the p-substrate. Figure 1(c) shows a PD with narrow shallow trench (ST) between cathode and anode. The size of all PDs is 100µmx100µm.

Figure 1. Schematic layout of single junction photodiodes.

Figure 2 shows schematics of the investigated double junction PDs (a and b) as well as a triple junction PD (c). They consist of a combination of p-wells in n-wells in p-substrate, thus forming two or three possible junctions, respectively. The wells used here differ in depth as well as in doping concentration.

Figure 2. Schematic layout of double junction PDs (a and b) and triple junction PD (c).

Three different substrate materials were investigated in the course of this study including lightly p-doped high quality bulk silicon as well as 14µm and 20µm thick lightly p-doped EPI layers on highly p-doped substrates.

2.2. Measurement Setup
To characterize the performance of the PDs we did capacitance (C) and dark current (DC) measurements as well as spectral responsivity (SR) measurements. Measurements have been performed with a Cascade Micromanipulator equipped with thermo chuck. Additionally a HP4284A precision LCR meter was used for C measurements and a Parameter Analyzer HP4155B for DC measurements. DC and C measurements have been performed at a temperature of 60°C. All optical measurements were performed according to the measurement setup depicted in Figure 3. An almost white Xenon lamp is used as light source, which is discrete band filtered in 1nm wavelength steps via a spectrometer. The monochromatic light beam is split, one half goes into a reference detector for
actual power measurement, while the other half is fed onto the optically active area of the device under test. To determine the responsivity of the device under test, the photocurrent generated by the incident light power is measured with a Parameter Analyzer HP4155B. Measurement data recordings as well as filter steering, calibration and reference light power measurements are controlled via serial bus interfaces and personal computers. The optical measurements were done at 0V bias in a wavelength region from 400nm to 900nm.

Figure 3. Experimental setup for spectral responsivity measurements.

3. Results
This section covers spectral responsivity (SR) results as well as dark current (DC) and capacitance (C) values for several PD layouts. The influence of the base material and substrate contact design on these parameters is shown on single junction diodes. On double and triple junction diodes we focus on spectral selection by different shorting methods.

3.1. Results on Single Junction PDs
Measurements have been performed on PDs as depicted in Figure 1.

3.1.1. Influence of base material. Figure 4a is a summary of SR data comparing 3 different base materials. The passivation nitride layer was removed on top of all PDs. Calculated external quantum efficiency (EQE) values of 90% and 100% are also included.

The 0.18µm n-well PDs show a very good EQE about 90% for the spectral range between 480nm to 720nm. For longer wavelengths the influence of the base material can clearly be seen. The bulk material has the highest SR followed by 20µm EPI and 14µm EPI. With increasing wavelength the penetration depth of light in silicon also increases according to Lambert-Beer’s law [1].

Table 1 shows depth values for some selected wavelength values, at which 70% of the incoming light intensity is absorbed in Si. At a wavelength of 850nm 30% of the incoming light is transmitted to a depth of 15µm. So eventually photo generation happens very close or even inside the highly doped EPI substrate where the generated carriers recombine thus decreasing the photocurrent.

DC measurement results on the three base materials are plotted in Figure 4b. DC on EPI wafers is about 4 times lower than on bulk wafers indicating higher lifetime and less defects in the EPI material. Capacitance measurements show no significant difference between different base materials.
3.1.2. Influence of substrate contact layout. This section shows DC measurements at 60°C on PDs with differently designed substrate contacts shown in Figures 1a to 1c. Different depths of p-doped substrate contacts have been studied and also distances between substrate contacts and PD cathode have been varied. In the case of Figure 1c an additional narrow shallow trench (ST) guardring has been added. For a better understanding of the electrical and optical behaviour of the photodiodes presented in this section, two-dimensional TCAD simulations [3] have been performed following our 0.18µm HV process technology and PD layout. DC simulation results presented below utilize standard recombination models including Shockley-Read-Hall and Auger models combined with standard mobility models dependent on the doping concentration, temperature, normal and saturation electrical fields and scattering effects. As DC simulations are uncalibrated the current scale has been omitted in the plots.

Figure 5 shows the influence of p+ substrate contact distance on DC for PDs processed on 20µm EPI substrates together with TCAD simulation results. A smaller distance of the substrate contact to the PD cathode shows smaller DC values, a trend which has also been confirmed by TCAD simulations. The further the substrate contact is away from the PD the larger is the space charge region (SCR) and the higher is the electron generation current and therefore the dark current of the PD.

In Figure 6a we compare DC measurement results of 3 different substrate contact layouts drawn in Figures 1a to 1c. It shows that having a deeper p-well connection to the substrate results in lower DC values compared to shallow p+ substrate contacts. If an additional narrow ST is placed between anode and cathode of the PD dark current values can be reduced further. In Figure 6b we provide the corresponding TCAD simulations which show the same trend as the measurement results.

| Wavelength (nm) | Depth of 70% absorption (µm) |
|-----------------|-----------------------------|
| 410             | 0.14                        |
| 660             | 3.9                         |
| 780             | 10                          |
| 850             | 15                          |

Table 1. Penetration depth of light in silicon.
Figure 5. DC measurement (a) and TCAD simulation results (b) of n-well PDs with p+ substrate contacts at distances of 1µm, 2µm and 5µm from the cathode.

Figure 6. DC measurement (a) and TCAD simulation results (b) of n-well PDs with different substrate contact layouts: p+ contact at a distance of 2µm from the cathode (p+ 2µm), p+ in p-well contact at a distance of 2µm from the cathode (p+ in PW 2µm) and narrow ST between p-well contact and cathode (with ST).

Figure 7 shows the corresponding capacitance results. PDs with the lowest DC values show the highest C values and vice versa. This tendency of increasing capacitance with increasing guard-ring depth is due to narrowing of the SCR and therefore increasing the sidewall capacitance of the structure.

Figure 7. Capacitance results of 0.18µm n-well PDs with different substrate contact layouts.

3.2. Results on Double- and Triple Junction PDs
This section provides an overview of spectral response of PDs consisting of two or three pn-junctions each, as schematically shown in Figure 2. The structures differ in junction-depth and doping
concentration as indicated by the shading. We show that appropriate junction combinations enable good spectral resolution for colour sensing applications even without any additional filter implementation. By shorting one of the two available junctions as indicated in Figure 8 the photocurrent contribution from this junction can be suppressed [4]. Shorting the p+ to the n-well (Figure 8a) blocks the upper junction and carriers generated in this region are forced to recombine and therefore do not contribute to the photocurrent while the lower junction (marked in Figure 8a) is active. In the same way the lower junction can be blocked and the upper junction set active as indicated in Figure 8b.

**Figure 8.** Shorting modes of double junction PDs: (a) n-well to p-substrate junction is activated; (b) shallow p+ to n-well junction is activated.

Figure 9 shows a comparison of the SR data as a function of wavelength for p+ in n-well in p-substrate PDs (a) and p-well in deep n-well in p-substrate PDs (b). Applied shortings are indicated in the legend.

**Figure 9.** SR of double junction PDs under different shorting conditions: p+ in n-well in p-substrate (a) and p-well in deep n-well in p-substrate (b).

For the n+ in p-well in deep n-well in p-substrate triple junction PD the applied shorting variations are shown in Figure 10. Active pn-junctions are again marked.

**Figure 10.** Shorting modes of triple junction PD: (a) deep n-well to p-substrate junction is activated; (b) p-well to deep n-well junction is activated; (c) n+ to p-well junction is activated.
Corresponding SR data for the three different shorting variations of the triple junction PD are shown in Figure 11.

![Figure 11. SR of n+ in p-well in deep n-well in p-substrate triple junction PD under different shorting conditions.](image)

As can be seen in Figures 9 and 11 spectral response of junction combinations can be optimized for peak sensitivities in the range of 400-500nm, 550-650nm or 700-900nm. By appropriate junction choice the ratios of the generated photo currents in their respective peak zones can exhibit more than a factor of 10 compared to the other photo diode combinations. This enables a fairly good spectral resolution for colour sensing applications without any filters.

4. Conclusion

It was shown by TCAD simulations as well as measurement data that different substrate contact designs available in 0.18µm CMOS and HV-CMOS processes help to lower the dark current values of PDs. Moreover by exploiting the wide variety of junctions available in these processes, the spectral responsivity of PDs can be optimized for peak sensitivities in the ranges of 400-500nm, 550-650nm or 700-900nm, thus offering the possibility to provide a very good spectral resolution for colour sensing applications without filters.

References

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