Parameter extraction and modelling of the MOS transistor by an equivalent resistance

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\textbf{ABSTRACT}
During the analysis of multi-transistor circuits, the need arises to evaluate the time delay or the power consumption of the circuit. Due to the complexity of the transistor model, several complicated equations arise from which a compact-form solution cannot be obtained and a suitable physical insight cannot be drawn. With this regard, two contributions are presented in this paper. The first one is a fully analytical parameter extraction approach to be applied on the MOS transistors. The second one is a quantitative method for simplifying the analysis of MOS circuits by modelling the MOS transistor by a suitable equivalent resistance adopting the time-delay or the power-consumption equivalence criteria. The parameter-extraction method is verified by using the extracted parameters in the derived expressions according to the second contribution. Compared to other representations, the agreement of the proposed model with the simulation results is very good.

\textbf{I. Introduction}
Modelling the MOS transistor is a very complicated task that was the topic of interest for myriad of researchers in the last few decades [1–12]. With the scaling down of the channel length of the MOS transistor, several second-order effects arise that cannot be neglected in today’s deep-submicron devices including the velocity saturation, mobility degradation, changing the threshold voltage with the channel length and the channel width, to name such a few [1,13], and [14]. The main purpose of analysing digital CMOS circuits is to obtain first-order estimates for the propagation delay and the power consumption and develop physical insights into the parameters that affect the performance of the circuit significantly. It is expected that the analysis of circuits including several N-channel and P-channel MOS devices is a formidable task. As a result, very complicated expressions that cannot be solved in a compact form are obtained. As a simplification to the analysis of multi-transistor circuits, the MOS transistor can be represented by a suitable equivalent resistance. In this paper, circuits containing only
MOS transistors and capacitors are referred to as transistor-like circuits while those that contain only resistances and capacitors are referred to as resistance-like circuits.

In this paper, two contributions are presented in the realm of modelling the MOS transistors in complicated circuits. The first one is a parameter-extraction method that is proposed for extracting suitable values for the parameters of the MOS transistor in accordance with the adopted model. The second one is a quantitative method for the evaluation of the equivalent resistance representing the transistor adopting one of the following two criteria; the 50% time delay of the resistance-like circuit is equal to that of the transistor-like circuit or the rise (or fall) times of the two circuits are equal. The equality of the 50% time delay guarantees that the propagation delays of the two circuits are equal while the equality of the rise or fall times guarantees that the short-circuit power consumption of the driven stage for the two circuits are equal. The rise (or fall) time is evaluated between the 90% and 10% time instants for the output waveform [15].

There are three important benefits that can be gained from representing the transistor by an equivalent resistance. The first and the most common one is the evaluation of the low-to-high and the high-to-low propagation delays of a CMOS circuit. In this case, the circuit simplifies to an RC circuit. The second aspect is the evaluation of the signal integrity by evaluating the rise or the fall times of the output waveforms of a CMOS circuit. The third aspect is the evaluation of the short-circuit power consumption which is related to the rise and fall times of the driving signal.

The remainder of this paper is organized as follows: A short discussion on the parameter extraction is presented in Section II along with the proposed approach. Section III presents the quantitative evaluation for finding the equivalent resistance of the MOS device considering the previously stated criteria preceded by a short discussion on the previous work in this realm. The simulation results are presented in Section IV. Finally, the paper is concluded in Section V.

II. Parameter extraction

Before describing the method of parameter extraction, the adopted MOSFET model is first presented.

A. Adopted MOSFET model

According to the adopted model, the current-voltage relationship in the subthreshold region of the NMOS devices is as follows [16]:

\[ i_D = I_{on} e^{\frac{V_{GS}-V_{thn}}{V_{thn}}} \left( 1 - e^{\frac{V_{DS}}{V_{thn}}} \right) \]  

(1)

where \( I_{on} \) is given by

\[ I_{on} = \mu_{on} C_{oxn} \left( \frac{W}{L} \right)_n (n_n - 1) V_{thn}^2 \]  

(2)

\( i_D \) is the drain current, \( \mu_{on} \) is the electron mobility, \( C_{oxn} \) is the gate-oxide capacitance per unit area, \( W \) is the channel width, \( L \) is the channel length, \( (W/L)_n \) is the aspect ratio, \( V_{thn} \)
is the threshold voltage, $v_{GS}$ is the gate-to-source voltage, $v_{DS}$ is the drain-to-source voltage, and $V_{th}$ is the thermal voltage which can be found from

$$V_{th} = \frac{KT}{q}$$

(3)

$K$, $q$, and $T$ are Boltzmann’s constant, the electronic charge, and the absolute temperature, respectively. Eq. (1) is valid for $v_{GS} < V_{thn}$. $n_n$ is the subthreshold-swing coefficient which is given by [17]

$$n_n = 1 + \frac{C_d}{C_{oxn}}$$

(4)

where $C_d$ is the depletion-layer capacitance per unit area. When $v_{GS}$ is larger than $V_{thn}$, the device operates in the triode or the saturation region. In the triode and saturation regions, the current-voltage relationships are

$$i_D = \mu_{effn} C_{oxn} \left( \frac{W}{L} \right) n \left[ (v_{GS} - V_{thn}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

(5)

and

$$i_D = W_n C_{oxn} v_{sath}(v_{GS} - V_{thn})(1 + \lambda_n v_{DS})$$

(6)

respectively. $v_{sath}$ is the free-electron saturation velocity and $\lambda_n$ is the channel-length modulation effect parameter. $\mu_{effn}$ is the effective mobility of free electrons which can be expressed as [18]

$$\mu_{effn} = \frac{\mu_{0n}}{1 + \theta_n (v_{GS} - V_{thn})}$$

(7)

$\mu_{0n}$ is the mobility of free electrons at low vertical electric fields across the gate oxide and $\theta_n$ is the mobility-degradation effect parameter. The edge of saturation is at $v_{DS} = V_{DSsat}$ and is given by

$$V_{DSsat} = (1 - k)(v_{GS} - V_{thn})$$

(8)

So, Eqs. (5) and (6) are valid for $v_{DS} < V_{DSsat}$ and $v_{DS} \geq V_{DSsat}$, respectively. Taking into account that the value of $k$ is very small [19], its effect will be neglected here. Due to the drain-induced barrier lowering (DIBL) and body effects, $V_{thn}$ changes with $v_{DS}$ and $v_{BS}$ (the body-to-source voltage), respectively. This change can be modelled by the following relationship [20]:

$$V_{thn} \approx V_{thn0} - \gamma_n v_{BS} - \eta_n v_{DS}$$

(9)

$V_{thn0}$ is the threshold voltage at $v_{DS} = v_{BS} = 0$ V. $\gamma_n$ and $\eta_n$ are the linearized body-effect parameter and the DIBL parameter, respectively. For typical values of $\eta_n$, the change of $V_{thn}$ with $v_{DS}$ can be safely neglected.

### B. Previous work

Simply stated, the model is defined as the set of equations that properly emulate the behaviour of the component. In order to perform accurate and reliable IC design
especially in the analog realm, accurate device models must be adopted. Device modelling can be performed by one of three approaches [21]. The first approach is a physics-based approach (also known as the analytical approach) in which the model parameters are closely related to the physical operation of the device and its operating regions. As a result, the extracted parameters are relatively very few and the results are rather inaccurate [14,22], and [23]. So, this approach is best suited to the application with simple device structures. The second approach is a best-fitting one (also known as the numerical approach) in which the parameters of the device model is fitted to the experimental results so that the accuracy will be enhanced. The third and final approach is a combination of these two approaches as a compromise between the accuracy and potential of physical interpretation.

The parameter extraction is the process of finding suitable values for the parameters of the model such that the measurement results and simulation results will be close to each other [24]. Parameter extraction is an important step in order to ensure the accuracy of the simulation results and its closeness to the experimental results.

Another reason for the importance of the parameter extraction is as follows: In order to get a physical insight into the performance of the circuit at hand and to find first-order estimates for the performance metrics, a hand quantitative analysis should be performed. To ensure the potential of deriving simple and accessible compact forms, the parameters of the adopted model hardly exceed ten. However, the models adopted for the device in the simulation program may contain hundreds of parameters. Thus, to obtain rather accurate results from the quantitative analysis, the accuracy of the adopted parameters must be guaranteed; hence the need for accurate parameter extraction. The link between the process characterization and the circuit simulation deserved a lot of research [25]. In fact, this point was the topic of many research papers.

The parameter extraction methods can be classified into two main approaches; optimization-based approaches and analytical approaches. According to the first one, the parameters extracted cover the complete operating range with suitable fitting algorithms applied but requires a relatively large time due to the need to deal with a large number of measurements [26] and [27]. The opposite is true for the second approach in which compact forms are derived for estimating the required parameters [28]. There are several methods for parameter extraction that vary in their accuracy and requirements in computer time [29].

Some of the techniques used with parameter extraction are associated with extracting accurate values for the parameters of the model used in the simulation with regard to the experimental measurements [30]. However, the parameter extraction performed here is associated with extracting accurate values for the parameters of the model used in the quantitative analysis from the simulation results, i.e., the approach presented for parameter extraction is such that the simulation results and analysis results will be close to each other. Specifically, due to the negligence of many short-channel effects in the adopted model in the analysis, this model is not appropriate for use with short-channel devices. The parameter-extraction process bridges the gap between the inaccurate simple MOSFET model and the rather accurate simulation results. The parameter extraction is performed using the MATLAB program. The procedure described in this paper for parameter extraction is simple, easy, fully analytical, and general in the sense that it
can be applied on the experimental results equally well as on simulation results. Also, it can be applied on conventional silicon and GaAs devices.

**C. Proposed parameter-extraction approach**

In order to extract the parameters of the MOSFET model presented earlier, the MOSFET transistor is attacked by several excitation sources and the responses are determined by simulation. Using the simulation results, the necessary model parameters can be extracted. In order to guarantee that the extracted parameters are a good representation of the transistor performance over the whole operating region, several information at different biasing values are used. Since the procedure can be applied on NMOS and PMOS devices as well, it is illustrated for the NMOS devices only.

1. **Extracting $V_{thno}$**

   Since the subthreshold current is not negligible, the $i_D$-$v_{GS}$ characteristics does not intersect the $v_{GS}$ axis at the threshold voltage. So, the threshold voltage is taken here as the intercept of the linear portion of the $i_D$-$v_{GS}$ characteristics with the horizontal axis as shown in Figure 1. Instead, for more accurate results, the $i_D$-$v_{GS}$ characteristics can be plotted for several values of $v_{DS}$ conditional that the range swept for $v_{GS}$ is such that the transistor will operate in the saturation region. This is to ensure that Eq. (6) is valid and the required intercept is $V_{thno}$. Then, the average of the extracted values is taken. The two functions, *polyfit* and *mean*, are used in finding the coefficients of the line that best fits the acquired data in MATLAB and the average of the extracted values, respectively.

![Figure 1](image.png)

*Figure 1.* Finding $V_{thno}$ as the intercept of the linear portion of the $i_D$-$v_{GS}$ characteristics with the horizontal axis. The curve corresponds to $v_{DS} = 1$ V. The term ‘exact relationship’ means data from the simulation results.
2. Extracting $\lambda_n$

As known, the Early voltage is simply the negative of the intersection of the $i_D$-$v_{DS}$ characteristics with the horizontal axis and the channel-length modulation effect parameter is its inverse. So, the procedure of finding the threshold voltage can be applied equally well in this context. Several values of $\lambda_n$ can be found from the slopes of the $i_D$-$v_{DS}$ curves at different values of $v_{GS}$ and then $\lambda_n$ is taken as their average. Again, the chosen values for $v_{GS}$ and $v_{DS}$ must ensure operating the transistor in the saturation region so that Eq. (6) will remain valid.

3. Extracting $C_{oxn}v_{satn}$

Since $C_{oxn}$ and $v_{satn}$ are multiplied by each other in Eq. (6) for the drain current in saturation, there is no way to find the value of each of them from the transistor characteristics. Fortunately, there is no need to find the value of each of them separately; there is a need to find their product. The same can be said about $\mu_{on}$ and $C_{oxn}$. Simply stated, find the drain current for certain values of $v_{GS}$ and $v_{DS}$ such that the transistor operates in the saturation region and Eq. (6) will be valid. Then, $C_{oxn}v_{satn}$ can be found from

$$C_{oxn}v_{satn} = \frac{i_D}{W_n(v_{GS} - V_{thn})(1 + \lambda_n v_{DS})} \quad (10)$$

4. Extracting $k_n'$ and $\theta_n$

There are two methods for determining $k_n'$ (the process-transconductance parameter which is equal to $\mu_{on}C_{oxn}$) and $\theta_n$. The two methods depend on Eq. (5). The first one depends on the deep-triode region in which $v_{DS}$ is much smaller than $2(v_{GS} - V_{thn})$. In this case, the $i_D$-$v_{DS}$ relationship is almost linear with a slope equal to

$$\frac{di_D}{dv_{DS}} = \mu_{effn}C_{oxn} \left(\frac{W}{L}\right) n (v_{GS} - V_{thn}) \quad (11)$$

So, this slope can be found for any two values of $v_{GS}$ such that the transistor operates in the deep-triode region and $k_n'$ and $\theta_n$ can be determined. The other method is as follows: Since $k_n'$ and $\theta_n$ are not multiplied by each other in Eq. (5), a simple way for finding each of them is to find the drain currents for two different sets of values for $v_{GS}$ and $v_{DS}$ such that the transistor will operate in the triode region and Eq. (5) will be valid. From Eqs. (5) and (7), we can get

$$k_n'(\frac{W}{L}) n = \frac{i_D}{1 + \theta_n(v_{GS} - V_{thn})} = \frac{i_D}{\left[(v_{GS} - V_{thn})v_{DS} - \frac{1}{2}v_{DS}^2\right]} \quad (12)$$

from which $k_n'$ and $\theta_n$ can be determined. Although the first method is easier, it is less accurate due to neglecting the term, $0.5v_{DS}^2$. So, the second method is adopted here.

5. Extracting $\gamma_n$ and $\eta_n$

One way for finding $\gamma_n$ is to first find $V_{thn0}$ as discussed previously by putting $v_{BS}$ equal to 0 V (with the change of $V_{thn}$ with $v_{DS}$ neglected), then finding $V_{thn}$ for any different value of $v_{BS}$. The procedure is nothing but solving Eq. (9) with $\eta_n$ neglected. Another procedure
for determining $V_{thn}$, $\gamma_n$, and $\eta_n$ is as follows: Plot $V_{thn}$ versus $v_{BS}$ and find the best straight-line fit to the plot; the slope of the resulting line is $-\gamma_n$. It must be noted that the adopted value of $v_{DS}$ must be such that the transistor operates in the saturation region for all cases. This is in order to ensure the validity of Eq. (6) and that the extracted $V_{thn}$ is simply the horizontal intercept of the linear portion of the $I_D-V_{GS}$ relationship. In fact, the effect of the term, $\eta_n v_{DS}$, in this case is just a shift in the value of $V_{thn}$ with the extracted value of $\gamma_n$ not affected. As will be seen shortly, the extracted value of $\eta_n$ is relatively small. So, the effect of the term, $\eta_n v_{DS}$, can be safely neglected in this case. The adopted value of $v_{DS}$ is 1 V. This procedure can be repeated for the relationship between $V_{thn}$ and $v_{DS}$ with $v_{BS}$ equal to 0 V. Refer to Figures 2 and Figures 3 for the plots of the threshold voltage versus $v_{BS}$ and $v_{DS}$, respectively, according to the extracted data and the best straight-line fit.

Figure 2. The extracted data and the best straight-line fit for the relationship between $V_{thn}$ and $v_{BS}$.

Figure 3. The extracted data and the best straight-line fit for the relationship between $V_{thn}$ and $v_{DS}$.
6. **Extracting $I_{on}$ and $n_n$**

The first direct method for finding $I_{on}$ and $n_n$ is to find the drain currents ($i_{D1}$ and $i_{D2}$) for two sets of values of $v_{GS}$ ($v_{GS1}$ and $v_{GS2}$) and $v_{DS}$ ($v_{DS1}$ and $v_{DS2}$) such that $v_{GS}$ is smaller than $V_{thn}$ and the transistor operates in the subthreshold region. From Eq. (1), we can get

$$i_{D1} = I_{on} e^{\left(\frac{v_{GS1} - V_{thn}}{n_n V_{th}}\right)} \left(1 - e^{\frac{-v_{DS1}}{V_{th}}}\right)$$

and

$$i_{D2} = I_{on} e^{\left(\frac{v_{GS2} - V_{thn}}{n_n V_{th}}\right)} \left(1 - e^{\frac{-v_{DS2}}{V_{th}}}\right)$$

In Eqs. (13) and (14), the body and the DIBL effects were neglected. After simple mathematical manipulations, we can write

$$n_n = \frac{v_{GS1} - v_{GS2}}{V_{th} \ln \left[\frac{i_{D1}}{i_{D2}} \frac{1 - e^{\frac{-v_{DS1}}{V_{th}}}}{1 - e^{\frac{-v_{DS2}}{V_{th}}}}\right]}$$

$I_{on}$ can then be determined from Eq. (13) or (14). Another method for determining $I_{on}$ and $n_n$ is from the slope of the drain current in the subthreshold region. From Eq. (1), if $v_{DS}$ is larger than $V_{th}$ such that the term, $e^{(-v_{DS}/V_{th})}$, is much smaller than 1, we can write

$$\ln i_D = \left(\frac{v_{GS} - V_{thn}}{n_n V_{th}}\right) + \ln I_{on}$$

which is a straight-line equation with vertical intercept equal to $\ln I_{on} - V_{thn}/(n_n V_{th})$ and slope equal to $1/(n_n V_{th})$. So, $I_{on}$ and $n_n$ can be determined.

7. **Extracting the internal capacitances**

As known, some of the internal capacitances of the MOSFET transistor are voltage dependent. For simplicity, all the internal capacitances at all the transistor terminals will be treated as voltage independent; however, they are size-dependent [31]. In order to determine the parasitic capacitance at a certain terminal of the device, this terminal must be attacked by a proper voltage or current source with a properly series or parallel resistance, then a transient analysis is performed. In the following, two methods for extracting the values of the internal capacitances associated with the four terminals are discussed. Let us illustrate these two methods in detail with regard to the gate terminal taking into account that the same procedure can be applied equally well on the other terminals.

The first method depends on applying a current source with a constant value at the gate terminal of the MOS transistor with the other terminals grounded as shown in Figure 4. If the gate contains only a capacitive impedance, the gate voltage is expected to increase linearly with a constant charging rate equal to $I/C_G$ where $I$ is the value of the charging current source and $C_G$ is the parasitic capacitance at the gate terminal. However, this is not the case as shown in Figure 5. Specifically, the instantaneous gate voltage, $v_G$, increases with a rather constant rate only at the beginning of the charging process, then
the charging rate decreases until $v_G$ saturates. The kink noted at the curve of Figure 5 before $t = 0.1$ ns can be attributed to the voltage dependence of $C_G$ on $v_G$.

It can be concluded that the gate does not simply contain a capacitance only; it may contain inductance and resistance as well. For the channel lengths and the frequencies of operation of interest, the effect of the parasitic inductance can be safely neglected [32]. The equivalent circuit of the gate is thus as shown in Figure 6 where $R_G$ represents the parasitic resistance of the gate terminal. In order to decide on the nature of $R_G$, current sources with different values are applied. The results are shown in Figure 7 for $I$ equal to 1

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**Figure 4.** The application of a constant current source at the gate terminal of the MOSFET transistor.

**Figure 5.** The gate voltage as a function of time for $I$ equal to 100 nA.

**Figure 6.** The equivalent circuit seen at the gate terminal.
It is obvious that increasing $I$ not only speeds-up the charging process but also causes the steady-state gate voltage, let it be $V_G$, to increase as expected. From Figure 6, $V_G$ is equal to $IR_G$. However, the resulting values of $V_G$ does not increase in direct proportion to $I$; rather, it increases at a smaller rate. Specifically, the three values of $V_G$ are 0.47 V, 0.9 V, and 1.4 V for $I$ equal to 1 nA, 10 nA, and 100 nA, respectively. So, $R_G$ is not constant but changes with $V_G$ in an inverse manner. This can be confirmed by Figure 8 which shows the $i_G$-$v_{GS}$ characteristics and Figure 9 which shows the relationship between $R_G$ and $v_{GS}$.

In order to find $C_G$, the 50% time delay of the charging process must first be found. Due to the voltage dependence of $R_G$, the differential equation describing the circuit of...
Figure 6 will not be with constant coefficients. So, no compact form of the 50% time delay can be derived and thus treating with the gate voltage of Figure 6 is not a practical way. On the other hand, the current applied on the gate terminal is constant and thus as an alternative way, $C_G$ can be found from the following relationship:

$$C_G = \frac{It}{\Delta V_G}$$  \hspace{1cm} (17)

where $t$ and $\Delta V_G$ (the change of the gate voltage) can be found from the plot of $v_G(t)$ in the linear range. Refer to Figure 10 for the relationship between the extracted values of $C_G$.

Figure 9. The relationship between $R_G$ and $v_{GS}$.

Figure 10. The extracted values of $C_G$ versus the constant current-source value.
and the constant current-source value. Figure 11 shows the relationship between the aspect ratio and the extracted values of $C_G$ which confirms the direct proportionality.

The second method for determining $C_G$ depends on applying a dc voltage source, $V_{GG}$, in series with a resistance, $R$, on the gate terminal of the MOSFET transistor with the other terminals grounded as shown in Figure 12. If the voltage source is connected directly to the gate terminal, the gate voltage will be equal to $V_{GG}$ at all cases and there will be no way of discovering the gate equivalent circuit. If the gate contains a capacitance only, the steady-state gate voltage, $V_G$, will be constant irrespective of the value of $R$. However, this is not the case; rather, $V_G$ decreases with increasing $R$ as indicated in Figure 13. So, the gate contains a resistance, $R_G$, as concluded in the illustration of the first method and illustrated in Figure 14. In order to avoid the effect of the voltage dependence of $R_G$ on $V_G$, relatively small values of $R$ are adopted so that the steady-state gate voltage will be constant at $V_{GG}$. As a result, the instantaneous gate voltage is described by the following relationship:

\[
V_G = \frac{V_{GG}}{1 + R/R_G}
\]

Figure 11. The relationship between the aspect ratio of the MOSFET transistor and the gate parasitic capacitance for $I = 10 \, \mu A$.

Figure 12. Applying a dc voltage source in series with a resistance on the gate terminal to find the value of $C_G$. 
The 50\% time delay is accordingly given by
\[ t_{50\%} = \ln(2)RG \]  
(19)

So, the gate capacitance can be evaluated from
\[ C_G = \frac{t_{50\%}}{(\ln 2)R} \]  
(20)

**Figure 13.** The relationship between the series resistance connected to the gate terminal and the steady-state gate voltage for $V_{GG} = 1$ V.

**Figure 14.** The equivalent circuit of the circuit of Figure 12

\[ v_G(t) = V_{GG} \left( 1 - e^{-\frac{t}{RC_G}} \right) \]  
(18)

**Figure 15.** shows the extracted values of $C_G$ for different values of $V_{GG}$. The estimated $C_G$ according to this method is thus close to that estimated by the first one. These two approaches can be applied on the other three terminals to find their associated parasitic capacitances taking into account these two points. First, the second method requires adopting a relatively small value for the serially connected resistance compared to the parasitic resistance of the terminal at hand so that the steady-state voltage at that terminal is equal to the applied one. This ensures that the voltage dependence of the parasitic resistance at that terminal will not affect the evaluation of the 50\% time delay and hence the extracted capacitance at that terminal. The second point is that when determining the
values of $C_D$, $C_B$, and $C_S$, the transistor must be deactivated in order to ensure that the applied current or voltage source charges the parasitic capacitance at the specified terminal at hand with no leaked current into that terminal. The list of the extracted parameters of the NMOS device to be used in the next section are shown in Table 1. The equality of $C_D$ and $C_S$ makes sense as the MOSFET is a bidirectional device with the drain and source terminals interchangeable.

### III. Finding the mosfet equivalent resistance

#### A. Previous work

There were previous attempts for representing the transistor by an equivalent resistance; however, very limited previous work was reported in this realm. In fact, most of the previous work related to this realm lies in estimating the parasitic resistances of the transistors [31–38] or modelling the dependence of the current of the transistor on a certain voltage difference [39]. In [40], an empirical $RC$ model for the transistor was

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**Table 1.** The list of the extracted parameters of the NMOS device.

| Parameter                                | Value       |
|-----------------------------------------|-------------|
| Threshold voltage                       | 0.27 V      |
| Process-transconductance parameter      | 740 $\mu$A/V$^2$ |
| Channel-length modulation effect parameter | 0.38 $V^{-1}$ |
| $C_{G_{satn}}$                           | 1600 $A/Vm$ |
| Mobility-degradation effect parameter   | 2.66 $V^{-1}$ |
| Linearized body-effect parameter        | 0.14        |
| DIBL parameter                          | 0.08        |
| Subthreshold-swing coefficient          | 1.72        |
| $I_0$ (a constant related to the subthreshold operation) | 3.7 $\mu$A |
| Internal capacitances                   |             |

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presented based on the equivalence of the time delay. The effective resistance according to this model depends on the type, size, and external connections of the transistor, the load, and the waveform of the input signal.

One of the most simple methods is representing the transistor by a resistance equal to the ratio between the drain-to-source voltage and the drain current in a certain region of operation. This includes representing the MOS transistor as a voltage-controlled resistance if it operates in the deep-triode region; that is, with $v_{DS} \ll 2(v_{GS} - V_{thn})$. The equivalent resistance, $R$, in this case is given by the ratio between the drain-to-source voltage and the drain current as follows [15]:

$$R = \frac{1}{k_n'(\frac{W}{L})_n(v_{GS} - V_{thn})}$$

(21)

Obviously, the term $0.5v_{DS}^2$ was neglected in Eq. (21). However, this representation is valid only for a limited range of voltages; specifically for $v_{DS} < 0.2(v_{GS} - V_{thn})$ which is typically smaller than 0.15 V for deep-submicron CMOS technologies. Alternately, in the saturation region, the equivalent resistance can be estimated as the ratio between $v_{DS}$ and $i_D$ with both $v_{DS}$ and $v_{GS}$ equal to the power-supply voltage, $V_{DD}$ [41];

$$R = \frac{V_{DD}}{\frac{1}{2}k_n'(\frac{W}{L})_n(V_{DD} - V_{thn})^2}$$

(22)

Since the device usually operates part of the time in the saturation region and another part in the triode region, a combination of these two regions can be performed by evaluating the equivalent resistance at the edge of saturation with $v_{GS} = V_{DD}$ and $v_{DS} = V_{DD} - V_{thn}$ as follows [41]:

$$R = \frac{2}{k_n'(\frac{W}{L})_n(V_{DD} - V_{thn})}$$

(23)

In [15], an empirical estimation was adopted for the equivalent resistances of the NMOS and PMOS devices in estimating the charging and discharging time delays with the inverse dependence between the equivalent resistances and the aspect ratios, $(W/L)_n$ and $(W/L)_p$, taken into account. According to this estimation, the equivalent resistances of the NMOS and PMOS devices are given by

$$R_N = \frac{12.5}{(W/L)_n} k\Omega$$

(24)

and

$$R_P = \frac{30}{(W/L)_p} k\Omega$$

(25)

respectively. It must be noted that the factors, 12.5 and 30, adopted in Eqs. (24) and (25) depend on the technology. It has been found that these values apply well for a number of processes including the 0.25 μm, 0.18 μm, and 0.13 μm CMOS processes [42]. Although estimating the performance of the circuit using these estimated equivalent resistances is
simple, several parameters were not taken into account such as the threshold voltage and the short-channel effects.

In [43], three methods were proposed for estimating the equivalent resistance of the MOS transistor. The first one is finding the ratio between the average drain-to-source voltage and the average drain current, $i_{D\text{avg}}$, with the average for each of them evaluated simply as the arithmetic average for the two values at the onset and end of the mode of operation of interest. The drawback of this method is that the estimated equivalent resistance depends on the output voltage of the circuit, which is not a transistor parameter; this is really the case with CMOS-transmission gates. The second method is using integration for estimating the average drain current as follows:

$$i_{D\text{avg}} = \frac{1}{v_{DSf} - v_{DSi}} \int_{v_{DSi}}^{v_{DSf}} i_D d v_{DS}$$  \hspace{1cm} (26)

According to Eq. (26), $i_D$ is expressed as a function of $v_{DS}$ with the other voltages such as $v_{GS}$ and $v_{DS}$ substituted by their average values over the same range. $v_{DSi}$ and $v_{DSf}$ certainly represent the values of $v_{DS}$ at the onset and end of the respective mode of operation. The third method depends on using the following integration [31] and [44]:

$$R = \frac{1}{v_{DSf} - v_{DSi}} \int_{v_{DSi}}^{v_{DSf}} \frac{v_{DS}}{i_D} d v_{DS}$$  \hspace{1cm} (27)

where $i_D$ is to be expressed as a function of $v_{DS}$. Although these compact forms for the equivalent resistance are more accurate than the formula of the deep-triode region, the propagation delay as well as the power consumption estimated in these ways are relatively inaccurate.

In this paper, more accurate compact forms are derived for the equivalent resistance such that each of the propagation delay and the rise and fall times evaluated using the equivalent-resistance circuit and the original circuit containing the MOSFET devices are equal. The main advantages of the proposed equivalent-resistance representation are:

1. The availability of a compact mathematical model with a relatively small number of components.
2. The accuracy is better in estimating the propagation delay and the power consumption.
3. The derivations of all the compact forms are straightforward with no need to deal with numerical analysis techniques, so it is relatively fast.
4. Finally, the derived expressions can be applied to any CMOS technology by substituting the values of the model parameters in the respective derived resistance expressions. There are neither empirical nor fix-up parameters that certainly depend on the adopted technology.

However, all these merits come at the expense of more complicated expressions; an expected demerit, since the accuracy is usually traded-off with simplicity. Also, since the derived resistance expressions are based on performance metrics related to digital signals, it must be noted that they are not suitable for use with analog signals.
B. Quantitative analysis

There are four cases that can be considered in the evaluation of the propagation delay in digital CMOS circuits. The first one is the discharging of a load capacitance, \( C_L \), through a single NMOS device. The second case is the discharging of \( C_L \) through serially or parallel connected NMOS devices. The third case is the discharging of \( C_L \) through the pull-down network (PDN) while there is a contention current from a PMOS load. The fourth and final case is the charge sharing between two capacitors through an NMOS device. The analysis for finding the equivalent resistance is performed for the NMOS case; PMOS-case expressions can be obtained in the same way with the parameters of the NMOS replaced by the PMOS ones.

Throughout the analysis performed in this paper, the load capacitance will be assumed to be much larger than the internal capacitances of the MOS transistors. This assumption is justified by the following reasoning: The load capacitance comprises three subcomponents; those due to the internal capacitances of the transistors in the driving stage, the interconnection line between the driving and the driven stages, and those due to the internal capacitances of the transistors in the driven stages. Taking into account that the percentage of the delay due to the interconnection lines increases with technology scaling [20,45–48], the parasitic capacitances due to the transistors of the driving stage can be safely neglected.

According to the proposed equivalence, the equivalent resistance neither will be evaluated using an integration nor will depend on certain voltages or currents in the circuit. The parameters of [49] are adopted in the following plots and all the devices are assumed to be minimum-sized unless otherwise specified. The parameters extracted using the previously presented extraction approach is used in the following analyses.

1. The first case

Now, refer to Figure 16 (a) for a simple NMOS transistor discharging a capacitance, \( C_L \), which is initially charged to \( V_{DD} \) and to Figure 16 (b) for its equivalent circuit in which the NMOS device is replaced by an equivalent resistance, \( R \). This is typically the case in the CMOS inverter when the input voltage is equal to the power-supply voltage, \( V_{DD} \). The purpose now is to find an expression for \( R \) in terms of the device dimensions and process parameters such that the 50% propagation delay, \( t_{50\%} \), or the fall time, \( t_f \), of the transistor-like circuit are equal to their counterparts of the resistance-like circuit. \( t_f \) is evaluated as the difference between the 10% and 90% points, \( t_{10\%} - t_{90\%} \). During the time interval of the discharging of \( C_L \), \( M_N \) operates in either the saturation or the triode region depending on

\[
\begin{align*}
&v_{\text{in}} & \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \Quad
\(v_{CL}\) (the voltage across \(C_L\)). In the saturation region, the discharging process is described by the following differential equation (where \(v_{DS}\) is substituted by \(v_{CL}\)):

\[
-C_L \frac{dv_{CL}}{dt} = W_n C_{oxn} v_{satn}(V_{DD} - V_{thn})(1 + \lambda_n v_{CL})
\]

(28)

So, \(v_{CL}(t)\) is given by

\[
v_{CL}(t) = \left(\frac{1}{\lambda_n} + V_{DD}\right) e^{-\frac{W_n C_{oxn} v_{satn}(V_{DD} - V_{thn})}{C_L} t} - \frac{1}{\lambda_n}
\]

(29)

\(M_N\) leaves the saturation region at \(t = t_{sat}\) when \(v_{CL}\) reduces below \(V_{DD} - V_{thn}\). So,

\[
t_{sat} = \frac{C_L}{W_n C_{oxn} v_{satn}(V_{DD} - V_{thn})} \ln \left[\frac{1 + \lambda_n V_{DD}}{1 + \lambda_n (V_{DD} - V_{thn})}\right]
\]

(30)

When \(v_{CL}\) becomes smaller than \(V_{DD} - V_{thn}\), \(M_N\) operates in the triode region and the discharging process of \(C_L\) is described by the following differential equation:

\[
-C_L \frac{dv_{CL}}{dt} = \frac{\mu_{0n} C_{oxn} \left(\frac{W}{L}\right)_n}{1 + \theta_n(V_{DD} - V_{thn})} \left[(V_{DD} - V_{thn}) v_{CL} - \frac{1}{2} v_{CL}^2\right]
\]

(31)

The solution of Eq. (31) is

\[
\ln \left[\frac{v_{CL}(t)}{2(V_{DD} - V_{thn}) - v_{CL}(t)}\right] = \frac{-\mu_{0n} C_{oxn} \left(\frac{W}{L}\right)_n (V_{DD} - V_{thn}) t}{[1 + \theta_n(V_{DD} - V_{thn})]C_L}
\]

(32)

The integration was performed taking \(t = 0\) as the instant of time corresponding to the entrance of the device in the triode region. Accordingly, the initial value of \(v_{CL}\) was taken equal to \(V_{DD} - V_{thn}\). The time interval from the instant at which \(M_N\) enters the triode region to that at which \(v_{CL}\) equals \(V_{DD}/2\), \(t_{triode}\) is thus

\[
t_{triode} = \frac{[1 + \theta_n (V_{DD} - V_{thn})]C_L}{\mu_{0n} C_{oxn} \left(\frac{W}{L}\right)_n (V_{DD} - V_{thn})} \ln \left[\frac{2(V_{DD} - V_{thn}) - 0.5 V_{DD}}{0.5 V_{DD}}\right]
\]

(33)

\(t_{50}\) is the sum of \(t_{sat}\) and \(t_{triode}\). So, \(t_{50}\) is given by

\[
t_{50} = \frac{C_L}{W_n C_{oxn} v_{satn}(V_{DD} - V_{thn})} \ln \left[\frac{1 + \lambda_n V_{DD}}{1 + \lambda_n (V_{DD} - V_{thn})}\right] + \frac{\mu_{0n} C_{oxn} \left(\frac{W}{L}\right)_n (V_{DD} - V_{thn}) C_L}{[1 + \theta_n(V_{DD} - V_{thn})]C_L} \ln \left[\frac{2(V_{DD} - V_{thn}) - 0.5 V_{DD}}{0.5 V_{DD}}\right]
\]

(34)

In case \(V_{DD}\) is smaller than \(2 V_{thn}\), \(V_{DD} - V_{thn}\) will be smaller than \(V_{DD}/2\) and \(M_N\) operates in the saturation region for the time interval extended from \(t = 0\) to \(t = t_{50}\). In this case, \(t_{50}\) is evaluated from Eq. (29) to be

\[
t_{50} = \frac{C_L}{W_n C_{oxn} v_{satn}(V_{DD} - V_{thn})} \ln \left[\frac{1 + \lambda_n V_{DD}}{1 + 0.5 \lambda_n V_{DD}}\right]
\]

(35)

\(t_{90}\) and \(t_{10}\) can be obtained with the aid of Eqs. (29) and (32) corresponding to \(v_{CL} = 0.9 V_{DD}\) (provided that \(V_{thn} > 0.1 V_{DD}\) and \(0.1 V_{DD}\), respectively, as
On equality where

\[ t_{90\%} = \frac{C_L}{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})\lambda_n} \ln \left[ \frac{1 + \lambda_n V_{DD}}{1 + 0.9\lambda_n V_{DD}} \right] \] (36)

and

\[ t_{10\%} = t_{sat} + \frac{[1 + \theta_n(V_{DD} - V_{thn})]C_L}{\mu_{on}C_{oxn}(\frac{W}{L})_n(V_{DD} - V_{thn})} \ln \left[ \frac{2(V_{DD} - V_{thn}) - 0.1V_{DD}}{0.1V_{DD}} \right] \] (37)

So, \( t_f \) is given by

\[
t_f = t_{sat} + \frac{[1 + \theta_n(V_{DD} - V_{thn})]C_L}{\mu_{on}C_{oxn}(\frac{W}{L})_n(V_{DD} - V_{thn})} \ln \left[ \frac{2(V_{DD} - V_{thn}) - 0.1V_{DD}}{0.1V_{DD}} \right] - \frac{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})\lambda_n}{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})\lambda_n} \ln \left[ \frac{1 + \lambda_n V_{DD}}{1 + 0.9\lambda_n V_{DD}} \right]
\] (38)

On the other hand, the voltage across \( C_L \) in the circuit of Figure 16 (b) is given by

\[ v_{CL}(t) = V_{DD}e^{\frac{t}{RC_L}} \] (39)

So, the corresponding three time instants, \( t_{50\%}, t_{90\%}, \) and \( t_{10\%} \) are given by

\[ t_m = RC_L \ln \left( \frac{1}{m} \right) \] (40)

where \( m \) is equal to 0.5, 0.9, and 0.1, respectively, for these time instants. If the 50% delay-equality criterion is applied, then the equivalent resistance, \( R \), is given by

\[
R = \ln \left[ \frac{1 + \lambda_n V_{DD}}{1 + \lambda_n (V_{DD} - V_{thn})} \right] + \left[ 1 + \theta_n(V_{DD} - V_{thn}) \right] \ln \left[ \frac{2(V_{DD} - V_{thn}) - 0.5V_{DD}}{0.5V_{DD}} \right] \] (41)

If the fall-time equality criterion is applied, then \( R \) is given by

\[
R = \frac{t_{sat}}{C_L} + \frac{[1 + \theta_n(V_{DD} - V_{thn})]C_L}{\mu_{on}C_{oxn}(\frac{W}{L})_n(V_{DD} - V_{thn})} \ln \left[ \frac{2(V_{DD} - V_{thn}) - 0.1V_{DD}}{0.1V_{DD}} \right] - \frac{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})\lambda_n}{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})\lambda_n} \ln \left[ \frac{1 + \lambda_n V_{DD}}{1 + 0.9\lambda_n V_{DD}} \right]
\] (42)

**Figure 17.** The relationships between the equivalent resistance of a single NMOS device and its (a) aspect ratio and (b) threshold voltage.
Refer to Figures 17 (a) and (b) for the plots of the relationships between the equivalent resistance of the single NMOS device evaluated according to the 50%-delay equivalence and the aspect ratio and the threshold voltage, respectively.

2. The second case

Now, we consider the case of the discharging of $C_L$ through serially or parallel connected NMOS devices. This is the case in wide fan-in CMOS NAND or NOR gates. In case of parallel connection of NMOS devices, the preceding analysis applies with replacing the channel width or the aspect ratio by the same parameter multiplied by $n$ where $n$ is the number of parallel NMOS devices. On the other hand, two scenarios are considered for the case of series connection; two and larger than two serially connected NMOS devices. For simplicity, the effects of the internal capacitances and the body effect are neglected here. Refer to Figure 18 (a) for illustration of the case of discharging through two serially connected NMOS devices. There are three time intervals for the discharge of $C_L$; both $M_1$ and $M_2$ are in saturation, $M_1$ is in triode and $M_2$ is in saturation, and both $M_1$ and $M_2$ are in triode; note that since the drain voltage of $M_2$ is at a higher voltage than that of $M_1$, $M_1$ enters the triode region before $M_2$ does. During the first time interval, the discharging process can be described by

$$
-c_L \frac{dv_{CL}}{dt} = W_{n1} C_{oxn} v_{satn} (V_{DD} - V_{thn}) \left(1 + \lambda_n v_{DS1}\right)
= W_{n2} C_{oxn} v_{satn} (V_{DD} - V_{thn} - v_{DS1}) \left(1 + \lambda_n v_{DS2}\right)
$$

(43)

where $v_{DS1}$ and $W_{n1}$ are the drain-to-source voltage and the channel width of $M_1$; $v_{DS2}$ and $W_{n2}$ are their counterparts for $M_2$. Since the sum of $v_{DS1}$ and $v_{DS2}$ equals $v_{CL}$, we can get $v_{DS2}$ in terms of $v_{CL}$ as

\[ v_{DS2} = v_{CL} - \left(1 + \lambda_n v_{DS1}\right) \]

**Figure 18.** Discharging of $C_L$ through (a) two transistors, (b) more than two transistors, and (c) equivalent circuit of (b) when all the devices except $M_n$ operate in the triode region.
\[ v_{DS2} = \frac{(V_{DD} - V_{thn})[W_{n1}(1 + \lambda_n v_{CL}) - W_{n2}]}{W_{n2}[\lambda_n(V_{DD} - V_{thn}) - 1] + \lambda_n W_{n1}(V_{DD} - V_{thn})} \]  

(44)

After substituting into Eq. (43), we get

\[ -\lambda_n(1 - b_1)W_{n1}C_{oxx}v_{satn}(V_{DD} - V_{thn})t = \ln \left[ \frac{(1 - a_1\lambda_n) + \lambda_n(1 - b_1)v_{CL}(t)}{(1 - a_1\lambda_n) + \lambda_n(1 - b_1)V_{DD}} \right] \]

(45)

where \( a_1 \) and \( b_1 \) are given by

\[ a_1 = \frac{(V_{DD} - V_{thn})(W_{n1} - W_{n2})}{W_{n2}[\lambda_n(V_{DD} - V_{thn}) - 1] + \lambda_n W_{n1}(V_{DD} - V_{thn})} \]

(46)

and

\[ b_1 = \frac{\lambda_n(V_{DD} - V_{thn})W_{n1}}{W_{n2}[\lambda_n(V_{DD} - V_{thn}) - 1] + \lambda_n W_{n1}(V_{DD} - V_{thn})} \]

(47)

respectively. \( M_1 \) leaves the saturation region at \( t = t_1 \) when \( v_{DS1} \) equals \( V_{DD} - V_{thn} \). This instant of time corresponds to \( v_{CL} = (V_{DD} - V_{thn} + a_1)/(1 - b_1) \). So,

\[ t_1 = \frac{C_L}{\lambda_n(1 - b_1)W_{n1}C_{oxx}v_{satn}(V_{DD} - V_{thn})} \ln \left[ \frac{(1 - \lambda_n a_1) + \lambda_n(1 - b_1)V_{DD}}{(1 - \lambda_n a_1) + \lambda_n(V_{DD} - V_{thn} + a_1)} \right] \]

(48)

The second time interval can be treated in a similar manner. In the second time interval, the discharging process can be described by the following equation:

\[ -C_L \frac{dv_{CL}}{dt} = \frac{\mu_{on}C_{oxx}(\frac{W}{L})_1}{[1 + \theta_n(V_{DD} - V_{thn})]} [(V_{DD} - V_{thn})v_{DS1}] \]

\[ = W_{n2}C_{oxx}v_{satn}(V_{DD} - V_{DS1} - V_{thn})[1 + \lambda_n v_{DS2}] \]

(49)

where the term \( 0.5v_{DS1}^2 \) was neglected. \( (W/L)_1 \) is the aspect ratio of \( M_1 \). After simple mathematical manipulations and neglecting the term \( v_{DS1}v_{DS2} \) and using the fact that the sum of \( v_{DS1} \) and \( v_{DS2} \) is equal to \( v_{CL} \), we get

\[ v_{DS1} = (v_{CL1} + 1/\lambda_n)a_2 \]

(50)

where \( a_2 \) is given by

\[ a_2 = \frac{[1 + \theta_n(V_{DD} - V_{thn})]\lambda_n W_{n2}C_{oxx}v_{satn}(V_{DD} - V_{thn})}{[1 + \theta_n(V_{DD} - V_{thn})]\lambda_n W_{n2}C_{oxx}v_{satn}(V_{DD} - V_{thn}) + \mu_{on}C_{oxx}(\frac{W}{L})_n(V_{DD} - V_{thn})} + [1 + \theta_n(V_{DD} - V_{thn})]W_{n2}C_{oxx}v_{satn} \]

(51)

\( v_{DS1} \) can be substituted in terms of \( v_{CL} \) from Eq. (50) into Eq. (49) with the result that

\[ -C_L \frac{dv_{CL}}{dt} = \frac{\mu_{on}C_{oxx}(\frac{W}{L})_1}{[1 + \theta_n(V_{DD} - V_{thn})]} [(V_{DD} - V_{thn})(v_{CL} + 1/\lambda_n)a_2] \]

(52)

Let \( a_3 \) and \( b_3 \) be given by

\[ a_3 = \frac{\mu_{on}C_{oxx}(\frac{W}{L})_1(V_{DD} - V_{thn})a_2}{\lambda_n[1 + \theta_n(V_{DD} - V_{thn})]} \]

(53)
and

\[ b_3 = a_3 \lambda_n \]  \hspace{1cm} (54)

respectively. So, Eq. (52) can be written as

\[-C_L \frac{dv_{CL}}{dt} = a_3 + b_3 \ v_{CL} \]  \hspace{1cm} (55)

Taking into account that the second time interval begins when \( v_{CL} \) equals \( (V_{DD} - V_{thn} + a_i)/(1 - b_i) \) and ends (at \( t = t_2 \)) when \( v_{CL} \) equals \( V_{DD} - V_{thn} \), we get the solution of Eq. (55) as

\[ t = \frac{C_L}{b_3} \ln \left[ \frac{a_3 + b_3 \left( \frac{V_{DD} - V_{thn} + a_i}{1 - b_i} \right)}{a_3 + b_3 v_{CL}(t)} \right] \]  \hspace{1cm} (56)

\[ t = t_2 \] when \( v_{CL} \) equals \( V_{DD} - V_{thn} \). So,

\[ t_2 = \frac{C_L}{b_3} \ln \left[ \frac{a_3 + b_3 \left( \frac{V_{DD} - V_{thn} + a_i}{1 - b_i} \right)}{a_3 + b_3 (V_{DD} - V_{thn})} \right] \]  \hspace{1cm} (57)

For the third time interval, the discharging process can be described by

\[-C_L \frac{dv_{CL}}{dt} = \mu_{on} C_{oxn} \left( \frac{W}{L} \right)_1 (V_{DD} - V_{thn}) v_{DS1} = \mu_{on} C_{oxn} \left( \frac{W}{L} \right)_2 (V_{DD} - V_{thn} - v_{DS1}) v_{DS2} \]

\[ \frac{1}{[1 + \theta_n(V_{DD} - V_{thn})]} \]  \hspace{1cm} (58)

After simple mathematical manipulations and neglecting \( v_{DS1} \) with respect to \( V_{DD} - V_{thn} \), we get

\[ v_{DS2} = \left( \frac{W}{L} \right)_1 v_{DS1} \]  \hspace{1cm} (59)

The latter approximation is justified by the fact that \( v_{DS1} \) is relatively small in this time interval. \( v_{CL} \) is consequently given by

\[ v_{CL} = \left( \frac{W}{L} \right)_1 + \left( \frac{W}{L} \right)_2 v_{DS1} \]  \hspace{1cm} (60)

After substituting \( v_{DS1} \) from Eq. (60) into Eq. (58), we get

\[-C_L \frac{dv_{CL}}{dt} = \mu_{on} C_{oxn} \left( \frac{W}{L} \right)_1 (V_{DD} - V_{thn}) \left( \frac{W}{L} \right)_2 v_{CL} \]

\[ \frac{1}{[1 + \theta_n(V_{DD} - V_{thn})]} \left[ \left( \frac{W}{L} \right)_1 + \left( \frac{W}{L} \right)_2 \right] \]  \hspace{1cm} (61)

The solution of Eq. (61) is

\[ \ln \left[ \frac{v_{CL}(t)}{V_{DD} - V_{thn}} \right] = -\mu_{on} C_{oxn}(V_{DD} - V_{thn}) \left( \frac{W}{L} \right)_1 \frac{t}{C_L[1 + \theta_n(V_{DD} - V_{thn})]} \left[ \left( \frac{W}{L} \right)_1 + \left( \frac{W}{L} \right)_2 \right] \]  \hspace{1cm} (62)

\( v_{CL} \) equals \( V_{DD}/2 \) when \( t = t_3 \) (estimated from the beginning of the third time interval). So,
\[ t_3 = \frac{C_L[1 + \theta_n(V_{DD} - V_{thn})][(W/L)_1 + (W/L)_2]}{\mu_{on}C_{oxn}(V_{DD} - V_{thn})(W/L)_1(W/L)_2} \ln \left( \frac{V_{DD} - V_{thn}}{0.5V_{DD}} \right) \]  

(63)

t_{50\%} is the sum of \( t_1, t_2, \) and \( t_3. t_{90\%} \) and \( t_{10\%} \) can be evaluated with the aid of Eqs. (45) and (62) corresponding to \( v_{CL} = 0.9V_{DD} \) and \( 0.1V_{DD} \), respectively. So,

\[ t_{90\%} = \frac{C_L}{\lambda_n(1 - b_1)W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})} \ln \left( \frac{(1 - \lambda_n a_1) + \lambda_n(1 - b_1)V_{DD}}{(1 - \lambda_n a_1) + 0.9\lambda_n(1 - b_1)V_{DD}} \right) \]  

(64)

and

\[ t_{10\%} = t_1 + t_2 + \frac{C_L[1 + \theta_n(V_{DD} - V_{thn})][(W/L)_1 + (W/L)_2]}{\mu_{on}C_{oxn}(V_{DD} - V_{thn})(W/L)_1(W/L)_2} \ln \left( \frac{V_{DD} - V_{thn}}{0.1V_{DD}} \right) \]  

(65)

The equivalent resistance can be simply found by equating the time delay or the fall time with the corresponding equations for the equivalent RC circuit.

Now, consider the scenario of the discharging of \( C_L \) through \( n \) transistors where \( n \) is larger than two (refer to Figure 18 (b) for illustration). There are two time intervals in this case; the first one corresponds to the operation of all the devices except \( M_n \) in triode region and the second one corresponds to the operation of all the devices in triode region.

Figure 18 (c) illustrates the representation of all the devices except \( M_n \) by a resistance, \( R_{triode} \). In order to find an expression for \( R_{triode} \), let the triode-region operated devices be represented by a single equivalent device with an aspect ratio of \((W/L)/n/(n-1)\); the \( i-v \) relationship of the equivalent device is given by

\[ i_D = \frac{\mu_{on}C_{oxn}(W/L)_n(1/n-1)(v_{GS} - V_{thn})v_{DS}}{[1 + \theta_n(v_{GS} - V_{thn})]} \]  

(66)

where the term, \( 0.5v_{DS}^2 \), was neglected. Now, the equivalent resistance of the device, \( R_{triode} \), is simply taken as the ratio between \( v_{DS} \) and \( i_D \) in Eq. (66) with \( v_{GS} \) substituted by an average value, \( v_{GSavg} \). In order to find \( v_{GSavg} \), let the average value of \( v_{CL} \), \( V_{DD}/2 \), be equally divided between the \((n-1)\) devices. This results in

\[ v_{GSavg} = \frac{V_{DD}(3n + 2)}{4n} \]  

(67)

Now, the discharging of \( C_L \) can be described by

\[ -C_L \frac{dv_{CL}}{dt} = W_nC_{oxn}v_{satn}(V_{DD} - V_{thn} - i_{sat}) \]  

(68)

in which the term, \( \lambda_n v_{DS} \), is neglected here. So,

\[ v_{CL}(t) = V_{DD} - \frac{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})t}{(1 + W_nC_{oxn}v_{satn}R_{sat})C_L} \]  

(69)

\( M_n \) leaves saturation at \( t = t_{sat} \) which can be shown to be given by

\[ t_{sat} = \frac{V_{thn}C_L(1 + W_nC_{oxn}v_{satn}R_{sat})}{W_nC_{oxn}v_{satn}(V_{DD} - V_{thn})} \]  

(70)
In the same manner, when $M_n$ leaves saturation, all the $n$ devices can be represented by a resistance

$$R_{\text{triode}} = \frac{n}{\mu_0 n C_{\text{oxn}}} \left[ 1 + \theta_n (v_{\text{GSavg}} - V_{\text{thn}}) \right]$$

(71)

with $v_{\text{GSavg}} = \frac{3n + 1}{4} V_{DD}/n$. So, $t_{50\%}$ in this case is given by $t_{50\%} = t_{\text{sat}} + t_{\text{triode}}$ where $t_{\text{triode}}$ (corresponding to $v_{CL} = V_{DD}/2$) is given by

$$t_{\text{triode}} = R_{\text{triode}} C_{L} \ln \left( \frac{V_{DD} - V_{\text{thn}}}{0.5 V_{DD}} \right)$$

(72)

t_{90\%} can be shown to be given by (from Eq. (69))

$$t_{90\%} = \frac{0.1 C_{L} (1 + W_n C_{\text{oxn}} v_{\text{satn}} R_{\text{sat}})}{W_n C_{\text{oxn}} v_{\text{satn}}}$$

(73)

t_{10\%} can be found in a similar way in the second time interval as

$$t_{10\%} = t_{\text{sat}} + R_{\text{triode}} C_{L} \ln \left( \frac{V_{DD} - V_{\text{thn}}}{0.1 V_{DD}} \right)$$

(74)

The equivalent resistance can thus be found in a manner similar to the previous case. Figures 19 (a), (b), and (c) portray the relationships between the equivalent resistance of a stack of NMOS devices and their aspect ratios, their threshold voltages, and the number of the transistors, respectively. $n$ is assumed to be equal to 8 unless otherwise specified.

![Figure 19](image-url)

**Figure 19.** The relationships between the equivalent resistance of a stack of NMOS devices and (a) their aspect ratios, (b) their threshold voltages, and (c) the number of transistors in the stack.
3. The third case

The third case to be considered is that when both the pull-up network (PUN) and the PDN are active. This is the case in the pseudo-NMOS logic-circuit family. Refer to Figure 20 (a) for the inverter in this family. When \( v_{in} \) is equal to 0 V, \( M_N \) is deactivated and the load capacitance, \( C_L \), charges to \( V_{DD} \) which is the output-high voltage, \( V_{OH} \). If \( v_{in} \) is equal to \( V_{DD} \), \( M_N \) is activated; however, the output-low voltage, \( V_{OL} \), is not equal to 0 V in this case due to the contention current of the always-activated PMOS transistor, \( M_P \). In this case, the equivalent circuit is as shown in Figure 20 (b) where \( R_N \) and \( R_P \) are the equivalent resistances of \( M_N \) and \( M_P \), respectively. It is now required to find the expressions of \( R_N \) and \( R_P \). Towards that end, the two circuits of Figures 20 (a) and (b) are analysed with the expressions of the high-to-low propagation delay, \( t_{PHL} \), and the fall time, \( t_f \), equalized for the two circuits.

Figure 21 shows the definitions of the 90%, 50%, and 10% points for this case. Evaluating the \( t_{10\%} \) point is based on the assumption that the NMOS device has a sufficient strength to pull down the output voltage, \( v_{out} \), to 0.1\( V_{DD} \) or less. The circuit of Figure 20 (b) can be described by the following equation:

![Figure 20](image)

**Figure 20.** (a) The pseudo-NMOS inverter and (b) the equivalent circuit of (a) when \( v_{in} \) is equal to \( V_{DD} \).

![Figure 21](image)

**Figure 21.** A qualitative plot for indicating the definition of the 90%, 50%, and 10% points [15].
\[ -C_L \frac{dv_{CL}}{dt} + \frac{(V_{DD} - v_{CL})}{R_P} = \frac{v_{CL}}{R_N} \]  

(75)

\( v_{CL}(0) \) is equal to \( V_{DD} \) for the initially charged capacitance. The solution of Eq. (75) is

\[
\ln \left[ \frac{-V_{DD}R_N + v_{CL}(t)(R_N + R_P)}{-V_{DD}R_N + V_{DD}(R_N + R_P)} \right] = -\frac{t}{C_L} \left( \frac{1}{R_N} + \frac{1}{R_P} \right) \]

(76)

t_{50\%}, t_{90\%}, and \( t_{10\%} \) can be derived with the aid of Eq. (76) by substituting the corresponding values of \( v_{CL} \). So,

\[
t_{50\%} = \frac{R_N R_P C_L}{(R_N + R_P)} \ln(2) \]

(77)

\[
t_{90\%} = \frac{R_N R_P C_L}{(R_N + R_P)} \ln\left(\frac{1}{0.9}\right) \]

(78)

and

\[
t_{10\%} = \frac{R_N R_P C_L}{(R_N + R_P)} \ln(10) \]

(79)

where \( V_{OL} \) was substituted by \( V_{DD}R_N/(R_N + R_P) \). The fall time, \( t_f \), is thus

\[
t_f = t_{10\%} - t_{90\%} = \frac{R_N R_P C_L}{(R_N + R_P)} \ln(9) \]

(80)

Now, refer to Figure 20 (a). Due to the change of the mode of operation of \( M_N \) and \( M_P \) between saturation and triode, the discharging process of \( C_L \) can be divided into three time intervals as shown in Figure 22 and Table 2. The discharging process of \( C_L \) can be described in region I by the following differential equation:

\[
-C_L \frac{dv_{CL}}{dt} + \mu_{0p} C_{oxp} \left( \frac{W}{L} \right)_p (V_{DD} - |V_{thp}|)(V_{DD} - v_{CL}) = W_n C_{oxn} v_{satn} (V_{DD} - V_{thn})(1 + \lambda_n v_{CL}) \]

(81)

where the term, \( 0.5(V_{DD} - v_{CL})^2 \), was neglected in the term of the current of \( M_P \). This negligence was justified by the fact that during region I, the voltage across \( C_L \) has a relatively large value and thus the voltage across \( M_P \) has a relatively small value. The solution of Eq. (81) is

\[
\ln \left[ \frac{a + bv_{CL}(t)}{a + bV_{DD}} \right] = \frac{bt}{C_L} \]

(82)

where \( a \) and \( b \) are given as

\[
a = \frac{\mu_{0p} C_{oxp} \left( \frac{W}{L} \right)_p (V_{DD} - |V_{thp}|) V_{DD}}{[1 + \theta_p (V_{DD} - |V_{thp}|)]} - W_n C_{oxn} v_{satn} (V_{DD} - V_{thn}) \]

(83)

and
respectively. $t_{90\%}$ can be found from Eq. (82) as

$$t_{90\%} = \frac{C_L}{b} \ln \left[ \frac{a + b(V_{OL} + 0.9(V_{DD} - V_{OL}))}{a + bV_{DD}} \right]$$

(85)

The time instant, $t_1$, at which $M_N$ leaves the saturation region and enters the triode region can be found by substituting $v_{CL}$ by $V_{DD} - V_{thn}$ into Eq. (82)

$$t_1 = \frac{C_L}{b} \ln \left[ \frac{a + b(V_{DD} - V_{thn})}{a + bV_{DD}} \right]$$

(86)

In order to simplify the analysis in region II, the average currents of $M_N$ and $M_P$, $i_{DNavg}$ and $i_{DPavg}$, are adopted. Each of these two currents is the average of the two currents at the onset and end of region II. So, region II can be described by the following differential equation:

$$-C_L \frac{dv_{CL}}{dt} + i_{DPavg} = i_{DNavg}$$

(87)
The solution of Eq. (87) is

\[ v_{CL}(t) = (V_{DD} - V_{thn}) - \left( \frac{i_{DNavg} - i_{DPavg}}{C_L} \right) t \]  

(88)

According to Eq. (88), \( t = 0 \) is the instant of time at which \( M_N \) enters the triode region. So, \( t_{50\%} \) is the sum of two times as follows:

\[ t_{50\%} = t_1 + t_{21} \]  

(89)

where \( t_{21} \) is the time at which \( v_{CL} \) reaches the level corresponding to the 50\% point; \( V_{OL} + 0.5(V_{DD} - V_{OL}) \). So,

\[ t_{21} = \frac{C_L(0.5V_{DD} - V_{thn} - 0.5V_{OL})}{(i_{DNavg} - i_{DPavg})} \]  

(90)

\( M_N \) leaves region II at time \( t = t_2 \) which is given by

\[ t_2 = \frac{C_L(V_{DD} - V_{thn} - |V_{thp}|)}{(i_{DNavg} - i_{DPavg})} \]  

(91)

The third region, III, can be described by the following differential equation:

\[ -C_L \frac{dv_{CL}}{dt} + W_P C_{oxp} v_{satp} (V_{DD} - |V_{thp}|) [1 + |\lambda_p|(V_{DD} - v_{CL})] = \frac{\mu_0 n C_{oxn} \left( \frac{W}{L} \right) n (V_{DD} - V_{thn}) v_{CL}}{[1 + \theta_n(V_{DD} - V_{thn})]} \]  

(92)

The term, \( 0.5v_{CL}^2 \), was neglected in Eq. (92). This negligence was justified by the fact that during region III, the voltage across \( C_L \) has a relatively small value. The solution of Eq. (92) is

\[ \ln \left[ c - d v_{CL}(t) \right] = -\frac{dt}{C_L} \]  

(93)

where \( c \) and \( d \) are given by

\[ c = W_P C_{oxp} v_{satp} (V_{DD} - |V_{thp}|) [1 + |\lambda_p|V_{DD}] \]  

(94)

and

\[ d = W_P C_{oxp} v_{satp} (V_{DD} - |V_{thp}|)|\lambda_p| + \frac{\mu_0 n C_{oxn} \left( \frac{W}{L} \right) n (V_{DD} - V_{thn})}{[1 + \theta_n(V_{D} - V_{thn})]} \]  

(95)

respectively. \( t_{10\%} \) is the sum of three times, \( t_1, t_2, \) and the time at which \( v_{CL} \) reaches \( V_{OL} + 0.1(V_{DD} - V_{OL}) \) in region III. So,

\[ t_{10\%} = t_1 + t_2 + \frac{C_L}{d} \ln \left[ \frac{c - d|V_{thp}|}{c - d[V_{OL} + 0.1(V_{DD} - V_{OL})]} \right] \]  

(96)

Now, in order to evaluate \( R_N \) and \( R_P \), we will adopt the assumption that the NMOS device has a much larger strength compared to the PMOS device; that is, \( R_N \) is much smaller than \( R_P \). Adopting this assumption and neglecting \( R_N \) with respect to \( R_P \) in Eq. (77) results in
where $t_{50\%}$ is given by Eq. (89). Now, from Eq. (80), we get the expression of $R_P$ as

$$R_P = \frac{t_f R_N}{C_L R_N \ln(9) - t_f} \tag{98}$$

where $t_f$ is given by the difference between the two times of Eqs. (96) and (85). Now, refer to Figures 23 (a) and (b) for the plots of the relationships between the equivalent resistance and the aspect ratio and the threshold voltage of the NMOS device, respectively. In these results, the following parameters of the PMOS transistor which were extracted using the approach presented in the previous section are adopted: $V_{thp} = -0.34$ V, $k_p' = 280$ μA/V², $\lambda_p = -0.45$ V⁻¹, and $C_{exp\ satp} = 650$ A/Vm. The aspect ratio of the PMOS device was assumed to be two.

4. The fourth case

The fourth and final case to be considered in this paper is that of the charge sharing between two capacitors through a MOS transistor. This case can be found in single-transistor single-capacitor dynamic-random access memories in which the charge is shared between a cell-storage capacitor and a bitline-parasitic capacitance [50], in domino logic in which the charge is shared between the dynamic-node capacitance and one of the internal parasitic capacitances in the PDN [15], or in circuits that depend on charge steering in their operation [51]. The latter circuits can be found in latches, demultiplexers, clock-and-data recovery circuits, and analog-to-digital converters.

For illustration, refer to Figure 24 (a) for two capacitors, $C_1$ and $C_2$, sharing their charge through the access device, $M_{N1}$. Figure 24 (b) represents the equivalent circuit of Figure 24 (a) in which the equivalent resistance of $M_{N1}$, let it be $R$, is shown. It is now required to find the expression of $R$. Towards that end, the following assumptions are made:

1. $C_1$ and $C_2$ may be different;
2. the initial voltage of $C_1$ is larger than that of $C_2$; that is, $v_{C1}(0) > v_{C2}(0)$;
3. neither $C_1$ nor $C_2$ is initially discharged;
4. the initial voltage of $C_1$ is larger than $V_{DD} - V_{thn}$; and

![Figure 23](image-url). The relationships between the equivalent resistance of the NMOS device and its (a) aspect ratio and (b) threshold voltage.
5. the steady-state voltage at the end of the charge sharing between $C_1$ and $C_2$ is smaller than $V_{DD} - V_{thn}$.

In spite of the previous assumptions, the analysis performed is general and the 50\% criterion is adopted in deriving the expression of the time required for charge sharing and evaluating $R$. The 50\% point is defined here as the time required for the voltage across $C_1$ to reach the average voltage of the initial and final voltages across $C_1$. Refer to Figure 25 for illustration. According to this figure, $t_{50\%}$ is given by

$$t_{50\%} = t_{\text{sat}} + t_{\text{triode}}$$

(99)

where $t_{\text{sat}}$ and $t_{\text{triode}}$ are the time intervals corresponding to the operation of $M_N$ in the saturation and triode regions, respectively. Using the principle of charge conservation \[15\], the final voltage of $C_1$ and $C_2$ at the end of the charge sharing is given by

$$v_{C1}(\infty) = v_{C2}(\infty) = \frac{C_1 v_{C1}(0) + C_2 v_{C2}(0)}{C_1 + C_2}$$

(100)

The charge-sharing problem can now be described as follows: Given $C_1$, $C_2$, $v_{C1}(0)$, and $v_{C2}(0)$, find the expression of $R$. At the onset of the charge sharing, $M_N$ operates in the saturation region. So, this time interval can be described by the following differential equation:

![Figure 24](image1.png)

**Figure 24.** The circuit schematic representing the charge sharing between $C_1$ and $C_2$ and (b) its equivalent circuit when representing the access device by an equivalent resistance, $R$.

![Figure 25](image2.png)

**Figure 25.** The voltage waveforms across $C_1$ and $C_2$ upon charge sharing between them.
Figure 26. The relationships between the equivalent resistance of the access device and its (a) aspect ratio and (b) threshold voltage.

\[-C_L \frac{dv_{CL}}{dt} = W_n C_{oxn} V_{satn}(V_{DD} - V_{C2}(t) - V_{thn})[1 + \lambda_n(v_{C1}(t) - V_{C2}(t))]\]  \hspace{1cm} (101)

In order to simplify the analysis, \(v_{C2}\) is substituted by its average value which is given by

\[V_{C2avg} = \frac{1}{2}[v_{C2}(0) + v_{C2}(\infty)]\]  \hspace{1cm} (102)

The solution of Eq. (101) is

\[\ln \left[ \frac{1 - \lambda_n V_{C2avg} + \lambda_n v_{C1}(t)}{1 - \lambda_n V_{C2avg} + \lambda_n v_{C1}(0)} \right] = -\frac{\lambda_n W_n C_{oxn} V_{satn} (V_{DD} - V_{thn} - V_{C2avg})}{C_1} t\]  \hspace{1cm} (103)

So, \(t_{sat}\) is given by

\[t_{sat} = \frac{C_1}{\lambda_n W_n C_{oxn} V_{satn} (V_{DD} - V_{thn} - V_{C2avg})} \ln \left[ \frac{1 - \lambda_n V_{C2avg} + \lambda_n v_{C1}(0)}{1 - \lambda_n V_{C2avg} + \lambda_n (V_{DD} - V_{thn})} \right]\]  \hspace{1cm} (104)

Now, the triode-region operation of \(M_N\) can be described by the following equation:

\[-C_L \frac{dv_{CL}}{dt} = \mu_{0n} C_{oxn} (\frac{W}{L})_n (V_{DD} - V_{thn} - V_{C2avg}) (v_{C1} - V_{C2avg})\]  \hspace{1cm} (105)

in which \(v_{C2}\) was substituted by its average value also and the term 0.5\(v_{DS}^2\) was neglected as it has a very limited value in the triode region. The solution of Eq. (105) is

\[\ln \left[ \frac{v_{C1}(t) - V_{C2avg}}{V_{DD} - V_{thn} - V_{C2avg}} \right] = -\frac{t}{\mu_{0n} C_{oxn} (\frac{W}{L})_n (V_{DD} - V_{thn} - V_{C2avg})} \ln \left[ \frac{V_{DD} - V_{thn} - V_{C2avg}}{v_{C1}(0) + v_{C1}(\infty) - V_{C2avg}} \right]\]  \hspace{1cm} (106)

So, \(t_{triode}\) is given by

\[t_{triode} = \frac{C_1 [1 + \theta_n(V_{DD} - V_{thn} - V_{C2avg})]}{\mu_{0n} C_{oxn} (\frac{W}{L})_n (V_{DD} - V_{thn} - V_{C2avg})} \ln \left[ \frac{V_{DD} - V_{thn} - V_{C2avg}}{v_{C1}(0) + v_{C1}(\infty) - V_{C2avg}} \right]\]  \hspace{1cm} (107)

Note that the previous estimation was based on the assumption that the average value of \(v_{C1} V_{C1avg}\) is smaller than \(V_{DD} - V_{thn}\). If this is not the case, then (with the aid of Eq. (104)), \(t_{50%}\) will be given by
Now, to find the relationship between $t_{50\%}$ and $R$, refer to Figure 24 (b). This circuit can be described by the following equation:

$$
-C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = \frac{v_{C1} - v_{C2}}{R}
$$

The solution of Eq. (109) is

$$
v_{C1}(t) = A_1 + A_2 e^{-\frac{(C_1+C_2)t}{RC_1C_2}}
$$

where $A_1$ and $A_2$ are given by

$$
A_1 = \frac{C_1 v_{C1}(0) + C_2 v_{C2}(0)}{C_1 + C_2}
$$

$$
A_2 = \frac{C_2 (v_{C1}(0) - v_{C2}(0))}{C_1 + C_2}
$$

respectively. So, $t_{50\%}$ is given by

$$
t_{50\%} = \frac{RC_1 C_2}{C_1 + C_2} \ln \left( \frac{A_2}{V_{C1avg} - A_1} \right)
$$

$R$ can be found by equating Eqs. (108) and (113). Now, refer to Figures 26 (a) and (b) for the plots of the relationships between the equivalent resistance of the access device and its aspect ratio and its threshold voltage, respectively.

**IV. Simulation results**

In this section, the analysis performed in the paper is verified and the estimated 50% time delay, from which the equivalent resistance is evaluated, will be compared with the simulation results and also with other time delays estimated by other previously proposed equivalent MOSFET resistances. The parameters of [49] are adopted for the 45 nm
CMOS Berkeley predictive-technology model (BPTM) in the simulation. The parameters extracted from this model will be adopted in plotting the derived equations with all the devices assumed to be minimum-sized except the PMOS device which has an aspect ratio of two. When citing [41] in the comparison, Eq. (23) is adopted. The load capacitance will be assumed to be equal to 10 fF.

Figures 27 (a) and (b) exhibit the estimated 50% time delay for the first case of a single NMOS device discharging an initially charged load capacitance. The estimated time delay according to the equivalent resistance of [42] does not depend on \( V_{thn} \) and is equal to 0.086 ns. It is apparent that the performed analysis not only gives the most accurate results compared to simulation but also the best agreement with the trend of the decrease or the increase of the time delay with \( W/L \) and \( V_{thn} \), respectively. Figures 28 (a) and (b) are the counterparts of Figures 27 (a) and (b) for the case of the NMOS stack with \( n = 8 \). Although the difference between the proposed model and the simulation results is perceptible, the adopted model gives the more accurate results compared to the other three models.

Figures 29 (a) and (b) give the results for the case of contention between an NMOS device and a PMOS one when discharging an initially charged capacitance. Finally, Figures 30 (a) and (b) give the results of the case of charge sharing between two capacitors with capacitances that are assumed to be 50 fF and 100 fF and are initially charged to 1
and \(0.35\) V, respectively. The equivalent resistance of [42] gives the more accurate results in this case with respect to the change of the aspect ratio of the NMOS device as shown in Figure 30 (a). However, the results of this work are not that bad.

V. Conclusions

In this paper, a fully analytical parameter-extraction approach was proposed and applied on the MOSFET devices. The proposed parameter-extraction procedure is simple, easy, fully analytical, and general in the sense that it can be applied on the experimental results equally well as on simulation results. Also, it can be applied on conventional silicon and GaAs devices.

The equivalence of the MOS transistor with a resistance was discussed with the expression of the equivalent resistance derived for four cases. The four cases considered were that of a single NMOS device discharging a capacitance, a stack of NMOS transistors discharging a capacitance, a capacitance discharging through an NMOS transistor with a contention current from a PMOS device, and a charge sharing between two capacitors through an NMOS device. The two criteria considered were the equivalence of the propagation delay and the fall time between the transistor-like circuit and their counterparts in the resistance-like circuit. The MOS model adopted in this paper was rather simple; yet, took some of the short-channel effects into consideration. Compared to other existent resistance models, the proposed analysis exhibited a very good agreement with simulation results.

Disclosure statement

No potential conflict of interest was reported by the authors.

References

[1] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd ed., Oxford University Press, New York, 2011.
[2] Q. Min, E.-P. Li, and J.-M. Jin, *Modeling and analysis for MOS capacitance of TSV considering temperature dependence*, Joint International Symposium on Electromagnetic
Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC), Sapporo, Japan, 3–7 Jun. 2019.

[3] M. Walit, Characterization and modeling of single charge trapping in MOS transistors, IEEE International Integrated Reliability Workshop (IIRW), South Lake Tahoe, CA, USA, 13–17 Oct. 2019.

[4] S. Tantry, B.H. Sagar, and K.S. Vinay, An unified EKV MOSFET model to achieve better performance of practical MOS circuits using Verilog-A, Global Conference for Advancement in Technology (GCAT), Bangaluru, India, 18–20 Oct. 2019.

[5] W. Grabinski, M. Pavanello, M. de Souza, D. Tomaszewski, J. Maleinska, G. Głużko, M. Bucher, N. Makris, A. Nikolau, A.A. Elhadid, M. Mierzwinski, L. Lemaitre, M. Brinson, C. Lallement, J.-M. Sallesse, S. Yoshitomi, P. Malisse, H. Oguey, S. Cserveny, C. Enz, F. Krummenacher, and E. Vittoz, FOSS EKV2.6 Verilog-A compact MOSFET model, 49th European Solid-State Device Research Conference (ESSDERC), Cracow, Poland, 23–26 Sep. 2019.

[6] V. Kumar, C.K. Dabhi, S.S. Parihar, and Y.S. Chauhan, Analysis and compact modeling of drain-extended FinFET, IEEE Conference on Modeling of Systems Circuits and Devices (MOS-AK India), Hyderabad, India, 25–27 Feb. 2019.

[7] R. Sasić, R. Ramović, and V. Herrmann, A new approximate model for short-channel MOS devices, Phys. Status Solidi (A). 165, 2, (Feb. 1998), pp. 445–454. doi:10.1002/(SICI)1521-396X(199802)165:2<445::AID-PSSA445>3.0.CO;2-O

[8] L.O. Chua and -C.-C. Chang, A simple dynamic circuit model for MOS structure, Int. J. Circuit Theory Appl. 15 (1987), pp. 143–170. doi:10.1002/cta.4490150205.

[9] H. Katoh and Y. Itoh, Analytical expressions for the static MOS transistor characteristics based on the gradual channel model, Solid State Electron 17 (1974), pp. 1283–1292. doi:10.1016/0038-1101(74)90006-9.

[10] P. Rossel, H. Martinot, and G. Vassilief, Accurate two sections model for MOS transistor in saturation, Solid-Slate Electron. 19 (1976), pp. 51–56. doi:10.1016/0038-1101(76)90133-7.

[11] T. Poorter and J.H. Satter, A D.C. model for an MOS-transistor in the saturation region, Solid-Slate Electron. 23 (1980), pp. 765–772. doi:10.1016/0038-1101(80)90135-5.

[12] Y. Roh and L. Trombetta, A comprehensive model for the formation of interface traps in MOS devices, Microelectron. Eng. 28, 1 – 4, (Jun 1995), pp. 23–26. doi:10.1016/0167-9317(95)00008-V

[13] Y. Cheng and C. Hu, MOSFET Modeling & BSIM3 User’s Guide, Kluwer Academic Publishers, Boston, 1999.

[14] N. Arora, MOSFET Modeling for VLSI Simulation: Theory and Practice, World Scientific, New Jersey, 2007.

[15] A.S. Sedra and K.C. Smith, Microelectronic Circuits, 7th ed., Oxford University Press, Oxford, New York, 2015.

[16] J. Yao, Dual-threshold voltage design of sub-threshold circuits, Doctor of Philosophy Thesis, Auburn University, Auburn, Alabama, 2 Aug. 2014.

[17] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and H.S.P. Wong, Device scaling limits of Si MOSFETs and their application dependencies, Proc. IEEE. 89, 3, (7 Aug. 2002), pp. 259–288. doi:10.1109/5.915374

[18] B. Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., McGraw-Hill, New York, 2017.

[19] S.M. Sharroush, Understanding the behavior of RTD-loaded NMOS inverter through compact-form analysis, Ain Shams Eng. J. 9, 4, (Dec. 2018), pp. 2453–2478. doi:10.1016/j.asej.2017.06.001

[20] V. Kursen and E.B. Friedman, Multi-Voltage CMOS Circuit Design, John Wiley & Sons Ltd., Great Britain, 2006.

[21] R. Burch, F. Najm, P. Yang, and T. Trick, A Monte Carlo approach for power estimation, IEEE Trans. Very Large Scale Integr. VLSI Syst. 1, 1, (Mar. 1993), pp. 63–71. doi:10.1109/92.219908
[22] G.T. Wright and H.M.A. Gaffur, Preprocessor Modeling of Parameter and Geometry Dependences of Short and Narrow MOSFET’s for VLSI Circuit Simulation, Optimization, and Statistics with SPICE, IEEE Trans. on Electron Devices, Vol. ED-32, No.7, (July 1985), pp. 1240 - 1245.

[23] M.F.F. Hamer and B. Sc, First-order parameter extraction on enhancement silicon MOS transistors, IEE Proc. Solid State Electron Devices 133 (2) (1986), pp. 49. doi:10.1049/ip-iet.1986.0011.

[24] W.R. Torres, Submicron CAD design and analysis of MOS current mirrors, Master Thesis, Florida Atlantic University, Boca Raton, Florida, 2004.

[25] B.J. Sheu, MOS transistor modeling and characterization for circuit simulation, Doctor of Philosophy Thesis, University of California, Berkeley, 1985.

[26] W. Maes, K.M. De Meyer, and L.H. Dupas, SIMPAR: A versatile technology independent parameter extraction program using a new optimized fit-strategy, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 5, 2, (Apr 1986), pp. 320–325. doi:10.1109/TCAD.1986.1270202

[27] D. Kasprowicz, Semiconductor device parameter extraction based on I–V measurements and simulation, 26th International Conference “Mixed Design of Integrated Circuits and Systems”, Rzeszów, Poland, Poland: IEEE, 27–29 Jun. 2019.

[28] H.P. Tuinhout, S. Swaving, and J.J.M. Joosten, A fully analytical MOSFET model parameter extraction approach, Proceedings of the IEEE International Conference on Microelectronic Test Structures, Long Beach, CA, USA, pp. 79–84, 22 – 23 Feb. 1988.

[29] Y. Park, S-CMOS: A robust deep-submicron CMOS transistor model for very low-power high-frequency VLSI applications, Doctor of Philosophy Thesis, University of Southern California, Los Angeles, California, 1999.

[30] S.M.A.M. Gowda, BSIM plus: An advanced MOS transistor model for VLSI circuits, Doctor of Philosophy Thesis, University of Southern California, Los Angeles, California, 1992.

[31] N.H.E. Weste and D.M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Addison-Wesley, Boston, 2011.

[32] C. Nguyen, Radio-Frequency Integrated-Circuit Engineering, 1st ed., Wiley, USA, 2015.

[33] J.-S. Park and A. Neugroschel, Current dependence of the emitter resistance of bipolar transistors, IEEE Trans. Electron Devices 37 (6) (1990), pp. 1540–1542. doi:10.1109/16.106254.

[34] T. Nakadai and K. Hashimoto, Measuring the base resistance of bipolar transistors, The Bipolar Circuits and Technology Meeting, Minneapolis, MN, USA: IEEE, 9–10 Sept. 1991.

[35] G. Verzellesi, A. Chantre, R. Turetta, M. Cappellin, P. Pavan, and E. Zanoni, A compact method for measuring parasitic resistances in bipolar transistors, 23rd European Solid State Device Research Conference, Grenoble, France: IEEE, 13–16 Sept. 1993.

[36] P. Pouvil, B. Zemour, D. Pasquet, and J. Gaubert, Determination of source and drain parasitic resistances of HEMTs, Electron. Lett. 28 (7) (1992), pp. 618-620. doi:10.1049/el:19920390.

[37] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M.J. Deen, P.R. Gray, and C. Hu, An effective gate resistance model for CMOS RF and noise modeling,” International Electron Devices Meeting, San Francisco, CA, USA: IEEE, 6 – 9 Dec. 1998.

[38] B. Heydari, CMOS circuits and devices beyond 100 GHz, Doctor of Philosophy Thesis, University of California, Berkeley, 2008.

[39] M. Qin, Y. Sun, X. Li, and Y. Shi, Analytical parameter extraction for small-signal equivalent circuit of 3D FinFET into sub-THz range, IEEE Access 6 (2018), pp. 19752–19761. doi:10.1109/ACCESS.2018.2822672.

[40] M.D. Peckel, A MOS delay model for switch-level simulation, Master Thesis, McGill University, Montreal, Canada, 1985.

[41] J.P. Uyemura, Chip Design for Submicron VLSI: CMOS Layout and Simulation, 1st ed., Thomson, New York, 2006.
[42] D.A. Hodges, H.G. Jackson, and R.A. Saleh, *Analysis and Design of Digital Integrated Circuits*, 3rd ed., McGraw-Hill, New York, 2004.

[43] S.M. Sharroush, *Representing the transistor by an equivalent resistor*, 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA), Ras Al Khaimah, United Arab Emirates: IEEE, 6–8 Dec. 2016.

[44] M. Fujishima, K. Asada, and T. Sugano, *Evaluation of delay-time degradation of low-voltage BiCMOS based on a novel analytical delay-time modeling*, IEEE J. Solid-State Circuits 26 (1) (1991), pp. 25–31. doi:10.1109/4.65706.

[45] Semiconductor Industry Association, *2001 International technology roadmap for semiconductors (ITRS)*, Semiconductor Industry Association, Aug. 21, 2001 [Online]. Available: https://www.semiconductors.org/resources/2001-international-technology-roadmap-for-semiconductors-ITRS/. [Accessed: Jan. 31, 2020].

[46] M.S. Ullah and M.H. Chowdhury, *Analytical models of high-speed RLC interconnect delay for complex and real poles*, IEEE Trans. Very Large Scale Integr. VLSI Syst. 25, 6, (Jun 2017), pp. 1831–1841. doi:10.1109/TVLSI.2017.2654921

[47] D. Prasad, C. Pan, and A. Naeemi, *Modeling interconnect variability at advanced technology nodes and potential solutions*, IEEE Trans. Electron Devices. 64, 3, (Mar 2017), pp. 1246–1253. doi:10.1109/TED.2016.2645448

[48] M. Sanaullah and M.H. Chowdhury, *Analysis of RLC interconnect delay model using second order approximation*, IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne VIC, Australia, 1–5 Jun. 2014.

[49] Nanoscale Integration and Modeling (NIMO) Group, ASU, *Berkeley predictive technology model (BPTM)*, Nanoscale Integration and Modeling (NIMO) Group, 2007. [Online]. Available: http://ptm.asu.edu/modelcard/45nm_MGK.pm. [Accessed: 12 Aug. 2020].

[50] M.A. Siddiqi, *Dynamic RAM: Technology Advancements*, CRC Press, New York, 2013.

[51] B. Razavi, *Charge steering: A low-power design paradigm*, Proceedings of the IEEE Custom Integrated Circuits Conference, San Jose, CA, USA: IEEE, 22-25 Sept. 2013