A Compact CMOS Memristor Emulator Circuit and its Applications

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Abstract—Conceptual memristors have recently gathered wider interest due to their diverse application in non-von Neumann computing, machine learning, neuromorphic computing, and chaotic circuits. We introduce a compact CMOS circuit that emulates idealized memristor characteristics and can bridge the gap between concepts to chip-scale realization by transcending device challenges. The CMOS memristor circuit embodies a two-terminal variable resistor whose resistance is controlled by the voltage applied across its terminals. The memristor ‘state’ is held in a capacitor that controls the resistor value. This work presents the design and simulation of the memristor emulalation circuit, and applies it to a memcomputing application of maze solving using analog parallelism. Furthermore, the memristor emulator circuit can be designed and fabricated using standard commercial CMOS technologies and opens doors to interesting applications in neuromorphic and machine learning circuits.

Index Terms—Memristors, memcomputing, neuromorphic, non-von Neumann computing, ReRAM.

I. INTRODUCTION

Moore’s Law has enabled the semiconductor industry to sustain continual advancement in computing architectures by steadily scaling transistor size, and adding more architectural complexity while improving the energy-efficiency of the integrated circuit architectures. This has sustained the development of several key computing and communication technologies for several decades. However it appears that in order to continue gaining from the transistor bounty of Moore’s scaling in the nanometer regime, we need to radically rethink existing computing architectures. The new architectures are required to transcend the device variability and interconnect scaling bottlenecks of the traditional von-Neumann architecture, should exploit massive parallelism and locally employ memory within the computing elements in a manner similar to biological brains. One emerging technology that is promising for such computing architectures is memristors, or resistive RAM (ReRAM). Recent progress in memristive devices has spurred renewed interest in reconfigurable and neuromorphic computing architectures [1]–[5].

The memristive devices, integrated with conventional CMOS, are expected to realize low-power neuromorphic circuits with increased reconfigurability and smaller physical layout area [6], [7]. Since multi-valued memristor device technology is yet to mature and its analog behavior in-situ with circuits is still being characterized in the literature [8]–[10], we propose a low-risk and robust alternative for prototyping machine learning and neuromorphic systems in standard CMOS. The rest of the manuscript is organized as follows. Section II presents a brief background on memristors along with the defining characteristics of memristive circuits and devices. Section III presents the CMOS memristor (emulator) circuit along with simulation results. Finally Section IV presents an application using the proposed circuit, followed by conclusion.

II. MEMRISTOR CHARACTERISTICS

Memristor was defined as a two-terminal circuit-theoretic concept in a seminal paper by Chua [11], and later extended to a wider class of memristive systems [12]. The generic equation to describe such memristive systems is given by

\[ y = g(x, u, t) \cdot u \]  

(1)

\[ \dot{x} = f(x, u, t) \]  

(2)

where \( x \) represents the state, and \( u \) and \( y \) are the outputs of the system respectively, \( f \) is a continuous function n-valued function, and \( g \) is a scalar function [3], [13]. This relation can be interpreted as a voltage-controlled memristor, where the current \( i \) in the memristor is related to the voltage \( u \) by

\[ i = G(x) \cdot v \]  

(3)

with its state update equation

\[ \dot{x} = f(x, u, t) \]  

(4)

Here, \( G(x) \) is called memductance (i.e. memory conductance), and depends upon the charge that has flown across the device [3]. Decades later in year 2008, HP correlated the ideal memristor concept with a metal-oxide resistive switching thin-film device [1]. In the same paper, a linear ion drift model was introduced to describe the behavior of the memristive device. Since then, several models have been investigated to fit the equations to the experimental device behavior [3], [14], [15].

A unique set of ‘fingerprints’ have been established based on the underlying circuit theory, to distinguish memristors from other resistance-switching devices. A memristor must exhibit a ‘pinched’ hysteresis loop that must pass through the origin in its \( i - v \) switching curve, when the applied sinusoid input is zero [16]. Further, the pinched hysteresis loops of ideal memristors must be odd symmetric, otherwise they are modeled as generic memristive devices [16]. Another fingerprint of a memristor is that, as the frequency of the input sinusoid is increased, the area enclosed in the pinched loops progressively shrinks and eventually collapses to a straight line, or a single-valued function [3]. The fundamental promise of the memristors lies in the ‘analog’ memory, that endows it with the ability to store as well as manipulate information...
in analog-domain, opposed to digital very large-scale integrated circuits (VLSICs). Furthermore, these elements can be combined to realize analog computing parallelism, enshrined under memcomputing [3], [17], [18]. This analog computing ability is also harnessed in neuromorphic computing, where memristors realize analog synapses that learn based on spiking-timing dependent plasticity (STDP), a local computing rule that is being investigated as an unsupervised learning approach for deep learning [6], [8], [10], [19]–[21].

III. CMOS Memristor Emulator Circuit

In-spite of several promising features of idealized memristors, their large-scale adoption has been impeded by the practical limitations of fabricated memristive or resistive-RAM (ReRAM) devices. Device characteristics such as the switching threshold voltages and resistances are variable (and stochastic) for each device and across several devices, and depend upon the initial ‘forming’ step [22]–[24]. Further, it is challenging to realize stable weights for more than 1-bit resolution in filamentary devices due to the relaxation of the filament and is currently being addressed in device research [10], [25]. HfOx and TaOx based devices have exhibited up to 9 states and their performance within a circuit is being investigated [26]. A greater impediment from circuit design perspective is the lower on-resistance observed in reported devices (100Ω – 100kΩ), which leads to power hungry driver circuits, and thus a fundamental trade-off between parallelism and energy-efficiency. Moreover, memristive devices fall well short of CMOS components in terms of their endurance. Thus, it is desirable to realize CMOS memristor (emulator) circuits for system-level design memcomputing exploration while the memristive devices mature and are integrated into a commercially available CMOS platform.

![Figure 1](image1.png)

Figure 1. (a) Conceptual block diagram for the CMOS memristor emulator, (b) A circuit implementation of the memristor concept.

We disclosed the dynamic memristor/synapse circuit concept in the patent application [27]. In this work, we present CMOS memristor circuit design details, analysis, and its application in memcomputing. The fundamental concept is illustrated in Fig. 1(a), where an n-channel MOSFET (NMOS) $M_1$ implements a floating variable resistance between terminals A and B. The variable resistance is achieved by operating the transistor $M_1$ in linear (triode) or near-linear region. The voltage difference across the terminals A and B, $V_{AB}$, is sensed, integrated over time and then used to control the gate of the transistor $M_1$. The integrator holds the ‘state’ of the variable resistor and updates it according to the voltage difference $V_{AB}$. If a positive voltage is applied across the resistor, the gate voltage is increased and thus resulting in a decrease in the resistance (or an increase in conductance) across A and B. Similarly, a negative potential across the resistor results in an increase in the resistance (or decrease in conductance). This circuit embodying a variable resistor with a dynamic memory, realizes the functionality of the idealized memristor concept. Further, this compact circuit can be modified to implement analog synapses that exhibits biocompatible learning rules, including the spike-timing dependent plasticity (STDP) [27].
In general, the dynamics of the memristor emulator circuit can be described as

\[ I \approx K P_n \frac{W}{L} (V_{GS} - V_{THN}) \cdot V_{AB} \]  

(5)

where \( V_{GS} \) and \( V_{THN} \) are the gate-to-source and threshold voltages, and \( K P_n \) is the transconductance parameter, \( W \) is the width and \( L \) is the length of the NMOS \( M_1 \). If the source of \( M_1 \) is held at a common-mode voltage \( V_{CM} \), the above equation can be equivalently interpreted as the variable conductance \( G \)

\[ G \approx K P_n \frac{W}{L} (V_{G} - V_{CM} - V_{THN}) \]  

(6)

which expresses a direct relation between the state \( (x \equiv V_{G}) \) and the conductance \( (G) \). In order to force \( M_1 \) in triode for large drain-source voltage swings, a zero-threshold voltage transistor (ZVT) device \( (V_{THN} = 0) \) available in standard CMOS platforms is preferred. Also, in these scaled CMOS technologies, the MOSFET output resistance \( (r_n) \) in moderate saturation is inherently low due to short channel effects. This allows the proposed circuit to exhibit desired memristive behavior even when \( M_1 \) is in moderate saturation. In general, the dynamics of the memristor emulator circuit can be described as

\[ I = G(x) \cdot V_{AB} \]  

(7)

\[ \dot{x} = \frac{G_m(V_{AB})}{C_m} \cdot V_{AB} \equiv f(V_{AB}, t) \]  

(8)

where Eqs. 7 and 8 are equivalent to memristor equations seen in Eqs. 3 and 4 respectively.

The simulated current-voltage hysteresis curve for the memristor circuit is shown in Fig. 3. The memristor was swept with a sinusoidal input of frequency 1 MHz, amplitude 200mV and a common-mode DC offset \( V_{CM} \) equal to 600mV, while \( \Phi_1 \) was held at logic high (1.2 V). The circuit characteristics in Fig. 3(a) exhibit a pinched hysteresis curve typical of an ideal memristor. The memory effect in the synapse is further confirmed by the elliptical-like state trajectory seen in Fig. 3(b). The memristor circuit is further characterized by applying a modulated half sine-wave (derived from a sine-wave of 1 GHz frequency) as shown in Fig. 3(a). This waveform can be understood as successive voltage sweeps being applied to the synapse, to trace closely spaced analog memory states. The circuit characteristics in Fig. 3(a) further exhibit near-ideal memristor behavior with multiple pinched lobes. The synapse state trajectory seen in Fig. 3(b), which demonstrates that the synapse can hold fine-grained analog memory states that can be precisely controlled by an external stimulus. Moreover, the pinched lobes collapse into a straight line as the input frequency is increased, as a signature of memristors as discussed in Section II. An advantage of this circuit is that the resistance range of the emulated memristor can be chosen as desired depending upon the sizing of NMOS \( M_1 \); a flexibility not conveniently available with memristive devices.

Figure 4. (a) Modulated half-sine wave input waveform to generate successive voltage sweeps. (b) I-V curves with the modulated sine-wave input at 1 GHz frequency. (c) state trajectory for the synapse.

The memristor circuit in Fig. 2 inherently realizes a current-mode sample-and-hold to hold the analog state of the synapses. The sampling switch \( (M_{sw}) \) prevents the transconductor \( G_m \)’s output from leaking the state \( (V_{G}) \) on capacitor \( C_m \) when no inputs are applied (since \( G_m \)’s output impedance is finite). This operation can also be interpreted as an energy barrier which prevents the stored electrons on \( C_m \) from leaking-out immediately. The electrons will however leak-out eventually due to subthreshold and junction leakages in the MOSFETs. However, we can achieve storage times of up to several seconds by using large \( C_m \) and a low-leakage devices. Fig. 2 shows transient simulation results which exhibit the analog state manipulation and short-term retention property of the dynamic memristor. Here, a pseudo-random sequence is applied with \( (\Delta T = 5 \text{ ns}, V_{pulse} = 100 \text{mV} \text{ amplitude}, V_{CM} = 600 \text{mV} \text{ DC offset}) \) and 1 MHz clock rate. We can observe that the state, \( V_G \), is incrementally updated corresponding to a positive or negative pulse input. Since the conductance updates of the memristor are monotonic with respect to the applied pulses (or voltage spikes), it can be used to dynamically store analog weights in a machine learning or spiking neural network circuit [8]. The drain-source resistance of \( M_1 \) is altered by updating the gate voltage, \( V_G \), by applying spikes across the terminals A-B. Assuming, rectangular spiking pulses, the incremental update in the gate voltage can be expressed as

\[ \Delta V_G \approx \frac{G_m}{C_m} \cdot V_{spk} \Delta T \]  

(9)
where $V_{\text{spk}}$ and $\Delta T$ are the spike height and width respectively.

Figure 5. Pulsed characterization response of the synapse circuit showing the monotonic incremental control of the state, when positive and negative pulse are applied.

The presented memristor circuit was conceived while trying to understand the relation between the pinched hysteresis behavior of memristor and their ability to hold analog states. As shown in this work, the switch $M_{\text{sw}}$ is not needed for generating the pinched hysteresis sweep, but is essential for retaining the analog state by presenting a barrier for the charge to leak away. This reinforces the understanding that in order to realize analog memristive device, an electrochemical, tunneling \cite{28} or other form of barrier is needed to retain multiple analog-like states. Also, in the presented dynamic memristor, the state eventually leaks away. A bistable version of the circuit can be realized by incorporating a weak latch structure to quantize the dynamic state for long-term binary retention (see \cite{27}).

The transconductor-based memristor emulator circuit presented in this work, even though simple in structure, offers tremendous advantages over previously reported emulators \cite{29}. The circuit is compact, consumes very small bias current ($10-100 nA$), can be fabricated in standard CMOS technology, offers design flexibility to choose memristor specifications, and doesn’t require an analog-to-digital converter (ADC) \cite{30}, or opamps \cite{31}-\cite{36} to implement its functionality.

IV. MEMCOMPUTING APPLICATION

The developed memristor emulator circuit can be leveraged for system-level exploration of memcomputation and neuromorphic computing applications \cite{17}, \cite{18}, in parallel to memristive device development. Here, we apply the circuit to realize a 2D maze solver using a memristive network based on \cite{17} and is shown in Fig. 6. Each tile of this network consists of two CMOS memristors and two NMOS switches each. This $8 \times 8$ grid size network topology is generic and can be configured to a specific maze pattern by selectively opening and closing the switches in Fig. 6 \cite{3}. \cite{17}. Initially, the states of all the memristor cells are set to zero (or high-resistance state) in simulation by initializing the respective gate voltages ($V_G$) to 0V. The array addressing scheme for switch configuration and state reset is not shown here. DC voltages $V_1 = 800 mV$ and $V_2 = 400 mV$ are applied across the desired entrance and exit nodes in the maze to solve for available paths, and the strobe $\Phi_1$ is set high to allow the network to settle. The simulation results for this network are illustrated in Fig. 7 where the state voltages for each of the memristor cells are plotted as a function of time, after the strobe $\Phi_1$ is applied. Here, the memristors in the path connecting the entrance and the exit, i.e. the solution of the maze, start conducting current as they decrease their respective resistances. On the other hand, the memristors in the non-conducting paths also start conducting due to leakage in the memristor circuit and the ‘sneak paths’, and their states increase as well, but at a lower rate as seen in Fig. 7(a&b). Eventually all state nodes try to reach closer to $V_{\text{DD}}$. The result of the network is read out by setting the strobe period such that the states of the ‘On’ memristors saturate, allowing for a voltage margin ($V_{\text{margin}}$) for sensing as shown in Fig. 7. The nodes that are in the maze solution path can be determined by thresholding their states above the voltage level set by leakage currents in ‘Off’ memristors. Here, the static power consumption is around $12.9 \mu A$ and peak dynamic current is $\sim 4.8 \mu A$ from the supply. This application circuit can be further optimized for maximizing the read margin, and the decision threshold and strobe times can be digitally calibrated to compensate for process, voltage and temperature (PVT) variations.

Figure 6. The $8 \times 8$ maze used for simulation using the CMOS memristor network.

Figure 7. Simulation results for the maze with: (a) $C_m = 1pF$ and $I_{\text{bias}} = 1\mu A$, (b) (left) $C_m = 100fF$ and $I_{\text{bias}} = 100nA$.

V. CONCLUSION

A compact memristor emulator circuit in standard CMOS has been presented along with simulation results. The circuit exhibits the signature characteristics for ideal memristors and can transcend the challenges associated with memristive device development in the near future. Furthermore, the circuit has been applied to parallel maze solving, and paves the path for applying the concept to other NP-hard problems that can be solved by exploiting the parallel analog computation.
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