Analysis and reduction of the voltage noise of multi-layer 3D IC with multi-paired power delivery network

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Abstract: Three-dimensional (3D) integrated circuit (IC) technology has been proposed and used to reduce the delay among layers by shortening interconnection with TSVs. However, large power and ground TSV structures generate voltage noise, and cause additional IR-drop in the power delivery network (PDN). In this work, we investigate and analyze the voltage noise in a multi-layer 3D IC stacking with PEEC-based on-chip PDN and frequency-dependent TSV models. Then, we propose a wire-added multi-paired on-chip PDN structure to reduce voltage noise in a 3D IC. Our proposed PDN architecture can achieve approximately a maximum 29% IR-drop reduction compared with the conventional PDN. In addition, we analyze the layer dependency on 3D IC between the conventional and the proposed PDN models.

Keywords: voltage noise, IR drop, 3D IC, TSV, power delivery network (PDN), PEEC, multi-paired

Classification: Integrated circuits

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1 Introduction

Recently, 3D IC stacking technology has been proposed and considered as a promising solution to exceed the limitations of the Moore era [1]. 3D IC has been proposed and considered as an enabler to extend Moore’s law by enhancing system integration and performance. In a 3D IC, shortening wire length with vertical interconnections, such as TSVs, can effectively reduce the propagation delay between layers [1, 2, 3, 4]. However, the multi-layer 3D IC inherently generates new issues for circuit and package designers in the power integrity (PI) of the power delivery network (PDN), manufacture of chip-bonding, thermal heat sink, TSV testing, etc. [4].

The operating voltage has been reduced below 1.0 V and current demand for high-performance has been increased, as the technology node is keeping scales down below 22-nm. Thus, voltage fluctuation (e.g., IR-drop) in the PDN has become one of the major problems for robust circuit operation in a 3D IC [5, 6, 7, 8].

In this study, we use a simple and accurate analysis methodology to investigate the power delivery network of 3D IC stacking structures. The parasitic of on-chip metal PDN is extracted with partial electrical equivalent circuit (PEEC)-based models [9]; and frequency-dependent TSV parameters, including C4 bumps, are generated by the EM modeling method [10, 11, 12]. We combine the on-chip PDN and TSV in multi-layer 3D IC for power integrity analysis of the static and dynamic
voltage drop. In addition, various PDN structures are investigated in the proposed 3D IC analysis methodology, and an optimal PDN architecture for reducing IR drop is obtained. Fig. 1 shows the general TSV-based 3D IC stacking methodology of two layers. The multiple dies are stacked in face-to-back bonding to stack more than two layers. We vary the number of stacking layers to identify the impact of the multi-layer on the power integrity.

The main contributions of our work are summarized as follows:

- We exploit the PEEC-based parasitic extraction models for on-chip PDN interconnect
- We use 3D EM based modeling methodology to generate frequency-dependent S-parameter for TSV structures.
- We combine the on-chip PDN and TSV in multi-layer 3D IC for power integrity analysis of both the static and dynamic voltage drop.
- We investigate various PDN structures in the proposed 3D IC analysis methodology, and propose an optimal PDN to reduce IR drop.

The rest of this paper is organized as follows: Section 2 explains the analysis methodology of on-chip PDN and S-parameter TSV models, which is used for the PDN of multi-layer 3D IC stacking. Section 3 explains the simulation and analysis results of the proposed multi-pared and wire-added PDN structures, while Section 4 concludes the paper.

2 Analysis of power delivery network in the TSV-based 3D IC

As the PDN has become complicated, and wire resistance has increased owing to interconnect scaling, supply voltage fluctuations due to the IR drop have become a significant problem in PDN design. A PEEC method [9] has been introduced for an accurate extraction of the RLC components of wires. We use the PEEC method to extract the RLC components from a PDN interconnect mesh having nine VDD and nine GND pads [10]. To obtain a frequency-dependent model of TSV structures, we use a 3D electromagnetic (EM) method [11]. Frequency-dependent S-parameters of the TSV structures are extracted from the 3D EM modeling method based on a mixed-potential integral equation [10, 11].
In this paper, we apply the EM modeling method to the TSV structure shown in Fig. 2, and generate S-parameter data with TSV parameters, as explained in Table I [1]. We then perform a dynamic transient analysis with clock buffers to simulate the IR-drop-related voltage fluctuations, and analyze the PDN architecture in 3D IC stacking.

Table I summarizes the metal interconnect parameters and TSV dimensions used in this study. The on-chip PDN consists of two top metal lines (i.e., M6 and M5), and the power supply of the logic block is connected through vias to supply the required current as shown in Fig. 3; (a) and (b) show 3D visualizations of the PEEC elements in the regular on-chip PDN structure and the multi-paired structure, respectively. All the wire segments and vias are plotted, and ports for the VDD and GND are shown in red color. The corresponding VDD and GND ports and the logic block is represented in Fig. 3(c). We assume that the 0.5 mm × 0.5 mm die contains nine VDDs and nine GNDs, and all of these ports are connected to the corresponding S-parameter TSV ports to construct the entire PDN of 3D IC, as shown in Fig. 1. We apply an ideal DC voltage source simultaneously to all the power and ground TSVs. The center VDD and GND ports are connected to the power supply pins of the logic gates (i.e., clock buffers) as shown in Fig. 3(c). The logic consists of 40 clock buffers to mimic the current load in the simulations, and is implemented in 22-nm technology node [13]. The nominal VDD value is set to 0.9 V, and the clock buffer size is \( W_n = 4 \mu m \) and \( W_p = 8 \mu m \). We then measure the power supply fluctuation for various configurations of 3D IC when the internal

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**Table I.** Structural parameters of the metal interconnect and TSV.

| Parameter               | Value (µm) |
|-------------------------|------------|
| Metal 5 (M5) width      | 5          |
| Metal 5 (M5) pitch      | 200        |
| Metal 6 (M6) width      | 10         |
| Metal 6 (M6) pitch      | 200        |
| TSV diameter (D)        | 10         |
| TSV height (H)          | 50         |
| TSV pitch               | 200        |
| TSV linear thickness    | 0.1        |
| TSV pad size            | 15         |

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logic makes transitions in SPICE transient analysis [14]. First, we stack a single layer of dies with TSV and C4 bump. Then, we vary the number of stacking layers, to identify the impact of the multi-layer on the IR-drop.

3 Multi-paired PDN structure for reduction of voltage noise

3.1 Multi-paired PDN structure

Fig. 4(a) shows the voltage fluctuation results of the 3D IC with a single layer TSV. As shown, the TSV attributes 89% additional voltage droop and 98% ground bump in a single layer. Fig. 4(b) shows the impact of the number of 3D IC layers on the
voltage drop in both RL and RLC PEEC models. As shown, larger voltage fluctuation is expected as the number of layer increases. In addition, the RLC model shows more impact on the voltage variation than the RC model. For example, approximately $1.8\times$ more VDD droop occurs for five layers 3D IC from single layer with all RLC included and the additional 10% (five layers) $\sim 43\%$ (single layer) droop attributes to large $L$ in the PDN. Therefore, the inductance ($L$) component should be considered in high-frequency 3D IC for accurate voltage fluctuation analysis, such as $L\text{d}i/\text{d}t$ noise.

Shorter wire space between VDD and GND can effectively reduce the mutual inductance of wire [15]. Thus, we propose and investigate the multi-paired PDN structure shown in Fig. 3(b), and compare the voltage fluctuation with that of the conventional regular structure (e.g., Fig. 3(a)). We measure the benefit of the proposed PDN architecture with increasing number of layers in 3D IC stacking. Table II compares the VDD droop between the regular PDN and the proposed multi-paired PDN. As shown, the proposed PDN architecture achieves up to 21% reduction in VDD droop for a single layer, and the benefit is attenuated as the number of layers increases.

### 3.2 Wire-added multi-paired PDN structure

As mentioned in the previous analysis, narrower wire space between VDD and GND effectively reduces mutual inductance, and appears to provide less voltage fluctuation on PDN. Based on this result, we investigate the effect of the metal density and the wire space between wire pairs.

First, additional VDD and GND wire pairs are added to the multi-paired PDN structure, as shown in Fig. 5. Then we vary the wire space between the original wires and newly added wire pairs. Fig. 5(a) shows the minimum space between the original wire pairs and added wire pairs (i.e., $20\,\mu m$). Then we increase this space to $140\,\mu m$ in $20\,\mu m$ steps, which is the minimum wire space of metal 6. The interconnect in metal 6 layer has larger width than metal 5, thus the same wire space can generate more symmetric structures in our study. Added wire pairs overlap the pre-existing original wires when the space becomes larger than $140\,\mu m$. Also, $80\,\mu m$ wire space is impossible, because the GND wire passes through the VDD TSV pad.

Table III summarizes the simulation results of the worst VDD droop for various wire space in the wire-added multi-paired structure. The reduction of the voltage fluctuation

| # of layer | Regular structure VDD droop (mV) | Proposed structure VDD droop (mV) | Reduction (%) |
|------------|----------------------------------|----------------------------------|---------------|
| 1          | 88.8                             | 70.2                             | 20.9          |
| 2          | 122.3                            | 109.1                            | 10.8          |
| 3          | 146.0                            | 136.0                            | 6.8           |
| 4          | 164.4                            | 155.7                            | 5.3           |
| 5          | 178.5                            | 170.8                            | 4.3           |
droop is calculated with respect to the conventional regular structure (Fig. 3(a)). As shown, the case of 20 µm wire space (Fig. 5(a)), which is the minimum, results in the best reduction of the VDD droop, because it has the shortest return paths. On the other hand, the 120 µm wire space case, shown in Fig. 5(b), provides the worst voltage fluctuation (and minimum reduction from the regular structure), because it

Table III. The worst VDD droop in the wire-added multi-paired (two pairs) PDN structure. 80 µm space is impossible, because the GND line runs over the VDD ports in metal 6.

| Wire space (µm) | Worst VDD droop (mV) | Reduction (%) (ref. to regular structure VDD droop) |
|-----------------|----------------------|---------------------------------------------------|
| 0 (no added wire) | 70.2                 | 20.9                                              |
| 20              | 64.8                 | 27.0                                              |
| 40              | 65.7                 | 26.0                                              |
| 60              | 66.9                 | 24.7                                              |
| 100             | 69.4                 | 21.8                                              |
| 120             | 71.2                 | 19.8                                              |
| 140             | 67.0                 | 24.5                                              |

Fig. 6. Top view of two VDD (green) and GND (blue) wires are added to the proposed multi-paired (three pairs) PDN structure.
has the longest current return paths. It is worth mentioning that a PDN structure that has more regular space between wires degrades the efficiency of inductance reduction (e.g., Fig. 5(b)).

In addition, to analyze the benefit of the proposed wire-added multi-paired PDN on the power integrity of the 3D IC, we apply the optimum wire-added multi-paired structure (i.e., minimum wire space) to multi-layer 3D IC. Fig. 6 shows that for symmetry, one more VDD and GND wire pair is added to the final PDN structure. Fig. 7 compares various PDN architectures. For a single layer, three pairs (two additional pairs) of VDD and GND reduce the VDD droop by more than 29%, compared to the regular (i.e., non-paired) PDN structure. However, the VDD droop reduction attenuates as the number of layer increases, showing approximately 29.1% to 6.8% reduction from one to five stacking layers. The benefit of the two wire-pair addition (three pairs) is only less than 2% points from the single wire-pair case. Therefore, a multi-paired (one pair) structure without adding any additional wire pairs is the best option to minimize voltage noise with limited wire resources. Two pairs of the multi-paired PDN structure is considered to be the best trade-off between voltage noise reduction and wire resources.

4 Conclusion

In this paper, we first investigate the voltage noise of multilayer 3D IC with a proposed analysis methodology of PEEC-based PDN and frequency-dependent TSV models. We find that TSV significantly affects voltage fluctuation in PDN. Moreover, the inductance component and frequent-dependent TSV models are vital for accurate understanding of the power integrity of the 3D IC. Second, we propose and investigate the multi-paired and wire-added on-chip PDN structure to reduce the voltage noise of PDN in 3D IC. The multi-paired structure effectively reduces IR-drop by approximately a maximum 21%, and as the number of layers increases, the advantage decreases. Additionally, we analyze the correlation between wire space and voltage noise. Simulations based on our proposed method reveal that
shorter wire space, by adding VDD and GND wire pairs, effectively reduces $L_{d/dt}$ noise. Our ongoing work seeks to analyze not only a simple layer configuration, assuming all layers are active, but also more complex configuration, such as the power gated 3D IC.

**Acknowledgments**

This research was supported by the Basic Science Research Program, through the National Research Foundation of Korea (NRF), funded by the Ministry of Education (NRF-2017R1D1A1B03028065). This present research has been conducted by the Research Grant of Kwangwoon University in 2016. EDA tools were partially supported by IDEC at KAIST.