Rectification at Graphene-Semiconductor Interfaces: Zero-Gap Semiconductor Based Diodes

S. Tongay\textsuperscript{1,2,3}, M. Lemaitre\textsuperscript{1}, X. Miao\textsuperscript{2}, B. Gila\textsuperscript{2,3}, B. R. Appleton\textsuperscript{2,3}, and A. F. Hebard\textsuperscript{2}

\textsuperscript{1} Materials Science and Engineering, University of Florida, Gainesville, Florida 32611
\textsuperscript{2} Department of Physics, University of Florida, Gainesville, FL 32611 and
\textsuperscript{3} Nanoscience Institute for Medical and Engineering Technology, University of Florida, Gainesville, FL 32611

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Using current-voltage (I-V), capacitance-voltage (C-V) and electric field modulated Raman measurements, we report on the unique physics and promising technical applications associated with the formation of Schottky barriers at the interface of a one-atom-thick zero-gap semiconductor (graphene) and conventional semiconductors. When chemical vapor deposited graphene is transferred onto n-type Si, GaAs, 4H-SiC and GaN semiconductor substrates, there is a strong van der Waals attraction that is accompanied by charge transfer across the interface and the formation of a rectifying (Schottky) barrier. Thermionic emission theory in conjunction with the Schottky-Mott model within the context of bond-polarization theory provides a surprisingly good description of the electrical properties. Applications, such as to sensors where in forward bias there is exponential sensitivity to changes in the Schottky barrier height due to the presence of absorbates on the graphene or to analogue devices for which Schottky barriers are integral components are promising because of graphene’s mechanical stability, its resistance to diffusion, its robustness at high temperatures and its demonstrated capability to embrace multiple functionalities.

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1. INTRODUCTION

Single atom layers of carbon (graphene) have been studied intensively after becoming experimentally accessible with techniques such as mechanical exfoliation\textsuperscript{[1]}, thermal decomposition on SiC substrates\textsuperscript{[2]} and chemical vapor deposition (CVD)\textsuperscript{[3, 4]} . Graphene is a zero-gap semiconductor (ZGS) with an exotic linearly dispersing electronic structure, high optical transparency, exceptional mechanical stability, resilience to high temperatures and an in-plane conductivity with unusually high mobility\textsuperscript{[5]}. Accordingly, graphene has been proposed as a novel material for incorporation into devices ranging from Schottky light emitting diodes (LEDs)\textsuperscript{[6–8]} to field effect transistors (FETs)\textsuperscript{[9, 10]}. Although integration of graphene into semiconductor devices is appealing, there is still very little known about the interface physics at graphene-semiconductor junctions. To this end, graphene/Si junctions showing successful solar cell operation have been produced by transferring either CVD-prepared\textsuperscript{[1]} or exfoliated\textsuperscript{[8]} graphene sheets onto Si substrates. The resulting diodes have shown ideality factors (measure of deviation from thermionic emission) varying from ~1.5 \textsuperscript{[6]} which is close to the ideal value of unity, to values in the range ~5-30 on exfoliated graphene\textsuperscript{[8]} implying that additional non-thermionic current carrying processes exist at the graphene/Si interface. Nevertheless these promising results point to the need for additional research on integrating graphene with technologically important semiconductors.

Here we report rectification (diode) effects at ZGS-semiconductor (i.e graphene-semiconductor) interfaces on a surprisingly wide variety of semiconductors.
2. EXPERIMENTAL METHODS

Our diodes are fabricated by transferring large scale graphene sheets grown by chemical vapor deposition (CVD) directly onto the semiconductor under investigation and allowing Van der Waals attraction to pull the graphene into intimate contact with the semiconductor. Large-area single layer graphene sheets were synthesized on Cu foils via a multi-step, low-vacuum CVD process similar to that used in Ref. [13]. A quartz tube furnace operating in CVD-mode was loaded with 25-50 µm-thick Cu foils (Puratronic, 99.9999% Cu), evacuated to 4 mTorr, and subsequently heated to 500 °C under a 25 sccm flow of H2 at 325 mTorr. After 30 minutes soak, the temperature was raised to 1025 °C for 60 minutes to promote Cu grain growth (mean grain size exceeds 5 mm2 determined by optical microscopy). An initial low-density nucleation and slow growth phase was performed at 1015 °C for 100 minutes with a mixture of CH4 and H2 at a total pressure of 90 mTorr and flows of ≤ 0.5 and 2 sccm, respectively. Full coverage was achieved by dropping the temperature to 1000 °C for 10 minutes while increasing the total pressure and methane flow to 900 mTorr and 30 sccm, respectively. A 1.5 µm-thick film of PMMA (MicroChem, 11% in Anisole) was then spin-cast onto the Cu foils at 2000 rpm for 60 seconds. The exposed Cu was etched in an O2 plasma to remove unwanted graphene from the backside of the samples. The PMMA supported films were then etched overnight in a 0.05 mg/L solution of Fe(III)NO3 (Alfa Aesar) to remove the copper. The graphene-PMMA films were then washed in deionized water, isopropyl alcohol (IPA), and buffered oxide etch for 10 minutes, each. After growth and transfer, the graphene films were characterized and identified using a Horiba-Yvon micro-Raman spectrometer with green, red and UV lasers.

Commercially available semiconducting wafers were purchased from different vendors. n-Si and n-GaAs samples were doped with P (2-6×1015 cm⁻³) and Si (3-6×10¹⁶ cm⁻³) respectively. Epilayers of n-GaN and n-4H-SiC, 3-6 µm-thick, were grown on semi-insulating sapphire substrates with Si (1-3×10¹⁶ cm⁻³) and N (1-3×10¹⁷ cm⁻³) dopants. During the sample preparation and before the graphene transfer, the wafers were cleaned using typical surface cleaning techniques. Ohmic contacts to the semiconductors were formed using conventional ohmic contact recipes [14-17]. Multilayer ohmic contacts were thermally grown at the back/front side of the semiconductor and were annealed at high temperatures using rapid thermal annealing. After the ohmic contact formation, a 0.5-1.0 µm thick SiO₂ window was grown on various semiconductors using a plasma enhanced chemical vapor deposition (PECVD) system, and ~ 500 nm thick gold electrodes were thermally evaporated onto SiO₂ windows at 5×10⁻⁷ Torr. The graphene contacting areas were squares with sides in the range 500 µm to 2000 µm. Application of IPA improves the success rate of the graphene transfer and does not affect the measurements presented here. After depositing the graphene/PMMA films, the samples were placed in an acetone vapor rich container for periods ranging from 10 minutes to ~10 hours. The acetone bath allows slow removal of the PMMA films without noticeable deformation of the graphene sheets.

Prior to the graphene transfer there is an open circuit resistance between the Au contacts and the semiconductor. After the transfer of the PMMA-graphene bilayer, the graphene makes simultaneous connection to the Au contacts and the semiconductor as evidenced by the measured rectifying I-V characteristics. Since the diodes made with the PMMA-graphene bilayer show essentially the same rectifying characteristics as the samples in which the PMMA has been dissolved away, we conclude that the carbon layer on the PMMA (shown by Raman measurements to be graphene) is making intimate contact with the semiconductor.

A schematic for our graphene based diodes is shown in FIG. 1: (a) Graphene/semiconductor diode sample geometry where the J – V characteristics were measured between ohmic contact (ground) and graphene (high) (b) Hall bar geometry for measurements of the carrier density of graphene. In this configuration the graphene does not make contact with the semiconductor. (c) Optical image of the graphene/Au/SiO₂ - graphene/Si transition edge after the graphene transfer. (d) Scanning electron microscope image of Cu foils after the CVD graphene growth showing formation of grain sizes large with respect to the 10 µm scale bar.
Fig. (a); the backside of the semiconductor substrate is covered with an ohmic contact and the graphene sheet transferred onto Cr/Au contacts grown on SiO$_2$ windows. After the transfer, the graphene and semiconductor adhere to each other in an intimate Van der Waals contact in the middle of the open window, and the Cr/Au contact pad provides good electrical contact with the graphene. Our ohmic contact arrangements allow current density versus voltage (J-V) and capacitance versus voltage (C-V) measurements to be taken separately. J-V measurements were taken in dark room conditions using a Keithley 6430 sub-femtoamp source-meter, and C-V measurements were taken using an HP 4284A capacitance bridge. The electric field modulated Raman measurements were made on the same configuration. Four-terminal transport and Hall measurements however were performed with an intervening layer of SiO$_x$, (Fig. 1(b)) using a physical property measurement system (PPMS), at room temperature in magnetic fields up to 7 Tesla.

In the literature the quality of graphene sheets is measured by a large 2D to G intensity ratio ($I_{2D}/I_G$) and a low D peak intensity ($I_D$). Single layer graphene is expected to show $I_{2D}/I_G > 2$, and the amount of disorder in the sheets is often correlated with $I_D$. In our samples, we observe $I_{2D}/I_G \geq 2$ and a negligible D peak amplitude. However after graphene transfer to the semiconductor substrate, we observe that $I_D$ becomes apparent while $I_{2D}/I_G$ remains the same (Fig. 2(b)). The increase in $I_D$ reflects the lower sheet mobility of CVD-grown graphene and gives rise to weak localization effects at low temperatures [18]. Moreover, because of the low solubility of carbon in Cu, graphene growth onto Cu foils is known to be self-limiting [3], therefore allowing large-area single layers of graphene to be grown onto Cu foil surfaces. After the graphene growth, the backside of the Cu foils have been exposed to O$_2$ plasma to remove unwanted graphene and checked with Raman spectroscopy. This step assures that bi-layer (or multi-layer) graphene is not formed on PMMA/graphene after etching the Cu.

**3. RESULTS AND DISCUSSION**

**A. Raman measurements**

In Fig. 2(a-d), we show typical Raman spectroscopy data taken on graphene sheets grown onto Cu foils by CVD deposition before and after transferring onto semiconductors. The presented scans have been reproduced at more than 20 random spots and are good representations of the quality of the graphene on the Cu foils before transfer and on the semiconductor surface after transfer. In Fig. 2(a), we show typical Raman spectra of CVD-grown graphene on Cu foils and graphene after transfer onto various semiconductor substrates. Graphene sheets show large $I_{2D}/I_G$ ratio, and after the transfer the graphene becomes slightly disordered. (c-d) Raman G and 2D peaks measured respectively on graphene/Cu and on graphene/semiconductor combinations indicated in the legend of panel (b).
foils (see Experimental methods).

The Raman spectrum of exfoliated graphene transferred onto Si/SiO$_2$ substrates has been previously studied as a function of applied bias [23]. It has been found that the G and 2D peaks of graphene are sensitive to the Fermi energy (carrier density) of graphene and allow one to estimate the bias-induced changes in $E_F^{gr}$. Considering the typical operating voltages of Schottky junctions, the low carrier density in graphene, and the associated bias dependence of $E_F^{gr}$, we have also measured the Raman spectrum of graphene transferred onto GaN as a function of applied bias. Our Raman measurements differ from those reported in Ref. [23] in the following three ways: (1) we are using CVD-prepared rather than exfoliated graphene, (2) the graphene is in direct contact with GaN rather than oxidized Si, and (3) the graphene is measured in situ as part of a Schottky rather than a gated FET. In Fig. 3, we show the evolution of the Raman spectrum as a function of applied bias. While G and 2D are almost identical with the same peak positions at 0V and 1V, in reverse bias at 10V, the G band shifts to higher (by $\sim$6--3 cm$^{-1}$) and the 2D band shifts to lower (by $\sim$7--3 cm$^{-1}$) wavenumbers. The relative shifts in the Raman peaks along with a reduction of the 2D/G peak ratio from 2.6 (at 0V) to 1.2 (at 10V) imply that graphene sheets transferred onto GaN become electron doped. Considering the previous results reported on graphene/SiO$_2$ [23], the shift in $E_F$ can be estimated to be in the range $\sim$0.2--0.5 eV.

### B. Hall measurements

Hall measurements show that the Hall mobility of the graphene sheets used in our diodes is in the range 1400--2100 cm$^2$/Vs, and that the sheets are hole doped with carrier densities in the range 2--8x10$^{12}$ cm$^{-2}$ (Fig. 4). The presence of extrinsic residual doping in exfoliated graphene has been previously reported [1] and attributed to residual water vapor ($p$ type) or NH$_3$ ($n$-type). In both cases annealing reduces the concentration of the dopants and forces $E_F^{gr}$ closer to the neutrality point. For our CVD prepared graphene, the presence of residual impurity doping can be attributed to a lowering of $E_F^{gr}$ due to hole doping of the graphene during the Fe(III)NO$_3$ etching-transfer process [10].

### C. Current-voltage measurements

Schottky diodes are expected to pass current in the forward bias (semiconductor is negatively biased) while becoming highly resistive in reverse bias (semiconductor is positively biased). As seen in Fig. 4(a-d), $J$--$V$ (main panels) and log$J$--$V$ (insets) data taken on various graphene/$n$-type semiconductor junctions display strong rectification. This rectification is a consequence of Schottky barrier formation at the interface when electrons flow from the semiconductor to the graphene as the Fermi energies equilibrate (Fig. 4(b)).

In principle, any semiconductor with electron affinity ($\chi_e$) smaller than the work function of the metal ($\phi_{metal}$) can create rectification at a metal-semiconductor (M-S) interface with Schottky barrier height, $\phi_{SBH} = \phi_{metal} - \chi_e$, given by the Schottky-Mott model. Electron transport over the Schottky barrier at the M-S interface is well described by thermionic emission theory (TE) with the expression;

$$J(T, V) = J_s(T)[\exp(eV/\eta k_B T) - 1],$$

where $J(T, V)$ is the current density across the graphene/semiconductor interface, $V$ the applied voltage, $T$ the temperature and $\eta$ the ideality factor [12]. The prefactor, $J_s(T)$ is the saturation current density and is expressed as $J_s = A^*T^2 \exp(-e\phi_{SBH}/k_B T)$, where $e\phi_{SBH}$ is the zero bias Schottky barrier height (SBH) and $A^*$ is the Richardson constant.

When electronic transport across the barrier is dominated by thermionic emission described by Eq. 1, semilogarithmic plots of the $J$--$V$ curves should display a linear region in forward bias. As seen in the insets of Fig. 4(a-d) the overlying straight line segments of our measurements typically reveal 2--4 decades of linearity, thus allowing us to extract $J_s$ and $\eta$ for each diode. The deviations from linearity at higher bias are due to series resistance contributions from the respective semiconductors. The temperature-dependent data for the graphene/GaAs diode (Fig. 4(a-b)) show that for both

![FIG. 4: $R_{xy}$ versus magnetic field data taken at 300 K. Typically sample mobilities are in the range 1400-2100 cm$^2$/Vs and carrier densities (holes) in the range 2.8x10$^{12}$ cm$^2$.](image-url)
bias directions, a larger (smaller) current flows as the temperature is increased (decreased) and the probability of conduction electrons overcoming the barrier increases (decreases). In forward bias, the TE process manifests itself as linear “log-J-V curves” (Fig. 5(b)) and linear “ln(I_s(T)/T^2) versus T^{-1} curves” (Fig. 5(c)) where I_s(T) = J_s(T)A. The SBH is calculated directly from the slope of this linear dependence. By repeating these temperature-dependent measurements for the four different diodes, we find that the SBH (φ_{SBH}^V) values at the graphene/semiconductor interfaces are 0.86 eV, 0.79 eV, 0.91 eV and 0.73 eV for Si, GaAs, SiC and GaN respectively (Table I). While the overall reverse current density increases as T is increased, we notice that at high reverse bias the magnitude of the breakdown voltage V_b decreases linearly with temperature (see boxed region in upper left hand corner of Fig. 5(b)) implying that V_b has a positive breakdown coefficient and that the junction breakdown mechanism is mainly avalanche multiplication [12].

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| Junction type     | \( \Phi_{SBH} \) | \( \Phi_{SBH} \) | \( N_D \) | \( N_D^{res} \) |
|-------------------|-----------------|-----------------|---------|----------------|
| Graphene/nSi      | 0.86            | 0.92            | 4.0 \times 10^{15} | 3.0 \times 10^{15} | 4.91 |
| Graphene/nGaAs    | 0.79            | 0.91            | 3.5 \times 10^{16} | 3.0 \times 10^{16} | 4.89 |
| Graphene/4H-SiC   | 0.91            | N/A             | N/A     | 1.0 \times 10^{16} | 4.31 |
| Graphene/nGaN     | 0.73            | N/A             | N/A     | 1.0 \times 10^{17} | 4.83 |

FIG. 5: Room temperature current density-voltage characteristics show Schottky rectification at the (a) graphene/n-Si, (b) n-GaAs, (c) n-4H-SiC and (d) n-GaN interfaces. Insets: Semilogarithmic leaf plots, log_{10}J-V, reveal a thermionic emission dominated current density in forward bias that spans at least two decades of linearity (dotted lines) allowing us to extract the Schottky barrier height recorded in Table I.

FIG. 6: (a) The temperature dependence of the current (I) versus voltage (V) curves measured across a graphene/GaAs junction from 250 K up to 320 K with 10 K intervals separating each isotherm. The arrows indicate the direction of increasing temperature. (b) The temperature dependence of I-V curves taken on graphene/GaAs junctions at different temperatures. (c) Extracted \( I_s \) values from Fig. 5(b) are plotted in terms of \( \ln(I_s)/T^2 \) versus 1000/T.

TABLE I: Extracted SBHs, doping densities, and corresponding graphene work function values on various graphene/semiconductor junctions.
of the metals used for contacts, as is found for example in GaAs \[15\]. On the other hand, the wide band gap semiconductors SiC and GaN are well described by the Schottky-Mott (S-M) limit,

$$\phi_{SBH} = \phi_{gr} - \chi_e,$$

(2)

where \(\phi_{gr}\) is the work function of the graphene and \(\chi\) is the electron affinity of the semiconductor. Using the extracted values of \(\phi_{SBH}\), and electron affinity values (\(\chi_{Si} \sim 4.05\ eV, \chi_{GaAs} \sim 4.1\ eV, \chi_{GaH-SiC} \sim 3.4\ eV\) and \(\chi_{GaN} \sim 4.1\ eV\)), we calculate \(\phi_{gr}\) (Table I). The calculated values of the work function are typically higher than the accepted values (\(\sim 4.6\ eV\)) of graphene when \(E_F\) is at the Dirac point (K point). The deviation from this ideal graphene work function can be attributed to the lowering of \(E_F\) due to hole doping of the graphene during the Fe(III)NO\(_3\) etching-transfer process\[19\] (Fig. 2(c-d)) together with the fact that the graphene is in physical contact with the gold electrodes\[20\] (Fig. 4).

Although the SBHs on Si, GaAs and GaN can be roughly explained within the S-M model, in reality GaAs surfaces have a high density of surface states and thus exhibit characteristic Fermi level pinning. In the Bardeen limit, GaAs based diodes generally have SBHs in the range of 0.75-0.85 eV as observed in our measurements, and proper interpretation of the SBH on GaAs/graphene junctions requires the Bardeen model. Subsequent to the placement of the graphene on the semiconductor surface, there is charge separation and concomitant formation of induced dipoles at the interface. According to bond polarization theory\[21, 22\], the SBH is determined by charge separation at the boundary between the outermost layers of the metal (here, a single layer carbon sheet) and the semiconductor. Our results are in good agreement with the findings of our earlier work on graphite and MLG junctions where the layer in closest proximity to the semiconductor surface is a single sheet of carbon atoms\[11, 12\]. On the other hand, barriers formed on the 4H-SiC substrates give an unphysically low value for \(\phi_{gr}\) (see Table I) and therefore cannot be explained by either model.

Next we turn our attention to reverse bias characteristics when the semiconductor (graphene) is positively (negatively) charged. In conventional metal-semiconductor Schottky diodes, the work function of the metal is pinned independent of bias voltage due to the high density of states at \(E_F\) while in the reverse (forward) bias the Fermi energy of the semiconductor shifts down (up) allowing observed rectification via an increase (decrease) in the built-in potential \(V_{bi}\). Unlike conventional metals, graphene’s work function \(\phi_{gr}\) is a function of bias \(V\), and for large voltage values the SBH does not stay constant. When Schottky diodes are forward biased, they pass large currents at voltages well below \(\sim 1\) V and and small decreases in the Fermi level of graphene cannot be distinguished from voltage drops associated with a series resistance. Said in another way, the deviation from linearity in the semilogarithmic plots of Fig. 5(a-d) for forward bias could be due to a combination of a series resistance becoming important at high currents together with a small increase in \(\phi_{gr}\) and a downward shift in \(E_F\) for the positively charged graphene. However, in reverse bias where the applied voltage can be larger than 10 V, \(E_F\) starts changing dramatically\[20\] and the fixed SBH assumption clearly no longer holds. In reverse bias when the graphene electrodes are negatively charged, \(E_F\) increases and \(\phi_{gr}\) decreases causing the SBH height to decrease as the reverse bias is increased. As observed in the insets of Fig. 5(a-d) this effect causes the total reverse current to increase as the magnitude of the bias is increased, thus preventing the Schottky diode from reaching reverse current saturation. This non-saturating reverse current has not been observed in graphite based Schottky junctions due to the fixed Fermi level of graphite\[11\].

D. Capacitance-voltage measurements

Capacitance-voltage \(C-V\) measurements made in the reverse bias mode are complementary to \(J-V\) measurements and provide useful information about the distribution and density \(N_D\) of ionized donors in the semiconductor and the magnitude of the built-in potential \(V_{bi}\). For a uniform distribution of ionized donors within the depletion width of the semiconductor, the Schottky-
Mott relationship between $1/C^2$ and the reverse bias voltage $V_R$, satisfies the linear relationship, $1/C^2 = 2(V_R + V_{bi})/eN_D$, which as shown in Fig. 6(a) is observed to hold for graphene/GaAs and graphene/Si junctions. Linear extrapolation to the intercept with the abscissa gives the built-in potential, $V_{bi}$, which is related to $\phi_{SBH}$ via the expression, $\phi_{SBH} = V_{bi} + e^{-1}k_b T \ln(N_c/N_D)$ [13]. Here $N_c$ is the effective density of states in the conduction band, $N_D$ is the doping level of the semiconductor, and the slope of the linear fitting to $1/C^2$ versus $V_R$ gives the doping density of the semiconductor. We list $\phi_{SBH}^c$ and $N_D$ values for the graphene/GaAs and graphene/Si junctions in Table I.

We note from Table I that the extracted $\phi_{SBH}^c$ values on the Si and GaAs junctions are generally higher than $\phi_{SBH}^c$. The discrepancy between the SBHs determined by the two methods can be attributed to: (a) the existence of a thin oxide or residue at the graphene/semiconductor interface, and/or (b) Schottky barrier inhomogeneity. Graphene sheets transferred onto SiO$_2$ are known to have charge puddles mostly due to the inhomogeneous doping either originating from natural graphite (mechanical exfoliation transfer) or from chemicals used during the graphene production or transfer (CVD graphene transfer process). Since the SBH is sensitive to the $E_F$ of graphene, patches with different charge densities (doping) are expected to have an impact on the SBH and hence the $J$-$V$ characteristics of the graphene diodes.

An important difference between the $C$-$V$ and $J$-$V$ techniques is that the $C$-$V$ measurements probe the average junction capacitance at the interface thereby yielding an average value for the SBH, while the $J$-$V$ measurements give a minimum value for the SBH, since electrons with thermionic emission probabilities exponentially sensitive to barrier heights choose lower barrier patches (less $p$-doped graphene patches) over higher patches (more $p$-doped graphene patches) [22]. While $C$-$V$ measurements give reasonable values of the SBH for graphene/GaAs and graphene/Si, we have not been able to obtain reliable $C$-$V$ measurements for graphene deposited on GaN and SiC because of high series resistance in these wide band gap semiconductors.

The linearity of the $C$-$V$ measurements shown in Fig. 4 is consistent with the Schottky-Mott model and the abrupt junction approximation, which assumes that the density of ionized donors $N_D$ is constant throughout the depletion width of the semiconductor. This good approximation invites a more quantitative analysis of the Fermi energy shifts in the graphene that are the source of the non-saturating reverse bias currents discussed in the previous subsection. We begin by writing the electron charge density per unit area $Q$ on the graphene as

$$Q = e n_{induced} = C_{dep}(V_{bi} + V_R),$$

where

$$C_{dep} = \frac{\epsilon_0 \epsilon_s N_D}{2(V_{bi} + V_R)}.$$  \hspace{1cm} (4)

is the Schottky-Mott depletion capacitance, $n_{induced}$ is the number of electrons per unit area and $V_R$ is the magnitude of the reverse bias voltage. Combining these two equations gives the result,

$$n_{induced} = \sqrt{\epsilon_s \epsilon_0 N_D (V_{bi} + V_R)/2e}.$$  \hspace{1cm} (5)

The above expression provides an estimate of the number of carriers per unit area associated with the electric field within the depletion width but does not account for extrinsic residual doping described by the carrier density $n_0$ on the graphene before making contact with the semiconductor. The processing steps used to transfer the CVD grown graphene from Cu substrates to semiconductor surfaces typically results in $p$-doped material with $n_0 \sim 5 \times 10^{12}$ cm$^{-2}$ as inferred from Hall data (Fig. 4) taken at 300 K. Accordingly, the final carrier density including contributions from the as-made graphene and the charge transfers associated with the Schottky barrier ($V_{bi}$ and the applied voltage $V_R$) reads as,

$$n_{final} = n_0 - n_{induced}.$$  \hspace{1cm} (6)

Using the well-known expression for graphene’s Fermi energy [2] we can write

$$E_F = -\hbar |v_F| k_F = -\hbar |v_F| \sqrt{\pi(n_0 - n_{induced})},$$

which in combination with Eq. 5 becomes

$$E_F = -\hbar |v_F| \sqrt{\pi(n_0 - \sqrt{\epsilon_s \epsilon_0 N_D (V_{bi} + V_R)/2e})},$$  \hspace{1cm} (8)

To calculate typical shifts in $E_F$, we use parameter values $\epsilon_0 = 8.84 \times 10^{-14}$ F/cm$^2$, $\hbar = 6.5 \times 10^{-16}$ eVs, $e = 1.6 \times 10^{-19}$ C, $v_F = 1.1 \times 10^8$ cm/s, $V_{bi} \sim 0.6$ V and $\epsilon_s \sim 10$ for a typical semiconductor. Thus the Fermi energy of the as-made graphene with $n_0 \sim 5 \times 10^{12}$ cm$^{-2}$ is calculated from $E_F = -\hbar |v_F| \sqrt{\pi n_0}$ to be $-0.287$ eV below the charge neutrality point, a shift associated with the aforementioned $p$-doping during processing. When the graphene is transferred to the semiconductor, equilibration of the chemical potentials and concomitant formation of a Schottky barrier (Fig. 4) results in a transfer of negative charge to the graphene and an increase in $E_F$ (calculated from Eq. 8 for $V_R = 0$) to be in the range 3 to 11 meV for $N_D$ in the range $1 \times 10^{16}$ to $1 \times 10^{17}$ cm$^{-3}$. The application of a typical 10 V reverse bias (see Figs. 4 and 6) creates significantly larger Fermi energy shifts which from Eq. 8 give $E_F$ in the range $-0.271$ to $-0.233$ eV for the same factor of ten variation in $N_D$. The corresponding shifts from the pristine value of $-0.287$ eV are in the range 15 - 53 meV and thus bring $E_F$ closer to
the neutrality point. These numerical calculations show that for our $n$-doped semiconductors, it is relatively easy to induce Fermi energy shifts on the order of 50 meV with the application of a sufficiently high reverse bias voltage. An upward shift in $E_F$ of 50 meV causes a reduction in $\Phi_{gr}$ by the same amount. Since the electron affinity of the semiconductor remains unchanged, the Schottky-Mott constraint of Eq. 2 enforces the same reduction in $\phi_{SBH}$ thus leading to a greater than 5% reduction in the measured SBH’s shown in Table I. We note that the induced shift in graphene’s $E_F$ as determined by the in-situ Raman spectroscopy measurements (Fig. 3) is larger ($\Delta E_F \sim 200-500$ meV) than our theoretical estimation ($\Delta E_F \sim 50$ meV).

The discrepancy between the theoretical estimate of $\Delta E_F$ and the experimental values might be attributed to: (1) the existence of an interface capacitance induced by dipoles at the graphene/semiconductor interface (within bond polarization theory) causing deviation from the ideal Schottky-Mott capacitance relation given by Eq. 4 and (2) the estimate of $\Delta E_F$ using relative peak shifts in the G and 2D peak positions for graphene deposited on Si/SiO$_2$ 23 might be different than the change in Fermi level for graphene transferred onto semiconductors.

### E. Modification of thermionic emission theory

As discussed in the previous sections, since the $E_F$ of graphene electrode is sensitive to the applied bias across the graphene/semiconductor interface, the SBH at the interface becomes bias dependent especially for large reverse voltages. However, extracting the SBH from $J$-$V$ characteristics using Eq. 4 which involves extrapolating current density to zero bias saturation current ($J_s$) yields the putative zero bias barrier height (Table 1). In this section, we present a simple modification to the Richardson equation (Eq. 4) considering the shift in $E_F$ of graphene induced by applied bias. The modified Richardson equation preserves the original functional form of Eq. 4 but allows one to estimate the SBH at fixed voltages.

The voltage-dependent SBH ($\Phi_{SBH}(V)$) can be written as,

$$\Phi_{SBH} = \Phi_{SBH}^0 + e\Delta \Phi_{SBH}(V) = \Phi_{SBH}^0 - \Delta E_F(V)$$  

(9)

where $\Phi_{SBH}^0$ is the zero bias SBH and $e\Delta \Phi_{SBH}(V)$ is the correction to the SBH at fixed voltage $V$.

For reverse bias (addition of electrons to the graphene) we use Eq. 5 in Eq. 7 together with the inequality $n_{induced} << n_0$ to calculate

$$e\Delta \Phi_{SBH}(V_R) = -\Delta E_F(V_R) =$$

$$\hbar v_F \left[ \sqrt{ \pi (n_0 - n_{induced}) - \sqrt{\pi n_0} } \right]$$

$$\approx -\frac{1}{2} \hbar v_F \sqrt{ \pi n_0 n_{induced} }$$

$$\approx -\frac{1}{2} \hbar v_F \sqrt{ \frac{\pi e_s e_0 N_D (V_b + V_R)}{2e n_0} }$$

(10)

Adding the reverse and forward current densities as is done in standard treatments of the diode equation 15 yields the total current density across the graphene/semiconductor interface,

$$J(V) =$$

$$A^* T^2 \exp \left( -\frac{e \Phi_{SBH}^0 + e\Delta \Phi_{SBH}(V)}{k_B T} \right) \left[ \exp \left( \frac{eV}{k_B T} \right) - 1 \right]$$

(11)

Here, we note that the original form of the Richardson equation is preserved with slight modifications to the saturation current term which is given as:

$$J_s = A^* T^2 \exp \left( -\frac{e \Phi_{SBH}^0 + e\Delta \Phi_{SBH}(V)}{k_B T} \right)$$

(12)

with $\Delta \Phi_{SBH}(V)$ for reverse bias given by Eq. 10.

In our conventional $J$-$V$ analysis using Eq. 4 the zero-bias saturation current $J_s$ is extracted by extrapolating the current density to zero bias limit. In this limit, the correction to the SBH is expected to be zero, since the graphene is not subject to applied bias and hence the Fermi level does not shift from the original value. However, using the extrapolated zero-bias saturation current density, one can extract the SBH and the correction to the SBH at fixed bias ($V$) can be taken into account by the additional term ($\Delta \Phi_{SBH}(V)$) in Eq. 12.

### CONCLUSION

In summary, we have used current-voltage and capacitance-voltage measurements to characterize the Schottky barriers formed when graphene, a zero-gap semiconductor, is placed in intimate contact with the $n$-type semiconductors: Si, GaAs, GaN and SiC. The good agreement with Schottky-Mott (S-M) physics within the context of bond-polarization theory is somewhat surprising since the S-M picture has been developed for metal-semiconductor interfaces, not for single atomic layer ZGS-semiconductor interfaces discussed here. Moreover, due to a low density of states, graphene’s Fermi level shifts during the charge transfer across the graphene-semiconductor interface. This shift does not occur at metal-semiconductor or graphite-semiconductor interfaces where $E_F$ remains fixed during Schottky barrier
formation and the concomitant creation of a built-in potential, $V_{BI}$, with associated band bending (see Fig. 4). Another major difference becomes apparent when under strong reverse bias. According to our in-situ Raman spectroscopy measurements, large voltages across the graphene/semiconductor interface change the charge density and hence the Fermi level of graphene as determined by relative changes in the G and 2D peak positions. The bias-induced shift in the Fermi energy (and hence the the work function) of the graphene causes significant changes in the diode current. Considering changes in the barrier height associated with bias induced Fermi level shift, we modify the thermionic emission theory allowing us to estimate the change in the barrier height at fixed applied bias. The rectification effects observed on a wide variety of semiconductors suggest a number of applications, such as to sensors where in forward bias there is exponential sensitivity to changes in the SBH due to the presence of absorbates on the graphene or to MESFET and HEMT devices for which Schottky barriers are integral components. Graphene is particularly advantageous in such applications because of its mechanical stability, its resistance to diffusion, its robustness at high temperatures and its demonstrated capability to embrace multiple functionalities.

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