Detection and Elimination of Non-Trivial Reversible Identities

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Abstract

Non-Trivial Reversible Identities (NTRIs) are reversible circuits that have equal inputs and outputs. NTRIs cannot be detected using optimization algorithms in the literature. Existence of NTRIs in a circuit will cause a slow down by increasing the number of gates and the quantum cost. NTRIs might arise due to integration between two or more optimal reversible circuits. In this paper, an algorithm that detects and removes NTRIs in polynomial time will be proposed. Experiments that show the bad effect of NTRIs and the enhancement using the proposed algorithm will be presented.

Keywords: Reversible Computing; Quantum Cost; Boolean Functions; Circuit Optimization.

1 Introduction

Reversible logic [4, 9] is one of the hot areas of research. It has many applications in quantum computation [11, 19], low-power CMOS [7, 6] and many more. Synthesis of reversible circuits cannot be done using conventional ways [24]. Synthesis and optimization of Boolean systems on non-standard computers that promise to do computation more powerfully [23] than classical computers, such as quantum computers, is an essential aim in the exploration of the benefits that may be gain from such systems.

A function is reversible if it maps an input vector to a unique output vector, and vice versa [22], i.e. we can re-generate the input vector from the output vector (reversibility). It is allowed for the inputs to be changed as long as the function maintains reversibility.

A lot of work has been done trying to find an efficient reversible circuit for an arbitrary reversible function. Reversible truth table can be seen as a permutation matrix of size $2^n \times 2^n$. In one of the research directions, it was shown that the process of synthesizing linear reversible circuits can be reduced to a row reduction problem of $n \times n$ non-singular matrix [20]. Standard row reduction methods such as Gaussian elimination and LU-decomposition have been proposed [5]. In another research direction, search algorithms and template matching tools using reversible gates libraries have been used [8, 13, 17, 18]. These will work efficiently for small circuits. A method is given in [12], where a very useful set of transformations for Boolean quantum circuits is shown. In this method, extra auxiliary bits are used in the construction that will increase the hardware cost. In [26], it was shown that there is a direct correspondence between reversible Boolean operations and certain forms of classical logic known as Reed-Muller expansions. This arises the possibility of handling the problem of synthesis and optimization of reversible Boolean logic within the field of Reed-Muller logic. A lot of work has been done trying to find an efficient reversible circuit for an arbitrary multi-output Boolean functions by using templates [13, 15] and data-structure-based optimization [21]. A method to generate an optimal 4-bit reversible circuits has been proposed [10]. In [1], a very useful set of rules for optimizing reversible circuits and sub-circuits with common-target gates has been proposed. Benchmarks for reversible circuits have been established [16].

The aim of the paper is to put a highlight on the problem of non-trivial reversible identities (NTRIs) that might arise during the process of integrating optimal reversible circuits to do more complex tasks. The
existence of a NTRI form a bug in the design that will increase the number of gates and the quantum cost. The paper proposes an algorithm that detects and removes NITRs in polynomial time. The paper is organized as follows. Section 2 gives a short background on reversible gates. Section 3 introduces the problem of NTRIs and gives some examples. Section 4 proposes a polynomial time algorithm to detect and remove NITRs. Section 5 shows the results of the experiments. The paper ends up with a conclusion in Section 6.

2 Background

2.1 Reversible Circuits

In building a reversible circuit with \(n\) variables, an \(n \times n\) reversible circuit will be used. \(C^n\) NOT gate is the main primitive gate that will be used in building the circuit since it was shown to be universal for reversible computation \[24\]. \(C^n\) NOT gate is defined as follows:

**Definition 2.1 \((C^n\) NOT gate)\**

\(C^n\) NOT is a reversible gate denoted as,

\[
C^n\text{NOT}(x_{n-2}, x_{n-2}, \ldots, x_0; f),
\]

with \(n\) inputs: \(x_{n-2}, x_{n-2}, \ldots, x_0\) (known as control bits) and \(f_{in}\) (known as target bit), and \(n\) outputs: \(y_{n-2}, y_{n-2}, \ldots, y_0\) and \(f_{out}\). The operation of the \(C^n\) NOT gate is defined as follows,

\[
y_i = x_i, \text{ for } 0 \leq i \leq n - 2,
\]

\[
f_{out} = f_{in} \oplus x_{n-2}x_{n-3} \ldots x_0,
\]

i.e. the target bit will be flipped if and only if all the control bits are set to 1. Some special cases of the general \(C^n\) NOT gate have their own names, \(C^n\) NOT gate with no control bits is called \(NOT\) gate as shown in Fig. 1b, where the bit will be flipped unconditionally. \(C^n\) NOT gate with one control bit is called \(Feynman\) gate as shown in Fig. 1c. \(C^n\) NOT gate with two control bits is called \(Toffoli\) gate as shown in Fig. 1d. For the sake of readability and to keep consistency with the literature, \(C^0\) NOT, \(C^1\) NOT, \(C^2\) NOT and \(C^3\) NOT will be written for short as \(NOT, CNOT, TOF\) and \(TOF4\) respectively.

2.2 Quantum Cost

*Quantum cost* is a term that appears in the literature and is used to refer to the technological cost of building \(C^n\) NOT gates. The quantum cost of a reversible circuit is subject to optimization as well as the number of \(C^n\) NOT gates used in the circuit. The quantum cost of a \(C^n\) NOT gate is based primarily on the number of bits involved in the gate, i.e. the number of elementary operations required to build the \(C^n\) NOT gate \[3\]. The calculation of the quantum cost for the circuits shown in this paper will be based on the cost table available in \[16\]. The state-of-art shows that both \(NOT(x)\) and \(CNOT(x; f)\) have quantum cost = 1, \(TOF(x_i, x_j; f)\) has a quantum cost = 5, and \(TOF4(x_i, x_j, x_k; f)\) has a quantum cost = 13.
Figure 2: Non-trivial Reversible Identities.

Figure 3: A NTRI before, part-a, and after, part-b, optimization.

3 Non-Trivial Reversible Identities

Circuit identities are usually refer to two or more circuits with the same specification but with different designs [1]. This is usually used to simplify and optimize circuits design [15]. In the context of this paper, reversible identities will refer to circuits that output their input without any change, i.e. do nothing. The existence of reversible identities in a circuit will increase the number of gates and the quantum cost. Reversible identities can be classified as trivial and non-trivial reversible identities.

Trivial reversible identities are those gates that can be easily detected and removed from a reversible circuit. For example, if two adjacent gates are identical then they can be removed due to reversibility. If the same concept is applied recursively on a circuit, many gates can be removed. For example, consider the circuit $CNOT(b, a)TOF(a, b, c)CNOT(c, b)CNOT(c, b)TOF(a, b, c) \equiv CNOT(b, a)$. The two $TOF(a, b, c)$ gates cannot be removed together until the two $CNOT(c, b)$ gates are removed. The problem of detection and removal of trivial reversible identities are not the main target of the paper, although they will be handled inclusively when dealing with non-trivial reversible identities.

Non-trivial reversible identities (NTRIs) are reversible identities that cannot be detected and removed using any known optimization algorithm, for example, [1, 15, 21]. Fig. 2 shows two examples of NTRIs. Applying any known optimization algorithm will report that these designs cannot be optimized further. Fig. 3-a shows another example of NTRI that is slightly optimized using [1] by decreasing the number of gates by one as shown in Fig. 3-b. NTRI must be removed completely from the circuit as they form a bug in the design.

It is important here to differentiate between synthesis and optimization of reversible circuits to show a situation where NTRI might arise as a bug. Synthesis of a reversible circuit is the process of constructing, from scratch, the best design for a given specification. Synthesis process always includes optimization. Optimization of a reversible circuit is the process of enhancing an existing design for a given specification by decreasing the number of gates and/or the quantum cost for a given circuit. NTRI is not likely to occur during the synthesizing process, while NTRI might arise as a problem during the optimization process.

To Design a reversible circuit that does a complex task, it will not be practical to do the synthesis process of that circuit from scratch. Instead, the complex task should be broken down to a set of simple modules, design the optimal form for each module then integrate the optimal designs in a complete design that perform the required task. NTRI might arise during the process of integration. For example, consider the two reversible circuits shown in Fig. 4. These circuits cannot be optimized further using any known optimization algorithm [1]. Consider that these two circuits should be integrated such that circuit in Fig. 4-b should be added to the rear of circuit in Fig. 4-a. The integrated circuit contains 23 gates with quantum cost = 125. No further optimization can be done on the integrated circuit although it is bugged by NTRI in
Figure 4: Two Reversible circuits are required to be integrated such that circuit in part-b should be added to the rear of circuit in part-a.

Figure 5: Circuit in part-a shows the discovered NTRI (the bug) and circuit in part-b shows the final circuit after elimination of the NTRI.

the middle of the integrated circuit. Fig.5a shows the NRTI and Fig.5b shows the circuit with 15 gates and quantum cost = 53 after removing the NTRI. Arrows in Fig.4a and Fig.4b mark the start and the end of the NTRI respectively. In the next section, an algorithm to remove NTRIs in polynomial time will be proposed. It is important to notice that this algorithm is not a substitution for the current optimization algorithms in the literature, this algorithm is recommended to be used as a module with any optimization algorithm.

4 Detection and Elimination of NTRIs

4.1 Data Structures

Consider a finite set $A = \{0, 1, ..., N - 1\}$ and a bijection $\sigma : A \rightarrow A$, then $\sigma$ can be written as,

$$
\sigma = \begin{pmatrix}
0 & 1 & 2 & \cdots & N - 1 \\
\sigma(0) & \sigma(1) & \sigma(2) & \cdots & \sigma(N - 1)
\end{pmatrix},
$$

(3)

i.e. $\sigma$ is a permutation of $A$. Let $A$ be an ordered set, then the top row can be eliminated and $\sigma$ can be written as,

$$
[\sigma(0), \sigma(1), \sigma(2), ..., \sigma(N - 1)].
$$

(4)
Any reversible circuit with \( n \) inputs can be considered as a permutation \( \sigma \) and Eqn.** is the specification of this reversible circuit such that \( N = 2^n \).

In order to detect reversible identities, it is required to store the output of the circuit after applying every gate. Two data structures are used in the proposed algorithm, \( \text{Circuit} \) and \( \text{CurrentSpecs} \). The first data structure, \( \text{Circuit} \), is a one dimensional array of size \( m \), where \( m \) is the number of gates in the reversible circuit. \( \text{Circuit} \) stores the gates of the reversible circuit such that, \( \text{Circuit}[1] \) contains the first gate and \( \text{Circuit}[m] \) contains the last gate.

The second data structure, \( \text{CurrentSpecs} \), is used to store the output specification after applying every gate in the reversible circuit. \( \text{CurrentSpecs} \) is a two dimensional array of size \( N \times m \).

### 4.2 The Algorithm

The outline of the proposed algorithm is as follows: Run the circuit by applying one gate at a time. Store the specification after applying each gate, and compare the current specification at position \( i \) with all the previously stored specifications. If specification at position \( i \) is equal to specification at position \( j \), where \( j < i \), then remove gates from point \( j \) to point \( i \). Repeat the detection until no more reversible identities are found.

**Algorithm 1** Eliminate NTRIs algorithm

```plaintext
procedure ELIMINATEIDENTITIES(Circuit)
    Finish <- false
    while Finish = false do
        Finish <- true
        CurrentCircuit <- nil
        m <- SIZE(Circuit)
        for i <- 1, m do
            CurrentCircuit <- Circuit[i] \( \cup \) CurrentCircuit
            CurrentSpecs[i] <- SPECS(CurrentCircuit)
            for j <- 1, i - 1 do
                if CurrentSpecs[j] = CurrentSpecs[i] then
                    REMOVEGATES(Circuit, j, i)
                    Finish <- false  \( \triangleright \) Finish inner loop early
                    j <- i - 1
                    \( \triangleright \) Finish outer loop early
                    i <- m
                end if
            end for
        end for
    end while
end procedure
```

The correctness of the algorithm is proved as follows. The \textbf{while loop} from Line:3 to Line:19 will repeat until no more reversible identities exist in \( \text{Circuit} \). The \textbf{for loop} from Line:7 to Line:18 traces \( \text{Circuit} \) one gate at a time and stores the circuit from gate 0 to gate \( i \) in \( \text{CurrentCircuit} \). \( \text{CurrentSpecs}[i] \) stores the specification for the circuit at point \( i \). The \textbf{for loop} from Line:10 to Line:17 checks if there exist any reversible identity by comparing specification of point \( i \) with specification of point \( j \) such that \( 1 \leq j < i \). At Line:11, if an identity is found, then gates from point \( j \) to point \( i \) is removed from \( \text{Circuit} \), and the algorithm starts all over again looking for more reversible identities.

The best case running time exists when no identities exist in \( \text{Circuit} \) where the \textbf{while loop} from Line:3 to Line:19 will run once so the algorithm has \( \Theta(m^2) \). The worst case running time exists when \( \text{Circuit} \) contains gates such that every two adjacent gates are identical where the \textbf{while loop} will repeat \( m/2 \) times, so the algorithm has \( \Theta(m^3) \). The proposed algorithm can detect and eliminate identities from the reversible circuit in polynomial time.
| Benchmark | Optimal Circuit | Random Identity | Insertion Pt. | Optimal \((g,c)\) | Bugged \((g,c)\) | Optimized \((g,c)\) |
|-----------|----------------|-----------------|--------------|----------------|----------------|----------------|
| 4,49      | APP1.1.a       | APP1.1.b        | 0            | (12,42)        | (19,61)        | (19,61)        |
| 4bit-7-8  | APP1.2.a       | APP1.2.b        | 5            | (7,19)         | (14,40)        | (12,34)        |
| decoded42 | APP1.3.a       | APP1.3.b        | 4            | (10,30)        | (16,52)        | (15,54)        |
| hwb4      | APP1.4.a       | APP1.4.b        | 7            | (11,39)        | (16,64)        | (16,62)        |
| imark     | APP1.5.a       | APP1.5.b        | 3            | (7,19)         | (17,43)        | (11,37)        |
| mperk     | APP1.6.a       | APP1.6.b        | 4            | (9,16)         | (22,52)        | (22,52)        |
| oc5       | APP1.7.a       | APP1.7.b        | 2            | (11,39)        | (23,66)        | (16,52)        |
| oc6       | APP1.8.a       | APP1.8.b        | 11           | (12,60)        | (20,74)        | (20,74)        |
| oc7       | APP1.9.a       | APP1.9.a        | 13           | (13,41)        | (29,219)       | (28,207)       |
| oc8       | APP1.10.a      | APP1.10.b       | 9            | (11,47)        | (25,197)       | (15,79)        |
| primes4   | APP1.11.a      | APP1.11.b       | 4            | (10,42)        | (18,98)        | (13,77)        |
| rd32      | APP1.12.a      | APP1.12.b       | 3            | (4,8)          | (10,54)        | (8,46)         |
| shift4    | APP1.13.a      | APP1.13.b       | 4            | (4,18)         | (20,146)       | (13,101)       |

Table 1: Optimal 4-bits reversible circuits from [10] bugged by random NTRIs and optimized using [1], where the pair \((g,c)\) represents the number of gates \((g)\) and the quantum cost \((c)\).

5 Experimental Results

Based on literature review, no method proposed the problem of NTRIs so far. To test the effect of NTRIs on the optimization of reversible circuits. Two software’s have been developed. The first generates random reversible circuits with NTRIs and the second generates random NTRIs. Experiments are based on 4-bits reversible circuits as a prototype.

The first experiment is done by inserting a random NTRI in a randomly chosen insertion point in the middle of optimal 4-bits reversible circuits [10]. Then the latest optimization method [1] using [2] is applied to test the effect of the NTRI on the final number of gates and the quantum cost of the circuit. Table 1 shows the results of the experiment where NTRIs affect the number of gates and the quantum cost. Applying Algorithm 1 before [1] gives the optimal results. Circuits used in the experiment are shown in Appendix 1.

The second experiment is used to test Algorithm 1 by generating random reversible circuits and checking the number of gates and the quantum cost in the following cases: (1) before applying any method, (2) after applying [1], (3) after applying the proposed method then [1]. Table 2 shows the results of the experiment with a better result using the proposed algorithm. Circuits used in the experiment are shown in Appendix 2.

6 Conclusion

Non-trivial reversible identities (NTRIs) are bugs that might arise in integrated reversible circuits to cause a slow down, increase in the number of gates and the quantum cost of the integrated circuits. A polynomial time algorithm is proposed to detect and eliminate NTRIs. The proposed algorithm is not a substitution of any optimization algorithm in the literature. The paper recommends the proposed algorithm to be used together with any optimization algorithm to handle the problem of NTRIs.
Table 2: Random reversible circuits with NTRIs optimized using [1] alone and optimized using a hybrid system from the proposed algorithm and [11], where the pair \((g, c)\) represents the number of gates \((g)\) and the quantum cost \((c)\).

| Specification | Random Circuit | Original \((g,c)\) | Optimized \((g,c)\) | Optimized + NTRIs Removal \((g,c)\) |
|---------------|----------------|-------------------|-------------------|-------------------------------|
| \([12,7,2,5,0,15,14,11,6,3,10,1,8,9,4,13]\) | APP2.1         | (21,113)          | (17,103)          | (10,30)                       |
| \([7,14,9,6,11,0,13,2,5,15,10,12,1,4,3,8]\) | APP2.2         | (30,210)          | (30,204)          | (18,102)                      |
| \([10,15,0,7,14,9,6,1,13,12,5,3,11,8,4,2]\) | APP2.3         | (23,103)          | (23,101)          | (13,43)                       |
| \([12,9,11,14,6,7,8,10,2,3,4,5,15,13,0,1]\) | APP2.4         | (22,90)           | (22,90)           | (9,30)                        |
| \([0,1,15,8,4,5,9,14,11,12,7,6,3,13,10,2]\) | APP2.5         | (23,137)          | (19,105)          | (10,50)                       |
| \([3,0,1,6,7,2,5,4,11,8,9,14,15,10,13,12]\) | APP2.6         | (25,133)          | (19,90)           | (6,14)                        |
| \([6,11,5,4,2,0,1,15,14,3,12,8,7,9,13,10]\) | APP2.7         | (21,137)          | (20,132)          | (15,59)                       |
| \([12,15,5,8,3,2,1,10,7,14,13,6,11,9,0,4]\) | APP2.8         | (23,125)          | (23,125)          | (15,53)                       |
| \([0,1,6,5,7,8,15,2,14,13,12,3,11,4,9,10]\) | APP2.9         | (17,65)           | (16,64)           | (11,47)                       |
| \([0,10,2,15,8,9,4,1,6,5,14,3,12,13,11,7]\) | APP2.10        | (20,80)           | (19,75)           | (13,57)                       |
| \([8,9,10,2,4,7,6,5,0,15,3,12,14,1,11]\) | APP2.11        | (21,93)           | (21,93)           | (12,80)                       |
| \([6,15,0,19,2,7,4,11,10,5,12,3,14,13,8]\) | APP2.12        | (29,73)           | (29,73)           | (17,53)                       |
| \([9,3,10,11,12,13,1,7,0,8,14,2,15,4,5,6]\) | APP2.13        | (25,81)           | (17,69)           | (12,52)                       |

References

[1] M. Arabzadeh and M. Saeedi and M. S. Zamani. Rule-based optimization of reversible circuits. In Proceedings of The 15th Asia and South Pacific Design Automation Conference (ASPDAC), pages. 849 - 854, 2010.

[2] M. Arabzadeh and M. Saeedi. RCVviewer+, version 1.87, 2010, available at http://ceit.aut.ac.ir/QDA/RCV.htm

[3] A. Barenco, C. H. Bennett, R. Cleve, D. P. DiVincenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter. Elementary gates for quantum computation. Phys. Rev. A, 52(5):3457–3467, Nov 1995.

[4] C. Bennett. Logical reversibility of computation. IBM Journal of Research and Development, 17(6):525–532, 1973.

[5] T. Beth and M. Roetteler. Quantum algorithms: Applicable algebra and quantum physics. In Quantum Information, pages 96–150. Springer, 2001.

[6] A. De Vos, B. Desoete, A. Adamski, P. Pietrzak, M. Sibinski, and T. Widerski. Design of reversible logic circuits by means of control gates. In Proceedings of the 10th International Workshop on Integrated Circuit Design, Power and Timing Modeling, Optimization and Simulation, pages 255-264, 2000.

[7] A. De Vos, B. Desoete, F. Janiak, and A. Nogawski. Control gates as building blocks for reversible computers. In Proceedings of the 11th International Workshop on Power and Timing Modeling, Optimization and Simulation, pages 9201–9210, 2001.
[8] G. W. Dueck and D. Maslov. Reversible function synthesis with minimum garbage outputs. In Proceedings of the 6th International Symposium on Representations and Methodology of Future Computing Technologies, pages 154–161, 2003.

[9] E. Fredkin and T. Toffoli. Conservative logic. International Journal of Theoretical Physics, 21:219–253, 1982.

[10] O. Golubitsky and S.M. Falconer and D. Maslov. Synthesis of the optimal 4-bit reversible circuits. In Proceedings of the 47th Design Automation Conference, pages 653-656, 2010.

[11] J. Gruska. Quantum Computing. McGraw-Hill, London, 1999.

[12] K. Iwama, Y. Kambayashi, and S. Yamashita. Transformation rules for designing CNOT–based quantum circuits. In Proceedings of the 39th Conference on Design Automation, pages 419–424. ACM Press, 2002.

[13] D. Maslov, G. W. Dueck, and D. M. Miller. Fredkin/Toffoli templates for reversible logic synthesis. In Proceedings of the ACM/IEEE International Conference on Computer-Aided Design, page 256, 2003.

[14] D. Maslov, G. W. Dueck, and D. M. Miller. Simplification of Toffoli networks via templates. In Proceedings of the 16th Symposium on Integrated Circuits and Systems Design, page 53, 2003.

[15] D. Maslov and C. Young and D. M. Miller and G. W. Dueck. Quantum circuit simplification using templates. Design, Automation and Test in Europe, pages 1208-1213, 2005.

[16] D. Maslov. Reversible logic synthesis benchmarks. [Online]. Available: http://www.cs.uvic.ca/~dmaslov/

[17] D. M. Miller and G. W. Dueck. Spectral techniques for reversible logic synthesis. In Proceedings of the 6th International Symposium on Representations and Methodology of Future Computing Technologies, pages 56–62, 2003.

[18] D. M. Miller, D. Maslov, and G. W. Dueck. A transformation based algorithm for reversible logic synthesis. In Proceedings of the 40th Conference on Design Automation, pages 318–323, 2003.

[19] M. Nielsen and I. Chuang. Quantum Computation and Quantum Information. Cambridge University Press, Cambridge, United Kingdom, 2000.

[20] K. N. Patel, I. L. Markov, and J. P. Hayes. Efficient synthesis of linear reversible circuits. arXiv e-Print quant-ph/0302002, 2003.

[21] A. K. Prasad and V. V. Shende and K. N. Patel and I. L. Markov and J. P. Hayes. Data structures and algorithms for simplifying reversible circuits. J. Emerg. Technol. Comput. Syst., 2(4), October 2006.

[22] V. Shende, A. Prasad, I. Markov, and J. Hayes. Reversible logic circuit synthesis. In Proceedings of ACM/IEEE International Conference on Computer-Aided Design, pages 353–360, 2002.

[23] D. Simon. On the power of quantum computation. In Proceedings of the 35th Annual Symposium on Foundations of Computer Science, pages 116–123, 1994.

[24] T. Toffoli. Reversible computing. In W. de Bakker and J. van Leeuwen, editors, Automata, Languages and Programming, page 632. Springer, New York, 1980. Technical Memo MIT/LCS/TM-151, MIT Lab for Computer Science (unpublished).

[25] B. C. Travaglione, M. A. Nielsen, H. M. Wiseman, and A. Ambainis. ROM-based computation: quantum versus classical. arXiv e-Print quant-ph/0109010, 2001.

[26] A. Younes and J. Miller. Representation of Boolean quantum circuits as Reed-Muller expansions. International Journal of Electronics, 91(7):431–444, 2004.
A Appendix 1

Circuits used in the first experiment where "#" shows the insertion point of the NTRI bug.

APP1.1.a
\[ \text{NOT}(a) \text{ CNOT}(c, a) \text{ CNOT}(a, d) \text{ TOF}(a, b, d) \text{ CNOT}(d, a) \# \text{ TOF}(c, d, b) \text{ TOF}(a, d, c) \text{ TOF}(b, c, a) \text{ TOF}(a, b, d) \text{ NOT}(a) \text{ CNOT}(d, b) \text{ CNOT}(d, c) \]

APP1.1.b
\[ \text{TOF}(b, d, c) \text{ CNOT}(c, a) \text{ CNOT}(d, c) \text{ CNOT}(d, a) \# \text{ CNOT}(c, d) \text{ CNOT}(d, b) \text{ CNOT}(d, a) \]

APP1.2.a
\[ \text{CNOT}(d, b) \text{ CNOT}(d, a) \text{ CNOT}(c, d) \text{ TOF}(a, b, d, c) \text{ CNOT}(d, a) \text{ TOF}(a, b, d, c) \text{ CNOT}(c, a) \text{ CNOT}(a, b) \text{ NOT}(a) \]

APP1.2.b
\[ \text{CNOT}(d, b) \text{ TOF}(a, d, c) \text{ CNOT}(c, a) \text{ TOF}(a, d, b) \text{ CNOT}(d, a) \text{ CNOT}(d, b) \text{ CNOT}(c, a) \text{ TOF}(a, d, c) \text{ TOF}(c, d, b) \]

APP1.3.a
\[ \text{CNOT}(b, d) \text{ CNOT}(d, a) \text{ CNOT}(c, d) \text{ TOF}(a, b, d, c) \# \text{ CNOT}(c, d) \text{ CNOT}(d, b) \text{ CNOT}(d, a) \]

APP1.3.b
\[ \text{TOF}(b, d, a) \text{ CNOT}(d, b) \text{ TOF}(c, d, b) \text{ TOF}(c, d, a) \text{ TOF}(b, d, a) \text{ TOF}(c, d, b) \]

APP1.4.a
\[ \text{CNOT}(b, d) \text{ CNOT}(d, a) \text{ CNOT}(a, c) \text{ TOF}(b, c, d, a) \text{ CNOT}(d, a) \text{ TOF}(a, c, b) \# \text{ TOF}(b, c, d, a) \text{ CNOT}(d, c) \text{ CNOT}(a, c) \text{ CNOT}(b, d) \]

APP1.4.b
\[ \text{TOF}(c, d, b) \text{ TOF}(a, d, c) \text{ TOF}(a, d, b) \text{ TOF}(c, d, b) \text{ TOF}(a, d, c) \]

APP1.5.a
\[ \text{TOF}(c, d, a) \text{ TOF}(a, b, d) \text{ CNOT}(d, c) \text{ CNOT}(b, c) \# \text{ CNOT}(d, a) \text{ TOF}(a, c, b) \text{ NOT}(c) \]

APP1.5.b
\[ \text{TOF}(a, d, b) \text{ CNOT}(c, a) \text{ CNOT}(d, a) \text{ CNOT}(d, a) \text{ CNOT}(d, b) \text{ TOF}(c, d, b) \text{ TOF}(a, d, b) \]

APP1.6.a
\[ \text{NOT}(c) \text{ CNOT}(d, c) \text{ TOF}(c, d, b) \# \text{ TOF}(a, c, d) \text{ CNOT}(d, b) \text{ CNOT}(d, a) \text{ CNOT}(c, a) \text{ CNOT}(a, b) \text{ CNOT}(b, c) \]

APP1.6.b
\[ \text{CNOT}(d, b) \text{ CNOT}(d, a) \text{ CNOT}(c, a) \text{ CNOT}(d, b) \text{ CNOT}(d, a) \text{ TOF}(a, d, b) \text{ TOF}(c, d, a) \text{ CNOT}(d, a) \text{ CNOT}(d, b) \text{ TOF}(c, d, a) \]

APP1.7.a
\[ \text{TOF}(b, d, c) \# \text{ TOF}(c, d, b) \text{ TOF}(a, b, c) \text{ NOT}(a) \text{ CNOT}(d, b) \text{ CNOT}(a, c) \text{ TOF}(b, c, d) \text{ CNOT}(a, b) \text{ CNOT}(c, a) \text{ CNOT}(a, c) \text{ TOF}(a, b, c) \]

APP1.7.b
\[ \text{CNOT}(d, b) \text{ CNOT}(c, a) \text{ CNOT}(d, a) \text{ CNOT}(c, a) \text{ CNOT}(d, b) \text{ TOF}(c, d, a) \text{ CNOT}(d, a) \text{ TOF}(c, d, b) \text{ TOF}(c, d, b) \text{ TOF}(c, d, a) \text{ CNOT}(d, b) \]
APP1.8.a
TOF(4, b, c, d, a) TOF(4, a, c, d, b) CNOT(d, c) TOF(b, c, d) TOF(c, d, a) TOF(4, a, b, d, c) NOT(a) NOT(a) CNOT(b, a) CNOT(b, d, c) NOT(b, d, c) CNOT(b, a) TOF(b, c, d) CNOT(c, b) CNOT(d, c) CNOT(a, d) # TOF(b, d, c)

APP1.8.b
TOF(c, d, a) CNOT(c, a) CNOT(d, b) TOF(c, d, a) CNOT(d, a) CNOT(d, a) CNOT(c, a) CNOT(d, b)

APP1.9.a
TOF(b, d, c) TOF(a, b, d) CNOT(b, a) TOF(4, a, c, d, b) CNOT(c, b) CNOT(d, c) TOF(a, c, d) NOT(b) NOT(d) CNOT(b, c) TOF(b, a, d) TOF(a, c, d) # CNOT(c, a)

APP1.9.a
TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c)

APP1.10.a
CNOT(d, a) TOF(b, c, a) TOF(c, d, b) TOF(4, a, b, d, c) TOF(4, a, b, d) TOF(4, a, b, d) NOT(a) NOT(b) TOF(b, a, d) # CNOT(a, d) TOF(b, c, d)

APP1.10.b
TOF(a, d, b) TOF(a, d, b) TOF(4, a, c, d, b) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c)

APP1.11.a
CNOT(d, c) CNOT(c, a) CNOT(d, b) # NOT(b) TOF(b, c, d) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(4, a, b, d, c) TOF(b, d, c) TOF(a, c, b) CNOT(c, d)

APP1.11.b
TOF(a, c, b) TOF(4, a, c, d, b) TOF(a, d, b) TOF(b, d, a) TOF(b, d, a) TOF(a, d, b) TOF(a, c, b)

APP1.12.a
TOF(a, b, d) CNOT(a, b) # TOF(b, c, d) CNOT(b, c)

APP1.12.b
TOF(c, d, b) TOF(4, a, c, d, b) TOF(a, d, b) TOF(a, d, b) TOF(4, a, c, d, b) TOF(4, a, b, d, c) TOF(b, d, c) TOF(4, a, c, d, b) TOF(b, d, c) TOF(a, d, b) TOF(b, d, c) TOF(a, d, b) TOF(4, a, c, d, b) TOF(4, a, c, d, b) TOF(4, a, b, d, c)

APP1.13.a
TOF(4, a, b, c, d) TOF(a, b, c) CNOT(a, b) # NOT(a)

APP1.13.b
TOF(a, d, b) TOF(b, d, c) TOF(a, d, b) TOF(a, d, b) TOF(4, a, c, d, b) TOF(4, a, b, d, c) TOF(b, d, c) TOF(4, a, c, d, b) TOF(b, d, c) TOF(a, d, b) TOF(b, d, c) TOF(a, d, b) TOF(4, a, c, d, b) TOF(4, a, b, d, c)

B Appendix 2
Circuits used in the second experiment where [...] shows the NTRI discovered by the proposed algorithm.

APP2.1
CNOT(b, c) NOT(b) TOF(4, a, b, c, d) CNOT(a, b) TOF(a, d, b) TOF(b, d, c) TOF(4, a, c, d, b) TOF(4, a, b, d, c) TOF(b, d, c) TOF(a, d, b) TOF(b, d, c) TOF(4, a, b, c, d) CNOT(a, d) TOF(a, b, d) NOT(b) TOF(a, b, c) NOT(c) TOF(c, d, b) CNOT(c, d)
APP2.13

CNOT(c, a) TOF(b, d, a) NOT(c) TOF(a, c, d) TOF(a, b, c) TOF4(a, b, d, c) TOF(b, d, a) CNOT(d, a) CNOT(b, d)
[CNOT(d, c) TOF(b, d, a) CNOT(d, c) TOF(b, c, a) CNOT(d, c) TOF(b, c, a) CNOT(d, c) ]NOT(a) NOT(d) TOF(a, b, d)
TOF(b, c, a) NOT(d) TOF(a, d, b) NOT(c) NOT(d) TOF(b, c, d)