Experimental Determination of Interface Trap Density and Fixed Positive Oxide charge in Commercial 4H-SiC Power MOSFETs

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This work was supported in part by the block gift grant from II-VI Foundation GR123525.

ABSTRACT We measure interface trap density near the conduction band edge and fixed oxide charge in commercial, packaged, 4H-SiC 1.2 kV planar Power MOSFETs. These traps determine the device threshold voltage, performance, and reliability. The subthreshold slope is used to extract interface trap density at the SiO2-SiC interface near the conduction band edge from three vendors, which varies from $5.8 \times 10^{12}$ to $9.3 \times 10^{12}$ cm$^{-2}$·eV$^{-1}$. Good agreement is obtained with threshold voltage measurements from 25°C to 150°C as devices with the highest interface trap densities exhibit the largest threshold voltage reduction over temperature. Fixed positive oxide charge, $N_{ox}$, balanced with interface traps and substrate doping, varies from $3.3 \times 10^{12}$ cm$^{-2}$ to $3.7 \times 10^{12}$ cm$^{-2}$. At high temperatures, electrons captured in interface traps emit to the conduction band and lower the threshold voltage together with fixed oxide charges, which are as high as interface trap densities. Thus, device design should be considered for a suitable threshold voltage to ensure the device does not operate in a Normally-ON condition and to protect against gate voltage surges. Therefore, more focus on characterization and reduction of the interface trap density and fixed oxide charge is needed to enable further improvement in effective electron mobility of SiC MOSFETs.

INDEX TERMS Silicon carbide (SiC), power MOSFET, oxide reliability, interface trap density, oxide charge, subthreshold slope, threshold voltage

I. INTRODUCTION SiC Power MOSFETs are efficient switching devices with low switching losses and high-power density over an extended temperature range [1]-[3]. SiC, similar to Si, uses thermally grown silicon dioxide (SiO2) as a native oxide. However, the gate oxide of SiC MOSFETs exhibits a higher density of trapped charges at or near the SiC-SiO2 interface. The high density of electrons in the interface traps ($D_{it}$) near the conduction band edge, along with fixed positive charges, $N_{ox}$, near the SiC-SiO2 interface create a design challenge for threshold voltage and cause reduced electron density in the conduction band. Furthermore, scattering of electrons in the channel results in a low effective electron mobility, a reduced current drive, and an increase in channel and ON resistance [4]-[7]. Post-oxidation annealing (POA) techniques with nitric oxide (NO), nitrous oxide (N2O), phosphosilicate glass (PSG), and phosphorus oxychloride (POCl3) have been employed to improve gate oxide quality and increase inversion electron mobility by passivating the SiC-SiO2 interface [8]-[16]. Recently, Kobayashi et al. [17] and Takichi et al. [18] have reported new approaches to reduce $D_{it}$ and improve effective mobility by preventing oxidation of SiC during gate oxide formation.

The combination of extremely low intrinsic carrier density combined with p-well doping places the Fermi level near the conduction band edge in strong inversion, where the high values of $D_{it}$ affects the threshold voltage and device reliability. The issues arising from the high $D_{it}$ become complex when devices with dissimilar $D_{it}$ operate at elevated temperature. Electrons trapped by interface traps emit back into the conduction band. This results in an uneven threshold voltage reduction and current drive. In a power module, where multiple devices are connected in parallel to share the current, the uneven threshold voltage reduction in paralleled devices results in uneven current sharing. The nonuniform current sharing can affect the long-term reliability of power modules. Even with reduction of $D_{it}$, the electron mobility is degraded by the scattering from the high density of fixed...
positive charges near the SiC-SiO₂ interface. Although the origin of oxide charge has not been determined, a SiC-SiO₂ transition layer with carbon clusters formed during the thermal oxidation process may be responsible for the donor-like defects [19]-[22].

In our work, we determine \( D_N \) and \( N_{ox} \) in commercially available 1.2 kV SiC Power MOSFETs. Transfer current-voltage (I-V) characteristics in the subthreshold region are used to extract the \( D_N \) near the SiC conduction band edge, which are confirmed with high temperature measurements of the device threshold voltage. We extract \( N_{ox} \) for an assumed p-well doping density.

II. EXTRACTION METHOD FOR \( D_{it} \)

In order to examine the trap density at the interface of SiO₂-SiC, we use the subthreshold characteristics. This permits the extraction of energy-dependent trap density by incorporating the surface potential derived from the subthreshold characteristics. We begin with the drain current in the subthreshold region [23], [24]

\[
I_{DS} = I_0 e^{qV_{GS}/nkT} (1 - e^{-qV_{DS}/kT}) = I_{DM} e^{\phi_S/kT} \tag{1}
\]

where \( I_0 \) is the current at \( V_{GS} = 0 \) and \( V_{DS} \gg kT/q \). \( I_{DM} \) is the maximum drain current at zero surface potential \((\phi_S = 0)\) which incorporates \( V_{DS} \). The ideality factor \( n \) is given as

\[
n = \frac{q}{2.3kT} \left( \frac{\partial I_{DS}}{\partial V_{GS}} \right)^{-1} = \frac{dV_{GS}}{d\phi_S} = 1 + \frac{C_D + C_a}{C_{ox}} \tag{2}
\]

where \( C_D \) is the depletion capacitance, \( C_a \) is the oxide capacitance and \( C_a \) is the interface trap capacitance per unit area with the interface trap density

\[
D_{it}(\phi_S) = \frac{C_a}{q} \tag{3}
\]

In practice, \( D_N \) is extracted at several gate voltages, as a function of surface potential, within the subthreshold region. Fig. 1 shows the energy band diagram under weak inversion where the Fermi level \((E_F)\) is slightly above the intrinsic Fermi level at the surface \((E_S)\).

The traps in the range \( E_F - E_S \) are filled with electrons and this range extends as the applied gate voltage increases to bring \( E_F \) closer to the conduction band at the surface, \( E_S \). The onset of inversion at \( \phi_S = 2\phi_F \) places the \( E_F \) near the edge of \( E_S \), where there is an increasing density of interface traps. The amount of the interface charge varies as the surface potential changes with the gate voltage. The surface potential is related to trap level, \( E_D \), by the following expression:

\[
E_{CS} - E_{TO} = \frac{E_g}{2} - q(\phi_S - \phi_F) \tag{4}
\]

where \( \phi_F \) is the Fermi potential. Both \( \phi_S \) and \( \phi_F \) are positive quantities in (4). The drain current value at a certain gate voltage at a fixed value of \( V_{DS} \) can be expressed as the last term in (1). The threshold voltage is set at \( \phi_S = 2\phi_F \) in (1), such that

\[
I_{DS}(2\phi_F) = I_{DM} e^{2\phi_F/kT} \tag{5}
\]

Combining (1) and (5) leads to \( \phi_S \) with the current level \( I_{DS}(\phi_S) \) measured at a certain gate voltage as

\[
\phi_S = 2\phi_F - 2.3kT \log \left[ \frac{I_{DS}(2\phi_F)}{I_{DS}(\phi_S)} \right] \tag{6}
\]

where the surface potential is in the range \( \phi_F < \phi_S < 2\phi_F \). \( I_{DS}(2\phi_F) \) is the drain current at threshold voltage which is determined by the linear extrapolation method from the measurement data. Finally, from (4) and (6), \( E_{CS} - E_{TO} \) is expressed as a function of surface potential:

\[
E_{CS} - E_{TO} = \frac{E_g}{2} - q \left( \phi_F - 2.3kT \log \left[ \frac{I_{DS}(2\phi_F)}{I_{DS}(\phi_S)} \right] \right) \tag{7}
\]

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. INTERFACE TRAP DENSITY DISTRIBUTION EXTRATION

We examine commercial SiC planar power MOSFETs. The devices under test (DUTs) are from three vendors, referred to as C, D, and E, which are rated at 1.2 kV and 7 – 12 A. Five devices from each vendor are selected with threshold voltage variation less than 0.05 V. All the electrical characterizations are performed with a Keysight B1505A analyzer. Fig. 2 shows \( I_{DS}-V_{GS} \) characteristics with a drain voltage of 0.1 V at room temperature. Threshold voltage at \( \phi_S = 2\phi_F \) is determined by a linear extrapolation (LE) method [25]. From the subthreshold curves, the ideality factors \( n \) can be determined with (2) as a function of \( V_{GS} \). Several gate voltages are selected in the subthreshold region. \( D_N \), as a function of trap energy, is obtained with (3) and (7). To determine \( C_{ox} \), oxide thicknesses are estimated by voltage ramp-to-breakdown measurements at room temperature as shown in Fig. 3. With an oxide breakdown field of 11 MV/cm [26, 27], DUT oxide thickness, from vendors C, D, and E, are 456, 452, and 389 Å, respectively. A p-type base doping concentration, \( N_A = 2\times10^{17} \) cm\(^{-3}\) has been assumed for all samples.
FIGURE 2. $I_{ds}$-$V_{gs}$ transfer characteristics at room temperature.

FIGURE 3. Voltage ramp-to-breakdown (V-ramp) measurements on DUTs.

Fig. 4 shows a sensitivity analysis of the extraction of interface trap density with varying p-base doping concentrations and oxide breakdown fields which affect the estimated gate oxide thickness. A small error can be incurred with this method since the p-base doping profile is not known for each vendor. $D_I$ distributions of devices from vendors C, D and E are shown in Fig. 5. For each vendor, $D_I$ distributions of five devices are overlapped which shows a small deviation across the devices from the same vendor. The $D_I$ increases exponentially near the conduction band edge. The channel electrons are captured and scattered by these interface traps during device operation and their effective mobility is reduced, which decreases the drive current since SiC Power MOSFETs operate in the region $E_{CS} - E_{TO} \leq 0.1 \text{ eV}$, where $D_I$ is high. At $E_{CS} - E_{TO} \approx 0.1 \text{ eV}$, where inversion occurs, the average $D_I$ values from the vendors C, D and E are $9.3 \times 10^{12}$, $6.8 \times 10^{12}$, and $5.8 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$, respectively. Vendors D and E might have very similar interface trap distribution since there can be a variation in p-well doping concentrations whereas vendor C appears to be quite different even at deeper energy levels.

The post oxidation anneal (POA) of the gate oxide plays a role in determining the $D_I$. Studies on the SiO$_2$-SiC interface demonstrate N$_2$O and NO anneal work best for the Si-face of 4H-SiC, which has been used in industry [28], [29]. N$_2$O and NO treated MOS capacitors, compared with simply oxidized MOS capacitors, exhibited approximately 83 percent and 90 percent lower $D_I$ at 0.1 eV below the conduction band, respectively [29]. Our $D_I$ values are higher than reported...
values in [29] since the DUTs are commercial MOSFETs with heavily implanted Al p-base regions.

B. TEMPERATURE-DEPENDENT THRESHOLD VOLTAGE

Threshold voltages are measured as a function of temperature in order to study the performance of DUTs with different Dit values at high temperature. The devices were placed in an oven and measured at 25°C intervals from room temperature to 150°C. IDS-VGS transfer characteristics as a function of temperature are shown in Fig. 6 (a). As the temperature increases, the curves shift in the negative direction in all samples. Noticeable difference in subthreshold characteristics between vendors is observed. Subthreshold swing (SS) which is the inverse slope of the log (IDS) versus VGS in the subthreshold region, is a simple indicator for Dit, as shown in (2) and (3).

Generally, the SS is higher in devices with larger Dit, which shows a gradual subthreshold slope. Fig. 6 (a) shows devices from vendor C present gradual subthreshold slopes with larger shift in IDS-VGS curve over the given temperature range. Whereas subthreshold slopes of devices from vendor E are steep and shift over the temperature is smaller. This indicates devices from vendor C have higher Dit. Vendor D is not shown for clarity but is located between the two vendors with medium subthreshold slope. Fig. 6 (b) shows the threshold voltage reduction with temperature. Devices from vendor C show the largest variation in threshold voltage with the temperature change as expected from the variation in I-V curves in Fig. 6 (a). High threshold voltage at 150°C for vendor C may be seen as an advantage from the point of view of safe operation of the circuit.

When threshold voltage at room temperature is taken as a reference, the threshold voltage reductions at 150°C in devices from vendors C, D, and E are 3.4 V, 2.6 V, and 1.7 V, respectively. The threshold voltage reduction at high temperature is primarily due to release of trapped electrons in interface states to the conduction band. The threshold voltage is defined as

\[ V_{TH} = \phi_{GS} + 2\phi_F + \frac{\sqrt{4\varepsilon_s qN_i\phi_F}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} - \frac{Q_F}{C_{ox}} \] (8)

Consequently, the less negative charges in the interface traps and more carriers in the conduction band result in threshold voltage reduction. Threshold voltage reduction from room temperature to 150°C, \( \Delta V_{TH} \), can be described as

\[ \Delta V_{TH} = \frac{\Delta Q_{it}}{C_{ox}} \] (9)

where variations in \( Q_F \) with temperature is assumed to be small. The first three terms in (8) involve temperature changes due to \( \phi_F \) and bandgap narrowing and amount to threshold voltage reduction of only 0.19 V, 0.19 V, and 0.18 V for vendors C, D, and E, respectively. Thus, the threshold voltage shift in experimental data is assumed to largely come from the emission of trapped charges in interface states. Interface traps per unit area, \( \Delta N_{it} \), can be expressed as

\[ \Delta N_{it} = \int_{\phi_{F,RT}}^{\phi_{F,HT}} D_{it}(\phi_F)d\phi_F \] (10)

where the threshold voltage is determined at \( \phi_S = 2\phi_F \). The Fermi potential change (\( \Delta \phi_F \)) from room temperature (\( \phi_{F,RT} \)) to 150°C (\( \phi_{F,HT} \)) is depicted in Fig. 7 (a) [30]. At elevated temperature, \( E_F \) is closer to the \( E_i \) at the bulk due to increasing intrinsic carrier density. Therefore, less band bending is required to induce a sufficient carrier density in the conduction band at the surface. Trapped electrons above the \( E_F \) emit back to the conduction band by the amount of Fermi potential change which results in fewer negative charges at the interface. \( \Delta \phi_F \) is the same for all samples as 0.085 V since we assume the same p-base doping for all DUTs. The effect of Fermi-Dirac distribution broadening at high temperature is neglected in the calculation.

\( N_{it} \) can be obtained by two methods, either by integrating \( D_{it} \) within the potential change using the \( D_{it} \) distribution in the previous section (method A), or from temperature-dependent threshold voltage reduction (method B). Table I shows the extracted \( N_{it} \) values from two methods. \( N_{it} \) extracted from method B is indeed the integration of \( D_{it} \) from the conduction...
band edge where $E_F$ locates at room temperature ($E_{CS} - E_{TO} \equiv 0$ eV) to $\Delta \phi_F$ ($E_{CS} - E_{TO} \equiv 0.085$ eV). Therefore, in order to integrate $D_\text{it}$ from the conduction band edge through $\Delta \phi_F$, method A has been further extended to estimate $D_\text{it}$ in the strong inversion. $I_D S (2\phi_F)$ in (7) is raised close to the inversion point, $E_{CS} - E_{TO} \equiv 0$ eV. $N_d$ from method A in Table I is the integrated areas under each $D_\text{it}$ curve in Fig. 7 (b). $N_d$ values extracted from both the techniques are in good agreement.

The number of fixed charges per unit area, $N_d (= n_F/q)$, is also calculated from (8) by subtracting the contribution of interface charges at room temperature. Here we assumed that the negative trapped charges within 0.3 eV of the conduction band contribute most of the negative charge in $N_d$. Therefore, integration is performed from $E_{CS}$ to $E_{CS} - 0.3$ eV for each vendor in Fig. 7. The value assumed for the p-well doping $N_d$ is $2 \times 10^{17}$ cm$^{-3}$ as mentioned previously. Extracted $N_d$ and $N_{it}$ values from DUTs are summarized in Table I. Although this method may provide relative comparison between devices and across the vendors, extracted values are not highly accurate compared to the real values since occupied trap density, $N_{it}$, is unlikely to be zero at $T=150 \, ^\circ C$. Therefore, our experimental condition gives a lower bound on $N_d$ and $N_{it}$.

**IV. CONCLUSIONS**

We describe a method to extract interface trap density, $D_{it}$, and oxide trap density, $N_{ox}$, on 1.2 kV commercial, packaged 4H-SiC Power MOSFETs since there is a delicate balance between the interface and oxide trap densities together with the design of the impurity profile to meet performance and reliability at room and elevated temperatures. These devices are under consideration for electric vehicles (EVs) and solar energy applications.

A subthreshold slope method, combined with temperature measurements of threshold voltage, is used to determine the above-mentioned trap densities, as shown in Table I. Since process information is often not available from vendors, in our studies we estimated a gate oxide thickness with ramp-to-breakdown measurement and assumed a substrate doping of $2 \times 10^{17}$ cm$^{-3}$. The results in Table I indicate the significant differences among three vendors. Five devices, each from three different vendors C, D, and E, are used in the study. For example, a threshold voltage reduction over a temperature range from 25°C to 150°C of 3.4 V for vendor C is correlated with the highest integrated interface trap density. In terms of device operation, under fast switching with high switching losses, increasing junction temperatures cause a negative shift in threshold voltage. The threshold voltage should be carefully chosen to be higher than a critical value for safe operation of the circuit.

At high temperatures, electrons trapped in interface states emit to the conduction band and lower the threshold voltage together with fixed oxide charges, which are as high as interface trap densities. Thus, the impurity profile must be adjusted to maintain a threshold voltage to ensure the device does not operate in a Normally-ON condition and to protect against gate voltage surges. Therefore, more focus on characterization and reduction of the interface trap density and fixed oxide charge is needed to enable further improvement in effective electron mobility of SiC MOSFETs. Moreover, in high power applications where multiple MOSFETs are paralleled within a power module and multiple power modules are used, current sharing across devices should be uniform for long-term reliability. Otherwise, devices with low threshold voltage will carry a larger share of the total current.

**ACKNOWLEDGMENT**

This research is supported in part by the block gift grant from the II-VI Foundation. The authors would also like to thank the Power Electronics Teams at Ford Motor Company’s Research and Innovation Centers for helpful discussions.
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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2021.3124706, IEEE Access
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He joined the Electrical and Computer Engineering Department at The Ohio State University in 2010. His teaching areas concern analysis and design of integrated circuits for systems applications and the physics of semiconductor devices. In the years, he has been in industry and the university, he has over 300 papers and 28 U. S. Patents with colleagues and students. His research interests are custom integrated circuit design, signal processing, solid-state imaging, nonvolatile charge-trap memories, CMOS transistor modeling, sensors, SiC Power Devices and BioMEMS. He has graduated 37 Ph.D. and 67 M.S. students.

Professor White was elected a member of the National Academy of Engineering in 2001. He received the IEEE EDS J. J. Ebers Award in 1997, the Masura Ibuka Consumer Electronics Award in 2000, the Aldert van der Ziel Award for distinguished teaching in 2001 and the IEEE EDS Distinguished Service Award in 2010. In 2011, he received OSU’s College of Engineering Distinguished Alumnus Award. In 2019 he received the International Image Sensor Society Pioneering Achievement Award for correlated double sampling (CDS), which is used in high-performance imaging systems.

Anant K. Agarwal (F’12) joined The Ohio State University at Columbus, Ohio in August 2017. Previously, he was with the US Department of Energy (DOE) during March 2013 - November 2016. While at DOE, Dr. Agarwal helped create and manage four programs related to wide band-gap technology and their applications including PowerAmerica, Next Generation of Electric Machines (I and II) and Graduate Traineeships. From 1999 to 2013, Dr. Agarwal was Director of Research and Development for Wide Band Gap (WBG) devices at Cree, Inc. In this role, he oversaw the development and commercialization of Silicon Carbide diode and MOSFET power devices. Today, these WBG semiconductors are being employed globally to improve efficiency and reduce power consumption in systems such as power supplies, solar inverters, and motor drives.

Previously, Dr. Agarwal was a Fellow at Northrop Grumman Science and Technology Center, Pittsburgh (1990-1999). While at Northrop Grumman he led research activities on radio frequency Silicon and Silicon-Germanium transistors. He was also instrumental in solving a large number of fundamental issues relating to WBG technologies.

Prior to joining Northrop Grumman, Dr. Agarwal held various teaching and research positions (1984-1990) including Associate Professor in Allahabad, India and Member of the Technical Staff at AT&T Bell Laboratories, Murray Hill, NJ. While at Bell Labs he was involved in the development of Gallium-Arsenide digital circuits for fiber-optic communications.

Dr. Agarwal received his PhD degree in Electrical Engineering from Lehigh University, PA in 1984; MS degree in Electrical Engineering from the University of Tennessee Space Institute (UTSI) in 1980; and Bachelor of Science in Electrical Engineering from MNR Engineering College, University of Allahabad, India in 1978. He jointly holds more than 60 patents, has co-authored more than 300 research papers, co-edited a book on Silicon Carbide Technology, co-authored five book chapters and was elected an IEEE Fellow in January 2012 for contributions to Wide Band Gap technologies.

As a leading research scientist in this area, Dr. Agarwal’s life goal has been to successfully commercialize WBG power devices to resurrect the domestic power electronics industry while educating the next generation of researchers. This will ultimately enable the creation of high-quality manufacturing jobs in the US while perpetuating a high-tech US workforce.