Reduced Voltage Stress Asymmetrical Multilevel Inverter with Optimal Components

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ABSTRACT The article presents a single phase asymmetrical multilevel inverter with a reduced components and low voltage stress which reduces the size and cost of the system. The structure provides a maximum output voltage of 23 levels with asymmetrical DC sources. There exists several reliability issues in lowering the total harmonic distortion (THD) by utilizing higher components in the design of MLI despite of its merits. Achieving reliability and lowering the THD is a challenging task for the researchers. The proposed 23-level MLI has been investigated with various performance parameters like total voltage standing (TSV), cost function (CF), power loss and efficiency analysis. The suggested MLI is compared with the existing topologies in the recent past and found that it has less voltage stress across the switches and cost-effective. The TSV calculations show that the proposed structure is more efficient in reducing the losses and increasing the efficiency. Hence, based on the evaluations and the comparisons made with the other topologies, it is found that the proposed MLI is well suited for the medium power applications such as FACTS, SVC, DSTATCOM and DVR. As the proposed architecture provides the 23 level output voltage values with asymmetrical DC sources, the configuration can be utilized for improving power quality in grid-connected renewable energy sources. The topology provides a less THD value which is under IEEE standards. The proposed architecture has been designed in MATLAB/Simulink and is implemented experimentally in hardware prototype in the laboratory environment.

INDEX TERMS Multi-level inverter, Maximum blocking voltage, Normalized voltage stress, Cost function, TSV Calculation, Total harmonic distortion (THD).

I. INTRODUCTION

Multilevel inverters (MLI) have gained abundant interest in recent decades because of their benefits of reduced dv/dt stress, greater electromagnetic compatibility, lesser total harmonic distortion (THD), and superior output waveforms. As a result, these are preferred in high-voltage applications including AC drives, renewable energy, FACTS, and dynamic voltage restorer (DVR) etc., [1]. MLI was first developed in 1975 by Baker and Bannister [2]. Cascaded H-bridge type (CHB) MLI is a common name for the topology, which consists of multiple series-connected H-bridges. The flying capacitor (FC), cascaded H-bridge (CHB), and neutral point clamped (NPC) techniques are the three most common MLI topologies. CHB has captured the market's interest and is extensively utilized by sectors due to features such as simplicity and adaptability, however, have a drawback in that it is restricted by the need for separate sources [3]. Static compensators, motor drives, grid-connected RES, and photovoltaics are just a few of the many uses for MLIs [4]. Traditional MLI designs have a substantial restriction to achieve higher voltage levels because of number power switch requirements. A converter system with more semiconductor switches is bulky, expensive, and complex because of a protection unit, gate driving unit, and heat sink are generally integrated with each power switch. As a result, one of the fastest-growing study fields in MLIs is lowering the power switch count, and several topologies with fewer devices have recently been presented [5]. Seventeen level asymmetric MLI topology for medium voltage applications
with less dc sources count, less power switches, and lower dv/dt stress on switches was proposed in [6].

 Novel MLI s have been presented to optimize the number of dc voltage sources and power switches [5]–[20]. The H-bridge structure was utilized to provide an alternate output voltage in the architectures presented in [7]. H-bridge switches, on the other hand, must be able to withstand large output voltages before they can be used. This issue is solved with H-type [8] and square T-type (ST-type) [9] structures, which provide alternate output voltage levels without the need for H-bridge. A new switched capacitor with single DC source and reduced components for low voltage RES applications was presented in [10] and an extended MLI topology with reduced switch and low voltage stress was presented in [11]. The topology presented in [12] employs the fewest total power electronic components. By connecting IGBT switch and diode in series/parallel. Using two dc sources and bidirectional switches coupled cross-network style, a rudimentary unit was created in [13]. As long as a full-bridge converter is used, this design may provide a multilevel output voltage on the load side while also working in asymmetrical mode. In [14], a topology is developed to minimize the maximum blocking voltage (MBV) on switches. The total standing voltage (TSV) in [15] is lower, making it a better choice for high-power applications. A unique generalized MLI configuration with optimal components, lesser power losses, and less blocking voltage is presented in [16]. The topology in [17] presents a switched capacitor MLI configuration with a low device count that has the benefits of negative polarity voltage generation without the use of an auxiliary H-bridge, the efficient voltage balancing can be done across the floating capacitors, and minimum PIV across the switches. In order to decrease the DC sources count, MLI based on switched capacitors are presented in [18] which produces nine voltage levels per DC source and also has several advantages such as enhancing the input voltage, but it suffers from a non-modularity feature.

In this work, a new MLI circuit is designed that solves all limitations and uses fewer components than similar topologies. The proposed MLI can be used to integrate distributed energy resources into medium voltage grids. The inverter's high-quality output voltage reduces the need for huge filters. The inverter reduces the size and weight along with the cost of the filters. Hence, the developed topology could be a reasonable solution for connecting PV sources in case of many DC sources are available. The proposed configuration can be employed in single-phase medium voltage applications. According to a comparison analysis, the recommended circuit uses fewer components, has reduced power loss values and increases the inverter's efficiency.

However, in modern topologies, the TSV at the power switches is analyzed for the performance calculations. To test the suggested circuit's performance, both simulation and experimental conditions of the proposed 23 level inverter are examined. The following are the most important characteristics of the suggested topology:

- Using only three sources and 12 switches, the suggested topology produces output voltage levels of 7 and 23 in both symmetrical as well as in asymmetrical configurations.
- The suggested architecture eliminates the need for an additional H-bridge circuit to produce alternate voltage levels, resulting in a considerable decrease in TSV.
- The majority of the switches have less voltage stress, allowing them to operate at medium voltages.
- The harmonic profile of proposed MLI is superior to traditional inverters, and adherence to the standard of IEEE 519.

The article is organized as follows: Section 2 presents the proposed circuit analysis as well as its general structure and also includes the selection of component value for extended topology, as well as TSV computations. Section 3 discusses comparative assessments of the suggested and other existing topologies. The proposed topology’s power losses and efficiency are calculated in section 4. Cost estimation of the proposed design for medium voltage applications is discussed in Section 5. Both simulation as well as prototype experimental results with control switching approaches are provided in Section 6, and the conclusion is provided in Section 7, preceded by the references cited.

II. PROPOSED 23 LEVEL MLI TOPOLOGY

The proposed configuration comprises three dc sources namely V1, V2, and V3, and twelve unidirectional switches S1 to S12 are depicted in Figure 1. There are three units in the proposed topology: a left unit (L-unit), a center unit (C-unit), and a right unit (R-unit). Each unit is powered by its dc power supply. V1, V2, and V3 respectively. In R-unit the switches (S1, S2) and (S3, S4), in C-unit the switches (S5, S6) and (S7, S8), in L-unit the switches (S9, S10), and (S11, S12) are never switched ON at the same time. In this manner a short circuit between the DC sources are prevented. Both symmetric and asymmetric combinations may be operated using the proposed topology.

Figure 1. Proposed 23 level multilevel configuration.
A. Components selection

1) For symmetric mode, the magnitudes of DC voltage sources are fixed to be same.

\[ V_1 = V_2 = V_3 = V_{dc} \]  \hspace{1cm} (1)

The required DC sources \( N_{DC} \) are mathematically related to the number of levels \( N_{Lev} \) by using the equation:

\[ N_{DC}^{Sym} = \frac{(N_{Lev}-1)}{2} \]  \hspace{1cm} (2)

The number of switches ‘\( N_{SW} \)’ required may be mathematically related to the number of levels \( N_{Lev} \), by using the equation:

\[ N_{SW}^{Sym} = 2(N_{Lev} - 1) \]  \hspace{1cm} (3)

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits \( N_{GDK} \) equals the number of IGBTs \( N_{SW} \), and is written as:

\[ N_{GDK}^{Sym} = N_{SW}^{Sym} = 2(N_{Lev} - 1) \]  \hspace{1cm} (4)

The maximum voltage output produced \( V_{L,max} \) is given by:

\[ V_{L,max}^{Sym} = \frac{(N_{Lev}-1)}{2} \]  \hspace{1cm} (5)

In symmetric mode, the proposed configuration produces 7 levels of voltage output with magnitudes of zero, \( \pm 1V_{dc} \), \( \pm 2V_{dc} \), and \( \pm 3V_{dc} \).

2) For asymmetric operation, the DC voltage source’s magnitudes are fixed as

\[ V_1 = 1V_{dc}; \ V_2 = 3V_{dc}; \ V_3 = 7V_{dc} \]  \hspace{1cm} (6)

The required DC sources \( N_{DC} \) in asymmetric mode may be mathematically related to the number of levels \( N_{Lev} \), used by the equation:

\[ N_{DC}^{Asym} = \frac{(N_{Lev}-5)}{6} \]  \hspace{1cm} (7)

\[ \text{FIGURE 2. Operating modes of twenty three level MLI topology} \]
The number of switches $N_{SW}$ required in asymmetric mode may be mathematically related to the number of levels $N_{Lev}$ used by the equation:

$$N_{SW}^{Asym} = \frac{(N_{Lev}+1)}{2}$$  \hspace{1cm} (8)$$

**Table I**

| Levels | Switch States $S_1S_2\ldots\ldots S_{N_{SW}}$ | Current conducting path | Active sources | Output Voltage (Volts) |
|--------|-----------------------------------------------|-------------------------|-----------------|------------------------|
| L1     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}+V_{5}+V_{1}$ | +11V dc |
| L2     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{1}+V_{2}$ | +10V dc |
| L3     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}+V_{5}+V_{1}$ | +9V dc |
| L4     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}+V_{1}$ | +8V dc |
| L5     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +7V dc |
| L6     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}+V_{1}$ | +6V dc |
| L7     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}+V_{1}$ | +5V dc |
| L8     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}+V_{1}$ | +4V dc |
| L9     | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}$ | +3V dc |
| L10    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}+V_{1}$ | +2V dc |
| L11    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{1}$ | +1V dc |
| L12    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{1}$ | 0V dc |
| L13    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{1}$ | +1V dc |
| L14    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}$ | +2V dc |
| L15    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}$ | +3V dc |
| L16    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}$ | +4V dc |
| L17    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{2}$ | +5V dc |
| L18    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +6V dc |
| L19    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +7V dc |
| L20    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +8V dc |
| L21    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +9V dc |
| L22    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +10V dc |
| L23    | $010101101010101$ | $V_{3S0S2S4S6S8S9S11S12}$ | $V_{3}$ | +11V dc |

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits $N_{GDK}$ equals the number of IGBTs $N_{SW}$, and is written as:

$$N_{GDK}^{Asym} = N_{SW}^{Asym} = \frac{(N_{Lev}+1)}{2}$$  \hspace{1cm} (9)$$

The maximum voltage output produced $V_{L_{max}}$ is given by:

$$V_{L_{max}}^{Asym} = \frac{(N_{Lev}+1)}{2}$$  \hspace{1cm} (10)$$

In asymmetric mode, the proposed configuration produces 23 levels of voltage output with magnitudes of zero, positive (+1 V dc to +11 V dc), and negative (-1 V dc to -11 V dc). The proposed 23-level asymmetric MLI topology’s switching states are tabulated in Table 1. In addition, Figure 2 shows the relevant connection diagrams for various voltage levels, while Figure 3 shows the expected output with varied switch states.

**B. Analysis of TSV**

Total maximum blocking voltage is one of the most important qualitative characteristics, which is referred to as the algebraic sum of the maximum voltage stress on the switches [21]. $S_1$ is expected to describe the TSV computation. Figure 2 is used to compute the MBV of $S_1$ (off-state). (+1V dc or +4V dc or...
+5V_{dc} or +8V_{dc} or +11V_{dc} or -2V_{dc} or -6V_{dc} or -9V_{dc}) in which standing voltage on S_1 is created by using the R-unit dc source V_{S1}= 1V_{dc}.

The MBV of particular switches are calculated as follows:

**For R-unit:**
- MBV_{S1} = MBV_{S4} = 1V_{dc}
- MBV_{S2} = MBV_{S3} = 1V_{dc}

**For L-unit:**
- MBV_{S9} = MBV_{S11} = 7V_{dc}
- MBV_{S10} = MBV_{S12} = 7V_{dc}

**For C-unit:**
- MBV_{S5} = MBV_{S7} = 3V_{dc}
- MBV_{S6} = MBV_{S8} = 3V_{dc}

The term "Normalized voltage stress (NV_{strs})" refers to the ratio of V_{strs} across the switch to the maximum voltage V_{L,max} [22], given by

\[ NV_{strs} = \frac{V_{strs}}{V_{L,max}} \]  
(11)

Where V_{strs} is real voltage stress of the switch and corresponding values are tabulated in Table 2. Switches S_1, S_2, S_3, and S_4 experience the lowest V_{strs} and NV_{strs}, i.e. V_{dc} and 9.09% respectively, whereas switches S_5, S_6, S_7, and S_8 experience three times the lowest V_{strs} and NV_{strs}, i.e. 3V_{dc} and 27.27% respectively, and switches S_9, S_{10}, S_{11}, and S_{12} experience the highest V_{strs} and NV_{strs}, i.e. 7V_{dc} and 63.36%.

### Table II

| Switch | Voltage Stress (V_{strs}) | Normalized Voltage Stress (NV_{strs}) |
|--------|--------------------------|-------------------------------------|
| S_1    | 1V_{dc}                  | \( \frac{1V_{dc}}{11V_{dc}} \) = 9.09% |
| S_2    | 1V_{dc}                  | \( \frac{1V_{dc}}{11V_{dc}} \) = 9.09% |
| S_3    | 1V_{dc}                  | \( \frac{1V_{dc}}{11V_{dc}} \) = 9.09% |
| S_4    | 1V_{dc}                  | \( \frac{1V_{dc}}{11V_{dc}} \) = 9.09% |
| S_5    | 3V_{dc}                  | \( \frac{3V_{dc}}{11V_{dc}} \) = 27.27% |
| S_6    | 3V_{dc}                  | \( \frac{3V_{dc}}{11V_{dc}} \) = 27.27% |
| S_7    | 3V_{dc}                  | \( \frac{3V_{dc}}{11V_{dc}} \) = 27.27% |
| S_8    | 3V_{dc}                  | \( \frac{3V_{dc}}{11V_{dc}} \) = 27.27% |
| S_9    | 7V_{dc}                  | \( \frac{7V_{dc}}{11V_{dc}} \) = 63.63% |
| S_{10} | 7V_{dc}                  | \( \frac{7V_{dc}}{11V_{dc}} \) = 63.63% |
| S_{11} | 7V_{dc}                  | \( \frac{7V_{dc}}{11V_{dc}} \) = 63.63% |
| S_{12} | 7V_{dc}                  | \( \frac{7V_{dc}}{11V_{dc}} \) = 63.63% |

![Figure 4](image.png)

**Figure 4.** (a) Voltage stress distribution, (b) normalized voltage stress in %, and (c) voltage constraints different switches in each level.

Figure 4 (a) depicts the stress distribution of each switch, Figure 4 (b) depicts the normalized voltage stress in percentage, and Figure 4 (c) depicts the voltage constraints in each level of the proposed topology. In traditional H-bridge-based MLI configurations, the blocking voltage experienced by four H-bridge switches is equal to the algebraic sum of DC sources in the circuit, i.e. 7V_{dc} [22]. The highest output voltage in the recommended MLI design is 11V_{dc}, which creates a level of 23 at the output voltage, but the algebraic sum of DC sources is more than the MBV (7V_{dc}) encountered by the
The required DC sources \( N_{\text{DC}} \) in extended structure may be mathematically related to the number of levels \( N_{\text{lev}} \) used by the equation:

\[
N_{\text{DC}}^{\text{Ext}} = \frac{\left(N_{\text{lev}}-5\right)}{6}
\]  

(17)

The number of switches \( N_{\text{SW}} \) required in extended structure may be mathematically related to the number of levels \( N_{\text{lev}} \) used by the equation:

\[
N_{\text{SW}}^{\text{Ext}} = \frac{(N_{\text{lev}}-1)+2n}{2}
\]  

(18)

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits \( N_{\text{GDK}} \) equals the number of IGBTs \( N_{\text{SW}} \), and is written as:

\[
N_{\text{GDK}}^{\text{Ext}} = N_{\text{SW}}^{\text{Ext}} = \frac{(N_{\text{lev}}-1)+2n}{2}
\]  

(19)

The maximum voltage output produced \( V_{L,\text{max}} \) is given by:

\[
v_{L,\text{max}}^{\text{Ext}} = \frac{\left(N_{\text{lev}}-1\right)}{2}
\]  

(20)

MBV of individual switches are given as:

- For R-unit: \( MBV_{S1} = MBV_{S4} = V_R \)
- For L-unit: \( MBV_{S6} = MBV_{S11} = V_L \)
- For C-unit: \( \sum_{i=1}^{n} MBV_{S_{i0}} = \sum_{i=1}^{n} MBV_{S_{i2}} = \sum_{i=1}^{n} MBV_{S_{i1}} = \sum_{i=1}^{n} V_C \)

Therefore for the extended topology, \( TSV_{\text{Ext}} \) is calculated as:

\[
TSV_{\text{Ext}} = 4\left(V_R + V_L\right) + 4\sum_{i=1}^{n} V_C
\]  

(21)

III. COMPARISONS

To evaluate the benefits and capabilities of the suggested topology, a comparison is made with other recent topologies. Quantitative and qualitative evaluations of similar and different asymmetrical MLI configurations are carried out to showcase the benefits of the suggested topology. For both the same number of output voltage level topologies [21-28] and different numbers of output voltage level topologies [6, 9, 16, 20, 29-31], a comparison has been made per level concerning the required driver circuits, DC sources, switches, the factor of the component count, maximum conducting devices, \( TSV_{\text{PU}} \), and cost factor are tabulated in Table 3.

Several parameters, such as the switch count \( N_{\text{SW}} \), source count \( N_{\text{DC}} \), driver circuit count \( N_{\text{GDK}} \), diode count \( N_D \), capacitor count \( N_C \), and total standing voltage \( TSV \) can be used to calculate the cost factor \( (CF) \). The cost factor is calculated with the following formula:

\[
CF = \frac{N_{\text{SW}} + N_{\text{DC}} + N_{\text{GDK}} + N_D + N_C + \alpha TSV_{\text{PU}}}{N_{\text{lev}}}
\]  

(22)

In practice, the value of ‘\( \alpha \)’ should be larger than and less than unity, respectively. For the optimal assessment of the cost function, the respective values of ‘\( \alpha \)’ are approximated as 0.5 (<1) and 1.5 (>1) in the designed MLI.

The component count per level is calculated as:

\[
CF/N_{\text{lev}} = \frac{N_{\text{SW}} + N_D + N_C + N_{\text{GDK}} + N_D + \alpha TSV_{\text{PU}}}{N_{\text{lev}}}
\]  

(23)

Figure 6 presents the display of several performance characteristics to assess the suggested topology. The suggested topology has a significantly higher performance in terms of required switches for producing the desired output.
levels, as shown in Figure 6a. However, the design in [25] requires fewer switches than the proposed MLI, but more DC sources. The topology in [25], [28] has better values than proposed, however, the demand for DC sources is considerable. As a result, as illustrated in Figure 6d, the total number of components per level is less as compared to other topologies. According to Figure 6e, the THD value is lower than the high TSVPu design [21], and the TSVPu of the suggested topology is lower than that of recent topologies, as shown in Figure 6f. Finally, from Figure 6g, the suggested topology has the lowest cost factor when compared to recent topologies.

TABLE III

| Topologies | Quantitative analysis | Qualitative analysis |
|------------|-----------------------|----------------------|
|            | Ref | Nlev | NSW | NDC | NGDK | NVar | MCD | CC/Nlev | TSVPu | % THD | CF/Lev | Negative level |
|            |     |   |     |     |     |     |     |     |     |     |       | alpha = 0.5 | alpha = 1.5 |
| Similar    | [21] | 23 | 12 | 6 | 12 | 0 | 6 | 1.30 | 5.81 | 2.59 | 1.43 | 1.68 | H-Bridge |
|           | [23] | 23 | 12 | 3 | 12 | 0 | 4 | 1.21 | - | 4.38 | - | - | H-Bridge |
|           | [24] | 23 | 14 | 5 | 14 | 0 | 7 | 1.43 | - | 5.47 | - | - | Inherent |
|           | [25] | 23 | 10 | 5 | 10 | 2 | 4 | 1.17 | 6.09 | - | 1.39 | 1.65 | Inherent |
|           | [26] | 23 | 12 | 8 | 12 | 0 | 7 | 1.39 | - | 4.09 | - | - | H-Bridge |
|           | [27] | 23 | 12 | 5 | 12 | 0 | 4 | 1.26 | 4.4 | 3.6 | 1.35 | 1.54 | Inherent |
|           | [28] | 23 | 12 | 5 | 9 | 5 | 3 | 1.34 | - | 4.17 | - | - | H-Bridge |
| Proposed  | [5]  | 23 | 12 | 3 | 12 | 0 | 6 | 1.17 | 4.0 | 3.23 | 1.26 | 1.43 | Inherent |
|           | [9]  | 23 | 12 | 4 | 10 | 2 | 5 | 1.64 | 5 | 3.06 | 1.61 | 1.91 | H-Bridge |
|           | [16] | 23 | 10 | 4 | 10 | - | 5 | 1.41 | 4.5 | 6.17 | 1.54 | 1.80 | Inherent |
|           | [20] | 23 | 14 | 4 | 16 | 4 | 6 | 3.05 | 5 | 4.23 | 3.58 | 4.02 | H-Bridge |
|           | [29] | 23 | 12 | 4 | 10 | 0 | 10 | 1.04 | 5 | - | 1.14 | 1.34 | H-Bridge |
|           | [30] | 23 | 10 | 3 | 10 | 0 | 5 | 1.35 | 4.0 | 5.17 | 1.52 | 1.76 | H-Bridge |
|           | [31] | 23 | 11 | 5 | 10 | 2 | 4 | 1.47 | 5.55 | 5.62 | 1.61 | 1.91 | H-Bridge |

(a) Number of Switches

(b) Driver circuits

(c) Number of Sources

(d) Components count/Level
IV. POWER LOSS AND EFFICIENCY CALCULATION

In multilevel inverters, there are two significant power losses. They are conduction power losses ($P_C$) and switching power losses ($P_{sw}$). Overall conduction loss is calculated by adding the conduction losses of both IGBTs ($P_{CD}$) and anti-parallel diodes ($P_{CD}$) in the current path and is expressed as:

$$P_C(t) = P_{C_{SW}}(t) + P_{C_{D}}(t)$$  \hspace{1cm} (24)

$$P_C(t) = (N_{SW} + R_{SW}i_m(t)) + (N_{D} + R_{D}i_m(t))i_m(t)$$  \hspace{1cm} (25)

Where $i_m$ is the peak output current. $V_{SW}, V_D$ is the power switch and diode threshold voltages, $R_{SW}, R_D$ are the ON-state switch resistance and diode resistance, and $\beta$ is a switch specification constant provided by datasheet.

If $N_{SW}$ and $N_D$ are the switches and diodes conducting at the same time ($t$) to produce each level then, the average conduction loss is

$$P_C = \frac{1}{2\pi} \int_0^{2\pi} [N_{SW}(t)P_{C_{SW}}(t) + N_D(t)P_{C_{D}}(t)]dt$$  \hspace{1cm} (26)

The power consumed at the instant of the switch turn ON and turn OFF is known as switching loss ($P_{sw}$). For both the switch and the antiparallel diode, this loss is estimated. The following formula can be used to determine turn-on and turn-off energy losses ($E_{on}, E_{off}$)

$$E_{off} = \int_0^{t_{off}} (v(t)i(t))dt$$

$$= \int_0^{t_{off}} \left[ \left( V_{SW}q t_{off} \right) - \frac{I}{t_{off}} (t - t_{off}) \right] dt$$

$$E_{off} = \frac{1}{6}V_{SW} q t_{off}$$  \hspace{1cm} (27)

Similarly,

$$E_{on} = \int_0^{t_{on}} (v(t)i(t))dt$$

$$= \int_0^{t_{on}} \left[ \left( V_{SW}q t_{on} \right) - \frac{I}{t_{on}} (t - t_{on}) \right] dt$$

$$E_{on} = \frac{1}{6}V_{SW} q t_{on}$$  \hspace{1cm} (28)

Where time to turn OFF and ON, and loss of the switch $q$ are $t_{off}, t_{on}$ and $E_{off}, E_{on}$ respectively. $I$ and $I'$ are the switch current before turn OFF and after turn ON and $V_{sw}$ is the OFF state switch voltage. Thus

$$P_{sw} = f \left[ \sum_{q=1}^{N_{sw}} E_{off} q + \sum_{i=1}^{N_{off}} E_{off} q i \right]$$  \hspace{1cm} (29)

Where fundamental frequency is $f$, $N_{off}$, and $N_{off}$ is the number of times $q^{th}$ switch turn ON or turn OFF in one fundamental cycle. Thus, total power losses are

$$P_T = P_c + P_{sw}$$  \hspace{1cm} (30)
The total efficiency (\(\eta\)) can be calculated as
\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_T}
\]  
(31)

The output and input powers are \(P_{\text{out}}\) and \(P_{\text{in}}\). The output power can be calculated as
\[
P_{\text{out}} = V_{\text{rms}} \times I_{\text{rms}}
\]  
(32)

Table 4 summarizes the power losses and efficiency of the proposed 23-level MLI and the efficiency at different loads are shown in Figure 7.

| TABLE IV |
| --- |
| SUMMARY OF POWER LOSS AND EFFICIENCY |
| Resistive load (ohms) | 100 | 200 | 320 | 400 | 500 |
| Vrms (Volts) | 282.84 | 282.84 | 282.84 | 282.84 | 282.84 |
| Irms (Amps) | 2.82 | 1.414 | 0.88 | 0.707 | 0.565 |
| Output power | 797.6 | 400 | 250 | 200 | 160 |
| Conduction loss Pc (Watts) | 58.47 | 19.77 | 10.05 | 7.48 | 5.6 |
| Switching loss Pswi (Watts) | 0.365 | 0.182 | 0.114 | 0.09 | 0.073 |
| Total loss PT (Watts) | 58.83 | 19.95 | 10.164 | 7.57 | 5.673 |
| Input power Pin (Watts) | 856.43 | 419.95 | 260.16 | 207.57 | 165.67 |

**V. COST EVALUATION**

It is necessary to compute the proposed MLI’s maximum working voltage in order to determine its greater cost-benefit when it is utilized for medium voltage applications. Considering that the maximum standard commercial voltage of a switch is \(V_{\text{SW ccv}}\), therefore the proposed multilevel inverter’s maximum operating voltage is equal to \(\sqrt{1.5} V_{\text{SW ccv}}\) \(\gamma\) and \(\gamma\) is a safe operating factor of the switch, which is generally assumed to be 1.7. As a result, the suggested topology’s operation voltage may be determined by determining the maximum switch voltage. For medium voltage applications, the switch voltage is calculated by assuming the 3-phase operating RMS voltage as 2.3 kV, if the maximum switch voltage is 3.3kV. For 1-\(\phi\), the operating RMS voltage will be 1328V, with a maximum voltage of 1878V. As a result, the voltage magnitudes of 23-level MLI will be \(V_1 = 170.72V, V_2 = 512.18V,\) and \(V_3 = 1195.04V\) for an RMS voltage of 1328V. Thus the switch rated voltage for the recommended topology is determined using Table 2 and \(V_{\text{SW ccv}}\) is considered from Table 5. Table 6 calculates and compares the costs of needed IGBTs and driver circuits for 1-\(\phi\) proposed 23-level MLIs and existing 13-level and 11-level MLIs [34], [33].

| TABLE V |
| --- |
| VOLTAGE RATING OF THE SWITCHES IN THE PROPOSED TOPOLOGY |
| Switches | Voltage | IGBTs Rating |
| --- | --- | --- |
| Standard | Normal | 600V, 400A | 600V, 400A |
| S1 | 170.72 V | 600 V | CM20MD-12H |
| S2 | 170.72 V | 600 V | CM20MD-12H |
| S3 | 170.72 V | 600 V | CM20MD-12H |
| S4 | 170.72 V | 600 V | CM20MD-12H |
| S5 | 518.16 V | 1200 V | CM400HA-24A |
| S6 | 518.16 V | 1200 V | CM400HA-24A |
| S7 | 518.16 V | 1200 V | CM400HA-24A |
| S8 | 518.16 V | 1200 V | CM400HA-24A |
| S9 | 1209.04 V | 2500 V | CM400DY-50H |
| S10 | 1209.04 V | 2500 V | CM400DY-50H |
| S11 | 1209.04 V | 2500 V | CM400DY-50H |
| S12 | 1209.04 V | 2500 V | CM400DY-50H |

| TABLE VI |
| --- |
| COST COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND EXISTING TOPOLOGIES |
| IGBT and Driver model number | Voltage and Current Rating | Unit Cost |
| --- | --- | --- |
| CM400DY-66H | 3300 V, 400A | $773 |
| CM400DY-50H | 2500 V, 400A | $550 |
| CM400DU-34KA | 1700V, 400A | $516 |
| CM400HA-24A | 1200V, 400A | $118 |
| CM20MD-12H | 600V, 400A | $60.77 |
| 1SC0450V2A0-65 | Up to 6500V | $267.62 |
| SKYPER-32PRO2 | Up to 1700V | $92.71 |
| 844-SD303C25S20C | 2500V, 350A | $102.50 |
| Overall cost | $4727.24 |
| Number of voltage output levels | 23 |

*Courtesy: www.nevonexpress.com, www.yaspro.com, * Prices may vary. 

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half-step with a value of $p_{	ext{DC}}$, appearing at the $0^\text{th}$ phase angle, which is $\alpha_0 = 0$. $M = (N-1)/2$ excluding $\alpha_0$, is the total phase switching angles per quarter-wave which is related to $N$ [34]. The generalization of voltage of staircase modulation waveform can be represented as

$$V(\theta) = \sum_{k=1}^{M} P_k u(\theta - \alpha_k) + f_{\text{tg}} P_0$$  \hspace{1cm} (33)$$

where $0$ and $\alpha_k$ is lies in between 0 to 90 degrees, unit step function $u(\theta - \alpha_k)$ is zero if $\theta < \alpha$ whereas its value is unity if $\theta \geq \alpha$ and the toggle function $f_{\text{tg}}$ is zero for odd and 0.5 for even.

The normalized fundamental component of voltage at modulation index $M$ is given by

$$V_1 = m_a = \frac{4}{\pi} \sum_{k=1}^{M} (P_k \cos(\frac{k\pi}{180})) + f_{\text{tg}} P_0$$  \hspace{1cm} (34)$$

The range of voltage is given by

$$\frac{4}{\pi} f_{\text{tg}} P_0 \leq m_a \leq \frac{4}{\pi}$$  \hspace{1cm} (35)$$

The expected staircase waveform for the proposed topology is shown in figure 9. The variation of modulation index $M$ with respect to the number of levels (NL) is shown in TABLE VII.

| TABLE VIII | VARIATION OF MI WITH LEVELS OF PROPOSED 23 LEVEL MLI |
|------------|---------------------------------|
| Modulation Index | Number of Levels |
| 0.09       | 3                  |
| 0.18       | 5                  |
| 0.27       | 7                  |
| 0.36       | 9                  |
| 0.45       | 11                 |
| 0.55       | 13                 |
| 0.64       | 15                 |
| 0.73       | 17                 |
| 0.82       | 19                 |
| 0.91       | 21                 |
| 1.00       | 23                 |

Figure 7. Efficiency of proposed MLI at various loads

The MITSUBISHI Company produces a nominal current of 400A commercial IGBTs. As a role example [32], the costs of power diode (single pack, Mouser Electronics) and IGBTs (single pack), as well as the driver circuits (Semikron, dual pack), are in USD. From the price comparison the proposed MLI is less expensive.

VI. RESULTS AND DISCUSSION

A. Control scheme

The gate pulses are generated in MATLAB/Simulink using the round-robin condition (staircase modulation approach). Because of its primary advantages, such as less complexity and lower switching losses, the staircase Modulation technique is preferred over the classic PWM technique. This is true for both high-rated MLIs with higher voltage levels ($N$) and low-rated MLIs with lower voltage levels ($N$). This is the most frequent and well-known method for multilevel inverters going forward. In addition, with its lower losses for MLIs with higher ratings, this technique is the greatest alternative to the sine PWM switching technique. While symmetric MLIs are the most prevalent, using asymmetric MLIs with a cascaded H-Bridge reduces total harmonic distortion (THD) even further.

Figure 8. Generalized representation of a quarter-wave staircase waveform

Figure 8 depicts the waveform generated by the staircase modulation method as a generalized quarter-wave representation, with M desired steps per quarter-wave and an optional extra half-step appearing at the origin. For every $k^{th}$ step appearing at the phase switching angle $\alpha_0$, consists of a normalized width and height concerning the DC supply voltage ratio of $P_k, \alpha = \{\alpha_1, \alpha_2, \ldots, \alpha_k\}$ and $P = \{P_1, P_2, P_3, \ldots, P_M\}$ are the phase switching angle and the DC supply voltage ratio expressed in in degrees and per unit values respectively. In order to provide even values of $N$, an extra

![Proposed MLI schematic diagram](image-url)
B. Simulation results

The performance of the suggested configuration has been evaluated through simulation experiments using MATLAB/Simulink software. TABLE VIII lists the many parameters that were used in the analysis. A carrier frequency of 5 kHz is used to produce the pulses in simulation, and the design is evaluated with resistive and inductive loads of 100 ohms 187mH respectively. Figure 10(a) shows the simulated output voltage, while Figure 10(b) displays the simulation output voltage and current waveforms. The magnitude of source voltages in asymmetric source configuration is considered as $V_1=35\text{V}$, $V_2=110\text{V}$, and $V_3=255\text{V}$. At 400V peak voltage and 4 A load current, the inverter can produce 23 levels of output. Figure 10(c) shows the enhanced output waveform with a THD of 3.23 %. The simulation output waveform of the modulation index for $M = 0.6$ consists of 15 levels, $M = 0.8$ with 19 levels and $M = 1$ with 23 levels are represented in FIGURE 10(d).

| TABLE VIII |
|------------|
| **LIST OF PARAMETERS USED FOR PROPOSED 23 LEVEL MLI** |
| Parameters | Simulation | Experimental |
| Voltage Sources | $V_1=35\text{V}$, $V_2=110\text{V}$, $V_3=255\text{V}$ | $V_1=35\text{V}$, $V_2=110\text{V}$, $V_3=255\text{V}$ |
| Load values | 100Ω | 100Ω |
| Motor load | Single phase 230V, 0.5 HP | Single phase 230V, 0.5 HP |
| Switching frequency | 5KHz | 5KHz |
| IGBTs | CM75DU-12H | CM75DU-12H |

C. Experimental results

As illustrated in Figure 11, a single-phase prototype is built in the lab to evaluate the proposed MLI technology. The prototype is made up of 12 IGBT switches (CM75DU-12H) that are activated by optocouplers (MCT2E), and a dual dc supply provides input dc sources. The load parameters are 100 resistive load and 187mH inductive load. The real-time controller dSPACE1104 is used to build the switching control scheme and DSO is used to observe the voltage and current waveforms. Figures 12 and Figures 13 show the experimental results with resistive load at a steady-state output voltage $V_0 = 400\text{V}$ (282.84 $V_{\text{rms}}$) and load current $I_0= 4\text{A}$ (2.82 $I_{\text{rms}}$) respectively. With motor load, the output voltage $V_0 = 400\text{V}$ and the load current $I_0 = 6.8\text{A}$ equivalent to 4.8A $I_{\text{rms}}$ are shown in Figure 14. As illustrated in Figures 15 and 16, the
dynamic response of the proposed MLI is accomplished by adding an inductive load parallel to resistive load or contrariwise. With a power analyzer, the total voltage harmonic spectrum of 3.23% is measured and is displayed in Figure 17.

![Figure 12. Experimental voltage output of proposed 23 level MLI](image)

![Figure 13. Experimental current and voltage output with R load](image)

![Figure 14. Experimental current and voltage output with motor load](image)

![Figure 15. Experimental current and voltage output with dynamic RL load](image)

![Figure 16. Experimental current and voltage output with dynamic LR load](image)

![Figure 17. Hardware voltage THD of proposed 23 level MLI](image)

**D. Applications**

Due to the wide range of operation with the modulation index, the proposed reduced switch count MLI is an alternative to traditional MLIs in industrial requirements. Individual photovoltaic panels with varying ratings are fed into each of the three input sources of proposed MLI, which correspond to the ratings of the DC sources [35]. To accomplish this, several control objectives must be met, including the inverter maintaining optimal power quality within grid constraints, minimizing harmonic distortions in the output ac voltage waveform, and extracting the maximum amount of energy possible from solar panels under varying irradiance conditions in order to provide an
efficient and stable output throughout its operation. Additionally, to ensure reliability, the extracted power has been transferred to the output with a power factor of unity. Due to the fact that different solar panel ratings are used for different DC sources, an efficient maximum power extraction method is used to harvest energy in a variety of irradiance conditions. In this regard Power factor control is critical to transferring solar power to the grid, which is closer to a power factor of 0.95. Because the inverter rating is low according to IEC 929-2000 and IEC 62109-2 standards, reactive power consideration is not required in these systems. Furthermore, the suggested MLI is more suitable for solar PV applications in terms of fault ride-through capability and power balance because it has redundant switching states[36].

VII. CONCLUSION
An asymmetrical reduced component 23 level single-phase multilevel inverter configuration was proposed for medium voltage applications. Twelve switches and three DC sources are used in the proposed topology to produce eleven positive voltage levels and can be expanded to produce n voltage levels by adding a few devices. According to the findings of the proposed MLI and the comparisons with existing MLIs, the suggested MLI requires a lower component count per level to generate more output voltage levels. For 23-level MLI, several characteristics are examined, including cost function (CF), total standing voltage (TSV), and total harmonic distortion (THD) which is under IEEE standards. The proposed MLI is compared with other existing topologies and found to be superior among various parameters and found that it is cost-effective and compatible with the TSV and component count per level factor. As the proposed MLI has an asymmetrical sources, it can be widely utilized in hybridized energy sources where the various types of sources are interfaced. Hence the proposed MLI is well suited for medium-power and grid-connected FACTS devices such as DSTATCOM, and DVR.

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REFERENCES
[1] Babaei, Ebrahim, and Sara Laali. "A multilevel inverter with reduced power switches." Arabian journal for science and engineering 41, no. 9 (2016): 3605-3617.
[2] Baker, Richard H., and Lawrence H. Bannister. "Electric power converter." U.S. Patent 3,867,643, issued February 18, 1975.
[3] Siddique, Marif Daula, Muhyaddin Rawa, Saad Mekhilef, and Noraisyah Mohamed Shah. "A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources." International Journal of Electrical Power & Energy Systems 128 (2021): 106730.
[4] Anand, Vishal, and Varsha Singh. "Implementation of cascaded asymmetrical multilevel inverter for renewable energy integration." International Journal of Circuit Theory and Applications 49, no. 6 (2021): 1776-1794.
[5] Siddique, Marif Daula, Saad Mekhilef, Noraisyah Mohamed Shah, and Mudaisir Ahmed Memon. "Optimal design of a new cascaded multilevel inverter topology with reduced switch count." IEEE Access 7 (2019): 24498-24510.
[6] Nyamathulla, Shaik, and C. Dhananjayulu. "Design of 17-Level Inverter with Reduced Switch Count." In 2021 Innovations in Power and Advanced Computing Technologies (i-PACT), pp. 1-8. IEEE, 2021.
[7] Babaei, Ebrahim, Sara Laali, and Zahra Bayat. "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches." IEEE Transactions on industrial electronics 62, no. 2 (2014): 922-929.
[8] Kamani, Piyush L., and Mahmadrasf A. Mulla. "A Home-type (H-type) Cascaded Multilevel Inverter with Reduced Device Count: Analysis and Implementation." Electric Power Components and Systems 47, no. 19-20 (2019): 1691-1704.
[9] Samadaei, Emad, Abdolreza Sheikholeslami, Sayyed Asghar Gholamian, and Jafar Adabi. "A square T-type (ST-type) module for asymmetrical multilevel inverters." IEEE Transactions on power Electronics 33, no. 2 (2017): 987-996.
[10] Siddique, Marif Daula, Jagabar Sathik Mohamed Ali, Saad Mekhilef, Asif Mustafa, N. Sandeep, and Dhafer Almkhles. "Reduced switch count based single source 7L boost inverter topology." IEEE Transactions on Circuits and Systems II: Express Briefs 67, no. 12 (2020): 3252-3256.
[11] Siddique, Marif Daula, Saad Mekhilef, Muhyaddin Rawa, Addy Wahyudie, Bekkhan Chokaev, and Islam Salmanov. "Extended multilevel inverter topology with reduced switch count and voltage stress." IEEE Access 8 (2020): 201835-201846.
[12] Ibrahim, SA Ahamed, Anbalagan Palanimuthu, and MA Jagabar Sathik. "Symmetric switched diode multilevel inverter structure with minimised switch count." The Journal of Engineering 2017, no. 8 (2017): 469-478.
[13] Khosroshahi, Mahdi Toupchi. "Crisscross cascade multilevel inverter with reduction in number of components." IET Power Electronics 7, no. 12 (2014): 2914-2924.
[14] Gupta, Krishna Kumar, and Shailendra Jain. "A novel multilevel inverter based on switched DC sources." IEEE Transactions on Industrial Electronics 61, no. 7 (2013): 3269-3278.
[15] Arif, M. Saad Bin, Uvais Mustafa, Shahrin Bin Md Ayob, Jose Rodriguez, Abdul Nadeem, and Mohamed Abdelrahem. "Asymmetrical 17-Level Inverter Topology With Reduced Total Standing Voltage and Device Count." IEEE Access 9 (2021): 69710-69723.

[16] Ali, Jagabar Sathik Mohamed, Rasoul Shalchi Alishah, N. Sandeep, Seyed Hossein Hosseini, Ebrahim Babaei, Krishnasamy Vijayakumar, and Udaykumar R. Yaragatti. "A new generalized multilevel converter topology based on cascaded connection of basic units." IEEE Journal of Emerging and Selected Topics in Power Electronics 7, no. 4 (2018): 2498-2512.

[17] Siddique, Marif Daula, Saad Mekhilef, Noraisyah Mohamed Shah, Jagabar Sathik Mohamed Ali, and Frede Blaabjerg. "A new switched capacitor 7L inverter with triple voltage gain and low voltage stress." IEEE Transactions on Circuits and Systems II: Express Briefs 67, no. 7 (2019): 1294-1298.

[18] Iqbal, Atif, Marif Daula Siddique, B. Prathap Reddy, and Pandav Kiran Maroti. "Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count." IEEE Transactions on Power Electronics 36, no. 7 (2020): 7372-7377.

[19] Prasad, Devalraju, C. Dhnamjayulu, Sanjeevikumar Padmanaban, Jens Bo Holm-Nielsen, Frede Blaabjerg, and Shaik Reddi Khasim. "Design and implementation of 31-level asymmetrical inverter with reduced components." IEEE Access 9 (2021): 22788-22803.

[20] Dhnamjayulu, C., Devalraju Prasad, Sanjeevikumar Padmanaban, Pandav Kiran Maroti, Jens Bo Holm-Nielsen, and Frede Blaabjerg. "Design and implementation of seventeen level inverter with reduced components." IEEE Access 9 (2021): 16746-16760.

[21] Thakre, Kishor, Kanungo Barada Mohanty, Aditi Chatterjee, and Vinaya Sagar Kommukuri. "A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count." International Transactions on Electrical Energy Systems 29, no. 6 (2019): e12011.

[22] Mahato, Bidyut, Saikat Majumdar, and Kartick Chandra Jana. "Single-phase Modified T-type–based multilevel inverter with reduced number of power electronic devices." International Transactions on Electrical Energy Systems 29, no. 11 (2019): e12097.

[23] Sorto-Ventura, Kevin-Rafael, Mostafa Abarzadeh, Kamal Al-Haddad, and Louis A. Dessaint. "23-level Single DC source hybrid PUC (H-PUC) converter topology with reduced number of components: Real-time implementation with model predictive control." IEEE Open Journal of the Industrial Electronics Society 1 (2020): 127-137.

[24] Khosroshahi, Mahdi Toopchi, Ali Ajami, Ata Ollah Mokhberdoran, and Mohammadreza Jannati OsKuee. "Multilevel hybrid cascaded-stack inverter with substantial reduction in switches number and power losses." Turkish Journal of Electrical Engineering & Computer Sciences 23, no. 4 (2015): 987-1000.

[25] Hossein zadeh, Mohammad Ali, Maryam Sarbanzadeh, Elham Sarbanzadeh, Marco Rivera, and Patrick Wheeler. "New Asymmetric Cascaded Multi-level Converter with Reduced Components." In 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), pp. 1-6. IEEE, 2018.

[26] Karasani, Raghavendra Reddy, Vijay B. Borghate, Prafullachandra M. Meshram, and H. M. Suryawanshi. "A modified switched-diode topology for cascaded multilevel inverters." Journal of Power Electronics 16, no. 5 (2016): 1706-1715.

[27] Meraj, Sheikh Tanzim, Nor Zaihar Yahaya, Kamrul Hasan, and Ammar Masaooud. "A hybrid T-type (HT-type) multilevel inverter with reduced components." Ain Shams Engineering Journal (2021).

[28] Thiruvengadam, Annamalai. "An enhanced H-bridge multilevel inverter with reduced THD, conduction, and switching losses using sinusoidal tracking algorithm." Energies 12, no. 1 (2019): 81.

[29] Siddique, Marif Daula, Saad Mekhilef, Noraisyah Mohamed Shah, Adil Sarwar, Atif Iqbal, and Mudasir Ahmed Memon. "A new multilevel inverter topology with reduce switch count." IEEE Access 7 (2019): 58584-58594.

[30] Siddique, Marif Daula, Saad Mekhilef, Noraisyah Mohamed Shah, Adil Sarwar, and Mudasir Ahmed Memon. "A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress." International Transactions on Electrical Energy Systems 30, no. 2 (2020): e12191.

[31] Hosseini Montazer, Babak, Javad Olamaei, Majid Hosseinpour, and Babak Mozafari. "A generalized diode containing bidirectional topology for multilevel inverter with reduced switches and power loss." International Journal of Circuit Theory and Applications.

[32] Samadaei, Emad, Mohammad Kaviani, and Kent Bertilsson. "A 13-levels module (K-type) with two DC sources for multilevel inverters." IEEE Transactions on Industrial Electronics 66, no. 7 (2018): 5186-5196.

[33] Barbie, Eli, Raul Rabinovic, and Alon Kuperman. "Analytical Formulation and Minimization of Voltage THD in Staircase Modulated Multilevel Inverters With Variable DC Ratios." IEEE Access 8 (2020): 208861-208878.

[34] Hossein zadeh, Mohammad Ali, Maryam Sarebanzadeh, Marco Rivera, Ebrahim Babaei, and Patrick Wheeler. "A reduced single-phase switched-diode cascaded multilevel inverter." IEEE Journal of Emerging and Selected Topics in Power Electronics (2020).

[35] Huang, Jing, and Keith A. Corzine. "Extended operation of flying capacitor multilevel inverters."
IEEE Transactions on power electronics 21, no. 1 (2006): 140-147.

[36] Hamidi, Muhammad Najwan, Dahaman Ishak, Muhammad Ammirrul Atiqi Mohd Zainuri, and Chia Ai Ooi. "An asymmetrical multilevel inverter with optimum number of components based on new basic structure for photovoltaic renewable energy system." Solar Energy 204 (2020): 13-25.

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