Induced quantum dot probe for material characterization

Yun-Pil Shim,1,2 Rusko Ruskov,1,2 Hilary M. Hurst,1 and Charles Tahan1
1) Laboratory for Physical Sciences, College Park, Maryland 20740, USA
2) Department of Physics, University of Maryland, College Park, Maryland 20742, USA

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We propose a non-destructive means of characterizing quantum dot parameters across a semiconductor wafer by inducing a quantum dot on the material system of interest with a separate probe chip that can also house the measurement circuitry. We show that a single wire can create the dot, determine if an electron is present, and be used to measure critical device parameters. Adding more wires enables more complicated setup and measurements. As one application for this concept we consider silicon metal-oxide-semiconductor and silicon/silicon-germanium quantum dot qubits relevant to quantum computing and show how to measure low-lying excited states (so-called “valley” states) in a novel way. The approach provides a simple and flexible method for characterization applicable to various quantum systems.

Semiconductor heterostructures often serve as the substrate for many solid-state devices. For quantum devices such as qubits, their quality depends crucially on the properties of the wafers. Often, these qubit characterization parameters can only be ascertained by fabricating the device and measuring it at cryogenic temperatures. Quantum dots (QDs) in silicon for quantum computing (QC) are a great example. The indirect band-gap of silicon creates low-lying excited states in the QD heterostructure; if this “valley splitting” is too small, initialization, readout and even gate operation of the qubits is impeded. Optimizing the valley splitting of silicon QD qubits—in addition to other important parameters such as coherence time, charge noise, etc.—is needed for the eventual construction of quantum computers, and is limited by the design-fabrication-test cycle time.

We propose a method of characterizing material properties using a separate probe chip that both creates the dot(s) and measures them. This concept was inspired by the ion trap approach where an ion qubit is trapped on a stylus-like tip that can be brought close to a material to characterize its properties, and also by the scanning nitrogen-vacancy (NV) center tip which can be used to detect magnetic fields at nanoscale for imaging or couple to spin qubits. While these ideas involve putting a qubit on the scanning tip itself, our scheme uses a separate gate chip to induce a qubit in the material structure under study, then measure those material and qubit parameters of interest using the circuits on the gate chip. Indeed, scanning tunneling microscope (STM) tips have already been used to create effective dots on the surface of InAs and, more recently, SiGe using tunneling to do spectroscopy. Here, we induce the dot qubit within the material in an environment realistic to quantum computing and consider dispersive readout for characterizing material and qubit properties.

To justify the viability of our approach we consider specifically silicon metal-oxide-semiconductor (MOS) type and silicon/silicon-germanium quantum well (QW) type structures as examples to investigate relevant properties for silicon-based qubit devices. We describe the general geometry of the heterostructure wafer and the gate chip and provide electrostatic simulations of the induced QD. Then, we show how to load the QD and detect the electron by dispersive readout using the quantum capacitance of the induced QD all with the same wire. Finally, methods for measuring the valley splitting based on a much stronger quantum capacitance of the qubit levels at spin-valley anticrossing are discussed using one or more wires.

Figure 1 shows the schematic pictures of a possible setup. The gate chip containing required trapping and measurement circuitry is placed perpendicular above a semiconductor structure, such as MOS [Fig. 1 (a)] or Si/SiGe QW structure [Fig. 1 (b)]. Applying positive voltage $V_g$ to the gate wire induces a confining electrostatic potential in the 2D quantum well in the structure [Fig. 1 (c)] and orbital wavefunctions show typical 2D QD orbital characters [Fig. 1 (d)]. Electrons can be trapped into the induced QD as was depicted by red regions in Fig. 1 (a) for MOS and (b) for QW. The energy levels of the induced QDs have nonzero second derivative w.r.t. the applied voltage (i.e. a quantum capacitance), allowing for a dispersive readout by coupling to a detector circuit which can be integrated in the gate chip.

We performed electrostatic simulation of the device using dimensions for MOS and QW devices that are typically used in experiments. For a MOS structure, a silicon oxide layer of 10nm overlays the silicon substrate of $\gg 200$ nm. For a QW structure, a strained silicon quantum well of 10nm is sandwiched between a $\gg 200$ nm SiGe substrate and a 40nm SiGe spacer which is capped by 10nm of silicon. We choose a reasonable and manufacturable gate chip design to demonstrate the main concepts in this work. The gate wire size is chosen to be $10\times10\times1$nm and 1$\mu$m long, and 10nm away from the top of the heterostructure. We considered different sizes of gate wafers as well as a bare metallic wire tip with no gate wafer for the simulations and obtained qualitatively similar results. To be specific, we present below results for the gate wire on a silicon wafer of 100nm depth and 200nm width.

To conduct measurements of useful device properties, especially for properties relevant for spin qubits, we need
to populate the induced quantum dot with a controlled number of electrons. This can be achieved in a number of different ways: e.g., (i) an electron-hole pair can be generated near the induced QD by light, and the electron is trapped to the QD while the hole is pushed away from the QD by the electrostatic force, or (ii) one can dope the semiconductor by implanting donors in a specific region (or use large “electron bath” gate\textsuperscript{13,15}) and use the dot accumulation wire to load electrons from the doped region into the QD (one could then possibly move the electron to another area on the chip as in the STM induced QD device\textsuperscript{13,15}).

We can possibly detect the charge in the QD via dispersive readout\textsuperscript{13,15} by incorporating a tank-circuit (often superconducting) resonator (typically with frequency $\omega_r$ of a few hundred MHz to a few GHz) into the gate wire and accumulated QD [e.g., Fig. 1(a)], and then sending and reflecting resonant microwaves to it. There would be no phase shift of the reflected signal from an empty dot, but if there is a trapped electron, the reflected signal will be phase shifted if the quantum capacitance of the electron energy level is large enough. We send an rf-signal (along with the DC voltage $V_g$): $V = V_g + V_1 \cos(\omega r t)$. In addition to the conventional capacitance of the gate-to-heterostructure QD, $C_{\text{MOS}}$, and a distributed parasitic capacitance $C_p$ of the gate to the ground plane, as was depicted in Fig. 1(a) and (b), there will be a quantum capacitance $C_q$ from the second derivative of the energy level $\partial^2 E_1 / \partial V_g^2$ of the induced QD, and the phase shift

FIG. 1. Schematic diagram of the device, for MOS (a) and QW (b) structures. A chip with a metallic wire or gate denoted by $M$ (and other necessary circuitry; $L$ is the inductance and $C_p$ is an unavoidable parasitic capacitance) on it is positioned above the semiconductor heterostructure to induce a QD for easy, non-invasive characterization. DC and AC voltages can be simultaneously applied to the gate wire for inducing the quantum dot and its characterization. QD confining potential and four lowest orbitals in MOS device with a DC gate voltage $V_g=0.02$V are shown in (c) and (d), respectively. Si/SiGe QW device has slightly larger QD than the MOS device for a given $V_g$ in our simulation. The position of the induced QD is slightly off the gate wire position due to the presence of the silicon wafer on which the gate wire is placed.

FIG. 2. Simulation of the QD potential and the quantum capacitance of the induced QD. (a) QD potential on MOS device, for various gate voltages $V_g=0.02, 0.2, 0.4, 0.6, 0.8, 1.0$ V from top to bottom. (b) is the QD potential for Si/SiGe QW device, for the same $V_g$ values. (c) and (d) are the second derivative of the two lowest energy levels of the induced QD for MOS and QW structures, respectively. The solid black curves are for the ground orbitals, and dashed red curves are for the first excited orbitals. $\partial^2 E_i / \partial V_g^2$ is in unit of $10^{-3}$e/V which is $1.6 \times 10^{-4}$ aF. Insets show the orbital energy splitting between two lowest orbitals vs the applied voltage $V_g$. (e) and (f) show the calculated phase shift of the reflected signal as a function of the applied voltage $V_g$ and the quality factor $Q$ of the resonator circuit for MOS and QW devices, respectively.
of the reflected signal due to $C_q$ would be

$$\Delta \phi \approx Q \frac{\delta C}{C_{\text{tot}}} \equiv Q \frac{C_q}{C_p + C_{\text{MOS}} + C_q},$$

(1)

where the Q-factor is defined via the tank-circuit relaxation $\kappa = \omega_r/Q$. Figure 2 (a) and (b) show the QD confining potentials at various $V_g$ values for MOS and QW devices, respectively. The second derivative of the orbital energy levels w.r.t. the applied magnetic field. The spin states of each valley states split due to the Zeeman splitting, and when the Zeeman splitting $E_Z$ is equal to the valley splitting $E_{VS}$, there is an anti-crossing of energy levels between the second and third levels. (b) A QD with two electrons in it has singlet and triplet states, which anti-cross at $E_Z = E_{VS}$. (c) A DQD with a single electron with tunable detuning of the dot energy levels. When the detuning reaches $\varepsilon = E_{VS}$ these anti-crossings affect the quantum capacitance and can be measured by rf-reflectometry.

Zeeman split (with energy splitting $E_Z$) into 4 levels, as was shown in Fig. 3 (a). The levels 2 and 3 (with different valley content) anti-cross when $E_Z = E_{VS}$, and the splitting at anti-crossing, $\Delta_\alpha$ can be phenomenologically parameterized with a dipole matrix element. We have estimated $\Delta_\alpha = 10^{-4} - 10^{-3} E_{VS}$, using a Rashba/Dresselhaus spin-orbit interaction induced at the heterostructure interface. This was used to describe the relaxation “hot spot” observed in the experiment, which is mainly due to acoustic phonon emission.

Given this explicit level structure we calculate the curvature of the levels with respect to the gate voltage $V_g$, obtaining the levels’ quantum capacitances, $C_{q,i}$ (this quantifies the non-linear response of the QD system). In the magnetic field at anti-crossing [Fig. 3 (a)], these quantum capacitances may be strongly enhanced w.r.t. that of the simple orbitals discussed above. The ground state has zero curvature ($C_{q,1} = 0$) from this effect, while for levels 2 and 3 one gets $C_{q,2} = -C_{q,3}$, with the capacitances sharply peaked near the anti-crossing ($\Delta_\alpha \ll E_{VS}$): $C_{q,3} \approx \frac{\alpha^2}{2\Delta_\alpha} \left[ \left( \frac{E_{VS} - E_{Z}}{\Delta_\alpha} \right)^2 + 1 \right]^{3/2}$, (using a simple model with linear dependence on $V_g$ for valley splitting and SOC constants without offset as an illustration). With the experimentally estimated $\Delta_\alpha$ and slope $\alpha$, we obtain

$$\left| C_{q,2,3} \right| = 0.1 - 1 \text{ aF},$$

(2)

which should be measurable in experiments. Another capacitance contribution may appear due to fast relaxation processes. While the relaxation rate $\Gamma_{\text{rel}}$ strongly increases at the spin-valley anti-crossing for a single electron QD (reaching $10^7 - 10^8 \text{s}^{-1}$), it is much slower than the chosen tank-circuit frequencies, $\Gamma_{\text{rel}} \ll \omega_r$, thus suppressing this capacitance contribution. A

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**FIG. 3.** Schematic energy level diagrams for valley-splitting measurement. (a) A QD with a single electron in an external magnetic field. The spin states of each valley states split due to the Zeeman splitting, and when the Zeeman splitting $E_Z$ is equal to the valley splitting $E_{VS}$, there is an anti-crossing of energy levels between the second and third levels. (b) A QD with two electrons in it has singlet and triplet states, which anti-cross at $E_Z = E_{VS}$. (c) A DQD with a single electron with tunable detuning of the dot energy levels. When the detuning reaches $\varepsilon = E_{VS}$ these anti-crossings affect the quantum capacitance and can be measured by rf-reflectometry.
way to enhance $|C_{q,2,3}|$ is to use the in-plane magnetic field with an angle such that $\Delta_3$ becomes much smaller\cite{22}, however making $\Delta_1$ smaller will narrow the region where $C_q$ is significantly non-zero.

By scanning (sweeping) the magnetic field we will register a sharp peak of phase change of the reflected signal when the Zeeman splitting is $E_Z = E_{VS}$. For this to work, we need to populate the excited states by choosing a temperature comparable to the valley splitting, e.g. for $E_{VS} = 100 \mu eV$ the temperature should be $T \sim 1 K$. Since $E_{VS} \gg \Delta_1$, the populations of the levels 2 and 3 in Fig. 3(a) will be comparable, thus leading to an effective quantum capacitance suppression by $\Delta_1/kT \sim E_{VS} \sim 10^{-3}$.

A way to mitigate these effects would be to use a single QD with two electrons. As shown in Fig. 3(b), the lowest two levels now anti-cross at $E_Z = E_{VS}$ with an anti-crossing splitting $\Delta_2^{\nu_2} = \Delta_4^{\nu_1}$ (cfr. Ref. 17), and the quantum capacitance is the same as in the 1-electron case, Eq. (2), while the relaxation is strongly suppressed at anti-crossing. Also, the suppression effect due to temperature will not be as strong as in the 1-electron case, since $kT \sim \omega_r \lesssim 1$ GHz and so $\Delta_4/kT \sim \Delta_4/\omega_r \sim 10^{-1} - 10^{-2}$. Since, however, we are in a regime $\omega_r \gg \Delta_4$ (opposite to that where a quantum capacitance approximation is valid) the effective quantum capacitance is suppressed by a form factor: $C_{q,\text{eff}} \simeq C_q (\Delta_4/\omega_r)^2$. E.g., for $E_{VS} \lesssim 100 \mu eV$ the suppression factor is $\left(\frac{\Delta_4}{\omega_r}\right)^2 \approx 1/40^2$. Thus, this method would be sufficient to measure not too small valley splitting.

An alternative method to measure the valley splitting with a slightly more complicated gate circuit is to induce a double QD using two or three gate wires on the gate chip. Let us consider a DQD with a single electron, assuming each QD has the same valley splitting. The detuning between the QDs can be changed by tuning the voltages on the two QD-defining gates. At zero detuning ($\varepsilon = 0$), one is at the degeneracy point of the lower eigenvalue v1-electrons. [v1 is the lower valley and v2 is the upper valley states. See Fig. 3(b)]. The left-right tunneling $t$ between the dots defines the splitting at anti-crossing, 2t. One then can measure the change of the reflected signal at the degeneracy point (where the energy curvature is maximal) using a tank-circuit frequency $\omega_r \ll 2t$. By sweeping the detuning to $\varepsilon = E_{VS}$ the v1-electron from the left can tunnel to the v2-level from the right. This tunneling possibility forms another anti-crossing and corresponding splitting (assume the same 2t). (This kind of tunneling is briefly discussed in Ref. 23 and then at length in Ref. 27.)

To measure the valley splitting, one starts at $\varepsilon = 0$, and populates the lowest two levels by temperature. One then moves (faster than the relaxation time $T_1$) to a detuning $\varepsilon = E_{VS}$, while sending a microwave with $\omega_r \ll 2t$, to encounter a sharp change in the reflected phase (provided that $t \ll E_{VS}$). This can be fulfilled for $2t \approx 2 - 4$ GHz and $\omega_r \approx 0.5 - 1$ GHz. Once $\varepsilon = E_{VS}$ is reached, the reflected signal changes accordingly, due to maximal quantum capacitance $C_q = \frac{e^2}{2\pi} \approx \frac{e^2}{8\pi}$ similar to the experiment of Pettersson et al.\cite{22}. The quantum capacitance at this anti-crossing is estimated of the order of 10fF, which is several orders of magnitude larger than at the spin-valley anti-crossing discussed above. In order to be able to distinguish the anti-crossings at $\varepsilon = 0$ and at $\varepsilon = E_{VS}$, one needs $E_{VS} > 2t$ which sets the lowest measurable valley splitting, $E_{VS} \gtrsim 5 - 10 \mu eV$. The main difference of this proposal from that of Ref. 27 is that the probing signal is far off resonance with the level splitting, at a constant tank-circuit frequency $\omega_r \ll 2t$, and the signature of valley splitting is easier to measure.

Finally, we note that an additional (tunable) microwave field can be introduced to the above proposed experiments to drive transitions between quantum dot states, which may allow for further or improved characterization (and also introduces another absolute energy scale to compare to, in addition to the magnetic field).

Inducing quantum dots offer the potential for non-destructive qubit characterization across a wafer, speeding optimization of materials and quantum devices such as qubits. Our concept is applicable to many different materials and systems as the inducing and measurement chip can be fabricated on a substrate different from the materials system under consideration. We showed that inducing QDs and measuring valley splitting in silicon devices are plausible with current experimental technology. Based on this concept, other materials and systems (germanium, holes instead of electrons, topological systems, etc.) and qubit approaches (encoded qubits, different readout techniques, even linear arrays of qubits making small quantum computers) can be explored without actually fabricating the quantum dots themselves.

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