Improved Gate Reliability of p-GaN Gate HEMTs by Gate Doping Engineering

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Abstract—We present a novel p-GaN gate HEMT structure with reduced hole concentration near the Schottky interface by doping engineering in MOCVD, which aims at lowering the electric field across the gate. By employing an additional unintentionally doped GaN layer, the gate leakage current is suppressed and the gate breakdown voltage is boosted from 10.6 to 14.6 V with negligible influence on the threshold voltage and on-resistance. Time-dependent gate breakdown measurements reveal that the maximum gate drive voltage increases from 6.2 to 10.6 V for a 10-year lifetime with a 1% gate failure rate. This method effectively expands the operating voltage margin of the p-GaN gate HEMTs without any other additional process steps.

Index Terms—p-GaN gate HEMT, doping engineering, gate reliability, time-dependent gate breakdown

I. INTRODUCTION

Gallium nitride (GaN) power transistors have drawn increasing attention in high-power, high-efficiency power conversion systems owing to their high breakdown voltage, fast switching speed and low ON-resistance [1-3]. In practical applications, enhancement-mode (E-mode) HEMTs with the normally-off operation are preferred for safety considerations.

Among different approaches to realize E-mode HEMTs [4-7], the p-GaN gate AlGaN/GaN HEMT emerged as a leading p-GaN gate HEMT structure Chave additionalepitaxial epi-structure and growth conditionsexcept that structure Band C adopted, as illustrated in Fig. 2(b). They have identical device structure types, named structure A, B and C, have been adopted special treatments in the gate-stacks to enhance the p-GaN gate HEMT process would be favored owing to the process simplicity.

In this work, we demonstrated that using an additional unintentionally-doped GaN (u-GaN) layer on top of p-GaN could effectively lower the electric field in the gate and thus enhance the reliability of HEMTs without additional annealing step. This u-GaN/p-GaN gate HEMT method neither impairs other electrical characteristics nor requires any extra process steps.

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II. DEVICE STRUCTURE AND FABRICATION

The p-GaN gate HEMTs were fabricated on 85 nm p-GaN/15-nm AlGaN/GaN epitaxial structure grown by metal-organic chemical vapor deposition (MOCVD) on 2-inch Si (111) substrates from Enkris Semiconductor Inc, as shown in Fig. 1(a). The p-GaN layer was doped with Mg to a concentration of \(4 \times 10^{19}\) cm\(^{-3}\). Three device structure types, named structure A, B and C, have been adopted, as illustrated in Fig. 2(b). They have identical epi-structure and growth conditions except that structure B and structure C have additional epitaxial u-GaN layers on top of the p-GaN grown by MOCVD, which was used to reduce the hole concentration in the region close to the Schottky interface with constraints on the gate driver design and resulted in lifetime reduction. It is highly desired to increase the gate BV and the \(V_{GS,\text{max}}\) for a wider gate drive window.

Several reliability studies focused on the p-GaN gate HEMTs have been carried out over the last few years [10-24]. Different failure mechanisms have been proposed, including: i) metal/p-GaN Schottky junction breakdown, which is widely accepted and most likely to happen prior to others [10-14]; ii) the passivation/p-GaN sidewall related breakdown, which is a bigger problem in self-aligned gate metal/p-GaN structure [15, 16]; and iii) p-GaN/AlGaN/GaN junction breakdown [17, 18]. Many researchers have been tackling the gate breakdown challenge with various methods [19-23]. Zhou et al. [19] and Zhang et al. [20] adopted special treatments in the gate-stacks to enhance the p-GaN/metal Schottky junction, where suppressed gate leakage currents and enhanced gate BV were achieved. An n-GaN/p-GaN/AlGaN/GaN epitaxial structure was proposed for gate reliability enhancement [22], where the Schottky junction was replaced by a metal-n-p junction. However, a high-temperature activation of p-GaN after the gate etching is required, which can be detrimental to the channel due to the strain relaxation of AlGaN [25, 26]. Thus, a technique based on the commonly used p-GaN gate HEMT process would be favored owing to the process simplicity.

In this work, we demonstrated that using an additional unintentionally-doped GaN (u-GaN) layer on top of p-GaN could effectively lower the electric field in the gate and thus enhance the reliability of HEMTs without additional annealing step. This u-GaN/p-GaN gate HEMT method neither impairs other electrical characteristics nor requires any extra process steps.

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the metal, thus widening the depletion region and reducing the maximum electric field in the GaN gate. The thicknesses of $u$-GaN were 20 and 30 nm for structure B and C, respectively. Due to the memory effect and diffusion of Mg, the $u$-GaN layers should be slightly $p$-type doping after processing [27].

The fabrication process started with a gate definition by a Cl-based plasma etch. Devices with structure A, B and C have an identical fabrication process except that B and C have longer GaN etching times. Thanks to the high-selectivity and low etching rate of the etching recipe, a smooth AlGaN surface with low etching damages has been obtained for all three structures (Fig. 2(b)). After the gate contact window opening, a Schottky-type contact was formed between the Ti/Au and the GaN gate. The devices tested feature a gate width ($W_G$) of 100 μm, a gate length ($L_G$) of 5 μm, a gate-source distance ($L_{GS}$) of 5 μm, and a gate-drain distance ($L_{GD}$) of 15 μm. The relatively longer $L_{GS}$ compared to literature is to suppress the gate breakdown induced by the passivation/$p$-GaN sidewall [12, 15]. On-wafer characterizations were performed by a Keithley 4200 analyzer.

III. DEVICE CHARACTERIZATIONS

A. Static Performance and Temperature Dependence

Fig. 2(a) depicts the transfer characteristics of the devices with structure A, B, and C. All devices exhibit a $V_{TH}$ of ~2.1 V (defined at $I_D = 0.01\,mA/mm$), and an ON/OFF ratio larger than 104. Fig. 2(b) and (c) show the output characteristic of devices with structure A and C, in both of which a $R_{ON}$ of 22 Ω·mm is obtained. These results show that the doping engineering has a negligible effect on the conduction characteristics (e.g., $R_{ON}$ and $V_{TH}$), consistent with [12, 20]. Meanwhile, a clear impact can be observed on the gate leakage characteristics as shown in Fig. 2(a) and Fig. 3(a). Under a forward bias, the gate leakage current is dominant by the metal/GaN Schottky junction [12]. Owing to the reduced acceptor doping concentration in $u$-GaN, structure B and C show lower gate leakage under forward bias.

Fig. 3(a) compares the forward gate breakdown characteristics of A, B and C measured at 25 °C. The breakdown mechanism was determined to be Schottky junction failure [14]. Compared to A, the additional $u$-GaN layer in B has effectively boosted the BV from 10.9 V to 13.2 V. For C with a thicker $u$-GaN layer, the gate BV further reached 14.6 V. By introducing the $u$-GaN layer between the $p$-GaN and metal, the hole concentration close to the Schottky junction can be effectively decreased, which promotes a wider depletion region when a positive bias is applied. Thus, the peak electric field is lowered and the gate BV is significantly enlarged. Tallarico et al. have adopted a similar strategy by Mg doping compensation in [12]. However, no significant gate BV increase has been observed in their work. This difference can be attributed to their short $L_{GS}$ and self-aligned metal/$p$-GaN architecture, which makes the $p$-GaN sidewall vulnerable [14-16].

Fig. 3(b) shows the statistical summary of the gate BVs of structure A, B and C at 25 °C, 100 °C and 150 °C. For each temperature, at least fifteen devices were measured for each structure. All the gate BVs of the three structures show weak dependences on the temperature. These results demonstrate that the doping engineering can effectively suppress the gate leakage current and boost the gate BV without impacting the threshold voltage or any additional fabrication process.

B. TDGB Analysis

Time-dependent gate breakdown (TDGB) tests with constant voltage stresses were performed to evaluate the gate reliability of the samples with structure A (Fig. 4) and C (Fig. 5). A constant voltage is applied on the gate with $V_{DS} = 0\,V$ at room
temperature. The time-to-breakdown (t_{BD}) is defined as when the gate leakage shows a sudden increase. For each structure, three different V_{GS} were adopted (10 V, 10.2 V, 10.4 V for structure A, and 12.8 V, 13 V, 13.2 V for structure C). t_{BD} distribution can be described by the Weibull statistics. The shape factor β extracted from structure A is 0.74 - 0.82, whereas it is 0.76 - 0.87 from structure C. The comparable β values indicate a similar degradation mechanism.

The lifetime prediction was performed using the most conservative exponential law (i.e., linear fitting of the ln(t_{BD})-V_{GS} relationship), as shown in Fig. 4(b) and Fig. 5(b). Considering a 10-year lifetime at a failure level of 1%, the V_{G,max} is determined to be 6.2 V for structure A. Meanwhile, a much higher V_{G,max} of 10.6 V has been achieved in structure C. The increased applicable gate voltage range offers more gate driver design flexibility and robust gate reliability.

Fig. 6 plots V_{G,max} and the corresponding V_{TH} observed in the p-GaN gate HEMTs in this work and other p-GaN gate HEMTs in literature [10, 15-17, 22, 24]. A high V_{TH} and large V_{G,max} are particularly desired in p-GaN gate HEMTs. The V_{G,max} values are extracted by the exponential law for a 10-year lifetime at a failure rate of either 1% or 63%. Structure C demonstrates the largest V_{G,max}.

Moreover, this technique requires no additional processing step after the MOCVD growth. The proposed u-GaN/p-GaN structure is highly effective in improving the p-GaN gate HEMT reliability for high-efficiency power conversion systems.

IV. CONCLUSION

In this work, a novel p-GaN gate HEMT structure with doping engineering was proposed and investigated. By growing an additional u-GaN layer on top of the p-GaN, more robust and reliable devices with lower gate leakage currents, higher gate BV (14.6 V), larger V_{G,max} (10.6 V) were obtained, with negligible impacts on the the V_{TH}, R_{ON} and sub-threshold slopes.

REFERENCES

[1] K. J. Chen, O. Haberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, “GaN-on-Si Power Technology: Devices and Applications,” IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657759.
[2] R. Rupp, T. Laska, O. Häberlen, and M. Treu, “Application specific trade-offs for WBG SiC, GaN and high end Si power switch technologies,” in 2014 IEEE International Electron Devices Meeting, 2014, pp. 2.3.1-2.3.4, doi: 10.1109/IEDM.2014.7046965.
[3] F. Zeng, J. An, G. Zhou, W. Li, H. Wang, T. Duan, L. Jiang, and H. Yu, “A Comprehensive Review of Recent Progress on GaN High Electron Mobility Transistors: Devices, Fabrication and Reliability,” Electronics, vol. 7, no. 12, p. 377, Dec. 2018, doi: 10.3390/electronics7120377.
[4] W. Choi, O. Seok, H. Ryu, H.-Y. Cha, and K.-S. Seo, “High-voltage and low-leakage-current gate recessed normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD-SiNx/RF-sputtered-HfO2,” IEEE Electron Device Lett., vol. 35, no. 2, pp. 175–177, Feb. 2014, doi: 10.1109/LED.2013.2293579.
[5] I. Hwang, J. Kim, H. S. Choi, H. Choi, J. Lee, K. Y. Kim, J. B. Park, J. C. Lee, J. Ha, J. Oh, J. Shin, U. I. Chung, “p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current,” IEEE Electron Device Lett., vol. 34, no. 2, pp. 202–204, Feb. 2013, doi: 10.1109/LED.2012.2230312.
[6] W. Chen, K.-Y. Wong, and K. J. Chen, “Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switchmode power supply converters,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796635.
[7] B. Lee, C. Kirkpatrick, X. Yang, S. Jayanti, R. Suri, J. Roberts, and V. Misra, “Normally-off AlGaN/GaN-on-Si MOSFETs with TaN floating gates and ALD SiO2 tunnel dielectrics,” in IEDM Tech. Dig., San Francisco, CA, USA, Dec. 2010, pp. 20.6.1–20.6.4, doi: 10.1109/IEDM.2010.5703401.
[8] GaN Systems. (2019). GS66502B 650V. [Online]. Available: https://gansystems.com/gan-transistors/gs66502b/
[9] EPC. (2019). EPC2019 200V. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2019_data_sheet.pdf
[10] A. N. Tallarico, S. Stoffels, P. Magnone, N. Posthuma, E. Sangiorgi, S. Decoutere, and C. Fiegna, “Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs,” IEEE Electron Device Lett., vol. 38, no. 1, pp. 99–102, Jan. 2017, doi: 10.1109/LED.2016.2631640.
[11] A. N. Tallarico, S. Stoffels, N. Posthuma, P. Magnone, D. Marcon, S. Decoutere, E. Sangiorgi, and C. Fiegna, “PBTI in GaN-HEMTs with p-type gate: Role of the aluminum content on V_{TH} and underlying degradation mechanisms,” IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 38–44, Jan. 2018, doi: 10.1109/TED.2017.2709167.
[12] A. N. Tallarico, S. Stoffels, N. Posthuma, S. Decoutere, E. Sangiorgi, and C. Fiegna, “Threshold voltage instability in GaN HEMTs with p-type gate: Mg doping compensation,” IEEE Electron Device Lett., vol. 40, no. 4, pp. 518–521, Apr. 2019, doi: 10.1109/TED.2019.2897911.
[13] J. He, G. Tang, and K. J. Chen, “$V_{TH}$ instability of p-GaN gate HEMTs under static and dynamic gate stress,” IEEE Electron Device Lett., vol. 39, no. 10, pp. 1576–1579, Oct. 2018. doi: 10.1109/LED.2018.2867938.

[14] G. Zhou et al., “Determination of the Gate Breakdown Mechanisms in p-GaN Gate HEMTs by Multiple-Gate-Sweep Measurements,” in IEEE Transactions on Electron Devices, doi: 10.1109/TED.2021.3057007.

[15] S. Stoffels, N. Posthuma, S. Decoutere, B. Bakeroott, A. N. Tallarico, E. Sangiorgi, C. Fiegna, J. Zheng, X. Ma, M. Borgia, E. Fabris, M. Meneghini, E. Zanoni, G. Meneghesso, J. Priesol, and A. Šatka, “Perimeter Driven Transport in the pGaN Gate as a Limiting Factor for Gate Reliability,” in 2019 IEEE International Reliability Physics Symposium (IRPS), 2019, pp. 1-10, doi: 10.1109/IRPS.2019.8720411.

[16] A. N. Tallarico, S. Stoffels, N. Posthuma, B. Bakeroott, S. Decoutere, E. Sangiorgi, and C. Fiegna, ”Gate Reliability of p-GaN HEMT With Gate Metal Retraction,” IEEE Transactions on Electron Devices, vol. 66, no. 11, pp. 4829-4835, 2019, doi: 10.1109/TED.2019.2938598.

[17] M. Tapajna, O. Hilt, E. Bahat-Treidel, J. Wurfl, and J. Kuzmik, ”Gate reliability investigation in normally-off p-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress,” IEEE Electron Device Lett., vol. 37, no. 4, pp. 385–388, Apr. 2016, doi: 10.1109/LED.2016.2535133.

[18] M. Ruzzarin, M. Meneghini, A. Barbato, V. Padovan, O. Haeberlen, M. Silvestri, T. Detzel, G. Meneghesso, and E. Zanoni, “Degradation mechanisms of GaN HEMTs with p-type gate under forward gate bias overstress,” IEEE Trans. Electron Devices, vol. 65, no. 7, pp. 2778–2783, Jul. 2018, doi: 10.1109/TED.2018.2836460.

[19] G. Zhou, Z. Wan, G. Yang, Y. Jiang, R. Sokolovskij, H. Yu, and G. Xia, “Gate leakage suppression and breakdown voltage enhancement in p-GaN HEMTs using metal/graphene gates,” IEEE Trans. Electron Devices, vol. 67, no. 3, pp. 875–880, Mar. 2020, doi:10.1109/TED.2020.2968596.

[20] L. Zhang, Z. Zheng, S. Yang, W. Song, J. He and K. J. Chen, ”p-GaN Gate HEMT With Surface Reinforcement for Enhanced Gate Reliability,” in IEEE Electron Device Letters, vol. 42, no. 1, pp. 22-25, Jan. 2021, doi:10.1109/LED.2020.3037186.

[21] A. Stockman, E. Canato, A. Tajalli, M. Meneghini, G. Meneghesso, E. Zanoni, P. Mocs, and B. Bakeroott, “On the origin of the leakage current in p-gate AlGaN/GaN HEMTs,” in Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Mar. 2018, pp. 4B.5-1–4B.5-4, doi:10.1109/IRPS.2018.8353582.

[22] C. Wang, M. Hua, S. Yang, L. Zhang and K. J. Chen, ”E-mode p-n Junction/AlGaN/GaN HEMTs with Enhanced Gate Reliability,” 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020, pp. 14-17, doi: 10.1109/ISPSD46842.2020.9170039.

[23] H. Jiang, R. Zhu, Q. Lyu, and K. M. Lau, ”High-voltage p-GaN HEMTs with OFF-state blocking capability after gate breakdown,” IEEE Electron Device Lett., vol. 40, no. 4, pp. 530–533, Apr. 2019, doi: 10.1109/LED.2019.2897694.

[24] I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, C. De Santi, S. Dalcanale, J. Wurfl, E. Zanoni, and G. Meneghesso, ”Temperature-dependent strain relaxation of the AlGaN barrier in AlGaN/GaN heterostructures with and without Si3N4 surface passivation,” Appl. Phys. Lett., 2006, 88(10): 102106, doi: 10.1063/1.2186369.

[25] M. Hou, S. R. Jain, H. So, T. A. Heuser, X. Xu, A. J. Suria, and D. G. Senesky, ”Degradation of 2DEG transport properties in GaN-capped AlGaN/GaN heterostructures at 600 °C in oxidizing and inert environments,” J. Appl. Phys., 2017, 122(19): 195102., doi: 10.1063/1.5011178.

[26] H. Xing, D. S. Green, H. Yu, T. Mates, P. Koza, D. Keller, S. P. Denbaars, and U. K. Mishra, “Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapor deposition,” Japanese journal of applied physics, 42(1R), 50, doi: 10.1143/JJAP.42.50.