Introduction

With the increase in solar energy generation, photovoltaic (PV) modules are connected in series for generating high voltages and power. Solar panels, however, can be exposed to high-voltage stress up to several hundreds of volts between the grounded module frame and the solar cell. Frequent high-voltage stress causes a power drop in the modules, and this type of degradation is called potential induced degradation (PID) [1–4]. Most of the PV modules already constructed are based on p-type crystalline silicon solar cells, and the various studies on PID focus on p-type silicon solar cells and modules. Studies of the PID mechanism in p-type solar cells showed that the Na ion decoration of the stacking fault in the silicon is responsible for the decrease in the shunt resistance after the PID test [5–9]. To reduce or minimize PID, various efforts have been developed from the cell level to the system level. SiNx films used for antireflection coating on solar cells are modified to reduce its resistivity [10]. An encapsulant having high volume resistivity or different types of polymers such as polyolefin or ionomer is adopted instead of conventional ethylene vinyl acetate (EVA) [11, 12]. Chemically modified cover glass is used for the module structure [13]. Choosing proper grounding poles in a solar power system is also one of the possible solutions for PID.

Of late, to overcome the limitations in the efficiency of the silicon solar cells, studies on n-type crystalline silicon solar cells are currently being used for achieving high efficiency. However, most of the photovoltaic modules already constructed are based on p-type silicon solar cells, and there are few studies on potential induced degradation (PID) in n-type solar cells. In this study, we investigated PID in n-type silicon solar cells with a front p+ emitter. Further, the PID characteristics of n-type solar cells are compared with those of p-type solar cells. The electrical properties of PID in solar cells are observed with the light I-V, quantum efficiency (QE), and electroluminescence (EL). The possible causes for the change in the external quantum efficiency (EQE) after PID are interpreted using PC1D and are discussed by comparing the experimental results with the simulation results.

Potential induced degradation of n-type crystalline silicon solar cells with p+ front junction

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Keywords
Boron-doped emitter, n-type silicon solar cell, photovoltaic module, potential induced degradation, quantum efficiency

Abstract

N-type silicon-based solar cells are currently being used for achieving high efficiency. However, most of the photovoltaic modules already constructed are based on p-type silicon solar cells, and there are few studies on potential induced degradation (PID) in n-type solar cells. In this study, we investigated PID in n-type silicon solar cells with a front p+ emitter. Further, the PID characteristics of n-type solar cells are compared with those of p-type solar cells. The electrical properties of PID in solar cells are observed with the light I-V, quantum efficiency (QE), and electroluminescence (EL). The possible causes for the change in the external quantum efficiency (EQE) after PID are interpreted using PC1D and are discussed by comparing the experimental results with the simulation results.
solar cells are being conducted. Power conversion efficiencies of over 25% are reported with an n-type silicon-based structure [14–16]. Compared to p-type silicon solar cells, there are fewer studies on PID in n-type silicon solar cells. PID in an n-type interdigitated back contact (IBC) solar cell was first reported by SUNPOWER in 2005 [17]; the PID test results of the IBC solar cell with different poles and voltage magnitudes were reported [18]. A p-n junction is formed at the rear side of the silicon wafer in the IBC solar cells; however, the junction is located at the front side of the silicon wafer in most high-efficiency n-type solar cells such as the HIT, TOPCON, bifacial solar cell, etc. Halm et al. [19] have reported PID results for an n-type IBC solar cell with a front floating emitter, and Hara et al. [20] have reported PID results for an n-type solar cell with a front p-n junction. In addition, Yamaguchi et al. [21] showed the PID results of silicon solar modules having a rear-side emitter fabricated by turning bifacial solar cells upside down. The overall results of PID in solar cell-based n-type wafers showed similar trends. The fill factor remains similar; on the other hand, current and voltage decrease with continuous tests. PID in n-type solar cells is attributed to the surface polarization effect [17] and the increase in the surface recombination velocity. The cause of PID in n-type solar cells, however, is still unclear and needs to be verified. Therefore, a study of PID in n-type solar cells is important owing to the increasing market trend for n-type solar cells.

In this study, the PID characteristics of n-type silicon solar cells with front p-n junctions having p+ emitters are investigated and compared with those of p-type silicon solar cells. From electrical analysis such as the light I-V and QE, the PID phenomenon in n-type solar cells is observed. Further, the possible reasons for the change in the EQE after PID are interpreted using PC1D, a solar cell simulation tool. Finally, the experimental results are compared with the simulated results, and the reasons for PID in n-type solar cells are discussed.

**Experimental**

Conventional structures of bifacial silicon solar cells with a front emitter and rear back surface field (BSF) are prepared for the PID test. The base wafers used in this study are phosphorous-doped n-type Czochralski (CZ), 6-inch monocrystalline silicon. The emitter and BSF within the solar cells are fabricated by BBF3 and POCl3 furnace doping, respectively. Both sides of the doped layers are passivated with stacked layers composed of silicon oxide and silicon nitride, and the electrodes are fabricated using a conventional screen printing of Ag paste and a firing process.

To analyze the PID characteristics of n-type solar cells, tests are conducted. The PID test for the solar cell is carried out without a modulated structure because the breakdown analysis of a modulated solar cell is difficult, and the quantum efficiency (QE) results of the solar cells measured at the structure of the module are inaccurate. Hence, the PID test scheme reported in the PID mechanism study without modulation is introduced [7]. The test setup is shown in Figure 1. The EVA and cover glass are stacked on the solar cells similar to the PV modules. The temperature of each solar cell is controlled by a hot plate at 60°C. The (+) electrode is connected to the front surface of the glass, and the (−) electrode is connected to the rear side of the solar cell. The area of the (+) electrode used in the PID test is 100 cm². A 1000 V bias is applied between the front and rear electrodes for 48 h using a high-voltage source measure unit (Keithley 2410). To evaluate the electrical properties, the light I-V (Wacom Electric Co., Ltd., Tanaka, Fukaya-shi, Saitama, Japan solar simulator), QE (PV Measurements, solar cell IPCE/QE measurement system), and electroluminescence (EL) were measured.

Next, for further investigation, the transfer length method (TLM) is employed, and a capacitance–voltage (C–V) measurement is conducted. To measure the TLM, the solar cells in which PID occurred are cut using a mechanical dicing machine into sizes of 1 cm × 2 cm with only fingers in the front metal design. The resistances between two fingers with different electrode distances are measured by a prove station system and a source measure unit (Keithley 2400). To measure the C–V, a metal–insulator–silicon structure is prepared. The capacitance and conductance with the voltage are measured by an LCR meter (HP 4284A).

**Results and Discussions**

**Electrical characteristics of PID**

Figure 2 shows the light I-V curves of the n-type silicon solar cell before and after the PID test. The short circuit
current density ($J_{sc}$) and the open circuit voltage ($V_{oc}$) are mainly reduced, but the fill factor (FF) is maintained after the PID test. A similar result for PID in an n-type solar cell was reported in the literature [19–21]. Based on the result that there is no decrease in the FF for the n-type solar cell PID test and considering that the FF is mostly degraded after PID in the p-type solar cell owing to a decrease in the shunt resistance, it can be considered that the behavior of PID differs according to the type of base and emitter doping. It is reported that Na ions are introduced into the stacking faults within the emitter, n⁺ doped, in p-type silicon solar cells and form shunt paths from the base silicon to the surface of the emitter after PID [5–7]. Stacking faults can also be formed inside boron-doped emitter [22], and the possibility of forming a shunt path still existed in the n-type solar cell. Shunt resistance and FF, however, are not decreased after PID in the n-type solar cell, and it can be argued that the stacking faults in the emitter of the n-type solar cells are not active after PID. From a study of the interaction energy between the silicon doping type and the stacking faults, this phenomenon can be interpreted by the relationship between the dopant in the silicon and the stacking faults [23, 24]. P-type and n-type dopants show (−) charges and (+) charges after they are activated in the silicon, respectively. From research, it is known that p-type dopants have a weaker interaction than n-type dopants with stacking faults, and the stacking fault is broadened only when n-type dopants agglomerate and reduce the energy of the stacking fault. The passage of the Na ions through the path of the stacking fault will then be difficult or easy depending on whether the p-type or n-type dopant is near the stacking fault, respectively.

Figure 3 shows the EQE of the n-type and p-type solar cells before and after the PID test. Although the reflectance data of the solar cells are not shown here, there is no difference in the reflectance before and after the test. This result suggests that the antireflection coating (ARC) of the solar cell is not changed after the PID test in both the solar cells, and the decrease in Isc is not because of the additional reflection of the sunlight. From the EQE curve of the n-type solar cell (Fig. 3A), it can be seen that the EQE decreases only at short wavelengths below 600 nm. Hence, it is considered that the EQE decreases only at short wavelengths below 600 nm. This may be owing to the increase in the front surface recombination after PID [20]. The details will be discussed in the next section. On the other hand, the EQE of the p-type solar cell decreases in parallel for the entire wavelength after the PID test (Fig. 3B). It is reported that the EQE decreases when the shunt resistance of the solar cell is extremely low [25]. The normalized EQE curve derived from the ratio between

![Figure 2. Light I-V curves of the n-type silicon solar cell before and after the potential induced degradation test.](image1)

![Figure 3. External quantum efficiency of the (A) n-type silicon solar cell (B) p-type silicon solar cell before and after the potential induced degradation test.](image2)
the $J_{sc}$ measured by the light I-V and by the QE, however, shows no change compared to the initial curve. It is demonstrated that there is no degradation within the solar cell in the case of the p-type solar cell, and only the electrical shunt path affects the final performance after PID. It is concluded that there are different causes for PID in n-type solar cells, excluding the shunt path.

To observe the shape of the degradation, the electroluminescence (EL) is measured on the samples in which PID occurred (Fig. 4). As shown in the EL images, the entire affected area is degraded uniformly in the n-type solar cell, but local degradation spots are observed in the p-type solar cell after PID. These two differences support the opinion that only the stacking faults of the p-type solar cell are affected, but different types of degradation such as surface recombination, inversion of the emitter, and changes in the doping density occur in the n-type solar cell.

**Causes of PID in n-type silicon solar cells with p+ front junctions**

**Interpretation of EQE changes using PC1D simulation**

It is experimentally observed that the EQE of n-type solar cells at short wavelengths decreases after PID. There are three possible causes for the decrease in the EQE only at short wavelengths: (1) decrease in the emitter doping density; (2) increase in the positive fixed charge of the front passivation layer; and (3) increase in the surface recombination velocity (SRV) owing to the interface defect density. Figure 5 shows the simulated EQE results obtained by PC1D. The other material and electrical parameters are fixed, and one of the three parameters – the emitter sheet resistance, the fixed charge, or the front SRV – is varied. The initial parameters used in Figure 5A are as follows: emitter sheet resistance = 63 $\Omega/\square$, fixed charge density = 1.1E12 cm$^{-2}$, and the front SRV = 4000 cm/sec. First, by decreasing the emitter sheet resistance to 23 $\Omega/\square$, or by increasing the doping density, the simulated EQE is fitted to the experimental curve after PID (Fig. 5B). The EQE at short wavelengths can be decreased if the emitter doping density is decreased. Next, by increasing the fixed charge density in the front passivation layer to 4.95E12 cm$^{-2}$, the simulated EQE is fitted to the experimental curve (Fig. 5C). Finally, by increasing the front SRV to 45,000 cm/sec, the simulated EQE is also matched with the experimental curve (Fig. 5D). If the other parameters are fixed, the SRV indicates the interface defect density between the passivation layer and the emitter surface. In summary, it is found by simulation that three possible scenarios – increasing the doping density, increasing the fixed charge, and increasing the interface defect density – can exist for the decrease in the EQE at short wavelengths.

**Experimental proof of causes of PID in n-type solar cells**

Figure 6 shows the sheet resistance calculated by the TLM before and after the PID test. The TLM is a well-known method for measuring the contact resistance between the contact electrode and the semiconductor [26]. By comparing the resistance between two different electrodes with the distances between the electrodes, the sheet resistance is calculated. From the result, it is observed that the sheet resistance is not changed after the PID test. Therefore, the change in the doping density is not the reason for PID in n-type solar cells as seen from the simulated EQE. Further, even if considerable amounts of Na ions drift into the emitter, the Na atoms act as the n-type dopant in silicon [27]. Next, to verify the changes in the fixed charge density and the interface defect density, a capacitance–voltage (C–V) measurement is conducted. By
comparing the capacitance–voltage curves, the fixed charge density in the dielectric layer and the interface defect density can be calculated [26, 28]. The calculated results for the fixed charge density and the interface defect density before and after the PID test are shown in Figure 7. The fixed charge density increases, but the interface defect
density remains the same. From the literature, it is known that the SRV and the emitter saturation current are proportional to the interface defect density [29]. The PC1D simulation results show that the SRV increases by an order of magnitude. Although it is impossible to compare the absolute values, the fixed charge density increases within one order of magnitude. The simulation result shows that a slight increase in the fixed charge density can affect PID. When the positive fixed charge is increased, the p-type-doped emitter in the n-type silicon solar cell is depleted or inverted owing to the repulsion of the majority carrier, the (+) charged holes. The diffusion of the minority carrier toward the surface will then be easier, and the emitter saturation current can be increased. In conclusion, when a high voltage is induced between the n-type solar cell and the module frame, it is demonstrated that PID occurs owing to an increase in the fixed charge in the passivation on the surface of the front p+ junction.

Cause of increase in positive fixed charges in passivation layer

It is reported that the cause of PID in p-type solar cells is the drift of Na ions to the solar cell under an external electric field. To confirm the role of the Na ions in PID in n-type solar cells, a simple PID test is conducted. Na is directly deposited on the surface of the solar cell by thermal evaporation, and the PID test is performed with the EVA only, without the glass. For comparison, the PID test is conducted on a solar cell without a Na source. To exclude the effects of the Na ions remaining within the EVA, the EVA is immersed in deionized (DI) water for 1 day before the PID test. Although not depicted here, degradation did not occur when the same EVA was used for the PID test in a p-type solar cell. The test results are shown in Figure 8. PID occurs regardless of the Na source. Interestingly, a power drop is observed in the sample using only the EVA without the Na source. Therefore, the origin of the positive fixed charge in the passivation layer over the emitter of the n-type solar cell is not the migrated ions but the polarization owing to the dielectric property. It is speculated that PID in an n-type solar cell is inevitable. In conclusion, to reduce PID in n-type solar cells, an appropriate choice of the properties of the passivation layer is needed, minimizing the dielectric constant and enhancing the conductivity. Further, using an encapsulation material having a higher volume resistivity, the PID can be reduced by decreasing the voltage drop in the passivation layer.

Conclusion

In this study, PID in n-type solar cells with front junctions was investigated. The characteristics of PID in n-type solar cells were observed by measuring the light I-V, EQE, and EL, and by comparison with PID in p-type solar cells. The parameters that were mainly reduced were $I_{sc}$ and $V_{oc}$; there was no drop in the FF after the PID test. Further, PID occurred uniformly over the affected area, and it is understood that PID in n-type solar cells cannot be explained by known mechanisms, including stacking faults in the emitter and the formation of shunt paths. By comparing the EQE results obtained from the experiments with the PC1D simulation, three possible changes – the doping density, the fixed charge density, and the interface defect density – were suggested. It was found that an increase in the positive fixed charge in the front passivation layer was the most likely cause of PID in n-type silicon solar cells, based on the experiments. Finally, to investigate the reason for the increase in the positive fixed charge, a PID test was conducted on an incomplete module structure, and it was observed that it was not caused by migrated ions such as Na, but because of the dielectric polarization of the passivation layer. PID in n-type solar cells can be prevented by introducing a passivation layer having a higher conductivity and a lower dielectric constant.

![Figure 8](image_url). Potential induced degradation results of the n-type solar cell (A) with an Na source (glass) and (B) without an Na source using only ethylene vinyl acetate.
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Conflict of Interest
None declared.

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