Negative resistance, capacitance in Mn/SiO₂/p-Si MOS structure

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Keywords: Mn/SiO₂/p-Si, negative capacitance, dielectric properties, MOS

Abstract
In this work is that we have manufactured a new structure that had not been studied by researchers before. This structure is Mn/SiO₂/Si was synthesised by liquid phase epitaxy (LPE) as a metal-oxide-semiconductor (MOS) and can be used as a tunneling diode; demonstrated from I–V measurement and negative resistance. The structure and its characterization were examined by scanning electron microscope, XRD diffraction, C–V and I–V measurements. We studied the temperature, voltage dependence of dielectric and electrical parameters of the fabricated Mn/SiO₂/P-Si MOS device. I–V measurements for this structure display diode tunnel behavior with negative resistance. Parameters such as series resistance (Rs), permittivity (ε″), dielectric loss (ε″), a tangent of the dielectric loss factor (tan δ), real and imaginary parts of electrical modulus (M′ and M″) and ac conductivity were examined in a temperature range of 303–393 K and frequency range (10 Hz–20 MHz) under 1 Vrms applied voltage along with dc bias range of (−2.0–2.0 V). We found that thermal reordering of the interface is a reason for a continuous density of interface states with homogenous relaxation time, which in turn induced a higher sensitivity to both C and G/w response with electric field frequency. The device showed negative values for capacitance (C), dielectric loss (ε″), and dielectric loss tangent (tan δ) at all temperatures.

1. Introduction

Industrial processing of semiconductor devices is a very critical issue when it comes to the interface layer; different categories that allow different functionalities based on their layer structure can be addressed. Namely Metal-insulator-semiconductor (MIS), Metal oxide semiconductor (MOS) in which the interfacial layer plays a critical role in determining the series resistance, the interface stiffness [1] and it’s build-up electric field due to work function differences between the two layers as well as the band bending near the interface. However, the interface is physically controlled by the migration of some atoms to another following some fractal [2–4] that characterizes the segregation process and gives rise to its physical properties, the migration process of particles in the interface is typical in many other semiconductor systems, in which temperature is the main factor to determine the layer content [5–9]. Consequently, together with dielectric and electrical properties of such devices are subjective by different non-idealities [10–12], for example, the interface density of states [12–19], thickness, or homogeneity of interfacial interface layer [20–22] and temperature [23–27]. The (MIS/MOS) structure is a semiconductor substrate covered by an insulator or oxide layer such as Si₃N₄, TiO₂, SiO₂, and SnO₂, and then a metal electrode is placed which is a typical structure. The presence of the insulating layer induces an intense effect on the electrical and dielectric properties of the MOS and MIS structures [4, 28–30]. At the metal-semiconductor interface, here is a broad spectrum of energy states that are allocated in the bandgap area of the semiconductor structure. Which induce different device behavior due to alternation of local energy states; in other words, their presence is the disruption of the episodic lattice construction at the surface [13, 14, 31]. These interface states are the reason for shifting the frequency dispersion property of the C and G/w curves [32–36]. However, the oxide layer might originate border state charges by bias due to an extra electric field

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in the insulator layer that impacts both electrical and dielectric features [32, 34, 36]. The insulator or oxide layer is a compelling part of the MIS or MOS structures as its thickness affects both the applied voltage and the series resistance in addition to the distribution of charges across this layer [37–39]. Consequently, the thickness of the insulator or oxide layer between metal and semiconductor determines the reliability and performance of MIS or MOS devices. By looking into C-V and G/w graphs, one can reveal information about the dielectric and electrical properties of the manufactured MOS device. The innovation in this article is that we have synthetic a construction that had not been introduced or cited by investigators before. This assembly is \( \text{Mn/\text{SiO}_2/p-Si} \) was manufactured by liquid phase epitaxy (LPE) as a metal-oxide- semiconductor (MOS) and can be used as tunneling diode as revealed from I–V measurement and negative resistance. The construction and description of this structure was inspected by scanning electron microscope, XRD diffraction, C-V and I–V measurements. This creation structure is considered new and therefore all properties are considered a unique. In this work, we measured the C and G/w as a function of temperature for different frequencies. The electrical and dielectric characterization of the \( \text{Mn/\text{SiO}_2/p-Si} \) (MOS) structure was characterized using C and G/w measurements in the temperature range of 30 °C–90 °C for dielectric properties and from 25 °C–150 °C for I–V measurements. The device characteristics were also measured at wide frequency range, to determine \( \varepsilon' \), \( \varepsilon'' \), tan \( \delta \), and M' and M'' of \( \text{Mn/\text{SiO}_2/p-Si} \) (MOS) construction, using the admittance technique [40].
2. Experimental procedure

(p-Si) Wafer single crystal of orientation (100) and resistivity 20 Ω·cm² were used to fabricate the device with dimension of 12 mm × 12 mm × 350 μm. We boiled the silicon wafer in NH₄OH + H₂O₂ + H₂O for 15 min. Then, in HCl + H₂O₂ + H₂O at 70 °C for another 10 min after, add another etching step in HF: 10 H₂O solutions to remove the oxide layer, and then we applied sonication in isopropanol and acetone,

Figure 3. XRD pattern of Mn/SiO₂/p-Si structure.

Figure 4. (a), (b) The C-V curves for the Mn/SiO₂/p-Si structure at (a) different temperatures (b) different frequencies. 4(c), (d) The G/ω-V curves for the Mn/SiO₂/p-Si structure at (c) different temperatures (d) different frequency.
respectively. The wafer is then left to dry in an argon atmosphere. The controlled thickness SiO$_2$ thin-film was formed by oxidation in a furnace in the presence of oxygen with the pressure of $2 \times 10^{-6}$ m bar at 850 °C.

### 2.1. Thin films preparation by LPE

The manufacture technologies were liquid phase epitaxy (LPE) and oxide furnace, to prepare the Mn/SiO$_2$/p-Si structure. The oxide layer of the SiO$_2$ is formed on top of the Si surface using the O$_2$ gas stream below high temperature. Mn film was deposited on SiO$_2$/p-Si substrates by LPE [41].

### 3. Results and discussion

#### 3.1. Structural properties

Figure 1 shows the structure of our MOS Mn/SiO$_2$/p-Si. This figure illustrates the three layers of the MOS structure along with the upper and lower silver paste covering the whole MOS surface to ensure good contact. Then the MOS is placed within the measuring cell of the broadband dielectric spectrometer, BDS, system (concept 40, Novocontrol, Germany) to be measured under mentioned temperature, frequency and dc bias voltage. Figure 2 shows the manganese thin film deposited on SiO$_2$/Si by liquid phase epitaxy, which appears smooth in the SEM images. It is noticed little separated islands are created rather than closed thin films. The deposited thin film is observed well covering, pinhole-free and crack-free. XRD patterns of the samples synthesized by the liquid phase epitaxy are shown in figure 3. The diffraction peaks of SiO$_2$, Mn, and Si can be identified in the XRD patterns. Moreover, the intensity of the Mn and Si diffraction peak is much higher than that of SiO$_2$. This means the degree of crystallinity of Mn is far better than that of SiO$_2$. The structure identified by x-ray diffraction forms for the epitaxial grown Mn/SiO$_2$/p-Si is revealed in figure 3. All the detected peaks were indexed in the form of both components. As shown, the form denoted only for the main structures of Si, SiO$_2$, and Mn in the lacking any new structures. The high-intensity peak in the figure is for Si with an orientation of (400). Furthermore, the figure displays the epitaxial growth of together SiO$_2$ and Mn with favored
orientations of (001) and (510), correspondingly. It is a novel structure, and therefore we have not found articles to cite.

3.2. Electrical properties

Figures 4(a)–(d) shows the measured C-V and G-W-V characteristics of the Mn/SiO₂/p-Si structure. As shown in figures 4(a), (b) shows capacitance, conductance versus applied voltage at different temperatures and frequency. Figure 4(a) shows negative capacitance values at all temperatures and applied voltage, it decreases with increasing temperature and its absolute value increases with increasing applied bias voltage. Which is
clearly seen from the \( G/\omega \) values increase with increasing temperature and applied bias voltage as shown in figure 4(c). The negative capacitance has many applications in numerous semiconductor devices, for example, detectors even in organic or inorganic semiconductor devices, (MOS), MS (LEDs), Schottky diodes, metal/polymer/semiconductor, heterojunction, \([42]\).

The inductive behavior of the materials from which such devices are formed is thought to cause such a negative capacitance behavior. Also, the accumulation region in the interface can lead to the reduction of the charge carriers at the electrodes \([43]\). Vural et al \([44]\) provided clarification for the negative capacitance, version to which the capacitance of some junction (C) can be defined by \( C = dQ/dV \). The diffusion process is sometimes exceeded by radiative recombination during forwarding bias. Consequently, the capacitance of this junction will be negative since \( dV \) necessity is positive altogether periods. At the exceptional values of the biasing voltage, the junction voltage got the fullness, and so the lesser values of \( dV \) and the exceptional values of capacitance. For the perfect diode, forward biasing voltage increases the minority carrier intensity exponentially, and henceforth, additional carriers are inserted. Such a procedure improves the recombination velocity at this junction. The overhead condition clues to the maximum and falls to be in negative values \([42–44]\). Change in

Figure 7. (a) \( \varepsilon' - V \), (b) \( \varepsilon'' - V \) and (c) \( \tan \delta - V \) curves for the Mn/SiO2/p-Si structure at different Frequencies.
capacities and $G/\omega$ with applied voltage and different frequency as shown in figures 4(b), (d) was very slight at high frequency. But increase with decrease frequency, and increase with increasing applied voltage.

Figures 5(a), (b) show $C$–T and $G/\omega$–T with different frequency; it is noticed the capacitance and $G/\omega$ increase with decreasing frequency and increasing temperature. This consequence can be ascribed in detail that the edge states subsequent the AC sign at all frequencies and this means an extra capacitance exists in adding to the space charges [44–48].

Furthermore, as shown in figure 4(c) the $G/\omega$–V characteristics of Mn/SiO$_2$–p–Si structure increased with increasing temperature depending on the applied bias voltage. Such performance is attributed to the reorganization of the edge state densities and Rs. Additionally, this exact $G/\omega$–V manners might be indorsed to a specific spreading of the interface states amid metal-semiconductor layers [34, 48, 49].

Figure 8. (a) $\varepsilon'$–T, (b) The $\varepsilon''$–T and (c) tan $\delta$–T curves for the Mn/SiO$_2$–p–Si structure at different temperatures.
Figures 6(a)–(c) shows the ě′-V, ě″-V, and tan δ-V of the MOS capacitor at different temperatures. As seen in figure 6(a), the values of ě′ are negative, like what happened in capacitance [43, 44, 50] and its absolute values increase with both bias voltage and temperature. In figure 6(b), the values of ě″ increase with increasing both temperature and applied voltage. In figure 6(c), shows tan δ-V the values of tan δ are negative, as mentioned before [43, 44] in capacitance and permittivity.

In figures 7(a)–(c) shows the ě′-V, ě″-V and tan δ-V of the MOS capacitor at a different frequency, the values of ě′, ě″ and tan δ increase with decreasing frequency and raise with raising the bias voltage, but remain constant at high frequencies because of the properties of surface conditions or polarization procedures and Rs of the construction or interfacial oxide layer, correspondingly. In other words, the variations of the ě′, ě″, and tan δ by frequency are the outcomes of the presence of the Nss and likely dipole and surface polarization [51, 52].

Figures 8(a)–(c) shows ě′-T, ě″-T and tan δ-T of Mn/SiO2/p-Si (MOS) with different frequencies. The values of ě′, ě″ and tan δ increase with increasing temperature especially in low frequency, Rising temperature enhances the appearance of imperfections/disorders effect in the lattice, adding to the mobility of the majority charge carriers (ions and electrons) which increase too by the escalating temperature. All these factors increase ě′ and ě″ values with increasing temperature. The increased concentration of the charge carriers influences the space charge effect [53–57]. Otherwise, while the tan δ decreases with increment frequency and nearly free temperature particularly at high frequencies [31, 58, 59].

Figures 9(a), (b) M′-V and M″-V the values of M′ and M″ display peaks in the high frequency and low bias voltage. The values of the actual share of electrical modulus result in M′ a characteristic peak at high frequencies due to the reorganization and rearrangement of the charges at the surface states below an exterior dc voltage or electric field [60–64].

Rs-V, Rs-T are shown in figures 10(a), (b) for various temperatures and frequencies. Figure 10(a), Rs increases with decreasing temperature; i.e. the device is having a metallic behavior. Also, Rs gives a peak in the voltage range of −1 to 0 V depending on temperature, shifting towards positive bias. Figure 9(b) shows the values of Rs as a function of temperature for different frequencies, Rs increase with decreasing frequency and decreases with increasing temperature.

Figure 11 displays σac versus T of Mn/SiO2/p-Si at different frequencies. The σac raise with raising both temperature and frequency. It is branded that the conductivity is proportional with increment of temperature,
settling the thermal steadiness of the Mn/SiO$_2$/p-Si and signifying that the procedure of dielectric polarization in MOS device receipts place through a mechanism alike to the conduction procedure [65–68]. It also noticeable that electrical conductivity usually rises with growing frequency. Like performance was detected in the literature [65–67]. The decrement in series resistance with increasing frequency causes this behavior [68]. Figure 12 shows a current-voltage characteristic (I–V) plot for MOS structure Mn/SiO$_2$/p-Si. From this figure, the I–V characteristic shows a rectifying behavior of tunnel diode. Tunnel diode displays negative resistance as shown in figure 12 inset. This is the significant property of diode because instead of absorbing power, a negative resistance
product power. In tunnel diode, the electric current is produced by ‘Tunneling’. The tunnel diode is used as a very fast switching device in computers. It is also used in high-frequency oscillators and amplifiers [69–71].

4. Conclusion

The Mn/SiO₂/p-Si structure was synthesized by liquid phase epitaxy (LPE), for the first time. This metal–oxide–semiconductor (MOS) can be used a tunneling diode as demonstrated from I–V measurement and negative resistance. The structure and characterization of this structure were examined by scanning electron microscope, XRD diffraction, C–V and I–V measurements. I–V measurements for Mn/SiO₂/p-Si performed negative resistance and Tunneling behavior. That means when the voltage has increased the current through it decreases, electrical and dielectric properties of Mn/SiO₂/p-Si (MOS) in the temperature range (30 °C–90 °C), frequency (10 Hz–10 MHz), analyzed the major physical parameters such as the Rs, ε', ε'', M', M'' and σac conductivity by using experimental (C–V and G/ω–V) measurements. Rs of the fabricated device decreases with increasing frequency and temperature. The ε', ε'', tan δ, M', M'' and σac depend on frequency, temperature, and applied voltage, ε', ε'', tan δ, increase with decreasing frequency and increase with increasing voltage and temperature. Moreover, M' and M'' rise with raising frequency and applied voltage. σac increases with rising temperature and frequency. The device showed negative values of capacitance (C), permittivity (ε'), dielectric loss tangent (tan δ) at all temperatures. The origin of negative values of (C, ε', tan δ) is due to the inductive behavior of the deliberate materials.

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