A Quadrature PLL With Phase Mismatch Calibration for 32GS/s Time-Interleaved ADC

SHUNLI MA, (Member, IEEE), TIANXIANG WU, (Student Member, IEEE), AND JUNYAN REN, (Member, IEEE)
State-Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China

Corresponding authors: Shunli Ma (shunlima@fudan.edu.cn) and Junyan Ren (junyanren@fudan.edu.cn)

This work was supported in part by the National Key Research and Development Program of China under Grant 2018YFB2202500, in part by Fudan University under Grant JIH1233034, and in part by NSFC under Grant 61934008.

ABSTRACT This article presents an accurate quadrature phase-locked loop (PLL) with quadrature phase mismatch calibration for 32 GS/s analog-to-digital converter (ADC). Due to the mismatches of clock distribution in layout and variations of the active devices, the quadrature phase of the sampling clock is significantly deteriorated. To solve the problem, a novel quadrature divider with phase calibration is induced in PLL loop. Moreover, a theoretical model of the quadrature divider is proposed to predict the performance and potential ability for phase calibration. Based on the theoretical and model analysis, the proposed PLL can realize accurate quadrature phase for high-speed real-time sampling system. The output frequency of PLL is 8 GHz with quadrature phases for 32 GS/s sampling rate. The proposed clock can realize 8-bit signal to noise ratio requirement with 16 GHz bandwidth. The proposed PLL was fabricated in 65-nm CMOS process with 28 mW dc power consumption under 1.2 V supply voltage. Testing results show that the phase noise of the clock is $-127$ dBc/Hz @10 MHz-offset frequency when the sampling speed is 27.4 GS/s. With proposed methods, the range of the phase error calibration is around $\pm20^\circ$.

INDEX TERMS Phase locked loop (PLL), quadrature phase, jitter, phase noise, quadrature divider, time-interleaved sampling, voltage-controlled oscillator (VCO).

I. INTRODUCTION

Nowadays, with the large amount of internet of thing (IoT) and wideband of 5G-communication technology, the bandwidth of the signals is getting wider and wider. To analyze these wideband signals with complex modulation types, the broadband analog to digital converters (ADCs) [1]–[3] are widely utilized to sampling the signals. The chips related to the sampling systems of the ADCs are widely implemented by GaAs process due to their high-speed characteristics. However, due to the limited integration capability, the price of the module for high-speed sampling is too expensive to be widely utilized. High-speed and real-time sampling circuits are the front-end part of oscilloscope, which consists of the high-speed track-and-hold amplifier (THA) and sampling clock. The function of the THA is to sample the wideband analog signals and the sampled voltages are converted into digital codes by analog to digital converter (ADC).

Due to the limited conversion speed of a single-channel ADC, time-interleaved technique is widely utilized. For example, article [3] shows a 56 GS/s ADC with 256 parallel channels and speed of each channel is only several hundred MS/s. With this time-interleaved structure, the high-speed sampling system design challenge moves to front-end THA design and clock distribution. Because the signal to noise ratio (SNR) of the sampling system performance is dramatically related to the clock jitter and clock skew between these channels, the clock sources are very important. A time-interleaved 6-bit THAs with 32 GS/s for high-speed sampling system is implemented in article [4] and the clock generation for the time-interleaved sampling system is analyzed and optimized in this article. The time-interleaved sampling clock generally requires multiple phases and each phase is utilized to sample the signal for an individual THA.

The sampling structure can be classified into three structures based on the clock distribution structure. The most widely utilized structure is directly multi-phase sampling [5] with low resolution. There is a trade-off between the number
of the THA and its SNR. Because the sampling time error between channels dramatically increases with large number of the channels due to the circuit variation and the asymmetry clock tree. Though the clock skews between differences sampling channels can be calibrated and the clock locates exactly sampling time to reduce the sampling error, the calibration algorithm is complex and needs extra chip area and power [6]. The SNR of this structure is limited to 6–8 bits after calibration. The secondly structure is full-rate sampling structure. Compared with the directing multi-phase sampling, the full-rate system can reduce the phase error without calibration. However, the front-end high-speed sampler is sensitive to the jitter of the sampling clock and the speed of the THA is difficult to implement. Based the above system analysis, quadrature-rate samplers with hierarchy sampling structure can unify two superiorities and the design challenge of the sampling system is quadrature phase clock with low clock jitter, low clock skew and high stability over process, voltage and temperature (PVT) variation [6]–[10].

Compared with the clock implemented by the voltage-controlled oscillator (VCO), phase locked loop (PLL) has more advantages because it can stabilize the frequency and phase over long time and PVT variation. Moreover, the PLL loop can filter the low frequency jitter of the VCO and optimize integration root mean square (RMS) jitter of the clock. Compared with the deterministic phase error, the jitter of the sampling system is random and difficult to suppress. In this article, the phase noise of the PLL is systematically optimize. However, the sampling phase error of the quadrature signals cannot be calibrated which are induced by the asymmetry layout and device mismatches.

In traditional method, the phase error calibrations require complex calibration algorithms that are complicated and power consumption in digital domain. In this article, the proposed chip is verified the phase skew calibration with an efficient structure with good results. To realize the phase skew calibration, the resolution of phase skew calibration circuit should be good enough. Traditional phase error calibration is realized by tuning the time delay of the inverter chain or phase of the phase shifter. However, resolution of conventional method is limited to picosecond. To overcome this limitation, this article overcome above problems and proposed an injection-locked quadrature divider with quadrature phase mismatch calibration as shown in Fig. 1.

This article is organized as follows. Section II presents the phase noise optimum of each blocks in PLL. Section III proposed the working principle and quadrature divider model for phase error calibration based on injection locking structure. Section IV shows circuits implements of the proposed quadrature PLL. Measurements results are shown in Section V and conclusions will be drawn in Section VI.

II. PHASE NOISE AND CLOCK JITTER ANALYSIS

With 32 GS/s sampling speed and 48 dB signal-to-noise ratios (SNR) requirements, an extremely low aperture jitter sampling clocks is essential. In this section, the theoretical phase noise optimizing of each block for sampling clock will be presented.

A. ANALYSIS OF THE SNR PERFORMANCE RELATED TO CLOCK JITTER AND PHASE NOISE

The spectrum purity of the PLL is often described in terms of phase noise rather than time jitter [4]. The phase noise shows the noise power in a 1-Hz bandwidth as a function of frequency as shown in Fig. 2(a)-(b) and it is defined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset \( f_m \) to the sampling clock signal amplitude at frequency \( f_c \). Compared to jitter characterizing time domain uncertainty, phase noise describing the signal purity in frequency domain is more widely used in radio frequency. The reason is that the phase noise is easier to be captured and measured by equipment with many practical methods. However, the accurate measurement of jitter needs high-speed oscilloscope whose sampling speed is at least 5 times of single bandwidth. What is
more, enough sampling data is required to capture the history of data to analyze. Because the phase noise of each building blocks in PLL loop can be well calculated, it is meaningful to develop an accurate method for converting the time jitter into phase noise of sampling clocks. The performances (SNR, SFDR, and THD) of time-interleaved ADCs are degraded by the jitter and phase skew of the clock [7].

Jitter in the sampling clock means uncertainty in the exact sample moment and the deviation from the ideal sampling moment leads to a voltage error in the sampled voltage. The sampling process is a multiplication of the sampling clock and the analog input signal. The multiplication is realized in the time domain and it is equivalent of the sampling clock moment leads to a voltage error in the sampled voltage. The sample moment and the deviation from the ideal sampling moment leads to the jitter and phase skew of the clock [7].

Phase noise induced by each building block is referred to its phase noise model of the PLL in phase domain.

In this article, the quadrature PLL is utilized to reduce the low phase noise at the reference oscillator as a function of the frequency offset. The low phase noise contributes to RMS phase jitter that can be expressed as

$$\Delta T_{RMS} (N) = \sqrt{\frac{2.10 \times 10^{-10}}{2\pi f_c}}$$

where \( f_c \) is carrier frequency, \( L(f) \) is the function of the phase noise. The low phase noise degrades the fundamental signal into several frequency bins and reduce the overall spectral resolution. The flat and high phase noise increases the noise floor and degrades overall SNR. To optimize the SNR, PLL can be utilized to reduce the low phase noise by filtering the low phase noise of the oscillator. The flat and high phase noise is realized by reducing the phase noise in each block.

**B. PHASE NOISE ANALYSIS OF EACH BLOCKS AND NOISE OPTIMIZING**

In this article, the quadrature PLL is utilized to reduce the low phase noise of the oscillator. The low phase noise contributes to RMS phase jitter that can be expressed as

$$H_{ol} (s) = \frac{K_{pd}K_{vco}Z_f(s)}{N.s}$$

Phased noise induced by each building block is referred to its output \( \theta_{out} (s) \). Based on the phase noise analysis, the phase noise contribution of each block is analyzed and optimized.

1) PHASE NOISE FROM REFERENCE \( \Theta_{in} (s) \)

The phase-noise contribution of the reference oscillator as a function of the frequency offset \( \Delta f_m \) is modeled by

$$S_{REF} (f) = S_{REF} (\Delta f_m) \frac{\Delta f_m^2}{f_c^2} + S_{REF, floor}$$

where \( f_c \) is reference frequency and an electrostatic-discharge-protected CMOS inverter is utilized for ESD protection as shown in Fig. 4. The reference buffer converts the crystal oscillator signal into a rectangular signal. To reduce the noise contribution by the buffer. The transconductance of the transistors should be large enough to reduce the transition
S. Ma et al.: Quadrature PLL With Phase Mismatch Calibration for 32GS/s Time-Interleaved ADC

FIGURE 4. The phase noise model of the input buffer, the noise sources include PMOS, NMOS and diodes.

FIGURE 5. The noise model of the charge pump. The noise of the current sources is modulated by the voltage pulse of the PFD.

time from sinusoidal wave to rectangle waveform making this noise negligible. Its noise transfer function is expressed as

\[ H_{REF}(s) = N \frac{H_{ol}(s)}{1 + H_{ol}(s)} \]  

(6)

It is low pass filter for input reference phase noise. The only way to reduce it is using high quality crystal oscillator and high gain input buffer to reduce the transition time.

2) CHARGE PUMP (CP) NOISE \( i_{cp}(s) \)

The model of CP is shown in Fig. 5 It converts the instantaneous phase difference to current pulses and the charge box is delivered to the loop filter. The nonlinearity of the CP will induce the incorrect amount of charge and this distorts the CP current introduces reference spur. The reference spur can also degrade the purity of the PLL output. A CP has both broadband noise and flicker noise. After the PLL locked, the CP output pulse width \( \tau \) is a certain value determined by the reset time of the PFD and its frequency is same as the input reference frequency. The current source consists of the flicker noise and white noise which can be expressed as

\[ i_{n.w}^2 = 4kT \left( \frac{2}{3} \right) g_m + \frac{K}{WLC_{ox}} g_m^2 \]  

(7)

where \( k \) is Boltzmann’s constant, \( T \) is temperature, the \( g_m \) is the transconductance of the current source, the \( W/L \) is the geometry of the devices, \( C_{ox} \) is the unity capacitance of the gate, and \( K \) is an empirical number.

Typically, the flicker noise corner is below the reference frequency and the flicker noise oversampled. The broadband white noise is under-sampled. To derive the output spectrum of sampled broadband noise of the CP, the output PSD of the sampled broadband noise and flicker noise can be expressed as

\[ \begin{align*}
    i_{out}^2 & = i_{out, w}^2 + i_{out, 1/f}^2 \\
    i_{out, w}^2 & = (i_{cp, w}^2 + i_{cp, 1/f}^2) \frac{\tau}{T_{ref}} \\
    i_{out, 1/f}^2 & = \left( i_{cp, w}^2 + i_{cp, 1/f}^2 \right) \frac{T_{ref}}{\tau} \\
    \end{align*} \]

(8)

where the \( T_{ref} \) is the period of the reference clock, \( i_{cp, w}^2 \) is the white noise spectrum and the \( i_{cp, 1/f}^2 \) is the flicker noise. Its noise transfer function is expressed as

\[ H_{CP}(s) = \frac{N}{K_{pd}} \frac{H_{ol}(s)}{1 + H_{ol}(s)} \]  

(9)

It is low pass characteristic. After noise optimum, the current is 200 \( \mu \)A.

3) LP FILTER NOISE ANALYSIS

For the sake of simplicity and completeness a three-order passive loop filter as shown in Fig. 6. This noise analysis due to thermal noise of the resistors, is given by

\[ \begin{align*}
    v_{n,R1}^2 & = 4KTR_1 \left( \frac{C_1}{(sC_1C_2R_1 + C_1 + C_2) (1 + sR_3C_3) + C_3 (sC_1R_1 + 1)} \right)^2 \\
    v_{n,R3}^2 & = 4KTR_3 \\
    \end{align*} \]

(10)
4) VCO PHASE NOISE ANALYSIS $\theta_{vco}$ (5)

Cross-coupled transistors are utilized in VCO and the noise are contributed by the active devices. The phase noise performance of the VCO is also determined by quality factor of the inductor and capacitor and its phase noise can be expressed as

$$S_{vco}(f_m) = \frac{FkT}{P_s} \left[ 1 + \frac{1}{f_m^2} \left( \frac{F_{out}}{2Q_L} \right)^2 \right] \left( 1 + \frac{f_c}{f_m} \right)$$

where $P_s$ is average power dissipated in the resistive part of the tank, $Q_L$ is quality factor of the VCO, $f_m$ is frequency offset from carrier, $f_c$ is oscillator carrier frequency, and $F$ is the empirical parameter. Its noise transfer function is expressed as

$$H_{VCO} = \frac{1}{1 + H_{ol}(s)}$$

Its noise transfer function is high-pass characteristic. Thus, lower loop bandwidth can filter more low frequency noise of the VCO. However, it is sacrificing the locking time.

5) DIVIDER PHASE NOISE ANALYSIS $\theta_{div}$ (5)

The divider structures are static source-coupled logic (SCL) dividers and true single-phase clock logic (TSPC) divider. The noise sources of SCL are mainly contributed by the loading resistors and the phase noise of the TSPC divider is sensitive to the slow slope of the waveform at the zero crossings. The resulting jitter and transfer function are expressed as

$$\sigma_{jtot}^2 = \frac{2kTCL}{I_B^2}$$

$$H_{div}(s) = -\frac{N}{1 + H_{ol}(s)}$$

where the $C_L$ is the loading capacitor and $I_B$ is the bias current as shown in Fig. 7. The noise transfer function is also low pass filter characteristic. The jitter is the ratio between the noise power of the capacitors and the square of the bias current. Because the load capacitor is certain, and the noise is inverse proportional to the bias current, thus increasing the bias current reduces the jitter.

Because different blocks noise has different transfer function and several trade-offs exists in the loop. Based on the system analysis, the phase noise of the total is shown in Fig. 8.

III. QUADRATURE PHASE MISMATCH CALIBRATION

The quadrature phase error degrades the SNR and cannot be filtered by the PLL loop. After the phase noise optimizing, the phase skew should be minimized for time-interleaved sampling. The quadrature phase can be generated by three methods. First method is utilizing the differential outputs of the VCO to drive a passive RC-CR phase shifter [13], [14]. However, the phase shifter attenuates the high frequency signals and has weak drivability. Thus, high gain buffers are needed which consume large power and degrade the phase noise performance. The second method is using QVCO to generate quadrature signals [15]. However, its quadrature phase and phase noise are highly correlated. Thus, the quadrature phase is difficult to be calibrated. The third method is using quadrature divider to generate quadrature signals. Because its quadrature phase and phase noise are independently [16]–[19]. With the novel divider circuit structure, the quadrature phase error can be calibrated.

A. CONVENTIONAL PHASE SKEW CALIBRATION METHODS

Due to the asymmetry of clock distribution in layout and active devices variation in CMOS process variation, the quadrature phase has mismatches. Traditional method to
calibrate the phase skew in low frequency is inserting tunable delay cells in clock tree. The delay chain is consisted of several stage inverters. The delay of the inverter is determined by the bias current as shown in Fig. 9. With different delay cells inserted into the quadrature clock phase, the phase skew can be calibrated. However, this method is widely used in low speed digital circuit whose clock frequency is limited to several hundred MHz due to the limited bandwidth of the delay cells. Moreover, its phase skew resolution is limited to picosecond that cannot meet the requirement of this article.

The phase skew calibration for radio or even mm-wave frequency is a completely different method. Passive phase shifter [20]–[22] is widely for phase tuning due to its simple structure, low power consumption and good power linearity. Its phase tuning is realized by changing the electrical characteristics of its path or switching between different paths. Passive phase shifter consists of high-pass/low-pass network for phase shifter as shown in Fig. 10.

For the low-pass π network in Fig. 10, the normalized transmission (ABCD) matrix of the circuit can be expressed as

\[
\begin{bmatrix}
A & B \\
C & D \\
\end{bmatrix}
= \begin{bmatrix}
1 & 0 \\
\frac{\omega_0L_2}{Z_0} & 1 \\
\end{bmatrix}
\begin{bmatrix}
1 & 0 \\
\frac{\omega_0L_2}{Z_0} & 1 \\
\end{bmatrix}
\]

\[
= \begin{bmatrix}
1 - \omega_0^2C_2Z_0 & j\omega_0L_2 \\
-j(2\omega_0C_2Z_0 - \omega_0^2L_2C_2^2Z_0) & 1 - \omega_0^2C_2Z_0 \\
\end{bmatrix}
\]

(17)

With the normalized impedance and admittance of these lumped elements, where \(\omega_0\) is the center frequency and \(Z_0\) is the characteristic impedance. The forward transmission coefficient \(S_{21}\) and the phase \(\varphi\) of \(S_{21}\) are expressed with the following equations

\[
S_{21} = \frac{2}{A + B + C + D}
\]

\[
= \frac{2}{2(1 - \omega_0^2C_2Z_0) + j\left(\frac{\omega_0L_2}{Z_0} + 2\omega_0C_2Z_0 - \omega_0^2L_2C_2^2Z_0\right)}
\]

(18)

\[
\varphi = \angle S_{21}
\]

\[
= -\arctan\left[\frac{\frac{\omega_0L_2}{Z_0} + 2\omega_0C_2Z_0 - \omega_0^2L_2C_2^2Z_0}{2(1 - \omega_0^2C_2Z_0)}\right]
\]

(19)

The loss of the phase shifter \((S_{21})\) in different channels are differ in different phase state, as a result the phase shifter will introduce amplitude error. Moreover, its phase skew resolution and accurate is highly determined by the device matching. The passive devices also take large areas and not suit for multi-phase time-interleaved structure. Based on above analysis, the conventional methods do not meet the specification requirements.

B. PHASE SHIFT MODEL OF INJECTION LOCKED OSCILLATOR

A simplified model for the oscillator is shown as Fig. 11(a). The LC-tank oscillates at \(f_0 = 1/\sqrt{LC}\) if the parasitic is neglected. Transistor \(M_1\) compensates the energy losses in \(R_1\) and offers a 180° phase shift. Then the closed-loop phase shift is 360°. When a signal is injected into the oscillator, the phase shift \(\alpha\) occurs due to the disturbance and the output frequency of the LC-tank is forced to follow the input frequency [23]–[25]. When the injection frequency is in the locking frequency range, according to the phase difference in Fig. 11(a), the input and output voltage are respectively expressed as:

\[
V_{in} = V_{inj}\cos\omega_{inj}t \\
V_{out} = V_{osc}\cos(\omega_{inj}t + \alpha)
\]

(20)

(21)

where the \(V_{in}\) is input frequency, whose frequency is \(\omega_{inj}\). \(\alpha\) is the phase shifter induced by the injecting-locked oscillator. According to the model in Fig. 11(b), based on the model and its equations for the output voltage amplitude A and output

FIGURE 9. The time delay circuit in low frequency digital and analog system.

FIGURE 10. The circuit of the phase shifter in radio frequency system.
are driven by differential signals whose oscillation frequency is the twice of the desired frequency, the two LC-dividers output phases have 90° phase shifted which shown in Fig. 12. Its model can be simplified two divider models because there is no coupling between the two dividers. Based the model analysis, the equations can be expressed as:

\[ V_{in} = V_{inj} \cos (2\omega t) , \quad V_{ip} = -V_{inj} \cos (2\omega t) , \quad (24) \]
\[ V_I = V_{I0} \cos (\omega t + \alpha_I) , \quad (25) \]
\[ V_Q = V_{Q0} \cos \left(\omega t + \frac{\pi}{2} + \alpha_I \right) . \quad (26) \]

where \( V_{in/p} \) are input differential signals and \( V_{I,Q} \) are the output quadrature signals. \( \alpha_I \) is the phase shift generated by the divider.

This structure has two drawbacks [26]–[29]. Firstly, the quadrature phases are sensitive to device mismatches. Secondly, the quadrature phases are highly related to its input anti-phase signals. If input signals are not ideal anti-phase signals with phase error, the quadrature outputs have phase error. The input signals of the divider are not ideal anti-phase due to the asymmetry layout and devices mismatches of VCO and its asymmetry signals distribution.

D. PROPOSED DIVIDER MODEL WITH MATHEMATICAL ANALYSIS

In this article, we proposed a quadrature model with tunable coupling coefficient and injection coefficient between the two parts of the dividers. To make the quadrature phase insensitive to the input anti-phase signals, the other injection locked loop is induced between the two LC-dividers as shown in Fig. 13. To build a model for the quadrature LC divider, it is important to define how the two divider cores are coupled. Fig. 13 shows the quadrature divider model. We denote the two differential output voltages by \( A_1 \exp(j\phi_1) \) and \( A_2 \exp(j\phi_2) \). After a phase lag of \( \phi_1 \) and \( \phi_2 \), each output voltage determines the injection current into the other tanks which are expressed as

\[ I_{C1} = \frac{4}{\pi} I_C \exp(j (\phi_2 - \phi_1)) \quad (27) \]
\[ I_{C2} = \frac{4}{\pi} I_C \exp(j (\phi_1 - \phi_2)) \quad (28) \]

The output current of mixer is made of the mixed current of the tank and the synchronizing double frequency injected signal which are expressed as

\[ I_{m1} = -\frac{4}{2\pi} I_{m1} \exp(j (\phi_3 - \phi_1)) \quad (29) \]
\[ I_{m2} = \frac{4}{2\pi} I_{m2} \exp(j (\phi_4 - \phi_4)) \quad (30) \]

\( \phi_3 \) and \( \phi_4 \) are the phases of the current after the mixers and the phases of \( \phi_3 \) and \( \phi_4 \) are induced by the injection currents. \( 4/2\pi \) is the gain of the mixer. Based on the model of the quadrature divider as shown in Fig. 13. and equations (27)-(30). The amplitudes and phases of the quadrature divider be
expressed as

\[ R_1 C_1 \frac{dA_1}{dt} + A_1 = \frac{4R_1}{\pi} (I_1 - I C_1 \cos (\theta_2 - \theta_1 - \phi_1) \]

\[ - \frac{4}{2\pi} I_{m1} \cos (\theta_3 - \theta_1 - \phi_3) \]  

(31)

\[ R_2 C_2 \frac{dA_2}{dt} + A_2 = \frac{4R_2}{\pi} (I_2 + I C_2 \cos (\theta_1 - \theta_2 - \phi_2) \]

\[ + \frac{4}{2\pi} I_{m2} \cos (\theta_1 - \theta_4 - \phi_4) \]  

(32)

where \( R_{1,2} \) and \( C_{1,2} \) are resistance and capacitance of the two tanks, respectively, \( A_{1,2} \) are the amplitudes of the two tanks and \( \omega_{01,2} \) are the self-oscillation of the tanks which are \( 1/\sqrt{L_{1,2}C_{1,2}} \). \( \lambda_{1,2} \) are the current ratio which can be
FIGURE 14. The mathematical model of the quadrature frequency divider based on the differential equations (27)-(34).

FIGURE 15. Mathematical model numerical solution of the output voltages \( I_{C1} = I_{C2} = I_1 = I_2 = 8\text{mA}, L_1 = L_2 = 0.8\text{nH}, C_1 = C_2 = 0.5\text{pF}, Q_1 = Q_2 = 20 \).

is shown in Fig. 14. If the two oscillator cores are perfectly matched, then the phase difference between \( V_{out1} \) and \( V_{out2} \) is 90° as shown in Fig. 15.

E. QUADRATURE PHASE MISMATCH CALIBRATION

Even though the analytical solution of (31) ~ (36) is not evident, numerical solution can show us some intuitive information. The building blocks of the equations are basic mathematical symbol and an implementation in Matlab Simulink.
FIGURE 17. The schematic of the proposed quadrature divider. VI_I and VI_Q are input bias voltage and VB_I and VB_Q are coupled signals bias voltage. By tuning these voltages, the quadrature phases can be calibrated.

FIGURE 18. The circuit of the charge pumps with two amplifiers to reduce the current mismatches.

\[ \phi_{m0} + \Delta \phi_{m0}/2 \leq \phi_m \leq \phi_{m0} + \Delta \phi_{m0}/2 \]

and assume that the mismatches are small enough that the two oscillators remain locked at a common frequency. Inserting all the mismatches in (31)\sim (36), the quadrature phase error \( \Delta \theta \) is expressed as

\[
\Delta \theta \approx \cos \phi_{m0} \frac{r \cos \phi_0}{\sin \phi_0 + r + m} \frac{\Delta I}{2I} - \frac{r \cos \phi_0}{\sin \phi_0 + r + m} \frac{\Delta I_c + \Delta I_m}{2I} \\
- Q \left( \frac{1 + m^2 + 2mr \sin \phi_0 \Delta \omega_0}{\sin \phi_0 + m + r} \frac{1 + m}{\omega_0} \right) \frac{\Delta R_0}{R_0} + \frac{\Delta \phi_0}{2} + \frac{\Delta \phi_{m0}}{2}
\]

The higher the coupling factor \( m = \Delta I_c/2I, r = \Delta I_m/2I \), the smaller the quadrature error. Phase error analytical expressions (36)\sim(37) can be derived to optimize the circuit parameters and shows the simulation results when the inductors and capacitors have mismatches as shown in Fig. 16. By tuning the bias voltage VB_I/Q to compensate the \( \Delta I \) mismatch as shown in Fig. 17, the \( \Delta \theta \) can be calibrated to realize phase adjustment based on the analysis of expressions (37). Thus, it is a feasible method to compensate the phase shift due to various mismatches.

IV. CIRCUIT IMPLEMENTATION

The quadrature PLL can guarantee a long-time stability of the output frequency and the quadrature phase calibration can guarantee the quadrature phase accuracy. The section will introduce the circuit design of the proposed quadrature PLL.

A. FREQUENCY AND PHASE DETECTOR (PFD) DESIGN

Based on the inputs of the tri-state PFD are the single-end reference clock from input reference clock and the last stage divider output from the divider chain. Inverter is utilized to sharp the edge of the clock signals. The outputs of the PFD are two pairs of differential signals that are connected to the charge pump. Symmetry layout and a transmission gate are utilized to compensate the time mismatch between UP signals and DOWN signals. Based on the phase noise analysis, the PFD dead zone is eliminated with a 200 ps delay implemented by inverter chains before the reset of the D flip-flop.

B. CHARGE PUMP (CP) CIRCUIT DESIGN

A fully differential CP is utilized to reject the common-mode signals and noise. The sink and source currents source
mismatch are reduced by utilizing a rail-to-rail operational amplifier that can also reduce the charge sharing effect, simultaneously. As a result, mismatch of the charge pump is less than 1% and the output voltage range cover of 90% the power supply as shown in Fig. 18. A capacitor with one resistor is utilized to compensate the phase margin of the amplifier over the 0.1-1.1 V output voltage range. A low pass filter is utilized to filter the low frequency flicker noise and the output current of CP is 200 µA.

C. VOLTAGE CONTROLLED OSCILLATOR (VCO) CIRCUIT DESIGN

This article utilizes traditional VCO structure with single LC tank structure including inductor and negative resistor as shown in Fig. 19(a). To realize a wideband VCO that is preferred to overcome PVT variation and improve sampling frequency range. However, there is a trade-off between the phase noise and frequency tuning range because large tuning range results in high gain of VCO [30]. The VCO is sensitive to the noise due to the high gain. In order to break the trade off, digital controlled capacitor arrays (DCCA) are used. Then, several tuning curves are realized to replace one curve. In this article, two switched controlled (DCCA) are utilized to realize four tuning curves for frequency tuning. Thus, it can realize wide frequency range with low phase noise.

D. QUADRATURE DIVIDER DESIGN

The proposed quadrature divider consists of two mixers (M₀ and M₁₀) and two LC divider coupled by transistors (M₃, M₄, M₇, and M₈) as shown in Fig. 17. Because the coupled transistors (M₃,₄) and (M₇,₈) are biased at VBIₑ₋₀ voltages, another injection locked loop exists in the dividers itself which reduce the sensitive to the mismatch of the input anti-phase signal. The bias of the injection signals VI₁₋₀ also can be adjusted to compensate the phase of the mixer. A programmable divider chain is implemented to realize different the output frequency range under a same input reference frequency. Following the quadrature divider structure is current mode logic that is implemented due to its wide frequency working range [31]. True single-phase clock (TSPC) logic divider with two modes is utilized to realize the programmable divider ratio (8~15) as shown in Fig. 19(b).

V. MEASUREMENT RESULTS

The chip photo is shown in Fig. 20. The chip is connected to the testing boards by the bonding wires as shown in Fig. 21. The inductance of the bonding wires is simulated and optimized with 3-D electromagnetic High-Frequency Structure Simulator (HFSS). After the measurement is setup, the PLL feedback loop stability is measured. After PLL is locked, the phase noise and phase calibration are measured, respectively.

A. PHASE LOCKED LOOP STABILITY MEASUREMENT RESULTS

The output voltage of the last stage divider is captured to check phase alignment with the input reference clock. The control voltage of the VCO is measured to check the PLL stability. The transient signals are measured by Agilent DSOX91304A oscilloscope with 2GS/s as shown in Fig. 22. Based on the analysis of the control voltage ripple, the phase margin of the PLL is larger than 45°.

B. PHASE NOISE MEASUREMENT RESULTS

The phase noise is measured by Keysight E5052A which can measure the phase noise of the signal frequency up to
26.5 GHz. The output pads are bonded to transmission lines with 50-ohms characteristic impedance the on-PCB traces. The insertion loss of cable, bonding wires and SMA is around 3-4 dB at 8 GHz. The measurement phase noise is -101 dBc/Hz @ 1 MHz offset frequency at 6.85 GHz center frequency. The phase noise is measured as shown in Fig. 23. Compared to the summation results, the in-band phase noise is larger than the simulation results. The time-domain measurement is shown in Fig. 24.

C. QUADRATURE PHASE AND CALIBRATION MEASUREMENT RESULTS

The transient quadrature phase measurement of the quadrature divider is difficult to measure due to the high frequency

FIGURE 22. The time-domain measurement for the settling of the QPLL.

FIGURE 23. Phase noise measurement of the QPLL.

FIGURE 24. Time domain measurement for the I/Q phase without phase calibration.

FIGURE 25. (a) Time domain measurement for I/Q phase calibration. (b) The phase skew calibration range when frequency is 8 GHz.

FIGURE 26. The edge of phase range when VB_I/Q is from 0.6-1 V.
and the mismatches of bonding wires, connectors and cables. The transient signals are measured by Keysight DSOX91304A oscilloscope with 40 GS/s and 13 GHz bandwidth.

The output swings of the quadrature signals are around 200 mV from 5.4 to 8 GHz. The measured I/Q phase error caused mismatches including devices, bonding wire, PCB traces and connection cable are within \(\pm 20^\circ\) without quadrature phase calibration. The measurement shows that the calibration range is \(\pm 20^\circ\) which can fully cover the above PVT variation and meets the sampling system requirement as shown in Fig. 25-26.

VI. CONCLUSION

In this article, a design methodology for quadrature PLL for 32 GS/s time-interleaved ADC is proposed. Based on the proposed model and simulation results, the quadrature phase error is well predicted and calibrated. With the proposed calibrated methodology, the mismatches induced by the asymmetry of the layout, bonding wires, connectors and cables are well calibrated with range of \(\pm 20^\circ\) phase mismatch capability. Due to above good performance, the quadrature PLL can be suitable for four-channel time-interleaved sampling system with 8-bit SNR requirements and 16 GHz bandwidth.

REFERENCES

[1] G. Trettter, M. M. Khafaji, D. Fritsche, C. Carta, and F. Ellinger, “Design and characterization of a 3-bit 24-GS/s flash ADC in 28-nm low-power digital CMOS,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 4, pp. 1143–1152, Apr. 2016.

[2] B. Xu, Y. Zhou, and Y. Chiu, “A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS,” IEEE J. Solid-State Circuits, vol. 52, no. 4, pp. 1091–1100, Apr. 2017.

[3] K. Sun, G. Wang, Q. Zhang, S. Elahmadi, and P. Gui, “A 56-GS/s 8-bit time-interleaved ADC with ENOB and BW enhancement techniques in 28-nm CMOS,” IEEE J. Solid-State Circuits, vol. 54, no. 3, pp. 821–833, Mar. 2019.

[4] S. Ma, H. Yu, and J. Ren, “A 32.5-GS/s sampler with time-interleaved track- and-hold amplifier in 65-nm CMOS,” IEEE Trans. Microw. Theory Techn., vol. 62, no. 12, pp. 3500–3511, Dec. 2014.

[5] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, “A CMOS 6-Bit 16 GS/s time-interleaved ADC using digital background calibration techniques,” IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 848–858, Apr. 2011.

[6] T. Kihara, T. Takahashi, and T. Yoshimura, “Digital mismatch correction for bandpass sampling four-channel time-interleaved ADCs in direct-RF sampling receivers,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 6, pp. 2007–2019, Jun. 2019.

[7] M. El-Chammas and B. Murmann, “A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration,” IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[8] M. El-Chammas and B. Murmann, “General analysis on the impact of phase-skew in time-interleaved ADCs,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 5, pp. 902–910, May 2009.

[9] H.-Y. Chang, C.-C. Chan, S.-M. Li, H.-N. Yeh, I. Y.-E. Shen, and G.-L. Huang, “Design and analysis of CMOS low-phase-noise low quadrature error V-band subharmonically injection-locked quadrature FLL,” IEEE Trans. Microw. Theory Techn., vol. 66, no. 6, pp. 2851–2866, Jun. 2018.

[10] S. Ma, H. Yu, Q. J. Gu, and J. Ren, “A 5–10-Gs/12.5-mW source synchronous I/O interface with 3-D flip chip package,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 2, pp. 555–568, Feb. 2019.
SHUNLI MA  (Member, IEEE) received the B.S. degree in microelectronics engineering from Shanghai Jiaotong University, Shanghai, China, in 2011, and the Ph.D. degree in micro-electronics engineering from Fudan University, Shanghai, China, in 2016. From 2012 to 2014, he was a Project Officer with Nanyang Technological University, Singapore. From 2016 to 2017, he worked in industry and designed 77-GHz FMCW PLL for automotive radar sensor. He received the Distinguished Designer Award for mm-wave PLL design for automotive radar.

He is currently an Assistant Professor with the State Key Laboratory of ASIC and Systems, Fudan University. He has authored or coauthored many high performances mm-wave circuits articles on top conferences, including ESSCIRC, CICC, RFIC, ASSCC, and IMS. His research interests are millimeter-wave integrated-circuit design, including mm-wave imaging sensing, mm-wave PLL and high-speed sampler in ADC, and biomedical RF circuits for cancer detection. His article has received finalist at IMS’15. He received the 2015 ISSCC Student Research Preview Award and the ISSCC STGA Award.

TIANXIANG WU (Student Member, IEEE) received the B.S. degree from Anhui University, Anhui, China, in 2014, and the M.S. degree from Southeast University, Jiangsu, China, in 2017. He is currently pursuing the Ph.D. degree in micro-electronics engineering with Fudan University, China. His current research interests include the design of PLL and MoS2 circuit design.

JUNYAN REN (Member, IEEE) received the B.S. degree in physics and the M.S. degree in electronics engineering from Fudan University, Shanghai, China, in 1983 and 1986, respectively. He is currently a Senior Member with the China Institute of Communications. From 1986 to 2000, he was with the Department of Electronics Engineering, Fudan University. In 2000, he joined the Department of Microelectronics, Fudan University, where he is currently a Full Professor. Since 1992, he has been a Research Member of the State-Key Laboratory of ASIC and System. His research interests include data conversion, signal processing, and analog/RF/mixed-signal designs. He received the Excellent Subject Chief Scientists Award, the Distinguished Young Faculty Award from the Shanghai municipal government, and the Excellent Graduate Advisor Award from Fudan University.

* * *

TIANXIANG WU (Student Member, IEEE) received the B.S. degree from Anhui University, Anhui, China, in 2014, and the M.S. degree from Southeast University, Jiangsu, China, in 2017. He is currently pursuing the Ph.D. degree in micro-electronics engineering with Fudan University, China. His current research interests include the design of PLL and MoS2 circuit design.