Abstract—Multi-core processors improve performance, but they can create unpredictability owing to shared resources such as caches interfering. Cache partitioning is used to alleviate the Worst-Case Execution Time (WCET) estimation by isolating the shared cache across each thread to reduce interference. It does, however, prohibit data from being transferred between parallel threads running on different cores. In this paper we present (SRCP) a cache replacement mechanism for partitioned caches that is aware of data being shared across threads, prevents shared data from being evicted from caches. Our technique outperforms TA-DRRIP and EHIC, which are existing state-of-the-art cache replacement algorithms, by 13.34\% in cache hit-rate and 10.4\% in performance over LRU (least recently used) cache replacement policy.

Index Terms—WCET, Shared Data, Multi-cores, Cache Partitioning

I. INTRODUCTION

Multithreaded applications which share data have not been studied in partitioned caches till date. When applications share information, the benefits of partitioned caches are lessened because duplicate data is put into the partitions, wasting cache space, causing data duplication problems, and degrading cache performance.

II. PROPOSED APPROACH

A. Overview of the SRCP Framework

The SRCP framework [1] uses way partitioning to divide the shared last-level cache (LLC). We performed static partitioning in LLC, a set of cache ways assigned to each core as per equation [1].

\[
\text{Partitions allotted} = \frac{\text{Associativity}}{\text{Number of cores}}
\]  

(1)

In the SRCP-architecture unlike standard partitioned caches, non-allocated cores can access a partition but can only evict a cache block from its own partition, based on [2]. To keep a track of the accesses made to the cache blocks three counters are used, LC, GCount and AFC which are dynamically updated and used by the SRCP cache replacement algorithm. The terms used in the cache architecture are as follows:

• Local Core: The core allocated to a partition is called local core.
• Global Core: The cores other than local core are global cores for a partition.
• Local Count (LC): A single-bit indicates if a cache block is accessed by the local core.

• Access Frequency Count (AFC): This is the frequency of accesses made to a block in a cache way by the local core. We used k-bit counter, where \( k = 8 \) bits.
• Global Count (GCount): This is the number of times a cache block is accesses by global cores within the partition. It’s a n-bit counter, where \( n = \log_2(\text{no. of cores}) \) as the value.

B. Cache Hit & Miss Handling

Initially, when a requested cache block is loaded into the LLC the GCount is set to null and AFC counter in ACT is set to an intermediate value, \( I \) i.e.,

\[ I_i = \text{average(max & min values of } AFC_i) \], for \( i^{th} \) core. (2)

The AFC value of the cache block is increased by one on a hit. Equation [3] specifies the criteria for deciding between frequently utilised and less often used cache lines. A frequently used cache line is loaded into the private cache to increase the cache hits and speed. Less frequently used data is not loaded into the private cache of a core.

\[
AFC_i = \begin{cases} 
\text{freq_used,} & \text{if } AFC_i \geq I_i, \\
\text{less_freq_used,} & \text{otherwise.} 
\end{cases}
\]  

(3)

When any global cores (other than local cores) visit a cache line in a partition, the GCount is incremented by one. Based on the GCount given by equation [4] data in a cache line can be shared or private.

\[
\text{Data} = \begin{cases} 
\text{Shared,} & \text{if } GCount_i \geq 1, \\
\text{Private,} & \text{otherwise.} 
\end{cases}
\]  

(4)

The AFC & GCount values are decreased by one for all the cache blocks in the partition that incurs cache miss when there is a cache miss. As a replacement victim the block with lowest AFC value and lowest GCount value is picked. If two or more least frequently used data and least shared data are tied for the selection of a victim cache block, the minimally used block in the recent past by the local core is evicted.

C. Cache Coherence

Reads and writes on private data, which are less frequent, are bypassed in our method, as are writes on shared data. The dynamic change in application behaviour is taken into account in our method. Because the requested shared cache line will be modified, loading it in the private cache is not allowed. The write operation is done directly in the LLC, skipping the L1 cache, resulting in consistent shared data and minimising coherence overheads by retaining only one copy of the shared data.
D. WCET Analysis

Equation 5 and 6 is used to compute the WCET of shared caches and the proposed framework respectively. The overall latency of a task on a hit is denoted as, \( L_{\text{hits}} \), while \( L_{\text{miss}}^{(n-1)} \) denotes latency on a miss, which includes overheads due to threads executing in the other \((n-1)\) cores. \( L_{\text{miss}} \) is the latency of a task when run solely in the cache partition allotted to it.

\[
WCET_{\text{tot}} = \text{Cache}_{\text{hits}} \times L_{\text{hits}} + \text{Cache}_{\text{miss}} \times L_{\text{miss}}^{(n-1)} \tag{5}
\]

\[
WCET_{\text{tot}}^{\text{SRCP}} = \text{Cache}_{\text{hits}} \times L_{\text{hits}} + \text{Cache}_{\text{miss}} \times L_{\text{miss}} \tag{6}
\]

\( WCET_{\text{tot}} > WCET_{\text{tot}}^{\text{SRCP}} \) as it includes overheads caused by shared cache interference due to threads running in remaining \((n-1)\) cores.

III. EXPERIMENTAL EVALUATION

A. Experimental Setup

The proposed technique was tested using the gem5 full-system simulator. The system parameters used are same as in [1]. The multi-threaded Parsec [4] and Splash-2 [5] benchmark suites is used to assess our proposed technique. Every application was run for a total of two billion instructions, & LRU was utilised as a reference point. The benchmarks are run on four cores with four threads each running on one core, with 16-way associative LLC. Performance is measured in terms of instructions per cycle (IPC).

B. Result & Analysis

The improvements in LLC hit-rate and performance are shown in Figures 1 and 2 respectively. Figure 1 shows comparison between our approach i.e., SRCP, TA-DRRIP [6] and EHC [7] approaches with LRU as baseline. In comparison to TA-DRRIP and EHC, our technique outperforms Splash-2 and Parsec multi-threaded benchmarks. Memory access is quite low for compute heavy applications like ferret. Because threads in multi-threaded ferret do not coordinate very much, its unlikely that a cache line will be accessed more than once therefore it does not get benefited much with our approach.

In comparison to LRU, our suggested technique improves cache hit-rate by up to 13.34%, while EHC and TA-DRRIP boost cache hit-rate by 9.4% and 7.3% respectively. In multi-core CPUs for multi-threaded benchmarks, our technique delivers up to 10.4% performance gain over LRU, whereas EHC achieves 6.2% and TA-DRRIP achieves 5%.

IV. CONCLUSION

This paper presents a simulation model and it is found that our partitioned cache framework is helpful for multi-threaded applications, since it avoids duplication of shared data across cache partitions while also avoiding eviction of shared data. The simulation model uses the already existing model in the gem5 simulator and extends it to add the SRCP features.

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