Parameters Optimization of an Intermediate Frequency Isolated SiC Power DC-DC Converter

CHENGWEI KANG\(^1,2\), HONGLIANG PAN\(^1\), SHUIYUAN HE\(^3\), JIAHUI REN\(^2\), PEICHENG CONG\(^4\), DAZHI HOU\(^2\), JINGYAN ZHANG\(^2\), AND LIJUN DIAO\(^3\) (Senior Member, IEEE)

\(^1\)National Maglev Transportation Engineering Technology Research and Development Center, Tongji University, Shanghai 201804, China
\(^2\)CRRC Changchun Railway Vehicles Company Ltd., Changchun 130022, China
\(^3\)School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China
\(^4\)Shanghai CRC Rail Transportation Equipment Co., Ltd., Shanghai 200245, China

Corresponding author: Lijun Diao (ljdiao@bjtu.edu.cn)

This work was supported in part by the Science and Technology Research and Development Plan of China National Railway Group Company Ltd., under Grant L2021J001 and Grant P2020J023.

ABSTRACT To improve the lightweight level of auxiliary converters for urban rail vehicles, full SiC intermediate frequency auxiliary converters have become a trend. Aiming at its core component, a full SiC intermediate frequency isolated DC-DC converter using Boost + LLC topology is studied in this paper. The working principle and characteristics of the converter are analyzed in detail. Based on the operating characteristics of the LLC resonant converter and the realization mechanism of soft switching, an optimization design method of the resonant parameters is proposed, which can make LLC resonant converters exhibit the characteristics of DC transformers and realize soft switching in the full load range. Considering the power losses of the converter and the voltage stress of SiC MOSFET, the intermediate bus voltage design method is given. Finally, the correctness of the parameter design method is verified by simulation and experiment, and the performance of the full SiC intermediate frequency isolated DC-DC converter is analyzed. When the input voltage is 1500V and the output power is 15kW, the efficiency of the converter reaches 96.21%. Compared with the Si intermediate frequency isolated DC-DC converter, the power density is improved by 80.62%.

INDEX TERMS Auxiliary converter, intermediate frequency isolation, SiC, LLC resonant converter.

I. INTRODUCTION

To enhance the lightweight level of the auxiliary converter of urban rail vehicles, a full SiC intermediate frequency auxiliary converter combining full SiC power devices and intermediate frequency auxiliary power supply technology has become a development trend [1], [2], [3], [4], [5], and the study of its core component, the full SiC intermediate frequency isolated DC-DC converter, is more important.

The literature [6], [7] investigated full SiC intermediate frequency isolated DC-DC converters with DC 750V input using a phase-shifted full-bridge topology. In the literature [7], the full SiC intermediate frequency isolated DC-DC converter was rated at 40 kW and operated at 40 kHz, reducing the size of the magnetic components by nearly 80% compared to the silicon intermediate frequency isolated DC-DC converter that operated at only 5 kHz. In the literature [8], a full SiC intermediate frequency isolated DC-DC converter with DC 1500V input is studied, also using a phase-shifted full-bridge topology. Since the maximum withstands voltage of current commercial full SiC power modules is only 1700V, it uses two sets of phase-shifted full-bridge input-series-output-parallel (ISOP) structure. The converter is rated at 70kW and operates at 40kHz with a full load efficiency of 95%.

It should be noted that although the phase-shifted full-bridge topology has been successfully used in full SiC intermediate frequency isolated DC-DC converters, some shortcomings should be pointed out. First, the resonant states of the overrunning bridge arm and the lagging bridge arm in the phase-shifted full-bridge converter are not identical,
and the lagging bridge arm is more difficult to achieve zero-voltage turn-on of its switches [7], [8]. Second, the converter has the phenomenon of effective duty cycle loss during the primary-side commutation [7], [8]. Finally, due to the presence of the secondary filter inductor, there are large voltage spikes in the rectifier diode when it is turned off, which not only affects the system efficiency but also causes oscillations. Especially, with the adoption of SiC power devices, the operating frequency of the converter is significantly increased and the voltage spikes and oscillation problems are even worse, thus requiring additional buffering and absorption circuits [7], [8], [9]. At low power conditions, the efficiency improvement of the converter is not significant.

In this paper, an ISOP structured full SiC intermediate frequency isolated DC-DC converter composed of Boost converter + full-bridge LLC resonant converter cascade module is studied. By using full SiC power devices with very low switching losses, the operating frequency and efficiency of the Boost converter are increased, and the LLC resonant converter has excellent soft switching performance, so the system has high efficiency [1], [10]. The increase in operating frequency results in a significant reduction in the weight and size of the magnetic components in the system. Combined with the fact that LLC resonant converters do not require a secondary filter inductor, higher power densities can be achieved with this topology.

The paper firstly introduces the operating principle and characteristics of the converter; then proposes the optimization design method of the converter circuit parameters and the design method of the intermediate DC bus voltage; finally, the correctness of the above parameter design method is verified by simulation and experiment, and the performance of the full SiC intermediate frequency isolated DC-DC converter is analyzed.

II. ANALYSIS OF THE MAIN CIRCUIT TOPOLOGY

A. WORKING PRINCIPLE

Fig. 1 gives the topology of a full SiC intermediate frequency isolated DC-DC converter, which consists of two sets of Boost converter + full-bridge LLC cascade modules connected in series with inputs and parallel with outputs. To improve the system efficiency, the switching frequency and duty cycle of the full-bridge LLC resonant converter are fixed, and the resonant parameters are reasonably designed to make its DC voltage gain constant. At this time, the rear full-bridge LLC resonant converter can be regarded as a DC transformer to play the role of isolation and voltage, the output voltage is regulated by the front Boost converter. Since the input side of the two Boost converters is connected in series, the power density of the system can be further improved by reducing the Boost inductance using interleaved control. The next section analyzes the operating principle of the interleaved Boost converter and the operating principle and characteristics of the full-bridge LLC resonant converter, respectively.

According to the relationship between \( V_{in} \) and \( V_{cb} \), the interleaved Boost converter has two operating modes with duty cycle \( D_b \leq 0.5 \) and \( D_b > 0.5 \). Figure 3 gives the main operating waveforms in these two modes, \( T_{sb} \) is the switching period. In both operating modes, the drive signals of Q12 and Q22 are staggered by 180°, and the current pulsation frequency of the inductor is twice the switching frequency \( f_{sb} \).
Operating mode I ($V_{\text{in}} \geq V_{cb}$, $D_b \leq 0.5$): When $Q_{12}$ is on and $Q_{22}$ is off or $Q_{12}$ is off and $Q_{22}$ is on, $v_{Lb} = V_{\text{in}} - V_{cb}$, $i_{Lb}$ rises linearly; while when $Q_{12}$ and $Q_{22}$ are off at the same time, $v_{Lb} = V_{\text{in}} - 2V_{cb}$, $i_{Lb}$ decreases linearly. The operating waveform is shown in Fig. 3(a).

![Figure 3. Main waveforms of the interleaved Boost converter.](image)

Operating mode II ($V_{\text{in}} < V_{cb}$, $D_b > 0.5$): When $Q_{12}$ and $Q_{22}$ are turned on at the same time, $v_{Lb} = V_{\text{in}}$, $i_{Lb}$ rises linearly; while when $Q_{12}$ is turned on and $Q_{22}$ is turned off or $Q_{12}$ is turned off and $Q_{22}$ is turned on, $v_{Lb} = V_{\text{in}} - V_{cb}$, $i_{Lb}$ falls linearly. The operating waveform is shown in Fig. 3(b).

From the volt-second balance principle of the inductor voltage, it is known that the interleaved Boost converter has the same voltage gain relationship in both operating modes, as

$$V_{cb} = \frac{V_{\text{in}}}{2} \left(1 - D_b\right)$$  \hspace{1cm} (1)

And inductor current ripple $\Delta i_{Lb}/I_{Lb}$ can be expressed as

$$\begin{align*}
\Delta i_{Lb}/I_{Lb} &= \frac{2V_{cb}^2 T_{sb} D_b (2D_b^2 - 3D_b + 1)}{P_{\text{in}} L_b}, \quad D_b \leq 0.5 \\
\Delta i_{Lb}/I_{Lb} &= \frac{2V_{cb}^2 T_{sb} D_b (1 - D_b)^2 (2D_b - 1)}{P_{\text{in}} L_b}, \quad D_b > 0.5
\end{align*}$$  \hspace{1cm} (2)

where $\Delta i_{Lb}$ and $I_{Lb}$ are the pulsating and RMS values of the inductor current, respectively, and $P_{\text{in}}$ is the input power. Then the maximum $\Delta i_{Lb}/I_{Lb}$ can be derived as

$$\frac{\Delta i_{Lb}}{I_{Lb}} \leq \frac{\sqrt{3} V_{cb}^2 T_{sb}}{9 P_{\text{in}} L_b}$$  \hspace{1cm} (3)

**B. OPERATING PRINCIPLE OF FULL-BRIDGE LLC RESONANT CONVERTER**

The circuit topology of the full-bridge LLC resonant converter is shown in Fig. 4, where $V_{cb}$ and $V_o$ are its input and output voltages, respectively; $Q_1$ and $Q_3$ are the upper and lower tubes of the half-bridge SiC power module, $Q_2$ and $Q_4$ are the same, $D_1 \sim D_4$ are the body diodes of SiC MOSFETs, $C_1 \sim C_4$ are the drain-source junction capacitors of SiC MOSFETs, and the capacitance values are equal to $C_{ds}$. $L_r$ is the resonant inductor, $L_p$ is the parallel resonant inductor; $T$ is the ideal transformer, whose primary and secondary ratios are $n:1$; the secondary side is a full-bridge rectifier circuit composed of $D_{R1} \sim D_{R4}$, the output filter capacitor is $C_o$, and the equivalent load is $R_{Ld}$, $V_{cr}$ and $i_{Lr}$ are the resonant capacitor voltage and resonant current, $v_{Lp}$ and $i_{Lp}$ are the parallel resonant inductor voltage and $i_{DR}$ is the rectifier bridge output current. During the operation, $Q_1$ and $Q_4$ drive signals are the same, $Q_2$ and $Q_3$ drive signals are the same, and the upper and lower tubes of the same bridge arm are staggered 180° conduction.

Define $f_r$ as the resonant frequency of $C_r$ and $L_r$, and $f_p$ as the resonant frequency of $C_r$, $L_r$, and $L_p$, as shown in (4) and (5), respectively. The zero-voltage turn-on of SiC MOSFETs (zero-voltage-switching, ZVS) and zero-current turn-off of rectifier diodes (zero-current-switching, ZCS) can be achieved simultaneously when the switching frequency $f_s$ is between $f_p$ and $f_r$. And, the closer the $f_s$ is to $f_r$, the higher the efficiency of the converter. When $f_s = f_r$, the LLC resonant converter works at the highest efficiency point.

$$f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \hspace{1cm} (4)$$

$$f_p = \frac{1}{2\pi \sqrt{(L_p + L_r) C_r}} \hspace{1cm} (5)$$

Since there will be a slight error in the resonance parameters in practical applications, this paper chooses $f_s$ slightly less than $f_r$, when the efficiency of the full-bridge LLC resonant converter is close to the highest and can ensure good soft-switching performance. The main waveforms in this operating mode are given in Fig. 5, from which it can be seen that a switching cycle can be divided into 8 time periods in this operating mode, and the operating process is analyzed next.

Stage I [$t_0$, $t_1$]: At the moment of $t_0$, $Q_1$ and $Q_4$ turn on with zero voltage, $i_{Lr}$ is greater than $i_{Lp}$, $D_{R1}$ and $D_{R4}$ conduct, the primary side transfers energy to the secondary side, $v_{Lp}$ is clamped to $nV_o$, $i_{Lp}$ rises linearly, and only $L_r$ and $C_r$ participate in resonance. In this period, the expressions of $i_{Lr}$
and \( i_{Lp} \) are shown

\[
\begin{align*}
 i_{Lr}(t) &= I_{Lrm} \sin(\omega_r t + \theta) \\
 i_{Lp}(t) &= \frac{nV_o}{L_p} (t - t_0) - 4L_{qpf} nV_o
\end{align*}
\tag{6}
\]

where, \( \omega_r = 2\pi f_r \), is the resonant angular frequency; \( I_{Lrm} \) is the peak resonant current; \( \theta \) is the phase angle between \( i_{Lr} \) and the resonant cavity input voltage \( v_{AB} \):

\[
\theta = \sin^{-1} \left( \frac{nV_o}{4L_{qpf} I_{Lrm}} \right)
\tag{7}
\]

Stage 2 \([ t_1, t_2 ]\): At the moment of \( t_1 \), \( i_{Lr} \) and \( i_{Lp} \) are equal, the rectifier diode is turned off at zero current, \( v_{Lp} \) is no longer clamped by the output, and \( L_r, C_r, \) and \( L_p \) resonate together. Since \( L_p \) is large, the size of \( i_{Lp} \) can be considered constant in this period. In this period, the expressions of \( i_{Lr} \) and \( i_{Lp} \) are

\[
i_{Lr}(t) = i_{Lp}(t) = \frac{nV_o}{4L_{qpf}}
\]

Stage 3 \([ t_2, t_3 ]\): At the moment of \( t_2 \), \( Q_1 \) and \( Q_4 \) are turned off, \( L_p \) is renewed through the circuit formed by the resonant cavity and the junction capacitors \( C_1 \sim C_4 \). \( C_1 \) and \( C_4 \) are charged and \( C_2 \) and \( C_3 \) are discharged. At that time, \( i_{Lr} \) and \( i_{Lp} \) still satisfy (9), and the voltages of \( C_1 \sim C_4 \) are

\[
\begin{align*}
 v_{C1}(t) &= v_{C4}(t) = \frac{nV_o}{8L_{qpf} C_{ds}} (t - t_2) \\
 v_{C2}(t) &= V_{C3}(t) = V_{Ch} - \frac{nV_o}{8L_{qpf} C_{ds}} (t - t_2)
\end{align*}
\tag{9}
\]

Stage 4 \([ t_3, t_4 ]\): At the moment of \( t_3 \), the voltages of \( C_1 \) and \( C_4 \) reach \( V_{Ch} \), while the voltages of \( C_2 \) and \( C_3 \) drop to zero, creating the conditions for the zero-voltage turn-on of \( Q_2 \) and \( Q_3 \). The \( i_{Lr} \) is smaller than \( i_{Lp} \), \( D_{R2} \) and \( D_{R3} \) conduct, the primary side transfers energy to the secondary side, \( v_{Lp} \) is clamped to \( -nV_o \), \( i_{Lp} \) decreases linearly, and only \( L_r \) and \( C_r \) participate in resonance. The second half of the switching cycle, the period \([ t_4, t_5 ]\), works in the same way as the first half of the cycle and will not be repeated.

In summary, when \( i_{Lr} \) lags behind \( v_{AB} \), the resonant network is inductive, and \( i_{Lr} \) can charge and discharge \( C_1 \sim C_4 \) within the dead time \( t_d \), which is period \([ t_2, t_4] \) or \([ t_6, t_8] \), creating conditions for ZVS of SiC MOSFETs. However, to fully realize ZVS, two conditions need to be satisfied: First, the peak value of \( i_{Lp} \) should be large enough to ensure that the junction capacitance can be discharged to zero within \( t_d \), according to which the range of \( L_p \) can be obtained as (10); second, in the dead time, \( i_{Lr} \) cannot be reversed, otherwise, the junction capacitance of the SiC MOSFET will be charged immediately after it is discharged to zero, and ZVS cannot be achieved. The condition in (11) must be fulfilled to make \( i_{Lr} \) not reverse during the dead time.

\[
L_p \leq \frac{nV_o I_d}{8f_r C_{ds} V_{Ch}}
\tag{10}
\]

\[
\sin^{-1} \left( \frac{nV_o}{4L_{qpf} I_{Lrm}} \right) \geq 2\pi f_r \left( t_d - \frac{8L_{qpf} C_{ds} V_{Ch}}{nV_o} \right)
\tag{11}
\]

C. OPERATING CHARACTERISTICS OF FULL-BRIDGE LLC RESONANT CONVERTS

Since \( f_s \) is very close to \( f_r \), the operating characteristics of the LLC converter are analyzed using the fundamental-wave approximation [11], [12], and the normalized voltage gain \( M \) of the converter and the input impedance \( Z_{in,AB} \) of the resonant network are obtained as

\[
M = \frac{nV_o}{V_{Ch}} = \frac{1}{\sqrt{\left(1 + \frac{1}{\lambda^2} - \frac{1}{4\lambda^2} \right)^2 + Q^2 \left( \frac{f_n}{f_s} - \frac{1}{\lambda^2} \right)}}
\tag{12}
\]

\[
Z_{in,AB} = \frac{\lambda^2 f_n^2 Q^2 R_{ac}}{1 + \lambda^2 f_n^2 Q^2} + j \left( \frac{f_n^2}{f_n} - 1 + \lambda^2 f_n^2 Q^2 \right) \frac{Q R_{ac}}{Q^2}
\tag{13}
\]

where, \( \lambda = L_p/L_r; f_n = f_s/L_r; Q = 2\pi f_r L_r/R_{ac}; R_{ac} = 8 n^2 R_{Lr}/\pi^2 \). To achieve ZVS, \( Z_{in,AB} \) needs to remain inductive over the full load range so its imaginary part needs to be larger than zero, so the quality factor \( Q \) should satisfy (14).

\[
Q \leq \frac{1}{\sqrt{\left( \frac{1}{\lambda^2} - \frac{f_n^2}{f_s} \right)}} = \frac{1}{(\beta f_n)^2}
\tag{14}
\]

From (12), it can be seen that the voltage gain of the converter is influenced by the resonance parameter, the switching frequency, and the load at the same time. Fig. 6(a) shows the curve of \( M \) versus \( f_n \) for different \( Q \). When the value of \( Q \) is large and does not satisfy (14), it can be seen that \( M \) decreases as \( Q \) increases, and the voltage gain curve will be below the voltage gain curve of the resistive resonant network. At this time, the resonant network is capacitive, ZVS can not be achieved, and the smaller the \( Q \) value, the closer the voltage gain curve to the curve at no load, that is, the less \( M \) is affected by the load. It can also be seen that when \( f_n = 1, M \) is not affected by the load and is constant at 1.

The curves of \( M \) versus \( f_n \) when the resonant network is resistive for different \( \lambda \) are given in Fig. 6(b). As \( \lambda \) increases, the voltage gain curve keeps shifting downward, which, combined with the analysis of Fig. 6(a), shows that the range of loads that can make the resonant network inductive is
expanded. It can also be seen that as $\lambda$ increases, the slope of the voltage gain curve at $f_i$ slightly less than 1 is closer to zero, which means that $M$ can be stabilized at the target value even if there is some error in the resonance parameters.

In summary, in the operating mode where $f_i$ is slightly less than $f_r$, the quality factor $Q$ of the resonant network needs to satisfy equation (14) to ensure that the resonant network is inductive in the full load range. In addition, to reduce the impact of load and resonant parameter changes on the stability of voltage gain, $Q$ should be reduced and $\lambda$ increased as much as possible during the parameter design.

III. OPTIMIZED DESIGN OF MAIN CIRCUIT PARAMETERS

In this section, firstly, the resonant parameters are optimized for the full-bridge LLC resonant converter in the full load range for voltage gain stability and soft-switching performance. After that, the design of the intermediate bus voltage is completed by considering the loss and voltage stress of power devices.

A. OPTIMIZED DESIGN OF FULL-BRIDGE LLC RESONANT CONVERTER PARAMETERS

From the analysis results in Section II.C, it can be seen that when $f_i$ is slightly less than $f_r$, $M$ is very close to 1. In the cascaded system of this paper, the LLC resonant converter is used as a DC transformer, so the resonant parameters need to be reasonably designed so that it can maintain a constant voltage gain under different load conditions. Combining with (12), the turns ratio $n$ can be written as

$$n = \frac{V_{Cb}}{V_o} \quad (15)$$

The conditions for achieving ZVS when the resonant network is inductive are given in (10) and (11), and the range of values of $L_p$ can be obtained by combining them. The (16) gives the expression of $I_{Lm}$. Substituting (10), (15) and (16) into (11), we can obtain the function $F(L_p)$ in (17), and ZVS can be realized when the resonant network is inductive only when $F(L_p) \geq 0$.

$$I_{Lm} = \frac{V_o}{4nR_{ld}} \sqrt{\frac{n^4R_{ld}^2}{L_{p1}^2} + 4\pi^2}$$

$$0 < L_p \leq \frac{t_d}{8f_r C_{ds}}$$

$$(17)$$

Fig. 7 gives the relationship curve between $F(L_p)$ and $L_p$. According to the condition that $F(L_p) \geq 0$, the range of $L_p$ values given by (10) can be divided into three intervals. In region 1 and region 3, both have $F(L_p) \geq 0$, and the LLC resonant converter has the conditions to realize ZVS. However, from (6) and (16), it can be seen that the larger the $L_p$, the smaller the $i_{tp}$ and $i_{tr}$, and the smaller the conduction loss and turn-off loss of the primary-side SiC MOSFET for the same load. Meanwhile, according to the analysis results in Section II.C, the larger the value of $\lambda$, the more stable the voltage gain of the LLC resonant converter, while the increase of $L_p$ and the decrease of $L_r$ can increase $\lambda$. In summary, the value of $L_p$ should be

$$L_p = \frac{t_d}{8f_r C_{ds}} \quad (18)$$

From (14), the value of $\lambda$ determines whether the resonant network can maintain inductance under the constant $f_i$. Before designing $L_r$, it is necessary to design $\lambda$. From (14), the range of values of $\lambda$ that enables the resonant network to maintain inductance is

$$\lambda \geq \frac{(1 - f_n^2)\pi^2 f_r^2 L_p^2}{16n^4 R_{ld}^2} + \frac{1 - f_n^2}{f_n^2} \quad (19)$$

FIGURE 6. Normalized voltage gain curves of LLC Converter.

FIGURE 7. The relation curve between $F(L_p)$ and $L_p$. 
Besides, the value of $\lambda$ also determines the stability of the voltage gain of the LLC resonant converter. In the full load range, let the maximum deviation of the normalized voltage gain $M$ be $\delta$, which can be obtained from (12).

$$1 - \delta \leq \frac{1}{\sqrt{\left(1 + \frac{1}{f_n^2} - \frac{1}{f_n^2}\right)^2 + Q^2 \left(f_n - \frac{1}{f_n}\right)^2}} \leq 1 + \delta$$

(20)

As can be seen from (5), in the operating frequency range of $f_p < f_r \leq f_r$, $M$ is always greater than 1 when the resonant network is inductive and reaches its maximum value at $Q = 0$. Considering that the $\lambda$ parameter is usually much larger than 1 and that $f_n$ is close to 1 in this paper, the range of $\lambda$ values that make the maximum deviation of $M$ not exceed $\delta$ can be obtained as

$$\lambda \geq \frac{1 - f_n^2}{f_n^2} + \frac{1 - f_n^2}{\delta f_n^2}$$

(21)

Combining (19) and (21), the value of $\lambda$ that stabilizes the voltage gain and keeps the resonant network inductive is

$$\lambda_{\text{max}} \geq \max \left\{ \frac{(1 - f_n^2) \pi^2 f_r^2 L_d^2}{16n^4 R_{ld}^2}, \frac{1 - f_n^2}{f_n^2}, \frac{1 - f_n^2}{\delta f_n^2} \right\}$$

(22)

From which, due to the large load power, $L_r$ can be taken as

$$L_r = \frac{L_p}{\lambda_{\text{min}}} = \frac{L_p}{(1 - f_n^2) \pi^2 f_r^2 L_d^2 / 16n^4 R_{ld}^2 + (1 - f_n^2) / f_n^2}$$

(23)

After the design of $L_r$ is completed, the resonant capacitor $C_r$ is designed as

$$C_r = \frac{1}{4\pi^2 f_r^2 L_r}$$

(24)

Considering the withstand voltage of the resonant capacitor, it can be seen from Fig. 5 that $C_r$ is charged during the first half resonant cycle and its voltage $v_{Cr}$ rises from a negative peak to a positive peak with a charging current of $I_{Lr}$. From this, the peak-to-peak value $V_{Cr,p-p}$ of $v_{Cr}$ can be got

$$V_{Cr,p-p} = \frac{V_o}{2nf_r C_r R_{ld}}$$

(25)

### B. INTERMEDIATE BUS VOLTAGE DESIGN

Since the input and output voltages, operating frequency, and power rating of the intermediate frequency isolated DC-DC converter are determined, the power device losses of the converter depend mainly on the intermediate bus voltage [13], [14]. To select the optimal intermediate bus voltage, the relationship between the total power device loss and the intermediate bus voltage $V_{Cb}$ needs to be derived.

It should be noted that this paper uses a half-bridge SiC power module manufactured by Wolfspeed, model CAS300M17BM2, which has a significant feature of minimal body diode reverse recovery loss. In addition, the LLC resonant converter realizes the ZCS of the secondary rectifier diode, so the reverse recovery loss of the diode is not considered during the analysis in this section.

The power device losses of the interleaved Boost converter are mainly composed of the switching losses $P_{sw}$ of $Q_{12}, Q_{22}$, the pass-state losses $P_{con}$ and the body diode pass-state losses $P_{Dcon}$ of $Q_{11}$ and $Q_{21}$, respectively, as

$$P_{sw,Q_{12}} = \frac{I_{Lb} f_d B \left(E_{on} + E_{off}\right)}{V_{in} f_n} V_{Cb}$$

(26)

$$P_{con,Q_{12}} = \frac{I_{Lb} R_{ds,on}}{2 V_{Cb}} \left(1 - \frac{V_{in}}{V_{in}}\right)$$

(27)

$$P_{Dcon,Q_{11}} = \frac{V_{FQ} P_o}{2 V_{Cb}}$$

(28)

where $I_{Lb}$ is the rms value of inductor current and $P_o$ is the output power; $E_{on}, E_{off}$, $V_n$ and $I_n$ are the turn-on loss, turn-off loss, drain-source voltage and drain current of the SiC MOSFET under standard test conditions, respectively, all given by the datasheet; $R_{ds,on}$ is the on-state resistance of the SiC MOSFET; $V_{FQ}$ is the forward conduction voltage drop of the body diode. In summary, the total power device losses of the interleaved Boost converter can be obtained as follows.

$$P_{\text{Boost}} = \frac{2I_{Lb} f_d B \left(E_{on} + E_{off}\right)}{V_{in} f_n} V_{Cb}$$

$$+ \frac{I_{Lb}^2 R_{ds,on}}{2 V_{Cb}} \left(2 - \frac{V_{in}}{V_{in}}\right) + \frac{V_{FQ} P_o}{V_{Cb}}$$

(29)

The power device losses of the LLC resonant converter are mainly composed of the pass-state losses of the SiC MOSFETs and the rectifier diodes. The total pass-state losses of SiC MOSFETs in the two LLC resonant converters are

$$P_{con,LLC} = \frac{R_{ds,on}}{8 R_{ld}^2} \left(\frac{V_{Cb}^2}{L_p^2 f_r^2} + \frac{4\pi^2 V_{Cb}^4}{V_{Cb}^2}\right)$$

(30)

In the two LLC resonant converters, the total on-state loss of the sub-side rectifier diode is

$$P_{\text{Dcon,LLC}} = \frac{2P_o V_{FD}}{V_o}$$

(31)

where $V_{FD}$ is the forward conduction voltage drop of the rectifier diode. It can be seen that the loss of the secondary rectifier circuit is independent of the intermediate bus and depends only on the output power and output voltage. In summary, the total power device losses of the two LLC resonant converters can be obtained as

$$P_{\text{LLC}} = \frac{R_{ds,on} V_{Cb}^2}{8 L_p^2 f_r^2} + \frac{\pi^2 R_{ds,on} V_o^4}{2 R_{ld}^2 V_{Cb}^2} + \frac{2P_o V_{FD}}{V_o}$$

(32)

Combining (29) and (32), the total power device loss of the whole converter can be obtained as

$$P_{\text{loss,total}} = P_{\text{Boost}} + P_{\text{LLC}}$$

(33)

Since the input voltage range of the auxiliary power supply system is large, Fig. 8 gives the total power device loss curves for different input voltages. From Fig. 8, it can be seen that the total power device loss decreases as the input voltage
increases. From the perspective of improving the system efficiency, the value of $V_{Cb}$ should be taken to ensure that the total power device loss is close to or reaches the minimum value under different input voltages, and to meet this condition, the size of $V_{Cb}$ should be around 1100V.

It is also important to note that the interleaved Boost converter is hard-switched. Due to the presence of power loop stray inductance, there is a large voltage spike at the drain-source of the SiC MOSFET. In the case of transient overcurrent, the device is subjected to high voltage stress. To avoid over-voltage damage to the SiC MOSFET, the intermediate bus voltage should also be selected in conjunction with the experimental measurement results of the turn-off voltage spikes. For the SiC MOSFET with a rated voltage of 1700V, considering the voltage safety margin and the power loss curve given in Figure 8, the final intermediate bus voltage is determined to be 1050V.

IV. SIMULATION AND EXPERIMENTAL VALIDATION
The main performance specifications of the full SiC intermediate frequency isolated DC-DC converter are given in Table 1. According to the proposed method in Section III, the circuit design parameters of the converter are shown in Table 2. Simulations and experiments are performed to verify the correctness of the proposed parameter design method.

| TABLE 1. Main performance index of the SiC intermediate frequency isolated DC-DC converter. |
|---------------------------------------------|
| Parameters                      | Symbols | Value |
|---------------------------------------------|
| Input Voltage                     | $V_{in}$ | 1000-1800V |
| Intermediate bus voltage          | $V_{Cb}$ | 1050V |
| Output Voltage                    | $V_{o}$ | 700V |
| Output Power                      | $P_{o}$ | 150kW |
| Boost switching frequency         | $f_{sb}$ | 20kHz |
| LLC switching frequency           | $f_{sc}$ | 30kHz |
| LLC resonant frequency            | $f_{r}$ | 32kHz |

A. SIMULATION VERIFICATION
The converter model was built in MATLAB/Simulink software for simulation verification. The simulated waveforms of $i_{Lb}$ and $v_{Cb}$ of the interleaved Boost converter at rated operating conditions are given in Fig. 9. It can be seen that $v_{Cb}$ is stable at 1050 V, while the pulsation frequency of the inductor current is twice the switching frequency.

The main simulated waveforms of the LLC resonant converter for different load cases are given in Fig. 10. It can be seen that the ZVS of the SiC MOSFET and the ZCS of the rectifier diode is achieved simultaneously in the full load range. $i_{Lp}$ is already small when the SiC MOSFET is turned off, so the SiC MOSFET also approximates the ZCS. It can also be seen that the output voltage is stable at about 700 V when the load is varied, which indicates that the LLC resonant converter has good voltage gain stability.

Fig. 11(a) gives the simulated waveform of the LLC resonant converter at $L_p=135\mu H$, when $L_p$ is in region 1 in Fig. 7 and $F(L_p) \geq 0$. Despite the realization of ZVS, the smaller $L_p$ leads to a high excitation current and a low efficiency of the converter. Fig. 11(b) gives the simulation waveform when $L_p=800\mu H$, at this time $L_p$ is in region 2 in Fig. 7, $F(L_p)<0$. At this time, the resonant current in the dead zone is reversed, and the ZVS is not realized effectively.

The above simulation results verify the correctness of the proposed parameter optimization design method.

B. EXPERIMENTAL VERIFICATION
To verify the correctness of the theoretical analysis and simulation results, an experimental platform with an input voltage...
of 1500V and an output power of 15kW was built, as shown in Fig. 12(a) and (b).

Fig. 13 gives the experimental waveforms of the full-bridge LLC resonant converter at different loads. The output voltage is stable at 700 V under different load conditions, which proves that the DC voltage gain of the converter has good stability. It is worth noting that the turn-off current of the primary SiC MOSFET is equal to the peak excitation current, which is much smaller than the load current, so there is almost no turn-off voltage spike at the terminals of the primary SiC MOSFET.

Fig. 14(a) and Fig. 14(b) give the experimental waveforms of the converter at the load jump and the experimental waveforms at the input voltage change, respectively. Where $i_{T11}$ and $i_{T22}$ are the transformer secondary output currents of the two sub-modules, and $i_{SIV}$ is the single-phase output current of the three-phase inverter. It can be seen that the intermediate bus voltage and output current of the two sub-modules are well synchronized without additional voltage and current equalization control strategies, and the full-bridge LLC resonant converter plays the role of a DC transformer. The above experimental results verify the correctness of the parameter optimization design method proposed in Section III of this paper.

Fig. 15 gives the variation curve of efficiency with the output power of the full SiC intermediate frequency isolated DC-DC converter at an input voltage of 1500V. It can be seen that the efficiency of the converter is low at light load. The main reason is that the LLC resonant converter has inherent
Fig. 16 gives a comparison of the component mass of Si intermediate frequency isolated DC-DC converter and SiC intermediate frequency isolated DC-DC converter with similar power index. The power density is improved by 80.62% compared to the Si intermediate frequency isolated DC-DC converter.

V. CONCLUSION
In this paper, a full SiC intermediate frequency isolated DC-DC converter with ISOP structure consisting of Boost converter + full-bridge LLC resonant converter cascade module is studied. The optimized design method of converter parameters is proposed, which can make the LLC resonant converter in it have stable DC voltage gain and soft switching performance, and play the role of a DC transformer. Meanwhile, based on the power device loss model of the converter, the design method of the intermediate DC bus voltage is proposed. After that, the correctness of the above parameter design method is verified by simulation and experiment, and the converter performance is analyzed. The efficiency of the converter reaches 96.21% at an input voltage of 1500V and an output power of 15kW.

REFERENCES
[1] O. Deblecker, A. Moretti, and F. Vallee, “Comparative study of soft-switched isolated DC–DC converters for auxiliary railway supply,” IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2218–2229, Sep. 2008, doi: 10.1109/TPEL.2008.2001879.
[2] M.-A. Ockenburg, M. Dohmen, X.-Q. Wu, and M. Helsper, “Next-generation DC–DC converters for auxiliary power supplies with SiC MOSFETs,” in Proc. IEEE Int. Conf. Electr. Syst. Aircr., Railway, Ship Propuls. Road Vehicles Int. Transp. Electrific. Conf. (ESARS-ITEC), Nov. 2018, pp. 1–6, doi: 10.1109/ESARS-ITEC.2018.8607463.
[3] D. Wu, C. Xiao, H. Zhang, and W. Liang, “Development of auxiliary converter based on 1700 V/325A full SiC MOSFET for urban rail transit vehicles,” in Proc. IEEE Transp. Electrific. Conf. Expo., Asia–Pacific (ITEC Asia-Pacific), Aug. 2017, pp. 1–6, doi: 10.1109/ITEC-AP.2017.8080769.
[4] M. Helsper and M. Ockenburg, “SiC MOSFET based auxiliary power supply for rail vehicles,” in Proc. 20th Eur. Conf. Power Electron. Appl. (EPE ECCE Europe), 2018, pp. 1–8.
[5] T. Liang, Q. Liu, and V. R. Dinavahi, “Real-time hardware-in-the-loop emulation of high-speed rail power system with SiC-based energy conversion,” IEEE Access, vol. 8, pp. 122348–122359, 2020, doi: 10.1109/ACCESS.2020.3006904.
[6] Q. Wu, M. Wang, W. Zhou, X. Wang, G. Liu, and C. You, “Analytical switching model of a 1200 V SiC MOSFET in a high-frequency series resonant pulsed power converter for plasma generation,” IEEE Access, vol. 7, pp. 99622–99632, 2019, doi: 10.1109/ACCESS.2019.2930535.
[7] B. Zhao, Q. Song, and W. Liu, “Experimental comparison of isolated bidirectional DC–DC converters based on all-Si and all-SiC power devices for next-generation power conversion application,” IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1389–1393, Mar. 2014, doi: 10.1109/TIE.2013.2258304.
[8] F. Li, Z. Yang, F. Lin, and Z. Wang, “Analysis of soft-switching behavior of SiC MOSFET in phase-shifted full-bridge circuits with different dead-time for APU,” in Proc. IEEE Vehicle Power Propuls. Conf. (VPPC), Oct. 2019, pp. 1–6, doi: 10.1109/VPPC46532.2019.8952400.
[9] G. Ivensky, S. Bronshtein, and A. Abramovitz, “Approximate analysis of resonant LLC DC–DC converter,” IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3274–3284, Nov. 2011, doi: 10.1109/TPEL.2011.2142009.
[10] C. Luo and S. Huang, “Novel voltage balancing control strategy for dual-active-bridge input-series-output-parallel DC–DC converters,” IEEE Access, vol. 8, pp. 103114–103123, 2020, doi: 10.1109/ACCESS.2020.2999034.
C. Kang et al.: Parameters Optimization of an Intermediate Frequency Isolated SiC Power DC-DC Converter

[11] M. Li, O. Ziwei, and M. A. E. Andersen, “High-frequency LLC resonant converter with magnetic shunt integrated planar transformer,” IEEE Trans. Power Electron., vol. 34, no. 3, pp. 2405–2415, Mar. 2019, doi: 10.1109/TPEL.2018.2842029.

[12] S.-T. Wu and C.-H. Han, “Design and implementation of a full-bridge LLC converter with wireless power transfer for dual mode output load,” IEEE Access, vol. 9, pp. 120392–120406, 2021, doi: 10.1109/ACCESS.2021.3107868.

[13] J. Lee, Y. Jeong, and B. Han, “An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications,” IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2926–2934, Jul. 2011, doi: 10.1109/TIE.2010.2076311.

[14] F. Wang, X. Wang, and X. Ruan, “An optimal design scheme of intermediate bus voltage for two-stage LLC resonant converter based on SiC MOSFET,” in Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia (WiPDA Asia), Aug. 2021, pp. 488–492, doi: 10.1109/WiPDAAsia51810.2021.9655998.

CHENGWEI KANG received the B.E. and M.E. degrees in locomotive and vehicle from Dalian Jiaotong University, Dalian, China, in 2004 and 2007, respectively.

He developed TCMS software and part of traction control software of CR400BF EMU. He is currently a Senior Research, a Development Engineer and a Specialist with CRRC. His research interests include traction system control and TCMS of EMU and subway.

HONGLIANG PAN received the B.S. degree in mechanical design and manufacturing from the Shanghai University of Technology, in 1993, the M.S. degree in mechanical manufacturing from Shanghai University, in 1996, and the Ph.D. degree in transportation information engineering and control from Tongji University, Shanghai, China, in 2013.

He is currently an Associate Researcher with the National Maglev Transportation Engineering Technology Research and Development Center, Tongji University. He is a Shanghai registered Consulting Expert, a national registered Consulting (Investment) Engineer, a national registered Safety Engineer, the Director of the Shanghai Engineering Management Society, and a registered Expert of the National Railway Bureau. His research interests include maglev transportation control systems, system safety research, and RAMS research of rail transit systems.

SHUIYUAN HE received the B.Eng. degree in electrical engineering and automation from the China University of Mining and Technology, in 2021. He is currently pursuing the master’s degree with Beijing Jiaotong University.

His research interest includes wide range resonant converter.

JIAHUI REN received the B.Eng. and B.S. degrees in electrical engineering and automation from Beijing Jiaotong University, Beijing, China, in 2019 and 2022, respectively.

His research interests include high-frequency and high-efficiency power electronics converters, series-parallel systems, and the control strategies of converter.

DAZHI HOU received the B.Eng. degree from the School of Electrical Engineering, Southwest Jiaotong University, in 2000.

Currently, he is a Senior Engineer with CRRC Changchun Railway Vehicle Company Ltd. His research interests include overall design of rail transit vehicles and with new energy integration technology.

PEICHENG CONG was born in Heilongjiang, China, in 1984. He received the B.S. degree from Yanshan University, in 2007, and the M.S. degree from Harbin Institute of Technology, in 2010, all in electrical engineering and automation.

He has been engaged in the research of motor control and its application in rail transit, since 2010. He is with Shanghai CRRC Rail Transportation Equipment Company Ltd., Shanghai, China.

JINGYAN ZHANG received the M.Eng. degree from Beijing Jiaotong University, in 2014.

Currently, she is a Senior Engineer with CRRC Changchun Railway Vehicle Company Ltd. Her research interests include traction drive control of rail transit and new energy storage technology.

LIJUN DIAO (Senior Member, IEEE) received the B.Eng. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2003 and 2008, respectively.

From 2008 to 2010, he was a Postdoctoral Researcher at the School of Electrical Engineering, Beijing Jiaotong University, where he is a Professor. He was a Project Investigator of the traction systems’ Research and Development for China’s first 100% low floor light rail vehicle, first hybrid EMU, metro, full-SiC converter, WPT, and other important projects. He is currently the Vice-Dean of the Beijing Engineering Research Center for Electrical Rail Transit and the Deputy Secretary-General of Committee of Electrical and Electronic Technologies for Rail Transportation, China-Electrotechnical Society. He was an Academic Visitor at the Faculty of Engineering and Physical Sciences (FEE), the University of Southampton, Southampton, U.K., from 2016 to 2017, and a Senior Academic Visitor at Technische Universität München (TUM), from January 2020 to February 2020. His research interests include power electronics and ac drives for transportation electrification, such as rail transit, ship and safety and energy management of multienergy drive systems.

VOLUME 10, 2022

94817