A new PWM approach for digital boost power factor correction controller

Li Lai, Ping Luo, and Qing Hua

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

Abstract: The OCC control approach for single-phase boost PFC rectifier without the requirement of input voltage sensing or complicated two loops compensation design could result in high power factor, low harmonic input current ingredients operation over universal loads in continuous conduction mode. The trialing triangle modulation adopted in this paper makes the acquisition of the average input current an easy process. The implementation of the controller is based on boost topology power circuit with low speed, low resolution A/D converters and economic FPGA development board. Experimental results demonstrate that the proposed PFC rectifier could get PF value up to 0.999 and the minimum THD down to 1.9% by a 120 W prototype.

Keywords: continuous current mode (CCM), one cycle control (OCC), power factor correction (PFC), trialing triangle modulation

Classification: Electronic instrumentation and control

References

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1 Introduction

According to international energy standards such as IEC1000-3-2 [1], it is necessary to use a single-phase power factor correction (PFC) boost rectifier to improve the power factor and energy quality of the electric system. A lot of research results on boost PFC control approach are presented. The one cycle control (OCC) of boost PFC converter is proposed in [2], which introduces the nonlinear control approach with merits as simple structure and low cost. The benefit of OCC lies in eliminating the need to sense the input voltage and using the simple integrator to
replace the complicated multiplier in average current mode control approach. However, the conventional OCC limits its application mostly in analog field. On the other hand in recent year, digital implementation boost PFC converters are attracting more and more attention. The most troublesome obstacle for implementing digital one cycle control (DOCC) approach is to imitating the integration part. In [3], an accumulator is used to calculate the sum of input current samples to get the average input current value. This method requires very fast A/D converters and adds heavy calculation burden to controller in every switching cycle. This paper proposes a FPGA-based DOCC boost PFC operating under continuous conduction mode (CCM) condition. This boost PFC rectifier adopts trialing triangle modulation method to capture the average input current of every switching cycle. The compensation part of controller is designed on a new voltage loop small signal model without explicit current loop compensation part, yet results in high power factor and low THD level over large load range.

2 Proposed trialing triangle modulation in PFC controller

The basic objective of PFC rectifier is make sure the input current is synchronized with grid voltage (with same frequency and phase), which can be written as \( i_L = v_{in} G_{in} \), where \( i_L \) is the average inductor current in one switching cycles, \( v_{in} \) is the rectified grid voltage and \( G_{in} \) is the emulated input admittance. By the quasi-state approximation in CCM boost PFC operation, assuming \( v_{in} \) and \( v_o \) is a constant value during one switching cycle \( T_s \), we get \( v_o (1 - d) = v_{in} \), where \( d \) is the switching duty ratio, \( v_o \) is the output voltage. The objective of PFC controller can be express as

\[
i_L = G_{in} v_{in} = G_{in} v_o (1 - d)
\]

Equation (1) indicates the duty ratio should be applied the switching converter in every duty cycle. Since \( v_{in} \) is expressed by the terms of \( v_o \) and \( d \), it is not necessary to sense the input voltage. The \( v_o \) is sampled by a low-cost A/D converter. \( G_{in} \) is computed by the compensation part of voltage loop, which will be detailed the derivation later. The mostly tricky problem is the acquisition of the average current of the duty cycle. There are four basic current sample methods (trailing edge mode,
leading edge mode, trailing triangle mode and leading triangle mode) used in switching power system, as shown in Fig. 1.

While trailing edge modulation or leading edge modulation is not suitable in average current acquisition, the triangle modulation is adopted in DOCC current sampling operation method. Since the rectifier might enter discontinuous current mode (DCM) mode, the current at $T_s/2$ instant could be hard to track and sample, we utilize the trailing triangle modulation in this paper and prototype design.

As shown in Fig. 2, the power switch will always be turned on at the beginning of every switching cycle, while be turned off at the $dT_s/2$ instant. The switch will not be open until $(1 - d/2)T_s$ instant. It can be concluded that the sample current $i_L[n - 1]$ at a instant will be the average current of $(n - 1)th$ switching cycle. According to the quasi-state approximation, the switching frequency is much faster than input current frequency, we could take the sample average current $i_L[n - 1]$ at a instant as the average current criterion $i_L[n]$ in nth switching cycle by assuming two consecutive switching cycles with the same average current. This approximation will bring great convenience in control analysis and system implementation.

![Fig. 2. Input current sample operation with trailing triangle modulation](image)

There are two main merits in adopting the trailing triangle modulation for average current $i_L[n]$ acquisition. 1. The average current of the switching cycle is obtained through a relative simple method without the need for accumulator in [3]. This could save the hardware consuming in FPGA implementation. The current sampled at fixed instant on switching frequency makes the utilization of low cost, low speed A/D converters possible. It also makes the design of sampling circuit easy. 2. The average current criterion is acquired at the begging of the switching cycle. This approach leaves enough time for calculating the appropriate duty ratio for the switching cycle online.

### 3 Implementation issues

The block diagram of the proposed duty cycle control for PFC is showed in Fig. 3. The proposed control algorithm is implemented in Cyclone III FPGA. The controller implementation based on FPGA could achieve multi-models system integration with few peripheral devices and routings. The parallel computing character of FPGA will also guarantee the real-time requirement of some complex algorithm. We only utilize the upper 8 bits digital output of chosen A/D converters LTC1412.
Since the MSB of the digital output indicates the sign of output value, the output range of LTC1412 is $-2.5\,\text{V} \sim 2.5\,\text{V}$, the gain of AD converters is $K_{\text{ad}} = 27/2.5 \approx 51$. Table I lists the parameters of proposed boost PFC prototype.

| simulation parameters | values |
|-----------------------|--------|
| line inductor $L$     | 500 $\mu\text{H}$ |
| output capacitor $C$  | 1000 $\mu\text{F}$ |
| switching frequency $f_s$ | 48.8 KHz |
| input RMS voltage $V_{\text{rms}}$ | 50 V |
| output voltage $V_o$  | 80 V |
| output power $P_o$    | 120 W |

Table I. Values of parameters

4 Experimental results

In Fig. 4, the picture is taken for the experiment set-up of the proposed boost PFC rectifier. For safety consideration, an isolating transformer (with transformer ratio 1:1) is used. The $V_{\text{rms}} = 50\,\text{V}$ is obtained by the voltage regulator. We use the IT8514 DC electronic load for generating the system load and load step. The PF and THD are measured by WT210 digital power meter.
Fig. 5(a) shows the DPWM waveform (upper) and LTC1412 transition signal waveform (under). It can be observed that the falling-edge of transition signal always occurs at the beginning of the switching cycle at fixed frequency $f_s$. To verify the validity of the voltage loop, we exhibit the output voltage $V_o$ waveforms. Fig. 5(b) shows the input voltage waveform (upper) and input current waveform (under) after the PFC, the input current is synchronized with input voltage perfectly. Fig. 5(c) shows the output voltage regulation process from 120 W to 40 W load step. As been observed in the figure, the maximum overshoot output voltage $v_{oo}$ is 92.5 V and it takes system about 1360 ms regulating voltage to steady state (80 V). Fig. 5(d) shows the output voltage regulation process from 40 W to 120 W load step, which is the converse process of load step in Fig. 5(c). It can be observed that it elapses 825 ms before the output voltage recovers to 80 V, the minimum undershoot output voltage $v_{ou}$ is 68.2 V. It takes more regulation time back to stability for the system when load step from 120 W to 40 W than the converse load step process from 40 W to 120 W. It is the typical phenomenon for single-ended Boost topology since it has no energy release path in load drop step process. The measured PF value and THD of proposed boost PFC converter are illustrated in Table II.

Table II. Converter performances with proposed control algorithm

| Output power | PF  | THD  |
|--------------|-----|------|
| 64 W         | 0.998 | 6.4% |
| 80 W         | 0.999 | 3.2% |
| 108 W        | 0.999 | 2.3% |
| 120 W        | 0.999 | 1.9% |
5 Conclusion

This paper proposes an FPGA-based fully digital controller for boost PFC converter. The proposed PFC converter realizes the DOCC control approach which requires no input voltage sensing, two loops compensation part design or complicated average current sampling and calculation process, yet results in high power factor, low harmonic input current ingredients operation over large range load in CCM. Experimental results demonstrate that the proposed PFC rectifier could get PF value up to 0.999 and the minimum THD down to 1.9% by a 120 W prototype operating in 50 V input line voltage. The feasibility and good dynamics response under variable load conditions of proposed prototype are proved to be satisfactory.

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