Going Further With Winograd Convolutions: Tap-Wise Quantization for Efficient Inference on 4x4 Tiles

Renzo Andri*, Beatrice Bussolino*†, Antonio Cipolletta*, Lukas Cavigelli*, Zhe Wang*

*Computing Systems Lab, Huawei Zurich Research Center
†DET, Politecnico di Torino, Italy

Abstract—Most of today’s computer vision pipelines are built around deep neural networks, where convolution operations require most of the generally high compute effort. The Winograd convolution algorithm computes convolutions with fewer multiply–accumulate operations (MACs) compared to the standard algorithm, reducing the operation count by a factor of 2.25x for 3x3 convolutions when using the version with 2x2-sized tiles $F_2$. Even though the gain is significant, the Winograd algorithm with larger tile sizes, i.e., $F_3$, offers even more potential in improving throughput and energy efficiency, as it reduces the required MACs by 4x. Unfortunately, the Winograd algorithm with larger tile sizes introduces numerical issues that prevent its use on integer domain-specific accelerators (DSAs) and higher computational overhead to transform input and output data between spatial and Winograd domains.

To unlock the full potential of Winograd $F_3$, we propose a novel tap-wise quantization method that overcomes the numerical issues of using larger tiles, enabling integer-only inference. Moreover, we present custom hardware units that process the Winograd transformations in a power- and area-efficient way, and we show how to integrate such custom modules in an industrial-grade, programmable DSA. An extensive experimental evaluation on a large set of state-of-the-art computer vision benchmarks reveals that the tap-wise quantization algorithm makes the quantized Winograd $F_3$ network almost as accurate as the FP32 baseline. The Winograd-enhanced DSA achieves up to 1.85x gain in energy efficiency and up to 1.83x end-to-end speed-up for state-of-the-art segmentation and detection networks.

Keywords—Machine Learning Acceleration, Winograd Convolution, ML System Design

I. INTRODUCTION

Convolutional neural networks (CNNs) have had a significant breakthrough in almost all Artificial Intelligence (AI) tasks in recent years, thanks to large, comprehensible, and publicly available data sets, easy-to-use frameworks, and the newly available vast compute resources. Nevertheless, state-of-the-art neural networks come with high computational costs (> GFLOPs/inference) and memory requirements (>10 MB), which has led to an explosion of DSAs in datacenters [21], [36] and edge devices [22].

Typically, floating-point numbers have been used to flexibly represent CNN computations, but floating-point datapath is very area- and power-hungry due to the large intermediate values, re-normalization, and exception handling, which require adequate hardware support. Thanks to the intrinsic error tolerance of neural networks [12], [70], 8-bit integer operations can be used for most inference applications with no to minimal accuracy degradation. As integer operations—like additions and multiplications—are one order of magnitude more energy-efficient than their floating-point counterparts [17], integer-based accelerators can achieve much higher peak throughput and energy efficiency.

In order to reduce operation count and memory footprint even further, recent works have proposed to adopt smaller convolutional kernel sizes [27], exploit sparsity [14], use group convolutions [27], [63], channel shuffling [68], and depthwise separable convolutions [18]. Nevertheless, compute-heavy, dense 3×3 convolutional layers are still widely used in many state-of-the-art computer vision models [39], [53], [54]. Thus, the adoption of the Winograd algorithm [62] represents an interesting optimization opportunity as it converts the 3×3 convolution operation into a much less expensive elementwise multiplication.

The Winograd convolution algorithm extends the Toom-Cook algorithm to support convolutions by applying the (polynomial) Chinese remainder theorem, minimizing the number of required multiplications [6], [62]. Specifically, the 2D convolution with a feature map $x$ of size $m \times m$ and convolutions kernel $f$ of size $3 \times 3$ is calculated with the Winograd (convolution) algorithm $F_m = F(m \times m, 3 \times 3)$ as follows:

$$Y = A^T \left[ (GfG^T) \odot (B^TxB) \right] A$$

(1)

where $G \in \mathbb{R}^{(m+2) \times 3}$, $B^T \in \mathbb{R}^{(m+2) \times (m+2)}$, and $A^T \in \mathbb{R}^{m \times (m+2)}$ are called transformation matrices. Specifically, the $G$ and $B^T$ matrices transform the weights and the input feature maps, respectively, from the spatial domain to the Winograd domain. Here, the convolution becomes an $(m+2)^2$-sized element-wise multiplication of the feature maps with the filter weights such that the number of multiplications is reduced from $m^2 \cdot 9$ to $(m+2)^2$. Then, the $A^T$ matrix transforms the output feature maps back to the spatial domain.

While larger feature map tile sizes $(m \uparrow)$ reduce the number of required multiply-and-accumulate operations

---

*This work was done while Beatrice Bussolino was an intern at Huawei Technologies - Zurich Research Center.
(MACs ↓) compared to the standard convolution algorithm, this comes at the cost of more complex transformation matrices, higher sensitivity to numerical inaccuracies, and so, in practice, diminishing returns [3]. Thus, the focus of actual implementations has been mainly put towards \( m \in \{2, 4\} \), resulting in a potential reduction of the number of MACs by 2.25× for \( F_2 \) and by 4× for \( F_4 \). Unfortunately, the numerical instability of \( F_4 \) prevents a straightforward adoption of \( \text{int}_8 \) operations [4], [11], [29]. Moreover, the challenges of processing more complex transformation matrices in a programmable AI accelerator have not been addressed in previous works [41], [44], [66].

This work aims primarily at enabling \( \text{int}_8 \) Winograd \( F_4 \) inference on a domain-specific accelerator. Particularly, we propose a novel tap-wise quantization algorithm to overcome the numerical issue of Winograd \( F_4 \) and an architectural and micro-architectural design space exploration for efficient hardware implementation. An extensive evaluation demonstrates that the tap-wise quantization algorithm guarantees negligible accuracy drop on several state-of-the-art CNNs.

In the following section, we introduce the Winograd \( F_4 \) algorithm in more detail, highlighting its challenges and our proposed solutions.

II. BEYOND WINOGRAD 2×2

The transformation matrices for Winograd \( F_2 \) can be derived from the polynomial roots \( \{0, 1, -1\} \) s.t.:

\[
B^T = \begin{bmatrix}
1 & 0 & -1 \\
0 & 1 & 0 \\
0 & -1 & 1
\end{bmatrix}, \quad
G = \begin{bmatrix}
2 & 0 & 0 \\
1 & 1 & 1 \\
1 & -1 & 1
\end{bmatrix}, \quad
\]

\[
A^T = \begin{bmatrix}
1 & 1 & 0 \\
0 & 1 & -1
\end{bmatrix}
\]

The matrices are relatively sparse and contain only ±1 in \( B^T \) and \( A^T \), requiring just additions and subtractions. The weight transformation matrix has mostly ±1 values, which can be implemented as a shift-by-1-and-add: \( c = \frac{1}{2} a + \frac{1}{2} b = (a + b)\gg 1 \).

To guarantee bit-true computation in the Winograd domain, \( B^T x B \) requires only 2 extra bits \( (k = 2^2) \), and \( G f G^T \) requires 3 extra bits \( (k = 3^2) \) as the sum of \( k \) \( \text{int}_8 \) values results in a \( \lceil \log_2((2^m - 1) + 1) \rceil \)-bit integer in the worst case. However, as weights and activation value distributions in CNNs usually follow a Gaussian distribution centered around zero, in practice, 8 bits are sufficient to keep the same accuracy.

The most common Winograd \( F_4 \) algorithm uses the root points \( \{0, 1, -1, \frac{1}{2}, \frac{1}{2}\} \), s.t.:

\[
B^T = \begin{bmatrix}
4 & 0 & -5 & 0 & 1 & 0 \\
0 & -4 & -4 & 1 & 1 & 0 \\
0 & -2 & -1 & 2 & 1 & 0 \\
0 & 2 & -1 & -2 & 1 & 0 \\
0 & 4 & 0 & -5 & 0 & 1
\end{bmatrix}, \quad
G = \begin{bmatrix}
3/4 & 0 & 0 \\
-1/2 & -1/2 & -1/2 \\
1/8 & 1/4 & 1/2 \\
1/8 & -1/4 & 1/2 \\
0 & 0 & 3
\end{bmatrix}, \quad
\]

\[
A^T = \begin{bmatrix}
1 & 1 & 1 & 0 \\
0 & 1 & -1 & 2 & -2 & 0 \\
0 & 1 & 1 & 4 & 4 & 0 \\
0 & 1 & -1 & 8 & -8 & 1
\end{bmatrix}
\]

The transformation matrices of \( F_4 \) are much less sparse, contain a wider range of coefficients, and require more computing effort. Therefore, while \( F_4 \) further reduces the number of MACs, it also introduces three significant challenges.

**Challenge I: Non-uniform dynamic range.** A bit-true \( F_4 \) Winograd algorithm requires 10 extra bits for the weights and 8 extra bits for both the input and output feature maps transformations. Clearly, such an increased bitwidth represents an unfeasible requirement for a high-throughput hardware accelerator as it significantly raises the power and area costs. However, quantizing all the taps to \( \text{int}_8 \) in a traditional fashion, i.e., using the same scaling factor for all the taps, has a disruptive effect on the accuracy of the network [11]. We found out that the Winograd transformation matrices significantly change the dynamic range of each output tap, as shown in Fig. 1 for three taps of the weights in Winograd domain \( G f G^T \) of ResNet-34.

To this end, we propose a tap-wise quantization algorithm to enable \( \text{int}_8 \) inference with the \( F_4 \) Winograd algorithm. Specifically, we present a training method that learns hardware-friendly powers-of-two scaling factors needed to independently quantize each tap based on its post-transformation dynamic range.

**Challenge II: Complex transformation operations.** As the heart of virtually all modern accelerators is a large and high-throughput 2D or 3D data path for matrix-matrix
multiplication (MatMul) [10], [21], [36], translating the lower computational complexity of the Winograd algorithm into wall-clock time speed-up is not straightforward. Among all the steps involved in the Winograd algorithm, only the tap-wise multiplications can be efficiently processed as a batched MatMul. On the other hand, the input, output, and weight transformations involve several small MatMuls and data-layout rearrangement operations, which cannot be processed at high throughput on a 2D or 3D MatMul engine. Thus, increasing the Winograd tile size moves “ops” from cheap, high-arithmetic intensity operations to more sparse, low-arithmetic intensity ones.

To address this challenge, we present a design space exploration of custom hardwired modules that implement the low-arithmetic intensity “ops” of the Winograd transformation operations in an area- and power-efficient way.

**Challenge III: Orchestrating heterogeneous operations.** One of the major challenges of developing a high-performance CNN accelerator is balancing memory bandwidth and compute throughput. By adding a new class of operations, the Winograd algorithm increases the heterogeneity of the compute operations, making the orchestration of data movements and computations much more complex. Moreover, the Winograd algorithm lowers the computational complexity of the Conv2D operation compared to the standard implementation but at the cost of substantially reducing the data reuse opportunities. This characteristic inevitably puts more pressure on the memory bandwidth requirements and calls for a careful dataflow development.

With this in mind, we show how to integrate the Winograd transformation engines in an industrial grade, programmable AI accelerator and how to tune the microarchitecture of such blocks to match the throughput of data movement, Winograd transformation, and compute operations, maximizing the overall compute efficiency. The presented methodology can serve as a guideline for DSA designers willing to exploit the Winograd transformation engines in other accelerators.

**III. TAP-WISE QUANTIZATION**

**Quantization.** Neural networks are commonly trained with floating-point numbers with 16–32 bits. However, this comes with a significant power and area cost. Quantization to integer numbers for inference has become popular as most neural networks can be quantized to int8 with minimal or no accuracy loss [12], [70]. Floating-point numbers are approximated as integer numbers with a shared FP32 scale factor $s$, s.t., $x_{\text{float32}} \approx \hat{x}_{\text{intn}}$, where $s = \frac{s_{\text{max}}}{2^n}$, and $x_{\text{max}}$ is the largest representable value, and the quantized value:

$$\hat{x}_{\text{intn}} = \left\lfloor \frac{x}{s} \right\rfloor_{\text{intn}} = \text{clamp}\left(\left\lfloor \frac{x}{s} \right\rfloor, -2^{n-1}, 2^{n-1} - 1\right) \quad (2)$$

We calibrate $x_{\text{max}}$ by calculating a running average of the maximum values obtained during the training of the full network. After scaling, the data is rounded to the next integer value, and clamped within the $n$-bit integer number range, i.e., [-128,127] for int8, denoted by the function $\lfloor x \rfloor_{\text{intn}}$.

Previously, several works have proposed to quantize directly in the Winograd domain [2], [11], [20], [32], [47]. Even though this helped to improve the performance of Winograd $F_2$ ($m = 2$), it is not sufficient for $F_4$ and larger tile sizes. Specifically, looking at the value distributions, we found out that the weights and feature maps in the Winograd domain heavily depend on their tap index, as shown in Fig. 1. For this reason, we propose to independently quantize each tap.

**Tap-wise Quantization.** Based on the formulas of Winograd (Eq. (1)), and the general quantization (Eq. (2)), tap-wise quantized Winograd (for a single output feature map (oFM) and single tile) can be described as follows:

$$y = \sum_{C_m} A^T \left( s_B \left| B^T \hat{x}_{C_m} B / s_B \right|_{\text{intb}} \odot s_G \left| G \hat{f}_{C_m} G^T / s_G \right|_{\text{intb}} \right) A_B$$

We then replace the linear scaling factors $s_B$ and $s_G$ with tap-wise scaling matrices $S_G, S_B \in \mathbb{R}^{(m+r-1) \times (m+r-1)}$ for the weights and the input feature map (iFM) respectively. We define $S_{BG} = S_G \odot S_B$ for the output feature map (oFM). The multiplications/divisions with scalars are substituted with their element-wise counterparts $\odot, \oslash$.

Finally, we apply the distributivity law and rearrange the linear operations to obtain the following quantization scheme:

$$A^T \left( S_{BG} \odot \sum_{C_m} \left| B^T \hat{x}_{C_m} B / s_B \right|_{\text{intb}} \odot \left| G \hat{f}_{C_m} G^T / s_G \right|_{\text{intb}} \right) A_B$$

The multiplications and accumulations over the input feature maps (iFMs) are calculated in the integer domain, and rescaling is applied just once before the back-transformation, as an element-wise multiplication with $S_{BG}$.

**A. Winograd-aware Training**

We use stochastic gradient descent to train the network. To improve the training outcome, we also adopt the static Winograd-aware training method [11], which propagates the gradients through the Winograd domain. Fernandez et al. [11] also proposed the flex variant, in which they learn the transformation matrices as a network parameter, and thus propagate the gradients back to $G, B$, and $A$. We are not considering this option because it introduces significantly more floating-point operations by making the transformation matrices dense and by preventing the use of HW-friendly shift-and-add operations.

**B. Power-of-two Tap-wise Quantization**

The scaling operations cannot be moved outside of the Winograd domain and therefore introduce one multiplication with an FP32 value per transformation and tap. These multiplications can be shared among the output channels for iFMs transformation and input channels for the oFMs
transformation. Nevertheless, it is favorable to restrict the scaling values to power-of-two values, such that the transformations can be performed with shift-and-add operations only, including the rescaling to adapt to the dynamic range. We evaluate and combine 3 approaches to learn the power-of-two scaling factors.

**Straight-forward power-of-two quantization.** All scaling factors calculated from the calibrated maximum values are rounded to the next power-of-two: \( \tilde{s}_{ij} := 2^\lceil \log_2 s_{ij} \rceil \), such that the quantized value is \( q_{\text{int}b}(x) := \lceil x/2^\lceil \log_2 r \rceil \rceil_{\text{int}b} \).

**Learned power-of-two quantization.** The scaling factor can be learned to find a more optimal representation range, particularly as improving the precision of smaller values might be more important for the end-to-end accuracy compared to having less clamped values.

The quantization function is a multi-step function and its derivative is zero almost everywhere thus preventing meaningful training. We approximate the gradient with the straight-through estimator \( \tilde{\nabla}x = \begin{cases} \tilde{x}, & \text{if } x < \text{clamping threshold} \\ 0, & \text{otherwise} \end{cases} \).

Instead of training the scale value \( s \), we can use learned scaling factors for \( s = 2^\lceil \log_2 r \rceil \) [19].

\[
\frac{\partial q(x)}{\partial \log_2(t)} = s \ln(2) \cdot \operatorname{clamp} \left( \frac{x}{s}, \frac{x}{s} - 2^{b-1}, 2^{b-1} - 1 \right)
\]

Furthermore, gradients need to be normalized for better convergence and to guarantee scale invariance for data and scaling factors, otherwise, they depend heavily on the relative distance of the input to the clamping threshold of the quantization function. For the scaling factors, we are using the Adam optimizer with its built-in gradient normalization \( \beta_1 = 0.9, \beta_2 = 0.99 \) [24]. For the other parameters, we stick to standard SGD with a separate learning rate.

**Knowledge distillation.** Knowledge distillation (KD) has been used to train compact networks (student) by minimizing the distance to a larger network (teacher). We also use KD in the proposed training flow by setting the power-of-two tapwise quantized network as the student and the floating-point baseline model as the teacher. We adopt the Kullback-Leibler divergence loss and the tempered softmax activation function [16].

As not all convolutional layers can be implemented efficiently with the Winograd algorithm, we only replace those with a \( 3 \times 3 \) kernel size and unitary stride, whereas all the others, like the \( 1 \times 1 \) pointwise convolutions, are processed using a standard algorithm. Although strided convolution can be implemented with the Winograd algorithm [65], [67], the control and compute overhead dominates the potential MACs reduction (i.e., stride-2 \( F_4 \) leads only to a \( 1.8 \times \) MACs reduction).

**IV. HARDWARE ACCELERATION**

A. Baseline Accelerator

Fig. 2 shows the architecture of our baseline inference DSA, featuring two AI cores (AIC0 and AIC1) inspired by the DaVinci architecture [36]. Each core exposes a custom instruction set architecture (ISA) and implements all functionalities necessary for processing CNN layers.

The datapath of the AI core comprises a Cube Unit for MatMuls, a Vector Unit for vector operations, and a Scalar Unit to handle scalar tasks. The Cube Unit performs a MatMul between two \( \text{int}8 \) matrices of size \( [16 \times 32] \) and \( [32 \times 16] \) to produce an \( \text{int}32 \) \( [16 \times 16] \) output matrix, which can be optionally accumulated to a third input operand. The memory access patterns are simplified by storing the input and output tensors for the Cube Unit in the fractal format [42], whereby the dimension of the tensor used as the reduction axis \( (C) \) is split into a sub-dimension of size \( C_0 = 32 \) and a super-dimension of size \( C_1 = \frac{C}{C_0} \). Thus, for instance, the data layout of the iFMs for a convolutional operation is \( \langle N, C_1, H, W, C_0 \rangle \).

The Vector Unit is \( 256 \text{B} \) wide and comprises multiple parallel lanes with a peak throughput of 128 FP16 or 256 \( \text{int}8 \) operations per cycle. It performs general arithmetic operations between vectors besides more specific ones needed in CNN workloads, e.g., data type conversion, ReLU, and pairwise reductions. The number of parallel lanes ensures that the throughput of the Vector Unit matches the output data rate of the Cube Unit for relevant CNN workloads.

The on-chip memory hierarchy follows a multi-level organization, where \( L0A \) and \( L0B \) serve as the input buffers for the Cube Unit and \( L0C \) as its output buffer, \( UB \) as the input and output buffer for the Vector Unit, and \( LI \) as the second level memory. The memory hierarchy is fully software-managed by the memory transfer engines (MTEs), which perform data movements and layout transformations. Specifically, the MTE2 is in charge of transferring chunks of data from global memory (GM) to \( LI \) or \( UB \), whereas the MTE3 of transferring data from \( UB \) to \( GM \) or to \( LI \) for fusing.
multiple consecutive layers. The MTE1 transfers input tiles from L1 to L0A or L0B and can optionally perform the im2col transformation \[8\] to lower a 2D convolution into a MatMul. The im2col engine supports 3, 5, and 7 as kernel sizes and 1 and 2 as stride parameters. The FixPipe module within the Vector Unit transfers the output of the Cube Unit from L0C to UB, potentially performing re-quantization operations on-the-fly.

The size and the number of banks of the on-chip memories are tuned to minimize the area while having enough bandwidth and capacity to avoid blocking the computational units. Specifically, L0A and L0B can feed one operand per cycle to the Cube Unit without incurring bank conflicts. Similarly, LOC can sustain write and read operations from the Cube Unit at the potential rate of one output tile per cycle, and it also has an additional read port towards the FixPipe module. LI has a rather complex addressing scheme and multiple read and write ports, managing bank conflicts at run time. The idle cycles caused by bank conflicts can be excluded from the critical path by exploiting data reuse in other memories.

The AI core relies on an in-order scalar front-end to offload instructions to the MTEs, the Vector Unit, and the Cube Unit. All units have a private instruction queue and a \(p\)-sequencer to repeat the same instruction on different data and reduce the dispatching overhead. Specifically, the current ISA of the core requires an instruction repetition factor and one stride parameter for each operand. Furthermore, the core also implements a form of \textit{decoupled access/execute strategy} \[37\] as the different units are synchronized with an explicit token exchanging mechanism \[48\]. Such a mechanism allows the programmer to control the overlap between data movements and compute operations.

We decided to use an accelerator based on a MatMul engine as our baseline since it represents a versatile and flexible design choice compared to a fully spatial architecture like Eyeriss \[9\] or MAERI \[28\]. Specifically, having an AI core grounded in linear algebra eases the development of the compiler infrastructure needed to support the growing diversity of AI workloads \[51\]. However, in the following section, we will present the microarchitectural space of the Winograd transformation blocks such that they can be tuned for the characteristics of the target accelerator system.

**B. Winograd Extensions**

1) \textit{Winograd Transformation Engines:} The Winograd transformations \(B^T x B, GfG^T, \text{ and } A^T YA\) from Eq. (1) can be generalized as follows:

\[
T \times s \times T = T \times \tilde{s},
\]

where \(T\) is a generic constant \([h_T \times w_T]\) transformation matrix, \(s\) is a \([h_T \times h_T]\) tile of the iFMs, oFMs, or weights, depending on the specific transformation. The operations in Eq. (4) are repeated multiple times to transform the entire input tensor, namely, \(\frac{H \times W}{m} \times C_{in/out}\) for the input/output transformations, and \(C_m \times C_{out}\) for the weight transformation.

To design an area- and power-efficient transformation engine, we unroll the whole Winograd transformation (Eq. (4)) into a flat data flow graph (DFG), which can be heavily optimized by exploiting that we only use integer operations and that the \(T\) matrix is constant and known at design time. Specifically, as the transformation matrices have many symmetries and common terms, we apply common subexpression elimination (CSE) to share computations in time or space, reducing the number of cycles or resources needed. Moreover, as most values in the transformation matrices are powers-of-two, we avoid using multipliers and carry out the computation using only shifters and adders. The few multiplications with non-power-of-two numbers are split into multiple shift-and-add operations, e.g., \(c = 5 \cdot a = (a << 2) + a\). The bitwidth is kept to the minimum for each intermediate operation. Finally, we perform the scheduling and resource allocation of the DFG, exploring different area-throughput trade-offs, and selecting the solution that works best based on the requirements of the target transformation. Specifically, we devise two high-level implementation strategies, which we denote as \textit{row-by-row and tap-by-tap transformation engines}.

In the \textit{row-by-row transformation engine} (Fig. 3a), we decompose the transformation operation (Eq. (4)) as a series of vector-matrix multiplications \(s \times T\), which we map on a spatial processing element (PE). Specifically, the PE reads one row at a time of the matrix \(s\) and performs the entire operation \(\tilde{s} = s \times T\) in multiple cycles. The PE hardcodes the multiplication of the input vector with the matrix \(T\), using only adders and fixed shifters. The second part of the Winograd transformation, namely, \(T^T \times \tilde{s}\), can be computed using the already allocated resources (\textit{slow solution}) or using additional spatial resources inside the PE (\textit{fast solution}). The former saves resources at the cost of higher latency, requiring only an additional set of \(h_T \times w_T\) registers to store the intermediate results. The latter requires additional \(w_T \cdot w_T\) lanes to compute \(s_w\) in an output-stationary fashion, reducing the number of required cycles but increasing the number of adders needed. Moreover, the former solution produces one row of the output matrix at a time, whereas the latter produces the entire output matrix. As shown in Fig. 3a, the PE can be replicated to perform multiple transformations in parallel. \(P_t\) and \(P_e\) represent the two factors controlling the number of parallel transformations along the channels and the spatial dimension, respectively. The parallelization strategy is not only constrained by the area budget but also by the memory bandwidth and access pattern requirements. Specifically, the row-by-row engine requires all the elements of a spatial row to be contiguous in memory and the memory bandwidth to be sufficient for reading multiple rows of different tiles in the spatial dimension. Similar considerations also apply to the input channels dimension.

The \textit{tap-by-tap transformation engine} (Fig. 3b) represents
Table I

|          | Cycles/Xform | Parallel | RD BW   | WR BW  |
|----------|--------------|----------|---------|--------|
| Row-by-row |   [cycles]   | [Xforms] | [B/cycle] | [B/cycle] |
| slow     | h_T + w_T   | P_t   | P_t · P_t · h_T | P_t · P_t · h_T |
| fast     | h_T         | P_t · P_t · h_T | P_t · P_t · h_T | P_t · P_t · h_T |
| Tap-by-tap | T dependent | P_t · P_t · P_t | P_t · P_t | P_t · P_t |

Figure 3. Winograd Transformation Engines.

2) Winograd Convolutional Operator: The baseline is extended with the transformation engines (reported in bold in Fig. 2) needed for the iFM and weight transformations in the MTE1, and for the oFM transformation in the FixPipe module. The data flow of the Winograd operator for a 3×3 Conv2D layer is reported in Listing 1. It refers to the computation of a subset of the channels of the oFMs, and it works as follows.

First, a tile of the weights is transferred from GM to LI and transformed to the Winograd domain (lines 2 – 6). Each core operates on different output channels of the weights (line 2). LOB is used as an intermediate buffer to store the weights before the transformations. Thus, the data transfer is carried out in tiles (line 5), each tile is transformed using the weight transformation engine within the MTE1 module, and the output is stored in LI (line 6). In order to overlap data transfers and the weight transformation, LOB is double-buffered (line 4), and proper token exchanging instructions synchronize the transfers performed by the MTE2 with the transformations performed by the MTE1. For simplicity, such synchronization instructions are not shown in the pseudocode. The transformed weights are kept stationary in LI and reused for all the iFMs. Three levels of loop blocking are used to perform double-buffering across the entire on-chip memory hierarchy, maximizing the concurrency between compute, data movement, and Winograd transformation operations. Specifically, in the outer-most loop block (lines 8 – 10), the load of the iFMs from GM (line 11) is overlapped with all the core-level compute and data-movement operations (lines 13 – 26). In the loop block in the middle (lines 13 – 15), the input transformation and the cube operations (lines 17 – 23) are done in parallel with the output transformation (line 24), the re-quantization step (line 25), and the write to GM (line 26). In the innermost loop block (lines 17 – 20), the input transformation (line 21) is overlapped with the batched MatMuls performed in the Cube Unit (lines 22 – 23).

Matching the production and consumption rates is key to maximizing the Cube Unit utilization, so compute efficiency. As any overhead in the innermost loop will be multiplied by the total number of outer iterations, matching the input transformation production rate with the Cube Unit consumption

a different point of the optimization space, where the DFG of Eq. (4) is completely unrolled in time. The PE is very simple in this solution, comprising only a configurable shifter, an adder/subtractor, and an accumulator register. Thus, in the worst case, the PE takes h_T · h_T cycles to compute one tap. Luckily, we can exploit two properties of the transformation matrices to reduce the total number of cycles: i) the transformation matrices are sparse, lowering the average number of cycles needed per tap; ii) some taps share a significant fraction of computations with other taps, so we can apply CSE in time to avoid recomputations. Higher throughput can be achieved by replicating the PEs to perform multiple transformations in parallel. Apart from P_t and P_s, we can use the number of parallel taps in a single PE, P_t, as an additional parallelization axis. Since one input value can be read once and shared to compute multiple taps in parallel, increasing P_t does not affect the input bandwidth requirements. Moreover, by splitting the write back into multiple sub-writes, P_t does not affect the output bandwidth requirements either.

We enhance the PE with an input or an output stage comprising a configurable shifter and a rounding module to support tap-wise quantization. The number of quantization stages depends on the number of taps produced or consumed in parallel per cycle. The overall performance and requirements for the two implementation styles are summarized in Tab. I.

In the following section, we will detail the data flow of the Winograd Operator, illustrating the motivations behind our specific design choices.
rate has the highest priority. As reported in Section IV-A, the fractal data layout \(N, C_1, H, W, 32\) is used for the iFMs in \(L_1\), making 32 input channels and the spatial dimension \(W\) contiguous in memory. This represents a perfect fit for the row-by-row engine as, given the read bandwidth of \(L_1\) and the write bandwidth of \(L_0A\), it allows us to replicate the PEs 32 times along the \(C_m\) dimension and two times along the \(W\) spatial dimension, performing up to 64 transformations in parallel. With this parallelism, the transformation engine has a production rate of 64 \(\text{MB/s}\), which is 4x slower than the consumption rate of the Cube Unit. Thus, to avoid blocking the Cube Unit, we need to reuse the transformed iFMs four times across the output channels, with two main consequences. First, we need to compute at least 4-16 output channels at a time. Second, \(L_0\) should store at least 64-16-36 \(\text{int}32\) elements, that is a total size of 288kB considering double-buffering. Note that the row-by-row engine produces multiple taps per cycle, which are read by the Cube Unit in different cycles. Thus, we enhance the addressing capabilities of \(L_0A\) with a diagonal write mode such that different rows of different banks can be accessed with one single memory access. As reported in the experimental results section, this modification has a negligible area and power overhead.

To keep the overall pipeline busy, the computations related to an input tile must be overlapped with the output transformation of the previous tile. In the case of the output transformation engine, the choice of the transformation engine to use was mainly driven by the need to minimize the number of memory accesses. The tap-by-tap engine reads multiple times the same data from the input memory, which is too costly in the case of \(L_0C\) as data is stored in \(\text{int32}\). Thus, we rely on the row-by-row engine for the output transformation engine. With the available \(L_0C\) bandwidth, up to 16 transformations can be performed in parallel along the output channel dimension. Thus, a volume of \(36 \cdot C_m \cdot \frac{W}{H} \cdot \frac{H}{4} \cdot 16\) \(\text{MB} / \text{s}\) feature map (taps) in the Winograd domain will be transformed in \(\frac{C_m}{16} \cdot \frac{W}{H} \cdot \frac{H}{4} \cdot 16\) or \(\frac{C_m}{16} \cdot \frac{W}{H} \cdot \frac{H}{4} \cdot 6\) cycles, depending on the chosen row-by-row engine solution. The same volume of data is produced by the Cube in \(\frac{C_m}{16} \cdot \frac{W}{H} \cdot \frac{H}{4} \cdot 16\) \(\text{MB} / \text{s}\) for the fast engine and 6 \(\text{MB} / \text{s}\) for the slow one \((C_m=192)\). As many layers of SoA networks have less than 192 input channels, we decide to use the fast engine. Moreover, as the Cube Unit writes the taps in different rows of \(L_0C\), the output transformation engine performs a gather operation to collect one row of the input matrices.

Finally, the read and write operations to and from \(GM\) must match the processing time of all the core-level operations. As the weights are read from \(GM\) and transformed on the fly (lines 2-6), the throughput of the weight transformation engine should match the external bandwidth. In this case, we rely on the tap-by-tap transformation engine as it produces the output data precisely in the data layout expected by the Cube Unit for the weights. Moreover, the layout of the weights can be reorganized offline such that we can avoid gathering operations when the PE reads the weights from the memory. With two available AI cores, we need to read at least \(2 \cdot 16 \cdot 18 \cdot C_m\) B of iFMs and to write \(2 \cdot 16 \cdot 16 \cdot 64\) B of oFMs to match the cores throughput, which corresponds to a \(GM\) bandwidth of \(2 \cdot 72 + \frac{C_m}{16}\) B/cycle assuming a peak compute efficiency for the core-level operations (lines 13-26). Being this requirement hardly met when the AI Core clock frequency is in the order of the hundreds of MHz, we apply three system-level and data flow optimizations. First, as the two cores work on different sets of output channels, the iFMs can be shared between the two cores, almost halving the required bandwidth. To this end, the cores are connected to the memory controllers via a Broadcast Unit (\(BU\) in Fig. 2). The \(BU\) can either accept independent memory requests from the MTEs of the two cores and transfer them to the memory controllers or process special broadcast requests in the form of a streaming access pattern [61]. When the BU retrieves two broadcast memory requests from the two cores, it acts as a DMA and broadcasts data from GM to the MTEs of the cores. To avoid deadlock, the \(BU\) has two separate queues for non-broadcast and broadcast requests, where the latter are served with higher priority. Second, when the iFMs shape is larger than \(18 \times 18\), the volume to be transferred can be reduced by exploiting the halo regions that characterize the unitary-stride \(3 \times 3\) Conv2d operator. Third, by prefetching input tiles and allocating multiple output buffers (instead of just two for double buffering), it is possible to decouple read and write operations, prioritizing the more critical read

```c
// WEIGHT Blocking
for (wt_tile_l0b in WT_GM[2*out_tile_sz + block_id;...].
get_next_tile
    cin_l0b_tile_sz, cout_l0b_tile_sz,
    double_buffering=True);
mt2.transfer(wt_tile_l0b, wt_tile_l0b)
mtl.weight_xform(wt_tile_l0b, wt_tile_l1[...])
// IFM L1 Blocking
for (ifm_l1_tile in IFM_GM.get_next_tile(
    batch_l2 Tile_sz, h_out_l2 Tile_sz,
    w_out_l2 Tile_sz, double_buffering=True)
mtl.transfer(ifm_l1_tile, ifm_l2(Tile), broadcast=True)
// IFM L0 Blocking
for (ifm_l0_tile in ifm_l2_tile.get_next_tile(,
    batch_l0a_tile_sz, h_out_l0a_tile_sz,
    w_out_l0a_tile_sz, double_buffering=True):
mtl.input_xform(ifm_l0, ifm_l0a_tile)
cube.mmad(ifm_l0a, wt_tile_l1[...],
out_l0c_tile[...])
vec.unit.out_xform(out_l0c_tile, out_prescale ub_tile)
vec.unit.conv(out_prescale ub_tile,
out_postscale ub_tile, alpha_q)
mtl3.write(out_postscale ub_tile, OUT_GM[;])
```

Listing 1. Dataflow of the Winograd operator
transfers.

V. EXPERIMENTAL EVALUATION

A. Tap-wise Quantization Algorithm

1) Datasets and Baseline Networks: We use two common image classification datasets, namely, CIFAR-10 [26] and ImageNet ILSVRC [55], to compare the proposed quantization flow with other Winograd-based algorithms. CIFAR-10 has 60k 32×32 RGB images divided into 10 classes, and ImageNet 1.4M 224×224 RGB images divided into 1k classes. We split the datasets into training (90% of 50k/1.3M training set), validation (10% of 50k/1.3M training set, used for learning rate scheduler), and test set (10k/100k, inference only). We use the standard preprocessing methods: random horizontal flip (training set only) and color normalization for CIFAR-10; resize, random crop, and color normalization for ImageNet.

We benchmark ResNet-34 and ResNet-50 for the ImageNet dataset, where we use the pre-trained networks from Torchvision. The baseline networks (im2col/FP32) achieve 72.6%/75.5% Top-1 and 90.7%/92.6% Top-5 accuracy on the test set. For CIFAR-10, we re-implement the ResNet-20 [15] and train it from scratch (94.4%). Furthermore, we use a light-version of VGG [49], used by Liu et al. [40] and Lance et al. [32], and replace all but the last dropout layers with batch normalization layers (92.2%). We trained the networks using PyTorch while extending the Winograd-Aware Training [11] with tap-wise quantization support.

2) Tap-Wise Quantization Evaluation: We retrain the network as a quantized int8 network from the FP32-baseline, whereas the weights and feature maps are quantized, as described in Eq. (2). All networks can be trained using 8-bit integers without any loss of precision. We train the Winograd $F_2$ ResNet34 on Imagenet following the (static) Winograd-Aware algorithm (Section III-A), achieving 71.4% (-1.2% drop) with 8-bit quantization. As expected, extending weights and feature map to 10 bits in the Winograd domain achieves the full accuracy because just 3 bits are required for a bit-wise quantization support. Furthermore, we train the Winograd $F_2$ version with the Winograd-Aware method and KD. The baseline Winograd $F_2$ shows a significant drop of 13.6%; even with two extra bits, the accuracy drops at least by 3.5%.

Tab. II gives an overview of the performance of ResNet-34 on the ImageNet dataset, comparing several training methods and configurations. In the second section of the table, we evaluate the tap-wise quantization with unrestricted quantization scaling factors, i.e., $s_{ij} \in \{1, 2, \ldots, 2^s\}$ and the weights by 2 to 10 bits. Particularly, the large difference between the shift values implies why quantizing with a single scalar cannot work well. Within the same tap, the distribution is in the range of 2–3 bits, but it needs to be learned independently per layer.

3) SoA Winograd-aware Quantization Methods: Recently, several approaches for Winograd-aware quantization have been presented. Tab. III gives a full overview of the main methods and of our solution. As the baseline accuracy varies across related works due to different training methods and implementation details, we report their baseline accuracy and compare relative performance. Our results are trained with the Winograd-aware method and powers-of-two tap-wise quantization, $\log_2$ gradients, and KD. The first network is ResNet-20 on CIFAR-10. Without adding any extra compute,
we improved the (static) Winograd-Aware WA accuracy from 84.3% to the full accuracy of 94.4% with powers-of-two tap-wise quantized $F_2$ [11]. Moreover, we also outperform both the WA-flex method, which trains the transformation matrices to recover some of the quantization losses [11], and the Legendre- $F_1$ method by 1.9% and 2.1%, respectively.

We retrain the light version of VGG (VGG-nagadomi [47]). Our baseline network reaches 92.0% accuracy, the tap-wise powers-of-two quantized $F_2$ performs with a drop of 1.2%, 0.1% or no drop (for int8, int8/9, and int8/10). For this network, no $F_2$ numbers have been presented in previous work, so we compare to $F_2$ results. Liu et al. prunes the weights in the Winograd domain to further reduce the compute intensity. They can retain their baseline performance of 93.3% [40]. Li et al. proposed to quantize to int8 in the Winograd domain, where they can achieve 90.3% (-0.1%) [32].

Finally, we train and compare ResNet-50 on ImageNet. We achieve 75.2% / 92.3 (-0.3% / -0.3) with 8 bits and 75.5% / 92.5 (0.0% / -0.1%) when extending the Winograd domain to 10 bits (int8/10). On such a benchmark, there are three main related works. Meng et al. uses complex root points leading to numerically more stable but complex transformation matrices [47] with a small drop, but with lower baseline (i.e., 73.2, -0.1%). Liu et al. uses the Residue Number System RNS. They use very large tile size of (i.e., 14 × 14) to compensate for the transformation overhead. Even though the RNS could perform the int8 operations losslessly (transformations and elementwise multiplications), the accuracy drops by 1.0% or 75.1%. It is expected that this is due to the quantization of the transformations matrices, furthermore, it is known [1], [29] that very large tiles introduce very high numerical error even for FP32. A very interesting approach is LoWino, they operate on FP32 weights and feature maps, but quantize linearly to 8 bits before and after the elementwise multiplication in the Winograd domain [31]. They achieve an identical accuracy of 75.5% as our method with int8/10, although with an accuracy drop of 0.6% instead of 0% as they start from a higher baseline. While LoWino provides the same reduction in operation count, it requires a 4x higher bandwidth than our proposed method, which eliminates any benefits as shown in Section V-B3. Notably, only our method with int8/10 can avoid any accuracy drop with ResNet-50.

4) Tap-wise vs. Channel-wise Quantization: Previous works have shown that fine-grain quantization strategies, particularly (output) channel-wise quantization, can significantly improve the accuracy of quantized networks [25], [35]. Therefore, in this section, we compare the tap-wise with the channel-wise quantization strategy. We use a pre-trained ResNet-34 from Torchvision, and we evaluate the quantization error on the weights, although similar trends can also be observed for the feature maps. The scaling factors $s$ are determined as follows:

$$\gamma = \arg \min_{\gamma} \sum_{f} |\text{Quant}_{\mu,s}(f) - f|/|f|, \quad s = \gamma \sigma/2^{n-1},$$

where $\text{Quant}_{\mu,s}(x) = \mu + s[(x - \mu)/s]_{\text{int}n}$ and the mean $\mu$, the standard deviation $\sigma$, and the optimized scaling factor $\gamma$ are obtained per layer (uniform quantization strategy), per channel, or per tap.

Fig. 4a shows the distribution of relative quantization error (in log2 scale) of all layers with kernel size 3 × 3 for a uniform and for a channel-wise quantization strategy in the spatial domain for $n = 8$ bits. Channel-wise quantization reduces the mean relative error by 1.7 × , namely, from $2^{-6.01}$ to $2^{-6.72}$. Fig. 4b shows, instead, the error distribution for uniform, channel-wise, and tap-wise quantization in the Winograd domain. Specifically, we quantize in the Winograd domain (i.e., $\text{Quant}(GfG^T)$), and then we transform the values back to the spatial domain to compare the error introduced by the quantization process. We calculate the Moore-Penrose inverse of the transformation matrices based on SVD to transform the quantized weights back to the spatial domain. In this case, the improvement of channel-wise quantization is significantly lower as the mean relative error reduces from $2^{-5.58}$ to $2^{-5.62}$. On the other hand, tap-wise quantization shows much better performance ($2^{-3.3}$), leading to a mean error as low as $2^{-6.78}$.

Combining channel-wise with tap-wise quantization further improves the average error by 1.06× at the cost of a much more complicated compute phase. For networks with significantly different channel distribution, the combined quantization strategy might achieve better performance.

| CIFAR-10/ResNet-20 | int8 | Top-1 | Ref. | $\Delta$ |
|---------------------|------|-------|------|---------|
| [2] Legendre (static) | $F_1$ | 8 | 85.0 | 92.3 | -7.3 |
| [2] Legendre (static) | $F_2$ | 8/9 | 89.4 | 92.3 | -2.9 |
| [2] Legendre (flex) | $F_2$ | 8 | 91.8 | 92.3 | -0.5 |
| [11] Winograd-Aware (s) | $F_2$ | 8 | 84.3 | 93.2 | -8.9 |
| [11] Winograd-Aware (f) | $F_3$ | 8 | 92.5 | 93.2 | -0.7 |
| [34] Winograd AdderNet | $F_2$ | 8 | 91.6 | 92.3 | -0.7 |
| Tapwise Quant. | $F_2$ | 8 | 93.8 | 94.4 | -0.6 |
| Tapwise Quant. | $F_2$ | 8/10 | 94.4 | 94.4 | 0.0 |
| CIFAR-10/VGG-nagadomi | int8 | Top-1 | Ref. | $\Delta$ |
| [40] Sparse | $F_2$ | FP32 | 93.4 | 93.3 | 0.1 |
| [32] Quant. Winograd | $F_2$ | 8 | 90.3 | 90.4 | -0.1 |
| Tapwise Quant. (static) | $F_2$ | 8 | 90.8 | 92.0 | -1.2 |
| Tapwise Quant. (static) | $F_2$ | 8/9 | 91.9 | 92.0 | -0.1 |
| Tapwise Quant. (static) | $F_3$ | 8/10 | 92.0 | 92.0 | 0.0 |
| ImageNet/ResNet-50 | int8 | Top-1 | Ref. | $\Delta$ |
| [47] Complex Numbers | $F_2$ | FP32 | 73.2 | 73.3 | -0.1 |
| [43] Residues Numbers | $F_2$ | 8 | 75.1 | 76.1 | -1.0 |
| [31] LoWino | $F_2$ | FP32/8 | 75.5 | 76.1 | -0.6 |
| Tapwise Quant. (static) | $F_2$ | 8 | 75.2 | 75.5 | -0.3 |
| Tapwise Quant. (static) | $F_2$ | 8/10 | 75.5 | 75.5 | 0.0 |

1Not reported. Reproduced with the open-source code [11].
B. System Evaluation

1) Experimental Setup: Area and Power. To assess the area and power consumption of the accelerator, we developed the RTL of the parts of the AI core most affected by the Winograd extensions, specifically the Cube Unit, the MTE1, and the FixPipe module.

We have implemented the design with a high-k metal gate (HKMG) 28 nm CMOS technology, and a corresponding multi-VT standard cell library at a supply voltage of 0.8 V in typical corner. We have synthesized the design and performed place-and-route, targeting a clock frequency of 500 MHz in typical operating conditions. We used an industrial-grade memory compiler for the SRAM and register file macros. We have selected input data segments from the first 3×3 layer of a ResNet-34 quantized using our method. Then we run a timing-annotated (SDF) post-place & route gate-level simulations with a cycle-accurate event-based RTL simulator. Finally, we simulate the power consumption based on the extracted switching activities (VCD).

Performance Profiling. An event-based simulator [59] was developed to model and profile the overall system. Besides modeling timing behavior, the simulator also models data movements and computation to check the correctness of the results. It was validated with micro benchmarking against the parts of the system developed in RTL. Specifically, we compared the number of cycles obtained from the RTL simulation with that estimated by the simulator. On several small and medium-sized Conv2D operations, the simulator shows a 5% worst-case difference. The simulator implements a simple model for the DRAM subsystem in which memory requests are served in order. Moreover, the completion time of a memory request depends on the maximum bandwidth (81.2 GB/cycle), which corresponds to \( \approx 0.8 \cdot 51.2 \text{ GB/s} \) given the clock frequency of the core, and on a fixed average latency (150 AI core cycles) with a jitter extracted from a zero-mean Gaussian distribution with a variance of 5 cycles. Such memory bandwidth and latency characteristics meet the expected performance of an LPDDR4x-3200 memory with two channels [13], [58]. Although we do not use a detailed model of all the DRAM resources (e.g., command scheduling, channel bandwidth, bank, and row-buffer conflicts), their effects on the performance of the cases under analysis are minimal [59] as the memory accesses are regular and follow a streaming pattern. We estimated the energy consumption by projecting the power consumption of computational units and memory obtained from the back-annotated gate-level simulations. For \( L1 \), we estimated its area and energy cost by multiplying the values obtained from the memory compiler by 1.5× to take into account the logic needed to manage bank conflicts and arbitration between read and write ports.

Workloads. To evaluate the system performance, we adopt two sets of benchmarks. The first is a synthetic benchmark suite comprising 63 3×3 Conv2D layers built using common values for batch size (B), height (H), and width (W) of the OFMs, and the number of input and output channels (C_in, C_out). The second is a benchmark suite comprising the Conv2D layers of 7 state-of-the-art CNN networks to quantify the speed-up and the energy savings on models with different architectures. Within the selected benchmarks, ResNet-34 and ResNet-50 [15] are taken as representative of computationally intensive networks used for classification tasks; RetinaNet-ResNet50-fpn [37], SSD-VGG16 [39], and YOLOv3 [53] for object detection tasks; U-Net [54] for high-resolution semantic segmentation tasks. We used the implementation of the networks available in the Torchvision Python package.

2) Area and Power Analysis: Tab. V reports the detailed area and power breakdown of the AI core and the physical layout of the implemented hardware extensions. The Cube Unit dominates both the area and the power of the compute modules, being at least 6.4× larger and requiring 6.7× more power than a single Winograd transformation engine.

Overall, all Winograd transformation engines occupy merely 6.1% of the core area. Note that most of the time, only the input and the output transformation engines are active simultaneously, whereas the power cost of the weight transformation engine is amortized over the computations of all activations.

Thus, the Winograd extension adds \( \approx 17\% \) of power.
Table IV
THROUGHPUT OF THE WINOGRAD OPERATOR NORMALIZED TO THE IM2COL OPERATOR FOR DIFFERENT \(3 \times 3\) Conv2D layers with stride equals to 1 and padding same. \(H, W\) refers to the output resolution.

| B  | 1  | 8  |
|----|----|----|
| Cin | 64 | 128 | 192 | 256 | 384 | 512 | 64 | 128 | 192 | 256 | 384 | 512 | 64 | 128 | 192 | 256 | 384 | 512 | 512 |
| Cost | 16 | 5.09 | 6.00 | 6.03 | 6.13 | 6.13 | 6.26 | 6.03 | 6.12 | 6.09 | 6.30 | 6.19 | 6.19 | 6.30 | 6.19 | 6.30 | 6.19 | 6.19 | 6.30 | 6.19 | 6.19 |

Table V
AI CORE breakdown at 0.8 V and 500 MHz. Power consumptions marked with \(\ast\) refer to the IM2COL kernel, or with \(\dagger\) to the \(F_3\) Winograd kernel. The cube TOPs/W reported for the \(F_3\) Winograd kernel are computed using the equivalent TOP in the spatial domain, i.e., \(4 \times \) the TOP of the Cube Unit.

| Unit    | Area      | Peak Power | TOPs/W |
|---------|-----------|------------|--------|
| Cube    | 2.04mm\(^2\) (19.2\%) | \(\ast\)1521mW | +5.39 |
|         | \(\dagger\)1923mW | +17.04 |
| IM2col  | 0.03mm\(^2\) (0.3\%) | 30mW | 5.3 |
| MTE1 IN\_XFORM | 0.23mm\(^2\) (2.2\%) | 145mW |
| MTE1 WT\_XFORM | 0.32mm\(^2\) (3.0\%) | 228mW |
| FIX\_PIPE OUT\_XFORM | 0.10mm\(^2\) (0.9\%) | 114mW |

3) Throughput Analysis: Table IV shows the speed-up of the Winograd operator compared to the im2col for different parameters of a \(3 \times 3\) Conv2D layer. Although the performance of the Winograd algorithm is highly dependent on the characteristics of the workload, we can identify two macro-trends.

Larger resolution or batch size \(\rightarrow\) higher speed-up. As explained in Section IV-B2, we adopt a weight-stationary dataflow, where the weights are reused for all the iFMs. Thus, when the reuse of the weights is small, the performance is limited by the transfer of the weights. For example, the speed-up increases from 1.98 to 3.30 when the resolution increases from 32 \times 32 to 128 \times 128 with 256 input and output channels at batch size equal to 1, and from 1.98 to 3.18 when changing the batch size from 1 to 8 at iso-resolution (32 \times 32). To better visualize the bottlenecks for different workloads, Fig. 5 shows the cycle usage breakdown of the critical path of the Winograd operator normalized to the im2col (hatched bar). Specifically, comparing the first and the third workloads in Fig. 5, a batch size of 8 instead of 1 decreases the normalized percentage of cycles occupied by weight transfer and weight transformations from 13% to 2%. Note that the throughput of the weight transformation engine has been tuned to match the external weight transfers while occupying the minimum area. Thus, removing the contribution of the weight transformation engine will reveal another critical path where the weight data transfer takes the place of the transformations. This analysis also shows the need for transforming the weights on-the-fly instead of reading the transformed weights from the external memory. As the weights in the Winograd domain are 4 \times larger than in the spatial domain, the load overhead will be much higher and difficult to amortize.

Larger number of input channels \(\rightarrow\) higher speed-up. A larger number of input channels increases the output reuse within the core, reducing the memory bandwidth occupied by the write operations of the oFMs. This increased data reuse frees bandwidth for the transfer of the iFMs,
with a remarkable effect on performance as the iFMs are broadcasted to the two cores. For example, the speed-up increases from $2.62 \times$ to $3.18 \times$ when increasing the number of input channels from 128 to 256, with batch size equal to 8, spatial resolution equal to $32 \times 32$, and output channels equal to 256. In Fig. 5, having more bandwidth to reserve for the iFMs transfer reduces the cycles occupied by the MTE2 from 5% to 2% for the first two workloads and from 15% to 6% for the last ones. The lack of bandwidth represents, in fact, the main reason why the $F_2$ Winograd operator does not achieve the theoretical $4 \times$ speed-up on our system. As shown in Fig. 5, the input and the output transformation engines never become the bottleneck of the operator as their throughput was sized to exactly match the input and output data rate of the Cube Unit.

4) Comparison with NVDLA: In Tab. VI, we compare our accelerator system with the open-source NVDLA accelerator version 1 which supports direct convolution (in FP16 and INT8) and Winograd $F_2$ (FP16 only) with an on-chip memory of 512 kB per engine [52]. As NVDLA does not provide any tools to convert a model that can be used with its compiler into a format accepted by its verification infrastructure, we have modified the Linux driver used in the virtual platform to write out the sequence of reads and writes from/to the control and status registers of the accelerator, which we then use to simulate the RTL for performance benchmarking. The results are compared with the expected values for functional correctness.

The results are summarized in Tab. VI. As a single NVDLA core has a peak throughput of 1 TOp/s at 1 GHz, we use 8 NVDLA engines to match the peak throughput of our system, namely, 8 TOp/s. We consider two different configurations for the NVDLA-based system: the leftmost column in Tab. VI refers to a system with quasi-infinite bandwidth, whereas the middle column refers to a system with 42.7 Gword/s, i.e., 85.4 GB/s in FP16, to match the more realistic bandwidth constraints of our system, i.e., 41 Gword/s (41 GB/s with INT8 for our system, 82 GB/s with fp16 for NVDLA). We use words rather than bytes for the iso-bandwidth evaluation, as the public NVDA version only supports FP16, and it can be expected that the performance scales with the word width. Even though NVDLA with quasi-infinite bandwidth gets close to the theoretical $2.25 \times$ speed-up, our accelerator still outperforms NVDLA by 21 to 50%. In the more realistic scenario of the system with limited external bandwidth, Winograd convolutional algorithm on NVDLA becomes strongly memory-bound, which significantly reduces its benefits over the direct convolutional algorithm. One of the reasons behind this degradation is that NVDLA needs the weights to be transformed offline, increasing the transferred weight volume by $4^2/3^2 = 1.78 \times$. Furthermore, if the input feature maps of a single layer cannot be stored entirely on-chip, they need to be transferred multiple times from external memory, which leads to cases where the Winograd kernel works even worse than the direct convolution. Overall, our accelerator system runs between 1.5 and 3.3x faster than NVDLA at the same peak throughput and same external bandwidth, thanks to using Winograd $F_4$ vs. $F_2$, bandwidth optimization through on-the-fly weight transformation, and higher utilization.

5) Full Network Evaluation: Tab. VII reports the evaluation of the proposed system on various state-of-the-art CNNs. The $F_2$ Winograd operator increases the throughput of the $3 \times 3$ compute-heavy Conv2D layers by $1.9 \times$ on average and up to $2.60 \times$. The gain on the throughput of the entire network depends on the specific architecture. In fact, the benefits of the Winograd Algorithm are lower for the networks with many $1 \times 1$ convolutions, like ResNet-50, compared to the networks dominated by the $3 \times 3$ convolutions, like U-Net or YOLOv3. However, the Winograd algorithm becomes remarkably beneficial when increasing the batch size or the input resolution. For example, for ResNet-34, the speed-up achieved increases from $1.07 \times$ to $1.36 \times$ when using a batch size of 16 instead of 1. Even more remarkable is the improvement on SSD-VGG-16 when increasing the batch size, with the speedup going from $1.55 \times$ to $1.83 \times$.

In Tab. VII, we also report the throughput of the $F_2$ Winograd operator implemented following the same methodology described in Section IV for $F_2$ and the same dataflow reported

---

Table VI

| Workload | NVDLA | Winograd | Ours |
|----------|-------|----------|------|
| Batch, HW, Cin, Cout | 8, 32, 128, 128 | 8, 32, 128, 256, 256 |
| Peak Throughput | 8 TOp/s | 8 TOp/s |
| Bandwidth | 128 Gword/s | 42.7 Gword/s |
| iso-bandwidth | 256 Gword/s | 41 Gword/s |

---

Figure 5. Cycle Breakdown for im2col vs. Winograd $F_2$.
in Listing 1. When the 2.25× computational reduction introduced by the $F_2$ operator makes the workloads of the layers memory-bound, $F_2$ and $F_3$ achieve similar performance, although the $F_3$ configuration always outperforms the $F_2$. However, when increasing the batch size or the input resolution, or for very compute-heavy networks such as SSD-VGG-16, YOLOv3, and U-Net, $F_3$ increases the throughput w.r.t. to $F_2$ up to 1.4×. To highlight the benefits of the Winograd $F_4$ algorithm, Tab. VII also shows the speed-up w.r.t. to the im2col algorithm for a system with a higher bandwidth (1.5×, i.e., the ratio between a DDR5 and a DDR4 memory). In this case, while Winograd $F_2$ hits a plateau around ≈ 1.8× of speed-up, the Winograd $F_3$ exploits the additional external memory bandwidth to double the end-to-end throughput compared to the baseline.

Overall, Winograd $F_3$ outperforms both im2col and $F_2$ in most cases, even though the improvements over $F_2$ are not always remarkable and highly dependent on the shapes of the specific layers of the network. Specifically, the presence of the Winograd transformation engines not only constrains the dataflow within a single AI core but also limits the feasible loop transformations, e.g., reordering and blocking, that can be applied on the outer loops of the convolution operation. Moreover, the spatial resolution of the output activation tiles must be a multiple of 4, limiting the choice of tiling factors and, in some cases, requiring zero-padding and adding ineffective computations. All these additional constraints affect the data reuse in the core and the access patterns to the external memory, making the bandwidth limitations even more visible. Further proof is given by the layer-wise analysis in Tab. VII, which reveals that not the same layers of the network are mapped either on Winograd $F_2$ or on Winograd $F_3$ depending on the available extension. For example, for YOLOv3 with an input resolution of 256 and batch size 1, the Winograd $F_2$ outperforms Winograd $F_3$ because it is used to process the deep layers of the network where the small spatial resolution ($\leq$ 16×16) makes the Winograd $F_2$ perform worse than the im2col algorithm. However, for the YOLOv3 with an input resolution of 256 and batch size 8, Winograd $F_3$ results in a 1.4× higher throughput than Winograd $F_2$ (i.e., with DDR4). Apart from the throughput gain, which could be lower than the theoretical 4× FLOPs reduction, the Winograd $F_3$ still reduces the utilization of the MatMul engine, usually the most power-hungry computational resources. Therefore the overall energy efficiency is improved, which is analyzed in the following paragraphs. Thus, depending on the application use cases and the area budget, accelerator designers can use the methodology presented in Section IV to develop the transformation engines for Winograd $F_2$ and to integrate them together with the Winograd $F_3$ ones, allowing the compiler to select the best computational kernel for each layer of the network.

Table VII

| Network       | Batch | Res. | $\text{im2col}$ | $F_2$ | $F_3$ vs. $\text{im2col}$ | $F_4$ vs. $\text{im2col}$ | $F_2$ vs. $F_3$ | $F_2$ vs. $F_4$ | $F_3$ vs. $F_4$ |
|---------------|-------|------|-----------------|------|---------------------------|---------------------------|----------------|----------------|----------------|
| ResNet-34     | 1     | 224  | 921             | 950  | 1.03x (1.29x)             | 1.07x (1.39x)             | 1.04x (1.08x) | 1.07x (1.15x) | 1.10x (1.52x)  |
| ResNet-50     | 1     | 224  | 669             | 676  | 1.01x (1.28x)             | 1.02x (1.37x)             | 1.01x (1.06x) | 1.02x (1.14x) | 1.03x (1.51x)  |
| ResNet-50     | 1     | 224  | 718             | 724  | 1.02x (1.32x)             | 1.03x (1.37x)             | 1.01x (1.06x) | 1.02x (1.14x) | 1.03x (1.51x)  |
| YOLOv3        | 1     | 256  | 317             | 349  | 1.10x (1.34x)             | 1.13x (1.46x)             | 1.03x (1.09x) | 1.15x (1.47x) | 1.16x (1.41x)  |
| SSD-VGG-16    | 1     | 300  | 162             | 243  | 1.50x (1.59x)             | 1.55x (1.89x)             | 1.03x (1.19x) | 1.58x (1.75x) | 1.71x (2.05x)  |
| U-Net         | 1     | 572  | 46              | 75   | 1.16x (1.71x)             | 1.74x (2.18x)             | 1.07x (1.27x) | 1.75x (1.85x) | 2.00x (2.49x)  |
| SSD-VGG-16    | 8     | 300  | 176             | 304  | 1.68x (1.71x)             | 1.83x (1.97x)             | 1.09x (1.15x) | 1.74x (1.77x) | 2.06x (2.26x)  |
| YOLOv3        | 8     | 256  | 496             | 664  | 1.33x (1.72x)             | 1.37x (2.40x)             | 1.03x (1.40x) | 1.42x (1.87x) | 1.51x (2.32x)  |
| ResNet-34     | 16    | 224  | 1472            | 2000 | 1.22x (1.73x)             | 1.36x (1.93x)             | 1.11x (1.12x) | 1.24x (1.52x) | 1.46x (2.29x)  |
| ResNet-50     | 16    | 224  | 816             | 848  | 1.05x (1.73x)             | 1.07x (1.90x)             | 1.02x (1.10x) | 1.06x (1.51x) | 1.10x (2.25x)  |
| YOLOv3        | 8     | 256  | 480             | 672  | 1.38x (1.92x)             | 1.38x (2.60x)             | 1.00x (1.35x) | 1.44x (2.01x) | 1.51x (2.46x)  |

Figure 6. Number of memory accesses (left) and energy breakdown (right) for Winograd $F_4$ w.r.t. $\text{im2col}$. 
as the weights are transformed on the fly in the core. On the other hand, the write accesses to \( L1 \) increase due to the expansion factor caused by the Winograd transformation, namely \( \frac{(m+2)2}{m} = 4 \) in the case of \( F4 \). The read accesses to the weights in \( L1 \) increase significantly, as the Cube Unit directly reads the weights from \( L1 \) instead of storing and reusing them in \( LOB \), as the im2col operator does. Nevertheless, the \( F4 \) Winograd algorithm reduces the total number of weight reads to one-fourth, and, as the \( L1 \) energy access cost is only \( 3 \times \) higher compared to that of \( LOB \), it also lowers the overall energy consumption. All the accesses to \( LOB \) are due to the weight transformations only, and so its cost is highly amortized over time. The read accesses to the iFMs in \( GM \) slightly increase, as the write accesses to \( L1 \), because the data reuse factor, i.e., the number of output channels, is limited to \( 64 \). The read accesses to the iFMs in \( L1 \) and the write accesses to \( LOA \) decrease as the Winograd transformation increase the volume of the iFMs only by a factor of \( \frac{(m+2)2}{m} = 2.25 \) for \( m = 4 \) instead of \( 9 \) as the im2col for a \( 3 \times 3 \) convolution. As the total number of Cube Unit active cycles decreases, so does the number of read accesses to \( LOA \). The number of read and write accesses to \( LOC \) is higher as the oFMs are in the Winograd domain. Overall, the energy spent on the memory subsystem is comparable between \( F4 \) Winograd and the im2col operator, yet the Winograd \( F4 \) algorithm lowers more than \( 2 \times \) the total energy consumption as it reduces the active cycles of the Cube Unit, which, as shown in Fig. 6, dominates the energy consumption of the core. This analysis reveals another key advantage of the Winograd \( F4 \) algorithm compared to the im2col and the Winograd \( F2 \) algorithm: although the theoretical \( 4 \times \) MACs reduction may not always translate into an equivalent throughput increase, it guarantees a higher energy efficiency, which makes it a perfect fit for inference DSA.

VI. RELATED WORK

Winograd Algorithm. Several works have been proposed to extend the original Winograd algorithm [62] to work on general 2D convolution [29], [65], [67], and to improve its performance by combining it with the Strassen algorithm [69] or its numerical accuracy by using higher-order polynomials [4] and better polynomial root points for \( m > 4 \) [1], [3]. Li et al. [34] combined the Winograd algorithm with AdderNet, which uses \( \ell_1 \) instead of \( \ell_2 \) norm for feature extraction, therefore replacing all MAC operations with additions. However, on CIFAR-10/ResNet-20, the proposed method introduces an accuracy drop from 92.3% for the FP32 baseline to 91.6%. Sparsity has been extensively used to reduce the computational complexity of CNNs. Liu et al. [40] and Li et al. [33] proposed to move the ReLU activation layer after the input transformation and to prune the weights in the Winograd domain. However, they use FP32 networks and only report the reduction of the number of MACs. Combining pruning with tap-wise quantization and assessing its benefit on a hardware accelerator represents an interesting future work direction.

Quantized Winograd. Gong et al. [20] and Li et al. [32] proposed to quantize \( F2 \) in the Winograd domain with a single quantization scalar per transformation. Meng et al. [47] extended the algorithm to use complex root points, increasing the number of valid root points for Winograd \( F4 \). Liu et al. [43] proposed to combine Winograd and Residue Number System (RNS), selecting 8 bit moduli 251,241,239 and Winograd \( F4 \). Fernandez et al. [11] proposed Winograd-Aware Training for Quantized Neural Networks, where gradients are propagated through the Winograd Domain. In the case of \( F4 \), they had to re-train the transformation matrices (WA-flex), making the transformation operation dense and introducing FP32 MACs. Barbaz et al. [4] extended the work of Fernandez et al. [11] using Legendre polynomial bases, where 6 additional sparse diagonal matrix multiplications are required. Li et al. [31] proposed to use FP32 feature maps and weights but to quantize the weights and feature maps in the Winograd domain. In this way, the elementwise multiplication can be performed using \( \text{int}_8 \), whereas the input and output transformations are carried out in FP32.

Custom Winograd Accelerators. Several custom accelerators targeting FPGAs were proposed to accelerate the Winograd algorithm [41], [44], [66]. They comprise a spatial architecture capable of performing only the Winograd algorithm, whereas we propose a methodology to integrate Winograd support in a programmable AI accelerator based on a high-throughput MatMul unit, which is the most adopted solution for ASIC accelerators. Wang et al. [60] proposed a RISC-V extension to support Winograd transformations efficiently. Xygkis et al. [64] proposed a solution to map the \( F2 \) Winograd operator on a general-purpose edge device with Vector Units. The closest proposal to our work is WinDConv [45], an accelerator based on NVDLA [52] which supports the \( F2 \) Winograd operator with a fused datapath. Unfortunately, a one-to-one comparison is difficult as they targeted a mobile application scenario, they reported a post-synthesis-only evaluation using a much newer technological node, and they did not consider the effects of external memory on the performance. However, their Winograd extension leads to an increase in energy efficiency over their baseline of \( 1.82 \times \) in the best case, i.e., considering 100% of utilization, whereas our proposal achieves a 2.1 \times increase of the energy efficiency on average for 12 state-of-the-art CNNs. Moreover, they also quantize to 6 bits in the spatial domain, which leads to a higher accuracy drop [50] than the proposed tap-wise quantization flow.

Winograd SW optimizations. Several efficient SW implementations of the Winograd algorithms were recently proposed for GPGPUs [7], [23], [38] and CPUs [30], [46]. All these papers adopt similar loop-level optimizations, such as loop unrolling, parallelization, or vectorization, to make
the most of the targeted platforms, whose characteristics and constraints differ significantly from ours.

VII. CONCLUSION

We presented the tap-wise quantization algorithm to enable efficient quantized Winograd on 4x4 tiles $F_3$. Using 8-bits integers for the feature maps and weights and 10-bits integers in the Winograd domain, the $F_3$ Winograd network achieves the same accuracy as the FP32 baseline for ResNet-20 and VGG-nagadomi on the CIFAR-10 benchmark and for ResNet-50 on the ImageNet classification task. The proposed method outperforms the state-of-the-art integer-only and $F_4$-aware quantization methods on all the tested networks and tasks. Furthermore, we presented a custom HW extension to efficiently process $F_4$ integer Winograd layers and its integration into an industrial-grade AI accelerator. Our proposed system outperforms NVDLA with its Winograd $F_2$ extension by 1.5 to 3.5x at the same compute throughput and bandwidth constraints due to the higher computational reduction from $F_3$, optimized bandwidth requirements by on-the-fly transformations, and higher utilization thanks to the optimized dataflow. The proposed hardware extensions have a small area (6.1% of the core area) and power (17% compared to the MatMul engine) overhead over the baseline architecture while achieving up to 3.42x speed-up on compute-intensive convolutional layers. An extensive evaluation over several state-of-the-art computer-vision benchmarks revealed up to 1.83x end-to-end inference speed-up and 1.85x energy efficiency improvement.

REFERENCES

[1] S. A. Alam, A. Anderson, B. Barabasz, and D. Gregg, “Winograd Convolution for Deep Neural Networks: Efficient Point Selection,” arXiv preprint arXiv:2201.10369, 2022.

[2] B. Barabasz, “Quantized Winograd/Toom-Cook Convolution for DNNs: Beyond Canonical Polynomials Base,” arXiv preprint arXiv:2004.11077, 2020.

[3] B. Barabasz, A. Anderson, K. M. Soodhalter, and D. Gregg, “Error analysis and improving the accuracy of Winograd convolution for deep neural networks,” ACM Transactions on Mathematical Software (TOMS), vol. 46, no. 4, pp. 1–33, 2020.

[4] B. Barabasz and D. Gregg, “Winograd Convolution for DNNs: Beyond Linear Polynomials,” in AI*IA 2019 – Advances in Artificial Intelligence, M. Alviano, G. Greco, and F. Scarcello, Eds. Cham: Springer International Publishing, 2019, pp. 307–320.

[5] Y. Bengio, N. Léonard, and A. Courville, “Estimating or propagating gradients through stochastic neurons for conditional computation,” arXiv:1308.3432, 2013.

[6] R. E. Blahut, Fast algorithms for signal processing. Cambridge University Press, 2010.

[7] R. L. Castro, D. Andrade, and B. B. Fraguela, “OpenCNN: A Winograd Minimal Filtering Algorithm Implementation in CUDA,” Mathematics, vol. 9, no. 17, p. 2033, 2021.

[8] K. Chellapilla, S. Puri, and P. Simard, “High Performance Convolutional Neural Networks for Document Processing,” in Tenth International Workshop on Frontiers in Handwriting Recognition, G. Lorette, Ed., Université de Rennes I. La Baule (France): Suvisoft, Oct. 2006, http://www.suvisoft.com. [Online]. Available: https://hal.inria.fr/inria-00112631

[9] Y.-H. Chen, T. Krishna, J. Emer, and V. Sze, “Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks,” in Proc. IEEE ISSCC, 2016, pp. 262–263.

[10] J. Choquette, W. Gandhi, O. Giroux, N. Stam, and R. Krashinsky, “Nvidia a100 tensor core gpu: Performance and innovation,” IEEE Micro, vol. 41, no. 2, pp. 29–35, 2021.

[11] J. Fernandez-Marques, P. N. Whatmough, A. Mundy, and M. Mattina, “Searching for winograd-aware quantized networks,” MLL 2021.

[12] Y. Guo, “A survey on methods and theories of quantized neural networks,” arXiv preprint arXiv:1808.04752, 2018.

[13] D. Hackenberg, R. Schöne, T. Ilsche, D. Molka, J. Schuchart, and R. Geyer, “An energy efficiency feature survey of the intel haswell processor,” in 2015 IEEE international parallel and distributed processing symposium workshop. IEEE, 2015, pp. 896–904.

[14] S. Han, J. Pool, m. j. Tran, W. J. Dally, J. Tran, W. J. Dally, m. j. Tran, and W. J. Dally, “Learning Both Weights and Connections for Efficient Neural Networks,” NIPS, 2015.

[15] K. He, X. Zhang, S. Ren, and J. Sun, “Deep Residual Learning for Image Recognition,” Proc. IEEE CVPR, pp. 770–778, 2015.

[16] G. Hinton, O. Vinyals, and J. Dean, “Distilling the Knowledge in a Neural Network,” arXiv preprint arXiv:1503.02531, 2015. [Online]. Available: http://arxiv.org/abs/1503.02531

[17] M. Horowitz, “1.1 computing’s energy problem (and what we can do about it),” in 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC). IEEE, 2014, pp. 10–14.

[18] A. G. Howard, M. Zhu, B. Chen, D. Kalenichenko, W. Wang, T. Weyand, M. Andreetto, and H. Adam, “Mobilenets: Efficient convolutional neural networks for mobile vision applications,” arXiv preprint arXiv:1704.04861, 2017.

[19] S. R. Jain, A. Gural, M. Wu, and C. H. Dick, “Trained quantization thresholds for accurate and efficient fixed-point inference of deep neural networks,” arXiv preprint arXiv:1903.08066, 2019.

[20] Jiong Gong, H. SHEN, X. D. Lin, and X. Liu, “Method and apparatus for keeping statistical inference accuracy with 8-bit winograd convolution,” 2018.

[21] N. Jouppi, “Google supercharges machine learning tasks with TPU custom chip,” 2016. [Online]. Available: https://cloudplatform.googleblog.com/2016/05/Google-supercharges-machine-learning-tasks-with-custom-chip.html
[51] T. Norrie, N. Patil, D. H. Yoon, G. Kurian, S. Li, J. Laudon, C. Young, N. Jouppi, and D. Patterson, “The design process for google’s training chips: Tpuv2 and tpuv3,” IEEE Micro, vol. 41, no. 2, pp. 56–63, 2021.

[52] NVIDIA. Nvdla primer - nvdla documentation. [Online]. Available: http://nvdla.org/primer.html

[53] J. Redmon and A. Farhadi, “YOLOv3: An Incremental Improvement,” arXiv:1804.02767, 2018. [Online]. Available: http://arxiv.org/abs/1804.02767

[54] O. Ronneberger, P. Fischer, and T. Brox, “U-net: Convolutional networks for biomedical image segmentation,” in Medical Image Computing and Computer-Assisted Intervention – MICCAI 2015, N. Navab, J. Hornegger, W. M. Wells, and A. F. Frangi, Eds. Cham: Springer International Publishing, 2015, pp. 234–241.

[55] O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, S. Ma, Z. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, “ImageNet Large Scale Visual Recognition Challenge,” IJCV, vol. 115, no. 3, pp. 211–252, 2015.

[56] L. Saglietti and L. Zdeborová, “Solvable model for inheriting the regularization through knowledge distillation,” in Mathematical and Scientific Machine Learning. PMLR, 2022, pp. 809–846.

[57] J. E. Smith, “Decoupled access/execute computer architectures,” in Proceedings of the 9th Annual Symposium on Computer Architecture, ser. ISCA ’82. Washington, DC, USA: IEEE Computer Society Press, 1982, p. 112–119.

[58] L. Steiner, M. Jung, and N. Wehn, “Exploration of ddr5 with the open-source simulator dramsys,” in MBMV 2021; 24th Workshop. VDE, 2021, pp. 1–11.

[59] O. Villa, D. Lustig, Z. Yan, E. Bolotin, Y. Fu, N. Chatterjee, N. Jiang, and D. Nellans, “Need for speed: Experiences building a trustworthy system-level gpu simulator,” in 2021 IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2021, pp. 868–880.

[60] S. Wang, J. Zhu, Q. Wang, C. He, and T. T. Ye, “Customized Instruction on RISC-V for Winograd-Based Convolution Acceleration,” in 2021 IEEE 32nd International Conference on Application-specific Systems, Architectures and Processors (ASAP). IEEE, 2021, pp. 65–68.

[61] Z. Wang and T. Nowatzki, “Stream-based memory access specialization for general purpose processors,” in 2019 ACM/IEEE 46th Annual International Symposium on Computer Architecture (ISCA), 2019, pp. 736–749.

[62] S. Winograd, Arithmetic complexity of computations. Siam, 1980, vol. 33.

[63] S. Xie, R. Girshick, P. Dollár, Z. Tu, and K. He, “Aggregated residual transformations for deep neural networks,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2017, pp. 1492–1500.

[64] A. Xygkis, D. Soudris, L. Papadopoulos, S. Yous, and D. Moloney, “Efficient winograd-based convolution kernel implementation on edge devices,” in 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC). IEEE, 2018, pp. 1–6.

[65] C. Yang, Y. Wang, X. Wang, and L. Geng, “A stride-based convolution decomposition method to stretch CNN acceleration algorithms for efficient and flexible hardware implementation,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 9, pp. 3007–3020, 2020.

[66] T. Yang, Z. He, T. Kou, Q. Li, Q. Han, H. Yu, F. Liu, Y. Liang, and L. Jiang, “BISWSRBS: A Winograd-based CNN Accelerator with a Fine-grained Regular Sparsity Pattern and Mixed Precision Quantization,” ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol. 14, no. 4, pp. 1–28, 2021.

[67] J. Yepez and S.-B. Ko, “Stride 2 1-D, 2-D, and 3-D winograd for convolutional neural networks,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 4, pp. 853–863, 2020.

[68] X. Zhang, X. Zhou, M. Lin, and J. Sun, “ShuffleNet: An Extremely Efficient Convolutional Neural Network for Mobile Devices,” in Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition, 2018, pp. 6848–6856.

[69] Y. Zhao, D. Wang, L. Wang, and P. Liu, “A faster algorithm for reducing the computational complexity of convolutional neural networks,” Algorithms, vol. 11, no. 10, p. 159, 2018.

[70] F. Zhu, R. Gong, F. Yu, X. Liu, Y. Wang, X. Li, X. Yang, and J. Yan, “Towards unified int8 training for convolutional neural network,” in Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, 2020, pp. 1969–1979.