1 Introduction

We describe a programming abstraction for heterogeneous parallel hardware, designed to capture a wide range of popular parallel hardware, including GPUs, vector instruction sets and multicore CPUs. Our abstraction, which we call HPVM, is a hierarchical dataflow graph with shared memory and vector instructions. We use HPVM to define both a virtual instruction set (ISA) and also a compiler intermediate representation (IR). The virtual ISA aims to achieve both functional portability and performance portability across heterogeneous systems, while the compiler IR aims to enable effective code generation and optimization for such systems.

HPVM effectively supports all forms of parallelism used to achieve computational speedups (as opposed to concurrency), including task parallelism, coarse-grain data parallelism, fine-grain data parallelism, and pipelined parallelism. HPVM also enables flexible scheduling and tiling: different nodes in the dataflow graph can be mapped flexibly to different combinations of compute units, and the graph hierarchy expresses memory tiling, essential for achieving high performance on GPU and CPU targets.
2 Design

In this section, we describe the design of the HPVM parallel abstractions, and how they are defined as an extension to the LLVM Internal Representation (IR). We also discuss briefly some features of the design that are primarily for performance rather than correctness (or “functionality”).

Section 6.1 contains a sample code written in HPVM. Throughout this section, we will refer to Section 6.1 and use the example to illustrate certain parts of the HPVM design.

2.1 Dataflow Graph

In HPVM, a program is represented as a hierarchical dataflow graph (DFG) with side effects, where nodes represent units of execution, and edges between nodes describe the explicit data transfer requirements. Each dataflow node in a DFG can either be a leaf node or an internal node. An internal node contains a complete dataflow graph (child graph), and the child graph itself can have internal nodes and leaf nodes. A leaf node contains a mixture of scalar and vector code, expressing actual computations. Figure 5 shows the dataflow graph of an application, sgemm, based on HPVM abstractions. Dataflow nodes SgemmLeaf and Allocation are leaf nodes, while SgemmInternal and SgemmRoot are internal nodes containing other dataflow graphs.

Dataflow edges can be ordinary edges, denoting a one-time data transfer, or streaming edges denoting that data items will be repeatedly transferred through this edge, and thus will need to be processed by repeated executions of the sink dataflow node. Figure 5 shows two (ordinary) dataflow edges from Allocation node to SgemmLeaf node, representing transferring of two data items.

To express data parallelism, which is inherently the replication of computation over data, we allow a single static dataflow node to represent multiple dynamic instances of the node. The dynamic instances of a node are required to be independent of each other, i.e., can be executed in parallel. For example, in sgemm (subsection 6.1), SgemmLeaf node has multiple dynamic instances, each computing different output elements of the multiplication result. Note that figure 5 shows the static dataflow graph, thus the replication of SgemmLeaf is not depicted.

Consequently, dataflow edges are also replicated. We provide two replication mechanisms:

- “all-to-all”: all dynamic instances of the source node are connected with all dynamic instances of the sink node, thus expressing a synchronization barrier between the two groups of nodes
- “one-to-one”: each dynamic instance of the source dataflow node is connected with a single corresponding instance of the sink node. One-to-one replication requires that the grid structure (number of dimensions and the extents in each dimension) of the source and sink nodes be identical.
In the context of HPVM extension to LLVM, intrinsic functions are used to implement the HPVM internal representation. These functions are designed to construct, query, and manage dataflow graphs. Here are some key intrinsic functions:

### Intrinsic Functions for Constructing Graphs

- **Create Node**: `llvm.hpvm.createNode1D(Function* F, i32 n)` creates a node with `n` dynamic instances executing node function `F` (similarly `llvm.hpvm.createNode2D/3D`).
- **Create Edge**: `llvm.hpvm.createEdge(i8* Src, i8* Dst, i32 sp, i32 dp, i1 ReplType, i1 Stream)` creates an edge from output `sp` of node `Src` to input `dp` of node `Dst`.
- **Bind Input**: `llvm.hpvm.bind.input(i8* N, i32 ip, i32 ic, i1 Stream)` binds input `ip` of current node to input `ic` of child node `N` (similarly, `llvm.hpvm.bind.output`).

### Intrinsic Functions for Querying Graphs

- **Get Node**: `llvm.hpvm.getNode()` returns a handle to the current dataflow node.
- **Get Parent Node**: `llvm.hpvm.getParentNode(i8* N)` returns a handle to the parent of node `N`.
- **Get Node Instance ID**: `llvm.hpvm.getNodeInstanceID.[xyz](i8* N)` gets the index of the current dynamic node instance of node `N` in dimension `x`, `y`, or `z`.
- **Get Number of Node Instances**: `llvm.hpvm.getNumNodeInstances.[xyz](i8* N)` gets the number of dynamic instances of node `N` in dimension `x`, `y`, or `z`.
- **Get Vector Length**: `llvm.hpvm.getVectorLength(i32 typeSz)` gets the vector length in the target compute unit for type size `typeSz`.

### Intrinsic Functions for Memory Allocation and Synchronization

- **Allocate Memory**: `llvm.hpvm.malloc(i32 nBytes)` allocates a block of memory of size `nBytes` and returns a pointer to it.
- **Atomic Operations**: `llvm.hpvm.atomic.add(i32*, i32)`, `llvm.hpvm.xchg(i32, i32)` perform atomic-fetch-and-add and atomic-swap, etc., on shared memory locations.
- **Barrier**: `llvm.hpvm.barrier()` provides a local synchronization barrier across dynamic instances of the current leaf node.

### Intrinsic Functions for Integration with Host Code

- **Launch Graph**: `llvm.hpvm.launch(Function* F, i8* args, i1 Stream)` launches a graph associated with function `F` asynchronously.
- **Wait for Graph Completion**: `llvm.hpvm.wait(i8* graphID)` waits for completion of graph `graphID`.
- **Push Arguments**: `llvm.hpvm.push(i8* graphID, i8* args)` pushes arguments as a streaming input of graph `graphID`.
- **Pop Arguments**: `llvm.hpvm.pop(i8* graphID)` reads the next streaming output of graph `graphID`.

In summary, the HPVM extension to LLVM leverages intrinsic functions to encapsulate graph construction, querying, memory allocation, and synchronization. These functions enable a seamless integration with the LLVM infrastructure, facilitating the efficient execution of dataflow graphs.

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### Table 1: Intrinsic functions used to implement the HPVM internal representation. `iN` is the `N`-bit integer type in LLVM.

| Intrinsic | Description |
|-----------|-------------|
| `llvm.hpvm.createNode1D` | Create node with `n` dynamic instances executing node function `F` (similarly `llvm.hpvm.createNode2D/3D`). |
| `llvm.hpvm.createEdge` | Create edge from output `sp` of node `Src` to input `dp` of node `Dst`. |
| `llvm.hpvm.bind.input` | Bind input `ip` of current node to input `ic` of child node `N`; similarly, `llvm.hpvm.bind.output`. |
| `llvm.hpvm.getNode()` | Return a handle to the current dataflow node. |
| `llvm.hpvm.getParentNode(i8* N)` | Return a handle to the parent of node `N`. |
| `llvm.hpvm.getNodeInstanceID.[xyz](i8* N)` | Get index of current dynamic node instance of node `N` in dimension `x`, `y`, or `z`. |
| `llvm.hpvm.getNumNodeInstances.[xyz](i8* N)` | Get number of dynamic instances of node `N` in dimension `x`, `y`, or `z`. |
| `llvm.hpvm.getVectorLength(i32 typeSz)` | Get vector length in target compute unit for type size `typeSz`. |
| `llvm.hpvm.malloc(i32 nBytes)` | Allocate a block of memory of size `nBytes` and return a pointer to it. |
| `llvm.hpvm.atomic.add(i32*, i32)` | Perform atomic-fetch-and-add on shared memory locations. |
| `llvm.hpvm.barrier()` | Provide a local synchronization barrier across dynamic instances of the current leaf node. |
| `llvm.hpvm.launch(Function* F, i8* args, i1 Stream)` | Launch a graph associated with function `F` asynchronously. |
| `llvm.hpvm.wait(i8* graphID)` | Wait for completion of graph `graphID`. |
| `llvm.hpvm.push(i8* graphID, i8* args)` | Push arguments as a streaming input of graph `graphID`. |
| `llvm.hpvm.pop(i8* graphID)` | Read the next streaming output of graph `graphID`. |

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2.2 HPVM Extension to LLVM

HPVM is implemented on top of LLVM using LLVM intrinsic functions (this choice is explained further at the end of this section). For a brief summary, refer to Table 1. We use HPVM intrinsics to describe and query the structure of the dataflow graph - *Graph Intrinsics* and *Query Intrinsics* respectively, with additional intrinsics for memory allocation and synchronization.

Each dataflow node is associated with a function, specified as function pointer, describing the functionality of the corresponding node. The incoming dataflow edges correspond to the incoming arguments to the node function. The outgoing dataflow edges are represented by the return type of the node function, which must be an LLVM struct type with one field per outgoing edge.

Functions associated with internal nodes may only contain HPVM graph intrinsics. Listing contains the internal node function `SgemmInternal` (lines 46-65), associated with dataflow node `SgemmInternal`. This function only includes HPVM graph intrinsics, e.g.
to create the leaf nodes `Allocation` (line 50) and `SgemmLeaf` (line 51) and the dataflow edges between them.

Functions associated with leaf nodes contain llvm IR with vector instructions and may also contain HPVM query, allocation and synchronization intrinsics. Listing 1 contains the leaf node functions `Allocation` (lines 14-23) and `SgemmLeaf` (lines 26-43), associated with dataflow nodes `Allocation` and `SgemmLeaf`. Note the use of HPVM query and allocation intrinsics, in lines 19, 31-37. Also, that the return type of function `Allocation` (defined in line 7) has two elements, just as the number of outgoing dataflow edges, while function `SgemmLeaf`, with no outgoing edges, has an empty struct (defined in line 9) as a return type.

Finally, we define intrinsics aimed to integrate the dataflow graph in the host code (which will be performing the computation that is not to be mapped to accelerators, e.g. initialization, output). In Listing 1, the host code initiates the execution of a dataflow graph associated with the function `SgemmRoot` and waits for its completion (lines 102 and 103 respectively).

The following listing includes a description of the HPVM intrinsics, divided according to their functionality. LLVM type `i8*` is used as an opaque handle to represent dataflow nodes and edges in the instruction set.

1. **HPVM Graph Intrinsics:** describing the structure of the dataflow graph:

   - `i8* llvm.hpvm.createNode(Function * F)`: Creates a dataflow node associated with the function `F`
   - `i8* llvm.hpvm.createNode{1-3}D(Function * F, int n1, ...)`: Creates `n1` dataflow nodes, all associated with the function `F`. There are three versions of this intrinsic depending on the number of dimensions of the grid of nodes.
   - `void llvm.hpvm.createEdge(i8* Src, i8* Dst, i1 ReplTy, i32 sp, i32 dp, i1 Stream)`: Creates a dataflow edge from output `sp` of node `Src` to input `dp` of node `Dst`. `Stream` argument specifies whether the defined dataflow edge is an ordinary or a streaming edge. `ReplTy` specifies the replication type, "one-to-one" or "all-to-all".
   - `void llvm.hpvm.bind.input(i8* N, i32 ip, i32 ic, i1 Stream)`: Bind input `ip` of node `N`’s parent node to input `ic` of child node `N`.
   - `void llvm.hpvm.bind.output(i8* N, i32 oc, i32 op, i1 Stream)`: Bind output `oc` of node `N` to output `op` of its parent node.

2. **HPVM Query Intrinsics:** querying the structure of the dataflow graph:

   - `i8* llvm.hpvm.getNode()`: Get a pointer to the current dataflow node
   - `i8* llvm.hpvm.getParentNode(i8* N)`: Get a pointer to the parent node, in the dataflow graph hierarchy, of node `N`
   - `i32 llvm.hpvm.getNumDims(i8* N)`: Get the number of dimensions of the grid of node `N`
   - `i32 llvm.hpvm.getNodeInstanceID.[xyz](i8* N)`: Get a unique identifier of a node instance of node `N` in the specified dimension
- i32 llvm.hpvm.getNumNodeInstances.[xyz](i8*, i32): Get the number of dynamic instances of node N in the specified dimension
- i32 llvm.hpvm.getVectorLength(i32 typeSize): Get vector length in target compute unit for type size typeSize

3. HPVM Memory Allocation Intrinsics:
- i8* llvm.hpvm.malloc(i32 nBytes): Allocates an object of size nBytes in global memory, shared by all nodes, although the pointer returned must somehow be communicated explicitly (just as with heap allocation in a multi-threaded C program).

4. HPVM Synchronization Intrinsics:
- void llvm.hpvm.barrier(): Only synchronizes the dynamic instances of the node that executes it, and not all other concurrent nodes.
- Atomic operations, e.g. i32 llvm.hpvm.atomic.add(i32*, i32).

5. HPVM Integration with Host Intrinsics:
- i8* llvm.hpvm.launch(Function* F, i8* args, i1 Stream): Launch dataflow graph associated with Function F asynchronously, and return a handle to identify the graph. Argument Stream indicates whether the dataflow graph contains streaming dataflow edges.
- void llvm.hpvm.wait(i8* graphID): Wait for completion of graph graphID.
- void llvm.hpvm.push(i8* graphID, i8* args): Push args as streaming input of graph graphID. args is a packed struct containing all arguments expected by the executing graph.
- i8* llvm.hpvm.pop(i8* graphID): Read streaming output of graph graphID.

- HPVM is implemented on top of LLVM [1] using LLVM intrinsic functions. This approach has many advantages. It is not-intrusive, allowing smooth integration existing analysis optimization passes, while at the same time enabling our custom passes to recognize them and handle each according to their specified semantics. The memory behaviour of the intrinsic functions can be specified, thus providing existing passes with the information required to include them in their analysis or transformation.

Additionally, using intrinsics we easily isolate the parallel code from the code executing sequentially (LLVM IR); we use the intrinsic llvm.hpvm.createNode**(Function* F, ... ) and the parallel code is included in F. This has the additional benefits of easily identifying the communication between the sequentially and parallelly executing parts. Only what is passed as arguments to the dataflow graph is accessible by it. This simplifies code generation in that generating code for the node function F alone is sufficient.
2.3 Performance features

When global memory must be shared across nodes mapped to devices with separate address spaces, the translator inserts calls to the appropriate accelerator runtime API (e.g., the OpenCL run-time) to perform the copies. Such copies are sometimes redundant, e.g., if the data has already been copied to the device by a previous node execution. It is important to avoid unnecessary memory copies between devices for good performance. We achieve this in two ways.

First, we differentiate between pointers to input/output data arrays using attributes in, out, and inout to node arguments. For example, annotating a pointer argument of a node as out allows us to avoid copying its initial data to the compute unit for which that node is compiled. In Listing 1 matrices A and B are annotated as in arguments, and thus are only inputs to the dataflow node SgemmLeaf, but C is both input and output (line 26).

Second, we implement a conceptually simple “memory tracker” to record the locations of the latest copy of data arrays, and uses this to avoid unnecessary copies. Calls to the memory tracker due to dataflow edge semantics are automatically inserted to the generated code. Host code, however, is required to explicitly use the memory tracker interface, since it does not access data using dataflow edges. The memory tracker runtime calls are:

- `llvm_hpvm_track_mem(i8* ptr, i64 memsize)`: Add the memory region starting from pointer `ptr` of size `memsize` in the tracked memory table.

- `llvm_hpvm_request_mem(i8* ptr, i64 size)`: Request to access the memory region associated with pointer `ptr`. This automatically results in a data copy if data is not already present in the host memory.

- `llvm_hpvm_untrack_mem(i8* ptr)`: Remove the memory region associated with pointer `ptr` in the tracked memory table.

In Listing 1 the host code contains calls to the HPVM runtime denoting that the locations of matrices A, B and C should be tracked (or no longer tracked), in lines 89-91 (109-111 respectively). Also, the host explicitly asks for the matrix C to be available in host memory (line 106).

3 Compilation Strategy

3.1 Frontend

The front end parses the source files and generates the textual representation of HPVM, a hierarchical dataflow graph (DFG) represented through HPVM intrinsics in LLVM IR along with code that may include HPVM intrinsics for the leaf nodes. Currently, we use C with dummy function calls with one-to-one correspondence to HPVM intrinsics to generate HPVM.
3.2 Analysis

First, the Graph Builder Pass constructs an internal representation for the DFG by parsing the HPVM intrinsics. Then, other passes may operate on and optimize the LLVM IR in the leaf nodes. Also, we have built analysis passes that determine features of interest in the DFG, e.g. read only memory (constantMemPass) or memory that is private and visible only to a set of dataflow nodes (localMemPass). This information is used for efficient code generation.

3.3 Backend Code Generation

In general, code generation proceeds in a bottom up approach, maintaining the invariant that when a node is encountered as a child node, code generation for it has already been performed and a native function that performs the node’s computation, \texttt{genFunc}, has been generated. \texttt{genFunc} is exposed to the higher graph levels as an interface to invoke the node’s execution.

The code generation pass uses the static dataflow graph to:

- Identify nodes which can be mapped to one or more available compute units efficiently. Currently, we use user-provided hints as to which target device to compile for, and thus which backend to invoke, e.g. in Listing 1 \texttt{SgemmLeaf} node is annotated as a GPU node using metadata (lines 119, 122).

- For the identified node, invoke appropriate backend to generate kernel code for the chosen target, and calls to HPVM runtime. The HPVM runtime invokes the appropriate accelerator runtime API to launch the generated kernel. All these calls are encapsulated in \texttt{genFunc}.

At the end of code generation, we have host code with HPVM runtime calls and target specific kernels.

Currently, we have implemented backend translators for three targets: nVidia GPUs, Intel Vector Hardware, and x86 processors. We leverage existing infrastructure for some of the translation process, the LLVM x86 and NVPTX backends and the proprietary Intel OpenCL compiler.

Listings 2 and 4 show fragments of the kernel and host code generated by the GPU backend respectively. For kernel code generation, in Listing 2 note that the HPVM intrinsics (previously in lines 31-37 of Listing 1) have been replaced by function calls to OpenCL library functions (please refer to associated code and comment in Listing 2, lines 13-20).

For host code generation, in Listing 4 note the function \texttt{SgemmRoot2}, defined in lines 76-143. This is the function generated by the GPU backend that encapsulates the generated calls to OpenCL runtime that are required to setup and call the generated kernel.

3.4 Code Generation for Memory Tiling

If the programmer wished to “tile” the computation, she would use an additional level in the dataflow graph hierarchy. The (1D, 2D or 3D) instances of a leaf node would become a single
(1D, 2D or 3D) tile of the computation. The (1D, 2D or 3D) instances of the parent node of the leaf node would become the (1D, 2D or 3D) blocks of tiles. Thus, a single mechanism, the hierarchical dataflow graph, represents both tiling for scratchpad memory on the GPU and tiling for cache on the CPU. On a GPU, the leaf node becomes a thread block and we create as many thread blocks as the dimensions of the parent node. On a CPU or AVX target, the code results in a loop nest with as many blocks as the dimensions of the parent node, of tiles as large as the dimensions of the leaf node.

Any memory allocated for each tile (using \texttt{llvm.hpvm.malloc} intrinsic in a leaf node) would be assigned to scratchpad memory on a GPU or left in global memory and get transparently cached due to temporal reuse on the CPU. We refer to a node performing such allocations as allocation node due to its functionality.

We have used this mechanism to create tiled versions of four of the seven Parboil benchmarks evaluated in Section 5. The tile sizes are determined by the programmer in our experiments. The expectation is that they will usually be determined by upstream optimization passes or autotuning tools. For the three benchmarks (\texttt{sgemm}, \texttt{tpacf}, \texttt{bfs}) for which non-tiled versions were available, the tiled versions achieved a mean speedup of 19x on GPU and 10x on AVX, with \texttt{sgemm} getting as high as 31x speedup on AVX.

Figure 5 shows an allocation node, Allocation. Listing 1 includes the node function (defined in lines 14-23), that uses the \texttt{llvm.hpvm.malloc} intrinsic to allocate memory and then passes it to \texttt{SgemmLeaf}. This memory, the argument \texttt{\%shB}, is now accessible only by the dynamic instances of \texttt{SgemmLeaf} that are created by the same dynamic instance of \texttt{SgemmInternal}. Listing 2 shows that \texttt{\%shB} has been mapped to the scratchpad by the backend code generator, as shown by the address space qualifier 3 (line 8).

### 3.5 Handling Pipelining

If a dataflow graph is identified as ”streaming”, then the dataflow nodes need to be persistent: instead of performing a one-time computation and complete their execution, they need to be available to process any new data items transferred through the streaming edges until the data stream ends.

For each pipeline stage, we create a separate thread to perform its computation, again represented by the native function \texttt{genFunc} that was generated for the associated node during code generation. The thread handles the required synchronization between its stage and the other pipeline stages-threads, as well as the data transfers represented by dataflow edges. Streaming edges are implemented using buffering.

### 4 Compiler Optimization

An important capability of a compiler IR is to support effective compiler optimizations. The hierarchical dataflow graph abstraction enables optimizations of explicitly parallel programs at a higher (more informative) level of abstraction than a traditional IR, like LLVM and many others, that lacks explicitly parallel abstractions. We describe some of the primitive graph transformations enabled by the representation, and two potentially important optimizations based on them – fusion of compute kernels and mapping data to constant memory in GPUs.
Our long term goal is to develop a full-fledged parallel compiler infrastructure that leverages the parallel abstractions in \textit{HPVM}.

4.1 Primitive Graph Operations

We use the graph abstractions in \textit{HPVM} to implement a number of primitive parallel program transformations as graph operations. We define an \textit{AllocCompute} graph as a simple two-node graph with one allocation node and one compute node. This structure is needed when the dynamic instances of the compute node must share a single memory object, e.g., by reading and writing to parts of it.

1. \textit{MergeIndependentNodes}(N1, N2): Merge two parallel leaf nodes \( N1 \) and \( N2 \) with no path of edges connecting them into a single leaf node \( N \). Make the incoming edges of both \( N1 \) and \( N2 \) the incoming edges of \( N \) (analogous, the outgoing edges). \( N1 \) and \( N2 \) must have the same parent node, dimensions, and size in each dimension.

2. \textit{MergeDependentNodes}(N1, N2): Like \textit{MergeIndependentNodes}, except that \( N1 \) and \( N2 \) are connected by one or more dataflow edges, which must all be 1-1 edges. These edges are omitted from \( N \), and simply replaced with variable assignments (copies).

3. \textit{MergeAllocComputeGraphs}(N1, N2): Merge two internal nodes \( N1 \) and \( N2 \), each of which contains an AllocCompute graph, defined above, into a new internal node \( N \) containing a merged AllocCompute graph. The allocation nodes of \( N1 \) and \( N2 \) are merged into a new allocation node in \( N \) and likewise for the compute nodes. There must be no path of edges from the compute node of \( N2 \) to the allocation node of \( N1 \) - that would prevent the merge of the allocation nodes.

4. \textit{InlineAuxFunction}(F\_node, F\_aux): Inline an auxiliary function \( F\_aux \) called from a node function \( F\_node \). This allows merging of \( N1 \) and \( N2 \) into a simple, new node function that calls the two original node functions, without introducing additional overhead for the function calls and without blocking optimizations across the function call boundaries.

In addition, note that the basic intrinsics, \texttt{createNode*}, \texttt{createEdge*}, \texttt{bind.input}, \texttt{bind.output}, \texttt{getNodeInstanceID.*}, etc., are directly useful for many graph analyses and transformations.

4.2 Node Fusion Using the Primitives

One key optimization we have implemented using these primitives is \textit{Node Fusion}, which can lead to more effective redundancy elimination across kernels, reduced launch overhead when kernels are executed on GPUs, improved temporal locality when kernels that reuse data are fused, and sometimes reduced barrier synchronization overhead as well. Merging nodes willy-nilly, however, can hurt performance greatly on some devices because of resource constraints or functional limitations. For example, each thread-block in a GPU has limited memory and scratchpad capacity and merging two nodes into one could force the use of fewer thread blocks, reducing parallelism. We use a simple policy to decide when to merge two nodes; for our experiments, we augment this with manual annotations to specify which
nodes should be merged. We leave it to future work to develop a more sophisticated merging policy, perhaps guided by profile information or autotuning.

The algorithm we use attempts to merge two nodes if they have the same parent node, same target, and are both annotated for merging. If so, the algorithm simply invokes the appropriate merge operation in the previous section (which check additional conditions the nodes must satisfy).

### 4.3 Mapping Data to GPU Constant Memory

GPU global memory is highly optimized (in nVidia GPUs) for coalescing of consecutive accesses by threads in a thread block: irregular accesses can have orders-of-magnitude lower performance. In contrast, constant memory is optimized for read-only data that is invariant across threads and is much more efficient for thread-independent data.

The HPVM translator for GPUs automatically identifies data that should be mapped to constant memory. The analysis is trivial for scalars, but also simple for array accesses because of the HPVM intrinsics: for array index calculations, we identify whether they depend on (1) the `getNodeInstanceId.*` intrinsics, which is the sole mechanism to express thread-dependent accesses, or (2) memory accesses. Those without such dependencies are uniform and are mapped to constant memory, and the rest to GPU global memory. HPVM translator identified such candidates in 3 (spmv, tpacf, cutcp) out of 7 benchmarks, resulting in 34% performance improvement in tpacf and no effect on performance of the other two benchmarks.

### 5 Evaluation

We evaluate the HPVM virtual ISA and compiler IR by examining several questions: (1) Is HPVM performance-portable: can we use the same virtual object code to get “good” speedups on different compute units? (2) Can HPVM achieve performance competitive with hand-written OpenCL programs on our target architectures? (3) Does HPVM effectively capture pipelined parallelism for streaming computations, which cannot be easily expressed in existing alternatives like PTX, HSAIL and SPIR?

#### 5.1 Experimental Setup and Benchmarks

Starting from C with a set of functions corresponding to the HPVM intrinsics we write parallel applications equivalent to a set of OpenCL applications, as described in section [3]. We translated the same HPVM code to two different target units: the AVX instruction set in an Intel Xeon E5 core i7 and a discrete nVidia GeForce GTX 680 GPU card with 2GB of memory. The Intel Xeon also served as the host processor, running at 3.6 GHz, with 16 GB RAM.

We used seven applications from the Parboil benchmark suite [3]: Sparse Matrix Vector Multiplication (spmv), Single-precision Matrix Multiplication (sgemm), Stencil PDE solver (stencil), Lattice-Boltzmann (lbm), Breadth-first search (bfs), Two Point Angular
Correlation Function (tpacf), and Distance-cutoff Coulombic Potential (cutcp). For the last question, we used a pipelined streaming application, described later below.

In the GPU experiments, our baseline for comparison is the best available OpenCL implementation. For spmv, sgemm, lbm, bfs and cutcp, that is the Parboil version labeled `opencl_nvidia`, which has been hand-tuned for the Tesla NVidia GPUs [2]. For stencil and tpacl, the best is the generic Parboil version labeled `opencl_base`. We further optimized the codes by removing unnecessary data copies (bfs) and global barriers (tpac, cutcp). nVidia’s proprietary OpenCL compiler is used to compile all applications.

In the vector experiments, with the exception of bfs, our baseline is the same OpenCL implementations we chose as GPU baselines, but compiled using the Intel OpenCL compiler, because these achieved the best vector performance as well. For bfs, we used `opencl_base` instead, as `opencl_nvidia` failed the correctness test. The HPVM versions were generated to match the algorithms used in the OpenCL versions, and that was used for both vector and GPU experiments.

We use the largest available input for each benchmark, and each data point we report is an average of ten runs. or generate a larger input when the runtime would be too small. Each data point we report is an average of ten runs. We repeated the experiments multiple times to verify their stability.

Figures 1 and 2 show the execution time of these applications on GPU and vector hardware respectively, normalized to the baselines mentioned above. Each bar shows segments for the time spent in the compute kernel (kernel), copying data (copy) and remaining time on the host. The total execution time for the baseline is shown above the bar to indicate the actual running times.

Comparing with the GPU baseline, HPVM achieves near hand-tuned OpenCL performance for all benchmark except bfs, where HPVM takes 20% longer. The overhead is because our translator is not mature enough to generate global barriers, and thus HPVM issues more kernels than the `opencl_nvidia` version, incurring significant overhead.

In the vector case, HPVM is within 7% of the hand-tuned baseline in the worst case. We see 20% speedup for sgemm, resulting exclusively from the kernel execution time, because LLVM applies more effective optimizations on the kernel than the nVidia OpenCL compiler.
5.2 Evaluation of Pipelined Parallelism

We used a six-stage image processing pipeline, Edge Detection in grey scale images, to evaluate the benefits of pipelined parallelism in HPVM. The application accepts a stream of grey scale images, $I$, and a fixed mask $B$ and computes a stream of binary images, $E$, that represent the edges of $I$. We feed 1280x1280 pixel frames from a video as the input and measure the frame rate at the output. This pipeline is natural to express in HPVM. The streaming edges and pipeline stages simply map to key features of HPVM. In contrast, expressing pipelined streaming parallelism in OpenCL, PTX, SPIR or HSAIL, although possible, is extremely awkward. In particular, while the parallel stages can be expressed using different command queues, the (buffered) data transfers and synchronization between stages are tedious, error-prone and difficult to scale to larger and more complex pipelines.

Expressing this example in HPVM allows for flexibly mapping computationally heavy stages of the pipeline to accelerators. We can map each stage to one of three targets (GPU, vector or a CPU thread), for a total of $3^6 = 729$ different configurations, all generated from a single HPVM code. Figure 3 shows the frame rate of 7 such configurations. It shows that HPVM (a) can capture pipelined, streaming computations effectively and achieve considerable speedups, and (b) is flexible enough to allow a wide range of configurations with different performance characteristics from a single code. The graph illustrates the dramatic differences in performance between different mappings. This flexibility of HPVM enables a (future) run-time scheduler to choose configurations based on properties of the code, available hardware resources, and energy constraints.

Note that, although our model allows us to exploit the pipeline parallelism between different stages, we do not use the stream interface in our prototype implementation. Thus the execution of different stages is not actually overlapped when executing on a single device. We do get the benefit of pipeline parallelism when we dispatch the execution of different stages to multiple devices.

5.3 Node Fusion Optimization Evaluation

We evaluated the benefits of Node Fusion using two widely used image processing kernels, Laplacian Estimate ($L$) and Gradient Computation ($G$). Most benchmarks we examined
have been hand-tuned to apply such transformations manually, making it hard to find Node Fusion opportunities (although they may often be more natural to write without manual merging). The two kernels’ dataflow graphs have similar structure, shown for $L$ in Figure 4. We compiled the codes to run entirely on GPU and fed the same video frames as before. We experimented with different choices of node sets to merge. Fusing all three nodes reduces the GPU invocations by two thirds, but showed a slowdown for both $L$ and $G$. Fusing just the two independent nodes reduced the number of GPU invocations by one third and gave a speedup of 7.4% and 10.4% on $L$ and $G$ respectively. These experiments show that significant benefits can occur when Node Fusion is applied to a carefully selected set of dataflow nodes.

6 Example

In this section, we show an example in HPVM and the translation process for an nVidia GPU target. We use the sgemm benchmark from the Parboil test suite.

6.1 SGEMM in HPVM

In HPVM, this benchmark is represented as a two level hierarchy with two leaf nodes performing memory allocation and computation, Allocation and SgemmLeaf respectively, an internal node SgemmInternal, plus a top level node, SgemmRoot, that interacts with the host code. The additional level of hierarchy exists because the top level node is required to have a single dynamic instance and is used to create the underlying graph structure. This is shown in figure 5. Listing 1 shows parts of the HPVM code that represents this dataflow graph, with inlined comments to point out the performed operations.

```plaintext
1 ; ModuleID = 'build/hpvm_sh_default/main.hpvm.ll'
2
3 ; %struct.RootIn is the struct type used to pack the arguments required by the dataflow graph
4 %struct.RootIn = type <{ float *, i64, i32, float *, i64, i32, float *, i64, i32, i32, float, float, i32, i32, i32, i32 }>
5 ; Examples of dataflow node return types:
6 ; - Allocation Node returns a pointer and an i64
7 %struct.out.Allocation = type <{ i8*, i64 }>  
8 ; - SgemmLeaf Node does not return anything
9 %emptyStruct = type <{}>
```

Figure 4: Dataflow graph of Laplacian Estimate.
Figure 5: Dataflow graph of sgemm.

11 ; ...
12
13 ; Allocation Node function, performing one of size block_x x block_y
14 define %struct.out.Allocation @Allocation(i32 %block_x, i32 %block_y) #2 {
15 entry:
16 %mul = mul nsw i32 %block_y, %block_x
17 %conv = sext i32 %mul to i64
18 %mul1 = shl nsw i64 %conv, 2
19 %call1 = call i8* @llvm.hpvm.malloc(i64 %mul1)
20 %returnStruct = insertvalue %struct.out.Allocation undef, i8* %call1, 0
21 %returnStruct2 = insertvalue %struct.out.Allocation %returnStruct, i64 %mul1, 1
22 ret %struct.out.Allocation %returnStruct2
23 }
24
25 ; Computation Leaf Node function, using HPVM query intrinsics
26 define %emptyStruct @SgemmLeaf ( float * in %A, i64 %bytesA, i32 %lda, float * in %B, i64 %bytesB, i32 %ldb, float * in out %C, i64 %bytesC, i32 %ldc, i32 %k, float %alpha, float %beta, float * nocapture %shB, i64 %bytesshB) #2 {
27 entry:
28 %c = alloca [16 x float], align 16
29 %0 = bitcast [16 x float]* %c to i8*
30 %call17 = call i8* @llvm.hpvm.getNode()
31 %call18 = call i8* @llvm.hpvm.getParentNode(i8* %call17)
32 %call129 = call i32 @llvm.hpvm.getNodeInstanceID.x(i8* %call17)
33 %call130 = call i32 @llvm.hpvm.getNodeInstanceID.y(i8* %call17)
34 %call1141 = call i32 @llvm.hpvm.getNumNodeInstances.x(i8* %call17)
35 %call11512 = call i32 @llvm.hpvm.getNumNodeInstances.y(i8* %call1141)
36 %call11613 = call i32 @llvm.hpvm.getNumNodeInstances.x(i8* %call11512)
37 %call117 = call i8* @llvm.hpvm.getAllocation()
38 %call118 = call i8* @llvm.hpvm.getParentNode(i8* %call17)
39 %call129 = call i32 @llvm.hpvm.getNodeInstanceID.x(i8* %call17)
40 %call130 = call i32 @llvm.hpvm.getNodeInstanceID.y(i8* %call129)
41 ; ... Remaining Computation
42 ret %emptyStruct undef
43 }
44
45 ; Internal Node function, using HPVM graph intrinsics
46 define %emptyStruct.19 @SgemmInternal ( float* in %A, i64 %bytesA, i32 %lda, float* in %B, i64 %bytesB, i32 %ldb, float* in out %C, i64 %bytesC, i32 %ldc, i32 %k, float %alpha, float %beta, i32 %block_x, i32 %block_y) #2 {
entry:

; Create two child nodes, Allocation and SgemmLeaf
%Allocation.node = call i8* @llvm.hpvm.createNode(18* bitcast (%struct.out.Allocation (132, i32)* @Allocation to i8*))
%SgemmLeaf.node = call i8* @llvm.hpvm.createNode2D(18* bitcast (%emptyStruct (float*, i64, i32, float*, i64, i32, float, float, float*, i64)* @SgemmLeaf to i8*), 132 %block_x, 132 %block_y)

; Create the dataflow edges between nodes Allocation and SgemmLeaf
%output = call i8* @llvm.hpvm.createEdge(i8* %Allocation.node, i8* %SgemmLeaf.node, i1 true, i32 0, i32 12, i1 false)
%output1 = call i8* @llvm.hpvm.createEdge(i8* %Allocation.node, i8* %SgemmLeaf.node, i1 true, i32 1, i32 13, i1 false)

; Bindings to transfer its inputs to child nodes Allocation and SgemmLeaf
call void @llvm.hpvm.bind.input(i8* %SgemmLeaf.node, i32 0, i32 0, i1 false)
call void @llvm.hpvm.bind.input(i8* %SgemmLeaf.node, i32 1, i32 1, i1 false)
... call void @llvm.hpvm.bind.input(i8* %Allocation.node, i32 12, i32 0, i1 false)
call void @llvm.hpvm.bind.input(i8* %Allocation.node, i32 13, i32 1, i1 false)
ret %emptyStruct.19 undef

; Root Node function, using HPVM graph intrinsics
define %emptyStruct.20 @SgemmRoot (float * in %A, i64 %bytesA, i32 %lda, float * in %B, i64 %bytesB, i32 %ldb, float * in out %C, i64 %bytesC, i32 %ldc, i32 %k, float %alpha, float %beta, i32 %block_x, i32 %block_y, i32 %grid_x, i32 %grid_y) #2 {
entry:
; Creates internal node SgemmInternal
%SgemmInternal.node = call i8* @llvm.hpvm.createNode2D(%emptyStruct.19(float*, i64, i32, float*, i64, i32, float*, i64, i32, i32, float, float, i32, i32, i32, i32)* @SgemmInternal to i8*), 132 %grid_x, 132 %grid_y)

; Bindings to transfer its inputs to child node SgemmInternal
call void @llvm.hpvm.bind.input(i8* %SgemmInternal.node, i32 0, i32 0, i1 false)
call void @llvm.hpvm.bind.input(i8* %SgemmInternal.node, i32 1, i32 1, i1 false)
... call void @llvm.hpvm.bind.input(i8* %Allocation.node, i32 12, i32 0, i1 false)
call void @llvm.hpvm.bind.input(i8* %Allocation.node, i32 13, i32 1, i1 false)
ret %emptyStruct.20 undef
}

; Function launching the dataflow graph defined by SgemmRoot and performing calls to HPVM runtime
define i32 @main(i32 %argc, i8 ** %argv) #2 {
entry:
... Placeholder for HPVM runtime to perform required initializations
call void @llvm.hpvm.init()
; Host calls to HPVM runtime, noting that the locations of arrays A, B, and C should be tracked
call void @llvm.hpvm.track_mem(i8* %24, i64 %mul219) #1
call void @llvm.hpvm.track_mem(i8* %26, i64 %mul222) #1
call void @llvm.hpvm.track_mem(i8* %28, i64 %mul2125) #1
... Argument Packing
%call23 = tail call noalias i8* @malloc(i64 88) #1
%A1.i = bitcast i8* %call23 to float**
store float* %A, float** %A1.i, align 1, !tbaa !3
%bytesA2.i = getelementptr inbounds i8* %call23, i64 8
%call23 = bitcast i8* %bytesA2.i to i64*
store i64 %bytesA, i64* %call23, align 1, !tbaa !6
... remaining arguments packed
; Launch dataflow graph SgemmRoot with arguments packed in %call23
%graphID = call i8* @llvm.hpvm.launch(i8% SgemmRoot to i8*), i8* %call23, i1 false)
call void @llvm.hpvm.wait(i8* %graphID)
6.2 SGEMM Kernel generated from GPU backend

After code generation for the GPU target, a GPU kernel is generated which is shown in listing 2. Again, inlined comments point out the performed operations and how they are introduced by the backend.

Listing 1: SGEMM in HPVM

```assembly
; ModuleID = 'build/hpvm_sh_default/main.hpvm.ll'

; Generated Kernel. Note the address space qualifiers: addrspace (1), addrspace (3) relates
; to global address space, addrspace (3) represents local address space accessible only for
; work items in the same work group. A tile of matrix B has been placed in local memory.
define void @SgemmLeaf (float addrspace (1) * in %A, i64 %bytesA, i32 %lda, float addrspace (1) * in %B, i64 %bytesB, i32 %ldb, float addrspace (1) * in out %C, i64 %bytesC, i32 %ldc, i32 %k, float %alpha, float %beta, float addrspace (3) * nocapture %shB, i64 %bytesshB) #0 {
  entry:
  %c = alloca [16 x float], align 16
  %0 = bitcast [16 x float]* %c to i8*
  ; ...
  ; Calls to OpenCL library calls are generated by the backend, to implement the HPVM
  ; intrinsic depends on the dataflow graph structure.
  %1 = call i32 @get_local_id(i32 0)
  %2 = call i32 @get_local_id(i32 1)
  %3 = call i32 @get_group_id(i32 0)
  %4 = call i32 @get_group_id(i32 1)
  %5 = call i32 @get_local_size(i32 0)
  %mul = mul nsw i32 %5, %2
  %add = add nsw i32 %mul, %1
  ; ... remaining computation
  ret void
}

; The OpenCL function implementations for the target platform are found by linking with libcclc
```
As pointed out in lines 28-29, the OpenCL library function implementations are found in libclc and are available after linking. For an nVidia GPU target, they are implemented using llvm intrinsics that are recognized by the LLVM NVPTX backend (and translated down to reading special hardware registers). Listing 3 shows such a function that is included in the kernel file we have generated after linking.

Listing 2: SGEMM - Kernel code generated from HPVM: LLVM + OpenCL library calls

Listing 3: OpenCL library function implementation from libclc

6.3 SGEMM Host generated from GPU backend

The GPU backend also generates host code to perform the necessary data copies and launch the generated kernel. The generated host code is shown in listing[]. Again, inlined comments
point out the performed operations.

1; ModuleID = 'build/hpvm_sh_default/main.hpvm.ll'
2
3; Function launching the dataflow graph defined by SgemmRoot and
4; performing calls to HPVM runtime
5define i32 @main(i32 %argc, i8** %argv) #2 {
6    entry:
7        ; ...
8    ; The following two calls replace the llvm.hpvm.init().
9    ; HPVM runtime initializes the OpenCL context.
10    %12 = call i8* @llvm_hpvm_ocl_initContext(i32 2)
11    ; This call loads the kernel from disk, compiles and creates a kernel
12    ; object associated with the dataflow graph. The information required
13    ; to launch this kernel are returned.
14    %graphSgemmLeaf = call i8* @llvm_hpvm_ocl_launch(i8* %FilenamePtr, i8* %KernelNamePtr)
15    ; Global variable storing the returned information
16    store i8* %graphSgemmLeaf, i8** @graphSgemmLeaf.addr
17    ; ...
18    ; Host calls to HPVM runtime. Locations of arrays A, B, and C
19    ; should be tracked
20    call void @llvm_hpvm_track_mem(i8* %25, i64 %mul19) #1
21    call void @llvm_hpvm_track_mem(i8* %27, i64 %mul22) #1
22    call void @llvm_hpvm_track_mem(i8* %29, i64 %mul25) #1
23    ; ...
24    ; Argument Packing
25    %call23 = tail call noalias i8* @malloc(i64 88) #1
26    %A1.i = bitcast i8* %call23 to float**
27    store float* %A, float** %A1.i, !tbaa !3
28    %bytesA2.i = getelementptr inbounds i8* %call23, i64 8
29    %23 = bitcast i8* %bytesA2.i to i64*
30    store i64 %bytesA, i64* %23, !tbaa !6
31    ; ... remaining argument packing
32    ; Runtime call replacing the llvm.hpvm.lanch intrinsic.
33    ; The called function, LaunchDataflowGraph, is responsible for calling
34    ; the x86 function generated by the GPU backend that launches the
35    ; generated kernel.
36    %graphSgemmRoot = call i8* @llvm_hpvm_x86_launch(i8* %LaunchDataflowGraph, i8* ← %call23)
37    call void @llvm_hpvm_x86_wait(i8* %graphSgemmRoot)
38    ; ...
39    ; Runtime call to request array C
40    call void @llvm_hpvm_request_mem(i8* %38, i64 %mul25) #1
41    ; Remove entries from memory tracker
42    call void @llvm_hpvm_untrack_mem(i8* %40) #1
43    call void @llvm_hpvm_untrack_mem(i8* %42) #1
44    call void @llvm_hpvm_untrack_mem(i8* %44) #1
45    ; Read information associated with kernel and clear the OpenCL runtime
46    ; information and context
47    %45 = load i8** %graphSgemmLeaf.addr
48    call void @llvm_hpvm_ocl_clearContext(i8* %45)
49    ret i32 0
50 }
51
52; Declarations of HPVM runtime functions
53declare void @llvm_hpvm_track_mem(i8*, i64) #0
54declare i8* @llvm_hpvm_ocl_initContext(i32)
55declare i8* @llvm_hpvm_ocl_launch(i8*, i8*)
56declare void @llvm_hpvm_ocl_wait(i8*)
57
58; Function associated with allocation node, modified by the backend to
59; only compute and return the allocation size.
60; To perform local memory allocation for a GPU, the size needs to be known
61; at launch time and passed as an argument. To that end, we use the
62; modified allocation node function to perform the size computation.
63; We insert a call to it in the host code before the kernel launch.
64define %struct.out.Allocation @Allocation1(i32 %block_x, i32 %block_y, i32 %ocall) #2 {
66  %mul = mul nsw i32 %block_y, %block_x
67  %conv = sext i32 %mul to i64
68  %null = shl nsw i64 %conv, 2
69  %returnStruct = insertvalue %struct.out.Allocation undef, i8* null, 0
70  %returnStruct2 = insertvalue %struct.out.Allocation %returnStruct, i64 %null, 1
71  ret %struct.out.Allocation %returnStruct2
72  }
73
74  ; x86 function for kernel setup, data copying and call.
75  ; This is genFunc (see section Compilation) for the generated kernel
76  define %emptyStruct.20 @SgemmRoot2 (float* %A, i64 %bytesA, i32 %lda, float* %B, i64 ←
77  %bytesB, i32 %ldb, float* %C, i64 %bytesC, i32 %ldc, i32 %k, float %alpha, float ←
78  %beta, i32 %block_x, i32 %block_y, i32 %grid_x, i32 %grid_y) {
79    entry :
80      ; Read information about the kernel that needs to be launched
81      ; We use it to determine which kernel to set arguments for
82      %graph.SgemmLeaf = load i8** @graphSgemmLeaf.addr
83      
84      ; Setting up kernel arguments
85      ; llvm_hpvm_ocl_argument_ptr / scalar / shared are wrappers around the OpenCL
86      ; runtime call setKernelArgument, that pass the arguments as required.
87      ; llvm_hpvm_ocl_argument_ptr additionally makes calls to the memory
88      ; tracker to determine if memory copy is required for the passed
89      ; argument. If required performs the data transfer and updates the
90      ; memory tracker information.
91      %A.i8ptr = bitcast float* %A to i8*
92      %0 = call i8* @llvm_hpvm_ocl_argument_ptr (i8* %graph.SgemmLeaf, i8* %A.i8ptr, i32 0, i64 ←
93      %bytesA, i1 true, i1 false)
94      %bytesA.ptr = alloca i64
95      store i64 %bytesA, i64* %bytesA.ptr
96      %bytesA.i8ptr = bitcast i64* %bytesA.ptr to i8*
97      call void @llvm_hpvm_ocl_argument_scalar (i8* %graph.SgemmLeaf, i32 12, i64 %bytesA.i8ptr)
98      
99      ; Compute local and global workgroup sizes
100     %LocalWGSize = alloca [2 x i64]
101     %LocalWGSize.0 = bitcast [2 x i64]* %LocalWGSize to i64*
102     %5 = sext i32 %block_x to i64
103     store i64 %5, i64* %LocalWGSize.0
104     %LocalWGSize.1 = getelementptr i64* %LocalWGSize.0, i64 1
105     %4 = extractvalue %struct.out.Allocation %GlobalWGSize.1, 1
106     call void @llvm_hpvm_ocl_argument_shared (i8* %graph.SgemmLeaf, i32 12, i64 %4)
107     ; set remaining kernel arguments
108     
109     %event.SgemmLeaf = call i8* @llvm_hpvm_ocl_executeNode (i8* %graph.SgemmLeaf, i32 2, i64 ←
110     %LocalWGSize.0, i64 %GlobalWGSize.0)
111     
112     ; Runtime call to launch kernel
113     call void @llvm_hpvm_ocl_wait (i8* %graph.SgemmLeaf)
114     ; Free allocated memory.
115     ; In our implementation, these are no-ops, since we free memory when
116     ; no longer required as determined by the memory tracker.
117     call void @llvm_hpvm_ocl_free (i8* %0)
118     call void @llvm_hpvm_ocl_free (i8* %1)
119     call void @llvm_hpvm_ocl_free (i8* %2)
120     
121     ret %emptyStruct.20 undef
122  }
123
124  ; Function called by launch runtime call. Used to perform
125  ; - argument unpacking
126  ; - call to the genFunc that is generated by the GPU backend
127  define i8* @LaunchDataflowGraph (i8* %data.addr) {

Listing 4: SGEMM Host generated from GPU backend
References

[1] Chris Lattner and Vikram Adve. LLVM: A compilation framework for lifelong program analysis and transformation. In Proc. Conf. on Code Generation and Optimization, pages 75–88, San Jose, CA, USA, Mar 2004.

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[3] John A Stratton, Christopher Rodrigues, et al. Parboil: A revised benchmark suite for scientific and commercial throughput computing. Technical report, 2012.