Memristors with Initial Low-Resistive State for Efficient Neuromorphic Systems

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1. Introduction

Developing new hardware for artificial intelligence systems is a major goal for the government of technologically advanced countries and leading companies in the field of nanoelectronics, and investments in this field are expected to keep growing exponentially in the next years. Recent studies demonstrated that crossbar arrays of metal–insulator–metal (MIM) nanocells—often called memristors—can be used to construct artificial neural networks (ANN) with unsupervised learning capability and they have been already employed to accomplish sophisticated operations, such as image classification, encryption, and position detection. In an ANN, memristors are used as electronic synapses, that is, elements that connect two neurons and that show the property of changing their conductance between different levels—often called resistive switching (RS).

The initial conductance of most MIM-like memristors is in the range of few pico-/nano-siemens with a larger set voltage or a higher resistance compared to the following cycles—from now on, we will refer to this type of devices with the etiquette “forming memristors.” The conductance of this type of devices can be increased by applying electrical stimuli or a higher resistance compared to the following cycles. From now on, we will refer to this type of devices with the etiquette “forming memristors.” The conductance of this type of devices can be increased by applying electrical stimuli.
between the two metallic electrodes; this generates local defects at random locations in the microstructure of the insulator (i.e., intrinsic vacancies and/or impurities from adjacent metallic electrodes) that promote charge transport.\textsuperscript{[15,16]} If the density of defects in the insulator is high enough a conductive nanofilament (CNF) can be effectively formed, which drives all the current flowing between the two electrodes and results in an overall linear conductance in the range of few millisiemens.\textsuperscript{[7]} In most MIM nanocells, the defects in the insulator and the CNF are stable after the bias is removed, and the conductance of the MIM cell can only be reduced by applying additional electrical stimuli (normally with opposed polarity).\textsuperscript{[5–7]}

When the CNF is only partially formed, it is said that the device is operated in a high-resistive state (HRS), and controlling its conductance in this regime is very challenging because the current flows across a random number of defects spread along the volume of the insulator, and the formation of new defects results in exponential increases of conductance.\textsuperscript{[8,9]} On the contrary, when the CNF is completely formed, it is said that the device is operated in low-resistive state (LRS), and controlling its conductance is much easier because all the current flows along the CNF, which can be accurately widened and narrowed by applying electrical stimuli of different polarities.\textsuperscript{[10]} MIM nanocells operating at high conductances above quantum conductance (77.5 μS),\textsuperscript{[11]} with a high linearity between current and voltage, can lead to accurate analog computing and stable multilevel states.\textsuperscript{[12]}

As the weight (i.e., conductance) of electronic synapses needs to be increased and decreased progressively and in a linear manner, MIM-like memristors for ANNs are normally operated in LRS and the typical maximum/minimum conductance ratio ($I_{\text{MAX}}/I_{\text{MIN}}$) is $\approx 10$ (see Table S1, Supporting Information). Consequently, most memristive electronic synapses need an initialization step to increase their initial conductance, which is an important nuisance for the fabrication of ANNs because it increases the complexity of the programming algorithms and peripheral hardware.\textsuperscript{[13]} One common solution to mitigate this problem is to fabricate forming-free memristors by introducing impurities in the insulator during the manufacturing process via ion implantation\textsuperscript{[14,15]} and/or reducing the thickness of the insulating film,\textsuperscript{[16]} which increases the initial conductance of the devices to the HRS (i.e., an effective CNF is not completely formed). However, the device-to-device variability of forming-free memristors with initial conductance in HRS (namely HRS memristors) is high (see Table S2, Supporting Information), due to the inhomogeneous distribution of impurities in the insulating film.\textsuperscript{[12,17]} Such increased device-to-device variability of the initial conductance represents a problem for the training of the ANN, as it may slow down the learning process and even present convergence problems.\textsuperscript{[18]}

Here, we report the first fabrication of memristors whose initial conductance is already in the LRS regime (namely LRS memristors) by using ultrathin TiO$_2$ films synthesized by magnetron sputtering. We have selected TiO$_2$ because, compared to other metal-oxides often used as dielectric in memristors (i.e., HfO$_2$, TaO$_x$, Al$_2$O$_3$), this material has the lowest bandgap. This makes that the initial conductance is higher even if the material might not be completely shorted. For all the devices tested (more than 20), the initial electrical resistance falls within a window narrower than one order of magnitude (i.e., between 100 and 714 Ω), which is much smaller than that of HRS memristors and forming memristors. The switching thresholds are uniform enough to enable analog tuning of individual devices in a crossbar-integrated circuit. More importantly, the compact design of peripheral circuits is feasible as devices are forming free, and the maximum switching threshold is compatible with the core voltage of standard complementary metal-oxide-semiconductor (CMOS) processes.

2. Results and Discussion

2.1. Device Characterization

Figure 1a shows the optical microscope image of an array of Au/TiO$_2$/Au cross-point memristors with lateral sizes ranging from 5 × 5 μm (left column) to 50 × 50 μm (right column), and Figure 1b shows a 3D topographic map of a 5 × 5 μm Au/TiO$_2$/Au memristor, collected via atomic force microscopy (AFM). Figure 1c shows an AFM topographic map of the surface of the sputtered TiO$_2$ film (on a 300 nm SiO$_2$/Si substrate). The root-mean-square (RMS) surface roughness is 4.6 nm, much larger than that of the SiO$_2$/Si substrate (≤0.3 nm),\textsuperscript{[19]} and much larger than that of TiO$_2$ films grown by atomic layer deposition (ALD) on SiO$_2$/Si substrates (≤0.2 nm).\textsuperscript{[20]} As Figure 1c shows, the surface of the sputtered TiO$_2$ thin film is composed of tall grains with diameters 131.2 ± 58.9 nm (see Figure 1d and S1, Supporting Information) separated by deep phase boundaries. To further characterize these features, we use focused ion beam (FIB) to cut the MIM cells and fabricate thin lamellas, and analyze them using transmission electron microscopy (TEM). The cross-sectional TEM images (Figure 1f) reveal that the thickness of the sputtered TiO$_2$ film is 4.5 nm (as expected), and that it contains few-nanometer-wide regions rich in Au every 125 nm, which correlate to the deep phase boundaries observed in the topographic AFM maps (Figure 1e).

When applying sequences of ramped voltage stresses (RVSs), the devices always show initial conductance of $\approx 5$ mS (typical of LRS regime) without the need of a forming process, followed by a conductance decrease to HRS regime at 0.1 V (see Table S1, Supporting Information).\textsuperscript{[9]} The device-to-device variability of the Au/TiO$_2$/Au memristors is quantified by calculating the coefficient of variance (C$_V$), defined as the standard deviation ($\sigma$) divided by the mean value ($\mu$),\textsuperscript{[21]} at 0.1 V. Figure 2g shows the histogram of set/reset voltage by combining all the 15 devices; in total, we measured 46 devices and 36 of them (i.e., 78%) exhibit similar switching behavior. Figure 2f shows the statistical analysis of set/reset voltage of 15 different devices. The device-to-device variability of the Au/TiO$_2$/Au memristors is quantified by measuring RVS in 15 devices and calculating the coefficient of variance (C$_V$), defined as the standard deviation ($\sigma$) divided by the mean value ($\mu$),\textsuperscript{[21]} at 0.1 V. Figure 2g shows the histogram of set/reset voltage by combining all the 15 devices; in total, 300 cycles are considered for both set and reset. The $\mu$ and C$_V$ are $-1.285$ V and 0.156 for set voltage, and 0.811 V and 0.153 for reset voltage, respectively. Figure 2d–g demonstrates...
that the bipolar RS is stable over multiple switching cycles, and that the device-to-device variability of the switching voltages is reasonably low. Current versus time curves measured under 0.1 V at room temperature in HRS and LRS prove long state/data retention of more than a day (Figure 2h).

The variability of the initial conductance of the Au/TiO$_2$/Au memristors is quantified by measuring RVS in 20 devices (Figure 3a) and plotting the value of the resistance at 0.1 V, which indicates that the initial resistance of all the devices ranges between 10$^2$ and 10$^3$ Ω. The device-to-device variability of the initial conductance of LRS memristors (Figure 3a) is compared with that of HRS memristors (in Figure 3b) and forming memristors (see Figure 3c) also fabricated during this investigation (see Methods section). As Figure 3d and S2, Supporting Information, show, the device-to-device variability of the LRS memristors is the lowest, indicating that these Au/TiO$_2$/Au devices present a competitive advantage (compared to HRS memristors and forming memristors) for the realization of ANNs.

Figure S3, Supporting Information, confirms that the relationship between current and voltage is linear, indicating that the devices are initially in LRS probably due to the formation of Au-rich regions in the TiO$_2$ film during the fabrication process (as shown in Figure 1e). Considering that the CNFs have the shape of a truncated cone (one of the radii is assumed to be four times greater than the other), which is the most typically observed in MIM-like RS devices,$^{[22]}$ we can estimate its size as follows.

![Figure 1. Fabrication of Au/TiO$_2$/Au synapses. a) Optical microscopy image of Au/TiO$_2$/Au cross-point memristor cells with sizes ranging from 50 × 50 μm to 5 × 5 μm. b) The 3D atomic force microscopy (AFM) topographic image of a 5 × 5 μm Au/TiO$_2$/Au memristor at the cross-point area (height color scale: black = 0 nm, white = 300 nm). Scale bar: 250 nm. c) AFM topography map of the sputtered TiO$_2$ on 300 nm SiO$_2$/Si substrate. d) Statistical analysis of TiO$_2$ phase size from 5 × 5 μm large-area scan. The original image and data-processing method are detailed in Figure S3, Supporting Information. e) Surface profile in (c) from A to A’ crossing two phases. f) Cross-sectional transmission electron microscope (TEM) image of an Au/TiO$_2$/Au device showing two phases, for which the phases size is in the same scale with (e). Scale bar: 25 nm.](image-url)
$r = \sqrt{\frac{\rho_{CNF} t_{OX}}{4\pi R}} = \frac{1}{2} \sqrt{\frac{\rho_{CNF} t_{OX}}{\pi R}}$  \hspace{1cm} (1)

where $R$ is the device resistance for a certain applied voltage (extracted from the RVS, see Figure 3a), $\rho_{CNF}$ is the electrical resistivity of the CNF (the conductivity is assumed to be $\sigma_{CNF} = 1/\rho_{CNF} = 5 \times 10^5 \Omega^{-1} \text{m}^{-1}$, an average value of several previously employed conductivities in different models; in particular, this value was chosen from ref.[22]), $t_{OX}$ is the thickness of the insulator (4.5 nm according to Figure 1f), and $r$ is one of the truncated cone radii. By repeating the calculation for all the devices measured, it can be observed that the deviation on the cone radii is relatively low (see Figure 3e). By calculating the radii of the CNF at different reading voltages, it is possible to discern the CNF narrowing at the onset of the reset process (Figure 3f), which is consistent with the observations in previous reports.[22–24] It is worth noting that the CNF radii calculated in Figure 3e,f are much narrower than that of the grain boundaries (GBs) observed in AFM scans (Figure 1e) and TEM images (Figure 1f). The reason behind this observation is that, despite the GBs are regions rich in Au ions (in these zones the CNF formation is favored), only few locations may be included in the percolation path that constitutes the CNF that shortens the electrodes.[25]

The switching of the Au/TiO$_2$/Au devices has been also confirmed by applying sequences of pulsed voltage stresses. First, binary bipolar RS has been confirmed. Figure 3g shows four consecutive read–write–read–erase–read operation of the device under pulse mode. The device starts in HRS with 1 nA read by a pulse of 0.5 V 1 ms. Then, the device is switched on by a write
Another read pulse shows the device is switched on with a current higher than 1 μA. Then, the device is switched back to HRS by an erase pulse of 5 V 1 ms. A relative high read pulse of 0.5 V is used to enable the reading of HRS over the noise level 0.2 nA.

2.2. Neuromorphic Circuits with Forming-Free Memristors

The most common operation in most practical neuromorphic networks is vector-by-matrix multiplication (VMM). The practical approach to implement such massive VMM blocks is to divide them into smaller VMMs (e.g., 64 \times 64 arrays) and integrate responses in the analog/digital domain. Figure 4a shows the emulation of a mixed-Signal VMM block using adjustable...
Figure 4. The circuit schematic of a vector-by-matrix multiplication (VMM) block and related components. a) The top-level schematic of a VMM block based on two-terminal memristive crossbars consisting of a crossbar, switch matrices, decoders, and sensing circuits. The analog input signal is supplied either by a digital-to-analog converter (DAC) (e.g., in time-multiplexed architectures) or the global sensing circuit from the previous stage (full-analog circuits). The tuning process is implemented via analog multiplexers (MUXes). The circuit implements vector-by-matrix operation (the input vector is in the analog domain, and the weight matrix is encoded to the conductance of memristors), and the response is sensed in the form of current by the sensing circuit (transimpedance amplifiers (TIAs)). b) The detailed circuit diagram of one channel that performs two-quadrant multiplication with highlighted lumped parasitic from crossbar and analog switch matrix (ASM). It is imperative to design the analog peripheries (DAC and local sensing) in core voltage to ensure efficient design. Our proposed memristors are forming free, which allows us to design the ASM in core voltage as well and improve throughput per area by $\times 1$ and energy by $\times 0.85$. In this figure, $D_i$ is input data; $I_u$ is unit current of the DAC; $V_b$ is bias voltage; $R_{F,1}$ and $R_F$ are TIA gains in DACs and sensing circuits, respectively; $C_{g,fi}$, $C_{sl,fi}$, $C_{bl,fi}$, $C_{g,bl,fi}$, $C_{bl,bl,fi}$ are parasitics associated crossbar lines; $G_{ave}$ is average conductance of the devices; $V_S$ ($V_{US}$) is the pulse signal applied to the selected (unselected) column.

Memristive devices. Due to their integration density, VMMs based on passive crossbars are promising\cite{30}; however, the fabrication of passively integrated memristive neuromorphic circuits is challenging due to the required uniformity and low switching threshold distribution. The uniformity allows the individual tuning of devices and mitigating half-select disturbance. Figure 2h shows low variability in switching thresholds, particularly in reset operation, which grants us to implement the V/2 tuning scheme\cite{29} (in a crossbar-integrated circuit) without employing partitioning/isolation/selector circuits that impose large-area overheads. We study this issue in our recent work\cite{21} by extensive simulations and demonstrate excellent prospects for devices with similar variability characteristics.

Here, we focus on the second challenge, that is, low-voltage switching characteristics and forming-free operation. The implications of low-voltage switching on inference accelerators’ performance are significant, even though we only perform switching operations during the tuning phase (note that our primary focus is on ex situ trained classifiers). The forming-free function and low switching voltage of memristors are crucial to designing CMOS compatible, (and hence) compact, and energy-efficient neuromorphic circuits. For our reported devices, the switching voltage in both reset and set regimes are very low. The $\mu + 3\sigma$ (where $\mu$ is the average and $\sigma$ is the standard deviation) of the set and reset switching threshold distributions are very close to 1.8 and 1.2 V, respectively. Unlike most previous devices, which either require high-voltage electroforming processes or feature large switching voltages, our devices are initially in the LRS state (and hence do not require high-voltage electroforming) and are switchable with CMOS-compatible input/output voltages (e.g., 1.8 V, which is the core voltage of a standard 180 nm process\cite{31}). Therefore, we may design all auxiliary CMOS circuitries that are inevitable to implement the desired functionality using thin-oxide MOSFETs.

Figure 4b shows the detailed yet simplified circuit schematic of one input and one output channel of VMM in Figure 4a. The analog switch matrix (ASM) block connects external pulse signals, peripheral circuits (data converter and local sensing), and the crossbar. It is crucial to use thin-oxide metal-oxide-semiconductor (MOS) devices (core-voltage devices) in ASM. This stems from the fact that voltage drop on analog switches could be highly detrimental to the VMM accuracy.\cite{31} Thus, CMOS switches in ASM could be as large as $10 \times$ to $50 \times$ of the minimum size, depending on the block size, network, etc. In crossbars with large tuning voltages, the use of thick-oxide MOSFETs in ASM is indispensable to avoid junction breakdown and punch through. This not only makes the ASM circuit large but also would necessitate the inclusion of level-shifter circuitries ($\approx 10 \times$ minimum size thick-oxide device) to deliver the voltage from the core-voltage decoders to the ASM at a proper level. As a second side effect, the larger the ASM, the higher inter- and intra-VMM parasitics. The sizeable parasitic capacitance associated with ASM affects the VMM speed and reduces the overall throughput.

To quantitatively assess our claims, we study a representative neuromorphic architecture: a fully analog massive multipli...
perceptron with seven hidden layers and ≈100M parameters (1024·16 384·16 384·4096·1024·1024·512·512·256·256·10). Note that as of 2017, >60% of the Google machine learning workload was two multilayer perceptron networks.\cite{33,34} We evaluate the performance of this network with two benchmarks: i) our forming-free devices that feature low switching voltage, and ii) passive devices that share the same specifications but require forming and high switching voltages. We design the classifier targeting high throughput and use physical layout and simulation of critical components (64 × 64 VMM blocks, peripheral circuits, digital blocks, ASMs, etc.) in Silterra’s 180 nm CMOS process.

Let us emphasize several vital points before discussing the results. Though the actual size of the fabricated device is much larger, we assume 4F² passive devices (where F is the half-pitch metal feature size, 250 nm in this CMOS technology) for meaningful results. Note the grain sizes in Figure 1 are ≈100 nm, which supports device miniaturization prospects. Since the device area shrinkage reduces the leakage current as well, it is expected (and presumed in this work) that the average conductance scale is linearly with device size. We simulate a critical path from one input to one output in all layers and properly model the intra-block parasitic capacitance on electrodes and global lines connecting the local sensing blocks in every layer. The total parasitic capacitance on electrodes consists of line-to-line capacitance in crossbar structure (M5/M4/M3) that includes coupling and fringing capacitors between conductors and the parasitics associated with ASM. We use the same design of critical analog components for both benchmarks; however, we optimize the settling time in each scenario, for example, by fine-tuning the compensation circuits within amplifiers. The neurons in the last layer are loaded with a 100 F capacitor.

Table S3, Supporting Information, shows relevant process parameters and simulations results. Our results indicate that the classifier with our forming-free memristors offers 1.83× better throughput per area and consumes ×0.85 less energy to classify a single image of the CIFAR-10 dataset, which stems from ≈63% better density and ≈17% faster operation. We explain the superior density by arguing that our forming-free devices are compatible with a voltage-cost design of ASM and operate without level shifters resulting in ≈35 × 10⁻⁸ μm² VMM block versus 86 × 10³ μm² required otherwise. The improved speed is also attributed to the fact that the total parasitic capacitance on every local sensing input lines (top electrodes or bitlines) is only 71 F (far less than 289 F) obtained for the memristors that require forming) in addition to the larger parasitics on global lines as well.

Finally, we would like to point out that our LRS memristors could also be used to build reliable fixed-resistance physically unclonable function circuits efficiently, a building block for many cryptographic systems. These circuits are normally designed using HRS pristine memristors, and previous works\cite{16,21} experimentally demonstrate significant performance improvement in part because of the elimination of tuning circuits. The downside of this approach is higher bit-error-rate due to the reduced noise margin and large temperature dependence of HRS pristine devices. Our proposed forming-free LRS memristor technology offers a clear advantage here: forming-free LRS memristors have the most benefits of previous designs\cite{16,21} and, additionally, provide a far better noise margin and significantly better temperature dependency.

3. Conclusion

We have fabricated the first memristors with initial conductance in the LRS regime, using sputtered TiO₂ films with thicknesses of ≈5 nm. The initial resistance and the switching voltages of these memristors are much more homogeneous than those of standard memristors (i.e., with the necessity of forming) and traditional forming-free memristors (i.e., with initial conductance in the HRS regime). The low device-to-device variability of the electrical properties of these memristors allowed using them to emulate efficient neuromorphic systems, and we checked their performance during CIFAR-10 image classification. We achieved ×1.83 better throughput per area and ×0.85 less energy consumption than standard memristors (i.e., with the necessity of forming), which stems from ≈63% better density and ≈17% faster operation. Our work presents a facile and inexpensive strategy to improve memristive neuromorphic systems by materials property modification, although the endurance of the memristors may require further improvement via device engineering before implantation in real systems.

4. Experimental Section

Fabrication of LRS Memristors: Matrixes of cross-point bottom electrodes consisting of 40 nm Au and 10 nm Ti (for better adhesion) were patterned on a 300 nm SiO₂/Si wafer by photolithography (mask aligner from SUSS MicroTec, model MJ84), electron beam evaporation (Kurt J. Lesker, model PVD75), and liftoff (rinse in acetone for 1 min). Then, a 4.5 nm thick TiO₂ film was deposited by magnetron sputtering (Kurt J. Lesker, model PVD 75), using a power of 60 W and a pressure of 5 mTorr during 10 min. Then top electrodes with the same shapes as the bottom ones (but rotated 90°) were patterned on the TiO₂ crossing the bottom electrodes and delimiting devices of areas 5 × 5 μm. The thickness of the top metal was 40 nm. Au.

Fabrication of HRS and Forming Memristors: The HRS memristors consisted of Au/Ti/h-BN/Cu structures, in which the h-BN stacks were synthesized by chemical vapor deposition (CVD) on Cu foils and had a thickness of 5–7 layers.\cite{33,34} The top Au/Ti electrodes were deposited using an electron beam evaporation and a laser-patterned shadow mask directly on the as-grown h-BN/Cu samples (i.e., no transfer process was required), and the Cu substrate used for the h-BN growth was served as bottom electrode.\cite{29} The lateral size of these devices was 50 × 50 μm. The forming memristors consisted of Au/h-BN/Au structures, in which the h-BN stacks were synthesized by CVD on Cu foils and had a thickness of 15–18 layers. The devices had a cross-point structure with the lateral size of 5 × 5 μm\cite{16,21} and required the transfer of the h-BN on Au pre-patterned electrodes on 300 nm SiO₂/Si wafers. In both cases, the thickness of the metallic electrodes deposited was 40 nm.

Device Characterization: The device morphology was investigated by optical microscopy (DM 4000M, Leica), scanning electron microscope (SEM, Supra 55, Carl Zeiss), and AFM (Multimode V, Veeco). Cross-sectional TEM (Thermo Fischer Scientific Titan Themis 60-300) was used to confirm the device structures and dielectric thickness. To do so, an FIB (model Helios NanoLab 450s from FEI) was used to cut the cross-point region of a fresh device into ultrathin lamellae. Before the FIB cuts, a protective 2 μm thick Pt layer was deposited on the devices. The electrical characterization was performed by using a...
probe station (M150, Cascade) connected to a semiconductor parameter analyzer (Keithley 4200). All the I–V curves were collected by applying RVS mode.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Data Availability Statement**

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

**Keywords**

forming-free devices, low-resistive state, memristors, neuromorphic systems, titanium dioxide

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