Abstract—In recent years, reversible logic has emerged as a promising computing paradigm having application in low power CMOS, quantum computing, nanotechnology, and optical computing. The classical set of gates such as AND, OR, and EXOR are not reversible. This paper utilizes a new 4 x 4 reversible gate called TSG gate to build the components of a primitive reversible quantum ALU. The most significant aspect of the TSG gate is that it can work singly as a reversible full adder, that is reversible full adder can now be implemented with a single gate only. A Novel reversible 4:2 compressor is also designed from the TSG gate which is later used to design a novel 8x8 reversible Wallace tree multiplier. It is proved that the adder, 4:2 compressor and multiplier architectures designed using the TSG gate are better than their counterparts available in literature, in terms of number of reversible gates and garbage outputs. This paper provides an initial threshold to build more complex systems which can execute complicated operations using reversible logic.

Keywords—Reversible Logic, Quantum Computing, Reversible gates, TSG Gate, Reversible ALU.

I. INTRODUCTION

This section provides an effective background of reversible logic with its definition and the motivation behind it.

A. Definitions

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann’s constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Furthermore, voltage-coded logic signals have energy of Esig = ½CV^2, and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [22]. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an NXN reversible gate can be represented as

\[ I_v=(I_1,I_2,I_3,I_4, \ldots \ldots \ldots \ldots \ldots I_N) \]

\[ O_v=(O_1,O_2,O_3, \ldots \ldots \ldots \ldots \ldots O_N). \]

Where \( I_v \) and \( O_v \) represent the input and output vectors respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states. There is a number of existing reversible gates such as Fredkin gate[3,4,5], Toffoli Gate (TG) [3, 4] and New Gate (NG) [6].

B. Motivation behind Reversible Logic

The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design [10], optical computing [11], quantum computing [12] and nanotechnology [13]. The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible, hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible). Thus, Quantum Arithmetic must be built from reversible logic components [14].

C. Proposed Contribution In Reversible Logic

In this paper, the focus is on the application of a new reversible 4x4 TSG gate [23,24]. The most significant aspect of the proposed gate is that it can work singly as a reversible
full adder, that is reversible full adder can now be implemented with a single gate only. A novel reversible 4:2 compressor is also designed from the proposed TSG gate. Furthermore, the optimized adder and 4:2 compressor are used to design the novel 8x8 reversible Wallace tree multiplier. It is proved that the adder, 4:2 compressor and multiplier architecture designed using the proposed TSG gate are better than their counterparts existing in literature, in terms of number of reversible gates and garbage outputs. This is the first attempt to design a reversible 4:2 compressor and reversible Wallace tree multiplier as far as existing literature and our knowledge is concerned. Minimizing the number of garbage outputs and reversible gates is one of the major concerns in reversible logic [7,8,9] and it is observed that TSG gate achieves this leading to high speed and low power reversible circuits. The reversible circuits proposed and designed in this work form the basis for an ALU of a primitive quantum CPU.

A number of reversible full adders were proposed in [6,7,8,9]. The reversible full adder circuit in [6] requires three reversible gates (two 3*3 new gates and one 2*2 Feynman gate) and produces three garbage outputs [garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to other gate]. The reversible full adder circuit in [7,8] requires three reversible gates (one 3*3 new gate, one 3*3 Toffoli gate and one 2*2 Feynman gate) and produces two garbage outputs. The design in [9] requires five reversible Fredkin gates and produces five garbage outputs. The proposed full adder using TSG in Figure 2 requires only one reversible gate (one TSG gate) and produces only two garbage outputs. Hence, the full-adder design in Figure 2 using TSG gate is better than the previous full-adder designs of [6,7,8,9]. A comparison of various full adders is shown in Table I.

III. REVERSIBLE 4:2 COMPRESSOR

The 4:2 compressor was introduced by Weinberger in 1981 which he called “4-2 carry save module” [16]. The 4:2 compressor structure actually compresses five partial products bits into three in which four of the inputs are coming from the same bit position of the weight j while one bit is fed from the neighboring position j-1 (known as carry-in). The outputs of 4:2 compressor consists of one bit in the position j and two bits in the position j+1. The structure of 4:2 compressor is shown in Figure 3. The efficiency of such a structure is higher since it reduces the number of partial product bits by one half at each stage. The delay of 4:2 compressor is 3 XOR gates in series making it more efficient than using 3:2 counters (full adder) in a regular “Wallace Tree” and has important feature that the interconnections between 4:2 cells follow more regular pattern than in case of the “Wallace Tree”[17,18,25].

In this paper, a reversible 4:2 compressor is also proposed as shown in Figure 4. The reversible 4:2 compressor is designed from two TSG gates, and it appears from the survey of literature that this is first attempt to design reversible 4:2 compressor. Figure 5 shows the block diagram of 4:2 compressor. Table II shows the comparison results of the 4:2 compressor using TSG with its implementation using existing reversible full adders.
**Figure 4.** Proposed Reversible 4:2 Compressor Designed from TSG gate

**Figure 5.** Block Diagram of Reversible 4:2 Compressor

**Table II.** A Comparison of 4:2 Compressors Using Various Full Adder Circuits

|                     | Number of Reversible Gates | Number of Garbage Outputs | Unit Clock Cycle |
|---------------------|-----------------------------|----------------------------|------------------|
| Full adder          | 2                           | 4                          | 2                |
| Using TSG           |                             |                             |                  |
| Existing Circuit[6] | 6                           | 6                          | 6                |
| Existing Circuit[7,8]| 6                           | 4                          | 4                |
| Existing Circuit[9] | 10                          | 10                         | 10               |

**Figure 6.**
(a) Use of Fredkin Gates to Generate the Partial Products In Parallel
(b) Proposed Reversible 8x8 Wallace Tree Multiplier Using Reversible 4:2 Compressor (R 4:2) and TSG gates
IV. REVERSIBLE WALLACE TREE

A multiply operation consists of three stages: partial products generation stage, partial products addition stage, and the final addition stage [19,20,21]. The second stage is the most important and determines the overall speed of the multiplier. In high-speed designs, the Wallace tree construction method is usually preferred to add the partial products in a tree-like fashion. The Wallace tree is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier.

A. Reversible Wallace Tree Construction

The method used to construct the Wallace tree considers all the bits in each fours rows at a time and compress them in an appropriate manner. The Wallace tree uses 4:2 compressor, full adders and half adders to compress the partial products tree. This paper proposes a reversible 8x8 Wallace tree multiplier using the reversible TSG gate. The proposed architecture can be generalized for NNX bits. The reversible half adder, full adder and 4:2 compressor designed from reversible TSG gate are used as the basic building blocks for the design of reversible 8x8 Wallace tree multiplier. The generation of all partial products of the multiplication can be done in parallel by using Fredkin gates (for ANDing the bits of the multiplier and multiplicand) as shown in Figure 6-a. Then the addition of partial products is performed using reversible Wallace tree. The Wallace tree uses reversible 4:2 compressors, full adders and half adders designed from TSG gate. Figure 6-b shows the proposed reversible 8x8 Wallace tree multiplier in which (R 4:2) represents reversible 4:2 compressor. In Stage 1, the partial products are added using 4:2 compressors, full adders and half adders, the S and C generated of all the blocks are arranged according to their weights. In the Stage 2, the reduced partial products are again added using 4:2 compressors, full adders and half adders. Finally, the result obtained in Stage 2 is finally added using a parallel adder designed from TSG gates to generate the product bits P0...P14, P15.

B. Evaluation of the Proposed Wallace Tree Multiplier

The proposed reversible 8x8 Wallace Tree is designed from reversible TSG gate. This is the first attempt in literature to design the reversible 8x8 Wallace Tree multiplier. The novelty lies in the introduction of reversible TSG gate and its implementation for designing the adder and compressor, which are later used to design the reversible Wallace tree multiplier. The proposed reversible architecture of the multiplier can be improved further by implementing block 32 in the architecture (Figure 6-b) with the efficient parallel adder architectures proposed in [23-24]. There seems to be no existing counterpart in literature and hence no comparative study is done. It has already been proved in the earlier sections that the adder and compressor designed from the TSG gate are the most optimized one, thus making the overall architecture of the Wallace tree multiplier as the most optimal one.

V. CONCLUSIONS

The focus of this paper is the application of a new reversible 4*4 TSG gate to design the components of a primitive quantum/reversible ALU. The novel optimized adder and 4:2 compressor are designed from TSG gate, which are later used to design the novel 8x8 reversible Wallace tree multiplier. It is proved that the adder, 4:2 compressor and multiplier architectures designed with the proposed TSG gate are better than their existing counterparts, in terms of number of reversible gates and garbage outputs, leading to a high speed and low power reversible circuits. All the proposed architectures are analyzed in terms of technology independent implementations. The proposed circuit can be used for designing large reversible systems. Thus, this paper provides the initial threshold to build more complex reversible systems.

REFERENCES

[1] R. Landauer, “Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development, 5, pp. 183-191, 1961.
[2] C.H. Bennett, “Logical Reversibility of Computation”, IBM J. Research and Development, pp. 525-532, November 1973.
[3] E. Fredkin, T Toffoli, “Conservative Logic”, International Journal of Theor. Physics, 21(1982),pp.219-253.
[4] T. Toffoli, “Reversible Computing”, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).
[5] Alberto LEPORATI, Claudio ZANDRON, Giancarlo MAURI," Simulating the Fredkin Gate with Energy-Based P Systems", Journal of Universal Computer Science, Volume 10, Issue 5,p.600-619.
[6] Md. M. H Azad Khan, “Design of Full-adder With Reversible Gates”, International Conference on Computer and Information Technology, Dhaka, Bangladesh, 2002, pp. 515-519.
[7] Hafiz Md. Hasan Babu, Md. Rafiquel Islam, Syed Mostahed Ali Chowdhury and Ahsan Raja Chowdhury, “Reversible Logic Synthesis for Minimization of Full Adder Circuit”, Proceedings of the EuroMicro Symposium on Digital System Design (DSD'03), 3-5 September 2003, Belek- Antalya, Turkey, pp-50-54.
[8] Hafiz Md. Hasan Babu, Md. Rafiquel Islam, Syed Mostahed Ali Chowdhury and Ahsan Raja Chowdhury,” Synthesis of Full-Adder Circuit Using Reversible Logic”,Proceedings 17th International Conference on VLSI Design (VLSI Design 2004), January 2004, Mumbai, India, pp-757-760.
[9] J.W. Bruce, M.A. Thornton.L. Shivakumarah, P.S. Kokate and X.Li, “Efficient Adder Circuits Based on a Conservative Logic Gate”, Proceedings of the IEEE Computer Society Annual Symposium on VLSI(ISVLSI'02),April 2002, Pittsburgh, PA, USA, pp. 83-88.
[10] G Schrom, “Ultra Low Power CMOS Technology”, PhD Thesis, Technischen Universitat Wien, June 1998.
[11] E. Knill, R. Laflamme, and GJ Milburn, “ A Scheme for Efficient Quantum Computation With Linear Optics”, Nature, pp 46-52, Jan 2001.
[12] M. Nielsen and I. Chuang, “Quantum Computation and Quantum Information”, Cambridge University Press, 2000.
[13] R.C. Merkle, “Two Types of Mechanical Reversible Logic”, Nanotechnology,4:114-131,1993.
[14] Vlatko Vedral, Adriano Barenco and Artur Ekert, “ Quantum Networks for Elementary Arithmetic Operations”, arXiv:quant-ph/9511018 v1, nov 1995.
[15] Hafiz Md. Hasan Babu and Ahsan Raja Chowdhury, “Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-Bit Parallel Adder”, 18th International Conference on VLSI Design (VLSI Design 2005), January 2005, Kolkata, India, pp-255-260.
[16] A. Weinberger, “4:2 Carry-Save Adder Module”, IBM Technical DisclosureBulletin, Vol.23, January 1981.

[17] V.G. Oklobdzija, D. Villegier, S. S. Liu, “A Method for Speed Optimized Partial Product Reduction and Generation of Fast Parallel Multipliers Using and Alghorimtic Approach”, IEEE Transaction on Computers, Vol. 45, No 3, March 1996.

[18] P. Stelling, C. Martel, V. G. Oklobdzija, R. Ravi, “Optimal Circuits for Parallel Multipliers”; IEEE Transaction on Computers, Vol. 47, No.3, pp. 273-285, March, 1998.

[19] C.S. Wallace, “A Suggestion for a Fast Multiplier”, IEE Transactions on Electronic Computers, EC-13, p.14-17, 1964.

[20] Niichi Itoh, Yuka Naemura, Hiroshi Makino, Yasunobu Nakase, “A Compact 54x54 Multiplier with Improved Wallace-Tree Structure”, 1999 Symposium on VLSI Circuits Digest of Technical Papers.

[21] Niichi Itoh, Yuka Naemura, Hiroshi Makino, Yasunobu Nakase, Tsutomu Yoshihara, and Yasutaka Horiba, “A 600-MHz 54 x 54-bit Multiplier with Rectangular-Styled Wallace Tree”, JSSC, vol.36, no. 2, February 2001.

[22] M. P. Frank, “Introduction to reversible computing: motivation, progress, and challenges”; In Proceedings of the 2nd Conference on Computing Frontiers, pages 385–390, 2005.

[23] Himanshu Thapliyal and M.B Srinivas, “A New Reversible TSG Gate and Its Application For Designing Efficient Adder Circuits”, 7th International Symposium on Representations and Methodology of Future Computing Technologies(RM 2005), Tokyo, Japan, September 5-6, 2005.

[24] Himanshu Thapliyal and M.B Srinivas, “Novel Reversible “TSG” Gate and Its Application for Designing Reversible Carry Look Ahead Adder and Other Adder Architectures”. Tenth Asia-Pacific Computer Systems Architecture Conference (ACSAC05), Singapore, October 24 - 26, 2005(Accepted).

[25] V. Oklobdzija, “High-Speed VLSI Arithmetic Units: Adders and Multipliers”, in "Design of High-Performance Microprocessor Circuits", Book Chapter, Book edited by A. Chandrakasan, IEEE Press, 2000.