A high gain V-band power amplifier for 5G applications

Xiaojian Zhu¹, Runxi Zhang¹, ², and Chunqi Shi¹

Abstract This paper presents a high gain millimeter-wave (mmW) power amplifier (PA) fabricated in a 55 nm CMOS technology for V-band 5G wireless communication applications. An accurate magnetically-coupled-resonator (MCR) analysis and evaluation method is proposed to capture the MCR characteristics and optimize PA gain and bandwidth. A low-loss-matching-resonator (LLMR) technology is developed to enhance power gain and efficiency. The PA achieves a peak gain of 21.1 dB at 67 GHz with a 3 dB bandwidth (BW) of 10 GHz. At 67 GHz, the measured saturated output power (P₁dB) and output 1 dB compression point (OIP₃dB) are 13.9 dBm, 9.7 dBm and 11.8%, respectively.

Keywords: millimeter-wave (mmW), V-band, high gain, magnetically-coupled-resonator (MCR), low-loss-matching-resonator (LLMR), power amplifier (PA)

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The increasing demand for high-speed data transmission in wireless communication applications justifies the mmW as a critical technology for 5G deployment due to its low latency and large available bandwidth [1, 2]. One of design challenges in mmW fully-integrated transceiver is to realize a high gain and high efficiency power amplifier (PA), while exploiting CMOS transistors with limited $f_t$ and $f_{max}$ [3, 4, 5, 6, 7, 8]. Recently, the WRC-19 meeting has identified 45.5–50.2 GHz, 50.4–52.6 GHz, 66–76 GHz, and 81–86 GHz frequency bands as the candidate frequencies for the next-generation wireless communications [9]. Among them, the largest bandwidth is the 66–76 GHz located in the V-band, which can supply the largest spectrum resources and theoretically obtain the highest transmission data rate [10].

In [11], a two-stage common source (CS) 60 GHz PA is proposed using a 65 nm CMOS process and achieves a 29% peak PAE and a 12 GHz BW at 77 GHz peak gain. In [12], a four-stage CS 94 GHz PA with a peak PAE of 10.2%, a $P_{sat}$ of 10.6 dBm and a signal peak gain of 12 dB is implemented. The achieved gains in [11] and [12] are both limited due to the cascode inter-stage parasitic problem, their peak gain are less than 18 dB.

In [13], a three-stage CS PA is developed with a peak PAE and a $P_{sat}$ of 14 dB and 3 dBm power gain. However, due to the lack of dealing with the cascode inter-stage parasitic problem, their peak gain are both less than 18 dB.

2. Circuit design

2.1 Accurate magnetically-coupled-resonator design

Fig. 1 shows schematic and layout of the proposed high gain V-band PA. The multi-stage structure is used in mmW PA to simultaneously achieve high gain, wide bandwidth and high efficiency performance. In general, there are two methods for inter-stage matching: the passive LC network and the magnetically-coupled transformer network. In [15], a three-stage CS PA is developed with a 17 dB peak gain. Due to the adoption of the LC matching network, it only obtains 3 GHz bandwidth at 77 GHz carrier frequency. Thus, in order to enhance PA bandwidth, the transformer-based coupling method has become the mainstream design [16, 17, 18].

In high frequency V-band PA design, for example, if adopting a 76 $\mu$m/60 nm power cell transistor, there is a significant parasitic capacitance on the transistor drain terminal which will obviously influence the magnetically-coupled-resonator (MCR) transimpedance response. Figs. 2(a) and (b) illustrate the traditional transformer independent simulation (TIS) scheme and the proposed MCR in-situ simulation (ISS) method. In the ISS method, the transformer is regarded as a two-port network and an ideal current source of the PA to achieve a 15% peak PAE, a 13 dBm $P_{sat}$ and a 13 dB power gain. However, due to the lack of dealing with the cascode inter-stage parasitic problem, their peak gain are both less than 18 dB.

Fig. 1 Schematic and layout of the proposed high gain V-band PA.

1 Institute of Microelectronic Circuits and Systems, East China Normal University, Shanghai, 200241, China

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In order to guide the V-band PA design, a theoretical analysis of $|Z_{21}|$ is described as follows. Taking the inter-stage MCR as an example, Fig. 4(a) shows its equivalent model. The input and output impedance can be expressed as [19]

$$ Z_{in} = R_1 + sL_1 + \frac{\omega^2 M^2}{R_2 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} + sL_2 - \frac{sR_{ds}^2 C_s}{1 + \omega^2 C_s R_L} $$

(1)

$$ Z_{out} = R_2 + sL_2 + \frac{\omega^2 M^2}{R_1 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} + sL_1 - \frac{sR_{ds}^2 C_s}{1 + \omega^2 C_s R_L} $$

(2)

If the quality factors of the primary and secondary coils are high (> 18 in this design), the quality factors of the input and output LC tanks are $\omega C_s R_L = R_c(C_s/L_1)^{1/2}$ and $\omega C_L R_L = R_c(C_L/L_2)^{1/2}$, respectively.

$$ sL_1 \approx \frac{sR_{ds}^2 C_s}{1 + \omega^2 C_s^2 R_L^2} $$

(3)

$$ sL_2 \approx \frac{sR_{ds}^2 C_L}{1 + \omega^2 C_s^2 R_L^2} $$

(4)

The input and output impedance can be simplified as

$$ Z_{in} = R_1 + sL_1 + \frac{\omega^2 M^2}{R_2 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} $$

(5)

$$ Z_{out} = R_2 + sL_2 + \frac{\omega^2 M^2}{R_1 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} $$

(6)

$$ R_{in} = Re(Z_{in}) = R_1 + \frac{\omega^2 M^2}{R_2 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} $$

(7)

$$ R_{out} = Re(Z_{out}) = R_2 + \frac{\omega^2 M^2}{R_1 + \frac{R_{ds}}{1 + \omega^2 C_s R_L}} $$

(8)

where $R_1$ and $R_2$ are the serial loss resistances of $L_1$ and $L_2$, $M$ is the mutual inductance between $L_1$ and $L_2$. According to Fig. 4(b), the relationship between $I_{sin}$ and $I_1$ can be calculated as

$$ I_1 = \frac{-I_{sin}}{s^2 L_1 C_s + sR_{in} C_S + \frac{R_{in}}{R_S} + 1 + \frac{sL_1}{R_S}} $$

(9)

According to Fig. 4(c), the output current of $I_2$ can be calculated as

$$ I_2 = \frac{s M I_1}{Z_L + R_{out} + sL_2} $$

(10)

the $|Z_{21}|$ of the inter-stage MCR is calculated as

$$ \frac{V_{out}}{I_{sin}} = \frac{1}{s^2 L_1 C_s + sR_{in} C_S + \frac{R_{in}}{R_S} + 1 + \frac{sL_1}{R_S}} $$

(11)
and then, two poles produced by the primary coil are

\[
p_{1,2} = \frac{R_{in} C_S + \frac{L_C}{R_{in}}}{2L_1 C_1} + \frac{\left(\frac{R_{in} C_S + \frac{L_C}{R_{in}}}{2L_1 C_1}\right)^2 - 1 + \frac{R_{in} C_S + \frac{L_C}{R_{in}}}{2L_1 C_1}}{L_1 C_1}
\]

In order to explain the relationship between \( L_1, C_S \) and poles clearly, we simplify the average value of two poles as

\[
p_{\text{mean}1} = \frac{p_1 + p_2}{2} = -\frac{R_{in} C_S + \frac{L_C}{R_{in}}}{2L_1 C_1}
\]

two poles from the secondary coil can be expressed as

\[
p_{3,4} = -\frac{R_{out} C_L + \frac{L_L}{R_{out}}}{2L_2 C_2} + \frac{\left(\frac{R_{out} C_L + \frac{L_L}{R_{out}}}{2L_2 C_2}\right)^2 - 1 + \frac{R_{out} C_L + \frac{L_L}{R_{out}}}{2L_2 C_2}}{L_2 C_2}
\]

here, \( p_{\text{mean}1} \) is a function of \( L_1, R_{in}, R_S \) and \( C_S \), while \( p_{\text{mean}2} \) is a function of \( L_2, R_{out}, R_L \) and \( C_L \). \( C_S \) is the parasitic capacitance at the first stage transistor drain terminal and \( C_L \) is the parasitic capacitance at the second stage transistor gate terminal. The MCR resonating peak can be dynamically adjusted through changing \( L_1, L_2 \) and the mutual inductance of \( M \). In this V-band PA design, the driver stage transistor size is roughly half of the power stage. Thus, \( C_L = 2C_S \) is a typical situation. As shown in Fig. 5, the main resonating peaks of the input balun, the output balun and the inter-stage transformer are used to realize an overall broadband frequency response.

In order to achieve a good input impedance matching, the coil diameter of the input balun is selected as 38 \( \mu m \) and it resonates at 69 GHz. The output balun coil diameter is 50 \( \mu m \) to resonate at a relatively lower frequency of 62 GHz. It also realizes the optimal load impedance transformation to obtain the maximum gain and power efficiency. The inter-stage transformer is composed of a small coil diameter of 34 \( \mu m \) and a long-line inductor to implement the high impedance conversion ratio with a 68 GHz resonating frequency. As shown in Fig. 5, the simulated overall resonating peak of PA is 68 GHz, it highly agrees with the measured S21 results.

2.2 Low-loss-matching-resonator (LLMR) technology

Compared with the CS topology, the cascode structure exhibits excellent performance by effectively suppressing the Miller effect and improving the output impedance, while achieving a better input and output isolation and signal gain. However, as shown in Fig. 6(b), there are two parasitic capacitances of \( C_1 \) and \( C_2 \) at the cascode inter-stage node which will significantly deteriorate the high frequency mmW PA power gain. In order to alleviate the parasitic effect of \( C_1 \) and \( C_2 \), two layout-optimized common source (CS) and common gate (CG) mmW transistors are proposed. For the CS transistor, the top copper metal (Metal11) with the lowest resistivity is used to connect the drain and the gate to reduce \( C_{GS} \) and \( C_{DS} \). The large-sized transistor is split into 2 parallel 38 \( \mu m/60 \) nm transistors to decrease the gate series resistance and enhance \( f_{MAX} \). Two bottom layers of Metal1 and Metal2 are used to form a large-area mesh grid to reduce the source parasitic resistance and inductance. In the CG transistor, the source and drain terminals are connected to the top metal from both sides to reduce the parasitic resistance and the parasitic capacitance of \( C_{SB} \). The optimized transistor is extracted using Calibre xACT-3D and the top metal interconnection line is modeled by ADS Momentum to improve design accuracy. As shown in Figs. 7(a) and (b), the simulation results show that the \( f_{MAX} \) and \( f_T \) of the layout-optimized CS transistor are 14.2% and 14.6% higher than those of the transistor provided by foundry PDK, respectively.

The serial inductor of \( L_1 \) is commonly used to eliminate parasitic capacitance in the cascode topology [20, 21]. As shown in Fig. 8(a), the current flowing through M2 and the input impedance of \( Z_s \) can be expressed as

\[
I_{out} = I_{in} \times \left(\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + \frac{1}{j\omega C_3}\right)
\]

Fig. 5  The simulated \(|Z_{21}|\) of the input balun, the output balun and the inter-stage transformer using the proposed in-situ simulation (ISS) method and the measured S21 result.

Fig. 6  (a) The common gate (CG) layout-optimized transistor (LOT), (b) the cascode topology, and (c) the common source (CS) layout-optimized transistor.

Fig. 7  The simulated (a) \( G_{MAX} \) and (b) \( H_{21} \) of the proposed layout-optimized CS transistor and the PDK transistor.
area is 720 mm\(^2\) PA fabricated in a 55 nm CMOS process. The core

\[ Z_x = \frac{1}{g_m \left(1 + \frac{\omega^2 C_1^2}{g_m^2}\right)} + \frac{1}{\omega C_2 \left(1 + \frac{g_m^2}{\omega^2 C_2^2}\right)} + j\omega L_1 + R_{L1} \]  

(17)

where \(R_{L1}\) is the series loss resistance of \(L_1\). When \(L_1\) and \(C_2\) resonating, the impedance of \(Z_x\) can be decreased. It can increase the current flowing through \(Z_x\) and M2. The impedance of \(Z_x\) can be expressed as

\[ Z_x = \frac{1}{g_m \left(1 + \frac{\omega^2 C_1^2}{g_m^2}\right)} + R_{L1} \]  

(18)

If \(L_1\) is lossless, the quality factor of LC-tank and the impedance of \(Z_x\) can be expressed as

\[ Q = \frac{1}{\omega C_2 \left(1 + \frac{g_m^2}{\omega^2 C_2^2}\right)} \left(1 + \omega^2 C_1^2 \right) \]  

(19)

\[ Z_x = \frac{1}{g_m \left(1 + \frac{\omega^2 C_1^2}{g_m^2}\right)} = \frac{1}{g_m (1 + Q^2)} \]  

(20)

Due to the reduction of \(Z_x\), the current flowing through M2 will increase. However, \(L_1\) is not lossless. So \(C_1\) will still shunt part of signal current. From the perspective of impedance matching, since the output resistance of M1 is \(r_o\) and the input resistance of M2 is \(1/g_m\), there is a big difference between them. In the traditional \(\pi\)-type matching network, \(C_1\) and \(C_2\) are definite and decided by CS and CG transistor sizes. It is difficult to realize the impedance matching only through controlling \(L_1\). Fig. 8(b) shows the proposed low-loss-matching-resonator (LLMR) network. Besides the serial inductor of \(L_1\), a parallel differential inductor of \(L_2\) is used to resonate with the parasitic capacitance of \(C_1\) to reduce the current loss further. In addition, in order to alleviate the parasitic effect of \(C_{GD}\) and improve gain and stability, a capacitive neutralization is also adopted. As illustrated in Figs. 9(a) and (b), the PA simulation result shows that through using the proposed LLMR composed of the serial inductor of \(L_1\), the differential inductor of \(L_2\) and the layout-optimized CS and CG transistors, the peak gain and the \(PAE_{MAX}\) are improved by 5 dB and 3.2%, respectively.

3. Measurement Results

Fig. 10 shows the chip photograph of the proposed V-band mmW PA fabricated in a 55 nm CMOS process. The core area is 720 \(\mu m \times 160 \mu m\). The power supply is 2.5 V and the PA consumes 80 mA when the CS transistor bias voltage is 0.8 V and the CG transistor bias voltage is 2.1 V, respectively. Fig. 11(a) summarizes the simulated and the measured S-parameters. The PA achieves a peak gain of 21.1 dB at 67 GHz with a BW\(-3dB\) of 10 GHz, a S11 < -7 dB from 66 to 76 GHz and a S22 < -10 dB from 62 to 80 GHz. The S12 is less than -50 dB across the entire frequency range. Good agreement between the simulation and the measurement results is achieved while combining the accurate MCR design method and the LLMR technology. Fig. 11(b) shows the measured large signal performance. At 67 GHz, it realizes a \(P_{sat}\) of 13.9 dBm, an \(OP_{1dB}\) of 9.7 dBm and a peak PAE of 11.8%. Table I [11, 12, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31] summarizes the proposed PA performance and compare it with prior works. The FOM1 evaluates PA performance by the saturated output power (\(P_{sat}\)), gain, the peak power-added efficiency (\(PAE_{MAX}\)) and the working frequency (\(f_c\)). Compared to the FOM1, the FOM2 takes the fractional 3 dB bandwidth (FWB) into consideration. The proposed PA achieves a good FOM1 and FOM2.
Table 1 Performance summary and comparison with the state-of-the-art wideband mmW PAs.

| Reference | Technology  | Freq. (GHz) | BW_3dB (GHz) | FBW (%) | $P_{sat}$ (dBm) | $P_{sat}$ (dBm) | Gain (dB) | PAE_{MAX} (%) | FOM1 | FOM2 |
|-----------|-------------|-------------|--------------|---------|----------------|----------------|-----------|---------------|------|------|
| [11] WMCS’2019 | 65 nm CMOS | 62 | 12 | 19.35 | / | 10.5 | 14 | 29 | 74.97 | 64.85 |
| [12] TCAS-I’2017 | 65 nm CMOS | 94 | 16 | 17 | 9.2 | 10.6 | 12 | 10.2 | 72.1 | 57.3 |
| [22] RFIC’2017 | 14 nm FinFET | 71 | 7.4 | 10.4 | 2 | 7.4 | 16.7 | 8.9 | 70.6 | 53.9 |
| [23] JSSC’2015 | 28 nm CMOS | 53 | 27 | 50.9 | 12 | 13.3 | 13 | 16 | 72.82 | 72.47 |
| [24] APMC’2017 | 90 nm CMOS | 53.2 | 4 | 7.5 | 13.36 | 17.7 | 16.9 | 78.28 | 61.27 |
| [25] TCAS-II’2019 | 40 nm CMOS | 120 | 38.5 | 32 | 9.3 | 14.6 | 16 | 9.4 | 81.9 | 70.4 |
| [26] JSSC’2019 | 90 nm CMOS | 75 | 24 | 32 | 5.7 | 12.8 | 16.6 | 26.3 | 81.1 | 73.7 |
| [27] IMS’2018 | 45 nm SOI | 68 | 28 | 41.2 | 15 | 18 | 12 | 20 | 79.7 | 75.3 |
| [28] TMTT 2018 | 65 nm CMOS | 60 | 17 | 28.3 | 18.7 | 21.8 | 8.7 | 12.4 | 77 | 70.5 |
| [29] MWCL 2018 | 45 nm SOI | 56 | 12.5 | 22.3 | 16.2 | 18.5 | 15 | 25.5 | 82.5 | 69.5 |
| [30] IEICE 2017 | 65 nm CMOS | 57 | 13 | 22.8 | / | 14.9 | 11 | 16.3 | 73.1 | 65.1 |
| [31] IECE 2020 | 65 nm CMOS | 115 | 21 | 18.2 | 8.7 | 13 | 11.5 | 14.7 | 77.3 | 61.37 |

This work: 55 nm CMOS | 67 | 10 | 14.9 | 9.7 | 13.9 | 21.1 | 11.8 | 82.2 | 69.1 |

**FOM1** = $P_{sat}$ (dBm) + Gain (dB) + 10log(PAE_{MAX} (%) + 20log(fo [GHz]).

**FOM2** = $P_{sat}$ (dBm) + Gain (dB) + 10log(PAE_{MAX} (%) + 20log(FBW_{b50} [GHz]).

Fig. 11 (a) The measured and simulated S-parameters and (b) the measured output power and PAE at 62 GHz, 67 GHz and 72 GHz.

### 4. Conclusion

This paper presents a high gain mmW PA fabricated in a 55 nm CMOS process for V-band 5G wireless communication applications. The magnetically-coupled-resonator (MCR) analysis and evaluation method has been developed to improve the design accuracy of the input balun, the output balun and the inter-stage transformer and optimize PA gain and bandwidth. The low-loss-matching-resonator (LLMR) technology has been proposed to improve PA gain and efficiency. The proposed PA achieves a peak gain of 21.1 dB, a BW_3dB of 10 GHz, a $P_{sat}$ of 13.9 dBm and a peak PAE of 11.8% at 67 GHz while consuming 80 mA current from 2.5 V power supply.

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### References

[1] K. Kang, et al.: “A 60 GHz OOK receiver with an on-chip antenna in 90 nm CMOS,” IEEE J. Solid-State Circuits 45 (2010) 1720 (DOI: 10.1109/JSSC.2010.2053095).

[2] D. Chen, et al.: “A V-band inverse class F power amplifier with 16.3% PAE in 65 nm CMOS,” IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT) (2016) 55 (DOI: 10.1109/ICMMT.2016.7761675).

[3] T. Suzuki, et al.: “60 and 77 GHz power amplifiers in standard 90 nm CMOS,” 2008 IEEE International Solid-State Circuits Conference (ISSCC) (2008) 562 (DOI: 10.1109/ISSCC.2008.4523307).

[4] C.Y. Law, et al.: “A high-gain 60 GHz power amplifier with 20dBm output power in 90 nm CMOS,” 2010 IEEE International Solid-State Circuits Conference (ISSCC) (2010) 426 (DOI: 10.1109/ISSCC.2010.5433882).

[5] B. Park, et al.: “Highly linear mm-wave CMOS power amplifier,” IEEE Trans. Microw. Theory Techn. 64 (2016) 4535 (DOI: 10.1109/TMTT.2016.262706).

[6] J. Tsai, et al.: “A 69–81 GHz power amplifier using 90 nm CMOS technology,” IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (2014) 77 (DOI: 10.1109/SIRF.2014.6828515).

[7] K-L. Wu, et al.: “77–110 GHz 65 nm CMOS power amplifier design,” IEEE Trans. THz Sci. Technol. 4 (2014) 391 (DOI: 10.1109/THZH.2014.2315451).

[8] J-L. Lin, et al.: “A K-band transformer based power amplifier with 24.4-dBm output power and 28% PAE in 90 nm CMOS technology,” IEEE MTTS International Microwave Symposium (IMS) (2017) 31 (DOI: 10.1109/MWSYM.2017.8059113).

[9] W-J. Lin, et al.: “A 67–86 GHz spectrum-efficient CMOS transmitter supporting 1024-QAM with a process-variation-tolerant de-
[10] Y. Li, et al.: “Radio resource management considerations for 5G millimeter wave backhaul and access networks,” IEEE Commun. Mag. 55 (2017) 56 (DOI: 10.1109/MCOM.2017.1601118).

[11] S. Huang, et al.: “A 60GHz CMOS power amplifier with parametric matching networks,” IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS) (2019) 1 (DOI: 10.1109/WMCAs.2019.8732546).

[12] Y. Lin, et al.: “94-GHz CMOS power amplifiers using miniature dual Y-shaped combiner with RL load,” IEEE Trans. Circuits Syst. I, Reg. Papers 64 (2017) 1285 (DOI: 10.1109/TCSI.2017.2684488).

[13] U. Çelik, et al.: “An E-band compact power amplifier for future array-based backhaul networks in 22 nm FD-SOI,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2019) 187 (DOI: 10.1109/RFIC.2019.8701866).

[14] B. Moret, et al.: “60GHz highly reliable power amplifier with 13dBm P_{sat} 15% peak PAE in 65 nm CMOS technology,” IEEE 15th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (2015) 58 (DOI: 10.1109/SIRF.2015.719874).

[15] Y. Hamada, et al.: “A high gain 77 GHz power amplifier operating at 0.7 V based on 90 nm CMOS technology,” IEEE Microw. Wireless Compon. Lett. 19 (2009) 329 (DOI: 10.1109/LMWC.2009.2017613).

[16] C. Chou, et al.: “A 60-GHz 20.6-Bm symmetric radial-combining wideband power amplifier with 20.3% peak PAE and 20-dB gain in 90-nm CMOS,” IEEE MTT-S International Microwave Symposium (IMS) (2016) 1 (DOI: 10.1109/MWSYM.2016.7540028).

[17] C.-W. Wang, et al.: “A 20.8-41.6-GHz transformer-based wideband power amplifier with 20.4-dB peak gain using 0.9-V 28-nm CMOS process,” IEEE/MTT-S International Microwave Symposium (IMS) (2020) 1323 (DOI: 10.1109/IMS30576.2020.9223905).

[18] P. Pahl, et al.: “A 50 to 146 GHz power amplifier based on magnetic transformers and distributed gain cells,” IEEE Microw. Wireless Compon. Lett. 25 (2015) 615 (DOI: 10.1109/LMWC.2015.2456639).

[19] A. Charles and S. Matthew: Fundamentals of Electric Circuits (McGraw-Hill, New York, 2012) 5th ed. 569.

[20] Z. Xu, et al.: “A W-band current combined power amplifier with 14.8dBm P_{sat} and 9.4% maximum PAE in 65nm CMOS,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2011) 1 (DOI: 10.1109/RFIC.2011.5940619).

[21] Y. Chai, et al.: “Design of a 60-GHz receiver front-end with broadband matching techniques in 65-nm CMOS,” IEICE Electron. Express 15 (2018) 20180935 (DOI: 10.1587/exelx.15.20180935).

[22] S. Callender, et al.: “A 73GHz PA for 5G phased arrays in 14nm FinFET CMOS,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2017) 402 (DOI: 10.1109/RFIC.2017.7969103).

[23] M. Bassi, et al.: “A 40–67 GHz power amplifier with 13 dBm P_{sat} and 16% PAE in 28 nm CMOS LP,” IEEE J. Solid-State Circuits 50 (2015) 1618 (DOI: 10.1109/JSSC.2015.2409295).

[24] J.-C. Chen, et al.: “A transformer-coupled power amplifier in 90-nm CMOS process for V-band applications,” IEEE Asia Pacific Microwave Conference (APMC) (2017) 318 (DOI: 10.1109/APMC.2017.8251443).

[25] H.S. Son, et al.: “Pole-controlled wideband 120 GHz CMOS power amplifier for wireless chip-to-chip communication in 40-nm CMOS process,” IEEE Trans. Circuits Syst. II, Exp. Briefs 66 (2019) 1351 (DOI: 10.1109/TCSI.2018.2880308).

[26] S. Callender, et al.: “An E-band power amplifier with 26.3% PAE and 24-GHz bandwidth in 22-nm FinFET CMOS,” IEEE J. Solid-State Circuits 54 (2019) 1266 (DOI: 10.1109/JSSC.2019.2899493).

[27] K. Ning, et al.: “An 14-dBm, 57 to 85-GHz, 4-stack FET power amplifier in 45-nm SOI CMOS,” IEEE/MTT-S International Microwave Symposium (IMS) (2018) 1453 (DOI: 10.1109/MWSYM.2018.8439649).

[28] C.-W. Wu, et al.: “Design of an 60-GHz high-output power stacked-FET power amplifier using transformer-based voltage-type power combing in 65-nm CMOS,” IEEE Trans. Microw. Theory Techn. 66 (2018) 4595 (DOI: 10.1109/TMTT.2018.2859980).

[29] J. Xia, et al.: “60-GHz power amplifier in 45-nm SOI-CMOS using stacked transformer-based parallel power combiner,” IEEE Microw. Wireless Compon. Lett. 28 (2018) 711 (DOI: 10.1109/LMWC.2018.2843160).

[30] D. Chen, et al.: “A wideband high efficiency V-band 65 nm CMOS power amplifier with neutralization and harmonic controling,” IEICE Electron. Express 14 (2017) 20171110 (DOI: 10.1587/exle.14.20171110).

[31] J. Pan, et al.: “A D-band CMOS power amplifier for short-range data center communication,” IEICE Electron. Express 17 (2020) 20200159 (DOI: 10.1587/exle.17.20200159).