We propose and numerically analyze novel reconfigurable logic gates using "single-electron spin transistors" (SESTs), which are single-electron transistors (SETs) with ferromagnetic electrodes and islands. The output characteristics of a SEST depend on the relative magnetization configuration of the ferromagnetic island with respect to the magnetization of the source and the drain, i.e., high current drive capability in parallel magnetization and low current drive capability in antiparallel magnetization. The summation of multiple input signals can be achieved by directly coupling multiple input gate electrodes to the SEST island, without using a floating gate. A Tucker-type inverter with a variable threshold voltage, a reconfigurable AND/OR logic gate, and a reconfigurable logic gate for all symmetric Boolean functions are proposed and simulated using the Monte Carlo method. [DOI: 10.1143/JJAP.46.6579]

KEYWORDS: reconfigurable logic, spin transistor, single electron transistor, Coulomb blockade (CB), tunneling magnetoresistance (TMR)

1. Introduction

Using the spin degree of freedom in active semiconductor devices and integrated circuits is one of the most attractive new directions in spintronics research. Recently, we have proposed a new spin metal–oxide–semiconductor field-effect transistor (spin MOSFET), consisting of a MOS gate structure and half-metallic-ferromagnet contacts for the source and drain. We also proposed novel spintronic reconfigurable logic gates employing spin MOSFETs. We showed that all symmetric Boolean gates (AND, OR, XOR, NAND, NOR, XNOR, all-"0", and all-"1") could be realized using only five complementary MOS (CMOS) inverters including four spin MOSFETs. The functions of these circuits are nonvolatile and can be changed by changing the magnetization configurations of spin MOSFETs. This example shows the possibility of using the spin degree of freedom in active devices.

In this study, we propose a new kind of reconfigurable logic design using “single-electron spin transistors” (SESTs), by which we can realize the analog input without using a floating gate. Figure 1 shows the schematic device structure and circuit notation of a SEST. The structure is similar to that of a single-electron transistor (SET), which exploits the Coulomb blockade (CB) effect to switch the tunneling electric current. The difference is that we use a ferromagnetic (FM) material for the island and electrodes for the SEST. This is possible because we use a ferromagnetic (FM) material for the island and electrodes for the SEST. The magnetization directions of the electrodes are fixed and maintained parallel to each other, whereas the magnetization of the island is reversible. Using the tunneling magnetoresistance (TMR) effect between the electrodes and the island, we can control the output current of the SEST by changing the magnetization direction of the island. When the magnetization of the island is parallel to that of the drain and the source electrode (parallel configuration; P), the tunneling resistances \( R_{1,P} \) and \( R_{2,P} \) are small; thus, the output current (drain current) is large. On the other hand, when the magnetization of the island is antiparallel to that of the drain and the source electrode (antiparallel configuration; AP), the tunneling resistances \( R_{1,AP} \) and \( R_{2,AP} \) are large; thus, the output current is small. Except for the TMR effect, the operating principle of the SEST is basically the same as that of the SET. The summation of the multiple input signals can be achieved by directly coupling the multiple input gate electrodes to the SEST islands, without using a floating gate. This is possible because the electrical characteristics of the SEST are determined by the total number of electrons on the counter electrodes of the island. This advantage, as well as the initial ultrasmall size of the SEST, makes circuits easy to be scaled down. Another advantage of the SEST is its high magnetico-current ratio, which originates from the tunneling nature of the drain–source current.

In the following sections, we show the operation principle of a SEST, and then we present reconfigurable logic designs.
using SESTs; a Tucker-type inverter with a variable threshold voltage, a reconfigurable AND/OR logic gate, and a reconfigurable logic gate for two-input all symmetric Boolean functions. We show that these circuits can be designed using just four SESTs and six SETs without any floating gates. We theoretically analyze and show the operation of these reconfigurable logic gates by Monte Carlo simulations.4)

2. Operation of Single SEST

In this section, we show the calculated operating characteristics of a SEST. The parameters used in the calculations are \( C_1 = 9.9 \text{ aF}, \ C_2 = 0.1 \text{ aF}, \ C_3 = 0.1 \text{ aF}, \ R_{1,P} = 9.9 \text{ M\Omega}, \ R_{1,AP} = 60.8 \text{ M\Omega}, \ R_{2,P} = 0.1 \text{ M\Omega}, \ R_{2,AP} = 0.95 \text{ M\Omega}, \text{ and } T = 0.01e^2/(C_1 + C_2 + C_3)k_B = 0.92 \text{ K}. \) Here, \( C_1, C_2, \text{ and } C_3 \) are the capacitances of the first tunnel junction, second tunnel junction, and gate electrode with respect to the island, respectively, as shown in Fig. 1; \( T \) is the temperature and \( k_B \) is the Boltzmann’s constant. Details of the calculation are shown in Appendix A.

Figure 2 shows \( I_{ds} - V_{ds} \) and \( I_{ds} - V_{gs} \) characteristics at different magnetization configurations of a SEST, where \( I_{ds}, V_{ds}, \text{ and } V_{gs} \) are the drain–source current, drain–source voltage, and gate–source voltage, respectively. The \( I_{ds} - V_{ds} \) characteristics show Coulomb gaps and the \( I_{ds} - V_{gs} \) characteristics show Coulomb oscillations, similarly to those of a SET. Step-like features called Coulomb staircases also appear clearly in Fig. 2(a) due to the strong asymmetry of the chosen parameters between the source-island and the island–drain tunnel junctions.5) Both the \( I_{ds} - V_{ds} \) and \( I_{ds} - V_{gs} \) characteristics have large output currents in P magnetization and low output currents in AP magnetization, as expected. The oscillating currents in Fig. 2(b) can be shifted along the \( V_{gs} \) axis by applying a voltage on the control gate coupled to the island through the control capacitor.5) This ability allows us to design the function of SEST as an n-type transistor or a p-type transistor by simply adjusting the voltage of the control gate.

We emphasize that the TMR effect is not the only method to change the resistance of the tunnel junctions by changing the magnetization direction of the electrodes. It is also possible to change the resistance of tunnel junctions using the anisotropy magnetoresistance (AMR) effect, which also causes a huge change in tunneling resistances under the CB regime.6) The SEST may include all kinds of SET whose tunneling resistances depend strongly on the magnetization directions of the FM electrodes. In the following sections, we assume that the tunneling resistances are changed by the TMR effect.

3. Tucker-Type Inverter with Variable Threshold Voltage

Figure 3 shows a Tucker-type inverter with a variable threshold voltage. The inverter is composed of two SESTs (SEST 1 and SEST 2). The structures of these two SESTs are exactly the same. The control gate of SEST 1 is connected to the ground so that it acts as a p-type transistor, i.e., when the gate voltage \( V_{in} \) is “1”, the transistor SEST 1 is OFF and vice-versa. On the other hand, the control gate of SEST 2 is connected to the supply voltage so that it acts as an n-type transistor, i.e., when the gate voltage \( V_{in} \) is “1”, the transistor SEST 2 is ON and vice-versa.7) In Fig. 4, we show the normalized transfer characteristics (\( V_{out}/V_{dd} \) vs \( V_{in}/V_{dd} \)) of this Tucker-type inverter, whose threshold voltage can be changed by the magnetization configuration. The parameters used in the calculations are \( C_1 = 1 \text{ aF}, \ C_2 = 2 \text{ aF}, \ C_b = 8 \text{ aF}, \ C_b = 7 \text{ aF}, \ C_{out} = 24 \text{ aF}, \ R_{1,P} = 0.5 \text{ M\Omega}, \ R_{1,AP} = 5 \text{ M\Omega}, \ R_{2,P} = 0.5 \text{ M\Omega}, \text{ and } T = 0.001e^2/(C_1 + C_2 + C_b + C_{out})k_B = 52 \text{ mK}. \) Here, \( C_b \) and \( C_{out} \) are the capacitances of the control gates and output terminal, respectively. Details of the calculation are shown in Appendix A. The blue curve shows the transfer characteristic when SEST 1 is in P magnetization and SEST 2 is in AP magnetization (\( (SEST1, SEST2) = (P, AP) \)). The red curve shows the transfer characteristic when SEST 1 is in AP magnetization and SEST 2 is in P magnetization (\( (SEST1, SEST2) = (AP, P) \)). In the region where \( V_{in} \) is smaller than the threshold voltage \( V_{th,SEST} \) of SEST 2 or
larger than the threshold voltage \( V_{th} \) of \( \text{SEST} 1 \) (the gray shaded area in Fig. 4), either \( \text{SEST} 2 \) or \( \text{SEST} 1 \) is OFF; thus, the output current does not flow. In this region, the output voltage does not depend on the magnetization configurations. However, the situation is different in the transient region (the white area in Fig. 4) where both \( \text{SEST} 2 \) and \( \text{SEST} 1 \) are ON. In the magnetization configuration of \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{P}, \text{AP} \} \), the resistances of the tunnel junctions of \( \text{SEST} 1 \) are smaller than those of \( \text{SEST} 2 \); thus, the output voltage is pulled up near the supply voltage (\( V_{dd} \)). In the magnetization configuration of \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{AP}, \text{P} \} \), the output voltage is pulled down near the ground level. In other words, we can change the threshold voltage of the inverter by changing the magnetization configuration of the circuit.

4. Reconfigurable AND/OR Gate

The first application of the Tucker-type inverter with a variable threshold voltage is a reconfigurable AND/OR gate, as shown in Fig. 5. The circuit is composed of two stages. The first stage, as shown in the white area of Fig. 5, is a two-input Tucker-type inverter with a variable threshold voltage and is composed of two \( \text{SESTs} \). Two-input gate electrodes \( V_A \) and \( V_B \) are directly coupled to each island of \( \text{SESTs} \) through two capacitors whose capacitances are half those of the Tucker-type inverter described in §3. This design creates an effective analog input \( V_m \) to both \( \text{SESTs} \) from two digital inputs \( V_A \) and \( V_B \) by the relation \( V_m = (V_A + V_B)/2 \). Consequently, the effective analog input \( V_m \) values corresponding to digital inputs “00”, “01” or “10”, and “11” of \( V_A \) and \( V_B \) are “0”, “1/2”, and “1”, respectively. As described in §3, the output \( V_m \) of the first stage is “1” and “0” when \( V_m \) is “0” and “1”, respectively, irrespective of the magnetization configurations of the two \( \text{SESTs} \). However, when \( V_m \) is “1/2”, \( V_B \) is weak “1” and weak “0” when the magnetization configurations of \( \text{SESTs} \) are \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{P}, \text{AP} \} \) and \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{AP}, \text{P} \} \), respectively. The second stage of the circuit, as shown by the gray area of Fig. 5, is a normal Tucker-type inverter composed of two \( \text{SESTs} \) and works as an inverse amplifier for \( V_m \). This second stage inverses weak “0”/weak “1” to strong “1”/strong “0” when the input \( V_m \) is “1/2”. Note that the second stage can be constructed by a normal CMOS-based inverter as well, but a SET-based inverter is preferable because its input capacitance is sufficiently small to cover the low current driving capability of \( \text{SESTs} \). The truth table of the circuit for each magnetization configuration is shown in Table I. By changing the circuit magnetization configuration from \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{P}, \text{AP} \} \) to \( \{ \text{SEST} 1, \text{SEST} 2 \} = \{ \text{AP}, \text{P} \} \), we can reconfigure the function of the circuit from the AND gate to the OR gate.

Figure 6 shows an example of the AND/OR circuit with parameters and its static operation calculated by Monte Carlo simulation. The parameters used in the simulations are \( C_1 = 1 \text{aF} \), \( C_2 = 2 \text{aF} \), \( C_g = 8 \text{aF} \), \( C_b = 7 \text{aF} \), \( C_{out} = 24 \text{aF} \), \( R_{1-AP} = R_{2-AP} = 0.5 \text{M}\Omega \), \( V_{dd} = 7 \text{mV} \), and \( T = 0.001e^2/(C_1 + C_g + C_b)k_B = 52 \text{mK} \). \( R_{1-AP} = R_{2-AP} = 5 \text{M}\Omega \), and \( R_{1-P} = R_{2-P} = 0.5 \text{M}\Omega \) for \( \text{SEST} 1 \) and \( \text{SEST} 2 \). As shown in Figs. 6(b) and 6(c), the circuit works as designed.

This example shows that it is possible to construct reconfigurable logic gates using only \( \text{SESTs} \) and \( \text{SESTs} \) without using any floating gate. Consequently, we are able to not only scale down the circuits but also keep the operating speed at an acceptable level. For the circuit in Fig. 5, the time constant of the output \( V_m \) of the first stage is given by \( R_{eff}(C_{out} + C_{ext}) \), where \( C_{ext} \) is the input capacitance of the second stage, and \( R_{eff} \) is the effective resistance of \( \text{SESTs} \), which is given by

\[
R_{eff} = \frac{C_1 + C_2 + C_g + C_b}{C_2} R_{1-ap} + \frac{C_1 + C_2 + C_g + C_b}{C_1 + C_g + C_b} R_{2-ap}.
\]

The time constant of \( V_m \) of the circuit shown in Fig. 6(a) is about 1.7 ns.

Let us then discuss about the possibility of fabricating
TMR materials. In the above calculation, an idealized TMR SEST that can work at room temperature using conventional TMR ratio.

We varied the TMR ratio by changing $T_{\text{MR}}$ of the above-mentioned circuit with different TMR ratios. The output voltages do not depend on the TMR ratio when the circuit can work, we have calculated the output voltages at which the circuit still works is about 150%. The high-temperature operation of SEST can be obtained using magnetic shape anisotropy or materials with large volume of the FM island. Such a condition can be achieved by reducing the sizes of the source, drain, and island to a few nanometers while keeping the thermal stability factor $K_v/V/k_BT$ larger than about 50 for 10 year nonvolatility, where $K_v$ is the magnetic anisotropy constant and $V$ is the volume of the FM island. Such a condition can be achieved using magnetic shape anisotropy or materials with large

\[
T_{\text{MRmin}} = \left( T_{\text{MRmin}} + \frac{\Delta R}{R} \right) \left( 1 - \frac{|\Delta R|}{R} \right).
\]

Here, $\Delta R/R$ is the resistance fluctuation. Consequently, when the fluctuation of the tunnel resistances exists, a larger minimum TMR ratio is required. For $|\Delta R/R| = 10\%$, $T_{\text{MRmin}}$ is 178%. Fortunately, $|\Delta R/R|$ as small as 2% has been realized at the mass production level by accurately controlling the tunnel barrier thickness of the vertical magnetic tunnel junctions.\(^{12}\) For such a small $|\Delta R/R|$, $T_{\text{MRmin}}$ is 155%, which is not much larger than $T_{\text{MRmin}}$.

The high-temperature operation of SEST can be obtained by reducing the sizes of the source, drain, and island to a few nanometers while keeping the thermal stability factor $K_v/V/k_BT$ larger than about 50 for 10 year nonvolatility, where $K_v$ is the magnetic anisotropy constant and $V$ is the volume of the FM island. Such a condition can be achieved using magnetic shape anisotropy or materials with large

\[
T_{\text{MRmin}} = \left( T_{\text{MRmin}} + \frac{\Delta R}{R} \right) \left( 1 - \frac{|\Delta R|}{R} \right).
\]
The integration of SETs and their room temperature operation has also been demonstrated. Analog pattern matching using integrated SET circuit has been performed at room temperature. Consequently, the fabrication of SESTs and their integrated circuits working at room temperature is not technologically unreachable.

5. Reconfigurable Logic Gate for All Symmetric Boolean Functions

In §4, the output is programmable only at $V_{in} = 1/2$; thus, reconfigurable functions are limited to the AND gate and OR gates. In this section, we show an extended version of the AND/OR gate whose output can be programmable at every input. This gate can perform any two-input symmetric Boolean functions (AND, OR, XOR, NAND, NOR, XNOR, all-"1", and all-"0"), as shown below. Figure 8 shows the circuit configuration of this reconfigurable gate. The circuit is composed of two stages. The first stage is composed of four SESTs (SEST 1, SEST 2, SEST 3, and SEST 4) and two SET based inverters (INV 1 and INV 2). SEST 1 and SEST 3 work as p-type transistors, whereas SEST 2 and SEST 4 work as n-type transistors. The inverter INV 1 has a threshold voltage higher than “1/2” and its output electrode is connected to the gate electrode of SEST 3. The inverter INV 2 has a threshold voltage lower than “1/2” and its output electrode is connected to the gate electrode of SEST 4. Two digital inputs $V_A$ and $V_B$ are coupled to each island of SEST 1, SEST 2, INV 1, and INV 2 through two capacitors whose capacitances are half those of the Tucker-type inverter described in §3, so that the inputs $V_{in}$ to these four devices are $(V_A + V_B)/2$. The second stage is a SET-based inverter (INV 3) with a threshold voltage of “1/2” working as an inverse amplifier for the output $V_{in}$ of the first stage. The operation of the circuit is as follows.

1. When $[V_A, V_B] = [1, 0]$ or $[0, 1]$, the input $V_{in}$ is “1/2”, thus SEST 1 and SEST 2 are ON, whereas SEST 3 and SEST 4 are OFF. In this case, the circuit works in the same way as the AND/OR gate in Fig. 5. When $[V_A, V_B] = [1, 1]$, the output is “0”, and when $[V_A, V_B] = [0, 0]$, the output is “1”.

2. When $[V_A, V_B] = [0, 0]$, the input $V_{in}$ is “0”, thus SEST 1 and SEST 4 are ON, whereas SEST 2 and SEST 3 are OFF. In this case, the electric current flows from the supply voltage to the ground through SEST 1 and SEST 3. By setting $R_{SEST \ 4-P} < R_{SEST \ 1-P} < R_{SEST \ 1-AP} < R_{SEST \ 4-AP}$, the output voltage $V_{out}$ is “1” and “0” when the magnetization configuration of SEST 4 is P and AP, respectively. Here $R_{SEST \ 1-P}$ and $R_{SEST \ 3-AP}$ are the resistance of the tunnel junctions of SEST $i$ in P and AP magnetization configurations, respectively.

3. When $[V_A, V_B] = [1, 1]$, the input $V_{in}$ is “1”, thus SEST 2 and SEST 3 are ON, whereas SEST 1 and SEST 4 are OFF. In this case, the electric current flows from the supply voltage to the ground through SEST 2 and SEST 3. By setting $R_{SEST \ 3-P} < R_{SEST \ 2-P} < R_{SEST \ 2-AP} < R_{SEST \ 3-AP}$, the output voltage $V_{out}$ is “1” and “0” when the magnetization configuration of SEST 3 is AP and P, respectively.

The truth table of this reconfigurable circuit for each magnetization configuration is shown in Table II. An example of the circuit with parameters and its operation calculated by Monte Carlo simulations are shown in Fig. 9. The parameters used in the simulations are $C_1 = 0.1 \text{ fF}$, $C_2 = 2 \text{ aF}$, $C_3 = 8 \text{ aF}$, $C_4 = 7 \text{ aF}$, $C_{out} = 24 \text{ aF}$, $V_{dd} = 7 \text{ mV}$, $T = 0.001e^2/(C_1 + C_2 + C_3 + C_bM_b) = 52 \text{ mK}$, $R_{1-AP} = R_{2-AP} = 50 \text{ M\Omega}$, and $R_{1-P} = R_{2-P} = 5 \text{ M\Omega}$ for SEST 1 and SEST 2, and $R_{3-AP} = R_{4-AP} = 500 \text{ M\Omega}$ and $R_{3-P} = R_{4-P} = 0.5 \text{ M\Omega}$ for SEST 3 and SEST 4. As shown in Fig. 9(b), all two-input symmetric Boolean functions are operated as designed.

6. Conclusions

We propose a new kind of reconfigurable logic design using single-electron spin transistors (SESTs), by which we can realize analog inputs without using a floating gate. A Tucker-type inverter, an AND/OR reconfigurable gate, and a reconfigurable logic gate for two-input all symmetric
Boolean functions were proposed and their operations were calculated by Monte Carlo simulations. The proposed logic gates can provide nonvolatile and scalable reconfigurable hardware for future electronics.

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Appendix A

Here, we describe the calculation procedure for the $I_{ds}-V_{ds}$ and $I_{ds}-V_{gs}$ characteristics of a single SEST and for the static operation of reconfigurable logic gates using SESTs. In the calculation, we assumed that the tunneling rate through every junction is much smaller than the rate of spin relaxation, so that the chemical potential in every island is spin-independent. This leads to a master equation that can be used to describe the time evolution of the probability $p_n(t)$ for $n$ excess electrons in a particular island:

$$\frac{dp_n}{dt} = \Gamma_{n+1 \rightarrow n} p_{n+1} + \Gamma_{n \rightarrow n+1} p_{n-1}$$

where the net tunnel rates $\Gamma_{n \rightarrow n+1}$ and $\Gamma_{n \rightarrow n-1}$ are given by

$$\Gamma_{n \rightarrow n+1} = \tilde{\Gamma}_L(n) + \tilde{\Gamma}_R(n),$$

$$\Gamma_{n \rightarrow n-1} = \tilde{\Gamma}_L(n) + \tilde{\Gamma}_R(n).$$

Here, $\tilde{\Gamma}_L(n)$ and $\tilde{\Gamma}_R(n)$ are the tunneling rates of an electron to the island through the left and right junctions, respectively. $\tilde{\Gamma}_L(n)$ and $\tilde{\Gamma}_R(n)$ are the tunneling rates of an electron out of the island through the left and right junctions, respectively. When there are $n$ electrons in the island, the tunneling rates can be calculated using the following equations\(^5\)

$$\tilde{\Gamma}_L(n) = \frac{1}{e^2 R_{LR} / C_{ds} + e^2 R_{LR} / C_{ds} G_{ds} / V_{gs}}$$

and

$$\tilde{\Gamma}_R(n) = \frac{1}{e^2 R_{LR} / C_{ds} + e^2 R_{LR} / C_{ds} G_{ds} / V_{gs}}$$

where $Q_1$ and $Q_2$ are the charge of the left and right junctions, and $Q_{c1}$ and $Q_{c2}$ are the critical charges of the left and right junctions, respectively. At the steady state, we can calculate $p_n$ by solving $dp_n/dt = 0$ with the condition $\sum_{n=-\infty}^{\infty} p_n = 1$. Then, the current through the island can be calculated by

$$I = e \sum_{n=-\infty}^{\infty} p_n [\tilde{\Gamma}_L(n) - \tilde{\Gamma}_R(n)].$$
solving eqs. (A-1)–(A-8). However, for reconfigurable logic gates using several SESTs, it is impossible to solve the master eq. (A-1) directly because the multidimensional space of all possible charge states becomes too large. Here, we use the Monte Carlo simulation to calculate the static voltages of the output terminals as follows: the duration to the next tunneling event in a particular junction is first calculated by

\[ t = -\frac{\ln r}{\Gamma}, \quad (A-9) \]

where \( r \) is an evenly distributed random number from the interval \([0,1]\) and \( \Gamma \) is the tunneling rate given by eq. (A-4) and eqs. (A-5)–(A-7). All possible durations at any junctions are calculated, and the shortest duration is taken. After a tunneling event, island charges and island voltages also change. The calculation using eqs. (A-4)–(A-7) and (A-9) is then repeated for a few \( 10^5 \) circles to calculate the time-averaged voltage values of the output terminals. In this way, we calculate the output voltages of the Tucker-type inverter with a variable threshold voltage, the reconfigurable AND/OR gate, and the reconfigurable logic gate for all symmetric Boolean functions at particular inputs.

Appendix B

Here, we calculate the TMR ratio fluctuation caused by the fluctuation of the tunnel resistances. From \( R_{\text{AP}} = (TMR + 1)R_P \), we obtain the relationship between the fluctuation \( \Delta TMR \) of the TMR ratio and the fluctuations \( \Delta R_A \) and \( \Delta R_P \) of tunnel resistances at AP and P magnetization configurations

\[ \frac{\Delta R_A}{R_A} = \frac{\Delta TMR}{TMR + 1} + \frac{\Delta R_P}{R_P}, \quad (B-1a) \]

or

\[ \frac{\Delta TMR}{TMR} = \left( \frac{\Delta R_A}{R_A} - \frac{\Delta R_P}{R_P} \right) \left( 1 + \frac{1}{TMR} \right). \quad (B-1b) \]

Since \( \Delta R_A/R_A \) has the same sign as \( \Delta R_P/R_P \) and \( |\Delta R_P/R_P| \leq |\Delta R_A/R_A| = |\Delta R/R| \), we have

\[ \left| \frac{\Delta R_A}{R_A} - \frac{\Delta R_P}{R_P} \right| \sim O\left( \frac{|\Delta R|}{R} \right) \ll \frac{|\Delta R|}{R}. \quad (B-2) \]

Consequently, the maximum \( |\Delta TMR| \) is given by

\[ \frac{|\Delta TMR|_{\text{max}}}{TMR} = \frac{\Delta R}{R} \left( 1 + \frac{1}{TMR} \right). \quad (B-3) \]

To satisfy \( TMR - |\Delta TMR|_{\text{max}} > TMR_{\text{min}} \), we need the TMR ratio \( TMR_{\text{min}}' \) to be greater than \( TMR_{\text{min}} \) to overcome the resistance fluctuation:

\[ TMR_{\text{min}}' = \left( TMR_{\text{min}} + \frac{\Delta R}{R} \right) \left( 1 - \left| \frac{\Delta R}{R} \right| \right). \quad (B-4) \]

1) S. Sugahara and M. Tanaka: Appl. Phys. Lett. 84 (2004) 2307.
2) T. Matsuno, S. Sugahara, and M. Tanaka: Jpn. J. Appl. Phys. 43 (2004) 6032.
3) K. K. Likharev: IEEE Trans. Magn. 23 (1987) 1142.
4) N. Kuwamura, K. Taniguchi, and C. Hamawaka: IEICE Trans. Electron. J77-C-II (1994) 221 [in Japanese].
5) G.-L. Ingold and Yu. V. Nazarov: in Single Charge Tunneling (Plenum Press, New York, 1992) Chap. 2, p. 21.
6) J. Wunderlich, T. Jungwirth, B. Kaestner, A. C. Irvine, A. B. Shick, N. Stone, K.-Y. Wang, U. Rana, A. D. Biddulph, C. T. Foxton, R. P. Campion, D. A. Williams, and B. L. Gallagher: Phys. Rev. Lett. 97 (2006) 077201.
7) J. R. Tucker: J. Appl. Phys. 72 (1992) 4399.
8) H. Butler, X.-G. Zhang, T. C. Schuttehess, and J. M. Maclaren: Phys. Rev. B 63 (2001) 054416.
9) X.-G. Zhang and W. H. Butler: Phys. Rev. B 70 (2004) 172407.
10) S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S. H. Yang: Nat. Mater. 3 (2004) 862.
11) S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando: Nat. Mater. 3 (2004) 868.
12) M. Motoyoshi, I. Yamamura, W. Ohtsuka, M. Shouji, H. Yamagishi, M. Nakamura, H. Yamada, K. Tai, T. Kikutani, T. Sagara, K. Moriyama, H. Mori, C. Fukushima, M. Watanabe, H. Hachino, H. Kano, K. Bessho, H. Narisawa, M. Hosomi, and N. Okazaki: Symp. VLSI Technology, 2004, p. 22.
13) D. Weller, A. Moser, L. Folks, M. E. Best, W. Lee, M. F. Toney, M. Schwikkert, J.-U. Thiele, and M. F. Doerner: IEEE Trans. Magn. 36 (2000) 10.
14) J. C. Slonczewski: J. Magn. Magn. Mater. 159 (1996) L1.
15) M. Hosomi, H. Yamagishi, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada, M. Shouji, H. Hachino, C. Fukushima, H. Nagao, and H. Kano: IEDM Tech. Dig., 2005, p. 459.
16) K. Uchida, J. Koga, R. Ohba, and A. Toriumi: IEDM Tech. Dig., 2000, p. 863.
17) M. Saitoh, T. Murakami, and T. Hiramoto: IEEE Trans. Nanotechnol. 2 (2003) 241.
18) M. Saito and T. Hiramoto: Electron. Lett. 40 (2004) 836.
19) M. Saito and T. Hiramoto: Appl. Phys. Lett. 84 (2004) 3172.
20) M. Saitoh, H. Harata, and T. Hiramoto: Jpn. J. Appl. Phys. 44 (2005) L338.
21) M. Saitoh, H. Harata, and T. Hiramoto: IEDM Tech. Dig., 2004, p. 187.