Analyzing FreeRTOS Scheduling Behaviors with the Spin Model Checker

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Abstract

FreeRTOS is a real-time operating system with configurable scheduling policies. Its portability and configurability make FreeRTOS one of the most popular real-time operating systems for embedded devices. We formally analyze the FreeRTOS scheduler on ARM Cortex-M4 processor in this work. Specifically, we build a formal model for the FreeRTOS ARM Cortex-M4 port and apply model checking to find errors in our models for FreeRTOS example applications. Intriguingly, several errors are found in our application models under different scheduling policies. In order to confirm our findings, we modify application programs distributed by FreeRTOS and reproduce assertion failures on the STM32F429I-DISC1 board.

1 Introduction

FreeRTOS is an open-sourced real-time operating system supporting various architectures [31]. Because of its portability, FreeRTOS is the third most popular operating system in 2019 [4]. It has been used in numerous embedded devices [1, 5, 13, 28, 30, 32, 38].

One of the most useful features in FreeRTOS is multitasking on uni-processor embedded devices. Through multitasking, applications can be divided into several simpler tasks sharing processor time. Indeed, FreeRTOS provides three configurable scheduling policies for different applications. Multitasking nevertheless can induce undesirable phenomenon such as deadlocks or starvation. It is therefore crucial to prevent such errors in deployment. Multi-tasking errors on the other hand are notoriously evasive. Due to complex interleavings among tasks, a very limited number of system behaviors can be tested. In order to check multi-tasking in FreeRTOS more thoroughly, we apply model checking in our analysis.

Model checking is a formal technique to analyze properties about systems [15]. In model checking, behaviors of the system under verification are specified in a formal model. Model checkers can verify the model automatically with formal properties provided by users. Different from testing tools, model checkers search model behaviors exhaustively. If a deviant behavior is found, it is reported to verifiers. If no deviance can be found after exhaustive search, all model behaviors conform to the specified property. The formal model is thus verified.

In this paper, we develop formal models for the FreeRTOS scheduler on ARM Cortex-M4 processors and analyze its properties by the SPIN model checker. Based on the reference manual, we build formal models for the ARM Cortex-M4 interrupt handling mechanism. Particularly, optimizing mechanisms such as tail chaining are implemented in our models. Through examining source codes of the FreeRTOS ARM Cortex-M4 port, formal models for the FreeRTOS scheduler, thread-safe data structures, and its applications are also built. Particularly, all FreeRTOS scheduling policies are formalized in our models as well.

With our behavior models for FreeRTOS, it remains to identify formal properties to check. Such properties however can be tricky to find. For formal analysis, high-level informal properties such as absence of deadlocks or starvation need to be specified concretely. In complex systems like FreeRTOS, high-level properties are often asserted with caveats to preclude minor or unrealistic errors. It can be very tedious to specify caveats formally. Moreover, one can not be sure of these caveats without FreeRTOS developers’ help. Different developers can also have different views on properties and caveats. Subsequently, formal properties specified by verifiers can be contrived or even incorrect.

We solve the property specification problem by verifying example applications in the FreeRTOS distribution. In order to highlight FreeRTOS features, developers provide a number of example applications for demonstration. Most example applications contain assertions to specify expected behaviors during execution. Intuitively, no assertion failure should be observed on any multi-tasking execution. We therefore add assertions to our model and verify them with the SPIN model checker. Intriguingly, the model checker reports errors on several example application models.

Assertion errors found in formal analysis do not necessarily imply assertion failures in real execution. In order to confirm
our findings, we modify FreeRTOS example applications to reproduce error traces in our formal behavior models. If assertion errors in formal analysis are genuine, we should observe assertion failures on real hardware. Using the STM32F429I-DISC1 board from STMicroelectronics, we successfully reproduce assertion failures in our experiments. We use the remote GDB debugger to confirm failures against intended assertions. All assertion failures require delicate interactions among tasks, the FreeRTOS scheduler, and the ARM Cortex-M4 interrupt handling mechanism. They are unlikely to be discovered by testing.

This paper is organized as follows. Section 2 introduces the SPIN model checker. Section 3 presents analysis methodology. Section 4 describes a task and an interrupt handler models. Section 5 describes FreeRTOS scheduling policies. Section 6 describes tasks delaying and suspending mechanism. Section 7 describes a thread-safe data shared by tasks. Section 8 describes FreeRTOS example applications. Section 9 classifies assertions in the applications as properties. Section 10 reports verification results and discussion. Section 11 gives related works. Section 12 concludes.

2 Background

Model checking is an automatic formal verification technique. In model checking, systems under verification are specified as formal models. Properties about systems are also formalized by logical properties about formal models. Given a formal model and a logical property, a model checker automatically verifies the logical property against the model through mathematical reasoning. If the model is verified, the property holds in the model mathematically. If the model is not verified, the model checker returns a trace to witness the error.

SPIN is a model checker designed for analyzing communicating concurrent processes [26]. It offers the PROMELA (PROCess MEta LAnguage) language to specify formal models for systems. A formal model in PROMELA consists of the main process. Additional processes can be instantiated if needed. A process contains a sequence of commands. Commands must be enabled before execution. Enabled commands in all processes (including the main process) are executed interleavingly. That is, exactly one enabled command is executed at any time. If several commands from different processes are enabled, one of the enabled commands is executed non-deterministically. If there is no enabled command among all processes, it is a deadlock. The PROMELA language allows verifiers to specify assertions in processes. An assertion command contains a Boolean expression and is always enabled. Its Boolean expression is evaluated when an assertion command is executed. If the Boolean expression is false, it is an assertion error. Recall that enabled commands are executed non-deterministically. Non-deterministic executions result in different traces. Some traces have assertion errors but others have not.

```
byte counter; bool b[3];

proctype Guess(byte idx) {
    atomic |
        if |
            true -> b[idx] = false; counter++;
            true -> b[idx] = true; counter++;
        fi;
    } |
    init |
        counter = 0;
        run Guess(0); run Guess(1); run Guess(2);
    do |
        counter == 3 -> break
    od;
    assert (!( b[0] && b[1] && !b[2] ));
}
```

![Figure 1: Boolean Satisfiability Solver](image)

Since traces formalize system behaviors, a deadlock or an assertion error in any trace represent undesirable system behaviors. We therefore would like to check if deadlocks or assertion errors occur among all traces. The SPIN model checker systematically explores all traces with sophisticated algorithms. If a deadlock or an assertion error occurs in any trace, SPIN will find the error trace and report it as a witness. If the model checker does not find any deadlock or assertion error after exploring all traces, the model is verified.

Figure 1 gives a simple PROMELA model solving Boolean satisfiability from the SPIN distribution. It contains the variable `counter` and the Boolean array `b` of size 3. The model declares a process called `Guess`. Given an index `idx`, `Guess(idx)` assigns a Boolean value to the array element with the index `idx`. The `if` command contains two commands. Since both commands are enabled, one of them is chosen to assign the array element non-deterministically. The variable `counter` is then incremented by one. The `atomic` keyword indicates all commands in its brackets are executed atomically.

The keyword `init` designates the main process. In the main process, `counter` is set to zero. An instance of the `Guess` process is created for each element in the Boolean array. After process instantiation, the main process enters a busy-waiting loop. The `do` command executes an enabled command repeatedly until the `break` command. The main process subsequently waits until the value of `counter` is equal to 3. When `counter` is 3, all array elements have been assigned. The main process checks if the Boolean expression in the `assert` command is true. If not, it is an assertion error.

Recall that the `Guess` process assigns a Boolean value to an array element non-deterministically. Depending on non-deterministic assignments, an assertion error may or may not occur in the `assert` command. The SPIN model checker verifies if an assertion error occurs in all traces induced by different non-deterministic assignments. In the example, SPIN finds an assertion error and reports the trace ending with `b[0] = b[1] = true and b[2] = false`.

Observe that assignments in the `Guess` process are not the
only non-deterministic behaviors. Since the main process and three instances of the Guess process are running, the order of execution is also non-deterministic. For instance, any of the three Guess processes may assign to its array element before the other two. In Figure 1, several traces indeed end with the state where the assertion error occurs. The SPIN model checker reports the first assertion error found.

In addition to assertions, SPIN allows verifiers to specify properties with Linear Temporal Logic (LTL) formulas. Particularly, we will use the LTL formula $\Box \Diamond Loc$ where $Loc$ denotes a process location. A trace satisfies $\Box \Diamond Loc$ if it visits the process location $Loc$ infinitely many times. We use the formula $\Box \Diamond Loc$ to specify that a process is free of starvation. More concretely, let $Loc$ be the location where a process finishes its job. A trace satisfies $\Box \Diamond Loc$ if the process finishes its job infinitely many times. More generally, the LTL formula $\Box \Diamond Loc_0 \rightarrow \Box \Diamond Loc_1$ specifies that the process location $Loc_1$ is visited infinitely many times if $Loc_0$ is visited infinitely many times.

3 Methodology Overview

In order to support different architectures, the FreeRTOS scheduler contains both architecture-dependent and architecture-independent codes. Roughly, scheduling policies are independent of underlying architectures. They provide abstract programming models for applications. Their implementations must depend on interrupt mechanisms in underlying architectures however. For instance, the FreeRTOS scheduler is called during periodic and sporadic interrupts in the ARM Cortex-M4 port. For analysis, it is essential to consider as many interrupt sequences as possible. Generating such interrupt sequences for testing is infeasible. A more effective technique is needed.

In this work, we develop a PROMELA model for the interrupt mechanism on ARM Cortex-M4 processors. Behaviors of optimizing mechanisms for ARM Cortex-M4 processors are carefully formalized in our model. More importantly, non-deterministic interrupts allow us to explore a gigantic amount of interrupt sequences unattainable by testing.

On top of our formal model for the ARM Cortex-M4 interrupt mechanism, we then specify a PROMELA model for the architecture-independent codes in the FreeRTOS scheduler. All three FreeRTOS scheduling policies are specified in our model. Our formal model for the FreeRTOS scheduler on ARM Cortex-M4 processors enables extensive analysis on task synchronization – task delay and suspension. We moreover build formal models for thread-safe data structures such as queues and locks (send/receive and give/take). These structures are widely used by FreeRTOS applications.

With formal models, we proceed to verify properties about the FreeRTOS scheduler. Although abstract properties such as the absence of deadlock and starvation are easily said, they are not precise enough for formal analysis. Additionally, properties are unlikely to be satisfied without provisions. Without FreeRTOS developers’ inputs, contrived or even misleading properties can be verified meaningless.

We address this problem by verifying FreeRTOS example applications. Similar to most open-sourced projects, FreeRTOS provides example applications to illustrate its features. These applications contain assertions to specify expected behaviors. Intuitively, these assertions are but formal properties written by FreeRTOS developers. No assertion failure should be observed under all circumstances. In order to verify assertions in FreeRTOS example applications, we build their formal models and check if an assertion error might occur. Intriguingly, several assertion errors were found in our analysis.

It is important to recall that formal models are different from real hardware and software by definition. Assertion errors found on the models do not necessarily correspond to assertion failures on real systems. In order to support our findings, we examine the error traces found by the SPIN model checker and reproduce them on the STM32F429I-DISC1 board. We moreover use the remote debugger GDB to confirm assertion failures on the ARM Cortex-M4 board. Many errors found by our formal analysis are successfully realized on real systems. These assertion failures require intricate interrupt events. They are unlikely to be found by traditional testing.

4 Execution Units

Our goal is to develop PROMELA models for the ARM Cortex-M4 interrupt mechanism, the FreeRTOS scheduler, thread-safe data structures, and example applications. An application has a number of tasks to be executed by the processor. When an interrupt is triggered, its interrupt handler will be executed by the processor. We therefore say a task or an interrupt handler are execution units. In our PROMELA model, an execution unit is formalized as a PROMELA process. Commands in the process thus specify the computation of the execution unit.

4.1 Task

Typical FreeRTOS tasks loop forever and never terminate. Their models are PROMELA processes with infinite loops (Figure 2). In PROMELA, an enabled command is executed non-deterministically among all such commands in all processes. Our FreeRTOS task models however need to be scheduled by our formal scheduler model before execution. To this end, we define the global variable $EP$ for (Executing Process) and assign each execution unit a unique identification number. Every guard and command in task models are annotated with the condition $EP == id$. The FreeRTOS scheduler model in turn assigns the variable $EP$ to elect task models.

More precisely, each guard $bexp$ is annotated with the macros $\text{SELE}(id, bexp)$ or $\text{ELSE}(id, bexp)$; each command $cmd$ is annotated with $\text{AWAIT}(id, cmd)$. The macros $\text{SELE}(id, bexp)$ and $\text{ELSE}(id, bexp)$ add the condition $EP ==
id in conjunction with the Boolean expression bexp and its negation respectively. If the task model is not scheduled for execution, the variable EP is not equal to its identification number and the annotated guard is false. Otherwise, the variable EP is set to its identification number and the guard bexp is then checked. The macro \texttt{AWAIT(id,cmd)} adds the guard EP $==$ id to the command cmd. The annotated command is enabled precisely when the task model is scheduled.

4.2 ARM Cortex-M4 Interrupt Handler

For ARM Cortex-M4 processors, an interrupt is triggered when it is set to the pending state. When an interrupt is pending, the processor decides whether the current execution should be interrupted. If the pending interrupt has a priority over the current execution and is unmasked, the current execution is interrupted by the interrupt handler of the pending interrupt.

Bookkeeping is needed when the current execution is interrupted. At exception entry, the current processor state is pushed onto a stack, the pending state of the interrupt is unset, and the processor is prepared to execute the interrupt handler. The interrupt handler is executed during the exception taken phase. When the interrupt handler finishes its execution, the interrupted processor state is restored at exception return. The interrupted execution is then resumed.

Recall that a triggered interrupt remains pending when it does not have the priority or is masked. At exception return, the processor checks if there is any pending interrupt with a priority over the topmost processor state on the stack. If so, exception return is bypassed and the pending interrupt proceeds to exception entry. This optimization is called tail chaining.

Figure 3 gives the outline of an interrupt handler model. An interrupt handler model with the identification number id consists of an infinite loop with a sequence of commands. The macro \texttt{IRQ(id)} (for interrupt request) checks the interrupt conditions before exception entry. In the macro, \texttt{IS_PENDING(id)} and \texttt{IS_MASKED(id)} check whether the interrupt id is pending and masked respectively. \texttt{PRIORITIZING(id, EP)} checks if the interrupt id has the priority over the running execution unit EP. \texttt{IRQ(id)} uses another macro \texttt{ExpEntry(id)} if all conditions are satisfied. In \texttt{ExpEntry(id)}, the current execution unit identification number is pushed on a stack, the pending state of the interrupt id is unset, and the variable EP is assigned to the identification number id of the interrupt handler model. Commands in the interrupt handler model can then be executed. After the interrupt handler model finishes, the \texttt{ExpReturn()} macro pops an identification number from the stack and assigns it to the variable EP. The interrupted execution unit can then continue.

When an interrupt is pending but masked, \texttt{IS_MASKED(id)} is true. The interrupt handler model will not execute \texttt{ExpEntry(id)}. Instead, the model waits until it becomes unmasked. Whenever a pending interrupt is unmasked, the corresponding handler model can check if it should execute \texttt{ExpEntry(id)}.

Finally, an interrupt may remain pending when it does not have the priority over the running execution unit (\texttt{PRIORITIZING(id, EP)} is false). When the interrupt with the priority finishes, the interrupt handler will be taken without exception entry by tailing chaining. Our interrupt handler model also performs tail chaining when an interrupt is pending due to insufficient priorities (not shown in Figure 3).

5 FreeRTOS Scheduler

The FreeRTOS scheduler implements three scheduling policies. In cooperative scheduling, a running task has to yield the processor explicitly. In preemptive scheduling without time slicing, a running task can be preempted by tasks with higher priorities. Finally, a task can moreover be preempted by using up its time slice in preemptive scheduling with time slicing. Depending on the policy, the FreeRTOS scheduler is called to elect the next task at different occasions.

In the FreeRTOS ARM Cortex-M4 port, scheduling policies are implemented via two interrupt handlers. The interrupt handler for the software interrupt PendSV is used for task scheduling and context switching. More precisely, the PendSV interrupt handler calls the FreeRTOS scheduler to elect the next task for execution. After a task is elected, the scheduler sets up the processor state through the ARM Cortex-
The interrupt handler model is taken and preemptive. This is implemented with the SysTick interrupt handler model as in real hardware. An error found in the model can be spurious. It has to be validated by corresponding failures in real hardware.

In cooperative scheduling, a task calls the FreeRTOS synchronization functions are implemented by the PendSV and SysTick interrupt handlers as well. The SysTick interrupt handler checks if any task in the delay queue has expired its duration periodically. If so, the interrupt handler removes such tasks from the delay queue. In contrast, suspended tasks are removed from the suspended queue when they are resumed by the running task. If preemptive scheduling is disabled, the running task continues its execution until it yields the processor.

If preemptive scheduling is enabled, the PendSV interrupt is triggered when the tasks removed from the delay or suspended queues have the priority over the running task. Effectively, the SysTick interrupt is triggered arbitrarily in our formalization. This is a simple but useful abstraction in our model. The conservative abstraction ensures that all SysTick interrupt sequences in real world are subsumed in our model. If there is any failure among all real interrupt sequences, it will be exposed in our model. On the other hand, not all interrupt sequences in our model are real. An error found in the model can be spurious. It has to be validated by corresponding failures in real hardware.

In addition to task scheduling, the FreeRTOS scheduler also provides basic functions for task synchronization. More concretely, a task can be delayed for a specified duration; it can also be suspended indefinitely. When a task is delayed, it is moved to a delay queue and hence cannot be scheduled for execution. Similarly, a suspended task is moved to a suspended queue and thus ineligible for scheduling. When its delay duration expires, a delayed task is removed from the delay queue and can be scheduled for execution. When a suspended task is resumed by the running task, it is removed from the suspended queue and ready for scheduling.

In the FreeRTOS ARM Cortex-M4 port, basic task synchronization functions are implemented by the PendSV and SysTick interrupt handlers as well. The SysTick interrupt handler checks if any task in the delay queue has expired its duration periodically. If so, the interrupt handler removes such tasks from the delay queue. In contrast, suspended tasks are removed from the suspended queue when they are resumed by the running task. If preemptive scheduling is disabled, the running task continues its execution until it yields the processor.

If preemptive scheduling is enabled, the PendSV interrupt is triggered when the tasks removed from the delay or suspended queues have the priority over the running task. The FreeRTOS scheduler elects a task with the highest priority for execution. A previously delayed or suspended task will continue its execution; and the running task will be preempted if it does not have the priority.

To simplify the boundary condition where all tasks are delayed or suspended, FreeRTOS creates an idle task. The idle task has the lowest priority and cannot be delayed nor suspended. It can also be configured to yield the processor on its own. If the idle task should yield, it yields the processor to the next scheduled task immediately. Otherwise, the idle task

```c
proctype PendSV_handler() {  
do  
:: atomic | IRQ(PID_PendSV) | -> /* Process delayed tasks */  
ifdef PREEMPTIVE_SCHEDULING  
/* SET_PENDING(PID_PendSV) if the expired tasks have  
the priority over the running task. */  
ifdef TIME_SLICING  
/* SET_PENDING(PID_PendSV) */  
endif  
endif  
AWAIT(PID_PendSV, ExpReturn());  
od  
}

proctype SysTick_handler() {  
do  
:: atomic | IRQ(PID_SysTick) | -> /* Process delayed tasks */  
ifdef PREEMPTIVE_SCHEDULING  
/* SET_PENDING(PID_SysTick) if the expired tasks have  
the priority over the running task. */  
endif  
AWAIT(PID_SysTick, ExpReturn());  
od  
}
```

Figure 4: PendSV and SysTick Interrupt Handler Models

M4 interrupt handling mechanism for context switching. After exception return, the context of the newly elected task is restored. The elected task resumes its execution as if it were returned from an interrupt handler in FreeRTOS. The PendSV interrupt is triggered whenever a task needs to be elected in all scheduling policies.

For preemptive scheduling with time slicing, the PendSV interrupt needs to be triggered at every time slice periodically. This is implemented with the SysTick interrupt. The SysTick interrupt is triggered by a hardware clock periodically. If preemptive scheduling is enabled, the SysTick interrupt handler triggers the PendSV interrupt. When the SysTick interrupt handler finishes, the PendSV interrupt handler will be executed directly by tail chaining.

Our PROMELA model follows the FreeRTOS ARM Cortex-M4 port to specify the scheduler in interrupt handler models for PendSV and SysTick (Figure 4). Both interrupt handler models use IRQ(PIDid) for interrupt requests and exception entry. When the PendSV interrupt handler model is executed, a task identification number is chosen by NextTaskId(). The chosen identification number then replaces the identification number on the top of stack. In ExpReturn(), the variable EP is set to the chosen identification number on stack. The elected task model can continue its execution.

The SysTick interrupt handler model is similar (Figure 4). When the interrupt handler model is taken and preemptive scheduling is enabled, it conditionally triggers the PendSV interrupt with SET_PENDING(PID_PendSV). If it is triggered, the PendSV interrupt presently has not the priority and will keep pending. The SysTick interrupt handler model then executes ExpReturn(). The PendSV interrupt handler model will be taken directly by tail chaining in our interrupt handler models. A task identification number can then be chosen by the PendSV interrupt handler model as in real hardware.

In our model, the SysTick interrupt is triggered with SET_PENDING(PID_SysTick). Since the PROMELA language is timeless, our model cannot trigger the SysTick interrupt periodically. Rather, our model non-deterministically triggers the interrupt. Effectively, the SysTick interrupt is triggered arbitrarily in our formalization. This is a simple but useful abstraction in our model. The conservative abstraction ensures that all SysTick interrupt sequences in real world are subsumed in our model. If there is any failure among all real interrupt sequences, it will be exposed in our model. On the other hand, not all interrupt sequences in our model are real. An error found in the model can be spurious. It has to be validated by corresponding failures in real hardware.

In cooperative scheduling, a task calls the FreeRTOS yield function to release the processor. The yield function simply triggers the PendSV interrupt to elect a task in the PendSV interrupt handler. It is straightforward to define the FreeRTOS yield function in our model:

```c
#define yield(id) AWAIT(id, SET_PENDING(PID_PendSV))
```
loops until it is preempted.

Our model for basic task synchronization follows the FreeRTOS Cortex-M4 port as well (Figure 4). The SysTick interrupt handler model checks if any delayed task has expired delay duration. Recall that our formal model is timeless. Delay duration cannot be formalized exactly. We therefore formalize delay duration by counters. When a task model is delayed, a counter is set. When the SysTick interrupt handler model is executed, it decreases counters of all delayed task models by one. A counter of a delayed task model is expired if it reaches zero. When their counters are expired, the SysTick interrupt handler model removes such tasks from the delay queue. In order to resume suspended tasks, the running task model removes such tasks from the suspended queue and prepares them for scheduling. If preemptive scheduling is enabled and the removed tasks have the priority, the PendSV interrupt is moreover triggered with \texttt{SET\_PENDING(PID\_PendSV)}.

Whether the idle task should yield has impacts on the FreeRTOS scheduler. The idle task is also formalized in our model. Our idle task model can also be configured to yield the processor whenever possible.

7 Thread-Safe Data Structures

In addition to basic task synchronization, FreeRTOS also provides thread-safe data structures for message passing and advanced synchronization among tasks. A thread-safe structure consists of its data and a waiting task queue. A task can modify a thread-safe structure immediately when its data are ready. Otherwise, the task will be blocked. When a task is blocked, it is moved to the waiting task queue of the thread-safe structure for specified duration. Different from basic task synchronization, tasks can be unblocked when its duration is expired or when the data become ready. It is a failure if the duration of a blocked task is expired before the data are ready.

FreeRTOS implements thread-safe queues for message passing. A thread-safe queue contains a bounded buffer as its data. The capacity of the buffer is specified by programmers. The buffer is ready for modification when it is neither empty nor full. A task will be blocked when it adds to a full buffer or removes from an empty buffer. FreeRTOS provides two functions for thread-safe queues. The \texttt{Send(delay)} function inserts a message into the buffer; the \texttt{Receive(delay)} function removes a message from the buffer. The parameter \texttt{delay} specifies the duration. Consider, for instance, a sender is blocked by sending a message to a full buffer. When a message is removed from the buffer, the sender will be unblocked immediately even before its duration expires. If the buffer remains full during the specified duration, the sender will be unblocked with a failure. Particularly, \texttt{Send(0)} returns a failure immediately if the thread-safe queue is full at the time of invocation. Similarly, \texttt{Receive(0)} returns a failure if the queue is empty at the time of invocation.

FreeRTOS also offers thread-safe locks. A thread-safe lock uses a counter as its data. Programmers can also initialize the counter. Two functions are provided for thread-safe locks. The \texttt{Give()} function increments the counter without blocking. If the counter is not zero, the \texttt{Take(delay)} function decrements the counter by one. Otherwise, the calling task is blocked for the duration specified by \texttt{delay}. Particularly, \texttt{Take(0)} returns a failure immediately when the thread-safe lock is zero at the time of invocation.

Thread-safe locks are used to implement mutexes or semaphores for task synchronization. For mutexes, tasks acquire a lock with the \texttt{Take(delay)} function. Not until the lock owner releases the lock with the \texttt{Give()} function can another task owns the lock. For semaphores, locks can be taken by a task and released by either a task or an interrupt handler.

Since thread-safe structures are widely used in FreeRTOS applications, they are also formalized in our models. Thanks to our ARM Cortex-M4 interrupt model and FreeRTOS scheduler model, our thread-safe structure models mostly follow the FreeRTOS ARM Cortex-M4 port.

8 Applications

To illustrate its features and demonstrate recommended programming styles, FreeRTOS provides example applications. Particularly, mutexes and semaphores are used for task synchronization. Thread-safe queues are also found in several applications for message passing.

8.1 Mutexes and Semaphores

\texttt{Recmutex} is an example application to illustrate priority inheritance in mutexes. Three tasks with different priorities are created in the application. They also share a mutex. Initially, the mutex is taken by the task with the high priority. After it releases the mutex, the task with the high priority suspends itself. The mutex is then taken by the task with the medium priority. Similarly, the task with the medium priority suspends itself after the mutex is released. The mutex is thus taken by the task with the low priority. Before releasing the mutex, the running task resumes the others. Because of priority inheritance, the priority of the running task should be raised. After the mutex is released, the running task recovers its low priority.

\texttt{Semtest} uses semaphores for task synchronization. The application contains two pairs of tasks. The tasks in each pair share a binary semaphore with its counter initialized to one. Both try to acquire the semaphore by calling \texttt{Take(delay)}. When a task acquires the semaphore, it will release the semaphore with the \texttt{Give()} function. The two task pairs however use different strategies to acquire semaphores. In the first pair, both tasks call \texttt{Take(0)} to acquire the semaphore. Since \texttt{delay} is zero, no task will be blocked. Rather, a failure is returned to the task without semaphore immediately. The
task without semaphore will yield the processor for the next attempt. In the second task pair, both tasks call the `Take(delay)` with a non-zero delay. The task without semaphore is hence blocked. It will be unblocked when the semaphore is released.

### 8.2 Queues

The `BlockQ` application demonstrates how to use thread-safe queues. The application consists of three task pairs. Each task pair contains a producer task and a consumer task. The producer task sends consecutive numbers through a thread-safe queue with the `Send(delay)` function. The consumer task receives numbers from the queue with `Receive(delay)`. Priorities and delay parameters are different in each task pair.

In the first pair, the producer task has the high priority but the consumer task has the low priority. The producer task also calls `Send(delay)` with a non-zero delay but the consumer task calls `Receive(0)` without blocking. In the second pair, the producer task has the low priority and the consumer task has the high priority. The producer task calls the non-blocking `Send(0)` function. The consumer task on the other hand calls `Receive(delay)` with a non-zero delay. Finally, both producer and consumer tasks have the low priority and invoke the thread-safe queue functions with non-zero delay.

Tasks in `BlockQ` behave very differently in different scheduling policies. Consider the first task pair where the producer task has a higher priority than the consumer task. Suppose the producer task is blocked by `Send(delay)` and then unblocked by the consumer task's `Receive(0)`. In preemptive scheduling, the consumer task is preempted by the FreeRTOS scheduler and the producer task continues its execution. The queue will not be empty when the consumer task resumes its execution later. In cooperative scheduling, the consumer task is not preempted when it calls `Receive(0)`. If the consumer task never yields, the producer task will not execute. The queue hence will become empty. The consumer task will then be blocked by `Receive(0)` eventually. No progress can be made in the first task pair. To ensure progress, low-priority tasks in `BlockQ` always yield in cooperative scheduling.

Using our thread-safe data models, it is almost straightforward to build models for `Recmutex`, `Semtest`, and `BlockQ`. We have indeed constructed formal models for several FreeRTOS example applications such as `PollQ`, `QPeek`, `Dynamic`, `Countsem`, and `GenQTest`. These applications are selected because they illustrate task synchronization and thread-safe structures in FreeRTOS. They are useful in our formal analysis of the FreeRTOS scheduler on ARM Cortex-M4 processors.

### 9 Formal Properties

It is impossible to analyze the FreeRTOS scheduler formally without formal properties. Such properties nevertheless are not always obvious. In real systems like FreeRTOS, high-level properties cannot be established without caveats. Without necessary provisions, formal properties could be contrived or even meaningless. In order to avoid contrived formal properties, we verify assertions in FreeRTOS example applications.

FreeRTOS developers annotate example applications with many assertions for testing. If a particular task schedule results in an assertion failure, it indicates an unintended behavior in an example application. In our analysis, we aim to prove the absence of assertion errors among all task schedules in our formal models. Since assertions are annotated by FreeRTOS developers, they are not contrived. Our models moreover simulate the ARM Cortex-M4 interrupt mechanism, the FreeRTOS scheduler, task synchronization, and thread-safe structures. Assertion errors found in our models likely correspond to assertion failures in FreeRTOS example applications. Our formal analysis is realistic as well.

Not all assertions are similar however. To organize our presentation, we classify assertions in FreeRTOS example applications into two categories. Intuitively, an assertion specifies a safety property if it indicates that a bad event should never happen; an assertion specifies a liveness property if it indicates that a good event should always happen.

#### 9.1 Safety

It is straightforward to specify safety properties with assertions. Programmers only need to write a Boolean expression deemed to be true in an assertion. In FreeRTOS example applications, the following safety properties are found:

- **(S0)** If a task is delayed for synchronization with other tasks, other tasks must finish before the delay duration expires.
- **(S1)** If a task is blocked by a thread-safe data, the data must be ready when the task is unblocked.
- **(S2)** If a task expects a thread-safe data to be ready, the data must be ready.
- **(S3)** Messages received through a thread-safe queue must preserve their order.
- **(S4)** Mutexes and binary semaphores must ensure mutual exclusive execution of critical sections.
- **(S5)** Frequencies of `Take(delay)` and `Give()` must be equal.
- **(S6)** A low-priority task must inherit priorities when its mutex was taken by tasks with higher priorities.

Property (S0) checks if basic task synchronization is used properly. When a task is delayed, the delayed duration must be sufficient for other tasks to finish their works. Property (S1) checks if thread-safe data are implemented correctly. When a
task is unblocked before its duration expires, the thread-safe data must be ready. Property (S2) is a special case of property (S1) where the parameter $delay$ is zero. Property (S3) checks that messages are delivered in order by thread-safe queues. Properties (S4) and (S5) check mutexes and semaphores are implemented correctly. Finally, property (S6) checks whether priority inheritance is implemented.

Not all properties are required in every application. Table 1 shows the safety properties specified in the eight FreeRTOS example applications.

### 9.2 Liveness

If a task does nothing, no bad event can happen. The task thus satisfies all safety properties. To avoid such vacuous safety, liveness properties are needed. Indeed, FreeRTOS developers write assertions to ensure tasks are making progress. To check progress by assertions, a task maintains a counter. The task increments the counter when its job is finished. Another task is added to check the counter periodically. It is an assertion failure if the counter remains unchanged between checks.

Adding a task to check progress is fine, but the added check task does not really contribute to the work of application. Precious energy and processor cycles are consumed by the check task. More importantly, the check task needs to be scheduled. Task schedules would be different should the check task be removed from its application. If an application is tested with a check task, it needs to be shipped with the check task in the final product. Otherwise, test results are debatable because task schedules necessarily change without the check task.

Such a dilemma is resolved in our formal analysis easily. Instead of checking progress in a task, we specify the liveness property with an LTL formula. Since the logic formula is not an execution unit, it has no impact on task schedules. Actually, the formula is not even a part of our formal models. Model behaviors cannot be changed. Formal models allow us to check progress without adding check tasks. Our analysis is valid for final products without check tasks.

Precisely, let $Loc_{SysTick}$ be the location triggering the SysTick interrupt and $Loc_i$ the location where task model $i$ finishes its job for $1 \leq i \leq n$. Consider the LTL formula:

$$\square \diamond Loc_{SysTick} \rightarrow (\square \diamond Loc_1 \land \square \diamond Loc_2 \land \cdots \land \square \diamond Loc_n.)$$

Informally, the formula states that all tasks finish their jobs infinitely many times if the SysTick interrupt is triggered infinitely many times. In our formal models, SysTick interrupts represent the progression of time. If the LTL formula is satisfied in our models, it means that all task models must finish their jobs infinitely often as time progresses. In other words, no task can stop making progress indefinitely. We verify this liveness property in place of assertions from check tasks in our formal analysis. The liveness property is required for all FreeRTOS application models (Table 1).

### 10 Verification Results

For each scheduling policy, we use the model checker SPIN to verify properties shown in Table 1. The model checker first verifies whether there is any assertion error for safety properties in an application model. After checking safety properties, SPIN is used again to verify the liveness property on the application model. In our experiments, we use SPIN 6.5.1 on an Ubuntu 20.04 server with two 3.2GHz octa-core CPUs and 512GB RAM.

Table 2 gives the verification results for safety properties in eight example applications under three scheduling policies. If all safety properties in an application are satisfied, the verification time (in seconds) is shown. If not, the failed property is shown with a cross mark in the table. For the liveness property, verification time is shown if an application satisfies the property. A cross mark represents that an application does not satisfy the liveness property.

### 10.1 Analysis of Safety Properties

Almost all applications satisfy their safety properties. SPIN finishes the verification with at most 56GB of memory in 16 minutes. For failed safety properties, the model checker also reports error traces with 10GB memory in 1 minute.

Under preemptive scheduling with time slicing, SPIN finds that the application models $Dynamic$ and $BlockQ$ violate safety properties (S0) and (S1) respectively. In error traces reported by SPIN, we find that a task may not execute even though it is scheduled by the FreeRTOS scheduler. To see how it happens, consider the SysTick interrupt triggers while the PendSV interrupt handler model is running. Since both interrupts have the same priority, the SysTick interrupt is pending until the PendSV interrupt handler model finishes. Recall that the PendSV interrupt handler model calls the scheduler model to elect a task model for execution. Let us call the elected task model as the victim. The victim task model is scheduled to execute after the exception return macro. However, the SysTick interrupt is still pending. Due to tail chaining, the SysTick interrupt handler model will execute before the victim
task. In the time slicing policy, the SysTick interrupt handler mode will trigger the PendSV interrupt to schedule a task model. The scheduler model incorrectly believes the victim task model has used up its time slice and chooses another task model for execution. The victim task model hence misses its time slice for execution. In error traces, the victim task model repeatedly misses its time slice and hence cannot prepare the thread-safe queue shared with another blocked task. When the blocked task expires its duration, the shared thread-safe queue is still not ready. Eventually, the models Dynamic and BlockQ violate safety properties (S0) and (S1) respectively.

Although assertion errors are found in our formal analysis, they are not necessarily failures in reality. It is important to recall that our application models are not FreeRTOS example applications. During model construction, abstraction and simplification are indispensable for effective formal analysis. For instance, the SysTick interrupt is not triggered periodically in our formal models because the PROMELA modeling language is timeless. Error traces found by SPIN are only realistic but never real. It is just as important to reproduce assertion failures in real hardware for assertion errors found in formal analysis. To this end, we install the FreeRTOS ARM Cortex-M4 port on the STM32F429I-DISC1 board with an ARM Cortex-M4 processor and modify FreeRTOS example applications to reproduce SPIN example applications on the board. If an assertion failure does occur, an on-board LED will flash with high frequency to indicate the failure.

The failed safety properties in Dynamic and BlockQ under preemptive scheduling with time slicing are successfully reproduced on STM32F429I-DISC1. Consider the safety property (S1) in BlockQ. We add a task to the example application. When the added task is scheduled for execution, it runs for the time slightly shorter than the SysTick period and then yields. After the added task yields, the FreeRTOS scheduler will choose, for example, a producer task in BlockQ. The elected producer task will be the victim. While the FreeRTOS scheduler is electing the victim task, the SysTick interrupt is triggered but remain pending. As described above, the victim task will be preempted before it executes. An assertion failure in the victim producer task is observed.

In reality, the SysTick interrupt may not be triggered shortly after the added task yields. The added task simply repeats itself whenever it is scheduled for execution. The assertion failure will be observed eventually. The failed safety property (S0) in Dynamic is reproduced similarly. Two assertion failures are found by our formal analysis successfully.

After reproducing the failures, we find that similar pattern had been independently exploited. Tsafrir et al. [36] made non-privileged applications arbitrarily monopolize processors by controlling processor cycles between two clock ticks. They concluded that any periodically ticking system at that time is vulnerable to their exploit. Their exploit and our reproduction are similar in controlling processor cycles between ticks, but different in the cause of the problem.

### 10.2 Analysis of Liveness Property

Table 2 also reports verification results for the liveness property in all example application models under different scheduling policies. SPIN uses up to 212GB of memory within 17 minutes for each verification run. Many example application models do not satisfy the liveness property.

#### 10.2.1 Liveness under cooperative scheduling

Only one application model fails to satisfy the liveness property in Table 2a. The error trace reported by SPIN shows that two of the task models in Semtest never yield. Recall that the first task pair in Semtest have zero delay (Section 8.1). Since preemption is disabled, other task models cannot be scheduled for execution. Both task models in the first task pair are moved to the waiting task queue. No progress can be made as time progresses. The liveness property fails.

It is easy to reproduce the error on the STM32F429I-DISC1 board. We configure FreeRTOS to use the cooperative scheduling policy. The on-board LED indicates an assertion failure without modifying the FreeRTOS example application.
10.2.2 Liveness under preemption without time slicing

The application models \textit{Semtest}, \textit{Countsem}, \textit{GenQTest}, and \textit{Dynamic} violate the liveness property under the preemptive scheduling without time slicing (Table 2b). After examining their error traces, we find a task model never yields and other task models are not delayed in each model. Since time slicing is not enabled, the SysTick interrupt handler model does not trigger the PendSV interrupt. No task model will be scheduled for execution. When thread-safe structures become not ready, never-yielding task models will be moved to waiting task queues. No progress can be made afterwards. The liveness property subsequently fails.

It is easy to reproduce assertion failures in \textit{Semtest}, \textit{Countsem}, and \textit{GenQTest}. After configuring FreeRTOS with the scheduling policy, assertion failures in check tasks are observed without any modification.

Most interestingly, \textit{Dynamic} does not have assertion failures under preemptive scheduling without time slicing. Contrary to our formal models, recall that additional tasks are used to check progress in these example applications (Section 9.2). These check tasks have the highest priority with non-zero delays. The never-yielding task in \textit{Dynamic} is preempted by its check task periodically; other tasks will then be scheduled for execution. Progress can still be made because of the check task in \textit{Dynamic}. To reproduce the assertion failure in \textit{Dynamic}, we have to change the execution order of consumer and producer tasks in the example application. After this simple modification, an assertion failure in the check task is observed in \textit{Dynamic}.

10.2.3 Liveness under preemption with time slicing

Surprisingly, the liveness property fails in almost all application models under preemptive scheduling with time slicing. After examining error traces, the problem in Section 10.1 is observed again. When the SysTick interrupt is triggered while the PendSV interrupt handler model is running, recall that a victim task model will miss its chance of execution. In the extreme scenario, a task model can be the victim whenever it is scheduled. The victim task model will never execute and starve. The liveness property hence fails.

It can be very tricky to reproduce the starvation on real hardware. As a proof of concept, we choose the example application \textit{Countsem} with two never-yielding tasks to reproduce the error. The idle task is configured to yield in the application. Similar to Section 10.1, we add a new task to \textit{Countsem}. The added task occupies the ARM Cortex-M4 processor for a fixed time. It ensures the SysTick interrupt is triggered shortly after the idle task yields. When the idle task yields, a task is elected and becomes the victim. The second task will be elected. After the second task finishes its execution, the added task repeats and forces the first task to be the victim again.

Incidentally, \textit{PollQ} satisfies the liveness property. We observe two factors that make \textit{PollQ} immune from the problem in Section 10.1. First, other tasks have higher priorities than the idle task. This prevents the idle task from preempting the next task when the idle task should yield the processor. Second, tasks in \textit{PollQ} delay themselves after synchronization. Recall that a running task may unblock others through the thread-safe structure. If the unblocked tasks have the priority, the running task is preempted. When the preempted task continues its execution, it then delays itself. The delay can prevent the executing task from repeatedly preempting the next task. Based on these factors, we propose a fix for the problem. The first step is to disable the idle task from yielding the processor. The second step is to delay the tasks that will definitely yield the processor by being preempted. The proposal is not the most efficient fix due to additional delays, but it can alleviate the problem without modifying the FreeRTOS kernel code.

10.3 Discussion

In our formal analysis, we find three types of assertion failures in FreeRTOS example applications. Section 10.1 reports assertion failures where a task may be preempted before its scheduled execution. Under preemptive scheduling with time slicing, the FreeRTOS scheduler can be invoked twice by consecutive executions of the PendSV and SysTick interrupt handlers. The task elected by the first invocation is preempted by the second invocation before its scheduled execution. A task therefore may not execute after it is scheduled. To observe such failures, the PendSV and SysTick interrupts need to be synchronized. Testing is unlikely to reveal such failures. We are not aware of any report about such assertion failures.

The second type of assertion failures are reported in Section 10.2.2. Under preemptive scheduling without time slicing, never-yielding tasks can lead to starvation when they use thread-safe structures. In this case, other tasks cannot be scheduled because never-yielding tasks are running. When thread-safe structures become not ready, never-yielding tasks are moved to waiting task queues and applications cannot progress. The second type of assertion failures can be elusive. Since FreeRTOS example applications add tasks to check progress. Because these check tasks change FreeRTOS scheduling, starvation may not happen. Even though check tasks do not contribute to computation actively, applications must be shipped with check tasks to prevent starvation. This is perhaps the most interesting lesson learned from our formal analysis.

Section 10.2.3 reports the third type of assertion failures. These failures are closely related to the first type. In the extreme scenario, a task is always preempted before its scheduled execution. The victim task cannot progress. It is almost impossible for testing to find such assertion failures. Yet we have successfully produced it in a FreeRTOS example appli-
cation with the help of our formal analysis.

11 Related Work

Many works had applied formal methods on FreeRTOS. Chong et al. [10,12] from the Amazon Web Services team formally verified the FreeRTOS’s task and queue implementation against memory safety such as buffer overflow, use after free, or NULL pointer dereferences. They propose a process to check the software in development [11] with Bounded Model Checking [14]. Chandrasekaran et al. [8] modeled a custom implementation of multi-core FreeRTOS in PROMELA. They used SPIN to verify their model against data-race and deadlock. Besides model checking, some works choose theorem proving. The scheduler [21] and the list data structure [34] of FreeRTOS were proved memory correctness with separation logic. Other works modeled the FreeRTOS scheduler in the B method [18] or the Z notation [9]. Both of the works proved FreeRTOS task invariants such as the running task always has the top priority. Divakaran et al. [19] verified the FreeRTOS scheduler with refinement-based method. Specifically, the method not only checks functional correctness but also proves that their abstraction in the Z notation is refined by the FreeRTOS implementation. In automata-based modeling method, Asadollah et al. [3] applied runtime verification on FreeRTOS. They parsed FreeRTOS’ runtime events to discover concurrent bugs such as deadlock and starvation. None of the above works considers architecture effects such as tail chaining. Architecture effects are highly relied on interrupt handling that often changes the processor context at runtime.

Some works considered hardware interrupts and preemption. Feng et al. [20] provided a Hoare-logic-like framework for certifying low-level system programs with interrupts enabled. Xu et al. [37] also provided a framework for specifying kernel behaviors with preemption and nested interrupts enabled. They further verified the kernel μC/OS-II against priority inversion. Our work has a similar goal, but further involves specific architecture effects.

As for other verified real-time kernels, de Oliveira et al. [16] modeled thread behaviors in the Linux PREEMPT_RT kernel based on automata. In the expansion of [16], de Oliveira et al. [17] developed a Linux kernel module to keep checking Linux runtime events are allowed by the automata model. Their method is efficient at finding mismatching behaviors between the logged events and the model. Hladik et al. [25] proposed an integrated tool to design, verify, and execute a real-time system. Their tool can guarantee that real-time tasks are executed in time constraint. Real-time tasks are C functions. They are managed by the tool and executed in a Linux PREEMPT_RT kernel at a specific tick frequency. Andronic et al. [2] proved the eChronos real-time operating system against the scheduling policy that the running task has the top priority. Other works analyzed response time with model checking or theorem proving. Guo et al. [24] verified communications in an in-vehicle network against timed properties. They abstracted nodes from the network and verified the abstraction with the timed model checker UPPAAL [6]. Cerqueira et al. [7] provides PROSA for proving task scheduling and response time. Their framework can be checked by the Coq theorem prover. Guo et al. [23] applied PROSA to RT-CertiKOS for further analysis.

Besides real-time kernels, notable verified microkernel seL4 [29] is proved functional correctness and their abstract model is also validated [35]. CertiKOS [22] is a concurrent operating system and supports multicore. Gu et al. proved that the CertiKOS implementation refines its specifications. Nelson et al. [33] developed an operating system kernel that is amenable to automated reasoning using satisfiability modulo theories solvers. In contrast to the above, we choose to validate our abstract model by reproducing the reported errors in real hardware.

12 Conclusion

We have presented a formal model for the FreeRTOS scheduler and a number of standard FreeRTOS applications on ARM Cortex-M4 cores. The standard FreeRTOS applications contain assertions to specify expected behaviors. By model checking, we find several assertion errors when we verify some application models under certain scheduling policies. Those assertion errors are analyzed and reproduced on a physical development board with the ARM Cortex-M4 core.

Based on our formalization of the ARM Cortex-M4 interrupt mechanism, the FreeRTOS scheduler model is specified almost naturally. Interrupt mechanisms in different architectures are also exploited in various FreeRTOS ports. How to generalize our methodology of formalization would be an interesting future work for formal analysis of other FreeRTOS ports. Specifically, we plan to model FreeRTOS SiFive HiFive1-RevB port to analyze how RISC-V architecture affects the FreeRTOS scheduler. Another future work is to model the official distribution of FreeRTOS symmetric multiprocessing [27] and consider the effect of memory model.

Availability

Our model is available at https://github.com/kaizsv/FreeRTOS-Spin and the reproduction is available at https://github.com/kaizsv/FreeRTOS-Spin-Reproduction.

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