Research on dynamic current sharing method of parallel connected IGBT modules for NPC three level converters

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Abstract. The parallel connection of IGBTs has been being applied in high power neutral point clamped (NPC) three level converters. This paper investigates the impact of gate parameters (gate resistor and capacitance) on dynamic current imbalance of parallel connected IGBT for NPC three level converter. A gate parameters calculation method is proposed in the paper, and the delay time and collector current difference can be analysed quantitatively. Experimental results have shown the effectiveness of the method.

1. Introduction
Multilevel converters have been attracting particular attention for high power applications such as marine electric propulsion. Insulated gate bipolar transistor (IGBT)-based the neutral point clamped (NPC) three level converters are widely studied topology. Although the output current ratings of these high power IGBT modules are steadily increasing, the parallel operations of IGBT modules are commonly adopted to reach higher output currents as are required by high power converter applications.

However, parallel operation of IGBT modules require a careful selection of IGBT modules and the special design of gate driver. Besides, although the parallel operation of IGBT modules expands the capacity of the high power NPC converters, it is difficult to maintain the complete consistency of the output current of parallel branches, which brings the problem of static and dynamic current imbalance due to the difference of internal parameters of each module and the asymmetry of circuit topology and driving circuit layout.

Figure 1 shows the definitions of static and dynamic current imbalance. The former means that the IGBT modules bears different current when in steady-state operation, and the latter means that the IGBT module bear unequal currents at the moment of switching action. Both of these two situations cause current imbalance and heat distribution imbalance of the device, and even damage the IGBT modules in serious cases.
The degree of current imbalance can be defined as

\[ i_{\text{cin}} = \frac{|i_{c1} - i_{c2}|}{i_{c1} + i_{c2}} \]  \hspace{1cm} (1)

Current balancing influence factors of parallel connected IGBT modules relate to static and dynamic cases. The former includes collector-emitter saturation voltage (\(V_{\text{cesat}}\)), collector current, junction temperature and equivalent resistance of commutation circuit, the latter includes gate threshold voltage (\(V_{\text{GTh}}\)), gate capacitance, gate resistor, junction temperature, stray inductance, gate driver, diode reverse recovery characteristics, load characteristics.

In the field of high power converter, many efforts have been made to achieve equal current sharing in the parallel connected IGBT modules. [1] proposed to control the gate conduction time and gate emitter voltage by checking the load current or emitter current to achieve current balance. The dynamic current imbalance in IGBT parallel connection is analyzed in [2], gate resistance compensation method is proposed in [3] to realize IGBT parallel current equalization. The realization of IGBT parallel current balance by gate resistance compensation method is demonstrated in [4-5], and the selection of resistance parameters is analyzed. Generally, the dynamic current sharing methods are more important to implement. Among the methods, optimization of gate resistor and gate capacitance are most feasible for high power NPC three level converters because,

- Change of Commercial IGBT module parameters is impossible
- The overall dimension of IGBT module is large, and each IGBT module generally adopts an independent drive board
- The commutation loops in busbar are different and complex, and the commutation loops of parallel connected IGBT modules are difficult to be symmetrical, which makes the stray inductances of commutation loops to be different

This paper studies the current sharing of parallel IGBT module of high power NPC three-phase converter, focusing on determination of gate resistor and gate capacitance to improve the dynamic current balance of parallel module.

2. Gate parameters analysis for current sharing

Figure 2 shows a circuit configuration of one phase of the IGBT-based NPC three level converters. Each phase contains four IGBT units and two diode units. Each IGBT unit includes two parallel connected IGBTs. In high power converters, the IGBT modules, diode modules, absorption capacitors and temperature sensors are generally installed on the barbus, which is necessary to form a power unit.
The commutation loops of NPC three-level converter are complex, and the commutation of parallel IGBT module are difficult to be symmetrical. As a result, the stray inductance of the parallel connected IGBT modules are different.

As shown in Figure 2, the turn-on and turn-off of IGBT can be approximately regarded as the charge and discharge process of a voltage source to a resistance-capacitance circuit. $R_g$ and $C_g$ are the gate resistance and gate capacitance set by the IGBT drive, respectively, and $C_{gi}$ is the gate equivalent input capacitance of the IGBT module.

The amplitude of turn-on and turn-off current pulse and the rise rate of gate voltage can be limited by adjusting the gate resistance and capacitance, that is, the smaller gate resistance and capacitance are, the shorter the gate turn-on and turn-off time are, and the the switching loss is reduced. Therefore, changing the gate parameters can affect the dynamic current sharing of IGBT modules.

For the IGBT-based NPC three level converters shown in Figure 3, the detailed gate drive circuit for two parallel connected IGBT modules could be shown in Figure 4, in which the inherent stray capacitors ($C_{gei}$, $C_{gci}$ and $C_{cei}$) are considered as well. $R_{g1}$, $R_{g2}$, $C_{g1}$, $C_{g2}$ are the gate resistance and gate capacitance set by the first and the second IGBT drive, respectively, $L_{o1}$, $L_{o2}$ ($L_{o1} \neq L_{o2}$) are the stray inductance of the two parallel connected IGBT modules.
IGBT turn-on delay time \((td)\) is greatly affect the transient current balancing of parallel connected IGBT modules.

The turn-on delay time for the two parallel connected IGBTs are calculated as

\[
t_{d1} = -\tau_1 \times \ln \left(1 - \frac{V_{GEb}}{V_{GE}}\right)
\]

\[
t_{d2} = -\tau_2 \times \ln \left(1 - \frac{V_{GEb}}{V_{GE}}\right)
\]

where the time constant \(\tau_1\) and \(\tau_2\) are

\[
\tau_1 = R_g1 \times (C_{g1} + C_{ge1} + C_{ce1})
\]

\[
\tau_2 = R_g2 \times (C_{g2} + C_{ge} + C_{ge2})
\]

The delay time difference then can be obtained

\[
\Delta t_d = t_{d1} - t_{d2} = \ln \left(1 - \frac{V_{GEb}}{V_{GE}}\right) (\tau_1 - \tau_2)
\]

In Figure 4, if \(L_{g1} > L_{g2}\), the difference between the collector current of the two parallel connected IGBT modules is described as

\[
\Delta i_{c_{\text{max}}} = \begin{cases} 
0 & t \leq \min(t_{d1}, t_{d2}) \\
1_{\Delta t_d} & t = \max(t_{d1}, t_{d2})
\end{cases}
\]

where

\[
k_1 = \frac{V_{GE} - V_{GEb}}{\tau_1 / g_{fs1} + L_{g1}}
\]

and \(g_{fs}\) is the forward transconductance.
if \( L_\sigma 1 > L_\sigma 2 \), the difference between the collector current of the two parallel connected IGBT modules is described as

\[
\Delta i_{c,max} = \begin{cases} 
0 & t \leq \min (t_{d1}, t_{d2}) \\
\frac{k_2 \Delta t_d}{k_2} & t = \max (t_{d1}, t_{d2}) 
\end{cases}
\]  \hspace{1cm} (9)

where

\[
k_2 = \frac{V_{GE} - V_{GE(\theta)}}{\tau_2 / g_f + L_\sigma 2}
\]  \hspace{1cm} (10)

In order to obtain the minimum \( \Delta i_c \), the Lagrange multiplier method can be used to analyze the minimum of the function

\[
f = \frac{(V_{GE} - V_{GE(\theta)}) \times \ln \left(1 - \frac{V_{GE(\theta)}}{V_{GE}}\right) \times (\tau_1 - \tau_2)}{\tau_1 / g_f + L_\sigma 1}
\]  \hspace{1cm} (11)

and leads to

\[
\begin{align*}
R_g 1 (C_{g1} + C_{g\sigma 1} + C_{g\sigma 1}) &= g_f 1 L_\sigma 2 \\
R_g 2 (C_{g2} + C_{g\sigma 2} + C_{g\sigma 2}) &= g_f 2 L_\sigma 1
\end{align*}
\]  \hspace{1cm} (12)

Careful selection of IGBT pairs is generally enough to ensure \( C_{g\sigma 1} = C_{g\sigma 2} \), \( C_{g\sigma 1} = C_{g\sigma 2} \) and \( g_f 1 = g_f 2 \), and they could be obtained in manufacture materials. \( L_\sigma 1 \) and \( L_\sigma 2 \) could be obtained using test or finite element calculation method. \( R_g 1 \) and \( R_g 2 \) can not be too large in order to limit switching loss. The selection of \( R_g \) and \( C_g \) interact and \( R_g \) is suggested to be obtained first.

3. Experimental verification

Experimental study presented in this paper is based on Infineon IGBT modules FZ3600R17HP4 and DIODE module DZ3600S17K3.

The test circuit configuration for the characterization of IGBT under hard switching condition is illustrated in Figure 6. A set of two pairs of IGBT modules is connected in parallel in the experimental setup (Figure 7). The middle parallel pair of IGBT modules are devices under test (T_1 location) while other pairs of IGBT modules remain under passive mode. The load inductor Lload is set to 400uH. The stray inductance \( L_\sigma 1 \) and \( L_\sigma 2 \) in the test circuit are tested to be can be 74uH and 49uH, respectively.

![Figure 6. Test circuit](image-url)
Figure 7. Test bed

The original IGBT driving board parameters are $R_{g1} = 3 \ \Omega$, $R_{g2} = 2 \ \Omega$, $C_{g1} = 4.7\mu F$, $C_{g2} = 3.9\mu F$. According to (12) and IGBT module parameters, and keep the gate resistance unchanged, it is calculated that $C_{g1} = 5.6\mu F$, $C_{g2} = 7.1\mu F$.

Different gate parameters are used to test the imbalance of $I_c$ of the two parallel connected IGBT located on T1, the result is shown in Figure 8 and Table 1. It can be seen that the current imbalance is reduced from 21.76% to 11.21%, which is beneficial to the safe operation of IGBT modules.

![Figure 8. Imbalance of $I_c$ test results](image)

| Gate parameters | Imbalance of $I_c$ |
|-----------------|-------------------|
| $R_{g1} = 3 \ \Omega$, $R_{g2} = 2 \ \Omega$, $C_{g1} = 4.7\mu F$, $C_{g2} = 3.9\mu F$ | 21.76% |
| $R_{g1} = 3 \ \Omega$, $R_{g2} = 2 \ \Omega$, $C_{g1} = 5.6\mu F$, $C_{g2} = 7.1\mu F$ | 11.21% |

4. Conclusion
This paper investigates the impact of gate parameters (gate resistor and capacitance) on dynamic current imbalance of parallel connected IGBT for NPC three level converter. A gate parameters calculation
method is proposed in the paper, and the delay time and Ic difference can be analyzed quantitatively. Experimental results have shown that the current imbalance is reduced from 21.76% to 11.21%.

References
[1] Hofer, R, Karrer, N., Gerster, C. (1996) Paralleling intelligent IGBT power modules with active gate-controlled current balancing. Proceedings of IEEE Power Electronics Specialists Conference (PESC), 2:1312-1316.
[2] Hofer-Noser P, Karrer N. (1999) Monitoring of paralleled IGBT/diode modules. IEEE Transactions on Power Electronics, 14(3):438-444.
[3] Schlapbach U. (2010) Dynamic paralleling problems in IGBT module construction and application. Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on. 2010:1-7.
[4] Y. Xiao, Q. Liu, Y. Tang, L. Du and H. Ma, (2014) Current sharing model of parallel connected IGBTs during turn-on. IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, 1350-1355.
[5] R. Letor. (1992) Static and dynamic behavior of paralleled IGBTs. IEEE Transactions on Industry Applications, 28(2): 395-402