Robust and Efficient Elimination of Cache and Timing Side Channels

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ABSTRACT
Timing and cache side channels provide powerful attacks against many sensitive operations including cryptographic implementations. A popular strategy for defending against these attacks is to modify the implementation so that the timing and cache access patterns of every hardware instruction is independent of the secret inputs. However, this solution is architecture-specific, brittle, and difficult to get right. In this paper, we propose and evaluate a robust low-overhead technique for timing and cache channel mitigation that requires only minimal source code changes and works across multiple platforms and architectures. We report the experimental results of our solution for C, C++, and Java programs. Our results demonstrate that our solution successfully eliminates the timing and cache side-channel leaks and incurs significantly lower performance overhead than existing approaches.

1. INTRODUCTION
Defending against cache and timing side channel attacks is known to be a hard and important problem in computer security. Timing attacks can be used to extract cryptographic secrets from running systems \cite{25, 15, 39, 34}, spy on Web user activity \cite{12}, and even undo the privacy of differential privacy systems \cite{23, 5}. Attacks exploiting timing side channels have been demonstrated for remote attackers, where the adversary and the target are separated by a network \cite{25, 15, 39, 34} and for local attackers, where the adversary runs unprivileged spyware on the target machine \cite{33, 8, 11, 4, 44, 7, 44}.

One way to defend against remote timing attacks is to make sure that the timing of any externally observable events is independent of any data that should be kept secret. Several strategies have been proposed to achieve this, including application-specific changes \cite{27, 10, 11}, static transformation \cite{17, 19} and dynamic padding \cite{10, 41, 18, 26, 24}.

These strategies do not defend against local timing attacks where the attacker spies on the target application by measuring the target’s impact on the local cache and other resources. Some strategies for defending against local attacks include static partitioning of resources \cite{25, 34, 40, 11}, flushing state \cite{17}, obfuscating cache access patterns \cite{8, 10, 13, 37, 32}, and moderating access to fine-grained timers \cite{31, 30, 39}. We survey these methods in related work (Section 5).

A popular approach for defending against local and remote timing attacks is to ensure that the low-level instruction sequence does not contain instructions whose performance depends on secret information. This is enforced by manually re-writing the code, as was done in OpenSSL\textsuperscript{1} or by changing the compiler to ensure that the generated code has this property \cite{19}.

This popular strategy can fail to ensure security for several reasons. First, the timing properties of instructions can differ in subtle ways from one architecture to another causing this approach may produce an instruction sequence that is unsafe for some architectures. Second, this strategy can fail for languages like Java where the JVM can optimize the bytecode at runtime and inadvertently introduce secret-dependent timing variations. Third, manually ensuring that a certain code transformations prevent timing attacks can be difficult, as was the case when updating OpenSSL to prevent the Lucky-thirteen timing attack \cite{29}.

\textbf{Our contribution.} We propose the first low-overhead, cross-architecture defense that can protect against both local and remote timing attacks with minimal application code changes. We show that our defense is language-independent by applying the strategy to protect applications written in Java and C/C++. Our defense requires relatively simple modifications to the underlying OS and can run on off-the-shelf hardware.

The key insights behind our solution (Section 4) are that:

\begin{itemize}
  \item The necessary time padding can be minimized by accurately accounting for the different causes for timing variations. We eliminate timing variations that are independent of protected data (e.g., caused by interrupts, the OS scheduler, or non-secret execution flow). Our accounting ensures that the time pad is the minimum needed to prevent timing variation that depend on secret data.
  \item The OS scheduler can be leveraged to isolate a sensitive function’s execution from other untrusted processes without incurring significant performance overhead. Dynamic resource isolation techniques like page coloring can further help in isolation of shared resources. Lazy state cleansing mechanisms for shared resources can amortize the costs of state cleansing while still maintaining the security guarantees.
  \item We fully implemented our approach in Linux and show that execution times are independent of secret data and that performance overhead is low. For example, the performance overhead to protect the entire state machine running inside a SSL/TLS server against
\end{itemize}

\textsuperscript{1}In the case of RSA private key operations, OpenSSL uses an additional defense called \textit{blinding}. 
known timing- and cache-based side channel attacks is less than 8.5% in connection latency.

- We show that our solution can defend applications written in different languages like C, C++, and Java with minimal application code changes. For Java our defense is implemented by inserting a small number of native code calls into the bytecode.

Overall we obtain an efficient application-independent solution that defends against a wide range of timing- and cache-based side channel attacks.

2. KNOWN TIMING ATTACKS

Before describing our proposed defense we briefly survey different types of timing attackers. In the previous section we discussed the difference between a local and a remote timing attacker: a local timing attacker, in addition to monitoring the total computation time, can spy on the target application by monitoring the state of shared hardware resources such as the local cache.

Concurrent vs. non-concurrent timing attacks.

In a concurrent attack, the attacker can probe shared resources while the target application is operating. For example, the attacker can inspect the state of the shared resources at intermediate steps of a cryptographic operation. The attacker’s process can control the concurrent access by adjusting its scheduling parameters and its core affinity in the case of symmetric multiprocessing (SMP).

Concurrent, local attacks are the most prevalent class of timing attacks in the research literature. Such attacks are known to be able to extract the secret/private key against a wide-range of ciphers including RSA [43, 4], AES [37, 43, 22, 32], and ElGamal [46]. These attacks exploit information leakage through a wide range of shared hardware resources: the L1 or L2 data cache [37, 33, 22, 32], instruction cache [1, 40], branch predictor cache [2, 3], floating-point multiplier [4], and the L3 cache [43, 24].

A non-concurrent attack is one in which the attacker only gets to observe the timing information or shared hardware state at the beginning and the end of the sensitive computation. For example, a non-concurrent attacker can extract secret information using only the aggregate time it takes the target application to process a request.

All existing remote attacks are non-concurrent, however this is not fundamental. A hypothetical remote, yet concurrent, attack would be one in which the remote attacker submits a request to the victim application at the same time that another non-adversarial client makes requests to the victim application. The attacker would then use the timing information collected from this setup to learn something about the non-adversarial client’s communication with the server.

There are several known local non-concurrent attacks as well. Osvik et al. [32], Tramer et al. [57], and Bonneau and Mironov [14] present two types of local, non-concurrent attacks against AES implementations. In the first, prime and probe, the attacker “primes” the cache, triggers an AES encryption, and “probes” the cache to learn information about the AES private key. The spy process primes the cache by loading its own memory content into the cache and probes the cache by measuring the time to reload the memory content after the AES encryption has completed. This attack involves the attacker’s spy process measuring its own timing information to indirectly extract information from the victim application. Alternatively, in the evict and time strategy, the attacker measures the time taken to perform the victim operation, evicts certain chosen cache lines, triggers the victim operation and measure its execution time again. By comparing these two execution times, the attacker can find out which cache lines were accessed during the victim operation. Osvik et al. were able to extract an 128-bit AES key after only 8,000 encryptions using the prime and probe attack.

3. THREAT MODEL

We allow the attacker to be local or remote and to execute concurrently or non-concurrently with the target application.

We assume that the attacker can only run spy processes as a different non-privileged user (i.e., without super-user privileges) than the owner of a target process. We also assume that the spy process cannot bypass the standard user-based isolation provided by the OS. We believe that these are very realistic assumptions because if either one of these assumptions fail, the spy process can steal the user’s sensitive information without resorting to side channel attacks in most existing OSes.

We assume that the operating system and the underlying hardware are trusted. Similarly, we assume that the attacker does not have physical access to the hardware and cannot monitor side channels such as electromagnetic radiations, power use, or acoustic emanations. We are only concerned with timing and cache side channels since they are the easiest side channels to exploit without physical access to the victim machine.

4. OUR SOLUTION

In our solution, a developer first annotates the sensitive computation(s) in their code that they would like to protect at the granularity of functions. For the rest of the paper, we refer to such functions as protected functions. Our solution ensures that the code inside the protected functions, all other functions that may be invoked as part of their execution, and all the secrets that they operate on are protected from timing attacks. We also support nested protected functions i.e. one protected function can call other protected functions. Our solution instruments the protected functions such that our stub code is invoked before and after execution of each protected function.

We defend a protected function against all known forms of timing attacks—remote, local non-concurrent, and local concurrent attacks—using two high-level mechanisms.

Time padding. We use time padding to defend against remote timing attacks and any local attack that measure the end-to-end runtime of a protected function. Essentially, we pad the protected function’s execution time to its worst-case runtime. Time padding has been used in past proposals [6, 11, 18, 28, 23], however previous solutions incurred high performance overheads. Our main contributions here are twofold:

- Computing the padding amount adaptively by separating out the secret-dependent sources of timing variations from external secret-independent sources (i.e., OS scheduler, interrupt handlers, etc.) and
• Designing a safe padding mechanism that avoids the information leakage occurring under naive padding approaches.

We show that time padding can be implemented efficiently while ensuring strong security guarantees.

A safe time padding scheme defends against attackers that measure the duration of a protected function using the timestamp counter or any other measure of real time. However, most modern hardware often also contain performance counters that keep track of different performance events such as the number of cache evictions or branch mispredictions occurring on a particular core. A local attacker with access to these performance counters may infer the secrets used during the sensitive computation despite time padding. Our solution, therefore, restricts access to performance monitoring counters so that a user’s process cannot see detailed performance metrics of another user’s processes. We do not restrict, however, a user from using hardware performance counters to measure the performance of their own processes.

**Shared resource isolation.** Our solution also prevents information leakage through shared resources across different users’ processes. We do this by dynamically reserving exclusive access to a physical core (including all per-core caches such as L1 and L2) while it is executing a sensitive function. This ensures that a local attacker does not have concurrent access to any per-core resources while a protected function is accessing them. We lazily clean the state left by the protected function in any of the per-core resources before handing them over to untrusted processes. Finally, we use page coloring to ensure that protected functions of a user do not perform any accesses outside of a reserved portion of the L3 cache, and to ensure that this reserved portion is not shared with other users. This ensures that the attacker cannot infer information about protected functions through the L3 cache.

We describe the components of time padding and shared resource isolation in detail next.

### 4.1 Time padding

#### 4.1.1 Computing the adaptive padding threshold

One key insight behind our solution is that there are two major sources of variation in a protected function’s execution time: secret-dependent variations and secret-independent variations. For example, program delays caused by the OS scheduler preemptions or interrupt handling are independent of accesses to a program’s secret data inside protected functions. Existing implementations of time padding incur extremely high overheads because they try to pad the execution time up to the worst-case in the presence of a large number of secret-independent variations. However, in our solution, we separate out the secret-independent variations from the secret-dependent ones and compute the padding amounts for these two cases separately. Most modern OSes like Linux keep track of the number of such external preemptions, and hence we can adapt the amount of padding depending on how many times a protected function is preempted. The padding mechanism we present will pad to some amount of time which the attacker observes, \( T_{\text{observed}} \), where \( T_{\text{observed}} = T_{\text{ext-preempt}} + T_{\text{max}} \). \( T_{\text{max}} \) is the worst case execution time of the protected functions when no external preemptions occur, and \( T_{\text{ext-preempt}} \) is the worst-case time spent during preemptions given the set of preemptions \( (\text{preempt}_1, \text{preempt}_2, \ldots, \text{preempt}_n) \) that occur during the execution of the protected function or the added padding. Note that the number of external preemptions, \( n \), is independent of the secret and thus the attacker does not learn anything sensitive by observing the total padded time \( T_{\text{observed}} \).

In practice, we estimate \( T_{\text{max}} \) through offline profiling of the protected function. Since this value is machine-specific, we perform this profiling on any machine which will run protected functions. Also, even though \( T_{\text{observed}} \) does not leak information about secrets, padding to this value will be costly if \( T_{\text{ext-preempt}} \) is high, due to frequent or long-running preemptions during the protected function. Therefore, we minimize external events that can delay the execution of the protected function. We describe the main external sources of delay during a protected function’s execution and how we deal with each one of them in detail below.

**CPU frequency scaling.** Modern CPUs include mechanisms to change the operating frequency of each core dynamically at runtime depending on the current workload to save power. If a core’s frequency decreases in the middle of the execution of a protected function or it enters the halt state, it will take longer in real-time, increasing \( T_{\text{max}} \). To reduce such variations, we disable CPU frequency scaling and low-power CPU states when a core executes a protected function.

**Paging.** If an attacker can cause memory paging events during the execution of a protected function, she can arbitrarily slow down the protected function. To avoid such cases, our solution forces a process executing the protected function to lock all of its pages in memory and disables page swapping. Our solution currently does not allow processes that allocate more memory than is physically available in the target system to use protected functions.

**Hyperthreading.** Hyperthreading is a technique supported by modern processor cores where one physical core supports multiple logical cores. The OS can schedule tasks on these logical cores independently and the hardware takes care of sharing the underlying physical core. We observed that protected functions executing on a core with hyperthreading enabled can encounter large amounts of slowdown. This slowdown is caused because the other concurrent processes executing on the same physical core can interfere with access to some of the CPU resources.

One potential way of avoiding this slowdown is to configure the OS scheduler to prevent another process from running concurrently on a physical core with a process in the middle of a protected function. However, such a mechanism results in high overheads either due to waiting on another running process to be scheduled off of a virtual core prior to running a protected function, or due to the cost of actively
unscheduling or migrating a process running on another virtual core. For our current prototype implementation, we simply disable hyperthreading as part of system configuration.

**Preemptions by other user processes.** Under regular circumstances, a protected function can be preempted by other user processes. This can delay the execution of the protected function as long as the process is preempted. Therefore, we need to minimize such preemptions while still keeping the system usable.

In our solution, we prevent preemptions by other user processes during the execution of a protected function by using a scheduling policy that prevents migrating the process to a different core and prevents other user processes from preempting a process while the process is running a protected function.

**Preemptions by interrupts.** Another common source of preemption is the hardware interrupts served by the core executing a protected function. One way to solve this problem is to block or rate limit the number of interrupts that can be served by a core while executing a protected function. However, such a technique may make the system non-responsive under heavy load. For this reason, in our current prototype solution, we do not apply such techniques.

Note that some of these interrupts (e.g., network interrupts) can be triggered by the attacker and thus can be used by the attacker to slow down the protected function’s execution. However, in our solution, such an attack increases $T_{\text{ext,preempt}}$, and hence degrades performance, but does not cause information leakage.

### 4.1.2 Safely applying padding

Once the padding amount has been determined using the techniques described above, waiting the target amount might seem easy at first glance. However, there are two major issues that make application of padding complicated in practice as described below.

**Handling limited accuracy of padding loops.** Figure shows that a naive padding scheme that repeatedly measures the elapsed time in a tight loop until the target time is reached leaks timing information. This is because the loop can only break when the condition is evaluated, and hence if one iteration of the loop takes $u$ cycles then the padding loop leaks timing information mod $u$.

Our solution guarantees that the distribution of running times of a protected function for some set of private inputs is indistinguishable from the same distribution produced when a different set of private inputs to the function are used. We call this property the **safe padding property**. We overcome the limitations of the simple wait loop by performing a timing randomization step before entering the simple wait loop. During this step, we perform $m$ rounds of a randomized waiting operation. This goal of this step is to ensure that the amount of time spent in the protected function before the beginning of the simple wait loop, when taken modulo $u$, is uniformly distributed. Hence, the loop will break at a time that is between the target time and the target time plus $u-1$.

Because the last iteration began when the elapsed execution time was uniformly distributed modulo $u$, these different cases will occur with equal probability. Hence, regardless of what is done within the protected function, the padded duration of the function will follow a uniform distribution of $u$ different values after the target time. Therefore, the attacker will not learn anything from observing the padded time of the function.

To reduce the worst-case performance cost of the randomization step, we generate the required randomness at the start of the protected function, before measuring the start time of the protected function. This means that any variability in the runtime of the randomness generator does not increase $T_{\text{max}}$.

**Handling preemptions occurring inside the padding loop.** The scheme presented above assumes that no external preemptions can occur during the execution of the padding loop itself. However, blocking all preemptions during the padding loop will degrade the responsiveness of the system. To avoid such issues, we allow interrupts to be processed during the execution of the padding loop and update the padding time accordingly. We repeatedly update the padding time in response to preemptions until a “safe exit condition” is met where we can stop padding.

Our approach is to initially pad to the target value $T_{\text{max}}$, regardless of how many preemptions occur. We then repeatedly increase $T_{\text{ext,preempt}}$ and pad to the new adjusted padding target until we execute a padding loop where no preemptions occur. The pseudocode of our approach is show
// At the return point of a protected function:
// \(T_{\text{begin}}\) holds the time at function start
// \(I_{\text{begin}}\) holds the preemption count at function start
1 \textbf{for} j = 1 \textbf{to} m
2 \textbf{Short-Random-Delay()}
3 \(T_{\text{target}} = T_{\text{begin}} + T_{\text{max}}\)
4 overtime = 0
5 \textbf{for} i = 1 \textbf{to} \(\infty\)
6 \textbf{before} = \text{Current-Time()}
7 \textbf{while} \text{Current-Time()} < \(T_{\text{target}}\), \text{re-check.}
8 // Measure preemption count and adjust target
9 \(T_{\text{ext/preempt}} = (\text{Preemptions()} - I_{\text{begin}}) \cdot T_{\text{penalty}}\)
10 \(T_{\text{next}} = T_{\text{begin}} + T_{\text{max}} + T_{\text{ext/preempt}} + \text{overtime}\)
11 // Overtime-detection support
12 \textbf{if} \(\text{before} \geq T_{\text{next}}\) \textbf{and} \(\text{overtime} = 0\)
13 \(\text{overtime} = T_{\text{next}}\)
14 \(T_{\text{next}} = T_{\text{next}} + \text{overtime}\)
15 \textbf{if} \(T_{\text{next}} = T_{\text{target}}\)
16 \textbf{return}
17 \(T_{\text{target}} = T_{\text{next}}\)

\textbf{Figure 2:} Algorithm for applying time padding to a protected function’s execution.

In Figure 2, our technique does not leak any information about the actual runtime of the protected function as the final padding target only depends on the pattern of preemptions but not on the initial elapsed time before entering the padding loops. Note that forward progress in our padding loops is guaranteed as long as some form of preemptions are rate limited on the cores executing protected functions.

The algorithm computes \(T_{\text{ext/preempt}}\) based on observed preemptions simply by multiplying a constant \(T_{\text{penalty}}\) by the number of preemptions. Since \(T_{\text{ext/preempt}}\) should match the worst-case execution time of the observed preemptions, \(T_{\text{penalty}}\) is the worst-case execution time of any single preemption. Like \(T_{\text{max}}\), \(T_{\text{penalty}}\) is machine specific and can be determined empirically from profiling data.

\subsection{Determining worst-case execution time}

We estimate \(T_{\text{max}}\), the worst-case execution time of a protected function using profiling data collected during an offline profiling phase. Since the worst-case execution time depends on the target machine, we perform this offline profiling on individual target machines.

To gather profiling information, we run an application that invokes protected functions with a input generating script either provided by the application or the system administrator. We instrument the protected functions in the application so that the worst-case performance behavior is stored in a profile file. We compute the padding parameters based on the output profiling results. To reduce the possibility of overtimes occurring due to uncommon inputs, it is important that we profile for both common and uncommon inputs.

To be conservative, we obtain all profiling measurements for the protected functions under high load conditions (i.e., in parallel with programs that stress test both memory and CPU). From these measurements, we compute \(T_{\text{max}}\) so that it is a worst-case bound when at most a \(\kappa\) fraction of profiling readings are excluded, where \(\kappa\) is a security parameter. Higher values of \(\kappa\) increase the frequency of overtimes but reduce \(T_{\text{max}}\), hence \(\kappa\) represents a performance-security trade-off. For our prototype implementation we set \(\kappa\) to \(10^{-5}\).

\subsection{Handling overtimes}

Due to the immense size of the input-space of most protected functions, despite our best efforts, we might miss some pathological input that takes significantly longer time than other inputs. If such a pathological input appears in the wild, the protected function may take longer than estimated worst-case bound and this will result in an overtime and leak information.

We therefore augment our technique to detect overtimes, that is, when the elapsed time of the protected function, even taking the interrupts into account, is greater than the computed padding target. When an overtime is detected, we pad to a significantly larger value than one would expect the function to take. This ensures that each overtime only leaks 1 bit of information.

To further limit leakage, if a sufficient number of overtimes are detected, we can also alert the system administrator and potentially refuse to service requests. The system administrator can then act on this alert by updating the secret inputs (e.g., secret keys) and increasing the parameters of the model \(T_{\text{max}}\) to avoid future overtimes.

Any changes to the memory-mapped file will immediately impact the padding parameters of any application invoking the protected function except the ones that are in the middle of the padding step.

\subsection{Shared resource isolation}

In our solution, isolation of shared resources are implemented in two ways — isolating shared resources between concurrent processes and cleansing state left in shared resources before handing them over to other untrusted processes. Isolating shared resources help in both preventing timing attacks from other concurrent processes, and also improving performance by minimizing variations in the runtime of protected functions. For example, consider the case where we disable hyperthreading during a protected function’s execution to improve performance as described earlier. This also ensures that an attacker cannot run spy code that snoops on per-core state while a protected function is executing. Also, preventing preemptions from other user processes during the execution of protected function ensures that the core and its L1/L2 caches are dedicated for the protected function.

To enforce resource isolation, we also make several modifications throughout the entire life-cycle of processes that invokes protected functions. We described the details below.

\textbf{Changes to system initialization.} We use page coloring to dynamically isolate the protected function’s data in the L3 cache. To provide page coloring at boot time, the OS initializes physical page allocators that do not allocate pages having any of \(C\) reserved “secure” page colors, unless the caller specifically requests a secure color. Pages are colored
based on which L3 cache sets a page maps to. Therefore, two pages with different colors are guaranteed never to conflict in the L3 cache in any of their cache lines.

**Changes to system configuration.** In order to support page coloring, the system configuration script disables transparent huge pages and sets up access control to huge pages. An attacker that has access to a huge page can evade the isolation provided by page coloring, since a huge page can span multiple page colors. Hence, we bar access to huge pages (transparently or by request) to non-privileged users.

Also as part of page coloring, the script disables memory deduplication features, such as kernel same-page merging. This prevents a secure-colored page mapped into one process from being transparently mapped as shared into another process. Disabling memory deduplication has been used in the past in hypervisors to prevent leakage of information across different virtual machines [30].

**Changes to process state.** During the initialization of the process calling protected functions, a kernel module routine is called that remaps all pages allocated by the process in private mappings (i.e., the heap, stack, text-segment, library code, and library data pages) to pages that are not shared with processes of any other user and that have a page color reserved by the user. The remapping transparently changes the physical pages that a process accesses without modifying the virtual memory addresses, and hence requires no special application support. If the user has not yet reserved any page colors or there are no more remaining pages of any of her reserved page colors, the OS allocates one of the reserved colors for the user. Also, the process is flagged with a "secure-color" bit. We modify the OS so that it recognizes this flag and ensures that the future pages allocated to a private mapping for the process will come from a reserved page color for the user. Note that since we only remap private mappings, we do not protect applications that access a shared mapping from inside a protected function.

This strategy for allocating page colors to users has the minor potential downside that such a system restricts the numbers of different users’ processes that can concurrently call protected functions. We believe that such a restriction is a reasonable trade-off between security and performance.

**Changes when a protected function returns.** To ensure that an attacker does not see the tainted state in a per-core resource after a protected function, when a protected function returns we mark the CPU as “tainted” with the user ID of the caller process. The next time a the OS attempts to schedule a process from a different user on the core, it will first flush all per-CPU caches, including the L1 instruction cache, L1 data cache, L2 cache, Branch Translation Buffer (BTB), and Translation lookaside buffer (TLB). Such a scheme ensures that the overhead of flushing these caches can be amortized over multiple invocations of protected functions by the same user.

5. IMPLEMENTATION

We implement a prototype implementation of our protection mechanism for the Linux OS running on the Intel Sandy Bridge architecture. We describe the different components of our implementation below.

5.1 Programming API

We implement a new function annotation `FIXED_TIME` for the C/C++ language that indicates that a function should be protected. The annotation can be specified either in the declaration of the function or at its definition. Adding this annotation is the only change to a C/C++ codebase that a programmer must make to use our solution. We wrote a plugin for the Clang C/C++ compiler that handles this annotation. The plugin automatically inserts a call to the function `fixed_time_begin` at the start of the protected function and a call to `fixed_time_end` at any return point of the function. These functions protect the annotated function using the mechanisms described in Section 4.

Alternatively, a programmer can also call these functions explicitly. This is needed for protecting ranges of code within function such as the state transitions of the TLS state machine (see Section 6.1). We provide a Java native interface wrapper to both `fixed_time_begin` and `fixed_time_end` functions, for supporting protected functions written in Java.

5.2 Time padding

For implementing time padding loops, we read from the timestamp counter in x86 processors to collect time measurements. In most modern x86 processors, including the one we tested on, the timestamp counter has a constant frequency regardless of the power saving state of a processor. We generate pseudorandom bytes for the randomized padding step using the ChaCha/8 stream cipher [9]. We use a value of 15 ms for $T_{\text{penalty}}$ as this bounds the worst-case slowdown due to a single interrupt we observed in our experiments.

The randomized wait operation we use takes an input $X$ and simply performs $X + c$ noops in a loop, where $c$ is a large enough value so that the loop takes one cycle longer for each additional iteration. We observe that $c = 46$ is sufficient to achieve this property.

Some of the OS modifications specified in our solution are implemented as a loadable kernel module. This module supports an IOCTL to mark the core as tainted at the end of a protected function. The module also supports a IOCTL call that enables fast access to the interrupt and context-switch count. In the standard Linux kernel, the interrupt count is usually accessed through the proc file system interface. However, such an interface is too slow for our purposes. Instead, the kernel module allocates a page of counters that is mapped into the calling process’ virtual address space and is also pointed to in its task struct. We modify the kernel to check on every interrupt and context switch if the current task has such a page, and if so, to increment the corresponding counter in that page.

**Offline profiling.** We provide a profiling wrapper script, `fixed_time_record.sh`, that computes worst-case execution time parameters of each protected function as well as the worst-case slowdown on that function due to preemptions by different interrupts or kernel tasks.

The profiling script automatically generates profiling information for any protected functions in an executable by running the application on a user-provided inputs. During the profiling process, we run a variety of applications in parallel to create a stress-testing environment that triggers worst-case performance of the protected function. To allow the stress testers to maximally slow down the user application, we reset the scheduling parameters and CPU affinity of a thread at the start and end of every protected function. One stress tester generates interrupts at a high frequency using a simple program that generates a flood of
UDP packets to the loopback network interface. We also run the mprime\(^2\), systester\(^3\) and the LINPACK benchmark\(^4\) to cause high CPU load and large amounts of memory contention.

### 5.3 Shared resource isolation

**Isolating a processor core and core-specific caches.**

We disable hyperthreading in Linux by selectively disabling virtual cores. This prevents any other processes from interfering with the execution of a protected function. As part of our prototype, we also implement a simple version of the page coloring scheme as described in Section 4.

We prevent a user from observing hardware performance counts showing the performance behavior of other users’ processes. The per*events* framework on Linux mediates access to hardware performance counters. We configure the framework to allow accessing per-cpu performance counters only by the privileged users. Note that an unprivileged user can still access per-process performance counters that measure the performance of their own processes.

For ensuring that a processor core executing a protected function is not preempted by other user processes, as specified in Section 4, we depend on a scheduling mode that prevents other userspace processes from preempting a protected function. For this purpose, we use the Linux SCHED_FIFO scheduling mode at maximum priority. In order to be able to do this, we allow unprivileged users to use SCHED_FIFO at priority 99 by changing the limits in the /etc/security/limits.conf file.

One side effect of this technique is that if a protected function manually yields to the scheduler or performs blocking operations, the process invoking the protected function may be scheduled off. Therefore, we do not allow any blocking operations or system calls inside the protected function. As mentioned earlier, we also disable paging for the processes executing protected functions by using the mlockall() system call with the MCL_FUTURE.

We detect whether a protected function has violated the conditions of isolated execution by determining whether any voluntary context switches occurred during the protected function’s execution. This usually indicates that either the protected function yield the CPU manually or performed some blocking operations.

**Flushing shared resources.**

We modify the Linux scheduler to check the taint of a core before scheduling a user process on a processor core and to flush per-core resources if needed as described in Section 4.

To flush the L1 and L2 caches, we iteratively read over a segment of memory that is larger than the corresponding cache sizes. We found this to be significantly more efficient than using the WBINVD instruction, which we observed cost as much as 300 microseconds in our tests. We flush the L1 instruction cache by executing a large number of NOP instructions.

Current implementations of Linux flush the TLB during each context switch. Therefore, we do not need to separately flush them. However, if Linux starts leveraging the PCID feature of x86 processors in the future, the TLB would have to be flushed explicitly. For flushing the BTB, we leverage a “branch slide” consisting of alternating conditional branch and NOP instructions.

### 6. EVALUATION

To show that our approach can be applied to protect a wide variety of software, we have evaluated our solution in three different settings and found that our solution successfully prevents potential timing and cache attacks in all of these settings. We describe these settings below.

**Encryption algorithms implemented in high level interpreted languages like Java.**

Traditionally, cryptographic algorithms implemented in interpreted languages like Java have been harder to protect from timing attacks than those implemented in low level languages like C. One of the key reasons behind this is the fact that virtual machines for the high level interpreted languages may contain data-dependent timing variations that are very hard to detect. While developers writing low level code can use features such as in-line assembly to carefully control the machine code of their implementation, such low level control is simply not possible in a higher level language.

We show that our techniques can take care of these issues. We demonstrate that our defense can make the computation time of Java implementations of cryptographic algorithms independent of the secret key with minimal performance overhead.

**Sensitive data structures.**

Besides cryptographic algorithms, timing channels also occur in the context of different data structure operations like hash table lookups. Hash table lookups may take different amount of time depending on how many items are present in the bucket where the desired item is located. It will take longer time to find items in buckets with higher number of items than in the ones with less items. This signal can be exploited by an attacker to cause denial of service attacks.

We demonstrate that our technique can prevent timing leaks in two different hash table implementations: associative arrays in C++ STL and HashMaps in Java.

**Cryptographic operations and SSL/TLS state machine.**

Implementations of cryptographic primitives other than the public/private key encryption or decryption routines may also suffer from side channel attacks. For example, a cryptographic hash algorithm like SHA-1 takes different amount of time depending on the length of the input data. In fact, such timing variations have been used as part of several existing attacks against SSL/TLS protocols (e.g., Lucky 13). Also, the time taken to perform the computation for implementing different stages of the SSL/TLS state machine may also be dependent on the secret key.

We find that our protection mechanism can protect cryptographic primitives like hash functions and individual stages of the SSL/TLS state machine from timing attacks while incurring minimal overhead.

**Experiment setup.**

We perform all our experiments on a machine with 2.3GHz Intel Xeon CPUs organized in 2 sockets each containing 6 physical cores. Each core has a 32KB L1 instruction cache, a 32KB L1 data cache, and a 256KB L2 cache. Each socket has a 15MB L3 cache. The machine has a total of 64GB of RAM.

For our experiments, we use OpenSSL version 1.0.11 and Java version BouncyCastle 1.52 (beta). The test machine
A. Unprotected

B. With time padding but no randomized noise

C. Full protection (padding+randomized noise)

Figure 3: Defeated distinguishing attack.

We found that our defense completely defeats such a distinguishing attack despite the highly favorable conditions for an attacker. Figure 3(A) shows the distributions of observed runtimes of the protected function on inputs 0 and 1 with no defense applied. Figure 3(B) shows the runtime distributions where padding is added to reach \( T_{max} = 5000 \) cycles \((\approx 2.17 \mu s)\) without the time randomization step. In both cases, it can be seen that the observed timing distributions for the two different inputs are clearly distinguishable. Figure 3(C) shows the same distributions when \( m = 5 \) rounds of timing randomization are applied along with time padding.

Preventing a simple timing attack. To determine the effectiveness of our safe padding technique, we first test whether our technique can protect against a large timing channel that can distinguish between two different inputs of a simple function. To make the attacker’s job easier, we craft a simple function that has an easily observable timing channel—the function executes a loop for 1 iteration if the input is 0 and 11 iterations otherwise. We use the x86 `loop` instruction to implement the loop and just a single `nop` instruction as the body of the loop. We assume that the attacker calls the protected function directly and measures the value of the timestamp counter immediately before and after the call. The goal of the attacker is to distinguish between two different inputs (0 and 1) by monitoring the execution time of the function. Note that these conditions are extremely favorable for an attacker.

We found that our defense completely defeats such a distinguishing attack despite the highly favorable conditions for an attacker. Figure 4 by plotting the variation of empirical statistical distance between the observed distributions as the amount of padding noise added is changed. The statistical distance is computed using the following formula.

\[
d(X, Y) = \frac{1}{2} \sum_{i=0}^{\infty} |P[X = i] - P[Y = i]|
\]

We measure the statistical distance over the set of observations that are within the range of 50 cycles on either side of the median (this contains nearly all observations.) Each distribution consist of around 600 million observations.

The dashed line in Figure 4 shows the statistical distance between two different instances of the test function with 0 as input. The solid line shows the statistical distance where one instance has 0 as input and the other has 1. We observe that the attack can be completely prevented when at least 2 rounds of noise are used.

Timing attack on RSA decryption. We next evaluate the effectiveness of our time padding approach to defeat the timing attack by Brumley et al. [15] against unblinded RSA implementations. Blinding is an algorithmic modification to RSA that uses randomness to prevent timing attacks. To isolate the impact of our specific defense, we apply our defense to the RSA implementation in OpenSSL 1.0.1h with such constant time defenses disabled. To do so, we configure OpenSSL to disable blinding, use the non-constant time exponentiation implementation, and use the non-word-based Montgomery reduction implementation. We measure the time of decrypting 256-byte messages with a random 2048-bit key. We chose messages to have Montgomery representations differing by multiples of \( 2^{1016} \). Figure 5A shows the average observed running time for such a decryption operation, which is around 4.16 ms. The messages are displayed from left to right in sorted order of how many Montgomery reductions occur during the decryption. Each message was sampled roughly 8000 times and the samples were randomly split into 4 sample sets. As observed by Brumley et al. [15], the number of Montgomery reductions can be roughly determined from the running time of an unprotected RSA de-
A. Unprotected

![Figure 5: Protecting against timing attacks on unblinded RSA encryption. Such information can be used to derive full length keys.](image)

We then apply our defense to this decryption using a $T_{max}$ of $9.68 \times 10^6$ cycles $\approx 4.21$ ms. One timer interrupt is guaranteed to occur during such an operation, as timer interrupts occur at a rate of 250/s on our target machine. Under 30 million measurements, we observe a multi-modal padded distribution with four narrow, disjoint peaks corresponding to the padding algorithm padding to $T_{\text{ext,preempt}}$ for between one and four interrupts. The four peaks represent, respectively, 94.0%, 5.8%, 0.6%, and 0.4% of the samples. We did not observe that these probabilities vary across different messages. Hence, in figure 5B, we show the average observed time considering only observations from within the first peak. Again, samples are split into 4 random sample sets, each key is sampled around 700 thousand times. We observe no message-dependent signal.

B. Protected

![Figure 5: Protecting against timing attacks on unblinded RSA encryption. Such information can be used to derive full length keys.](image)

We addressed both challenges by generalizing the notion of a protected function to that of a **protected interval**, which is an interval of execution starting with a call to fixed_time_begin and ending with fixed_time_end. We then split an execution of the TLS protocol into several intervals on boundaries defined by transitions of the TLS state machine and on low-level socket read and write operations. To achieve this, we first inserted calls to fixed_time_begin and fixed_time_end at the start and end of each state within the TLS state machine implementation. Next, we modified the low-level socket read and socket write OpenSSL wrapper functions to end the current interval, communicate with the socket, and then start a new interval. Thus divided, all cryptographic operations performed inside the TLS implementation are within a protected interval. Each interval is uniquely identifiable by the name of the current TLS state concatenated with an integer incremented every time a new interval is started within the state's TLS state (equivalently, the number of socket operations that occurred so far during the state).

The advantage of this strategy is that, unlike any prior defenses, it protects the entire implementation of the TLS state machine from any form of timing attack. However, such protection schemes may incur additional overheads due to protecting parts of the protocol that may not be vulnerable to timing attacks because they do not work with secret data.

We evaluate the performance of the fully protected TLS state machine as well as an implementation that only protects the public key signing operation in Figure 7. We observe an overhead of less than 8.5% on connection latency even when protecting the full TLS protocol.

### 6.1 Performance evaluation

**Performance costs of individual components.** Table 6 shows the individual cost of the different components of our defense. Our total performance overhead is less than the total sum of these components as we do not perform most of these operations in the critical path. Note that retrieving the number of times a process was interrupted or determining whether a voluntary context switch occurred during a protected function’s execution is cheap due to the modifications to the Linux kernel described in Section 5.

**Macrobenchmark: protecting the TLS state machine.** We applied our implementation to protect the server-side implementation of the TLS connection protocol in OpenSSL. The TLS protocol is implemented as a state machine in OpenSSL, and this presented a challenge for applying our solution which is defined in terms of protected functions. Additionally, reading and writing to a socket is interleaved with cryptographic operations in the specification of the TLS protocol, which conflicts with our solution’s requirement that no blocking I/O may be performed within a protected function.

| Component                                      | Cost (ns) |
|------------------------------------------------|-----------|
| $m = 5$ time randomization step, WCET          | 710       |
| Get interrupt counters                        | 16        |
| Detect context switch                          | 4         |
| Set and restore SCHED_FIFO                    | 2,650     |
| Set and restore CPU affinity                   | 1,235     |
| Flush L1D+L2 cache                            | 23,000    |
| Flush BTB cache                               | 7,000     |

![Figure 6: Performance overheads of individual components of our defense. WCET, worst-case execution time. Only costs listed in the upper half of the table are incurred on each call to a protected function.](image)

Note that the delays experienced in any real applications will be significantly less than these micro benchmarks as real applications will also perform some I/O operations that will amortize the performance overhead.

Focusing on the BouncyCastle results, we observe a small improvement in performance when protecting RSA signing
Connection latency (RSA) & Mean (ms) & 99% Tail \\
Stock OpenSSL & 6.02 & 6.99 \\
Stock OpenSSL+ Our solution (sign only) & 6.16 & \textbf{6.34} \\

Connection latency (ECDSA) & Mean (ms) & 99% Tail \\
Stock OpenSSL & 5.21 & 5.44 \\
Stock OpenSSL+ Our solution (sign only) & 5.27 & 5.48 \\
Stock OpenSSL+ Our solution & 5.66 & 5.90 \\

Figure 7: The impact on TLS v1.2 connection latency when applying our defense to the OpenSSL server-side TLS implementation. We evaluate the cases where the server uses an RSA 2048-bit or ECDSA 256-bit signing key with SHA-256 as the digest function. Latency given in milliseconds and measures the end-to-end connection time. The client uses the unmodified OpenSSL library attempts. We evaluate our defense when only protecting the signing operation and when protecting all server-side routines performed as part of the TLS connection protocol that use cryptography. Even when the full TLS protocol is protected, our approach adds an overhead of less than 8.5% to average connection latency. Bold text indicates measurements that are lower than the baseline.

Figure 8: Impact on performance of signing a 100 byte message using SHA-256 with RSA or ECDSA for the OpenSSL and BouncyCastle implementations. Measurements are in milliseconds. We disable blinding when applying our defense to the RSA signature operation. Bold text indicates a measurement that is lower when using our defense than the stock implementation.

(1.32μs at κ = 10^-5). The same worst-case execution estimate increases to 13.3μs when interrupt cases are not excluded, hence our scheme benefits significantly from adapting to interrupts during padding for this example.

7. LIMITATIONS

8. RELATED WORK

8.1 Defenses against remote timing attacks

The remote attacks described earlier exploit the input-dependent execution times of cryptographic operations. There are three main approaches to make cryptographic operations constant time, that is, so that the execution time is independent of the inputs: static transformation, application-specific changes, and dynamic padding. We describe each of them in below.

Application-specific changes. One conceptually simple way to defend an application against timing attacks is to modify its sensitive operations such that their timing behavior is not key-dependent. For example, AES [27, 10] implementations can be modified to ensure that their execution times are key-independent. Note that, since the cache behavior impacts running time, achieving secret-independent timing usually requires rewriting the operation so that its memory access pattern is also independent of secrets. Such modifications are application specific and very hard to design.
Static transformation. An alternative approach to prevent remote attacks is to use static transformations on the implementation of the cryptographic operation to make it constant time. One can use a static analyzer to find the longest possible path through the cryptographic operation and insert padding instructions that have no side-effects (like NOP) along other paths so that they take the same amount of time as the longest path. While this approach is generic and can be applied to any cryptographic operations, it has several drawbacks. In modern architectures like x86, the execution time of several instructions (e.g., the integer divide instruction and multiple floating-point instructions) depend on the value of the input of these instructions. This makes it extremely hard and time consuming to statically estimate the execution time of these instructions. Moreover, it’s very hard to statically predict the changes in the execution time due to internal cache collisions in the implementation of the cryptographic operation.

Dynamic padding. Dynamic padding techniques add a variable amount of padding to a sensitive computation that depends on the observed execution time of the computation in order to mitigate the timing side-channel. Several prior works have presented ways to pad the execution of a black-box computation to certain predetermined thresholds and obtain bounded information leakage. Zhang et al. designed a new programming language that, when used to write sensitive operations, can enforce limits on the timing information leakage. One of the major drawbacks of existing dynamic padding schemes is that the estimation of the worst-case execution time tends to be overly pessimistic as it depends on several external parameters like OS scheduling, cache behavior of the simultaneously running programs etc. For example, Zhang et al. used a worst-case execution time to be 300 seconds for protecting a Wiki server. Such overly pessimistic estimates increase the amount of required padding and thus results in significant performance overheads (90 – 400% in ).

8.2 Defenses against local attacks

Local attackers can also perform timing attacks, hence some of the defenses provided in the prior section also defend against some local attacks. However, local attackers have access to shared hardware resources that contain information related to the target cryptographic operation and have access to fine-grained timers. A common attack vector is to probe a shared hardware resource, and then, using the fine-grained timer, measure how long the probe took to run. Most of the proposed defenses try to remove either access to fine-grained timers or, instead, isolate access to the shared hardware resources. Still others obfuscate We describe these approaches below.

Removing fine-grained timers. Several prior works have evaluated removing or modifying time measurements taken on the target machine. Such solutions are often quite effective at preventing side channel attacks as the underlying states of most shared hardware resources can only be read by accurately measuring the time taken to perform certain operations (e.g., read a cache line). However, even removing access to wall clock time is not sufficient, as an attacker using multiple threads can infer time measurements by observing the scheduling behavior of the threads. Using instruction-based scheduling can eliminate such an attack.

Preventing sharing of hardware state across processes. Many proposed defenses prevent an attacker from observing state changes to shared hardware resources caused by a victim process. We divide the proposed defenses five categories and describe them next.

Resource partitioning. Partitioning shared hardware resources can defeat local attackers, as they cannot access the same partition of the resource as a victim. Kim et al. present an efficient management scheme which locks memory regions accessed by sensitive functions into reserved portions of the L3 cache. Their approach defeats cache-based side channel attacks and can be more efficient than page coloring. Ristenpart et al. suggest allocating dedicated hardware to each virtual machine instance to prevent cross-VM cache attacks.

Limiting concurrent access. Varadarajan et al. propose using minimum runtime guarantees to ensure that a VM is not preempted too frequently. When gang scheduling is used or hyperthreading is disabled, an attacker can only observe per-CPU resources when it has preempted a victim. Hence, reducing the frequency of preemptions reduces the feasibility of cache-attacks on per-CPU caches.

Custom hardware. Custom hardware can be used to obfuscate and randomize the victim process’s usage of the hardware. For example, Wang et al. augmented the OpenSSL with dynamic padding along with other attacks. Düppling et al. attempt to flush per-CPU L1 and (optionally) L2 caches periodically, and only when a context switch has occurred on a core following a protected operation. Their solution requires that hyperthreading is disabled. This is similar to our solution’s technique of flushing per-CPU resources in the OS scheduler whenever a context switch to a different user occurs following a protected operation. They report modest overheads of less than 7% even on workloads that are dominated by protected operations.

Flush state. Another class of defenses ensure that the state of any per-CPU hardware resources are cleared before transferring them from one process to another. Düppling, by Zhang et al., attempts to flush per-CPU L1 and (optionally) L2 caches periodically, and only when a context switch has occurred on a core following a protected operation. They report modest overheads of less than 7% even on workloads that are dominated by protected operations.

Application transformations. Cryptographic operations in different programs can also be modified to exhibit either secret-independent or obfuscated hardware access patterns. If the access to the hardware is independent of secrets, then an attacker cannot use any of the state leaked through shared hardware to learn anything meaningful about the cryptographic operations. Several prior works have shown how to modify AES implementations so that they obfuscate their cache access patterns. Another example is that recent versions of OpenSSL use a modified implementation of RSA specifically with secret-independent cache accesses. These modifications are specific to particular cryptographic operations and are very hard to implement correctly. For example, 924 lines of assembly code had to be added to OpenSSL to implement the Montgomery modular exponentiation used in the modified RSA implementation.

Crane et al. implement a system that dynamically applies cache-access obfuscating transformations to an application at runtime.
9. CONCLUSION

In this paper, we have presented a low-overhead, cross-
architecture defense that protects applications against both local and remote timing attacks with minimal application code changes. We have also demonstrated that our defense is language-independent. We hope that our work will motivate application developers to use our techniques to defend against a wide variety of timing attacks without incurring any significant performance overhead.

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References

[1] O. Acı̈mez, Yet Another MicroArchitectural Attack: Exploiting I-Cache. In CSoW, 2007.
[2] O. Acı̈mez, Ç. Koç, and J. Seifert. On the power of simple branch prediction analysis. In ASIACCS, 2007.
[3] O. Acı̈mez, Ç. Koç, and J. Seifert. Predicting secret keys via branch prediction. In CT-RSA, 2007.
[4] O. Acı̈mez and J. Seifert. Cheap hardware parallelism implies cheap security. In FDTC, 2007.
[5] M. Andryszc, D. Kohlbrenner, K. Mowery, R. Jhala, S. Lerner, and H. Shacham. On subnormal floating point and abnormal timing. In Proc. of IEEE S&P, 2015.
[6] A. Askarov, D. Zhang, and A. Myers. Predictive black-box mitigation of timing channels. In CCS, 2010.
[7] G. Barthe, G. Betarte, J. Campo, C. Luna, and D. Pichardie. System-level non-interference for constant-time cryptography. In Proceedings of the ACM Conference on Computer and Communications Security, pages 1267–1279, 2014.
[8] D. Bernstein. Cache-timing attacks on aes, 2005.
[9] D. Bernstein. Chacha, a variant of salsa20. http://cr.yp.to/chacha.html
[10] J. Blomer, J. Guajardo, and V. Krummel. Provably secure masking of aes. In Selected Areas in Cryptography, pages 69–83, 2005.
[11] J. Bonneau and I. Mironov. Cache-collision timing attacks against AES. In Cryptographic Hardware and Embedded Systems - CHES 2006, 6th International Workshop, Yokohama, Japan, October 10-13, 2006, Proceedings, pages 201–215, 2006.
[12] A. Bortz and D. Boneh. Exposing private information by large-scale timing attacks on aes. In Proceedings of the 16th international conference on World Wide Web, pages 621–628. ACM, 2007.
[13] E. Brickell, G. Graunke, M. Neve, and J. Seifert. Software mitigations to hedge AES against cache-based software side channel vulnerabilities. IACR Cryptology ePrint Archive, 2006.
[14] B. Brunley and N. Tuver. Remote timing attacks are still practical. In ESORICS, 2011.
[15] D. Brunley and D. Boneh. Remote Timing Attacks Are Practical. In USENIX Security, 2003.
[16] F. R. K. Chung, P. Diaconis, and R. L. Graham. Random walks arising in random number generation. The Annals of Probability, pages 1148–1165, 1987.
[17] J. Cleemput, B. Coppens, and B. D. Sutter. Compiler mitigations for time attacks on modern x86 processors. TACO, 8(4):23, 2012.
[18] D. Cock, Q. Ge, T. Murray, and G. Heiser. The Last Mile: An Empirical Study of Some Timing Channels on sel4. In CCS, 2014.
[19] B. Coppens, I. Verbauwhede, K. D. Bosschere, and B. D. Sutter. Practical mitigations for timing-based side-channel attacks on modern x86 processors. In S&P, 2009.
[20] S. Crane, A. Homescu, S. Brunthaler, P. Larsen, and M. Franz. Thwarting cache side-channel attacks through dynamic software diversity. 2015.
[21] S. A. Crosby and D. S. Wallach. Denial of service via algorithmic complexity attacks. In USENIX Security, volume 2, 2003.
[22] D. Gullasch, E. Bangrter, and S. Krenn. Cache games-bringing access-based cache attacks on aes to practice. In S&P, 2011.
[23] A. Haebeler, B. C. Pierce, and A. Narayana. Differential privacy under fire. In USENIX Security Symposium, 2011.
[24] C. Irazoqui, T. Eisenbarth, and B. Sunar. Jackpot stealing information from large caches via huge pages. Cryptology ePrint Archive, Report 2014/970, 2014. http://eprint.iacr.org/
[25] T. Kim, M. Peinado, and G. Maino-Rui. Stealthmem: System-level protection against cache-based side channel attacks in the cloud. In USENIX Security symposium, pages 189–204, 2012.
[26] P. Kocher. Timing attacks on implementations of Diffie-Hellman, RSA, DSS, and other systems. In CRYPTO, 1996.
[27] R. Könighofer. A fast and cache-timing resistant implementation of AES. In CT-RSA, 2008.
[28] B. Kopf and M. Durnuth. A provably secure and efficient countermeasure against timing attacks. In CSF, 2009.
[29] A. Langley. Lucky thirteen attack on tls cbc, 2013. www.imperialviolet.org/2013/02/04/luckythirteen.html
[30] P. Li, D. Gao, and M. Reiter. Mitigating access-driven timing channels in clouds using StopWatch. In DSN, 2013.
[31] R. Martin, J. Demme, and S. Sethumadhavan. Timewarp: rethinking timekeeping and performance monitoring mechanisms to mitigate side-channel attacks. In ISCA, 2012.
[32] D. Osvik, A. Shamir, and E. Tromer. Cache attacks and countermeasures: the case of AES. In CT-RSA, 2006.
[33] C. Percival. Cache missing for fun and profit, 2005.
[34] T. Ristenpart, E. Tromer, H. Shacham, and S. Savage. Hey, you, get off of my cloud: exploiting information leakage in third-party compute clouds. In CCS, 2009.
[35] D. Stefan, P. Buiras, E. Yang, A. Levy, D. Terei, A. Russo, and D. Mazières. Eliminating cache-based timing attacks with instruction-based scheduling. In ESORICS, 2013.
[36] K. Suzuki, K. Iijima, T. Yagi, and C. Artho. Memory deduplication as a threat to the guest os. In Proceedings of the Fourth European Workshop on System Security, page 1. ACM, 2011.
[37] E. Tromer, D. Osvik, and A. Shamir. Efficient cache attacks on AES, and countermeasures. Journal of Cryptology, 23(1):37–71, 2010.
[38] C. Varadarajan, T. Ristenpart, and M. Swift. Scheduler-based defenses against cross-vm side-channels. In Usenix Security, 2014.
[39] B. Vattikonda, S. Das, and H. Shacham. Eliminating fine grained timers in xen. In CCSW, 2011.
[40] Z. Wang and R. Lee. New cache designs for thwarting software cache-based side channel attacks. In ISCA, 2007.
[41] Z. Wang and R. Lee. A novel cache architecture with enhanced performance and security. In MICRO, 2008.
[42] Y. Yarom and N. Benger. Recovering OpenSSL ECDSA Nonces Using the FLUSH+ RELOAD Cache Side-channel Attack. IACR Cryptology ePrint Archive, 2014.
[43] Y. Yarom and K. Falkner. Flush+Reload: a High Resolution, Low Noise, Lb Cache Side-Channel Attack. In USENIX Security, 2014.
[44] D. Zhang, A. Askarov, and A. Myers. Predictive mitigation of timing channels in interactive systems. In CCS, 2011.
[45] D. Zhang, A. Askarov, and A. Myers. Language-based control and mitigation of timing channels. In PLDI, 2012.
[46] Y. Zhang, A. Juels, M. Reiter, and T. Ristenpart. Cross-vm side channels and their use to extract private keys. In CCS, 2012.
[47] Y. Zhang and M. Reiter. Dübpen: Retooling commodity operating systems to mitigate cache side channels in the cloud. In CCS, 2013.