Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs described with Band Broadening

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Abstract—In the standard MOSFET description of the drain current $I_D$, as a function of applied gate voltage $V_{GS}$, the subthreshold swing $SS(T)$ obtained as $dV_{GS}/d\log I_D$ has a fundamental lower limit as a function of temperature $T$ given by $SS(T) = \ln 10 k_B T/e$. However, recent low-temperature studies of different advanced CMOS technologies have reported $SS$ values (4 K or lower) which are at least an order of magnitude larger. Here, we present and analyze the saturation of $SS(T)$ in 28 nm fully-depleted silicon-on-insulator (FD-SOI) devices for both n- and p-type MOSFETs of different gate oxide thicknesses and gate lengths down to 4 K. Until now, the increase of $SS$ values has been put forward to understand the saturation. Here, an original explanation of the phenomenon is presented by considering a disorder-induced tail in the density of states at the conduction (valence) band edge for the calculation of the MOS channel transport by applying Fermi-Dirac statistics. This results in a subthreshold $I_D \sim e^{V_{GS}/k_B T_0}$ for $T_0 = 35 K$ with saturation value $SS(T < T_0) = \ln 10 k_B T_0/e$. The proposed model adequately describes the experimental data of $SS(T)$ from 300 down to 4 K using $k_B T_0 \approx 3$ meV for the width of the exponential tail and can also accurately describe $SS(I_D)$ within the whole subthreshold region. Our analysis allows a direct determination of the temperature-dependent band-tail extension forming a crucial element in future compact modeling and design of cryogenic circuits.

Index Terms—Cryogenic electronics, MOSFET, Subthreshold Swing, 28nm FD-SOI, Band tail, Quantum computing.

I. INTRODUCTION

The development of electronic circuits at cryogenic temperatures (4 K or even lower) has great importance for a large spectrum of applications such as high-performance classical computing, cryogenic sensors and detectors, space electronics, low power neuromorphic circuits, and quantum computing [1]–[4]. The nowadays progress in the realization of quantum bit (qubit) systems at low temperatures has proven the necessity of having nearby cryogenic electronics to enable fast and efficiently-controlled manipulation and read-out of a large number of qubits [1], [5], [6]. In this respect, the recent demonstrations of silicon qubits could be combined with state-of-the-art CMOS electronics [7]–[9].

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The 28nm fully-depleted silicon-on-insulator (FD-SOI) MOSFETs with undoped channel have numerous advantages for low-temperature applications compared to Si bulk transistors, such as the reduced impact of dopant freeze-out, reduced variability, tuning of threshold voltage thanks to back-biasing, higher mobility, and quasi-ideal electrostatic control [10], [11].

The present study focuses on the exponential gate-voltage ($V_{GS}$) dependence of the subthreshold drain current $I_D$ of a MOSFET as a function of the temperature $T$ captured by the subthreshold swing $SS(T) = dV_{GS}/d\log I_D = m \ln 10 k_B T/e$ (SS(300 K) = 60 mV/dec for $m = 1$), where $k_B$ is the Boltzmann constant and $e$ the absolute elementary charge. The factor $m = (C_{ox} + C_{it})/C_{ox} \geq 1$ takes into account the capacitance of the interface traps $C_{it}$ with respect to the geometric gate capacitance $C_{ox}$ (in our case of FD-SOI, the depletion capacitance can be neglected). The very small value of $SS$ in the (sub)K-range results in an ideal $I_D(V_{GS})$ switch leading to a high on/off current ratio and low power dissipation in the stand-by regime.

Cryogenic investigations of $SS(T)$ in advanced CMOS devices reveal at least one order of magnitude larger values at 4 K compared with the expected value $SS(4K) = 0.79$ mV/dec for $m = 1$. For bulk MOSFETs, typical values for SS(4K) range from 30 to 10 mV/dec [3], [4], [13], [14]. Even though an effective operation of different SOI technologies at cryogenic temperature has been demonstrated, the reported SS values turned out to be as high as 7 mV/dec at 4K [15]–[18], even at sub-1K temperatures [19].

Common explanations correlate the $SS(T)$ dependence in bulk Si transistors to an important increase of the density of interface traps $D_{it}$ close to the band edges [20]. Similarly, for planar SOI devices, the increase of $D_{it}$ has been demonstrated to extend more than 100 meV inside the band gap using the spectroscopic charge-pumping technique [21]. However, especially at the lowest temperatures, analyzing the saturation with a strongly temperature dependent increase of $m$ via $C_{it} = e^2 D_{it}$ leads to an estimate of unrealistic $D_{it}$ values that are even larger than the silicon density of states of free carriers [19]. More recently, a constant contribution to $SS(T)$ has been derived at 4 K by modeling the thermal occupation of the interface-trap distribution [17], [22]–[24] which needs temperature-specific modeling for an application to all temperatures.

In order to explain the cryogenic saturation of $SS$, we propose a new approach introducing a disorder-induced exponential tail in the density of states (DOS) for the calculation of the subthreshold charge-carrier transport. The model is...
validated on the experimental data of long- and short-channel MOSFETs with different oxide thicknesses in terms of both $SS(T)$ and $SS(I_D)$ dependences from 300 K down to 4.3 K.

II. EXPERIMENT

Thin (GO1) and thick (GO2) gate oxide low-threshold-voltage (LVT) FD-SOI transistors were fabricated with a gate-first high-$k$ metal gate by STMicroelectronics on 300 mm (100) SOI wafers with a buried oxide thickness of 25nm [11], [25]. The equivalent oxide thickness (EOT) is 1.55 nm for GO1 and 3.7 nm for GO2. The 7 nm-thick channel is undoped.

Both n-type and p-type long-channel GO2 (gate length $L = 0.15, 2 \ \mu$m and width $W = 2 \ \mu$m) and n-type short-channel GO1 ($L = 28.34 \ \text{nm}$ and $W = 80,210 \ \text{nm}$) transistors were investigated. P-type short-channel devices couldn’t be analyzed for the $SS(T)$-dependence because of oscillatory variations in $SS(I_D)$ below threshold at cryogenic temperatures. This results from the enhanced boron diffusion from the source/drain regions affecting subthreshold current at low $V_{DS}$ (see [18], [26]).

The transistors cleaved from a wafer were mounted to the sample holder of a cryogenic probe station equipped with 4 adjustable contact needles connected to Source/Measurement Units. Then, they were cooled down under continuous He flow with temperature regulation between 4 and 300 K. The data acquisition was done using a parameter analyzer (HP 4155A).

Fig. 1a shows $I_D(V_{GS})$ at temperatures between 300 and 4.3 K for the n-type long- and short-channel devices at $|V_{DS}| = 50$ mV and back-gate voltage $V_{BACK} = 0$ V. Both cases reveal a classical, oscillation-free $I_D(V_{GS})$ down to the lowest temperatures. The saturation of $SS(T)$ below about 40 K can be clearly seen from the $SS(I_D)$ data as illustrated in Fig. 1b. The same trend holds for p-type long-channel and n-type short-channel devices.

In Fig. 1c, $SS(T)$ from 300 K down to roughly 40 K follows the expected dependence $m_{1,2} \ln 10 \ \text{k} T/e$ with $m_1 = 1.14$ for the long devices and $m_2 = 1.23$ for the short device. The slightly higher $SS$ (described by $m_1 = 1.14$) for the long devices is explained by the presence of interface traps ($C_p$), and the larger $m_2 = 1.23$ follows from additional electrostatic short-channel effects [27]. $SS(4.3 \ \text{K})$ saturates at 7.3 mV/dec for n-type long-channel, 7.4 mV/dec for p-type long-channel, and 7.7 mV/dec for n-type short-channel.

III. MODEL DESCRIPTION AND DISCUSSION

The diffusive subthreshold transport is proportional to the density $n$ of the mobile charge carriers in the channel assuming a constant diffusion constant (mobility) [12]. Using the Fermi-Dirac statistics for the occupation of electron states [27], [28], here for the n-type case, $n$ can be expressed as a function of the semiconductor potential $\Psi_s$ via

$$ n(\Psi_s) = \int_{-\infty}^{\infty} f(E)N_{c}^{2D}(E)\,dE $$

with the Fermi function $f(E) = 1/(e^{(E-E_F)/k_BT} + 1)$ and a step function for the two-dimensional DOS $N_{c}^{2D}(E)$ from zero to $N_{c}^{2D} = g_e m^*/\pi \hbar^2$ at the band edge $E_c = E_0 - e\Psi_s$.

For the flat band condition with $\Psi_s = 0$, the Fermi energy $E_F$ is taken at mid-gap with $E_0 = 0.55 \ \text{eV}$ (considering a temperature-independent energy gap 1.1 eV for Si). Other parameters are the valley degeneracy $g_v = 0.19 m_0$ (free-electron mass $m_0$). Finally, the equilibrium electron density $n(\Psi_s)$ can be transposed to $n(V_{GS})$ using $V_{GS} = \Psi_s + n(\Psi_s)/C_{ox}$ [27], for the sum of the semiconductor potential $\Psi_s$ and the voltage drop $n/eC_{ox}$ over the geometric gate capacitance $C_{ox}$ $= k T_0/t_{EOT}$ [Fm$^2$] supposing $m = 1$. $\epsilon_0$ is the free-space permittivity, $k = 3.9$ the relative dielectric constant of SiO$_2$, and $t_{EOT} = 3.7$ nm the equivalent oxide thickness in case of GO2.

The calculated $n(V_{GS})$ data for a sharp band edge reveal the standard exponential dependence $I_D \sim e^{V_{GS}/k_BT}$, confirming the linear temperature dependence $SS(T) = \ln 10 \ \text{k} T/e$. However, only using the Fermi-Dirac statistics is not enough to explain the experimentally observed saturation at low temperatures as shown in Fig. 1c.

To describe the saturation of $SS$ at low temperatures, a broadened band edge [29], [30] was added to the DOS in the form $N_{D}^{2D}(E-E_c)/k_BT_0$ for $E < E_c$ (inset in Fig. 2c). The parameter $k_BT_0$ quantifies the extent of the exponential tail resulting from, e.g., crystalline disorder, residual impurities, and strain, surface roughness, etc. Assuming a proportionality between $I_D(V_{GS})$ and $n(V_{GS})$, the calculated $I_D(V_{GS})$ is shown in Fig. 2a for different temperatures with $T_0 = 35$ K (resulting in $k_BT_0 = 3$ meV). A saturation value $SS(T \leq T_0) = \ln 10 \ k_BT_0/e = 6.9$ mV/dec is obtained for $m = 1$ (see Fig. 2b). The 3 meV tail was determined empirically to describe the experimental $SS(4.3 \ \text{K})$ of 7-8 mV/dec.

To compare with the model, the saturation values $SS(T)$ in the weak inversion measured at $I_D = 10 \ \text{pA}$ are plotted in Fig. 2c after normalization with the corresponding $m_{1,2}$ (for the values, see Fig. 1c). It should be noted that the chosen
Subthreshold swing, SS (mV/dec)

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Fig. 2. a) Calculated $I_D(V_{GS})$ for the model parameters given in the main text, assuming an exponential tail below the conduction band edge with $k_B T_0 = 3$ meV. b) Calculated $SS(I_D)$. c) Calculated $SS(T)$ compared to experimental data normalized by $m_1 g$ (symbols) and to $\ln 10 k_B T/e$. The inset shows a schematic representation of the exponential tails of the Fermi distribution function $f(E)$ for $E > E_F$ and of the DOS $N^2D(E)$ for $E < E_c$. The product of $f(E)$ and $N^2D(E)$ for $T < T_0$ gives the distribution of occupied states with a maximum around $E_F$.

$k_B T_0$ gives a good description of the experimental data for all studied MOSFETs. The obtained exponential extent for the band tail is comparable to that of 2-10 meV probed with Electron Spin Resonance on Si MOSFETs in [31].

FD-SOI cryogenic back-biasing was already demonstrated to be efficient down to 4 K [32]. By using forward-back-biasing (FBB), the conductive channel can be displaced towards the Si-BOX interface. Therefore, if the increase of $D_{it}$ was responsible for $SS(T)$ saturation, one would expect a significant difference in $SS(I_D)$ profiles. However, the experimental data in Fig. 3a and 3b for an n-type device at 4.3 K reveal that $SS(I_D)$ curves hardly change for $V_{BACK}$ up to 3 V, implying that the edge-broadened DOS cannot be explained with just $D_{it}$ at the Si-SiO$_2$ interface.

At the lowest temperatures, the measured $SS(I_D)$ characteristics reveal an increased gate-voltage dependence (Fig. 1b) as compared to the constant $SS(I_D)$ from our calculations (Fig. 2b). This variation of $SS(I_D)$ can also be modeled by including an energy dependence $m(E)$ in the relation $V_{GS}(\Psi_s) = m(\Psi_s)\Psi_s + n(\Psi_s)e/C_{ox}$, similarly to the description of the interface traps below the band edge with the additional capacitance $C_{it}$ in the introduction. In Fig. 3c the calculated $SS(I_D)$ is shown for an exponential dependence $m(E) \sim e(E - E_c)/E_m$. A good agreement with the experimental data is found for a variation of $m(E)$ from 1.14 to 1.34 with an empirically-determined energy range $E_m = 10$ meV below $E_c$. Regarding the physical reasoning behind the improved model which includes $m(E)$, we note that not all the states in the band tail contribute to the transport [33]. Therefore, the $V_{GS}$-induced occupation of states in the band tail influences both the subthreshold current due to mobile states and the efficiency of gate control via $m(\Psi)$ because of trapped states.

IV. CONCLUSION

To explain the generally observed saturation of $SS$ at low temperature in FD-SOI MOSFETs, an exponential tail at the band edge is introduced yielding $I_D(V_{GS})$ of the form $e^{-V_{GS}/k_B T_0}$ that replaces the usual temperature dependence $e^{-V_{GS}/k_B T}$ for $T > T_0$. The determined $T_0 = 35$ K holds for all measured FD-SOI devices with long- and short-channel lengths for different oxide thickness and accurately describe the $SS(T)$ from 300 K down to 4.3 K. In addition, we address the problem of the increased cryogenic $SS(V_{GS})$ dependence at low temperatures and successfully model a non-constant $SS(I_D)$ profile below $V_{TH}$ by introducing an energy-dependent $m(E)$ in the gate-control efficiency. Finally, our results indicate that the implementation of band-tail broadening could form an important technological parameter for the correct modeling of MOSFETs at low temperatures.

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