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On the depletion behaviour of low-temperature covalently bonded silicon sensor diodes

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Abstract: Low temperature covalent direct wafer-wafer bonding allows for the fusion of multiple semiconductor wafers without any additional material at the bonding interface. In the context of particle pixel detectors this might provide an alternative to bump-bonding for joining sensors to readout chips. Previous investigations have shown that the amorphous layer formed at the interface during bonding is detrimental to charge propagation. To investigate the influence of the bonding interface on signal collection we have fabricated custom test structures by bonding high-resistivity N to high-resistivity P-type silicon wafers thus forming P-N junctions. Scanning transmission electron microscopy shows indeed the formation of ca. 3 nm wide amorphous layer at the interface. Using a scanning transient current technique (TCT) setup we were able to record generated signals. Illuminating our sample with light of different wavelengths and from different sides, indicates that the P side of the bonded structures can be fully depleted, but not the N side. This indicates a strongly asymmetric depletion behaviour which we attribute to the presence of the bonding interface.

Keywords: Si microstrip and pad detectors; Solid state detectors; Charge transport and multiplication in solid media; Detector design and construction technologies and materials

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1 Introduction

One of the challenges of building highly efficient X-ray imaging detectors, is the stochastic interaction of X-ray photons with matter dominantly via the photoelectric effect. This applies to the X-ray energy ranges commonly used in medical X-ray applications, ranging up to 100 keV. Within this range, the probability of an X-ray photon being absorbed within a certain detector volume is closely related to the atomic number of the material used and its density. Silicon (Si) is the material of choice for implementing particle/radiation pixel detectors, due to the availability and relative affordability of silicon semiconductor processing. But from the perspective of X-ray interaction silicon is not an ideal detector material [1]. This is for instance the case for X-ray photons with an energy $E_\gamma = 30$ keV which lies in the energy range often used for medical mammography examinations [2]. For medical applications, there is strong interest in having efficient pixel detectors, as this allows to obtain similar or higher quality images while at the same time exposing the patient to less radiation. In order to have a near 100% detection efficiency with a pure silicon detector, the interaction layer would need to be 2 cm thick. Such thick detectors are impossible to manufacture with modern silicon semiconductor fabrication processes. The standard wafer thickness for a 200 mm silicon process is ca. 700 μm. This motivates the interest in different types of semiconductor interaction materials such as gallium-arsenide (GaAs) or cadmium-telluride (CdTe), also called high-Z materials. Highly efficient X-ray detectors can be built with reasonably thin layers of these alternative semiconductor materials. But this only concerns the interacting part of an X-ray pixel detector. For economic reasons it is impossible to fabricate the integrated electronic circuits necessary for pixel detectors in GaAs or CdTe. In order to build a highly efficient X-ray pixel detector it is extremely convenient to combine readout electronics implemented with standard silicon processes together with interaction layers made of high-Z materials. It is possible to build such detectors, based on the hybrid manufacturing approach. Hybrid detectors are created by separately fabricating the interaction layer (called the sensor) and the readout electronics. The two parts are then joined together used bump bonding [3]. Due to the separate processing of the sensor part which usually consists of a simple implanted P-N junction, it is possible to create
hybrid detectors, where the sensitive layer is made of a high-Z material [3]. We investigate a novel approach for assembling high-Z particle pixel detectors based on a low-temperature covalent wafer-wafer bonding process. Low temperature covalent wafer-wafer bonding is routinely utilized in the production of micro-electromechanical systems (MEMS) to encapsulate structures [4], as well as in the production of high efficiency solar cells [5]. This bonding process enables the fusion of semiconductor materials without any additional material at the interface. The process allows to bond different materials together, such as bonding a GaAs wafer to a Si wafer. In the ideal case this would lead to abrupt hetero-junctions at the bonding interface. As the bonding process is carried out at or near room temperature, it is compatible with fully processed CMOS wafers. Materials with different thermal expansion coefficients can also be considered. This would allow to combine readout circuits fabricated using standard silicon processes with a wide range of different interaction materials, such as Ge, GaAs or CdTe. The bonding is carried out at a wafer level, which enables mass processing compared to bump-bonding which usually occurs on a chip basis.

The covalent bonding process is based on the principle of spontaneous covalent bonding between two wafers with dangling bonds at their surface [6]. The bonding process involves the following steps, which are all carried out under ultra-high vacuum \((p < 5 \times 10^{-8} \text{ mbar})\): both wafers are introduced into the vacuum and the surface of the first wafer is sputter-cleaned via either an argon beam or an argon plasma [4, 7].\(^1\) The sputter-cleaning removes any contaminants at the surface of the wafer as well as the thin native oxide layer formed on top of the silicon crystal. Due to the removal of the oxide layer, dangling (or activated) silicon bonds are generated at the surface. The second wafer is treated in the same way as the first one. The activated surfaces of both wafers are then brought in contact. Given that the entire process is carried out in ultra-high vacuum, very little to no re-oxidation of the activated surfaces can occur. Therefore the activated bonds at the two surfaces spontaneously bond under moderate pressure. The resulting wafer-wafer bond is oxide-free and the mechanical bond strength approaches or equals the semiconductor bulk strength [4]. High-temperature annealing is unnecessary for achieving high bond strengths, which ensures the compatibility of the process with fully processed CMOS wafers [7]. Figure 1 shows a schematic view of the bonding process. The surface activation via argon beam or argon plasma does not only remove the native oxide and contaminants, but it also attacks the surface of the semiconductor to be bonded. This leads to damages in the crystalline structure of the semiconductor and by extension to an amorphous layer at the location of the bonding interface. The thickness of this bonding interface is typically of the order of a few nano-meters, but amorphous layers as thin as 0.5 nm have been reported in literature [7]. The result of this amorphous layer is the presence of bulk defects in the region around the bonding interface. These bulk defects influence the electrical properties of the bonded structure. When using covalent wafer bonding for steady-state applications (for example solar cells), the effects of the bulk defects can be mitigated by including high doping concentrations at the interface [8]. This type of mitigation is not directly applicable to the fabrication of pixel detectors, since having highly-doped concentrations in the interaction layers will increase the necessary voltage for fully depleting the sensitive volume. Additionally, in

\(^1\)While argon is the most commonly used gas for surface activated bonding, the use of different noble gases such as neon has also been explored [4].
Figure 1. Conceptual view of the different steps of the surface activated covalent bonding method. Processing is carried out in high-vacuum (\(<5 \times 10^{-8}\) mbar). Contamination and oxide layers at the surface are removed using an argon beam, leaving behind activated dangling atom bonds. Bringing together two activated wafers leads to spontaneous bonding without the use of high temperatures.

In the context of pixel detectors, the steady-state effects of the bulk defects are secondary. Our main interest lies with the transient effects occurring when a signal pulse crosses the bonding interface.

So in order to build efficient detectors in the future based on low-temperature direct wafer-wafer bonding, the effects of the defects at the bonding interface need to be studied in detail. Previous work in [9] has investigated the usage of Si/Si wafer bonds for pixel detectors with Schottky diode based samples. The bonded wafers had the same doping type. Using transient current technique (TCT) measurements it was observed that the bonding interface blocks the passage of generated charge clouds. In [10] p-Si/p-Si wafer bonded structures were fabricated, and the forward and backward bias currents were analysed. Again an influence of the bonding interface was observed reducing the conductivity of the bonded structure. In both of these works, an alternative approach was proposed which might mitigate these observed problems. This alternative approach is to bond wafers of different types, so bonding a P-type to an N-type wafer, therefore creating a P-N junction located at the bonding interface. Under reverse bias, this structure would start depleting from the bonding interface, thus ensuring a high electric field at the bonding interface which is expected to facilitate charge transport across the interface. This approach is studied in the present work. For simplicity reasons, as in the cited publications, this first investigative attempt is done with structures entirely composed of silicon. Once the simple case of silicon bonded to silicon is understood, future investigations will analyse the creation of hetero-junctions, for example GaAs bonded to silicon.

2 Pad diode test structures fabrication

To evaluate the influence of the bonding interface on charge transport and signal collection, we fabricated custom test structures. Each test structure is a pad diode, where the P-N junction is formed by bonding a P-type wafer to an N-type wafer. Figure 2 (left) shows the cross-section of such a test structure. Ion beam implantation on the outer surfaces of the wafers form ohmic contacts between the silicon bulk and the metal used for contacts [11]. The contact doping concentration at the wafer surface is targeted to be in the order of \(N_c \approx 10^{20} \text{ cm}^{-3}\). The metal contacts are formed
by a layered stack of chromium (as an adhesion layer), aluminium and gold (to prevent oxidation). On the N side guard rings are formed around the main central contact, in order to be able to reduce the leakage current across the diode edges. Experimentally we found that this was not necessary.

**Figure 2.** Left: schematic view of the cross-section of the fabricated test structures. A high resistivity N-type silicon wafer is bonded to a high resistivity P-type wafer. Each wafer has high-dose implants at the surface in order to ensure good ohmic conduction between the silicon substrate and the metal contacts. Image not to scale. — Right: P side of a fully processed wafer pair.

Diodes with contact edge lengths of 2 mm, 4 mm, 6 mm, 8 mm and 12 mm are fabricated on the same wafer. A subset of the diodes on each wafer have circular metal openings centred on the contact, which will be used for TCT measurements. Figure 2 (right) shows an image of a fully processed wafer pair where the arrangement of different diode sizes can be seen. As substrates we used 100 mm (4′′) high resistivity N and P-type float zone wafers, as are used for fabrication of particle pixel detectors. The specifications of the used wafers are presented in table 1.

| Type          | Orientation | Size      | Thickness | Resistivity | Doping          |
|---------------|-------------|-----------|-----------|-------------|-----------------|
| P (Boron)     | ⟨100⟩       | 100 mm    | 500 ± 7 μm | >10 kΩ cm   | <2 × 10^{12} cm\(^{-3}\) |
| N (Phosphorous)| ⟨100⟩       | 100 mm    | 490 ± 8 μm| 7–10 kΩ cm  | (4–6) × 10^{11} cm\(^{-3}\) |

An overview of the processing steps is shown in table 2. Processing was carried out in the Binnig and Rohrer Nanotechnology Center (BRNC) cleanroom of ETHZ/IBM as well as in the Center of MicroNanoTechnology (CMI) at EPFL. Certain steps were carried out with external companies, namely the ion beam implantation with *Ion Beam Services S.A.* [13], chemical-mechanical polishing (CMP) with *Optim Wafer Services* [14], wafer-wafer bonding with *EV Group GmbH* [15] and laser dicing with *Synova S.A.* [16].

CMP of the backside ensures that the RMS roughness of the wafer surfaces to be bonded is <1 nm [5]. Additionally during the same process step, ca. 25 μm of silicon was removed from the backside, in order to remove any contamination from the previous processing steps.
Table 2. Processing steps for the fabrication of the bonded test structures. Up to step 6 wafers were processed individually. Starting from step 8 wafers were processed as bonded pairs. Entries in *italic* were carried out by external partners.

| Step | N-Wafer                  | P-Wafer                  |
|------|--------------------------|--------------------------|
| 0    | Alignment marker etching | Alignment marker etching |
| 1    | 20 nm PECVD cap oxide    | 20 nm PECVD cap oxide    |
| 2    | Implant photolithography | Implant photolithography |
| 3    | *Ion beam implantation*  | *Ion beam implantation*  |
|      | (8 × 10^{15} cm^{-2}@30 keV) | (6 × 10^{15} cm^{-2}@80 keV) |
| 4    | Cap oxide removal        | Cap oxide removal        |
| 5    | Doping activation        | Doping activation        |
|      | (50 min@1050°C)          | (70 min@1050°C)          |
| 6    | Backside polishing with CMP | Backside polishing with CMP |
| 7    | Wafer-wafer bonding      |                         |
| 8    | N side metal evaporation |                         |
| 9    | N side metal lift-off    |                         |
| 10   | P side metal evaporation |                         |
| 11   | P side metal lift-off    |                         |
| 12   | Laser dicing             |                         |

Figure 3. Left: SAM measurement of a bonded wafer pair indicating a good bond quality with one void due to a contaminating particle. — Right: STEM image of the bonding interface for the same pair, showing an amorphous layer in between the two crystalline silicon wafers.

2.1 Fabrication quality control

Quality control of the bonded pairs was carried out with scanning acoustic microscopy (SAM) measurements by the bonding company. The SAM measurements show a good bond quality with
some voids due to contaminating particles. Figure 3 (left) shows an example SAM measurement. In order to evaluate the width of the amorphous layer at the bond interface, scanning transmission electron microscopy (STEM) measurements were carried out at ScopeM — ETH Zürich using a Hitachi HD 2700 STEM. Figure 3 (right) shows the result of these STEM measurements.

We estimated the width of the amorphous layer via numerical image processing. After rotating the image in order to have the interface vertically aligned, we calculated the average image intensity in function of the \((x)\) axis perpendicular to the bonding interface. Figure 4 shows the resulting curve (in arbitrary units) overlaid onto the STEM image. The amorphous layer on average has a higher image intensity. The increase in intensity at the left (resp. right) side transition from crystalline to amorphous material is then fitted using a modified error function (ERF)

\[
I_{L,R}(x) = A \cdot \text{erf} \left( \frac{x - \mu_{L,R}}{\sqrt{2} \sigma_{L,R}} \right) + I_{\text{offset}}.
\]

We find the following width for the amorphous interface

\[
d_{\text{amorph}} = (\mu_{R} - \mu_{L}) \pm (\sigma_{R} + \sigma_{L}) = 2.97 \pm 0.75 \text{ nm}.
\]

**Figure 4.** Estimation of the width of the amorphous layer. The overlayed white graph shows the average image intensity along the \(x\) axis. The two red dashed lines show the fit of the modified ERF for each edge of the amorphous layer. The estimated width of the amorphous layer is calculated based on the \(\mu\) and \(\sigma\) of the two fitted ERF.

The mask set of our process includes transfer length method (TLM) structures which we use for assessing the quality of the fabricated ohmic contacts [17]. The contact resistivities measured with the TLM structures are in the order of \(\rho_{\text{Contact}} \approx 0.05 \Omega \text{ cm}^2\). Accordingly we expect contact
resistance of the order of $1 \Omega$ for our smallest ($2 \times 2$ mm) pad diodes. This is negligible in context of the high resistivity substrates and confirms the fabrication of good ohmic contacts.

3 Transient current technique measurements

Scanning TCT measurements were carried out using the Large Scanning TCT setup acquired from Particulars [18] shown in figure 5 (left). Reverse bias is supplied by a Keithley 2410 SMU via the bias tee supplied by Particulars. For our analysis we use two different lasers, one with a wavelength of 660 nm (red laser) and one with a wavelength of 1064 nm (IR laser). Illumination with the red laser emulates the interaction of an alpha particle, in the sense that all the red light (the energy) is absorbed close to the sensor surface. Illumination with the IR laser gives a minimum ionizing particle (MIP) like interaction, as the IR laser beam penetrates the entire sensor and is not fully absorbed. But while the MIP interaction is constant over the entire thickness of the sensor, the IR laser beam is attenuated and the laser intensity decreases exponentially within the sensor.

Figure 5. Left: TCT setup with a test structure installed in a custom diode holder. — Right: example curves recorded when illuminating our samples with the red laser from the P side.

A pad diode with a contact size of 4 mm was used for the in-depth analysis. The diode has a 1 mm diameter metal opening on each side and, accordingly, we carried out laser illumination from the P and the N side of the diode. Focusing of the TCT laser was carried out with a standard knife-edge scan making use of the edge of the metal opening [19, 20]. Signals were recorded with a Lecroy Waverunner 8104 oscilloscope with a bandwidth of 1 GHz and a sampling rate of 20 Gsps. For each recorded data point we averaged 1000 acquisitions in order to remove any (non correlated) noise. We acquired reverse bias scans for bias voltages up to $|V_{\text{Bias}}| = 650$ V for all combinations of red and IR laser, and P side and N side illumination. Figure 5 (right) shows example curves recorded when illuminating the P side with the red laser.

In addition to the averaging of the curves using the oscilloscope, the recorded curves pass through two additional pre-process steps before analysis. To remove any constant offset in the signal, the mean signal value up to the trigger point is calculated (average over ca. 30 ns of signal) and subtracted from the entire curve. The raw recorded signals have a superposed sinusoidal
interference at a frequency of \( f_{\text{sin}} \approx 290 \text{ MHz} \). We apply a notch filter with a centre frequency of \( f_c = f_{\text{sin}} \) and a quality factor of \( Q = 1 \) to filter out this sinusoidal interference.

### 3.1 Results

TCT signals could be recorded in all four cases mentioned above, except in the case of illuminating the N side with the red laser. Up to a bias voltage of \(|V_{\text{Bias}}| = 650 \text{ V}\) no signal was observed in this case. For the other three cases, the integrated pulse amplitude (i.e. the collected signal) as a function of the bias voltage is shown in figure 6. It is immediately visible that in all three cases a maximum of collected charge is reached at bias voltages below 100 V. In the case of the illumination with the red laser, this maximum is reached at ca. \( V_{\text{Red}} \approx 82 \text{ V} \). In the case of illumination with the IR, the maximum is reached at ca. \( V_{\text{IR}} \approx 92 \text{ V} \).

![Figure 6. Integrated pulse amplitude in function of the applied bias voltage for different cases of TCT illumination. The decrease in collected signal beyond 100 V in the case of IR laser pulses is currently unexplained and subject to further research.](image)

The depletion region under reverse bias always grows from the P-N junction outwards. In the case of red illumination on the P side, we observe a plateau in signal being collected at \( V_{\text{Bias}} > V_{\text{Red}} \). At \( V_{\text{Bias}} < V_{\text{Red}} \) we see an exponential increase in collected signal. This indicates that \( V_{\text{Red}} \) is the voltage at which the electric field effectively reaches the surface of the P side, and therefore is equal to the voltage necessary to fully deplete the P wafer. At this voltage, the N side does not appear to be fully depleted, as otherwise a signal would also be observed under red laser illumination from the N side. One would expect the depletion region to grow further into the N side at \( V_{\text{Bias}} > V_{\text{Red}} \) and thus the signal collected should also further increase beyond \( V_{\text{Bias}} > V_{\text{Red}} \) due to the longer drift distance (Ramo’s theorem [21]). In conclusion, from the perspective of the charges collected on the P side, the drift distance seems to be limited to the width of the P wafer.

Under IR illumination the observed behaviour is more puzzling. Not only is the voltage at which the maximum is observed \( V_{\text{IR}} \) higher, but also there is a very pronounced decrease in detected
signals at $V_{\text{Bias}} > V_{\text{IR}}$. At $V_{\text{Bias}} \gg V_{\text{IR}}$ the observed signal under IR illumination eventually reaches a steady state value. Under IR light illumination free charges are generated on both sides of the bonding interface. Therefore, even under the assumption that the bonding interface inhibits the drift of charge carriers, any increase in the depletion region in the N wafer should still lead to an increase in signal collected. The observation, that the two voltages $V_{\text{IR}}$ and $V_{\text{Red}}$ are very close together, gives a hint, that any depletion of the N-wafer at $V_{\text{Bias}} > V_{\text{Red}}$ is very limited in size. All of this implies that there is a strongly asymmetric depletion behaviour between the P and N side of our structures. We attribute this behaviour to the presence of the bonding interface. A total of six samples have been tested and the results from all six samples are consistent. The different samples showed variations in the voltage necessary for full depletion, which we attribute to differences in the precise substrate doping of each sample. Upcoming edge TCT measurements should give us a more detailed and precise view of the exact depletion behaviour of these structures.

4 Conclusions

We fabricated custom pad diode test structures based on low-temperature covalent wafer-wafer bonding of high resistivity N to P-type silicon wafers. Implanting a highly doped layer at the surface of each wafer allows for good ohmic contacts. The inspection of the wafer-wafer bond with SAM measurements shows a good bond quality over the entire wafers. STEM measurements of the bonding interface show a ca. 3 nm thick amorphous layer at the bonding interface, which originates from the surface activation via an argon beam during the bonding process. Transient signals could be observed in our samples when illuminated using a TCT setup with red and IR laser pulses. Bias dependent measurements with the red laser indicate that a full depletion of the P side is possible, but not of the N side. The same measurements are consistent with the drift of charges not crossing the bonding interface. Together with the results from the IR laser measurements we observed a highly asymmetric depletion of the P side versus the N side. Further measurements will give more details about the exact shape of the depletion of our samples.

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