Abstract—When we study the Karnaugh map in the switching theory course, we learn that the ones in the map must be combined in groups of $a \times b$ elements, being $a$ and $b$ powers of two. The result is the logic function described as a sum of products. This paper shows that we can also make groups where $a$ and/or $b$ are equal to three. This does not result in a sum of products, but in a logic function that is simpler than the sum of products in terms of logic gates. This idea is extended later in the paper to groups of $2^n - 1$ elements.

Index Terms—Boolean algebra, digital circuits, groups of non-power-of-two elements, Karnaugh map, logic function, simplification.

I. INTRODUCTION

When we study the Karnaugh map [1], [2], we learn that the ones in the map must be combined in groups of $a \times b$ elements, where $a$ and $b$ are powers of two [1]. Other shapes and rectangles of other sizes are not allowed. A simple example is when there are three ones in a row of the Karnaugh map, as shown in Fig. 1(a). In this case, two groups of two elements are created. One with the first element and the middle one and the other group with the middle element and the last one. The alternative shown in Fig. 1(b), where three elements are grouped together, is not allowed.

When the rule for grouping elements is followed, the result is a logic function represented as a sum of products (SOP). This representation has the advantage that it leads to a circuit with low delay [3]. By contrast, the resulting circuit is generally not efficient in terms of the number of logic gates. For this reason, it is reasonable to wonder why we look for a SOP representation if it does not lead to hardware-efficient results. This question should make us reconsider the motivation to use the Karnaugh map. As achieving a hardware-efficient circuit is a main goal when designing a digital circuit, we should figure out ways to provide it, such as current optimization methods to simplify boolean functions [2]–[5]. Conversely, achieving low delay, as the Karnaugh map actually does, is a usually a secondary goal in most digital designs. In this sense, the aim of the current paper is to provide a new perspective to the Karnaugh map that makes it suitable for the design of hardware-efficient circuits, not only low delay ones. This is done by a new way to group the ones in the Karnaugh map that considers groups of a number of elements that is not a power of two. This widens the understanding of the Karnaugh map and makes it a more powerful tool.

The proposed approach is developed in the paper as follows. First, making groups of three, six and nine elements is studied in Section II. Then, the ideas are generalized to groups of $2^n - 1$ elements in Section III, which completes the approach. Later, in Section IV it is explained how to use the proposed approach to improve the explanation of the Karnaugh map. Finally, the main conclusions of the paper are summarized in Section V.

II. MAKING GROUPS OF THREE, SIX AND NINE ELEMENTS

Figure 1(a) shows how to group three ones in a Karnaugh map according to the conventional approach, which consist of making two groups of two elements. The logic function for this case is

$$\text{(1)}$$

$$f = a\overline{c}d + b\overline{c}d,$$

which can be implemented with 5 2-input logic gates. As a general criterion throughout the paper, the number of logic gates is counted as the number of 2-input logic gates.

The alternative presented in Fig. 1(b) groups all the three elements together. In this case, the second row corresponds to $\overline{c}d$, whereas the three last columns correspond to the function $a + b$. This leads to

$$\text{(2)}$$

$$f = (a + b)\overline{c}d,$$

which can be implemented with 3 logic gates. Therefore, grouping three elements together is more hardware-efficient than making two groups of two elements.

This idea can be extended to groups of three elements that form an $L$ shape, as is shown in Fig. 2. The three ones in the center correspond to $bd (\overline{c} + a)$ and those in the corners correspond to $\overline{b}d (\overline{c} + \overline{a})$.

When there are two groups of three elements that intersect as in Fig. 3 the conventional approach in Fig. 3(a) obtains the logic function by making three groups of two elements, which results in

$$\text{(3)}$$

$$f = b\overline{c}d + a\overline{b}\overline{c} + \overline{a}bd.$$
Fig. 2. Example where groups of three elements are made and these groups have an L shape.

Fig. 3. Two groups of three elements. (a) Conventional approach. (b) Making groups of three elements. (c) Proposed approach.

The circuit used to calculate this equation requires 8 logic gates. By contrast, making groups of three elements as in Fig. 3(b) results in

\[ f = (a + b)\overline{c}d + (\overline{c} + d)\overline{ab}, \]  

(4)

which requires 7 logic gates. However, there is an even better alternative shown in Fig. 3(c), which consists of a group of two elements and a group of three elements and leads to

\[ f = b\overline{c}d + (\overline{c} + d)\overline{ab}, \]  

(5)

and requires 6 logic gates.

The examples in Figs. 1 and 3 lead to two interesting conclusions. First, a group of three elements is more hardware-efficient than two groups of two elements. Second, a group of two elements is more hardware-efficient than a group of three elements. These conclusions serve as decision rule when making the groups.

Another interesting case is when there is a square of \(3 \times 3\) ones, as shown in Fig. 4. The use of the conventional approach requires to make four squares of \(2 \times 2\) and leads to

\[ f = bd + ad + bc + ac, \]  

(6)

which requires 7 logic gates.

The alternative for this case is to group all the 9 elements together. The three last columns correspond to the function \(a + b\) and the three last rows to \(c + d\), which results in

\[ f = (a + b)(c + d). \]  

(7)

In this case, the calculation only requires 3 logic gates, which is a significant reduction of the hardware cost with respect of grouping the elements in squares of \(2 \times 2\).

As a final example of making groups with a number of elements that is multiple of three, Fig. 5 highlights the case of grouping 6 elements together. The conventional approach solves the Karnaugh map in Fig. 5(a) by making three groups of \(2 \times 2\), and obtains

\[ f = a\overline{c} + bd + ad, \]  

(8)

which requires 5 logic gates.

The alternative of using two groups of 6 elements in Fig. 5(b) results in

\[ f = a(\overline{c} + d) + (a + b)d, \]  

(9)

which also requires 5 logic gates.

Finally, by using a group of 6 elements and a group of 4 elements as in Fig. 5(c) the resulting logic function is

\[ f = a\overline{c} + (a + b)d. \]  

(10)

In this case, the number of logic gates is reduced to 4.

This example illustrates the facts that a group of 4 elements is more hardware-efficient than a group of 6 elements, whereas a group of 6 elements is more hardware-efficient than two groups of 4 elements.
III. MAKING GROUPS OF $2^n - 1$ ELEMENTS

The ideas for groups with a number of elements that is a multiple of three can be generalized to groups of $2^n - 1$ elements where $n \in \mathbb{N}$. These elements must be embedded in a rectangle of size $2^i \times 2^j$ where both $i, j \in \mathbb{N}$ and $i + j = n$. According to this, there will be a single element in the $2^i \times 2^j$ rectangle that is not a one. This element will be excluded from the group by using an OR function.

As an example, Fig. 6 shows a group of 7 elements. In this case, $i = 1, j = 2, n = 3, 2^1 \times 2^2 = 2^n = 8$ and $2^n - 1 = 7$. According to the conventional approach in Fig. 6(a), the ones are grouped in three groups of four elements, leading to

$$f = cd + bd + ad. \quad (11)$$

This logic function requires 5 logic gates.

According to the proposed approach, the ones are embedded in a rectangle of $2 \times 4$ whose logic function is $d$. Inside the rectangle, the function is $(a + b + c)$. This leads to

$$f = d(a + b + c), \quad (12)$$

which results in 3 logic gates. Again, this strategy reduces the number of logic gates.

IV. MAKING THE KARNAUGH MAP A MORE POWERFUL TOOL

The proposed approach allows for presenting the Karnaugh map as an optimization tool with two possible goals: To reduce the delay of the circuit or to obtain a hardware-efficient digital circuit.

In order to reduce the delay of the circuit, we derive the SOP expression with the conventional approach by using the following rules:

- Group the ones in the Karnaugh map in squares or rectangles of $2^i \times 2^j$ elements.
- Borders of the Karnaugh map are connected to the opposite borders, which allows to connect elements from both extremes.
- A one in the map may be included in one or several groups.
- Each group must include at least one that is not included in any other group. Otherwise, the group is redundant.
- Groups must be made with the aim of making the smallest number of groups and include the largest number of ones in these groups.

In order to obtain a hardware-efficient circuit, we incorporate the ideas presented in this paper and consider making groups of a number of elements that is not a power of two. This transforms the design rules into:

- Group the ones in the Karnaugh map in squares or rectangles of $a \times b$ elements where $a, b \in 1, \ldots, 4$, or groups of $2^n - 1$ elements embedded in a square or rectangle of size $2^i \times 2^j$, being $i + j = n$.
- Borders of the Karnaugh map are connected to the opposite borders, which allows to connect elements from both extremes.
- A one in the map may be included in one or several groups.
- Each group must include at least one that is not included in any other group. Otherwise, the group is redundant.
- Groups must be made with the aim of making the smallest number of groups and include the largest number of ones in these groups.

V. CONCLUSION

In this paper, a new way to understand the Karnaugh map has been presented. The new approach enables groups of ones whose size is not a power of two, which is not allowed in the conventional approach. As a result, the new approach allows for a further simplification of the logic functions, leading to digital circuits with smaller number of gates.

This enriches the explanation of the Karnaugh map, which can be explained as a tool to either minimize the delay of the circuit or reduce the number of logic gates.

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