DSP based current controlled single stage single phase integrated converter with external compensating signal for Class-C & Class-D appliances

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Abstract: Design and implementation of a current controlled single stage single phase integrated AC/DC isolated Power Factor Correction (PFC) converter is presented in this paper. With the integrated topology reduces the number control switches. The proposed converter has the advantage of low bulk capacitor voltage and only single control switch hence reduce in complexity in control and cost. Sub-harmonic oscillations which are produced in conventional current controller. By adding an external compensating signal effect of oscillations are reduced and performance of the converter is improved. The proposed scheme is implemented in real time by TMS320F2812 digital signal processor (DSP) board. The performance of converter is verified both experimentally and by simulation at different load and line conditions. The proposed converter is designed for 90–230 V, 50 Hz AC input, 48 V DC output and operating at 100 kHz switching frequency. The Experimental results shows that the DSP-based fuzzy controlled single phase single switch integrated PFC converter achieve high power factor and satisfies IEC-61000-3-2 and other European input current harmonic limits for Class-C & Class-D applications.

Subjects: Power & Energy; Electrical & Electronic Engineering; Digital Signal Processing; Electronics

Keywords: DSP; integrated converter; current control; IEC-61000-3-2; PFC

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PUBLIC INTEREST STATEMENT
An integrated converter is a synthesized device based on the overall system integration, which is simplified by the system objective and can implement the system functions similar to the discrete converters without integration. Simplification means the process of synthesizing converters with reduced components, smaller size, and lower weight or cost. System objectives can include minimum cost, maximum efficiency, high reliability, low power packing, wide conversion range, PFC and output regulation, inverter PFC, and better performance.

In this paper 1-phase integrated buck-flyback converter (IBFC) is analyzed, designed and implemented for Class-C & Class-D appliances. Experimental results of the proposed converter satisfy the IEC-61000-3-2 and other European standards.
1. Introduction

Based on the current harmonic limits by IEC-61000-3-2 and other European standards, electrical equipment are classified into four groups: Class-A, Class-B, Class-C and Class-D (Table 1).

At present many works have been developed in order to comply with IEC-61000-3-2 power supply to above groups is through power electronic converters. In literature two techniques are proposed to comply these regulations (Basu & Bollen, 2005; Huber, Zhang, Jovanovic', & Lee, 2001; Lu, Lu, & Pjevalica, 2008; Singh, Singh, Chandra, Al-Haddad, & Pandey, 2003).

1. Using passive elements like inductor, capacitor along with uncontrolled rectifiers. It is a good solution only for low power ratings and difficult to operate in universal range of input due to the large size of passive elements (Singh et al., 2003).

2. Other technique uses active power factor correction (PFC) circuit which consists of switching converter along with small size filter components. This technique reaches high efficiency and high power factor. Despite its expensiveness, complexity and EMI generation, this topology is considered as the best solution for high power levels and operating in universal range of input.

Active PFC techniques are of two types- single stage and two stage. Single stage topologies are boost, buck-boost or flyback converter. Major drawbacks with this topology are poor dynamic response and high switching stress (Basu & Bollen, 2005; Lu et al., 2008).

In two stage topology, first stage employees either buck or boost converter as a Power factor correction (PFC) and second stage consists of buck-boost derived topologies or flyback converter for power conditioning (PC). Though this topology gives unit power factor and fast dynamic response has drawback of high component size and cost.

An alternate solution to meet the IEC-61000-3-2 standards for Class-C & Class-D equipment is integrated single stage converter. This is formed by integration of PFC stage and PC stage. In this, single control switch shares the two stages. This converter performance is same as two stage topology with reduced component size and cost. There are different integrated topologies presented in literature (Alonso, Calleja, Ribas, Corominas, & Rico- Secades, 2004; Dalla Costa, Alonso, Marchesan, Cervi, & Prado, 2007; Dalla Costa et al., 2010). This paper focuses on integrated buck flyback converter (IBFC) as a power factor corrected converter. In IBFC, buck converter for PFC and flyback converter feeds supply to the load, both converters are operating in DCM to achieve high power factor.

Analog PFC control used to be the general commercial control for Class-C & Class-D equipment. Due to advantages like insensitive to parameter variations, more reliable, less number of passive components, now a days, digital control has become a competitive option. Digital control can be implemented using low cost microprocessor or Digital signal processor (DSP) or Field programmable gate array (FPGA). In literature, several analog and digital control approaches have been proposed to improve power factor and achieve regulated voltage (Buccella, Cecati, & Latafat, 2012; Gegner & Lee, 1996; Jiuming & Shulin, 2011; Murahari Rao, Kumar Jain, Reddy, & Behal, 2008; Yang et al., 2015; Ye & Jovanovich, 2005; Zhang & Feng, 2006).

| Table 1. Classification of electrical equipment |
| Class          | Equipment (Example)         |
|----------------|----------------------------|
| Class A        | Household appliances        |
| Class B        | Non-professional arc welding equipment |
| Class C        | Lighting equipment          |
| Class D        | Personal computers          |
In this paper, analysis and design of DSP (TMS320F2812) based Constant frequency Current Controlled Integrated buck flyback Converter with External ramp is implemented for Class-D & Class-C appliances to achieve high power factor and regulated voltage.

2. Integrated power converter
An integration criterion in switched mode converters reduces number of control switches and increases steadfastness of converter. Both features of buck and flyback converters are integrated into a converter named IBFC is implemented in this paper as shown in Figure 1. In this, buck converter is a PFC converter and flyback converter is a power control converter. Buck Converter consists of $L_b$, $D_c$, $D_a$, SW1, $C_b$, $V_p$ and Flyback Converter consists of $C_o$, $V_o$, $1:m$, $D_d$, $D_o$, $D_p$, $C_o$. Here SW1 is common for both the converters.

This converter operates in four stages,

**First Stage:** When SW$_1$ is on, buck inductor $(L_b)$ and flyback primary inductor $(L_f)$ are storing energy and output capacitance $(C_o)$ feeding load.

**Second Stage:** When SW$_1$ is off, buck inductor $(L_b)$ is discharging and flyback secondary inductance is discharging.

![Figure 1. Buck integrated flyback converter.](image)

![Figure 2. Operation of IBFC.](image)
Third Stage: Even before complete discharge of flyback secondary inductor energy, buck inductor discharges its energy completely.

Fourth Stage: In this, flyback secondary inductor discharges energy completely and output capacitor feeds load.

The above four stages of working are shown in Figure 2.

3. Digital current control with slope compensation
Due to high computational speed, high reliability and cost reduction now a day’s DSPs have been using extensively in various applications like control of drives, communication systems, intelligent systems etc. Figure 3 shows the block diagram of current controlled IBFC with external ramp by using DSP (TMS320F2812). This control approach contains two loops an inner current loop to achieve near unity power factor and outer voltage loop to achieve regulated voltage. The control to output transfer function without external signal has high frequency term, due to this sub harmonics will occur, so in inner loop a compensating signal is added to reduce sub harmonic oscillations. Control to output transfer function is,

$$\frac{1}{1 + \frac{s}{W_Q} + \frac{s^2}{W_n}}$$

(1)
where $Q_c$ is Quality factor, $m_c$ is slope of compensating ramp, $D$ is duty ratio, $W_n = \pi/T_s$, $T_s$ is switching frequency.

By selecting suitable value of $Q_c$, which is less than or equal to 1, then external signal slope can be adjusted to reduce sub harmonics. This compensation technique is implemented in TMS320F2812 processor by using library functions. Height of the external signal must be converted into digital value to subtract from DAC register over a switching period.

The flow chart shown in Figure 4 is used to accomplish the software.
4. Design example

In this section, design example is presented to define component values. Table 2 shows some of the
defined parameters. To meet IEC-1000-30-2 regulations, the minimum conduction angle is 130°
selected to achieve maximum powerfactor of 0.96 as in Alonso et al. (2004).

The voltage ratio ($m$) is calculated from the following relation;

$$m = \sin \frac{\pi - \theta}{2} = \frac{V_b}{V_p} = 0.4226$$

where $\theta$ is the conduction angle, $V_b$ is the bulk capacitor voltage, $V_p$ is the peak value of line voltage.
In the universal line voltage range (90–265 V) the minimum bulk capacitor voltage of 53 V and maxi-
mum value rises up to 158 V. In this design considered bulk capacitor voltage ($V_b$) = 137 V

Flyback converter resistance ($R_f$) = \[
\frac{V_b^2}{P_f} = \frac{137^2}{200/0.9} = 84.46 \Omega
\]

(4)

From the analysis of IBFC

$$R_b = \left( \frac{2L_b f}{D^2} \right)$$

$$R_f = \frac{2L_f}{D^2}$$

(5)

(6)

Table 2. Design parameters for IBFC

| Parameter         | Value                                      |
|-------------------|--------------------------------------------|
| Source voltage ($V_p$) | 90–265 V (R.M.S) universal input range |
| Load voltage ($V_o$)   | 48 V                                       |
| Load power          | 200 W                                      |
| Conduction angle ($\theta$) | 130°                                      |
| Switching frequency ($f_s$) | 100 kHz                                   |

Figure 5. MATLAB/Simulink model of current controlled IBFC with external compensating signal.
Figure 6. Source voltage and current waveform for \( V_{rms} \) of 150 V.

Figure 7. Source voltage and current waveform for \( V_{rms} \) of 230 V.

Figure 8. Load voltage waveform without load change.

Figure 9. Load current waveform without load change.
From (5) \( L_b = 178 \, \mu H \) and From (6) \( L_f = 754 \, \mu H \).

Buck capacitor \( (C_b) = 220 \, \mu F \).

5. Simulation and experimental results

5.1. Simulation results

Current controlled integrated converter with external ramp compensation is implemented in MATLAB/Simulink. Figure 5 shows the simulink model of converter.
Table 3. The power factor and %THD with respect to universal line voltage range at rated load

| Input voltage | Load    | %THD (Input current) | Power factor (Input current) |
|---------------|---------|----------------------|-----------------------------|
| 90            | Full load | 24                   | 0.9                         |
| 110           |         | 22                   | 0.91                        |
| 120           |         | 20                   | 0.93                        |
| 150           |         | 19                   | 0.94                        |
| 230           |         | 15                   | 0.96                        |

Table 4. The power factor and %THD with load variation at line voltage of 230 V (RMS)

| % Load | %THD (Input current) | Power factor (Input current) | V_o |
|--------|----------------------|-----------------------------|-----|
| 20     | 25                   | 0.92                        | 48  |
| 40     | 22                   | 0.93                        | 48  |
| 60     | 20                   | 0.94                        | 48  |
| 80     | 19                   | 0.95                        | 48  |
| 100    | 15                   | 0.96                        | 48  |

Figure 14. Hardware model of Proposed converter.
5.2 Experimental results

Designed converter performance is verified for universal line voltage range at different load conditions. Figure 6 shows the source voltage and source current waveform for source voltage of 150 V at rated load, it is observed that source voltage and currents are in phase. The calculated power factor is 0.94 and respective line current %THD is 19%.

Converter is supplied with 230 V at rated load the corresponding line voltage & line current waveform is shown in Figure 7. The power factor and line current %THD are 0.96 and 15%.

The Load voltage and load current wave forms are shown in Figures 8 and 9. It is observed that regulated load voltage of 48 V is appeared across the load and load current of 4A.

Load change is done on the converter at 0.2sec from rated load of 200–100 W the converter giving the regulated voltage of 48 V across the load terminals. This shows that converter operating effectively for load changes Figures 10 and 11 shows the respective load current and voltage waveforms of the converter with load change.

Figure 12 shows the bulk capacitor voltage is around 130 V, which is low voltage as compared to two stage and single stage converters. This is the special feature of integrated converter. Figure 13 shows the bulk capacitor voltage after load change at 0.25 s (Tables 3 and 4).

Digital current controlled IBFC with external compensating signal is implemented experimentally by using TMS320F2812 DSP. Hardware setup was implemented in the laboratory as shown in the Figure 14 to investigate the performance of the controller for the integrated buck-flyback converter. The components used in the experimental work are tabulated in Table 5.

The source voltage and current waveforms at supply voltage of 230 V, 50 Hz and 150 V, 50 Hz at rated load are shown in Figures 15 and 16. In Figure 17 i5 is the load current waveform and V5 is the load voltage waveform. Figure 18 shows the bulk capacitor voltage waveform.

| S. No. | Component name               | Symbol | Series number       |
|--------|------------------------------|--------|---------------------|
| 1      | Control switch (Power IGBT)  | SW1    | FGA15N120ANTD       |
| 2      | Power diode                  | Dd     | MUR3060PT           |
| 3      | Power diode                  | Da, Db, Dc | MUR3040PT       |
| 4      | DSP                          | DSP    | TMS320F2812         |

Table 5. Hardware components

![Figure 15. Source voltage and current at supply voltage of 230 V, 50 Hz (200 V/div).](image)
The harmonic content in the input current wave is shown in bar chart of Figure 19. From FFT analysis the %THD of current is 15% at full load condition.

Experimental results of Power Factor for universal Input voltage range at rated load is shown in Table 6.

Simulation and experimental results comparative table is shown in Table 7.
6. Conclusion

Integrated power converter is designed by cascading buck converter with flyback converter because of having feature of current flowing through switch is either buck current or flyback current not sum of both currents, hence switch losses are reduced. Designed converter results are verified for different line and load conditions obtained lower value of power factor is 0.9 at low line voltage and reaches to 0.96 for 230 V, highest percentage of THD is 24% and lowest percentage of THD is 15% and it meets the IEC-6100-3-2 norms for Class-C & Class-D appliances. In the proposed current controller a digital compensating ramp signal is used for slope compensation to reduce sub-harmonics. This scheme applied to the converter and implemented in MATLAB/Simulink tool, their performance was evaluated both in steady state and dynamic conditions. Simulation and experimental results shows that controller acts quickly for load changes as shown in the load current waveform. Experimental results validate the satisfactory with simulation results.

| Table 6. Experimental results for universal input voltage range |
|---------------------------------------------------------------|
| Input voltage (V)    | 120  | 150  | 230  | 250  |
| Power factor        | 0.93 | 0.94 | 0.957| 0.943|

| Table 7. The comparative results |
|----------------------------------|
| Simulation results | Experimental results |
| Input voltage | 230 | 229 |
| Output voltage | 48  | 47.354 |
| %THD           | 15  | 15.47 |
| Power factor   | 0.96| 0.957 |

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