Persistent Kernels for Iterative Memory-bound GPU Applications

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Abstract—Iterative memory-bound solvers commonly occur in HPC codes. Typical GPU implementations have a loop on the host side that invokes the GPU kernel as much as the time/algorithm steps there are. The termination of each kernel implicitly acts as the barrier required after advancing the solution every time step. We propose a scheme for running memory-bound iterative GPU kernels: PERsistent KernelS (PERKS). In this scheme the time loop is moved inside a persistent kernel, and device-wide barriers are used for synchronization. We then reduce the traffic to device memory by caching a subset of the output in each time step in registers and shared memory to be used as input for the following time step. PERKS can be generalized to any iterative solver: they are largely independent of the solver’s implementation. We explain the design principle of PERKS and demonstrate the effectiveness of PERKS for a wide range of iterative 2D/3D stencil benchmarks (geometric mean speedup of 2.29x in small domains and 1.53x in large domains), and a Krylov subspace solver (geometric mean speedup of 4.67x in smaller SpMV datasets from SuiteSparse and 1.39x in larger SpMV datasets, for conjugate gradient).

Index Terms—Persistent gpu kernel, stencil, conjugate gradient

I. INTRODUCTION

GPUs are becoming increasingly prevalent in HPC systems. More than half the systems on the Top500 [1] list include discrete GPUs and seven of the systems in the top ten are GPU-accelerated (November 2021 list). As a result, extensive efforts went into optimizing iterative methods for GPUs, for instance: iterative stencils [2]–[5] used widely in numerical solvers for PDEs, iterative stationary methods for solving systems of linear equations (ex: Jacobi [6], [7], Gauss–Seidel method [7]–[9]), iterative Krylov subspace methods for solving systems of linear equations (ex: conjugate gradient [10], [11], BiCG [11], [12], and GMRES [11], [13]).

Although the device memory bandwidth of GPUs has been increasing from generation to generation, the gap between compute and memory is widening. Given that iterative stencils and implicit solvers typically have low arithmetic intensity [4], significant efforts went into optimizing them for data locality. These included moving the bottleneck from global memory to on-chip scratchpad memory [14], [15], or further pushing the bottleneck to the register files [5], [16]. Those efforts become increasingly effective since the aggregate volume of register files and scratchpad memory capacity are increasing with newer generations of GPUs [17]. In iterative solvers, due to spatial dependencies, a barrier is typically required at the end of each time step (or several time steps when doing temporal blocking [4]). That is to assure that advancing the solution in time step $k$ would only start after all threads finish advancing the solution in time step $k-1$. Invoking the kernels from the host side in each time step acts as an implicit barrier, where the kernel invocation in time step $k$ would happen after all threads of the kernel invocation at time step $k-1$ have finished execution. In-between kernel invocations, data stored in registers and scratchpad memory would be wiped out, and the next kernel invocation would start by reading its input from the device memory. One opportunity to improve the data locality is to extend the lifetime of the kernel across the time steps and take advantage of the large volume of register files and scratchpad memory in reducing traffic to the device memory. In this paper, we propose a generic scheme for running iterative solvers on GPUs to improve data locality. PERsistent KernelS (PERKS) have the time loop inside them, instead of the host, and use recently supported device-wide barriers (in CUDA) for synchronization. Next, we identify the cachable data in the solver: data that is the output of time step $k-1$ and input to time step $k$, as well as the repeatedly loaded constant data. Finally, we use either the scratchpad memory or registers (or both) to cache the data, and reduce the traffic to device memory. PERKS can be an effective technique for not just iterative memory-bound solvers; PERKS can also improve the locality for iterative compute-bound solvers (when storing an iteration’s output cannot be effectively overlapped with compute). That is because compute-bound solvers would benefit from reducing memory traffic in-between the iterations, even if each iteration is running compute-bound code.

While the basic idea of PERKS is seemingly simple, there are several challenges for effectively improving performance with PERKS. First, it is crucial to understand and adapt to the pressure on resources (particularly registers and shared memory) by reducing the occupancy (number of active threads) while maintaining high enough concurrency to saturate the device. Increased pressure on resources from a persistent kernel reduces the number of registers available for caching and, even worse, can lead to performance degradation if register spilling occurs. Second, we need to analyze and pick the ideal scheme to traverse the domain of input array(s) at each step to improve the locality and increase the volume of cached data when in...
transition between time steps. Third, for ideal locality, it is important for PERKS solvers that have more than one array involved (ex: Conjugate Gradient) to have a model of which arrays to cache based on their size and how they are accessed. Finally, identifying PERKS implementation quality and latent bottlenecks necessitates a robust performance model.

It is important to note that PERKS are orthogonal to temporal blocking optimizations. Temporal blocking relies on combining multiple consecutive iterations of the time loop to reduce the memory transactions between them. The dependency along the time dimension is resolved by either: a) redundantly loading and computing cells from adjacent blocks, which limits the effectiveness of temporal blocking to low degrees of temporal blocking [18–20], or b) using tiling methods of complex geometry (e.g., trapezoidal and hexagonal tiling) along the time dimension and restrict the parallelism due to the dependency between neighboring blocks [21–23]. In contrast, the execution scheme of PERKS does not necessitate the resolution of the dependency along the time dimension since PERKS include an explicit barrier after each time step. This means the PERKS model can be generalized to any iterative solver and can be used on top of any version of the solver. In other words, iterative kernels written as PERKS do not compete with optimized versions of those iterative kernels. For instance, a stencil PERKS does not compete with kernels applying aggressive locality optimizations; the performance gain from PERKS is added to the performance gain from whatever stencil optimizations are used in the kernel. As a matter of fact, the more optimized the kernel before it is ported to the PERKS execution scheme, the higher the speedup that would be gained by PERKS. That is since optimizations to the kernel proportionally increases the overhead of data storing and loading in between iterations, which PERKS aim to reduce.

The contributions in this paper are as follows:

- We introduce the design principles of PERKS and provide analysis of the different caching scheme w.r.t. how and where the domain is cached, and how to effectively port iterative solvers to PERKS.
- We implement a wide range of iterative 2D/3D stencil benchmarks and a conjugate gradient solver as PERKS in CUDA. We include an elaborative discussion on the implementation details and performance-limiting factors such as the domains sizes, concurrency, and resource contention.
- Using highly optimized baselines comparable to state-of-the-art 2D/3D stencil implementations, with A100 and V100, our PERKS-based implementation achieves geometric mean speedups of 2.29x and 1.53x in small and large domains, respectively. PERKS-based conjugate gradient achieves a geometric mean speedup of 2.47x in comparison to the highly GPU-optimized production library Ginkgo [11] for SpMV datasets in SuiteSparse. For smaller datasets, the speedup goes up to 4.67x. The source code of all PERKS-based implementations in this paper is available at the following anonymized link: https://tinyurl.com/2p9atawr.

II. BACKGROUND AND MOTIVATION

CUDA’s programming model includes: threads, the basic execution unit (32 threads are executed together as a warp); thread block (TB), which is usually composed of hundreds of threads; grid, which is usually composed of tens of thread blocks.

On-chip memory in a streaming multiprocessor (SMX) includes: shared memory (scratchpad memory), L1 cache, and register file (RF) and. Off-chip memory includes global memory and L2 cache. Data in global memory can reside for the entirety of the program, while data in on-chip memory has the lifetime of a kernel. The shared memory is shared among all threads inside a thread block.

A. Trends of Nvidia GPUs

The trend in Nvidia GPUs is that the register file size and cache capacity, in aggregate, increase. In codes that are bound by memory bandwidth, increasing locality by effectively using the registers and cache to reduce traffic to the device memory is a widely used approach (e.g. fusing kernels [24–28]). The challenge, however, of improving locality is the need to resolve temporal and spatial dependencies.

B. GPU Device-wide Synchronization

Synchronization in GPUs was limited to groups of threads: thread blocks in CUDA (or a work group in OpenCL). Starting from CUDA 9.0, Nvidia introduced cooperative group APIs [31] that include an API for device-wide synchronization. Before introducing grid-level synchronization, the typical way to introduce device-wide synchronization was to launch sequences of kernels in a single CUDA stream. Zhang et al. [32] conducted a comprehensive study to compare the performance of both methods. The result shows that the latency difference between explicit device-wide synchronization versus implicit synchronization (via repetitive launching of kernels) is negligible in most kernels.

C. Iterative algorithms

In iterative algorithms, the output of time step \( k \) is the input of time step \( k + 1 \). Iterative methods can be expressed as:

\[
x^{k+1} = F(x^k)
\]  

(1)

When the domain is mapped out to fine grained GPU cores, there are two points to consider:

- Spatial dependency necessitates synchronization between time steps, or else advancing the solution in the following

2Shared memory is a configurable portion of L1 cache that can be used as a user-managed scratchpad memory.
In time step $k + 1$, each thread or thread block needs input from the output of itself in time step $k$ (i.e., temporal dependency). This gives the opportunity for caching data between steps to reduce device memory traffic.

In the following sections, we briefly introduce iterative stencils and Krylov subspace methods. Throughout the paper, we use them as motivation examples, and we use them to report the effectiveness of our proposed methods, given their importance in the High Performance Computing (HPC) scientific and industrial codes.

### 1) Iterative Stencils: Iterative stencils are widely used in HPC. Take 2D Jacobian 5-point stencil (2Dpt) as an example:

$$
x(i, j)^{k+1} = N \ast x(i, j+1)^k + S \ast x(i, j-1)^k + C \ast x(i, j)^k + W \ast x(i-1, j)^k + E \ast x(i + 1, j)^k
$$

Computation of each point at time step $k + 1$ requires the values of the point itself and its four neighboring points at time step $k$.

Two blocking methods are widely used to optimize iterative stencils for data locality: **Spatial Blocking** [33], [34] and **Temporal Blocking** [4], [55].

In spatial blocking we split the domain into sub-domains, where each thread block can load its sub-domain to the shared memory to improve the data reuse. In the meantime, we require redundant data accesses at the boundary of the thread block to data designated for adjacent thread blocks.

In iterative stencils, each time step depends on the result of the previous time step. One could advance the solution by combining several time steps. The temporal dependency, in this case, is resolved by using a number of halo layers that match the number of combined steps. The amount of data that can be computed depends on the stencil radius ($\text{rad}$) and the number of time steps in-between ($b_t$). In overlapped tiling [36–38], this region can be represented as $2 \times b_t \times \text{rad}$ (halo region). Methods based on this kind of blocking are called overlapped temporal blocking schemes.

### 2) Krylov Subspace Methods: Krylov methods are popular solvers for large sparse (and dense) linear systems of equations [39]. Krylov subspace methods can be described as:

$$\kappa_r(A, b) = \text{span}\{b, Ab, A^2b, \ldots, A^{r-1}b\}$$

Assuming that $A$ is an invertible matrix, it is possible to compute $x = A^{-1}b$ (or solve $Ax = b$) by searching the Krylov subspace without directly computing $A^{-1}$. Searching the Krylov subspace is a sequence of matrix vector multiplications, where at each step the approximation of the solution vector $x$ is updated proportionally to the residual error (vector $r$) from the previous time step.

Conjugate gradient is a main solver in the family of Krylov subspace methods. It is mainly used to solve systems of linear equations for symmetric and positive-definite matrices.

### D. Motivational Example

We use a motivational example of a double precision 2D 9-point Jacobian stencil to motivate implementing iterative solvers as PERKS. Why PERKS: latency across all operations/instructions in newer generation GPUs has been significantly dropping [41]. As a result, often fewer numbers of warps are enough for CUDA runtime to hide the latency effectively and hence maintain high performance at low occupancy [42]. In Fig 1 we vary the number of thread blocks per streaming multiprocessor (TB/SMX) and plot its performance (left Y-axis). For each TB/SMX configuration, we plot on the right Y-axis the unused resources (shared memory and registers). As the figure shows, when TB/SMX decreases, the performance drops (74.6 → 62.0 GCells/s [3]) while the freed shared memory and registers gradually increase. Even at its peak performance, more than 11.2MB of shared memory and register files are not in use. By reducing the TB/SMX to its

3GCells/s denotes giga-cells updated per second.
The prospect of PERKS is to reduce/eliminate this data movement time that dominates the runtime in highly optimized stencil implementations. Finally, while temporal-blocking does also reduce the data movement to some extent, resolving the temporal and spatial dependency adds compute overhead and also reduce the data movement to some extent, resolving the stencil implementation. To summarize, PERKS reduces what amounts to be Amdahl’s law serial portion of the solver, and hence the more optimized a code, i.e., a faster parallel portion, the higher the speedup that would be attributed to PERKS.

**Impact on Optimized Kernels:** It is very important to note that PERKS is orthogonal to the optimization level applied to the compute part of the kernel. As a matter of fact, the more optimized the baseline kernel, the more performance improvement we expect from PERKS. That is since optimizations reduce the time per iteration, i.e., a single kernel invocation, while the time to store/load to global memory in-between iterations remains the same. To summarize, PERKS reduces what amounts to be Amdahl’s law serial portion of the solver, and hence the more optimized a code, i.e., a faster parallel portion, the higher the speedup that would be attributed to PERKS.

**PERKS in Distributed Computing:** PERKS in this paper is demonstrated on a single GPU. In distributed applications that require halo regions (e.g., stencils), PERKS can be used on top of communication/computation overlapping schemes [43], [44]. In overlapping schemes, the boundary points that are computed in a separate kernel would not be cached, while the kernel of the interior points would run as a PERKS and cache the data of the interior points. PERKS could also be used with communication avoiding algorithms (e.g., communication-avoiding Krylov methods [45]).

**Use of Registers:** PERKS uses registers and shared memory for caching data in-between time steps. It should be noted that there are no guarantees that the compiler releases all the registers after the compute portion in each iteration is finished (with Nvidia’s nvcc compiler we did not observe such inefficiency). If such register reuse inefficiency exists, imperfect register reuse by the compiler could result in fewer registers being available for caching and leaves only shared memory to be used for caching. PERKS would not be effective if the target kernel consumes all on-chip resources (both register file and shared memory) even in its minimal occupancy.

**Iterative Solvers as PERKS:** While this paper’s focus is to demonstrate PERKS model for iterative stencils and Krylov subspace methods (conjugate gradient), the discussion in this section (and paper in general) is applicable to a high degree of communication/computation overlapping schemes [43], [44].
A caching policy is required to determine which portion of the domain (or data) to cache. When the entire domain (or data) can fit in register files and shared memory used for caching, the entire algorithm can run from the cache (this is particularly useful in the cases of strong scaling where per node domain size becomes smaller as the number of nodes grows). When only a fraction of the domain can be cached, a policy is required to select the data to prioritize for caching. In the following sections, we elaborate on the caching policy.

1) Considerations for dependency between threads Blocks: Algorithms that do not require dependency between the thread blocks can use the cache space most efficiently because all the load and store transactions to global memory can be eliminated. The dependencies within the thread block are resolved by using either the shared memory or shuffle operations. In iterative solvers, there is often neighbor dependency (ex: a stencil kernel where a cell update relies on values computed in neighboring threads). In such a case, caching the results of the threads at the interior of the CUDA thread blocks eliminates the stores and loads from global memory. The threads at the boundary of thread blocks would, however, continue to store and load from global memory (since the shared memory scope is the thread block). When the capacity of cache is large enough, w.r.t. the domain size to be cached, the performance drawback would be negligible.

2) Identifying which data gets priority to be cached: In many cases, the capacity of register files and shared memory is limited, i.e., it is impossible to cache the entire domain/input. In cases where all the domain/input array elements are accessed at the same frequency, one could assume it is not necessary to use a cache policy that prioritizes specific parts of the domain/input. However, this is not always true.

Take iterative stencil as an example. The data managed by the threads at the boundary of the thread block is stored in main memory to be accessed by the neighboring threads blocks in the following iterations; caching those boundary elements saves one load operation. On the other hand, data at the interior of the thread block is not involved in inter thread block dependency; caching saves one load and one store operation. Finally, data in the halo region is updated at each time step; there is no benefit in caching the layers in the halo region. To conclude, the priority in caching yielding the highest reuse would be: $Data_{no\_inter\_TB\_dependency} > Data_{inter\_TB\_dependency}$, i.e., the priority is to cache the data of the interior threads of the thread block, followed by the data of the threads at the boundary of the thread block, and no caching for the halo region.

For other iterative solvers, such as conjugate gradient, there are different data arrays that could be potentially cached, unlike a single domain array in stencils. The cacheable variables and usage per array element for the conjugate gradient solver are as follows: a) one load and no stores for the matrix $A$, and b) three loads and one store for the residual vector $r$. So by assuming that each operation accesses data in a coalesced access pattern, it would be more effective to cache vector $r$. As a result, the ideal cache priority is $r > A$.

To summarize, while PERKS does not touch on the compute part of the original kernel, attention should be given to identify the ideal caching policy for each solver implemented as PERKS. That being said, one could assume this step can be automated by using a dedicated profile-guided utility (or even sampling from the profiler directly) to aid the user in swiftly identifying an ideal caching policy, based on the access patterns and frequency of access of data arrays in the solver.

IV. Performance Analysis

In this section, we propose a performance model that serves the following purposes. First, we propose a projection of achievable performance that we compare with measured results to detect abnormal behavior or implementation shortcomings. We relied on this projection in the analysis of our PERKS implementation quality (Section IV-B). Second, we identify the bounds on reducing concurrency before dropping performance and use concurrency to explain potential optimizations for further performance improvement (Section IV-D). It is worth mentioning that the concurrency analysis is not a requirement for porting kernels to PERKS; we use the analysis to understand the feasibility of PERKS in practice, and address its implication on performance. In contrast, end-users wishing to port the kernel to PERKS need only to satisfy the concurrency requirements by setting the device occupancy to minimum occupancy while maintaining performance.

A. Overview

This performance model relies on three performance attributes: a) measured performance $M$ of our PERKS implementation, b) the projected peak performance $P$ achievable on a given GPU, and c) the efficiency function $\mathcal{E}(\cdot)$ describing the efficiency of the given kernel running on the device. More specifically, $\mathcal{E}(\cdot)$ is a function of the concurrency exposed by the software $C_{sw}$ and the concurrency required by the hardware $C_{hw}$. The relation of measured performance to projected peak performance becomes:

$$M = P \times \mathcal{E}(C_{sw}, C_{hw})$$ (4)

$^4$Occupancy in CUDA is the ratio of active warps to the maximum number of warps supported on a given device. Occupancy can be controlled, manually or by auto-tuning [46-48] by changing the grid and thread block sizes (subject to constraints of resources).
We discuss projected peak performance in the following section. A detailed discussion of the efficiency and concurrency functions is in Section 4.C.

B. Projecting Peak Achievable Performance

We rely on the FOM (Figure Of Merit) as the performance metric in this analysis. In stencils, we use the giga-cells updated per second (GCells/s) [4], [5]. Given the memory-bound nature of the conjugate gradient solver, we directly use sustained memory bandwidth as a metric, following other works on conjugate gradient [11]. Due to space limitations, this section mainly focuses on stencils to explain the performance analysis. Without loss of generality, the analysis is applicable to other cases (ex: conjugate gradients) by adjusting the performance metric and code concurrency accordingly.

We use a simple performance model inspired by the roofline model [49], [50]. The model’s utility is to project the upper bound on performance based on the reduction of global memory traffic. This model, in turn, helps us in this paper to identify performance gaps in our PERKS implementation and later inspect the reasons for those gaps (e.g., register spilling).

In a kernel implemented as PERKS, the bottleneck could either be the global memory bandwidth or the shared memory bandwidth (if the PERKS caching scheme moves the bottleneck to become the shared memory bandwidth). We don’t assume the registers to be a bottleneck since we assume that as long as we ensure that no register spilling occurs, we avoid register pressure.

We initially do not account for the memory accesses to global memory originating from the boundary threads in each thread block, e.g., halo region in stencil, and confine our analysis to the dependency in cached region. We then expand our analysis to consider those unavoidable global memory accesses (Equation 9).

We assume a total domain of size \( D \) bytes, the cached portion to be \( D_{\text{cache}} \) bytes, and the uncached portion to be \( D_{\text{uncache}} = D - D_{\text{cache}} \) bytes. The cached portion of the domain data would be divided between registers and shared memory (since we cache in both registers and shared memory):

\[
D_{\text{cache}} = D_{\text{gm}} + D_{\text{sm}}.
\]

For \( N \) time steps, assuming the number of bytes stored to global memory in each time step is \( S_{gm} \) and the number of bytes loaded is \( L_{gm} \), the total global memory bytes accessed \( A_{gm} \) becomes:

\[
A_{gm}(D) = N \cdot (L_{gm} + S_{gm}) = 2 \cdot N \cdot D_{\text{uncache}} + 2 \cdot D_{\text{cache}} \tag{5}
\]

In the case when the kernel is bounded by global memory bandwidth, i.e., the volume of cached data does not move the bottleneck from global memory to shared memory, for the global memory bandwidth \( B_{gm} \) and data type size of \( \mathcal{S}(\text{type}) \), the time \( T_{gm}(D) \) for accessing the global memory becomes:

\[
T_{gm}(D) = A_{gm}(D) / B_{gm} \tag{6}
\]

In the case when the kernel is bounded by shared memory bandwidth, i.e., the volume of data cached in shared memory moves the bottleneck to be the shared memory bandwidth, the total shared memory (in bytes) accessed \( A_{sm} \) becomes:

\[
A_{sm}(D_{\text{sm}}) = N \cdot (L_{sm} + S_{sm}) = 2 \cdot (N - 1) \cdot D_{\text{sm}} \tag{7}
\]

Assuming \( A_{sm}(\text{KERNEL}) \) to be the shared memory originally used by the kernel, e.g., shared memory used in the baseline implementation of a stencil kernel to improve the locality, and \( B_{sm} \) to be the shared memory bandwidth, the time \( T_{sm}(D) \) for accessing the shared memory becomes:

\[
T_{sm}(D_{\text{sm}}) = \left( A_{sm}(D_{\text{sm}}) + A_{sm}(\text{KERNEL}) \right) / B_{sm} \tag{8}
\]

Next, we consider the unavoidable global memory accesses necessary to resolve the neighborhood dependencies in \( D_{\text{cache}} \), e.g., the halo region of stencils. In the cached portion of the domain, the halo region requires global memory accesses to resolve the dependencies. Assuming the global memory accesses, in bytes, for the halo region of the data computed by the boundary threads in thread blocks that are in the cached portion of the domain to be \( A_{gm}(\mathcal{S}(D_{\text{cache}})) \), the time for accessing those halo region \( T_{gm}(\mathcal{S}(D_{\text{cache}})) \) would be:

\[
T_{gm}(\mathcal{S}(D_{\text{cache}})) = A(\mathcal{S}(D_{\text{cache}})) \cdot \mathcal{S}(\text{type}) / B_{gm} \tag{9}
\]

The projected best-case total time required for the PERKS kernel may be written as:

\[
T_{\text{PERKS}} = \max(T_{gm}(D) + T_{gm}(\mathcal{S}(D_{\text{cache}})), T_{sm}) \tag{10}
\]

Accordingly, the projected peak performance \( P \) in Equation 4 for the \( N \) time steps can be expressed as:

\[
P = D \cdot N / T_{\text{PERKS}} \tag{11}
\]

To further illustrate how this performance analysis works, we give two examples while computing \( N = 1000 \) time-steps of a single precision 2D 5-point Jacobi stencil on A100.

We use the domain size \( D = 3072^2 \) as an example of a large domain size; the total cache-able region is \( D_{\text{cache}} = 3072 - 2448 \) leading to \( T_{gm}(D) \) of 9900.70 us. The total number of bytes for the halo accesses is \( A(\mathcal{S}(D_{\text{cache}})) = 1000 \cdot 2 \cdot 216 \cdot (136 \cdot 2 + 256 \cdot 2) \). Thus \( T_{gm}(\mathcal{S}(D_{\text{cache}})) = 871.22 \) us. So \( P_{\text{PERKS}} = 3072^2 \cdot 1000 / T_{\text{PERKS}} = 876.09 \) GCells/s, the measured performance is 444.19 GCells/s (50.70% of \( P \); in the following sections we elaborate on the analysis of concurrency and its impact on the gap between measured and projected peak).

We use the domain size \( D = 3072 \cdot 2448 \) as an example of small domain/ size, i.e., when the whole domain can be cached. In our baseline implementation used \( A_{sm}(\text{KERNEL}) = D \cdot 1000 \cdot 4 \) bytes of shared memory. The shared memory cached portion is \( D_{\text{cache}} = 3072 \cdot 1152, \) so \( A_{sm}(D_{\text{cache}}) = 3072 \cdot 1152 \cdot (999) \cdot 2. \) We get \( T_{sm} = 7.6 \) ms and \( P = D \cdot 1000 / T_{\text{PERKS}} = 986.38 \) GCells/s, the measured performance is 609.30 GCells/s (61.77% of \( P \)).
C. Concurrency and Micro-benchmarks

Reducing device occupancy increases the availability of resources to be used for caching in PERKS (as illustrated earlier in Figure 1). On the contrary, reducing occupancy can lead to lower device utilization. To effectively implement PERKS, one has to reduce the occupancy as much as possible without sacrifying performance. Inspired by the findings of Volkov [42], we assume that the efficiency function \( \varepsilon \) reaches its peak point when the code provides enough concurrency to saturate the device (irrespective of the occupancy):

\[
\varepsilon(C_{sw}, C_{hw}) = 100\% \text{, if } \forall C_{sw} \geq C_{hw}
\]

Where \( C_{sw}(\Omega \mathcal{P}) \) is the minimum number of concurrently executable instructions of the operation \( \Omega \mathcal{P} \) exposed by the launched kernel, and \( C_{hw}(\Omega \mathcal{P}) \) is the maximum numbers of instructions of the operation \( \Omega \mathcal{P} \) that the device is capable of handling concurrently. Because this paper mainly focuses on memory bound applications, the \( \Omega \mathcal{P} \) referred to in this paper are limited to data access operations, i.e., global memory load/store \( C(GM) \), shared memory load/store \( C(SM) \), and L2 cache load/store \( C(L2) \).

1) Measuring \( C_{sw}^{SMX} \), \( C_{hw}^{SMX}(\Omega \mathcal{P}) \), the kernel concurrency at the streaming multi-processor (SMX) level, can be computed based on the concurrency exposed by the threads of a thread block \( C_{TB}^{TB}(\Omega \mathcal{P}) \) and number of concurrently running thread blocks per stream multiprocessor \( TB/SMX \):

\[
C_{sw}^{SMX}(\Omega \mathcal{P}) = C_{TB}^{TB}(\Omega \mathcal{P}) \cdot TB/SMX.
\]

2) Measuring \( C_{hw} \). According to Little’s Law [51], the hardware concurrency \( C_{hw} \) can be determined by the throughput \( THR \) and latency \( L \) [42]:

\[
C_{hw}(\Omega \mathcal{P}) = THR(\Omega \mathcal{P}) \cdot L(\Omega \mathcal{P})
\]

The throughput \( THR \) for different data access operations are available in Nvidia online documents [52], [53]. We measure the latency \( L \) with commonly used microbenchmarks [54]–[56] (The latency measurements are collected in the AD/AE appendix).

D. Concurrency Analysis

In this section, we briefly describe how we analyze the concurrency to reduce the occupancy of the original kernel in order to release resources for caching while sustaining performance. We conduct a static analysis to extract the data movement operations in the kernel. Note that we account for any barriers in the original kernels that could impact the concurrency of operations, i.e., we do not combine operators/instructions from before and after the barrier when we count the operators. Finally, we apply a simple model to identify the least occupancy we could drop to before the concurrency starts to drop. For example, we did a static analysis of a single precision 2D 5-point Jacobi stencil kernel to conduct a concurrency analysis. It is worth mentioning that the baseline kernel we use is fairly complex since it is highly optimized by using shared memory to reduce traffic to global memory to its minimum [15].

Table II: Concurrency analysis of global memory accesses of a single precision 2D-5point Jacobi stencil kernel running on A100 (1000 time-steps on 3072² domain)

| TB/SMX | Used Reg. /SMX | Unused Reg. /SMX | GM Load op/SMX | GM Store op/SMX | Measured GCells/s |
|--------|----------------|-----------------|----------------|----------------|------------------|
| 1      | 32KB           | 224KB           | 20640          | 2048           | 94.75            |
| 2      | 64KB           | 192KB           | 2580           | 4096           | 133.24           |
| 8      | 256KB          | 0KB             | 20640          | 16384          | 138.29           |

in Table II show that for this kernel, we could reduce the original occupancy to \( 1/4^{th} \) while maintaining performance.

To understand the gap between the projected upper-bound on achievable performance and the measured performance (94.75/138.29 = 68.52%), we inspect the efficiency function \( \varepsilon() \). The number of concurrent global memory accesses and shared memory accesses in the 2D 5-point Jacobi stencil kernel are enough to saturate A100 when TB/SMX=1. Accordingly, we get \( \varepsilon(C_{sw}=2d5pt.TB/SMX\geq1, C_{hw}=A100) = 1 \), which would indicate that the observed gap in performance is not due to a drop in concurrency we did not model. While this confirms the effectiveness of the concurrency analysis (i.e., since the concurrency analysis resonates with the empirical measurements in Table II), it does not uncover the gap between measured and projected peak achievable. Further investigative profiling revealed that the concurrency for accesses in L2 cache, not global memory, is impacted by reducing occupancy on A100 in specific to the level that affects performance notably. More particularly, access to global memory for the halo region garners a high L2 cache hit rate. This effectively means that higher concurrency is necessary to saturate the L2 cache when hit rates are high. To confirm, we manually doubled the concurrency \( C_{TB}^{TB} \); the performance increased to 123.94 GCells/s with TB/SMX=1 (from 68.52% up to 89.6%).

E. Register pressure in PERKS

One concern with PERKS is that kernels might run into register pressure if the compiler is not optimally reusing registers for different time steps, potentially affecting concurrency and penalizing performance. To illustrate this issue, a high register-pressure 2D 25-point double precision Jacobi stencil uses 78 registers per thread, yet the PERKS version uses 112 registers.

Similar behavior is also observed in other stencil benchmarks. Reducing the occupancy while maintaining the concurrency —as mentioned in the previous section— reduces the impact of this compiler inefficiency in register reuse in all the benchmarks we report in the results section. In the above example, at worst, 48 registers among the maximum available 178 registers per thread could not be used for caching data; it neither harms concurrency nor triggers register spilling.

V. IMPLEMENTATION

This section elaborates on how we implemented memory-bound iterative methods (namely 2D/3D stencils and a conjugate gradient solver) as PERKS.

[5] We gathered the number of registers used by finding the maximum number of registers available as cache before spilling with “launch_bounds=” instruction. Register spilled can be indicated by “-Xptxas="-v -dlcm=cg"” flag.
PERKS highly relies on cooperative groups related APIs (supported since CUDA 9.0 [31]). Currently, the API does not allow over-subscription, i.e., one needs to explicitly assign workload to blocks and threads to expose enough parallelism to the device. However, it is worth mentioning that this API does not limit the flexibility, as different kernels can still run concurrently in a single GPU, as long as they as a whole doesn’t exceed the hardware limitation.

B. Transforming Stencil Kernels to PERKS

Our 3D stencil implementation uses the standard shared memory implementation where 2D planes (1D planes in 2D stencils) are loaded one after the other in shared memory, and each thread computes the cells in a vertical direction [3], [57]. In our PERKS implementation, before the compute starts, planes that already have the data cached from the previous time step do not load from global memory. We do not interfere with compute; only after the compute is finished that we store the results in the registers/shared memory. As Figure 4 shows, after adjusting to handle the input and output of the computation part of the kernel, transforming the existing kernel to PERKS is straightforward. To ensure coalesced memory accesses in the halo region, we transpose the vertical edges of the halo region in global memory. Finally, if the original kernel uses shared memory [6], [57] or registers [5] to optimize stencils, we use the version of the output residing in shared memory or registers at the end of each time step as an already cached output. This way, we avoid an unnecessary copy to shared memory and registers we would be using as cache.

C. Transforming the Conjugate Gradient Solver to PERKS

For its simplicity and accessibility, we use the Conjugate Gradient (CG) solver implementation that is part of CUDA SDK samples (conjugateGradientMultiBlockCG [58]). Since the SpMV implementation in the CG sample is relatively naive, we use the highly optimized merge-based SpMV [59] that is part of the C++ CUB library in CUDA Toolkit [60], since it fits naturally with the caching scheme in PERKS. We do not discuss the details of merge-based SpMV due to the space limit. The reader can refer to details in [59].

We made several slight modifications to the merge-based SpMV implementation. First, merge-based SpMV is composed of two steps: search and compute. The search step is done twice. We first find the workload for each thread block, and then find the workload for each thread inside a thread block. We save the search result of thread block workloads in global memory since the matrix is static throughout the entire iteration. The second search (thread-level) is conducted in shared memory. Those two steps repeatedly generate intermediate data. Two alternative cache policies here would be caching the TB-level search result and caching the thread-level search result. We implemented the two policies and merged them with the other two direct caching policies when conducting the conjugate gradient solver evaluations.

Second, merge-based SpMV originally uses small thread blocks, i.e., 64 threads per TB. This introduces a high volume of concurrently running thread blocks per streaming multiprocessor. We increase the TB size to 128 and slightly change the memory access order to accommodate the larger TB size.

D. New Features in Nvidia Ampere

The Nvidia Ampere generation of GPUs introduced two new features that have the potential to improve the performance of PERKS. Namely, asynchronous copy for shared memory and L2 cache residency control [29]. When testing asynchronous copy to cache in PERKS, we did not observe noticeable performance difference. For L2 cache residency control, we experimented with setting the input and halo region to be persistent. We observed 8% slowdown and no change in performance, respectively. Accordingly, we do not use those new features in our PERKS implementations.

E. Transforming Kernels to PERKS: an end-user perspective

This section briefly discusses how an end-user could approach transforming kernels to PERKS.

1) Identify minimal concurrency of a kernel: An end-user only needs to reduce the device occupancy to minimum (while maintaining performance) via manual tuning of the kernel launch parameters or using auto-tuning tools [46–48].
TABLE III: Stencil benchmarks. A detailed description of the stencil benchmarks can be found in [15], [35].

| Benchmark (Stencil Order, FLOPs/Cell) | single precision | double precision |
|----------------------------------------|-----------------|-----------------|
| 3d5pt(1,10)                            | 256             | 2304            |
| 2ds9pt(2,18)                           | 256             | 2304            |
| 2d13pt(3,26)                           | 256             | 2304            |
| 2d17pt(4,34)                           | 256             | 2304            |
| 2d21pt(5,42)                           | 256             | 2304            |
| 2d25pt(6,59)                           | 256             | 2304            |
| 2d29pt(7,76)                           | 256             | 2304            |
| 3d7pt(1,14)                            | 256             | 2304            |
| 3d13pt(2,26)                           | 256             | 2304            |
| 3d17pt(3,34)                           | 256             | 2304            |
| 3d21pt(4,42)                           | 256             | 2304            |
| 3d25pt(5,50)                           | 256             | 2304            |
| 3d29pt(6,68)                           | 256             | 2304            |
| poisson[138]                           | —               | —               |

TABLE IV: Minimum domain sizes that would saturate the stencil benchmarks can be found in [16], [35].

VI. EVALUATION

A. Hardware and Software Setup

The experimental results presented here are evaluated on the two latest generations of Nvidia GPUs: Volta V100 and Ampere A100 with CUDA 11.5 and driver version 495.29.05.

B. Benchmarks and Datasets

1) Stencil Benchmarks: To evaluate the performance of PERKS-based stencils, we conducted a wide set of experiments on various 2D/3D stencil benchmarks (listed in Table III). The baseline implementation uses state-of-the-art optimizations such as shared memory and heavy unrolling (to counter the reduction in over-subscription). We report the performance (CGells/s) of the baseline implementation for all benchmarks in Figures 5 and Figure 6. The baseline performance is on-par to (and often exceeds) state-of-the-art GPU-optimized stencil codes reporting the highest performance across different stencil benchmarks. Namely, SSAM [5], register-optimized stencils [62], [63], StencilGen [40], and temporal blocking AN5D [4].

We use the test data provided by StencilGen [40]. We tested three PERKS implementations: PERKS (sm) that only uses shared memory to cache data; PERKS (reg) that only uses register to cache data; and PERKS (mix) that uses both shared memory and registers to cache data. Due to space limitations, we report only the peak performance among these three PERKS variants.

2) Conjugate Gradient Datasets: the conjugate gradient solver datasets come from the SuiteSparse Matrix Collection [61]. We selected symmetric positive definite matrices that can converge in a CG solver. The details of the selected datasets are listed in Table VI.

We compare the performance of the PERKS CG solver to Ginkgo [11], a widely used library heavily optimized for GPUs (including A100). We run 10,000 time-steps in our performance evaluation (Similar to Ginkgo’s basic setting [11]). We report the speedup per time step, and the measured sustained bandwidth achieved by Ginkgo.

For PERKS, we ran different variants that implement: a) the two caching policies discussed in Section II-B (i.e., caching the vectors or the matrix) and, b) the additional caching TB-level search result and thread-level search result policies mentioned in Section V.C. We only report the top performing variant for each dataset due to space limitations.

For all iterative stencils and conjugate gradient experiments, we run each single evaluation five times, and report the run with the highest performance.

C. Sizes of Domains and Problems

PERKS intuitively favors small domain/problem sizes. However, for a fair evaluation of PERKS, we can not choose arbitrarily small domain sizes; we need domain/input sizes that fully utilize the compute capability of the device. We conducted an elaborate set of experiments for every individual stencil benchmark to identify the minimum domain size that would fully utilize the device. Note that domain/problem sizes that are beyond domain/problem sizes that could fully utilize the device are effectively serialized by the device once we go beyond peak concurrency sustainable by the device. Table VI summarizes the domain sizes for stencil benchmark that would provide a base for a fair comparison.

For the conjugate gradient experiments, we include datasets from SuiteSpare that cover a wide range of problem sizes: from strong-scaling small dataset sizes that would fit in L2 cache and up to large dataset sizes typically reported by libraries for a single GPU of the same generations we use (Ginkgo [11], [64] and MAGMA [65]).

D. Iterative 2D/3D Stencils

Figure 5 shows the PERKS speedups for large domain sizes listed in Table VI. The geometric mean speedup for 2D stencils is 1.58x in A100 and 2.01x in V100. The geometric mean speedup for 3D stencils is 1.10x for A100 and 1.29x for V100.

It is important to note three points: a) the benchmarks we use include both low-order and high-order stencils, b) the speedups are particularly higher on low-order stencils that...
TABLE V: Datasets for CG solver (from SuiteSparse [61])

| Code | Name (61) | Rows | NNZ  |
|------|-----------|------|------|
| D1   | Trefethen | 2,001| 41,906|
| D2   | mcs01440  | 1,440| 46,270|
| D3   | fv1       | 9,604| 85,264|
| D4   | msc04515  | 4,515| 97,707|
| D5   | Mmu       | 7,102| 170,134|
| D6   | crsn02    | 13,965| 322,905|
| D7   | shallow_water2 | 81,920| 327,680|

are more commonly used in practice (ex: average of 26% reduction in runtime for up to 2-order 3D stencils on V100 and A100, in double precision), and c) the speedups we report are not limited to the –very optimized– implementation we use as baseline; other stencil implementations, regardless of their internals, can also benefit from being transformed to PERKS.

Since small domains occur in strong scaling, we also report in Figure 6 results for small domains that could be fully cached. PERKS for small domain 2D stencils are 2.48x faster on A100 and 3.15x faster on V100. PERKS for small domain 3D stencils are 1.45x faster on A100 and 1.94x faster on V100.

E. Conjugate Gradient With Merge-based SpMV

Figure 7 compares PERKS to Ginkgo. When the input is less than the L2 capacity, PERKS running on A100 achieve a geometric mean of 4.55x and 4.87x speedups for single and double precision, respectively; on V100, PERKS achieve 4.32x and 5.05x speedups. When the input matrix exceeds the L2 cache capacity, PERKS running on A100 achieve a geometric mean of 1.30x speedup for single precision and 1.15x speedup for double precision. On V100, PERKS achieve a geometric mean of 1.44x (single) and 1.59x (double) speedups. It is important to remember that the Ginkgo library we use as baseline is among the top performing libraries in CG solvers, emphasizing GPU optimizations [11]. Note that regardless of whether we stay within the L2 cache capacity or exceed it, we are still caching the domain using one of the caching policies we described earlier. Yet upon analyzing results, we observed a clear drop in speedup once we exceed the L2 capacity.
F. Discussion of the Results

We want to emphasize that for large problem sizes, PERKS achieves very high performance. To illustrate it, as can be deduced from Figure 5. By applying PERKS in V100, the geometric mean speedup is 1.70x, which is 97% of what one generation of hardware improvements in A100 provide (1.72x). Similarly, in the conjugate gradient solver with the large datasets D15-D20 (Figure 7), by applying PERKS in V100, the geometric mean speedup is 1.16x, which is even more than the improvements A100 can provide (1.15x). Finally, since the results for small problems are outstanding, we report the results for smaller problem size separately to emphasize the large extent to which PERKS would be beneficial for strong scaling.

G. Caching

1) Where to Cache: Shared Mem., Registers, or Both?: The intuition is that using both shared memory and registers would always be better (more cache-able space). The results (see Figure 8) show that this is usually the case. There can, however, be exceptions. For instance, in our observations, we see that for higher order stencils, using shared memory and registers is often not the ideal choice (presumably due to arising register pressure).

2) What to Cache?: We highlight important observations when varying the data to cache in the conjugate gradient solver (see Figure 7). First, the implicit cache policy (IMP) achieves a geometric mean of 3.61x and 1.19x over Ginkgo for data sets size both within and (surprisingly) when exceeding L2 cache, respectively. This means PERKS can gain speedup before applying any explicit caching policy by getting hits in the L2 cache. Second, the speedup difference between caching the vector (VEC) or not is usually insignificant for most situations. This might be because vectors are generally not large enough to consume all available cache resources. Third, as expected, the general tendency is that the more PERKS caches, the more speedup there is. So we generally get the highest speedup with caching the matrix (MAT) or caching both the vector and matrix (MIX). The exception is in the case of single precision when the dataset sizes exceed L2 cache: we still get speedup from MAT and MIX, though not the highest speedup.

3) What Should the End-user Do?: In summary, the cache policy analysis for conjugate gradient (which is a fairly complex solver) shows that a simple greedy approach of targeting the largest data arrays in as many caching resources as possible gives mostly the best performance. While there can be outliers, the simple greedy policy is, in most cases, effective enough, and also simple for end-users (since they only need to identify the arrays generating the most traffic).

H. Performance Analysis

The roofline-like model we propose suffers from the same limitations of the roofline model, e.g., it has an implicit assumption of perfect overlap of compute and memory accesses.
workload balance. For details, please refer to the merge_spmv paper \[59\].

3. workload: merge_spmv uses a search function to balance workload. We can cache the result of workload balance. For details, please refer to the merge_spmv paper \[59\].

\[ Ax - b = r \]

**POLICY**

| IMP | MIX | MAT | VEC |
|-----|-----|-----|-----|
| A100 (Single) | 5.0 | 3.6 | 2.6 |
| A100 (Double) | 5.0 | 3.6 | 2.6 |
| V100 (Single) | 3.0 | 1.2 | 0.9 |
| V100 (Double) | 3.0 | 1.2 | 0.9 |

1. IMP: Explicit cache [PERKS w/o caching; rely on hits in L2]
2. MIX: Explicitly cache residual vector \( r \)
3. MAT: Explicitly cache matrix \( A \), using remaining resources to cache matrix \( A \)

Additionally, inaccuracies can arise from the L2 concurrency issues we discussed in Section IV-C. The projected peak performance is effective in serving the purposes of identifying unanticipated performance gaps and guiding our occupancy reduction. That being said, it is important to note that projected peak performance showed is taken as an indicator of the bound on performance improvement and not as accurate performance prediction. In large-domain stencils, we observed 64% (36% ~ 85%) of the projected peak. In the small-domain stencils, we observe 59% (34% ~ 97%) of the projected peak.

**VII. RELATED WORK**

The concept of persistent threads and persistent kernels dates back to the introduction of CUDA. The main motivation for persistence at the time was load imbalance issues with the runtime warp scheduler \[66\], \[67\]. Later research focused on using persistent kernels to overcome the kernel invocation overhead (which was high at the time). GPUrDMA \[68\] and GPU-Ether \[69\] expanded on the concept of persistent kernels to reduce the latency of network communication.

As on-chip memory sizes increased, researchers began to capitalize on data reuse in persistent kernels. GPUrDMA \[68\] proposed a matrix-vector product persistent kernel holding a constant matrix in shared memory. Khorasani et al. \[70\] use persistent threads to keep parameters in cache. Zhu et al. \[71\] proposed a sparse persistent implementation of recurrent neural networks.

It is worth mentioning that Kshitij et al. \[72\] a decade ago was the first that summarized the "persistent thread" programming style. Yet, the four scenarios the authors listed to be targeted for persistent threads are mostly out of data. The only scenario that still gives an advantage in the current GPU programming environment is to bypass the hardware scheduler for manual load balance, as a recent study showed \[73\].

To our knowledge, this work is the first to propose a methodological and generic blue print for accelerating memory bound iterative GPU applications using persistent kernels.

**VIII. CONCLUSION**

We propose a persistent kernel execution scheme for iterative GPU applications. We enhance performance by moving the time loop to the kernel and caching the intermediate output of each time step. We show notable performance improvement for iterative 2D/3D stencils and a conjugate gradient solver for both V100 and A100 over highly optimized baselines. We further report notably high speedups in small domain/problem sizes, which is beneficial in strong scaling cases.

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