At-speed DfT Architecture for Bundled-data Design

Ricardo Aquino Guazzelli, Laurent Fesquet
Univ. Grenoble Alpes, CNRS, Grenoble INP*, TIMA, 38000 Grenoble, France *Institute of Engineering Univ. Grenoble Alpes
\{ricardo.guazzelli, laurent.fesquet\}@univ-grenoble-alpes.fr

The main objective to the proposed architecture is to allow verifying whether this timing constraint has been respected after fabrication.

Figure 1 illustrates the proposed testing structure with a push channel structure. Regarding testing, the circuit has multiple testing signals:

- **Test mode** ($T_{mode}$): when enabled, it bypasses the control logic and allows to control register with an external clock signal $T_{clk}$. This signal is usually added for stuck-at testing with scan chains;
- **Scan enable** ($SC_{en}$): when enabled, it bypasses the combinational logic presented in the circuit data paths, allowing to load and unload the scannable registers in the circuit. This signal is also presented for stuck-at testing with scan chains;
- **Handshake breakers** ($HSB_i$): this signal allows to disable or enable the left handshake signals of a given controller. When enabled, this signal disables the left handshake signals and permits external control of the left request signal of the controller through $ext_{req}$. When disabled, the left handshake signals are connected to the previous stage(s) and the controller operates normally;
- **External request signal** ($ext_{req}$): this signal is added specially for the at-speed testing methodology in this work. During at-speed testing, this signal is responsible to internally propagate tokens in control paths;
- **External acknowledge signal** ($ext_{ack}$): signal responsible initialize the left acknowledge signal of a given controller when $HSB_i$ is enabled. This signal only serves to initialize the left acknowledge signal before at-speed testing and may be remove or optimized depending of the handshake protocol.

![Fig. 1. Proposed testing structure. Lower MUX logic controlled by $T_{mode}$ and $SC_{en}$ are already presented for stuck-at testing. The proposed testing structure adds two more MUX gates that allows to disable the left handshake signals of the controller.](image)

![Fig. 2. Behavior of the testing signals during a test cycle.](image)

A. Test Cycle

The test cycle is composed by three main steps: (1) scan in, (2) test run and (3) scan out. Figure 2 illustrates the behavior of the main test signals. During the first step (1), both $T_{mode}$ and $SC_{en}$ signals are enabled. This will put the circuit in test mode and will allow loading the scan chain and configuring each $HSB_i$ signal. Once the scan chain and the HSB shift register are loaded, $T_{mode}$ and $SC_{en}$ signals are disabled, the circuit goes back in normal mode. When $ext_{req}$ is enabled, it launches all controllers in launch mode ($HSB_i$ enabled) and propagates tokens to the remaining controllers set in capture mode ($HSB_i$ disabled) – this is the application step. Finally, the circuit is put in test mode again to scan out the circuit and verify if the capturing registers contain the expected test vectors.