A metal oxide TFT gate driver with a single negative power source employing a boosting module

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ABSTRACT

This paper presents a new gate driver integrated by In-Zn-O thin-film transistors (IZO TFTs) with the etch stop layer (ESL) structure, in which only a single negative power source is used on account of a new boosting module. The boosting module is controlled only by the VIN signal for generating a lower level than VSS. The proposed gate driver with 15 stages is fabricated through the IZO TFT process on a glass substrate to verify its function. The experiment results showed that the proposed gate driver can successfully output full-swing waveforms with resistive load $R_L = 2 \, \text{k}\Omega$ and capacitive load $C_L = 30 \, \text{pF}$ at the 16.7 and 66.7 kHz clock frequencies, and can also output as small as $3.2 \, \mu\text{s}$ pulse width with little distortion, revealing good stability.

1. Introduction

Thin-film transistors (TFTs) are the key to implementing active-matrix flat panel displays (FPDs), such as the active-matrix organic light-emitting diode (AMOLED) or the thin-film transistor liquid crystal display (TFT LCD). Integrating gate driver circuits on glass substrates can eliminate the conventional gate driver integrated circuit (IC), reduce the fabrication cost, and make FPDs thinner and the borders narrower [1–3]. Metal oxide TFTs (MOTFTs) have attracted much attention of late due to their several advantages, such as their good uniformity, high mobility, and low process temperature [4,5]. Unlike a-Si:H or low-temperature polysilicon (LTPS) TFTs, however, MOTFT generally operates in depletion mode, and there will be considerable leakage current when the gate source voltage is zero [6,7]. Therefore, the gate driver integrated by MOTFTs has problems due to its depletion mode.

The double negative power source method is often used in gate drivers to solve the problem of leakage current induction by the depletion mode of MOTFTs [8,9]. The voltage of one source is set to be lower than the other one for completely shutting off the pull-down TFTs of the output module. Various integrated gate drivers with double negative power sources have been reported [10–13]. Double negative power sources, however, will increase the complexity of signal connections with a timing controller, and will result in higher power consumption because of the larger voltage range. The capacitor coupling effect is often used in gate driver circuit design [8–13]. The voltage at the internal key nodes is boosted by the capacitor coupling effect, thereby reducing the leakage current [12,13]. Figure 1(a) shows the conventional gate driver circuit. The pull-up TFT is made much larger to improve the driving ability, resulting in high parasitic capacitance. During the non-working period, it is easy for the voltage of node Q to fluctuate due to the capacitor coupling effect of $C_gd$ at the CLK transition, introducing obvious noise to the output signal. Figure 1(b) shows the newly designed circuit. Node Q will be kept stable at a low level because M5 is kept on during the non-working period. Furthermore, during the working period, the $V_{gs}$ values of M3, M4, and M5 are all lower than 0 V in Figure 1(b) while that of M3 is 0 V in Figure 1(a). Thus, the newly designed circuit can effectively suppress noise to realize a stable output waveform.

This paper proposes a new gate driver integrated by MOTFTs, which employs a single negative power source realized by a simple boosting module. The boosting module can generate power at a level lower than the negative power source, and can maintain such for a sufficient time.

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Figure 1. (a) Conventional gate driver circuit. (b) Newly designed circuit.

Figure 2. Measured transfer characteristic and structure of TFTs.

2. Proposed gate driver operation

Figure 2 shows the measured transfer characteristic of IZO TFTs (W/L = 50 μm/10 μm) with an etch stop layer (ESL) structure, which is employed in the fabrication of the proposed gate driver. The extracted values of the threshold voltage, field effect mobility, and subthreshold swing are \(-0.6\) V, 27.64 cm²/(V·s), and 90 mV/dec, respectively. The structure of the ESL TFT is shown in the inset of Figure 2, and the fabrication is as follows. A 200 nm Mo thin film is deposited onto a glass substrate via DC sputtering, as a gate metal. Then a 250/50-nm thick SiO₂/Si₅Nₓ stacked insulator layer is deposited via plasma-enhanced chemical vapor deposition (PECVD). After that, a 20 nm IZO film is deposited on the insulator via radio frequency (RF) magnetron sputtering, as the active layer. Then, 200 nm SiO₂ is fabricated via PECVD as an ESL at 230°C to protect the active layer. 200 nm Mo is deposited via DC sputtering as the S/D electrode. Finally, 300 nm SiO₂ is formed as a passivation layer to protect the TFT device.

Figure 3 shows the schematic diagram of the proposed gate driver with one stage, its timing diagram, and the block diagram, respectively. One stage of the gate driver, which consists of 12 transistors and two capacitors, can be divided into the input, boosting, reset, and output modules. As shown in Figure 3(a), transistors M4, M5, and M7 make up the input module mainly for the initiation of the gate driver while transistors M1, M2, M3, and C1 constitute the boosting module. The VIN signal is directly connected to C1, which causes node Qb to become a more negative voltage through the capacitor coupling effect, while in [14], the lower voltage generated by the negative voltage generating module cannot hold for a sufficiently long time due to a few leakage current paths. In addition, the reset module includes transistors M6 and M8 while the output module contains transistors M9, M10, M11, M12, and C2. Figure 3(b) shows the timing diagram of each stage. The clock frequencies of CLK1, CLK2, and CLK3 are the same, and their duty ratios are all 16.7%. The operation of the gate driver includes the four periods below.

1. Initialization period. The input signals VIN and CLK1 turn to high at the same time; thus, node Qb is discharged to low through transistors M1 and M3. As a result, transistor M8 is turned off, and node Q is charged to high through transistors M4 and M5.

2. Holding period. CLK2 and CLK3 remain low when the input signals VIN and CLK1 switch to low, and node Qb will be pulled down to a voltage level lower than VSS due to the capacitor coupling effect of C1. Simultaneously, the gate voltage of M3 drops to a level lower than VSS according to the coupling effect of the parasitic capacitor of M2. Obviously, M2 is used to reduce the leakage current of node Qb. Thus, transistors M10 and M12 are completely turned off. Node Q holds a high voltage during this stage.

3. Output period. The clock signal CLK2 switches to high, and the output nodes COUT and OUT are charged to high through transistors M9 and M11, respectively. Note that node Q will be boosted to a level higher than VDD due to the capacitor coupling effect of C2. As a result, nodes COUT and OUT will be charged to high more quickly.

4. Reset period. The clock signal CLK2 switches to low, and the output nodes COUT and OUT are pulled down to low. After that, the clock signal CLK3 turns to high, so node Qb is charged to high by transistor M6. Consequently, node Q is discharged to low through transistor M8 turned on by node Qb.

Figure 3(c) shows the connections among multiple stages of the gate driver employing the bi-side driving
It is shown that the gate driver alternately outputs pulse waveforms in the even and odd sides.

Figure 4 shows the simulated waveforms of Qb under different values of C1. It is shown that the voltages of node Qb are all lower than VSS (−6 V) during the output period. When the VIN signal changes from a high to a low level, node Qb becomes a floating point because transistors M1 and M3 are turned off. At the same time, the voltage of node Qb becomes lower than VSS due to the capacitor coupling effect of C1. The voltage of node Qb decreases with the increase of the value of C1. The value of C1 not only impacts the voltage value of node Qb during holding period ② but also affects the value of the voltage variation caused by the overlap capacitors in M10 and M12 during output period ③. It is noted that the value of C1 has little effect on the power consumption of the whole circuit because the working period (①, ②, ③, and ④) occupies only a small proportion of one frame time. Considering the tradeoff between the circuit area and the performance, capacitor C1 with 4 pF may
be suitable for the proposed gate driver. Note that the main leakage path of Qb is M6 when Qb is boosted down during the holding and output periods. Figure 5 presents the simulated waveforms of Qb with different values of the threshold voltage for M6. The voltage of Qb may get closer to VSS when the threshold voltage shifts to the negative direction. The voltage of Qb, however, has less time to leak with the increase in clock frequency. Then it may remain lower than VSS at the negative threshold voltage condition. Figure 6 shows the simulated waveforms of OUT and the node between RL and CL. It is observed that the waveform of the node between RL and CL is nearly the same as that of OUT because the time constant \( \tau = RL^*CL \) is quite small. Figure 7 shows the simulated waveforms of OUT and the nodes between RL and CL for the 1st, 3rd, 5th, and 18th stages of the proposed gate driver. The simulation results showed that the proposed gate driver could work well with a single negative power source.

3. Results and discussion

The proposed gate driver with 15 stages is fabricated through the IZO TFT process employing an ESL structure. Table 1 shows the design parameters of the proposed gate driver. Note that the pull-up TFT M11 is made much larger than others to improve the driving ability. Figure 8 shows the micrograph of the proposed scan driver. The area of a single stage, including the signal wires, is 1040 \( \times \) 330 \( \mu \)m.

Figure 9 shows the measured output waveforms of the 1st and 15th stages with resistive load \( R_L = 2 \) k\( \Omega \) and capacitive load \( C_L = 30 \) pF at a 16.7 kHz clock frequency. The measured pulse width was 10.7 \( \mu \)s. The 1st stage is denoted by the green line with a \(-6.4-9.8\) V voltage swing whereas the 15th stage is denoted by the yellow line with a \(-6.3-9.6\) V voltage swing. It is shown that the proposed gate driver can achieve a full swing output. Good noise suppression characteristics with little distortion from the output waveforms of the 1st and 15th stages were observed. As a result, the proposed gate driver can realize a normal function although employing a single negative power source.

Figure 10 shows the output waveforms of the 1st and 15th stages with the same load values as in Figure 9 at a 66.7 kHz clock frequency. The measured pulse width was 3.2 \( \mu \)s. It was found that the swing of the output voltage...
Figure 6. Simulated waveforms of OUT and the node between RL and CL.

Figure 7. Simulated waveforms of the proposed gate driver’s 1st, 3rd, 5th, and 18th stages.

Table 1. Design Parameters of the Proposed Scan Driver.

| Parameter          | Value      |
|--------------------|------------|
| CLK1, CLK2 (V)     | −6 ~ 10    |
| VSS (V)            | −6         |
| Circuit area       | 1040 × 330 μm |
| M1, M3 (μm/μm)     | 40/10      |
| M4, M5, M9, M12 (μm/μm) | 240/10 |

is still close to the power source range. Furthermore, the output waveforms at a higher frequency are as good as those at a low frequency. This means that the proposed gate driver may be suitable for application in high-resolution displays. Take UHD (3840(RGB)*2160) for example; it takes only about 3.8 μs to drive each row line at a 120 Hz frame rate.

4. Conclusions

This paper presents a new gate driver integrated by metal oxide TFTs employing a single negative power source. Thereinto, a new boosting module is designed to generate a lower voltage level than the negative power source. Fifteen stages of the proposed gate driver are fabricated through the IZO TFT process with an etch stop layer (ESL) structure. It was shown that the proposed gate driver can generate full swing output waveforms at the
16.7 and 66.7 kHz clock frequencies, and that it can work well even though the output pulse width is as small as 3.2 μs. There is little distortion comparing the output waveform of the 1st stage with that of the 15th stage, revealing the good stability of the proposed gate driver.

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