CAn’t Touch This: Practical and Generic Software-only Defenses Against Rowhammer Attacks

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Abstract—Rowhammer is a hardware bug that can be exploited to implement privilege escalation and remote code execution attacks. Previous proposals on rowhammer mitigation either require hardware changes or follow heuristic-based approaches (based on CPU performance counters). To date, there exists no instant protection against rowhammer attacks on legacy systems.

In this paper, we present the design and implementation of two practical and efficient software-only defenses against rowhammer attacks. Our defenses prevent the attacker from leveraging rowhammer to corrupt physically co-located data in memory that is owned by a different system entity. Our first defense, B-CATT, extends the system bootloader to disable vulnerable memory pages. Kim et al. [12] were the first defense, B-CATT, extends the system bootloader to disable vulnerable memory pages. Kim et al. [12] were

Rowhammer Attack Diversity. Although it might seem that single bit flips are not per-se dangerous, recent attacks demonstrate that rowhammer can be used to undermine access control policies and manipulate data in various ways. In particular, it allows for tampering with the isolation between user and kernel mode [21]. For this, a malicious user-mode application locates vulnerable memory cells and forces the operating system to fill the physical memory with page-table entries (PTEs), i.e., entries that define access policies to memory pages. Manipulating one PTE by means of a bit flip allows the malicious application to alter memory access policies, building a custom page table hierarchy, and finally assigning kernel permissions to a user-mode memory page. Rowhammer attacks have made use of specific CPU instructions to force DRAM access and avoid cache effects. However, prohibiting applications from executing these instructions, as suggested in [21], is ineffective because recent rowhammer attacks do no longer depend on special instructions [3]. As such, rowhammer has become a versatile attack technique allowing compromise of co-located virtual machines [19] [27], and enabling sophisticated control-flow hijacking attacks [5, 20, 23] without requiring memory corruption bugs [4, 7, 21]. Lastly, a recent attack, called Drammer [24], demonstrates that rowhammer is not limited to x86-based systems but also applies to mobile devices running ARM processors.

Rowhammer Mitigation. The common belief is that the rowhammer fault cannot be fixed by means of any software update, but requires production and deployment of redesigned DRAM modules. Hence, existing legacy systems will remain vulnerable for many years, if not forever. An initial defense approach performed through a BIOS update was unsuccessful as it only slightly increased the difficulty to conduct the attack [21]. The only other software-based mitigation of rowhammer, we are aware of, is a heuristic-based approach that relies on hardware performance counters [3]. However, it induces a worst-case overhead of 8% and suffers from false positives which impedes its deployment in practice.

Goals and Contributions. The goal of this paper is to develop the first practical and generic software-based defenses against rowhammer attacks that can instantly protect existing vulnerable legacy systems without suffering from any performance overhead and false positives. Intuitively, a defense against rowhammer needs to prevent the dangerous bit flips by disabling vulnerable memory pages. Kim et al. [12] were first discussing this idea, however, they conclude that this
mitigation will generate very high overhead and significantly reduce the amount of available memory. To validate this defense approach, we developed our first mitigation scheme, called B-CATT\footnote{The name B-CATT is composed of two parts: B refers to our Bootloader based solution, CATT abbreviates CAN’t Touch This.} that systematically scans the memory to identify and blacklist vulnerable memory pages. We implemented B-CATT as a bootloader extension to support and protect a wide range of operating systems. In contrast, to the conclusion drawn in \cite{12}, we show that B-CATT is highly efficient and prevents all existing rowhammer attacks. On the other hand, it is not yet known whether memory vulnerable to bit flips changes over time or under different experiment conditions (e.g., temperature, methodology to identify bit flips). This motivated us to develop a second and more generic mitigation scheme, called G-CATT\footnote{G-CATT is short for Generic CATT.} that does not aim to prevent bit flips but rather remove the dangerous effects (i.e., exploitation) of bit flips. This is achieved by limiting bit flips to memory pages that are already in the address space of the malicious application, i.e., memory pages that are per-se untrusted. For this, we extend the operating system kernel to enforce a strong physical isolation of different system entities, e.g., user and kernel space.

To summarize, our main contributions are:

- We present practical software-based defenses against rowhammer. In contrast to existing solutions, our defenses require no hardware changes \cite{12}, do not deploy unreliable heuristics \cite{3}, and still allow legacy applications to execute instructions that are believed to alleviate rowhammer attacks \cite{21}.
- We systematically revisit the practicality and effectiveness of an intuitive mitigation approach that proposes marking memory, vulnerable to rowhammer, unavailable to the system. We also developed a prototype, B-CATT, which implements this approach for the first time.
- We propose a generic enforcement mechanism for operating system kernels, G-CATT, to mitigate rowhammer attacks. Our design ensures that the attacker can only flip bits in memory that is already under her control.
- We present two prototype implementations, one for the Linux kernel version 4.6 and one for the GRUB bootloader, and demonstrate their effectiveness in mitigating all previously presented rowhammer attacks \cite{7, 21}.
- We successfully applied our Linux kernel patch for G-CATT to the Android version 4.4 for Google’s Nexus devices. This allows us to also mitigate Drammer \cite{23}, a recent rowhammer-based privilege escalation exploit on ARM.
- We extensively evaluate the performance, robustness and security of our defense approaches against rowhammer attacks to demonstrate the effectiveness and high practicality of both B-CATT and G-CATT. In particular, our performance measurements indicate no computational overhead for common user and kernel benchmarks.

Note that recent research demonstrates a variety of exploitation strategies that rely on rowhammer \cite{4, 19, 27}. While these attacks show the versatility of rowhammer, they are not always practical. For example, attacking the browser with rowhammer can take up to 45 minutes \cite{41}, and attacking a virtual machine may require a couple of days of preparation time \cite{19}. Hence, our proof-of-concept implementation of G-CATT aims to mitigate practical rowhammer attacks that escalate the privileges to the superuser root by manipulating the kernel page tables \cite{21, 24}. We discuss further deployment cases in Section \ref{sec:deployment}.

II. BACKGROUND

In this section we provide the basic background knowledge necessary for understanding the remainder of this paper.

A. Dynamic Random Access Memory (DRAM)

A DRAM module, as shown in Figure 1, is structured hierarchically. The hardware module is called Dual Inline Memory Module (DIMM), which is physically connected through a channel to the memory controller. Modern desktop systems usually feature two channels facilitating parallel accesses to memory. The DIMM can be divided into one or two ranks corresponding to its front- and backside. Each rank contains multiple banks which are the chips that contain the memory cells. Each bank is organized in columns and rows, as shown in Figure 2.

An individual memory cell consists of a capacitor and a transistor. To store a bit in a memory cell, the capacitor is electrically charged. By reading a bit from a memory cell, the cell is discharged, i.e., read operations are destructive. To prevent information loss, read operations also trigger a process that writes the bit back to the cell. A read operation always reads out the bits from a whole row, and the result is first saved in the row buffer before it is then transferred to the memory controller. The row buffer is also used to write back the content into the row of memory cells to restore their content.

It is noteworthy to mention that there exists a non-linear mapping between physical memory address and the rank-bank-row on the hardware module. Consequently, two consecutive physical memory addresses can be mapped to memory cells
that are located on different ranks, banks, or rows. For example, on Intel Ivy Bridge CPUs the 20th bit of the physical address determines the rank. As such, the consecutive physical addresses 0x2FFFFF and 0x300000 can be located on front and back side of the DIMM for this architecture. The knowledge of the physical memory location on the DIMM is important for both rowhammer attacks and defenses, since bit flips can only occur on the same bank. For Intel processors, the exact mapping is not officially documented, but has been reverse engineered [16, 27].

B. Rowhammer Overview and Challenges

As mentioned before, memory access control is an essential building block of modern computer security, e.g., to achieve process isolation, isolation of kernel code, and manage read-write-execute permission on memory pages. Modern systems feature a variety of mechanisms to isolate memory, e.g., paging [11], virtualization [11, 10], IOMMU [2], and special execution modes like SGX [11] and SMM [11]. However, these mechanisms enforce their isolation through hardware that mediates the physical memory accesses (in most cases the CPU). Hence, memory assigned to isolated entities can potentially be co-located in physical memory on the same bank. Since a rowhammer attack induces bit flips in co-located memory cells, it provides a subtle way to launch a remote attack to undermine memory isolation.

Recently, various rowhammer-based attacks have been presented. Specifically, rowhammer was utilized to undermine isolation of operating system and hypervisor code, and escape from application sandboxes leveraged in web browsers. In the following, we describe the challenges and workflow of rowhammer attacks. A more elaborated discussion on real-world, rowhammer-based exploits will be provided in Section IX

The rowhammer fault allows an attacker to influence the electrical charge of individual memory cells by activating neighboring memory cells. In particular, Kim et al. [12] demonstrate that repeatedly activating two rows separated by only one row, called aggressor rows (1 and 3 in Figure 2), lead to a bit flip in the enclosed row (2), called victim row. To do so, the attacker has to overcome the following challenges: (i) undermine memory caches to directly perform repetitive reads on physical DRAM memory, and (ii) gain access to memory co-located to data critical to memory isolation.

Overcoming challenge (i) is complicated because modern CPUs feature different levels of memory caches which mediate read and write access to physical memory. Caches are important as processors are orders of magnitude faster than current DRAM hardware, turning memory accesses into a bottleneck for applications [25]. Usually, caches are transparent to software, but many systems feature special instructions, e.g., clflush or movnti for x86 [18, 21], to undermine the cache. Further, caches can be undermined by using certain read-access patterns that force the cache to reload data from physical memory. Such patterns exist, because CPU caches are much smaller than physical memory, and system engineers have to adopt an eviction strategy to effectively utilize caches. Through alternating accesses to addresses which reside in the same cache line, the attacker can force the memory contents to be fetched from physical memory.

The attacker’s second challenge (ii) is to achieve the physical memory constellation shown in Figure 2. The attacker needs access to the aggressor rows in order to be able to activate (hammer) them (rows 1 and 3 in Figure 2). Additionally, the victim row must contain data which is attackable by a bit flip (2) in Figure 2. Both conditions cannot be enforced by the attacker, however, he can achieve them with high probability through the following approaches. First, the attacker allocates memory hoping that the aggressor rows are contained in the allocated memory. If the operating system maps the attacker’s allocated memory to the physical memory containing the aggressor rows the attacker has achieved the first condition. Since the attacker has no influence on the mapping between virtual memory and physical memory he cannot directly influence this step, but he can increase the probability by allocating large amounts of memory; also, the attacker can repeat this step until he succeeds. Once the attacker has the aggressor rows under his control he releases all allocated memory except the parts containing the aggressor rows. Next, the attacker needs the data he wants to manipulate to be stored in the victim row. Again, he cannot directly influence which data is stored in the physical memory and needs to resort to a probabilistic approach. The attacker induces the creation of many copies of the victim data with the goal that one copy of the victim data will be placed in the victim row. The attacker cannot directly verify whether the second step was successful, he has to execute the rowhammer attack and check if the attack is successful, otherwise he has to repeat the second step.

In [21], the authors successfully implemented this approach to compromise the kernel from an unprivileged user process. They gain control over the aggressor rows and then make the OS create huge amounts of page table entries with the goal of placing one page table entry in the victim row. By flipping a bit in a page table entry the authors gain control over a subtree of the page tables allowing them to manipulate memory access control policies.

III. Threat Model and Assumptions

Our threat model is in line with related work [4, 7, 18, 19, 21, 27]: rowhammer-based attacks assume that the
adversary is capable of executing malicious code in an isolated environment. Depending on the attack scenario, the isolated environment can be a JavaScript to launch browser-based attacks, a malicious user-mode application to construct kernel exploits, or an entire operating system for running attacks against co-located virtual machines in a cloud setting. The goal of an adversary is to undermine the isolation. In other words, the attacker aims to break out of the established trust boundary by inducing bit flips in memory that does not belong to the isolated environment. Ultimately, an adversary gains a higher privilege level than originally assigned to the isolated environment.

Our threat model differentiates between reliable and unreliable bit flips. The former can be reproduced, e.g., across multiple reboots, the latter cannot be produced on every attempt to flip a bit through rowhammer. Note that all available rowhammer-based attacks depend on reliable bit flips. However, in this paper, we consider software-defenses against both types of bit flips.

IV. OVERVIEW AND DESIGN

In this section, we present the high-level idea and design of our practical software-based defenses against rowhammer attacks. Our first defense, dubbed B-CATT, mitigates malicious bit flips by marking memory vulnerable to rowhammer as unavailable at boot-time. In contrast, our second defense, called G-CATT, tackles the malicious effect of rowhammer-induced bit flips by instrumenting the operating system’s memory allocator to constrain bit flips to the boundary where the attacker’s malicious code executes (cf. Section III). Both solutions B-CATT and G-CATT are completely transparent to applications, and do not require any hardware changes. We provide a detailed description of our implementation of both solutions in Section V-A.

A. Boot-CATT

Prior to launching a rowhammer attack, the attacker needs to probe the memory to locate vulnerable memory. Hence, a software-only defense needs to identify the vulnerable memory parts and mark them as unavailable. While simple in theory, it was commonly believed that this defense strategy is inefficient and significantly reduces the amount of available memory [12]. To validate this, we developed B-CATT, a new bootloader extension that locates and disables vulnerable memory parts (see Figure 3a). Implementing this defense strategy is challenging without inducing performance penalties. While we investigated different implementation strategies, we opted for a bootloader extension in order to protect a wide range of operating systems. That is, our bootloader-based approach does not require any changes to the operating system and is fully compatible with legacy systems.

In general, all bootloaders commit a list of available memory to the operating system (3). This list is dynamically obtained during boot time using the system’s firmware (e.g., BIOS/UEFI). It is common that certain physical memory addresses cannot be used by the operating system, e.g., the memory reserved for hardware devices such as graphics or network cards. B-CATT extends the bootloader and hooks into this process. Specifically, it adds the physical addresses of vulnerable memory to the list of unavailable memory (2).

To locate vulnerable addresses, we re-use techniques from existing rowhammer exploitation tools [6, 7] and slightly adjust them for the purpose of our approach. Note that this analysis is performed offline prior the system is protected with B-CATT (1). From the operating system’s perspective, the vulnerable physical memory simply becomes unavailable (4). Since handling unavailable memory regions is a core functionality of operating systems, B-CATT adheres to common system functionality.

B. Generic-CATT

Note that B-CATT takes a snapshot of vulnerable memory addresses. Since there is no security guarantee that vulnerable memory changes over time or other memory addresses get vulnerable under different test conditions, we developed a second prototype that provides long-term protection against rowhammer attacks. Our second defense, called G-CATT, follows a different and more generic defense strategy: it tolerates rowhammer-induced bit flips, but prevents bit flips from affecting memory belonging to higher-privileged security domains, e.g., the operating system kernel or co-located virtual machines. As discussed in Section II-B, a rowhammer attack requires the adversary to bypass the CPU cache. Further, the attacker must arrange the physical memory layout such that the targeted data is stored in a row that is physically adjacent to rows that are under the control of the attacker. Hence, G-CATT ensures that memory between these two entities is physically separated by at least one row.

To do so, G-CATT extends the physical memory allocator to partition the physical memory into security domains. G-CATT supports a wide range of memory partitioning levels, i.e., the granularity of security domains can be tuned from coarse-grained levels such as the separation between user and kernel memory to fine-grained memory partition within a single process.

Figure 3b illustrates the concept. Without G-CATT the attacker is able to craft a memory layout, where two aggressor rows enclose a victim row of a higher-privileged domain such as row 3 in Figure 3. With G-CATT in place, the rows which are controlled by the attacker are grouped into the security domain A, whereas memory belonging to higher-privileged entities resides with their own security domain (e.g., the security domain B). Both domains are physically separated by at least one row which will not be assigned to any security domain.

Security Domains. The definition of security domains is critical to ensure the effectiveness of G-CATT. Judging from previous privilege escalation attacks, good candidates for such domains are kernel and user-mode, virtual machines, as well as plugins and scripts in web browsers. Privilege escalation attacks are popular and pose a severe threat to modern systems. In particular, the isolation of kernel and user-mode is critical and the most appealing attack target. If a user-space application

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Kim et al. [12] mention that the rowhammer fault does not only affect memory cells of directly adjacent rows, but also memory cells of rows that are next to the adjacent row. Although we did not encounter such cases in our experiments, G-CATT supports multiple row separation between adversary and victim data memory.
The physical isolation of data raises the challenge of the described scenarios. Beyond kernel and user-mode, we believe that there is no major code. Although we have not yet implemented security domains allocations of trusted browser code and untrusted sandboxed ing escapes in browsers [4], G-CATT needs to distinguish the security domain for untrusted third-party processes. For in- and deallocations will eventually lead to inefficient usage of memory, i.e., memory fragmentation. If memory fragmentation is an issue, G-CATT could resort in only assigning a dedicated security domain for untrusted third-party processes. For in-process isolation, e.g., to prevent rowhammer-based sandboxing escapes in browsers [4], G-CATT needs to distinguish the allocations of trusted browser code and untrusted sandboxed code. Although we have not yet implemented security domains beyond kernel and user-mode, we believe that there no major conceptual obstacles in supporting security domains for each of the described scenarios.

Challenges. The physical isolation of data raises the challenge of how to effectively isolate the memory of different system entities. To tackle this challenge, we first require knowledge of the mapping between physical addresses and memory banks. Since an attacker can only corrupt data within one bank, but not across banks, G-CATT only has to ensure that security domains of different system entities are isolated within each bank. However, as mentioned in Section II-A, hardware vendors do not specify the exact mapping between physical address and banks. Fortunately, Pessl et al. [16] and Xiao et al. [27] provide a methodology to reverse engineer the mapping. For G-CATT, we use this methodology to discover the physical addresses of rows.

Lastly, we need to ensure that the physical memory management component is aware of the isolation policy. This is vital as the memory management components have to ensure that newly allocated memory is adjacent only to memory belonging to the same security domain. To tackle this challenge, we instrumented the memory allocator to keep track of the domain association of physical memory and serve memory requests by selecting free memory from different pools depending on the security domain of the requested memory.

V. IMPLEMENTATION

Both of our software-based defenses are based on modifications to low-level system software components, i.e., the bootloader (B-CATT) and the operating system kernel (G-CATT). We chose GRUB2 and Linux 4.6 as targets for our proof-of-concept implementations for two reasons: (1) their source code is freely available, and (2) both projects are widely used. First, we briefly describe how B-CATT blacklists rowhammer-affect ed pages. Thereafter, we explain the implementation of G-CATT’s policy enforcement mechanism in the Linux kernel which allows for the partitioning of physical memory into isolated security domains. Note that our prototype implementation of B-CATT targets x86-based systems, whereas G-CATT targets both x86 and ARM-based systems. Until today, rowhammer attacks have been only demonstrated for these two prominent architectures. Furthermore, as mentioned before, our prototype implementations target rowhammer exploits that aim at violating the isolation between kernel and user-mode since these are the most prominent and practical types of rowhammer exploits.

A. B-CATT

To mitigate the exploitation of the rowhammer hardware bug in legacy systems, B-CATT features a blacklisting mechanism to prevent the operating system from using vulnerable pages. Recall that Kim et al. [12] concluded that blacklisting is not practical if the majority of rows are susceptible to rowhammer. However, our evaluation (Section VI-A2) suggests that only a fraction of rows are vulnerable in practice. This is also in line with previous work [21]. In fact, we noticed that blacklisting vulnerable memory is highly practical as it only requires a small extension to the bootloader (64 lines of code). We exploit the fact that operating systems already feature a function that allows blacklisting certain physical memory addresses. Specifically, x86 compatible operating systems detect usable memory through the so-called e820 map [9]. This map contains a list of usable physical memory. It can be
obtained from the BIOS through the interrupt number 0x820. On modern systems, this map is not directly requested by the operating system. In contrast, the bootloader forwards the map to the operating system. To prevent rowhammer attacks, B-CATT instruments the GRUB2 bootloader to add physical addresses of vulnerable memory to the e820 map. Note that the original e820 specification only supports 128 entries. However, the EFI Platform Initialization specification – which is also supported by GRUB2 – does not limit the number of entries \[23\]. In fact, GRUB2 first allocates a buffer to store both the original e820 map and additional entries. Once it has stored the original e820 entries into this buffer, it passes a pointer to this buffer to the operating system. Our B-CATT patch increases the size of the allocated buffer to additionally fit the entries for the blacklisted pages.

Figure 4 depicts the detailed workflow of B-CATT. After upgrading the existing GRUB2 installation, the vulnerable memory rows are identified with the help of publicly available tools during an offline analysis \[6, 7, 21\]. These programs scan the memory of the machine for vulnerable pages by allocating large amounts of memory and trying to produce bit flips. We made some modifications, which we describe in detail in Section VI-A.

Further, these rows are included as an environment variable in the boot configuration file of GRUB2 (Step 1). Next, the BIOS starts GRUB2 which then requests the e820 map (Step 2-4). Before GRUB2 starts the operating system, it reads out the environment variable and extends the e820 map (Step 5-6). Henceforth, the Linux kernel will not use the vulnerable memory thereby preventing the attacker from leveraging rowhammer-based attacks.

2) Tracking Security Domains: The extension of the page frame map associates pages to security domains. However, this assignment is dynamic and changes over time. In particular, a page frame may be requested, allocated, and used by one domain, after it has been freed by another domain. Note that this does not violate our security guarantees, but is necessary for the system to manage physical memory dynamically. Yet, we need to ensure that page frames being reallocated continue to obey our security policy. Therefore, we reset the security domain upon freeing a page.

In the following, we describe how we map individual memory pages to domains, keep track of different domains, modify the physical memory allocator, and define partitioning policies for the system’s DRAM hardware.

1) Mapping Page Frames to Domains: To be able to decide whether two pages belong to the same security domain we need to keep track of the security domain for each page frame. Fortunately, the kernel already maintains meta data about each individual page frame. More specifically, each individual page frame is associated with exactly one meta data object (struct page). The kernel keeps a large array of these objects in memory. Although these objects describe physical pages, this array is referred to as virtual memory map, or vmemmap. The Page Frame Number (PFN) of a physical page is used as an offset into this array to determine the corresponding struct page object. To be able to associate a page frame with a security domain, we extend the definition of struct page to include a field that encodes the security domain. Since our prototype implementation targets rowhammer attacks that aim at violating the separation of kernel and user-space, we encode security domain 0 for kernel-space, and 1 for user-space. For preventing rowhammer attacks crossing the process boundary, G-CATT could exploit the process identification number (PID) to distinguish security domains. As such, each process will be treated as a separate security domain, and the kernel will be associated with its own security domain.

In our proof-of-concept implementation of G-CATT, we focus on hardening Linux against rowhammer-based attacks since its memory allocator is open-source. We successfully applied the described changes to the x86-kernel version 4.6 and the Android kernel for Nexus devices in version 4.4.

The basic idea underlying our generic software-based rowhammer defense is to physically separate rows that belong to different security domains. Operating systems are not per-se aware of the notions of cells and rows, but rather build memory management based on paging. Commodity operating systems use paging to map virtual addresses to physical addresses. The size of a page varies among architectures. On x86 and ARM, the page size is typically 4096 bytes (4K). As we described in Section II-A, DRAM hardware consists of much smaller units of memory, i.e., individual memory cells storing single bits. Eight consecutive memory cells represent a byte, 4096 consecutive bytes a page frame, two to four page frames a row. Hence, our implementation of G-CATT changes low-level components of the kernel to make the operating system aware of the concept of memory rows.
To achieve physical separation of user space, we need to implement a strategy for isolating individual user processes. This includes providing an implementation that enforces strict physical isolation. In the following, we describe our implementation of the partitioning strategy that leverages the physical address to DRAM mapping information beyond x86 and ARM. We build on this prior research and implement various strategies for architectures and memory configurations that are supported on x86 starting with Intel’s Skylake and AMD’s Zen architecture. Hence, it is possible to develop similar policy implementations for additional hardware configurations.

3) Modifying the Physical Page Allocator: The Linux kernel uses different levels of abstraction for different memory allocation tasks. The physical page allocator, or *zoned buddy allocator*, is the main low-level facility handling physical page allocations. It exports its interfaces through functions such as `alloc_pages`, which can be used by other kernel components to request physical pages. In contrast to higher-level allocators, the buddy allocator only allows for allocating sets of memory pages with a cardinality which can be expressed as a power of two (this is referred to as the order of the allocation). Hence, the buddy allocator’s smallest level of granularity is a single memory page. We modify the implementation of the physical page allocator in the kernel to include a mechanism for separating and isolating allocated pages according to the security domain of the origin of the allocation request. In particular, the page allocator already performs maintenance checks on free pages. We extend these maintenance checks to add our partitioning policy before the allocator returns a physical page. If this check fails, the page allocator is not allowed to return the page in question, but has to continue its search for another free page.

4) Defining DRAM Partitioning Policies: Separating and isolating different security domains is essential to our proposed mitigation. For this reason, we incorporate detailed knowledge about the platform and its DRAM hardware configuration into our policy implementation. While our policy implementation for a target system largely depends on its architecture and memory configuration, this does not represent a fundamental limitation. Indeed, independent research [16, 27] has provided the architectural details for the most prevalent architectures, i.e., it shows that the physical address to DRAM mapping can be reverse engineered automatically for undocumented architectures. Hence, it is possible to develop similar policy implementations for architectures and memory configurations beyond x86 and ARM. We build on this prior research and leverage the physical address to DRAM mapping information to enforce strict physical isolation. In the following, we describe our implementation of the partitioning strategy for isolating kernel and user-space, as well as providing an implementation strategy for isolating individual user processes.

**Kernel-User Isolation.** To achieve physical separation of user and kernel space, we adopt the following strategy: we divide each bank into a top and a bottom part, with a separating row in-between. Page frames for one domain are exclusively allocated from the part that was assigned to that domain. The part belonging to the kernel domain is determined by the physical location of the kernel image. As a result, user and kernel space allocations may be co-located within one bank, but never within adjacent rows. Different partitioning policies would be possible in theory: for instance, we could confine the kernel to a certain DRAM bank to avoid co-location of user domains within a single bank. However, this would likely result in a severe increase of memory latency, since reads and writes to a specific memory bank are served by the bank’s row buffer. The benefit of our partitioning policy stems from the fact that we distribute memory belonging to the kernel security domain over multiple banks thereby not negatively impacting performance. For our solution towards kernel isolation, we only need to calculate the row index of a page frame. More specifically, we calculate this index from the physical address (PA) in the following way:

$$\text{Row}(PA) := \frac{\text{PA}}{\text{PageSize} \cdot \text{PagesPerDIMM} \cdot \text{DIMMs}}$$

Here, we calculate the number of pages per DIMM as $\text{PagesPerDIMM} := \text{PagesPerRow} \cdot \text{BanksPerRank} \cdot \text{RanksPerDIMM}$. Because all possible row indices are present once per bank, this equation determines the row index of the given physical address. We note, that this computation is in line with the available rowhammer exploits [21] and the reported physical to DRAM mapping recently reverse engineered [16, 27]. Since the row size is the same for all Intel architectures prior to Skylake [7], our implementation for this policy is applicable to a wide range of system setups, and can be adjusted without introducing major changes to fit other configurations as well.

**Isolating User Processes.** To physically isolate individual user processes, we suggest a more flexible partitioning policy, i.e., not requiring user space pages to be confined to a certain part of DRAM. Instead, we propose to check process pages for conflicting security domains dynamically. For instance, the kernel could prevent the physical memory allocator from assigning a page to a process, which contains neighboring memory cells in the rows directly above or below, that already belong to another process. In case such a memory constellation is detected, the buddy allocator would deny handing out the page, otherwise it would be allowed to assign the page to the requesting process. While this partitioning policy is much more fine-grained than the policy we adopt for isolating the kernel from processes, our implemented mechanism supports such a strategy in principle. However, implementing this policy is more complex than maintaining a fixed boundary between two domains, since we also need to calculate the channel, rank, and bank index for each page frame in this case. Hence, an implementation of a process-isolation policy is more specific to the individual hardware setup and would require several different implementations to support additional hardware configurations.

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2This is usually at 1MB, although Kernel Address Space Layout Randomization (KASLR) may slightly modify this address according to a limited offset.

5The default values for DDR3 on x86 are 4K for the page size, 2 pages per row, 8 banks per rank, 2 ranks per DIMM and between 1 one 4 DIMMs per machine. For DDR4 the number of banks per rank was doubled. DDR4 is supported on x86 starting with Intel’s Skylake and AMD’s Zen architecture.
Averaged the amount of bit flips. Executed the rowhammer test on each system three times and rebooting the system after each test run, we found 133 pages with exploitable bit flips for S1, 31 pages for S2, and 23 pages for S3.

Table II: Results of our security evaluation. We found that B-CATT and G-CATT can mitigate rowhammer attacks. We executed the rowhammer test on each system three times and averaged the amount of bit flips.

VI. SECURITY EVALUATION

The main goal of our software-based defenses is to protect legacy systems from rowhammer attacks. We tested the effectiveness of B-CATT and G-CATT on diverse hardware configurations. Among these, we identified three hardware configurations, where we observed many reproducible bit flips. Table I lists the exact configurations of the three platforms we use for our evaluation. Our effectiveness evaluation of B-CATT and G-CATT is based on two attack scenarios. For the first scenario we systematically search for reproducible bit flips based on a tool published by Gruss et al. Our second attack scenario leverages a real-world rowhammer exploit published by Google’s Project Zero. We compared the outcome of both attacks on our vulnerable systems before and after applying B/G-CATT. As shown in Table II both tests only succeed when our protections are not in place. Next, we elaborate on the two attack scenarios and their mitigation in more detail.

A. Rowhammer Testing Tool

We use a slightly modified version of the double-sided rowhammering tool, which is based on the original test by Google’s Project Zero [21]. Specifically, we extended the tool to also report the aggressor physical addresses, and adjusted the default size of the fraction of physical memory that is allocated. The tool scans the system memory for memory cells that are vulnerable to the rowhammer attack. To provide comprehensive results, the tool needs to scan the entire memory of the system. However, investigating the entire memory is hard to achieve in practice since some parts of memory are always allocated by other system components. These parts are therefore not available to the testing tool, i.e., memory reserved by operating system. To achieve maximum coverage, the tool allocates a huge fraction of the available memory areas. However, due to the lazy allocation of Linux the allocated memory is initially not mapped to physical memory. Hence, each mapped virtual page is accessed at least once, to ensure that the kernel assigns physical pages. Because user space only has access to the virtual addresses of these mappings, the tool exploits the /proc/pagemap kernel interface to retrieve the physical addresses. As a result, most of the systems physical memory is allocated to the rowhammering tool. We also discuss on how we achieve almost full coverage in Section VII-C.

Afterwards, the tool analyzes the memory in order to identify potential victim and aggressor pages in the physical memory. As the test uses the double-sided rowhammering approach two aggressor pages must be identified for every potential victim page. Next, all potential victim pages are challenged for vulnerable bit flips. For this, the potential victim page is initialized with a fixed bit pattern and “hammered” by accessing and flushing the two associated aggressor pages. This ensures that all of the accesses activate a row in the respective DRAM module. This process is repeated 10^6 times. Lastly, the potential victim address can be checked for bit flips by comparing its memory content with the fixed pattern bit. The test outputs a list of addresses for which bit flips have been observed, i.e., a list of victim addresses.

1) Preliminary Tests for Vulnerable Systems: Using the rowhammering testing tool we evaluated our target systems. In particular, we were interested in systems that yield reproducible bit flips, as only those are relevant for practical rowhammer attacks. This is because an attacker cannot force the system to allocate page tables at a certain physical position in RAM. In contrast, the attacker sprays the memory with page tables to increase her chance of hitting the desired memory location.

Hence, we configured the rowhammering tool to only report memory addresses where bit flips can be triggered repeatedly. We successively confirmed that this list indeed yields reliable bit flips by individually triggering the reported addresses and checking for bit flips within an interval of 10 seconds. Additionally, we tested the bit flips across reboots through random sampling.

The three systems mentioned in Table II are highly susceptible to reproducible bit flips. Executing the rowhammer test on these three times and rebooting the system after each test run, we found 133 pages with exploitable bit flips for S1, 31 pages for S2, and 23 pages for S3.

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https://github.com/IAIK/rowhammerjs/tree/master/native
https://bugs.chromium.org/p/project-zero/issues/detail?id=283
2) **B-CATT**: We installed B-CATT on our three test systems S1 – S3. For each system, we blacklisted the vulnerable physical pages collected in the previous step. We first verified that the list of vulnerable memory pages was correctly reported to the operating system. B-CATT adds vulnerable pages as reserved regions to the e820 map (cf. Section V). Hence, these pages need to be listed in the e820 map used by the OS.

Next, we executed the rowhammer test on the evaluation systems to verify that it can no longer find vulnerable memory addresses. We executed the test three times on each system to yield a reasonable coverage. For all test runs, the rowhammer test failed with an error message when trying to allocate the physical addresses that belongs to a blacklisted page. As such, all attempts of bit flips on vulnerable pages are prevented by B-CATT. Thus, B-CATT prevents all previously presented rowhammer attacks [4, 7, 18, 21].

3) **G-CATT**: To install G-CATT, we patched the Linux kernel of each system to use our modified memory allocator. Recall that G-CATT does not aim to prevent bit flips but rather constrain them to a security domain. Hence, executing the rowhammer test on G-CATT-hardened systems still locates vulnerable pages. However, in the following, we demonstrate based on a real-world exploit that the vulnerable pages are not exploitable.

### B. Real-world Rowhammer Exploit

To further demonstrate the effectiveness of our mitigations, we tested B-CATT and G-CATT against a real-world rowhammer exploit. The goal of the exploit is to escalate the privileges of the attacker to kernel privileges (i.e., gain root access). To do so, the exploit leverages rowhammer to manipulate the page tables. Specifically, it aims to manipulate the access permission bits for kernel memory, i.e., reconfigure its access permission policy[7].

To launch the exploit, two conditions need to be satisfied: (1) a page table entry must be present in a vulnerable row, and (2) the enclosing aggressor pages must be allocated in attacker-controlled memory.

Since both conditions are not directly controllable by the attacker, the attack proceeds as follows: the attacker allocates large memory areas. As a result, the operating system needs to create large page tables to maintain the newly allocated memory. This in turn increases the probability to satisfy the aforementioned conditions, i.e., a page table entry will eventually be allocated to a victim page. Due to vast allocation of memory, the attacker also increases her chances that aggressor pages are co-located to the victim page.

Once the preconditions are satisfied, the attacker launches the rowhammer attack to induce a bit flip in victim page. Specifically, the bit flip modifies the page table entry such that a subtree of the paging hierarchy is under the attacker’s control. Lastly, the attacker modifies the kernel structure that holds the attacker-controlled user process privileges to elevate her privileges to the superuser root. Since the exploit is probabilistic, it only succeeds in five out of hundred runs. Nevertheless, a single successful run allows the attacker to compromise of the entire system.

1) **B-CATT**: As B-CATT prevents any rowhammer induced bit flips on a system, it also prevents this exploit. As vulnerable memory pages are not available anymore, the attacker does not succeed in allocating page table entries on vulnerable pages. Hence, the attacker cannot manipulate the kernel’s page tables.

2) **G-CATT**: Our generic defense mechanism does not prevent the occurrence of bit flips on a system. Hence, we have to verify that bit flips cannot affect data of another security domain. Rowhammer exploits rely on the fact that such a cross domain bit flip is possible, i.e., in the case of our exploit it aims to induce a bit flip in the kernel’s page table entries.

However, since the exploit by itself is probabilistic, an unsuccessful attempt does not imply the effectiveness of G-CATT. As described above, the success rate of the attack is about 5%. After deploying G-CATT on our test systems we repeatedly executed the exploit to minimize the probability of the exploit failing due to the random memory layout rather than due to our protection mechanism. We automated the process of continuously executing the exploit and ran this test for 45h on all three test systems. In this time frame, the exploit made on average 3500 attempts of which on average 175 should have succeeded. However, with G-CATT, none of the attempts was successful. Hence, as expected, G-CATT effectively prevents rowhammer-based exploits.

As we have demonstrated, G-CATT successfully prevents the original attack developed on x86 by physically isolating pages belonging to the kernel from the user-space domain. In addition to that, the authors of the Drammer exploit [24] confirm that G-CATT prevents their exploit on ARM. The reason is, that they follow the same strategy as in the original kernel exploit developed by Project Zero, i.e., corrupting page table entries in the kernel from neighboring pages in user space. Hence, G-CATT effectively prevents rowhammer exploits on ARM-based mobile platforms as well.

### VII. PERFORMANCE EVALUATION

One of our main goals is practicability, i.e., inducing negligible performance overhead. To demonstrate practicability of our two defenses, we thoroughly evaluated the performance and stability impact of B-CATT and G-CATT on different benchmark and testing suites. In particular, we used the SPEC CPU2006 benchmark suite [8] to measure the impact on CPU-intensive applications, LMBench3 [15] for measuring the overhead of system operations, and the Phoronix test suite [17] to measure the overhead for common applications. We use the Linux Test Project, which aims at stress testing the Linux kernel, to evaluate the stability of our test system after deploying B-CATT and G-CATT. We performed all of our performance evaluation on system S2 (cf. Table I).

### A. Run-time Overhead

Table III summarizes the results of our performance benchmarks. In general, the SPEC CPU2006 benchmarks measure the impact of system modifications on CPU intensive applications. Since our mitigations mainly affect the physical memory...
management, we did not expect a major impact on these benchmarks. However, since these benchmarks are widely used and well established we included them in our evaluation. In fact, we observe a minimal performance improvement for B-CATT by 0.43% and G-CATT by 0.49% which we attribute to measuring inaccuracy. Such results have been reported before when executing a set of benchmarks for the same system with the exact same configuration and settings. Hence, we conclude that B/G-CATT does not incur any performance penalty.

LMBench3 is comprised of a number of micro benchmarks which target very specific performance parameters, e.g., memory latency. For our evaluation, we focused on micro benchmarks that are related to memory performance and excluded networking benchmarks. Similar to the previous benchmarks, the results fluctuate on average between $-0.4\%$ and $0.11\%$. Hence, we conclude that both of our mitigations have no measurable impact on specific memory operations.

Finally, we tested the impact of our modifications on the Phoronix benchmarks. In particular, we selected a subset of benchmarks\(^\text{[10]}\) that, on one hand, aim to measure memory performance (IOZone and Stream), and, on the other hand, test the performance of common server applications which usually rely on good memory performance.

To summarize, our rigorous performance evaluation with the help of different benchmarking suites did not yield any measurable overhead. This makes B-CATT and G-CATT highly practical mitigations against rowhammer attacks.

### B. Memory Overhead

Both, B-CATT and G-CATT, prevent the operating system from allocating certain physical memory.

For B-CATT the memory overhead depends on the individual system, since all memory pages containing vulnerable memory cells are blacklisted. As this list is specific per system, we cannot make general statements. However, we evaluated the memory overhead for our three test systems. Table IV lists the number of blacklisted pages for our test systems $S1$ – $S3$: the total memory pages available in the system and the fraction of blacklisted pages from the overall memory. As shown, the memory overhead of B-CATT is at most $0.0063\%$ (<1MB) for our test systems.

The memory overhead of G-CATT is constant and depends solely on number of memory rows per bank. Per bank, G-CATT omits one row to provide isolation between the security domains. Hence, the memory overhead is $1/\#\text{rows}$ ($\#\text{rows}$ being rows per bank). While the number of rows per bank is dependent on the system architecture, it is commonly in the order of $2^{15}$ rows per bank\(^\text{[17]}\) i.e., the overhead is $2^{-15} \approx 0.003\%$.

### C. Robustness

Our mitigations restrict the operating systems access to the physical memory. To ensure that this has no effect on the overall stability, we performed numerous stress tests with the help of the Linux Test Project (LTP)\(^\text{[14]}\). These tests are designed to cause problems for the operating system. We first run these tests on a vanilla Debian 8.2 installation to receive a baseline for the evaluation of B-CATT and G-CATT. We summarize our results in Table V and report no deviations for our mitigations compared to the baseline. Further, we also did

| System | Blacklisted pages | Total pages | Overhead  |
|--------|-------------------|-------------|-----------|
| $S1$   | 133               | 2,097,152   | 0.0063\%  |
| $S2$   | 31                | 2,097,152   | 0.0015\%  |
| $S3$   | 23                | 2,097,152   | 0.0011\%  |

Table IV: Memory overhead for B-CATT.

\(^{10}\)The Phoronix benchmarking suite features a large number of tests which cover different aspects of a system. By selecting a subset of the available tests we do not intend to improve our performance evaluation. On the contrary, we choose a subset of tests that is likely to yield measurable performance overhead, and excluded tests which are unrelated to our modification, e.g., GPU or machine learning benchmarks.

\(^{14}\)https://lackingrhoticity.blogspot.de/2015/05/how-physical-addresses-map-to-rows-and-banks.html
not encounter any problems during the execution of the other benchmarks. Thus, we conclude that B-CATT and G-CATT do not affect the stability of the protected system.

VIII. DISCUSSION

Both of our prototype implementations target Linux-based systems. Linux is open-source allowing us to implement our defenses. Further, all publicly available rowhammer attacks target this operating system. B-CATT already protects all operating systems that can be loaded with the commodity bootloader GRUB2. Further, G-CATT can be easily ported to memory allocators deployed in other operating systems. In this section, we discuss in detail the generality and coverage aspects of our software-based defenses against rowhammer.

A. Generality Aspects of B-CATT

Extending the GRUB2 bootloader to blacklist vulnerable memory allows us to protect all Linux-based systems, OpenBSD, and Xen [26]. Xen is an open-source hypervisor that is widely deployed on production systems. Similar to the Linux kernel, Xen receives the list of available and reserved memory through GRUB2. Hence, the current implementation of B-CATT can defeat recently presented rowhammer attacks in a cloud scenario [19] [27].

Unfortunately, GRUB2 is not capable of directly booting Windows systems. Instead, in order to boot Windows, GRUB2 starts the native bootloader of the Windows installation. This process is called chainloading. GRUB2 does not pass the list of unavailable memory addresses to the Windows bootloader, i.e., the Windows components discover the memory layout by themselves. To make B-CATT available to Windows three approaches are possible: (1) Microsoft extends its bootloader to include the modifications we applied to GRUB2. (2) The BIOS vendor adapts B-CATT and provides a modified e820 which includes vulnerable memory. (3) GRUB2 hooks into the e820 BIOS interrupt allowing B-CATT to add vulnerable memory when the Windows bootloader searches for usable memory.

In the current implementation of B-CATT we do not support UEFI. However, since UEFI provides a similar mechanism to the e820 map, there are no obstacles to add support for UEFI in B-CATT.

B. Generality Aspects of G-CATT

With our current implementation of G-CATT we focus on isolating the user and kernel memory to prevent privilege escalation attacks, because this is the most practical and single publicly available attack vector. However, as described in Section V-B2 we are currently looking into isolating memory of user processes, i.e., assigning a security domain per process. Although we are not aware of any cross-process rowhammer attacks we anticipate to see such attacks in the future as an alternative to kernel-based privilege escalation attacks. Further, these attacks are conceptually similar to cross-VM attacks which have been already demonstrated recently [19].

By isolating the physical memory of different processes, G-CATT can stop such attacks (cf. Section V-B2). Similarly, when implementing G-CATT in the hypervisor, physical memory of different virtual machines (VMs) can be isolated.

1) Fine-Grained In-Process Isolation: In fact, our design also allows an fine-grained isolation within a process. Separation within a single process has many security applications, e.g., application sandboxes, or isolating attacker-controllable data. As an example, in 2014, Microsoft improved the heap allocator for Internet Explorer which separates the heap objects on the heap into two parts [27]. As shown in Figure 5, data objects in virtual memory are divided into meta data and payload data. The payload data (Buffer1 and Buffer2) are attacker-controlled data. The meta data (length and *ptr) are usually isolated from the attacker. In the example from Figure 5, the array object is comprised of a memory buffer (Buffer2), a pointer to the buffer (Buffer + *ptr) and a field for the length (length). On a monolithic heap the meta data (length and *ptr) would be adjacent with the corresponding buffer (Buffer2). In this case, the attacker can overwrite the meta data by overflowing Buffer2.

The separated heap, as shown in Figure 5, prevents this attack, as an overflow in Buffer2 would only affect other attacker-controlled data (e.g., Buffer1). However, the separation of meta data and payload data exists only in the virtual memory space. In the physical memory space meta data and payload data can still be stored in adjacent locations: Figure 5 shows a possible mapping of the data into physical memory.

Given this setting, the attacker can modify the meta data by leveraging rowhammer. By “hammering” Buffer1 and Buffer2, she can launch a double-sided rowhammer attack. As a result, she can modify data belonging to security domain A by accessing data of security domain B [4] [7].

To prevent such attacks, the security domain isolation needs to be expanded into the physical memory space. G-CATT allows the creation of arbitrary security domains. However, G-CATT is implemented in the kernel while the semantics of the security domains (the separated heaps) are only known to the application. Hence, to enable applications to have isolation in the physical memory space this information must be provided to the physical memory allocator in the kernel. This can be achieved by extending the memory allocation interface of the kernel (e.g., malloc) with an additional parameter allowing an application to indicate which security domain should be assigned to the newly allocated memory.

Table V: Result for individual stress tests from the Linux Test Project.

| Linux Test Project | Vanilla | B-CATT | G-CATT |
|--------------------|---------|--------|--------|
| clone              | ✓       | ✓      | ✓      |
| ftruncate          | ✓       | ✓      | ✓      |
| pcntl              | ✓       | ✓      | ✓      |
| ptrace             | ✓       | ✓      | ✓      |
| rename             | ✓       | ✓      | ✓      |
| sched_prio_max     | ✓       | ✓      | ✓      |
| sched_prio_min     | ✓       | ✓      | ✓      |
| mmstress           | x       | x      | x      |
| shmt               | x       | x      | x      |
| vhangup            | x       | x      | x      |
| ioctl              | x       | x      | x      |

12 https://technet.microsoft.com/en-us/library/security/ms14-035.aspx
2) Applying G-CATT to Mobile Systems: The rowhammer attack is not limited to x86-based systems, but has been recently shown to also affect the ARM platform [24]. The ARM architecture is predominant in mobile systems, and used in many smartphones and tablets. As G-CATT is not dependent on any x86 specific properties, it can be easily adapted for ARM based systems. We demonstrate this by applying our extended physical memory allocator to the Android kernel for Nexus devices in version 4.4. Since there are no major deviations in the implementation of the physical page allocator of the kernel between Android and stock Linux kernel, we did not encounter any obstacles during the port.

C. Coverage of Rowhammer Testing Tool

B-CATT relies on the fact that all vulnerable memory pages can be identified and blacklisted. In general, the problem of discovering vulnerable bits is orthogonal to the enforcement mechanism by B-CATT. For our prototype implementation and evaluation, we use the rowhammer testing tool developed and published by Google [6]. However, there are two factors that impact the comprehensiveness of identifying vulnerable bits: spatial coverage and temporal coverage. Since identifying vulnerable memory is not required for G-CATT, we focus on B-CATT for the following discussion on this aspect.

1) Spatial Coverage Aspects: The memory coverage of the rowhammer testing tool is limited to the physical memory it can access. Since the rowhammer testing tool executes as an ordinary process on the system, it has no influence on the physical memory assigned when allocating memory. In particular, there are parts of physical memory which will never be assigned to the rowhammer test tool, as some memory is reserved by other systems entities, e.g., memory reserved by the kernel. Figure 5 shows an abstract view of the memory assignment during multiple runs of the rowhammer testing tool. Note that the kernel memory as well as the reserved memory can never be assigned to a process. Hence, the rowhammer testing tool can never test these regions for vulnerable bits.

Additionally, the rowhammer testing tool has to share the system's memory with other processes. Figure 5 shows that the rowhammer testing tool cannot allocate all memory since other processes (and other dynamic components like loadable kernel modules – LKM) also require memory. However, since these memory allocations are dynamic they can easily change among reboots and runs. Figure 5 shows that the coverage of the rowhammer testing tool for each individual run is limited. However, the cumulative coverage of the rowhammer testing tool achieves coverage of the entire process' allocatable memory. Lastly, even if the rowhammer testing tool cannot detect all vulnerable memory bits, it still can detect all bits that are exploitable from the attacker's point of view, i.e., the attacker leverages the same techniques as the rowhammer testing tool to detect vulnerable bits.

2) Temporal Coverage Aspects: Rowhammer is a novel attack technique. To the best of our knowledge, there are no studies on the system’s susceptibility to rowhammer over a large time frame. However, one could easily imagine that memory cells could wear-off over time and cells which have been unaffected before become vulnerable. Since there is no data available whether this can happen or at which rate cells can become vulnerable, no definitive statements can be made at the time of writing. In general, if cells become vulnerable over time, the detection of vulnerable pages would need to be repeated periodically for B-CATT. As mentioned before, these updates can be fully automated to run without requiring user interaction. Moreover, an attacker cannot simply utilize newly appearing victim pages, but would have to repeat the memory profiling for the targeted machine as well.

D. Single-sided Rowhammer Attacks

From our detailed description in Section V-A one can easily follow that both of our proposed solutions can defeat all known rowhammer attacks in general, and single-sided rowhammer attacks [24] in particular. In contrast to double-sided rowhammer attacks (see Figure 2), single-sided rowhammer attacks relax the adversary's capabilities by requiring that the attacker has control over only one row adjacent to the victim memory row. However, as shown in Figure 5 B-CATT will prevent the system from allocating memory that is vulnerable to rowhammer attacks. Hence, even if the system contains memory that is vulnerable to single-sided rowhammer, B-CATT ensures that this memory remains unused throughout the entire run time of the system. As described in more detail in Section V-A G-CATT isolates different security domains in the physical memory. In particular, it ensures that different security domains are separated by at least one buffer row that is never used by the system. This means that the single-sided rowhammer adversary can only flip bits in own memory (that it already controls), or flip bits in buffer rows.

E. Benchmarks Selection

We selected our benchmarks to be comparable to the related literature. Moreover, we have done evaluations that go beyond those in the existing work to provide additional insight. Hereby, we considered different evaluation aspects: We executed SPEC CPU2006 to verify that our changes to the operating system impose no overhead of user-mode applications. Further, SPEC CPU2006 is the most common benchmark in the field of memory-corruption defenses, hence, our solutions can be compared to the related work. LMBench3 is specifically designed to evaluate the performance of common system operations, and used by the Linux kernel developers to test whether changes to the kernel affect the performance. As such LMBench3 includes many tests. For our evaluation we included those benchmarks that perform memory operations and are relevant for our defenses. Indeed we have also tested all other memory-related benchmarks in LMBench3 and observed
For all our benchmarks we did not observe any measurable overhead (0.2%) as well. Finally, we selected a number of common applications from the Phoronix test suite as macro benchmarks, as well as the pts/memory tests which are designed to measure the RAM and cache performance. For all our benchmarks we did not observe any measurable overhead (see Table III).

IX. RELATED WORK

In this section, we provide an overview of existing rowhammer attack techniques, their evolution, and proposed defenses. Thereafter, we discuss the shortcomings of existing work on mitigating rowhammer attacks and compare them to our two software-based defenses.

A. Rowhammer Attacks

Kim et al. [12] were the first to conduct experiments and analyze the effect of bit flipping due to repeated memory reads. They found that this vulnerability can be exploited on Intel and AMD-based systems. Their results show that over 85% of the analyzed DRAM modules are vulnerable. The authors highlight the impact on memory isolation, but they do not provide any practical attack. Seaborn and Dullien [21] published the first practical rowhammer-based privilege-escalation attacks using the x86 clflush instruction. In their first attack, they use rowhammer to escape the Native Client (NaCl) sandbox. NaCl aims to safely execute native applications by 3rd-party developers in the browser. Using rowhammer malicious developers can escape the sandbox, and achieve remote code execution on the target system. With their second attack Seaborn and Dullien utilize rowhammer to compromise the kernel from an unprivileged user-mode application. Combined with the first attack, the attacker can remotely compromise the kernel without exploiting any software vulnerabilities. To compromise the kernel, the attacker first fills the physical memory with page-table entries by allocating a large amount of memory. Next, the attacker uses rowhammer to flip a bit in memory. Since the physical memory is filled with page-table entries, there is a high probability that an individual page-table entry is modified by the bit flip in a way that enables the attacker to access other page-table entries, modify arbitrary (kernel) memory, and eventually completely compromise the system. Qiao and Seaborn [18] implemented a rowhammer attack with the x86 movnti instruction. Since the memcpy function of libc – which is linked to nearly all C programs – utilizes the movnti instruction, the attacker can exploit the rowhammer bug with code-reuse attack techniques [22]. Hence, the attacker is not required to inject her own code but can reuse existing code to conduct the attack. Aweke et al. [3] showed how to execute the rowhammer attack without using any special instruction (e.g., clflush and movnti). The authors use a specific memory-access pattern that forces the CPU to evict certain cache sets in a fast and reliable way. They also concluded that a higher refresh rate for the memory would not stop rowhammer attacks. Gruss et al. [7] demonstrated that rowhammer can be launched from JavaScript. Specifically, they were able to launch an attack against the page tables in a recent Firefox version. Similar to Seaborn and Dullien’s exploit this attack is mitigated by G-CATT. Later, Bosman et al. [4] extended this work by exploiting the memory deduplication feature of Windows 10 to create counterfeit JavaScript objects, and corrupting these objects through rowhammer to gain arbitrary read/write access within the browser. In their follow-up work, Razavi et al. [19] applied the same attack technique to compromise cryptographic (private) keys of co-located virtual machines. Concurrently, Xiao et al. [27] presented another cross virtual machine attack where they use rowhammer to manipulate page-table entries of Xen. Further, they presented a methodology to automatically reverse engineer the relationship between physical addresses and rows and banks. Independently, Pessl et al. [16] also presented a methodology to reverse engineer this relationship. Based on their findings, they demonstrated cross-CPU rowhammer attacks, and practical attacks on DDR4. Van der Veen et al. [24] recently demonstrated how to adapt the rowhammer exploit to escalate privileges in Android on smartphones. Since the authors use the same exploitation strategy of Seaborn and Dullien, G-CATT can successfully prevent this privilege escalation attack. While the authors conclude that it is challenging to mitigate rowhammer in software, we present two viable implementations that can mitigate practical rowhammer attacks.

Note that all these attacks require memory belonging to a higher-privileged domain (e.g., kernel) to be physically co-located to memory that is under the attacker’s control. Since our defenses prevent direct co-location, we mitigate these rowhammer attacks.

B. Defenses Against Rowhammer

Kim et al. [12] present a number of possible mitigation strategies. Most of their solutions involve changes to the hardware, i.e., improved chips, refreshing rows more frequently, or error-correcting code memory. However, these solutions are not very practical: the production of improved chips requires an improved design, and a new manufacturing process which would be costly, and hence, is unlikely to be implemented. The idea behind refreshing the rows more frequently (every 32ms instead of 64ms) is that the attacker needs to hammer rows...
many times to destabilize an adjacent memory cell which eventually causes the bit flip. Hence, refreshing (stabilizing) rows more frequently could prevent attacks because the attacker would not have enough time to destabilize individual memory cells. Nevertheless, Aweke et al. [3] were able to conduct a rowhammer attack within 32ms. Therefore, a higher refresh rate alone cannot be considered as an effective countermeasure against rowhammer. Error-correcting code (ECC) memory is able to detect and correct single-bit errors. As observed by Kim et al. [12] rowhammer can induce multiple bit flips which cannot be detected by ECC memory. Further, ECC memory has an additional space overhead of around 12% and is more expensive than usual DRAM, therefore it is rarely used.

Kim et al. [12] also suggest to disable faulty rows similar to our B-CATT that we present in Section IV-A. However, they provide no implementation and evaluation. In contrast, we present the full implementation and evaluation of B-CATT. While the authors concluded that this strategy is not practical, we demonstrate that it is an efficient and practical solution that effectively prevents rowhammer attacks as a short-term solution. Kim et al. suggest to use probabilistic adjacent row activation (PARA) to mitigate rowhammer attacks. As the name suggests, reading from a row will trigger an activation of adjacent rows with a low probability. During the attack, the malicious rows are activated many times. Hence, with high probability the victim row gets refreshed (stabilized) during the attack. The main advantage of this approach is its low performance overhead. However, it requires changes to the memory controller. Thus, PARA is not suited to protect legacy systems.

To the best of our knowledge Aweke et al. [3] proposed the only other software-based mitigation against rowhammer. Their mitigation, coined ANVIL, uses performance counters to detect high cache-eviction rates which serves as an indicator of rowhammer attacks [3]. However, this defense strategy has three disadvantages: (1) it requires the CPU to feature performance counters. In contrast, our defenses do not rely on any special hardware features. (2) ANVIL’s worst case run-time overhead for SPEC CPU2006 is 8%, whereas our worst case overhead is 0.29% (see Table III). (3) ANVIL is a heuristic-based approach. Hence, it naturally suffers from false positives (although the FP rate is below 1% on average). In contrast, we provide deterministic approaches that are guaranteed to stop rowhammer attacks.

X. Conclusion

Rowhammer is a hardware fault, triggered by software, allowing the attacker to flip bits in physical memory and undermine CPU-enforced memory access control. Recently, researchers have demonstrated the power and consequences of rowhammer attacks by breaking the isolation between virtual machines, user and kernel mode, and even enabling traditional memory-corruption attacks in the browser.

In this paper we introduce two practical and effective defenses against rowhammer, B-CATT and G-CATT. B-CATT extends the bootloader to blacklist vulnerable memory which completely prevents the attacker from inducing bit flips through rowhammer. G-CATT, on the other hand, is a generic mitigation that tolerates rowhammer attacks by dividing the physical memory into security domains, and limiting rowhammer-induced bit flips to the attacker-controlled security domain.

Our detailed evaluation of B-CATT and G-CATT verifies that both schemes prevent all known rowhammer attacks. Further, our mitigation schemes do not affect the run-time performance or the stability of the system.

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