The Effect of Coupling Memory and Block Length on Spatially Coupled Serially Concatenated Codes

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Abstract—Spatially coupled serially concatenated codes (SC-SCCs) are a class of spatially coupled turbo-like codes, which have a close-to-capacity performance and low error floor. In this paper we investigate the impact of coupling memory, block length, decoding window size, and number of iterations on the performance, complexity, and latency of SC-SCCs. Several design tradeoffs are presented to see the relation between these parameters in a wide range. Also, our analysis provides design guidelines for SC-SCCs in different scenarios to make the code design independent of block length. As a result, block length and coupling memory can be exchanged flexibly without changing the latency and complexity. Also, we observe that the performance of SC-SCCs is improved with respect to the uncoupled ensembles for a fixed latency and complexity.

I. INTRODUCTION

It has been shown that spatial coupling improves the decoding threshold of low-density parity-check (LDPC) codes [1]. More specifically, the threshold of an iterative belief propagation (BP) decoder saturates to the threshold of the optimal maximum-a-posteriori (MAP) decoder [2], [3]. The concept of spatial coupling has been extended to turbo-like codes in [4], where it has been proven that threshold saturation also occurs for this class of codes. The decoding of spatially coupled codes can be done efficiently using window decoding [5]–[7]. An information-coupled version of the turbo codes from the LTE standard was proposed in [8]. On the other hand, it has been demonstrated in [9] that spatial coupling leads to a new tradeoff between error floor and waterfall performance of turbo-like codes. As a result, with spatial coupling, serially concatenated codes (SCCs) achieve better performance than parallel concatenated codes (PCCs) in both the waterfall and the error floor regions [9]. For this reason, spatially coupled serially concatenated codes (SC-SCCs) are selected as the focus of this paper.

From the analysis in [4] it can be seen that the decoding thresholds can be improved by increasing the coupling memory. But since the required size of the decoding window increases with the coupling memory, this option may not look appealing from a latency perspective. In this paper, we take another approach and propose some design criteria that allow us to increase the coupling memory without increasing latency or complexity and without any performance loss. To this end, we investigate the effect of block size, coupling memory, window size, and number of iterations on the performance,

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named as $q_t^0, q_t^1, \ldots, q_t^m$. This implies that $m+1$ should be smaller than $2K$ and also divide $2K$. The first subsequence, $q_t^0$, is used to generate the input of the current inner encoder at time $t$ and the other ones, $q_t^1, \ldots, q_t^m$, will be used in the next inner encoders at times $t+1, \ldots, t+m$, respectively. Thus, at time $t$, the sequence $(q_t^0, q_{t-1}^0, \ldots, q_{t-m}^0)$, which is generated by the current and previous $m$ outer encoders is permuted by Interleaver 2 and sent to the inner encoder to produce the parity sequence $p_t^I$. Finally, the output of the SC-SCC encoder at time $t$ is $v_t = (u_t, p_t^O, p_t^I)$. In this paper, a code rate of $1/3$ is considered. Therefore, the output of the inner encoder, $p_t^I$, is punctured such that only half of it, i.e. $K$ bits, is transmitted.

Similar to protograph-based LDPC codes, we can describe turbo-like codes by compact graphs [9]. The compact graph representation of SCCs is shown in Fig. 1(b), where the input and parity sequences are shown by black circles and referred to as variable nodes. Also, the outer and inner code trellises are represented by squares, which are referred to as factor nodes and labeled by the corresponding trellis lengths.

The corresponding compact graph representation of an SC-SCC with coupling memory $m = 1$ is shown in Fig. 3. The double circles are referred to as state variable nodes, which transfer the encoder state at time $t$ to the encoder at time $t+1$. As a result, our scheme performs the encoding continuously without termination. The reason behind this strategy is described in Section III-B. In a similar way, the compact graph of an SC-SCC with larger $m$ can be obtained.

C. SC-SCC Window Decoder

Analogously to LDPC codes, the nodes in an iterative message passing decoder exchange log-likelihood ratios (LLRs) along the edges in the graph (see Fig. 3). The inner and outer trellises are decoded using the Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm. Let us consider a decoding window of size $W$ blocks, which starts at time $t$ and ends at $t+W-1$, as shown by a solid rectangle in Fig. 3. Among these blocks, the first one to be decoded is referred to as the target block, which is located at the leftmost side of the window.

For all blocks with index $t' = t, \ldots, t+W-1$, first the inner and then the outer decoder perform $I_W$ decoding iterations as follows. In each iteration, the inner decoder receives three sequences: the channel LLR values $L_{ch}(u_{t'})$ and $L_{ch}(p_{t'}^O)$, and the a-priori LLR values $L_a(p_{t'}^I)$, which are obtained based on the previous extrinsic LLRs of the corresponding outer decoder, $L_e(p_{t'}^I)$. The inner decoder produces the extrinsic LLRs, $L_e(p_{t'}^I)$, and sends them back to the outer decoder. Then, similarly, the outer decoder receives the channel LLR values $L_{ch}(u_{t'})$ and $L_{ch}(p_{t'}^O)$, and the a-priori LLRs, $L_a(p_{t'}^O)$, which are computed based on the previous extrinsic LLRs of the corresponding inner decoder, $L_e(p_{t'}^I)$. The outer decoder produces the extrinsic LLRs, $L_e(p_{t'}^O)$, and sends them back to the inner decoder. After $I_W$ iterations, the decoding of the target block, $u_t$, is finished and the window is moved by one block. The same process is done for the next window, i.e. the latent memory in Fig. 3 to decode the target block $u_{t+1}$.

**Definitions:** The strength of spatially coupled codes depends on the constraint length, which is defined as

$$C = K \cdot (m+1), \quad m < W, 2K. \quad (1)$$

Also, the structural latency [10], [11] is represented as

$$L = W \cdot K, \quad \text{(bit)} \quad (2)$$

which for simplicity we call latency in the rest of the paper.

III. DESIGN GUIDELINES FOR FLEXIBLE CHOICE OF BLOCK SIZE AND COUPLING MEMORY

A. Using Higher Coupling Memory in a Fixed Latency

A window decoder will perform very poorly if the window size, $W$, is smaller than $m+1$. Thus, if a higher coupling memory is needed, $W$ should be increased, which considerably increases the latency as stated in (2). To solve this problem, we propose to reduce the block length, $K$, and increase the number of blocks per window, $W$, simultaneously. As a result, a higher coupling memory can be used without changing the latency.

Fig. 4 shows an example of an SC-SCC scheme with a coupling memory $m=1$. Two decoding windows with $W=4$ blocks are shown.
imply that the coupling memory cannot be larger than $m = 3$. On the other hand, the same latency is achieved in Fig. 4(b) by reducing the block length to $K = 512$ bits and doubling the window size while the coupling memory can be increased up to $m = 7$. Thus, depending on the block length, different window sizes should be considered to have a fixed latency and relax the limitation of the coupling memory. In Section IV-A we will show that in a fixed latency scenario, a higher coupling memory results in a better performance compared to a smaller one. However, there are some challenges to employ small blocks and large coupling memory, which are addressed in our scheme as follows.

**B. Continuous Encoding**

The classical way of encoding the SC-SCCs is to terminate the encoder after each block [2], i.e. encoder starts and ends in the zero state. The drawback of such schemes is a significant rate loss for small block lengths, $K$. One of the contributions of this paper is to perform continuous encoding without termination after each block to avoid the rate loss specially for the small $K$. For this purpose, after encoding of the block at time $t$, the encoder state is passed to the encoder of the block at time $t+1$. Thus, the last state of the encoder at time $t$ is used as the starting state of the encoder at time $t+1$. To represent this concept, we have added the *state variable nodes* to the SC-SCC graph, as shown by double circles in Fig. 3.

**C. Performance Improvement of Boundaries**

The traditional window decoding algorithm usually works in a block-wise basis [2] as shown in Fig. 5(a). Thus, at time instant $t$, the computation of $\alpha$ and $\beta$ are done in the forward and backward recursions for the block $u_t$. Then, the results at time $t$ are used in decoding of the next block, $u_{t+1}$. This method works properly for large block lengths, $K$. However, in case of small block lengths, running the BCJR for a very short trellis results in a poor performance at the boundaries between blocks. This is due to the unreliable states at the start and end of each trellis. Thus, the bits which are close to the boundaries will have a weak protection. To some extent this problem can be resolved by doing more iterations, but the computational complexity will be increased significantly.

To address this challenge, we propose to perform the decoding over the whole window at once. As shown in Fig. 5(b), the $\alpha$ computation is done in the forward recursion over the whole window at once and then $\beta$ is computed in the backward recursion. Thus, regardless of the value of block length, $K$, and window size, $W$, in our scheme the BCJR algorithm is run one time per iteration over the whole window instead of $W$ times per iteration. As a result, the presented decoding scheme will be independent of the block length and window size. Also, since the trellis length becomes large the boundary states are more reliable, which can improve the performance especially for small block lengths.

**D. Fixed Complexity**

Since, the trellis length of the inner decoder is twice the one of outer decoder, we define $2O_D$ and $O_D$ as the complexity of the inner and outer decoders. Due to the overlaps between the successive windows, shown in Fig. 4 each block is processed $W \cdot I_W$ times, where $I_W$ is the number of iterations per window position. Thus, the computational complexity per bit is

$$O_{bit} = \frac{W \cdot (3O_D) \cdot I_W}{K} = \frac{3O_D \cdot I_{eff}}{K},$$

which is proportional to the effective number of iterations $I_{eff} = W \cdot I_W$, since $O_D$ is proportional to $K$. Consequently, if the same $I_W$ is used for both cases in Fig. 4(a) and (b), the scenario in Fig. 4(b) will have higher complexity than the one in Fig. 4(a), which is due to the larger $W$ and amount of overlaps between successive windows.

Here, $I_{eff}$ specifies how often the BCJR is run to decode a certain block. The goal is to adjust the $I_W$ such that the same $I_{eff}$ is achieved for all scenarios, which results in the same complexity per bit. This enables us to perform a fair comparison between different SC-SCC scenarios regardless of their block length, window size, and latency. For example, to have the same complexity in both scenarios in Fig. 4 the $I_W$ in the second scenario, Fig. 4(b), should be set to

$$I_{W2} = \frac{W_1 \cdot I_{W1}}{W_2},$$

where $W_1$ and $I_{W1}$ are corresponding to the case in Fig. 4(a). It can be seen that less iterations per window, $I_W$, are used for smaller blocks. Also, it is important to point out that from a complexity perspective, both cases in Fig. 4 are the same and it does not matter to run a long BCJR or several short ones.

It is worth to mention that the computational complexity is not the only comparison metric that should be taken into account. There are other costs like the size of required memory and routing, which contribute to the hardware cost. However, these implementation issues are mainly related to the hardware architecture, which is not in the scope of this paper.

**IV. PERFORMANCE EVALUATION**

We have investigated the effect of code properties (e.g. $K$, $m$) and also the decoding parameters (e.g. $W$, $I_{eff}$) on the performance and complexity of SC-SCCs. To this end,
A. Effect of Coupling Memory on the Performance

We have investigated the effect of coupling memory, $m$, on the performance of SC-SCCs. The goal is to fix the window size, $W$, and block length, $K$, and then find the value of coupling memory, $m$, which leads to the best performance. As an example, this concept is investigated for three cases: \{\mathcal{L} = 1024, K = 32, W = 32\}, \{\mathcal{L} = 8192, K = 512, W = 16\}, and \{\mathcal{L} = 8192, K = 64, W = 128\} and the corresponding results are depicted in Fig. 6(a)-(c). As a result, by increasing the coupling memory up to $m = W/2 - 1$ the performance will be improved considerably (i.e. 0.2 dB to 1.1 dB). Also, the error floor goes down to the lower BERs and the waterfall performance becomes better. But, if $m > W/2 - 1$ the performance will be degraded, as shown with dotted curves in Fig. 6. This is due to the fact that in such a case we cannot see even one constraint length, $C$, inside the window (see Fig. 3) and therefore the performance of the decoder cannot fully exploit the code. Thus, for a given $K$ and $W$ the coupling memory of $m = W/2 - 1$ results in the best performance in such a setup. It is worth to mention that this performance improvement is achieved without compromising the latency and complexity.

B. Shorter Block Length with Higher Coupling Memory

As mentioned in Section IV-A, the coupling memory of $m = W/2 - 1$ leads to the best performance for the given $K$ and $W$. This choice of coupling memory results in the constraint length of $C = K \cdot (m + 1) = K \cdot W/2$, which can be achieved by either a small $K$ and large $m$ or a large $K$ and small $m$ while the latency remains fixed ($\mathcal{L} = 2C$). For example, \{$K = 256, W = 4, m = 1$\} and \{$K = 64, W = 16, m = 7$\} achieve the same latency of $\mathcal{L} = 1024$ bits and constraint length of $C = 512$ as shown in Table 1.

It is expected to achieve better performance for the scenarios, which have the same constraint length. We have investigated this concept for the five scenarios in Table 1 and the simulation results are shown in Fig. 7(a)-(e). In each scenario the latency and constraint length are fixed while the complexity is the same for all of them by considering $I_{eff} = 80$. Simulation results show that, for a certain latency and constraint length, selecting a small block length, $K$, and large coupling memory, $m$, can lead to a better performance compared to a large block length and small coupling memory. This performance improvement can be seen in both waterfall and error floor regions in Fig. 7.

As a result, our analysis reveals the flexibility of SC-SCCs such that for a given latency and constraint length, it is possible to make the block length smaller and use higher coupling memory while we get the same or even better performance compared to the larger $K$. It is worth to mention that, in case of very small $K$ the performance degrades and an error floor appears at high BERs, which are shown by the dashed curves in Fig. 7(a)-(e). This is mainly due to the fact that in our scheme, we have employed independent random interleavers to show how the performance changes for different block lengths. But, in case of very small $K$ the short-length random interleavers are not efficient. In such cases, the interleavers should not be designed independently. Moreover, since we want to have the same complexity for different block lengths,

\begin{table}[h]
\centering
\caption{Different Scenarios of SC-SCCs with the Same Latency (\mathcal{L}), Constraint Length (\mathcal{C}), and Computational Complexity.}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
\mathcal{L} & K & m & I_{eff} & W/2 & \mathcal{C} & \mathcal{L} \\
\hline
16384 & 4096 & 4 & 20 & 128 & 64 & 128 \\
1024 & 2048 & 6 & 20 & 128 & 64 & 128 \\
512 & 1024 & 8 & 20 & 128 & 64 & 128 \\
\hline
8192 & 2048 & 2 & 20 & 128 & 64 & 128 \\
4096 & 1024 & 4 & 20 & 128 & 64 & 128 \\
2048 & 1024 & 6 & 20 & 128 & 64 & 128 \\
\hline
\end{tabular}
\end{table}

1We have picked a set of pseudo-random interleavers and fixed them for all the code sequences through the simulations.

2We plan to investigate a joint interleaver design for small block lengths, $K$, in our future research.
$I_W$ would be very low (e.g. $I_W = 1, 2, 3$ in Table I) for the very small $K$, which degrades the performance. Note that a small or large block length is relative to the latency. For example, $K = 128$ is considered as a large $K$ in case of $L = 1024$, while it is a small $K$ for $L = 8192$.

C. Performance Comparison with Uncoupled Codes

Fig. 8 shows the performance comparison between the presented SC-SCC scheme and the uncoupled ensembles, SCC, for different latencies, $L$, and block lengths, $K$. To have a fair comparison, the same complexity is considered for both SC-SCC and SCC regardless of $L$ and $K$ as described in Section III-D. It can be seen that spatial coupling significantly improves the performance of the SCC and makes it much closer to the capacity. Having considered the same interleaver size (i.e. fixed block length, $K$) the SC-SCC achieves around 1 dB better performance than the corresponding SCC scheme with the same $K$. Also, in case of equal latency, the SC-SCC scheme still achieves around 0.5 dB better performance than the SCC at the BER of $10^{-4}$. The latency of an SCC is $L = K$. Moreover, Fig. 8 shows that the performance improvement resulting from increasing the latency is more pronounced in SC-SCCs than SCCs. More specifically by increasing the latency from $L = 1024$ to $L = 32768$ bits, 0.7 dB and 1.1 dB performance improvement is achieved in SCC and SC-SCC, respectively.

It is worthwhile to mention that, even with lower latency, the SC-SCC can achieve even better performance than the SCC scheme. For example, as shown in Fig. 8 the SC-SCC with $L = 8192$ has better performance than the SCC with $L = 32768, 16384$. This means that by just increasing the latency and block length the SCC cannot achieve better performance than the SC-SCC, which is due to the threshold improvement resulting from spatial coupling. Moreover, asymptotic decoding thresholds of the SCC and SC-SCC ensembles for the AWGN channel are depicted using vertical lines in Fig. 8. These values are computed using the erasure channel prediction method introduced in [12].

V. Design Tradeoffs

So far we assumed fixed latency and complexity in the evaluations. Now we are interested to see the performance gain of SC-SCCs if we increase the latency or the complexity.

A. Performance-Latency Tradeoff

As mentioned in Section IV-A, for a given latency, $L$, and complexity, the performance can be improved by increasing the constraint length $C$, i.e., larger $m$ or $K$. Now, we want to see if for a given constraint length and complexity, it is possible to improve the performance by increasing the latency? More specifically, having considered a fixed $K$ and $m$, how does the performance change if we make the window size, $W$, larger? We have investigated this concept and the results are shown in Fig. 9. For a given constraint length and complexity, if we only change the window size (e.g. doubling $W$) we will not gain too much in performance while the latency is increased (e.g. twice latency). So, if the targeted application can tolerate the higher latencies, it is better to increase the coupling memory, $m$, as well to make the code stronger rather than just increasing the window size, $W$. As a result, this strategy provides the effective use of a certain latency to achieve better performance. It is worth to mention that, the larger window size enables us to employ a higher coupling memory. This is due to the limitations on the coupling memory, i.e. $m \leq W/2 - 1$, as described in Section IV-B.

Fig. 10 shows the tradeoff between latency and performance for the scenarios in Table I. In each scenario the latency,
K and \( K_{eff} \) in Table I. The same computational complexity is considered for all scenarios (\( I_{eff} = 80 \)).

The required \( E_b/N_0 \) to achieve BER of \( 10^{-5} \) is shown in x-axis. The listed values of \( K \) in the legend are corresponding to the markers from left to right. The same computational complexity is considered for all scenarios (\( I_{eff} = 80 \)).

\( L \), and constraint length, \( C \), are fixed and the complexity is the same for all scenarios. In this figure, x-axis shows the required \( E_b/N_0 \) to achieve the BER of \( 10^{-5} \) in all scenarios. The markers, which tend to the lower left corner of Fig. 10, are corresponding to the scenarios with a low latency, \( L \), and good performance. Thus, by considering this tradeoff the proper values of \( W \), \( K \), and \( m \) can be obtained.

**B. Performance-Complexity Tradeoff**

It is worthwhile to see the effect of number of iterations on the performance: how will the performance be improved if we would spend more complexity? We have considered different effective number of iterations, \( I_{eff} \), for the SC-SCC scheme in case of \( L = 4096 \) and \( L = 16384 \) bits latencies. The corresponding simulation results are shown in Fig. 11(a) and (b), respectively. Simulation results show that the performance improvement resulting from a higher effective number of iterations, \( I_{eff} \), is more pronounced in the high latency, \( L \), scenarios than the low latency scenarios. Also, it can be seen that by spending more complexity the error floor goes down and it happens at a much lower BER.

**VI. Conclusion**

We have investigated the effect of coupling memory, block length, window size, and number of iterations on the performance, complexity, and latency of SC-SCCs. Our approach provides the flexibility to exchange the block size with the coupling memory, which makes the code design independent of the block length. We have demonstrated that how the higher coupling memory can be used without increasing the latency and complexity. Moreover, we have shown that SC-SCCs can achieve better performance than the uncoupled ensembles with the same latency and complexity.

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