Simulation of Different Third Harmonic Injected PWM Strategies for 5-Level Diode-Clamped Multilevel Inverter

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Abstract: Multilevel Inverters (MLI) have widespread use in industrial drive applications, HVDC transmission with Uninterruptable Power Supply systems. They also have applications in the stand-alone and the grid connected renewable energy systems. Multi-level Inverters also find optimum application in Stand-alone and Grid-connected Systems. Majority of losses i.e. switching losses are considered with constrained device rating, the traditional two-level inverters face limits especially when operating at high frequency. The solution which is optimum and appropriate by many power quality researchers is the use of MLIs. Among various MLI topologies the Diode-Clamped Multilevel Inverter (DCMLI) give a promising solution as they can give better voltage performance for different switching frequencies and an improved total harmonic distortion (THD) profile without the use of filter. To meet the voltage and frequency requirement various modulation techniques are applied to MLIs. The additional switching states created by these topologies provide greater flexibility to control more circuit breakers. This paper presents the comparison of a 5-level DCMLIs with several modulation schemes. The simulation results are discussed in detail and the comparison table is presented in terms of Output voltage and THD.

Index Terms: MLI (Multi-Level Inverter), THD (Total Harmonic Distortion), DCMLI (Diode-Clamped Multi Level Inverter).

1. Introduction

Various topologies of inverters i.e. DC-AC converters are in the literature [1]. The main aim of the inverter is the conversion along with compliance of the international standards so that it could be adopted for commercial applications. The concept of multilevel converters either for rectification or inverter operation is required for gain significance over past two decades due to the improved power quality, capability of voltage, switching losses to be minimum and better electromagnetic compatibility. They are mainly applicable for applications where voltage is high, power is high due their advantages with synthetization of better waveform with less harmonics to achieve high voltages with less maximum power ratings of the switches. They also reduce the dv/dt stress and hence protect the motor winding insulation.

As per literature survey, the MLIs has been introduced in 1975 as another solution of medium voltage and high-power applications. With the latest technology, many industrial applications demand high power applications almost megawatts range along with medium or low power utilities [2][3]. Use
of a high-power source in industrial loads can be required for high-power machines but it may damage the other loads. In small and medium scale industries require medium voltage viable speed drive applications. The inverter is the integral part in many applications such as air conditioning, Solar PV (photovoltaic) power systems etc.

Specific to the application of distributed power generation like PV, with the basic function of converter for inverting operation like DC-AC conversion, it should also be assured by output power quality. It should have flexible protection scheme as well as system controls. The requirements of such inverters are high efficiency and reliability, good tolerance on a wide range of input variations and low cost. This has driven more research in the inverters leading to solutions such as simpler topologies, lower switching components, better modular designs while fulfilling the primary quality requirements. It has become obvious that instead of connecting a dingle power semiconductor switch, use of these modular inverters has gained much more importance. This helps in easy maintenance and at the same time meets the power demand at high voltages as discussed earlier [3].

From the different multi-level inverters, three-level inverter is considered in [4]. Output voltage has more steps or levels in the increasing voltage as a stepwise type for minimizing total harmonic distortion than the conventional two-level inverter. However, as the number of levels increase there arise problems such as voltage imbalances and increase the control complexity in terms of switching.

By considering Single-phase w.r.t. no. of levels used or adopted per phase as shown in FIGURE 1 with no. of switches. For better understanding each power semiconductor switch is shown by an ideal multi position switch. It can be seen from FIGURE 1(a) that multi-level inverter has step by step levels (values) by considering neutral terminal by the passive element, whereas step by step levels which has an intermediate level to create levels as shown in FIGURE 1(b) and further levels as shown in FIGURE 1(c).

The no. of levels of the output voltage are considered with respect to negative or neutral terminal of the converter when acting as an inverter. The no. of steps considered as ‘K’ and is assumed between the lines and connected in shunt when load is connected. Where m is the no.of steps used in MLI.

\[ K = 2m+1 \]  
\[ P = 2K-1 \]

2. Types of Multi Level Inverters

From literature survey, among various topologies that have been proposed, the main three different topologies that has large impact identified as follows [4]-[9].

- Clamped MLI: Neutral Point or Diode
- Flying Capacitor or Clamped with Capacitor MLI
Interconnected with many cells with isolated inputs which are based on direct current or voltage (Cascaded H-Bride) MLI

These are the classic topologies shown in FIGURE 2 with several new configurations with some modifications with these topologies.

![Multilevel Inverters Classification](image)

**FIGURE 2: Multilevel Inverters Classification**

Based on the application of the inverter and its topology and switching frequency, numerous variants of the above modulation techniques have been adopted. Each of them has its own advantages and disadvantages. FIGURE 3 gives the classification of such modulation schemes based on switching frequency for MLIs operation. The switching frequency with respect to high power applications are normally referred in the order of one to many kHz.

Also, for various switching requirements analysis has been done in different modulation techniques and with strategies that can be adopted for these MLIs. Among all of them are listed below.

- SHE (Harmonic Elimination with Selective frequencies)
- SPWM (Pulse Width Modulation with Sinusoidal)
- SVM (Space Vector Modulation)

Pulse Width Modulation with Sinusoidal wave (SPWM): Considering carrier-based method which involves comparing a reference signal(sinusoidal) with a carrier signal(triangular) which has signals that are horizontally and vertically changing to minimize the harmonic content.

Harmonic Elimination with Selective frequencies (SHE): In this type the lower or minimal order frequencies are removed or eliminated from the total frequencies and Fourier analysis is adopted. This eliminates the undesired lower order harmonics which indirectly minimizes the cost of filtering equipment.

Space Vector Modulation (SVM): This method is also a PWM method, but the time is calculated for the switch non-operating region which is represented in the form of space vectors for three-phase from a reference point. The advantage of this method is the inverter is switched off rather than provide a switching that goes to neutral reference temporarily for creating neutral voltage.

One more method, with different series, parallel and series-parallel connections in modulation with the one operating with minimum and maximum switching frequencies. Generally adopted in Cascaded H Bridge inverters with asymmetric configuration which minimize breakdown losses obtained in high-level switches with upper units of power.
3. Diode-Clamped Multi Level Inverters

With respect to the practical applicability, the DCMLI or NPC inverter is first MLI. This topology uses diode as a switching of the switches for increasing or decreasing of DC voltage to obtain desired output voltage levels. They are utilized to control the power semiconductor voltage. \( V_{dc} \) is the voltage across switch or capacitor. With the stepwise size ‘k’ is considered as no. of levels of inverter has ‘k-1’ capacitors or DC sources, ‘2(k-1)’ switches (IGBT/MOSFET) and ‘(k-1) *(k-2)’ blocking diodes. Considering the number of levels with the increase in the number of levels of output voltage with sinusoidal input thereby reducing the harmonic content.

**Principle of Operation and Switching sequence of 5-level Multi Level Inverter - Diode Clamped**

DC MLI with five levels has 4 capacitors, each of value \( V_{dc}/4 \). There are eight Power semiconductor switches. For the multi-level inverter with five levels of output voltage across phase will have multi levels, \( \pm V_{dc}/2, \pm V_{dc}/4 \) and 0. One phase/leg of a three phase five-level DCMLI is shown in FIGURE 4. Switching sequence of the switches is included in the Table 1. An entry High in the row denotes that the switch associated with levels include ON/OFF or 0/1 for that output voltage level. An entry Low in the row of the table denotes the Switch is OFF/LOW/0 for that voltage level.

For any output voltage level, we have only four switches conducive at the same time and remaining four switches are OFF.

![FIGURE 4: Single-phase 5-level DCMLI](image-url)
The DCMLI provides several voltage levels by connecting the phases to several passive elements. Based on the no. of levels, the passive elements like capacitors are added either in series or parallel. As discussed in the earlier section, there are two capacitors connected via a DC bus which gives three levels in MLI topology. This extra level was because of DC bus neutral point. Even though a neutral point includes a pair with levels of output voltage which is never available, sometimes Multiple Point Clamped (MPC) is used. Capacitor voltage with balance problems are considered with diode inverter is limited in industrial applications. Multi-level Inverter with Diode Clamped Applications are:

- Drives with flexible speed control.
- Compensation with static var
- System interconnections with High voltage
- Transmission lines with High voltage AC and DC

4. Modelling Schemes and Simulation Results

The 5-level DCMLI was modeled, and its performance is studied using the MATLAB_SIMULINK environment. Different PWM methods such as VAPDPWM (Variable Amplitude Phase Disposition PWM), PDPWM (Phase Disposition PWM), POPWM (Phase Opposition Disposition PWM), VFPWM (Variable frequency PWM), Carrier Overlapping PWM-A scheme(COPWM-A) and Carrier Overlapping PWM-B scheme(COPWM-B) schemes are simulated and analyzed. The system is tested for different modulations varies within 0.6 to 1 with their supporting harmonic level values seen by considering Fast Fourier analysis. The measurements of the FFT block show the output voltage in line to line of the inverter in terms of RMS voltage of the inverter in terms of phase value with ‘M’ as modulation index. Simulation analysis can be concluded, the PDPWM strategy produces energies of the 65th, 70th, 76th, 80th and 84th harmonics. VAPDPWM produces the energies of the 10th, 15th, 75th, 80th, 85th, 100th, 150th, 160th and 180th harmonics.

The PODPWM methods generates the energy of 10th, 80th and 160th harmonics. The VFPWM generates the energies of the 11th, 13th and 16th harmonics. COPWM-A produces 3rd, 78th and 84th harmonics. COPWM-B produces the 3rd, 65th, 77th and 169th harmonics. The modulation index is 0.8 and number of samples is 40. The output line voltage waveform, THD and output phase voltage and its frequency spectrum for 5-level inverter for various PWM schemes with a frequency with a cut-off value 1 kHz as mentioned in Figure 5 to Figure 21.

The harmonic content and disconnection losses estimated with carrier frequency varies by the range of 1500 Hz to 10000 Hz. It is noted that with the increase of no. of levels in MLI, the performance of the system is controlled and minimized by switching losses and overall harmonic distortion. Line starting time is 0.0109 secs. The secondary voltage across phase is 0.02 V with 50 Hz as frequency reference.
1) **Phase Disposition PWM Scheme (PDPWM):**

![Figure 5: Line voltage Versus Time (secs)](image1)

![Figure 6: Total harmonic distortion versus Harmonic order](image2)

**FIGURE 7:** Output phase voltage generated by PDPWM schemes

2) **Variable Amplitude Phase Disposition PWM Scheme (VAPDPWM):**

![Figure 8: Output Line Generated by VAPDPWM Schemes](image3)

![Figure 9: Output Phase Voltage Generated by VAPDPWM Schemes](image4)

**FIGURE 8:** Output Line Generated by VAPDPWM Schemes

**FIGURE 9:** Output Phase Voltage Generated by VAPDPWM Schemes

3) **Phase Opposition Disposition Scheme (PODPWM)**

![Figure 10. Output line voltage generated by PODPWM schemes](image5)

![Figure 11: FFT spectrums for PODPWM schemes.](image6)

**FIGURE 10:** Output line voltage generated by PODPWM schemes

**FIGURE 11:** FFT spectrums for PODPWM schemes.
4) **Variable Frequency PWM Scheme (VFPWM)**

![FIGURE 13: Output line voltage generated by VFPWM](image1)

![FIGURE 14: FFT spectrums for VFPWM schemes](image2)

**FIGURE 15:** Output phase voltage by VFPWM schemes

5) **CARRIER OVERLAPPING PWM-A SCHEME**

![FIGURE 16: Output line voltage generated by COPWM-A](image3)

![FIGURE 17: FFT spectrums for COPWM-A schemes](image4)
5. CONCLUSIONS

It concluded from the simulation analysis that the power quality issues related to convention two level inverters can be solved using MLIs. The simulation is done for a three phase 5-level DCMLI with various modulation strategies such as PDPWM, VAPDPWM, PODPWM, VFPWM, COPWM-A, COPWM-B. The THD content in these various schemes differ with ±5% for the same modulation index. Based on the control strategy that can be used and the application one of them can be selected appropriately.

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