Quantum circuits which perform integer arithmetic could potentially outperform their classical counterparts. In this paper, a quantum circuit is considered which performs a specific computational pattern on classically represented integers to accelerate the computation. Such a hybrid circuit could be embedded in a conventional computer architecture as a quantum device or accelerator. In particular, a quantum multiply-add circuit (QMAC) using a Quantum Fourier Transform (QFT) is proposed which can perform the calculation on conventional integers faster than its conventional counterpart. Whereas classically applying a multiply-adder (MAC) \( n \) times to \( k \) bit integers would require \( O(n \log k) \) parallel steps, the hybrid QMAC needs only \( O(n + k) \) steps for the exact result and \( O(n + \log k) \) steps for an approximate result.

*Keywords*: quantum circuits, quantum arithmetics, multiply-add

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## 1 Introduction

Quantum computing has the potential to dramatically change the nature of computing, but has mostly been a theoretical subject partly due to the difficulties in building physical quantum circuits. However, recent progress has enabled the first, albeit small, quantum devices to be constructed, see for example [1] utilising photonics. These devices are not complete quantum computers, but consist of simple quantum circuits capable of processing information to solve specific problems. Critically, these devices can be fabricated in silicon which could lead to their integration with conventional microelectronics. How would such a hybrid of conventional and quantum microprocessor be used? Co-processor architectures have been developed in the past but perhaps the most promising context would be to consider the quantum device as an accelerator.

There are several examples of modern heterogeneous computer architectures. For exam-
ple, Graphical Processing Units (GPUs) have been used extensively in the field of scientific numerical computing to accelerate specific aspects of these calculations, where some suitably defined compute kernel is offloaded from the CPU and executed faster on the GPU. Another analogy can be drawn with field programmable gate arrays (FPGAs) where particular computational patterns in software can be instantiated in hardware using the reprogrammable logic of these devices, see for example [2, 3]. Rather than accelerating an entire kernel as would be required for a GPU, a quantum device could be employed to accelerate a specific computational pattern. Moreover, as this device would function as an accelerator, a complete quantum computer would not be required. Furthermore, the effects of quantum decoherence which destroys quantum information can be mitigated because such quantum circuits need only to be in an entangled state for brief period.

The addition and multiplication of small integers are the simplest computational patterns. Here, the manipulation of \( n \) classically represented integers of size \( k \) bits by a quantum circuit is considered. A key consideration is the number of parallel steps it takes to execute a quantum circuit, i.e. the depth of the quantum circuit implementing the computation. The first quantum addition circuit was proposed by Vedral et. al. in 1995 [4]. It is a quantum version of the classical ripple carry adder. The quantum ripple carry adder has been further studied in the circuit model of quantum computing [6, 7, 8, 9] and in the Measurement Based Quantum Computing Model (MBQC) [10]. The quantum circuits implementing the classical carry-lookahead adder have been investigated in [11, 8, 12] and the MBQC design in [13].

Most of the quantum adders constructed are thus quantum versions of classical ripple carry or carry-lookahead adders. A notable exception is the addition circuit proposed by Draper in [14], which utilises the quantum Fourier transform (QFT) operation. Whilst this particular circuit performs no better than a classical carry-lookahead circuit, employing circuit features which are specific to quantum circuits rather than quantum analogues of classical circuits may allow performance gains to be achieved.

Quantum arithmetic circuits for integer multiplication have been proposed in [15, 16], but this is the first work studying the multiply-add operation in the quantum setting. Although quantum arithmetic logic units (ALUs) have been proposed in several papers [17, 18, 19, 20], none of them analyse if the addition and multiplication could be merged into a single, more efficient multiply-add operation.

In this work, the QFT, highly entangled quantum states obtained through "fanning-out" [21] of the QFT states, and the classical properties of a hybrid circuit are combined together to produce a QFT multiply-add circuit (QMAC) for classical integers which outperforms a conventional multiply-add unit.

The rest of the paper is organised as follows: In Section 2 the QMAC is described. In Section 3 the depth of the circuit is analysed and compared to a conventional multiply-add circuit. Finally, in Section 4 the results are presented.

2 The QFT Multiply-Add Circuit

Consider a unitary operator, \( M \), which when combined with the QFT can be used to compute the action of a classical integer MAC: \( z + y \cdot x \), where \( z, y, x \in \mathbb{Z} \). This operator is then decomposed into single qubit gates. The decomposition shown is particularly useful, since it

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*see for example [5] for a textbook on circuit design*
allows for the construction of a parallel hybrid circuit which is presented at the end of this section. For the sake of notational simplicity, only unsigned integers are considered but the presented circuits can work with signed integers if the two’s complement representation is used.

Let \( z_k \cdots z_2 z_1 \) be the binary representation of a \( k \) bit integer \( z \) such that \( z = z_k 2^{k-1} + \cdots + z_2 2^1 + z_1 2^0 \) and \( 0.z_k \cdots z_2 z_1 \) the binary fraction \( z_k/2^1 + \cdots + z_2/2^{k-1} + z_1/2^k \). Then the QFT of a \( k \) qubit computational basis state \( |z\rangle \) can be written as [22]:

\[
QFT|z\rangle = \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i 0.1z_1}|1\rangle) \\
\otimes \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i 0.2z_2 z_1}|1\rangle) \\
\otimes \cdots \\
\otimes \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i 0.2^k z_k z_2 z_1}|1\rangle).
\]

Let \( M_j(y, x) \) be a single qubit unitary operator defined as follows:

\[
M_j(y, x)|0\rangle \rightarrow |0\rangle \\
M_j(y, x)|1\rangle \rightarrow e^{2\pi i 0.y_j \cdots y_1 \cdot x}|1\rangle,
\]

where \( x, y \in \mathbb{Z} \) are \( k \) bit integers. The effect of applying \( M_j(y, x) \) to a state which has the first \( j \) bits of a \( k \)-bit integer \( z \) encoded in its relative phase is

\[
M_j(y, x) \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i 0.z_j \cdots z_2 z_1}|1\rangle) = \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i (0.z_j \cdots z_2 z_1 + 0.y_j \cdots y_2 y_1 \cdot x)}|1\rangle).
\]

The above equation shows that the action of \( M_j(y, x) \) is similar to applying a MAC operator to the binary fraction encoded in the relative phase, i.e., it multiplies the binary fraction \( 0.y_j \cdots y_2 y_1 \) with \( x \) and adds it to \( 0.z_j \cdots z_2 z_1 \). The \( k \) qubit quantum operator \( M \) corresponding to a MAC is defined as

\[
M(y, x) = M_1(y, x) \otimes M_2(y, x) \otimes \cdots \otimes M_k(y, x).
\]

The application of \( M(y, x) \) to \( QFT|z\rangle \) will result in the state

\[
M(y, x)QFT|z\rangle = \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i (0.z_1 + 0.y_1 \cdot x)}|1\rangle) \\
\otimes \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i (0.z_1 z_2 + 0.y_2 y_1 \cdot x)}|1\rangle) \\
\otimes \cdots \\
\otimes \frac{1}{\sqrt{2}}(|0\rangle + e^{2\pi i (0.z_k \cdots z_2 z_1 + 0.y_k \cdots y_2 y_1 \cdot x)}|1\rangle) = QFT|z + y \cdot x\rangle.
\]

Applying the \( QFT^\dagger \) operator and measuring the result in the computational basis gives the output \( z + y \cdot x \), which would also be the effect of a classical MAC applied to \( x, y, z \). Note that since \( e^{2\pi i (m + 0.y \cdots y_2 z_1 z_1)} = e^{2\pi i 0.z_1 \cdots z_2 z_1} \) for every \( m \in \mathbb{Z}, z \in \{0, 1\}^k \), and \( l \in \{1, 2, \cdots, k\} \) the output is computed modulo \( k \).
Any realistic quantum device would have to be built using quantum gates acting on a limited number of qubits, thus the $M(y,x)$ operator needs to be decomposed into one- and two-qubit quantum gates. To obtain a performance that surpasses classical MACs the $M(y,x)$ operation will be constructed in a way that allows every gate in its circuit to be applied in one simultaneous step. The following gates are used in the circuit construction:

$$R_j = \begin{bmatrix} 1 & 0 \\ 0 & e^{2\pi i/2^j} \end{bmatrix}, \quad \text{CNOT} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix},$$

where $R_j$ is a phase shift gate and CNOT is the controlled NOT gate. Note that the operator $R_j$ has the following properties:

$$\forall j \in \mathbb{Z} < 1 \quad R_j = I \quad (8)$$

$$R_j^{2^m} = \begin{bmatrix} 1 & 0 \\ 0 & e^{2\pi i/2^{j-m}} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & e^{2\pi i/2^{-m}} \end{bmatrix} = R_{j-m}. \quad (9)$$

The $j$-qubit fan-out operator $F_j$ which maps $|a\rangle|b_1\rangle\cdots|b_{j-1}\rangle \rightarrow |a\rangle|b_1 \oplus a\rangle\cdots|b_{j-1} \oplus a\rangle$, where $b_i \oplus a = (b_i \oplus a) \bmod 2$ is also required. It is trivial to see that $F_j^T = F$. The operator $Q_j(y) = R_{y_1} R_{y_2} \cdots R_{y_j} R_1 y_j$ is used as a sub-circuit in the $M(y,x)$ construction. The effect of $Q_j(y)$ on the one qubit computational basis is:

$$|0\rangle \rightarrow |0\rangle \quad (10)$$

$$|1\rangle \rightarrow e^{2\pi i 0 \cdot y_1 \cdots y_j} |1\rangle. \quad (11)$$

Note that since $y_m$, where $m \in \{1, 2, \cdots, j\}$, is a binary value and $R_0 = R^0 = I$ for every $l \in \mathbb{Z}$, the operator $Q_j(y)$ can be written as follows:

$$Q_j(y) = R_{y_j} \cdots R_{y_2} R_{y_1}. \quad (12)$$

Furthermore, from the equalities $[8]$ and $[9]$ it follows that:

$$Q_j(y)^{2^m} = R_{y_j}^{2^m} \cdots R_{y_2}^{2^m} R_{y_1}^{2^m} = R_{y_j-m} \cdots R_{y_2-m} R_{y_1-m} = Q_{j-m}(y). \quad (13)$$

The above equation implies that $Q_{j-m} = I$ if $j - m < 1$, therefore the $M_j(y,x)$ operator can be written as:

$$M_j(y,x)|1\rangle = e^{2\pi i 0 \cdot y_1 \cdots y_l \cdot x} |1\rangle \quad (14)$$

$$= e^{2\pi i 0 \cdot y_1 \cdots y_l \cdot (x_1 2^0 + x_2 2^1 + \cdots + x_k 2^{k-1})} |1\rangle$$

$$= Q_j(y)^{x_k 2^{k-1}} \cdots Q_{j-1}(y)^{x_2 2} Q_j(y)^{x_1 2} |1\rangle$$

$$= Q_j(y)^{x_j} \cdots Q_{j-1}(y)^{x_2} Q_j(y)^{x_1} |1\rangle$$

$$M_j(y,x)|0\rangle = Q_1(y)^{x_j} \cdots Q_{j-1}(y)^{x_2} Q_j(y)^{x_1} |0\rangle = |0\rangle. \quad (15)$$
The decomposition of $M_j(y, x)$ into $Q_j(y)$ (Eq. 14 and 15) operators and $Q_j(y)$ into $R_j$ operators (Eq. 12) will be used to construct a parallel quantum circuit for $M(y, x)$. Note that the descriptions of $M(y, x)$, $M_j(y, x)$, and $Q_j(y)$ contain the arguments $x$ and $y$. This is undesired for practical implementations of a circuit, since a circuit cannot in general change depending on the input. In the design below, this problem is resolved by using the bits of the arguments as controls for quantum gates, i.e. the value of classical bits is used to determine if a particular quantum gate should be applied or not. First, the parallel hybrid circuit for $Q_j(y)$ is constructed. Since $R_j^0 = I$ and $R_j^1 = R_j$, the effect of a input bit $y_m$ in Eq. 12 where $m \in \{1, 2, \cdots, j\}$, is to control the application of the gate $R_{j+1-m}$. Thus the quantum circuit of $Q_j(y)$ can be constructed using only single qubit $R_j$ gates controlled by classical bits $y_m$. All of the $R_j$ gates in $Q_j(y)$ can be applied in parallel using auxiliary qubits and the $F_j$ gate. Thus the parallel hybrid circuit $F_jQ_jF_j$ of $Q_j(y)$ can be constructed as shown in Figure 1.

![Fig. 1. The parallel version of the operator $Q_j(y)$. The $F_j$ blocks can be applied in $O(\log j)$ steps. $|\psi\rangle$ is an arbitrary 1 qubit state. The dashed lines represent classical bits and the continuous lines qubits. A single line crossing a wire represents a single bit/qubit and three lines crossing a wire represent multiple bits/qubits.]

Since $Q_j(y)^0 = Q_j(0) = I$ and $x_j$ is a binary value, $M_j$ can be written as $M_j(y, x) = Q_1(y \cdot x_j) \cdots Q_{j-1}(y \cdot x_2)Q_j(y \cdot x_1)$. The values of both $y$ and $x$ are classical bit-strings, hence the operation $y \cdot x_j$ can be performed classically in one parallel computational step using an AND operator between $x_j$ and every bit of $y$. Since $M_j(y, x)$ can be decomposed into diagonal operators $Q_j(y)$, there exists a parallel hybrid circuit where all the $O_j(y)$ operators are applied simultaneously. In this circuit’s construction the parallel hybrid circuit $O_j$ is used as seen in Figure 2. Since $M(y, x)$ is a tensor product of the operators $M_j(y, x)$, where $j \in \{1, \cdots k\}$, the circuit of $M(y, x)$ can be created by simply applying an appropriate $M_j$ sub-circuit to each of the input qubits as shown in Figure 3. The circuit $FJM$ in the aforementioned figure corresponds to the operator $M(y, x)$ and together with the $QFT$ comprises the quantum MAC circuit.

3 Analysis of the Circuit

The main result of this work concerns the depth of the hybrid MAC circuit in the case of sequential application. When the circuit $FJM$ in Figure 3 is applied in repeatedly, then the only $F$ gates having a non-trivial effect will be at the beginning and the end of the computation. This is due to the fact that $FF = FF^\dagger = I$ and thus $(FJM)(FJM) = FJMF$. Combining the circuit in Figure 3 with the $QFT$ and using it to perform the
multiply-addition operation of $n$ integers results in the hybrid circuit depicted in Figure 4. As can be seen from the figure, the overall depth will depend on the depth of $M$, which according to the next lemma is constant.

**Lemma 1** The depth of the hybrid circuit $M$ is 2.

**Proof.** It can be seen from Figure 3 that the depth of the $M$ circuit has to be equal to the maximum depth of any $M_j$ sub-circuits, where $j \in \{1, \cdots, k\}$. It is apparent that by substituting the $Q_j$ circuits in $M_j$, shown in Figure 2 with the one described in Figure 1, a circuit with one layer of classical AND gates and one layer of single qubit $R_m$ gates can be constructed. Thus the combined depth of any $M_j$ and hence $M$, circuit is 2 □.

When determining the depth of a circuit, gates of variable size, such as the $F$ gate have to be decomposed into one- and two-qubit quantum gates. An $F_m$ gate can be written as an $O(\log m)$ depth circuit consisting of only $\text{CNOT}$ gates, where $m$ is the number of qubits $F_m$ acts upon. From Figure 3 it can be seen that the number of qubits $F$ acts upon, is equal to the number of qubits $M_n$ acts upon. This in turn is equal to the number of quantum gates in $M$ since by Lemma 1 there is only one layer of quantum gates. Thus the depth of the circuit in 4 it is given by the number of gates in $M$.

**Lemma 2** The size of the hybrid circuit $M$ is $O(k^3)$. 
Fig. 4. The hybrid quantum circuit computing the MAC operation \( n \) times in a sequence with multiplicand pairs \((x_1, y_1), \ldots, (x_n, y_n)\), where \( z, x_1, y_1 \in \mathbb{Z} \). Here \( z' = z + \sum_{i=1}^{n} x_i \cdot y_i. \)

Proof. Let \( \text{size}(C) \) be the size of a quantum circuit \( C \), i.e. the number of one- and two-qubit quantum gates in the decomposition of \( C \). Every \( M_j \) sub-circuit in \( M \) corresponds to one \( M_j(y, x) \) operator in the definition of \( M(y, x) \). Furthermore, every \( Q_l \) sub-circuit in \( M_j \) corresponds to a \( Q_l(y) \) operator in the definition of \( M_j(y, x) \) (Eq. 14 and 15) and each \( R_m \) gate in \( Q_l \) corresponds to a \( R_m \) operator in the definition of \( Q_l(y) \) (Eq. 12). It can be seen from Eq. 12 that \( \text{size}(Q_l) = l \) and the size of the circuit \( M \) is therefore

\[
\text{size}(M) = \sum_{j=1}^{k} \text{size}(M_j) = \sum_{j=1}^{k} \sum_{l=1}^{j} \text{size}(Q_l) = \sum_{j=1}^{k} \sum_{l=1}^{j} l = \sum_{j=1}^{k} \frac{j(j-1)}{2} = O(k^3). \tag{16}
\]

\( \square \).

Now the overall depth of a hybrid circuit performing \( n \) MAC operations on \( k \) bit integers can be estimated. This is done for both the exact and approximate case.

**Theorem 1** There exists a hybrid quantum circuit with depth in \( O(n+k) \) which performs \( n \) multiply additions of \( k \) bit integers exactly using \( O(k^3) \) qubits.

Proof. The quantum circuit used to perform \( n \) multiply additions is shown in Figure 4. The number of qubits used by the circuit is equal to the number of qubits the \( M \) operator acts upon, which by Lemma 2 is \( O(k^3) \).

The \( \text{QFT} \) and \( \text{QFT}^\dagger \) of \( k \) qubits can be applied in \( O(k) \) depth \( [23] \). The fan-out operations \( F \) can be constructed using a tree-like structure so that the depth of that circuit is logarithmic in the number of qubits to which they are applied \([21] \), i.e. \( O(\log k^3) = O(\log k) \). The \( M \) circuit can be performed in exactly two steps as proven in Lemma 1 and it is applied it exactly \( n \) times. Thus the overall depth, i.e. the number of parallel steps required for the application of the circuit, is \( n \cdot O(1) + 2 \cdot O(\log k) + 2 \cdot O(k) = O(n + k) \) \( \square \).

In practice it is unlikely that any quantum gates, or indeed, classical logic gates, could be implemented perfectly. That is, there will always be a small probability of the implemented gate failing, resulting in a wrong answer. However, it is sufficient to obtain the correct result with high enough probability. When an exact result is not required, the depth of a hybrid circuit computing multiple MAC operations can be even smaller. A unitary operator is approximated with precision \( \epsilon \) if for any pure input quantum state the Euclidian distance between the desired unitary \( U \) and the implemented unitary \( V \) is at most \( \epsilon \).
Theorem 2 There exists a hybrid quantum circuit with depth $O(n + \log k + \log \log 1/\epsilon)$ which performs $n$ multiply additions of $k$ bit integers with precision $\epsilon$ using $O(k^3 + k \cdot \log(k/\epsilon))$ qubits.

Proof. To obtain a better depth than in the exact case a slightly modified version of the circuit in Figure 4 is used in the approximate case. The initial QFT can be replaced with a single layer of Hadamard gates applied to the $k$ qubit state $|0\rangle$. Note that this is equivalent to applying QFT to $|0\rangle$. Next the $M$ circuit is used to add $z \cdot 1$ to $QFT|0\rangle$, which gives us the state $QFT|0 + z \cdot 1\rangle = QFT|z\rangle$. This is the same result as would be obtained by the exact circuit, but can be done in constant depth.

An approximate version of $QFT^\dagger$, introduced in [23], can be used as the final step. This $QFT^\dagger$ has depth $O(\log k + \log \log 1/\epsilon)$ and size $O(k \cdot \log(k/\epsilon))$ with precision $\epsilon$. The depth of the fan-out and $M$ operations are discussed above. The $M$ is applied exactly $n + 1$ times. Thus the overall depth is $(n + 1) \cdot O(1) + O(1) + 2 \cdot O(\log k) + O(\log k + \log \log 1/\epsilon) = O(n + \log k + \log \log 1/\epsilon)$.

The number of qubits used by the circuit is equal to the maximum number of qubits the $M$ operator acts upon, which by Lemma 2 is $O(k^3)$, and the number of qubits $QFT^\dagger$ acts upon. Thus the total number of qubits acted upon is $O(k^3 + k \cdot \log(k/\epsilon))$. □

4 Results and Discussion

The depth of the proposed circuit for adding $n$ integers of $k$ bits is $O(n + k)$ for the exact circuit and $O(n + \log k)$ for the approximate circuit. The classical implementations of MAC are limited by the depth complexity of the multiplication operations. This is true even for the lowest depth multiplication circuits such as Wallace [24] and Dadda [25] multipliers which are used in most CPU architectures and have a depth of $O(\log k)$. Thus the sequential application of $n$ classical MACs requires at least $O(n \log k)$ parallel steps. It is unlikely that gate delays in classical and quantum circuits will be the same. Indeed, they vary for different classical circuits. However, in this analysis of the different circuits the simple counting of the number of gates is used. It is worth nothing that the advantage in depth gained by using a QMAC increases with the number of sequential applications and the size of integers used. Thus independent of the gate delays, there will be for every integer size an $n$ such that performing at least $n$ MAC operations has less depth when using the hybrid QMAC circuit than a classical one.

The small depth of the QMAC is a consequence of using the QFT, a highly entangled quantum state and classical fan-out, that is, copying of bits. First, since the MAC operation is performed on the QFT state, only diagonal gates are necessary. This makes it possible to entangle the quantum register with auxiliary qubits in a way that allows the simultaneous application of every single-qubit quantum gate. Second, the states of a bit can be copied by using multiple output wires to more than two registers for the next computational step. Thus the information propagates in one step to all the quantum gates controlled by these bits. This can be interpreted as influencing the state of an unbounded number of qubits with just one fan-out operation.
The hybrid QMAC circuit implements a very specific computational pattern, the MAC. This makes it suitable for use as an execution unit in a hybrid CPU or even a separate accelerator device such as a FPGA or GPU in future computers. Moreover, the fact that implementing this circuit does not require a full quantum computer makes it more likely to be realisable in the near future. The small depth of the circuit contributes to the ease of implementation, since the time needed to keep the quantum state coherent depends on the circuit depth. A further consequence of the hybrid nature of the circuit is that the number of qubits and two-qubit gates used is relatively small. Instead of using only quantum registers, two of the three registers in QMAC circuit are classical. Using classically controlled single qubit gates instead of fully quantum controlled gates limits the number of two-qubit gates used. However, the entangled state used requires $O(k^3)$ auxiliary qubits and two-qubit gates.

Future work would be to consider how to adapt the hybrid QMAC circuit floating to point operations, which are used in most of the time-intensive computations. This would greatly increase the number of problems which would benefit from quantum devices. Another direction would be to consider hybrid circuits for other arithmetic operations for example division and look at how the different circuits can be combined together. The QMAC introduced in this paper has a lower depth than a classical MAC only if it is applied in a sequence. Hence combining different quantum arithmetic operators could result in an improved depth compared with classical circuits.

References

1. D Bonneau, E Engin, K Ohira, N Suzuki, H Yoshida, N Iizuka, M Ezaki, C M Natarajan, M G Tanner, R H Hadfield, S N Dorenbos, V Zwijler, J L O’Brien, and M G Thompson. Quantum interference and manipulation of entanglement in silicon wire waveguide quantum circuits. Journal of Physics A: Mathematical and Theoretical, 14(4):045003, April 2012.
2. R Baxter, S Booth, M Bull, G Cawood, J Perry, M Parsons, A Simpson, A Trew, A McCormick, G Smart, R Smart, A Cantle, R Chamberlain, and G Genest. Maxwell - a 64 FPGA Supercomputer. In 2nd NASA/ESA Conference on Adaptive Hardware and Systems, pages 287–294, Edinburgh, August 2007. IEEE.
3. O Almer, R V Bennett, J Böhm, A C Murray, X Qu, M Zuluaga, B Franke, and N P Topham. An End-to-End Design Flow for Automated Instruction Set Extension and Complex Instruction Selection based on GCC. In Proceedings of 1st International Workshop on GCC Research Opportunities, 2009.
4. Vlatko Vedral, Adriano Barenco, and Artur Ekert. Quantum networks for elementary arithmetic operations. Physical Review A, 54(1):147–153, July 1996.
5. Michael John Sebastian Smith. Application-Specific Integrated Circuits. Addison-Wesley Professional, 1 edition, June 1997.
6. Kai-Wen Cheng and Chien-Cheng Tseng. Quantum full adder and subtractor. Electronics Letters, 38(22):1343–1344, October 2002.
7. Steven A Cuccaro, Thomas G Draper, Samuel A Kutin, and David Petrie Moulton. A new quantum ripple-carry addition circuit. arXiv.org, quant-ph, October 2004.
8. Amlan Chakrabarti and Susmita Sur-Kolay. Designing Quantum Adder Circuits and Evaluating Their Error Performance. In International Conference on Electronic Design, pages 1–6, December 2008.
9. Yasuhiro Takahashi, Seiichiro Tani, and Noboru Kunihiro. Quantum Addition Circuits and Unbounded Fan-Out. Quantum Information and Computation, 10(9&10):872–890, 2010.
10. Robert Raussendorf, Daniel Browne, and Hans Briegel. Measurement-based quantum computation on cluster states. Physical Review A, 68(2), August 2003.
11. Thomas G Draper, Samuel A Kutin, Eric M Rains, and Krysta M Svore. A Logarithmic-Depth Quantum Carry-Lookahead Adder. *Quantum Information and Computing*, 6(4&5):351–369, July 2006.

12. Lafifa Jamal, Md Shamsujjoha, and Hafiz Md Hasan Babu. Design of Optimal Reversible Carry Look-Ahead Adder with Optimal Garbage and Quantum Cost. *International Journal of Engineering and Technology*, 2(1):44–50, January 2012.

13. Agung Trisetyarso and Rodney Van Meter. Circuit Design for A Measurement-Based Quantum Carry-Lookahead Adder. *International Journal of Quantum Information*, 8(5):843–867, August 2010.

14. Thomas G Draper. Addition on a Quantum Computer. *arXiv.org*, quant-ph, August 2000.

15. J J Álvarez-Sánchez, J V Álvarez-Bravo, and L M Nieto. A quantum architecture for multiplying signed integers. *Journal of Physics: Conference Series*, 128(1):1–9, October 2008.

16. Himanshu Thapliyal and M.B Srinivas. Novel Reversible Multiplier Architecture Using Reversible TSG Gate. *IEEE International Conference on Computer Systems and Applications*, cs.AR:100–103, May 2006.

17. H Thapliyal and M.B Srinivas. Novel Reversible ‘TSG’ Gate and Its Application for Designing Components of Primitive Reversible/Quantum ALU. In *Information, Communications and Signal Processing, 2005 Fifth International Conference on*, pages 1425–1429, 2005.

18. Moayad A Fahdil, Ali Foud Al-Azawi, and Sammer Said. Operations Algorithms on Quantum Computer, January 2010.

19. Michael Kirkedal Thomsen, Robert Glück, and Holger Bock Axelsen. Reversible arithmetic logic unit for quantum arithmetic. *Journal of Physics A: Mathematical and Theoretical*, 43(38):382002, August 2010.

20. Y Syamala and A.V.N Tilak. Reversible Arithmetic Logic Unit. In *3rd International Conference on Electronics Computer Technology*, pages 207–211, 2011.

21. Cristopher Moore and Martin Nilsson. Parallel Quantum Computation and Quantum Codes. *SIAM Journal on Computing*, 31(3):799–815, January 2001.

22. Michael A Nielsen and Isaac L Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, 10 anv edition, January 2011.

23. Richard Cleve and John Watrous. Fast Parallel Circuits for the quantum Fourier transform. In *Proceedings of the 41st Annual Symposium on Foundations of Computer Science*, pages 526–536, Rendo Beach, CA, USA, 2000. IEEE Comput. Soc.

24. C S Wallace. A Suggestion for a Fast Multiplier. *IEEE Transactions on Electronic Computers*, EC-13(1):14–17, 1964.

25. L Dadda. Some schemes for parallel multipliers. *Alta Frequenza*, 34:349–356, 1965.