MOS structures containing silicon nanoparticles for memory device applications

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Abstract. Metal-oxide-silicon structures containing layers with amorphous or crystalline silicon nanoparticles in a silicon oxide matrix are fabricated by sequential physical vapour deposition of SiO x (x=1.15) and RF sputtering of SiO 2 on n-type crystalline silicon, followed by high temperature annealing in an inert gas ambient. Depending on the annealing temperature, 700 °C or 1000 °C, amorphous or crystalline silicon nanoparticles are formed in the silicon oxide matrix. The annealing process is used not only for growing nanoparticles but also to form a dielectric layer with tunnelling thickness at the silicon/insulator interface. High frequency C-V measurements demonstrate that both types of structures can be charged negatively or positively by applying a positive or negative voltage on the gate. The structures with amorphous silicon nanoparticles show several important advantages compared to the nanocrystal ones, such as lower defect density at the interface between the crystalline silicon wafer and the tunnel silicon oxide, better retention characteristics and better reliability.

1. Introduction
Layers containing silicon nanocrystals (Si NCs) have been studied actively in recent years since they are promising for application in distributed floating gate memory devices [1,2]. The usage of nanocrystals as discrete charge storage nodes can result in better stability [3] compared to the conventional floating gate memory device since a single leakage path will not discharge all of the nanocrystals and thus cause loss of information.

Various techniques have been used to obtain layers with Si nanocrystals embedded in a dielectric matrix: deposition of amorphous silicon followed by oxidation [4,5]; ion implantation [2,6]; thermal evaporation of SiO [3,7,8] etc. Our previous results [8-10] clearly demonstrate that annealing of thermally evaporated SiO layers at 1000 °C and 700 °C leads to formation of crystalline silicon nanoparticles in a SiO 2 matrix or amorphous silicon nanoparticles (a-Si NPs) in a silicon suboxide matrix, respectively. Dielectric layers with a-Si NPs have been studied for obtaining light emitting structures but too little is known about the possibility to use such layers in memory devices. In this work, results about charging effects in metal-oxide-silicon (MOS) structures containing a-Si NPs are presented and compared with charging effects in similar MOS structures containing Si nanocrystals.
2. Experimental details
The experimental structures explored in this study were fabricated by physical vapour deposition of an ultrathin SiO$_x$ (x=1.15) layer [7] with a thickness of ~15 nm on top of n-type (100) crystalline silicon with resistivity of 4-6 $\Omega$ cm, followed by radio frequency (RF) sputtering of a control silicon oxide with a thickness of ~40 nm. In order to form amorphous or crystalline silicon nanoparticles (with size ~5 nm), the structures were annealed for 60 min at 700 °C in Ar or 1000 °C in N$_2$, respectively [8-10]. The annealing process was used not only for growing of silicon nanoparticles but also to form simultaneously a dielectric layer with tunnelling thickness at the interface with the silicon wafer. After the annealing, Al metallization was carried out through a mask and MOS capacitors with area of ~2×10$^{-3}$ cm$^2$ were formed. Aluminium was also used as a back contact to the crystalline silicon. High frequency capacitance-voltage (C-V) and parallel conductance-voltage (G-V) measurements at 1 MHz were used to study the charging and discharging phenomena in the structures.

3. Results and discussion
Figure 1 shows high frequency C-V hysteresis curves of an as-deposited (not annealed) sample measured in three voltage ranges: (0 - 1.5 V) and back (curve 1), ± 5 V (curve 2) and ± 8 V (curve 3). In all measurements, ± scanning means that the gate bias was first swept from positive to negative voltage and then in the reverse direction. In order to avoid charging of the structures, the first measurement on each MOS capacitor (this sample, as well as the annealed ones) was carried out in a narrow enough range given in the corresponding figure caption. It is seen that curve 1 has a very small hysteresis when compared to that of curves 2 and 3. The hysteresis of the ± 5 V and ± 8 V scans is a result of carrier capture in traps in the SiO$_x$ layer and is due mainly to a shift of the C-V characteristic towards more negative voltages. The behavior of the C-V characteristic after charging the structure with positive voltage is not typical. Normally, the higher the amplitude of the positive voltage, the stronger the shift in the positive direction. However, in these samples the application of a higher positive voltage causes a shift which corresponds to a smaller value of the trapped negative charge (compare the right branches of curves 3 and 2 with flatband voltages $V_{FB}$ ≈ -1.3 V and -0.3 V, respectively). Moreover, the +8 V bias shifts the C-V characteristic even to the left of curve 1. A possible explanation is that the positive charge resulting from electrons escaping from traps and reaching the top electrode is larger than the negative charge due to captured electrons injected from the c-Si wafer. Another important feature of the as-deposited structures is that they lose the charge created by negative bias quite fast (for several minutes).

![Figure 1](image-url)  
**Figure 1.** Normalised high frequency C-V characteristics measured at 1 MHz of an as-deposited sample:  
curve 1 – measured by sweeping the gate voltage between 0 and -1.5 V and back,  
curves 2 and 3 – in the ranges ± 5 V and ± 8 V, respectively.  
C$_{acc}$ is the structure capacitance in accumulation.

Figures 2 (a) and (b) show high frequency C-V hysteresis curves of two samples with amorphous and crystalline silicon nanoparticles, respectively, measured in the ranges ±11 V (curves 2) and
± 15 V (curves 3). Curve 1 was measured in a narrower range +3 V, -7 V. From the capacitance in accumulation, a value of about 56 nm was obtained for the insulator effective thickness. This value is in good agreement with the total thickness of the deposited SiOx and SiO2 layers.

![Figure 2](image1.png)

**Figure 2.** C-V dependencies measured at 1 MHz of samples with (a) amorphous (b) crystalline silicon nanoparticles. Curve 1 was measured in the range +3 V, -7 V for both (a) and (b) samples, curves 2 and 3 - in the ranges ±11 V and ±15 V, respectively.

In both types of samples the application of a positive voltage shifts the curves to the right, which corresponds to a larger negative charge trapped in the oxide close to the crystalline silicon wafer, and vice versa, a negative bias shifts the curves in the opposite direction. The value of the clockwise hysteresis is about 4.3 and 9 V (a) and 5.5 and 9.8 V (b) for ±11 V and ±15 V scanning ranges. The maximum average electric field across the gate dielectric, which corresponds to these scanning ranges, is about 2.0 MV/cm and 2.7 MV/cm, respectively. The shifts in figure 2 can be explained assuming charging of the nanoparticles with electrons/holes, which tunnel from the substrate through the thin oxide at positive/negative biases. The C-V characteristics of the a-Si NP structure are much steeper, which indicates lower defect density at the c-Si wafer/silicon oxide interface.

Figures 3 (a) and (b) show the equivalent parallel conductance G vs. gate bias of both types of samples. The measurements of G and C were carried out simultaneously in a single voltage scan. Curves in figures 3 (a), (b) are corrected for in-series resistance using the expressions in [11]. The observed shape of the equivalent parallel conductance, with a peak in weak inversion, corresponds to energy loss due to carrier generation and recombination through interface states [11]. If defects in the

![Figure 3](image2.png)

**Figure 3.** Equivalent parallel conductance measured at 1 MHz of samples with (a) amorphous and (b) crystalline silicon nanoparticles. The scanning ranges are the same as for C-V measurements in figure 2.
oxide layer contribute to the loss, they should be situated very close to the c-Si wafer/dielectric interface in order to be able to respond to the measuring frequency of 1 MHz. It is seen that the curves of structures with a-Si NPs are narrower than those of structures with Si NCs. Also, the peak of the parallel conductance has a smaller value (with about 40%) for the a-Si NP sample. These observations confirm the above conclusion that the structures with a-Si NPs have better c-Si substrate/dielectric interface than those with Si NCs. We suggest that due to the greater flexibility of the structure of a-Si NPs they fit easier in the SiO\textsubscript{x} matrix, because of which the internal strain in the SiO\textsubscript{x} matrix is lower than in the SiO\textsubscript{2} one and this could result in a better c-Si wafer/SiO\textsubscript{x} interface, i.e. lower interface defect density compared to the case of Si nanocrystals.

The retention characteristics of structures with a-Si NPs and NCs were obtained by measuring the time-dependent variation of the flatband voltage (figure 4), which is proportional to the area density of the trapped charge. In both types of structures, the charge loss follows approximately a logarithmic law. For our samples, an essential advantage of the a-Si nanoparticle structures compared to the NC ones is the much slower discharging process observed, especially of trapped electrons.

![Figure 4.Retention characteristics of structures with a Si NPs (a) and nanocrystals (b) after charging structures negatively with +15 V or positively with –15 V.](image)

4. Conclusions

C-V hysteresis curves of MOS structures containing amorphous or crystalline silicon nanoparticles demonstrate that the formation of these nanoparticles is essential for the memory effect observed. The structures with a-Si nanoparticles have several important advantages in comparison with the NC structures, the most important of which are lower defect density at the crystalline silicon/insulator interface and better retention characteristics, especially when the layers are charged negatively.

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