Design of Ultra-low Power Consumption Low-dropout Regulator

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Abstract—This paper designs a type of ultra-low power consumption LDO with the CSMC 0.5μm technology, which can output the 1.5V voltage. In this LDO, the error amplifier is structured with two-stage operational amplifiers. The input of first stage uses PMOS differential pairs that can decrease the noises and the second stage uses the common-source structure in order to increase the open-loop gain. In addition, the MOS amounts we use are as less as possible over the whole circuit, which decrease the die size to satisfy the trend of product miniaturization. The result of simulator Spectre shows that the LDO proposed can output the 1.5V voltage stably, the PSR is -66dB at 1kHz, and the loop gain is 72.5dB, the lowest dropout voltage is 93mV, the power consumption is only 1mW.

1. INTRODUCTION
With the reduction of characteristic size of transistors, electronic products and devices show a trend of product miniaturization. So far, with the wide application of miniature electronic products, the demand of portable electronic products is also increasing rapidly. Therefore, it is inevitably accompanied by a large demand for power management IC(PMIC). These typical products generally include: DC/DC, PFM/PWM control IC and linear voltage regulator. Among them, the analog low-dropout(LDO) regulator in voltage regulator IC is the main demand as well as several digital low-dropout regulators have been also proposed [1~6]. For instance, in portable mobile devices, the PMIC unit requires many LDO regulators with different output voltages and load current capacities to support many applications, such as application processor(AP), camera, memory, radio-frequency integrate circuit(RFIC) transceivers, universal serial bus(USB), and so on[7~12]. Besides, the DC/DC switching regulator operates with an internal conversion from DC to AC and then to DC, involving many off-chip capacitors, which makes it difficult to apply it to small electronic devices. In addition, for baseband, antenna and other high-frequency applications that require low input-output dropout voltage and high-power ripple rejection ratio, the low-dropout regulator is the best choice for many occasions. As the main research direction of LDO is no longer to pursue high load and high current, but to improve the accuracy, reduce the dropout voltage, increase the ripple rejection ratio, reduce the power consumption and speed up the transient response as much as possible, this paper designs a basic LDO to meet the above requirements by optimizing the structure of each part.
2. DESIGN PRINCIPLE OF LDO

The LDO consists of a reference circuit, an error amplifier, a buffer, a PMOS power transistor $M_p$, compensation capacitors and divided resistors, as shown in Figure 1.

![Fig. 1 LDO structure](image)

The main ports for LDO to interact with the outside world are: input voltage $V_{in}$ (It is also the power supply of bias circuit and error amplifier), output voltage $V_{out}$ and GND. The rest of the peripheral devices are compensation device ESR resistors and capacitors, plus equivalent load $R_L$. LDO works on the principle that a bandgap reference source, which is virtually immune to external influences, generates an ideal constant voltage as the reference voltage $V_{ref}$, which is used as one of the inputs to the error amplifier to compare voltage. When the input voltage increases and causes the output voltage to increase in a very short time, the voltage increment at the output end is perceived by sampling the resistor connected through the voltage divider, and then sent to the other end of the error amplifier through the feedback loop and compared with the reference voltage. The positive difference is amplified by the error amplifier and sent to the Gate end of the $M_p$, which causes the current $I_D$ flowing through the $M_p$ to decrease, and then the output voltage $V_{out}$ satisfies the following relationship:

$$V_{out} = I_D \times \left( R_1 + R_2 \right)$$ (1)

Therefore, in this case, the decrease of $I_D$ will inevitably lead to the decrease of $V_{out}$, so as to achieve the purpose of voltage stabilization. Conversely, when the input voltage is reduced, the output voltage is also reduced by it. The feedback network samples the reduced output voltage and transmits it to the other end of the error amplifier through the feedback loop, and then it will be compared with the reference voltage, resulting in a negative difference which is amplified by the error amplifier and transmitted to the Gate end of the $M_p$, which causes the current $I_D$ flowing through the $M_p$ to increase. From formula (1), we can see that $V_{out}$ will increase at this time, so as to achieve the purpose of voltage stabilization.

3. ERROR AMPLIFIER

The overall error amplifier is designed as two-stage amplification. The first stage uses a PMOS differential pair as the input stage because of its lower noise characteristics compared to NMOS [13]. Although cascode or folded-cascode can achieve higher gain and swing, it is not necessary for LDO used in low-voltage environments.

In order to reduce the noise parameters of devices and structures as much as possible and increase the output swing, the second stage of the error amplifier uses a common-source structure. In this way, the two-stage operational amplifier provides higher open-loop gain but lower power consumption and less noise as much as possible compared with sleeve structure and folding structure [14][15]. The specific circuit is shown in Figure 2.
From Figure 2 and the auxiliary theorem, the following results can be obtained.

The differential amplification gain of the first stage is:

\[
A_{v1} = -g_{m1} \cdot \left( \frac{r_{o1}}{r_{o3}} \right)
\]

The common-source amplification gain of the second stage is:

\[
A_{v2} = -g_{m8} \cdot \left( \frac{r_{o6}}{r_{o8}} \right)
\]

The total gain of the two-stage operational amplifier is:

\[
A_v = A_{v1} \cdot A_{v2}
\]

4. ZERO-POLE ANALYSIS

Suppose there are two poles and one zero of the two-stage operational amplifier, which are respectively located at the EA output (recorded as \(\omega_{p1}\)) and the Buffer output, including the ESR compensation capacitor \(C_L\) (recorded as \(\omega_{p2}\)) and of the LDO output, in addition the zero (recorded as \(\omega_z\)) is at the ESR with the output. the Bode plot of the two-stage operational amplifier is shown in Figure 3:

![Figure 3](image_url)

It can be seen that both main poles are close to the origin and the phase is already close to -180°, which is much lower than that of the third pole. In other words, the phase margin is likely to be close to 0 before the third pole produces a phase shift [16]. Therefore, the next thing we need to do is to move the first main pole \(\omega_{p1}\) closer to the origin so that the intersection point when the gain is reduced to 0 dB is far lower than the phase intersection point, but since the unit gain bandwidth after compensation is unlikely to exceed the frequency of the second pole of the open-loop system, if the value of \(\omega_{p1}\) is reduced, the achievable bandwidth will be limited to a low value of about \(\omega_{p2}\) [16]. On the other hand, for the main pole to become a very small value, a very large compensation capacitor is required.

Therefore, in this case, we use Miller compensation, which is equivalent to establishing a low-frequency pole with a moderate value of capacitor, and significantly increases the input capacitor and decreases the output capacitor. The specific analysis is as follows.

As shown in Fig.4 the LDO system introduces three poles P1, P2 and P3 and one zero Z1, in which the P1 should be the dominant pole, and the P3 is the load pole varies with the load current \(I_{LOAD}\), the P2 is the buffer output pole. Then we can write down these poles and zero to be[17]
\[ P_1 = \frac{1}{2\pi \times R_{o1} (1 + A_{e2}) C_m} \] (5)

\[ P_2 = \frac{1}{2\pi \times R_{o2} C_m} \] (6)

\[ P_3 = \frac{1}{2\pi \times \left( \frac{R_1 + R_2}{R_p} \right) (C_L + C_p)} \] (7)

\[ Z_1 = \frac{1}{2\pi \times ESR \times C_L} \] (8)

where the \( R_{o1}, R_{o2} \) and \( R_p \) are resistances seen at the output terminals of EA, Buffer, and \( M_p \), respectively. The \( C_m \) is the Miller capacitor connecting between the input and output of the Buffer.

5. SIMULATION OF LDO CIRCUIT

5.1 Overall circuit of LDO
Next, several important parameters of LDO are simulated. The overall LDO circuit schematic is shown in Figure 5. (Miller compensation capacitor of error amplifier are not indicated.)

5.2 Gain and phase margin of error amplifier
The error amplifier used in this LDO is tested by simulator Spectre, and its gain and phase curves are shown in Figure 6.
The open-loop gain of the op-amp is 83.6dB and the phase margin is 62°.

As mentioned earlier, Miller compensation is used to adjust the zero-pole to make the system run stably, with the gain and phase curves of the loop shown in Figure 7.

It can be seen from the curve that the loop gain is 72.5dB and the phase margin is 65°, which can ensure the stability of the system and meet the design requirements.

5.3 **The lowest dropout voltage**

The LDO is designed with a constant output of 1.52V. The input DC voltage is gradually increased from 0V to 10V when scanning. The voltage amplitude is observed at the output end. The lowest input-output dropout voltage is defined as the difference between the input voltage and the output voltage that can maintain the LDO in the normal voltage stabilization.

As shown in Figure 8, the input voltage is increased from 0V to 1.613V when it starts to enter the linear regulated operating state. At this time, the output voltage is 1.52V, which means that the lowest input-output dropout voltage of this LDO is 93mV.
5.4 Response time
Response time is a very important transient response parameter for LDOs, which reflects how quickly the entire LDO system responds to sudden changes in voltage. This test inputs two transient signals at the LDO and observes the corresponding output amplitude at the LDO. Specifically, when \( t=0 \), the input voltage is kept at 0V, then the output voltage will also be 0V; a step signal with an amplitude of 2.5V is suddenly added at \( t=2\mu s \); when the LDO output voltage returns to 0V, a step signal with an amplitude of 0.5V is suddenly added, which is lower than the normal regulated input range. The transient response of LDO output is shown in Figure 9.

It can be seen from Figure 8 that the overshoot response of this LDO is:

\[ \Delta t_1 = 5.45 - 2\mu s = 3.45\mu s \]

The undershoot response is:

\[ \Delta t_2 = 13 - 10\mu s = 3\mu s \]

5.5 Power supply rejection (PSR)
The power supply rejection (PSR) reflects the ability of LDO to suppress noise. Set the 1V AC small signal as the input and set the load as 2kΩ. The simulator Spectre is used to conduct AC simulation,
with the sweep frequency range from 0.01Hz to 100MHz. The 20lg amplitude at the output is observed, as shown in Figure 10.

Fig.10 The PSR

The figure shows that the PSR at f=1kHz is about -66dB; the PSR at f=10kHz is about -59.5dB.

5.6 Linear regulation rate

The linear regulation rate reflects the ability of the output voltage to remain stable when the supply voltage changes [18]. The supply voltage is set to 3V, and then a square wave with an amplitude of ±300mV is connected in series to this supply, causing the supply to undergo a large fluctuation. The voltage amplitude at the output is observed, as shown in Figure 11.

Fig.11 The line regulation

When the power supply continuously fluctuates in the range of 3±0.3V, the voltage at the output fluctuates in the range from 1.515V to 1.537V. The linear regulation rate is:

\[ \Delta S_0 = \frac{\Delta V_{out}}{\Delta V_{dd}} \approx 3.67\% \]

5.7 Power consumption

The minimum input voltage for the LDO to enter the regulated state at no load is 1.613V. An input voltage of 1.613V is added to the LDO, then the quiescent current of the LDO is 371.447nA. Therefore, the power consumption of LDO at no load is

\[ 371.447nA \times 1.613V \approx 0.6 \mu W \]
When the load is 2kΩ, the minimum input voltage for the LDO to enter the regulated state is 2.8V. An input voltage of 2.8V is added to the LDO. Then the quiescent current of the LDO is 760.6μA, the load current is 760μA, and the load voltage is 1.52V. Therefore, the power consumption of LDO at this time is:

\[(2.8-1.52V) \times 0.76mA \approx 1mW\]

### 6. CONCLUSION

Based on the CSMC 0.5μm technology, an ultra-low power consumption low-dropout regulator with a constant output voltage of 1.5V has been designed in this paper. The circuit has been simulated and optimized by the simulator Spectre to meet the design requirements. Taking [19][20][21] as examples, the quiescent current under no-load state in this paper is further reduced compared to some low power consumption designs, which effectively reduces the LDO power consumption. The comparison is shown in the table below.

| TABLE I. PERFORMANCE COMPARISON |
|---------------------------------|
|                   | Dropout/mV | Quiescent current/μA | PSR /dB@Hz |
| [19]              | 200        | 0.9                   | -58@10kHz  |
| [20]              | 200        | 0.9                   | -42@1MHz   |
| [21]              | 200        | 0.61                  | -26@1MHz   |
| This paper        | 93         | 0.37                  | -59@10kHz  |

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