A highly linear 25 MHz bandwidth Gm-C SOI complex filter

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Abstract. In this paper, a highly linear complex filter in SOI X-FAB 180 nm technology is proposed for 25 MHz bandwidth with 25 MHz center frequency. Third harmonic compensation technique is used for transconductance amplifier design. Reactance transform is used for the filter synthesis. Layout design is discussed. Simulations show THD better than -75 dB @ 25 MHz 1 Vpp for temperature range of -40 to +200 °C.

1. Introduction
Nowadays, frequency selective circuits are widely used in modern homodyne and low-IF (intermediate frequency) quadrature channel system-on-chip transceivers in different applications from wireless telecommunications to navigation and RFID systems [1-4]. Due to additional image rejection and convenient realization in basis of integrators, complex filter is a preferable choice for channel selection. There are several known implementations for CMOS in ARC and Gm-C techniques, for example see Refs. [5-7]. For high operating temperatures SOI (silicon-on-insulator) technology could be used, though publications are rare, for example see Refs. [8-9]. Gm-C technology provides wide frequency operating range for a moderate power consumption, but require linearization techniques to be implemented for acceptable input voltage range.

In this paper, a relatively wide frequency operating range complex filter for high temperatures (up to 200 °C) is proposed. Thus, it is a SOI Gm-C solution that is chosen. As Gm-C filter essentially consists of transconductance amplifiers (TA) and capacitors, the linearization of TA is of interest. Refs. [10-11] report solution, analog of which is used for SOI design. In this paper, second part is devoted to transconductance amplifier realization, third part describes complex filter synthesis through reactance transform of a Gm-C LPF (low-pass prototype filter), and in fourth part layout realization and comparison of results are provided.

2. Transconductance amplifier realization
In order to provide maximum linearity in terms of THD (third harmonic distortion), compensation technique similar to proposed in Refs. [7, 10-11] is used. In essence, two CMOS transconductance amplifiers with transistors in different regimes, e.g. in saturation region and in triode region, are connected in parallel. Third harmonic current for such transistors has opposite polarity, thus output current formed of sum of saturation region current and triode region current, has lower third harmonic level. As with standard CMOS process, it is optimal in terms of linearity achieved for Gm/I ratio. As it is a SOI technology, for similar structure and transistors sizes performance differ from standard CMOS prototype. For design proposed, X-FAB XT018 library components are used with Cadence Virtuoso 6.17 software for simulation process.
Figure 1 shows the schematic of the proposed transconductance amplifier. Top six p-transistors form current mirror; bottom left four transistors provide main amplifier in saturation region, three transistors next to it provide half of CMFF (common-mode voltage feedforward circuit); next four transistors form compensation amplifier in triode region, three transistors next to it form second half of CMFF. As in Ref. [7], common control voltage $V_c$ is used instead of $V_c$ and $V_{inCM}$, as in Refs. [10-11].

Transistor widths for design proposed are as follows: 11.6 um for current mirror, 1.44 um for main amplifier (four transistors), 144 um for lower pair of compensation amplifier, 0.22 um for upper pair of compensation amplifier; 1.44 um for left CMFF lower transistor, for upper pair 0.72 um; 72 um for right CMFF lower pair, 0.22 um for upper transistor.

Length of transistors is chosen as minimal and equals to 0.18 um, which provides the largest operating frequency range. For supply voltage of 1.8 V and control voltage of 0.9 V TA provides $Gm$ value of 78 uA/V for 222 uA supply current, which corresponds to $Gm/I$ of 0.35. It is smaller than that in Ref. [7], but it is typical for $Gm/I$ ratio to be less than 1. Figure 2 shows results of DC simulation for different $V_c$ from 0.8 to 1.2 V, which provides tuning range of ±50% of $Gm$ value. For nominal value of 78 uA/V 1 % $Gm$ value variation input voltage range ($V_{diff}$) is ±104 mV, 0.707 $Gm$ value (-3 dB of power) corresponds to ±253 mV. It is significantly narrowed in comparison with that of Ref. [7], but it is one of the drawbacks of SOI versus standard CMOS technology.

Nevertheless, cutoff frequency for $Gm$ value is 1.33 GHz, which provides stable $Gm$ for all possible applications, as for $Gm = 78$ uA/V capacitor values should be around 0.25 pF to reach 100 MHz bandwidth and less for higher frequencies.

THD was measured through transient analysis for the sinusoidal input signal and ideal $Gm$ load in resistance mode. At 100 MHz for 200 mV Vpp THD is -58 dB. Thus, for 1% $Gm$ value variation THD is similar to that of the TA realized in a standard CMOS process.

Figure 3 shows the results of DC simulation for different temperatures from -40 up to +200°C. It is shown that the proposed amplifier maintain performance with $Gm$ value variation of 86 down to 62 uA/V.
Figure 2. Proposed transconductance amplifier DC characteristic versus control voltage $V_c$. $V_c$ varies from 0.8 V (corresponds to 42 uA/V $G_m$ value) to 1.2 V (corresponds to 122 uA/V $G_m$ value).

Figure 3. Proposed transconductance amplifier DC characteristic versus temperature. Temperature varies from -40° C (corresponds to 86 uA/V $G_m$ value) to +200° C (corresponds to 62 uA/V $G_m$ value).

3. Complex filter synthesis

Proposed filter structure is in essence similar to that from Ref. [7]. Figure 4 shows the structure of a 5+5 order fully differential complex filter with input voltage to current converter. Input converter can be of higher value than the main transconductance amplifier to compensate for in-band losses.

For VCCS (voltage controlled current source) basis, of which transconductance amplifier is a special case, synthesis procedure for ladder structure can be described as follows:

- choose the prototype from attenuation and in-band ripple requirements;
- renormalize capacitors using the input-output load and calculate capacitors of inductance imitators for an LPF with the cut-off frequency equal to a half of the complex filter passband;
- calculate a gyrator for each capacitor for the interconnection between I and Q channels as

$$G_{ii} = \omega_0 C_i$$  \hspace{1cm} (1)

where $G_{ii}$ – $G_m$ value of the TA used in gyrator, $\omega_0$ – frequency shift, $C_i$ – capacitor value.
Butterworth regular approximation is used as a compromise between the attenuation and phase characteristic linearity. For proposed 25 MHz bandwidth and 25 MHz center frequency with main TA $Gm$ value of 78 $\text{uA/V}$ values of capacitors and interconnection TAs are as follows:

- $C1 = C5 = 1.226 \text{ pF}$
- $C2 = C4 = 3.21 \text{ pF}$
- $C3 = 3.97 \text{ pF}$
- $G11 = G55 = 96 \text{ uA/V}$
- $G22 = G44 = 251.4 \text{ uA/V}$
- $G33 = 310.6 \text{ uA/V}$

Figure 5 shows a frequency response of the ideal complex filter. Simulation results confirm good performance of synthesis procedure. At 50 MHz signal rejection is 30 dB (6 dB/octave), $IRR$ (image rejection ratio, lower curve) is better than 30 dB.

Interconnection transconductance amplifiers differ from the channel TA only in the part of main amplifier and current mirror, the compensation amplifier is equal for all TAs. For real TAs the finite output resistance (about 160 kOhm for main TA) and parasitic capacitances degrade its frequency response. In case of the SOI filter, either capacitances and control voltages for channel and interconnection TAs (separately) were corrected to get desired frequency response. Corrected values are as follows:
\[ C_1 = C_5 = 0.615 \, \text{pF} \]
\[ C_2 = C_4 = 2.24 \, \text{pF} \]
\[ C_3 = 2.96 \, \text{pF} \]
\[ V_{c1} = 925 \, \text{mV} \, \text{(channel TA)} \]
\[ V_{c2} = 890 \, \text{mV} \, \text{(interconnection TA)} \]

Figure 6 shows the filter frequency response after the correction. In-band loss is 12.5 dB (6.5 dB additional loss), attenuation is 25 dB/octave due to finite output resistance. Center frequency is 24.5 MHz for values listed, passband 24.95 MHz. Ideal correction is meaningless due to technological process variations and other factors, that will lead to frequency response changes. Tuning system should be implemented in a real application.

Supply current of the filter in DC mode is 8.94 mA, while in transient mode it is up to 10.06 mA for 1 Vpp input signal (corresponds to 18.1 mW). Because of capacitive load of input TA, linear input voltage range expands, thus \( THD \) was measured at 1 Vpp. At 25 MHz \( THD \) is -75.88 dB for 1 Vpp.

Figure 7 shows changes of the filter frequency response versus temperature. Frequency response changes in either passband and in-band losses, but the filter maintain working ability in range of -40 up to +200° C. A tuning system should compensate this changes in the filter response.

The tuning system is designed as a PLL (phased-locked loop) based on Gm-C VCO (voltage controlled oscillator). The inductor tank of the VCO is realized as a gyrator block with the same Gm parameter as the filter.

4. Layout realization
The proposed complex filter layout realization was accomplished in several steps. First, the main transconductance amplifier was designed. Space required for 78 uA/V TA is 55.41 um x 29.49 um. Interconnection amplifiers differ less than several um per side, as the triode part is equal and the mirrors have the same finger length. Performance of the extracted TAs (the extraction was performed with Assura Quantus QRC) differ from the schematic TAs less than for 1% for each parameter.

Second step was the filter core layout design. With VDD (supply voltage) and VSS (ground) busses space required is 416.91 um x 347.62 um. Overall filter frequency response change is less than 5% in
passband and center frequency (simultaneous changes). Next step is introducing pads. From simulation results, ESD structure for X-FAB X018 for 1.8 V supply introduces 4 pF parasitic capacitance for each pad to either VDD and VSS buses. Thus, a layout without ESD structure is proposed, as shown in Figure 8. Space required is 616.91 um x 578 um. Figure 9 shows the frequency response of the proposed layout. Overall filter frequency response is nearly the same as for the core without pads.

It should be noted that for image rejection ratio the effects of mismatch are more evident than for passband.

![Figure 8. Layout of complex filter with pads without ESD structure.](image1)

Transient response of the filter in the terms of current consumption and *THD* is much the same as that for the schematic realization. Comparison of the results with previously published is provided in Table 1.

![Figure 9. Frequency response of the extracted complex filter with pads. Lower curve – image rejection ratio, difference in I and Q channels due to mismatch effects.](image2)
Table 1. Comparison with previously published results.

| Parameter                | This work | [5] | [6] | [7] | [8] |
|--------------------------|-----------|-----|-----|-----|-----|
| Technology               | Gm-C, SOI | Gm-C, CMOS | ARC, CMOS | Gm-C, CMOS | Gm-C, FDSOI |
| Resolution, nm           | 180       | 180 | 65  | 180 | 28  |
| Order                    | 5+5       | 6+6 | 6+6 | 5+5 | 6+6 |
| Power, mW                | 18.2      | 0.72 | 8.5 – 26 | 36 | 1.42 – 1.73 |
| Bandwidth, MHz           | 25        | 3   | 4.2 – 18 | 25 | 1.195 |
| Center frequency, MHz    | 25        | 2   | 4 – 28 | 25 | 2   |
| IRR, dB                  | >37       | 55  | >31 | >47 | >90 |
| Linearity                | $THD -75.8$ dB @25 MHz 1 Vpp | $THD 45$ dB @2 MHz 0.2 Vpp | $IIP3 25 – 28$ dBm | $THD -80.0$ dB @25 MHz 1 Vpp | unknown |

5. Conclusion
In this paper, a highly linear complex filter in SOI X-FAB 180 nm technology is proposed for 25 MHz bandwidth with 25 MHz center frequency. Third harmonic compensation technique is used for transconductance amplifier design. Reactance transform is briefly described and used for complex filter synthesis. Layout design is discussed, refusal from using ESD structure is justified. Simulations show $THD$ better than -75 dB @25 MHz 1 Vpp for temperature range of -40 to +200 °C and power consumption no more than 18.2 mW. Results are comparable to that of 180 nm standard CMOS process.

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