Comparison of NMOS and PMOS Input Driving Dynamic Comparator in 45nm Technology

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Abstract. A comparison of NMOS and PMOS input driving dynamic comparator is carried out in 45nm technology. NMOS driving dynamic comparator shows lesser delay and consumes less power as compared to PMOS driving comparator. The advantage of the later is the noise immunity at higher frequencies. The normalized energy-noise-delay-product (ENDP) for NMOS dynamic comparator and PMOS dynamic comparator is 2.08 and 4.48, respectively.

1. Introduction
Analog-to-digital converter (ADC) is the channel between the analog and digital world. ADCs are classified into two groups based on the sampling rate: Nyquist rate and Oversampling. Flash ADC is a Nyquist rate ADC which is also the fastest ADC. It is comprised of comparator and an encoder. Comparator is the backbone of an ADC. Several comparators have been designed in the recent past which includes TIQ based comparator [1], OPAMP based comparator, and dynamic comparators [3, 4, 5, 6, 7]. A TIQ based comparator sets a threshold point by changing the dimension of NMOS and PMOS transistors. Other comparator designs require an additional resistor ladder circuit. Two conventional dynamic comparator designs are compared in this paper. The first one is NMOS driven dynamic comparator and the other is PMOS driving dynamic comparator. The advantage of using a dynamic comparator is that it is efficient as compared to other comparators in terms of power dissipation and delay. The dynamic comparator works in three stages: reset stage, comparison stage and regeneration stage. The output code generated by the comparator bank is termed as thermometer code. The number of comparators depends upon the resolution of flash ADC. The required number of parallel computing comparators is 2^n − 1 for n number of bits.

The characteristics of NMOS and PMOS driving dynamic comparators in 45nm technology is laid down in this paper. The energy-noise-delay product (ENDP) is calculated to observe the overall performance of the two comparators. A strong ARM latch [6] is used as a comparison circuit to observe the outputs characteristics. Several other dynamic comparators are designed in the recent advancements that are based on single tail [2] or dual tail [5] architectures to provide better results. In this paper, only a single tail architecture is used for comparison because it is the base for other architectures. Based on the comparison matrix, choice of input driving transistors can be made for a particular application.
The paper is divided into four sections to depict the granularity of the comparison. Section 1 provides a brief introduction of the selected topic. Section 2 demonstrates an overview of both the dynamic comparators. Section 3 showcases the simulated results and comparison matrix of both the designs. And, finally, Section 4 inferences the idea of comparison and its role in ADC design. The simulations are carried out in 45nm technology using LTSpice simulator.

Table 1. Status of transistors of NMOS and PMOS dynamic comparator

| Stage                    | Transistor | Status | Region of Operation |
|--------------------------|------------|--------|---------------------|
| Reset Phase              | M1         | OFF    | Cutoff              |
|                          | M2, M3     | ON     | Saturation          |
|                          | M4, M5     | ON     | Linear              |
|                          | M6, M7     | OFF    | Cutoff              |
|                          | M8, M9     | ON     | Linear              |
| Comparison Phase         | M1         | ON     | Linear              |
|                          | M2, M3     | ON     | Saturation          |
|                          | M4, M5     | ON     | Linear              |
|                          | M6, M7     | OFF    | Cutoff              |
|                          | M8, M9     | OFF    | Cutoff              |
| Regeneration Phase       | M1         | ON     | Linear              |
|                          | M2, M3     | ON     | Saturation          |
|                          | M4, M5     | ON     | Linear              |
|                          | M6, M7     | ON     | Linear              |
|                          | M8, M9     | OFF    | Cutoff              |

Table 2. Comparison matrix of NMOS and PMOS dynamic comparator

| Parameters              | NMOS Comparator | PMOS Comparator |
|-------------------------|-----------------|-----------------|
| Delay (ns)              | 35.1            | 55.5            |
| Power Dissipation (W)   | 4.328           | 4.44            |
| Noise (nV/Hz1/2)        | 3.9             | 3.28            |
| Normalized PDP (J)      | 1.51            | 2.46            |
| Normalized EDP (Js)     | 5.332           | 13.76           |
| Normalized ENDP (JsV/Hz1/2) | 2.08       | 4.48            |

2. Dynamic Comparator

Dynamic comparator has three stages: reset, comparison and regeneration. During the reset phase, the differential output is set to logic ‘0’ or logic ‘1’. After the reset phase, the comparator enters comparison phase and compares the differential inputs. When comparator enters regeneration phase, the outputs are regenerated to reach HIGH or LOW voltage levels.
based on differential inputs. Strong ARM latch based dynamic comparator is used to compare both the designs. NMOS and PMOS driving comparator circuit is depicted in figure 1 and figure 3, respectively. In both the designs, the tail transistor is either in active region or cutoff region. The input transistors are in saturation region and latch is in linear region. The clock pulse given to the NMOS comparator is the reciprocal to the pulse given to the PMOS comparator. The PMOS comparator pulls up the output faster than the NMOS comparator and the NMOS comparator pulls down the output faster than the PMOS comparator. A lower technology node is considered for simulation in order to consider the effect of small channel length devices. A comparison of NMOS input driving comparators is carried out earlier in [3],

**Figure 1.** Circuit diagram of NMOS dynamic comparator

**Figure 2.** Transient analysis of NMOS dynamic comparator
[11]. In order to explore the possibilities of PMOS driving comparators a comparison is made for application specific designs. PMOS input transistors based amplifiers provide lower noise in high frequencies. For fast amplifiers or comparators NMOS input transistors are preferred.

NMOS input driving dynamic comparator consists of an NMOS input amplifier and a latch circuit. The circuit diagram is depicted in figure 1. During the reset phase, CLK pulse is set to GND (or 0V) and the tail transistor M1 is turned OFF whereas the PMOS load transistors M8 & M9 turns ON pulling up both the output nodes to VDD (or 1V). During the comparison phase, CLK pulse is set to VDD and M1 turns ON. The input pairs M2 & M3 amplifies the differential input. During the regeneration phase, the latches pulls up or down the output node based on the differential input provided by the input differential NMOS pairs. The status of the transistors is shown in table 1. The transient analysis of NMOS transistor is shown in figure 1.
The voltage gain equation of the NMOS comparator is given by equation 1.

\[ \text{Voltage Gain}, \ A_{v,n} = \left( g_{mn2,3} V_{th,n} \right) / I_1 \]  

where, \( g_{mn2,3} \) is the transconductance of the input NMOS transistor pairs, \( I_1 \) is the tail current and \( V_{th,n} \) is the threshold voltage of an NMOS transistor.

Let, \( t_{amp} \) be the amplifier delay and \( t_{latch} \) be the latch delay, then total delay of the NMOS comparator is given by equation 2.

\[ \text{Delay}, \ t_{delay,n} = t_{amp} + t_{latch} = 2 \left( \frac{C_l |V_{thp}|}{I_1} \right) \left( \frac{C_l}{g_{m, eff}} \right) \ln \left( \frac{V_{DD}}{4 |V_{thp}| \Delta V_{in}} \right) \sqrt{\frac{I_1}{\beta_{2,3}}} \]  

where, \( C_l \) is the load capacitance, \( I_1 \) is the tail current, \( g_{m, eff} \) is the effective transconductance of the latch, \( V_{thp} \) is the threshold voltage of the PMOS transistor, \( V_{DD} \) is the supply voltage, \( \Delta V_{in} \) is the differential input, and \( \beta_{2,3} \) is the current coefficient of input NMOS transistor pair.

The regeneration time is given by the equation 3.

\[ \text{Regeneration time}, \ t_{reg,n} = \frac{C_{x,y}}{g_{m4,5} \left( 1 - \frac{C_{x,y}}{C_l} \right)} \]  

where \( g_{m4,5} \) is the transconductance of the latch NMOS pair, \( C_{x,y} \) is the capacitance across output nodes of the amplifier and \( C_l \) is the load capacitance.

Similarly, PMOS input driving dynamic comparator consists of a PMOS input amplifier and a latch circuit. The circuit diagram is depicted in figure 3. During the reset phase, \( CLK \) pulse is set to \( V_{DD} \) (or 1V) and the tail transistor M1 is turned OFF whereas the NMOS load transistors M8 & M9 turns ON pulling down both the output nodes to GND (or 0V). During the comparison phase, \( CLK \) pulse is set to GND and M1 turns ON. The input pairs M2 & M3 amplifies the differential input. After comparison, the comparator enter into the regeneration phase, the latches pulls up or down the output node based on the differential input provided.
by the input differential PMOS pairs. The status of the transistors is shown in table 1. The transient analysis is given in figure 4. The gain and delay equations of PMOS comparator is similar to that of the NMOS and is given by the following equations 4, 5, 6.

\[ Voltage \ Gain, \ A_{v,p} = \frac{g_{mp2,3}.V_{th,p}}{I_1} \]  

\[ Delay, \ t_{delay,p} = t_{amp} + t_{latch} \]  
\[ = 2. Cl|V_{th,n}| + \frac{Cl}{g_{m,eff}} \cdot \ln(\frac{VDD}{4.|V_{th,n}|\Delta V_{in}}) \sqrt{\frac{I_1}{\beta_{2,3}}} \]  

\[ Regeneration \ time, \ t_{reg,p} = \frac{C_{x,y}}{g_{m4,5} \left( 1 - \frac{C_{x,y}}{Cl} \right)} \]  

where, \( g_{mp2,3} \) is the transconductance of the PMOS input transistor pairs, \( V_{th,p} \) is the threshold voltage of the PMOS transistor, \( I_1 \) is the tail current through \( M1 \), \( Cl \) is the load capacitance, \( V_{th,n} \) is the threshold voltage of the NMOS transistor, \( \Delta V_{in} \) is the differential input, \( VDD \) is the supply voltage, \( g_{m,eff} \) is the effective transconductance of the latch, and \( \beta_{2,3} \) is the current coefficient of input PMOS transistor pair.

3. Observation and Results

The simulations are done in 45nm technology using LTSpice simulator. The supply voltage \( VDD \) is set to 1V because of the maximum voltage supported by the technology node. For a differential input of 10mV and clock pulse of period 200ns, the comparison matrix is tabulated in figure 2. Figure 5 compares the transient behaviour of both the comparators. It is observed that if the supply voltage is increased, the difference in the delay for voltage change is more for PMOS comparator and minimal for NMOS comparator. The delay change in NMOS varies from 235.1ns to 233.9ns whereas, for PMOS it varies from 155ns to 117.17ns. For input frequency of 100MHz, the calculated normalized ENDP (\( JV_s/Hz1/2 \)) for NMOS and PMOS comparator are 2.08 and 4.48, respectively.

4. Conclusion

It can be inferred from the above results that the NMOS dynamic comparator provides better results. However, PMOS comparator at higher frequencies provides better noise immunity. The PMOS dynamic comparators can be used in applications where noise is an important factor. The normalized power-delay product (PDP) for NMOS and PMOS dynamic comparator are calculated to be 1.51 and 2.46, respectively. The normalized energy-delay product (EDP) for NMOS and PMOS dynamic comparator are calculated to be 5.332 and 13.76, respectively. The normalized energy-noise-delay product (ENDP) for NMOS and PMOS dynamic comparator are calculated to be 2.08 and 4.48, respectively. The overall result favours the wide use of NMOS input driving dynamic comparator. The study provides a platform for use of application based comparators.

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