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Normally-Off p-GaN Gated AlGaN/GaN MIS-HEMTs with ALD-Grown Al$_2$O$_3$/AlN Composite Gate Insulator

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Abstract: A metal–insulator–semiconductor p-type GaN gate high-electron-mobility transistor (MIS-HEMT) with an Al$_2$O$_3$/AlN gate insulator layer deposited through atomic layer deposition was investigated. A favorable interface was observed between the selected insulator, atomic layer deposition–grown AlN, and GaN. A conventional p-type enhancement-mode GaN device without an Al$_2$O$_3$/AlN layer, known as a Schottky gate (SG) p-GaN HEMT, was also fabricated for comparison. Because of the presence of the Al$_2$O$_3$/AlN layer, the gate leakage and threshold voltage of the MIS-HEMT improved more than those of the SG-HEMT did. Additionally, a high turn-on voltage was obtained. The MIS-HEMT was shown to be reliable with a long lifetime. Hence, growing a high-quality Al$_2$O$_3$/AlN layer in an HEMT can help realize a high-performance enhancement-mode transistor with high stability, a large gate swing region, and high reliability.

Keywords: p-GaN E-mode HEMT; normally-off; gate insulator; lifetime; reliability

1. Introduction

High-electron-mobility transistors (HEMTs) are crucial for high-frequency and high-power applications because of their outstanding thermal properties, high breakdown fields, and high mobility levels. For fail-safe reasons, the power integrated circuits usually require high-performance normally-off devices [1]. Several strategies, such as the use of fluorine ion treatment [2], gate recess [3], and a p-type GaN cap layer [4,5], have been employed in normally-off HEMT devices. Normally-off devices fabricated with p-GaN gate technology offer low on-state resistance and large positive threshold voltage. However, to uniformly etch away the p-GaN in the non-gated access region and to overcome the plasma-induced damage during the p-GaN removal are extremely challenging tasks. Therefore, several teams are investigating the p-GaN etching process, such as etching stop technique [6], oxidation technique [7], and H plasma technique [8]. A positive threshold voltage can be obtained in HEMTs with p-type GaN layers, without affecting channel mobility; therefore, strategies involving the use of a p-type GaN layer are widely considered as the most effective among the strategies mentioned above. However, uniformly etching p-GaN away from the ungated access region and mitigating plasma-induced damage [9] during p-GaN removal are challenging. Cl$_2$-based ion etching is typically used to remove the p-GaN layer. If the etching is imprecise, the surface becomes rough with plasma bumps and in-surface defects, which may cause gate lag [10]. To control the etching depth, an AlN etch stop layer [5] is inserted between the p-GaN and barrier layers. This helps achieve highly...
selective etching to obtain superior etching uniformity, lower gate leakage, and lower dynamic on-resistance. Usually, the low hole concentration of p-GaN limits the threshold voltage; when this occurs, the resulting product is unsatisfactory practical applications. Moreover, the p–n junction gate turns on at strong forward bias, leading to a considerably high gate leakage current. In this study, to minimize the defects that may arise after p-GaN etching and increase the gate swing region, we deposited Al₂O₃ and AlN layers [11] on the surface of the device through atomic layer deposition (ALD); these layers also improved the device performance, increased the turn-on voltage, reduced the gate leakage current, and increased the device stability at high temperatures.

2. Device Structure

The HEMT structures used for proposed devices were grown on 6-inch Si (111) substrates through metal–organic chemical vapor deposition (MOCVD). A 300-nm-thick undoped GaN channel was deposited on top of a 4-μm-thick undoped GaN buffer transition layer. Subsequently, a 12-nm-thick Al₀.₁₇Ga₀.₈₃N layer, a 1-μm-thick AlN layer, and a 70-nm-thick p-type GaN top layer were deposited. The Al₂O₃/AlN interlayer was deposited through ALD. A schematic representation of the device is shown in Figure 1a.

The device was thermally annealed in an MOCVD chamber at 720 °C for 10 min in a N₂ atmosphere. The activated Mg concentration was determined to be 1 × 10¹⁸ / cm³ using the Hall measurement. The device was fabricated using mesa isolation with inductively coupled plasma (ICP) in the first step. Second, a p-GaN layer was etched through ICP etching with Cl₂/BCl₃/SF₆ as the etching gas. When the mixed gas reached the AlN layer, the SF₆ plasma [12] reacted with the Al atoms and formed a thin AlF₃ etch stop layer. Subsequently, the sample was soaked in a diluted HF/NH₄F solution to remove AlF₃. Then, a Ti/Al/Ni/Au (25/120/25/150 nm) ohmic metal stack was deposited through electron beam (e-gun) evaporation to serve as the source and drain; the metal stack was annealed at 875 °C for 30 s in a N₂ atmosphere in an RTA system, and the contact resistance of the MIS-HEMT and SG-HEMT were 7.6 × 10⁻⁶ and 8.1 × 10⁻⁶ Ω-cm², respectively. The oxide/insulator layer Al₂O₃/AlN (9/2.5 nm) was deposited through ALD, as shown in Figure 1b. In addition, Trimethylalumina, O₂, and N₂ were used as metal precursors, O and N source, respectively. The RF power and chamber temperature were 60 W and 300 °C. Then, an ohmic via was etched using buffered oxide etching. Ti/Au (25/120 nm) layers were then deposited through e-gun evaporation to serve as gate electrodes. By contrast, the gate metal of the SG-HEMT was just a deposited Ti/Au (25/120 nm) layer.

Figure 2 shows the conduction bands of the MIS-HEMT and SG-HEMT, which were obtained through TCAD simulation. The aim of this study was to increase V⁺ with and the gate voltage swing of the device by using Al₂O₃/AlN to increase the conduction band. The 2DEG height of the MIS-HEMT was more than that of the SG-HEMT, which resulted in the MIS-HEMT exhibiting better characteristics than the SG-HEMT.

![Figure 1](image_url)

**Figure 1.** (a) Schematic of the device structure with L₇/G₇/G₁₀/W₇ = 2/4/10/100 μm. (b) transmission electron microscopy (TEM) photograph of the device.
higher drain current density and on/off ratio than the SG-HEMT. The off-state breakdown voltage of 656 V. A comparison of the two devices shows that the MIS-HEMT had a higher off-state breakdown voltage than the SG-HEMT. The off-currents of the MIS-HEMT and SG-HEMT were 6 × 10⁻⁶ and 2 × 10⁻⁴ mA/mm, respectively, at V_DS = 10 V, as shown in Figure 3b. The I_DS–V_DS characteristics show that the AlN/AlGaN layer had a high gate voltage swing of more than 20 V [13]. To determine the device reliability, we measured off-state breakdown voltage; when measuring the off-state breakdown voltage, the device gate must be biased to 0 V to ensure that the device is in the off state. The results are plotted in Figure 3d. Because the Al₂O₃/AlN layer exhibited an effect similar to passivation and minimized any damage that might have been caused by etching, the Al₂O₃/AlN gate device had a high off-state breakdown voltage of 656 V.

To analyze the higher off-state breakdown voltage of the MIS-HEMT, we simulated the electric field distributions of the MIS-HEMT and SG-HEMT using TCAD. Figure 4 shows the schematic cross-sections of the two devices. The electric field was always concentrated at the gate edge in the drain side, and the electric field distributions of both devices were simulated at V_DS = 10 V. A comparison of the two devices shows that the electric field of the MIS-HEMT was low at the gate edge owing to the electric field being dispersed by the insulator layer. Negative charges appeared at the interface between the insulator and AlGaN owing to the negative polarization, which reduced the electric field near the gate edge at the drain side [14]. Consequently, MIS-HEMT had a higher off-state breakdown voltage due to the presence of the AlN/Al₂O₃ stack.

Figure 2. Energy band diagrams of schottky-gated high electron mobility transistor (SG-HEMT) and metal–insulator–semiconductor-high electron mobility transistor (MIS-HEMT) obtained through TCAD simulation.

3. Experimental Result and Discussion

For examining the effect of the Al₂O₃/AlN/p-GaN interface on device performance and for investigating the relationship of the AlN layer formed through ALD with an AlN etch stop layer at the sidewall and ungated region, we measured the I–V characteristics of the devices. Because an Al₂O₃/AlN layer can fill the nitrogen vacancies on the surfaces of p-GaN and AlN, depositing an Al₂O₃/AlN layer had the same effect as passivation. The I–V curve revealed that the gate leakage current was suppressed. Furthermore, because the polarization effect was enhanced due to the presence of the Al₂O₃/AlN layer, the MIS-HEMT had a higher drain current density and on/off ratio than the SG-HEMT. The off-state drain currents of the MIS-HEMT and SG-HEMT were 6 × 10⁻⁶ and 2 × 10⁻⁴ mA/mm, respectively, at V_GS = 0 V and V_DS = 10 V, as shown in Figure 3a. The I_DS–V_DS characteristics are shown in Figure 3b. The saturated drain currents of the MIS-gate and metal-gate devices were 363 and 247 mA/mm at V_DS = 10 V. Figure 3c shows the MIS-gate HEMT data. The figure indicates that the Al₂O₃/AlN layer had a high gate voltage swing of more than 20 V [13]. To determine the device reliability, we measured off-state breakdown voltage; when measuring the off-state breakdown voltage, the device gate must be biased to 0 V to ensure that the device is in the off state. The results are plotted in Figure 3d. Because the Al₂O₃/AlN layer exhibited an effect similar to passivation and minimized any damage that might have been caused by etching, the Al₂O₃/AlN gate device had a higher off-state breakdown voltage of 656 V.

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Figure 3. (a) Log-scale $I_{DS}$–$V_{GS}$ transfer characteristics, (b) $I_{DS}$–$V_{DS}$ output characteristics, (c) $I_{GS}$–$V_{GS}$ characteristics, and (d) off-state breakdown voltages of the MIS-HEMT and SG-HEMT.

Figure 4. Electric field distributions of the SG-HEMT and MIS-HEMT simulated using TCAD.

Typical C-V characteristics were measured at 500 kHz, as shown in Figure 5. As the gate bias increases above a certain voltage, the capacitance value starts increasing and satu-
rates. MIS-HEMT showed higher capacitance than SG-HEMT due to the Al₂O₃/AlN stacking. Figure 6a shows the dynamic on-resistance to static on-resistance ratio (R_{Dynamic,on}/R_{Static,on}) at different quiescent gate voltages. There are two bias conditions that must be considered: pulse voltage (V_{GSP}, V_{DSP}) and quiescent voltage (V_{GSQ}, V_{DSQ}). During the measurement, when the pulse voltage switched to the quiescent voltage rapidly with a 2 µs pulse width and 200 µs period, the charge carriers were trapped by defects. The quiescent gate bias was swept from 0 to −15 V in increments of −5 V. As seen in the figure, the MIS-HEMT had a lower dynamic Ron than the SG-HEMT; the MIS-HEMT had a dynamic Ron of 1.18, whereas the SG-HEMT had a dynamic Ron of 2.13. Therefore, the MIS-HEMT had a lower surface trap density surface, which inhibited current collapse. In this study, forward TDDB measurements were performed on the MIS-HEMT to assess the strength of the Al₂O₃/AlN gate dielectric. Figure 6b shows the variation in gate current during the TDDB experiments at three different gate voltages (14, 15, and 16 V). The gate current was initially low, owing to the accumulation of negative charges under the gate. Then, the gate leakage current became noisy owing to the formation of a percolation path. This was followed by a sudden increase in the gate leakage current owing to the hard breakdown of the gate dielectric [15]. A Weibull plot was drawn based on the time-to-breakdown distributions. The slope shows a tight distribution and less variability, as shown in Figure 6c. Moreover, lifetimes of 1% and 63.2% were investigated and are shown in Figure 6d. The gate leakage mechanisms at the measured gate bias region were determined to be 8.5 V at a failure rate of 63.2% and 6.1 V at a failure rate of 1%. Therefore, the MIS p-GaN can effectively suppress the trapping/detraping behavior and then enhance the gate reliability. Figure 7 compares the V_{G,BD}–I_{G} characteristics of the MIS-HEMT with that of other reported p-GaN gate HEMTs [5,16–22]. The MIS-HEMT fabricated in this study exhibited the highest V_{G,BD} and lowest gate leakage current.

![C–V characteristics of SG-HEMT and MIS-HEMT.](image)

Figure 5. C–V characteristics of SG-HEMT and MIS-HEMT.
Figure 6. (a) Gate lag behavior and dynamic Ron, (b) TDDB gate current with three different gate voltages, (c) Weibull plot of the time-to-breakdown distributions, and (d) lifetime prediction with failure rate of 63.2% and 1% of MIS-HEMT.

Figure 7. Comparison between the $V_{G_{BD}}$–$I_G$ characteristics of the proposed device and those of other devices [5,16–22].
4. Conclusions

A normally-off p-GaN HEMT with an Al2O3/AlN layer was investigated. The device exhibited excellent I–V characteristics. The turn-on voltage was higher than 20 V, with a threshold voltage of 3 V and a high saturation drain current of approximately 363 mA/mm. Moreover, the gate leakage current and instability were suppressed. The device off-state breakdown voltage in the MIS gate was increased because of the presence of the Al2O3/AlN layer deposited using ALD; this layer helped form an excellent interface between p-GaN and AlN. The lower trap density and trapping/detrapping effects were analyzed using pulse measurement. Overall, an Al2O3/AlN dielectric gate layer considerably improves the performance, reliability, and stability of HEMTs. Therefore, the as-developed design has a high potential for use in the manufacture of normally-off p-GaN gate HEMTs, which would allow them to be used in practical applications.

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