Testability-Aware Low Power Controller Design with Evolutionary Learning

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Abstract—XORNet-based low power controller is a popular technique to reduce circuit transitions in scan-based testing. However, existing solutions construct the XORNet evenly for scan chain control, and it may result in sub-optimal solutions without any design guidance. In this paper, we propose a novel testability-aware low power controller with evolutionary learning. The XORNet generated from the proposed genetic algorithm (GA) enables adaptive control for scan chains according to their usages, thereby significantly improving XORNet encoding capacity, reducing the number of failure cases with ATPG and decreasing test data volume. Experimental results indicate that under the same control bits, our GA-guided XORNet design can improve the fault coverage by up to 2.11%. The proposed GA-guided XORNets also allows reducing the number of control bits, and the total testing time decreases by 20.78% on average and up to 47.09% compared to the existing design without sacrificing test coverage.

I. INTRODUCTION

The scale and complexity of integrated circuits (IC) continue to grow thanks to the ever advanced semiconductor technologies. However, the associated large volume of test data to retain satisfactory test coverage leads to significant test cost. To mitigate this issue, a large amount of test compression techniques were proposed in the literature [1]–[11]. Nowadays, the mainstream technique is to store the compressed test patterns on the automated test equipment (ATE) and expand them on-chip before loading onto scan chains.

At the same time, with the continuous downscaling of transistor size, the circuit in scan test mode may behave quite differently from that in functional mode. In particular, scan test patterns could induce much higher switching activities than functional patterns, leading to unnecessary test yield loss. To address this critical problem, it is essential to consider the problem of test data compression and the problem of low power test together. Consequently, various low power test data compression solutions were proposed [12]–[22]. Among these works, the design of low power test controller has been widely adopted by commercial tools. The basic idea is to use a control block to output gating (masking) signals to scan chains such that they can be either connected with the decompressor or fed by a constant value of 0 (1) on a per pattern basis [13].

Both test compression and low power test control techniques exploit the fact that scan test patterns often feature a large portion of unspecified bits. Consequently, we could use a decoder (instantiated as LFSR reseeding structure [13], [15] or XORNet [13], [15]) with a small number of control bits to obtain the gating signals in low power test controller. Take XORNet in [13], [15] as an example (see Fig. 1), the gating signal for a specific scan chain is the XOR-ed output from certain control bits. When we need to drive the scan chains with specified bits from the decompressor, the control bits should be configured in a way that the gating signals for these scan chains are all 1’s. The remaining gating signals are determined by both the XORNet structure and the other control bits.

In order to minimize the impact of the linear dependency between different gating signals, the conventional XORNet design will evenly distribute the scan chains to certain XORNet control bits (e.g., 3) [2], [13], [23]. Such configuration implicitly assumes uniform XOR operand setting and equal encoding capacity of each scan chain. In practice, different scan chains in a circuit have distinct encoding requirements and they also vary among circuits. Consequently, the number of control bits is usually set conservatively high to ensure high encoding capability (e.g., 25 control bits for a circuit with 128 scan chains), leading to sub-optimal controller design.

In this paper, we take the above issue into consideration and propose a testability-aware low power controller design with evolutionary learning techniques. The proposed method implicitly extracts testability information via applying genetic algorithm (GA) on the sampled test cubes, and customizes XORNet-based low power controllers for different circuits under test. The proposed GA-guided XORNet design outperforms existing solutions by a significant margin across different settings.

The contributions of this paper are summarized as follows:

- We use fault sampling to generate sampled test cubes and extract the scan chain usage distribution that embeds testability information.
- We propose to apply the genetic algorithm on sampled test cubes to explore a better XORNet structure for the low power test controller design. The genetic algorithm operations are designed specifically for XORNet structures.
- We apply GA-guided XORNet design as the low power test controller for various industrial circuits and our experimental results show significant improvements in terms of test coverage, test time and control bit count.

We organize the remainder of this paper as follows. We review related works in Section II Section III introduces the conventional XOR-based low power test controller design, which motivates the proposed genetic algorithm for XORNet designs presented in Section IV. Then, Section V presents our experimental results on various industrial circuits. Finally, Section VI concludes this paper.

II. RELATED WORKS

In this work, we focus on scan shift power reduction and we discuss previous work in Section II-A. Then, Section II-B introduces preliminaries of evolutionary learning algorithms.

A. Low-Power Test Data Compression

Generally speaking, low shift-power testing techniques can be categorized into ATPG-based and DFT-based solutions. ATPG-based techniques (e.g., test vector reordering [19], adjacent filling [24], X-filling ATPG [25], [26]) try to minimize test patterns’ switching activities during test generation. However, these techniques
are not friendly with test compression and hence are rarely used for shift power reduction in practice. DFT-based low power test solutions, on the other hand, add design-for-test (DFT) hardware to reduce circuit switching activities during testing. Representative techniques include scan chain partitioning and modification [20], [27], clock gating [21], test point insertion [28], adaptive power scaling [29], and low power controller design [13], [14]. Among them, low power controller can be easily integrated into the test compression environment and is widely adopted in the industry. To be specific, the low power test controller is usually an LFSR-based or XORNet-based encoder, which expands the control bits into gating signals for every scan chain. The gating signals are AND-ed or OR-ed with the decompressed scan data for test power reduction. One example XORNet-based low power controller design is illustrated in Fig. 1. In this paper, we consider the above low power test compression architecture and try to improve its efficiency.

B. Evolutionary Learning Algorithm

Inspired by biological evolution, the common idea behind variants of evolutionary learning algorithms [30]–[33] is the same: given a population of individuals within some environment that has limited resources, competition for those resources causes natural selection. Among different evolutionary learning algorithms, genetic algorithm [34]–[36] is arguably the most popular one, which has been widely used for many optimization problems. Given an optimization problem, a population of candidate solutions is evolved towards better solutions. The solutions are in the form of strings of numbers, which is similar to chromosomes in genes, and can be mutated and altered. In order to evaluate the performance of different solutions, the fitness of the population is defined and serves as the optimization objective. The evolution usually starts from a population of randomly generated individuals and then steps into an iterative process. In each generation, the fitness function is applied to every individual; Based on these fitness values, potentially better candidates are stochastically chosen as the mating parents to seed the next generation. The recombination (i.e., crossover) and possibly randomly mutation are performed to produce new candidates. The new generation of candidate solutions is then used in the next iteration of the algorithm. This process is repeated until a candidate with sufficient quality is found or a previously set computational limit is reached.

III. XORNet-Based Low Power Controller Design

The binary vector \( \mathbf{x} \in \{0, 1\}^N \) of a test cube, wherein the \( i^{th} \) dimension indicates the \( i^{th} \) scan chain being specified (value 1) or not (value 0), represents the usage of scan chains. We use a XORNet to encode \( \mathbf{x} \) into compressed representation \( \mathbf{z} \) as the control bits, which will be loaded into the control register before decompression (See Fig. 1). The XORNet is a binary matrix, \( \mathbf{A} \in \{0, 1\}^{N \times M} \), defined by \( \mathbf{A}(i, j) = I(z_j = x_i) \) (the notation \( z_j \in x_i \) here means that the \( j^{th} \) control bit is the operand of XOR for the \( i^{th} \) scan chain). The row vector \( \mathbf{a}_i \) denotes the operands for the \( i^{th} \) scan chain. The control bits \( \mathbf{z} \in \{0, 1\}^M \) represents the controlling signal for XORNet, while the expanded scan chain gating signal \( \hat{\mathbf{x}} \in \{0, 1\}^N \) is the decoded signal from XORNet. Here we have the following step to get the control signals for test cubes:

\[
\mathbf{z} = \begin{cases} 
\text{XORSolver}(\mathbf{A}, \mathbf{x}), & \text{if } \mathbf{x} \text{ is solvable} \\
\text{None,} & \text{otherwise.}
\end{cases}
\] (1)

The XORSolver uses the Gauss-Jordan method, except that we consider the finite field of integers modulo 2. Note that we only solve the equations with the output being 1. What’s more, when the system has more than one solution, the unspecified control bits are random-filled. On the other hand, if the system has no solution, it counts as a failure case.

If the system is solvable, we can decode the control signals by XOR \( \mathbf{A} \) and \( \mathbf{z} \), and get the gating signal \( \hat{\mathbf{x}} \), wherein the \( i^{th} \) entry with value 1 indicates the \( i^{th} \) scan chain is driven by decompressor (i.e., the scan chain is activated/enabled):

\[
\hat{\mathbf{x}} = \mathbf{A} \oplus \mathbf{z}
\] (2)

The design goal of the XORNet-based low power controller is to minimize the power consumption as much as possible, within the minor loss of fault coverage. Usually, the power dissipation should meet the pre-defined requirements so that the overheating problem can be avoided during testing. To model the problem, we formally define a few indicators as follows.

Firstly, during ATPG, XORNet may fail to encode the test cubes. Specifically, the failure cases happen when the system \( (\mathbf{A}, \mathbf{x}) \) has no solution. We define Unsolvable (UNS) as the number of failure cases of XORNet encoding for a given test cube set:

\[
\text{UNS} = \#\{\text{XORNet Encoding Failure Case}\}
\] (3)

It should be noted that when all gating signals are decoded by \( 2k + 1 \) (\( k \) is an integer) of control bits, there is no UNS. The reason is that when all control bits are set with 1, the XOR outputs of \( 2k + 1 \) ones must be 1, causing all scan chains are activated.

Then we consider the cases where the power consumption exceeds the user-defined limit. Toggling the internal value of scan cell directly testing will cause circuit damaged, the ATPG process should specify the user-defined limit. Toggling the internal value of scan cell directly will be loaded into the control register before decompression (See Fig. 1). The XORNet is a binary matrix, \( \mathbf{A} \in \{0, 1\}^{N \times M} \), defined by \( \mathbf{A}(i, j) = I(z_j = x_i) \) (the notation \( z_j \in x_i \) here means that the \( j^{th} \) control bit is the operand of XOR for the \( i^{th} \) scan chain). The row vector \( \mathbf{a}_i \) denotes the operands for the \( i^{th} \) scan chain. The control bits \( \mathbf{z} \in \{0, 1\}^M \) represents the controlling signal for XORNet, while the expanded scan chain gating signal \( \hat{\mathbf{x}} \in \{0, 1\}^N \) is the decoded signal from XORNet. Here we have the following step to get the control signals for test cubes:

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Then we consider the cases where the power consumption exceeds the user-defined limit. Toggling the internal value of scan cell directly consumes power in scan testing. Because the excessive power during testing will cause circuit damaged, the ATPG process should specify a peak value as maximum instantaneous power consumption. To measure the shift cycle power in load and unload phases, we follow the definition of scan cell transition rate in [37], denoted as the Transition Rate at clock cycle \( t \):

\[
r_t = \frac{\#\{\text{Transition Cells}\} \text{ at } t}{\#\{\text{Cells}\}}
\] (4)

For example, one scan chain consists of 5 scan cells with internal states \( S = \{c_0, c_1, c_2, c_3, c_4\} \) and we assume the current internal states \( S_t = \{0, 0, 1, 1, 0\} \). In the next clock cycle, scan cell \( c_4 \) is loaded 1, the internal states should be \( S_{t+1} = \{0, 1, 1, 0, 1\} \). The scan cells \( c_1 \) and \( c_4 \) take falling transition from 1 to 0, the scan cells
c_3$ takes rising transition from 0 to 1, and other cells keep the state in the last clock cycle. Therefore, there are 3 transition cells among total 5 cells, the transition rate at clock $t$ is $r_t = 0.6$. The upper limit of $r_t$ is defined as Maximum Transition Rate ($R$), which is determined by the user. If the transition rate of a test cube at any cycle is larger than $R$, this test cube is counted as a High Power (HP) cube. The loss of test coverage is caused by discarding such HP cubes.

Evaluating transition rate for each test cube for all clock cycles is time-consuming. To efficiently estimate the power consumption, we use the ratio of the activated scan chains to the total number of scan chains to approximate the power consumption, named as Scan Chain Activated Rate (SCA).

$$SCA(x) = \frac{\# \text{ Activated Scan Chain}}{\# \text{ Scan Chain}} \in [0, 1]$$  \hspace{1cm} (5)

We then define Scan Chain Activated Exceeding Counts (SCAE) as the number of test cubes which exceeding the SCA limit, and the SCA as the average scan chain activated rate for a given test cube set.

$$SCAE = \# \{ x | SCA(x) > Limit \}$$  \hspace{1cm} (6)

$$SCA = \text{mean} \{ SCA(x) \}$$  \hspace{1cm} (7)

When a test cube activates too many scan chains or it cannot be encoded by the XORNet, the test cube is regarded as Unsuccessfully Encoding (UE) cube. The number of UE is the sum of SCAE and UNS, which can be calculated as:

$$UE = SCAE + UNS$$  \hspace{1cm} (8)

Not double to say, the primary objective of XORNet-based low power controller is to reduce the cases which violate the power requirements as much as possible. However, the conventional XORNet design is merely random and conservative. For example, given a circuit design with $N$ scan chains, $M$ ($M < N$) control bits will be assigned for XORNet, and 3 control bits are connected randomly to one scan chain, i.e.:

$$\hat{X}_i = z_j \oplus z_k \oplus z_p$$  \hspace{1cm} (9)

The random seed to generate XORNet is set as the number of scan chains by convention. Also, different scan chains in a circuit have distinct encoding requirements and they also vary among circuits. So the number of control bits is usually set conservatively high so that the low power controller does not cause high loss of test coverage. For example, 11 control bits are allocated for a circuit with 46 scan chains in the industrial tool.

Although such XORNet design is simple, it ignores circuit-specific testability characteristics and can be sub-optimal due to this fact. For example, the design of circuit is non-uniform, resulting in uneven distribution of scan chain usage. We analyze two test cases with the distribution of scan chain usage. For the Case 1, some scan chains can be frequently used, and consume around 16.0% of total specified chain counts, while some other scan chains are activated for less than 1.0% times. What’s more, the distribution of specified scan chain counts for two cases varies significantly. To be specific, the usage peak value appears on scan chain #22 and #23 for the Case 1, but those scan chains are merely used in Case 2. In the following discussion, the distributions of scan chain usage are regarded as one form of circuit testability properties.

In general, different circuits maintain different testability properties, which implies a unitary XORNet design is unsatisfactory.

In this case, we need different control strengths for different scan chains. If a sufficient number of in-distribution scan chains sampled from a specific circuit are available, then in principle, Learning-based approach should be able to extract the underlying patterns and produce a better XORNet structure for this circuit.

Due to the logical properties of XOR operation, XORNet is neither differentiable, nor is its coding ability directly related to the number of control bits. Consequently, conventional optimization methods cannot be directly applied to XORNet design. For example, the gradient descent method cannot deal with the XOR encoding optimization problem. In this paper, we propose an evolutionary-learning-guided approach to search XORNet structure, which is elaborated in Section IV.

IV. Genetic Algorithm for XORNet

To realize the idea of customizing XORNets for different circuits in practice, we take the idea of genetic algorithm, one of the evolutionary learning approaches, with the following two reasons:

- One row of XORNet matrix $A$ corresponds to the XOR operand settings for one scan chain. Different rows are independent and do not interfere with each other. Consequently we can modify XORNet at the row level. If two XORNets are given, we can randomly exchange rows of two matrices and obtain a new XORNet. Such procedure can be modeled as the crossover operation in GA.

- For the $i^{th}$ scan chain, its control bits are determined by entries being 1 of $a_i$ ($a_i$ is the $i^{th}$ row of XORNet matrix $A$). To explore different setting of control bits for the scan chain, one can flip the entries of $a_i$. Such entry-wise operation can be regarded as one variation of mutation in GA.

To this end, we propose to use GA for searching better XORNet structure in low power controller design. Fig. 2 shows the overview of the GA pipeline and the GA learning procedure is illustrated in Algorithm 1. We elaborate the GA for XORNet-based low power controller design in the following sub-sections.

A. Data Preparation

To enable GA learning, we have to prepare a pool of test cubes $X$, which approximates the distribution of test cubes in ATPG pipeline. As the XORNet structure is to be determined, the final circuit netlist...
Algorithm 1: GA Learning for Low-Power Test Compression

**Input:** Sampled Test Cubes $\mathbf{X}$, # of Scan Chain $N$, # of Control Bits $M$, # of Individuals $Size_{Pop}$, # of Parents $Size_{Parents}$, # of Parents $Size_{Children}$, # of generations $Size_{Gen}$, Mutation ratio $\gamma$, Coefficient $\lambda$.

**Output:** XORNet $\mathbf{A}$ searched by GA.

```plaintext
/* Initialize Population */
1 $\{\mathbf{A}\} = \text{InitPop}(N, M, Size_{Pop})$;
2 $i = 1$;
/* Define Fitness Function */
3 $\ell = \text{UE} + \lambda \times SCA$;
4 while Not Convergence or $i \leq Size_{Gen}$ do
5     /* Fitness Calculation */
6     fitness = $\ell(\{\mathbf{A}\}, \mathbf{X})$;
7     /* Select Parents to Mating Pool */
8     $\{\mathbf{A}_{parent}\} = \text{top}(\{\mathbf{A}\}, \text{fitness}, Size_{Parents})$;
9     /* Crossover */
10    $\{\mathbf{A}_{child}\} = \text{CrossOver}(\{\mathbf{A}_{parent}\}, Size_{Children})$;
11    /* Mutation */
12    $\{\mathbf{A}_{child}\} = \text{Mutation}(\{\mathbf{A}_{child}\}, \gamma)$;
13    /* New Population */
14    $\{\mathbf{A}\} = \{\mathbf{A}_{parent}\} + \{\mathbf{A}_{child}\}$;
15    $i++$;
6 end
/* Best XORNet */
12 $\mathbf{A} = \text{top}(\{\mathbf{A}\}, \text{fitness}, 1)$;
13 return $\mathbf{A}$;
```

is not available during the GA training stage, hence we cannot directly run ATPG and sample the exact test tubes. As the low-power controller occupies only a small part of the final circuit, we consider applying fault sampling on the original circuit netlist. Specifically, we randomly select a small subset of faults (less than 4.0% of the total faults) and run ATPG, extract their scan chain usage information, and use them as the training dataset for GA learning. The key observation is that a small portion of faults are already sufficient to reflect the statistic of scan chain usage and is able to help GA search a better XORNet structure than conventional XORNet.

### B. GA Specifications

1) **Population Initialization:** The population consists of multiple XORNet set $\{\mathbf{A}\}$, wherein each XORNet matrix $\mathbf{A}_i \in \{0, 1\}^{N \times M}$ represents an individual solution. Because the number of 1’s directly affects the hardware overhead of XORNet (the more 1’s, the larger the area), we restrict the sparsity of $\mathbf{A}$ so that on average there are 3 control bits being the operands for each scan chain. In other words, 3 entries of $\mathbf{a}_i$ are 1’s and the remaining entries are set as 0. Through this initialization method, we ensure that the area of XORNet searched by the GA is comparable to the one by the previous works.

2) **Fitness Function:**

The most significant factor affecting the search space is the size of population. With more individual solutions in the population, we have more diversity in the searching space. But with too many individuals the convergence speed may be slow. In our experiments, we observe that setting the population size as 40 is enough to get a desired results across different test circuits.

2) **Fitness Function for Low-Power Test Design:** The objective of GA learning has two-fold: Firstly, we want to improve the XORNet encoding capacity so that it can merge more test cubes during ATPG. From this aspect, we use $UE$ (defined in Eq. 5) as indicators, which is the number of failure cases of XORNet encoding and validation of the power requirement. Note that in order to efficiently estimate the power consumption, instead of the transition power, we use $SCA$ defined in Eq. 6. Secondly, except for the use-defined power limit, we also want the average power during test to be as low as possible. Thus, $SCAE$ (defined in Eq. 7) should be minimized. Based on the above considerations, we set the fitness function as the sum of $UE$ and $SCA$, and use GA learning to minimize such fitness function, as shown in Eq. 10. In our experiments, we set coefficient $\lambda$ as 100 to scale up the range of $SCA$ from $(0, 1)$ to $(0, 100)$.

$$Fitness\ Function = UE + \lambda \times SCA \quad (10)$$

3) **Mating:** To select the individuals as parents to generate children (offspring), we evaluate each individual on test cube set $\mathbf{X}$ and put the ones with low fitness into the mating pool. The utility function $top()$ (line 6 in Algorithm 1) ranks the fitness of individuals from the lowest to the highest and selects the top XORNets with the size of $Size_{Parents}$ (5 in our experiments) accordingly. The set $\{\mathbf{A}_{parent}\}$ being selected is the mating pool for generating children.

4) **Crossover:** As discussed before, each row of individuals is independent for XORNet decoding. Consequently, To re-combine two XORNets, one feasible way is to do crossover operation at the row level. Specifically, given two $i^{th}$ row vectors $\mathbf{a}_i^{p1}$ and $\mathbf{a}_i^{p2}$ (the superscript indicates the identity of parent individual) from the parent $\mathbf{A}^{p1}$ and the parent $\mathbf{A}^{p2}$, one of them is randomly picked and designated as $\mathbf{a}_i^c$, the $i^{th}$ row of children XORNet $\mathbf{A}^c$:

$$Crossover: \mathbf{a}_i^c = \text{RandomPick}(\mathbf{a}_i^{p1}, \mathbf{a}_i^{p2}) \quad (11)$$

The illustration of crossover is shown in Fig. 4(a). Such crossover results in the rows of $\mathbf{A}^c$ either from $\mathbf{A}_i^{p1}$ or from $\mathbf{A}_i^{p2}$. It gives the chance that the children inherit good XORNet connection settings from both parents and perform better than parents.

5) **Mutation:** In order to get better solutions, we use mutation to slightly alter the obtained children solutions. As the representation of solution is all binary, bit-flip fits well to XORNet mutation. As shown in Fig. 4(b), given the $i^{th}$ row of children XORNet, we select
TABLE I
TESTING CIRCUIT CHARACTERISTICS (CBC: CONTROL BIT COUNTS, PC: PATTERN COUNTS, TC: TEST COVERAGE)

| ID   | # Gate | # Chain | # Cell | R=50.0% | R=30.0% |
|------|--------|---------|--------|---------|---------|
|      | CBC    | PC      | TC     | CBC     | PC      | TC     |
| C1   | 86,917 | 33      | 328    | 9       | 1,263   | 98.57% | 16     | 1,323   | 97.97% |
| C2   | 121,259| 46      | 358    | 11      | 2,660   | 96.01% | 23     | 2,539   | 95.82% |
| C3   | 782,934| 81      | 329    | 20      | 10,893  | 97.05% | 40     | 13,426  | 96.91% |
| C4   | 54,930 | 100     | 360    | 25      | 5,171   | 94.79% | 50     | 2,027   | 88.35% |
| C5   | 107,438| 128     | 328    | 25      | 1,393   | 99.47% | 64     | 1,154   | 98.80% |
| C6   | 136,112| 380     | 40     | 56      | 3,850   | 93.80% | 190    | 3,876   | 94.05% |
| C7   | 91,115 | 400     | 31     | 80      | 2,471   | 98.10% | 200    | 2,540   | 98.00% |
| C8   | 104,155| 413     | 330    | 82      | 661     | 99.56% | 82     | 656     | 99.51% |
| C9   | 86,915 | 500     | 25     | 100     | 2,451   | 98.59% | 250    | 2,558   | 98.49% |
| C10  | 136,872| 760     | 20     | 114     | 3,952   | 93.66% | 152    | 3,952   | 93.66% |

the positions of elements to be flipped with the probability of $\gamma$ (set as 0.05 in our experiments):

$$\text{Mutation: } a_i = \text{RandomFlip}(a_i, \gamma)$$  

After crossover and mutation, we combine the parent set \(\{A_{\text{parent}}\}\) and the children set \(\{A_{\text{child}}\}\) together as the new generation. Then GA steps into the next evolution iteration. The learning stops when the fitness value of generations is converged or GA runs for predefined \(\text{Size}_\text{Gen}\) generations. At last, the XORNet with the lowest fitness value is selected as the final output (line 12 in Algorithm [1]).

C. Low-Power Requirements

So far, we discuss a stand-alone XORNet as the decoder. The implicit power limit, in this case, is that the decoded test stimuli toggles 25.0% test cells randomly on average, as the probability of output of XOR gate being 1 is 50.0%. When users require more stringent power consumption limit, previous works add AND gates to control the probability of scan chain being activated. To be specific, a XORNet A and a ANDNet B are combined together so that two outputs from XOR gates are ANDeD to get the final output. The proposed GA scheme can be easily generalized to these cases, wherein we fix the ANDNet B and let GA search for XORNet A.

V. EXPERIMENTS

A. Circuit Datasets and Baselines

We compare the proposed testability-aware XORNet design searched by GA with the standard XORNet design adopted by commercial tools on 10 industrial circuit designs, ranging in size from 54K to 782K gates. Table I summarizes the circuit characteristics including the number of gates (# Gate), the number of scan chains (# Chain), the maximum number of scan cells for each scan chain (# Cell). Besides, we consider the test compression with two low power requirements: maximum transition rates $R = 50\%$ and $R = 30\%$, which represents the peak shift cycle power limit. When the shift cycle power limit is 50.0%, the one-level of XORNet structure is deployed. When the shift cycle power limit is 30.0%, the two-level XORNet structure is deployed.

With two different transition rates, two types of conventional XORNet are generated as baselines. In our experiments, we use the number of scan chains as the random seed to generate the XORNets. Therefore, two different circuits with the same number of scan chains share the same XORNet-based low power controller design.

To detect multiple faults with a single test pattern, we consider the incremental merging scheme. To be specific, the ATPG procedure generates some test cubes, and some eligible test cubes are incrementally merged into a test pattern to cover other faults as much as possible without losing any test coverage. Such procedure is executed only if the merging pattern activates scan chains less than the maximum SCA.

As shown in the second and third columns in Table I we report the control bit counts (CBC) of test compression structures, ATPG pattern counts (PC) and test coverage (TC) when the conventional XORNet is used as the low power controller.

B. GA Hyper-parameters and Fitness Function Convergence

We try different hyper-parameter settings for GA and observe that as long as the population size is set to be relatively large (i.e., > 20), the fitness function will easily be converged. Consequently, the GA hyper-parameters for experimental results shown in this section are all set as the same as follows: number of generations \(\text{Size}_\text{Gen} = 20\), population size \(\text{Size}_\text{Pop} = 40\), number of parents for mating pool \(\text{Size}_\text{Parents} = 5\), number of children \(\text{Size}_\text{Children} = 25\), mutation ratio $\gamma = 0.05\$, coefficient $\lambda = 100$.

In Fig. 5 we sample one circuit (C1) and trace the fitness function values during evolution. Note that a similar trend of fitness value on other circuits is observed. As the fitness function has two components $UE$ (blue dots) and $SCA$ (green dots), we show them independently in the figure. In each generation ($x$-axis), the fitness values ($y$-axis) for all 40 XORNet solutions are demonstrated, while the fitness values of the best individuals for all generations are connected as line charts (See the blue line and green line in the figure). As can be observed in this figure, both $UE$ and $SCA$ go down and converge within 20 generations. Because we prioritize $UE$ optimization in our fitness function, it can be seen in the figure that the final XORNet solution has a minimum $UE$, and may have sub-optimal $SCA$.

C. Effectiveness of GA on XORNet Design

As demonstrated in Fig. 6 different circuits exhibit different testability properties. The testability-aware low power XORNet takes these properties into account by applying genetic algorithm on sampled test cubes, thus improve the encoding capability for a specific circuit. In this subsection, we demonstrate the effectiveness of GA in terms of the test coverage, testing time and the number of control bits.

1) Improve Test Coverage: The low power controller encoding process is trying to find a qualified solution of linear equations that all pre-specific gating signals should be assigned the correct value.
after decoding. At the same time, the number of activated scan chains by gating signals cannot exceed the maximum SCA, otherwise, the test cube will be counted as HP and be dropped during ATPG.

Table I compares GA-guided XORNet with baselines w.r.t the test coverage. We list four circuits (C1-C4) with HP after coupling the low power test compression structure, while the other cases (C5-C10) are ignored because they have no HP. When the maximum transition rate \( R = 50.0\% \), the GA learned encoding XORNet can reduce almost all HP and improve by 2.11\% test coverage at most. When \( R = 30.0\% \), the GA-guided XORNet improves test coverage up to 0.63\%. Comparing with the conventional XORNet, the average TC on 4 circuits increase by 1.25\% and 0.43\% under two different low power limits, which is significant.

Overall, compared with the conventional low power test compression structure, with embedded testability information, the GA-guided low power controller can avoid activating more than necessary scan chains for the test cubes which are regarded as HP on the former structure. Therefore, the GA learned controller can improve the test coverage.

2) Reduce Testing Time under The Same Coverage: The design of test compression structure targets reducing test data volume and testing time. In this testability-aware low power test compression structure, the controller keeps the current control bits during shifting each test pattern. For each pattern, the load values should be shifted in bits by bits. Thus, the total testing cycle indicating testing time is noted as:

\[
\text{Total Testing Cycle} = \left( \frac{\text{CBC} + D}{C_{in}} + \# \text{Cell} \right) \times \text{PC} \quad (13)
\]

The constant \( D \) represents the number of configuration bits for test pattern decompression, which is determined by circuit size. \( C_{in} \) is the number of input channels of test compression structure, and all circuits are configured with the same \( C_{in} = 1 \). The CBC, \# Cell and PC are shown in Table II. The low power controller needs \( (\text{CBC} + D/C_{in}) \) cycles to configure the control register and testing register and \#Cell cycles to shift in the current test pattern.

To ensure that the same volume of faults are covered when testing the circuits with the conventional and testability-aware low power compression structures, the new test cubes will be generated until the ATPG process reaches the target test coverage. The target test coverages for each circuit with two maximum transition rates are set as the two columns under TC in Table I, respectively. Table II shows that the testability-aware low power test compression structure can reduce at most 45.23\% and 15.16\% pattern counts with \( R = 50.0\% \) and \( R = 30.0\% \). According to the Eq. (13) without modifying the low power controller structure, the variation of total testing cycles is only related to the pattern counts, i.e. reduce 45.23\% and 15.16\% testing cycles. On average, the evolutionary testing compression approach save 10.18\% and 6.09\% testing time when the maximum transition rates are 50.0\% and 30.0\%, respectively.

From the above, the GA-guided low power controller can reduce the number of activated scan chains for most test cubes. Thus, the incremental merging process is carried out more times until reaching the maximum SCA. More test cubes can be merged into a test pattern and the pattern counts (PC) can be reduced.

3) Reduce Control Bit Counts to Reduce Testing Time: Different from the conventional XORNets, as XORNets generated by GA utilizes testability properties, the latter can use fewer control bits to reach the same test coverage. We try to reduce the control bit counts to save testing cycles further. To explore the influence of CBC reduction on test coverage and XORNet encoding capability, we take the cases with relatively high TC and more \# Chain as examples (i.e. C8 and C9) in Table III. The target test coverage for C8 and C9 are set to 99.56\% and 98.57\%, respectively, and the minimum control bit counts have been reduced by 75.61\% and 70\%, which means the testability-aware network only takes about 30\% of original control bit counts to achieve the same coding capability with the randomly connected XOR encoding network. It should be noted that when CBC is excessively reduced, the test coverage cannot meet the target test coverage. Therefore, the minimum CBCs for C8 and C9 are 20 and 30 respectively.

However, the total testing cycle is determined by pattern counts, the longest scan chain and the circuit structure, as the cycle metrics Eq. (13). By restricting the number of control bits, the XORNet encoding capability decreases and fewer test cubes are merged into a pattern, so that it will lead to the increase of pattern counts to consume testing time. For example, if the CBC of C8 is reduced by 75.61\% (from 82 to 20), the test cycle reduction does not reach the optimal value. We observe that the XORNet with 26.83\% CBC reduction has minimal testing cycles, as shown in Figure 6.

It is not recommended that reducing control bits for circuits that
control bits to further reduce the testing time at most. The best results according to the above analysis of C8 and C9, the low power circuits (C1-C4) whose CBCs are less than 50 so that exceed the maximum SCA. Restricting control bit strategy when the maximum transition rate is equal to 50.

This indicator directly corresponds to the test coverage strengths on different scan chains.

Table IV

| ID | CBC | Reduction | PC | TC | Cycles | Reduction |
|----|-----|-----------|----|----|--------|-----------|
| *82* | – | 661 | 99.56% | 327,195 | – |
| 82 | 0.00% | 362 | 99.56% | 179,190 | 45.23% |
| 70 | 14.63% | 367 | 99.56% | 177,261 | 45.82% |
| 60 | 26.83% | 366 | 99.56% | 173,118 | 47.09% |
| 50 | 39.02% | 393 | 99.56% | 181,959 | 44.39% |
| 40 | 51.22% | 418 | 99.56% | 189,354 | 42.13% |
| 30 | 63.41% | 443 | 99.56% | 196,249 | 40.02% |
| 20 | 75.61% | 501 | 99.56% | 216,933 | 33.70% |
| 10 | 87.80% | 649 | 99.48% | 274,527 | 16.10% |

*Baseline: Test with the conventional XORNet

have few scan chains and CBC, because the reduction of CBC compression structures may activate more percentage of scan chains so that exceed the maximum SCA. Restricting control bit strategy is more suitable for circuits with more scan chains. Therefore, the circuits (C1-C4) whose CBCs are less than 50 are not considered. According to the above analysis of C8 and C9, the low power controller with the least CBC may not reach the minimal testing cycles. In the Table IV we generate the testability-aware low power test compression structures for the circuits and configure fewer control bits to further reduce the testing time at most. The best results are saving 47.09% and 36.11% testing time by reducing control bits when the maximum transition rate is 50.0% and 30.0%, respectively. When \( R = 50.0\% \), the testability-aware approach can reduce 46.09% CBC to save about 20.78% testing cycles on average. Besides, for more power consumption limited situations \( R = 30.0\% \), GA can reduce 19.40% testing cycles by decreasing about 35.84% CBC.

D. GA-guided XORNet Analysis

In this section, we explore and analyze why GA-guided XORNet outperforms conventional XORNet from the perspective of control bit connection and scan chain activated frequency during ATPG.

Firstly, we show the number of scan chains controlled by each control bits for case C3 in Figure 7. As in the XORNet-based low power controller, the control bits are expanded into final gating signals for scan chains. Usually, the number of control bits is much less than the number of scan chains. In other words, one control bit will participate in the control of multiple scan chains. As can be observed from this figure, the conventional XORNet (the blue line) is configured randomly and each encoding bit controls a similar number of scan chains (i.e., around 12). On the contrary, the GA-guided XORNet (the red line) can differentiate different scan chain (i.e., a control bit can control 18 at most and 5 at least) and assign different numbers of control bits for each scan chain. Such results are in line with our expectation as GA-guided XORNet can exert different control strengths on different scan chains.

Secondly, to show more evidence of better encoding capacity obtained from GA-guided XORNet, we count which scan chain needs to be activated by successfully merged cubes during incremental merging. This indicator directly corresponds to the test coverage and reflects the coding ability of XORNet. The more activated times of scan chains, the more test cubes are generated and merged successfully which are able to detect more faults and improve the test coverage. In order to show the GA-guided XORNet advantage clearly, we take the case (C3) with the largest test coverage improvement as an example. As shown in Figure 8, GA-guided XORNet (the red bar) constantly outperforms the conventional XORNet (the blue bar) regarding the activated times of scan chain during ATPG. The relative improvement is essentially large on some scan chains (e.g., scan chain #37), which shows the benefit of GA-guided XORNet. Similar improvements are emerging in other cases.

To sum up, GA-guided XORNet is able to extract the testability properties from sampled test cubes, and rearrange the control bit...
connections so that the encoding capacity outperform conventional XORNet by a significant margin.

VI. CONCLUSIONS

In this paper, we propose to use an evolutionary learning algorithm to improve the performance of low power test compression. By applying the genetic algorithm on sampled test cubes to extract testability information, and further employing XORNet searched by genetic algorithm as the low power controller, the proposed design can achieve better encoding capacity of XORNet. The empirical results show that the GA-guided XORNet can improve test coverage by up to 2.11% and 0.63% when the maximum transition rate $R = 50.0\%$ and $30.0\%$, respectively. Meanwhile, the testability-aware low power controller allows merging more test cubes, which effectively decreases the testing time by 10.18% with $R = 50.0\%$ and 6.09% with $R = 30.0\%$ on average. Restricting the number of control bits can further reduce the testing cycles by 20.78% and 19.40% on average when the maximum transition rate is 50.0% and 30.0%, respectively. In conclusion, compared with the conventional low power controller, the testability-aware controller consisting of GA-guided XORNet can improve the test coverage and reduce testing cycles without loss of fault coverage.

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