RESEARCHING THE EFFICIENCY OF BUCK CONVERTER SYNCHRONOUS RECTIFIER

The object of study is synchronous buck-voltage converter with digital control system. One of the most problematic things is energy changing and transmission in converters to reach certain numerical range with minimal losses in the components of the electrical circuit. An enormous calculated parameters of electrical scheme. There was advised and described both structure and electrical scheme of synchronous converter, which, thanks to digital system, provides dates with more accuracy connected with an impact on working scheme. There was shown detailed analysis example with a numerical value for the certain elements of electrical scheme. It’s a fundament in order to choose certain parts of electrical scheme according to the certain categories.

During research there was used selection of hardware and software tools: elements for buck-converter – key, diode and capacitor; certain voltage and frequency range for microcontroller; control of the power keys of the circuit with the corresponding operating parameters for driver. There was analyzed and calculated all over the possible losses during the process bucking of the voltage to the certain level, an enormous losses in the components of the converter electrical scheme – induction coil, keys and capacitors. It’s an important part of synchronous buck-converter. There was calculated power losses and efficiency through the received graphics of keys commutation in electrical scheme. There were received graphic dependence of converter efficiency on output power; time characteristics of the control signal pulse-width modulation (PWM) and output voltage; dependence on the commutation losses. This is because advised synchronous converter has a set of features. Particularly analog to digital converter in the capacity of feedback, digital regulation system with a discrete step and rectification by replacing diodes with actively controlled switches. There are keys of low-side and high-side levels according to the passing voltage and current values. Therewith provides possibility for receiving more accuracy value. In comparison with analogic buck-converters, this converter has voltage parameter with fractional error.

Keywords: buck converter, digital control, buck converter losses, buck-converter efficiency, synchronous rectifier.

1. Introduction

Nowadays energy efficient projects are becoming more popular. An enormous converter, which can be used in photovoltaic power generation systems, renewable energy systems and a number of other systems. For example, modern aircraft use a lot of radio equipment for communication systems, navigation, landing, meteorological, avoiding the collision of aircrafts. For obvious reasons, the weight and dimensions of this equipment must be reduced. The traditional construction scheme uses one powerful transmitter and a number of switched antennas or antenna array. In addition, there is a constant integration of equipment in the direction of combining several systems within a single functional unit [1]. At the same time, of course, the weight and dimensions are reduced, but additional requirements are imposed on the element base.

Modern equipment is characterized by a high complexity. Device requires different voltages in order to supply its own component parts [2].

When there is electric power supply in order to use different voltage steps, it is important to use special converters (regulators). The problem for receiving different voltage supply values is in portable equipment.

There is in mains-powered devices can be build an electric power supply with the required voltage. By the way portable devices operate from stand-alone power sources and certain voltage stages can be received by using DC / DC (DC means direct current) converters.

Requirement in order to receive huge coefficient of efficiency is important for devices with a stand-alone power sources.

It is relevant to study the existing schemes of energy converter and carry out a comparative analysis, because the buck converters use the active modes for switching [3]. Thus, the object of research is synchronous buck converter with digital control system. The aim of the article is the researching of the scheme and developing the foundations for construction in order to reach high efficiency level of buck converter.
2. Methods of research

2.1. Engineering analysis of buck converter. There is in Fig. 1 an electrical principle scheme of the buck voltage converter. Power circuit of converter has transistor VT1. If the key switched on, output current, which flows through the inductance coil \( L \), rises. Inductance coil is coupling magnetic field energy. If the key switched off, coupled electrical energy in the inductance coil will be send to the capacitor \( C \) and load \( R_L \). Bypass diode \( VD_1 \) lets the pass for the current to flow.

In order to realize the scheme it is important to calculate nominals of the elements in the buck converter \([4, 5]\). Calculation would be finished with a certain parameters: maximal output current \( I_{\text{out,max}} = 0.522 \text{ A} \), frequency switching \( f_{\text{sw}} = 10 \text{ kHz} \), inductive current ripple factor \( LIR = 0.3 \), range of input voltage \( U_{\text{in}} = 7-24 \text{ V} \) and output voltage \( U_{\text{out}} = 6 \text{ V} \) \([6]\).

Inductance calculation is an important moment during converter projecting, insofar as there is dependence on values of maximal input \( U_{\text{in,max}} \) and output \( U_{\text{out}} \) voltage:

\[
L = \frac{U_{\text{in,max}} - U_{\text{out}}}{f_{\text{sw}}} \frac{I_{\text{out,max}}}{LIR \cdot I_{\text{out,max}}},
\]

\[
L = (24-6) \text{ V} \cdot \frac{1}{24 \text{ V} \cdot 10^4 \text{ Hz} \cdot 0.3 \cdot 0.522} = 2.87 \text{ mH},
\]

where \( f_{\text{sw}} \) – frequency switching transistor; \( LIR \) – inductive current ripple factor; \( I_{\text{out,max}} \) – maximal value of output current.

Peak current of the inductance coil \( I_{\text{peak}} \) solves as:

\[
I_{\text{peak}} = I_{\text{out,max}} + \frac{\Delta I_{\text{ind}}}{2},
\]

\[
I_{\text{peak}} = 0.522 \text{ A} + \frac{0.3 \cdot 0.522}{2} = 0.6 \text{ A},
\]

where \( \Delta I_{\text{ind}} = LIR \cdot I_{\text{out,max}} \) – variable inductance value.

Output capacitor with a maximum available amplitude swing of ripples of the output voltage \( \Delta U \) (accept \( \Delta U = 100 \text{ mV} \)):

\[
C_{\text{out}} = \frac{L}{(\Delta U + U_{\text{out}})^2 - U_{\text{out}}^2} \left( I_{\text{out,max}} + \frac{\Delta I_{\text{ind}}}{2} \right).
\]

\[
C_{\text{out}} = \frac{2.87 \text{ mH}}{(100 \text{ mV} + 6)^2 - 6^2} \left( 0.522 + 0.1566 \right) = 0.8 \text{ mF}.
\]

Duty cycle of the open state power key relative period of the pulse width modulation:

\[
D = \frac{U_{\text{out}} - 6 \text{ V}}{12 \text{ V}} = 0.5 = 50 \%.
\]

2.2. Synchronous rectifier. Pulse regulators are known as highly efficient power supplies. In order to increase their efficiency, it is important to understand the basic mechanism of power loss. This instruction for use explains the coefficients of electricity losses and methods of their calculation. This also explains how the relative importance of power loss factors depends on the switching power supply specifications \([2]\).

Fig. 2 shows a block diagram of a synchronous rectifier type of \( DC/DC \) converter \( \text{(DC means «direct current»)} \). Fig. 3 shows the waveform of the voltage node of the switch and the current waveform of the inductor. Striped lines are areas where losses can be explained.
The following nine factors are the main causes of power loss:
1) conduction losses caused by the on-resistance of the MOSFET $P_{ON-H}$, $P_{ON-L}$;
2) switching-loss in the MOSFET $P_{SW-H}$, $P_{SW-L}$;
3) reverse recovery losses in the body diode $P_{dss}$;
4) output capacitance losses in the MOSFET $P_{Coss}$;
5) dead time loss $P_{dead}$;
6) conduction losses in the MOSFET $P_c$;
7) operation losses caused by the integrated circuit (IC) control circuit $P_{IC}$;
8) conduction losses in the inductor $P_{L(OCR)}$;
9) losses in the capacitor $P_{CUT}$;

2.3. Buck converter losses

2.3.1. Conduction loss in the MOSFET. The conduction loss in the MOSFET is calculated in the A and B sections of the waveform in Fig. 3. As the high-side MOSFET is ON and the low-side MOSFET is OFF in the A section, the conduction loss of the high-side MOSFET can be estimated from the output current, on-resistance, and on-duty cycle. As the high-side MOSFET is OFF and the low-side MOSFET is ON in the B section, the conduction loss of the low-side MOSFET can be estimated from the output current, on-resistance, and off-duty cycle.

$P_{ON-H} = I_{on} \cdot R_{on-H} \cdot \frac{U_{out}}{U_m} [W]$

$P_{ON-L} = I_{off} \cdot R_{on-L} \left( 1 - \frac{U_{out}}{U_m} \right) [W]$

where $I_{on}$ and $I_{off}$ are minimal value of the induction current; $U_m$ – minimal value of the gate voltage; $f_m$ – transistor switching frequency; $L$ – inductance value.

2.3.2. Switching-loss in the MOSFET. The switching-losses can be calculated into the «C» and «D» sections or in the «E» and «F» sections of the waveform in Fig. 2. When the high-side and low-side MOSFET transistors are turn «ON» and «OFF» alternately, a loss is generated during the transition of the on-switching. Since the equation for calculating the area of the two triangles is similar to the equation for calculating the power losses during the rising and falling transitions, this calculation can be approximated using a simple geometric equation. The switching-loss $P_{SW-H}$ is calculated with the following equation:

$P_{SW-H} = \frac{1}{2} U_m I_{on}(t_{on} + t_{off}) f_m [W]$,

where $t_{on}$ and $t_{off}$ are High-side MOSFET rise time and High-side MOSFET fall time.

When the low-side MOSFET is turned ON by the gate voltage while the body diode is energized and then the FET is turned OFF by the gate voltage, the load current continues to flow in the same direction through the body diode. Therefore, the drain voltage becomes equal to the forward direction voltage and remains low. Then, the resulting switching-loss $P_{SW-L}$ is very small, as described in the following equation:

$P_{SW-L} = \frac{1}{2} U_m I_{off}(t_{on} + t_{off}) f_m [W]$. 

Fig. 3. Graphic of switching waveform and loss
where \( t_{r-L} \) and \( t_{f-L} \) are Low-side MOSFET rise time and Low-side MOSFET fall time; \( U_D \) – forward direction voltage of low-side MOSFET body diode.

2.3.3. Reverse recovery loss in the body diode. When the high-side MOSFET is turned «ON», the transition of the body diode of the low-side MOSFET from the forward direction to the reverse bias state causes a diode recovery, which in turn generates a reverse recovery loss in the body diode. This loss is determined by the reverse recovery time of the diode \( t_{DD} \). From the reverse recovery properties of the diode, the loss is calculated with the following equation:

\[
P_{\text{diode}} = U_D \cdot I_{\text{sat}} \cdot t_{\text{deadtime}} \cdot f_{\text{sw}} [W]
\]

where \( t_{\text{dead}} \) is a body diode reverse recovery time; \( I_{\text{sat}} \) is a peak value of body diode reverse recovery current.

2.3.4. Output capacitance loss in the MOSFET. In each switching cycle, the loss is generated because the output capacitances of the high-side and low-side MOSFET transistors are charged. This loss is calculated with the following equation:

\[
P_{\text{GSS}} = \frac{1}{2} (C_{\text{GSS-L}} + C_{\text{GSS-H}}) U_{\text{ds}}^2 f_{\text{sw}} [W]
\]

where \( C_{\text{GSS-L}} \) and \( C_{\text{GSS-H}} \) are low-side and high-side MOSFET output capacitance; \( C_{\text{GS-L}} \) and \( C_{\text{GD-L}} \) are low-side and high-side MOSFET drain-source capacitance; \( C_{\text{GD-H}} \) are high-side MOSFET gate-drain capacitance.

2.3.5. Dead time loss. When the high-side and low-side MOSFETs are turned ON simultaneously, a short circuit occurs between the \( U_{\text{in}} \) and ground, generating a very large current spike. A period of dead time is provided for turning OFF both of the MOSFETs to prevent such current spikes from occurring, while the inductor current continues to flow. During the dead time, this inductor current flows to the body diode of the low-side MOSFET. The dead time loss \( P_{\theta} \) is calculated in the G and H sections of the waveform in Fig. 2 with the following equation:

\[
P_{\theta} = U_D I_{\text{sat}} (t_{\text{rL}} + t_{\text{fL}}) f_{\text{sw}} [W]
\]

where \( t_{\text{rL}} \) – dead time for rising; \( t_{\text{fL}} \) – dead time for falling.

2.3.6. Gate charge loss. The gate charge loss is the power loss caused by charging the gate of the MOSFET. The gate charge loss depends on the gate charges (or gate capacitances) of the high-side and low-side MOSFET transistors. It is calculated with the following equations:

\[
P_{G} = (Q_{\text{G1-H}} + Q_{\text{G1-L}}) U_{\text{ds}} f_{\text{sw}} \quad \text{or} \quad P_{G} = (Q_{\text{G2-H}} + Q_{\text{G2-L}}) U_{\text{ds}}^2 f_{\text{sw}}
\]

where \( U_{\text{ds}} \) – gate drive voltage; \( Q_{\text{G1-H}} \) and \( Q_{\text{G1-L}} \) – gate charge of low-side and high-side MOSFET.

2.3.7. Operation loss caused by the integrated circuit. The consumption power used by the IC control circuit \( P_{IC} \) is calculated with the following equation:

\[
P_{IC} = U_{\text{IC}} I_{\text{IC}}
\]

where \( I_{\text{IC}} \) is integrated current consumption.

The losses in the integrated circuit are caused by excessive temperature, ionizing radiation, mechanical shock and many other reasons. In semiconductor devices, problems in the device package can cause failures due to contamination, mechanical loads on the device.

2.3.8. Conduction loss in the inductor. There are two types of the power loss in the inductor: the conduction loss caused by the resistance and the core loss determined by the magnetic properties. Since the calculation of the core loss is too complex, it is not described in this article. The conduction loss is generated by the DC resistance (DCR) of the winding that forms the inductor. The \( DCR \) increases as the wire length increases; on the other hand, it decreases as the wire cross-section increases. If this trend is applied to the inductor parts, the \( DCR \) increases as the inductance value increases and decreases as the case size increases. Since the inductor is always energized, it is not affected by the duty cycle. Since the power loss is proportional to the square of the current, higher output current results in a greater loss. For this reason, it is important to select the appropriate inductors. The conduction loss of the inductor can be estimated with the following equation:

\[
P_{\text{LD}} = I_{\text{sat}} \cdot \text{DCR}.
\]

Since the output current is used in this equation, the average current of the inductor is used for the calculation. Similar to the above-mentioned calculation for the conduction loss of the MOSFET, the loss can be calculated in more detail by using the ramp waveform for the inductor current calculation:

\[
P_{\text{LD}} = \left[ I_{\text{sat}} + \frac{(I_{\text{r}} - I_{\text{f}}) T}{12} \right] \cdot \text{DCR}[W].
\]

2.3.9. Loss in the capacitor. Although several losses are generated in the capacitor – including series resistance, leakage, and dielectric loss – these losses are simplified into a general loss model as equivalent series resistance (ESR). The power loss in the capacitor is calculated by multiplying the \( ESR \) by the square of the root-mean-square (RMS) value of the AC current flowing through the capacitor:

\[
P_{\text{C}} = I_{\text{C}}^2 \cdot \text{ESR}[W],
\]

where \( I_{\text{C}} \) is root-mean-square (RMS) current of capacitor.

The RMS current in the input capacitor is complex, but it can be estimated with the following equation:

\[
I_{\text{C}} = \frac{1}{\sqrt{3}} \sqrt{I_{\text{in}}^2 + (U_{\text{in}} - U_{\text{sat}})^2} [A].
\]

The RMS current in the output capacitor is equal to the RMS value of the ripple current in the inductor, and calculated with the following equation:

\[
I_{\text{C}} = \Delta I_{\text{L}} / \sqrt{3},
\]

where \( \Delta I_{\text{L}} \) – ripple current of inductor:

\[
\Delta I_{\text{L}} = \frac{(U_{\text{in}} - U_{\text{sat}}) f_{\text{sw}} L}{U_{\text{in}}}[A].
\]
2.3.10. Total power loss. The power loss of the IC $P$ is obtained by adding all the losses together:

$$P = P_{ON-H} + P_{ON-L} + P_{SW-H} +$$

$$+ P_{SW-L} + P_{D} + P_{COSS} + P_{CR} +$$

$$+ P_{D} + P_{DCR} + P_{C_{on}} + P_{C_{off}}.$$  

Since the total power loss is obtained, the efficiency can be calculated with the following equation:

$$\eta = \frac{U_{in} - U_{out}}{U_{in}} \cdot P_{out}.$$  

2.4. Electrical principle scheme of buck converter synchronous rectifier. There is in Fig. 4 a realization of electrical principle scheme of buck converter synchronous rectifier (Fig. 4, a) and its implementation in the software application Proteus (Fig. 4, b). There was taken [7, 8] as a basis. This circuit uses a digital control system, because it maintains a constant output voltage, the controller changes the duty cycle of the control signal, which is directly reflected in the efficiency of the electrical circuit.

For the MOSFET in case of high-side voltage was used transistor IRF540 and transistor IRF540N in case of low-side n-channel voltage MOSFET. It was selected IR2184S as driver MOSFET of the high voltage in the integrated scheme. It can be controlled by the keys in the half-bridge and bridge schemes of the low resistance both with high-side and low-side voltage level. PIC16F877A scheme was used as microcontroller (Fig. 4) [9, 10].

This scheme is very easy to use, coding of this controller is also not difficult. One of the main advantages is that it can be write-erase as many times as possible because it uses FLASH memory technology.

3. Research results and discussion

During the simulation of electrical scheme, there were received characteristics in Fig. 5 with the pulse interval for the graphics of the both MOSFET transistors $T = 20 \mu s$ (20 microseconds).

Fig. 6 shows the switching characteristics of the power switch in the buck converter, which is regulated by the control system, in particular for the field-effect transistor IRF540 (a) and the power transistor IRF540N (b).

The driver IR2184S is used as a control system. Pulsating value of direct current inductance, where $f_{sw} = 1/20 \mu s = 50 \text{kHz}$:

$$aL = \frac{(U_{in} - U_{out}) \cdot U_{out}}{f_{sw} \cdot L} = \frac{(12 \text{ V} - 6 \text{ V})}{50 \text{ kHz} \cdot 2.87 \text{ mH} \cdot 12 \text{ V}} = 21 \text{ mA}.$$
Peak value of induction current:
\[ I_p = I_{\text{sat}} + \frac{\Delta I}{2} = 0.011 \text{ A} + \frac{21 \text{ m A}}{2} = 21.5 \text{ mA}. \]

Minimal value of induction current:
\[ I_{\text{v(colreg)}} = 0.011 \text{ A} - \frac{21 \text{ m A}}{2} = 0.5 \text{ mA}. \]

The conduction transistor losses accepting resistance \( R_{\text{ON-H}} = 0.5 \text{ Ohm} \) for IRF540 and \( R_{\text{ON-L}} = 40 \text{ mOhm} \) for \( n \)-channel MOSFET IRF540N:
\[ P_{\text{ON-H}} = \left( \frac{0.011 \text{ A}}{2} \right)^2 + \frac{(21.5 \text{ mA} + 0.5 \text{ mA})^2}{12} \times 0.5 \text{ Ohm} = 0.430 \times 10^{-4} \text{ W}. \]
\[ P_{\text{ON-L}} = \left( \frac{0.011 \text{ A}}{2} \right)^2 + \frac{(22 \text{ mA})^2}{12} \times 40 \text{ mOhm} = 0.326 \times 10^{-4} \text{ W}. \]

From the graphs in Fig. 4, the on-off time for a transistor with «high voltages» \( t_{\text{ON-H}} = 150 \text{ ns} \) (150 nanoseconds), \( t_{\text{ON-L}} = 0.25 \text{ us} \) (0.25 microseconds) and «low voltage» – \( t_{\text{OFF-H}} = 0.90 \text{ us}, t_{\text{OFF-L}} = 0.55 \text{ us} \). Switching losses for the field-effect transistor IRF540 and \( n \)-channel MOSFET-transistor for the diode voltage \( U_D = 1 \text{ V} \) in it, respectively, are equal to:
\[ P_{\text{SW-H}} = \frac{1}{2} 12 \text{ V} \cdot 0.011 \text{ A}(150 \text{ ns} + 0.25 \text{ us}) 50 \text{ kHz}, \]
\[ P_{\text{SW-L}} = \frac{1}{2} 1 \text{ V} \cdot 0.011 \text{ A}(0.9 \text{ us} + 0.55 \text{ us}) 50 \text{ kHz}, \]
\[ P_{\text{SW-H}} = 1.32 \text{ mW}, \quad P_{\text{SW-L}} = 398.75 \text{ uW}. \]

According to graphic in picture 4, dead time loss, accepting dead time for rising \( t_{\text{ph}} = 275 \text{ ns} \) and dead time for falling \( t_{\text{ph}} = 0.52 \text{ us} \):
\[ P_D = 1 \text{ V} \cdot 0.011 \text{ A} \times (0.275 \text{ us} + 0.52 \text{ us}) \times 50 \text{ kHz} = 0.4 \text{ mW}. \]

Reverse recovery loss in the body diode is calculated with the following equation:
\[ P_{\text{D,rev}} = (0.275 \text{ us} + 0.52 \text{ us}) \times 0.011 \text{ A} \cdot 1 \text{ V} \cdot 50 \text{ kHz} = 0.43725 \times 10^{-3} \text{ [W]}. \]

Capacitance loss in the MOSFET can be calculated with the following equation, where capacitance values are:
\[ C_{\text{GSS-H}} = 167 \text{ pF for IRF540 and } C_{\text{GSS-L}} = 295 \text{ pF for IRF540N}: \]
\[ P_{\text{Coss}} = \frac{1}{2} (167 \text{ pF} + 295 \text{ pF}) 12^2 \cdot 50 \text{ kHz} = 1.663 \text{ mW}. \]

The gate charge loss for transistors \( P_g \), accepting voltage value for both high-side and low-side voltage transistors \( U_{\text{GS}} = 0 \):
\[ P_g = (10 \text{ nC} + 5.4 \text{ nC}) \cdot 50 \text{ kHz} = 0. \]

Operation loss caused by the control system – integrated circuit with a current consumption value \( I_{\text{CC}} = 40 \text{ uA} \):
\[ P_{\text{L(DCR)}} = 161.3 \times 10^{-6} \cdot 1.95\text{[W]} = 315.535 \times 10^{-4} \text{[W]}. \]

Losses in the input and output capacitors \( P_{\text{CAP(ESR)}} = \frac{1}{2} I_{\text{ESR}}^2 U_{\text{ESR}}[\text{W}] \), accepting root mean square currents of the input and output capacitors are respectively equal:
\[ I_{\text{ESR}} = \sqrt[2]{U_{\text{in}} - U_{\text{out}}} U_{\text{out}} = 0.011 \text{ A} \sqrt[3]{(12 \text{ V} - 6 \text{ V}) 6 \text{ V}} = 5 \text{ mA}, \]
\[ P_{\text{CAP(ESR)}} = (5 \text{ mA})^2 \cdot \text{ESR}, \]
\[ P_{\text{CAP(ESR)}} = (5 \text{ mA})^2 \cdot 0 = 0, \]
\[ I_{\text{ESR}} = \frac{\Delta I}{2 \sqrt{3}} = 20.3 \text{ mA} \sqrt{2 \sqrt{3}} = 5.86 \text{ mA}, \]
\[ P_{\text{CAP(ESR)}} = (5.86 \text{ mA})^2 \cdot \text{ESR}, \]
\[ P_{\text{CAP(ESR)}} = (5.86 \text{ mA})^2 \cdot 0 = 0. \]
As a result, the total value of power loss and efficiency are equal:

\[ P = P_{IN-H} + P_{IN-L} + P_{SW-H} + P_{SW-L} + P_{diode} + P_{loss} + P_{L} + P_{C} + P_{MOSFET} + P_{F(M)} + P_{F(out)} = 0.005057 \text{W}. \]

\[ P = 4.03 \times 10^{-3} + 3.226 \times 10^{-6} + 1.32 \times 10^{-3} + 3.9875 \times 10^{-6} + + 0.43725 \times 10^{-3} + 1.663 \times 10^{-3} + 0.4 \times 10^{-3} + 0.48 \times 10^{-6} + + 315.535 \times 10^{-6} + 0 + 0 = 0.005057 \text{W}. \]

\[ \eta = \frac{U_{out} \cdot I_{out}}{U_{in} \cdot I_{in} + P} = 0.066 \text{W} + 0.004578 \text{W} = 93.5\%. \]

There are pictures in Fig. 7, which can describe impact of losses on the efficiency of buck voltage converter. There are diagram and graphic of loss in Fig. 7, b. There are losses, which were received during the development of the electrical scheme of buck voltage converter.

Fig. 7, a shows the graphs of the dependence of the efficiency \( \eta \) on the active power \( P_{ac} = U_{ac} \cdot I_{ac} \). Analyzing graphs for constant values of power loss \( P = 0.005057 \text{W}, \) without capacitance loss in MOSFET and without taking into account without capacitance in MOSFET and «high-voltage» field-effect transistor losses.

Fig. 7, b shows a diagram of the power losses that occurred during the construction of the electrical circuit of the buck converter (Fig. 4). Thus, the largest value of losses falls on the output capacitances of the high-side and low-side MOSFET (35.05%), switching-loss (36.16%) and reverse recovery loss in the body diode (9.69%).

### 4. Conclusions

The principles of technical implementation of a semiconductor buck voltage converter with a synchronous type of rectification, which can be used in wireless chargers, have been developed.

The possibility of creating a power supply based on the PWM of the DC input voltage is considered.

It is determined that for the practical implementation of a buck voltage converter based on an inductive-capacitive converter, it is advisable to use a digital control system. This scheme has been successfully tested, as evidenced by the relevant graphs.

The efficiency and loss power of the buck converter with synchronous rectification type are investigated, in particular, it is determined that the largest values of losses relate to the diode, the opening of the transistor gate and the capacitance of the output capacitor.

Synchronous rectification type of buck converters like this is widely used for specific loads. An enormous computer, increasingly power distribution architectures composed of power electronics are being considered or implemented for ships, cars, airplanes and so on. There are facilities to take advantage of alternative energy sources or attempt to increase efficiency and system availability.

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