Electron irradiation of multilayer PdSe$_2$ field effect transistors

A Di Bartolomeo$^{1,2}$, F Urban$^{1,2,3}$, A Pelella$^{1,2}$, A Grillo$^{1,2}$, M Passacantando$^4$, X Liu$^5$ and F Giubileo$^2$

1 Department of Physics, University of Salerno, via Giovanni Paolo II, Fisciano 84084, Italy
2 CNR-SPIN Salerno, via Giovanni Paolo II, Fisciano 84084, Italy
3 INFN – Gruppo collegato di Salerno, via Giovanni Paolo II, Fisciano 84084, Italy
4 Department of Physical and Chemical Sciences, University of L’Aquila, and CNR-SPIN L’Aquila, via Vetoio, Coppito 67100, L’Aquila, Italy
5 National Laboratory of Solid State Microstructures, School of Physics, Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing 210093, People’s Republic of China

E-mail: adibartolomeo@unisa.it

Received 21 February 2020, revised 17 April 2020
Accepted for publication 19 May 2020
Published 30 June 2020

Abstract

Palladium diselenide (PdSe$_2$) is a recently isolated layered material that has attracted a lot of interest for its pentagonal structure, air stability and electrical properties that are largely tunable by the number of layers. In this work, multilayer PdSe$_2$ is used as the channel of back-gate field-effect transistors, which are studied under repeated electron irradiations. Source-drain Pd electrodes enable contacts with resistance below 350 kΩ µm. The transistors exhibit a prevailing n-type conduction in high vacuum, which reversibly turns into ambipolar electric transport at atmospheric pressure. Irradiation by 10 keV electrons suppresses the channel conductance and promptly transforms the device from n-type to p-type. An electron fluence as low as $160 e^-/nm^2$ dramatically changes the transistor behavior, demonstrating a high sensitivity of PdSe$_2$ to electron irradiation. The sensitivity is lost after a few exposures, with a saturation condition being reached for fluence higher than $\sim 4000 e^-/nm^2$. The damage induced by high electron fluence is irreversible as the device persists in the radiation-modified state for several hours, if kept in vacuum and at room temperature. With the support of numerical simulation, we explain such a behavior by electron-induced Se atom vacancy formation and charge trapping in slow trap states at the Si/SiO$_2$ interface.

Keywords: palladium diselenide, field effect transistor, electron irradiation

(Some figures may appear in colour only in the online journal)

1. Introduction

Two dimensional materials such as graphene [1, 2] and transition-metal dichalcogenides [3] (TMDs) have been considered for several applications and in particular for space instrumentation [4] due to their low size and weight, high robustness and chemical inertness, as well as for their unique optoelectronic properties [5–9]. Use in space electronics, sensors, batteries, photovoltaics or light sources requires qualifications against vibrations and shocks, vacuum and thermal cycles, and exposure to radiation. In general, vibrations and shocks are not a threat for nanodevices and vacuum and thermal cycles are widely experimented in laboratories [10–13]. Similarly, the effect of radiation has been largely investigated for graphene [14–17] and well-known TMDs, such as MoS$_2$, WS$_2$, MoSe$_2$, and WSe$_2$ [14, 18–23], although most of the irradiation studies have been carried out using high energy protons, ions, electrons or $\gamma$ beams, typically in the MeV range. However, the application of these materials in the context of radiation-based medical diagnostics and treatments, radioprotection, monitoring of special nuclear materials or instrumentation and in other areas of nuclear science, also requires the understanding of their behavior when exposed to lower energy...
radiation sources. Low-energy (<100 keV) electron beams are commonly used during device fabrication by electron beam lithography (EBL) as well as for characterization and imaging through scanning and transmission electron microscopy (SEM and TEM). Furthermore, exposure to low energy electrons occurs in plasma treatments often used for device fabrication.

While high energy charged particles have a reduced probability of interaction in few-layer materials and primarily damage the supporting substrate, low-energy electrons can produce significant modifications of the properties of 2D-material based devices. Their stopping power in 2D materials becomes higher at decreasing energies below 100 keV [4, 24]. Elastic and inelastic scattering of low energy electrons can cause ionization and atomic displacement or sputtering, creating interstitials and vacancies, which impact the electronic performance of graphene or TMDs. Indeed, using first-principles simulations, it has been calculated that the displacement threshold energies and the formation energies of chalcogen vacancies lay between 4 and 8 eV in most common TMDs [22, 25]. The maximum energy transferred by 80 keV electrons to a S (or Mo) atom in MoS$_2$ is 6 (or 2) eV [26], and the formation of vacancies due to S sputtering in MoS$_2$ sheets has been demonstrated by TEM under 80 keV electron beam irradiation [25]. It has been shown that the filling of such vacancies with impurity atoms can control the doping of the material, thereby suggesting new ways for engineering the electronic structure of TMDs [27]. Analogously, the formation of vacancies due to S sputtering in WSe$_2$ creates localized carrier-trapping deep states within the band gap and, if two adjacent Se atoms are removed in the same chalcogenide layer, the change in the local crystal structure induces a transition from direct to indirect band gap [24]. It has been also reported that 1 keV to 3 keV electron irradiation can transform the structure of the MoS$_2$ films from amorphous to crystalline, thus enhancing the performance of MoS$_2$-based photodetectors [28]. The capability of electron beam irradiation to generate vacancies has enabled patterning and cutting of graphene or MoS$_2$ in nanoribbons [26, 29, 30]. Using SEM electron beams at energies 5, 10, 20 and 30 keV, it has been found that high electron fluxes (∼10$^4$ e$^-$/nm$^2$) result in permanent loss of photoluminescence for WSe$_2$ monolayers, owing to the creation of chalcogen vacancies by knock-on damage, which cause recombination and quenching of the photoluminescence [4]. Remarkably, even at the highest fluxes, the radiation induced damage was found to be mitigated if the electron energy increased to 30 keV as higher-energy electrons have a smaller interaction cross-section.

In this paper, we investigate the properties of multilayer PdSe$_2$ that we use as the channel of back-gate field effect transistors. PdSe$_2$ is a noble-metal TMD with pentagonal structure and puckered layers, which is air stable [31–33]. It has been obtained in the 2D form only recently [31] and is still poorly understood, even though it has been already exploited for high-sensitivity photodetectors [34, 35], field effect transistors [10, 36], thermoelectric devices [37], field emission [38] or water splitting [39]. The choice of nanosheets consisting of several layers is motivated by the recent discovery that defects in PdSe$_2$ can induce strong interlayer interactions and lead to the formation of new material phases. Indeed, it has been reported that the formation of Se vacancies by 60 keV electron irradiation in PdSe$_2$ can lead to local interlayer melding and result in the formation of the new Pd$_x$Se$_{(3-x)}$ 2D phase [40]. Here, we show that the use of Pd electrodes over multilayer PdSe$_2$ nanosheets gives rise to contacts with relatively low resistance even without any special treatments. We demonstrate that the dominant n-type conduction in high vacuum can be turned into an ambipolar or p-type conduction either by raising the pressure in air or by electron irradiation. We find that long exposure to 10 keV electron beams in an SEM chamber changes the channel doping and transforms the device from n- to p-type. Using Monte Carlo simulations, we show that the electron beam induces defects mainly in the PdSe$_2$ nanosheet and at the interface between the Si back-gate and the SiO$_2$ gate dielectric. Such defects permanently change the electric conduction in the device. This study highlights the high sensitivity of PdSe$_2$ to low-energy electron irradiation, a finding that limits its use in radiation-rich environments and requires caution when an electron beam is used for device fabrication and analysis. On the other hand, this property could enable highly-sensitive radiation detection, exploitable for applications in medical or nuclear instrumentation, radioprotection, radiotherapy and environmental monitoring.

2. Fabrication and methods

PdSe$_2$ nanosheets were exfoliated from bulk PdSe$_2$ single-crystal by the adhesive tape method and transferred onto a highly-doped p-type silicon substrate covered with 300 nm thick SiO$_2$. The PdSe$_2$ single-crystal was synthesized through a two-step thermal process from compressed tablets of selenium (99.999%) and palladium (99.95%) powders, mixed in the atomic ratio of 2 : 1. The tablets were heated up at 850 °C for 72 h in a quartz tube at 7.5 × 10$^{-6}$ Torr pressure.

Finally, the cooled down poly-crystalline PdSe$_2$ tablets were mixed with Se powder in a mass ratio of 1 : 4 and subjected to a second similar temperature annealing cycle.

The stoichiometric Pd : Se atomic ratio close to 1 : 2 and the layered crystallographic structure along the c-axis of the transferred nanosheets (the unit cell of PdSe$_2$ is orthorhombic with space group Pbca [31, 41, 42]) were confirmed by energy dispersive x-ray spectroscopy, x-ray diffractometry and Raman spectroscopy as reported in a previous work, where we used the same production batch [10].

Nanosheets with thickness of 10 – 15 nm were used for device fabrication through electron-beam lithography, metal evaporation and lift-off. Several structures for transfer length measurements (TLM) were contacted using Pd/Au (5/40 nm) leads. An example of a long flake, 2.5 µm wide, with six Pd/Au leads at a distance of 1.5 µm from each other, is shown in figure 1(a). The z-profile, obtained by atomic-force microscope (AFM), shows that the nanosheet has a thickness of 12 nm (figures 1(b) and (c)) corresponding to ~30 atomic layers (the theoretical thickness of a monolayer is 0.41 nm [36]).

The electrical characterization of the device was carried out by means of a Keithley 4200 semiconductor analyzer in
three-terminal configuration, as shown in the schematic setup of figure 1(d), where the two top metal leads are the source and drain and the silicon substrate is the back gate of a field effect transistor. The electrical measurements were performed inside a SEM chamber (ZEISS, LEO 1530) at room temperature and, if not otherwise specified, at pressure \( \sim 10^{-6} \text{Torr} \).

The 10 keV and 10 pA electron beam of the SEM was used for time-controlled irradiations of the channel region.

### 3. Results and discussion

Figure 2(a) shows the common-source transfer characteristics (drain-current versus gate-voltage, \( I_{ds} - V_{gs} \), at fixed drain-voltage, \( V_{ds} \)) of the transistor between metal leads labelled 5 and 6, at different pressures. The device, kept at \( \sim 10^{-6} \text{Torr} \) for several hours, shows drain electron dominant conduction over the \( \pm 50 \text{V} \) range (larger biases were avoided to prevent dielectric damage). The hysteresis obtained when the gate voltage is swept back and forth is very common in 2D-material field effect transistors and is caused by charge trapping in defects that can be intrinsic (e.g. Se vacancies) or extrinsic (e.g. adsorbates and dielectric or interface trap states) to the channel [43–48]. The transistor has an on/off ratio around 50, a negative threshold voltage, \( V_{th} \sim -10 \text{V} \), and a maximum field-effect electron mobility \( \mu = \frac{1}{W} \frac{1}{C_{ox}} \frac{dI_{ds}}{dV_{gs}} \sim 30 \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) (\( C_{\text{SiO}_2} = 11 \text{nF cm}^{-2} \)) is the capacitance per unit area of the 300 nm SiO2 gate dielectric, \( L = 1.5 \mu\text{m} \) and \( W = 2.5 \mu\text{m} \) are the channel length and width, respectively). The electronic mobility is within the range reported for similar ultrathin PdSe2 devices [31, 34, 36, 49].

The low-bias output characteristics (\( I_{ds} - V_{ds} \) curves at given \( V_{gs} \)) are straight-lines and the back-gate modulates the channel current without changing the linearity, as shown in figure 2(b).

The n-type behavior of the transistor and the linear output curves can be understood considering a low intrinsic n-type doping of PdSe2 and an ideal band alignment with the Pd metal contacts [50–52]. The n-type doping can be caused by intrinsic defects such as selenium vacancies [53–55]. The presence of defects in the PdSe2 channel is strongly suggested by the clockwise hysteresis [44, 45, 56, 57]. Furthermore, the work function difference between the 12 nm thick PdSe2 (work function \( \sim 5.0 \text{eV} \) [53]) and the Pd contacts (work function \( \geq 5.20 \text{eV} \) [58, 59]) originates a band bending that favours the electron conduction, as shown in the schematic energy diagram along the channel direction in the inset of figure 2(b). The low Schottky barriers at the contacts, owed to the small work function difference and the narrow bandgap of PdSe2, that for \( \sim 30 \) layers is less than \( 0.3 \text{ eV} \) [32, 34, 53], can contribute to the contact resistance but does not cause rectification at low bias. We note that, differently from here, non-linear output characteristics were reported for PdSe2 with similar channel thickness and Pd/Au contact [34], but this could be ascribed to a slight asymmetry of the two Schottky barriers which seems not to occur in the device under study [51].

Furthermore, figure 2(a) shows that the behavior of the transistor is dramatically changed by pressure, as often reported for TMDs materials [10, 49, 56, 60, 61]. The raising pressure gradually suppresses the channel current and the transistor becomes ambipolar at atmospheric pressure. The effect of pressure has been widely investigated and mainly attributed to adsorption of molecular O2 and water at defect sites which counter-dope the channel till reverting its polarity [10, 54, 56, 62]. As shown in figure 2(a), the effect of pressure is fully reversible as the transistor returns to its pristine status if the high vacuum is restored in a time of few hours [54]. Figure 2(c) displays the output characteristics at grounded gate of other devices of the same TLM structure obtained considering different couples of the metal leads; remarkably, the linear behavior is maintained even if the source and drain include one or more floating contacts in between. From figure 2(c), we extracted the external (source-drain) resistance, \( R_T \), as a function of the channel length, which is shown in figure 2(d). \( R_T \) includes the two contact resistances, \( R_C \), assumed equally distributed between the two contacts, and the channel resistance [63, 64], \( R_{ch} = R_{Sh} \frac{L}{W} \), where \( R_{Sh} \) is the channel sheet resistance in \( \frac{\Omega}{\text{square}} \) and \( L \) is the separation between two leads:

\[
R_T = 2R_C + R_{Sh} \frac{L}{W}
\]
Figure 2. Transfer characteristics at various pressures in time sequence (a) and output characteristics (b) at $10^{-6}$ Torr of the transistor with PdSe$_2$ channel between leads 5 and 6. The inset of (b) shows the band energy diagram along the channel direction for grounded gate. (c) Output characteristics between different combinations of the metal contacts and (d) external resistance versus channel length ($L$) at $\sim 10^{-6}$ Torr and for grounded gate (the PdSe$_2$ length covered by floating metal leads between source and drain is not included in $L$).

From the straight line fitting of figure 2(d), we obtain $R_c = 25^{+120}_{-25} \Omega$ and $R_{sh} = 1.27 \pm 0.15 \Omega \mu m$. The contact resistance can be expressed as the specific contact resistance, normalized by the width of the PdSe$_2$ channel, $\rho_c = R_c W = 60^{+300}_{-60} \Omega \mu m$. Despite the high incertitude, the maximum contact resistance of $360 \Omega \mu m$ is significantly lower than the contact resistance $\geq 1 \Omega \mu m$ obtained with as-deposited Ti [36, 65] or Ni [32] contacts, thus confirming the good choice of Pd metal leads.

The sheet resistance is comparable to that measured in grain structures of monolayer MoS$_2$ with missing S [66] or undoped multilayer MoS$_2$ (with comparable mobility) [67] and even lower than in undoped WSe$_2$ monolayers [68].

To study the effect of the irradiation by an electron beam at 10 keV and 10 pA, commonly used for SEM imaging, we selected the device between lead 1–2, which is the second most conducting transistor of the TLM structure according to figure 2(c). The channel of such transistor had not been exposed to radiation before, besides that from fast and low magnification imaging of the entire device area, corresponding to very low fluence on the channel region ($\sim 3 e^-/nm^2$).

We characterized the device shortly before and soon after each irradiation by repeatedly measuring the transfer and output characteristics. To control the electron fluence, the irradiation was performed by selecting only the channel region and imaging it for given times. Figure 3(a) shows that electron irradiation has an effect somehow similar to pressure as it suppresses the channel conductance and changes the conduction polarity. The effect of the irradiation is further clarified in figures 3(b) and (c) which show the forward and the reverse branches of the transfer characteristics, respectively.

Starting from the unirradiated device, three distinct groups of transfer characteristics (taken one after the other between consecutive irradiations) can be distinguished, corresponding to successive irradiations of 10 s, 60 s, 180 s (total fluences of $165 e^-/nm^2$, $1170 e^-/nm^2$, $4160 e^-/nm^2$). Surprisingly, figure 3(a) shows that most of the change occurs already at the low fluence of $165 e^-/nm^2$, i.e. after the first 10 s irradiation, which is enough to significantly suppress the channel conductance and cause the appearance of p-type conduction. Such an effect is enhanced by the successive 60 s irradiation. Further irradiation of 180 s or more (300 s) provokes only minor modifications. This observation indicates that the device becomes...
Figure 3. Full-loop (a), forward branch (b) and reverse branch (c) of the transfer characteristics of the transistor between leads 1–2 after electron beam irradiation of different duration. (d) Output characteristics after the whole cycle of irradiations. (e) Field effect mobility as a function of the electron beam irradiation. (f) Effect of the irradiation on the conductance minimum, $V_{gs}^{MIN}$.

gradually insensitive to the electron irradiation, meaning that the effect of electron irradiation saturates after a certain fluence. However, while low fluence irradiation can make reversible changes, that might be annealed after 1 h at room temperature, as we have reported before [10], here we found that a total irradiation time of 550 s corresponding to a fluence of $9160 e^−/nm^2$ set the device in a new state in which it persisted for the observation time of about 5 h.

Figure 3(d) shows that, despite the decrease of the transistor current, the linear behaviour of the output characteristics is unaffected. The linearity is essentially related to the properties of the Pd/PdSe$_2$ interface, which is preserved as we avoided irradiation of the Pd/PdSe$_2$ contact region. Figures 3(e) and (f) demonstrate that the irradiation results in a significant degradation of the charge carrier mobility as well as in a right-shift of the minimum conductance points, $V_{gs}^{MIN}$, obtained from
both the forward and the reverse transfer curves. The mobility degradation is indicative of structural damaging and charge trapping that may generate long range coulomb scattering, while the right-shift corresponds to a doping change as the device gradually becomes p-type.

To further understand the effect of the 10keV electron beam, we performed Monte Carlo simulation to track the electrons trajectories and the energy loss into the materials. The energy released by electrons can be estimated through the cathodoluminescence, i.e. the light emission caused by electron excitation, whose intensity is shown in figure 4(a). We used CASINO software [69, 70], a Monte Carlo simulator of electron trajectories in solids, specially designed for low-energy beam interaction in bulk and thin foils and widely used in scanning electron microscopy and microanalysis.

The simulation shows that the rate of energy loss in PdSe$_2$ and Si are comparable and higher than in SiO$_2$. As expected, most of the energy is released in the silicon substrate where the electrons penetrate for about $\sim 1\ \mu m$ as shown by figure 4(b) reporting the maximum penetration depth. The inset of figure 4(b) confirms that there is energy loss in the PdSe$_2$ layer. The energy loss in PdSe$_2$ can be up to 2keV, enough to cause atom displacement or sputtering [71]. The appearance of defects, preferentially Se vacancies as the energy required to displace the chalcogen ($\leq 7\ eV$) is about three times lower than that required to remove the transition metal from the same crystal [71], causes the observed reduction of the charge carrier mobility. Figure 4(a) also shows that there is an uptick in the release of energy at the SiO$_2$/Si interface. The formation of defects at such interface introduces electron trap states [72–74], which can contribute to enhance the p-type doping of the PdSe$_2$ channel. The pile-up of negative charge at the SiO$_2$/Si during prolonged irradiation exposures acts as an extra negatively-biased gate and right-shift $V_{gs,\ MIN}$ thus increasing the hole-doping of the channel. We note that the formation of defects at the SiO$_2$/Si, corresponding to trap states below the conduction band edge, created by a 10keV electron-beam exposure, has been reported in standard Si based MOS field-effect transistors [75].

4. Conclusions
We have studied PdSe$_2$ back gate field-effect transistors and shown that their electrical behavior can be dramatically affected by an SEM electron beam. We have highlighted that the beam has a twofold effect: it deteriorates the mobility of the PdSe$_2$ by creating intrinsic defects and changes the polarity of the device through pile-up of negative charges at the interface. The high sensitivity of PdSe$_2$ to low energy irradiation must be taken into account and can limit the use of the material in high radiation environments as well as its treatment by electron beams or plasmas. Our study suggests the opportunity to perform electrical characterization of PdSe$_2$ devices prior to SEM imaging and demonstrates the suitability of the material for low-energy radiation detectors for medical or nuclear instrumentation as well as for environmental monitoring of caves, mines, nuclear plants or space.

Acknowledgments

We thank Shi Jun Liang from Nanjing University in China for providing the samples used in this study.

ORCID iDs

A Di Bartolomeo https://orcid.org/0000-0002-3629-726X
M Passacantando https://orcid.org/0000-0002-3680-5295
F Giubileo https://orcid.org/0000-0003-2233-3810

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