CMOS platform for atomic-scale device fabrication

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Abstract

Controlled atomic scale fabrication based on scanning probe patterning or surface assembly typically involves a complex process flow, stringent requirements for an ultra-high vacuum environment, long fabrication times and, consequently, limited throughput and device yield. We demonstrate a device platform that overcomes these limitations by integrating scanning-probe based dopant device fabrication with a CMOS-compatible process flow. Silicon on insulator substrates are used featuring a reconstructed Si(001):H surface that is protected by a capping chip and has pre-implanted contacts ready for scanning tunneling microscope (STM) patterning. Processing in ultra-high vacuum is thereby reduced to a few critical steps. Subsequent reintegration of the samples into the CMOS process flow opens the door to successful application of STM fabricated dopant devices in more complex device architectures. Full functionality of this approach is demonstrated with magnetotransport measurements on degenerately doped STM patterned Si:P nanowires up to room temperature.

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(Some figures may appear in colour only in the online journal)

1. Introduction

An early demonstration of the potential of scanning probe microscopy (SPM) in the area of atomic scale fabrication was the famous quantum coral [1]. Since then, a large number of distinct probe-based fabrication methods have been developed based either on direct atomic assembly or tip induced patterning [2]. However, broader adoption of these methods is often impeded by their inability to compete in speed and throughput with conventional lithography techniques and to find a packaging approach that allows preservation of the atomic scale devices outside an ultra high vacuum (UHV) environment.

One of the most promising SPM-based fabrication techniques is scanning tunneling microscopy (STM) based dopant device fabrication [3]. In this case, a hydrogen passivation layer on Si(001):H is locally desorbed with an STM tip in a current induced process [4, 5] to create reactive sites for selective attachment of dopant precursor molecules (see figure 1(b) and supplementary information is available online at stacks.iop.org/NANO/29/435302/mmedia). After thermal incorporation of the dopants into surface substitutional sites, overgrowth with epitaxial silicon, and ex situ contacting of the dopant device layer, these atomically precise devices can be electrically measured in the same way as conventional semiconductor devices. The technique provides a way of defining degenerately doped metallic regions in a semiconductor with atomic-scale resolution.
It allows deterministic placement of single dopant atoms \[6, 7\], creation of wires \[8\] and quantum dots \[9, 10\] with atomic scale dimensions and enables exploration of the quantum properties of these nanoscale systems. Furthermore, it may also provide the necessary atomic precision needed for donor based quantum computing architectures \[11–13\].

However, as with other probe-based fabrication schemes, STM dopant device fabrication is technically extremely challenging. It requires the use of dedicated UHV equipment and the process flow for the device fabrication is very time consuming, tedious and prone to failure. As a result, only a handful of groups in the world have successfully made devices with this technique \[3, 9, 14, 15\], and despite efforts directed at simplifying some parts of the process \[16, 17\] its current application potential remains somewhat limited.

To overcome these limitations we present a platform for STM based dopant device fabrication that is fully integrated with a CMOS process flow. It drastically reduces the fabrication time and complexity, and adds additional functionalities to STM fabricated dopant devices. The key features of this platform are outlined in figure 1. Silicon on insulator (SOI) substrates are prepared at wafer scale (200 mm) in a cleanroom environment using an original integration based on standard CMOS processes. Wafers are diced into samples containing localization markers and pre-implanted contacts. Each sample is protected with a sacrificial Si capping chip, which can be easily removed inside the UHV system by inserting a molybdenum blade in the recess between the substrate and the cap. Both chips have reconstructed and hydrogen terminated Si \((001):H\) surfaces with low defect densities directly suitable for STM patterning without the need for high-temperature \textit{in situ} surface preparation. Large implanted contact pads serve as easy-to-reach contact terminals for post-processing while shallow implant extensions come as close as 670 nm from each other and are easily accessible in the STM patterning process. After UHV fabrication and Si overgrowth, the devices can either be contacted from the top using optical or e-beam lithography or the chips can be reintegrated into the CMOS workflow using a chip-to-wafer bonding process (figure 1(c)). In the latter case, many devices can be simultaneously contacted from the backside by removal of the silicon substrate and contact can be made to the device through vias in the buried oxide layer (4).

Figure 1. SOI-based platform for atomic scale dopant device fabrication. (a) Hydrogen passivated SOI substrates with pre-implanted contacts and alignment markers protected from the ambient environment by a similarly passivated capping chip that is hydrogen bonded to the sample. After loading the sample into UHV, the capping chip is removed with a molybdenum blade exposing a high quality Si\((001):H\) surface ready for STM patterning. (b) The STM tip is aligned to the pre-implanted contacts with the help of etched alignment markers and a desired pattern is written by locally desorbing the hydrogen from the surface. Precursor gas (PH\(_3\)) selectively sticks to the dehydrogenated surface creating highly doped areas with defined geometry. After the incorporation anneal and encapsulation of the dopant device with a thin layer of Si, electrical contacts are fabricated. (c) Chip is bonded to a carrier wafer (1), original handle wafer is removed in a chemical-mechanical process (2), and metal connections (3) are fabricated through vias in the buried oxide layer (4).
Table 1. Comparison of the main aspects of the standard STM based dopant device fabrication on a conventional bulk Si substrate and on the CMOS platform.

|                                | Standard fabrication                                                                 | CMOS platform                                                                 |
|--------------------------------|--------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| Substrate preparation (ex situ) | Lithography for markers, chemical cleaning of individual chips                        | Wafer scale substrate patterning and capping using CMOS processes             |
| Substrate preparation (in situ) | Surface reconstruction at $T > 1000 \, ^\circ \text{C}$, hydrogen passivation         | Low temperature degas                                                         |
| STM lithography                | Tip alignment, device + contact patterning 1–3 h per electrical contact               | Fast tip alignment, only device patterning 1 h total                          |
| UHV post-processing            | Incorporation and overgrowth similar for both approaches                               |                                                                              |
| Ex-situ post-processing        | Custom e-beam process for each chip                                                  | Optical/e-beam lithography processing at wafer scale for reintegration        |
| Electrical measurements        | Only low temperature device operation due to substrate leakage between contacts       | Dopant device operation up to room temperature because of SOI architecture and backgate |

In section 2 we describe the experimental details of the sample fabrication process and electrical measurements. In section 3 we describe the STM fabrication of two dopant nanowires on the SOI substrates and in section 4 we analyze their magnetotransport properties.

2. Experimental details

2.1. SOI substrate processing

The pre-fabricated SOI substrates were made in a cleanroom at CEA LETI. Figure 2 outlines the process flow for the substrate preparation, STM device fabrication and post-processing. The substrate preparation is performed at wafer scale using Deep UV lithography. We start with a 200 nm SOI wafer with a 200 nm thick device layer (boron doped, resistivity $\sim 10^{-18} \, \Omega \cdot \text{cm}$) and 400 nm thick BOX. In the first step we etch the alignment marks. They are 50 nm deep and sidewalls are at an angle of 55° which provides good marker visibility, but does not represent a problem for scanning with the STM.

Contact implantation is performed in a two-step process: the deep implants (fluence of $3 \times 10^{15} \, \text{cm}^{-2}$ and ion energy of 20 keV and 80 keV for phosphorus and boron, respectively) extend all the way through the device layer and allow contacting from the backside as required for CMOS reintegration [18]. In contrast, the shallow implants (fluence of $3 \times 10^{15} \, \text{cm}^{-2}$ and ion energy of 5 keV and 12 keV for P and B, respectively) only create a 20 nm deep doped layer (before reconstruction) and limit damage to the surface from the implantation process.

In order to achieve sufficient surface quality, retain marker geometry and limit dopant diffusion near the contact pads we use a reduced pressure chemical vapor deposition process [19] for surface reconstruction and hydrogen termination of the SOI substrates. The surface reconstruction step is performed at a temperature of 950 °C which is sufficiently low to prevent substantial dopant diffusion. Finally, we protect the reconstructed surface by hydrophobic bonding with a sacrificial capping wafer [20]. The sandwich is then diced and the chips can be introduced into UHV for dopant device fabrication. Once capped, the samples may be kept in ambient conditions for many months without any noticeable degradation of the surface quality.

Figure 3 shows the layout of the localization markers and the implants. Each chip contains five device positions, two with a single pair of phosphorus implants, two with a single pair of boron implants and one compound position with a pair of implants for both dopant types. Below the position numbers a row of various test structures were used to characterize the implanted contact structures. Just below position 5 there is a test structure which is identical to device positions 1 and 2 but with an implanted stripe connecting the two contacts. This test structure was used to evaluate the magnetoresistance of the phosphorus implants in section 4.

2.2. Dopant device fabrication with STM lithography

In order to handle the SOI samples in the UHV STM we designed a specialized sample holder that clamps the substrate from the sides allowing for easy in situ removal of the capping chip. After introducing the sample into the system, it is first degassed for 1 h at 300 °C in order to get rid of adsorbed chemical species. The capping chip (see figure S1 in the supplementary information) is removed by pressing a molybdenum blade in a recess between the sample and the cap. Finally, the sample is transferred to the STM stage where the patterning is performed.

For this we use a commercial variable temperature STM from Scienta Omicron with custom control software and hardware. Alignment markers are used to position the tip close to the central device area which contains the contact implants (figure 3 shows the detailed layout of the localization markers, for additional information see figures S2, S3 in the supplementary information).
For STM imaging of the samples we typically use a sample bias of $-2.5\, \text{V}$ and tunneling current setpoint of $100\, \text{pA}$. In order to desorb hydrogen from the surface, we switch to writing parameters and scan over the desired areas with the feedback switched on. For patterning we apply a positive sample bias between $+4.5\, \text{V}$ and $+7\, \text{V}$ and tunneling current of around $4\, \text{nA}$. For slow writing of fine features we use tip velocities down to $10\, \text{nm}\, \text{s}^{-1}$, line separations in the desorption pattern of $\sim 0.5\, \text{nm}$ and voltages from the lower part of the range of $+4.5\, \text{V}$ to $+5.5\, \text{V}$. For rapid, coarse patterning of large areas we use tip velocities up to $100\, \text{nm}\, \text{s}^{-1}$, line separations of $\sim 5\, \text{nm}$ and voltages up to $+7\, \text{V}$. We use Python scripts to generate the desired patterns for desorption and to programmatically control the STM tip movement along the pattern.

After STM desorption of the pattern is complete, we typically image the desorbed area (or a part of it) in order to confirm desorption quality and check for desorption errors. Then we proceed with gas-phase doping (similar to the procedure described in [9]). The sample is exposed to a 10 Langmuir dose of phosphine gas whilst in the STM stage. Afterwards, the sample is transferred to the preparation chamber (of the same UHV system), placed on a heated manipulator and annealed to $370\, ^\circ\, \text{C}$ for 1\, min. After cooling the sample to a temperature of about $270\, ^\circ\, \text{C}$, a $20\, \text{nm}$ thick layer of intrinsic Si is grown on top of the device surface using a silicon sublimation source from MBE-Komponenten GmbH at a growth rate of about $1\, \text{nm}\, \text{min}^{-1}$.

### 2.3. Sample post-processing

Compared to the conventional dopant device fabrication on bulk Si substrates, the contact fabrication procedure is facilitated by the presence of the large ($10\, \mu\text{m} \times 10\, \mu\text{m}$) pre-implanted contact pads. There are two possibilities for post-processing: (I) direct e-beam lithography (or, alternatively, optical lithography) contacting on a single chip level or (II) reintegration of the samples in a wafer scale CMOS process flow (see figure 2 for detailed process flow).

(I) For the e-beam process, metal contacts are fabricated directly on the upper side of the samples. After overgrowth, the implanted areas are buried under a $20\, \text{nm}$ thick layer of intrinsic Si. We first use reactive ion etching to etch a grid of $1 \times 1\, \mu\text{m}^2$ large and $50\, \text{nm}$ deep holes into the implant pads and subsequently deposit $100\, \text{nm}$ thick Al contacts in a standard lift-off process. The contacts are then annealed to $350\, ^\circ\, \text{C}$ for 15 \, min in a reducing atmosphere (5\% H, 95\% Ar) at 200 mbar. In order to minimize leakage between the handle wafer (used as a gate in this case) and the device layer, we etch a frame around each device position isolating the active area from the rest of the device layer (particularly from the edges of the sample which were found to cause leakage). Finally, the sample is glued into a chip carrier using silver epoxy (Epotec H20e) and wire-bonded. In order to apply a gate voltage to the handle wafer, the backside of the sample is scratched with a diamond scribe prior to gluing in order to penetrate the oxide.

![Diagram](image_url)
For CMOS reintegration, the chips are first bonded to a new handle wafer (bulk Si wafer with a 200 nm oxide layer on top) with the device layer (where the STM device is located) facing towards the handle wafer. The original SOI substrate is then completely removed using a chemical-mechanical process, exposing the backside of the original BOX layer. In the next step we etch vias through the BOX exposing the bottom side of the deep contact implants in the device layer. Finally, we deposit aluminum silicon alloy contacts which connect the implants through the vias to wire-bonding pads. A custom lithography step was performed on the 30 nm NW sample to additionally define a metallic top gate. This could have been done in the reintegration step but was not foreseen in the mask-set that was used. Finally, the sample is also glued in a chip carrier and wire-bonded.

3. Dopant device patterning

In the STM stage the pre-implanted contacts are localized using an optical microscope and large area STM scans that in total typically take less than 30 min (see supplementary information). A schematic of the device position with pre-implanted contacts is shown in figure 4(a), whereas figure 4(b) shows the corresponding scanning electron microscopy image. Figure 4(c) is a constant current topographic STM image taken just before defining a nanowire between two n-type contacts. The implants are clearly visible thanks to a height difference of a few Si monolayers (5–10) caused by different oxidation and etch rates for heavily doped Si in the surface reconstruction process after the ion implantation step. The typical quality of the Si(001):H sample surface in the central area is indicated by the STM image in figure 4(d).

Figure 4(d) shows the center of the same device position with a 30 nm nanowire defined by hydrogen desorption (see experimental details) with the STM tip. A dimensional representation of the nanowire pattern which was used is given in figure 4(d). The duration of the writing process in this case was about 15 min. After the writing step the sample was dosed with phosphine, annealed at 370 °C for one minute to incorporate and electrically activate the dopants, overgrown with 20 nm of intrinsic Si and then removed from UHV (see section 2.2). This specific nanowire device was subsequently reintegrated into the 200 nm CMOS process flow for backside contact fabrication. In the following this device is referred to as 30 nm NW.
Figure 4. STM-based dopant device fabrication on an SOI sample with pre-implanted contacts. (a) Schematic of the central device region of the SOI samples with both boron (B) and phosphorus (P) implants. (b) Scanning electron microscope image of the device region with both types of implanted contacts each giving a different contrast. (c) STM image of two n-type contacts (top right to bottom left) and the three etched alignment markers (dark areas). (d) STM image of the device area with a desorbed 30 nm wide nanowire connecting the two contacts. (e) High resolution STM image of the device area showing the typical surface quality of the SOI substrates, with few residual defects that result from the de-bonding process and (f) high resolution image of the 30nm wide nanowire from image (d).
In a similar way we fabricated a 120 nm wide nanowire with the same length of 670 nm. This second sample was post-processed using e-beam lithography and by contacting the large implant pads from the front. This sample is referred to as 120 nm NW. A third sample containing no STM defined structures was post-processed together with the 120 nm NW sample. Two device positions with an implant separation of 670 nm and 1170 nm were contacted and are referred to as Blank 1 and Blank 2, respectively.

4. Electrical measurements

An important advantage of the SOI substrate is that the charge carrier density in the device layer can be tuned by application of a voltage to the silicon substrate. For samples contacted from the top by e-beam lithography we find that the presence of trapped charges at the BOX interface shifts the Fermi level in a way that leakage occurs between contacts in the device layer. By application of a negative voltage to the substrate this can be fully suppressed and the charge compensated.

In figure 5(a) we present room temperature measurements of the electrical transport through the nanowires and Blank positions as a function of the applied gate voltage. In the case of the 120 nm NW and Blank positions the gate was realized by applying a voltage to the handle wafer, while for the reintegrated 30 nm NW a metallic gate was lithographically defined in the post-processing step (see figure 2). For the three e-beam contacted samples, the trapped charges in the BOX shift the layer into inversion. Application of a negative bias of $-10$ V leads to a depletion of the device layer and fully insulating behavior even at room temperature. This uniquely enables the measurement of electrical transport through STM defined dopant devices at room temperature.

The situation is similar for the 30 nm NW; however, after removal of the handle wafer in the reintegration process the Fermi level offset is not as pronounced as for the other samples and even at zero gate bias substrate leakage is small.

Figure 5(b) shows the resistance of the 120 nm NW as a function of temperature. The resistance drops with decreasing temperature as expected for a metallic system and at temperatures below 25 K it increases again due to the onset of weak localization (WL) [21]. This regime is governed by
enhanced backscattering from constructive interference of time-reversed paths with a length that is shorter than the phase coherence length. Resistivity is therefore sensitive to time-reversal symmetry breaking by a magnetic field and the increase in resistance is suppressed for high enough fields [22]. Figures 5(d) and (e) show in more detail the magnetoresistance of the two nanowires at different temperatures. Aside from the WL peak around $B = 0$ T, the resistance of the nanowires (particularly the 120 nm NW) is also affected by universal conductance fluctuations [21]. The relative magnitude of the WL effect in the two nanowires at 2 K is compared in figure 5(f). The dotted lines are fits of the peaks to the 1D WL theory (see supplementary information). The resistivity of the 30 nm NW and 120 nm NW is 1.74 kΩ/$\square$ and 1.96 kΩ/$\square$ and the phase coherence length based on fits to WL theory is 56 nm and 54 nm, respectively. This is comparable to previously reported values [23]. The blue curve shows the situation for a reference sample with no gap between the implanted contacts where the dopants form a 3D channel with a crosssection of about 700 $\times$ 100 nm. Figure 5(c) compares the magnitude and characteristic field of the WL effect for the three different cases. As expected, the magnitude reduces as the width and thickness of the dopant layer increases. The characteristic phase breaking field is, however, larger again for the implant case, since only the projection of the 3D scattering paths onto a plane perpendicular to the field is relevant for phase breaking. The electrical transport measurements of the dopant nanowires show consistent behavior similar to previous reports and confirm that the suggested alternative strategy for sample pre- and post-processing is compatible with the sensitive STM-based dopant device fabrication process.

### 5. Conclusions

In summary, we have developed a platform which integrates STM-based nanoscale dopant device fabrication in the standard CMOS process flow. Performing STM lithography on pre-implanted and hydrogen terminated SOI substrates greatly reduces the fabrication time and complexity and it facilitates sample post-processing. The thin SOI device layer suppresses substrate current leakage and, with the assistance of a gate, allows room temperature operation of the dopant devices. Last but not least, the demonstrated CMOS compatibility opens the possibility to integrate atomic scale dopant devices with additional on-chip circuitry and may in the future be extended to other STM fabricated devices such as the ones resulting from molecular assembly.

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