A Novel Reconfigurable Architecture of a DSP Processor for Efficient Mapping of DSP Functions using Field Programmable DSP Arrays

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Abstract- Development of modern integrated circuit technologies makes it feasible to develop cheaper, faster and smaller special purpose signal processing function circuits. Digital Signal processing functions are generally implemented either on ASICs with inflexibility, or on FPGAs with bottlenecks of relatively smaller utilization factor or lower speed compared to ASIC. Field Programmable DSP Array (FPDA) is the proposed DSP dedicated device, redolent to FPGA, but with basic fixed common modules (CMs) (like adders, subtractors, multipliers, scaling units, shifters) instead of CLBs. This paper introduces the development of reconfigurable system architecture with a focus on FPDA that integrates different DSP functions like DFT, FFT, DCT, FIR, IIR, and DWT etc. The switching between DSP functions is occurred by reconfiguring the interconnection between CMs. Validation of the proposed architecture has been achieved on Virtex5 FPGA. The architecture provides sufficient amount of flexibility, parallelism and scalability.

Keywords- Digital Signal Processing (DSP), Application Specific Integrated Circuit (ASIC), Field Programmable Gate Array (FPGA), Field Programmable DSP Array (FPDA), Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Discrete Wavelet Transform (DWT), Finite Impulse Response (FIR), Infinite Impulse Response (IIR), Look Up Table (LUT), Configurable Logic Block (CLB), Common Module (CM), Distributed Arithmetic (DA)

I. INTRODUCTION

Computationally DSP functions [3], [6] are computationally intensive and exhibit spatial [2], [4] parallelism, temporal [5] parallelism or both. High speed applications like Software Defined Radio (SDR), satellite modems, HDTV etc. need very high performance that is not achievable with currently available DSP processors [22], [23]. Even though higher performance achievement, relatively lower cost and low power dissipation are the major advantages of ASICs, high degree of inflexibility restricts their usage for rapidly changed scenario in the current high end applications as mentioned above. On the other hand, mapping different DSP functions at run-time, dynamically reconfigurable FPGAs [4], [7], [8] are becoming popular because of their flexibility and low risk factor. However, lower utilization factor due to wastage of area in SRAM based CLBs, higher cost and relatively lower performance due to complex interconnection and routing delay are the major bottlenecks of the FPGAs. Although, some of the FPGAs of virtex family offer DSP basic building blocks like Multiply and Accumulation (MAC) units but silicon utilization factor is not optimized for the LUT based architecture [24] of FPGA. The proposed FPDA architecture eliminates the drawbacks of FPGAs and ASICs. DSP functions are mainly of two types: ‘Filter Functions’ (FIR, IIR etc.) and ‘Linear Transforms’ (DFT, FFT, DCT, DWT etc.). Keeping these in views, this paper presents a novel reconfigurable DSP architecture which combines different DSP functions by interconnections among different CMs.

Section- II of the paper describes Distributed Arithmetic Principle which has been used to implement DSP functions (like FIR, IIR, DCT, DWT etc.) in the proposed architecture. Section- III of the paper describes different DSP functions and their implementation proposal in proposed architecture. Section- IV describes the detailed representation of “Reconfigurable Architecture”. Section- V analyzes the performance with
various simulations, implementation and comparison results and Section- VI concludes the paper.

II. DSP FUNCTIONS AND PROPOSED IMPLEMENTATION

A. Finite Impulse Response Filter

An FIR with constant coefficients is an LTI digital filter. The output of an FIR of length L, to an input series x[n] is finite version of convolution sum:

\[ y[n] = \sum_{k=0}^{L-1} c[k]x[n-k] \]  \hspace{1cm} (1)

Where \( c[0] \neq 0 \) through \( c[L-1] \neq 0 \).

16 tap FIR filter has been implemented using Parallel DA in Fig. 1 and Fig. 2. DA [11], [12], [21] architecture replaces multiplier block by adder and shifter. LUT contents for DA FIR are \( f(c[n-k], x[n]) \). A LUT of \( 2^{16} \) locations is needed to implement 16 tap FIR using DA. This paper proposes FIR architecture with 32 numbers of \( 2^4 \) LUTs that cause decrease in memory locations and fast execution at the cost of excess LUTs, registers and adders. Each bit of each input enters in parallel to the LUTs (2 LUTs for a coefficient). The Proposed FIR architecture is scalable. The basic building blocks, needed to implement FIR filter, are LUTs, adders and registers.

![Fig. 1 FIR unit for a coefficient](image)

![Fig. 2 PDA FIR Filter Architecture](image)

B. Infinite Impulse Response Filter

IIR filter is a recursive filter as it has feedback from output. The difference equation for such a system yield:

\[ y[n] = \sum_{l=0}^{L-1} a[l]x[n-l] + \sum_{m=0}^{M} b[m]y[n-m] \]

(2)

According to Fig. 3, IIR is basically combination of two FIR filters and an adder. Implementation of IIR using Parallel DA has been done by forward filter and a feed backward filter. Feed backward filter is basically having the same input of forward filter with different LUTs. The basic building blocks, needed to develop an IIR filter, are LUTs, adders and registers.

For 3tap IIR filter:

\[ y_2 = (a_0x_2 + a_1x_1 + a_2x_0) + (b_2y_1 + b_1y_0) \]  \hspace{1cm} (3)

Can be re written as:

\[ y_2 = (a_0x_2 + a_1x_1 + a_2x_0) + \{x_0(b_2b_1a_0) + x_1(b_2a_0)\} \]  \hspace{1cm} (4)
From the above equations, it is observed that an IIR filter can be implemented using two FIR filters with same inputs.

Fig. 3 PDA IIR Architecture

C. Discrete Wavelet Transform

Discrete Wavelet Transform has been widely used in digital signal processing and image compression (like JPEG) domain in recent years. The coefficients of DWT are calculated recursively using Mallat’s Pyramid Algorithm.

\[
W_L(n, j) = \sum_{m} W_L(m, j-1) h_0(m - 2n) \\
W_H(n, j) = \sum_{m} W_L(m, j-1) h_1(m - 2n)
\]

Where \(W_L(n, j)\) and \(W_H(n, j)\) are the \(n^{th}\) scaling and wavelet coefficient at the \(j^{th}\) stages, \(h_0(n)\) and \(h_1(n)\) are dilation coefficients [18] corresponding to scaling and wavelet functions.

Fig. 4 Discrete Wavelet Transform

The forward DWT has been implemented using Decimator block, which consists of a PDA FIR filter and down sampling operator. The PDA FIR has been implemented as FIR architecture described above in Fig. 4. The FIR Daubechies 8- tap has been chosen for the implementation as shown in TABLE I.

TABLE I
DAUBECHIES 8 TAP FILTER COEFFICIENT

| \(H_0\)   | \(L_0\)   |
|----------|----------|
| -0.0106  | 0.2304   |
| -0.0329  | 0.7148   |
| 0.0308   | 0.6309   |
| 0.1870   | -0.0280  |
| -0.0280  | -0.1870  |
| -0.6309  | 0.0308   |
| 0.7148   | 0.0329   |
| -0.2304  | -0.0106  |

The FIR input has been driven by the clock i.e. tied to the clock input of the 1bit counter in Fig. 5. The output port of FIR is connected to the input of parallel load register. Receiving and Blocking of the input to register depend upon the state of the counter. The input enters decimator at the rate of 1sample/ clock while filtered output comes out at the rate of 1sample/ 2 clocks.

Fig. 5 Implementation of Decimator

D. Fast Fourier Transform

Discrete Fourier Transform is a discrete transform for Fourier analysis of the signal. The formulation of DFT for an input signal:

\[
X[k] = \sum_{n=0}^{N-1} x[n] e^{-j\frac{2\pi kn}{N}}
\]

FFT is basically computation process of Discrete Fourier transform with multi-dimensional index mapping, suitable for real time application. The proposed FFT architecture has been implemented with Cooley-Tukey Algorithm [14], [15]. The efficient complex multiplier has been implemented for complex multiplication of butterfly, as shown in Fig. 6.

Final product of the complex multiplication:

\[
R + jI = (a + ib)(\cos \theta + j \sin \theta)
\]

\[
R = (\cos \theta - \sin \theta) b + \cos \theta (a - b)
\]

\[
I = (\cos \theta + \sin \theta) a - \cos \theta (a - b)
\]
Instead of cosine and sine table to compute complex multiplication, the implementation can be accomplished with three multipliers, one adder and two subtractors at the cost of one additional table, as shown in TABLE II. The Butterfly has been implemented using proposed efficient complex multiplier.

TABLE II

| Basic blocks of each butterfly unit | Number |
|------------------------------------|--------|
| Adder                              | 1+1=2  |
| Subtractor                         | 1+2=3  |
| Multiplier                         | 3      |

![Fig. 6 Butterfly Architecture](image)

![Fig. 7 Scalable FFT Architecture](image)

16 point proposed scalable FFT architecture has been implemented using eight butterfly units, sixteen registers, sixteen 4:1 multiplexers and fourteen 2:1 multiplexers in Fig. 7.

The parallelism of the proposed architecture has been achieved by performing each stage with only 8 butterfly units [20] that cause increase in speed. Output of stage n is the input of stage (n+1). Output of butterfly unit is fed back to the input. Multiplexer’s select lines s0, s1 determine the stages while s2 incurs the scalability to the proposed architecture.
E. Discrete Cosine Transform

Discrete Cosine Transform is a Fourier related transform, dealing with real numbers only. 2D DCT, one of the efficient functions, is used for different compression techniques.

N point 1D DCT is defined by

\[
Y[k] = \frac{2}{N} \sum_{n=0}^{N-1} X[n] \cos \left( \frac{2\pi}{N} (2n+1)k \right) \tag{11}
\]

Where, \( k = 0, 1, \ldots, N-1 \)

\[
C_k = \begin{cases} 
\frac{1}{\sqrt{2}} & \text{When, } k=0 \\
1 & \text{else}
\end{cases}
\]

The formula of 2D DCT can be computed by row-column decomposition of two 1D DCTs. 1D DCT blocks along row and column implement 2D DCT. In the proposed architecture of 1D Fast Discrete Cosine Transform, it has been implemented by Distributed Arithmetic [16], [19] in Fig. 8. DCT constant coefficient for \( N = 16 \) can be represented as:

\[
A = \cos \frac{\pi}{8}, 
B = \cos \frac{3\pi}{8}, 
C = \cos \frac{5\pi}{8}, 
D = \cos \frac{7\pi}{8}, 
E = \cos \frac{\pi}{2}, 
F = \cos \frac{3\pi}{2}, 
G = \cos \frac{5\pi}{2}, 
H = \cos \frac{7\pi}{2}, 
I = \cos \frac{\pi}{4}, 
J = \cos \frac{3\pi}{4}, 
K = \cos \frac{5\pi}{4}, 
L = \cos \frac{7\pi}{4}, 
M = \cos \frac{\pi}{8}, 
N = \cos \frac{3\pi}{8}, 
O = \cos \frac{5\pi}{8}, \text{ and } Q = \cos \frac{7\pi}{8}
\]

The matrix has been decomposed into even and odd subscript matrices. Even subscript matrix has been decomposed again into 4x4 matrices. Odd subscript matrix has been decomposed into a number of 4x4 matrices followed by adders.

III. PROPOSED RECONFIGURABLE ARCHITECTURE

The proposed reconfigurable architecture consists of CMs like adders, substractors, multipliers, scaling units, registers etc. for ‘Linear Transforms’ (DWT, FFT and DCT) and ‘Filter functions’ (FIR and IIR) in Fig. 9. Interconnection Matrix basically connects these CMs for a specific configuration. Different control signals define different configuration modes of the architecture, as shown in TABLE IV. A separate Decoder block has been introduced for generation of the control signal and selection of configuration mode. One configuration can be made at a time.

| Control Signals for Different Configuration Modes |
|-----------------------------------------------|
| Control Function | C1 | C2 | C3 | C4 | C5 |
|------------------|----|----|----|----|----|
| FIR              | 1  | 0  | 0  | 0  | 0  |
| IIR              | 0  | 1  | 0  | 0  | 0  |
| DCT              | 0  | 0  | 1  | 0  | 0  |
| FFT              | 0  | 0  | 0  | 1  | 0  |
| DWT              | 0  | 0  | 0  | 0  | 1  |
IV. RESULTS AND ANALYSIS

The reconfigurable architecture has been validated on Virtex-5 FPGA. The synthesis report has been discussed below.

A. Final Reports

Selected Device: 5vlx330tff1738-2
Number of Slice Registers: 7476 out of 207360 3%
Number of Slice LUTs: 4686 out of 207360 2%
Number used as Logic: 4686 out of 207360 2%
Number of IOs: 886

Slice Logic Distribution:
Number of Bit Slices used: 8829
Number with an unused Flip Flop: 1353 out of 8829 15%
Number with an unused LUT: 4143 out of 8829 46%
Number of fully used Bit Slices: 3333 out of 8829 37%

Timing Summary:-
Speed Grade: -2
Minimum period: 4.937ns
Maximum Frequency: 202.558MHz
Minimum input arrival time before clock: 4.222ns
Maximum output required time after clock: 2.799ns

Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 3 out of 32 9%
Number of DSP48Es: 24 out of 192 12%
Requirements: 7476 slices, 4686 LUTs, 886 IOB.

B. Analysis

| Func            | Counter | Adder | LUT | Sub | Register | MUX    | Multiplier |
|-----------------|---------|-------|-----|-----|----------|--------|------------|
| FIR             | -       | 3     | 32  | -   | 16       | 1(2:1) | -          |
| IIR             | -       | 6     | 62  | -   | 31       | 1(2:1) | -          |
| DWT (DECIMATOR) | 1(1BIT) | 8     | 8   | -   | 9        | -      | -          |
| FFT             | -       | 6     | 4   | 48  | 48       | 16(4:1)| 14(2:1) 24|
| DCT             | -       | 4     | 24  | 3   | 32       | 8(2:1) | -          |

The Reconfigurable Architecture has been implemented using only one 1bit counter, 62 adders, 94 LUTs, 36 subtractors, 24 multipliers as shown in TABLE IV. Reconfigurable architecture has been implemented using 4686 slice LUTs out of 207360 slice LUTs of FPGA whereas, FPDA is the alternative architecture to implement this combined architecture with only 94 LUTs. This Proposed DSP dedicated Reconfigurable Architecture combines different DSP functions here with optimized silicon area compare to FPGA.
In Fig. 10, Blue indicates minimum number of LUTs which are needed to implement the combined architecture in FPGA. In contrast, Brown indicates the minimum number of LUTs that are needed to implement the same architecture in FPDA.

Fig. 10 Simulation result of 16 tap FIR filter

Fig. 11 shows the comparison of device utilization factors of ‘Combined Architecture’ on virtex-5 FPGA with utilization of only 3% of slice register. Only 37% fully used bit slice Out of 8829. Number with an unused Flip Flop in bit slices is 15%. 46% of the bit slices with at least an unused LUT. It is clear from the above analysis, that implementation of DSP functions on FPGA has a serious bottleneck of lower utilization factor. “FPDA” is an array of basic common modules (CMs). Interconnections among those modules configure the device for a specific DSP function. The proposed reconfigurable architecture “FPDA” has relatively better utilization factor compare to FPGA.

Fig. 11 Comparison of Device utilization Factor

Fig. 12 shows the timing comparison between different DSP functions on the proposed architecture. Worst case timing from a flip-flop to other flip-flop through the logic within the FPGA is termed as “minimum period” i.e. 4.937ns for the proposed architecture when implemented on virtex-5 FPGA. “Minimum input arrival time before clock” is the worst case input data setup time requirement to clock pin has been reported 4.222ns. This minimum input arrival time before clock is maximum for configuration of DCT. The worst case data output delay after clock pin which is same in all cases, is termed as “Maximum output required time after clock” in the final report. No combinational data path from input to output. “FPDA” will offer high speed as configuration is basically interconnections among basic modules of DSP instead of complex interconnections in FPGA.

There are so many advantages to realize DSP algorithms in the proposed FPDA architecture other than FPGA:

- different DSP functions can be made by changing the connectivity among the basic building blocks,
- placement & routing of basic building blocks in such a fashion that it should be optimum in delay than FPGA,
- architecture has a low design complexity,
- higher utilization factor than FPGA,
- high degree of parallelism and scalability.
V. CONCLUSIONS

The proposed “Reconfigurable Architecture” includes ‘Filter Functions’ and ‘Linear Transforms’. The combined circuit is basically the union of all the basic building blocks mentioned above and they are required for implementing each of the functions. By interconnecting different building blocks in different fashions various DSP functions can be made. This process can be viewed as “Configuration”. The architecture also offers scalability as new transforms with higher number inputs or higher tapped filter functions can also be implemented with those basic building blocks. The problems of inflexibility of ASICs, low utilization factor and low performance of FPGAs can be overcome with the proposed architecture as the major building blocks which are common to most of the DSP functions are implemented by direct hardware and not by LUT thereby optimizing the silicon utilization factor. Only one configuration can be made at a time which can be observed as a limitation of the architecture. But, minimization and maximum utilization of the hardware have been achieved at the cost of mentioned limitation. The future work can be proceed with

- the VLSI implementation of the proposed architecture,
- the implementation of different filter or linear transform functions in the proposed architecture and globalize the architecture for implementation of all DSP functions,
- implementation of high speed building blocks to achieve comparatively more faster architecture,
- time and hardware complexity analysis of the proposed hardware with other DSP functions and analysis the feasibility.

Employing Distributed Arithmetic approach for FIR, IIR, DWT and DCT functions and exploitation of the inherent parallelisms of the DSP functions, enhance the speed of the proposed architecture over the FPGAs substantially.

The Proposed architecture was validated on Xilinx virtex-5 FPGA on 5vx330tf1738-2 using Xilinx ISE 9.1i.

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