Staggered parallel asymmetric boost converter based on coupled inductor

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Abstract. Aiming at the problems of insufficient voltage gain, excessive voltage stress and current stress of switches in DC boost converters, an interleaved parallel asymmetric boost converter is proposed. The circuit adopts interleaved parallel boost converters, coupled inductors and switched capacitors to form an asymmetric boost converter structure, so that the voltage gain of the converter is more than twice that of the traditional coupled inductor boost converter; and it adopts the passive clamp circuit to eliminate the switch voltage spike at the moment of turn-off, so that the voltage stress and current stress on the switch devices are reduced. The simulation results show that the boost converter obtains high voltage gain and high efficiency, and is suitable for applications with large DC boost ratio.

1. Introduction
The DC boost converter is the key part of photovoltaic power generation and motor drive, which is required to have the characteristics of high voltage gain, low voltage stress and high efficiency [1]. The traditional boost converter and interleaved parallel boost converter achieve high gain by controlling the switch duty cycle, but the boost ratio is limited by the duty cycle, and the switch current stress and voltage stress are large, which will reduce the switch life [2-3]. In addition, the diode reverse recovery problem will increase the loss of the diode [4]. In order to improve the voltage gain, Literature [3] uses an interleaved structure to reduce the current stress. Two capacitors are connected in series on the output side to achieve high voltage gain, but the boost ratio is still limited by the duty cycle. Literature [5] uses diode-capacitor ladder to achieve high voltage gain on this basis. However, its volume and cost are increased. In order to solve the problem that the parasitic parameters affect the duty cycle, the design of coupled inductor instead of the original inductor is introduced. Since the turn ratio can be set, the control degree of freedom also increases the voltage gain. The leakage inductor in the coupled inductor completes the zero-current-switch (ZCS) turn-on operation of the switch, and the reverse recovery problem of the diode is suppressed. The traditional coupled inductor boost converter has greater switch voltage stress and current stress due to its leakage inductor. In order to solve this problem, Literature [6] proposes a passive clamp circuit consisting of capacitors and diodes to absorb the leakage inductor energy and suppress the voltage spike when the switch is turned off, but the voltage stress of the related devices is still a little large.

Therefore, while improving the voltage gain of the boost conversion, it should also be able to suppress the voltage and current stress of the switch components. This paper proposes to adopt the interleaved parallel boost converter, and obtain a new kind of high voltage gain interleaved parallel asymmetrical boost converter by integrating the existing circuits and devices mainly, such as the...
coupled inductor and the switched capacitor. Compared with the traditional coupled inductor boost converter, the voltage gain is improved due to the coupled inductor and the switched capacitor; the leakage inductor energy is absorbed by the passive clamp circuit, which suppresses the switch voltage spike, the voltage and current stress of the switch are also reduced, and its efficiency is also improved.

2. Interleaved parallel asymmetric boost converter

2.1. Circuit configuration
The proposed converter mainly integrates the existing circuits and devices to form a new boost converter and is shown in Figure 1. Compared with the traditional interleaved parallel boost converter, the original inductor is replaced by the two pairs of coupled inductors \( L_{11} \) and \( L_{12} \), \( L_{21} \) and \( L_{22} \). The voltage gain can be improved by controlling turn ratio and the switch duty cycle. And the coupled inductor also eases the diode reverse recovery problem. In addition, passive clamp circuits are formed by the diodes \( D_{C1} \), \( D_{C2} \) and capacitors \( C_{C1} \), \( C_{C2} \) on the primary sides of the coupled inductors \( L_{11} \) and \( L_{21} \), which are used to absorb leakage inductor energy and recirculate it to the circuit, thereby suppress the switches \( S_{1} \) and \( S_{2} \) voltage spikes at the moment of turn-off; the capacitors \( C_{2} \) and \( C_{3} \) also improve voltage gain, and the diode \( D_{3} \) provides a conduction loop for circuit.

![Figure 1. The proposed converter.](image1)

The coupled inductor can be equivalent to: an ideal transformer with the primary and secondary turn ratios of \( n_{12}/n_{11} \) and \( n_{22}/n_{21} \), which are connected in parallel with the magnetizing inductors \( L_{m1} \) and \( L_{m2} \), and then connected in series with the leakage inductors \( L_{s1} \) and \( L_{s2} \). Therefore, when analyzing the proposed converter, the equivalent circuit can be analyzed. In addition to the above-mentioned parameters, \( U_{in} \) is the input voltage source; \( D_{1} \) and \( D_{2} \) are the output rectifier diodes; \( C_{1} \) and \( C_{2} \) are output capacitors; \( R \) is the load resistance.

2.2. Working modal analysis
In order to simplify the working principle and process analysis of the proposed converter, the following assumptions are given: (1) All diodes and switch devices are considered ideal. (2) All capacitors are large enough to neglect their voltage ripple. (3) The duty ratio \( D \) of the main switches \( S_{1} \) and \( S_{2} \) are equal, and between 0.5-1, working in continuous mode. (4) The coupled inductor is modeled as an excitation inductor, a leakage inductor and an ideal transformer, and the turn ratio is \( n=n_{12}/n_{11}=n_{22}/n_{21} \). (5) Due to the short turn-on and turn-off time of the main switches, its process analysis is omitted.

![Figure 2. Clamp circuit analysis.](image2)

![Figure 3. Correlation waveforms of the proposed converter.](image3)
The clamp circuits of $D_{C1}$, $C_{C1}$ and $D_{C2}$, $C_{C2}$ mainly absorb the energy of $L_{s1}$ and $L_{s2}$ at $S1$, $S2$ turn-off time to suppress voltage spikes. In order to simplify the analysis, the process is not analyzed at its turn-off time. Therefore, before analyzing the modal process, the principle and process of the passive clamp circuit when the switch $S1$ starts to be turned on are introduced here to understand the action process as shown in Figure 2. When $S1$ is turned off, $D_{C1}$ starts to conduct. The leakage energy stored in $L_{s1}$ is absorbed by the clamp capacitor $C_{C1}$ and decreases linearly. Finally, $i_{Ls1}$ reaches zero. The clamp circuits composed of $D_{C2}$, $C_{C2}$ has similar role and process, so no more introduction.

A working process $T$ are divided into 4 modes. The main waveforms are roughly shown in Figure 3 and the equivalent circuits of four modes are shown in Figure 4- Figure 7, where $g_1$ and $g_2$ are the switches $S1$ and $S2$ turn-on signals; $U_{S1}$ is the $S1$ voltage, $U_{D1}$ is the voltage across the diode $D_1$; $i_{s1}$ is the current flowing through $S1$. In addition, there are the voltage $U_{S2}$ and the current $i_{S2}$ across the switch $S2$ and the voltage $U_{D2}$ across the diode $D_2$. Although the converter has an asymmetric structure, the voltage at both ends of the switch device and the flowing current are basically similar in the subsequent analysis and calculations, so only one of the waveforms is drawn. Before $t_0$, $S1$ and $S2$ are both in the on state, and $L_{m1}$, $L_{s1}$ and $L_{m2}$, $L_{s2}$ are charged by $U_{in}$.

**Figure 4. Mode 1.**

**Figure 5. Mode 2.**

**Figure 6. Mode 3.**

**Figure 7. Mode 4.**
Mode 3 ($t_2$-$t_3$): At $t_2$, $S_2$ is turned off. In this mode, the magnetizing inductor current $i_{L_{m2}}$ charges $C_1$ through the secondary side of the coupled inductor and $D_2$. Since $S_1$ remains on, $U_{in}$ charges $L_{m1}$ and $L_{s1}$. In addition, $U_{in}$ and $C_2$ are connected in series to transmit energy to the load $R$. The linear reduction of $i_{L_{m2}}$ is shown in Equation (3). In Equation (3), $U_{CC2}$ is the voltage across $C_{C2}$.

$$i_{L_{m2}} = I_{L_{m2}}(t_2) + \frac{U_{in} - U_{CC2} - U_{in}}{L_{m2}}(t-t_2)$$ (3)

Mode 4 ($t_3$-$t_4$): Mode 4 is the same as Mode 2. Excitation current and leakage inductor current are shown in Equation (4).

$$i_{L_{m2}}(t) = I_{L_{m2}}(t_3) + \frac{U_{in}}{L_{m2} + L_{s2}}(t-t_3)$$ (4)

3. Converter performance analysis

The proposed converter can use a simple control strategy (constant duty cycle control) to compare performance. However, other methods can be used to achieve greater efficiency in some special cases.

3.1. Converter voltage gain

In this converter, since $L_{m1} >> L_{s1}$ and $L_{m2} >> L_{s2}$, $L_{s1}$ and $L_{s2}$ are ignored in the calculation. According to the voltage-second balance principle of the inductor, voltage-second balance can be written for $L_{m1}$ and $L_{m2}$ which results in Equation (5).

$$U_{in}D_T = (U_{C_1} - U_{in} - U_{CC2})(1-D)T \Rightarrow \begin{cases} U_{in}D = \frac{(U_{C_1} - U_{in} - U_{CC2})(1-D)}{n} \\ U_{in}D = \frac{(U_{C_1} - U_{in} - U_{CC2})(1-D)}{n} \end{cases}$$ (5)

$U_{CC1} = U_{CC2}$ can be calculated from Equation (5). Similarly, in this circuit, since the value of the capacitor is large enough and in order to simplify the voltage relationship, $C_1$ and $C_2$ are considered the same, and according to the circuit diagram, the Equation (6) can be obtained.

$$\begin{cases} U_{C_1} + U_{C_2} = U_0 \\ U_{C_1} = U_{C_2} \end{cases} \Rightarrow U_{C_1} = U_{C_2} = U_0$$ (6)

According to the work process analysis, $C_{C1}$ and $C_{C2}$ recover the energy of the leakage inductor. By using the KVL principle, the voltages of $C_{C1}$ and $C_{C2}$ are determined as Equation (7).

$$U_{C_{C1}} = U_{C_{C2}} = \frac{U_{C_1} - U_{in}}{1 + n} = \frac{U_0 - U_{in}}{1 + n}$$ (7)

By substituting Equations (6) and (7) into Equation (5), the voltage gain of the converter can be obtained as Equation (8).

$$\frac{U_0}{U_{in}} = \frac{2(nD + 1)}{1 - D}$$ (8)

3.2. Voltages of switches

From the working process, the voltages of $S_1$ and $S_2$ can be obtained as Equation (9).

$$U_{S1} = U_{S2} = U_{C_{C1}} + U_{in}$$ (9)

Substituting Equations (7) and (8) into (9), the switches voltages can be obtained as Equation (10).

$$U_{S1} = U_{S2} = \frac{U_0}{2(nD + 1)} = \frac{1 - D}{2} U_{in}$$ (10)

3.3. Converter performance comparison

Table 1 compares the voltage gain, switch voltage of the proposed converter, traditional interleaved parallel boost converter, Literature [1] and Literature [7], respectively.
Table 1. Comparison of converter parameters.

| converter parameters      | voltage gain          | switch voltage         |
|---------------------------|-----------------------|------------------------|
| the proposed converter    | \(\frac{2(nD+1)}{1-D}\) | \(\frac{U_0}{2(nD+1)}\) |
| traditional interleaved parallel boost converter | \(\frac{1}{1-D}\) | \(U_0\) |
| Literature [1]            | \(\frac{2}{1-D}\)    | \(\frac{U_0}{2}\)     |
| Literature [7]            | \(\frac{D+n}{(1-D)n}\) | \(\frac{nU_0}{1+n}\) |

The duty ratio of the proposed converter is \(0.5<D<1\), \(n\) is a positive integer. Assuming that the denominator of the voltage gain in Table 1 is \(1-D\), the numerator value of the proposed converter is greater than 3 and the numerator value in the Literature [7] is between 1-2. So the voltage gain of the proposed converter is the largest. Similarly, the size relation between the switch voltages can also be obtained. Thereby, the proposed converter can achieve higher voltage gain and lower switch voltage. According to the Table 1, the voltage gain \(\frac{2(nD+1)}{(1-D)}\) also increases as the turn ratio \(n\) increases.

4. Simulation results and analysis

In order to verify the voltage gain, voltage stress and current stress of the switch of the proposed converter, the model is established in the Simulink platform of MATLAB. The simulation parameters: \(U_{in}=25V\), \(n=1\); \(L_{m1}=L_{m2}=120mH\), \(L_{s1}=L_{s2}=6\mu H\); \(C_{C1}=C_{C2}=2\mu F\); \(C_1=C_2=2\mu F\); \(f=100kHz\); \(D=0.7\). For comparative analysis, the traditional coupled inductor boost converter simulation parameter settings are kept consistent. The \(t\) in Figure 8 starts from \(t=0\) and the \(t\) in Figure 9 to Figure 10 is the relative time.

Figure 8 shows the output voltage waveforms of the boost converter. It can be seen from Figure 8 that the output voltage \(U_0\) of the proposed converter is stabilized at 283.3V, while the output voltage \(U_0\) of the traditional coupled inductor boost converter can only boost to 139.9V. So the proposed converter voltage gain is more than twice that of the traditional coupled inductor boost converter and has a higher voltage gain.

Figure 9 shows the output switch voltage waveforms of the boost converter. It can be seen from Figure 9 that the output switch voltage of the proposed converter is more stable than the traditional coupled inductor boost converter.

![Figure 8. Comparison of the boost converter output voltage.](image)

![Figure 9. Comparison of the boost converter switch voltage.](image)
Figure 9 is the comparison of the boost converter switch voltage. The switch voltage $U_S$ of the proposed converter is basically constant at 83V, and there is no voltage spike due to the switch being turned off. In the traditional coupled inductor boost converter, although the switch voltage $U_S$ is also 83V, there is a large voltage spike. Therefore, it can be concluded that the influence of the switch voltage spike is suppressed, so that the voltage stress is reduced.

![Figure 9: Comparison of boost converter switch voltage](image)

(a) Traditional coupled inductor switch current  
(b) The proposed switch current

**Figure 9.** Comparison of the boost converter switch voltage.

Figure 10 is the comparison of the boost converter switch current. It can be seen that the current $i_S$ of the proposed converter is basically constant at 0.85A, while the switch current $i_S$ is about 1.8A in the traditional coupled inductor boost converter, and there is a spike. Therefore, it can be concluded that the switch current in the proposed converter has a smaller current stress.

![Figure 10: Comparison of boost converter switch current](image)

**Figure 10.** Comparison of the boost converter switch current.

Figure 11 is the comparison of the boost converter output efficiency. When the power is between 0-200W, the efficiency of the proposed converter can reach the maximum efficiency 94.22% when the power is 140W, and the traditional coupled inductor converter reaches 91.02%, so the efficiency of the proposed converter is improved.

![Figure 11: Comparison of boost converter output efficiency](image)

**Figure 11.** Comparison of the boost converter output efficiency.

In summary, the voltage gain of the proposed converter is more than twice that of the traditional coupled inductor boost converter; the switch voltage spike is suppressed, so that the voltage and current stress are smaller. The efficiency is higher and more stable, so the converter can run efficiently and stably.

5. Conclusions

The simulation results shows that the proposed interleaved parallel asymmetric boost converter uses coupled inductors and switched capacitors to form an new asymmetric boost converter and make the conversion. When the turn ratio is 1, its voltage gain is more than twice that of the traditional coupled inductor boost converter, and the voltage gain also increases as the turn ratio increases. The passive clamp circuits suppress the switch voltage spike, the voltage and current stress of the switch are reduced. In addition, the efficiency of the converter has been improved. Therefore, the boost converter is suitable for large conversion ratio occasions of DC boost conversion, and has better feasibility.

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References

[1] Wang G P and Zhu L J 2020 A staggered parallel symmetric boost converter Journal of Guangxi Normal University (Natural Science Edition) 38(4) 11-20

[2] Yazici I 2015 Robust voltage-mode controller for DC-DC boost converter IET Power Electron 8(3) 342-349

[3] Wang P, Zhou L, Zhang Y, et al 2017 Input-parallel output-series DC-DC boost converter with a wide input voltage range, for fuel cell vehicles IEEE Transactions on Power Electronics 66(9) 7771-7781

[4] Chen J Y, Niu P J and Gao S W 2017 Research and simulation of two-phase interleaved parallel boost converter Electrical Engineering 5(1) 42-51

[5] Priyadarshi A, Kar P K and Karanki S B 2020 A wide load range ZVS high voltage gain hybrid DC-DC boost converter based on diode-capacitor voltage multiplier circuit International Transactions on Electrical Energy Systems 30(1)

[6] Kianpour A and Shahgholian G 2017 A floating-output interleaved boost DC–DC converter with high step-up gain Automatika 58(1) 18-26

[7] Shi L L and Zhu L J 2016 A new type of high-gain boost converter Journal of Henan University of Science and Technology (Natural Science Edition) 37(6) 51-54+60