Investigating microwave loss of SiGe using superconducting transmon qubits

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Silicon-Germanium (SiGe) is a material that possesses a multitude of applications ranging from transistors to electro-optical modulators and quantum dots. The diverse properties of SiGe also make it attractive to implementations involving superconducting quantum computing. Here we demonstrate the fabrication of transmon quantum bits on SiGe layers and investigate the microwave loss properties of SiGe at cryogenic temperatures and single photon microwave powers. We find relaxation times of up to 100 µs, corresponding to a quality factor Q above 4 M for large pad transmons. The high Q values obtained indicate that the SiGe/Si heterostructure is compatible with state of the art performance of superconducting quantum circuits.

Over recent years there have been significant developments within superconducting quantum processors. Currently small processors containing a few tens of qubits have been demonstrated. The operational fidelity of the processors are ever improving. It is realistic to believe that quantum algorithms will soon be able to outperform their classical counterparts in several areas. However, to achieve fault tolerant quantum computing a multitude of problems needs to be addressed. A major limitation of quantum processors based on superconducting circuits is the relatively short coherence time of the quantum bits (qubits). By improving the intrinsic coherence properties of the qubits the overhead for operating a fault tolerant logical qubit can be reduced. It is therefore of utmost importance that the coherence properties of the physical qubit are not degraded when new components or materials are incorporated in the quantum processor.

Superconducting quantum circuits have traditionally been fabricated on either undoped silicon substrates or on sapphire substrates in order to maintain high coherence. There is significant interest in expanding the functionality of superconducting quantum circuits by incorporating new materials and structures. One material of great interest for a number of quantum applications is Ge or Ge intermixed with silicon (Silicon-Germanium SiGe). Ge and SiGe have been incorporated in applications ranging from Josephson field effect transistors to spin qubits, and recently it has been proposed that SiGe can provide a pathway for on-chip optical to microwave transduction. Here we investigate the coherence properties of transmon qubits fabricated on a Si substrate where a heterostructure of SiGe capped by an additional layer of epitaxial silicon (epi-Si) has been added. The possibility to combine SiGe technology with highly coherent superconducting quantum circuits could have significant implications for the development of quantum devices and applications.

The main question we are trying to answer is if high coherence superconducting quantum circuits can be fabricated in conjunction with the growth of the Si/SiGe/Si stack. In order to test this hypothesis, we fabricate transmon devices with four different capacitor pad designs, as shown in FIG. 1, on top of the heterostructure (sample G) and compare them to devices fabricated on our standard bare Si substrate (sample S). The capacitors pads are engineered to have varying amounts of electric field stored in the different layers and interface. The transmons are fabricated in a planar circuit geometry where each qubit has an on-chip Coplanar Waveguide (CPW) resonator for state readout. Each of the four designs are fabricated on 4×8 mm2 chips with four identical qubits per chip. The readouts are addressed through a common feed line using hanger style capacitive couplings.

The starting substrate for sample fabrication is a 750 µm thick high resistivity (>1 kOhm-cm) 200 mm silicon wafer. The native oxide is removed just prior to SiGe growth through an in-situ 1050°C wafer anneal. A 100 nm thick SiGe layer with a Ge mole fraction of approximately 15% is epitaxially grown using Rapid Thermal Chemical Vapor Deposition (RTCVD) at a temperature of 650°C. This composition is commensurate with application to optical to microwave transduction that minimizes refractive index contrast and sensitivity to loss associated with scattering and absorption. The layer is limited to this thickness in order to minimize formation of defects in the SiGe. X-ray diffraction analysis of the SiGe film (not shown) confirmed a fully strained layer corresponding to a Ge fraction of approximately 16.5%. The SiGe is capped with a 50 nm layer of epitaxially grown Si. The effective dielectric constant for the Si1−xGe x layer is approximated through the expression \( \varepsilon_{\text{SiGe}} = \varepsilon_{\text{Si}} + 4.5x \) which for \( x = 15\% \) mole fraction gives \( \varepsilon_{\text{SiGe}} \approx 12.35 \). To form the superconducting circuitry a 200 nm thick layer of Niobium is sputtered on top of the Si/SiGe/epi-Si stack. The qubit capacitor pads and readout resonators are patterned using a subtractive process that incorporates optical lithography and Reactive Ion Etch (RIE). As can be seen in the cross-sectional, transmission electron microscope image, FIG. 1(b), the RIE process creates an over-etch of approximately 50 nm which leads to a partially exposed SiGe surface where the Nb has been removed. As a final step an Al2O3/Al Josephson junction is placed between the capacitor pads. The Josephson junction is fabricated using a Dolan bridge technique based on a PMMA/MMA resist stack and e-beam lithography. The aluminum is evaporated at two different angles with an oxidation step prior to the second deposition. Reference samples are formed on an identical Si substrate but without the presence of the SiGe and epi-Si.

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A major source of loss in superconducting qubits is attributed to Two Level Systems (TLS) that couple to the electric field of the qubits\textsuperscript{13,14} . The physical origin of the TLS’s is not fully understood but evidence suggests that they are primarily located at device surfaces and interfaces.\textsuperscript{21} More precise pinpointing of the TLS locations can be achieved using electrostatic gates.\textsuperscript{21} Such measurements indicate that the dielectric surfaces close to conductor edges, as well as the Josephson junction are areas of high TLS density. To estimate how much such regions of the circuit may contribute to the qubit loss, we determine the amount of electric field energy stored in each region. The electric field energy fraction is referred to as the filling factor or participation ratio. Due to the high aspect ratio of the interfacial layers for a typical transmon design (a few nm thickness and up to a few mm in the plane), the fact that the electric field diverges at the edges of the conductors, calculations of the filling factor are not straightforward. Several methods have been suggested for extracting surface participation\textsuperscript{15,18,20}. Here we calculate filling factors $F_L$ for the different interfaces and the SiGe and epi-Si layers $L$ using a 2D electromagnetic Finite Element (FEM) solver to extract the static electric field distribution for the qubit designs shown in Figure 1(a). For each design we create a cross-sectional model; for interdigitated capacitors (IDC) qubits (design A and B), a representative cross-section is taken across the fingers and for parallel plates (design C and D) across the pads as indicated by arrows in Figure 1(a). In the FEM model we assign a static differential voltage to the two capacitor pads of $+1$ V and $-1$ V and 0 V to any ground electrodes (further details on assumed interface layer thicknesses and dielectric constants are provided in Table I).

\[
F_L = \frac{\int_{V} \vec{E} \cdot \vec{D} \, dV}{\int_{V} \vec{E} \cdot \vec{D} \, dV}.
\]

Using the expression in Eq. (1) we can solve for the filling factors of the epitaxial Si capping layer, the SiGe layer as well as the other surfaces and interfaces of the device. The values are summarized in Table I. The combined surface loss can then be expressed as:

\[
\frac{1}{Q_{\text{tot}}} = \sum_{L} F_L \tan(\delta_{L}) + \delta_{\text{bg}}
\]

where $Q_{\text{tot}}$ refers to the measured qubit quality factors, $L \in \{\text{epi, SiGe, MS, MA, SA}_{\text{epi}}, \text{SA}_{\text{SiGe}}, \text{Si}\}$, $\tan(\delta_{L})$ the corresponding loss tangents and $\delta_{\text{bg}}$ represents all other sources of loss, such as radiation, quasiparticles, etc.

The devices were packaged and then measured in a $^3$He/$^4$He dilution refrigerator with a base temperature of approximately 15mK. In our setup the input lines are heavily attenuated (in total 70 dB of attenuation distributed over the different thermal stages such that the added thermal noise only corresponds to a few nK). The outputs from the four chips are routed through an electro-mechanical microwave switch and amplified by a HEMT amplifier. The samples are protected from thermal noise coming from the HEMT input by two 4-12 GHz cryogenic isolators, placed at the base temperature of the cryostat. One chip (4 qubits) of each design was measured.

\begin{table}
\centering
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline
Design & Epi-Si ($\times 10^{-2}$) & SiGe ($\times 10^{-2}$) & MS ($\times 10^{-3}$) & MA ($\times 10^{-4}$) & $SA_{\text{SiGe}}$ ($\times 10^{-4}$) & $SA_{\text{epi}}$ ($\times 10^{-4}$) \\
\hline
A & 2.4 & 6.68 & 2.40 & 4.08 & 2.37 & 1.57 \\
B & 0.74 & 2.20 & 0.76 & 1.02 & 0.78 & 0.39 \\
C & 0.41 & 1.24 & 0.42 & 0.54 & 0.44 & 0.21 \\
D & 0.18 & 0.56 & 0.19 & 0.21 & 0.20 & 0.08 \\
\hline
\end{tabular}
\caption{Filling factors of the SiGe layer, the epitaxial Si capping layer, the Metal-Substrate (MS), Metal-Air (MA) and the two Substrate-Air (SA) interfaces $SA_{\text{SiGe}}$ and $SA_{\text{epi}}$. The filling factors are calculated using a FEM solver employing a 2D cross-sectional geometry of the samples. The relative dielectric constant of Nb$_2$O$_5$ can vary vastly, in the calculations we are assuming $\varepsilon_r = 30$\textsuperscript{20} and a thickness of 5nm for MA, $\varepsilon_r = 3.9$ and a thickness of 2nm for MS and the two SA layers.}
\end{table}
TABLE II. Measured energy relaxation times and frequencies for each qubit of sample G (SiGe) and sample S (Si). The $T_1$ times are measured over a period of 3 hours with approximately 20 measurements each. The standard deviation of the $T_1$ measurements in a time series is typically in the range of 5-30%.

The For $Q_1$ on chip B the qubit pulses were not calibrated correctly so no data was acquired. †This outlier value is somewhat surprising and we have excluded it from the calculation of the mean value. It is possible that $Q_2$ on chip D was temporarily strongly coupled to a TLS that reduced the $T_1$ time significantly.

| Qubit (chip) | $T_1 (\mu s)/f_Q (GHz)$ | $T_1 (\mu s)/f_Q (GHz)$ | $T_1 (\mu s)/f_Q (GHz)$ | $T_1 (\mu s)/f_Q (GHz)$ |
|-------------|--------------------------|--------------------------|--------------------------|--------------------------|
| G           | 18.5/2.58                | 23.4/6.01                | -5.441                   | 48.6/3.29                |
| S           | 26.5/4.28                | 18.4/6.45                | 41.5/5.21                | 55.7/4.76                |
| G           | 28.5/5.73                | 13.4/6.70                | 58.5/6.87                | 53.4/7.62                |
| S           | 27.5/5.52                | 22.4/4.89                | 57.5/5.57                | 40.4/9.06                |
| G           | 80/5.567                 | 90/4.622                 | 71/4.575                 | 79/4.657                 |
| S           | 59/4.767                 | 89/4.674                 | 95/4.786                 | 107/4.89                 |
| G           | 130/5.460                | 71/4.735                 | 114/5.635                | 81/4.686                 |
| S           | 49/4.773                 | 83/4.672                 | 110/5.448                | 87/4.742                 |

Mean $24.7/5.492$ $194.602$ $52/5.552$ $49/4.773$ $94/5.462$ $83/4.672$ $110/5.448$ $87/4.742$

FIG. 2. Extracted bounds of the loss tangent for six layers and interfaces. The loss corresponding to the reciprocals of the measured quality factors ($1/Q$) for the different qubit designs is plotted as a function of participation for the different layers SiGe, epi-Si, MS, SA, SiGe, and SA$_{epi-Si}$. The slope of the linear fit gives an upper bound on the loss tangent for the different interfaces. (a) Metal-substrate interface for sample G and S. (b) Substrate-Air interface for sample S and G. (c) For sample G, the sidewall components of the SA interface are all Si and the trench bottom is SiGe. By subtracting the sidewall loss we can get a bound for the SiGe-Air interface. (d) Bounds on the loss tangents for the SiGe layer and the epi-Si layer respectively.

in a single cooldown. The frequencies and energy relaxation times ($T_1$) are shown in Table II where we see the expected trend that qubit designs with closely spaced capacitor pads exhibit lower $T_1$.

From the $T_1$ and qubit frequency ($f_Q$) we extract the quality factors $Q_{tot} = 2\pi f_Q/T_1$. The qubit frequencies are approximately 0.65 to 1.1 GHz higher for SiGe devices, however the small coupling to the readout resonators (< 50 MHz), large detuning (> 1.2 GHz) and a small resonator kappa (< 1 MHz) leads to a Purcell induced relaxation time of at least 550 microseconds for any of the qubits. We therefore concluded that Purcell loss is not impacting the observed energy relaxation times in a significant manner. The total loss ($1/Q_{tot}$) for each design is plotted as a function of filling factor for the different interfaces in FIG. 2. From a linear fit we extract an upper bound for the loss tangent of each interface or layer. The fits for the SiGe and epi-Si layers correspond to upper bounds on the loss tangent of $\tan(\delta_{SiGe}) < 1.56 \times 10^{-5}$ and $\tan(\delta_{epi}) < 4.26 \times 10^{-5}$ respectively (see FIG. 2(d)). Even though these values are orders of magnitude larger than that of bulk Si (< $3 \times 10^{-7}$) they confirm that high qubit quality factors can be achieved in the presence of such layers. It is also reasonable to assume that the actual loss of the SiGe and epi-Si could be significantly lower than these bounds, considering that devices formed on bare Si substrates typically do not outperform the devices measured here. As discussed previously the Nb overetch stopped just at the interface between the SiGe and the epi-Si. We hence divide the substrate-air (SA) interface into two parts: the Si sidewalls and the SiGe trench surface. If we use the extracted loss tangent for SA of sample S we can subtract the loss contribution of the sidewalls and get a more accurate bound on the SiGe-Air interface loss. This is indicated in FIG. 2(c). We find a bound on the loss tangent of $1.58 \times 10^{-3}$ which suggests that the SiGe-Air interface is as good if not better than the Si-Air interface, which could explain why sample G outperforms sample S in a majority of the cases.

We also measured the $T_2$ echo times ($T_{2\varepsilon}$) of the devices, plotted in FIG. 3. We find that the $T_{2\varepsilon}$ values tend to not be fully $2 \times T_1$ limited but are typically closer to $T_1$ indicating that our experimental setup also produces a significant fraction of external dephasing. To determine if the SiGe layer introduces any extra sources of dephasing we extract a $T_{2\varepsilon}/T_1$ ratio averaged over all qubits for each substrate. For the devices fabricated on a pure Si substrate we arrive at a value of 1.365 whereas for the SiGe substrate the value is 1.37, suggesting that the SiGe does not contribute excess dephasing over that from pure Si substrates.

To conclude, we have fabricated high coherence transmon qubits on a stack of Si/Si$_{0.95}$Ge$_{0.05}$/epi-Si layers, and observe $T_1$ and $T_{2\varepsilon}$ times in excess of 100 microseconds, on par with state of the art transmon devices. We find that even though these layers are relatively thick, their electric energy participation still scales in a fashion similar to surface participation for the different capacitor designs. By naïvely assigning all loss to one of the layers we can estimate an upper bound on...
FIG. 3. Measured $T_2$, values for all of the qubits. The lines represent the mean $T_1$ and $2T_1$ boundaries for the S (dashed) and G (dotted) samples. As is commonly observed for transmon qubits the $T_2$ values do not reach the theoretical limit of $2T_1$ but tend to lie between $T_1$ and $2T_1$. The mean $T_2/T_1$ ratio for the SiGe sample is found to be comparable to the reference Si sample, suggesting that the presence of SiGe does not add any additional channels of dephasing over those associated with the bare Si substrate.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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