HipBone: A performance-portable GPU-accelerated C++ version of the NekBone benchmark.

Noel Chalmers¹, Abhishek Mishra², Damon McDougall¹, and Tim Warburton³

Abstract

We present hipBone, an open source performance-portable proxy application for the Nek5000 (and NekRS) CFD applications. HipBone is a fully GPU-accelerated C++ implementation of the original NekBone CPU proxy application with several novel algorithmic and implementation improvements which optimize its performance on modern fine-grain parallel GPU accelerators. Our optimizations include a conversion to store the degrees of freedom of the problem in assembled form in order to reduce the amount of data moved during the main iteration and a portable implementation of the main Poisson operator kernel. We demonstrate near-roofline performance of the operator kernel on three different modern GPU accelerators from two different vendors. We present a novel algorithm for splitting the application of the Poisson operator on GPUs which aggressively hides MPI communication required for both halo exchange and assembly. Our implementation of nearest-neighbor MPI communication then leverages several different routing algorithms and GPU-Direct RDMA capabilities, when available, which improves scalability of the benchmark. We demonstrate the performance of hipBone on three different clusters housed at Oak Ridge National Laboratory, namely the Summit supercomputer and the Frontier early-access clusters, Spock and Crusher. Our tests demonstrate both portability across different clusters and very good scaling efficiency, especially on large problems.

Keywords
Nekbone/Nek5000/NekRS, high performance computing, CUDA, HIP, GPU-Direct, gather-scatter communication, high-order, spectral element discretization

Introduction

Nek5000 (Fischer et al. 2008a) is a high-order incompressible Navier-Stokes solver used in large-scale computational fluid dynamics applications. It is widely used in the computational fluid dynamics (CFD) research community and is commonly used on the world’s largest supercomputers. Understanding how large complex applications will perform on new and evolving architectures is made easier by distilling key computational components into proxy applications. NekBone” is a proxy-application for Nek5000 and only solves for the pressure term in the Navier-Stokes equations since the pressure solve is one of the most computationally intensive portions of solving the incompressible Navier-Stokes equations. NekBone is a Tier-1 CORAL-2 benchmark¹ and will be used to demonstrate performance on the all of the initial exascale supercomputer systems funded by the US Department of Energy CORAL-2 program.

With the growing popularity of highly heterogeneous system architectures, in particular systems with nodes containing one or more accelerators, there is a increasing need for high-performance computing (HPC) applications to leverage the often significantly higher throughput accelerators offer over traditional CPUs. Early efforts to adapt the finite element methods (FEM) to GPU accelerators were presented by Göddeke et al. (2007a), and Göddeke et al. (2007b). Shortly after, both Klöckner et al. (2009) and Komatitsch et al. (2009) demonstrated accelerated high-order FEM implementations using CUDA. Since these seminal works, GPUs have gradually grown in popularity for FEM applications. To name only a few, Dong et al. (2014) detail the porting of a large FEM hydrodynamics application to leverage GPU acceleration, Kronbichler et al. (2017) and Kronbichler et al. (2018) and show results of using GPUs in the deal.II FEM library, and Beams et al. (2020) detail applying GPU-accelerated batch linear algebra routines to FEM applications.

As accelerated parallel processing becomes more ubiquitous, portability between different vendors becomes of concern as each platform may offer several different (and often competing) programming models which enable developers to extract high throughput from accelerators. Some of the most popular programming models are OpenMF, OpenACC, …
CUDA, HIP, OpenCL™, and SYCL™, but few of these are available/consistent across all vendors, and those that are often rely on advanced and slow-moving compiler technologies. This is especially true for Fortran applications such as Nek5000, where native options are limited to OpenMP, OpenACC, or CUDA Fortran for GPU-acceleration.

There have been several efforts to enable GPU-acceleration in the Nek5000 application. In a series of papers, Gong et al. (2014), Markidis et al. (2015), Cebamanos et al. (2014), Otero et al. (2019), and Vincent et al. (2021) have studied an OpenACC version of Nek5000. As is natural for a proxy application, these efforts often begin by studying the porting and performance of NekBone. Gong et al. (2016) demonstrated a GPU-accelerated version of NekBone using OpenACC and CUDA Fortran. This version was later improved by Karp et al. (2020) using native CUDA C

While the studies of utilizing OpenACC in NekBone and Nek5000 have shown some success, the increasing landscape of GPU-accelerated systems as part of the US Exascale initiative has made extracting even more performance from GPU accelerators, across several GPU vendors, imperative. It is therefore desirable to explore implementing Nek5000 on other programming models using some portability framework. To this end, a new GPU-accelerated version of Nek5000, namely NekRS, was presented by Fischer et al. (2021). NekRS is an open-source C++ version of Nek5000, providing access to the standard Nek5000 interface and features allowing users to leverage existing application-specific source code and data files on GPU-based platforms. NekRS is built off an early fork of the libParanumal project by Chalmers et al. (2020), a self-contained high-order finite element library that uses highly optimized kernels and leverages the Open Concurrent Compute Abstraction (OCCA) (see Medina et al. (2014)) for performance and portability across several parallel programming models.

In this paper we present hipBone, a C++ implementation of the main components of NekBone, which serves as a proxy for NekRS in much the same way as NekBone does for Nek5000. Like NekRS, hipBone is written using several simplified libParanumal libraries and leverages performance portability via OCCA. From the outset, we designed hipBone to be portable, to extract high performance from modern GPU accelerators, and scale to many GPUs in a compute cluster. With this design in mind, we describe several implementation and algorithmic differences between hipBone and NekBone. Notably, we choose to store the degrees of freedom of the global problem in assembled form, which significantly reduces the amount of data motion in each iteration of the benchmark at the cost of needing two distinct nearest neighbor communication phases. To counter this, we also present a novel splitting algorithm for computing the action of the main operator in hipBone which aggressively hides MPI communication overheads by local computation. We also implement several routing algorithms to perform the nearest neighbor MPI communications, and leverage GPU-Direct RDMA technologies in MPI when available. We demonstrate high performance of the main operator kernel, and then present scaling studies on some current-generation GPU accelerators to demonstrate that hipBone obtains high performance and scalability on many GPUs.

The remainder of this paper is organized as follows. We begin by giving an overview of the algorithm used in NekBone and the computations performed. We then give an overview of the hipBone benchmark, describing the major implementation differences with NekBone, including the Poisson operator kernel, data layout, MPI nearest-neighborhood collectives, and communication hiding. We present near optimal performance of the Poisson operator kernel in hipBone on NVIDIA Tesla V100, AMD Instinct MI100, and AMD Instinct MI250X GPU accelerators. Finally, we demonstrate efficient scaling of the hipBone benchmark using the Oak Ridge National Laboratory (ORNL) Summit supercomputer, as well as the Frontier early-access Spock and Crusher clusters at ORNL, and give some concluding remarks.

The NekBone Benchmark

The NekBone benchmark solves a screened Poisson equation discretized via the spectral element method (SEM) using a conjugate gradient iterative method. It is formulated to serve as a proxy-application for the principal computational phase of the Nek5000 application (see: Fischer et al. (2008a)).

The full Nek5000 application is an open-source Fortran code for simulating incompressible flows. Nek5000 uses MPI for parallel communication, but otherwise has no additional threading or GPU acceleration. The discretization scheme used in Nek5000 is based on the spectral-element method (see: Patera (1984) and Tufo and Fischer (1999)). In particular, the domain is discretized into hexahedral elements and the high-order polynomial basis functions are chosen as the tensor-product of Lagrange polynomials, interpolating the Gauss-Legendre-Lobatto (GLL) quadrature points.

The NekBone benchmark follows a similar design to the Nek5000 application; NekBone is an open-source Fortran code, using MPI for parallelization. NekBone implements a Conjugate Gradient (CG) iterative method (listed in detail in Algorithm 1) to solve a screened Poisson equation. In particular, NekBone runs a fixed 100 iterations of the CG method, recording the total time taken, and outputting a computed floating-point operations per second (FLOPS) metric as the figure-of-merit (FOM).

The problem setup in NekBone consists of regular mesh of \( E \) hexahedral elements, together with a degree \( N \) polynomial discretization amounting to \( (N+1)^3 \) interpolation points on each element. Collected across the entire mesh, this totals to \( N_L = E(N+1)^3 \) element-local interpolation points. However, as many points are shared between one or more elements along element boundaries, the actual number of degrees-of-freedom (DOFs), \( N_G \), is strictly smaller than \( N_L \). The exact number depends on the mesh geometry and boundary conditions, but \( N_G \approx EN^3 \) for large meshes.

The screened Poisson operator in NekBone can be written as

\[
A = S + \lambda I,
\]

where \( S \) is SEM discrete Laplacian operator, and \( I \) is the identity matrix. The discrete Laplacian is derived from the...
typical variational form of the Laplacian. It can be written as an ‘assembled’ action from each element, that is

$$S = Z^T S_L Z.$$ \hfill (2)

While not explicitly formed, the sparse \(N_L \times N_G\) matrix \(Z\) in (2), also called simply the ‘scatter’ operator, is a boolean matrix containing a single non-zero per row, encoding the connectivity of the global mesh of grid-points. Its transpose, \(Z^T\) is often called the ‘gather’ operator. The reader is referred to Canuto et al. (2012), Deville et al. (2002), and Henderson and Karniadakis (1995) for a more complete description of the gather and scatter operators. As these operations involves data from neighboring elements, the entirety of the MPI communication required for the SEM Poisson operator are contained in these operations.

The \(N_L \times N_L\) matrix \(S_L\) in (2) is block-diagonal, each block \(S_L^e\) corresponding to element \(e\) and can be written as a product of several operators:

$$S_L^e = D^T G^e D.$$ 

Here, \(D\) is a \((3(N+1)^3) \times (3(N+1)^3)\) discrete gradient operator which can be written in the following tensor-product form

$$D = \begin{pmatrix} D \otimes I \otimes I \\ I \otimes D \otimes I \\ I \otimes I \otimes D \end{pmatrix},$$

where \(D\) is the \((N+1) \times (N+1)\) one-dimensional SEM derivative operator, and \(I\) is the identity matrix. The metric tensor geometric factor, \(G^e\), is a \((3(N+1)^3) \times (3(N+1)^3)\) matrix which has the following symmetric form:

$$G^e = \begin{pmatrix} G_{er}^e & G_{es}^e & G_{et}^e \\ G_{es}^e & G_{ss}^e & G_{st}^e \\ G_{et}^e & G_{st}^e & G_{tt}^e \end{pmatrix},$$

where each \(G^e\) is a diagonal \((N+1)^3 \times (N+1)^3\) matrix of pointwise values of the corresponding entry of the element’s metric tensor, combined with GLL quadrature weights.

The tensor product form allows the local Poisson operators, \(S_L^e\), to be implemented using highly-tuned matrix-matrix multiplication routines in the NekBone benchmark. Since each multiplication by the one-dimensional derivative matrix \(D\) requires \(2(N+1)^2\) FLOPs, the application of the full gradient operator \(D\) and its transpose \(D^T\) require \(12(N+1)^4\) FLOPs per element. On the other hand, the multiplication of the geometric factors \(G^e\) requires only \(15(N+1)^3\) FLOPs per element.

 Rather than storing the length \(N_G\) DOF vector \(x_G\), NekBone, like Nek5000, instead stores the scattered vector \(x_L = Zx_G\), which has length \(N_L\). This requires extra memory, since \(N_L > N_G\), but has the effect that computing the action of the screened Poisson operator in (1) can be written as

$$b_G = Ax_G,$$

$$Zb_G = Z(Z^T S_L Z + \lambda I)x_G,$$

$$b_L = (Z(Z^T S_L + \lambda I))x_L.$$ 

That is, the action of the discrete Laplacian, \(S\), can be computed by applying the element-local \(S_L\) to \(x_L\), followed by the ‘gather-scatter’ operator, \(ZZ^T\). Since all MPI communication is contained inside this operation, a combined gather-scatter routine is implemented and communication is done using custom exchange algorithms implemented inside the gsllib library, based on the work of Tufo (1998) and Fischer et al. (2008b). An in-depth study of the performance of specialized communication routines in NekBone on structured grids was present by Ivanov et al. (2015).

Storing the DOF vector in the scattered form leads to a subtlety in the CG iteration. Since the scattered vectors have repeated values whenever degrees of freedom are shared between elements, computation of global inner products as part of the CG method therefore requires a ‘weighted’ variant, where each contribution to the global summation is weighted by the inverse counting vector (i.e. the entries of the diagonal matrix \(Z^T Z\)). This weight vector is pre-computed and of length \(E(N+1)^3\), but the computation of inner product does require reading this vector from memory and performing \(E(N+1)^3\) additional FLOPs. Taking the weighted inner products into account, the total FLOP count per CG iteration is the sum of the total FLOP count for the evaluation of the screen Poisson operator, together with the assortment of vector operations as part of the CG iteration. The NekBone benchmark uses the total of \(12E(N+1)^4 + 34E(N+1)^3\), FLOPs per CG iteration in order to compute its FLOPS figure-of-merit.

**HipBone**

HipBone, our re-implementation of the NekBone benchmark, is built upon a core set of libraries from the open-source finite element library libParanumal (cf. Chalmers et al. (2020)). These core libraries provide routines for simple hexahedral mesh generation, finite element operator construction, accelerated linear algebra and linear solvers, and nearest-neighbor communication collectives.

As part of the libParanumal core, hipBone uses the Open Concurrent Compute Abstraction (OCCA) library (cf. Medina et al. (2014)) to abstract between different parallel...
programming models such as OpenMP, OpenCL™, CUDA, HIP, and SYCL™. OCCA is a required dependency of libParanumal and provides a portable abstraction through a unified API which allows users to implement parallel kernel code in a (slightly decorated) C++ language, called OKL. As runtime, the user can specify which parallel programming model to use. OCCA then translates the OKL source code into the desired target language and Just-In-Time (JIT) compiles kernels for the user’s target hardware architecture. Leveraging JIT compilation also allows different vendor compilers additional optimization, e.g., loop unrolling.

The hipBone benchmark itself is fairly lightweight on top of the libParanumal libraries. In addition to simple vector operator kernels, the benchmark contains only two additional kernels. The first is used only once to populate a pseudo-random initial forcing vector, and the second is the performance-critical screened Poisson operator.

HipBone does not replicate the full functionality of NekBone at this point in time. Most notably, hipBone does not form of preconditioning in the CG iteration, while NekBone supports simple diagonal preconditioning as well as a much more sophisticated hybrid-Schwarz multigrid preconditioner detailed in Lottes and Fischer (2005). We omit this functionality for now in order to first focus on optimized GPU performance, portability, and scalability of the Poisson operator and streaming operations in hipBone, leaving the topic of preconditioning on modern GPU accelerators for future study. There are, additionally, several key algorithmic/implementation differences between hipBone and NekBone. In the remainder of this section, we overview the most significant changes and their impact on performance.

### DOF Storage

As described above, the NekBone benchmark stores the DOF vectors in scattered form, with \( N_L \) entries instead of \( N_G \). This implementation choice has the benefit of allowing the MPI communication required in the Laplacian operator to be combined into a single gather-scatter operation, reducing MPI messaging latency costs. This is especially beneficial when strong-scaling a fixed problem size to many MPI ranks. The trade-off, however, is that vectors are now (potentially significantly) longer. Indeed, \( \frac{N_L}{N_G} \approx \frac{(N+1)^3}{N^2} \), which is still a 21.3% overhead at the relatively high order of \( N = 15 \). Furthermore, global reduction operations such as inner products require accessing an additional weight vector, leading to even more required data movement during each CG iteration.

Each of the vector operations in the CG iteration are of very low arithmetic intensity, i.e. they perform very little (often less than one) FLOPs per byte of data loaded from main memory. Even the element-local Laplacian operator has a fairly low arithmetic intensity, owing to the tensor-product form. Such low arithmetic intensity operations are often referred to as ’streaming’ operations, and their runtimes often are well-modeled by an Amdhal-like model \( t = \alpha + \beta B \), where \( \alpha \) is some fixed latency cost, \( \beta \) is an effective asymptotic streaming bandwidth, and \( B \) is the amount of data moved in the operation. The reader is referred to Hockney (1982) and Hockney (1985) for a more complete discussion, and more recently Chalmers and Warburton (2020) who studied streaming performance on several modern GPU-accelerators. With GPUs, the \( \alpha \) term includes the latency cost of off-loading a kernel to the device and eventually synchronizing back with the host process. This is often referred to as a kind of ‘kernel launch latency’. However, once a significant amount of data is moved in HBM (typically \( \sim 10\text{MB} \)), performance becomes dominated by the effective HBM bandwidth of the accelerator, \( \beta \).

When targeting modern GPU-accelerators, the implementation choice of storing vectors in scattered form in NekBone has the effect of increasing data movement (therefore reducing effective performance) for large problem sizes. On the other hand, it also reduces MPI latency costs for small problem sizes, but in this regime the GPU’s performance is primarily limited by kernel launch latency. With hipBone, we are interested in the case where the problem size is at least large enough to saturate the main memory bandwidth of the GPU. We therefore have made the implementation choice to store the DOF vectors in their assembled ordering. With this choice, vectors in the CG iteration become length \( N_G \), rather than \( N_L \), and some data motion, such as the accessing the weight vector in the global inner products, is avoided completely. This allows for significant effective performance improvements for large problems in each of the vector operations in the CG iteration. This design choice also aligns closely with the implementation of libParanumal’s elliptic solvers, and the MFEM finite element library (cf. Anderson et al. (2021)).

### Poisson Operator

The performance of the SEM Laplacian operator on hexahedral elements on modern GPU-accelerators has been studied previously by several authors. Remacle et al. (2016) presented an implementation of a high-order spectral element elliptic solver on GPU accelerators. In this work, the authors detail a Laplacian kernel that exploits fine-grain parallelism of the accelerator by mapping each of the elements to distinct threadblocks, and assigning each DOF in an element to an individual GPU thread. This approach creates a 3D thread structure of \( (N+1)^3 \) in each threadblock. This approach was limited to \( N = 9 \) due to the 1024 thread-per-block limit in CUDA, and \( N = 5 \) due to OpenCL’s limit of 256 work-items per work-group on AMD GPUs.

The approach of Remacle et al. (2016) was later extended by Świrydowicz et al. (2019) as part of the Center for Efficient Exascale Discretizations (CEED) Exascale Computing Project co-design center4. In this work, the authors studied the GPU-implementation and optimization of several high-order finite element operators, including mass matrix multiplication, and diffusion matrix multiplication with/without higher-order quadrature rules. The case of the diffusion operator without higher-order quadrature is particularly useful for our hipBone implementation, as this aligns very closely with the screened Poisson operator in NekBone. The authors detail two optimized kernel implementations. The first follows the approach of

---

4 [http://ceed.exascaleproject.org](http://ceed.exascaleproject.org)
Remacle et al. (2016) by using a 3D threadblock structure, but has additional optimizations such as processing several elements in a single threadblock for small polynomial orders, $N$. The second implementation uses a layer-by-layer processing of the hexahedral element, mapping individual GPU threads to $(N+1)^2$ nodes of a single face of the hexahedral (see for instance Stilwell (2013)). This implementation makes heavy use of register space, but allows for higher polynomial order $N$ to be used. Both implementations heavily rely on shared memory as a scratchpad to store temporaries, and many of the FLOPs performed in the kernels have one or more of the inputs/outputs residing in shared memory. This can become a performance limiter as arithmetic intensity increases, as inputs/outputs residing in shared memory. This can become significantly slower than performing the FLOP.

In hipBone, we implement a single kernel to compute an intermediate vector $y_L = (S_L + \lambda W) Z x_G$, where $W$ is a diagonal matrix of the inverse degree weights which can be defined as the diagonal matrix which satisfies $Z^T W = I$. We compute this intermediate vector $y_L$ so that the final action of the Poisson operator $A$ can be computed by gathering $y_L$, i.e. $A x_G = Z^T y_L$, which requires MPI communication. To compute $y_L$, we use a combined approach of the 3D and 2D threadblock structure kernels from Świrydowicz et al. (2019), with some minor changes. First, for $N < 9$ we use the 3D threadblock kernel, while for larger $N$ we use the 2D threadblock structure kernel. The decision to use the 2D threadblock kernel for $N = 9$ is made based on empirical performance measurements and current generation GPU accelerators, but is configurable. We also implement a blocking strategy in both kernel implementations, which allows for multiple elements to be processes by a single threadblock. This helps to minimize idle threads in warps/wavefronts. Finally, we slightly alter the storage of the geometric factors, $G'$, so that all geometric factors at a given degree of freedom in an element are packed together. When SIMD lanes of a processor subsequently load the first geometric factor, the load will be strided since each lane loads factors different degrees of freedom. However, this load populates the lowest-level cache, and the packed storage format makes the loads of the remaining geometric factors more efficient.

The fused action of $S_L + \lambda W$ and $Z$ into a single kernel is a notable difference in our implementation compared to that presented by Świrydowicz et al. (2019). This fusing causes the reading of the element-local DOFs into the local memory on the processor to be an indirect read of $x_G$. This requires additional indexing data to be stored in memory and read-in by the kernel before accessing entries of $x_G$, but the ordering of elements in the mesh and repetition of DOFs shared between elements can allow for some entries of $x_G$ to be found in cache during this indirect load. With MPI parallelism, this indirect read also relies on a halo region to be populated with DOFs belonging to other processes. We detail this procedure, and the MPI parallelization of the gather operator $Z^T$, below.

The total amount of data moved through main memory and the total FLOPs done by the Poisson operator can be estimated as follows. First, the load of $x_G$ into element-local storage requires a 4 byte index, encoding a row of the scatter operator $Z$, to load each 8 byte entry of $x_L$, totaling to $12N_L$ bytes loaded. With perfect caching of repeatedly used entries of $x_G$, the amount of data moved from main memory can actually be as low as $8N_G + 4N_L$. The load of the six geometric factors in $G'$ and inverse degree count $W$ for each of the $N_L$ entries total to an additional $56N_L$ bytes, and the write of the final $8N_L$ bytes for the output of $y_L$ brings the total data motion to approximately $8N_G + 68N_L \approx 8E N^3 + 68E(N+1)^3$ bytes, assuming perfect caching. The FLOP count, on the other hand, consists of $12E(N + 1)^4 + 15E(N + 1)^3$ FLOPS to apply $S_L$ and $3E(N + 1)^3$ additional FLOPS to add the $\lambda W$ contribution, for a total of $12E(N + 1)^4 + 18E(N + 1)^3$ FLOPS.

With these estimates for data motion and FLOP count, we model the compute rate, $R$, of the screened Poisson operator kernel, in FLOPS, using a typical roofline model:

$$R = \min \left( C, \frac{12(N+1)^4 + 18(N+1)^3}{8N^3 + 68(N+1)^3} B \right),$$

where $C$ is the peak compute rate of the processor in FLOPS, and $B$ is the peak (bidirectional) bandwidth of the processor’s main memory in bytes/s. As most current-generation GPU accelerators have peak FP64 compute rates typically measured in TFLOPS, and peak HBM memory bandwidths near 1 TB/s, we see that the low arithmetic intensity of the Poisson operator implies performance will be primarily limited by memory bandwidth, even for large degrees $N$. We demonstrate this on several accelerators in the computational tests below.

**MPI Communication**

The global mesh of hexahedral elements in hipBone is parallelized over multiple processes by partitioning the mesh evenly among the $P$ processes. Message passing between process is then done via MPI, with a given processes requiring communication from processes that border it along a face, edge, or corner of an element. While the mesh used in NekBone and hipBone is a structured cube of uniform hexahedrals, the message passing algorithms used assume no underlying mesh structure. This more accurately represents the larger Nek5000 and NekRS codes, which are generally unstructured.

In hipBone, we have re-written and extended the functionality of the gslib library, used in NekBone and Nek5000 for MPI communication, to a ‘device-aware’ gather-scatter library. This new library replicates the combined gather-scatter operations provided by gslib, and as well as its various communication algorithms, on both host memory or OCCA device buffers. The library also provides new gather, scatter, and halo exchange operations, which are needed for the screened Poisson operator in the assembled DOF ordering. Since each of these MPI communication operations in the new library can cast as a sparse nearest-neighbor collective operation, and the underlying communication algorithms from the gather-scatter operation can be re-used for other operations. The library also supports leveraging GPU-Direct RDMA capabilities by directly passing pointers to device memory to MPI calls when the MPI library being used is “GPU-aware”. This allows the MPI implementation to leverage high
bandwidth GPU-to-GPU or GPU-network links in a system when they are present.

Our new device-aware gather-scatter library implements the following exchange routines for nearest neighbor collective communication:

**All-to-all** The simplest of the exchange routines, the All-to-all exchange performs all required data movement between via a single `MPI_Alltoallv` function. This exchange heavily relies on existing optimized sparse all-to-all communication algorithms in the MPI implementation. Since this MPI function is one of most general MPI collective patterns, the performance of this algorithm is typically not optimal.

**Pairwise** Another relatively simple exchange algorithm, the pairwise exchange implements the nearest neighbor collective operation by simply having every process send/receive all needed data to/from its neighbors, using several calls to `MPI_Isend` and `MPI_Irecv`. This exchange algorithm communicates using the maximum number of MPI messages, thereby incurring the maximum amount of messaging latency, but with direct routing moves the least amount of data possible. For very large problems where the inter-process exchanges are sensitive to the bandwidth of the network and not messaging latency, this exchange likely performs well.

**Crystal Router** The crystal router algorithm performs the nearest neighbor collective via recursive hypercube folding. The algorithm is described in full by Lamb et al. (1988), and some performance results of this algorithm’s use in Nek5000 were presented by Schleipake and Laure (2014). For a $P$ process grid, the algorithm can be summarized as follows: divide the grid in half and pair each process $p_l$ in the lower half with a distinct process $p_h$ in the upper half. Then, if process $p_l$ has data needed by *any* process in the upper half, it sends that data to $p_h$, and vice versa for its partner $p_h$. The algorithm then proceeds recursively on the two halves of the grid.

The crystal router performs the nearest neighbor collective in $\lceil \log_2(P) \rceil$ bidirectional messages, thereby minimizing the total number of messages sent/received. With a suitable distribution of the global mesh, such as that obtained by recursive mesh bisection, some messages may be avoided altogether. The amount of data sent and received in total, however, is larger than the pairwise exchange. This exchange routine, therefore, is primarily useful for smaller problems that are sensitive to network latency.

During the initial setup of the gather-scatter library, each of the exchange routines is timed, and the fastest exchange is selected for use in subsequent communication operations. When exchanging device-resident data, the gather-scatter library must either move the needed data to host memory, after which the host calls the MPI routines, or use GPU-aware MPI routines where available. In either case, a buffer of the data needed for communication is first extracted from the input vector using a device kernel. After this kernel completes, the user is free to queue additional work to the device to hide some or all of the time spent in MPI routines. Once the communication is complete on the host or device, the communication buffer is scattered back to its original order in the input vector. The exchanges, in addition to the MPI messaging latency costs, also incur device synchronization and kernel launch latency costs during the exchange as the host process must synchronize with the device to ensure the communication buffer is ready to be sent with MPI. When performing a crystal router exchange in device memory with GPU-aware MPI, we incur $\lceil \log_2(P) \rceil$ total device synchronizations and kernel launch latencies, as intermediate kernels are required to prepare the data to be sent in the next hypercube fold. As this exchange is primarily useful for small, latency-sensitive problems, it is unlikely for the device-resident crystal router to be the fastest exchange.

**Overlapping halo and gather communication**
At a high level, the Poisson operator application in hipBone is broken down into three stages: halo data communication, element-local Poisson operator application, and finally a gather operation. The first and third stages both require MPI communication, thus any efforts to hide this communication by local computation will greatly improve scaling efficiency. To describe how such communications are hidden, it is useful to first define a few terms relating to the degrees of freedom in elements owned by an arbitrary MPI process (Figure 1).

An arbitrary MPI process has ‘ownership’ of a number of spectral elements, meaning that in the scattered DOF storage each element, i.e. its constituent nodes, is stored entirely on a single distinct MPI rank. At the inter-process boundary between elements in the global mesh are nodes which are contained in two or more elements owned by different processes. We call these nodes, ‘halo nodes’, and all other nodes we call ‘interior nodes’. ‘Halo elements’ are subsequently defined as elements which contain at least one halo node and ‘interior elements’ are all elements that are not halo elements. In Figure 1, we depict this for the case of two processes in two dimensions for simplicity. In the figure, each process owns nine quadrilateral elements with a degree $N = 3$ grid of interpolation nodes, and the inter-process boundary between them leads to several halo nodes in six halo elements. On each process, each of red-shaded elements is a halo element and the six remaining blue-shaded elements are interior elements. Within each halo element is a mixture of interior and halo nodes. In Figure 1, the halo nodes are colored red and the interior nodes are colored blue.

While there is a well-defined notion of ‘ownership’ of an element by a process, in the assembled DOF storage each element, i.e. its constituent nodes, is stored entirely on a single distinct MPI rank. At the inter-process boundary between elements in the global mesh are nodes which are contained in two or more elements owned by different processes. We call these nodes, ‘halo nodes’, and all other nodes we call ‘interior nodes’. ‘Halo elements’ are subsequently defined as elements which contain at least one halo node and ‘interior elements’ are all elements that are not halo elements. In Figure 1, we depict this for the case of two processes in two dimensions for simplicity. In the figure, each process owns nine quadrilateral elements with a degree $N = 3$ grid of interpolation nodes, and the inter-process boundary between them leads to several halo nodes in six halo elements. On each process, each of red-shaded elements is a halo element and the six remaining blue-shaded elements are interior elements. Within each halo element is a mixture of interior and halo nodes. In Figure 1, the halo nodes are colored red and the interior nodes are colored blue.

While there is a well-defined notion of ‘ownership’ of an element by a process, in the assembled DOF storage each element, i.e. its constituent nodes, is stored entirely on a single distinct MPI rank. At the inter-process boundary between elements in the global mesh are nodes which are contained in two or more elements owned by different processes. We call these nodes, ‘halo nodes’, and all other nodes we call ‘interior nodes’. ‘Halo elements’ are subsequently defined as elements which contain at least one halo node and ‘interior elements’ are all elements that are not halo elements. In Figure 1, we depict this for the case of two processes in two dimensions for simplicity. In the figure, each process owns nine quadrilateral elements with a degree $N = 3$ grid of interpolation nodes, and the inter-process boundary between them leads to several halo nodes in six halo elements. On each process, each of red-shaded elements is a halo element and the six remaining blue-shaded elements are interior elements. Within each halo element is a mixture of interior and halo nodes. In Figure 1, the halo nodes are colored red and the interior nodes are colored blue.

While there is a well-defined notion of ‘ownership’ of an element by a process, in the assembled DOF storage each element, i.e. its constituent nodes, is stored entirely on a single distinct MPI rank. At the inter-process boundary between elements in the global mesh are nodes which are contained in two or more elements owned by different processes. We call these nodes, ‘halo nodes’, and all other nodes we call ‘interior nodes’. ‘Halo elements’ are subsequently defined as elements which contain at least one halo node and ‘interior elements’ are all elements that are not halo elements. In Figure 1, we depict this for the case of two processes in two dimensions for simplicity. In the figure, each process owns nine quadrilateral elements with a degree $N = 3$ grid of interpolation nodes, and the inter-process boundary between them leads to several halo nodes in six halo elements. On each process, each of red-shaded elements is a halo element and the six remaining blue-shaded elements are interior elements. Within each halo element is a mixture of interior and halo nodes. In Figure 1, the halo nodes are colored red and the interior nodes are colored blue.

While there is a well-defined notion of ‘ownership’ of an element by a process, in the assembled DOF storage each element, i.e. its constituent nodes, is stored entirely on a single distinct MPI rank. At the inter-process boundary between elements in the global mesh are nodes which are contained in two or more elements owned by different processes. We call these nodes, ‘halo nodes’, and all other nodes we call ‘interior nodes’. ‘Halo elements’ are subsequently defined as elements which contain at least one halo node and ‘interior elements’ are all elements that are not halo elements. In Figure 1, we depict this for the case of two processes in two dimensions for simplicity. In the figure, each process owns nine quadrilateral elements with a degree $N = 3$ grid of interpolation nodes, and the inter-process boundary between them leads to several halo nodes in six halo elements. On each process, each of red-shaded elements is a halo element and the six remaining blue-shaded elements are interior elements. Within each halo element is a mixture of interior and halo nodes. In Figure 1, the halo nodes are colored red and the interior nodes are colored blue.
is launched to apply the action of \((S_L + \lambda W)Z\) to all the halo elements.

At this point, all that is left to do is to apply the operator to the other half of the interior elements, and then gather the intermediate vector \(y_L\). The interior nodes do not need to send any data to other process for the gather operation, and so the strategy for hiding MPI communication in the gather is similar to the strategy used for hiding the halo data communication. Following the kernel which computes the local operator application on the halo elements, we queue a kernel to gather values at the halo nodes into MPI buffers to be communicated as part of the global action of \(Z^T\). Once the buffers are assembled, a kernel is launched to compute the action \((S_L + \lambda W)Z\) on the remaining half of the interior elements. Another kernel, which computes the entirely process-local action of the gather operator \(Z^T\) is also queued at this point. While both of these kernels are executing, the MPI communication required for the gather operator is performed, and the resulting gathered values at the halo nodes is written to the output vector. We show a graphical representation of this procedure in Figure 2. The figure illustrates a possible timeline of host and device activity during the application of the Poisson operator.

**Conjugate gradient Iteration**

The remaining operations in the Conjugate Gradient method are relatively simple. After computing \(Ap\) for the current \(p\) vector in line 7 of Algorithm 1, the operations for the remainder of the iteration are each simple vector operations. The only remaining MPI communication required comes with the computation of global inner products \(r \cdot r\), and \(p \cdot Ap\). Implementing these global reductions along with the rest of the vector operations in the CG iteration offered some additional opportunities for optimization.

We assume that at the beginning of the \(j\)-th iteration we have already computed the current value of \(r_j \cdot r_j\). The computation of \(\alpha\) in line 7 of Algorithm 1 only requires the inner product \(p \cdot Ap\), which we locally compute with a dedicated inner product kernel on each rank, and complete with a MPI_Allreduce. Using \(\alpha\), we compute \(r_{j+1}\) and simultaneously accumulate the local inner product \(r_{j+1} \cdot r_j\). Fusing this reduction with the update of \(r\) avoids the need for a separate kernel to read the vector \(r\) again. Moreover, the subsequent MPI_Allreduce call which completes the global reduction can be well-hidden by first queuing a kernel which performs the AXPY update of \(x\) in line 8 of Algorithm 1 beforehand. This optimization slightly improves scaling efficiency by hiding the latency-sensitive MPI collective communication time.

For the entire CG iteration, recall from the discussion above that the screened Poisson operator kernel moves a total of \(8N_N + 68N_L\) bytes through main memory. The gather operator \(Z^T\) reads a vector of length \(N_L\), along with a compressed sparse-row (CSR) encoding of the non-zero structure of \(Z^T\), and outputs a vector of length \(N_G\) totaling to 12\(N_G + 12N_L\) bytes moved through main memory. The remaining vector operations; the inner product, fused AXPY and inner product, and two AXPYs, total to 11 more reads and writes of vectors from main memory, totaling \(88N_G\) bytes. This brings the total data motion to

\[
108N_G + 80N_L \approx 108EN^3 + 80E(N + 1)^3.
\]
bytes moved per CG iteration. Similarly, the number of FLOPs done by the screened Poisson kernel is \(12E(N + 1)^4 + 18E(N + 1)^3\), the subsequent gather performs \(E(N + 1)^3\) FLOPs, and the remaining vector operations require only \(10NG\) FLOPs, bringing the total FLOPs to approximately
\[
12E(N + 1)^4 + 19E(N + 1)^3 + 10EN^3, \tag{5}
\]
FLOPs per CG iteration. Comparing this to the FLOP count (3) used in the original NekBone benchmark, hipBone’s FLOP count has the same leading order term, \(12E(N + 1)^4\), from the screened Poisson operator application, but performs slightly fewer FLOPs overall due to the unweighted inner products and smaller vector sizes. This difference has only a minor impact on the reported FOM in FLOPS. For consistency with other NekBone studies, we use the original FLOP count from NekBone when reporting the FOM in our numerical experiments below.

### Computational Tests

This section describes the computational studies we performed on three different machines at the Oak Ridge Leadership Compute Facility (OLCF): Summit, Spock, and Crusher. Summit\(^\dagger\) is an IBM system, each node consisting of a dual socket configuration of two IBM POWER9 CPUs, six NVIDIA Tesla V100 GPUs, and one dual-rail 100Gbps Mellanox Connect X-5 EDR InfiniBand network card. Spock\(^\ddagger\) is an HPE system, each node consisting of a single socket AMD EPYC 7662 CPU, four AMD Instinct MI100 GPUs, and one HPE Slingshot 100Gbps network card. Finally, Crusher\(^\mathsection\) is an HPE Cray EX supercomputer system serving as a Frontier early-access system, each node consisting of a single socket optimized 3rd Gen EPYC 64 core processor, four AMD Instinct MI250X accelerators, and four HPE Slingshot 200Gbps network interfaces.

On Summit, we use GCC v9.1.0 as our C++ compiler,CUDA v11.0.3 to JIT compile device kernels, and Spectrum-MPI v10.4.0 as the MPI implementation. On Spock, we use GCC v11.2.0 as our C++ compiler, ROCm v4.5.0 to JIT compile HIP kernels, and Cray-MPICH v8.1.12 as the MPI implementation. Finally, on Crusher we GCC v11.2.0 as our C++ compiler, ROCm v4.5.2 to JIT compile HIP kernels, and Cray-MPICH v8.1.12 as the MPI implementation. For each of these systems, we perform several performance and scaling studies and present their results below.

#### Poisson Operator Performance

Our first test measures the performance of the screened Poisson operator kernel on each of the three different GPU accelerators considered, as its performance is critical to the overall performance of the benchmark. To isolate the performance on each accelerator, we use a single NVIDIA Tesla V100, a single AMD MI100, and one of the two Graphics Compute Die (GCD) on the AMD Instinct MI250X Multi-Chiplet Module (MCM). It is important to note that while each GCD in the MI250X presents as a distinct GPU to the operating system, the two GCDs on the MI250X share the total power budget on the full MI250X MCM. Testing on a single GCD, therefore, allows for the GCD to potentially use more than half of the overall power budget of the MI250X, and operate at high clock frequencies than one would observe when running the same workload on both GCDs simultaneously. For the operator tests in this section, however, in which performance is predominately bound by HBM streaming rates, we have not observed any significant performance difference between kernels executed on a single GCD of the MI250X, or both GCDs in the MCM simultaneously.

We measure the performance of the Poisson operator kernel by time-averaging 50 back-to-back invocations of the kernel for each polynomial degree \(N = 1, \ldots, 15\). For each degree, we use a fixed mesh of elements, chosen large enough so that the number of DOFs in the mesh is approximately \(NG \approx 40\) million. This helps to minimize effects such as kernel launch latency, threadblock scheduling latency and tail effects, and core clock variations due to temporary boosting.

We also compute, for each device, an empirically calibrated roofline using the model in equation (4). We use as the peak bandwidth, \(B\) in the roofline model, not the quoted theoretical peak of each device’s HBM memory, but rather an empirically measured peak streaming rate. To measure this rate, we use a simple streaming kernel in which each thread in the threadblocks only reads 8 FP64 values from main memory, and writes back one FP64 value. This 8:1 read-write ratio closely matches the data movement of the Poisson operator kernel, but is also idealized in that there is no unstructured load, no data re-use in cache, and the kernel uses a uniform threadblock size. We compute an asymptotic streaming rate for this kernel using the methodology described in Chalmers and Warburton (2020), finding streaming rates of \(B = 810\) GB/s for the NVIDIA Tesla V100, \(B = 982\) GB/s for the AMD Instinct MI100, and \(B = 1117\) GB/s for a single GCD of the AMD Instinct MI250X. We do not treat these streaming rates, nor the roofline model itself, as absolute bounds on the performance of the Poisson operator kernel. Rather, we use this roofline model as guidance for what one would expect the performance of the operator kernel to be, if it were to read and write data to main memory as efficiently as a pure streaming kernel.

We show the results of the Poisson operator performance test in Figure 3. We show the performance in GFLOPS of the operator kernel for each \(N = 1, \ldots, 15\) on the NVIDIA Tesla V100, AMD Instinct MI100, and a single GCD of the AMD Instinct MI250X in Figures 3a, 3b, and 3c, respectively. For each device, we see that the measured operator performance closely matches the empirical roofline model for \(N < 9\), indicating near-optimal performance of the 3D threadblock kernel described above. At \(N = 9\) and beyond, wherein the kernel implementation switches to the 2D threadblock algorithm, performance becomes more variable, with some degrees falling significantly below the roofline. This is especially noticeable in the performance on the AMD Instinct MI100 which sees a performance dip

\[^\dagger\text{https://docs.olcf.ornl.gov/systems/summit_user_guide.html}\]
\[^\ddagger\text{https://docs.olcf.ornl.gov/systems/spock_quick_start_guide.html}\]
\[^\mathsection\text{https://docs.olcf.ornl.gov/systems/crusher_quick_start_guide.html}\]
Some important metrics regarding the occupancy of the Poisson operator kernel. For each polynomial degree, \( N \), the threadblock size of the 2D threadblock operator kernel is \((N + 1)^2\). This threadblock is then divided into several 32-lane-wide ‘warp’ on the NVIDIA Tesla V100, and 64-lane-wide ‘wavefronts’ on the AMD GPUs. Any additional threads in excess of the threadblock size are simply masked out when executing on the hardware. Each warp/wavefront then has access to a number of vector registers. On the NVIDIA Tesla V100, a warp is able to reserve a maximum of 255 128B vector registers (each register being 32 lanes of 4B words) within a Stream Multiprocessor (SM) on the GPU. Similarly, on the AMD GPUs each wavefront is able to reserve a maximum of 256 256B vector registers (each register being 64 lanes of 4B words) in each Compute Unit (CU). While terminology between the GPU vendors differ, they share the property that warps/wavefronts reserving large amounts of register space can substantially affect the number of warps/waves which can be simultaneously active on an SM/CU. Each GPU’s SMs/CUs have vector register files that are divided evenly between four SIMD units, with both the NVIDIA Tesla V100 SMs and the AMD Instinct MI100 CUs having a total of 256KB of vector register space, and the AMD Instinct MI250X CUs having 512KB of vector register space. The ‘occupancy’ of a kernel then refers to the average number of warps/wavefronts which are active on each SM/CU during the kernel’s execution. Other constraints, such as the requirement that all warps/wavefronts from a given threadblock must occupy the same SM/CU can also restrict the occupancy of a kernel.

We list in Table 1 some metrics regarding the occupancy of the Poisson operator kernel on each of the GPUs considered above. For each threadblock size, we list the number of warps/wavefronts required to decompose the block. We then list the number of vector registers required by each warp/wavefront to execute the kernel, information we extract from the assembly generated by the compiler. Using these values, we list the occupancy of the operator kernel both in terms of warps/wavefronts active per SM/CU, and in terms of how many spectral elements each SM/CU processes while occupied.

Comparing the occupancy metrics of the operator kernel on the AMD Instinct MI100 on the NVIDIA Tesla V100 in Table 1 to the achieved performance in Figure 3b, we see that the drop in performance observed at \( N = 11 \) corresponds to a drop in occupancy on each CU. The occupancy drop itself is caused by the threadblock size of \( 144 \) requiring one additional wavefront at the same register usage compared to at \( N = 11 \). While performance continues to climb after \( N = 11 \), the gap between the measured performance and the roofline is never fully recovered. Despite the departure from the roofline model on each GPU, all the devices achieve the highest GFLOPS at the highest polynomial degree \( N = 15 \), with the NVIDIA Tesla V100 achieving 2101.4 GFLOPS, the AMD Instinct MI100 achieving 2135.2 GFLOPS, and a single GCD of the AMD Instinct MI250X achieving 2774.9 GFLOPS.

The inefficiencies that appear in the Poisson operator kernel for large \( N \) may be due to the combination of high register pressure, masked threads, and large threadblocks. To gain some insight into these effects, we can consider some important metrics regarding the occupancy of the Poisson operator kernel. For each polynomial degree, \( N \), the threadblock size of the 2D threadblock operator kernel is \((N + 1)^2\). This threadblock is then divided into several 32-lane-wide ‘warp’ on the NVIDIA Tesla V100, and 64-lane-wide ‘wavefronts’ on the AMD GPUs. Any additional threads in excess of the threadblock size are simply masked out when executing on the hardware. Each warp/wavefront then has access to a number of vector registers. On the NVIDIA Tesla V100, a warp is able to reserve a maximum of 255 128B vector registers (each register being 32 lanes of 4B words) within a Stream Multiprocessor (SM) on the GPU. Similarly, on the AMD GPUs each wavefront is able to reserve a maximum of 256 256B vector registers (each register being 64 lanes of 4B words) in each Compute Unit (CU). While terminology between the GPU vendors differ, they share the property that warps/wavefronts reserving large amounts of register space can substantially affect the number of warps/waves which can be simultaneously active on an SM/CU. Each GPU’s SMs/CUs have vector register files that are divided evenly between four SIMD units, with both the NVIDIA Tesla V100 SMs and the AMD Instinct MI100 CUs having a total of 256KB of vector register space, and the AMD Instinct MI250X CUs having 512KB of vector register space. The ‘occupancy’ of a kernel then refers to the average number of warps/wavefronts which are active on each SM/CU during the kernel’s execution. Other constraints, such as the requirement that all warps/wavefronts from a given threadblock must occupy the same SM/CU can also restrict the occupancy of a kernel.

We list in Table 1 some metrics regarding the occupancy of the Poisson operator kernel on each of the GPUs considered above. For each threadblock size, we list the number of warps/wavefronts required to decompose the block. We then list the number of vector registers required by each warp/wavefront to execute the kernel, information we extract from the assembly generated by the compiler. Using these values, we list the occupancy of the operator kernel both in terms of warps/wavefronts active per SM/CU, and in terms of how many spectral elements each SM/CU processes while occupied.

Comparing the occupancy metrics of the operator kernel on the AMD Instinct MI100 on the NVIDIA Tesla V100 in Table 1 to the achieved performance in Figure 3b, we see that the drop in performance observed at \( N = 11 \) corresponds to a drop in occupancy on each CU. The occupancy drop itself is caused by the threadblock size of \( 144 \) requiring one additional wavefront at the same register usage compared to...
follows the same progression to the occupancy metrics in Table as on the AMD Instinct efficiency, though the occupancy increase at \( N = 11 \) may have additional impacts.

The differences in the assembly generated by the compiler two kernels makes them difficult to compare, however, since not. The different number of registers per warp between these degrees of higher occupancy per SM, especially at the moderately high warp compared with the AMD compiler, allowing for a much MI100, but the dips in performance are less pronounced and Tesla V100 in Figure CU occupancy doubling. This efficiency improvement is likely due to

## Table 1. Occupancy metrics for 2D threadblock algorithm for the Poisson operator kernel in hipBone. The number of warps/wavefronts must be sufficiently large to cover the threadblock size. Each warp/wavefront then uses some number of vector registers, which is the primary factor limiting SM/CU occupancy. The occupancy in terms of warps/SM or wavefronts/CU is listed for each kernel, along with the occupancy in terms of elements per SM/CU.

| \( N \) | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|
| Block size, \((N+1)^2\) | 100 | 121 | 144 | 169 | 196 | 225 | 256 |
| NVIDIA Tesla V100 | | | | | | | |
| Warps/Block | 4 | 4 | 5 | 6 | 7 | 8 | 8 |
| Registers/Warp | 80 | 80 | 104 | 90 | 82 | 102 | 100 |
| Occupancy (Warps/SM) | 24 | 24 | 15 | 18 | 14 | 16 | 16 |
| Elements/SM | 6 | 6 | 3 | 3 | 2 | 2 | 2 |
| AMD Instinct MI100 | | | | | | | |
| Warfronts/Block | 2 | 2 | 3 | 3 | 4 | 4 | 4 |
| Registers/Wavefront | 113 | 125 | 125 | 125 | 125 | 125 | 125 |
| Occupancy (Wavefronts/CU) | 8 | 8 | 6 | 6 | 8 | 8 | 8 |
| Elements/CU | 4 | 4 | 2 | 2 | 2 | 2 | 2 |
| AMD Instinct MI250X | | | | | | | |
| Warfronts/Block | 2 | 2 | 3 | 3 | 4 | 4 | 4 |
| Registers/Wavefront | 126 | 124 | 124 | 124 | 124 | 124 | 124 |
| Occupancy (Wavefronts/CU) | 16 | 16 | 12 | 12 | 16 | 16 | 16 |
| Elements/CU | 8 | 8 | 4 | 4 | 4 | 4 | 4 |

\( N = 10 \). This third wavefront will also unfortunately have 48 of its lanes masked while executing. The subsequent \( N = 12 \) kernel on the AMD Instinct MI100 achieves the same occupancy as \( N = 11 \), and the performance sees a increase which follows the trend of the roofline model, but shares the same inefficiencies as \( N = 11 \), albeit with less masked lanes. At \( N = 13 \) and onward, the kernel requires four wavefronts per threadblock and occupancy in terms of wavefronts/CU is recovered. The kernels, however, now do more computation with more wavefronts synchronizing their activity to coordinate accesses to shared memory. The performance continues to track upwards, but the inefficiency compared to the roofline model is never recovered.

The occupancy metrics of the operator kernel on the AMD Instinct MI250X in Table 1 follows the same progression as the AMD Instinct MI100, but overall occupancy is immediately doubled due to the 2x larger register file size per CU. We see a similar qualitative trend in the achieved performance of the operator kernel on the AMD Instinct MI250X in Figure 3c as on the AMD Instinct MI100, but the dips in performance are less pronounced and performance stays closer to the empirical roofline model for high degrees. This efficiency improvement is likely due to the CU occupancy doubling.

Finally, comparing the performance trend of the NVIDIA Tesla V100 in Figure 3a to the occupancy metrics in Table 1, the effects of different occupancies and registers per warp between kernels are more difficult to reason about. Overall, the NVIDIA compiler uses significantly fewer registers per warp compared with the AMD compiler, allowing for a much higher occupancy per SM, especially at the moderately high degrees of \( N = 9 \) and 10. The occupancy decrease at \( N = 11 \), however, appears to correspond to an increase in relative efficiency, though the occupancy increase at \( N = 12 \) does not. The different number of registers per warp between these two kernels makes them difficult to compare, however, since the differences in the assembly generated by the compiler may have additional impacts.

## Scaling

Overall performance of hipBone on a single GPU device is almost completely determined by the streaming efficiency of the accelerator and the performance of the Poisson operator kernel, with latency effects such as kernel launch latency and host-to-device synchronization latency being important factors for small problem sizes. The design focus in hipBone, however, is to scale efficiently to many GPU devices by leveraging GPU-Direct RDMA technologies in GPU-Aware MPI libraries, and aggressively hiding communication times behind local computation. To demonstrate the efficacy of this design we present in this section a series of performance tests of the full hipBone benchmark, rather than simply the Poisson kernel in isolation as presented above. We scale hipBone to several MPI ranks, each using a GPU accelerator, on the ORNL Summit, Spock, and Crusher clusters, sweeping over a variety of problem sizes on several GPUs/nodes.

We restrict our attention to the two polynomial degrees, \( N = 7 \) and \( N = 15 \), for the scaling tests in this section. The choice of degree \( N = 15 \) is of course of interest for hipBone as a benchmark, as this degree maximizes the GFLOPS of the operator kernel, and thus maximizes the overall FOM. For other polynomial degrees \( N \) there will be little qualitative difference in the scaling behavior of hipBone for sufficiently large global meshes. Once there is enough local work in the Poisson operator kernels to completely hide the MPI communication time, performance (as in the single GPU case) is bound only by the asymptotic streaming rate of the GPU devices, which is not appreciably affected by \( N \), and the streaming rate of the Poisson operator kernel which, as demonstrated in the tests above, is consistently near the roofline streaming rate for all \( N \). For smaller problems, however, there can be differences between the scaling behaviors of different degrees due to the variety of different latency effects. We therefore include degree \( N = 7 \) in our scaling tests, which uses the 3D threadblock algorithm.
Figure 4. Performance of full hipBone benchmark on the ORNL Summit cluster using NVIDIA Tesla V100 GPUs. Performance is measured over a variety of problem sizes, on 1 to 48 MPI ranks, each utilizing a single NVIDIA Tesla V100.

for the Poisson operator kernel, so that any qualitative difference in scaling behavior can be observed.

For each test, we sweep through several global mesh sizes, ranging from the very small \( \approx 2500 \) degrees of freedom per MPI rank, to the very large \( \approx 45M \) degrees of freedom per MPI rank. In this way, we collect performance data from both the extremely strong-scaled as well as weak-scaled regimes. On each cluster, we perform tests on an increasing number of GPUs, with small numbers of GPUs initially communicating entirely on-node using fast GPU-GPU data links, then over the network with GPU-Direct RDMA. Due to the different node architectures between the clusters, namely Summit nodes consisting of six GPU devices, Spock nodes consisting of four GPUs, and Crusher nodes consisting of four accelerators which appear to the OS as eight GPU devices, we scale the number of GPUs to eventually utilize a single full node, and continue scaling by using multiple full nodes. We label the configuration of each test as \( N_x y \) to indicate the execution was on \( x \) nodes of the cluster, using \( y \) total GPU devices.

We show the results of the scaling tests on the ORNL Summit, Spock, and Crusher clusters in Figures 4, 5, and 6, respectively. In each figure, we show the FOM of the hipBone application, given in GFLOPS, for \( N = 7 \) and \( 15 \) for each problem size. As noted above, for a better comparison with historical data we use the FLOP count (3) of the original NekBone benchmark to compute the FOM, rather than the slightly smaller true FLOP count of hipBone in (5).

It is difficult to immediately see how efficiently hipBone strong/weak scales from the plots of the FOM alone. One clear observation, however, is the significantly higher single rank performance of hipBone on small problem sizes. This can be attributed to some latency effects being completely
avoided for single rank execution, as no MPI communication is required at all. Indeed, recalling the timeline of the Poisson operator application in Figure 2, we see that in addition to avoiding MPI latency itself, when no communication is required the two instances of host-device synchronization after packing data buffers for MPI can be skipped. Avoiding these significant sources of latency leads to better single rank performance for latency-sensitive problem sizes.

To obtain a more useful visualization of the scaling behavior of hipBone, we also show in each figure plots of the performance in terms of a ‘throughput’ metric, similar to that used in Fischer et al. (2020), defined as

$$\text{Throughput} = \frac{\text{DOFs} \times \text{CG Iterations}}{\text{Number of Ranks} \times \text{Time}}.$$  \hspace{1cm} (6)

This throughput metric essentially normalizes the FOM measurements by computing a rate-of-work. As the benchmark is predominately streaming bandwidth limited, and the time taken to stream data scales linearly with amount of data moved, the work done by each CG iteration therefore scales linearly with the number of degrees of freedom, $N_G$. By multiplying the global problem size with the number of CG iterations done (which is a fixed 100 iterations), the numerator of (6) encodes a measure of the amount of work performed. The denominator of (6) then encodes an amount of computational resources by multiplying the number of process, each with a separate GPU, by the wall-clock time required to complete the CG iterations.

In each of the Figures 4, 5, and 6, we show the throughput metric of each scaling test plotted against a normalized DOFs-per-rank measure. Were all tests to weak scale perfectly in all regimes, the lines on these plots would collapse to a single curve, implying the same throughput per rank can be achieved even while increasing the number.
of compute resources (ranks), at every problem size. This is not what is typically seen in practice, as the smaller problem sizes typically under-saturate the compute resources and communication overheads lead to lower throughput as the problem is weak-scaled. At the very large problem sizes, however, we observe a clustering of throughputs near their peak values for all numbers of ranks. This regime demonstrates the ideal weak scaling regime in which the compute resources are saturated and MPI communication is effectively hidden.

Examining the scaling results for Summit and Spock in Figures 4 and 5, respectively, we see a fair amount of variability in throughputs in the latency-sensitive strongly-scaled regimes. This is somewhat expected, as we do no averaging of repeated runs on any of the clusters, and noise or jitter in communication latency, especially in multi-node tests, is normal. We see as well in the throughput plots a distinct separation of throughput curves for the multi-GPU runs which communicate entirely on-node with fast GPU-GPU links compared to the multi-node runs. Indeed, throughput on both clusters drops in the strongly-scaled regime once communication travels over the network, with the throughput on Summit remaining fairly stable as the node count is increased to eight, and the throughput on the Spock cluster appearing to take additional impacts as node count increases. Comparatively, the throughput data from the Crusher cluster in Figure 6 indicates excellent scalability of hipBone to multiple MI250X GPUs. The tight clustering of all the multi-GPU throughput curves indicates very little additional latency and communication overheads as the number of ranks is increased, even to multi-node.

In the weak scaled regime of each test, we see excellent weak scaling efficiency even compared to the single rank FOM on each GPU. We list the peak FOM of the degree $N =$...
We have presented hipBone**, an open source and freely available GPU port of the NekBone proxy application built on top of the libParanumal finite element library and using the OCCA portability layer. HipBone implements several optimizations over the original CPU NekBone proxy application. Storing degrees of freedom in assembled form reduces the amount of data moved in the streaming operations as part of the CG iteration, and avoids some data motion completely. Our GPU-aware gather-scatter library implements several nearest neighbor MPI communication algorithms and elides any explicit device-to-host data motion by leveraging GPU-Direct RDMA when possible and beneficial for performance. HipBone also aggressively hides MPI communication in several places to improve the overall scalability of the proxy application. Firstly, the communication overhead to perform the halo exchange overlaps with the Poisson operator application kernel on one half of the interior elements. Afterwards, the gather operation needed to convert the solution vector back to global DOF layout overlaps with the Poisson operator application on the other half of the interior elements. Finally, the MPI all-reduce required for the norm calculation of the residual vector is hidden by the update of the solution vector.

In general, the hipBone proxy application code is a high-performing GPU port of the original NekBone CPU proxy application. We have analyzed and demonstrated its performance on three systems at ORNL, each with different modern GPU accelerators. We have presented a portable Poisson operator application kernel with near-roofline performance over a range of spectral element orders. At low orders, performance is entirely bound by memory bandwidth. At higher orders, performance of the Poisson operator kernel deviates slightly from the empirical roofline on some GPUs. These deviations correlate with drops in occupancy as a result of increased register pressure.

In scaling tests, we observe excellent scalability of the hipBone benchmark, especially for large problems. Scaling efficiency is especially good on the Crusher cluster, which has additional network injection bandwidth with its four 200Gbps network cards per node. In the strong scaled regime performance becomes sensitive to latencies introduced by MPI communication overhead, GPU kernel launch, and host-device synchronization. In the weak scaled regime, we observe the multi-node weak scaling efficiency on Summit to be 94.9%, and more than 98% on Spock and Crusher, up to eight compute nodes.

Currently hipBone does not replicate all the capabilities of the original NekBone benchmark. Most notably we have refrained from implementing any sort of preconditioner on the GPU, and left this topic for future study. Many optimizations we have described here, however, are easily forwarded into the libParanumal library and, by extension, NekRS. The Poisson operator kernel, gather-scatter communication library, and operator splitting algorithm can be ‘dropped in’ to these projects with minimal effort. HipBone thus serves as an excellent proxy application for a crucial computational portion of these larger projects.

**https://github.com/paranumal/hipbone

---

### Conclusion

15 tests in Table 2 wherein we see that when weak-scaled we observe 943.6 GFLOPS or higher on each NVIDIA Tesla V100, 1062.8 GFLOPS or higher on each AMD Instinct MI100, and 1287.1 GFLOPS or higher on each GCD of AMD Instinct MI250X. Comparing to other GPU performance values for NekBone in the literature, Karp et al. (2020) used a version of NekBone with a native CUDA Poisson operator kernel to report $\approx 410$ GFLOPS on a single NVIDIA Tesla V100 at degree $N = 9$. Figure 4a shows our hipBone benchmark exceeding this FLOP rate at the lower polynomial degree $N = 7$, achieving 657.6 GFLOPS a single NVIDIA Tesla V100 despite the lower arithmetic intensity. Performance on an NVIDIA Tesla K20X was also reported by Gong et al. (2016) using an OpenACC version of NekBone with a CUDA Fortran Poisson operator kernel to achieve 78.2 GFLOPS at degree $N = 15$, while hipBone achieves a FLOP rate over 13 times higher the same degree on a single NVIDIA Tesla V100, despite an only 3.6x increase in peak memory bandwidth of the GPU. Gong et al. (2016) also reported significant communication overhead which effected weak scaling. Using Table 2, we see that the NVIDIA Tesla V100 has weak scaling efficiency from 1 to 48 GPUs of 89.7%, while the AMD Instinct MI100 observes a 94.5% weak scaling efficiency from 1 to 32 GPUs, and the AMD Instinct MI250X achieves 92.9% efficiency scaling from 1 to 64 GCDs. Considering just the scaling efficiency from two to eight nodes on each cluster, the NVIDIA Tesla V100 achieves a 94.9% scaling efficiency, while both AMD GPUs observe greater than 98% efficiency. This indicates that when sufficiently weak scaled, our optimizations in hipBone are very effective at hiding MPI communication overheads.

##### Table 2. Summary of peak FOM in GFLOPS recorded on several multi-GPU runs of hipBone on ORNL Summit, Spock, and Crusher clusters.

| Ranks | Peak FOM (GFLOPS) | FOM per Rank (GFLOPS) |
|-------|------------------|-----------------------|
| 1     | 1051.5           | 1051.5                |
| 3     | 3086.1           | 1028.7                |
| 6     | 6129.7           | 1021.6                |
| 12    | 11935.5          | 994.6                 |
| 24    | 23611.4          | 983.8                 |
| 48    | 45294.6          | 943.6                 |
| 1     | 1124.8           | 1124.8                |
| 2     | 2172.5           | 1086.3                |
| 4     | 4333.0           | 1083.3                |
| 8     | 8690.5           | 1076.2                |
| 16    | 17065.0          | 1066.6                |
| 32    | 34011.7          | 1062.9                |
| 1     | 1386.1           | 1386.1                |
| 2     | 2669.6           | 1334.8                |
| 4     | 5316.9           | 1329.2                |
| 8     | 10548.8          | 1318.6                |
| 16    | 20968.0          | 1310.5                |
| 32    | 41779.4          | 1305.6                |
| 64    | 82375.7          | 1287.1                |

12

Currently hipBone does not replicate all the capabilities of the original NekBone benchmark. Most notably we have refrained from implementing any sort of preconditioner on the GPU, and left this topic for future study. Many optimizations we have described here, however, are easily forwarded into the libParanumal library and, by extension, NekRS. The Poisson operator kernel, gather-scatter communication library, and operator splitting algorithm can be ‘dropped in’ to these projects with minimal effort. HipBone thus serves as an excellent proxy application for a crucial computational portion of these larger projects.
An additional future research topic is the investigation of the performance of hipBone on other vendors’ hardware and/or other programming models, such as SYCL, but we note that hipBone is well-positioned to leverage such technology via the OCCA portability framework.

Acknowledgments

This research was supported in part by the Exascale Computing Project, a collaborative effort of two U.S. Department of Energy organizations (Office of Science and the National Nuclear Security Administration) responsible for the planning and preparation of a capable exascale ecosystem, including software, applications, hardware, advanced system engineering, and early tested platforms, in support of the nation’s exascale computing imperative.

This research was also supported in part by the John K. Costain Faculty Chair in Science at Virginia Tech. Computing facilities were furnished in part by the Advanced Research Computing group at Virginia Tech.

This research used resources of the Oak Ridge Leadership Computing Facility at the Oak Ridge National Laboratory, which is supported by the Office of Science of the U.S. Department of Energy under Contract No. DE-AC05-00OR22725.

AMD, the AMD Arrow logo, Instinct, EPYC, and combinations thereof are trademarks of Advanced Micro Devices, Inc. OpenCL is a trademark of Apple Inc. used by permission by Khronos Group, Inc. SYCL is a registered trademark of the Khronos Group, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

References

Anderson R, Andrej J, Barker A, Bramwell J, Camier JS, Cerveny J, Dobrev V, Dudouit Y, Fisher A, Kolev T et al. (2021) MFEM: A modular finite element methods library.

Computers & Mathematics with Applications 81: 42–74.

Beams N, Abdelfattah A, Tomov S, Dongarra J, Kolev T and Dudouit Y (2020) High-order finite element method using standard and device-level batch GEMM on GPUs. In: 2020 IEEE/ACM 11th Workshop on Latest Advances in Scalable Algorithms for Large-Scale Systems (ScalA). IEEE, pp. 53–60.

Brown N (2020) Exploring the acceleration of Nekbone on reconfigurable architectures. In: 2020 IEEE/ACM International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC). IEEE, pp. 19–28.

Canuto C, Hussaini MY, Quarteroni A, Thomas Jr A et al. (2012) Spectral methods in fluid dynamics. Springer Science & Business Media.

Cebamanos L, Henty D, Richardson H and Hart A (2014) Auto-tuning an OpenACC accelerated version of Nek5000. In: International conference on exascale applications and software. Springer, pp. 69–81.

Chalmers N, Karakus A, Austin AP, Swirydowicz K and Warburton T (2020) libParanual: a performance portable high-order finite element library. DOI:10.5281/zenodo.4004744. URL https://github.com/paranual/libparanual. Release 0.4.0.

Chalmers N and Warburton T (2020) Portable high-order finite element kernels I: Streaming operations. arXiv preprint arXiv:2009.10917.

Deville MO, Fischer PF and Mund EH (2002) High-order methods for incompressible fluid flow, volume 9. Cambridge university press.

Dong T, Dobrev V, Kolev T, Rieber R, Tomov S and Dongarra J (2014) A step towards energy efficient computing: Redesigning a hydrodynamic application on CPU-GPU. In: 2014 IEEE 28th International Parallel and Distributed Processing Symposium. IEEE, pp. 972–981.

Fischer P, Kerkemeier S, Min M, Lan YH, Phillips M, Rathnayake T, Merzari E, Tomboulides A, Karakus A, Chalmers N and Warburton T (2021) NekRS, a GPU-accelerated spectral element Navier-Stokes solver. arXiv preprint arXiv:2104.05829.

Fischer P, Lottes J and Kerkemeier S (2008a) Nek5000 Web page. URL http://nek5000.mcs.anl.gov.

Fischer P, Lottes J, Pointer D and Siegel A (2008b) Petascale algorithms for reactor hydrodynamics. In: Journal of Physics: Conference Series, volume 125, no. 1. IOP Publishing, p. 012076.

Fischer P, Min M, Rathnayake T, Dutta S, Kolev T, Dobrev V, Camier JS, Kronbichler M, Warburton T, Štyrydowicz K et al. (2020) Scalability of high-performance PDE solvers. The International Journal of High Performance Computing Applications 34(5): 562–586.

Göddeke D, Strzodka R, Mohd-Yusof J, McCormick P, Buijssen SH, Grajewski M and Turek S (2007a) Exploring weak scalability for FEM calculations on a GPU-enhanced cluster. Parallel Computing 33(10-11): 685–699.

Göddeke D, Strzodka R and Turek S (2007b) Performance and accuracy of hardware-oriented native-, emulated-and mixed-precision solvers in FEM simulations. International Journal of Parallel, Emergent and Distributed Systems 22(4): 221–256.

Gong J, Markidis S, Laure E, Otten M, Fischer P and Min M (2016) Nekbone performance on GPUs with OpenACC and CUDA Fortran implementations. The Journal of Supercomputing 72(11): 4160–4180.

Gong J, Markidis S, Schliepke M, Laure E, Henningson D, Schlatter P, Peplinski A, Hart A, Doleschal J, Henty D et al. (2014) Nek5000 with OpenACC. In: International Conference on Exascale Applications and Software. Springer, pp. 57–68.

Henderson RD and Kamiadakis GE (1995) Unstructured spectral element methods for simulation of turbulent flows. Journal of Computational Physics 122(2): 191–217.

Hockney RW (1982) Characterization of parallel computers and algorithms. Computer Physics Communications 26(3-4): 285–291.

Hockney RW (1985) (rroc, n12, s12) measurements on the 2-CPU CRAY X-MP. Parallel Computing 2(1): 1–14.

Ivanov I, Gong J, Akhmetova D, Peng IB, Markidis S, Laure E, Machado R, Rahn M, Bartsch V, Hart A et al. (2015) Evaluation of parallel communication models in NekBone, a Nek5000 mini-application. In: 2015 IEEE International Conference on Cluster Computing. IEEE, pp. 760–767.

Karp M, Jansson N, Podobas A, Schlatter P and Markidis S (2020) Optimization of tensor-product operations in NekBone on GPUs. arXiv preprint arXiv:2005.13425.
Klöckner A, Warburton T, Bridge J and Hesthaven JS (2009) Nodal discontinuous Galerkin methods on graphics processors. *Journal of Computational Physics* 228(21): 7863–7882.

Komatitsch D, Michéa D and Erlebacher G (2009) Porting a high-order finite-element earthquake modeling application to NVIDIA graphics cards using CUDA. *Journal of Parallel and Distributed Computing* 69(5): 451–460.

Kronbichler M, Allalen M, Ohlerich M and Wall WA (2018) Which architecture is better suited for matrix-free finite-element algorithms: Intel Skylake or NVIDIA Volta? *Supercomputing*.

Kronbichler M, Ljungkvist K, Allalen M, Ohlerich M, Pasichnyk I and Wall WA (2017) Performance optimization of matrix-free finite-element algorithms within deal.II. *Supercomputing*.

Lamb DA, Fox GC, Johnson MH, Lyzenga G and Otto S (1988) *Solving Problems on Concurrent Processors: General techniques and regular problems*, volume 1. Prentice Hall.

Lottes JW and Fischer PF (2005) Hybrid multigrid/Schwarz algorithms for the spectral element method. *Journal of Scientific Computing* 24(1): 45–78.

Markidis S, Gong J, Schliephake M, Laure E, Hart A, Henty D, Heisey K and Fischer P (2015) OpenACC acceleration of the Nek5000 spectral element code. *The International Journal of High Performance Computing Applications* 29(3): 311–319.

Medina DS, St-Cyr A and Warburton T (2014) OCCA: A unified approach to multi-threading languages.

NekBone (2018) NekBone: Proxy app for Nek5000. URL https://github.com/Nek5000/Nekbone.

Otero E, Gong J, Min M, Fischer P, Schlatter P and Laure E (2019) OpenACC acceleration for the PN–PN-2 algorithm in Nek5000. *Journal of Parallel and Distributed Computing* 132: 69–78.

Patera AT (1984) A spectral element method for fluid dynamics: laminar flow in a channel expansion. *Journal of Computational Physics* 54(3): 468–488.

Remacle JF, Gandham R and Warburton T (2016) GPU accelerated spectral finite elements on all-hex meshes. *Journal of Computational Physics* 324: 246–257.

Schliephake M and Laure E (2014) Performance analysis of irregular collective communication with the crystal router algorithm. In: *International Conference on Exascale Applications and Software*. Springer, pp. 130–140.

Stilwell N (2013) gNek: A GPU accelerated incompressible Navier Stokes solver. Rice University.

Świrydowicz K, Chalmers N, Karakus A and Warburton T (2019) Acceleration of tensor-product operations for high-order finite element methods. *The International Journal of High Performance Computing Applications* 33(4): 735–757.

Tufo HM (1998) Algorithms for large-scale parallel simulation of unsteady incompressible flows in three-dimensional complex geometries. Brown University.

Tufo HM and Fischer PF (1999) Terascale spectral element algorithms and implementations. In: *Proceedings of the 1999 ACM/IEEE Conference on Supercomputing*. pp. 68–es.

Vincent J, Gong J, Karp M, Pepinski A, Jansson N, Podobas A, Jocksch A, Yao J, Hussain F, Markidis S et al. (2021) Strong scaling of OpenACC enabled Nek5000 on several GPU based HPC systems. *arXiv preprint arXiv:2109.03592*.