eSampling: Energy Harvesting ADCs

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Abstract

Analog-to-digital converters (ADCs) allow physical signals to be processed using digital hardware. The power consumed in conversion grows with the sampling rate and quantization resolution, imposing a major challenge in power-limited systems. A common ADC architecture is based on sample-and-hold (S/H) circuits, where the analog signal is being tracked only for a fraction of the sampling period. In this paper, we propose the concept of eSampling ADCs, which extend the structure of S/H ADCs without altering its conversion procedure, while harvesting energy from the analog signal during the time periods where the signal is not being tracked. This harvested energy can be used to supplement the ADC itself, paving the way to the possibility of zero-power consumption and power-saving ADCs. The amount of energy harvested can be increased by reducing the sampling rate. We analyze the tradeoff between the ability to recover the sampled signal and the energy harvested, and provide guidelines for setting the sampling rate in the light of accuracy and energy constraints. Our analysis indicates that eSampling ADCs operating with up to 12 bits per sample can acquire bandlimited analog signals such that they can be perfectly recovered (up to the distortion induced in quantization) without requiring power from the external source. Furthermore, our theoretical results reveal that eSampling ADCs can in fact save power by harvesting more energy than they consume. Furthermore, we show how these results imply that an eSampling ADC acquiring a bandlimited signal at Nyquist rate with 8 bit ADCs can harvest over 15 dB more energy than it consumes in the conversion procedure. To verify the feasibility of eSampling ADCs, we present a circuit-level design using standard complementary metal oxide semiconductor (CMOS) 65 nm technology. An eSampling 8-bit ADC which samples at 40 MHz is designed on a Cadence Virtuoso

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platform. Our experimental study involving Nyquist rate sampling of bandlimited signals demonstrates that such ADCs are indeed capable of harvesting more energy than that spent during analog-to-digital conversion, without affecting the accuracy.

Index Terms

Energy harvesting, analog-to-digital conversion, sample-and-hold circuits.

I. INTRODUCTION

Physical signals are analog in nature, taking values in continuous sets over a continuous time interval. In order to process and extract information from such signals using digital hardware, they must be accurately represented in digital form. Analog-to-digital converters (ADCs) thus play an important role in digital signal processing systems [2]. ADCs are typically a major source of energy consumption, as their power dissipation grows with the sampling rate and the quantization resolution, and thus their ability to accurately represent the acquired signal is typically limited by the available power [3]. Nowadays, ADCs are utilized in a multitude of energy-limited systems, including communication devices [4], wireless sensors [5], and medically implanted devices [6]. Therefore, there is a growing need for ADCs capable of reliably acquiring signals while consuming low power.

The existing strategies proposed in the literature to facilitate energy efficient acquisition of analog signal can be divided into those taking a signal processing approach, and techniques focusing on circuit level design. Signal processing approaches typically aim for allowing the ADC to operate at reduced sampling rate and quantization resolution by accounting for how the acquired signal is processed and prior information on the signal itself [5], [7]–[10]. Additionally, in scenarios where the signal is acquired for some task, i.e., to recover some underlying information, it was recently shown that the desired information could be accurately recovered from the output of low-resolution ADCs by properly designing the acquisition system [11]–[14]. An alternative signal processing oriented method which does not limit the rate and resolution of ADC is based on acquiring a portion of the analog signal to be processed while utilizing the remaining part for energy harvesting. This strategy, typically studied in the context of communication receivers as simultaneous wireless information and power transfer (SWIPT), considers time or power splitting of the analog signal [15]–[18]. However, it induces some inevitable loss on the system performance as only a portion of the signal is converted into a digital representation. These aforementioned signal processing methods typically focus on the signal model and the task for which it is acquired, without accounting for the ADC circuitry.
Circuit level methods rely on the hardware architecture of ADC devices. The circuit level approach generally considers designing energy efficient ADC circuitry, which is capable of operating with reduced power consumption. This can be achieved by reducing the circuit power supply [6] and/or limiting the operating frequency [19] in order to reduce the overall power consumption. An alternative technique is to modify the circuit components in existing ADC architectures and combine various designs in the acquisition, such as sample-and-hold (S/H) ADCs, flash ADCs, sigma-delta ADCs, and time-interleaved ADCs, to improve their energy efficiency, see, e.g., [20]–[23]. Such circuit-oriented designs which focus on the hardware aspects of acquisition, do not account for the model of the analog signal and the task for which it is acquired.

A popular power efficient ADC is the S/H based successive approximation register (SAR) architecture, which is capable of operating at high resolution and a small form factor with relatively low power consumption [24]. The power consumption of SAR ADCs can be further reduced by incorporating energy efficient switching schemes, as proposed in [25], [26]. In S/H architectures, the circuit used to sample the input analog signal consists of two phases, acquisition phase and hold phase in each sampling period. In the acquisition phase, the S/H circuit tracks the input analog signal. The sampled value captured in the acquisition phase is then converted into digital form, i.e., a sequence of bits, during hold phase. Therefore, during the sampling process of S/H ADCs, the input signal is processed only for a fraction of the overall sampling period (acquisition phase) and is neglected/discharded for the remaining time interval (hold phase) [27], [28]. The fact that the signal is not accessed in a dominant portion of the sampling period, motivates the extension of S/H ADCs, and particularly S/H SAR ADCs, to continuously utilize the analog signal in order to mitigate power consumption.

In this work, we combine signal processing tools with circuit level methods to propose an $e$Sampling ADC, which harvests energy from the acquired signal while converting it into a digital representation. The $e$Sampling ADC builds upon the S/H ADC architecture while introducing an additional energy harvesting circuit. In the resulting architecture, the signal is harvested during hold phase, i.e., when it is not utilized in conventional S/H ADCs. This operation allows $e$Sampling ADCs to harvest energy from the sampled signal without altering the conversion procedure. Our analysis of $e$Sampling ADCs formulates the theoretical foundations for joint acquisition and energy harvesting, and generalizes the experimental results of our previous work [29], which demonstrated that energy harvesting can be combined with sensing circuits. As opposed to SWIPT systems, in which the overall operation of the system is modified to allow energy harvesting while conventional ideal ADCs are assumed [18], $e$Sampling exploits an inherent property of ADC devices to harvest energy as a natural byproduct of their hardware architecture. This makes $e$Sampling an attractive technology which can be easily incorporated into existing devices.
Our theoretical study of eSampling ADCs analyzes its potential in terms of the ability to harvest energy while maintaining a desired accuracy of signal reconstruction. To that aim, we focus on the acquisition of stationary random processes and characterize the resulting tradeoff between the ability to accurately reconstruct the signal from its samples and the energy harvested from it, referred to henceforth as the energy-fidelity tradeoff. Our analysis identifies how to set the sampling rate to optimize this tradeoff when operating under energy constraints or fidelity restrictions on the reconstruction. The results allow us to numerically characterize the maximal accuracy in which any signal can be eSampled using only harvested energy, i.e., without requiring any energy from its power source. The energy consumed in acquisition is determined by the specific components comprising the ADC circuit. We show that eSampling ADCs operating with a typical set of ADC parameters are capable of fully reconstructing signals of various power spectral density (PSD) profiles with negligible distortion, while harvesting at least as much energy as they consume. In particular, we show that an eSampling ADC with 12 bits quantization can acquire a bandlimited signal at the Nyquist rate while harvesting more energy than it consumes.

We then proceed to illustrate the hardware feasibility of such a device. To that aim, we design the circuitry of an eSampling 8-bit SAR ADC which samples at 40 MHz on 65 nm complementary metal oxide semiconductor (CMOS) technology, and provide guidelines for setting its parameters to achieve a desired amount of harvested energy. The experimental evaluation of the eSampling SAR ADC circuit, carried out on the Cadence Virtuoso platform, shows that the amount of energy harvested can be much larger than the amount of energy consumed during the conversion procedure. This is achieved without affecting the signal reconstruction accuracy when acquiring a bandlimited signal while satisfying Nyquist condition. Our experiment indicates that the theoretical potential of eSampling can be translated into an actual ADC circuit, which accurately acquires analog signals while harvesting more power than it consumes.

The rest of this paper is organized as follows: In Section II, we present our eSampling system model. Section III analyzes the associated energy-fidelity tradeoff. The circuit-level design and its experimental study are presented in Section IV. Finally, Section V provides concluding remarks.

II. SYSTEM MODEL

In this section, we detail the proposed ADC model from a high-level perspective. We begin by briefly reviewing S/H-based SAR ADCs and their associated energy consumption in Subsection II-A. Then, we present how S/H ADCs can be extended into eSampling ADCs which harvest energy in addition to signal acquisition in Subsection II-B.
Figure 1. S/H SAR ADC illustration: (a) acquisition phase (b) hold phase.

A. Sample-and-Hold ADC Model

1) High-level description: S/H is a common ADC architecture. Such ADCs acquire each sample in two phases, determined by a switch $S$, as illustrated in Fig. 1: In the acquisition phase, the signal is connected to a capacitor $C_h$, referred to as a holding capacitor, which is charged to the input analog voltage, as depicted in Fig. 1(a). The time required by the holding capacitor to charge to the input voltage, which dictates the acquisition time, is given by [24]

$$T_{aq} = \alpha \tau R_{on} C_h,$$

(1)

where $R_{on}$ is the on-resistance of the switch $S$, and $\alpha \tau$ is the number of time constants, i.e., $R_{on} C_h$ required for the capacitor to be fully charged.

Once the acquisition phase is over, the hold phase begins, in which the discrete sample, i.e., the voltage stored in the holding capacitor, is quantized into digital bits. During hold phase, whose duration is denoted by $T_h$, the input signal is disconnected from the S/H circuit and $C_h$ holds the acquired voltage to accomplish the successful conversion of the acquired sample into digital bits as illustrated in Fig. 1(b). Both $T_h$ and $C_h$, must be set to allow the quantization circuit of the ADC to complete the conversion.

When the quantizer is based on SAR logic, the overall architecture is referred to as a SAR ADC. An $n$-bit SAR ADC consists of a comparator, digital-to-analog converter (DAC), and a SAR logical circuit which successively refines the digital representation. To allow successful quantization into $n$ bits, the hold time required to quantize each sample must satisfy [28]

$$T_h \geq n \alpha \tau R_q C_h,$$

(2)

where $R_q$ is the equivalent resistance of the quantizer binary scale switches. Therefore, the sampling period, i.e., the duration of acquiring a single sample, is lower bounded by the following expression

$$T_s = T_{aq} + T_h \geq (R_{on} + n R_q) \alpha \tau C_h.$$

(3)
In S/H SAR ADCs, the on-resistance of the switch $R_{\text{on}}$ is commonly not larger than the resistance of the quantizer binary scale switches $R_q$. Thus from (1) and (2), it is evident that $T_h$ is typically much larger than $T_{\text{aq}}$, particularly when using high resolution quantizers, such as ADCs with $n \geq 8$ bits. Consequently, the input signal, which is tracked only during the acquisition phase, is discarded during most of the sampling period.

2) Energy consumption: In general, the energy consumption of a circuit is typically a function of the time duration it is active, and the amount of power drawn from the supply, denoted here by $V_{\text{ref}}$. As $T_h$ is typically much larger than $T_{\text{aq}}$, most of the energy required by S/H SAR ADCs is consumed during hold phase [25], [28].

In particular, the only energy consumed during acquisition phase, denoted $E_{\text{aq}}$, is that needed to toggle the sampling switch $S$. In contrast, the energy consumption during hold phase, denoted $E_{\text{hold}}$, is comprised of the energy used by each of the components taking part in the quantization:

$$E_{\text{hold}} = E_{\text{DAC}} + E_c + E_{\text{sl}},$$

(4)

where $E_{\text{DAC}}$, $E_c$, and $E_{\text{sl}}$ are the energy consumption of the DAC array, comparator, and SAR logic, respectively. Consequently, $E_{\text{hold}}$ effectively represents the power consumed per sample by S/H SAR ADCs [25], [28]. We elaborate on the quantities in (4), which are dictated by the specific circuit parameters used, in Section IV where a concrete circuit-level design is discussed. Here, we note that $E_{\text{hold}}$ typically takes the form of a second-order polynomial in the reference voltage $V_{\text{ref}}$ [30], i.e.,

$$E_{\text{hold}} = a_1(n)V_{\text{ref}} + a_2(n)V_{\text{ref}}^2.$$  

(5)

The coefficients $a_1(n)$ and $a_2(n)$ in (5) are positive constants determined by the number of bits $n$ and the quantization circuit parameters, and can grow dramatically with $n$. This makes energy consumption a major bottleneck of high resolution ADCs, motivating the proposed eSampling architecture detailed next.

B. eSampling ADC Architecture

As mentioned above, during hold phase, the capacitor $C_h$ holds the acquired voltage sample, which is converted into a set of digital bits. In this interval, the input signal is disconnected from the circuit by the switch $S$. In order to mitigate the energy consumption of S/H SAR ADCs without modifying their sampling and quantization procedure, we propose to harvest the input signal energy by connecting it to an energy harvesting circuit during the hold phase, as illustrated in Fig. 2. Henceforth, the proposed architecture is referred to eSampling ADC.

As depicted in Fig. 2, the energy harvesting capability is enabled by passing the signal observed during hold time through a conditioning circuit, whose output is used to charge an energy harvesting capacitor
$C_{EH}$ to a voltage level $V_{EH}$. The energy harvesting circuit can be designed using passive elements, as we do in our proposed design detailed in Section IV. Hence, no external power supply is required [31]. The purpose of the signal conditioning circuit used in energy harvesting devices is to facilitate the storage of the energy of the signal in the capacitor $C_{EH}$ [32]–[34]. For instance, a rectifier can act as a signal conditioning circuit, reducing fluctuations in the amount of energy harvested in the presence of alternating signals. Similarly, voltage regulator circuits and DC-DC step up converters can also be used to enhance the overall efficiency of the energy harvesting system [35]. The common measure for the quality of an energy harvesting circuit is the efficiency parameter, denoted by $\eta \in [0, 1]$, which represents the fraction of the energy of the input signal that is harvested. Finally, in order to connect the input signal to the quantization circuit during acquisition time and to the energy harvesting circuit during hold time, the sampling switch $S$ is replaced by a two-way switch $\tilde{S}$. A possible circuit design such a two-way switch is detailed in Section IV.

The amount of energy consumed in acquisition phase given in (5) is dictated by the design parameters of the circuitry, which also affect the sampling rate via (3). In particular, the sampling duration is the sum of the acquisition time $T_{aq}$ and the hold time $T_h$. Further, the amount of time during which energy is harvested from the input signal per sampling period is at most $T_h$. Recalling that typically $T_h \gg T_{aq}$, a significant portion of the sampling interval can be allocated for harvesting energy from the input signal. Since energy is only harvested during hold time, in which conventional S/H ADCs do not utilize the analog signal, the ability to harvest energy in eSampling ADCs does not affect the acquisition operation. Specifically, for a given sampling rate, eSampling ADCs implement the same conversion mapping as standard S/H ADCs operating at the same rate. Nonetheless, eSampling provides the ability to trade acquisition accuracy for harvesting more energy. This is due to the fact that increasing the sampling interval allows eSampling ADCs to dedicate more time to energy harvesting, possibly at the cost of degrading the accuracy in reconstructing the analog signal from its digital representation.

The goal of our analysis of eSampling ADCs presented in the following section is to quantify the theoretical potential benefits of such an architecture, which is capable of simultaneously acquiring analog signals into a digital form while harvesting their energy. Both the amount of energy consumed in conversion and that harvested in eSampling are determined by the specific circuitry, encapsulated in (5) and the energy efficiency parameter $\eta$, respectively. Therefore, in our analysis we fix the circuit parameters, e.g., $a_1(n)$, $a_2(n)$, $\eta$, etc., and express how the accuracy in reconstruction and the amount of energy harvested vary as the sampling interval changes. We are particularly interested in characterizing the amount of energy harvested in the regime in which the distortion induced by S/H conversion is negligible, e.g., Nyquist rate sampling of bandlimited signals, and understanding when is it possible for
eSampling ADCs to operate at this regime while harvesting at least as much energy as they consume. Our theoretical analysis detailed in the sequel reveals that such a regime of operation is indeed feasible with typical ADC circuit parameters when acquiring bandlimited signals while using up to 12 bits per sample.

III. eSampling ADC Analysis

In this section, we analyze the capabilities of the proposed eSampling ADC in terms of the amount of energy one can harvest while meeting a given level of reconstruction accuracy, as well as the achievable accuracy for harvesting a desired amount of energy. The interplay between these key performance measures is determined by the selection of the sampling rate, as we show in the following. We begin by formulating the signal model under which our analysis is carried out, and the corresponding problem of characterizing the associated energy-fidelity tradeoff, which arises from the eSampling ADC paradigm in Subsection III-A. Then, we derive the achieved normalized mean-squared error (NMSE) under the considered model in Subsection III-B. The derived NMSE is used to characterize the energy-fidelity tradeoff in Subsection III-C, and to obtain as a special case the maximal amount of energy which can be harvested when sampling a bandlimited signal at a rate satisfying the Nyquist condition, i.e., allowing perfect recovery. We demonstrate a few examples of energy-fidelity tradeoff curves for signals with different spectral profiles in Subsection III-D. Finally, we discuss the pros and cons of eSampling ADC in light of our analysis in Subsection III-E.

A. Problem Formulation

The eSampling ADC detailed in Subsection II-B harvests energy during hold phase. This implies that more energy can be harvested by increasing the hold time, which in turn increases the sampling period, potentially degrading the ability to reconstruct the signal from its samples. Therefore, to unveil the potential of eSampling ADCs, we first wish to analyze the fundamental tradeoff between the amount of energy harvested in eSampling and the resulting fidelity in signal reconstruction. We are particularly interested in: 1) Quantifying the maximum amount of energy that could be harvested when acquiring bandlimited signals at the Nyquist rate, i.e., without compromising the signal reconstruction accuracy; and 2) Characterizing the achievable NMSE when the ADC harvests at least as much power as it consumes.

In the analysis carried out in this section we consider a stochastic input signal $x(t)$ modeled as a zero-mean wide sense stationary (WSS) process, with variance $\sigma_x^2$, and PSD $S_x(f)$. The signal $x(t)$ is sampled uniformly with sampling interval $T_s$, resulting in the discrete-time signal $x(kT_s), k \in \mathbb{Z}$, where $\mathbb{Z}$ is the set of integers. The sampled series is quantized with $n$ bits per sample into the digital sequence $\tilde{x}(kT_s)$. 
The digital representation is utilized to recover the analog signal $x(t)$ using a linear reconstruction filter $G(t)$, which is designed to minimize the NMSE between $x(t)$ and the recovered signal $\hat{x}(t)$ as in [10], [36]. The reconstructed signal is

$$\hat{x}(t) = \sum_{k \in \mathbb{Z}} G(t - kT_s)\bar{x}(kT_s).$$

(6)

The overall system is illustrated in Fig. 3.

The NMSE in reconstructing $x(t)$ from $\hat{x}(t)$ is given by

$$\zeta = \frac{1}{\sigma_x^2 T_s} \int_0^{T_s} E\{|x(t) - \hat{x}(t)|^2\} \, dt,$$

(7)

where $E\{\cdot\}$ is the stochastic expectation. The amount of expected energy harvested per sampling period is given by

$$E_h = \eta \frac{1}{R_h} \int_0^{T_h} E\{|x(t)|^2\} \, dt = \eta \frac{T_h}{R_h} \sigma_x^2,$$

(8)

where $\eta$ and $R_h$ is the efficiency and the resistance of the energy harvesting circuit, respectively. As mentioned above, the energy harvesting circuit is comprised of passive elements, and does not require an external power source. Therefore, the overall energy consumption per sample using the proposed $e$Sampling ADC can be given as $E_{aq} + E_{hold} - E_h$ as illustrated in Fig. 3. Recall that the overall energy consumption is typically dominated by the energy used during hold phase, i.e., $E_{aq} \ll E_{hold}$, and hence the ratio of the amount of energy harvested to the energy consumption per sample can be approximated as $E_{ratio} = \frac{E_h}{E_{hold}}$. The value of $E_{hold}$ is dictated by the power supply voltage $V_{ref}$ and the number of quantization bits $n$, as well as the SAR architecture and circuit parameters, as we show for our design detailed in Section IV.

In the following subsections, we study the fundamental tradeoff between the reconstruction accuracy, modelled as the NMSE, and the portion of the energy consumed in analog-to-digital conversion to that
harvested by eSampling, referred to as the energy-fidelity tradeoff. To trade energy efficiency for fidelity, we modify the sampling rate for a fixed quantization resolution $n$ and fixed acquisition time $T_{\text{act}}$. The reconstruction accuracy can be improved by increasing the sampling rate, however eSampling ADC will harvest less energy, and hence the inherent tradeoff between these parameters. In particular, we focus on ADCs operating with relatively high resolution, where energy consumption constitutes a major challenge. The following analysis sheds light on the potential of joint acquisition and energy harvesting. For example, it quantifies the minimal recovery NMSE which allows a fixed $n$-bit ADC to operate at zero power, i.e., $E_{\text{ratio}} = 0$ dB. Alternatively, it allows identifying the quantization resolution $n$ for which the eSampling ADC can sample a bandlimited signal at Nyquist condition and operate at zero power. For instance, we use our results to show that bandlimited signals can be eSampled at Nyquist rate with up to 12 bits per sample while harvesting more energy than that consumed. Finally, the characterization of the energy-fidelity tradeoff allows computing the maximal amount of energy which can be harvested for an allowed level of reconstruction accuracy for both bandlimited and non-bandlimited signals, as a function of the ADC circuitry parameters.

### B. Reconstruction NMSE

In general, the NMSE depends on both the sampling rate as well as the quantization resolution [37]. Since we focus on relatively high rate quantization, the NMSE due to quantization is well-approximated by the 6 dB rule-of-thumb [38, Ch. 23], and is thus on the order of $10^{-0.6n}$ [24], resulting in a negligible contribution to the overall NMSE of less than roughly $10^{-5}$ for $n \geq 8$. Therefore, henceforth the focus is on the the NMSE between $x(t)$ and $\hat{x}(t)$ due to the sampling procedure alone, expressed in the following theorem, derived in [36]:

**Theorem 1:** The minimal achievable NMSE in reconstructing a uniformly sampled WSS signal $x(t)$ with sampling frequency $f_s = 1/T_s$ using a linear reconstruction filter, $G(t)$ is

$$\zeta(T_s) = 1 - \frac{1}{\sigma_x^2} \sum_{k \in \mathbb{Z}} \int_{-T_s/2}^{T_s/2} \frac{|S_x(f - kf_s)|^2}{\sum_{k' \in \mathbb{Z}} S_x(f - k'f_s)} df.$$  

(9)
To achieve (9), the linear recovery filter $G(t)$ in (6) is set according to [10], [36], i.e., its frequency response $F(G)(f)$ should be set to $F(G)(f) = \sum_{k \in \mathbb{Z}} S_x(f - kf_s)$, where $F(\cdot)$ denotes the Fourier transform. This digital filter setting results in the minimal achievable NMSE between $x(t)$ and $\hat{x}(t)$. Theorem 1 generalizes the celebrated Shannon-Nyquist theorem, as stated in the following corollary:

**Corollary 1:** When $x(t)$ is bandlimited and the sampling frequency satisfies Nyquist condition, the resulting NMSE is zero.

*Proof:* If $x(t)$ is bandlimited, then there exists some finite $f_m$ such that $S_x(f) = 0$ for all $|f| > f_m$. When the sampling rate satisfies Nyquist condition, then $f_s \geq 2f_m$. Consequently, the summands in (9) are non-zero only at $k = k' = 0$, and hence

$$
\zeta(1/f_s) = 1 - \int_{-f_m}^{f_m} \frac{|S_x(f)|^2}{S_x(f)} df = 0,
$$

proving the corollary.

We next give an example of how Theorem 1 is computed:

**Example 1:** Consider a bandlimited signal whose spectral support is $[-f_m, f_m]$ for some $f_m > 0$ with flat PSD. The obtained NMSE for such signals computed via Theorem 1 is given by

$$
\zeta(1/f_s) = \begin{cases} 
1 - \frac{f_s}{2f_m} & f_s \leq 2f_m, \\
0 & \text{otherwise}. 
\end{cases}
$$

Fig. 4 illustrates of the recovery NMSE result in Theorem 1, showing which spectral portions of a signal with a flat PSD as in Example 1 are preserved by the NMSE minimizing reconstruction. In particular, Fig. 4 demonstrates how the complete spectrum is preserved when sampling above Nyquist rate, while sub-Nyquist sampling yields some recovery error due to aliased components. Fig. 4 also depicts the amount of energy harvested from the signal based on (8), showing that reduction in the sampling rate allows to harvest more energy in $\epsilon$-Sampling at the cost of less accurate recovery, leading to the energy-fidelity tradeoff of $\epsilon$-Sampling analyzed in the sequel.

**C. Energy-Fidelity Tradeoff**

In order to express the energy consumed in acquisition, we must first specify the voltage of the power supply $V_{\text{ref}}$. This value should be larger than the amplitude of the input signal with high probability to avoid overloading the ADC. Consequently, in the following we write the value of $V_{\text{ref}}$ as some multiple $K > 1$ of the input standard deviation, i.e., the supply voltage is written as $V_{\text{ref}} = K\sigma_x$. This general formulation allows us to relate the reference voltage with the overload probability of the quantizer, since
Figure 4. Illustration of eSampling of a signal with a flat PSD for: (a) Sampling at Nyquist rate, while harvesting an amount of energy proportional to $T_h = 1/f_s - T_{aq}$; (b) Sampling at sub-Nyquist rate, thus trading recovery accuracy for harvesting more energy.

the overload probability satisfies $P(|x(t)| \geq V_{ref}) \leq K^{-2}$ by Chebyshev’s inequality [11]. Therefore, the ratio between the expected energy harvested (8) and consumed (5) for eSampling of a WSS signal can be written as

$$E_{\text{ratio}} = \frac{\eta R_h (T_s - T_{aq}) \sigma_x^2}{a_2(n) K^2 \sigma_x^2 + a_1(n) K \sigma_x}.$$  

(12)

Recall that for a fixed sampling interval, eSampling ADCs implement the same conversion mapping as conventional S/H ADCs. Consequently, when one does not account for the distortion induced in quantization as we do here, WSS signals acquired by an eSampling ADC operating with sampling interval $T_s$ can be recovered with the NMSE $\zeta(T_s)$ stated in Theorem 1. We therefore use the expressions for the achievable NMSE (9) and the energy ratio (12) to characterize the energy-fidelity tradeoff of eSampling.

Under the considered setting, we formulate how the recovery accuracy and the energy ratio behave as the sampling period $T_s$ varies. Recalling that the acquisition time $T_{aq}$ is determined by the ADC circuit parameters (1), modifying the sampling period is equivalent to tuning the hold time $T_h$. The energy-fidelity tradeoff of eSampling is thus encapsulated in two complementary optimization problems: The
first aims at finding the minimal achievable NMSE under a given energy constraint $\delta > 0$, i.e.,

$$\zeta^* (\delta) = \min_{T_s > T_{aq}} \zeta,$$  \hspace{1cm} (13)

subject to $E_{ratio} \geq \delta$.

Setting $\delta = 0$ dB, implies that $E_{hold} = E_h$. Therefore, solving (13) with $\delta = 0$ dB reveals the minimal NMSE achievable by an $e$Sampling ADC which harvests at least as much energy as it consumes, i.e., when operating at zero power. A positive value of $\delta$ (in dB) implies an energy saving ADC which harvests more energy than its consumption per sample, namely, converting the signal only adds power to the system.

An alternative formulation seeks to maximize the energy harvested under a given fidelity constraint $\epsilon > 0$, i.e.,

$$E_{ratio}^\epsilon (\epsilon) = \max_{T_s > T_{aq}} E_{ratio},$$  \hspace{1cm} (14)

subject to $\zeta \leq \epsilon$.

For instance, consider a bandlimited signal. In such a case, one can achieve $\zeta = 0$ by $e$Sampling at Nyquist rate, and harvest energy ratio $E_{ratio}^{opt}(0)$, i.e., the maximal ratio of the harvested to energy to the consumed one when seeking ideal recovery. For non-bandlimited signals, approaching zero NMSE generally requires infinitesimally small sampling interval, which is not feasible due to the lower bound on $T_s$ dictated by the ADC circuity in (3). Consequently, when acquiring non-bandlimited signals (or extremely wideband signals), one would typically be more interested in evaluating (14) for some small yet feasible NMSE bound $\epsilon > 0$.

Problems (13)-(14) allow to characterize the energy-fidelity tradeoff, stated in the following theorem:

**Theorem 2:** Let $T_h(\delta)$ be given by

$$T_h(\delta) := \frac{\delta R_h}{\eta \sigma^2_x} \left( a_2(n) K^2 \sigma^2_x + a_1(n) K \sigma_x \right).$$

By setting $f_s(\delta) = \frac{1}{T_{aq} + T_h(\delta)}$, the solution to (13) is

$$\zeta^* (\delta) = 1 - \frac{1}{\sigma^2_x} \sum_{k \in \mathbb{Z}} \int_{-\frac{f_s(\delta)}{2}}^{\frac{f_s(\delta)}{2}} \frac{|S_x(f - kf_s(\delta))|^2}{S^H_x(f - k' f_s(\delta))} df.$$  \hspace{1cm} (15a)

Similarly, by letting $T_s(\epsilon)$ be the maximal sampling interval satisfying $\zeta(T_s(\epsilon)) = \epsilon$ in (9), then the solution to (14) is

$$E_{ratio}^\epsilon (\epsilon) = \frac{\frac{\eta R_h}{2}(T_s(\epsilon) - T_{aq}) \sigma^2_x}{a_2(n) K^2 \sigma^2_x + a_1(n) K \sigma_x}.$$  \hspace{1cm} (15b)
Proof: The theorem follows by noting that $\zeta(T_s)$ in (9) is monotonically decreasing in $T_s$, while $E_{\text{ratio}}$ in (12) is a monotonically increasing function of $T_s$. Consequently, both (13) and (14) are obtained by identifying the minimal/maximal value of $T_s$ for which the constraint holds with equality, hence proving the theorem.

In the following subsection we provide a few examples of energy-fidelity tradeoffs which arise from the above analysis.

D. Examples

The characterization of the energy-fidelity tradeoff in Theorem 2 identifies the achievable energy ratio for a given recovery accuracy and vice versa. It also reveals the achievable energy ratio when $e$Sampling a bandlimited signal of maximum frequency $f_m \geq 0$ with zero reconstruction error. In particular, combining Corollary 1 and Theorem 2 indicates that this energy ratio is given by

$$E_{\text{ratio}}^0(0) = \frac{R_h}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}.$$  (16)

An example of how Theorem 2 is computed for arbitrary sampling rates is given in the following:

**Example 2 (Flat PSD):** Consider again the bandlimited signal with flat PSD of Example 1. In this case, by (11), an NMSE of $\zeta(1/f_s) \leq \epsilon$ is guaranteed by using $f_s \geq 2f_m(1-\epsilon)$. Consequently, by Theorem 2 the energy ratio under fidelity constraint $\epsilon$ for such signals is given by

$$E_{\text{ratio}}^0(\epsilon) = \frac{R_h}{a_2(n)K^2\sigma_x^2 + a_1(n)K\sigma_x}.$$  (17)

The resulting energy-fidelity tradeoff curve for different numbers of quantization bits is depicted in Fig. 5 under the following settings: We use $K^2 = 20$, guaranteeing a probability of over 95% that $|x(t)| \leq V_{\text{ref}}$, while the ADC circuit parameters are set to $f_m = 19.8$ MHz, $T_{\text{aq}} = 2.5$ ns, $C_u = 10$ fF, $C_c = 5$ fF, $C_s = 0.7$ fF, $R_h = 23.75$ $\Omega$, $A_k = 1.8$, $V_e = 0.05$ V, $\alpha_x = 5$, $V_{\text{ref}} = 0.8$ V, $g = 0.4$, and $\eta = 0.7$. Finally, the signal power $\sigma_x^2$ is accordingly set to $V_{\text{ref}}^2/2R_h$.

The specific design parameters used in evaluating Fig. 5 correspond to the $e$Sampling ADC circuit design presented in Section IV, and are in the typical ranges provided in previous works on ADC circuitry, e.g., [30], [39], [40]. The efficiency of the energy harvesting system $\eta$ is in line with similar values reported for energy harvesting circuits in [41]–[43].

As expected, the achievable energy ratio in Example 2 coincides with (16) when perfect recovery is required, i.e., $\epsilon = 0$. The energy ratio characterized in (17) is increased by reducing the sampling rate, which in turn increases the reconstruction error, $\epsilon$, as illustrated in Fig. 4. The fundamental balance between these measures follows from the structure of $e$Sampling ADCs, in which increasing the hold
time degrades the ability to recover the signal from its samples, while allowing to harvest more energy. This unique property of $e$Sampling can lead to ADCs which harvest more power than they consume, as observed in Fig. 5.

The results shown in Fig. 5 demonstrate that an $e$Sampling ADC with up to 12 bits acquiring a bandlimited signal can harvest more power than it consumes while sampling at Nyquist condition, and hence achieving zero-approaching reconstruction error. While the ability of $e$Sampling ADCs to sample at Nyquist rate and zero-power is observed in Fig. 5 for signals with flat PSDs, it holds for arbitrary PSD shapes as long it is bandlimited to $f_m$ and the variance of the signal is $\sigma_x^2$. This follows since by (12), the energy ratio for a given sampling rate and signal variance does not depend on the shape of the PSD. However, for the ADC to operate at zero power with higher resolution quantization, one has to sample below the Nyquist rate and hence compromise in reconstruction error. In particular, each of the curves in Fig. 5 reaches zero NMSE for $f_s = 2f_m$, while reducing the sampling rate allows achieving improved energy ratio at the cost of reduced reconstruction accuracy, reaching poor recovery performance of $\zeta = 0.85$ as $f_s$ is reduced to $0.3f_m$. It is emphasized that for a given sampling rate, $e$Sampling ADCs implement the same acquisition mapping as conventional S/H ADCs, and thus their the ability to harvest energy using $e$Sampling ADCs does not come at the expense of conversion accuracy. However, $e$Sampling provides to possibility to increase the amount of energy harvested by increasing the sampling interval, which in turn may degrade the ability to recover the analog signal.

As discussed above, while the recovery NMSE depends not only on the sampling rate but also on the

Figure 5. NMSE ($\zeta$) versus $E_{ratio}$, flat PSD.
shape of the PSD $S_x(f)$ (9), the energy ratio for a fixed sampling rate is affected only by the overall input energy $\sigma_x^2 = \int S_x(f)df$ (12). This follows from the fundamental difference between the two objectives of eSampling, i.e., acquisition and energy harvesting: The purpose of acquisition is to allow the complete signal, whose profile depends on the shape of its PSD, to be recovered from its digital representation. However, energy harvesting aims at extracting energy from the signal without having to maintain sufficiency or to avoid distorting the signal, and is invariant of the specific shape of its PSD. The dependency of the energy-fidelity tradeoff on the PSD profile is demonstrated in the following two examples which, unlike Example 2, consider non-purely-bandlimited signals:

**Example 3 (Unimodal PSD):** Let $x(t)$ be a WSS signal with a PSD given by $S_x(f) = \alpha e^{-\frac{f^2}{2\sigma^2}}$, where $\alpha = \frac{\sigma_x^2}{\sqrt{2\pi}^2}$ such that $\int_{-\infty}^{\infty} S_x(f)df = \sigma_x^2$. The parameter $\sigma^2$ controls the PSD width, and is set to $\sigma = f_m/3$. The resulting energy-fidelity tradeoff computed via Theorem 2 under the ADC circuit parameters used in Example 2 is depicted in Fig. 6, along with an illustration of the PSD.

**Example 4 (Multimodal PSD):** Let $x(t)$ be a WSS signal with a PSD $S_x(f) = \frac{\sigma}{2}(e^{-\frac{(f-f_m)^2}{2\sigma^2}} + e^{-\frac{(f+f_m)^2}{2\sigma^2}})$. Here, $\sigma$ is set to $\sigma = f_m/6$. This PSD profile and the energy-fidelity tradeoff evaluated using Theorem 2 under the ADC circuit parameters used in Example 2 is depicted in Fig. 7.

These examples illustrated in Figs. 6 and 7 demonstrate that eSampling ADCs applied to signals with such spectral profiles can operate with zero power for up to $n = 16$ bits of quantization resolution, while achieving approximately ideal reconstruction. Observing Figs. 6-7 and comparing them to Fig. 5, we note that different PSD profiles lead to different energy-fidelity curves. This property is solely due to the
dependence of the achievable NMSE on the PSD, which follows from Theorem 1, since both the amount of energy harvested from a stationary signal as well as that consumed in eSampling do not depend on the spectral profile of the signal, but on the sampling rate and the variance $\sigma_x^2$.

In particular, the amount of energy harvested (8) when eSampling at $f_s = 2f_m$ is numerically evaluated as 0.35 pJ, while the corresponding amount of energy consumed (21) when using $n = 8$ bit quantizers is 21.2 pJ. This implies that the eSampling ADC is able to harvest much more energy from the signal than it consumes in converting it into a digital representation, as the energy ratio indicates an energy gain of 17.8 dB. In particular, it is observed that eSampling ADCs operating with up to 16 bits per sample are capable of saving power. However, this mode of operation comes at the cost of increased NMSE for higher values of $n$. The examples presented in this subsection indicate that the power consumption of high resolution ADCs can be notably reduced and even mitigated by properly combining acquisition and energy harvesting via eSampling. In Section IV we demonstrate that these results do not follow only from a numerical evaluation of our theoretical results, but also reflect the performance in terms of recovery accuracy and energy efficiency of a dedicated eSampling ADC circuit design.

E. Discussion

Our characterization in the previous subsections focuses on the general family of stationary signals. When the signal obeys some structure, e.g., it is known to be sparse in the frequency domain, ideal recovery can be achieved at low sampling rates using generalized sampling methods [2], allowing
to harvest more energy without affecting the recovery NMSE. This indicates that the energy-fidelity tradeoff of $e$Sampling ADCs can be further improved by accounting for structured signals, as commonly encountered in communication [8] and radar [9] systems. We leave the analysis of $e$Sampling of structured signals for future work.

The fact that $e$Sampling gives rise to ADCs which operate with zero power and can even harvest more energy than they consume, makes it an attractive technology for low-power systems, such as internet of things devices, sensor networks, as well as wearable and implantable medical units. However, the applicability of the proposed $e$Sampling ADC is limited in some scenarios since its architecture is based on S/H ADCs. For example, S/H ADCs typically operate at sampling rates below 1 GHz, and are not suitable for operating at extremely high sampling rates, where flash ADCs are more commonly used. While we conjecture that the concept of $e$Sampling, namely, the integration of energy harvesting into signal acquisition, can also be combined with alternative ADC technologies other than S/H, we leave this study for future research.

While our analysis focuses on WSS signals for analytical tractability, the proposed $e$Sampling ADCs applies to a much broader family of acquired analog signals. For example the $e$Sampling ADC circuitry detailed in the following section is experimented when acquiring a sinusoidal signal, demonstrating its ability to accurately reconstruct the signal in a power saving manner. Furthermore, our proposed analysis is based on linear recovery, being a common reconstruction framework in sampling theory. In particular, the reconstruction of Nyquist rate sampled bandlimited signals, shift-invariant signals, and various other structures studied in the literature, is based on linear filtering [2]. However, the architecture of the $e$Sampling ADC is invariant to the reconstruction mechanism, and alternative recovery schemes would result in a different characterization of the energy-fidelity tradeoff.

IV. $e$Sampling ADC Circuit-level Design

In order to demonstrate the hardware feasibility of the concept of $e$Sampling, we present the circuit-level design of such a device. In particular, we design an $e$Sampling ADC circuit based on the model shown in Fig. 2 using standard 65 nm CMOS technology, and carry out its experimental study using a Cadence Virtuoso platform. In order to design the $e$Sampling ADC based on the high-level architecture illustrated in Fig. 2, one has to design its three main sub-blocks: The two-way switch $\tilde{S}$; the quantizer logic; and the energy harvesting circuit. We thus first elaborate on each of these sub-blocks, after which we present the experimental study.
A. Two-way switch

The two-way switch $\tilde{S}$ allows the input signal to be connected to the hold capacitor during acquisition phase and to the energy harvesting circuit during the hold phase. In our design, $\tilde{S}$ is implemented using two one-way switches, one for each operation phase, namely, when one switch is open, the other is closed. Each of these switches is realized using a different topology. The switch designed to connect the input signal to the energy harvesting circuit is implemented using a PMOS transistor, as illustrated in Fig. 8(a). The PMOS transistor turns ON when the clock signal $Clk$ is at logic '0', indicating that hold phase is active. When $Clk$ is at logic ‘1’, it turns OFF and isolates the input signal from the next block. In order to allow both switches of $\tilde{S}$ to utilize the same single clock pulse, the switch designed to connect the input signal with the quantizer is implemented using an NMOS transistor, which turns on when $Clk$ is at '1'.

The on-resistance of a MOS transistor, which determines the value of $R_{on}$ in (1), is sensitive to fluctuations in the input signal and may vary accordingly [24]. Such variations in $R_{on}$ may introduce a non-linear distortion at the output of the ADC. To avoid such distortion, we use an NMOS bootstrap switch to connect the input signal to the quantizer, which ensures a constant $R_{on}$, as proposed in [44]. The design of the NMOS transistor based bootstrapped switch used in this work is illustrated in Fig. 8(b). To achieve nearly constant $R_{on}$, the gate of the transistor $M1$ in Fig. 8(b) is bootstrapped using two PMOS transistors $M2$ and $M3$, three NMOS transistors $M4$, $M5$ and $M6$, and one capacitor $C_B$, following [44]. Two CMOS inverters $I1$ and $I2$ are also employed in the structure to generate the required clock.

Figure 8. Circuit diagram of (a) PMOS transistor switch, (b) NMOS bootstrapped switch.

1The term ‘implement’ used here implies the design/simulation of the circuit in Cadence Virtuoso platform, in line with the similar usage of this terminology in [20]–[23], [26].
signals needed for proper operation of the switch.

The value of the on-resistance $R_{on}$ as well as the hold capacitor $C_h$ affect the setting of the acquisition time $T_{aq}$, as follows from (1). To maximize the amount of energy harvested, small values of $T_{aq}$ are preferable, so that more time could be allocated to harvesting the input signal energy. Reducing $R_{on}$ requires increasing the width of the transistors [24], which in turn increases the device capacitance, and thus reduces the operating speed of the ADC. In addition, wider devices may result in charge injection [45], which degrades the signal-to-noise-distortion ratio (SNDR) of the ADC, and hence the performance of the ADC. Alternatively, employing small values for $C_h$ results in mismatch issues and sampling noise, which degrade the ADC conversion accuracy [46], [47]. These drawbacks require the acquisition time $T_{aq}$ to be large enough such that the ADC performance is not compromised, and is in fact the primary reason S/H ADCs are typically limited to operate with sampling rates below 1 GHz, as discussed in Subsection III-E.

B. Quantizer

The dedicated eSampling ADC circuit design is based on S/H SAR ADC architectures [25], [30], [48] as illustrated in Figs. 1-2. Such quantizers generally consist of a DAC, a voltage comparator and a SAR logic, which map the voltage of the hold capacitor (also known as the total capacitance of DAC array) into an $n$-bit value by successively refining the digital representation using a binary search algorithm. In our eSampling ADC circuit we use a single-ended merge capacitor switching (MCS) based SAR ADC. For such devices, the total capacitance of the DAC array is $C_h = 2^{n-1}C_u$, where $C_u$ is the unit capacitance of the DAC array, as illustrated in Fig. 9.

In particular, during acquisition phase the input signal $x(t)$ is connected to the top plate of the DAC capacitor array, while the bottom plate is connected to the common mode voltage, i.e., $V_{cm} = \frac{V_{ref}}{2}$. Once the acquisition phase is over, the voltage at the top plate of the DAC capacitor array is reduced by common mode voltage, and hence equals to $x(kT_s) - \frac{V_{ref}}{2}$. The top plate of the DAC capacitor array is connected to the positive terminal of the comparator, while the negative terminal of the comparator is grounded. The comparator then compares the voltage of its positive terminal with its negative terminal. If the voltage at the positive terminal is higher than the negative terminal, the comparator yields an output of logic ‘1’, else logic ‘0’. The output of the comparator is passed to the SAR logic, which resolves the most significant bit (MSB). The decision on the MSB is fed back to the DAC and the bottom plate of the largest capacitor of DAC capacitor array is switched from $V_{cm}$ to ground (if MSB=1) or $V_{ref}$ (if MSB=0). This operation changes the voltage at the top plate of the DAC capacitor array, and a new decision is made by the comparator, which is sent to the SAR logic to resolve the second MSB and so on. The
process continues for all \( n \) bits. The overall resistance of the switches is determined by the binary scale switch resistance, \( R_q \), as illustrated in Fig. 9.

As discussed in Subsection II-A, the energy consumption of S/H SAR ADCs is effectively dictated by its quantization sub-blocks. Therefore in the following, we detail the circuitry used for the quantizer along with its energy usage per sample.

The voltage comparator is implemented using a dynamic latch. The energy consumed per sample of a dynamic latch comparator is given by [30]

\[
E_c = nC_c V_{\text{ref}}^2 + 2V_{\text{ref}}\gamma_n,
\]

where \( \gamma_n := V_c C_c \left( n \ln 1/A_k + \frac{n(n+1)}{2} \ln 2 + n \right) \), \( C_c \) is the capacitive load of the comparator, \( A_k \) is the gain during regenerative phase, and \( V_c \) is the ratio of the drain current of the device with its trans-conductance [39]. The SAR logic is realized using two arrays of shift registers that operate in serial-in-parallel-out and parallel-in-parallel-out modes [49]. Each register is implemented using a D flip-flop circuit, and the resulting energy consumption is given by [30]

\[
E_{sl} = 16n^2 g C_s V_{\text{ref}}^2,
\]

where \( C_s \) is the input capacitance of the D flip-flop, and \( g \in [0, 1] \) is the total activity parameter of the SAR logic. Finally, the DAC is based on a binary-weighted capacitive DAC, designed using the MCS
scheme [25]. The energy consumption of the MCS DAC is given by [25]

\[ E_{DAC} = \rho_n n C_u V_{ref}^2, \]  

(20)

where \( \rho_n = \sum_{i=1}^{n-1} 2^{n-3-2i}(2^i - 1) \).

To summarize, the total energy consumption during hold phase of our dedicated eSampling ADC circuit design, which dictates the overall energy consumed per sample, is given by

\[ E_{\text{hold}} = E_{DAC} + E_{sl} + E_c \]

\[ \overset{(a)}{=} V_{ref}^2 (\rho_n C_u + n C_c + 16 n^2 C_s g) + 2V_{ref}\gamma_n, \]  

(21)

where \( (a) \) follows from (18), (19), and (20). The energy term in (21) obeys the second-order polynomial model of (4), used in our analysis of eSampling ADCs in Section III.

C. Energy Harvesting Circuit

The proposed eSampling ADC harvests the input signal energy during hold phase and stores this energy in a capacitor, \( C_{EH} \). As detailed in Subsection II-B, energy harvesting circuits typically consist of a capacitor, in which the harvested energy is stored, and a signal conditioning circuit, whose purpose is to facilitate the charging of the capacitor. In our design, we do not include a signal conditioning circuit and forward the input signal directly to \( C_{EH} \) during hold time. This simplified design is sufficient for our experimental purposes, where we use synthetic controlled input signals with strictly positive voltage values. However, in order to achieve efficient energy harvesting of a low voltage complex rapidly alternating signals, one should also include signal conditioning devices, such as a rectifier, voltage regulator, and DC-DC converter.

To quantify the maximum amount of energy that can be harvested in an analytically tractable manner, we consider the case where the input signal is approximately constant during the hold phase, i.e., \( x(t) \approx x(T_s) \) for each \( t \in [T_{aq}, T_s] \). The purpose of this approximation is to facilitate characterizing the amount of energy harvested in a tractable manner. In addition, we focus on the scenario in which the capacitor is empty at the beginning at the hold phase, namely, the voltage on the capacitor \( C_{EH} \), denoted \( V_{EH}(0) \), satisfies \( V_{EH}(T_{aq}) = 0 \). In this setup, the capacitor voltage at the end of the hold phase, i.e., at time instance \( t = T_s \), is given by

\[ V_{EH}(T_s) \approx x(T_s) \left( 1 - e^{-\frac{T_s}{\tau_{EH}}} \right), \]  

(22)
where, as defined in Subsection III-A, $R_h$ is the resistance of the energy harvesting circuit. This resistance is dictated here by the on-resistance of the PMOS transistor in the two-way switch. The amount of energy harvested in such a sampling interval is given by

$$E_h = \frac{1}{2} C_{EH} V_{EH}^2(T_s)$$

$$(a) \approx \frac{1}{2} C_{EH} \left( 1 - e^{-\frac{T_h}{R_h C_{EH}}} \right)^2 x^2(T_s)$$

$$(b) \approx \frac{1}{2T_h} C_{EH} \left( 1 - e^{-\frac{T_h}{R_h C_{EH}}} \right)^2 \int_{T_{hs}}^{T_h} |x(t)|^2 dt, \quad (23)$$

where (a) follows from (22), and (b) stems from the fact that the input is approximately constant during the hold phase. Comparing (23) and (8) reveals that the efficiency of this simple energy harvesting circuit can be approximated as

$$\eta \approx \frac{R_h C_{EH}}{2T_h} \left( 1 - e^{-\frac{T_h}{R_h C_{EH}}} \right)^2. \quad (24)$$

The expression for the energy harvesting efficiency in (24) can be used to provide guidelines for determining the capacitance $C_{EH}$ used in the circuit. In particular, it can be shown that (24) is maximized when $C_{EH} \approx 0.796 \frac{T_h}{R_h}$. However, the derivation of (24) is carried out assuming that the capacitor is empty at the beginning of the hold phase. This implies that its stored energy is transferred to some external storage device, e.g., battery, after each sample. In practice, energy transfer typically takes much longer than a single sampling interval, and thus it is preferable to carry out such a transfer only once every multiple samples. This is achieved by using a capacitor with a larger value of $C_{EH}$, which allows to store more energy and provides a nearly constant voltage at the load, but requires more time to charge. In particular, in our experimental setup detailed in Subsection IV-D, we set $C_{EH} = 42.2 \frac{T_h}{R_h}$, which results in the capacitor taking approximately 340 samples to charge up. Under such a setting, the period dedicated to transferring its energy once it is fully charged, during which energy harvesting is inactive, has only a minor effect on the overall harvested energy.

**D. Experimental study**

To validate that the energy saving potential of eSampling ADC observed in Section III also reflects its behavior in a real world environment, we next evaluate the eSampler circuit design. To that aim, a schematic of the eSampling ADC circuit has been created in Cadence Virtuoso platform based on the circuit-level design detailed in the previous subsections. The proposed eSampling ADC operates at a sampling frequency of 40 MHz with an $n = 8$ bit quantizer. For our experimental purpose, we use a sinusoidal signal, being a common benchmark for evaluating the accuracy of ADC circuits [50, Ch. 2].

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The maximum frequency of the input signal is 19.8 MHz, thus the sampling rate satisfies the Nyquist condition. The amplitude of the signal varies from 0 to $V_{\text{ref}}$. Here, we use an energy harvesting capacitor of $C_{\text{EH}} = 40$ nF, while the remaining parameters are the same those detailed in Examples 2-4.

We first assert that the eSampling ADC is indeed capable of accurately reconstructing the signal sampled at the Nyquist rate. To that aim, we depict the fast Fourier transform (FFT) of the reconstructed signal, computed using a 1024-point FFT, in Fig. 10. As expected, the FFT noise floor is determined by the SNDR due to quantization, computed by the 6 dB rule of thumb as approximately 48 dB, with the additional FFT processing gain of $10\log_{10}(1024/2) \approx 27$ dB [50, Ch. 2]. In particular, the gap between the noise floor observed in Fig. 10 and the energy of the signal at its central frequency of 19.8 MHz, is roughly $75.52$ dB, settling with the theoretical performance of ADCs satisfying Nyquist condition, and indicating that the designed eSampling ADC accurately reconstructs the observed analog signal.

Next, we focus on the energy harvesting circuit of the designed eSampler, in order to identify how many sampling rounds are required for the capacitor to charge up. To that aim, we plot in Fig. 11 the voltage on the energy harvesting capacitor over time. Observing Fig. 11, we note that for the given input signal, the capacitor reaches a steady level of $V_{\text{EH}} = 481.152$ mV after 8.432 $\mu$s, which correspond to 337 samples at 40 MHz. Based on Fig. 11, we design the eSampling ADC to transfer the energy stored in its energy harvesting capacitor once every 337 samples. We dedicate approximately 1.5 $\mu$s for each transfer, during which the energy harvesting circuit is inactive, resulting in each cycle of harvesting and transferring taking approximately 500 samples. Consequently, the effective amount of energy harvested
per sample of the eSampling ADC is given by

\[ E_h = \frac{1}{2 \cdot 500} C_{EH} V_{EH}^2 (337 \cdot T_s) = 9.26 pJ. \] (25)

The amount of energy harvested per sample, evaluated in (25) based on the experiment in Fig. 11, does not represent the overall energy balance of the eSampling ADC, as it accounts only for the amount of energy harvested. Therefore, to demonstrate that the eSampling ADC circuit design not only accurately recovers the signal and harvests energy, but also saves more energy than it consumes, we next evaluate both the energy harvested and the energy consumed by the ADC circuit. The average energy consumption of our designed circuit is computed by evaluating the current drawn from its reference source \( V_{ref} \), denoted \( I_{ref}(t) \), and thus the energy consumed at each time instance can be obtained by

\[ E_{cons}(t) = V_{ref} \int_0^t I_{ref}(\tau)d\tau. \] (26)

The resulting growth of both the energy consumed and the energy harvested are depicted in Fig. 12. Observing Fig. 12, we note that the eSampling ADC harvests much more energy than it consumes, while still being able to accurately reconstruct its input signal as demonstrated in Fig. 10. In particular, the consumed energy is shown to grow in an approximately linear manner, with an average energy consumption of 0.56 pJ per sample. The maximal amount of energy which can be obtained is dictated by the external battery, to which the harvested power is periodically transferred. Comparing this to (25) reveals that the true energy ratio of the eSampling ADC, which periodically transfers its harvested energy to an external battery, is approximately 12.1 dB, which is within a relatively small gap from the theoretical
results observed in Subsection III-D. This gap can be further reduced by using more advanced energy harvesting circuitry, compared to the simplistic design detailed in Subsection IV-C. In particular, using more advanced harvesting architecture can increase the efficiency $\eta$, allowing to achieve improved energy-fidelity tradeoffs compared to those observed here. Nonetheless, despite its relatively simple architecture, the $e$Sampling ADC circuit design is still shown to be able to achieve accurate reconstruction while harvesting substantially more energy than it consumes.

V. CONCLUSION

In this paper, we proposed the $e$Sampling ADC architecture, which modifies the traditional conversion process of a S/H ADC to harvest energy from the discarded portion of the input signal. We analyzed the amount of energy which can be harvested from stationary signals and characterized the underlying fundamental tradeoff between energy harvested and reconstruction fidelity which arises from the joint acquisition and energy harvesting paradigm. Our theoretic characterization reveals that an $e$Sampling ADC with up to 12 bits can harvest more power than it consumes, when sampling both bandlimited signals and non-bandlimited ones at a sampling rate allowing recovery with negligible error. Then, we presented a circuit-level design of an $e$Sampling ADC using CMOS 65 nm technology demonstrating the feasibility of this concept. Our experimental results validated the theoretical observations, showing that an $e$Sampling 8-bit ADC circuit applied to a sinusoidal signal harvests more power than it consumes while recovering the analog signal in a nearly perfect manner.
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