A Study on Ultra Low Power High Linear LNA Based on Dual Cross-Coupling Capacitance Feedback in Artificial Intelligence

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Abstract. In this paper, by means of big data technology and RF feedback technology, the dual capacitor feedback technology is further proposed in the amplifier. Then, through the double-cross coupling structure, the harmonic signal is weakened in different feedback loops, so as to achieve the improvement of IIP3 and the realization of ultra-low power and high linear LNA.

Keywords: Artificial Intelligence, Input Third-Order Cut-Off Point, High Linearity, Low Noise Amplifier, Negative Feedback

1. Introduction

First of all, for a very short period of time, the capacitor is inside the circuit, which means that instead of electrons passing through between the electrodes of the capacitor, the electrons will accumulate on one side of the plate, and they'll build up. On the other hand, at the other end of the board, the potential is different because of the difference in the number of electrons on the other side. This is when the field is created. There is a field between the plates, there is a potential, which is equivalent to a battery. If the polarity of one of the plates on which the capacitor stores the charge changes suddenly, the negative electrode, where the electrons are stored, suddenly sucks them back into the cell (as does the positive electrode) [1,2]. At this point, the electrons at both ends of the capacitor's polarity move quickly, which is equivalent to a current (this can happen even if the capacitor's polarity changes at one end and the other end is grounded). This is the coupling function of the capacitor. In this paper, the research of ultra-low power and high linear LNA based on double cross-coupling capacitor feedback is discussed.

2. About capacitive feedback

The basic function of feedback is to use linear active devices in the feedback path to correct the nonlinearity generated by nonlinear active devices in the forward path of the circuit. feedback is an
effective way to improve linearity in analog and rf circuits [3-5]. However, in the rf domain, feedback may cause harmonic feedback components that deteriorate the linearity of the circuit. In the low frequency domain, the harmonic feedback component is usually suppressed by the high loop gain. However, in the rf domain, it is difficult to obtain the high loop gain because the open loop gain is already very low. For example, in a common-source circuit structure, voltage-current feedback techniques implemented with source-pole degenerate inductors do not improve the performance IIP3 the input third-order cut-off points. This is because the source-pole degenerate inductors generate second-harmonic components at the source end of the amplified transistor, feedback back to the input port via capacitor feedback between transistor gate sources, are mixed with the original signal into third-order alternating modulation components IMD3, and degenerate circuit IIP3, exist in many rf feedback circuits.

3. Circuit design and theoretical analysis

3.1. Feedback and IIP3

The third-order intermodulation distortion modulation distortion cutoff point of the feedback system is:

\[ AIP3_{cl} = \sqrt{\frac{4}{3} \frac{b_3}{b_1}} = \frac{\sqrt{\frac{4}{3} a_1}}{1 + T} \frac{\left(2a_2^2 f \right)}{(1 + T)^3} \]  

(1)

The b1 is the closed loop linear gain, the b3 is the closed loop third order nonlinear coefficient, the a1, a2 and a3 are the open loop linear gain, the open loop second order nonlinear coefficient and the open loop third order nonlinear coefficient is feedback loop gain.

3.2. Cross-coupled co-gate structure

Figure 1 presents a conventional cross-coupled co-gate (CCCG) topology that reduces the drain thermal noise by half and doubles the circuit gain by increasing the transconductance. Another property of the CCCG structure is to reduce the second-order cross-modulation through a cross-coupled structure. Figure 2 is a schematic diagram of the forward feedback mechanism of the fundamental signal and the second harmonic signal in the CCCG structure [6,7].
Figure 1. Circuit diagram of conventional cross-coupled common-gate amplifiers

(a) Basic wave signal   (b) Second harmonic signal

Figure 2. Positive feedback principle of cross-coupled common-gate circuit
\[ AIP3_{cl} = \sqrt[3]{\frac{4}{3} \left| \frac{b_1}{b_3} \right|} \]
\[ i_{\text{fand}} = g_m \left( v_{\text{in}} + A_i v_{\text{in}} \right) \]  
\[ (2) \]
\[ i_{2\text{nd}} = g_{m2} \left( v_{\text{in}} - A_i v_{\text{in}} \right)^2 \]  
\[ (3) \]
\[ b_{1\text{CCCG}} = \frac{2 \left\{ \frac{C_c}{C_c + C_{gs}} \right\} g_m (Z_s / R_s) Z_{\text{load}}}{1 + 2 \left\{ \frac{C_c}{C_c + C_{gs}} \right\} g_m (Z_s / R_s) Z_{\text{load}} R_s} \]  
\[ (4a) \]
\[ a_{1\text{CCCG}} = \frac{2 \left( \frac{C_c}{C_c + C_{gs}} \right) g_m (Z_s / R_s) Z_{\text{load}}}{R_s} \]  
\[ (4b) \]
\[ a_{3\text{CCCG}} = \frac{1}{3} \left( \frac{C_c}{C_c + C_{gs}} \right) g_m'' (Z_s / R_s) Z_{\text{load}} \]  
\[ (4c) \]
\[ T_{\text{CCCG}} = \frac{2 \left( \frac{C_c}{C_c + C_{gs}} \right) g_m (Z_s / R_s)}{R_s} \]  
\[ (4d) \]
\[ F_{\text{CCCG}} = \frac{R_s}{Z_{\text{load}}} \]  
\[ (4e) \]

Where the Rs is the input source impedance ;2 Cc / (Cc egs) is the transconductance enhancement coefficient, if the Cc is much larger than the transconductance enhancement coefficient approximately 2.

**Figure 3.** Equivalent half-edge circuit of cross-coupled common gate circuit

The third-order intermodulation distortion cut-off point of CCCG topology is obtained from formula (1) and formula (4) AIP3CCCG as follows:
The formulas (4d) and (5) show that if the transconductance \( g_m \), is increased, the loop gain can be increased \( T_{CCCG} \), and the \( AIP3CCCG \) can be improved. The loop gain.

3.3. Double cross coupled common gate structure

The block diagram of the double feedback loop is given in figure 5, in which the \( A \) is an open loop amplifier, the \( f \) is a feedback coefficient, the \( S_i \) is an input signal, the \( S_o \) is an output signal, and the \( S_e \) is the difference between the \( S_i \) and the two [8].

\[
AIP3CCCG \approx \frac{4}{3} \sqrt{\frac{a_{1CCCG}}{T_{CCCG} + 1}} \left( \text{and} \right) \left( \frac{g_m^2}{8} \left[ 2g_m \left( Z_s || R_s \right) + 1 \right] \right) \quad (5)
\]

Among them:

\[
S_e = S_i - f_1 S_o - f_2 S_o
\]

(6b)
Among them:

\[ b_{1\text{dual}} = \frac{a_1}{1 + T_1 + T_2} \quad T_s = a_1 f_s \]  

(7b)

\[ b_{2\text{dual}} = \frac{a_2}{(1 + T_1 + T_2)^3} \]  

(7c)

\[ b_{3\text{ dual}} = \frac{a_3(1 + T_1 + T_2) - 2a_2^2(f_1 + f_2)}{(1 + T_1 + T_2)^5} \]  

(7d)

The \( b_{1\text{dual}} \), \( b_{2\text{dual}} \) and \( b_{3\text{dual}} \) are closed-loop linear gain, second-order nonlinear coefficient and third-order nonlinear coefficient, respectively, the \( T_x \) is the feedback loop gain of the corresponding loop. The third-order intermodulation distortion cut-off point of the dual-feedback system can be obtained from formula (1), formula (7b) and formula (7d) AIP3\text{dual} as follows:

\[
AIP_{3\text{dual}} = \sqrt[4]{\frac{4}{3}} \left| \frac{b_{1\text{dual}}}{b_{3\text{dual}}} \right| = \sqrt{\frac{4}{3}} \left( \frac{a_1}{1 + T_1 + T_2} \right)^3 \left[ \frac{2a_2^2(f_1 + f_2)}{1 + T_1 + T_2} \right] \left[ \frac{1}{(1 + T_1 + T_2)^5} \right]
\]  

(8)

The equivalent half-side circuit of the DCCG structure is given in figure 6 to calculate the relevant parameters of the feedback circuit. The relevant parameters of the feedback circuit of the DCCG structure are as follows:

\[
b_{1\text{DCCG}} = \frac{2g_m}{1 + 2g_m} \left( Z_s \parallel R_s \parallel \frac{1}{j\omega C_f} \right) \frac{Z_{\text{load}}}{R_s} \frac{1}{1 + j\omega C_f Z_{\text{load}}} \left( \frac{1}{1 + j\omega C_f Z_{\text{load}}} \right)
\]  

(9a)

\[
a_{1\text{DCCG}} = \frac{2g_m}{1 + 2g_m} \left( Z_s \parallel R_s \parallel \frac{1}{j\omega C_f} \right) \frac{Z_{\text{load}}}{R_s} \frac{1}{1 + j\omega C_f Z_{\text{load}}} \left( \frac{1}{1 + j\omega C_f Z_{\text{load}}} \right)
\]  

(9b)

\[
a_{3\text{DCCG}} = \frac{6}{1} \left( 2g_m \right) \left( Z_s \parallel R_s \parallel \frac{1}{j\omega C_f} \right) \frac{Z_{\text{load}}}{R_s} \frac{1}{1 + j\omega C_f Z_{\text{load}}} \left( \frac{1 + 2j\omega C_f Z_{\text{load}}}{1 + j\omega C_f Z_{\text{load}}} \right)
\]  

(9c)

\[
T_{\text{DCCG}} = 2g_m \left( Z_s \parallel R_s \parallel \frac{1}{j\omega C_f} \right) \cdot \left( 1 + 2j\omega C_f Z_{\text{load}} \right)
\]  

(9d)
When the input source impedance $R_s$ is much less than $1/\omega C_f$, the third-order intermodulation distortion cutoff point of DCCG topology can be deduced from formula (9 AIP3DCCG which can be simplified as follows:

$$\sqrt{8}\left| \frac{g_m}{g_{m}} \left[ 2g_m (Z_s \| R_x) \left\{ \frac{1 + 2j\omega C_f Z_{load}}{1 + j\omega C_f Z_{load}} \right\} + 1 \right] \right|^3$$

(10)

From formula (5) and formula (10), the loop gain is increased to (1) due to the DCCG structure $j\omega C_f Z_{load}/(1 j\omega C_f Z_{load})$ times, thus increasing the AIP3 to $[(1 j\omega C_f Z_{load})/(1 j\omega C_f Z_{load})]^{3/2}$ times, further improving circuit linearity.

4. Chip implementation and test results

Based on the SMIC 0.18 $\mu$m CMOS process, Flow chip implementation and test verification of the LNA proposed in this paper. Figure 7 shows a picture of the LNA chip, Circuit core size 1.03 mm2, the test results of gain S21 input matching parameter S11 and output matching parameter S22 are shown in figure 8. The gain is 18 dB, at 2.4 GHz operating frequency Input and output matching parameters are lower than -10 dB. Figure 9 shows the test results of the noise coefficient NF, At 2.4 GHz frequency, NF dB.2.02 Figure 10 shows the test results IIP3 the third-order cut-off point, At 2.4 GHz frequency, IIP3 up to dBm,8.3 achieved high linearity, The power of the chip is only 2.5 mW. V 1.1 voltage The comprehensive performance index is superior to the test results reported in previous literature, The IIP3 of the circuits designed by the literature are -7.5 dBm and -0.5 dBm, respectively Compared with the high linearity of 8.3 dBm in this paper, LNA at the forefront of the system receiver, Need a high linearity to receive RF signals from the antenna, A high linearity of 8.3 dBm designed in this paper fully meets this need, The noise coefficients of the circuits reported are 6 dB and 2.7 respectively Also slightly inferior to this article obtained 2. The low noise coefficient of 02 dB, the LNA at the front end of the system receiver directly determines the noise performance of the whole receiver, so the smaller the LNA noise coefficient, the better [9,10].

5. Analysis of design results

The LNA proposed in this paper adopts dual feedback loop based on capacitive feedback in CCCG structure, Without compromising other performance, Improve the linearity of the circuit. CCCG structure not only enhances the transconductance of fundamental frequency, Improved gain and noise performance, And the second harmonic signal is suppressed by feedback, Improved linearity, Based on this DCCG structure, Introducing capacitive feedback between transistor sources, Further improve the
linearity of the circuit. Based on the SMIC 0.18 μm CMOS process, Flow chip implementation and test verification of the LNA proposed in this paper. 2.4 GHz, test frequency Experimental results show that the LNA achieves better performance at lower power consumption, If it consumes only 2.5 mW of power, Gain of 18 dB, 2.02 dB noise factor, dBm input third-order cut-off point IIP3, 8.3 At the same time, the input and output match well, The comprehensive performance index reaches the advanced ranks at home and abroad.

6. Conclusion

To sum up, the LNA design based on double cross-coupling capacitor feedback design in this paper can fully meet the requirements of ultra-low power and high linearity, and the comprehensive index has been in the forefront.

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References

[1] YE R F, Horng T S, Wu J M. Two CMOS dual-feedback common-gate low-noise amplifiers with wideband input and noise matching [J]. IEEE Transactions on Microwave Theory and Techniques, 2013, 61(10): 3690-3699.

[2] Parvizi M, Allidina K, Ei-Gamal M N. Short channel output conductance enhancement through forward body biasing to realize a 0.5V 250μW 0.6-4.2GHz current-reuse CMOS LNA [J]. IEEE Journal of Solid-State Circuits, 2016, 51(3): 574-586.

[3] IM D, Nam I A. Wideband digital TV receiver front-end with noise and distortion cancellation [J]. IEEE Transactions on Circuits and Systems—I: Regular papers, 2014, 61(2): 562-574.

[4] Stewart D, Saavedra C E. Extending the bandwidth of low-noise microwave amplifier through dKIM N, AParkin V, LarsoN L E. Analysis of IM3 asymmetry in MOSFET small-signal amplifiers [J]. IEEE Transactions on Circuits and Systems—I: Regular papers, 2011, 58(4): 668-676.

[5] Sansen W. Distortion in elementary transistor circuits [J]. IEEE Transactions on Circuits and Systems—II: Analog and Digital Signal Processing, 1999, 46(3): 315-325.

[6] Parvizi M, Alidina K, Ei-Gamal M N A. SubmW, ultra-low-voltage, wideband low-noise amplifier design technique [J]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23(6): 1111-1122.

[7] Yoon J, Park C A. CMOS LNA using a harmonic rejection technique to enhance its linearity [J]. IEEE Microwave and Wireless Components Letters, 2014, 24(9): 605-607.
[8] WOO S, KIM W, LEE C H, et al. A wideband low-power CMOS LNA with positive-negative feedback for noise, gain, and linearity optimization [J]. IEEE Transactions on Microwave Theory and Techniques, 2012, 60(10): 3169-3178. NS M R. Design and performance analysis of a 866-MHz low-power optimized CMOS LNA for Uhfrrfid [J]. IEEE Transactions on Industrial Electronics, 2013, 60(5): 1840-1849.

[9] Li Xiangmin, Kang Zhuang. Design of a New High Performance Ultra Wide Band Low Noise Amplifier Journal of the Chinese Academy of Electronic Sciences, 2017, 12(1): 106-109.

[10] Chen Z, Zheng Y, Choong F C, et al. A low-power variable-gain amplifier with improved linearity: analysis and design [J]. IEEE Transactions on Circuits and Systems—I: Regular papers, 2012, 59(10): 2176-2185.