Research Article

Tunable First-Order Resistorless All-Pass Filter with Low Output Impedance

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This paper presents a voltage mode cascadable single active element tunable first-order all-pass filter with a single passive component. The active element used to realise the filter is a new building block termed as differential difference dual-X current conveyor with a buffered output (DD-DXCCII). The filter is thus realized with the help of a DD-DXCCII, a capacitor, and a MOS transistor. By exploiting the low output impedance, a higher order filter is also realized. Nonideal and parasitic study is also carried out on the realised filters. The proposed DD-DXCCII filters are simulated using TSMC the 0.25 \( \mu \)m technology.

1. Introduction

Analog first-order filter design using a variety of active building blocks has been the focus of research for the past several decades. Operational amplifier was the active element of choice during the earlier stages of development. Later, the advent of second generation current conveyors (CCII), differential voltage current conveyor (DVCC), current controlled current conveyor (CCCII), and dual-X current conveyor (DXCCII) signalled the era of voltage-mode and current-mode signal processing. Since then, there has been a significant amount of technical literature available on the subject. Obviously, it is not possible to attempt a thorough review of all the related works. However, a survey of some of the recently published first-order voltage mode all-pass filters (APF) is presented in this section. A variety of circuits are available based on the above-mentioned conveyors [1–22]. The filter in [1–8] is composed of more than one active element while the method proposed in [9–22] employs only a single active element and passive components. The filters in [16, 17] employ four passive components; the filter in [19] employs two to three passive components while the filters designed in [10–13, 15, 20, 21] employ three passive components. Out of these, the filters presented in [11, 20, 21] do not exhibit a low output impedance and hence fall in the category of noncascadable filters while those in [10, 12, 13, 15] have a low output impedance and are classified as cascadable filters. The filters in [1, 3, 4, 18] are resistorless circuits based on one or more active elements. A distinct advantage of the filter presented in [18] is that it employs a single active and a passive element with low output impedance.

However, none of the above-mentioned filters support tuning as a feature except the filter in [1].

The DXCCII presented in [15], even though contains a buffered output, requires an additional current source to obtain a low output impedance terminal, while, in this work, no additional current source is required. The DD-DXCCII is utilized to design a tunable voltage mode cascadable first-order filter.

The single active element all-pass filter presented in this paper exhibits the following features:

(a) single active element DD-DXCCII,
(b) single passive element,
(c) resistorless,
(d) low output impedance,
(e) tunable,
(f) no matching condition.

A detailed comparison of some of the reported single active element voltage mode filters with the proposed filter is shown in Table 1. From this table, it is clear that none of the reported filters exhibit all the above-mentioned features.
Table 1: Comparison of single active element based proposed and existing first-order circuits.

| Ref no. | Active element | No. of passive components | Resistorless | High input impedance | Low output impedance | Supply voltages | Matching condition required | Tunable | Highest operating frequency |
|---------|----------------|---------------------------|--------------|-----------------------|----------------------|----------------|----------------------------|---------|---------------------------|
| [9]     | CCII           | 5                         | No           | Yes                   | No                   | No             | Yes                        | No      | ~10 KHz                  |
| [10]    | FDCCII         | 3                         | No           | Yes                   | Yes                  | ±3.3 V         | Yes                       | Yes     | 1.59 MHz                 |
| [11]    | CCII           | 3                         | No           | Yes                   | No                   | No             | Yes                        | No      | —                         |
| [12]    | UVC            | 3                         | No           | Yes                   | Yes                  | ±2.5 V         | Yes                       | Yes     | 1.17 MHz                 |
| [13]    | CBTA/          | 3                         | No           | Yes                   | No                   | ±2.5 V         | Yes                        | No      | 119 KHz                  |
|         | CCCDBA         |                            |              |                       |                      |                |                            |         |                          |
| [14]    | DDCC           | 2                         | No           | No                    | No                   | ±2.5 V         | Yes                       | No      | 1.59 MHz                 |
| [15]    | DXCCII         | 2/3                       | No           | Yes                   | Yes                  | ±2.5 V         | No                        | No      | 25 MHz                   |
| [16]    | CCIII          | 4                         | No           | No                    | No                   | No             | Yes                       | No      | 1 KHz                    |
| [17]    | DXCCII         | 4                         | No           | Yes                   | No                   | ±1.25 V        | Yes                       | No      | 1.59 MHz                 |
| [18]    | VD-DIBA        | 1                         | Yes          | Yes                   | Yes                  | —              | No                        | No      | 318 KHz                  |
| [19]    | ICCII          | 2                         | No           | No                    | No                   | ±2.5 V         | Yes                       | Yes     | 370 KHz                  |
| [20]    | CCII           | 3                         | No           | No                    | No                   | ±2.5 V         | Yes                       | No      | 1 MHz                    |
| [21]    | CCII           | 3                         | No           | No                    | No                   | No             | Yes                       | No      | 159 KHz                  |
| [22]    | FDCCII         | 2                         | No           | Yes                   | Yes                  | ±3 V           | No                        | No      | 3.11 MHz                 |
| Proposed| DDDXCCII       | 1                         | Yes          | No                    | Yes                  | ±1.25 V        | No                        | Yes     | 4–6 MHz                  |

The rest of the paper is organized as follows. Section 2 presents a brief overview of the DD-DXCCII, with buffered output followed by the design and analysis of a new voltage-mode, first-order, all-pass filter section based on a single DD-DXCCII. In Section 3, nonideal and parasitic analysis of the proposed circuit is performed. The feature of easy cascadability is highlighted in Section 4 while Section 5 presents the results of computer simulations of the proposed circuits using the PSPICE program. Some conclusive remarks appear in Section 6.

2. Proposed First-Order All-Pass Filter

The differential difference dual-X current conveyor with buffered output has been proposed as an eight-terminal device characterized by the following port relations:

\[
\begin{bmatrix}
I_{y1} \\
I_{y2} \\
V_{xp} \\
V_{xn} \\
I_{zp} \\
I_{zn} \\
V_{wm}
\end{bmatrix} = 
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\
-1 & +1 & -1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0
\end{bmatrix} 
\begin{bmatrix}
V_{y1} \\
V_{y2} \\
V_{xp} \\
V_{zn} \\
I_{xp} \\
I_{xn} \\
V_{wm}
\end{bmatrix}.
\]

(1)

Figure 1 shows the schematic symbol of a DD-DXCCII with buffered output. The CMOS implementation of DD-DXCCII with buffered output at \(Z_n\) is shown in Figure 2.

The input side has three terminals (called \(Y_1, Y_2,\) and \(Y_3\)) and there are two \(X\)-terminals (\(X_p\) and \(X_n\)). At the output side, there are three terminals \(Z_p, Z_n,\) and \(W_n\). For the \(Z_p\) terminal, the direction and magnitude of the conveyed current are the same as those of the current flowing in the \(X_p\)-terminal whereas for the \(Z_n\)-terminal, the current is the same as in the \(X_n\)-terminal. The voltage that appears at terminal \(W_n\) is equal to the voltage at \(Z_n\).

The proposed tunable voltage-mode first-order all-pass filter section is shown in Figure 3. As can be seen, the circuit has minimal complexity and employs a single DD-DXCCII, a single capacitor, and an NMOS transistor biased in the triode region.

The transfer function of an all-pass filter can be given as

\[
T_{AP} = \frac{V_{out}}{V_{in}} = \frac{s - 2/R_M C}{s + 2/R_M C},
\]

(2)

where \(R_M\) is the resistance of the MOSFET transistor \((M)\) in Figure 3 and is given by

\[
R_M = [\mu_n C_{ox} \left(\frac{W}{L}\right)(V_C - V_T)]^{-1},
\]

(3)
\[ \mu_n, C_{ox}, V_T, W, \text{ and } L \text{ are the surface mobility, oxide capacitance, threshold voltage, channel width, and length of MOS. From (2) the pole frequency } \omega_0 \text{ can be expressed as} \]

\[ \omega_0 = \frac{2}{R_M C}. \quad (4) \]

From (4) it is clear that the pole frequency of the all-pass filter can be tuned by varying the resistance \( R_M \) of the triode MOSFET resistor \( M \). The phase angle of the all-pass filter can be expressed as

\[ \angle \phi = \pi - 2 \tan^{-1} \left( \frac{\omega CR_M}{2} \right). \quad (5) \]

\section{Nonideal Study}

\subsection{Effect of Nonideal Transfer Gain}

The port relations defining the DD-DXCCII, as given in (1), correspond to an ideal device in which the current and voltage conveying processes are deemed perfect. For a more realistic understanding of the operation of the circuit of Figure 3, the nonidealities associated with the DD-DXCCII need to be taken into consideration. The nonideal port relationship can be expressed as

\[ V_{xp} = \beta_{p1} V_{y1} - \beta_{p2} V_{y2} + \beta_{p3} V_{y3}, \]
\[ V_{xn} = \beta_{n1} V_{y1} - \beta_{n2} V_{y2} + \beta_{n3} V_{y3}, \]
\[ I_{zp} = \alpha_p I_{xp}, \quad I_{zn} = \alpha_n I_{xn}, \]
\[ V_{wn} = \gamma_n V_{zn}. \quad (6) \]

where \( \beta_{pi} (\beta_{ni}) \) is the voltage transfer gain from the \( Y_i \) port to \( X_p \) (\( X_n \) port), where \( i = 1 \) to 3, \( \alpha_p (\alpha_n) \) is the current transfer gain from the \( X_p \) port to \( Z_p \) port (\( X_n \) port to \( Z_n \) port) and \( \gamma_n \) is the voltage transfer gain from \( Z_n \) port to \( W_n \) port (ideally, these transfer gains are unity in magnitude).

Using (6) the ideal transfer functions of the AP filter section, given in (2), yield the following nonideal transfer function:

\[ T_{AP, \text{nonideal}} = \frac{V_{out}}{V_{in}} = \frac{s - (2\alpha_p \beta_3 / R_M C)}{s + (2\alpha_p \beta_3 / R_M C)}. \quad (7) \]

From (7) the nonideal pole frequency can be expressed as

\[ \omega_{0, \text{nonideal}} = \frac{2\alpha_p \beta_3}{R_M C}. \quad (8) \]

Equation (8) shows that, due to nonideal voltage and current transfer gain, the pole frequency does get affected. The sensitivity analysis shows that the pole frequency due to the nonidealities is unity in magnitude.

\subsection{Effect of Parasitics}

The parasitics associated with the actual DD-DXCCII are the same as those of the DXCCII [23]. In Figure 3, \( Y_1 \) and \( Z_p \) port parasitics are in parallel; that is, \( R_{y1}/C_{y1}/C_{z1}/V_{y3} \), and \( Z_n \) port resistances and capacitances are also in parallel, that is, \( R_{y3}/C_{y3}/C_{z3}/V_{zn} \). Also, the \( X_p \) and \( X_n \) parasitics, that is, \( R_{xn} \) and \( R_{xn} \), merge with the resistance of triode MOSFET. The proposed circuit is reanalyzed by taking into account the above parasitics.
The nonideal transfer gain due to parasitics then becomes

\[ T_{\text{AP,parasitic}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \left( \frac{C + C'}{C} \right) \left( \frac{s - 2/R_M (C + C')}{s + 2/R_M C} \right), \]  

(9)

where \( C' = C_{y1}/C_{xp} \) and since \( C \gg C' \), the transfer function reduces to

\[ T_{\text{AP,parasitic}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \left( \frac{s - 2/R_M C}{s + 2/R_M C} \right). \]  

(10)

From (10) it is clear that the pole frequency is unaffected in the presence of parasitics.

### 4. Higher Order All-Pass Filter

It is well known that higher order filters exhibit a larger rate of phase change at constant magnitude when compared to a first-order filter. They can also be used as a group delay equalizer in video and communication applications. These features are the motivating factor behind realizing a higher order filter in this work. The proposed \( n \)th order APF filter is presented in Figure 4 which is obtained by cascading \( n \)-stages of the first-order filter described in Figure 3. The proposed filter employs \( n \)-stages of DD-DXCCII and \( n \)-capacitors and MOS resistors operating in the triode region.

Analysis of the above circuit yields the following transfer function:

\[ T_{\text{AP,nth order}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \left( \frac{s - 2/R_M C_1}{s + 2/R_M C_1} \right) \times \left( \frac{s - 2/R_M C_2}{s + 2/R_M C_2} \right) \times \cdots \times \left( \frac{s - 2/R_M C_n}{s + 2/R_M C_n} \right). \]  

(11)

From (11) the pole frequency can be expressed as

\[ \omega_0,\text{nth order} = \left( \frac{2^n}{(R_{M1} \cdot R_{M2} \cdots R_{Mn}) \cdot (C_{M1} \cdot C_{M2} \cdots C_{Mn})} \right)^{1/n}. \]  

(12)

### 5. Design and Verification

The performance of the first-order all-pass shown in Figure 3 was verified using PSPICE program. Supply voltages were kept at \( \pm 1.25 \) V. The proposed filter was designed with \( C = 10 \) pF and gate control voltages are \( V_C = 0.8 \) V, 1.0 V, and 1.2 V. The gain and phase plot is shown in Figure 5 which shows the variation in pole frequency at different control words. As can be seen, the pole frequency is varied from 4 MHz, 5 MHz, and 6 MHz at \( V_C = 0.8 \) V, 1.0 V, and 1.2 V, respectively. The time domain response of the proposed all-pass filter as shown in Figure 6 is obtained by applying a sine wave of 80 mV peak-to-peak amplitude at 6 MHz. The output is 88.9° phases shifted, which corresponds well with the theoretical value of 90°. The total harmonics distortion was found to be 1% at pole frequency of 6 MHz. The Fourier spectrum of input and output waveform is also shown in Figure 7.

The circuit proposed in Figure 4 is verified for a third-order filter; that is, \( n = 3 \). The filter was designed at \( C = 10 \) pF at different gate control voltages of the MOS transistor; that is, \( V_C = 0.8 \) V, 1.0 V, and 1.2 V. Simulated gain and phase response at different pole frequencies is shown in Figure 8. The pole frequencies are found to be 4 MHz, 5 MHz, and 6 MHz at a phase of −90°. The variation in pole frequency is obtained by varying the control word. The total harmonics distortion (THD) variation of first- and third-order filter is shown in Figure 9, which shows that the THD variation is around 3% up to 300 mV of the variation in the input signal amplitude.
6. Conclusion

In this paper a new active element, that is, DD-DXCCII with buffered output, is presented. By employing DD-DXCCII a new voltage mode tunable resistorless all-pass filter using single passive element is realized. The proposed filter does not require any matching condition. The filter has low output impedance which is elaborated by designing a third-order filter. Nonidealities of the active element along with parasitics are also considered, so as to evaluate the proposed filter. The filter reported in [23, 24] is a current mode all-pass filter while the filter presented in this work is a voltage mode all-pass filter.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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References

[1] T. Tsukutani, H. Tsunetsugu, Y. Sumi, and N. Yabuki, “Electronically tunable first-order all-pass circuit employing DVCC and OTA,” International Journal of Electronics, vol. 97, no. 3, pp. 285–293, 2010.

[2] M. A. Ibrahim, S. Minaei, and E. Yuce, “All-pass sections with rich cascadability and IC realization suitability,” International Journal of Circuit Theory and Applications, vol. 140, pp. 477–488, 2012.

[3] S. Maheshwari, “A canonical voltage-controlled VM-APS with grounded capacitor,” Circuits, Systems, and Signal Processing, vol. 27, no. 1, pp. 123–132, 2008.

[4] S. Minaei and O. Cicekoglu, “A Resistorless realization of the first-order all-pass filter,” International Journal of Electronics, vol. 93, no. 3, pp. 177–183, 2006.

[5] S. Minaei and E. Yuce, “Novel voltage-mode all-pass filter based on using DVCCs,” Circuits, Systems, and Signal Processing, vol. 29, no. 3, pp. 391–402, 2010.
[6] S. Maheshwari, “High input impedance voltage-mode first-order all-pass sections,” *International Journal of Circuit Theory and Applications*, vol. 36, pp. 511–522, 2008.

[7] S. Maheshwari, “High input impedance VM-APSs with grounded passive elements,” *IET Circuits, Devices and Systems*, vol. 1, no. 1, pp. 72–78, 2007.

[8] S. Maheshwari, J. Mohan, and D. S. Chauhan, “Novel voltage-mode cascadable all-pass sections employing grounded passive components,” *Journal of Circuits, Systems, and Computers*, vol. 22, Article ID 1250065, 2013.

[9] A. M. Soliman, “Generation of current conveyor-based all-pass filters from op amp-based circuits,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 4, pp. 324–330, 1997.

[10] J. Mohan, S. Maheshwari, and D. S. Chauhan, “Voltage mode cascadable all-pass sections using single active element and grounded passive components,” *Circuits and Systems*, vol. 1, pp. 5–11, 2010.

[11] K. Pal and S. Rana, “Some new first-order all-pass realizations using CCII,” *Active and Passive Electronic Components*, vol. 27, no. 2, pp. 91–94, 2004.

[12] N. Herencsar, J. Koton, J. Jerabek, K. Vrba, and O. Cicekoglu, “Voltage-mode all-pass filters using universal voltage conveyor and MOSFET-based electronic Resistors,” *Radioengineering*, vol. 20, no. 1, pp. 10–18, 2011.

[13] S. Maheshwari, “Voltage-mode all-pass filters including minimum component count circuits,” *Active and Passive Electronic Components*, vol. 2007, Article ID 79159, 5 pages, 2007.

[14] M. A. Ibrahim, H. Kuntman, and O. Cicekoglu, “First-order all-pass filter canonical in the number of resistors and capacitors employing a single DDCC,” *Circuits, Systems, and Signal Processing*, vol. 22, no. 5, pp. 525–536, 2003.

[15] S. Maheshwari and B. Chaturvedi, “High-input low-output impedance all-pass filters using one active element,” *IET Circuits, Devices and Systems*, vol. 6, no. 2, pp. 103–110, 2012.

[16] S. Maheshwari and I. A. Khan, “Novel first order all-pass sections using a single CCII,” *International Journal of Electronics*, vol. 88, no. 7, pp. 773–778, 2001.

[17] S. Minaei and E. Yuce, “Unity/variable-gain voltage-mode/current-mode first-order all-pass filters using single dual-X second-generation current conveyor,” *IETE Journal of Research*, vol. 56, no. 6, pp. 305–312, 2010.

[18] D. Biolek and V. Biolkova, “First-order voltage-mode all-pass filter employing one active element and one grounded capacitor,” *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 123–129, 2010.

[19] M. A. Ibrahim, H. Kuntman, S. Ozcan, O. Suvak, and O. Cicekoglu, “New first-order inverting-type second-generation current conveyor-based all-pass sections including canonical forms,” *Electrical Engineering*, vol. 86, no. 5, pp. 299–301, 2004.

[20] B. Metin and O. Cicekoglu, “Component reduced all-pass filter with a grounded capacitor and high-impedance input,” *International Journal of Electronics*, vol. 96, no. 5, pp. 445–455, 2009.

[21] A. Toker, S. Özcan, H. Kuntman, and O. Çiçekoglu, “Supplementary all-pass sections with reduced number of passive elements using a single current conveyor,” *International Journal of Electronics*, vol. 88, no. 9, pp. 969–976, 2001.

[22] S. Maheshwari, J. Mohan, and D. S. Chauhan, “Voltage-mode cascadable all-pass sections with two grounded passive components and one active element,” *IET Circuits, Devices and Systems*, vol. 4, no. 2, pp. 113–122, 2010.