The Processing Using Memory Paradigm:
In-DRAM Bulk Copy, Initialization, Bitwise AND and OR

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Abstract

In existing systems, the off-chip memory interface allows the memory controller to perform only read or write operations. Therefore, to perform any operation, the processor must first read the source data and then write the result back to memory after performing the operation. This approach consumes high latency, bandwidth, and energy for operations that work on a large amount of data. Several works have proposed techniques to process data near memory by adding a small amount of compute logic closer to the main memory chips. In this article, we describe two techniques proposed by recent works that take this approach of processing in memory further by exploiting the underlying operation of the main memory technology to perform more complex tasks. First, we describe RowClone, a mechanism that exploits DRAM technology to perform bulk copy and initialization operations completely inside main memory. We then describe a complementary work that uses DRAM to perform bulk bitwise AND and OR operations inside main memory. These two techniques significantly improve the performance and energy efficiency of the respective operations.

1 Introduction

In modern systems, the channel that connects the processor and off-chip main memory is a critical bottleneck for both performance and energy-efficiency. First, the channel has limited data bandwidth. Increasing this available bandwidth requires increasing the number of channels or the width of each channel or the frequency of the channel. All these approaches significantly increase the cost of the system and are not scalable. Second, a significant fraction of the energy consumed in performing an operation is spent on moving data over the off-chip memory channel [30].

To address this problem, many prior and recent works [11, 12, 13, 15, 40, 42, 44, 45, 47, 48, 51, 52, 54, 56, 57, 79, 85, 95, 103, 105, 114, 143, 149] have proposed techniques to process data near memory, an approach widely referred to as Processing in Memory or PiM. The idea behind PiM is to add a small amount of compute logic close to the memory chips and use that logic to perform simple yet bandwidth-intensive and/or latency-sensitive operations. The premise is that being close to the memory chips, the PiM
module will have much higher bandwidth and lower latency to memory than the regular processor. Consequently, PiM can 1) perform bandwidth-intensive and latency-sensitive operations faster and 2) reduce the off-chip memory bandwidth requirements of such operations. As a result, PiM significantly improves both overall system performance and energy efficiency.

In this article, we focus our attention on two works that push the notion of processing in memory deeper by exploiting the underlying operation of the main memory technology to perform more complex tasks. We will refer to this approach as Processing using Memory or PuM. Unlike PiM, which adds new logic structures near memory to perform computation, the key idea behind PuM is to exploit some of the peripheral structures already existing inside memory devices (with minimal changes) to perform other tasks.

The first work that we will discuss in this article is RowClone [115], a mechanism that exploits DRAM technology to perform bulk data copy and initialization completely inside DRAM. Such bulk copy and initialization operations are triggered by many applications (e.g., bulk zeroing) and system-level functions (e.g., page copy operations). Despite the fact that these operations require no computation, existing system must necessarily read and write the required data over the main memory channel. In fact, even with a high-speed memory bus (DDR4-2133) a simple 4 KB copy operation can take close to half a micro second for just the data transfers on the memory channel. By performing such operations completely inside main memory, RowClone eliminates the need for any data transfer on the memory channel, thereby significantly improving performance and energy-efficiency.

The second work that we will discuss in this article is a mechanism to perform bulk bitwise AND and OR operations completely inside DRAM [114]. Bitwise operations are an important component of modern day programming. Many applications (e.g., bitmap indices) rely on bitwise operations on large bitvectors to achieve high performance. Similar to bulk copy or initialization, the throughput of bulk bitwise operations in existing systems is also limited by the available memory bandwidth. The In-DRAM AND-OR mechanism (IDAO) avoids the need to transfer large amounts of data on the memory channel to perform these operations. Similar to RowClone, IDAO enables an order of magnitude improvement in the performance of bulk bitwise operations. We will describe these two works in detail in this article.

In this article, we will discuss the following things.

- We motivate the need for reducing data movement and how processing near memory helps in achieving that goal (Section 2). We will briefly describe a set of recent works that have pushed the idea of processing near memory deeper by using the underlying memory technologies (e.g., DRAM, STT-MRAM, PCM) to perform tasks more complex than just storing data (Section 3).

- As the major focus of this article is on the PuM works that build on DRAM, we provide a brief background on modern DRAM organization and operation that is sufficient to understand the mechanisms (Section 4).
• We describe the two mechanisms, RowClone (in-DRAM bulk copy and initialization) and In-DRAM-AND-OR (in-DRAM bulk bitwise AND and OR) in detail in Sections 5 and 6, respectively.

• We describe a number of applications for the two mechanisms and quantitative evaluations showing that they improve performance and energy-efficiency compared to existing systems.

2 Processing in Memory

Data movement contributes a major fraction of the execution time and energy consumption of many programs. The farther the data is from the processing engine (e.g., CPU), the more the contribution of data movement towards execution time and energy consumption. While most programs aim to keep their active working set as close to the processing engine as possible (say the L1 cache), for applications with working sets larger than the on-chip cache size, the data typically resides in main memory.

Unfortunately, main memory latency is not scaling commensurately with the remaining resources in the system, namely, the compute power and memory capacity. As a result, the performance of most large-working-set applications is limited by main memory latency and/or bandwidth. For instance, just transferring a single page (4 KB) of data from DRAM can consume between a quarter and half a microsecond even with high speed memory interfaces (DDR4-2133 [65]). During this time, the processor can potentially execute hundreds to thousands of instructions. With respect to energy, while performing a 64-bit double precision floating point operation typically consumes few tens of pico joules, accessing 64-bits of data from off-chip DRAM consumes few tens of nano joules (3 orders of magnitude more energy) [30].

One of the solutions to address this problem is to add support to process data closer to memory, especially for operations that access large amounts of data. This approach is generally referred to as Processing in Memory (PiM) or Near Data Processing. The high-level idea behind PiM is to add a small piece of compute logic closer to memory that has much higher bandwidth to memory than the main processor. Prior research has proposed two broad ways of implementing PiM: 1) Integrating processing logic into the memory chips, and 2) using 3D-stacked memory architectures.

2.1 Integrating Processing Logic in Memory

Many works (e.g., Logic-in-Memory Computer [125], NON-VON Database Machine [120], EXECUBE [79], Terasys [47], Intelligent RAM [105], Active Pages [103], FlexRAM [43, 68], Computational RAM [40], DIVA [35] ) have proposed mechanisms and models to add processing logic close to memory. The idea is to integrate memory and CPU on the same chip by designing the CPU using the memory process technology. The reduced data movement allows these approaches to enable low-latency, high-bandwidth, and low-energy data communication. However, they suffer from two key shortcomings.
First, this approach of integrating processor on the same chip as memory greatly increases the overall cost of the system. Second, DRAM vendors use a high-density process to minimize cost-per-bit. Unfortunately, high-density DRAM process is not suitable for building high-speed logic \[105\]. As a result, this approach is not suitable for building a general purpose processor near memory, at least with modern logic and high-density DRAM technologies.

### 2.2 3D-Stacked DRAM Architectures

Some recent DRAM architectures \[3, 62, 85, 92\] use 3D-stacking technology to stack multiple DRAM chips on top of the processor chip or a separate logic layer. These architectures offer much higher bandwidth to the logic layer compared to traditional off-chip interfaces. This enables an opportunity to offload some computation to the logic layer, thereby improving performance. In fact, many recent works have proposed mechanisms to improve and exploit such architectures (e.g., \[11, 12, 13, 15, 17, 42, 44, 45, 48, 51, 56, 57, 85, 95, 100, 131, 143, 149\]). 3D-stacking enables much higher bandwidth between the logic layer and the memory chips, compared to traditional architectures. However, 3D-stacked architectures still require data to be transferred outside the DRAM chip, and hence can be bandwidth-limited. In addition, thermal factors constrain the number of chips that can be stacked, thereby limiting the memory capacity. As a result, multiple 3D-stacked DRAMs are required to scale to large workloads. Despite these limitations, this approach seems to be the most viable way of implementing processing in memory in modern systems.

### 3 Processing Using Memory

In this article, we introduce a new class of work that pushes the idea of PiM further by exploiting the underlying memory operation to perform more complex operations than just data storage. We refer to this class of works as *Processing using Memory (PuM)*.

Reducing cost-per-bit is a first order design constraint for most memory technologies. As a result, the memory cells are small. Therefore, most memory devices use significant amount of sensing and peripheral logic to extract data from the memory cells. The key idea behind PuM is to use these logic structures and their operation to perform some additional tasks.

It is clear that unlike PiM, which can potentially be designed to perform any task, PuM can only enable some limited functionality. However, for tasks that can be performed by PuM, PuM has two advantages over PiM. First, as PuM exploits the underlying operation of memory, it incurs much lower cost than PiM. Second, unlike PiM, PuM does not have to read any data out of the memory chips. As a result, the PuM approach is possibly the most energy efficient way of performing the respective operations.

Building on top of DRAM, which is the technology ubiquitously used to build main memory in modern systems, two recent works take the PuM approach to accelerate certain important primitives: 1) RowClone \[115\], which performs bulk copy and initialization operations completely inside DRAM, and 2) IDAO \[114\], which performs bulk bitwise AND/OR operations completely inside DRAM. Both these works exploit the operation of the DRAM
sense amplifier and the internal organization of DRAM to perform the respective operations. We will discuss these two works in significant detail in this article.

Similar to these works, there are others that build on various other memory technologies. Pinatubo \citep{89} exploits phase change memory (PCM) \citep{81, 82, 83, 107, 109, 138, 148} architecture to perform bitwise operations efficiently inside PCM. Pinatubo enhances the PCM sense amplifiers to sense fine grained differences in resistance and use this to perform bitwise operations on multiple cells connected to the same sense amplifier. As we will describe in this article, bitwise operations are critical for many important data structures like bitmap indices. Kang et al. \citep{67} propose a mechanism to exploit SRAM architecture to accelerate the primitive “sum of absolute differences”. ISAAC \citep{119} is a mechanism to accelerate vector dot product operations using a memristor array. ISAAC uses the crossbar structure of a memristor array and its analog operation to efficiently perform dot products. These operations are heavily used in many important applications including deep neural networks.

In the subsequent sections, we will focus our attention on RowClone and IDAO. We will first provide the necessary background on DRAM design and then describe how these mechanisms work.

4 Background on DRAM

In this section, we describe the necessary background to modern DRAM architecture and its implementation. While we focus our attention primarily on commodity DRAM design (i.e., the DDRx interface), most DRAM architectures use very similar design approaches and vary only in higher-level design choices. As a result, the mechanisms we describe in the subsequent sections can be extended to any DRAM architecture. There has been significant recent research in DRAM architectures and the interested reader can find details about various aspects of DRAM in multiple recent publications \citep{21, 24, 53, 70, 71, 77, 78, 80, 87, 90, 91, 106, 116}.

4.1 High-level Organization of the Memory System

Figure 1 shows the organization of the memory subsystem in a modern system. At a high level, each processor chip consists of one or more off-chip memory channels. Each memory channel consists of its own set of command, address, and data buses. Depending on the design of the processor, there can be either an independent memory controller for each memory channel or a single memory controller for all memory channels. All modules connected to a channel share the buses of the channel. Each module consists of many DRAM devices (or chips). Most of this section is dedicated to describing the design of a modern DRAM chip. In Section 4.3, we present more details of the module organization of commodity DRAM.
4.2 DRAM Chip

A modern DRAM chip consists of a hierarchy of structures: DRAM cells, tiles/MATs, subarrays, and banks. In this section, we describe the design of a modern DRAM chip in a bottom-up fashion, starting from a single DRAM cell and its operation.

4.2.1 DRAM Cell and Sense Amplifier

At the lowest level, DRAM technology uses capacitors to store information. Specifically, it uses the two extreme states of a capacitor, namely, the empty and the fully charged states to store a single bit of information. For instance, an empty capacitor can denote a logical value of 0, and a fully charged capacitor can denote a logical value of 1. Figure 2 shows the two extreme states of a capacitor.

![Figure 2: Two states of a DRAM cell](image)

Unfortunately, the capacitors used for DRAM chips are small, and will get smaller with each new generation. As a result, the amount of charge that can be stored in the capacitor, and hence the difference between the two states is also very small. In addition, the capacitor can potentially lose its state after it is accessed. Therefore, to extract the state of the capacitor, DRAM manufacturers use a component called sense amplifier.

Figure 3 shows a sense amplifier. A sense amplifier contains two inverters which are connected together such that the output of one inverter is connected to the input of the other and vice versa. The sense amplifier also has an enable signal that determines if the inverters are active. When enabled, the sense amplifier has two stable states, as shown in Figure 4. In both these stable states, each inverter takes a logical value and feeds the other inverter with the negated input.

Figure 5 shows the operation of the sense amplifier from a disabled state. In the initial disabled state, we assume that the voltage level of the top terminal (V_a) is higher than that
of the bottom terminal ($V_b$). When the sense amplifier is enabled in this state, it *senses* the difference between the two terminals and *amplifies* the difference until it reaches one of the stable states (hence the name “sense amplifier”).

![Figure 3: Sense amplifier](image1)

![Figure 4: Stable states of a sense amplifier](image2)

![Figure 5: Operation of the sense amplifier](image3)

### 4.2.2 DRAM Cell Operation: The ACTIVATE-PRECHARGE cycle

DRAM technology uses a simple mechanism that converts the logical state of a capacitor into a logical state of the sense amplifier. Data can then be accessed from the sense amplifier (since it is in a stable state). Figure 6 shows the connection between a DRAM cell and the sense amplifier and the sequence of states involved in converting the cell state to the sense amplifier state.

As shown in the figure (state 1), the capacitor is connected to an access transistor that acts as a switch between the capacitor and the sense amplifier. The transistor is controlled by a wire called *wordline*. The wire that connects the transistor to the top end of the sense amplifier is called *bitline*. In the initial state 1, the wordline is lowered, the sense amplifier is disabled and both ends of the sense amplifier are maintained at a voltage level of $\frac{1}{2}V_{DD}$. We assume that the capacitor is initially fully charged (the operation is similar if the capacitor was empty). This state is referred to as the *precharged* state. An access to the cell is triggered by a command called*ACTIVATE*. Upon receiving an *ACTIVATE*, the corresponding wordline is first raised (state 2). This connects the capacitor to the bitline. In the ensuing phase called *charge sharing* (state 3), charge flows from the capacitor to the bitline, raising the voltage level on the bitline (top end of the sense amplifier) to $\frac{1}{2}V_{DD} + \delta$. After charge sharing, the sense amplifier is enabled (state 4). The sense amplifier detects the difference in voltage levels between its two ends and amplifies the deviation, till it reaches the stable
state where the top end is at $V_{DD}$ (state 3). Since the capacitor is still connected to the bitline, the charge on the capacitor is also fully restored. We shortly describe how the data can be accessed from the sense amplifier. However, once the access to the cell is complete, the cell is taken back to the original precharged state using the command called PRECHARGE. Upon receiving a PRECHARGE, the wordline is first lowered, thereby disconnecting the cell from the sense amplifier. Then, the two ends of the sense amplifier are driven to $\frac{1}{2}V_{DD}$ using a precharge unit (not shown in the figure for brevity).

4.2.3 DRAM MAT/Tile: The Open Bitline Architecture

A major goal of DRAM manufacturers is to maximize the density of the DRAM chips while adhering to certain latency constraints (described in Section 4.2.6). There are two costly components in the setup described in the previous section. The first component is the sense amplifier itself. Each sense amplifier is around two orders of magnitude larger than a single DRAM cell [87, 108]. Second, the state of the wordline is a function of the address that is currently being accessed. The logic that is necessary to implement this function (for each cell) is expensive.

In order to reduce the overall cost of these two components, they are shared by many DRAM cells. Specifically, each sense amplifier is shared by a column of DRAM cells. In other words, all the cells in a single column are connected to the same bitline. Similarly, each wordline is shared by a row of DRAM cells. Together, this organization consists of a
2-D array of DRAM cells connected to a row of sense amplifiers and a column of wordline drivers. Figure 7 shows this organization with a $4 \times 4$ 2-D array.

To further reduce the overall cost of the sense amplifiers and the wordline driver, modern DRAM chips use an architecture called the *open bitline architecture*. This architecture exploits two observations. First, the sense amplifier is wider than the DRAM cells. This difference in width results in a white space near each column of cells. Second, the sense amplifier is symmetric. Therefore, cells can also be connected to the bottom part of the sense amplifier. Putting together these two observations, we can pack twice as many cells in the same area using the open bitline architecture, as shown in Figure 8.

![Figure 7: A 2-D array of DRAM cells](image)

![Figure 8: A DRAM MAT/Tile: The open bitline architecture](image)
As shown in the figure, a 2-D array of DRAM cells is connected to two rows of sense amplifiers: one on the top and one on the bottom of the array. While all the cells in a given row share a common wordline, half the cells in each row are connected to the top row of sense amplifiers and the remaining half of the cells are connected to the bottom row of sense amplifiers. This tightly packed structure is called a DRAM MAT/Tile \[77, 132, 144\]. In a modern DRAM chip, each MAT typically is a 512 \times 512 or 1024 \times 1024 array. Multiple MATs are grouped together to form a larger structure called a DRAM bank, which we describe next.

### 4.2.4 DRAM Bank

In most modern commodity DRAM interfaces \[64, 65\], a DRAM bank is the smallest structure visible to the memory controller. All commands related to data access are directed to a specific bank. Logically, each DRAM bank is a large monolithic structure with a 2-D array of DRAM cells connected to a single set of sense amplifiers (also referred to as a row buffer). For example, in a 2Gb DRAM chip with 8 banks, each bank has \(2^{15}\) rows and each logical row has 8192 DRAM cells. Figure 9 shows this logical view of a bank.

In addition to the MAT, the array of sense amplifiers, and the wordline driver, each bank also consists of some peripheral structures to decode DRAM commands and addresses, and manage the input/output to the DRAM bank. Specifically, each bank has a row decoder to decode the row address of row-level commands (e.g., ACTIVATE). Each data access command (READ and WRITE) accesses only a part of a DRAM row. Such individual parts are referred to as columns. With each data access command, the address of the column to be accessed is provided. This address is decoded by the column selection logic. Depending on which column is selected, the corresponding piece of data is communicated between the sense amplifiers.
and the bank I/O logic. The bank I/O logic in turn acts as an interface between the DRAM bank and the chip-level I/O logic.

Although the bank can logically be viewed as a single MAT, building a single MAT of a very large dimension is practically not feasible as it will require very long bitlines and wordlines. Therefore, each bank is physically implemented as a 2-D array of DRAM MATs. Figure 10 shows a physical implementation of the DRAM bank with 4 MATs arranged in 2 × 2 array. As shown in the figure, the output of the global row decoder is sent to each row of MATs. The bank I/O logic, also known as the global sense amplifiers, are connected to all the MATs through a set of global bitlines. As shown in the figure, each vertical collection of MATs consists of its own columns selection logic and global bitlines. In a real DRAM chip, the global bitlines run on top of the MATs in a separate metal layer. One implication of this division is that the data accessed by any command is split equally across all the MATs in a single row of MATs.

Figure 10: DRAM Bank: Physical implementation. In a real chip, the global bitlines run on top of the MATs in a separate metal layer. (components in figure are not to scale)

Figure 11 shows the zoomed-in version of a DRAM MAT with the surrounding peripheral logic. Specifically, the figure shows how each column selection line selects specific sense amplifiers from a MAT and connects them to the global bitlines. It should be noted that the width of the global bitlines for each MAT (typically 8/16) is much smaller than that of the width of the MAT (typically 512/1024). This is because the global bitlines span a much longer distance and hence have to be thicker to ensure integrity.

Each DRAM chip consist of multiple banks as shown in Figure 12. All the banks share the chip’s internal command, address, and data buses. As mentioned before, each bank operates mostly independently (except for operations that involve the shared buses). The
chip I/O manages the transfer of data to and from the chip’s internal bus to the memory channel. The width of the chip output (typically 8 bits) is much smaller than the output width of each bank (typically 64 bits). Any piece of data accessed from a DRAM bank is first buffered at the chip I/O and sent out on the memory bus 8 bits at a time. With the DDR (double data rate) technology, 8 bits are sent out each half cycle. Therefore, it takes 4 cycles to transfer 64 bits of data from a DRAM chip I/O on to the memory channel.

4.2.5 DRAM Commands: Accessing Data from a DRAM Chip

To access a piece of data from a DRAM chip, the memory controller must first identify the location of the data: the bank ID \( B \), the row address \( R \) within the bank, and the column address \( C \) within the row. After identifying these pieces of information, accessing the data involves three steps.

The first step is to issue a **PRECHARGE** to the bank \( B \). This step prepares the bank for a data access by ensuring that all the sense amplifiers are in the **precharged** state (Figure 6 state 1). No wordline within the bank is raised in this state.
The second step is to activate the row $R$ that contains the data. This step is triggered by issuing a `ACTIVATE` to bank $B$ with row address $R$. Upon receiving this command, the corresponding bank feeds its global row decoder with the input $R$. The global row decoder logic then raises the wordline of the DRAM row corresponding to the address $R$ and enables the sense amplifiers connected to that row. This triggers the DRAM cell operation described in Section 4.2.2. At the end of the activate operation the data from the entire row of DRAM cells is copied to the corresponding array of sense amplifiers.

Finally, the third step is to access the data from the required column. This is done by issuing a `READ` or `WRITE` command to the bank with the column address $C$. Upon receiving a `READ` or `WRITE` command, the corresponding address is fed to the column selection logic. The column selection logic then raises the column selection lines (Figure 11) corresponding to address $C$, thereby connecting those sense amplifiers to the global sense amplifiers through the global bitlines. For a read access, the global sense amplifiers sense the data from the MAT’s local sense amplifiers and transfer that data to the chip’s internal bus. For a write access, the global sense amplifiers read the data from the chip’s internal bus and force the MAT’s local sense amplifiers to the appropriate state.

Not all data accesses require all three steps. Specifically, if the row to be accessed is already activated in the corresponding bank, then the first two steps can be skipped and the data can be directly accessed by issuing a `READ` or `WRITE` to the bank. For this reason, the array of sense amplifiers are also referred to as a `row buffer`, and such an access that skips the first two steps is called a `row buffer hit`. Similarly, if the bank is already in the precharged state, then the first step can be skipped. Such an access is referred to as a `row buffer miss`. Finally, if a different row is activated within the bank, then all three steps have to be performed. Such an access is referred to as a `row buffer conflict`.

### 4.2.6 DRAM Timing Constraints

Different operations within DRAM consume different amounts of time. Therefore, after issuing a command, the memory controller must wait for a sufficient amount of time before it can issue the next command. Such wait times are managed by what are called the `timing constraints`. Timing constraints essentially dictate the minimum amount of time between two commands issued to the same bank/rank/channel. Table 1 describes some key timing constraints along with their values for the DDR3-1600 interface.

### 4.3 DRAM Module

As mentioned before, each `READ` or `WRITE` command for a single DRAM chip typically involves only 64 bits. In order to achieve high memory bandwidth, commodity DRAM modules group several DRAM chips (typically 4 or 8) together to form a `rank` of DRAM chips. The idea is to connect all chips of a single rank to the same command and address buses, while providing each chip with an independent data bus. In effect, all the chips within a rank receive the same commands with same addresses, making the rank a logically wide DRAM chip.
| Name       | Constraint | Description                                                                 | Value (ns) |
|------------|------------|-----------------------------------------------------------------------------|------------|
| tRAS       | ACTIVATE → PRECHARGE | Time taken to complete a row activation operation in a bank                  | 35         |
| tRCD       | ACTIVATE → READ/WRITE | Time between an activate command and column command to a bank               | 15         |
| tRP        | PRECHARGE → ACTIVATE  | Time taken to complete a precharge operation in a bank                      | 15         |
| tWR        | WRITE → PRECHARGE   | Time taken to ensure that data is safely written to the DRAM cells after a write operation (write recovery) | 15         |

Table 1: Key DRAM timing constraints with their values for DDR3-1600

Figure 13 shows the logical organization of a DRAM rank. Most commodity DRAM ranks consist of 8 chips. Therefore, each READ or WRITE command accesses 64 bytes of data, the typical cache line size in most processors.

![Figure 13: Organization of a DRAM rank](image)

5 RowClone

In this section, we present RowClone [115], a mechanism that can perform bulk copy and initialization operations completely inside DRAM. This approach obviates the need to transfer large quantities of data on the memory channel, thereby significantly improving the efficiency of a bulk copy operation. As bulk data initialization (specifically bulk zeroing) can be viewed as a special case of a bulk copy operation, RowClone can be easily extended to perform such bulk initialization operations with high efficiency.

RowClone consists of two independent mechanisms that exploit several observations about DRAM organization and operation. The first mechanism, called the Fast Parallel Mode (FPM), efficiently copies data between two rows of DRAM cells that share the same
set of sense amplifiers (i.e., two rows within the same subarray). The second mechanism, called the *Pipelined Serial Mode*, efficiently copies cache lines between two banks within a module in a pipelined manner. Although not as fast as FPM, PSM has fewer constraints and hence is more generally applicable. We now describe these two mechanisms in detail.

### 5.1 Fast-Parallel Mode

The Fast Parallel Mode (FPM) is based on the following three observations about DRAM.

1. In a commodity DRAM module, each `ACTIVATE` command transfers data from a large number of DRAM cells (multiple kilo-bytes) to the corresponding array of sense amplifiers (Section 4.3).

2. Several rows of DRAM cells share the same set of sense amplifiers (Section 4.2.3).

3. A DRAM cell is not strong enough to flip the state of the sense amplifier from one stable state to another stable state. In other words, if a cell is connected to an already activated sense amplifier (or bitline), then the data of the cell gets overwritten with the data on the sense amplifier.

While the first two observations are direct implications from the design of commodity DRAM, the third observation exploits the fact that DRAM cells can cause only a small perturbation on the bitline voltage. Figure 14 pictorially shows how this observation can be used to copy data between two cells that share a sense amplifier.

![Figure 14: RowClone: Fast Parallel Mode](image)

The figure shows two cells (`src` and `dst`) connected to a single sense amplifier. In the initial state, we assume that `src` is fully charged and `dst` is fully empty, and the sense amplifier is in the precharged state (1). In this state, FPM issues an `ACTIVATE` to `src`. At the end of the activation operation, the sense amplifier moves to a stable state where the bitline is at a voltage level of $V_{DD}$ and the charge in `src` is fully restored (2). FPM follows this operation with an `ACTIVATE` to `dst`, without an intervening `PRECHARGE`. This operation lowers the wordline corresponding to `src` and raises the wordline of `dst`, connecting `dst` to the bitline. Since the bitline is already fully activated, even though `dst` is initially empty,
the perturbation caused by the cell is not sufficient to flip the state of the bitline. As a result, the sense amplifier continues to drive the bitline to $V_{DD}$, thereby pushing $dst$ to a fully charged state ($\bar{0}$).

It can be shown that regardless of the initial state of $src$ and $dst$, the above operation copies the data from $src$ to $dst$. Given that each ACTIVATE operates on an entire row of DRAM cells, the above operation can copy multiple kilo bytes of data with just two back-to-back ACTIVATE operations.

Unfortunately, modern DRAM chips do not allow another ACTIVATE to an already activated bank – the expected result of such an action is undefined. This is because a modern DRAM chip allows at most one row (subarray) within each bank to be activated. If a bank that already has a row (subarray) activated receives an ACTIVATE to a different subarray, the currently activated subarray must first be precharged [77]. Some DRAM manufacturers design their chips to drop back-to-back ACTIVATEs to the same bank.

To support FPM, RowClone changes the way a DRAM chip handles back-to-back ACTIVATEs to the same bank. When an already activated bank receives an ACTIVATE to a row, the chip allows the command to proceed if and only if the command is to a row that belongs to the currently activated subarray. If the row does not belong to the currently activated subarray, then the chip takes the action it normally does with back-to-back ACTIVATEs—e.g., drop it. Since the logic to determine the subarray corresponding to a row address is already present in today’s chips, implementing FPM only requires a comparison to check if the row address of an ACTIVATE belongs to the currently activated subarray, the cost of which is almost negligible.

Summary. To copy data from $src$ to $dst$ within the same subarray, FPM first issues an ACTIVATE to $src$. This copies the data from $src$ to the subarray row buffer. FPM then issues an ACTIVATE to $dst$. This modifies the input to the subarray row-decoder from $src$ to $dst$ and connects the cells of $dst$ row to the row buffer. This, in effect, copies the data from the sense amplifiers to the destination row. With these two steps, FPM can copy a 4KB page of data 12.0x faster and with 74.4x less energy than an existing system (we describe the methodology in Section 8.1).

Limitations. FPM has two constraints that limit its general applicability. First, it requires the source and destination rows to be within the same subarray (i.e., share the same set of sense amplifiers). Second, it cannot partially copy data from one row to another. Despite these limitations, FPM can be immediately applied to today’s systems to accelerate two commonly used primitives in modern systems — Copy-on-Write and Bulk Zeroing. In the following section, we describe the second mode of RowClone – the Pipelined Serial Mode (PSM). Although not as fast or energy-efficient as FPM, PSM addresses these two limitations of FPM.

5.2 Pipelined Serial Mode

The Pipelined Serial Mode efficiently copies data from a source row in one bank to a destination row in a different bank. PSM exploits the fact that a single internal bus that is shared across all the banks is used for both read and write operations. This enables the opportunity
to copy an arbitrary quantity of data one cache line at a time from one bank to another in a pipelined manner.

To copy data from a source row in one bank to a destination row in a different bank, PSM first activates the corresponding rows in both banks. It then puts the source bank into read mode, the destination bank into write mode, and transfers data one cache line (corresponding to a column of data—64 bytes) at a time. For this purpose, RowClone introduces a new DRAM command called TRANSFER. The TRANSFER command takes four parameters: 1) source bank index, 2) source column index, 3) destination bank index, and 4) destination column index. It copies the cache line corresponding to the source column index in the activated row of the source bank to the cache line corresponding to the destination column index in the activated row of the destination bank.

Unlike READ/WRITE, which interact with the memory channel connecting the processor and main memory, TRANSFER does not transfer data outside the chip. Figure 15 pictorially compares the operation of the TRANSFER command with that of READ and WRITE. The dashed lines indicate the data flow corresponding to the three commands. As shown in the figure, in contrast to the READ or WRITE commands, TRANSFER does not transfer data from or to the memory channel.

5.3 Mechanism for Bulk Data Copy

When the data from a source row (src) needs to be copied to a destination row (dst), there are three possible cases depending on the location of src and dst: 1) src and dst are within the same subarray, 2) src and dst are in different banks, 3) src and dst are in different subarrays within the same bank. For case 1 and case 2, RowClone uses FPM and PSM, respectively, to complete the operation (as described in Sections 5.1 and 5.2).

For the third case, when src and dst are in different subarrays within the same bank, one can imagine a mechanism that uses the global bitlines (shared across all subarrays within a bank – described in [77]) to copy data across the two rows in different subarrays. However,
RowClone does not employ such a mechanism for two reasons. First, it is not possible in today’s DRAM chips to activate multiple subarrays within the same bank simultaneously. Second, even if we enable simultaneous activation of multiple subarrays, as in [77], transferring data from one row buffer to another using the global bitlines requires the bank I/O circuitry to switch between read and write modes for each cache line transfer. This switching incurs significant latency overhead. To keep the design simple, for such an intra-bank copy operation, RowClone uses PSM to first copy the data from \texttt{src} to a temporary row (\texttt{tmp}) in a different bank. It then uses PSM again to copy the data from \texttt{tmp} to \texttt{dst}. The capacity lost due to reserving one row within each bank is negligible (0.0015\% for a bank with 64k rows).

Despite its location constraints, FPM can be used to accelerate \textit{Copy-on-Write} (CoW), an important primitive in modern systems. CoW is used by most modern operating systems (OS) to postpone an expensive copy operation until it is actually needed. When data of one virtual page needs to be copied to another, instead of creating a copy, the OS points both virtual pages to the same physical page (source) and marks the page as read-only. In the future, when one of the sharers attempts to write to the page, the OS allocates a new physical page (destination) for the writer and copies the contents of the source page to the newly allocated page. Fortunately, prior to allocating the destination page, the OS already knows the location of the source physical page. Therefore, it can ensure that the destination is allocated in the same subarray as the source, thereby enabling the processor to use FPM to perform the copy.

### 5.4 Mechanism for Bulk Data Initialization

Bulk data initialization sets a large block of memory to a specific value. To perform this operation efficiently, RowClone first initializes a single DRAM row with the corresponding value. It then uses the appropriate copy mechanism (from Section 5.3) to copy the data to the other rows to be initialized.

Bulk Zeroing (or BuZ), a special case of bulk initialization, is a frequently occurring operation in today’s systems \cite{66, 140}. To accelerate BuZ, one can reserve one row in each subarray that is always initialized to zero. By doing so, RowClone can use FPM to efficiently BuZ any row in DRAM by copying data from the reserved zero row of the corresponding subarray into the destination row. The capacity loss of reserving one row out of 512 rows in each subarray is very modest (0.2\%).

While the reserved rows can potentially lead to gaps in the physical address space, we can use an appropriate memory interleaving technique that maps consecutive rows to different subarrays. Such a technique ensures that the reserved zero rows are contiguously located in the physical address space. Note that interleaving techniques commonly used in today’s systems (e.g., row or cache line interleaving) have this property.
In-DRAM Bulk AND and OR

In this section, we describe In-DRAM AND/OR (IDAO), which is a mechanism to perform bulk bitwise AND and OR operations completely inside DRAM. In addition to simple masking and initialization tasks, these operations are useful in important data structures like bitmap indices. For example, bitmap indices [19, 102] can be more efficient than commonly-used B-trees for performing range queries and joins in databases [2, 19, 139]. In fact, bitmap indices are supported by many real-world database implementations (e.g., Redis [6], Fast-bit [2]). Improving the throughput of bitwise AND and OR operations can boost the performance of such bitmap indices.

6.1 Mechanism

As described in Section 4.2.2, when a DRAM cell is connected to a bitline precharged to \( \frac{1}{2} V_{DD} \), the cell induces a deviation on the bitline, and the deviation is amplified by the sense amplifier. IDAO exploits the following fact about DRAM cell operation.

The final state of the bitline after amplification is determined solely by the deviation on the bitline after the charge sharing phase (after state \( \Theta \) in Figure 6). If the deviation is positive (i.e., towards \( V_{DD} \)), the bitline is amplified to \( V_{DD} \). Otherwise, if the deviation is negative (i.e., towards 0), the bitline is amplified to 0.

6.1.1 Triple-Row Activation

IDAO simultaneously connects three cells as opposed to a single cell to a sense amplifier. When three cells are connected to the bitline, the deviation of the bitline after charge sharing is determined by the majority value of the three cells. Specifically, if at least two cells are initially in the charged state, the effective voltage level of the three cells is at least \( \frac{2}{3} V_{DD} \). This results in a positive deviation on the bitline. On the other hand, if at most one cell is initially in the charged state, the effective voltage level of the three cells is at most \( \frac{1}{3} V_{DD} \). This results in a negative deviation on the bitline voltage. As a result, the final state of the bitline is determined by the logical majority value of the three cells.

Figure 16 shows an example of activating three cells simultaneously. In the figure, we assume that two of the three cells are initially in the charged state and the third cell is in the empty state \( \Theta \). When the wordlines of all the three cells are raised simultaneously \( \Theta \), charge sharing results in a positive deviation on the bitline. Hence, after sense amplification, the sense amplifier drives the bitline to \( V_{DD} \) and fully charges all three cells \( \Theta \).

More generally, if the cell’s capacitance is \( C_c \), the the bitline’s is \( C_b \), and if \( k \) of the three cells are initially in the charged state, based on the charge sharing principles [69], the deviation \( \delta \) on the bitline voltage level is given by,

\[
\delta = \frac{k.C_c.V_{DD} + C_b.\frac{1}{2}V_{DD}}{3C_c + C_b} - \frac{1}{2}V_{DD}
\]
From the above equation, it is clear that $\delta$ is positive for $k = 2, 3$, and $\delta$ is negative for $k = 0, 1$. Therefore, after amplification, the final voltage level on the bitline is $V_{DD}$ for $k = 2, 3$ and 0 for $k = 0, 1$.

If $A$, $B$, and $C$ represent the logical values of the three cells, then the final state of the bitline is $AB + BC + CA$ (i.e., at least two of the values should be 1 for the final state to be 1). Importantly, using simple boolean algebra, this expression can be rewritten as $C(A + B) + \overline{C}(AB)$. In other words, if the initial state of $C$ is 1, then the final state of the bitline is a bitwise OR of $A$ and $B$. Otherwise, if the initial state of $C$ is 0, then the final state of the bitline is a bitwise AND of $A$ and $B$. Therefore, by controlling the value of the cell $C$, we can execute a bitwise AND or bitwise OR operation of the remaining two cells using the sense amplifier. Due to the regular bulk operation of cells in DRAM, this approach naturally extends to an entire row of DRAM cells and sense amplifiers, enabling a multi-kilobyte-wide bitwise AND/OR operation.

6.1.2 Challenges

There are two challenges in this approach. First, Equation 1 assumes that the cells involved in the triple-row activation are either fully charged or fully empty. However, DRAM cells leak charge over time. Therefore, the triple-row activation may not operate as expected. This problem may be exacerbated by process variation in DRAM cells. Second, as shown in Figure 16 (state Θ), at the end of the triple-row activation, the data in all the three cells are overwritten with the final state of the bitline. In other words, this approach overwrites the source data with the final value. In the following sections, we describe a simple implementation of IDAO that addresses these challenges.
6.1.3 Implementation of IDAO

To ensure that the source data does not get modified, IDAO first *copies* the data from the two source rows to two reserved temporary rows (T1 and T2). Depending on the operation to be performed (AND or OR), our mechanism initializes a third reserved temporary row T3 to (0 or 1). It then simultaneously activates the three rows T1, T2, and T3. It finally copies the result to the destination row. For example, to perform a bitwise AND of two rows A and B and store the result in row R, IDAO performs the following steps.

1. *Copy* data of row A to row T1
2. *Copy* data of row B to row T2
3. *Initialize* row T3 to 0
4. *Activate* rows T1, T2, and T3 simultaneously
5. *Copy* data of row T1 to row R

While the above mechanism is simple, the copy operations, if performed naively, will nullify the benefits of our mechanism. Fortunately, IDAO uses RowClone (described in Section 5), to perform row-to-row copy operations quickly and efficiently within DRAM. To recap, RowClone-FPM copies data within a subarray by issuing two back-to-back ACTIVATEs to the source row and the destination row, without an intervening PRECHARGE. RowClone-PSM efficiently copies data between two banks by using the shared internal bus to overlap the read to the source bank with the write to the destination bank.

With RowClone, all three copy operations (Steps 1, 2, and 5) and the initialization operation (Step 3) can be performed efficiently within DRAM. To use RowClone for the initialization operation, IDAO reserves two additional rows, C0 and C1. C0 is pre-initialized to 0 and C1 is pre-initialized to 1. Depending on the operation to be performed, our mechanism uses RowClone to copy either C0 or C1 to T3. Furthermore, to maximize the use of RowClone-FPM, IDAO reserves five rows in each subarray to serve as the temporary rows (T1, T2, and T3) and the control rows (C0 and C1).

In the best case, when all the three rows involved in the operation (A, B, and R) are in the same subarray, IDAO can use RowClone-FPM for all copy and initialization operations. However, if the three rows are in different banks/subarrays, some of the three copy operations have to use RowClone-PSM. In the worst case, when all three copy operations have to use RowClone-PSM, IDAO will consume higher latency than the baseline. However, when only one or two RowClone-PSM operations are required, IDAO will be faster and more energy-efficient than existing systems. As our goal in this article is to demonstrate the power of our approach, in the rest of the article, we will focus our attention on the case when all rows involved in the bitwise operation are in the same subarray.

6.1.4 Reliability of Our Mechanism

While the above implementation trivially addresses the second challenge (modification of the source data), it also addresses the first challenge (DRAM cell leakage). This is because, in our approach, the source (and the control) data are copied to the rows T1, T2 and T3 just before the triple-row activation. Each copy operation takes much less than 1 µs, which
is five orders of magnitude less than the typical refresh interval (64 ms). Consequently, the cells involved in the triple-row activation are very close to the fully refreshed state before the operation, thereby ensuring reliable operation of the triple-row activation. Having said that, an important aspect of the implementation is that a chip that fails the tests for triple-row activation (e.g., due to process variation) can still be used as a regular DRAM chip. As a result, this approach is likely to have little impact on the overall yield of DRAM chips, which is a major concern for manufacturers.

6.1.5 Latency Optimization

To complete an intra-subarray copy, RowClone-FPM uses two ACTIVATEs (back-to-back) followed by a PRECHARGE operation. Assuming typical DRAM timing parameters (tRAS = 35 ns and tRP = 15 ns), each copy operation consumes 85 ns. As IDAO is essentially four RowClone-FPM operations (as described in the previous section), the overall latency of a bitwise AND/OR operation is $4 \times 85\text{ ns} = 340\text{ ns}$.

In a RowClone-FPM operation, although the second ACTIVATE does not involve any sense amplification (the sense amplifiers are already activated), the RowClone paper [115] assumes the ACTIVATE consumes the full tRAS latency. However, by controlling the rows $D_1$, $D_2$, and $D_3$ using a separate row decoder, it is possible to overlap the ACTIVATE to the destination fully with the ACTIVATE to the source row, by raising the wordline of the destination row towards the end of the sense amplification of the source row. This mechanism is similar to the inter-segment copy operation described in Tiered-Latency DRAM [87] (Section 4.4). With this aggressive mechanism, the latency of a RowClone-FPM operation reduces to 50 ns (one ACTIVATE and one PRECHARGE). Therefore, the overall latency of a bitwise AND/OR operation is 200 ns. We will refer to this enhanced mechanism as aggressive, and the approach that uses the simple back-to-back ACTIVATE operations as conservative.

7 End-to-end System Support

Both RowClone and IDAO are substrates that exploit DRAM technology to perform bulk copy, initialization, and bitwise AND/OR operations efficiently inside DRAM. However, to exploit these substrates, we need support from the rest of the layers in the system stack, namely, the instruction set architecture, the microarchitecture, and the system software. In this section, we describe this support in detail.

7.1 ISA Support

To enable the software to communicate occurrences of the bulk operations to the hardware, the mechanisms introduce four new instructions to the ISA: memcopy, meminit, memand, and memor. Table 2 describes the semantics of these four new instructions. The mechanisms deliberately keep the semantics of the instructions simple in order to relieve the software from worrying about microarchitectural aspects of the DRAM substrate such as row size, alignment, etc. (discussed in Section 7.2.1). Note that such instructions are already present
in some of the instructions sets in modern processors – e.g., rep movsd, rep stosb, ermsb in x86 \[59\] and mvcl in IBM S/390 \[58\].

| Instruction | Operands      | Semantics                                                                 |
|-------------|---------------|---------------------------------------------------------------------------|
| memcopy     | \textit{src, dst, size} | Copy \textit{size} bytes from \textit{src} to \textit{dst}                |
| meminit     | \textit{dst, size, val} | Set \textit{size} bytes to \textit{val} at \textit{dst}                  |
| memand      | \textit{src1, src2, dst, size} | Perform bitwise AND of \textit{size} bytes of \textit{src1} with \textit{size} bytes of \textit{src2} and store the result in the \textit{dst} |
| memor       | \textit{src1, src2, dst, size} | Perform bitwise OR of \textit{size} bytes of \textit{src1} with \textit{size} bytes of \textit{src2} and store the result in the \textit{dst} |

**Table 2: Semantics of the memcopy, meminit, memand, and memor instructions**

There are three points to note regarding the execution semantics of these operations. First, the processor does not guarantee atomicity for any of these instructions, but note that existing systems also do not guarantee atomicity for such operations. Therefore, the software must take care of atomicity requirements using explicit synchronization. However, the microarchitectural implementation ensures that any data in the on-chip caches is kept consistent during the execution of these operations (Section \[7.2.2\]). Second, the processor handles any page faults during the execution of these operations. Third, the processor can take interrupts during the execution of these operations.

### 7.2 Processor Microarchitecture Support

The microarchitectural implementation of the new instructions has two parts. The first part determines if a particular instance of the instructions can be fully/partially accelerated by RowClone/IDAO. The second part involves the changes required to the cache coherence protocol to ensure coherence of data in the on-chip caches. We discuss these parts in this section.

#### 7.2.1 Source/Destination Alignment and Size

For the processor to accelerate a copy-initialization operation using RowClone, the operation must satisfy certain alignment and size constraints. Specifically, for an operation to be accelerated by FPM, 1) the source and destination regions should be within the same subarray, 2) the source and destination regions should be row-aligned, and 3) the operation should span an entire row. On the other hand, for an operation to be accelerated by PSM, the source and destination regions should be cache line-aligned and the operation must span a full cache line.

Upon encountering a \texttt{memcpy/meminit} instruction, the processor divides the region to be copiedinitialized into three portions: 1) row-aligned row-sized portions that can be
accelerated using FPM, 2) cache line-aligned cache line-sized portions that can be accelerated using PSM, and 3) the remaining portions that can be performed by the processor. For the first two regions, the processor sends appropriate requests to the memory controller, which completes the operations and sends an acknowledgment back to the processor. Since TRANSFER copies only a single cache line, a bulk copy using PSM can be interleaved with other commands to memory. The processor completes the operation for the third region similarly to how it is done in today’s systems. Note that the CPU can offload all these operations to the memory controller. In such a design, the CPU need not be made aware of the DRAM organization (e.g., row size and alignment, subarray mapping, etc.).

For each instance of memand/memor instruction, the processor follows a similar procedure. However, only the row-aligned row-sized portions are accelerated using IDAO. The remaining portions are still performed by the CPU. For the row-aligned row-sized regions, some of the copy operations may require RowClone-PSM. For each row of the operation, the processor determines if the number of RowClone-PSM operations required is three. If so, the processor completes the execution in the CPU. Otherwise, the operation is completed using IDAO.

### 7.2.2 Managing On-Chip Cache Coherence

Both RowClone and IDAO allow the memory controller to directly read/modify data in memory without going through the on-chip caches. Therefore, to ensure cache coherence, the controller appropriately handles cache lines from the source and destination regions that may be present in the caches before issuing the in-DRAM operations to memory.

First, the memory controller writes back any dirty cache line from the source region as the main memory version of such a cache line is likely stale. Using the data in memory before flushing such cache lines will lead to stale data being copied to the destination region. Second, the controller invalidates any cache line (clean or dirty) from the destination region that is cached in the on-chip caches. This is because after performing the operation, the cached version of these blocks may contain stale data. The controller already has the ability to perform such flushes and invalidations to support Direct Memory Access (DMA) [60]. After performing the necessary flushes and invalidations, the memory controller performs the in-DRAM operation. To ensure that cache lines of the destination region are not cached again by the processor in the meantime, the memory controller blocks all requests (including prefetches) to the destination region until the copy or initialization operation is complete. A recent work, LazyPIM [17], proposes an approach to perform the coherence operations lazily by comparing the signatures of data that were accessed in memory and the data that is cached on-chip. Our mechanisms can be combined with such works.

For RowClone, while performing the flushes and invalidates as mentioned above will ensure coherence, we propose a modified solution to handle dirty cache lines of the source region to reduce memory bandwidth consumption. When the memory controller identifies a dirty cache line belonging to the source region while performing a copy, it creates an in-cache copy of the source cache line with the tag corresponding to the destination cache line. This has two benefits. First, it avoids the additional memory flush required for the dirty source cache line. Second and more importantly, the controller does not have to wait for all the dirty source cache lines to be flushed before it can perform the copy. In the evaluation section,
we will describe another optimization, called RowClone-Zero-Insert, which inserts clean zero cache lines into the cache to further optimize Bulk Zeroing. This optimization does not require further changes to the proposed modifications to the cache coherence protocol.

Although the two mechanisms require the controller to manage cache coherence, it does not affect memory consistency — i.e., the ordering of accesses by concurrent readers and/or writers to the source or destination regions. As mentioned before, such an operation is not guaranteed to be atomic even in current systems, and software needs to perform the operation within a critical section to ensure atomicity.

7.3 Software Support

The minimum support required from the system software is the use of the proposed instructions to indicate bulk data operations to the processor. Although one can have a working system with just this support, the maximum latency and energy benefits can be obtained if the hardware is able to accelerate most operations using FPM rather than PSM. Increasing the likelihood of the use of the FPM mode requires further support from the operating system (OS) on two aspects: 1) page mapping, and 2) granularity of the operation.

7.3.1 Subarray-Aware Page Mapping

The use of FPM requires the source row and the destination row of a copy operation to be within the same subarray. Therefore, to maximize the use of FPM, the OS page mapping algorithm should be aware of subarrays so that it can allocate a destination page of a copy operation in the same subarray as the source page. More specifically, the OS should have knowledge of which pages map to the same subarray in DRAM. We propose that DRAM expose this information to software using the small EEPROM that already exists in today’s DRAM modules. This EEPROM, called the Serial Presence Detect (SPD) [63], stores information about the DRAM chips that is read by the memory controller at system bootup. Exposing the subarray mapping information will require only a few additional bytes to communicate the bits of the physical address that map to the subarray index. To increase DRAM yield, DRAM manufacturers design chips with spare rows that can be mapped to faulty rows [55]. The mechanisms can work with this technique by either requiring that each faulty row is remapped to a spare row within the same subarray, or exposing the location of all faulty rows to the memory controller so that it can use PSM to copy data across such rows.

Once the OS has the mapping information between physical pages and subarrays, it maintains multiple pools of free pages, one pool for each subarray. When the OS allocates the destination page for a copy operation (e.g., for a Copy-on-Write operation), it chooses the page from the same pool (subarray) as the source page. Note that this approach does not require contiguous pages to be placed within the same subarray. As mentioned before, commonly used memory interleaving techniques spread out contiguous pages across as many banks/subarrays as possible to improve parallelism. Therefore, both the source and destination of a bulk copy operation can be spread out across many subarrays.

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7.3.2 Granularity of the Operations

The second aspect that affects the use of FPM and IDAO is the granularity at which data is copied or initialized. These mechanisms have a minimum granularity at which they operate. There are two factors that affect this minimum granularity: 1) the size of each DRAM row, and 2) the memory interleaving employed by the controller.

First, in each chip, these mechanisms operate on an entire row of data. Second, to extract maximum bandwidth, some memory interleaving techniques map consecutive cache lines to different memory channels in the system. Therefore, to operate on a contiguous region of data with such interleaving strategies, the mechanisms must perform the operation in each channel. The minimum amount of data in such a scenario is the product of the row size and the number of channels.

To maximize the likelihood of using FPM and IDAO, the system or application software must ensure that the region of data involved in the operation is at least as large as this minimum granularity. For this purpose, we propose to expose this minimum granularity to the software through a special register, which we call the Minimum DRAM Granularity Register (MDGR). On system bootup, the memory controller initializes the MCGR based on the row size and the memory interleaving strategy, which can later be used by the OS for effectively exploiting RowClone/IDAO. Note that some previously proposed techniques such as sub-wordline activation [132] or mini-rank [136, 147] can be combined with our mechanisms to reduce the minimum granularity.

8 Evaluation

To highlight the benefits of performing various operations completely inside DRAM, we first compare the raw latency and energy required to perform these operations using different mechanisms (Section 8.1). We then present the quantitative evaluation of applications for RowClone and IDAO in Sections 8.2 and 8.3 respectively.

8.1 Latency and Energy Analysis

We estimate latency using DDR3-1600 timing parameters. We estimate energy using the Rambus power model [108]. Our energy calculations only include the energy consumed by the DRAM module and the DRAM channel Table 3 shows the latency and energy consumption due to the different mechanisms for bulk copy, zero, and bitwise AND/OR operations. The table also shows the potential reduction in latency and energy by performing these operations completely inside DRAM.

First, for bulk copy operations, RowClone-FPM reduces latency by 12x and energy consumption by 74.4x compared to existing interfaces. While PSM does not provide as much reduction as FPM, PSM still reduces latency by 2x and energy consumption by 3.2x compared to the baseline. Second, for bulk zeroing operations, RowClone can always use the FPM mode as it reserves a single zero row in each subarray of DRAM. As a result, it can reduce the latency of bulk zeroing by 6x and energy consumption by 41.5x compared to
existing interfaces. Finally, for bitwise AND/OR operations, even with conservative timing parameters, IDAO can reduce latency by 4.78x and energy consumption by 31.6x. With more aggressive timing parameters, IDAO reduces latency by 7.65x and energy by 50.5x.

The improvement in sustained throughput due to RowClone and IDAO for the respective operations is similar to the improvements in latency. The main takeaway from these results is that, for systems that use DRAM to store majority of their data (which includes most of today’s systems), these in-DRAM mechanisms are probably the best performing and the most energy-efficient way of performing the respective operations. We will now provide quantitative evaluation of these mechanisms on some real applications.

### 8.2 Applications for RowClone

Our evaluations use an in-house cycle-level multi-core simulator similar to memsim [9, 117, 118], along with a cycle-accurate command-level DDR3 DRAM simulator, similar to Ramulator [10, 78]. The multi-core simulator models out-of-order cores, each with a private last-level cache. We evaluate the benefits of RowClone using 1) a case study of the fork system call, an important operation used by modern operating systems, 2) six copy and initialization intensive benchmarks: bootup, compile, forkbench, memcached [4], mysql [5], and shell (Section 8.2.2 describes these benchmarks), and 3) a wide variety of multi-core workloads comprising the copy/initialization intensive applications running alongside memory-intensive applications from the SPEC CPU2006 benchmark suite [29]. Note that benchmarks such as SPEC CPU2006, which predominantly stress the CPU, typically use a small number of page copy and initialization operations and therefore would serve as poor individual evaluation benchmarks for RowClone.
We collected instruction traces for our workloads using Bochs [1], a full-system x86-64 emulator, running a GNU/Linux system. We modify the kernel’s implementation of page copyinitialization to use the `memcpy` and `meminit` instructions and mark these instructions in our traces. For the `fork` benchmark, we used the Wind River Simics full system simulator [8] to collect the traces. We collect 1-billion instruction traces of the representative portions of these workloads. We use the instruction throughput (IPC) metric to measure single-core performance. We evaluate multi-core runs using the weighted speedup metric [41, 122]. This metric is used by many prior works (e.g., [23, 39, 94, 113, 126, 127, 141, 142]) to measure system throughput for multi-programmed workloads. In addition to weighted speedup, we use five other performance/fairness/bandwidth/energy metrics, as shown in Table 7.

8.2.1 The `fork` System Call

`fork` is one of the most expensive yet frequently-used system calls in modern systems [112]. Since `fork` triggers a large number of CoW operations (as a result of updates to shared pages from the parent or child process), RowClone can significantly improve the performance of `fork`.

The performance of `fork` depends on two parameters: 1) the size of the address space used by the parent—which determines how much data may potentially have to be copied, and 2) the number of pages updated after the `fork` operation by either the parent or the child—which determines how much data is actually copied. To exercise these two parameters, we create a microbenchmark, `forkbench`, which first creates an array of size $S$ and initializes the array with random values. It then forks itself. The child process updates $N$ random pages (by updating a cache line within each page) and exits; the parent process waits for the child process to complete before exiting itself.

As such, we expect the number of copy operations to depend on $N$—the number of pages copied. Therefore, one may expect RowClone’s performance benefits to be proportional to $N$. However, an application’s performance typically depends on the overall memory access rate [128, 129], and RowClone can only improve performance by reducing the memory access rate due to copy operations. As a result, we expect the performance improvement due to RowClone to primarily depend on the fraction of memory traffic (total bytes transferred over the memory channel) generated by copy operations. We refer to this fraction as FMTC—Fraction of Memory Traffic due to Copies.

Figure 17 plots FMTC of `forkbench` for different values of $S$ (64MB and 128MB) and $N$ (2 to 16k) in the baseline system. As the figure shows, for both values of $S$, FMTC increases with increasing $N$. This is expected as a higher $N$ (more pages updated by the child) leads to more CoW operations. However, because of the presence of other read/write operations (e.g., during the initialization phase of the parent), for a given value of $N$, FMTC is larger for $S = 64$MB compared to $S = 128$MB. Depending on the value of $S$ and $N$, anywhere between 14% to 66% of the memory traffic arises from copy operations. This shows that accelerating copy operations using RowClone has the potential to significantly improve the performance of the `fork` operation.

Figure 18 plots the performance (IPC) of FPM and PSM for `forkbench`, normalized to that of the baseline system. We draw two conclusions from the figure. First, FPM im-
Figure 17: FMTC of forkbench for varying $S$ and $N$

Figure 18: Performance improvement due to RowClone for forkbench with different values of $S$ and $N$

proves the performance of forkbench for both values of $S$ and most values of $N$. The peak performance improvement is $2.2x$ for $N = 16k$ (30% on average across all data points). As expected, the improvement of FPM increases as the number of pages updated increases. The trend in performance improvement of FPM is similar to that of FMTC (Figure 17), confirming our hypothesis that FPM’s performance improvement primarily depends on FMTC.

Second, PSM does not provide considerable performance improvement over the baseline. This is because the large on-chip cache in the baseline system buffers the writebacks generated by the copy operations. These writebacks are flushed to memory at a later point without further delaying the copy operation. As a result, PSM, which just overlaps the read and write operations involved in the copy, does not improve latency significantly in the presence of a large on-chip cache. On the other hand, FPM, by copying all cache lines from the source row to destination in parallel, significantly reduces the latency compared to the baseline (which still needs to read the source blocks from main memory), resulting in high performance improvement.

Figure 19 shows the reduction in DRAM energy consumption (considering both the DRAM and the memory channel) of FPM and PSM modes of RowClone compared to that of the baseline for forkbench with $S = 64MB$. Similar to performance, the overall DRAM energy consumption also depends on the total memory access rate. As a result, RowClone’s potential to reduce DRAM energy depends on the fraction of memory traffic generated by copy operations. In fact, our results also show that the DRAM energy reduction due to
FPM and PSM correlate well with FMTC (Figure 17). By efficiently performing the copy operations, FPM reduces DRAM energy consumption by up to 80% (average 50%, across all data points). Similar to FPM, the energy reduction of PSM also increases with increasing \( N \) with a maximum reduction of 9% for \( N=16k \).

![Figure 19: Comparison of DRAM energy consumption of different mechanisms for forkbench (\( S = 64\text{MB} \))](image)

In a system that is agnostic to RowClone, we expect the performance improvement and energy reduction of RowClone to be in between that of FPM and PSM. By making the system software aware of RowClone (Section 7.3), i.e., designing the system software to be aware of the topology (subarray and bank organization) of DRAM, as also advocated by various recent works [74, 98, 101], we can approximate the maximum performance and energy benefits by increasing the likelihood of the use of FPM.

### 8.2.2 Copy/Initialization Intensive Applications

In this section, we analyze the benefits of RowClone on six copy/initialization intensive applications, including one instance of the forkbench described in the previous section. Table 4 describes these applications.

| Name     | Description                                                                 |
|----------|-----------------------------------------------------------------------------|
| bootup   | A phase booting up the Debian operating system.                             |
| compile  | The compilation phase from the GNU C compiler (while running cc1).          |
| forkbench| An instance of the forkbench described in Section 8.2.1 with \( S = 64\text{MB} \) and \( N = 1k \). |
| mcached  | Memcached [4], a memory object caching system, a phase inserting many key-value pairs into the memcache. |
| mysql    | MySQL [5], an on-disk database system, a phase loading the sample employeedb |
| shell    | A Unix shell script running ‘find’ on a directory tree with ‘ls’ on each sub-directory (involves filesystem accesses and spawning new processes). |

Table 4: Copy/Initialization-intensive benchmarks
Figure 20 plots the fraction of memory traffic due to copy, initialization, and regular read/write operations for the six applications. For these applications, between 10% and 80% of the memory traffic is generated by copy and initialization operations.

Figure 20: Fraction of memory traffic due to read, write, copy and initialization

Figure 21 compares the IPC of the baseline with that of RowClone and a variant of RowClone, RowClone-ZI (described shortly). The RowClone-based initialization mechanism slightly degrades performance for the applications which have a negligible number of copy operations (mcached, compile, and mysql).

Figure 21: Performance improvement of RowClone and RowClone-ZI. Value on top indicates percentage improvement of RowClone-ZI over baseline.

Our further analysis indicated that, for these applications, although the operating system zeroes out any newly allocated page, the application typically accesses almost all cache lines of a page immediately after the page is zeroed out. There are two phases: 1) the phase when the OS zeroes out the page, and 2) the phase when the application accesses the cache lines of the page. While the baseline incurs cache misses during phase 1, RowClone, as a result of performing the zeroing operation completely in memory, incurs cache misses in phase 2. However, the baseline zeroing operation is heavily optimized for memory-level parallelism (MLP) [46, 84, 97, 99, 100]. Memory-level parallelism indicates the number of concurrent outstanding misses to main memory. Higher MLP results in higher overlap in the latency of the requests. Consequently, higher MLP results in lower overall latency. In contrast, the cache misses in phase 2 have low MLP. As a result, incurring the same misses in Phase 2 (as with RowClone) causes higher overall stall time for the application (because the latencies
for the misses are serialized) than incurring them in Phase 1 (as in the baseline), resulting in RowClone’s performance degradation compared to the baseline.

To address this problem, RowClone uses a variant called RowClone-Zero-Insert (RowClone-ZI). RowClone-ZI not only zeroes out a page in DRAM but it also inserts a zero cache line into the processor cache corresponding to each cache line in the page that is zeroed out. By doing so, RowClone-ZI avoids the cache misses during both phase 1 (zeroing operation) and phase 2 (when the application accesses the cache lines of the zeroed page). As a result, it improves performance for all benchmarks, notably forkbench (by 66%) and shell (by 40%), compared to the baseline.

Table 5 shows the percentage reduction in DRAM energy and memory bandwidth consumption with RowClone and RowClone-ZI compared to the baseline. While RowClone significantly reduces both energy and memory bandwidth consumption for bootup, forkbench and shell, it has negligible impact on both metrics for the remaining three benchmarks. The lack of energy and bandwidth benefits in these three applications is due to serial execution caused by the cache misses incurred when the processor accesses the zeroed out pages (i.e., phase 2, as described above), which also leads to performance degradation in these workloads (as also described above). RowClone-ZI, which eliminates the cache misses in phase 2, significantly reduces energy consumption (between 15% to 69%) and memory bandwidth consumption (between 16% and 81%) for all benchmarks compared to the baseline. We conclude that RowClone-ZI can effectively improve performance, memory energy, and memory bandwidth efficiency in page copy and initialization intensive single-core workloads.

| Application | Energy Reduction | Bandwidth Reduction |
|-------------|------------------|---------------------|
|             | RowClone | +ZI | RowClone | +ZI |
| bootup      | 39%      | 40% | 49%      | 52% |
| compile     | -2%      | 32% | 2%       | 47% |
| forkbench   | 69%      | 69% | 60%      | 60% |
| mcached     | 0%       | 15% | 0%       | 16% |
| mysql       | -1%      | 17% | 0%       | 21% |
| shell       | 68%      | 67% | 81%      | 81% |

Table 5: DRAM energy and bandwidth reduction due to RowClone and RowClone-ZI (indicated as +ZI)

8.2.3 Multi-core Evaluations

As RowClone performs bulk data operations completely within DRAM, it significantly reduces the memory bandwidth consumed by these operations. As a result, RowClone can benefit other applications running concurrently on the same system. We evaluate this benefit of RowClone by running our copy/initialization-intensive applications alongside memory-intensive applications from the SPEC CPU2006 benchmark suite [29] (i.e., those applications with last-level cache MPKI greater than 1). Table 6 lists the set of applications used for our multi-programmed workloads.
Copy/Initialization-intensive benchmarks

bootup, compile, forkbench, mcached, mysql, shell

Memory-intensive benchmarks from SPEC CPU2006

bzip2, gcc, mcf, milc, zeusmp, gromacs, cactusADM, leslie3d, namd, gobmk, dealII, soplex, hmmer, sjeng, GemsFDTD, libquantum, h264ref, tlm, omnetpp, astar, wrf, sphinx3, xalancbmk

Table 6: List of benchmarks used for multi-core evaluation

We generate multi-programmed workloads for 2-core, 4-core and 8-core systems. In each workload, half of the cores run copy/initialization-intensive benchmarks and the remaining cores run memory-intensive SPEC benchmarks. Benchmarks from each category are chosen at random.

Figure 22 plots the performance improvement due to RowClone and RowClone-ZI for the 50 4-core workloads we evaluated (sorted based on the performance improvement due to RowClone-ZI). Two conclusions are in order. First, although RowClone degrades performance of certain 4-core workloads (with compile, mcached or mysql benchmarks), it significantly improves performance for all other workloads (by 10% across all workloads). Second, like in our single-core evaluations (Section 8.2.2), RowClone-ZI eliminates the performance degradation due to RowClone and consistently outperforms both the baseline and RowClone for all workloads (20% on average).

![Figure 22: System performance improvement of RowClone for 4-core workloads](image)

Table 7 shows the number of workloads and six metrics that evaluate the performance, fairness, memory bandwidth and energy efficiency improvement due to RowClone compared to the baseline for systems with 2, 4, and 8 cores. We evaluate fairness using the maximum slowdown metric, which has been used by many prior works [14, 31, 32, 33, 34, 37, 38, 72, 73, 75, 76, 86, 117, 126, 127, 128, 129, 133, 134, 135] as an indicator of unfairness in the system. Maximum slowdown is defined as the maximum of the slowdowns of all applications that are in the multi-core workload. For all three systems, RowClone significantly outperforms the baseline on all metrics.

To provide more insight into the benefits of RowClone on multi-core systems, we classify our copy/initialization-intensive benchmarks into two categories: 1) Moderately copy/initialization-intensive (compile, mcached, and mysql) and highly copy/initialization-intensive (bootup, forkbench, and shell). Figure 23 shows the average improvement in weighted speedup for the
| Number of Cores | 2 | 4 | 8 |
|-----------------|---|---|---|
| Number of Workloads | 138 | 50 | 40 |
| Weighted Speedup Improvement | 15% | 20% | 27% |
| Instruction Throughput Improvement | 14% | 15% | 25% |
| Harmonic Speedup Improvement | 13% | 16% | 29% |
| Maximum Slowdown Reduction | 6% | 12% | 23% |
| Memory Bandwidth/Instruction Reduction | 29% | 27% | 28% |
| Memory Energy/Instruction Reduction | 19% | 17% | 17% |

Table 7: Multi-core performance, fairness, bandwidth, and energy

different multi-core workloads, categorized based on the number of highly copy/initialization-intensive benchmarks. As the trends indicate, the performance improvement increases with increasing number of such benchmarks for all three multi-core systems, indicating the effectiveness of RowClone in accelerating bulk copy/initialization operations.

![Figure 23: Effect of increasing copy/initialization intensity](image)

We conclude that RowClone is an effective mechanism to improve system performance, energy efficiency and bandwidth efficiency of future, memory-bandwidth-constrained multi-core systems.

### 8.2.4 Memory-Controller-based DMA

One alternative way to perform a bulk data operation is to use the memory controller to complete the operation using the regular DRAM interface (similar to some prior approaches). We refer to this approach as the memory-controller-based DMA (MC-DMA). MC-DMA can potentially avoid the cache pollution caused by inserting blocks involved in the copy/initialization unnecessarily into the caches. However, it still requires data to be transferred over the memory bus. Hence, it suffers from the large latency, bandwidth, and energy consumption associated with the data transfer. Because the applications used in our evaluations do not suffer from cache pollution, we expect MC-DMA to perform comparably or worse than the baseline. In fact, our evaluations show that MC-DMA degrades performance compared to our baseline by 2% on average for the six copy/initialization inten-
sive applications (16% compared to RowClone). In addition, MC-DMA does not conserve any DRAM energy, unlike RowClone.

8.2.5 Other Applications

*Secure Deallocation.* Most operating systems (e.g., Linux [18], Windows [111], Mac OS X [121]) zero out pages newly allocated to a process. This is done to prevent malicious processes from gaining access to the data that previously belonged to other processes or the kernel itself. Not doing so can potentially lead to security vulnerabilities, as shown by prior works [25, 36, 49, 50].

*Process Checkpointing.* Checkpointing is an operation during which a consistent version of a process state is backed-up, so that the process can be restored from that state in the future. This checkpoint-restore primitive is useful in many cases including high-performance computing servers [16], software debugging with reduced overhead [124], hardware-level fault and bug tolerance mechanisms [26, 27, 28], mechanisms to provide consistent updates of persistent memory state [110], and speculative OS optimizations to improve performance [20, 137]. However, to ensure that the checkpoint is consistent (i.e., the original process does not update data while the checkpointing is in progress), the pages of the process are marked with copy-on-write. As a result, checkpointing often results in a large number of CoW operations.

*Virtual Machine Cloning/Deduplication.* Virtual machine (VM) cloning [80] is a technique to significantly reduce the startup cost of VMs in a cloud computing server. Similarly, deduplication is a technique employed by modern hypervisors [135] to reduce the overall memory capacity requirements of VMs. With this technique, different VMs share physical pages that contain the same data. Similar to forking, both these operations likely result in a large number of CoW operations for pages shared across VMs.

*Page Migration.* Bank conflicts, i.e., concurrent requests to different rows within the same bank, typically result in reduced row buffer hit rate and hence degrade both system performance and energy efficiency. Prior work [130] proposed techniques to mitigate bank conflicts using page migration. The PSM mode of RowClone can be used in conjunction with such techniques to 1) significantly reduce the migration latency and 2) make the migrations more energy-efficient.

*CPU-GPU Communication.* In many current and future processors, the GPU is or is expected to be integrated on the same chip with the CPU. Even in such systems where the CPU and GPU share the same off-chip memory, the off-chip memory is partitioned between the two devices. As a consequence, whenever a CPU program wants to offload some computation to the GPU, it has to copy all the necessary data from the CPU address space to the GPU address space [61]. When the GPU computation is finished, all the data needs to be copied back to the CPU address space. This copying involves a significant overhead. In fact, a recent work, Decoupled DMA [88], motivates this problem and proposes a solution to mitigate it. By spreading out the GPU address space over all subarrays and mapping the application data appropriately, RowClone can significantly speed up these copy operations. Note that communication between different processors and accelerators in a heterogeneous System-on-a-chip (SoC) is done similarly to the CPU-GPU communication and can also be accelerated by RowClone.
8.3 Applications for IDAO

We analyze our mechanism’s performance on a real-world bitmap index library, FastBit [2], widely-used in physics simulations and network analysis. Fastbit can enable faster and more efficient searching/retrieval compared to B-trees.

To construct an index, FastBit uses multiple bitmap bins, each corresponding to either a distinct value or a range of values. FastBit relies on fast bitwise AND/OR operations on these bitmaps to accelerate joins and range queries. For example, to execute a range query, FastBit performs a bitwise OR of all bitmaps that correspond to the specified range.

We initialized FastBit on our baseline system using the sample STAR [7] data set. We then ran a set of indexing-intensive range queries that touch various numbers of bitmap bins. For each query, we measure the fraction of query execution time spent on bitwise OR operations. Table 8 shows the corresponding results. For each query, the table shows the number of bitmap bins involved in the query and the percentage of time spent in bitwise OR operations. On average, 31% of the query execution is spent on bitwise OR operations (with small variance across queries).

| Number of bins | 3   | 9   | 20  | 45  | 98  | 118 | 128 |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| Fraction of time spent in OR | 29% | 29% | 31% | 32% | 34% | 34% | 34% |

To estimate the performance of our mechanism, we measure the number of bitwise OR operations required to complete the query. We then compute the amount of time taken by our mechanism to complete these operations and then use that to estimate the performance of the overall query execution. To perform a bitwise OR of more than two rows, our mechanism is invoked two rows at a time. Figure 24 shows the potential performance improvement using our two mechanisms (conservative and aggressive), each with either 1 bank or 4 banks.

![Figure 24: Range query performance improvement over baseline](image)

As our results indicate, our aggressive mechanism with 4 banks improves the performance of range queries by 30% (on average) compared to the baseline, eliminating almost all the overhead of bitwise operations. As expected, the aggressive mechanism performs better than the conservative mechanism. Similarly, using more banks provides better performance. Even
if we assume a 2X higher latency for the triple-row activation, our conservative mechanism with 1 bank improves performance by 18% (not shown in the figure).

8.4 Recent Works Building on RowClone and IDAO

Some recent works \[22, 89\] have built on top of RowClone and IDAO and have proposed mechanisms to perform bulk copy and bitwise operations inside memory. As we described in Section 5.3 to copy data across two subarrays in the same bank, RowClone uses two PSM operations. While this approach reduces energy consumption compared to existing systems, it still does not reduce latency. Low-cost Interlinked Sub-Arrays or LISA \[22\] addresses this problem by connecting adjacent subarrays of a bank. LISA exploits the open bitline architecture and connects the open end of each bitline to the adjacent sense amplifier using a transistor. LISA uses these connections to transfer data more efficiently and quickly across subarrays in the same bank. Pinatubo \[89\] takes an approach similar to IDAO and uses Phase Change Memory (PCM) technology to perform bitwise operations inside a memory chip built using PCM. Pinatubo enables the PCM sense amplifier to detect fine-grained differences in cell resistance. With the enhanced sense amplifier, Pinatubo can perform bitwise AND/OR operations by simultaneously sensing multiple PCM cells connected to the same sense amplifier.

9 Conclusion

In this article, we focused our attention on the problem of data movement, especially for operations that access a large amount of data. We first discussed the general notion of Processing in Memory (PiM) as a potential solution to reducing data movement so as to achieve better performance and efficiency. PiM adds new logic structures, sometimes as large as simple processors, near memory, to perform computation. We then introduced the idea of Processing using Memory (PuM), which exploits some of the peripheral structures already existing inside memory devices (with minimal changes), to perform other tasks on top of storing data. PuM is a cost-effective approach as it does not add significant logic structures near or inside memory.

We developed two new ideas that take the PuM approach and build on top of DRAM technology. The first idea is RowClone, which exploits the underlying operation of DRAM to perform bulk copy and initialization operations completely inside DRAM. RowClone exploits the fact DRAM cells internally share several buses that can act as a fast path for copying data across them. The second idea is In-DRAM AND/OR (IDAO), which exploits the analog operation of DRAM to perform bulk bitwise AND/OR operations completely inside DRAM. IDAO exploits the fact that many DRAM cells share the same sense amplifier and uses simultaneous activation of three rows of DRAM cells to perform bitwise AND/OR operations efficiently.

Our evaluations show that both mechanisms (RowClone and IDAO) improve the performance and energy-efficiency of the respective operations by more than an order of magnitude. In fact, for systems that store data in DRAM, these mechanisms are probably as efficient as...
any mechanism could be (since they minimize the amount of data movement). We described many real-world applications that can exploit RowClone and IDAO, and have demonstrated significant performance and energy efficiency improvements using these mechanisms. Due to its low cost of implementation and large performance and energy benefits, we believe Processing using Memory is a very promising and viable approach to minimize the memory bottleneck in data-intensive applications. We hope and expect future research will build upon this approach to demonstrate other techniques that can perform more operations in memory.

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