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Multi-level operation in VO$_2$-based resistive switching devices

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Abstract

Vanadium dioxide (VO$_2$) is widely studied for its prominent insulator–metal transition (IMT) near room temperature, with potential applications in novel memory devices and brain-inspired neuromorphic computing. We report on the fabrication of in-plane VO$_2$ metal–insulator–metal structures and reproducible switching measurements in these two-terminal devices. Resistive switching can be achieved by applying voltage or current bias, which creates Joule heating in the device and triggers the IMT. We analyze the current/voltage-induced resistive switching characteristics, including a pronounced intermediate state in the reset from the low to the high resistance state. Controllable switching behavior is demonstrated between multiple resistance levels over several orders of magnitude, allowing for multibit operation. This multi-level operation of the VO$_2$-bridge devices results from exploiting sub-hysteresis loops by Joule heating.

Introduction

Inspired by the functions of biological neurons and synapses in the brain, the memristor, a two-terminal switchable resistive memory, becomes the main functional unit for energy-efficient neuromorphic computing. In this development, there is a need for controllable and versatile resistive switching technologies, which is pursued along various routes. While many methods rely on thermal- or electric field-induced atomic rearrangements in the devices, an attractive option is offered by systems that exhibit hysteretic resistance vs temperature characteristics concomitant with electronic phase transitions. A particular case is the Mott insulator VO$_2$, which exhibits an insulator–metal transition (IMT) just above room temperature, with resistivity changes of several orders of magnitude. The IMT can be tuned by chemical doping, epitaxial strain, and external stimuli, such as temperature and electrical current/voltage. This makes VO$_2$ a suitable material for memristive devices and the realization of artificial neurons. For example, Yi et al. demonstrated 23 biological neuron spiking behaviors within one VO$_2$-based device. In a previous work of our group, Rana et al. observed multiple stable resistive states between the insulating and metallic states in VO$_2$ films by tailored temperature sweeps or external electrical stimuli, following an earlier work by Driscoll et al. The existence of the intermediate resistive states is unique and particularly attractive for reconfigurable electronic circuitry.

In this work, we fabricated planar bridge-structure devices from VO$_2$ thin films. By applying voltage sweeps, which create Joule heating in the device and trigger the IMT, we observed repeatable switching behavior with a correlation between the switching power and device dimensions. It shows a combination of digital switching and analog-like switching, and the reset happens gradually with steps, resulting in stable intermediate resistive states between the high resistive state (HRS) and the low resistive state (LRS). By tuning the applied voltage bias, we realized multistate memory within one VO$_2$-based memory cell (in our demonstration 3 bits per cell) and reliable multilevel operation. Additionally, we show multistate operation with a VO$_2$-based two-terminal parallel-bridge device as an outlook, providing another versatile route to realize multistate memory.

Methods

Epitaxial VO$_2$ thin films were deposited on single crystal TiO$_2$ (001) substrates using pulsed laser deposition (PLD) from a...
polycrystalline $\text{V}_2\text{O}_3$ target$^6$ [Fig. S1(a)]. The distance between the target and the sample is ~45 mm. A KrF excimer laser ($\lambda = 248$ nm, 20 ns pulse duration) was used with an energy density of ~1.3 J/cm$^2$ and a pulse repetition rate of 10 Hz. The growth temperature was 400 °C, and the oxygen background pressure was 10$^{-7}$ mbar. After deposition, the samples were cooled at 10 °C/min at the same oxygen pressure. To check the crystalline quality of the film, x-ray diffraction (XRD) scans were performed as a function of temperature. Atomic force microscopy (AFM) scans were conducted in the tapping mode to study the surface topography.

The as-deposited VO$_2$ films were patterned into single or parallel bridges with photolithography and wet or dry etching techniques. For single bridges [Fig. S1(b)], a 35% mass fraction nitric acid solution was used, while Ar$^+$ ion beam etching was used for the parallel-bridge devices [Fig. S3(a)]; for detailed settings, see Table S1 of the supplementary material. Two-terminal devices were fabricated with Ti (4.5 nm)/Au (50 nm) contact pads via RF sputtering and lift-off. The dimensions ($W \times L$) of the VO$_2$ single bridges measured in this work are $5 \times 10, 5 \times 15,$ and $5 \times 20$ μm$^2$. The VO$_2$ film thickness after all processing steps was in all cases ~10 nm, as verified by AFM [Figs. S1(d) and S1(e)].

Temperature-dependent transport measurements were carried out in a Quantum Design Physical Properties Measurement System (PPMS), and the resistivity was derived using a Van der Paw method. Electrical measurements were performed in a probe station with a Keithley 4200A-SCS parameter analyzer applying voltage or current sweeps at room temperature.

RESULTS AND DISCUSSION

The AFM image [Fig. 1(a)] of the as-deposited film shows that the VO$_2$ film is homogenous with an rms roughness of 0.6 nm. For the XRD measurement, a 2θ/ω scan [Fig. 1(b)] was performed to collect the diffraction peaks related to crystallographic planes parallel to the sample’s surface, therefore pointing to the out-of-plane direction. There are two peaks in the spectra: one from the (001)-oriented TiO$_2$ substrate at ~62.76° and the other from the rutile phase of VO$_2$ at ~65.70°. The clearly resolved thickness fringes indicate high sample quality and the calculated thickness is ~11 nm. There are no other peaks in Figs. 1(b) and S2, which confirms the epitaxy and phase purity of the VO$_2$ film, and the film is fully strained, as expected for a thickness below the critical thickness shown by Rodríguez et al.$^{14}$ Normally, this critical thickness is around 15 nm, and thicker films display cracking patterns due to the relaxation from the strain and consequent appearance of the monoclinic phase.$^{15}$

To study the IMT of the VO$_2$ film, the temperature evolution of both the first-order structural transition Fig. 1(c) and the resistivity Fig. 1(d) has been measured. Temperature-dependent XRD measurements were carried out under 25, 30, 40, 50, 60, 70, 80, and 90 °C, focusing on the VO$_2$ (002)$_h$ diffraction peak. As marked by the black arrow in Fig. 1(c), the (002)$_h$ peak shifts from ~65.70° to ~65.55° when the temperature increases from 25 to 90 °C. The slight shift to a lower angle suggests the expansion of the out-of-plane lattice parameter, but there is no phase transition. The hysteresis loop in Fig. 1(d) shows that the VO$_2$ film undergoes a sharp IMT with a 4-orders-of-magnitude decrease in resistivity. The transition temperature $T_{\text{IMT}}$ is 318 K (~44.9 °C), defined by the midpoint of the transition in the curve measured during the warm-up process. The IMT is normally accompanied by structural transformation from an insulating monoclinic (M1, P2$_1$/c) phase to a metallic rutile (R, P4$_2$/mm) phase as well as the dimerization of neighboring vanadium atoms.$^{16}$ However, the driving force behind the IMT of VO$_2$ still requires further investigation. The transition has been explained by two main theories. One considers a Mott–Hubbard transition in which strong Coulomb interaction between electrons splits the near-Fermi-level electronic states, while the other proposes a Peierls transition where the monoclinicrutile structural transformation with dimerization opens the insulating gap.$^{16}$ These two theories are relevant, although the order of occurrence remains under debate.$^{13}$ However, in this work, the VO$_2$ film is fully strained and already in the rutile phase at room temperature. The IMT happens while the temperature increases without an obvious crystallographic phase transition according to the temperature-dependent XRD results [Fig. 1(c)], which suggests that the IMT can be a purely electronic phase transition. It is also reported that the IMT in strained VO$_2$ films can result from electronic softening of Coulomb correlations within V–V singlet dimers happening at a lower temperature compared to the $T_{\text{IMT}}$. The coexistence of both the metallic and insulating phases within the hysteresis span of the IMT results in intermediate resistive states.$^{15,22}$ As shown in Fig. 1(e), during the heating process, we increased the maximum temperature in steps to gradually heat the film. For the cooling process, after the complete IMT, the film was gradually cooled by reversing the temperature midway [Fig. 1(f)]. The intermediate resistive states can be stabilized by tuning the temperature during the sweep before complete transition for both heating and cooling process. It is to be noted that the resistivity changes at a lower temperature when the film was heated up from the intermediate temperatures [Fig. 1(f)], which indicates that the film needs less heating to transform from the intermediate states to the metallic phase than the first transition. These minor loops within the hysteresis span are similar to the mathematical Preisach model of hysteresis,$^{22}$ which is normally used for ferromagnetic and ferroelectric material systems.

The above characterizations were done on unstructured VO$_2$ films. Subsequently, the VO$_2$ films were fabricated into two-terminal devices, according to the above-described procedure, and the $I$–$V$ characteristics were measured at room temperature. As shown in Fig. 2(a), while operating the devices at room temperature, they show typical volatile switching behavior, as the VO$_2$ bridges spontaneously return from the LRS to the HRS after the removal of the applied voltage. For the set process, the current of the device increases abruptly when the applied voltage surpasses the threshold value ($V_{\text{th}}$). For the reset process, the current first drops gradually with the decreasing applied voltage, followed by a sudden drop when the applied voltage is smaller than the hold voltage ($V_{\text{hold}}$). Hence, within one VO$_2$ bridge, there are both fast digital switching and continuous analog-like switching, which provides possibilities to control the resistive states. In addition, the device requires more voltage and power to switch for the first cycle than all the subsequent cycles. This forming process leads to a slight decrease of the HRS, making the device easier to switch with lower power.$^{23}$ The forming is not permanent and the devices normally recover in one or two days, which is consistent with previously reported data.$^{23}$ All other resistive switching characteristics reported were measured after the
forming. Figure 2(b) shows the $I-V$ curve of the DC voltage sweep in both positive and negative bias. The symmetrical curve indicates that the switching is independent of bias polarity, as expected from a Joule heating-based mechanism. A current compliance ($I_{CC}$) should be set to protect the devices. It plays an important role in the switching behavior and the control of resistive states since it maximizes the Joule heating generated inside the VO$_2$ bridges. Therefore, the $I-V$ characteristics have been measured with different current compliances [Fig. 2(c)]. Surprisingly, an intermediate step occurs during the reset process when higher current compliances were used.
FIG. 2. (a) Typical I(V) characteristics of the VO$_2$-based single-bridge devices ($W=5\,\mu m$, $L=20\,\mu m$). The curves of the first, second, and 500th cycles are plotted. $I_{CC}=0.1\,mA$. (b) I(V) characteristics of a VO$_2$-based single-bridge device ($W=5\,\mu m$, $L=20\,\mu m$) in positive and negative bias. $I_{CC}=1\,mA$. (c) I(V) characteristics of the VO$_2$-based single-bridge device ($W=5\,\mu m$, $L=20\,\mu m$) with varying current compliances ranging from 200 $\mu$A up to 5 mA. (d) I(V) characteristics of a VO$_2$-based single-bridge device ($W=5\,\mu m$, $L=20\,\mu m$) for 100 cycles. The curves of all cycles are shown. The inset figure shows the I(V) characteristics of 1 cycle in linear scale. $I_{CC}=1\,mA$.

In addition, it is shown in Fig. 2(d) that this behavior is repeatable and stable for over 100 cycles. It indicates that there are intermediate states between the LRS and HRS and it is possible to stabilize them by tuning the applied voltage and the compliance current history. The correlation between the switching parameters and device length can be found in Fig. 3 of the supplementary material. The set voltage and power both scale with device length, while the set current does not. Shorter devices require a lower voltage and power to switch since they have lower resistance and more Joule heating at a given voltage. In addition, for longer devices, the window between set and hold is wider. Figure S2(d) shows the ON-state resistance (recorded at $V_{\text{hold}}$) and OFF-state resistance (at 0.5 V) of devices with different lengths. The ON/OFF ratio is 1 order of magnitude for all the devices due to the moderate measurement settings ($I_{CC}=1\,mA$).

To map out the hysteresis loops for different intermediate resistive states, first, the DC voltage is swept from 0 V to the maximum value (5 V) to set the device to the LRS, and then it is swept back to an intermediate value such as 1.7 V. Afterward, it is swept from 1.7 to 5 V again and from there all the way back to 0 V to reset the device to the HRS. The voltage sweeping process can be found in Fig. S4 of the supplementary material. The results are plotted in Fig. 3(a), showing that multiple resistance states can be achieved when voltage sweeps are reversed at different intermediate voltages during the reset process. Similar to the temperature-dependent measurement in Fig. 1(f), it requires less voltage to switch from the intermediate states to the LRS at the second set event. In addition to voltage sweep measurements, static voltages have also been applied during the reset process to study the stability over time of these intermediate states. For this, the device is first set to the LRS, and then the voltage is swept back and maintained steady at a certain intermediate value [2, 2.5, or 2.8 V in Fig. 3(b)]. As it can be seen in Fig. 3(b), varying intermediate resistive states are stabilized. Moreover, the current compliance is still important to affect the resistance value of the intermediate state. With a lower $I_{CC}$ (like $<0.5\,mA$), the LRS is still fairly high and the controllable range of resistive states is correspondingly small. However, with a higher $I_{CC}$ (like $>5\,mA$), the LRS is very low, which raises the risk for irreversible breakdown.
FIG. 3. (a) Device resistance as a function of the voltage for one of the VO$_2$-based single-bridge devices. The DC voltage is swept from 0 V to the maximum value (5 V) and then is swept back and kept at an intermediate value, e.g., 1.7 V (as indicated by the black arrows). The voltage is then swept from 1.7 to 5 V again, and finally, all the way back to 0 V (as indicated by the red dashed arrows). $I_{CC} = 5$ mA. (b) Different resistance states obtained for three different applied voltage values (2, 2.5, and 2.8 V) in a VO$_2$-based single-bridge device ($W = 5$ $\mu$m, $L = 15$ $\mu$m). The upper panel shows the biasing scheme, while the bottom panel shows the time evolution of the resistance under that biasing scheme for three different values of the compliance current. (c) Time evolution of the resistance of the same device as in (b) under four different applied voltage values after an initial IMT step. The voltage was held for 5 min. The upper panel again shows the biasing scheme, and the correspondent measured resistance is shown below.

FIG. 4. Time evolution of the resistance of a VO$_2$-based single-bridge device ($W = 5$ $\mu$m, $L = 15$ $\mu$m) under different voltage-biasing schemes. Eight distinguishable states (color-coded dashed lines) can be reached within one device. States are accessible in (a) consecutive ascending order or (b) consecutive descending order by adjusting the intermediate voltage value. (c) Each level can also be independently reached. Upper panels show the applied voltage and calculated power plotted as a function of time, and lower panels are the resistance as a function of time.
can be reached independently and randomly. While accessing the states in consecutive descending order, under voltage bias, the device is first set to the LRS before the resistance is fixed on the return to the high resistance state. This is because set processes to the low resistance states are too abrupt to stabilize under voltage bias. With current control this can straightforwardly be accomplished though, without the need to first go completely to the LRS. Fortunately, the set–reset processes can happen comparatively faster as the required temperature swings of a few degrees associated with this electronic phase transition are low as compared to the devices relying on crystalline phase changes. The power is also calculated and plotted in the upper panels of Fig. 4. The required power to switch to the LRS is 2.5 mW, and the one to maintain the intermediate states is less than 1 mW. Obviously, these are high values for practical devices, but the values will be decreased if the device dimensions are reduced from the microscale to the nanoscale.

The switching mechanism has been widely studied. It is known that the conducting filament formation triggered by Joule heating in the VO$_2$ bridge leads to resistive switching. With various
in situ characterization techniques, the forming process of the filaments has been visualized both statically\textsuperscript{1,26} and dynamically.\textsuperscript{27,28} As reported before,\textsuperscript{28} the current flows inhomogeneously due to intrinsic defects in the bridge, leading to the nucleation of the metallic domains. Once a small portion transits to the metallic state, the current increases and the Joule heating triggers filament formation and expansion. The filament formation is avalanche-like on a time scale of nanoseconds.\textsuperscript{28} However, the rupture of the filament is a much slower process on a time scale of milliseconds.\textsuperscript{28} During the reset process, the metallic domains inside the filament relax to the insulating state at different speeds due to inhomogeneity.\textsuperscript{24,25} The filament becomes partially metallic and partially insulating, and this intermediate state can be held with a small external stimulus since the residual metallic domains can attract the current and maintain the IMT. When the device is set to different intermediate resistive states, the ratio between the metallic domains and insulating domains is being tuned. Figure 5 schematically shows the filament status for the whole process of nucleation, formation, partial retention, and rupture. There are two intermediate states shown, intermediate state I with more metallic domains and intermediate state II with fewer metallic residues. To switch from I to II, the applied voltage can be decreased so that the metallic domains that remained will further become insulating. However, switching from II to I requires the device to be fully set again, and then, the applied voltage can be decreased to the right value. If the applied voltage simply increases, the device will undergo the complete IMT with a lower power instead of going to a lower intermediate resistive state since the filament formation is unpredictable and ultrafast.

Beyond the V\textsubscript{O2}-based single-bridge memristive devices, we also fabricated devices with two identical parallel V\textsubscript{O2} bridges with varying bridge-to-bridge distances [see the device structure in Fig. S5(a) of the supplementary material]. It is to be noted that the initial resistance of parallel-bridge devices is lower, possibly because we used Ar\textsuperscript{+} etching for the structuring of these bridges. Figure 6(b) shows the I–V characteristics measured with a current-controlled sweep. Different from the voltage-controlled curves in Fig. 6(a), there are two snapbacks in the set process providing intermediate resistance states [Fig. 6(c)]. The distance between bridges plays an important role in the occurrence of the intermediate state (see Fig. S3 of the supplementary material). If the bridges are close to each other, in this experiment <20 \textmu m, the heat dissipation of one bridge will affect the other and both bridges will switch to the ON state almost at the same time so that there is no stable intermediate state during the set process. It is likely that the characteristic length scale for the occurrence of this thermal crossstalk-induced synchronization depends on the individual V\textsubscript{O2} bridge dimensions and the current pulse duration, requiring further study. Figure 6(d) schematically shows the switching status of two distant bridges corresponding to different resistive states. In the beginning, both of the bridges are OFF and the overall device shows a HRS. Once the current is applied, due to the intrinsic inhomogeneity, one bridge will switch to the ON state first; therefore, the device shows the intermediate state. Finally, the other bridge will also switch to the ON state with increased current and the device shows a LRS. Systematic investigation on the stability and repeatability of the intermediate states is still required. However, the current results indicate the potential for multilevel operation of such parallel bridge configurations within a single two-terminal V\textsubscript{O2}-based device. The concept can readily be extended to more parallel channels and complex network configurations. Moreover, one may further use multilayering to stack bridges in the vertical direction and provide a further dimension for multibit operations.

**CONCLUSION**

In conclusion, we have investigated two-terminal memristive devices based on V\textsubscript{O2} thin film bridges. By tuning the applied voltage or current, we realized multistate memory within one V\textsubscript{O2}-based memory cell and reliable multilevel operation at room temperature. This multi-level operation of the V\textsubscript{O2}-bridge devices results from exploiting sub-hysteresis loops by Joule heating, which provides opportunities for novel (neuromorphic) electronics.

**SUPPLEMENTARY MATERIAL**

See the supplementary material for the device structures and additional measurement data showing the correlation between switching behavior and device dimensions.

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**AUTHOR DECLARATIONS**

Conflict of Interest

The authors declare no conflict of interest.

**DATA AVAILABILITY**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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