DeepDive: An Integrative Algorithm/Architecture Co-Design for Deep Separable Convolutional Neural Networks

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Abstract

Deep Separable Convolutional Neural Networks (DSCNNs) have become the emerging paradigm by offering modular networks with structural sparsity in order to achieve higher accuracy with relatively lower operations and parameters. However, there is a lack of customized architectures that can provide flexible solutions that fit the sparsity of the DSCNNs. This paper introduces DeepDive, which is a fully-functional, vertical co-design framework, for power-efficient implementation of DSCNNs on edge FPGAs. DeepDive’s architecture supports crucial heterogeneous Compute Units (CUs) to fully support DSCNNs with various convolutional operators interconnected with structural sparsity. It offers an FPGA-aware training and online quantization combined with modular synthesizable C++ CUs, customized for DSCNNs. The execution results on Xilinx’s ZCU102 FPGA board, demonstrate 47.4 and 233.3 FPS/Watt for MobileNet-V2 and a compact version of EfficientNet, respectively, as two state-of-the-art depthwise separable CNNs. These comparisons showcase how DeepDive improves FPS/Watt by 2.2× and 1.51× over Jetson Nano high and low power modes, respectively. It also enhances FPS/Watt about 2.27× and 37.25× over two other FPGA implementations. The DeepDive output for MobileNetV2 is available at https://github.com/TeCSAR-UNCC/DeepDive.

1 Introduction

The astonishing growth in deep learning algorithms, particularly, Convolutional Neural Networks (CNNs), has enabled many exciting applications in visual analytics. We have observed a recent shift towards Domain-Specific Architectures (DSA), e.g., Systolic Arrays, CGRAs, Tensor Cores, to cope with the significant computation demand raised by deep learning paradigms [6, 7, 14, 17, 23, 26, 28]. These emerging DSAs often transform convolutional operations into dense linear algebraic operations across the channels and kernels. This maximizes parallelism and compute resource utilization, as well as minimizes data movements, by increasing data re-usability. They are typically designed to be a generic, one-size-fits-all architecture that allows hardware reuse between different layer operations. As a result, they execute the target CNN layer-by-layer sequentially. A notable example is the recently introduced Versatile Tensor Accelerator (VTA) [14], which is an open, generic, and customizable deep learning accelerator with a complete TVM-based compiler stack, targeted for edge FPGAs. Another such accelerator design presented by [12] introduces a configurable architecture, pipelined, and timing controlled design with fixed hardware solution specially designed for MobileNet.

Deep Separable CNNs (DSCNNs) [9, 11, 15, 19, 25, 27] have emerged as an innovative algorithmic solutions to achieve higher accuracy with relatively lower parameters and operations. State-of-the-art separable CNNs, e.g., MobileNet family [9,11] and EfficientNet [19], offer modular networks with structural sparsity over various convolutional operators — group, depthwise, and pointwise convolution. DSCNNs often result in relatively higher computational sparsity, more data-dependent layer-to-layer communication, and less data reuse potential over their predecessor networks, such as

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ResNet [8] or VGG [18]. At the same time, the modular design, combined with the structural sparsity of DSCNNs, allows the designer to systematically trade between algorithmic accuracy, and computational demand, via tunable knobs that vary the sparsity of the network, e.g., varying degree of width multiplication in MobileNet-V2.

The structural sparsity of DSCNNs makes existing DSAs, e.g., VTA or Tensor Cores, less suitable for efficient execution of DSCNNs, as the current DSAs have been often designed for dense operations with highly regular data access and high data reuse. At the same time, current DSAs are often optimized for a single design point in isolation, which limits their efficiency when running DSCNNs. For instance, they convert sparse convolutions to dense matrices (e.g., depthwise to group-convolution transform), which leads to higher computational overhead than the original DSCNNs, while delivering the same accuracy. As an example, VTA had to make a specialized version of MobileNet, which they call MobileNetG, to remove depthwise separable convolution and make it running efficiently on systolic array implemented on FPGAs. FPGA implementation introduced in [12] has massive data movements as a result of their configurable data path design which results in high latency. Also such type of fixed architectures adopted in [2,12,13,24] makes it difficult to achieve scalability to support modern DSCNNs, e.g. EfficientNet.

This paper proposes a fully functional framework called DeepDive for an agile, power-efficient execution of DSCNNs. DeepDive offers a novel architecture for efficient execution of DSCNNs, combined with a vertical algorithm/architecture optimization and synthesis on edge FPGAs. The framework is designed to identify key heterogeneous Compute Units (CUs), to fully support DSCNNs with heterogeneous convolutional operations, such as group, depthwise, and point-wise convolution. Fig. 1 abstracts DeepDive design flow. At the front-end, DeepDive receives the network description model (e.g., PyTorch), and optimizes the model based on the FPGA-aware training and online quantization. This includes algorithm-specific fusing of batch normalization and convolutional operators, which reduces the computation by ~4%, and extremely low-bit per-channel-quantization across all separable convolution layers. The output of the front-end will be QNet, which contains all of the meta-data regarding the FPGA-aware trained as well as quantized network model. At the back-end, DeepDive relies on the recent advances in High-Level Synthesis (HLS) and shifts the optimization abstraction to pre-RTL design. The Network SoC Compiler creates a customized memory path and synthesizable model of the entire hardware accelerator for Programmable Logic (PL) based on pre-designed CUs and provided convolution operators. It also generates the host CPU code running on ARM cores located in the Processing System (PS) side of SoC for synchronization and scheduling. The host code, bundled with a scheduler, enables the DeepDive back-end system to support multiple run-time software stacks such as Pynq and Linux. The key contributions are:

- The structure and the flexibility of DeepDive enables an agile framework to support the fast-growing and up-coming DSCNNs. To the best of our knowledge, this work is the first scalable solution with the support of recently introduced EfficientNet DSCNN families.
- It proposes a novel scalable vertical framework for the execution of DSCNN on FPGAs. The vertical integration and library-based operation mapping enables true comprehensive design space exploration on FPGAs.

The rest of this article is organized as the following: Section 2 discuss the algorithmic properties of DSCNNs and further motivates DeepDive. Section 3 presents DeepDive’s front-end, focusing on FPGA-aware training and online quantization. Section 4 details DeepDive’s back-end architecture and design flow. Section 5 presents DeepDive’s execution results on Xilinx’s ZCU102 FPGA and comparison against state-of-the-art solutions. Section 6 reviews the related work. Finally, Section 7 concludes this paper.

2 Algorithmic Principles of Deep Separable CNNs

DSCNNs [9, 11, 19, 27] have emerged as a new paradigm to achieve higher accuracy with relatively fewer parameters and operations over the classical CNNs. The efficiency of DSCNNs stems from their structural sparsity, combined with a modular configurable network topology, that can be scaled up or down, depending on desired accuracy and corresponding computational overhead. In this section, we define the basic principles and structural properties of DSCNN. For ease of access, we summarized the symbols that appeared in this paper and their description in Table 1. These symbols will be used throughout this paper.

| Item | Parameter | Description |
|------|-----------|-------------|
| 1    | $N$       | Input channel size |
| 2    | $M$       | Output channel size |
| 3    | $K$       | Kernel size |
| 4    | $H$       | Height of input feature |
| 5    | $W$       | Width of input feature |
| 6    | $G$       | Group size |
| 7    | $BW$      | Bit-width |
| 8    | $\alpha$  | Width multiplier |
| 9    | $k$       | Number of classes |

Fig. 2(a) shows normal convolution filters with the shape of $M \times N \times K \times K$; thus, the computational cost of normal convolution is $C = H \times W \times K^2 \times N \times M$. Group-convolution, shown in Fig. 2(b), minimizes the computation cost of a convolution operator by grouping its channel in $G$ receptions, reducing computation to $C/G$, where $M = f \cdot G$ where $f \in \mathbb{N}$. Depthwise convolution [5, 9] is an extreme case of group-convolution, where $G = N, f = 1$. In this case, each filter is applied to each input channel individually based on Fig. 2(c), and in contrast to the normal convolution, there is no reduction (summation) across channels. Pointwise convolution is another type of operator which minimizes the computation by not capturing spatial dependencies within a frame pixels by setting the kernel size to $1 \times 1$.

![Figure 2: Different convolutional operators.](image-url)
Figure 3: Inverted Residual Block (IRB) for MobileNet-V2 (a) and EfficientNet (b), respectively. The illustration of Batch Normalization and Activation layers repeated after each convolution are ignored.

As mentioned earlier, depthwise convolution minimizes computation by removing reduction along the input channels; thus, it is not able to capture the channel-wise information. In the same fashion, pointwise convolution reduces the computation complexity by removing spatial filtering, while it has a full reduction in channel depth. Depthwise separable convolution, used in MobileNet-V1 [9], is an integrated operator composed of a depthwise convolution, followed by pointwise convolution, in order to capture information in both spatial and channel domains, respectively. However, there is still information loss as features move along the network depth and are embedded into lower-dimensional space. MobileNet-V2 [11] introduced inverted residual connections to its previous network, further reducing both multiply-add operations, and model size, without sacrificing the network accuracy. The idea of residual connections was inspired by the ResNet [8] architecture to minimize information loss and speed up the training phase. Fig. 3 shows the structure of the Inverted Residual Block (IRB). IRB consists of a pointwise (expansion) convolution, followed by a depthwise convolution, followed by another pointwise (projection) convolution, to embed the features in a lower dimension. The MobileNet-V2 can control IRB layer input channel width, i.e., $N$, by altering the $\alpha$, which changes $N$ to $\alpha \times N$. The $\alpha = 1$ is the baseline model. Selecting $\alpha < 1$ can reduces the computational complexity and the model size quadratically by roughly $\alpha^2$. We have examined the effect of this knob and image input size on the final hardware performance and its accuracy in Section 5.

Another recently introduced example is EfficientNet, which further optimizes the IRB by adding Squeeze and Excitation (SE) blocks. Fig. 3(b) presents the EfficientNet IRB with SE block. The SE block consists of a squeeze operation that captures the global spatial features, followed by an excitation operation that uses a gating function to allow important features to be captured while ignoring the rest. Traditionally, the normal sigmoid is used as the gating function for the SE block, but is replaced with the hard sigmoid to further reduce computation complexity. The hard sigmoid is a non-smooth approximation of the sigmoid function and is described as:

$$ReLU_6(x + 3), \quad \frac{6}{x}$$

$$ReLU_6(x) = \begin{cases} x, & \text{if } 0 \leq x \leq 6 \\ 0, & \text{otherwise} \end{cases}$$

The design principles of DSCNNs result in relatively higher computational sparsity due to heterogeneous computing operators that cannot share hardware resources. Depthwise convolution accumulates only across the spatial axis and needs only $K \times K$ fused-multiply-add (FMA) operations since its weight shape is $[M, 1, K, K]$. Since versatile systolic arrays are often designed to support both spatial and channel accumulation, they perform more FMA operations. They map depthwise to matrix multiplication problem by kernel zero-padding and reshaping appropriately; however, the cost of memory real estate, and the redundant computation demand, are not affordable for resource-constrained hardware platforms.

In next, we introduce DeepDive as a fully vertical and versatile solution to support sparse operators introduced in DSCNNs. As case studies, we selected MobileNet-V2 and EfficientNet as two examples of DSCNNs, and we thoroughly elaborate their implementation with the aid of DeepDive in section 5.1 and 5.2, respectively.
3 DeepDive: Front-end

This section describes the front-end of DeepDive, which brings hardware-awareness into training DSCNNs. Fig. 4 illustrates the main components of the front-end and their corresponding output. The procedure starts by feeding a pre-trained floating-point network into the DeepDive. The **Batch-Norm Fusing** merges the batch-normalization operator into the convolution in order to remove any floating-point operations in the final hardware solution. Next, **Online Channel-wise Low-Bit Quantization** quantizes while training the fused network at extremely low-bit resolutions (e.g., 3-6 bit) across all channels within separable layers. Then, the trained network will be calibrated by extracting the minimum and maximum values across all channels per layer of the network. The **Post-Trained Model Quantization** then uses these acquired ranges to fuse the activation layer, i.e., ReLU6, into the convolution operator. The outcome, \( QNet \), consists of only convolution operators that have had their output set to the minimum and maximum quantized value automatically—when they are less than 0 and greater than 6, respectively. In the following, we explain the details of two important aspects of front-end: (1) Batch-Norm Fusing, and (2) Online Channel-wise Low-Bit Quantization.

### 3.1 Batch-Normalization Fusing

Batch-Normalization (BN) [10] is a linear operator, generally seen following a convolution layer, in order to normalize the output of the convolution. BN improves the training speed and stability of the network. The BN function is defined by Eq. 3:

\[
\hat{x} = \gamma \frac{x - \mu}{\sqrt{\sigma^2 + \epsilon}} + \xi,
\]

where \( \gamma \) is BN weight, \( \xi \) is its bias, and \( \mu \) and \( \sigma \) are mean and variance of training batch calculated during the training, respectively. \( \epsilon \) is a small constant defined to prevent division by zero. Both \( \gamma \) and \( \beta \) are trainable parameters.

For networks where its convolution operators are always followed by BN, DeepDive online training fuses these two consecutive layers together by applying following equations:

\[
\hat{\omega} = \frac{1}{\sigma^2 + \epsilon} \hat{\omega},
\]

\[
\hat{\omega}_{\text{conv}} = \omega_{\text{conv}} \times \text{diag} (\gamma \cdot \hat{\omega}),
\]

\[
\hat{B}_{\text{conv}} = B_{\text{conv}} + (\xi - (\gamma \cdot \mu \cdot \hat{\omega})),
\]

where \( \omega_{\text{conv}} \) and \( B_{\text{conv}} \) are trained weights and biases of convolution operator, respectively. After BN fusion, the network model is ready for quantize-aware training.

### 3.2 Online Channel-wise Low-bit Quantization

Quantization is a well-known approach to compress the network model size, and speed up the computation, by mapping number representations from floating-point single precision (FP32) to integer representation. Due to the malleability of FPGA fabrics, designers can greatly reduce the integer bit-width, while minimizing the introduced quantization error, by training the network for the new representation. DeepDive applies the Range-Based Linear quantization to compress the network weights and biases. Let’s define \( T = \{ x \mid x \in \mathbb{R} \} \), such that \( T \) is the floating-point pre-trained network...
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convolution operators. In simple words, the Network SoC Compiler generates a network graph containing the network

highly-optimized RTL micro-architectural blocks or synthesizable C++ model for depthwise, pointwise, and normal

the system for both hardware (as synthesizable C++ models mapped to FPGAs fabric), software codes, and system

configurations. To generate the optimized hardware for DSCNNs, the Network SoC Compiler uses pre-designed

highly-optimized RTL micro-architectural blocks or synthesizable C++ model for depthwise, pointwise, and normal

convolution operators. In simple words, the Network SoC Compiler generates a network graph containing the network

layout and data dependencies. It then creates key heterogeneous CUs, called QNet Accelerators, with respect to

DeepDive’s system architecture.

In the following, at first, we describe micro-architectural details of convolutional operators, and then we discuss the
details of the Network SoC compiler and system architecture.

4.1 Convolutional Operators

Since DeepDive is specially designed for DSCNNs, it naturally supports all convolutional operations, namely, normal
convolution, depthwise convolution, and pointwise convolution. Each convolution operator buffers minimum job
data size, which is necessary to start the computation, with the assumption that the network parameters necessary for
computing are transferred to internal memory, and that the intermediate feature maps are streamed in and out. These
operators are pipelined and parallelized in a way that is ideal for both memory-bound and compute-bound operations.
The heart of a convolutional operator is a reconfigurable Direct Convolution core with different degrees of parallelism.
The amount of parallelism defines the utilization, and parallel read/write ports required by the scratchpad or local buffers.
This flexibility allows the Network SoC Compiler to manage the resources efficiently by tweaking the parallelism knobs to achieve the best performance (will be further discussed in section 4.2). Next, we elaborate on each operator from the design standpoint. In addition, we formulate the amount of parallelism per each convolutional operator.

### 4.1.1 Depthwise Convolution

The Depthwise convolution uses a 3D line buffer and 3D window to perform direct convolution. The input feature is streamed into a line buffer and then copied into a window buffer with parallel read access, as shown in Fig. 7. Once the computation is finished, the data in the computation core will be flushed and reloaded with the new one from the line buffer. The hardware design ensures the data movement involved in this process is fully pipelined, and the initiation interval is limited to a single cycle. Computation starts as soon as the required amount of data is streamed from the main memory. For the current design, the max achievable parallelism is limited to the $K$ and $N$. 

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**Figure 6:** DeepDive: Back-end.

**Figure 7:** Shift and update mechanism of Window and Line Buffer. ① Line Buffer is filled with input feature data. ② Window Buffer is convoluted with weights. ③ The data in window is left shifted. ④ New data from the line buffer is copied in to the window. ⑤ & ⑥ Data from the FIFO is then copied into the line buffer and window buffer. All the Data Movements are pipelined.
Fig. 8 presents the micro-architecture of depthwise and normal convolution operators. As depicted in Fig. 8, the selected input is read in streaming fashion into the 3D line buffer and then copied into the sliding window. The weights are burst read into the weight scratch pad. The Sliding Window and the Weight scratchpad have multiple read ports. Every channel of the input is processed by the direct convolution compute core. The direct convolution compute core has a parallel multiplier, and a pipelined adder tree, together which carryout the MAC operation, followed by the Approximator and Clip unit. This unit truncates, or rounds, the results and then clips them to \([0, 2^BW - 1]\) based on the quantization parameters extracted at the front-end for this operator. Therefore, this unit also acts as the ReLU6 activation layer defined in MobileNet-V2 or EfficientNet. The depthwise convolution is more sparse, and has the least amount of data reuse. The maximum parallel operations are calculated as the following:

\[
ParallelOps = K_{max}^{dw} \times K_{max}^{dw} \times N_{max}^{dw},
\]

In Eq. 8, \(K_{max}^{dw}\) and \(N_{max}^{dw}\) are the maximum kernel size and maximum input-channel across all the depthwise convolutions in the network, respectively.

### 4.1.2 Normal Convolution

The DSCNN has one normal convolution, and it is the first operator to embed patterns from both spatial and channel dimensions from the given input image. Since the next layer after normal convolution is depthwise, it is essential to generate output pixels column-wise (spatial dimension) so the depthwise can start the job immediately. Therefore, we improve the parallelism level by having a dedicated adder tree located after the direct convolution kernel for the input channel reduction. The block diagram of normal convolution is, also shown in Fig. 8. The parallelism in normal convolution is across kernel size and input channels — described in the following:

\[
ParallelOps = K_{max}^{nc} \times K_{max}^{nc} \times N_{max}^{nc},
\]

where \(N_{\text{MaxSize}}^{nc}\) is the maximum input channel size, and \(K_{max}^{nc}\) is the maximum kernel size, assigned from all normal convolution. Normal convolution has slightly more data movements compared to the depthwise convolution due to the pipelined adder tree implemented at the end of direct convolution core.
4.1.3 Pointwise Convolution

Due to the dense operation of pointwise, the design of this operator can be similar to the design of a general matrix multiplication, which is well suited for the systolic array. With maximum data reuse, this operator can leverage maximum parallelism. It has both fewer algorithmic, and fewer data movement complexity, which makes it best fit for a high amount of parallelism. Fig. 9 shows the structure of pointwise convolution operator. The required input is directly read into the input scratchpad from the read buffer. The weights are burst read into the weight scratchpad. The input buffer and the weight scratchpad have multiple read ports for parallel data access. The single-cycle parallel multiplier and the adder tree take advantage of the multiple ports to perform the MAC operations in parallel fashion. The amount of parallelism for our design is across the input channels.

\[
\text{ParallelOps} = N^{PW}_{\text{max}}_{\text{type}},
\]

where \(N^{PW}_{\text{max}}_{\text{type}}\) is the maximum input channel size across all the specific type (e.g. projection or expansion pointwise in the MobileNet-V2) of pointwise convolutions mapped to specific compute unit.

4.2 Network SoC Compiler

The Network SoC Compiler observes the network graph, the targeted hardware device, and existing pre-designed synthesizable C++ IPs for convolution, and then translates the network graph by grouping the convolutional operators into customized \(QNet\) CUs with respect to system architecture. It tweaks the hardware architectural knobs to maximize parallelism, fusing as many convolutional operators as possible to reduce the number of shared memory transactions, and increase the overlap between computation and memory latency. Based on the repetitive pattern, it wraps the convolution operators in four different heterogeneous CUs: ① The \textit{Head CU} generally consists of Normal Convolution followed by a special case of IRB which is only called once; ② The \textit{Body CU} invokes IRB since it has maximum repetitions based on the DSCNNs architectures; ③ The \textit{Tail CU} usually consists of pointwise convolution followed by Average Pooling to embed the features and make them ready in respect of size and shape for the classifier; ④ Finally, the mapping of Tail CU output to \(k\) classes is accomplished by \textit{Classifier CU}.

Below, we describe the details of Network SoC Synthesizer including, system architecture, memory organization, Heterogeneous \(QNet\) CUs, host code scheduling and CUs management.
Figure 10: System level architecture of DeepDive.

4.2.1 DeepDive System Architecture

As emphasized before, the convolutional operators of DSCNNs demonstrate a repetitive structural behavior wherein some either appear once, or they are repeated across the entire network. Depending on the recurrence of the convolutional operators, they are mapped to the Head, Body, Tail, and Classifier CU. Fig. 10 shows the system architecture of DeepDive Hardware Accelerator. Each CU has its own dedicated Direct Memory Access (DMA), and its parameters, such as array pointers, $N$, $M$, and $H$, can be configured at runtime via the control bus (e.g., AXI Lite Bus). After configuration, each CU can transfer the input/output features map and weights tensors via streaming channels (e.g., AXI HP Interface) through System Memory Management Unit (SMMU). The composition of CU is parameterized by the buffer shapes, data type widths, and the computation core, which are a few of the architectural knobs provided while designing the hardware accelerator. This makes our design scalable and reconfigurable for DSCNNs. We will discuss our hardware knobs and each CU’s internal composition in detail after we explain the memory transactions and management. The CUs are scheduled and pipelined to increase the concurrency.

4.2.2 Memory Organization

Each CU has its own dedicated buffer and scratchpad to handle its memory requirements. The memory layout of the on-chip buffers are designed to satisfy the data access pattern required by the convolutional operators, in order to minimize the pipeline depth implemented in the computation core. The memory transactions in the CUs can be categorized into two groups: ① memory to memory transaction, where data is burst read from DDR memory to PL memory, and ② memory to stream transaction, where data is streamed via DMA to or from PL memory. As an example, Fig. 11(a) demonstrates the memory transactions for Head CU targeted for MobileNet-V2. Convolutional network
parameters like weights, quantization parameters, and biases are burst read from DDR to PL buffers. The input/output feature maps are streamed from DDR to PL. Apart from memory transactions of input/output features between DDR and PL, the inter-CU data transfers within its operators also occurs in streaming fashion, where intermediate feature map data is streamed in-between different convolutional layers. Stream FIFO offers two main advantages, memory and computation latency overlap and data movement reduction between DDR and PL.

4.2.3 QNet Heterogeneous CUs

In this subsection, we will explain the heterogeneous CUs, and the available architecture knobs that can be tweaked based on hardware and performance constraints. As mentioned earlier, Network SoC Compiler creates four unique CUs for each DSCNNs. The CUs are completely parameterizable, and customizable, for scalability and flexibility. Following section describes each CU in detail. We also provide illustrative figures for the example of MobileNet-V2.

**Head CU**: DSCNNs tend to start with a particular pattern, which comprises of a fixed set of layers that are not recurrent in any other part of the network. As explained in the section 4.2.2, the Head CU has its own dedicated internal memory for buffers. The data transactions occur in memory-to-memory mode and the intermediate data streams between convolutional layers within the head CU. As an example, Fig. 11(a) demonstrates the Head CU for MobileNet-V2 model, which is composed of normal convolution followed by depthwise and pointwise convolution, all fused by FIFO stream. This CU is scheduled once during the course of any DSCNN implementation. After running the head of CU, the repeatable pattern will be merged and mapped to the Body CU explained in the next part.

**Body CU**: The Body CU is the most important CU within DeepDive’s system architecture. It is responsible for executing majority of DSCNNs blocks iteratively. As an example, the IRB, which is the most repetitive block of MobileNet-V2, is entirely mapped to the Body CU. The IRB consists of pointwise (expansion), depthwise, and pointwise (projection) layers, all running concurrently in a fused fashion within the Body CU. Fig. 11(b) shows the structure of this CU for MobileNet-V2. Upon examining the network graph of DSCNNs, we see that occasionally, the IRB needs to perform residual connections. Depending upon the network graph, DeepDive facilitates residual connections implementation within or outside the PL targeted device resources. The Body CU is parameterized so as to support both memory-bound IRBs, which ideally are earlier blocks of DSCNNs, and compute-bound IRBs, which tend to be later blocks of DSCNNs. Therefore, the network SoC compiler configures the Body CU with maximum buffer size needed by memory-bound IRBs, and maximum level of parallelism to meet the demand imposed by compute-bound IRBs. At the same time, the Body CU supports convolution operations with variable stride over different IRBs. These features increase the framework inclusiveness by supporting multiple IRB scenarios within the same DSCNN.

**Tail CU**: The Tail CU consists of the last layers of DSCNNs. The task of this CU is to make the embedded feature size ready for the dense layer implemented in the Classifier CU. Fig. 11(c) represents the structure of Tail CU in MobileNet-V2. This CU is comprised of a single pointwise convolution operator, followed by an average pool. As intermediate feature maps are streamed from layer to layer in a channel-wise fashion, the reshape block reorders the memory layout of the feature map in a column-wise mode. Therefore, the average pooling can accumulate the input on-the-fly and stream out.

**Classifier CU**: The last Compute Unit is the Classifier CU, which concludes the DSCNN implementation. Fig. 11(d) represents the MobileNet-V2 Classifier CU. Similar to others, this CU is parameterized such that the parallelism across the computing core can be adjusted based on the available hardware resources. Classifier CU comprises compute-bound operations and has a similar configuration to the pointwise convolutional operators.

4.2.4 Host Code Scheduling and CUs Management

Finally, the Network Soc Compiler also manages the host-level scheduling of CUs. Fig. 12 visualizes the CUs scheduling and their memory footprints on shared memory. The host or PS initializes the DDR with network models and quantization parameters. The DeepDive back-end generates the memory layout so that the network data region is shared between PL and PS. Therefore at each CU invocation, the PS only passes the data pointer, and the PL fetches the data based on the provided pointer rather than copying the data to its region. This memory layout will remove the necessity of copying data between the PL and PS memory region. The host starts scheduling procedure by configuring the Head CU with appropriate memory pointer addresses, offsets, network parameters, and network configuration.
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Figure 12: Host level scheduling and memory footprint of CUs.

i.e., $M, N, H$, which are compiled into network configuration header files. When Head CU completes execution, it writes back the data in feature tensors and interrupts the host CPU. Following the same trend, the host will schedule the Body CUs for $j$ times, where $j$ is the number of Body CU invocations calculated based on CU’s mapping. Host CPU then schedules the Tail CU, which executes the compute-bound operations quickly. And finally, the last call is to the Classifier CU, which will update the content of feature tensor needed by the softmax layer to calculate the confidence. Host CPU creates a sequential yet fused scheduling and management of CUs for DSCNNs.

5 Experimental Results

We have chosen the Xilinx Zynq UltraScale+ MPSoC ZCU102 evaluation board, which has XCZU9EG chip, to demonstrate the capabilities of DeepDive. The ARM processors host Ubuntu 16.04, running at 1.2GHz; the OS can program the FPGA fabric at runtime. We also use Vivado HLS 2018.3 to synthesize the network models compiled by DeepDive. The FPS and power consumption reported for DeepDive are based on QNet accelerator running at 200MHz. We targeted MobileNet-V2 and EfficientNet networks as two cases of DSCNNs. The Top-1 accuracy reported in this section is based on training and evaluating the network on the ImageNet dataset. Since the input image has a square shape, we reported only $H$ as input feature size. Later, we elaborate the design exploration and implementation of each one of these networks as a case study.

5.1 Case Study: MobileNet-V2

The procedure starts from a PyTorch model of MobileNet-V2, pre-trained on ImageNet. At DeepDive’s front-end, we configured the FPGA-aware training for different $BW$ based on the channel-wise asymmetric ranged linear quantization. Fig. 13 shows the Top-1 accuracy for MobileNet-V2 when its $\alpha = 0.75$ and $H = 160$. As can be seen, DeepDive maintains accuracy with respect to FP32 by reducing the $BW$ to 8 for first Normal Convolution, and 4 for the rest of the layers, respectively. The per layer-specific quantization compresses the model size with a ratio of 8, with 4.4% degradation in Top1 accuracy. The results demonstrate a dramatic drop in accuracy for $BW = 3$. For the rest of this case study, $BW = 4$, as it achieves competitive accuracy with considerably smaller model size.

5.1.1 Design Exploration

The front-end is configured to re-train, quantize, and calibrate the network for different $\alpha$ and $H$ values. Table 2 summarizes the model size, operation numbers and Top1 accuracy per each design point. Based on Table 2, we observe that model size is only effected by $\alpha$, while the number of operation number is a function of both $\alpha$ and $H$. Top1 accuracy is also a function of both $H$ and $\alpha$; however, it is not a linear relationship. For instance, design point $(H = 224, \alpha = 0.75)$ has better Top1 accuracy compared to design point $(H = 160, \alpha = 1)$ while its model size is 33%
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Figure 13: The effect of different computation types on Top1-accuracy and model size. Based on Fig. 13(a), UInt4 has almost accuracy similar to floating-point, while a notable drop can be observed for UInt3. Also, Fig. 13(b) shows integer quantization causes an exponential decrease in the model size.

Figure 14: Top1-Network Complexity Pareto front. Design point $(H = 96, \alpha = 1)$ has similar network complexity while its Top1 accuracy is less than $(H = 224, \alpha = 0.5)$.  

less than the latter one. Therefore, we introduce the network complexity as the product of the network model size and network operation number to consider both of them.

Fig. 14 depicts the Top1-Network Complexity Pareto front. The network complexity helps the front-end to measure the final hardware complexity at a higher level of abstraction. We annotate the starting point of each $\alpha$ in this figure and one non-Pareto point for the sake of comparison. Here, we observed that the design point $(H = 96, \alpha = 1)$ has approximately the same network complexity with respect to $(H = 224, \alpha = 0.5)$, while its Top1 accuracy is almost 4% less than top achievable accuracy.
Table 3: Effect of altering $\alpha$ and $H$ for fixed $BW = 4$ at 200Mhz on FPS and FPGA Resource Utilization

| $\alpha$ | 0.75 | 0.5 | 0.35 |
|----------|------|-----|------|
| $H$      | 224  | 192 | 178  |
| FPS      | 11   | 14  | 18   |
| Power(mW)| 460  | 450 | 440  |
| DSP(%)   | 57   | 57  | 58   |
| LUTs(%)  | 57   | 58  | 57   |
| BRAM(%)  | 96   | 96  | 97   |

5.1.2 Execution Results and Comparison

This subsection evaluates DeepDive’s execution performance for MobileNet-V2 on the Hardware Accelerator, different energy-efficient design points implementations, and finally provides a comparison against two other FPGA accelerators [12, 14]. Since there are no other solutions that support both MobileNet-V2 and EfficientNet, we also compare it against Nvidia’s Jetson Nano as existing state-of-the-art system.

Mapping: As discussed in section 4, based on the network graph generated by Network Compiler, DeepDive’s back-end identifies the mapping between the convolutional operators and heterogeneous CUs. Fig. 15 reveals the mapping of MobileNet-V2 to heterogeneous CUs. The Head, Tail, and Classifier CU are scheduled only once, but the Body is scheduled 16 times. Because of this, DeepDive allocates maximum resources to the Body CU to gain maximum performance. It makes the body CU support both memory-bound and compute-bound operations. For $\alpha = 1.0$, DeepDive was not able to fit the design in XCZU9EG SoC chip. If we configure the DeepDive to select different values, less than $N_{max}$ per operator, we observed a significant degradation in the final accelerator performance. Therefore, for the rest of this section, we did not consider these design points.

![Figure 15: MobileNet-V2 mapped to CUs.](image)

Energy efficiency: Here we configure the back-end to compile different network architecture by altering $\alpha$ and $H$. Multiple fully functional execution instances have been created for all configurations in Table 2, except when $\alpha = 1.0$.

![Figure 16: Power consumption difference between two mode.](image)
Table 4: Power Consumption and delay for MobileNet-V2

| H  | Power(W) Nano(H) | Power(W) Nano(L) | Power(W) DeepDive | Delay(ms) Nano(H) | Delay(ms) Nano(L) | Delay(ms) DeepDive |
|----|------------------|------------------|-------------------|-------------------|------------------|-------------------|
| 224| 5.49             | 2.64             | 0.46              | 14.91             | 20.73            | 88.49             |
| 192| 5.22             | 2.51             | 0.45              | 13.61             | 19.96            | 70.32             |
| 160| 4.78             | 1.88             | 0.44              | 13.07             | 19.6             | 54.45             |
| 128| 3.35             | 1.56             | 0.37              | 11.24             | 17.19            | 45.51             |
| 64 | 3.25             | 1.32             | 0.35              | 7.89              | 13.91            | 35.71             |

(H = 96, α = 0.35) has the lowest power consumption at 250mW, as compared to (H = 224, α = 0.75) with the highest power consumption at 460mW. Fig. 17 depicts Top1-Energy Efficiency (FPS/Watt) Pareto front. We only annotate the design points that have a higher than 50% accuracy. DeepDive enables us to understand the relationship between energy efficiency and accuracy. As we can see, design point (H = 160, α = 0.75) has almost the same FPS/Watt and Top1 accuracy with (H = 224, α = 0.5). Similarly, the next design point, (H = 192, α = 0.5), can improve energy efficiency by 45.14%, while the accuracy is dropped by only 2.48%. Based on the design points provided by DeepDive, it can be observed that by decreasing α and increasing the H, we can improve FPS/Watt without sacrificing the Top1-accuracy dramatically.

Figure 17: Top1-Energy Efficiency Pareto front. Design point (H = 192, α = 0.5) and (H = 128, α = 0.75) has similar energy efficiency while Top1 accuracy for (H = 192, α = 0.5) is more.

Comparison: To showcase the energy efficiency of DeepDive, we compare its FPS/Watt against off-the-shelf Nvidia Jetson Nano IoT Edge Device. We mapped the design points of Table 3 to TensorRT and obtained the metrics after its graph optimization and quantization. Similar to the DeepDive, we calculate the power consumption only for inference time. We compared the delay and power consumption between DeepDive and Jetson Nano in two different power consumption modes: high power, and low power. It can be seen that DeepDive consumes a lot less power when compared to Jetson Nano, as depicted in Table 4. Fig. 18 shows the comparison of the Jetson Nano energy efficiency against DeepDive for different input sizes while α = 0.75. DeepDive, on average, can improve the FPS/Watt 2.2× and 1.51× against high and low power mode, respectively. DeepDive outperforms Nano because: (1) DeepDive performs extreme bit quantization as opposed to nano which uses FP16; (2) Although, TensorRT optimized the network model to fuse convolutional operators, DeepDive groups the convolutional operators in heterogeneous CUs at higher granularity. This heterogeneity effectively reduces the shared memory transactions and overlaps both computing and memory latency; (3) DeepDive provides a customized dataflow for depthwise separable convolution as opposed to Jetson Nano which performs general matrix multiplication for depthwise convolution due to fixed systolic array implementation.

Table 5 provides a comparison between DeepDive configured with (H = 224, α = 0.75) design and other similar accelerators. Since VTA’s [14] architecture does not support depthwise convolution, they modify the MobileNet to have group convolutions instead of depthwise convolutions, coined MobileNetG. Their MobileNetG was not accessible; hence, there was no chance to present a straightforward comparison. However, we realized that ResNet-18 has almost same inference latency when compared to MobileNetG based on their results, so we decided to compare the energy efficiency of VTA running ResNet-18. As we can see, DeepDive can improve energy efficiency 2.27×. The instruction-
based scheduling approach, and versatile systolic array adopted by VTA, both need to consume more power to decode instructions and map layers to the ALU sequentially, which leads to more shared memory transactions and higher power dissipation. Similarly, we compare DeepDive with the hardware accelerator presented by [12]. DeepDive outperforms [12] by 37.25× in energy efficiency. This improvement is because of two main reasons: 1) Extreme bit-quantization, BN, and ReLU activation fusion accomplished by front-end which increases the efficiency of the hardware accelerator. 2) DeepDive groups the convolutional operators in the CUs at higher granularity to overlap the memory transactions and computations.

Table 5: Performance Comparison in Classification

| Design         | Network      | Platform | Freq. (MHz) | Speed (FPS) | Power (W) | Energy Efficiency (FPS/W) |
|----------------|--------------|----------|-------------|-------------|-----------|--------------------------|
| VTA [14]       | ResNet-18    | ZCU102   | 200         | 15.44       | 1.47      | 10.51                    |
| [12]           | 0.5 MobileNet| ZYNQ 7Z045| 100         | 1.38        | 2.15      | 0.6418                   |
| Ours           | MobileNet-V2 | ZCU102   | 200         | 11          | 0.46      | 23.91                    |

5.1.3 6-bit Data-path

To showcase the ability to create random bit data-paths, We reconfigure DeepDive to generate and synthesize the MobileNet-V2 for \(BW=6\) to understand the effect of different bit resolution on the final Top1 accuracy and the hardware efficiency. We observe that \(BW=6\) can improve the Top1 accuracy by 1.49%, while the effectiveness of the hardware (FPS/W) drops by 4.88% on the average.

Overall, DeepDive improves hardware efficiency by adopting customized functional blocks for depthwise and point-wise convolutions. Heterogeneous CUs also remove unnecessary memory transactions between the PL and shared memory by fused pipeline execution across layers within a block which decreases the power consumption, while improving the overall system performance.

5.2 Case Study: EfficientNet

The baseline EfficientNet model was intentionally designed to be larger than MobileNet-V2. While this might be ideal for state-of-the-art accuracy, it was not suitable for low-power embedded devices. Taking advantage of the compound model scaling factors introduced in [19], we were able to compress the model using smaller \(\alpha\), network depth, and \(H\), to achieve a model size capable of running on edge devices. The algorithmic details and hardware resource utilization of this model can be seen in Table 6.

Mapping: EfficientNet is structurally different as compared to MobileNet-V2. Fig. 19 shows the mapping of EfficientNet to the CUs. The squeeze and excitation convolutional operators are represented as PW-SQ and PW-EX, respectively. DeepDive takes advantage of EfficientNet architecture by fusing more convolutional operators together.
Table 6: Compressed EfficientNet Algorithmic Specs and FPGA Resource Utilization with fixed BW = 4, Frequency = 200 MHz

| Algorithmic Parameters | Hardware Parameters |
|------------------------|---------------------|
| $H$ | Parameters (Mb) | #Ops (M) | Top1 (%) | FPS | Power (mW) | DSP (%) | LUTs (%) | BRAM (%) |
| 128 | 7.81 | 4.914 | 55.02 | 35 | 150 | 90 | 80 | 68 |

EfficientNet comparatively has a larger body than the MobileNet-V2, with six layers fused. This mapping helps in achieving better performance by reducing more memory transactions by invoking the Body CU only nine times. For the case of EfficientNet, we excluded the classifier from mapping and also comparison.

Table 7: Power Consumption and delay for Compressed EfficientNet

| $H$ | Power(W) | Delay(mS) |
|-----|----------|-----------|
| Nano(H) | Nano(L) | DeepDive Nano(H) | Nano(L) | DeepDive |
| 128 | 5.61 | 2.22 | 0.15 | 6.581 | 12.6 | 28.57 |

**Energy Efficiency:** As we can see in Table 6, the number of body CU invocation is $1.78 \times$ less than MobileNet-V2, which leads to less power consumption and higher FPS due to fewer memory transactions. Table 6 shows DeepDive reaches to 35 FPS for a power consummation of 150mW. This model gives us the Energy Efficiency of 233.3 FPS/Watt.

**Comparison:** Table 7 compares the FPS/Watt against Nvidia Jetson Nano. For EfficientNet, DeepDive can improve the FPS/Watt $8.6 \times$ and $6.7 \times$ against high and low power mode, respectively. Based on the massively fused layers in Body CU, fewer memory transactions translates to more energy-efficient hardware.

6 Related Work

Modern CNN accelerators can be divided into two main categories: single compute engine [6, 7, 17, 23, 26, 28], and multiple streaming compute engines [1, 4, 20–22, 28]. Single compute-engine accelerators are typically a systolic array of processing elements (PEs) that execute the target CNN layer-by-layer sequentially. They have a versatile solution to support different CNNs with the cost of some execution deficiencies. In contrast, streaming architectures consist of multiple dedicated hardware blocks, customized for the target CNN’s layers running in producer/consumer fashion. While achieving relatively higher efficiency, they have less scalability to support different networks [3, 16].

Many recent frameworks have proposed a vertical design flow from algorithm to the hardware [14, 17, 21, 22, 28]. However, the primary focus is on optimizing classical CNNs with dense operation with regular memory access, such as YOLO and ResNet network family. One notable example of single-engine architecture is DNNWeaver [17]. It offers customizable, hand-optimized RTL templates capable of shrinking or expanding the architecture based on the target CNN workload and target device hardware constraints. The templates support common CNN layer operations such as standard convolution, pooling, and batch normalization. However, the design-flow is not autonomous as it requires the user to define the network topology and layer structure. Wei et al. [23] designed a novel 2D systolic array that localizes data shifting to between neighboring PEs. This removes the need for multiplexers and simplifies the routing complexity, allowing for higher throughput. They also employ a custom C-based front-end, which, similar to [17], requires user interaction to define the nested convolutional loop using custom pragmas in C++. The custom front-end makes it more challenging to integrate with existing high-level DNN libraries (PyTorch, TensorFlow, Caffe, etc). VTA is another
recently introduced approach, which presents a versatile hardware solution to support different dense CNNs. VTA enjoys the generality by adapting instruction-based scheduling and flexible systolic array. However, this generality leads to more power dissipation. Another aspect that should be considered is that solutions based on versatile systolic arrays intrinsically do not support depthwise convolutions due to introduced sparsity in these types of convolutions; thus, users need to convert the depthwise convolutions to group-convolution to execute a DSCNN on designs similar to VTA. All these succumb to more power dissipation and memory transactions, which lead to having an inefficient hardware solution for DSCNNs.

The design proposed in [30] presents a framework to minimize the complexity and the model size of dense CNN by mapping normal convolution to depthwise separable convolution. Similarly, TuRF [29] replaces standard convolution layers with depthwise separable convolution and applies layer fusion to enhance the performance of dense networks. The design presented by [2] is another hardware accelerator based on matrix multiplication and customized adder-tree to support MobileNet-V2. However, their fixed design platform is not scalable to support fast-growing and forthcoming DSCNNs. A parallel acceleration scheme proposed in [12], demonstrates computing reusability with design reconfigurability. However, the accelerator suffers from massive data movements due to frequent reads and writebacks to the DDR because of the lack of fused layer execution. Moreover, the design-flow is not autonomous and requires the user to define the layer structure. A MobileNet-V2 based hardware accelerator on FP32 computation is presented in [13]. DPU [24] is another solution to support MobileNet-V2 based on an optimized RTL hardware model with a dedicated operator for depthwise; however, it cannot be considered as a versatile solution to support DSCNNs due to lack of support for swish activation function and pointwise multiplication. To the best of our knowledge, none of the above approaches present a fully vertical framework to implement the state-of-the-art DSCNN architectures, e.g., EfficientNet family.

7 Conclusion

This paper introduced DeepDive, as a fully functional framework for an agile, power-efficient execution of DSCNNs on edge FPGAs. DeepDive offers a vertical algorithm/architecture optimization, starting from the network description model down to full system synthesis and implementation. At the front-end, DeepDive performs high-level optimization such as BN fusing, and Online channel-wise low-Bit quantization at extremely low-bit resolutions to bring FPGA-awareness when training DSCNNs. At the back-end, Network SoC Compiler receives the design properties from DeepDive’s front-end and generates a full design of the system for both hardware model and software host codes. To generate the optimized hardware for DSCNNs, the Network SoC Compiler uses pre-designed micro-architectural blocks for depthwise, pointwise, and normal convolution operators. For the results, we have synthesized, executed, and validated two state-of-the-art DSCNNs, MobileNet-V2 and EfficientNet on Xilinx’s ZCU102 FPGA board. The execution results demonstrated 47.4 and 233.3 FPS/Watt for MobileNet-V2 and a compact version of EfficientNet, respectively. These comparisons showcased how DeepDive improved FPS/Watt by 2.2 × and 1.51 × over Jetson Nano high and low power modes, respectively. It also enhances FPS/Watt about 2.27 × and 37.25 × over two other FPGA implementations.

As future work, we plan to improve the back-end of DeepDive to support cloud-based FPGAs such as Alveo family. We plan to extend support for multiple instances of Body CU to improve both latency and throughput. Each body could have a different level of parallelization based on the knobs introduced in Section 4.1. The host would also map the IRB layers to the body CUs based on the required computation power. Various Body CUs with varying degrees of parallelization could improve DeepDive without power and hardware resource compromises.

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