Digital photonics parity bit error detection system

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Abstract. The optical communication medium is emerging to be one of the potential replacements to the current electronic systems widely used today. This is due to its much higher data transmission with extremely low loss properties, not to mention that it is almost invulnerable to electromagnetic interference. In this paper we demonstrated our proposed design of a digital photonic parity bit error detection system, one of the fundamental digital electronic circuits used during long-range digital signal transmission. Silicon photonic micro-ring resonators are used as its core component, where each of the rings operates as a digital logic XOR mode, by taking advantage of the resonance shifting properties of the silicon waveguide. Dynamic response characterization has been carried out by simulating the proposed circuits at the data rate of 1Gbps, with the data sampling rate of 1.6THz, and clear timing waveform was generated to show that the proposed circuit operates as the parity bit error detection system.

1. Introduction
Digital electronic circuits have become one of the most important aspects of any CPU builds. However, with the exponential rise in technological development, many believed that electronic circuits have reached their limit, as the data transmission inside the circuit is limited to the speed of electrical signals traveling to the physical material. Optical channels, however, allows for the data transmissions at higher data rate (at the speed of Gbps), with lower channel transmission loss and relatively small crosstalk as well as electromagnetic interference [1, 2]. Photonic integrated circuit (PIC) is a circuit in which photonic devices used are built by taking advantage of the currently available CMOS fabrication technology, thus making it available for design and extensive research to be carried out. It also enables the circuit to be built based on different kinds of materials, in which Lithium Niobate (LiNbO3), as well as Galium Arsenide (GaAs), have been demonstrated [3, 4].

Amongst many of the digital logic circuits, combinational logic circuits are a group of logic circuits that is time-independent and can produce logical output operation instantaneously, with no feedbacks needed. Combinational logic circuits are commonly classified into three categories, arithmetic, and logical functions, data transmission and code converters. Amongst many combinational logic circuits, parity bit generator, as well as checker, are the two logic circuits used widely in binary serial transmissions. A parity bit is generated and embedded together with the data bits and sent to the receiving node. At the receiving end, number of bits are counted to detect errors in transmission, depending on the system, whether it is odd or even parity bit, errors in transmission will be detected. This has been researched and demonstrated in quantum dot applications for low power nanocommunications [5-7].
Several breakthroughs have been demonstrated in silicon photonics, where digital logic mode operations have been achieved by using the single mode Fabry-Perot laser diode (FP-LD) [8, 9]. However, such designs cannot be incorporated into on-chip CMOS level circuitry, thus micro-scale photonic micro-ring resonators are being implemented into digital logic circuits. We have also shown that one silicon micro-ring resonator can be used and configured to operate as digital logic AND, NAND, OR as well as NOR modes [10]. Several logic gates and circuits have also been demonstrated, where two symmetric micro-ring resonators are used to design directed OR/NOR and AND/NAND logic circuits [11], micro-ring resonators-based D type flip-flop [12], half adder [13], bit magnitude comparator and digital encoders [14, 15]. Micro-ring resonators have also been used in communication circuits such as WDM systems [16].

This paper presents the principal design of the digital photonic even parity bit checker circuit, by using silicon micro-ring resonator as its core element. The ring waveguide uses electro-optic effect based on free carrier plasma diffusion PIN diode setup. This work also details the time-varying simulation for both circuits at the data rate of 1Gbps in order to demonstrate that the proposed bit checker is working as desired.

2. Design Principle of the Proposed Error Detection Circuit

A 3-bit even parity error detection circuit is basically a digital parity bit checker that has a total of three digital logic XOR gates, where the first two XOR gates output is then fed into the third XOR gate, to generate a parity check ($C_P$) bit. In our proposed bit generator, we replaced the digital logic gates with silicon micro-ring resonators operating as digital logic XOR mode as shown in Figure 1. The equation representing the operation of the bit checker output is $C_P = (A \oplus B) \oplus (C \oplus P)$ and the entire operation bit by bit for the circuit is as shown in Table 1, where $C_P$ is only at digital logic state ‘1’ when the total number of logic state ‘1’ s for the received four bits is an odd number, indicating that the received information contains error.

![Figure 1](image-url)
Table 1. Even Parity Bit Checker Truth Table.

| A | B | C | P | CP |
|---|---|---|---|----|
| 0 | 0 | 0 | 0 | 0  |
| 0 | 0 | 0 | 1 | 1  |
| 0 | 0 | 1 | 0 | 1  |
| 0 | 0 | 1 | 1 | 0  |
| 0 | 1 | 0 | 0 | 1  |
| 0 | 1 | 0 | 1 | 0  |
| 0 | 1 | 1 | 0 | 0  |
| 0 | 1 | 1 | 1 | 1  |
| 1 | 0 | 0 | 0 | 1  |
| 1 | 0 | 0 | 1 | 0  |
| 1 | 0 | 1 | 0 | 0  |
| 1 | 0 | 1 | 1 | 1  |
| 1 | 1 | 0 | 0 | 0  |
| 1 | 1 | 0 | 1 | 1  |
| 1 | 1 | 1 | 0 | 1  |
| 1 | 1 | 1 | 1 | 0  |

Notice that in Figure 1, components labeled O/E is shown, which is the optical to electrical converter. This circuit converts the optical output power of 5dBm to electrical signal of 0.2V linearly, which can be achieved using PIN photodetector connected to electrical attenuator. PIN photodetector converts the optical signal to electrical signal linearly and electrical attenuator lowers the voltage to the desired level, which in this case is 0.2V.

3. Design Architecture of the Silicon Micro-Ring Resonator

![Diagram](attachment:image.png)

Figure 2. (a) Architecture of silicon micro-ring resonator. (b) Schematic setup for XOR and XNOR mode operation.
The silicon micro-ring resonator we used is the PIN diode structure ring waveguide to facilitate the shift in resonance properties of the silicon material [17]. The ring is constructed with a ring length of 31.8um, with its initial effective index of 2.77 and its group index of 3.961. The coupling coefficient is found to be 0.5. The ring waveguide is doped accordingly so that free carriers can be injected into the waveguide’s core, thus effectively changing its effective index. Initial simulation for the ring shows that the ring propagation loss is 5.93dB/cm. The modulation voltage polarity is set up so that the positive terminal is connected to the p-doped side of the ring waveguide, while the electrical negative terminal is connected to the other n-doped side of the ring waveguide, as shown in Figure 2(a). The change in effective index versus the modulation voltage applied to the ring is as shown in Figure 3, where there is no major change in effective index from 0V up to 0.7V, but there is a linear change in effective index from 0.8V up to 1.4V [18]. This change in effective index profile can then be used to design the ring so that it operates as digital logic XOR mode.

![Graph showing change in effective index versus modulation voltage applied to the ring.](image-url)

**Figure 3.** Change in effective index versus modulation voltage applied to the ring.

However, since there are two electrical input signals to be fed into the ring resonator, we used electrical voltage adders to add the two electrical signals and finally fed the signal to the ring, as shown in Figure 2(b). Based on our previous research, we can obtain XOR mode operation by taking the drop port output and applying three voltage levels, 0.9V, 1.1V and 1.3V so that the resonance spectra for the drop port looks like shown in Figure 4. The working wavelength we selected is the resonance wavelength when the voltage applied is 1.1V, which is 1550.3nm. When the voltage applied is 0.9V, the optical output power at working wavelength is at logic state ‘0’ (optical power = -11.7dB). When the voltage applied is 1.1V, the optical power at working wavelength is at logic state ‘1’ (optical power = -2.15dB), and when the voltage is 1.3V, the resonance shifted even more, thus at working wavelength, the output is at logic state ‘0’ again (optical power = -11.2dB). With these voltages, together with a constant voltage source of 0.9V, and each of the input shown in Figure 3(b) is at amplitude of 0.2V, we can achieve the XOR mode operation with a single silicon micro-ring resonator.
4. Dynamic Response Test

The proposed circuits were then tested in one of the commercially available photonic simulation software, Lumerical INTERCONNECT. The ring resonators are injected with a single wavelength light source of 1550.3nm with the optical power of 5dBm. Four digital bit signal generators are used to generate predetermined bit information with the amplitude of 0.2V, where the input A received the repeating \((0000000011111111)\)\(_2\), while input B received a repeating \((0000111100001111)\)\(_2\) with input C is injected with a repeating information signal of \((0011001100110011)\)\(_2\) and finally the parity bit input signal is generated with repeating information of \((0101010101010101)\)\(_2\). A single PIN photodetector is used to convert the optical output signal P to an electrical signal, in which 1dBm of optical light power is linearly converted into 1V of electrical voltage signal. The entire simulation setup for the bit checker circuit is as shown in Figure 5.

![Diagram](image)

**Figure 5.** Simulation block setup for the bit checker.
Figure 6. Timing waveform for the proposed bit checker.

Figure 6 shows the timing waveforms for all the input as well as output signals received from the simulation that have been carried out with the setup in Figure 5. The time window for the simulation is 20ns with the data injection rate of 1Gbps in order to demonstrate our proposed circuit operation. Predetermined electrical inputs are as shown in (a), (b), (c) and (d), while the parity bit error signal was generated as shown in (e), where each data iteration is in accordance with the truth table shown in Table 1. Based on the generated output, we measured the highest logic ‘1’ power level to be 4.3dBm while the highest logic ‘0’ power level to be 1.3dBm. If we are to consider the logic ‘1’ power level to be within 4dBm to 5dBm and logic ‘0’ power level to be within 0dBm up to 1.3dBm, then the generated result is as desired for our target of designing the parity bit checker error detection circuit.
5. Conclusion
This paper has presented the circuit design of a digital photonic parity bit error detection system with silicon micro-ring resonator as its base element. We have shown that the micro-ring resonator used is following the free carrier plasma diffusion electro-optic effect, where no change in the effective index when the voltage applied to it is within 0V up to 0.7V, and a linear change is observed from 0.8V up to 1.4V. We have also detailed the use of the micro-ring resonator to operate as a digital logic XOR mode by using electrical adder as an extra essential component. This XOR mode operated micro-rings were then used and replaced the logic gates in the digital bit checker. Dynamic response characterization has also been carried out with the predetermined digital input signals at the data rate of 1Gbps in order to demonstrate that our proposed circuit operates as digital parity bit checker, which yields the clear timing waveform results following the operation summarized by the digital bit checker truth table.

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