Wafer-scale low-disorder 2DEG in $^{28}\text{Si}/\text{SiGe}$ passivated by dichlorosilane

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(Dated: February 17, 2022)

We grow $^{28}\text{Si}/\text{SiGe}$ heterostructures by reduced-pressure chemical vapor deposition and use dichlorosilane chemistry for passivating the SiGe barrier at 500 °C, rather than for growing an epitaxial Si cap at a higher temperature. As a result, $^{28}\text{Si}/\text{SiGe}$ heterostructure field-effect transistors feature a sharp semiconductor/dielectric interface and support a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 nm wafer. At $T = 1.7 \text{K}$ we measure a high mean mobility of $(1.8 \pm 0.5) \times 10^5 \text{cm}^2/\text{Vs}$ and a low mean percolation density of $(9 \pm 1) \times 10^{10} \text{cm}^{-2}$. From the analysis of Shubnikov–de Haas oscillations at $T = 70 \text{mK}$ we obtain a long single particle relaxation time of $6.1 \text{ps}$, corresponding to a quantum level broadening of only $(34 \pm 1) \mu\text{eV}$, and a high quantum mobility of $(5.6 \pm 0.1) \times 10^5 \text{cm}^2/\text{Vs}$, indicating reduced scattering from long range impurities and a low-disorder environment for hosting high-performance spin-qubits.

Strained $^{28}\text{Si}/\text{SiGe}$ heterostructures are a compelling platform for scalable qubit tiles based on gate-defined quantum dots.[1, 2] In these $^{28}\text{Si}$ buried quantum wells, electron spins experience a quiet electrical and magnetic environment. The electronically noisy semiconductor/dielectric interface is far away, separated from the quantum well by a SiGe epitaxial barrier, and the nuclear spins have been removed by isotopic enrichment. Continuous advances in the material science of $^{28}\text{Si}/\text{SiGe}$ and improved device fabrication have enabled quantum logic with spin qubits crossing the surface code threshold.[3–5] Coherent coupling of two electron spins at a distance via virtual microwave photons,[6] and CMOS-based cryogenic control of quantum circuits.[7] In the mainstream approach to quantum dot fabrication, the last step in the heterostructure growth cycle comprises the heteroepitaxial deposition of a thin Si cap on the SiGe barrier.[8] This is to avoid the formation of low-quality Ge-based oxides upon exposure of SiGe to air. After the Si cap deposition, a high-$\kappa$ dielectric is deposited ex-situ and at low-temperature ($\approx 300 \text{ °C}$) to insulate the gate from the buried and undoped quantum well. This low-temperature process preserves the strain in the quantum well but induces large concentrations of impurities at the critical semiconductor/dielectric interface. These impurities can influence the electrostatic confining potential landscape induced by the gates, leading to the formation of unintentional quantum dots.[9] and are a source of charge noise limiting qubit performance.[10–11] While efforts have focused on achieving uniform and high-purity $^{28}\text{Si}$ quantum wells with sharp interfaces,[12–14] now more attention is needed to optimize the step which terminates the heterostructure deposition cycle and has a critical role in defining the semiconductor/dielectric interface.

In this letter, we explore $^{28}\text{Si}/\text{SiGe}$ heterostructures passivated by dichlorosilane ((DCS) chemistry at a temperature well below the threshold for growing Si. By avoiding the growth of a Si cap altogether, we obtain $^{28}\text{Si}/\text{SiGe}$ heterostructure field effect transistors (H-FETs) with a sharp semiconductor/dielectric interface. We show that the $^{28}\text{Si}$ quantum well supports a two-dimensional electron gas with less disorder and improved quantum transport properties compared to heterostructures with a Si cap deposited with DCS chemistry at higher temperatures.

Figure 1(a) illustrates the workflow to fabricate $^{28}\text{Si}/\text{SiGe}$ H-FETs. We grow $^{28}\text{Si}/\text{SiGe}$ heterostructures on 100 mm Si(001) wafers using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. We use isotopically-enriched $^{28}\text{SiH}_4$ for growing the $^{28}\text{Si}$ quantum well (residual $^{29}\text{Si}$ concentration of 0.08%[3, 7, 15]) and DCS ($\text{H}_2\text{SiCl}_2$) and $\text{GeH}_4$ for all other layers. The heterostructure comprises a 3 μm step-graded $\text{Si}_{1-x}\text{Ge}_x$ layer (final $x = 0.3$), a 2.5 μm $\text{Si}_{0.7}\text{Ge}_{0.3}$ strain-relaxed buffer, a 8 nm tensile-strained $^{28}\text{Si}$ quantum well and a 30 nm $\text{Si}_{0.7}\text{Ge}_{0.3}$ barrier. To achieve sharp interfaces and minimize Si/Ge interdiffusion, the temperature is decreased from 750 °C for growing the quantum well to 625 °C for the barrier. We now introduce a major difference compared to our previous experiments. In Refs. [3, 7, 12, 15] we used DCS chemistry at 675 °C to grow a thin Si cap. Here we reduce the substrate temperature to 500 °C, below the desorption temperature of chlorine from the surface (600–650 °C),[17, 18] under the same conditions of DCS fow and pressure. According to literature[19–23], we expect that DCS chemistry at 500 °C essentially suppresses growth but provides a Si-rich passivation layer for $\text{Si}_{0.7}\text{Ge}_{0.3}$. After terminating the deposition cycle with this passivation step, the heterostructure is removed from the growth reactor and a native oxide is formed upon exposure to air at room temperature. We identify the native oxide as $\text{SiO}_x$ based on the chemical analysis in Fig. 1(c),(d). Then, we fabri-
A Hall-bar shaped H-FETs using the process described in Ref. [12]. In short, the process comprises the implantation of ohmic contacts and rapid thermal annealing at 700 °C, the atomic layer deposition at 300 °C of a 10 nm Al2O3 dielectric layer on the SiOx, and the final deposition of a Hall-bar shaped metallic gate, electrically insulated from the heterostructure by the SiOx/Al2O3 dielectric stack.

Figure 1(b) shows a high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the heterostructure and of the dielectric stack under the gate stack. The Si quantum well is uniform, without extended defects, and is characterized by sharp top and bottom interfaces to the Si0.7Ge0.3 layers, in agreement with our previous reports.[3, 7, 12] The semiconductor/dielectric interface is similarly sharp with a strong dark/light contrast due to the atomic-weight sensitivity of HAADF-STEM. Two distinct amorphous layers, which we identify as the SiOx and AlOx layers, appear on the dielectric side of the interface. We gain insights over the nature of the semiconductor/dielectric interface and of the dielectric stack by performing Electron Energy Loss Spectroscopy (EELS) with high energy resolution (≈ 1 eV). In Fig. 1(c) the Si (blue) and Ge (red) concentration profiles decrease together whilst the oxygen (green) signal is increasing. We deduce that oxidation of the DCS-passivated Si0.7Ge0.3 barrier results in a sharp SiGe/SiOx semiconductor/dielectric interface. This is confirmed by the minor Ge pile-up on the semiconductor side of the interface,[26, 27] which appears as a dark line in HAADF-STEM [Fig. 1(b)]. Furthermore, the Al signal (black line) rises after the Si signal from SiOx has trailed, indicating that the dielectric stack retains the two distinct SiOx and AlOx layers.

In Fig. 1(d) we show the chemical mapping by EELS of Si (blue), SiOx (magenta), and AlOx (green) along and across the semiconductor/dielectric interface, together with the intensity profiles. The SiGe/SiOx interface is sharp throughout the image, whereas the SiOx/AlOx interface shows some interdiffusion. By fitting the intensity profiles with exponential functions,[28] we characterize the sharpness of the interfaces with the leading (towards the surface) and trailing (from the surface) exponential slopes $\lambda_L$ and $\lambda_T$. We find $\lambda_L^{SiOx} = (1.0 \pm 0.1)$ nm and $\lambda_T^{SiOx} = (0.8 \pm 0.1)$ nm, indicating a sharp transition from epitaxial to amorphous layers at the SiGe/SiOx interface. Conversely, we find $\lambda_L^{AlOx} = (1.9 \pm 0.1)$ nm and $\lambda_T^{AlOx} = (3.1 \pm 0.2)$ nm, pointing to a degree of intermixing between the two dielectrics at the SiOx/AlOx interface.

We characterized the H-FETs by magnetotransport measurements at a temperature of 1.7 K and 70 mK in refrigerators equipped with cryo-multiplexers.[29] With this approach, we measure multiple devices from a wafer in the same cool-down. The devices are operated in accumulation mode, in which electrons populate the undoped 28Si quantum well by applying a positive DC gate voltage ($V_G$). We measure the longitudinal and transverse component of the resistivity tensor, $\rho_{xx}$ and $\rho_{xy}$, by using standard four-probe lock-in techniques at fixed AC source-drain bias of 100 µV. We calculate the longitudinal $\sigma_{xx}$ and transverse $\sigma_{xy}$ conductivity via tensor inversion. We measure electron density ($n$) and mobil-
ity (μ) with the classical Hall effect at low perpendicular magnetic field B.

Figure 2(a) shows for a typical device the turn-on and pinch-off source-drain current $I_{SD}$ as a function of increasing and decreasing $V_G$, respectively. Above a threshold voltage ($V_G = 350 \text{ mV}$), the current starts flowing in the channel and increases monotonically. If the gate voltage is operated within the operational gate voltage range $\Delta V_G$ (red curve), $I_{SD}$ is stable and the threshold and pinch-off voltages overlap. At higher $V_G$, $I_{SD}$ saturates due to charge build-up at the semiconductor/dielectric interface, triggering hysteresis and, consequently, a shift in pinch-off voltage. As shown in Fig. 2(b), if $V_G$ is swept within the operational gate voltage range, $n$ increases linearly with $V_G$ up to $6 \times 10^{11} \text{ cm}^{-2}$, from which we derive a constant effective capacitance of $C \approx 205 \text{ nF/cm}^2$. This is consistent with a parallel-plate capacitor model where the 2DEG in the $^{28}\text{Si}$ quantum well and the metallic top gate are insulated by a SiGe/SiO$_x$/AlO$_x$ dielectric stack. Figure 2(c) shows the density-dependent mobility measured in the same density range as in Fig. 2(b). The mobility increases steeply at low density due to increased screening of long-range scattering from remote impurities, likely at the semiconductor/dielectric interface. At higher density, the mobility becomes limited by short-range scattering from impurities within or nearby the quantum well and approaches saturation at a value above $2.5 \times 10^5 \text{ cm}^2/\text{Vs}$.

In Fig. 2(d)–(f) we plot the distributions of the maximum electric field ($E_z^{max}$), the percolation density ($n_p$), and the mobility at high density for heterostructures passivated with DCS chemistry at $500 \degree \text{C}$ (blue) and, as a benchmark, for heterostructures with a Si cap grown by DCS chemistry at $675 \degree \text{C}$ (red). These metrics are obtained from the analysis of measurements in Fig. 2(a)–(c). $E_z^{max}$, calculated as $C\Delta V_G/\epsilon_0$ (where $C$ is the maximum electric field that we can apply to the H-FETs before hysteresis. Large $E_z^{max}$ are desirable for device stability, increased tunability, and large valley splitting. $n_p$ characterizes disorder in low density regime, relevant for quantum dot operation, and is obtained by fitting the density-dependent $\sigma_{xx}$ to percolation theory. Finally, the mobility at high density is a probe for disorder arising from within or nearby the quantum well. Overall, H-FETs perform better when the heterostructures are exposed to DCS chemistry at $500 \degree \text{C}$. We measure a 9% increase in mean $E_z^{max}$, 7% decrease in mean percolation density, and a 40% increase in mean average mobility. Most importantly, we observe a reduction in the spread of $E_z^{max}$, $n_p$, and $\mu$ of $\approx 300\%$, $\approx 200\%$, and $\approx 30\%$ respectively, pointing to an increased uniformity on a 100 mm wafer scale.

We further characterize disorder in the $^{28}\text{Si}/\text{SiGe}$ heterostructure at 70 mK by measuring the single-particle relaxation time $\tau_q$ in the quantum Hall regime for the H-FET with the highest mobility. From $\tau_q$ we derive the quantum level broadening of the momentum eigenstates $\Gamma = h/2\tau_q$ and the quantum mobility $\mu_q = e\tau_q/m^*$, where $e$ is the elementary charge and $m^*$ is the effective mass. $\mu_q$, associated with $\tau_q$, is influenced by all scattering events and is different from the mobility $\mu = e\tau_t/m^*$, where the scattering time $\tau_t$ is unaffected by forward scattering. Therefore $\tau_q$ and $\mu_q$ qualify the disorder in the heterostructure more comprehensively than $\tau_t$ and $\mu$. Figure 3(a) shows a measurement of $\rho_{xx}$ plotted for clarity against the Landau level filling factor $\nu = \hbar n/\epsilon_B$, where $\hbar$ is the Plank constant. This measurement was performed at fixed density $n = 4.75 \times 10^{11} \text{ cm}^{-2}$ by keeping $V_G$ constant and sweeping $B$. Onset of Shubnikov–de Haas oscillation, Zeeman splitting, and valley splitting occurs at 0.125, 0.43, and 1.15 T, respectively, corresponding to $\nu = 152, 42$ and 17. The observation of Shubnikov–de Haas oscillations, Zeeman and valley split-
Figure 3. (a) Longitudinal resistivity \( \rho_{xx} \) measured at \( T = 70 \) mK as a function of Landau level filling factor \( \nu \). These measurements are performed at fixed \( n = 4.75 \times 10^{11} \text{ cm}^{-2} \) while sweeping the perpendicular magnetic field \( B \). Spin and valley degenerate Landau levels correspond to \( \nu = 4k \) (\( k = 1, 2, 3, \ldots \)), Zeeman split levels to \( \nu = (4k-2) \), whereas valley split levels correspond to odd integer filling factors \( \nu \). Arrows indicate the filling factors at which Zeeman spin splitting and valley splitting are resolved. The red dashed line is the theoretical fit of the oscillations envelope to the function \( \Delta \rho_{xx}/\rho_0 = \frac{\rho_0 \chi(T)}{4 \rho_0} \exp(-\pi/\omega_c \tau_q) \), where \( \chi(T) = \frac{(2\pi k_B T/\hbar \omega_c) \sinh(2\pi k_B T/\hbar \omega_c)}{(2\pi k_B T/\hbar \omega_c)} \), \( k_B \) is the Boltzmann constant, \( \hbar \) is the reduced Planck constant, \( \omega_c \) is the cyclotron frequency and \( T \) is the electron temperature (Fig. 3(b), red curve).\[37\]\[38\] The Dingle plot of Fig. 3(c) reports the fit from which we extract \( \tau_q = 6.1(1) \) ps. Accordingly, we derive \( \mu_q = 5.6(1) \times 10^4 \text{ cm}^2/\text{Vs} \), and \( \Gamma = 34(1) \) meV, setting a benchmark for Si-based materials supporting spin-qubits. We find a Dingle ratio \( \tau_\ell/\tau_q \approx 4.8 \), indicating reduced long-range scattering, likely as a consequence of the improved semiconductor/dielectric interface associated with the low-temperature passivation process in this heterostructure.

In summary, we challenged the mainstream approach to deposit a Si cap on \( ^{28}\text{Si}/\text{SiGe} \) heterostructures and, instead, we passivated the SiGe barrier by DCS chemistry at low temperature. Compared to previous heterostructures that have already produced high performance spin qubits,\[3\][7], we demonstrate an improvement in performance of H-FETs in terms of mean value and spread of mobility, percolation density, and maximum electric field before hysteresis. Furthermore, we demonstrate that these heterostructures support 2DEGs with very low-disorder, characterized by early onsets of the Shubnikov–de Haas oscillations and long single-particle relaxation time. By having a better semiconductor/dielectric interface and wafer-scale uniformity, we expect that this material stack may lead to Si spin qubits with improved yield and performance. These results motivate new studies to understand in detail the nature of DCS-passivated SiGe and to use this knowledge as a tool for further optimizing the semiconductor/dielectric interface.

This research was supported by the European Union’s Horizon 2020 research and innovation programme under the grant agreements No. 951852 (QLSI project), and in part by the Army Research Office (Grant No. W911NF-17-1-0274). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office (ARO), or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein. This work is part of the research program OTP with project number 16278, which is (partly) financed by the Netherlands Organisation for Scientific Research (NWO).

Data sets supporting the findings of this study will be available at [10.4121/19181597](https://doi.org/10.4121/19181597)

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