With the continued scaling of CMOS devices below the 10 nm node, process technologies become more and more challenging as the allowable thermal budget for device processing continuously reduces. This is especially the case during epitaxial growth, where a reduction of the thermal budget is required for a number of potential reasons for example to avoid uncontrolled layer relaxation of strained layers, surface reflow of narrow fin structures, as well as doping diffusion and material intermixing. Further aspects become even more challenging when Ge is used as a high-mobility channel material and when the device concept moves from a FinFET design to a nanowire FET design (also called Gate-All-Around FET). In this contribution we address some of the challenges involved with the integration of high mobility Group IV materials in these advanced device structures.

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With continued scaling beyond the 10 nm node, MOS device complexity increases and novel channel materials, such as epitaxial Ge for pMOSFETs and epitaxial Ge or IIIV for nMOSFETs, are being considered.1–7 These so-called high mobility materials are implemented in new device concepts and novel architectures, for example tunnel FETs and gate-all-around devices, in order to meet the power and performance requirements. Reference 7 gives an overview of the innovations in materials and new device concepts that will be needed to continue Moore’s law to sub-7nm technology nodes. The high mobility material can be a single material (e.g. Ge) or a combination of different materials, such as compressively strained Ge grown on top of a SiGe-Strain Relaxed Buffer (SRB), which allows the formation of a heterojunction. The latter can be used to form a quantum well structure aiming at improving the electrostatics in the final transistor by confining the carriers in a region which is fully controlled by the high mobility material. A carefully designed epitaxial Source/Drain stressor contact allows to increase the uni-axial strain in the channel, although it needs to be taken into account that this strain engineering technique becomes less efficient with reducing device dimensions especially the contact to poly pitch.12,13 This resulted in a renewed interest in the use of SiGe SRBs as virtual substrate for the introduction of compressive stress in the Ge channel.

Figure 1 shows a typical example of a strained Ge p-type FinFET device. Device fabrication consists of three or four epitaxial growth steps with two common approaches: STI-first or STI last. The STI-first approach (also known as replacement channel approach) starts with the formation of the Si Shallow Trench Isolation (STI). Next, the Si is partly removed using either an in-situ HCl vapor etching1,2 or an ex-situ wet chemical etching routine.3,4 The recessed Si is replaced by the high mobility material. Subsequent oxide recess is then used to reveal the fin. As mentioned above, the high mobility material can be a single material (e.g. Ge) or a combination of different materials, such as compressively strained Ge grown on top of a SiGe SRB. It has been shown that the high aspect ratio of the STI trench can be used to trap the defects at the bottom of the trench and the STI sidewalls.2,5,6 In this case, a single SiGe layer is used as virtual substrate. This aspect ratio trapping typically works well perpendicular to the trench, but along the trench innovations in epitaxial growth are needed to reduce the number of defects. The second epi step is the deposition of a Si-passivation layer on top of the different fin surfaces, which is one possible way to improve the high-k/channel interface.7,8,9,10 The process flow also contains the epitaxial growth of the Source/Drain contacts to increase the uni-axial strain in the channel, although the strain engineering technique becomes less efficient with reducing device dimensions.11,12 Reduced device dimensions set also a clear need to reduce the S/D contact resistivity as this might limit device performance.13–16

The STI last approach enables to fabricate devices with a lower defect density in the active part of the device. The first step in the creation of strained Ge pMOS devices is the STI fabrication in blanket wafers containing a strained Ge layer epitaxially grown on top of a (step-) graded SiGe SRB. During the last years, efforts have been made to improve material quality of SiGe SRBs by controlling the threading-dislocation density and the propagation of dislocations e.g. by the deposition of a back side stressor layer before epitaxial growth of the SiGe SRB.23,24 A limitation of this approach is the difficulty to combine different materials for n- and p-MOSFETs on one substrate. This is easier in case of the STI-first approach, which is based on the replacement of the Si material by selective epitaxial growth (SEG) of the high mobility material.6

![Figure 1. Scheme of a strained Ge p-type FinFET device.](image-url)
As scaling continues, FinFET devices will also suffer from subthreshold degradation.\textsuperscript{23} From these nodes on, nanowire or gate-all-around (GAA) FETs (Fig. 2) are expected to have clear advantages of subthreshold slope compared to a FinFET device at the same gate length.\textsuperscript{25–27} Their production promises little deviation from a standard FinFETs processing flow, but a significant improvement of the electrostatic properties. The process scheme of our Si and Ge GAA FETs starts with the deposition of a stack of two materials on blanket wafers (STI-last approach), typically Si/SiGe on Si and SiGe/Ge on graded SiGe-SRBs. An ultimate scaling of this technology assumes the use of either Si or Ge and SiGe with high Ge content close to 50%. Epitaxial growth is challenging as the large lattice mismatch sets a need for low process temperatures to avoid strain relaxation.

In this manuscript we address some of the challenges involved with the integration of high mobility Group IV materials in these advanced device structures with a main focus on the epitaxial growth schemes.

Experimental

The epitaxial layers were grown in either an ASM Epsilon 3200 or in ASM Intrepid epi reactors.\textsuperscript{28,29} These are standard horizontal cold wall, load-locked Reduced Pressure Chemical Vapor Deposition (RP-CVD) single wafer systems designed for production applications. The ASM Epsilon 3200 is a stand-alone reactor. On the ASM Intrepid up to four process modules can be configured, including the Premium integrated low-temperature surface cleaning module which offers a solution for low temperature oxide removal from the starting surface.\textsuperscript{30} A broad range of process gases are available and the selection was based on the specific needs for the given epitaxial layer. The details of the device fabrication schemes are described in Ref. 1.2,4,6,7,15,22,27.

High Resolution X-Ray Diffraction (HRXRD) measurements were performed using a Bruker JVTX7300ML X-ray metrology tool. The tool is equipped with both a large X-ray beam for measurements on blanket wafers and large arrays of fin structures, as well as a medium spotsize beam suitable for measurements on patterned wafers. Switching between sources is fully automated within recipes, and both sources were used in this work. For standard monitoring, regular $\omega$-20 scans and $\omega$ rocking curves were used. Additionally, we acquired reciprocal space maps (RSMs) around asymmetric reflections along and perpendicular to the fins in order to determine the lattice parameters and hence relaxation/strain values for the various layers in all three directions.\textsuperscript{6,15,31}

Results and Discussion

Selective growth of relaxed Ge in narrow STI trenches.—Some years ago, we described the issue of Ge thermal instability against surface migration during epitaxial Ge growth by means of CVD in extremely narrow channels isolated by SiO$_2$.\textsuperscript{32,33} In wide structures, Ge trench filling after Si recess is possible, although facet formation is more pronounced at higher growth temperatures.\textsuperscript{24} For extreme narrow trenches a critical growth temperature exists, above which filling is prohibited by Ge migration over the surface (Fig. 3a) due to the high Ge chemical potential in such narrow channels. The Ge thermal instability in terms of surface migration out of the narrow trench depends on the fin design and the channel width. For structures with contact pads, we extracted a critical channel width of 50 nm from both simulations and experimental results.\textsuperscript{32} The Ge surface migration rate is dominated by the surface diffusion activation energy barrier that is significantly enhanced by the adsorbed surface hydrides. During epitaxial Ge growth at a temperature below 450$^\circ$C and using GeH$_4$ as Ge precursor, a hydride-terminated surface is maintained which increases the Ge surface diffusion barrier and retards the migration of the Ge ad-atoms, providing excellent channel filling (Fig 3b). However, epitaxial Ge grown at such a low temperature contains twin defects which have been generated at the vertical SiO$_2$/Ge interface (Fig. 3a). These twin defects are only partially removed after post epi thermal treatments. In addition, the growth against the STI-oxide side wall might be disturbed resulting in a very irregular Ge layer.

More recently, we described the effect of the fin design on the epitaxial growth process\textsuperscript{35} and especially the strong influence on the Ge migration inside the narrow trench due to presence/absence of large Source/Drain contact pads. Source/Drain contacts act as a “sink” for mass transport as it has a lower chemical potential (Fig. 3). For fin structures without Source/Drain contacts (Fig. 5), the driving force for
Ge diffusion out of the trench is lower. This leads to an increase of the critical growth temperature, above which filling of narrow trenches is prohibited by Ge migration. This is critical as maintaining material quality sets a lower limit on the growth temperature. Indeed, the slight increase in growth temperature results in an impressive improvement of the Ge crystalline quality. No twin defects are seen in cross section Transmission Electron Microscopy (TEM) graphs (Fig. 4b) and the surface morphology is significantly better (Fig. 5).

Selective growth of strained Ge-cap/relaxed SiGe SRBs.—Similar limitations need to be taken into account for the SEG of compressively strained Ge on top of a Si$_{0.3}$Ge$_{0.7}$ SRB. The SiGe and Ge growth temperatures have to stay below mask design dependent critical values to avoid surface reflow out of the STI trench. In addition, the reduced STI depth, used for high density fins, restricts the thickness of the SiGe SRB layer. The use of a V-shaped Si recess, eventually combined with the deposition of a Ge-rich SiGe seed layer before the SRB growth, allows to reduce the Si$_{0.3}$Ge$_{0.7}$ SRB thickness down to $\sim$55 nm while maintaining full strain relaxation (Figs. 6, 7). To investigate the strain state in more detail, reciprocal space maps (RSMs) were performed both along (longitudinal) and across (transverse) the fins. RSMs measured on optimized strained Ge/Si$_{0.3}$Ge$_{0.7}$-SRB fins (Fig. 7), show that the single SiGe layer is relaxed in both in-plane directions while the Ge channel is fully strained w.r.t. the SiGe SRB in the direction along the fin. The uni-axial strain in Ge was confirmed by Nano Beam Diffraction (NBD) measurements. The TEM cross-section along the fin shows that the dislocations are mainly confined to the Si$_{0.3}$Ge$_{0.7}$-SRB/Si-substrate interface. On the other hand, some stacking faults which are propagating into the Ge are visible in Figure 6b. The V-shaped Si recess also results in an improved uniformity of the Ge concentration within the SiGe-SRB in comparison to a “flat” Si recess. In case of Si recess by in-situ vapor etching, the Si$_{0.3}$Ge$_{0.7}$ growth starts from a (001) surface. During Si$_{0.3}$Ge$_{0.7}$ growth, {111} facet formation cannot be suppressed. The slightly higher Ge incorporation on (111) surfaces, compared to (001) surfaces, explains the non-uniform Ge incorporation within the SiGe SRB as seen in Figure 8a. In this case, the dislocation network is less confined to the Si$_{0.3}$Ge$_{0.7}$-SRB/Si-substrate interface and the number of threading dislocations reaching the strained Ge-cap layer is higher (Fig. 8b). The asymmetric shape

![Image](image_url)
for Ge channels seen in Figure 8a is due to the angle of the left and right STI sidewalls being slightly different from the trench etch. This asymmetry was not seen for wider trenches and for narrow fins it can also be avoided by optimizing the STI fabrication scheme (see e.g. Fig. 2 in Ref. 2).

**Si passivation layer.**—In most of our publications, we used an ultrathin Si layer to passivate the Ge surface in the high-k gate module. The benefit of the Si passivation layer above GeOx-based gate stacks is its potential to improve Bias Temperature Instability ( BTI) reliability. It is important to avoid surface segregation of Ge through the Si layer during the epitaxial growth as this leads to an increase of the interfacial trap density and distribution in the finalized gate stack. On the other hand, the Si passivation layer has to be sufficiently thin to approach an Equivalent Oxide Thickness (EOT) close to 1 nm as implemented in the current 14 nm-node FinFET. The Ge segregation into the Si passivation layer is independent of the choice of the Si precursor (cf. SIMS results in Figure 9). In this figure, SIMS profiles were aligned at the Si-cap/Ge interface. The independency of the Ge segregation of the choice of the Si precursor is in contradiction with previous results, where we observed a higher Ge segregation if the Si is grown using SiH4 or SiCl2H2. The difference between previous and current results is caused by differences in the pre-epi treatment used to remove the native oxide from the Ge starting surface. In previous experiments, the native oxide was removed by a pre-epi bake at a relative high temperature (600 °C). For the samples shown in Figure 9, the oxide was removed by a wet-chemical treatment without in-situ bake. For SiH4, enhanced Ge segregation into the Si layer was indeed confirmed on samples that received a pre-epi bake at 600 °C. Based on the atomistic modeling reported in Reference 20, we conclude that in case of SiH4 or SiCl2H2, the presence or absence of H passivation on the starting and growing surface strongly affects the Ge segregation. This is not the case for the higher order Si precursors where Si growth proceeds in a different growth mechanism. In this case, the Ge segregation is not affected by a potential in-situ thermal treatment before the Si growth. If the Si passivation layer is grown on strained Ge FinFET structures, there is a risk for Ge surface reflow during the Si deposition. This in turn would lead to a (partial) relaxation of the strained Ge layer. It sets the need to use higher order Si-precursors such as Si3H8 and Si4H10 to enable epitaxial growth at the required extremely low Si growth temperatures (∼350 °C). Despite the use of these higher order precursors it is challenging to avoid the Ge reflow, especially for narrow fins (Fig. 10).

**Source/drain contact layers.**—In case of strained channels on top of a SRB, the additional longitudinal stress created by source/drain stressors is very similar irrespective of the presence of a prior S/D recess. A major challenge is to maintain the material quality. To avoid strain relaxation of the channel and surface reflow of the uncovered S/D areas, surface treatments at elevated temperatures should be avoided. This sets the need for internal cleaning routines of the Ge or SiGe starting surface. In case of Ge devices, the low dopant solubility (especially for B, P, and As) makes it also challenging to obtain the required active doping concentration. In SiGe the doping solubility is slightly higher, making it somewhat easier to get a higher active doping concentration (Fig. 11). These SiGe layers were grown with conventional precursor gases (dichlorosilane and germane) which sets a lower limit to the growth temperature of ∼450 °C. These temperatures are too high for strained Ge fin devices as they result in surface reflow of the strained Ge fin. For Ge, novel low temperature epitaxial growth schemes to increase the active dopant incorporation are often based on attempts to move the growth rate as far as possible away from the equilibrium. The use of Ge2H6 allows the reduction of the growth temperature to 320 °C, while still maintaining material quality and an acceptable growth rate. An active n-dopant concentration up to $6 \times 10^{19}$ cm$^{-3}$ has been achieved. However, the use of a higher order precursor requires the use of a cyclic deposition and etch process for the S/D growth on device wafers as the Ge growth itself is...
not selective. In Ref. 39 Margetis et al. reported the epitaxial growth of in-situ doped GeSn on blanket Ge virtual substrates using GeH4 and SnCl4 as Ge and Sn precursors, respectively. The incorporation of Sn acts as a catalyzer enabling epitaxial growth at low growth temperatures thereby enabling active boron concentrations above $1 \times 10^{20}$ cm$^{-3}$. The chosen precursors including GeH4 instead of the normally used Ge2H6 permit selective GeSn deposition without growth on oxide and nitride surfaces. At imec, work is ongoing to study the selective growth characteristics and the material qualify for in-situ doped GeSn growth on the Source/Drain areas of fin patterned structures.

**SiGe/Ge multilayers for Ge GAA devices.**—Epitaxial Si/SiGe or SiGe/Ge multi-layers grown on blanket wafers are used to produce GAA FETs made of vertically stacked horizontal nanowires. Si GAA FETs can be fabricated from Si/SiGe with 25–30% Ge. The layers with the required steep compositional gradients (from SIMS we extracted $\sim 1.5$ nm wide interface between Si and SiGe) can be easily grown using standard process conditions and conventional Si and Ge precursors such as SiH4, SiCl2H2, and GeH4. HCl vapor etching and alkaline etching are options to selectively remove Si0.75Ge0.25 to Si0.2741 and Si to Si0.75Ge0.25, respectively.42 Recently, we demonstrated Si GAA FETs made of vertically stacked horizontal nanowires with excellent short-channel characteristics.27 An ultimate scaling of this technology assumes the use of either Si or Ge and SiGe with high Ge contents close to 50%. Growth of such Si/SiGe or Ge/SiGe stacks with a large lattice mismatch is challenging since it needs to be done at low temperatures to avoid strain relaxation which would lead to the formation of extended crystalline defects. The use of higher order precursors allows to deposit fully strained and defect free Si/Si0.6Ge0.4 and Ge/Si0.35Ge0.65 stacks with steep interfaces between the layers (Fig. 12).43 The Ge/Si0.35Ge0.65 layers are grown on Si0.3Ge0.7 step graded SRBs. The slightly higher Ge content in the SRB with respect to the SiGe in the multi-stack leads to a slight reduction of the lattice mismatch between the strained Ge and the virtual substrate. This reduces the risk for layer relaxation and defect formation. Within the multi-stack the difference in material composition is preferentially as large as possible to increase the selectivity in etching between the two materials. Symmetric and asymmetric RSM measurements confirm that the Ge layers are fully strained with respect to the underlying step graded Si0.3Ge0.7 SRB (Fig. 13). The observed fringes reflect the high quality Si0.35Ge0.65/Ge/Si0.35Ge0.65/Ge/Si0.35Ge0.65 multi-layer stack with fully strained Ge.

**Figure 11.** Active carrier concentration as measured for boron doped SiGe layers with different Ge concentrations. The highest active concentrations are obtained for Ge concentrations between $\sim 40$ and 70%. Different symbols refer to different lot numbers of our experiments, but don’t have a specific meaning for data interpretation.

**Figure 12.** Cross-section TEM micrographs of Si/Si0.6Ge0.4 and Ge/Si0.35Ge0.65 epi-stacks as used for Si and Ge GAA devices and grown on Si and a step graded SiGe SRB with Si0.3Ge0.7 in the final layer, respectively. The given Ge concentrations have been extracted from the Energy-Dispersion Spectra.

**Figure 13.** Symmetric and asymmetric RSM measured on a Si0.35Ge0.65-cap/Si0.35Ge0.65/Ge/Si0.35Ge0.65 epi-layer grown on top of a step graded SiGe SRB with Si0.3Ge0.7 in the topmost layer.
In this work we have addressed some of the challenges involved with the integration of (strained) Ge as high mobility Group IV material in ultra-narrow FinFET and GAA devices. Below a certain fin width, a critical growth temperature exists above which Ge or SiGe trench filling after Si recess on STI patterned wafers is prevented by SiGe or Ge surface migration. The mask design has some impact on the maximum allowable growth temperature, which is slightly higher for fin structures without source/drain pads. This helps to maintain material quality as demonstrated for epitaxial growth of relaxed Ge.

Strained Ge layers have been grown on top of fully relaxed Si$_{2}$Ge$_{0.7}$ virtual substrates which can be as thin as 55 nm. Full strain relaxation of the SiGe has been obtained using STI patterned wafers with a V-shaped Si recess and the deposition of a Ge-rich SiGe seed layer before the SRB growth. The (111) surfaces of the V-shaped Si recess are not only beneficial to increase layer relaxation but also facilitate the confinement of the dislocation network close to the substrate/SRB interface. The presence of uni-axial strain in the Ge channel was assessed to increase the active doping concentration. Finally, we briefly discussed the epitaxial growth of Si/SiGe and SiGeGe multi-layers grown on blanket wafers which are used to produce GAA devices. Again, higher order precursors and extreme low growth temperatures are used to prevent layer relaxation.

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