On the Impact of Device-Level Techniques on Energy-Efficiency of Neural Network Accelerators

Seyed Morteza Nabavinejad  
School of Computer Science  
Institute for Research in Fundamental Sciences (IPM)  
Tehran, Iran  
nabavinejad@ipm.ir

Behzad Salami  
Barcelona Supercomputing Center (BSC)  
Barcelona, Spain  
behzad.salami@bsc.es

Abstract—Energy-efficiency is a key concern for neural network applications. To alleviate this issue, hardware acceleration using FPGAs or GPUs can provide better energy-efficiency than general-purpose processors. However, further improvement of the energy-efficiency of such accelerators will be extremely beneficial specially to deploy neural network in power-constrained edge computing environments. In this paper, we experimentally explore the potential of device-level energy-efficiency techniques (e.g., supply voltage underscaling, frequency scaling, and data quantization) for representative off-the-shelf FPGAs compared to GPUs. Frequency scaling in both platforms can improve the power and energy consumption but with performance overhead, e.g., in GPUs it improves the power consumption and GOPs/J by up to 34% and 28%, respectively. However, leveraging reduced-precision instructions improves power (up to 13%), energy (up to 20%), and performance (up to 7%) simultaneously, with negligible reduction in accuracy of neural network accuracy.

Index Terms—hardware accelerators, neural networks, DVFS, reduced-precision instructions, power-efficiency

I. INTRODUCTION

Deep Neural Networks (DNNs), especially Convolutional Neural Networks (CNNs), are a very popular subcategory of machine learning with significant success rates in classification problems. They are essential for cutting-edge real-world applications, such as image and video classification, speech recognition, and robotics. DNNs learn a model from a dataset during the training phase and in the classification phase, make predictions about a new dataset that has not been seen previously. The computation and the memory requirements of these models are increasing depending on the size of the data as well as the number of layers and the filters. The massive amount of data movement and computational power required for such models limit their scalability for enterprise applications specially on power-constrained scenarios like drones and mobile devices.

Hardware acceleration using Graphics Processing Units (GPUs) [1], Field Programmable Gate Arrays (FPGAs) [2], or Application-Specific Integrated Circuits (ASICs) [3] is a promising solution to overcome such energy-efficiency drawbacks of DNNs. Among them, FPGAs are efficient data parallel compute engines with increasing use for data centers [4]. They attract great attention with their higher power efficiency than GPUs and better flexibility compared to ASICs. Additionally, recent advances in High-Level Synthesis (HLS) tools make it easier to map applications on FPGAs [5]. On the other hand, GPUs with internal Single Instruction Multiple Thread (SIMT) structure are convenient to accelerate these DNN models. Many of the emerging deep learning frameworks, such as Caffe [6], Torch [7], and TensorFlow [8] are specifically optimized to run on GPUs with CUDA programming interface. However, the high power consumption of GPUs raises cooling concerns in data centers. Moreover, ASIC-based accelerators are more power- and energy-efficient than FPGAs and GPUs [9]. However, further improving the energy-efficiency of FPGA- and GPU-based CNN accelerators can enable their deployment in power-constrained environments, as they provide better flexibility than ASICs. Toward this goal, this study aims to comparatively explore the potential of such off-the-shelf hardware platforms to take advantage of energy-efficiency techniques such as supply voltage underscaling, frequency underscaling, and reduced-precision instructions.

We study the following techniques: (i) Undervolting, i.e., the supply voltage level underscaling below the nominal level, reduces the total power consumption of the underlying hardware. Thus, it directly leads to the improved energy-efficiency. (ii) Frequency underscaling is used to prevent the undervolting-related errors that may occur due to the increased circuit delay when operating at reduced voltage levels. Although, frequency underscaling (simultaneously with supply voltage reduction) may lead to reduced performance but energy-efficiency improves while it prevents the neural network accuracy loss. (iii) As a common software-level technique, quantization can decrease the precision level of a numerical value used as a weight. This technique aims to reduce the size of CNNs without a significant loss of classification accuracy [10].

Our experimental study is based on a representative Xilinx ZCU102 Ultrascale+ (FPGA) and Nvidia Tesla P40 (GPU). We also perform our study on two state-of-the-art image classification models in the classification phase, i.e., ResNet50 and Inception. On this setup, we evaluate the three above-mentioned energy-efficiency techniques and in detail discuss the efficiency of such techniques. For the GPU accelerator, we deployed the networks on the GPU and applied different techniques to study their effect. For the FPGA-based accelerator, we adopted the experimental results presented in [11]. The experimental results indicate the surprising finding
that unlike FPGA-based accelerator, in GPU-based accelerator the highest power-efficiency and energy-efficiency cannot be simply achieved by highest and lowest frequency, but with careful exploration of all the frequency level options. The right combination of frequency level and precision of the models can lead to up to 35% power-efficiency and 28% energy-efficiency improvement. The temperature of the GPU accelerator can also be reduced by around 20% using the lowest frequency level, to meet certain limitations in temperature-critical situations in embedded systems.

To our knowledge, this is the first paper to simultaneously evaluate several energy-efficiency hardware- and software-level techniques on FPGA- and GPU-based neural networks. We make the following major contributions in this paper:

- We explore the effect of quantization and employment of reduced-precision instructions on the performance of DNNs as a function of computational complexity of the DNNs. We observe that more complex DNNs benefit from the reduced-precision instructions more than less complex ones in terms of runtime, power, and energy consumption.
- Conducting extensive set of experiments, we study the impact of DVFS on runtime, power, energy, and temperature of the networks. We show that the difference between runtime under lowest and highest GPU frequency is significant. So when the DVFS is reduced, it is possible to employ reduced-precision instructions to improve the runtime and mitigate the negative impact of low frequency.
- We evaluate the potential of energy-efficiency techniques on FPGA and GPU architectures while running a neural network applications.
- Comparing FPGA and GPU regarding frequency scaling, we find that in FPGA the best results for various metrics can be obtained at highest or lowest level of frequency. However, in GPU, more careful exploration of available frequency levels is needed since the best results for some metrics is achievable at frequency levels other than highest and lowest one.

The rest of the paper is organized as follows: In Section II we present and discuss the methodology and experimental results for our GPU-based CNN accelerator. In Section III we compare and discuss the energy-efficiency results between FPGA- and GPU-based accelerators. In Section IV we review the related works and conclude the paper in Section V.

II. GPU-BASED DNN

A. Background

Various Machine Learning (ML) frameworks are presented such as Caffe [6], Torch [7], and TensorFlow [8]. TensorFlow employs dataflow graphs to represent computation pattern of ML approaches including DNNs. It maps the dataflow graph nodes on available computing cores of a single machine or a cluster of machines. Hence, it can support large-scale and heterogeneous clusters or hardware with hundreds of computing cores such as GPUs. It can also work with other hardware platforms including multi-core CPUs and ASICs. While TensorFlow focuses on deep neural networks, it can support a variety of other ML applications as well [8].

TensorRT platform is developed and extended on top of CUDA to optimize the inference phase DNNs and consists of an inference optimizer and a runtime library. A trained DNN in the form of a frozen graph with its parameters is the input of TensorRT. TensorRT generates an optimized inference engine based on the frozen graph of DNN. TensorRT leverages a set of methods and techniques such as graph optimization and layer fusion for optimizing the inference engine of DNN. It can also generate reduced-precision versions of the inference engine that are able to employ the reduced-precision instructions of GPU families that provide architectural support for such instructions. Deep learning inference applications such as image classification and video streaming can leverage various reduced-precision versions of DNNs such as FP32, FP16, and INT8 that are offered by TensorRT to improve the inference latency, power, and energy, provided that the GPU supports those precision [12].

B. Methodology

The steps that we follow to conduct the experiments are presented in Fig. 1. We use the frozen graph model of DNNs that is generated for inference. The frozen graph is generated from the pre-trained model that is trained with ImageNet dataset [13]. To have FP32 and INT8 precision models of the network we first generate their counterpart frozen graph with TensorRT and then deploy them on the GPU. After that, the frozen graph starts execution on GPU to classify the images and tag them with the predefined labels. The predefined set of labels includes 1000 label classes from ImageNet dataset. During the execution, the desirable metrics such as power consumption are monitored and collected using the GPU Monitoring Interface (NVIDIA System Management Interface- nvidia-smi [14]). Upon completion of inference, the labels generated for each image are compared to original labels provided by dataset to calculate the accuracy of the results. The performance reported for the networks throughout the paper is based on the inference of all the images. The GPU Dynamic Voltage and Frequency Scaling (DVFS) controller is also used to control the frequency of GPU.

1) Quantization Technique: In our work, we use TensorRT to quantize the weights from FP32 to INT8. TensorRT is developed to optimize the inference phase of deep learning applications. TensorRT optimizes neural network models that are trained in major frameworks such as TensorFlow by calibrating the weights for lower precision with negligible accuracy loss. Symmetric linear quantization is used to scale FP32 to INT8. A saturation threshold for scale factor is considered and any value above (below) that threshold is mapped to +127 (-127)
DNN Frozen Graph
Default-Precision

TensorRT

Parameter
Quantization

GPU

DNN Frozen Graph
Reduced-Precision

GPU Monitoring Interface (Nvidia-SMI)

Runtime
Accuracy
Power

GPU DVFS Controller

Image 1
Image 2
Image 3
Image 4
Image 5
Image 6
Image 7
Image 8
Image N

GPU DVFS
Controller

Fig. 1. Flow of experimental results. First, TensorRT is employed to generate the FP32/INT8 version of the DNNs. Then, they are deployed on GPU for execution. During the execution, the various metrics such as power consumption are monitored using nvidia-smi tool. We use the same tool to apply DVFS on GPU and conduct the related experiments. Finally the labels generated for images by network are compared against the original ones provided by the dataset to evaluate the accuracy of results.

The GPU has 79 DVFS levels, starting from 544 MHz to 1531 MHz. Levels are very close to each other and moving from one level to another has negligible effect on GPU performance and power consumption. So, we chose 10 levels that have more distance from each other, and consequently, their effect is more significant: 544 MHz, 632 MHz, 734 MHz, 835 MHz, 949 MHz, 1063 MHz, 1189 MHz, 1303 MHz, 1430 MHz, and 1531 MHz. GPU vendor only allows controlling the frequency, but not the voltage. It adjusts the voltage according to selected frequency via the GPU driver, automatically.

D. Experimental Results

In this section, we present the experimental results to study the impact of DVFS on performance, accuracy, and power consumption of networks under various precision. For each network, we consider FP32 and INT8 precision, apply various GPU DVFS levels, and measure the performance, accuracy, and power consumption. As mentioned in previous section, we choose 10 DVFS levels of GPU. The performance results are depicted in Fig. 2. The performance of networks for processing 50000 images is measured under different DVFS settings for each precision, and normalized to the lowest performance of that precision (performance of the lowest DVFS level, i.e., 544 MHz in that specific precision). The black dots indicate the performance for each DVFS level and the horizontal lines of each box show the 25th, 50th, and 75th percentile of dots. For both networks, we see notable performance fluctuation as we change the frequency of GPU. However, the performance variation is more significant in FP32 precision than INT8. We see that INT8-precision can improve the performance that is affected by DVFS. In both networks, the INT8-precision can mitigate the impact of DVFS remarkably.

Moreover, we see that the performance of ResNet50 is more sensitive to frequency scaling than Inception in both precision. We can conclude that the effect of DVFS on performance of DNNs has a direct relationship with their architecture. Since DVFS mainly affects the computation time rather than data transfer time, larger and more complex networks are more affected by frequency scaling of GPU. The computation time relative to the overall execution time is higher for larger networks in comparison to small ones, and hence, they are more prone to performance degradation due to DVFS. We conclude that employing reduced-precision instructions can help networks to resist against frequency scaling and reduce its negative impact. It is very useful for systems that have specific Service Level Agreements (SLA) and should reach a certain level of Quality of Service (QoS) in the form of a predefined tail latency or other similar metrics.

Obviously, the power consumption of GPU is also affected by DVFS. The results for power consumption are depicted in Fig. 3. As expected, the power consumption decreases with the frequency underscaling. We also observe that the INT8-precision instructions lead to lower power consumption than FP32. Hence, we can conclude that combining low frequency and reduced precision can yield more power reduction than traditional frequency scaling approach. Finally, Fig. 4 shows the effect of frequency scaling, hence the power consum-
In this section, we comparatively evaluate the impact of the energy-efficiency techniques for FPGA- and GPU-based CNN workloads, as described in section II. Here we report Giga Operations per second (GOPs), power-efficiency (GOPs/W), and energy-efficiency (GOPs/J) for both Inception and ResNet50 in Table I and II, respectively. All results are normalized to the highest frequency (1531 Mhz). While the best value of GOPs is obtained with the highest frequency setting, the best value of power consumption is achieved with the lowest frequency setting. However, for GOPs/W and GOPs/J, a frequency setting different than the highest and lowest ones has better results based on the network and the precision.

III. FPGA- vs. GPU-based CNN Accelerators

In this section, we comparatively evaluate the impact of the energy-efficiency techniques for FPGA- and GPU-based CNN workloads, as described in section II. Here we report Giga Operations per second (GOPs), power-efficiency (GOPs/W), and energy-efficiency (GOPs/J) for both Inception and ResNet50 in Table I and II respectively. All results are normalized to the highest frequency (1531 Mhz). While the best value of GOPs is obtained with the highest frequency setting, the best value of power consumption is achieved with the lowest frequency setting. However, for GOPs/W and GOPs/J, a frequency setting different than the highest and lowest ones has better results based on the network and the precision.

A. Performance Analysis Through Voltage and Frequency Underscaling

Based on the results presented in Table 2 of [11], Table I and Table II, we compare the impact of voltage and frequency scaling on the performance (i.e., GOPs) of FPGA and GPU running CNN workloads. More specifically, we observe that:

- in the FPGA case, the highest frequency is nearly 50% more than the lowest frequency. However, in the GPU case, the highest frequency is almost three times of lowest one. The reason is that in the FPGA implementation of this technique, the minimum supply voltage that we could practically underscale is limited to Vcrash, which FPGA stops operating below it.
- for the FPGA case, the GOPs varies by 30% from highest to lowest frequency. But for the GPU case, the GOPs variation is less significant. The highest variation happens for ResNet50 in FP32 precision, where the GOPs gap is around 15%, and the lowest gap is 5% for Inception in INT8 precision. For both networks, we see that GOPs variation in INT8 is less than FP32, which means that we can expect less performance variation in the presence of reduced-precision instructions.

### Table I

| Frequency (MHz) | GOPs (FP32) | GOPs (INT8) | Power (W) | GOPs / W | GOPs / J |
|----------------|-------------|-------------|-----------|----------|----------|
| 1531           | 0.99        | 0.99        | 0.12      | 1.00     | 1.00     |
| 1430           | 0.99        | 0.99        | 0.12      | 1.00     | 1.00     |
| 1303           | 0.98        | 0.98        | 0.12      | 1.00     | 1.00     |
| 1189           | 0.96        | 0.96        | 0.12      | 1.00     | 1.00     |
| 1063           | 0.94        | 0.94        | 0.12      | 1.00     | 1.00     |
| 949            | 0.92        | 0.92        | 0.12      | 1.00     | 1.00     |
| 835            | 0.90        | 0.90        | 0.12      | 1.00     | 1.00     |
| 734            | 0.88        | 0.88        | 0.12      | 1.00     | 1.00     |
| 632            | 0.86        | 0.86        | 0.12      | 1.00     | 1.00     |
| 544            | 0.84        | 0.84        | 0.12      | 1.00     | 1.00     |

### Table II

| Frequency (MHz) | GOPs (FP32) | GOPs (INT8) | Power (W) | GOPs / W | GOPs / J |
|----------------|-------------|-------------|-----------|----------|----------|
| 1531           | 0.99        | 0.99        | 0.35      | 1.00     | 1.00     |
| 1430           | 0.98        | 0.98        | 0.35      | 1.00     | 1.00     |
| 1303           | 0.97        | 0.97        | 0.35      | 1.00     | 1.00     |
| 1189           | 0.95        | 0.95        | 0.35      | 1.00     | 1.00     |
| 1063           | 0.94        | 0.94        | 0.35      | 1.00     | 1.00     |
| 949            | 0.93        | 0.93        | 0.35      | 1.00     | 1.00     |
| 835            | 0.91        | 0.91        | 0.35      | 1.00     | 1.00     |
| 734            | 0.89        | 0.89        | 0.35      | 1.00     | 1.00     |
| 632            | 0.87        | 0.87        | 0.35      | 1.00     | 1.00     |
| 544            | 0.85        | 0.85        | 0.35      | 1.00     | 1.00     |
B. Power Consumption Analysis Through Voltage and Frequency Underscaling

For power consumption, again we see a wider gap in the FPGA (i.e., almost 46%) than the GPU case (i.e., 34% highest in ResNet50). Relatively narrower gap in INT8 than FP32 can be seen in GPU results as well. The power gap difference observed between FPGA and GPU can justify the difference between $\text{GOPS/W}$ gap discussed earlier. The wider gap in power consumption can translate to wider computing power gap, which leads to wider $\text{GOPS}$ gap. Since the power gap between the lowest and the highest frequency is wider in FPGA than GPU, we see a wider gap between $\text{GOPS}$ of the lowest and the highest frequency in FPGA as well.

C. Power- and Energy-efficiency Analysis Through Voltage and Frequency Underscaling

The first paragraph of this section would talk about the figure and the second would explain it.

Fig. 4 shows the different behavior of GPU and FPGA regarding $\text{GOPS/W}$ and $\text{GOPS/J}$. In this figure, we have only depicted the INT8 results for GPU. Since the frequency levels in FPGA (7) is less than GPU (10), only seven points for FPGA are depicted. Finally, since the value of frequency levels in FPGA and GPU are different (for GPU from 544 MHz to 1531 MHz, and for FPGA from 200 MHz to 333 MHz), we have used numbers from 1 to 10 to show frequency levels, instead of the exact values.

While the best results for $\text{GOPS}$ and power is obtained by the same level of frequency in both FPGA and GPU (the highest frequency for $\text{GOPS}$ and the lowest one for power), for $\text{GOPS/W}$ and $\text{GOPS/J}$ the pattern is different. In the FPGA case, the best result for $\text{GOPS/W}$ is obtained by the lowest frequency and for $\text{GOPS/J}$ by the highest one. These results indicate that FPGA-based NN designs with frequency scaling has the optimal energy operation point at lowest frequency while the optimal energy-delay operation point is at the highest frequency. In contrast with FPGA, for GPU the frequency that yields the best performance-power and performance-energy ($\text{GOPS/W}$, $\text{GOPS/J}$) trade-off is between the lowest and highest frequency. We see in Table I and Table II that the best frequency for $\text{GOPS/W}$ and $\text{GOPS/J}$ depends on both network and precision. These results indicate the non-linear behavior of GPU regarding frequency scaling. Simply selecting the highest or lowest frequency cannot always guarantee the best results.

D. Temperature Effects for FPGA- vs GPU-based CNN Accelerator

In Fig. 10 of [11], we see that the temperature has a direct impact on the accuracy of FPGA results in critical region. As the temperature increases, the accuracy increases too. However, for GPU, we do not observe any relation between temperature and accuracy. While the temperature increases as the frequency increases, the accuracy of both networks remains constant. The reason is that in the critical region of the FPGA, the voltage is so low that the effect of temperature on latency, and consequently the error rate, of circuit is significant. However for GPU, the voltage is still in guardband region even for very low frequencies, and hence, the temperature does not affect the accuracy of the networks. As mentioned in section II-C, there is no interface for controlling the voltage of GPU. Therefore, we cannot set the voltage of GPU in critical region to further study the effect of temperature on accuracy.

IV. RELATED WORK

Energy-efficiency is an important concern specially for power-constrained modern applications like DNNs. Energy-efficiency, specially in the hardware-level, is studied either using simulators or on the real underlying hardware. For instance, about undervolting as one of the energy-efficiency techniques evaluated in this paper, majority of the simulation-based studies target CPUs [16], [17], [18], specifically designed for caches [19], [20], [21] or branch predictors [22]. There are also studies for ASIC CNN accelerators [23], [24]. Additionally, there are FPGA-based designs either fully in simulation [25] or emulation of FPGA netlists on simulation frameworks [26], [27]. Conducting similar analysis on the real hardware requires a moderate engineering effort regarding physical limitations, but provides relatively more accurate results. For instance, there are several undervolting approaches targeting real hardware system components, such as CPUs [28], [29], GPUs [30], [31], ASICs [32], [33], DRAMs [34], [35], and FPGAs [36].
This paper complements the second approach on the real hardware by a more comprehensive experimental study of several state-of-the-art energy efficiency techniques on GPUs and also, compare it with FPGAs, while running DNN applications.

DVFS is a common method to manage the power consumption of a processor via tuning the frequency of clock, and consequently, supply voltage. Controlling the power consumption and performance of GPUs using DVFS has been studied in a large body of research [11], [12], [13], [14]. Jiao et al. [15] leveraged the capability of modern GPUs for hosting concurrent kernels, along with GPU core and memory frequency scaling to improve the performance per watt. Guerreiro et al. [16] proposed classification models for impact of DVFS on performance and power of GPU applications. Based on the models, they aimed to predict the impact of different DVFS levels on the applications and set the frequency of GPU accordingly. To reduce the energy consumption of matrix multiplication in GPUs, GreenMM [17] proposed GPU undervolting while keeping the frequency constant. Undervolting beyond minimum operational voltage leads to increase in number of faults. To address this challenge, GreenMM proposes an algorithm called Algorithm Based Fault Tolerance (ABFT). Tang et al. [18] studied the impact of GPU DVFS on performance and energy consumption of several DNNs and convolutional algorithms. They employed three GPUs with different architectures and four DNNs to conduct their experiments. Based on the results, the impact of high frequency on improving the performance and energy inefficiency of default frequency settings are explained. None of the aforementioned works studies the impact of reduced-precision instructions on performance of GPUs.

V. CONCLUSION

In this paper, we evaluated the energy-efficacy of CNN workloads running on off-the-shelf FPGA and GPU accelerators, using supply voltage underscaling techniques. We also evaluated the effect of frequency scaling, as well as architectural quantization techniques on the performance, power, and energy of such accelerators. We found that combining frequency scaling and reduced-precision instructions can significantly improve the energy-efficiency of GPU, while suffering from negligible accuracy loss. Moreover, comparing the GPU and FPGA, we observed that unlike FPGA that achieves best results for various metrics at highest or lowest frequency level, GPU achieves the best results for some metrics such as GOPs/J at a frequency level between lowest and highest. Therefore, it is necessary to explore the entire frequency state space of different GPUs to find the best results for a specific metric.

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