Article

Generalized Circuit Averaging Technique for Two-Switch PWM DC-DC Converters in CCM

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1. Introduction

The control of DC-DC converters is essential to achieve regulated voltage and current. There are several methods for obtaining the open-loop transfer functions viz., small signal modeling, circuit averaging, and state space averaging. The ideal converters show noticeable deviations from the practical converters in terms of stability due to ESR in the capacitor. In the past, several attempts have been made in determining the transfer functions of \( G_{vd} \) and input voltage to output voltage \( G_{vg} \) for several complex converters using different methods. Small signal modeling and state space averaging are some of the techniques employed for obtaining the open loop response for converters like Buck, Boost, and Buck-Boost. These methods become laborious when the order of the converter increases. Hence, a simpler method, circuit averaging, was introduced to the Cuk converter and Single Ended Primary Converter (SEPIC) [1]. In [2,3], a mathematical model for Cuk was presented. The importance of selecting a proper step size in MATLAB/Simulink was highlighted. The closed-loop operation for obtaining constant output voltage was simulated. In [4], the circuit averaging for the Cuk converter was carried out using a Saber circuit simulator, and \( G_{vd} \) and \( G_{vg} \) were found out theoretically and verified using simulation. \( G_{vd} \) showed complex pole conjugates and \( G_{vg} \) showed a right half plane (RHP) zero. In [5], circuit averaging using LTSpice for basic converters during ideal conditions was analyzed. However, the simulation and analysis for non-ideal higher-order converters was not carried out. In [6], the modeling of switching DC-DC converters was shown using state space modeling including parasitic values considering switching and conduction losses. In [7], a state space modeling approach for a fourth-order converter using MATLAB / Simulink was shown.

Circuit averaging is applied to Buck, Boost, Buck-Boost, and Cuk converters operating in CCM and the non-idealities like inductor and capacitor ESRs are included [8]. However, the non-idealities in the diode and the MOSFET were not considered.
A generalized technique for a non-ideal Cuk and SEPIC converter operating in CCM and DCM is shown in [9]. The model was simulated using LTSpice and the converter selected its operation based on the value of the duty cycle.

In any DC-DC converter, the switching losses are higher than the conduction losses [1]. The switching loss for a two-switch PWM converter is modeled as a resistor. Hence, the switching power loss can be incorporated into existing averaged small-signal dynamic models in basic converters operating in CCM [10]. To determine the value of the switching loss resistor component, an energy balance equation was used. A SEPIC operating in DCM was selected to drive a light-emitting diode (LED) for constant voltage application [11]. An average and a switching model were developed, modeled in MATLAB/Simulink, and validated against the experimental results. The transfer functions $G_{vd}$ and $G_{vg}$ were derived. It was shown that the SEPIC provided lower input current harmonics. An ideal SEPIC and Cuk operating in DCM were selected and used for power factor correction (PFC) [12]. The input to the converters was supplied by a single-phase rectifier. The open-loop transfer function obtained using the small signal model was validated against the hardware results and they were found to be closely correlated. The concept of circuit averaging for converters like Buck, Boost, and Buck-Boost in DCM was discussed [13]. It was shown that the input and output ports of such converters behave like a resistive and power sink, respectively.

In this paper, averaged models for non-ideal fourth-order converters like Cuk and SEPIC operating in CCM is analyzed using the LTSpice simulation tool. In earlier works, the dynamics of the converters considering the non-idealities using the circuit averaging technique were not presented for specific converters like Cuk and SEPIC. The equations required to model the switch network are shown in detail in this paper. The behavior in the output voltage under a variable inductor ESR was also studied. The modeling approach is generic and hence can be applied to a DC-DC converter of any order operating in CCM having MOSFET and diode. Circuit averaging is an advanced technique to determine $G_{vd}$ using an averaged switch network. This technique involves less computation (switch voltages and currents) to determine the frequency response of $G_{vd}$ and is recommended when the converter contains more than one inductor and capacitor. $G_{vd}$ obtained from circuit averaging matches with that obtained from the state space model.

2. Circuit Averaging for an Ideal SEPIC

Figure 1 shows an ideal SEPIC with MOSFET and a diode. The voltages and currents are denoted as $V_1$, $V_2$, $I_1$, and $I_2$, respectively. Figure 2 shows the converter with the switches separated.

![Figure 1. Circuit diagram.](image-url)
Figure 2. Separate the switches.

Circuit averaging of any converter involves three major steps viz.:
1. Separate the switch network from the converter and define the ports.
2. Sketch the waveform of the switch current and voltage waveforms and average it.
3. Simplify the equations and draw the equivalent switch network.

Averaging $V_1$, $V_2$, $I_1$, and $I_2$ waveforms:

$$\langle V_1 \rangle = (1-d)(V_{c1} + V_{c2}) \quad (1)$$

$$\langle V_2 \rangle = d(V_{c1} + V_{c2}) \quad (2)$$

$$\langle I_1 \rangle = d(i_{L1} + i_{L2}) \quad (3)$$

$$\langle I_2 \rangle = (1-d)(i_{L1} + i_{L2}) \quad (4)$$

From (1) and (2), eliminating $(V_{c1} + V_{c2})$:

$$V_{c1} + V_{c2} = \frac{V_1}{d} = \frac{V_2}{1-d} \quad (5)$$

$$V_{c2} = \frac{V_1 d}{1-d} \quad (6)$$

Similarly, from (3) and (4), eliminating $(i_{L1} + i_{L2})$:

$$I_1 = I_2 \frac{d}{1-d} \quad (7)$$

From (7) and (8), the turns ratio for the transformer can be derived as:

$$M = \frac{V_2}{V_1} = \frac{N_2}{N_1} = \frac{D}{1-D} \quad (8)$$

Equations (7) and (8) represent the generalized equations applicable to any switch PWM converter operating in CCM having two switches.

3. Small Signal Model

The small signal model provides the AC equivalent circuit in which the non-linear equations are linearized. $V_1$, $V_2$, $I_1$, and $I_2$ derived are now perturbed.

Perturbing (6):

$$\left( d' - \hat{d} \right) (V_2 + \hat{V}_2) = \left( d + \hat{d} \right) (V_1 + \hat{V}_1) \quad (9)$$

where $d' = 1-d$.

Similarly, perturbing (7):

$$\left( d' - \hat{d} \right) (I_1 + \hat{I}_1) = \left( d + \hat{d} \right) (I_2 + \hat{I}_2) \quad (10)$$
Figure 3 shows the equivalent large signal DC/AC switch model.

Figure 3. Equivalent switch network, where {1} is \( \frac{\delta V_1}{d\delta d} \) and {2} is \( \frac{\delta d}{d\delta d} \).

4. Circuit Averaging for a Non-Ideal SEPIC

Figure 4 shows the non-ideal SEPIC with \( V_0 = V_{c2} \).

\[
\langle V_1 \rangle = d(Ron_1*(iL_1+iL_2)) + d'(V_{c1}+V_{c2}) + V_d + Rd(iL_1+iL_2) \tag{11}
\]

\[
\langle V_2 \rangle = d((V_{c1}+V_{c2}) - Ron_1(iL_1+iL_2)) + d'(V_d + Rd(iL_1+iL_2)) \tag{12}
\]

\[
\langle I_1 \rangle = d(iL_1+iL_2) \tag{13}
\]

\[
\langle I_2 \rangle = d'(iL_1+iL_2) \tag{14}
\]

Simplifying (13) and (14):

\[
\frac{I_1}{d} = \frac{I_2}{1-d} \tag{15}
\]

From (12):

\[
V_{c1} + V_{c2} = \frac{V_2}{d} + \frac{Ron_1*(iL_1+iL_2)}{d} - d'(V_d + Rd*(iL_1+iL_2)) \tag{16}
\]

Substituting (16) in (11) and upon simplification:

\[
V_2 = \frac{I_1Ron_1}{d} + \left(1 - \frac{d}{d}\right) \left( V_2 + V_d + \frac{Rd*I_1}{d} \right) \tag{17}
\]

The equivalent circuit for (18) is shown in Figure 5.
5. Circuit Averaging for a Non-Ideal Cuk

Figure 6 shows an ideal Cuk converter operating in CCM. Figure 7 shows the MOSFET and diode separated from the converter.

Figure 8 shows the waveforms of switch voltages and currents at $dT_s$ and $(1 - d)T_s$ intervals, which is similar to Figure 9.

\[
\langle V_1 \rangle = V_c1 \ast (1 - d) \\
\langle V_2 \rangle = dV_c1 \\
\langle I_1 \rangle = d \ast (iL1 + iL2) \\
\langle I_2 \rangle = (1 - d) \ast (iL1 + iL2)
\]
5. Circuit Averaging for a Non-Ideal Cuk

Figure 6 shows an ideal Cuk converter operating in CCM. Figure 7 shows the MOSFET and diode separated from the converter.

Figure 6. Circuit diagram.

Figure 7. Switches separated.

Figure 8 shows the waveforms of switch voltages and currents at $dT_s$ and $(1 - d)T_s$ intervals, which is similar to Figure 9.

Figure 8. Waveforms during switch ON and OFF conditions.

Figure 9. Waveforms during Switch ON and OFF conditions, where {1} and {2} are $V_{c1} + V_{c2}$ and {3} and {4} are $i_{L1} + i_{L2}$.

Eliminating $V_{c1}$:

$$\frac{V_1}{1 - d} = \frac{V_2}{d}$$  (22)

$$V_2 = \frac{(V_1 \cdot d)}{d'}$$  (23)

The turns ratio of the transformer irrespective of the converter would remain the same, i.e.:

$$M = \frac{N_2}{N_1} = \frac{V_2}{V_1} = \frac{D}{1 - D}$$

Therefore, the equivalent circuit would remain the same as that of the SEPIC.
6. Circuit Averaging for Non-Ideal Cuk Converter

On averaging the voltages and currents across the switches:

\[ \langle V_1 \rangle = d (R_{on1} \cdot (iL_1 + iL_2)) + d' (Vc1 + V_d + R_d \cdot (iL_1 + iL_2)) \]  \hspace{1cm} (24)

\[ \langle V_2 \rangle = d (Vc1 - R_{on1} \cdot (iL_1 + iL_2)) - d' (V_d + R_d \cdot (iL_1 + iL_2)) \]  \hspace{1cm} (25)

\[ \langle I_1 \rangle = d (iL_1 + iL_2) \]  \hspace{1cm} (26)

\[ \langle I_2 \rangle = d' (iL_1 + iL_2) \]  \hspace{1cm} (27)

Eliminating \( iL_1 \) and \( iL_2 \):

\[ \frac{I_1}{d} = \frac{I_2}{d} \]  \hspace{1cm} (28)

From (25):

\[ Vc1 = \frac{V_2}{d} \cdot \frac{R_{on1} \cdot I_1}{d} + \frac{1 - d}{d} \cdot \left( V_d + \frac{R_d \cdot I_1}{d} \right) \]  \hspace{1cm} (29)

Substituting (29) in (24):

\[ V1 = I_1 \cdot \frac{R_{on1}}{d} + \frac{1 - d}{d} \cdot \left( V_d + \frac{R_d \cdot I_1}{d} \right) \]  \hspace{1cm} (30)

The small signal is generic and provides results for any DC-DC converter having two switches operating in CCM.

7. Converter Specifications

Table 1 shows the specifications of Non-ideal Cuk converter.

| SL.NO | Specifications                     | Value   |
|-------|-----------------------------------|---------|
| 1     | Input Voltage, \( V_g \)         | 28 V    |
| 2     | Output Voltage, \( V_o \)        | 10 V    |
| 3     | Output Current, \( I_o \)        | 1 A     |
| 4     | Inductors, \( L_1 \) and \( L_2 \) | 330 \( \mu \)H |
| 5     | Inductor ESR, \( R_{L1} \) and \( R_{L2} \) | 0.1 \( \Omega \) |
| 6     | MOSFET Resistance, \( R_{on1} \) | 31 \( \text{m} \)\( \Omega \) |
| 7     | Duty Cycle, \( D \)              | 0.3     |
| 8     | Capacitors, \( C_1 \) and \( C_2 \) | 6.8 \( \mu \)H |
| 9     | Capacitor ESR, \( R_{esr} \)     | 0.2 \( \Omega \) |
| 10    | Switching Frequency, \( f_s \)    | 100 \( \text{kHz} \) |
| 11    | Diode Drop, \( V_d \)            | 0.8 V   |
| 12    | Diode Forward Resistance          | 0.8 \( \Omega \) |

Table 2 shows the specifications of Non-ideal SEPIC.
Table 2. Specifications of non-ideal SEPIC.

| SL.NO | Specifications            | Value          |
|-------|---------------------------|----------------|
| 1     | Input Voltage, Vᵢ          | 300 V          |
| 2     | Output Voltage, V₀         | 400 V          |
| 3     | Output Current, Iₒ         | 5 A            |
| 4     | Inductors, L₁ and L₂       | 2.57 mH & 1.71 mH |
| 5     | Inductor ESR, Rₑ₁ and Rₑ₂ | 130 mΩ & 110 mΩ |
| 6     | MOSFET Resistance, Rₒ₁     | 321 mΩ         |
| 7     | Duty Cycle, D              | 0.571          |
| 8     | Capacitors, C₁ and C₂      | 4.7 µF & 3.57 µF |
| 9     | Capacitor ESR, Rₑₑ         | 270 mΩ & 350 mΩ |
| 10    | Switching Frequency, fₛ     | 100 kHz        |
| 11    | Diode Drop, Vᵈ            | 0.62 V         |
| 12    | Diode Forward Resistance   | 80 mΩ          |

8. Results

Simulations were performed using LTSpice software. The equivalent switch network was available as a built-in library under ‘average.lib’ library.

D was varied from 0.3 to 0.6 every 1 ms and the corresponding iL₁ and V₀ were analyzed. Figures 10 and 11 show the variation of iL₁ and V₀ with respect to the D for Cuk and SEPIC, respectively. It was observed that an increase in D caused an increase in iL₁. However, V₀ for Cuk and SEPIC increased in the negative and positive directions, respectively.

![Figure 10](image1.png)  
*Figure 10. Variation of iL₁ and V₀ with change in D (Cuk). (a) Output Voltage Vs. Control Voltage, (b) Inductor 1 Current Vs. Control Voltage*
In Figure 12, $R_L$ was varied from 0.1 $\Omega$ to 0.3 $\Omega$ in steps of 0.1. It was observed that higher $R_L$ provided higher $iL_1$ and $V_0$. SEPIC also showed similar features. In Figure 13, $R_{L1}$ and $R_{L2}$ were varied. It was found that the lowest value of $R_{L1}$ and the highest value of $R_{L2}$ provided higher voltage levels.

Figure 11. Variation of $iL_1$ and $V_0$ with change in $D$ (SEPIC). (a) Output Voltage Vs. Control Voltage, (b) Inductor 1 Current Vs. Control Voltage

Figure 12. Variation of $iL_1$ and $V_0$ with change in $R_L$ (Cuk). (a) Output Voltage Vs. Control Voltage, (b) Inductor 1 Current Vs. Control Voltage
Figure 12. Variation of $i_{\text{L1}}$ and $V_0$ with change in $R_L$ (Cuk). (a) Output Voltage Vs. Control Voltage, (b) Inductor 1 Current Vs. Control Voltage

Figure 13. Variation of $i_{\text{L1}}$ and $V_0$ with change in $R_L$ (SEPIC). (a) Output Voltage Vs. Control Voltage, (b) Inductor 1 Current Vs. Control Voltage

Figure 14 shows the Bode plot of $G_{vd}$ for an SEPIC under the variation of $D$ from 0.2 to 0.9 in steps of 0.01 considering a fixed load. The crossover frequency was about 4.207 kHz, gain cross over frequency about 169.45 kHz, gain margin about $-43.60$ dB, and phase margin about $-30^\circ$. Thus, the open loop behavior of SEPIC is unstable. A step change in $R$ varying from 80 $\Omega$ to 100 $\Omega$ in steps of 10 $\Omega$ was simulated. As shown from Figure 15, a higher value of $R$ created higher resonance.

Figure 14. $G_{vd}$ for SEPIC for fixed $R$. 

Figure 15. $G_{vd}$ for SEPIC for variable $R$. 

Figure 14 shows the Bode plot of $G_{vd}$ for an SEPIC under the variation of $D$ from 0.2 to 0.9 in steps of 0.01 considering a fixed load. The crossover frequency was about 4.207 kHz, gain crossover frequency about 169.45 kHz, gain margin about $-43.60\,\text{dB}$, and phase margin about $-30^\circ$. Thus, the open loop behavior of SEPIC is unstable. A step change in $R$ varying from $80\,\Omega$ to $100\,\Omega$ in steps of $10\,\Omega$ was simulated. As shown from Figure 15, a higher value of $R$ created higher resonance.

Figure 14. $G_{vd}$ for SEPIC for fixed $R$. 

Figure 15. $G_{vd}$ for SEPIC for variable $R$. 

Similar to that of SEPIC, $D$ was varied from 0.2 to 0.9 in steps of 0.01 for a non-ideal Cuk converter. The cross-over frequency was about 2.92 kHz with a gain margin and phase margin of about $-23.85\,\text{dB}$ and $-160.894^\circ$, respectively. Thus, the open-loop system was unstable. Figure 16 shows a bode plot of $G_{vd}$ for a fixed value of $R$. A similar feature in $G_{vd}$ for varying $R$ was seen in the practical Cuk converter shown in Figure 17. $G_{vd}$ was computed in LTSpice software using the AC sweep command.

Figure 16. $G_{vd}$ for Cuk for variable $R$. 

Similar to that of SEPIC, $D$ was varied from 0.2 to 0.9 in steps of 0.01 for a non-ideal Cuk converter. The cross-over frequency was about 2.92 kHz with a gain margin and phase margin of about $-23.85\,\text{dB}$ and $-160.894^\circ$, respectively. Thus, the open-loop system was unstable. Figure 16 shows a bode plot of $G_{vd}$ for a fixed value of $R$. A similar feature in $G_{vd}$ for varying $R$ was seen in the practical Cuk converter shown in Figure 17. $G_{vd}$ was computed in LTSpice software using the AC sweep command.
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The frequency response of $G_{vd}$ obtained from the circuit averaging and small signal model for a non-ideal Cuk converter was compared. The specifications shown in [3] were chosen, simulated, and compared. Figure 18 shows the circuit averaging model for the selected converter using the LTSpice software tool. Figure 19 shows $G_{vd}$ obtained from the circuit averaging technique using the AC sweep command. Figures 20 and 21 show the $G_{vd}$ plots based on [3].

Figure 17. $G_{vd}$ for Cuk for variable $R$.

Figure 18. Circuit averaged model.
The frequency response of $G_{vd}$ obtained from the circuit averaging and small signal model for a non-ideal Cuk converter was compared. The specifications shown in [3] were chosen, simulated, and compared. Figure 18 shows the circuit averaging model for the selected converter using the LTSpice software tool. Figure 19 shows $G_{vd}$ obtained from the circuit averaging technique using the AC sweep command. Figures 20 and 21 show the $G_{vd}$ plots based on [3].

Figure 18. Circuit averaged model.

Figure 19. $G_{vd}$ for a non-ideal Cuk converter.

Figure 20. Theoretically derived $G_{vd}$ for a non-ideal Cuk converter [4].
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Figure 20. Theoretically derived $G_{vd}$ for a non-ideal Cuk converter [4].

Figure 21. MATLAB-generated $G_{vd}$ for a non-ideal Cuk converter [4].

It can be observed that $G_{vd}$ obtained from circuit averaging and [4] closely match.

9. Conclusions

The circuit averaging technique for fourth-order converters like Cuk and SEPIC was carried out using the LTSpice software tool. This generalized approach to predict the frequency response of $G_{vd}$ can be applied for any two-switch PWM DC-DC converters operating in CCM. This method is comparatively simple and easy to implement compared to the conventional small signal and state space averaged models. The lowest value of $R_{L1}$ and the highest value of $R_{L2}$ cause higher voltage levels. $G_{vd}$ becomes unstable in the open-loop configuration for the chosen converters. This technique does not provide the transfer function equation of $G_{vd}$. However, the specifications like gain and phase margins and gain and phase cross-over frequencies can be easily found and its stability can be analyzed. The LTSpice model was used for the two-switch configuration in this paper. However, it can be extended to converters having multiple switches.

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