A sub-picosecond digital clock monitoring system

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ABSTRACT: We describe a low-cost system designed to monitor wander in digital clocks with a precision of \( \leq 1\) ps. With this system we have shown that it is possible to track phase variations at the sub-picosecond level by adding noise to a reference clock. As in many cases where a clock is part of a complex distribution network small changes in temperature and other effects can lead to small changes in the clock’s phase. As a further demonstration of the system, we have used it to measure the phase changes induced in optical signals in fibers.

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1 Introduction

Systems that can distribute precision reference clocks stable to a level of a few picoseconds is a common theme in many current and proposed experiments in high energy physics. At the CERN High-Luminosity LHC (HL-LHC) the average number of interactions in each bunch crossing, will be 140 or higher. To help contend with this level of pile up, both the ATLAS and CMS Collaborations are planning to install specialized detectors capable of measuring the arrival time of a particle to 30 ps or less.

For these detectors and others that exploit precision timing, both distributing and monitoring the stability of the reference clock will be an essential task. In this paper we describe a clock-monitoring system that we have developed to monitor drifts in the reference clock with sub-picosecond precision.

At the sub-picosecond level, the use of currently available frequency counters or time interval counters are precluded. One method for comparing two clocks employs a scheme known as the Dual Time-Difference Measurement circuit, where the clock signals are heterodyned and the beat clock used to extract the time difference [1]. A digital version of this circuit, the digital dual mixer time difference (DDMTD) circuit, was first proposed by Moriera and Darwazeh [2]. The circuit has recently been implemented in an FPGA [3] and with phase stabilization has achieved a level of $\approx 2$ ps [4]. In this paper we report how we have used this approach with modern discrete RF components to design a system to measure variations in a clock’s phase to less than 100 fs.

In this report we describe the basic principle of operation of a DDMTD circuit and report on results obtained from the laboratory measurements. We show that it is feasible to detect sub-picosecond phase variations with such a system.
2 Principle of operation

The DDMTD is a digital circuit composed of a phase-locked-loop (PLL) and two flip-flops (FF) that can be used to compare the time interval error (TIE) of two clocks with high precision. In the circuit two input clocks, a reference and a test clock, are input to two D-type flip-flops. These are clocked with an offset frequency clock generated by a ‘helper’ PLL phase-locked to the reference clock. The outputs of the two flip-flops are beat clocks, whose relative phases can be compared to measure changes in the phase difference between the two input clocks.

Formally, if $u_1$ and $u_2$ are the reference and test clocks with frequencies $\nu_1$ and $\nu_2$ and periods $\tau_1$ and $\tau_2$, then the frequency of the offset clock, $\nu_{\text{ddmtd}}$, can be selected using equation (2.1):

$$\nu_{\text{ddmtd}} = \frac{N}{N + 1} \cdot \nu_1 (2.1)$$

where $N$ is an integer that determines the number of input clock cycles required for a full phase cycle of the beat clock, whose frequency is given by equation (2.2)

$$\nu_{\text{beat}} = \frac{1}{N} \cdot \nu_{\text{ddmtd}} = \frac{\nu_1}{N + 1} (2.2)$$

The time difference between the two input clocks can be measured with a minimum sensitivity that is given by equation (2.3):

$$t_{\text{min}} = \frac{1}{\nu_{\text{ddmtd}}} \cdot \frac{\nu_{\text{beat}}}{\nu_1} = \frac{\tau_{\text{ddmtd}}}{N + 1} = \frac{\tau_1}{N} (2.3)$$

where $\tau_{\text{ddmtd}}$ is the period the offset clock.

By measuring the difference between the transitions of the beat clocks, $\Delta t_{\text{beat}}$, the time difference between $u_2$ and $u_1$ can be measured as in equation (2.4) [2].

$$\Delta t = \Delta t_{\text{beat}} \cdot \frac{\nu_{\text{beat}}}{\nu_1} = \frac{\Delta t_{\text{beat}}}{N + 1} (2.4)$$

One of the limits of this method is set by the precision with which the helper PLL can accurately generate the offset clock. For the results reported in this paper, we have used a digital input clock with a frequency of 160 MHz and $N = 100k$ and 10k, which, by equation (2.3), have minimum sensitivities of 62.5 fs and 625 fs, respectively.

As the time difference between the input clocks is determined from both the positive and negative edges of the beat clocks, the highest frequency that it can be measured is given by equation (2.5), with $\nu_{\text{max}}$ approximately 1.6 kHz and 16 kHz for $N = 100k$, and 10k respectively.

$$\nu_{\text{max}} < \frac{\nu_{\text{beat}}}{2N} < \frac{\nu_{\text{beat}}}{2\text{Nyquist Limit}} = \frac{\nu_1}{N + 1} (2.5)$$

When the offset clock has a transition edge close to the transition edge of the input clocks, the set-up and hold times may be violated and the output of the flip-flop becomes unstable. This instability can last for several clock cycles of the input clock. To estimate the exact time of the transition, the average of the time of the first and last transitions can be used. The length of this instability is determined by the setup and hold times of the flip-flops used. Standard CMOS devices have setup and hold times of ~800 ps, while for the silicon-germanium NB7V52M flip-flops used in the circuit discussed below, they are ~15 ps. Thus the exact time of the transition can be more accurately estimated.
3 System design

The clock-monitoring system that we developed to investigate the precision that can be achieved is shown in figure 1. It is based on a 5U motherboard, which supports a Nexys Video board and a Raspberry Pi, with the DDMTD circuit mounted in a mezzanine board connected to the Nexys Video board via an FMC connector. The Raspberry Pi manages the configuration of the on-board electronics and the data acquisition from the Artix-7 FPGA on the Nexys Video board. The beat clocks from the DDMTD mezzanine card are sampled by the FPGA and stored in memory until the Raspberry Pi starts data acquisition.

Figure 1. DDMTD Nexys Board.

A schematic of the DDMTD mezzanine is shown in figure 2. The circuit is equipped with four high-performance flip-flops (FF),\(^1\) which have a maximum clocking rate of 12 GHz and a Silicon Labs Si5344 Jitter Attenuator/Clock Multiplier IC that has a quoted rms jitter of 90 fs.\(^2\) The choice of duplicating the two input flip-flops was to allow the investigation of the properties and stability of the flip-flops.

The two input clocks are fed into the mezzanine board as differential pairs on SMA connectors. The clocks are fanned out to the four flip-flops and to the Si5344 using the 1-to-6 fan-out chip NB7VQ1006M from ON Semiconductors. These fan-outs are high-performance with a typical

\(^1\)NB7V52M, manufactured by ON-Semiconductors.
\(^2\)https://www.skyworksinc.com/en/Products/Timing/Coherent-Optical-Clocks/Si5344H.
Figure 2. Schematic of the DDMTD Mezzanine. The clocks $u_{\text{ref}}$ and $u_{\text{test}}$ are fed into flip flops that are clocked by an offset clock generated by a Si5344 Jitter Attenuator / Clock Multiplier. The outputs of the flip-flops are sent via the FMC connector to the Artix-7 FPGA on the Nexys video board.

RJ (Random Jitter) + DJ (Deterministic Jitter) = (0.2 + 3.0) ps.\textsuperscript{3} The differential D-type flip-flop NB7V52M has an RMS jitter < 0.8 ps.\textsuperscript{4} The output of the helper PLL Si5344 is distributed to the clock inputs of all the flip-flops using a second NB7VQ1006M. A copy of this clock (CLK PLL) is transmitted to the Artix-7 FPGA to drive the sampling logic in the FPGA.

The firmware logic implemented on the Artix-7 FPGA is shown in figure 3. Two FIFOs are used to store the value of a 32-bit counter, which is incremented by the CLK PLL. Whenever one of the beat clocks, Q1A or Q1B, changes state the value of the counter is pushed to the FIFO. When the FIFO chain is almost full, the Raspberry Pi pulls the data through the SPI bus and sends it to the PC via Ethernet.

Offline a Fast Fourier Transform (FFT) is used to determine the frequency components of the jitter. The exact time of the phase transition between the two clocks is estimated from the difference between the first and the last edges of the meta-stable region.

4 Characterizing system performance by injecting noise

To investigate the performance of the DDMTD and to measure the precision with which TIE can be measured, sinusoidal jitter patterns were injected onto a 160 MHz digital clock. For this two 160 MHz clocks were generated by a pulse pattern generator,\textsuperscript{5} and jitter was injected onto one

\textsuperscript{3}https://www.onsemi.com/pub/Collateral/NB7VQ1006M-D.PDF.
\textsuperscript{4}https://www.onsemi.com/pub/Collateral/NB7V52M-D.PDF.
\textsuperscript{5}Keysight 81134A.
of them using a secondary function generator\textsuperscript{*} connected to the Delay Control Input of the pulse generator. While the nominal amplitude of the jitter generated by the function generator for a 1 V input signal was 25 ps, all our measurements were consistent with \(\sim 12\%\) calibration error, such that a 1 V signal produced a \(\approx 28\) ps jitter.

The injected jitter pattern was compared to the jitter pattern recovered using the DDMTD-Nexys Board. The schematic of the configuration used for the tests is shown in figure 4. With this set up we were able to investigate sinusoidal jitter injection patterns with amplitudes between 0.25 ps and 25 ps and frequencies up to 6 kHz.

For these tests the offset parameter (as defined in equation (2.1)) was set to \(N=100,000\) corresponding to a \(v_{\text{max}}\) of 1.6 kHz at a carrier clock frequency of 160 MHz. Figure 5 shows the results from the DDMTD for a injected sinusoidal variation of 50 Hz at a noise amplitude of 25 ps. We observe the 50 Hz signal and its higher monotones in the FFT. Figure 6 shows the response of the system when the input jitter was modulated from 40 Hz to 750 Hz with amplitudes ranging from 0.25 ps to 25 ps.

Similar observations are shown in figures 7 and 8, where the recovered noise amplitudes were compared against the injected noise amplitudes.

The response of the DDMTD system to different frequencies of injected noise are shown in figures 9 and 10 and is observed to be flat across all the injected frequencies with a maximum standard deviation less than 100 fs.

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5 Measurements made with the DDMTD

5.1 Effects of temperature on front-end electronics and optical fiber

We used the clock-monitoring system to investigate temperature effects in transmission optical fibers and in a front-end emulator with an LpGBT and a VTRx+ optical transceiver [5]. The configuration of the test system is shown in figure 11.

For these tests we used an Si5345 jitter attenuator as the source of a stable 40 MHz clock that was transmitted to a front end electronics emulator through a custom designed board, FLY 640 [6], on a 25 m long 12-channel multimode optical fiber. The front end emulator, consisting of a VTRX+
Figure 6. Recovered Noise Frequency vs. Injected Noise Frequency 0.25 to 25 ps.

Figure 7. Recovered noise amplitudes for injected noise amplitudes between 2.5 to 25 ps; N = 100k. The plots are staggered for readability.

and an LpGBT characterization board, returned the 40 MHz clock signal back through the optical fiber to the DDMTD clock-monitoring system. A copy of the 40 MHz clock was also sent from the Si5344 board directly to the DDMTD as the reference clock.

With this setup, we measured the temperature effects on a 25 m optical fibre and on the front-end emulator by separately placing them inside a climate chamber. The parts of the set up that were kept inside the chamber are shown in figure 11 with red dotted boxes.

Compared to our qualification tests discussed above, the carrier frequency was 40 MHz rather than 160 MHz. At this frequency, with N = 100 k, only jitter frequencies up to 400 Hz are detectable, which is nevertheless much faster than any effects expected from temperature changes.

The first test was performed with the up-link and down-link fibres in the temperature-controlled chamber and the clock monitoring system was used to track changes in the signal delay time as the fiber temperature was changed. The results of these tests are shown in figure 12a. We
Figure 8. Recovered noise amplitudes for injected noise amplitudes between 0.25 to 2.5 ps; N = 100 k. The plots are staggered for readability.

Figure 9. Stability of the recovered amplitude of the injected harmonic noise as a function of frequency, for injected amplitudes between 2.5 and 12.5 ps, measured with N = 100 k.

observe a change of ≈ 4 ps/°C. Assuming that the up-link and down-link shifts are symmetric, we measure the delay change of an optical clock signal propagating in multi-mode fiber to change by 0.08 ± 0.01 ps/m·°C.

In the second test we investigated the effect of temperature changes on the front-end emulator. figure 12b shows the time interval error as the temperature of the emulator board was changed from −30°C to 60°C in steps of 10°C. Assuming a symmetric up-link and down-link delay, we observe a delay coefficient of ≈ 1.3 ps/°C.

These results are consistent with the measurements made with a digital oscilloscope and a phase noise analyser.
Figure 10. Stability of the recovered amplitude of the injected harmonic noise as a function of frequency, for injected amplitudes between 0.25 and 2.5 ps, measured with N = 100 k.

Figure 11. Configuration of the clock monitoring system used to measure the effect of temperature on an optical fiber and on the front-end emulator.

5.2 Tests with a pure clock distribution system

As part of our investigation into the problem of distributing a precision clock we have designed and tested a scalable pure clock distribution system using high-performance, low-jitter, off-the-shelf components. Full details of the system may be found in [6]. In the system, a 640 MHz low-jitter digital clock is generated and distributed to two distribution boards, where copies of the clock are made using 1–6 fan-out and distributed using 12-channel SAMTEC Firefly Tx modules. The optical signal from the Fireflies is sent via 100 m long multi-mode fibers to front-end emulator boards (FE), where the optical signal is converted back to an electrical signal and divided by four and made available on SMC connectors. The system is shown schematically in figure 13.

We report here on tests made with this system using the DDMTD clock monitor with N = 10 k and 100 k. The maximum frequency of the jitter that we are sensitive to is 16 kHz with N = 10 k, and 1.6 kHz with N = 100 k for a clock frequency of 160 MHz. First we measured with the DDMTD the noise floor of the Si5344 in the “Master” by comparing two output clocks set at 160 MHz, where we
obtained standard deviations of 0.3 ps and 0.4 ps for 100 K and 10 K, respectively. In both cases the noise level in the frequency domain was flat between 1 Hz and the upper limit of the measurement, 1.6 kHz for N = 100 k and 16 kHz for N = 10 k.

When we compared two output clocks from the same FE board, supplied by the same FLY 640 boards, we obtained a standard deviation of 0.6 ps and 1.0 ps for N = 100 k and 10 k, respectively, and a flat response in frequency domain. Comparing clocks distributed to two separate FE boards, which is comparable to how two reference clocks would be distributed in an experiment, we obtained the TIE distributions shown in figures 14 and 15 for channel 1 in each FE board, with a standard deviations of 0.5 ps and 0.8 ps for N = 100 K and 10 K, respectively. Similar results were obtained comparing different combinations of the output clocks. The summary of the results obtained are given in table 1.
Figure 14. Measurement of the TIE at 160 MHz between the outputs FE-1A and FE-1B of the clock distribution system made with the DDMTD with \( N = 100,000 \).

Figure 15. Measurement of the TIE at 160 MHz between the outputs FE-1A and FE-1B of the clock distribution system made with the DDMTD with \( N = 10,000 \).

Table 1. Time-interval error measurements of the Pure Clock Distribution System using the DDMTD circuit.

| \( u_1 \)   | \( u_2 \)   | \( \sigma_{\text{TIE}} \) (ps) |
|------------|------------|-------------------------------|
| Master-1   | Master-2   | \( N = 10 \text{ k} \) | \( N = 100 \text{ k} \) |
| FE-1A      | FE-2A      | 0.5                           | 0.3                      |
| FE-1B      | FE-2B      | 1.1                           | 0.7                      |
| FE-1A      | FE-1B      | 0.9                           | 0.5                      |
| FE-2A      | FE-2B      | 1.1                           | 0.6                      |
6 Summary

We describe the design and operation of a digital dual mixer time different (DDMTD) circuit built with discrete radio-frequency components. To characterise the circuit, harmonic noise with amplitudes ranging from 0.25 ps to 25 ps and frequencies ranging from 50 Hz to 710 Hz was injected onto a 160 MHz digital clock. With the DDMTD we were able to recover the noise frequency of the injected noise with a precision of 0.2% and the measured amplitudes of the injected noise were found to be stable across different injection frequencies, with a maximum standard deviation of less than 100 fs.

Tests made with a pure clock distribution system had a maximum standard deviation of 1.1 ps between two parallel distributions systems with 100 m multi-mode fibers in each path. We have also measured the delay of an optical clock signal propagating in a multi-mode fiber to be 0.08 ± 0.01 ps/m·°C.

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