Thermal analysis for optimized selection of cooling techniques for SiC devices in high frequency switching applications

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Abstract. The inception of wide bandgap power semiconductors has paved way for the evolution of highly efficient power switches. A deep understanding about the thermal characteristics of the SiC power device is essential to utilize its advantages in terms of higher thermal and power handling capability. The primary objective of this paper is to establish an accurate thermal model by proposing and comparing different methodologies for thermal analysis of commercially available SiC device, which in turn will aid to select optimum cooling techniques for higher system efficiency. Exponential curve fitting technique was exploited to deduce the parameters for RC equivalent network model. A high frequency sinusoidal pulse width modulated SiC MOSFET inverter with a fixed load was considered for electro-thermal analysis using a unified software platform PLECS. The effect of switching frequency on heat sink volume was established through simulation studies with imbibed datasheet parameters of a commercial power device. Finally, a 3-D model of the commercially available SiC power MOSFET in SOT-227B package was built to analyse the device heat dissipation profile for an optimized cooling choice. The proposed modelling approach serves to provide a platform for the thermal optimization of power devices and can be extended to other semiconductor devices.

1. Introduction
Power semiconductor devices evolved over several decades to exhibit improved performance in terms of extended life, reduced device cost and package size. Recently, the compound semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) are emerging as viable alternatives on account of their superior characteristics over their silicon counterparts in terms of higher efficiency, low on state resistance, high voltage blocking capability, very high switching frequency, high input impedance, high power density and more importantly the ability to operate at higher junction temperatures. These figures of merit have made the over-temperature, over-current and over-voltage protections to become cost effective for wide band gap devices compared to the legacy Si devices. A substantial entity of the power electronic system cost is associated with cooling and passive components as evident from figure 1 for conventional Si based system design. However, power electronic integration has always contemplated for a substantial reduction in the cost and size of passive elements by operating the semiconductor switches at very high switching frequencies [2]. But, the maximum junction temperature limits of the legacy Si power devices restrained the maximum operating frequencies eventually retaining the share of cooling and passives the same over decades as in figure 1. Market research states that Silicon Carbide Field Effect Transistor or SiCFET’s are expected to penetrate the entire market base for power...
semiconductor domain [3]. Further decrease in the required installation space can be realized even with the SiC devices by warranting an optimized cooling system specifically designed for any desired high frequency as demanded by the application. However, presently the thermal modelling of these devices is meagrely dealt in the literature as they have just entered into the field and has not been attempted in commercial scale deployments.

Figure 1. Cost distribution for a Silicon based Power Electronic System [2]

Thermal modelling of semiconductor devices is a standard followed to emulate operating conditions for determining the thermal stress on the device accurately [5]. Further, based on the results from this modelling technique, the heat sink size and other cooling techniques specifically to be appended for a particular application can be determined effectively. Generally, thermal modelling is carried out with the transient thermal impedance characteristics presented in the datasheets of any power semiconductor devices. But substantial data like the inner and outer dimensions, material characteristics and construction of the complete device are required [4][7] for a successful thermal modelling which are generally not made available by the device manufacturers. This curbs the development of a precise heat flow path representation through thermal equivalent networks, especially for the emerging wide band gap materials. Hence, high level of approximations is involved while estimating the junction temperature rise using the thermal equivalent networks [2] resulting in a sub-optimal cooling solution. This urged the development of an accurate thermal modelling with the available data from the manufacturer, with a higher level of accuracy and the same is presented in this paper. The proposed attempt is to accurately estimate the device temperature rise through the development of an electro-thermal model for off the shelf available SiCFET when utilized in a high frequency SPWM inverter. The results for three different thermal modelling techniques are compared and detailed analysis with illustrations are presented.

2. Data Interpretation of thermal impedance characteristics
The fundamental aspect of a power electronic system design is the interaction of power losses of an SiCFET with the thermal impedance of the system. With precise thermal modelling the power electronic system can be designed to handle high values of output current without exceeding the maximum junction temperature limits continuously and also be reliable in terms of power cycling. Thermal modelling of devices requires substantial data from the power device manufacturers about the inner and outer dimensions, material characteristics and construction of the complete device [4][7]. Due to limited availability of design data, development of a precise model for heat flow path representation is another crucial task. The transient thermal impedance characteristics provided in a datasheet are a combined effect of the thermal resistance and thermal capacitance of the physical structure of a power semiconductor device. The effective thermal analysis/modelling of the SiCFET or any power device can
be realized by the total power dissipation which is a function of conduction, switching and blockage losses. With the advantage of the behavioural analogy across thermal and electrical components, a thermal equivalent RC network model or electrothermal analysis of device can be constructed and validated on an equivalent platform.

Table 1. Analogy between Electrical and Thermal domain [9]

| Thermal         | Electrical       |
|-----------------|------------------|
| Temperature     | Voltage          |
| Heat Flow       | Current          |
| Thermal Resistance | Electrical Resistance |
| Thermal Capacitance | Electrical Capacitance |

| Temperature | T in K or °C |
|-------------|--------------|
| Heat Flow   | P in W       |
| Resistance  | Rth in K/W    |
|             | or °C/W     |
| Capacitance | Cth in Ws/K  |

The plot shown in Figure 2 depicts the changes in transient thermal impedance with respect to pulse width for IXFN50N120SiC is utilized to achieve the aforementioned thermal model. Generally, the thermal impedance plot in the data sheet is provided either for a single pulse or for a fixed duty ratio pulses [11]. However, at steady state the thermal impedance will be equal to the thermal resistance for larger pulse widths. For the proposed work, the SiCFET IXFN50N120SiC has been considered for detailed thermal analysis with three distinct strategies so as to identify an optimized choice for cooling solutions when the device is operating in a typical PWM inverter.

The first method is a curve-fitting technique employed using the steady-state value of thermal resistance of junction to case of the device and the transient thermal impedance plot to determine RC parameters of the thermal equivalent network. Whereas, the second method is an electro-thermal analysis of the power semiconductor device utilized in a high frequency SPWM inverter. The final method is thermal analysis using average heat dissipation in an actual 3-D model of the same SiC device.

2.1. Thermal Analysis of Compound Semiconductors using equivalent network models

The thermal behaviour of compound semiconductors can be described using different equivalent circuit models out of which the Cauer and Foster R-C network models are largely accepted [13]. The continued fraction network or Cauer filter model depicts the actual dynamic behaviour of the compound semiconductor based on thermal capacitances representing the thermal storage behaviour of the material.
along with intermediary thermal resistances. The individual RC-elements can be mapped to individual layers of the power device Viz. chip, chip solder, substrate, substrate solder, baseplate with the circuit nodes provide ingress to internal temperatures of the physical layers. The Cauer model shown in figure 3 can be established only when details of the material properties and correct mapping of the thermal spreading on the individual layers are known. Data for Cauer modelling are generally not made available by power semiconductor manufacturers. In stark contrast to Cauer model, the coefficients of Foster tank model can be easily extracted from a measured cooling curve of the power device and analytical estimations can be made easily. Generally Foster model of Figure 4 is preferred over Cauer model for estimating the thermal behaviour from the datasheet thermal impedance curve of power semiconductor devices [15].

\[ Z_{th}(t) = \sum_{i=1}^{n} R_i (1 - \exp(-t/\tau_i)) \]  

(1)

And the thermal capacitance can be determined from,

\[ \tau_i = R_i \times C_i \]  

(2)

After estimating the switching and conduction losses \( P_L(t) \) and with the assumption of a known case temperature \( T_C(t) \), the junction temperature \( T_J(t) \) can be determined from the equation 3 as shown below:

\[ T_J(t) = P_L(t) \times Z_{th}(t) + T_C(t) \]  

(3)

A simplified assumption of a constant case and heatsink temperature is not accurate as the load cycle is not negligible when compared to the heat sink time constants. For dynamic operating conditions either \( T_C(t) \) must be measured or the SiC model must be linked to a heatsink model. The thermal impedance curve is reproduced using data points from the transient thermal impedance plot provided in the datasheet. Further the plot is utilized to calculate the values of R-C elements of the Foster network through the curve fitting tool in MATLAB. The thermal impedance expressed in Equation 1 forms the base for fitting the plotted curve by extracting data points from thermal impedance plot. The package of SiCFET considered (IXFN50N120SiC) is SOT-227B package and ninth order thermal impedance befits the best for this power MOSFET with this package. Nine values of R-C parameters were determined from curve fitting. The actual thermal impedance graph and resultant curve fit for foster model are compared by plotting on the same time scale shown in figure 5.

The R-C parameters for Cauer thermal equivalent network model can be obtained directly from the device manufacturers. Here, the RC parameters of the Cauer network were estimated from the Foster network parameters using the software platform Piecewise Linear Electrical Circuit Simulation (PLECS). A ninth order Cauer and Foster RC network was used to model the thermal impedance characteristics of IXFN50N120SiC MOSFET. The thermal resistance and capacitance values represented in table 2 were established after curve fitting in MATLAB. The thermal equivalent circuit with RC values from table 2 is modelled in Simulink as shown in figure 6. The power dissipation profile for this simulation was from a computed average power dissipation of an 800 V SiC based SPWM inverter operating at 100 kHz and supplying a rms current of 30 A. The power profile is varied to match the average power dissipation of the inverter over a fixed time duration so as to result a typical temperature rise pattern. Now the heat sink can be selected to curtail the temperature rise beyond any desired value if present in the aforesaid temperature rise pattern. The junction temperature is analogous...
to the voltage measurement across the first capacitor in the network. The maximum power dissipation is 160W for a duration of 10ms and the equivalent junction temperature was found to be approximately 168°C from Cauer thermal network model.

![Figure 5. Plot of curve fit tool and actual transient impedance in MATLAB](image)

**Figure 5.** Plot of curve fit tool and actual transient impedance in MATLAB

|                      | Foster Model RC Parameters | Cauer Model RC Parameters |
|----------------------|---------------------------|---------------------------|
|                      | R-C values                | R-C values                | Units       |
| R1                   | 0.06667                   | 0.2482                    | K/W         |
| C1                   | 0.528123594               | 0.01187                   | J/K         |
| R2                   | 0.008861                  | 0.1517                    | K/W         |
| C2                   | 18.45164203               | 0.01187                   | J/K         |
| R3                   | 0.1974                    | 0.09511                   | K/W         |
| C3                   | 0.013424519               | 0.4947                    | J/K         |
| R4                   | 0.07207                   | 0.06191                   | K/W         |
| C4                   | 15.4155682                | 1.346                     | J/K         |
| R5                   | 0.06968                   | 0.0282                    | K/W         |
| C5                   | 3.892078071               | 5.185                     | J/K         |
| R6                   | 0.09297                   | 0.01432                   | K/W         |
| C6                   | 0.157685275               | 7.624                     | J/K         |
| R7                   | 0.01278                   | 0.02013                   | K/W         |
| C7                   | 4.120500782               | 22.23                     | J/K         |
| R8                   | 0.08157                   | 0.004021                  | K/W         |
| C8                   | 1.218953046               | 59.76                     | J/K         |
| R9                   | 0.02166                   | 7.99E-05                  | K/W         |
| C9                   | 9.173591874               | 234.2                     | J/K         |

**Table 2.** A summary of RC parameters for Foster and Cauer thermal equivalent networks

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2.2. Electro-Thermal Analysis of Compound Semiconductors using PLECS

A much more accurate junction temperature estimation can be carried out by electro-thermal analysis using the simulation tool PLECS. PLECS is a software developed by Plexim for system-level simulations and design of power electronic circuits. In PLECS any power device can be affixed with thermal components like heat sinks of any rating as desired by the system designer. The electrical and
thermal network is represented in a unified model of PLECS is shown in figure 7. The conduction, turn-on and turn-off switching losses obtained from the datasheet for different temperatures were defined as simulation parameters as shown in figure 8, in order to account them into the inverter power loss and the subsequent device temperature rise. An operating voltage of 800 V with a continuous RMS current of 28.28 A flows through the SiCFET with an RL load connected at the inverter output.

![Cauer Thermal Equivalent Circuit](image)

**Figure 6.** Cauer Thermal Equivalent Circuit

Various switching frequencies in the range of 10 kHz to 1 MHz has been considered to operate the inverter at the aforementioned load conditions. The required thermal resistance for heat sink was estimated from the conduction and switching losses of the SiC devices used in the simulation. A steady state analysis for the SiCFET was performed in PLECS and the maximum junction temperature rise for each switching frequency was found and the same is used to estimate the corresponding value of heat sink. This method gives much more accurate result than the Cauer and Foster model as the input power loss profile is not approximated from that of the exact dissipation profile.

![Electro-thermal Analysis of SiCFET with heat sink based SPWM Inverter in PLECS](image)

**Figure 7.** Electro-thermal Analysis of SiCFET with heat sink based SPWM Inverter in PLECS

The power dissipation and junction temperature rise of the SiC device was observed for different switching frequencies at steady state. The heat sink volume [12] can be computed using,

\[ V_{(\text{Heat Sink})} = \frac{R_v}{\theta_{st}} \]  

(4)
Where \( V \) is the Volume of the heat sink, \( R_V \) is the volumetric resistance expressed in \( \text{cm}^3 \degree \text{C/W} \) and \( \theta_{SA} \) is the thermal resistance in \( \degree \text{C/W} \). The volumetric resistance was taken from the table given in reference [12]. The volume of heat sink and its thermal resistance required has been computed using equation (3) and can be plotted for further analysis. The width of heat sink is observed to play a vital role in the performance of heat sink [12].

2.3. Thermal Analysis of SiC MOSFET in Solidworks

Solid Works Simulation provides a platform to carry out analysis to manage heat, validating miniaturized concepts, and building in reliability which can be addressed at the initial product development cycle itself so as to result a higher quality design with reduced failure issues. The principle of conduction, convection and radiation is applied during thermal analysis to CAD model of actual semiconductor device for simulating various thermal boundary conditions. Generalized procedure for analysis would be (1) meshing the design, (2) setting any relevant constraints and (3) configuring power or heat flux conditions associated with a physical structure of the model. As material properties of power semiconductor component includes coefficient of thermal expansion, thermal conductivity, and heat capacity, an accurate prediction of temperature distributions under stipulated loads and wide operating conditions can be achieved. A 3D model and meshing of the IXFN50N120SiC in SOT-227 (minibloc) package was created in SOLIDWORKS as shown in figures 9 and 10 respectively. The thermal analysis was carried out for a power dissipation of 80 W calculated for electro-thermal Inverter model operating at 100 kHz dissipation in PLECS and boundary conditions for conduction, convection and radiation were configured.

3. Results

The junction temperature rise is estimated for the corresponding power profile plot applied to the thermal equivalent circuit models shown in figure 11. This kind of modelling technique can be utilized initially
for off the shelf available wide band semiconductors to determine their junction temperature profile for different operating conditions. The major setbacks of this technique is the assumption of a constant case to ambient temperature. The maximum rated junction temperature of IXFN50N120SiC as per the datasheet is 175°C. The thermal equivalent model of the semiconductor module in datasheet is established by a measurement in combination with a specific heatsink. An air cooled heatsink has exhibited a lower Rθ(j-c) and lead to a wide spread heat flow. The junction temperature rise in figure 11 is not accurate due to reverse effect on the thermal spreading in the device. Hence the linking of SiC device and heat sink is found not accurate either in the Cauer or Foster model.

Figure 11. Junction temperature rise of IXFN50N120SiC by using Cauer and Foster thermal modelling techniques

A steady state thermal analysis for IXFN50N120SiC utilized in high frequency SPWM inverter was performed using PLECS and maximum junction temperature for different switching frequencies were observed. A Steady state plot of temperature rise and heat flow for switching frequency of 0.5 MHz is shown in figure 12. Such a high switching frequency has greatly contributed in the reduction in size of the low pass filter at the inverter output for the same harmonic profile. The output current of inverter switched at 0.5 MHz is shown in figure 13.

Figure 12. Steady state analysis of rise in junction temperature of IXFN50N120SiC with heat sink by using electrothermal analysis using PLECS

The trend of the heat sink volume and the required heat sink thermal resistance for varying switching frequencies are shown in figure 14 and from which it can be validated that the selection of operating switching frequency is a compromise between inverter performance and system enclosure volume. Obviously, heat sinks with lower thermal resistance will demand large volume. Enclosure with better ventilation, forced cooling like fans or blowers has to be utilized if it is desired to bring down the size of heat sink. Else the rise in ambient temperature will cause decrease in the rate of heat flow due to convection and radiation until a thermal protection trips the converter circuit. The exact junction temperature rise can be estimated using thermal simulation of the IXFN50N120SiC in SOLIDWORKS where all factors like conduction, convection and dissipation were effectively considered. The temperature rise on the entire geometry of SiCFET estimated by SOLIWORKS is presented in Figure 15 and it can be observed that it reaches as high as 160.3°C.
Figure 13. Output Voltage and a very low THD Current profile of SiC inverter operating at switching frequency of 0.5 MHz

Figure 14. Heat Sink volume and thermal resistance with respect to frequency for Natural Convection

Figure 15. Thermal analysis of 1XFN50N120SiC using SolidWorks.

4. Conclusion
The thermal characteristics of SiCFET are more robust when compared to that of conventional silicon MOSFET. It is comprehended that, SiCFET’s can operate at very high switching frequencies in the order of MHz, leading to steep decrease in footprint of passive elements like filters, inductors and capacitors. Estimating the exact junction temperature rise of a power semiconductor device aids in optimizing the cooling technique for the design. The electro-thermal analysis is found to be better than foster or Cauer analysis as it considers dissipation due to conduction, switching and blockage losses.
Due to reverse effect on the thermal spreading in the device, the linking of SiC and heatsink is not accurate either in the continued fraction or in the partial fraction model. A way to counter this issue is to model complete thermal path from junction via module, thermal grease, heatsink to ambient. A substantial variation of case ambient temperature will occur due to convection and radiation at power device case. Analysis using SOLIDWORKS was found to be most effective among all for effective temperature estimation for heat sink selection. The dimension of heat sink for low thermal resistance will be high and so forced convection must be utilized in tandem with smaller heat sinks having higher thermal resistance for achieving drastic reduction in cost and size of the converter.

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