A Low-distortion Hardware Efficient MASH $\Sigma \Delta$ Modulator with Enhanced Noise Shaping

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ABSTRACT

This paper proposes an improved multi-stage noise shaping $\Sigma \Delta$ modulator architecture that can attain an enhanced noise shaping through analog inter-stage feedback paths. The elimination of the feed-forward adder before the quantizer in the first stage and enhanced noise shaping without any increase in the number of active blocks makes this architecture hardware efficient. The shifted loop delay techniques utilized in this architecture helps to relax the signal processing timing issues in digital to analog conversion and dynamic element matching process. The low-distortion architecture in both stages of MASH structure reduces the integrator associated non-idealities. The resolution of this modulator is further improved by noise transfer function zero optimization methods. The low-distortion architecture, selection of low oversampling ratio, fewer number of adder and active blocks and achievement of fourth-order noise transfer function makes this modulator suitable for low power wideband applications. The behavioral simulations and mathematical analysis confirm the effectiveness of this proposed modulator.

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1. Introduction

The demand for high-performance and low power electronic systems often required in next generation wideband applications has intensified the research attention toward developing new efficient wideband analog to digital converter (ADC) architectures. ADC
act as a key element in many communication systems. Compared to other kind of ADCs, sigma delta ADC (ΣΔ ADC) is well suited for medium to high resolution wideband applications. ΣΔ ADC achieves high resolution through oversampling and noise shaping techniques [1]. The ADCs used in higher bandwidth applications are often designed at low oversampling ratio (OSR) due to CMOS technology scaling constraints. A low value of OSR will obviously decrease the achievable signal to noise ratio (SNR). The techniques to improve the resolution in the case of low OSR include increasing the order of loop filter and employing a multi-bit quantizer. The cascaded or multi-stage noise shaping (MASH) ΣΔ modulator architecture eliminates the loop filter instability problems associated with the single-loop higher order ΣΔ modulator structures and became appropriate for the broadband applications. In MASH architecture, the quantization noise of the first-stage modulator is extracted and provided to the next stage as input. An appropriate digital signal processing logic cancels the quantization noise of all except the last stage. The last stage quantization noise is shaped by a noise transfer function (NTF) of order equal to the sum of all the orders.

In input feed-forward or low-distortion architecture, the input signal is added directly before the quantizer and the integrators in the loop filter process only the quantization noise [2]. The analog feed-forward path structure causes a reduction in the output swing of integrators and minimizes the integrator associated non-idealities. This relaxes the settling and DC gain requirements on the integrator active block. However, the low-distortion architecture also suffers a drawback, the analog adder before the quantizer needs to be implemented either by a passive or active circuit. The passive adder circuit does not need an extra op-amp, but the active adder requires a fast power-hungry op-amp. The passive adder will be effective when the number of quantizer bits is small. In the case of multi-bit quantization, a buffer is needed between the switched capacitor circuit network and the quantizer for proper operation.

An improved low-distortion architecture saves one adder and the number of active blocks, required to implement the improved low-distortion ΣΔM, is decreased by one [3]. A shifted loop delay topology [4], relaxes the timing issues in the feedback path. Several techniques have been proposed in the literature to enhance the noise shaping ability of modulator, especially in broadband applications with low OSR. Noise coupling techniques or error feedback modulator [5,6], VCO-based quantizer [7], and resonation-based structures [8,9] are the techniques to enhance the order of noise transfer function. The local resonation technique used in MASH ΣΔM enhances the resolution, but it affects the digital cancelation logic [8]. In global resonation, a scaled version of last stage quantization noise is injected before the first quantizer with the help of inter-stage feedback paths [9,10]. The resonation techniques help to move the zeros of the NTF from dc to an optimal place in the signal band. The in-band quantization noise gets minimized by these shifting of zeros from dc to a frequency within the signal band [11]. A MASH 2-1 architecture could also attain fifth-order noise shaping through inter-stage feedback paths [12,13].

A MASH 2-1 ΣΔ Modulator which utilizes analog inter-stage paths and noise transfer function zero optimization for a higher reduction in in-band noise is shown in Figure 1 [9]. This architecture requires a feed-forward adder before the quantizer in the first stage.

The outline of the paper is as follows: Section 2 deals with the proposed MASH ΣΔ Modulator. The simulation results are presented in Section 3. Switched capacitor
implementation of the proposed architecture is described in Section 4. Section 5 concludes the paper.

2. Proposed MASH Architecture

Figure 2 shows the improved MASH 2-1 architecture. This proposed architecture utilizes the improved feed-forward topology and it offers many advantages. This third-order modulator attains an enhanced fourth-order noise shaping with fewer active blocks. A portion of the second-stage quantization noise injected into the first stage acts as a dither signal there. Moreover, the unity signal transfer function (STF) relaxes the analog circuit non-idealities. A shifted loop delay topology, introduces delay in the feedback path, which is used to relax the signal processing timing for digital to analog conversion (DAC) and dynamic element matching techniques (DEM). In this architecture, the adder block before the quantizer is shifted to the input of second integrator and an extra feedback path is inserted in the modulator loop. This saves one power hungry feed-forward active adder required in multi-bit quantization. The mathematical analysis of the proposed modulator shows, how a third-order modulator can achieve a fourth-order NTF using inter-stage feedback paths. The output of first and second stage of MASH structure is given by

\[
Y_1(z) = X(z) + \frac{1}{g}z^{-1}(1 - z^{-1})^2 V(z) + E_1(z)(1 - z^{-1})^2
\]  

where \( X(z) \), \( Y_1(z) \), and \( E_1(z) \) represents the input signal, output of the first stage and quantization noise of the first stage of MASH structure, respectively. The inter-stage gain is represented by \( g \). \( V(z) \) is the output of the integrator in the second stage of MASH architecture.

\[
Y_2(z) = \left[ gE_1(z)z^{-1} - Y_2(z)z^{-1} \right] \frac{1 + h}{1 - z^{-1}(1 + h)} + gE_1(z) + E_2(z)
\]

The output and quantization noise of the second-stage modulator are denoted by \( Y_2(z) \), and \( E_2(z) \).
The second stage of the proposed modulator shown in Figure 2 is simplified through block reduction methods and the resulting structure is shown in Figure 3.
Figure 5. Location of the optimized NTF zeros.

The integrator output in the second stage, $V(z)$ is injected into the first stage through analog feedback paths. The $V(z)$ signal is delayed and added at the input of last integrator in first stage. The signal $V(z)$ can be obtained as

$$V(z) = \frac{1}{1 - z^{-1}(1 + h)} \left[ gE_1(z)z^{-1} - Y_2(z)z^{-1} \right]$$

$$Y_2(z) = gE_1(z) + E_2(z) \left[ 1 - z^{-1}(1 + h) \right]$$

The NTF of the second-stage modulator is

$$\text{NTF}_2(z) = 1 - z^{-1}(1 + h)$$

$$V(z) = -z^{-1} \text{NTF}_2(z)E_2(z)$$

$$V(z) = -z^{-1}E_2(z)$$

Substituting $V(z)$ in Equation (1), we get

$$Y_1(z) = X(z) - \frac{1}{g} z^{-2}(1 - z^{-1})^2 E_2(z) + E_1(z)(1 - z^{-1})^2$$

The overall output of the modulator is represented by $Y(z)$

$$Y(z) = Y_1(z) - \frac{1}{g_{\text{dig}}} (1 - z^{-1})^2 Y_2(z)$$

we assume that there is good matching between analog and digital coefficients, then $g = g_{\text{dig}}$

$$Y(z) = X(z) - \frac{1}{g} (1 - z^{-1})^2 \left[ 1 - z^{-1}(1 + h) + z^{-2} \right] E_2(z)$$

If the value of $h = 1$, then

$$Y(z) = X(z) - \frac{1}{g} (1 - z^{-1})^2 \left[ 1 - 2z^{-1} + z^{-2} \right] E_2(z)$$
The output $Y(z)$ contains the input signal and the shaped quantization noise of the second-stage modulator. The first-stage quantization noise has completely eliminated and the second-stage noise is shaped by an NTF of order four.

The easiest method to have a further increase in SNDR, in higher order modulators utilized in wideband applications is to optimally place a pair of complex conjugate zeros of the NTF from dc to a frequency $f_0$. The in-band quantization noise gets minimized by these shifting of zeros from dc to a frequency within the signal band. The reduction in in-band noise will ultimately results in a better SNDR value. In order to obtain an optimum value for $h$, let’s examine an $L$th order $\Sigma\Delta$ modulator. If $L \geq 2$, then the NTF can be represented by, $\text{NTF}(z) = (1 - z^{-1})^{L-2}(1 - \delta z^{-1} + z^{-2})$ [14].

Similarly, $h$ can be calculated as

$$h = 2 \cos \left( \frac{2\pi f_0}{f_s} \right) - 1$$

where $L$ is the order of NTF and $f_{BW}$ is the signal bandwidth, the optimum value for the coefficient $h$ is

$$f_0 = \sqrt{\frac{2L - 3}{2L - 1}} f_{BW}$$

The value of $h$ corresponding to maximum SNDR can also be verified using behavioral simulations. Figure 4 shows the variation of SNDR with the coefficient $h$. It also confirm that the maximum value of SNDR will be obtained, when $h$ hold the value 0.89. The pole–zero plot provides the location of the NTF zeros. Since the NTF is of order four in the proposed architecture, we have four zeros. Figure 5 shows the position of zeros, two zeros are located at dc and the shifted complex conjugate pair zeros are located at $0.945 \pm 0.327i$, which is within the signal band. By adjusting the value of a single coefficient $h$, we were able to optimize the NTF zeros.

In the proposed MASH structure, the half-clock period delay ($z^{-1/2}$) of the first integrator is shifted to the input signal and feedback paths. The half-delay in the feedback path helps to relax the speed requirement for DEM logic operation, which can be easily realized in transistor level by holding half phase. This modulator also shifts one loop delay ($z^{-1}$) from the second integrator of first stage into the newly formed feedback branch to stabilize the loop. The delay in the input signal path helps to maintain the low-distortion property. Both stages of this architecture use the shifted loop delay techniques.

3. Simulation Results

The behavioral simulations were conducted to evaluate the performance of the proposed MASH architecture shown in Figure 2 using MATLAB and SIMULINK. The OSR, bandwidth (BW) and sampling frequency ($F_s$) used in all the simulation were 8, 10 MHz and 160 MHz, respectively. Four bit quantizers were used in both stages of the modulator with an inter-stage gain ($g$) of value 4. Figure 6 depicts the power spectral density (PSD) plot
Figure 6. PSDs of proposed and conventional MASH 2-1 Modulator.

Figure 7. SNDR vs. Input signal amplitude.

comparison between the proposed architecture and the conventional feed-forward MASH structure. We can observe a notch near 10 MHz for the proposed, which is lying inside the signal band [0, \( f_{BW} \)]. The optimal value of the coefficient \( h \) places a pair of complex conjugate NTF zeros inside the signal bandwidth and it will leads to a reduction in the in-band noise. This will contribute to a further increase in the resolution of the proposed MASH structure.

The proposed architecture along with the traditional feed-forward MASH 2-1 architecture, MASH modulator with highly reduced in-band quantization noise [9], MASH 2-2 with global resonance [15] were simulated, and plotted the SNDR against input amplitude swept from –100 to 0 dB in Figure 7. The PSDs of the node voltages \( V_1, V_2, V, Y_1, Y_2 \) and \( Y \) marked in Figure 2 are depicted in Figure 8. The node \( V_1 \) is before the first integrator, its PSD plot indicates the absence of any signal component because of low-distortion topology. A comparison of the output swing of the three integrators in the proposed MASH architecture is shown in Figure 9. The histogram output of the first integrator shows the presence of quantization error alone due to the swing suppression feature of the low-distortion topology. Since the feed-forward input is directly added at the input of the second integrator, its output swing is more compared to other integrators.
3.1. Non-ideality Analysis

The analysis of the proposed modulator against different non-idealities like finite op-amp gain, finite slew rate and finite gain bandwidth (GBW) were performed and compared with other MASH structures based on the models proposed in [16]. In order to have a fair comparison in the result, all the structures were simulated for the same OSR, BW and $F_s$ mentioned above. Input amplitude of –2 dB with reference to the full-scale level is used to compare the SNDR. The variation in SNDR when different circuit non-idealities were introduced are shown in Figure 10. The minimum gain required for the op-amp in the proposed modulator is 60 dB. From Figure 10, we could understand that the op-amp gain requirement for these MASH architectures with inter-stage feedback path is almost same. The variation in SNDR of the proposed architecture as a function of GBW and slew rate
Figure 9. Output swing of the integrators in the proposed modulator.

Figure 10. SNDR variation with (a) op-amp gain (b) slew rate (c) gain bandwidth for the proposed modulator.
Figure 11. SNDR variation of the proposed architecture as a function of GBW and slew rate.

Figure 12. SNDR variation vs. mismatch between analog inter-stage gain $g$ and its digital estimate $g_{\text{dig}}$.

is shown in Figure 11. The GBW and slew rate requirements are almost the same when compared with other two architectures.

3.2. Matching Requirements in MASH Architecture

The matching between the analog and digital circuits is highly essential in MASH structures, otherwise it may lead to the leakage of quantization noise. A good matching between analog loop filter and digital noise cancelation filters often demand high-gain operational
amplifiers and accurate modulator coefficients. The SNDR value is sensitive to the disparity between digital and analog coefficients. The degradation in SNDR vs. mismatch between the analog coefficient \((g)\) and digital coefficient \((g_{\text{dig}})\) in the proposed architecture is shown in Figure 12. A \(\pm 5\%\) variation in analog and digital coefficients leads to a degradation of 22 dB in SNDR.

4. Switched Capacitor Implementation of the Proposed Modulator

The single-ended switched capacitor implementation of the proposed MASH modulator is shown in Figure 13. This architecture requires three integrators and an active feed-forward adder in the second stage for the operation. A 4-bit quantizer has been implemented using 15 clocked comparators. The inter-stage feedback paths are connected at the input of the second integrator, so it does not need a separate op-amp for the implementation. It can be implemented using passive components.

The PSDs of the node voltages depicted in Figure 8 indicates the absence of signal component in \(V_1\). Also, the histogram output of the first integrator represented in Figure 9
Figure 14. Monte Carlo simulations for Capacitor mismatch ($C_G$).

(a) Variation in SNDR for 1000 iterations by considering ±1% mismatch in $C_G$

(b) corresponding Histogram results

Figure 14. Monte Carlo simulations for Capacitor mismatch ($C_G$).
Figure 15. Monte Carlo simulations for Capacitor mismatch ($C_F$).

(a) Variation in SNDR for 1000 iterations by considering ±1% mismatch in $C_F$.

(b) corresponding Histogram results
Table 1. Performance summary.

| Parameter          | Conventional MASH 2-1 with highly reduced in-band quantization noise [9] | MASH 2-2 with global resonation [15] | This work |
|-------------------|--------------------------------------------------------------------------------|---------------------------------------|-----------|
| Architecture      | MASH 2-1 with inter-stage feedback | MASH 2-2 with inter-stage feedback | MASH 2-2 with inter-stage feedback |
| $F_s$             | 160 MHz                                         | 160 MHz                                   | 160 MHz                |
| Bandwidth         | 10 MHz                                          | 10 MHz                                   | 10 MHz                 |
| OSR               | 8                                               | 8                                        | 8                      |
| SNDR$_p$ (dB)     | 78.2                                           | 98.5                                     | 98.5                   |
| DR                | 79                                             | 99                                       | 99                     |
| Order of NTF      | 3                                               | 4                                        | 4                      |
| No. of Integrators| 3                                               | 3                                        | 4                      |
| No. of feed-forward adder | 2                              | 2                                        | 1                      |

confirms the absence of input signal. So the first stage of MASH structure maintains the low-distortion property. It is clear that the first integrator process only the quantization noise. The output of the first integrator is provided as the input to the second stage. Two non-overlapping clocks $\phi_1$ and $\phi_2$ used for the operation of the circuit.

The scaling coefficients were realized by the ratio of sampling and integrating capacitances. In Figure 13, the capacitance $C_F$ contribute to the inter-stage feedback path gain and the inter-stage gain $g$ is realized using the capacitor $C_G$. The architecture proposed here is tested against the effect of capacitor mismatches by performing a Monte Carlo simulation of 1000 iterations. The degradation in the value of SNR due to mismatch in capacitor values can be analyzed through this simulation. The simulations were conducted for the capacitor values $C_G$ and $C_F$ by assuming a mismatch of ±1% in the capacitor values. The capacitor values are randomly selected, Gaussian-distributed and the resulting SNR values are plotted. The variation in SNR due to capacitor mismatch and the resulting histogram output based on Monte Carlo simulation are shown in Figures 14 and 15.

The performance summary of the proposed architecture is shown in Table 1. The proposed modulator achieves an SNDR$_p$ of value 98.5 dB and a dynamic range of 99 dB. The proposed MASH structure achieves the same performance and saves one feed-forward adder, when compared with MASH modulator with highly reduced in-band quantization noise [9]. It could also attain an identical performance when compared with MASH 2-2 with global resonation [15], while saving one integrator and adder.

5. Conclusion

A multi-stage noise shaping $\Sigma\Delta$ architecture that utilizes only fewer active blocks for attaining a fourth-order noise shaping is presented. The enhancement in the resolution is achieved through inter-stage paths and NTF zero optimization methods. The low-distortion architecture, reduction in active components and elimination of a power hungry adder helps this modulator to be used in low power applications. The shifted loop delay techniques solve the timing issues in the critical path of the modulator. The behavioral simulations, mathematical analysis and an SNDR and dynamic range of value above 90 dB prove the fitness of this modulator to be used in wideband applications.
Disclosure Statement

No potential conflict of interest was reported by the authors.

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