Design of Cryogenic CMOS LNAs for Space Communications

Mahesh Mudavath¹, Sresta Valasa², Avunoori Saisrinithya³ and Amgothu Laxmi Divya⁴

¹Associate professor, Department of ECE, Vaagdevi College of Engineering, Warangal (Telangana State), India
²,³,⁴ M.Tech Scholar, Department of ECE, Vaagdevi College of Engineering, Warangal (Telangana State), India

*Corresponding author E-mail: mahesh_m@vaagdevi.edu.in, shreshtavalasa@gmail.com, asaisrinithya@gmail.com, laxmidivya213@gmail.com

Abstract: This manuscript presents the 45nm CMOS Low Noise Amplifier (LNA) designed for cryogenic use in spaces. A revised approach has been adopted to classical LNA architecture. External discreet components were added to the LNA in such a way that the LNA S₁₁ and S₂₂ were under −10dB from 70K to 290K at 2.44GHz designated for spatial communications. The LNAs IIP₃ performance was analyzed, in particular at cryogenic temperatures, and linearity improvements were demonstrated by using the proposed approach. Although the LNA was not specifically hardened by radiation, no degradation was observed in its performance. Results analysis present that LNA achieves input and output impedance matching’s of -24.024 and -23.131dB, NFs of 0.9dB, power gain of 26.7dB, P-1dB of -10.63dBm, IIP₃ of -10.6dBm at 2.44GHz, respectively.

Index Terms—Low noise amplifier (LNA), cryogenics, CMOS, noise figure, linearity.

I. INTRODUCTION

In many applications, cryogenic semiconductor technology is used either for its improved efficiency in high-energy and nuclear physics experiments to minimize thermal noise or for its operability in harsh environments in quantum computing and space (deep) applications [1]. While several technologies are permitted at cryogenic temperatures, simply the complementary metal oxide semiconductor (CMOS) enables billions of transistors to be integrated into a single chip, thanks to the evolvement made under Moore's legislation [3]. Thus, CMOS deals the best choice for the potential incorporation of multifaceted and accessible cryogenic microelectronic systems [2].

Because of numerous rapidly emerging low-temperature applications, the design of the cryogenic LNA circuit has recently become a research subject. Due to harsh environmental conditions, sensors and communication circuits in space electronics can work at temperatures below 100K. Moreover in infrared sensors and bio-molecular detectors, cryogenic of the front-end receiver is generally used to increase sensitivity, thus reducing the contribution of thermal noise [4]. The LNA must be able to offer adequate amplification, but it should not be greater such that the next stages are saturated. It should introduce small amounts of external noise into the device. It should also be linear enough to conform to high-power interferences coming from the wireless interface. For communication systems, the LNA role is used to
amplify poor signals received by an antenna. It is located far closer to the aerial, so that feed line losses are less critical [9].

II. LITERATURE SURVEY

There are several cryogenic LNAs in the literature which have been developed using different device technologies. However, the performance of CMOS LNAs has not been recorded satisfactorily at cryogenic temperatures [1][2]. In contrast to competing system technologies such as silicon germanium (SiGe), HBT, HEMT amplifiers and silicon-on-insulator (SOI) transistor technologies, cryogenic LNA design must be newly of particular interest [2]. A moderately long lifetime can be achieved for CMOS devices at room and cryogenic temp., under low drain-source operating voltages. Usually, because of greater carrier mobility, the CMOS LNA the noise figure (NF) decreases principally and power gain tends to increases with relation to the decrease in temperature. Only one paper presents IIP3 output with measurement results at room and cryogenic temperatures among the associated work on cryogenic LNAs, in which it is claimed that IIP3 decreases as the temperature droplets [5].

The overall linearity based on the efficiency of the gain of additional phases, so it is difficult to infer the real linearity performance at cryogenic temperatures. In addition, a separate study proposes that at cryogenic temperatures [6]. However, this assumption is based on performed simulations using a cryogenic SiGe (HBT) device model, the accuracy of which has not been thoroughly verified by the measurement results. Therefore in cryogenic environments, the linearity properties of LNAs have not yet been extensively researched.

III. PROCEDURE OF LNA DESIGN

This paper's innovation lies for the first time in the linearity analysis and enhancement of a cryogenic cascode-LNA using the linearity principle. The conventional methodology of LNA is based on the instantaneous balancing of input and noise, somewhere linearity is optimised by proper transistor sizing. In order to fit cryogenic conditions, this approach has been updated, thereby maintaining IIP3 efficiency characteristics [2][18]. An LNA configuration using this technique is implemented and seen at 77K in the 45 nm CMOS technology, which corresponds to the temperature of liquid nitrogen. In this job, it is presumed that most of the crucial applications linking space electronics will cover 77K [4].

By using cryogenic transistor models, cryogenic circuit design can be achieved. As an alternative, by studying the behavior of transistors at cryogenic temperatures, the circuit built with typical device models can be adjusted for cryogenic conditions [12]. In this study, the second approach was chosen because of its more realistic design [10]. The design has been carried out in such a way that the LNA bias can be modified to achieve the desired specifications at 77K. In addition, instead of more sophisticated topologies, the cascade LNA structure was chosen to specifically demonstrate the dependence of LNA metrics on various design constraints shown in Figure 1[7].

In this schematic, two transistors were used in parallel for both the CS and CG phases, and both pair is signified as transistor (M1 and M2) in the schematic as shown in Figure 1[13]. In order to maximize the noise temperature of the LNA as drawn in, a capacitor was placed amongst the gate-source of the CS [8][9].

The major issues in cryogenic LNA design are the optimization of DC operational points, impedance matching, and linearity at cryogenic temperatures. Although the cascade is a one-stage amplifier, for the sake of linearity, it can also be interpreted as a two-stage structure [11]. The overall AIP3, then, will become:

\[
\frac{1}{\text{IIP3}_{\text{Total}}} \cong \frac{1}{\text{IIP3}_{\text{CS}}} + \frac{A_{VCS}^2}{\text{IIP3}_{\text{CG}}} \tag{1}
\]

Where, \(A_{VCS}^2\) is the CS-stage gain.
By simulation, it was verified that the CS-stage gain is greater than unity; thus, in the linearity expression, $AIP_3$ of the CG-stage is the prevailing term [11]. This means that the overall temperature-based $AIP_3$ change is calculated by the linearity variation of the CG-stage due to temperature. The CG amplifier in Figure 1 has, therefore, been studied as a separate single stage for its $AIP_3$. $RD$ is the actual impedance at the operation frequency of the load matching circuit, and $RS$ is the input port resistance, which is usually 50Ω in RF circuits [14] [15].

A linearity analysis is provided for CS amplifiers by ignoring the body effect and the channel length modulation. In this analysis, the CS transistor is presumed to be in strong inversion and, as in equation (2), the $AIP_3$ of the CS is obtained [16].

$$AIP_3_{CS} \approx \frac{4}{3} \frac{\alpha_1}{\alpha_3} = \frac{2\beta_1 (1+\beta_1 R_1)^2}{K_1}$$  \hspace{1cm} (2)$$

Where, $K_1 = \frac{1}{2} \mu_C C_{ox} \left( \frac{W}{L} \right)_1$, and resistance $R_1$ is the CS transistor of the source generation. Also, $\alpha_1$ and $\alpha_3$ are the CS stage of first and third-order transconductances, respectively. For the CG stage, while the similar linearity analysis is executed, as the signal is applied to the source terminal of the CG amplifier, only the signs of $\beta_1$ and $\beta_3$ in the drain current ($i_{out}$) expression (3) of the CG stage differ from $\beta_1$ and $\beta_3$. Thus, the CG amplifier’s $AIP_3$ expression is principally the same as the CS stage $AIP_3$ expression as shown in (4).

$$i_{out}(v_{in}) = \beta_1 v_{in} + \beta_2 v_{in}^2 + \beta_3 v_{in}^3 \cdots \cdots \cdots$$  \hspace{1cm} (3)$$

$$AIP_3_{CG} \approx \frac{4}{3} \frac{\beta_1}{\beta_3} = \frac{2\beta_2 (1+\beta_2 R_2)^2}{K_2}$$  \hspace{1cm} (4)$$

Figure 1. The schematic of designed cascode-LNA
If (4) is expressed by assuming that $g_{m2}R_s >> 1$ in terms of drain current $I_D$, then (4) becomes:

$$AIP3_{CG} \approx 8I_D R_s^2 \frac{I_D}{3R_s(V_{GS2} - V_{TH2})}$$  \hspace{1cm} (5)$$

The equation (5) is the IIP3 of the CG-stage. Moreover, because the threshold voltage ($V_{TH2}$) rises, linearity can also increase. Finally, as seen in (6), the gain of the CS drops with the increase in $g_{m2}$, which is due to the rise in $V_{TH2}$ [17].

$$A_{V1} = \frac{R_{D} + r_{o2}}{1 + g_{m2}r_{o2}} \frac{\sqrt{(L_1 + L_0)C_{GS1}}}{2L_1}$$  \hspace{1cm} (6)$$

Where, $L_1$ and $L_0$ are respectively inductors for source degeneration and input matching. The overall capacitance value amongst the source and gate of CS transistor and the output of CG drain resistance respectively $C_{GS1}$ and $r_{o2}$. As given in (1), the decrease in $A_{V1}$ also has a positive effect on the overall linearity. For the operating voltage at which the room and cryogenic temperatures, provides the same current value.

**IV. RESULTS AND DISCUSSION**

The LNA circuit’s design parameters are evaluated with respect to the 2.44GHz operating frequency. Figure 2 to Figure 7 displays a plot of the s-parameters and necessary parameters. The obtained $S_{21}$ (power/voltage transmitted to port2 from port1) = $\frac{b_2}{a_1} \bigg|_{a_2=0} = 26.7$dB plot shown in Figure 2.

![Figure 2](image_url)  
Figure 2 The maximum gain of the LNA at 2.44 GHz is 26.7 dB
$S_{12}$ (power/voltage transmitted to port1 from port2) = $\frac{b_2}{a_1}$ as $a_{1=0} = -48$dB plot shown in Figure 4.

Figure 3 The NF and NF minimum of the LNA at 2.44GHz is 0.9dB

Figure 4 Simulated reverse isolation ($S_{12}$) = -48dB @2.4GHz center Frequency

Figure 5 The impedance matching ($S_{11}$ and $S_{22}$) are -24.2dB each.
$S_{11}$ (ratio of input power to reflected voltage back to port-1, not transmitted) = \frac{b_1}{a_{11}a_{22}} = -24.2\text{dB}

$S_{22}$ (ratio of output power to reflected voltage back to port-2, not transmitted) = \frac{b_2}{a_{22}a_{11}} = -24.1\text{dB} \text{ plot is shown in Figure 5.}

1-dB compression point is the input signal level that drives the small-signal gain to drop by 1dB. It is obtained as -10.6dBm at a 2.44GHz frequency as shown in Figure 6.

![Figure 6 The P1dB of the LNA is -10.6dB](image)

![Figure 7 The IIP3 of the LNA is -10.6657 dB](image)

A report on comparative studies taken in regards to directions for proposed work could tabulate in Table 1.
A report on comparative studies taken in regards to directions for proposed work could tabulate in Table 1.

Table 1: Performance summary and comparison of CMOS LNAs

| Parameters         | This work | [1] | [2] | [18] |
|--------------------|-----------|-----|-----|------|
| Center Frequency (GHz) | 2.44     | 2   | 2   | 2.3  |
| CMOS Tech. (nm)    | 45        | 180 | 180 | 180  |
| Power Gain (dB)    | 26.7      | 18  | 25  | 23.8 |
| Noise Figure (dB)  | 0.9       | 2.2 | 2.3 |      |
| $S_{11}$ (dB)      | -24.4     | -15 | -10 | -18  |
| $S_{12}$ (dB)      | -48.3     |     |     |      |
| $S_{21}$ (dB)      | 26.7      | 18  | 25  | 22.8 |
| $S_{22}$ (dB)      | -23.4     | -13 | -20 | -25  |
| Power supply (V)   | 1.2       | 1.8 | 1.8 |      |

V. CONCLUSION
The LNAs IIP$_3$ performance was analyzed, in particular at cryogenic temperatures, and linearity improvements were demonstrated by using the proposed approach. Results analysis present that LNA achieves in and out impedance matching of -24.024 and -23.131dB, NFs of 0.9dB, power gain of 26.7dB, P-1dB of -10.63dBm, IIP$_3$ of -10.6dBm at 2.44GHz, respectively.

We have therefore checked that through this method, all performance metrics of an LNA can be improved. To determine the measurement uncertainty correctly, a thorough study of the cryogenic noise measurement was conducted. These are the lowermost noise temperatures recorded for any silicon-based amplifiers operating across this frequency range to the best of the writers' knowledge.

The design of higher frequency SiGe cryogenic amplifiers, enhanced noise modeling of the first stage transistor, and tailored narrow band amplifiers for particular applications will be investigated in future work.

References

1. Alican Ça’ğlar, Student Member, IEEE, and Mustafa Berke Yelten, Senior Member, IEEE, “Design of Cryogenic LNAs for High Linearity in Space Applications”, in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS, Volume: 66, Issue: 12, Dec. 2019, Page(s): 4619 – 4627.
2. Andrew Janzen; Sander Weinreb, “Manufacturable cryogenic SiGe LNA for radio astronomy and space communications”, in 2016 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), IEEE, 2016.
3. HARALD HOMULLE, LIN SONG, EDOARDO CHARBON, and FABIO SEBASTIANO, “The Cryogenic Temperature Behavior of Bipolar, MOS, and DTMOS Transistors in Standard CMOS” in Journal of the electron devices society, Vol. 6, 2018, pp.: 263-270.
4. Mahesh Mudavath, K. Hari Kishore, Azham Hussain and C.S. Boopathi “ Design and analysis of CMOS RF receiver front-end of LNA for wireless applications,” *Microprocessors and Microsystems*, volume 75 (2020), pages:1-11, article no. 102999, doi: https://doi.org/10.1016/j.micpro.2020.102999.

5. Arnout Beckers, Farzan Jazaeri, and Christian Enz, Senior Member, IEEE, “Cryogenic MOS Transistor Model”, in *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 65, NO. 9, SEPTEMBER 2018, pp. 3617-3625.

6. Bishnu Patra, Rosario M. Incandela; Jeroen P. G. van Dijk; Harald A. R. Homulle; Lin Song; Mina Shahmohammadi; Rober., “Cryo-CMOS circuits and systems for quantum computing applications,” *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

7. B. Aja, E. Villa, L. de la Fuente, and E. Artal, “Cryogenic performance of a 3–14 GHZ bipolar SiGe low-noise amplifier,” *Cryogenics*, vol. 99, pp. 18–24, Apr. 2019.

8. S. Montazeri, W.-T. Wong, A. H. Coskun, and J. C. Bardin, “Ultra-lowpower cryogenic SiGe low-noise amplifiers: Theory and demonstration,” *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 178–187, Jan. 2016.

9. Mahesh Mudavath and K. HariKishore “Design and analysis of receiver front-end of CMOS cascode common source stage with inductive degeneration low noise amplifier on 65nm technology process,” *Journal of Computational and Theoretical Nanoscience (JCTN)*, Vol.16, No.5/6, page: 2628-2634, 2019, ISSN 1546-1955 (Print); ISSN 1546-1963 (Online).

10. M. Varonen, K. Cleary, D. Karaca, and K. A. I. Halonerr, “Cryogenic millimeter-wave CMOS low-noise amplifier,” in *IEEE MTT-S Int. Microw. Symp. Dig.*., Jun. 2018, pp. 1503–1506.

11. P. A. ’t Hart, J. P. G. van Dijk, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, “Characterization and model validation of mismatch in nanometer CMOS at cryogenic temperatures,” in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2018, pp. 246–249.

12. Kabao’glu, N. ,Sahin-Solmaz, S. Ilik, Y. Uzun, and M. B. Yelten, “Statistical MOSFET modeling methodology for cryogenic conditions,” *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 66–72, Jan. 2019.

13. R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, “Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures,” *IEEE J. Electron Devices Soc.*., vol. 6, pp. 996–1006, Apr. 2018.

14. Mahesh Mudavath and K. Hari Kishore “Differential CMOS low noise amplifier design for wireless receivers,” *International Journal of Recent Technology and Engineering (IJRTE)*, ISSN: 2277-3878, Volume-8, Issue-4, 2019, pp: 2467-2474.

15. H. Coskun and J. C. Bardin, “Cryogenic small-signal and noise performance of 32nm SOI CMOS,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.

16. X. Zhang et al., “Development of cryogenically-cooled low noise amplifier for mobile base station receivers,” *Chin. Sci. Bull.*, vol. 56, no. 35, pp. 3884–3887, Dec. 2011.

17. Mahesh Mudvath and K. Hari Kishore “A low NF, high gain of 2.4GHz differential LNA design for wireless applications,” *International Journal of Scientific & Technology Research (IJSTR)*, Volume-8, Issue-12, December-2019, pp: 109-116, ISSN: 2277-8616

18. J. Schleeh et al., “Cryogenic LNAs for SKA band 2 to 5,” in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 164–167.