ADIC: Anomaly Detection Integrated Circuit in 65nm CMOS utilizing Approximate Computing

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Abstract—In this paper, we present a low-power anomaly detection integrated circuit (ADIC) based on a one-class classifier (OCC) neural network. The ADIC achieves low-power operation through a combination of (a) careful choice of algorithm for online learning and (b) approximate computing techniques to lower average energy. In particular, online pseudoinverse update method (OPIUM) is used to train a randomized neural network for quick and resource efficient learning. An additional 42% energy saving can be achieved when a lighter version of OPIUM method is used for training with the same number of data samples lead to no significant compromise on the quality of inference.

Instead of a single classifier with large number of neurons, an ensemble of $K$ base learner approach is chosen to reduce learning memory by a factor of $K$. This also enables approximate computing by dynamically varying the neural network size based on anomaly detection. Fabricated in 65nm CMOS, the ADIC has $K = 7$ Base Learners (BL) with 32 neurons in each BL and dissipates 11.8$pJ/OP$ and 3.35$pJ/OP$ during learning and inference respectively at $V_{dd} = 0.75V$ when all 7 BLs are enabled. Further, evaluated on the NASA bearing dataset, approximately 80% of the chip can be shut down for 99% of the lifetime leading to an energy efficiency of 0.48$pJ/OP$, an 18.5 times reduction over full-precision computing running at $V_{dd} = 1.2V$ throughout the lifetime.

Index Terms—Anomaly Detection, Internet of Things, Edge computing, Predictive Maintenance, One Class Classification, Energy Savings, Approximate Computing.

I. INTRODUCTION

Anomaly detection is an important topic in the field of machine learning and deep learning, which focuses on the efficient detection of anomalous activity in a process. A typical data visualization of an anomaly (outlier) is presented in Fig. 1 for a two-dimensional ($2D$) data $(X, Y)$ [1]. This $2D$ data is easy to visualize and requires relatively simpler statistical analysis to identify the highlighted outlier. For high dimensional data beyond $2D$, it requires more sophisticated computations like Mahalanobis distance. Typically, there is no prior knowledge to characterize an anomaly, nor ample data is available in any of the practical fields that symbolize these outliers [2]. A few examples of anomaly detection are the detection of rare (unusual) events in real life scenarios such as medical complications depicted in ECG/EEG data abnormalities [3], [4], [5], malfunctioning of rotary machines due to various physical factors [6], [7], security threat in cyber-physical systems [8], [9], [10], [11] or even fraud detection in financial systems [12].

This paper focuses on finding anomalies in rotating machines, also known as machine health monitoring in Industry 4.0. In many industrial setups, rotating machines are of utmost importance in its functioning. Their failure can lead to a catastrophic impact such as loss of productivity and accidents leading to safety concerns of the working personnel. Therefore, maintenance of these machines becomes very critical, thus requiring constant human supervision or by automatic instrumentation. Periodic maintenance based on statistical models and reliability data [13] results in fewer breakdowns. However, this is not a cost-effective approach due to unacceptable wastage of the residual useful life of the healthy machines [14]. Contrarily, reactive maintenance comes into effect only when a machine fails leading to an unpredictable loss in productivity. Therefore, the industry is poised to move towards Predictive Maintenance (PdM) and is shown to be more effective in reducing the downtime of a machine and the overall cost of maintenance.

Machine learning (ML) based techniques in PdM such as aero-engine control system sensor fault detection [15], fault diagnostics of rotary machines [16] and machine health monitoring tasks [17] are a few examples of PdM which rely on detecting a trend of fault in a machine as an anomaly. Lack
of adequate failure data prohibits a multi-class classification based fault detection model [17]. Furthermore, the failure signatures vary drastically from one machine to another and hence is not practical to build a generic detection system using a generic set of data pertaining to a set of machines of the same category. Instead, each model needs to learn the parameters from the sensor data attached to the machine corresponding to it. In summary, this is a classic case of One-Class Classification (OCC), where a classifier is trained to learn similar data distribution. In this work, the proposed anomaly detector model learns from the healthy data and identifies the occurrence of signatures corresponding to the mechanical failures as the deviations from a healthy state of the machines [18].

In a large enterprise, a large number of sensors are interconnected through a network to a central server, typically over the Internet, and are commonly referred to as Internet-Of-Things (IoT). It involves a large amount of data transmission for subsequent processing over the network leading to significant power consumption and bandwidth requirement. This turns out to be a bottleneck in case of critical low latency remedial actions. Alternatively, the data processing engine is being pushed to the edge of the network, i.e., in the vicinity of the sensor modules, enabling the system to transmit the decision to the servers only, thus saving on energy consumption and reducing bandwidth requirement. In many IoT applications, the computing engines placed near the sensors need to be battery operated. This demands an edge computing device to be more energy efficient during its operation, thus elongating its operation lifetime [19]. Our study showed that no low power integrated circuit (IC) implementation of an edge computing device exists for anomaly detection.

This paper presents a novel energy-efficient machine learning co-processor referred to as Anomaly Detection Integrated Circuit (ADIC). This design implements a popular machine learning framework called Extreme Machine Learning (ELM) [20] used for shallow neural networks. The key differentiators of the proposed ASIC implementation from the microprocessor-based anomaly detector [21] are the followings:

1) Use of pseudo-random binary sequence (PRBS) based weight generation eliminating memory required for weights in the first stage of ELM.

2) Online learning using OPIUM [22] and OPIUM-Lite [23] learning rule (without matrix inverse) for individual devices to learn their own baseline condition.

In addition, ADIC also supports ensemble classifier architecture to implement approximate computing using ADEPOS algorithm [24].

In this paper, we start with a brief overview of a single hidden layer neural network model and one-class classification in Section II. This section also discusses the ELM framework and relevant online learning algorithms. Subsequently, we present the architecture and design details of the ADIC is followed by a discussion on ADEPOS scheme in Section III. Finally, section IV contains the experimental results, on-chip characterization as well as health prediction results on the NASA bearing dataset [25] followed by the concluding remarks in the last section.

II. BACKGROUND: ONE-CLASS CLASSIFICATION, ELM AND ADEPOS

A single layer feed-forward neural network, as depicted in Fig. 2(a), consists of input layer, \( x = [x_1, x_2, \ldots, x_d]^T \), output layer, \( \hat{x} = [\hat{x}_1, \hat{x}_2, \ldots, \hat{x}_m]^T \), and hidden layer, \( h = [h_1, h_2, \ldots, h_L]^T \). Here, \( d, m, \) and \( L \) denote the respective number of input, output and hidden neurons. This network is most commonly referred to as an Auto Encoder (AE) engine when \( m = d \). The AE network is trained to learn the input data distribution and reconstruct them at the output with minimal reconstruction error. While the hidden layer nodes encode an input vector \( x \) into a feature space \( h \) using the connection weights \( W \) and biases \( b = [b_1, b_2, \ldots, b_L]^T \), the output layer weights \( \beta \) between the hidden and output neurons are used to decode the feature space embedded in \( h \) aimed at reconstruction of the input features \( x \).

![Figure 2: A Single (Hidden) Layer Feed-forward Neural Network (SLFN): (a) input reconstruction to outputs and (b) output mapped to a single node](image)

Details of the encoding and decoding process of AE are mathematically given in Eq. (1) and (2), where \( g() \) refers to the neural activation function and \( h_j \) denotes the output of the \( j^{th} \) hidden neuron.

\[
h_j = g \left( \sum_{i=1}^{d} W_{ji} x_i + b_j \right); \quad j = 1, 2, \ldots, L
\]
\[ \hat{x}_k = \sum_{j=1}^{L} \beta_{jk} h_j; \quad k = 1, 2, \ldots, m \]  

(2)

Although the sigmoid function is typically chosen as the activation function, \( g(\cdot) \), Rectified Linear Unit (ReLU) has gained traction lately due to its effectiveness to solve the vanishing gradient problem and the ease of implementation on hardware.

### A. ELM based OCC

We define a list of symbols in the following that will be used throughout this subsection:

- \( W \) input layer weights
- \( \beta \) output layer weights
- \( X \) input layer activation of N samples
- \( H \) hidden layer activation of N samples
- \( x_i \) input layer activation at \( i^{th} \) input vector
- \( E_i \) reconstruction error at \( i^{th} \) input sample
- \( h_i \) hidden layer activation at \( i^{th} \) input sample
- \( \eta_i \) learning rate at \( i^{th} \) input sample
- \( K, \theta \) intermediate variables for calculation

A traditional autoencoder (T AE) requires a sufficiently large amount of data and computational resources in order to identify an optimal \( W \) and \( \beta \) values. The back-propagation (BP) method, although known to yield very accurate models, incurs high computational overhead due to its two-pass approach on each epoch. On the contrary, the training following the Extreme Learning Machine (ELM) framework is faster where input weights, \( W \), and biases, \( b \) are generated randomly from a continuous probability distribution \([20], [27]\). A Pseudo-random Binary Sequence Generator (PRBS) for a given seed is able to generate a set of random numbers of specified data width in hardware implementation. This simplifies the network optimization for optimal output weights \( \beta \).

In the batch learning approach \([20]\), finding the optimal values of \( \beta \) corresponding to least-square optimization requires to compute the hidden neuron outputs \( H = [h_1, h_2, \ldots, h_N] \) for a batch of \( N \) input data samples \( \bar{X} = [x_1, x_2, \ldots, x_N] \).

Since the output nodes (targets) are the same as training samples \( \bar{X} \) for a reconstruction based AE, the optimal output weight \( \beta^* \) is computed as shown below.

\[ \beta^* = H^T \bar{X} \]  

(3)

Notably, this equation reduces the task of parameter optimization for the entire AE network to a matrix inversion operation. Since these are non-square matrices, Moore-Penrose generalized inverse method \([28]\) is used to compute the pseudo-inverse \( H^T \) of \( H \).

Therefore, huge computational overhead, as well as large memory requirement, make this approach difficult to implement in hardware. In order to overcome these limitations, another version of ELM was proposed in \([29]\). Known as Online Sequential ELM (OSELM), this method outlines the learning of output weight matrix \( \beta \) based on a single data point \( x_i \) in every iteration until convergence is attained. This approach is found to be similar to the stochastic gradient descent method used in the back-propagation method since the output error due to a single input vector \( x_i \) is used to update the output weight matrix \( \beta^{(i-1)} \) to \( \beta^{(i)} \).

A set of equations describing this weight update process is presented in Eq. \([4] - [6]\), details of which can be found in \([29]\).

\[ K_i = K_{i-1} + H_i^T H_i \]  

(4)

\[ E_i = x_i - H_i \beta_{i-1} \]  

(5)

\[ \beta_{(i)} = \beta_{i-1} + K_i^{-1} H_i^T E_i \]  

(6)

Nevertheless, the OSELM approach requires heavy computational overhead due to matrix inversion operation for each weight update as shown in Eq. \([6]\). These equations are valid for small batch of samples, say \( N_i \ll N \), of \( X_i = x_1, x_2, \ldots, x_{N_i} \), including \( N_i = 1 \) which refers to a single input sample \( x_i \).

Recently, a simpler online weight update method was proposed in \([22], [23]\) which relies on the sequential update of the output weights using only one input sample \( x_i \). This method is referred to as Online Pseudo-Inverse Update Method (OPIUM). The set of equations that describe the OPIUM method are presented in Eq. \([7] - [9]\). A close look at these equations reveal that (a) no matrix inversion is needed, and (b) weight update depends only on matrix multiplication. The matrix product \( h_i^T \theta_{i-1} h_i \) in Eq. \([7]\) turns out to be a scalar entity, and hence eliminate the need for matrix inversion. Thus, all matrix multiplication operations can be realized in hardware using Multiply-and-Accumulate (MAC) approach, which is a fundamental building block used in machine learning-based hardware designs.

\[ \eta_i = \frac{\theta_{i-1} h_i}{1 + h_i^T \theta_{i-1} h_i} \]  

(7)

\[ \beta_i = \beta_{i-1} + \eta_i (x_i - \beta_{i-1} h_i) \]  

(8)

\[ \theta_i = \theta_{i-1} - \eta_i \beta_{i-1} h_i \]  

(9)

This indicates that the usage of the ELM framework with the OPIUM learning algorithm is suitable for efficient hardware implementation of a single hidden layer feed-forward neural (SLFN) network. The combination of these methods reduces both computational overhead and energy consumption during training, without sacrificing on the quality of the trained model \( \beta^* \) after convergence. The computational complexity of the OSELM method is estimated to be \( O(L^3) \), while that of OPIUM is \( O(L^2) \) for a network with \( L \) hidden nodes. Moreover, OSELM versions require 3X higher memory space due to matrix inverse operation using the LU decomposition method.

To further reduce the computational complexity, the network in Fig \([2a]\) can be transformed to the one in Fig \([2b]\) having only one output node \((m = 1)\) \([26]\). We refer to the network modes in Fig \([2 a]\) as reconstruction mode and Fig \([2 b]\) as boundary mode. In this paper, we subsequently denote them as ELM-AE and ELM-B respectively. Unlike in ELM-AE, the
single output node in ELM-B is set with any constant target value, e.g., \( x_1 = 1 \), such that the output weight \( (\beta^*) \) is obtained after the training is expected to reconstruct a value of (or near to) 1 at the output node \( 26 \) for any \( x_i \) that represents a healthy data. A faulty data \( x_j \) exhibits a significant deviation from the reference value of 1 depending on the quality of training of the output weight, i.e., the trained value \( \beta^* \). The number of samples required for a good \( \beta^* \) to converge depends on the network structure, i.e., whether ELM-AE or ELM-B. A comprehensive study on training convergence for different AE models has been summarized in [24].

B. Ensemble Learning

In Fig. 3 we illustrate an ensemble of \( K \) ELM based OCC engines, henceforth termed as a Base Learner (BL) engine. Each BL engine is designed to be trained with the same set of input data \( x_j \). However, the characteristic of each BL differs due to different seed values used in the PRBS module. This facilitates different distribution of input layer weights \( W \) and biases \( b \) and thus yields different trained \( \beta \) values for each BL. Therefore, the performance of each BL during inference is expected to be different. This ensemble architecture can have a configurable number of active BLs (up to a maximum \( K \) BLs) during inference while the rest remain inactive depending on the application. The output from each active BL engine can be used to generate the final output by several ensemble methods such as majority voting scheme. In the case of majority voting, an odd number of active BLs is required in order to avoid tied voting. Other than majority voting, this design can also support other ensemble applications such as AdaBoost method [30], [31] in order to enhance system performance. However, this exercise is beyond the scope of this paper and considered to be addressed in our future works.

C. The ADEPOS algorithm

Now, we briefly discuss the ADEPOS algorithm [24] for energy-saving suitable for the proposed OCC engine ADIC. During early life, a machine presumably remains to be healthy and unlikely to show any fault due to wear and tear. During this healthy period, the output of the OCC-engine will not flag error indicating any failure in the machine. Thus the detection of an anomaly at this stage is rare unless caused by unexpected failures of the machine or even spurious signals coming from the sensor module. This fact is utilized by the ADEPOS algorithm which is based on the hypothesis that we can employ inaccurate computing at this stage of early inference. Errors due to this approximation can be overcome by careful inspection of the fault and its trend of crossing the threshold. The pseudocode in Algorithm 1 outlines the ADEPOS algorithm, showing only the variation in the number of active BLs.

The effective number of hidden neurons in the proposed ensemble framework, \( L_k \), is given by:

\[
L_k = K \times L
\]

where \( K \) is the number of base learners (BL) in the ensemble network.

From the hardware viewpoint, the training of a larger neural network of \( K \times L \) hidden neurons requires a large memory of the size of \( K^2 \times L^2 \) for storing \( \theta \) (Eq. 9), whereas an ensemble of \( K \) BLs with \( L \) neurons require only \( K \times L^2 \) memory. This saves memory area by a factor of \( K \).

III. ADIC HARDWARE ARCHITECTURE

Here, we discuss the proposed hardware architecture of ADIC and its implementation that supports online learning (via OPIUM) and approximate computing (via ADEPOS). Fig. 4 depicts an overview of the architecture for the proposed ELM based OCC engine, alternatively called BL engine in the ensemble discussed in the previous section. Each BL consists of a PRBS module, a TDM (time division multiplexing) hidden and output neuron, and an online learning module. As discussed in the previous section, the training of \( \beta \) values in each BL is done with different seed values for the corresponding PRBS module in it. This pseudo-random generator module generates a maximum 16-bit random number for the input weights \( W = \{ w_{ij} | i \in \{1, d\}, and, j \in \{1, L\} \} \) and biases \( b = \{ b_j | j \in \{1, L\} \} \) within the dynamic range of \(-2^{15}\) to \(2^{15} - 1\). The implementation of the PRBS module eliminates the need to store the input weights and biases and the need to obtain their trained values as in the case of back-propagation based methods. Thus, the memory requirement to hold the
trained parameters for this network is reduced by \( \approx 50\% \). Additionally, this approach reduces the training overhead for \{W; b\}. Power analysis using a post-layout extracted netlist in INNOVOS shows that the combined logic of PRBS and MAC in hidden layer computation consumes 3.5X less power over the MAC and the memory cells used to store the input weights \( W \) and biases \( b \). Moreover, we achieve an area reduction of 80\% in the hidden layer by implementing PRBS. This eliminates the need to store the random weights and biases \{W, b\} for the first stage of ELM based SLFN network only.

The proposed ADIC implements the online learning framework OPIUM \[22\] in order to reduce the computational overhead per input sample, \( x = \{ x_i | i \in \{ 1: d \} \} \), yielding 3X reduction in memory requirement over OSELMM method. This reduces the total power consumption due to the inverse calculation required in the OSELMM method. In this design, we adopted a single physical neuron that works in time-division-multiplexing (TDM) fashion for both the 1\textsuperscript{st} and 2\textsuperscript{nd} layers of the ELM as depicted in Fig. 4. This approach emulates the scenario of \( L \) physical hidden nodes and also \( m \) output neurons, by suitable configuration of \( L \) and \( m \). This approach not only reduces the requirement for large area requirement for logic and memory but also reduces the power consumption due to the number of computes depending on the value of these parameters. In the design, \( L \) can vary in the range of \( 1 - 32 \) while \( m \) can vary in the range of \( 1 - d \) with a maximum value of \( d = 16 \). As a result, this architecture also provides the required flexibility to configure the ADIC as a boundary based ELM engine for one class classification by programming the number of output neurons \( m = 1 \) and \( x_1 = 1 \). This enables trading off the higher processing time required for reconstruction mode with the quality of inference in boundary mode. As mentioned earlier, the number of output neurons \( m \) for reconstruction mode remains the same as the number of input neurons \( d \). With these parameters, including the number of hidden nodes \( L \), the entire network can be made configurable. These configurable parameters also dictate the PRBS module to accordingly generate the required number of input weights \( W \) and biases \( b \), having the respective dimensions of \( L \times d \) and \( L \times 1 \).
This design has configurable datapath ranging from 8 to 16 bits in steps of 4 bits, while the number of input (d) and output neurons (m) can also be varied from 1 to 16. Moreover, the number of hidden nodes L is made configurable and go up to 32 in each base learner (BL) module. In order to reduce the area and the leakage power due to SRAM cells, we restrict the maximum datapath width to 16bit (signed integer) for encoding W, b, β as well as the input data x_i. Additionally, we provide another level of bit precision control by independently controlling the bit width of the random numbers generated by the PRBS module for W and b, and can range from 2 bits to a maximum of 8 bits in steps of 2 bits. It is important to note that these bit-precision control approaches apply to inference mode only, while the training is always done with the highest allowable precision of 16 bits. This ensures that the training phase gets the highest accuracy of computations.

In addition to that, a method to reduce power consumption during training by reducing computational overhead during training was proposed in [23] as a Lite version of OPIUM. This method is commonly referred to as OPIUM-Lite. As discussed in [23], we introduce a provision to prohibit the update of θ variable and initialize it with a configurable value, in order to realize the OPIUM-Lite version. The corresponding SRAM module in each BL that stores θ values and the logic around it are completely turned off by clock-gating. This technique, by prohibiting the read/write access, reduces the dynamic power significantly as it is the largest memory cell used and has almost double the combined size of all other SRAM cells used in each BL.

Figure 5 presents a timing diagram of the dataflow of on-chip calculation during the training and testing of a BL. ADIC follows Eqs. (1)-(2) for hidden and output neurons calculation and Eq. (7)-(9) for parameter updates during online training. For illustration, we show the update of all the elements (h_j/x_m/β) of each parameter in every clock cycle. However, the calculation of each element takes several clock cycles except the input (X) dataflow. Even though all the parameters are 16-bit precision, calculations of the partial sum are done in higher bit precision to avoid overflow. For instance, we use 32-bit for the calculation of ACC in hidden and output neurons (Fig. 4). However, based on the 2-bit configuration, we choose intermediate 16-bit of final ACC calculation, such as ACC[27:12] for hidden and output neurons (H and X).

In Fig. 6, we present Matlab simulation results for commonly used machine health monitoring dataset [25], using both OPIUM and OPIUM-Lite training for the same number of samples. This dataset exhibits a healthy initial part and therefore is used for training. While most of the remaining data points represent a healthy state, data points beyond 1600 tend to show increasing fault levels due to higher vibration levels. The results show that OPIUM-Lite takes relatively less number of input samples (x_i) to converge than OPIUM method, as depicted in Fig. 6 (a) and (b) for OPIUM and OPIUM-Lite respectively. Notably, the norm of β appears to be noisier in the case of OPIUM-Lite than OPIUM even towards the end of the training. Likewise, the inference response of OPIUM-Lite based training (6(d)) appears to be noisier than OPIUM method (6(c)), specially during the period of good health. However, this does not adversely affect the performance due to two reasons: first, the threshold in case of OPIUM-Lite is proportionately increased (red line in 6(c) & (d)) and second, the relative change in test error on encountering an actual anomaly is still much larger than the baseline and crosses the threshold at the same sample index. We calculate the test error as ∥x − x̂∥, where x and x̂ denote the input and reconstructed output vectors respectively. In ADIC, there is a provision of choosing between OPIUM and OPIUM-Lite methods depending on the application and thus exploits the energy-saving capabilities of OPIUM-Lite due to the lesser number of samples used for training, without any significant compromise on fault detection. The prohibition to update θ in OPIUM-Lite also incurs significant energy savings. Relevant experimental results are presented in Section IV.

IV. RESULTS

In this section, we first present results of the characterization of the ADIC in terms of operational power supply range, clock
frequency and power dissipation. Later, we present results of applying ADIC to a predictive maintenance task to determine health condition of bearings.

Figure 7: Experimental Setup: (a) fabricated device ADIC, and (b) the test infrastructure

A. Characterization of ADIC

Figure 7 shows the packaged chip for ADIC, and the test setup for online learning and machine health monitoring. Even though in this setup, an FPGA board sends the extracted features to ADIC for ease of testing, other low power microcontrollers can be employed to transfer the data as well to reduce system power in deployed solutions. We vary the $V_{dd}$ of ADIC from 0.75V to 1.2V, while the input clock frequency is varied from 10MHz to 50MHz. The current implementation of ADIC supports 16-bit data, as well as up to 14-bit address bus and the control signals for read/write operations. In the next two subsections we will discuss the characterization of ADIC with respect to supply voltage, frequency and number of active BLs.

1) Dynamic Voltage and Frequency Scaling (DVFS): We present the power consumption of ADIC across different supply voltages as well as frequencies in Fig. 8(a)-(b). These results are presented for both training and inference phases of ADIC for the maximum number of active BLs ($K=7$) in the system. It can be seen from the figures that the device is functional to a minimum $V_{dd}$ of 0.75V although 1.2V is the nominal supply voltage. For both training and inference mode, the trend clearly shows that we have power saving of (a) 3X when $V_{dd}$ is reduced from 1.2V to 0.75V at 20MHz, and (b) 2.5X when $V_{dd}$ is reduced from 1.2V to 0.75V at 10MHz. Also, it can be seen that the minimum required supply voltage for clock frequencies above 40MHz turns out to be $V_{dd} = 0.9V$.

The previous plots show reduction of both power and throughput by DVFS. Next, figure 9 presents the inference energy per operation of ADIC for the DVFS data presented earlier. ADIC takes $\approx 1000$ clock cycles to generate an output decision for a single BL in the inference phase. This includes the cycles needed to transfer the data from the input layer to the output layer. Evidently, a trade-off exists between energy consumption and the throughput of the system. ADIC can achieve a maximum of 10K classifications per second at the cost of 3.35pJ/OP at 10MHz and 0.75V. On the contrary, for the ADIC to cater a higher throughput of say 50K classifications per second, the clock frequency is required to be increased to 50MHz leading to the corresponding increase in energy from 4.83pJ/OP at 0.9V to 8.28pJ/OP at 1.2V. As an application (PdM) point of view, we can operate the system at the lowest frequency possible due to the lower data rate. However, a faster classification rate is preferable since this also implies lesser time to classify one sample and more time to be spent in low-energy sleep mode.

Hence, depending on the applications that demand higher classification throughput, the ADIC can be run at the most favorable $V_{dd}$ and clock frequency for the best energy per operation value. It is noticeable from the plots in Fig. 9 that the energy efficiency of ADIC decreases with higher $V_{dd}$. However, these variations are practically insignificant with respect to the variation in clock frequency running at the same $V_{dd}$ value. This is due to the fact the dynamic power consumption ($\propto CV_{dd}^2f_{clk}$) in ADIC is the most dominant component in total power consumption while the static power (which gets amortized with higher clock frequency) is negligible. For example, these plots show a marginal variation in pJ/OP with respect to clock frequency at $V_{dd} = 1.2V$ and get flatter as the $V_{dd}$ is reduced to a lower working value. This is attributed to the further decrease in static power with the corresponding decrease in $V_{dd}$.

Figure 8: Power ($mW$) vs Supply voltage $V_{dd}$ (V) at different clock frequencies (10-50MHz) and $K = 7$: (a) Training, and (b) Inference.

As it is also depicted in Fig. 8, the minimum supply voltage $V_{dd}$ required to run at a given clock frequency varies in order
to ensure that the timing of the most critical paths in the design are not violated. For example, $V_{dd} = 0.75\text{V}$ can handle an operating frequency up to $20\text{MHz}$, while $V_{dd} = 0.9\text{V}$ is required for running the design for a higher clock frequency of $30 - 50\text{MHz}$.

2) Power consumption Vs # active BLs: Figure 10 presents the mean detection accuracy and false positive rate of ADIC across a different number of hidden neurons in the network using the NASA bearing dataset. As long as the accuracy of each BL (weak learner) is higher than the random guess (50%), we can build a stronger model by an ensemble of multiple weak models. Therefore, even though the mean detection accuracy of each BL is 95% due to its simple architecture, we achieved 100% detection accuracy by an ensemble of 7 BLs. Moreover, since we are getting 100% detection accuracy deploying the single hidden layer network in conjunction with the ADEPOS algorithm, we did not increase the depth of our architecture beyond two layers.

As discussed in Section III the existing ADEPOS algorithm achieves energy savings by varying the number of active BLs ($K$) during the inference phase. The results in Fig. 11 (b) show how the variation in $K$ can be beneficial in reducing the power consumption during the inference phase when the machine is in good condition and the classification can be done with majority voting among a fewer number of active BLs. During the early life of a machine, $K$ can be as low as 1 yet giving acceptable results showing good health of the machine. However, as the ADEPOS algorithm dictates, on detection of any error by the current active BLs, $K$ can be increased to monitor the recurrence of the error on the same data. This process continues while increasing the current $K$ to the next allowable value if the error persists. If $K$ reaches the maximum value of 7 (supported in this implementation) and error is detected on the same input data sample from the sensors, then the machine is identified as a faulty one. It can be seen that a 1.8X reduction in power consumption is possible when running with $K = 1$ compared to $K = 7$ at $V_{dd} = 1.2\text{V}$. Moreover, this algorithmic power reduction is invariant of supply and operating frequency of ADIC.

Since the ADEPOS algorithm demands that all the BLs should be trained so that they are ready for the inference phase, we also plot the power requirement of a different number of BLs during the training phase in Fig. 11 (a). In general, we expect that the energy consumption overhead for training is much less as compared to the inference energy. This is due to the fact that the training is done with a relatively smaller (limited) number of input samples at the beginning of deployment, while the inference can go as long as the energy source to the device is not depleted or until the fault is detected in the machine.

B. Energy Saving in Inference: ADEPOS

Figure 12 summarizes a comparative study among ADIC with all 7 BLs that are turned on for full precision computing throughout the lifetime of a machine at different supply voltages and a case when the ADEPOS algorithm is run on ADIC at lower supply voltage. It has been observed that when the ADEPOS algorithm runs on ADIC, it keeps 80% of the chip in inactive mode (clock gated) for $\approx 99\%$ of the lifetime based on testing with the NASA bearing dataset. This yields an energy efficiency of $0.48pJ/\text{OP}$, an $18.5X$ and $6.96X$ reduction over the full-precision compute by ADIC at $1.2\text{V}$ and $0.75\text{V}$ with all 7 BLs turned on respectively. Of course, the savings obtained are entirely data dependent.

In a generic case, we can calculate the effective energy efficiency for ADIC over the entire lifetime of a machine data as:

$$E_{total} = \sum_{i} \alpha_i E(N_i) \quad s.t. \quad N_i \in \{1, 3, \cdots K\}$$

Here, $E(N_i)$ denotes the energy dissipated by ADIC when $N_i$ BLs are active at any point of time and $\alpha_i$ denotes the fraction of the total lifetime during which $N_i$ BLs are active. When ADIC is running with full accuracy (i.e. without ADEPOS), $\alpha_i = 1$ for $N_i = K$ and the rest of the $\alpha_i$s are zero. However, for energy savings according to the ADEPOS algorithm, $\alpha_i$ has the largest value when $N_i = 1$ and has significantly
decaying value with the increasing number of active BLs \( (N_i = 3, 5, \cdots K) \) in case when \( ADIC \) starts to flag a fault.

When ADEPOS runs on \( ADIC \) during the healthy state of a machine, it performs with similar accuracy as \( ADIC \) without ADEPOS running on it and thus effectively saves the number of computes. In order to compute the energy efficiency for ADEPOS, we divide the total energy dissipated \( E_{total} \) by the same number of computes required by \( ADIC \) operating with \( K \) active BLs for the same accuracy computation throughout its lifetime. As mentioned earlier, the current implementation of \( ADIC \) has a maximum number of BLs \( K \) as 7. Hence, the ADEPOS algorithm can potentially achieve a maximum 7X improvement in energy saving in case of no-fault detection when only one BL is active.

\section*{C. Energy Saving in Training: OPIUM-Lite}

The results presented in Fig. 12 shows the power consumption during the online training phase of \( ADIC \) leveraging OPIUM and OPIUM-Lite online learning algorithm respectively. We obtain the results for \( K = 7 \), at 10MHz clock frequency while the supply voltage \( V_{dd} \) is varied from 0.75V to 1.2V. We achieve an average of 42.8\% training energy savings when OPIUM-Lite mode is used over OPIUM.

As discussed in the previous section, this power saving is a cumulative effect due to the fact that OPIUM-Lite mode turns off the update mechanism for \( \theta \) parameters in the respective memory of each BL, thus saving the dynamic power consumed by the respective memories. The energy efficiency computed for the OPIUM mode is 11.87\( pJ/OP \), while OPIUM-Lite exhibits a better energy efficiency of 8.12\( pJ/OP \) at 0.75V and 10MHz. The plot in Fig. 13 summarizes that OPIUM-Lite running at 0.75V mode can achieve a maximum 3.6X energy efficiency with respect to OPIUM operating at 1.2V supply.

\section*{D. Performance Evaluation in PdM}

In order to validate the online learning of \( ADIC \) in machine health monitoring applications, we opt for the widely used NASA bearing dataset provided by the Center for Intelligent Maintenance Systems (IMS), University of Cincinnati [25].

The dataset consists of 12 time-series run to failure bearing data and 4 of them have been failed at the end of their life. The vibration data of the bearings are sampled at 20KHz for 1s duration at an interval of 10 minutes. In order to reduce the amount of data seen by \( ADIC \), we extract statistical time-domain features such as (a) RMS, (b) Kurtosis, (c) Peak-Peak, (d) Crest factor, and (e) Skewness for each 20K data samples which are shown to be useful for bearing health monitoring [32]. Although frequency-domain features are also used for machine health monitoring in the industries to a great extent [33], but are expensive in terms of the number of computes. Due to space limitation, we confined ourselves to showcase the time-series response of \( ADIC \) on one dataset that exhibits a failure trend towards the end of its lifetime. Similar responses were obtained for all the other failing dataset, while the responses for all non-failing dataset do not show any failure.

As per the description of the NASA bearing dataset, there is no specific information regarding the time instance at which failures start to occur, except the success/failure label provided.
for each dataset. Hence, we determine a threshold \(<\text{Thr}\>) that draws a boundary between the response indicating good health of a machine under consideration and that of a fault. Here, we assume that the machine remains healthy during its early life and degrades only after a significant lifespan. Hence, initial data from the machine are used to train the BLs.

1) Threshold Selection: In order to estimate a threshold value \(<\text{Thr}\>\), we leverage a leave-one-out strategy (leave 1 out of 12 bearing dataset for testing, while the rest are used for training). In this method, the reconstruction errors (the difference between the expected and actual output of \textit{ADIC}), \(e\), for all 11 training bearings data are calculated as follows:

\[
e = \|x - \hat{x}\|
\]  

where \(x\) and \(\hat{x}\) denote the input and reconstructed output vectors respectively. Following this, the threshold \(<\text{Thr}\>\) is calculated according to Eq. \((13)\):

\[
\text{Thr} = \mu_e + 0.1 \times k \times \sigma_e
\]  

where \(\mu_e\) and \(\sigma_e\) denote the mean and standard deviation of the reconstructed errors respectively. The calculated \(<\text{Thr}\>\) is then used to test the remaining (left out) bearing data, in order to observe the response being a true fault or not. We iterate this approach for each of 12 bearing data to complete the cross-validation.

For a good estimate of \(k\) used in Eq. \((13)\), the values of \(k\) are swept from 10 to 100 and both false positives (FP) and false negatives (FN) are observed. In this work, we define true positive (TP) as good health and true negative (TN) for fault. The results of this exercise are presented in Fig. \((15)\) and it shows the optimum value of \(<k>\) lies between 40 to 60. We choose the optimum value as 50 which guarantees that no faulty state of a machine is classified as a healthy state (\(FP = 0\)) and a good machine is flagged as a faulty machine (\(FN = 0\)). Although the latter is not a critical situation, it may lead to over-maintenance of the machine.

2) Time Series Response: Figure \((16)\) presents a set of reconstructed error responses of \textit{ADIC} for the time-series data pertaining to a faulty machine given in the NASA bearing dataset. The responses for both OPIUM and OPIUM-Lite modes are obtained at 0.75\(V\) and 10\(MHz\). The x-axis in the figure represents the sample count of the data, while the y-axis represents the reconstruction errors from \textit{ADIC}. The threshold \(<\text{Thr}\>\) is plotted in red color in each of these plots and represents the classification boundary for anomaly detection. It can be seen that the response for the vibration data pertaining to the faulty machine is crossing the threshold line approximately around the sample count of 1700, while the response for a good machine never crosses the threshold.

It is to be noted that both the modes used the healthy data prevailing during the early stage of the machine’s life, similar to the sub-threshold error response for the first few hundred data samples in these plots. We also note that these responses are quite similar to our Matlab simulation results presented in Fig. \((6)\) for the same dataset. The test error crosses the threshold near the end of the life of bearing data. The plots are slightly different due to a) Fig. \((6)\) is plotted in semi-log scale b) data is scaled and converted to 7-bit signed integer format for the processing in \textit{ADIC}.

E. Comparison with Existing Works

In Table \([1]\) we present a comparative study of this work, with and without ADEPOS, and other recent published neural network integrated circuits \([34]\), \([35]\), \([36]\), \([37]\), \([38]\), \([39]\). The proposed \textit{ADIC} implements an ensemble of two layer fully connected (FC) network that is most similar to \([39]\). \([36]\) while most other works have implemented convolutional networks (CNN). Moreover, we exploit the random weights in our first layer to replace weight memory with a PRBS generator. Additionally, most of these works depend on offline learning while the proposed \textit{ADIC} implements online learning. The energy efficiency in our approach comes from usage of approximate computing at several layers while using a standard digital flow that does not rely on special memory macros for in-memory computing. It can be seen that energy efficiency of our proposed approach is competitive with respect to these recent published results. Furthermore, we compare \textit{ADIC} with the microprocessor-based anomaly detector \([21]\). The performance of \textit{ADIC} is an order of magnitude better in terms of energy efficiency.

V. Conclusion

In this paper, we present an anomaly detection integrated circuit (\textit{ADIC}), a machine learning co-processor based on extreme learning machines (ELM) algorithmic framework. \textit{ADIC} consists of an ensemble of one-class classification (OCC) engines for anomaly detection in machine health monitoring, using majority voting. This design implements an online pseudo-inverse update method (OPIUM), learning from in-situ data coming from the sensor nodes attached to the machines under health monitoring and is fabricated using 65nm CMOS process. \textit{ADIC} enables \(3.6\) times energy savings during training by using a combination of an approximate training algorithm (OPIUM Lite) and DVFS. During inference, it can save \(18.8\) times energy over a baseline model exploiting approximate computing algorithm ADEPOS combined with DVFS. The experiments are performed with the NASA bearing dataset, popularly used for evaluating predictive maintenance algorithms; however, the presented \textit{ADIC} can be used for other anomaly detection algorithms as well.
ACKNOWLEDGMENT
This work was conducted within the Delta-NTU Corporate Lab for Cyber-Physical Systems with funding support from Delta Electronics Inc. and the National Research Foundation (NRF) Singapore under Corp-Lab@University Scheme.

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Table I: Comparing ADIC (with ADEPOS) with some existing ML Co-Processors

| Parameters | This work (ADIC) | Existing Works |
|-----------|-----------------|----------------|
| Network Type | 38nm | Conv-DNN | 0.75 | SVM | 28nm |
| Technology | SLFN | Conv-DNN | 148 | Conv-DNN | 1152 |
| Training Method | Offline | Offline | 0.900 | Offline | Offline |
| Error Output | 0.298 | 38nm | 1.1 | 65nm | 0.82 |
| Data Samples | 10 | 38nm | 1.1 | 65nm | 1.0 |
| Energy Efficiency (TOPS/W) | 0.298 | 38nm | 1.1 | 65nm | 1.0 |

Figure 16: Reconstruction error of ADIC for a faulty machine from NASA bearing dataset: (a) OPIUM at 0.75V, (b) OPIUM-Lite at 0.75V demonstrating both algorithms are successful in detecting fault at approximately the same time.
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