Compact Continuous Time Common-Mode Feedback Circuit for Low-Power, Area-Constrained Neural Recording Amplifiers

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Abstract: A continuous-time common-mode feedback (CMFB) circuit for low-power, area-constrained neural recording amplifiers is proposed. The proposed CMFB circuit is compact; it can be realized by simply replacing passive components with transistors in a low-noise folded cascode operational transconductance amplifier (FC-OTA) that is one of the most widely adopted OTAs for neural recording amplifiers. The proposed CMFB also consumes no additional power, i.e., no separate CMFB amplifier is required, thus, it fits well to low-power, area-constrained multichannel neural recording amplifiers. The proposed CMFB is analyzed in the implementation of a fully differential AC-coupled neural recording amplifier and compared with that of an identical neural recording amplifier using a conventional differential difference amplifier-based CMFB in 0.18 μm CMOS technology post-layout simulations. The AC-coupled neural recording amplifier with the proposed CMFB occupies ~37% less area and consumes ~11% smaller power, providing 2.67× larger output common mode (CM) range without CM bandwidth sacrifice in the comparison.

Keywords: common-mode feedback; folded-cascode operational transconductance amplifier; multichannel neural recordings

1. Introduction

Multichannel neural recording in vivo is an essential electrophysiology tool to understand brain activities [1,2]. To simultaneously record complex activities from multiple neurons in a designated small brain area, multichannel recording amplifiers must be integrated with area- and energy-efficient manners [3–5]. For the last decades, integrated circuit design techniques for multichannel neural recording amplifiers to reduce power and area consumptions have been significantly progressed, resulting in ultralow power consumption (a few μW to sub-μW power consumption per channel) and high-density integration (>1000 channels in a few mm² silicon areas).

In neural recording amplifiers, an operational transconductance amplifier (OTA) is a key building block. Except for a few demonstrations where neural signals are directly sampled in a variable MOS capacitor (a parametric amplifier) [6] or an on-chip passive capacitor to get passive voltage gain [7], most neural recording amplifiers require OTAs in their implementation [8–16]. In particular, an AC-coupled closed-loop amplifier that is one of the most widely used neural recording amplifiers must have a high-performance OTA inside because it mainly determines the overall performance necessary for neural recordings, such as low input-referred noise (IRN), large bandwidth, low power, and small area consumptions, acceptable input/output signal ranges, and low distortion. Recent state-of-the-art neural recording amplifiers have been extensively explored by adopting various OTA topologies, such as a current mirror [8], two-stage [4,5,16–18], and folded cascode (FC) OTAs [9,19–21], in addition to the novel circuit design techniques [13,20–23]. Among the aforementioned OTA topologies, the FC-OTA has demonstrated that it reached...
the theoretical noise efficiency factor (NEF) limit of roughly 2 (~2.67), without adding the special circuit design techniques such as pre-amplification, current-reuse, and body biasing, and with the simple adaptation of large current scaling ratio and source degeneration [9].

Fully differential operation of neural recording amplifiers exhibits superior performance to single-ended ones, particularly when the supply voltage is reduced to achieve low-power operations. It provides large output voltage excursion even with high gain and low supply voltage (those are common in neural recordings), as well as immunity for common-mode (CM) interference such as power line noise (50/60 Hz) and removal of even-order harmonics. However, to realize the fully differential operation in amplifiers, a dedicated common-mode feedback (CMFB) circuit to set a proper output bias voltage should be incorporated. Especially, for low-power neural recording amplifier implementations where some transistors reside in the subthreshold region to maximize transconductance efficiency ($g_m/I_d$), a CMFB circuit with decent performance is highly required to make sure that all transistors stay in the saturation region because the operating points of transistors are not far away from the linear region, resulting in performance degradation by small deviations from the desired values.

Since a CMFB circuit usually consists of a common-mode sensor and an OTA for feedback, it results in additional power and area consumption and it becomes an implementation overhead for multichannel neural recording amplifiers. Figure 1 shows one instantiation of a fully differential FC-OTA for neural recordings, where a conventional differential difference amplifier (DDA)-based CMFB is employed. As shown, a fully differential operation in an FC-OTA requires two additional differential pairs (MC1–4) and load transistors (MC6–7), which consume more power ($2I_{BIAS}$) and area as compared with a single-ended version. Careful design consideration for stability is also required when employing the CMFB OTA otherwise, differential operation exhibits instability.

In this work, a compact CMFB circuit that does not require an additional OTA is presented. It simply reuses the source degeneration resistors used in the conventional low-power, low-noise FC-OTA for neural recordings to realize a CMFB function, and therefore does not need additional power and area consumption. The operation mechanism of the proposed CMFB is generic, in other words, it can be applied for any OTAs that have a CMFB control knob in their tail (or head) current sources. All performance of the proposed work is fairly compared with a conventional DDA-based CMFB in the implementation of an AC-coupled neural recording amplifier based on the same FC-OTAs. According to our analysis, a designed OTA with the proposed CMFB saves 37% area and achieves 11% power consumption reduction as compared with the circuit in Figure 1 and shows 34% fewer process variations and $2.67 \times$ wider output CM range.

Figure 1. A folded cascode operational transconductance amplifier (FC-OTA) for neural recordings with a conventional differential-difference amplifier-based common-mode feedback (CMFB).
2. Proposed CMFB Scheme

The proposed CMFB with the same FC-OTA in Figure 1 is depicted in Figure 2a. The bias network, except for the essential part for the explanations, is not shown for simplicity. For the output CM regulation, the proposed circuit shares the same operating principle as the circuit in Figure 2b where $M_{C1}$ and $M_{C2}$ operating in the triode region increase or decrease output current to adjust the CM output. As shown in Figure 2a, the only difference is that the sources of $M_5$ and $M_6$ are not physically connected, unlike the node $x$ in Figure 2b, but virtually shorted by connecting the positive ($V_{outp}$) and negative ($V_{outn}$) outputs via $M_{R1}$ and $M_{R2}$ ($M_{R3}$ and $M_{R4}$). Therefore, $M_{R1}$ and $M_{R2}$ ($M_{R3}$ and $M_{R4}$) can function as both a CM sensor and an input transconductor for CM regulation ($V_x \approx V_y$ for CM signals). This physical separation opens up the possibility to use $M_{R1}$–$M_{R4}$ for noise reduction in $M_5$ and $M_{Io}$, like $R_s$ in Figure 1. $R_s$ in Figure 1 provide a source degeneration of $M_5$ and $M_6$ (by series-series feedback), enabling a reduction of effective transconductance seen in the drain of them [9]. The part of the source degeneration circuit is redrawn in Figure 2c. The power spectral density of channel current noise of $M_5$ without $R_s$ is $4kT\gamma m_{5s}$ and it is proportional to the transconductance, $g_{m5}$. By degenerating the source terminal of $M_5$ with $R_s$, as shown in Figure 2c, the effective transconductance, $G_{m5,eff}$, becomes:

$$G_{m5,eff} = \frac{g_{m5}}{1 + (g_{m5} + g_{ds5})R_s},$$  \hspace{1cm} (1)

where $g_{ds5}$ is the drain to source conductance of $M_5$ and the body effect is ignored. If selecting values of $g_{m5}$ and $R_s$ properly to satisfy $g_{m5}R_s >> 1$ and assuming $g_{ds5} << g_{m5}$, $G_{m5,eff}$ reduces into:

$$G_{m5,eff} \approx \frac{1}{R_s},$$  \hspace{1cm} (2)

The channel noise of $M_5$ with $R_s$ is, therefore, modified and becomes $4kT\gamma m_{5s}$ (scaled by a factor of $\sim 1/g_{m3}R_s$), contributing to the noise reduction in the FC-OTA (recall that $1/R_s << g_{m5}$). Besides, $1/f$ noise at the gate of $M_5$: $K/[C_{ox}(W/L)]f$ ($K$, a process dependent parameter for $1/f$ noise and $C_{ox}$, oxide capacitance) is similarly attenuated when being reflected in the drain current. In the simulation, the IRN reduction by $R_s$ is $\sim 26\%$ ($\sim 5.2 \, \mu V_{rms}$ to $3.83 \, \mu V_{rms}$) in the neural recording amplifier using the FC-OTA in Figure 1.

![Figure 2. Cont.](image-url)
In this work, MR1 and MR2 (or MR3 and MR4) play the same role with RS as VX and VY are physically separated and only virtually connected for CM signals, as shown in Figure 2a. In other words, by replacing RS with two transistors operating in the triode region and applying the outputs as shown in Figure 2a, MR1-MR4 can serve CM stabilization and source degeneration for DM signals, respectively. In addition, unlike the CMFB in Figure 2b where the output CM value highly depends on the process parameters [24], a CMFB servo is designed in the existing bias current circuit to accurately adjust the output CM voltage, as suggested in [25]. The voltage VX and VXR are given as:

\[
V_{XR} \approx \frac{I_{D16}}{\mu_nC_{ox}\left(\frac{W}{L}\right)_{RR}(V_{CM} - V_{TH})}, \quad V_X \approx \frac{I_{DS}}{\mu_nC_{ox}\left(\frac{W}{L}\right)_{R1,R2}(V_{outp} + V_{outn} - 2V_{TH})}
\]

where \(\mu_n\) and \(C_{ox}\) are the electron mobility and oxide capacitance, respectively. In the design, MR1-MR4 has the same aspect ratio and the bias current \(I_{DS}\) is \(N\) times larger than \(I_{D16}\) in the CMFB servo, and \((W/L)_{R1-R4} = (N/2)(W/L)_{RR}\). Since the gate voltages for M5 (and M6), and M16 are set as \(V_{B1}\) (by a bias network not shown in Figure 2a), \(V_{XR} = V_X\) therefore:

\[
\frac{1}{2}(V_{outp} + V_{outn}) = V_{CM},
\]

The average of the output voltage well follows \(V_{CM}\) without any apparent errors if all involved transistors are well-matched.

In addition to the compact implementation and no additional power consumption, the proposed CMFB demonstrates better matching than the conventional work. The resistors, \(R_S\) in Figure 1, play as a primary source of mismatch in the output current in the OTA [9,24]. When denoting the nominal value of \(I_{DS}\) and \(I_{D6}\) in Figure 1 as \(I_D\), the mismatch of \(\Delta I_D\) by \(\Delta R_S\) to be:

\[
\frac{\Delta I_D}{I_D} \approx -\frac{(g_m + g_{mb})R_S}{1 + (g_m + g_{mb})R_S} \frac{\Delta R_S}{R_S} \approx -\frac{\Delta R_S}{R_S},
\]

where \(g_m\) and \(g_{mb}\) represent the nominal transconductance and body transconductance of \(M_5\) and \(M_6\). Since it is known that matching of resistors is very poor (~±15%) in modern CMOS processes, the passive \(R_S\) was deliberately made three times the minimum required width to reduce random mismatches into 1–2% [9], resulting in large implementation overhead. In the proposed CMFB, a small mismatch (<±1%) can be easily obtained with a reasonable implementation area because \(R_S\) is implemented with a transistor that has better matching property than a resistor. When assuming the threshold voltage variation
(ΔV_{TH}) is the largest contribution to mismatch of a transistor [24], the resistance mismatch (ΔR_{ds}) by the transistors (M_{R1}−M_{R4}) is given as:

\[
\frac{ΔR_{ds}}{R_{ds}} \approx \frac{ΔV_{TH}}{V_{GS} - V_{TH}},
\]

where \(R_{ds}\) is the effective resistance formed by \(M_{R1}−M_{R4}\) and \(V_{GS}\) is the CM output voltage in steady-state. Since \(ΔV_{TH}\) (in mV) is given as [26]:

\[
ΔV_{TH} \approx \frac{A_{VTH}}{\sqrt{WL}}
\]

where \(A_{VTH} \approx 3.96 \text{ mV/}/\sqrt{\text{μm}}\) in the given 0.18 μm technology and \(W\) and \(L\) are the width and length of a transistor, respectively, an aspect ratio of \((W/L) = 6/16\) (1.5/16 and 4 multiplication) providing an equivalent resistance of 550 kΩ for each \(M_{R1}−M_{R4}\) can easily achieve <0.5% mismatch. For comparison, if the equivalent resistance is implemented with a passive p+ poly resistor without silicide that gives the highest resistivity and best matching in the given process technology, the minimum area of ~900 µm² should be used for a single \(R_S\), that is >4 times larger than the equivalent implementation using transistors. In addition, the variation of the p+ poly resistor is roughly ±15% according to the process datasheet, which means that an even larger area is required to achieve a comparative matching of roughly 1%. Unlike the CMFB loop in Figure 1 or any other CMFB loops employing a separate OTA, the proposed CMFB has a single dominant pole in its loop. Figure 3 shows the CMFB loops for the conventional DDA-based CMFB (Figure 3a) and the proposed CMFB (Figure 3b). While the conventional one has two poles, i.e., a dominant pole at the output and a non-dominant pole at \(V_p\) (at the output of the CMFB OTA), the proposed CMFB has only one dominant pole at the output, thus, there is no stability concern.

\[\text{Figure 3. Simplified CMFB circuits for common mode (CM) control. (a) Conventional differential difference amplifier (DDA)-based CMFB; (b) Proposed CMFB.}\]

One disadvantage of the proposed CMFB may be a low CMFB loop gain and bandwidth due to the low input transconductance formed by the transistors (\(M_{R1}−M_{R4}\), \(M_{RR}\)) in the triode region. To partially compensate for the low bandwidth, the split output capacitor network consisting of \(C_{L1}\) and \(C_{L2}\) was developed, as shown in Figure 2a, instead of \(C_L\) in Figure 1. In the depicted capacitor network, differential signal sees ~2\(C_{L1}\) (by Miller effect) + \(C_{L2}\), while the CMFB operation only does 2\(C_{L2}\). Therefore, the dominant pole at
the output of the proposed CMFB becomes $1/2R_{out}C_{L2}$ that locates at a higher frequency than the dominant pole of the conventional CMFB, $1/2R_{out}C_{L}$ ($C_L >> C_{L2}$). One more apparent disadvantage in the proposed CMFB is the $1/f$ noise contribution from $M_{R1} - M_{R4}$ as compared with $R_S$ in Figure 1 that does not generate $1/f$ noise. However, since the $1/f$ noise from $M_{R1} - M_{R4}$ is scaled by the transconductance of $M_{R1} - M_{R4}$ that is small, the overall noise contribution of the $1/f$ noise from $M_{R1} - M_{R4}$ is negligible.

3. Results and Discussion

To fairly compare the performance, two identical AC-coupled neural recording amplifiers were implemented by using the circuits in Figures 1 and 2b where the same FC-OTAs are used. The design criteria for the FC-OTA were followed in [8], i.e., $g_{m}/I_d$ of the input transistors is maximized ($\approx 27$ V$^{-1}$) and transconductance of other transistors are minimized to meet the specifications for neural recordings. The schematic of the AC-coupled neural recording is shown in Figure 4. This schematic is employed from [8,27], and implemented with a closed-loop gain of 40 dB, a bandwidth of 0.05 Hz to 7.5 kHz, and IRN of $\approx 3.8 \mu$Vrms, which meet the specifications for neural recordings [28]. In addition, $C_{in} = 12$ pF and $C_{fb} = 120$ fF were used and $R_{in}$ is a high resistance pseudo-resistor, which is $\approx 32$ kΩ, which are the values used for a commercial neural recording amplifier [29]. In addition, to emulate the real operations, the noise and output impedance specifications of a commercial regulator (LT 3021$-$1.2) [30] were extracted and used for the power supply, and the lumped model of a bond-wire (assumed that it is an aluminum wire with 1 mil in diameter and 30 mil in length) and the parasitics of the pads were also carefully examined.

Figure 4 shows the simulated CM voltage excursions of the two AC-coupled amplifiers while sweeping $V_{CM}$ from 0 to $V_{DD}$ (1.2 V here). As shown, the output CM voltage varies almost rail-to-rail, 0.12$-$1.08 V, while the conventional DDA-based CMFB operates properly only within one-third of the power supply, 0.42$-$0.79 V. That is an apparent superiority of the proposed CMFB, which comes from the chosen circuit topology. On the one hand, the conventional DDA-based CMFB limits the output swing because the differential pairs for the CMFB have smaller voltage headroom than that in the FC-OTA output branch. On the other hand, the proposed CMFB stacks the transistors, i.e., $M_{R1} - M_{R4}$ in the triode region at the output branch in the FC-OTA, which requires only $\approx 70$ mV additional voltage headroom. As mentioned, one known disadvantage of the proposed CMFB is low CMFB dc gain and bandwidth due to the low input transconductance of $M_{R1} - M_{R4}$. The loop gains (LGs) of the conventional DDA-based CMFB, the proposed CMFB with and without the split capacitor network, and the open-loop gain of the FC-OTA are described in Figure 6. Even though the dc gain of the proposed CMFB is lower than the conventional CMFB by $\approx 2$ dB,
it is roughly 100 dB, showing only 15 dB degradation as compared with the FC-OTA. The relatively high dc gains in the proposed CMFB may guarantee small output CM tracking errors. The smaller bandwidth of ~190 kHz than that of ~300 kHz in the conventional CMFB may be an issue when considering large CM voltage variations commonly observed in neural recording applications. However, when applying the proposed split capacitor network, the bandwidth extends to ~633 kHz. In the implementations, 3.3 and 0.15 pF are used for \( C_{L1} \) and \( C_{L2} \), respectively, while 6.8 pF is assigned for \( C_L \), thereby achieving further area saving as well (6.8 pF \( \rightarrow \) 3.6 pF for output capacitors). In addition, as explained in the previous section, the proposed CMFB does not show the second pole, while the conventional CMFB has it at a frequency of ~300 kHz.

![Loop gains of the conventional DDA-based CMFB and proposed CMFB with and without the split capacitor network.](image)

**Figure 5.** Output CM voltage adjustments according to a reference of \( V_{CM} \) variation for the conventional DDA OTA-based CMFB (red) and proposed CMFB (blue). The ideal voltage transfer characteristic (VTC) is also depicted.

![Loop gains of the conventional DDA-based CMFB and proposed CMFB with and without the split capacitor network.](image)

**Figure 6.** Loop gains of the conventional DDA-based CMFB and proposed CMFB with and without the split capacitor network.

To compare large-signal CM sensitivity, transient noise simulations have been performed. For the simulation, a 1 kHz sinewave of 4 mVpp amplitude input with a 5 kHz CM signal of amplitudes from 50 to 500 mV is applied to both amplifiers, and signal-to-noise and distortion ratios (SNDRs) for both have been calculated, as shown in Figure 7. Considering the broadband neural signals, 1 kHz, 4 mVpp differential input may be able to cover the expected largest amplitude and speed of neural signals [28]. The fast CM with the relatively larger amplitudes than the differential one mimics the artifacts by electrical

| Output CM Voltage (V) | Proposed CMFB | Conventional DDA-based CMFB |
|-----------------------|---------------|-----------------------------|
| ~0.96 V               |               |                             |
| ~0.36 V               |               |                             |

![Output CM voltage adjustments according to a reference of \( V_{CM} \) variation for the conventional DDA OTA-based CMFB (red) and proposed CMFB (blue). The ideal voltage transfer characteristic (VTC) is also depicted.](image)
stimulation. Due to the noise from the power supplies and their finite impedance, the SNDR is degraded by ~3 dB from the ideal value (indicated in the dotted line in Figure 7). The circuit noise limited SNDR (~3.83 μVrms IRN) of ~51.34 dB is also indicated in Figure 7. On the one hand, a relatively constant SNDR was observed, up to 250 mV CM variation in the amplifier with the conventional CMFB, however, it dropped significantly for the larger CM variations. On the other hand, the amplifier with the proposed CMFB shows relatively smooth SNDR degradation, exhibiting better performance when the amplitude of the input CM voltage is larger than 250 mV.

![Signal-to-noise and distortion ratio (SNDR) variations according to input CM amplitude change.](image)

This is because the performance of the DDA-based CMFB highly depends on that of DDA in the CMFB loop, in other words, all the transistors in the DDA must be in the saturation region for the CMFB to work properly. However, the proposed CMFB does not need any specific amplifiers for the CMFB control and only depends on the region of operation of the transistors, i.e., MR1–MR4. As CM voltage grows up, some MR1–MR4 get out of the triode region and operate in the saturation region, resulting in relatively poor CM sensing. But this shift is not abrupt, thus, the proposed CMFB shows higher SNDR even if the CM voltage gets extremely large. The early SNDR degradation of the proposed CMFB comes from the fixed aspect ratio of MR1–MR4 for the fair comparison by realizing 275 kΩ, which can be retarded by adjusting the aspect ratio. To compare the process and mismatch variations of the two implementations, Monte Carlo (MC) simulations were also performed. Figure 8 shows a thousand run global and mismatch MC simulation of IRN from neural recording amplifiers with the DDA-based and proposed CMFBs. The variation of the IRN from the DDA-based CMFB is 1.4 × larger than that from the proposed CMFB. This may not be a meaningful outcome, but we can guess the reason as follows. Since the amplifier with the conventional DDA-based CMFB exhibits more mismatches due to RS, the mean IRN becomes larger in the statistical mismatch simulations. In addition, the mean of the IRN from the amplifier with the conventional DDA-based CMFB shifts higher. The noise from the CMFB OTA cannot play a role in ideal differential signal processing, however there may be a finite CM to DM gain (ACM−DM) when considering mismatches. In other words, some mismatches in the output current (including noise) may convert the CM signal from the CMFB into the DM signal, resulting in the increased IRN. Figure 9 shows the layout of the two FC OTAs with the proposed and the conventional DDA-based CMFBs. Because the proposed CMFB does not require an additional OTA and passive source degeneration (RS), it occupies a smaller area (from 45 × 788 μm² to 45 × 488 μm²).
Table 1 summarizes and compares the key performance of the low-power, low-noise neural recording amplifiers implemented with the conventional DDA-based CMFB and the proposed CMFB. A neural recording amplifier (similar specifications with this work) with a modified DDA-based CMFB [31] is also compared in Table 1 [32]. Moreover, some important performance metrics, such as power and area consumptions and figure of merits (FoM) [29] from the recent standalone CMFBs are added in Table 1 [33,34]. The amplifier with the proposed CMFB consumes ~11% less power and requires ~37% smaller area for implementation because there is no dedicated amplifier for the CMFB and passives for $R_S$ are replaced by transistors. The area occupied by the output capacitors is also reduced by almost half (6.8 to 3.6 pF) due to the split capacitors and the output CM range is extended from 0.64 to 0.96 V. One of the most outstanding feature of the proposed CMFB is the lowest FoM, thanks to zero power consumption for the common-mode regulation.

Table 1. Performance comparison of the neural recording amplifiers with the conventional DDA-based and proposed CMFBs, and other recent standalone CMFBs.

| Tech. Node (nm) | Input Ref. Noise ($\mu V_{rms}$) | Max. $V_{in}$@1 KHz (mV) | $1^\text{st}$ Out CM Var. Thd (mV) | $2^\text{nd}$ $P_{\text{tot}}$ (µW) | $P_{\text{CMFB}}$ (µW) | $3^\text{rd}$ Area (mm²) | $4^\text{th}$ FoM ($\mu A$/kHz) |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Proposed CMFB  | 180 ($σ = 0.0177$) | 3.87 | 5.4 | 80 | 4.82 | 0.022 | 0 |
| DDA-based CMFB | 180 ($σ = 0.0242$) | 3.91 | 4.7 | 30 | 5.42 | 0.035 | 0.0026 |
| [32] 250 | 2.3–2.9 | $>+15$ | $^5$ 35 | 23 | 3 | - | - |
| [33] 180 | - | - | 36 | - | 187 | 0.156 | 0.0002 |
| [34] 180 | - | - | $^5$ 60 | - | 176 | $^5$ 0.003 | $^5$ 0.0041 |

1 Output CM variation range is a percentile for the ratio of the output CM variation range to the supply voltage. 2 $P_{\text{tot}}$ includes the power consumption from all components in a neural recording amplifier, such as OTA, CMFB, and bias networks. 3 MIM capacitors are not included since the active circuit can be buried under the MIM capacitors. 4 FoM is defined by the ratio of current consumption to unity gain bandwidth in Hz. 5 Estimated.
4. Conclusions

A compact continuous-time CMFB circuit for low-power, area-constrained neural recording amplifiers is proposed and the performance of the proposed CMFB is analyzed in the implementation of a fully differential AC-coupled neural recording amplifier and compared with that of an identical neural recording amplifier using a conventional DDA-based CMFB in 0.18 μm CMOS technology post-layout simulation. The proposed CMFB circuit exhibits superior performance to the conventional one. It requires smaller implementation area and no additional power, resulting in ~37% area and 11% power reductions when engaged in a FC-OTA for neural recording amplifiers. In addition, the proposed CMFB facilitates 2.67× larger output CM tuning range and shows ~27% less process variation. All of the advanced performances of the proposed CMFB are preferable for power and area-constrained multichannel neural recording amplifiers.

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