From IC Layout to Die Photo: A CNN-Based Data-Driven Approach

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Abstract—Since IC fabrication is costly and time-consuming, it is highly desirable to develop virtual metrology tools that can predict the properties of a wafer based on fabrication configurations without performing physical measurements on a fabricated IC. We propose a deep learning-based data-driven framework consisting of two convolutional neural networks: i) LithoNet that predicts the shape deformations on a circuit due to IC fabrication, and ii) OPCNet that suggests IC layout corrections to compensate for such shape deformations. By learning the shape correspondence between pairs of layout design patterns and their SEM images of the product wafer thereof, given an IC layout pattern, LithoNet can mimic the fabrication procedure to predict its fabricated circuit shape for virtual metrology. Furthermore, LithoNet can take the wafer fabrication parameters as a latent vector to model the parametric product variations that can be inspected on SEM images. In addition, traditional lithography simulation methods used to suggest a correction on a lithographic photomask is computationally expensive. Our proposed OPCNet mimics the optical proximity correction (OPC) procedure and efficiently generates a corrected photomask by collaborating with LithoNet to examine if the shape of a fabricated IC circuitry best matches its original layout design. As a result, the proposed LithoNet-OPCNet framework cannot only predict the shape of a fabricated IC from its layout pattern, but also suggests a layout correction according to the consistency between the predicted shape and the given layout. Experimental results with several benchmark layout patterns demonstrate the effectiveness of the proposed method.

Index Terms—Design for manufacturability, convolutional neural networks, virtual metrology, lithography simulation, optical proximity correction.

I. INTRODUCTION

AFTER IC circuit design and layout, it typically takes two to three months to fabricate a 12-inch IC wafer, involving a multi-step sequence of photolithographic and chemical processing steps. Among these steps, a lithography process is used to transfer an IC layout pattern from a photomask to a photosensitive chemical photosresist on the substrate, followed by an etching process that chemically removes parts of a polysilicon or metal layer, uncovered by the etching mask, from the wafer surface. Because it is hard to control the exposure conditions and the chemical reactions involved in all fabrication steps, the two processes together lead to nonlinear shape distortion of a designed IC pattern, which is usually too complicated to model. This fact gives rise to an issue so-called mask optimization, a procedure that computes an optimized photomask (or etching mask) to make the shape of the fabricated IC wafer best consistent with its source layout design.

The inevitable shape deformations on a fabricated IC due to the imperfect lithography and etching processes often cause IC defects (e.g., thin wires or broken wires) if an IC circuit layout is not appropriately designed, especially on the first few metal layers. Nevertheless, in most cases we still cannot identify such IC defects due to inappropriate IC circuit layout until capturing and analyzing the scanning electron microscope (SEM) images of metal layers after the wafer fabrication process, making the circuit verification very costly and time-consuming.

It is therefore desirable to develop pre-simulation tools, including i) a lithography simulation method for predicting the shapes of fabricated metal lines based on a given IC layout along with IC fabrication parameters, and ii) a mask optimization strategy for predicting the best mask to compensate for the shape distortions caused by the lithography and etching processes.

As for lithography simulation, there are two categories of conventional approaches: physics-level rigorous simulation and compact model-based simulation [1], [2]. Rigorous simulation methods simulate physical effects of materials to accurately predict a fabricated wafer image and thus are very time-consuming [3], [4]. On the contrary, a compact model-based simulation method follows loosely physical phenomena to chase a faster computational speed by exploiting complicated, parameter-dependent, non-linear functions. Different from traditional methods, we aim at developing a convolutional neural network (CNN) based approach, which learns the parametric model of physical and chemical phenomena of a fabrication process directly from a training dataset containing pairs of IC layouts and their corresponding SEM images. Based on the learned network model, we can predict a fabricated wafer image more accurately and efficiently than conventional methods.

Moreover, fab-engineers usually optimize a mask pattern by iteratively modifying the layout design based on its lithogra-
phy simulations. However, rule-based lithography simulations resort to linear combinations of optical computations derived from several similar yet not identical historical fab-models. This fact may make conventional mask optimization methods unreliable against new layout patterns. The simulation reliability largely relies on a rich amount of historical fabrication data in the database, which is, however, very costly because ground-truth fab-models need to be gathered by fabricating a layout pattern with all possible configurations.

The relationship among the IC fabrication process, lithography simulator, and mask optimizer is illustrated in Fig. 1 where the “OPC” block stands for optical proximity correction, a standard approach to photomask correction for compensating for the shape distortions due to diffraction or process effects as well as guaranteeing the printability of a layout pattern, especially the printability at the corners of the process window. As illustrated in the red dashed rectangles in Fig. 1 the mask used in the fabrication process is a modified version of a source layout design, aiming to compensate for possible “shrinkages” in line shapes due to the fabrication to mitigate the deviation of a fabricated IC circuitry from its layout design pattern. However, traditional OPC simulations have two primary drawbacks. First, it runs simulations based on those rules and patterns already known; thus, an OPC correction may be unreliable if an unseen layout design is given. Second, not only is a single OPC simulation computationally expensive, but also the whole OPC procedure is a time-consuming trial-and-error routine that is iterated until no irregularity can be found in the OPC estimation result. Due to its high complexity, the OPC simulation is usually performed on a limited number of regions of interest (ROIs) rather than on the whole layout design to reduce computation. Take the ICWB software (IC WorkBench) developed by Synopsys for example. ICWB takes, in average, about 34 seconds to run a simulation on an $4 \times 1.7\mu m^2$ layout patch with an Intel Xeon E5-2670 CPU and 128GB RAM. It will cost around 4 days to run once an $4 \times 170\mu m^2$ layout design, and such computational cost makes a complete OPC simulation procedure impractical. It is therefore highly desirable to develop an efficient photomask optimization scheme.

Recent progress on image-to-image translation techniques makes them suitable to tackle the above-mentioned lithography simulation (i.e., Layout-to-SEM) and photomask optimization (i.e., SEM-to-Layout) problems. However, these two issues are more complicated than general image-to-image translation problems. Take Layout-to-SEM prediction for example. First of all, the domain of IC layout images and the domain of SEM images are heterogeneous. An IC layout is a purely man-made blueprint with only lines and rectangles on it, and hence it is noise-free and artifact-free. On the contrary, an SEM image is formed by the intensity of detected signal from raster-scanning the IC surface with a focused electron beam. In additional to the continuous shape distortions introduced by the lithography and etching processes, the SEM imaging process itself also suffers from several kinds of interference (e.g., scan-line noise and shading). This fact leads SEM images to a significantly different domain from that formed by layout images. Hence, this issue is essentially a cross-domain image matching and translation problem. Second, in order to predict the corresponding SEM image from an IC layout, our solution must be capable of characterizing the shape correspondence between these two domains of images. This fact raises an unsupervised cross-domain image matching problem, which usually has not been concerned in general image-to-image translation techniques, and thus it requires a more sophisticated solution, as the concerns stated in [8], [9]. Third, for mask optimization problem, it is very costly to collect a comprehensive set of ground-truth OPC-corrected photomasks, making the training of a photomask optimization network infeasible.

To address the above problems, as illustrated in Fig. 2, we propose a fully data-driven framework that comprises two CNN-based modules, namely, LithoNet and OPCNet, functionally complementary to each other. In short, LithoNet is a cross-domain simulator of the lithography and etching processes in IC fabrication, and OPCNet is a self-supervised mask optimization CNN using the prediction results of LithoNet as supervision for the purpose of optical proximity correction.
This paper has four primary contributions:

- To the best of our knowledge, we are the first to formulate the Layout-to-SEM deformation prediction problem as a cross-domain image translation and correspondence problem, and we propose a two-step CNN-based framework to address it.
- The proposed LithoNet-OPCNet system is computationally much more efficient than typical optical-based contour simulation scheme, while achieving comparable prediction accuracy. Therefore, our method could enable IC fabrication plants to run a full, large-scale screening on new IC layout designs. Note that the standard OPC approaches rely on sophisticated design rules and design patterns already in the database, and thus it can only examine a limited amount of areas each time.
- The proposed LithoNet is parameterized with fabrication settings. Hence, it can also predict results under different fabrication conditions so as to assist fabrication plants to find the best suitable working intervals of parameters and thus be beneficial for yield-rate improvement.
- The proposed OPCNet overcomes the difficulty in lack of ground-truth mask patterns. With the aid of a novel training objective function called \textit{IO-consistency} loss, the proposed OPCNet can well simulate the mask optimization process in collaboration with LithoNet.

The remainder of this paper is organized as follows. We review related literature in Section II. The proposed LithoNet and OPCNet are detailed in Section III and IV, respectively. Section V demonstrates and discusses our experimental results. Finally, we draw our conclusion in Section VI.

II. RELATED WORK

A. Virtual Metrology

In IC fabrication, virtual metrology (VM) refers to the methods for predicting wafer properties based on fabrication parameters and sensor data from equipment without performing physical measurements on the product wafer produced by a whole costly fabrication process [10]. Since VM techniques can significantly reduce the cost of IC fabrication, various kinds of VM methods have been proposed to address the fabrication quality prediction issues. For example, for the prediction of average Silicon Nitride cap layer thickness, regression-based VM methods were developed as surveyed in [11]. Specifically, Susto et al. exploited the knowledge collected in the process steps to improve the accuracy of VM prediction via a multi-step strategy [12]. In addition, the demand of VM methods also triggers the development of theoretical techniques. The method proposed in [13], for instance, focused on the OPC mask design problem and modeled it as an inverse problem of optical microlithography. Optical lithography is a process used for transferring binary circuit patterns onto silicon wafers, and related discussions about lithography techniques can be found in [14]. Recently, people have been attempting to integrate machine learning methods with IC implementation and VM [11]. This research has resulted in various works, such as Yang et al. [17], [18]. For example, Yang et al. proposed a generative adversarial network (GAN) based inverse method to estimate the optimal mask used in the fabrication process from an OPC simulation result [17]. However, Yang et al.’s design concentrates only on the OPC-to-Layout problem, which operates in an opposite direction of our Layout-to-SEM prediction. Therefore, to the best of our knowledge, there is no existing technique focusing simultaneously on both Layout-to-SEM (lithography simulation) and SEM-to-Layout (mask optimization) image translation problems. We deem that a hybrid method of image-to-image translation or feature mapping techniques could compose a naive solution to these two prediction problems.

B. Lithography Simulation

Recently, there have been lithography simulation methods developed based on machine learning techniques. For instance, Watanabe et al. proposed a fast and accurate lithography simulation by determining an appropriate model function via CNN [11], and Ye et al. developed a GAN-based end-to-end lithography modeling framework, named LithoGAN, to map directly the input mask pattern to the output resist pattern [2]. Specifically, LithoGAN models the shape of the resist pattern based on a conditional GAN (cGAN) model and predict the center location of the resist pattern via a CNN model. LithoGAN has a dual learning framework, and similarly our LithoNet also adopts a dual learning framework.

As will be detailed in Section III, we formulate the Layout-to-SEM prediction as a cross-domain image-to-image translation problem in the LithoNet design. Recent image-to-image translation methods can be divided into two groups. One requires pairwise training images, e.g., [20], [21], and the other supports training on unpaired data, e.g., [22]. The method proposed in [22] was based on GANs [19] and VAEs [23], but it was designed for unsupervised image-to-image translation tasks, which could be considered as a conditional image generation model. Furthermore, the Pix2pix model [20] consists of a Unet-architected generator and a PatchGAN discriminator. Pix2pix uses the PatchGAN discriminator to model high-frequencies by classifying if each patch in an image is real or fake. Therefore, it can be adopted in various applications, such as the conversion of a cartoon map to a satellite image and the conversion of a sketch to a natural image, and becomes a benchmark in this field. The Pix2pix method was further enhanced in [21] by taking advantages of a course-to-fine generator, a multi-scale discriminator, and a robust adversarial learning objective function so as to generate high-resolution photo-realistic images. However, none of above methods addresses the shape correspondence or the deformation field between two different domains of images, and neither do other representative image-to-image translation methods, such as CycleGAN [24], DualGAN [25], Coupled GANs [26], and [22].

However, existing image-to-image translation methods are usually inappropriate for this Layout-to-SEM image translation problem for the IC-fabrication VM purpose. Because characterizing the deviations on metal lines in a product IC from their source layouts is a critical point in IC-industry, those traditional image-to-image translation methods that lack
Fig. 3. Block diagram of the proposed two-step framework for cross-domain image-to-image matching and translation. The upper step adopts CycleGAN to transfer the training SEM images to another reference domain as ground-truth binary labels. The lower LithoNet step estimates the deformation maps between the input layout patterns and their corresponding ground-truth binary labels.

a mechanism for precisely estimating a deformation field or the shape correspondence between the layout and SEM images are not applicable to this problem. To serve the above purpose, the proposed LithoNet model performs cross-domain image-to-image translation via learning the shape correspondence between paired training images so as to output a predicted deformation map for further VM applications.

C. Mask Optimization

There also exist machine learning-based mask optimization approaches. For example, the GAN-OPC method proposed in [17] takes source layout patterns and their OPC simulation results as training inputs, and accordingly for an input layout design, predicts a corrected photomask that minimizes the deviations on the (simulated) fabricated circuit shapes from its original design. In order to facilitate the training process and guarantee convergence, GAN-OPC involves a pre-train procedure that trains jointly the neural network and the inverse lithography technique (ILT) [29]. After GAN-OPC converges, the obtained quasi-optimal photomask is further used as a good enough initial for further ILT operation. In addition, Yu et al.’s method can perform simultaneously sub-resolution assist feature (SRAF) [30] and edge-based OPC according to a DNN framework [18]. However, both the two methods require a collection of photomask images, such as those suggested by OPC or historical data gathered during actual fabrication process, as the ground-truth dataset for training. Because it is expensive and time-consuming to collect qualified mask images, the cardinality of the training dataset forms a performance bottleneck of these two methods. To eliminate such bottleneck, powered by LithoNet, we propose the OPCNet model for mask optimization. Because OPCNet and LithoNet are the inverse function to each other, OPCNet can be trained directly by using the SEM-styled images predicted by LithoNet without the need of using expensive photomask patterns, as will be elaborated later.

Fig. 4. Two heterogeneous domains of images. (a) Layout designs. (b) SEM images.

III. LithoNet: A CNN-Based Simulator of Lithography

As illustrated in Fig. 3, the proposed LithoNet consists of a CycleGAN-based [24] domain transfer network and a deformation prediction network. LithoNet is designed to learn how an IC wafer fabrication process deforms the shape contours of a layout pattern. It thus can simulate the fabrication process to predict the shape deformation caused by the fabrication process for further virtual metrology applications based on i) a given layout and ii) a set of fabrication parameters. One major difficulty in learning the deformation model between a layout pattern and the corresponding SEM image of its fabricated circuitry lies in the fact that they are from heterogeneous domains. Specifically, an SEM image is a high-resolution, 8-bit, gray-scaled image with deep DOF (depth of field), whereas a layout is no more than a man-made binary pattern with only rectangular regional objects on it. As a result, the goal of LithoNet is to predict the contour shapes by learning the pixel-wise shape correspondence between every paired layout and SEM images. Nevertheless, due to the poor contrast and scanning pattern noise in SEM images, it is usually difficult to
capture edge contours correctly from SEM images, on which a 1-pixel-drift corresponds to a nanometer-scale displacement on real IC products. Therefore, transferring the domain of SEM images to another intermediate domain without the above-mentioned contrast and noise problems would be beneficial.

To this end, we propose a two-step framework. In the first step, we use CycleGAN \cite{24} to transfer a gray-scale SEM image to an intermediate domain, where images have SEM-styled shape contours and layout-styled clear background. Then, in the second step, given a source layout along with fabrication parameters, LithoNet predicts the shape deformation due to the fabrication process. In sum, Step-I learns to remove the difference between the SEM image and its man-made binary shape so that Step-II can learn the shape correspondence between the SEM image and its original layout. In the following subsections, we will introduce our design in details.

A. Step I: Image domain transfer

Because SEM and layout images are of heterogeneous domains (styles), as demonstrated in Fig.4 we adopt an image domain transfer technique to align their domains. By removing the interference introduced the SEM imaging process, such as bias in brightness/contrast and scan-line noise in the background, via CycleGAN \cite{24}, the processed SEM image can be regarded as in the same domain as the layout. That is, the processed SEM image retains its curvilinear shape boundaries yet is binarized as if it were a layout.

To this end, we train CycleGAN using i) a set of product-ICs’ SEM images and ii) their associated segmentation masks. The second set of images can be derived by applying either advanced thresholding \cite{31}, \cite{32}, interactive segmentation \cite{33}, \cite{34}, or pseudo-background subtraction \cite{35} on the source SEM images. Note that in order to guarantee the performance of domain transfer, segmentation masks with incorrect segmentation results are discarded under user-supervision. Finally, we utilize the well-trained CycleGAN to transfer source SEM images into the layout style, and these processed SEM images are further taken as reference ground-truths to train LithoNet in Step-II.

Employing CycleGAN for domain transfer has two advantages. First, CycleGAN is an unpaired image-to-image translation method, and hence it can learn the majority decision of many image segmentation algorithms, including the analysis software provided by the SEM vendor, for SEM images based on a large collection of segmentation results of different methods. Second, utilizing a "U-net Generator" to translate images, CycleGAN is essentially a U-net-based segmentation method \cite{36} supervised by its built-in "Discriminator" through an adversarial loss, thereby suggesting a more reliable segmentation result than U-net, a state-of-the-art segmentation benchmark. Additionally, we can simply discard some rare unreliable CycleGAN segmentation results by quick human-inspection to prevent our LithoNet from learning incorrect contour correspondences.

B. Step II: Shape Deformation Prediction

To learn the shape correspondence and the deformation field between SEM and layout images, LithoNet is trained by image pairs, each containing a layout and a ground-truth segmentation mask, i.e., a processed SEM image, generated in Step-I described in Section III-A.

As shown in Fig.5 LithoNet consists of a generator and a warping module. The generator is a U-net \cite{36} like network that outputs a 2D dense correspondence map depicting the deformation field between the paired training images. Then, using the sampling strategy used in the spatial transformer network (STN) \cite{37}, the warping module synthesizes a warped version of the given input layout to simulate a wafer-fabricated circuitry based on the deformation map. STN is a differentiable module designed for enabling neural networks to actively spatially transform feature maps so that neural network models can learn invariance to translation, scale, rotation, and warps. Consequently, we adopt the sampling strategy of STN to benefit our LithoNet.

In contrast with common image generation networks like \cite{20}, \cite{38}, the advantages of LithoNet are twofold. First, LithoNet can generate and visualize a predicted deformation field, and therefore what have been learned by the network, i.e., the shape correspondences between input training image pairs, can be verified straightforwardly. Second, based on the visualized deformation field, it would be easier to identify possible impacts (e.g., defects), no matter global or local, caused by the layout and the configuration parameters during fabrication process, on the physical appearance of an IC’s metal layer. Concisely, the deformation field generated by our LithoNet is beneficial for clarifying both global and local shape correspondences between a layout and the SEM image of its product IC.

C. Training Loss Functions

The training loss function \( L_{total} \) of LithoNet is primarily defined in the following form

\[
L_{total} = L_{rec} + L_{var} + L_{smooth} + L_{reg} + L_{par}. \tag{1}
\]

where, \( L_{rec} \) denotes the reconstruction loss that measures the dissimilarity between the training ground-truth \( I \) and the synthetic SEM-styled image \( J \). Meanwhile, \( L_{var} \) measures the variability difference between a paired training image pair, and \( L_{smooth} \) guarantees the smoothness of the deformation map. Finally, \( L_{reg} \) is used to penalize large displacements on the deformation map, and \( L_{par} \) is the regression loss of fabrication parameters.

A) Reconstruction Loss:

The reconstruction loss term \( L_{rec}(I, J) \) is defined as the \( L_1 \) loss between the training ground-truth \( I \) and the synthetic SEM-styled image \( J \) as follows:

\[
L_{rec}(I, J) = \frac{1}{n} \| I - J \|_1, \tag{2}
\]

where \( n \) denotes the number of pixels. We derive \( L_{rec} \) by the following steps: i) sampling densely pixel positions on the to-be-generated \( J \); ii) locating the correspondences of them on the input layout according to the deformation map \( M \) that records the mapping relationship between pixels on \( I \) onto their counterparts on \( J \); iii) using backward interpolation to estimate the sampled pixel values on \( J \), i.e., \( J(x, y) = \)
\[ L_{\text{var}}(I, J) = \sum |\nabla(I - J)|. \] (3)

This term is designed to align the shape contours of \( J \) with those of \( I \). Without this term, the loss function might be dominated by the reconstruction loss described in (2), and consequently LithoNet would generate a bizarre synthetic image \( J \), which can produce a high overlap ratio compared with ground-truth image \( I \) but has unnaturally jiggling contours. In other words, \( L_{\text{var}} \) aims to retain the shape similarity.

C) Smoothness Loss

The smoothness loss is a penalty term defined as the \( L_1 \)-norm of the weighted gradient of the deformation map:

\[ L_{\text{smooth}} = \| \nabla(M) \circ W \|_1, \] (4)

where \( \circ \) denotes the Hadamard product, and \( W \) is an edge-aware weighting matrix defined as

\[ W(x, y) = e^{-|\nabla S(x,y)|+|\nabla I(x,y)|}. \] (5)

Note that contour edges on the input layout \( S \) and the ground-truth layout-styled SEM image \( I \) result in discontinuities in the deformation map \( M \). Because such discontinuities contribute to unnecessary smoothness penalty, \( L_{\text{smooth}} \) should be suppressed appropriately according to the gradient information of both layout and SEM images.

D) Regularization Loss

The regularization loss is defined as the \( L_1 \)-norm of the deformation map \( M \):

\[ L_{\text{reg}} = \| M \|_1. \] (6)

This term reflects the fact that the deformation caused by wafer fabrication tends to be small, as will be discussed in Section V.C.2.

E) Regression Loss for Fabrication Parameters

Because the configuration parameters of a fabrication process are continuous variables that influence the physical appearance of a wafer layer, we formulate the relationship between the fabrication parameters and the appearance of wafer layer as a regression problem. The regression loss \( L_{\text{par}} \) is defined as

\[ L_{\text{par}} = \| D_y(G(S|y_0) - y_0) \|_2 + \| D_y(I_{y_0}) - y_i \|_2. \] (7)

where \( I \) is the reference IC shape segmented from the ground-truth SEM image used for training; \( y_0 \) is the fabrication parameter corresponding to \( I_{y_0}, S \) and \( y_0 \) respectively denote the input layout and input fabrication parameter vector for prediction, and \( G(S|y_0) \) is the predicted deformed IC shape. Therefore, this loss term aims to train i) a generator able to predict a synthesized SEM-styled image based on the given \( S \) and \( y_0 \), and ii) a discriminator able to estimate the fabrication parameter vector \( y_i \) associated with \( I_{y_0} \).

IV. OPCNet: A CNN-Based Photomask Corrector Based on LithoNet

As described in Section II-C, the major challenge in developing a learning-based mask optimizer is to collect a comprehensive amount of ground-truth mask data corresponding to various layout patterns, e.g., well OPC-corrected photomasks leading to desired shapes of fabricated circuitry. This is, however, very costly and time-consuming. To overcome this difficulty, as shown in Fig. 2 we utilize a pre-trained LithoNet as an auxiliary module to train our photomask optimizer, OPCNet. Given an IC layout pattern, OPCNet aims to predict an OPC-corrected mask pattern so that, after being deformed by the lithography and etching processes that are simulated by LithoNet, the predicted deformed shape will be as close as the original layout pattern. Therefore, OPCNet can be regarded as the inverse model of LithoNet. As a result, for a desired layout pattern, we can use its predicted outputs of LithoNet as the input of OPCNet, and the desired layout itself as the corresponding output of OPCNet. Given a collection of such input-output pairs, we can train OPCNet without the need of collecting the “ground-truth” OPC-corrected photomask patterns.

Specifically, given a layout design pattern \( S \), OPCNet aims to generate a photomask \( K \), whose lithography and etching simulation result \( J \) predicted by LithoNet best matches \( S \). This design makes our OPCNet “groundtruth-free” during the training stage should LithoNet have been already well-trained. In addition, with the design of the input-output consistency loss used to measure the dissimilarity between a layout design pattern \( S \) and its lithography simulation result \( J \), OPCNet becomes an self-supervised learning method. The whole pipeline of our mask optimization method is illustrated in Fig. 3. Note that i) the pretrained LithoNet is fixed while training OPCNet, and ii) OPCNet is intrinsically a generator for translating a layout pattern \( S \) into its optimal photomask \( K \) based on the wafer fabrication model learned by LithoNet.

A. Training Loss Functions for OPCNet

The overall training loss \( L_K \) of OPCNet is defined as

\[ L_K = L_{\text{IO}} + L_{K_{\text{var}}} + L_{K_{\text{smooth}}}. \] (8)

where, \( L_{K_{\text{consistency}}} \) denotes the input-output consistency loss measuring the dissimilarity between input layout \( S \) and LithoNet’s output \( J \). \( L_{K_{\text{var}}} \) represents the total variation loss on the difference between \( S \) and \( J \). \( L_{K_{\text{smooth}}} \) denotes the mask smoothness loss for ensuring the smoothness of the obtained photomask patterns \( K \).

A) Input-Output Consistency Loss:

The input-output consistency loss \( L_{K_{\text{consistency}}}(S, J) \) aims to guide the learning of OPCNet so that the shape predicted by LithoNet \( J \) best matches the desired input layout.
settings ranging from −0.9 to +0.9. In total, UMC dataset #1 contains (i) a 942-pair training subset and (ii) a 100-pair blind testing subset, whereas UMC dataset #2 contains (i) a subset comprising $1057 \times 7$ pairs for training and (ii) another subset comprising $12 \times 7$ pairs for blind testing. All images in the blind testing set are collected from historical fabrication data; compared with those in the training sets, the blind test images are of much larger dimension and contain unseen design patterns. We trained CycleGAN for style-transfer in Step-I on UMC dataset #1, and LithoNet on UMC datasets #1 and #2. As for OPCNet, it was trained on paired data, each of which contains (i) a layout image $S$ in the first dataset and (ii) its fabricated IC shape $J$ predicted by feeding $S$ into a pre-trained LithoNet. As a result, OPCNet can be trained in an unsupervised manner. In our experiments, all image patches are downsampled from $512 \times 512$ to $256 \times 256$ to reduce the computational complexity. The five loss terms described in (1) are weighted empirically by $(100, 0.001, 150, 0.002, 10)$.

B. Performance Metrics

The performance of our model is evaluated objectively in terms of some widely-used similarity metrics, including Intersection Over Union (IOU), SSIM [40], and per pixel error rate. We will demonstrate in detail that our model outperforms other image-to-image translation methods and the standard OPC approach.

C. LithoNet

1) Image domain transfer: In Fig. 5, we compare our image domain transfer results with images derived by the traditional Otsu’s method [32]. Obviously, the source SEM images contain typical complications from SEM image processing, such as bias in brightness/contrast probably due to gain-shift and scanning-pattern noise. It is thus difficult for common methods to threshold an SEM image appropriately. By exploiting a well-trained translator, e.g., CycleGAN [24], an SEM image can be transferred into a layout-styled format with its contour shape keeping unchanged.

2) Prediction Results: Fig. 6 illustrates the deformation map predicted from the input layout, the predictions of fabricated IC shapes based on the deformation map, and the corresponding ground-truths of fabricated IC shapes extracted from their associated SEM images. The deformation maps show that LithoNet successfully learns to widen lines within open areas and to condense lines otherwise. Because such information is the key to the metrology applications, such as layout scoring and OPC simulation described in Fig. 1, this experiment also demonstrates that LithoNet can be used to bridge computer vision techniques with both fields of semiconductor manufacturing and computer-aided-design.

3) Ablation Study of Loss Terms: Here we examine and discuss the effectiveness of individual loss terms in (1). First of all, we made numerical comparisons among different loss settings in Table I and Table II, each of which corresponds to

\[ L_{K_{var}}(S, J) = \sum |\nabla (S - J)|, \]  

\[ L_{K_{smooth}} = \|\nabla K\|_1. \]
Fig. 6. Comparison of the input layout patterns, predicted deformation maps, the predictions of fabricated IC shapes based on the deformation maps, and the ground-truths of fabricated IC shapes extracted from their associated SEM images.

Fig. 7. Prediction results by LithoNet trained on UMC dataset #1 without the smoothness loss term $L_{\text{smooth}}$.

Fig. 8. Subject visual quality comparison of LithoNet with and without the total-variation loss $L_{\text{var}}$, where the “Baseline” column demonstrates images derived using $L_{\text{total}} - L_{\text{var}}$ and the “Full” column shows predictions synthesized using $L_{\text{total}}$.

The visual effect brought by the total-variation loss $L_{\text{var}}$ is demonstrated in Fig. 8, where the “Baseline” column demonstrates images derived using $L_{\text{total}} - L_{\text{var}}$, whereas the “Full” column shows predictions synthesized using $L_{\text{total}}$. This experiment set shows how $L_{\text{var}}$ improves the visual quality of synthetic SEM-styled images. Take regions highlighted by red rectangles in Fig. 8 for example. Without $L_{\text{var}}$, LithoNet tends to produce straight-line edges and sharp corners, although there are no such patterns on the training images produced by a real IC fabrication process, as shown in “Ground truth” column. By adding $L_{\text{var}}$ to the total loss function, such artifacts can be largely mitigated, thereby more faithfully predicting the shapes of segmented SEM images.

4) Comparison with Pix2pix: As LithoNet is kind of image-to-image translation schemes, we compare it with Pix2Pix...
a representative GAN-based image-to-image translation method. This experiment set was designed for two purposes. One is to verify if LithoNet is able to learn special shape correspondence between layout and SEM images, and the other is to check if LithoNet is more advantageous than Pix2pix in this regard.

As shown in Table I, Pix2pix achieves slightly higher objective metric values than LithoNet. This situation, however, lies in the fact that these objective metrics mainly reflect the effect of the reconstruction loss term solely. Nevertheless, compared to Pix2pix, our total loss function described in (1) contains several additional loss terms, including $L_{reg}$, $L_{par}$, and $L_{smooth}$, which do actually lead to better visual quality as will be explained later.

As illustrated in Fig. 9, Pix2pix produces artifacts like blurred and jiggled contour edges, whereas LithoNet is able to generate clear and smooth ones. Since both Pix2pix and LithoNet utilize $L_1$-norm to guarantee a global shape similarity, this phenomenon would be probably due to the different control strategies over local shapes. Specifically, LithoNet makes use of the total-variation loss, smoothness loss, and regularization loss to control the local deformations, whereas Pix2pix relies on its discriminator architecture, the so-called PatchGAN design that penalizes a structure at the scale of patches, to handle local deformations. Consequently, because PatchGAN does not put any penalty on blurred and jiggled edges and learns only to classify if each generated patch looks realistic, such artifacts are reasonable trade-offs of Pix2pix’s PatchGAN design.

Fig. 10 compares the prediction results of feeding LithoNet and Pix2pix with test images containing significantly distinct layout patterns from those in the training image set. Moreover, the source dimension of these testing images is much larger than the training data. Therefore, through this experiment we can appraise the reliability and robustness of LithoNet and Pix2pix in mimicking an IC fabrication process when the input layout is a brand new, unseen pattern of a different scale. We can observe from Fig. 10 that, for unseen layout patterns of a different scale, LithoNet significantly outperforms Pix2pix in terms of the clarity and integrity of shape boundaries, although the predictions of LithoNet still cannot perfectly match the ground-truth for lack of suitable training samples. Finally, Table III lists the numerical comparisons between LithoNet and Pix2pix for this case.

5) Fabrication parameters: Fig. 11 compares the predictions by LithoNet trained on UMC dataset #2 driven by different configuration parameter values for wafer fabrication. We focus on one configuration parameter which is normalized to the range of $[-0.9, 0.9]$ and is inversely proportional to the degree of etching: the larger the parameter value, the lower the degree of etching. Those parameters values used in the training dataset are colored black, whereas those values not used in training are colored red. This experiment shows that the proposed LithoNet, thank to the regression loss term $L_{par}$ described in (7), does learn the relationship between the line width and the fabrication parameter used to control the degree of etching in the fabrication process. Concisely speaking, the larger the parameter is, the wider the metal line should be. Hence, our LithoNet model is able to mimic the fabrication process and generate parameter-dependent prediction results. This is an important aspect of LithoNet design, and such de-

| Method       | Avg IOU  | Avg SSIM | Avg Error |
|--------------|----------|----------|-----------|
| Pix2pix      | 0.6587   | 0.6396   | 0.1358    |
| LithoNet     | 0.7107   | 0.6906   | 0.1170    |

TABLE III
Comparison between LithoNet and Pix2pix, both trained on UMC dataset #1, for unseen layout patterns of a different scale
Fig. 10. Subjective visual quality comparison between Pix2pix and LithoNet, both trained on UMC dataset #1, for some unseen layout patterns of a different observation scale.

Fig. 11. Predictions by LithoNet trained on UMC dataset #2 driven by different configuration parameter values for wafer fabrication. We focus on one configuration parameter which is inversely proportional to the degree of etching: the larger the parameter value, the lower the degree of etching, and the wider the metal lines. Those parameters values used in the training dataset are colored black, whereas those values not used in training are colored red.

sign makes LithoNet suitable for semiconductor manufacturing simulations.

6) Model generality: We examine here LithoNet’s range of applicability. The image pair in the top row of Fig. 12 shows that, in an open area, the general fabrication process typically produces a metal line wider than its layout design, as highlighted by the red rectangle. The predicted image shown in the bottom row of Fig. 12 tells that LithoNet learns the shape correspondence between paired training images, so it predicts a wider line in an open area and a narrower one in between two neighboring lines. In addition, the highlighted regions in Fig. 13 demonstrate that at image borders the predictions by LithoNet are different from the ground-truths. This is because, at image borders the shape deformations due to the lithography and etching processes behave differently from those in non-border regions, but LithoNet treats them regularly. For example, LithoNet regards a line reaching a patch border should extend to the adjacent patch rather than shrink from the border. Such border effects can be easily handled by collecting enough training data at image borders.
along with an additional label signifying whether a region is a border one. Consequently, LithoNet can be expected to forecast fabrication results as long as a large enough amount of training data is given.

Finally, we design another experiment to show that LithoNet can well learn the "necking" and "rounding" effects that usually occur in IC fabrication, as highlighted by red rectangles in Fig. 14(a) and indicated by the red and blue arrows in Fig. 14(b). Necking is a high-risk pattern caused by either a tip-to-line or a line-end too close to another line on the layout design. As illustrated in Fig. 14(b), such situations may result in a line narrower than designed after fabrication. Hence, this experiment set evidences again that a well-trained LithoNet is capable of mimicking the semiconductor lithography and etching procedures.

D. OPCNet

1) Impacts of Loss Functions: As described in Section IV, given a layout design pattern \( S \), OPCNet aims to generate a mask \( K \) whose lithography simulation result \( J \) predicted by LithoNet is best similar to \( S \). The OPCNet is controled jointly by the IO-consistency loss \( L_{IO} \), the total-variation loss \( L_{Kvar} \), and the mask smoothness loss \( L_{Ksmooth} \). The former two loss terms measures the dissimilarity between \( S \) and \( J \), whereas the third one focuses on the smoothness of \( K \). We here examine how \( L_{Kvar} \) and \( L_{Ksmooth} \) contribute to the mask prediction task.

Demonstrated in Fig. 15 are three columns of images, each of which corresponds to one loss setting. Comparing the mask predicted by using \( L_{IO} \) with that by \( L_{IO} + L_{Kvar} \), we can find that \( L_{Kvar} \) guarantees the quality of shape contour in the lithography simulation. No matter the \( L_{var} \) of LithoNet or the \( L_{Kvar} \) of OPCNet, such total variation loss accounts for the difference between predicted contours and their ground-truth and focuses on \( k \) pixels around the contour pixels. This term helps \( L_{IO} \) guarantee the similarity between the input layout and the lithography simulation and also avoid unexpected artifacts at contours. Finally, comparing the mask predicted by \( L_{IO} + L_{Kvar} \) with that by \( L_{IO} + L_{Kvar} + L_{Ksmooth} \), we find that \( L_{Ksmooth} \) can globally suppress unexpected artifacts on the predicted mask image. The mask prediction derived by \( L_{mask} \) described in [8] can thus be artifact-free and smooth.

2) Mask Prediction Results: Finally, demonstrated in Fig. 16 are the masks predicted by OPCNet. Given a well-trained and accurate lithography simulator LithoNet, Fig. 16 evidences that our mask optimizer OPCNet can successfully perform the mask optimization task in a self-supervised learning manner without the need of collecting ground-truth OPC-corrected masks. With OPCNet, a layout pattern can be adequately corrected so that the resulting circuit shape best matches the source layout pattern, after an IC-fabrication process.

VI. CONCLUSIONS

In this paper we proposed a data-driven framework involving two convolutional neural networks: LithoNet and OPCNet. First, given a layout for virtual metrology, LithoNet mimics the lithography and etching processes in IC fabrication to predict the shape of a fabricated IC circuitry of a given layout design. By learning the shape correspondence between paired training images, i.e., IC layout designs and their fabricated IC SEM images, LithoNet can predict the shape deformation field of the layout and then generate a lithography simulation result. Second, with pre-trained LithoNet, OPCNet can learn a mask optimization model without ground-truth OPC-corrected masks based on the proposed input-output consistency loss. Experimental results evidently demonstrate that, in the lithography simulation issue, our method is more appropriate than existing image-to-image translation schemes and outperforms the standard compact model-based simulations. In the mask optimization problem, OPCNet can correctly predict the mask that its lithography simulation image is close to the expected layout. One on-going extension of this work is to establish a scoring system, based on the deformation map or SEM-styled image derived by our method, so that a virtual metrology system for IC circuit layout quality assessment can be developed.

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Fig. 14. Prediction results of LithoNet: (a) Comparison between a layout and the prediction based on the layout, and (b) conceptual illustration of Necking and Rounding where the necking effects are highlighted by red boxes and arrows and the rounding effects are indicated by blue arrows.

Fig. 15. Illustrations of masks predicted by the mask generator and their lithography simulation outputs.

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