Coding Scheme for 3D Vertical Flash Memory

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Abstract—Recently introduced 3D vertical flash memory is expected to be a disruptive technology since it overcomes scaling challenges of conventional 2D planar flash memory by stacking up cells in the vertical direction. However, 3D vertical flash memory suffers from a new problem known as fast detrapping, which is a rapid charge loss problem. In this paper, we propose a scheme to compensate the effect of fast detrapping by intentional inter-cell interference (ICI). In order to properly control the intentional ICI, our scheme relies on a coding technique that incorporates the side information of fast detrapping during the encoding stage. This technique is closely connected to the well-known problem of coding in a memory with defective cells. Numerical results show that the proposed scheme can effectively address the problem of fast detrapping.

I. INTRODUCTION

Aggressive scaling down of the device dimension has driven the continuous growth of flash memory density. However, the scaling down leads to many challenges such as photolithography limitation, increased intercell interference (ICI), and disturbance [1], [2]. In order to overcome these scaling challenges, a paradigm shift from the 2-dimensional (2D) planar structure to the 3D vertical structure is underway. The change is stacking up cells in the vertical direction instead of shrinking cells within a 2D plane [2–5].

The recent 3D vertical NAND flash memory with 24 word-line (WL) shows better device characteristics compared to 2D 1x nm planar flash memory [5]. However, 3D vertical flash memory has a problem of fast detrapping, which is a quick charge loss phenomenon resulting in larger threshold voltage variations in programmed cells [5, 6].

The fast detrapping usually occurs in charge trap cells rather than floating gate cells [5, 6]. Since 3D vertical flash memory uses charge trap cells such as damascened metal-gate silicon-oxide-nitride-oxide-silicon (SONOS) cell for easier 3D integration [1–5], fast detrapping is an important problem of 3D vertical flash memory. On the other hand, the fast detrapping does not happen in 2D planar flash memory consisting of floating gate cells.

In order to cope with fast detrapping, several approaches have been proposed. These approaches include cell structure engineering at device level and reprogramming at circuit level [5, 6]. In this paper, we try to combat the fast detrapping at coding level. The basic idea is to compensate the charge loss due to fast detrapping through intentional ICI. Although the ICI is a well-known adverse effect, it can be utilized to alleviate the effect of the fast detrapping through the proposed scheme. It is worth mentioning that the proposed scheme at coding level can cooperate with other approaches at different levels.

We will formulate the problem of controlling the intentional ICI into coding in a memory with defective cells model of [7], which is a notable example of coding with side information available at the encoder [8]. With this formulation, the additive encoding schemes in [9, 10] can be applied to control the intentional ICI.

Recently, coding schemes with the side information available at the encoder have drawn attention for phase change memories (PCM), write once memories (WOM), and flash memories [11–13]. In [11], the side information corresponding to the variability of PCM is used at the encoder to reduce the effect of variability. [12] assumes that the current state of the memory is known to the encoder for rewriting WOM. Also, the encoder exploits the side information corresponding to the ICI of flash memory and reduces the effect of the ICI in [13]. In this paper, the side information is related to the fast detrapping of 3D vertical flash memory, and coding with this side information controls the intentional ICI to compensate the fast detrapping.

Although the above coding schemes improve the reliability (i.e., decoding failure probability) by using the side information at the encoder, the write speed performance would be degraded during the obtaining of the side information and incorporating this side information into encoding. Note that soft decision decoding schemes such as low-density parity check (LDPC) codes in flash memory improve the decoding failure probability at the expense of decreased read speed due to multiple read operations needed to obtain soft decision values. Thus, we can claim that the coding schemes using side information at the encoder are complementary to the soft decision decoding schemes.

In memory systems, it is well-known that the read speed performance is more critical than the write speed performance since the write operation is typically not on the critical path because of write buffers in the memory hierarchy and the write latency can be hidden [11, 14]. Also, the read operations are required more often than the write operations in many memory applications. Thus, the coding schemes using side information at the encoder have an advantage over soft decision decoding from the perspective of speed performance compared to soft decision decoding.

The rest of this paper is organized as follows. Section II
threshold voltage distribution can be made tighter, however the write time increases [15], [17].

The positions of program states are determined by verify levels and the tightness of each program state depends on the incremental step voltage $\Delta V_{pp}$. By reducing $\Delta V_{pp}$, the threshold voltage distribution can be made tighter, however the write time increases [15], [17].
gate is formed as an electron storage layer upon single crystal planar silicon channel, the 3D vertical flash memory has a nitride layer inside oxide-nitride-oxide (ONO) stack which is grown as a charge trap layer along the circumference of the thin poly-silicon vertical channel. Note that each charge trap layer in this 3D vertical flash memory is surrounded by the metal gates along WL plane.

By taking into account the structure of 3D vertical flash memories, we will address the ICI of 3D vertical flash memories. In flash memory, the threshold voltage shift of one cell affects the threshold voltage of its adjacent cell because of the ICI. The ICI is mainly attributed to parasitic capacitances coupling effect between adjacent cells [18].

Suppose that \( V_{(i,j,k)} \) is the threshold voltage of \((i, j, k)\) cell which is situated at \(i\)-th WL, \(j\)-th BL, and \(k\)-th SSL as shown in Fig. 2. The threshold voltage shift \( \Delta_{ICI} V_{(i,j,k)} \) of the \((i, j, k)\) cell due to the ICI can be given by

\[
\Delta_{ICI} V_{(i,j,k)} = \gamma_{WL-to-WL} (\Delta V_{(i-1,j,k)} + \Delta V_{(i+1,j,k)}) \\
+ \gamma_{BL-to-BL} (\Delta V_{(i,j-1,k)} + \Delta V_{(i,j+1,k)}) \\
+ \gamma_{SSL-to-SSL} (\Delta V_{(i,j,k-1)} + \Delta V_{(i,j,k+1)})
\]

which is an extension of the ICI model of 2D planar flash memories in [18]. \( \Delta V_{(i\pm1,j\pm1,k\pm1)} \) in the right hand side represent the threshold voltage shifts of adjacent cells after the \((i, j, k)\) cell has been written. Note that \( \gamma_{WL-to-WL} \) is coupling ratio between WL plane and adjacent WL plane. Also, \( \gamma_{BL-to-BL} \) is coupling ratio between bit-line (BL) and adjacent BL. Finally, \( \gamma_{SSL-to-SSL} \) is coupling ratio between SSL group and its adjacent SSL group. It is worth mentioning that the diagonal ICIs are neglected since they are very small due to the longer distance between cells.

Since each charge trap layer in this 3D vertical flash memory is surrounded by the metal gates along WL plane, the ICI between adjacent BLs typically found in high density 2D planar flash memory is completely absent in the same WL plane. Similarly, the ICI between adjacent SSL groups will be negligible due to the metal gates.

The ICI between adjacent WL planes is also reduced compared to the conventional 2D planar flash memory since the charge trap layer in the 3D vertical flash memory is much thinner than the floating gate layer in the 2D flash memory. However, the ICI between adjacent WL planes increases as the distance between WL planes is reduced for the higher cell density. Thus, it is enough to take into account only the ICI between adjacent WL planes in the same SSL group and BL. By setting \( \gamma_{WL-to-WL} = \gamma_{BL-to-BL} = \gamma_{SSL-to-SSL} = 0 \), the ICI model of (1) will be simplified into

\[
\Delta_{ICI} V_{(i,j,k)} = \gamma (\Delta V_{(i-1,j,k)} + \Delta V_{(i+1,j,k)}).
\]

C. Fast Detrapping

As mentioned in [18], nitride charge trap layer is attractive for integration of the 3D vertical flash memory. However, the fast detrapping from this trap layer is a critical challenge in the 3D vertical flash memory [6].

Fig. 3. Fast detrapping and identifying cells that suffer from fast detrapping.

The cause of fast detrapping can be explained by shallowly trapped electrons in charge trap layers, which immediately detrap and tunnel out after the programming pulse is terminated [6]. Thus, the charge loss due to fast detrapping quickly decreases the threshold voltage of corresponding cells and degrades the threshold voltage distribution, as shown in Fig. 3(a) and 3(b). The fast detrapping occurs immediately after write operation, and is almost completed within 1 sec [6].

The device level approaches such as cell structure and material could not completely solve this problem [6]. In [5], a counter-pulse program using self-boosting was proposed in circuit level, which accelerates fast detrapping before a verify operation of ISP; such that fast detrapped cells can be reprogrammed by the subsequent programming pulses. Nevertheless, fast detrapping can happen again in the later programming pulses, which requires a different approach at higher levels such as coding level. Since the approaches at different levels can coexist, the proposed scheme at coding level can cooperate with other approaches at lower levels in combating fast detrapping.

D. Channel Model

A channel model of conventional 2D planar flash memories can be given by

\[
Y = X + S_{2D} + Z \quad (3)
\]

\[
= X + Z_{\text{write}} + S_{2D} + Z_{\text{read}} \quad (4)
\]

\[
= V + S_{2D} + Z_{\text{read}} \quad (5)
\]

where \( X \) and \( Y \) are the channel input and output. Also, \( S_{2D} \) represents the ICI from adjacent cells in the conventional 2D
planar flash memory. The additive random noise $Z$ is a sum of $Z_{\text{write}}$ and $Z_{\text{read}}$ where $Z_{\text{write}}$ is the write noise due to the initial threshold voltage distribution after erase operation and the incremental step voltage $\Delta V_{pp}$ of ISPP. $Z_{\text{read}}$ is the read noise due to other noise sources.

Since the write noise $Z_{\text{write}}$ precedes the ICI $S_{3D}$, we consider a random variable $V = X + Z_{\text{write}}$. The shifts of $V$ in adjacent cells determine the ICI $S_{3D}$. (3) and (4) come from the flash memory channel model in [13], [19]. The channel model of (3) was recently validated by experimental results from the 2x nm 2D planar flash memory in [19].

The 3D vertical flash memory channel model can be extended from the 2D planar flash memory channel model as follows.

\[
Y = V + S_{3D} + Z_{\text{read}} = V + S_{3D} + Z_{\text{fast}} + Z_{\text{random}}
\]

(6)

(7)

where $Z_{\text{read}} = Z_{\text{fast}} + Z_{\text{random}}$. $Z_{\text{fast}}$ denotes the noise due to fast detrapping. All the other read noise sources are represented by $Z_{\text{random}}$. In addition, the ICI of the 3D vertical flash memory is given by $S_{3D}$. Note that $S_{3D}$ of $(i,j,k)$ cell is the same as $\Delta ICI V_{(i,j,k)}$ of (1) and (2).

III. PROPOSED SCHEME

We propose a new scheme in coding level in order to overcome fast detrapping. Since the proposed scheme will be explained by the problem of coding with side information available at the encoder, we should address the following two questions.

- How does the encoder obtain the side information?
- How does the encoder use the side information?

We will address these two problems and propose the solutions in the following subsections.

A. HOW DOES THE ENCODER OBTAIN THE SIDE INFORMATION?

First, the encoder should obtain the side information corresponding to fast detrapping. Fig. 3(a) shows the threshold voltage distribution before fast detrapping happens. After writing the $i$-th WL, some of cells in the $i$-th WL immediately suffer from fast detrapping and their threshold voltages decrease as shown in Fig. 3(b).

The cells suffering from the fast detrapping can be identified by two read operations at the read level $\eta$ and the identify level $\zeta$, as shown in Fig. 3(c). If a cell’s threshold voltage is between $\eta$ and $\zeta$, we can claim that this cell suffers from fast detrapping and the encoder obtains the location of this cell, which is the side information about fast detrapping.

If the encoder holds the original data of the $i$-th WL, we can obtain this side information of fast detrapping by just one read operation since we do not need to apply the read operation at the read level $\eta$. By combining the original data and the binary data obtained from the read operation at the identify level $\zeta$, the encoder can identify the cells suffering from fast detrapping.

Note that the identify level $\zeta$ do not need to be the same as the verify level $v$. We can change the identify level $\zeta$ by taking into account the strength of fast detrapping. The number of identified cells depend on the identify level $\zeta$.

B. HOW DOES THE ENCODER USE THE SIDE INFORMATION?

Now the encoder knows the side information corresponding to fast detrapping in cells of the $i$-th WL. The side information represents the locations of identified cells, which suffer from fast detrapping. The next step is to use this side information during encoding.

The key idea is to compensate the effect of the fast detrapping in the $i$-th WL by controlling the intentional ICI from the $(i + 1)$-th WL. The intentional ICI can compensate the decrease of threshold voltage due to fast detrapping since the ICI increases the threshold voltage of the interfered cell. Note that fast detrapping results in charge loss, which decreases the corresponding cells’ threshold voltages.

Assume that a cell $C_{(i,j)}$ in Fig. 4 suffered from fast detrapping, which has been identified by the read operations as explained in [11]. If the upper cell $C_{(i+1,j)}$ in the $(i + 1)$-th WL is written into $S_1$, the ICI from $C_{(i,j)}$ will increase the threshold voltage of $C_{(i,j)}$ during increasing the threshold voltage of $C_{(i+1,j)}$ from $S_0$ to $S_1$. If $C_{(i+1,j)}$ is written into $S_0$, the threshold voltage of $C_{(i+1,j)}$ remains at the initial erase state $S_0$, so the ICI from $C_{(i+1,j)}$ is absent.

Thus, in order to compensate the effect of fast detrapping, the upper cell $C_{(i+1,j)}$ of the identified cell $C_{(i,j)}$ should be written into $S_1$ which is mapped into binary data “0” as shown.
in Fig. 3(a). We have to control the intentional ICI to alleviate the effect of fast detrapping.

We will formulate this problem of controlling the intentional ICI into coding in a memory with defective cells in [7]. The problem of coding in a memory with defective cells has been well studied in literature [7], [9], [20]. A binary memory cell is called defective if its cell value is stuck-at a particular value regardless of the channel input. As shown in Fig. 5 this channel model has the ternary state \( S \in \{0, 1, \lambda\} \), which will be the side information of defect. The state \( S = 0 \) corresponds to a stick-at 0 defect that always outputs a 0 independent of its input value, the state \( S = 1 \) corresponds to a stick-at 1 defect that always outputs a 1, and the state \( S = \lambda \) corresponds to a normal cell that can be modelled by a binary symmetric channel (BSC) with crossover probability \( p \). The probabilities of these states are \( P(S = 0) = \varepsilon_0 \), \( P(S = 1) = \varepsilon_1 \), and \( P(S = \lambda) = 1 - \varepsilon_0 - \varepsilon_1 \), respectively. Note that \( X \) and \( Y \) represent the channel input and output.

In order to solve the problem of coding in a memory with defective cells, Tsymbaik proposed additive encoding which masks defects by adding a carefully selected binary vector \([9]\). Masking defects is to make a codeword whose values at the locations of defects match the stuck-at values at those locations \([9], [21]\). The additive encoding is a capacity achieving scheme \([10], [22]\).

Since the cell \( C_{(i+1,j)} \) in Fig. 4 should store a binary 0 (i.e., \( S_1 \)) for the intentional ICI, we will regard this cell \( C_{(i+1,j)} \) as stick-at 0 defects. Then, the additive encoding tries to make the codeword’s element corresponding to the cell \( C_{(i+1,j)} \) become 0. After writing the additive encoded codeword into the \((i+1)\)-th WL, the ICI from the cell \( C_{(i+1,j)} \) increases the threshold voltage of the cell \( C_{(i,j)} \), which compensates the threshold voltage decrease of the cell \( C_{(i,j)} \) due to fast detrapping.

In summary, the encoder obtains the locations of identified cells which are suffering from fast detrapping in the \( i \)-th WL before writing the \((i+1)\)-th WL. These locations can be obtained by one or two read operations, which would degrade the write speed performance. For the intentional ICI, the upper cells in the \((i+1)\)-th WL of the identified cell in the \( i \)-th WL will be regarded as stuck-at 0 defects. Note that the side information of fast detrapping in the \( i \)-th WL will be changed into the side information of defects in the \((i+1)\)-th WL. Afterwards, we can harness the intentional ICI by a coding technique such as additive encoding.

### IV. Simulation Results

In this section, the simulation results are presented. The simulation parameters are summarized in Table I. The initial threshold voltage distribution (after erasing a flash memory block) is assumed to be the Gaussian distribution \( \mathcal{N} (-4, 1^2) \). The ISPP was implemented with the parameters of the verify level for \( S_1 \), i.e., \( \nu_{S_1} = 1 \) and the incremental step voltage \( \Delta V_{pp} = 1 \).

The noise due to fast detrapping \( Z_{fast} \) is assumed to be the Gaussian distribution \( \mathcal{N} (-0.2, \sigma_{Z_{fast}}^2) \) by taking into account experimental results in [6]. The random noise due to other read noise sources \( Z_{random} \) is assumed to be \( \mathcal{N} (0, \sigma_{Z_{random}}^2) \).

For the additive encoding, we use \([n = 1023, k = 923, l, r]\) partitioned Bose, Chaudhuri, Hocquenghemp (PBCH) codes where \( n, k, l, \) and \( r \) denote the codeword size, the information size, the redundancy size for masking defects, and the redundancy size for correcting random errors, respectively. The PBCH code is a special class of partitioned linear block codes, which can be designed by a similar method of standard BCH codes \([10]\). For the given \( n = 1023 \) and \( k = 923 \) (i.e., the total redundancy size is 100), all possible redundancy allocation candidates of PBCH codes are presented in Table II [23]. Note that \( l \) and \( r \) are multiples of 10 that is the degree of Galois field. For the efficient computation complexity, two-step encoding scheme of \([21], [23]\) has been used for encoding of PBCH codes.

Fig. 6 shows that controlling ICI by additive encoding can compensate the effect of fast detrapping. After compensating the fast detrapping by the intentional ICI, the threshold voltage distribution improves.

Fig. 7 shows that the probability of decoding failure

| Parameters | Values |
|------------|--------|
| Bits per cell | \( B = 1 \) (SLC) |
| Initial threshold voltage distribution | \( \mathcal{N} (-4, 1^2) \) |
| Verify level for \( S_1 \) | \( \nu_{S_1} = 1 \) |
| Incremental step voltage | \( \Delta V_{pp} = 1 \) |
| Coupling ratio \( \gamma \) of \( \mathcal{N} \) | 0.1 |
| \( Z_{fast} \) of \( \mathcal{N} \) | \( \mathcal{N} (-0.2, \sigma_{Z_{fast}}^2) \) |
| \( Z_{random} \) of \( \mathcal{N} \) | \( \mathcal{N} (0, \sigma_{Z_{random}}^2) \) |
| Read level | \( \eta = 0 \) |
| Identify level | \( \zeta \) |
| Additive encoding | \([n = 1023, k = 923, l, r]\) |

| PBCH Codes |

| Code | \( l \) | \( r \) | Notes |
|------|------|------|------|
| 0   | 0    | 100  | Only correcting random errors |
| 1   | 10   | 90   |  |
| 2   | 20   | 80   |  |
| 3   | 30   | 70   |  |
| 4   | 40   | 60   |  |
| 5   | 50   | 50   |  |
| 6   | 60   | 40   |  |
| 7   | 70   | 30   |  |
| 8   | 80   | 20   |  |
| 9   | 90   | 10   |  |
| 10  | 100  | Only masking defects |

| TABLE II |

| All Possible Redundancy Allocation Candidates of \([n = 1023, k = 923, l, r]\) PBCH Codes |

| Code | \( l \) | \( r \) | Notes |
|------|------|------|------|
| 0   | 0    | 100  | Only correcting random errors |
| 1   | 10   | 90   |  |
| 2   | 20   | 80   |  |
| 3   | 30   | 70   |  |
| 4   | 40   | 60   |  |
| 5   | 50   | 50   |  |
| 6   | 60   | 40   |  |
| 7   | 70   | 30   |  |
| 8   | 80   | 20   |  |
| 9   | 90   | 10   |  |
| 10  | 100  | Only masking defects |
Fig. 6. Comparison of threshold voltage distributions ($\sigma_{Z_{\text{int}}} = 0.4$, $\sigma_{Z_{\text{random}}} = 0.2$, $\zeta = 0.4$).

Fig. 7. $P(\text{decoding failure})$ for different identify levels $\zeta$ ($\sigma_{Z_{\text{int}}} = 0.4$, $\sigma_{Z_{\text{random}}} = 0.2$).

$P(\text{decoding failure})$ is improved by the proposed scheme. If the redundancy for masking $l$ is zero, it means that the side information of fast detrapping is ignored. Otherwise, the encoder uses the side information of fast detrapping to improve $P(\text{decoding failure})$. Note that $P(\text{decoding failure})$ depends on the identify level $\zeta$ since it controls the number of identified cells, which is equivalent to the number of cells identified as defects in the upper WL. Also, the optimal redundancy allocation ($l^*, r^*$) to minimize $P(\text{decoding failure})$ depends on the identify level $\zeta$. For larger $\zeta$, the number of cells identified as defects increases, which requires more redundancy for masking defects during additive encoding. For the given parameters in Fig. 7, the identify level of $\zeta = 0.2$ minimizes $P(\text{decoding failure})$.

Fig. 8 shows the improvement of $P(\text{decoding failure})$ by the proposed scheme for different levels of fast detrapping $Z_{\text{fast}}$. Note that $\sigma_{Z_{\text{int}}}$ changes from 0.2 to 0.5 for the given $\sigma_{Z_{\text{random}}} = 0.2$. From Fig. 8(a), we can obtain the optimal redundancy allocation ($l^*, r^*$) minimizing $P(\text{decoding failure})$. It is worth mentioning that the optimal redundancy for masking $l^*$ increases for larger $\sigma_{Z_{\text{int}}}$. This is because we should allot more redundancy for masking defects (i.e., compensating the fast detrapping) as $\sigma_{Z_{\text{int}}}$ increases.

Fig. 8(b) compares $P(\text{decoding failure})$ for $(l, r) = (0, 100)$, (i.e., coding without the side information of fast detrapping) and that for $(l^*, r^*)$ (i.e., coding with the side information of fast detrapping). By using the side information of fast detrapping, we can significantly improve $P(\text{decoding failure})$ for different $\sigma_{Z_{\text{int}}}$.

Fig. 9 shows the improvement of $P(\text{decoding failure})$ by the proposed coding scheme for different random noise $Z_{\text{random}}$. Note that $\sigma_{Z_{\text{random}}}$ changes from 0.2 to 0.3 for the given $\sigma_{Z_{\text{int}}} = 0.4$. From Fig. 9(a), we can obtain the optimal redundancy allocation ($l^*, r^*$) minimizing $P(\text{decoding failure})$. Fig. 9(b) compares $P(\text{decoding failure})$ for $(l, r) = (0, 100)$, (i.e., coding without the side information of fast detrapping) and that for $(l^*, r^*)$ (i.e., coding with the side information of fast detrapping). It is worth mentioning that the improvement of $P(\text{decoding failure})$ becomes significant as the fast detrapping $Z_{\text{fast}}$ dominates the random noise $Z_{\text{random}}$.

V. CONCLUSION

We proposed a scheme to compensate the effect of fast detrapping by intentional ICI. The main idea comes from the
ICI by using the side information of fast detrapping. Although can be extended to MLC flash memories. whereas fast detrapping decreases the threshold voltage of core-

Fig. 9. \( P(\text{decoding failure}) \) for different \( \sigma^2_{\text{random}} \) (i.e., not using any side information) and that for the optimal redundancy allocation \((l^*, r^*)\).

observation that ICI increases the threshold voltage of a cell whereas fast detrapping decreases the threshold voltage of corresponding cell. Additive encoding can control the intentional ICI by using the side information of fast detrapping. Although this paper focused on SLC flash memory, the proposed scheme can be extended to MLC flash memories.

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