Ultra-high-resolution printing of flexible organic thin-film transistors

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ABSTRACT

Fully printed electronics on plastic have attracted considerable interest owing to their high compatibility and ease of integration. Here, an ultra-high-resolution printing technique based on parallel vacuum ultraviolet patterning that can produce high-contrast wettability regions on flexible substrates was developed. This technique was used to selectively deposit a functional ink with a 1 µm feature size, thereby allowing the large-scale fabrication of organic thin-film transistors with channels as short as 1 µm under an ambient atmosphere. Moreover, in short-channel devices, hole injection barriers can be tuned by printing the optimum gate overlaps associated with selectively doping semiconductor/electrode interfaces, resulting in a marked reduction in contact resistance from 20 to 1.5 kΩ cm, and an elevation of the charge carrier mobility to a record high of 0.3 cm² V⁻¹ s⁻¹ in a 1-µm-channel device. The results indicate that the developed technique is promising for the fabrication of large-area, high-resolution, low-cost electronics.

KEYWORDS

Fully printed electronic; high-resolution electronic circuit; organic thin-film transistor; short channel; field effect mobility

1. Introduction

Shrinking device dimensions to the few-micron scale is the primary step in manufacturing high-resolution electronics. Particularly in the field of high-definition liquid crystal displays, thin-film transistors (TFTs) with channel lengths of no more than 5 µm are typically required. Large-area, short-channel TFTs are generally fabricated using photo or electron beam lithography for patterning [1,2], which are indeed highly developed methods but have poor efficiency and high cost. On the other hand, extensive studies on organic semiconductors exclusively point to the superiority of fully solution-based processes such as printing [3] or coating [4] for preparing organic OTFTs. These processes can be carried out under an ambient atmosphere and are typically applicable to flexible substrates.

Although various printing techniques have been proposed to fabricate OTFTs, such as inkjet printing [5], gravure [6], and aerosol jet printing [7], it is still a challenge to integrate short-channel OTFTs into a large-area array through facile printing techniques. For devices with channel lengths less than 10 µm, the short-channel effect highly dominates the device performance; thus, parameters such as series parasitic resistance, channel length, apparent threshold voltage, and apparent field effect mobility (μFET) are taken into account in constructing the model. In particular, the problem of how to enhance the mobility while minimizing the short-channel effect is even more intractable. For example, 5-µm-channel polymer OTFTs prepared via inkjet printing exhibited a field effect mobility of 0.02 cm² V⁻¹ s⁻¹ [5], whereas when the channels were further downscaled to hundreds of nanometers, much lower μFET values ranging from 0.001 to 0.005 cm² V⁻¹ s⁻¹ were observed [8]. The undesired slowdown of charge carrier transport as well as the low on/off ratio of 10²–10³ in short-channel OTFTs is pervasive due not only to the variation of the topological parameters but also to the parasitic contact resistance. Therefore, achieving competitive electrical properties in short-channel devices requires the reduction of the contact resistance by modifying the device architecture and/or semiconductor/electrode interface through a solution-based method. In addition, it is essential to construct ultra-thin discrete organic semiconducting islands with well-oriented crystals for lowering the off-state current and suppressing the crosstalk effect between adjacent devices.

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Reported in this article is a pioneering high-resolution printing technique based on the parallel vacuum ultraviolet (PVUV) technique with \( \pi \)-junction Au nanoparticle (AuNP) ink, which enables the room-temperature fabrication of large-scale, high-resolution electronic circuits on flexible substrates. The results revealed that a series of Au lines and gaps with widths down to 1 \( \mu \)m can be prepared via solution-based printing, which offers a higher resolution than the conventional photolithography. Moreover, the present technique was developed to fabricate short-channel OTFTs in large-area arrays on plastic substrates. In particular, employing room-temperature processes throughout the fabrication prevented the undesired distortion of the substrate due to thermal annealing, which allowed the fabrication of fully printed devices with ultra-high accuracy even on a heat-sensitive flexible substrate. To obtain high performance in short-channel devices, the optimum gate overlap length was printed with high precision, in combination with the controllable modification of the metal/organic semiconductor interface via fully solution-based processes to reduce the contact resistance to 1.5 k\( \Omega \) cm, which is an order of magnitude lower than that in unoptimized devices. As a result, the \( \mu \)FET was enhanced to as high as 0.3 cm\(^2\) V\(^{-1}\) s\(^{-1}\) in the 1-\( \mu \)m-channel OTFTs, which, to the best of the authors’ knowledge, is a record-high value.

2. Experiment

A system using a vacuum ultraviolet (VUV) light source in printing AuNP inks [9] into electronic circuits at room temperature was established [10]. The exposure of the surfaces of the hydrophobic self-assembled monolayers [11] or polymers [12] by VUV makes such surfaces hydrophilic, followed by the application of Au ink, resulting in the patterned Au electrodes shown in Figure 1(a). The irradiation procedure was commonly carried out by the conventional diffusive VUV system with a tube light (Figure 1(b)). In such a system, once the gap width of the photomask decreases to dozens of microns, the obtained patterns exhibit rough shapes, with undesired expansion or constriction in the sidelines and corners. This is because the VUV rays are emitted divergently from the source, and as a consequence, the diffusive rays expose areas wider than the gaps in the mask. To overcome such limitations in the printing of narrow lines and gaps and to achieve high accuracy, the PVUV source was explored for high-resolution patterning. A spotlight was fixed at the focal point of a parabolic mirror so that the light would be reflected by the parabolic reflector to generate parallel incident rays with high-directivity beams irradiated straight onto the substrate surfaces, thus minimizing the expansion of the exposed areas, as illustrated in Figure 1(c).

Source/drain contacts and semiconductor, gate dielectric, and gate electrode layers (Figure 2) were deposited to fabricate short-channel OTFTs at a large scale (77 devices in 2 \( \times \) 2 cm\(^2\) sizes). It can be seen from the image in a scanning electron microscope that the precise printing of a 1-\( \mu \)m channel was realized, which exhibited only a slight deviation. The optical micrograph of a 1-\( \mu \)m-channel OTFT on plastic showed accurate stacking of all the components, indicating that this printing technique is feasible for the layer-by-layer assembly of multi-layered electronics. For the contact electrodes, various channel lengths \( (L) \) were achieved, from 1 to 50 \( \mu \)m. For the gate electrodes, the same printing method introduced earlier was used. An optical image of the gate electrodes clearly demonstrated the well-defined and sharp edges. The printed Au source, drain, and gate electrodes exhibited a uniform surface morphology with less than 10 nm roughness and where the coffee ring effects were negligible. As all the layers were quite thin, the OTFT arrays were highly flexible and transparent, as exhibited in Figure 2.

In addition, to print separate semiconducting thin-film crystals, a removable lyophobic guide layer screen-printed with Cytop solution to form rectangular active regions was employed. The bank depth could be precisely adjusted by varying the Cytop concentration; the as-purchased Cytop solution gave rise to a 500-nm-thick bank that surrounded the lyophilic regions and directed the deposition of the 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) solution. Moreover, the narrow banks were able to control the molecular orientation during the crystal growth, as reported [13], and enabled the incubation of large crystals with aligned domains crossing the channels. To suppress the ‘coffee stain’ effect and to form thin, uniform crystals, a mixture consisting of a solvent with low surface tension (anisole) and an antisolvent with high surface tension (DMF) was typically used for semiconductor deposition [14]. As the solvent evaporated, crystal nuclei initially appeared near the upper surface of the droplets owing to the concentration gradient, followed by the formation of ultra-thin organic thin films in the bank regions. After the complete evaporation of the solvent, the Cytop guide layer could be washed away by the Cytop solvent while the thin-film island array stayed in situ, as shown in Figure 2. Compared with the other strategies used to fabricate organic thin-film islands [14], the process described herein is capable of producing ultra-thin and well-aligned crystalline films. For the top-gate dielectric, a parylene layer was used because it is crosslinked and has high VUV light absorbance and can thus prevent the destruction of the
active layer. The optimal film thickness of parylene and C8-BTBT were found to be 100 and 50 nm, respectively. A detailed investigation of the effect of the film thickness showed that the thicker parylene and C8-BTBT layers resulted in lower-performance devices.

3. Results and discussion

The transfer characteristics of three typical devices with 1, 5, and 30 μm channel lengths, respectively, are shown in Figure 3(a). As the channel length was decreased, the saturation currents increased with the elevated off-state as a result of the short-channel effect [15]. Indeed, the $\mu_{FE}$ of the 1-μm-channel device reached 0.1 cm² V⁻¹ s⁻¹ while that of the 5-μm-channel device exceeded 0.5 cm² V⁻¹ s⁻¹. A dramatic increase in mobility accompanied by a decrease in threshold voltage ($V_{th}$) can be clearly seen from 1 to 50 μm in Figure 3(b), which reveals that the charge carrier transport was strongly limited by contact injection [16], especially in the short-channel devices. This effect became minimal when the channel length increased up to beyond 40 μm, where both the saturation mobility and the threshold voltages approached constant values (3.5 cm² V⁻¹ s⁻¹ and 0.8 V, respectively). In the following, two approaches will be tried to reduce the contact resistance so as to achieve
higher mobility in short-channel OTFTs: (i) controlling the gate overlaps and (ii) inserting dopant layers in the contact interface by printing.

Based on the precise printing technique, an OTFT array with various gate overlap lengths (denoted as ‘op’) was printed to determine the effect of the gate overlap length on the contact injection, and to optimize the device performance. The evolution of the transfer characteristics of the short-channel devices (3 μm) with varied op is shown in Figure 3(c). An increase in op brought about higher saturation currents and negative on-voltage ($V_{on}$) but did not lead to remarkable changes in the threshold voltages ($V_{th}$) and off-state current ($I_{off}$). As a result, the effective mobility was enhanced from 0.33 to 0.85 cm² V⁻¹ s⁻¹. Apparently, upon the expansion of the contact areas, more charges were injected into the organic films to form conduction. To quantify the effect, the total resistance normalized to the channel width ($R_{tot}$ W) was plotted against the channel length ($L_t$) to extract the contact resistance ($R_c$ W) through the transmission line method [17]. As shown in Figure 3(d), the extracted $R_c$ W remarkably decreased from the initial 20 kΩ cm at $op = 5$ μm to 2.7 kΩ cm at $op = 20$ μm, almost 7 times smaller. The results indicate that the contact injection was non-ohmic, and that there was a large-spatial injection barrier at the interface, through which the injection was via Schottky tunneling. The injection barrier could be narrowed by a sufficient gate field given by gate overlapping [18], and so that the injection would be enhanced. Based on this mechanism,
the OTFT performance was simulated with varied $op$, and the device parameters were measured in the experiments and were tuned only to two free parameters: the work function of the Au electrodes and the semiconductor mobility. The best fitting to the experiment results is shown in Figure 3(d), when the work function of gold was 4.69 eV and the semiconductor mobility was $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which are consistent with the values obtained from the measurements. The above results illustrate that a highly accurate printing and patterning technique can control the gate overlap length to reduce $R_c$. Also, the OTFT performance will be further enhanced if the injection barrier at the contact will be reduced.

To further enhance the injection efficiency, solution-processed MoO$_3$ was employed as a dopant layer. The transition metal oxides are well-known p-type dopants for organic electronics due to their appropriate ionization energy of 5.6 eV and their ability to dope organic semiconductors to enhance the hole injection [19]. More importantly, they can dissolve in water even if the 500 mg L$^{-1}$ saturation concentration is quite low, which allowed the preparation of an aqueous MoO$_3$ solution. The aqueous MoO$_3$ (99.5%, Sigma-Aldrich) dopant solution was used for coating with a blade moving along the channel direction (Figure 4(a)). In detail, the aqueous MoO$_3$ solution moved with a tail on the AuNP electrodes, and indeed left a thin solution film covering the electrode surface, as revealed by the real-time optical images in Figure 4(b). The process took full advantage of the wettability contrast between the source/drain and the substrate surface, where the solution was repelled by the hydrophobic regions and was adsorbed by the hydrophilic regions. Consequently, a thin MoO$_3$ film was selectively deposited onto the Au electrodes; furthermore, the film thickness could be easily controlled by changing the solution concentration and/or shearing speed.

Compared to the undoped device, the 1-μm-channel OTFT with an MoO$_3$ layer exhibited threefold higher saturated mobility, reaching $0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, representing the record value for printed short-channel OTFTs (Figure 4(c)). This enhancement can also be observed in the output curves in Figure 4(e), which show a significant increase in the saturation current in the doped devices. It was noted that the off-state current was slightly higher than that of the undoped device, probably due to the fact that the carrier concentration near the contact was increased by the dopant, and so that the charge injection would become easier. In devices with long channels, the increase trend of the charge carrier mobility obviously slows down due to the dominative bulk resistance. A quantitative analysis via TLM revealed that the enhanced hole injection by the MoO$_3$ interlayer significantly lowered the value of $R_cW$ to $1.5 \text{k}\Omega \text{ cm}$ (with 20 μm $op$, as shown in Table 1). In total, the contact resistance in the gate electrodes and dopant layers was reduced to about 7% of the original value by the developed sufficient printing technique.

4. Conclusion

In conclusion, using a PVUV patterning system associated with AuNP ink, the room-temperature printing of narrow Au lines and gaps down to 1 micron in size...
and the printing of short-channel OTFTs on a large scale were achieved. In particular, discrete organic semiconducting thin films were fabricated with the assistance of a removable guide layer, which produced 20- to 50-nm thin films with aligned crystal domains, minimizing the bulk resistance. Moreover, gate electrodes with various widths were printed out with high precision to determine the effect of gate overlap on the device performance, and the results indicated that a medium overlap of 20 μm could play significant roles. Based on this optimized condition, the further enhancement of the charge carrier transport was investigated by selectively locating an aqueous MoO3 solution onto the surfaces of source and drain electrodes, which ultimately resulted in a sufficiently low contact resistance of 1.5 kΩ cm and a high mobility of 0.3 cm² V⁻¹ s⁻¹. This room-temperature printing strategy for high-resolution electronics combined with the practical doping method will be promising in the field of lithography-free, large-area, and high-resolution flexible devices.

**Disclosure statement**

No potential conflict of interest was reported by the authors.

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