Abstract—The control logic models built by Simulink or Ptolemy have been widely used in industry scenes. It is an urgent need to ensure the safety and security of the control logic models. Test case generation technologies are widely used to ensure the safety and security. State-of-the-art model testing tools employ model checking techniques or search-based methods to generate test cases. Traditional search based techniques based on Simulink simulation are plagued by problems such as low speed and high overhead. Traditional model checking techniques such as symbolic execution have limited performance when dealing with nonlinear elements and complex loops. Recently, coverage guided fuzzing technologies are known to be effective for test case generation, due to their high efficiency and impressive effects over complex branches of loops.

In this paper, we apply fuzzing methods to improve model testing and demonstrate the effectiveness. The fuzzing methods aim to cover more program branches by mutating valuable seeds. Inspired by this feature, we propose a novel integration technology SPSCGF, which leverages bounded model checking for symbolic execution to generate test cases as initial seeds and then conduct fuzzing based upon these worthy seeds. In this manner, our work combines the advantages of the model checking methods and fuzzing techniques in a novel way. Since the control logic models always receive signal inputs, we specifically design novel mutation operators for signals to improve the existing fuzzing method in model testing. The evaluated benchmarks which consist of industrial cases, SPSCGF could achieve 8% to 38% higher model coverage and 3x-10x time efficiency compared with the state-of-the-art works.

Index Terms—model testing, model verification, fuzzing

I. INTRODUCTION

MATLAB Simulink [1] is the most widely used modelling tool, which supports physical simulation, automatic code generation, formal verification and continuous testing for complex control systems. It has also been widely deployed in a number of domains, such as biotechnology, chemical industry, finance, and so on. After modelling the physical world by Simulink, engineers need to check the model to find possible safety or security problems. The automatic test generation and verification technologies based on Simulink have been proposed to help engineers to achieve their goals. Although existing state-of-the-art methods achieved considerable performance in small or medium scenarios, they still face certain challenges when deployed to complex industrial cases.

Simulink models are highly complex, they may contain a large number of blocks and hierarchy levels. In large industrial cases, the resulting Simulink models often consist of more than ten thousand blocks and hundreds of hierarchy levels. This exposes hard problems for model testing and validation. The execution of the Simulink model is not only time driven, but also event driven [2]. The time-event mixed computing makes the testing and validation even harder. For model verification methods, they always suffer from the state space explosion problem, making them nearly impossible to be applied to complex industrial models. Recently, search-based model testing methods have become popular techniques to find safety and security matters. They are light-weight and effective, capable to discover various kinds of deep-in-hiding bugs when combined with bug detection algorithms.

Among tools based on verification methods [3], [4], [5], [6], [7], [8], the most grinding one is Simulink Design Verifier [8]. Simulink Design Verifier converts the Simulink model into a linear hybrid system [9] and uses formal methods to analyze that system. The test case generation functionality of Simulink Design Verifier cannot handle nonlinear elements. If a cycle exists in Stateflow chart or an integrator exists in Simulink model, Simulink Design Verifier will fail and the semi-finished coverage report will be given. But for linear elements, Simulink Design Verifier can achieve very good results. As for search-based model testing tools [10], [11], [12], [13], [14], [15], [16], [17], they basically define fitness value according to the testing objective and leverage genetic algorithms to search for test cases with highest fitness value. Existing available tools are based on Simulink simulation which requires additional overhead and does not support parallel execution. These tools have serious efficiency problems when applied to large industrial cases. Recently, coverage guided fuzzing methods are proposed not only to achieve high coverage but also to test the model in pressure to discover possible defects. The fuzzing methods are extremely fast. Tens of thousands of inputs can be generated and executed in a second. In this paper, we try to apply the coverage guided fuzzing methods to model testing and combine the traditional bounded model checking methods together.

The fuzzing method was originally used for source code testing. To use that method in model testing, the model is transferred to the source code first and the fuzzing method is applied to the code of the model. But employing fuzzing techniques for model testing still requires adaptations. The main reason is that the inputs of a control logic model are usually signals, and generating a legal signal is not straightfor-
ward. Figure 1 gives an example about the commonly appeared signals in Simulink models. Traditional model checking techniques leverage the symbolic execution to generate the signal value in each time step, which is time consuming especially when the total time step number is large. Fuzzing techniques randomly choose predefined mutation operators to generate the signal value at each time step. These techniques often lead to irregular signal waves. The irregular signal waves make the final coverage unsatisfactory. Thus, traditional source code testing techniques need to be improved. To improve the effectiveness of the fuzzing method, based on original mutation operators of fuzzing methods, we summarize the commonly used signal patterns and design mutation operators to mutate signal data more efficiently.

In this paper, we put forward a novel model testing framework SPsCGF, which is composed of two stages. The first stage is to use bounded model checking to collect and solve all path constraints in the control logic to generate initial test cases. The loop in the control logic is expanded a finite number of times. The second stage is to use coverage guided fuzzing techniques to mutate the initial test cases in the first stage to cover the uncovered branches. The guided fuzzing methods not only explore the program paths as many as possible but also explore the extreme boundary conditions of the program to ensure the safety and security. Through the two stages, we combine the advantages of existing bounded model checking methods and fuzzing methods together. The framework reveals a lightweight test case generation method.

The experiments prove the effectiveness of the proposed framework. Compared with tools based on formal verification methods such as Simulink Design Verifier, the framework can handle nonlinear elements which are not fully supported by Simulink Design Verifier. When a model contains complex embedded code, the framework performs better. Compared with tools based on search based methods, the fuzzing method performs 3x-10x faster. The main reason for the efficiency improvement is that existing search based tools are based on Simulink simulation while the proposed framework is based on raw code execution. The Simulink simulation requires additional overhead compared with raw code execution, and does not support parallel execution. According to experiments, the proposed framework can achieve 8% to 38% coverage improvement compared to state-of-art tools. Our contributions are as follows:

1) We developed SPsCGF, an integration method which integrates the bounded model checking method and coverage guided fuzzing method together to generate test cases for models with signal inputs. In coverage guided fuzzing modules, SPsCGF takes signal patterns into consideration to improve the mutation operators of fuzzing methods. We have implemented SPsCGF as a standalone application. The SPsCGF relies on the existing state-of-the-art model checking tool CBMC [18] as well as AFL [19], a state-of-the-art, open source coverage guided fuzzing framework.

2) We compared SPsCGF with two state-of-art baselines to assess the effectiveness and efficiency of the proposed testing method. Our experiments, performed on 12 publicly-available Simulink models from the commonly used benchmarks and industry cases, show that, on average, SPsCGF achieves 8% to 38% more coverage and performs 3x to 10x faster than state-of-art baselines.

3) We evaluated the usefulness and the applicability of SPsCGF in real large industrial CPS models from the vehicle control domain. Those models are real industry models from our industrial partner. Those models have different formats and run under different environments. SPsCGF successfully tests those models and achieves high coverage.

![Fig. 1: Signal Example](image-url)

II. MODEL TESTING WITH TIME SERIES DATA INPUT

In this section, we describe the difference between traditional source code testing and model testing. Then, we formulate the problems. We use a real case to show the difficulties about testing Simulink models with time series data inputs. This explains why we need to specially design mutation operators based on signal patterns in fuzzing.

Take a model which simulates the forced shutdown of an electronic device in automobile as an example to show why models with time series data inputs are difficult to test. The model is shown in Figure 2. This model is a simple molecular model of the original big embedded model which is actually used in industrial scene. We intercept the small core part to show its key control logic. In Figure 2, the input $u$ represents the signal about button pressing down, the input $Tset$ indicates how long the electronic device will be forced to shut down after the shutdown key is pressed and held. At each time the input signal arrives, the $ONDLC$ module is responsible for generating the output signal. The output signal of the model will be used as the input of the model in the next round. The core logic of $ONDLC$ is also given in Figure 2 (b). If the input signal $u$ at current time is 10, the counter will increase by 1, otherwise the counter will be reset to 0. If the accumulated value of the counter in the past time reaches the threshold specified by $Tset$ port, the output signal will be true and shows that the electronic device will be forced to shut down, otherwise, the output signal remains false.

Although this logic is simple and clear, but this control logic cannot be directly solved by symbolic execution as the impact of $u$ to the final output is indirect. The symbolic execution...
can only solve the constraint \( u = 10 \) at each time step. If the number of total time steps is \( n \), the symbolic execution will produce \( 2^n \) results. However, only one kind of results in total \( 2^n \) results can make the final output to be true. That is, \( u \) keeps being 10 for \( N \) (specified by \( Tset \)) time steps and is set to 0 for other time steps. For bounded model checking, the loops are only expanded for a finite number of times. If \( n \) is larger than the number of expanding times, bounded model checking cannot give useful results. This core model is only a part of the original big embedded model. Things become more complicated if we consider the original big embedded model. If the taint analysis technique in search based test generation is used, it will find that each \( u \) in each time step has influences for the final results. Thus, those techniques still cannot efficiently generate test cases for models with signals as inputs. For models which receive curve signals, traditional testing techniques perform much worse. Thus, it is necessary to handle signals specially.

III. OVERALL FRAMEWORK

Figure 3 shows the overall workflow chart. Given a Simulink model, as shown in Figure 3, there are four steps to test that model. In the first step, the model is translated into code. The code format is C++. To be compatible with Simulink and Ptolemy, in this step, actually, the model is translated into an intermediate representation (IR). This IR is an intermediate model representation which contains both Simulink and Ptolemy semantics. Then, we design a code generator which generates C++ code based on IR. Note that this IR can directly contain source code. For complex Simulink elements, we directly put the code of those elements into IR. In the second step, based on the C/C++ code, the initial test cases are generated. The tool uses bounded model checking to do symbolic execution to generate test cases. The detailed components about initial test case generation are shown in the left part of Figure 4. The third step is to do coverage guided fuzzing. The detailed components about coverage guided fuzzing are shown in the right part of Figure 4. The last step is to measure the generated test cases and update the test case pool. The details are described in the following paragraphs.

/*
 * ONDLC is a Simulink S-Function.
 */
function y = ONDLC(u, old, set)
    if (u == 10)
        if old < set
            y(1) = false;
            y(2) = old + 1;
        else
            y(1) = true;
            y(2) = old;
        end
    else
        y(1) = false;
        y(2) = 0;
    end
end

(b) code of ONDLC in model

Fig. 2: Model Example with Signal Input

In the steps just described, the initial test case generation module and the coverage guided fuzzing module are two core modules of the proposed testing framework. As shown in Figure 3 when generating initial test cases, we not only use bounded model checking to do symbolic execution, but also use n-wise algorithm to generate test inputs. The n-wise algorithm ensures that all combinations of all possible values of n ports must exist in the test cases. This algorithm is expensive, so it is only applied on constant ports. After generating initial test cases, we put the generated test cases into a test case pool. The coverage guided fuzzing selects a test case from the test case pool at each time and mutates that test case for multiple rounds to generate new test cases.

The remaining subsections correspond to the four steps in the workflow chart in Figure 3 one by one. The technical details including the algorithms and the important implementation tricks are described in the following subsections.
Based on IR, we implement a code generator which generates runnable code. The code generator is also responsible for generating the test driver for bounded model checking and coverage guided fuzzing. The IR can directly contain source code. For complex Simulink models, we cannot easily translate those models into IR, thus, we directly use Simulink Coder to generate code and include the code in IR. The libraries used by the code are also added to IR. The self implemented code generator generates code based on IR.

```c
/* Model code and CBMC driver. */
// input data for one time step.
int in1[1];
int in2[1];
int out1[1];
// set up symbols for symbolic execution.
*(int*) in1+0 = nondet_int();
__CPROVER_input("int", *((int*) in2+1));
*(int*) in2+1 = nondet_int();
__CPROVER_input("int", *((int*) in2+1));
// target function code.
AddFunc(in1[0],in2[0],&(out1[0]));
```

(a) IR to C with Test Driver for CBMC

```c
/* Model code and Fuzzing driver. */
// inputs generated by fuzzing engine.
byte buffer[bufLen];
// input data for one time step.
int in1[1];
int in2[1];
int out1[1];
// assign buffer data to each port.
memcpy(in1, buffer + 0, 4);
memcpy(in2, buffer + 4, 4);
// target function code.
AddFunc(in1[0],in2[0],&(out1[0]));
```

(b) IR to C++ Code with Test Driver for Fuzzing

Figure 5 shows a simple Simulink model and its corresponding IR. Figure 6 shows the corresponding C/C++ code for the IR in Figure 5. The new work we do in code generator is to generate test drivers for two main modules of the proposed framework: the bounded model checking and coverage guided fuzzing. For bounded model checking, the test driver is responsible for assigning the symbol indicator to variables corresponding to input ports so that the bounded model checking tool CBMC can recognize the symbol indicator to do symbolic execution. CBMC can only handle C code so the test driver for CBMC is in strict C format. For fuzzing, the existing fuzzing tool only accepts a byte buffer as a test case. Thus, the test case in our fuzzing module is also a byte buffer. We splice the data of all input ports into a byte buffer. The position and
length of each port data in that buffer are recorded. After a test case (byte buffer) is generated, the test driver is responsible for assigning values in the byte buffer to variables corresponding to input ports. After the value assignment, functions which use those variables can run properly. Figure 6 shows how the test drivers assign the symbol indicators to the input ports.

In Figure 6 (a), the functions nondet_int and _CPROVER_input are CBMC utility functions which are responsible for registering symbols in CBMC symbolic executor. The nondet_int function is responsible for marking which data is the symbol. The _CPROVER_input function is just to provide some additional comments and explanations for the data which is marked by nondet_int function. The example only shows the data in one time step for simplicity. The in1, in2 are two input ports of model and out1 is the output port. After marking in1 and in2 as symbols, the next step is just to pass in in1 and in2 as parameters of function AddActor corresponding to the model logic. In Figure 6 (b), the buffer is the test case generated by fuzzing engine. How to generate this data will be described in the following section. The driver assigns the data in the buffer to each port using memcpy function.

B. Initial Test Case Generation

Based on the driver for CBMC, we can directly use CBMC to do symbolic execution to get the desired test cases. The CBMC tool not only generates test cases aimed for statement coverage or branch coverage, but also generates test cases aimed for modified condition/decision coverage (MC/DC) coverage. By using CBMC, a large amount of workloads can be reduced. However, only using CBMC to generate test cases is not enough. Looking back at the motivation example model mentioned in Figure 2 even for the model without nonlinear elements or external library dependencies, the symbolic execution cannot solve the branches which have indirect impacts on the input ports. If the model contains nonlinear elements, there is a high probability that the symbolic executor will not generate any test case. If the model contains arithmetic components that involve float-point numbers, there are also probabilities that the symbolic executor cannot solve the constraint. In extreme cases, CBMC may generate only one or two test cases if the model is not suitable for bounded model checking. In this situation, the fuzzing method plays an important role for the coverage improvement.

Some ports are not signals but only constant values. For those input ports or parameters, if the candidate values are given, we use n-wise algorithm to generate the combination of values of ports. In actual industrial scenario, the company will force such n-wise testing. The n-wise algorithm ensures that the value combinations of every n ports must appear in the test cases. We figure out a fast algorithm which is based on dynamic programming. Algorithm 1 uses a recursive function FastNWise to show the details. The symbol \( \times \) in Algorithm 1 is the Cartesian product. Assume each element in a set is a list. If an element is a single value, it is taken as a list containing that single value. The Cartesian product of such two sets still produces a set which consists of lists. The FastNWise in Algorithm 1 accepts two parameters. The first parameter is \( n \) of n-wise. The second parameter is the index of the constant port. For constant ports, we give them index from 0 to \( k \). The \( k+1 \) is the total number of constant ports. The return value of FastNWise(n, k) is the desired all n-wise combinations.

\[
\text{FastNWise}(n, k) \quad \text{return value of FastNWise}(n, k) \quad \text{algorithm is fast. After generating initial test cases, we put those generated test cases into a test case pool which will be used in fuzzing.}
\]

**Algorithm 1 FastNWise(n, portIndex)**

**Require:** two parameters;
1: n is the desired n-wise;
2: portIndex is the relative index of all constant ports;

**Ensure:** the test cases \( C_n \) which satisfy n-wise;
3: S = all constant values of port at portIndex;
4: a = randomly select an element in S;
5: \( R = S - a \);
6: \( P_n = \{a\} \times \text{FastNWise}(n, \text{portIndex}-1) \);
7: \( Q_n = R \times \text{FastNWise}(n-1, \text{portIndex}-1) \);
8: \( C_n = P_n \cup Q_n \);
9: return \( C_n \);

C. Coverage Guided Fuzzing

We maintain a test case pool which was initially filled in test cases generated by previous subsection. With the test case pool, in each fuzzing turn, we select a test case which is also named as seed from the test case pool. The seed selection algorithm takes the selection times of a seed and the execution times of half flipped conditions in a seed into consideration. The details are described in Algorithm 2.

The function SelectTimes in Algorithm 2 returns the number of times the test case is selected for fuzzing. The function ExecTimes is responsible for returning the execution times of a half flipped condition in all test case executions. If the True state of a condition is covered while the False state is not covered, this condition is the half flipped condition. If the False state of a condition is covered while the True state is not covered, this condition is also the half flipped condition. Existing methods often guide testing using distance to uncovered branches, this guidance is not enough because in many cases, a branch (also named as decision) contains two or more conditions. Only considering branches will lose information of conditions in a branch. Thus, we use conditions to guide the testing. The basic idea of selecting a seed in
Algorithm 2 SeedSelect(pool)

Require: one parameter:
1: pool is the test case pool;
Ensure: one suitable test case;
2: distribute = [];
3: for each case ∈ pool do
4:     prob = \frac{\text{SelectTimes}(\text{case})}{\text{ExecTimes}(\text{condition})};
5:     prob2 = 0;
6:     counter = 0;
7:     for condition ∈ half flipped conditions do
8:         prob2 += \frac{1}{1+\text{ExecTimes}(\text{condition})};
9:         counter++;
10:     end for
11:     case_prob = prob * (prob2 / counter);
12:     distribute.append(case_prob);
13: end for
14: index = \text{Sample}(\text{distribute});
15: return index_th test case in pool;

After selecting a seed, that seed will be mutated for multiple times. The mutations fall into two categories: traditional mutation and time series data mutation. The traditional mutation inherits from mutation operators in AFL. The time series data mutation is designed to generate square or curve shaped input signal. The two categories of mutations are defined as follows.

Traditional Mutation. The traditional mutations contain RandomSet mutation, BitFlip mutation, Math mutation and Havoc mutation. The details of are described as follows.

1) RandomSet. This mutation randomly chooses a number of positions and changes the values on those positions to another random values. The random values can be the mined constant values mentioned in previous subsections. The value ranges of ports are taken into consideration. If some positions in test input have the constraint of value ranges, we will randomly set values according to ranges.

2) BitFlip. This mutation flips test cases by bits. The smallest unit to bit flip is a byte. We flip n bytes at each time and n is a random number. For example, if we flip a byte in a test input, this makes the original test input byte from 01110001 to 10001110. The non-deterministic mutation randomly selects bytes for flipping. The deterministic mutation flips all bytes in a test input. We combine deterministic mutations and non-deterministic mutations together.

3) Math. This mutation randomly selects a number of positions in test input to do mathematical operations. The operations contain commonly used math operations such as add, subtract, multiply and divide. The operands are selected from 1 to a specified MAX value.

+ +1, +2, +3, +4, ..., + MAX
- -1, -2, -3, -4, ..., -MAX
* *2, *3, *4, ..., *MAX
/ /2, /3, /4, ..., /MAX

4) Havoc. This mutation is to destroy test cases as much as possible. The destruction includes setting some data in test input to specific extreme values such as −128 and 127 for a char type value, −32,768 and 32,767 for a short type value and so on. If the data type of the test input cannot be determined, some consecutive bytes of test input are randomly selected, and all bits in them are assigned 1 or 0. The destruction also includes swapping parts of a single test case and crossing over two test cases.

Time Series Data Mutation. The mutations for time series data divide into two categories: square signal mutation and curve signal mutation. The first one is responsible for generating histogram shape signals. The second one is responsible for generating curve shape signals. The details are as follows.

1) Square Signal Mutation. The square signal mutation does not strictly force the signal to be the shape of square. Instead, this mutation randomly chooses a continuous piece of data in test input and makes all the chosen data to be the same value. This mutation is applied when the inputs of some ports are time series data.

2) Curve Signal Mutation. The curve signal mutation randomly chooses a continuous piece of data and sets the data to the randomly generated continuous curve. The curve generating algorithm is as follows: result = \sum_{i=0}^{n} \sin(rand() * x + rand()) + \sum_{j=0}^{2} \cos(rand() * x + rand()). The generated curve will be randomly truncated to be the same length as the data chosen for mutation.

All above mutations are randomly chosen for one or multiple times when mutating a test case. This means that the final generated test case may be a complete square signal, a complete curve signal, or a combination of these two signals. The coverage of each newly generated test case will be recorded to determine whether to discard the test case and how to update the test case pool. This will be described in the following subsection.

D. Test Case Measure and Update

In this section, we describe how we instrument the code and measure test cases. We use three kinds of code coverage to measure test cases: model unit coverage, condition/decision coverage and modified condition/decision (MC/DC) coverage. Ptolemy and Simulink also allow users to insert custom C or C++ code into the model, the proposed method can also be applied to the general C or C++ source code. In our practice, we find that there are many difficulties in source code instrumentation. Some Boolean expressions may have side effects, for example, a < b +. The execution of this expression will affect the data in memory. This will cause problems if we use the traditional source code instrumentation method: each condition in a large decision in the source code is extracted separately in advance and assigned to a Boolean variable. Then, the result of the Boolean variable will be recorded. In most cases, the traditional source code instrumentation method works fine but it will fail when the Boolean expressions have short circuit characteristics. Take the Boolean expression c < d || a < b + as an example.
The $c < d$ is extracted as a variable and instrumented as
\texttt{bool b1 = c < d, record(b1)}. The $a < b++$ is extracted as a
variable and instrumented as \texttt{bool b2 = a < b++, record(b2)}.
The expression $c < d || a < b++$ is rewritten as $b1 || b2$.
Before executing $b1 || b2$, two expressions \texttt{bool b1 = c < d}
and \texttt{bool b2 = a < b++} have already been executed. However,
because of the short circuit characteristics of Boolean
expressions, if $c < d$ is true, $a < b++$ should not be
executed. Executing $a < b++$ will cause data inconsistency
between the original code and the instrumented code.
To overcome this problem, we design a novel lightweight source
code instrumentation method which can be applied to general
C or C++ source code to collect MC/DC coverage.

For MC/DC coverage, we use a novel technique to do instru-
mentation. To insert the instrumentation code to the Boolean
expression, we utilize the ternary operator. For each Boolean
expression $e$, we rewrite $e$ into $e ? \text{record(true, cond_index,}
de\text{c_index)} : \text{record(false, cond_index, dec_index)}$. The
\texttt{cond_index} is the condition index (described later) of
expression $e$. The \texttt{dec_index} is the decision index (described later)
of the decision expression (described later) containing
expression $e$; A Boolean expression $e$ must be either a decision
or a condition. A Boolean expression $e$ is a decision, meaning
that the Boolean expression $e$ is not contained by any other
Boolean expressions, otherwise, a Boolean expression $e$ is a
condition. For each decision, we assign a global index to that
decision. This index is referred to as \texttt{dec_index}. If a Boolean
expression $e$ is a decision, we give the condition index 0 to
that expression. For each child condition in a decision, we
assign an index (starts from 1) to that condition. This index is
referred to as \texttt{cond_index}. The condition index only considers
all conditions in a decision. The record function is defined
in Algorithm 3. By using Algorithm 3 Boolean result of a
decision and Boolean results of all conditions in that
decision can be recorded in a single integer and that integer is stored
in a slot of \texttt{bitmap} array.

\begin{algorithm}[h]
\caption{record(res, cond_index, dec_index)}
\begin{algorithmic}[1]
  \Require two parameters;
  \State res is the Boolean result of expression $e$;
  \State cond_index is the condition index of expression $e$;
  \State dec_index is the decision index of the expression contain-
  \State expression $e$;
  \Ensure record the result: res;
  \State $\text{bitmap[index]} | = res << \text{cond_index};$
  \State return res;
\end{algorithmic}
\end{algorithm}

Because the result of a Boolean expression is either 0 or
1, we can use bits in a long long integer to store the result
of Boolean expressions in a decision. A long long integer
can only store 64 conditions in a decision, if there are more
than 64 conditions in a decision, we use more long long
integers. Here, we only use one long long integer to show
the algorithm for simplicity. Then, after executing test case
t1, assume the final bitmap generated according to the above
description is \texttt{bitmap1}. After executing test case t2, assume
the final generated bitmap is \texttt{bitmap2}. For a decision with
decision index $d\_idx$, the decision is flipped (decision results
are different in two test cases t1 and t2) can be computed by $\text{dec\_flipped} = (((\text{bitmap1}[d\_idx] \text{ xor bitmap2}[d\_idx])
& 0x1) == 1)$. The condition in that decision with index
\texttt{cond\_idx} is flipped and all other conditions are not flipped
can be computed by $\text{cond\_flipped} = ((\text{bitmap1}[d\_idx] \gg 1
\text{ xor bitmap2}[d\_idx]) > 1) == 1 \ll (\text{cond\_idx} - 1))$. If the
decision is flipped and one condition is flipped with all other
conditions not flipped, one MC/DC condition is covered.

When updating the test case pool, if a test case increases the
model unit coverage or condition/decision coverage or MC/DC
coverage, then, this test case is considered interesting and will
be added to the test case pool. For each test case, we record
each specific branch or condition it covers. We generate a
signature for all branches and conditions a test case covers.
When we get the signature of a new test case, we will compare
the signature with the signatures of all the test cases in the
test case pool. If the signature of that new test case never
appears, that new test case will also be added to test case
pool. Otherwise, that test case will be dropped.

IV. Evaluation

In this section, we empirically evaluate the proposed frame-
work by answering the following research questions:

Effectiveness - RQ1: Can this proposed method improve
the coverage compared to baselines? How much coverage can
this proposed method improve?

Efficiency - RQ2: Can this method improve the running
speed compared to baselines? How much faster can this
method run?

Usefulness - RQ3: In the actual large-scale model, do the
newly proposed mutation operators based on signal patterns
have any effect? Can the fuzzing module improve MC/DC
coverage?

Implementations. This tool is a standalone cross-platform
application which contains 26000 lines of C++ code. Both
Windows and Linux platforms are supported. Associated tools
are provided, including Simulink model code to IR tool and an
embedded self written C code parser. The materials[7] including
benchmarks and the academic version of the tool are publicly
available. For parallel execution, multiple fuzzing processes
are started, and they can communicate with each other by
sharing the same test case pool.

The baselines. One of the baselines is Simulink Design
Verifier (SLDV). Because SLDV[8] is a famous testing and
verification tool which supports both the static analysis and
dynamic analysis. Besides, SLDV is a commercial tool which
has a user base of tens of millions. Another baseline tool is
an academic tool. There are many academic tools in the last
decades but most of them are unavailable now. The recently
available tool is SimCoTest[20] which uses genetic algorithms
to generate test cases for Simulink models.

The subject models. At present, all mainstream tools are
based on Simulink rather than Ptolemy, so here, we only use
Simulink models for comparative experiments. For non-CI-
CPS models, we used the publicly available benchmarks (i.e.,
RHB, AT, AFC, IGC) that have been previously used in the

1https://github.com/EmbedSystemTest/SimulinkTest
literature on testing of CPS models [21], [22], [23], [24], [25].

The models represent realistic CPS systems from different domains, including IoT, smart home and automobile. As the models contain state machines and continuous behaviors, we must use Simulink Rapid Simulation Target in Simulink Coder to generate code under test. By configuring the solver to be in fixed step mode, this target can generate code interacting with the Simulink real time library to simulate the real time environment. In addition to non-CI-CPS models, we also include pure control logic models in control fields such as fuel control, road control based on Euler distance and neural network guidance. These models are previously used in the Simulink verification survey [26].

A. RQ1 - Effectiveness

A key challenge regarding the empirical evaluation of SPsCGF is that, both SPsCGF and SimCoTest rely on randomized algorithms. Hence, we have to repeat our experiments numerous times for different models. To compare the SPsCGF with baselines, the condition and decision coverage are collected. As the testing report of SLDV takes all unique conditions or decisions as the objectives, we follow the same rule to compute the coverage. Table [I] shows the coverage values for SPsCGF-BMC, SPsCGF, SLDV and SimCoTest. The SPsCGF-BMC is part of SPsCGF. SPsCGF-BMC only uses bounded model checking to generate initial test cases, and does not contain the fuzzing module. The SPsCGF is the proposed tool which does fuzzing based on initial test cases generated by SPsCGF-BMC. All tools are configured to run for 60 seconds. However, even we set the rules, SLDV and SimCoTest seldom obey the rules, they often take more than 180 seconds to finish running.

| Model          | Condition Coverage SPsCGF-BMC | Condition Coverage SPsCGF | Condition Coverage SLDV | Condition Coverage SimCoTest |
|---------------|------------------------------|---------------------------|-------------------------|-----------------------------|
| NLGuidance    | 38%                          | 69%                       | 38%                     | 31%                         |
| RHB1          | 0%                           | 89%                       | 0%                      | 81%                         |
| RHB2          | 0%                           | 91%                       | 0%                      | 85%                         |
| Euler321      | 94%                          | 94%                       | 50%                     | 47%                         |
| BasicTwoTanks | 100%                         | 100%                      | 96%                     | 53%                         |
| EB            | 98%                          | 98%                       | 93%                     | 0%                          |
| MH1209        | 0%                           | 96%                       | 0%                      | 92%                         |
| AFC           | 0%                           | 67%                       | 0%                      | 67%                         |
| AT            | 0%                           | 79%                       | 0%                      | 68%                         |
| IGC           | 0%                           | 100%                      | 0%                      | 96%                         |
| Regulator     | 75%                          | 75%                       | 64%                     | 50%                         |
| BMultiplexor  | 88%                          | 88%                       | 88%                     | 69%                         |

For non-CI-CPS models, SLDV cannot generate a single test case. The coverage achieved by SLDV is 0%. The reason given by SLDV is that there exists an integrator in the model. There are also other elements SLDV cannot solve, for example, the event dispatch in Stateflow state loop or complex embedded C code. In the meanwhile, SPsCGF and SimCoTest perform significantly better than SLDV. The coverage of SPsCGF is higher than that of SimCoTest about 4% to 38% in non-CI-CPS models. The speed of SimCoTest is slow, the SPsCGF fuzzing method can generate tens of thousands of test cases in a second, that is the reason SPsCGF fuzzing method performs better than SimCoTest. In other models, SPsCGF and SLDV perform better than SimCoTest. That is because SPsCGF and SLDV use symbolic execution to solve constraints while SimCoTest solely uses random testing. In overall results, without considering the most extreme cases, SPsCGF performs 8% to 38% better than SimCoTest and performs 11% to 31% better than SLDV. Because SimCoTest and SLDV both rely on Simulink simulation, in practice, the running overhead of SimCoTest and SLDV is much larger than SPsCGF which is based on source code. The comparison about the speed of each tool will be described in next subsection.

B. RQ2 - Efficiency

The execution times of SPsCGF, SLDV and SimCoTest for the subject models in the benchmark are shown in Table [I]. To be fair, we collect the time taken for each tool to reach a certain coverage. This certain coverage is the lowest coverage achieved by the three tools. The results show that SPsCGF is significantly more efficient than SLDV or SimCoTest. Without considering the most extreme cases, the efficiency improvement that SPsCGF brings about over SimCoTest for most models ranges from 3x to 10x. In most situations, SimCoTest does not stop at the preset time. In most cases, SPsCGF only consumes 10-20 seconds to accomplish a task while SimCoTest consumes 2-3 minutes to accomplish the same task. The SLDV is much slower than expected, it takes too many times to do symbolic analysis. As the state-of-art tools such as SimCoTest and SLDV depend on the simulation environment of Simulink to run, this decreases the efficiency of testing. In contrast, the SPsCGF relies on generated code to do fuzzing testing and symbolic execution, this contributes to the high speed of testing. Besides, SPsCGF follows the fuzzing framework which supports parallel execution of the model, while SLDV and SimCoTest do not support parallel execution. From the results, we conclude that the fuzzing method has great advantages in efficiency.

C. RQ3 - Usefulness

We use the MH1209 model as the case study. This model takes 8 input ports and 54 parameters. A small part of the model is shown in Figure [I]. The COMP and ONDLC are special Simulink components containing the user written code. In this experiment, we compare the coverage results by using two methods: SPsCGF method and the raw coverage guided
fuzzing (rawCGF) method. The only difference between these two methods is that SPsCGF uses mutation operators based on signal patterns.

The MHI1209 model contains elements which SLDV cannot handle, thus the comparison of SLDV is omitted here. Figure 8 shows the coverage results over time. As can be seen from the Figure 8, Both two tools will improve coverage in 50 seconds. It is difficult for two tools to achieve a significant coverage increase after 60 seconds. From the figure, we can show that SPsCGF do improve the coverage and the mutation operators based on signal patterns take effect.

We further examine the elements covered by SPsCGF but not covered by rawCGF. Those elements are shown in Table III. The logic of ONDLC has been shown in Figure 2 (b) and OSHOTC has a similar logic pattern as ONDLC. As can be seen, in those elements, the coverage difference is huge. This confirms that the mutation operators based on signal patterns take effect in fuzzing procedure.

For MC/DC coverage, the decision expressions in most models only have one condition. In this case, the MC/DC coverage is equivalent to condition coverage or decision coverage. In benchmarks, there are only two models that contain two or more decisions which consists of two or more conditions. The only two models are NLGuidance and Euler321.

The MC/DC coverage is collected on these models. As shown in Table IV, SPsCGF-BMC performs well because CBMC (the kernel of SPsCGF-BMC) has an efficient built-in algorithm specially designed for MC/DC coverage. Even so, the fuzzing method achieves higher MC/DC coverage based on the initial seeds generated by CBMC.

| TABLE IV: MC/DC Coverage |
|---------------------------|
| Model         | SPsCGF-BMC | SPsCGF | SLDV |
| NLGuidance    | 0%         | 20%    | 0%   |
| Euler321      | 57%        | 76%    | 0%   |

V. RELATED WORK

Formal verification techniques [3], [4], [5], [6], [7] aim to exhaustively check the correctness of models, but they often face scalability issues for complex CPS models. Simulink Design Verifier [8] is the representative tool which uses formal verification techniques. For small and medium models, Simulink Design Verifier can achieve high coverage, but for large models, Simulink may fail to generate test cases. In order to verify large systems, The counterexample-guided abstraction refinement (CEGAR) frameworks [27], [28], [29], [30], [31], [32] have been proposed. Those techniques abstract hybrid system models into discrete finite state machines without dynamics or replace the complex system with a simpler one. However, these techniques need human intervention as the abstraction of the models need to be predefined. Search based techniques [10], [11], [12], [13], [14], [16], [17], [20] such as genetic algorithms or guided simulation algorithm [15] are also widely used in model testing to get high coverage. The concolic testing [33] is also applied to Simulink model to ensure the model safety. To generate inputs to find defects or wrong output signal patterns, different genetic algorithms [20], [34] have been proposed. Those algorithms use different fitness functions and fitness definitions to guide the search. The search based techniques can also be used to approximate the system [35], [36], [37] to help generate test cases. To evaluate the effectiveness of the test cases, mutation testing techniques [38], [39] have also been applied to models. By injecting manually created faults into models, the effectiveness of test cases can be evaluated according to whether the test cases can find the manually created faults.

VI. CONCLUSION

We presented a framework that combines bounded model checking with coverage guided fuzzing in a novel way to generate test cases. In the given benchmarks, the proposed framework can achieve 8% to 38% coverage improvement and 3x-10x speed improvement compared with the state-of-art baselines. Existing works have serious efficiency problems in industrial scenarios, and the proposed method can effectively improve testing efficiency.
