An Isolated Gate Driver for Multi-Active Bridges with Soft Switching

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Abstract—The design of gate drivers is an important topic in power converter topologies that can help reduce switching losses and increase power density. Gate driving techniques that offer zero-voltage switching and/or zero current switching have recently been successfully proposed for different modular multilevel converters such as the cascaded H bridge. Previous papers on other multilevel converters such as the multi-active bridge, however, do not sufficiently assess the topics of gate driver design for this topology. This work presents a novel isolated gate driver architecture tailored to the multi-active bridge topology. Zero voltage switching is then achieved using two multi-winding transformers. The advantages of the proposed topology are not only a reduction of switching losses but also reduced component count. The topology is evaluated on a prototype using experimental results. It was shown using simulation and experiments that the proposed topology has a high efficiency while providing compact power packaging. Especially for converters with many levels, the proposed topology is therefore advantageous compared to existing solutions.

Index Terms—Zero voltage switching, auxiliary supply, gate driver, multi-active bridge

\textbf{NOMENCLATURE}

- $x$: Second time derivative of $x$.
- $\dot{x}$: First time derivative of $x$.
- $A$: System matrix.
- $b$: Input vector.
- $x$: State-space variable.
- $x_{ss}$: Steady state of the state-space variable.
- $C_{DC}$: DC-link capacitance of the multi-active bridge circuit.
- $C_{dc}$: DC-link capacitance of the gate driver.
- $C_{DS}$: Drain-Source capacitance.
- $C_{eq}$: Equivalent gate-source capacitance of the multi-active bridge.
- $C_{GS}$: Gate-Source capacitance.
- $i_m$: Magnetization current of the gate driver transformer.
- $i_{GS}$: Current charging the gate-source capacitance.
- $L_s$: Stray inductance of the gate driver transformer.
- $L_M$: Magnetization inductance of the multi-active bridge circuit.
- $L_m$: Magnetization inductance of the gate driver.
- $M$: Number of modules of the multi-active bridge.
- $N$: Turns number of the multi-active bridge circuit transformer windings.
- $n$: Turns number of the gate driver transformer windings.
- $Q$: Switch on the multi-active bridge circuit.
- $q$: Switch on the gate driver.
- $R_c$: Conduction resistance of the gate driver.
- $R_{eq}$: Equivalent resistance of the gate driver.
- $R_{ON}$: ON-state resistance of the gate drive MOSFET.
- $S_i$: Signal that is applied to switch $i$.
- $t_{\text{fall}}$: Timing constant.
- $t_{\text{high}}$: Timing constant.
- $t_{\text{low}}$: Timing constant.
- $t_{\text{rise}}$: Timing constant.
- $t_{\text{zero}}$: Timing constant.
- $V_{\text{DC}}$: DC-voltage of the multi-active bridge.
- $V_{\text{gs}}$: Supply voltage of the gate driver.
- $V_{GS}$: Voltage between the Gate and Source terminals on the multi-active bridge circuit.
- $V_{\text{mid}}$: Midpoint voltage of the multi-active bridge circuit.
- $V_S$: Supply voltage of the multi-active bridge.
- $x_i$: $i$-th entry of the vector $x$.
- \text{GND}: Multi-active bridge reference voltage.
- \text{gnd}: Gate driver reference voltage.
- $u$: Input variable.

I. INTRODUCTION

Recent advances in multi-winding transformer research have produced interesting novel approaches for power converters derived from the multi-winding transformer technology [1].

![Circuit diagram of the multi-active bridge converter with ideal switches.](image)

A promising multi-winding transformer-based DC/DC topology is the multi-active bridge (MAB) [1]–[9]. The circuit diagram of a MAB converter is shown in Fig. 1. A more detailed introduction to MAB-based DC/DC converters is given. The MAB topology is a combination of many...
active bridges connected magnetically through a multi-winding transformer. Its advantage over regular cascaded H-bridge-based multilevel converters is the strong self-balancing which can be achieved by using a multi-winding transformer with a single core. In this way, all windings will be exposed to the same magnetic flux. If all windings also possess the same number of turns, the AC voltage in each active bridge will be similar which results in a balanced state. This solves the problem of the requirement of large DC/DC converters which significantly increases the power density of the converter. Over the past few years, several applications for MABs have been identified such as wireless charging [4], grid connections [5], and battery balancing [6]. Furthermore, the usage of the MAB has been proposed as a versatile solution for hybrid renewable energy systems [7], multilevel inverters [8] and energy routers [9].

Since the MAB is an AC-link-based topology, it requires constant switching at high frequencies to prevent its magnetics from going into saturation. For this reason, the reduction of switching losses in MAB-based topologies is of great importance. Over the past few decades, several approaches to quick and lossless gate-driving of MOSFET switches have been introduced [10]–[15]. Common state-of-the-art approaches include charge-pump [10] and bootstrap [11], [12] solutions. To reduce losses, [13] suggested saving the energy stored in the input capacitance of the MOSFET in an external resonant circuit. While those gate drivers rely on a half-bridge to generate the switching signal, an approach based on a class $\Phi_2$ inverter consisting only of a single switch has been proposed in [14]. In addition to that, [15] proposed to isolate the switching signal from the power circuit by using a transformer to transfer the information about the desired switching state as shown in Fig. 2 (a). While those solutions have been proven to work well for driving a single MOSFET which is sufficient for simple circuits, more complex topologies might consist of more than one switch. A key question, therefore, is how these concepts can be generalized to drive more than one switch with a minimal increase in complexity of the driving circuit. Isolating the driving circuits from each other is important not only because it offers protection of the gate driver from faulty switches but also allows to safely connect one power supply to many switches which are placed at different voltage levels to a common reference voltage [16]–[20]. Therefore, based on the approach presented in [15], many solutions for isolated gate drivers have been introduced, [16]–[20]. For certain applications, such as half-bridges, some of the switches always will be opened in a mutually exclusive manner. In this case, all switches can be attached to the transformer isolation as a tertiary winding and the mutual exclusive switching can be implemented by different turn directions of the windings [16]. Furthermore, the concept has been extended to high-power switches, adding overcurrent protection and thermal protection in [17]. In the case of a multilevel converter, the gate driver concepts have to be further extended to drive not only a few but an arbitrarily large amount of switches. While the basic concept of gate driving remains similar, the transformer isolation now is realized with a multi-winding transformer such as the cascaded half-bridge [18]. In [19] several techniques to reduce the EMI for this configuration have been examined. Furthermore, an isolated gate driver for a different multilevel inverter concept, the solid-state transformer, has been introduced in [20].

While several approaches for the topology of power supplies of MABs have been proposed, the design of a transformer-isolation-based power supply for gate drivers comes with several challenges [21]–[25]. One of these challenges is designing the transformer which starts with choosing the correct basic transformer geometry. While regular transformers, such as the toroidal transformer [21] have small parasitic capacitances, they are bulky and reduce the power density of the supply [21]. Planar transformers, on the other hand, provide a high power density but larger parasitic capacitances [22]. Once the basic geometry has been chosen, its parameters can be optimized to obtain the best transformer tailored to the desired application [22], [23] and reduce the effects of parasitic elements. To reduce the parasitic capacitance, several techniques have been examined such as geometric optimization with the help of finite element analysis [22]. Alternatively, formulas to estimate the parasitic capacitance from the parameters of this geometry can be used as shown in [23]. It is moreover possible to supply other low-power components using the same multi-winding transformer as the gate driver [24]. This can be achieved by attaching more windings to the transformer. If different voltage levels are required, the number of turns can be varied for those cases [24]. In addition to the optimization of the transformer, system theoretic aspects such as the stability of the gate driver can be taken into account when designing the circuit to ensure safe and reliable operation [25].

Several solutions for zero voltage switching in MABs have been proposed in [26]–[28]. A resonant tank can be used to reduce the voltage oscillations within the circuit as shown in [26]. Furthermore, the resonant tank can be used to increase the balancing speed of the DC-voltages of the MAB which was presented for battery balancing in [27]. In [28], the authors derived soft-switching conditions for MABs and gave guidelines for the selection of a suitable operating point. Although a variety of interesting concepts for power supplies for modular multilevel converters as well as resonant configurations for MABs has been presented in the literature, a combination of the two approaches, i.e. a power supply for MABs that allows lossless switching, is still subject to research.

In this paper, we propose an advanced isolated gate driver for MABs with a unique energy recovery technique that allows lossless switching of all transistors of the circuit. To store the energy of the parasitic capacitances of the switching in the MAB and the gate driver, two multi-winding transformers will be employed, one being part of the gate driver and the other being the regular MAB transformer that connects the modules. Contrary to the regular transformer isolation shown in Fig. 2 (a), the control part of the gate driver is entirely on the primary side of the multi-winding transformer which results in a centralized control approach, shown in Fig. 2 (b). In addition, the proposed gate driver is capable of ensuring synchronized switching of all modules.

The remainder of the paper is structured as follows: Section II
provides an overview of the proposed topology and its basic operating principle. In Section III, a state-space model and analysis of the proposed model are presented. Experiment results are given in Section IV and the conclusion follows in Section V.

II. TOPOLOGY OVERVIEW AND OPERATING PRINCIPLE

An overview of the overall design is shown in Fig. 2 (b). The switches in the MAB change their switching state when the gate-source capacitance is charged or discharged, for which an auxiliary power supply is used. A primary DC/AC converter topology is fed by the auxiliary power supply and determines whether the gate-source capacitors are charged or discharged. To synchronize charge or discharge of gate-source capacitances and ensure isolation of the switches from each other, a multi-winding transformer is used that transmits the power from the primary DC/AC converter circuit to all switches in the MAB. The goal is to minimize the power consumption of this circuit which is provided by the auxiliary supply.

A. Proposed topology

To properly drive the MOSFETs of an active bridge, the gate driver topology must be able to produce the following switching states:

1) a positive output voltage which indicates that the switches which are to be driven are closed
2) a negative output voltage which shows that the switches to be driven by the gate driver are open. In case there are other switches connected to the gate driver transformer with the opposite turns direction, those switches will be closed when the negative voltage is applied.
3) A third switching state that gives the possibility to save
the energy which is stored in the gate-source capacitance of the MOSFETs.

4) A switching state that sets the midpoint voltage to zero and allows energy exchange between the high power transformer and the drain-source capacitances of the MOSFETs to be switched to reduce switching losses.

Quantities that refer to the low-power gate driver will use small case letters while quantities that refer to the high-power MAB will be capitalized for the remainder of this paper. An example of a topology that satisfies those requirements is the clamped active bridge, shown in Fig. 3. Using the auxiliary supply $V_{gd}$ as well as the switches $q_i$, $i \in \{1, 2, 3, 4, 5, 6\}$, the following midpoint voltages can be created: If the switches $q_2$ and $q_3$ are closed, the midpoint voltage will be positive. In case the switches $q_1$ and $q_4$ are closed, the midpoint voltage will be negative. Closing the switches $q_5$ and $q_6$ yields a zero midpoint voltage. Opening all switches gives a floating midpoint. An overview of the switching states can be seen in Table I.

**TABLE I**

|                | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $V_{mid}$  |
|----------------|-------|-------|-------|-------|-------|-------|------------|
| High           | 0     | 1     | 1     | 0     | 0     | 0     | $+V_{gd}$  |
| Low            | 1     | 0     | 0     | 1     | 0     | 0     | $-V_{gd}$  |
| Zero           | 0     | 0     | 0     | 0     | 1     | 1     | 0          |
| Floating       | 0     | 0     | 0     | 0     | 0     | 0     | Varying    |

The goal is to use the gate driver topology to drive all switches of the MAB synchronously. To successfully drive all switches in the MAB, the gate driver needs to be able to access all switches in the MAB converter. This is achieved by connecting it to each of the switches with a multi-winding transformer. Each winding of the multi-winding transformer is connected to one MOSFET of the MAB. All switches of the MAB that are mutually exclusive (as seen in Fig. 4) must furthermore have different turns directions in the secondary windings to ensure that they cannot be closed at the same time as shown in Fig. 5. To connect a MAB, other active bridges can be connected magnetically to the gate driver transformer in a similar way. Furthermore, the energy that is stored in the gate-source capacitors of the switches that are turned off can be transferred to the magnetization inductance $L_m$ of the gate-driver transformer during the floating state which achieves lossless operation of the gate driver. During the zero states, the energy stored in the drain-source capacitors will be stored in the magnetization inductance $L_M$ of the main circuit which results in the lossless operation of the MAB switches as well.

**B. Operating principle**

An overview of the operating principle during one switching can be seen in Figure 6. For this section, we assume that the switching frequency is high enough so that both transformers will not go into saturation. One operation cycle consists of 6 steps which will be given in the following:

- **Step 1:** In the beginning, $Q_1$ and $Q_4$ are closed, and their gate-source and drain-source capacitors are fully charged. The gate driver ensures this by keeping $q_1$ and $q_4$ closed which results in a voltage of $+V_{gd}$ at the transformer windings attached to $Q_1$ and $Q_4$ and $-V_{gd}$ at the transformer windings attached to $Q_2$ and $Q_3$. This configuration is shown in Fig. 6(a).

- **Step 2:** As soon as $Q_1$ and $Q_4$ should be opened, the gate driver opens $q_1$ and $q_4$ resulting in all gate driver switches being open and the midpoint voltage changing to floating. Since the voltage across the gate-driver magnetization inductance $L_m$ is now not fixed by the gate driver anymore, it will start discharging the gate-source capacitors of $Q_1$ and $Q_4$, storing the energy from these two capacitors. Fig. 6(b) shows this configuration.
In this section, a system model of the gate driver is derived for each of the modules of the MAB. The purpose of the state-space model is to analyze the behavior of the system similar pattern, in reverse order. If the capacitors charge and discharge linearly, the switching losses of the MAB will be negligible if combined with the proposed gate driver. A hard-switching gate driver with the same auxiliary supply would ensure that the midpoint voltage will stay constant and allow the drain-source capacitors of the MAB to be charged through the magnetization inductance of the MAB transformer. This step is shown in Fig. 6 (d).

Switching $Q_2$ and $Q_3$ off and $Q_1$ and $Q_4$ on again follows a similar pattern, in reverse order. If the capacitors charge and discharge linearly, the switching losses of the MAB will be negligible if combined with the proposed gate driver. A hard-switching gate driver with the same auxiliary supply would yield losses of $\frac{1}{2}C_{GD}(2V_{bus})^2$ for each of the $4M$ switches per switching action.

### III. STATE-SPACE MODELLING AND ANALYSIS

In this section, a system model of the gate driver is derived to get a more detailed insight into its behavior. The purpose of the state-space model is to analyze the behavior of the system
and derive design criteria for a prototype. The modeling is based on the following assumptions:

1) Negligible parasitic capacitances within the transformer.
2) All switches are synchronized.
3) All transformer windings are identical.
4) Linear magnetization inductance, stray inductances, conduction losses, and Gate-source capacitances of the driven MOSFET.
5) 100% coupling of transformer windings.
6) The behavior of all circuit elements is independent of the frequency of the signals given to the gate driver.

A multi-active full-bridge converter consists of 4M high-power MOSFETs. Since all windings of the gate driver transformer share the same magnetic flux, the secondary AC voltages of each winding are identical. The second assumption together with the third assumption allows replacing the 4M secondary windings attached to the gate-source capacitances $C_{GS}$ of the MAB with one single equivalent winding. Furthermore, it is assumed that each element has a linear resistance resulting in one equivalent resistance $R_{eq}$ for each Step, consisting of $R_{ON}$, the ON-state resistance of the gate-driver MOSFETs $q_1, ..., q_6$ and $R_{c}$ which is the conduction resistance of the multi-winding transformer. In addition to the equivalent capacitance, assuming negligible cross-coupling allows representing the multi-winding transformer as a single T-model shown in Fig. 7. To fully describe the system, a three-dimensional state-space vector $x(t)$ is necessary, consisting of

$$x(t) = \begin{bmatrix} i_{gs}(t) & V_{gs}(t) & i_{lm}(t) \end{bmatrix}^T \in \mathbb{R}^3.$$  \hspace{1cm} (1)

Furthermore, the input $u(t)$ of the gate driver shall be defined as the gate-driver supply voltage, which is changing for different different steps,

$$u(t) = \begin{cases} -V_{gd}, & \text{Step 1} \\ 0, & \text{Step 2, Step 3, Step 4, Step 5} \\ +V_{gd}, & \text{Step 6} \end{cases}$$  \hspace{1cm} (2)
While the switches of the MAB are ON, the gate driver is represented by the equivalent circuit shown in Fig. 7 (a). Using Kirchhoff’s equations, the dynamics of the system can be derived as

\[
\dot{x}(t) = \begin{bmatrix}
\frac{R_e}{L_s} & -\frac{1}{L_s} & -\frac{R_e}{L_s} \\
\frac{C_{GS}}{L_m} & 0 & 0 \\
\frac{C_{GS}}{L_m} & 0 & -\frac{R_e}{L_m}
\end{bmatrix} x(t) + \begin{bmatrix}
\frac{1}{L_s} \\
0 \\
\frac{1}{L_m}
\end{bmatrix} u(t),
\]

for Step 1 and Step 6. For those cases, the system reaches steady state for

\[
x_{1,6}^s = \begin{bmatrix} 0 & 0 & \frac{u}{R_{eq}} \end{bmatrix}^T.
\]

This indicates that the transformer will go into saturation and the magnetization current will become 0 after a while. In this situation, the gate driver loses its functionality and the supply will simply force a current going through the primary side. To avoid this, the circuit must be operated at a minimum operating frequency.

During the floating phase, no external power supply is connected to the gate driver transformer. An equivalent circuit for this case is given in Fig. 7 (b). Therefore, the only way to change the voltage across the magnetization inductance is through exchange with the gate-source capacitance. For this reason, the input \( u(t) \) will not influence the system behavior in this case. Since there is no resistor current \( i_R \), the third row of the state-space matrix will be zero and the system matrix will be overdetermined.

\[
\dot{x}(t) = \begin{bmatrix}
0 & -\frac{1}{L_m + L_s} & 0 \\
\frac{C_{GS}}{L_m} & 0 & 0 \\
0 & 0 & 0
\end{bmatrix} x(t) + \begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix} u(t).
\]

In this situation, the entire system dynamics can be formulated as a second order differential equation,

\[
\ddot{x}_1(t) = \frac{1}{C_{GS}(L_m - L_s)} \dot{x}_1(t).
\]

This equation is a homogeneous linear differential equation of second order and thus has a sinusoidal solution in a steady-state condition. It can therefore be observed that there will be a constant fluctuation of energy between the magnetization inductance and the gate-source capacitance. An equivalent circuit for the case when the switches at the midpoint clamping are closed is given in Fig. 7 (c). As in the previous step, there is no external source supplying the primary side of the gate driver. In this case, however, there is a current \( i_R \) flowing through the midpoint clamping which can be characterized from the ON-state resistance of the closed switches \( q_5 \) and \( q_6 \). The system equations for this situation are given as

\[
\dot{x}(t) = \begin{bmatrix}
-\frac{R_e}{L_s} & -\frac{1}{L_s} & -\frac{R_e}{L_s} \\
\frac{C_{GS}}{L_m} & 0 & 0 \\
\frac{C_{GS}}{L_m} & 0 & -\frac{R_e}{L_m}
\end{bmatrix} x(t) + \begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix} u(t).
\]

The steady state conditions for this case are given as

\[
x_{3,4}^s = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix}^T.
\]

This indicates that the system will converge towards an idle state during this switching state, allowing charge exchange for the drain-source capacitances \( C_{DS} \) with the main transformer magnetization inductance \( L_M \). It should be noted that the system matrix for this switching state is identical to the one for Steps 1 and 6. During all Steps, the system has a linear structure of

\[
x(t) = Ax(t) + bu(t).
\]

Having the system equations, it is possible to predict the behavior of the gate-source voltage of the MAB switches under ideal operating conditions:

Ideal operating conditions are defined as the switching frequency being high enough to have an almost constant gate-source voltage during Step 1 and Step 6 and a gate driver supply that ensures that the gate-source voltage is almost linear during the floating state. Furthermore, the clamping switches shall be activated when the midpoint voltage reaches zero. In this case, behavior such as the one depicted in Fig. 8 can be observed. This behavior can also be seen in simulation results as shown in Fig. 9.

A. Design Guidelines

This section discusses several design aspects of a prototype of the proposed gate driver topology. The design process in this paper is based on the assumption that the user has already selected a MAB with a known MOSFET gate-source capacitance \( C_{GS} \). Then, the remaining steps are as follows:

1. Select a switching frequency and compute the desired magnetization inductance that can charge and discharge the MOSFET capacitors within this frequency.
2. Compute values for \( L_s \) and \( R_{eq} \) that guarantee a stable system during \( t_{high}, t_{low} \) and \( t_{zero} \).
3. Tune the timing constants \( t_{zero}, t_{high}, t_{low}, t_{rise}, t_{fall}, t_{zero} \) to ensure operation with minimal switching losses.

The following sections discuss these steps in more detail. Having selected the magnetization inductance, the question of how to choose the other parameters \( L_s \) and \( R_{eq} \) shall be selected. Therefore, we examine the stability properties of the system matrix \( A \) derived in the previous section. To examine the dynamic behavior of the system, the Eigenvalues \( \lambda \) were computed for different scenarios:

\[
\det (A - \lambda I) = 0,
\]

where \( I \) is a 3×3 identity matrix. Since the system matrix is the same for the switching Steps 1,3,4,6 and the system is always boundary stable for Steps 2 and 5, only the system matrices for Steps 1,3,4,6 are discussed. Although the presented system has a switching nature, and thus stability for all individual Steps does not necessitate stability for the system under switching conditions, it can be achieved in this case by changing to Step 3 or 4 and waiting until the dynamic components of the system discharge through the equivalent resistance.

Using the Eigenvalue analysis, it was found that \( A \) does not become unstable for all examined realizations of the system. However, choosing the correct values for \( L_s \) and \( R_{eq} \) has an impact on the oscillations in the system and thus the power
losses.
The system has two complex conjugated and one real eigenvalue as can be seen from Fig. 10. In case the resistance $R_{eq}$ is zero, the real part of all Eigenvalues is 0 and the system will continue to oscillate. Increasing $R_{eq}$ will add a negative real part to all three Eigenvalues. This reduces the amplitude of the oscillations and introduces damping to the system. A high resistance however also increases the conduction losses of the system and thus decreases the efficiency. For this reason, a trade-off has to be reached for $R_{eq}$.

A variation in the stray inductance $L_s$ only influences the two complex conjugated eigenvalues as can be seen from Fig. 11. The smaller the value, the more negative the real part of the eigenvalue pair. In addition to that, small values of $L_s$ also increase the imaginary part of the eigenvalues which results in higher oscillation frequencies. Those oscillations would however, decay over time due to the negative real part of the Eigenvalue. Furthermore, having no $L_s$ will result in an $L$-$C$-resonant tank formed by the magnetization inductance $L_m$ and the MOSFET capacitance $C_{GS}$. For decreasing $L_s$ the behavior of the system will therefore converge towards the one of a conventional $R$-$L$-$C$ parallel circuit.

B. Operation Timing Selection

To successfully operate the gate driver, the timing constants have to be chosen correctly which shall be discussed in this paragraph. To minimize losses of the gate driver, it is important to obtain a curve with continuous transitions at the midpoint as shown in Fig. 8. In this case, the timings are selected in a way that the transition to the zero-state will take place when the midpoint voltage is zero and the transition to the high/low state takes place when the midpoint voltage is $\pm V_{GD}$. Additionally, the zero-time must be chosen to be large enough to accommodate discharging and charging the drain-source capacitances of $Q_s$ and allowing a sign change in the midpoint

![Fig. 10. Root locus of the gate driver system matrix for changing $R_{eq}$. A magnetization inductance of $L_m = 4.1\, \mu\text{H}$, a stray inductance of $L_s = 0.1\, \text{nH}$ and a gate-source capacitance of $C_{GS} = 2.23\, \text{pF}$ were selected for this scenario. Then, 500 values with logarithmic spacing between $1\, \Omega$ and $1\, \Omega$ were chosen for $R_{eq}$. The figure shows the change of the eigenvalues of the system matrix $A$ for the different values of $R_{eq}$.](image)

![Fig. 11. Root locus of the gate driver system matrix for different values of the stray inductance $L_s$. For this scenario, a magnetization inductance of $L_m = 4.1\, \mu\text{H}$, an equivalent resistance of $R_{eq} = 0.125\, \Omega$ and a gate-source capacitance of $C_{GS} = 2.23\, \text{nF}$ were chosen. After that, the Eigenvalues of the system matrix $A$ were evaluated for 500 different values of the stray inductance which were logarithmically spaced between $L_s = 0.001\, \text{nH}$ and $L_s = 1\, \text{H}$. Shown are the trajectories of the two complex conjugated Eigenvalues. The third Eigenvalue is independent of $L_s$ and does not move.](image)

IV. Prototype Construction and Experimental Results

To verify the findings proposed in this paper, a gate driver prototype shown in Fig. 12 was built. The prototype consists of two assemblies, the primary gate driver board which can be seen in Fig. 12 (a) and the gate driver transformer together with a MAB shown in Fig. 12 (b). To verify the efficiency for large-scale multilevel converters, the gate driver is tested for a MAB with 4 groups of modules, each of which is made up of 4 active bridges that are connected in parallel. The 400 V MAB thus consists of 16 modules with 64 switches which were used to test the proposed gate driver. The 64 switches each have an input capacitance of 2330 pF and output capacitance of 220 pF that need to be charged during the switching. To get insight into the efficiency of the proposed topology, the switching losses for hard-switching can be estimated by $E_{sw} = 0.5 C_{GS} V_{G}^2 \approx 0.456\, \mu\text{J}$ per switch. In the case of a frequency of 125 kHz, the average power loss is equal to 57 mW for each switch. To change the switching state, it is furthermore necessary to maintain a threshold voltage of 2.9 V across the gate-source terminals of the MOSFETs. A DC voltage of 7.0 V was selected as the operating voltage of the gate driver to ensure the

![Fig. 12. (a) Gate driver prototype. (b) gate driver transformer together with a MAB.](image)
threshold voltage requirements are met. The gate driver prototype, therefore, needs a multi-winding transformer with 64 secondary windings. To optimize the power packaging and increase the power density, the gate driver transformer is implemented as a planar transformer with 16 primary windings (P) and 64 secondary windings (S) as shown in Fig. 12 (c). The winding arrangement is $S^+ - S^- - S^+ - S^- - P$. All windings are identical and have 2 turns where the notation $S^+$ and $S^-$ refer to the turn directions of each winding. Since a full identification of this transformer requires $0.5 \cdot 80 \cdot 79 = 3160$ measurements, a full characterization of the prototype will not be given in this paper and all tuning will be performed "by inspection" to obtain preliminary results for the verification of our findings. However, a qualitative assessment of the behaviour of the device For the remainder of this section, symmetric operation is assumed, i.e. $t_{\text{rise}} = t_{\text{fall}}$ and $t_{\text{high}} = t_{\text{low}}$.

Figure 13 shows the midpoint waveform with the modulator being correctly timed. The curve verifies the theoretical analysis and modeling shown in Fig. 8 which suggests a similar pattern in the second subfigure. The main difference is seen as a decaying sinusoidal noise during the high-, low- and zero states. This is due to the limited resolution of the FPGA which is controlling the modulator. All timings are selected as an integer multiple of the clock frequency of the FPGA. In case this value is not exactly equal to the optimal value, a small deviation will remain which is further amplified by the turn-ON and turn-OFF delays of the switches on the gate driver circuits.

If the timings are not chosen correctly, the gate-source voltage waveform will be distorted. Choosing the rise/fall time too small will result in ripples as seen in Fig. 14 which occur due to the gate-source voltage not yet reaching the desired value when the next switching state is applied. Choosing the timings too small will result in a curved waveform during the rise/ fall time. This is due to the sinusoidal nature of the voltage during that switching state which was derived in the previous section. Choosing a correct timing however, will result in only the approximately linear part of the waveform being present since the circuit switches to Step 1 or Step 6 before the peak of the sinusoidal is reached. Figure 15 shows that the overall energy consumption of the gate driver circuit
Fig. 14. Experiment results of the effects of different timing selections on the gate driver waveform concerning $t_{\text{rise}}$. The top subfigure (a) shows a waveform corresponding to a value of $t_{\text{rise}} = 100$ ns. The middle subfigure (b) depicts a waveform with $t_{\text{rise}} = 1000$ ns and the bottom subfigure (c) represents $t_{\text{rise}} = 1500$ ns. In all cases, the zero-time is $t_{\text{zero}} = 800$ ns and the switching frequency is $f_s = 125$ kHz.

Fig. 15. Experiment results of the power loss for different values of $t_{\text{rise}}$. The top figure (a) shows the energy loss of the main gate driver circuit per MAB MOSFET in mW. For reference, the power loss that would occur on a gate driver topology with hard switching is shown in orange. The lower subfigure (b) shows the overall losses of all 64 MAB MOSFETs and the auxiliary power losses for DC/DC converters, diagnostics LEDs, ... For these experiments, the zero-time is $t_{\text{zero}} = 800$ ns and the switching frequency is $f_s = 125$ kHz.

Fig. 16. Experiment results of the effects of different timing selections on the gate driver waveform with respect to $t_{\text{zero}}$. The top subfigure (a) shows the midpoint waveform for $t_{\text{zero}} = 100$ ns. A zero-time of $t_{\text{zero}} = 800$ ns can be seen in the middle subfigure (b) while the bottom subfigure (c) shows a waveform with $t_{\text{zero}} = 1500$ ns. A rise time of $t_{\text{rise}} = 1000$ ns and a switching frequency of $f_s = 125$ kHz were selected during the experiments.

Fig. 17. Experiment results of the power loss for different values of $t_{\text{zero}}$. The top figure (a) represents the power that is used by the primary active bridge to maintain operation, normalized for the total number of high-power MAB switches. In addition, the power loss of a gate driver topology based on hard-switching is shown in orange. The bottom figure (b) depicts the total power losses, used by the MAB as well as the auxiliary supply for the gate driver circuit. To obtain a fair comparison, the rise time of $t_{\text{rise}} = 1000$ ns and switching frequency of $f_s = 125$ kHz were used in all cases.

decreases until the optimal value is found and stays constant after that.

A similar effect can be seen when the zero time is varied. Selecting a zero time too short will result in the drain-source capacitor not fully discharging which results in distorted waveforms (Fig. 16) and higher losses (Fig. 17). Similarly, choosing the zero time too large will result in an increase in losses as seen in Fig. 17 which can be explained by staying in the zero states while the energy is completely transferred and the energy might flow back to the drain-source capacitance. In between of those effects, an optimal value can be obtained as shown in Fig. 17.

Varying the switching frequency of the MAB frequency will decrease the power consumption of the gate driver as seen in Fig. 18. However, choosing a frequency too low will result in restrictions of the zero and rise timings which will again yield a decrease in performance.

V. CONCLUSION

This paper presented a novel gate driver model for MAB DC/DC converters. To maximize the efficiency of the MAB, a zero-voltage switching scheme was employed within the gate driver. Therefore, the topology utilizes a multi-winding transformer to exchange energy stored in the gate-source capacitances of the MOSFETs in the MAB. Similarly, the energy within the drain-source capacitance was exchanged
with the parasitic inductances in the drain-source capacitance. The fundamental working principle was derived with a system model and verified with experiment results. The advantages of the topologies are the lower switching losses and the requirement for fewer components. Furthermore, guidelines for the modulation of the gate driver are given. However, it is not possible to implement phase-shifts between the individual active bridges of the MAB which is the major limitation of the proposed topology.

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