Very low temperature epitaxy of group-IV semiconductors for use in FinFET, stacked nanowires and monolithic 3D integration

Porret, C.; Hikavyy, A.; Granados, J. F. Gomez; Baudot, S.; Vohra, A.; Kunert, B.; Douhard, B.; Sammak, A.; Scappucci, G.; More Authors

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As CMOS scaling proceeds with sub-10 nm nodes, new architectures and materials are implemented to continue increasing performances at constant footprint. Strained and stacked channels and 3D-integrated devices have for instance been introduced for this purpose. A common requirement for these new technologies is a strict limitation in thermal budgets to preserve the integrity of devices already present on the chips. We present our latest developments on low-temperature epitaxial growth processes, ranging from channel to source/drain applications for a variety of devices and describe options to address the upcoming challenges. © The Author(s) 2019. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0071908jss]
observed that peculiar relaxation mechanisms occur at wafers edges. In the case of Si\textsubscript{0.7}Ge\textsubscript{0.3} grown on 300 nm Si(001) wafers, more than 200 nm thick SiGe layers could be grown relaxation-free at the center of the wafer. However, relaxation was systematically initiated at wafers edges. SP3 haze maps acquired on two 200 nm thick Si\textsubscript{0.7}Ge\textsubscript{0.3} layers grown on Si and corresponding thickness profiles extracted by HR-XRD are shown in Figure 1c and Figure 1d. Details about the haze measurement technique can be found in Ref. 14. Light areas, mostly observed on outer rings at wafers periphery, correlate with regions where high haze signals were recorded. These regions match with areas layers an onset of SiGe relaxation was confirmed with XRD-RSM (not shown here). The only difference between the two presented wafers is that a -8°C relative edge temperature offset (colder edge during epi) has been applied when processing the wafer shown in Figure 1d. As expected, the thickness profile was varied from edge-thick to center-thick. Correspondingly, the importance of the high haze area decreased, i.e. a lower fraction of the wafer surface was covered by partly relaxed SiGe. In the case of Figure 1d, relaxation at wafer edge cannot be attributed to an increase in SiGe thickness toward the edge. However, it shows that relaxation can to some extent be delayed by decreasing the thermal budget applied to wafer edges, indicating that great care should be devoted to the control of epi layers structural properties in the vicinity of wafers edges in order to avoid variability in devices properties across the wafers.

**Figure 1.** (a) Degree of strain relaxation extracted from XRD-RSM acquired in the vicinity of the asymmetric (224) Bragg reflection on as-grown and annealed Si\textsubscript{0.7}Ge\textsubscript{0.3} layers of different thicknesses grown on Si(001) at wafers center. Error bars correspond to a relaxation of \( \pm 5\% \). The post epi anneals were done in 300 mm production furnaces with the following conditions. Long anneals were performed at 700°C for 30 min in N\textsubscript{2} ambient. The temperature ramp rate was 10°C/min. “Spike” anneals were executed in He and took advantage of a different technology. The reactor was kept at the target temperature of 1000°C prior to loading the wafer in the close vicinity of the reactor walls, from which it is separated by a very thin layer of gas (here He), allowing for a very efficient and extremely fast energy transfer. (b) XRD-RSM acquired in the direction parallel to the 20 nm wide fins around the (113) Si Bragg reflection, at the center of the wafer. (c), (d) 2D plots of scattered light intensity (haze maps) originating from the surface of two 200 nm thick Si\textsubscript{0.7}Ge\textsubscript{0.3} layers grown on Si and corresponding thickness profiles extracted from 6-points HR-XRD radius scans, with a -8°C relative edge temperature offsets applied in the case of (d).
SiGe diffraction spots are vertically aligned at H = 1, demonstrating that the SiGe epi layer has the same in-plane lattice parameter as the underlying substrate. After fin etch, Shallow Trench Isolation (STI) filling between fins and fins reveal (STI recess), the SiGe spot is found close to its initial position, indicating that most of the initial 1.10% compressive strain is preserved. An accurate fitting and analysis of the XRD-RSM data shown in Figure 1b allows to extract a compressive longitudinal strain of 1.03% after fin reveal. The reported values are in good agreement with the ~1.13% compressive strain expected for Si_{0.7}Ge_{0.3} grown on Si. Note that no high thermal budget has been applied between these two steps. As a conclusion, thick SiGe epi layers needed for the fabrication of tall fins should be grown with a controlled and limited thermal budget to ensure the formation of metastable strained layers and avoid relaxation during epi. After fin etch, free sidewalls allow for some elastic deformation which helps avoid plastic relaxation, making 50 nm Si_{0.7}Ge_{0.3} a viable option for device processing.

**SiGe/Si or SiGe/Ge multi-stacks for GAA preparation.**—In the GAA geometry, horizontally-stacked Si, SiGe or Ge nanowire or nanosheet channels are formed by selective etching of sacrificial SiGe layers, epitaxially grown in SiGe/Si, Si_{1-x}Ge_{x}/Si_{1-y}Ge_{y} (x > y) or SiGe/Ge multi-stacks, respectively. For Si- and SiGe-channel GAA devices, strained multi-layers can be grown with conventional precursors (SiH₄ or DCS in combination with GeH₄) at conventional temperatures of 600–700°C. The obtained compositional gradients are sufficiently steep to allow efficient wire release by selective SiGe or Si removal.

As already shown in Ref. 16, the use of SiGe/Si multi layers enables the growth of metastable stacks with larger equivalent SiGe critical thicknesses compared to blanket SiGe. In this work, we observe that SiGe/Si multi-stacks, generate lower wafer bow and warp than their single-layer counterparts, confirming improved mechanical stability (Figure 2). This allows to maintain a very low surface roughness (<1 nm RMS, not shown here). With this approach, multi-stacks can be grown without relaxation, allowing the fabrication of GAA devices including up to 7 stacked nanowires or more. However, one should take into account difficulties for patterning dense SiGe/Si fins with high h/w ratios and for uniformly releasing the different channels. Indeed, adding Si spacers increases the required patterned fin height (doubled if t_{SiGe} = t_{Si}) for a given SiGe active section, thereby strongly complexifying fin patterning steps with additional risks for damages to materials and pattern collapse. In other words, with very high h/w ratios are required to compete with equivalent single-layer fins. In the case of Ge GAA, the epitaxial growth of Ge-rich SiGe/Ge on SiGe Strain Relaxed Buffers (SRB) is more challenging. Extremely low process temperatures (<400°C) are required to avoid strain relaxation. These layers necessitate the use of higher order precursors (Si₂H₆ and Ge₂H₆), since conventional precursors become ineffective.

**Figure 2.** (a) Schematic cross-section of the SiGe/Si multi-stacks used for Si GAA devices and cross-section SEM of a stack including 15 [10 nm Si_{0.7}Ge_{0.3}/10 nm Si] periods. (b) Measured wafer bow and warp as a function of SiGe nominal thickness (e.g. 50 nm Si_{0.7}Ge_{0.3} corresponds to a multi-stack with 5 [10 nm Si_{0.7}Ge_{0.3}/10 nm Si] periods). (c) Degree of strain relaxation extracted from XRD-RSM acquired around the (113) Bragg reflection for Si_{0.7}Ge_{0.3} layers as a function of Si_{0.7}Ge_{0.3} nominal thicknesses. Error bars correspond to a degree of relaxation of ±5%.
Si passivation for Ge-rich channels.—The epitaxial growth of ultra-thin Si layers on (strained) Ge fins or nanowires has been thoroughly discussed in Ref. 18. In this work, SiH₄ and Si₂H₆ were used as Si precursors to enable the epitaxy of very thin Si films to passivate Ge channels at temperatures as low as 330°C. It was found that the strain due to the lattice mismatch between the Si passivation layer and the Ge fin is the driving force for unwanted Ge surface reflow during Si deposition. The reflow is strongly affected by H-passivation during Si-capping and can be avoided by carefully selecting process conditions and keeping the epi thermal budget as low as possible.

Low temperature epitaxy of p-type S/D materials for SiGe and Ge finFETs and GAA.—The downscaling of transistors systematically leads to a reduction in the S/D contact area. As a result, the contact resistance becomes a key contributor to device parasitics⁹,¹⁹,²⁰ and device performance might be limited by the metal-semiconductor contact. For this reason, minimizing the contact resistivity at metal-S/D level is mandatory. Contact resistivity values of ≤ 1 × 10⁻⁹ Ω cm² are typically considered as targets for advanced technology nodes. To meet this objective, the right materials, matching interfaces from band structure perspective, should be grown selectively in S/D areas with thermal budgets compatible with existing devices. Required active doping levels are usually extremely high (> 1 × 10²⁰ cm⁻³) and far above the dopants solubility limits. This motivates the use of far-from-thermodynamic-equilibrium processes. In addition, S/D epi materials are often used as channel stressors to boost carrier mobility. The later aspect must also be taken into account when defining S/D for a given technology. In the next section we focus on p-type S/D. For reference, results on the SEG of highly-doped Si:P have been presented in Ref. 9.

Low temperature SiGe epitaxy and etch.—Decreasing epi or etch temperature typically results in a decrease in growth or etching rate, respectively, until the processes become ineffective (no growth, no etch). Conventional epi precursors typically provide decent growth rates of a few nm/min down to temperatures of ~ 500°C (SiH₄) and ~ 350°C (GeH₄).⁶ From the etch side, HCl can be used down to ~400°C for the etch of pure Ge but to etch Si or SiGe, the process temperature needs to be strongly increased, up to ~ 600°C, as soon as the Si content exceeds 50%.²¹ Higher order silanes and germanes enable important reductions in SiGe growth temperatures.⁶ In addition, Cl₂ allows dramatic reductions of the vapor etching temperature, e.g. down to ~ 350°C for Si₉₃Ge₀₇.¹¹ We considered different combinations of precursors and etchants as described in the following paragraphs.

p-type SiGe.—Highly B-doped SiₓGeₓ (with 40% ≤ x ≤ 70%) materials are often regarded as the best option for the epitaxy of S/D for pMOS Si devices.²²–²⁵ In addition to acting as a natural stressor for Si channels, an additional benefit of using SiGe as S/D material is the capability to selectively deposit layers with very high active B concentrations (~ 1 × 10²¹ cm⁻³), using conventional precursors at temperatures of 500°C or higher, as illustrated in Figure 3a. The situation differs for so-called high-mobility channel devices, where the Si channel is replaced by compressively strained Ge in case of pMOS. There, SiGe S/D layers do not apply the right stress and, for pure Ge (or SiGe with > 70% Ge), the low B solubility makes it extremely challenging to reach a high active doping concentration. Moreover, for Ge pMOS and 3D stacking of Si, SiGe or Ge based devices, the epi thermal budget should be reduced. For these reasons, alternative process conditions are being explored. We consider the use of disilane (Si₂H₆) and digermane (Ge₂H₆) for the epitaxy of highly-doped SiGe at reduced temperatures (~ 450°C). Initial results obtained from Si₉₃Ge₀₇:B epi layers grown at 400°C have yielded an active B concentration of 5 × 10²⁰ cm⁻³, which still needs to be increased in order to compete with conventional processes. In addition, these low temperature processes have the drawback of being non-selective, resulting in the unwanted deposition of amorphous or polycrystalline SiGe on STI-oxide and nitride spacers. This makes it mandatory to work with cyclic schemes including low temperature growth and selective etching of amorphous/polycrystalline SiGe versus crystalline SiGe using Cl₂. Figure 3b displays top-view SEM images acquired on (80 × 80 μm²) measurement pads and 100 nm Si fin test structures surrounded by STI, after the cyclic deposition-etch of Si₉₃Ge₀₇:B at 400°C. Different deposition/etch time ratios were used. We observed that selective depositions could be achieved for deposition/etch time ratios lower than 5. For reference, a deposition/etch time ratio of 5 provided a net growth rate of ~ 1.4 nm per cycle on wafers used for the 3D sequential stacking of planar devices. Obviously, the growth and etch rates per cycle depend on the considered mask (percentage of area covered by silicon oxide and nitride) and device geometry, so these timings are to be adjusted for every application. More optimizations are obviously needed to develop processes fully selective toward nitride spacers used for advanced devices and to further increase active doping. Nevertheless, low temperature SiGe doped processes provide new options for the epitaxy of advanced S/D.

Figure 3. (a) Highest active B concentrations obtained in Si, SiGe and Ge SEG S/D epi layers grown with conventional precursors (DCS, SiH₄, GeH₄, HCl) as measured by Micro Hall Effect measurements (MHE). To extract active doping values, a Hall Scattering Factor of 1 is assumed. (b) Top-view SEM images acquired on test structures after the cyclic deposition-etch of Si₉₃Ge₀₇:B using Si₂H₆, Ge₂H₆ and Cl₂ at 400°C with different deposition/etch ratios between 10 and 2.
Ga as an alternative p-type dopant for SiGe S/D.—The solubility of boron in Ge is more than a factor 10 lower than that of boron in Si, as listed in Table I. As a result, achieving high B-doping in Ge-rich SiGe is a challenge. For this reason, Ga is considered as a promising alternative dopant, due to the higher solubility of Ga in Ge. Ga can also be used for SiGe, eventually as a co-dopant in addition to B.26 Experimental evidences of contact resistivity improvements using Ga have already been provided in Ref. 27, where record-breaking low contact resistivity values below \(10^{-9}\) \(\Omega \cdot\text{cm}^2\) have been demonstrated with Ga-implanted SiGe layers. However, the reported processing scheme requires an unwanted high thermal budget (laser anneal) for dopants activation and does not allow conformal doping profiles on patterned structures. Therefore, the selective epitaxial growth of in-situ doped Ge:Ga and SiGe:Ga or SiGe:B:Ga is highly desired to ensure a full compatibility with advanced finFET and Gate-All-Around devices, both in terms of selectivity, conformality, process complexity and thermal budget. Achieving high p-type doping of SiGe with Ga has some challenges. Indeed, the low Ga solubility in Si leads to a severe risk for Ga precipitation and agglomeration. Moreover, unwanted carbon incorporation can be an issue, as all commercially available Ga process gases contain alkyl groups (\(\text{CH}_x\)). We have explored the RPA-CVD of Ga-doped SiGe and [B + Ga] co-doped SiGe S/D materials. Dopants incorporation and distribution in the semiconductor matrix were investigated and correlated with the electrical properties of the layers.

**Ga-doped SiGe.**—To the best of authors’ knowledge, Ga-doping of Si\(_{1-x}\)Ge\(_x\) has not been reported in the literature. The epitaxy of SiGe:Ga with an active B doping level close to \(10^{20}\) \(\text{cm}^{-3}\) and atomic density of \(5.0 \times 10^{22}\) \(\text{cm}^{-3}\) has not been reported in the literature. The epitaxy of SiGe:Ga with an active B doping level close to \(10^{20}\) \(\text{cm}^{-3}\) and atomic density of \(5.0 \times 10^{22}\) \(\text{cm}^{-3}\) has not been reported in the literature. The epitaxy of SiGe:Ga with an active B doping level close to \(10^{20}\) \(\text{cm}^{-3}\) and atomic density of \(5.0 \times 10^{22}\) \(\text{cm}^{-3}\) has not been reported in the literature. The epitaxy of SiGe:Ga with an active B doping level close to \(10^{20}\) \(\text{cm}^{-3}\) and atomic density of \(5.0 \times 10^{22}\) \(\text{cm}^{-3}\) has not been reported in the literature.

**Table I. Atomic radius and maximum solubilities of several dopants in Si and Ge.**

| Specie | Atomic radius (pm) | Max. solub. in Si (\(\text{cm}^{-3}\)) | Max. solub. in Ge (\(\text{cm}^{-3}\)) |
|--------|------------------|---------------------------------|----------------------------------|
| B      | 87               | \(8 \times 10^{20}\)            | \(2 \times 10^{18}\)            |
| Si     | 111              | Atomic density: \(5.0 \times 10^{22}\) |                                   |
| Al     | 118              | \(2 \times 10^{19} \sim 8 \times 10^{20}\) | \(4 \times 10^{20}\)          |
| Ge     | 125              | Atomic density: \(4.4 \times 10^{22}\) |                                   |
| Ga     | 136              | \(4 \times 10^{19} \sim 1 \times 10^{20}\) | \(5 \times 10^{20}\)          |
| Sn     | 145              | \(7 < 10^{19}\)                 | \(4 < 10^{20}\)               |

**First MR-CTLM assessment of [B + Ga] co-doped SiGe layers.—** Multi-Ring Circular Transmission Line Model (MR-CTLM) structures were used to evaluate the accessible contact resistivity. Details about method and process are given in Refs. 32,33. Using the SiGe:B:Ga layer shown in Figure 4a, grown with non-optimized conditions on a 300 mm Si wafer, we could demonstrate contact resistivities as low as \(2.9 \times 10^{-9}\) \(\Omega \cdot\text{cm}^2\). This value should be compared with the contact resistivity of \(6.1 \times 10^{-9}\) \(\Omega \cdot\text{cm}^2\) obtained with a similar layer grown without Ga. This is a clear demonstration that Ga-doping helps in reaching contact resistivity targets for future technology nodes, although the limits of the evaluated approaches are not yet known.

Growth of Ge:Ga on blanket and selectively on GeSi.—The Ga-doping of CVD or MOCVD grown Ge has been reported previously.34,35 For these layers grown at relatively high temperatures (\(>550°C\)) limited doping values were obtained and Ga segregation observed. However, epitaxial Ge:Ga S/D will be candidate for Ge technologies in case low temperature processing (\(<500°C\)) can be applied. In order to avoid a reflow of the Ge channel material, which can cause strain relaxation and the generation of defects. Using GeH\(_4\) and TMGa (which was the Ga MO precursor initially available in the Epsilon reactor), we could successfully grow Ge:Ga on Ge virtual substrates (VS) at temperatures \(<500°C\) (i) without any noticeable oxygen and C incorporation (C detection limit \(<5 \times 10^{17}\) \(\text{cm}^{-2}\) in the layer nor at the Ge:Ga/VS interface, (ii) with flat Ga profiles (see e.g. the SIMS data in Figure 4c) and (iii) active doping levels above \(1 \times 10^{20}\) \(\text{cm}^{-3}\), as confirmed by MHE measurements, using a Hall Scattering Factor (HSF) of 1. The grown Ge:Ga layers exhibited resistivity values lower than 0.4 m\(\Omega\)\cdot\text{cm}. When growing such a layer, the main difficulty is to keep Ga diluted in the Ge matrix and avoid any uncontrollable Ga clustering. Indeed, EDX compositional analyses (not presented here) have shown that Ga-rich dots with Ga contents up to 8% can form in non-optimized growth conditions. Remarkably, Ge:Ga layers can be selectively deposited at these relatively low temperatures (Figure 4d). However, controlling Ga clustering has shown to be even more challenging on patterned wafers. Interestingly, by reducing the Ga precursor flow and/or the growth temperature, we could decrease Ga segregation. Ga-rich clusters were then mostly found close to the Ge-STI interface and their density decreased when moving toward the inner parts of the pads. We interpret the result presented in Figure 4d as a clear indication for Ga loading effects.

**Very low temperature processes: B-doped Ge and GeSn.—** As already discussed, increasing active doping concentration in Ge-rich S/D materials can be achieved by increasing the growth rate at low temperature. Epitaxial growth is a non-equilibrium process which can be moved further away from equilibrium by modifying growth chemistries.36 This can be done by either using a high-order precursor like dimerane (Ge\(_2\)H\(_6\))37,38 or by taking advantage of specific reactions or catalytic effects by combining different precursors as it is likely the case for GeSn materials.39,39 Both approaches own their specific challenges though. Indeed, achieving the selective epitaxial growth of highly doped materials with controlled properties is not straightforward.

**Highly-doped Ge:B grown at low growth temperature using Ge\(_2\)H\(_6\).**—Growing Ge:B with B\(_2\)H\(_6\) and Ge\(_2\)H\(_6\) instead of Ge\(_4\)H\(_{10}\) allows maintaining decent growth rates of a few mm/min at reduced temperatures (\(<350°C\)). At low growth temperatures, dopants adsorbed on the growing surfaces see their diffusion length and desorption rate reduced. As a consequence, dopants incorporation and activation are enhanced, as previously reported for Ge:P.40 In order to assess the electrical properties of our Ge:B epi layers, we have combined SIMS, micro 4-points probe (m4pp) and Micro Hall Effect (MHE) measurements. Figure 5a summarizes the results in these respects. In addition, no oxygen peak was observed at the SiGe:B/GaSi interface. Interestingly, although the addition of Ga does not lead to a significant increase in active doping, it indeed lowers the material resistivity (Figure 4b, ASIM data), which is also promising for devices’ performance improvements. Still, a better control over unwanted C incorporation is required.
Figure 4. (a) B, Ga and Ge SIMS profiles extracted from a 35 nm thick Si0.5Ge0.5:B:Ga layer directly grown on Si. (b) SiGe:B:Ga resistivity as a function of Ga precursor flow (ASM data). (c) Ga, P and Ge SIMS profiles measured in a 180 nm thick Ga-doped Ge layer, epitaxially grown on 200 nm Ge:P on Ge/Si. (d) SEM images of selectively grown Ge:Ga layers at two different growth temperatures T1 and T2, all other conditions being the same. At temperature $T_2 < T_1$, Ga clustering is clearly reduced.

data do not show any saturation and an active doping concentration as high as $3 \times 10^{20} \text{cm}^{-3}$ could be obtained. However, mobility values keep on reducing with increasing B content. On the other hand, $m_{4pp}$ data shows an apparent saturation in active doping concentration, which implies that assumed mobility values (available in literature for [B]active up to $\sim 1 \times 10^{20} \text{cm}^{-3}$) are not correct (overestimated) for these highly-doped layers. Finally, by using a Ge:B process providing an active B concentration of $2.2 \times 10^{20} \text{cm}^{-3}$, a low Ti/p+Ge contact resistivity of $5.5 \times 10^{-9} \Omega \text{cm}^2$ has been obtained without any post-epi treatment. Due to the non-selective nature of the process, we expect similar properties on patterned structures as loading effects should be absent or very weak.

As Ge:B growth with Ge2H6 is not selective, a cyclic deposition-etch routine needs to be used for selective S/D deposition schemes. Because of the low processing temperature, Cl2 is suggested as etchant. The desired epi layer thickness and process selectivity were tuned by optimizing individual steps and the number of deposition/etch cycles. Although tuning the uniformity of both epitaxy and etch steps was not a straightforward task, very decent thickness and resistivity profiles have been achieved with a 1-standard-deviation uniformity of 0.9% for a $\sim 105$ nm thick Ge:B layer grown on blanket Ge/Si (Figure 5b). These optimized conditions resulted in an average layer resistivity of $\rho_{\text{Ge:B}} \sim 0.43 \Omega \text{cm}$. The impact of B-doping on layers’ structural properties was evaluated with Triple-Axis XRD (TA-XRD) measurements for Ge:B layers grown on undoped Ge VS (Figure 5c). The peak located at $\sim -5450$ arcsec is assigned to the slightly tensile strained Ge VS and the peak at higher angles is assigned to Ge:B. The position of the Ge:B peak shifts toward higher angles with increasing B contents, due to an increase in tensile strain in the layer. Finally, Ge:B processes were applied to fin device structures. An example SEM image is provided in Figure 5d, where the full selectivity of the process versus STI-oxide and nitride spacers is confirmed. It also indicates that the S/D material quality obtained on 20 nm fins is sufficiently high as the selective etching does not result in any observable etch pits nor roughness.

**GeSn:B selective epitaxial growth for S/D.**—Adding SnCl4 to the GeH4 + B2H6 growth chemistry allows the selective epitaxial growth (without the need for cyclic selective etching) of GeSn:B with active B concentrations up to $3.2 \times 10^{20} \text{cm}^{-3}$.41 The active doping can be further increased up to $5 \times 10^{20} \text{cm}^{-3}$ for $\delta$-doped GeSn.42 Due to the presence of Sn, one can expect the achievement of low contact resistivities and the transfer of compressive strain to Ge channels (see Table 1). However, due to the low Sn solubility in Ge, there is a risk for Sn precipitation and clustering, similar to what was observed for Ga-doping. This is especially important for the epitaxy of GeSn on patterned wafers where loading effects can enhance this risk. After an optimization of growth conditions $p_\text{B}$ values as low as $3.6 \times 10^{-9} \Omega \text{cm}^2$ were extracted from MR-CTLM measurements on Ti/Ge0.95Sn0.05:B stacks. Again, this low $p_\text{B}$ value was obtained without post-growth thermal treatments to increase active dopant concentration. We have also worked on the implementation of Ge0.99Sn0.01:B S/D on advanced Ge GAA devices and could demonstrate very good process conformality and selectivity. More details about these aspects are discussed in Ref. 41.
Conclusions

In this contribution, we have presented some of our latest developments on the low-temperature epitaxial growth of group-IV semiconductors. Working on new devices and chips architectures imply new constraints for the growth processes. Epi thermal budgets should in general be reduced, especially when working with high-mobility channel materials, where relaxation needs to be avoided and strain preserved. We have seen that 50 nm tall strained Si$_{0.7}$Ge$_{0.3}$ fins can be prepared using standards Si and Ge precursors. Blanket Si$_{0.7}$Ge$_{0.3}$ layers are metastable and do not sustain the high thermal budgets required for state-of-the-art fin processing. For this reason, care has to be taken to ensure that fully-strained layers reach fin patterning, after which transverse elastic relaxation helps maintaining longitudinal strain in the fins. Si$_{0.7}$Ge$_{0.3}$/Si multi-stacks, as used for GAA, improve fins mechanical stability but complexify subsequent fin etch steps. Therefore, compromises are to be found to fabricate tall and strained SiGe fins devices. Additional challenges arise when considering source/drain processes. The low temperature deposition processes should remain selective and provide very high doping levels. We consider different approaches to meet these objectives. Higher order precursors are used for the growth of Ge and SiGe materials at very reduced temperatures of $\leq 400{^\circ}C$. If interesting electrical properties can be obtained, these processes are typically non-selective, which makes their implementation in devices difficult. B-doped GeSn alloys are an interesting alternative to Ge source/drain, as the deposition is intrinsically selective and high growth rates are obtained at low temperature with conventional GeH$_4$. Finally, we also consider alternative dopants such as Ga to circumvent limitations due to the low solubility of B in Ge.

We demonstrate that adding Ga dopants in source/drain layers enables a reduction in contact resistivities. Results obtained with Ti/p+Ge$_{0.99}$Sn$_{0.01}$:B and Si$_{0.5}$Ge$_{0.5}$:B:Ga materials yielded $\rho_c$ values as low as low as $3.6 \times 10^{-9}\ \Omega\cdot\text{cm}^2$ and $2.9 \times 10^{-9}\ \Omega\cdot\text{cm}^2$, respectively, for layers grown conformally and without post-growth thermal treatments.

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ORCID

C. Porret https://orcid.org/0000-0002-4561-348X
A. Vohra https://orcid.org/0000-0002-2831-0719
R. Loo https://orcid.org/0000-0003-3513-6058

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