Low Frequency Noise Analysis of Impact of Metal Gate Processing on the Gate Oxide Stack Quality

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A review is given about the impact of the metal gate (MG) in a High-k/Metal Gate (HKMG) stack on the quality and defectivity of the dielectric, assessed by low-frequency (LF) noise spectroscopy. In a first part, processing aspects are discussed, like, the thickness of the MG and the implementation of a gate-last approach. In the latter case, it is shown that both the cleaning (or dummy gate removal), the growth of the interfacial SiO₂ layer (chemical versus thermal) and a post-HfO₂-deposition heat or SF₆ plasma treatment need to be optimized for reducing the gate oxide trap density. In a second part, different MGs are compared from a viewpoint of noise magnitude. It is generally found that alternatives to the standard TiN gate yield better static and noise performance. Results will be presented both for scaled planar and FinFET technologies; the latter fabricated on either bulk or Silicon-on-Insulator (SOI) substrates. Also results on Gate-All-Around NanoWire FETs (GAA NWFETs) fabricated on SOI will be included.

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It is well-established that the gate oxide quality and reliability strongly depend on the type of high-k and interfacial oxide layer, the deposition method and the implementation of possible post-deposition annealing or passivation treatments. Low-frequency (LF) noise is a parameter which is very sensitive to the presence of traps and charges in the gate dielectric.¹⁻⁴ For large-area Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), the 1/f or flicker noise (γ = 1) typically found can be either due to carrier trapping in oxide traps (so-called Δμ model).⁵ For small-area transistors, the current fluctuations may become dominated by a single trap, resulting in so-called Random Telegraph Noise (RTN).⁶ Both RTN and 1/f noise are commonly used to characterize traps in the gate dielectric, revealing their energy level, capture cross section and position with respect to the interface with the channel.⁶⁻¹¹ Assuming direct elastic tunneling of carriers, one can derive from a 1/f²-spectrum an oxide trap density profile as a function of the depth, whereby an exponent γ > 1 indicates a uniform profile, while γ < 1 or γ > 1 corresponds with a trap density increasing or decreasing toward the interface.⁶⁻¹¹ As a result, the low-frequency noise magnitude or Power Spectral Density (PSD) may be largely affected by the gate dielectric processing details, whereby it has been shown that the noise PSD usually increases when switching from SiO₂ or SiON to high-k layers.¹⁵⁻¹⁹

What is less studied is the impact of the gate material itself on the gate stack quality. The combination of a polycrystalline (poly) silicon gate with a high-k dielectric leads to undesirable phenomena like Fermi level pinning and associated high threshold voltage (Vₜ) and poly depletion effects, which increase the Equivalent Oxide Thickness (EOT). In addition, the charges in the poly gate cause remote coulomb scattering of inversion layer carriers, which also results in a higher 1/f noise.²⁰⁻²⁴ Replacing a poly gate by a metal gate (MG), therefore, generally results in a lowering of the 1/f noise PSD. Often, TiN-based MGs are being implemented. Early results indicate that the thickness of the TiN layer, defined by the number of Atomic Layer Deposition (ALD) cycles, has an impact on the noise PSD.²⁵ A reduction of the noise PSD was reported for a higher number of ALD cycles, i.e., a thicker TiN layer.

The present work reviews the low-frequency noise of High-k/Metal Gate (HKMG) MOS transistors with emphasis on the role of the specific gate metal. Devices with different architectures (planar, FinFET and NanoWire (NW) FETs) will be addressed in addition to the gate first versus gate last (or replacement metal gate – RMG) integration.²⁶⁻²⁸

Processing Impact

In this part, the impact of the process implementation of a metal gate is investigated. First, the effect of the processing of a W plug or fill metal on the LF noise performance of planar 22 nm pMOSFETs is reported. A second example studies the impact of the thickness of the TiN layer on the noise performance of Silicon-on-Insulator (SOI) Multiple Gate FETs (MuGFETs). Finally, different processing aspects with respect to the implementation of an RMG will be addressed from a viewpoint of the noise performance, both for planar and FinFET transistors.

W plug processing.—The impact of the W plug processing on the LF noise of planar 22 nm CMOS compatible pMOSFETs is illustrated in Fig. 1. The gate dielectrics consist of a 0.8 nm SiO₂ interfacial layer and 2 nm HfO₂ deposited by Atomic Layer Deposition (ALD). The MG sandwich consists of 2 nm ALD TiN, 3 nm Ti deposited by Physical Vapor Deposition (PVD), 5 nm TiN fabricated by Metal Organic Chemical Vapor Deposition (MOCVD) and 75 nm ALD W, whereby two different processes have been studied, namely, using B₁H₆ + W or SiH₄ + W precursors. The current noise PSD (S_I) has been measured in linear operation (V_DS = −0.05 V), stepping the gate voltage V_GS from weak to strong inversion (more negative values). The input-referred noise voltage PSD has been derived from the measured S_I, through S_I/V_GS = S_I/gₘ², with gₘ the measured transconductance in each bias point.

As can be seen in Fig. 1, S_I at a frequency f = 10 Hz versus the absolute drain current I_D is higher for the B₁H₆ precursor case, compared with the W deposition using SiH₄ as precursor. The higher input-referred voltage noise PSD is not caused by a difference in V_T as the S_I/V_GS at flatband has been determined at V_GS = −V_T, but is interpreted in terms of a higher oxide trap density, which is evidenced by the bump at about 100 μA drain current (I_D), which is thought associated with a gate oxide trap, causing a Random Telegraph Signal (RTS). The oxide trap density Nₕ is calculated from the 1/f noise PSD using:⁷

\[ N_h = \frac{1}{2} \left[ \frac{k_BT}{Q_L} \right] \frac{S_I}{(V_T)^2} \]

[1]
with q the elementary charge; $k_b$ Boltzmann’s constant and T the absolute temperature. Further, W and L are the device width and length, respectively, $C_{EOT}$ the capacitance density (F/cm$^2$) corresponding with the Equivalent Oxide Thickness (EOT) and $\alpha_t$ the hole tunneling parameter in the gate oxide. It has been shown that the increase in $S_{Vg}$ at higher gate voltages can be interpreted in terms of the correlated mobility fluctuations model, whereby the gate voltage dependence can be described by:

$$S_{Vg}^{1/2} = S_{Vgf}^{1/2}[1 \pm \alpha_t \mu_{eff} C_{EOT} (V_{GS} - V_T)]$$

with $S_{Vgf}$ the input-referred voltage noise PSD at flatband voltage ($V_{FB}$), $\alpha_t$ the coulomb scattering coefficient and $\mu_{eff}$ the effective low-field mobility. The + or − sign depends on the nature of the oxide traps (donor or acceptor type). An example of such analysis is given in Fig. 2 for $f = 10$ Hz for both SiH$_4$ and B$_2$H$_6$ precursors. It can be noticed that the B$_2$H$_6$ W pMOSFET has a higher $S_{Vg}^{1/2}$, and in strong inversion, the $S_{Vg}^{1/2}$ curve has a similar trend as the SiH$_4$ W device.

The resulting $S_{Vgf}$ and $\alpha_t$ for the SiH$_4$ and B$_2$H$_6$ splits are summarized in Fig. 3. As can be seen from the figure, the average $S_{Vgf}$ is about one decade higher for the B$_2$H$_6$ pMOSFETs, on the one hand due to the presence of more pronounced Generation-Recombination (GR) humps at $f = 10$ Hz, as found in Fig. 1. In addition, also the background 1/f noise PSD is higher, indicating a higher trap density in the oxide. These could possibly be related to the ion-diffusion of B in the gate dielectric, which would introduce an acceptor state near the conduction band of the high-$\kappa$ dielectric.

Another trend to be derived from Fig. 3 is the 4 times higher average $\alpha_t$ for the B$_2$H$_6$ devices. This indicates that the charged oxide traps in the latter case are significantly more efficient coulomb scattering centers, possibly because they are on the average closer to the Si/SiO$_2$ interface. A higher $\alpha_t$ is usually found when the inversion layer charge is closer to the border traps in the oxide. This may support again B in-diffusion as a possible cause of the increased oxide trap density.

Information about the location of the generation-recombination deep traps can be obtained by studying the gate voltage dependence of the corner frequency, as shown in Fig. 4 for W plugs fabricated with the two different precursors. It can be noticed that for SiH$_4$ devices there is a strong gate voltage dependence of the Lorentzian peak maximum, indicating that the traps are located in in the gate oxide layer. On the other hand, the gate voltage independence of the corner frequency, corresponding with the peak maximum is characteristic for deep traps located in the depletion layer.

**Impact of the TiN thickness on SOI FinFETs.**—As mentioned before, the thickness of the TiN gate plays a crucial role in defining the threshold voltage and the LF noise of planar devices. This has also been investigated for SOI n- and p-channel Multiple Gate FETs (MuGFETs), fabricated on a 65 nm film, a 150 nm Buried Oxide (BOX) thickness and with fin widths down to 25 nm. The gate stack consists of a 1 nm SiO$_2$ IL and 2.3 nm MOCVD HfSiO. TiN capped with 100 nm polysilicon was used as gate electrode. The TiN thickness has been varied between 2 nm (64 ALD cycles), 5 nm (160 ALD cycles) and 10 nm (320 ALD cycles). The LF noise was measured in linear operation (50 mV).

The outcome of this study is summarized in Fig. 5a, showing that the oxide trap density derived from $S_{Vgf}$ increases with TiN thickness, contrary to the previous case. At the same time, the low-field mobility $\mu_0$ of the n-channel transistors is improved for smaller TiN thickness, indicating a correlation between the two parameters. This is again associated with a higher coulomb scattering factor, as more clearly shown in Fig. 5b, which plots the inverse low-field mobility versus the coulomb scattering term $q_\alpha_t N_{ox}$. The higher product $q_\alpha_t N_{ox}$ corresponds with a lower $\mu_0$. The possible origin of the higher $N_{ox}$ with thicker TiN layer could be related with the higher oxygen scavenging ability, which leaves behind electrically active, “noisy” oxygen vacancy centers in the gate dielectric. The possible influence of the EOT has been considered in order to calculate both the mobility from the Y-function method and the $N_{ox}$. The impact of the TiN thickness on the analog parameters of MuGFETs has also been studied, indicating that a thinner TiN metal gate yields an enhanced voltage gain which can be attributed to the increased Early voltage.
Impact of RMG processing.—Implementation of a HKMG has become standard for state-of-the-art FinFET technologies.\textsuperscript{32} Moreover, so-called high-k-last or RMG integration schemes offer a wider process window for the deposition of metal-oxide cap layers to tune the effective work function and, hence, the threshold voltage.\textsuperscript{33,34} This implies that a dummy amorphous or polysilicon gate and gate oxide need to be removed first, before fabricating the final HKMG stack. In order to enable the deposition of a good quality gate dielectric, effective pre-cleaning of the silicon surface is of vital importance.\textsuperscript{32,33} Different types of pre-cleaning can be considered,\textsuperscript{35} including standard diluted HF cleaning, a remote plasma (RP) cleaning in NF\textsubscript{3}/NH\textsubscript{3} called siconi\textsuperscript{36} or a combination of the two. This was followed by an in situ O\textsubscript{3} oxidation to form an interfacial SiO\textsubscript{2} layer (IL-SiO\textsubscript{2}).\textsuperscript{35} Subsequent deposition of HfO\textsubscript{2} resulted in planar pMOSFETs with...
an EOT of about 1 nm. A standard TiN gate with W fill metal was implemented. A LF noise evaluation of the different oxide-removal steps revealed that the RP clean yields a significantly lower input-referred voltage noise PSD, compared with the standard diluted HF clean, indicating a better quality gate stack.

A second approach to improve the gate stack quality is by forming a good quality interfacial SiO2 layer. Comparing a chemical oxide IL with in situ steam generated (ISSG) oxidation prior to HfO2 growth has revealed a two times higher 1/f noise PSD for planar n- and p-channel MOSFETs, fabricated with an EOT of about 1 nm. The gate dielectric consisted of a thin (<1 nm) SiO2 IL (ISSG or ozone treatment) and between 2 and 2.5 nm HfO2. On the other hand, there was little impact of the HfO2 thickness, varying between 2.0 and 2.5 nm nor the fill metal (W versus Al) on the average gate oxide trap density.

A final way to improve the quality of a RMG is by performing a post-deposition treatment. In Ref. 28, a post-deposition annealing (PDA) in N2 at 500 °C for 1 min was compared with a post-HfO2-ALD SF6 plasma treatment for different times (3, 6 or 9 min), followed by the same PDA. This should introduce F in the gate stack, which is known to passivate oxide traps and reduce the 1/f noise PSD. The investigated pMOSFETs had a 0.6 nm chemical (ozone) SiO2, formed after standard diluted HF clean, 36 ALD cycles of HfO2 (∼1.8 nm thickness) and TiN gate followed by a fill metal. As illustrated in Fig. 6, showing for the different process options the experimental data and median value, optimal noise performance was found for a 3 to 6 min SF6 treatment, resulting in a clear reduction of the average noise PSD and the device-to-device variation.

Overall, combining a siconi removal of the dummy gate oxide, an ISSG SiO2 IL and an SF6 post-HfO2-ALD treatment of 3 to 6 minutes, followed by a 500 °C PDA should result in the lowest 1/f noise PSD for planar pMOSFETs, using a TiN metal gate. Finally, similar improvements in the LF noise PSD have been achieved for RMG p-type FinFETs after an SF6 plasma treatment.

Different Metal Gate Materials

So far, the focus was on the integration aspect of a MG in the process flow, with TiN as the standard metal. However, it has been seen before that for example the thickness of the TiN layer can impact on the gate oxide quality, as probed by the LF noise PSD. The question arises what happens if TiN is replaced by another metal? Here, two examples will be given, showing that replacing TiN by an alternative material can drastically improve the LF noise and, hence, the oxide trap density.

TaN versus TiN in thick oxide IO pMOSFETs.—Input-Output (IO) transistors for DRAM applications have traditionally been fabricated with a thick SiO2 layer (∼5 nm) and a polysilicon gate. This yields a low 1/f noise PSD, corresponding with a low oxide trap density and at the same time leads to a high Negative-Bias-Temperature Instability (NBTI) lifetime. However, these devices become more and more adopted to the processing of the peripheral logic material, characterized by a HKMG stack. This implies that the polysilicon gate is being replaced by a MG (TiN) and that on top of the SiO2 a HfO2 layer is deposited. This is usually followed by a rather high DRAM thermal budget so that there is a good chance that the SiO2 layer quality becomes degraded by the in-diffusion (or out-diffusion) of certain elements. As shown before, this indeed leads to a degradation of the LF noise PSD, an increase in the Nt and a degradation of the NBTI characteristics for IO pMOSFETs.

In order to improve the NBTI performance or even recover the original behavior for the poly/SiO2 reference several process options have been considered, like, for example a post-deposition SF6 plasma treatment or replacing the TiN gate by TaN. An example of the latter case is shown in Fig. 7, comparing the noise spectra of a 1 μm × 0.170 μm planar IO pMOSFET biased in linear operation (VDS = −0.05 V) at different gate biases and processed either with a standard HKMG stack (TiN/HfO2) or with a TaN gate. As can be seen, the spectra are predominantly 1/f-noise like with some GR noise humps, occurring at different frequencies from device to device. As shown elsewhere, the 1/f noise is dominated by number fluctuations, so that an oxide trap density (and profile) can be extracted from the noise spectra. It is also evident that in the case of Fig. 7, the TaN...
gate pMOSFET has a significantly lower 1/f noise PSD compared with the TiN reference. This goes along with an improvement of the NBTI behavior. However, another parameter which is relevant with respect to noise is its variation or spread across the wafer. Therefore, Fig. 8 gives the average input-referred voltage noise PSD at 10 Hz for a number of pMOSFETs arranged along the vertical diameter of both wafers. It can be observed that, while TaN-gate devices potentially have the lowest noise PSD, which is comparable to the poly/SiO$_2$ IO pMOSFETs, the device-to-device spread is significantly larger, spanning more than a decade. It has been observed that this is related with the more frequent occurrence of excess GR noise at $f = 10$ Hz for the TaN devices. Its origin is not clear for the moment but deserves future more detailed studies. For both TiN and TaN devices the $f \times S_{\mu}$ spectra have been studied as shown in Fig. 9. Except for the higher noise level for TiN, a similar behavior is found for TiN and TaN, i.e., a similar frequency exponent of the spectra, implying in this case a more or less uniform oxide trap density in the frequency range studied. At the same time, the better NBTI behavior found for larger-area TaN pMOSFETs supports the idea that their gate stack quality is intrinsically better, i.e., corresponding with a smaller trap density. The physical origin of this observation is not clear but could point to a different oxygen scavenging by TaN compared with TiN.

In order to optimize the gate stack from a viewpoint of work function tuning and to improve the overall quality and reliability issues much work has been performed on the use of capping layers and possibly the use of sandwich metal layers. The systematic study of the impact of capping layers such as Al$_2$O$_3$, LaO$_x$ and Mg, taking into account the location of the cap layer (above or below the gate dielectric) in relation to the dielectric layer and the thermal anneal budget, indicated that the noise PSD and its variability increase for capping layers underneath the gate dielectric and for higher anneal temperatures.

The impact of capping layers and metal gate structures is summarized in Fig. 10. Based on the median value for the different process options, it can be seen that 1) the TiN deposition technique (ALD vs PVD) has no real influence on the noise performance, 2) the impact of the Al$_2$O$_3$ layer in combination with HKMG is limited, 3) the lowest noise level is obtained for TaN, and 5) the use of a sandwich structure TaN-TiN marginally influences the noise compared to the TaN case, while TaN-Al$_2$O$_3$-TiN seems to lead a small increase.

**TiAl versus TiN in gate-all-around nanowire transistors.**—Ultimately, the Gate-All-Around (GAA) nanowire (NW) architecture may take over at the end of the Roadmap due to the superior gate control over the short-channel effects. Improved performance has been demonstrated for GAA NW n- and pMOSFETs fabricated on SOI substrates, compared with tri-gate FinFETs. More interestingly, a pronounced impact of the metal gate has been noted as well. This is illustrated in Fig. 11 for the maximum transconductance $g_m$ of the n-channel GAA NW FETs. At the same time, it has been shown...
that the 1/f noise PSD is significantly smaller as well (horizontal axis of Fig. 11), confirming a general correlation between $N_\text{ox}$ and $g_m$; a lower $N_\text{ox}$ goes hand in hand with a higher transconductance.

In order to understand better the origin of this strong impact of the metal gate, the noise spectra have been transformed into oxide trap density profiles versus trap depth with respect to the Si/SiO$_2$ interface. This is represented in Fig. 12, revealing an increase of $N_\text{ox}$ toward the metal gate for the TiN device, which is absent for the TiAl case. This suggests a possible oxygen scavenging effect of Ti on the gate stack,\(^5\) creating an excess of “noisy” oxygen vacancy centers in the high-$x$ layer.

**Summary**

An overview has been given about the impact of the metal gate on the LF noise PSD of both planar FETs, triple-gate FinFETs and GAA NWFETs. In a first part, it has been demonstrated that the processing of a Mg can have a significant effect on the overall gate stack quality. Both the metal gate fill processing, as well as the thickness of a TiN gate can modify the oxide trap density. Devices with $B_2H_6 + W$ processed metal gate were found to have a higher mean trap density and scattering coefficient than SiH$_4 + W$ processed gate metal. For SiH$_4$ devices there is a strong gate voltage dependence of the Lorentzian peak maximum, indicating that the traps are located in the gate oxide layer. In the case of $B_2H_6$ the traps are located in the silicon depletion layer.

Especially in the case of present-day RMG processing, one should carefully optimize the pre-cleaning (dummy gate removal) and the metal gate layer. Post-high-$x$ treatments can also be implemented in order to improve the device performance and lower the 1/f noise PSD. An SF$_6$ plasma exposure followed by a PDA appears to be most successful in this.

Finally, the choice and most likely the deposition method of the metal gate can have a strong impact on the underlying gate stack. In the case of TiN, no significant difference has been observed between ALD and PVD deposition techniques. Replacing TiN by TaN results in a strong reduction of the average noise power spectral density. One of the key mechanisms is the oxygen scavenging potential of the metal in direct contact with the gate dielectric.

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