A Hybrid Switching Modulation of Isolated Bidirectional DC-DC Converter for Energy Storage System in DC Microgrid.

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ABSTRACT Isolated bi-direction DC-DC converters are widely used for energy storage systems (ESS) of DC microgrids. Particularly, a current-fed isolated bi-directional DC-DC converter (CF-IBDC) receives much attention due to its merits such as the naturally attenuated current ripple on the battery side. However, high efficiency cannot be obtained at the light and heavy load conditions under the conventional control methods. In this paper, a hybrid switching modulation is proposed to improve the power conversion efficiency of the CF-IBDC under light and heavy load conditions. The duty cycle of the secondary sides and the phase shift angle are independently controlled according to the amount of the transferred power. The control strategy is based on the optimization of zero-voltage switching (ZVS) conditions and the minimization of the circulating current in the power converter. Using the proposed control algorithm, the ZVS capability can be obtained under the entire load condition, and the circulating current can be minimized under the single phase-shift modulation (SPSM). Experimental results with a 1-kW laboratory prototype CF-IBDC validate the effectiveness of the proposed modulation algorithm.

INDEX TERMS Current-fed topology, Bidirectional DC-DC converter, Pulse-width modulation, Single phase shift modulation, Hybrid control strategy, Battery applications.

I. INTRODUCTION

Since renewable energy resources are required for DC microgrids, and developed energy from energy resources is commonly irregular due to various operating conditions such as weather and temperature. Therefore, an energy storage system (ESS) is essential to ensure the power quality and the reliability of the power supply. To interface the ESS with the DC microgrid, an isolated bi-directional DC-DC converter is used to charge and discharge batteries in the ESS system [1]-[3]. Since the ESS consists of many battery cells which have low voltage ratings and variable voltage ranges, an appropriate converter should handle the wide voltage range and high power conversion efficiency.

Under the single phase-shift modulation (SPSM) due to the inherent zero-voltage switching (ZVS) capability and the simple control algorithm with seamless bi-directional power flow capability, a voltage-fed dual-active-bridge (VF-DAB) converter is widely adopted to bi-directional applications [4]-[7]. However, this control strategy has drawbacks such as circulating current and backflow power in the VF-DAB converter under heavy load conditions [8]-[9]. In addition, since the inductor current is highly sensitive to voltage gain and load conditions, the ZVS can be failed under light load conditions. In particular, the circulating current rapidly increases and the non-ZVS range is extended in the operating region far from the unity voltage gain.

To overcome the limitations of the SPSM, many control strategies such as pulse width modulation plus phase-shift [10]-[12], extended phase-shift,[13], dual phase-shift [14],[15] and triple phase-shift [16]-[18] modulations are proposed. By introducing internal phase-shift (PS) between the two legs of full-bridges, three-level ac waveforms on the phase voltage can be generated, so that the length of a
zero-vector can be adjusted. The key technique of those modulations is to extend the degree of freedom (DoF) of the control strategy which expands the soft-switching range and reduces the circulating current, thereby reducing the conduction loss. Although ZVS can be achieved over wide load ranges using various modulation schemes, it is difficult to obtain full ZVS capability over the entire load range because of the high complexity of its implementation [15]. Since there are lots of DoFs, including the internal phase shift of the primary bridge, the internal phase shift of the secondary bridge, and the external phase shift between two ac voltages, linear interpolation can be used to determine the selection of the variables based on the lookup table in the digital signal processor (DSP). However, it can degrade the system’s dynamic response.

Furthermore, the characteristics of the VF-DAB converter are not suitable for charging and discharging batteries, which requires the power conversion capability for wide voltage ranges. This is because of a relatively high current ripple from the capacitive output filter of the VF-DAB converter, which adversely affects battery life. Therefore, the VF-DAB converter should not be used directly for the battery interface and a power filter should be connected between the battery and the converter.

As shown in Fig. 1, a current-fed isolated bi-directional DC-DC converter (CF-IBDC) consists of a synchronized buck/boost converter cascaded with the DAB converter including equivalent resistance [19]. The CF-IBDC is suitable for the interface between the battery and the high-voltage DC bus since it has the power conversion availability for the wide voltage range, small output voltage ripple, and high-power conversion efficiency. Comparing with the VF-DAB converter, the CF-IBDC can expand the ZVS region under a wide voltage range since the synchronized buck/boost converter controls the output voltage based on PWM control, and it makes the effective gain of CF-IBDC unity. Also, the current-fed structure can make the current ripple in the battery side attenuated naturally, which can prolong the lifetime of energy storage.

To control the CF-IBDC over the wide-range voltage, a PWM plus phase shift (PPS) control has been proposed [20]. The output voltage is controlled by the clamping operation using the PWM technique on the low voltage side (LVS), while the duty ratio is fixed as 50% on the high voltage side (HVS). The bi-directional power flow is controlled by phase-shift modulation (PSM) between H-bridges. However, under the light load condition, the power conversion efficiency can be poor since high current spikes and high circulating current are induced. To overcome the PPS, a PWM plus dual phase-shift (PPDPS) was proposed to reduce the conduction loss [21]. However, ZVS cannot be obtained over the entire load range. The asymmetric PPDPS control is proposed in [22] to reduce the peak current and the circulating current, but only the zero current switching (ZCS) can be achieved instead of ZVS in HVS, which increases switching losses. In [23], a modified PWM plus phase-shift (MPPS) modulation is proposed to reduce conduction losses, but ZVS cannot be achieved under light load conditions. In [24], a fixed duty control between H-bridges is proposed to obtain ZVS capability of all the switches even under no-load conditions; however, in the heavy load condition, the circulating current increases due to the existence of zero-vectors in HVS by using the modulation method used in [24].

In this paper, a hybrid switching modulation of the CF-IBDC is proposed to improve power conversion efficiency and reduce the computational burden of the control algorithm. The model analysis based on mathematical approaches is presented. The circulating current and ZVS conditions are also analyzed. The structure of this paper is as follows: In Section 2, the operational principles of the proposed hybrid switching modulation are given. In Section 3, the circulating current based on peak current, RMS current, and ZVS conditions are presented. Also, the design considerations are analyzed. In Section 4, experimental results verify the validity and the performance enhancement of the proposed hybrid switching modulation and control algorithm using a 1-kW prototype CF-IBDC. Section 5 provides a conclusion.

II. OPERATION PRINCIPLES

The schematic of the CF-IBDC is illustrated in Fig. 1. In the LVS, there are two DC inductors of \( L_{DC1} \) and \( L_{DC2} \) which make up the interleaved and synchronized bi-directional buck/boost converter. It is assumed that \( L_{DC1} = L_{DC2} \) is achieved in this paper. The inductance \( L_s \) represents the coupling inductance, which is coupled between the leakage inductance in the transformer and the external series inductance. The phase voltage of the LVS and the HVS is defined as \( v_{ab} \) and \( v_{cd} \), respectively. The clamping capacitor is defined as \( C_C \). The phase-shift angle between \( v_{ab} \) and \( v_{cd} \) is normalized by \( \pi \) and defined as \( \phi_{PS} (= \phi/\pi) \).

A. OPERATION PRINCIPLES OF VOLTAGE MATCHING CONTROL

Fig. 2 shows the waveforms of the steady-state operations using the proposed modulation strategies for the CF-IBDC. The synchronized buck/boost converter can match the voltage gain of \( m (=v_{Cf}/V_0) \) as 1 when \( V_{bat} \) widely fluctuates during the charging and discharging process. On the LVS, \( S1-S6 \) control to help the clamping voltage of \( V_C \) to match the output voltage. The battery
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**FIGURE 2. Proposed modulation strategy for the CF-IBDC.**

Voltage of $V_{bat}$ is controlled to $V_{C_{2}} (= V_{O(n)}$) by using the PWM control of bottom switches, $D_i$ where $n$ is the turn ratio of the transformer. The relationship between $V_{C_{2}}$ and $V_{bat}$ is expressed as shown in (1).

$$V_{C_{2}} = \frac{V_{bat}}{1 - D_i} \quad (1)$$

Even if the unity voltage gain is not optimal in terms of the RMS phase current, the converter can achieve ZVS of all the switches at the light load when the voltage gain is unity [18]. Besides, if the gain is not unity voltage gain, the slew rate of the phase current will be steep, causing a high current spike and circulating loss. Therefore, to reduce both the switching loss and the conduction loss, the voltage gain of $m$ is set as one in this paper and the slew rate of the phase current is zero during the positive or negative voltage overlapped period in $v_{ab}$ and $v_{cd}$.

In Fig. 2, the phase voltage of the LVS and the HVS is indicated as red and blue lines of three-level waveforms, respectively. To control the length of zero-vector on each side, an asymmetrical PWM control is employed in the LVS, and an inner phase shift between legs of the H-bridge is adopted in the HVS. The duty ratio of the HVS is defined as $D_2$, which is like the duty ratio of the LVS. The zero-vectors duration of the phase voltage on the primary and secondary is defined as $Z_{pri}$ and $Z_{sec}$, which are free-wheeling time intervals expressed as follows:

$$Z_{pri} = D_2T - \frac{T}{2}, \quad Z_{sec} = D_2T - \frac{T}{2} \quad (2)$$

The difference between $Z_{pri}$ and $Z_{sec}$ is redefined as $Z_d$. The non-overlapped period between the LVS and the HVS is defined as $T_{S1}$ and $T_{S2}$, respectively. The relation between $T_{S1}$ and $T_{S2}$ is expressed as follows:

$$\begin{align*}
T_{S1} - T_{S2} &= T(D_1 - D_2) = Z_d \\
T_{S1} + T_{S2} &= \phi T = \frac{\phi_{PS} T}{2}
\end{align*} \quad (3)$$

As following [19]-[23], many patterns have already been proposed to control the CF-IBDC using the three-level waveforms of both bridges; however, those have the following disadvantages. In the case of $D_1 < D_2$, ZVS cannot be achieved even under medium load conditions due to not enough current for soft switching.

In addition, the transferred power is also limited even if the phase-shift angle increases. Besides, under the heavy load condition, even though ZVS can be achieved, the circulating current is high to make power conversion efficiency decrease. Therefore, the case of $D_1 < D_2$ is not considered in this analysis. The theoretical concept of the proposed control algorithm is shown in Fig. 3, in which ZVS can be achieved in all the switches with low conduction loss by a small circulating current. The mode can be divided into four modes according to the output power. Each mode is controlled by only one parameter which is duty ratio or phase shift.

**B. ANALYSIS OF KEY OPERATION**

The power delivered from the LVS to the HVS is defined as a forward bias, whereas the power transmission from the HVS to the LVS is defined as a reverse bias. Since the forward and reverse bias are symmetric, only the forward bias is chosen as an example for the analysis in this paper. In addition, since the operating waveforms are repeated every half cycle with opposite polarity, the analysis of the phase current is only obtained in a half switching period. Finally, the reverse bias can be analyzed in the same way.

1) **LIGHT-LOAD (LL)- I OPERATION**

In many CF-IBDC-related papers, it has been difficult to satisfy ZVS conditions at no-load or very light load conditions. In [24], an effective modulation method was proposed to achieve ZVS even under no-load conditions. However, this method is not suitable for heavy load conditions due to the existence of the zero-voltage vector on the HVS regardless of load conditions, resulting in high circulating current and high reactive power in the converter. Therefore, the algorithm shown in [24] is employed in the proposed algorithm only for light load conditions.

Fig.3-(a) shows the steady-state waveforms of the proposed algorithm under very light load conditions. In the light load (LL-I) condition, to generate the bias current, the magnitude of $Z_d$ is selected at a positive constant value as $T(D_1 - D_2)$. It makes the active switches of the HVS enable ZVS operations. Based on Fig. 3-(a), specific times of $t_0$, $t_1$, $t_2$, $t_1$, and $t_4$ can be represented by $D_1$, $D_2$, and $\phi_{PS}$ as shown in (4).
The phase current can be derived by (5) per period.

\[
\Delta I_{D} = \frac{V_{C}}{L_{s}} \Delta t
\]  

(5)

The current of \( I_1 \) and \( I_2 \) in Fig. 3-(a) can be expressed as (6).

\[
\begin{align*}
I_1 &= \frac{V_{C}}{2L_{s}f_{S}} \phi_{PS} \\
I_2 &= \frac{V_{C}}{2L_{s}} (1 - D_2 - \phi_{PS}) \left( \frac{T}{2} \right)
\end{align*}
\]  

(6)

The current of \( I_1 \) is only associated with variable \( \phi_{PS} \), and \( I_2 \) is only associated with variable \( Z_d \).

The output power in LL-I mode is expressed as shown in (7).

\[
P_o = \frac{2}{T} \int_{0}^{T} \frac{V_{C}}{L_{s}f_{S}} (1 - D_1) \phi_{PS} dt
\]  

(7)

The output power is only associated with \( D_1 \) and \( \phi_{PS} \). The peak phase current in the LL-I mode is represented as \( I_2 \) where it depends on \( D_1 \) and \( D_2 \). In the case of the duty ratio \( D_2 \) is changed depending on \( D_1 \) to maintain the constant value of \( Z_d \). Due to \( D_1 \) is controlled by the battery voltage, to reduce the RMS current and peak current, \( Z_d \) should be reduced. The design process of \( Z_d \) is introduced in Section 3 with the ZVS conditions of the HVS. The phase angle of this mode has the range as follows:

\[
0 \leq \phi_{PS} \leq (D_1 - D_2)
\]  

(8)

2) LIGHT-LOAD (LL) - II OPERATION

When \( \phi_{PS} \) reaches \((D_1 - D_2)\), the operating mode is changed to the light-load II (LL-II). As shown in Fig. 3-(b), this mode is the same as the PPDPS mode but the magnitude of \( D_2 \) depends on \( D_1 \) to maintain the fixed \( Z_d \) in the LL-I mode, which is the extended LL-I mode. According to Fig. 3-(b), \( t_0 \), \( t_1 \), \( t_2 \), \( t_3 \), and \( t_4 \) can be represented by \( D_1 \), \( D_2 \), and \( \phi_{PS} \) as follows:

\[
\begin{align*}
t_0 &= 0 \\
t_1 - t_0 &= t_1 = \left( \frac{D_1 - 1}{2} \right) T \\
t_2 - t_1 &= \frac{T}{2} (D_1 - D_2 - \phi_{PS}) \\
t_3 - t_2 &= (1 - D_2) T \\
t_4 &= \frac{T}{2}
\end{align*}
\]  

(9)
The transmitted power in the LL-II mode is expressed as

\[
P = \frac{V_c^2}{4L_f} \left[-\phi_{PS}^2 + 2(2-D_1-D_2)\phi_{PS} - (D_1-D_2)^2\right]
\]

The transmitted power is related to \(D_1\) and \(\phi_{PS}\) in the LL-II mode as same as the LL-I mode. \(I_1\) and \(I_2\) in Fig. 3-(b) can be expressed as (6). Even if \(I_1\) and \(I_2\) in the LL-II mode are the same as the LL-I mode, the peak current is changed from \(I_2\) to \(I_1\) as \(\phi_{PS}\) increases. The amplitude of \(I_1\) does not change since \(I_2\) depends on \(Z_{dc}\), which is held in overall LL mode. When \(\phi_{PS}\) arrives at half of \(Z_{mii}\), half of \(Z_{dc}\) is the same as \(T_{S2}\).

In this mode, the phase angle is in the range expressed by (11).

\[
(D_1 - D_2) \leq \phi_{PS} \leq D_1 - \frac{1}{2}
\]

Therefore, \(D_1\) and \(D_2\) should be longer than 0.5+(\(D_1\)-\(D_2\)) and 0.5 to obtain the LL-II mode, respectively. Here, the range of \(D_1\) is limited to as narrow as possible since the range of \(D_1\) is proportional to the circulating current range. The circulating current can be minimized when \(D_1\) is 0.5; however, to obtain the ZVS capability, the minimum value of \(D_1\) should be greater than 0.5.

3) MEDIUM-LOAD (ML) OPERATION

When \(\phi_{PS}\) is arrived at (\(D_1\)-1/2), the entire LL mode is finished, and the operating mode is changed to the medium-load (ML) mode. As the middle between the LL mode and the heavy-load (HL) mode, the ML mode connects the two modes smoothly. In the ML mode, \(D_1\) is controlled to regulate the output voltage based on the PMW control of \(D_2\) by using an inner PS modulation of the HVS. Fig. 4 shows the theoretical concept of the ML mode as output power increases. Since the waveforms of the phase voltage and the phase current in the ML mode are the same as the LL-II mode, the time interval is equivalent, which is represented in (6). The current of \(I_1\) and \(I_2\) in Fig. 3-(c) can be expressed as (12).

\[
\begin{align*}
I_1 &= \frac{V_c}{2L_f} \phi_{PS} = \frac{V_c(2D_1-1)}{4L_f} \\
I_2 &= \frac{V_c(D_2-D_1)}{2L_f}
\end{align*}
\]

In the ML mode, since \(\phi_{PS}\) is fixed, the amplitude of \(I_1\) does not change unless the battery voltage alters. Being different from the entire LL mode, \(I_2\) is changed during the ML mode. When \(D_2\) decreases until 0.5, \(I_2\) increases. The transmitted power in the ML mode is expressed as shown in (13).

\[
P = \frac{V_c^2}{4L_f} \left(-D_1^2 + 4D_2^2 + 6D_1 - \frac{9}{4}\right)
\]

From (13), since \(\phi_{PS}\) is held as (\(D_1\)-1/2) in the ML mode, the output power is only associated with \(D_1\) and \(D_2\). Before the ML mode, \(D_2\) changes according to \(D_1\) to maintain a constant \(Z_{dc}\) while \(D_2\) in the ML mode actively changes to regulate the output voltage.

As shown in Fig. 5, when \(D_2\) decreases, the transferred power increases, and the maximum power can be obtained when \(D_2\) is 0.5 in the ML mode regardless of \(D_1\). It should be noted that the several combinations of \(D_1\) and \(D_2\) are possible to transmit power to the backward bias. In Fig. 5, a gray plane shows delivered power zero. This is because \(D_2\) in the ML mode can decrease to 0.5 regardless of \(D_1\), which does not satisfy (11). Therefore, the proper range of \(D_1\) is also required with the consideration of \(D_2\). The intuitive criterion of mode change from the ML mode to the HL mode is the length of \(D_2\). When \(D_2\) reaches 0.5, the mode changes.

4) HEAVY-LOAD (HL) OPERATION

As shown in Fig. 3-(d), in the HL mode, the secondary phase voltage is a square waveform, and the transmitted power is controlled by only \(\phi_{PS}\) control. This control strategy is the same as conventional PPS control. The time
interval $t_0$, $t_1$, $t_2$, and $t_3$ can be represented only by $D_1$ and $\phi_{PS}$ as follows:

$$
\begin{align*}
& t_0 = 0 \\
& t_1 - t_0 = t_1 = \frac{T}{2} \left( \frac{1}{2} - D_1 + \phi_{PS} \right) \\
& t_2 - t_1 = \frac{T}{2} \left( \frac{3}{2} - (D_1 + \phi_{PS}) \right) \\
& t_3 = \frac{T}{2}
\end{align*}
$$

(14)

In addition, $I_1$ and $I_2$ in Fig. 3-(d) can be expressed as (15).

$$
\begin{align*}
I_1 & = \frac{V_c}{2L_N f_s} - \phi_{PS} \\
I_2 & = \frac{V_c}{2L_N f_s} (2D_1 - 1 - \phi_{PS})
\end{align*}
$$

(15)

Since, in the ML mode, $\phi_{PS}$ is fixed to $(D_1 - 1/2)$, the output power consisting of $D_1$ and $D_2$ can be reorganized in terms of $\phi_{PS}$, which is expressed as follows:

$$
P = \frac{V_c^2}{4L_N f_s} \left( -4D_1^2 + 6D_1 - 2 \right) = \frac{V_c^2}{4L_N f_s} \left( -4\phi_{PS}^2 + 2\phi_{PS} \right)
$$

(16)

From (16), the maximum power can be obtained when $\phi_{PS}$ is 0.25. In the HL mode, the range of the phase angle is expressed by (17).

$$
D_1 - \frac{1}{2} \leq \phi_{PS} \leq \frac{1}{4}
$$

(17)

To satisfy (17), $D_1$ is limited to 0.75. Finally, to protect the reverse power transmission, the proper range of $D_1$ is limited as (18).

#### C. CONTROL STRATEGY OF THE PROPOSED OPERATING MODE

Fig. 6 shows the phase voltage and the phase current waveforms under the various control modulations according to the load conditions. In Fig. 6-(a) and Fig. 6-(b), a high peak current occurs under the light load condition, resulting in high conduction loss and core loss. When the PPDPS with the fixed $Z_d$ in Fig. 6-(c) is alternatively employed in this paper under the light load condition, power loss can be reduced since the duration of high peak current ends only when $\phi_{PS}$ reaches $Z_d/2$.

Meanwhile, the shaded area in Fig. 6 shows the circulating current of the phase current due to the zero-vector of the HVS. For the proposed control strategy in the HL mode, the PPS method is shown in Fig. 6-(d) is adopted to reduce the circulating current. Since the PPS method can eliminate the zero-vector on the HVS under the heavy load condition, it can minimize circulating current and reactive power compared with Fig. 6-(e) and Fig. 6-(f). As shown in Fig. 6-(e), when the PPDPS is employed, the non-power transmission region is extended as power increases. The PPDPS with the fixed $Z_d$ under the heavy load condition shown in Fig. 6-(f) also has the same problem since the zero-vector on the HVS is maintained continuously. This is the reason why the fixed $Z_d$ with the PPDPS is limited to be used only in the light load condition. The ML mode is an intermediate process from the LL mode to the HL mode. Since in the ML mode, the PWM of $D_2$ is only used to control the output power, the PPDPS with the fixed $Z_d$ at the light load condition can be smoothly changed to the PPS control as power increases with the simple control strategy.

Fig. 7 shows the control diagram of the CF-IBDC based on the proposed algorithm. Two control loop controllers are required to implement: the clamping voltage control loop ($G_{vc}(s)$) and an output voltage control loop ($G_{vo}(s)$ & $G_{d}(s)$). The clamping voltage control loop is required for voltage matching control with the reference of $V_{in}$ based on the modulation of $D_1$. The output voltage control loop consists of a dual closed-loop system. The inner-control loop is essential to control the battery current. The outer-control loop is used to control power flows, which is based on the adjustment of $\phi_{PS}$ and $D_2$. The output of the outer-control loop of $G_{vo}(s)$ is the reference of the inner-control loop. The control variables of $\phi_{PS}$ and $D_2$ are independently controlled by considerations of the ZVS operation and the minimization of the circulating current and the simple control strategy.
Fig. 8 shows the trajectory for the output power when the value of $D_1$ is different from the proposed control modulation where $V_O = 380 V$, $V_{CC} = 127 V$, $L_S = 20 \mu H$, $V_{bat} = 48 - 60 V$, and $f_S = 50 kHz$. As shown in Fig. 8, the control variables of $D_2$ and $\phi_{PS}$ can be separated and be individually controlled, making transmitted power increases smoothly and seamlessly. The maximum power can be obtained when $\phi_{PS}$ is 0.25, and $D_2$ is 0.5. As $D_1$ is smaller, the region of the LL-II and the ML mode is reduced, and the range of the HL mode is extended. As the increase in the time interval of LL-II and the ML mode under the same power conditions, the circulating time is extended, resulting in reactive power and conduction losses increased. In order words, to obtain high efficiency, the duration of the LL-II and the ML mode should be minimized. Therefore, although the maximum value of $D_1$ is calculated as 0.75 from (18), the CF-IBDC converter operates under the $D_1$ range as narrow as possible.

### III. EFFECTIVE HARDWARE DESIGN STRATEGY

When handling the application of the wide voltage range applications such as ESS, there is commonly a trade-off between the conduction loss and the switching loss. Therefore, careful design considerations are required to obtain the high performance of the CF-IBDC.

#### A. ANALYSIS OF CURRENT STRESS

1) **PEAK OF PHASE CURRENT**

The peak current has a significant effect on the RMS current and it also relates to the core loss of the transformer and extra series coupling inductance. To improve the efficiency, the conduction loss, and the core loss in the CF-IBDC should be minimized. Based on the analysis of peak phase current, the tendency of the conduction loss and the core loss can be estimated. The peak phase current shown in Fig. 3 can be derived as follows:

$$V_{CC}Z_d, \quad 0 \leq \phi_{PS} < (D_1 - D_2) \quad \& \quad D_2 = (D_1 - Z_d)$$

$$V_{CC} = \frac{2L_S}{D_2}, \quad (D_1 - D_2) \leq \phi_{PS} < (D_1 - \frac{1}{2}) \quad \& \quad D_2 = (D_1 - Z_d)$$

$$V_{CC} = \frac{2D_1 - 1}{4L_S f_S}, \quad \phi_{PS} = (D_1 - \frac{1}{2}) \quad \& \quad (D_1 - Z_d) \leq D_2 \leq \frac{1}{2}$$

$$V_{CC} = \frac{2L_S f_S}{\phi_{PS}}, \quad (D_1 - \frac{1}{2}) \leq \phi_{PS} \leq \frac{1}{4} \quad \& \quad D_2 = \frac{1}{2}$$

From (19), the peak current is expressed as the function of $Z_d$, $D_1$, and $\phi_{PS}$. Since the proposed algorithm is employed to the PPDPS with a fixed $Z_d$ at light load conditions and the PPS algorithm at heavy load conditions, the peak current at the light load and the heavy load is equal to each control method. Therefore, the proposed algorithm has a low peak current over the entire load range compared with the conventional control strategies.

2) **DISCUSSION OF PHASE CURRENT IN CIRCULATING TIME INTERVAL**

As shown in Fig. 9, each waveform represents non-active power transfer stages shown in the shadowed area, which depends on the load conditions and the modulation methods. Since the proposed algorithm consists of the PPDPS with the fixed $Z_d$ control in the LL mode, PWM of $D_2$ control in

**FIGURE. 7.** Control diagram for the proposed current-fed bi-directional DC-DC converter.

**FIGURE. 8.** Trajectories for output power versus $D_1$ and $\phi_{PS}$ according to the proposed modulation strategy.

**FIGURE. 9.** Time interval of circulating current according to $D_1$ and $D_2$ at LL mode: (a) Case of large $D_1$ and $D_2$, (b) Case of small $D_1$ and $D_2$. **FIGURE. 8.** Control diagram for the proposed current-fed bi-directional DC-DC converter.
the ML mode, and PPS control in the HL mode, respectively, the circulating current is required to be analyzed for each mode. For the simplification of the analysis, when the dead time of the gate signal and the resonance between the output capacitance of the power switches and the coupling inductance is negligible, the circulating current in the LL-I mode can be expressed as (20).

\[
i_{c,LL-I} = \frac{V_C}{2L_s} \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} ; \quad 0 < t < \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} (20)\]

\[
i_{c,LL-II} = \frac{V_C}{2L_s} \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2}; \quad \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} < t < \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} (21)\]

The RMS value of the circulating current in the LL-I mode can be derived as follows:

\[
i_{c,RMS,LL-I} = \frac{1}{\sqrt{2}} \int_{0}^{T} i_{c,LL-I}^2 (t) dt = V_C \frac{Z_{pr}}{2L_s} \sqrt{3} T (21)\]

where \(i_{c,RMS,LL-I}\) is the RMS value of the circulating current during the LL-I mode, \(i_{c,LL-I}\) is the circulating current expressed in (18). In the same way, the circulating current in the LL-II mode and the ML mode can be derived as shown in (22).

\[
i_{c,LL-II} = \frac{V_C}{2L_s} \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2}; \quad \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} < t < \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} (22)\]

\[
i_{c,ML} = \frac{V_C}{L_s} \left( \frac{Z_{pr}}{2} + t - \frac{\phi_{ps} T}{2} \right); \quad \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} < t < \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} (23)\]

The RMS value of the circulating current at the LL-II mode can be obtained as shown in (23).

\[
i_{c,ML} = V_C \frac{Z_{pr}}{2L_s} \left( \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} \right) \left( \frac{\phi_{ps} T}{2} + \frac{Z_{pr}}{2} \right) (23)\]

Since the shape of the phase current is the same as the case of the LL-II mode, the circulating current and the RMS current can be obtained by replacing \(Z_{pr}\) with \((D_1-D_2)T\) in (22) and (23). Since the zero-vector in HVS is zero in the HL mode, the circulation time interval does not exist. As shown in Fig. 6, even if the peak current shown in Fig. 6-(c) is lower than that shown in Fig. 6-(a) and Fig. 6-(b), the circulating time interval in Fig. 6-(c) is larger than that in Fig. 6-(a) and Fig. 6-(b). Therefore, the proper range of \(D_2\) should be decided. Fig. 9 shows the circulating region according to \(D_2\). As \(D_2\) is set from 0.5, the circulating time interval increases. Since the value of \(D_2\) at the LL mode is determined by \(D_1\), the maximum value of \(D_1\) should be as small as possible with a suitable voltage matching control strategy.

B. ANALYSIS OF SOFT SWITCHING CONDITIONS

1) LOW VOLTAGE SIDE (LVS)

Since the CF-IBDC should handle the wide range voltage, the current-fed structure of the battery connected side and the DC bus interface is used as shown in Fig. 1. Therefore, the ZVS condition is different from each side. Fig. 10 shows theoretical switching waveforms in the LVS containing the DC filter current and the dead time duration. In Fig. 10, the maximum and minimum values of the DC filter inductor current are indicated by the phase current. The ZVS criteria of the power switches are indicated as blue circles. Since the switch current in the LVS is related to the filter current, the output capacitance of the switches in the LVS, \(C_{oes,LVS}\), is charged and discharged by the current difference between \(i_{DC}\) and \(i_{t}\) during the dead time. The ZVS conditions can be derived by the relationship between the phase current and the filter current as follows:

\[
i_{LS} > 2C_{es,LVS} V_C \Delta \left( \frac{t_d}{t} \right) = I_{min,req,L} (24)\]

\[
i_{LS} > 2C_{es,LVS} V_C \Delta \left( \frac{t_d}{t} \right) = I_{min,req,L} (24)\]

\[
i_{DC} = I_{DC,max} - I_{DC,min} > I_{min,req,L} (24)\]

\[
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\[
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The ZVS conditions can be derived by the relationship between the phase current and the filter current as follows:

\[
i_{LS} > 2C_{es,LVS} V_C \Delta \left( \frac{t_d}{t} \right) = I_{min,req,L} (24)\]

\[
i_{LS} > 2C_{es,LVS} V_C \Delta \left( \frac{t_d}{t} \right) = I_{min,req,L} (24)\]

\[
i_{DC} = I_{DC,max} - I_{DC,min} > I_{min,req,L} (24)\]

\[
i_{DC} = I_{DC,max} - I_{DC,min} > I_{min,req,L} (24)\]

\[
i_{DC} = I_{DC,max} - I_{DC,min} > I_{min,req,L} (24)\]

where \(I_d\) is the dead time duration, \(I_{DC,max}\) and \(I_{DC,min}\) are the maximum and minimum value of the DC filter current, respectively, and \(I_{min,req,L}\) is the desired minimum current for fully charging or discharging \(C_{oes,LVS}\). The maximum and minimum values of the DC filter current can be expressed as follows:

\[
i_{DC,max} = I_{DC} = \frac{V_C}{2L_{DC,F}} \left( 1 - D_1 \right) (25)\]

\[
i_{DC,max} = I_{DC} = \frac{V_C}{2L_{DC,F}} \left( 1 - D_1 \right) (25)\]

\[
i_{DC,max} = I_{DC} = \frac{V_C}{2L_{DC,F}} \left( 1 - D_1 \right) (25)\]

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Fig. 11 shows the criteria of the DC filter inductance for the ZVS capability according to $V_{bat}$ and output power. In Fig. 11, when the inductance is less than the boundary area, the ZVS capability in the LVS is obtained. It is most difficult to obtain the ZVS capability when $V_{bat} = 48$ V at the no-load condition. If $L_{DC1}$ and $L_{DC2}$ are small enough, the ZVS capability of the LVS switches can easily be obtained; however, the peak current and the RMS current of the DC filter increase, which causes high conduction loss. Therefore, the DC filter inductance should be designed as large as possible to obtain ZVS in the LVS.

1) HIGH VOLTAGE SIDE (HVS)

Being different from the ZVS condition of the LVS switches, that of the HVS switches only depends on the phase current. The basic ZVS condition of the HVS switches can be derived as follows:

\[
\begin{align*}
Q_1 & \cap Q_2 : \frac{i_{Ls}(t)}{\pi} > 2C_{oes,HVS}\frac{V_{increase}}{\Delta t_{res}} = I_{min,req,H} \\
Q_1 & \cap Q_2 : \frac{i_{Ls}(t)}{\pi} > I_{min,req,H}
\end{align*}
\]

where $C_{oes,HVS}$ is the output capacitance of the switches in the HVS and $I_{min,req,H}$ is the desired minimum current for fully charging and discharging of $C_{oes,HVS}$. Since, as shown in (27), the ZVS capability can be obtained by the phase current, the amplitude of the phase current at the switching moment is significant, which means that the ZVS can easily be achieved under not the light load condition but the heavy load condition in the CF-IBDC. This is the same as the performance issue in most of the DAB converters.

To overcome this limitation, the proposed control algorithm using the fixed $Z_d$ with the PPDPS is employed under the light load condition as shown in Fig. 3-(a). Fig. 12 shows the ZVS process in the HVS under the proposed control algorithm. Just as shown in Fig. 10, the ZVS criteria for each switch in the HVS are described as red circles. Difficult points for the ZVS condition are indicated as dotted circles. Details of the resonant time interval are also shown in Fig. 12 where $t_{res}$ is the resonant time duration between $C_{oes,HVS}$ and $L_s$. In Fig. 12-(a) and Fig. 12-(b), the DC currents of $I_{Ls,before,r}$ and $I_{Ls,after,r}$ are generated by the fixed $Z_d$ with the PPDPS in the LL-I mode and the LL-II mode, respectively. The current of $I_{Ls,before,r}$ indicates that the constant value before the resonance during the dead time, and it makes charging and discharging of the output capacitance of the HVS switches.

The most important consideration of selecting $Z_d$ is the minimum current, $I_{Ls,before,r}$, for charging/discharging the output capacitance of the power switches. As $Z_d$ increases, the amplitude of the minimum current increases, which can reduce ZVS failure. However, it also increases the conduction loss because of RMS current increment. This is the reason why the optimal value of $Z_d$ is required. In [24], the ZVS condition for the HVS switches with the fixed $Z_d$ is explained in detail by considering the resonant process and the parameter design of $\Delta T$. From [24], the length of $Z_d$ can be derived. The ZVS condition is that $I_{Ls,before,r}$ should be larger than zero at the fixed $Z_d$ as follows:
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\[

d_{res} \leq t_{res} \leq t_{res,\text{max}} = \pi \sqrt{\frac{2L_{CC,\text{HVS}}}{Z_d}} \tag{28}
\]

Even though the large \(Z_d\) can easily make the output capacitance of HVS switches charge and discharge, it makes long circulation time interval as analyzed above, which causes higher conduction loss, i.e., the trade-off between the switching loss and the circulation status. Meanwhile, as shown in Fig. 13, \(t_{res}\) should be shorter than \(t_d\) for obtaining full ZVS condition. Therefore, the dead time is desired to get the ZVS condition as shown in (29).

\[
t_{res} < t_d < t_{res,\text{max}} = \frac{\pi L_{CC,\text{LVS}}}{Z_d} \tag{29}
\]

Note that the dead time duration should be shorter than \(t_{d,\text{max}}\) to prevent capacitor voltage dumping where the resonant current flowing in the reverse direction again to charge the output capacitance.

### IV. EXPERIMENTAL RESULTS

Table I shows the parameter specifications of the CF-IBDC, which are used in analysis and experiment. A prototype of the CF-IBDC converter is shown in Fig. 13. It is composed of two DC inductors and an H-bridge which make the interleaved boost converter in the LVS. In the LVS, SUG80050E manufactured by VISHAY is selected as the power switch since it has a low \(R_{ds,on}\) of 5.4 m\(\Omega\) with 150 V rated voltage, resulting in decreasing conduction loss.

![Photograph of the proposed CF-IBDC converter prototype.](image1)

**TABLE I**

| Quantity | Value     |
|----------|-----------|
| PO       | 1-kW      |
| \(V_{bat}\) | 48 V–60 V |
| \(V_{CC}\) | 127 V     |
| \(V_{out}\) | 380 V     |
| \(D_1\)  | 0.527–0.622 |
| \(n\)    | 1:3       |
| \(f_s\)  | 50 kHz    |
| \(L_s\)  | 30 \(\mu\)H |
| \(C_{res,\text{LVS}}\) | 540 pF |
| \(C_{res,\text{HVS}}\) | 55 pF |
| \(Z_d\)  | 130 nsec  |
| \(L_{DC}\) | 120 \(\mu\)H |
| \(C_{O\text{HVS}}\) | 680 \(\mu\)F |
| \(S_1, S_2\) | SUG80050E |
| \(Q_1, Q_2\) | SCT3060KL |

![Steady-state operating waveforms using the proposed control algorithm under \(V_{bat} = 48\) V: (a) LL-I mode, (b) LL-II mode (c) ML mode (d) HL mode](image2)
In the HVS, a SiC MOSFET of SCT3060KL manufactured by ROHM is selected to reduce the junction capacitance which is 55 pF with 60 mΩ of $R_{\text{ds,on}}$. In addition, to reduce internal leakage inductance, a toroidal DC inductor core is employed due to its singularity: the closed concentric geometry [25]. According to the considerations of the ZVS condition and the conduction loss in section 3.2, each $L_{\text{DC}}$ is selected to 120 $\mu$H. From (26) and Fig. 12, $Z_i$ is selected to 130 ns, and the dead time duration of $t_d$ is selected around 0.3 $\mu$s. As the controller of TM320F28335 manufactured by TI is employed to control the proposed power converter.

1) STEADY-STATE OPERATING WAVEFORMS

Fig. 14 and Fig. 15 show the steady-state waveforms as the output current increases when $V_{\text{bat}}$ is fixed at 48 V and 60 V using the proposed hybrid control algorithm under the forward bias, respectively. Fig. 14 - (a) and Fig. 15 - (a) show the waveforms of the LL-I mode under the no-load condition. Based on the proposed hybrid algorithm, the DC bias current shown in Fig 12 is generated by $Z_d$, which allows the soft switching of the HVS switches. The LL-II mode is shown in Fig. 14 - (b) and Fig. 15 - (b). In the LL mode, $Z_i$ is maintained and $\phi_{PS}$ is controlled as power changes. When $\phi_{PS}$ reaches half of $Z_{pri}$, the ML mode in Fig. 14 - (c) and Fig. 15 - (c) starts. In Fig. 14, the ML mode starts at 550 W and ends at 800 W, while the ML mode in Fig. 15 starts at 300 W and ends at 400 W. As the output power increases, $D_2$ is going to 0.5 in the ML mode, which makes the duty of the secondary side be 0.5. After that, it moves to the HL mode, which is the same as the conventional PPS control. In the HL mode shown in Fig. 14 - (d) and Fig. 15 - (d), only $\phi_{PS}$ is controlled to regulate the output power.

The entire mode transition is smooth and seamless. The difference between Fig. 14 and Fig. 15 is only the time interval of the ML mode. In Fig. 14, it has a large portion of power transmission, while the ML mode shown in Fig. 15 is narrow. As $D_1$ is longer, the interval of ML mode becomes wider, resulting in relatively easy ZVS conditions. Since $D_2$ goes to 0.5 as the output power increases in the ML mode, the reactive power and the circulating current is reduced in the HL mode as shown in Fig. 6 and Fig. 9, respectively, resulting in the trapezoidal current waveform.

Fig. 16 illustrates the experimental measurements of a step load response from 200 W to 1-kW with $V_{\text{bat}} = 48$ V under the forward bias. Zoomed waveforms are shown on the right side, which operates under the LL mode (above) and the HL mode. The phase current passing through the LVS increases from 4.7 A to 23.2 A during the step load experiment. The undershoot of the output voltage is measured as around 10 V, which is 3% of the output voltage. The transient state returns to the steady state within about 25ms. It shows that the proposed CF-IBDC converter shows good dynamic performance and enough stability in the transient operation. Since the control variable changes
during the power transition from $\phi_{PS}$ to $D_2$ and from $D_2$ and $\phi_{PS}$, the transient time seems to be relatively long. However, as the proposed hybrid control algorithm can maximize the efficiency of battery applications. Using the uninterrupted power flow control of the entire load range with only a single control variable, the transient time duration of ESS is less important than the case of steady-state operations.

2) SOFT SWITCHING WAVEFORMS

Fig. 17 shows the double pulse test waveforms of power switches to verify the ZVS conditions of the proposed hybrid control algorithm. The worst case of the ZVS condition is the lowest battery voltage at the no-load condition. In Fig. 17, the gate voltage, the drain-to-source voltage, and the leakage inductor current of the bottom switches in the LVS of $S_4$ and the upper and bottom switches in the HVS of $Q_1$ and $Q_4$ are captured. As shown in Fig. 17, the soft-switching capability can be obtained even under the no-load condition with the lowest $V_{bus}$. The bias current of $I_{Ls,before}$ shown in Fig. 12 is selected as the smallest value to decrease the circulating current. The experimental waveforms demonstrate that the theoretical analysis in Section III.2 of the ZVS condition is well achieved for the full load range.

3) POWER CONVERSION EFFICIENCY

Fig. 18 shows the power conversion efficiency curves according to load and battery voltage variations. Fig. 18-(a) shows the comparison of power conversion efficiency between the proposed control algorithm (red line) and the conventional control algorithms of the PPS (green line) and the PPDPS with $\Delta T$ (blue line) when $V_{bat}$ is 48 V. Under the light load condition, the efficiency when the PPDPS with $\Delta T$ is employed is significantly higher than the case of the PPS control. This is because the ZVS can be achieved under the former control method under low RMS phase current. While, at the heavy load condition, the PPS modulation makes high efficiency compared with the PPDPS due to the decrement of the circulating current in the secondary side, which induces low conduction loss. Since the proposed algorithm is employed by the PPDPS with $\Delta T$ at the light load condition and by the PPS at the heavy load condition, the efficiency can be maximized. Therefore, the efficiency of the proposed algorithm is matched by PPDPS with $\Delta T$ under light load conditions, and by PPS under the heavy load condition, i.e., measured higher efficiency in most of the entire load range than the

![Power Conversion Curve](image)

**FIGURE 17.** Experimental waveforms of double pulse test for power switches under the worst case of ZVS condition under $V_{bus} = 48$ V at no load condition: (a) Bottom switches of $S_4$ in LVS, (b) Upper switches of $Q_1$ in HVS, (c) Bottom switches of $Q_4$ in HVS

**FIGURE 18.** Power conversion efficiency curves: (a) Comparison between the proposed and conventional algorithms, (b) According to battery voltage
vi. conclusion

This paper proposes the effective hybrid switching modulation to overcome the limitations of the existing control algorithm and to improve the power conversion efficiency under the light and heavy load conditions of the CF-IBDC. By adopting the fixed $Z_d$ and designing DC-filter based on the theoretical analysis at light load conditions, the entire ZVS range can be guaranteed. To minimize the circulating current and the reactive power, the duty cycle of the secondary sides is changed according to load conditions. In addition, the proposed hybrid algorithm controls the decoupled duty cycle of the secondary sides and the phase shift angle between the primary and secondary sides, which can mitigate control complexity.

The effectiveness of the proposed hybrid control algorithm is verified by the prototype of 1 kW CF-IBDC from 48 to 60 V of $V_{bat}$ at 380 V of $V_{out}$. The ZVS conditions of all the power switches are verified using the double pulse test. The performance of the proposed control algorithm is also verified by the steady-state operation and the dynamic response. Based on the experimental results with the proposed hybrid algorithm, the efficiency of both light and heavy load conditions is improved to 3.3 % and 1.8 %, respectively, compared with the conventional control algorithms. The highest efficiency is measured as 96.67% at 800 W under $V_{bat} = 60$ V and the effectiveness of the proposed switching pattern is demonstrated.

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