Research and Design of High-Speed Camera Trigger Circuit for Arc Welding Monitoring System

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Abstract. Based on the change of current waveform during arc welding short-circuit transition process, a trigger circuit is designed to trigger the shutter of high-speed camera in arc welding monitoring system with the core of FPGA, which can solve the trigger timing problem of the camera, and obtain clear and non-interference photos and videos, which have been verified in experiments.

1. Introduction
At present, CO2 gas shielded welding is one of the most commonly used gas shielded welding methods in welding process. Short-circuit transfer is mainly used in thin wire CO2 gas shielded welding below 1.6mm. The dynamic waveform of arc voltage and current in short circuit transition is shown in Fig. 1 [1]. In CO2 shielded welding, because of the strong oxidation of CO2 gas itself, the alloy elements will be burned during the welding process, so that the pool image obtained by arc welding monitoring system is disturbed by strong arc light and smoke, and the noise and stain are serious. Common arc welding monitoring system mainly consists of high-speed electronic camera, data acquisition card, computer system and image processing software. Clear welding pool image acquisition and analysis can improve the stability of welding arc, improve weld formation, reduce metal spatter, improve welding quality and productivity, and realize welding automation is of great significance.

In Figure 1, T is a short circuit period, t1 is arcing time, t2 is arc extinguishing time, t3 is voltage recovery time after droplet breaking, T= t1 + t2 + t3. The short-circuit transition frequency is generally 20-200 HZ, and the current is generally 80-200 A. The welding pool image is taken by the high-speed camera of the monitoring system. The trigger of the high-speed camera shutter can be set by the trigger circuit of the camera itself in the camera software. However, camera software can only set the trigger frequency or time interval when the camera shutter is opened. If the camera is photographed during the arc time t1, because of the existence of arc and splash, the image taken by the camera will be disturbed by arc and splash, resulting in ambiguity, as shown in Figure 2.

In view of the above phenomena, a special trigger circuit can be designed to replace the trigger circuit of the camera itself. In the short-circuit arc extinguishing time T2 without arc and spatter, trigger pulse can be generated to trigger the camera to take photos, and clear and undisturbed image information can be obtained. According to Figure 1, it can be seen that it is easier to process in t2 period according to the change of current.
2. Scheme and circuit design
The system hardware block diagram is shown in Fig. 3.

2.1. Current sensor and impedance matching circuit
The advantage of Hall current sensor is that the primary side and the secondary side are completely isolated. The signal shaping circuit has been integrated in the current transformer U5. The output voltage is directly the voltage, and the output voltage changes linearly with the input current.

Figure 1. Dynamic waveform of arc voltage and current in short circuit transition

Figure 2. Weld pool image (The camera itself triggers)

Figure 3. system hardware block diagram
Because the 5 m 4 core shielded wire is used between the sensor and the signal processing circuit to transmit the signal and provide auxiliary power for the sensor, the joint attenuation in the signal circuit makes it difficult to avoid strong interference in the industrial production environment, so the impedance matching circuit is very necessary. In this design, the welding current signal is 50-200 HZ AC signal, so the isolation capacitor C10 is used. Straight isolation, R19 determines DC 1.6V bias potential, and the input impedance of the system reaches 100K level. U3B is a voltage follower consisting of a first-stage LM358 to reduce the influence of the latter circuit on the input impedance. The circuit is shown in Fig. 4.

2.2. Controllable gain amplifier circuit
Controllable gain amplifier adopts AD603. Voltage gain can be determined by differential mode voltage of Gpos and Gneg foot. FDBK foot and Vout foot are joined together to determine the amplification ratio range of -10 dB to 30 dB [3]. Gpos voltage is generated by universal DAC to achieve gain programmable control.

The AD input protection clamp circuit consists of 3.3V voltage regulator diode D3 and resistance R34, which limits the output voltage of AD603 to 0-3.3V and protects the input of ADC. The circuit is shown in Fig. 5.

2.3. ADC and DAC
ADC uses ADS7842, which is a 12-bit parallel ADC with the highest sampling rate of 200 ksp/s. It can be powered by 3.3V. It can avoid the problem of level matching between ADC chip and FPGA. Analog power supply and digital power supply are separated to enhance the anti-interference ability of the system. The circuit is shown in Fig. 6.

2.4. FPGA core and related circuits
The core of system control is EP2C5T144 with 4608 LE. The resources are enough to meet the design requirements.

The configuration chip of the FPGA is EPCSISI8, which realizes the power-on loader to the FPGA and the power-off maintenance of the FPGA program.

3.3V and 5V bus buffers are SN74LVC4245A, which can realize output buffering and TTL level matching.

![Figure 4. Current Sensor and Impedance Matching Circuit](image)
3. Fpga Software Composition Block Diagram

The software block diagram is shown in Fig. 7.

3.1. ADS7842 interface module

ADS7842 interface circuit and ADS7842 chip form the clock and other response signals needed for data transmission, and receive the incoming data, then the relevant data are transmitted to the peak holding module, zero-crossing comparison module, and trigger module and so on.
3.2. **PID control module**

PID algorithm is abbreviated as proportional, integral and differential algorithm. It is suitable for situations where the mathematical model of control object is difficult to establish. In this design, the closed-loop control between gain control and signal peak value is very suitable to use this algorithm for control, and the use of PID algorithm can keep the waveform amplitude stable.

3.3. **Outbound level control module**

The trigger signal generating module counts the pulses generated by the trigger compiling and generating module, and outputs the final output signal.

3.4. **Positive and negative edge generation module of flip-flop**

The positive and negative edge generation module of flip-flop is a double-limit comparator. When the data $AD_{Data}[11.0]$ sampled by AD is larger than that of $D_{up}[11.0]$, the output edge of the module rises; when the data $AD_{Data}[11.0]$ is smaller than that of $D_{down}[11.0]$, the output edge of the module falls.

3.5. **Trigger signal generation module**

The trigger signal generating module counts the pulses generated by the trigger compiling and generating module, and outputs the final output signal.

3.6. **Key control module**

The trigger signal generation module controls the output of $C_{Data}$ from 0 to 99 by processing the key value.

3.7. **Dynamic scanning module**

Dynamic scanning module drives two digital tubes to display the value of $C_{Data}[5.0]$ by dynamic scanning mode.

4. **Measured waveform**

When the trigger is finished, it is connected to the welding monitoring system. When the welding machine works normally, the input waveform of the current sensor and the output waveform of the trigger are measured as shown in Fig. 8.

![Figure 7. FPGA software composition block diagram](image)
5. Practical application effect
Connect the output of the trigger to the trigger pulse input interface of the high-speed camera of the monitoring system. The function of the trigger chooses to output the positive trigger pulse along the declining waveform of the input current, i.e. the t2 time period in Fig. 1. The camera chooses the positive trigger shutter along the external trigger pulse. In the normal operation of the welding machine, the photograph of the welding pool can be taken. As shown in the fig. 9, the image of the welding pool can be clearly observed. In contrast, as shown in Fig. 2, the image taken by the trigger circuit of the camera itself triggers the shutter. The visible arc and spatter are serious, and the shape of the molten pool is not easy to observe.

6. Conclusion
The design and fabrication of flip-flop have solved the problem of triggering time of shutter of high-speed camera in welding monitoring system. It can get clear and identifiable image of molten pool, which lays a foundation for the application and function development of the whole system.

![Figure 8. Measured waveform](image)

![Figure 9. weld pool image(Trigger incentive camera)](image)

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