Multistage switching hardware and software implementations for student experiment purpose

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Abstract. Current communication and internet networks are underpinned by the switching technologies that interconnect one network to the others. Students’ understanding on networks rely on how they convert the theories. However, understanding theories without touching the reality may exert spots in the overall knowledge. This paper reports the progress of the multistage switching design and implementation for student laboratory activities. The hardware and software designs are based on three stages Clos switching architecture with modular 2x2 switches, controlled by an Arduino microcontroller. The designed modules can also be extended for batcher and banyan switch, and working on circuit and packet switching systems. The circuit analysis and simulation show that the blocking probability for each switch combinations can be obtained by generating random or patterned traffics. The mathematic model and simulation analysis shows 16.4% blocking probability differences as the traffic generation is uniform. The circuits design components and interfacing solution have been identified to allow next step implementation.

1. Introduction
Switching system enables terminal equipment such as telephone, facsimile, and computer to be connected to the same equipment in other places [1, 2]. Switching system is the basic technology for both telephone system and internetworking.

One of the most famous switching architecture is three-stage Clos switching system [3]. The sample of the switching architecture is shown in Figure 1. Number of input of the first stage is N,
number of input the second stage is K, then the switching matrix in the first, second and the third stages are NxK, KxK and KxN. The probability of blocking is approximated by Lee [4]:

\[ P_B = \frac{u!}{m!(2u-m)!} (1-p)^{2u-m} p^m \]  

where u=n-1, n is number of input in the first stage module, m is number of switching modules in second stage, p is the probability of an input link busy.

Since then, the switching research and development are improved rapidly [5]. However, the academics approach for laboratory activities are limited to a sample of mini switching system that is hardly representing the way those switches working, or analytic approach containing mathematic and simulation, that are also hardly showing how the switch works.

This paper reports the initial work on designing a multistage switching system that is aimed for student’s laboratory. The switch is designed based on the threestage Clos switching system and made of digital circuits and analog switch IC’s that are controlled by the Arduino. Initial designed presents the circuit analysis using Lee approximation, circuits’ performance evaluation using discrete event simulation, circuits interfacing problem identifications and interfacing solutions.

2. Research Methods

2.1 Hardware Design

In order to realize the multistage switching system, the following devices are required:

- Switch to connect input and output ports. In order to operate in both analogue and digital technologies, the analogue switch integrated circuit that is controlled by digital signal is needed.
- Latch is employed to buffer digital output, programmed by Arduino and drive the switches.
- Decoder is employed to allow Arduino choose which switch is programmed by sending 8 bits control signal.
- Arduino is employed as the switching controller

The designed circuit blog is shown in Figure 2. The Arduino programs the switch modules by sending 8 bits to latch. As there are multiple switch modules, the programmed latch is chosen by using a decoder.

![Figure 2. Circuit Block Diagram](image-url)
2.2 Software Design

Software design for Arduino is shown in Figure 3. Arduino as the processor and the controller receives connection instructions from the controller or test circuit which is separately reported. The Arduino program should perform the following function:
- Configure the selected switch depending NxK size.
- Choose the correlated or the alternative switch route to connect the assessed input and output.
- Response to next connection without losing the existing connection.

2.3 System Simulation

Simulation is conducted by using Java programming language by:
- Identifying switches for any input and output connections.
- Generating traffic based on offered traffic in Erlang.
- Evaluating the successful and the blocking rates.

3. Current Results

The results reported by the time this paper written includes the components that have been selected, potential interfacing problems that have been resolved, and simulations that have been performed.

3.1 Circuit Components

HCF4066B [6] is selected as the switch IC in DIP package. HCF4066B is a quad bilateral switch as shown in Figure 3a.

IC SN74HC574 [7], a D-type flip-flop octal edge-triggered with 3-state output is employed for driving IC HCF4066B. SN74HC574 receives data when clock transition is from low to high. Pin output-enable (OE) is used to activate output. Figure 3b shows the schematic diagrams for IC SN74HC574.

HD74LS138 [8] is chosen as the decoder to allow Arduino selecting switch modules to be programmed by changing latch states. This IC decides which pin is active by using 3 digit binary numbers in select pins. The two active-low and one active-high enable-pins is used to cascade more than one decoder. Finally, the Arduino UNO is selected as the processor and the controller.

3.2 Potential Problems

The main problem when working with digital ICs is the interfacing between ICs with different technologies such as CMOS (complementary metal oxide semiconductor) and TTL (transistor-transistor logic).

As HCF4066B is a CMOS IC and SN74HC574 is a TTL IC, the input and output voltage differences require a specific pin connection. Table 1 shows the voltage differences.

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![Figure 3. HCF4066B, SN74HC574 and HD74LS138](image-url)
Table 1. Interfacing 74574 and 4066

| SN74HC574 Output | HCF4066B Input |
|------------------|----------------|
| High=4.3-5V      | High= Vcc     |
| Low= 0-1.8V      | Low= VDD     |

Table 2. Interfacing 74138 and 74574

| HD74LS138 Output | SN74HC574 Input |
|------------------|-----------------|
| High=2.7-5V      | High= 4.2-5V   |
| Low= 0-0.5V      | Low= 0-1.8V    |

Even dough, SN74HC574 specification with voltage supply from –0.5 V to 7 V, output clamp current reaches 20 mA, continuous output current ±35 mA, and continuous current through VCC achieves ±70 mA. By considering these values and control current for switch HCF4066B less than 10uS, the SN74HC574 can be connected directly to HCF4066B. It is supported the fact that the high-current 3-State Non inverting Outputs of SN74HC574 is able to drive bus line up to 15 LSTTL ICs. So the interfacing solution is depicted in Figure 4a.

(a). Interfacing 74 HC ke TTL [9]

(b). Interfacing LS TTL to HC CMOS

Figure 4. IC Interfacing [9]

The same analysis falls to HD74LS138 and SN74HC574 interfacing with voltage levels as shown in Table 2 and a solution as depicted in Figure 4b. Meanwhile, the interfacing between the Arduino UNO and SN74HC574 as well as the Arduino and IC HD 74LS138 can be connected directly.

3.3 Analytical and Simulation Evaluations

By using Lee approximation and a discrete event simulation to a sample of three stage clos switching system as depicted in Figure 5, which have the plotted switch alternatives for each connection.
Figure 5. 9x9 Switching System

An offered traffic in each link generates the probability of a link busy, \( p \). Every time a traffic comes, system should decide which route is taken by considering free switches status. If one of the switches in the first route is occupied, system checks the next alternatives. The generated traffic should not request connection to the busy output as the blocking assessment is only to switching blocking rate. By doing so, adjusting offered traffic from 0.1 to 1 erlang, the results are plotted in Figure 6. Despite 16.4% deviation, the simulation results pattern is matched to Lee approximation.

Figure 6. Simulation Results

4. Conclusions
This paper has presented the initial result in designing multistage clos switching system for student’s laboratory activities. Potential components and problems have been identified and initial analysis as well as simulation has been carried out. Although the last generated 16.4% deviation, the model and simulation patterns are inline.

Future work is to implement the selected components to electronic board. Changes may apply depending on the circuit performances.
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