A High-Speed True Random Number Generator Based on a Cu$_{x}$Te$_{1-x}$ Diffusive Memristor

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Herein, a true random number generator (TRNG) based on a Cu$_{x}$Te$_{1-x}$ diffusive memristor (DM) using its threshold switching (TS) behavior is reported. The intrinsic stochasticity of the TS behavior contributes to the randomness of the TRNG system. The switching behavior is discussed through field-induced nucleation theory and surface diffusion dynamics. Demonstrating the performance of TRNG as a hardware security application, the DM-based TRNG passes all 15 National Institute of Standards and Technology randomness tests without any post-processing step, even in high-temperature conditions. Moreover, a nonlinear-feedback shift register is implemented for a high-speed TRNG, producing the highest rate among the reported volatile-memristor-based TRNGs.

1. Introduction

A memristor is a resistive switching device that exhibits tunable resistance states by applying an external bias. It has attracted considerable interest due to its low power consumption, scalability, switching speed, and a simple metal–insulator–metal (MIM) structure. Engineered in the desired way, a memristor can be either volatile or nonvolatile. While the conventional nonvolatile memristor is a resistance switching (RS) device that requires both SET (switching from off to on state) and RESET (switching from on to off state) processes to switch the resistance state, the volatile memristor exhibits threshold switching (TS) behavior, reaching an ON (TS-on) state with a certain threshold voltage, and switches back to the OFF (TS-off) state by simply removing the voltage.

Among the various types of memristors, a conducting bridge random access memory (CBRAM) device, also known as an electrochemical metallization cell (ECM), is based on a metal ion-based filamentary conducting mechanism. In this case, the metal ions drift out of an active electrode, such as Cu or Ag, or anode to form a conductive filament (CF) between the active electrode and a passive electrode, such as TiN or Pt. Various materials have been investigated for the electrodes and insulators in the MIM structure. For the insulating layer, chalcogenide electrolytes, such as GeS and GeSe, were initially studied. However, due to the higher diffusivity of metal cations, various transition metal oxides, such as HfO$_2$, TiO$_2$, and Ta$_2$O$_5$, were later introduced to enhance the CBRAM switching properties. Among active metals, Ag exhibits higher mobility than Cu in the above-mentioned insulating layers. However, due to its incompatibility with the conventional complementary metal–oxide–semiconductor (CMOS) process, the focus has recently shifted to Cu.

Nonetheless, adopting an elemental Cu electrode has caused several problems due to the uncontrolled injection of Cu ions into the oxide matrix, which affects the stability of the CF, resulting in a high reset current during the RS operation. Several methods have been suggested to avoid this problem. Adopting Cu alloy electrodes has shown promising results due to the well-controlled amount of Cu ions drifting out of the electrode. Notably, a Cu$_{x}$Te$_{1-x}$ active electrode shows diverse switching behaviors depending on the Cu concentration in the Cu$_{x}$Te$_{1-x}$ compound; a low Cu concentration in the device exhibits TS behavior, whereas a high Cu concentration leads to an RS behavior.

With the tremendous growth of the Internet of Things (IoT), data security has become the subject of intensive research. This work exploits the TS performance of the Cu$_{0.1}$Te$_{0.9}$ electrode to construct a true random number generator (TRNG), which is a crucial component of a hardware security system that exploits the physical stochasticity of entropy sources to generate random bit streams. While the randomness or stochasticity of TS in many memristors is undesirable in typical memory applications, it can be feasibly used for randomness applications, such as TRNGs.

Previously reported memristor-based TRNGs used stochastic characteristics of nonvolatile memristors, including current fluctuation, voltage variation, and random telegraph noise. Although these TRNG schemes seemed applicable, none of them passed the National Institute of Standards and Technology (NIST) randomness tests, and all relied on a post-processing step.
due to their lack of true randomness. Therefore, the research focus has shifted toward volatile-memristor-based TRNGs. The first reported volatile-memristor-based TRNG was used the stochastic delay time of a Ag:SiO$_2$-based diffusive memristor (DM). It was the first memristor-based TRNG to pass the NIST randomness tests without any post-processing step. Volatile-memristor-based TRNGs can be considered superior to nonvolatile-memristor-based TRNGs, as they do not require the RESET step. However, all the aforementioned TRNGs have low bit generation rates and are, thus, limited to low-speed encryption applications. To enable a wide range of encryption applications, the bit generation rate must be improved. In our previous TRNG research, a volatile-memristor-based TRNG, which was based on the carrier trapping/detrapping mechanism in a Pt/HfO$_2$/TiN memristor, was combined with a nonlinear-feedback shift register (NFSR) to improve the bit generation rate while maintaining randomness. The bit generation rate increased 2.7 times compared with the previous work using the Ag:SiO$_2$-based DM, which was already a substantial improvement. However, it was also found that a device with an even faster switching time is required to further increase the bit generation rate and broaden the range of TRNG applications.

In this work, a Cu$_{0.1}$Te$_{0.9}$/HfO$_2$/Pt (CTHP) DM was used to create a DM-based TRNG (DMTRNG). The DMTRNG was combined with an NFSR to achieve a higher bit generation rate without significantly increasing power consumption. The CTHP memristor has a stochastic delay and relaxation times, which were used as entropy sources. The DMTRNG produced a bit generation rate of 32 kb s$^{-1}$, which is the highest among the reported volatile-memristor-based TRNGs. For a deeper understanding of CTHP DM, its switching behavior was further analyzed using field-induced nucleation theory and surface diffusion dynamics.

2. Results and Discussion

2.1. TS Behavior in a CTHP Memristor

Figure 1 shows the TS behavior of the CTHP memristor. As shown in the scanning electron microscopy (SEM) image of Figure S1a, Supporting Information, an $8 \times 8 \mu m^2$ electrode area of the CTHP memristor was fabricated with a cross-point structure. The memristor’s structure was confirmed by Auger electron spectroscopy (AES) and transmission electron microscopy (TEM) images (Figure S1b,c, Supporting Information). Te nanoclusters were found from the lattice fringe analysis using the fast Fourier

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Figure 1. TS behavior in a CTHP memristor. a) $I-V$ curves of the CTHP memristor. The inset shows a schematic of the CTHP memristor. b) Pulse switching behavior of the CTHP memristor. The inset shows the pulse measurement system in a circuit configuration. c) Metallic filament formation at a high (left) and low $I_{cc}$ (right). Yellow spheres represent the Cu atoms.
transform (FFT) technique, as shown in the inset of Figure S2c, Supporting Information. The glancing-angle X-ray diffraction (GAXRD) pattern of the device showed that amorphous HfO$_2$ was grown (Figure S1d, Supporting Information). No peak was found other than Te, Pt, and Si. The switching behavior of the Cu$_x$Te$_{1-x}$-based memristor was examined in the range 0.1 < x < 0.4. Volatile performance was observed only at x = 0.1, whereas higher x values showed nonvolatile behavior. Accordingly, a Cu$_{0.1}$Te$_{0.9}$ layer was adopted in this experiment. The low composition of Cu in the Cu$_x$Te$_{1-x}$ layer tends to exhibit volatile characteristics. When a positive bias is applied to the Cu$_{0.1}$Te$_{0.9}$ electrode, only a small concentration of Cu ions migrates into the HfO$_2$ layer, which then forms a miniscule Cu CF. In this case, a weak Cu CF had higher interface energy with the HfO$_2$ matrix, and the Cu atoms in the filament diffused back to the active electrode after voltage removal, as shown in Figure S2a, Supporting Information. At high x values, on the other hand, large Cu electromigration led to the formation of a stronger Cu CF formation and prevented its dissolution, exhibiting nonvolatile characteristics (Figure S2b, Supporting Information). Moreover, as the electron affinity of Cu (118.4 kJ mol$^{-1}$) is lower than that of Te (190.2 kJ mol$^{-1}$), more oxidation is expected to occur in Cu. Therefore, Cu preferentially contributes to the filament formation over Te.

Figure 1a shows the current–voltage (I–V) curves of the memristor with a compliance current ($I_c$) of 10 nA. An electroforming process was required at 4.5 V, and 30 consecutive sweeps showed that the threshold voltage ranged from 1.5 to 2.5 V. As shown in the pulse measurement (Figure 1b), a threshold voltage of 6 V was required for the TS-on process, and a hold voltage of 0.6 V was applied to observe the TS-off process. Here, a delay time before the device switched to the TS-on state and a relaxation time until the device relaxed back to zero were observed. The application of multiple pulses to the device showed that both the delay and relaxation times were stochastic. Jiang et al. used dynamic nanoparticle simulations to identify the stochastic nature of the switching time.$^{[24]}$ The stochasticity of the switching behavior is attributed to the stochastic process of nanoclusters detached from the active electrode before the formation of the CF. The simulation predicts nanoparticle dynamics based on the electrical, mechanical, and thermal degrees of freedom. The time needed for the particle to overcome the interfacial barrier between the active electrode and the insulator during the detachment process is estimated to be random in nature by the probabilistic Fokker–Plank equation. Similarly, the stochasticity of the delay and relaxation times in this device originated from a stochastic process whereby Cu atoms were detached from the CuTe electrode and Cu CF, respectively. The switching behavior of the device is discussed in detail later. Furthermore, $I_{cc}$ controls the number of Cu atoms, that compose the CF.$^{[28,29]}$ Depending on the level of $I_{cc}$, the device can exhibit either nonvolatile or volatile behavior, as shown in Figure 1c. At high $I_{cc}$, a large number of metal atoms forms a thick CF, which is sufficiently strong to make the device nonvolatile. At a low $I_{cc}$, on the other hand, a weaker CF is formed from fewer metal bands. In this case, when the voltage is removed, the Cu atoms composing the CF move more easily, leading to its dissolution.

### 2.2. Delay Time Supported by Field-Induced Nucleation Theory

Figure 2a shows the influence of the input pulse on the delay time. It is based on 50 sampling points for each input pulse. With a higher pulse, the delay time exponentially decreased. This can be explained by field-induced nucleation theory.$^{[30–33]}$ According to this theory, a CF is formed by the growth of a metallic nucleus. Under an external field, a stable nucleus can only be formed when the nucleation energy barrier $W(E)$ is overcome, and filament formation occurs when the nucleus radius exceeds the critical radius $R_0$, as shown in Figure 2b. When the field is removed, the nucleation energy barrier recovers its initial value $W_0$. Depending on the nucleus radius, the filament either ruptures ($<R_0$) or maintains its structure ($>R_0$). In other words, the device can have both volatile TS and nonvolatile RS behaviors, depending on the nucleus size. The nucleation energy barrier under the external field has the form

$$W(E) = W_0 \alpha \exp\left(\frac{W_0}{kT}\right)$$

where $h$ is the dielectric thickness, $E_0$ is the voltage acceleration factor independent of the external field with the typical value of 1 MV cm$^{-1}$, $\alpha$ is the geometric factor, assumed to be 0.5, which corresponds to the highest nucleation energy barrier, and $V$ is the applied voltage. Here, the delay time, $\tau_d$, can be expressed as follows$^{[31,32]}

$$\tau_d = \tau_0 \exp\left(\frac{W(E)}{kT}\right) = \tau_0 \exp\left(\frac{W_0 \alpha \exp\left(\frac{W_0}{kT}\right)}{kTV}\right)$$

The exponential decrease in delay time with the increase in the input pulse is in line with field-induced nucleation theory.

The nucleation energy barrier at zero field ($W_0$) is calculated from the slope of the plot shown in Figure 2c. The $W_0$ value was 0.51 eV. Previous studies reported that the $W_0$ value of a HfO$_2$-based CBRAM device was 0.47 eV, which is reasonably consistent with the value in this work.$^{[34,35]}

### 2.3. Relaxation Time Analysis based on Surface Diffusion Dynamics

The relaxation time was also studied under different input voltages; 50 samples are measured for each input pulse in the same way as Figure 2a. Unlike the delay time, the relaxation time increased exponentially with a higher pulse, as shown in Figure 3a. In volatile filamentary switching, once the external voltage is removed, metal ions migrate from the CF and form spherical nanoclusters to minimize the surface energy. Considering the small size of the device, the primary mechanism of migration must be surface diffusion.$^{[36,37]}$ To explain the CF dissolution time, the kinetic process mainly involving surface diffusion dynamics based on the thermodynamic Gibbs–Thomson effect should be considered. The surface atomic flux of the Cu filament, $J$, is derived according to the Nernst–Einstein relation and Fick’s law as follows

$$J = -\frac{D\Delta \Omega n}{kT} \nabla \kappa$$
where $D$ is the diffusion coefficient, $\gamma_A$ is the specific surface energy, $\Omega$ is the atomic volume, $n$ is the number of atoms per unit volume, $k$ is Boltzmann’s constant, $T$ is the temperature, and $\kappa$ is the surface curvature of the metal filament, given by $\kappa = \frac{1}{r_1} + \frac{1}{r_2}$, where $r_1$ and $r_2$ are the principal radii of the curvature of the CF, shown graphically in Figure 3b (see Note 1, Supporting Information, for further information about the derivation of Equation (3)). By this relation, the stability of the metal filament is strongly influenced by the surface curvature when there is no external field. Assuming that CF profile is the same, the smaller the filament diameter, which is equivalent to the larger surface curvature, the larger the atomic flux during the dissolution process, and thus, the shorter the relaxation time. Moreover, the voltage pulse amplitude was converted into the filament diameter according to the assumption shown in Note 2, Supporting Information. The relationship between the size of the CF and the dissolution time can be explained by Herring’s scaling law, which describes the time scaling with structural dimension changes for various atomic migration mechanisms, under the assumption that atomic migration occurs in the direction of minimizing the surface energy. According to Herring’s scaling law for the surface diffusion-based dissolution process, it is known that $r_i$ is proportional to $d_0^4$, where $d_0$ is the initial filament diameter.\(^{[40]}\) This is consistent with the logarithmic slope calculation results shown in Figure 3c. It can be concluded that the dissolution of the Cu CF is mainly driven by the force to minimize its surface energy, and that the underlying mechanism is the surface diffusion of Cu ions.

Figure 3d shows the relationship between the filament diameter and the relaxation time of previously reported CBRAM devices with Cu-based active electrodes. The CTHP device in this work showed a significantly shorter relaxation time compared with previously reported Cu-electrode devices. Due to the low concentration of Cu in the active electrode, the injection of Cu atoms into the oxide matrix decreased, which was intensified by the existence of stable Cu–Te bonds in the active electrode.\(^{[17,18,41]}\) Consequently, a thinner Cu CF was formed compared with those of other Cu-based devices. A thinner Cu CF with a larger surface curvature resulted in a faster dissolution rate, shortening the relaxation time.

### 2.4. Implementation of TRNG

Figure 4a shows the circuit design of the DMTRNG, including a memristor, an NFSR consisting of an XNOR gate (SN74LS266, Texas Instruments), an XOR gate (HD74HC86, Renesas), and shift registers that are composed of four D flip-flops (MC14015B, ON Semiconductor). The working principle of
the DMTRNG is schematically shown in Figure 4b and has also been reported elsewhere.\(^\text{(27)}\) It is a proof of concept, which helps to understand the working principle of this work. As it is the proof of concept, no coordinate axes are given. The pulse sequences at each step labeled in Figure 4a are displayed. When the input pulse (\(V_1\)) is applied to the memristor (panel 1), the output voltage (\(V_2\)) can be shown (panel 2). \(V_2\) appears after the delay time and continues at a high level until the end of the relaxation time. It is then sent to the XNOR gate along with the feedback peak (\(V_3\) in panel 3) from the XOR gate. The output peak (\(V_4\) in panel 4) from the XNOR gate shows the inverter-like function, which is explained in detail in the following. Finally, \(V_4\) goes into the shift register. The shift register generates the output bit by reflecting the \(V_4\) peak at every edge of the clock signal (panel 5).

The actual experimental demonstration of the DMTRNG is shown in Figure 4c. Random output bits were observed from two consecutive cycles of the lowest-order bit monitored with an oscilloscope. The input pulse was 7 V and had a width of 350 \(\mu\)s. To allow the memristor to fully relax, a 150 \(\mu\)s rest time was provided before the next pulse. The bit generation rate was 32 \(\text{kb s}^{-1}\), which is the fastest speed among the reported volatile-memristor-based TRNGs.\(^\text{(24,25,27)}\) In this work, the possibility of speed enhancement was experimentally proved through two ways: circuit modification and device engineering. The speed was improved with the combination of NFSR. Previous volatile-memristor-based TRNGs mainly used T flip-flops to produce the output bits. In this work, D flip-flops are used, as they can generate more bits than the T flip-flop within the same period. The speed can be improved by simply increasing the number of D flip-flops, and it can potentially reach 100 \(\text{Mb s}^{-1}\) according to previous reports.\(^\text{(20)}\) However, adding too many D flip-flops may cause circuit size and power consumption issues. Besides circuit modification, a higher switching speed of the memristor could improve the bit generation rate. The switching speed can determine the period of one TRNG cycle, which is the period of the input pulse applied to the memristor. Therefore, a higher switching speed can shorten the period, enhancing the bit generation rate. Further optimizations of the device dimension and insulator materials can be the possible solutions for the switching speed increase. Thinner insulator thickness can effectively reduce the operating voltage. Insulators allowing higher Cu ion diffusivity in the matrix or insulators with a smaller activation energy of metal-ion diffusion can improve the switching speed of the device.

The NFSR is a simple approach to increasing the bit generation rate without consuming too much power. A seed is the
initial bits of the NFSR, and the XOR gate is called a tap or a feedback connection, to which the bits enter to form new ones. Previous studies have shown that a linear-feedback shift register (LFSR) could be used to improve the bit generation rate with minimal power consumption.\cite{24,42} However, its inherent linearity and locked-up state issues hamper the functionality of TRNG.\cite{27} As the linear feedback connection from the XOR gate is predictable, it can easily be attacked. Also, the D flip-flops can be locked up when the initial bits are all “0,” continuously generating the output bit “0” from the XOR gate. These problems can be solved with this DMTRNG circuit. The truly random seed from the memristor’s stochastic switching times and the additional XNOR gate make the feedback function nonlinear.

Figure S3, Supporting Information, explains the nonlinearity of NFSR by comparing three types of shift registers: a pure shift register, an LFSR, and an NFSR. The pure cycling of Figure S3a, Supporting Information, can be improved by the feedback connection $f$, as shown in Figure S3b, Supporting Information. The LFSR is more complex than the pure shift register, but its linear feedback connection remains predictable. Here, the logic function from the memristor and the XNOR gate was added to form a new feedback function $f_2$. When the memristor is in the TS-off state (logic function “0”), $f_2$ is the opposite of $f_1$. This inverter-like function can be seen in panels 3 and 4 of Figure 2b. The flowchart of Figure S3c, Supporting Information, shows how the feedback function is determined by the memristor output. In addition, the XNOR gate can prevent the locked-up state, as it is the logical complement of the XOR gate.

Figure 4. Implementation of the TRNG. a) A circuit diagram (left) of the TRNG with a memristor, an XNOR gate, an XOR gate, and four D flip-flops, and a photograph (right) of the circuit built on a breadboard. b) Working principle of the TRNG at each step as labeled in (a). No coordinate axes are given, because this is a proof of concept. c) Experimental demonstration of the TRNG with two consecutive cycles.

Table 1. Comparison between the proposed DMTRNG and three previously reported volatile-memristor-based TRNGs.

| Source of randomness | Ag:SiO$_2$ DMTRNG | Pt/HfO$_2$/TiN memristor TRNG | Pt/HfO$_2$/TiN memristor TRNG combined with NFSR | CuTe-based DMTRNG |
|---------------------|-------------------|-------------------------------|-----------------------------------------------|------------------|
| TS mechanism        | Ionic             | Electronic                    | Electronic                                    | Ionic            |
| Bit generation rate | 6 kb s$^{-1}$     | 6 kb s$^{-1}$                 | 16 kb s$^{-1}$                                | 32 kb s$^{-1}$   |
| NIST tests          | Passed            | Passed                        | Passed                                        | Passed           |
| Post-processing     | No                | No                            | No                                            | No               |

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| TS mechanism        | Ionic             | Electronic                    | Electronic                                    | Ionic            |
| Bit generation rate | 6 kb s$^{-1}$     | 6 kb s$^{-1}$                 | 16 kb s$^{-1}$                                | 32 kb s$^{-1}$   |
| NIST tests          | Passed            | Passed                        | Passed                                        | Passed           |
| Post-processing     | No                | No                            | No                                            | No               |

Figure 4.

Table 1.

| Source of randomness | Ag:SiO$_2$ DMTRNG | Pt/HfO$_2$/TiN memristor TRNG | Pt/HfO$_2$/TiN memristor TRNG combined with NFSR | CuTe-based DMTRNG |
|---------------------|-------------------|-------------------------------|-----------------------------------------------|------------------|
| TS mechanism        | Ionic             | Electronic                    | Electronic                                    | Ionic            |
| Bit generation rate | 6 kb s$^{-1}$     | 6 kb s$^{-1}$                 | 16 kb s$^{-1}$                                | 32 kb s$^{-1}$   |
| NIST tests          | Passed            | Passed                        | Passed                                        | Passed           |
| Post-processing     | No                | No                            | No                                            | No               |
The performance of the DMTRNG was assessed through the NIST Statistical Test Suite. The suite consists of 15 tests, evaluating the randomness and unpredictability of a TRNG. Each test is considered passed if the $P$-value is higher than 0.0001, and the minimum pass rate is achieved. The $P$-value expresses the probability that the observed data confirm the null hypothesis, considering that the null hypothesis is true. The significance level of 0.0001 is the value at which the measured data reject the null hypothesis. The greater the $P$-value, the stronger the evidence that the null hypothesis is supported. The null hypothesis in this study was that the bit streams collected from the DMTRNG are random. Thus, the $P$-value has to be greater than the significance level to accept the null hypothesis; 55 sequences of 10$^6$ bits were collected, and they passed all 15 NIST tests without any post-processing step. This showed that the proposed DMTRNG is immune to harsh environments, showing outstanding performance under high-temperature conditions.

### Table 2. NIST randomness test results.

| Test                                      | P-value     | Minimum pass rate | Pass/fail |
|-------------------------------------------|-------------|-------------------|-----------|
| 1. Frequency Test                         | 0.689521    | 52/55             | Pass      |
| 2. Frequency test within a block          | 0.690284    | 52/55             | Pass      |
| 3. Runs test                              | 0.153473    | 52/55             | Pass      |
| 4. Test for the longest run of ones in a block | 0.056449    | 52/55             | Pass      |
| 5. Binary matrix rank test                | 0.037055    | 52/55             | Pass      |
| 6. Discrete Fourier transform test        | 0.103806    | 52/55             | Pass      |
| 7. Non-overlapping template matching test | 0.057974    | 52/55             | Pass      |
| 8. Overlapping template matching test     | 0.292062    | 52/55             | Pass      |
| 9. Maurer’s “Universal Statistical” test  | 0.006699    | 52/55             | Pass      |
| 10. Linear complexity test                | 0.197135    | 52/55             | Pass      |
| 11. Serial test                           | 0.547051    | 52/55             | Pass      |
| 12. Approximate entropy test              | 0.527399    | 52/55             | Pass      |
| 13. Cumulative sums test                  | 0.397523    | 52/55             | Pass      |
| 14. Random excursions test                | 0.785526    | 52/55             | Pass      |
| 15. Random excursions variant test        | 0.869791    | 52/55             | Pass      |

### 3. Conclusion

In this work, we created a TRNG using the stochastic delay and relaxation times of a TS Cu$_{0.1}$Te$_{0.9}$ DM as random sources. Field-induced nucleation theory and surface diffusion dynamics were used to analyze the delay and relaxation times of the miniscule Cu CF of the device. With the combination of the Cu$_{0.1}$Te$_{0.9}$ DM with an NFSR, the DMTRNG produced the bit streams with the highest rate among the reported volatile-memristor-based TRNGs. The random bit streams collected from the DMTRNG passed all the NIST randomness tests without any post-processing step. The robustness of the memristor-based TRNG under high-temperature conditions (80°C) proves its feasibility. As the importance of hardware-based security is increasing in the IoT era, the adoption of TS DMs in TRNGs plays a crucial role in data security.

### 4. Experimental Section

The CTHP memristor was fabricated in a cross-point structure on a SiO$_2$/Si substrate. An 8-nm-thick Ti adhesion layer and a 50-nm-thick Pt bottom electrode were deposited in sequence using an electron beam evaporator (SRN-200, SORONA) and patterned by a lift-off process. A 10-nm-thick HfO$_2$ insulator layer was then deposited via thermal atomic layer deposition (ALD), with Hf[N(CH$_3$)$_2$]$_4$ as a Hf precursor and O$_2$ as an oxygen source, using an 8” scale traveling-wave-type ALD reactor (Plus 200, CN-1 Co.) at a 280°C substrate temperature. Then, a 40-nm-thick Cu$_{0.1}$Te$_{0.9}$ top electrode was direct current (DC)-sputtered by co-sputtering Cu and Te targets (07SN014, SNTEK) with a power of 10 and 120 W, respectively, and a 40-nm-thick Pt passivation layer was deposited using an electron beam evaporator (SRN-200, SORONA), followed by a lift-off process. The purpose of adding the Pt layer on top of the Cu$_{0.1}$Te$_{0.9}$ top electrode was to reduce the sheet resistance of the top electrode. The l–V characteristics were measured using a semiconductor parameter analyzer (HP4145B, Hewlett-Packard) in DC voltage sweep mode. For the pulse measurements, an Agilent 81110A pulse generator was used. The top electrode was biased, and the bottom electrode was grounded during the measurements. The cross-point structure was observed using SEM (S-4800, Hitachi). A cross-sectional image of the device was acquired using TEM (JEM-F200, JEOL), and the TEM specimen was prepared via a focused ion beam (Helios C4, Thermo Fisher Scientific). The depth profile was examined using AES (PHI-700, ULVAC-PHI). The crystallinity of the device was measured by GAXRD (X’Pert PRO MPD, PANalytical). The local crystallization was analyzed by the FFT method. The parasitic capacitance of the measurement setup was $\approx$100 pF. The circuit delay time was $\approx$0.1 ms when the series resistance of the oscilloscope was set to 1 MΩ.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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### Conflict of Interest

The authors declare no conflict of interest.
Data Availability Statement

Research data are not shared.

Keywords

conductive filaments, diffuse memristors, nonlinear-feedback shift registers, threshold switching, true random number generators

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