Development, testing and installation of a Superconducting Fault Current Limiter for medium voltage distribution networks

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Abstract

Since 2009 Ricerca sul Sistema Energetico (RSE S.p.A.) has been involved in the design of resistive-type Superconducting Fault Current Limiter (SFCL) for MV applications to be installed in the A2A Reti Elettriche S.p.A distribution grid in the Milano area. The project started with simulations, design and testing activities for a single-phase device; in this paper we report on the successive step, which is concerned with developing, testing and installation at the hosting utility of the final three-phase SFCL prototype. The result of this research activity is a resistive-type 9 kV/3.4 MVA SFCL device, based on first generation (1G) BSCCO tapes, developed by RSE in the framework of a R&D national project. Owing to the positive test results of partial discharge, dielectric and short-circuit results the three-phase SFCL device is being to be installed in the A2A distribution grid in the Milano area and it is going to be soon energized starting a one-year long field-testing activity.

1. Introduction

The Superconducting Fault Current Limiter (SFCL) is an innovative device that, when properly designed and placed in appropriate positions in an electrical grid, is able to limit the short-circuit current $I_{sc}$ to values compatible with safety and reliability of the installed network components [1]. Among all different types of SFCL nowadays under study, resistive-type SFCL are expected to be one of the first technically and economically viable applications of High Temperature Superconductors (HTS) [2-3]. By
exploiting their intrinsic properties, HTS have characteristics that make them particularly suitable for this type of device: their electrical resistivity, in fact, undergoes a sudden ramp-up when they are carrying currents whose instant value exceeds a threshold called "critical current" ($I_c$), conventionally defined by using the electric field criterion of 1μV/cm. Silver-alloy sheathed BSCCO-2223 tapes, first generation (1G) wires, are historically the most applicable solution for usage at the temperature of 77 K [4]; nevertheless, many applications of YBCO coated conductors second generation (2G) wires, are nowadays in course of study [5-6]. From the utilities point of view, the SFCL is highly attractive, as it provides not only a solution to deal with the growing level and incidence of fault currents, but also facilitates innovative planning of electricity grids[7].

A2A Reti Elettriche S.p.A., one of the largest Italian utilities, has already experienced high fault current level at different positions within its MV network and identified a few very suitable locations in its 23 kV and 9 kV grids where a SFCL device could be efficiently installed.

In this work we report on the development, testing and installation of a resistive-type SFCL device for MV applications, performed in the framework of an Italian RTD project aimed at installing a resistive-type SFCL device in the A2A distribution grid in the Milano area. As a first step, a single-phase SFCL device for MV applications was developed and successfully short-circuit tested [1]. In this paper, the development, testing and realization activities devoted to installing the final three-phase resistive-type SFCL device for feeder [2] MV applications at the hosting utility are described.

2. SFCL Design Principles

According to the considered grid location (Table 1), a SFCL device enabling a limitation factor LF = 1.7-2, being this value the ratio between the prospective $I_{SC}$ in the absence of SFCL and the limited current $I_{Lim}$ in the presence of the SFCL device, is highly desirable. In the past, RSE developed MVA-class single and three-phase SFCL prototypes with solenoid winding design, constituted by HTS layers anti-inductively wound on fiberglass cylinders [8, 9]. This configuration is able to dramatically lower (almost annihilate) the magnetic self-field [10].

The SFCL device is made up by means of a HTS tape total length equal to 1880 m. The HTS material used is a multifilamentary stainless steel reinforced silver-alloy sheathed BSCCO-2223 tape insulated by a helicoidally wound Kapton layer with a 50% overlapping and thickness of 12.5 μm. The 1G HTS tape overall cross-sectional dimensions are 4.65 mm x 0.37 mm (including insulation). The self-field critical current at 77 K is about 180 A. Each phase is constituted by three series-connected HTS windings coaxially arranged, moreover each phase is shunted by an air-reactor of 0.4 Ω with power factor $cosφ$ equal to about 0.1. Each winding is realized by two HTS layers anti-inductively wound on fiberglass cylinders and between the two layers a supplementary insulation Kapton layer (125 μm thick) is added.

| Table 1. Network requirements |
|-----------------------------|------------------|
| **Parameter**               | **A2A requirements** |
| Rated voltage               | $V_{nom} = 9$ kV |
| Rated current               | $I_{nom} = 220$ A |
| Prospective short-circuit current | $I_{SC} = 12.3$ kA_{rms} |
| Maximum prospective short-circuit current | $I_{SCP} = 30$ kA_{p} |
| Prospective short-circuit power factor | $cosφ_{SC} = 0.1$ |
| Ungrounded short-circuit duration | $t_{fault} = 400$ ms |
| Limitation factor = $I_{SC} / I_{Lim}$ | LF = 1.7 - 2 |
The three phases are inserted in a liquid nitrogen bath within a cryostat 1800 mm high and characterized by an internal diameter of 600 mm. A closed-circuit Stirling LN liquefier, with cooling power of 1000 W at 77 K (700 W at 65 K) is used for the SFCL refrigeration.

3. SFCL main characterizations

3.1. Critical current ($I_c$) measurements

$I_c$ measurements have been performed at 65 K and 77 K for each winding of the three-phase device. Since each phase is made up of three coaxially arranged windings, nine HTS windings have been tested. To reduce the possible stress applied to the HTS windings, $I_c$ measurements were performed to electrical fields up to about 0.3 μV/cm and the critical current at 1 μV/cm has been then estimated by means of proper exponential fitting functions. The $I_c$ measurement carried out on phase R1, R2, R3 and the resulting curve for the whole phase R are reported in Fig. 1.

3.2. AC losses measurements

The HTS windings have undergone the experimental procedure for the evaluation of AC losses, which consists in injecting 50 Hz modulated-amplitude sinusoidal-AC currents in the HTS windings immersed in a liquid nitrogen bath at 77 K. During the measurement, voltage drop across winding terminals and injected current have been acquired with a sampling frequency of 100 kHz for a time-interval of ten periods (200 ms). Experimental data have been acquired, processed and then compared with those calculated by the Norris equation [11].

Fig. 2 shows the AC losses for phase R as function of the injected current amplitude. In particular, the three coaxial windings R1, R2, R3 are considered separately and the experimental measurements are compared to the analytical results calculated by the Norris equation; moreover, the total AC loss for the whole phase R elaborated starting from the experimental measurements of each coil is also reported; clearly the Norris equation is not able to properly approximate AC losses for the phase under test.

4. SFCL qualification and acceptance tests

SFCL technology has to overcome a relevant obstacle in order to become marketable: nowadays no standards are available because the application of SFCL in power systems is not common yet. Qualification tests concerned with insulation may be considered as the most conventional activity. This allows to consider the existing standards and to adjust them in compliance with the unique features of the device. One of the aims is to look for possible drawbacks in manufacture and this goal may be reached by means of a proper Partial Discharge test (PD); moreover, insulation is to be tested in order to validate the
dielectric withstand capability of the device and this goal may be reached by means of the short-duration power-frequency withstand voltage test and of the Basic Impulse insulation Level test (BIL) [12-14].

SFCL acceptance tests are the most innovative activity because they are aimed at proving the device capability of limiting short-circuit currents in agreement to the networks requirements provided by the hosting utility. On one hand, alike the qualification tests the lack of a proper standardization forces to adjust the existing technical norms [15] to the SFCL device; on the contrary, tailored current testing procedures are to be set in order to validate its limiting capability. In the following, the results of both dielectric and short-circuit testing activities are presented: the first has recently been performed, the latter was performed during the first quarter of 2011. Both tests have been successfully completed.

4.1. Dielectric tests

It is mandatory to test the SFCL device in the same conditions as for its nominal operation in field. For example, the cooling system has to be working during the test and cryostat must be filled in with liquid Nitrogen (LN$_2$). The test full voltages ($V_0$) for the short-duration power-frequency withstand voltage test and for the BIL were equal to 28 kV$_{rms}$ and 60 kV$_p$ respectively [13].

4.1.1. Short-duration power-frequency withstand voltage test

The test procedures followed at RSE laboratories adhere to international standard recommendations, that for what concerns the present application may be briefly summarized as follows [14]:
- The test is to be performed for each SFCL phase individually, i.e. three-times in total. When one single phase is supplied, all the other terminals (the other two phases), cryostats and external vessel must be earthed. The phase supplied is characterized by one terminal connected to the voltage source, while the other terminal is kept floating (or short-circuited with the terminal supplied)
- The test commences at a voltage not greater than one-third (i.e., $<10$ kV$_{rms}$) of the specified full test value and then voltage is increased up to the final test value (i.e., 28 kV$_{rms}$). The voltage is then reduced to less than one-third of the test value (i.e., $<10$ kV$_{rms}$) before switching off. The full-voltage is to be maintained for 1 minute and the test is considered passed if no disruptive discharges occur.

4.1.2. Basic impulse insulation level test (BIL)

Alike the previous test, the testing procedures implemented at RSE laboratories has been compliant with international standards. For what concerns the test sequence, in compliance with [13,14], it did not commence at full voltage. Initially, an impulse of a voltage equal to 0.5$V_0$ (i.e., 30 kV) was applied; afterwards the voltage was gradually increased until the full voltage and then it was decreased; following sequence was applied: (0.6 – 0.8 – 1 – 0.8 – 0.6)$V_0$. The waveform applied is the standard 1.2$\mu$s/50$\mu$s full lightning impulse and test procedure foresees five positive and negative impulses of 60 kV$_p$.

4.1.3. Partial discharge (PD) test

The calibration process for this test was performed by injecting a 5 pC charge through the phase to be tested [12]; the background noise characterizing the test facility was measured to be as low as 1 pC during past experiences. Calibration was repeated whenever a phase was tested. In compliance with the international standards [12], the full voltage was not directly applied; intermediate voltage levels were applied and maintained for a time-period of 30 s and then the PD activity was finally measured.

Table 2 reports the PD measurement results. It is to be noted that phase R exhibits significantly higher PD levels at voltages close to the nominal value with respect to the other two SFCL phases. However, the result was accepted because the test was performed in a very conservative way since the windings were not immersed in liquid nitrogen. Nevertheless, PD measurements will be repeated after the final assembly and further improvements. Fig. 3 shows the experimental output related to PD tests at 9.1 kV on phase T.
Table 2. PD testing results

| Applied Voltage (kV) | PD level phase R (pC) | PD level phase S (pC) | PD level phase T (pC) |
|---------------------|----------------------|----------------------|----------------------|
| 5.2                 | 0.3                  | 0.3                  | 0.3                  |
| 6.2                 | 3.5                  | 0.3                  | 0.3                  |
| 7.0                 | 5.2                  | 0.3                  | 0.3                  |
| 8.3                 | 29.2                 | 0.4                  | 3.2                  |
| 9.0                 | 45.1                 | 0.5                  | 3.3                  |

4.2. Short-circuit current tests

The SFCL system as a whole has been moved to the CESI high-power laboratory in order to test its compliance against the network requirements during both nominal and short-circuit condition. Two voltage levels have been applied: 5.3 kV and 10.2 kV. The tests circuit parameters have been set in order to meet the requirements of nominal currents (220 A_{rms}), nominal power factor (0.99), prospective current (12.3 kA_{rms}) and prospective short-circuit power factor (\( \cos \varphi \leq 0.1 \)).

In Fig. 4 the comparison between short-circuit current without SFCL (prospective short-circuit current) and short-circuit current with SFCL (limited short-circuit current) is shown. It is worthy to note that, owing to the SFCL limiting action, the short-circuit current peak value of 33.28 kA was reduced down to 18.22 kA. A very long fault transient, started at \( t = 20 \) ms lasting for 300 ms has been applied; test duration has been fixed to 300 ms instead of 400 ms to avoid excessive stress and possible ageing.

When the SFCL becomes resistive, the limited current starts flowing also through the shunt reactors and as shown in Fig. 5 and predicted by the simulation results, at the end of fault the current carried by the HTS is only a small fraction (1.80 kA vs 18.22 kA). Another critical issue in the SFCL design is constituted by the final temperature reached by the HTS at the end of fault. Conservatively, an upper limit value of \( T = 280 \) K was set for the maximum temperature of 1G HTS to preserve its integrity. Measuring the temperature is therefore mandatory but at the same time it is hardly feasible being the short-circuit event very fast. Thus temperature has been calculated starting from silver-alloy resistance measurements evaluated in correspondence of current peaks. Such procedure gives good results under the assumption that the temperature exceeds the HTS \( T_c \) (109 K); in fact, if this condition is met, the current almost completely flows through the metallic matrix. In Fig. 6 the resistance measurements for each phase and the calculated temperatures are reported: all temperatures at the end of fault are within the limit. Finally, Fig. 7 ascertains the perfect agreement between limited current results from experiments and simulations.
5. Conclusions

In this work we reported on the development of a three-phase 9 kV/3.4 MVA Superconducting Fault Current Limiter prototype for MV applications, performed in the framework of an Italian RTD project. In particular, we briefly presented the distribution network requirements, the criteria and methodologies that have been used in the optimization of the SFCL design and the result of its acceptance tests. Qualification type test, which were aimed at testing the general design, and of acceptance type test, which were aimed at ascertaining if the device correctly meets the hosting utility requirements.

Owing to the positive results, the SFCL device is being to be installed in the A2A distribution grid in the Milano area and will be soon energized starting a one-year long field-testing activity. The next step of the research will consist in the field testing data collection, but also in developing a three-phase SFCL with rating current of 1 kA to be installed at the same substation to protect a MV/MV transformer.

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