Data-Model-Circuit Tri-Design for Ultra-Light Video Intelligence on Edge Devices

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ABSTRACT
In this paper, we propose a data-model-hardware tri-design framework for high-throughput, low-cost, and high-accuracy multi-object tracking (MOT) on High-Definition (HD) video stream. First, to enable ultra-light video intelligence, we propose temporal frame-filtering and spatial saliency-focusing approaches to reduce the complexity of massive video data. Second, we exploit structure-aware weight sparsity to design a hardware-friendly model compression method. Third, assisted with data and model complexity reduction, we propose a sparsity-aware, scalable, and low-power accelerator design, aiming to deliver real-time performance with high energy efficiency. Different from existing works, we make a solid step towards the synergized software/hardware co-optimization for realistic MOT model implementation. Compared to the state-of-the-art MOT baseline, our tri-design approach can achieve 12.5× latency reduction, 20.9× effective frame rate improvement, 5.83× lower power, and 9.78× better energy efficiency, without much accuracy drop.

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1 INTRODUCTION
The past decade has witnessed a tremendous success of deep neural networks (DNNs) [2]. In this paper, we focus on DNN-based multi-object tracking (MOT), which has been used as a technological basis for video intelligence and is drastically improving the quality of human life, e.g., autonomous driving (AD) [23]. Despite a proliferation of MOT techniques [10], little research effort has been made towards the data-efficient and co-design solutions for MOT across the full software/hardware stack. Our work aims to close this gap by developing a high-throughput, low-cost, and high-accuracy video processing algorithm/hardware pipeline. We provide a holistic viewpoint on how contemporary MOT methods can be renovated to deal with massive quantities of data and high-complexity DNNs.

Despite extensive existing works, data and model efficiencies of MOT are mainly studied either from the algorithm perspective or from the model design perspective. For example, in [19], the MOT efficiency is improved by leveraging meta learning [5] to solve an instance detection problem. In addition to algorithms, several works have focused on developing model compression techniques (such as weight pruning and weight quantization) to reduce the model complexity of MOT [14, 18]. However, the efficiency of “compressed” models are evaluated without considering the practical hardware platform, such as low-power FPGAs. Known FPGA acceleration techniques [8, 25] do not explore data sparsity or model sparsity, thereby missing huge optimization opportunities. Additionally, existing accelerators are evaluated on the ImageNet dataset with small input image sizes and do not scale to real-world High-Definition (HD) video frames, limited by the device and/or design tool capabilities. To the best of our knowledge, there is no prior work that discusses efficient implementation of MOT on the edge for HD video processing by fully utilizing data- and model-level sparsity.

Contributions. To close the gap between MOT algorithm design and efficient implementation, we propose a data-model-hardware tri-design approach. We summarize our contributions as follows.

• Dynamic frame filtering. We propose a reinforcement learning-based lightweight algorithm to achieve temporal data reduction.
• Spatial attention focusing. We propose a saliency-guided spatial data reduction method to eliminate uninformative pixels from both the input frames and the intermediate feature maps.
• Hardware-aware model compression. We leverage kernel-wise pattern-aware sparsity of an MOT model to achieve hardware-friendly model compression.
• Tri-design implementation and evaluation. We implement the proposed tri-design framework on a hardware platform comprising of one Xilinx ZCU104 and two Xilinx Alveo U50 FPGAs and conduct extensive experiments to evaluate its effectiveness in both accuracy and on-device efficiency metrics. We demonstrate that our approach can achieve 12.5× latency reduction, 20.9× effective frame rate improvement, 5.83× lower power, and 9.78× better energy efficiency, without much accuracy drop compared to the state-of-the-art MOT baseline [16] on the BDD100K dataset [22].

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2 PRELIMINARIES AND MOTIVATION

In this paper, we focus on MOT (multiple-object tracking) which deals with massive video data. Current MOT methods are commonly built upon DNNs and follow the paradigm of tracking-by-detection [20]. QDTrack [16] is the state-of-the-art MOT algorithm introduced on the BDD100K dataset [22], one of the most representative and challenging self-driving car datasets. QDTrack employs Faster R-CNN [17] with Feature Pyramid Network (FPN) [12] as an object detection backbone network, leverages Contrastive Learning [21] to optimize the backbone network parameters, and utilizes Bi-directional Softmax [16] in the embedding space for object association and tracking. The focus of this work is not to develop new MOT model algorithms but to instead build a high-throughput, low-cost, and high-accuracy video processing implementation pipeline across the full data-processing/DNN operation/hardware stack.

The computational landscape of MOT has been rapidly evolving on dedicated computing hardware (e.g., FPGAs and ASICs) [24]. Despite the advancements of hardware accelerators [11] and software/hardware co-design techniques [8], critical limitations still exist for real-time video processing. First, there is a sharp increase not only in ML model size but also computation complexity, especially for HD video frames. With HD inputs, any two $3 \times 3$ convolution layers of ResNet-50 already have higher complexity than the entire ResNet-50 with ImageNet inputs. This asserts huge pressure for real-time inference on hardware. Second, both the hardware devices and design tools exhibit poor scalability. For example, the most powerful FPGA till date, Xilinx Alveo U55C, has 9,024 DSP slices. It can provide peak performance of 2,256 GOPs for QDTrack (157.9 GOPs), but the performance upper bound is 70 ms per frame, which is far from real-time requirement. Meanwhile, the design tools are strictly limited by the largest parallelism that can be supported. For example, Xilinx Vitis HLS tool constrains that the parallelism factor should be lower than 4096 [1], while Intel Design Toolkit does not support more than 256 concurrent kernels. With larger parallelism, hardware designs can easily take days or even weeks to synthesize, which drastically increases the development cycle and the time-to-market (TTM). Consequently, there is still a huge gap between the low-power real-time video processing requirements and the limited capability of existing hardware acceleration techniques.

As inspired by above, our work advances the design of practical MOT systems by tackling the following challenges (C1–C3). (C1): The massive video data and their high frame rates make the implementation of MOT prohibitively expensive in energy and latency. Thus, our first goal is to develop novel data complexity reduction techniques that can fully exploit the temporal and saliency redundancy of video frames over time and space. (C2): SOTA DNN-based MOT models typically contain gigantic number of weights making them poor candidates for hardware implementation. To this end, we propose a hardware-friendly model compression technique for MOT. (C3): A holistic data-model-hardware full-stack design approach is lacking. It remains elusive how current MOT solutions can be applied subject to Small Size, Weight, and Power (SWaP) constraints in practice. To the best of our knowledge, there is no prior work that addresses the challenges (C1–C3) in a single unified MOT implementation pipeline.

3 METHODOLOGY

3.1 Overview of proposed approach.

The proposed data-model-hardware tri-design includes four main components as shown in Fig. 1. (Data) Temporal frame filtering. It is achieved using reinforcement learning (RL) to filter unnecessary frames at the front-end data processing stage and eventually reduce processing power along with latency costs on hardware. (Data) Spatial saliency focusing. It provides the second-stage data complexity reduction by peering into the salient region of a frame to eliminate uninformative pixels. (Model) Hardware-friendly deep model pruning. It exploits the structured sparsity patterns of weights to reduce the model size on hardware without much loss of accuracy. (Hardware) Backend acceleration. Guided by the algorithmic pipeline, it adopts low-power FPGAs to achieve realistic implementation of MOT with high throughput, low latency, and high energy efficiency. In a nutshell, components 1 and 2 are designed for tackling the data complexity challenge (in response to C1); Component 3 reduces the complexity of backend model (in response to C2); Component 4 unveils the practical efficiency of hardware solutions for MOT (in response to C3).

3.2 Data complexity reduction

3.2.1 RL-based temporal frame filtering. The embedded MOT solution requires a high throughput in terms of the number of frames that can be processed in unit time. The frame processing rate should also consider the practical latency cost. Considering the massive quantities of video frames, achieving a video processing rate of less than 30ms (for real-time inference) becomes implausible even on high-end FPGAs. Due to this hardware constraint, it is necessary to reduce the data complexity through the lens of temporal video frame dropping. Particularly, in the AD (autonomous driving) datasets, consecutive video frames may contain largely-overlapped frame content such as street and road scenes. Thus, temporal frame filter is not only necessary but also reasonable for real-time MOT. In our preliminary experiments, we test a random filtering policy with different dropping ratios. As shown in Fig. 7, dropping frames randomly significantly hampers the object tracking performance. The incapability of random filtering drives us to design a lightweight learning-based solution that can self-adjust the frame dropping scheme based on the task-end tracking performance.

Inspired by above, we propose an RL-based policy network for temporal frame filtering. Our policy network takes the current frame and the difference between the current frame and the previous frame as inputs. At the beginning of the policy network, we adopt a lightweight 3-layer convolutional network to extract a 2D...
We propose a method that achieves spatial saliency by detecting and characterizing video sequence $p$. The output is a localized sub-image for each frame, where $p$ might still have responses "leaked" from neighborhood unfiltered areas, caused by filter stride, padding, etc.

3.2.2 Spatial saliency focusing. Based on the first-stage temporal filtering, we next propose the second-stage data reduction, which attentively focuses on the salient region of a frame and its feature map to eliminate uninformative pixels.

Towards the goal of spatial reduction, our MOT model (i.e., QD-Track) achieves spatial saliency by detecting and characterizing important spatial signals while monitoring high-rate video streams with low latency. The output is a localized sub-image for each frame, on which the subsequent backend algorithm on FPGA can focus. We use the number of ID Switches per frame (i.e., IDSw in Sec. 4.1) as the reward function to evaluate the quality of frame dropping: $R(v') = -\text{IDSw}(v')/n'$, where $n'$ is the number of remaining frames in the video sequence $v'$. In (1), inspired by [26], we also regularize the salience scores $G(v_i)$ with a hyperparameter $\mu$ to avoid the case of no frame dropping and obtaining high reward for free.

$J = -R(v') \sum_{i=1}^{n} \log p(G(v_i)) + a \sum_{i=1}^{n} (G(v_i) - \mu)^2,$

where $R(v')$ is the reward of the updated video sequence $v'$ and $p(G(v_i))$ is the probability to sample an individual frame $v_i$. We use the number of ID Switches per frame (i.e., IDSw in Sec. 4.1) as the reward function to evaluate the quality of frame dropping: $R(v') = -\text{IDSw}(v')/n'$, where $n'$ is the number of remaining frames in the video sequence $v'$. In (1), inspired by [26], we also regularize the salience scores $G(v_i)$ with a hyperparameter $\mu$ to avoid the case of no frame dropping and obtaining high reward for free.

3.3 Model pruning for computation reduction

The SOTA tracking model is overwhelmingly large. It has been proven that model pruning is an efficient way to reduce model complexity. For effective and efficient hardware implementation, structured pruning is much more beneficial compared to unstructured pruning, as the latter introduces additional overhead such as sparse representation and format conversion. Furthermore, unstructured pruning hinders full utilization of parallel architectures [3]. Therefore, we advocate for and propose structured pruning to fully accommodate our hardware design.

3.3.1 Kernel-wise sparsity embedded in irregular weight pruning. The SOTA pruning method is iterative magnitude pruning (IMP) [7], which enables aggressive weight sparsity without loss of model accuracy, as justified by the lottery ticket hypothesis [6]. In Table 1, we apply IMP to the QDTrack model and indeed observe a competitive MOT accuracy, measured by IDF1 and MOTA, as illustrated in Sec. 4. However, the weight sparsity pattern achieved by IMP is unstructured, leading to the compatibility issue with hardware. Spurred by this fact, we examine if there exists a structured sparsity pattern hidden in the irregular weight sparsity achieved by IMP. As shown in Table 1, the sparse kernel ratio, i.e., the ratio of pruned 3 x 3 kernel weights over the total number of pruned weights takes over 30% in different weight pruning ratios (from 80% to 90%). This implies that kernel-wise sparsity is embedded in irregular weight pruning on QDTrack.

3.3.2 Integration with irregular pattern-aware pruning. We leverage the irregular pattern-aware pruning method [13] to enforce sparse weights that cannot be covered using kernel-wise sparse patterns. The rationale behind such irregular pattern-aware pruning is that the effective area of a convolution kernel often maintains specific sparse patterns even if it does not yield kernel-wise sparsity, i.e., kernels with all zero weights. Thus, we follow [13] to pre-define irregular sparse patterns [15] for 3 x 3 kernels, and leverage them to conduct irregular but pattern-aware weight pruning. Note that pruning using a fixed number of pre-defined sparse patterns facilitates efficient hardware implementation compared with the conventional irregular weight pruning.

![Pattern-aware convolution kernels](image)

![Binary sparse pattern mask](image)
Together with kernel-wise pruning, we propose the following hardware-aware pruning method:

- Call IMP to achieve the irregular weight sparse mask $M_{IMP}$;
- Extract kernel-wise sparsity mask $M$ from $M_{IMP}$;
- Conduct irregular pattern-aware pruning on remaining weights identified by $(1 - M)$, then update $M$ to obtain a new mask $M'$;
- Retrain non-zero model weights under fixed pruning mask $M'$.

### 3.4 Hardware implementation and acceleration

#### 3.4.1 Patch dropping compatible tile-based accelerator design

Given HD input frames and the large ML model, the intermediate feature map for even a single layer is too large to be fully stored in the device’s on-chip memory. Therefore, it is required that the input images and feature maps be partitioned into tiles and load/compute tile-by-tile, as shown in Fig. 4(a). Fortunately, incorporating our patch dropping strategy, a tile-based accelerator design is beneficial since it allows the accelerator to completely skip the loading and computing of a tile if it is dropped at an early stage; this not only reduces the computation latency but also significantly reduces energy consumption, since off-chip data movement is much more power consuming than on-chip computation [4].

#### 3.4.2 Pruning-aware and multi-level parallelism

To achieve extremely high parallelism and to simultaneously exploit structured pruning, we propose a novel multi-level pruning-aware parallelization architecture, as illustrated in Fig. 4. Consider one convolution layer as an example, where the input is a data tile of size $T_I \times T_W \times T_C$ along with a weight kernel of size $K \times K \times T_C$. The commonly adopted parallel computation is along the $T_C$ dimension, i.e., $T_C$ channels are computed simultaneously [8]. However, such a parallelization scheme fails to employ the structured and pattern-based pruning, since a pruned-away channel in a kernel still needs to be computed with other channels in parallel. Therefore, in this work, we explore the parallelism along $T_I$ and $T_W$ dimensions in two levels, and exploit the sparsity along $T_C$ dimension.

First, row-level parallelism, as shown in Fig. 4(b), allows that at each clock cycle, one input row is computed with $K$ rows of a kernel, followed by self-accumulation for partial sum. Second, for column-level parallelism as shown in Fig. 4(c), within the same clock cycle, $T_W$ multiplications are executed, followed by a $K$-to-1 adder tree. Third, since the row-level and column-level approaches have provided sufficient parallelism, we perform the convolution channel-by-channel sequentially without sacrificing computation latency. As shown in Fig. 4(d), if one channel of a filter is pruned, we skip the data loading and computation for that channel, reducing energy and latency almost linearly. Specifically, with structured pruning, if $p\%$ channels are pruned away within a filter, the latency linearly reduces by $p\%$. Similarly, for pattern-based pruning, our proposed design uses a fixed sparsity pattern for the entire channel.

#### 3.4.3 Dataflow architecture using multi-FPGA for scalability

To overcome the device and design tool scalability issue, as mentioned in Sec. 2, we propose a novel dataflow architecture using multiple FPGAs, as illustrated in Fig. 5. Instead of executing the entire model on a giant FPGA with extremely high parallelism, which is
we dissemble the ML model into components and map them to different FPGAs. As demonstrated in Fig. 5, multiple FPGAs work in a dataflow manner: 1) The first FPGA executes the backbone ResNet-50 computation for one frame and meanwhile passes the intermediate feature maps to the second FPGA. Once the first FPGA finishes the backbone computation for one frame, it would start the computation for the next one. 2) The second FPGA starts the computation as soon as it receives the first tile of intermediate feature maps. Such a dataflow architecture not only significantly reduces end-to-end latency but also increases the throughput by overlapping the computations of multiple frames. In addition, it resolves the scalability issue of both the device and the development tool as each FPGA can be developed independently.

4 EXPERIMENTS

4.1 Experiment setup

We conduct the MOT task under the BDD100K dataset [22], one of the most representative and challenging self-driving car datasets that incorporates geographic, environmental, weather diversity and intentional occlusions. It contains 100K videos with 30 frames per second. In our experiments, the training set has 1,400 videos and the validation set has 200 videos.

To evaluate the accuracy performance of our proposed tri-design approach, we adopt the standard MOT metrics, ID F1 Score (IDF1) and Multi-Object Tracking Accuracy (MOTA). These are two aggregated metrics widely used to evaluate the overall tracking performance by taking into account object detection accuracy and tracking consistency. In addition, we use the number of Identity Switches (IDSw) metric to evaluate the RL reward function in the first stage of data complexity reduction.

To evaluate the efficiency of hardware implementation of our proposed tri-design approach, we demonstrate the QDTrack model on a dataflow cluster composed of three FPGAs: two mid-end Xilinx Alveo U50 boards (5,952 DSPs, 28 MB on-chip memory), and one low-end Xilinx ZCU104 (1,728 DSPs, 1.37 MB on-chip memory) board. The accelerator is developed using Vitis HLS 2021.1 and deployed using Vivado 2021.1.

4.2 Experiment results

4.2.1 Results on video frame dropping. We peer into the effect of the RL-based frame dropping model on our proposed tri-design pipeline. We compare our frame dropping approach with two baselines: uniform dropping and random dropping. The former one drops the frames at a fixed time window for each video, and the latter one randomly selects and drops frames in a video stream. Fig. 7 shows the frame dropping performance at different drop rates from 15% to 60%. As can be seen, our RL-based model generally outperforms the random drop model at different dropping ratios, indicating the effectiveness of the RL-based frame dropping model. We also observe that the ‘sweet’ dropping ratio is achieved around 40%, which strikes the most graceful balance between spatial reduction and IDSw. In what follows, unless specified otherwise, we will assume that 40% temporal frame reduction is applied to MOT.

4.2.2 Results on saliency-based image patch dropping. We also studied the effect of spatial patch dropping in our framework. In Fig. 6, we compare the saliency-based method with random dropping versus different patch drop sizes. As can be seen, our RL-based model generally outperforms the random dropping baseline at different patch size. We also observe that IDF1 and MOTA have similar performance for sizes smaller than 175 × 175, and they start to decrease if the drop patch size becomes larger than 175 × 175. Therefore, we set the drop patch size as 60 × 60 in other experiments along with drop ratio as 20% so as to maintain the IDF1 accuracy around 0.7.

4.2.3 Results on model pruning. We compare our proposed model compression method with two commonly-used pruning baselines: irregular weight magnitude pruning (IMP) and channel-wise structured pruning. The results are demonstrated in Fig. 7. As can be seen, channel-wise pruning is quite sensitive to the pruning ratio. By contrast, our proposed hardware-aware pruning method is capable of achieving MOT performance similar to IMP across different pruning ratios. Additionally, in Table 2 we show that when integrating with the spatiotemporal data reduction algorithms, our proposed hardware-aware pruning method yields back-end acceleration according to the performance of on-board latency and the effective video frame rate.

4.2.4 Tri-design performance. We next summarize the performance of integrated frame dropping, patch dropping, and model compression. In Table 2, we demonstrate both MOT accuracy and hardware...
implementation efficiency metrics of our proposed tri-design approach. The baselines include the original QDTrack [16] implementation on GPU Tesla V100 and the Xilinx FPGA Alveo U50 cluster (Section 3.4, Fig. 5). We present the results of different configurations of data complexity reduction and model weight pruning; each configuration results in one variant of the proposed tri-design method. Accuracy. As we can see, the use of proposed data complexity reduction strategy (i.e., the row ‘Variant’) does not hamper the MOT accuracies in terms of IDF1 and MOTA scores. Throughput. Comparing to GPU baseline, our tri-design approach reduces latency by 1.37× and improves the effective frame rate (EFR) by 1.67×; comparing to FPGA baseline, our tri-design together with proposed sparsity-aware multi-level parallelism reduces latency by 12.5× and improves the EFR by 20.9×, demonstrating significant performance boost. Energy Efficiency. Meanwhile, our approach shows remarkable energy efficiency. The baseline GPU Tesla V100 has a power consumption of 296W, while our FPGA cluster has only 50.8W, leading to 9.78× power reduction. Together with 1.67× higher frame rate, the energy efficiency is 9.78× higher (5.83× × 1.67). To summarize, our approach outperforms GPU and FPGA baselines in all hardware efficiency metrics with negligible accuracy loss.

5 CONCLUSIONS

We introduce data-model-hardware tri-design for MOT implementation on the edge devices, which exploits aggressive data reduction, model compression, and ultra-low-power hardware innovation for a hardware-aware ultra-light algorithm development. We demonstrate the effectiveness of the proposed tri-design through extensive experiments. Compared to SOTA MOT baseline, our approach on Alveo U50 FPGAs achieves 12.5× latency reduction, 20.9× effective frame rate improvement, 5.83× lower power, and 9.78× better energy efficiency comparing to Tesla V100 GPU.

Table 2: Performance comparison of our proposal with its variants and the QDTrack [16] baselines (implemented by GPU and FPGA respectively) under various metrics including accuracy (IDF1 and MOTA) and hardware metrics given by on-board latency in the unit of millisecond, effective frame rate (EFR) in the unit of FPS, and power in the unit of Watt. The data reduction is implemented using 40% temporal frame dropping together with 20% spatial patch dropping. The ‘×’ indicates the case of no data/model compression, and ‘—’ means not applicable. The improvement of our proposed tri-design approach over GPU and FPGA baselines are summarized.

| Methods                 | Data/model compression | Pruning | Metrics                      | Power | Energy Efficiency (↓) |
|-------------------------|------------------------|---------|------------------------------|-------|-----------------------|
| QDTrack (GPU baseline)  | ×                      | ×       | IDF1 (↑) 0.714 (↑)           | 60.9  | 9.78×                 |
| QDTrack on FPGA          | ×                      | ×       | MOTA (↑) 0.637 (↑)           | 22.5  | 13.2× /frame          |
| Variant: Frame + patch drop | (40%, 20%)          | ×       | Latency (↓) 1.37× ×         | 4.4   | 3.7× /frame           |
| Tri-design (ours)        | (40%, 20%)            | 90%     | EFR (↑) 2.3 (↑)              | 50.8  | 22.9× /frame          |
| Improv. over GPU baseline| —                     | —       | IDF1 (↓) 3.14% (↓)           | —     | —                     |
| Improv. over FPGA baseline| —                     | —       | MOTA (↓) 3.14% (↓)           | —     | —                     |

Figure 7: Performance comparison: Left: Temporal filtering; Right: Pruning.

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