A Mixed Precision, Multi-GPU Design for Large-scale Top-K Sparse Eigenproblems

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Abstract—Graph analytics techniques based on spectral methods process extremely large sparse matrices with millions or even billions of non-zero values. Behind these algorithms lies the Top-K sparse eigenproblem, the computation of the largest eigenvalues and their associated eigenvectors. In this work, we leverage GPUs to scale the Top-K sparse eigenproblem to bigger matrices than previously achieved while also providing state-of-the-art execution times. We can transparently partition the computation across multiple GPUs, process out-of-core matrices, and tune precision and execution time using mixed-precision floating-point arithmetic. Overall, we are 67× faster than the highly optimized ARPACK library running on a 104-thread CPU and 1.9× than a recent FPGA hardware design. We also determine how mixed-precision floating-point arithmetic improves execution time by 50% over double-precision, and is 12× more accurate than single-precision floating-point arithmetic.

I. INTRODUCTION

Modern data science and numerical mathematics applications operate on larger and larger data, often with strict requirements of minimizing execution time and power consumption. For many of these applications, hardware accelerators such as Graphics Processing Units (GPUs) and Field Programmable Gate Arrays (FPGAs) are a highly-effective solution, especially when mixed-precision and reduced-precision arithmetic come into play [1]–[6]. As spectral methods become ubiquitous in the large scale graph pipelines of Spectral Clustering [7], Information Retrieval (IR) [8] and ranking [9], such techniques require algorithms that can compute only a subset of the most relevant eigenvalues (i.e. the largest in modulo) and their associated eigenvectors while taking advantage of the sparsity of real-world graphs. Graph analytics pipelines usually operate on graphs with millions or even billions of edges, rendering traditional methods computing all eigenvalues impractical, as their space and time cost scales at least quadratically with the number of vertices. As the size of real-world graphs exceeds the device memory size of modern GPUs, an eigensolver must be able to handle out-of-core matrices as well as be capable of distributing the computation to multiple GPUs. Moreover, they need to support different numerical data types for storage and computation to meet storage and accuracy requirements.

In this work, we introduce a novel Top-K GPU eigensolver for real-valued, sparse matrices capable of handling matrices with billion of non-zero entries, of partitioning the computation across multiple GPUs and leveraging mixed-precision arithmetic to optimize accuracy and execution time. We compare how our eigensolver against state-of-the-art CPU and FPGA implementations and investigate how mixed-precision enables intermediate operations with higher precision while results are stored with space-efficient representations.

In summary, we present the following contributions:

• A multi[GPU] mixed precision, Top-K eigensolver that can process out-of-core sparse matrices with billions of non-zeros. To the best of our knowledge, this is the largest amount reported in the literature (Section III).
• A performance evaluation of our CPU eigensolver against state-of-the-art Top-K eigensolvers on multiple architectures. We are on average 67× faster than a multi-core CPU implementation and 1.9× than an FPGA hardware design, with average reconstruction error below 10−5 (Section IV-B).
• A characterization of mixed-precision arithmetic in terms of accuracy versus execution time. We prove how mixed-precision is 50% faster than double-precision floating-point arithmetic, and 12× more accurate than single-precision (Section IV-D).

II. RELATED WORK

Although solving Top-K sparse eigenproblems is computationally demanding and has strong practical applications, little prior research optimizes them with hardware accelerators. On GPUs, most Top-K eigensolvers are domain-specific, do not support large-scale inputs and multiple devices, or are outright not supported on modern GPUs architectures [10]–[12]. The nvGRAPH library [13] by Nvidia uses internally the Lanczos algorithm, whose implementation is, however,
Our sparse eigensolver employs a two-phase algorithm, as in Figure 1. The first step is based on the Lanczos [19] algorithm, which takes as input the original matrix \(M\), the number of desired eigencomponents \(K\) and a \(L2\)-normalized random vector \(v_{1} \in \mathbb{R}^{n}\). The algorithm proceeds by incrementally building a Kiryllov subspace (the Lanczos vectors \(V\)) of \(M\), through vector projections (Algorithm 1, line 9) and orthogonalizations (lines 11–21). A tridiagonal matrix \(T\) stores the residuals of the previous operations (lines 6, 10) and reduces the problem from size \(n \times n\) to one of size \(K \times K\) (\(K \ll n\)).

The second phase employs the Jacobi algorithm [20] to solve the eigenproblem on the much smaller matrix \(T\). The Jacobi algorithm stores the eigenvalues of \(M\) in the main diagonal of \(T\), and the eigenvectors of \(T\) in \(V\). The eigenvectors of \(M\) are given by \(VV\).

### A. Optimizing sparse eigensolvers for GPUs

We desire to render our GPU sparse eigensolver scalable to real-world matrices with billions of non-zero values, often encountered in graph analytics. To do so, we devise a workload partition scheme that distributes the computation acros multiple GPUs while minimizing unnecessary data movements and synchronization events.

The Lanczos algorithm has two synchronization points (Algorithm 1, lines 6 and 10), corresponding to the computation of \(\alpha\) and \(\beta\) (Figure 1(A) 3). Another optional synchronization point occurs if reorthogonalization of the Lanczos vectors is needed (lines 15–18, Figure 1(C)). All other operations operate linearly on the input arrays and can be computed across multiple GPUs independently. The input matrix is partitioned by balancing the number of non-zero elements in each partition. All vectors, except for \(v_i\), are partitioned according to the same partition scheme as the input matrix. As the Sparse Matrix-Vector Multiplication (SpMV) performs indirect accesses to the vector \(v_i\), we replicate it to all GPU instead of partitioning it. There is an additional synchronization at each iteration when the previous Lanczos vector becomes the input of the SpMV. We prevent this synchronization by having each GPU copy, in a round-robin fashion, a single partition to a single replica of \(v_i\) (Figure 1(C)). When all GPUs have completed a cycle, \(v_i\) has been fully copied, and the computation can proceed to a new iteration.

The orthogonality of the Lanczos vectors and the quality of the final eigencomponents produced crucially depends on the output of the scalar product (\(\alpha\), line 10) and the \(L2\)-norm (\(\beta\), line 6). For this reason, our eigensolver can perform the intermediate operations of each kernel in double-precision floating-point arithmetic to ensure maximum accuracy. However, vectors can still be stored in single-precision floating-point arithmetic to consume less device memory and better use the available memory bandwidth. In our experiments, other data types (half-precision FP16, BFLOAT16) resulted in numerical instability, and have been omitted from Section IV.

### III. IMPLEMENTATION

Our sparse eigensolver employs a high-bandwidth memory (HBM) controller force unnecessary data replication and allow achieving only a fraction of the maximum HBM bandwidth. To the best of our knowledge, no other work optimizes large Top-K sparse eigencomputations using architectures or domain-specific architectures (DSAs). There are numerous implementations of large-scale Top-K sparse eigenproblem solver for CPUs [15–17]. However, none is as well-known as ARPACK [18].

### Algorithm 1 Top-K eigenvalues/vectors Lanczos algorithm

Require: Input Matrix \(M\), partitioned in \(M_1 \ldots M_G\)
Require: \(K\), number of output eigenvectors
Require: \(L2\)-normalized input vectors \(v_1 := \{v_1^1, \ldots, v_1^G\}\)
Require: Temporary vectors \(v_{tmp}\) and next vectors \(v_{nxt}\)

1: function LANCZOS\((M, K, v_1, v_{tmp}, v_{nxt})\)
2: \(\alpha_1 \leftarrow 0; \quad \beta_1 \leftarrow 0 \quad \triangleright \text{Initialization}\)
3: for \(i \in [1, K]\) do
4: \(\triangleright \text{Normalize and compute new Lanczos vector}\)
5: if \(i \neq 1\) then
6: \(\beta_i \leftarrow \sqrt{\sum_{j=1}^{G} (v_{nxt}^j)^2} \quad \triangleright \beta_i \leftarrow \|v_{nxt}\|_2\)
7: \(v_i^{[1..G]} \leftarrow v_j^{[1..G]} / \beta_i \triangleright v_i \leftarrow v_{nxt} / \beta_i\)
8: \(\triangleright \text{Compute the next projection}\)
9: \(v_i^{[1..G]} \leftarrow \text{SpMV}(M_1 \ldots M_G, v_1^{[1..G]}))\)
10: \(\alpha_i \leftarrow \sum_{j=1}^{G} v_i^j \cdot v_j^i\)
11: \(v_i^{[1..G]} \leftarrow v_{nxt}^{[1..G]} - \alpha_i v_i^{[1..G]} - \beta_i v_1^{[1..G]}\)
12: for \(j \in [1, i]\) do \(\triangleright \text{Orthogonalization}\)
13: if \(j\%2 \neq 0\) then
14: \(o \leftarrow \sum_{k=1}^{G} v_j^k \cdot v_{n,k}\)
15: \(v_i^{[1..G]} \leftarrow v_i^{[1..G]} - o \cdot v_j^{[1..G]}\)
16: else
17: \(o \leftarrow \sum_{k=1}^{G} v_j^k \cdot v_{n,k}\)
18: \(v_i^{[1..G]} \leftarrow v_i^{[1..G]} - o \cdot v_j^{[1..G]}\)
19: if \(i == j\) then \(\triangleright \text{Copy to temporary vector}\)
20: \(v_i^{[1..G]} \leftarrow v_i^{[1..G]}\)
21: \(\triangleright \text{Tridiagonal matrix } T\) and Lanczos vectors \(V\)
22: return \(\{T = [\alpha_1, \ldots, \alpha_K], [\beta_1, \ldots, \beta_K-1]\}\)
23: return \(V = [v_1, \ldots, v_K]\)
We implemented our eigensolver using the GrCUDA API [21] and GraalVM [22] to support several high-level programming languages automatically, while we wrote the core GPU computational kernels in CUDA. Since GrCUDA internally leverages CUDA unified memory, our eigensolver can scale to out-of-core computations on sparse matrices that would not otherwise fit in the CPU memory. We also modified the internal GrCUDA runtime to schedule GPU kernels across multiple devices, using a round-robin device selection policy for kernels operating on disjoint data. Through the partition swapping presented in Section III-A we minimize unnecessary memory transfers between devices and out-of-core memory pages, guaranteeing scalability in what would be an otherwise memory and transfer-bound computation (Section IV-C). The small triadiagonal matrices that the Lanczos algorithm outputs \((\approx 24 \times 24)\) cannot saturate the stream processors of a modern GPU [23]. Instead, we achieve better execution time by performing this step on a CPU (Figure 1).

B. Implementation details

We measure results for our Top-K sparse eigensolver using up to 8 Nvidia Tesla V100s (16 GB of HBM2 for each GPU). As baselines, we employ the multi-threaded ARPACK library [18], a Top-K sparse eigensolver that uses the IRAM algorithm, running on two Intel Xeon Platinum 8176M (104 threads in total) and 755 GB of DDR4 memory, with single-precision floating point arithmetic. We also compare against the recent FPGA implementation by Sgherzi et al. [6], running on a Xilinx Alveo U280 accelerator card equipped with 8 GB of HBM2 memory. We repeat measurements 20 times, using random initialization for the Lanczos vectors \(v_1\).

To provide a fair comparison, we use the same collection of sparse matrices in Sgherzi et al. [6], enriched with two extremely large matrices (billions of non-zero entries) that do not fit in the FPGA's and GPU's device memory, and allows us to test the out-of-core performance of our GPU implementation. All matrices come from the SuiteSparse collection [24] and represent graph topologies, although the eigensolvers in our analysis can be applied to other domains as well [25].

B. Execution Time Comparison

We first compare the speed of our GPU eigensolver, when running on a single GPU against the CPU and FPGA baselines, on matrices of increasing size (Figure 2). Results have been aggregated over an increasing amount of eigenvectors \(K\), from 8 to 24, as the execution time scales linearly with \(K\). For the FPGA implementation, we use the values reported by the authors. Results of the two largest matrices (KRON and URAND) have been omitted for the FPGA hardware design as it does not support out-of-core computations.

TABLE I: Sparse matrices used in our evaluation, by increasing number of non-zero entries (in millions). We also report the memory footprint in GB of each matrix, stored as COO.

| ID | Name          | Rows (M) | Non-zeros (M) | Sparsity (%) | Size (GB) |
|----|---------------|----------|---------------|--------------|-----------|
| WB-TA | wiki-Talk    | 2.39     | 5.02          | \(8.79 \times 10^{-4}\) | 0.06 GB   |
| WB-GO | web-Google   | 0.91     | 5.11          | \(6.17 \times 10^{-4}\) | 0.07 GB   |
| WB-BE | web-Derkhan  | 0.69     | 7.60          | \(1.60 \times 10^{-3}\) | 0.10 GB   |
| FL   | Flickr        | 0.82     | 9.84          | \(1.46 \times 10^{-3}\) | 0.13 GB   |
| IT   | italy_osm     | 6.69     | 14.02         | \(3.13 \times 10^{-5}\) | 0.18 GB   |
| PA   | patents       | 3.77     | 14.97         | \(1.05 \times 10^{-4}\) | 0.19 GB   |
| VL3  | venture.evel3| 4.02     | 16.10         | \(9.96 \times 10^{-5}\) | 0.21 GB   |
| DE   | germany_osm   | 11.54    | 24.73         | \(1.86 \times 10^{-5}\) | 0.32 GB   |
| ASIA | asia_osm      | 11.95    | 25.42         | \(1.78 \times 10^{-5}\) | 0.33 GB   |
| RC   | road_central  | 14.08    | 33.87         | \(1.71 \times 10^{-5}\) | 0.43 GB   |
| WK   | Wikipedia     | 3.56     | 45.00         | \(3.55 \times 10^{-4}\) | 0.60 GB   |
| HT   | hugetrace-00020 | 16.00 | 47.80 | \(1.87 \times 10^{-5}\) | 0.61 GB   |
| WB   | wb-edu        | 9.84     | 57.15         | \(5.90 \times 10^{-5}\) | 0.73 GB   |
| KRON | GAP-kron      | 134.21   | 4294.96       | \(8.79 \times 10^{-5}\) | 51.45 GB   |
| URAND| GAP-urand     | 134.21   | 4294.96       | \(8.79 \times 10^{-5}\) | 51.45 GB   |
Fig. 3: (a) Relative execution time for increasing number of GPUs. Two outlier matrices (plotted separately) perform worse with more GPUs due to the larger inter-GPU communication. (B) Accuracy of our eigensolver, in terms of orthogonality of the eigenvectors and L2 error, for increasing $K$.

CPU and GPU use single-precision floating point arithmetic, while the FPGA hardware design uses 32-bit signed fixed point arithmetic with one bit of integer part ($\frac{1}{2} \times 30$) for Lanczos, and half-precision floating point arithmetic for Jacobi.

Our GPU eigensolver is always faster than both the CPU and FPGA baselines (on the RC matrix the difference is not statistically significant). On average, the GPU eigensolver is $67 \times$ faster than the CPU implementation and $1.9 \times$ faster than the FPGA hardware design. The FPGA hardware design is still competitive in terms of Performance/Watt, as the FPGA design consumes $38\text{W}$ [6], versus the $300\text{W}$ of the GPU [26].

As our partitioning minimizes inter-GPU data-transfer (Section III-A), we are $\approx 180\times$ faster than the CPU on very large out-of-core matrices despite storing only a small fraction of the input data on the GPU at any given time.

C. Multi-GPU Performance

Scaling the computation of the Top-K eigenvectors on sparse matrices to multiple GPUs is far from trivial, as explained in Section III-A. From Figure 3(a) we observe how our partitioning scheme improves the execution time when using multiple GPUs with somewhat diminishing returns. On average, two GPUs provide a $50\%$ speedup, while eight GPUs are close to a $100\%$ speedup. Only on two very small matrices we observe a loss of performance on systems with 4 or 8 GPUs. This phenomenon is explained by the heterogeneous NVLink interconnection found in V100-based systems like ours [27]. Some GPU pairs are not directly connected with NVLink, and data transfer has to go through the CPU and PCIe, which has $\approx 10\times$ lower bandwidth than NVLink.

D. Impact of Reorthogonalization and Mixed-precision

To measure the quality of our eigensolver, we measure the average angle that occurs between every pair of eigenvectors. Eigenvectors are by definition pairwise orthogonal, i.e. their angle is $\pi/2$, and their dot product must be 0. Figure 3(b) provides, for increasing $K$, the average orthogonality and the L2 norm of $Mv - \lambda v$, the reconstruction error computed using the definition of eigenvalues. Both results are aggregated for all matrices due to space limitations. We observe how reorthogonalization improves the results’ quality, with $\approx 2$ degrees of difference compared to the implementation without reorthogonalization. Choosing whether reorthogonalization is suitable or not depends on the application. Spectral methods in machine learning often do not demand the same numerical accuracy as engineering applications, and reorthogonalization increases the algorithmic complexity by an $O(nK^2/2)$ factor.

Employing mixed-precision arithmetic in numerical algorithms is usually a matter of trade-offs, with better precision translating to higher execution time. We visualize this behavior in Figure 4 showing for each matrix the L2 reconstruction error and the relative execution time, and a linear regression to capture the general trend. In all cases, increasing precision reduces the error and increases the execution time. The float-double-float (FDF) configuration (Section III-A) is $50\%$ faster than a pure double-precision implementation (DDD). Its error is only $40\%$ higher, and $12\times$ lower than the floating-point implementation (FFF), showing how mixed-precision arithmetic is a great compromise in Top-K sparse eigensolvers.

V. Conclusion

As graph analytics and spectral methods deal with larger and larger sparse matrices, it is critical to have high-performance Top-K sparse eigensolvers to extract low-dimensional representations of sparse datasets. We provide a novel Top-K sparse eigensolver that can scale to out-of-core matrices with billion of non-zero entries, partition the computation over multiple GPUs, and leverage mixed-precision floating-point arithmetic. We are on average $67\times$ faster than the multicore ARPACK CPU library implementation and $1.9\times$ faster...
than a state-of-the-art FPGA hardware design. As future work, we will extend our implementation to fixed-point arithmetic and validate if novel interconnection technologies such as NVSwitch can improve even further multi-GPU scaling.

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