Adaptive and Fair Transformation for Recoverable Mutual Exclusion

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Mutual exclusion is one of the most commonly used techniques to handle contention in concurrent systems. Traditionally, mutual exclusion algorithms have been designed under the assumption that a process does not fail while acquiring/releasing a lock or while executing its critical section. However, failures do occur in real life, potentially leaving the lock in an inconsistent state. This gives rise to the problem of recoverable mutual exclusion (RME) that involves designing a mutual exclusion (ME) algorithm that can tolerate failures, while maintaining safety and liveness properties.

In this work, we present a framework that transforms any algorithm that solves the RME problem into an algorithm that can also simultaneously adapt to (a) the number of processes competing for the lock, as well as (b) the number of failures that have occurred in the recent past, while maintaining the correctness and performance properties of the underlying RME algorithm. Additionally, the algorithm constructed as a result of this transformation adds certain desirable properties like fairness (a variation of FCFS) and bounded recovery.

We further extend our framework by presenting a novel memory reclamation algorithm to bound the worst-case space complexity of the RME algorithm. The memory reclamation techniques maintain the fairness, performance and correctness properties of our transformation. The technique is general enough that is may also be employed to bound the space of other RME algorithms.

One of the important measures of performance of any ME algorithm, including an RME algorithm, is the number of remote memory references (RMRs) made by a process—for acquiring and releasing a lock as well as recovering the lock structure after a failure.

Assume that the worst-case RMR complexity of a critical section request in the underlying RME algorithm is \( R(n) \), where \( n \) denotes the number of processes in the system. Then, our framework yields an RME algorithm for which the worst-case RMR complexity of a critical section request is given by \( O(\min(\bar{c}, \sqrt{F+1}, R(n))) \), where \( \bar{c} \) denotes the point contention of the request and \( F \) denotes the number of failures in the recent past of the request.

In addition to read and write instructions, our algorithm uses compare-and-swap (CAS) and fetch-and-store (FAS) hardware instructions, both of which are commonly available in most modern processors.

CCS Concepts: • Theory of computation → Concurrency; Concurrent algorithms; Distributed computing models.

Additional Key Words and Phrases: mutual exclusion, persistent memory, fault tolerance, adaptive, fairness, RMR complexity, memory reclamation

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1 INTRODUCTION

One of the most commonly used techniques to handle contention in a concurrent system is to use mutual exclusion (ME). The mutual exclusion problem was first defined by Dijkstra more than half a century ago in [9]. Using locks that provide mutual exclusion enables a process to execute its critical section (part of the program that involves accessing
shared resources) in isolation without worrying about interference from other processes. This avoids race conditions, thereby ensuring that the system always stays in a consistent state and produces correct outcome under all scenarios.

Generally, algorithms for mutual exclusion are designed with the assumption that failures do not occur, especially while a process is accessing a lock or a shared resource. However, such failures can occur in the real world. A power outage or network failure might create an unrecoverable situation causing processes to be unable to continue. If such failures occur, traditional mutual exclusion algorithms, which are not designed to operate properly in the presence of failures, may fail to guarantee important safety and/or liveness properties (e.g., system may deadlock). In many cases, such failures may have disastrous consequences. This gives rise to the recoverable mutual exclusion (RME) problem. The RME problem involves designing an algorithm that ensures mutual exclusion under the assumption that process failures may occur at any point during their execution, but the system is able to recover from such failures and proceed without any adverse consequences.

Traditionally, concurrent algorithms use checkpointing and logging to tolerate failures by regularly saving relevant portion of application state to a persistent storage such as hard disk drive (HDD). Accessing a disk is orders of magnitude slower than accessing main memory. As a result, checkpointing and logging algorithms are often designed to minimize disk accesses. Non-volatile random-access memory (NVRAM) is a new class of memory technologies that combines the low latency and high bandwidth of traditional random access memory with the density, non-volatility, and economic characteristic of traditional storage media (e.g., hard disk drive). Existing checkpointing and logging algorithms can be modified to use NVRAMs instead of disks to yield better performance, but, in doing so, we would not be leveraging the true power of NVRAMs [16, 25]. NVRAMs can be used to directly store implementation specific variables and, as such, have the potential for providing near-instantaneous recovery from failures.

Most of the application data can be easily recovered after failures by directly storing implementation variables on NVRAMs. However, recovery of implementation variables alone is not enough. Processor state information such as contents of general and special purpose CPU registers (e.g., program counter, condition code register, stack pointer, etc.) as well as contents of cache cannot always be recovered fully. In other words, recovery may be lossy, and, if not handled properly, a failure may cause the system to behave erroneously upon recovery. Due to this reason, there is a renewed interest in developing fast and dependable algorithms for solving many important computing problems in software systems vulnerable to process failures using NVRAMs. Using innovative methods, with NVRAMs in mind, we aim to design efficient and robust fault-tolerant algorithms for solving mutual exclusion and other important concurrent problems.

The RME problem in the current form was formally defined a few years ago by Golab and Ramaraju in [15]. Several algorithms have been proposed to solve this problem [8, 12, 16, 19–22]. One of the most important measures of performance of an RME algorithm is the maximum number of remote memory references (RMRs) made by a process per critical section request in order to acquire and release the lock as well as recover the lock after a failure. Intuitively, RMR complexity captures the number of “expensive” steps performed by a process. Whether or not a memory reference is considered an RMR depends on the underlying memory model. The two most common memory models used to analyze the performance of an RME algorithm are cache-coherent (CC) and distributed shared memory (DSM) models. Roughly speaking, a step is considered to incur an RMR in the CC model if it causes a memory location to be cached or a cached copy to be invalidated, and in the DSM model if it accesses data stored on a remote memory module. The CC model captures the working of the caching system used by hardware manufacturers to mask the high latency of memory, whereas the DSM model captures the NUMA (non-uniform memory access) effect observed in machines.
Table 1. Comparison of known solutions to recoverable mutual exclusion problem with respect to RMR complexity under three different scenarios.

| Algorithm | RMR Complexity | Adaptive to Contention |
|-----------|----------------|------------------------|
|           | No failures    | Limited failures       | Arbitrarily number of failures |
| Golab and Ramaraju’s transformation for recoverability [16, Section 4.1] using MCS lock | \( O(1) \) | \( O(n^F + 1) \) | unbounded | No |
| Golab and Ramaraju’s transformation for bounding RMR complexity [16, Section 4.2] using MCS lock | \( O(1) \) | \( O(n) \) | \( O(n) \) | No |
| Golab and Hendler’s arbitration tree using \( k \)-port MCS lock*†‡ | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | No |
| Jayanti and Joshi’s wait-free recoverable lock [20] | \( O(\log n) \) | \( O(\log n) \) | \( O(\log n) \) | No |
| Jayanti, Jayanti and Joshi’s arbitration tree using \( k \)-port MCS lock [21] | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | No |
| Chan and Woelfel’s array-based recoverable lock‡ | \( O(1) \) | \( O(n^F + 1) \) | unbounded | No |
| Katzman and Morrison’s abortable and recoverable lock [12] | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | \( O(\log n/\log \log n) \) | Yes |
| Our recoverable lock (this work)† | \( O(1) \) | \( O(n^F + 1) \) | \( O(\log n/\log \log n) \) | Yes |

* the number of processes in the system
† the number of failures in the system
‡ RMR complexity measures only hold for the CC model
‡† RMR complexity is constant in the amortized case

with large number of cores when memory is partitioned into multiple modules. Hereafter, any RMR complexity bounds mentioned in the text is assumed to hold for both CC and DSM models unless otherwise stated.

Different RME algorithms provide different trade-offs in performance guarantees under different failure scenarios. For example, one of the RME algorithms proposed in [16] has an RMR complexity that grows linearly with the number of failures. Specifically, it has optimal RMR complexity of \( O(1) \) in the absence of failures, but its RMR complexity may grow unboundedly if failures occur repeatedly. On the other hand, the RME algorithm in [19] has an RMR complexity of \( O(\log n/\log \log n) \), where \( n \) is the number of processes in the system, irrespective of how many failures have occurred in the system (including the case when the system has not experienced any failures). Recently, Chan and Woelfel have proved a lower bound of \( \Omega(\log n/\log \log n) \) on the worst-case RMR complexity of any RME algorithm using currently available hardware instructions and practical word size of \( \Theta(\log n) \) [7]. A more detailed description of the related work is given later in section 9.

1.1 Our Contributions

Our main contribution in this work is a novel framework that transforms any algorithm that solves the RME problem into an algorithm that is simultaneously adaptive to (a) the number of processes competing for the lock, as well as (b) the number of failures that have occurred in the recent past, while having the same worst-case RMR complexity as that of the base RME algorithm. In particular, assume that the worst-case RMR complexity of a critical section request in the underlying RME algorithm is \( R(n) \), where \( n \) denotes the number of processes in the system. Then, our framework yields an RME algorithm for which the worst-case RMR complexity of a critical section request is given by \( O(\min\{\hat{c}, \sqrt{F + 1}, R(n)\}) \), where \( \hat{c} \) denotes the maximum number of requests that are simultaneously active while the given request is outstanding (referred to as point contention) and \( F \) denotes the number of failures that have occurred...
in the recent past of the given request (referred to as failure-density). Note that the RMR complexity of a request in our algorithm is high only when both point contention and failure-density of the request are high.

In addition to preserving the safety and liveness properties of the underlying RME algorithm (mutual exclusion, starvation freedom and critical section re-entry), our transformation also maintains its other desirable properties such as bounded exit and bounded recovery as applicable. Roughly speaking, an RME algorithm satisfies the bounded exit property if a process is able to leave its critical section within a bounded number of its own steps unless it fails. It satisfies the bounded recovery property if a process is able to recover from a failure within a bounded number of its own steps unless it fails again.

The key idea behind our approach is to use a solution to a weaker variant of the RME problem, which we refer to as weakly RME problem, in which a failure may cause the mutual exclusion property to be violated temporarily albeit in a controlled manner, repeatedly as a “filter” to limit contention and achieve adaptability. To that end, we present an efficient algorithm for a weakly RME algorithm that has optimal RMR complexity of only $O(1)$.

We also show that our RME algorithm is fair; in particular, it satisfies a variant of the first-come-first-served (FCFS) property, which we refer to as CI-FCFS. Intuitively, CI-FCFS guarantees first-come-first-served (FCFS) order among requests provided their recent past is failure-free.

Finally, we design a novel memory reclamation algorithm that enables us to bound the space complexity of our weakly RME algorithm by $O(n^2)$. This, in turn, enables us to bound the space complexity of the algorithm generated by our framework by $O(n^2 \cdot R(n) + S(n))$, where $S(n)$ denote the space complexity of the underlying RME algorithm.

1.2 Organization of the Text

The rest of the text is organized as follows.

We describe our system model and formally define the RME problem in section 2. We define the weaker variant of the RME problem and its properties in section 3.

We present a highly efficient solution to the weaker variant of the RME problem with constant RMR complexity in section 4. In section 5.1, we present a framework to transform any given RME algorithm into a new RME algorithm that preserves the worst-case RMR complexity of the original RME algorithm but has lower RMR complexity in the absence of failures. This transformation uses a solution to the weaker variant of the RME problem as a building block. Applying this transformation recursively, we create a new transformation in section 5.2 that preserves the worst-case RMR complexity of the original RME algorithm and whose performance degrades sub-linearly with the number of “recent” failures (specifically, in proportion to $\sqrt{F}$). This transformation achieves the desired RMR complexity for each of the three scenarios mentioned earlier (as shown in table 1). In section 6, we discuss the fairness guarantee provided by our RME algorithms (weakly as well as strongly recoverable).

In section 7, we present a recoverable broadcast object with constant RMR complexity that allows a process to notify other processes that are waiting on it to reach a certain point in its execution. We use the broadcast object to design a recoverable memory reclamation algorithm that bounds the space-complexity of our (recursive) framework while maintaining its RMR complexity in section 8.

A detailed description of the related work is given in section 9. Finally, in section 10, we present our conclusions and outline directions for future research.

2 SYSTEM MODEL AND PROBLEM FORMULATION

We follow the same model as used by Golab and Ramaraju in their work on recoverable mutual exclusion (RME) [16].
2.1 System model

We consider an asynchronous shared-memory system consisting of \( n \) unreliable processes labeled \( p_1, p_2, \ldots, p_n \). Shared memory is used to store variables that can be accessed by any process. Besides shared memory, each process also has its own private memory that is used to store variables that can only be accessed by that process (e.g., program counter, CPU registers, execution stack, etc.). Processes can only communicate by performing read, write and read-modify-write (RMW) instructions on shared variables. Processes are not assumed to be reliable and may fail.

A system execution is modeled as a sequence of process steps. In each step, some process either performs some local computation affecting only its private variables or executes one of the available instructions (read, write or RMW) on a shared variable or fails. Processes may run at arbitrary speeds and their steps may interleave arbitrarily. In any execution, between two successive steps of a process, other processes can perform an unbounded but finite number of steps.

2.2 Failure model

We assume the crash-recover failure model. A process may fail at any time during its execution by crashing. A crashed process recovers eventually and restarts its execution. A crashed process does not perform any steps until it has restarted. A process may fail multiple times, and multiple processes may fail concurrently.

Note that, upon restarting after a failure, the state of the lock as well as the underlying application utilizing the lock needs to be restored to a proper condition. In this work, we focus only on the recovery of the internal structure of the lock. Restoring the application state to its proper condition (using logs and/or persistent memory) is assumed to be the responsibility of the programmer and is beyond the scope of this work \[12, 16, 19\].

We assume that, upon crashing, a process loses the contents of its private variables, including but not limited to the contents of its program counter, CPU registers (general and special purpose) and execution stack. However, the contents of the shared variables remain unaffected and are assumed to persist despite any number of failures. When a crashed process restarts, all its private variables are reset to their initial values.

Processes that have crashed are difficult to distinguish from processes that are running arbitrarily slow. However, we assume that every process is live in the sense that a process that has not crashed eventually executes its next step and a process that has crashed eventually recovers. In this work, we consider a failure to be associated with a single process. If a failure causes multiple processes to crash, unless otherwise stated, we treat each process crash as a separate failure.

2.3 Process execution model

A process execution is modeled using two types of computations, namely non-critical section and critical section. A critical section refers to the part of the application program in which a process needs to access shared resources in isolation. A non-critical section refers to the remainder of the application program.

If multiple processes access and modify shared resource(s) concurrently, it may lead to race conditions which may prevent the application from working properly and may possibly have disastrous consequences. To avoid such race conditions, a lock (or a mutual exclusion (ME) algorithm) is used to enable each process to execute its critical section in isolation. At most one process can hold the lock at any time, and a process can execute its critical section only if it is holding the lock. The lock can be granted to another request only after the process (more specifically, request) holding
Algorithm 1: Process execution model.

```plaintext
while true do
    Non-Critical Section (NCS)
    Recover
    Enter
    Critical Section (CS)
    Exit
end while
```

the lock releases it after completing its critical section. Hereafter, we use the terms “mutual exclusion algorithm”, “ME algorithm” and “lock” interchangeably.

The execution model of a process with respect to a lock is depicted in algorithm 1. As shown, a process repeatedly executes the following five segments in order: NCS, Recover, Enter, CS and Exit. The first segment, referred to as NCS, models the steps executed by a process in which it only accesses variables outside the lock. The second segment, referred to as Recover, models the steps executed by a process to perform any cleanup required due to past failures and restore the internal structure of the lock to a consistent state. The third segment, referred to as Enter, models the steps executed by a process to acquire the lock so that it can execute its critical section in isolation. The fourth segment, referred to as CS, models the steps executed by a process in the critical section where it accesses shared resources in isolation. Finally, the fifth segment, referred to as Exit, models the steps executed by a process to release the lock it acquired earlier in Enter segment.

We assume that, in the NCS segment, a process does not access any part of the lock or execute any computation that could potentially cause a race condition. Moreover, in the Recover, Enter and Exit segments, a process accesses shared variables pertaining to the lock (and the lock only). Our execution model only considers steps taken by a process during its Recover, Enter or Exit segments.

A process may crash at any point during its execution, including while executing the NCS, Recover, Enter, CS or Exit segment. We assume that a crashed process upon restarting starts its execution from the beginning of the loop shown in algorithm 1, specifically from the beginning of NCS segment. Note that any steps executed by a process to recover the application state are not explicitly modeled here. Specifically, both NCS and CS segments may consist of code in the beginning to recover relevant portions of the application state.

In the rest of the text, by the phrase “acquiring a recoverable lock,” we mean “executing Recover and Enter segments (in order) of the associated RME algorithm.” Likewise, by the phrase “releasing a recoverable lock,” we mean “executing Exit segment of the associated RME algorithm.”

**Definition 2.1 (passage).** A passage of a process is defined as the sequence of steps executed by the process from when it begins executing Recover segment to either when it finishes executing the corresponding Exit segment or experiences a failure, whichever occurs first.

**Definition 2.2 (failure-free passage).** A passage of a process is said to be failure-free if the process has successfully executed Recover, Enter and Exit segments of that passage without experiencing any failures.

**Definition 2.3 (super-passage).** A super-passage of a process is a maximal non-empty sequence of consecutive passages executed by the process, where only the last passage of the process in the sequence can be failure-free.

**Definition 2.4 (failure-free super-passage).** A super-passage of a process is said to be failure-free if it consists of exactly one passage.
For ease of exposition, if a process has a super-passage in-progress \((i.e., \text{not completed})\), then we say that the process has a pending or outstanding \textit{request} for a critical section or super-passage. Note that a process may execute multiple failure-free CS segments during its. This is because a super-passage is considered to be complete only after the process has completed a failure-free passage, which includes Exit segment. We consider all these CS segments to be associated with the \textit{same} request.

2.4 Problem definition

A \textit{history} is a collection of steps taken by processes. A process \(p\) is said to be \textit{live} in a history \(H\) if \(H\) contains at least one step by \(p\). We assume that every critical section is finite.

\textbf{Definition 2.5 (fair history).} A history \(H\) is said to be \textit{fair} if (a) it is finite, or (b) if it is infinite and every live process in \(H\) either executes infinitely many steps or stops taking steps after a failure-free passage.

Designing a recoverable mutual exclusion (RME) algorithm involves designing Recover, Enter and Exit segments such that the following correctness properties are satisfied.

\textbf{Mutual Exclusion (ME)} For any history \(H\), at most one process is in its CS at any point in \(H\).

\textbf{Starvation Freedom (SF)} Let \(H\) be an infinite fair history in which every process fails only a finite number of times during each of its super-passage. Then, if a process \(p\) leaves the NCS segment in some step of \(H\), then \(p\) eventually enters its CS segment.

\textbf{Bounded Critical Section Reentry (BCSR)} For any history \(H\), if a process \(p\) crashes inside its CS segment, then, until \(p\) has reentered its CS segment at least once, any subsequent execution of Enter segment by \(p\) either completes within a bounded number of \(p\)’s own steps or ends with \(p\) crashing.

Note that mutual exclusion is a safety property, and starvation freedom is a liveness property. The bounded critical section reentry is a safety as well as a liveness property. If a process fails inside its CS, then a shared object or resource \((e.g.,\ a\ \text{shared data structure})\) may be left in an inconsistent state. The bounded critical section reentry property allows such a process to “fix” the shared resource if needed before any other process can enter its CS \((e.g.,\ [12, 16, 19])\). This property assumes that a CS is idempotent in the sense that, within the same super-passage, executing a CS multiple times, possibly partially in some cases, is equivalent to executing it once. Our correctness properties are the same as those used in \([12, 16, 19]\). We have stated them here for the sake of completeness. In addition to the correctness properties, it is also desirable for an RME algorithm to satisfy the following additional properties.

\textbf{Bounded Exit (BE)} For any infinite history \(H\), any execution of the Exit segment by any process \(p\) either completes in a bounded number of \(p\)’s own steps or ends with \(p\) crashing.

\textbf{Bounded Recovery (BR)} For any infinite history \(H\), any execution of Recover segment by process \(p\) either completes in a bounded number of \(p\)’s own steps or ends with \(p\) crashing.

2.5 Performance measures

We measure the performance of RME algorithms in terms of the number of \textit{remote memory references (RMRs)} incurred by the algorithm during a \textit{single} passage \((i.e.,\ Recover, Enter and Exit segments)\). The definition of a remote memory reference depends on the memory model implemented by the underlying hardware architecture. In particular, we consider the two most popular shared memory models:
Cache Coherent (CC) The CC model assumes a centralized main memory that acts as a global, shared store of variables. In addition, each process has a local cache memory. Whenever a process accesses (reads or writes) a variable, a copy of the variable is stored in the cache of that process. Any subsequent access to that variable is serviced using that cached copy as long as the copy is still valid. A write access causes other cached copies of the variable to be either updated or invalidated. In addition, it may also cause the copy stored in the main memory to be updated. In this model, a step incurs an RMR if it causes the contents of any of the caches to be modified (including invalidation).

Distributed Shared Memory (DSM) The DSM model assumes that the main memory is partitioned into multiple memory modules with one module attached to every process. A process can access a variable stored on any memory module, be it local or remote. However, accessing a variable stored on its local module is much faster than accessing the one stored on a remote module. In this model, a step incurs an RMR if it involves accessing a variable stored on a remote memory module.

In the rest of the text, if not explicitly specified, the RMR complexity measure of an algorithm applies to both CC and DSM models.

We analyze the RMR complexity of an RME algorithm under three scenarios: (a) in the absence of failures (failure free RMR complexity), (b) in the presence of F failures (limited failures RMR complexity), and (c) in the presence of an unbounded number of failures (arbitrary failures RMR complexity).

Let \( g(n, F) \) be a function of \( F \) and \( n \), where \( n \geq 1 \) is the number of processes in the system and \( F \geq 0 \) is the number of failures that have occurred so far. We assume that \( g(n, F) \) is a monotonically non-decreasing function of \( n \) and \( F \) since the function is used to represent the worst-case RMR complexity of an RME algorithm. We identify several desirable performance measures applicable to an RME algorithm. To that end, we first define the following concepts for the function \( g(n, F) \).

PM 1. (Constantness) In the absence of failures, the function has a constant value independent of \( n \). Formally, \( g(n, 0) = O(1) \).

PM 2. (Adaptiveness) In order to capture adaptiveness, we define a function \( \Delta(n) \) as:
\[
\Delta(n) = \{ F \mid g(n, F) < g(n, F + 1) \}
\]

With limited number of failures, we identify three different cases.
(a) The function has a non-trivial dependence on \( F \). Formally, \( \Delta(n) = \Omega(1) \).
(b) The function has a strong dependence on \( F \). Formally, \( \Delta(n) = \omega(1) \).
(c) The function has strong and sub-linear dependence on \( F \). Formally, \( \Delta(n) = \omega(1) \) and \( g(n, F) = o(F) \).

PM 3. (Boundedness) With arbitrary number of failures, we identify two different cases:
(a) The function is finite-valued even as \( F \) tends to infinity. Formally, \( \lim_{F \to \infty} g(n, F) \) is finite-valued.
(b) The function is bounded by a sub-logarithmic function of \( n \). Formally, \( \forall F : g(n, F) = O(\frac{\log n}{\log \log n}) \).

Note that PM 2(b) implies PM 2(a), PM 2(c) implies PM 2(b) and PM 3(b) implies PM 3(a).

Consider an RME algorithm \( \mathcal{A} \) and let \( g(n, F) \) denote the best known bound on the worst-case RMR complexity of \( \mathcal{A} \). We call \( \mathcal{A} \) based on the performance measures satisfied by \( g(n, F) \) as follows:

1. Based on adaptiveness
   - non-adaptive if it does not satisfy PM 2(a).
   - semi-adaptive if it satisfies PM 2(a).

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Table 2. Comparison of known solutions to recoverable mutual exclusion problem with respect to the five performance measures.

| Algorithm | Performance Measure | Classification |
|-----------|---------------------|----------------|
|           | PM 1    | PM 2(a) | PM 2(b) | PM 2(c) | PM 3(a) | PM 3(b) |
| Golab and Ramaraju's transformation for recoverability \[15, Section 4.1\] using MCS lock | ✓ | ✓ | ✓ | ✓ | ✓ | unbounded adaptive |
| Golab and Ramaraju's transformation for bounding RMR complexity \[15, Section 4.2\] using MCS lock | ✓ | ✓ | ✓ | ✓ | ✓ | bounded semi-adaptive |
| Golab and Hendler's arbitration tree using k-part MCS lock* \[12\] | ✗ | ✗ | ✗ | ✗ | ✗ | well-bounded non-adaptive |
| Jayanti and Joshi's wait-free recoverable lock \[20\] | ✗ | ✗ | ✗ | ✗ | ✓ | bounded non-adaptive |
| Jayanti and Joshi's arbitration tree using k-part MCS lock \[19\] | ✗ | ✗ | ✗ | ✗ | ✓ | well-bounded non-adaptive |
| Chan and Wotruff's array based recoverable lock† \[8\] | ✓ | ✓ | ✓ | ✓ | ✗ | unbounded adaptive |
| Katzan and Morrison's abortable and recoverable lock \[22\] | ✗ | ✓ | ✓ | ✓ | ✓ | well-bounded non-adaptive |
| Our recoverable lock [this work] | ✓ | ✓ | ✓ | ✓ | ✓ | well-bounded super-adaptive |

* It has been recently shown in \[19\] that the algorithm is prone to deadlocks
† RMR complexity is constant in the amortized case

- **adaptive** if it satisfies PM 2(b) (hence also PM 2(a)).
- **super-adaptive** if it satisfies PM 2(c) (hence also PM 2(b) and PM 2(a)).

(2) Based on boundedness
- **unbounded** if it does not satisfy PM 3(a).
- **bounded** if it satisfies PM 3(a).
- **well-bounded** if it satisfies PM 3(b).

A comparison of the known RME algorithms with respect to the above performance measures PM 1 to PM 3 is shown in table 2. As shown in table 2, all existing RME algorithm are either non-adaptive, semi-adaptive or unbounded adaptive. To our knowledge, there is no bounded-adaptive, let alone well-bounded super-adaptive RME algorithm currently for either memory model. Note that our taxonomy may not be able to classify all possible RME algorithms (or recoverable algorithms in general), but it is sufficient for classifying and comparing all existing RME algorithms.

To quantify the impact of failures on the performance of an RME algorithm, we use the notion of consequence interval of a failure. Roughly speaking, we use it to capture the maximum duration for which the impact of the failure may be felt in the system. It is related to, but different from, the notion of k-failure-concurrent passage defined by Golab and Ramaraju in \[16\]. A more detailed comparison of the two notions is deferred to section 6.2.

**Definition 2.6 (consequence interval).** The consequence interval of a failure in a history \(H\) is defined as the interval in time that starts from the onset of the failure and extends to the point in time when either every super-passage that started before this failure occurred in \(H\) has completed or the last step in \(H\) is performed, whichever happens earlier.

An illustration of the consequence interval of a failure is provided in fig. 1. Intuitively, we consider a failure to be recent with respect to a time \(t\) if \(t\) is contained in the consequence interval of the failure. The following notion captures the “concentration” of failures in the recent past of a request.

**Definition 2.7 (failure-density).** The failure-density of a request is defined as the number of failures whose consequence interval overlaps with the super-passage of the request.
We show that our framework yields an RME algorithm that is adaptive not only to failure-density (our main focus) but also to contention. To show the latter, we use the well-known notion of point contention defined as follows:

Definition 2.8 (point contention). The point contention of a request is defined as the maximum number of super-passages that are simultaneously in-progress at any point during the super-passage associated with the request.

In the remainder of the text, unless stated otherwise, the term “adaptive” is used in the context of failure-density.

2.6 Synchronization primitives

We assume that, in addition to read and write instructions, the system also supports atomic fetch-and-store (FAS) and compare-and-swap (CAS) read-modify-write (RMW) instructions.

A fetch-and-store instruction takes two arguments: address and new; it replaces the contents of a memory location (address) with a given value (new) and returns the old contents of that location.

A compare-and-swap instruction takes three arguments: address, old and new; it compares the contents of a memory location (address) to a given value (old) and, only if they are the same, modifies the contents of that location to a given new value (new). It returns true if the contents of the location were modified and false otherwise.

Both instructions are commonly available in many modern processors such as Intel 64 [18] and AMD64 [1].

3 WEAK RECOVERABILITY

To design a well-bounded super-adaptive RME algorithm, we use a solution to the weaker variant of the RME problem as a building block in which a failure may cause the ME property to be violated albeit only temporarily and in a controlled manner. We refer to this variant as the weakly recoverable mutual exclusion problem.

To formally define how long a violation of the ME property may last, we use the notion of consequence interval of a failure defined earlier.

Definition 3.1 (weakly recoverable mutual exclusion). An algorithm is a weakly recoverable mutual exclusion algorithm if, in addition to starvation freedom, it satisfies the following property: for any history H, if two or more processes are
in their critical sections simultaneously at some point in $H$, then that point overlaps with the consequence interval of some failure.

Roughly speaking, a weakly RME algorithm satisfies the ME property as long as no failure has occurred in the “recent” past. Hereafter, to avoid confusion, we sometimes refer to the traditional recoverable mutual exclusion problem (respectively, algorithm) as defined in subsection 2.4 as strongly recoverable mutual exclusion problem (respectively, algorithm).

The bounded exit, bounded recovery and bounded critical section reentry properties defined earlier in subsection 2.4 are applicable to weakly RME problem as well.

We demonstrate that it is possible to design an optimal weakly recoverable mutual exclusion algorithm using existing hardware instructions whose worst-case RMR complexity is only $O(1)$ under both CC and DSM models. In contrast, as proven in [7], the worst-case RMR complexity of any strongly RME algorithm is $\Omega(\log n/\log \log n)$ under both CC and DSM models. We exploit this gap to design an RME algorithm that is adaptive and bounded. To prove that our algorithm is also well-bounded super-adaptive, we utilize some additional properties of our weakly RME algorithm.

Note that not all failures may cause the ME property to be violated when using a weakly RME algorithm. To that end, we define the notion of sensitive instruction of an algorithm.

Definition 3.2 (sensitive instruction). An instruction $\sigma$ of a weakly RME algorithm is said to be sensitive if there exists a finite history $H$ that satisfies the following conditions: (a) it contains exactly one failure in which a process crashes immediately after executing said instruction $\sigma$ and (b) two or more processes are in CS at the end of $H$; it is said to be non-sensitive otherwise.

Definition 3.3 (unsafe failure). A failure is said to be unsafe with respect to a weakly RME algorithm if it involves a process crashing while (immediately before or after) performing a sensitive instruction with respect to the algorithm; it is said to be safe otherwise.

Note that, by definition, every instruction of a strongly RME algorithm is a non-sensitive instruction. As a result, every failure is safe with respect to a strongly RME algorithm.

The next notion limits the “degree” of violation (of the ME property) by a weakly RME algorithm if and when it occurs.

Definition 3.4 (responsive weakly recoverable mutual exclusion). We say that a weakly recoverable mutual exclusion algorithm is responsive if, for all $k \geq 1$, it satisfies the following property: for any history $H$, if at least $k + 1$ processes are in their critical sections simultaneously at some point in $H$, then that point overlaps with the consequence intervals of at least $\Omega(k)$ (unsafe) failures.

3.1 Composite recoverable locks

The properties defined above are with respect to a single weakly recoverable lock. In order to construct a well-bounded super-adaptive (strongly) recoverable lock with desired performance characteristics, we use multiple weakly recoverable locks. We call a lock as composite if it is employs one or more (weakly or strongly recoverable) locks. Composite locks might have several possible structures. For instance, the Enter segment of one lock could be contained in the Enter or CS segment of another lock or the CS segment of one lock may be contained in the NCS segment of another lock. An example of a composite lock is a lock based on the tournament algorithm [16].

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Note that, when we have multiple locks, the notions defined earlier, namely consequence interval, sensitive instruction and unsafe failure, become relative to the specific lock. For example, a failure will have a different consequence interval with respect to each lock. An instruction may be sensitive with respect to one lock but non-sensitive with respect to another. Thus, in a composite lock, a failure may be unsafe with respect to one or more weakly recoverable locks.

**Definition 3.5 (locality property).** A composite (weakly or strongly) recoverable lock is said to satisfy the *locality property* if, for any instruction $\sigma$, $\sigma$ is sensitive with respect to at most one of its component weakly recoverable locks.

A composite lock whose component locks are all strongly recoverable trivially satisfies the locality property.

## 4 AN OPTIMAL WEAKLY RECOVERABLE LOCK

In this section, we present a weakly recoverable lock whose RMR complexity is $O(1)$ per passage for all three failure scenarios under both CC and DSM models. Our lock is based on the well-known MCS queue-based (non-recoverable) lock [24]. The original lock did not satisfy the bounded exit property. Dvir and Taubenfeld proposed an extension to the original algorithm in [10] to make the Exit segment wait-free. We extend the augmented MCS lock, which satisfies bounded-exit property, to make it weakly recoverable.

### 4.1 Original MCS queue based lock

Processes in the MCS mutual exclusion algorithm use queue nodes to synchronize their executions of CS segments. The algorithm maintains a first-come-first-served (FCFS) queue of outstanding requests using a linked-list of their associated nodes. A node contains two fields: (a) `next`, a reference to its successor node in the queue (if any), and (b) `locked`, a boolean variable used by a process to spin while waiting for its turn to enter its critical section. The queue itself is represented using a shared variable `tail` that contains a reference to the last node in the queue if non-empty and `null` otherwise.

To acquire the lock, a process first initializes its queue node by setting its `next` and `locked` fields to `null` and `true`, respectively. It then appends the node to the queue by performing an FAS instruction on `tail` using the reference to its own node as an argument (to the instruction). Note that the instruction returns the contents of `tail` just before it is modified. If the return value is `null`, then it indicates that the lock is free and the process has successfully acquired the lock. If not, then it indicates that the lock is not free and the return value is the reference to the predecessor of the process’ own node in the queue. In that case, it notifies the owner of the predecessor node of its presence. To that end, it stores the reference to its own node in the `next` field of the predecessor node, thereby creating a forward link between the two nodes. It then starts spinning on the `locked` field of its own node waiting for it to be reset to false by the owner of the predecessor node as part of releasing the lock.

To release the lock, a process first tries to reset the `tail` variable to `null` (if `tail` still contains the reference to this process’ node) using a CAS instruction. If the instruction returns true, then it implies that the queue does not contain any more outstanding requests and the lock is now free. On the other hand, if the instruction returns false, then it implies that the queue contains at least one outstanding request and its own node is guaranteed to have a successor. It then waits until the `next` field of its own node contains a valid reference (a non-null value) indicating that a link has been created between its own node and its successor. Finally, it follows this link and resets the `locked` field in its successor node to false.
4.2 Adding bounded exit property

The original algorithm as described above does not satisfy the bounded-exit property since a process leaving its critical section may have to wait until a link between its own node and its successor has been created.

To achieve the bounded-exit property, the original algorithm is augmented with a mechanism that allows a leaving process to notify the process next in line to acquire the lock that the lock is now free. To that end, a process, on leaving its critical section, attempts to store a special value (e.g., reference to its own node) in the next field of its own node using a CAS instruction. Likewise, a link is also created using a CAS instruction instead of a simple write instruction as in the original algorithm. Both CAS instructions are designed to succeed only if the next field contains `null` value, thereby ensuring that the next field can only be modified once.

Thus, if the CAS instruction performed by a process leaving its critical section returns false, then that process can conclude that the forward link has already been created and it then follows this link and resets the locked field of its successor node. On the other hand, if the CAS instruction performed by a process trying to create the link returns false, then that process can infer that the lock is free and that it now holds the lock.

With this modification, unlike in the original algorithm, a process cannot always reuse its own node for the next request after releasing the lock.

4.3 Adding weak recoverability

A pseudocode of the weakly recoverable lock is given in algorithms 2 and 3. Our pseudocode uses the following shared variables. The first variable, tail, contains the address of the last node in the queue if the queue is non-empty and `null` otherwise. The next three variables, state, mine and pred, are arrays with one entry for each process. The i-th entry of state, denoted by state[i], contains process pi’s current state with respect to the lock (explained later). The i-th entry of mine, denoted by mine[i], contains the address of the queue node associated with process pi’s most recent request. The i-th entry of pred, denoted by pred[i], contains the address of the predecessor node, if any, of process pi after its node has been appended to the queue.

The state of a process with respect to a lock has five possible values, namely Free, Initializing, Trying, InCS and Leaving. At the beginning, the state of a process, say pi, is set to Free. It is changed to Initializing at the end of the Recover segment (line W.71). It is changed to Trying after (1) pi has initialized mine[i] with the address of a new node (line W.23), (2) initialized the two fields of mine[i] (lines W.25 and W.26) and finally (3) initialized pred[i] by setting it equal to mine[i] (line W.27). It is changed to InCS after pi has acquired the lock. It is changed to Leaving when pi starts releasing the lock, and is changed to Free again after pi finishes releasing the lock.

Our algorithm has only one sensitive instruction, namely the one involving the FAS instruction (line W.32). Recall that a process uses this instruction to append its own node to the queue and also obtain the address of its predecessor node. If a process fails immediately after executing this instruction (line W.32) but before it is able to store its return value to the shared memory (line W.33), there is no easy way to recover this address (of the predecessor) based on the current knowledge of the failed process. The queue continues to grow beyond this node, but it would be disconnected from the previous part of the queue, thereby creating one more sub-queue. For an example, please refer to fig. 2. Thus, an unsafe failure occurs if a process fails immediately after executing the instruction at line W.32.

If a process detects that it may have failed while executing the (FAS) instruction, it “relinquishes” its current node, informs its successor (if any) that the lock is now “free” using the wait-free signalling mechanism described earlier, retires the current node and retries acquiring the lock using a new node. This potentially creates multiple queues (or...
Algorithm 2: Pseudocode of process $p_i$ for a weakly recoverable MCS-based lock with wait-free exit.

```plaintext
/* Data structure used by the algorithm */

struct QNode {
  /* location used for spinning while waiting to enter CS */
  locked: boolean variable;
  /* reference to the successor node */
  next: reference to QNode;
};

/* initialize fields of my own node */

function ENTER( )
begin
  if (state[i] = INITIALIZING) then
    if (mine[i] = null) then
      mine[i] ← GetNewNode( );
    end if
  end if

  /* initialize fields of my own node */
  pred[i] ← mine[i];
  state[i] ← TRYING;
end if

if (state[i] = TRYING) then
  if (pred[i] = mine[i]) then
    /* append my own node to the queue */
    QNode result ← FAS( tail, mine[i] );
    pred[i] ← result;
  end if
end if

if (state[i] = TRYING) then
  if (pred[i] ≠ null) then
    /* have a predecessor; create the link */
    CAS( pred[i].next, null, mine[i] );
    if (pred[i].next = mine[i]) then
      /* wait for the predecessor to complete */
      await not(mine[i].locked);  // spin
    end if
  end if
end if

state[i] ← InCS;
end if
```

sub-queues) which may allow multiple processes to execute their critical sections concurrently, thereby violating the ME property. A node is relieved (either after failure or completion of critical section) by executing the cleanup function (lines W.47 to W.59). The function can be invoked from either Recover or 5x1t segment. All other instructions of our algorithm, except for FAS, are non-sensitive. We achieve that by using the following ideas.

First, a process does not use the outcome of the CAS instruction used to modify the next field of a node (line W.38 and line W.51). After performing the CAS instruction on the next field, it reads the contents of the field again and determines its next step based on what it read. Note that, once initialized, the next field can only be modified once. This makes the two steps involving the CAS instruction on the next field as idempotent; the effect of performing the CAS instruction multiple times if interrupted due to failures is the same as performing it once.

Second, portions of Recover and Enter segments are enclosed in if-blocks to be executed conditionally. Intuitively, the guard of an if-block represents the pre-condition that needs to hold before its body can be executed. The outermost if-blocks use guards based on the current state of the process, which is advanced only at the end of the block. The inner if-blocks use guards based on other variables. Except for the if-block containing the FAS instruction (which constitutes a sensitive instruction), all other if-blocks are idempotent and can be executed repeatedly if interrupted due to failures without any adverse impact starting from the evaluation of the guard (lines W.63 to W.66, lines W.67 to W.69, lines W.70).
Algorithm 3: Pseudocode of process $p_i$ for a weakly recoverable MCS-based lock with wait-free exit (continued).

```plaintext
Function CLEANUP()

if (mine[i] != null)
  if (mine[i] == null)
    CAS tail, mine[i], null;
  else
    CAS mine[i].next, null, mine[i];
end if
end if

Function RECOVER()

if (state[i] == LEAVING)
  if (pred[i] == mine[i])
    /* may have failed earlier while performing PAS instruction; abort the attempt */
  end if
  CLEANUP();
end if

Function EXIT()

begin
  // execute cleanup method
end
```

Fig. 2. Processes $p_1 \ldots p_8$ successfully append their nodes to the tail of the queue using an FAS instruction. Processes $p_4$ and $p_7$ failed to store the outcome of the FAS instruction to persistent memory, and are thus unable to set the next field of the nodes of $p_3$ and $p_0$. Process $p_3$ has captured the address of the node of $p_2$ and is about to set the corresponding next field on the node of $p_2$. Effectively, three sub-queues are created due to failures of $p_4$ and $p_7$.

to W.72, lines W.21 to W.29 and lines W.37 to W.42). Note that if the guard of an if-block does not hold, its body is not executed.

Third, similar to the case of the next field, a process does not use the outcome of the CAS instruction used to modify the tail pointer of the queue in the cleanup function (line W.50). After performing the CAS instruction on the tail pointer, irrespective of the outcome of the instruction, it blindly executes the remainder of the steps pertaining to signalling the successor node (lines W.51 to W.54). If the node has no successor, then the steps are redundant, but have no adverse impact even if the node has already been removed from the queue by an earlier CAS instruction.

The functions GetNewNode and RetireLastNode are “hooks” for the memory reclamation algorithm described later.
We refer to the algorithm for a weakly recoverable lock described in this section as WR-LOCK. Note that lines W.21 to W.35, which do not contain any loop, constitute the doorway of WR-LOCK whereas lines W.36 to W.44 constitute its waiting room.

4.4 Correctness proof

We prove that WR-LOCK is a responsive weakly recoverable mutual exclusion algorithm. We first define some concepts and notations used in our proofs. All definitions use the notion of current time.

The WR-LOCK uses a queue node to synchronize among processes and serialize their critical section executions. In the absence of failures, a process allocates a new node at the beginning of a passage and relieves it at the end of that passage. However, in the presence of failures, a node allocated during one passage may be relieved during a different passage. Every node is owned by a (unique) process. Let owner($u$) denote the owner process of the node $u$. A node becomes active once it has been appended to the queue by storing its address in the tail pointer using a FAS instruction (line W.32). It follows from code inspection that:

**Proposition 4.1.** A node is appended to the queue at most once.

Note that active nodes can be ordered based on the sequence in which they were appended to the queue. We refer to the last active node to be appended to the queue as the tail node. Note that

If a node $v$ is appended to the queue immediately after a node $u$, then we say that $v$ is the successor of $u$ and there is an edge from $v$ to $u$. We use $\text{succ}(u)$ to denote the successor of node $u$ and $\text{edge}(v,u)$ to denote the edge from node $v$ to node $u$ provided $v = \text{succ}(u)$. Intuitively, the edge $\text{edge}(v,u)$ captures the wait-for dependency that $v$ has on $u$. In particular, $\text{owner}(v)$ cannot enter its CS segment until $\text{owner}(u)$ has relieved $u$. The set of active nodes along with the set of edges, as defined above, form a chain referred to as global chain.

A node is said to have been relieved if its owner has executed either the CAS instruction at line W.51 successfully (to signal its successor process) or the write instruction at line W.53 (to unlock the successor node).

A node is said to be admissible if it is active but not relieved.

The following proposition follows from code inspection:

**Proposition 4.2.** A process can own at most one admissible node in the global chain. Further, if a process owns an admissible node in the global chain, then it has a super-passage in progress.

Consider two nodes $u$ and $v$ such that $v = \text{succ}(u)$ and let $p = \text{owner}(v)$. The edge $\text{edge}(v,u)$ is said to be admissible if the following conditions hold. First, $u$ is admissible. Second, when $p$ appended $v$ to the queue, the FAS instruction returned the address of $u$. Third, since $p$ appended $u$ to the queue, either $p$ has not failed or has stored the address of $u$ in the persistent memory by executing the write instruction at line W.33. Intuitively, if the edge $\text{edge}(v,u)$ is not admissible, then either $\text{owner}(u)$ has already relieved $u$ or $\text{owner}(v)$ has lost the address of $u$.

We call any non-empty connected set of nodes in the global chain as a fragment. A fragment is said to be admissible if all its nodes as well as all its edges are admissible. An admissible fragment is said to be maximal if it is not strictly contained in another admissible fragment.

We define sub-queue as a maximal admissible fragment. Note that each sub-queue has a front node (no outgoing admissible edge) and a rear node (no incoming admissible edge).

Figure 3 gives an illustration of the concepts defined so far.

The following propositions follow from the above concepts.
that the incoming edge to an admissible non-tail node can only be disrupted by an unsafe failure. Moreover, an unsafe failure can disrupt at most one edge in the global chain.

**Proposition 4.3.** Any two distinct sub-queues are node disjoint.

**Proposition 4.4.** If a process owns a node in some sub-queue, then it has a super-passage in progress. Moreover, if a process is in its CS, then it owns the front node of some sub-queue.

**Proposition 4.5.** Assume that every process fails only a finite number of times during each of its super-passage. If a process owns the front node of some sub-queue, then it eventually relieves the node.

**Proposition 4.6.** If a process owns the front node of some sub-queue and never fails thereafter in its super-passage currently in progress, then the super-passage eventually completes.

Note that every active non-tail node has an incoming edge. Consider an admissible non-tail node $u$ and let $v = \text{succ}(u)$. Note that, just after $v$ is appended to the queue, the edge from $v$ to $u$ is admissible. Thus, if the edge from $v$ to $u$ is not admissible now, then it implies that $\text{owner}(v)$ failed before it was able to store the address of $u$ in the persistent memory. If this happens, then we say that the edge from $v$ to $u$ (whose status changed from admissible to non-admissible) has been disrupted by the unsafe failure.

The following proposition follows from above concepts.

**Proposition 4.7.** The incoming edge to an admissible non-tail node can only be disrupted by an unsafe failure. Moreover, an unsafe failure can disrupt at most one edge in the global chain.

Based on the above propositions, we prove the following results about WR-Lock.

**Lemma 4.8.** Given a history $H$ and a non-negative integer $k$, if at least $k$ processes are in their critical sections simultaneously, then the global chain contains at least $k$ distinct sub-queues.

**Proof.** The lemma follows from propositions 4.3 and 4.4.

**Theorem 4.9.** Given a history $H$, and a non-negative integer $k$, if $k + 1$ processes are in their critical sections simultaneously, then there exists at least $k$ unsafe failures whose consequence interval is still in-progress.

**Proof.** It follows from lemma 4.8 that the global chain contains at least $k + 1$ distinct sub-queues. Clearly, the rear node of all sub-queues, except possibly for one, is a non-tail node. It follows from proposition 4.7 that the incoming edge of every non-tail rear node was disrupted by a unique unsafe failure.

Now, consider an arbitrary sub-queue whose rear node, say $u$, is a non-tail node. Note that the global chain contains at least $k$ such nodes. Let $v = \text{succ}(u)$ and let $f$ be the unsafe failure that disrupted $\text{edge}(v, u)$. Clearly, $u$ is appended to the queue before $v$, and $v$ is appended to the queue before $f$ occurred. Using proposition 4.2, it implies that $\text{owner}(u)$
has a super-passage currently in progress that started before $f$ occurred. In other words, the consequence interval of $f$ is still active.

**Theorem 4.10.** WR-Lock satisfies the SF property.

**Proof.** Assume that every process fails only a finite number of times during each of its super-passage. Assume, on the contrary, that some super-passage, say $\Pi$, belonging to a process, say $p$, never completes. Let $\sigma$ denote the first passage that $p$ starts after recovering from its last failure in $\Pi$. By assumption, $p$ never fails during $\sigma$. Clearly, $p$ eventually advances to line W.35 during $\sigma$ at which point it is guaranteed to own an admissible node, say $u$, in the global chain. By applying proposition 4.5 repeatedly, we can infer that $u$ eventually becomes the front node of its sub-queue. By applying proposition 4.6, we can infer that $\Pi$ eventually completes—a contradiction.

**Theorem 4.11.** WR-Lock satisfies the BCSR property.

**Proof.** Assume that some process, say $p_i$, fails while executing its CS segment implying that $state[i] = \text{InCS}$ at the time of failure. Upon restarting, $p_i$ executes NCS, Recover and Enter segments in that order. As the code inspection shows, since $state[i] = \text{InCS}$, $p_i$ only evaluates a constant number of if-conditions, all of which evaluate to false, and is therefore able to proceed to the CS segment in a bounded number of its own steps.

It follows from theorems 4.9 to 4.11 that

**Theorem 4.12.** WR-Lock is a responsive weakly recoverable mutual exclusion algorithm.

**Theorem 4.13.** WR-Lock satisfies the BR and BE properties.

**Proof.** As the code inspection shows, Recover and Exit segments do not involve any loops. Thus, a process can execute these segments within a bounded number of its own steps. Hence, WR-Lock satisfies the BR and BE properties.

4.5 Complexity analysis

**Theorem 4.14.** The RMR complexity of each of Recover, Enter and Exit segments of WR-Lock is $O(1)$.

**Proof.** As the code inspection shows, Recover and Exit segments do not contain any loop and only contain a constant number of steps. The Enter segment, however has one loop at line W.40 of algorithm 2, but otherwise contains a constant number of steps. This loop involves waiting on a boolean variable until it becomes true and the variable can be written to only once. This incurs only $O(1)$ RMRs in the CC model. In the DSM model, this variable is mapped to a location in local memory module. Hence, the RMR complexity of the Enter segment is also $O(1)$ in both CC and DSM models.

5 A STRONGLY RECOVERABLE WELL-BOUNDED SUPER-ADAPTIVE LOCK

In this section, we describe a framework that uses other types of recoverable locks with certain properties as building blocks to construct a lock that is not only strongly recoverable but also well-bounded super-adaptive under both CC and DSM models. We describe our (well-bounded super-adaptive) lock in two steps. We first describe a basic framework to transform a bounded non-adaptive strongly recoverable lock to a bounded semi-adaptive strongly recoverable lock. We then extend this framework to make the lock super-adaptive while ensuring that it stays strongly recoverable and...
bounded. Finally, instantiating the framework with an appropriate well-bounded non-adaptive lock yields the desirable well-bounded super-adaptive lock.

The basic framework is based on the one used by Golab and Ramaraju in [16, Section 4.2] to construct a strongly recoverable lock that is semi-adaptive. Specifically, in their framework, Golab and Ramaraju use two different types of strongly recoverable locks, referred to as base lock and auxiliary lock, along with two other components to build another strongly recoverable lock, referred to as target lock. The target lock constructed is bounded semi-adaptive based on the base lock that is unbounded adaptive and the auxiliary lock that is non-adaptive. They achieve this by customizing the base lock so that, upon detecting a failure, processes can abort their attempts and reset the (base) lock. In the presence of failures (even a single failure), the RMR complexity of the target lock is dominated by the overhead of aborting the attempt to acquire the base lock and then resetting the base lock, thereby making the lock semi-adaptive.

In the rest of the text, we use the term “target lock” to refer to the (strongly recoverable) lock we want to build.

5.1 A well-bounded semi-adaptive RME algorithm

5.1.1 Building blocks. We use four different components as building blocks.

- **Filter lock**: A responsive weakly recoverable lock that provides mutual exclusion in the absence of failures. We use an instance of the lock proposed in section 4, which has \(O(1)\) RMR complexity for all three failure scenarios.
- **Splitter**: Used to split processes into fast or slow paths. If multiple processes navigate the splitter concurrently (which would happen only if an unsafe failure has occurred with respect to the filter lock), only one of them is allowed to take the fast path and the rest are diverted to the slow path. In other words, the splitter is biased. Intuitively, it can be viewed as a strongly recoverable try lock. It is implemented using an atomic integer and a CAS instruction, which has \(O(1)\) RMR complexity for all three failure scenarios.
- **Arbitrator lock**: A dual-port strongly recoverable lock. Each port corresponds to a side. We refer to the two sides as \(L/e.sc/f.sc/t.sc\) and \(R/i.sc/g.sc/h.sc/t.sc\). At any time, at most one process should be allowed to attempt to acquire the lock from any side. However, any two of the \(n\) processes can compete to acquire the lock. We use the implementation of the dual-port RME algorithm proposed by Golab and Ramaraju in [16, Section 3.1] (a transformation of Yang and Anderson’s mutual exclusion algorithm to add recoverability), which has \(O(1)\) RMR complexity for all three failure scenarios.
- **Core lock**: A (presumably non-adaptive) strongly recoverable lock that assures mutual exclusion among processes taking the slow path. We may use an instance of any of the existing RME algorithms.

Note that our target lock satisfying BCSR, BR and BE properties is contingent upon filter, arbitrator and core locks satisfying BCSR, BR and BE properties.

5.1.2 The execution flow. In order to acquire the target lock, a process proceeds as follows. It first waits to acquire the filter lock. Once granted, it navigates through the splitter trying to enter the fast path. If successful, it then attempts to acquire the arbitrator lock from the \(L\) side. If one or more failures occur that are unsafe with respect to the filter lock, then multiple processes may acquire the filter lock simultaneously. If this results in contention at the splitter, then all but one processes are diverted to the slow path. If a process is forced to take the slow path, it attempts to acquire the core lock. Once granted, it then waits to acquire the arbitrator lock from the \(R\) side. Finally, once the process has successfully acquired the arbitrator lock, it is deemed to have acquired the target lock as well, and is now in the CS of the target lock.
A pictorial representation of the execution flow is depicted in Figure 4. Note that the pictorial representation depicts the two sides of the arbitrator lock as left and bottom, which actually correspond to the LEFT side and the RIGHT side of the arbitrator lock respectively.

In the absence of failures, every process takes the fast path, albeit one at a time. However, some processes do take the fast path even if their super-passage overlaps with the consequence interval of an unsafe failure with respect to the filter lock. Note that at most one process can take the fast path at a time and at most one process can hold the core lock at a time. Any process that takes the fast path will always attempt to acquire the arbitrator lock from the LEFT side. Any process that takes the slow path and acquires the core lock will always attempt to acquire the arbitrator lock from the RIGHT side. Since the core lock is strongly recoverable, at most one process will try to acquire the arbitrator lock from each side at a time.

In order to release the target lock, a process simply releases its component locks in the reverse order in which it acquired them: the arbitrator lock, followed by the core lock (in case the process took the slow path), followed by the splitter and finally the filter lock.

The RMR complexity of the fast path is given by the sum of the RMR complexities of the filter lock, the splitter and the arbitrator lock. On the other hand, the RMR complexity of the slow path is given by the sum of the RMR complexities of the filter lock, the splitter, the core lock and the arbitrator lock.

For ease of exposition, we use the following terminology. Before a process is assigned a particular path, we refer to it as a normal process. It is classified as a fast process if it takes the fast path and a slow process otherwise. A slow process becomes a medium-slow process once it acquires the core lock.

The pseudocode is given in algorithm 4. The pseudocode closely follows the above description in text. A splitter is implemented using an integer (shared) variable, namely owner. The fast path is occupied if and only if owner has a non-zero value, in which case the value refers to the identifier of the process currently occupying the fast path. To take the fast path, a process attempts to store its own identifier in owner using a CAS instruction provided its current value is zero (line F.24). If the attempt fails, the process changes its path type to SLOW (line F.27). Note that a process resets its path type from SLOW to its default value of FAST only after it has executed the Exit segment of the core lock at least once without encountering any failure (line F.42).
Algorithm 4: Pseudocode of process $p_i$ for the framework to design a semi-adaptive lock.

```plaintext
F.1 shared variables
F.2 $\mathcal{F}$: $n$-process weakly recoverable lock;
F.3 $\mathcal{C}$: $n$-process strongly recoverable lock;
F.4 $\mathcal{A}$: $n$-process dual-port strongly recoverable lock;
F.5 $\text{type}$: array $[1..n]$ of boolean variables;
F.6 initialization
F.7 begin
F.8 owner ← 0;
F.9 foreach $j \in [1,2,\ldots,n]$ do
F.10 | $\text{type}[j] \leftarrow \text{FAST}$;
F.11 end foreach
F.12 end definitions
F.13 side($\text{type}$) = $\begin{cases} \text{LEFT} & \text{if } \text{type} = \text{FAST} \\ \text{RIGHT} & \text{otherwise} \end{cases}$
F.14 Function Recover( )
F.15 begin
F.16 /* In order to follow the execution model of a lock described in section 2 (NCS, Recover, Enter, CS, Exit in that order), we execute the Recover segment of each of the recoverable locks ($\mathcal{F}$, $\mathcal{C}$ and $\mathcal{A}$) just prior to executing their respective Enter segments */
F.17 end
F.18

F.19 Function Enter( )
F.20 begin
F.21 $\mathcal{F}$.Recover(); // recover the filter lock
F.22 $\mathcal{F}$.Enter(); // acquire the filter lock
F.23 if (type[i] ≠ SLOW) then // not yet on the slow path
F.24 | CAS(owner, 0, i); // attempt to take the fast path
F.25 end if
F.26 if (owner ≠ i) then // unable to take the fast path
F.27 | type[i] ← SLOW; // committed to take the slow path
F.28 | C.Recover(); // acquire the core lock
F.29 | C.Enter(); // acquire the core lock
F.30 end if
F.31 $\mathcal{A}$.Recover(side(type[i])); // acquire the arbitrator lock
F.32 | $\mathcal{A}$.Enter(side(type[i])); // acquire the arbitrator lock
F.33 end
F.34 Function Exit( )
F.35 begin
F.36 $\mathcal{A}$.Exit(side(type[i])); // release the arbitrator lock
F.37 if (type[i] = SLOW) then // took the slow path
F.38 | $\mathcal{C}$.Exit(); // release the core lock
F.39 else // took the fast path
F.40 | owner ← 0; // the fast path is now empty
F.41 end if
F.42 | type[i] ← FAST; // reset the path type to default
F.43 | $\mathcal{F}$.Exit(); // release the filter lock
F.44 end
```

In Golab and Ramaraju's framework, even if a process takes the fast path, it may still incur $\Omega(n)$ RMR complexity in the presence of even a single failure because of the overhead of aborting an attempt and then resetting the base lock, which is an expensive operation. In our framework, on the other hand, a process taking the fast path incurs only $O(1)$ RMR complexity even with arbitrary number of failures because the RMR complexity of acquiring the filter lock, followed by navigating the splitter to take the fast path and finally acquiring the arbitrator lock is only $O(1)$ irrespective of the number of failures.

5.1.3 Correctness proof and complexity analysis. We refer to the algorithm described in the previous section as SA-Lock. The doorway of SA-Lock is given by the doorway of its filter lock. When convenient, we use $\mathcal{F}$ and $\mathcal{C}$ to refer to the filter and core locks, respectively, of SA-Lock.

**Theorem 5.1.** SA-Lock satisfies the ME property.

**Proof.** A process enters the CS segment of SA-Lock after acquiring the arbitrator lock from one of the sides. The arbitrator lock satisfies the ME property as long as no more than one process attempts to acquire it from either side Left or Right at any time. The splitter ensures that, at any time, at most one process attempts to acquire the arbitrator lock from the Left side. The core lock ensures that, at any time, at most one process attempts to acquire the arbitrator lock from the Right side. Therefore, SA-Lock satisfies the ME property. □
Theorem 5.2. SA-Lock satisfies the SF property.

Proof. Assume that every process fails only a finite number of times during each of its super-passage.
All three locks used in the framework, namely filter, core and arbitrator, individually satisfy SF and BCSR properties.
Also, navigating a splitter involves executing a constant number of instructions.
Consider an infinite fair history $H$, a process $p$ that is live in $H$ and a super-passage $\Pi$ of $p$ in $H$. Clearly, there exists a time after which $p$ does not fail any more in $\Pi$. Let $t$ denote the earliest such time. Consider the first passage that $p$ starts after time $t$.
Note that either the SF or BCSR property of the filter lock guarantees that $p$ eventually leaves the Enter segment of the filter lock and enters its CS segment. Process $p$ then completes navigating the splitter within a bounded number of its own steps. Note that, if it was able to enter the fast (respectively, slow) path during an earlier passage of $\Pi$, then it is guaranteed to take the fast (respectively, slow) path again in this passage. As in the case of filter lock, we can argue that $p$ is guaranteed to enter the CS segment of the core lock if it takes the slow path during this passage. Likewise, we can argue that $p$ is guaranteed to enter the CS segment of the target lock. □

Theorem 5.3. SA-Lock satisfies the BCSR property.

Proof. If some process $p_i$ is in the CS segment of SA-Lock, then it currently holds the filter lock and it either (a) acquired the arbitrator lock from the Left side by taking the fast path or (b) acquired the core lock first and then acquired the arbitrator lock from the Right side by taking the slow path.
If $p_i$ fails in the CS segment of SA-Lock, it determines the path it took by checking the type[$i$] variable and then retraces the same steps it had executed earlier. Since the filter lock, the core lock as well as the arbitrator lock satisfy the BCSR property, and the fact that the splitter is wait-free, $p_i$ is guaranteed to be able to acquire the requisite locks and reenter the CS segment of SA-Lock within a bounded number of its own steps. Hence, SA-Lock satisfies the BCSR property. □

Theorem 5.4. SA-Lock satisfies the BE and BR properties.

Proof. The Recover segment of SA-Lock is empty and hence it trivially satisfies the BR property.
As part of the Exit segment of SA-Lock, a process executes the Exit segment of the arbitrator lock, optionally followed by the Exit segment of the core lock, followed by the Exit segment of the filter lock. Since each of three locks individually satisfy the BE property, and the splitter is wait-free, it follows that SA-Lock also satisfies the BE property. □

It follows from theorems 5.1 to 5.4 that

Theorem 5.5. SA-Lock is a strongly recoverable lock.

Theorem 5.6 (SA-Lock is bounded semi-adaptive). The RMR complexity of any passage in a super-passage of SA-Lock is $O(1)$ if the failure-density of the super-passage is zero and $O(R(n))$ otherwise, where $R(n)$ denotes the worst-case RMR complexity of the core lock for $n$ processes.

Proof. In the absence of failures, only one process can successfully acquire the filter lock (definition 3.1). This process navigates the splitter in $O(1)$ steps, takes the fast path and acquires the arbitrator lock from the Left side
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The RMR complexity of the arbitrator lock is $O(1)$. Thus, in this case, the RMR complexity of the target lock is given by $O(1)$.

In the presence of failures, all $n$ processes may be able to successfully acquire the filter lock and proceed to the splitter. Only one of these processes is allowed to take the fast path, which then attempts to acquire the arbitrator lock from the left side. The remaining $(n - 1)$ processes are diverted to the slow path and have to acquire the core lock and then acquire the arbitrator lock from the right side. Thus, in this case, the RMR complexity of the target lock is given by $O(R(n))$.

**Theorem 5.7 (A well-bounded semi-adaptive lock).** Assume that we use Jayanti, Jayanti and Joshi’s or Katzan and Morrison’s RME algorithm [19, 22] to implement the core lock. Then, the RMR complexity of any passage in a superpassage of SA-Lock is $O(1)$ if the failure-density of the superpassage is zero and $O(\log n/\log \log n)$ otherwise.

In the rest of this subsection, we prove an important lemma that is crucial to establish that the lock described in the next subsection is super-adaptive. Recall that the notions of superpassage and unsafe failures are relative to a specific lock.

Intuitively, the set of processes that attempt to acquire the core lock is strictly smaller than the set of processes that attempt to acquire the filter lock. Further, the size of the former set depends on the number of unsafe failures that have occurred with respect to the filter lock. To capture this formally, we first define some notations. Let $P\ell(t, t)$ denote the set of processes that have a superpassage in progress with respect to lock $\ell$ at time $t$. Also, let $UF(t, t)$ denote the set of all failures that are unsafe with respect to the lock $\ell$ and whose consequence interval extends at least until time $t$.

Further, if a process $p$ has a superpassage in progress with respect to the target lock at time $t$, then we use $\Pi(p, t)$ to denote the superpassage of $p$ with respect to the target lock at time $t$.

Recall that $F$ and $C$ refer to the filter and core locks, respectively, of SA-Lock.

**Lemma 5.8.** Consider a time $t_C$ such that $|P(C, t_C)| > 0$. Then there exists time $t_F$ with $t_F \leq t_C$ such that the following properties hold.

(a) $P(C, t_C) \subseteq P(F, t_F)$.
(b) $\forall p \in P(C, t_C), \Pi(p, t_F) = \Pi(p, t_C)$, and
(c) $|UF(F, t_F)| \geq |P(C, t_C)|$.

**Proof.** None of the processes in the set $P(C, t_C)$ was able to take the fast path while navigating the splitter. Let $q$ be the last process in $P(C, t_C)$ to read the contents of the variable $owner$ and $t$ denote the time when it performed the read step. Clearly, $t \leq t_C$. Furthermore, let $r$ denote the process whose identifier was stored in $owner$ when $q$ read its contents. We set $t_F$ to $t$. We now prove each property one-by-one.

(i) Due to the arrangement of the locks, each process in the set $P(C, t_C)$ holds the lock $F$ at time $t_F$. Moreover, process $r$ also holds the lock $F$ at time $t_F$. In other words, $P(C, t_C) \subseteq P(F, t_F), r \in P(F, t_F)$, and $r \notin P(C, t_C)$.

Thus the property (a) holds.

(ii) Consider an arbitrary process $s \in P(C, t_C)$. Assume, by the way of contradiction, that $\Pi(s, t_F) \neq \Pi(s, t_C)$. This means that process $s$ started a new superpassage after time $t_F$. Since $s \in P(C, t_C)$, process $s$ read the contents of the variable $owner$ some time after $t_F$ but before $t_C$. This contradicts our choice of $t_F$. In other words, $\Pi(s, t_F) = \Pi(s, t_C)$. Since $s$ was chosen arbitrarily, it follows that for each $p \in P(C, t_C)$, $\Pi(r, t_F) = \Pi(p, t_C)$.

Thus the property (b) holds.
5.2 A well-bounded super-adaptive RME algorithm

5.2.1 The main idea. We use the gap between the worst-case RMR complexity of implementing a weakly recoverable lock and that of implementing a strongly recoverable lock to achieve our goal.

The main idea is to recursively transform the core lock using instances of our semi-adaptive lock. We transform the core lock repeatedly up to a height $m$ that is equal to the worst-case RMR complexity of another strongly recoverable lock under arbitrary number of failures. The strongly recoverable lock now becomes the base case of the recursion. For ease of exposition, we refer to the core lock in the base case as the base lock.

Let $\text{SA-Lock}$ be a bounded (presumably non-adaptive but does not have to be) strongly recoverable lock, whose worst-case RMR complexity is $O(R(n))$ for $n$ processes. Let $\text{BA-Lock}$ denote an instance of the semi-adaptive lock described in subsection 5.1. And, finally, let $\text{BA-Lock}$ denote the bounded super-adaptive lock that we wish to construct (NA-LOCK is the base lock and BA-LOCK is the target lock). The idea is to create $m = R(n)$ levels of $\text{SA-Lock}$ such that the core lock component of the $\text{SA-Lock}$ at each level is built using another instance of $\text{SA-Lock}$ for up to $m - 1$ levels and using an instance of $\text{NA-Lock}$ at the base level (level $m$). Let $\text{SA-Lock}[i]$ denote the instance of $\text{SA-Lock}$ at level $i$. Formally,

\[
\text{BA-Lock} = \text{SA-Lock}[1] \\
\text{SA-Lock}[i, \text{core}] = \text{SA-Lock}[i + 1] \quad \forall i \in \{1, 2, \ldots, m - 1\} \\
\text{SA-Lock}[m, \text{core}] = \text{NA-Lock}
\]

A pictorial representation of the execution flow of the recursive framework is depicted in Figure 5.

In order to acquire the target lock, a process starts at the first level as a normal process and waits to acquire the filter lock at level 1. It stays on track to become a fast process until an unsafe failure occurs with respect to the filter lock at the first level as a result of which multiple processes may be granted the (filter) lock simultaneously. All of these processes then compete to enter the fast path by navigating through the splitter. The splitter allows only one process to take the fast path at a time, and the rest are diverted to take the slow path. Note that a slow process is created at the first level only if an unsafe failure occurs with respect to the filter lock at the first level. All slow processes at the first level then move to the second level as normal processes. If no further failure occurs, then no slow process is created at the second level and all processes leave this level one-by-one as fast processes with respect to this level. Thus, only $O(1)$ RMR complexity is added to the passages of all the affected processes until the impact of the first failure has subsided. However, if one or more slow processes are created at the second level, then we can infer that a new unsafe failure must have occurred with respect to the filter lock at the second level. All these slow processes at the second level then move to the third level as normal processes, and so on and so forth. At each level, a slow process, upon either acquiring the base lock or returning from the adjacent higher level (whichever case applies), becomes a medium-slow process. Irrespective of whether a process is classified as fast or medium-slow, it next waits to acquire the level-specific processor.
arbitrator lock. Once granted, it either returns to the adjacent lower level or, if at the initial level, is deemed to have successfully acquired the target lock.
Note that in our algorithm, at least $k$ unsafe failures are required at any level to force $k$ processes to be “escalated” to the next level. Each level except for the last one would add only $O(1)$ RMR complexity to the passages of these processes, thus making the target lock adaptive under limited failures. There is no further “escalation” of slow processes at the base level and a bounded (possibly non-adaptive) strongly recoverable lock is used to manage all slow processes at that point, thus bounding its RMR complexity under arbitrary number of failures as well.

As before, in order to release the target lock, a process releases its components locks in the reverse order in which it acquired them.

To prove that our target lock is well-bounded super-adaptive, we utilize two properties of our framework, namely, our weakly recoverable lock is responsive, and our target lock, which is a composite lock, satisfies the locality property.

5.2.2 Correctness proof. Let $F_i$ and $C_i$ denote the instances of the filter and core locks, respectively, at level $i$ for $i = 1, 2, \ldots, m$.

**Theorem 5.9.** For each level $i$ with $1 \leq i \leq m$, SA-Lock$[i]$ is a strongly recoverable lock.

**Proof.** The proof is by backward induction on the level number of SA-Lock starting from level $m$.

- **Base case (SA-Lock$[m]$ is a strongly recoverable lock).** Note that SA-Lock$[m] = NA$-Lock. By construction, NA-Lock is a bounded strongly recoverable lock. Thus, SA-Lock$[m]$ is a strongly recoverable lock.

- **Induction hypothesis (SA-Lock$[i + 1]$ is a strongly recoverable lock for some $i$ with $1 \leq i < m$).** We prove that SA-Lock$[i]$ is also a strongly recoverable lock. Note that SA-Lock$[i]$ is an instance of our semi-adaptive lock described in section 5.1 with SA-Lock$[i + 1]$ as its core lock. Since SA-Lock$[i + 1]$ is a strongly recoverable lock, it follows from theorem 5.5 that SA-Lock$[i]$ is also a strongly recoverable lock.

Thus, by induction, we can conclude that SA-Lock$[i]$ is a strongly recoverable lock for each level $i = 1, 2, \ldots, m$. □

By construction, BA-Lock = SA-Lock$[1]$. Therefore,

**Theorem 5.10.** BA-Lock is a strongly recoverable lock.

Using induction similar to the one used in theorem 5.9, we can show that

**Theorem 5.11.** BA-Lock satisfies the BR and BE properties.

5.2.3 Complexity analysis. To analyze the RMR complexity of a passage, we first prove certain results.

**Theorem 5.12.** BA-Lock satisfies the locality property.

**Proof.** BA-Lock uses three types of locks, namely filter, arbitrator and base; only filter lock is weakly recoverable. There is one instance of the filter lock at each level. By construction, the Enter segments of any two instances of the filter lock do not overlap. The only sensitive instruction of the filter lock is the FAS instruction in its Enter segment. Therefore, BA-Lock satisfies the locality property. □

By the construction of our recursive framework, we have

**Proposition 5.13.** For each level $i$ and time $t$ with $1 \leq i \leq m$, $\mathbb{P}(C_i, t) = \mathbb{P}(SA$-Lock$[i + 1], t) = \mathbb{P}(F_i, t)$.

Note that the set of processes that attempt to acquire the filter lock at any level becomes progressively smaller as the level number increases. Furthermore, the number of processes that are escalated to the next level depends on the number of unsafe failures experienced by the filter lock at the current level. This is captured by the next lemma.
Lemma 5.14. Consider a process \( p \), time \( t \) and level \( x \), where \( 1 \leq x \leq m \), such that process \( p \in \mathcal{P}(\mathcal{F}_x, t) \). Then there exist \( x \) times \( t_1, t_2, \ldots, t_{x-1}, t_x \) with \( t_1 \leq t_2 \leq \cdots \leq t_{x-1} \leq t_x = t \) such that the following properties hold. For each \( i \) with \( 1 \leq i < x \), we have

\[
\begin{align*}
(a) & \quad \Pi(p, t_i) = \Pi(p, t), \\
(b) & \quad \mathcal{P}(\mathcal{F}_i, t_i) \supseteq \mathcal{P}(\mathcal{F}_{i+1}, t_{i+1}), \text{ and} \\
(c) & \quad |\mathcal{U}(\mathcal{F}_i, t_i)| \geq |\mathcal{P}(\mathcal{F}_{i+1}, t_{i+1})|.
\end{align*}
\]

Proof. The proof is by backward induction on \( x - 1 \). In order to prove our results, we use the following auxiliary properties, which are part of the induction statement. For each \( i \) with \( 1 \leq i < x \), we have,

\[
\begin{align*}
(d) & \quad |\mathcal{P}(\mathcal{F}_i, t_i)| > 0, \text{ and} \\
(e) & \quad p \in \mathcal{P}(\mathcal{F}_i, t_i).
\end{align*}
\]

We are now ready to prove the result.

- **Base case** (properties (a)-(e) hold for \( i = x - 1 \)). By definition, \( t_x = t \). By assumption, \( p \in \mathcal{P}(\mathcal{F}_x, t_x) \). By applying proposition 5.13, we obtain that \( p \in \mathcal{P}(C_{x-1}, t_x) \) thereby implying that \( |\mathcal{P}(C_{x-1}, t_x)| > 0 \). We can now apply lemma 5.8 once to infer that \( t_{x-1} < t_x \), and the analogous properties hold.

- **Induction hypothesis (assumption that the properties (a)-(e) hold for some \( i \) with \( 1 < i < x \)).** We now prove that properties (a)-(e) also hold for \( i - 1 \). Note that, by induction hypothesis, \( |\mathcal{P}(\mathcal{F}_i, t_i)| > 0 \). Thus, we can now apply lemma 5.8 once to infer that \( t_{i-1} < t_i \), such that the following properties hold.

The next corollary quantifies the number of processes that must be present at each of the lower levels for some process to be escalated to a certain level.

Corollary 5.15. Consider a process \( p \), time \( t \) and level \( x \), where \( 1 \leq x \leq m \), such that process \( p \in \mathcal{P}(\mathcal{F}_x, t) \). Let times \( t_1, t_2, \ldots, t_{x-1}, t_x \) be as given by lemma 5.14. Then, for each \( i \) with \( 1 \leq i < x \),

\[
|\mathcal{P}(\mathcal{F}_i, t_i)| \geq x - i + 1.
\]

The next corollary quantifies the number of unsafe failures that must occur with respect to the filter lock at each of the lower levels for some process to be escalated to a certain level.

Corollary 5.16. Consider a process \( p \), time \( t \) and level \( x \), where \( 1 \leq x \leq m \), such that process \( p \in \mathcal{P}(\mathcal{F}_x, t) \). Let times \( t_1, t_2, \ldots, t_{x-1}, t_x \) be as given by lemma 5.14. Then, for each \( i \) with \( 1 \leq i < x \),

\[
|\mathcal{U}(\mathcal{F}_i, t_i)| \geq x - i.
\]
For the rest of this section, unless otherwise stated, assume that super-passage of a process and consequence interval of a failure are defined relative to the target lock.

**Theorem 5.17.** Suppose a process $p$ advances to level $x$ at some time $t$ during its super-passage, where $1 \leq x \leq m$. Then, there exist at least $x(x-1)/2$ failures that occurred at or before time $t$ whose consequence interval overlaps with the super-passage of the process $p$.

**Proof.** Let $t_1, t_2, \ldots, t_x$ be the times as given by lemma 5.14. Since BA-Lock satisfies the locality property, the set of failures that are unsafe with respect to one instance of its filter lock is disjoint from the set of failures that are unsafe with respect to another instance of its filter lock. Formally,

$$\forall i, j : 1 \leq i, j \leq x \text{ and } i \neq j : UF(\mathcal{F}_i, t_i) \cap UF(\mathcal{F}_j, t_j) = \emptyset$$

(pairwise disjoint property)

Let $\Pi$ denote the super-passage of $p$ at time $t$. From the property (a) of lemma 5.14, $\Pi = \Pi(p, t_1) = \Pi(p, t_2) = \ldots = \Pi(p, t_x)$. In other words, $p$ is executing the same super-passage during the period $[t_1, t_x]$.

Let $\Phi(t)$ denote the set of all failures that occurred at or before time $t$ and whose consequence interval overlaps with the super-passage $\Pi$. Note that the consequence interval of any failure with respect to the target lock contains the consequence interval of that failure with respect to any instance of its filter lock. This is because all pending requests for that instance of the filter lock are also pending requests for the target lock. Thus, $\forall i : 1 \leq i < x : UF(\mathcal{F}_i, t_i) \subseteq \Phi(t)$.

This in turn implies that

$$\bigcup_{i=1}^{x-1} UF(\mathcal{F}_i, t_i) \subseteq \Phi(t)$$

(containment property)

We have

$$| \Phi(t) | \geq \left| \bigcup_{i=1}^{x-1} UF(\mathcal{F}_i, t_i) \right|$$

(using containment property)

$$= \sum_{i=1}^{x-1} | UF(\mathcal{F}_i, t_i) |$$

(using pairwise disjoint property)

$$= \sum_{i=1}^{x-1} (x - i)$$

(using corollary 5.16)

$$= (x - 1) + \cdots + 2 + 1$$

(expanding the sum)

$$= \frac{x(x-1)}{2}$$

(algebra)

This establishes the result. \qeda

The following results then follow from the above two theorems.

**Theorem 5.18 (BA-Lock is bounded super-adaptive).** The RMR complexity of any passage in a super-passage of BA-Lock is given by $O(\min\{\sqrt{k+1}, R(n)\})$, where $k$ denotes the failure-density of the super-passage and $R(n)$ denotes the RMR complexity of the base NA-Lock for $n$ processes.

**Corollary 5.19 (A well-bounded super-adaptive lock).** Assume that we use Jayanti, Jayanti and Joshi’s [19] or Katzan and Morrison’s RME algorithm [22] to implement the NA-Lock. Then the RMR complexity of any passage in a Manuscript submitted to ACM
super-passage of BA-Lock is given by $O(\min\{\sqrt{k+1} \log n/\log \log n\})$, where $k$ denotes the failure-density of the super-passage.

We now show that BA-Lock is adaptive to contention as well.

**Theorem 5.20.** Suppose a process $p$ advances to level $x$ at some time $t$ during its super-passage, where $1 \leq x \leq m$. Then, there exist at least $x-1$ super-passage and therefore it is the only passage of its super-passage.

**Proof.** Let $t_1$ denote the time as postulated in the statement of lemma 5.14. Clearly, we can infer that $\Pi(p, t_1) = \Pi(p, t), p \in P (\mathcal{F}(t_1, t))$ and $|P (\mathcal{F}(t_1, t)) \setminus \{p\}| \geq x-1$.

This implies that BA-Lock is adaptive to both failures and contention as stated in the next theorem.

**Theorem 5.21 (Dual Adaptivity).** The RMR complexity of any passage in a super-passage of BA-Lock is given by $O(\min\{\varepsilon, \sqrt{k+1}, R(n)\})$, where $\varepsilon$ denote the point-contention of the super-passage, $k$ denotes the failure-density of the super-passage and $R(n)$ denotes the RMR complexity of the NA-Lock for $n$ processes.

## 6 Fairness

An important desirable property satisfied by many ME algorithms is fairness. Intuitively, fairness ensures that no process is able to monopolize shared resources. To define fairness, the Enter segment is partitioned into two segments—doorway followed by waiting room. A doorway consists of a bounded number of steps that a process executes in the beginning of its Enter segment, whereas waiting room is the rest of the Enter segment.

In this work, we use a novel definition for fairness referred to as CI-FCFS. To that end, we first define the notion of exclusive passage as follows. A failure-free passage is said to be exclusive if its associated super-passage is failure-free (and therefore it is the only passage of its super-passage).

**CI-FCFS** A history $H$ is said to satisfy CI-FCFS if it satisfies the following property. Consider a pair of passages $r$ and $s$ in $H$ belonging to processes $p$ and $q$, respectively, such that (a) both $r$ and $s$ are exclusive passages, (b) $p$ completes its doorway in $r$ before $q$ begins its doorway in $s$, and (c) $r$ does not overlap with the consequence interval of any failure. If $q$ has started the CS segment of $s$, then $p$ has started the Exit segment of $r$.

An RME algorithm is said to satisfy CI-FCFS if every history generated by the algorithm satisfies CI-FCFS. Note that, in the absence of failures, CI-FCFS reduces to traditional FCFS (first-come-first-served) property.

We first argue that both our weakly RME lock, namely WR-Lock, and our strongly RME lock, namely SA-Lock, satisfy CI-FCFS. We then compare our notion of fairness with the one used by Golab and Ramaraju in [16].

Note that BA-Lock is a special case of SA-Lock and thus would also satisfy CI-FCFS. Also, note that we do not require the core lock of the framework to be fair.

### 6.1 Fairness of our RME Algorithms

The doorway of WR-Lock consists of lines W.21 to W.35.

**Theorem 6.1.** WR-Lock satisfies the CI-FCFS property.

**Proof.** Consider a history $H$, and let $r_i$ and $r_j$ be passages of processes $p_i$ and $p_j$ respectively such that: (a) $p_i$ completes its doorway in $r_i$ before $p_j$ starts its doorway in $r_j$, (b) both $r_i$ and $r_j$ are exclusive passages, and (c) $r_i$ does not overlap with the consequence interval of any failure.
Assume, on the contrary, that there exists a time instant in $H$ such that, at time $t$, $p_j$ is in the CS segment of $r_j$ but $p_j$ has not started the $\text{Exit}$ segment of $r_i$. Note that, by time $t$, both $p_i$ and $p_j$ have completed the doorways for their respective passages. Let $t_i$ and $t_j$ denote the time instants when $p_i$ and $p_j$, respectively, executed their FAS instructions. Further, let $u_i$ and $u_j$ denote the admissible nodes owned by $p_i$ and $p_j$, respectively, at time $t$. Clearly, $t_i < t_j < t$. We first prove the following claim.

**Claim 6.1.** As long as $u_i$ is admissible, both $u_i$ and $u_j$ belong to a single sub-queue.

The proof of the claim is by contradiction. Assume not. This implies that there exists a process $p_k$ such that $p_k$ (a) executed an FAS instruction at time $t_k$ with $t_i < t_k < t_j$, but (b) experienced an unsafe failure $f$ at time $t_f$ with $t_k < t_f < t$. Since $t_i < t_k$, $t_k < t_f$ and $t_f < t$, it follows that $t_i < t_f < t$. Clearly, $r_i$ contains both $t_i$ and $t$. This implies that $r_j$ contains $t_f$ and thus overlaps with the consequence interval of $f$. This is a contradiction. Thus the claim holds.

It follows from the claim that, until $u_j$ stays admissible, $u_j$ cannot become the front node of its sub-queue. In other words, $p_j$ cannot enter the CS segment of $r_j$ until $p_i$ has started executing the $\text{Exit}$ segment of $r_i$. $\square$

We now prove that the target lock of our framework satisfies the CI-FCFS property. To that end, we assume that the filter lock satisfies the CI-FCFS property.

**Theorem 6.2.** $\text{SA-Lock}$ satisfies the CI-FCFS property.

**Proof.** Consider a history $H$, and let $r_i$ and $r_j$ be passages of processes $p_i$ and $p_j$ (with respect to the target lock) such that: (a) $p_i$ completes its doorway in $r_i$ before $p_j$ starts its doorway in $r_j$, (b) both $r_i$ and $r_j$ are exclusive passages, and (c) $r_j$ does not overlap with the consequence interval of any failure. Assume that $p_j$ in the CS segment of $r_j$. Let $r_i(F) \subseteq r_i$ and $r_j(F) \subseteq r_j$ denote the passages of $p_i$ and $p_j$, respectively, with respect to the filter lock. Due to the arrangements of the locks, we can infer the following. First, if the three conditions of the CI-FCFS property hold for $r_i$ and $r_j$, then they also hold for $r_i(F)$ and $r_j(F)$. Second, if $p_j$ is the CS segment of $r_j$, then it is also in the CS segment of $r_i(F)$. Third, if $p_i$ has started the $\text{Exit}$ segment of $r_i(F)$, then it has also started the $\text{Exit}$ segment of $r_i$.

Since BA-Lock is a special case of SA-Lock, we have:

**Corollary 6.3.** $\text{BA-Lock}$ satisfies the CI-FCFS property.

### 6.2 Comparison with k-FCFS

Golab and Ramaraju define the concept of a $k$-failure-concurrent passage, where $k \geq 0$, to capture how a failure may impact the RMR complexity of a passage. The concept is recursively defined. Given a history, a passage of a process is said to be 0-failure-concurrent if it either ends with or begins after a crash of the process. It is said to be $k$-failure-concurrent if it is either $(k-1)$-failure-concurrent or its super passage overlaps with another super passage containing a $(k-1)$-failure-concurrent passage. Intuitively, the parameter $k$ measures the "distance" of a passage from a 0-failure-concurrent passage in a given history. (Note that a passage is exclusive if and only if it is not 0-failure-concurrent.)

We, on the other hand, use the concept of consequence interval of a failure in this work. Given a history, a passage is said to be CI-concurrent if its super-passage overlaps with the consequence interval of one or more failures.

A natural question is to ask how the concept of $k$-failure-concurrent is related to CI-concurrent. We show that CI-concurrent is "stronger" than 2-failure-concurrent and "incomparable" with 1-failure-concurrent.
Fig. 6. Passages $r_1$ and $r_2$ are the only 0-failure-concurrent passages in the history. Passage $r_3$ overlaps $r_1$ and thus is 1-failure-concurrent, but is not CI-concurrent.

**Theorem 6.4.** Given a passage $r$ in a finite history $H$, if $r$ is CI-concurrent, then it is also 2-failure-concurrent.

**Proof.** For convenience, given a passage $r$, we use $\Pi(r)$ to denote the super-passage associated with $r$.

Consider a passage $r_i$ of process $p_i$ that is CI-concurrent. By definition, $\Pi(r_i)$ overlaps with the consequence interval of a failure, say $f$. Let $f$ involve the failure of process $p_j$ while executing the passage $r_j$. We use $\mathcal{P}(f)$ to denote the set of processes that have a super-passage in progress at the time when $f$ occurred. Note that $\mathcal{P}(f) \neq \emptyset$ because $p_j \in \mathcal{P}(f)$. Let $p_k \in \mathcal{P}(f)$ denote the process whose super-passage, which was in progress when $f$ occurred, extends for the longest time in $H$. Finally, let $r_k$ denote the most recent passage of $p_k$ that started before $f$ occurred.

Note that $\Pi(r_k)$ overlaps with $\Pi(r_j)$. This in turn implies that $r_k$ is (at most) 1-failure-concurrent because $r_j$ is 0-failure-concurrent. Also, note that $\Pi(r_k)$ contain the consequence interval of $f$ and hence overlaps with $\Pi(r_i)$. This implies that $r_i$ is (at most) 2-failure-concurrent.  

We now provide examples to show that 1-failure-concurrent and CI-concurrent are incomparable properties, i.e., neither implies the other.

**Theorem 6.5.** There exists a history $H$ and a passage $r$ in $H$ such that $r$ is 1-failure-concurrent but not CI-concurrent.

**Proof.** Consider the history shown in fig. 6. The passage $r_3$ in the history is 1-failure-concurrent but not CI-concurrent.

**Theorem 6.6.** There exists a history $H$ and a passage $r$ in $H$ such that $r$ is CI-concurrent but not 1-failure-concurrent.

**Proof.** Consider the history shown in fig. 7. The passage $r_4$ in the history is CI-concurrent but not 1-failure-concurrent.

Finally, we show that CI-concurrent is a strictly stronger property than 2-failure-concurrent, i.e., the latter does not imply the former.

**Theorem 6.7.** There exists a history $H$ and a passage $r$ in $H$ such that $r$ is 2-failure-concurrent but not CI-concurrent.

**Proof.** Consider the history shown in fig. 8. The passage $r_5$ in the history is 2-failure-concurrent but not CI-concurrent.
Golab and Ramaraju use the notion of $k$-failure concurrency to define a notion of fairness especially suited to RME algorithms, referred to as $k$-FCFS. Intuitively, $k$-FCFS guarantees FCFS among two passages provided none of them is $k$-failure-concurrent. The results above also establish the following relationship among different fairness properties:

(a) CI-FCFS implies 2-FCFS, and (b) CI-FCFS and 1-FCFS are incomparable.

Incidentally, our framework yields an RME algorithm that not only satisfies the CI-FCFS property but also satisfies the 1-FCFS property. We have,

**Theorem 6.8.** **WR-Lock satisfies the 1-FCFS property.**

**Proof.** The proof is analogous to the proof of theorem 6.1 with the following modification. Let $r_k$ denote the passage of $p_k$ that ends with the failure $f$. Clearly, $r_k$ is 0-failure-concurrent passage and overlaps with $r_i$. This implies that $r_i$ is a 1-failure-concurrent passage—a contradiction. Thus the claim holds in this case as well. □

**Theorem 6.9.** **SA-Lock satisfies the 1-FCFS property.**

**Proof.** The proof is identical to that of theorem 6.2. □

Thus it follows that:

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A CONSTANT-RMR BROADCAST OBJECT

An important component of our memory reclamation algorithm is a recoverable broadcast object, hereafter denoted by \( \text{Broadcast} \), that allows a designated process to notify and "wake up" one or more processes waiting for it to reach a certain point during its execution.

The \( \text{Broadcast} \) object is similar to the \( \text{Signal} \) object used by Jayanti, Jayanti and Joshi in [19] to design an RME algorithm with sub-logarithmic RMR complexity. It is also similar to the \( \text{Barrier} \) object used by Golab and Hendler in [13] to design an RME algorithm for system-wide failures with \( O(1) \) RMR complexity.

The \( \text{Signal} \) object in [19] can only be used once and different processes must wait on the object sequentially. However, a \( \text{Broadcast} \) object can be used repeatedly and multiple processes can wait on the object concurrently.

The \( \text{Barrier} \) object in [13] assumes that all processes fail together and may lead to a deadlock if processes fail independently. In that sense, the definition of \( \text{Broadcast} \) object and its implementation can be viewed as a generalization of \( \text{Barrier} \) object for the independent failure model.

7.1 Definition

Our broadcast object, in essence, is a recoverable MRSW (Multi-Reader Single-Writer) counter object that stores a non-negative value and supports three operations, namely Set, Wait and Read, with the following behavior.

1. \( \text{Set}(x) \) takes a positive number \( x \) as an argument and sets the counter value to \( x \) if its current value is smaller than \( x \).
2. \( \text{Wait}(x) \) also takes a positive number \( x \) as an argument and blocks until the counter value has advanced to at least \( x \).
3. \( \text{Read}() \) returns the current counter value.

A Broadcast object is owned by a process and only the owner can change the value of the object. Thus Set operation can only be invoked by the owner process and Wait operation can only be invoked by a non-owner process.

An operation of a Broadcast object is invoked by a process from within an RME algorithm. As such, if a process crashes while executing the operation, then it does not resume execution from where it failed upon recovery. Rather, like in an RME algorithm, the process restarts from the beginning. In the context of a Broadcast object, this translates to the process invoking the operation again at some point in the future. We formalize this behavior by requiring a history of the RME algorithm, when limited to the steps relevant to the Broadcast object, to satisfy certain properties.

As such, in the rest of this section, we consider a history to only consist of steps taken by processes while executing the operations of a Broadcast object. We refer to different invocations of operations in a history as instances. An instance of an operation terminates when the calling process either crashes (while executing the instance) or returns (from the invocation).

A history \( H \) is said to be well-formed with respect to a Broadcast object if it satisfies the following conditions:

\( W1 \) The owner process invokes \( \text{Set} \) operation in an incremental manner. Specifically, let \( \text{Set}(x) \) and \( \text{Set}(y) \) be two consecutive instances of the \( \text{Set} \) operation in \( H \). Then, \( x \leq y \leq x + 1 \).

\( W2 \) The argument of every \( \text{Wait} \) operation is "close" to the argument of its immediately preceding \( \text{Set} \) operation. Specifically, let \( x \) denote the argument of a \( \text{Wait} \) operation in \( H \), and let \( y \) denote the argument of its immediately
preceding invocation of Set operation in \( H \). In case no such Set operation exists, we set \( y \) to 0. Then, \( x \leq y + 1 \).

Intuitively, a well-formed history helps to guarantee that the Broadcast operations are safe.

An instance of an operation (Set, Wait or Read) is referred to as failure-free if the process does not crash while executing the instance. An instance of Wait or Read operation is said to have completed-successfully if it has terminated without failing. On the other hand, an instance of Set(\( x \)) is said to have completed-successfully if it has terminated (possibly with a failure) and an invocation of the Read operation by the owner immediately afterwards would return the value at least \( x \). Note that an instance of Set operation may have completed-successfully even though it was not failure-free if the owner process was able to execute “enough” steps before crashing.

We now formulate requirements on the history to guarantee that the Broadcast operations are live. These requirements are primarily needed for the DSM model because its algorithm is based on helping. To that end, we define the notion of a legal history, which is based on the notion of run.

Given a history \( H \) and a process \( p \) that is live in \( H \), let \( W(H, p) \) denote the sequence of all instances of Wait operation invoked by \( p \) in \( H \). A non-empty sub-sequence \( \lambda \) of the sequence \( W(H, p) \) forms a run if it satisfies the following conditions:

(a) All instances in \( \lambda \) have the same argument.
(b) Two instances are consecutive in \( \lambda \) only if they are consecutive in \( W(H, p) \).
(c) Every non-last instance in \( \lambda \) terminates with a failure (i.e., does not complete-successfully).

Note that the last instance in \( \lambda \), in case \( \lambda \) is finite, may or may not terminate, and, if it does terminate, it may terminate with a failure. We are now ready to define the notion of legal history. A well-formed history \( H \) is said to be legal if it satisfies the following conditions:

(L1) If an instance (of an operation) invoked by a process \( p \) in \( H \) has not terminated, then eventually \( p \) either crashes or takes another step in \( H \).
(L2) Every run in \( H \) contains a finite number of instances.
(L3) The last instance of every maximal run in \( H \) is failure-free.

The first condition (L1) implies that a history does not abruptly stop in the “middle” of an operation. The last two conditions (L2) and (L3) together imply that a process repeatedly invokes an instance of Wait operation with the "same" argument until it is able to execute a failure-free instance.

Our algorithm for the Wait operation under the DSM model uses helping as it uses a wakeup-chain to bound the worst-case RMR complexity by \( O(1) \). As such, it is guaranteed to complete-successfully only if the history is legal.

7.2 Implementation

We describe implementations of the Broadcast object separately for CC and DSM models since the algorithms to achieve \( O(1) \) RMR complexity for all three operations are quite different.

7.2.1 CC model. It is relatively trivial to implement the Broadcast object for the CC model in which all three operations have \( O(1) \) RMR complexity in the worst case as shown in algorithm 5.

The algorithm uses a single shared MRSW integer variable \( count \). In Set(\( x \)) operation, the owner process writes \( x \) to the \( count \) if its current value is smaller than \( x \) (lines C.13 to C.14). In Wait(\( x \)) operation, a non-owner process spins until the variable has value of at least \( x \) (line C.18). In Read operation, the process simply returns the current value
Algorithm 5: Pseudocode of process $p_i$ for implementing Broadcast object under the CC model.

C.1 shared variables
   
C.2 // integer variable to model the counter
   C.3 count;

C.4 initialization
C.5 begin
   C.6 // initialize counter value
   C.7 count ← 0;

C.8 end
   /* returns the current counter value */
C.9 Function Read( )
C.10 begin
   C.11 return count;
C.12 end

C.13 Function Set( x: integer variable )
C.14 begin
   C.15 if (count ≥ x) then return:
   C.16 count ← x;
C.17 end
   /* wait until the counter has reached a desired value; can only be invoked if process $p_i$ is a non-owner process */
C.18 Function Wait( x: integer variable )
C.19 begin
   C.20 await count[i] ≥ x;
C.21 end

of count (line C.9). Note that only Wait operation has a loop, and (W2) guarantees that a process busy-waiting in the
loop incurs only $O(1)$ RMRs.

We refer to the algorithm for the CC model as Broadcast-CC.

7.2.2 DSM model. The solution for the CC model has unbounded RMR complexity for Wait operation in the DSM
model. This is because, when $n \geq 3$, at least one non-owner process has to spin on a remote memory location
Another approach is for a non-owner process to spin on a local memory location, while the owner process is responsible
for waking up all the waiting processes by updating the memory location of each spinning process. This approach,
however, yields $O(n)$ RMR complexity for Set operation.

In this section, we describe an efficient algorithm to implement the Broadcast object in the DSM model that incurs
only $O(1)$ RMRs for all three operations and uses $O(n)$ space per Broadcast object. The main idea is that, instead of
notifying the spinning processes by itself, the owner process creates a wake-up chain in its local memory such that
each process in the chain is responsible for waking up at most one other process. The owner process then only needs
to wake up the first process in the chain. This technique is similar to the one used by Golab, et al. in [14] to derive a
leader election algorithm with $O(1)$ RMR complexity under the DSM model. However, their algorithm was designed
to operate in a failure-free environment, whereas our algorithm is designed to be recoverable. Further, our Broadcast
object can be used repeatedly by processes for synchronization with no additional space overhead.

The pseudocode of our algorithm is given in algorithm 6. Our algorithm uses two shared integer variables, namely $A$
and $B$, and three shared integer array variables, namely announce, target and wakeup. Each array variable is of size
$n$ with one entry for each process. The variables $A$ and $B$ both store the counter value; they are updated at beginning
and end, respectively, of a Set operation. The array variables announce and wakeup are local to the owner process.
However, the array variable target is distributed among all processes with the $i$-th entry local to process $p_i$. A process
$p_i$ uses announce[i] to inform the owner process of its intention to wait until the counter value has advanced to a
desired value and target[i] to busy-wait until it is released (from spinning) by another process (note that target[i] is
local to $p_i$). Finally, the owner process uses the wakeup array to set up a wake-up chain, where $p_i$, upon waking up, is
responsible for notifying the process whose identifier is stored in wakeup[i], if any.

Wait operation. Let $x$ denote the input argument of the operation. The invoking process, say $p_i$, writes $x$ to target[i]
and announce[i] in order (lines D.40 to D.41), thereby informing the owner process of its intention to wait for the
Algorithm 6: Pseudocode of process $p_i$ for implementing Broadcast object under the DSM model.

D.1 shared variables
   // two integer variables to model the counter
D.2   $A, B$: integer variable;
   /* used by a non-owner process to inform the owner process of its intention to wait until the counter has advanced to a certain value; all entries are local to the owner process */
D.3   announce: array $[1..n]$ of integer variable;
   /* memory location for each non-owner process to spin on; the $i$-th entry is local to process $p_i$ */
D.4   target: array $[1..n]$ of integer variable;
   /* used by the owner process to create a wake-up chain; all entries are local to the owner process */
D.5   wakeup: array $[1..n]$ of integer variable;
D.6 initialization
D.7 begin
   // initialize both counter values
D.8   $A ← 0$;
D.9   $B ← 0$;
D.10 foreach $j ∈ \{1, 2, …, n\}$ do
D.11     target[$j$] ← 0;
D.12    announce[$j$] ← 0;
D.13    wakeup[$j$] ← 0;
D.14 end foreach
D.15 end
   /* returns the current counter value */
D.16 integer Function Read() 
D.17 begin
D.18   return $B$;
D.19 end
D.20
D.21 Function Set( $x$: integer variable )
D.22 begin
D.23 if ($B ≥ x$) then return;
D.24 $A ← x$;  // update the first counter
D.25 /* create the wake-up chain */
D.26 last ← 0;
D.27 for $j ← 1$ to $n$ do
D.28    if (announce[$j$] = $x$) then
D.29        /* assign process $p_j$ to wake-up the last waiting process */
D.30        wakeup[$j$] ← last;
D.31        /* affirm that process $p_j$ is still waiting */
D.32        last ← $j$;
D.33 end if
D.34 end for
D.35 if (last > 0) then
D.36 $B ← x$;  // update the second counter
D.37 end
D.38 Function Wait( $x$: integer variable )
D.39 begin
D.40 target[$i$] ← $x$;  // initialize the location to spin on
D.41 announce[$i$] ← $x$;  // announce the intention to wait
D.42 /* no need to wait if the owner process has previously invoked Set operation with argument value $x$ */
D.43 if ($A ≥ x$) then
D.44     target[$i$] ← 0;   // reset the location
D.45     /* spin until some process resets the location */
D.46 end if
D.47 await target[$i$] = 0;
D.48 announce[$i$] ← 0;  // revoke the announcement
D.49 $k ←$ wakeup[$i$];  // check if any process to wake up
D.50 if ($k > 0$) then
D.51 /* wake up the next process in the chain */
D.52 CAS( target[$k$], $x$, 0);
D.53 end if
D.54 $B ← x$;  // update the second counter
D.55 end

...
instruction (line D.49). Note that the target array may contain multiple chains; our algorithm ensures that all processes in the same chain are reached with the same value.

Set operation. Let x denote the input argument of the operation. The invoking process first writes x to A variable (line D.23). This ensures that any process that invokes Wait(x) hereafter does not block. It then scans the announce array looking for processes that may be waiting for the counter value to advance to x and chains all of them together (in reverse order of their identifiers) using the wakeup array (lines D.24 to D.32). Consider two processes p_k and p_j with k < j such that announce[k] = x, announce[j] = x and, for each k with k < j, announce[k] ≠ x. The owner process then sets wakeup[j] = ℓ indicating that process p_j, upon being released from spinning, is responsible for notifying process p_k. After writing ℓ to wakeup[j], the owner process reads announce[j] again (line D.28) to ascertain that p_j has not already stopped busy-waiting and thus may have missed reading wakeup[j] field; otherwise it may create a situation in which p_k spins indefinitely with no process responsible for notifying it. After building this chain, the owner process notifies the first process in the chain by clearing its entry in the target array (line D.34), which then leads to a sequence of cascading notifications. Finally, it writes x to B variable (line D.36).

Read operation. It returns the value of B variable (line D.18). The main use of the operation is to determine the last set operation that completed-successfully, prior to invoking a new set operation.

All three operations are designed to be idempotent in the sense that executing an operation multiple times with the same argument, possibly partially in some cases, does not lead to any erroneous behavior.

We refer to the algorithm for the DSM model as Broadcast-DSM.

7.3 Correctness proofs

We focus on proving the correctness of Broadcast-DSM because the correctness proof of Broadcast-CC is quite straightforward.

In the rest of this section, we use p_w to refer to the owner process. The following proposition follows from the facts that only p_w can write to A and p_w invokes set operation in an incremental manner (W1).

Proposition 7.1. Given a well-formed history H, if the variable A has value at least x at time t, then there exists an invocation of Set(x) by p_w in H at or before time t.

The next proposition follows from code inspection.

Proposition 7.2. Given a well-formed history H, if process p_w executes the CAS instruction on line D.34 with an expected value of x at some time t, then the variable A has a value that is at least x at time t in H.

Next, we prove the same property for a non-owner process.

Lemma 7.3. Given a well-formed history H, if a process p_i, where i ≠ w, executes the CAS instruction on line D.49 with an expected value of x at time t, then the variable A has a value that is at least x at time t in H.

Proof. It is sufficient to prove that the statement holds if p_i is the first non-owner process in H to invoke the CAS instruction line D.49 with the expected value of x. As the code inspection shows, p_i executes the CAS instruction only after quitting its busy-waiting loop, which can happen only after the entry target[i] has been reset (to zero). The entry can be reset in only three ways. First, p_i resets target[i] itself at line D.43 because it read the value of A to be at least
x earlier at line D.42. Second, \( p_w \) resets \( target[i] \) using the CAS instruction on line D.34. In this case, it follows from proposition 7.2 that \( A \) has value at least \( x \) at the time \( p_w \) performed the CAS instruction. Third, another non-owner process, say \( p_j \) with \( j \not\in \{w, i\} \), resets \( target[i] \) using the CAS instruction on line D.49. By our assumption that \( p_j \) is the first non-owner process to invoke the CAS instruction line D.49 with an expected value of \( x \), the third case cannot occur.

\[ \square \]

**Theorem 7.4.** Given a well-formed history \( H \), if an invocation of \( \text{Wait}(x) \) by a process \( p_r \), where \( r \not= w \), returns at some time \( t \) in \( H \), then process \( p_w \) has invoked \( \text{Set}(x) \) before time \( t \) in \( H \).

**Proof.** As the code inspection shows, \( p_r \) quits the busy-waiting loop in the \( \text{Wait} \) operation after \( target[r] \) has been reset to 0. The entry can be reset in only three ways. We show that each of the three cases implies that the value of \( A \) is at least \( x \) at the time the entry was reset. The statement then follows from proposition 7.1.

First, \( p_r \) resets \( target[r] \) itself at line D.43 because it read the value of \( A \) to be at least \( x \) earlier at line D.42.

Second, \( p_w \) resets \( target[r] \) using a CAS instruction on line D.34. In this case, it follows from proposition 7.2 that the value of \( A \) is at least \( x \) at the time the entry was set.

Third, another non-owner process, say \( p_s \), where \( s \not\in \{w, r\} \), resets \( target[r] \) using a CAS instruction on line D.49. In this case, it follows from lemma 7.3 that the value of \( A \) is at least \( x \) at the time the entry was reset. The result then follows from proposition 7.1.

\[ \square \]

In Broadcast-DSM, \( \text{Set} \) operation completes-successfully once it has successfully executed line D.36.

**Theorem 7.5.** Let \( H \) be a legal history in which at least one instance of \( \text{Set}(x) \) completes-successfully. Then every instance of \( \text{Wait}(x) \) eventually terminates.

**Proof.** It suffices to only consider failure-free instances of \( \text{Wait}(x) \). Assume, on the contrary, that there exists at least one process in \( H \) that invokes \( \text{Wait}(x) \) and does not crash but the invocation never returns. Among all such processes, pick the one with the largest identifier, say \( p_\ell \), and let \( I_\ell \) denote an instance of \( \text{Wait}(x) \) in \( H \) invoked by \( p_\ell \) that never terminates. This also implies that \( p_\ell \) eventually advances to the busy-waiting loop during \( I_\ell \) (L1) and gets stuck in the loop. Let \( I_w \) denote the first instance of \( \text{Set}(x) \) in \( H \) that \( p_w \) is able to complete-successfully. It follows from code inspection that \( p_w \) is able to write \( x \) to variable \( B \) (line D.36) during \( I_w \). Further, any subsequent invocation of \( \text{Set}(x) \) by \( p_w \) in \( H \) simply returns after ascertaining that variable \( B \) has value at least \( x \), without creating any “new” wake-up chain.

Before proceeding further with the proof, we define some notation. Suppose a process \( p \) is executing an instance \( I \) of an operation \( op \), where \( op \in \{\text{Set}, \text{Wait}\} \). Let \( m \) denote the number of a line belonging to \( op \) in the pseudocode shown in algorithm 6. If the line is not part of the for-loop in \( \text{Set} \), then we use \( t(I, m) \) to denote the time when \( p \) finished executing the line numbered \( m \) during \( I \). Otherwise, we use \( t(I, m, k) \) to denote the time when \( p \) finished executing the line for the iteration (of the for-loop) with \( j \) set to \( k \) during \( I \). Finally, given a variable \( var \), we use \( var^t \) to denote the value of \( var \) at time \( t \).

For ease of exposition, unless otherwise stated, steps of processes \( p_w \) and \( p_\ell \) are assumed to belong to instances \( I_w \) and \( I_\ell \), respectively.

Since \( p_\ell \) never advances beyond the busy-waiting loop, \( target[\ell] \) and \( announce[\ell] \) are never reset. Formally,

\[ \forall t : t \geq t(I_\ell, D.42) : (announce^t[\ell] = x) \land (target^t[\ell] = x) \]
Clearly, \( p_\ell \) reads the value of \( A \) before \( p_w \) writes value \( x \) to \( A \). Formally,
\[
t(I_\ell, D.42) < t(I_w, D.23)
\] (2)
We use \( C = \{c_1, c_2, \ldots, c_h\} \) to denote the set of process indices in the wake-up chain created by \( p_w \) (in the reverse order of their identifiers). We prove that \( p_\ell \) must be part of this wake-up chain, i.e., \( \ell \in C \). Using (1) and (2), we can infer that
\[
\forall t : t \geq t(I_w, D.23) : (\text{announce}^{\ell}[t] = x) \land (\text{target}^{\ell}[t] = x)
\] (3)
This implies that, when \( p_w \) reads the value of \( \text{announce}[\ell] \) twice at lines D.26 and D.28, it finds it to be \( x \) both times. Thus \( \ell \in C \).

It is now sufficient to prove that some process executes \( \text{CAS}(\text{target}[\ell], x, 0) \) after time \( t(I_w, D.23) \), thereby resetting \( \text{target}[\ell] \) to 0 and enabling \( p_\ell \) to quit its busy-waiting loop. The remainder of the code after the busy-waiting loop is wait-free, thereby implying that \( l_\ell \) eventually returns. This will contradict our original assumption that \( l_\ell \) never returns. There are two cases to consider.

**Case 1** (\( \ell = c_1 \)) : It follows from code inspection that \( p_w \) proceeds to reset \( \text{target}[c_1] \) to 0 using a \( \text{CAS} \) instruction, which is guaranteed to succeed due to (3).

**Case 2** (\( \ell = c_j \), where \( j > 1 \)) : Since \( p_{c_{j-1}} \) is part of the wake-up chain created by \( p_w \), when \( p_w \) reads \( \text{announce}[c_{j-1}] \) for the second time, \( p_w \) finds that \( \text{announce}[c_{j-1}] \) has value \( x \). This implies that \( l_w \) "overlaps" with one or more runs of \( \text{Wait}(x) \) invoked by \( p_{c_{j-1}} \). Let \( l_{c_{j-1}} \) denote the last instance of the last run of \( \text{Wait}(x) \) invoked by \( p_{c_{j-1}} \) that "overlaps" with \( l_w \). Note that \( l_{c_{j-1}} \) is guaranteed to exist because: (i) \( l_w \) is finite (by choice of \( l_w \)) and hence there is a last run, and (ii) every run in \( H \) is of finite length (L2) and hence the last run has a last instance. Furthermore, \( l_{c_{j-1}} \) is failure-free since the last instance of every maximal run in \( H \) is failure-free (L3). By our choice of \( p_\ell, l_{c_{j-1}} \), is finite (i.e., completes-successfully). Again, for ease of exposition, unless otherwise stated, steps of process \( p_{c_{j-1}} \) are assumed to belong to instance \( l_{c_{j-1}} \).

By our choice of \( l_{c_{j-1}} \), once \( p_{c_{j-1}} \) resets \( \text{announce}[c_{j-1}] \) to 0, it is not set to \( x \) again at least until \( l_w \) terminates. Formally,
\[
\forall t : t(l_{c_{j-1}}, D.46) \leq t(l_w, D.36) : \text{announce}^{\ell}[c_{j-1}] \neq x
\] (4)
It follows from code inspection that \( p_w \) writes \( c_j \) to \( \text{wakeup}[c_{j-1}] \) before it reads \( \text{announce}[c_{j-1}] \) for the second time. Formally,
\[
t(I_w, D.27, c_{j-1}) < t(I_w, D.28, c_{j-1})
\] (5)
Since \( p_{c_{j-1}} \) is part of the wake-up chain created by \( p_w \), when \( p_w \) reads \( \text{announce}[c_{j-1}] \) for the second time, \( p_w \) finds that \( \text{announce}[c_{j-1}] \) has value \( x \). Thus, using (4), we can infer that
\[
t(I_w, D.28, c_{j-1}) < t(l_{c_{j-1}}, D.46)
\] (6)
It also follows from code inspection that \( p_{c_{j-1}} \) resets \( \text{announce}[c_{j-1}] \) to 0 before it reads the value of \( \text{wakeup}[c_{j-1}] \). Formally,
\[
t(l_{c_{j-1}}, D.46) < t(l_{c_{j-1}}, D.47)
\] (7)
Combining (5), (6) and (7), we obtain that \( p_w \) writes \( c_j \) to \( \text{wakeup}[c_{j-1}] \) before \( p_{c_{F-1}} \) reads from \( \text{wakeup}[c_{j-1}] \). Formally,

\[
    t(I_w, D.27, c_{j-1}) < t(I_{c_{j-1}}, D.47)
\]

When \( p_w \) reads \( \text{announce}[c_{j-1}] \) for the second time, it finds it to be \( x \). Thus, using (W1), we can infer that

\[
    \forall t : t(I_w, D.28, c_{j-1}) \leq t \leq t(I_{c_{j-1}}, D.47) : \text{announce}^t[c_{j-1}] \in \{x, 0\}
\]

Since any subsequent invocation of \( \text{Set}(x) \) by \( p_w \) (after \( I_w \)) does not create any new wake-up chain, it implies that \( p_w \) does not write to \( \text{wakeup}[c_{j-1}] \) between \( t(I_w, D.27, c_{j-1}) \) and \( t(I_{c_{j-1}}, D.47) \). As a result, when \( p_{c_{j-1}} \) reads the value of \( \text{wakeup}[c_{j-1}] \), it finds that it is set to \( c_j (= t) \). It follows from code inspection that \( p_{c_{j-1}} \) proceeds to execute \( \text{CAS}(\text{target}[i], x, 0) \), which is guaranteed to succeed due to (1).

In both cases, we arrive at a contradiction, thereby proving the statement.

The following theorem follows directly from code inspection since \( \text{Set} \) and \( \text{Read} \) operations are wait-free.

**Theorem 7.6.** Every instance of \( \text{Set} \) and \( \text{Read} \) operation in a legal history eventually terminates (possibly with a failure).

**Theorem 7.7.** Each instance of \( \text{Read} \), \( \text{Set} \) or \( \text{Wait} \) operation has worst-case RMR complexity of \( O(1) \).

**Proof.** It is trivial to see that \( \text{Read} \) incurs \( O(1) \) RMRs. The \( \text{Set} \) operation contains a loop from line D.24 to line D.32 where process \( p_w \) accesses variables \( \text{announce} \) and \( \text{wakeup} \). Both these variables are local to process \( p_w \) and thus the \( \text{Set} \) operation incurs \( O(1) \) RMRs. Finally, the \( \text{Wait} \) operation also contains only one loop at line D.45 where only variable \( \text{target}[i] \) is repeatedly accessed by process \( p_i \). The variable \( \text{target}[i] \) is local to process \( p_i \) and therefore the \( \text{Wait} \) operation also incurs only \( O(1) \) RMRs. Thus, the theorem holds.

It can be easily verified that \( \text{Broadcast-CC} \) satisfies theorems 7.4 to 7.7 as well.

8 **BOUNDING SPACE COMPLEXITY OF THE FRAMEWORK**

Note that our framework uses three types of locks—a weakly recoverable filter lock, a strongly recoverable \( n \)-process base lock and a strongly recoverable dual-port arbitrator lock. The first lock can be implemented using the weakly RME algorithm described in section 3. The second lock can be implemented using sub-logarithmic RME algorithm proposed by Katzan and Morrison\(^1\) in [22]. Finally, the third lock can be implemented using Yang and Anderson’s algorithm augmented to handle failures [16]. The RME algorithm by Katzan and Morrison has space complexity of \( O(n \log^2 n) \) under both CC and DSM models. The augmented Yang and Anderson’s algorithm has \( O(n) \) space complexity under both CC and DSM models. However, the weakly RME algorithm described in section 3 (WR-Lock) has unbounded space complexity because, upon generating a request, it allocates a queue node at run time (additional in case of unsafe failures). It is non-trivial to determine when the memory of these nodes can be reclaimed without causing the algorithm to misbehave due to dangling pointers while, at the same time, maintaining its \( O(1) \) RMR complexity.

In this section, we describe an algorithm for memory reclamation that can be used to bound the space complexity of augmented WR-Lock by \( O(n^2) \) under both CC and DSM models. Our memory reclamation algorithm uses ideas

\(^1\)The algorithm has the added feature of abortability, which is not used in our framework.
from two well known approaches for memory reclamation, namely epoch-based [11] and quiescent-state-based [3, 23], with the added benefits that it (a) has bounded space complexity and (b) is recoverable.

The quiescent-state-based memory reclamation algorithms assume that processes exhibit the following behavior:

,Q1) Every process alternates between quiescent and non-quiescent states during its execution.
,Q2) A process can access a shared object only when it is in a non-quiescent state.
,Q3) A shared object has to be retired before its memory can be reclaimed.
,Q4) While in a non-quiescent state, a process cannot access any shared object that was retired prior to it entering its non-quiescent state.

This behavior can be leveraged to obtain the following general memory reclamation scheme: upon retiring a shared object, a process can reclaim the memory of the object safely after every process in the system has been in its quiescent state at least once since then. We use this main idea to design a memory reclamation algorithm that has the desired RMR and space complexities.

If processes do not fail, then quiescent and non-quiescent states of a process can be taken to be NCS segment and passage, respectively, and it can be verified that properties (Q1)–(Q4) hold. If processes can fail, then one possible approach is to consider a process to be in non-quiescent state when it is executing its super-passage. Although the properties (Q1)–(Q4) hold, however, this straightforward extension does not yield a memory reclamation algorithm with bounded space complexity, at least directly. This is because, every time a process experiences an unsafe failure, it needs a “fresh” queue node. As a result, a process may “consume” an arbitrarily large number of queue nodes during a single super-passage.

To obtain a memory reclamation algorithm with bounded space complexity, we model a super-passage of WR-Lock as consisting of a sequence of attempts. Loosely speaking, an attempt begins when a process requests allocation of a new node at line W.23 (using the GetNewNode function) and ends when it retires\(^\text{2}\) the allocated node at line W.58 (using the RetireLastNode function). We use two monotonically non-decreasing counters for every process to demarcate the beginning and end of its attempt. The counters for process \(p_i\) are denoted by \(\text{start}[i]\) and \(\text{finish}[i]\); the latter is a Broadcast object described in section 7. They represent the number of attempts a process has started (respectively, finished) across all super-passages so far. A process increments its start counter just before it enters the doorway of WR-Lock, and increments its finish counter at the completion of the RetireLastNode function.

If a process is not executing an attempt, it is said to be in a quiescent state, at which point its two counters will have the same value. At all other times, the finish counter of each process lags behind its start counter by exactly one. As desired, when a process is executing the doorway or waiting room of WR-Lock as part of an attempt, it is in non-quiescent state.

Note that “attempt” and “passage” are related but different concepts. They provide two different ways to model the execution of a process within its super-passage. The boundaries of attempts and passages do not align. A failure ends a passage but not an attempt. A process may fail multiple times during an attempt. As such, an attempt of a process can overlap with multiple passages of that process, but a passage of a process can overlap with most two attempts of that process.

\(\textbf{Definition 8.1 (useful attempt).}\) An attempt of a process is said to be useful if the process takes at least one step of its CS segment during the attempt; otherwise, it is said to be useless.

\(\textsuperscript{2}\text{Note that the notion of “retire” is distinct from that of “relieve” (defined in section 4.4). Also, note that a node is relieved before it is retired.}\)
It can be shown that an attempt of a process becomes useless if and only if the process crashes while executing the FAS instruction at line \text{W.32}. Every completed super-passage in an infinite fair history consists of at least one useful attempt. In particular, the last attempt of a completed super-passage is useful. A node allocated during an attempt is said to be have been \textit{retired} if the process has completed the execution of the \textsc{RetireLastNode} function during that attempt at least once without crashing. It can be easily verified that:

\textbf{Proposition 8.2.} \textit{WR-Lock satisfies (Q1)--(Q4).}

\textbf{Proposition 8.3.} \textit{A process consumes at most one queue node during an attempt.}

Note that, even after a node has retired, another process may still hold a reference to that node and may dereference it in the future. Our memory reclamation algorithm relies on the notion of a \textit{grace period} to determine when it is safe to reclaim the memory of a node after it has been retired [3, 17, 23]. A time interval \([t, t']\) is said to be a \textit{grace period} if, after time \(t'\), no process holds a reference to any node that was retired at or before time \(t\). We define a related notion of allowance period to highlight the grace period \textit{with respect to a retired node} as follows.

\textit{Definition 8.4 (allowance period).} Given a history \(H\) and a node \(x\), an interval \([t, t']\) in \(H\) is said to be the \textit{allowance period} with respect to \(x\) if \(x\) was retired at time \(t\) and no process holds any reference to \(x\) after time \(t'\).

It follows from proposition 8.2 that:

\textbf{Lemma 8.5.} \textit{The allowance period with respect to a node retired at time \(t\) expires once every process has been in a quiescent state at least once after time \(t\).}

Typically, in existing epoch based memory reclamation algorithms, a process uses a \textit{non-blocking} method to detect that the allowance period of a node it retired earlier has expired. The length of allowance period depends on the execution speeds of other processes. As such, it may last arbitrarily long, during which period the process may retire many more (possibly unbounded number of) nodes. This makes it hard to achieve bounded space complexity. In this work, we use a \textit{blocking} approach to detect that the allowance period of a retired node has expired. This is feasible in our case because the underlying application, namely mutual exclusion, is inherently blocking (provided that any additional blocking does not create a deadlock). One of the main components of our memory reclamation algorithm is a routine to detect expiration of the allowance period with respect to a retired node (or, more precisely, a set of retired nodes), denoted by \textit{APTD} routine, using a blocking synchronization that yields a bounded space complexity. In particular, the routine is designed to satisfy the following property:

\textbf{Lemma 8.6.} \textit{Suppose an instance of APTD routine began at time \(t\) and completed at time \(t'\). Then, the allowance period of every node retired at or before time \(t\) has expired at or after time \(t'\).}

A simple approach to implement the APTD routine is as follows. A process, while in its quiescent state, waits for the \textit{finish} counter of every process to "catch up" to its \textit{start} counter, one-by-one. After the APTD routine completes, it follows from lemma 8.6 that the process can safely reclaim the memory of any node it retired in the previous attempt. Due to its blocking nature, a process executes the APTD routine in the \texttt{Enter} segment before starting a new attempt in order to maintain BR and BE properties. Executing the routine in a quiescent state cannot create any deadlock since, both \textit{start} and \textit{finish} counters have the same value while a process is in a quiescent state, and the process does not own any node in any sub-queue section 4.4. Thus, no process can be busy-waiting on another process executing the APTD routine. This approach, however, increases the RMR complexity of each passage of WR-Lock to \(O(n)\).
8.1 Achieving constant RMR complexity

A possible approach to reduce RMR complexity is to amortize the overhead of executing a APTD routine over $\Omega(n)$ attempts. For example, a process can execute the APTD routine after every $n$ attempts. Once the APTD routine completes, all nodes retired prior to the $n$ attempts can be safely reclaimed. This, however, requires another set of $n$ nodes that can be used to service requests for allocating queue nodes during these $n$ attempts. Thus, to use this optimization, a process has to maintain two pools of nodes, each containing $n$ nodes. While nodes in one pool are waiting for their allowance period to expire, nodes in the other pool can be used to serve requests for node allocation. We refer to the two pools as active and backup with obvious meaning. The role of the two pools is then switched after every $n$ attempts. With this optimization, each passage of WR-Lock has $O(1)$ RMR complexity in the amortized case but $O(n)$ RMR complexity in the worst case.

We now describe a way to keep the worst-case RMR complexity of each passage at $O(1)$. The main idea is to execute the APTD routine incrementally over $\Theta(n)$ attempts in such a way that (a) is recoverable, (b) adds only $O(1)$ RMRs to each passage of WR-Lock, (c) uses only $O(n^2)$ space, and (d) maintains the CI-FCFS property of WR-Lock.

To maintain the fairness guarantee, we use a third counter that is incremented after a process has completed the doorway of the original WR-Lock without crashing during a passage, referred to as checkpoint counter. The checkpoint counter for process $p_i$ is denoted by $checkpoint[i]$ and is basically a Broadcast object described in section 7. At any given time, the counters satisfy the following invariants for each process $p_i$:

$$\begin{align*}
start[i] - 1 &\leq finish[i] \leq checkpoint[i] \leq start[i]
\end{align*}$$

(10)

In case an attempt is rendered useless due to an unsafe failure, the checkpoint counter is incremented before the finish counter even though the process crashed while executing the doorway in order to maintain the above invariant.

**Phases and strides.** To design a recoverable APTD routine that can be executed incrementally, we divide the execution of the APTD routine into four phases as follows:

- **Phase 1 (snapshot phase):** the process reads and records the value of the start counter of each process.
- **Phase 2 (catch-up phase):** the process waits for the checkpoint counter of each process to catch up to its start counter.
- **Phase 3 (yield phase):** the process waits for the finish counter of each process to catch up to its start counter.
- **Phase 4 (switch phase):** the process switches the role of the two pools.

The second phase is required to achieve the desired fairness guarantee. To enable incremental execution of the APTD routing, we further divide each phase into multiple strides\(^5\). Intuitively, a stride constitutes a “unit of execution” of the APTD routine and incurs $O(1)$ RMRs under both CC and DSM models. The first three phases consist of $n$ strides each and the fourth phase consist of two strides. Thus the routine as a whole consists of $3n + 2$ strides. A **single stride** of the APTD routine is executed by invoking the function $executeOneStride$. Each process maintains a stride counter to keep track of the numbers of strides of the current instance of the APTD routine it has executed so far; the counter is reset during the switch phase as the designation of the two pools is flipped. We use $stride[i]$ to denote the stride counter of process $p_i$. The pseudocode of the function $executeOneStride$ is shown in algorithm 7. The function is written in a way such that executing it multiple times with the same value of the stride counter does not cause any undesirable behavior. Further, we consider repeated invocations of $executeOneStride$ function when the stride counter

\(^5\)A stride means a long step, which is an apt description of what it denotes in this context.
counter of the invoking process has the same value until the value of the stride counter changes as essentially the same stride.

*When to execute a stride?* The main idea is to execute one stride of the APTD routine “between” two consecutive attempts. Specifically, our memory reclamation algorithm satisfies the following property:

**Proposition 8.7.** Suppose a process begins two consecutive attempts at times $t$ and $t'$ with $t < t'$. Then, it executes at least one stride of the APTD routine without failing between times $t$ and $t'$.

To ensure that the currently active pool does not run out of nodes at least until all strides of the APTD routine have been executed successfully, each pool now consists of $3n + 2$ nodes. When combined with proposition 8.7, this is necessary and sufficient because the APTD routine consists of $3n + 2$ strides and a process can consume at most one node in an attempt.

If fairness can be foregone, then a simple memory reclamation algorithm that meets all other desirable requirements (except for fairness) works as follows. A process executes one stride of the APTD routine in its `Enter` segment if it is in quiescent state. Executing a stride of the APTD routine in quiescent state, specifically after finishing an attempt but before starting a new attempt, helps to easily avoid a deadlock.

### 8.2 Achieving fairness

A fairness property is typically defined with respect to a doorway, which is a *wait-free* piece of code that a process executes at the beginning of an `Enter` segment. As described earlier, a process executes a stride of the APTD routine at the *beginning* of its `Enter` segment when in a quiescent state before starting a new attempt. Since a stride may involve blocking (i.e., busy waiting in a loop), it makes it infeasible to define the notion of doorway in the algorithm described so far.

To remedy this shortcoming, we proceed as follows. If an attempt of a process is useful, then the process executes a stride of the APTD routine immediately after completing the doorway of `WR/Lock` rather than after completing that attempt. We refer to this stride as *regular stride*. However, if an attempt of a process is useless, then the process executes a stride of the APTD routine immediately after completing that attempt as before (in quiescent state). We refer to this stride as *penalty stride*. With this change, it can be verified that proposition 8.7 still holds. Note that a process executes both types of strides during its `Enter` segment. Specifically, a process executes *at most one* regular and *at most one* penalty stride during its `Enter` segment so that the (worst-case) RMR complexity of a passage remains $O(1)$.

To ensure the BCSR property, we guarantee that a process executes a regular stride during an attempt exactly once. In other words, once it has completed a stride of the APTD routine, it does not execute another stride during that attempt even it were to fail and start a new passage (but same attempt); otherwise the process may not be able to reenter its CS segment within a bounded number of its own steps. To that end, whenever it starts a new attempt, it records the current value of its stride counter and executes a stride later only if the recorded and current values of its stride counter match. This also helps to avoid a deadlock by guaranteeing that a process that owns a node in a sub-queue never waits on a process that appended its node to the same sub-queue *after* its own. Specifically, we prove later that if a process $p_i$ is waiting on a process $p_j$ (either in the yield phase of the APTD routine or in the waiting room of `WR/Lock`) and attempts of both processes are useful, then $p_i$ executed its FAS instruction after $p_j$.  

Manuscript submitted to ACM
Algorithm 7: Pseudocode of process \( p_i \) for bounding space complexity of WR-Lock described in algorithm 2.

\[
\text{shared variables} \\
\mathcal{F}: \text{an instance of WR-Lock;} \\
\text{start: } \text{array } [1 \ldots n] \text{ of integer variable;} \\
\text{checkpoint: } \text{array } [1 \ldots n] \text{ of Broadcast object;} \\
\text{finsh: } \text{array } [1 \ldots n] \text{ of Broadcast object;} \\
\text{pool: } \text{array } [1 \ldots n][0, 1][1 \ldots 3n+2] \text{ of two pools of } 3n+2 \text{ QNodes;} \\
\text{currentPool: } \text{array } [1 \ldots n] \text{ of integer variable;} \\
\text{backupPool: } \text{array } [1 \ldots n] \text{ of integer variable;} \\
\text{snapshot: } \text{array } [1 \ldots n][1 \ldots n] \text{ of integer variable;} \\
\text{stride: } \text{array } [1 \ldots n] \text{ of integer variable;} \\
\text{penalty: } \text{array } [1 \ldots n] \text{ of boolean variable;} \\
\text{latest: } \text{array } [1 \ldots n] \text{ of integer variable;} \\
\text{initialization} \\
\text{begin} \\
\text{foreach } j \in \{1, 2, \ldots, n\} \text{ do} \\
\text{currentPool}[j] \leftarrow 0; \\
\text{backupPool}[j] \leftarrow 1 - \text{currentPool}[j]; \\
\text{start}[j] \leftarrow 0; \\
\text{stride}[j] \leftarrow 1; \\
\text{latest}[j] \leftarrow \text{stride}[j]; \\
\text{penalty}[j] \leftarrow \text{false}; \\
\text{foreach } k \in \{0, 1\}, \ell \in \{1, \ldots, 3n+2\} \text{ do} \\
\text{pool}[j][k][\ell] \leftarrow \text{new QNode}; \\
\text{end foreach} \\
\text{end foreach} \\
\text{end} \\
\text{Function ExecuteOneStride( )} \\
\text{begin} \\
\text{if } (\text{stride}[i] \in \{1, n\}) \text{ then} \\
\text{snapshot[i][i] \leftarrow start[j];} \\
\text{else if } (\text{stride}[i] \in \{n+1, 2n\} \text{ and } (j \neq i)) \text{ then} \\
\text{catch-up phase, wait for other processes to complete their doorway \text{/}} \\
\text{checkpoint[j].Wait(snapshot[i][j]);} \\
\text{else if } (\text{stride}[i] \in \{2n+1, 3n\} \text{ and } (j \neq i)) \text{ then} \\
\text{yield phase: wait for other processes to complete their attempt \text{/}} \\
\text{finish[j].Wait(snapshot[i][j]);} \\
\text{else if } (\text{stride}[i] \in \{3n+1, 3n+2\}) \text{ then} \\
\text{switch phase: switch current and backup pools \text{/}} \\
\text{if } (\text{stride}[i] = 3n+1) \text{ then} \\
\text{switch the backup pool \text{/}} \\
\text{backupPool[i] \leftarrow currentPool[i];} \\
\text{else \text{/}} \\
\text{switch the current pool \text{/}} \\
\text{currentPool[i] \leftarrow 1 - backupPool[i];} \\
\text{end if} \\
\text{end if} \\
\text{if } (\text{stride}[i] < 3n+2) \text{ then} \\
\text{stride[i] := stride[i] + 1;} \\
\text{else stride[i] := 1;} \\
\text{end}
\]

We refer to the augmented weakly recoverable lock with bounded space complexity as WR-Lock-MR, and its pseudocode is given in algorithms 7 and 8. To avoid repetition, we only provide the pseudocode for Enter segment, GETNewNode function and RETIRELastNode function. The pseudocode for Recover and Exit segments is same as that for WR-Lock and has been omitted.

First, consider the Enter segment. A process first executes a penalty stride, if applicable (lines \text{M.48} to \text{M.53}). It then begins a new attempt, if in quiescent state, and also records the current value of the stride counter (lines \text{M.54} to \text{M.57}). It next executes the doorway of WR-Lock (line \text{M.58}) and increments the checkpoint counter if lagging (line \text{M.59}).
It then executes a regular stride, if needed (lines M.60 to M.62). Finally, it executes the waiting room of WR-Lock (line M.63).

Next, consider the GetNewNode function. We use stride counter as an index into the active pool. So an invocation of GetNewNode simply returns the reference to the node stored at the corresponding location in the pool (line M.68).

Finally, consider the RetireLastNode function. A process checks if the current attempt is useless, and, if so, sets the penalty flag and records the current value of the stride counter (line M.71). It then increments the finish counter if lagging (line M.76).

We now define the doorway of WR-Lock-MR as follows. Let $B$ denote the maximum number of steps a process executes in the Enter segment in order to reach line M.59 provided that the passage is exclusive. Recall that, in an exclusive passage, the process does not execute a penalty stride. In the absence of penalty stride, the code in the Enter segment contains one only bounded loop, namely in the Set operation (lines D.25 to D.32). The doorway of WR-Lock-MR then consists of the first $B$ steps of a process in the Enter segment.

### 8.3 Correctness proofs

Note that WR-Lock-MR uses $2n$ Broadcast objects for synchronization among processes given by $\text{checkpoint}[i]$ and $\text{finish}[i]$ for each $i = 1, 2, \ldots, n$. As such, the correctness of WR-Lock depends on the broadcast objects behaving

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as expected (satisfying safety and liveness properties). In particular, the conditions mentioned in the statements of theorems 7.4 and 7.5 should hold as and when needed. For example, theorem 7.4 requires that the (sub)history with respect to a Broadcast object should be well-formed, while theorem 7.5 requires that the (sub)history should be legal as well.

The correctness proof consists of two parts. We first argue that the conditions required for a Broadcast object to behave correctly actually hold. We then argue that WR-Lock-MR behaves correctly.

### 8.3.1 Broadcast objects behave correctly

For each \( i = 1, 2, \ldots, n \), process \( p_i \) owns the two Broadcast objects \( \text{checkpoint}[i] \) and \( \text{finish}[i] \). As required, only process \( p_i \) invokes Set operation on \( \text{checkpoint}[i] \) and \( \text{finish}[i] \), and, only process \( p_j \), where \( j \in \{1, 2, \ldots, n\} \setminus \{i\} \), invokes Wait operation on \( \text{checkpoint}[i] \) and \( \text{finish}[i] \). For convenience,

\[
\mathcal{B} = \{\text{checkpoint}[i] \mid 1 \leq i \leq n\} \cup \{\text{finish}[i] \mid 1 \leq i \leq n\}
\]

Given a history \( H \) and a Broadcast object \( b \in \mathcal{B} \), we use \( H \mid b \) to denote the sub-history that consists of only those steps of \( H \) that processes take while executing an instance of one of the three operations of \( b \).

We first establish that the assumption postulated in theorem 7.4 holds.

**Theorem 8.8.** Let \( H \) denote a history of WR-Lock-MR. Then, for every Broadcast object \( b \in \mathcal{B} \), \( H \mid b \) is well-formed with respect to \( b \).

**Proof.** Consider a Broadcast object \( b \) owned by process \( p_i \).

The property \((W1)\) holds because (a) the argument passed to any instance of Set operation on \( \text{checkpoint}[i] \) or \( \text{finish}[i] \) counter is the current value of \( \text{start}[i] \) counter, and (b) \( \text{start}[i] \) counter has monotonically non-decreasing value.

The property \((W2)\) holds (a) the argument passed to any instance of Wait operation on \( \text{checkpoint}[i] \) or \( \text{finish}[i] \) counter is the value of \( \text{start}[i] \) counter read in the past, (b) \( \text{start}[i] \) counter has monotonically non-decreasing value, and (c) the three counters of a process \((\text{start}[i], \text{checkpoint}[i], \text{finish}[i])\) satisfy (10).

We next establish that the assumptions postulated in theorem 7.5 also hold. To that end, we need to prove that, under the assumptions made in the definition of the SF property, (i) the (sub)history with respect to a Broadcast object is legal, (ii) a checkpoint counter value eventually catches up to the corresponding start counter value and, (iii) a finish counter value eventually catches up to the corresponding start counter value. We prove each of the three conditions one-by-one.

A line \( t \) of a function \( f \) is said to be inevitable if it satisfies the following property: if a process fails while executing the line \( t \), then, in every invocation of the function \( f \) by the (same) process thereafter, the line \( t \) lies on all possible execution paths that can be taken by the process inside the function \( f \), until the execution of the line has been completed-successfully. Typically, a line is considered to have completed-successfully if the execution of the line was failure-free, except in some cases as follows. We say that line \( M.50 \) or line \( M.61 \) of the Enter function has been completed-successfully if the value of the stride counter is modified inside the function.

**Proposition 8.9.** Lines \( M.50 \) and \( M.61 \) of the Enter function are inevitable.

**Proposition 8.10.** Lines \( M.33 \) and \( M.35 \) of the ExecuteOneStride function are inevitable.

We are now ready to prove the desired results.
Theorem 8.11. Assume that every process fails only a finite number of times in each of its super-passage. Let \( H \) denote an infinite fair history of WR-LOCK-MR. Then, for every broadcast object \( b \in \mathcal{B} \), \( H \mid b \) is legal with respect to \( b \).

Proof. Consider a broadcast object \( b \) owned by process \( p_i \).

The property (L1) holds because, in an infinite fair history, a process can stop taking steps only after executing a failure-free passage.

The properties (L2) and (L3) hold because, as implied by propositions 8.9 and 8.10, if a process fails during an instance of Wait(x) operation, then it is guaranteed to repeatedly invoke instances of Wait(x) until the stride counter has changed. Moreover, a process can fail only a finite number of times during its super-passage, thereby implying that any run of Wait operation in \( H \) is of finite length and ends with a failure-free instance.

Theorem 8.12. Assume that every process fails only a finite number of times in each of its super-passage. Let \( H \) denote an infinite fair history of WR-LOCK-MR and consider a process \( p \). Then, for every positive value \( x \) assumed by \( \text{start}[i] \) counter in \( H \), there exists at least one instance of \( \text{set}(x) \) operation on checkpoint \([i]\) in \( H \) that completes-successfully.

Proof. After a process begins an attempt, it has to execute only a bounded number of steps to increment its checkpoint counter unless it fails. However, by assumption a process can fail only a finite number of times during each of its super-passage and hence during each of its attempt.

The proof for the last assumption (the finish counter value eventually catches up to the corresponding start counter value) is more involved since a process may have to wait after incrementing the checkpoint counter value but before incrementing the finish counter value. We classify a wait-for dependency into three types:

(T1) Waiting for a checkpoint counter value to catch up to the associated start counter value (line M.33 executed as part of penalty stride or regular stride).

(T2) Waiting for a finish counter value to catch up to the associated start counter value (line M.35 executed as part of penalty stride or regular stride).

(T3) Waiting inside the waiting-room as part of WR-Lock (line M.63).

Theorem 8.12 implies that waiting of type item (T1) is finite. So, we focus on the other two types of waiting and prove that they are finite as well. Note that, if an attempt of a process is rendered useless, then the process eventually abandons the queue node it allocated at the beginning of the attempt and increments its finish counter for that attempt. Therefore, we only focus on useful attempts and argue that every useful attempt eventually completes. To that end, we are only concerned with the situation in which a process \( p \) is waiting on another process \( q \) such that:

(A1) Both \( p \) and \( q \) are currently executing a useful attempt.

(A2) Both \( p \) and \( q \) have appended their respective nodes in the queue successfully using an FAS instruction.

The next lemma proves a crucial property common to both types of waiting.

Lemma 8.13. If a process \( p \) is waiting on another process \( q \) such that (A1) and (A2) hold, then \( p \) executed its most recent FAS instruction after that of \( q \).

Proof. Clearly, the statement holds if \( p \) is waiting for \( q \) in the waiting room of WR-Lock. Thus, it is sufficient to focus on the case in which \( p \) is waiting for \( q \) in the yield phase of a penalty or regular stride. Let the useful attempts of \( p \) and \( q \) be denoted by \( A_p \) and \( A_q \), respectively. We define four instants of time as follows:

- \( t_q \) is the time when \( q \) executed the FAS instruction for \( A_q \)
top left

> $t_c$ is the time when $p$ completed its stride for the first time during which it waited for the checkpoint counter of $q$ to catch up to its start counter for $A_q$
> $t_a$ is the time when $p$ started the attempt $A_p$
> $t_p$ is the time when $p$ executed the FAS instruction for $A_p$

We show that $t_q < t_c < t_a < t_p$, thereby proving that $t_q < t_p$.

> $t_q < t_c$ because a process executes the FAS instruction before incrementing the checkpoint counter for a admissible attempt
> $t_c < t_a$ because a process executes only one regular stride of APTD routine during a useful attempt (and, in the regular stride for $A_p$, $p$ is waiting for the finish counter of $q$ to catch up to its start counter for $A_q$)
> $t_a < t_p$ because a process executes the FAS instruction after starting an attempt

This proves that the statement holds.

Using the above lemma, we are now able to show the following.

**Theorem 8.14.** Assume that every process fails only a finite number of times in each of its super-passage. Let $H$ denote an infinite fair history of WR-Lock-MR. Then, every attempt in $H$ eventually completes.

**Proof.** Let $I(t)$ denote the set of attempts in $H$ that execute their FAS instructions at or before time $t$ and have not completed by time $t$.

Consider an arbitrary attempt, say $A$ in $H$. Clearly, a useless attempt has no busy-waiting loop and, thus, is guaranteed to complete. Therefore, assume that $A$ is a useful attempt. Let $p$ denote the process to which $A$ belongs, and let $t_A$ denote the time when $p$ performs the FAS instruction during $A$ to append its node to the queue.

Consider $I(t_A)$. We can order all attempts in $I(t_A)$ based on the sequence in which their FAS instructions are executed. Lemma 8.13 implies that, after time $t$, an attempt in $I(t_A)$ can only busy-wait on another attempt in $I(t_A)$. We can prove using induction (on the order in which FAS instructions are performed) that every attempt in $I(t_0)$ eventually completes.

Since $A$ was chosen arbitrarily, we can infer that every attempt in $H$ eventually completes.

Clearly, it follows that:

**Corollary 8.15.** Assume that every process fails only a finite number of times in each of its super-passage. Let $H$ denote an infinite fair history of WR-Lock-MR and consider a process $p_i$. Then, for every positive value $x$ assumed by start[$i$] counter in $H$, there exists at least one instance of Set(x) operation on finish[$i$] in $H$ that completes-successfully.

In other words, all three assumptions required for theorem 7.5 to apply hold.

### 8.3.2 WR-Lock-MR behaves correctly.

We only focus on SF and BCSR properties of the RME problem because the proofs for other properties (ME, BE, BR and CI-FCFS) are almost identical to those for WR-Lock.

To establish the SF property, we first prove the following lemma about a penalty stride.

**Lemma 8.16.** Assume that every process fails only a finite number of times in each of its super-passage. Let $H$ denote an infinite fair history of WR-Lock-MR and consider a process $p_i$. Then every penalty stride executed by a process in $H$ eventually terminates.
A process executing a penalty stride may either wait in the catch-up phase or the yield phase of the APTD routine. The first type of wait is finite due to theorem 8.12, while the second type due to corollary 8.15.

Thus we have:

**Lemma 8.17.** *WR-Lock-MR satisfies the SF property.*

**Proof.** When executing a passage, a process may wait at three different points: (a) while performing a penalty stride (line M.50), (b) while performing a regular stride (line M.61), or (c) while executing the waiting room of WR-Lock (line M.63) Lemma 8.16 establishes that the first type of waiting is finite. Theorem 8.14 establishes that the other two types of waiting are also finite.

**Lemma 8.18.** *WR-Lock-MR satisfies the BCSR property.*

**Proof.** If a process crashes inside its critical section, then it implies that the process is currently executing a useful attempt. We show that, upon restarting, it does not execute any stride of the APTD routine—penalty or regular.

It does not execute a penalty stride because it is not in a quiescent state. It does not execute a regular stride because it would have already executed one prior to entering the critical section for the first time during this attempt. By design, it does not execute another regular stride until it completes the current attempt by executing the Exit segment.

**Lemma 8.19.** *WR-Lock-MR satisfies the CI-FCTS property.*

It now follows that:

**Theorem 8.20.** *WR-Lock-MR satisfies ME, SF, BCSR, BE, BR and CI-FCTS properties. Further, it has $O(1)$ (worst-case) RMR complexity and $O(n^2)$ space complexity.*

**Theorem 8.21.** *The space complexity of BA-Lock is given by $O(\sqrt{n} \log n / \log \log n + S(n))$, where $S(n)$ denotes the space complexity of the base NA-Lock for $n$ processes.*

**Corollary 8.22.** *Assume that we use Katzan and Morrison’s RME algorithm [22] to implement the NA-Lock. Then the space complexity of BA-Lock is given by $O(\sqrt{n} \log n / \log \log n)$.*

### 9 RELATED WORK

Bohannon et al. [5, 6] were the first ones to investigate the RME problem. However, their system model is different from the one assumed in this work. Specifically, in their system model, at least one process is reliable while other processes may be unreliable. Once an unreliable process fails, it never restarts. The reliable process is responsible for continuously monitoring the health of all other processes, and, upon detecting that an unreliable process has failed during its passage, it performs recovery by “fixing” the lock. The two RME algorithms differ in the way they implement the lock; the one in [6] uses test-and-set instruction whereas the one in [5] uses MCS queue-based algorithm.

Golab and Ramaraju formally defined the RME problem in [15]. We use the same system model as in their work. In [15], Golab and Ramaraju also presented four different RME algorithms—a 2-process RME algorithm and three $n$-process RME algorithms. The first algorithm is based on Yang and Anderson’s lock [27], and is used as a building block to design an $n$-process RME algorithm. Both RME algorithms use only read, write and comparison-based primitives. The worst-case RMR complexity of the 2-process algorithm is $O(1)$ whereas that of the resultant $n$-process algorithm is $O(\log n)$. Both RME algorithms have optimal RMR complexity because, as shown in [2, 4, 27], any mutual exclusion

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algorithm that uses only read, write and comparison-based primitives has worst-case RMR complexity of $\Omega(\log n)$. The remaining two algorithms are unbounded adaptive (with $f(x) = x$) and semi-adaptive (with $g(x) = x$), respectively (where $f$ and $g$ are as per the definitions of adaptivity and boundedness respectively from section 2).

Later, Golab and Hendler [12] proposed an RME algorithm with sub-logarithmic RMR complexity of $O(\log n/\log \log n)$ under the CC model using MCS queue based lock [24] as a building block. Note that MCS uses FAS instruction, which is not a comparison-based RMW instruction, and thus the result does not violate the previously mentioned lower bound. Their algorithm does not satisfy the bounded exit property. Moreover, it has been shown to be vulnerable to starvation [19].

Ramaraju showed in [26] that it is possible to design an RME algorithm with $O(1)$ RMR complexity provided the hardware provides a special RMW instruction to swap the contents of two arbitrary locations in memory atomically. Unfortunately, at present, no hardware supports such an instruction to our knowledge.

In [20], Jayanti and Joshi presented an RME algorithm with $O(\log n)$ RMR complexity. Their algorithm satisfies bounded (wait-free) exit and FCFS (first-come-first-served) properties.

In [19], Jayanti, Jayanti and Joshi proposed an RME algorithm that has sub-logarithmic RMR complexity of $O(\log n/\log \log n)$. To our knowledge, this is the best known RME algorithm as far as the worst-case RMR complexity is concerned that also satisfies bounded recovery and bounded exit properties.

Using a weaker version of starvation freedom, Chan and Woelfel [8] present a novel solution to the RME problem that incurs a constant number of RMRs in the amortized case, but its worst case RMR complexity may be unbounded.

In [13], Golab and Hendler proposed an RME algorithm under the assumption of system-wide failure (all processes fail and restart) with $O(1)$ RMR complexity.

A useful extension to the RME problem is when a process may decide to abort its request for critical section; this extension is referred to as the abortable RME problem. Recently, Katzan and Morrison [22] and Jayanti and Joshi [21] have proposed efficient algorithms for solving the problem under both CC and DSM models. The algorithm by Jayanti and Joshi uses $f$-arrays and has $O(\log n)$ RMR complexity [21]. On the other hand, the algorithm by Katzan and Morrison uses a $k$-port abortable RME algorithm as a building block to design a sub-logarithmic abortable RME algorithm with RMR complexity of $O(\log n/\log \log n)$ [22].

Recently, Chan and Woelfel have proved a lower bound of $\Omega(\log n/\log \log n)$ on the RMR complexity of any RME algorithm using currently available hardware instructions and practical word size of $\Theta(\log n)$ [7].

10 CONCLUSIONS AND FUTURE WORK

In this work, we have described a general framework to transform any non-adaptive RME algorithm into a super-adaptive one without increasing its worst-case RMR complexity. In addition to the hardware instructions used by the underlying non-adaptive RME algorithm, our framework uses CAS and FAS RMW instructions, both of which are commonly available on most modern processors. When applied to the non-adaptive RME algorithm proposed by Jayanti, Jayanti and Joshi in [19] or Katzan and Morrison in [22], it yields a well-bounded super-adaptive RME algorithm that is simultaneously adaptive to (a) the number of processes competing for the lock, as well as (b) the number of failures that have occurred in the recent past, while having the same (asymptotic) worst-case RMR complexity as that of the base RME algorithm. We have also shown that the RME algorithm obtained by applying our framework is fair and satisfies a variant of the FCFS property, even if the base RME algorithm is unfair.

To make the framework practical, we have described an extension to our framework to reclaim the memory of shared objects when no longer needed. Our memory reclamation algorithm bounds the worst-case space complexity...
of the framework, while maintaining all its desirable properties at the same time. Our approach is general enough that it can be applied to other RME algorithms as well to bound their space complexity, such as Jayanti, Jayanti and Joshi’s algorithm in [19].

In our framework, a failed process, upon restarting, attempts to reacquire all the locks at every level it had advanced to, beginning from level one. As a result, the worst-case RMR complexity of a super-passage is given by $O(F_0 \cdot \min\{\bar{c}, \sqrt{F + 1}, \log n/\log\log n\})$, where $F_0$ denotes the number of times the process fails while executing its (own) super-passage. However, we can modify our framework to allow a process to keep track of its last level. With this modification, the worst case RMR complexity of a super passage reduces to $O(F_0 + \min\{\bar{c}, \sqrt{F + 1}, \log n/\log\log n\})$.

In the future, we plan to explore ways to design a more responsive and space-efficient filter lock. We also plan to develop efficient recoverable algorithms for important variants of the ME problem including read-write mutual exclusion (RWME) and group mutual exclusion (GME).

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REFERENCES

[1] AMD. 2019. AMD64 Architecture Programmer’s Manual Volume 3: General Purpose and System Instructions. AMD. https://www.amd.com/system/files/TechDocs/24594.pdf
[2] J. H. Anderson and Y.-J. Kim. 2002. An Improved Lower Bound for the Time Complexity of Mutual Exclusion. Distributed Computing (DC) 15, 4 (Dec. 2002), 221–253. https://doi.org/10.1007/s00446-002-0084-2
[3] A. Arcangeli, M. Cao, P. E. McKenney, and D. Sarma. 2003. Using Read-Copy-Update Techniques for System V IPC in the Linux 2.5 Kernel. In USENIX Annual Technical Conference, FREENIX Track. 297–309.
[4] H. Attiya, D. Hendler, and P. Woelfel. 2008. Tight RMR Lower Bounds for Mutual Exclusion and Other Problems. In Proceedings of the 40th Annual ACM Symposium on Theory of Computing (STOC). ACM, New York, NY, USA, 217–226. https://doi.org/10.1145/1374376.1374410
[5] P. Bohannon, D. Lieuwen, and A. Silberschatz. 1996. Recovering Scalable Spin Locks. In Proceedings of the 7th IEEE Symposium on Parallel and Distributed Processing (SPDP). IEEE Computer Society, Washington, DC, USA, 314–322. http://dl.acm.org/citation.cfm?id=829517.830751
[6] P. Bohannon, D. Lieuwen, A. Silberschatz, S. Sudarshan, and J. Gava. 1995. Recoverable User-level Mutual Exclusion. In Proceedings of the 7th IEEE Symposium on Parallel and Distributed Processing (SPDP). IEEE Computer Society, Washington, DC, USA, 293–301. http://dl.acm.org/citation.cfm?id=829516.830651
[7] D. Chan and P. Woelfel. 2021. A Tight Lower Bound for the RMR Complexity of Recoverable Mutual Exclusion. In Proceedings of the 40th ACM Symposium on Principles of Distributed Computing (PODC). Association for Computing Machinery (ACM).
[8] D. Y. C. Chan and P. Woelfel. 2020. Recoverable Mutual Exclusion with Constant Amortized RMR Complexity from Standard Primitives. In Proceedings of the 39th ACM Symposium on Principles of Distributed Computing (PODC). Association for Computing Machinery (ACM), New York, NY, USA, 10.
[9] E. W. Dijkstra. 1965. Solution of a Problem in Concurrent Programming Control. Communications of the ACM (CACM) 8, 9 (1965), 569.
[10] R. Dviri and G. Taubenfeld. 2017. Mutual Exclusion Algorithms with Constant RMR Complexity and Wait-Free Exit Code. In Proceedings of the 21st International Conference on Principles of Distributed Systems (OPODIS), James Aspnes, Alysson Bessani, Pascal Felber, and João Leitão (Eds.), Vol. 95. Schloss Dagstuhl–Leibniz-Zentrum fuer Informatik, Dagstuhl, Germany, 17:1–17:16. https://doi.org/10.4230/LIPIcs.OPODIS.2017.17
[11] K. Fraser. 2004. Practical Lock-Freedom. Ph.D. Dissertation. University of Cambridge.
[12] W. Golab and D. Hendler. 2017. Recoverable Mutual Exclusion in Sub-Logarithmic Time. In Proceedings of the ACM Symposium on Principles of Distributed Computing (PODC). ACM, New York, NY, USA, 211–220. https://doi.org/10.1145/3087801.3087819
[13] W. Golab and D. Hendler. 2018. Recoverable Mutual Exclusion Under System-Wide Failures. In Proceedings of the ACM Symposium on Principles of Distributed Computing (PODC). ACM, New York, NY, USA, 17–26. https://doi.org/10.1145/3212734.3212755
[14] W. Golab, D. Hendler, and P. Woelfel. 2006. An $O(1)$ RMRs Leader Election Algorithm. In Proceedings of the 25th ACM Symposium on Principles of Distributed Computing (PODC). Association for Computing Machinery (ACM), New York, NY, USA, 238–247. https://doi.org/10.1145/1146381.1146417
[15] W. Golab and A. Ramaraju. 2015. Recoverable Mutual Exclusion: [Extended Abstract]. In Proceedings of the ACM Symposium on Principles of Distributed Computing (PODC). ACM, New York, NY, USA, 65–74. https://doi.org/10.1145/2893057.2893087
[16] W. Golab and A. Ramaraju. 2019. Recoverable Mutual Exclusion. Distributed Computing (DC) 32, 6 (Nov. 2019), 535–564.
[17] T. E. Hart, P. E. McKenney, A. D. Brown, and J. Walpole. 2007. Performance of Memory Reclamation for Lockless Synchronization. Journal of Parallel and Distributed Computing (JPDC) 67, 12 (2007), 1270–1285.
[18] Intel 2016. Intel 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A: Instruction Set Reference, A-M. Intel. https://software.intel.com/sites/default/files/managed/a4/60/325383-sdm-vol-2abcd.pdf

[19] P. Jayanti, S. Jayanti, and A. Joshi. 2019. A Recoverable Mutex Algorithm with Sub-logarithmic RMR on Both CC and DSM. In Proceedings of the ACM Symposium on Principles of Distributed Computing (PODC). ACM, New York, NY, USA, 177–186. https://doi.org/10.1145/3293611.3331634

[20] P. Jayanti and A. Joshi. 2017. Recoverable FCFS Mutual Exclusion with Wait-Free Recovery. In Proceedings of the 31st Symposium on Distributed Computing (DISC), Andréa W. Richa (Ed.), Vol. 91. Schloss Dagstuhl–Leibniz-Zentrum für Informatik, Dagstuhl, Germany, 30:1–30:15. https://doi.org/10.4230/LIPIcs.DISC.2017.30

[21] P. Jayanti and A. Joshi. 2019. Recoverable Mutual Exclusion with Abortability. In Proceedings of the International Conference on Networked Systems (NETYSYS). Springer International Publishing, 217–232.

[22] D. Katzan and A. Morrison. 2021. Recoverable, Abortable, and Adaptive Mutual Exclusion with Sublogarithmic RMR Complexity. In Proceedings of the 24th International Conference on Principles of Distributed Systems (OPODIS) (Leibniz International Proceedings in Informatics (LIPIcs)), Q. Bramas, R. Oshman, and P. Romano (Eds.), Vol. 184. Schloss Dagstuhl–Leibniz-Zentrum für Informatik, Dagstuhl, Germany, 15:1–15:16. https://doi.org/10.4230/LIPIcs.OPODIS.2020.15

[23] P. E. McKenney and J. D. Slingwine. 1998. Read-Copy Update: Using Execution History to Solve Concurrency Problems. In Proceedings of the IASTED International Conference on Parallel and Distributed Computing and Systems. 509–518.

[24] J. M. Mellor-Crummey and M. L. Scott. 1991. Algorithms for Scalable Synchronization on Shared-Memory Multiprocessors. ACM Transactions on Computer Systems 9, 1 (Feb. 1991), 21–65. https://doi.org/10.1145/103727.103729

[25] D. Narayanan and O. Hodson. 2012. Whole-System Persistence. In Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS). ACM, New York, NY, USA, 401–410.

[26] A. Ramaraju. 2015. RGLock: Recoverable Mutual Exclusion for Non-Volatile Main Memory Systems. Master’s thesis. Electrical and Computer Engineering Department, University of Waterloo. http://hdl.handle.net/10012/9473

[27] J.-H. Yang and J. H. Anderson. 1995. A Fast, Scalable Mutual Exclusion Algorithm. Distributed Computing (DC) 9, 1 (March 1995), 51–60. https://doi.org/10.1007/BF01784242

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