Cryogenic data storage technology is of use in superconducting single-flux quantum electronics and quantum computing. However, the lack of compatible cryogenic memory technology, which can operate at temperatures of 4 K (or lower), hinders the development of practical and scalable systems. Here we examine the development of cryogenic memory technologies. We explore three areas of memory technology: cryogenic non-superconducting memories (including those based on charge and resistance), superconducting memories (including those based on Josephson junctions, superconducting quantum interference devices and superconducting memristors) and hybrid memories (which use both superconducting and non-superconducting technologies). We consider the key challenges involved in the integration of such memories with single-flux quantum circuits and quantum computers. We also provide a comparison of the capabilities of the different technologies in the context of the requirements of superconducting electronics and quantum computing.

Silicon-based complementary metal–oxide–semiconductor (CMOS) technology can now be used to accommodate more than one billion transistors on a chip. However, the aggressive device scaling that has led to this has also created considerable challenges related to power dissipation. To circumvent this, numerous beyond-CMOS technologies are being explored, including superconducting single-flux quantum (SFQ) electronics. SFQ circuits and systems are based on superconducting devices such as Josephson junctions (JJs) and superconducting quantum interference devices (SQUIDs), and are generally faster and more energy efficient than their CMOS counterparts due to the dissipationless current flow in superconductors. SFQ circuits—coupled with lossless and low-dispersion interconnects—have, in particular, been shown to improve the performance of several applications including digital radio-frequency receivers and high-end computing. However, the lack of fast, low-power, high-density cryogenic memory that is compatible with the performance of SFQ circuits limits the development of practical and reliable SFQ systems.

Cryogenic memory is also required in the development of quantum computers. Quantum computers could be used to solve commercially and scientifically important problems that classical computers cannot handle in a realistic timeframe. Qubits, the basic computing unit of a quantum computer, need to be placed at cryogenic temperature to avoid the impact of thermal noise. However, although a number of technologies have been used to implement qubits, superconducting qubits are of interest due to their non-dissipative and strongly nonlinear behaviour. To guarantee the required environment for the superconductors, superconducting qubits must be placed at cryogenic temperature. Therefore, to implement a quantum computer with thousands of qubits, a suitable cryogenic memory is required.

In this Review, we explore the development of cryogenic memory technologies. We first consider the benefits of using cryogenic memory in cryogenic electronics and quantum computers. We then examine the different cryogenic memories available—cryogenic non-superconducting memories (including charge-based memories and resistance-based memories), superconducting memories (including superconductor–insulator–superconductor JJ-based, magnetic JJ-based, superconducting memristor-based and ferroelectric SQUID-based memories) and hybrid memories (that use both superconducting and non-superconducting technologies)—and provide a comparison of their capabilities in regards to the requirements of superconducting electronics and quantum computing. We also consider the key challenges involved in the integration of such memories with SFQ circuits and quantum computers.

The need for cryogenic memory
Superconducting electronics could be used to solve the speed and power issues faced by CMOS technology due to the faster and more energy-efficient operation offered by superconducting devices (Fig. 1b).

Received: 31 July 2021
Accepted: 25 January 2023
Published online: 2 March 2023

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However, superconducting devices must be operated in a cryogenic (4 K or below) environment to guarantee a suitable operational environment for the superconductors. Therefore, to implement energy-efficient superconducting electronics, a suitable memory, logic circuits and interconnects operating at cryogenic temperature are required. Among these, the lack of a scalable and compatible 4 K memory is a key challenge and currently restricts the superconducting electronics to niche applications. Existing superconducting processors call for 4 K memories due to the lower power and latency afforded by physical proximity.

A typical quantum computer has three major components: a quantum substrate (qubits), a control processor and a memory block (Fig. 1a). The qubit is the basic unit of quantum information realized with a two-state device. To protect the quantum states of the noise-sensitive qubits, the qubits are placed at a few millikelvin temperature. In current lab-scale quantum computers, a conventional computer at room temperature (300 K) is used as the control processor, and long control cables are required to connect the qubits and the control processor. This architecture works fine for a small number of qubits, but it cannot be scaled to a few hundreds of qubits because it would require a large number of wires to establish a connection between the room-temperature control processor and the qubits at cryogenic temperature. However, a quantum computer needs to be scaled up to, at least, thousands of qubits to be of use. For example, to run Shor’s algorithm for prime factorization on a 1,024-bit number, two quantum registers—one with 2,048 qubits and another with 1,024 qubits—are required.

The control processor should thus be placed at a temperature very close to that of the qubits using the superconducting interconnects. The use of superconducting interconnects here, rather than metal wires, is beneficial because of their dissipationless nature. However, to use superconducting interconnects, the control processor needs to be placed at 4 K or below. This places a restriction on the type of memory that can be used in conjunction with quantum computers: room-temperature memories cannot be used because the interconnects between the room-temperature memory and the cryogenic control processor would have considerable thermal leakage. This leakage stems from the huge temperature difference (about 300 K) between the room temperature and the cryogenic temperature, and leads to thermal noise that is large enough to destroy the quantum states of the qubits. Cryogenic 4 K memory, which is compatible with the superconducting control processor, could be used to circumvent this issue.

Another requirement for the storage device of a quantum computer is high capacity. State-of-the-art quantum algorithms require a large number of arbitrary rotations, which eventually necessitate a large program memory. Furthermore, to preserve the data integrity of the qubit states, the qubits undergo continuous error-correction schemes, and this requires extensive memory and bandwidth.

While 4 K memories should allow scalability of a quantum computer and offer very low thermal leakage, the option of placing...
memories at a temperature higher than the processor temperature has also been explored. This is because the cost of cooling memory systems down to 4 K is around 200 times higher than for room-temperature memory. To reduce cost, memories can also be placed at a higher temperature (such as 77 K) than 4 K, although there is then a small thermal leakage.

A range of device technologies are available that could potentially be used with SFQ circuits and quantum computing, and we categorize state-of-the-art cryogenic memory technologies into three broad categories: cryogenic non-superconducting memories, superconducting memories and hybrid memories (Fig. 1d).

**Cryogenic non-superconducting memories**

Non-superconducting devices are prime candidates for cryogenic memory due to their technological maturity and high storage capacity. It has been shown that CMOS devices and circuits manufactured can operate better at 4 K than at room temperature. However, operating at 4 K entails higher costs. Therefore, operating at a slightly higher temperature can potentially offer an optimized solution.

The temperature levels of a typical cryogenic (dilution) refrigerator are 20 mK, 4 K, 77 K and 120 K (Fig. 1a). A natural choice is to run the CMOS memory operations at 77 K/120 K. This cuts costs down compared with working at 4 K, but can still reduce the leakage current substantially and improve carrier mobility, leading to an enhancement in the driving capability of access transistors and the overall memory operation (Fig. 1c). Importantly, these temperatures are within the ideal operating temperature range for the CMOS devices. However, while this scheme may work for smaller quantum computers, it will most certainly limit the scaling of the quantum computer due to the large number of connections between the 77 K/120 K memory and the 4 K control processor (and the resulting thermal loss). Furthermore, some emerging memories have been reported to show successful operation at 4 K temperature.

We classify the non-superconducting memories into two categories: charge-based and resistance-based.

**Charge-based memories**

In charge-based memories, data are stored in a small capacitor. The capacitor can be either charged or discharged, which provides the two memory states (‘0’ and ‘1’) in the cell. There are two main categories of these CMOS dynamic random-access memories (DRAMs): DRAM with a capacitor (typically known as one-transistor one-capacitor (1T1C) DRAM) and capacitorless DRAM (known as one-transistor (1T) DRAM).

**1T1C DRAM.** 1T1C DRAMs (Fig. 2a) are a strong candidate for cryogenic memory because of their technical maturity, high storage capacity and expected performance improvements at low temperatures due to the reduced junction leakage of cell transistors. Low-operating temperature also reduces the required refresh power and switching energy. In the late 1980s, IBM demonstrated low-temperature operation (85 K). silicon-on-insulator (PDSOI) n-type metal oxide semiconductor field effect transistor (n-MOSFET) with a floating body (Fig. 2d). Memory operations (write ‘0’, write ‘1’, hold and read) were demonstrated by choosing suitable bias conditions for the gate and drain of the transistor. One of the major drawbacks of capacitorless DRAM cells is the possibility of retention failure. The use of low temperature alleviates such failures. Figure 2e shows the temperature dependence of the retention time, \( t_{\text{ret}} \) (during hold operation) and dynamic retention time, \( t_{\text{d,ret}} \) (during read operation), indicating substantial improvement at lower temperatures. For example, 10 times longer dynamic retention times (Figs. 2e) and 2.5 times larger current sense margins (Fig. 2f) have been achieved at 80 K compared with 300 K.

**Resistance-based memories**

Resistance-based memories offer better scalability (down to nanometres), faster speed (nanosecond range switching time), lower power consumption and refresh-free operation compared with charge-based memories. Moreover, resistance-based memories offer non-volatility, which implies better energy efficiency compared with the charge-based DRAMs. In these memory cells, two resistance states (known as high-resistance state (HRS) and low-resistance state (LRS)) define the two memory states (‘0’ and ‘1’). Resistance-based memories include memristive, ferroelectric, spintronic, quantum anomalous Hall effect (QAHE)-based and phase-change-based memories (Fig. 3).

**Memristive memories.** Memristive (resistive) random-access memory (ReRAM)—that is, a metal–insulator–metal device (Fig. 3a)—is a candidate for cryogenic memory due to its subnanosecond switching time, low switching energy (<0.1 pJ per bit), excellent scalability (down to a few nanometres), endurance (10^4 cycles) and CMOS compatibility. The current–voltage characteristics of these devices show a hysteretic response where two distinct resistance states (HRS and LRS) are observed (Fig. 3e). Resistive switching has been observed in numerous material systems, including binary transition-metal oxides (such as 
PdO (ref. 39), TiO2 (ref. 39) and HfO2 (ref. 40), perovskite-type oxides, silicon oxides and single-molecule systems. Among these, HfO2-based ReRAMs show the most promise as a cryogenic memory.

In 2014, the I–V characteristics of a Pt/Al2O3/HfO2/Er/Pt ReRAM device were explored over the temperature range of 40 K to 350 K (ref. 40). It was found that LRS and HRS become more resistive as the temperature is lowered. The device in LRS has a greater dependence on temperature than the one in HRS. Later, memory operation of indium tin oxide (ITO)/HfO2/ITO metal–insulator–metal structure with a large \( R_{\text{off}}/R_{\text{on}} \) ratio, excellent endurance (5 × 10^4 cycles), extrapolated...
memristive (the MTJ resistance ($R_{MTJ}$) versus MTJ current characteristics of magnetic ($g$) and the Hall resistance versus bias current ($I_{bias}$) characteristics of QAHE-based ($h$) memories. The characteristics shown in $e$–$h$ show the HRS and LRS, which define the two memory states. Here, $V_{HRS}$ and $V_{LRS}$ are the threshold voltages for the set and reset operations of the memristor, respectively. $I_c$ represents the compliance current, $I_{bias}$ represents the current corresponding to $V_{HRS}$, and $P$ refers to the remnant polarization and $E_c$ refers to the coercive field of ferroelectric materials. $R_s$ ($R_p$) is the resistance of the MTJ when the magnetization of the free and pinned layers are parallel (antiparallel) to each other. $I_{bias}$ and $I_{bias}$ are the critical current for $P \rightarrow AP$ ($AP \rightarrow P$) switching. $V_{xy}$ represents the Hall voltage and $B$ is the external magnetic field.

Fig. 2 | Cryogenic characterization of non-superconducting charge-based memories. $a$, $b$, Schematics of 1T1C DRAM ($a$) and 3T DRAM ($b$) cells. In ITIC DRAM, the capacitor $C_t$ stores the data whereas in 3T DRAM, the parasitic capacitance $C_b$ stores the data. Also, unlike the ITIC DRAM, 3T DRAM uses separate transistors for read and write operations. $c$, Summary of cryogenic DRAMs over the years along with the effects of cryogenic temperature on different performance metrics. $d$, Schematic of a PDSOI n-MOSFET with floating body as 1T DRAM$^{34}$ that can act as a capacitorless DRAM. Here, $L_e$ represents the gate length, $t_{ox}$, $t_{box}$, and $t_s$ represent the thickness of the oxide layer, buried oxide (BOX) and body channel, respectively. $e$, $f$, Temperature dependence of static retention time, $t_{set}$ and dynamic retention time, $t_{d,ret}$ ($e$) and current sense margin, $\Delta I_c$ ($f$). At lower temperature, the retention time and sense margin substantially improve.

Fig. 3 | Non-superconducting resistance-based memories. $a$–$d$, Schematic structures of ReRAM ($a$), ferroelectric ($b$), spintronic ($c$) and QAHE-based ($d$) memory devices. $e$–$h$, Signature hysteresis in the $I$–$V$ characteristics of memristive ($e$), the polarization–electric field characteristics of ferroelectric ($f$), the MTJ resistance ($R_{MTJ}$) versus MTJ current characteristics of magnetic ($g$) and the Hall resistance versus bias current ($I_{bias}$) characteristics of QAHE-based ($h$) memories. The characteristics shown in $e$–$h$ show the HRS and LRS, which define the two memory states. Here, $V_{HRS}$ and $V_{LRS}$ are the threshold voltages for the set and reset operations of the memristor, respectively. $I_c$ represents the compliance current, $I_{bias}$ represents the current corresponding to $V_{HRS}$, and $P$ refers to the remnant polarization and $E_c$ refers to the coercive field of ferroelectric materials. $R_s$ ($R_p$) is the resistance of the MTJ when the magnetization of the free and pinned layers are parallel (antiparallel) to each other. $I_{bias}$ and $I_{bias}$ are the critical current for $P \rightarrow AP$ ($AP \rightarrow P$) switching. $V_{xy}$ represents the Hall voltage and $B$ is the external magnetic field.

retention ability (over $10^8$ s) and a wide working temperature range of 10 K to 490 K was demonstrated$^{46}$. Here, the ON-state resistance ($R_{ON}$) decreases and the OFF-state resistance ($R_{OFF}$) increases with the lowering of the temperature and therefore $R_{OFF}/R_{ON}$ improves at lower temperatures. However, this comes with the cost of larger set/reset voltages, which increases the power requirement.
In 2015, resistive switching of Pt/HfO$_x$/TiN devices at ultralow temperatures (4 K and 77 K) was demonstrated$^{47}$. Here, the resistances in both LRS and HRS increase with the lowering of the temperature. This structure was subsequently improved and found that TiN/Ti/HfO$_x$/TiN devices can operate between 4 K and 300 K (ref. $^{48}$). Here, the resistive switching showed no notable change at lower temperatures. Considering the demonstration of proper switching between LRS and HRS in HfO$_x$-based ReRAM devices at low and ultralow temperatures, these ReRAM devices should be further explored as a potential cryogenic memory.

**Ferroelectric memories.** Ferroelectric memories are among the most promising candidate devices available. They are two major types: ferroelectric capacitor (FeCap)-based ITIC memory and ferroelectric field-effect transistor (FeFET)-based IT memory. The construction of FeCap memories is similar to ReRAMs—the only difference is that a ferroelectric layer is used instead of a dielectric/insulating layer (Fig. 3b), which provides the non-volatility. The signature of the FeCap is the hysteretic polarization versus electric field curve (Fig. 3f). The advantages of FeCap memories include fast speed (nanosecond range switching time), large endurance (about 10$^{9}$ to 10$^{10}$ cycles) and retention time of more than 10 years$^{49}$. However, destructive read operation is a major issue for FeCap memories.

FeFET memories avoid the destructive read by providing separate read/write paths along with fast (around nanosecond) program/erase time$^{50}$. Therefore, the properties of the ferroelectric materials (an integral part of FeFET) have been extensively studied over the past few decades down to the millikelvin temperature range$^{32}$. Recently, the cryogenic characteristics of an n-type FeFET containing a silicon-doped hafnium oxide (Si:HfO$_x$) as a ferroelectric layer was studied down to 6.9 K (ref. 5). This showed that the lowering in temperature leads to an increase in the memory window with the cost of an increase in the program/erase voltage.

To explore the feasibility of realizing cryogenic FeCap and FeFET memories, several ferroelectric materials have been characterized at low temperature. This includes SrTiO$_3$, oxygen-18 substituted SrTiO$_3$ and KTaO$_3$ up to 50 K (ref. 5). PbZr$_{0.5}$Ti$_{0.5}$O$_3$ thin films up to 4 K (ref. 5) and antiferroelectric zirconium dioxide up to 50 mK (ref. 5). The lowering of temperature, the coercive field increased for PbZr$_{0.5}$Ti$_{0.5}$O$_3$ thin films and decreased for antiferroelectric zirconium dioxide. For PbZr$_{0.5}$Ti$_{0.5}$O$_3$ thin films, the both the saturation and remnant polarizations kept increasing at low temperatures. These studies indicate the necessity of design trade-offs in ferroelectric memories at cryogenic temperature.

**Spintronic memories.** Spintronic memories (magnetic random-access memories (MRAMs)) have the potential to outperform CMOS charge-based memories due to their non-volatile nature, high density, fast speed (switching time of less than 1 ns) and low-power operation, high endurance (more than 10$^{10}$ cycles), and long retention time (around 10 years)$^{33}$. The basic building block of MRAMs is a magnetic tunnel junction (MTJ), consisting of two ferromagnetic materials (free layer and pinned layer) separated by a thin insulating layer (barrier oxide) (Fig. 3c). For parallel and anti-parallel magnetization in the free layer and pinned layer, two levels of magnetoresistance are observed in the MTJ, which are used to define the memory states (Fig. 3g).

Different spintronic memory devices$^{52–54}$ have been explored at cryogenic conditions to use in cryogenic MRAMs. A functioning CoFeB/MgO-based MTJ device with perpendiccular magnetic anisotropy at 9 K has been demonstrated$^{55}$, which offered reliable and low error rate (<10$^{-4}$) switching. With the lowering of temperature to 9 K, the endurance (over 10$^{10}$ cycles) also improved by around three orders of magnitude. A CoFeB-based orthogonal spin-transfer device has also been studied at 4 K as a cryogenic memory element$^{56}$. This work reported high-speed switching (around 200 ps) and lower error rate (as low as 10$^{-5}$) compared with room-temperature operations. However, the device achieved such low write error rate only for a limited pulse condition and provided low magnetoresistance. In 2017, a toggle MRAM at 4.2 K was characterized for implementing a hybrid JJ-MRAM memory system$^{57}$. Along with the successful operation of the toggle MRAM, this work reported an enhanced magnetoresistance at 4.2 K, which improved the signal-to-noise ratio of the memory system.

**Other resistance-based memories.** Along with the traditional resistance-based memories, exotic quantum phenomena can be leveraged to construct cryogenic memories. For example, a cryogenic non-volatile memory has been proposed based on the QAHE$^{62}$. The QAHE is the precise quantization of Hall resistance at ±$e^2/h$ (where $h$ is Planck’s constant and $e$ is the charge of an electron) without an external magnetic field. QAHE-based memory uses these quantized Hall resistance states (±$e^2/h$) observed in a twisted bilayer graphene moiré heterostructure$^{63}$ to define the memory states (Fig. 3d, h). This design allows the memory cell to be written and read by applying nanosquare-level bias currents, which should make the design attractive as an ultralow-power and highly scalable cryogenic memory.

Phase-change random-access memory (PCRAM) is another emerging non-volatile memory. PCRAMs have been explored for storage applications because of their non-volatility, fast speed and scalability$^{59}$. They use two phases of chalcogenide materials: the amorphous phase provides an HRS and the crystalline phase provides an LRS. A unique hysteretic behavior in resistance as a function of the electric field emerges in (La, Pr, Ca)MnO$_3$, up to 10 K (ref. 60). These stable resistive states can be switched repeatedly with the application of various voltage pulses and hence the behaviours can be used to implement a fast, non-volatile and scalable cryogenic phase-change memory.

Table 1 summarizes reports on resistance-based cryogenic memories.

**Superconducting memories.** J and SQUID-based SFQ technology has emerged as a promising platform to design the control processor for quantum computers. SFQ processors can operate at ultralow temperature (4 K) with high speed (close to terahertz) and low switching energy (0.1–1 aJ). Although non-superconducting memories can offer excellent scalability, they have higher power demand and provide lower speed compared with superconducting SFQ circuits and systems. Therefore, superconducting memory is an obvious choice for cryogenic applications. However, superconductor–insulator–superconductor (SIS) JJ and SQUID-based memories offer unreasonably low storage capacity due to the large cell area (a few hundreds of square micrometres), transformer-based coupling with address lines and flux trapping$^{61}$. The trapped fluxes affect the superconducting circuits in two ways: they can penetrate JJs or can couple with magneto-sensitive gates$^{62}$. The first step to prevent flux trapping is to shield Earth’s magnetic field, although this cannot solve the problem completely. Therefore, it is necessary to keep some space on the superconducting chips so that frozen vortices remain far from the magneto-sensitive portions of the chips$^{63}$. Most JJ-based memories use address lines coupled with transformers, which are magneto-sensitive. Therefore, this flux trapping imposes a limitation on the integration density of JJ and SQUID-based memories.

Besides the storage capacity, energy efficiency at large scale is an issue$^{64}$. It has been shown the available superconducting memories consume too much power and therefore cannot be used as memory at 4 K (ref. 65).
The fabrication of scaled JJs is a major step towards implementing high-density SFQ memories83. A fabrication process that can yield circuits with over $7 \times 10^4$ JJs on a 5 x 5 mm$^2$ chip has, for instance, been developed84. The ongoing development of fabrication technology for JJs may lead to scalable JJ-based memory.

Three alternative technologies are magnetic JJ (MJJ) memories, superconducting memristor-based memories and ferroelectric SQUID-based memories, which have the potential to offer high capacity, speed and energy efficiency, while being capable of integration on a single chip with SIS JJs. These traits result in a fast operation, even at a similar clock speed to the fast SFQ control processor and SFQ digital circuits. We thus examine superconducting memories in four areas: SIS JJ-based, MJJ-based, superconducting memristor-based and ferroelectric SQUID-based memories.

**SIS JJ-based memories**

SIS JJ-based cryogenic memory design has garnered considerable research attention over the past few decades (Fig. 4a)74-80. Despite this effort, the designs suffer from low capacity and so far only 4 kbit memory has been demonstrated experimentally74.

A non-destructive readout Josephson vortex transition (VT) memory cell was demonstrated in 198975. The memory cell consisted of two superconducting loops (contains Nb/AIO/Nb JJs and inductors) and a two-junction interferometer gate as a sense gate (Fig. 4b). In loop 1 and loop 2 (Fig. 4b), resistors are connected in parallel to JJs (J1 and J2) to ensure suitable damping conditions for the junctions. In this design, loop 1 stores the information in the form of an SFQ pulse, and the stored data are read by the switching of the sense gate caused by the vortex transition75 in loop 2, which again depends on the stored SFQ pulse in loop 1.

In a later work, two 4 kbit RAMs, composed of $64 \times 64$ (ref. 68) and $256 \times 16$ (ref. 75) VT memory cells, were demonstrated. The VT memory cell was then modified later and used to create a pipeline structure to design a d.c.-powered RAM71. To control the modified VT memory cell with d.c. signals, a two-junction SQUID gate was used as the write gate and a control line was magnetically coupled to loop 1. Subsequently, the VT memory cell was improved by reducing the number of Nb layers from three to two72. Using this improved design, a 16 kbit RAM comprising four blocks (4 kbit each) was created73. A pipelined d.c.-powered RAM was developed74 (Fig. 4d)77. The designed memory cell consists of single-junction Nb/AIO/Nb JJs and inductors like the VT memory cell, has also been developed85 and used to implement a 2 kbit RAM86. This design uses three sense gates (unlike just one in VT memory cells) to solve the ‘half select’ problem of SIS JJ-based memories.

In 1995, an alternative design concept for the JJ-based RAM was proposed (Fig. 4d)77. The designed memory cell consists of single-junction SQUIDs that are serially connected to the bit lines and coupled inductively to the word lines. Write and read operations are performed by sending pulses in appropriate directions into bit lines and d.c. pulses with appropriate polarity along word lines.

More recently, a different design for SIS JJ-based memory cell was developed85-87 (Fig. 4e) and experimentally demonstrated87. The memory cell consists of three inductively coupled SIS JJs and offers three memory states. Write operations are performed by applying SFQ pulses into appropriate junctions and read operation is performed using one of the write mechanisms. However, based on the mechanism used to sense the stored data, one of the read operations (I/U) will be destructive (half-destructive read). However, non-destructive readout can be achieved with the same design and same readout technique. This involves sending a weaker read pulse compared to the ones sent during the write operations85-87.

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**Table 1 | Resistance-based cryogenic memories**

| Type of memory | Material system | Temperature range | Effects of lower temperature (compared with 300 K) |
|----------------|-----------------|------------------|-------------------------------------------------|
| Memristive     | Pt/AIO$_2$/HFO$_2$/Er/Pt (ref. 65) | 40–3 K | - $R_{ON}$: 5.5x; $R_{OFF}$: 0.75x; $R_{ON}/R_{OFF}$: 0.3x |
| ITO/HFO$_2$/ITO (ref. 66) | 10–490 K | - $R_{ON}$: 0.75x; $R_{OFF}$: 2.65x; $R_{ON}/R_{OFF}$: 3.5x; Excellent endurance (5 x 10$^4$ cycles); Long retention time (over 10$^9$s) |
| Pt/HFO$_2$/TiN (ref. 67) | 4–77 K | - $R_{ON}$: 2.5x; $R_{OFF}$: 2x; $R_{ON}/R_{OFF}$: 0.8x; Set voltage: 1.32x; Reset voltage: 1.08x |
| TiN/Ti/HFO$_2$/TiN (ref. 68) | 4–300 K | - $R_{ON}$ decreases with the lowering of temperature |
| Ferroelectric  | PbZr$_{0.5}$Ti$_{0.5}$O$_3$ thin films55 | Down to 4 K | - Saturation polarization: 1.04x; remnant polarization: 1.24x; coercive field: 3.7x |
| Antiferroelectric zirconium dioxide | Down to 50 mK | - Lower critical field (in polarization–electric field curve); High endurance (over 10$^7$ cycles) |
| Si:HFO$_2$-based FeFET67 | Down to 6.9 K | - Memory window: 1.7x; Forward subthreshold slope: 0.15x; Increased program/erase voltage |
| Spintronic     | CoFeB/MgO-based perpendicular MTJ58 | Down to 9 K | - 1.7x magnetoresistance; 33–93% larger switching voltage; 1,000+ endurance (10$^7$ cycles); Reliable error rate (<10$^{-5}$) |
| CoFeB-based orthogonal spin transfer device59 | Down to 4 K | - Suppressed magnetoresistance; High speed (~200 ps); Low error rate (10$^{-5}$) |
| Toggle MRAM60 | Down to 4.2 K | - 1.5x magnetoresistance; Improved signal-to-noise ratio |
| QAHE-based Twisted bilayer graphene moire heterostructure61 | Down to 2 K | - Does not work above 9 K; Hall resistance states become more robust at lower temperature; Ultralow-power switching; Topologically protected Hall resistance states |
| PCRAM         | Perovskite (La, Pr, Ca)MnO$_3$ (ref. 65) | Down to 2 K | - High distinguishability (10$^3$) between two phase resistances |
Cell area, speed, storage capacity and energy efficiency are the major performance metrics for cryogenic memories. Figure 4f,g and compares the cell area, access time, capacity and power consumption for notable SIS JJ-based memories. Ultrahigh-speed and low power consumption are attractive features, but scalability is a major concern for these memories. A more detailed analysis of this memory technology is available in refs. 90,91.

**Magnetic JJ-based memories**

An SIS JJ is the main building block of superconducting electronics and the control processor of superconducting qubit-based quantum computers. Therefore, a memory that is compatible with the speed, power and fabrication method of SIS JJs should be a strong candidate for cryogenic memory applications. However, SIS JJ-based memories suffer from low capacity. In the 1990s, the idea of combining ferromagnetic and superconducting materials to develop a high-capacity cryogenic memory was explored as an alternative to SIS JJ-based memories 92.

An MJJ is a version of Josephson junction, built by sandwiching a ferromagnetic layer between two superconducting materials (Fig. 5a). An MJJ and an SIS JJ have the same fabrication process and hence MJJs can be integrated on a single chip with SIS JJs93. The most important advantage of MJJs is their ability to be in a Josephson state with the inversion of phase difference, which is known as a π state94,95. The incorporation of the ferromagnetic layer in the Josephson junction

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**Fig. 4 | JJ-based superconducting memories.**

*a* Evolution of SIS JJ-based memories over the past few decades. **b–e**, Schematics of a Josephson vortex transition memory cell67 (**b**), a buffered Josephson memory cell75 (**c**), a single JJ SQUID-based memory cell77 (**d**) and a three inductively coupled SIS JJ-based memory cell85,87 (**e**). Here, $I_x$, $I_y$, $I_d$, $I_s$, $I_e$, $I_b$, $I_w$ and $I_n$ are the applied bias currents. WE (RE) is the enable signal for write (read) operation. The components marked by L, M, R and J are the inductors, mutual inductance, resistors and JJs, respectively. Q represents the superconducting loop. **f, g**, Comparison of SIS JJ-based memories based on cell area and access time (**f**) and cell area and power dissipation (**g**). CRAM, cryogenic RAM.
suitable current (with zero external magnetic field, $H$) of two JJs have the same critical current but different conductance. Superconducting and non-superconducting states of the device. The application of an external magnetic flux ($\Phi$) to the MJJ can lead to superconducting and non-superconducting states of the device. An MJJ-based memory with fast and energy-efficient SFQ switch-based superconducting memories.

**a**. Schematic of SFS, SIFS and SIS(J) junctions. Incorporation of additional insulating and superconducting layers to the SFS structure improves the switching speed. **b**. Hysteric dependence of critical current $I_c$ on magnetic field $H$.

An MJJ-based memory with fast and energy-efficient SFQ switching readout was proposed in 2012\(^\text{122}\), where the ability of a superconductor–ferromagnet–superconductor (SFS) JJ ($\text{Nb}/\text{Pd}_0\_8\_\text{Fe}_{0\_0}/\text{Nb}$) to operate as a Josephson magnetic switch was demonstrated. The hysteretic behaviour of $I_c$ on the external magnetic field was observed in the memory design. A similar hysteretic behaviour has been observed in SFS JJs with both strong and weak ferromagnets\(^\text{160–169}\). The speed of an MJJ-based memory cell depends on the inductance of the control current line and the intrinsic switching time ($\tau_j$) of the corresponding SFS junction, $\tau_j$ is given by\(^\text{160}\):

$$\tau_j = \frac{\Phi_0}{2\pi I_c R_N}.$$  \hspace{1cm} (1)

where $\Phi_0$ is the single-flux quantum and $R_N$ is the normal resistance of the junction\(^\text{160}\).

SFS JJs provide a low junction characteristic voltage $V_c (= I_c R_N)$ (on the order of nanovolts)\(^\text{160}\). It limits the switching time to around 100 ns, which is not compatible with the speed of the SIS JJs. To increase $V_c$, an additional insulator layer in the SFS Josephson junction has been inserted (Fig. **5a**\(^\text{99}\)). A superconductor–insulator–ferromagnetic-superconductor (SIFS) MJJ ($\text{Nb}/\text{AlO}_x/\text{Pd}_{0\_0}/\text{Fe}_{0\_0}/\text{Nb}$) with a higher $V_c$ has also been shown. This design retains the magnetic memory properties. Both weak and strong ferromagnets have also been
used to design SIFS MJJs. The characteristic voltage had been further increased by inserting an additional superconducting layer (SIS/SFS JJ)\(^{101-103}\). Using an SIS/SIFS JJ (Fig. 5a), a maximum \(V_c\) of around 700 \(\mu\)V (which implies around 200 GHz switching) has been obtained\(^ {104}\).

Besides the MJJs with one ferromagnetic layer, multiple ferromagnetic layers have been used (S/F/F/.../S). These MJJs are commonly known as spin-valve JJs. Such MJJs allow tuning of the ground-state phase difference and critical current by the mutual orientation of the ferromagnetic layers\(^ {94-100}\). A spin-valve JJ-based cryogenic memory was demonstrated in 2004\(^ {110}\). Similar spin-valve JJs have since been demonstrated with several ferromagnetic materials and alloys, including CuNi (ref. \(^ {109}\)), PdNi (ref. \(^ {111}\)), PdFe (refs. \(^ {99,102}\)), Fe (ref. \(^ {98}\)), Co (ref. \(^ {99}\)), NiFe (refs. \(^ {113,114}\)), NiFeNb (ref. \(^ {115}\)), NiFeMo (ref. \(^ {97}\)) and NiFeCo (ref. \(^ {113}\)).

Quantized Abrikosov vortex memory is another example of MJJ-based memory, which has been created using two different architectures; Josephson spin-valve structures and planar JJs\(^ {112}\). Two resistance states (HRS and LRS) are observed in these memory cells depending on the presence and absence of the Abrikosov vortex\(^ {111}\). The vortex can be introduced (removed) by applying a positive (negative) current of around 20 \(\mu\)A. These memory cells demand an extremely low write energy (on the order of attojoules), offer non-volatility (due to the quantized nature of the Abrikosov vortex) and can be scaled to nanometre size. However, the challenge is that the required magnetic field becomes substantially high (around 1 kOe) for smaller structures\(^ {111}\).

Finding a suitable ferromagnetic material for MJJs is challenging because strong and weak ferromagnets used in MJJs suffer from short characteristic length and severe depression of critical current, respectively. Weak ferromagnets have two key advantages over strong ferromagnetic materials. First, weak ferromagnets require less switching energy. Stoner–Wohlfarth theory\(^ {104}\) predicts that the switching field required by a single-domain nanomagnet is proportional to the magnetization, and the switching energy is proportional to the square of its magnetization. Therefore, lower magnetization implies lower switching energy. Second, strong ferromagnets have a short characteristic length scale \(\xi\); exceeding this length will lead to oscillatory switching between 0/π-type JJs\(^ {90,96}\). Strong ferromagnetic materials (such as Co or Fe) typically exhibit \(\xi < 1 \text{ nm}\) (ref. \(^ {97}\)), which implies that the junction properties will fluctuate even if the average thickness of the ferromagnetic layer changes by a fraction of the atomic monolayer. Weak ferromagnets instead show much larger \(\xi\), which makes it easier to control the thickness of the ferromagnets and, hence, junction properties show a smaller sample-to-sample variations\(^ {90,96}\). Despite these advantages, weak ferromagnets are not yet prominent in spin-valve JJ-based memory, as they lead to a drastic reduction in critical current\(^ {94}\). Low critical current in MJJs will lead to a smaller hysteresis window in the JJ-based memory, as they lead to a drastic reduction in critical current\(^ {94}\). Weak ferromagnets are typically used instead of strong ferromagnets (Co, Fe, Ni) in MJJs, which have a smaller sample-to-sample variations\(^ {90,96}\).

Superconducting memristor-based memories

One of the most recent designs of cryogenic memory uses a superconducting memristor\(^ {118}\) as the storage element. The superconducting memristor can be created using a conductance asymmetric SQUID (CA-SQUID), harnessing the phase-dependent conductance of JJs (Fig. 5d). The superconducting memristor exhibits a pinned hysteresis loop in its \(I-V\) characteristics (reminiscent of an ideal memristor), and combines the scalability of classical memristors with the ultrafast speed and high energy efficiency of JJs\(^ {118,119}\). Traditionally, the two JJs in a CA-SQUID are designed with two different superconducting electrodes to ensure same critical current and asymmetric conductance.

The dynamics of a CA-SQUID can be explained with the modified resistively and capacitively shunted junction model\(^ {110,122}\) with four shunt paths: the Josephson inductance to capture the supercurrent\(^ {112}\), a constant resistance \(R_s\) to capture the single-electron tunnelling\(^ {121}\), a capacitance \(C\) due to the junction capacitance and a dissipative current path due to the phase-dependent conductance of the JJ. With a suitable flux bias \((\Phi_{\text{bias}} - \Phi_c)/2\), the effect of critical current can be suppressed while maintaining the asymmetric conductance; this leads to the pinned hysteresis loop in the \(I-V\) characteristics of the CA-SQUID (Fig. 5e)\(^ {118}\). The two resistance states of the CA-SQUID are used to define the memory states (Fig. 5f).

Array-level implementations of a CA-SQUID are on the horizon. Recently, for instance, a cryogenic memory array design was developed\(^ {120}\), which uses a superconducting memristor-based memory cell and heater cryotron \(h\text{Tron}\)\(^ {121}\)-based access device.

**Ferroelectric SQUID-based memories**

A ferroelectric SQUID (FeSQUID) is a hybrid superconductor–ferroelectric device in which a SQUID containing two parallel weak links is fabricated on top of a ferroelectric substrate (Fig. 5g)\(^ {125}\). The ferroelectric layer has a switchable polarization that can be controlled by a voltage bias (Fig. 5h). The ferroelectric material can show two voltage-controlled non-volatile polarization states \((P^+\text{ and } P^-)\). These two states can be used to define the two memory states \((0\text{ and } 1\text{, respectively})\). Therefore, the write operation of this type of memory is voltage-based.

The polarization state of the ferroelectric material determines the bound charge in the ferroelectric, which eventually controls the superconductor charge density and related parameters. One of the most important parameters of the SQUID on top of the ferroelectric substrate that changes based on the polarization is the critical temperature. As the critical temperature consequently affects the critical current of the SQUID, \(P^+\text{ and } P^-\) polarization states result in two distinct levels of critical current \((I_{\text{c,high}}\text{ and } I_{\text{c,low}})\). Negative polarization state \((P^-\text{ leads to higher critical current than the positive polarization state})\ (P^+\text{).}) (Fig. 5i).

For read operation, a suitable bias current \((I_{\text{bias}}\text{ can be applied to the FeSQUID to invoke superconducting/non-superconducting behaviour based on the stored memory states. For }|I_{\text{c,low}}| < |I_{\text{bias}}| < |I_{\text{c,high}}|\) (Fig. 5i), FeSQUID shows superconducting (0 V) behaviour for the \(P^+\text{ state and non-superconducting behaviour (non-zero voltage) for the } P^-\text{ polarization state. The difference in the voltage across the FeSQUID device based on the polarization state during read operation can be used for the sensing mechanism. FeSQUID-based memory combines the advantages of the superconducting devices (such as high speed and low power consumption) with the advantages of the ferroelectric materials (such as non-volatility, scalability, voltage-based control and separate read–write paths). A cryogenic memory array has been designed for FeSQUIDs where } h\text{Tron has been used as the access device)}\(^ {122}\).

**Hybrid memories**

Conventional non-superconducting memories provide excellent scalability, but suffer from lower speed and higher power demand compared with JJ-based control processors. SIS JJ-based superconducting memories, however, suffer from very low capacity\(^ {90,92}\). To combine the advantages of these two technologies, hybrid memories have been proposed. The hybrid design is a promising approach to develop high-speed, energy-efficient and high-capacity cryogenic memories\(^ {121}\). In this approach, highly scalable memories (such as static RAMs, DRAMs, MRAMs and so on) are used as the storage element, and JJ-based superconductive devices are used to access them (Fig. 6a).
Ghoshal et al.\textsuperscript{127} put forward this concept and some simulations and measurements were reported in their subsequent studies\textsuperscript{128-131} to verify the feasibility of the idea. This approach was first explored using 3T DRAMs as the storage element and used to demonstrate a 64 kb (256 × 256) hybrid memory system (Fig. 6b)\textsuperscript{128-131}. A similar hybrid memory system was also designed (for operation at 4 K) using CMOS static RAM as the memory cell\textsuperscript{132}. Moreover, instead of using only JJs to design the access circuit for JJ–CMOS hybrid memories, three-terminal nanocryotron have been used for CMOS/DRAM memory systems\textsuperscript{133}. Integration of MRAMs with Josephson junctions is another way to develop a hybrid cryogenic memory (Josephson–MRAM memory)\textsuperscript{134}. To start, the operation of MTJ devices at 4.2 K was examined\textsuperscript{135}, demonstrating successful switching operations. Spin Hall effect (SHE)-based MTJ devices\textsuperscript{136} have also been explored for cryogenic memory\textsuperscript{137}. An energy-efficient (6 pJ per switching operation) 4 × 4 array was demonstrated\textsuperscript{138} using an SHE MTJ and an hTTRON. The memory cells in the array were accessed with 100 μA current signals, which makes the design compatible with SFQ control circuits.

In the hybrid memories mentioned above, two technologies are placed at the same temperature. However, a hybrid cryogenic memory system in which two technologies are placed at different temperatures has also been explored\textsuperscript{139}. This approach integrates a high-density semiconductor memory at room temperature and a high-speed 4.2 K rapid single-flux quantum (RSFQ) cache that is integrated on a chip with an RSFQ processor. The approach is not suitable for large-scale quantum computers due to the interconnection between the room-temperature memory and the cryogenic cache. Nevertheless, it is suitable for digital radio-frequency receivers due to the high capacity of semiconductor memory and the fast readout ability of superconductive devices.

**Comparison of cryogenic memories**

Non-superconducting memories—including CMOS DRAM, memristive memory, spintronic memory and ferroelectric memory—are relatively mature compared with the other memory technologies. And it may take a long time for the emerging superconducting memories to catch up. All the non-superconducting memories offer better scalability compared with the superconducting memories. Most of the conventional memories also exhibit successful operation (even with performance improvement in some cases) at 4 K, implying that these memories are suitable for integration with the superconducting control processor in terms of operating temperature. However, 4 K non-superconducting memories suffer from low-speed and high-power issues compared with the fast and energy-efficient superconducting SFQ circuits, systems and processors. Therefore, non-superconducting memories will require a CMOS-based control processor because they cannot operate at the same speed and the same power budget as the SFQ circuits\textsuperscript{131}. Moreover, the non-superconducting CMOS devices consume high power at large scale, which cannot be sustained at 4 K.

SIS JJ and SQUID-based emerging superconducting memories are attractive due to their 4 K operations and excellent compatibility with the control processor in terms of operating temperature, speed and power. An important remaining challenge is the implementation of a high-capacity memory system for quantum computers and other applications. To solve the scalability issue, MJJ-based memory and hybrid variants are promising. However, both options have their own challenges. MJJ-based memories offer compatibility with the SIS JJ-based SFQ circuits, systems and processors on integration in the same chip, operating temperature, speed and power. But a suitable ferromagnetic material is yet to be found, partly because they suffer from fluctuations arising from the ferromagnetic layer thickness and the severe depression of the critical current. Also, the array design for MJJ-based memories is challenging.

The hybrid approach could be used to solve the issues faced by non-superconducting memories and emerging superconducting technology. It combines the best features of both the technologies, such as the maturity and high capacity of the non-superconducting memories and the fast and energy-efficient operation of the superconducting circuits. Since 4 K operation of the conventional non-superconducting memory has been reported, the only remaining challenge is to find a suitable electrical interface between the non-superconducting and superconducting devices. The interface circuits are mainly cryogenic amplifier circuits, which amplify millivolt signals of Josephson circuits to volt-level signals required for CMOS circuits. Superconducting amplifiers\textsuperscript{132}, semiconducting amplifiers\textsuperscript{133} and hybrid superconductor–semiconductor amplifiers\textsuperscript{134} are being explored for use in Josephson–CMOS interface circuits. Designing these interfaces is challenging and requires further research. To start, their speed and energy demand must not impose any additional bottlenecks. (It is worth noting here that unlike other hybrid approaches, the memory based on the SHE...
MTJ and hTron\textsuperscript{13} does not require such an interface circuit.) As long as the scalability issue of superconducting memories persists, hybrid memories may be the most feasible and compatible option for cryogenic applications.

**Outlook**
Quantum computers and superconducting SFQ circuits and systems could address the limitations and challenges of classical computers and CMOS electronics. However, the lack of a compatible cryogenic memory system currently limits them to niche applications. Cryogenic versions of non-superconducting memories offer a large capacity, but suffer from speed and power compatibility issues with the SFQ control processor. Conversely, JJ-based emerging memories are compatible with the control processor and SFQ circuits, but they lack scalability due to their larger size and the requirement of inductive coupling. Hybrid memories can combine the advantages of superconducting and non-superconducting technologies. However, the design of suitable interface circuits remains a challenge. Moreover, for a reliable superconducting and hybrid memory, the operating temperature must be kept way below the critical temperature of the superconducting material. How the fluctuation in the operating temperature affects the reliability of the superconducting and hybrid memory systems has also not yet been explored. The development of cryogenic memory technologies thus demands extensive future research that leverages novel materials, devices and architectures.

**Data availability**
The data that support the plots within this paper are available from the corresponding author on reasonable request.

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Author contributions
All authors conceived the idea of this Review. S.A. performed the literature analysis and collected data. All authors took part in writing the paper, discussed the data and contributed to the final paper. A.A. supervised the project.

Competing interests
The authors declare no competing interests.

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Peer review information Nature Electronics thanks Swamit Tannu and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

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