Locally Rewritable Codes for Resistive Memories

Yongjune Kim*, Abhishek A. Sharma*, Robert Mateescu†, Seung-Hwan Song†, Zvonimir Z. Bandic†, James A. Bain*, and B. V. K. Vijaya Kumar*

*Data Storage Systems Center (DSSC), Carnegie Mellon University, Pittsburgh, PA, USA
†HGST Research, San Jose, CA, USA

Email: {yongjunekim, abhisheksharma}@cmu.edu, {jbain, kumar}@ece.cmu.edu
Email: {robert.mateescu, seung-hwan.song, zvonimir.bandic}@hgst.com

Abstract—We propose locally rewritable codes (LWC) for resistive memories inspired by locally repairable codes (LRC) for distributed storage systems. Small values of repair locality of LRC enable fast repair of a single failed node since the lost data in the failed node can be recovered by accessing only a small fraction of other nodes. By using rewriting locality, LWC can improve endurance limit and power consumption which are major challenges for resistive memories. We point out the duality between LRC and LWC, which indicates that existing construction methods of LRC can be applied to construct LWC.

I. INTRODUCTION

In the big data era, coding for storage systems has become more important than before. Recently, coding for distributed storage systems has become an attractive research area at the (higher) system level. In addition, coding for nonvolatile memories and hard disk drives (HDD) is also important to achieve high-density storage systems at the (lower) physical level.

An important group of codes for distributed storage systems is locally repairable (or recoverable) codes (LRC) [1], [2]. An \((n, k, d, r)\) LRC is a code of length \(n\) with information (message) length \(k\), minimum distance \(d\), and repair locality \(r\). If a symbol in the LRC-coded data is lost due to a node failure, its value can be repaired (i.e., reconstructed) by accessing at most \(r\) other symbols [2], [3].

One way to ensure fast repair is to use low repair locality such that \(r \ll k\) at the cost of minimum distance \(d\). The relation between \(d\) and \(r\) is given by [2]

\[
d \leq n - k - \left\lfloor \frac{k}{r} \right\rfloor + 2. \tag{1}
\]

It is worth mentioning that this bound is a generalization of the Singleton bound. The LRC achieving this bound with equality are called optimal. Constructions of the optimal LRC were proposed in [4]–[5]. Recently, several binary LRC constructions have been proposed [6]–[10].

At the lower (physical) level, coding for nonvolatile memories is an active research area since nonvolatile memories including flash memories and resistive memories are important parts of mobile devices and solid state drives (SSD).

In this paper, we investigate coding for resistive memories including phase change memories (PCM) and resistive random-access memories (RRAM). Resistive memory technologies are promising since they are expected to offer higher density than dynamic random-access memories (DRAM) and better speed performance than NAND flash memories [11].

The major challenges of resistive memories are endurance limit and power consumption [12], [13]. Endurance limit refers to the maximum number of writings that the memory can endure. In order to improve endurance and power consumption of such memories, we propose locally rewritable codes (LWC) [1]. Inspired by the repair locality defined for distributed storage systems, we introduce the rewriting locality which improves power consumption and endurance limit. In addition, we show the duality between LRC and LWC, which indicates that existing construction methods of LRC can be used to construct LWC.

The rest of this paper is organized as follows. Section II explains the basics and challenges of resistive memories. Section III presents the notation and the defect channel model for resistive memories. In Section IV we propose LWC and explain the duality of LRC and LWC. In Section V we will discuss the future work and conclude the paper.

II. RESISTIVE MEMORIES

PCM and RRAM are two major types of resistive memories. Both have attracted significant research interest due to their scalability, compactness, and simplicity. The main challenges that prevent their large-scale deployment are endurance limit and power consumption [12], [13]. The endurance limit refers to the maximum number of writes before the memory becomes unreliable. As explained in following subsections, the resistive memory cells have the limited endurance. Beyond this number, these cells can become stuck-at defects. In addition, the power consumption depends on the number of writes.

A. Phase Change Memories (PCM)

PCM consists of chalcogenide materials like Ge-Sb-Te (GST), which are known to have two stable resistance states [12]. As shown in Fig. 1, the low resistance state (LRS) corresponds to a crystalline structure of the chalcogenide material, whereas the high resistance state (HRS) corresponds to an amorphous structure. The transition from HRS to LRS, known as SET, is brought about by applying a long and low-power heat pulse to the device by the means of a heating element. Similarly, the transition from LRS to HRS,
or RESET, is brought about by pulsing the device with a short and high-power heat pulse that melts the chalcogenide, thus amorphizing it. Both operations can be done on the nanosecond time scale. However, the elapsed time for SET operation could be up to ten times of RESET operation [12]. [14].

PCM has shown great promise as a storage-class memory due to its superior resistance ratio, scalability, low-energy switching, and high-speed [14], [15]. However, one of the main challenges for PCM is its endurance limit. From the point of view of the data, this corresponds to stuck-at defects (or stuck-at faults). Such defects may either appear in as-fabricated devices due to process variations or may be generated during the cycling process, i.e., rewriting.

The stuck-at defects in PCM are classified into: (1) stuck-at LRS defect which corresponds to the device in LRS being unable to RESET to HRS; and (2) stuck-at HRS defect which corresponds to the device in HRS incapable of being SET to LRS for the same operating conditions [16]. The stuck-at LRS defect is traditionally attributed to the formation of crystallites in the amorphous state that do not melt (during the amorphization pulse) due to local inhomogeneities [17]. This causes the HRS to gradually move towards the LRS with cycling. Similarly, the stuck-at HRS is attributed to the formation of voids in the materials and their eventual agglomeration [18]. This causes the material to experience an inhomogeneous and often insufficient heating during the SET operation.

B. Resistive Random-Access Memories (RRAM)

RRAM is another resistance change memory that relies on microstructural change in the material that causes the cell to have two resistance states (LRS and HRS). As shown in Fig. 2, the RRAM cell consists of a metal-oxide-metal (MOM) stack in which the sub-oxide is typically TaO$_x$, HfO$_x$, or TiO$_x$. The devices do not start off as being resistive switching memories; they have to go through a one-time programming process known as forming. The forming process involves the application of a high voltage pulse that causes the oxide to breakdown and form a conductive filament that shunts the two metal electrodes, causing the resistance to decrease [19]. The LRS corresponds to the shunted conductive filament. This filament can be disconnected by applying a voltage of the opposite polarity. Once the conductive filament is disconnected, the device resistance increases, and the device is said to be in the HRS. The device can now be cycled between LRS and HRS by applying voltages of opposite polarity as shown in Fig. 2.

As the RRAM switching mechanism is filamentary in nature, the RRAM devices are highly scalable, operate at ultra-low powers, have good retention characteristics, and can be integrated into a compact crossbar array [13].

However, similar to PCM, RRAM also suffers from limited endurance, especially when operated at low power [20]. In RRAM, the stuck-at defects may be additionally introduced during the forming process due to poor power-limiting during the breakdown [19].

The stuck-at LRS defects in RRAM have been attributed to the widening of the conductive filament [21]. Once the filament widens, the device resistance drops and the RESET power is insufficient to disconnect the filament. This causes the cell to be permanently set to LRS. The widening of the filament is thought of as a stochastic increase in the number of oxygen vacancies in the filament during the SET and forming operation. It can be explained by an incomplete retraction of oxygen vacancies during the previous RESET [22]. Similarly, the devices can also suffer from a stuck-at-HRS defect if the devices undergo over-RESET [23]. In this process, the oxygen vacancies are retracted irreversibly, making the device stuck-at HRS defect.

Similar to PCM, once the device starts experiencing the over-SET or over-RESET which precedes endurance failure, the devices would undergo a positive feedback that would make the stuck-at defects imminent. Moreover, as the endurance failure is mediated by stochastic motion of oxygen vacancies during the SET or RESET processes [24], it is very difficult to prevent these stuck-at defects.

III. CHANNEL MODEL

In Section II we explained that both PCM and RRAM suffer from stuck-at HRS or LRS defects. The resistance state can be sensed as either 0 or 1, depending on the sensing scheme of read operation (e.g., HRS → 0, LRS → 1 or vice versa). Thus, we can claim that the defect channel model by Kuznetsov and Tsybakov [25] is a proper mathematical model for resistive
A. Notation

We use parentheses to construct column vectors from comma separated lists. For a \( n \)-tuple column vector \( \mathbf{a} \in \mathbb{F}_q^n \) (where \( \mathbb{F}_q \) denotes the finite field with \( q \) elements and \( \mathbb{F}_q^n \) denotes the set of all \( n \)-tuple vectors over \( \mathbb{F}_q \)), we have

\[
(a_1, \ldots, a_n) = \begin{bmatrix} a_1 \\ \vdots \\ a_n \end{bmatrix} = [a_1 \ldots a_n]^T
\]

where superscript \( T \) denotes transpose. Note that \( a_i \) represents the \( i \)-th element of \( \mathbf{a} \). For a binary vector \( \mathbf{a} \in \mathbb{F}_2^n \), \( \pi \) denotes the bit-wise complement of \( \mathbf{a} \). For example, the \( n \)-tuple all-ones vector \( \mathbf{1}_n \) is equal to \( \mathbf{1}_n \), where \( \mathbf{0}_n \) is the \( n \)-tuple all-zero vector. Also, \( \mathbf{0}_{m,n} \) denotes the \( m \times n \) all-zero matrix.

In addition, \( ||a|| \) denotes the Hamming weight of \( a \) and \( \text{supp}(a) \) denotes the support of \( a \). We use the notation of \( [i : j] = \{i, i+1, \ldots, j\} \) for \( i < j \) and \( [n] = \{1, \ldots, n\} \). Note that \( \mathbf{a}_{[i:j]} = (a_i, \ldots, a_j) \) and \( \mathbf{a}_{\backslash i} = (a_1, \ldots, a_{i-1}, a_{i+1}, \ldots, a_n) \).

B. Channel Model: Defect Channel

We summarize the defect channel model in [25]. Define a variable \( \lambda \) that indicates whether the memory cell is defective or not and \( \mathbb{F}_q = \mathbb{F}_q \cup \{\lambda\} \). Let “\( \circ \)” denote the operator \( \circ : \mathbb{F}_q \times \mathbb{F}_q \rightarrow \mathbb{F}_q \) as in [26]

\[
x \circ s = \begin{cases} x, & \text{if } s = \lambda; \\ s, & \text{if } s \neq \lambda.\end{cases}
\]

By using the operator \( \circ \), an \( n \)-cell memory with defects is modeled by

\[
y = x \circ s
\]

where \( x, y \in \mathbb{F}_q^n \) are the channel input and output vectors. Also, the channel state vector \( s \in \mathbb{F}_q^n \) represents the defect information in the \( n \)-cell memory. Note that \( \circ \) is the vector component-wise operator.

If \( s_i = \lambda \), this \( i \)-th cell is called normal. If the \( i \)-th cell is defective (i.e., \( s_i \neq \lambda \)), its output \( y_i \) is stuck-at \( s_i \) independent of the input \( x_i \). So, the \( i \)-th cell is called stuck-at defect whose stuck-at value is \( s_i \). The probabilities of stuck-at defects and normal cells are given by

\[
P(S = s) = \begin{cases} 1 - \beta, & \text{if } s = \lambda; \\ \frac{\beta}{q}, & \text{if } s \neq \lambda.\end{cases}
\]

where the probability of stuck-at defects is \( \beta \). Fig. 3 shows the binary defect channel for \( q = 2 \).

In the defect channel model, it is assumed that the encoder knows the side information of defects before writing data to memories [25]. Hence, it can be explained by Gelfand-Pinsker problem [27].

IV. LOCALLY REWRITABLE CODES (LWC)

A. Motivation and Toy Example

As a toy example, suppose that \( n \)-cell binary memory has a single stuck-at defect. It is easy to see that this stuck-at defect can be handled by the following simple technique [25].

\[
\mathbf{c} = (\mathbf{m}, 0) + \mathbf{1}_n \cdot p
\]

where \( \mathbf{c} \in \mathbb{F}_2^n \) is a codeword and \( \mathbf{m} \in \mathbb{F}_2^k \) is an information (message) where \( k = n - 1 \) and \( p \) is a parity (redundant) bit.

Suppose that \( i \)-th cell is a defect whose stuck-at value is \( s_i \in \mathbb{F}_2 \). If \( i \in [n - 1] \) and \( s_i = m_i \), or if \( i = n \) and \( s_n = 0 \), then \( p \) should be 0. Otherwise, \( p = 1 \). Thus, \( p \) decides whether to flip \( \mathbf{m} \) or not. It is worth mentioning that this simple coding is optimal since it achieves the following upper bound in [25] with equality.

\[
n - t - \left\lfloor \log_2 \ln 2^t \left( \begin{bmatrix} n \\ t \end{bmatrix} \right) \right\rfloor \leq \log_2 \mathcal{M} \leq n - t
\]

where \( \mathcal{M} \) is the number of codewords and \( t \) is the number of stuck-at defects among \( n \) cells. For linear codes, \( k = \log_2 \mathcal{M} \), i.e., \( k \leq n - 1 \).

If there is no stuck-at defect among \( n \) cells, then we can store \( \mathbf{m} \) by writing \( \mathbf{c} = (\mathbf{m}, 0) \) (i.e., \( p = 0 \)). Now, consider the case when stored information needs to be updated causing \( \mathbf{m} \) to become \( \mathbf{m}' \). Usually, \( ||\mathbf{m} - \mathbf{m}'|| \ll n \), which happens often due to the updates of files. Instead of storing \( \mathbf{m}' \) into another group of \( n \) cells, it is more efficient to store \( \mathbf{m}' \) by rewriting only \( ||\mathbf{m} - \mathbf{m}'|| \) cells. For example, suppose that \( m_i' \neq m_i \) for an \( i \in [k] \) and \( m_j' = m_j \) for all other \( j \in [k] \setminus i \). Then, we can store \( k \)-bit \( \mathbf{m}' \) by rewriting only \( i \)-th cell.

An interesting problem arises when a cell to be rewritten is defective. Suppose that \( i \)-th cell is a stuck-at defect whose stuck-at value is \( s_i \). If \( s_i = m_i \neq m_i' \), then we should write \( \mathbf{c} = (\mathbf{m}, 0) \) for storing \( \mathbf{m} \). However, in order to store the updated information \( \mathbf{m}' \), we should write \( \mathbf{c}' = \mathbf{c} = (\mathbf{m}, 1) \) where \( p = 1 \). Thus, \( n - 1 \) cells should be rewritten to update one bit data \( m_i' \) without stuck-at error. The same thing happens when \( s_i = m_i' \neq m_i \). When considering endurance limit and
power consumption, rewriting $n - 1$ cells is a high price to pay for preventing one bit stuck-at error.

In order to relieve this burden, we change (6) by introducing an additional parity bit as follows.

$$c = \left[m_{[1:2]}, 0, m_{[2+1:n]}\right] + G_0p$$

$$= \left[m_{[1:2]}, 0, m_{[2+1:n]}\right] + \left[\frac{1}{2} 0 0 \right] \left(p_1, p_2\right)$$

where $k = n - 2$. For simplicity’s sake, we assume that $n$ is even. Then, $1_2$ and $0_2$ are all-ones and all-zeros column vectors with $n/2$ elements. By introducing an additional parity bit, we can reduce the number of rewriting cells from $n - 1$ to $n - 2$.

This idea is similar to the concept of Pyramid codes which are the early LRC [1]. For $n$ disk nodes, single parity check codes can repair one node failure (i.e., single erasure) by

$$1_2^T \hat{c} = 0$$

where $\hat{c}$ represents the recovered codeword from disk node failures. Assuming that $c_i$ is erased due to a node failure, $c_i$ can be recovered by

$$\hat{c}_i = c_i = \sum_{j \in [n] \setminus i} c_j.$$ 

For this recovery, we should access $k = n - 1$ nodes which degrades the repair speed. For more efficient repair process, we can add a new parity as follows.

$$H^T \hat{c} = \left[\frac{1}{2} 0 0 \right] \hat{c} = 0$$

Then, a failed node $c_i$ can be repaired by accessing only $\frac{n}{2} - 1$ nodes. Note that the repair locality of (12) is $\frac{n}{2} - 1$ whereas the repair locality of (10) is $n - 1$ which is a simple but effective idea of Pyramid codes.

An interesting observation is that $G_0$ of (8) is the same as $H$ of (12). In addition, note that the number of resistive memory cells to be rewritten is the same as the number of nodes to be accessed in distributed storage systems. This observation will be further discussed in Subsection IV-C.

**B. Locally Rewritable Codes**

In this subsection, we propose LWC by generalizing the idea of the toy example in the previous subsection. A traditional coding scheme for defect channel is additive encoding which masks defects by adding a carefully selected vector. The goal of masking stuck-at defects is to make a codeword whose values at the locations of defects match the stuck-at values of corresponding defects [23], [28]. The additive encoding can be formulated as

$$c = (m, 0_{n-k}) + c_0 = (m, 0_{n-k}) + G_0p$$

where $G_0 \in \mathbb{F}_2^{n \times (n-k)}$. By adding a vector $c_0 = G_0p \in \mathcal{C}_0$, we can mask stuck-at defects among $n$ cells. For the systematic codes, $G_0$ is given by [26]

$$G_0 = \left[ \begin{array}{c} R \\ I_{n-k} \end{array} \right]$$

where $R \in \mathbb{F}_2^{k \times (n-k)}$ and $I_{n-k}$ is the $(n-k)$-dimensional identity matrix. Note that the identity matrix is located in the parity part unlike the conventional error-control codes.

The decoding can be given by

$$\hat{m} = H^T y$$

where $\hat{m}$ represents the recovered message of $m$. Note that the parity check matrix $H_0$ of $\mathcal{C}_0$ is given by $H_0 = [I_k R]^T$ and $H_0^T G_0 = 0_{k,n-k}$. Note that (15) is equivalent to the equation of coset codes.

The minimum distance of additive encoding is given by

$$d^* = \min_{x \neq 0} \|x\|$$

which means that any $d^* - 1$ rows of $G_0$ are linearly independent. Thus, additive encoding guarantees masking up to $d^* - 1$ stuck-at defects [26], [28].

Now we investigate rewriting locality of additive encoding. As repair locality of LRC is meaningful only for single disk failure, rewriting locality is valid when there is one stuck-at defect among $n$ cells. In distributed storage systems, the most common case is a single node failure among $n$ nodes [1]. Similarly, for a proper defect probability $\beta$, we can claim that the most common scenario of resistive memories is that there is a single stuck-at defect among $n$ cells.

We define initial writing cost and rewriting cost which are related to write endurance and power consumption.

**Definition 1 (Initial Writing Cost):** Suppose that $m$ was stored by its codeword $c$ in the initial stage of $n$ cells where all the normal cells are set to zeros. The writing cost is given by

$$\Delta(m) = \|c\| - t_\lambda 0$$

where $t_\lambda 0$ denotes the number of stuck-at defects whose stuck-at values are nonzero.

In (17), we assume that there are $t$ stuck-at defects among $n$ cells and $c$ masks these $t$ stuck-at defects successfully. So, we do not need to write stuck-at defects since their stuck-at values are the same as corresponding elements of $c$.

**Definition 2 (Rewriting Cost):** Suppose that $\hat{m}$ was stored by its codeword $c$ in $n$ cells. If $c'$ is rewritten to these $n$ cells to store the updated $\hat{m}'$, the rewriting cost is given by

$$\Delta(m, m') = \|c - c'\|$$

where we assume that both $c$ and $c'$ mask stuck-at defects.

High rewriting cost implies that the states of lots of cells should be changed, which is harmful to write endurance and increases power consumption.

It is worth mentioning that, in general, the rewriting cost is more important than the initial writing cost since most of write operations will be rewriting. If a device offers write endurance of 10000 cycles, the write operations of 9999 will be rewriting whereas only one among 10000 writing is the initial write operation (i.e., 0.01%). However, there may be some storage applications (such as for archival storage), where the number of initial writings and rewritings may be similar.
Now, we introduce the rewriting locality which affects initial writing cost and rewriting cost.

**Definition 3 (Information Rewriting Locality):** Suppose that \( m_i \) for \( i \in [k] \), i.e., information (message) part, should be updated to \( m_i' \neq m_i \) and the corresponding \( i \)-th cell is a stuck-at defect. If \( m_i \) can be updated to \( m_i' \) by rewriting \( r^* \) other cells, then the \( i \)-th coordinate has information rewriting locality \( r^* \).

**Lemma 4:** If the \( i \)-th coordinate for \( i \in [k] \) has information rewriting locality \( r^* \), then there exists \( c_0 \in C_0 \) such that \( i \in \text{supp}(c_0) \) and \( \|c_0\| = r^* + 1 \).

**Proof:** For \( m \) and \( m' \), suppose that \( m_i \neq m_i' \) for an \( i \in [k] \) and \( m_j = m_j' \) for all other \( j \in [k] \setminus i \). Note that \( i \)-th cell is a stuck-at defect whose stuck-at value is \( s_i \). We should consider the following cases:

1. \( m_i' \neq m_i = s_i \).
2. \( m_i \neq m_i' = s_i \).
3. \( m_i \neq m_i' \neq s_i \) and \( m_i' \neq s_i \).

For \( m_i' \neq m_i = s_i \), it is obvious that \( c = (m, 0_{n-k}) \) and \( c' = (m', 0_{n-k}) + c_0' \) where \( c_0' = c_0 \) and \( m_i = m_i' = s_i \). For the information rewriting locality \( r^* \), \( c_0' \in C_0 \) should satisfy \( \|c_0'\| = r^* + 1 \) to mask the stuck-at defect by writing \( r^* \) cells. Note that we do not need to write the stuck-at defect since its stuck-at value is \( s_i = c_0' \). For \( m_i' \neq m_i = s_i \), the proof is similar.

For \( m_i \neq m_i' \), \( m_i \neq s_i \) and \( m_i' \neq s_i \), \( c = (m, 0_{n-k}) + c_0 \) and \( c' = (m', 0_{n-k}) + c_0' \) where \( c_0' = c_0 \) and \( m_i = m_i' = s_i \). We can pick \( c_0 \) and \( c_0' \) such that \( \|c_0\| = r^* + 1 \) to satisfy the condition.

**Definition 5 (Parity Rewriting Locality):** Suppose that only one nonzero symbol \( m_i \) should be stored to the initial stage of \( n \) cells. Note that there is a stuck-at defect in the parity location \( j \) for \( j \in [k + 1 : n] \) (i.e., parity part) and \( s_j \neq 0 \). If \( m_i \) can be stored by writing at most \( r^* + 1 \) cells, then the \( j \)-th coordinate has parity rewriting locality \( r^* \).

**Lemma 6:** If the \( j \)-th coordinate for \( j \in [k + 1 : n] \) has parity rewriting locality \( r^* \), then there exists \( c_0 \in C_0 \) such that \( j \in \text{supp}(c_0) \) and \( \|c_0\| = r^* + 1 \).

**Proof:** Suppose that \( m \) should be stored to the initial stage of \( n \) cells where \( m_i \neq 0 \) for \( i \in [k] \) and \( m_i' = 0 \) for \( i' \in [k] \setminus i \). By (13), \( c = (m, 0_{n-k}) + c_0 \) such that \( m_i = s_i \) where \( s_i \)-th cell is a stuck-at defect for \( j \in [k + 1 : n] \). For the rewriting locality \( r^* \), \( c_0 \) should satisfy \( \|c_0\| = r^* + 1 \). If \( i \in \text{supp}(c_0) \), then it is possible to store \( m_i \) without stuck-at error by writing \( \|c_0\| = r^* \) cells since we do not need to write \( m_i \). Otherwise, we should write both \( m_i \) and \( \|c_0\| \), i.e., \( r^* + 1 \) cells.

**Definition 7 (Locally Rewritable Codes):** If any \( i \)-th coordinate for \( i \in [n] \) has (information or parity) rewriting locality at most \( r^* \), then this code is called locally rewriteable code (LWC) with rewriting locality \( r^* \). \((n, k, d^*, r^*)\) LWC code is a code of length \( n \) with information length \( k \), minimum distance \( d^* \), and rewriting locality \( r^* \).

Now, we show in the following theorem that rewriting locality \( r^* \) is an important parameter for rewriting cost.

**Theorem 8:** Suppose that \( m \) is updated to \( m' \) by LWC with rewriting locality \( r^* \). If there is a single stuck-at defect in \( n \) cells, then the rewriting cost \( \Delta(m, m') \) is given by

\[
\Delta(m, m') \leq \|m - m'\| + r^* - 1. \tag{19}
\]

**Proof:** First, suppose that the single defect’s coordinate is \( i \in [k] \) and its stuck-at value is \( s_i \). If \( m_i = m_i' \), then \( \Delta(m, m') = \|m - m'\| \) since \( c = (m, 0) + c_0 \) and \( c' = (m', 0) + c_0 = (m', 0) + c_0 \) where \( c_0 = 0 \).

If \( m_i \neq m_i' = s_i \), then \( c = (m, 0) + c_0 \) and \( c' = (m', 0) + c_0 = (m', 0) \) where \( c_0 = 0 \). In order to mask the stuck-at defect, \( i \in \text{supp}(c_0) \). Then,

\[
\Delta(m, m') = \|c - c'\| = \|(m, 0) + c_0 - (m', 0)\| \leq \|m - m'\| + \|c_0\| - 2 = \|m - m'\| + r^* - 1 \tag{23}
\]

Now, if \( s_i \neq 0 \), then \( s_i = c_0 \). By supposing \( m_i \neq m_i' = c_0 \), \( c_0 = 0 \) is the \( i \)-th element of \( c_0 \). Also, (23) follows from Lemma 4. If \( s_i \neq 0 \), then \( c_0 = 0 \) is the \( i \)-th element of \( c_0 \). By supposing \( m_i \neq m_i' = c_0 \), \( c_0 = 0 \) is the \( i \)-th element of \( c_0 \). We show that existing construction methods of LRC and LWC are helpful for improving endurance and power consumption.

**C. Duality of LRC and LWC**

In this subsection, we investigate the duality of LRC and LWC. We show that existing construction methods of LRC can be used to construct LWC based on this duality. First, the relation between minimum distance \( d^* \) and rewriting locality \( r^* \) is observed.
Definition 10: If \( C_0 \) is cyclic, then the LWC is called cyclic.

Lemma 11: Let \( C_0 \) denote a cyclic code whose minimum distance is \( d_0 \). Then, corresponding cyclic LWC’s rewriting locality is \( r^* = d_0 - 1 \).

Proof: Due to the property of cyclic codes, we can claim that there exists \( c_0 \in C_0 \) such that \( i \in \text{supp}(c_0) \) and \( \|c_0\| = d_0 \) for any \( i \in \{n\} \). Since \( d_0 \) is the minimum distance of \( C_0 \), we can claim that the rewriting locality is \( r^* = d_0 - 1 \).

From the definition of \( d^* \) in (16), \( d^* = d_0^\perp \) which is the minimum distance of \( C_0^\perp \), namely, dual code of \( C_0 \). Thus, the parameters of cyclic LWC is given by

\[
(d^*, r^*) = (d_0^\perp, d_0 - 1).
\]

In [8, 9], an equivalent relation for cyclic LRC was given by

\[
(d, r) = (d, d^\perp - 1).
\]

By comparing (28) and (29), we observed the duality between LRC and LWC. This duality is important since it indicates that we can construct LWC using existing construction methods of LRC as shown in the following theorem.

Theorem 12: Suppose that \( H^LRC \in \{0, 1\}^{(n-k) \times (n-k)} \) is the parity check matrix of cyclic LRC \( C^LRC \) with \( (d, r) = (d, d^\perp - 1) \). By setting \( G_0 = H^LRC \), we can construct cyclic LWC \( C^LWC \) with

\[
(d^*, r^*) = (d, d^\perp - 1).
\]

Proof: By setting \( G_0 = H^LRC \), the LWC’s codeword \( c \in C^LWC \) is given by

\[
c = (m, 0) + H^LRC \cdot p.
\]

The minimum distance \( d^* \) of \( C^LWC \) is given by

\[
d^* = \min_{x \neq 0} \|x\|_{H^LRC^T x = 0}
\]

which is equivalent to the minimum distance \( d \) of \( C^LRC \). Hence, we can claim that

\[
d^* = d_0^\perp = d.
\]

From (28) and (31), \( r^* = d_0 - 1 = d^\perp - 1 \).

Remark 13 (Optimal Cyclic LWC): Theorem 12 shows that the optimal cyclic \( (n, k, r, d) \) LRC can be used to construct the optimal cyclic \( (n, k, r^*, d^*) \) LWC such that

\[
d^* = n - k - \left\lceil \frac{k}{r^*} \right\rceil + 2.
\]

Hence, the optimal LWC can be constructed from the optimal LRC.

Remark 14 (Bound of LWC): From Theorem 12 and Remark 13, we can claim the following bound for LWC.

\[
d^* \leq n - k - \left\lceil \frac{k}{r^*} \right\rceil + 2
\]

which is equivalent to the bound for LRC given by (1).

In Table I, the duality properties of LRC and LWC are summarized. In the decoding of LRC, \( \hat{c} \) denotes a recovered codeword from node failures. In addition, \( \hat{m} \) in the decoding of LWC represents the recovered message. It is worth mentioning that this duality can be connected to the duality between erasures and defects [29].

V. CONCLUSION AND FUTURE WORK

Inspired by LRC for distributed storage systems, we proposed LWC to improve endurance limit and power consumption of resistive memories. We showed the relation between rewriting cost and rewriting locality of LWC. Also, we investigated the duality between LRC and LWC, which makes it possible to construct LWC by using existing construction methods of LRC.

As part of our future work, we plan to evaluate the performance of LWC. Although some recent works have investigated the characteristics of endurance limit [20, 24], a proper channel model is not available. Hence, the performance evaluation would need to be based on the experiments with real resistive memory chips.

**REFERENCES**

[1] C. Huang, M. Chen, and J. Li, “Pyramid codes: Flexible schemes to trade space for access efficiency in reliable data storage systems,” in Proc. IEEE Int. Symp. Netw. Comput. Appl. (NCA), Jul., 2007, pp. 79–86.
[2] P. Gopalan, C. Huang, H. Simitci, and S. Yekhanin, “On the locality of codeword symbols,” IEEE Trans. Inf. Theory, vol. 58, no. 11, pp. 6925–6934, Nov. 2012.
[3] I. Tamo and A. Barg, “A family of optimal locally repairable codes,” IEEE Trans. Inf. Theory, vol. 60, no. 8, pp. 4661–4676, Aug. 2014.
[4] N. Silberstein, A. S. Rawat, O. O. Koyluoglu, and S. Vishwanath, “Optimal locally repairable codes via rank-metric codes,” in Proc. IEEE Int. Symp. Inf. Theory (ISIT), Jul. 2013, pp. 1819–1823.
[5] I. Tamo, D. S. Papailiopoulos, and A. G. Dimakis, “Optimal locally repairable codes and connections to matroid theory,” in Proc. IEEE Int. Symp. Inf. Theory (ISIT), Jul. 2013, pp. 1814–1818.
[6] S. Goparaju and R. Calderbank, “Binary cyclic codes that are locally repairable,” in Proc. IEEE Int. Symp. Inf. Theory (ISIT), Jul. 2014, pp. 676–680.
[7] M. Shahabinejad, M. Khabbazian, and M. Ardakani, “An efficient binary locally repairable code for hadoop distributed file system,” IEEE Commun. Lett., vol. 18, no. 8, pp. 1287–1290, Aug. 2014.
[8] P. Huang, E. Yaakobi, H. Uchikawa, and P. H. Siegel, “Cyclic linear binary locally repairable codes,” in Proc. IEEE Inf. Theory Workshop (ITW), Apr. 2015, pp. 1–5.
[9] I. Tamo and A. Barg, “Cyclic LRC codes and their subfield subcodes,” in Proc. IEEE Int. Symp. Inf. Theory (ISIT), Jul. 2015, pp. 1262–1266.
[10] N. Silberstein and A. Zeh, “Optimal binary locally repairable codes via antcodes,” in Proc. IEEE Int. Symp. Inf. Theory (ISIT), Jun. 2015, pp. 1247–1251.

2Fig. 4 in [29] shows that the relation between the endurance and the probability of stuck-at defects might be modeled by the lognormal distribution. However, only 25 cells were observed, which would not be enough to characterize the channel model.
Intel and Micron, “3D XPoint Technology,” 2015. [Online]. Available: https://www.micron.com/about/innovations/3d-xpoint-technology

H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, “Phase change memory,” Proc. IEEE, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.

H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, “Metal–Oxide RRAM,” Proc. IEEE, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

S. Raoux, F. Xiong, M. Wuttig, and E. Pop, “Phase change materials and phase change memory,” MRS Bulletin, vol. 39, pp. 703–710, Aug. 2014.

S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y. C. Chen, R. M. Shelby, M. Saliga, D. Krebs, S.-H. Chen, H. L. Lung, and C. H. Lam, “Phase-change random access memory: A scalable technology,” IBM Journal of Research and Development, vol. 52, no. 4.5, pp. 465–479, Jul. 2008.

S. Kim, P. Y. Du, J. Li, M. Breitwisch, Y. Zhu, S. Mittal, R. Cheek, T.-H. Hsu, M. H. Lee, A. Schrott, S. Raoux, H. Y. Cheng, S.-C. Lai, J. Y. Wu, T. Y. Wang, E. A. Joseph, E. K. Lai, A. Ray, H.-L. Lung, and C. Lam, “Optimization of programming current on endurance of phase change memory,” in Proc. Int. Symp. VLSI Technol., Syst., Appl. (VLSI-TSA), Apr. 2012, pp. 1–2.

C. F. Chen, A. Schrott, M. H. Lee, S. Raoux, Y. H. Shih, M. Breitwisch, F. H. Baumann, E. K. Lai, T. M. Shaw, P. Flaitz, R. Cheek, E. A. Joseph, S.-H. Chen, B. Rajendran, H. L. Lung, and C. Lam, “Endurance improvement of Ge2Sb2Te5-based phase change memory,” in Proc. IEEE Int. Memory Workshop (IMW), May 2009, pp. 1–2.

A. A. Sharma, M. Noman, M. Abdelmoula, M. Skowronski, and J. A. Bain, “Electronic instabilities leading to electroformation of binary metal oxide-based resistive switches,” Adv. Functional Mater., vol. 24, no. 35, pp. 5522–5529, Jul. 2014.

S. I. Gelfand and M. S. Pinsker, “Coding for channel with random parameters,” Probl. Contr. and Inf. Theory, vol. 9, no. 1, pp. 19–31, 1980.

B. S. Tsybakov, “Additive group codes for defect correction,” Probl. Peredachi Inf., vol. 11, no. 1, pp. 111–113, Jan.–Mar. 1975.

Y. Kim and B. V. K. Vijaya Kumar, “On the duality of erasures and defects,” arXiv preprint arXiv:1403.1897, vol. abs/1403.1897, 2014. [Online]. Available: http://arxiv.org/abs/1403.1897

A. V. Kuznetsov and B. S. Tsybakov, “Coding in a memory with defective cells,” Probl. Peredachi Inf., vol. 10, no. 2, pp. 52–60, Apr.–Jun. 1974.