A Novel VLSI Architecture of Fixed-complexity Sphere Decoder

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Abstract—Fixed-complexity sphere decoder (FSD) is a recently proposed technique for multiple-input multiple-output (MIMO) detection. It has several outstanding features such as constant throughput and large potential parallelism, which makes it suitable for efficient VLSI implementation. However, to our best knowledge, no VLSI implementation of FSD has been reported in the literature, although some FPGA prototypes of FSD with pipeline architecture have been developed. These solutions achieve very high throughput but at very high cost of hardware resources, making them impractical in real applications. In this paper, we present a novel four-nodes-per-cycle parallel architecture of FSD, with a breadth-first processing that allows for short critical path. The implementation achieves a throughput of 213.3 Mbps at 400 MHz clock frequency, at a cost of 0.18 mm² Silicon area on 0.13μm CMOS technology. The proposed solution is much more economical compared with the existing FPGA implementations, and very suitable for practical applications because of its balanced performance and hardware-complexity; moreover it has the flexibility to be expanded into an eight-nodes-per-cycle version in order to double the throughput.

Keywords—MIMO detection; Fixed-complexity Sphere Decoder; constant throughput; parallel architecture; breadth-first processing; VLSI implementation

I. INTRODUCTION

Multiple-input multiple-output (MIMO) system has been widely investigated to provide high data-rate and robust wireless link, with an acceptable implementation complexity [1]. It has been already included in some wireless communication standards, such as IEEE 802.16. One of the most challenging problems in MIMO system is to separate the interferences caused by the multiple antennas. Therefore, several MIMO detection algorithms have been proposed to solve this problem.

Among the large variety of MIMO detection techniques, Sphere decoder (SD) is one of the most promising solutions. The well known depth-first sphere decoder employs Schnorr-Euchner enumeration [2] (SEE-SD) to perform tree traversal and achieves maximum-likelihood (ML) performance. However, a major limitation of SEE-SD is the intrinsic variable throughput, which tends to drop off significantly with decreasing signal-to-noise ratio (SNR) [3]. Some other sub-optimal algorithms, such as K-best algorithm and fixed-complexity sphere decoder (FSD), are proposed to obtain constant throughput and lower hardware-complexity, at an acceptable cost of performance loss [4][5]. The first proposed SDs were hard-output, while, recently, soft-output MIMO detectors have been investigated to construct iterative decoding systems integrated with channel decoders, such as convolutional decoders or Turbo decoders, to achieve near-capacity performance [6]. Soft-information could be easily obtained by extending the existing hard-output SD into list sphere decoder (LSD), which generates a candidate list instead of the only ML solution. Then log-likelihood-ratios (LLR) are calculated from the list for each codeword bit and forwarded to the channel decoder.

The soft-output SEE-SD achieves optimal performance, but still with a variable throughput [7]. Efficient VLSI implementations have also been recently proposed for single tree search SD (STS-SD) [8][9], which provide excellent throughput at medium to high SNR values, but tend to be much less efficient at low SNR. Furthermore, several MIMO detection algorithms can hardly be mapped to highly parallel architectures, because of the adopted sequential search order.

Some other algorithms guarantee constant throughput at the price of a certain performance loss, which is due to the use of sub-optimal search methods. Examples of this approach are the soft-output K-best SD [4], which requires sorting operation, and FSD [5], which also achieves a constant throughput with a relatively lower hardware complexity, making it very suitable to perform soft-output MIMO detection. The most attracting advantage of the FSD is the regular tree traversal order that enables highly-efficient implementation. At the same time, the data dependency between two levels of the tree can be avoided in FSD, so allowing for higher clock frequency.

The present work deals with this kind of constant throughput approach and specifically with FSD implementation. As far as we know, all the reported implementations of FSD are based on FPGA devices, and no VLSI solution is available. These implementations achieve very high throughput by employing pipeline architectures, but at the cost of large hardware resources [10][11]. Furthermore, they do not fully exploit the breadth-first visiting order of FSD, in order to improve the decoding speed.

In this paper we present a high-speed and low-cost VLSI implementation of FSD, applying two major innovations:
• A four-nodes-per-cycle parallel architecture that increases the throughput with respect to the usual one-node-per-cycle solution.

• A processing schedule that combines breath-first node visiting order and pipelining to remove the data dependency between two adjacent levels and shorten the critical path.

These new solutions do not result into an efficient FPGA implementation, mainly because of the poor performance of multi-operand adders on FPGA technology. However it will be shown that the proposed solution enables high efficiency in Silicon implementation. The occupied Silicon area is close to 0.18 mm², on a 0.13μm CMOS technology, and the achieved throughput is 213.3 Mbps at 400 MHz clock frequency. It is one of the most efficient FSD implementations among the reported works and is easily scalable to higher degrees of parallelism to meet the increasing throughput requirements of current and future wireless communication standards.

This paper is organized as follows: Section II introduces the system model of FSD; details of the proposed four-nodes-per-cycle parallel architecture are discussed in Section III; Section IV compares the overall performance among several implementations of SD; finally, Section V concludes the paper.

II. SYSTEM MODEL OF FSD

In an iterative MIMO decoding system (as shown in Fig. 1) with \( N_t \) transmit antennas and \( N_r \) receive antennas, the source bits \( s_{y_1} \) are firstly encoded into \( y_1 \) by a channel encoder, such as convolutional encoder or Turbo encoder. Then the coded bit stream after interleaving (II), \( x_i \), is mapped to a \( N_r \)-dimensional transmit signal vector \( s = [s_{N_t-1}, \ldots, s_1, s_0]^T \). Each symbol \( x_i \) is chosen independently from a complex constellation \( \Omega \) with \( M \) binary bits per symbol, i.e., \( |\Omega| = 2^M \). For 16-QAM modulation, \( M = 4 \) and \( |\Omega| = 16 \). The received vector can be denoted as

\[
y = Hs + n,
\]

where \( H \) is the \( N_r \times N_t \) complex channel matrix, assumed to be perfectly known at the receiver through channel estimation, \( n = [n_{N_r-1}, \ldots, n_1, n_0]^T \) is a \( N_r \)-dimensional complex Gaussian noise vector.

The soft-output MIMO detector is employed to generate soft-information based on the received vector \( y \) and the channel matrix \( H \). Several algorithms are investigated to perform soft-output MIMO detection, such as minimum mean square error (MMSE) and LSD. In this paper we assume LSD is employed, output MIMO detection, such as minimum mean square error (MMSE) and LSD. In this paper we assume LSD is employed.

In the transmitted vector symbol constellation \( \Omega^N_t \), there exists a ML solution that can be expressed as

\[
s^{ML} = \arg \min_{s \in \Omega^N_t} \| y - Hs \|^2 .
\]
At the beginning of decoding, the radius is set to infinity. Tree traversal moves from top to down. Whenever a leaf in the lowest level is reached, and the PED of the leaf is less than the current radius, the radius is replaced by the value of the PED. The SEE-SD performs tree pruning by comparing the PED of each node with the current radius. If the PED is larger than the radius, the node with the whole branch under it is pruned. So the total number of visited nodes is significantly reduced with respect to exhaustive-search, still yielding ML performance.

The soft-output SEE-SD performs the similar depth-first tree search to get a candidate list. The difference compared with the hard-output SEE-SD is that the radius will not be updated until a required number of candidates are obtained [6], making it slower than the hard-output counterpart, because it needs to visit more nodes. In the soft-output case, the whole candidate list is sent to a LLR generator to calculate the soft-information, which is needed by the channel decoder in the iterative MIMO decoding system. LLRs are evaluated for each information, which is needed by the channel decoder in the candidate list is sent to a LLR generator to calculate the soft-information, which is needed by the channel decoder in the iterative MIMO decoding system. LLRs are evaluated for each bit according to

\[
L_k(x_k | y) = \frac{1}{2} \max_{x_k \in \mathcal{X}_k} \left\{ -\frac{1}{\sigma^2} \|y - Hs_k + x_k \|_2^2 + \sum_{l=1}^{K} l \cdot L_{k+l} \right\},
\]

where \(x_k \in \mathcal{X}_k\) and \(x_{k+1} \in \mathcal{X}_{k+1}\) represent the sets of vector \(x\) having \(x_k = +1\) and \(x_k = -1\) respectively, \(\sigma^2\) is the noise variance, \(x_k\) is the subvector of \(x\) omitting the bit \(x_k\), and \(L_{k+l}\) is the subvector of the a-priori information vector \(L\).

The FSD is also based on PED calculation while traversing the tree. The main difference compared with the SEE-SD is that the FSD does not need to update the hypersphere radius in order to perform tree pruning. At each level of the tree, the number of nodes to be visited is pre-fixed. It can be defined in different ways, which yield different performance. A theoretically derived formula giving the best node distribution along the tree is not available. However, the best solution can be found based on the Monte Carlo simulations for the SEE-SD, and choosing the node numbers in each level from a small set \(\{1, N_b\}\), where \(N_b\) is the number of branches per node [14].

We performed design space exploration in order to search the best node distribution, and finally found that for the system with 4×4 antennas and 16-QAM modulation, the node distribution of \(\{11111144\}\) achieves the best BER performance. This representation means that in the highest two levels, all the 4 child nodes are visited, while in the lower levels, only one child node with minimum PED is visited. Therefore, 4 nodes are visited in the top level and 16 nodes are visited in each of the lower levels. We also found that a simple sorted QR decomposition (SQRD) [15] significantly improves the performance. Fig. 2 shows the performance offered by both FSD and SEE-SD soft-output detectors coupled with a four state, 1/3 code rate Turbo decoder, which executes 8 decoding iterations; the detectors operate on a 4×4 MIMO channel with 16-QAM modulation and performance are given after two iterations between detection stage and channel decoder. In the reported results, it can be seen that the FSD with SQRD achieves a better performance compared with ordinary QRD.

Because the FSD does not need to reach the lowest tree level immediately to update the radius, the traversal order is very flexible, and can be done either in depth-first or in breadth-first style. We found that the breadth-first order is an essential feature of FSD because the data dependency between a pair of parent-child nodes can be avoided by performing breadth-first tree traversal. It is helpful to shorten the critical path, and we utilized this feature in the proposed four-nodes-per-cycle architecture. Another advantage of the FSD is that the numbers of visited nodes are the same for both hard-output and soft-output versions. Therefore they have the same throughputs.

### III. PARALLEL FSD ARCHITECTURE

Fixed and regular traversal order makes the FSD very suitable to adopt parallel architectures and to improve the throughput. FSD algorithm also admits a scalable amount of parallelism, which enables to trade-off complexity for performance. A straightforward way to increase throughput is to adopt a pipeline architecture, as reported in [10] and [11]. These implementations achieve very high throughput, however, they also involve very high hardware complexity, which makes them impractical in real applications. To solve this problem, we propose a novel four-nodes-per-cycle parallel architecture to reduce the hardware complexity, while maintaining a throughput high enough for most applications.

#### A. Four-nodes-per-cycle architecture

In each level, a group of four nodes are processed in parallel, thanks to the fact that there is no data dependency between them. In the top level, all the four nodes are processed in one cycle, while in each of the lower levels, four cycles are needed to process the 16 nodes which are chosen to be visited, by applying the breadth-first order, in a zig-zag fashion, as shown in Fig. 3. Four nodes of each group in dashed blocks are processed in parallel.

![Figure 2. BER performance of the iterative MIMO decoding system for soft-output SEE-SD and FSD with different QR decompositions. The list size is 16 for both SEE-SD and FSD. Node distribution \{11111144\} is adopted for FSD. "2 iterations" means two iterations between the soft-output MIMO detector and the Turbo decoder.](image_url)
In a SEE-SD, there always exists a data parallel and in the breadth-first order. The essence of breadth-first visiting order is that the three main arithmetic tasks, including $d_i$ calculation, $b_i$ calculation and direct enumeration, are processed in the same single cycle for three different groups of nodes, and there is not any data dependency among them, which insures that the critical path is successfully divided into independent shorter paths.

To clarify the proposed breadth-first visiting order, the timing details for the graph example of Fig. 3 are explained in Table I. In each cycle, $d_i$ calculation, $b_i$ calculation and direct enumeration are performed separately for three different groups of node illustrated in Fig. 3. In the first cycle, $b_i$ for all the four groups in level 6 are calculated, because all the nodes in each of the four groups share the same value of $b_i$. Therefore they can be calculated concurrently by the four $b_i$ units. Moreover, in the top two levels, the output of DE units are discarded, because all the nodes in the two levels are visited and it is not needed to perform enumeration.

### C. Architecture details

The implementation is targeted to a MIMO system with $4 \times 4$ antennas and 16-QAM modulation. The internal data width is chosen to be 12 bits, based on the evaluation of numerical simulation. In this paper we mainly focus on the FSD implementation. The QR decomposition and LLR calculation are implemented in standard algorithms without special optimization.

1) **Diagram of the four-nodes-per-cycle architecture**

The block scheme of the four-nodes-per-cycle FSD architecture is shown in Fig. 4. Each of the main arithmetic tasks employs four units with the same internal structure, in order to process four nodes in parallel per clock cycle.

Because of the breadth-first processing order, different tasks of processing a node are performed in different cycles. The signals with index $\text{crt}$ are referred to the current cycle, while those with index $\text{prv}$ are related to the previous cycle. The signal lines with slashes are referred to four different values for each of the four nodes in a certain group.

The tree traversal paths in FSD are highly regular, as shown in Fig. 3, which ensures that the nodes being processed in each cycle have definite positions. The FSD performs different tasks in each cycle according to the position, which is controlled by a level counter and a column counter in the control unit. The tree traversal path contains eight levels and four columns, as shown in Fig. 3. Therefore a 3-bits register is enough for the level counter and a 2-bits register is employed as the column counter.

2) **Calculation of $b_i$**

In the first level, $b_1 = y_1^2Z^P$, therefore the value of $y_1^2Z^P$ is directly written into $b_1$ cache at reset. Then in the first cycle, it is immediately used by the $d_i$ units for calculating the PED. In the following levels, the four $b_i$ units are responsible for $b_i$ calculation.

### Table I. Task Distribution in Each Cycle

| Cycle | $d_i$ | $b_i$ | DE |
|-------|-------|-------|-----|
| 1     | $G_{6,3}$ | $G_{6,4}$ | -   |
| 2     | $G_{6,2}$ | $G_{6,3}$ | -   |
| 3     | $G_{6,1}$ | $G_{6,2}$ | $G_{6,3}$ |
| 4     | $G_{6,4}$ | $G_{6,5}$ | $G_{6,6}$ |
| 5     | $G_{6,6}$ | $G_{6,7}$ | $G_{6,8}$ |
| 6     | $G_{6,7}$ | $G_{6,8}$ | $G_{6,9}$ |
| 7     | $G_{6,9}$ | $G_{6,10}$ | $G_{6,11}$ |
| 8     | $G_{6,11}$ | $G_{6,12}$ | $G_{6,13}$ |
| ...   | ...   | ...   | ... |
When computing $b_i$, because the value of $\hat{s}_j$ is chosen from a small set $\{+3, +1, -1, -3\}$ for 16-QAM modulation, the multiplication between $R_{ij}$ and $\hat{s}_j$ can be transformed into an addition:

$$R_{ij} \times (+3) = R_{ij} + 2R_{ij}, \quad (11)$$

$$R_{ij} \times (+1) = R_{ij}, \quad (12)$$

$$R_{ij} \times (-1) = -R_{ij}, \quad (13)$$

$$R_{ij} \times (-3) = -R_{ij} - 2R_{ij}. \quad (14)$$

The value of $2R_{ij}$ and $-2R_{ij}$ can be easily obtained through left shifting operation. But the additions are not performed immediately. Instead, the summands and addends are just left separated. Then a Wallace compress tree [16] is constructed involving all the outputs of the multipliers. In order to shorten the delay path, all of the 14 variables are compressed into a Wallace tree of carry save adder (CSA) with 6 levels, which is followed by a common ripple carry adder (RCA), as shown in Fig. 5.

The $b_i$ units are the most complicated blocks in the FSD architecture. Therefore we considered another solution for $b_i$ calculation in order to choose a more efficient solution. Instead of calculating the values in a single cycle, we distribute the accumulation task into several cycles by employing additional registers to store the updated values of $\sum_{j=1}^{7} R_{ij} \hat{s}_j$ in each cycle, as shown in Fig. 6. Because $R_{ij} \hat{s}_j$ is used immediately, it does not need to be stored. Therefore 6 registers are needed for lower levels. The output selection is controlled by the level counter in the control unit, as shown in Fig. 4.

We compared the two solutions in order to choose the most efficient one. From synthesis results given in Table II, the complexity of the CSA based $b_i$ calculation is 2,677 GE (gate equivalent). Synthesis has been performed at the clock frequency of 500 MHz on 0.13 $\mu$m CMOS technology. As four $b_i$ need to be calculated in parallel, the whole cost is $2,677 \times 4 = 10.7$ K GE. On the other side, the second solution of Fig. 6 results into a cost of 2,728 GE when synthesized on the same technology at the same clock frequency. The performances of the two individual solutions are quite similar. However if we consider the whole design, the adoption of the second solution in a breadth-first architecture implies that 16 $b_i$ calculation units are allocated, and therefore the total cost is $2,728 \times 16 = 43.6$ K GE. We conclude that the CSA based solution is more appropriate for breadth-first FSD algorithm.

We also found that the first solution is well suitable for VLSI implementation but not for FPGA, because of its larger number of logic levels, which has significant impact on speed. This will be discussed in Section IV.

3) Direct enumeration

Direct enumeration is employed to choose which child node in the next level will be visited, by comparing $|e_j|$ among all the child nodes of a common parent node. The child node with minimum $|e_j|$ is chosen as survival. Because all the nodes are visited in the top two levels, there is no need to perform the direct enumeration. Therefore the output of the DE unit is discarded for nodes belonging to the top two levels.

![Figure 4. Diagram of the four-nodes-per-cycle FSD architecture](image)

![Figure 5. The first solution for $b_i$ calculation](image)

![Figure 6. The second solution for $b_i$ calculation](image)

| | Silicon Area Solution 1 | Solution 2 |
|---|---|---|
| Combinational area (GE) | 2,677 | 2,000 |
| Noncombinational area (GE) | - | 728 |
| Total area (GE) | 2,677 | 2,728 |
Since \( b_i \) is already calculated in the previous cycle, the task of DE unit is just to compare the value of \( |b_i - R_i \hat{s}_i| \) among the child nodes, as shown in Fig. 7. \( R_{ij} \) is multiplied with each element of the set \{+3, +1, -1, -3\} separately. Then all the products are subtracted by \( b_i \). Two levels of 12-bits comparators are employed to choose the child node with minimum absolute value of \( |b_i - R_i \hat{s}_i| \).

4) Calculation of \( d_i \)

Four \( d_i \) units are employed to calculate the PED of each node. The value of \( |e| \) has been previously calculated when performing direct enumeration for this node, however it costs more Silicon area to save the value in memory than to calculate it again with the enumerated \( \hat{s}_i \). Through VLSI synthesis, we find that the area of a register is similar with the area of a full adder of the same length. However, 16 registers will be needed (the same as the number of candidates in the list) if we want to keep the value of \( |e| \) for reuse, but if we calculate it again, only 4 adders are necessary.

In Fig. 8, two multipliers are employed, denoted as M1 and M2. M1 is a simple multiplication-addition converter as shown in Fig. 6, while M2 is a common multiplier for calculating the square value of \( |e| \). The product is then added to the PED of the parent node, i.e., \( d_{i+1} \). But only 12 bits of the result are assigned to \( d_i \). In the case that the product exceeds the maximum permissible value, \( d_i \) is simply set to the maximum permissible value.

5) Memory organization

Whenever a new node is chosen to be visited, \( \hat{s}_i \) of the node is stored in the path history cache, which will contain the final candidate symbols in the end of decoding. Because all the nodes in the top two levels are visited, their paths have fixed values, which can be directly hard-connected to wires to save silicon area. Therefore, only the paths in the lowest 6 levels need to be kept in memory. Totally \( 16 \times 6 \times 2 = 192 \) flip-flops are required by the path history cache.

Because of the breadth-first processing order, calculated \( b_i \) are not immediately used. They are stored in the \( b_i \) cache with 16 entries, the same as the number of candidates in the list.

The PED cache contains the PED of each visited node, which are used to calculate soft-information by LLR generator after finishing the tree traversal. The number of entries is the same as the number of candidates in the list.

The sizes of major registers are given in Table III, in terms of number of flip-flops (number of entries × data width).

![Figure 7. Direct enumeration](image)

![Figure 8. \( d_i \) calculation](image)

### Table III. Size of Registers

| Path history cache | \( b_i \) cache | PED cache |
|--------------------|----------------|-----------|
| \( 16 \times 6 \times 2 = 192 \) | \( 16 \times 12 = 192 \) | \( 16 \times 12 = 192 \) |

IV. IMPLEMENTATION RESULTS

A. Synthesis report

The four-nodes-per-cycle architecture is implemented in VHDLL, and is validated with ModelSim. It is then imported into Synopsys Design Vision to perform synthesis, on a 0.13 \( \mu \)m CMOS technology. The synthesis reports show that the implementation of FSD can work at a clock frequency of 400 MHz, with a Silicon area of 0.18 mm\(^2\). Area breakdown is shown in Table IV. We can see that the \( b_i \) units occupy a large portion of the overall area while the DE units and \( d_i \) units are relatively smaller.

The four-nodes-per-cycle architecture employs extra three units for each of the major arithmetic tasks, while requires the same number of registers compared with the one-node-per-cycle version. Also the control unit has approximately the same complexity in the two cases. Therefore, we can roughly estimate that the implementation of the one-node-per-cycle version would cost a Silicon area of

\[
\frac{(42.2\% + 16.7\% + 10.0\%) \times 4 + 31.1\%}{4} = 48.3\%\]

compared with the four-nodes-per-cycle architecture. It means that the throughput is increased to four times after adopting the four-nodes-per-cycle parallel architecture while the hardware cost is only doubled, showing that the efficiency is improved significantly (93.2\% in terms of the throughput/area quotient).

Thanks to the use of the CSA tree, the critical path after synthesis on the 0.13 \( \mu \)m technology dose not lie in the \( b_i \) unit. The two levels of 12-bit comparators in the DE unit are the architecture bottleneck in terms of delay and set the maximum clock frequency.

B. Throughput

The throughput can be denoted as

\[
\text{throughput} = \frac{f_c \times M \times N_f}{N_c},
\]

where \( f_c \) is the clock frequency, \( N_f \) is the number of cycles required to perform an entire tree traversal.

### Table IV. Area Breakdown

| \( b_i \) unit×4 | DE unit×4 | \( d_i \) unit×4 | Registers and control | Total area |
|-----------------|-----------|-----------------|----------------------|------------|
| 42.2\%          | 16.7\%    | 10.0\%          | 31.1\%               | 100\%      |
In our implementation for 16-QAM and 4×4 antennas, a total of \(4 + 16 \times 7 = 116\) nodes are visited in 29 cycles, an additional clock cycle is needed to start a new tree traversal, thus \(N_c = 30\) and the throughput is

\[
\frac{400 \times 4 \times 4}{30} = 213.3 \text{ Mbps.}
\]

In the system of 4×4 antennas, with 16-QAM modulation, 16 information bits are transmitted in each channel use. Therefore the throughput without consideration of clock frequency can be given by \((4 \times 4)/N_c = 0.53 \text{ bit/cycle.}\)

C. Comparison with other works

To evaluate the performance and efficiency of the implemented parallel FSD, we choose two recently published FSD implementations [10][11] and three implementations of other algorithms [3][4][8] for comparison, as shown in Table V. Both the FPGA implementations employ pipeline architectures. Although they are hard-output, the tree traversal parts are similar with the soft-output FSD. The throughput for FSD and K-best algorithms are all constant, while the throughput for depth-first SD is variable therefore the value is given at 20 dB and 12 dB SNR for [3], at 16 dB and 12 dB SNR for [8].

To facilitate comparisons, the Silicon area is converted into number of Gate Equivalent (GE). The Silicon area is divided by 6.05 ×10⁻⁶ \(\text{mm}^2\) (the area of two-input NAND gate with minimum drive strength in the technology library) to obtain GE. However, the hardware-complexity of FPGA implementation is difficult to be compared with Silicon area. So we re-synthesized the four-nodes-per-cycle parallel architecture on Xilinx XC2VP70 FPGA. Only basic hardware resources such as slices, flip-flops and LUTs are used, without particular optimization.

We can see that the speed of the four-nodes-per-cycle architecture on FPGA is much lower than the other two FPGA implementations. The reason for such a large difference is that the critical path after FPGA synthesis is in the \(b_1\) unit and it is due to the Wallace tree structure that is very inefficient for FPGA implementation. It has 24 logic levels, leading to a long delay path. However, the FPGA results are only used to compare the hardware-complexity.

The two FPGA implementations both employ pipeline architectures. They achieve very high throughput at relatively lower clock frequency. [10] visits all nodes in one level in each clock cycle, with a throughput of 4 bit/cycle, and [11] uses two cycles to complete the same task, with a throughput of 2 bit/cycle. They are much higher than the proposed four-nodes-per-cycle architecture, which achieves only 0.53 bit/cycle. However, the high throughput comes with very high hardware complexity, making them impractical for real applications.

The hardware cost of the proposed four-nodes-per-cycle architecture on FPGA is much smaller than the other two FSD implementations employing pipeline architectures, even if no particular optimizations for FPGA are applied and no special hardware resources such as multipliers and DSP blocks are utilized. The VLSI implementation is also compact and costs only 29.8 K GE on Silicon.

The soft-output K-best implementation MKSE in [4] achieves an acceptable throughput, however, at a high cost of hardware resource. Furthermore, the clock frequency reaches to only 200 MHz, on a 0.13\(\mu\)m CMOS technology. The hard-output SEE-SD implementation ASIC-II in [3] achieves higher throughput at 20 dB SNR and costs lower hardware resource compared with MKSE. However, the throughput is variable, and drops dramatically at lower SNR. For example, the throughput drops to 85.9 Mbps at 12 dB SNR and to less than 50 Mbps when the SNR is below 5 dB. Therefore the FSD and the K-best algorithms are more efficient compared with the depth-first SEE-SD in low SNR conditions, because of the constant throughput. The soft-output STS-SD implementation reported in [8] also achieves a variable throughput at a higher cost of hardware-complexity than the four-nodes-per-cycle architecture.

Although the other two FSD implementations achieve higher throughput, they also cost much higher hardware resources, which is definitely a burden for practical applications. Instead of pursuing high throughput, the four-nodes-per-cycle parallel architecture aims at reducing the

| Work                      | Four-nodes-per-cycle FSD | [10] | [11] | [4] | [3] | [8] |
|---------------------------|--------------------------|------|------|-----|-----|-----|
| Antennas                  | 4×4                      | 4×4  | 4×4  | 4×4 | 4×4 | 4×4 |
| Modulation                | 16-QAM                   | 16-QAM| 16-QAM| 16-QAM| 16-QAM| 16-QAM|
| Algorithm                 | FSD                      | FSD  | FSD  | FSD | K-best | Depth-first SD |
| List Size                 | 16                       | 16   | 16   | 5   | -    | -    |
| Technology                | 0.13 \(\mu\)m CMOS       | FPGA XC2VP70 | FPGA XC2VP70 | FPGA EP2S60F672C3 | 0.13 \(\mu\)m CMOS | 0.25 \(\mu\)m CMOS |
| Hardware Cost             | 29.8 K GE                | 3,438 slices (10%) | 12,721 slices (38%) | 13,743 ALUs (28.2%) | 97 K GE | 50 K GE |
|                           | 660 flip-flops (1%)      | 15,332 flip-flops (23%) | 1,412 flip-flops (2.94%) | 4 DSP blocks | 60 K GE |
|                           | 6,587 LUTs (9%)          | 16,119 LUTs (24%) | 160 multipliers (48%) | 160 multipliers (48%) | 71 MHz | 384 MHz |
| Max. Clock Freq.          | 400 MHz                  | 52 MHz | 100/150 MHz | 102 MHz | 200 MHz | 85.9 Mbps@12 dB |
| Throughput                | 213.3 Mbps               | 27.7 Mbps | 400/600 Mbps | 800 Mbps | 106.6 Mbps | 70 Mbps@16 dB |

TABLE V. Comparison between SD implementations
hardware-complexity while maintaining a relatively high throughput for most applications. Furthermore, the proposed four-nodes-per-cycle architecture is very flexible to be extended into an eight-nodes-per-cycle version in order to double the throughput.

D. Real vs. complex channel model

We adopted real valued channel model to implement the four-nodes-per-cycle FSD architecture. The effects of using real or complex models have been widely discussed in the literature [17]. For SEE-SD, smaller number of tree levels helps speeding up the updating of radius. Therefore the complex model needs to visit lower number of nodes, yielding higher throughput. For breadth-first SD algorithms, such as K-best and FSD, although the number of visited nodes is constant, the real model needs to visit approximately double of the nodes compared with the complex model with the same list size, because of the doubled number of tree levels. However, the higher throughput of complex model comes at the higher cost of hardware-complexity, because the real and the imaginary parts need to be processed concurrently. Therefore appropriate trade-offs are needed for different applications. The study in [17] suggests that the real valued model results into more efficient hardware implementation.

For FSD, complex model leads to higher degree of parallelism, but also results in higher hardware-complexity, as shown in [10][11]. The increased hardware-complexity mainly comes from two factors: approximately doubled arithmetic tasks for real and imaginary parts, and the child node enumeration from a larger number of child nodes. For example, in a system with 16-QAM modulation, the enumeration from four child nodes is relatively simple with a real model. But for complex model it becomes more complicated because the number of child nodes increases to 16. More multipliers and comparators are needed to perform the enumeration, not only increasing the complexity, but also slowing the speed.

To summarize, we can say that the adoption of real or complex channel model results into different trade-offs between throughput and occupied area. Moreover, these trade-offs also depend on the specific chosen algorithm to visit the tree. The choice of the real model in this work is motivated by the search for a low-area implementation.

V. CONCLUSION

In this paper we present a low cost implementation of the Fixed-complexity Sphere Decoder. FSD is very suitable for constructing iterative MIMO decoding systems and allows for highly efficient parallel architectures. We propose a novel four-nodes-per-cycle parallel architecture that exploits the breadth-first visiting order to improve throughput and shorten the critical path. Compared with the previously published pipeline architectures, the four-nodes-per-cycle architecture reduces the cost of hardware resources significantly while maintaining a high throughput, making it suitable for practical applications with balanced performance and hardware-complexity. It is also very flexible to be extended to meet the increasing requirement of new wireless communication standards.

ACKNOWLEDGMENT

The authors would like to thank Maurizio Martina for providing the C++ implementation of the Turbo decoder.

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