Test setup using DC metering approach for loss measurements of inductive components – principle, characterization, validation and application

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Abstract
Accurate loss estimation of magnetic components is crucial for power electronics engineers. Unfortunately, loss predictions remain a quite challenging task, as these depend on many parameters and manufacturers typically do not deliver a sufficient database for precise loss estimations. Therefore, this paper revisits an approach allowing loss measurements. In contrast to the most common used approach using alternating current (AC) waveforms to gain information about the losses, this approach relies on measuring direct current (DC) voltage and current. After characterizing the experimental setup, air inductors serve as references to validate the approach. In a first step, the test setup is used to extract core losses with and without DC bias by designing a special device under test (DUT) featuring low winding loss. Furthermore, this paper demonstrates that the test setup is also able to gain the overall losses of complete magnetic components by using the DC metering approach.

1 | INTRODUCTION

Nowadays, converter designs are subject to strong cost constraints or require highest efficiency and power density. Therefore, the designer of power electronic converters requires accurate loss estimations of all components in their daily work for optimizing their products. While calculating the conduction losses for power semiconductors is relatively simple, switching loss determination represents a quite challenging task. Due to the trend towards miniaturisation, this problem is not present anymore, as it requires high switching frequencies, which inevitably demand lossless turn-on (zero voltage switching, ZVS) of the power switches. However, the intended higher operating frequencies lead to more severe problems in the estimation as well as the AC characterization of losses in magnetics. Nevertheless, accurate loss predictions of magnetic components are vital in order not to oversize them on the one hand and to avoid overheating of the component under real application conditions on the other.

Losses in inductive components are particularly difficult to obtain, as different loss mechanisms exist: Winding and core loss. Winding losses can further be separated into RMS winding losses, skin and proximity losses [1]. The core losses resulting from the high frequency excitation of the magnetic material represents another part of the inductor losses. These depend on many parameters like frequency, excitation, temperature, and direct current (DC)-bias, making their estimation difficult [2]. Additionally, manufacturers do not deliver sufficient data and those are subject to tolerances [2]. The aforementioned arguments demonstrate that core loss measurements under real operating conditions are essential for optimized magnetic components.

There are numerous methods to obtain core losses during high frequency excitation, which are all accompanied by different advantages and drawbacks. In case of electrical measurements, impedance of ferrite chokes feature a large imaginary part and a comparably small real part leading to a very small phase angle, which has to be measured. Thus, already small phase errors introduced by the measurement lead to massive deviations of the resulting losses.

The most common approach, the alternating current (AC) metering method, needs a core under test (CUT) also called...
device under test, DUT) with two windings. In the 80s [3] and 90s [4] this approach was used, and also one decade later [5] it was studied. Recent publications [6, 7] show that core loss measurement is still a crucial topic. Winding one acts as the excitation winding and delivers the magnetic field strength. The second winding senses the voltage of the winding electromotive force (EMF) in order to gain the magnetic flux density within the core. Plotting flux density over field strength delivers the B-H-loop, whose area equals the occurring losses per cycle [3]. This approach allows to use arbitrary voltages as excitation [8]. Also sub loops within the B-H-loop are possible [9]. Furthermore, the impact of the DC bias of the flux density is studied using this approach [7]. As the core losses are temperature dependent, [10] introduces a test setup using the AC metering approach capable of using a specific core temperature. However, this approach requires an amplifier capable of high frequency and power rating as well as many other expensive equipment.

Another method represents measuring the impedance using an impedance analyser with an amplifier to excite the DUT [11], but phase angles close to 90° can cause large errors. Resonant techniques employ low loss capacitors in combination with the DUT to build a resonant tank and observe the damping to extract the losses [12].

Due to the difficulty in measuring power losses by electrical quantities, thermal measurements are applied in power electronics. On overview gives [13]. [14] compares two calorimetric methods which use different temperature measurement techniques. While [15] uses a calorimeter in thermal steady state, transient measurements, which use the temperature rise over time to determine core loss are also used [16]. Compared to the steady state calorimeter, transient calorimeters can shrink the measurement time, since the DUT does not have to reach thermal steady-state [16, 17]. In addition, thermal measurements also allow arbitrary voltage excitations for the magnetic device [16]. Nevertheless, thermal measurements cannot be used in a meaningful way because they are difficult in characterizing and measurements are very time-consuming [2].

Another promising approach for measuring losses in inductive components represents the DC metering approach introduced more than 20 years ago [2, 18] takes up this method years later and thus, shows that it is a promising approach. This method relies on measuring the input power of a half-bridge circuit where the inductor of the accompanied LC output load represents the DUT. Furthermore, this approach promises accurate results while only relying on affordable equipment typically available for power electronics engineers.

The consideration of the above given arguments and the cited literature shows that in the past the power electronics community had with the AC-metering approach a good measurement principle at hand that serves their needs to determine losses of magnetic components. However, for a long time researchers applying this principle also point out that the usefulness will diminish when switching frequencies enter the range of several hundred kHz or even MHz [7, 19]. With wide bandgap semiconductors becoming widely available a lot of newly discussed applications operate in this frequency range. The need to find a new tool for power electronics engineers to be able to measure the losses for future applications at even higher switching frequencies calls for a new measurement principle whose accuracy does not suffer at higher switching frequencies. The DC-metering approach represents the most promising candidate to become the new standard for measurement of losses in magnetic components.

To really appreciate the future impact of the DC-metering approach, a short discussion of existing reasons to measure losses in magnetic components is needed, starting with a typical engineer designing power electronic equipment in short run. Typically, the magnetic components for such design tasks have to be chosen from the shelf. Unfortunately, the datasheets typically do not deliver enough information to estimate the losses for the application under investigation. The engineer faced with this situation would be fully satisfied if the measurement setup delivers the total losses of the magnetic component close to real operating conditions. The DC-metering approach perfectly suits this purpose as will be shown by two examples in Section 5.3. The second typical scenario occurs in case of designs for products for the mass market. Here customized magnetic components have to be designed. The optimization requires knowledge about the winding as well as core losses. While for winding losses numerical tools like the finite element method (FEM), boundary element method (BEM), etc. are used, the core losses are obtained from empirical formulas derived from core loss measurements. However, the datasheets deliver only core losses for sinusoidal excitation without DC-bias. Again, the DC-metering approach provides in combination with FEM/BEM simulations for the winding losses the required core losses under real operating condition including DC-bias as shown in Sections 5.1 and 5.2. This directly leads to the third application scenario of the proposed test setup. This application aims at generating coefficients for widely used core loss models like Steinmetz and its extensions [17, 20–22]. An alternative approach to predict core losses tries to obtain and improve hysteresis models, like Jiles-Atherton [23] or Preisach [24], for high frequencies, under DC-bias, etc. The DC-metering approach perfectly supports the first approach (Steinmetz) by directly providing the core loss data needed. The second approach (Jiles-Atherton and Preisach) requires information that cannot directly be derived from the DC-metering approach. Nevertheless the DC-metering approach can play an important role for the verification of hysteresis models as well by providing an independent second method for verification of core loss results obtained from optimized hysteresis models. The usefulness of the DC-metering approach for all these different needs clearly demonstrates its impact on determination of losses in magnetic components in the future.

This fact is also supported by the literature, as the DC-metering method is also applied to switching loss measurements, where all other losses within the circuit, including the inductor, are accurately assessed [25, 26]. The switching losses can then be gained by the input power and all other losses within the circuit [27]. Thus, for switching loss measurement, the DC-metering approach starts to replace the conventional double pulse test, which is a kind of AC-metering.
However with the respect of losses in magnetic components, [2, 18] only introduce the DC-metering approach with its basics and some fundamental requirements. In order to be able to apply this promising approach profitably for the use cases mentioned above, further details of the approach need to be considered, which are missing in the literature so far. Unfortunately the earlier contributions lack a study on the resulting accuracy depending on the used components and thus the reader was not able to make proper component choices. Even worse, literature delivers no validation of the DC-metering approach which is crucial for generating confidence in this measuring principle. Last but not least a real practical realization for a given specification is missing which would be extremely helpful as a starting point for other measurement tasks at hand. The technical contribution of this paper addresses these important missing aspects enabling optimised measurement setups for future challenges in the loss determination of magnetic components. This is achieved by characterizing a test setup suitable for delivering losses of magnetic components used for industrial, information technology and consumer products. Widely used converters in this relevant field of application such as the boost power factor correction or DC/DC converters like buck or flyback typically utilize a maximum voltage of 400 V. For this given practical specification the study comprises a detailed description of the requirements on the components used as well as a careful selection of all components and their accurate characterization. Since the test setup should deliver reliable results, an uncertainty analysis is inevitably required. Moreover, a validation of the results must be carried out. Consequently, the paper has the following structure:

At first, the DC metering approach is introduced and reviewed. After that, Section 3 describes the test setup used within this paper with all its components, loss estimations, and the results from a detailed uncertainty analysis, followed by Section 4 which shows the verification of the proposed test setup. Section 5 demonstrates the wide applicability of the setup by conducting different loss measurements with inductive components. The paper also includes a discussion of the measuring principle and the test setup.

2 OPERATING PRINCIPLE

The method is based on measuring the input power of a half-bridge circuit to determine the losses within an inductive component. Switching the power semiconductors of the half-bridge with the intended switching frequency circulates magnetizing current through the DUT. Using dramatically oversized bypass capacitors and half-bridge switches minimizes the losses of the circuit. Therefore, measuring the input power of the test setup allows for gaining the losses occurring within the DUT, if all other loss components of the circuit are accurately known and subtracted from the input power. This approach is already introduced by [2], using conventional metal oxide semiconductor field effect transistors (MOSFETS) for building the circuit. [18] describes this approach as well, but gives only little detail regarding component selection and implementation. [2] only describes the test setup and the requirements for the components used in the test setup. It presents no practical implementation and does not perform any validation of the test setup. An uncertainty analysis is also missing. Furthermore, no application examples are provided. Thus, this paper focuses on these missing aspects, due to their importance for a wide acceptance of this accurate and affordable measurement method.

Since this approach relies on low losses of all components within the circuit, recent developments in power semiconductors, like silicon carbide (SiC) and gallium nitride (GaN), make this method an even more promising candidate. GaN high electron mobility transistors (GaN-HEMTs) offer much lower on-state resistance, which directly affects the losses occurring within the circuit. This boosts the accuracy of this approach. Ensuring ZVS allows for accurate loss predictions. GaN switches are well suited for this task, as they exhibit significantly reduced device parasitics and therefore the occurring half-bridge voltage waveform is much closer to an ideal rectangular one.

Furthermore, the test setup relies on simple DC-measurements with digital voltmeters. Therefore, this approach exhibits a significant advantage compared to the AC metering approach, which requires precise and costly instruments to measure the voltage and current waveforms over time. For that purpose, normal oscilloscopes cannot be used as the input stage does often not meet the requirements [7]. In contrast, the DC metering approach uses simple DC measurements with digital voltmeters, which are typically present in each power electronics laboratory. For this reason, the approach presented here is also interesting for small laboratories.

The test setup, originally designed to measure core losses of ferrite cores, is also capable of measuring losses of complete inductive components under their specific operating point. Thus, the DC metering approach allows to show if an inductive component (self-made or bought off the shelf) for a power converter can handle the intended current ripple at the applied excitation frequency of a specific application.

3 TEST SETUP

Figure 1 shows the circuit diagram of the proposed inductor loss tester employing the DC metering approach. It mainly consists of a half-bridge circuit with a LC load. One terminal of the DUT is directly attached to the half-bridge midpoint. The half-bridge power semiconductors switch with the intended switching frequency and duty cycle, resulting in a triangular flux density in case the DUT exhibits an air gap. As a result, a triangular current occurs at the DUT. The magnetizing current of the DUT enables turning on the semiconductors under ZVS, thus eliminating turn-on losses. The magnetizing energy of the DUT allows for commutating the current from one half-bridge switch lossless to the other. The proposed idea requires ZVS because it is very complicated to accurately predict switching losses. In order to avoid turn-off losses, the semiconductors are turned off fast and hard enough to hold the gate voltage below the threshold (snubbed turn-off). For the capacitors $C_i$ and
$\text{Figure 1}$ Test setup for inductive components using DC metering approach

$\text{Figure 2}$ PCB with probes and instrumentation of the test setup

$C_i$ dramatically oversized components featuring low losses are used.

A power supply provides the input voltage $U_{\text{source}}$ (and power) of the test setup. Two filters (filter 1 and filter 2) interconnect the power supply and the half-bridge circuit. Since already small common or differential mode disturbances can negatively affect the measurement, filter 1 prevents disturbances of the power source $U_{\text{source}}$ from reaching the digital voltmeters measuring the DC voltage and DC current. In order to keep switching noise, generated by the half-bridge circuit, away from the input power measurement, filter 2 is inserted. Figure 2 shows the test setup including the instrumentation and personal computer with MATLAB.

### 3.1 Specification

The specification of the test setup should be matched to the intended final applications of the converters where the DUTs are designed for. Since it relies on low and well characterized losses of the power stage, especially, when low voltage applications are addressed, the semiconductors and capacitors should be low voltage components as well. These feature, in particular, lower losses than high voltage components and thus guarantee precise results of the approach. This specification stems from the applications that are typically present in the author’s laboratory. Since many converters are single phase grid applications, for example, used in industrial and consumer products,
Loss calculation

Theoretical analysis of the setup and its limits

Now that the specification is known, one can proceed with the theoretical analysis of the test setup. The analysis is done assuming a lossless converter in steady-state. The voltage across the capacitor $C_g$ can be gained using Kirchhoff’s law and the fact that in steady-state of the converter $\hat{u}_L = 0$. Therefore, the capacitor voltage $U_c$ equals $\hat{u}_{hbl}$, which is the averaged half-bridge voltage. The averaged half-bridge voltage $\hat{u}_{hbl}$ is the input voltage multiplied by the duty-cycle $\delta$:

$$U_c = \hat{u}_{hbl} = U_c \delta$$  

Assuming constant voltages at the input and the output allows for deriving the current ripple of the DUT $\hat{i}_{L,+} = \hat{i}_{L,-}$ for a given operating point. In order to do so, the fundamental equation of an inductance is applied:

$$\mu_L = L_{DUT} \frac{di_L}{dt}$$  

The steady-state analysis of the converter delivers the current ripple:

$$\hat{i}_{L,+} - \hat{i}_{L,-} = \frac{U_i (1 - \delta) \delta}{L_{DUT} f_s}$$  

Figure 3 displays the theoretically achievable current ripple of the test setup depending on the switching frequency $f_s$ and inductance of the DUT for a duty-cycle $\delta = 0.5$. Since Figure 3 uses the maximum input voltage of 400 V, it is the maximum inductor current ripple that can be set for a given frequency and inductance. From the figure it can be seen, that, due to the limited input voltage, the current ripple shrinks with increasing switching frequency and inductance. Possible adaptations of the measurement setup discussed in Section 6 allow to apply the DC-metering approach for other operating ranges (with lower and higher input voltages) as well.

Input power measurement

As already mentioned, the proposed test setup relies on simply measuring the DC input power $P_i$ of the circuit instead of logging the AC waveforms of the DUT. Typically, measuring DC currents and voltages allows for very accurate and reliable results [2, 28]. Compared to the AC metering approach, the instrumentation is very easy to handle and affordable, as the power loss measurement requires only two digital voltmeters [2]. One digital voltmeter directly measures the input voltage $U_i$, whereas a voltage measurement ($U_{DC,Shunt}$) at a shunt $R_{DC,Shunt}$ delivers the current information $I_i$. Usually, DC voltages can be measured much more precisely than currents, thus this test setup uses voltage measurement [28]. In steady-state, the input voltage source only supplies the power losses of the circuit. The corresponding small input current allows a few ohms for the current shunt delivering a reasonable voltage for the voltmeter and thus a good signal to noise ratio. Of course, the shunt applied must be characterized carefully with sufficient accuracy to achieve high-precision current measurement. Equation (4) delivers the input power $P_i$ of the circuit by multiplying the input voltage $U_i$ by the input current $I_i$.

$$P_i = U_i I_i = U_i \frac{U_{DC,Shunt}}{R_{DC,Shunt}}$$  

Measuring the shunt resistance with a milliohmmeter [29] employing kelvin source connection directly at the terminals of the shunt ensures accurate measurements. The measurement delivers a resistance of $R_{DC,Shunt} = 9.99 \Omega \pm 140 \text{ ppm}$ [29]. As the shunt does not heat up during operation of the circuit, temperature correction is not necessary.

Loss calculation

As already mentioned, the losses of the DUT $P_{V,DUT,BC}$ are determined by the difference of the measured input power $P_i$ and the estimated power stage losses $P_{V,PS}$ resulting from the components used:

$$P_{V,DUT,BC} = P_i - P_{V,PS} = U_i I_i - (P_{V,F} + P_{V,S} + P_{V,G} + P_{V,G})$$  

$P_{V,PS}$ comprises all losses resulting from the power stage of the circuit including filters $P_{V,F}$, half-bridge $P_{V,S}$, and bypass...
capacitors ($P_{V,C1}$ and $P_{V,C2}$) except for the DUT's losses. To determine these loss components, the DUT's current is measured. In order to prevent that the driving losses of the power semiconductors and the power consumption of the logic circuitry affect the loss measurement, an external voltage supply powers these parts of the circuit. The following sections will describe all other shares of losses step by step in detail.

The parasitic resistors shown in Figure 4 represent the major loss mechanisms. Oversized semiconductors and capacitors with negligible temperature dependence minimize these losses so that the small errors remaining in the loss prediction are negligible compared to the losses of the DUT.

3.4.1 DC-filters ($P_{V,F}$)

Of course, the input current causes losses in filter 1 and filter 2. As the losses occurring in filter 1 do not contribute to the input power measured, these losses do not need to be considered. Nevertheless, losses caused by filter 2 $P_{V,F}$ should be accurately assessed. As both filters and the input capacitor $C_i$ prevent high frequent currents generated by the power stage from flowing in this path, only the DC current losses must be calculated. Experiments show that using a common-mode choke in conjunction with the input capacitance is sufficient to keep high frequent currents away from the DC measuring instruments. Using a milliohmeter [29] delivers the DC resistances of both windings of the common mode choke $R_{F,2,1}$ and $R_{F,2,2}$, which are 4.9 mΩ for each the positive and negative supply path. The losses arising within filter 2 can be gained using:

$$P_{V,F} = I^2 (R_{F,2,1} + R_{F,2,2})$$  \hspace{1cm} (6)

3.4.2 Conduction loss estimation of GaN-HEMTs

As the power semiconductors of the half-bridge turn on under ZVS, no turn-on losses occur. Snubbed turn-off ensures negligible turn-off losses [30]. Consequently, only the conduction losses $P_{V,S}$ must be accurately calculated, assuming negligible losses due to leakage currents in off-state. As already mentioned, the measurement procedure presented here relies on the one hand on low losses the power stage which on the other hand should be well predictable. Taking the first requirement into consideration directly leads to the use of wide bandgap components and especially GaN-devices with their advantage of extremely low on-state resistance. Having a look at the second point, the literature regarding GaN-HEMTs alerts, since these devices can exhibit increased on-state resistance during switching operation compared to DC resistance [31, 32]. This results from charge trapping effects within the device. In order to satisfy both requirements, the device's behaviour must be studied carefully and the on-state resistance should be quantified accurately for the intended GaN-devices. Therefore, measurements are carried out for the complete operating range of the semiconductors. A special test setup with a drain-source voltage clamping circuit determines the on-state resistance of the GaN-HEMTs [31, 33]. As this paper here focuses on loss measurements of magnetic components, only the results needed to predict conduction losses of the semiconductors are presented.

The study shows that the increase of on-state resistance mainly depends on the drain-source voltage of the device and therefore Figure 5 depicts this dependency. It shows the normalized (to the static on-state resistance as a function of the component temperature given in Figure 6. For describing the measured on-state resistance versus temperature (or the datasheet curve), a curve fit can be used (e.g. an exponential function):

$$R_{dc,on}(T_C) = R_{dc,on}(T_C) e^{b(T_C)}$$  \hspace{1cm} (7)

For the device studied here, a curve fit delivers $a = 0.836$ and $b = 0.007$ and the curve fit is displayed in Figure 6 as well (normalized to $R_{dc,on}(25 \degree C)$).
The increase in temperature mainly affects the static on-state resistance of these components [34, 35]. The results show that the increase of on-state resistance due to charge trapping effects is not as large as sometimes reported in literature and therefore, the components can be used here.

The conduction losses can be gained using the RMS value of the current $I_L$ through the GaN-HEMTs and the on-state resistance depending on the device voltage $u_{DS}$ and temperature $T_C$:

$$P_{V,S} = I_L^2 R_{ds,on}(u_{DS}, T_C)$$

(8)

Generally, the conduction losses of the half-bridge switches should be minimized and assessed accurately. The aforementioned results show that for these devices the requirements of the DC-metering method of low and well predictable losses are fulfilled. In principle, instead of accurately measuring the on-state resistance of the devices, also theoretical models describing the device’s conduction loss mechanisms can be used in case these show sufficient accuracy. It is important to keep in mind that production tolerances (and batch to batch variations) can lead to discrepancies between the loss prediction and the losses actually occurring. Thus, measurements are the best way to achieve highly accurate results.

3.4.3 Losses of input and output capacitors

Regardless of whether applying the best capacitors or not, the ripple current causes losses within both capacitors. These must be minimized and accurately determined as well and can be addressed by a series resistor (equivalent series resistor, ESR) for each capacitor. As not only the capacitors itself, but also the printed circuit board (PCB) tracks contribute to the losses, considering the PCB is necessary. Thus, small signal AC resistance measurements of the output circuitry, from the DUT connection through the output capacitor up to the node of the lower half-bridge switch, are performed. An impedance analyser delivers $R_{Co}(f)$. As the fast Fourier transform (FFT) spectrum of the current flowing through the output circuitry has components at the switching frequency and its harmonics, the frequency dependent resistance of the output circuitry $R_{Co}(f)$ must be considered. Equation (9) delivers the occurring losses, where $i_{L,FFT}(f)$ represents the FFT of the inductor current $i_L$, which equals the current flowing through $C_o$. This equation uses harmonics of the current and the corresponding resistance to gain the losses of the output circuitry. $n_{OS}$ is the number of harmonics which are considered for the loss estimation. A study shows that setting $n_{OS}$ to 10 is sufficient for an accurate loss prediction.

$$P_{V,Co} = \sum_{n=1}^{n_{OS}} \left( \frac{i_{L,FFT}(nf)}{\sqrt{2}} \right)^2 R_{Co}(nf)$$

(9)

Figure 7 depicts the frequency dependent resistance of the output circuitry including the error bars based on the specification of the manual of the impedance analyzer [36].

Using the same approach for the input circuitry delivers $R_{Ci}(f)$ (shown in Figure 8), which causes the losses of the input side. As the operating range is from 25 up to 400 kHz, the low frequency AC resistance of the input capacitor is not relevant for loss calculation. Adapting Equation (9) to the input circuitry, supplies the losses of the input side. When comparing the small signal series resistance of the input circuitry (shown in Figure 8) and the output circuitry (Figure 7) it is noticeable that they have completely different shapes. These result from the different component technologies used for realizing both
capacitances. For the input capacitance, a combination of electrolytic capacitors with ceramic capacitors close to the switching cell is used, whereas a film capacitor builds the output capacitor.

### 3.5 Instrumentation

The described measurements require suitable instrumentation. There are different tasks to be performed: First, the DC input power measurement, which has the highest requirements regarding accuracy. Therefore, two digital voltmeters for the input voltage $U_i$ and the voltage across the input current shunt ensure high precision. The second measurement task within this test setup is to verify the operating point of the DUT. A current probe accompanied by a digital storage scope measures the current waveform exciting the core material $i_L$. Stable triggering is necessary in order to be able to employ waveform averaging of the periodic current waveform. Thus, a passive voltage probe measures the half-bridge voltage $u_{ib}$, which allows stable triggering. Table 1 shows all used instrumentation.

### 3.6 Setting the operation point

Before starting the loss measurement, the intended operating point must be set. The half-bridge switches are controlled by a microcontroller, which is linked to a personal computer via MATLAB. Assuming a symmetrical (without DC bias) triangular excitation current waveform $i_L$, the operating point is specified by the inductance of the DUT $L_{DUT}$, switching frequency $f_s$, duty cycle $\delta$, and current ripple $\tilde{i}_{L+} - \tilde{i}_{L-}$ (difference between maximum $\tilde{i}_{L+}$ and minimum $\tilde{i}_{L-}$ inductor current during one switching period). MATLAB sets the switching frequency and duty cycle via the microcontroller of the test setup. The ripple current depends on the input voltage of the test setup, which must be adjusted to reach the intended ripple current value. Rearranging Equation (5) from the theoretical analysis in Section 3.2 delivers Equation (10), which allows for approximately calculating the input voltage required for the operating point given. If desired, an iterative process can adjust the operating point with high accuracy.

$$U_i = \frac{(\tilde{i}_{L+} - \tilde{i}_{L-}) L_{DUT} f_s}{(1 - \delta) \delta}$$

### 3.7 Dead time optimization

During ZVS transitions, the GaN-HEMTs enter reverse conduction when the voltage across the switch, which turns on next, passes the zero voltage level and the dead time has not been elapsed. As the reverse voltage across this type of semiconductor massively exceeds that of its on-state, reverse conduction must be avoided in order to achieve low and well predictable losses. It is difficult to obtain the reverse conduction losses, as reverse conduction duration (typically in ns-range) must be determined accurately. Therefore, after setting the operating point, the test setup optimizes the dead time $t_{dead}$ of the half-bridge in order to minimize this effect. The half-bridge switch should be immediately turned on, when the voltage across it reaches zero (ZVS). Besides reverse conduction the dead time optimization routine must prevent the half-bridge switches to turn on hard, which induces massive losses due to capacitive charging. At first, an initial dead time (which is too large) is set. For this dead time, the power loss is evaluated from the two digital voltmeters. After that, the routine slightly reduces the dead time and the routine reads the power loss again. The routine reaches the optimal dead time when the input power approaches its minimum. For performing the measurements, the dead time gained by the optimization method is used to ensure accurate measurements. The setup must be operating until it reaches thermal steady-state of the DUT and the half-bridge switches before starting dead time variations and reading power loss.

### 3.8 Power loss error calculation

This section describes a power loss error calculation, also called uncertainty analysis. Error propagation allows for calculating the total error of Equation (5). Table 2 displays for one operating point (also given in the table) the resulting errors and their impact on the losses. The occurring errors are calculated based

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**Table 1** Instrumentation of the test setup

| Signal | Range | Instrument |
|--------|-------|------------|
| $U_i$  | 0–400 V | Digital voltmeter FLUKE 289 |
| $i_L$  | 0–400 V | Passive voltage probe P6139A 10:1, Tektronix DPO7000 [37] |
| $i_{ib}$ | 0–400 V | Current probe TCPA300 [38], Tektronix DPO7000 [37] |

**Table 2** Example error calculation for one operating point

| Symbol | Value | Tolerance | Resulting loss tolerance |
|--------|-------|-----------|-------------------------|
| $f_s$  | 200 kHz | – | – |
| $\tilde{i}_{L+}$ | 10 A | – | – |
| $\delta$ | 0.5 | – | – |
| $t_{dead}$ | 40 ns | – | – |

$\Delta P_{J,DUT,BC}$
on the technical specifications of the applied instruments. As can be seen from the table, the main uncertainties result from the small signal AC characterization of the input and output circuitry $R_G(f)$ and $R_C(f)$ used in the test setup. As already mentioned, input power measurement exhibits very small errors, as the test setup relies on DC measurements. The operating point used for exemplarily calculating the errors is depicted in Figure 12 for a peak current of $\tilde{i}_{L+} = 10$ A and exhibits losses of the DUT of $P_{V,DUT,BC} = 9.76$ W. Thus, the setup yields for this operating point an accuracy of 3.3%.

41 VERIFICATION OF THE TEST SETUP

In order to ensure proper measurement results with the proposed test setup, validation is necessary. The applied validation measurements use air inductors. Due to the absence of ferrite material, which normally introduces nonlinearity to the device, the series resistance of air inductors does not depend on the excitation level (assuming constant temperature). This linear, frequency dependent series resistance $R_L(f)$ can be accurately determined by small signal impedance measurements. Finally, using FFT of the inductor current $i_{L,FFT}(f)$ in conjunction with $R_L(f)$ yields a calculated reference value for comparison with the measured results. Adapting Equation (9) by replacing the small signal resistance $R_C(n \cdot f_s)$ by $R_L(n \cdot f_s)$, delivers the losses $P_{V,DUT,ref}$ occurring within the DUT, when operating the air inductor within the test setup. The losses $P_{V,DUT,ref}$ gained by $i_{L,FFT}(f)$ and $R_L(f)$ should match the losses delivered by the test setup $P_{V,DUT,BC}$ using the DC metering approach. Of course, deviations of the two results will occur, which are due to the errors accompanied with both approaches. Drawing this comparison for the complete operating range of the test setup validates the approach and thus ensures proper results. Using two inductors with different inductance values allows for characterizing the complete operating range. Figures 9 and 10 depict the AC series resistance and the corresponding error bars of the two aforementioned air inductors serving as reference [36].

The first one (air inductor I) has an inductance value of $L_1 = 7.5$ µH and therefore fits for the operating range with input voltages up to 120 V. For higher voltages ($U_i = 120–400$ V) air inductor II with $L_2 = 100$ µH serves as reference. The design of the air inductors aims at the following characteristics: They should deliver losses in the same range as the intended DUTs for a given operating point. Furthermore, they must exhibit low parasitic capacitances to minimize ringing during switching transients and to ensure that the measured inductor current is mainly caused by the inductive and not by the capacitive behaviour of the DUT. Figures 11 and 12 depict the measurement results $P_{V,DUT,ref}$ gained by impedance measurements in combination with the FFT of the inductor current and the losses delivered by the test setup $P_{V,DUT,BC}$. Both figures prove good correlation between the curves showing the dependence on the switching frequency $f_s$ and peak current $\tilde{i}_{L+}$ using air inductor I. Figures 13 and 14 exploit air inductor II and determine the same losses for both approaches with sufficient accuracy when sweeping the duty cycle $\delta$ and the peak current $\tilde{i}_{L+}$. All parameters of the studies are given in the caption of the corresponding figure.
Typically, the power electronics designer uses the Steinmetz equation (or a modified one) in order to estimate core losses by simulation [21, 20, 39]. A lot of work has been done to improve the accuracy and applicability of Steinmetz equation [22, 40–42]. But regardless of the approach used, gaining accurate core loss data is essential. Therefore, after the successful validation of the proposed setup, this section presents three application examples for the test setup the paper deals with. These studies show the wide applicability of the approach, as various loss measurements are conducted. First measurements study core losses of a gapped RM core, as these gapped cores are often used in power converters. The study includes measurements with symmetrical flux density, which exhibits no DC-bias, as well as measurements under DC-bias. After that, measurements of total losses of real magnetic components follow, which were available in the author’s laboratory. Of course, due to the broad applicability of the test setup, any other component, whether bought off the shelf or specifically designed, could be used as well.

5.1 Symmetrical flux density (no DC-bias)

At first, studies with symmetrical flux density (no DC bias) are performed. Typically, the power electronics engineer uses simple equations. Rearranging the definition of the inductance using the flux linkage delivers Equation (11). This equation assumes a homogenous flux density in the core to estimate saturation and to gain the flux density swing for Steinmetz equation, since it is a quite complex task to determine the real field distribution within a magnetic core.

$$\hat{i}_{L+} = \frac{NA_e}{L_{DUT}} \hat{B}$$ (11)

There \( N \) represents the number of turns, \( A_e \) the effective core area, and \( L_{DUT} \) is the inductance of the DUT. \( \hat{i}_{L+} \) equals the required peak current to reach the intended peak flux density \( \hat{B} \). For this example here, Figure 15 shows, gained by boundary element method, the field distribution within the core, which is inhomogeneous [43] and thus does only roughly meet the assumptions of Equation (11) [44]. The shape of the core for simulation results from the transformation from 3D to 2D [45]. Conventional core loss measurements use thin and small toroidal cores, since these feature nearly homogenous flux density. However, due to their shape, in cores applied to power
electronics no homogenous flux density results. The described setup perfectly suits for this core shapes, since it provides the core loss for the inhomogeneous field distribution and thus delivers results closer to real applications for the intended core shape and size. Since user needs to apply Equation (11) to calculate the required current from the intended flux density as well, the results from the DC metering approach reflect the real configuration. Thus, the same assumptions apply for both calculations. Therefore, the results obtained by the setup are directly useful for the designer of a converter.

However, to ensure proper extraction of the core losses, the DUT must be appropriately designed. Again, the boundary element method delivers the core as well as winding losses \( P_{\text{V,w,wind,BC}} \) for a given winding and core configuration [43, 44]. This first step uses datasheet parameters for permeability and geometry to design the component to gain the magnetic field distribution within the coil former at the position of the winding. Using litz wire with small strand diameter for the winding minimizes skin and proximity losses. Avoiding placing turns in regions with high magnetic field strength (fringing field of the air gap) further decreases proximity losses. Choosing a litz wire with significantly oversized copper area (compared to the inductor current) minimizes RMS losses as well. Since this first study is not focused on measuring the overall losses of a complete optimized inductive component for real applications, but rather on determining the core losses of a specific core type and material under given operating conditions, it is reasonable to select the best litz wire and optimize the winding design in order to achieve small and well-predictable winding losses. Following this routine, the winding losses \( P_{\text{V,w,wind,BC}} \) are relatively small and well known compared to the core losses and thus allows accurate core loss predictions.

The described example measures a gapped (air gap length \( \ell_g = 400 \, \mu \text{m} \)) RM12 core with the core material N87 [46]. The winding comprises five turns with litz wire of strand diameter 0.1 mm and 45 strands. The winding is built as a single layer and the turn positions are fixed in the coil former, to ensure that the winding arrangement corresponds to the simulated configuration.

Figure 16 shows the measured losses \( P_{\text{V,DUT,BC}} \) and the simulated winding losses for the given winding configuration in combination with the measured inductor current, which ensures comparable operating points. The winding temperature is fed into the simulation as well to ensure proper results for the winding losses. Subtracting the winding loss \( P_{\text{V,w,wind,BC}} \) gained by simulation from the overall losses \( P_{\text{V,DUT,BC}} \) delivers the core loss \( P_{\text{V,core}} \). The core losses increase more than quadratically with the flux density, what seems to be reasonable [1]. However, Figure 16 also reveals the peculiarity of this measurement method. Each operating point exhibits a specific temperature due to the amount of power loss generated by the chosen conditions. However, this scenario resembles the normal operation of magnetic components in the intended application. Heating or cooling the core allows for emulating the conditions during real operation. Furthermore, by placing the CUT in an oil bath, measurements at constant temperature could be conducted as well.

5.2 | Flux density with DC-bias

Besides applying symmetrical magnetic flux density to the DUT, measurements with DC-bias are also possible. Many applications in power electronics generate flux density with DC-bias, which makes these measurements necessary. Typical converters featuring this are the well-known flyback or buck. For the DUT, the same requirements (low and well known winding losses) as in the previous section apply. As the proposed test setup relies on ZVS and input power measurement, DC-bias cannot be directly generated by the test setup. In order to excite the DUT with a DC in combination with an AC flux density, the test setup generates the AC part and a second winding applied to the DUT injects a DC current resulting in DC flux density. Due to the air gap, the DC current allows for programming the desired DC flux density [7]. Applications with DC-bias typically need cores with air gap and well defined magnetizing inductance. Injecting the DC current requires additional external instrumentation. Figure 17 shows the circuit for DC injection, which comprises a DC voltage source with an external resistor converting it to a
constant current source. This circuitry feeds a current $I_{DC}$ into the second winding of the DUT. As the DUT has two windings on the same core, both currents and secondary current, excite the core. However, the DUT in principle acts as a transformer. Thus, a part of the primary side current could flow to the secondary side instead as desired through the magnetizing inductance. In order to prevent this, a huge inductor ($L_{DC} \approx 4 \text{ mH}$) in the circuitry inserts a high impedance for the high frequency ripple current. This leads to a negligible small AC current on the secondary side. Thus, the primary side AC current excites the core material of the DUT. The inductor $L_{DC}$ should feature low parasitic capacitance to avoid high frequency bypass of the inductor. Figure 18 depicts the ripple current on primary side $i_L$ and DC current on secondary side $I_{DC}$ for one switching period. This waveform shows that the huge inductance on the secondary side prevents the AC current to flow on the secondary side, as the secondary side waveform exhibits a constant current. The primary current shows DC-offset free triangular waveform, as required for ZVS. These waveforms display, that the secondary winding excites the core by a DC flux density and the primary side injects an AC flux density with triangular waveform. Therefore, these waveforms prove that the conducted experiments meet the assumptions.

The DUT with the magnetizing inductance $L_m$ comprises a P26/16I pot core made of N87 with an inner leg air gap of 150 $\mu\text{m}$ [46]. The coil former has three equally sized chambers and only the lower holds the two windings in order to avoid proximity losses caused by the fringing field of the air gap. Figure 19 depicts the practical realization of the DUT chosen for DC-bias measurements. Besides the primary and secondary winding, also wires of thermocouples for core and winding temperature measurements are placed.

Each winding consists of three turns where the inner layer is the primary side and the outer one the secondary. This configuration results in a primary side inductance of 7.48 $\mu\text{H}$. Figure 20 shows the results for core loss measurement under DC-bias. The procedure to gain the curves in Figure 20 is as follows. In the first step, the DUT operates under the intended operating point until thermal steady state. Then, again employing the simulation tool for magnetics [43, 44], delivers the winding losses $P_{V,wind}$ for the operating point using the current waveforms measured by the test setup. Subtracting these from the overall losses of the DUT $P_{V,\text{DUT,DC}}$ delivers the DUT’s core losses $P_{V,\text{core,corr}}$ depicted in Figure 20. As the high frequency primary side current induces proximity losses on the secondary side, these must be taken into account as well. The RMS losses on the secondary side are supplied by the DC voltage source and therefore, they must not be subtracted from the overall losses. As a result, the winding losses $P_{V,\text{core,corr}}$ include the RMS and skin losses of the primary side as well as all proximity losses (primary and secondary side).

Since the device temperature in the study changes due to the occurring losses and the core losses are temperature dependent as well, the temperature effect must be compensated in order to gain measurement data showing only the influence of DC-bias of flux density on the core loss. Therefore, Figure 20 introduces $P_{V,\text{core,corr}}$ which represents the core losses $P_{V,\text{core}}$ converted to 100 $^\circ\text{C}$ using the temperature dependency given in the core material’s datasheet [46].

Figure 20 reveals that the core losses increase with rising DC-bias of the flux density. The losses with a DC-bias of $B_{DC} = 115 \text{ mT}$ is approximately 13 % higher than applying only AC excitation to the core. These results demonstrate that accurate core loss predictions for inductive components require measurements especially in case of power electronic converters.
exhibiting a DC component in their magnetizing current, since this information is not included in the datasheet.

5.3 Complete components

When the power electronics designer needs to buy inductors off the shelf, he is restricted to the information provided by the manufacturers. However, this data basis does not deliver all information necessary to perform a reliable prediction of the losses for the intended switching frequency and ripple current. Often the information available for loss calculation is even restricted to only the DC-resistance of the inductors. If in the intended application other loss components than the DC losses are present, the developer requires a possibility to obtain the missing information. The proposed test setup allows designers of power electronic circuits to gain accurate loss data even under conditions close to the final usage. In addition, the setup delivers the losses already before building a first prototype of the desired product. Thus, the total power loss of the complete component (the sum of winding and core loss) for a given operating point can be easily measured.

Figure 21 displays the overall losses of two components depending on the switching frequency [47, 48].

Furthermore, the dashed lines show the loss data given by the manufacturer. For the ‘Würth HCI 1890’ 10 µH inductor, the data is gained by an online simulation tool from the manufacturer for the given operating points [47]. However, it predicts lower losses than the measurement delivers. The datasheet of ‘Vishay IHLP’ inductor with 3.3 µH only gives the DC resistance [48]. Therefore, the only way to predict losses is to use the RMS current and the DC resistance, which estimates significantly lower losses than the measured ones. These measurements show that there exists an urgent need to perform loss measurements for inductive components. Besides the power losses of a dedicated component, the measurement also delivers thermal information concerning the DUT. As the component operates under the intended operating conditions of the application, the device temperature gained by the test setup indicates whether the component is capable of handling the power dissipation with an acceptable temperature rise.

6 DISCUSSION

The applications shown within this paper demonstrate that the DC-metering approach, which was originally introduced by [2], is an encouraging alternative to other measurement principles to gain losses of magnetics. Furthermore, the measurement results presented in the previous section reveal the necessity to measure losses of magnetics, which is mainly caused by the lack of datasheet values.

The paper demonstrates, that it is vital for accurate results to select all components used within the test setup carefully. With the advent of new semiconductors, like GaN, the approach takes up here becomes more prominent, since these devices feature minimized parasitics due to the superior device technology and packages. GaN components currently available on the market allow an operating range of up to 400 V. The operating range could be extended by using SiC semiconductors. However, worse parasitic properties have to be accepted. As the capacitors used within the test setup also cause a significant share of losses, their ESR should be as low as possible at the switching frequency and its harmonics to ensure accurate results. Future technologies for capacitors could play an important role in improving this approach.

In addition, this method can be used for a test setup that is exclusively designed for core losses estimation on toroidal cores. For that reason low voltage GaN-HEMTs, featuring best performance like [49], should be applied. In order to be able to carry out measurements depending on the core temperature, the DUT should be placed in an oil bath to ensure that the core has the intended temperature.

In conclusion, the test setup motivates to conduct further studies to open up more applications using this approach.

7 CONCLUSION

This paper takes up an already known measuring approach, which is originally proposed more than 20 years ago by [2]. This method relies on low and accurately assessed losses of the power stage to determine losses of magnetic components by measuring the DC input power of a power electronic circuit. The setup, in particular, allows the determination of losses of magnetic components intended for use in modern power electronic circuits employing high switching frequency. Since [2, 18] only introduce the DC metering approach but do neither deliver any details of a practical realization with the corresponding characterization nor a validation of the method, this paper directly addresses these gaps. Besides the principle operation of the test setup, this paper describes the component selection and characterizes all components used. Since the approach relies on low losses, it significantly takes advantage of GaN devices, as these feature superior properties. In order to ensure valid results from the test setup, an uncertainty analysis follows. As the losses of air inductors can
be accurately predicted, these serve as reference components to validate the accuracy of the proposed test setup. After that, the wide applicability is demonstrated by conducting several measurements of core losses without and with DC bias of the flux density as well as loss measurements of complete components, which can be bought off the shelf. Therefore, it could be shown that the approach allows for application oriented measurements of the losses occurring in magnetic components.

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How to cite this article: Kohlhepp, B., et al.: Test setup using DC metering approach for loss measurements of inductive components – principle, characterization, validation and application. IET Power Electron. 14, 1856–1870 (2021).
https://doi.org/10.1049/pel2.12155