Implementation of the DCS System for the validation of MM HV Boards and the DCS System of the new BIS78 Chambers for the upgrade of muon system of the ATLAS Experiment

Ioannis Drivas-Koulouris
National Technical University of Athens

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Outline

• **New Small Wheel High Voltage (HV)**
  1. High Voltage Scheme
  2. Hardware Installation
  3. Validation of High Voltage Boards

• **sMDT BIS78 DCS Integration**
  1. Power Supply
  2. JTAG/MDM
  3. ELTX
  4. P2C
  5. Gas
New Small Wheel (NSW)

- the installation of NSW will reduce the trigger rate in the forward region (|\eta|>1.3) of the Spectrometer.

- Cope with future LHC Luminosities.

- Two new sub-detectors: MicroMegas (MM), small Thin Gas Chambers (sTGC).

\[\text{Distance to IP indicator}
\]

\[\text{Radial indicator}
\]

+ **MMG : Z2, Z3**

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Instead of 1 channel per layer, new mapping scheme includes 1 channel per PCB, 8 PCBs per layer!

- **Mapping:** Radial + clockwise
  A01 R1 Layer1 PCB1,...  A01 R1 Layer1 PCB5, A01 R2 Layer1 PCB1,...  A01 R2 Layer1 PCB3, A02 R1 Layer1 PCB1,... so on.

- **New Layout:** x3 mainframes
US15 Work

Mainframe’s number of slots: 16
Can host 5 boards of A7038ST (3 slots) type or 16 of A7038A (1 slot) type.

- 4 A7038STP + 1 A7038STN Boards
  4 x 32 = 128 channels for read-out
  Mapping: 16 sectors x 1 quadruplet x 1 layer x 8 PCBs

- 16 A7038AP Boards (NEW)
  16 x 48 = 768 channels for read-out
  Mapping: 16 sectors x 2 quadruplets x 3 layers x 8 PCBs
  = 8 boards/quadruplet

- 32 channels
- 3 slots in mainframe

- 48 channels
- 1 slot in mainframe
MM HV Board Testing Site

- Testing Site on BB5 Balcony
- One Mainframe with 16 slots
- 4 cables
- 2 loads (Resistors)
- Testing 2 boards at the time

validation PC

HV DCS PROJECT

OPC CLIENT

Opc-ua

OPC UA SERVER

Opc-ua Via network

Caen Mainframe

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**NSW MM Board “Burn In” Validation Project**

- **Purpose**: the boards can work under specific conditions with stable behavior.
- A Project was created for validation of the Caen A7038(ST,A) boards at BB5.
- Create buttons on every board to start/stop the test.
- Create buttons on the panel for the test of all the boards and to change test parameters.
- A root scripts has been developed in order to analyze the files created at the end of each run.

**Test Steps**

1. All channels of the board are ON for 10’
2. All ODD channels are OFF and EVEN are ON for 30’
3. All EVEN channels are OFF and ODD are ON for 30’
4. Switch OFF all channels for 2h.
5. Switch ON all channels for 50’
6. Switch OFF all channels
HV TESTING A7038AP BOARD (~4 HOURS)

- 1st Batch (5 Boards)
- No issues
- Some more times on different durations for crosscheck
HV TESTING A7038AP BOARD (~4 HOURS)

- 2nd-3rd Batch (22 Boards)
- Some issues with opc connection and mainframe (fixed)
- Maximum Voltage on 700 V
- Some more times on different durations for crosscheck

```
dpSetWait(EasyBoard + ".userDefined.nominal.v0", 700); //400
dpSetWait(EasyBoard + ".userDefined.nominal.v1", 300);
dpSetWait(EasyBoard + ".userDefined.nominal.10", 100);
dpSetWait(EasyBoard + ".userDefined.nominal.svMax", 800);
dpSetWait(EasyBoard + ".userDefined.nominal.tripTime", 10);
dpSetWait(EasyBoard + ".userDefined.nominal.rUp", 25);
dpSetWait(EasyBoard + ".userDefined.nominal.rDown", 25);
dpSetWait(EasyBoard + ".userDefined.nominal.vSafe", 100);
dpSetWait(EasyBoard + ".userDefined.nominal.vMax", 800);
dpSetWait(EasyBoard + ".userDefined.nominal.vMin", 100);
```
Small Diameter Drift Tubes (sMDT) BIS7

• The phase-1 upgrade for BIS78 chambers is a pilot for the phase-2 upgrade and aims to improve high momentum muon trigger system in the transition region between Barrel and Endcap of Muon spectrometer: $1 < |\eta| < 1.3$.

• New sMDT in BIS integrated with new RPCs (trigger).

• Our focus is the sMDT BIS7 that replaced the old BIS7 and BIS8 MDT Chambers.
Improvements with respect to the current MDT chambers:

• Replace 32 BIS78 Monitored Drift Tube (MDT) chambers in Barrel inner region with 16 small-diameter MDT (sMDT) chambers and 32 thin Resistive Plate Chambers (tRPC).

• Decreasing the tube diameter by 1/2 compared to current MDT detectors reduces the detector size with minimal loss of resolution permitting the insertion of RPC trigger chambers adding crucial trigger acceptance in the barrel/endcap transition region.

• sMDTs have 8 times lower background detector occupancy compared to MDTs (factor of 4 from reduction of max drift time, and factor of 2 from smaller diameter).

• Electronics dead time decreased by four times (from 750 ns to 175 ns).

• sMDT operated with Ar:CO2 gas at 3bar and at HV = 2730V.
Power Supply Project

- Two PS Project on the MDT Side (Barrel-EndCap Region)
- On Hardware:
  1. New mapping has been developed for max current and voltage requirements.
  2. A new board have been installed for the the Mapping (rest are old boards).
- Low level structure: Data points, mapping, archive, alarms.
- Modified Finite State Machine (FSM) and UI visualisation of several Panels.
- Create new panels for the new PS Mapping scheme (shared channels).
JTAG/ETLX BIS78 Project

- **What is JTAG?**
  - **Joint Test Action Group**, it was initially devised for testing printed circuit boards using boundary scan.

- New Data points have been created BIX7/BIY7(*two csms* per new chambers).

- CSM stands for Chamber Service Module and controls electronics(Mezzanines cards).

- Modified MDT scripts and libraries to accommodate the new name.

- Recreate FSM and modified FSM Panels.
P2C Project(PVSS2COOL)

- Cool DataBase has details for the offline Data Quality and the Athena such as the High and Low Voltage and Jtag.

- Create new channels for the new BIX/Y Data points.

- Create corresponding configs for the new Data Points.

- Remove BIS8A Chambers.

- New names need to be adopted by Data Quality.
GAS PROJECT

- Work on THE Low Level structure (Data Points).
- Modified the main Gas colormap.
- Update copy manager (copy_data) for updates.
- Check connection with DataBase.
- Check interlock mechanism for the BIS7A Chambers (Advanced panels).

sMDT DCS Intervention ends well (thanks to the whole MDT Team)
Summary

• 27 A7038AP Boards have been tested successfully. No major issue found, thus all the qualified HV Boards for side A have been installed at P1.
  The installation of the mainframes, the HV boards and the relevant cabling for side A is done. When the time comes the same work will be applied for side C.

• The sMDT DCS integration for all the relevant sub-systems (PS, JTAG, etc) has been finalised successfully. This will be used as future reference for side C.

• For P2C Project the corresponding folders have been created in order to be connected with the DATA QUALITY (DQ).

THANK YOU!!!