Effect of ALD Processes on Physical and Electrical Properties of HfO$_2$ Dielectrics for the Surface Passivation of a CMOS Image Sensor Application

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ABSTRACT The surface passivation of a CMOS image sensor (CIS) is highly beneficial for the overall improvement of a device performance. We employed the thermal atomic layer deposition (T-ALD) and plasma enhanced (PE-ALD) techniques for the deposition of 20 nm HfO$_2$ as well as stacked with 3 and 5 nm Al$_2$O$_3$ thin films. The HfO$_2$/Si and Al$_2$O$_3$/HfO$_2$/Si metal-oxide-semiconductor structures were used to analyze the fixed charge density ($Q_f$) and interface trap density ($D_{it}$). The as-synthesized samples show high $D_{it}$ and $Q_f$ values ($10^{12}$ cm$^{-2}$eV$^{-1}$) and a minority carrier lifetime of 15-300 $\mu$s. The finite-difference time-domain simulation of high-k dielectrics confirmed that the Al$_2$O$_3$ (top)/HfO$_2$ stacked structures expected higher quantum efficiency for CIS application. The effect of vacuum annealing (VA) and forming gas annealing (FGA) treatments succeeded with the decomposition of the $D_{it}$ and increase in carrier lifetime. The H$_2$ ambient FGA samples showed a remarkable decrease in the $D_{it}$ values. To improve the overall performance of the device after passivation, we employed an Al$_2$O$_3$/HfO$_2$ bilayer structure, which showed a low $D_{it}$ of $10^{11}$ cm$^{-2}$eV$^{-1}$ and a minority carrier lifetime of $\sim$3,700 $\mu$s after 400 $^\circ$C and 30 min FGA. We believe that this surface passivation strategy will pave way for future CIS technology regarding the development of lower defective surface and superior performance.

INDEX TERMS Atomic layer deposition, carrier lifetime, CMOS image sensor, surface passivation, forming gas, HfO$_2$ interface trap density.

I. INTRODUCTION

The rapid progress in CMOS circuit technology is extending a dominant market extension regarding novel electronic devices [1]. CMOS technology plays an important role in the evolution of image sensors as modern low-cost sensors require high resolution, high speed, and low power consumption [2]. However, the performance of the CMOS image sensor (CIS) is highly affected by defects (Si-dangling bonds) and impurities that are linked with Si interfaces and surfaces. Therefore, it is important to passivate the Si surface to achieve better device performance.

The defects at the Si/dielectric interface introduce different energy levels into the Si bandgap, which are generally termed as interface trap density ($D_{it}$). Therefore, excellent chemical surface passivation is required to suppress the defects at the Si/dielectric interface, which can reduce the $D_{it}$ [3]. On the other hand, the fixed charge ($Q_f$) is the charge accumulation within a few nm of the Si/dielectric interface. The $Q_f$ is the resultant of the surface properties and annealing conditions. The presence of charges in the dielectric film established an electric field at the interface, which can either attract or repel the carriers from the surface [4]. Thus, attracting or repelling one type of carrier from the surface limits the charge recombination rate [5]. Also, the negative charges for the p-type Si and the positive charges for the n-type Si...
can improve the quality of the field-effect passivation in the entire injection level range. The quality of passivation by the dielectric is commonly examined by the minority carrier lifetime [6]. The minority carrier lifetime depends on the surface recombination and the dark current of the thermally generated electrons at the interface. This results in the excitation of electrons from the valence band to the conduction band surface recombination and the dark current of the thermally generated electrons at the interface. This results in the excitation of electrons from the valence band to the conduction band.

Up to now, a variety of high-k dielectric materials, such as Al₂O₃, HfO₂, Ta₂O₅, and TiO₂ are of beneficial interest for the surface passivation [7]–[9]. Among these high-k materials, HfO₂ and Al₂O₃ dielectrics are of receiving progressive attention due to their outstanding defect decomposition properties in regard to the CIS applications [10]. Interestingly, the bilayer or laminated structures of the dielectric materials, such as Al₂O₃, HfO₂, SiO₂, and TiO₂ are widely adopted due to their overall surface passivation benefits and improved device performance [7], [8]. However, the high quality of chemical as well as field effect passivation is introduced by Al₂O₃ and HfO₂ which effectively passivates the defects. This is because of the improvement in the interfacial layer due to the bilayer structure of Al₂O₃ and HfO₂. Owing to the excellent interfacial characteristics, these Al₂O₃/HfO₂ bilayer structures are getting more and more attention for the improvement of passivation quality. The synthesis of the dielectric thin films has been implemented by a variety of techniques [11]. Atomic layer deposition (ALD) is a state-of-the-art and crucial technique among the various techniques to synthesize different dielectric materials. The ALD process represents the key features of the as-synthesized films, which include a highly effective uniform deposition, low-temperature process, and layer-by-layer growth. Also, it is the most favorable as compared to other techniques due to a self-limited reaction mechanism that is based on the chemisorption of two or more precursors [12], [14].

In this research work, we have investigated the different process parameters as well as the post-metal annealing conditions that realized the decomposition of the Dør and increased Qf for a single HfO₂ structure. However, to increase the carrier lifetime and improve the interface, we have employed the bilayer Al₂O₃/HfO₂ laminate structures. The results show that the H₂ ambient forming gas annealing (FGA) remarkably decreases the Dør values than vacuum annealed (VA) samples. The Al₂O₃/HfO₂ bilayer structure may show better field-effect and chemical passivation effect [18] in an integration of CIS process by minimizing the formation of interfacial layer (Si/dielectric) and improve characteristics of the dielectric properties. Hence, after FGA of Al₂O₃/HfO₂ bilayer structure, the interfacial layer gets improved which results in reduction of Dør values and recombination. Also, combining effect of these high-k materials effectively enhances the passivation quality. We believe that this surface passivation strategy will pave a way for future CIS technology regarding the development of lower defective surface and superior performance.

II. EXPERIMENTAL DETAILS

The HfO₂ ALD films were deposited using a tetraakis (ethylmethylaminohafnium) (TEMAHf, Hf[N(C₂H₅)(CH₃)]₄) precursor at a temperature range between 100 °C to 400 °C. The p-type Si ((100), 18 Ω-cm) substrates were cleaned using an ammonia peroxide mixture (NH₃:H₂O₂:de-ionized (DI) water with a ratio of 1:1:5 at 70 °C for 10 min) and diluted hydrofluoric acid (50:1, DI H₂O) at room temperature for 1 min before the deposition. The HfO₂ films were then deposited using ALD reactor (Plus 200 system, Quros). The TEMAHf precursor was supplied with O₂ plasma at a 200 sccm flow rate and a power of 100 W, for the sequential surface reactions in the plasma-enhanced ALD (PE-ALD) at a chamber pressure of 0.4 mTorr. Also, H₂O precursor was used in thermal ALD (T-ALD) for the 20-nm-target film thickness instead of the O₂ plasma for PE-ALD deposited films. For comparison of the different HfO₂ films synthesized using different ALD processes, the T-ALD HfO₂ and PE-ALD HfO₂ samples were prepared at different deposition temperatures (250 °C and 280 °C) on the pre-cleaned Si wafer. The post-deposition annealing was performed in a tube furnace at room temperature and forming gas (N₂:H₂ = 95 %:5 %) conditions for all the HfO₂ samples. The annealing temperature was kept constant at 400 °C for 30 min.

To fabricate the standard Al/HfO₂/Si and Al/Al₂O₃/HfO₂/ Si MOS capacitor (MOSCAP) like structures, a 300 nm Al top electrode was deposited using thermal evaporation. The custom-made shadow mask with a 150 × 150 μm² dimension was used for the dot structure as a gate electrode for all the structures. The capacitance-voltage (C-V) and the current density-voltage (J-V) measurements of the prepared structures were then conducted using the Agilent B1500A parameter analyzer. All the measurements were traced at room temperature with a high frequency (1 MHz) under dark conditions. The dual C-V curves of 10 devices in the forward and backward directions were collected from the accumulation to the inversion region properties of the MOSCAPs. The J–V characteristics were then conducted to investigate the effect of the different passivation layers on the electrical properties of the prepared MOSCAPs.

The Dør and Qf values were estimated using C-V curves from Eqs. 1 and 2, respectively [15].

\[
Q_f = \frac{(\varphi_{ms} - V_{FB})C_{ox}}{qA},
\]

(1)

where \( \varphi_{ms} \) is defined by the difference between the metal and the semiconductor work functions, \( V_{FB} \) is the flat band voltage, \( C_{ox} \) is the oxide capacitance, \( q \) is the electron charge, and \( A \) is the electrode area.

\[
D_{\text{f}} = \frac{2\omega C_{ox}^2 G_{\text{max}}}{qA(G_{\text{max}}^2 + \omega^2 (C_{ox} - C_m C_{\text{max}})^2)},
\]

(2)

where \( G_{\text{max}} \) is the maximum conductance, and \( C_m \) is the measured capacitance at the frequency \( \omega \).

The thickness and refractive index (n) of the HfO₂ films were determined using spectroscopic ellipsometry (alpha SE,
J. A Woollam co., Ltd. The minority carrier lifetime (injection level-dependent) of the Si-wafers was measured using the quasi-steady-state photocurrent (QSS-PC) method with the lifetime tester (WCT-120, Sinton Instruments) [16]. The minority carrier lifetime was extracted at an intermediate carrier level injection of $1 \times 10^{15} \text{ cm}^{-3}$.

### III. RESULTS AND DISCUSSION

In this study, the ALD synthesis of the HfO$_2$ thin films was conducted at a wide temperature range from 100 °C to 400 °C using a TEMAHf precursor to examine the thorough deposition variation. Fig. 1 illustrates the growth per cycle (GPC) and $n$ of the HfO$_2$ thin films with respect to the deposition temperature. The GPC vs the deposition temperature curve (black) in Fig. 1 indicates that the GPC decreases at 200 °C and reaches a stable value of about 1.5 Å/cycle in the range of 250 °C to 300 °C. After that, the GPC increased in the temperature range from 300 °C to 400 °C. Thorougly, the initial temperature range (100-200 °C) possesses minimal activation energy for the formation and growth of the HfO$_2$ thin films [17]. On the other hand, temperature above 300 °C showed a CVD-type growth performance, which showed a high GPC value [18]. This implies that the temperature range of 250-300 °C is a crucial temperature range for the optimal process window. Additionally, the ellipsometry measurements showed a slanted increase of the $n$ from 100 °C to 200 °C. However, with a further increase in temperature, the $n$ values acquire a stable range from 250 °C to 300 °C, which again decreased for both ALD processes. Thus, the overall results imply that the ALD process window is optimum in the range of 250-300 °C. Fig. 2(a) shows the C-V characteristics of the as-deposited PE-ALD HfO$_2$ samples at 250 °C under different annealing conditions. The arrows indicate the voltage sweep direction in the C-V curves. The obtained C-V curves display hysteresis in the as-prepared HfO$_2$ films. The hysteresis in the C-V curves is related to the existence of a certain amount of interface defects at HfO$_2$/Si interface. [19], [20]. However, after VA and FGA treatments there is a remarkable reduction in the C-V hysteresis due to a reduction in interface defects [19], [21]. Further, after VA and FGA, the $V_{FB}$ showed a negative value, which reflects the existence of trapped positive oxide charges in the HfO$_2$ passivation layer. The T-ALD films also exhibited similar characteristics as PE-ALD grown films.

In addition to $V_{FB}$, the permittivity ($K$) and other parameters of the as-grown films are summarized in Table 1. The $EOT$ and the $K$ of the HfO$_2$ films were extracted using the relation provided below Eqs. 3 and 4. [22]:

$$EOT = \frac{K_{SiO_2} \times \varepsilon_0}{C_{\text{max}}/A},$$

$$K = \frac{K_{SiO_2} \times t_{hk}}{EOT - t_{SiO_2}},$$

where $K_{SiO_2}$ is the permittivity of SiO$_2$, $A$ is the area of the Al electrode, $C_{\text{max}}$ is the accumulation capacitance, and $t_{hk}$ is the thickness of the HfO$_2$ films. The annealing effect on the HfO$_2$ films prepared at 250 °C in PE-ALD showed an increase in the $EOT$ and a reduction in $K$, as illustrated in Table 1. For the films prepared at 280 °C (T-ALD), 250 °C (PE-ALD), and 280 °C (PE-ALD), the same trend was observed. It can be concluded that the HfO$_2$ passivation layer can be attributed to the formation of the interface layer after the annealing [23], [24].

The J-V characteristics of the 280 °C PE-ALD grown films with VA and FGA conditions were measured after applying a negative bias. We observed a very low current density of $4.5 \times 10^{-7} \text{ A/cm}^2$ at $-1 \text{ V}$ after the annealing process at 400 °C. Due to the existence of a small number of dangling bonds and an interface charge trapping, the leakage current gets reduced after FGA [22], [25].

Fig. 3 shows the role of VA and FGA on the $D_h$values of the 20-nm-thick HfO$_2$ thin films deposited using T-ALD and PE-ALD growth techniques. For both synthesis techniques, the as-prepared films possessed high $D_h$ values ($1.2 \sim 1.5 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}$) before the annealing process. However, T-ALD showed lower $D_h$ values as compared to the PE-ALD technique. The Si-dangling bonds and the inferior HfO$_2$ and Si interface seemed to cause the high $D_h$ values for the as-prepared samples [15], [16]. Interestingly, in both ALD processes, the as-prepared HfO$_2$ films show a remarkable reduction in the $D_h$ values ($6 \sim 11 \times 10^{11} \text{ cm}^{-2} \text{eV}^{-1}$), which
FIGURE 3. Interface trap density ($D_{it}$) for 20-nm-thick HfO$_2$ films after annealing at 400 °C for 30 min. (a) thermal-ALD grown HfO$_2$ films and (b) plasma enhanced-ALD grown HfO$_2$ films.

FIGURE 4. Fixed charge density ($Q_f$) for 20-nm-thick HfO$_2$ films after annealing at 400 °C for 30 min. (a) thermal-ALD grown HfO$_2$ films and (b) plasma enhanced-ALD grown HfO$_2$ films.

FIGURE 5. Finite-difference time-domain (FDTD) simulation results: (a) reflectance at 500 nm incident wavelength as a function of thickness for each high-k dielectric, (b) reflectance as a function of wavelength for the Al$_2$O$_3$ films, and (c) reflectance as a function of wavelength for the HfO$_2$ films.

The graphical representation of reflectance at 500 nm was found to be linearly proportional to the thickness in the all-dielectric materials in the simulation. However, the lower reflectance values of the Al$_2$O$_3$ and HfO$_2$ dielectrics result in higher quantum efficiency (QE) values than Ta$_2$O$_5$ and TiO$_2$. Nevertheless, the comparison between the reflectance of Al$_2$O$_3$ and HfO$_2$ reveals that Al$_2$O$_3$ results in better QE than HfO$_2$ films (Fig. 5(b) and Fig. 5(c)). Furthermore, the Al$_2$O$_3$/HfO$_2$ stack structure results in high QE, and it is helpful for the CIS applications with its low reflectance. The reflectance of the Al$_2$O$_3$ and HfO$_2$ dielectrics results in higher quantum efficiency (QE) values than Ta$_2$O$_5$ and TiO$_2$. Nevertheless, the comparison between the reflectance of Al$_2$O$_3$ and HfO$_2$ reveals that Al$_2$O$_3$ results in better QE than HfO$_2$ films (Fig. 5(b) and Fig. 5(c)). Furthermore, the Al$_2$O$_3$/HfO$_2$ stack structure results in high QE, and it is helpful for the CIS applications with its low reflectance.

The generation and recombination of the carriers at the interface due to defects might result in the emergence of a dark current which can demean the QE of the CIS [32]. On the other hand, the reduction of carrier recombination is the key feature in fabricating Si-based high-performance cutting-edge electronic devices [33]. Figs. 6(a) and 6(b) demonstrate the effective carrier lifetime of the as-prepared and the FGA HfO$_2$ devices that were prepared by T-ALD and PE-ALD.
In Fig 6(a), T-ALD grown HfO₂ films show similar values under all conditions. However, the as-prepared samples exhibit lower carrier lifetime values as compared to the FGA samples, which is shown in Fig. 6(b). The low lifetime values of the as-prepared samples occur due to the recombination centers induced by the interfacial defects [34]. However, the carrier lifetime value of the single-layer HfO₂ films gets improved after the FGA (300 µs). The minimized charge carrier recombination is attributed to the enhanced lifetime after the FGA processing conditions. For further improvement in the carrier lifetime, the bilayer Al₂O₃/HfO₂ stacked structure was utilized as predicted by the FDTD simulation (Fig 5). Fig. 6(c) depicts the carrier lifetime measurements of the Al₂O₃/HfO₂ bilayer structures, deposited by PE-ALD with 3-nm and 5-nm thick HfO₂ and 20-nm-thick of Al₂O₃. As predicted, bilayer stacked structures of Al₂O₃/HfO₂ showed a higher carrier lifetime than the single-layer HfO₂ samples. The high quality of the chemical passivation can reduce the defects, which can increase the carrier lifetime. Later, both the Al₂O₃/HfO₂ bilayer structures were subjected to the FGA processing. The Al₂O₃/3-nm HfO₂ structure showed a carrier lifetime of 2,100 µs. However, the Al₂O₃/5-nm HfO₂ structure showed a maximum carrier lifetime of 3,750 µs owing to the better interface caused by the 5-nm-thick HfO₂ with Si. The record performance of the bilayer structures shows that the interface traps or the Si dangling bonds were banished and effectively passivated by the hydrogenation [34], [35]. Further, Fig. 6(d) shows that the Al₂O₃/HfO₂ bilayer structure shows lower Dᵢ values (1.0 × 10¹¹ cm⁻²·eV⁻¹) than the single-layer HfO₂ structures (6.0 × 10¹¹ cm⁻²·eV⁻¹) after the FGA processing conditions. Thus, the enhancement in the carrier lifetime due to hydrogenation after the annealing affects the chemical passivation of Al₂O₃/HfO₂, resulting in the record performance.

To study the interface property of Al₂O₃/5-nm HfO₂ bilayer structures, we used cross-sectional transmission electron microscopy (TEM). In Fig. 7, the TEM micrographs display the different MOS structures with an interface layer between HfO₂/Si. It was observed that the as-deposited Si/5-nm (target thickness) HfO₂/20-nm Al₂O₃ (target thickness)/Al samples showed a clear interface between the Si and HfO₂ with a 6.2-nm-thick HfO₂ and a 20.8-nm-thick Al₂O₃. These calculated values from the TEM are corroborated with the expected thickness from the ALD process. The fully amorphous nature of the oxide layers can be observed in the as-deposited ALD structures.

After FGA processing, the thickness of the interface between the HfO₂ and Si showed an improvement, and crystallinity gets increased as shown in Fig. 7(b) [8]. The increased interface thickness is crucial for the reduction of Dᵢ values [36]. In addition to this, hydrogenation played a very crucial role in the suppression of the Si dangling bonds, which also accounted for the Dᵢ suppression. Thus, the densification of the interface of the bilayer Al₂O₃/HfO₂ after FGA will result in decreased EOT and increased Kox as shown in Table 1.
The overall finding of this study revealed that the defects that are associated with the Si surface and its interfaces with oxides can be potentially controlled by chemical and field-effect passivation, which is emerging with CIS technology as well as Si-based electronic devices.

IV. CONCLUSION
In this study, the plasma-enhanced ALD (PE-ALD) and thermal atomic layer deposition (T-ALD) HfO2 thin films were prepared. The ALD process window was optimum in the temperature range from 250 °C to 300 °C. The high deposition temperature showed higher fixed charge density (Qit) values in both ALD techniques. In the case of interface trap density (Dit), the values for the T-ALD prepared HfO2 films were lower than the values for the PE-ALD grown films, which indicates that the moderate temperature played a crucial role in the surface passivation for the ALD processes. To improve the overall performance, we studied the Al2O3/HfO2 stack structures. The finite-difference time-domain (FDTD) simulation finding for the Al2O3/HfO2 stack showed higher QE for the CMOS image sensor (CIS) applications. The Al2O3/HfO2 stack layers possessed a minimum Dit of ~1.0 x1011 cm−2eV−1. The H2 ambient forming gas anneal (FGA) (400 °C for 30 min) is advantageous for chemical passivation in CIS applications. The bilayer Al2O3/HfO2 stacked structures showed an increased minority carrier lifetime from ~300 µs up to ~3,700 µs. The analyzed structures can help to increase the carrier lifetime as well as decrease the Dit values, which also reveal the importance of the FGA, and can assist with the advancement of the upcoming CIS technology.

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