Study on Energy Reduction Techniques in STT-RAM

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Abstract. Spin Transfer Torque Random Access Memory (STT-RAM) is suitable to be considered for cosmic memory. In STT-RAM the altercative period of attractive burrowing intersection is exchanged by the showing up of turn enraptured current over the intersection and it appear to be the most preparing elective with the more thickness and low introduction power, one of the major test for STT-RAM is the more write current, this paper proposes dual source write assist circuit method to reduce the equal compose vitality that prompts a diminishing in power utilization and the limit voltage of dynamic transistor to rising temperature. The MTJ temperature will increase than the write error rate is reduced. The final result is by effective use of VDD and threshold voltage values the write energy will be reduced. Right now, results utilizing a CMOS 65-nm get to transistor and the 40-nm MTJ innovation affirm that the projected compose help strategy prompts 81% of robustness is spared and its further incorporates just 9.6% territory excess to a 16-kb of STT-RAM cluster. And furthermore, another compose help technique is proposed to the end the compose activity in the wake of exchanging happens in the attractive burrowing intersection (MTJ), thus the both compose time vitality utilization of 1T-1MTJ piece cells will create.

Keywords: Magnetic Memories, Memory array, Non-Volatile Memory, Error free, complementary metal oxide semiconductor, vitality.

1. Introduction
Up to 80% of the built-up space in the processors is occupied by the memory array [1]. This consequently, ensures that there is low-spillage, and the process is fast. Scaling CMOS rationale circuits improve the working for example speed, area and power utilization [2]. Beyond the 45-nm CMOS node technology, increment in spillage current reason the powerful usage [3]. To diminish the introduction current, utilize the non-unpredictable recollections rather than a volatile memory is the best arrangement. MTJ(attractive passage intersection is a capacity to lessens the interconnect deferral and remove the spillage current, MTJ is equipped with a stuck layer and Mgo (protecting oxide) in the middle of them, and it is comprises of two resistive states one is arrange state and another is non-organize state, STT system is occupied to enable the states of the MTJ for more power ability [4].Many auto mobile industries are already consists and introduced the STT-MRAM into their manufactured items for the non-volatile storage. To decrease the unwanted power at the write current in memory, In compose end strategy methodology the write current oscillation cut-off is used once the data are transferred into the MTJ device. The Periodic read operation may be used for the compose consummation location but it only relevant for one particular MTJ phase transition [5].
Right now a self-ended compose help method, for moving of MTJ stage utilization STT, a bi-directional current is necessary for the voltage constraint between the change over the large current is depending on the right information and these data is boosted using the buffer chain. The hired data is used as input to the memory. At that point the compose fulfillment screening should be possible by the XNOR operation. The given input data and saved date with acceptable edge sense [6]. The turn move torque arbitrary access memory have one of a kind particular are non-volatility, less exposure, long life ability, CMOS amity, and high-speed access[2]. And it additionally clears the poor stability in MRAM approach [3]. Even though they suffer from more writing current that can be lead to be more power utilization [7]. Writers introduced an idea for ceaseless compose recognition for both MTJ states however the expense is high because of two different flip-flops are producing a self-write end frame work, by using self-ending hardware, both zone and vitality have expanded yet the composing vitality of MTJ diminishes. Hence the primary goal of the paper is to decrease the composing vitality of STT-RAM.

The diagram of this article is as per the following. In area II fundamentals of STT-RAM and MTJ (attractive passage intersections). Segment III recently proposed philosophies and strategies to diminish the compose current in STT-RAM. At long last, ends are section IV.

2. Literature Review

BASIC OF STT-RAM: STT - RAM is a new type of Magnetic Random-Access Memory [8]. STT-RAM cells need a Magnetic Tunnel Junction (MTJ) to the information in the binary form and the MTJ may have two layers 1. Reference layer 2. Tunnel and Tunnel free layer [2]. The magnetic way alternate layer is established when the free layer of magnetic way is changed. STT-RAM uses spin-polarized current passing via MTJ to vary the way of its magnetic way in the free level [6]. The relevant magnetization sandwiched between the reference level and free level the outcome is in particular resistance of MTJ [2]. The STT-RAM handling the low switching current than conventional MRAM[2]. STT-RAM thresholds current reduces the size of the MTJ gets smaller. STT-RAM faces the high current as compared to the SRAM [4]. Fig. 1 defines the STT-RAM cell [9]. The above section has a magnetic tunnel junction (MTJ) and NMOS access transistor, those are in series connection. It is applied to save the binary information and is mixed of an oxide barrier (MgO) in the middle of the two ferromagnetic layers. Write operation Stochastic Nature– in STT-RAM the full converting period having the incubation period and transfer period, formation period is known as the period required for the charge to go up the potential barrier in MTJ [4]. The transit period is defined as the period for charges to drop from the potential barrier to other phases [4].

Figure 1: 1T-1MTJ STT-RAM Cell
Write operation Asymmetric Nature - Write process in STT-RAM is processed by giving the spin-polarized current in to the desired way and to write the 1 on an MTJ cell takes more time than the 0 on MTJ cell. This Asymmetry is due to the three dissimilar speculates. One is the MTJ resistance is less in p-state and second one the derivable of the access transistor is automatically reduces [7].

2.1 Previously Proposed Techniques
Low Vth in STT-RAM- to increase the writing efficiency in STT-RAM, the lower Vth of the device to allow the large current flow by them, the increased current would be trade with the smaller cell space, faster write time lower write efficiency at ISO speed/area and larger MTJ area, brunt of using low Voltage device on the write margin and space benefits, programming of a 1 can processed by using an economic 32nm process at low voltage and typical NMOS corner with temperature range at 110 degree Celsius, reducing the voltage by 200mV giving in the right margin for the same width of NMOS and Vth. By using the lower Vth NMOS device is high leakage current passing through each unselect bit cell on the column as the bit cell [10].

MTJ Model Used – MTJ model is depend on Landau-Lifshitz-Gilbert (LLG) derivation including external magnetic fields and spin torque. Heat diffusion calculations, LLG, thermal forms, electrons transmission is implemented by using voltage-based current sources and capacitors, due to the operation deviation, MTJ cell is the change in space and this variations effects the write current has been led the variation of the switch hold-on[8]. The MTJ cell is to write the values 1 and 0 takes another time span as well as another potential and the writing in one way is quicker than the other direction [10]. MTJ cell aid to change faster and it is likely to perceive the arriving data if the write process is slow. Then the write operation can be increased using thermally assisted technique. Fig. 2 shows the fundamental step in read-before-write operation.

Self-Terminated Write Assist Methodology- This method is for write detection to decrease the unwanted power absorption at write operation [20]. The information is written by passing the bidirectional write current through the MTJ device for writing corresponding row and bit lines using column decoder [10]. A column transistor is used for facilitating particular column for read and writes operations. The voltage waveform is used to expose the state change of the MTJ device.

RT-WT Technique- WT approach is expected that it not only notice the MTJ switching and also improve the stability to system variations are related with the VOW and VEW methodologies. Two proposals are suggested in the SDWT method to decrease the effect of variation in the system.

1. Differential Sense proposal- The BL and SL voltages vary in different ways when the write operation switching is happening. In order to apply the VSL and VBL to the input of the comparator then they have to be at the same levels.

2. Self-Referenced sense proposal- In this approach the initial voltages BL and SL on the two capacitors are the referred voltages. This is noted at the beginning of write operation before the switching occurs. Then the voltages will be adjusted on two capacitors to find the MTJ switching. They are two capacitors having the same voltages then the BL and SL are consisting of same potential levels.
3. Results

To find the effect of process variations on the different approaches Monte Carlo analysis with number of interactions are used. In transient simulation of dwt method, the write operation is disabled. With this more energy is saved and it depends on the application of the device. By writing the ‘1’ and ‘0’ in this technique maximum of 49% of the power is saved. To increase the power saving transistor access sizes with 400-nm width, TW has 15ns under these specifications 81% of power is saved. By using the CMOS and Adiabatic technologies 60% of the power is decreased, while in STT-RAM the CMOS have the average power of 1.9e-002 and Adiabatic have the average power of 1.3e-002. This adiabatic technique is the latest technique for reducing the power consumption in ram.

During the write operation if switching is occurring then SL and BL voltages are varied in different ways and VSL range from 840mV-950mV and the VBL range from 88mV-95mV.

4. Conclusion

STT-Ram is non-volatile, has high density and CMOS compatible. STT-RAM suffering from high write latency is one of the drawbacks of this technology. By decreasing the threshold voltage of the transistors the current pulse time period is heated up, as a results the power consumption is increased so we decided to use the dual source technique to decrease the power consumption in fast write path with decrement the over all write latency by approximately 11.4% and the proposed write termination technique reduce the write energy upto 81% as compared with the cell with out write termination technique.
Table 1: Table showing the type of write technique used and the corresponding result

| S. No | Type of Technique                        | Result                                                                 |
|-------|-----------------------------------------|------------------------------------------------------------------------|
| 1     | Low Vth in STT-RAM                      | It improves the writing ability in STT-RAM.                           |
| 2     | MTJ model used.                         | It helps to switch quickly and also detects the arriving data.        |
| 3     | Self-Termination write assist technique.| In this technique it reduces the unwanted power consumption at write operation. |
| 4     | Dual source write termination Method.    | Apart from results, writes fast with less amount of energy.          |
| 5     | RT-WT Technique.                        | Significantly robust compared with the different techniques.          |

References

[1] F. Moradi, S. K. Gupta, G. Panagopoulos, D. T. Wisland, H. Mahmoodi, And K. Roy, “Asymmetrically doped FinFETs for low-power robust SRAMs,” IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4241–4249, Dec. 2011.
[2] Y. Huai, “Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects,” AAPPS Bull., vol. 18, no. 6, pp. 33–40, Dec. 2008.
[3] Q. Li, J. Li, L. Shi, M. Zhao, C. J. Xue, and Y. He, “Compiler-assisted STT-RAM-based hybrid cache for energy-efficient embedded systems,” IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 22, no. 8, pp. 4456–4459, Jul. 2013.
[4] S. Fujita et al., “Novel nonvolatile L1/L2/L3 cache memory hierarchy using nonvolatile SRAM with voltage-induced magnetization switching and ultra low-write-energy MTJ,” IEEE Trans. Magn., vol. 49, no. 7, pp. 4456–4459, Aug. 2014.
[5] J. Talafy and H. R. Zarandi, “Soft error analysis of MTJ-based logic in-memory full adder: Threats and solution,” International Symposium on On-Line Testing and Robust System Design, pp. 207–208, 2017.
[6] F. Moradi et al., "Asymmetrically doped FinFETs for low-power robust SRAMs," IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4241–4249, Dec. 2011.
[7] Y. Huai, “Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects,” AAPPS Bull., vol. 18, no. 6, pp. 33–40, Dec. 2008.
[8] Z. Sun, X. Bi, H. Li, W. F. Wong, and X. Zhu, “STT-RAM cache hierarchy with multi retention MTJ designs,” IEEE Trans. VLSI Systems, vol. 22, no. 6, pp. 1281–1293, Jun. 2014.
[9] T. Zheng, J. Park, M. Orshansky, and M. Erez, “Variable-energy write STT-RAM architecture with bit-wise write-completion monitoring,” Symposium on Low Power Electronics and Design, pp. 229–234, Sep. 2013.
[10] Albert Ciprut, Eby G. Friedman, "Energy-Efficient Write Scheme for Nonvolatile Resistive Crossbar Arrays With Selectors", Very Large Scale Integration (VLSI) Systems IEEE Transactions on, vol. 26, no. 4, pp. 711-719, 2018.
[11] Albert Ciprut, Eby G. Friedman, "On the write energy of non-volatile resistive crossbar arrays with selectors", Quality Electronic Design (ISQED) 2018 19th International Symposium on, pp. 184-188, 2018.
[12] T. Devolder et al., “Single-shot time-resolved measurements of nanosecond-scale spin-transfer induced switching: Stochastic versus deterministic aspects,” Phys. Rev. Lett., vol. 100, p. 057206, Feb. 2008.
[13] Y. Wang, Y. Zhou, and F.-C. Zhang, “Influence of quantum and thermal noise on spin-torque-driven magnetization switching,” Appl. Phys. Lett., vol. 103, no. 2, p. 022403, Jul. 2013.
[14] X. Wang, Y. Zheng, H. Xi, and D. Dimitrov, “Thermal fluctuation effect on spin torque induced switching: Mean and variations,” J. Appl. Phys., vol. 103, no. 3, p. 034507, 2008.

[15] Z. Diao et al., “Spin-transfer torque switching in magnetic tunnel junctions and spin-transfer torque random access memory,” J. Phys., Condens. Matter, vol. 19, no. 16, p. 165209, 2007.

[16] Y. Zhang, X. Wang, Y. Li, A. K. Jones, and Y. Chen, “Asymmetry of MTJ switching and its implication to STT-RAM designs,” in Proc. Design, Autom. Test Eur. Conf. Exhibit. (DATE), Dresden, Germany, Mar. 2012, pp. 1313–1318.

[17] X. Fong, S. H. Choday, and K. Roy, “Bit-cell level optimization for non-volatile memories using magnetic tunnel junctions and spintransfer torque switching,” IEEE Trans. Nanotechnol., vol. 11, no. 1, pp. 172–181, Jan. 2012.

[18] C. J. Lin et al., “45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell,” in Proc. IEEE Int. Electron Device Meeting (IEDM), Baltimore, MD, USA, Dec. 2009, pp. 1–4.

[19] D. D. Tang and Y.-J. Lee, Magnetic Memory: Fundamentals and Technology, New York, NY, USA: Cambridge Univ. Press, 2010, pp. 122–164.

[20] X. Bi, Z. Sun, H. Li, and W. Wu, “Probabilistic design methodology to improve run-time stability and performance of STT-RAM.

[21] J. Talafy and H. R. Zarandi, “Soft error analysis of MTJ-based logic in-memory full adder: Threats and solution,” International Symposium on On-Line Testing and Robust System Design, pp. 207–208, 2017.

[22] H. Bardareh, A. M. Hajisadeghi and H. R. Zarandi, “A low-cost soft error tolerant read circuit for single/multi-level cross-point RRAM arrays,” International Symposium on On-Line Testing and Robust System Design, 2018.

[23] A. M. Hajisadeghi, H. Bardareh, and H. R. Zarandi, “MOMENT: A Cross-Layer Method to Mitigate Multiple Event Transients in Combinational Circuits,” Euromicro Conference on Digital System Design, 2018.

[24] R. Bishnoi, M. Ebrahimi, F. Oboril, and M. B. Tahoori, “Improving write performance for STT-MRAM,” IEEE Transaction on Magnetics, vol. 52, no. 8, 2016.

[25] Swami S, Mohanram K. Reliable nonvolatile memories: Techniques and measures. IEEE Design & Test. 2017 Mar 15;34(3):31-41.