Fully-integrated DCDC buck converter based on PID algorithm

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Abstract. With the continuous development of power supply technology, the application of power management chips becomes more extensive, and the requirements for fully integrated power management chips are getting higher. This paper designs a buck converter with a fully integrated digital control circuit and power circuit with an output voltage of 2V. In voltage mode, digital pulse width modulation (DPWM) technology and PID algorithm are used, and a digital closed-loop control buck circuit system is designed by cadence tools. The performance of analog and digital closed-loop control circuits is compared at the same buck power stage. Under rated load conditions, the lock-up time of the digital control buck circuit is 826us, the output voltage ripple is 14.75mV, the response time of load sudden change at light load is about 900us, and the response time of load sudden change at heavy load is about 2ms.

1. Introduction
With the increasing requirements for DCDC circuit accuracy and power consumption, digitally controlled power supplies have also become a hot spot in recent years.

The architecture diagram of the analog buck converter is shown in figure1. The buck topology for analog closed-loop control consists of a power stage, an error amplifier, a comparator and a drive circuit.

The digital control power supply has the advantages of high accuracy, low power consumption, high efficiency, and small size. It is widely used in various applications in the industry, such as the power management of new energy vehicles, the power adapter of electronic equipment, and the communication industry. Nowadays, the digital control power supply used in the industry mainly implements algorithms through DSP or FPGA[1]. This control method is costly, the area of the circuit board is larger, and the circuit reliability is relatively low. The fully integrated digital control power supply proposed in this paper fully integrates the power levels except for inductors and capacitors, and all digital closed-loop control modules into one chip, which effectively reduces the cost of the chip, the area of the power management chip, at the same time, also greatly increases the reliability of the chip. Compared with analog circuit control, the advantages of digital circuit control are high flexibility, high accuracy, and online tuning[2]. Fully integrated digital control chip has gradually become a trend[3].

2. Digital closed loop control system

2.1. Digital DCDC controller
The system architecture diagram of the digital DCDC buck converter is shown in figure 2[4]. The circuit consists of two switch devices, a PID controller, a PWM modulator, a boost driver, an ADC converter...
and a power stage. The two MOSFETs Q1 and Q2 are controlled by two PWM signal with dead time. The output voltage is directly converted to a digital value through the ADC converter. The digital value is compared with the reference value to produce a difference, which is passed The PID algorithm calculates and outputs the corresponding duty value, and controls the DPWM module to generate two PWM signal to control the opening and closing of the switching device.

![Figure 1. Analog control buck circuit structure](image1.png)

![Figure 2. Digital control buck circuit structure](image2.png)

### 2.2. PID control algorithm

The PID incremental algorithm means that the output of the digital quantity is only the increment of the control quantity $\Delta u[k]$. The core of this algorithm is the PID control equation of the discrete domain incremental algorithm, as shown in equation 1 and equation 2.\(^5\)

$$u[k] = K_p e[k] + K_i \sum_{i=0}^{n} e[k] + K_d \{e[k] - e[k-1]\}$$

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In the equation, $T$ is the sampling period, the discrete independent variable is $k$, $K_p$ is the proportional coefficient, $T_i$ is the integral time constant, and $T_d$ is the derivative time constant. From equation 3, the Z-domain transfer function of the PID incremental algorithm can be obtained as equation 4. Assuming $u[k] = u[k-1] + \Delta u[k]$, we can get formula 3 by inserting formula 2.

$$\Delta u(k) = K_p \Delta e(k) + K_i e[k] + K_d \Delta e(k) - \Delta e(k-1)$$

In the formula, $\Delta e[k] = e[k] - e[k-1]$. Since the general control system does not change after the sampling period $T_s$ is determined, thus, as long as the error value of the first three samples is taken, the control increment can be calculated by equation 3. The discrete domain transfer function of the incremental PID algorithm is shown in figure 3.

$$D(z) = \frac{A(z)}{e(z)} = K_p [1 - z^{-1}] + K_i [1 - 2z^{-1} + z^{-2}]$$

The advantage of the incremental control algorithm is that there is no need for accumulation in the equation, and the determination of the control increment $\Delta u[k]$ is only related to the last three sampling values, and it is easier to obtain better control effects through weighting processing.\(^6\)
The PID filter designed in this paper generates and latches the current error value and the error value of the first two states when the rising edge of the clock arrives, and calculates the $u[k]$ and duty values through equations. The final output duty value is the high-level time. Input the high-level time into the PWM controller and we can get a PWM signal with the corresponding duty cycle. The logic block diagram of the PID module is shown in figure 4.

### 2.3. Conversion circuit design

Because of this design adopts synchronous rectification technology \cite{7}, when the regulator device PMOS and rectifier device NMOS are turned on alternately, there will be simultaneous conduction. The addition of a conversion circuit can further ensure the dead time of the two switching device, at the same time, the PWM signal output by the DPWM module is increased from 1.8V to 5V. The schematic diagram of the conversion circuit is shown in figure 5. One of the main problems of this circuit is that the rise time and fall time of the boosted PWM signal are relatively long, which will offset a certain dead time. Therefore, we can appropriately extend the dead time in the digital circuit to leave a margin for the drive circuit, thus setting an appropriate dead time.

### 2.4. Design of DPWM and ADC modules

The DPWM module generates a modulation signal through a counter, compares the $u[k]$ value with the modulation signal generated by the counter through digital logic, and design a dead time through digital logic to generate two PWM signal that are not turned on at the same time. The logic block diagram of the DPWM module is shown in figure 6. At each rising edge of the pwm1 waveform, the module will lock the current duty value and start counting. When the counter reaches the duty value, it will flip pwm1 to complete a cycle of pwm1 signal. In the logic judgment of generating pwm2, the duty is delayed by
20n dead time, and finally two PWM signal with dead time and not conducting at the same time are obtained. The determination of the dead time is mainly determined by the PWM duty.

![Figure 5. The schematic of conversion circuit](image)

![Figure 6. Logic diagram of DPWM module](image)

The ADC module is designed by VerilogA language, and a nine-bit ADC module is designed. The main function is to convert the analog signal of the sampling resistor into a nine-bit digital signal, so that the digital algorithm can be used to process the analog quantity.

3. Test results

3.1. Static performance test

The reference voltage is 2.00v, to ensure that the rated load resistance remains unchanged, while the input voltage is from 3v-15. The maximum output steady-state error of the digital control buck circuit is only 0.078v, the deviation from the reference voltage value is only 3.9%, and the average change rate of the output voltage to the input voltage is 6.5mv/v.

The reference voltage is 2.00v, the input voltage is 5V, and the load resistance is from 5Ω to 30Ω. The maximum steady-state error of the output voltage of the digital control buck circuit is 0.019V, and the deviation from the reference voltage value is only 0.95%. The rate of change of the output voltage relative to the load resistance is about 0.00076Ω/V, and the maximum output current is 700mA. The resistance is 2.85Ω.

3.2. Dynamic performance test

**Input voltage sudden change test:** When the load of the digital buck converter is kept constant, the input voltage changes suddenly from 5V to 12V, and then from 12V to 5V. The output voltage waveform is shown in figure 7. In the figure, the output voltage waveform when the input voltage of the digitally controlled buck circuit changes abruptly. The fluctuation of the output voltage of the digital circuit is
about 310mv, and all will return to the reference voltage in about 2.5ms. When the input voltage is 12V, the stable output voltage is 2.091V, and when the input voltage is 5V, the output voltage is 2.019V.

**Load mutation test:** Keep the input voltage unchanged, and set the output reference voltage at 2.00V. When the load resistance is connected and disconnected (no load-100mA rated load-no load), the output voltage of digital closed loop control is shown in figure 8. The sudden load change of the digital control buck circuit causes the output voltage to fluctuate about 97mv. The stable time from no-load to rated load change is 1.094ms, and the stable time from rated load to no-load change is 894.64us. The stable output voltage under load is 2.093V, and the stable output voltage under 100mA load is 2.01V.

![Figure 7. Output voltage waveform of input voltage mutation](image1)

![Figure 8. Output voltage waveform of load mutation](image2)

### 3.3 Inductor current waveform
In the case of 700mA current load, the inductor current waveform is shown in figure 9. The system locks in 3.5ms, and the peak value of the inductor current is 1.1723A when it is stable. In the case of a 100mA current load, the inductor current waveform is shown in figure 10. The system locks in 3.5ms, and the peak value of the inductor current is 628.89mA when it is stable.
4. Conclusion
This article takes the buck converter as the target research object, and realizes the digitally controlled DCDC converter based on the AMS simulation in cadence. The digital controller has good robustness, high control accuracy and fast dynamic response when the internal parameters of the system change. When the DCDC converter load is 200mA, the comparison between the analog DCDC converter and the digital DCDC converter is shown in Table 1. The test conditions are:
- Input voltage 12V,
- Load 2.58Ω or no load.

The experimental results show that the digital circuit has a faster lock-in time and more accurate output adjustment ability, which can further improve the performance of buck circuit.

|                  | Output voltage (V) | Output ripple (mV) | Stabilization time (us) | Maximum current (mA) | Adjustment range (V) |
|------------------|--------------------|--------------------|-------------------------|----------------------|----------------------|
| Analog converter | 2.085              | 27.73              | 821                     | 400                  | 3-6                  |
| Digital converter| 2.010              | 13.39              | 1510                    | 700                  | 3-5                  |
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