Effects of Parasitics and Interface Traps On Ballistic Nanowire FET In The Ultimate Quantum Capacitance Limit

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Abstract

In this paper, we focus on the performance of a nanowire Field Effect Transistor (FET) in the Ultimate Quantum Capacitance Limit (UQCL) (where only one subband is occupied) in the presence of interface traps ($D_{it}$), parasitic capacitance ($C_L$) and source/drain series resistance ($R_{s,d}$) using a ballistic transport model and compare the performance with its Classical Capacitance Limit (CCL) counterpart. We discuss four different aspects relevant to the present scenario, namely, (i) gate voltage dependent capacitance, (ii) saturation of the drain current, (iii) the subthreshold slope and (iv) the scaling performance. To gain physical insights into these effects, we also develop a set of semi-analytical equations. The key observations are: (1) A strongly energy-quantized nanowire shows non-monotonic multiple peak C-V characteristics due to discrete contributions from individual subbands; (2) The ballistic drain current saturates better in the UQCL compared to CCL, both in presence and absence of $D_{it}$ and $R_{s,d}$; (3) The subthreshold slope does not suffer any relative degradation in the UQCL compared to CCL, even with $D_{it}$ and $R_{s,d}$; (4) UQCL scaling outperforms CCL in the ideal condition; (5) UQCL scaling is more immune to $R_{s,d}$, but presence of $D_{it}$ and $C_L$ significantly degrades scaling advantages in the UQCL.

Index terms: Nanowire FET, Coupled Poisson-Schrodinger Equations, Quantum Capacitance, Ballistic Transistor, Transistor scaling, Parasitic Capacitance, Interface traps.
I. INTRODUCTION

As we scale down the lateral as well as the longitudinal dimensions of the channel of a non-planar transistor and replace the Silicon channel by a so-called ‘high-mobility’ (or low effective mass) material, we start reaching two limits. The first limit is an electrostatic one, termed as ‘Quantum Capacitance Limit (QCL)’ [1]-[8]. The strong energy quantization due to the geometrical confinement in a multi-gated structure and the low density of states due to small effective mass of the channel material causes a small ‘quantum capacitance’ $C_q$ to be in series with the gate oxide capacitance $C_{ox}$. The small quantum capacitance dominating the total gate capacitance results in a number of interesting effects in the transistor characteristics [6]-[8]. There have been a number of experimental efforts as well, in a variety of systems to capture the effect of such quantum capacitance [9], [10]. The other limit, so called ‘Ballistic Transport Limit (BTL)’ is transport related which results from the scaling of the channel length and the relatively large mean free path of high mobility channel materials [11]-[14]. Scaling of multi-gate transistors thus leads to a regime where the transistor is expected to be operating in both the limits.

In this work, we analyze a Gate-All-Around nanowire transistor operating in such limiting conditions. There have been a few reports in the recent past where the performance of such a transistor has been evaluated in the QCL in an ideal condition and compared with the classical capacitance limit (CCL) where the gate oxide is dominant [8], [15], [16]. However, the effects of device non-idealities on transistor performance become extremely important in this regime. The presence of parasitic capacitance and interface traps significantly reduces the fraction of the useful (mobile) charge in the total switching charge in the strong quantum capacitance limit. On the other hand, strong energy quantization increases the relative channel resistance in this limit which in turn improves immunity of the transistor towards the source/drain series resistance. Thus, the combined effects of these non-idealities are expected to play a significant role in the transistor characteristics in the strong quantum capacitance limit and are addressed in detail in the present work.

The paper is organized as follows: we describe the simulation model used in this work in sec. II In sec. III we start with a formal definition of the Ultimate Quantum Capacitance Limit (UQCL), followed by a detailed analysis of the C-V characteristics of a nanowire transistor in this regime in presence of the interface traps. Sec. IV presents a comparative analysis between UQCL and CCL regime of operation on (i) the saturation of drain current and (ii) the subthreshold slope, both in the presence and absence of different device non-idealities. In the same section, we also analyze the scaling performance of the transistor in such limits. The performance benchmarking procedure that we follow in this work is based on the criteria proposed in [17]. This is followed by the discussion on the effects of the above said non-idealities on the scaling performance in sec. V We demonstrate that the device non-idealities should be carefully taken into account for realistic performance evaluation in a nanowire transistor in the UQCL regime. Finally, we conclude the paper in sec. VI.
II. A BALLISTIC NANOWIRE FET MODEL

Here we use a FET model, which is a variation of the ‘Top-of-the-Barrier’ model described in [12], for a gate-all-around (GAA) square nanowire of width \( W \), schematically shown in Fig. [1]. We assume a parabolic bandstructure of the nanowire described by an isotropic effective mass \( m^* \).

First, a hypothetical nanowire FET is assumed where the top of the source to channel barrier at \( x = x_0 \) is physically far off from the source and the drain eliminating any potential coupling from the source or the drain. Then, the gate voltage (\( V_g \)) governed 2-D potential profile \( \phi_0(y, z) \) and the carrier density profile \( N_0(y, z) \) are obtained at \( x = x_0 \) plane of the hypothetical FET using coupled 2-D Schrodinger-Poisson equations:

\[
\left( \frac{\hbar^2}{2m^*} \frac{\partial^2}{\partial y^2} + \frac{\hbar^2}{2m^*} \frac{\partial^2}{\partial z^2} + q\phi_0(y, z) + E_i^0 \right) \psi_i^0(y, z) = 0
\]

and

\[
\frac{\partial^2\phi_0(y, z)}{\partial y^2} + \frac{\partial^2\phi_0(y, z)}{\partial z^2} = \frac{q}{\epsilon} N_0(y, z)
\]

Here \( E_i^0 \) is the energy minimum of the \( i^{th} \) subband, \( q \) and \( \epsilon \) are the electronic charge and dielectric constant of the channel respectively. Assuming a ballistic channel, the carriers with \(+k\) and \(-k\) states are in equilibrium with the chemical potentials of the source (\( \mu_s \)) and the drain (\( \mu_d \)) respectively with \( \mu_d = \mu_s - qV_d \). Thus,

\[
N_0(y, z) = N_s(y, z) + N_d(y, z)
\]

where

\[
N_{s,d}(y, z) = \frac{1}{2} \sum_i \left[ \int_{E_0^i}^{\infty} D_i(E) f_{s,d}(E) \psi_i^0(y, z)^2 dE \right]
\]

\( D_i(E) \) is the 1D density of states (DOS) of the \( i^{th} \) subband in the channel given by

\[
D_i(E) = \frac{1}{\pi \hbar} \sqrt{\frac{m^*}{2(E - E_i^0)}} S(E - E_i^0)
\]

where \( S \) is a step function. \( f_{s,d}(E) \) are the Fermi-Dirac probabilities which, at temperature \( T \), are expressed as

\[
f_{s,d}(E) = \frac{1}{1 + e^{(E - \mu_{s,d})/k_BT}}
\]

where \( k_B \) is the Boltzmann constant. The wavefunction \( \psi_i^0(y, z) \) is assumed to be zero at the channel-gate dielectric interface. Once self-consistency is achieved among Eq. (1), (2) and (3), \( \phi_0(y, z) \) and \( N_0(y, z) \) correspond to the solutions at the top of the barrier for the hypothetical long channel ballistic FET.

Now, to obtain the characteristics of a realistic short channel ballistic nanowire FET, we define two terminal voltage dependent coupling parameters: the source and drain coupling parameters \( \alpha_s(V_g, V_d) \) and \( \alpha_d(V_g, V_d) \) respectively such that the actual potential distribution at the top of the source barrier is given by

\[
\phi(y, z) = \alpha_s V_s + \alpha_d V_d + (1 - \alpha_s - \alpha_d) \phi_0(y, z)
\]

For a given set of device parameters, the actual values of \( \alpha_s \) and \( \alpha_d \) can be extracted by fitting 3-D simulation data [12]. It is important to note that the final potential \( \phi(y, z) \) at the top of the barrier has been found using a
non-self-consistent perturbation to \( \phi_0(y, z) \), which, as we will see later, helps us to develop a set of semi-analytical equations to gain insights into transistor characteristics. However, this introduces small inaccuracies in the short channel terminal characteristics where the drain can have significant contribution to \( \phi(y, z) \). However, improved gate coupling due to the small \( m^* \) and strong geometrical confinement in the present context largely improves the gate to channel coupling, forcing \( \alpha_s \) and \( \alpha_d \) to be small validating our assumption in Eq. 7. Although the model is valid for any arbitrary dependence of the coupling parameters on terminal voltages, to simplify the problem, we further assume that \( \alpha_s \) and \( \alpha_d \) are independent of terminal voltages. In the rest of the paper, we assume a “well-behaved” transistor [12], [18], and do not explicitly mention about the length of the transistor, rather assume that the short channel effects are being captured by the parameters \( \alpha_s \) and \( \alpha_d \).

Using this \( \phi(y, z) \), new energy eigen values \( E_i \) and carrier density \( N(y, z) \) are recalculated. Finally, the ballistic current is obtained by Landaur’s formula:

\[
I_d = \frac{q}{\pi \hbar} \sum_i \left[ \int_{E_i}^{\infty} (f_s(E) - f_d(E))dE \right]
\]

The effect of series source and drain resistance \( (R_{s,d}) \) on the drain current are included as a posteriori effect [19].

In this work, the transistor, even in presence of interface traps, has been considered to be ballistic to keep the focus on the relative performance between the UQCL and the CCL, assuming that the increase in scattering from the traps has a similar impact on carrier transport in both the regimes. The numerical simulation method described in this section has been used to generate all the results to follow in the rest of the paper.

III. THE ULTIMATE QUANTUM CAPACITANCE LIMIT (UQCL) IN A NANOWIRE FET

A. Definition

Generally, a qualitative definition, namely \( C_q \ll C_{ox} \) is used to identify whether a transistor is in the QCL or not. To give a more quantitative definition taking care of the infinitely long high energy tail of the Fermi-Dirac probability, in the present work, we choose to call a FET to be operating in the UQCL when more than 99% of the carriers populate the first subband. Note that, in the present context of low \( m^* \) and strong geometrical confinement in a nanowire, this formal definition automatically meets \( C_q \ll C_{ox} \). In Fig. 2 we plot the maximum \( V_g \) allowed as a function of \( W \) and \( m^* \) to keep at least 99% of the carriers in the first subband. Thus, for any operating point in the \((V_g, m^*, W)\) space that lies below the indicated surface is said to be operating in the UQCL. In the CCL regime, the operating point is expected to be much above the surface where large number of subbands contribute. We also define a region called ‘Quasi-QCL’ which essentially represents those points which are just above the indicated surface in Fig. 2. Limited number of subbands contribute to the total carrier density in this regime. In the rest of the paper, we perform a comparative study of two sets of points in the \((V_g, m^*, W)\) space which are chosen carefully such that one of them \((V_g = 0.6V, m^* = 0.07m_0, W \leq 10nm)\) is into or very close to the UQCL regime of operation whereas the other \((V_g = 0.6V, m^* = 0.5m_0, W \geq 10nm)\) is closer to the CCL regime. Note that, in both the cases, we assume the same bandgap \((E_g)\) of 0.74eV to compare them under the same terminal bias.
conditions. This does not allow the difference in bandgap hide the insights that we are looking for. Though this is a theoretical construct, we do see such examples in reality for semiconductors that are relevant to MOSFET channel. For example, both In$_x$Ga$_{1-x}$As with $x = 0.53$ and Si$_{1-y}$Ge$_{y}$ with $y \approx 0.85$ have similar bandgap of $\sim 0.74$eV, however they show a wide difference in the electron effective masses \[20\]-\[22\]. From Fig. 2, it is understandable that for a given $V_g$, reducing the nanowire cross section or the effective mass of the channel material will push the operating condition deeper into UQCL.

B. Gate Capacitance

For an undoped nanowire, the total gate capacitance for the structure in Fig. 1 can be expressed as a summation of the contributions from all the subbands as

$$C_g(V_g) = \sum_i C_{gi}(V_g)$$  (9)

where

$$C_{gi}(V_g) = \frac{\partial Q_{gi}(V_g)}{\partial V_g} = q \left[ \frac{\partial}{\partial V_g} \int_{E_i}^{\infty} D_i(E) f(E) dE \right]$$  (10)

$Q_{gi}$ is the total mobile charge contribution from the $i^{th}$ subband. Using Eq. (5) and writing in terms of Fermi integral, we obtain

$$C_g(V_g) = \frac{q}{\pi \hbar} (2m^*k_BT)^{-1/2} \sum_i \frac{\partial}{\partial V_g} \left[ F_{-1/2} \left( \frac{\mu_s - E_i^0}{k_BT} \right) \right]$$  (11)

The numerically simulated C-V characteristics are shown in Fig. 3(a) and (b) for multi-gate nanowire in the two different regimes. It is clearly observed that, close to the CCL (Fig. 3(b)), $C_g$ scales almost linearly with the number of gates $N_G$. However, in the UQCL (Fig. 3(a)), the scaling is much slower with $N_G$ due to the small series quantum capacitance $C_q$. Consequently, migrating from double-gate to gate-all-around structure is expected to be less effective in the UQCL as compared to CCL regime.

We clearly observe the non-monotonicity of the nanowire C-V characteristics close to UQCL in Fig. 3(a). This is explained in Fig. 3(c) with a ‘parallel-subband-capacitance’ concept using the fact that the total mobile charge is a sum of the contributions from the individual subbands. Elementary electrostatics leads us to an equivalent capacitance model using $C_{ox}$ and individual subband quantum capacitances $C_{qi}$, as shown in the inset of Fig. 3(c). Unlike 2-D and 3-D structures, in a 1-D nanowire, the DOS of individual subbands falls with energy as $E^{-1/2}$ (Eq. 5). Into the UQCL, where only one subband contributes, the impact of the DOS is manifested as a drop in $C_g$ after certain $V_g$. This is arising from the non-monotonic behavior of the function $\frac{\partial}{\partial x} F_{-1/2}(x)$ in the Eq. (11). However, as we move away from UQCL, more number of subbands start contributing, and since each of them has its own threshold (Fig. 3(c)), the total gate capacitance shows multiple peaks. Thus, the number of peaks in these highly quantized nanowires is a signature of the number of subbands contributing to the total carrier density. However, as we go closer to CCL, as shown in Fig. 3(d), large number of closely spaced subbands contributing to the total carrier density destroy the humps.
We would like to mention a subtle point here: the physical origin of $C_q$ is different from $C_{ox}$. When $C_{ox}$ is small, the coupling between the gate and the channel degrades. However, a strongly confined, low $m^*$ channel, resulting in low $C_q$, provides an excellent gate control allowing the channel to attain almost uniformly the terminal gate voltage with negligible drop across the oxide.

C. Effect of Interface Traps

The reduced gate capacitance in the UQCL increases the impact due to the interface traps. The issue is aggravated by the fact that, to date, no high mobility channel MOSFET has been reported with excellent gate insulator interface [10], [23]. Thus, it becomes essential to include the effects of interface traps in the UQCL regime of operation. In this paper, we assume that the trap density $D_{it}$ is distributed uniformly over the bandgap of the channel material and hence the boundary condition of the normal components of the displacement vectors at the channel-insulator interface is changed to $D_{it}^{ch} - D_{it}^{ins} = \rho_{it}$ where $\rho_{it} = -qD_{it}\int_{-\Delta E}^{0} f(E) dE$. $\Delta E$ is the relative shift in the position of the intrinsic level. In Fig. 4(a) and (b), we plot the capacitance-voltage characteristics in presence of different $D_{it}$ for UQCL and CCL regime of operation. As expected, for a given $D_{it}$, particularly at high $D_{it}$, the characteristics are significantly altered, and the effect is more at UQCL compared to CCL. To investigate the effect on mobile charges, we also plot the mobile charge capacitance $C_m$ in Fig. 4(c) and (d) which we define as the rate of change of channel charge due to carriers with respect to gate bias. It clearly shows that with an increase in the $D_{it}$, the curves are shifted towards the right along the $V_g$ axis indicating an increase in the threshold voltage.

IV. NANOWIRE FET CHARACTERISTICS IN THE UQCL

A. Drain Current Saturation

Saturation of the drain current with increase in drain bias is an important requirement for the transistor to be useful for VLSI applications. For example, lack of saturation in the drain current leads to poor transfer characteristics of a CMOS inverter reducing the noise margin of an SRAM cell. In the following, we show that a ballistic FET shows better saturation characteristics in the UQCL regime as compared to the CCL.

Assuming $\beta = e^{qV_d/k_B T}$ and $G_c = \frac{q}{\pi \hbar}$, Eq. (8) reduces to

$$I_d = G_c \sum_i \left[ \int_{E_i}^{\infty} \left( \frac{1}{1 + \Gamma(E)} - \frac{1}{1 + \beta \Gamma(E)} \right) dE \right]$$

(12)

where $\Gamma(E) = e^{(E-E_s)/k_B T}$. Clearly, in the saturation region, $\beta \Gamma(E) >> 1$. Thus, Eq. (12) gives

$$I_d = G_c \left( \frac{\beta - 1}{\beta} \right) \sum_i \left( \int_{E_i}^{\infty} \frac{dE}{1 + \Gamma(E)} \right)$$

(13)

Integrating,

$$I_d = G_c k_B T \left( \frac{\beta - 1}{\beta} \right) \sum_i \ln \left( 1 + e^{\frac{E_i - E_s}{k_B T}} \right)$$

(14)
Now the perturbation to the original Hamiltonian in Eq. (1) due to introduction of the source and drain coupling in Eq. (7) is given by

$$\Delta H = -q(\phi - \phi_0) = q(-\alpha_s V_s - \alpha_d V_d + (\alpha_s + \alpha_d)\phi_0)$$ (15)

Using first order perturbation theory, the correction to the energy is obtained as

$$\Delta E_i = \langle \psi^0_i | \Delta H | \psi^0_i \rangle = -q\alpha_s V_s - q\alpha_d V_d + q(\alpha_s + \alpha_d)\langle \psi^0_i | \phi_0 | \psi^0_i \rangle$$ (16)

Hence, assuming source is grounded,

$$E_i = E^0_i + \Delta E_i = E^0_i - q\alpha_d V_d + q(\alpha_s + \alpha_d)\bar{\phi}^0_i$$ (17)

where $\bar{\phi}^0_i = \langle \psi^0_i | \phi_0 | \psi^0_i \rangle$. We should note that, both $E^0_i$ and $\bar{\phi}^0_i$ are almost independent of $V_d$ for relatively large $V_d$ in saturation region since the contribution of $N_d(y, z)$ to top of the source barrier carrier density $N(y, z)$ becomes relatively negligible in Eq. (3). Thus, Eq. (14) reduces to

$$I_d = G_c k_B T \left( \frac{\beta - 1}{\beta} \right) \sum_i \ln \left( 1 + \beta^{\alpha_s} e^{\theta_i} \right)$$ (18)

where $\theta_i = \mu_s - \frac{E^0_i - q(\alpha_s + \alpha_d)\bar{\phi}^0_i}{k_B T}$. Here, $\beta$ is the only parameter that is dependent on $V_d$. Thus, we can find the slope of the drain current in saturation region as

$$\frac{\partial I_d}{\partial V_d} = G_c q \beta^{-1} \sum_i \ln(1 + \beta^{\alpha_s} e^{\theta_i}) + G_c q \alpha_d (1 - \beta^{-1}) \sum_i \frac{1}{1 + \beta - \alpha_d e^{-\theta_i}}$$ (19)

Few conclusions can be drawn from Eq. (19): (1) If drain coupling parameter $\alpha_d \approx 0$ (the case of a ballistic long channel hypothetical FET), the second term is very small and the first term goes to zero exponentially with increase in $V_d$, leading to excellent saturation. This argument supports the results obtained from numerical simulations with $\alpha_d = 0$, as shown in Fig. 5(a). (2) For nonzero $\alpha_d$, $I_d$ does not completely saturate. However, with stronger quantization, the magnitude of $E^0_i$ is larger which in turn reduces $\theta_i$, hence reducing the magnitude of both the terms in Eq. (19). Consequently, if we operate close to the UQCL, a short channel ballistic FET will show better saturation characteristics as compared to a FET operating close to CCL. Similar conclusion can be drawn from the results of numerical simulations shown in Fig. 5(a) for $\alpha_d=0.04$ and $D_{it}=0$.

The presence of finite $D_{it}$ screens the gate voltage reducing the magnitude of $\theta_i$ which in turn degrades the saturation characteristics. In presence of extremely large $D_{it}$, as shown in Fig. 5(a), UQCL loses its saturation performance benefit over CCL. In Fig. 5(b), we show the output characteristics of the same devices, but with $R_s=R_d=200\Omega \cdot \mu m$ and $D_{it} = 10^{12} eV^{-1} cm^{-2}$ where it is observed that UQCL operation retains its performance benefit over CCL. This is due to the fact that stronger quantization in the UQCL compared to CCL increases the relative channel resistance, resulting in more immunity from series resistance effect.

From Eq. (18), we can also find the transconductance as

$$G = -\frac{\partial I_d}{\partial V_g} = -G_c \left( \frac{\beta - 1}{\beta} \right) \sum_i \left[ \frac{1}{1 + \beta - \alpha_d e^{-\theta_i}} \times \frac{\partial}{\partial V_g} \left( E^0_i + q(\alpha_s + \alpha_d)\bar{\phi}^0_i \right) \right]$$ (20)

The numerically computed transconductance (not shown) was found to have improved marginally in the UQCL compared to its CCL counterpart.
B. Subthreshold Slope

To obtain the subthreshold slope of such a nanowire FET, we find from Eq. (18):

\[
\ln(I_d) = \ln(Gc_kB_T) + \ln \left( \frac{\beta - 1}{\beta} \right) + \ln \left[ \sum_i \ln \left( 1 + \beta^{\alpha_d} e^{\theta_i} \right) \right] 
\]

(21)

which gives

\[
\frac{\partial \ln(I_d)}{\partial V_g} = \left( -\frac{1}{k_B T} \right) \left( \sum_i \frac{1}{(1 + e^{\eta_i})} \right) \times \sum_i \left[ \frac{e^{\eta_i}}{1 + e^{\eta_i}} \frac{\partial}{\partial V_g} \left( E_i^0 + q(\alpha_s + \alpha_d) \phi_i^0 \right) \right] 
\]

(22)

where \( \eta_i = \theta_i + \alpha_d \frac{qV_d}{k_B T} \). Now, at subthreshold, coupled with the low \( V_d \) operation, \( \eta_i < 0 \) and \( |\eta_i| > 1 \) which gives \( \ln(1 + e^{\eta_i}) \simeq e^{\eta_i} \). Also, at subthreshold, both \( \frac{\partial \phi_i^0}{\partial V_g} \) and \( \frac{\partial E_i^0}{\partial V_g} \) are nearly constant, and let us call them \( \kappa_1 \) and \( -\kappa_2 \). Thus we obtain,

\[
\frac{\partial \ln(I_d)}{\partial V_g} \simeq \frac{q}{k_B T} \left( \kappa_2 - (\alpha_s + \alpha_d) \kappa_1 \right)
\]

(23)

Hence, the subthreshold slope is

\[
S = \ln(10) \frac{\partial V_g}{\partial \ln(I_d)} = \left( \ln(10) \frac{k_B T}{q} \right) \times \frac{1}{\kappa_2 - (\alpha_s + \alpha_d) \kappa_1}
\]

(24)

In the case of infinite channel \( (\alpha_s=\alpha_d=0) \) with no \( D_{it} \), putting \( \kappa_2 \) as 1, the limit of subthreshold slope reduces to expected \( \ln(10) \frac{k_B T}{q} \) (=60mV/decade). Note that, both \( \kappa_1 \) and \( \kappa_2 \) are relatively insensitive to the region of operation (UQCL or CCL) resulting in similar subthreshold slopes, as shown in Fig. 5(c). The same trend remains even in the presence of moderately large \( D_{it} \) and hence both UQCL and CCL suffer from similar degradation in subthreshold slope in presence of \( D_{it} \). When \( \alpha_s \) and \( \alpha_d \) are small, from Eq. (24) we can express \( S \) in mV/decade as

\[
S \simeq \frac{60}{\kappa_2} \times \left( 1 + (\alpha_s + \alpha_d) \frac{\kappa_1}{\kappa_2} \right)
\]

(25)

which explains the almost linear degradation of subthreshold slope with \( \alpha_d \) at a given \( D_{it} \) in Fig. 5(c).

C. Scaling and Performance

In this section, we will compare the performance of the ballistic nanowire FET between UQCL and CCL. Due to stronger quantization, the ON current, normalized with the perimeter of the nanowire, degrades in the vicinity of UQCL, which is shown in Fig. 6(a). It can also be observed that in this regime, the normalized ON current is more sensitive to the nanowire dimension \( (W) \), which can be a potential cause to add variability to the device.

Let us now present the relative performance of UQCL and CCL in the light of the performance metrics proposed in [17]. It has been pointed out in [8] that there is no scaling disadvantage in CV/I metric while operating in the UQCL, for both ballistic as well as non-ballistic transport. However, following the discussion of C-V characteristics in sec. III we wish to point out that CV/I may not be able to reflect the intrinsic gate delay accurately in the UQCL due to the non-monotonic dependence of \( C_g \) on \( V_g \). This is explained in the inset of Fig. 6(b) where only one subband contributes to the total mobile charge pushing the transistor deep into UQCL. As shown, CV/I will overestimate the delay at point A whereas at point B, it will under estimate due to wrong computation of the total
charge as indicated by the dotted rectangles. We thus take \( \frac{\int C_g dV_g}{I_d} \) as the delay metric in this work which represents the gate delay more accurately by taking care of the details of the C-V curve.

Using Eqs. (11) and (18), we find the intrinsic gate delay as

\[
\tau = \left( \frac{2m^*}{(k_B T)^{3/2}} \right) \times \left[ \frac{\sum_i F_i - \frac{1}{2} \left( \frac{\mu_s - E_0}{k_B T} \right)}{\sum_i F_0 (\mu_s - E_i)} \right]
\]

Fig. 6(b) shows the numerically computed delay as a function of the nanowire dimension from two different metrics. It is found that in the UQCL, CV/I significantly over estimates the delay. However, it becomes closer to the \( \frac{\int C_g dV_g}{I_d} \) metric as we move out of the UQCL regime (larger \( W \)). Note that, in a very narrow nanowire, lower \( m^* \) channel material shows higher gate delay due to strong ON current degradation.

Energy-delay product, which has been obtained as \( E \cdot \tau = \left( \int Q dV \right) \left( \int C dV \right) / I_d \), is found to be very impressive at UQCL (Fig. 6(c)) as compared to its CCL counter part. This is because the transistor at UQCL operates at significantly lower switching charge. The normalized delay versus \( I_{on} / I_{off} \) has been plotted in Fig. 6(d) for both UQCL and CCL. It can be clearly seen that at UQCL, the transistor operation can be pushed towards the ideal right-bottom corner of the delay - \( I_{on} / I_{off} \) space. However, in the extremely deep UQCL (smaller \( W \) in the plot), the delay performance is adversely impacted due to excessive degradation of ON current.

V. SCALING AND PERFORMANCE IN PRESENCE OF NON-IDEALITIES

The fact that a transistor in its UQCL regime of operation switches relatively small amount of mobile charge, it is prone to performance degradation in presence of parasitic capacitances and traps since the fraction of the useful charge (mobile charge that drives the drain current) reduces significantly in the total switching charge. Here we separately discuss the effects of the interface traps, parasitic capacitance and source/drain series resistance, and finally comment on the combined effect of all of them.

Fig. 7(a) shows the effect of \( D_{it} \) on intrinsic delay of the FET, for two different \( m^* \). Increase in \( D_{it} \) increases the threshold voltage reducing the ON current and also increases the unused charge at the dielectric interface, degrading the gate delay. As expected, we observe that the delay in the larger \( m^* \) channel is less sensitive to \( D_{it} \) compared to the lower \( m^* \) and there is a severe degradation of delay at the narrower dimension for low \( m^* \) material. However, at comparatively larger dimension (\( W 10nm \)), it is still possible to retain the relative speed advantage of the low \( m^* \) case, even with significant \( D_{it} \). We observe similar trends when we have parasitic capacitance as the only source of non-ideality, as shown in Fig. 7(b). This is again due to the fact that when we are deep into quantum capacitance limit, presence of parasitic capacitance significantly reduces the ratio of mobile charge to total charge that is switched. However, it is interesting to note that the relative degradation of the intrinsic gate delay in the quantum capacitance limit is less compared to the classical capacitance limit in the presence of series source/drain resistance (\( R_{s,d} \)), which is shown in Fig. 7(c). This arises due to the increased channel resistance in the UQCL due to stronger energy quantization, improving the immunity from parasitic series resistance effect. In fact, deep into the quantum capacitance limit (lower \( m^* \) and lower \( W \)), presence of series resistance does not at all alter the
intrinsic gate delay, as shown in Fig. 7(c). Finally, 7(d) shows the combined effect of all the three non-idealities together which clearly shows a negative impact on the speed advantages that UQCL can have over CCL in the ideal scenario.

In Fig. 8(a), we present the energy-delay product in presence of similar non-ideal conditions showing a significant relative degradation in the UQCL. However, as shown in Fig. 8(b), even in the presence of the non-idealities, UQCL operation manages to offer significantly higher ON to OFF current ratio at comparable gate delays if we choose $W$ appropriately. We conclude that the extremely deep UQCL may not be the optimum design for a ballistic nanowire FET in presence of parasitics. At the same time, to retain the OFF performance advantage, better drain current saturation and immunity from series resistance, designing much away from UQCL is also not desirable. The ‘Quasi-QCL’ regime (where few subbands contribute) with low $m^*$ and moderately large $W$, can provide the optimum design to achieve both ON and OFF state performance.

VI. CONCLUSION

To conclude, a ballistic nanowire FET model has been proposed in the work, which is a variation of the ‘Top-of-the-barrier’ model, to analyze the transistor characteristics. The UQCL and CCL regimes have been formally defined in the $(V_g, m^*, W)$ design space based on the subband occupation. The non-monotonic C-V characteristics close to UQCL regime has been explained using a ‘parallel-subband-capacitance’ model. The small quantum capacitance has been found to play a critical role in this regime in presence of interface traps. The saturation characteristics of the drain current are found to improve in the UQCL as compared to CCL regime, both in presence and absence of parasitic resistance and interface traps. It has also been found that the subthreshold slope in UQCL is similar to CCL, even in the presence of interface traps. In the ideal condition, the scaling performance at UQCL regime has been shown to outperform its CCL counterpart. The UQCL operation has been found to be more immune from series resistance effect compared to CCL, whereas the presence of interface traps and parasitic capacitance are shown to diminish the relative performance advantages of the UQCL operation significantly. In presence of the combined effects of all these parasitics, the UQCL operation retains its $I_{on}/I_{off}$ advantage at comparable gate delay. A careful design in the ‘Quasi-QCL’ regime with low effective mass and moderate nanowire width is required to obtain optimum ON and OFF performance.

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FIGURE CAPTIONS:

Fig. 1: a): Schematic diagram of a gate-all-around nanowire FET. (b): Locus of the conduction band minimum from source to drain with the top of the barrier height at $x=x_0$.

Fig. 2: UQCL regime of operation in the $(V_g, m^*, W)$ space: More than 99% of the carriers populate only the first subband at any operating point below the indicated surface and hence operates in the UQCL, whereas multiple subbands are occupied at points above the surface. The CCL regime, where a large number of subbands contribute, is far above the surface.

Fig. 3: (a): Total gate capacitance $C_g$ for $m^*=0.07m_0$, $W=10$nm and EOT=1nm ($C_{ox}=0.35\times N_G$ in nF/m) shows non-monotonic C-V characteristics. The number gates $N_G$ is 2, 3 and 4. (b): Same as (a) with $m^*=0.5m_0$. (c): Contribution from individual subbands to the total capacitance causes multi-peak C-V close to UQCL. The inset shows a ‘parallel-subband-capacitance’ model. (d): Large number of subbands contribute to the total capacitance close to CCL resulting a smooth monotonic characteristics.

Fig. 4: Total gate capacitance $C_g$ in presence of interface traps for $W=10$nm with (a): $m^*=0.07m_0$ and (b): $m^*=0.5m_0$. The $D_{it}$ is assumed to be $10^{10}, 10^{11}, 10^{12}, 5\times 10^{12}$ and $10^{13}$ eV$^{-1}$cm$^{-2}$. (c)-(d): The corresponding mobile charge capacitance (rate of change of mobile charge in the channel with $V_g$) in the two scenarios.

Fig. 5: (a): Output characteristics of a gate-all-around 10nm X 10nm ballistic nanowire FET with EOT=1nm and $V_g=0.6$V for $\alpha_d=0$ and 0.04. The red and blue curves correspond to $m^*=0.07m_0$ and 0.5$m_0$ respectively. The circles and squares correspond to $D_{it}=0$ and $5\times 10^{12}$ eV$^{-1}$cm$^{-2}$ respectively. (b): The output characteristics in presence of parasitic source and drain resistance of 200$\Omega$-$\mu$m and $D_{it}=10^{12}$eV$^{-1}$cm$^{-2}$. The red and blue curves correspond to $m^*=0.07m_0$ and 0.5$m_0$ respectively. (c): Degradation of subthreshold slope with $D_{it}$ concentration for $\alpha_d=0$, 0.05, 0.1 and 0.15. The solid and dotted curves (which almost coincide) represent $m^*=0.07m_0$ and 0.5$m_0$ respectively. $\alpha_s=0.01$ for all the curves.

Fig. 6: (a): ON current as a function of nanowire width $W$. (b): Normalized intrinsic gate delay ($\tau$) computed from two different metrics as a function of $W$ for $m^*=0.07m_0$ and 0.5$m_0$. In the inset, The delay predicted by $CV/I$ is given by the area of the rectangles shown by the dotted lines, which depends on the operating condition and can either overestimate (at point A) or underestimate (at point B) the actual delay given by $\int C dV/I$. (c): Lower switching charge results in better energy-delay product ($E.\tau$) at UQCL. (d): Delay versus $I_{on}/I_{off}$ for different $W$. In all the plots, EOT=1nm, $\alpha_d=0.05$, $\alpha_s=0.01$, $V_d=0.6$V and $V_g=0.6$V have been assumed.

Fig. 7: (a): Normalized gate delay in presence of (a): only $D_{it}$ with $R_{s,d}=0$ and $C_L=0$, (b): only $C_L$ with $D_{it}=0$ and $R_{s,d}=0$, (c): only $R_{s,d}$ with $D_{it}=0$ and $C_L=0$ and (d) $R_{s,d}=200\Omega$-$\mu$m, $D_{it}=5\times 10^{11}$cm$^{-2}$eV$^{-1}$ and $C_L=0.5$nF/m. In all the plots, the blue lines with star and squares represent the reference delay with zero non-ideality for $m^*=0.07m_0$ and $m^*=0.5m_0$ respectively. EOT=1nm, $\alpha_d=0.05$, $\alpha_s=0.01$, $V_d=0.6$V and $V_g=0.6$V have been assumed.

Fig. 8: (a): Energy-delay product and (b) gate delay versus $I_{on}/I_{off}$ plot with $R_{s,d}=200\Omega$-$\mu$m, $D_{it}=5\times 10^{11}$cm$^{-2}$eV$^{-1}$ and $C_L=0.5$nF/m. In both the plots, the blue lines with star and squares represent the reference
with zero non-ideality for $m^* = 0.07m_0$ and $m^* = 0.5m_0$ respectively. EOT=1nm, $\alpha_d = 0.05$, $\alpha_s = 0.01$, $V_d = 0.6\text{V}$ and $V_g = 0.6\text{V}$ have been assumed.
Fig. 1.
Fig. 2.

$V_{g_{\text{max}}} (V)$ for first subband occupation

- $W$ (nm)
- $m^*/m_0$
Fig. 3.
Fig. 4.
Fig. 5.
Fig. 6.
Fig. 7.
Fig. 8.