A surface-potential-based drain current model suitable for poly-Si thin film transistors with thin body and thin gate oxide

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Abstract. Polycrystalline silicon thin film transistors with thin body and thin gate oxide can realize high performance and relative low power consumption simultaneously. Considering their wide applications, a surface-potential-based drain current model suitable for devices with the above structure is derived on charge sheet approximation considering the double exponential trap state distribution, the interface charge and the effect of the back surface potential. According to the calculated areal density of the charges under the gate oxide, the ionized acceptors and the trapped charges, the areal density of the inversion charge is obtained. Under several mathematical treatments, a surface-potential-based drain current model suitable for devices with thin body and thin gate oxide is developed accompanying the quantitative model-validity conditions for low and high state densities respectively. Under high and low state densities respectively, this proposed surface-potential-based drain current model is verified by 2D-device simulation in devices’ transfer characteristics under various drain biases in the situations without or with interface charge.

1. Introduction
Polycrystalline silicon thin film transistors (poly-Si TFTs) with thin body and thin gate oxide can realize high performance and relative low power consumption simultaneously [1]. Considering their wide applications, the drain current model suitable for devices with the above structure is in dire need of being developed. As the new-generation approach, the surface-potential-based modeling strategy [2, 3] originating from the Pao-Sah model [4] takes the lead position in compact MOSFET modeling. Meanwhile, charge sheet approximation [5] considering both drift and diffusion components with the merit of its simplification and convenience for calculation is widely adopted in device modeling. Therefore, based on the charge sheet approximation, a surface-potential-based drain current model suitable for poly-Si TFTs with thin body and thin gate oxide is to be derived in this work.

2. Model formulation
For n-type fully-depleted poly-Si TFT with the channel length $L$ and the channel width $W$, it is assumed with the very thick insulator substrate. The $z$ direction is perpendicular to the poly-Si/oxide front interface where $z$ is 0. The $y$ direction is along the channel where $y=0$ at the source end and $y=L$ at the drain end. For devices’ turn-on operation, only the tail and deep acceptor-like trap states in the
bulk are taken into account with the double exponential distribution [6]. Moreover, the role of the interface charge is considered. By calculating the areal density of the trapped charges with the assumed electrostatic potential distribution as

$$\psi = \psi_{sf} + \frac{\psi_{sb} - \psi_{df}}{t_{si}} z$$

where $\psi_{sf}$ is the front surface potential, $\psi_{sb}$ is the back surface potential and $t_{si}$ is the thickness of the poly-Si layer, the areal density of the charges under the gate oxide and the ionized acceptors respectively, the areal density of the inversion charge is obtained as

$$Q_i = -C_{ox} \{ (V_b - V_{fb} - \psi_{sf} - qN_{a0} t_{si}) - \frac{t_{si}}{C_{ox}} \} \frac{N_{deep} K T_d}{\psi_{sf} - \psi_{sb}} \exp\left(\frac{\psi_{sf} - \phi_f - V_c - E_g}{2q}\right)[1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{K T_d / q}\right)]$$

$$+ \frac{N_{tail} q \phi_f}{\alpha (\psi_{sf} - \psi_{sb})} \exp\left(\frac{\psi_{sf} - \phi_f - V_c - E_g}{2q}\right)[1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{\phi_f}\right)]\}$$

where $C_{ox}$ is the gate oxide capacitance per unit area, $V_b$ is the gate voltage, $V_{fb}$ is the flat band voltage, $q$ is the electron charge, $N_{a0}$ is the active acceptor concentration, $N_{deep} = g_a \frac{K \pi T}{\sin\left(\frac{\pi T}{T_d}\right)}$ where $g_a$ is the deep state density at the conduction band edge, $T$ is the absolute temperature, $K$ is the Boltzmann constant and $T_d$ is the characteristic temperature of the deep states, $N_{tail} = g_s KT_s\left[\frac{2 \pi - 4}{3} \left(\frac{T}{T_i}\right)^2 + (6 - 2 \pi) \frac{T}{T_i} + \frac{4 \pi - 8}{3}\right]$ where $g_s$ is the tail state density at the conduction band edge and $T_i$ is the characteristic temperature of the tail states, $\alpha = -\frac{4}{15} \left(\frac{T}{T_i}\right)^2 + \frac{T}{T_i} + \frac{1}{15}$, $\phi_f$ is the thermal voltage, $\phi_f$ is the bulk Fermi potential, $V_c$ is the channel potential and $E_g$ is the band gap.

Define $A = V_b - V_{fb} - \psi_{sf} - qN_{a0} t_{si}$ and $B = \frac{N_{deep} K T_d}{\psi_{sf} - \psi_{sb}} \exp\left(\frac{\psi_{sf} - \phi_f - V_c - E_g}{2q}\right)[1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{K T_d / q}\right)]$

$$+ \frac{N_{tail} q \phi_f}{\alpha (\psi_{sf} - \psi_{sb})} \exp\left(\frac{\psi_{sf} - \phi_f - V_c - E_g}{2q}\right)[1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{\phi_f}\right)]$. Therefore, (1) can be rewritten as

$$Q_i = -C_{ox} (A - \frac{t_{si}}{C_{ox}} B)$$

(2)

And it is obviously that

$$B < \frac{N_{deep} K T_d}{\psi_{sf} - \psi_{sb}} [1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{K T_d / q}\right)] + \frac{N_{tail} q \phi_f}{\alpha (\psi_{sf} - \psi_{sb})} [1 - \exp\left(\frac{\psi_{sb} - \psi_{df}}{\phi_f}\right)]$$

(3)

When devices are with low trap densities, the depletion approximation model is adopted [7]. Therefore, the relationship between the front and back surface potential can be expressed as $\psi_{sf} - \psi_{sb} = \frac{q}{2\varepsilon_{si}} N_{a0} t_{si}^2$ where $\varepsilon_{si}$ is the silicon permittivity. Substituting this into (3), it can be obtained that
\[ B < \frac{2e_{e_s}N_{\text{dep}}KT_d}{qN_{\text{sta}}t_{st}^2} [1 - \exp(-q^2N_{\text{sta}}t_{st}^2)] + \frac{2e_{e_s}N_{\text{tail}}\phi_i}{2e_{e_s}\phi_i} [1 - \exp(-qN_{\text{sta}}t_{st}^2)] = DL \] (4).

When devices are with high trap densities, the \( \psi_{sb} = 0 \) V model is used [7]. So (3) turns into
\[ B < \frac{N_{\text{dep}}KT_d}{\psi_{sf}} [1 - \exp(-\frac{-\psi_{sf}}{KT_d/q})] + \frac{N_{\text{tail}}q\phi_i}{\alpha\psi_{sf}} [1 - \exp(\alpha - \frac{-\psi_{sf}}{\phi_i})] < \frac{N_{\text{dep}}KT_d}{\psi_{sf}} + \frac{N_{\text{tail}}q\phi_i}{\alpha\psi_{sf}} \]
\[ \leq \frac{N_{\text{dep}}KT_d}{\psi_{sf}(0)} + \frac{N_{\text{tail}}q\phi_i}{\alpha\psi_{sf}(0)} = DH \] (5).

In the meanwhile, it can be obtained that \( A_{\text{min}} = V_g - V_{fb} - \Psi_{sf}(L) - qN_{\text{sta}}t_{st} \frac{t_{st}}{C_{ox}} \). When devices are with low trap densities, if \( \beta A_{\text{min}} \geq \frac{t_{st}}{C_{ox}}DL \) where \( \beta \) is chosen as 0.2, i.e.
\[ t_{st} \frac{t_{st}}{C_{ox}} \leq \frac{\beta A_{\text{min}}e_{e_s}}{DL} \] (6),
or when devices are with high trap densities, if \( \beta A_{\text{min}} \geq \frac{t_{st}}{C_{ox}}DH \), i.e.
\[ t_{st} \frac{t_{st}}{C_{ox}} \leq \frac{\beta A_{\text{min}}e_{e_s}}{DH} \] (7),
the term \( \frac{t_{st}}{C_{ox}}B \) is negligible compared with the term \( A \) in (2). Therefore, when the condition (6) for devices with low trap densities or the condition (7) for devices with high trap densities is satisfied, (2) turns into
\[ Q = -C_{ox}(V_g - V_{fb} - \Psi_{sf}(L) - qN_{\text{sta}}t_{st} \frac{t_{st}}{C_{ox}}) \] (8).

So the drain current based on charge sheet approximation, considering both drift and diffusion currents, can be written as
\[ I = \frac{W\mu C_{ox}}{L} \left\{ (V_g - V_{fb} + \phi_i - qN_{\text{sta}} \frac{t_{st}}{C_{ox}}) [\Psi_{sf}(L) - \Psi_{sf}(0)] - \frac{1}{2} [\Psi_{sf}^2(L) - \Psi_{sf}^2(0)] \right\} \] (9)
where \( \mu \) is the channel mobility assumed to be constant.

Obviously, condition (6) or (7) is more likely to be satisfied when devices are with thin body and thin gate oxide. So (9) is a surface-potential-based drain current model suitable for poly-Si TFTs with thin body and thin gate oxide accompanying the quantitative model-validity conditions (6) for low state densities and (7) for high state densities. And as the surface potential is concerned, it can be calculated by the front and back surface potential equation [8]
\[ \psi_{sf} = V_g - V_{fb} - \frac{1}{C_{ox}} \left\{ 2qe_{e_s}N_{\text{sta}}(\psi_{sf} - \psi_{sb}) + N_{\text{sta}} \phi_i \exp(-V_c - 2\phi_i) \right\} \exp(\frac{\psi_{sf}}{\phi_i}) - \exp(\frac{\psi_{sb}}{\phi_i}) \]
\[ + N_{\text{dep}} \frac{KT_d}{q} \exp(-\frac{-\phi_{fo} - V_c - \frac{E_g}{2q}}{KT_d/q}) \left\{ \exp(\frac{\psi_{sf}}{KT_d/q}) - \exp(\frac{\psi_{sb}}{KT_d/q}) \right\} + N_{\text{tail}} \frac{\phi_i}{\alpha} \exp(\alpha - \frac{-\psi_{sf} - V_c - \frac{E_g}{2q}}{\phi_i}) \psi_{sf} - \psi_{sb} - V_c - \frac{E_g}{2q} \}
\[ - \exp(\alpha - \frac{-\psi_{sf} - V_c - \frac{E_g}{2q}}{\phi_i}) \phi_i \}
\] (10)
where \( Q_{ic} \) is the areal interface charge density, and the coupling effect of the front and back surface potentials [8].
\[
\psi_{ob} = \psi_{of} - \frac{q}{2e\alpha} N_{i\alpha} \cdot \frac{t_s}{e_{ox}}^2 - \frac{q}{e_{ox}} \left( \frac{t_s}{e_{ox}} \right)^2 (N_i^2 \phi_i^2 \exp(\psi_{of}) - \exp(\psi_{of})) + \frac{N_i^2 K T_o}{q} \left( \exp\left(\frac{\psi_{of}}{K T_o/q}\right) - \exp\left(\frac{\psi_{ob}}{K T_o/q}\right) \right) + N_s \phi_s^2 \exp(\psi_{of}) - \exp(\psi_{of}) \right]
\]

\[
+ N_s \phi_s^2 \exp(\psi_{of}) - \exp(\psi_{of}) \right)
\]

\[
\psi_{ob} = \psi_{of} - \frac{q}{2e\alpha} N_{i\alpha} \cdot \frac{t_s}{e_{ox}}^2 - \frac{q}{e_{ox}} \left( \frac{t_s}{e_{ox}} \right)^2 (N_i^2 \phi_i^2 \exp(\psi_{of}) - \exp(\psi_{of})) + \frac{N_i^2 K T_o}{q} \left( \exp\left(\frac{\psi_{of}}{K T_o/q}\right) - \exp\left(\frac{\psi_{ob}}{K T_o/q}\right) \right) + N_s \phi_s^2 \exp(\psi_{of}) - \exp(\psi_{of}) \right]
\]

where \( N_i = N_{i\alpha} \cdot \exp\left(-V_i - \frac{2\phi_{\alpha}}{2q}\right) \), \( N_s = N_{s\alpha\alpha} \cdot \exp\left(\frac{-\phi_{\alpha} - V_s - \frac{E_{\alpha}}{2q}}{K T_o/q}\right) \), and \( N_i = N_{i\alpha} \cdot \exp\left(\frac{-\phi_{\alpha} - V_i - \frac{E_{\alpha}}{2q}}{K T_o/q}\right) \).

By solving (9), (10) and (11), the drain current can be obtained.

3. Result and discussion

For n-type fully-depleted poly-Si TFTs with the very thick insulator substrate, including both tail and deep acceptor-like trap states in the bulk and the interface charge, the above proposed surface-potential-based drain current model (9) suitable for devices with thin body and thin gate oxide is compared with the simulation results of the two-dimensional-device simulator MEDICI [9] from the transfer characteristics of both low and high state densities for without or with interface charge situation respectively. The devices’ parameters used in the model are shown in Table 1.

Figure 1 to figure 4 show transfer characteristics of devices with the low and high state densities under different drain biases when \( Q_{ox} = 0 \) C/cm\(^2\) and \( Q_{ox} = 1.6 \times 10^8 \) C/cm\(^2\) respectively. In figure 1 and figure 3, \( g_d = 1 \times 10^{18} \) cm\(^3\)eV\(^{-1}\) and \( g_d = 5 \times 10^{18} \) cm\(^3\)eV\(^{-1}\) for low state density. In figure 2 and figure 4, \( g_d = 2 \times 10^{19} \) cm\(^3\)eV\(^{-1}\) and \( g_d = 1 \times 10^{20} \) cm\(^3\)eV\(^{-1}\) for high state density. In figure 1 to figure 4, when the gate voltage varies from 2 V to 20 V, the drain current model (9) matches the 2D-device simulation under \( V_d = 0.1 \) V, 0.5 V and 1 V respectively.

4. Conclusion

A surface-potential-based drain current model suitable for poly-Si TFTs with thin body and thin gate oxide is proposed considering the double exponential trap state distribution, the interface charge and the effect of the back surface potential. According to the calculated areal density of the charges under the gate oxide, the ionized acceptors and the trapped charges, the areal density of the inversion charge is obtained. Under several mathematical treatments, a surface-potential-based drain current model suitable for devices with thin body and thin gate oxide is developed based on charge sheet approximation, accompanying the quantitative model-validity conditions for low and high state densities respectively. Under high and low state densities respectively, this proposed surface-potential-based drain current model is verified by 2D-device simulation in devices’ transfer characteristics under various drain biases in the situations without or with interface charge.

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Table 1. Values of parameters used in the model.

| Symbol | Parameter                                      | Value                                |
|--------|------------------------------------------------|--------------------------------------|
| $N_{a0}$ | active acceptor concentration                   | $10^{16}$ cm$^{-3}$                      |
| $g_d$   | deep state density at the conduction band edge | $1 \times 10^{18}$ cm$^{-3}$eV$^{-1}$ (for low state density) |
|         |                                                | $2 \times 10^{19}$ cm$^{-3}$eV$^{-1}$ (for high state density) |
| $g_t$   | tail state density at the conduction band edge | $5 \times 10^{18}$ cm$^{-3}$eV$^{-1}$ (for low state density) |
|         |                                                | $1 \times 10^{19}$ cm$^{-3}$eV$^{-1}$ (for high state density) |
| $T_d$   | characteristic temperature of the deep states  | 1060K                                  |
| $T_t$   | characteristic temperature of the tail states  | 335K                                   |
| $T$     | absolute temperature                            | 300K                                   |
| $t_{ox}$| gate oxide thickness                            | 1 nm                                   |
| $V_{fb}$| flat band voltage                               | -0.6 V                                 |
| $Q_{ic}$| areal interface charge density                  | 0 C/cm$^2$ (without interface charge)  |
|         |                                                 | $1.6 \times 10^8$ C/cm$^2$ (with interface charge) |
| $t_{si}$| thickness of the poly-Si layer                  | 60 nm                                  |
| $\mu$  | channel mobility                                | 600 cm$^2$/V$\cdot$S                    |
| $W$     | width of the channel                            | 10 $\mu$m                              |
| $L$     | length of the channel                           | 10 $\mu$m                              |

Figure 1. Transfer characteristics of device with low state density under different drain biases via the drain current model (9) and the 2D-device simulation for $Q_{ic} = 0$ C/cm$^2$.

Figure 2. Transfer characteristics of device with high state density under different drain biases via the drain current model (9) and the 2D-device simulation for $Q_{ic} = 0$ C/cm$^2$.

Figure 3. Transfer characteristics of device with low state density under different drain biases via the drain current model (9) and the 2D-device simulation for $Q_{ic} = 1.6 \times 10^8$ C/cm$^2$.

Figure 4. Transfer characteristics of device with high state density under different drain biases via the drain current model (9) and the 2D-device simulation for $Q_{ic} = 1.6 \times 10^8$ C/cm$^2$. 