Large-Signal Stability Guarantees for Cycle-by-Cycle Controlled DC–DC Converters

Xiaofan Cui, Graduate Student Member, IEEE, and Al-Thaddeus Avestruz, Senior Member, IEEE

Abstract—Stability guarantees are critical for cycle-by-cycle controlled dc–dc converters in high performance applications including microprocessors and LiDAR. Traditional stability analysis on cycle-by-cycle dc–dc converters is incomplete because the inductor current ramps are considered fixed; however, inductor ramps are dependent on the output voltage in large-signal transients, which results in a previously neglected feedback path that often creates instability. We present a new modeling approach together with large-signal stability theory based on a linear fractional transformation of the feedback system. This analysis reveals analytical stability criteria that are straightforward to ensure in practice; the criteria bound sufficient conditions for two practical time constants that are design parameters familiar to power electronics engineers: $L/R$ and $RC$ time constants of the dc–dc converter. These time constants determine the amount of coupling between the current ramp and the output voltage. Specifically, we perform the analysis, simulation, and hardware verification on a buck converter, but the theory and modeling methods apply to other hard-switching power converters.

Index Terms—Cycle-by-cycle control, large-signal stability analysis, DC-DC converters.

I. INTRODUCTION

Power electronics engineers need faster transient performance from cycle-by-cycle control at high switching frequencies. At the same time, they need a way to determine whether their choice of power electronics design is stable for large-signal transients, which appear in critical applications. Often in practice, instability when it appears, is unexpected. This letter offers analysis and criteria for an instability that is often encountered when the output voltage has a large-signal variation that couples to the inductor current ramp at high switching frequencies.

This letter focuses on one of the most widely-used cycle-by-cycle controlled power converters — current-mode dc–dc converters, which have a number of varieties including constant on-time control [1], constant off-time control [2], and fixed-frequency peak-current control [3]; specifically, we discuss the buck converter in this letter, but the theory and methods can be extended to other types of converters, e.g., boost converters [2], among others. In existing large-signal stability analysis for current-mode converters, the current control loop and the outer voltage loop in current-mode dc–dc converters are considered decoupled and are designed separately; this cannot model a common current control loop instability. To address this deficiency, we develop a new large-signal stability theory which models the current-mode buck converter as a feedback connection system, as shown in Fig. 1, in the switching-synchronized sampled-state space (SSS). While the small-signal stability in SSS has been widely discussed in [4], the large-signal stability of cycle-by-cycle controlled dc–dc converters had not been adequately addressed. Several discrete-time robust control tools, including small-gain theorem, dissipativity theory, and Lure system theory are utilized to rigorously study the stability of the resulting discrete-time nonlinear system. The specific list of contributions are as follows:

1) Guarantee of the large signal stability boundary of cycle-by-cycle controlled dc–dc converters.
2) Providing a closed-form criterion for the values of inductance and load, switching frequency, which is useful and straightforward for the practical power electronics hardware engineer.

This letter is organized as follows: (i) Section I introduces this letter; (ii) Section II is a review of the state of the art; (iii) Section III develops the large-signal models for the current control loop and voltage block of a current-mode buck converter using constant on-time control; (iv) the ultimate goal, which is illustrated in Section IV, is to derive...
the large-signal stability guarantees for current mode dc-dc converters; (v) Section V concludes this letter.

II. REVIEW OF THE STATE OF THE ART

Cycle-by-cycle controlled dc-dc converters are widely used in PoL (point-of-load [5]) regulators, VRMs (voltage regulation modules [6, 7]), and LiDAR power supplies [8] because of its faster transient response compared to the traditional averaging-based control, which is based on a window of many cycles [9]. However, this well-known averaging theory cannot model the fast switching-frequency-scale dynamics of cycle-by-cycle controlled dc-dc converters due to the slow-varying perturbation assumption. Cycle-by-cycle control is important in converters from 1 W to 1 kW where the speed-power tradeoff is challenging.

However, during large-signal transients, the output voltage significantly changes, hence the inductor current ramp changes every switching cycle. The cycle-varying inductor current ramp affects the amount of charge pumped into the output, and ultimately affects the output voltage dynamics. The traditional stability analysis of the current control loop, which fully neglects the voltage block and assumes a fixed inductor current ramp, cannot guarantee the stability of the current control loop for large-signal transients. The stability of the current control loop, which is referred to as “fast-scale stability”, was studied by assuming the rising ramp and falling ramp of the inductor current are fixed as $m_1$ and $m_2$ [10]. The stability of the voltage block, which is referred to as “slow-scale stability”, was studied by utilizing averaging theory because of neglecting voltage ripple and treating the current control loop as a controlled current source. A perturbation model of a fixed frequency converter using an averaging discrete-time model with uniform sampling was used to model a variable frequency converter in [11]; unfortunately, this model does not exhibit routinely encountered subharmonic oscillations.

This letter focuses on one of the most widely-used cycle-by-cycle controlled dc-dc converters — current-mode dc-dc converters, which have a number of varieties including constant on-time control [1], constant off-time control [2], and fixed-frequency peak-current control [3]. In comparison to the bilinear nonlinearity in the averaging model, the converter model in $5S$ displays higher fidelity nonlinear behaviors that affect stability. The $5S$ model is a more accurate and tractable alternative [4] to conventional averaging models. A similar stability analysis was performed in [12] in continuous time; we extended this analysis through mathematical proof in a sampled state space [13].

III. 5S MODELING OF CONSTANT ON-TIME BUCK CONVERTER

A. Converters, Systems, and Definitions

A class $\Sigma$ buck converter is shown in Fig. 2 that imposes a constant on time through a timer and a flip-flop [4]. The voltage from a current sense resistor $R_s$ triggers the valley current response through a comparator that is commanded by a voltage controller. This switched converter is modeled in Simulink and a switched simulation is performed in the time domain. The inductor current and capacitor voltage trajectories are shown in Fig. 3. $V_{in}$ and $T_{on}$ are the input voltage and constant on time, respectively. Off time $t_{off}[n]$ varies every cycle and is determined by the event when the current sensor output equals the current command $i_c$. Because of the uncertainty in the inductor current measurement, the current sensor output does not equal the actual inductor current. We denote the uncertainty by $w(t)$, which is defined in [13]. According to the cycle-by-cycle control law in [4], the output voltage $v[n]$ is sampled during the on-time, once per switching cycle. The sampling time point for $v[n]$ can be expressed as the convex combination of the time of the inductor current valley $t_v[n]$ and the time for the inductor current peak $t_p[n]$, $t_v[n] = \lambda t_v[n] - (1 - \lambda) t_p[n]$; the parameter $\lambda$ is between 0 and 1. The slopes of the rising and falling ramps of the inductor current are denoted by $m_1[n] = (V_{in} - v[n])/L$ and $m_2[n] = v[n]/L$, respectively.

We introduce the one-cycle-delayed valley current sequence $[v_{out}[n]]$ as $v_{out}[n] = v[n] + T_{off}$. We denote the equilibrium of the system by $v_{out}[n] = V_{out}$, $i_c[n] = I_c$, $v_{out}[n] = V_{out}$, and $t_{off}[n] = T_{off}$. The equilibrium is defined by the following:

$$I_c \triangleq \frac{V_{out}}{R} - \frac{1}{2} \frac{V_{in} - V_{out}}{L} T_{on}, \quad v[n] = I_c - w(T_{off}), \quad (1a)$$

$$T_{off} \triangleq \frac{V_{in} - V_{out}}{V_{out}} T_{on}, \quad T_{on}^{ss} \triangleq T_{on} + T_{off}. \quad (1b)$$

![Fig. 2. Schematic diagram of a digitally-controlled current-mode constant on-time buck converter.](image)

![Fig. 3. Constant on-time buck converter using cycle-by-cycle current-mode control.](image)
to \( t_{i,n+1} \), and output charge of the capacitor, respectively. To prevent the switching transient from disturbing the valley current detection denoted by the sense voltage \( v_s \) in Fig. 2, the time-varying off-time is bounded from below [4] and to avoid the misdetection of the valley current event, the time-varying off-time is bounded from above by

\[
T_{\text{off}}^\text{min} \leq t_{\text{off}}[n] \leq T_{\text{off}}^\text{max}.
\]

IV. STABILITY AND CONTROL PERFORMANCE ANALYSIS OF CONSTANT ON-TIME BUCK CONVERTERS

The current control loop includes a feedback path from the output voltage, shown in Fig. 1, that had not been considered previously as a cause for instability. The nonlinear dynamics of the current control loop together with this output voltage feedback is modeled in SS as a separable static nonlinearity \( \psi(\cdot) \) and time-dependent \( m_2[n] \), where \( z^{-1} \) is a delay, in Fig. 4, which generalizes into the linear fractional transformation system in Fig. 5.

A. Current Control Loop

In this section, we propose a method to calculate the \( \mathcal{L}_2 \) gain from \( \bar{v}[n] \) to \( \bar{c}_p[n] \), denoted by \( \Gamma_{\bar{v} \rightarrow \bar{c}_p} \). The proposed method is the discrete-time domain extended version of the result on \( \mathcal{L}_2 \) gains of norm-bound LDI in [12, Sec. 6.3.2].

The method applies to the system that can be expressed in \( F_u(L, \Delta) \) form, as shown in Fig. 5, with mathematical representation as

\[
x[n+1] = Ax[n] + B_1 h[n] + B_2 r[n],
\]

\[
\rho[n] = C_1 x[n] + D_{11} h[n] + D_{12} r[n],
\]

\[
e[n] = C_2 x[n] + D_{21} h[n] + D_{22} r[n],
\]

\[
h[n] = \Delta (\rho[n]).
\]

The upper bound of the \( \mathcal{L}_2 \) gain can be numerically calculated using the following Theorem:

**Theorem I:** Assume \( \Delta : \mathbb{R} \rightarrow \mathbb{R} \) is an \([\hat{\alpha}, \hat{\beta}]\) sector-bounded nonlinearity. Also, assume \( F_u(L, \Delta) \) is well-posed. If \( \exists \mathcal{P} > 0, \Lambda \geq 0, \) and \( \gamma > 0 \) such that

\[
\begin{bmatrix}
\hat{\alpha} \hat{\beta} \\
\hat{\alpha} + \hat{\beta} \\
-\hat{\alpha} \hat{\beta} \\
\hat{\alpha} + \hat{\beta} \\
\end{bmatrix}
\begin{bmatrix}
A^T PA - P & A^T PB_1 & A^T PB_2 \\
B_1^T PA & B_1^T PB_1 & B_1^T PB_2 \\
B_2^T PA & B_2^T PB_1 & B_2^T PB_2 - \gamma^2 I \\
\end{bmatrix}
+ \Lambda
\begin{bmatrix}
C_1 & D_{11} & D_{12} \\
0 & I & 0 \\
\end{bmatrix}^T
\begin{bmatrix}
-\hat{\alpha} \hat{\beta} \\
\hat{\alpha} + \hat{\beta} \\
\hat{\alpha} + \hat{\beta} \\
\hat{\alpha} + \hat{\beta} \\
\end{bmatrix}
\begin{bmatrix}
C_1 & D_{11} & D_{12} \\
0 & I & 0 \\
\end{bmatrix}
+ \begin{bmatrix}
D_{21}^T \\
D_{22}^T \\
\end{bmatrix}
\begin{bmatrix}
C_2 & D_{12} & D_{22} \\
\end{bmatrix} < 0,
\]

then \( \|F_u(L, \Delta)\| \leq \gamma \).
Proof Sketch: The Theorem can be proved using the dissipativity theory. The storage function can be constructed as $V(x) = x^T P x$. Multiply the left and right by $[x[n]]^T p[n] [x[n]]^T r[n]^T$ and its transpose to obtain
\[
V(x[n + 1]) - V(x[n]) + \Delta h[n] - \dot{\alpha} p[n] \left( \beta p[n] - h[n] \right) + \left( e[n]^T e[n] - \dot{\gamma}^2 r[n]^T r[n] \right) < 0.
\] (8)

The second term with $\dot{\alpha}$ and $\dot{\beta}$ is non-negative because of the sector-bounded nonlinearity and positive scalar term $\Delta$. By summing up both sides of (8), we have $\| e \|^2 < \dot{\gamma}^2 \| r \|^2$, hence the $L_2$ norm of $F_u(L, \Delta)$ is bounded by $\dot{\gamma}$. The detailed proof can be found in [14].

We can reformulate the current control loop in a unitless $F_u(L, \Delta)$ form as
\[
\begin{align*}
\tilde{v}^*[n + 1] &= 0\tilde{v}^*[n] + \tilde{i}_e[n] + 0\tilde{u}[n], \\
\tilde{i}_e[n] &= \tilde{v}^*_e[n] - \tilde{i}[n] + \tilde{u}[n], \\
\tilde{v}^*_e[n] &= \tilde{v}^*_e[n] + 0\tilde{u}_e[n] + 0\tilde{u}[n], \quad \tilde{i}[n] = \Delta(\tilde{i}_e[n]).
\end{align*}
\] (9)

where
\[
\tilde{u}[n] = \frac{T_{ss}}{L} \tilde{v}[n], \quad \Delta(\tilde{i}_e) = -\psi \left( \frac{\tilde{i}_e}{m_2[n]} \right),
\] (10)

and $\Delta(\tilde{i}_e) \in [\dot{\alpha}, \dot{\beta}]$ is a sector-bounded time-varying nonlinearity.

From Theorem 1, the gain $\dot{\gamma}$ of unitless $F_u(L, \Delta)$ form can be obtained from following optimization problem:
\[
\begin{align*}
\min_{\dot{\gamma}, \lambda, P} & \quad \dot{\gamma}^2 \\
\text{subject to} & \quad P > 0, \lambda \geq 0, \dot{\gamma} > 0, \text{Inequality (7)}.
\end{align*}
\] (11)

Problem (11) is in linear matrix inequality (LMI) form, hence is convex and the global minimum exists. By applying an LMI solver (e.g., CVX), we obtain the gain of system (9) as a function of the sector bounds $\dot{\gamma} = g(\dot{\alpha}, \dot{\beta})$ in Fig. 6.

If there is no interference, $\dot{\alpha} = \dot{\beta} = 0$, system (9) has zero gain, and voltage does not affect the current. As $\dot{\alpha}$ decreases and $\dot{\beta}$ increases, system (9) has larger gain, as shown in Fig. 6. Interference is an example of uncertainty and $\Delta(\tilde{i}_e)$ in (9) is a sector-bounded time-varying nonlinearity.

Theorem 2: Given the class $\Sigma$ buck converter modeled by (4), the $L_2$ gain from the one-cycle-delayed inductor current sequence $[\tilde{i}_e[n]]$ to sampled output voltage sequence $[\tilde{v}[n]]$ is bounded from above by
\[
\Gamma_{v \rightarrow i} \leq \frac{T_{ss}}{L} g(\dot{\alpha}, \dot{\beta}).
\] (12)

B. Voltage Block

The voltage dynamics, which is described by the nonlinear time-invariant system (4), is a nonlinear system with quadratic and fractional nonlinearities. Existing algorithmic methods [15] can only give the $L_2$ gain for a specific $L$, $C$, and $R$ in a buck converter. In fact, no mathematical tools exist to calculate the $L_2$ gain in closed form in general.

However, we overcome this challenge by taking advantage of the specific inherent physical constraint of constant on-time buck converters of a cycle-varying off-time that is bounded by (5) to provide a closed form bound. This is valuable in giving a physical intuition to power electronics designers through the $L/R$ and $RC$ time constants of the converter.

Theorem 2: Given the class $\Sigma$ buck converter modeled by (4), the $L_2$ gain from the one-cycle-delayed inductor current sequence $[\tilde{i}_e[n]]$ to sampled output voltage sequence $[\tilde{v}[n]]$ is bounded from above by
\[
\Gamma_{i \rightarrow v} \leq \frac{R}{\left( 1 + \frac{T_{on}}{2\tau_2} \right) T_{ss}^\max},
\] (13)

where $T_{ss}^\min$ and $T_{ss}^\max$ are the shortest switching period and longest switching period, respectively, and $\tau_2$ is the $L/R$ time constant,
\[
T_{ss}^\max \triangleq T_{on} + T_{off}, \quad T_{ss}^\min \triangleq T_{on} + T_{off}^\min, \quad \tau_2 \triangleq \frac{L}{R}.
\] (14)

Proof: (i) Voltage Block Model Reformulation: The nonlinear time-invariant system (4) can be transformed to the following linear time-varying system
\[
\begin{align*}
\tilde{v}[n + 1] &= \alpha[n] \tilde{v}[n] + \beta[n] \tilde{i}_e[n] + \gamma[n] \tilde{v}^*_e[n] + \tilde{u}[n], \\
\alpha[n] &= 1 - \frac{T_{on} + T_{off}^\min[n]}{RC} \frac{T_{on} T_{off} + T_{off}^\min[n]}{2LC}.
\end{align*}
\] (15)
\[
\beta[n] = \frac{1}{C} \left(1 - \lambda T_{on} + \frac{1}{2} T_{off}[n]\right),
\]
\[
\gamma[n] = \frac{1}{C} \left(\lambda T_{on} + \frac{1}{2} T_{off}[n]\right).
\]

From (5), the time-varying coefficients are bounded by

\[
0 < \alpha[n] \leq \alpha_{\text{max}} = 1 - \frac{T_{\text{min}}}{RC} - \frac{T_{on} T_{\text{min}}}{2LC},
\]
\[
0 < \beta[n] \leq \beta_{\text{max}} = \frac{1}{C} \left(1 - \lambda T_{on} + \frac{1}{2} T_{\text{max}}\right),
\]
\[
0 < \gamma[n] \leq \gamma_{\text{max}} = \frac{1}{C} \left(\lambda T_{on} + \frac{1}{2} T_{\text{max}}\right).
\]

By definition, the
\[
L = \begin{bmatrix}
0 \\
1
\end{bmatrix}
\]

The \(L_2\) gain of the system (17b) can be obtained from the Cauchy-Schwarz Inequality as

\[
\bar{V}^2[n] = (q[n] + \gamma[n] \bar{\gamma}[n])^2 \\
\leq \left(\gamma^2[n] + \gamma[n] \bar{\gamma}[n]\right) \left(\frac{1}{\gamma_{\text{max}}^2} + \frac{\gamma[n]}{1-\gamma_{\text{max}}^2}\right) \left(\frac{1}{\beta_{\text{max}}^2} + \frac{\beta[n]}{1-\beta_{\text{max}}^2}\right).
\]

Summing both sides of the inequality for all \(n\) yields the \(L_2\) gain of the system (17b) \(\|V\|_2 \leq \Gamma_1\), where \(\Gamma_1\) is the \(L_2\) norm and

\[
\Gamma_1 = \frac{\beta_{\text{max}} + \alpha_{\text{max}} \gamma_{\text{max}}}{1-\beta_{\text{max}}^2}(1-\beta_{\text{max}}^2)^{1/2}.
\]

The \(L_2\) norm of \(q[n]\) can be bounded by

\[
\|q\|^2 \leq \Gamma_1^2 \|\bar{\gamma}\|^2 + \frac{V(1) - V(\infty)}{1-\beta_{\text{max}}^2} \leq \Gamma_1^2 \|\bar{\gamma}\|^2 + \frac{V(1)}{1-\beta_{\text{max}}^2} \leq \frac{V(1)}{1-\alpha_{\text{max}}^2}.
\]

By definition, the \(L_2\) gain of system (17a) is bounded from above by \(\Gamma_1\).
The theoretical contribution of this letter provides an analytical and practical stability criterion for designing current-mode dc-dc converters with large-signal stability guarantees. The criteria indicate that the $L/R$ and $RC$ time constants are the design parameters which determine the amount of coupling between the current control loop and voltage block. The current control loop and voltage block can be decoupled by increasing $L/R$, $RC$, or $T_{0}^{\min}$, or by decreasing $T_{0}^{\max}$.

VI. Conclusion

The results in $|\hat{\alpha}| = 0.182$; this value satisfies the stability criterion $|\hat{\alpha}| < 0.213$, showing a stable inductor current waveform on the oscilloscope shown in Fig. 7 for a step change in output voltage. The current control waveform becomes unstable in Fig. 8 because $|\hat{\alpha}| = 0.754$ no longer satisfies the stability criterion $|\hat{\alpha}| < 0.373$, both during and after the transient from an inductor current step. A higher inductance is a typical choice of power electronics engineers to reduce both inductor current ripple and output voltage ripple; however, this blind selection results in instability.

**TABLE I**

| Param. | Values | Param. | Values | Param. | Values |
|--------|--------|--------|--------|--------|--------|
| $V_{in}$ | 12 V | $L$ | 290 nH | $T_{0}$ | 200 ns |
| $V_{out}$ | 1 V | $C$ | 100 $\mu$F | $R_{s}$ | 10 m$\Omega$ |

**TABLE II**

| Case | $R$ ($\Omega$) | $L$ ($\mu$H) | $|\hat{\alpha}|$ | Criterion (26) | Stability |
|------|---------------|-------------|--------------|----------------|-----------|
| 1    | 0.21          | 290         | 0.182        | $|\hat{\alpha}| < 0.213$ | Stable    |
| 2    | 0.21          | 1200        | 0.754        | $|\hat{\alpha}| < 0.373$ | Unstable  |

**REFERENCES**

[1] X. Cui, C. Keller, and A.-T. Avestruz, “A 5 MHz high-speed saturating inductor DC-DC converter using cycle-by-cycle digital control,” in *Proc. IEEE 20th Workshop Control Model. Power Electron. (COMPEL)*, Toronto, ON, Canada, 2019, pp. 1–8.

[2] X. Cui and A.-T. Avestruz, “Switching-synchronized sampled-space state space modeling and digital controller for a constant off-time, current-mode boost converter,” in *Proc. Amer. Control Conf. (ACC)*, Philadelphia, PA, USA, 2019, pp. 1–8.

[3] L. Ding, S.-C. Wong, and C. K. Tse, “Bifurcation analysis of a current-mode-controlled DC cascaded system and applications to design,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3214–3224, Dec. 2020.

[4] X. Cui and A.-T. Avestruz, “A new framework for cycle-by-cycle digital control of megahertz-range variable frequency buck converters,” in *Proc. IEEE 19th Workshop Control Model. Power Electron. (COMPEL)*, Padua, Italy, 2018, pp. 1–8.

[5] F. C. Lee and Q. Li, “High-frequency integrated point-of-load converters: Overview,” *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

[6] V. Švěkoč, J. J. Cortés, P. Alou, J. A. Oliver, O. García, and J. A. Cobos, “Multiphase current-controlled buck converter with energy recycling output impedance correction circuit (OICC),” *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5207–5222, Sep. 2015.

[7] K.-Y. Cheng, S. Tian, F. Yu, F. C. Lee, and P. Mattavelli, “Digital hybrid ripple-based constant on-time control for voltage regulator modules,” *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3132–3144, Jun. 2014.

[8] X. Cui, C. Keller, and A.-T. Avestruz, “Cycle-by-cycle digital control of a multi-megahertz variable-frequency boost converter for automatic power control of LiDAR,” in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Baltimore, MD, USA, 2019, pp. 702–711.

[9] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. New York, NY USA: Springer, 2007.

[10] R. Roll and I. Novak, “Instabilities in current-mode controlled switching voltage regulators,” in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 1981, pp. 17–28.

[11] K. Hariharan, S. Kapat, and S. Mukhopadhyay, “Constant on/off-time hybrid modulation in digital current-mode control using event-based sampling,” *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3789–3803, Apr. 2019.

[12] S. Boyd, L. El Ghaoui, E. Feron, and V. Balakrishnan, *Linear Matrix Inequalities in System and Control Theory*. Philadelphia, PA, USA: SIAM, 1994.

[13] X. Cui and A.-T. Avestruz, “Overcoming high frequency limitations of current-mode control using a control conditioning approach—Part I: Modeling and analysis,” 2022, arXiv:2206.10518.

[14] X. Cui and A.-T. Avestruz, “Large-signal stability guarantees for cycle-by-cycle controlled DC-DC converters,” May 2022, arXiv:2205.10155.

[15] H. Mazaheri, A. Francés, R. Asensi, and J. Uceda, “Nonlinear stability analysis of DC-DC power electronic systems by means of switching equivalent models,” *IEEE Access*, vol. 9, pp. 98412–98422, 2021.

[16] Y. Okuyama, *Discrete Control Systems*. London, U.K.: Springer, Nov. 2014.

[17] H. K. Khalil, *Nonlinear Systems*. Upper Saddle River, NJ, USA: Prentice-Hall, 2002.