A Family of Current References Based on 2T Voltage References: Demonstration in 0.18-μm with 0.1-nA PTAT and 1.1-μA CWT 38-ppm/°C Designs

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Abstract—The robustness of current and voltage references to process, voltage and temperature (PVT) variations is paramount to the operation of integrated circuits in real-world conditions. However, while recent voltage references can meet most of these requirements with a handful of transistors, current references remain rather complex, requiring significant design time and silicon area. In this paper, we present a family of simple current references consisting of a two-transistor (2T) ultra-low-power voltage reference, buffered onto a voltage-to-current converter by a single transistor. Two topologies are fabricated in a 0.18-μm partially-depleted silicon-on-insulator (SOI) technology and measured over 10 dies. First, a 7T nA-range proportional-to-absolute-temperature (PTAT) reference intended for constant- gm biasing of subthreshold operational amplifiers demonstrates a 0.096-nA current with a line sensitivity (LS) of 1.48 %/V, a temperature coefficient (TC) of 0.75 %/°C, and a variability (σ/μ) of 1.66 %. Then, two 4T+1R μA-range constant-with-temperature (CWT) references with (resp. without) TC calibration exhibit a 1.09- μA current with a 0.21-%/V (resp. 0.20-%/V) LS, a 38-ppm/°C (resp. 290-ppm/°C) TC, and a 0.87-% (resp. 0.65-%) (σ/μ). In addition, portability to common scaled CMOS technologies, such as 65-nm bulk and 28-nm fully-depleted SOI, is discussed and validated through post-layout simulations.

Index Terms—Current reference, voltage reference, ultra-low-power (ULP), proportional-to-absolute-temperature (PTAT), constant- gm biasing, constant-with-temperature (CWT), temperature-independent.

I. INTRODUCTION

CURRENT and voltage references are crucial components of mixed-signal circuits, ranging from ultra-low-power (ULP) sensor nodes for the Internet of Things (IoT) [1] to high-performance circuits for compute-in-memory accelerators, such as data converters [2], [3]. Despite the widely different contexts in which these references are used, they share the common objective of ensuring robustness against PVT variations. On the one hand, recent advances in the design of voltage references have led to simple topologies [4]–[6], consisting of only a handful of transistors and consuming a few pW at ambient temperature. While these topologies demonstrate remarkably competitive supply voltage and temperature dependencies with respect to more advanced references, they generally suffer from an increased dependence on process variations and need to be trimmed. Nevertheless, their main advantage lies in the design time reduction arising from the limited number of degrees of freedom. On the other hand, current references remain more complex than their voltage counterparts, often requiring more components and an intricate sizing [7]. Nonetheless, recent works have shown that a 2T voltage reference can be used to generate a reference current once replicated onto a gate-leakage transistor by a 1T buffer [8], [9]. Such works suggest that simpler yet competitive architectures are within reach.

In this paper, we build upon [8], [9] to create a family of simple current references without startup circuit sharing two key principles: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering by a single transistor onto a voltage-to-current (V-to-I) converter. Compared with [8], [9], we substitute the gate-leakage transistor by either a self-cascode MOSFET (SCM) or a resistor, respectively resulting in a nA- and μA-range current. This leads to two novel current reference topologies, fabricated in a 0.18-μm partially-depleted silicon-on-insulator (PDSOI) process. First, a proportional-to-absolute-temperature (PTAT) current reference built by applying a PTAT voltage to an SCM, which is similar to [10], [11] but with a different PTAT voltage generation. The measured 0.096-nA current has a line sensitivity (LS) of 1.48 %/V, a temperature coefficient (TC) of 0.75 %/°C and a (σ/μ) of 1.66 %, while the current reference consumes down to 0.28 nW at 25°C. It consists of seven transistors and occupies a silicon area of 8700 μm². Second, a constant-with-temperature (CWT) current reference is obtained by the ratio of a voltage and a resistance with matching TCs. It provides a measured 0.99-μA current with an LS of 0.20-%/V, a TC of 290 ppm/°C, and a (σ/μ) of 0.65 %. It consumes down to 0.64 μW at 25°C, and is made of four transistors and a polysilicon resistor, occupying a total silicon area of 3410 μm². Another version with a 4-bit TC calibration reduces temperature dependence down to 38 ppm/°C, and provides a 1.09-μA current within a 4270-μm² silicon area.

The remainder of this paper is organized as follows. Section II presents existing MOS-based current generation techniques. Then, Section III highlights the principles shared by both proposed PTAT and CWT topologies, whose sizing is detailed in Section IV. Next, simulation and measurement results are discussed in Section V. We address additional design considerations for an implementation in scaled technologies in Section VI. Finally, Section VII compares our work to the state of the art and Section VIII offers some concluding remarks.

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II. MOS-BASED CURRENT GENERATION TECHNIQUES

In this section, we describe previous PTAT and CWT current references implemented in a CMOS or BiCMOS technology, based on the four main techniques depicted in Fig. 1.

A. PTAT Current Reference Topologies

Among current references, only the self-biased $\beta$-multiplier (Fig. 1(a)) is generally used for the generation of a PTAT current, achieved by operating transistors $M_{1-2}$ in weak inversion. Indeed, a difference of gate-to-source voltages $\Delta V_{GS}$ proportional to the thermal voltage $U_T$ is applied to the resistor. A common problem is that generating a nA-range current requires a resistance in the order of $\Omega$, which occupies a significant silicon area. [10], [12] have thus proposed to replace the resistor by a 2T SCM, as this structure has a smaller area footprint and generates a current based on the specific sheet current $I_{SO} \propto T^{2-m}$, where $T$ is the absolute temperature and $m$ is the temperature exponent of the carrier mobility. As $m$ is comprised between 1.2 and 2 in bulk CMOS [13], the current can depend quasi-linearly on temperature. Variants of this topology improve the LS through cascading [11] or a 1T feedback amplifier [14]. While the PTAT self-biased $\beta$-multiplier only requires a handful of components, the SCM sizing can be tedious because transistors are operated in moderate inversion. However, an SCM can be implemented with transistors from a single threshold voltage ($V_T$) type and reaches a low current within a small area.

B. CWT Current Reference Topologies

All four topologies depicted in Fig. 1 can be used to generate a CWT reference current. First, a self-biased $\beta$-multiplier (Fig. 1(a)) can generate a CWT current with $M_{1-2}$ operating either in weak [15]–[19] or in strong inversion [20]–[24]. The strengths of the CWT self-biased $\beta$-multiplier are rather similar to the ones emphasized for the PTAT topologies and therefore not reminded here.

Second, a CWT current can be produced by biasing a transistor close to its zero temperature coefficient (ZTC) with a slightly temperature-dependent $V_{GS}$ (Fig. 1(b)). On the one hand, a strong-inversion MOSFET is biased close to its ZTC with either a CWT [25], [26] or a slightly PTAT [27] gate voltage. On the other hand, a weak-inversion MOSFET requires a slightly complementary-to-absolute-temperature (CTAT) $V_{GS}$ buffered by an OTA [28] or a fixed gate voltage and PTAT source voltage, produced by two independent bias circuits [29]. Simpler topologies can operate in weak (resp. strong) inversion with a CTAT (resp. PTAT) gate voltage generated by a 2T ULP voltage reference [30], [31]. Overall, this current generation technique can be made process-independent with relative ease, by letting the gate voltage track process variations, and has the advantage of a pW-to-nW power consumption. However, a competitive TC can only be achieved close to the ZTC, often resulting in a large reference current. Moreover, complex voltage generators often entail a considerable area overhead.

Third, the subtraction of PTAT currents with different TCs (Fig. 1(c) left), or the weighted sum of PTAT and CTAT currents (Fig. 1(c) right), can also lead to a CWT current. The subtraction can be done (i) between a PTAT current and its purely temperature-dependent component [32] or (ii) between two different currents [33]–[35]. Besides, the weighted sum is performed with a PTAT current, implemented with bipolar transistors as the ratio of a difference of base-to-emitter voltages $\Delta V_{BE}$ and a resistance, and a CTAT current obtained by the ratio of a $\Delta V_{GS}$ [36] or a $V_{BE}$ [37], [38] and a resistance. This topology is quite simple, but suffers from several limitations: (i) a calibration of the relative weighting of the currents is necessary to achieve a competitive TC, (ii) the generation of PTAT and CTAT currents can require the use of bipolar transistors, and (iii) two current generators are needed instead of one, resulting in significant area usage.

Finally, a CWT current can be obtained as the ratio between a voltage and a resistance with matched TCs (Fig. 1(d)). A first category relies on the ratio of a CWT voltage applied either to a CWT resistance [39], [40] or to gate-leakage transistors [8], [41]. A second category uses the ratio of a temperature-dependent voltage whose TC matches the one of the resistance. It can be achieved by (i) a slightly PTAT voltage buffered by a linear regulator [42], (ii) a CTAT voltage buffered by a single transistor [9], or (iii) a voltage matching the 1st and 2nd order TCs of a polysilicon resistor [7]. This type of current reference can easily be calibrated to reach a competitive TC performance by matching the 1st order TC of the resistance, but usually relies on an operational amplifier to buffer the reference voltage onto the resistor, and can lead to rather complex voltage generator architectures if 2nd order TC matching is required. Obviously, the buffer and voltage generator can result in a considerable power and area overhead.

III. A FAMILY OF CURRENT REFERENCES

Fig. 2 presents the proposed family of current references, which share the same current generation principle. A reference
voltage $V_{\text{REF}}$ is generated by a the 2T ULP structure formed by $M_{1-2}$, and then buffered onto a V-to-I converter by transistor $M_3$. The range and temperature dependence of the reference current, denoted as $I_{\text{REF}}$, are conditioned by the type of transistors used in the voltage reference and the chosen V-to-I converter. The first current reference, in Fig. 2(a), relies on a CWT voltage reference biasing a gate-leakage transistor, which acts as a resistance in the order of $G\Omega$. This structure was proposed in [8], [9] and generates a CWT reference current in the pA range. Second, the current reference in Fig. 2(b) relies on a PTAT voltage reference biasing an SCM and generates a nA-range reference current proportional to the specific sheet current of $M_{6-7}$ [10], [11]. Third, the current reference in Fig. 2(c) relies on a quasi-CWT voltage reference biasing a resistor and compensating for its temperature dependence, and generates a temperature-independent reference current in the $\mu$A range. Fig. 2(d) summarizes the characteristics of the three references described hereabove. In the remainder of this paper, we focus on the nA- and $\mu$A-range current reference topologies, as the pA-range one has already been proposed in previous art [8], [9].

The topology brought forward in this work offers three main advantages. First, it requires a small number of transistors with a potentially dense layout, thus limiting the area footprint and reducing the design time by restraining the number of degrees of freedom. Second, the voltage reference draws a supply current in the pA-to-nA range, resulting in a low power consumption compared to a $\beta$-multiplier or bandgap voltage reference. Third, it does not require any startup circuit as the reference has a unique stable operation point corresponding to a non-zero current, leading to further area savings.

A. 2T ULP Voltage Reference

The 2T ULP voltage reference used in this work was proposed in [8], [9] in the context of current references and shares the same operation principle as [4], [5], [43]. It relies on the balance of the subthreshold currents in transistors $M_{1-2}$ to generate a reference voltage. There are three main assumptions underlying the reasoning that follows: (i) for the sake of generality, $M_{1-2}$ have distinct characteristics, (ii) both transistors operate in weak inversion, and (iii) the drain-to-source voltage $V_{DS}$ is larger than $4U_T$, where $U_T$ is the thermal voltage, so the transistors are saturated. Under these assumptions, the drain-to-source current can be expressed as

$$I_{DS} = I_{SQ} S \exp\left(\frac{V_{GS} - V_{T0}}{nU_T}\right),$$

where $I_{SQ} = \mu C_{ox} (n-1)U_T^2$ is the specific sheet current, $\mu$ is the carrier mobility, $C_{ox}$ is the normalized gate oxide capacitance, $S = W/L$ is the transistor aspect ratio, $V_{T0}$ is the threshold voltage at zero body-to-source voltage, and $n$ is the subthreshold slope factor. Applying (1) to $M_{1-2}$ and solving for the reference voltage yields

$$V_{\text{REF}} = n_1U_T \log \left(\frac{I_{SQ2} S_2}{I_{SQ1} S_1}\right) + \left(n_2 V_{T01} - n_1 V_{T02}\right).$$

For the $\mu$A-range reference, $M_1$ is chosen to have a larger threshold voltage than $M_2$, i.e., $V_{T01} > V_{T02}$, and the ratio $S_2/S_1$ can be used to tune the reference voltage’s TC, whereas for the nA-range current reference, the same transistor type is used for $M_{1-2}$ and it simplifies to a purely PTAT voltage

$$V_{\text{REF}} = nU_T \log \left(\frac{S_2}{S_1}\right),$$

assuming no mismatch between $M_{1-2}$. The LS of the reference voltage is computed from the small signal schematic in Fig. 3 where $r_{\text{out}}$ denotes the output resistance of the V-to-I converter. First, assuming that $g_{m3} \gg g_{d3}$ and $g_{m4} \gg \frac{1}{r_{\text{out}}}$, the transfer function between $v_x$ and $v_{\text{ref}}$ is given by (4). Then, if $g_{m3} \gg \frac{1}{r_{\text{out}}}$, this expression further simplifies to one, which is in line with the common-drain configuration of $M_3$.

$$v_x \approx g_{m3} + g_{d3} + \frac{1}{r_{\text{out}}} \approx 1$$

Then, the supply dependence of $V_{\text{REF}}$, i.e., $v_{\text{ref}}/v_{dd}$, is given by (5) and simplifies to $g_{d2}/g_{m1}$ for $g_{m} \gg g_{d}$.

B. nA-Range PTAT Current Reference

To generate a current proportional to the specific sheet current $I_{SQ}$, the nA-range reference relies on a moderate-inversion SCM formed by $M_{6-7}$ and biased by a PTAT voltage, as proposed in [10]. The use of moderate inversion

Fig. 2. Overview of the family of current references, generating a reference voltage $V_{\text{REF}}$ with a 2T ULP structure and converting it into a current by single-transistor buffering onto (a) a gate-leakage transistor [8], [9], (b) an SCM, and (c) a resistor, generating a pA-, nA- and $\mu$A-range current, respectively. Finally, (d) summarizes the TC of $V_{\text{REF}}$, as well as the TC and range of $I_{\text{REF}}$ across the different architectures.
requires the advanced compact model (ACM) \cite{44} to describe the transistor I-V relationship. The drain current \( I_D \) is given by

\[ I_D = I_{SQ} S (i_f - i_r), \]

where \( I_{SQ} = \frac{1}{2} \mu C_{ox} n U_D^2 \) is the ACM specific sheet current, \( S \) is the transistor aspect ratio, and \( i_f, i_r \) the forward and reverse inversion levels. The reverse inversion level is non-zero only when the transistor is in triode. Furthermore, the forward inversion level is linked to the gate and source voltages by

\[ V_D - V_S = U_T \left[ \sqrt{1 + i_f} - 2 + \log \left( \sqrt{1 + i_f} - 1 \right) \right], \]

where \( V_P = \frac{V_D - V_S}{n} \) is the pinch-off voltage. A similar relationship is obtained for the reverse inversion level if \( V_S \) is replaced by \( V_D \) and \( i_f \) by \( i_r \) in (7). The ACM equations applied to \( M_{6-7} \), respectively in moderate-inversion triode and saturation, give \( i_{f6} = i_{f7} \) \cite{10}. Then, defining \( \alpha \triangleq \frac{i_{f6}}{i_{f7}} \), \( i_{f7} \) is determined by solving the non-linear equation

\[ V_{REF} = U_T \left[ \sqrt{1 + \alpha i_f} - 1 \right], \]

Finally, the aspect ratios of \( M_{6-7} \) must comply with

\[ \frac{S_6}{S_7} = \frac{I_{SQ} S_6}{I_{SQ} S_7} = \frac{N+1}{N} \frac{1}{\alpha - 1}. \]

Moreover, the line sensitivity and mismatch of the reference current are directly related to the characteristics of the voltage reference, through the sensitivity \( S_{I_{REF}} \). It is computed by means of the chain rule as

\[ S_{I_{REF}} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{REF}} = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial i_f} \frac{\partial i_f}{\partial V_{REF}}, \]

where the variation of \( i_f \) with respect to \( V_{REF} \) is derived from (8) and the sensitivity is thus expressed as

\[ S_{I_{REF}} = \frac{2}{i_f U_T} \left[ \frac{1}{\sqrt{1 + \alpha i_f} - 1} - \frac{1}{\sqrt{1 + i_f} - 1} \right]^{-1}. \]

The line sensitivity and mismatch of the reference current can thus be expressed as

\[ \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{DD}} = S_{I_{REF}} g_{m2}/g_{m3}, \]

\[ \left( \frac{\sigma}{\mu} \right)_{I_{REF}} = S_{I_{REF}} \sigma_{V_{REF}}, \]

and depend on both the characteristics of the voltage reference and the sizing of the SCM.

C. \( \mu \)A-Range CWT Current Reference

To generate a temperature-independent reference current, the \( \mu \)A-range current reference relies on a resistor biased by a CWT reference voltage. The reference current is thus given by \( I_{REF} = \frac{V_{REF}}{R} \). Assuming that the threshold voltage of transistor \( M_t \), denoted as \( V_{T0_t} \), decreases linearly with temperature \( T \) following \( V_{T0_t}(T) = V_{T0_t}(T_0) - \alpha_{V_{T0_t}} (T - T_0) \), and that the resistance temperature variation is captured by \( \frac{\partial R}{\partial T} \), the temperature variation of \( I_{REF} \) is given by

\[ \frac{\partial I_{REF}}{\partial T} = \frac{1}{R} \left( \frac{nk}{q} \log \frac{I_{SQ} S_2}{I_{SQ} S_1} + (\alpha_{V_{T01}} - \alpha_{V_{T02}}) \right) \frac{\partial V_{REF}}{\partial T} \]

and

\[ \frac{\partial I_{REF}}{\partial V_{REF}} = \frac{1}{R} \left( \frac{nk}{q} \log \frac{I_{SQ} S_2}{I_{SQ} S_1} + (V_{T01} - V_{T02}) \right) \frac{\partial R}{\partial T}. \]

Therefore, the ratio \( S_2/S_1 \) leading to zero temperature variation of the reference current at \( T = T_0 \) is

\[ I_{SQ} \exp \left( \frac{q}{nk} (V_{T01} - V_{T02}) \frac{\partial R}{\partial T} + (\alpha_{V_{T01}} - \alpha_{V_{T02}}) \right)^{\frac{1}{1 - \frac{\partial R}{\partial T}}}. \]

Similarly to the PTAT current reference, the line sensitivity and mismatch are expressed by (12) and (13), where \( S_{I_{REF}} \) is expressed as. Interestingly, these quantities only depend on the characteristics of the voltage reference.

IV. CIRCUIT DESIGN AND SIZING METHODOLOGY

In this section, we explain the design choices and detail the steps of the sizing methodology used to implement the proposed references in the XFAB 0.18-\( \mu \)m PDSOI technology.

A. \( n \)A-Range PTAT Current Reference

The sizing of the PTAT current reference illustrated in Fig. 2(b) has a twofold objective: minimizing the LS and variability of \( I_{REF} \), while achieving the reference current target in nominal conditions (TT process, 25°C). Four main parameters can be tuned to achieve this objective:

1) \( S_2/S_1 \), the ratio of \( M_{1-2} \) aspect ratios, which amounts to \( W_2/W_1 \) if these transistors have the same length;
2) \( m \), the multiplier or number of parallel devices used to implement both \( M_1 \) and \( M_2 \);
3) \( \alpha = i_{f6}/i_{f7} \), the ratio of \( M_6 \) and \( M_7 \) inversion levels;
4) \( N \), the multiplicative factor in the current mirror formed by \( M_4 \) and \( M_5 \).

The first two degrees of freedom are linked to the 2T voltage reference, while the later ones are related to the SCM. We will first explain the sizing of the V-to-I converter, i.e., the SCM, and will then turn to the 2T voltage reference. Besides, low-\( V_T \) (LVT) devices are selected to implement the proposed reference, as they lead to a lower minimum supply voltage than regular-\( V_T \) (RVT) devices and ensure the proper
TABLE I
PROPERTY OF MAXIMUM-LENGTH 25-µM TRANSISTORS IN THE XFAB 0.18-µM PDSOI TECHNOLOGY, AT 25°C. \( I_{SQ} \) IS DETERMINED IN THE SENSE OF THE ACM MODEL.

| Transistor type | \( n \) | \( I_{SQ} \) [nA] | \( V_T0 \) [V] |
|-----------------|--------|-----------------|----------------|
| LVT nMOS        | 1.21   | 99.63           | 0.433          |
| LVT pMOS        | 1.14   | 23.98           | -0.383         |
| RVT nMOS        | 1.29   | 67.10           | 0.668          |
| RVT pMOS        | 1.41   | 29.26           | -0.749         |

Fig. 4. (a) \( S_{IREF} \) is dependent on two key design parameters, namely \( S_2/S_1 \), related to the 2T ULP voltage reference, and \( \alpha = i_{f6}/i_{f7} \), related to the SCM. The red star indicates the chosen design point. (b) Inversion level \( i_{f7} \) and sensitivity \( S_{IREF} \), for different values of \( \alpha \) and (c) reference voltage \( V_{REF} \), normalized by the thermal voltage \( U_T \), as a function of \( S_2/S_1 \).

operation of the 2T voltage reference at low temperature, as will be discussed in Section VI-A. Then, we choose to invert the topology shown in Fig. 2(b), i.e., nMOS and pMOS devices are swapped, as well as ground and supply connections. This change makes it easier to reach a low reference current and avoids using several well voltages, requiring deep trench isolation (DTI) in PDSOI or triple-well devices in bulk. Finally, the sizing of the SCM and its current mirror is similar to [10], [11], and performed at 25°C. It consists of the following steps:

1) Compute \( V_{REF} \) using (3).
2) Determine the inversion level of \( M_7 \) by solving (8) for \( i_{f7} \). By definition, the inversion level of \( M_6 \) is computed as \( i_{f6} = \alpha i_{f7} \), and the sensitivity \( S_{IREF} \) is calculated using (11).
3) Compute the aspect ratio and width of transistors \( M_6 \) and \( M_7 \), forming the SCM. \( S_7 \) is computed as

\[
S_7 = \frac{N I_{REF}}{T_{SQ7} i_{f7}}
\]

based on (6), while \( S_6 \) is calculated from (7).
4) Compute the aspect ratio and width of \( M_{3-5} \) using (6).

This methodology is implemented in Matlab, and the transistor properties, summarized in Table I, are computed from DC Spice simulations following [45]. Contrary to [10], [11], we do not limit ourselves to the methodology detailed hereabove, but we provide guidelines on how to select the main design parameters required by this methodology, namely \( S_2/S_1 \), \( \alpha \) and \( N \). Steps 1) and 2) are mostly technology-agnostic, as only the subthreshold slope factor \( n \) is required at this stage. Indeed, the two other parameters coming into play are \( S_2/S_1 \) and \( \alpha \), which do not depend on the technology choice. Fig. 4(a) depicts sensitivity \( S_{IREF} \) as a function of these two parameters, and allows to select a couple \( (S_2/S_1; \alpha) \) meeting the target value for \( S_{IREF} \), here arbitrarily set to 5 %/mV. The chosen design point \( (S_2/S_1 = 8; \alpha = 3) \) is marked by a red star in Fig. 4(a) and yields a sensitivity of 4.72 %/mV. Furthermore, the trends observed in Fig. 4(a) are better understood by looking at Figs. 4(b) and (c). Increasing \( S_2/S_1 \) pushes \( M_{6-7} \) into moderate inversion, as evidenced by the increase of \( i_{f7} \) (Fig. 4(b)), due to the higher reference voltage \( V_{REF} \) applied to the SCM (Fig. 4(c)). It should be noted that, for a fixed \( \alpha \), the sensitivity approximately improves as \( 1/i_{f7} \), as indicated by the first term in (11). Then, decreasing \( \alpha \) provides a second tuning knob for improving \( S_{IREF} \), by pushing \( M_7 \) even further into moderate inversion (Fig. 4(b)). Next, the results of step 3) are technology-dependent, because they rely on (i) the specific sheet current (Table I) and (ii) the \( I_{REF} \) target, here set to 0.1 nA. Fig. 5(a) represents the aspect ratio of \( M_{6-7} \) as a function of \( \alpha \), for different values of \( N \) and for a fixed voltage reference corresponding to \( S_2/S_1 = 8 \). Similarly to Fig. 4(b), decreasing \( \alpha \) pushes \( M_{6-7} \) into moderate inversion, thus decreasing their aspect ratio at constant current. Besides, higher values of the multiplicative factor \( N \) increase \( S_{6-7} \), as expected from (9) and (16), facilitating the implementation of these transistors at the cost of a higher power consumption. Here, we select \( N = 2 \), which gives \( S_6 = 1.12 \times 10^{-3} \) and \( S_7 = 1.49 \times 10^{-3} \). The very low values obtained for these aspect ratios cannot be achieved with a single device, but will be implemented as a composite transistor, i.e., the series

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This text describes a methodology for designing transistors in a 25-µm PDSOI technology, focusing on selecting design parameters and implementing the design in Matlab. It includes tables with transistor properties and figures illustrating the behavior of the designed circuits.

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**TABLE II**

**SIZING OF THE NA-RANGE PTAT CURRENT REFERENCE IN XFAB 0.18-µM PDSOI.**

| Type | Sizing algorithm output | Final implementation |
|------|-------------------------|----------------------|
| \( M_1 \) | LVT pMOS | 4x1 | 20 | - | 4x1 | 20 |
| \( M_2 \) | LVT pMOS | 32x1 | 20 | 32x1 | 20 |
| \( M_3 \) | LVT pMOS | 0.34 | 10 | 0.12 | 35 | 10 |
| \( M_4 \) | LVT nMOS | 1.03 | 2x25 | 0.05 | 2x0.5 | 2x25 |
| \( M_5 \) | LVT nMOS | 2.06 | 2x25 | 0.05 | 4x0.5 | 2x25 |
| \( M_6 \) | LVT nMOS | 0.56 | 20x25 | 16.83 | \( \text{0.64} \) | 20x25 |
| \( M_7 \) | LVT pMOS | 0.74 | 20x25 | 5.61 | \( \text{0.86} \) | 20x25 |
connection of several devices. Step 4) is straightforward as it is a direct consequence of previous choices.

Finally, let us consider the sizing of the 2T voltage reference. As mentioned earlier, LVT pMOS devices are selected to ensure a proper operation in all process corners down to -40°C, as will be explained in Section VI-A. In addition, a length of 20 µm is chosen to reduce the output conductance of $M_2$ and improve the LS, as captured by (12). $M_{1-2}$ are then sized based on Fig. 5(b), illustrating the trade-off between the standard deviation of the reference voltage due to local mismatch, denoted as $\sigma_{V_{REF}}$, and its power in nominal conditions. First, $S_2/S_1$ marginally impacts mismatch, as it is dominated by the threshold voltage variations of the smallest device, here $M_1$, whose sizes do not change with $S_2/S_1$. Consequently, increasing $S_2/S_1$ only results in a linear increase of the power consumption, shifting the curve to the right of Fig. 5(b). Second, the multiplier $m$ improves mismatch as $1/\sqrt{m}$, following Pelgrum’s law, while increasing power as $m$. A multiplier $m = 4$ is selected, in addition to the previously chosen $S_2/S_1 = 8$, and gives a power of 6.26 pW and a standard deviation of 0.42 mV.

The transistor sizes output by the sizing algorithm are summarized in Table III. Two main changes are applied for the final implementation: (i) $M_{3-5}$ are split into parallel devices to enable a common centroid layout, and (ii) $M_{6-7}$ are widened based on simulation results to match the 0.1-nA $I_{REF}$ target in nominal conditions. It should be noted that $\alpha$, and therefore $S_6/S_7$, must remain constant during this upscaling, to preserve the reference behavior.

### B. µA-Range CWT Current Reference

The sizing of the CWT current reference shown in Fig. 2(c) focuses on minimizing the TC of $I_{REF}$ while achieving the current reference target, here set to 1 µA. The sizing methodology boils down to three steps:

1. Select a resistor with a low temperature coefficient of resistance (TCR);
2. Size transistors $M_{1-2}$ to minimize the TC of $I_{REF}$;
3. Tune $R$ to reach the current reference target in TT.

Note that, similarly to the PTAT current reference, we choose to invert the topology depicted in Fig. 2(c). First, at step 1, selecting a resistor with a low TCR is desirable to avoid the 2T voltage reference from compensating large and highly nonlinear resistance variations, which would lead to a poor TC of $I_{REF}$. Table IV summarizes the properties of the available resistors, namely their density and their TCR, computed as:

$$\text{TCR} = \frac{(R_{\text{max}} - R_{\text{min}})}{R(25^\circ\text{C})} \frac{T_{\text{max}} - T_{\text{min}}}{T_{\text{avg}}}.$$  \hspace{1cm} (17)

P+ poly resistors, i.e. poly over a p-type-doped substrate, present the lowest TCR values, with 102 and 802 ppm/°C for the regular and high resistance flavors, respectively. A regular P+ poly resistor (ppp1) is selected for its low TCR, despite its modest density of 295 Ω/μm. Next, the objective of step 2) is to size $M_{1-2}$ to minimize the TC of $I_{REF}$. For the 2T voltage reference to operate properly, Fig. 6 highlights the need for $M_1$ to have a larger threshold voltage than $M_2$, which is why an RVT and LVT pMOS are chosen. The length of both transistors being fixed to 5 µm to reach a competitive LS, Fig. 7 demonstrates that the TC of $I_{REF}$ is minimized by a $W_2/W_1$ ratio of 0.56, as suggested by (15). Widths of 2.25

### TABLE III

| Resistor type | Density [Ω/μm] | Average TCR [ppm/°C] |
|---------------|----------------|-----------------------|
| N+ diff.      | 65             | 1388                  |
| P+ diff.      | 80             | 4037                  |
| N+ poly.      | 339            | 1303                  |
| N+ poly. (high res.) | 6564 | 3562                  |
| P+ poly.      | 295            | 102                   |
| P+ poly. (high res.) | 1058 | 802                   |
| Nwell         | 1165           | 3307                  |

Fig. 6. Current reference TC in the -40-to-125°C range, as a function of transistor widths $W_1$ and $W_2$. The red star indicates the chosen design point. TC is computed as explained in Section V.

### TABLE IV

| Type          | w/o TC calib. | w/ TC calib. |
|---------------|---------------|--------------|
|               | $W$ [µm]     | $L$ [µm]     | $W$ [µm]     | $L$ [µm]     |
| $M_1$         | RVT pMOS     | 4 × 2.25     | 5            | 12 × 0.8     | 5            |
| $M_{1V}$      | RVT pMOS     | /            | /            | 1 - 8 × 0.8  | 5            |
| $M_{SW}$      | RVT pMOS     | /            | /            | 0.22         | 5            |
| $M_2$         | LVT pMOS     | 4 × 1.25     | 5            | 4 × 2        | 5            |
| $M_3$         | LVT pMOS     | 10 × 10      | 1            | 10 × 10      | 1            |
| $M_4$         | LVT nMOS     | 10 × 10      | 1            | 10 × 10      | 1            |
| $R$           | P+ poly.     | 0.45         | 26 × 13.1    | 0.45         | 26 × 11.9    |

Fig. 7. A 4-bit TC calibration scheme is implemented by changing the width of $M_1$ and thus the ratio $W_2/W_1$. |
and 1.25 \, \mu m are selected for \( M_1 \) and \( M_2 \), on the grounds of variability, giving a TC of 18 \, ppm/\degree C. Finally, step 3 simply consists in tuning the value of the resistance to reach the 1- \, \mu A target. Transistors \( M_{3-4} \) can be easily sized, with the main limitations being that in all PVT corners, \( M_1 \) must ensure that \( M_1 \) remains saturated, and \( V_{GS4} \) must be larger than \( 4U_T \) for the current mirror to operate properly.

Nevertheless, the ratio \( W_2/W_1 \) leading to the minimum TC is process-dependent. A calibration mechanism, represented in Fig. 7, is consequently implemented by tuning the width of \( M_1 \) with a 4-bit control signal. This allows to change \( W_2/W_1 \) from 0.37 to 0.83, leading to a TC for \( I_{REF} \) in the 10-to-30-ppm/\degree C range in most process corners, as will be shown in Section V-B. To conclude, the chosen transistor sizes for the CWT current reference without and with calibration are summed up in Table IV.

V. Simulation and Measurement Results

This section presents the simulation and measurement results for the three current references fabricated in XFAB 0.18- \, \mu m PDSOI. Their layouts are shown in Fig. 8 together with the chip microphotograph. Simulations are performed post-layout, to account for non-idealties due to layout effects and parasitic diodes. Current measurements are carried out with a Keithley 2636A source meter, connected to the PCB including the chip through triaxial cables. The PCB is placed in an Espec SH-261 climatic chamber, in which temperature is swept from -40 to 85 \, \degree C by steps of 5 \, \degree C while leaving humidity uncontrolled. Temperature is limited to 85 \, \degree C as some pieces of equipment cannot withstand higher temperatures.

In what follows, the LS and TC are computed using the box method, i.e.,

\[
LS = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}(V_{DD,max} - V_{DD,min})} \times 100 \, \%/V,
\]

\[
TC = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}(T_{max} - T_{min})} \times 10^6 \, \text{ppm}/\degree C,
\]

A. nA-Range PTAT Current Reference

Post-layout simulation results are represented in Figs. 9 and 10. First, as discussed in Section III-A, the LS can be predicted by (12). With \( S_{I_{REF}} = 4.72 \, \%/\text{mV} \) given by the design point and the LS of \( V_{REF} \) equal to 0.37 \, mV, as shown in Fig. 9(b), (12) predicts an LS of 1.75 \%/V. Figs. 9(a) and (b) display that \( V_{DD,min} \) is around 0.55 \, V and is limited by the minimum voltage required to bias the 2T voltage reference. The LS is 2.21 \%/V from 0.55 to 1.8 \, V in TT, which is larger than the 1.75-\%/V prediction as it does not account for the supply voltage dependence coming from the current mirror biasing the SCM. In addition, LS is relatively stable among process corners and is mainly impacted by process variations of \( I_{REF} \), i.e., +14.5 \, \% in FF and -11.6 \, \% in SS. Thus, the worst-case LS is 2.93 \%/V in FS. Next, the variability of \( I_{REF} \) can be linked to \( \sigma_{V_{REF}} = 0.42 \, \text{mV} \) through (13), giving a prediction of 1.98 \%. Again, this value is lower than the simulation result of 2.78 \% exhibited in Figs. 9(c) and (d), as the local mismatch in the SCM and the current mirror has not been accounted for. Finally, Figs. 10(a) and (b) depict the temperature dependence of the PTAT current reference.
Fig. 11. Measured average (a) $I_{\text{REF}}$ and (c) power consumption vs. $V_{\text{DD}}$ at 25°C, with (b)-(d) details of the 10 dies, for the nA-range current reference. Histograms of (e) $I_{\text{REF}}$ and (f) LS across the 10 dies.

Fig. 12. Measured temperature dependence of (a) $I_{\text{REF}}$ and (d) power consumption at 0.9 V, for all 10 dies. (b) Power breakdown between the SCM and the 2T voltage reference. (d) Histogram of TC across the 10 dies.

Fig. 13. Simulated µA-range CWT current reference (a) $I_{\text{REF}}$ and (b) $V_{\text{REF}}$, as a function of supply voltage, in all process corners and at 25°C.

Fig. 14. Simulated temperature dependence of $I_{\text{REF}}$ (a) without and (b) with TC calibration, in all process corners and at 1.2 V.

Regarding power consumption (Fig. 11(c)), the measured value is larger than the simulated one by roughly 2× due to additional leakage in the 2T voltage reference, but a minimum power of 0.28 nW is reached at 0.55 V. Moreover, details of the 10 measured dies are provided in Figs. 11(b) and (d). Then, the variability of $I_{\text{REF}}$ across the 10 dies is depicted in Fig. 11(e), with an average and (σ/µ) equal to 0.096 nA and 1.66%, compared to 0.101 nA and 2.78% in simulation. Given that in Fig. 11(f), the average LS (1.48%/V) is also lower than in simulation (2.21%/V), we hypothesize that both observations are explained by a lower-than-expected sensitivity $S_{I_{\text{REF}}}$. Finally, Fig. 12(a) illustrates the temperature dependence of $I_{\text{REF}}$ for all 10 dies, which closely matches the post-layout simulations. The measured average TC is 0.75%/°C in TT from -40 to 85°C (Fig. 12(c)), with a standard deviation of 0.30%/°C. Regarding power consumption, Fig. 12(b) suggests that the increase from simulation to measurement comes from a temperature-independent leakage current in the 2T voltage reference. Furthermore, we observe in Fig. 12(d) that the 2T voltage reference power becomes dominant above 60°C, and leads to a larger growth than in TT simulations.

B. µA-Range CWT Current Reference

Post-layout simulation results are shown in Figs. 13 to 15. First, Figs. 13(a) and (b) depict $I_{\text{REF}}$ and $V_{\text{REF}}$ as a function of $V_{\text{DD}}$. Similarly to the PTAT reference, they highlight that $V_{\text{DD,min}}$ is limited by the 2T voltage reference and is equal to 0.65 V. From Fig. 12, we know that LS is inversely proportional to the intrinsic gain $g_m/g_d$. Given the large $g_m/g_d$ in this technology, an LS of 0.53%/V is reached in TT from 0.65 to 1.8 V, with the worst-case LS corresponding to 0.65%/V in FS. Besides, $I_{\text{REF}}$ is strongly impacted by process variations, with +33.3% in FF and -25.6% in SS. Furthermore, the temperature dependence of $I_{\text{REF}}$ is represented in Fig. 14 without...
and in measurement. I \( \mu = 0.99 \mu A \) calibration codes on a single die, for the \( \pm 1 \sigma \) for \( 10^4 \) Monte-Carlo runs in TT and at 1.2 V.

Fig. 15. Simulated temperature dependence of (a) \( I_{REF} \) and (b) \( V_{REF} \) with \( \pm 1 \sigma \) for \( 10^4 \) Monte-Carlo runs in TT and at 1.2 V.

Fig. 16. Measured (a) temperature dependence of \( I_{REF} \) at 0.9 V, for all 16 calibration codes on a single die, for the \( \mu A \)-range current reference. (b) \( I_{REF} \) TC obtained for each calibration code, in TT post-layout simulations and in measurement.

Fig. 17. Measured (a) average \( I_{REF} \) vs. \( V_{DD} \), and details of the 10 dies (c) without and (e) with TC calibration, at 25°C. Histograms of (b) \( I_{REF} \) and LS (d) without and (f) with TC calibration, across the 10 dies.

and with TC calibration. Fig. 14(a) illustrates that without TC calibration, an excellent TC of 18 ppm/°C is obtained in TT, but it degrades in skewed corners with 229 ppm/°C PTAT in SF and 212 ppm/°C CTAT in FS, due to a change of temperature dependence of \( V_{REF} \). Nevertheless, Fig. 14(b) demonstrates that a simple 4-bit calibration of the \( W_2/W_1 \) width ratio (Fig. 7) can reduce the TC below 30 ppm/°C in all process corners except for SF, in which the 119 ppm/°C PTAT TC would require a slightly larger tuning range. Lastly, in Fig. 15(a), \( I_{REF} \) presents a 2nd order temperature dependence below 100°C, and leakage leads to a current increase above this limit. Moreover, the \( (\sigma/\mu) \)'s of \( I_{REF} \) and \( V_{REF} \) are equal, as stated by (13), and amount to 0.41 % (Figs. 15(a) and (b)), featuring a perfect match between theory and simulations. Regarding \( I_{REF} \), its average value is 1 \( \mu A \) at 25°C, and its average TC reaches 14.9 ppm/°C, with a variability of 2.14 %.

Measurement results are summarized in Figs. 16 to 18. As the TC of \( I_{REF} \) is mostly impacted by process variations rather than local mismatch, we select the optimal code by sweeping the 16 calibration codes on a single die, as shown in Fig. 16(a).

Because we are using a voltage reference with pMOS devices for \( M_{1-2} \) and the control switches, increasing the calibration code decreases the actual \( W_1 \), thus reducing the PTAT part of \( V_{REF} \) and boosting the CTAT behavior of \( I_{REF} \). Based on Fig. 16(b), we select a code of 0x0001 with a 36.4-ppm/°C TC, which is different from the simulated one, here 0x0110 with a 19.2-ppm/°C TC, likely due to process variations. Next, Fig. 17(a) shows the average \( I_{REF} \) behavior with supply voltage, with a \( V_{DD,min} \) at 0.65 V and a slight increase of \( I_{REF} \) from 0.99 to 1.09 \( \mu A \) due to TC calibration (Fig. 18(b)). In both cases, the average LS is around 0.20 %/V, which represents a 2.7× reduction compared to simulations and could result from a larger \( g_m/g_d \). Variability reaches 0.65 % and 0.87 % without and with TC calibration (Fig. 17(b)). The larger value compared to 0.41 % in simulation likely comes from the yellow and red curves on the bottom of Figs. 17(c) and (e), which appear to be outliers leading to an overestimation of \( (\sigma/\mu) \). To conclude, the temperature dependence of \( I_{REF} \) is represented in Figs. 18(a) and (b). On one side, without calibration, \( I_{REF} \) presents a CTAT behavior leading to a TC of 290 ppm/°C in the -40-to-85°C range. On the other side, with calibration, the TC reduces down to 38 ppm/°C, corresponding to a 7.6× improvement. In Figs. 18(b) and (d), we observe a 2nd order temperature dependence below 70°C, as predicted by simulations. A small current surge above this limit comes from the power consumption of the 2T voltage reference, which is measured together with the reference current, but is not taken into account in the TC.
VI. IMPLEMENTATION IN SCALED TECHNOLOGIES

Novel current references are often developed in the 0.18-\(\mu\)m technology node or above. However, their portability to common scaled technologies such as 65-nm bulk, 28-nm fully-depleted SOI (FDSOI), or 14-nm FinFET, is hardly discussed and poses a series of challenges. This section details these challenges and how they can be overcome for the proposed family of current references by focusing on the implementation of the 2T voltage reference.

A. Leakage-Induced Non-Idealities

A PTAT voltage reference, implemented with pMOS devices in 65-nm bulk, is used to highlight the non-idealities of the 2T voltage reference. In Fig. 19(a), we note an increase in the reference voltage below 0°C in the slow pMOS process corners (SS and FS). A similar yet weaker behavior can be observed below -20°C in TT. Fig. 19(b) depicts the transconductance efficiency \(g_m/I_D\) and the ratio between gate and drain currents \(I_G/I_D\), for a zero-\(V_{GS}\) pMOS in SS, as a function of temperature. The non-ideal behavior noticed in Fig. 19(a) coincides with a drop in \(g_m/I_D\), which should increase at low temperature as the transconductance efficiency in deep subthreshold is proportional to \((g_m/I_D)_{max} = 1/(nU_T)\). As gate leakage has increased by several orders of magnitude from 0.18-\(\mu\)m to 65-nm [47], [48], this drop can be explained by an increased \(I_G/I_D\) ratio, coming from the fact that the current flowing in the 2T voltage reference is a drain-to-source leakage, decreasing exponentially with a temperature reduction, while the gate leakage remains approximately constant with temperature. \(I_G\) thus becomes non-negligible, reaching 6.5 \% of \(I_D\) at 0°C in SS. Two tuning knobs can be used to mitigate this non-ideal behavior: the transistor type and sizes. First, Fig. 20(a) illustrates the impact of the transistor type using the same kind of curves as Fig. 19(b). It points out that increasing the threshold voltage from LVT to high-VT (HVT) degrades the voltage reference behavior by shifting the point at which \(g_m/I_D\) drops, corresponding to an \(I_G/I_D\) around 1 to 5 \%, to higher temperature. LVT devices are thus selected to implement the voltage reference. Second, Fig. 20(b) depicts the evolution with the transistor sizes of the ratio between \(g_m/I_D\) at zero \(V_{GS}\) and \((g_m/I_D)_{max}\). A length increase degrades this ratio, as it linearly increases \(I_G\) by expanding the gate area, while simultaneously decreasing \(I_D\) as 1/L. A width increase has a limited impact, because at first order, \(I_G\) and \(I_D\) both increase linearly with it. Nevertheless, Fig. 20(b) shows that 2\(^{nd}\) order effects also come into play. Based on this figure, we select a design point with a \(g_m/I_D\) at zero \(V_{GS}\) equal to 91.2 \% of \((g_m/I_D)_{max}\), corresponding to \(W = 0.3 \mu m\) and \(L = 6 \mu m\).

Moreover, we argue that the \(g_m/I_D\) drop is a useful technology indicator for design as it captures various leakage sources degrading the voltage reference behavior. Indeed, in 65-nm bulk, the drop can be explained by the impact of gate leakage. Yet, in 0.18-\(\mu\)m PDSON and 28-nm FDSOI, gate-induced drain leakage (GIDL) prevails, as the gate leakage is limited by the use of thick oxide and high-\(\kappa\) gates, respectively.

![Fig. 19. Temperature dependence of (a) a PTAT voltage reference implemented with pMOS devices in 65-nm bulk and (b) the \(g_m/I_D\) and \(I_G/I_D\) of a zero-\(V_{GS}\) pMOS transistor in the SS process corner with \(V_{DS} = 1.2\) V.]

![Fig. 20. For a 65-nm zero-\(V_{GS}\) pMOS in SS, (a) impact of the transistor flavor on the \(g_m/I_D\) and \(I_G/I_D\) curves vs. temperature, and (b) fraction of \((g_m/I_D)_{max}\) obtained at 0°C, depending on the transistor sizes.]

Monitoring the \(g_m/I_D\) drop allows to capture any such effects, regardless of their origin.

B. Line Sensitivity Enhancement Techniques

As stated in [5], the LS of the reference voltage is inversely proportional to the intrinsic gain, which is getting worse with each technology node as a result of increased output conductance [46]. In addition, the problem posed by gate leakage and GIDL at low temperature does not allow to select a maximum-length transistor, which would have lead to a large \(g_m/g_d\) and thus a lower LS. While this issue is not critical in 28-nm FDSOI, as the intrinsic gain is larger than in bulk technologies [49], it significantly degrades the LS in 65-nm bulk. Therefore, several LS enhancement techniques are proposed in Fig. 21 (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking. These techniques are illustrated for nMOS topologies, albeit subsequent simulation results correspond to pMOS implementations. Fig. 23 compares the various LS enhancement techniques to the basic solution, using a single transistor for \(M_2\) and reaching an LS of 8.5 mV/V. First, employing a stack of \(N\) devices with their body tied to their source (Figs. 21(a) and 22(a)), the LS is expressed as

\[
\frac{v_{ref}}{v_{dd}} = \frac{g_{d21}}{g_m1 + g_d1 + \frac{g_{d21}}{N}} \approx \frac{g_{d21}}{g_m1} \frac{1}{N},
\]

under the assumptions that \(g_m1 \gg g_d1, g_{d21}\) and \(v_x = v_{ref}\). The LS decrease does not exactly scale as 1/\(N\), because the small signal parameters are impacted by the change of operation point due to stacking. Nevertheless, Fig. 23 shows an improved LS of 6.9 and 5.9 mV/V for a stacking of \(N = 2\) and 3 devices. Second, the LS using SBB stacking (Figs. 21(b) and 22(b)), i.e., all bodies tied to \(V_X\), or hybrid stacking...
and (c) hybrid stacking.

Fig. 21. Line sensitivity enhancement techniques, illustrated here for nMOS topologies, using (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking.

First, our PTAT design reaches the lowest current and power among nA-range references (Table VI), as depicted in Fig. 23(c), and is only outperformed by references using gate-leakage transistors. For the 0.18-µm reference, this corresponds to a 4.3 x current and 7.1 x power reduction compared to [10], respectively, enabled by a cut of $V_{DD,min}$ from 1.1 to 0.55 V. $I_{REF}$ is slightly larger for the 65- and 28-nm references (0.2/0.22 nA), with a power consumption of 0.8/0.88 nW due to the larger $I_{REF}$ and $V_{DD,min}$. Moreover, our 0.18-µm reference has the lowest $V_{DD,min}$ (0.55 V) among references in the nA range, followed by [11], [40] and our 65- and 28-nm designs in the 0.65-to-0.75-V range. Regarding LS, our 0.18-µm and 28-nm designs reach competitive values of 1.48 %/V and 0.78 %/V allowed by a large intrinsic gain in these technologies, while the 65-nm one exhibits a 4.43 %/V LS. Nonetheless, LS is significantly reduced from above 15 %/V down to 4.43 %/V as a result of using an hybrid stack of three devices (Section VI-B). Then, the proposed topology is strikingly simple compared to other works, with only seven to nine transistors: two to four for the voltage reference and five for the SCM. Furthermore, it can be implemented with a single transistor type, and does not require any BJTs, startup circuit or trimming, thus resulting in a low silicon area ranging from 8700 µm² in 0.18-µm down to 2900 µm² in 28-nm (Fig. 24(a)). Only [27] and [21] use simpler structures, but either occupy a 1.9 x larger or unreported area. Speaking of area, [51] is the closest competitor, but it suffers from a prohibitive power of 28.5 µW for a reference current of 25 nA. As far as temperature range is concerned, the lower limit in 65- and 28-nm designs is due to gate leakage and GIDL, respectively, while the upper limit of 85°C shared by all designs originates from the leakage in parasitic nwell/psubstrate diodes at high temperature. The temperature dependence of all three proposed references follows the specific sheet current, meaning that TC is not a relevant comparison criterion, but also that the main drawback of the proposed topology is that it suffers from process variations, although additional $I_{REF}$ calibration is possible. Regarding the variability due to local mismatch, it is limited to 1.66 % in the 0.18-µm reference, which is among the lowest values reported in Table VI while 65- and 28-nm references exhibit a larger variability due to a larger standard deviation of $V_{REF}$.

Second, our CWT current references (Table VI) also present a simple structure, consisting of a single resistor and four

Fig. 23. Comparison of the various LS enhancement techniques for a PTAT voltage reference implemented with 6-µm-length LVT pMOS devices in 65-nm bulk. The LS is measured from 0.6 to 1.2 V at 25°C.

VII. COMPARISON TO THE STATE OF THE ART

This section compares our work to the state of the art of nA-range current references in Table V and µA-range temperature-independent ones in Table VI. These tables are complemented by Fig. 24 representing some of the most important trade-offs for current references. For both PTAT and CWT designs, measurements are reported for the 0.18-µm PDSOI references. In addition, we present post-layout simulations in 0.18-µm PDSOI, 65-nm bulk and 28-nm FDSOI, while the vast majority of other works limit themselves to older technology nodes, typically 0.18-µm or above.

Figs. 21(c) and 22(b)), i.e., the body of $M_{2,n}$ tied to the source of $M_{2,n-1}$, is expressed as

$$v_{ref} \approx \frac{g_{d2,1}}{g_{d2,1} + g_{d1} + g_{m2,2} + g_{d2,1} + g_{d2,2}}, \quad g_{d2,2}$$

$$v_{ref} \approx \frac{g_{d2,1}}{g_{d2,1} + g_{d1} + g_{m2,2} + g_{d2,1} + g_{d2,2}}, \quad g_{d2,3}$$

for stacks of $N = 2$ and 3 devices, respectively. SBB and hybrid are equivalent for $N = 2$ and lead to an LS of 3.4 mV/V, thanks to the second factor related to the body effect of $M_{2,2}$. Then, SBB and hybrid differ for $N = 3$, reaching a 2.6- and 1.8-mV/V LS, respectively. This difference comes from increased $g_{d2,1}$ and $g_{d2,2}$ in the SBB stack, arising from a $V_{DS}$ lower than $4U_T$ for both $M_{2,1}$ and $M_{2,2}$. On the other hand, $M_{2,2}$ is saturated in the hybrid stack, lowering $g_{d2,2}$ and improving the LS. An hybrid stack with three devices is thus selected to implement the voltage reference.
to five transistors, depending on the voltage reference implementation. Therefore, the silicon area is modest compared to other μA-range references (Fig. 24(a)), with 3410/4270 μm² in 0.18-μm, down to a best-in-class 440-μm² area in 28-nm. [30] has both a small 750-μm² area and a simple structure, as it relies on a 2-V voltage reference to bias transistor gate (Fig. 1(b)), but it suffers from degraded LS and TC, and has a limited 0-to-80°C temperature range. [52], [20] and [22] rely on a handful of components, but [52] has a large 0.003-mm² area, and [20], [22] require a substantial supply voltage above 2 V to operate. [34] occupies a limited 2000-μm² area, but its 720-ppm/°C TC is relatively poor, and the 187+3R structure will likely lead to prohibitive variability due to local mismatch. Regarding TC, our three references feature a very low 38-ppm/°C TC for this current level (Fig. 24(d)), and offer the best trade-off between TC and silicon area (Fig. 24(b)). Other works in Table VI present a low TC, such as [20] with 28 ppm/°C, which requires a 2.5-V supply voltage and consumes a considerable 68.3-μW power, and [25] with 22 ppm/°C, which necessitates a bandgap reference voltage to have a decent LS and occupies 5.3× more area than our largest design. For other metrics, LS amounts to 0.2 %/V and 0.57 %/V in 0.18-μm and 28-nm, but increases up to 4.38 %/V in 65-nm, despite the use of an SBB stack of two devices. On one side, the lower temperature limit is -40°C, except in 0.18-μm where it is limited to 85°C by the measurement equipment. Similarly to their PTAT counterparts, our CWT references are significantly affected by process variations, an issue that can be alleviated through a calibration of IREF. Nevertheless, variability due to local mismatch is comprised between 0.65 and 0.87 %, which is among the best in the state of the art.

### TABLE V

**Comparison of CWT (left) and PTAT (right, with TC highlighted in green) NA-range current references.**

| Publication | Year | Type of work | Technology | Power [μW] | Area [μm²] | Temperature range [°C] | IREF [μA] | IREF var. (process) [%] | IREF var. (mismatch) [%] | No. of samples | Trimming type | Complexity | Special components |
|-----------|-----|-------------|------------|----------|-----------|-----------------------|---------|------------------|-------------------|--------------|---------------|-----------|------------------|
| ISAC5     | 2017 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |
| ISAC6     | 2018 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |
| ISAC7     | 2019 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |
| ISAC8     | 2020 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |
| ISAC9     | 2021 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |
| ISAC10    | 2022 | Sim. silicon | 0.18x 0.18x 0.18x | 2.5x 2x 1.6x | 0.5x 0.5x | -40 to -85 | 1.15 | 0.15 | 0.05 | 10 | Hf 4b | 2BJT + 5C + 2R |

### TABLE VI

**Comparison of μA-range temperature-independent current references.**

| Area [μm²] | Bandgap | Core | Emitter | PNP | PTAT | W | Y | Year | Latitude | Logistics | This work |
|-----------|---------|-----|--------|-----|-----|--|--|-----|---------|----------|-----------|
| ISAC5     | 2017    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |
| ISAC6     | 2018    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |
| ISAC7     | 2019    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |
| ISAC8     | 2020    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |
| ISAC9     | 2021    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |
| ISAC10    | 2022    | 10 | 10     | 10  | 10  | N/A | N/A | 10  | 10     | 10       | 10        |

**Notes:**
- *Estimated from the microscope photograph in Fig. 6 of [25].
- ‡ Varying due to the combined effects of process and mismatch variations.
- ▲ Average of the measurement results.
- Estimated from Fig. 3 of [39].
- § Unretracted and trimmed results.
- ▲ Maximum of the measurement results.
- * In this work, simulations refer to post-layout simulations including parasitic diodes.
In this work, we proposed two novel current reference topologies sharing two key ideas: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering onto a V-to-I converter by a single transistor. These references are fabricated in a 0.18-µm PDSOI process. First, a nA-range PTAT current is obtained by biasing an SCM with a PTAT voltage. It generates a 0.096-nA current, the lowest to date for current references without gate-leakage transistors, and it does so while consuming only 0.28 nW at 0.55 V and 25°C. Second, a µA-range CWT current is obtained by biasing a polysilicon resistor with a matched-TC voltage. It generates either a 0.99-µA current with a 290-ppm/C CTAT TC, or a 1.09-µA current with a 38-ppm/C TC, using a 4-bit calibration of the 2T voltage reference width ratio. Both references exhibit a decent LS (1.48 / 0.21%/V), a low $V_{DD,min}$ (0.55 / 0.65 V), a low variability due to local mismatch (1.66 / 0.87 %), while relying on simple 7T/4T+1R structures without any startup circuit and occupying a limited silicon area of 8700 / 4270 µm². The main drawback of such architectures is their sensitivity to process variations. Furthermore, we discuss the challenges posed by gate leakage, GIDL, and declining intrinsic gain to the implementation of 2T voltages references in scaled 65- and 28-nm technologies. We demonstrate that a proper selection of the transistor type and sizes, together with the use of LS enhancement techniques, can mitigate these non-idealities.

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REFERENCES

[1] D. Blaauw et al., “IoT Design Space Challenges: Circuits and Systems,” in Proc. IEEE Symp. VLSI Technol., 2014, pp. 1–2.

[2] J. Zhang, Z. Wang, and N. Verma, “In-memory computation of a machine-learning classifier in a standard 6T SRAM array,” IEEE J. Solid-State Circuits, vol. 52, no. 4, pp. 915–924, 2017.

[3] S. Yin, X. Sun, S. Yu, and J.-x. Seo, “High-Throughput In-Memory Computing for Binary Deep Neural Networks with Monolithically Integrated RRAM and 90-nm CMOS,” IEEE Trans. Electron Devices, vol. 67, no. 10, pp. 4185–4192, 2020.

[4] M. Seok, K. Kim, D. Blaauw, and D. Sylvester, “A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5V,” IEEE J. Solid-State Circuits, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[5] A. Campos De Oliveira, D. Cordova, H. Klimach, and S. Bampi, “A 0.12-0.4V, Versatile 3-Transistor CMOS Voltage Reference for Ultra-Low Power Systems,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 11, pp. 3790–3799, Sept. 2018.

[6] L. Fassio, L. Lin, R. De Rose, M. Lanuzza, F. Crupi, and M. Alioto, “Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW,” IEEE J. Solid-State Circuits, vol. 56, no. 10, pp. 3134–3144, Oct. 2021.

[7] D. Wang, X. L. Tan, and P. K. Chan, “A 65-nm CMOS Current Source with Reduced PVT Variation,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 4, pp. 1373–1385, Dec. 2016.

[8] H. Wang and P. P. Mercier, “A 3.4-pW 0.4-V 469.3ppm/C Five-Transistor Current Reference Generator,” IEEE Solid-State Circuits Lett., vol. 1, no. 5, pp. 122–125, May 2018.

[9] H. Zhuang, J. Guo, C. Tong, X. Peng, and H. Tang, “A 8.2-pW 2.4-µA Current Reference Operating at 0.5V with No Amplifiers or Resistors,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 7, pp. 1204–1208, July 2020.

[10] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, “A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 2, pp. 61–65, Feb. 2005.

[11] E. M. Camacho-Galeano, J. Q. Moreira, M. D. Pereira, A. J. Cardoso, C. Galup-Montoro, and M. C. Schneider, “Temperature Performance of Sub-1V Ultra-Low-Power Current Sources,” in Proc. IEEE Int. Symp. Circuits Syst., 2008, pp. 2230–2233.

[12] F. Serra-Graells and J. L. Huertas, “Sub-1V CMOS Proportional-to-Absolute Temperature References,” IEEE J. Solid-State Circuits, vol. 38, no. 1, pp. 84–88, Jan. 2003.

[13] Y. Tsividis, Operation and Modeling of the MOS Transistor Second Edition. New York: McGraw-Hill, 1999.

[14] J. V. De la Cruz and A. L. Aita, “A 1-V PTAT Current Reference Circuit with 0.05%/V Current Sensitivity to $V_{DD}$,” in Proc. IEEE Int. Symp. Circuits Syst., 2005, pp. 1205–1208.

[15] Z. Huang, Q. Luo, and Y. Inoue, “A CMOS Sub-IV Nanopower Current and Voltage Reference with Leakage Compensation,” in Proc. IEEE Int. Symp. Circuits Syst., 2010, pp. 4069–4072.

[16] J. Wang and H. Shionohara, “A CMOS 0.85-V 15.8-nW Current and Voltage Reference without Resistors,” in 2019 Int. Symp. VLSI Design Autom. Test, Hsinchu, Taiwan, Apr., 22-25, 2019, pp. 1–4.

[17] H. J. Oguey and D. Aebischer, “CMOS Current Reference Without Resistance,” IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1132–1135, July 1997.

[18] T. Hirose, Y. Asai, Y. Amemiya, T. Matsuoka, and K. Taniguchi, “UltraLow-Power Temperature-Insensitive Current Reference Circuit,” in Proc. IEEE Sensors, 2005, pp. 1205–1208.

[19] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, “A 95-nA, 523ppm/C, 0.6-µW CMOS Current Reference Circuit with Subthreshold MOS Resistor Ladder,” in 16th Asia and South Pacific Design Autom. Conf., 2011, pp. 113–114.

[20] F. Fiori and P. S. Crovetti, “A New Compact Temperature-Compensated MOS Current Reference,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 11, pp. 724–728, Nov. 2005.

[21] T. Kim, T. Brient, C. Han, and N. Maghari, “A Nano-Amperic 2nd Order Temperature-Compensated CMOS Current Reference Using Only Single Resistor for Wide-Temperature Range Applications,” in Proc. IEEE Int. Symp. Circuits Syst., 2016, pp. 510–513.

[22] D. Osipov and S. Paul, “Compact Extended Industrial Range CMOS Current References,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 6, pp. 1998–2006, Jan. 2019.

[23] C. Azcona, B. Calvo, S. Celma, N. Medrano, and M. T. Sanz, “Precision CMOS Current Reference with Process and Temperature Compensation,” in Proc. IEEE Int. Symp. Circuits Syst., 2014, pp. 910–913.

[24] S. S. Chouhan and K. Halonen, “A 0.67-µW 177-ppm/C All-MOS Current Reference Circuit in a 0.18-µm CMOS Technology,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 8, pp. 723–727, Feb. 2016.
[25] A. Bendali and Y.Audet, “A 1-V CMOS Current Reference with Temperature and Process Compensation,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 7, pp. 1424–1429, July 2007.

[26] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, “A 46-ppm/°C Temperature and Process Compensated Current Reference with On-Chip Threshold Voltage Monitoring Circuit,” in 2008 IEEE Asian Solid-State Circuits Conf., 2008, pp. 161–164.

[27] Q. Dong, I. Lee, K. Yang, D. Blaauw, and D. Sylvester, “A 1.02 nW PMOS-Only, Trim-Free Current Reference with 282 ppm/°C from -40°C to 120°C and 1.6% within-wafer inaccuracy,” in IEEE 43rd Eur. Solid State Circuits Conf., 2017, pp. 19–22.

[28] M. Choi, I. Lee, T.-K. Jang, D. Blaauw, and D. Sylvester, “A 23pW, 780 ppm/°C Resistor-Less Current Reference Using Subthreshold MOS-FETs,” in IEEE 40th Eur. Solid State Circuits Conf., 2014, pp. 119–122.

[29] D. Cordova, A. C. de Oliveira, P. Toledo, H. Klimach, S. Bampi, and E. Fabris, “A Sub-1 V, Nanopower, ZTC Based Zero-V Temperature-Compensated Current Reference,” in Proc. IEEE Int. Symp. Circuits Syst., 2017, pp. 1–4.

[30] F. Crupi, R. De Rose, M. Paliy, M. Lanuzza, M. Perna, and G. Iannaccone, “A Portable Class of 3-Transistor Current References with Low-Power Sub-0.5V Operation,” Int. J. Circuit Theory Appl., vol. 46, no. 4, pp. 779–795, Dec. 2017.

[31] L. Fassio, L. Lin, R. De Rose, M. Lanuzza, F. Crupi, and M. Alioto, “A 0.6-to-1.8 V CMOS Current Reference with Near-100% Power Utilization,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 9, pp. 3038–3042, Sept. 2021.

[32] Y.-S. Park, H.-R. Kim, J.-H. Oh, Y.-K. Choi, and B.-S. Kong, “Compact 0.7-V CMOS Voltage/Current Reference with 54/29-ppm/°C Temperature Coefficient,” in Proc. Int. SoC Design Conf., 2009, pp. 496–499.

[33] A. Far, “Subthreshold Current Reference Suitable for Energy Harvesting: 20ppm/°C and 0.1%/V at 140nW,” in 2015 IEEE Int. Autum Meet. Power Electron. Comput., 2015, pp. 1–4.

[34] C. Yoo and J. Park, “CMOS Current Reference with Supply and Temperature Compensation,” Electron. Lett., vol. 43, no. 25, pp. 1422–1424, Dec. 2007.

[35] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, “A Nano-Ampere Current Reference Circuit and its Temperature Dependence Control by Using Temperature Characteristics of Carrier Mobilities,” in IEEE 36th Eur. Solid State Circuits Conf., 2010, pp. 114–117.

[36] W. Liu, W. Khalili, M. Ismail, and E. Kussener, “A Resistor-Free Temperature-Compensated CMOS Current Reference,” in Proc. IEEE Int. Symp. Circuits Syst., 2010, pp. 845–848.

[37] B.-D. Yang, Y.-K. Shin, J.-S. Lee, Y.-K. Lee, and K.-C. Ryu, “An Accurate Current Reference Using Temperature and Process Compensation Current Mirror,” in Proc. IEEE Asian Solid-State Circuits Conf., 2009, pp. 241–244.

[38] C. Wu, W. L. Goh, C. L. Kok, W. Yang, and L. Siek, “A Low TC, Supply Independent and Process Compensated Current Reference,” in Proc. IEEE Custom Integr. Circuits Conf., 2015, pp. 1–4.

[39] Q. Huang, C. Zhan, L. Wang, Z. Li, and Q. Pan, “A 40°C to 120°C, 169 ppm/°C Nano-Ampere CMOS Current Reference,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 9, pp. 1494–1498, Sept. 2020.

[40] L. Wang and C. Zhan, “A 0.7-V 28-nW CMOS Subthreshold Voltage and Current Reference in One Simple Circuit,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 9, pp. 3457–3466, Aug. 2019.

[41] H. Wapu and P. P. Mercier, “A 14.5 PW, 31 ppm/°C Resistor-Less 5 pA Current Reference Employing a Self-Regulated Push-Pull Voltage Reference Generator,” in Proc. IEEE Int. Symp. Circuits Syst., 2016, pp. 1290–1293.

[42] J. Lee and S. Cho, “A 1.4-μW 24.9-ppm/°C Current Reference with Process-Insensitive Temperature Compensation in 0.18-μm CMOS,” IEEE J. Solid-State Circuits, vol. 47, no. 10, pp. 2527–2533, July 2012.

[43] S. Adriaensen, V. Dessard, and D. Flandre, “25 to 300°C Ultra-Low-Power Voltage Reference Compatible with Standard SOI CMOS Process,” Electronics Letters, vol. 38, no. 19, pp. 1103–1104, September 2002.

[44] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, “An MOS Transistor Model for Analog Circuit Design,” IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[45] P. G. Jespers and B. Murmann, “Systematic Design of Analog CMOS Circuits.” Cambridge University Press, 2017.

[46] B. Murmann, P. Nikaean, D. Connelly, and R. W. Dutton, “Impact of Scaling on Analog Performance and Associated Modeling Needs,” IEEE J. Solid-State Circuits, vol. 53, no. 16, pp. 2160–2167, Sept. 2006.

[47] L. L. Lewyn, T. Ytterdal, C. Wulf, and K. Martin, “Analog Circuit Design in Nanoscale CMOS Technologies,” Proc. IEEE, vol. 97, no. 10, pp. 1687–1714, Oct. 2009.

[48] E. Bohannon, C. Washburn, and P. R. Mukund, “Analog IC Design in Ultra-Thin Oxide CMOS Technologies with Significant Direct Tunneling-Induced Gate Current,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 4, pp. 645–653, Apr. 2011.

[49] A. Catelin, “Fully Depleted Silicon on Insulator Devices CMOS: The 28-nm Node Is the Perfect Technology for Analog, RF, mm-W, and Mixed-Signal System-on-Chip Integration,” IEEE Solid-State Circuits Mag., vol. 9, no. 4, pp. 18–26, Nov. 2017.

[50] Y. Ji, C. Jeon, H. Son, B. Kim, H.-J. Park, and J.-Y. Sim, “5.8 A 3.9 nW All-in-One Bandgap Voltage and Current Reference Circuit,” in Proc. IEEE Int. Solid-State Circuits Conf., 2017, pp. 100–101.

[51] H. Kayahan, O. Ceylan, M. Yarali, S. Zhi and Y. Gurbuz, “Wide Range, Process and Temperature Compensated Voltage Controlled Current Source,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 5, pp. 1345–1353, March 2013.

[52] M. S. Eslampanah, S. Kananian, E. Zendehrouh, M. Shariﬁkhani, A. M. Sodagar, and M. Shabany, “A Low-Power Temperature-Compensated CMOS Peaking Current Reference in Subthreshold Region,” in Proc. IEEE Int. Symp. Circuits Syst. 2017, pp. 1–4.

[53] G. Serrano and P. Hasler, “A Precision Low-TC Wide-Range CMOS Current Reference,” IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 558–565, Feb. 2008.