Quality Control (QC) of FBK preproduction 3D Si sensors for ATLAS HL-LHC Upgrades

D M S Sultan, a,∗ M. A. Abdulla Samy, a, b J. X. Ye, a, b M. Boscardin, a, c F. Ficorella, a, c
S. Ronchin a, c and G.-F. Dalla Betta a, b

a TIFPA INFN, Via Sommarive 14, 38123 Trento, Italy
b Department of Industrial Engineering, University of Trento,
Via Sommarive 9, 38123 Trento, Italy
c Fondazione Bruno Kessler, Via Sommarive 18, 38123 Trento, Italy

E-mail: d.m.s.sultan@cern.ch

Abstract: The challenging demands of the ATLAS High Luminosity (HL-LHC) Upgrade aim for a complete swap of new generation sensors that should cope with the ultimate radiation hardness. FBK has been one of the prime foundries to develop and fabricate such radiation-hard 3D silicon (Si) sensors. These sensors are chosen to be deployed into the innermost layer of the ATLAS Inner Tracker (ITk). Recently, a pre-production batch of 3D Si sensors of 50 × 50 μm² pixel geometry, compatible with the full-size ITKPix (RD53B) readout chip, was fabricated. Two wafers holding temporary metal were diced at IZM, Germany, and a systematic QC test campaign was carried out at the University of Trento electronics laboratory. The paper briefly describes the 3D Si sensor design for ATLAS ITk and the required QC characterization setups. It comprises electrical tests (i.e., I-V, C-V, and I-T) of non-irradiated RD53B sensors. In addition, the study of several parametric analyses, i.e., oxide charge density, oxide thickness, inter-pixel resistance, inter-pixel capacitance, etc., are reported with the aid of Process Control Monitor (PCM) structures.

Keywords: Detector design and construction technologies and materials; Hybrid detectors; Radiation-hard detectors; Solid state detectors

© 2022 IOP Publishing Ltd and Sissa Medialab https://doi.org/10.1088/1748-0221/17/12/C12016
1 Introduction

The Large Hadron Collider (LHC) Phase-II upgrade to the higher luminosity \((7.5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1})\) machine known as the High Luminosity-LHC (HL-LHC) [1] shall go through a complete replacement of current ATLAS detectors. A new generation of radiation-hard silicon sensors [2] shall be loaded in the innermost layer “L0” of the Inner Tracker (ITk) with different linear, R0, and R0.5 triplet-flavours. Almost 900 3D Si sensors, compatible with the full-size ITKPix (RD53B) readout chip, shall be needed for this purpose’s required number of triplets. These sensors should sustain a harsh environment of radiation damage for an integrated luminosity up to 2000 fb\(^{-1}\) and a Total Ionizing Dose (TID) of 1 Grad before the replacement. All three foundries (FBK, CNM, and SINTEF) involved in the ATLAS ITk 3D Sensor Collaboration started pre-production fabrication a year ago. Sensors are fabricated on a Si-on-Si wafer, which consists of a high-resistivity float zone active layer of the desired thickness directly bonded to a low-resistivity Czochralski handle wafer. Quality control on FBK pre-production aims to assure the fabrication confidence to ATLAS ITk 3D sensors specifications (AT2-IP-EP-0002). Since no bias structure is allowed on the pixelated 3D detectors, a temporary metal [3, 4] is deposited on the readout side of the wafer, shorting all n-type columns to allow for the measurement of the sensor characteristics. Soon after the measurements are done, the metal layer is removed from the foundry side. As a part of quality control, two dedicated wafers holding temporary metal were diced at IZM, Germany, and shipped to the University of Trento (UniTN) electronics laboratory.
A later section of the paper reports a systematic QC electrical characterization of RD53B 3D sensors: forward I-V, reverse I-V, C-V, and I-T, along with several parametric studies, i.e., oxide charge density, oxide thickness, inter-pixel resistance, inter-pixel capacitance, etc., that help to understand process parameters, their relationship with device characteristics, and failure mechanisms (whether they exist).

2 Sensor Design and Technology

Several processing technologies have been explored for FBK 3D Si sensors [5]. The foreseen HL-LHC extreme radiation damage sets constraints on a small granular pixelated design, with small inter-electrode distances of \( \sim 50 \mu m \) or less. With such a small pitch design, the dead area due to the 3D electrodes is potentially a concern of the detector efficiency. A small electrode diameter of \( \sim 5 \mu m \) has been implemented at FBK to address this issue, reducing the ReadOut Chip (ROC) input capacitance. The state-of-art Deep Reactive Ion-Etching (DRIE) process used to create 3D electrodes has an aspect ratio of about 30:1, compatible with active substrate thickness (150\( \mu m \)). An FBK pre-production batch of \( 50 \times 50 \mu m^2 \) geometry was recently released with the temporary metal (figure 1(a)). Figure 1(b) shows the 3D Si sensor cross-schematic fabricated on the 6-inch wafer. The single-sided process has been adopted to assure mechanical integrity, a lower risk of high wafer bow, and bump-bonding complexity.

![Figure 1.](image)

As a part of the fabrication steps, DRIE is applied to form \( P^+ \)-columns through 150\( \mu m \) high-resistive silicon after the necessary oxidation and implantation of p-spray to the sensor front side, penetrating the low-resistive 500\( \mu m \) handle wafer (thus allowing the sensor back bias). \( N^+ \)-columns are formed at a safety distance of 25\( \mu m \) from the handle wafer to avoid an early breakdown. Both columns are doped with the respective dopants by the thermal diffusion process, followed by filling (at least partially) with poly-Si. A small extrusion poly-Si cap structure is kept in the column openings for a lower leakage current [6]. Several layers of tetra-ethyl-ortho-silicate (TEOS) oxide are poured into protecting the etched columns. Near \( N^+ \)-columns, metal and n-poly Si are separated by \( \sim 150 \) nm thick thermal oxide and TEOS. Bump pads are placed a little further away to avoid a possible capacitive discharge-driven early breakdown and connected with n-poly Si via the contact structure. Finally, an oxide-nitride passivation layer is deposited over the metal,
followed by the openings of bump pads. A temporary metal grid is realized on pixelated sensors and finally removed once the electrical tests are complete. FBK’s recent 3D production technology uses stepper lithography, with a minimum feature size of 350 nm and alignment accuracy of 80 nm [7], allowing enough room to fabricate 24 ITkPix-compliant sensors on a 6-inch wafer (see figure 2). Process Control Monitor (PCM) structures were added around the wafer’s periphery, holding different test structures: 3D diode of different dimensions, 3D strips, planar-MOS, etc.

![Figure 2. Wafer layout details.](image)

3 Experimental setup

QC setup at UniTN holds a manual probe station without thermal chuck in a dark enclosure. No dry air or N₂ flash-inlet is available. A commercial Sensirion temperature & humidity sensor was placed close to the measuring die, and data were logged through an external computer (see figure 3). The experimental ambient condition remained almost stable (temperature $\sim 21 \degree C \pm 2 \degree C$, and RH < 25%). A Keithley 4200 SCS parametric analyzer with four 4210 medium HV-SMUs was used in tests, allowing bias up to $-400$ V ($\pm 210$ V), with the applied voltage accuracy of $\pm 2 \mu$V and the current sensing resolution of 100 fA. This instrument also has a 4210-CVU unit, allowing C-V measurements of the frequency sweep range between 1 kHz–1 MHz. This CVU unit can measure 100 fF noise-limited capacitance. A long integration window was applied for measuring small capacitances below 1 nF. For noise-sensitive C-V measurements, a custom measurement window was used: $(A/D$ integration time, 10 PLC) $\times$ (fill factor, 10).
An Agilent/Keysight SMU mainframe E5270B with Keysight Precision LCR-Meter E4980A was used to perform electrical tests. HV-SMU of the E5270B mainframe has a precision sensing resolution of 10 fA, and the precision LCR-meter can measure aF capacitance. Wafers were probed in dark conditions with a semiautomatic probe station using a dedicated probe card in the controlled ambiance: temperature $\sim 20 \, ^{\circ}\mathrm{C} \pm 1 \, ^{\circ}\mathrm{C}$ and RH < 5%.

4 Experimental results

This section reports a systematic QC study at UniTN on non-irradiated sensors from wafers W09 and W13 (saw-diced at IZM Germany), holding N$^+$-junction columns shorted by temporary metal grids and routed to contact pads in the periphery. Selective electrical tests were made at FBK on wafers.

4.1 Leakage current

I-V tests were performed at FBK on RD53B sensors and test diodes of different dimensions: small (40 × 40 pixels) and big (40 × 80 pixels), with a current compliance of 100 $\mu$A with the applied reverse bias ($V_{\text{bias}}$) of 1 V step and a delay time of 2 seconds. The following breakdown voltage ($V_{\text{bd}}$) definition was used:

$$\frac{I_{\text{leak}} @ (V_{\text{bias}} + 2 \, \text{V})}{I_{\text{leak}} @ (V_{\text{bias}} + 1 \, \text{V})} > 2.$$ (1)

The approach suggests $V_{\text{bd}}$ when there is a 50% leakage rise in a bias step, suitable for a steep avalanche breakdown. A good RD53B sensor reticle is identified with a leakage current <2.5 $\mu$A/cm$^2$ before breakdown voltage ($V_{\text{bd}}$). $V_{\text{bd}}$ value has to be 20 V more than the sensor’s depletion voltage ($V_{\text{depl}}$). Typically, a non-irradiated 3D Si sensor has $V_{\text{depl}}$ of a few volts.

UniTN measurements follow a breakdown measurement approach independent of the depletion voltage. They are also suitable for cases where the leakage current shows a smooth and continuous rise due to defects existing in the original wafer or introduced in the silicon lattice after irradiation [8]. Here, $V_{\text{bd}}$ is the maximum applied reverse bias where the adimensional function $k(I, V) < k_{\text{bd}}$. $k_{\text{bd}}$ is a breakdown value that can be retrieved using the following function of a slope ($\frac{\Delta I}{\Delta V}$) of measured I-V data by using equation (2):

$$k(I, V) = \frac{\Delta I}{\Delta V} \cdot \frac{V}{T},$$ (2)
$k < 1$ represents the sensor ohmic state before the breakdown, and $k \gg 1$ corresponds to the actual avalanche characteristics. In this paper, $k_{bd} = 4$ is chosen, which also suits a large set of irradiated I-V data of the FBK double-sided 3D sensors [9].

UniTN data were acquired after dicing up to a maximum reverse bias of 150 V or until a hard breakdown was noticed. For example, figure 4(a) shows the I-V data for two RD53B sensors of both wafers (W09 and W13), where the leakage current is in good agreement before and after dicing. These results point to a good dicing recipe applied at IZM and minimal contribution of peripheral leakage. The measured leakage before and after dicing is almost two orders of magnitude smaller than the specification. I-V tests were also made for diced diode test structures of different dimensions from wafer W09 (figures 4(b) and (c)), showing a hard breakdown greater than 100 V.

Figure 4. I-V curves normalized to 20 °C: (a) RD53B sensors of wafer W09 and W13 before and after dicing, (b) W09 big diodes ($80 \times 40$ pixels) after dicing, and (c) W09 small diodes ($40 \times 40$ pixels) after dicing.

Figure 5. Measured I-V summary of RD53B sensors of different wafers before dicing: (a) W09 and (b) W13.
Figure 5 reports the I-V summary of RD53B sensors from wafers W09 and W13, measured at FBK on the wafer. Yields of wafer W09 and wafer W13 can be estimated as 54% and 50%, respectively. FBK identified an RD53B sensor as good in the case of $V_{bd} > 25 \text{ V}$ and leakage $< 2.5 \mu\text{A/cm}^2$ (corresponding to 9.6 $\mu\text{A}$ for the considered sensor area). The bias range was limited to 80 $\text{V}$ for a time constraint. Interestingly, many sensors report $V_{bd}$ at 80 $\text{V}$, ascribed from the FBK $V_{bd}$ definition that fails to find smooth breakdowns.

Figures 6(a) and (b) report the I-V data summary of RD53B sensors, measured at UniTN after dicing. A good RD53B sensor is marked when it has $V_{bd} > 30 \text{ V}$ and leakage $< 2.5 \mu\text{A/cm}^2$. The determination of $V_{bd}$ based on $k$-function allows finding the sensor’s actual avalanche-driven breakdown ($\sim 50$–$70 \text{ V}$). Sensors’ operation beyond $V_{bd}$ can input a higher noise to ROC and may also lead to sensor surface-quality degradation by employing electrical stress-driven oxide-charge enhancement over time. For wafer W09, the yield appears precisely the same at 54% after dicing, whereas for wafer W13, the yield drops to 38%. It can be anticipated from the saw dicing uncertainties: (1) broken and rough edges that may lead to form micro-cracks and creates peripheral leakage channel into the active sensor volume, and (2) surface damage during handling, possible source of point-defects. For example, damages were noticed in the W13 RD53B “F” sensor (figure 6(c)), indeed exhibiting an early breakdown.

![Figure 6](image-url)

**Figure 6.** Measured I-V summary of RD53B sensors of different wafers after dicing: (a) W09 and (b) W13. (c) An RD53B reticle “F” micrograph of wafer W13 after dicing.

### 4.2 Leakage stability

Possible time evolution of leakage current is an important operational aspect of 3D Si sensors at ATLAS ITk. The same sensors in figure 4(a) were studied for leakage stability by applying a reverse bias voltage of 30 $\text{V}$ for 48 hours at UniTN. The ambient temperature and relative humidity were logged: $20.5 ^\circ \text{C} \pm 1 ^\circ \text{C}$ and $\sim 19.6 \pm 3.1 \%$. The leakage fluctuation ($F$) was estimated by using equation (3):

$$F = \frac{\max (I) - \min (I)}{\text{average}(I)} \times 100\%.$$

(3)
Figure 7 reports the stability test report. The estimated fluctuation of both sensors was $\sim 5\%$, well below the specification (25%), and can be anticipated from the variation in the ambient conditions.

![Figure 7. Measured RD53B I-T data of different wafers: W09 and W13.](image)

4.3 Bulk capacitance

Bulk capacitance measurements were performed to define the sensor depletion voltage. During the C-V tests of both RD53B sensors and test diodes, an AC signal was chosen with an amplitude of 100 mV. The frequency was set to 10 kHz. For example, figure 8(a) shows RD53B sensors $1/C^2$-V data from different wafers after dicing. The reverse bias was systematically applied with a 1 V increment up to a large reverse bias (till breakdown or dissipation factor $< 1$). The lateral inter-electrode full depletion is reached at a few volts of substrate bias ($\sim 2$–3 V). The capacitance continues decreasing up to large voltages due to the depletion of the p-spray layer at the surface. A second knee is noticed at $\sim 60$ V. A possible explanation is that a weak electric field can be expected underneath the non-passing-through N$^+$-column, requiring a sufficiently large bias to
deplete the gap region. The depletion summary of all RD53B sensors of both wafers can be found in figures 8(b) and (c). Here, $V_{\text{depl}}$ is determined by the interception of two fitted linear segments. The uncertainty of values accounts for the instrument sensing accuracy, errors of linear fits, and the ramp step chosen for substrate biasing. The maximum uncertainty of the reported value is 20%.

### 4.4 Forward current

The forward I-V test is an essential step of sensor QC. It addresses the parasitic series resistance that can play a role in charge collection when it is sufficiently high ($>100 \, \text{k} \Omega$). To address parasitic series resistance ($R_s$), the measured forward I-V data (up to 1 mA) was fitted with the numerical model of ideal current-voltage relation:

$$I_D = I_S \left[ \exp \left( \frac{V_D - (R_S \times I_D)}{\eta \times V_T} \right) - 1 \right]. \quad (4)$$

Rearranging,

$$V_D = \eta \times V_T \times \ln \left( \frac{I_D}{I_S} + 1 \right) + (R_S \times I_D). \quad (5)$$

Here, $I_D$ is the diode current for an applied voltage, $V_D$. $I_S$ is the reverse saturation current (typically, $10^{-15}$ A for Si diode), and $V_T$ is the thermal voltage (0.0254 V for 21 °C). $\eta$ is the ideality factor that accounts for the effect of electron-hole recombination in the depleted volume. If recombination is negligible, the ideality coefficient $\eta \approx 1$, whereas it can otherwise vary in a range ($1 < \eta \leq 2$).

Figure 9(a) shows the measured forward I-V data of RD53B sensors. A numerical fitting model was developed in a MATLAB framework for equations (4) and (5) and applied to the measured forward I-V data using a robust fit-option (i.e., Bisquare). The fit lines are also shown in figures 9(b) and (c). The parasitic series resistance has been several 100 $\Omega$ only (negligible), while the ideality factor was found to be $\sim 1.5$.

![Figure 9](image)

**Figure 9.** (a) Forward I-V plot of RD53B sensors from both wafers. The numerical fit model of the parasitic resistance was applied on: (b) RD53B-W09D & (c) RD53B-W13G.
4.5 Inter-pixel resistance

Interpixel resistance ($R_{\text{int}}$) measurement allows the information of the p-spray isolation implanted between electrodes. A strip test structure was chosen for the test. The central strip was used for sensing current ($I_{\text{int}}$). Two neighboring strips were shorted together (figure 10(a)), and a systematic voltage sweep ($V_{\text{app}}$) was made between $-3$ V to 3 V with a step of 0.2 V. Substrate reverse bias was applied from 5 V to 60 V with a 5 V step. A long integration window was used. $R_{\text{int}}$ is calculated by using equation (6):

$$R_{\text{int}} = \frac{2}{(dI_{\text{int}}/dV_{\text{app}})}.$$

(6)

The ambient temperature was $\sim 21.5$ °C, and relative humidity was below 20%. The remaining strips of the strip structure were kept floating during the tests. Inter-pixel resistance was normalized from the number of pixels per strip (figure 10(b)). As expected, the interpixel resistance is the order of several GΩ (well above the specification) and is independent of the substrate reverse bias.

4.6 Inter-pixel capacitance

Inter-pixel capacitance ($C_{\text{int}}$) measurement quantifies the input capacitance of ROC, which impacts noise. The same strip structure of section 4.5 was chosen for the test. Figure 11(a) shows the experimental setup schematics. 4210 CVU along HV-SMUs was used to probe the inter-strip capacitance. An input AC signal of 100 mV amplitude and 10 kHz frequency was applied from the central strip to neighboring strips in a parallel mode for a substrate bias (varied from 5 V to 100 V with a 5 V step). The rest neighboring strips were kept floating, which would cause a 10% additional contribution to measured capacitance. The maximum uncertainty would vary by 20% of the reported values, considering the instrumentation errors.

The measured interstrip capacitance has been only a few 100 fF per strip, which makes the measurement very challenging. The test needs precise open corrections to eliminate parasitic capacitance from the cables and the whole setup. Particular attention is required for placing several probe needles onto a tiny area on strip pads that generates large stray capacitances whose fluctuations caused by minimal movements of the probe holders are much higher than the
value to be measured. Inter-strip capacitance has been normalized to the number of pixels per strip. Inter-pixel capacitance is $\sim 4 \text{ fF}$ (figure 11(b)) and is independent of applied substrate bias (as expected).

### 4.7 Surface parameters

Dedicated planar MOS structures (with nPoly & Metal, Metal, and TempMetalOnly gate electrodes) were studied to quantify the sensor’s surface conditions from both wafers. Substrate bias varied from $-150 \text{ V}$ to $150 \text{ V}$ with $1 \text{ V}$ step. Figure 12(a) shows three distinctive regions: accumulation, depletion, and inversion. The depletion state has been spread over a large bias range, ascribed from the continuous p-spray depletion between electrodes. A careful finding of flat-band voltage from the measured C-V data, material work-function values, and the FBK process parameters (i.e., substrate doping, etc.) allows for estimating oxide charge and thickness, summarized in figure 12(b). Values are in excellent agreement with the FBK process. Oxide charge density was at most $\sim 10^{11} \text{ cm}^{-2}$, indicating a good surface quality.

![Figure 12. (a) C-V plot of PCM2, 42-W09 different MOS structures for the different substrate biases. (b) Summary of estimated oxide thickness and oxide charge.](image-url)
5 Conclusions

This paper reports FBK $50 \times 50 \mu m^2$ 3D pre-production batch QC studies for non-irradiated diced pixel sensors compared with data measured on the wafer at FBK. Leakage current, leakage stability, and depletion voltage are found within the ATLAS ITk sensor specification and are in good agreement before and after dicing. Parasitic series resistance, interpixel resistance, and interpixel capacitance of FBK 3D sensor production are negligible. The lower yield found for wafer W13 is ascribed to dicing problems. Functional studies (i.e., CCE) and investigations on irradiation candidates shall be explored soon.

Acknowledgments

This work was partially funded by the Italian National Institute for Nuclear Physics (INFN), Projects RD_FASE2 and FASE2_ATLAS (CSN1), and by the H2020 project AIDA-2020, GA No. 654168.

References

[1] C. Gemme et al., The ATLAS Tracker detector for HL-LHC, JPS Conf. Proc. 34 (2021) 010007.
[2] G.-F. Dalla Betta et al., Development of a new generation of 3D pixel sensors for HL-LHC, Nucl. Instrum. Meth. A 824 (2016) 386.
[3] G. Giacomini et al., Development of double-sided full-passing-column 3D sensors at FBK, IEEE Trans. Nucl. Sci. 60 (2013) 2357.
[4] C. Da Via et al., 3D silicon sensors: design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade, Nucl. Instrum. Meth. A 694 (2012) 321.
[5] C. Da Via, G.-F. Dalla Betta and S.I. Parker, Radiation Sensors with 3D Electrodes, ch 4, CRC Press, Boca Raton, FL (2019).
[6] D.M.S. Sultan et al., Characterization of the first double-sided 3D radiation sensors fabricated at FBK on 6-inch silicon wafers, 2015 JINST 10 C12029.
[7] M. Boscardin et al., Advances in 3D sensor technology by using stepper lithography, Front. Phys. 8 (2021) 625275.
[8] N. Bacchetta et al., Improvement in breakdown characteristics with multiguard structures in microstrip silicon detectors for CMS, Nucl. Instrum. Meth. A 461 (2001) 204.
[9] G.-F. Betta et al., Investigation of leakage current and breakdown voltage in irradiated double-sided 3D silicon sensors, 2016 JINST 11 P09006.