Abstract—In this work we present two techniques that tremendously increase the performance of tensor-network based quantum circuit simulations. The techniques are implemented in the QTensor package and benchmarked using Quantum Approximate Optimization Algorithm (QAOA) circuits. The techniques allowed us to increase the depth and size of QAOA circuits that can be simulated. In particular, we increased the QAOA depth from 2 to 5 and the size of a QAOA circuit from 180 to 244 qubits. Moreover, we increased the speed of simulations by up to 10 million times. Our work provides important insights into how various techniques can dramatically speed up the simulations of circuits.

I. INTRODUCTION

Quantum information science has a tremendous potential to speed up calculations of certain problems over classical calculations [1]. To continue the advances in this field, however, often requires classically simulating quantum circuits. Such simulation is done by using classical simulation algorithms that replicate the behavior of executing quantum circuits on quantum hardware on classical hardware such as personal computers or high-performance computing (HPC) systems. These algorithms play an important role and can be used to (1) verify the correctness of quantum hardware, (2) help the development of hybrid classical-quantum algorithms, (3) find optimal circuit parameters for hybrid variational quantum algorithms, (4) validate the design of new quantum circuits, and (5) verify quantum supremacy and advantage claims.

Several approaches have been employed to simulate quantum circuits. The major types include the state-vector evolution approach [2]–[7], linear algebra open system simulation [8], and tensor network contractions [9]–[12]. All these simulators have various advantages and disadvantages. For example, the state-vector evolution approach, while being relatively easy to implement, has an exponential memory requirement with respect to the number of qubits in the circuit, which is a major bottleneck preventing the quantum simulations beyond approximately 46 qubits on modern supercomputers.

In our opinion the most promising type of simulator is the tensor network contraction approach. It is especially efficient for simulating shallow-depth circuits. This approach can be sensitive to the connectivity of a quantum circuit and the types of gates. In this paper we describe the tensor network simulator implementation and show two optimization techniques that enable dramatic speedup of simulations. We use quantum circuits from the Quantum Approximate Optimization Algorithm (QAOA) algorithm since it is a promising candidate for demonstrating quantum advantage and benchmarking quantum devices.

All simulations in our paper used QTensor [13], developed at Argonne National Laboratory. It is a quantum circuit simulator that uses a tensor network contraction approach with a special focus on the simulation of QAOA circuits. It supports simulating both probability amplitudes and energy expectation values.

In the following section we introduce the tensor network contraction approach and describe the QAOA quantum circuits. In particular, we show how the usage of the Feynman path formalism provides the possibility for optimization. We then describe the optimization techniques and the resulting speedup of simulations. The final section contains our conclusions and further directions of research.

II. QAOA ALGORITHM

The QAOA algorithm, introduced by Farhi and Goldstone in 2016 [14], is a seminal hybrid quantum-classical algorithm for approximate optimization. The algorithm can be used to find approximate solutions to NP-complete combinatorial optimization problems. Here we will demonstrate how it works to solve the MaxCut problem and all benchmarking simulations are performed for MaxCut, but this work also applies to other types of tensor network simulations.

The goal of the MaxCut problem is to color all vertices of a given graph $G = (V, E)$, such that the two resulting parts of the graph are connected to each other by the maximum number of edges. The cost function for MaxCut is $C = \frac{1}{2} \sum_{i,j,k} e_{ij} Z_i Z_j + 1$, where $Z_i$ is a label of each vertex.

To solve this problem using QAOA, one has to find optimal parameters for the parametrized ansatz state $|\gamma \beta \rangle$ such that the expectation value of the Hamiltonian cost function $\langle \gamma \beta | H | \gamma \beta \rangle$ is maximized. The ansatz state depends on two parameter vectors $\gamma$ and $\beta$. The length of the parameter vector, denoted $p$, is an important parameter that defines the quality of the solution. For a QAOA depth $p$ with MaxCut on graph $G = (V, E)$, the ansatz state is equal to
$|\gamma\beta\rangle_p = \prod_{k=1}^{p} U_C(\gamma_k)U_B(\beta_k)|+\rangle$, \hspace{1cm} (1)

where $U_B(\beta) = e^{-i\beta\sum_{j\in V} X_j}$ and $U_C(\gamma) = e^{-i\gamma\sum_{(i,j)\in E}(I-Z_iZ_j)}$. Substituting $U_B$ and $U_C$ into (1) and discarding the global phase, we obtain

$|\gamma\beta\rangle_p = \prod_{q=1}^{p} \left[ \prod_{i,j\in E, k\in V} e^{i\delta_kZ_iZ_j} e^{-i\beta_kX_k} \right] |+\rangle$. \hspace{1cm} (2)

A quantum circuit that generates the ansatz state for MaxCut on a fully connected 4-node graph is shown in Figure 1. For a more detailed description of QAOA see [14].

The energy calculation is an important part of the QAOA method, since one can use a classical computer to optimize the $\gamma, \beta$ parameters without having to use noisy quantum devices. In this work, however, we focus on simulating a single amplitude of the ansatz state as a benchmark for demonstrating the optimizations. The results for energy simulations will be discussed in future works.

### III. Methodology

#### A. Tensor network approach

Quantum computers operate by applying gates to a quantum state that describes a quantum system consisting of $N$ subsystems (qubits). One way to describe the evolution of the quantum system is to apply quantum gates in matrix form on the wavefunction in the form of a state vector. With the state-vector evolution approach, each gate action should be described as an operator that acts on the whole system, even if the gate is local to a certain subsystem of qubits. As a result, the whole state vector needs to be stored, which is extremely inefficient in terms of computational resources and memory.

The tensor network approach associates a state vector of the system with a tensor of $N$ indices. Each index in this tensor labels the state of a particular subsystem. That is, the dimension of the index is equal to number of states of the subsystem, which is always 2 in our case. Each gate that
acts on a subsystem can then be described as a tensor. The amplitudes of the resulting state can be calculated by summing the product of the state tensor and the operator tensor over the index of the subsystem.

For example, given a system of two qubits and operator \( \hat{X}_0 \) acting on the first qubit, the resulting state in the state-vector formalism would be \( |\phi\rangle = \hat{X}_0 \otimes I_1 |\psi\rangle \). In tensor network representation, this equation is \( \psi_{ij} = X_{ij} \psi_{ij} \).

If the system is in a product state, then the corresponding state-tensor is a product of smaller tensors representing each subsystem state. In particular, a 2-qubit system in a state \( |0\rangle \) is represented by \( \psi_{ij} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \). Note that the size of this object is \( 2N \) compared with that of \( 2^N \) in the state-vector notation. More details on tensor network formalism are available in [15].

**B. Tensor network contraction**

Simulation of probability amplitudes of a quantum state can be done by contracting a tensor network that represents the quantum circuit that generates the state.

The contraction of a general tensor network can be written by using a line graph approach as following:

\[
R_{i_1 \ldots i_p} = \sum_{j_1, \ldots, j_q \in E} \prod_{e \in F} W_{ij}^e,
\]

where tensor indices \( i, j \in U \) are represented by vertices of a hypergraph \( L = (U, F) \), \( e \in F \) is a hyperedge of \( L \), edges are tuples of indices \( e_i = (v_1, v_2, \ldots, v_d), \forall v_k \in U \), and tensors \( W_{ij}^e \) have the number of dimensions \( d \), the same as the number of vertices in a corresponding edge. For two-level quantum systems, where each tensor dimension has size 2, the sum [3] has \( 2^q \) elements, and each element corresponds to assignment of 0, 1 to each variable.

Instead of calculating every element of this sum, one can merge tensors with each other, producing an intermediary tensor after each merge operation. One way to do this is by selecting some vertices \( j_i \) from all contracted vertices \( \{ j_k \}_{k=1}^q \) and evaluating values of a new intermediary tensor by summing over \( j_i \) a product of only those tensors that have \( j_i \) as their index. The order in which \( j_i \) are selected determines the size of the largest tensor that needs to be stored as an intermediate step in the contraction. Thus the total contraction speed and memory requirements are determined by this intermediate largest tensor, which can reach a very large number of dimensions. More information on ordering tensor networks is available in [16, 12, 17].

**IV. OPTIMIZATION TECHNIQUES**

To speed up and reduce memory requirements of tensor network contraction, we applied two techniques, which we describe in detail in this section. In the first technique we combined gates, and in the second technique we took advantage of the diagonal properties of the gates.

### A. Optimization of QAOA circuit structure

A typical QAOA circuit is shown in Figure 1. We note that Pauli-Z gates are enclosed by two CNOT gates or by Hadamard gates. One can merge these gates in a specialized 2-qubit gate with a parameter \( \gamma \) or parameter \( \beta \) respectively, as shown in the equations below.

\[
\hat{U} = e^{i\gamma \hat{Z}_i \hat{Z}_j}
\]

This gate optimization technique reduces the complexity of the tensor network line graph, as shown in Figure 2. It also makes finding an optimal tensor contraction sequence easier since the line graph has fewer vertices.

### B. Diagonal gate simplification

A certain property of tensors \( W_{ij}^e \) can provide an opportunity for optimization in terms of how these tensors are stored and computed. Each index of sum [3] can have a value 0 or 1 for an \( N \)-qubit system, and each assignment of values to indices corresponds to a single Feynman path which evaluates to an element of the sum [3]. Since the value of each Feynman path is a product of values of different tensors, we know in advance that if for some assignment the value of any tensor is 0, the whole contribution is 0 as well.

In particular, if a tensor \( W_{ij}^e \) from Equation [3] is diagonal, in other words \( W_{ij}^0 = \alpha_i \delta_{ij} \), then for any assignment of indices \( (l, m) = (i_j, l, m) \in U \) from sum [3], in which values of the diagonal tensor indices match, the corresponding element in the sum will be equal to zero. The tensor \( W_{ij}^0 \) can then be safely removed from the tensor network and replaced by \( \alpha_i \) without changing the result.

Here is a 2-gate example demonstrating how our diagonalization technique is applied.

\[
|\phi\rangle = \hat{U} \hat{D}|\psi\rangle = \sum_{j_k} U_{ij} D_{jk} \psi_k = \sum_{j} U_{ij} \alpha_j \psi_j
\]

We note that QAOA circuits have only one type of a 2-qubit gate: \( \hat{Z} \hat{Z} = e^{i\gamma \hat{Z}_i \hat{Z}_j} \). The \( \hat{Z} \) gate is diagonal, as is \( \hat{Z} \hat{Z} \); therefore, the matrix of the \( \hat{Z} \hat{Z} \) gate in the 2-qubit basis will be diagonal.

\[
\hat{Z} \hat{Z} (\gamma) = e^{i\gamma \hat{Z}_i \hat{Z}_j} = \text{diag}(e^{i\gamma}, e^{-i\gamma}, e^{-i\gamma}, e^{i\gamma})
\]

We can use this fact to replace the 4-index tensor \( U_{ijkl} \) representing a generic 2-qubit gate with a 2-index tensor \( U_{ij} = (\hat{D}_{pi}) \), \( p = e^{i\gamma} \) that represents a diagonal gate. This significantly reduces the computational cost for tensor contraction and the memory requirements to store these tensors.
In this section we evaluate the simulation complexity of different combinations of quantum circuits. For this work we used the number of FLOPs required for contraction as the main metric of simulation complexity. We used only the FLOPs metric because it is easy to use and both computational and memory requirements can be easily estimated from each other. The number of FLOPs can be estimated as \( 2^C \), where \( C \) is a contraction width, or the number of dimensions of the largest intermediary tensor. Thus, one can safely assume that the maximum memory in bytes for the contraction will be \( 16 \times 2^C \), positing the size of a single complex number to be 16 bytes.

First, we selected 5 random 3-regular graphs, for which we formulated the MaxCut problem by using QAOA. Then, each graph was used to generate quantum circuits that produce QAOA ansatz. There are two types of circuits: one using ordinary decomposition of 2-qubit gates into three gates and another using the \( \hat{Z} \hat{Z} \) gate simplification, as described in Section IV-A, where the complexity of the circuit is reduced. For each quantum circuit, we constructed a tensor network using two approaches: with diagonal simplification and without it, as described in Section IV-B. The tensor network was then sliced to produce the first amplitude of the ansatz state when all its indices are contracted. We then used the \texttt{rgreedy} algorithm from the \texttt{QTensor} package with \( n \_\text{repeats}=10 \) and \( \text{temp}=0.02 \) to obtain a contraction sequence, which we used to estimate the number of FLOPs required for the contraction. Dependence of the contraction complexity from the contraction ordering time is shown in Figure 3. The experiments in this paper aim to demonstrate the difference between simulation of quantum circuits optimized using different techniques, rather than absolute values of the simulation cost. Hence, we pick relatively modest ordering algorithm parameters that result in 1 second of ordering time.

Further analysis of contraction complexity is shown in Figure 3. In this figure, the number of FLOPs for simulating a single amplitude of QAOA ansatz circuit versus the number of QAOA iterations \( p \) is shown. The data in the plot is evaluated for five random 3-regular graphs. From the figure one can see that diagonal gates and \( \hat{Z} \hat{Z} \) gate optimization techniques dramatically reduce the number of FLOPs compared with the original unoptimized tensor network graphs.

We also analyzed how the number of FLOPs is correlated with the size of the circuit in terms of the number of qubits \( N \). Figure 4 shows the number of FLOPs for simulating a single amplitude of QAOA ansatz circuit versus the number of QAOA iterations \( p \) is shown. The data in the plot is evaluated for five random 3-regular graphs. From the figure one can see that diagonal gates and \( \hat{Z} \hat{Z} \) gate optimization techniques dramatically reduce the number of FLOPs compared with the original unoptimized tensor network graphs.

From the analysis of Figures 3, 4, and 5, it is surprising to find out that using only \( \hat{Z} \hat{Z} \) gate optimization is not enough to get significant computational and memory savings. We note that using the diagonal gates is what really provides dramatical better results, especially when combined with gate optimization.

The simulation of quantum circuits is usually a memory-bound task because of memory requirements to store an intermediate tensor. The optimization techniques described in this paper allow simplification of a tensor network structure with \( \hat{Z} \hat{Z} \) and diagonal gates, which in turn helped us find the optimal tensor contraction sequence. As a result, we extended the depth \( p \) and the number of qubits \( N \) of the largest circuits that is feasible to simulate using a laptop or a supercomputer, as shown in Tables I and II. A laptop is assumed to have 4 GB of memory, and a supercomputer is assumed to have 800 TB of aggregated memory.

Our optimization techniques also can be applied to the simulation of the QAOA energy expectation value. Thus, it would allow us to find parameters for even larger circuits with higher depth.
In this work, we implemented and demonstrated that $\hat{Z}Z$ gate optimization and diagonal gate techniques can lead to dramatic savings in terms of memory and computation requirements. As a result, we were able to simulate much larger QAOA circuits both in size and in depth, as shown in Tables I and II.

We were able to increase $p$ from 2 to 5 and the size of a QAOA circuit $N$ from 180 to 244 qubits on a supercomputer. These numbers were estimated without actually running on a supercomputer, but the laptop results have been actually verified.

The tensor network contraction method for simulation of quantum circuits is a powerful approach that has the potential to simulate very large quantum circuits. At the same time, however, a lot of improvements, simplifications, and approximations can be used to improve the simulations and dramatically decrease memory and computational requirements. For example, in this work we sped up quantum simulations by up to 10 million times, as can be seen in Figure 3 in the “diagonal+ZZ gates” curve versus “default” curve for $p = 5$.

Moreover, there is room to speed up simulations by an even larger factor. This work underscores how one needs to be careful when comparing tensor network simulations against classical solvers and quantum hardware for demonstration of quantum supremacy and advantage. Our work provides important insights into how various optimization techniques can speed up tensor network simulations and what other techniques can be used to achieve this goal.

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