Scalable Realization of Surface Code Quantum Memory by Applying Multi-Qubit Parity Detector Gates
Sahar Daraeizadeh . Sarah Mostame . Preethika Kumar Eslami . Marek Perkowski . Xiaoyu Song

Abstract We analytically designed the control bias pulses to realize new multi-qubit parity detector gates for 2-Dimensional (2D) array of superconducting flux qubits with non-tunable couplings. We designed two 5-qubit gates such that the middle qubit is the target qubit and all four coupled neighbors are the control qubits. These new gates detect the parity between two vertically/horizontally coupled neighbor qubits while cancelling out the coupling effect of horizontally/vertically coupled neighbor qubits. For a 3×3 array of 9 qubits with non-tunable couplings, we simulated the effect of our new 5-qubit horizontal and vertical parity detector gates. We achieved the intrinsic fidelity of 99.9% for horizontal and vertical parity detector gates. In this paper we realize Surface Code memories based on the multi-qubit parity detector gates for nearest neighbor superconducting flux qubits with and without tunable couplings. However, our scheme is applicable to other superconducting qubits as well. In our proposed memory realization, error correction cycles can be performed in parallel on several logical qubits or even on the entire 2D array of qubits, this makes it a desirable candidate for large scale and longtime quantum computation. In addition to extensive reduction of the number of control parameters in our method, the error correction cycle time is reduced and does not grow by increasing the number of qubits in the logical qubit layout. Another advantage of this approach is that there will not be any dephasing from idle qubits since all the qubits are used in the error correction cycles.

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Abbreviations
NN Nearest neighbor
1D 1-Dimensional
2D 2-Dimensional
CNOT Controlled-NOT
QEC Quantum error correction
1 Introduction

One of the most important areas of research in the field of quantum computing is to design and implement high efficiency and fault tolerant scalable quantum architectures. The quantum systems are intrinsically error prone since the state of qubits can change by environmentally-induced errors. Therefore, it is required to apply quantum error correction schemes to preserve the state of qubits during the idle times. Quantum errors on single qubits will propagate in quantum circuits through multi-qubit quantum gates. A bit-flip error in a control qubit propagates to the target qubit and a phase-flip error in a target qubit propagates to the control qubit. Additionally, erroneous gates can introduce errors to their coupled qubits. Furthermore, in Quantum Error Correction (QEC) schemes, an error in measurement can introduce errors to the result of calculation, however we are not considering these errors in this paper.

There are many quantum error correcting codes [1]. Some of the most recognized ones are Shor’s 9 qubits code [2], Steane 7 qubits code [3], Calderbank-Shor-Steane (CSS) code [4], Stabilizer code [5], and more recently the Bacon-Shore code, Repetition Code, and Surface Code [6, 7, 8, 9]. One of the most promising fault tolerant quantum computing schemes that follows the fault tolerant metrology proposed by Martinis [10] is the Surface Code [1]. Martinis [10] proposed a metrology for fault-tolerant error correction for scalable quantum computers by measuring qubit parities which detect bit-flip and phase-flip errors in pairs of qubits. Based on his metrology, in a parity operation which consists of one-qubit, two-qubits and measurement components, we need to keep the error probability of each component less than a defined threshold to reach an error suppression factor $\Lambda$ of higher than 1. Higher order error detections lead to lower logical error probability $P_l$ as follows [10]:

$$P_l = \Lambda^{-(n+1)} \quad (1)$$

here $n$ is the order of error, and $\Lambda = \epsilon_t/\epsilon$ is the error suppression factor, where $\epsilon$ is the probability of physical error, $\epsilon_t$ is the error threshold. According to Martinis, $\Lambda$ is “the key metrological figure of merit that quantifies how much the decoding error drops as the order $n$ increases by one” [10]. Here $\Lambda > 1$ means that the physical error $\epsilon$ is lower than the threshold $\epsilon_t$, and by making the error correction code larger the decoding error is decreased exponentially with $n$ [10]. Assuming after Martinis that a typical quantum algorithm implementation uses 1018 operations, and that we need to achieve the overall logical error probability of less than $P_l = 10^{-18}$ meaning a suppression factor of $\Lambda = 10$, this leads to order error $n = 17$. To achieve error correction of $n$ order in a Surface Code architecture [8] we need $(4n+1)\times(4n+1)$ array of qubits. This requires as many as 4761 qubits for $n=17$. Although the cited above number seems to be large, Surface Code architecture still is the best practical error correction method for fault tolerant
quantum computing because of high tolerance to the errors which allows error rate of 1% per operation. Moreover, its two-dimensional physical layout with nearest neighbor couplings makes it a scalable and practical approach in solid-state quantum computers [1], [8], [10]. Furthermore, because of simple projective measurements, and tracking of the detected errors in software, there is no need for applying physical correction gates, therefore introducing less noise and perturbation to the physical system. In Surface Code error correction, it is of high interest to be able to perform error correction cycles on many qubits simultaneously which is the focus of this work.

The surface code architecture is based on the stabilizer formalism and consists of Z and X stabilizers [7]. Surface Code introduces ancillary qubits dedicated to these stabilizers and repetitively performs projective quantum non-demolition (QND) parity measurements on these ancillary qubits to measure the bit-flip and phase-flip errors of the data qubits [8]. The number of ancillary qubits in these measurements is approximately equal to the number of data qubits. Although it has been shown that this approach results in storing information with a lower error rate, the Surface Code methodology has a high computational and resource overhead to realize the logical states and process information. It has been shown [34-38] that the distance-three Surface Code is achievable with reduced number of physical qubits from Surface-25 to Surface-17 and Surface-13. In [8] the authors created a logical qubit from 13 physical qubits and performed quantum error correction to preserve the logical states. In [35] the authors showed that the Surface-17 code has the best threshold with lowest cost and is a suitable candidate for experiments and architectural explorations [35], [19]. Therefore, we focus on Surface-17 code to illustrate our memory architecture, however, our proposed scheme is extensible to very large-scale Surface Code architectures and larger logical qubits. Surface-17 code consists of 9 data qubits surrounded by 8 measurement qubits (four X and four Z stabilizers).

Quantum errors and instability of quantum states are considered fundamental obstacles to achieve large scale quantum computers. Therefore, investigating methodologies to design quantum architectures with efficient error correction schemes is an important area of research. By efficient designs we mean those that have reduced control circuitry and less computational overhead, are more reliable and faster. In this work we aim to find such an efficient Surface-17 Code implementation to realize large scale 2-Dimensional Nearest Neighbor (NN) quantum computers. This was possible due to our new multi-qubit (more than three qubits involved) parity detector gates which can act on many qubits simultaneously.

1.1 Previous works
In [19] a scalable scheme for Surface Code implementation is proposed for flux tunable transmons [23] with nearest-neighbor couplings. The authors use two-qubit controlled-phase gate as the primitive gate for executing error correction cycles. In their method, each cycle includes 4 sequences of two-qubit controlled-phase gates (each takes 40 ns) in combination with Hadamard gates (each takes 20 ns) and measurement operations (takes 500 ns). For Surface Code architectures constructed from logical qubit layouts of sizes 8 and 17, this leads to the circuit depths 7 and 9, respectively. The number of gate levels to realize one full error correction cycle is considered as the circuit depth. In [19], without considering the time for measurement operation, the remaining time required to perform error correction cycle on Surface-8 code is 200 ns, while this time increases to 240 ns for Surface-17 code.

Ghosh et. al. in [24] investigated three different Surface Code architectures based on transmons. Their so-called Textbook Surface Code architecture [24] consists of 2D array of tunable transmons with tunable couplings. The time duration for each error correction cycle for Textbook architecture is 164 ns.

The Helmer architecture [36] consists of transmons in a 2D array such that each transmon is coupled to one vertical and one horizontal cavity, and the Surface Code cycle time is 160 ns. This architecture has tunable couplings, but it is not scalable to large number of qubits as the method requires to allocate frequencies to all qubits and the minimum frequency range needed is proportional to the square root of the number of qubits [24].

In DiVincenzo architecture [37], each transmon is dispersively coupled to two resonators, while each resonator is coupled to four qubits. This architecture is fully scalable, however; the couplings are not tunable, and each error correction cycle time takes 400 ns.

The Textbook and Helmer architectures both have tunable couplings and the qubit relaxation time is 1-10 µs, while DiVincenzo architecture with non-tunable coupling has 1-40 µs qubit relaxation time.

The discussed above architectures and their timings [19, 36, 37] considered a transmon based physical realization. Currently we don’t know any Surface Code architecture based on flux qubits in literature and since quantum computers based on flux qubits remain of high importance among Superconducting qubits architectures, here we propose an efficient scalable Surface Code architecture for flux-based physical model.

We consider a 2D nearest neighbor superconducting architecture consisting of flux qubits with long-range DC-SQUIDs (DC Superconducting Quantum Interference Devices) couplings. In [22] Fowler et. al. presented an architecture based on flux qubits with long-range couplings that is scalable and suitable for 2D error correction codes. In [21] authors designed tunable couplings based on the architecture proposed by Fowler in [22]. This motivated us to design a single-shot multi-qubit parity detector gate for tunable
coupled [21] flux qubits architectures. A single-shot gate means that only one single pulse is required to realize the gate operation. In [11] we introduced a novel single-shot multi-qubit parity detector gate and applied this parity gate to generate efficient circuits for Mirror Inversion (MI) [12, 13, 14] as a sequence of controlled-unitary operations between 2-Dimensional nearest neighbor qubits. The method from [11] significantly increased the efficiency by lowering the computational overhead since the state transfer could be achieved in less computational steps without needing ancillary qubits. Furthermore, there was not any dephasing from idle qubits since all the qubits were used in the MI operation as target or control qubits. Dephasing or qubit precession is a phenomenon in qubits based on Josephson junction or trapped ion in which the basis states are non-degenerate in the absence of external interactions. Therefore, when no gate operations are performed, a time-varying relative phase develops between the basis states [15]. One way to overcome dephasing is to design special encoding architectures as presented in [15] and [16].

In [17], the author analytically showed how a multi-qubit controlled-unitary gate can be achieved in a single pulse and suggested the usage of this gate in error correction codes. These results motivate us to extend the work from [11, 17] to investigate designing multi-qubit parity detector gates and apply them to the Surface Code architecture to achieve less computational overhead, less control circuitry, and faster error correction cycles.

1.2 Our proposed architecture

Here we explain how the parity detector gates can be used in a memory realization for 2D NN architectures based on Surface Code error correction. We achieved reduced computational overhead and overall error correction cycle time and simplified control circuitry. For the systems with non-tunable couplings where couplings cannot be turned off, we realize Surface Code architecture by designing a new multi-qubit parity detector gate where each target qubit is connected to 4 adjacent control qubits. In tunable coupling architectures, we can complete each error correction cycle in two pulse sequences of multi-qubit gates in combination with Hadamard gates and measurement operations. This approach leads to maximum depth 5 circuit realization for any size Surface Code architecture. The multi-qubit gate operation only takes 10 ns in our considered physical model. This approach extensively reduces the error correction cycle time comparing with possible corresponding traditional approaches which would utilize 4 CNOT gates, each taking 10 ns for flux qubit-based architectures.

For systems with non-tunable couplings, the interaction between qubits cannot be turned off. Therefore, we designed two new 5-qubit parity detector gates that detect the parity of horizontal or vertical coupled
qubits, respectively. Each gate takes three pulse sequence, each taking 10 ns, and the total gate time is 30 ns. In section 3, we show in detail how a five-qubit parity detector gate can be realized in systems with non-tunable couplings. Using these new gates, a Surface Code architecture is designed where each error correction cycle can be completed in four sequences of multi-qubit gate operations in combination with Hadamard gates and measurement operations.

Since the gate operation time is a control parameter, it is important to note that we can reduce the multi-qubit gate operation time even more by adjusting other system parameters. Additionally, in our approach there are no qubit left idle, therefore, it does not suffer from qubits precessions in idle times.

In section 2, we provide some background about simulation method and analytical design of existing single-shot parity detector gate for systems with tunable couplings. In section 3, we explain the physical model that we used in this work as well as the analytical design of the new multi-qubit parity detector gate for systems with non-tunable couplings. In section 4, we briefly introduce the Surface Code memory realization. In section 5, the Surface Code architectures utilizing the multi-qubit parity detector gates are proposed. In section 6, we conclude our work and plot the future research directions.

2 Background

In [11] authors introduced a novel single-shot multi-qubit parity gate for superconducting qubits with Ising interactions. This gate inverts the state of the target qubit only if the two neighbor control qubits have opposite logical states. Here in section 2.1, the quantum simulation method is explained. In section 2.2 we introduce a new logical notation to describe a parity detector gate. In section 2.3, the analytical approach for designing a quantum gate for systems with tunable couplings is reviewed.

2.1 Simulation method

To simulate the dynamics of a quantum system, a Time Dependent Schrödinger Equation (TDSE) needs to be solved. Knowing the initial state of the system and the Hamiltonian, the time evolution of the state of the system is calculated as follows:

$$|\psi(t)\rangle = e^{-iHt/\hbar} |\psi(t_0)\rangle$$  \hspace{1cm} (2)

Here, for a single qubit system, the state $|\psi(t_0)\rangle$ is the initial state of the system at start time $t_0$, the state $|\psi(t)\rangle$ is the probability distribution for the outcome of each possible measurement on the system at time $t$:

$$|\psi(t)\rangle = \alpha |0\rangle + \beta |1\rangle \hspace{1cm} |\alpha|^2 + |\beta|^2 = 1$$  \hspace{1cm} (3)
where \( \alpha \) is the probability amplitude of qubit being in state \(|0\rangle\) and \( \beta \) is the probability amplitude of qubit being in state \(|1\rangle\). The Hamiltonian \( H \) is the time evolution operator that maps the current quantum state to the next state. \( \hbar = \hbar / 2\pi \), where \( \hbar \) is the Planck constant. In our simulations Planck constant is normalized to 1.

We can write the Schrödinger equation as below where \( U \) is the unitary transformation of the system.

\[
|\psi(t)\rangle = U |\psi(t_0)\rangle \tag{4}
\]

Any single qubit gate operation can be realized using a 2x2 unitary matrix \( U \) \cite{29}:

\[
U = e^{i\alpha} R_z(\beta) R_y(\gamma) R_z(\delta) = e^{i\alpha} \begin{bmatrix} e^{-i\frac{\beta}{2}} & 0 \\ 0 & e^{i\frac{\beta}{2}} \end{bmatrix} \begin{bmatrix} \cos \frac{\gamma}{2} & -i \sin \frac{\gamma}{2} \\ i \sin \frac{\gamma}{2} & \cos \frac{\gamma}{2} \end{bmatrix} \begin{bmatrix} e^{-i\frac{\delta}{2}} & 0 \\ 0 & e^{i\frac{\delta}{2}} \end{bmatrix} \tag{5}
\]

where \( \alpha \) is the global phase factor, \( R_z(\beta) \) and \( R_z(\delta) \) are the rotations \( \beta \) and \( \delta \) around the Z axis, and \( \gamma \) is the rotation around the Y axis in a Bloch sphere.

In the realm of gate design, we would like to set up the control parameters of the system such that the unitary operation \( U \) becomes as close as possible to our target gate transformation matrix. This can be done experimentally \([20, 25, 26, 27, 30]\), analytically \([32]\), by utilizing optimization methods \([33]\), or Machine Learning approaches \([18, 28]\).

### 2.2 Introducing the notation of parity detector gate

As we know the symbol of full colored circle on a control qubit means that when the logical state of control qubit is 1, the gate operation is performed on the target, while the symbol of empty circle means that when the logical state of control qubit is 0, the gate operation is performed on the target qubit. As shown in Fig. 1 (a), we introduce the half-colored circles which mean that the logical state of the control qubit can be 1 or 0. The half-colored circles are meaningful when applied in pairs to represent the opposite states of two control qubits resulting in a gate operation on target qubit as shown in Fig. 1 (b). For instance, in Fig. 1.b. there is a left-half colored circle on top control qubit, while on the bottom control qubit there is a right-half colored circle. This means that the two pairs of control qubits must be in opposite states for the target qubit to change its state (detect parity).

![Fig. 1](a) Notations to represent the state of the control qubits in controlled unitary operations (b) A 3-qubits parity detector gate. Half colored circles can be used in pairs to represent the parity of the states of a pair of control qubits.
2.3 Parity detector gate for systems with tunable couplings

In this section we explain the analytical derivation of Multi-qubit single-shot parity detector gate for 2D NN systems with tunable couplings based on the work in [11]. To illustrate how we can analytically design controlled-unitary gates, consider the example for a 3-qubit parity detector gate, where the target B is the middle qubit and the adjacent qubits A and C as shown in Fig. 2 are the control qubits. The state of B changes from $B = b$ to $B = a \oplus b \oplus c$, while the states of qubits A and C do not change, $A = a$, and $C = c$. We consider a 1D NN superconducting architecture that consists of flux qubits inductively coupled through DC-SQUIDs [21, 22].

![Fig. 2 Three adjacent qubits in a 1D NN architecture](image)

We define the couplings $\xi_1$ and $\xi_2$ between qubits A and B, and B and C, respectively. In tunable coupling systems, during the quantum computation we can change the value of the couplings from negative to positive values including zero [21]. We consider systems in which all qubits have the same tunneling energy parameter $\Delta$, and the coupling energy is much higher than the tunneling energy ($\xi \gg \Delta$) [31]. Knowing that any single-qubit gate operation can be realized using a 2×2 unitary matrix $U$ as shown in Eq. (6), we can use a reduced Hamiltonian scheme [31, 32] to realize arbitrary controlled-unitary operation with multiple control qubits and one target qubit. To design such a gate, we apply a high bias $\varepsilon$ to all the control qubits to preserve their state, and we adjust the bias on the target qubit for the duration of gate operation. The Hamiltonian of a system shown in Fig. 2 can be written as follows:

$$H = \Delta (\sigma_x A + \sigma_x B + \sigma_x C) + \varepsilon_A \sigma_z A + \varepsilon_B \sigma_z B + \varepsilon_C \sigma_z C + \xi_1 \sigma_x A \sigma_x B + \xi_2 \sigma_x B \sigma_x C$$

(6)

For a parity detector gate realized as shown in Fig. 2, qubits A and C are control qubits, therefore, we can decompose the Hamiltonian in Eq. 6 to 4 subspaces depending on the logical states of A and C. The expectation value of $\sigma_z$ Pauli matrices for qubits A and C are +1 or -1 depending on the state of them being in $|0\rangle$ or $|1\rangle$. The expectation values of $\sigma_x$ Pauli matrices for qubits A and C are zero when their states are frozen to $|0\rangle$ or $|1\rangle$. Therefore, the above Hamiltonian is reduced to four 2×2 Hamiltonians for qubit B in the subspaces based on the basis states of qubits A and C being $|00\rangle$, $|01\rangle$, $|10\rangle$, and $|11\rangle$ [11].

$$H_B^{00} = \Delta \sigma_x B + \varepsilon_B \sigma_z B + \xi_1 \sigma_z B + \xi_2 \sigma_z B$$

(7)

$$H_B^{01} = \Delta \sigma_x B + \varepsilon_B \sigma_z B + \xi_1 \sigma_z B - \xi_2 \sigma_z B$$

(8)

$$H_B^{10} = \Delta \sigma_x B + \varepsilon_B \sigma_z B - \xi_1 \sigma_z B + \xi_2 \sigma_z B$$

(9)

$$H_B^{11} = \Delta \sigma_x B + \varepsilon_B \sigma_z B - \xi_1 \sigma_z B - \xi_2 \sigma_z B$$

(10)
Note that the bias terms associated with the control qubits A and B only contribute to a global phase. By adjusting the bias values such that the overall global phase would be an integer multiple of $2\pi$, we can remove the unwanted phase. For each subspace we take the integration of the Schrödinger equation over the time of gate operation and equate the generated unitary matrix to the desired 2×2 unitary gate operation. For example, to realize a parity detector gate, we want to realize an X operation in subspace $AC = |10\rangle$ and $AC = |01\rangle$, and we want to realize an Identity operation for subspaces $AC = |00\rangle$ and $AC = |11\rangle$. By solving the system parameters for parity operation, we can find the duration time and amplitude of the bias pulse needed to be applied on qubit B. Consider we keep biases on A and C at a high value (3GHz) such that it does not cancel the effect of the couplings and apply a bias pulse to qubit B. We have shown in [11] that by choosing bias on qubit B to be zero and solving system parameters to cancel out unwanted phases we can realize a controlled unitary parity detection gate with 100% fidelity. By changing the bias of qubit B from 3 GHz to zero for duration $T = 10$ ns in a system with the following parameters we achieved a parity detector gate: $\Delta = 25 MHz$, $\xi_1 = \xi_2 = 1 GHz$, $\epsilon_A = \epsilon_C = 3 GHz$. Notice that only one pulse needs to be applied to qubit B to realize the controlled unitary operation. It is important to mention that the gate operation time $T$ is a flexible parameter and we can achieve a shorter gate operation time by increasing the tunneling $\Delta$. The analytical derivation of these values is shown in [11] as well as how the proposed gate can be efficiently used to realize mirror inversion operations in 2D and 3D arrays of NN architectures. In [11], we introduced four single-shot operations based on parity detector gate named P, CNOT-P-CNOT, P-CNOT, and CNOT-P, shown in Fig. 3. All of them can be used in our Surface Code architecture for tunable coupling systems. Note that we can add/remove arbitrary number of three-qubit parity detector gates in the middle to scale up or down these single-shot gates.
We can generalize the Parity detector gate realization to multi-qubit parity detector gate for very large-scale array of qubits. The simulation results for a 9-qubit parity detector P gate (see Fig. 3 (a)) with the input $|Q_9Q_8Q_7Q_6Q_5Q_4Q_3Q_2Q_1\rangle = |100011110\rangle$ are shown in Fig. 4. Looking at the output after applying parity detector gate $|Q_9Q_8Q_7Q_6Q_5Q_4Q_3Q_2Q_1\rangle = |110111100\rangle$, we see that the states of qubits $Q_6$, $Q_7$, and $Q_8$ have changed because the parities were detected between $Q_1$ vs $Q_3$, $Q_5$ vs $Q_7$ and $Q_7$ vs $Q_9$, respectively. While the states of all control qubits were preserved during the gate operation time.
In section 5, we explain how the multi-qubit parity detector operations from Fig. 3 can be used to realize a quantum memory with Surface Code error correction.

3 New Multi-qubit parity detector gates for 2D NN systems with non-tunable couplings

In this section, after describing our physical model we explain the analytical approach of designing the new multi-qubit parity detector gates for systems with non-tunable couplings.

3.1 Physical Model

Consider a 2D NN system with m rows and n columns, where qubits are located using index (j, k), j = 1, 2, ..., m, and k = 1, ..., n. The evolution of a 2D NN system of m×n superconducting flux qubits inductively coupled through DC-SQUIDs [21, 22] with and without tunable couplings [39-42] can be represented by the following Hamiltonian:

$$H = \sum_{k=1}^{n} \sum_{j=1}^{m} (\Delta_{(j,k)} \sigma_x(j,k) + \varepsilon_{(j,k)} \sigma_z(j,k)) + \sum_{k=1}^{n} \sum_{j=1}^{m-1} \xi_{(j,k)(j+1,k)} \sigma_z(j,k) \sigma_z(j+1,k) +$$

$$\sum_{k=1}^{n-1} \sum_{j=1}^{m} \xi_{(j,k)(j+1,k)} \sigma_z(j,k) \sigma_z(j+1,k)$$

(11)

where $\Delta_{(j,k)}$ is the tunneling energy for the qubit located at index $(j, k)$. $\varepsilon_{(j,k)}$ is the bias energy for the qubit located at index $(j, k)$. Here $\xi_{(j,k)(j+1,k)}$ is the coupling energy between two adjacent vertically...
coupled qubits in column \( k \). Similarly, \( \xi_{(j,k)(j,k+1)} \) is the coupling energy between two adjacent horizontally coupled qubits in row \( j \). The couplings can be tunable or non-tunable depending on the physical constraints of the system.

The Hamiltonian operator in Eq. 11 is a \( 2^{m\times n} \times 2^{m\times n} \) matrix. Here, when the number of qubits in the system increases; it is very hard to analytically solve this matrix to derive the system parameters. However, using a reduced Hamiltonian technique [15], we can solve the system parameters to realize a desired gate operation as explained in section 3.2, where it is analytically shown how to derive the control parameters to achieve a multi-qubit parity detector gate. Following a brief introduction to Surface Code in section 4, we show how to use this gate in Surface Code architectures in section 5.

### 3.2 New Multi-qubit parity detector gates for 2D NN systems with non-tunable couplings

In a 2D array of qubits with non-tunable couplings, each qubit is interacting with 4 neighbors. Therefore, to realize a gate operation for 5 qubits, a \( 32 \times 32 \) Hamiltonian matrix represents the evolution of a 5 qubits system (qubits with black labels in Fig. 5). We use the reduced Hamiltonian scheme [31, 32] to break this Hamiltonian to sixteen \( 2 \times 2 \) Hamiltonian matrices. Each \( 2 \times 2 \) Hamiltonian describes evolution of the target qubit \( T \) in a subspace depending on the states of the control qubits \( A, B, C, \) and \( D \). Then for each \( H_{2 \times 2} \) Hamiltonian we generate the unitary matrix by integrating the Schrödinger equation, and next equating the generated unitary matrix to a desirable controlled unitary gate operation for that subspace. In Fig. 5, we show a 9 qubits system that we used in our simulation to prove that the states of the surrounded qubits \( E, F, G, \) and \( H \) are not affected by the proposed parity detector gate operation.

**Fig. 5** In non-tunable coupling systems, each qubit is interacting with 4 neighbor qubits. In this figure, we are interested to perform a Parity detector gate on the target qubit \( T \) where it is coupled directly to qubits \( A, B, C, \) and \( D \). For simulation we considered a sub-system of 9-qubits as shown in the black rectangle. The qubits \( E, F, G, \) and \( H \) don’t have a direct interaction with the target qubit \( T \), but have interactions with \( A, B, C, \) and \( D \). Therefore, we include them in our simulation to show that when their biases stay high the states of these qubits are preserved as well as the states of qubits \( A, B, C, \) and \( D \).
The reduced Hamiltonian for the target qubit T shown in Fig. 5 is represented as below:

\[ H_T^{(\psi)} = \Delta \sigma x_T + (\varepsilon_T + \xi_1 \langle \psi | \sigma z_A | \psi \rangle + \xi_2 \langle \psi | \sigma z_B | \psi \rangle + \xi_3 \langle \psi | \sigma z_C | \psi \rangle + \xi_4 \langle \psi | \sigma z_D | \psi \rangle) \sigma z_T \]  

where \( |\psi\rangle \) represents the subspace where the state of each qubit A, B, C, and D is initialized to \( |0\rangle \) or \( |1\rangle \). We keep all the biases on non-interacting qubits E, F, G, and H high, such that their states are preserved. Note that the qubits E, F, G, and H do not contribute to the Hamiltonian of the target qubit T as they don’t have any direct coupling with T. We can write the unitary operation on target qubit based on the system parameters such as follows:

\[
U = e^{i\theta} \begin{bmatrix}
\cos(\omega t) - i \frac{2\pi}{\omega} \sin(\omega t) & \frac{2\pi(k-i\Delta)}{\omega} \sin(\omega t) \\
\frac{2\pi(-k-i\Delta)}{\omega} \sin(\omega t) & \cos(\omega t) + i \frac{2\pi}{\omega} \sin(\omega t)
\end{bmatrix}
\]  

where \( \varepsilon \) is the effective bias, \( \omega \) is the angular momentum of gate operation, \( \Delta \) is the tunneling, and \( \omega = 2\pi \sqrt{\Delta^2 + E^2} \). Here \( \theta \) is the global phase factor, and \( k \) is considered zero in our physical model.

Depending on the initial state of \( |\psi\rangle \), the expectation value of \( \sigma z_i \) operator can be +1 or -1, where \( i = A, B, C, D \). Now we can choose the system parameters such that the bias of the middle qubit T and couplings of two vertically adjacent qubits A and B (\( \varepsilon_T \pm \xi_1 \pm \xi_2 \)) cancel out the couplings of two horizontally adjacent qubits C and D (\( \pm \xi_3 \pm \xi_4 \)), such that the middle qubit T will not get affected by the horizontally coupled qubits. Therefore, we assume controlled-unitary operations as shown in Fig. 6 (a) to cancel out the effect of horizontal couplings. The architecture to cancel out the effect of vertical couplings is shown in Fig. 6 (b).

Note that the two gates in the middle as shown in Fig. 6 (a) or (b) can be combined in one gate that operates on target qubit if both A vs B, and C vs D are in different states. We can present this gate with four half colored circles on the control qubits, where AB and CD are considered the pairs with opposite half-colored circles as shown in Fig. 7. The pairs of half-colored circles are color coded.
Now we explain the analytical approach to design a multi-qubit vertical parity detector gate in 2D NN array of qubits with non-tunable couplings in more details, then the details of designing a multi-qubit horizontal parity detector gate will be trivial. As shown in Fig. 5, consider qubit T is the target qubit and we want to apply a parity detector gate to detect parity of only qubits A and B which are vertically coupled to the target qubit T. Therefore, we would like to perform an X unitary operation on qubit T \((U_T = X)\) in subspaces \(Q_AQ_B = |10\rangle\) and \(Q_AQ_B = |01\rangle\), irrespective of the states of qubits C, D. In all other subspaces where \(Q_AQ_B = |00\rangle\) or \(Q_AQ_B = |11\rangle\) we want to perform an Identity unitary operation on target qubit T \((U_T = I)\).

| AB  | CD  | Effective Bias                           |
|-----|-----|-----------------------------------------|
| | | \(E = \epsilon_T + \xi_1 + \xi_2 + \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 + \xi_2 + \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 + \xi_2 - \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 + \xi_2 - \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 - \xi_2 + \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 - \xi_2 + \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 - \xi_2 - \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T + \xi_1 - \xi_2 - \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 + \xi_2 + \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 + \xi_2 + \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 + \xi_2 - \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 + \xi_2 - \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 - \xi_2 + \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 - \xi_2 + \xi_3 - \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 - \xi_2 - \xi_3 + \xi_4\) |
| | | \(E = \epsilon_T - \xi_1 - \xi_2 - \xi_3 - \xi_4\) |
Note we consider only the qubits that have direct coupling with the target T. In table 1 we list the effective bias in all 16 possible subspaces of Q_AQ_B = |10⟩, Q_AQ_B = |01⟩, Q_AQ_B = |00⟩, and Q_AQ_B = |11⟩, where qubits C, and D, have arbitrary values.

First let’s consider the subspace Q_AQ_B = |10⟩, where qubits C, and D have arbitrary values, then the effective bias is as follows:

\[ E = \varepsilon_T - \xi_1 + \xi_2 \pm \xi_3 \pm \xi_4 \] (14)

where the notation \( \pm \) means either + or -.

To realize an X operation, we need to cancel the diagonal terms in Eq. 13, and force

\[ \frac{-i2\pi \Delta}{\omega} \sin(\omega t) = -i, \]

where \(-i\) contributes as a global phase factor \( \theta = 3\pi/2 \) on the target qubit. Therefore, the following conditions must satisfy:

\[ \frac{2\pi \Delta}{\omega} \sin(\omega t) = 1 \] (15)

\[ \cos(\omega t) - i \frac{2\pi \varepsilon}{\omega} \sin(\omega t) = \cos(\omega t) + i \frac{2\pi}{\omega} \sin(\omega t) = 0 \Rightarrow E = 0, \cos(\omega t) = 0 \] (16)

Therefore, we need to cancel out the effective bias (\(E=0\)) and satisfy \(\sin(\omega t) = 1\) which results in the following condition:

\[ E = 0, \omega = 2\pi \sqrt{\Delta^2 + \varepsilon^2} \Rightarrow \omega = 2\pi \Delta \] (17)

\[ \sin(\omega t) = 1 \Rightarrow \omega T = \frac{(4n+1)\pi}{2} \] (18)

where \(n\) is an integer and \(T\) is the gate time duration.

One set of parameters to solve Eq. 18 is \(\Delta = 25 MHz\), \(n=0\), \(T=10\) ns, and to cancel out the effective bias (\(E=0\)) we need the following condition:

\[ \varepsilon_T = \xi_1 - \xi_2 \pm \xi_3 \pm \xi_4 \] (19)

where the notation \(\pm\) means either + or -. As shown in Table 1, the effective bias in Eq. 19 (subspace Q_AQ_B = |10⟩), expands to four subspaces depending on the state of Q_CQ_D:

\[ Q_CQ_D = |00\rangle, \varepsilon_T = \xi_1 - \xi_2 - \xi_3 - \xi_4 \] (20)

\[ Q_CQ_D = |01\rangle, \varepsilon_T = \xi_1 - \xi_2 - \xi_3 + \xi_4 \] (21)

\[ Q_CQ_D = |10\rangle, \varepsilon_T = \xi_1 - \xi_2 + \xi_3 - \xi_4 \] (22)

\[ Q_CQ_D = |11\rangle, \varepsilon_T = \xi_1 - \xi_2 + \xi_3 + \xi_4 \] (23)

By choosing \(\xi_1 = \xi_2\), and \(\xi_3 = \xi_4\), Eq. 21 and Eq. 22 converge to \(\varepsilon_T = 0\), while Eq. 20 and Eq. 23 simplify to \(\varepsilon_T = -\xi_3 - \xi_4 = -2\xi_4\), and \(\varepsilon_T = \xi_3 + \xi_4 = 2\xi_4\).

Similar calculation can be done for subspace Q_AQ_B = |01⟩ and reach the same results for bias on target qubit T (\(\varepsilon_T\)).
Therefor to realize an X operation on target qubit T, we keep biases on all control qubits high $\epsilon_A = \epsilon_B = \epsilon_C = \epsilon_D = 3$ GHz, and apply a bias pulse on target qubit with three sequences each taking 10 ns with the following magnitudes.

$$\epsilon_{T_1} = -\xi_3 - \xi_4$$  \hspace{1cm} (24)
$$\epsilon_{T_2} = 0$$  \hspace{1cm} (25)
$$\epsilon_{T_3} = \xi_3 + \xi_4$$  \hspace{1cm} (26)

where $\epsilon_{T_i}$ represents bias magnitude of the $i^{th}$ sequence on target qubit T. The order of applying these three sequences does not matter, since in the end of applying these three sequences (after 30 ns), the desired gate operation has been realized.

Table 2 summarizes all possible effective biases in each subspace under the three pulses given by Eq. 24, Eq. 25, and Eq. 26. Table 2 is derived by substituting the bias value of the target qubit under each sequence $(\epsilon_{T_1}, \epsilon_{T_2}, \epsilon_{T_3})$ in the Effective bias (E) formula shown in Table 1.

To perform an X gate in subspaces $Q_AQ_B = |10\rangle$ and $Q_AQ_B = |01\rangle$, we set the coupling values such that we cancel out the effective bias in one of the three pulse sequences shown in table 2. Under the remaining two pulse sequences in subspaces $Q_AQ_B = |10\rangle$ and $Q_AQ_B = |01\rangle$, as well as all three pulse sequences in subspaces $Q_AQ_B = |00\rangle$ and $Q_AQ_B = |11\rangle$, we want to achieve Identity operation. By choosing $\xi_1 = \xi_2$ and $\xi_3 = \xi_4$, most of the equations in Table 2 simplify or cancel out and only 7 effective bias equations remain which are listed below.

$$E = 2\xi_2$$  \hspace{1cm} (27)
$$E = 2\xi_4$$  \hspace{1cm} (28)
$$E = 4\xi_4$$  \hspace{1cm} (29)
$$E = 2\xi_2 + 2\xi_4$$  \hspace{1cm} (30)
$$E = 2\xi_2 - 2\xi_4$$  \hspace{1cm} (31)
$$E = 2\xi_2 + 4\xi_4$$  \hspace{1cm} (32)
$$E = 2\xi_2 - 4\xi_4$$  \hspace{1cm} (33)

Under the above effective biases, we like to achieve an Identity gate operation. Therefore, we should choose the coupling values such that the off-diagonal terms in Eq. 13 be zero and diagonal terms be 1, this results in the following condition:

$$\cos(\omega t) = 1 \Rightarrow \omega T = 2\pi n \Rightarrow \omega = \frac{2\pi n}{T}$$  \hspace{1cm} (34)
where \( n \) is an integer. Knowing \( \xi \gg \Delta \), we can ignore \( \Delta^2 \) in \( \omega = 2\pi \sqrt{\Delta^2 + E^2} \), which results in \( \omega = 2\pi E = \frac{2\pi n}{T} \). Therefore, we choose the effective biases in equations above as a multiple of some integer over gate duration (10 ns) such as below.

\[
2\xi_2 = 2\frac{\nu}{T} \\
2\xi_4 = 2\frac{w}{T}, \quad 4\xi_4 = 4\frac{w}{T} \\
2\xi_2 \pm 2\xi_4 = \frac{2\nu \pm w}{T} = 2\frac{\nu \pm 2w}{T} \\
2\xi_2 \pm 4\xi_4 = \frac{2\nu \pm w}{T} = 2\frac{\nu \pm 2w}{T}
\]

(35) \quad (36) \quad (37) \quad (38)

Table 2. Effective bias in each subspace under each pulse sequence

| AB  | CD  | \( \epsilon_{T_1} = -\xi_3 - \xi_4 \) | \( \epsilon_{T_2} = 0 \) | \( \epsilon_{T_3} = \xi_3 + \xi_4 \) |
|-----|-----|---------------------------------|----------------|----------------------------------|
| 00  | 00  | \( E = +\xi_1 + \xi_2 \)       | \( E = \xi_1 + \xi_2 + \xi_3 + \xi_4 \) | \( E = \xi_1 + \xi_2 + 2\xi_3 + 2\xi_4 \) |
| 00  | 01  | \( E = \xi_1 + \xi_2 - 2\xi_4 \) | \( E = \xi_1 + \xi_2 - \xi_3 + \xi_4 \) | \( E = \xi_1 + \xi_2 + 2\xi_3 \) |
| 00  | 10  | \( E = \xi_1 + \xi_2 - 2\xi_3 \) | \( E = \xi_1 + \xi_2 - \xi_3 + \xi_4 \) | \( E = \xi_1 + \xi_2 + 2\xi_4 \) |
| 00  | 11  | \( E = \xi_1 + \xi_2 - 2\xi_3 - 2\xi_4 \) | \( E = \xi_1 + \xi_2 - \xi_3 - \xi_4 \) | \( E = +\xi_1 + \xi_2 \) |
| 01  | 00  | \( E = +\xi_1 - \xi_2 \)       | \( E = \xi_1 - \xi_2 + \xi_3 + \xi_4 \) | \( E = \xi_1 - \xi_2 + 2\xi_3 + 2\xi_4 \) |
| 01  | 01  | \( E = \xi_1 - \xi_2 - 2\xi_4 \) | \( E = \xi_1 - \xi_2 + \xi_3 - \xi_4 \) | \( E = \xi_1 - \xi_2 + 2\xi_3 \) |
| 01  | 10  | \( E = \xi_1 - \xi_2 - 2\xi_3 \) | \( E = \xi_1 - \xi_2 - \xi_3 + \xi_4 \) | \( E = \xi_1 - \xi_2 + 2\xi_4 \) |
| 01  | 11  | \( E = \xi_1 - \xi_2 - 2\xi_3 - 2\xi_4 \) | \( E = \xi_1 - \xi_2 - \xi_3 - \xi_4 \) | \( E = +\xi_1 - \xi_2 \) |
| 10  | 00  | \( E = -\xi_1 + \xi_2 \)       | \( E = -\xi_1 + \xi_2 + \xi_3 + \xi_4 \) | \( E = -\xi_1 + \xi_2 + 2\xi_3 + 2\xi_4 \) |
| 10  | 01  | \( E = -\xi_1 + \xi_2 - 2\xi_4 \) | \( E = -\xi_1 + \xi_2 + \xi_3 - \xi_4 \) | \( E = -\xi_1 + \xi_2 + 2\xi_3 \) |
| 10  | 10  | \( E = -\xi_1 + \xi_2 - 2\xi_3 \) | \( E = -\xi_1 + \xi_2 - \xi_3 + \xi_4 \) | \( E = -\xi_1 + \xi_2 + 2\xi_4 \) |
| 10  | 11  | \( E = -\xi_1 + \xi_2 - 2\xi_3 - 2\xi_4 \) | \( E = -\xi_1 + \xi_2 - \xi_3 - \xi_4 \) | \( E = -\xi_1 + \xi_2 \) |
| 11  | 00  | \( E = -\xi_1 - \xi_2 \)       | \( E = -\xi_1 - \xi_2 + \xi_3 + \xi_4 \) | \( E = -\xi_1 - \xi_2 + 2\xi_3 + 2\xi_4 \) |
| 11  | 01  | \( E = -\xi_1 - \xi_2 - 2\xi_4 \) | \( E = -\xi_1 - \xi_2 + \xi_3 - \xi_4 \) | \( E = -\xi_1 - \xi_2 + 2\xi_3 \) |
| 11  | 10  | \( E = -\xi_1 - \xi_2 - 2\xi_3 \) | \( E = -\xi_1 - \xi_2 - \xi_3 + \xi_4 \) | \( E = -\xi_1 - \xi_2 + 2\xi_4 \) |
| 11  | 11  | \( E = -\xi_1 - \xi_2 - 2\xi_3 - 2\xi_4 \) | \( E = -\xi_1 - \xi_2 - \xi_3 - \xi_4 \) | \( E = -\xi_1 - \xi_2 \) |

where \( \nu \) and \( w \) are integers. One set of values we choose for a system with tunneling energy \( \Delta = 25 \text{ MHz} \), and \( T = 10 \text{ ns} \) results in the coupling values \( \xi_1 = \xi_2 = 1 \text{ GHz} \) and \( \xi_3 = \xi_4 = 1.4 \text{ GHz} \).

The above set of parameters realize a parity detector gate that detects the parity of qubits A vs B (vertical) while ignoring the parity of D vs C (horizontal). Fig. 8 shows the simulation result of vertical parity detection gate.
Fig. 8 Simulation results of a 5 qubits vertical parity detector in non-tunable coupling systems. The vertical axis shows the probability amplitude of each qubit being in state $|1\rangle$, and the horizontal axis shows the time considering 0.1 ns time steps. In the simulation, we included 5 ns before and 5 ns after gate operation. The vertical parity detector gate takes 30 ns. At the end of gate duration, the state of the middle target qubit is changed if and only if the vertically coupled neighbors (A and B) are in different states. The state of the horizontally coupled qubits (C and D) do not affect the target qubit.

Similar calculations can be done to design a parity detector gate that detects the parity of qubits D vs C (horizontal) and ignoring the parity of A vs B (vertical). We would like to perform an X unitary operation on qubit $T$ ($U_T = X$) in subspaces $Q_{CQ_D} = |10\rangle$ and $Q_{CQ_D} = |01\rangle$, no matter what the states of qubits A and B are. In all other subspaces where $Q_{CQ_D} = |00\rangle$ or $Q_{CQ_D} = |11\rangle$, we want to perform an Identity unitary operation on qubit $T$ ($U_T = I$). Using the same set of parameters, we can apply a bias pulse with three sequences each taking 10 ns on target qubit with the following magnitudes.

$$\varepsilon_{T_1} = -\xi_1 - \xi_2$$  
$$\varepsilon_{T_2} = 0$$  
$$\varepsilon_{T_3} = \xi_1 + \xi_2$$

Fig. 9 shows the simulation result of horizontal parity detection gate.
Fig. 9 Simulation results of a 5 qubits horizontal parity detector in non-tunable coupling systems. The vertical axis shows the probability amplitude of each qubit being in state $|1\rangle$, and the horizontal axis shows the time considering 0.1 ns time steps. In the simulation, we included 5 ns before and 5 ns after gate operation. At the end of gate duration, the state of the middle target qubit is changed if and only if the horizontally coupled neighbors (C and D) are in different states. The state of the vertically coupled qubits (A and B) do not affect the target qubit.
The simulation results of architectures from Fig. 7 (a) and (b) are shown in Fig. 8 and Fig. 9, respectively. We consider qubits E, F, G, H in the simulation to show that their states will remain unchanged during the 5-qubit gate operations. The average gate fidelity of 99.9% was achieved for a 5 qubits vertical parity detector gate and horizontal parity detector gate operating on a 9 qubits system as shown in Fig. 8 and Fig. 9, respectively.

We used the following formula for the gate fidelity:

\[
\text{Fidelity} = \frac{\text{Abs}(\text{Tr}(U_{\text{target}}^\dagger U))}{512}
\]  \hspace{1cm} (42)

where \( U_{\text{target}} \) is the unitary transformation of the target parity detector gate, and \( U \) is the achieved unitary transformation calculated from the time evolution of the system as follows:

\[
U = e^{-i\frac{\tau}{T}H(\tau)Td\tau}
\]  \hspace{1cm} (43)

where \( T \) is the gate operation time, and \( H(\tau) \) is the Hamiltonian of the system at time \( \tau \).

4 Introduction to Surface Code memory realization

In this section, we briefly introduce the Surface Code memory realization. In surface code quantum computing [8], a 2-Dimensional array of physical qubits is constructed with interleaving data qubits and measurement qubits called measure-Z and measure-X ancillary qubits, and a methodology is presented to protect the architecture from both bit-flip and phase-flip errors at the same time.

In Surface Code error correction, multiple physical qubits form a logical qubit. Therefore, the quantum information is distributed over many physical qubits that consist of data qubits and ancillary measurement qubits. The measure-X and measure-Z qubits detect phase-flip and bit-flip parities, respectively. Each measurement qubit is surrounded by four data qubits in a 2-Dimensional array. At the start, all measurement qubits are initialized to zero. At each error correction cycle, we perform measurements only on ancillary measurement qubits which stabilize the data qubits, i.e., the states of data qubits are not perturbed by the measurement. A software maps the detected error syndromes (bit-flip, phase-flip, measurement error) to a graph model which keeps track of errors and fixes the errors [1].

In [9], Kelly et al. developed an error correction methodology on one-Dimensional (1D) array of linear nearest neighbor (LNN) superconducting qubits named Repetition Code which preserves the logical states of qubits. In the beginning of an error correction cycle, all the measurement qubits are initialized to zero. When qubits are idle, the ZZ operators are repeatedly applied to measure all the measure-Z ancillary qubits in a Repetition Code cycle. If the state of a measure-Z ancillary qubit is flipped in a cycle, a bit-flip error syndrome in adjacent data qubits is detected. If the state of a measure-Z ancillary qubit changes per
two consecutive cycles, a measurement error syndrome is detected. Then the error syndromes are mapped to a graph which represents in software the error propagation model, and a recovery operation is applied to restore the states. It is notable that the recovery operations are applied only in software by tracking error syndromes of all cycles, the software corrects the final data measurement by fixing, if necessary, the measured data [9]. The circuitry used in [9] utilizes the primitive two-qubit controlled-phase gate in combination with single-qubit rotation gates. These gates are applied to qubits in at least three sequences [9] of two-qubit gates on each cycle of Repetition Code before performing parity measurements on the ancillary qubits. They use the parity measurements information to detect bit-flip errors, and then perform some recovery operations to restore the quantum states [9]. Using our proposed parity detector gate, there is only one multi-qubit gate application on all qubits needed in each cycle of Repetition Code in 1D NN architecture. However, here we introduce a more generalized method of error correction in Surface Code that detects both bit-flip and phase-flip errors in 2D nearest neighbor architecture.

We now introduce the building block circuitry that are currently used in the Repetition Code and Surface Code architectures. As we know, applying $\hat{Z}\hat{Z}$ operator to $|00\rangle$ and $|11\rangle$ results in $+|00\rangle$ and $+|11\rangle$, respectively. Applying $\hat{Z}\hat{Z}$ operator to $|10\rangle$ and $|01\rangle$ results in $-|10\rangle$ and $-|01\rangle$, respectively. Therefore, states $|00\rangle$, $|01\rangle$, $|10\rangle$, and $|11\rangle$ are eigenstates of $\hat{Z}\hat{Z}$ operator with corresponding eigenvalues $+1$, $-1$, $-1$, and $+1$. The $\hat{Z}\hat{Z}$ operator then can be used to detect the changes in parity of data qubits. The $\hat{Z}\hat{Z}$ operator can be realized using two CNOT gates applied to three qubits while the ancillary qubit is the target qubit and two data qubits are the control qubits as depicted in Fig. 10. The ancillary target qubit is a measurement qubit called measure-Z qubit and it can be repetitively measured to detect any bit-flip between its neighbor data qubits.

![ZZ operator built from two CNOT gates can detect any bit-flip error of the first and third qubits](image)

Similarly, the measure-X qubit can be used to detect phase-flip errors. An $\hat{X}\hat{X}$ operator can be realized using two CNOT gates applied to three qubits where the middle qubit is the measure-X ancillary qubit and has the control role while the two adjacent data qubits are the target data qubits as depicted in Fig. 11. In Fig. 11, by applying Hadamard gates before and after the ancillary measure-X qubit; we can change the state of measure-X qubit from $|0\rangle$ to $|+\rangle$ and revert it back after applying $\hat{X}\hat{X}$ operator. Since the phase
errors propagate to the control qubit, if adjacent data qubits contain any phase-flip error, it will change the state of measure-X qubit from $|+\rangle$ to $|−\rangle$, then the last Hadamard gate operation converts it to $|1\rangle$. Therefore, the $X\hat{X}$ operator can be used to detect any phase-flip of the adjacent data qubits.

![Diagram](image)

**Fig. 11** Two CNOT gates in combination with Hadamard gates on the second qubit can detect any phase-flip error of the first and third qubits

In stabilizer formalism, such $X\hat{X}$ and $Z\hat{Z}$ operators are called stabilizers. Knowing the fact that all $\hat{X}$ and $\hat{Z}$ operators on different qubits commute with one another $[X_{Df}\hat{X}_{De}, Z_{Df}\hat{Z}_{De}] = 0$ (Please refer to the black box in Fig. 12), it is possible to measure the phase and amplitude of a two data qubit system simultaneously without perturbing the state of the system. As we know $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$ and $|\rangle = \frac{1}{\sqrt{2}}(|0\rangle − |1\rangle)$ are eigenstates of $\hat{X}$ operator, with eigenvalues +1 and -1, respectively. Considering a two-qubit system, applying $X\hat{X}$ operator to the Bell states $(\frac{1}{\sqrt{2}})(|00\rangle + |11\rangle)$, $(\frac{1}{\sqrt{2}})(|01\rangle + |10\rangle)$, $(\frac{1}{\sqrt{2}})(|00\rangle − |11\rangle)$, and $(\frac{1}{\sqrt{2}})(|01\rangle − |10\rangle)$ results in eigenvalues +1, +1, -1, and -1, respectively. While applying $Z\hat{Z}$ operator to the same set of states results in eigenvalues +1, -1, +1, and -1, respectively.

Table 3 shows the set of the Bell states as eigenstates of $X_{Df}\hat{X}_{De}$ and $Z_{Df}\hat{Z}_{De}$ operators with their corresponding eigenvalues. The eigenvalues for $X_{Df}\hat{X}_{De}$ and $Z_{Df}\hat{Z}_{De}$ are recorded by measuring measure-X and measure-Z qubits labeled Xc and Zb, respectively. Suppose we have initialized the system in the $(\frac{1}{\sqrt{2}})(|00\rangle + |11\rangle)$ state. If an X (bit-flip) error happens on Df data qubit, the new state of the system becomes $(\frac{1}{\sqrt{2}})(|01\rangle + |10\rangle)$. As such, the $X_{Df}\hat{X}_{De}$ and $Z_{Df}\hat{Z}_{De}$ operators show measurement results that change from the pair of eigenvalues (+1, +1) to (+1, -1). Note that, if an X error happens on De, we will get the same result. Consequently, we cannot distinguish which data qubit the error occurred because they both will have the same measurement result. This is true for Z (phase-flip) errors too. Therefore, to uniquely identify errors on specific data qubits, we need to consider a more complex mechanism such as Surface Code [8].
Table 3. The set of eigenstates and corresponding eigenvalues for two-qubit stabilizers $\hat{X}_{Df}\hat{X}_{De}$ and $\hat{Z}_{Df}\hat{Z}_{De}$.

| $\hat{X}_{Df}\hat{X}_{De}$ | $\hat{Z}_{Df}\hat{Z}_{De}$ | $|\psi\rangle$ |
|-----------------------------|-----------------------------|-----------------|
| +1                          | +1                          | $\frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)$ |
| +1                          | -1                          | $\frac{1}{\sqrt{2}}(|01\rangle + |10\rangle)$ |
| -1                          | +1                          | $\frac{1}{\sqrt{2}}(|00\rangle - |11\rangle)$ |
| -1                          | -1                          | $\frac{1}{\sqrt{2}}(|01\rangle - |10\rangle)$ |

In Surface Code, each data qubit is surrounded with 4 measurements qubits while each measurement qubit is surrounded with 4 data qubits as shown in Fig. 12. The measure-Z qubit stabilizes the product of $\hat{Z}$ operators on the surrounding qubits. For example, in Fig. 12, the qubit Zb forces the data qubits Df, De, Dc, and Db to an eigenstate of operator outer product $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$. The measure-X qubit stabilizes the product of $\hat{X}$ operators on the surrounding qubits. In Fig. 12, the qubit Xc forces the data qubits Di, Df, Dh, and De to an eigenstate of operator outer product $\hat{X}_{Di}\hat{X}_{Df}\hat{X}_{Dh}\hat{X}_{De}$. Note the chosen stabilizers $\hat{X}_{Di}\hat{X}_{Df}\hat{X}_{Dh}\hat{X}_{De}$ and $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ must commute with one another to force the projective measurement outcome of the system into a unique eigenstate of all the stabilizers. Table 4 shows the eigenstates of $\hat{X}_{Di}\hat{X}_{Df}\hat{X}_{Dh}\hat{X}_{De}$ and $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ operators with their corresponding eigenvalues.

The order of applying $\hat{X}$ and $\hat{Z}$ on data qubits to realize 4-qubit stabilizers are important. The order must be chosen to ensure that we are not measuring the result of $\hat{X}$ and $\hat{Z}$ operators of any data qubit simultaneously. Failure to keep commutation relationship of neighbor stabilizers results in random measurements [8]. In our example, the order of $\hat{X}$ and $\hat{Z}$ in $\hat{X}_{Di}\hat{X}_{Df}\hat{X}_{Dh}\hat{X}_{De}$ and $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ guarantees that the two stabilizers are commuting as well as the shared data qubits Df and De between the two stabilizer types ($\hat{X}_{Di}\hat{X}_{Df}\hat{X}_{Dh}\hat{X}_{De}$ and $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$) are interacting with one ancilla qubit of a type (Xc or Zb) at a time. This ensures robustness of Surface-17 Code to ancilla errors [35].
Fig. 12 A 2D array of NN qubits forming a Surface Code. The labeled qubits form a logical qubit containing 17 physical qubits, 9 of which are data qubits and 8 of which are measurement qubits. The box shows two data qubits De and Df in green, one measure-Z qubit Zb in blue and one measure-X qubit Xc in orange.

Suppose we have initialized the system in $|0000\rangle$ state. If an X error happens on Df data qubit, measuring the system using $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ stabilizer reports a change from eigenstate $|0000\rangle$ to $|1000\rangle$. Now if an X error happens on De, measuring the system using $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ stabilizer reports a change from $|0000\rangle$ to $|0100\rangle$. As it can be seen in Table 4, a single error in any data qubit can be uniquely specified as the measurement result lands on a specific eigenstate with eigenvalue -1.

Table 4. The set of eigenstates and corresponding eigenvalues for four-qubit stabilizers $\hat{X}_{Df}\hat{X}_{De}\hat{X}_{Dh}\hat{X}_{Dc}$ and $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$. Note $\hat{X}$ and $\hat{Z}$ are Pauli operators acting on the data qubits as shown in Fig. 12 where the measure-X qubit Xc stabilizes $\hat{X}_{Df}\hat{X}_{De}\hat{X}_{Dh}\hat{X}_{Dc}$ operator and the measure-Z qubit Zb stabilizes $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ operator.

| Eigenvalue | $\hat{X}_{Df}\hat{X}_{De}\hat{X}_{Dh}\hat{X}_{Dc}$ | $\hat{Z}_{Df}\hat{Z}_{De}\hat{Z}_{Dc}\hat{Z}_{Db}$ |
|------------|-----------------------------------------------|-----------------------------------------------|
| +1         | $|+++\rangle$                               | $|0000\rangle$                                |
| +1         | $|++-\rangle$                                | $|0110\rangle$                                |
| +1         | $|--+\rangle$                                | $|0101\rangle$                                |
| +1         | $|--\rangle$                                 | $|1111\rangle$                                |
| -1         | $|+++\rangle$                                | $|0001\rangle$                                |
| -1         | $|+-+\rangle$                                | $|0010\rangle$                                |
| -1         | $|--+\rangle$                                | $|0110\rangle$                                |
| -1         | $|--\rangle$                                 | $|1110\rangle$                                |
In this work, our focus is on efficient Surface Code memory realization and in using multi-qubit gates as the building block circuitry. Performing quantum computation in Surface Code is not in the scope of this paper. The interested reader is referred to [8] for further information about Surface Code.

5 Surface Code memory based on parity detector gate

Designing quantum architectures to prevent dephasing as well as error correction schemes to detect and correct phase-flip errors and bit-flip errors are of high interest [1-10]. In section 5.1 and 5.2 we explain how we can use multi-qubit parity detector gates to realize Surface Code error correction.

5.1 Surface Code architecture based on parity detector gate for systems with tunable couplings

The parity detector gates in combination with Identity and Hadamard gates can detect any bit-flip or phase-flip error. Fig. 13 (a) shows one sequence of simultaneous application of bit-flip detectors (columns with purple connections) and phase-flip detectors (columns with red connections) on columns of a Surface-17 Code. Note that all these gate applications are achieved using only single-shot multi-qubits parity detector gates over a 1D array of qubits (each column). When we apply these vertical gates, the horizontal couplings between qubits are turned off. Fig. 13 (b) shows the simultaneous horizontal application of the bit-flip detectors (columns with purple connections) and phase-flip detectors (columns with red connections), while the vertical couplings between qubits are turned off. Since, the $X$ and $Z$ operators on two different qubits always commute, the simultaneous application of parity detector gates of different types on the vertical columns or horizontal rows of a Surface Code 17 is possible. The following shows the proof for simultaneous vertical parity detector gates operations on four columns, similar calculation can be done for the horizontal application of parity detector gates on four rows that results in

$$[X_{Da}X_{Dd}X_{De}X_{Di}, Z_{Db}Z_{Df}Z_{Dg}Z_{Dh}] = 0.$$  

$$[X_{Db}X_{Da}X_{Df}X_{Dh}, Z_{Dc}Z_{Dg}Z_{Dl}] = (X_{Db}X_{Da}X_{Df}X_{Dh})(Z_{Dc}Z_{Dg}Z_{Dl}) - (Z_{Dc}Z_{Dg}Z_{Dl})(X_{Db}X_{Da}X_{Df}X_{Dh}) = (X_{Db}Z_{Dc}X_{Da}Z_{Dg}Z_{Dl}) - (Z_{Dc}X_{Db}Z_{Dg}Z_{Dl}X_{Da}Z_{Df}Z_{Dh}) = 0$$  

(43)
A Surface-17 code in a 2D array of flux qubits with tunable couplings (the lines between qubits) is shown containing 9 data qubits in green, 4 measure-Z qubits in blue, and 4 measure-X qubits in orange. The multi-qubits parity detector gates along with Hadamard operations can be performed by globally applied pulses in two sequences of vertical/horizontal gate applications. In each sequence of vertical (a) or horizontal (b) gate applications, all the blue couplings are turned off, these are the unwanted horizontal/vertical couplings. Both phase-flip and bit-flip of a Surface-17 code can be detected in two sequences of global pulse applications resulting in reduced control circuitry. Note the order of applying these sequences are not important, since the stabilizers don’t share any data qubit simultaneously.

Fig. 14 shows the required gate operations needed to implement a Surface-17 Code error correction cycle. On each sequence, Hadamard gates are applied to measure-X qubits before and after parity detector gates to detect phase-flip errors. However, since the two consecutive Hadamard gates result in Identity operation, in Fig. 14, the pairs of Hadamard gates between vertical and horizontal parity detector operations realizing X stabilizers are removed which results in reducing the depth of cycle from 7 to 5. Therefore, we only need Hadamard gates on measure-X qubits in the beginning and ending of each error detection cycle to detect the phase-flip errors. Also, Identity gates are applied to measure-Z qubits in the beginning and ending of each error correction cycle by simply waiting to compensate the timing of the Hadamard operations on measure-X qubits. To perform the single-qubit Hadamard gates, we must turn off the couplings between the desired qubit and its neighbor qubits.

As depicted in Fig. 14, the circuit has depth of 5 including parity detection operations, the Hadamard gates, and measurements operations. Each global pulse application to realize the multi-qubit parity detector gate takes only 10 ns. We consider 7.1 ns timing period and bias value equal to tunneling (25 MHz) for each single-qubit Hadamard gate operation [32]. The bias value of all control qubits is 3 GHz, the bias value of all target qubits for parity detection is zero for 10 ns. For CNOT gates, the bias on all target qubits equals the coupling value between the control and target qubit for 10 ns. All the qubits are involved in each vertical or horizontal sequence gate operation, therefore, there is no qubit left idle at any time. This
prevents occurrence of dephasing in the system. In each sequence (yellow areas) of an error correction cycle, the gates involved in X stabilizers are depicted in red, while the gates involved in Z stabilizers are depicted in purple.

Note that the total circuit depth of proposed error correction cycle is always 5 regardless of the total size of the Surface Code. This would allow for very large-scale Surface Code architectures with extensively reduced control circuitry.

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**Fig. 14** Quantum circuit of depth 5 for one cycle of error correction in Surface-17 code for systems with tunable couplings. Two sequences (vertical and horizontal) of multi-qubit parity detector gates are required to detect all bit-flip and phase-flip errors. In the figure the required gates regarding X stabilizers are depicted in red, while the required gates regarding Z stabilizers are depicted in purple. All gates are applied to nearest neighbors, on the left the data qubits are green, X-measurement qubits are orange, and Z-measurement qubits are blue. see Fig. 13 to match the cycles. Note that all the gates specified in the pink regions are applied simultaneously, therefore, considering the required Hadamard gate operations and measurement the depth of the circuit is 5.
5.2 Surface Code architecture based on parity detector gates for systems with non-tunable couplings

Although the tunable coupling architectures are very good candidates for error correction schemes and it is easier to perform multi-qubit gates, there are some disadvantages such as the increased circuit complexity and more noise introduction. Therefore, it is valuable to design Surface Code architecture for systems with non-tunable couplings [32, 39-42], where the coupling values will not change during the quantum computation.

In systems with non-tunable couplings, we cannot implement a parity detector operation simultaneously where two neighbor qubits are target qubits since each target qubit must be surrounded by 4 control qubits. These control qubits should have high bias values to preserve their states during gate operation. Therefore, it is not possible to simultaneously realize two vertical/horizontal parity detector gates on two neighbor columns/rows in a 2D Surface Code. The error correction cycle is performed by applying 4 sequences of multi-qubit parity detector gates as shown in Fig. 15 (a), (b), (c), and (d). Note the order of applying these multi-qubit operators is not important, since the stabilizers are configured along the columns or rows and don’t share any data qubit simultaneously. However, we chose an arbitrary order as follows: first a multi-qubit vertical X operator, second a horizontal X operator, third a horizontal Z operator, and fourth a vertical Z operator.

![Fig. 15 (a) Applying multi-qubit X operator on all vertical columns in 2D array of qubits](image-url)
Fig. 15 (b) Applying multi-qubit X operator on all horizontal rows in 2D array of qubits

Fig. 15 (c) Applying multi-qubit Z operator on all horizontal rows in 2D array of qubits

Fig. 15 (d) Applying multi-qubit Z operators on all vertical columns in 2D array of qubits

Fig. 16 shows the required sequence of multi-qubit gates. In Fig. 16, the required gates regarding X stabilizers are depicted in red, while the required gates regarding Z stabilizers are depicted in purple. All gates are applied to nearest neighbors. In Fig. 16, as before, the data qubits are depicted in green, X-
measurement qubits are shown in orange, and Z-measurement qubits are depicted in blue. Compare Fig.
15 and Fig. 16 to match the cycles.

Fig. 16 Quantum circuit of depth 7 for one cycle of error correction in Surface-17 code for systems with non-tunable
couplings. Four sequences (vertical and horizontal) of multi-qubit parity detector gates are required to detect all bit-
flip and phase-flip errors. Note that all the gates specified in the pink regions are applied simultaneously, therefore,
considering the required Hadamard gate operations and measurement the depth of the circuit is 7

Note that we can add/remove arbitrary number of five-qubit parity detector gates to scale up or down
these gates in a larger 2D array of qubits when realizing a large-scale Surface Code memory. For example,
in Fig. 15.d, a 9-qubit vertical parity detector gate is realized with two target qubits Zb and Zc, and control
qubits Db, Dc, Df, De, Dd, Dh, and Dg. The notation for this 9-qubit gate is shown in the last vertical Z
operator (last pink column) in Fig. 16. Since, the 9-qubit vertical parity detector detects only parity of
vertically coupled control qubits Dc versus De, and De versus Dg, to simplify Fig. 16, we did not show the
connection of horizontally coupled control qubits Db and Df connected to target qubit Zb, as well as horizontally coupled control qubits Dd and Dh connected to target qubits Zc.

6 Conclusions

We designed two new multi-qubit parity detector gates for nearest neighbor (NN) architectures with non-tunable couplings. We achieved fidelity of 99.9% for 5-qubit horizontal and vertical parity detector gates. These gates are designed for the physical realization of nearest-neighbor flux qubits inductively coupled to each other. However, the proposed multi-qubit parity detector gates and proposed Surface Code architectures can be applied to other physical realizations. These gates are realized in only 3 sequences of pulse applications, and thus extensively reduce the control circuitry. There are many applications for these new gates, here we proposed the application of these gates in Surface Code scheme for quantum memory realization to detect both bit-flip and phase-flip errors. Furthermore, for nearest neighbor (NN) architectures with tunable couplings, we applied the existing single-shot parity detector gates to realize Surface Code memory.

The advantages of using our proposed Surface Code architectures can be summarized in four main points:

- It extensively simplifies the control circuitry.
- It achieves a much faster error detection cycle. Since the gate operation time is a control parameter, we can reduce the error detection cycle time even more by adjusting the system parameters such as tunneling.
- It is scalable to very large-scale Surface Code architectures and only needs a circuit of depth 5 for any size of 2-Dimensional array of qubits with tunable couplings. And only needs a circuit of depth 7 for any size of 2-Dimensional array of qubits with non-tunable couplings.
- Our method removes the possibility of developing relative phases (dephasing) during idle times, since there are no idle qubits in these schemes.

We considered the Surface-17 code to show how using our proposed multi-qubit parity detector gates greatly reduces the control circuitry complexity. However, investigating new logical qubit layout patterns which are optimized based on multi-qubit gates as building blocks is another topic for future research. For example, in Surface-17 Code scheme for systems with non-tunable couplings, we require to apply four sequences of parity detector gates per each error correction cycle, while CNOT gates (on the borders of Surface-17 logical qubit layout) are performed in parallel with parity detector gates. For our considered
physical realization with non-tunable coupling, the gate time of CNOT gates is longer than the parity detector gates, since for realizing a CNOT gate between two qubits, the interaction of the target qubit with its three other neighbors must cancel out. Thus, for smaller Surface code logical qubit layouts like Surface-17, the use of CNOT gates on the borders increases the cycle time. However, if we consider different logical qubit layout pattern such that we don’t use CNOT gates at all, using presented parity detector gates extensively raises the performance of a large-scale Surface Code architecture.

Note that the experimentalists can realize the parity detector gates proposed in this work by choosing different set of parameters which match with their physical system. They simply can multiply each parameter by a scaling factor such that the conditions explained in section 3.2 remain satisfied [11].

In this work, we considered ideal control pulses to design the new gates. The effect of rise and fall times of non-ideal control pulses as well as the effect of the next to nearest neighbor couplings on the gate fidelity will be future topics of research.
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