Optimizing Huffman Decoding for Error-Bounded Lossy Compression on GPUs

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Abstract—More and more HPC applications require fast and effective compression techniques to handle large volumes of data in storage and transmission. Not only do these applications need to compress the data effectively during simulation, but they also need to perform decompression efficiently for post hoc analysis. SZ is an error-bounded lossy compressor for scientific data, and cuSZ is a version of SZ designed to take advantage of the GPU’s power. At present, cuSZ’s compression performance has been optimized significantly while its decompression still suffers considerably lower performance because of its sophisticated loss-less compression step—a customized Huffman decoding. In this work, we aim to significantly improve the Huffman decoding performance for cuSZ, thus improving the overall decompression performance in turn. To this end, we first investigate two state-of-the-art GPU Huffman decoders in depth. Then, we propose a deep architectural optimization for both algorithms. Specifically, we take full advantage of CUDA GPU architectures by using shared memory on decoding/writing phases, online tuning the amount of shared memory to use, improving memory access patterns, and reducing warp divergence. Finally, we evaluate our optimized decoders on an Nvidia V100 GPU using eight representative scientific datasets. Our new decoding solution obtains an average speedup of 3.64× over cuSZ’s Huffman decoder and improves its overall decompression performance by 2.43× on average.

I. INTRODUCTION

High-performance computing (HPC) applications are generating increasingly large amounts of data. For example, Hardware/Hybrid Accelerated Cosmology Code (HACC) is a cosmological simulation package designed for HPC environments. For HACC simulations consisting of trillions of particles, one snapshot of the simulation takes up 220 TB of data, while an entire simulation run can take up 22 PB of data [12]. Another such application is the pruning and compression of deep neural networks, which are becoming deeper and wider, and therefore larger, as computing capacity is increasing and deep neural networks are becoming more widely used [18]. However, leading supercomputers such as Summit [56], have limited storage capacities of approximately 50∼200 PB to share between hundreds of users. Thus, these applications require data reduction techniques that attain both high performance and high compression ratios. SZ, for instance, is a lossy data compressor that aims to achieve these goals. It offers over a 2x increase in compression ratio over state-of-the-art compressors. Furthermore, it allows users to specify how much error they wish to tolerate in their data and allows them to make a tradeoff between data distortion and compression ratios [37].

As a result of the evolution of supercomputer architecture (e.g., more powerful GPUs on a single node), many HPC applications are being implemented on graphics processing units (GPUs) due to their high performance and parallelism. For example, a recent study of cosmological simulations on the Summit supercomputer [33] shows a significant performance improvement compared to prior work without using GPUs [13]. However, even ignoring the time to transfer the uncompressed data from the GPU to the CPU, CPU-based lossy compressors would still cause more than 10% overhead of the overall performance, which would limit the I/O performance gain by lossy compression, according to prior studies [37,19]. Thus, several lossy compressor development teams have recently released their GPU versions to reduce the compression overhead. These GPU versions can both accelerate the compression computation and reduce the time needed to transfer the data between the GPU and CPU after the compression. For example, both SZ and MGARD [1] have a GPU adaptation (known as cuSZ [39] and cuMGARD [5]), which have been implemented for GPU hardware, and more specifically Nvidia’s CUDA platform.

Furthermore, an important use case of lossy compression is to reduce the memory footprint by storing the data in the compressed format and calculating from the lossy data in memory [4]. Compared to the amount of data handled in extreme-scale applications, memory is scarce on HPC systems. Lossy compression can be introduced to ease this pressure in applications that can tolerate some loss of fidelity in their working data. An example of in-memory compression is Wu et al.’s work on quantum circuit simulation [43], where in-memory compression reduced the total memory usage on 4,096 nodes from 32 exabytes to 768 terabyte. This compression allowed for 2∼16 more qubits to be simulated than if no compression was used. Another example is Jin et al.’s work on reverse time migration (RTM) simulation [17], where in-memory compression reduced the memory usage by about 10× on average. Moreover, for some applications, in-memory compression can decrease repetitive computations and accelerate execution [4]. For example, Gok et al.’s work on quantum chemistry simulation—GAMESS [10]—proposes to calculate, compress, and write each unique data block of two-electron integrals into the memory once; and whenever a block is needed again in simulations, it is read from the memory and decompressed. Compared with the original
GAMES, where all blocks are generated and consumed by the simulation on the fly and are then deleted from the memory. Gok et al.’s approach achieves a reduction in the block recomputation costs. Note that all these computations should be done at runtime because integral blocks are generated and consumed repeatedly during a simulation. Consequently, in-memory (de)compression throughputs are critical to the overall performance. To this end, in this work, we focus on improving decompression throughputs on GPUs without considering GPU-to-CPU data-movement overheads, as decompressed data do not need to be transferred to CPUs or disks.

An important component of both cuSZ and cuMGARD is Huffman coding, a classic lossless compression technique initially developed by David Huffman in 1952 [14]. Tian et al.’s work proposes an optimized Huffman encoder for GPUs [40]; their work has been applied to improve cuSZ’s compression throughput. Although efficient compression is important to speedup the overall data movement, efficient decompression is also important to enable fast and effective post-analysis based on compressed data. However, Huffman decoders used by error-bounded lossy compressors currently employ only a limited degree of parallelism and do not fully exploit the GPU’s power. Two state-of-the-art works propose improved Huffman decoding on the GPU: one of these works, Weißenberger and Schmidt’s [42], uses the self-synchronization property of Huffman codes to extract greater parallelism, while the other work, Yamamoto et al.’s [45], proposes a new data structure called a gap array to extract greater parallelism. But both works suffer from two main issues: (1) they do not fully take advantage of the GPU architecture for performance optimization, and (2) they must be adapted for use in error-bounded lossy compression.

To facilitate their efficient use in scientific data compression, we explore both Huffman decoding algorithms in depth. Furthermore, we identify opportunities for deep optimization of both algorithms based on GPU architecture considerations. Finally, we adapt both algorithms for use in error-bounded lossy compression such as cuSZ, and then evaluate them on eight representative scientific datasets. The contributions of our work are summarized as follows:

- We analyze Weißenberger and Schmidt’s and Yamamoto et al.’s algorithms in depth by evaluating their performance on scientific datasets and understanding their tradeoffs.
- We perform a deep architectural optimization for both Huffman decoding algorithms by using shared memory in the decoding and writing phase, improving memory access patterns, and reducing warp divergence.
- We propose an efficient approach to online tune the amount of shared memory used to decode different parts of the data based on the data characteristics.
- We adapt our optimized decoders to multi-byte data for cuSZ and evaluate them on eight scientific datasets. Experiments show our solution can improve decoding throughput by $3.64 \times$, compared with cuSZ’s naive decoder, and can improve cuSZ’s overall performance by $2.43 \times$, on average.

In §III, we present background information about scientific data compression, Huffman coding, and GPU-based lossy compression. In §IV we discuss both Weißenberger and Schmidt’s and Yamamoto et al.’s Huffman decoding algorithms in detail, comparing them and discussing their limitations. In §V we describe our architectural optimizations for efficient Huffman decoding, as well as our adaptations to enable decoding of scientific datasets. In §VI we show the experimental evaluation results on scientific datasets. In §VII and §VIII we discuss the related work and conclude our work.

II. BACKGROUND

A. Scientific Data Compression

Scientific data compression has been studied for decades and categorized into two types of compression: lossless compression and lossy compression. Lossless compressors such as FPZIP [29] and FPC [3] keep the data intact but can only provide a compression ratio of about $2 \times$ on scientific data [35]. Lossy compression, on the other hand, can compress data beyond lossless compression (typically one or more orders of magnitude) but introduces information loss in the reconstructed data. In recent years, a new generation of high accuracy lossy compressors for scientific data have been proposed and developed for scientific floating-point data, such as SZ [8, 37, 25], ZFP [28], and MGARD [1]. These lossy compressors provide parameters that allow users to finely control the information loss introduced by lossy compression. Unlike traditional lossy compressors such as JPEG [41] for images (in integers), SZ, ZFP, and MGARD are designed to compress floating-point data and can provide a strict error-controlling scheme based on the user’s requirements. Generally, lossy compressors provide multiple compression modes, such as error-bounding mode and fixed-rate mode. Error-bounding mode requires users to set an error type, such as the point-wise absolute error bound and point-wise relative error bound, and an error bound level (e.g., $10^{-3}$). The compressor ensures that the differences between the original data and the reconstructed data do not exceed the user-set error bound level. Fixed-rate mode means that users can set a target bit-rate (the number of bits to represent each data point), and the compressor guarantees the actual bit-rate of the compressed data to be lower than the user-set value.

B. Huffman Coding

Huffman Coding is a classic technique developed by David Huffman in 1952 for performing lossless compression [14]. It encodes a fixed-length value as a variable-length code. We call the fixed-length input value an input symbol, and we call the variable-length output value a codeword. In Huffman coding, space savings result from the fact that more frequently occurring symbols are represented by codewords with fewer bits, and vice versa for less frequently occurring symbols. Huffman codewords are also prefix-free; no one codeword can be a prefix of any other codeword.

C. CUDA Architecture

Thread: The thread is the basic programmable unit that allows programmers to use massive numbers of CUDA cores.
CUDA threads are grouped at different levels including warp, block, and grid.

Warp: The warp is a basic-level scheduling unit in CUDA associated with SIMD (single-instruction multiple-data). Specifically, the threads in a warp achieve convergence when executing exactly the same instruction; otherwise, warp divergence happens. In the current CUDA architecture, the number of threads in a warp is 32, hence, it works as 32-way SIMT when converging. However, when diverging happens, diverged threads add extra overhead to the execution.

Block: Unlike the warp, the thread block (or simply block) is a less hardware-coupled description of thread organization, as it is explicitly seen in the kernel configuration when launching one. Threads in the same block can access the shared memory, a small pool of fast programmable cache. On one hand, shared memory is bound to active threads, which are completely scheduled by the GPU hardware; however, on the other hand, a grid of threads may exceed the hardware-supported number of active threads at a time. As a result, the data stored in the shared memory used by the previous batch of active threads may be invalid when the current or following batch of active threads are executing. Thus, we must carefully tune the shared memory size for different workloads toward high performance.

Grid: A grid encompasses the entire set of blocks that are launched as part of a CUDA kernel. Usually, the grid of threads describes either the entire problem or a working set of the problem at hand. Moreover, all the blocks within a grid share a common configuration; each block within a grid contains the same amount of shared memory and the same number of threads per block.

D. Error-bounded Lossy Compression on GPU

SZ, ZFP, and MGARD were first developed for CPU architectures, and all started rolling out their GPU-based lossy compression recently. The SZ team, the ZFP team, and the MGARD team released their CUDA versions, called cuSZ [39], cuZFP [7], and cuMGARD [5], respectively. All the versions provide much higher throughputs for compression and decompression compared with their CPU versions [39, 19, 38].

Nevertheless, since GPUs have so many cores, we can improve performance by proposing a fine-grained solution—a solution that launches many threads that operate on fewer data elements.

It is possible to extract greater parallelism from cuSZ’s existing coarse-grained Huffman decoder by decreasing the size of each chunk; however, since Huffman codes are variable length, very small chunks may not be able to be filled, leaving empty space in chunks that degrade the compression ratio. One avenue for increasing the parallelism in Huffman decoding is to determine a starting point in the bitstream for each thread; two connected strategies for doing this are described in the following subsections.

B. Self-Synchronization Based Huffman Decoding

Weißenberger and Schmidt proposed a parallel algorithm for Huffman decoding on the GPU using a property of Huffman codes called self-synchronization [42]. Their technique is in turn based on an earlier CPU-based parallel Huffman decoder by Klein and Wiseman [22]. This algorithm is designed to work on pure Huffman codes; no modifications to the Huffman encoding step need to be done. It uses the self-synchronization property of Huffman codes to determine where in the bitstream each thread starts decoding, allowing for finer-grained parallelism than a chunk-based approach.

1) Self-Synchronization: The self-synchronization property of Huffman codes is the tendency for a Huffman decoder to correct itself even if a few bits of the input were skipped in error [9]. An example of self-synchronization is as follows: consider the bit pattern ‘111000001111000’ with the Huffman codebook from [9], shown in Listing 1. A correct decoding of this pattern is ‘(11)(10)(00)(010)(11)(10)(00)’, or ‘CBADCBA’. However, if one bit is skipped in the input, then the pattern is decoded as ‘(11)(00)(00)(10)(11)(10)(00)’, or ‘CAABCA’. The first four characters’ outputs are incorrect, but after decoding four erroneous characters (8 bits), the decoder starts decoding the correct characters, i.e., it self-synchronizes.

Listing 1: Example self-synchronizing codebook from [9].
In turn is divided into UNITS sequence that a single CUDA thread works on. A subsequence to understand the steps of the above algorithm, we define a described as follows:

- Each thread decode data, starting at a synchronization point, and write it to the output array.
- Use self-synchronization to determine the synchronization points within each sequence;
- Use self-synchronization to adjust the synchronization points between sequences;
- Use a prefix sum to determine where each thread writes to in the output array;
- Have each thread decode data, starting at a synchronization point, and write it to the output array.

To understand the steps of the above algorithm, we define a SEQUENCE to be a chunk of the input data that a single CUDA thread block operates on. A subsequence is a subdivision of a sequence that a single CUDA thread works on. A subsequence in turn is divided into UNITS: unsigned 32-bit numbers that contain the individual codewords. The number of synchronization points within a given dataset is equal to the number of subsequences in the input data. Steps 1 and 2 ensure that all the synchronization points reference valid codewords. During this process, the number of valid codewords in each subsequence is recorded. These numbers are then prefix-summed in step 3 to determine the first output index for each subsequence. Finally, in step 4, each thread starts decoding at its synchronization point and outputs data starting at the index generated by the prefix sum. We refer readers to [42] for more details.

Limitation: Although the self-synchronization based Huffman decoding allows for finer-grained Huffman decoding, it contains some major performance bottlenecks. One major bottleneck is determining synchronization points; to do this, the algorithm needs to decode the input data multiple times depending on the particular dataset to be decoded.

C. Gap Arrays

To address the self-synchronization’s performance issue, Yamamoto et al. work proposed a new data structure called a gap array to eliminate this decoding bottleneck, in exchange for some extra encoding overhead [45]. Note that although the work also proposes an optimized encoding scheme, our main focus is its decoding scheme. Similar to Weißenberger and Schmidt’s algorithm, Yamamoto et al.’s decoder divides its input data into sequences, subsequences, and units as defined above. However, instead of finding out where each thread starts decoding within a subsequence by determining synchronization points, this information is stored alongside the compressed data in a gap array. A GAP ARRAY is a byte array, with one byte per subsequence, that indicates to each thread how many bytes it must skip before accurate data can be decoded. For example, a gap array for the codewords in Figure 1 would be [0, 0, −2, −1], as these are the offsets from the subsequence boundaries that each thread would have to keep track of in order to decode correctly. The gap array is used in combination with a technique called Single Kernel Soft Synchronization (SKSS) to determine output indices, decode the codewords, and write output symbols to memory. We refer readers to [45] for more details.

Limitation: Although the gap array reduces the necessity of performing the self-synchronization phase and speeds up the decoding, gap arrays introduce other overheads. These overheads include the extra space required to store the gap array as well as extra work for the encoder. Nevertheless, the extra space required to store a gap array is minimal, as Yamamoto et al. has shown that the size of the gap array is less than 3% of the size of the data on their tested datasets of varying compression ratios [45]. However, the extra work the encoder must perform in generating the gap array means that the encoder and the decoder must be coupled. This reduces the flexibility of gap-array-based Huffman decoding, as it will not be able to decode Huffman codes generated by encoders not designed to create gap arrays. Nevertheless, since there are compelling reasons to use both self-synchronization and gap arrays in practice (will be discussed in detail in §V-C), we consider both solutions in our optimization work.

D. Challenges of Using Existing Huffman Decoders

Both Weißenberger and Schmidt’s and Yamamoto et al.’s works have been evaluated across a wide range of general-purpose datasets [42, 45]. However, in error-bounded lossy
as well as in our online repository. Details of the decoders can be found both in this subsection and (2) the decoding and writing phase (i.e., Step 4), for both (i.e., Step 1), for self-synchronization based Huffman decoding; current algorithm: (1) the intra-sequence synchronization phase by input. We continue by examining the bottlenecks in the Schmidt’s implementation as a baseline and adapt it to multi-
structural optimizations on both Weißenberger and Schmidt’s and Yamamoto et al.’s solutions. We start with Weißenberger and Schmidt’s implementation as a baseline and adapt it to multi-byte input. We continue by examining the bottlenecks in the current algorithm: (1) the intra-sequence synchronization phase (i.e., Step 1), for self-synchronization based Huffman decoding; and (2) the decoding and writing phase (i.e., Step 4), for both self-synchronization and gap-array-based Huffman decoding. Details of the decoders can be found both in this subsection as well as in our online repository.

IV. DESIGN METHODOLOGY

To allow efficient Huffman decoding of multi-byte input such as quantization codes in cuSZ, we perform a series of architectural optimizations on both Weißenberger and Schmidt’s and Yamamoto et al.’s solutions. We start with Weißenberger and Schmidt’s implementation as a baseline and adapt it to multi-byte input. We continue by examining the bottlenecks in the current algorithm: (1) the intra-sequence synchronization phase (i.e., Step 1), for self-synchronization based Huffman decoding; and (2) the decoding and writing phase (i.e., Step 4), for both self-synchronization and gap-array-based Huffman decoding. Details of the decoders can be found both in this subsection as well as in our online repository.

A. Optimized Self-Synchronization

We note that although the average behavior of self-synchronization is well-predictable, the amount of data each thread needs to decode to achieve self-synchronization can vary, as aforementioned. More severely, although each thread needs to decode only two subsequences on average to find and validate a synchronization point, up to 5% of threads decode greater than two subsequences, and individual threads can decode up to 125 subsequences on the test datasets in order to find and validate synchronization points. As a result, the local unpredictability of self-synchronization hinders GPU implementation because if one thread decodes more subsequences than other threads in the same CUDA warp, the other threads are held up until the longest-running thread finishes its job. This inefficiency is exacerbated by the fact that, in the self-synchronization phase, a CUDA block-wide thread barrier is required for correctness. Thus, the longest-running thread determines the running time of the entire block; and other threads within a block remain idle.

A potential solution to this issue is to perform load balancing to ensure that threads in a block are not idle; however, due to the overhead of load balancing and the relatively low occurrence of exceptionally long-running threads, we do not pursue the load balancing approach. Instead, we do optimize the intra-sequence self-synchronization kernel to minimize the impact of long-running threads and conform more closely to the CUDA architecture. Specifically, in the original code for self-synchronization based Huffman decoding, after each thread discovers and validates a synchronization point, it busy-waits not only until the longest-running thread in the thread block finishes but also until the maximum possible number of subsequences that a thread may decode until self-synchronization is reached (e.g., 128 subsequences in this case). To allow thread blocks to exit as early as possible, we record each thread’s “finished” status in a Boolean variable. By using the CUDA warp primitive __all_sync, we can determine whether all the threads have finished finding their synchronization points; and if so, we will terminate the kernel immediately, freeing up warps within a CUDA Streaming Multiprocessor to execute other blocks in the kernel. This optimized intra-sequence self-synchronization runs, on average, 11% faster than the baseline code, and these benefits are concentrated in lower compression ratio datasets, in which this phase is a more significant bottleneck than in high compression-ratio datasets.

B. Optimized Decoding and Writing of Codewords

In both presented decoders, threads decode and write code-words directly to the GPU’s global memory. There is a stride between different threads’ output indices; this stride reflects the number of codewords that can be found between the two threads’ input locations. This counters one of the characteristics of CUDA’s memory architecture: coalesced memory loads and stores. Specifically, a coalesced memory access is when sequential global memory transactions are combined with each other to reduce the number of memory transactions actually performed. For example, in CUDA, a 32-thread warp writing 32-bit values to sequential locations in memory have its write requests processed as a single 128-byte transaction. Note that inefficient memory access patterns result in many more transactions being made, which decreases the throughput of the global memory.

For high compression-ratio datasets, this memory inefficiency is even worse, because not only are the gaps between adjacent threads’ output indices large, but also the number of values written to global memory, and hence the number of transactions are large. This is a significant factor in the dramatic drop in performance with high compression-ratio datasets

Fig. 2: Decoding performance versus error bounds on HACC dataset. Note that the larger the error bound, the larger the compression ratio. compression such as cuSZ, since input data are quantization codes, the resulting quantization codes are often highly compressible, especially in a well-predicted dataset. Our experiments show that both their works underperform on high-compressible datasets, as can be seen in Figure Note that in general, as error bound increases, the resulting quantization codes become easier to compress. The figure illustrates a drop in the throughput of both decoders as data becomes more easily compressible. Thus, not only do we optimize both their solutions in general, but we also specifically focus on techniques to optimize high compression-ratio cases commonly seen in scientific data reduction.
Algorithm 1: Decoding and writing using a shared memory buffer.

```plaintext
● DecodeWrite — decode and write using shared memory
1 sharedBuffer[n]  [The shared memory buffer of size n]
2 si ← outIndex[blockIdx.x • blockDim.x]
3 ei ← outIndex[(blockIdx.x + 1) • blockDim.x]
4 gid ← threadIdx.x + blockDim.x • threadIdx.x
5 tempEnd ← ei
6 while si < ei do
7 start ← outIndex[gid] - si, end ← outIndex[gid + 1]
8 if si ≤ start and end ≤ si + n then
9 outArray[start ... end] ← Decode(inArray, startPoint[gid])
   [If symbols can fit into the buffer, decode them]
10 else if start < si + n and end ≥ si + n then
11 tempEnd ← outIndex[gid]
   [Executed by one thread if buffer is not large enough; results in another iteration]
12 end if
13 outArray[si ... tempEnd] ← sharedBuffer[0 ... tempEnd - si]
14 si ← tempEnd
15 end while
```

To solve this issue, we propose to first decode the input data into a thread block-local buffer, and then write it out sequentially to global memory to attain coalesced and hence efficient writes. For the thread block-local buffer, we use shared memory. Specifically, first, given the global output index of each thread, the kernel will compute the local index where each thread will put the decoded symbol within the shared memory buffer. Then, the kernel will decode and have each decoder write its data into the shared memory. Finally, all threads in the thread block cooperatively write the data in the shared memory to the global memory output array. Note that the codebook that is used for decoding is kept in global memory; since this codebook is shared across all thread blocks, it is kept in cache, so we do not need to consider keeping a codebook in shared memory and can dedicate the shared memory for the decoding buffer. Note that if the shared memory is not large enough to store all the data that threads inside the block will decode, that the shared memory will be filled up with the initial chunk of decoded data by the initial group of threads, that data will be written, and then the rest of the threads will fill up the shared memory with the rest of the decoded data. More details about this procedure can be found in Algorithm 2.

Algorithm 2: Our proposed shared memory optimization that partitions input sequences among kernels launched with different amounts of shared memory. Lines implemented by host code are in blue, while lines implemented by CUDA kernels are in red.

```plaintext
● ShmemOptDecodeWrite — decode and write with optimal shared memory size
1 compRatio[n]  [The precomputed compression ratios of the n sequences]
2 for all i in [0 ... n) concurrently do
3 compClass[i] ← ClassifyCPR(compRatio[i])
4 end for
5 compClassFreq ←getParam(compClass)
6 compIndex ← [0, 1, ..., n - 1]
7 for i in [0 ... T.high + 1) do
8 compClassStart[i] ← 0
9 for i in [1 ... T.high + 1) do
10 compClassStart[i] ← compClassStart[i - 1] + compClassFreq[i - 1]
11 end for
12 for all i in [0 ... T.high + 1] asynchronously do
13 DecodeWrite(optShmem(i), compClassStart[i], compClassFreq[i])
14 end for
```

We now give more details about this strategy, which are illustrated in Algorithm 2. First, this strategy requires each sequence’s compression ratio as input. This is taken from an earlier phase of each algorithm: the self-synchronization phase for Weißenberger and Schmidt’s algorithm and redundant decoding in Yamamoto et al.’s algorithm required to determine where each thread writes its data. After this is done, (1) the shared memory optimization starts by classifying each
sequence’s compression ratio into \( T_{high} + 1 \) groups, where \( T_{high} \) is an architecture-specific threshold, on lines 2-4. This classification is then stored inside an on-device array, \( T_{high} \) of these groups are the compression ratios in the intervals \((0, 1], (1, 2], \ldots, (T_{high} - 1, T_{high}], \) and the \( T_{high} + 1 \)-th group encompasses compression ratios in the interval \((T_{high}, 16]\). Thus, at most \( T_{high} + 1 \) different kernels with varying amounts of shared memory are launched. (2) The array is then histogrammed on the GPU, in order to see how many sequences fall into each compression ratio group. The algorithm used is the same variation of Gómez-Luna et al. \([11]\) that is used in cuSZ. (3) Once the classification array is histogrammed, on line 5, it is then sorted on the GPU as part of a key-value sort, with the classification being used as the key and a sequential list of indices being used as the values. The resulting values will be the primary means by which sequences in a particular compression ratio group are accessed and decoded. The algorithm used is the DeviceRadixSort routine in CUB \([39]\). Furthermore, since \( T_{high} \) is fairly small, sorting \( T_{high} + 1 \) fast is using CUB (will be proved in Table I). (4) After being transferred back to the CPU, the histogram is then used to generate a prefix sum that indicates where in the list of indices the sequences belonging to that compression ratio group begin. (5) Finally, up to \( T_{high} + 1 \) kernels are launched with an amount of shared memory (mostly) proportional to their corresponding compression ratio group’s upper bound. For example, sequences in the \((3, 4]\) compression ratio group would be decoded by a kernel with a shared memory buffer of length 4096. Each kernel is launched on a separate CUDA stream in order to allow the CUDA driver maximum flexibility in scheduling and running \( T_{high} + 1 \) kernels. These kernels then finish decoding the data and write their data to the output array.

### Table I: Comparison between our shared memory optimization and brute-force search for decoding and writing

| Platform   | NVIDIA HACC | EXAALT | CESM | Nya | HURR | QMC | RTM | GAMESS |
|------------|-------------|--------|------|-----|------|-----|-----|--------|
| tuned GB/s | 1071.9      | 991.7  | 642.7| 642.6| 565.9| 565.1| 571.8| 570.8  |
| % diff. from tuned | 1.4%       | -2.5%  | -15.1%| 1.7%| 1.5%| -0.3%| -0.4%| -2.9%  |
| best brute-force GB/s | 235.5      | 212.2  | 173.8| 174.6| 152.2| 214.9| 173.7| 146.6  |
| shared memory buffer size | 5240 | 5048 | 5632 | 5042 | 5042 | 5042 | 5042 | 5042 |
| % diff. from tuned | 8.5%        | -0.5%  | -6.5%| 3.0%| 3.3%| 1.1%| 10.3%| 6.7%|
| worst brute-force GB/s | 157.2     | 159.9  | 117.8| 92.1| 92.4| 131.3| 88.6| 88.9  |
| shared memory buffer size | 5042 | 5042 | 5042 | 5042 | 5042 | 5042 | 5042 | 5042 |
| % diff. from tuned | 17.5%       | 6.3%   | -0.7%| 1.2%| 2.8%| 2.4%| 4.0%| 3.8%|
| tuning speed GB/s | 20723 | 11268 | 14713 | 10979 | 13474 | 12894 | 6498 | 30619 |
| tuned GB/s | 197.3 | 194.0 | 166.8 | 126.6 | 127.4 | 160.1 | 101.4 | 119.0 |
| % diff. from tuned | 23.0% | 17.8% | 24.9% | 27.5% | 27.5% | 22.2% | 14.9% | 25.3% |
| % diff. from worst case | 20.3% | 17.8% | 29.4% | 27.3% | 27.5% | 22.2% | 14.9% | 25.3% |

Note that in order to prevent a large reduction in occupancy caused by allocating too much shared memory, there is a threshold up to which we can allocate an amount of shared memory proportional to the compression ratio: this threshold is called \( T_{high} \), as aforementioned. To attain \( T_{high} \) for a particular GPU architecture, calculate the amount of shared memory required to attain at least 25% occupancy, and divide that amount by 16384 bytes to attain that level of occupancy, so the corresponding value of \( T_{high} \) is 8. If the compression ratio exceeds \( T_{high} \), our experiments have demonstrated that 3584 symbols are an optimal size for the buffer in most situations on the V100 GPU.

### V. PERFORMANCE EVALUATION

In this section, we present our experimental setup (including platforms, baselines, and datasets) and our evaluation results.

#### A. Experiment Setup

1) **Evaluation Platforms:** We conduct our experimental evaluation on the Bridges-2 supercomputer \([2]\) at Pittsburgh Supercomputing Center (PSC), of which each GPU node is equipped with two Intel Xeon Gold 6248 CPUs and eight 32 GB NVIDIA Tesla V100 GPUs.

2) **Comparison Baselines:** We compare our optimized Huffman decoding with multiple baselines. Specifically, we compare our solution with (1) the original self-synchronization-based Huffman decoder \([42]\), (2) the original gap-array-based

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3Note that in order to achieve maximum throughput, different sections must be decoded with different amounts of shared memory.
Huffman decoder [45], and (3) cuSZ’s naïve Huffman decoder [15] cannot be adapted to multi-byte inputs due to a bug, we estimate its performance by trimming each multi-byte quantization code to a single byte, considering most quantization codes are concentrated in the middle.

Table II: A comprehensive evaluation of all proposed decoding solutions on V100: Huffman decoders using cuSZ quantization codes generated with a relative error bound of 0.03 on V100. GB/s is computed relative to the size of the generated quantization codes, i.e., half the dataset size.

| Techniques                  | HACC | EXAALT | CSEM | Mys | Hurr | QMC | RTM | GAMESS |
|-----------------------------|------|--------|------|-----|------|-----|-----|--------|
| Compression ratio           | in subblocks | data, because the current cuSZ only works with single-precision verified by truncating and decoding the HACC dataset, datasets portion of the total available memory. However, as we have where the datasets to be compressed often take up a significant scientific applications, especially in in-memory applications where the datasets to be compressed often take up a significant portion of the total available memory. However, as we have verified by truncating and decoding the HACC dataset, datasets as small as 10 MB can exhibit speedups over the baseline cuSZ decoder. In addition, the datasets tested are all single-precision data, because the current cuSZ only works with single-precision data. However, since our underlying optimizations work on Huffman decoding of multibyte symbols, our technique applies to double-precision data as well.

B. Experimental Results

1) Huffman Decoding: Table IV illustrates the compression ratios of our optimized decoders and the baselines on the test datasets. We note that the differences between the compression ratios of different methods are up to around 10%. Thus, compression ratio is not the primary factor for choosing the most appropriate Huffman decoding approach; by comparison, throughput is more important. Note that, although the "original gap-array" row in Table IV refers to an 8-bit decoder, we double the compression ratio, so it can be used as a baseline for comparison with 16-bit decoders.

Table III: Real-world float-type datasets used in the evaluation.

| Datasets                  | Data size | #Fields | Examples(s) |
|---------------------------|-----------|---------|-------------|
| HACC                      | 1,071.7 MB| 3,600   |             |
| molecular dynamics        | 951.7 MB  | 1,071   |             |
| EXAALT                    | 233.6 MB  | 64,000  |             |
| CSEM-ATM                  | 26 MB     | 512     |             |
| Nyx                       | 512 MB    | 512     |             |
| Hurricane                 | 10 MB     | 4,000   |             |
| Quantum circuits          | 64 MB     | 100     |             |
| QMCPack                   | 115 MB    | 100     |             |
| Petroleum exploration     | 100 MB    | 100     |             |
| RTM                       | 449 MB    | 449     |             |
| GAMESS                    | 306 MB    | 306     |             |

Table IV: Compression ratio of eight evaluated methods. The original gap-array-based Huffman decoding method in GB/s, their compression ratios are doubled to provide a fair comparison.

| Techniques                  | HACC | EXAALT | CSEM | Mys | Hurr | QMC | RTM | GAMESS |
|-----------------------------|------|--------|------|-----|------|-----|-----|--------|
| Compression ratio           | in subblocks | data, because the current cuSZ only works with single-precision verified by truncating and decoding the HACC dataset, datasets portion of the total available memory. However, as we have where the datasets to be compressed often take up a significant scientific applications, especially in in-memory applications where the datasets to be compressed often take up a significant portion of the total available memory. However, as we have verified by truncating and decoding the HACC dataset, datasets as small as 10 MB can exhibit speedups over the baseline cuSZ decoder. In addition, the datasets tested are all single-precision data, because the current cuSZ only works with single-precision data. However, since our underlying optimizations work on Huffman decoding of multibyte symbols, our technique applies to double-precision data as well.

On the other hand, Table V shows the throughput of each decoded method in GB/s. The average speedup of our optimized self-synchronization solution compared to the baseline (in this case cuSZ’s decoder) is 2.74×, and the average speedup of our optimized gap-array solution is 3.64×. Note that the speedup over the original implementations of self-synchronization and gap-array solutions is more notable on high compression-ratio datasets. This is because the original implementations do not write out symbols to global memory in an efficient manner which is in turn exacerbated by the fact that high compression-ratio datasets have more symbols to be written out to memory. This underscores the importance of the optimizations for efficient memory access and use of shared memory introduced in §IV-B especially when considering quantization codes generated by effective prediction methods. Note further that the original gap-array solution, although its GB/s numbers are computed relative to 8-bit quantization codes, still achieves performance numbers that are greater than our optimized self-synchronization solution. Nevertheless, in addition to the practical reasons detailed above, that solution...
also exhibits the same performance issues on high compression-ratio datasets described earlier.

As a result, the baseline cuSZ decoder has a relatively high compression-ratio input that other finer-grained decoders have. But this is compensated by performance gains elsewhere while decoding a high compression-ratio dataset.

We note that our optimized decoder achieves the lowest speedup relative to the baseline (1.55× and 2.07×) on the Nyx quant dataset. This can be explained by examining both the dataset and the baseline cuSZ decoder: (1) The Nyx dataset is extremely high-compressible, and the encoded Nyx dataset consists mostly of codewords of length one. Since cuSZ’s decoder works one bit at a time, it is able to decode more codewords. (2) Since fewer threads run on cuSZ’s coarse-grained decoder, it does not encounter the same issues with high compression-ratio input that other finer-grained decoders have. As a result, the baseline cuSZ decoder has a relatively high performance on the Nyx dataset compared to the other datasets.

2) cuSZ Decompression: Figure 4 demonstrates the impact of our optimized decoders on the overall performance of cuSZ’s decoder, by comparing the baseline decoder and our two optimized solutions. On average, substituting the baseline decoder with our optimized decoders resulted in 2.08× faster decompression using self-synchronization and 2.43× faster decompression using gap arrays. Note that in this scenario, we calculate GB/s with regard to the size of the scientific dataset itself rather than just the quantization codes. The reason that such a significant speedup can be attained is that cuSZ spends a substantial amount of time doing Huffman decoding; in the HACC dataset, cuSZ spent over 83% of the overall decompression time doing Huffman decoding. As a result, with our optimized decoders, the optimized cuSZ can decode at speeds of over 100 GB/s on the V100 on most of the test cases.

Additionally, in many GPU applications, compressed data is retained on CPU memory, which is a larger resource than GPU memory. When data is needed for processing on the GPU, before decompression, compressed data must be transferred from CPU memory to GPU memory. Thus, in Figure 5 we incorporate host-to-device “memcpy” into our evaluation. In this case, our optimized decompression performed, on average, 1.53× faster for self-synchronization and 1.65× faster for gap arrays over the cuSZ baseline. These speedups are lower than the results shown in Figure 4 as data transfers are a bottleneck due to a relatively slow bandwidth between the GPU and the CPU. Further note that the datasets with a relatively high throughput are those with a high compression ratio; this is because there is less actual data being transferred, so the compressed data transfer is relatively fast for those datasets.

C. Use-case of Our Two Decoders

In this paper, we introduced two algorithms from the literature for fast parallel Huffman decoding and implemented deep optimizations for these two algorithms. Although both approaches are designed for fine-grained parallel Huffman decoding, and both approaches benefit from our architectural optimizations with regard to shared memory and decoding,

### TABLE V: Decoding throughputs of eight evaluated methods.

| Method                | HACC  | EXAALT | CESM  | Nyx  | Hurr. | QMC. | RTM  | GAMESS |
|-----------------------|-------|--------|-------|------|------|------|------|--------|
| baseline cuSZ decoder | 26.4  | 26.1   | 25.2  | 50.2 | 24.8 | 23.7 | 28.8 | 37.0   |
| 1.00×                  | 1.00× | 1.10×  | 1.00× | 1.00×| 1.00×| 1.00×| 1.00×| 1.00×  |
| ori. self-sync         | 39.7  | 40.9   | 6.8   | 6.8  | 35.1 | 9.6  | 5.9  | 5.9    |
| 1.50×                  | 1.57× | 1.27×  | 0.99× | 0.99×| 1.48×| 0.53×| 0.18×| 0.18×  |
| opt. self-sync         | 83.0  | 71.5   | 101.9 | 92.1 | 78.1 | 63.1 | 64.8 | 87.3   |
| 3.14×                  | 2.74× | 4.05×  | 1.55× | 1.55×| 2.66×| 2.25×| 2.36×| 2.36×  |
| ori. gap-array 4-bit   | 84.4  | 87.7   | 30.0  | 37.3 | 87.2 | 31.9 | 25.9 | 25.9   |
| 5.26×                  | 3.38× | 1.19×  | 0.30× | 0.30×| 3.64×| 1.13×| 0.70×| 0.70×  |
| opt. gap-array         | 112.8 | 106.4  | 123.9 | 122.4| 95.4 | 96.3 | 84.7 | 110.1  |
| 4.27×                  | 4.08× | 4.92×  | 2.07× | 3.85×| 4.07×| 2.94×| 2.98×| 2.98×  |
both self-synchronization and gap array based parallel Huffman decoding are more suitable in some circumstances than others. Specifically, on one hand, if raw decoding performance is essential, our optimized gap array based Huffman decoding will inherently be faster than the self-synchronization based approach due to the costly and relatively unpredictable nature of finding synchronization points (particularly on GPUs). However, on the other hand, to obtain this raw decoding performance, applications must compute and store a gap array, which adds storage overhead as well as overhead to the encoder. Even in situations where these added costs are relatively insignificant, the encoder and the decoder must be coupled, meaning the encoder needs to be re-engineered. Therefore, in applications where flexibility is important, self-synchronization based Huffman decoding is more transparent to the encoders having different-source data and can balance this flexibility.

VI. RELATED WORK

In addition to works focusing on parallel Huffman decoding that have been referred to extensively throughout the paper (namely, Weißenberger and Schmidt’s work [12], Yamamoto et al.’s work [45], and to a lesser extent Klein and Wiseman’s work [22]), Johnston and McCreadh additionally proposed an algorithm for massively parallel Huffman decoding [21]. Their algorithm proposes to deal with the problem of decoding variable length codes by starting decoding from every location in the bit sequence, eventually decoding the bit sequence correctly. Taking advantage of the GPU manycore architectures, the algorithm performs slightly faster on the GPU than a single-CPU-core Huffman decoder. This approach is not well-suited for our purposes, as their approach results in large amounts of computation for only marginal gains over CPU-based decoders. Thus, in this work we only consider the other two algorithms.

Many works have been done that focus on optimizing parallel Huffman-type encoding. For example, Lal et al. proposed a Huffman-based entropy encoding system (E2MC) for GPUs [23]. More recently, Tian et al. proposed a fast parallel Huffman codebook construction algorithm and a parallel Huffman encoder for modern GPU architectures [40]. Since much work has already been focused on optimizing Huffman encoding, we do not presently consider optimizing encoding in our work.

VII. CONCLUSION

In this work, we comprehensively analyze two state-of-the-art Huffman decoding algorithms for error-bounded lossy compression of scientific data and propose a deep architectural optimization for both algorithms. We also propose an efficient online approach to tune the shared memory to decode different parts of the data based on the data characteristics. We then adapt our optimized decoders to multi-byte data and integrate it into cuSZ. Our evaluation on eight representative scientific datasets shows that our solution can improve cuSZ’s Huffman decoding throughput by 3.64× on average and cuSZ’s overall decoding throughput by 2.43× on average. In the future, we plan to optimize and evaluate our Huffman decoder for generic datasets such as text data on Nvidia A100 GPU.

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