Plasma Etching of Tapered Features in Silicon for MEMS and Wafer Level Packaging Applications

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Abstract. This paper is a brief report of plasma etching as applied to pattern transfer in silicon. It will focus more on concept overview and strategies for etching of tapered features of interest for MEMS and Wafer Level Packaging (WLP). The basis of plasma etching, the dry etching technique, is explained [1] and plasma configurations are described elsewhere [2][3]. An important feature of plasma etching is the possibility to achieve etch anisotropy. The plasma etch process is extremely sensitive to many variables such as mask material, mask openings and more important the plasma parameters.

Keywords: Plasma Etch, DRIE, tapered silicon profile, Wafer Level Packaging, MEMS.

1. Introduction and motivation. Why tapered silicon profile?
The technical challenges and the manufacturing complexity confronting conventional methods of increasing IC device density in 2-D are increasing at a high rate. In 1965, Moore’s Law postulated that the number of transistors per chip would double roughly every 2 years. In parallel with the increased device density within a chip, there is an increased overall functionality. This trend can be seen in applications such as MEMS (Micro Electro Mechanical Systems), RF circuits, where microsensors, microactuators are integrated with digital and analog electronic components. This complexity leads to smaller bond pads on devices and packaging challenges.

One of the requirements for the packages of image sensors and MEMS devices (such as RF- and AeroMEMS) or solar cells is the backside contact. The optical devices require an interface with environment without any restriction caused by the packages and on the other hand require a protection against the environment. [4]. The AeroMEMS need an interface with environment to detect or to modify the flow behavior [5]. Via-contact technology, developed by company Schott fulfills this requirements. The technology has been described in [4]. The main process steps are shown in Figure 1. The three key processes are plasma etching of via holes for the electrical contact to the front-end pads and the scribe-channels, the 3-D lithography to create the contact window in this via holes and the metallization to redistribute the pads connections. A similar technology to create backside contact for RF-MEMS has been described in [6]. To have good uniformity and step coverage in spray coating,
in lithography processes and metallization inside the features a tapered sidewall is needed. Features with vertical sidewall as normally seen in Bosch- [7] or cryogenic-processes [8] can not be used, since it is not feasible to have good step coverage at the sharp corner in following spray coating or sputtering processes. KOH and TMAH were the most methods used to generate tapered features in silicon since it is cheap and easy to use technique. In [6] the silicon substrate has been etched in KOH-solution. The limitations of this technique are the low etch rate (1µm/min) and the unflexibility for design (fixed angle at 54,7°) [9].

For microfluidic applications vias with tapered sidewall can be used as diffuser or nozzle. Use of channels with tapered sidewalls has obvious advantages such as simple geometry for calculation, higher possible flow rate and small thermal time constant.

Figure 1: SCHOTT IP, via contact technology for wafer level packaging of image sensors. Step a): plasma etch of tapered via holes and channel structures in silicon. b): deposition of passivation and IDL (Inter Dielectric Layer) layers, spray coating of resist and resist opening in via holes. c) plasma etching of back-end passivation/IDL layer/front-end passivation layer, resist stripping. d) sputtering of contact metal for redistribution. Solder mask and bumping.

2. State-of-the-art
The basic idea of plasma anisotropic etching is to find a balance between feature sidewall passivation and feature bottom etching. Plasma etching of tapered features in this paper has been developed and performed on HR (High Rate) ICP (Inductive Coupled Plasma) STS plasma kit tool. The etching gas is SF₆. Newest development shows that etching rate up to 25µm/min in silicon can be achieved with SF₆ based plasma [10].

The plasma etch process depends on the chemical reaction, the etch rate is dependant on the diffusion rate of the reactive species generated by the plasma to the etch front, and on the diffusion rate of the etch products away from the etch front. The rates of diffusion to and from the etch front are reduced relative to the shallow silicon structures. This reduces the etching rate, as the etch depth increases.

The Bosch process is an etch process based on continuous cycling of passivations and etch steps. Cryogenic plasma etch also could be used for etching of tapered profile [8]. The mechanism used in cryogenic etching is the combination of formation of blocking layer and reduction of the reaction probability of radicals at silicon surface. Disadvantage of this method is the cryogenic temperature. This low temperature makes it not usable for most applications due to the temperature limitations. Cryogenic plasma etching is not a focus of this work.
2.1. SF₆/O₂ gas chemistry

It has been found out that it is easy to create tapered features up to 30µm depth in silicon with SF₆/O₂ (up to 30% O₂) gas mixture. For features deeper than 30µm the sidewall tends to have overhangs. Figure 2 shows two vias etched with the same recipe but different etch times. The via on the left has no overhang, but the via on the right has an overhang about 20µm. This overhang (bowing) is very critical for the next process steps as shown in Figure 1 such as spray coating, deposition of passivation layers and metallization since it leads to bad step coverage at this area.

The SF₆/O₂-Si system is an ion-inhibitor process. In this gas system oxygen is passivating the silicon surface with silicon oxide and the SF₅⁺ ions are etching the passivator making it possible for the F⁻ radicals to etch the silicon substrate. The possible causes of the overhang are: sidewall charging - because the passivation layer is an insulator (SiO) so the ions colliding with the sidewall will leave their charge which is difficult to compensate with electrons. This charging can repel the next ions. Ion deflection – is most pronounced for SF₆/O₂ etch gas mixture. The negative potential of the via walls deflect the ions to the vias wall. Ion shadowing – when ions arrive under an angle the topside of the features will block ions from etching the area under the mask layer.

![Figure 2: SEM pictures. Vias etch with same recipe but different etch time. a) lower etch time, etch depth 17µm with no overhang. b) longer etch time, etch depth 54µm with overhang.](image)

It is to believe that the ion deflection is the main driving force of the overhang in the via profile (bowing). To overcome this draw back an approach has been used. This approach is shown in Figure 3. Firstly a profile with overhang is etched. It is followed by a stripping step. In this step the mask layer has been removed by pure oxygen plasma. The final step is an isotropic etching step to remove the overhang and to achieve the final feature geometry. In our packaging application, the stress containing silicon layer with crystal dislocation, generated in a mechanical thinning step, can be removed to guarantee a reliable package performance. Figure 3 shows the approach and the results. The sidewall angles are adjustable in the range between 55-75°. The roughness inside the features is excellent (<<200nm). The selectivity silicon to resist is higher than 50.

The ion deflection, main driving force of the bowing, can be minimized by increasing the sidewall passivation, the wall charging or the energy of the ions before entering the vias and channels. This can be achieved by adding an extra fluorine based passivation gasses.
Figure 3: Multistep etch approach. The etch scheme is shown on the left. In the first initial step profile with bowing has been generated in a high etch rate SF₆/O₂ plasma (~10%O₂). The typical etching rate in this step is higher than 10µm/min (for 5% etch area). Second, the etch mask has been removed in pure oxygen plasma. In last step, the final profile has been achieved in an isotropic etch step (SF₆ plasma). Results on 6inch wafer are shown on right side.

2.2. SF₆/O₂/passivation gas 1 chemistry
The glow discharge of this passivation gas 1 produces chemically reactive polymer precursor species, which can be employed to deposite blocking polymer film isotropically over the wafer surface. Detailed work on a Bosch-type process with this gas chemistry for etching of tapered silicon sidewalls can be found in [11]. Because the passivation material is FC polymer, effects such as ion charging and ion deflection can be avoided. It has been found that tapered profile can be achieved in one step etch approach with this gas chemistry. Figure 4 shows the approach and the results achieved on 8inch wafer size. Using this gas mixture enables an easy design but the roughness inside the features is critical for some applications. The typical roughness using this gas mixture is about 3µm. For applications, which need good roughness such as microfluidic or electronic packaging, an extra improving step is needed.

Figure 4: One step etch approach. Via etched with SF₆/O₂/passivation gas 1 chemistry on 8inch material on the left. Roughness inside via is about 3µm. Selectivity silicon to resist is about 80.
2.3. SF₆/O₂/passivation gas 2 chemistry
This gas chemistry enables passivation the silicon surface with silicon oxide and polymer (FC fluorocarbon). The passivation gas is not only the source of the fluorocarbon polymer passivating the silicon surface but also the source of CFₓ ions, which in turn are responsible for the removal of SiOₓFᵧ layer at the bottom of the features forming the volatile COₓFᵧ. The F:C ratio is important, so the lower the F:C ratio the more stable is the passivation polymer [12]. In that case the passivation polymer can be removed by O₂ plasma completely. Figure 5 shows the one step approach and the via etched with this gas chemistry.

![Image](image_url)

Figure 5: One step etch approach (left) with SF₆/O₂/passivation gas 2 chemistry. Etched via on the right. Etching rate is about 11µm/min. Micro roughness is lower than 200nm.

3. Conclusion
Dimensional control in structuring of small features is necessary for advanced micromachining. Plasma etching is becoming a widely accepted standard process. The investment for plasma equipments is still high, but it is introduced rapidly due to the anisotropy of etching without using the crystal orientation such as in KOH or TMAH, the ability to faithfully transfer defined mask pattern into silicon, cleanliness and compatibility with other vacuum-processing technologies and more important the becoming higher etching rates achievable in the newest plasma etch chambers [10].

We have successfully developed plasma etch processes to etch tapered features and successfully applied for WLP application [4]. SF₆/O₂ gas chemistry tends to generate bowing in silicon. A multistep etch strategy has been used with this gas chemistry. Tapered profile with sidewall angles between 55-75° can be generated. The overall etching rate with this approach is about 10µm/min. The profile has a roughness lower than 200nm.

One step etch approach can be used with different fluorine based passivation gasses. Etching with SF₆/O₂/passivation gas 1 has typically roughness about 3µm. This roughness might be critical for some applications. An improving step is needed for this gas chemistry. SF₆/O₂/passivation gas 2 seems to be the best compromise. The overall achieved etch rate is depending on the roughness quality required (between 7-12µm/min for 5% opened area). All gas chemistries have very high selectivity to photoresist (AZ), typically higher than 50:1. It shows a big potential for other MEMS applications such as RF MEMS structures, which needs back side contacts and microfluidic applications.

References
[1] Lieberman, A. M., „Principles of Plasma Discharges and Materials Processing”, John Wiley & Sons, New York, 1994.
[2] Popov, O. A., “High density plasma sources. Design, Physics and Performances”, Noeys Publications, Park Ridge, New Jersey, USA, 1995.
[3] Rossnagel, S. M., Cuomo, J. J., Westwood, W. D., „Handbook of plasma processing technology”, Noeys Publications, Norwich, New York, USA, 1990.
[4] Leib, J., Töpper, M., „New Wafer-Level-Packaging Technology using silicon via contacts for optical and other sensor applications”, ECTC, Las Vegas, USA, 2004.
[5] Løfdahl, L., Gad-el-Hak, M., “MEMS applications in turbulence flow control, Progress in Aerospace Science, 35, 101-203, 1999.
[6] Pham, N. P., Sarro, P. M., Burghartz, J. N. “IC-compatible process for pattern transfer in deep wells for integrations of RF components”, Proc. SPIE, Santa Clara, USA, 4174390-7, 2000.
[7] Robert Bosch GmbH, Patent 5501893, 1996.
[8] Online Information Alcatel Vacuum Technology, France, www.adixen.fr.
[9] Seidel, H., Csepregi, L., Heuberger, A., Baumgarten, H., “Anisotropic etching of crystalline silicon in alkaline solutions: I. Orientation dependence and behavior of passivation layers,” Journal of the Electrochemical Society, vol. 137, no. 11, pp. 3612-3626.
[10] Online Information Surface Technology Systems, UK, www.stsystems.co.uk.
[11] Chamber, A., “Silicon Micro-Machining as an Enabling Technology for Advanced Packaging”, Semiconductor Manufacturing Magazine, Nov 2004, pp. 38-43.
[12] Shul, R. J., Pearton, S. J., “Handbook of advanced plasma processing techniques”, Springer, Germany, 2000.