Silicon carbide (SiC) has the potential to replace conventional semiconductors in high-frequency and high-power applications such as in pulse-width modulated electric vehicles, smart grids and next-generation power electronics. SiC’s advantages over silicon, the current industry standard, include high saturation velocity (high current), and wide bandgap (high voltage/temperature), both of which enable minimization of parasitic capacitances and reduction of active cooling, leading to transformational architectural improvements in power electronics.

While the device structures have been well optimized, other challenges in SiC technology remain in material quality. Research in the past few years has focused on growing high-quality single-crystal SiC substrates and epilayers with low densities of structural defects. In addition to the high structural quality, there are other requirements that must be met for these epilayers to be useful in power devices. In a power transistor chip, the metalized backside and fingers on the epitaxial side introduce a passive parasitic capacitance, limiting the performance at high frequencies. This parasitic capacitance can be minimized by using semi-insulating (SI) epilayers/substrates. One of the methods of introducing SI property to the substrate is to use vanadium as a deep level dopant to pin the Fermi level near mid-bandgap. Although this is the originally conceived method of producing commercial SI substrates, reports indicate that vanadium degrades the crystal quality.  

The alternative is to pin the Fermi level deep in the bandgap by compensating shallow donors/acceptors from residual impurities with intrinsic deep defects. The development of such high-purity semi-insulating (HPSI) SiC was reported, but determination of the exact nature of the defects and compensation mechanism are still in progress. Electron paramagnetic resonance (EPR) measurements on as-grown HPSI 4H-SiC material detected carbon vacancies \( V_C \). A broad range of defects including \( V_{Si}, V_{C}-V_{Si} \), and \( V_{C}-C_{Si} \) have been reported by Son et al. A recent report by Mitchel et al. summarized the deep levels present in the upper half of the band gap of the 4H-SiC HPSI material which includes \( Z_{4/2}, RD_{1/2} \), and \( \text{EH}_{0/7}, Z_{1/2} \) is an efficient recombination center and acts as a lifetime killing defect in 4H-SiC.

Identification of the electronic levels due to intrinsic defects responsible for lifetime control and compensation in HPSI 4H-SiC is of great technological importance.

In this letter, we discuss the chemical vapor deposition (CVD) growth conditions for achieving HPSI epitaxial layers by defect competition epitaxy and identify the deep defect centers, responsible for SI behavior, using high-resolution photoinduced transient spectroscopy (HRPITS). The epitaxial films discussed here were all grown on commercial 4H-SiC, n-type Si-face substrates off-axis towards the (1120) direction, in a vertical hot-wall CVD reactor at temperatures of 1450–1650 °C and pressures of 80–120 Torr. Dichlorosilane and propane are the precursors in a hydrogen ambient. The growth rate was 30 μm/h with no intentional dopants incorporated. The epilayers were characterized using X-ray diffraction (XRD) for crystal quality, transmission line model (TLM) for resistivity, time-resolved photoluminescence spectroscopy (TRPL) for carrier lifetime, secondary ion mass spectroscopy (SIMS) for impurity concentration (Evans Analytical Group, NJ), and HRPITS for trap centers.

Site competition epitaxy enables the control of impurity incorporation into SiC by adjusting the C/Si ratio. Nitrogen (n-dopant) competes for C sites and boron (p-dopant) competes for Si sites of the SiC epilayer. Increasing the C/Si ratio decreases nitrogen incorporation, making the epilayer less n-type, while decreasing the C/Si ratio decreases boron incorporation, making the epilayer less p-type. It is expected that there is a transition between n- and p-types where impurity incorporation is minimized to produce SI SiC, when the necessary deep levels are present.

A wide variation of epilayer doping with respect to the C/Si ratio was observed, as in Fig. 1. For \( 1.3 < C/Si < 1.5 \), the as-grown epilayer shows SI behavior. We term this regime “defect competition epitaxy” to distinguish it from the “site competition” regime shown in the figure for reasons that will be discussed further below. Approximately 20 samples were produced in this regime with resistivity \( \rho > 10^9 \Omega \text{cm} \) supported by TLM measurements. From TLM, a resistivity of \( \rho = 1.6 \times 10^9 \Omega \text{cm} \) was measured for SI samples with C/Si ~ 1.4. This is a lower bound, as the TLM patterns were not mesa isolated due to the thickness of the films (60 μm). Therefore, spreading resistance is not accounted for. A typical epilayer X-ray rocking curve
guide the eye and distinguish n-type from p-type behavior, respectively.

Table I. SIMS analysis of 4H-SiC HPSI and n-type samples. The only elements detected are the shallow level impurities nitrogen and boron.

| Elements | n-type (C/Si: 0.9) | HPSI (C/Si: 1.4) | HPSI cree |
|----------|-------------------|-----------------|-----------|
| B        | $1.0 \times 10^{14}$ | $3.6 \times 10^{14}$ | $7.0 \times 10^{13}$ |
| N        | $1.6 \times 10^{15}$ | $1.8 \times 10^{15}$ | $2.0 \times 10^{16}$ |
| Al       | $5.0 \times 10^{13}$ | $<7.0 \times 10^{13}$ | $<5.0 \times 10^{13}$ |
| V        | —                 | $<2.0 \times 10^{12}$ | $5.0 \times 10^{13}$ |

Resistivity ($\Omega$ cm) 
$\sim 30$ 
$\sim 1.0 \times 10^9$ 
$\sim 1.0 \times 10^{11}$

a) Ref. 12.

full-width half maximum (FWHM) is $\sim 8$ arcsec, close to 6–8 arcsec for perfect SiC. This compares very favorably with results showing FWHM’s of 18 arcsec for HPSI and 24 arcsec for V-doped SiC.

To determine how C/Si affects background impurity incorporation, SIMS analysis was performed. Table I shows N, Al, and B (major n- and p-type dopants in SiC, respectively) concentrations in low-doped n-type (C/Si $\sim 0.9$) and in HPSI (C/Si $\sim 1.4$) samples, along with the best published HPSI SIMS result to date. Surprisingly, we see that increasing C/Si from 0.9 to 1.4 does not significantly change the concentration of impurity incorporation but does change the resistivity from $\sim 30$ to $\sim 10^9 \Omega$ cm. Hence, at these low impurity levels, rather than driving out nitrogen, a higher C/Si introduces intrinsic deep levels, which account for pinning the Fermi level far away from the band edge. A high C/Si ratio promotes Si-vacancy ($V_Si$) while a low C/Si ratio promotes C-vacancy ($V_C$) formation. The variation of these intrinsic defects with C/Si ratio, as opposed to impurity incorporation, leads to the term defect competition, in contrast with site competition. Vanadium compensation can be excluded completely (Table I).

Using the impurity concentrations from SIMS (Table I), together with the doping and resistivity data, the schematic band diagram using Fermi statistics can be determined. Figure 2(a) shows the band diagram for the low-doped n-type (C/Si: 0.9, doping from C–V = $1.5 \times 10^{15}$ cm$^{-3}$) sample, where the Fermi level ($E_f$) is 0.25 eV below the conduction band ($E_c$). Here, we have taken the band gap $E_g \approx 3.26$ eV, $E_c - E_v \approx 90$ meV, $E_a - E_v \approx 220$ meV$^{15}$ and $n_e = (N_d - N_v) = 1.45 \times 10^{15}$ cm$^{-3}$.

The band diagram for the HPSI sample [Fig. 3(a)] is determined using resistivity $\rho = 1.6 \times 10^9 \Omega$ cm and mobility $\mu = 900$ cm$^2$ V$^{-1}$ s$^{-1}$ for 4H-SiC, and the equation, $\rho = 1/n\mu$, resulting in a free electron density, $n \approx 10^6$ cm$^{-3}$. Given that the SiC effective density of states in the conduction band $N_c = 1.5 \times 10^{15}$ cm$^{-3}$ for HPSI (C/Si $\sim 1.4$) is located 0.8 eV below $E_c$. Though the actual $\mu$ of the Si material might be lower, this value is taken in the absence of a proper $S_F$ value. Any $\mu$ in the range of 100–1000 cm$^2$ V$^{-1}$ s$^{-1}$ still pins the $E_f$ around 0.7–0.8 eV below $E_c$. This $E_f$ is not consistent with SIMS unless the residual donors ($N_d - N_F$) are completely compensated by intrinsic deep defects pinning $E_f$ at 0.8 eV below $E_c$. From this analysis, the intrinsic trap concentration must be $<1.45 \times 10^{15}$ cm$^{-3}$.

To confirm the presence of the inferred traps, TRPL measurements were performed on both samples at room temperature. Excitation was provided using a frequency doubled, modelocked, cavity-dumped Ti:sapphire laser (355 nm, 150 fs pulse width, 100–500 kHz, 5 nJ/pulse). The average injection level over the layer was $\approx 2 \times 10^{14}$ cm$^{-3}$. The n-type sample showed a lifetime of 0.8 μs, whereas the HPSI sample showed no band edge emission. This occurs if either the crystal quality is poor or if there are enough traps to provide effective nonradiative recombination centers. The XRD FWHM $\approx 8$ arcsec demonstrates the high quality of these crystals, while SIMS demonstrates their purity, indicating that the short lifetimes inferred in the HPSI sample are from intrinsic deep defects.

To identify the nature of these intrinsic defects, HRPITS measurements were performed on both low-doped n-type
and Si samples. HRPITS is a characterization technique in which the sample is illuminated with pulsed light. The resulting photocurrent transients are recorded as a function of temperature, revealing information about traps in the material. The experimental details and photocurrent relaxation analysis are found elsewhere. HRPITS in low doped n-type (C/Si: 0.9) samples revealed [Fig. 2(b)] the presence of EH_{6/7} (VC related traps), as expected under Si-rich growth conditions. The common shallow level impurity boron was not observed, in agreement with the low B concentration from SIMS (Table I). We note that the defect levels are spread throughout the gap.

HRPITS on the HPSI (C/Si: 1.4) sample reveals [Fig. 3(b)] a contrasting picture. Only Si-vacancy (V_{Si}) and carbon-antisite (C_{Si})-related deep defect levels were observed, in accordance with the increased C/Si ratio, where V_{Si} and C_{Si} are expected to dominate. The positions of these levels cluster around 0.8 eV below E_{c}, in agreement with the E_{c} position extracted from TLM. Also, we see that the dominance of residual shallow donours (SIMS in Table I) favors negatively (V_{Si}^{-}) charged defects. No Z_{i/2} and EH_{6/7} levels are observed, again in accordance with the increased C/Si ratio. In other words, by adjusting C/Si, the dominant generation/recombination (G–R) energy level is moved from near midgap (typical for SiC) to far away from midgap. Such a controllable compensation scheme has not been demonstrated in SiC technology.

This non-midgap Fermi level in HPSI SiC has important implications in high-frequency SiC power devices. Using Shockley–Reed–Hall (SRH) recombination statistics, the recombination lifetime

\[ \tau_r = \frac{1}{\frac{2n_i}{n_{th}} + \frac{p_{th}}{n_{th}}} \cosh \left( \frac{E_c - E_i}{kT} \right) \]

is inversely proportional to N_{i}, the concentration of recombination centers/traps where n_{th}, \sigma_{0}, and E_{i} are intrinsic carrier concentration, thermal velocity, capture cross section, and trap level, respectively. For high-speed switching operations, short recombination lifetimes are required. Deeper levels provide faster recombination. Using N_{i} \sim 1 \times 10^{16} \text{cm}^{-3}, \sigma_{0} = 10^{-15} \text{cm}^{-2}, \text{ and } n_{th} = 10^{15} \text{cm}^{-3}, \text{ we estimate } \tau_r = 7 \text{ ns for the HPSI material, compared with 5 ns for midgap G–R centers (Table II). This opens the possibility of switching speeds in the gigahertz range with the HPSI. Despite shifting the dominant G–R level away from the midgap, switching speed can be maintained (Table II). However, the carrier generation time, which controls the leakage current in bipolar devices, given by \tau_g/\tau_r \equiv 2 \cosh((E_c - E_i)/kT) increases. In other words, \tau_g becomes longer as E_c moves away from midgap, strongly suppressing the leakage current (Table II), which in SiC is dominated by generation current (ideality, n \approx 2), I_{gen} \equiv qn_iW/\tau_g. Table II shows that the generation current can effectively be removed, potentially enabling the leakage current to be band to band (n = 1). This may enable much higher blocking voltages than those achievable for devices with mid-gap G–R centers. While we assume that the same levels are responsible for generation and recombination to simplify this discussion, this may not always be the case. Nevertheless, this does not change the conclusion that moving the major traps away from the midgap suppresses leakage currents. The demonstrated HPSI material may increase the blocking voltage in SiC bipolar devices.

In summary, the growth of thick HPSI 4H-SiC (0001) epilayers has been demonstrated in a vertical hot-wall CVD reactor at a high growth rate of 30\mu m/h. This was achieved through a novel compensation scheme that controls the formation of Si-related vacancies through defect competition. A wide window of defect competition epitaxy has been demonstrated. Resistivity \geq 10^7 \Omega cm has been shown by TLM. A high C/Si ratio is the key for introducing Si behavior supported by the presence of only Si vacancy-related defects shown by HRPITS. These HPSI materials with G–R centers away from the midgap can be used in fast-switching bipolar devices with high blocking voltage.

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| Table II. Comparison of calculated recombination and generation lifetimes for mid-bandgap and V_{Si} related trap levels and their device implications. |
|---|---|---|---|
| **Mid bandgap** | **V_{Si} related traps** | **Device implication** |
| \( E_i = E_c - 1.63 \text{ eV} \) | \( E_i = E_c - 0.88 \text{ eV} \) | |
| \( \tau_r \) | 5 ns | 7 ns | Fast switching |
| \( \tau_g \) | 2\tau_r | \( 8 \times 10^3 \times \tau_r \) | Low leakage current |

1) H. K. Song et al.: Appl. Phys. Lett. 89 (2006) 152112.
2) W. C. Mitchell et al.: J. Appl. Phys. 86 (1999) 5040.
3) V. V. Konovalov et al.: Physica B 308–310 (2001) 671.
4) E. N. Kalabukhova et al.: Phys. Rev. B 64 (2001) 235302.
5) N. T. Son et al.: Mater. Sci. Forum 457–460 (2004) 437.
6) W. C. Mitchell et al.: J. Appl. Phys. 101 (2007) 053716.
7) T. Kimoto et al.: Phys. Status Solidi B 245 (2008) 1327.
8) I. Chowdhury et al.: J. Cryst. Growth 316 (2011) 60.
9) D. J. Larkin et al.: Appl. Phys. Lett. 65 (1994) 1659.
10) K. Fujihira et al.: Appl. Phys. Lett. 80 (2002) 1586.
11) J. H. Yim et al.: Mater. Sci. Forum 556 (2007) 763.
12) J. R. Jenney et al.: J. Electron. Mater. 32 (2003) 432.
13) L. Torpo et al.: J. Phys.: Condens. Matter 13 (2001) 6203.
14) S. M. Sze: Physics of Semiconductor Devices (Wiley, New York, 1981) 2nd ed.
15) W. J. Choyke and G. Pensl: MRS Bull. 22 (1997) 25.
16) Yu. Goldberg et al.: Properties of Advanced Semiconductor Materials (Wiley, New York, 2001) p. 93.
17) N. T. Son et al.: Appl. Phys. Lett. 66 (1995) 1074.
18) P. Kaminski et al.: Opto-Electron. Rev. 17 (2009) 1.
19) N. T. Son et al.: Phys. Rev. B 75 (2007) 155204.
20) C. G. Hemmingson et al.: J. Appl. Phys. 81 (1997) 6155.
21) T. Kimoto et al.: Appl. Phys. Lett. 79 (2001) 2761.
22) M. E. Levinstein et al.: Solid-State Electron. 49 (2005) 1228.