A 40-Gb/s 3-tap forward feedback equalizer with DLL-based delay time calibration

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Abstract: This paper presents a 40-Gb/s 3-tap forward feedback equalizer (FFE) incorporating broadband active delay cell, multiplier & summer and a delay-locked loop (DLL). The active delay cell employs capacitive degeneration and negative impedance structures to broaden the bandwidth. The source-degenerated linear transconductor based multiplier & summer circuits are used through appropriate setting of the FFE tap coefficients. The delay time of the delay cells are calibrated by a DLL against process, voltage, and temperature (PVT) variations. For improving calibration accuracy, the phase detector adopting two symmetric XOR gates and the charge pump utilizing current splitting and self-detection compensation techniques are designed. The proposed circuit is fabricated in 130 nm BiCMOS process, which achieves a data rate of 40 Gb/s through 20-inch FR-4 PCB trace and the horizontal and vertical eye openings of 0.55 UI and 150 mV.

Keywords: feed-forward equalizer (FFE), delay-locked loop (DLL), delay time calibration, broadband technique, PVT insensitivity

Classification: Integrated circuits

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1 Introduction

With the ever-increasing demand of the broadband wired data communications, high speed equalization techniques have been popular to mitigate the inter-symbol interference (ISI) caused by the channel dispersion. Since the responses of the backboard channels have frequency-dependent losses, the transceivers usually need equalizer to provide an inverse transfer function of the channel to maintain signal integrity.

In general, the equalizers are divided into linear and nonlinear types. Compared with the nonlinear decision feedback equalizer (DFE), the linear feed-forward equalizer (FFE) has the advantages that it can compensate the precursor ISI, be easy to realize and immune to error propagation. However, it will also amplify the noise or crosstalk [1]. When the channel loss is moderate, the FFE is preferred.

The delay line circuit is a crucial element in FFE, which is used to realize the algorithm of equalization. The accuracy of delay time accounts for the equalization effect and should be taken care of. Generally, both active and passive delay methods can be adopted to realize the delay line [2, 3]. The passive delay cell, such as transmission line or lumped LC ladder, has low power dissipation, high bandwidth and good accuracy, but occupy large chip area. The active delay cell has negligible chip area, yet it is susceptible to PVT variations and has limited bandwidth [4]. Therefore, the loop calibration method utilizing feedback and accurate external reference is proposed to guarantee the delay time accuracy.

The FFE core involves the active wideband delay cells with tunability and compactness, which are matched to those in DLL. That induces that the delay time can be automatically and accurately calibrated regardless of the PVT variations.
This DLL features a symmetric phase detector and low current-mismatch charge pump, which has low locked error and better calibration performance.

The characteristics of this paper mainly have three aspects: first, the DLL is adopted to mitigate delay errors of FFE caused by PVT disturbance to improve the equalization, second, the novel active wideband tunable delay cell and multiplier & summer in FFE core are proposed, third, phase detector and charge pump in DLL are presented, which can reduce loop-locked error and improve the calibration performance.

This paper is organized as follows. Section II presents the architecture of equalizer system. Section III describes the designs of main sub-circuits and PVT immunity simulation. Section IV shows the experimental results and performance summary. Finally a conclusion is drawn in section V.

2 System architecture

Fig. 1 shows the overall architecture of the proposed equalizer in a typical high-speed wired receiver. The proposed equalizer system consists of an FFE core and a DLL-based calibration loop.

In FFE core, the signals of each tap are multiplied by tap coefficients $C_{-1}$, $C_0$, $C_1$ and summed up to improve the quality of the received data. Through the analysis and calculation method of the FFE tap-coefficients in [5], the equalization tap coefficients can be achieved preliminarily, and further fine tuning will be needed to compensate the pre-cursor and post-cursor components in the pulse response. The unit tap delay in FFE is determined by $V_{ctrl}$ from DLL, which has the replicated delay cells and be controlled the external reference clock to mitigate the effect of PVT variations.

The DLL is mainly composed of phase detector (PD), charge pump (CP), voltage-controlled delay line (VCDL) and filter. When the delay difference equals to 1/4 period of the input reference signal, the output voltage $V_{ctrl}$ of the charge pump is stable that controls the delay time of the VCDL and the tap in the FEE.

![Fig. 1. Architecture of proposed equalizer system](image-url)
3 Circuit design

3.1 Active wideband delay cell

To meet high data transmission requirement, it is necessary to design a broadband short-delay delay cell. Some popular wideband techniques are used, such as inductive peaking, capacitive degeneration, $f_T$ doublers, Cherry-Hopper. The active inductive shunt peaking technique can broaden the bandwidth and be controlled by the external voltage. However, this structure limits the output swing and the gain cannot be tuned. The $f_T$ doublers and Cherry-Hopper techniques are unrealistic as the delay line due to the excessive power.

Fig. 2(a) shows the proposed active wideband delay cell with the controlled voltage $V_{ctrl}$ from DLL. The delay cell is composed of two stages. The first stage is a wideband amplifier with the capacitive degeneration structure and the second stage is a source follower with negative impedance structure, which is used as the voltage-level shifter. The effective source resistor $R_S$ is the parallel one of MOS resistor $M_{10}$ and $R_0$. The $M_4$ and $M_5$ compose the MOS varactor $C_S$. The $V_{ctrl}$ controls $R_S$ and $C_S$ at the same time. The negative impedance $Z_f$ can further broaden the bandwidth and can be derived as [6]:

$$Z_f = \frac{1}{g_f} = - \frac{1}{sC_n} - \frac{2}{g_{m9}}$$

(1)

where $C_n$ is the MOS capacitor. Fig. 2(b) depicts single-ended equivalent of the proposed delay cell. The voltage gain of the delay cell can be expressed as

$$A_v = \frac{v_{out}}{v_{in}} = A_0 \cdot \frac{1 + s/z_1}{(1 + s/p_1)(1 + s/p_2)}$$

(2)

The output resistor is

$$R_L = \frac{1}{g_{m3}} \left| \frac{1}{g_{m5}} \left( - \frac{1}{g_{m8}} \right) \right| = \frac{1}{g_{m3} + g_{m5} - g_{m8}}$$

(3)

which contributes a zero $\omega_z = (R_S C_S)^{-1}$, two poles $\omega_p1 = (1 + g_{m1} R_S/2)/R_S C_S$, and $\omega_p2 = (g_{m3} + g_{m5} - g_{m8})/(C_L - 2C_n)$. The voltage gain and group delay are expressed by

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1} R_D}{1 + g_{m1} R_S/2} \cdot \frac{g_{m3}}{1 + \frac{g_{m3} + g_{m5} - g_{m8}}{g_{m3} + g_{m5} - g_{m8}} + \frac{sR_S C_S}{1 + g_{m1} R_S/2} \left( 1 + s \frac{C_L - 2C_n}{g_{m3} + g_{m5} - g_{m8}} \right)}$$

(4)

$$GD(\omega) = -\frac{d\phi}{d\omega} = -\frac{R_S C_S}{1 + (\omega R_S C_S)^2} + \frac{2R_S C_S}{1 + \left( \frac{2\omega R_S C_S}{2 + g_{m1} R_S} \right)^2} + \frac{C_L - 2C_n}{1 + (\omega \cdot \frac{C_L - 2C_n}{g_{m3} + g_{m5} - g_{m8}})^2}$$

(5)
At the lower frequency, the group delay can be expressed by

\[ GD(0) = \frac{C_L - 2C_n}{g_m3 + g_m5 - g_m8} - \frac{g_m1R_S^2C_S}{2 + g_m1R_S} \tag{6} \]

Based on equations (4) to (6), through adjusting the size of \( M_8, M_9 \) and \( C_n \), the \( \omega_n^2 \) may be transformed into a new zero, which will effectively improve the bandwidth and reduce the delay time. Meanwhile, the \( V_{\text{ctrl}} \) can adjust the gain and delay time through controlling \( R_S \) and \( C_S \). Fig. 3 shows the bandwidth comparison with different structures, where the proposed active delay cell has the broader bandwidth than the conventional structures.

3.2 Multiplier & summer

The proposed multiplier & summer circuit, as shown in Fig. 4, adopts the source-degenerated linear transconductors to improve the input dynamic range and current.
mode logic (CML) structure with passive resistance loads to enhance the bandwidth and output swing. The transconductor converts the input voltages into currents that are summed up and transformed to the output voltage by the resistor. Compared with the conventional the multiplier & summer, the proposed circuit utilizes the source degenerated resistors ratios to denote the linear transconductance ratios, which are easy to realize the tap coefficients.

![Fig. 4. Multiplier & summer circuit.](image)

### 3.3 Phase detector & charge pump of DLL

The proposed PD with two symmetric XOR gates, as shown in Fig. 5, is used to realize the $90^\circ$ phase difference (i.e. $1/4$ period) between input signal and the feedback signal. Signal $A$ and $B$ are from the input signal, and signal $\bar{A}$ and $\bar{B}$ are from the VCDL. The XOR gate implements the logic:

$$V_o = A \cdot B + \bar{A} \cdot \bar{B} = A \oplus B$$  \hspace{1cm} (7)

This proposed symmetric structure is superior to the conventional source coupled logic (SCL) XOR circuit, which can reduce the phase error induced by the asymmetric signal paths at high frequency [7].

![Fig. 5. The proposed PD with two symmetric XOR gates.](image)
To mitigate the current mismatch from the non-ideal characteristics, such as channel length modulation effect, the proposed CP, as shown in Fig. 6, combines the current splitting and self-detection compensation techniques to reduce the current mismatch in the area \( a \) and \( b \), respectively [8, 9], which avoiding an error amplifier with the extra design complexity and power.

Compared with conventional current-steering CP, the proposed current splitting technique adds mirror current branches \( M_5 \) and \( M_6 \) to reduce the current ratio, which has smaller \( I_{Dn} \) and \( I_{Up} \). \( M_1 \) and \( M_2 \) compensate the imbalance of \( I_n \) and \( I_p \) if \( V_{ctrl} \) deviates the proper voltage value. When \( V_{ctrl} \) is low, \( M_2 \) turns on and pulls \( M_4 \) gate to VDD, which will further reduce the current mismatch. When \( V_{ctrl} \) is high, then \( M_1 \) will work.

Fig. 7 shows the simulation comparison of the current mismatch versus \( V_{ctrl} \) for the proposed CP, conventional current-steering CP with and without compensation techniques. In the graph, the current mismatch of proposed CP is almost closed to zero for most of \( V_{ctrl} \) compared with others, which can reduce the loop-locked error and improve calibration accuracy.

![Fig. 6. The schematic of proposed CP.](image)

![Fig. 7. Simulated current mismatch for different CP structures.](image)
3.4 PVT immunity simulation

The unit tap delay stability reflects the PVT insensitivity and determines the equalization quality. For a 40-Gb/s transmission data rate, the unit delay of delay line, i.e. the T/2 tap spacing, should be set as 12.5 ps. Depending on DLL calibration, the unit tap delay amount is close to the normal value 12.5 ps against PVT variations as shown in Fig. 8(a). The simulated worst-case deviation is within 0.2 ps, which is superior to one without DLL over different PVT. The Monte Carlo simulation for the unit tap delay distribution is shown in Fig. 8(b). The mean value and standard deviation are 12.52 ps and 0.29 ps, respectively, which show the robustness of the unit tap delay against process variation.

![Fig. 8. (a) Unit tap delay variation with and without DLL over different PVT (b) Monte Carlo simulation result for the unit tap delay.](image)

4 Measurement results

The proposed FFE with DLL calibration is fabricated in IBM 0.13-μm SiGe 8HP BiCMOS process. The chip microphotograph is shown in Fig. 9, which measures 0.89 × 0.62 mm² including pads and active area occupies 0.64 × 0.35 mm². The chip has been tested on the probe station with SHF data generator (SHF04)

![Fig. 9. Chip microphotograph of the proposed FFE.](image)
providing the PRBS input and the Agilent 86100D oscilloscope. The equalizer system consumes 293 mW power totally and FFE core dissipates 117 mW under 2.5-V supply.

Fig. 10 shows the S-parameter for 20-inch FR4 PCB trace for experiment, which has 27-dB loss at 20 GHz. The measured 40-Gb/s eye diagram for PRBS $2^{15}-1$ pattern before equalization for the 20-inch FR-4 PCB trace are shown in Fig. 11(a), Fig. 11(b), (c) and (d) show the measured eye diagrams after equalization under 2.3, 2.5 and 2.7-V supplies, respectively. The measured equalization results are almost similar, but the magnitudes and eye openings are enlarged as power supplies increase. However, the process corner of the fabricated chip is fixed and the test temperature is hard to be adjusted, thus the process and temperature

![Fig. 10. Measured S-parameter for 20-in FR4 trace.](image)

![Fig. 11. Measured eye diagrams at 40 Gb/s (a) before equalization, (b) after 2.3 V-supply equalization, (c) after 2.5 V-supply equalization, (d) after 2.7 V-supply equalization.](image)
variations only depend on simulation to verify in Section 3.4. Through setting the equalizer coefficients, the horizontal and vertical eye openings are 0.55 UI and 150 mV, respectively. Table I presents the performance summary and comparison with the previous reported equalizer.

**Table I. Performance summary and comparison**

| Ref. | Ref. [10] | Ref. [11] | Ref. [12] | Ref. [13] | This work* |
|------|-----------|-----------|-----------|-----------|------------|
| Technology | 65 nm CMOS | 65 nm CMOS | 28 nm CMOS | 45 nm CMOS | 130 nm BiCMOS |
| Architecture | 7-tap FFE | 5-tap FFE | 2-tap FFE | CTLE DTLE 2-tap DFE | 3-tap FFE |
| Data rate (Gbp/s) | 40 | 40 | 40 | 40 | 40 |
| Eye opening (UI) | 0.7 | 0.4 | 0.27 | 0.28 | 0.55 |
| Power Efficiency (mW/Gbps/Lane) | 1.625 | 3.37 | 3.25 | 0.23 | 2.9 |
| Power (mW) | 65 | 135 | 130 | 9.2 | 117 |
| Die area** (mm²) | 0.75 | 0.6 | 0.75 | 0.02 | 0.22 |

*Equalizer core  
**Active area only

5 Conclusion

This work presents a 40-Gb/s active FFE using DLL-based delay time calibration. The active delay line uses the capacitive degeneration and negative impedance techniques to improve bandwidth. The charge pump of DLL reduces current mismatch without an error amplifier. Through DLL calibration, the loop calibration can improve the robustness for PVT variations. The measurement results demonstrate successfully transmission of 40-Gb/s data rate over 20-inch FR-4 PCB trace.

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