Positron lifetime setup based on DRS4 evaluation board

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Abstract. A digital positron lifetime setup based on DRS4 evaluation board designed at the Paul Scherrer Institute has been constructed and tested in the Positron annihilation laboratory Slovak University of Technology Bratislava. The high bandwidth, low power consumption and short readout time make DRS4 chip attractive for positron annihilation lifetime (PALS) setup, replacing traditional ADCs and TDCs. A software for PALS setup online and offline pulse analysis was developed with Qt,Qwt and ALGLIB libraries.

1. Introduction
Today, digital PALS setups are the usual upgrades from analog PALS systems in positron laboratories. Pulse processing with constant fraction discriminators and time to amplitude convertors are replaced by full software solution applied on digitized detector output signals. To process short nanosecond pulses relatively high bandwidth and sampling rate are needed. For this purpose expensive digital scopes [1], or special digitizer cards [2] were used. Now relatively cheaper cards like PicoScope digitizer with excellent triggering possibilities were used in [3]. Another possibility is to use a digitizer with switched capacitor arrays.

2. Experimental setup
The DRS4 evaluation board (EVB) [4] is based on the DRS4 Switched Capacitor Array chip. In order to simplify the EVB design, only four from eight available inputs are used to digitize the electronic pulses at the sampling speed of 5.12 GS/s. Analog bandwidth of the evaluation board is 700 MHz. This board is equipped with a trigger input and communicates with a computer, controlled by the data acquisition program through an USB interface. Four inputs channels enables to realize not only a standard two detector setup (fig.1), but also a three detector setup (fig.2). An obvious two detectors setup is used in standard PALS measurements. In our setup, the detectors are used in both - "Start” and "Stop” roles at the same time like in [5]. The constant fraction discriminator level for both detectors is set to trigger if pulses are coming from gamma quanta with energy higher than 400 keV. Measured Samples including the $^{22}_{\text{Na}}$ source are placed above the detectors in order to suppress coincidences of the annihilation rays, emitted in opposite directions. Additional lead shield is inserted between these two detectors to minimize unwanted gamma scattering. Final start, stop separation of the pulses is based on the software pulse amplitude discrimination.
The three detector setup is usually used to measure samples containing disturbing Co\textsuperscript{60}. Constant fraction discriminators are set so that the middle detector detects the "Start" pulses from 1275 keV photons, and the side ones the "Stop" pulses from 511 keV photons. The three detector setup has lower counting rate due to the need of triple coincidence. However better time resolution can be achieved on condition that the resulting lifetime is calculated as the average from the two lifetimes obtained by the three detector system \cite{1}. The BaF\textsubscript{2} cylindrical scintillators with size of 25 mm in diameter and 12 mm in height are coupled to XP2020Q photomultipliers, like in our analog setup and use a high voltage (HV) divider with dynode timing outputs \cite{6}. The fast dynode outputs of all detectors are transmitted to DRS4 evaluation board, that input range is from - 500 mV to 500 mV. The slow dynode outputs are amplified and inverted by Ortec VT120B amplifiers. Signal from these amplifiers feeds the constant fraction discriminators (CFD, Ortec 584). The blocking CFD outputs are summed in signal combiners consisting of a BNC tee connector and 6 dB passive attenuators. The summed signal from all CFD's feeds the leading edge discriminator (LE, Canberra 1428A. According to the LE level and chosen setup, two or three pulse coincidence is used. Standard positive pulse output signal from the LE discriminator is used as a trigger for the DRS4 evaluation module. The trigger rate obtained by this setup in two detector mode with a 1 MBq positron source is around 200 cps. Maximum count rate obtained by evaluation board is about 500 frames per second. One frame means 4 x 1024 measured samples (4 channels, 14 bits waves (2 bytes)). This should be due to limitation of the used USB controller. To obtain higher count rate, the WaveDream board \cite{7} with the same DRS4 chip, but Gigabit Ethernet interface should be considered.

Figure 1. Two detector PALS setup with DRS4 evaluation board.

Figure 2. Three detector setup.

3. Waveform collecting
For every trigger event the DRS4 evaluation board provides four waveforms, with length of 200 ns in 1024 samples at 5.2 GS/s sampling rate. These waveforms are transformed to floating values from 14 bit ADCs which are reading data from DRS4 capacitor arrays. Together with measured amplitude arrays, timing information are send to PC through USB2 data interface. The USB connection is implemented with a micro controller (Cypress\textregistered CY2C68013A). The high speed modus of the USB 2.0 bus allows for data transfer rates of more than 20 MB/sec.
4. Pulse processing
The data from the DRS4 evaluation board are in nonuniform sampled form. It means that there are small deviation from obvious uniform 192 ps sampling period. This deviation is measured during the calibration procedure provided by the evaluation board libraries and applied to time arrays.

It was reasonable to implement the digital constant fraction, which is one of the most used method to extract timing information from the detector pulse. Principle of the standard digital constant fraction is shown in the figure 3. The method is based on finding the time at which the rising pulse edge crosses 25% of its amplitude, calculated as a difference between the pulse baseline and the minimum of the pulse. Data from the digitizer are in discrete form, therefore to find this time, a data interpolation is required. The Cubic Spline method was found as usable for this purpose [8]. In our software, penalized regression spline provided by the ALGLIB C++ library [9] was applied in the area around 25% of the constant fraction level. The penalized regression spline is a 1-dimensional curve fitting algorithm which is suited for noisy fitting problems. To identify the pulse amplitude we used simple data average value from 10 samples taken before the pulses leading edge, and parabolic least squares fitting around peak to find minimum of the pulse. Finally lifetimes counted as differences between the start/stop times are summed in the PALS histograms.

![Figure 3. Digital constant fraction principle](image)

**Figure 3.** Digital constant fraction principle

![Figure 4. MS windows program QtPALS with user interface using Qt, and Qwt library.](image)

**Figure 4.** MS windows program QtPALS with user interface using Qt, and Qwt library.

5. QtPALS
To make software user friendly, the standard MS windows program written in C++ using Qt and Qwt libraries was developed. Software is separated into two parts. The first one is used to record samples from detectors, and is capable to do online analysis with collecting two PALS spectra and energy spectra for used detectors. The second part is used for offline analysis, and primarily is used to find optimal parameters for online QtPALS part (fig.4).

6. Results
The developed setup was tested with a reference Si sample and a $^{22}$Na source encapsulated in a kapton foil measurement. The best setup resolution (FWHM) in the two detector mode was 190 ps and in the three detector mode with lifetime averaging 148 ps.

7. Conclusion
In our laboratory different digitizers were tested as digital PALS setups in past. In comparison with them (Acqiris DP210, ZT4612), the DRS4 evaluation board is interesting according to its good price and properties which are suitable for processing fast detector pulses. According to the
obtained results, there was not significant difference between all of them. To make EVM module even better, delayed coincidence triggering should be delighted. Preliminary QtPALS software is developed under GNU license and is available at http://sourceforge.net/projects/qtpals

8. Acknowledgment
This article was granted by VEGA 1/0204/13 and VEGA 1/0366/12

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