A novel DC-DC converter and LDO cascaded circuit with improved dynamic response and loop stability

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Abstract  Presented is a new type of DC-DC converter and low dropout voltage regulator (LDO) cascaded circuit, which has improved dynamic response and loop stability. In this novel cascaded circuit, the gate voltage of the pass element of the LDO is quantized and compared with a target value to form an error value to finally control the feedback coefficient of the DC-DC converter. Meanwhile, the adjusting speed of this feedback coefficient can be changed dynamically through the gain compensator, which is minimized to obtain the best loop stability when approaching the steady-state and increased to achieve a fast transient response during large dynamic change. The testing results of the prototype designed to verify the feasibility show that the novel cascaded circuit can increase the response speed by 22 times and optimize the voltage ripple by 1.9 times.

Keywords: DC-DC converter, low dropout voltage regulator (LDO), dynamic response, loop stability

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

With the rapid growth of the demand for various portable devices and wearable electronic products, the demand for high-performance power management chips is also increasing. The efficiency of DC-DC converters can reach more than 90% [1, 2, 3, 4, 5, 6, 7, 8, 9]. However, its large output ripple limits its applications in sensitive electronic load where additional LDO is required to achieve low power noise and ripple [10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. Hybrid methods of switched-mode, switched-capacitor-mode DC-DC, low dropout voltage regulator (LDO) are proposed in recent years [20, 21, 22, 23, 24]. The traditional architecture of the analog switched-mode DC-DC converter with embedded LDO is shown in Fig. 1, the output voltage of the DC-DC converter must meet the dropout voltage requirement of the LDO under maximum load conditions, resulting in low efficiency under general load or light load [25, 26]. In the paper [27, 28, 29], several hybrid DC-DC and LDO cascading methods with digital controlled DC-DC converter shown as Fig. 2 are proposed to improve the performance. In [29], by using the pass element’s gate voltage of the LDO as the voltage detection point of the DC-DC converter loop, the

DC-DC converter can provide just enough dropout voltage for different loads. However, since the loop characteristics of the LDO are added to the feedback loop of the DC-DC converter, the two-loop characteristics become more complex which requires complicated loop compensation. Other papers such as [28, 30] also proposed the methods of adaptive change of the dropout voltage. Although the zero/pole of the LDO is avoided to be brought into the DC-DC converter loop, these dropout voltage adjustment methods are not the most efficient for the gate voltage of the LDO’s pass element is not detected directly.

In this paper, in order to improve dynamic response and loop stability further, a new type of DC-DC converter and LDO cascaded circuit with the gain compensator is proposed to change the speed of the feedback coefficient of the digital controlled DC-DC converter dynamically.

2. Working principle of the proposed circuit

The novel architecture of a digital controlled DC-DC converter and an LDO is illustrated in Fig. 3. A low-power ADC2 is used to quantize the gate voltage (V_{pgate}) of the PMOS pass element MP of the LDO. The output of the ADC2 compares with a target digital value to form the error
value that will be sent to a variable gain compensator (the input voltage of the ADC2 corresponding to this target digital value is the voltage target of the PMOS’s gate voltage). The output value of the gain compensator is normalized to form a feedback coefficient that finally controls the feedback of the DC-DC output voltage.

As shown in Fig. 3, the input value of the DC-DC converter’s control module can be written as:

\[ D_{dcdc, in} = \beta D_{dcdc, adc} \]  \hspace{1cm} (1)

where \( D_{dcdc, in} \) is the output value of ADC1 and \( \beta \) is the feedback coefficient that can be expressed as:

\[ \beta = (2^N - D_{comp})/2^N \]  \hspace{1cm} (2)

where \( N \) is the bit number of the compensator output \( D_{comp} \), which can be expressed as:

\[ D_{comp} = k(D_{ldo, adc} - D_{ldo, target})H(z) \]  \hspace{1cm} (3)

where \( D_{ldo, adc} \) is the output of ADC2, \( D_{ldo, target} \) is the target digital value of the PMOS’s gate voltage and \( H(z) \) is the loop filter transfer function, and the loop gain parameter \( k \) can be expressed as:

\[ k = f(|\Delta|) = f(|D_{ldo, adc} - D_{ldo, target}|) \]  \hspace{1cm} (4)

where \( f(|\Delta|) \) is a compensation function related to \( |D_{ldo, adc} - D_{ldo, target}| \).

According to (1), the value of \( \beta \) reflects the corresponding response speed during load switching. According to (2)–(4), when \( |D_{ldo, adc} - D_{ldo, target}| \) becomes large (> 0.2) suddenly (load switching), \( k \) needs to be a large number correspondingly to accelerate the dynamic response of the DC-DC converter.

When \( |D_{ldo, adc} - D_{ldo, target}| \) is close to zero (≤ 0.2), \( k \) needs to be a small number dramatically such that the two loops behave as two approximately independent loops. This conclusion can be obtained through the following proof process.

The complete small-signal model of the proposed circuit is illustrated in Fig. 4. The loop gain of the LDO can be expressed as:

\[ G_{LDO} = g_m Z_o H(s) \]  \hspace{1cm} (5)

where \( Z_o \) is the output impedance of the LDO which can be expressed as:

\[ \frac{Z_o}{s} = \frac{R_{out}}{1 + \frac{s}{\omega_{op}}} \]  \hspace{1cm} (6)

And \( A(s) \) is the gain of the error amplifier which can be expressed as:

\[ A(s) = \frac{G_{op}}{1 + \frac{s}{\omega_{op}}} \]  \hspace{1cm} (7)

The gain of the gain compensator can be expressed as:

\[ K_{comp}(s) = \frac{K}{s} \]  \hspace{1cm} (8)

The small-signal of \( \beta \) can be expressed as:

\[ \hat{\beta} = \hat{V}_{\alpha, dcdc} \frac{K_{comp}(s)G_{LDO}}{1 + G_{LDO}} \]  \hspace{1cm} (9)

Then substituting (5)–(8) into (9), we can get:

\[ \hat{\beta} = \hat{V}_{\alpha, dcdc} \frac{K}{s} \cdot \frac{1}{1 + \frac{s}{\omega_{LDO, target}}} \]  \hspace{1cm} (10)

In the main DC-DC loop, the input value \( D_{dcdc, in} \) before the PID compensator is equal to the sum of the steady-state value and the change value which can be expressed as:

\[ \hat{V}_{\alpha, dcdc} \cdot MK_{LDO} \cdot K_{B, steady} + \hat{\beta} \]  \hspace{1cm} (11)

According to (11), when \( K \) is very small, the second term (second-order term) can be ignored at small-signal mode. Then the input value before the PID compensator can be expressed as:

\[ \hat{V}_{\alpha, dcdc} \cdot MK_{LDO} \cdot K_{B, steady} \]  \hspace{1cm} (12)

At this time, the characteristic of the DC-DC loop has nothing to do with LDO. In other words, when \( K \) is very small, the two loops (DC-DC loop and LDO loop) behave as two approximately independent loops. Thus, this topology can maintain the two loops’ AC stability when approaching steady-state, and has a quick transient response for a dynamic change.

In order to realize the special properties of \( k \), the compensation function \( f(|\Delta|) \) can be expressed as:

\[ k = f(|\Delta|) = \frac{4.5}{1 + e^{-1000(|\Delta| - 0.23)}} + 0.5 \]  \hspace{1cm} (13)

And the waveform of the compensation function \( f(|\Delta|) \) is illustrated in Fig. 5 showing that the value of \( k \) can be switched from 0.5 to 5 according to \( |D_{ldo, adc} - D_{ldo, target}| \).
3. Simulation results

The Simulink block of the proposed cascaded circuit is shown in Fig. 6. And three conditions are simulated to verify the improvement of the proposed cascaded circuit as shown in Fig. 7.

When $k$ is a fixed value and a small number ($=0.5$), the simulation result is shown as Fig. 7(a). At this time, the response speed of the circuit is slow ($\Delta t=0.25\text{ms}$) when the load is switched from 200mA to 300mA, because the corresponding feedback coefficient $\beta$ is very small.

When $k$ is a fixed value and a large number ($=5$), the simulation result is shown as Fig. 7(b). The response speed of the circuit becomes fast ($\Delta t=0.03\text{ms}$) when the load is switched from 225mA to 300mA, because the corresponding feedback coefficient $\beta$ becomes larger. However, it can be seen from the previous analysis that the characteristic of the DC-DC loop will be affected by LDO when $k$ is large. Thus, the loop stability of DC-DC is poor at this time.

The simulation result is shown in Fig. 7(c) when the value of $k$ is determined by the gain compensation. It is shown that the circuit can maintain good stability and fast response speed at the same time.

4. Experimental results

A prototype is also designed to verify the feasibility of the system as shown in Fig. 8. The test system employs NCP302025 as the integrated driving circuit of the DC-DC converter, FDV304P as the pass element, and LT1719 as the EA of the LDO. And two ADCs (ADC12020) are employed to provide 8-bit quantization for the gate voltage of the pass element and $V_{o,\text{DCDC}}$. The PID compensator and DPWM are realized through FPGA. A load current step between 225mA and 300mA is applied to the prototype with 6V input voltage.

Fig. 9(a) shows the case for fixed $k=0.5$ where the ripple voltage of the LDO is 17mV@300mA and 13mV@225mA, while the output voltage of the DC-DC converter varies from...
3.30V to 3.05V. And when the load is switched, the response time is 2.01ms.

Fig. 9(b) shows the case for fixed $k = 5$ where the ripple voltage of the LDO is 25mV@300mA and 21mV@225mA, and when the load is switched, the response time is only 104μs.

Fig. 9(c) shows the case for $k$ determined by the gain compensation. The response time of the DC-DC converter is only 88μs which is much smaller than the case for $k = 0.5$. While the ripple voltage of the LDO is 15mV@300mA and 13mV@225mA, the circuit with gain compensation optimizes the voltage ripple by 1.9 times.

5. Conclusion

A feedback coefficient obtained from quantizing and compensating the pass element’s gate voltage of the LDO can be used to control the DC-DC converter to provide the adaptive dropout voltage for the cascaded LDO. Furthermore, by adaptively changing the gain of the compensator linking the two loops, good loop stability and fast transient response are both achieved in this system when approaching steady-state and undergoing large dynamic change, respectively.

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