Abstract—The emerging brain-inspired computing paradigm known as hyperdimensional computing (HDC) has been proven to provide a lightweight learning framework for various cognitive tasks compared to the widely used deep learning-based approaches. Spatio-temporal (ST) signal processing, which encompasses biosignals such as electromyography (EMG) and electroencephalography (EEG), is one family of applications that could benefit from an HDC-based learning framework. At the core of HDC lie manipulations and comparisons of large bit patterns, which are inherently ill-suited to conventional computing platforms based on the von-Neumann architecture. In this work, we propose an architecture for ST signal processing within the HDC framework using predominantly in-memory compute arrays. In particular, we introduce a methodology for the in-memory hyperdimensional encoding of ST data to be used together with an in-memory associative search module. We show that the in-memory HDC encoder for ST signals offers at least 1.80× energy efficiency gains, 3.36× area gains, as well as 9.74× throughput gains compared with a dedicated digital hardware implementation. At the same time it achieves a peak classification accuracy within 0.04% of that of the baseline HDC framework.

Index Terms—Hyperdimensional computing, In-memory computing, Biosignal processing

I. INTRODUCTION

Almost all breakthroughs in artificial intelligence in the last decade are characterized by an underlying machine learning model that entails a higher complexity in terms of the number of operations and parameters compared to contemporary models. Such increased model complexity demands more energy to perform training and inference tasks. Nevertheless, the human brain, with its far-reaching cognitive capabilities, consumes several orders of magnitude less power. This disparity has paved the way to exploring brain-inspired alternatives. Hyperdimensional computing (HDC) [1] is one promising brain-inspired computing approach that relies on representing entities using high-dimensional (up to 10,000 dimensions) vectors called hypervectors. Similarly to the brain, where representations are spread across thousands of randomly originated neurons, a set of (pseudo)random orthogonal hypervectors forms the basis in the HDC framework. These hypervectors are then combined and compared using a well-defined set of algebraic operations to derive representations for composite entities and to find similarities, respectively.

HDC has been deployed in a diverse set of application domains, for instance in solving Raven's progressive matrices [2], analogical reasoning [3], natural language processing [4], robotics [5], [6], text classification [7]–[10], activity recognition [11], DNA sequencing [12], and biosignal processing [13]–[18] (see [19] for an overview).

A promising application domain for HDC is the spatio-temporal (ST) processing of signals, acquired by EMG sensors for example. The corresponding HDC algorithm was presented in [13], and later scaled up for high-density flexible EMG sensors [14], [18]. The same HDC algorithm has been used in a variety of applications such as EEG [16], iEEG [17], ExG [19] in general, as well as speech recognition [20], delivering higher classification accuracy than the established approaches. ST signal processing differs from other classes of applications because numerical data sequences received from multiple channels within a certain time window are considered as the input. Due to often being deployed at the edge of the Internet of Things and the confidential nature of the input data, the ST applications identified above could benefit immensely from energy-efficient hardware platforms.

Earlier works address ST HDC signal processing in low-power hardware platforms, such as PULP [15] and ARM Cortex-A53 [21]. For example, PULP-HD [15] describes the implementation of the ST HD encoder on multiple cores in a PULP cluster for achieving a target of 10 ms detection latency in real-time. Nevertheless, the energy efficiency could be improved further by using in-memory computing approaches [10], [22], [23]. In-memory computing is an emerging paradigm where the physical attributes of memory devices are exploited to compute in place [24]. Operations that require manipulation and comparison of large strings of bit patterns, which are at the core of the HDC framework, are particularly well suited for in-memory computing [10].

In this work, we propose an in-memory computing-based system for ST signal processing with HDC. An illustration of the system is given in Fig. [1] taking the EMG-based hand gesture recognition as a use case. Compared to prior work on in-memory HDC encoding [10], we present a novel in-memory computing HDC encoding architecture tailored for ST inputs. When coupled with an in-memory associative memory search module, such as the one presented in [10], we get a complete in-memory HDC processor for ST signal processing. We derive classification accuracy results from simulations using a statistical model of phase-change memory (PCM)
crossbar arrays. Furthermore, we estimate the throughput, area, and energy efficiency of the in-memory ST HDC encoder and compare it with a dedicated digital encoder as well as a ST HDC encoder running on a low-power general purpose compute platform, PULP-HD [15].

II. ALGORITHM
A. Conventional ST HDC encoding algorithm
In the conventional ST HDC encoding algorithm [13], the input acquired from each channel goes through several pre-processing steps [15] and is converted to a stream of discrete time samples. An HDC encoder maintains a record of $N$ consecutive time samples from $M$ channels to generate an encoded $N$-gram hypervector embedding defined as:

$$f : \{s_{n,m}\}^{N \times M} \in \{l_1, l_2, ..., l_L\}^{N \times M} \to G \in \{0, 1\}^D,$$  \hspace{1cm} (1)

where $n \in \{1, 2, ..., N\}$ is the relative time index, $m \in \{1, 2, ..., M\}$ denotes the source channel index and $\{l_1, l_2, ..., l_L\}$ are the $L$ discrete quantization levels given in ascending order $l_1 < l_2 < ... < l_L$. The output of the embedding function $G$ is a D-dimensional binary hypervector.

First, the encoder projects the sample values $s_{n,m}$ to a high dimensional space using a so-called continuous item memory ($CiM$) [13]. As opposed to assigning quasi-orthogonal hypervectors to every unique discrete sample value, the $CiM$ sets the Hamming distance ($HamD$) between two vectors to be proportional to the absolute difference between the corresponding sample values. This is achieved by choosing quasi-orthogonal hypervectors for the minimum and maximum levels $l_1$ and $l_L$, and hypervectors corresponding to the intermediate levels that satisfy:

$$HamD(CiM(l_i), CiM(l_j)) = \text{Floor} \left( \frac{|D_{l_i - l_j}|}{2|l_L - l_1|} \right)$$  \hspace{1cm} (2)

The $CiM$-projected vectors are then bound to the relevant channel ID hypervector $E_m$. The channel ID hypervectors are stored in an item memory ($IM$) and are quasi-orthogonal. The channel-bound hypervectors are given by $I_{m,n} = CiM(s_{n,m}) \ast E_m$, where $\ast$ denotes the element-wise XOR binding operation. The channel-bound hypervectors are then bundled together to produce spatial hypervectors

$$S_n = \text{Majority}(I_{1,n}, I_{2,n}, ..., I_{M,n}),$$  \hspace{1cm} (3)

where, for each dimension, the majority function outputs $I(0)$ if the majority of channels have $I(0)$.

The spatial hypervectors $S_1, S_2, ..., S_N$ then enter a temporal encoding stage, which outputs the final encoded $N$-gram $G$ according to the following equation:

$$G_t = \rho^{N-1}S_1 \ast \rho^{N-2}S_2 \ast ... \ast S_N$$  \hspace{1cm} (4)

where $t$ is the time step at which the $N^{th}$ sample of the current data record enters the system, and $\rho$ is the vector permutation operator, which is implemented as a circular right shift.

During the training phase, $N$-grams collected from the same class are further bundled to produce class prototype hypervectors $P_c$, where $c \in \{1, 2, ..., C\}$, and $C$ is the number of classes. During the inference phase, the $N$-gram produced from the same encoder is called a query hypervector $Q$ and used to measure binary dot product similarity against each of the prototype hypervectors $P_c$. The class with the highest similarity is selected as the predicted class.

B. Adaptations to suit in-memory computing
We propose several adaptations to the conventional algorithm to suit in-memory computing. First, all channel-bound hypervectors are pre-computed and unrolled using:

$$I'_m = CiM(l) \ast E_m \hspace{1cm} \forall l \in \{1, ..., L\}, \forall m \in \{1, ..., M\}$$  \hspace{1cm} (5)

Fig. 1. Concept of in-memory hyperdimensional encoding of spatio-temporal signals within the application of hand gesture recognition. First, the EMG signals are acquired from the electrodes connected to different parts of the subject’s arm. After a pre-processing step, the data from different channels are embedded into one hypervector using spatial encoding and temporal encoding in a first memristive crossbar array, which is the focus of this work. The resulting query vector is passed to a second crossbar array to perform the associative memory search. The final result collected from the peripheral of the second crossbar predicts the class of the hand gesture.

1. Preprocessing
2. Spatio-temporal Encoding
3. In-memory Spatiotemporal HD Encoding
4. On-chip Accelerator
5. Crossbar I
6. Crossbar II
7. Peripheral
8. Gesture Classes
9. Comparator
10. Comparator
11. $Q, P_1, P_2, ..., P_C$
12. $Q, P_1, P_2, ..., P_C$
13. $Q, P_1, P_2, ..., P_C$
14. $Q, P_1, P_2, ..., P_C$
and stored in the memristive crossbar array. The other major modification to the conventional ST encoding algorithm is that the temporal encoding is performed immediately on each of the channel-bound hypervectors to obtain intermediate temporal hypervectors $T_m$ as given in:

$$T_m = \rho^{-1} I_{1,m} \ast \rho^{-2} I_{2,m} \ast \ldots \ast I_{N,m}$$  \hspace{1cm} \text{(6)}$$

instead of waiting for the spatial bundling given in (5). Finally, the hypervectors $T_m$ are bundled to produce the adapted $N$-gram hypervector $G'$, given by:

$$G'_m = \text{Majority}(T_1, T_2, \ldots, T_M)$$  \hspace{1cm} \text{(7)}$$

In summary, compared to the ST encoder in [13], the proposed in-memory ST encoding algorithm pre-computes channel-bound hypervectors and pushes the bundling portion of the spatial encoding step downstream of the temporal encoding step. This offers further flexibility to set individual quantization levels and $N$-gram sizes per channel, which is not possible with the conventional encoder. This is a useful feature to exploit channel specific spatial and temporal dynamics.

III. ARCHITECTURE

The architecture of the in-memory ST HDC encoder is shown in Fig. 2. It consists of a memristive crossbar array and a few peripheral circuits, namely a circular buffer, a binder, and a bundler. The circular buffer maintains the last $N$ samples and reading them sequentially. It has $M$ write pointers ($wp_1, \ldots, wp_M$), synchronized to each one of the low-frequency external input channels that write data in parallel to the next allotted locations in the buffer. There is a single read pointer that is synchronized to the internal clock frequency which is set at least $N \cdot M \times D$ faster than the external frequency to avoid any data loss. The read pointer ($rp$) traverses the whole input data record sequentially: it samples in chronological order within each channel and repeats over all channels.

As shown in Fig. 2, the pre-computed channel-bound hypervectors $H'_m$ given in (5) are stored along the rows of the $M \cdot L \times D$ crossbar array. This allows us to save $D \cdot N \cdot M$ XOR operations per input data record. Performing temporal encoding on each channel separately allows us to reduce the number of intermediate buffers in the digital domain that must possess read/write capability at the expense of additional read-only storage in the PCM crossbar array. This is an acceptable trade-off because the PCM device consumes approximately 23 fJ of energy per read operation [25]. This is just a fraction of the energy incurred by digital read/write buffers. Furthermore, thanks to their non-volatile nature, PCM devices do not consume energy when retaining their content in idle mode.

The output of the crossbar array is connected to an array of sense amplifiers. Sequential processing of the data record allows time sharing the sense amplifier array and the downstream binder module, allowing us to save a significant amount of energy and area in the peripherals. The binder module consists of an array of $D$ XOR gates daisy-chained with $D$ registers, which collectively implement (6).

The bundler module in the architecture implements (7). An optional scan chain, which propagates a random hypervector generated bit-by-bit from a linear feedback shift register, is activated at the start of the encoding cycle when the number of input channels is even, with ties that are broken randomly. The majority function is implemented as an array of $\log_2 M$-bit accumulators, followed by an array of comparators whose reference is set at $ceil((M + 1)/2) - 0.5$.

The controller module receives the encoding parameters and coordinates the flow across the rest of the modules. For example, it communicates the start/end addresses for each of the write pointers, the offset value added to circular buffer read data to derive the row address in the crossbar array, when to update the 1-bit register array in the binder module, when to update accumulators in the bundler, etc.

IV. RESULTS AND DISCUSSION

A. Experimental setup

The proposed in-memory ST HDC architecture is benchmarked on the EMG hand gesture recognition dataset [13]. It includes data acquired from five subjects who perform five classes of gestures. The data is sampled at a 500 Hz frequency via four EMG electrodes attached to each subject’s forearm. The class label and channel readings are provided at each time frame. We use 25% of the 175× down-sampled data to train a 10,000-D HDC model for each subject and test on 800 queries on average per subject. The result is averaged across the subjects to obtain the classification accuracy. For PCM simulations, the statistical model described in [10] is used, which captures non-ideal effects such as spatial and temporal variations in the PCM crossbar array.

B. Classification accuracy results

Fig. 3 shows the classification accuracy obtained from an in-memory ST encoder running in software, as well as the same encoder simulated using the statistical model, and comparing these results with the baseline ST encoder [13]. In all three models of encoders, the in-memory associative memory search module is also simulated with the statistical model. The
proposed in-memory ST encoder achieves a peak accuracy of 98.9% (see Fig. 3(a)) when \( N=9, L=15 \). This is only 0.04% lower than the peak accuracy in the baseline ST encoder. It is also a 1.1% improvement over the peak accuracy of 97.8% reported in the reference encoder [13], which uses the binding result of two channels to break ties while performing the associative memory search using Hamming distance.

As the \( N \)-gram size decreases, the spatial encoding plays a more prominent role than the temporal encoding. Thus, the higher accuracy delivered by the in-memory ST encoder compared to the conventional ST encoder (see Fig. 3(a)) for smaller \( N \)-gram sizes can be explained by the spatial bundling operation being relocated downstream in the in-memory ST encoder. This allows retaining more useful spatial information in the encoded \( N \)-gram hypervector.

Fig. 3(b) shows that the in-memory encoder simulated with the statistical model exhibits an increasing accuracy drop, compared to the same encoder running in software, as the quantization levels increase. This is because as the quantization levels are increased, the PCM crossbar array size increases linearly, thereby amplifying the negative effect of spatial PCM variations on the classification accuracy. However given that the in-memory ST encoding operations in Equations (5) to (7) involve element-wise operations, or operations that involve neighboring elements, the crossbar array can be easily split into several realistic size 26 subarrays with simple single wire connectivity between subarray peripherals. This facilitates the silicon realization with negligible additional cost in terms of energy and area, as well as the mitigation of the effect of PCM spatial variations by compensating for subarray level conductance variation.

### C. Energy efficiency study and benchmark

We performed an energy efficiency study of the in-memory ST encoder. The binary PCM device specifications given in [10] are used as the reference for obtaining power and timing numbers of the crossbars. The power and timing numbers for the digital peripherals are obtained from component-wise simulations of a post-synthesis netlist generated with 65nm CMOS technology. For comparison, we considered an equivalent digital ST encoder operating entirely in CMOS, whose power and timing numbers are obtained from a component-wise simulation of the post-synthesis netlist generated at the same technology node. Both digital peripherals and the equivalent CMOS encoder operate at 440 MHz and 1.2 V supply voltage.

We observe that the in-memory ST encoder is able to produce 31.5M, 18.9M, and 10.5M \( N \)-grams/s for \( N \)-gram sizes of 3, 5, and 9, respectively, which is a throughput improvement of 9.74× over the digital counterpart and a 0.28M× improvement over the 10 ms fixed latency PULP-HD [15]. The total area of the in-memory ST encoder varies from 0.37 to 0.44 and 0.51 \( mm^2 \) when quantization levels are set to 3, 12 and 21, respectively. This is a 3.36×, 5.46×, and 6.97× area reduction, respectively, compared to the digital CMOS ST encoder. When breaking down the area numbers further we find that, irrespective of the number of quantization levels, a fixed area of 0.32 \( mm^2 \) is occupied by the digital peripheral logic including the circular buffer, the binder and the bundler; another area of 0.02 \( mm^2 \) is occupied by the row decoders and the sense amplifiers; while the rest of the area is taken by the PCM device array itself.

We estimated the energy efficiency of the in-memory ST encoder and compared it with the digital ST encoder as shown in Fig. 4. The in-memory ST encoder achieves a peak energy efficiency of 75.1M \( N \)-grams/s/W with \( N=3 \) and \( L=3 \). The total energy required for encoding an \( N \)-gram using this configuration is 13.3 nJ, 91.4% of which are spent on digital peripheral circuits, 8.4% on sense amplifiers/row decoders, and a mere 0.12% on PCM devices. This results in a 1.80× energy efficiency gain compared to a similarly configured digital ST
encoder. The gain improves to a maximum of $8.83 \times 10^4$ as the N-gram sizes and quantization levels are increased (see Fig. [4]).

Table II presents physical and performance characteristics of 1-core and 4-core PULP-HD encoders compared with a dedicated digital CMOS encoder and the proposed PCM-based in-memory ST encoder with the same parameter configuration ($N = 3, L = 21$). The energy required for N-gram encoding is reduced from the $\mu J$ range for the PULP-HD implementations to the $n J$ range for the dedicated CMOS and PCM-based in-memory encoders. In summary, when compared with 1-core and 4-core PULP-HD encoders, the in-memory ST encoder achieves $1320 \times 10^4$ and $284 \times 10^4$ higher energy efficiency, respectively.

V. CONCLUSION

In this paper, we have demonstrated HDC encoding on spatio-temporal signals using in-memory computing techniques on memristive crossbar arrays. This approach allows selecting separate parameter combinations for each channel, further enhancing the flexibility of the encoding process. By simulating our architecture with a phase-change memory statistical model, we obtain a peak classification accuracy of 98.9% (within 0.04% of the baseline), while achieving $1.80 \times 10^3$ higher energy efficiency over a dedicated digital CMOS encoder and a $284 \times 10^4$ gain energy efficiency over an encoder running on a low-power general purpose computing platform.

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REFERENCES

[1] P. Kanerva, “Hyperdimensional Computing: An Introduction to Computing in Distributed Representation with High-Dimensional Random Vectors,” Cognitive Computation, vol. 1, no. 2, pp. 139–159, 2009.
[2] B. Emmrui et al., “Analogical mapping and inference with binary spatter codes and sparse distributed memory,” in The 2013 International Joint Conference on Neural Networks (IJCNN), 2013, pp. 1–8.
[3] P. Kanerva, “What we mean when we say ‘what’s the dollar of mexico?’: Prototypes and mapping in concept space,” in AAAI Fall Symposium: Quantum Informatics for Cognitive, Social, and Semantic Processes, 2010, pp. 2–6.
[4] P. Alonso et al., “Hyperembed: Tradeoffs between resources and performance in nlp tasks with hyperdimensional computing enabled embedding of n-gram statistics,” arXiv preprint arXiv:2003.01821, 2020.
[5] A. Mitrokhin et al., “Learning sensorimotor control with neuromorphic sensors: Toward hyperdimensional active perception,” Science Robotics, vol. 4, no. 30, 2019.
[6] M. Hersche et al., “Integrating event-based dynamic vision sensors with sparse hyperdimensional computing: A low-power accelerator with online learning capability,” in Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design, ser. ISLPED ’20. New York, NY, USA: Association for Computing Machinery, 2020, p. 169–174.
[7] A. Joshi et al., “Language geometry using random indexing,” in Quantum Interaction, J. A. de Barros et al., Eds. Cham: Springer International Publishing, 2017, pp. 265–274.
[8] A. Rahimi et al., “A robust and energy-efficient classifier using brain-inspired hyperdimensional computing,” in Proceedings of the 2016 International Symposium on Low Power Electronics and Design, ser. ISLPED ’16. New York, NY, USA: ACM, 2016, pp. 64–69.
[9] F. R. Najafabadi et al., “Hyperdimensional computing for text classification,” ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), March 2016.
[10] G. Karunaratne et al., “In-memory hyperdimensional computing,” Nature Electronics, vol. 3, no. 6, pp. 327–337, 2020.
[11] O. Rasänen et al., “Modeling dependencies in multiple parallel data streams with hyperdimensional computing,” IEEE Signal Processing Letters, vol. 21, no. 7, pp. 899–903, 2014.
[12] M. Imani et al., “Hdna: Energy-efficient dna sequencing using hyperdimensional computing,” in 2018 IEEE EMBS International Conference on Biomedical Health Informatics (BHI), 2018, pp. 271–274.
[13] A. Rahimi et al., “Hyperdimensional biosignal processing: A case study for emg-based hand gesture recognition,” in 2016 IEEE International Conference on Rebooting Computing (ICRC), 2016, pp. 1–8.
[14] A. Moin et al., “An emg gesture recognition system with flexible high-density sensors and brain-inspired high-dimensional classifier,” in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018, pp. 1–5.
[15] F. Montagna et al., “Pulp-hd: Accelerating brain-inspired high-dimensional computing on a parallel ultra-low power platform,” in Proceedings of the 55th Annual Design Automation Conference, ser. DAC ’18. New York, NY, USA: ACM, 2018, pp. 111:1–111:6.
[16] A. Rahimi et al., “Hyperdimensional computing for noninvasive brain-computer interfaces: Blind and one-shot classification of eeg error-related potentials,” 10th EAI Int. Conf. on Bio-inspired Information and Communications Technologies, 2017.
[17] A. Barrello et al., “One-shot learning for eeg seizure detection using end-to-end binary operations: Local binary patterns with hyperdimensional computing,” in 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2018, pp. 1–4.
[18] A. Moin et al., “A wearable biosensing system with in-sensor adaptive machine learning for hand gesture recognition,” Nature Electronics, vol. 4, no. 1, pp. 54–63, 2021.
[19] A. Rahimi et al., “Efficient biosignal processing using hyperdimensional computing: Network templates for combined learning and classification of eeg signals,” Proceedings of the IEEE, vol. 107, no. 1, pp. 123–143, 2019.
[20] M. Imani et al., “Voicehd: Hyperdimensional computing for efficient speech recognition,” in 2017 IEEE International Conference on Rebooting Computing (ICRC), 2017, pp. 1–8.
[21] Y. Kim et al., “Efficient human activity recognition using hyperdimensional computing,” in Proceedings of the 8th International Conference on the Internet of Things, ser. IOT ’18. New York, NY, USA: Association for Computing Machinery, 2018.
[22] H. Li et al., “Device-architecture co-design for hyperdimensional computing with 3d vertical resistive switching random access memory (3d vram),” in 2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2017, pp. 1–2.
[23] T. F. Wu et al., “Brain-inspired computing exploiting carbon nanotube fets and resistive ram: Hyperdimensional computing case study,” in 2018 IEEE International Solid - State Circuits Conference - (ISSCC), 2018, pp. 492–494.
[24] A. Sebastian et al., “Memory devices and applications for in-memory computing,” Nature Nanotechnology, vol. 15, pp. 529–544, 2020.
[25] S. R. Nandakumar et al., “Mixed-precision deep learning based on computational memory,” Frontiers in Neuroscience, vol. 14, p. 406, 2020.
[26] M. Le Gallo et al., “Mixed-precision in-memory computing,” Nature Electronics, vol. 1, no. 4, pp. 246–253, 2018.