We propose and numerically simulate novel reconfigurable logic gates employing spin metal–oxide–semiconductor field-effect transistors (spin MOSFETs). The output characteristics of the spin MOSFETs depend on the relative magnetization configuration of the ferromagnetic contacts for the source and drain, that is, high current-drive capability in parallel magnetization and low current-drive capability in antiparallel magnetization [S. Sugahara and M. Tanaka: Appl. Phys. Lett. 84 (2004) 2307]. A reconfigurable NAND/NOR logic gate can be realized by using a spin MOSFET as a driver or an active load of a complimentary MOS (CMOS) inverter with a neuron MOS input stage. Its logic function can be switched by changing the relative magnetization configuration of the ferromagnetic source and drain of the spin MOSFET. A reconfigurable logic gate for all symmetric Boolean functions can be configured using only five CMOS inverters including four spin MOSFETs. The operation of these reconfigurable logic gates was confirmed by numerical simulations using a simple device model for the spin MOSFETs. [DOI: 10.1143/JJAP.43.6032]
complimentary MOS (CMOS) inverter with a neuron MOS (vMOS) input stage. A reconfigurable logic gate for all symmetric Boolean functions (AND, OR, XOR, NAND, NOR, XNOR, all-"0" and all-"1") can also be configured by using only five CMOS inverters including four spin MOSFETs. The operation of these reconfigurable logic gates was analyzed with the numerical circuit simulator HSPICE using a simple device model for spin MOSFETs.

2. Device Model for Spin MOSFETs

A simple device model was applied to the spin MOSFET for performing logic simulations. Since \( \beta(mos) = \frac{n}{dI/dVG} \) of the spin MOSFET shows an approximately linear increase with increasing gate bias \( V_{GS} \), when \( V_{GS} \) is higher than the threshold voltage \( V_t \), the output characteristics (the drain current \( I_D \)) of the spin MOSFET can be approximated as \( I_D = \beta(V_{GS} - V_t)^2 \), where \( \beta \) is the gain coefficient. This means that the ordinary device models for conventional MOSFETs are useful for the spin MOSFET. Assuming that the drain current of the spin MOSFET has the same function formula as that of the gradual channel approximation for MOSFETs, the static transfer characteristics of the logic gates presented in this paper can be expressed by the gain coefficient ratio of their load and driver transistors (the transfer characteristics of a conventional CMOS inverter are described in the same manner). Thus, the absolute drain current values of the spin MOSFETs and conventional MOSFETs are not needed in the static operation analysis of the presented logic gates. Instead, the gain coefficient ratios of the load and driver transistors are used in the following simulations.

To reproduce the magnetization-configuration-dependent output characteristics of the spin MOSFET, large and small gain coefficients are introduced into the device model of a single spin MOSFET, that is, the spin MOSFET in parallel (antiparallel) magnetization is represented by a MOSFET with a large (small) gain coefficient \( \beta^P (\beta^{AP}) \). Since the gain coefficient of MOSFETs is proportional to the device dimension ratio \( W/L \) (where \( W \) is the channel width and \( L \) the channel length), \( \beta^P \) and \( \beta^{AP} \) for a single spin MOSFET are separately realized by the appropriate choice of \( W/L \) values for parallel and antiparallel magnetizations. Note that although the gate capacitance of this spin MOSFET model is changed according to the \( W/L \) values for parallel and antiparallel magnetizations, this variation of the gate capacitance can be neglected when using a vMOS input stage, as described later.

The numerical simulations of the presented logic gates were performed with a commercially available HSPICE simulator that is based on a sophisticated device model to reproduce transistor characteristics and circuit performance with reasonable accuracy. The design rule and the supply voltage \( V_{DD} \) used for the simulations were 0.35 \( \mu \)m and 3.3 V, respectively, although the design rule of sub-100 nm and \( V_{DD} \) of 1–1.5 V would be more realistic for the spin MOSFET.\(^1\) The threshold voltage \( V_t \) of the \( n \)-channel and \( p \)-channel MOSFETs were 1.2 and 1.3 V, respectively. These values were also used for the spin MOSFET for simplicity. Note that \( V_t \sim 1 \text{ V} \) for \( V_{DD} = 3.3 \text{ V} \) can be scaled to \( V_t = 0.2–0.3 \text{ V} \) for \( V_{DD} = 1–1.5 \text{ V} \) which is a favorable value for sub-100-nm-scale spin MOSFETs.\(^1\) Red and blue curves in Fig. 1(b) show the output characteristics of this spin MOSFET model in parallel and antiparallel magnetizations, respectively, where the \( W/L \) values are 8.75 for parallel magnetization and 1.25 for antiparallel magnetization and the resulting \( \beta^P/\beta^{AP} \) value is 7.0. The gain coefficient ratio \( \beta^P/\beta^{AP} \) of the spin MOSFET is a suitable parameter for controlling the device performance, since \( \beta^P/\beta^{AP} \) directly determines the magnetization-configuration-dependent output characteristics of the spin MOSFET as well as the operational margin of the reconfigurable logic gates presented in this paper. Although the operational margin depends on the ratio \( \beta^P/\beta^{AP} \), the appropriate range of \( \beta^P/\beta^{AP} \) seems to be extremely wide, 3–1000, as estimated from our simulated results. Note that the operating speed and power dissipation of the proposed reconconfigurable logic gates also depends on the gain coefficient ratio \( \beta^P/\beta^{AP} \), e.g., a large \( \beta^P/\beta^{AP} \) ratio results in small power dissipation at the expense of the operating speed.

3. Reconfigurable AND/OR Gate

Figure 2 shows a reconfigurable NAND/NOR gate for the output \( V_{O1} \), which acts as an AND/OR gate for the output \( V_{O2} \). The NAND/NOR gate can be realized by using a
$p$-channel MOSFET as the active load ($Q_1$) and an $n$-channel spin MOSFET as the driver ($Q_2$) of CMOS inverter with a $n$MOS input stage having two binary inputs ($A$ and $B$). Here, the gain coefficients of $Q_1$ and $Q_2$ in parallel and antiparallel magnetizations are expressed by $\beta_1^p$, $\beta_2^p$ and $\beta_1^{AP}$, respectively, and these are set to satisfy $\beta_2^{AP} < \beta_1^p < \beta_2^p$, as discussed later. The function of a CMOS inverter $G_0$ (whose logic threshold voltage is set at 1/2$V_{DD}$) is also described later. Note that this logic gate can also be configured with a $p$-channel spin MOSFET as $Q_1$ and an $n$-channel MOSFET as $Q_2$, and with $p$- and $n$-channel spin MOSFETs as $Q_1$ and $Q_2$, respectively.

The $n$MOS input stage has a floating gate coupled capacitively with two input gates. The floating-gate voltage $V_{FG}$ of the $n$MOS is given by$^9$)

$$V_{FG} = \frac{C_A A + C_B B}{C_0 + C_A + C_B} = \frac{A + B}{2},$$

where $C_0$ denotes a capacitance between the substrate and the floating gate, $C_A$ and $C_B$ represent a coupling capacitance for inputs $A$ and $B$, and we assume $C_A = C_B$ and $C_{AB} \gg C_0$. The binary input voltages of 0 and $V_{DD}$ for $A$ and $B$ can be simply expressed by “0” and “1” which are measured units in units of $V_{DD}$ (hereafter, quotation marks are used to denote values measured in units of $V_{DD}$). When the input combinations are $A = B = “0”$ and $A = B = “1”$, $V_{FG}$ is “0” and “1”, respectively. When one of the two inputs is “1” (i.e., $A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$), $V_{FG}$ is “1/2”.

Red and blue dotted curves in Fig. 2(b) show the transfer characteristics ($V_{OI}/V_{DD}$ vs. $V_{FG}/V_{DD}$) of the reconfigurable logic gate in parallel and antiparallel magnetizations for the spin MOSFET $Q_2$, respectively, where $\beta_1^p/\beta_1^p = 2.7$ and $\beta_2^{AP}/\beta_1^p = 0.4$. When the magnetization of the source and drain of $Q_2$ is parallel, the logic threshold voltage $V_T$ is $V_{TL}$, which is lower than “1/2”. By flipping the magnetization of $Q_2$ from the parallel to antiparallel configuration, the logic threshold voltage $V_T$ is changed to $V_{TH}$, which is higher than “1/2” [see Fig. 2(b)]. This can be explained by assuming that the conventional MOSFET model is applicable to the spin MOSFET as follows: The logic threshold voltage $V_T$ of the reconfigurable logic gate is given by

$$V_T = \frac{V_{DD} - |V_{i1}| + V_{i2}\sqrt{\beta_2^p/\beta_1^p}}{1 + \sqrt{\beta_2^p/\beta_1^p}},$$

where $V_{i1}$ and $V_{i2}$ are the threshold voltages for the drain currents of $Q_1$ and $Q_2$, respectively, and $\xi$ is denoted $P$ for parallel magnetization and AP for antiparallel magnetization. When $|V_{i1}| \approx V_{i2}$, $V_T$ is lower than “1/2” for $\beta_2^p/\beta_1^p > 1$ and is higher than “1/2” for $\beta_2^p/\beta_1^p < 1$. Thus, when $Q_2$ is in the parallel (antiparallel) magnetization state, the logic threshold voltage is $V_{TL}$ ($V_{TH}$), owing to the above-noted relation, $\beta_2^{AP} < \beta_1^p < \beta_2^p$.

The logic operations of the reconfigurable NAND/NOR gate can be obtained using the transfer characteristics shown in Fig. 2(b). When the spin MOSFET $Q_2$ is in the parallel magnetization state, the logic threshold voltage $V_{TL}$ is lower than “1/2” as shown by the red dotted curve in the figure. For the input combinations of $A = B = “0”$, $A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$ and $A = B = “1”$, $V_{FG}$ takes “0”, “1/2” and “1”, respectively, as described above. These $V_{FG}$ values are transformed to $V_{O1} = “1”$, “0” and “0”, respectively, via the transfer characteristics. Thus, the reconfigurable logic gate shows a NOR function when $Q_2$ is in the parallel magnetization state. Note that when $V_{FG} = “1/2”$ ($A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$), $V_{O1}$ is slightly higher than “0”. However, this deviation can be included in a logic margin, i.e., using the logic margin $\Delta V$, the “0” level for $V_{O1}$ is given by “0” $\leq V_{O1} \leq “0” + \Delta V$. This deviation disappears after the inverse amplification from $V_{O1}$ to $V_{O2}$ by the output inverter $G_0$, as shown by the solid red curve in Fig. 2(b).

When the spin MOSFET $Q_2$ is in antiparallel magnetization, the logic threshold voltage $V_{TH}$ is higher than $V_{FG} = “1/2”$, as shown by the dotted blue curve in Fig. 2(b). Owing to this transfer characteristics, the input combinations of $A = B = “0”$, $A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$ are transformed to $V_{O1} = “1”$, “1/2” and “1”, respectively) are transformed to $V_{O1} = “1”$, “1” and “0”. Thus, the reconfigurable logic gate shows a NAND function when $Q_2$ is in the antiparallel magnetization state. Note that when $V_{FG} = “1/2”$ ($A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$), $V_{O1}$ is slightly lower than “1”. Since this deviation can be included in the logic margin for the “1” level (”1” $- \Delta V \leq V_{O1} \leq “1”$), it is also eliminated by the output inverter $G_0$, as shown by the solid blue curve in Fig. 2(b). The logic function for the output $V_{O2}$ is inverted from NAND to AND.

Figure 3 shows another reconfigurable AND/OR gate for the output $V_{OI}$ and a NAND/NOR gate for the output $V_{O2}$, where the capacitively coupled inputs of the $n$MOS input stage are replaced by CMOS inverters $G_A$ and $G_B$ that are directly connected to the common gate of $Q_1$ and $Q_2$. Since the logic threshold voltages of $G_A$ and $G_B$ are set to $V_T = “1/2”$, the voltage input to the common gate is “1”, “1/2” and “0” for the input combinations of $A = B = “0”$, $A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$ and $A = B = “1”$, respectively. Thus, this input stage shows a similar function to that of the $n$MOS input stage, although the logic functions of the output are inverted by $G_A$ and $G_B$. In practice, a $n$MOS input stage requires a large area in order to realize a large input capacitance. On the other hand, the input stage shown in Fig. 3 is effective for reducing the occupied
area for the reconfigurable logic gate, though it has a disadvantage of relatively large power dissipation due to the current from $G_A$ (G_b) to $G_B$ (G_A) through the common gate.

4. Reconfigurable Logic Gate for All Symmetric Boolean Functions

Figure 4(a) shows a reconfigurable logic gate for all symmetric Boolean functions (AND, OR, NOR, NAND, NOR, XOR, XNOR, all-“1”, all-“0”). Whereas forty-eight transistors (including an address decoder, static random access memory (SRAM), and a flip– flop) would be needed with conventional MOSFETs alone, the circuit in Fig. 4(a) is composed of only ten transistors (five CMOS inverters) including four spin MOSFETs. A CMOS input stage and a CMOS inverter G_{12} consisting of p-channel and n-channel spin MOSFETs Q_1 and Q_3 act as a NAND/NOR gate for the output V_{O1}. A CMOS inverter G_0 (G_{34}) and a p-channel (n-channel) spin MOSFET Q_3 (Q_4) are connected between the floating gate and the output V_{O1} terminal, as shown in the figure. A CMOS inverter G_0 at the output stage is used for the inverse amplification of the V_{O1} signal in order to eliminate deviations of V_{O1} from the complete “0” and “1” states. Note that since the p-channel and n-channel spin MOSFETs Q_3 and Q_4 can also create a CMOS configuration (G_{34}), this logic gate is compatible with CMOS technology. Hereafter, the gain coefficient of the spin MOSFET Q_i (i = 1, 2, 3 and 4) is referred to as $\beta_i$, where $\xi$ represents P for parallel magnetization and AP for antiparallel magnetization. The relationships of $\beta^A_P$, $\beta^A_P < \beta^A_P$, $\beta^A_P < \beta^P_P$, $\beta^P_P < \beta^P_P$, $\beta^P_P$ are required, as discussed later. The logic threshold voltage of G_{12} can be controlled by the magnetization configurations of Q_1 and Q_2. When Q_1 (Q_2) is parallel magnetization and Q_2 (Q_1) is antiparallel magnetization, the logic threshold voltage is $V_{TH} > “1/2”$ ($V_{TL} “1/2”$) owing to $\beta^2_P/\beta^P_P < 1$ ($\beta^2_P/\beta^P_P > 1$). This relationship is the same qualitatively as the logic gate shown in Fig. 2, i.e., this relationship can be obtained from eq. (2) by replacing $\beta_i$ with $\beta_i$. The logic threshold voltages $V_{TP}$ and $V_{TN}$ of the CMOS inverters G_0 and G_N are designed to realize the relationships “1/2” $V_{TP} < V_{TH}$ and $V_{TL} < V_{TN} “1/2”$, respectively. Owing to the logic threshold voltage of G_P (G_N), Q_1 (Q_4) turns on only when $A = B = “0”$. The logic threshold voltage of the output inverter G_0 is set to “1/2”, as well as the reconfigurable logic gate shown in Fig. 2. Note that the CMOS input stage can be replaced by the input stage consisting of the inverters G_A and G_B with the common gate, as shown in Fig. 3.

The logic functions of the reconfigurable logic gate shown in Fig. 4(a) can be switched by changing the combination of magnetization configurations of the spin MOSFETs Q_1, Q_2, Q_3 and Q_4. Hereafter, the magnetization configurations of Q_1, Q_2, Q_3 and Q_4 are specified using the expression of $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, \xi_3, \xi_4\}$, where $\xi_i$ (i = 1, 2, 3 and 4) represents the magnetization configuration of Q_i and $\xi_i = P (AP)$ is for the parallel (antiparallel) magnetization. Figures 4(b)–(e) show transfer characteristics for $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, \xi_3, \xi_4\}$, $\{\xi_1, \xi_2, P, AP\}$, $\{\xi_1, \xi_2, AP, P\}$, $\{\xi_1, \xi_2, P, AP\}$ and $\{\xi_1, \xi_2, P, AP\}$, respectively, where $\beta^P_P/\beta^A_P = 7.0$, $\beta^P_P/\beta^A_P = 1.2$, $\beta^P_P/\beta^A_P = 8.0$, $\beta^A_P/\beta^A_P = 0.8$, $\beta^P_P/\beta^A_P = 22.5$, $\beta^A_P/\beta^A_P = 0.5$ and $\beta^P_P/\beta^A_P = 14.0$. The dotted and solid curves in the figure are the transfer characteristics for the output V_{O1} and V_{O2}, respectively. Although the output V_{O1} shows deviations from the complete “0” and “1” states (i.e., the “0” level for V_{O1} means “0” $V_{O1} ≤ “0” + AV$, and the “1” level for V_{O1} “1” $V_{O1} “1”$), these deviations can be eliminated using the output inverter G_0. Since the resulting logic functions for the output V_{O2} are easily obtained from the inverted logic functions for the output V_{O1}, the operation of the reconfigurable logic for the output V_{O1} is described below. Note that all symmetric Boolean functions (AND, OR, XNOR, NOR, XOR, all-“1”, all-“0”) are also realized for the output V_{O2}, as well as V_{O1}.

In the following, we will describe in detail how the function of this circuit can be selected from among all symmetric Boolean functions (AND, OR, NAND, NOR, XOR, XNOR, all 1, all 0) by controlling the magnetization (transconductance) of the four spin MOSFETs (Q_1, Q_2, Q_3 and Q_4). Table I shows the truth tables of this circuit.

When $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}$, the reconfigurable logic gate can switch NAND/NOR functions, the logic function of which can be selected by the magnetization configuration combination $\{\xi_1, \xi_2\} = \{P$, AP\} or $\{AP, P\}$. Although Q_2 and Q_3 turn on for $V_{FG} > V_{TP}$ and $V_{FG} < V_{FN}$, respectively, the influences of Q_2 and Q_3 can be neglected because of their small gain coefficients (drain current) compared with those of Q_1 and Q_2, owing to the above noted relationship of $\beta^AP_P < \beta^AP_P$, $\beta^AP_P < \beta^P_P$, $\beta^P_P$. This, thus, reconfigurable logic gate exhibits qualitatively the same transfer characteristics as the NAND/NOR gate shown in Fig. 2. The blue and red dotted curves in Fig. 4(b) show the transfer characteristics for $\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, AP, AP\}$ and $\{AP, P, AP, AP\}$, respectively. Since these magnetization configurations realize $\beta^AP_P > 1$ and $\beta^P_P > \beta^P_P$, the logic threshold voltages of these transfer characteristics become $V_{TH} > “1/2”$ for $\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, AP, AP\}$ and $V_{TL} “1/2”$ for $\{Q_1, Q_2, Q_3, Q_4\} = \{AP, P, AP, AP\}$. The transfer characteristics with $V_{TH}$ and $V_{TL}$ realize NAND and NOR functions (Fig. 4(b)), respectively, as well as those in Fig. 2(b).

When $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, P, AP\}$, the reconfigurable logic gate can switch all-“1”/XNOR functions. The blue and red dotted curves in Fig. 4(c) show the transfer characteristics for $\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, P, AP\}$ and $\{AP, P, P, AP\}$, respectively. Since the gain coefficients $\beta^P_P$ and $\beta^AP_P$ satisfy the relationship $\beta^AP_P < \beta^AP_P$, $\beta^AP_P < \beta^P_P$, $\beta^P_P < \beta^P_P$, Q_3 turns on and affects the output V_{O1} when $V_{FG} > V_{TP}$, but Q_3 does not affect the output V_{O1} even when $V_{FG} < V_{FN}$. Thus, when $V_{FG} > V_{TP}$, the transfer characteristics are almost the same as that for $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}$, and when $V_{FG} > V_{TP}$, the output V_{O1} is forced to increase to the “1” level by Q_3 due to the large gain coefficient $\beta^P_P$. Owing to these transfer characteristics, the input combinations of $A = B = “0”$, $A = “0”$, $B = “1”$, or $A = “1”$, $B = “0”$ (corresponding to $V_{FG} “0”$, “1/2” and “1”), respectively) are transformed to $V_{O1} = “1”$, “1” and “1” (all-“1” function) for $\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, P, AP\}$ and to $V_{O1} = “1”$, “0” and “1” (XNOR function) for $\{Q_1, Q_2, Q_3, Q_4\} = \{AP, P, P, AP\}$, respectively.

When $\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, P\}$, the reconfig-
urable logic gate can switch XOR/all-"0" functions. The blue and red dotted curves in Fig. 4(d) show the transfer characteristics for \{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, AP, P\} and \{AP, P, AP, P\}, respectively. Owing to the relationship \(\beta_3^{AP} < \beta_1^{AP}, \beta_2^{AP} < \beta_1^{P}, \beta_2^{P} < \beta_4^{P}\), Q_4 turns on and affects the output \(V_{O1}\) when \(V_{FG} < V_{TN}\), but Q_3 has no influence on the output \(V_{O1}\) even when \(V_{FG} > V_{TP}\). Thus, when \(V_{FG} > V_{TN}\), the transfer characteristics are almost the same as those for \{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}, and when \(V_{FG} < V_{TN}\), the output \(V_{O1}\) is forced to decrease to the

Fig. 4. (a) Circuit configuration of a reconfigurable logic gate for two-input all symmetric Boolean functions. Transfer characteristics \((V_{O1} - V_{FG})\) and \((V_{O2} - V_{FG})\) characteristics normalized by \(V_{DD}\) for (b) \(\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}\), (c) \(\{\xi_1, \xi_2, P, AP\}\), (d) \(\{\xi_1, \xi_2, AP, P\}\) and (e) \(\{\xi_1, \xi_2, P, P\}\) are shown. Dotted and solid curves are the transfer characteristics for outputs \(V_{O1}\) and \(V_{O2}\), respectively, and blue and red curves show the transfer characteristics for \{\xi_1, \xi_2\} = \{P, AP\} and \{AP, P\}, respectively.
Table I. Truth table of the reconfigurable circuit of Fig. 4(a) for each condition. Tables for (a) \{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}, (b) \{\xi_1, \xi_2, P, AP\}, (c) \{\xi_1, \xi_2, AP, P\} and (d) \{\xi_1, \xi_2, P, P\} correspond to Figs. 4(b), 4(c), 4(d), and 4(e), respectively.

\[
\begin{array}{cccc}
A & B & V_{OG} & V_{OI} \\
0 & 0 & 0 & \sim 1 \sim 0 \sim 1 \sim 0 \\
0 & 1 & 1/2 & \sim 1 \sim 0 \sim 1 \sim 0 \\
1 & 1 & \sim 1 \sim 0 \sim 1 \sim 1 \sim 0 \sim 1 \\
0 & 1 & 1/2 & \sim 1 \sim 0 \sim 1 \sim 0 \\
0 & 0 & 0 & \sim 0 \sim 1 \sim 0 \sim 1 \\
0 & 1 & 1/2 & \sim 1 \sim 0 \sim 1 \sim 0 \\
1 & 1 & \sim 1 \sim 0 \sim 1 \sim 1 \sim 0 \sim 1 \\
\end{array}
\]

For "0" level by \(Q_3\) due to the large gain coefficient \(\beta_0, P\). The input combinations of \(A = B = "0", [A = "0", B = "1", or \(A = "1", B = "0", \) and \(A = B = "1", \) (corresponding to \(V_{OG} = "0", "1/2" \) and "1", respectively) are transformed to \(V_{OI} = "0", "1" \) and "0" (XOR function) for \(\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, AP, P\}\) and to \(V_{OI} = "0", "0" \) and "0" (all-"0" function) for \(\{Q_1, Q_2, Q_3, Q_4\} = \{AP, P, AP, P\}\), respectively.

When \(\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, P, P\}\), this logic gate can switch OR/AND functions. The blue and red dotted curves in Fig. 4(e) show the transfer characteristics for \(\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, AP, P\}\) and \(\{AP, P, P, P\}\), respectively. \(Q_1\) and \(Q_3\) turn on when \(V_{OG} < V_{TN}\) and \(V_{OG} > V_{TP}\), respectively, and there exists the relationship \(\beta_{AP} = \beta_{P} < \beta_{AP} < \beta_{AP} < \beta_{P}\). Therefore the transfer characteristics are almost the same as those for \(\{Q_1, Q_2, Q_3, Q_4\} = \{\xi_1, \xi_2, AP, AP\}\) only when \(V_{TN} < V_{FG} < V_{TP}\). When \(V_{FG} < V_{TN}\) and \(V_{OG} > V_{TP}\), the output \(V_{OI}\) is shifted to the "0" and "1" levels by \(Q_1\) and \(Q_3\), respectively. The input combinations of \(A = B = "0", [A = "0", B = "1", or \(A = "1", B = "0", \) and \(A = B = "1", \) (corresponding to \(V_{FG} = "0", "1/2" \) and "1", respectively) are transformed to \(V_{OI} = "0", "1" \) and "1" (OR function) for \(\{Q_1, Q_2, Q_3, Q_4\} = \{P, AP, P, P\}\) and to \(V_{OI} = "0", "0" \) and "1" (AND function) for \(\{Q_1, Q_2, Q_3, Q_4\} = \{AP, P, P, P\}\), respectively.

A possible application of the proposed reconfigurable logic gates is in the recently emerging field programmable gate array (FPGA). The most advanced type of FPGA is realized by using look-up tables (LUTs) as its logic blocks. Since static random access memory (SRAM) is used for the LUT, logic functions defined in the LUT are reconfigurable but volatile. Thus, nonvolatile memory is required to define the logic functions, which results in the increase of the chip size of FPGA. On the other hand, our reconfigurable logic gates can store the information of logic functions in the form of the magnetization configuration of the spin MOSFETs.

Therefore, the logic functions of our reconfigurable logic gates are nonvolatile. A new FPGA architecture without SRAM and without nonvolatile memory for logic blocks can be established by using spin MOSFETs.

This new class of reconfigurable logic gates could be used for reconfigurable computing, which is an emerging new computing paradigm satisfying both flexibility and performance. Since our device (spin MOSFET) and reconfigurable logic gates are predicted to have both high performance and flexibility as well as nonvolatility, we believe that they will find a variety of applications.

5. Conclusion

Novel spintronic reconfigurable logic gates employing spin MOSFETs were proposed. All symmetric Boolean functions can be realized using only five CMOS inverters including four spin MOSFETs, and the logic functions can be switched by changing the combination of the magnetization configurations of the spin MOSFETs. These reconfigurable and nonvolatile logic gates will be fully compatible with the current CMOS technology, and will provide new "spintronic" Si integrated circuit architectures.

Acknowledgements

The authors would like to thank Professor T. Shibata and Dr. Y. Mita at the University of Tokyo for helpful discussions. This work was supported by the PRESTO program of Japan Science and Technology Agency, a Giant-in-Aid for Science Research on the Priority Area "Semiconductor Nanospintronics" (14076207), the IT program of RR2002 from the Ministry of Education, Culture, Sports, Science and Technology, Toray Science Foundation, and VLSI Design and Education Center (VDEC) at the University of Tokyo in collaboration with Synopsys, Inc.

1) S. Sugahara and M. Tanaka: Appl. Phys. Lett. 84 (2004) 2307.
2) R. A. de Groot, F. M. Mueller, P. G. van Engen and K. H. J. Buschow: Phys. Rev. Lett. 50 (1983) 2024.
3) A. Yanase and K. Shiratori: J. Phys. Soc. Jpn. 53 (1984) 312.
4) K. Schwarz: J. Phys. F16 (1986) L211.
5) M. Shirai: Physica E10 (2001) 143.
6) M. Shirai: J. Appl. Phys. 93 (2003) 6844.
7) K. Sato and H. Katayama-Yoshida: Semicond. Sci. Technol. 17 (2002) 367.
8) The \(g_m, P\) and \(g_m, AP\) values can be designed by tuning the spin injection efficiency of the spin-polarized electrons from the HMF source. This can be realized by adjusting the thickness (or barrier height of the energy barrier induced by the insulating spin band) of the HMF source. Also see S. Sugahara and M. Tanaka: Ext. Abstr. of the 9th Symp. on the Physics and Applications of Spin-related Phenomena in Semiconductors, Tokyo, June 2003, p. 221.
9) T. Shibata and T. Ohmi: IEEE Trans. Electron Devices 39 (1992) 1444.
10) T. Shibata and T. Ohmi: IEEE Trans. Electron Devices 40 (1993) 750.
11) C. L. Lee and C. W. Jen: IEE Proc.-G 139 (1992) 63.
12) S. Trimberger: Proc. IEEE 81 (1993) 1030.
13) S. Hauck: Proc. IEEE 86 (1998) 625.
14) K. Bondalapati and V. K. Prasanna: Proc. IEEE 20 (2002) 1201.