A Novel Architecture for 10-bit 40MSPS Low Power Pipelined ADC Using a Simultaneous Capacitor and Op-amp Sharing Technique

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Abstract
This work presents a low-power 10-bit 40 MSPS Pipelined ADC with 1.8V supply voltage in a 180nm silicon-based CMOS process. Simultaneous capacitor sharing and op-amp sharing technique is used between two successive stages of a Sample-and-Hold Amplifier (SHA) to reduce the power consumption. The memory effect in the proposed ADC is eliminated by a low input capacitance variable g_m op-amp. The differential and integral nonlinearity of the converter is within LSB. Simulation results show that the required Signal-Furious-Dynamic range (SFDR) of 70dB, Signal-to-Noise-plus Distortion Ratio (SNDR) of 56.1dB and 9.02 Effective Number of Bits (ENOB) has been achieved with a 2 MHz, 1-V_{p-p, diff} input signal while consuming only 7.3mW power from 1.8V supply.

Keywords Op-amp · Capacitor sharing · Power consumption · Dynamic comparator · Analog to Digital converter (ADC)

1 Introduction
With the increasing demand for the Application Specific Integrated Circuits (ASICs), there is a wide development of mixed-signal design, compatible with System-on-Chip (SoC). Data converters have become an important block in SoC design for data communication and image processing applications [1]. Among the different ADC designs, pipelined ADCs are suitable for high speed, medium resolution, and low power applications [2–4]. Since the accuracy decreases in the later stages of pipeline ADC, proper scaling of capacitors are required in pipelined ADC [5–7].

Sharing an op-amp between two consecutive stages can further reduce power consumption [8–10]. Furthermore, switched-op-amp techniques [11, 12] were proposed to reduce the power consumption of pipelined ADC. The maximum power is consumed in the first stage of the pipelined ADC [12].

To reduce the power consumption of the ADC capacitor sharing technique was proposed [13–16]. To further reduce the power consumption, the front-end sample and hold circuit (S/H) are eliminated [17, 18]. SHA introduces an additional noise signal which is integrated into the analog signal and results in large power dissipation and occupies more die area. Also, the S/H circuit is removed by integrating the SHA in the first stage of pipeline ADC to reduce the power [19]. Hence certain applications need to simplify the pipelined ADC by eliminating the supplementary blocks such as the SHA circuit [20]. The aperture error is reduced by matching the delays that occur between the sampling networks of the sub-blocks including the first MDAC and comparators [21]. In this paper, a novel SHA-less pipelined ADC using a combination of simultaneous capacitor and amplifier sharing with a sampling frequency of 40 MSPS is presented. To achieve low-power and high performance, the P-gain, and N-gain boosted variable g_m op-amp and dynamic comparators have been designed.
2 The Architecture of SHA-less Pipelined ADC

The proposed SHA-less Pipelined ADC architecture is shown in Fig. 1. It mainly contains an SHA-less front-end followed by the second stage in which two op-amps are shared in neighboring stages followed by 3-bit Flash ADC. To limit the overall conversion rate the bandwidth of the Switched Capacitor (SC) circuit is to be maximized. The closed-loop gain of the amplifier is 2 so that a large feedback factor and a low load capacitance are achieved. Since the capacitance load is very less and the feedback factor is large the bandwidth of the amplifier which is used in the intermediate stages can be increased. The main advantage in pipelining the structure is cascading every stage for better performance. In pipelined
ADC all the stages are integrated and when one stage is sampling the analog input signal the next stage amplifies the signal. This is the main advantage of pipelining the structure. The outputs from each stage are given to Digital Error Correction (DEC) Logic and it provides the output in a concurrent fashion. Pipelined ADC provides optimum results in power dissipation, speed and resolution. Figure 2 shows the first and second stages of the ADC.

2.1 Operational Amplifier

An op-amp is the main important sub-circuit of analog systems[22–25]. The common-mode noise and even harmonics are reduced in the fully differential amplifier which employs a two-stage topology when compared with the single-ended output op-amp. Also, the linearity is increased in the fully differential amplifier. Figure 3 shows the designed
two-stage fully differential OTA which uses the gain boosted auxiliary amplifier. Here the fully differential structures are used in P gain boost and N gain boost amplifiers. With 1.8 V supply voltage, the gain boosted amplifier is simulated initially to verify the desired specifications which were described by [26–28].

2.1.1 Design of the Op-amp

The op-amp is the most essential block in ADC [29, 30]. The output impedance \( R_{out} \) is increased by the added gain stage \( A_{OTA} \) as given in the following equation:

\[
R_{out} = \left( g_{m2} r_{02} (A_{add} + 1) + 1 \right) r_{01} + r_{02}
\]  \hspace{1cm} (1)

Further more, the DC gain of the op-amp is improved in several orders of magnitude:

\[
A_{0,tot} = g_{m1} r_{01} (g_{m2} r_{02})(A_{new} + 1) + 1
\]  \hspace{1cm} (2)

\[
= A_{OTA} g_{m1} g_{m2} r_{01} r_{02}
\]  \hspace{1cm} (3)

To improve the voltage gain of the folded cascode amplifier, the output impedance of the circuit needs to be increased as shown in Fig. 4. The design procedure starts with the design of a fully differential op-amp and the second step is to

Fig. 5  P gain boost amplifier

Fig. 6  N gain boost amplifier
introduce the gain boosting amplifier to obtain the desired gain without affecting the bandwidth of the op-amp. To start with, the sizing of the main differential input pair of the transistors MN₀, MN₁ is selected using the desired phase margin and the gain bandwidth specifications. This op-amp design includes the design of differential inputs, differential outputs, folded cascode bias circuits with common-mode feedback (CMFB), and gain-boosting amplifiers [31–33].

The feedback factor $\beta$ is given by:

$$\beta = \frac{C_f}{C_1 + C_p + C_f}$$  \hspace{1cm} (4)

The unity gain frequency is given by:

$$\omega_{\text{unity}} = \frac{g_m}{C_o (C_i + C_p + C_f + (C_i + C_p) C_f)}$$  \hspace{1cm} (5)

The settling time $\tau$ can be found by:

$$\tau = \frac{C_p + C_i + C_o + (C_i + C_p) C_o}{g_m} \left( \frac{C_f}{C_1 + C_p + C_f} \right)$$  \hspace{1cm} (6)

In Fig. 5 the overdrive voltage of M10 is assigned high than that of input transistors M8 and M9 to boost the gain. The gain of this op-amp is mostly based upon the transistors M₃, M₅, and M₈. The transistors M₀ and M₁ should be matched and kept wide enough to act as a resistor i.e. the overdrive voltage assigned is more compared to all.

The bias circuit is used in this op-amp is the current biasing circuit which is a current source with one Silicon-based NMOS for n-bias and a current source with one Silicon-based PMOS for p-bias. The current in the current source is scaled to give the bias voltage needed to make the circuit stable. Figure 6 shows the N gain boost amplifier.
Fig. 8 Proposed sampling network for the first stage

Fig. 9 Timing Diagram for the sampling network

Fig. 10 Obtained FFT spectrum of pipelined ADC
2.1.2 Analysis of the Op-amp

For the residue signal generated by the MDAC, the op-amp loop-gain has to be at least $2^9$ (54 dB). In the design of the op-amp, the main stage is the folded cascode op-amp which produces high gain. The $V_{cm}$ node is used to control the common-mode bias voltage of the op-amp. Table 1 shows the performance summary of P Gain and N Gain Boost Amplifiers.

Simulation results show that the total DC gain of the op-amp is 86dB. The phase Margin value of the variable $g_m$ op-amp is greater than 80°. Table 2 shows the performance summary of variable $g_m$ op-amp.

Table 3 Performance summary of 10-bit SHA less pipelined ADC

| Technology  | 180nm |
|-------------|-------|
| Resolution  | 10bit |
| Input Range | 1Vpp |
| Frequency Range (f_s) | 2MHz |
| Sampling frequency (f_s) | 40MHz |
| DNL         | +0.57/-1 LSB |
| INL         | +0.74/-0.74 LSB |
| SFDR        | 70dB |
| SNDR        | 56.12dB |
| ENOB        | 9.0289 bits |
| FOM         | 0.35pJ/step |
| Total Power | 7.3mW |
| Conversion time | 2.5ns |
| Area        | 0.63mm^2 |

3 Simultaneous Capacitor Sharing and Op-amp Sharing MDAC

The capacitor $C_{1f}$ is composed of two parts: $C_{2f}$ and $C_{2s}$. During phase $\Phi_1$, the analog input signal is sampled on the two capacitors $C_{1f}$ and $C_{1s}$. The residue signal is generated from each stage during phase $\Phi_2$ and the residue signal is not provided to the sampling capacitors in the second stage of the pipelined ADC. The residue signal is detained on $C_{1f}$ which is the feedback capacitor. Using the stored value on the capacitor $C_{1f}$, a residue signal is produced. This stored value is provided to the sampling capacitors of the third stage $C_{3f}$ and $C_{3s}$ during the next phase $\Phi_1$. When the second stage is generating its residue signal, the next input signal that needs to be sampled is used[34–36]. The feedback capacitors named $C_{1fe}$ and $C_{1fo}$ are used. The matching network is used in the initial stage of ADC. In the proposed pipelined ADC the simultaneous capacitor sharing and op-amp sharing technique is used. Figure 7 shows the simultaneous capacitor and op-amp sharing technique.

3.1 Sampling Network for Stage 1

The use of the S/H circuit is avoided with the MDAC and the sub-ADC performing the sampling procedure [37]. In this work, the aperture error is minimized by matching the sampling network through the cautious design of the aspect ratio (W/L) of the transistor. The gate-source voltage ($V_{gs}$) is the same for the sampling capacitance $C_s$ and $C_{com1}$-$C_{com4}$ in the
sampling network. This is because the above-mentioned sampling capacitance is connected to the same common-mode voltage. Figure 8 shows the proposed sampling network for the initial stage. Figure 9 shows the timing diagram for the sampling network.

4 Results and Discussion

The SHA-less Pipelined ADC is simulated in a 180nm Silicon-based CMOS process. Various sub circuits like dynamic comparator, op-amp, MDAC, Sub ADC, and sub-DAC were integrated for pipelined ADC [38–40]. Figure 10 shows the 1024 points FFT spectrum with an input frequency of 2 MHz.

Figure 11 shows the layout of 10-bit SHA less pipelined ADC. The delay and the power consumption obtained after the post-layout simulation is 15.1ns and 15mW.

Table 3 shows the Performance summary of 10-bit SHA less pipelined ADC. The 10-bit SHA less pipelined ADC was designed in a 180nm Silicon-based CMOS process and achieves 56.12 dB SNDR, 56.20 dB SNR, 70 dB SFDR, from a 1.8 V supply voltage.

Table 4 shows the comparison of the 10-bit SHA-less pipelined ADC with some reported pipelined ADCs. Comparing the present work with the reported work at [27] 39.1 % of power reduction has been achieved. When compared to the other pipelined ADCs reported in previously reported works this 10-bit SHA less Pipelined ADC has less power consumption.

5 Conclusions

A 40MSPS pipelined ADC which is suitable for low power has been described. By removing the front-end SHA, considerable power saving is obtained. The variable g_m operational transconductance amplifier used in the design has been designed with a gain of 45dB. Clocked dynamic comparator is also designed and the same is used to build sub-ADC’s which generate the LSB and MSB of every single stage. Simulation results of the pipelined ADC in a 180nm Silicon-based CMOS process show an SFDR of 70 dB, SNDR of 56.12 dB, ENOB of 9.02 bits, and FOM of 0.35pJ/step while consuming only 7.3mW for a 2 MHz input signal. From the results, it was shown that the designed ADC maintains good dynamic performance and low power consumption suitable for SOC Digital TV Application.

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Authors’ Contributions All authors whose names appear on the submission.
1) made substantial contributions to the conception or design of the work.
2) drafted the work or revised it critically for important intellectual content.
3) approved the version to be published.
4) agree to be accountable for all aspects of the work in ensuring that questions related to the accuracy or integrity of any part of the work are appropriately investigated and resolved.

Data Availability Not applicable.

Code Availability Not applicable.

Declarations

Conflicts of Interest/Competing Interests The authors declare that they have no competing interests.

Ethics Approval Not applicable.

Consent to Participate Not applicable.

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Table 4 Comparison of the SHA-less pipelined ADC with some reported pipelined ADCs

| Reference | Technology (nm) | Supply Voltage (V) | Sample Frequency (MSPS) | Resolution (bits) | Power (mW) | SNDR (dB) | SFDR (dB) | ENOB | DNL/INL (LSB) | Area (mm²) |
|-----------|----------------|-------------------|--------------------------|------------------|------------|-----------|-----------|------|----------------|------------|
| [10]      | 180            | 1.8               | 40                       | 10               | 23.4       | 59.53     | 71.67     | 9.40 | 0.28/0.62     | 0.63       |
| [12]      | 180            | 1.8               | 30                       | 10               | 21.6       | 57.41     | 65.93     | 9.10 | 0.57/0.80     | 0.70       |
| [30]      | 180            | 1.8/3             | 80                       | 10               | 69.0       | -         | 72.78     | 9.29 | + 0.20/-0.25  | 1.85       |
| [31]      | 180            | 1.8               | 50                       | 10               | 12.0       | 56.20     | 72.70     | 9.03 | 0.39/0.81     | 0.86       |
| [32]      | 180            | 1.8               | 30                       | 10               | 21.6       | 58.50     | 66.10     | -    | 0.30/0.46     | 1.85       |
| [34]      | 180            | 1.8               | 200                      | 10               | 56.0       | 61.07     | -         | 9.85 | -              | 1.44       |
| Present work | 180            | 1.8               | 40                       | 10               | 7.30       | 56.10     | 70.00     | 9.02 | + 0.57/-1 + 0.7/-0.74 | 0.35       |
