Choice of Si doping type for optimizing the performances of a SiOx-based tunneling electron source fabricated on SiOx/Si substrate

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Abstract

A new type on-chip electron source based on electroformed SiOx is recently reported to show dense and efficient electron emission under low working voltage. Here we study the effect of the Si doping type of SiOx/Si substrate on the performances of the SiOx-based electron source fabricated on it. The electron source is composed of an array of parallelly integrated micro-emitters. Each micro-emitter is composed of a square nanogap with a width about 100 nm which is spaced by two concentric graphene films on the SiOx substrate. The inner graphene film contact with bottom Si electrode through a via hole opening to the bottom Si layer and the outer graphene film contact with the common metal electrode. Effective emission current and efficiency of the electron source are found to be significantly influenced by both the polarity of the driven voltage applied between the metal electrode and bottom Si layer and the polarity of the Schottky barrier at graphene-Si contact. The performances of electron sources can be optimized by choosing n-type doping of SiOx/Si substrate to make the positive influence of the two aspects achieved at the same time. An emission current up to 100 μA and emission density of 250 mA cm⁻² are achieved for an optimized device with 64 micro-emitters at bias voltage of 32.8 V.

1. Introduction

High-performance electron sources fabricated on chips by microfabrication technologies and driven by electricity have been pursued for more than 60 years by researchers [1, 2], because they possess several advantages compared with traditional thermionic electron sources, including compactness, being integratable, fast temporal response, and high efficiency and reliability in batch fabrication. Furthermore, on-chip electron sources can advance the development of miniature electronic devices and instruments relying on free electron beams, such as miniature X-ray tubes [3, 4], miniature electron microscopes [5, 6]. Making use of on-chip electron sources, it is even possible to miniaturize vacuum electronic devices on chips and several such on-chip vacuum electronic devices have been reported, such as on-chip vacuum triodes [7], on-chip vacuum sensors [8, 9], on-chip traveling wave tubes [10], on-chip mass spectrometers [11, 12], on-chip vacuum pumps [9, 13] and so on. Additionally, on-chip vacuum electronic devices can be monolithically integrated with solid state devices to enable more device functions.

Since on-chip electron sources have promising applications, many efforts have been devoted to them and several types of on-chip electron sources have been reported. Previous on-chip electron sources can be roughly divided into three categories in terms of emission mechanism: external field emission sources (e.g. Spindt emitters [2], silicon tip emitters [14], nanotube emitters [15] and surface conduction emitters [16]), internal field emission sources which are based on Schottky barriers [17], p-n junctions [18], negative-electron-affinity structure [19], tunneling junctions [1], and thermionic emission sources based on graphene [20, 21] and carbon nanotubes [22, 23]. However, these electron sources have rarely been put into practical applications because they...
all exhibit performances bottlenecks. For example, external field emission sources represented by the Spindt emitters require high operating voltage [24], ultra-high vacuum [25], and show poor uniformity [26], whereas the internal field emission sources represented by metal-insulator-metal tunneling sources encountered problems of low emission density and low emission efficiency [27, 28]. As for the on-chip thermionic emission sources, they are still facing the difficulties of low emission current [23] and low efficiency [20]. Recently, we reported a new type of on-chip electron sources based on electroformed silicon oxide in square nanogap with a width about 100 nm spaced by two concentric graphene films [29]. The new type on-chip electron sources own several encouraging properties, including high emission density, large emission current, high emission efficiency and low working voltage, and provide a new choice for developing high-performance on-chip electron sources. The SiO$_x$-based electron source is composed of an array of parallelly integrated micro-emitters fabricated on a SiO$_x$/Si substrate. Each micro-emitter is composed of a square nanogap with a width about 100 nm which is spaced by two concentric graphene films. The inner graphene film contacts with bottom Si electrode through a via hole opening to the Si layer and the outer graphene film contacts with the common metal electrode. In this paper, we found that effective emission current and efficiency of the electron source can be significantly influenced by both the polarity of the driven voltage applied between the metal electrode and Si layer and the polarity of the Schottky barrier at graphene-Si contact. To optimize the performances of electron sources, we conclude that n-doped SiO$_x$/Si substrate should be chosen for device fabrication as it can make the positive influences of the two aspects achieved at the same time. An electron source with 64 micro-emitters array fabricated on n-doped SiO$_x$/Si substrate shows emission current up to 100 μA and corresponding emission density of 250 mA cm$^{-2}$ at bias voltage of 32.8 V.

2. Device structure and fabrication

The structure of an electron source and the setup of its emission current measurement are schematically shown in figure 1(a). The electron source consists of an array of micro-emitters fabricated on a SiO$_x$/Si substrate. As shown in figure 1(b), a micro-emitter is composed of a square nanogap with a width about 100 nm which is spaced by two concentric graphene films on the SiO$_x$ substrate. The inner graphene film contacts with bottom Si electrode through a via hole opening to the Si layer and the outer graphene film contacts with the common metal electrode. All micro-emitters in an array are therefore integrated in a parallel way between the top common metal electrode and the bottom Si layer which acts as a common bottom electrode. To active and drive the electron source, a bias voltage is applied between the top metal electrode and the bottom Si electrode. Emission current is measured using a collecting electrode locating ∼250 μm above the electron source and applied with a
210 V collecting voltage. Based on two considerations, concentric graphene films structure between top metal electrode and bottom Si electrode is employed in our electron source. The first consideration is to facilitate parallel integration of a large number of micro-emitters between the common top metal electrode and bottom Si electrode, and to realize high emission current. More importantly, it facilitates Joule heat dissipation generated in the device. The chip with electron sources can be placed on a massive heat sink, so the Joule heat generated mainly at the nanogaps can be taken away through the conducting graphene and silicon from the device to the heat sink.

Electron sources are fabricated on both n-type and p-type thermal-oxidized SiOx/Si substrates with a SiOx layer thickness of 300 nm. All fabrication processes are completed by semiconductor fabrication technology, including via holes array fabrication, graphene transfer, nanogaps fabrication, and metal electrode deposition. First, an array of via holes were obtained by electron beam lithography followed by wet etching. A Polymethyl metacrylate (PMMA) 950 K layer was spin-coated at 4000 rpm and then baked on a hot plate at 170 °C for 5 min. The position of via holes array were defined by electron beam lithography (Raith 150 II system) and then the silicon oxide in via holes was etched by diluted HF with buffered solution (buffered oxide etch, BOE). During the etching, the chip was shaken slightly for solvent exchange to obtain uniform via holes array. The second is graphene transfer. High-quality and cheap graphene can be grown on copper foil by chemical vapor deposition, which is used in our experiments [30]. Using a PMMA mediated method [31], graphene was transferred to the substrate with via holes array. As graphene has great flexibility, it will cover the via holes and contact with the bottom silicon without wrinkles and broken holes. Third, it is to fabricate the ~100 nm nanogap. Using Raith 150 II system and PMMA 950 K as electron beam resist, an array of square nanogaps with a width of approximately 30 nm was defined. The graphene in the nanogaps was etched immediately by O2 reactive ion etching. Due to the lateral expansion of the etching, ~100 nm nanogaps between graphene films were finally obtained. Finally, the metal electrodes were fabricated. After electron beam exposure patterning, metal film deposition and lift–off processes, we fabricated 90 nm Au/5 nm Ti metal electrodes. Using the above fabrication process, we can fabricate parallel micro-emitter arrays with various micro-emitter numbers.

Figure 1(c) shows the scanning electron microscopy (SEM) image of an electron source, where an 8 × 8 array of micro-emitters are fabricated in an area of 200 × 200 μm². Figure 1(d) shows the SEM image of a micro-emitter. The width of the square nanogap which is spaced by two concentric graphene films is about 100 nm and the edge is 11 μm. The inner graphene film is in electrical contact with bottom conducting Si layer of the substrate through a via hole with a diameter of 8 μm. The outer graphene film is in electrical contact with a common metal electrode. Emission current is measured in the Janis probe station chamber with a vacuum about 10⁻³ Pa. With Keithley 4200 semiconductor characterization system, bias voltage and current can be applied to the electrodes of electron source, and the corresponding emission current can also be detected.

### 3. Results and discussion

As silicon oxide in the graphene nanogaps is insulating, the as-fabricated electron source has to be activated to achieve electron emission. Usually, a sweeping bias voltage (Vbias) from 0 to ~20 V is repeatedly applied to the electron source through its top common metal electrode and bottom Si one to activate it. When the emission current no longer increases with more voltage sweeps, it means that the electron source is fully activated. Figures 2(a) and 2(b) show the simultaneously measured emission current (Ie) and conduction current (Ic) between top metal and bottom Si electrodes when an electron source with an 8 × 8 array of micro-emitters fabricated on a p-type substrate was activated. Conduction current here is defined as the electron current leaving the graphene film with a lower electric potential. When a sweeping voltage was firstly applied to an as-fabricated device, there was no measurable conduction current and emission current at the beginning until the conduction current increased sharply to a few μA at about 4.5 V (figure 2(a)), which means that the insulating silicon oxide in graphene nanogaps was transformed to be conductive at the moment. As bias voltage continued to increase, conduction current increased with bias voltage until around 8 V, where conduction current started to decrease and became fluctuating and emission current became measurable. Emission current then increased with bias voltage to ~40 nA at 15 V. Further voltage sweeps exhibited similar characteristics of both conduction current and emission current with those of the first sweep in figure 2(a), but resulted in larger and larger conduction current and emission current (figure 2(b)). After being activated by 12 voltage sweeps, emission current of the electron source reach 12 μA at 24 V.

According to our previous research, in electroformed silicon oxide, there are horizontal tunneling diodes where electrons are emitted [29, 32, 33]. When a sufficiently high voltage is applied to the nanogaps spaced by the graphene films, silicon oxide in the nanogaps is softly broken–down or electroformed. Oxygen vacancies in silicon oxide migrate under the electric field to form conducting filaments during electroforming process [34], so insulating silicon oxide transforms to be conductive. When electroformed silicon oxide in the nanogaps is set
to a high-resistance state, conducting filaments will rupture under the effects of electric field and Joule heat [35, 36]. Therefore, a horizontal tunneling diode with a conducting filament-insulating gap-conducting filament structure is formed in the shallow substrate surface of the nanogaps (figure 2(c)). As shown by energy diagram in figure 2(d), when a bias voltage larger than the work function of conducting filaments is applied to a horizontal tunneling diode, electrons can be accelerated to above vacuum level after transporting across the tunneling diode and can be emitted into vacuum. Detailed emission mechanism can be referred to our previous papers [32, 33].

When an electron source is driven by applying a bias voltage between the top metal electrode and the bottom Si one, the top electrode can be positively biased or negatively biased relative to the bottom one. For ease of description, we define forward bias and reverse bias for an electron source when the top electrode is positively and negatively biased. Both conduction current and emission current of an electron source were found to depend on the polarity of the bias voltage. As shown in figure 3(a), when an electron source fabricated on a p-type substrate is forward biased, its conduction current and emission current are, respectively, lower and larger than those in the case of reverse bias. The ratio of emission current to conduction current is defined as emission efficiency, which is one of important parameters depicting the performances of internal field emission sources. Emission efficiency of an electron source in forward bias is therefore much higher than that in reverse bias. It is worth noting that the emission current mentioned here actually refers to effective emission current, namely the part of the electrons current collected by the collecting electrode. Some of emitted electrons are intercepted by metal electrodes and graphene films, and cannot be collected by the collecting electrode. The effective emission current is determined by two factors: the amount of emitted electrons and the collection ratio of the electrons by the collecting electrode.

Why emission current is higher when the electron source is forward biased than that when it is reversely biased? Silicon oxide exhibits unipolar resistive switching behavior [37], which means that the polarity of driven voltage has no effect on the formation and rupture of conducting filaments, and the properties of conducting filaments. Therefore, the formation of horizontal tunneling diodes and the amount of emitted electrons are independent of the polarity of driven voltage. So attentions should be paid to the collection ratio. Due to the distinctive structure of the electron source, the polarity of driven voltage will affect the distribution of electric field above the electron source and further electrons trajectories, which in turn affects the collection ratio of emitted electrons by collecting electrode. To confirm the speculation, the trajectories of emitted electrons with different polarities of driven voltage are simulated.
To simulate the trajectories of emitted electrons, a single micro-emitter fabricated on silicon substrates with a silicon oxide layer of 300 nm is used as the model (Figure 3b). The micro-emitter occupies an area of 25 $\times$ 25 $\mu$m$^2$, equaling to the sizes of one micro-emitter in our real devices. Similar with the single micro-emitter in real devices, the micro-emitter model consists of two concentric conductive carbon films which are spaced by a square nanogap with a width of 100 nm and a side length of 11 $\mu$m. The inner carbon film is contact with the bottom Si layer through a 4.8 $\times$ 4.8 $\mu$m$^2$ square via hole. In the simulation, a collecting electrode with 25.2 V collecting voltage is set 30 $\mu$m above the micro-emitter, which imposes the same strength of electric field in the vacuum zone between electron emitters and collecting electrode as that of the real measurement. When simulating a forward biased electron emitter, the top electrode and bottom Si electrode are set to 0 V and $-21$ V, respectively. For a reversely biased electron emitter, the voltage setting is reversed. Electrons are assumed to be emitted vertically from the nanogap. To account for energy distribution of electrons, the initial energies of emitted electrons are set to be uniformly distributed in discrete values with an interval of 0.25 eV in range of 0–5 eV. Figures 3(c) and 3(d) show the simulation results when an electron emitter is forward and reversely biased, respectively. It can be seen that much more emitted electrons can fly away from the substrate or are collected by collecting electrode when electron source is forward biased (Figure 3c). While the electron emitter is reversely biased, considerable electrons return back to the substrate and are intercepted by inner graphene film (Figure 3(d)). We therefore attribute higher emission current of an electron source in forward bias than that in reverse bias to much lower interception of electrons in the former case. To make an electron source show higher effective emission current, it has to work in forward bias.

So what is the reason for lower conduction current when the electron source in figure 3(a) is forward biased? As is mentioned above, the inner graphene films electrically contact with the bottom silicon layer through via holes. A fact that cannot be ignored is that there exists a graphene/Si Schottky barrier at the interface between graphene and silicon because of their work function difference [38, 39]. Figure 4(a) shows the energy band diagram of graphene/p-type Si Schottky junction. If graphene is positively biased relative to p-type Si or an electron source is in forward bias, Schottky junction is reversely biased. Conversely, if graphene is negatively biased relative to p-type Si or an electron source is in reverse bias, Schottky junction is forward biased. These are in good agreement with the rectifying behavior of $I$–$V$ characteristic curve of the graphene/p-type Si Schottky junction as shown in figure 4(b). The $I$–$V$ curve in figure 4(b) was measured by applying a bias voltage to the top electrode relative to the bottom one. Graphene/p-type Si Schottky junction is therefore reversely biased when a positive bias voltage is applied to the top electrode. This explains well why conduction current is lower when an electron source is forward biased as shown in figure 3(a). As emission efficiency of a horizontal tunneling diode...
shows no dependency on the polarity of bias voltage and have a fixed value for a specific bias voltage, a higher conduction current will result in a higher emission current. To get a higher emission current, an electron source therefore needs to work with graphene/Si Schottky junction forward biased.

Electron sources fabricated on p-type substrate are found to experience frequent breakdown when they work with graphene/p-type Si Schottky junction reversely biased, which provides another reason for why an electron source needs to work with graphene/Si Schottky junction forward biased. Figures 4(c) and 4(d) show the results of six continuous voltage sweeps of the same electron source with $8 \times 8$ micro-emitters during its activation when graphene/Si Schottky junction was alternatively forward and reversely biased. Conduction current and emission current at a specific bias voltage in the case of forward biased Schottky junction (figure 4(c)) are, respectively, higher and lower than those in the case of reversely biased Schottky junction (figure 4(d)). Importantly, a sudden drop can be observed in both conduction current and emission current in the case of reversely biased Schottky junction. The current drops are attributed to breakdown of some activated micro-emitters. Figures 4(e) and 4(f) are SEM images of the electron source after breakdown. As can be seen from the figures, the breakdown occurred at the contact between silicon and graphene, where an explosion hole can be observed. When graphene/Si Schottky junction is reversely biased, the strength of electric field in depletion region of Si increases with the bias voltage increase, which eventually leads to avalanche breakdown. Because of the continuous breakdown of micro-emitters, micro-emitters of an electron source therefore cannot be completely activated and work at the same time, which significantly degrades overall emission current of an

Figure 4. Performances of electron sources fabricated on p-type SiO$_x$/Si substrate. (a) The energy band diagram of graphene/p-type Si Schottky junction. Note: $E_F$ is Fermi level; $E_v$ and $E_c$ are valence band top and conduction band bottom respectively; $E_{vac}$ is vacuum level; $\Psi$ is the height of Schottky barrier. (b) Typical I-V characteristic curve of the graphene/p-type Si Schottky junction. (c) $I_c$-$V_{bias}$ and $I_e$-$V_{bias}$ curves the electron source when it was forward biased. (d) $I_c$-$V_{bias}$ and $I_e$-$V_{bias}$ curves of the electron source when it was reversely biased. (e) SEM image of an electron source with micro-emitters broken down. (f) SEM image of a micro-emitter after breaking down.
electron source. However, the breakdown of micro-emitters seldom takes place when Schottky junction is forward biased as shown in figure 4(c).

In order to obtain higher conduction current and avoid breakdown of micro-emitters, an electron source has to work with graphene/n-type Si Schottky junction in forward bias or the top metal electrode negatively biased. However, when the top metal electrode is negatively biased, an electron source is in reverse bias and the effective emission current measured by the collecting electrode is significantly decreased due to the remarkable interception of electrons by the inner graphene films (figure 3). The dilemma can be overcome by using n-type silicon substrates instead of p-type silicon substrates to fabricate electron sources, which reverses the polarity of graphene/Si Schottky barrier. Figure 5(a) shows the energy band diagram of graphene/n-type Si Schottky junction. Figure 5(b) is the I-V characteristic curve of the graphene/n-type Si Schottky junction, which demonstrates the polarity of Schottky junction has changed when compared with figure 4(b). In the case of n-type silicon substrates, an electron source and graphene/Si Schottky junction can be forward biased at the same time by applying a positive voltage to the top metal electrode. Figure 5(c) shows the $I_c-V_{bias}$ and $I_e-V_{bias}$ curves of an electron source fabricated on an n-type Si substrate when it was forward and reversely biased. From the figure, we can see that both conduction current and emission current of an electron source in forward bias are higher than those in reverse bias when bias voltage is less than 21.4 V. The smaller conduction current after 21.4 V is attributed to the wider tunneling junction which dominates electron transport of an electron source when electron emission occurs. More significantly, there is no breakdown of micro-emitters when an electron source is forward biased. So a much larger bias voltage can be applied to an electron source to make it more fully activated and a higher emission current can be obtained. By using an n-type silicon substrate, emission current of a fully activated electron source containing $8 \times 8$ micro-emitters in the $200 \times 200 \mu m^2$ area can reach 100 $\mu A$, and the corresponding emission current density reaches 250 mA cm$^{-2}$ at bias voltage of 32.8 V (figure 4(d)).

Even though on-chip tunneling electron sources based on electroformed silicon oxide and graphene electrodes have been previously reported both experimentally and theoretically [29, 32, 33], we here report for the first time the effects of the polarity of driven voltage and the doping type of Si substrate on the performances of SiO$_x$-based tunneling electron sources with via holes. Compared with previously reported electron sources which employed the planar device structure without via holes in Ref. 32, 33, electron sources with via holes exhibits advantages of enhanced Joule heat dissipation, ease of parallel emitter array integration, and reduced electron interception by side electrodes. The results reported in this paper enable us to optimize the performances of our on-chip electron sources and increase their emission current closer to that needed for practical applications.

**Figure 5.** Performances of electron sources fabricated on an n-type SiO$_x$/Si substrate. (a) The energy band diagram of graphene/n-type Si Schottky junction. (b) Typical I-V characteristic curve of the graphene/n-type Si Schottky junction. (c) $I_c-V_{bias}$ and $I_e-V_{bias}$ curves of an electron source in both forward and reverse bias. (d) $I_c-V_{bias}$ and $I_e-V_{bias}$ curves of an electron source with $8 \times 8$ micro-emitters fabricated on an n-type substrate when it was forward biased.
4. Summary

We investigate the effects of the polarity of driven voltage and the doping type of Si substrate on the performances of a SiO$_2$-based tunneling electron source, which is composed of micro-emitters parallelly integrated between the top metal electrode and bottom Si one through via holes. Effective emission current and efficiency of an electron source are found to be significantly influenced by both the polarity of the driven voltage and the polarity of the Schottky barrier at graphene-Si contact. The performances of electron sources can be optimized by choosing n-type silicon substrate for device fabrication as it makes the positive influence of both the polarity of driven voltage and Schottky barrier achieved at the same time. By fabricating an electron source with 64 micro-emitters on n-type SiO$_x$/Si substrate, an emission current up to 100 μA and emission density of 250 mA cm$^{-2}$ are achieved. The work paves a way for realizing a large emission current by integrating large number of micro-emitters on a chip with our device structure.

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