A nanosecond-accuracy clock synchronization circuit for IEEE 1588-2008 using tapped delay lines

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Abstract: This letter presents a high-accuracy clock synchronization circuit, which reduces the time error between the master and slave clocks to less than 1 ns. To suppress quantization errors resulted in generation of time-stamps and pulse-per-second (PPS) signals, time-to-digital converters (TDC) and digital-to-time converters (DTC) have been implemented using tapped delay lines. The proposed scheme provides a cost-effective solution for applications of clock synchronization since it works on gigabit Ethernet using copper media (1000BASE-T) without any extra clock synthesis. Experimental results show that the two nodes over network share synchronized timing within the error between $-0.74$ ns and 0.89 ns.

Keywords: clock synchronization, IEEE 1588, tapped delay lines

Classification: Integrated circuits

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1 Introduction

Clock synchronization has captured a lot of attention in various applications including telecommunications, distributed measurement and control, and high energy physics since it becomes more critical to meet stringent timing requirements [1, 2, 3]. As IEEE 1588-2008 introduced transparent clocks (TCs) to address the asymmetric propagation delay issues [4], the experimental results of time errors less than 20 ns have been reported thanks to implementation of TCs [5, 6].

To achieve even higher accuracy, the next target to tackle is the quantization errors in generation of timestamps and pulse-per-second (PPS) signals. By taking timestamps with very stable 1-GHz clocks from signal generators, the time error less than 3 ns has once been observed between two computers connected directly with no network [7]. Using a clock faster than 1 GHz for better synchronization performance, however, makes circuit design very difficult. Asymmetry mitigation techniques based on line swapping and timestamp averaging has been presented recently [8]. The main challenge of the suggested approach, however, is to generate additional asynchronous clock. CERN has developed White Rabbit, the clock synchronization system based on IEEE 1588, to conduct very accurate experiments for sub-atomic particles [9]. Although WR provides the sub-nanosecond synchronization, the need for optical fibre cabling causes too much cost.

This letter presents a nanosecond-accuracy clock synchronization circuit using tapped delay lines. It is remarkable that the proposed scheme works on the low-cost copper-based Ethernet and only requires Ethernet clock from the transceiver and no additional clocks. Experimental results using the implementation in contemporary FPGAs show that the time error between the master and slave can be reduced into the range from −0.74 ns to 0.89 ns.

2 Clock synchronization based on IEEE 1588

IEEE 1588 specifies Precision Time Protocol (PTP) and mandates implementation of dedicated circuits to support the protocol. PTP works just like Network Time Protocol (NTP) [10] does with much higher accuracy on the order of sub-microsecond. A master has a stable reference clock and broadcast the timing information on SYNC messages. Then a slave over network adjusts its own local clock as close
to the masters as possible by exchanging PTP messages with the master and neighboring slaves.

Fig. 1 shows the overall architecture of the proposed circuit for clock synchronization. RX module extracts the timing information from the received PTP messages. If the slave has multiple network ports, the received SYNC messages, peer delay, and the calculated phase and frequency offsets are sent to the bus control to share them with the other ports. TX module simply forwards the received SYNC messages or sends new PTP messages for peer delay measurement. CLOCK module contains the very time register and keeps trying synchronize it to the master’s time. Based on the local time register, timestamps are generated to record the incoming and outgoing events of PTP messages. CLOCK module also generates PPS to indicate that the local clock reaches every second.

In many design cases with various implementation styles reported so far, asymmetric propagation delays often occupy the most significant portion of the overall time error. As the asymmetries have been corrected using transparent clocks, the time error is now dominated by quantization errors. Note that the non-deterministic errors in generation of timestamps and PPSs are accumulated up to tens of nanoseconds along the whole network path.

3 Circuit for high accuracy using delay lines

3.1 Time-to-digital converter for timestamp generation

A quantization error occurs because the timestamp itself does not contain the exact time when a PTP message crosses the boundary between the physical layer and data link layer. In many practical designs, an Ethernet device uses the local oscillator of 125 MHz as system clock source, and then the time register is being updated every 8 ns. Assume that system clock CLK lags to Ethernet receive clock RXCLK by 5 ns as shown in Fig. 2a. Although a timestamp should be taken when the start-of-frame delimiter (SFD) comes in at 995 ns, the actual coarse timestamp is generated at 1000 ns since the slave detects the SFD on the rising edge of CLK. The difference
between the coarse and ideal values can be compensated if we measure the phase difference between the two clocks, which is what a time-to-digital converter (TDC) does.

Fig. 2b shows a simple flash TDC [11] that converts the time difference between the rising edges of CLK and RXCLK. A tapped delay line makes multiple delayed RXCLK signals, which are provided to flip-flops. Each Q is then set when the delayed RXCLK rises earlier than CLK, and vice versa. As a result, the Q outputs make a thermometer code, which equals the phase difference between CLK and RXCLK. Here the number of 1’s is decoded into CLK_to_RXCLK[7:0] of 00000010 since only two flops give 1’s. As it is difficult to measure the absolute value of \( \tau \) directly, the phase difference in nanosecond scale can be calculated by the relationship

\[
\text{phase difference} = \frac{\text{CLK_to_RXCLK} \times \text{time per cycle}}{\text{CLK_to_CLK}},
\]

where \( \text{CLK_to_CLK} \) is an 8-bit code for the period of CLK measured using the same TDC and \( \text{time per cycle} \) is the exact time value for the period of CLK in nanosecond scale.

### 3.2 Digital-to-time converter for pulse-per-second generation

Another sort of quantization error also results from discontinuity of the local time register value. Consider a situation that the slave’s local clock \( \text{CLK}_S \) oscillates slower than the master’s \( \text{CLK}_M \) by 5 ppm and its phase is 5 ns later. As shown in Fig. 3a, the master keeps the reference time register TIME\(_M\) simply accumulating the exact 8 ns every cycle. Master’s pulse-per-second \( \text{PPS}_M \) asserts when \( \text{TIME}_M \) reaches 10 s. On the other hand, the slave keeps the synchronized time \( \text{TIME}_S \) accumulating 8.00004 ns every cycle. Although the exact 10 s in \( \text{TIME}_S \) would be reached in between 9,999,999,995 ns and 10,000,000,003 ns, \( \text{PPS}_S \) asserts at 10,000,000,003.00012 ns. To make the ideal \( \text{PPS}_S \) at the exact 10 s, a pulse should
be generated one cycle earlier and then delayed by 4.9992 ns using a digital-to-time converter (DTC).

The proposed DTC consists of a tapped delay line and a multiplexer as shown in Fig. 3b. PPS_{CLKS} asserts with CLK_{S} one cycle before TIME_{S} would exceed 10 s. For a single PPS_{CLKS} input, the delay chain makes multiple delayed pulses, which are provided to the multiplexer to select the precisely delayed one. Consequently, the DTC converts SELECT[7:0] code into the delay to apply to the original PPS_{CLKS}. SELECT is calculated as

$$SELECT = \text{phase\_offset} \times \frac{\text{CLK\_to\_CLK}}{\text{time\_per\_cycle}}$$

(2)

where phase\_offset is the amount of time by which the local clock is later than the master’s reference timing.

4 Experimental results

Measurement in the test setup as depicted in Fig. 4 shows the synchronization accuracy improved remarkably by applying the proposed scheme. IEEE 1588 master and slave are connected to a simple network with two transparent clocks. The master has the most accurate and stable reference clock from a pattern generator.
generator to broadcast SYNC messages. Receiving the messages, the slave then estimates the phase and frequency offsets to synchronize its local clock to the master’s timing. To emulate practical network situation, two dummy traffic generators introduce random propagation delays to the message exchanges. A high-speed digital sampling oscilloscope shows the time difference between PPS signals from the master and slave.

As shown in Fig. 5, the PPS from the slave $PPS_S$ has been captured for 10 minutes with $PPS_M$ as a trigger source. A histogram on the top of the screenshot shows the rising edges of $PPS_S$ are distributed over the range from $-0.74$ ns to $0.89$ ns. Note that experiments on the same conditions with the proposed circuits disabled show $PPS_S$ distributed in between $-17.2$ ns and $30.4$ ns. Applying the proposed scheme, the overall time error has been reduced down to less than one-thirtieth.

5 Conclusion

The clock synchronization circuit of sub-nanosecond accuracy has been presented using tapped delay lines to suppress quantization errors. Realized on contemporary FPGAs, the proposed circuit was verified to own the measured time error less than 1 ns. Moreover, gigabit Ethernet implementation on existing copper media without additional clock synthesis circuits makes it excellent for low-cost but high-accuracy applications.

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