Efficient Fault Detection Architecture of Bit-Parallel Multiplier in Polynomial Basis of GF(2^m) Using BCH Code

Saeideh Nabipour
Department Computer and Electrical Engineering
University of Mohaghegh Ardabili
Ardabil, IRAN
Saeideh.nabipour@gmail.com

Javad Javidan
Department Computer and Electrical Engineering
University of Mohaghegh Ardabili
Ardabil, IRAN
javidan@uma.ac.ir

Gholamreza Zare Fatin
Department Computer and Electrical Engineering
University of Mohaghegh Ardabili
Ardabil, IRAN
zare@uma.ac.ir

Abstract—The finite field multiplier is mainly used in many of today’s state of the art digital systems and its hardware implementation for bit parallel operation may require millions of logic gates. Natural causes or soft errors in digital design could cause some of these gates to malfunction in the field, which could cause the multiplier to produce incorrect outputs. To ensure that they are not susceptible to error, it is crucial to use a finite field multiplier implementation that is effective and has a high fault detection capability. In this paper, we propose a novel fault detection scheme for a recent bit-parallel polynomial basis multiplier over GF(2^m), where the proposed method aims at obtaining high fault detection performance for finite field multipliers and meanwhile maintain low-complexity implementation which is favored in resource constrained applications such as smart cards. The proposed method is based on BCH error correction codes, with an area-delay-efficient architecture. The synthesis results show that for 45-bit multiplier with 5-bit errors the proposed error detection and correction architecture achieves 37% and 49% reduction in critical path delay over the existing designs. Moreover, the area overhead for 45-bit multiplier with 5 errors is within 80% which is significantly lower than the best existing BCH based fault detection method in finite field multiplier.

Keywords—Finite Field Multiplier, Fault Detection, BCH Code, Error Correction, Area-Delay-Efficient Architecture

I. INTRODUCTION

The reliability of field-level product like memory and logic block has become a major concern, particularly as technology scales. High performance integrated circuits, which are characterised by high operating frequencies, low voltage levels, and small noise margins, will become more susceptible to various failures as integrated circuit density rises [16]. Furthermore, it has been recently demonstrated that, faults can be injected into the hardware for many digital signature and identification schemes by malicious attacks and resulting in inaccurate outputs that can entirely reveal the secret signatures. There are two categories for attacks against the hardware of digital design: invasive and non-invasive. While the invasive attacks require direct access to the internal components of the device which are costly, the non-invasive method, which is also known as the side channel attacks exploits the implementation weakness of the device [21]. Furthermore, malicious modification of hardware during design or fabrication which known as hardware trojan causes an integrated circuit (IC) to alter functional behavior. In these attacks, the secret information is obtained by injecting random events into the hardware, such as transitory failures [21].

Many important areas such as implementation of error-correcting codes (ECC), coding theory, computer algebra, pseudo random number generation, and digital signal processing have recently concentrated on finite field arithmetic. Multiplication is the fundamental arithmetic operation that has received the most attention among the basic arithmetic operations over finite fields GF(2^m) in the literature [2], [15], [17], [19]. This is mostly due to the fact that a multiplier’s implementation is significantly more complicated than that of a finite field adder, and because by repeatedly performing a multiplication operation, one can execute additional challenging field operations like inversion and exponentiation [1], [2]. Comparing finite field multiplication to its equivalents in integer and floating-point number systems reveals significant differences. The field size can be very high for many reliability applications, and each multiplier input can be 160 to 2,048 bits long. It is feasible that such multiplier will require millions of logic gates and it is possible that errors will occur in that computation [1]. Reliability applications could run more dependably if they had a multiplier that could detect errors online when certain faults were present [1].

Numerous techniques for detecting errors in finite field multipliers have been proposed in the literature. In [13] a parity prediction technique has been proposed to detect errors in bit-serial multipliers in GF(2^m). In their proposed method a special class of fields for error detection are defined using irreducible all-one polynomials. In [3], [8] the parity prediction technique has been applied for detecting faults in the architecture of the Advanced Encryption Standard (AES).

A data block can be encrypted (and decrypted) in the AES using a block key consisting of 11 rounds and each round has four operations. The 128-bit data block is divided into a number of bytes such as 16 bytes, and the polynomial \( z^8 + z^4 + z^3 + z + 1 \) generates each byte which is an element in the finite field GF(2^8). Then, arithmetic operations over GF(2^8) can be used for each round of the AES algorithm. [8] proposed a low-cost error detection technique for the AES hardware design, which requires one parity bit for each 128-bit data block and compares the predicted parity with the actual parity once each round. Error detection and recalulation methods are one of the well-known fault tolerant schemes for detecting/correcting single error which
were proposed in [4] and [9]. In the error detection and recalculation scheme, an error occurrence can be monitored by the concurrent error detection circuitry (CED) and, in case of one error, it rolls backs and recalculates again. The high delay penalty is the main disadvantage of this method. Another commonly used approach is the N-modular redundancy (NMR). In NMR, the actual functional block is replicated N times and the output is compared for correctness with a voter. The main drawback of this method is the hardware complexity which is increased with number of bit error corrections. Several methods named the SEC/DED schemes have been proposed for double error detection and single error correction. A single error correction (SEC) scheme based on the Hamming codes and LDPC codes have been proposed in [6] and [7] respectively. In [10] and [11] was proposed a dynamic error correction architectures, based on the BCH codes for bit parallel polynomial basis (PB) multiplier.

Motivated by BCH fault detection method proposed in [10] and [11], in this paper, we consider fault detection architecture for a novel bit-parallel polynomial basis (PB) multiplier GF(2^m) [17] based on an area-delay-efficient BCH decoder architecture that can detect and correct multiple errors in the case of multiple faults due to malicious attacks or natural causes that result in a number of errors at the output. Our technique fundamentally differs from the proposed technique in [10] and [11], in two critical issues. Firstly, our proposed bit parallel polynomial basis (PB) multiplier achieves low-area, so it would be preferable in situations where space complexity and saving energy are more relevant than time complexity such as parallel image watermarking in image sensors, a scenario which has area limitations, or a typical domestic application that needs a handful of IoT edge-devices. Secondly, for more area-delay implementation of our BCH decoder, we apply re-encoding technique and FIBM algorithm in the first and second sub-modules of BCH decoder respectively, and more importantly, Berlekamp-Rumsey-Solomon (BRS) algorithm [18], [20] have been used together with the Chien-search method in the third sub-module of BCH decoder to find the position of errors with least delay. We show that the proposed algorithms require less time and area overhead with compared to other proposed methods in the literature. The organization of this paper is described as follows: In Section I, we provide notations and preliminaries of a new bit-parallel polynomial basis (PB) multipliers in GF(2^m). In Section II, fault detection architecture for the proposed bit-parallel multipliers based on BCH codes is presented. Section IV presents the experimental results. Finally, the conclusion remarks are given in Section V.

II. PRELIMINARIES

Recently, a new class of low complexity multiplier based on the method of serial interleaved multiplication has been proposed in [17] which is investigated in this section. In terms of hardware complexity, the proposed formulated algorithm gates uses a well-known logical relation to replace the logical XOR (XNOR) gates with a NAND gate to implement multiplication more efficiently. This is mainly because NAND gate has a lower area and time complexities as compared to other gates such as AND or XOR/XNOR, which can significantly improve hardware complexity. As previously stated, the current research is focused on polynomial (canonical or standard) finite field elements. A development galois field can be entirely created by an m\textsuperscript{th} degree monic polynomial of the form, over GF (2^m).

\[ f(x) = \sum_{j=0}^{m-1} f_j x^j + 1 \]

assumed as an irreducible polynomial. If a polynomial over GF(2^m) of degree m is not divided by any polynomial over GF(2^m) of degree less than m, it is irreducible [14]. In polynomial basis, all elements of the extension field GF(2^m) can be formed as a result of polynomials over GF(2) of degree less than m [14]. Assume \( \alpha \in GF(2^m) \) shows a root of the irreducible polynomial over GF(2^m). Then, the polynomial basis is produced by the following set of m elements as \( (1, \alpha, \alpha^2, \ldots, \alpha^{m-1}) \), and \( f(\alpha) = 0 \). In GF(2^m), standard basis multiplication is usually done in two steps: ordinary polynomial multiplication and field polynomial reduction. Assume \( A(x) = a_0 + a_1 x + \ldots + a_{m-1} x^{m-1} \) and \( B(x) = b_0 + b_1 x + \ldots + b_{m-1} x^{m-1} \) be two field elements and \( C(x) = c_0 + c_1 x + \ldots + c_{m-1} x^{m-1} \) their product module where all \( a_j, b_j, c_j \in GF(2) \), then the finite field multiplication is accomplished by performing following equation [2]:

\[
C(x) = A(x) \times B(x) \mod f(x) = (a_0 + a_1 x + \ldots + a_{m-1} x^{m-1}) \times (b_0 + b_1 x + \ldots + b_{m-1} x^{m-1}) \mod f(x)
\]

\[
\sum_{j=0}^{m-1} b_j x^j A(x) \mod f(x)
\]

The product \( A(x) \times B(x) \mod f(x) \) must be computed firstly, resulting in a polynomial with a degree of no more than 2^m - 2. The modular reduction is conducted in a second stage, resulting in the polynomial C(x) with a degree of at most m - 1. Each \( b_j x^j A(x) \) in equation (1) can be carried out recursively as follow:

\[
C(x) = \ldots ((b_{m-1} x A(x) \mod f(x) + b_{m-2} A(x)) x \mod f(x) + b_{m-3} A(x)) x \mod f(x) + \ldots + b_1 x A(x) \mod f(x) + b_0 A(x)
\]
\[ P^{(1)}(x) \mod f(x) \]
\[ = \left( (p^{(1)}(m-1)x + p^{(1)}m-2x^{m-1} + \ldots + p^{(1)}1x + f_{0}) \mod f(x) \right) \]
\[ = \left( (p^{(1)}(m-1)x + f_{m-2}x^{m-1} + \ldots + f_{1}x + f_{0}) \right) \]
\[ = \left( (p^{(1)}(m-1)x + p^{(1)}m-2x^{m-1} + \ldots + p^{(1)}1x + p^{(1)}m-3x^{m-2} + \ldots + p^{(1)}1x + p^{(1)}0) \right) \]
\[ = \left( (p^{(1)}m-1x + p^{(1)}m-2x^{m-1} + \ldots + p^{(1)}1x + p^{(1)}m-3x^{m-2} + \ldots + p^{(1)}1x + p^{(1)}0) \right) \]
\[ \mod f(x) \]
\[ \text{(3)} \]

The term of \( b_{m-1}A(x) \) should be done \((m-1)\) times and can be considered as \( P^{k-1}(x) \), so module reduction will be done on \( xp^{k-1}(x) \), which \( p^{k-1}(x) \) is a partial-product polynomial constructed in iteration \((k-1)\)th. It can be written as a polynomial in the form \((m-1)\)deg:
\[ P^{K}(x) = P^{(k-1)}(x) + b_{m-k}A(x) \]
\[ \text{(4)} \]
For each \( k \leq m \), the equation \( (4) \) can be evaluated as follows, which \( k \) is the number of iterations,
\[ \text{for } k = 1: \quad P^{(0)}(x) = 0 \]
\[ \text{(5)} \]
\[ \text{for } k = 2: \quad P^{(1)}(x) = b_{m-1}A(x) \]

At the first, for evaluating \( P^{1}(x)x \mod f(x) \), \( P^{1}(x)x \) as the product polynomial needs to be performed and then be reduced using \( f(x) \) as follow:
\[ C(x) = \ldots [(b_{m-1}A(x) + b_{m-2}A(x))x + b_{m-3}A(x)]x + \ldots + b_{1}xA(x) + b_{0}A(x) \mod f(x) \]
\[ \text{(6)} \]
Based on equation \( (6) \), it can be seen that the modular reduction is decreased to the summation of \( p^{(k-1)}m-1f \) and \( P.x^{i} \). By left shifting \( P \) during \( i \) times, the \( P.x^{i} \) can be calculated, that can be represented in the following way:
\[ P^{(K-1)}(x) = p^{(k-1)}m-1f + P.x^{i} \]
\[ \text{(7)} \]
The product term \( b_{m-2}A(x) \) should be added to equation \( (2) \), due to the left-most term equation \( (1) \). For the next iteration, the result of summation can be denoted by \( P^{(2)}(x) \).

Therefore, the equation \( P^{K}(x) = P^{(k-1)}(x) + b_{m-k}A(x) \) should be repeated \( m \) times to carried out the final multiplication result of equation \( (1) \). It’s worth noting that the summation is done with XOR operator. So, equation \( (7) \) can be represented as:
\[ P^{K}(x) = P^{(k-1)}(x) \oplus b_{m-k}A(x) \]
\[ \text{(8)} \]

Since for every two logic variables \( a \) and \( b \), we can have
\[ (a \oplus b) = ((a \text{ NAND} (a \text{ NAND} b)) \text{ NAND} ((a \text{ NAND} b) \text{ NAND} b) \], the logical form of XOR operation can be reduced to an analogous circuit that just employs NAND that can be implemented efficiently as shown below:
\[ P^{K}(x) = P^{(k-1)}(x) \oplus (b_{m-k}A(x)) \]
\[ = P^{(k-1)}(x)\underbrace{b_{m-k}A(x) + P^{(k-1)}(x)b_{m-k}A(x)} \]
\[ = P^{(k-1)}(x)\underbrace{[P^{(k-1)}(x)\underbrace{b_{m-k}A(x)} + P^{(k-1)}(x)\underbrace{b_{m-k}A(x)}]} \]
\[ = P^{(k-1)}(x)\underbrace{b_{m-k}A(x) + b_{m-k}A(x)} \]
\[ \text{(9)} \]

The logical NAND operation is denoted by the letter \( \wedge \). It can be utilized rather than the logical XOR operation to obtain the required multiplication result, as shown in equation \( (9) \). This technique can considerably reduce hardware complexity as compared to the conventional equation. The suggested sequential PB multiplier’s architecture is shown in Fig. 1. Furthermore, the hardware details for the proposed design has been illustrated in Fig. 2. Both blocks are built up of four levels of logic gates, each of which has an array of \( m \) NAND gates to accomplish the NAND operations proposed in equation \( (9) \). For further details, refer to reference [17].

Fig. 1. The top-level of proposed structure for bit-serial sequential multiplier [17]
III. PROPOSED FAULT TOLERANT MULTIPLIER

3.1. BCH Codes

In this section, a novel technique based on BCH error correction codes for designing fault tolerant bit parallel multipliers over GF(2^m) is proposed. BCH codes are based on finite field arithmetic which operate under GF(2^m). Fig. 3 depicts the suggested fault-tolerant multiplier architecture. It includes one encoder and one decoder block in addition to the multiplier’s functional unit. As shown in Fig. 3, the output of the multiplier block is treated as a message that is encoded by the BCH encoder before being passed on to the error detection and correction block (syndrome generation and decoding).

Recently, BCH codes have received much attention due to their ability to correct and detect multiple faults. For any positive integers m (m ≥ 3) and t (t < 2^m-1), there exists a binary BCH code which is represented with following parameters [14]:

Block length:  n = 2^m − 1
Number of information bits:  k ≥ n − mt
Minimum distance:  d_{\text{min}} ≥ 2t + 1

Obviously, this code could correct any combination of t or fewer errors in a block of n = 2^m − 1 digits. This code is called a t-error-correcting BCH code. The generator polynomial of this code is defined in terms of its roots over the galois field GF(2^m) as discussed in [14]. Let \( \alpha \) be a primitive element in GF(2^m). The generator polynomial \( g(x) \) of the code is the lowest degree polynomial over GF(2), which has \( \alpha, \alpha^2, \alpha^3, \ldots, \alpha^{2t} \) and their conjugates as all its roots \([ g(\alpha^i) = 0, \ 1 \leq i \leq 2t ] \). Let \( \phi_i(x) \) be the minimal polynomials of \( \alpha^i \) then generator polynomial of BCH code is formed by finding the LCM of the minimal polynomials as follow [14]:

\[
g(x) = \text{LCM} \{ \phi_1(x), \phi_2(x), \ldots, \phi_{2t}(x) \}
\]  

3.2. BCH Encoder

Assume that a k-bit message is converted to an n-bit codeword. The BCH encoder takes a k-bit message as input and generates (n-k)-bit parity.

\[
c(x) = m(x)x^{n-k} + \text{rem}(m(x)x^{n-k})_{x^{(n-k)}}
\]

Where \( c(x) \) is the code word, \( m(x) \) is the output of multiplier block to be transmitted, and \( g(x) \) is the generator polynomial. Following encoding, the (n-k)-bit parity is combined with the k-bit message to generate a codeword that is kept in FIFO memory. The n-bit data is retrieved from memory and supplied into the BCH decoder for error detection and correction throughout the decoding process.

3.3. BCH Decoder

Fig. 4 shows a block diagram of the decoding process for a t-error correcting BCH code, which is divided into three basic steps:

A. SYNDROME GENERATOR

The 2t syndrome components \( S_1, S_2, \ldots, S_{2t} \) can be computed by substituting the field element \( \alpha, \alpha^2, \ldots, \alpha^{2t} \) into the received polynomial \( r(x) \) when decoding a t-error-correcting BCH code as follow:

\[
S_i = r(\alpha^i) = c(\alpha^i) + e(\alpha^i) = e(\alpha^i)
\]

\[
= \sum_{j=0}^{n-1} e_j (\alpha^i)^j
\]  

Fig. 2. Logic diagram of module G and H [17]
The syndromes are not all zero if the received codeword contains errors. The syndromes are a collection of the field elements in $GF(2^m)$, and each syndrome component is calculated as follow:

$$r(X) = q_i(X)\phi_i(X) + b_i(X)$$  \hspace{1cm} (13)

$\phi_i(X)$ is the minimal polynomial and $b_i(X)$ is reminder. Considering that $\phi_i(\alpha^i) = 0$, syndrome components can be calculated by evaluating $b_i(X)$ with $X = \alpha^i$. As a result, we have the equation:

$$S_i = r(\alpha^i) = b_i(\alpha^i)$$  \hspace{1cm} (14)

Our syndrome block has been implemented in parallel for low-latency implementation. As pointed out in [14] for binary BCH codes, we have $S_{2j} = S_j^2$, so only $t$ parallel syndrome generators are needed to calculate the odd-indexed syndromes, followed by considerably simpler square circuits that can process $p$ input bits in one cycle, as mentioned in [14]. The decoding latency is a critical factor in achieving a high-performance fault detection circuit. A codeword $r(X)$ read from a channel is re-encoded as a pretreatment of the syndrome computation, known as the re-encoding approach, to reduce the latency of BCH decoding [5]. It is an effective method that is achieved with no additional circuit by utilizing the BCH encoder that is idle at that time. So, for the syndrome generator in our decoder, a re-encoding strategy is used before the actual decoding, with no additional hardware cost, by re-using the BCH encoder that is idle at the moment. For further details, refer to reference [5].

### B. Finding Error-Location Polynomial:

The BCH decoding procedure continues with the key equation solver. If any of the syndrome values are non-zero, there has been an error, and this step is used to obtain the key equation, where $i$ is the number of error bits to be corrected.

$$\sigma(X) = \sigma_0 + \sigma_1 X + \sigma_2 X^2 + \ldots + \sigma_v X^v$$

$$\sigma(X) = (1 + \beta^i X)(1 + \beta^2 X) \ldots (1 + \beta^v X)$$  \hspace{1cm} (15)

$$\sigma(x) = 1 + \sigma_1\alpha^i + \ldots + \sigma_v(\alpha^i)^i = 0$$

The Berlekamp-Massey algorithm (BMA) [14] is a well-known iterative approach for determining error-location polynomials. The error locator polynomial can be calculated using a variety of hard-decision decoding techniques, including the Peterson algorithm, Berlekamp–Massey algorithm, and the Euclidean algorithm among which Berlekamp-Massey (BM) algorithm is the most well-known algorithm in BCH decoding process. Furthermore, many formulation algorithms of the BM method have been proposed in the literature among which FiBM technique offers the lowest hardware complexity of all available algorithms for binary BCH code, making it more appropriate for low-power VLSI implementations like the one utilized in our BCH decoder. For further details, refer to reference [12].

### C. Chien Search Algorithm

The last step is to determine the error locations by finding the roots of error locating polynomial (identifying the position of erroneous bit). The most well-known algorithm is Chien search method, in which all $2^m$ possible elements of Galios field are substituted into the error polynomial, one after another, and the polynomial is evaluated. If the result is equal to zero, then there will be a root for the polynomial. Chien search circuit produces an error vector $e$ in such a way that, if $\alpha^i$ is a root, then the $(n-i)th$ component $e_{n-i} = 1$; otherwise $e_{n-i} = 0$ for all $0 \leq i \leq n - 1$. Finally, error will be corrected in the received codeword.

### 3.4. Improved Error Locator Design

Finding of the positions of the errors is one of the most time-consuming stages of BCH decoding. Chien search algorithm has very high time complexity for the case of large fields and polynomials of high degree. To make the root-finding problem more efficient for BCH decoder, the Berlekamp-Rumsey-Solomon (BRS) algorithm [18], [20], together with the Chien-search method, is developed in order to find the roots of error locator polynomial for BCH decoder. Before description of the algorithm, first consider some definitions and a theorem that are needed to develop this algorithm.

**Definition 1**: The polynomial $L(y)$ over $GF(2^m)$ is called a $p$-polynomial or linearized polynomials for $p=2$ if:

$$L(y) = \sum c_i y^{2i}, \text{where } c_i \in GF(2^m)$$  \hspace{1cm} (16)

**Definition 2**: An affine polynomial is a polynomial such as $A(y)$ over $GF(2^m)$ if

$$A(y) = L(y) + \beta$$  \hspace{1cm} (17)

Where $L(y)$ is a $p$-polynomial and $\beta \in GF(2^m)$.

**Theorem 1**: Let $y \in GF(2^m)$ and let $a_0, a_1, a_2, \ldots, a_{m-1}$ be a standard basis. If $y$ is represented in the standard basis, i.e.,

$$y = \sum_{k=0}^{m-1} y_k \alpha_k$$  \hspace{1cm} (18)

where $y_k \in GF(2)$, then

$$L(y) = \sum_{k=0}^{m-1} y_k L(\alpha_k)$$  \hspace{1cm} (19)

Let us consider a simple quadratic $p$-polynomial over $GF(2^3)$, such as $A(y) = y^3 + a^3 y + a^4 = 0$ that can be rewritten as

$$y^2 + a^3 y = a^4 = a^2 + a + 1$$  \hspace{1cm} (20)

Let $\alpha$ be the primitive element of $GF(2^3)$. Here, $P(x) = x^3 + x^2 + 1$ is the primitive polynomial. If we consider left-hand side of equation (20) as $L(y) = y^2 + a^3 y$, then...
which is a $p$-polynomial over $GF(2^2)$, (20) can be expressed as:

$$L(y) = \alpha^2 + \alpha + 1$$  \hspace{1cm} (21)

If $y = y_2 \alpha^2 + y_1 \alpha + y_0 \in GF(2^3)$, with regard to theorem 1, (21) can be written as:

$$y_2 L(\alpha^2) + y_1 L(\alpha) + y_0 L(0) = \alpha^2 + \alpha + 1$$  \hspace{1cm} (22)

Where

$$L(\alpha^0) = L(1) = 1 + \alpha^3 = \alpha^2,$$
$$L(\alpha) = L(1) = \alpha^2 + \alpha^3 = \alpha + 1,$$
$$L(\alpha^2) = \alpha^4 + \alpha^3 = \alpha^2$$  \hspace{1cm} (23)

by substitution of (23) into (22) we have:

$$(y_2 + y_0) \alpha^2 + y_1 \alpha + y_0 = \alpha^2 + \alpha + 1$$  \hspace{1cm} (24)

It can be expressed as a matrix form as following:

$$\begin{bmatrix} y_2 & y_1 & y_0 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$  \hspace{1cm} (25)

It is obvious that the roots of (20) can be found by solving the three simultaneous equations given in (25) with three unknown $y_0, y_1$ and $y_2$. Evidently solutions of (24) are $y = 011$ and $y = 110$, which are two roots of (24). From this example, it is clear that instead of all of the values $L(\alpha^0), L(\alpha^1), \ldots, L(\alpha^6)$ required in the Chien-search method, computing of the three values $L(\alpha^0), L(\alpha^1)$ and $L(\alpha^2)$ is only needed. The aforementioned Berlekamp-Rumsey-Solomon (BRS) algorithm together with chien search algorithm can be used to easily find all the roots of error locator polynomial. The main feature of this algorithm is grouping of some summands of the polynomial of degree not higher than 11 into multiples of affine polynomials which can be evaluated using very small pre-computed tables leading to fast computation. For the sake of clarity, polynomial root finding of degree 6 is also examined.

Let $\sigma_6 x^6 + \sigma_5 x^5 + \sigma_4 x^4 + \sigma_3 x^3 + \sigma_2 x^2 + \sigma_1 x + \sigma_0 = 0$ is a polynomial of degree 6, or $A_6(x) = B_6(x)$ Where $A_6(x) = \sigma_4 x^4 + \sigma_2 x^2 + \sigma_1 x + 1$ and $B_6(x) = \sigma_6 x^6 + \sigma_5 x^5 + \sigma_3 x^3$. Since $A_6(x)$ is an affine polynomial over $GF(2^6)$, then the values of $A_6(\alpha), A_6(\alpha^2), \ldots, A_6(\alpha^{2^{m-1}})$ can be obtained by applying of algorithm illustrated in previous example.

On the other hand, the values of $B_6(\alpha), B_6(\alpha^2), \ldots, B_6(\alpha^{2^{m-1}})$ can be obtained by Chien-search method. If $A(\alpha^i) = B(\alpha^i)$ for $1 \leq i \leq 2^m - 1$, then $x = \alpha^i \in GF(2^m)$ is the solution of $A_6(x) = B_6(x)$ . Therefore, by exhaustively searching all nonzero field elements in $GF(2^m)$ for the roots of $A_6(x) = B_6(x)$, there exists a set of field elements such that they satisfy $A_6(x) = B_6(x)$. These solutions are the roots of $\sigma_6 x^6 + \sigma_5 x^5 + \sigma_4 x^4 + \sigma_3 x^3 + \sigma_2 x^2 + \sigma_1 x + \sigma_0 = 0$ for further details, refer to reference [18], [20].

VI. EXPERIMENTAL RESULT

The VHDL models of the proposed fault-tolerant based on BCH error correction codes for two structures of 16-bit and 45-bit multiplier are modelled and then simulated and synthesized using the Synopsys tools in the UMC technology library, using the 0.18 micron CMOS technology to verify its functionality. Synopsys Power CompilerTM was also used to estimate the power consumptions. It is worth mentioning that the technique can be easily extended to bit parallel multipliers of any size. Table 1 shows the comparison of attributes such as delay, area, power consumption, ADP (area-delay product) and PDP (power-delay product) of 16-bit and the 45-bit PB GF multipliers in our method versus the proposed PB GF multipliers in [10]. These designs are synthesized in both 180nm and 90nm TSMC technology. It can be observed from implementation results that the proposed multiplier implementation in 180nm technology achieves 69% and 66% reduction in area-delay product (ADP) and 72% and 76% reduction in power-delay product (PDP) for 16-bit and 45-bit multiplier over the proposed multiplier in [10], respectively. Furthermore, in 90nm technology, for 16-bit and 45-bit multiplier, the proposed architecture offers 88% and 98% area-delay improvement (ADP) and 85% and 81% power-delay product improvement (PDP) in comparison with multiplier in [10], respectively. Hence, the FPGA implementation results confirms that the proposed multiplier achieves better area-delay product and power-delay product (PDP) complexities than that of the multiplier in [10].
Table 1. Comparison of 16-bit and 45-bit GF Multiplier Specifications with the proposed GF Multiplier in [10].

| Multiplier Size | 16-bit Multiplier [10] | The proposed 16-bit Multiplier | 45-bit Multiplier [10] | The proposed 45-bit Multiplier |
|-----------------|------------------------|--------------------------------|------------------------|--------------------------------|
| Area (µm²) -180nm | 10863.2 | 6523.2 | 77514.5 | 56212 |
| T-Power (µW) -180nm | 489 | 264 | 3300 | 1650 |
| Delay(ns) -180nm | 3.11 | 1.6 | 6.86 | 3.2 |
| ADP | 33784.55 | 10437.12 | 531749.47 | 179878.4 |
| PDP | 1520.79 | 422.4 | 22638 | 5280 |
| Reduction in ADP | 0.69% | - | 0.66% | - |
| Reduction in PDP | 0.72% | - | 0.76% | - |
| Area (µm²) -90nm | 3029.4 | 1065.2 | 19795.6 | 564.2 |
| T-Power (µW) -90nm | 78.5 | 34.2 | 375.46 | 105.45 |
| Delay(ns) -90nm | 0.6 | 0.2 | 1.06 | 0.7 |
| ADP | 1817.64 | 213.04 | 20983.33 | 394.94 |
| PDP | 47.1 | 6.84 | 397.98 | 73.81 |
| Reduction in ADP | 0.88% | - | 0.98% | - |
| Reduction in PDP | 0.85% | - | 0.81% | - |

Table 2 compares the delay overhead of the proposed fault tolerant method based on BCH decoder in both 180 nm and 90 nm TSMC technology for the 16-bit and 45-bit BCH code with the capability of correcting 5 errors with BCH decoder design proposed in [10]. It is obvious that with the proposed Berlekamp-Rumsey-Solomon (BRS) algorithm together with the Chien-search method, in 180nm and 90nm technology the computation delay for detection of errors in multiplier output is 0.56% and 0.66% for BCH(31,16) and 0.37% and 0.49% for BCH(63,45) lower than the Chien search block in [10], respectively. So, the proposed algorithm could result in the lowest delay in finding the position of errors in the multiplier output.

Table 3 compares the hardware complexity of our proposed fault tolerant method based on BCH decoder with method [10]. The proposed method offers 85.4%, 92.4% and 90.4% hardware improvements for 3, 4 and 5 errors with compare to its counterpart BCH based fault tolerant method in [10], respectively. It is obvious that our proposed fault tolerant algorithm are more area efficient. This is mainly because, in terms of area overhead, we used re-encoding method which is performed before the actual decoding and can be performed for the syndrome generator with no additional hardware cost by re-using the BCH encoder that is idle at that time. Furthermore, while in [10] Peterson’s algorithm has been used in second stage of BCH decoding that it’s complexity increases significantly for larger t, in our decoder, FIBM algorithm applied which can save huge amount of silicon area and reduce the power consumption. More importantly, our proposed bit-parallel polynomial basis (PB) multipliers offers area-efficient architecture with compare to the multiplier in [10], because in our implementation no XOR gates are required and it can be completely used using NAND gate leading to regularity and modularity of VLSI implementation of finite field multipliers.

Table 2. Delay Comparison of Proposed ECC Blocks BCH with [10].

| Scheme | Delay(ns)-180nm | Delay(ns)-90nm | Reduction in Delay-180nm | Reduction in Delay-90nm |
|--------|----------------|----------------|--------------------------|--------------------------|
| BCH(31, 16) [10] | 7.8 | 1.95 | 0.56% | 0.66% |
| The proposed BCH(31, 16) | 3.4 | 0.658 | - | - |
| BCH(63, 45) [10] | 11.76 | 2.37 | 0.37% | 0.49% |
| The proposed BCH(63, 45) | 7.4 | 1.2 | - | - |

VII. CONCLUSION

Error correction is an effective way to mitigate fault related attacks in reliability applications. In this paper, we have considered an area-delay efficient fault detection architecture based on BCH error correction code in a new parallel polynomial basis multipliers which has capability of correcting multiple errors. The paper also proposed an optimized Berlekamp-Rumsey-Solomon (BRS) algorithm [18], [20], together with the Chien-search algorithm for finding the roots of the error locator polynomials in BCH error correction decoder with least delay which gives the location of errors in the multiplier output. The proved complexity analysis of the proposed scheme in this paper has a lower complexity in terms of area and delay and power compared with other existing well known technique which is desirable in constrained applications, such as smart cards, IoT devices, and implantable medical devices.

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