Three-level Generalized Discontinuous Pulse-width Modulation Strategy Considering Neutral Point Potential Balance

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Abstract. Traditional discontinuous pulse width modulation (DPWM) cannot be efficiently used in some inverters like active power filters (APFs) whose currents are difficult to predict. Therefore, this paper proposes a new generalized discontinuous pulse width modulation (GDPWM) strategy considering neutral point potential balance for neutral-point clamped (NPC) three-level inverters. The core of the proposed strategy is the optimal efficiency modulation strategy. The optimal efficiency modulation strategy determines the clamp mode in real time based on the current flowing through the converter. This strategy minimizes switching losses by clamping the converter to the phase with the largest absolute value of current. At the same time, according to the neutral point potential shift, the neutral point balance strategy and the optimal efficiency modulation strategy are switched to achieve the balance between the switching loss and the neutral point potential. The proposed strategy can be efficiently applied in NPC three-level APFs to minimize the switching losses without the need of predicting the currents and to make neutral point potential balance. In this paper, the proposed modulation strategy is theoretically analyzed, and simulation and experimental verification are carried out.

1. Introduction

The three-level topology has many advantages such as less output harmonics, easy to use for higher voltage conditions, and less filter inductance. It is widely used in APFs, photovoltaic power generation [1]–[2] and so on. As the voltage and current level of the grid-connected device increases, the switching loss also increases. To ensure the safety of the converter, the switching frequency of the converter is limited to a certain range. Thereby it is especially important to reduce switching losses and increase the equivalent switching frequency. DPWM is a modulation strategy that can be applied to three-level converters and effectively reduce switching losses [4]. Due to the many advantages of this modulation strategy, it is also widely used in APFs [3], inverter [4] and many other fields. This modulation strategy can reduce switching losses by reducing the frequency of actions per switching device while the equivalent switching frequency is constant.

Many scholars around the world have done a lot of research on traditional DPWM strategies. Many papers introduce a variety of different traditional three-level DPWM strategies. Literature [5] introduced its principle and implementation method. And Literature [6] compared the switching losses and harmonic characteristics of these different DPWM strategies. It can be seen that the common feature of the traditional DPWMs is that the clamp interval is fixed, and only related to the position of the voltage level.
vector. The neutral point potential fluctuation problem is an inherent problem of the NPC three-level topology. In order to make the converter of this structure safe and stable, it is necessary to ensure that the neutral point potential balance [8]. Literature [9], [10] introduced a method to solve the three-level neutral point balance problem by two different DPWMs switching methods. There are few papers on how to achieve an optimal efficiency modulation strategy for the case where the current cannot be predicted. Only the literature [11] proposed a GDPWM method for the two-level APF to clamp in the maximum phase of the current, and similar modulation methods for the three-level converter have little research. In this paper, a GDPWM strategy considering the neutral point potential balance is proposed for the characteristics of three-level converters with difficult current prediction. The modulation strategy can well balance the control of the neutral point potential balance and the optimal efficiency modulation strategy, so that the converter achieves optimal efficiency within the allowable range of the neutral point potential fluctuation.

The three-level modulation method generally adopts space vector pulse width modulation (SVPWM) and carrier-based pulse width modulation (CBPWM). According to the literature [12], the two modulation methods are essentially the same. Since SVPWM is more intuitive in describing the modulation methods described herein, SVPWM is used herein to describe the modulation strategy.

2. The basic principle of three-level DPWM

2.1. NPC three-level converter topology and switch vector

The NPC three-level converter topology is shown in Figure 1. As can be seen from the figure, the converter topology consists of four switching tubes with anti-parallel freewheeling diodes and two clamping diodes per phase. Each phase can output three levels, and the phase A is used as an example to define the following. When \( S_{a1} \) and \( S_{a2} \) are turned on and the output level is \( +U_{dc1} \), the switching function \( S_A \) is 2; When \( S_{a2} \) and \( S_{a3} \) are turned on and the output level is 0, the switching function \( S_A \) is 1; When \( S_{a3} \) and \( S_{a4} \) are turned on and the output level is \( -U_{dc2} \), the switching function \( S_A \) is 0; Similarly, the definitions of B and C phase switching functions \( S_B \) and \( S_C \) can be obtained.

For a three-level converter topology, there are three switching states for each phase, and a total of 27 switching states for three phases. Analysis of Figure 2 shows that 27 switch states correspond to 19 switch vectors.

2.2. The basic principle of three-level DPWM

According to the nearest three vector principle of the three-level space vector modulation method [12]. The DPWM strategy is to select one of the two redundant switching states of the small vector so that one phase is clamped to a certain level during each switching cycle. Compared with continuous PWM, the purpose of reducing switching losses at the same equivalent switching frequency is achieved. However, since there is no complementary small vector complement, the neutral point potential fluctuation is caused. According to this principle, different clampable ways in each small area can be obtained as shown in Figure 3.

Figure 1. Topology of NPC three-level inverter

Figure 2. Space vector of three-level inverter

Figure 3. Clamp figure of three-level DPWM in sector 1
3. Three-level neutral point potential balance GDPWM strategy

3.1. Neutral point potential balance principle

The neutral point potential balance problem is an inherent problem of the NPC three-level structure. Inconsistent switching characteristics, inconsistent circuit parameters such as capacitors will cause fluctuations in the neutral point potential. The traditional three-level DPWM method does not consider the problem of neutral point potential balance. The neutral point potential imbalance is further exacerbated by the fact that one phase level is clamped and a small vector that compensates for each other cannot be used.

For any phase bridge wall, when the output is 0 level, the current flows into or out of the neutral point of the DC voltage, that is, the neutral point of the two capacitors. This will cause the neutral point potential to shift. The DC neutral point current $i_0$ is shown as the formula (1):

$$i_0 = i_a(1-|S_a-1|) + i_b(1-|S_b-1|) + i_c(1-|S_c-1|)$$

(1)

Among them, $S_a$, $S_b$, and $S_c$ are respectively ABC three-phase switch states; $i_a$, $i_b$, and $i_c$ are respectively the three-phase outflow current of the converter ABC. The offset of the neutral point potential $(\Delta U_{dc})$ after a switching period $T_s$ from time $t$ is as shown in formula (2):

$$\Delta U_{dc} = \frac{1}{C} \int_{t}^{t+T_s} i_0(t)dt$$

(2)

$$\Delta U_{dc} = \frac{1}{C} \int_{t_c}^{t_{c+T_{n}}} i_a(t)(1-\left|S_{an}-1\right|) + i_b(t)(1-\left|S_{bn}-1\right|) + i_c(t)(1-\left|S_{cn}-1\right|) dt$$

(3)

In summary, (1) and (2) can obtain the change of the neutral point potential in the action time of a certain switch vector as shown in formula (3), where $T_n$ (n can take 1, 2, 3) is the action time of the nth switch vector. And the neutral point potential change in one switching cycle is as shown in formula (4).

$$\Delta U_{dc} = \Delta U_{dc1} + \Delta U_{dc2} + \Delta U_{dc3}$$

(4)

For large vectors, for example, (2,0,0), with (1), the inflow neutral point current is 0. Other large vector inflow neutral point currents are equally available, and large vectors have no effect on the neutral point potential. For the medium vector, for example, (2,1,0) brings in (1), the current flowing into the neutral point is $i_b$. Other medium vector inflow neutral point currents are equally available. Since the medium vector has no redundant switching state, its influence on the neutral point potential is related to the current. For small vector two redundant switch states, such as (1,0,0), (2,1,1) brought in (1), there are inflow neutral point currents $i_a$ and $i_a$ respectively. Similarly, the inflow neutral point current of other small vectors can be obtained. The switching states of the small vectors that are redundant with each other have the opposite effect on the neutral point potential.

The following analysis analyzes the influence of the DPWM strategy on the neutral point potential of different switching states in the same region, taking the first sector A region as an example. As shown in Figure 3, there are three clamp modes in Zone A, namely 1XX, X1X and XX1. The switching states of the three clamp modes are respectively brought into (1), (3), and (4), and the influence of the neutral point potential in each clamp mode can be derived. The switching vector used in each clamp mode and its effect on the neutral point potential are shown in Table 1, where $T_x$, $T_y$, and $T_z$ are the action times of the x, y, and z vectors, respectively. It can be seen from Table 1 that different clamp modes have different effects on the neutral point potential, and this characteristic can be used to formulate a modulation strategy to ensure the neutral point potential balance.
3.2. neutral point potential balanced DPWM modulation strategy

It can be seen from Table 1 that the effect of different clamping modes on the neutral point potential is only related to the integral value of the associated current. Since the time of each switching cycle is very short, we use the current and time product to approximate the integral. The definition of the neutral point impact factor (NPIF) is shown in formula (5). $\Delta U_{dcT}$ can be converted to NPIF as shown in Table 1.

$$NPIF = \left( U_{dc1} - U_{dc2} \right) \left( C \cdot \Delta U_{dcT} \right)$$

(5)

| Clamp mode | $\Delta U_{dcT}$ | NPIF |
|------------|----------------|------|
| 1XX        | $\frac{1}{C} \left( \int_{t_a}^{t_b} i_a \, dt + \int_{t_f}^{t_e} i_e \, dt \right)$ | $(U_{dc1} - U_{dc2}) \left( \overline{i_a} \cdot i_a + \overline{i_e} \cdot i_e \right)$ |
| X1X        | $\frac{1}{C} \left( \int_{t_a}^{t_b} i_a \, dt + \int_{t_f}^{t_e} i_e \, dt \right)$ | $(U_{dc1} - U_{dc2}) \left( \overline{i_a} \cdot i_a + \overline{i_e} \cdot i_e \right)$ |
| XX1        | $\frac{1}{C} \left( \int_{t_a}^{t_b} i_a \, dt - \int_{t_f}^{t_e} i_e \, dt \right)$ | $(U_{dc1} - U_{dc2}) \left( \overline{i_a} \cdot i_a - \overline{i_e} \cdot i_e \right)$ |

Where $\overline{i_a}, \overline{i_b}, \overline{i_c}$ is the algebraic average of the sampling current and the reference current. Compare the three NPIFs to get the maximum of them. The clamp mode with maximum NPIF is optimal, and the switching state of the mode is selected as the switching vector.

4. Three-level optimal efficiency GDPWM modulation strategy

The core of the modulation strategy proposed in this paper is the optimal efficiency GDPWM strategy. The difference between this modulation strategy and the traditional DPWM strategy is that this modulation strategy can determine the clamp mode in real time according to the current sampling under the premise that the current is unpredictable, so that the switch clamps as much as possible in the phase with the largest absolute value of the current. This reduces switching losses.

4.1. Three-level optimal efficiency GDPWM strategy

As shown in Figure 3, the reference voltage vector can have at least two clamping modes in any one area. There are three clamping modes in the A and C areas. In these two regions, when the absolute value of any phase current is the maximum value of the three phases, the level clamp control of the corresponding phase can be realized in the modulation. In the other two areas, the B and D areas can achieve two-phase level clamping. The above redundant characteristics provide theoretical possibilities for the modulation strategy proposed in this paper.

The basic modulation process of the optimal efficiency GDPWM is as follows. Under the condition that the neutral point potential satisfies the optimal modulation strategy (the method of judging is introduced later). Firstly, according to the sampling current, the phase with the largest absolute value of the current is determined from the three-phase current. Secondly, in the region where the reference voltage is located, the clamp mode is selected based on the principle that the absolute value of the clamp phase potential is the largest. That is, the switch vector used is determined. If the reference voltage vector is in a region similar to the B and D regions, which has only two redundant states, and the phase with the largest absolute value of the current is just not clamped, then select a phase with the second largest absolute value of the current as the clamp phase to ensure that the switching loss is minimized.

For example, the absolute value of phase A current is the largest, and the reference voltage vector is as shown in Figure 3. Phase A potential can be clamped to a high level during this switching cycle. Therefore, the selected switching vector is $(2,1,0)$, $(2,2,0)$, and $(2,1,1)$. The above completes a selection process of the switch vector.
4.2. Comparison of switching loss between optimal efficiency GDPWM strategy and traditional DPWM strategies

For inverters operating at a constant DC bus voltage, it is assumed that the switching frequency of the device is infinite and the current varies linearly during turn-on and turn-off of the device. The switching loss at this time is actually proportional to the load current. The switching loss $P$ in one fundamental period can be determined by formula (7) and (8) [6]. Where $U_e$ is the equivalent DC voltage, $I_m$ is the load current amplitude:

$$P = U_e I_m \frac{1}{2\pi} \int_{0}^{2\pi} f(\theta) d\theta$$

(6)

$$f(\theta) = \begin{cases} 0, \text{Clamped} \\ \cos(\theta + \varphi), \text{Not clamped} \end{cases}$$

(7)

Define the switching loss function (SLF) as formula (9). Where $P_{ref}$ is the continuous PWM switching loss.

$$SLF = \frac{P}{P_{ref}} = \frac{1}{4} \int_{0}^{2\pi} f(\theta) d\theta$$

(8)

Define the modulation index (MI) as shown in formula (10). Where $U_{dc} = U_{dc1} + U_{dc2}$ is the total voltage on the DC side. MI is 1 on the inscribed circle of the hexagon in Figure 2.

$$MI = \frac{\sqrt{3} |V_{ref}|}{U_{dc}}$$

(9)

According to the definition of several traditional DPWM strategies such as DPWM0, DPWM1, DPWM2, DPWM3, DPWMmin, DPWMmax, and the principle of efficiency GDPWM strategy in Section 3.1, the SLF diagram of three-phase symmetrical current under different power factors can be made as shown in Figure 4.

It can be seen from the figure that when MI<0.577, the SLF of optimal efficiency GDPWM strategy is stable to 0.5 regardless of the power factor angle. This is because the reference voltage vector is now located in the internal subspace similar to the A region in Figure 3. Therefore, according to the principle of the optimal efficiency GDPWM strategy, the voltage is always clamped to the phase with the largest absolute value of the current. With the increase of MI, the reference voltage vector becomes longer, and there are more and more cases in the area where only two clamping methods are used. In the case where $|\varphi|$ is large, as the MI increases the SLF will become larger. The SLF reaches the maximum when MI=1 as shown in Figure 4. When -30° < $|\varphi|$ < 30°, the SLF is kept at 0.5 and does not change with the change of MI.

It can be seen from Figure 4 that the SLF of the optimal efficiency GDPWM is smaller than any other traditional DPWM strategy regardless of the MI and the power factor angle, which is the advantage of the modulation strategy.

4.3. Comparison between the optimal efficiency GDPWM strategy and the traditional DPWM strategies for the fundamental and harmonic modulation waveforms

The traditional DPWM takes DPWM1 as an example, and the clamp mode of DPWM1 is shown in Figure 5 [3]. The clamp mode determines the switching vector based only on the position of the voltage vector, independent of the current flowing through the converter.
The reactive current is emitted when MI<0.57, and the modulation waveforms of the two modulation strategies are compared as shown in Figure 6. In Figure 6, there are the three-phase current diagram, the A-phase voltage diagram under the DPWM1 strategy, and the A-phase voltage diagram under the GDPWM strategy. In the case of MI<0.57, the voltage vector is always in the internal subspace, and the optimal efficiency GDPWM is always clamped to the phase with the largest absolute value of the current, so the comparison of the two modulation methods is more intuitive. In the waveform diagram of the DPWM1 strategy, it can be seen that the voltage is usually clamped in the region where the absolute value of the current is small. In the waveform diagram of the optimal efficiency GDPWM strategy, it can be seen that the voltage is clamped in the region where the absolute value of the a-phase current is the largest among the three phases. This figure intuitively reflects the advantages of optimal efficiency GDPWM in reducing switching losses.

Figure 7 shows a case where the modulated wave is a fundamental voltage and the converter emits a harmonic current at a low MI. Here, the fifth harmonic is taken as an example. In Figure 7, there are the three-phase current diagram, the phase A voltage diagram under DPWM1 strategy and the phase A voltage diagram under GDPWM strategy. It can be seen that in one fundamental period, the voltage waveform of the GDPWM strategy has multiple clamp intervals, and each clamp interval corresponds to the interval in which the absolute value of the A-phase current is the largest. The clamp interval of...
the DPWM1 strategy is fixed in the region near the peak of the reference voltage. The comparison of the two strategies shows that the GDPWM strategy has a lower switching loss.

5. GDPWM modulation strategy considering neutral point potential balance

5.1. Switching method between two modulation strategies

The purpose of the modulation strategy proposed in this paper is to reduce the switching loss as much as possible to improve the efficiency of the device, and to ensure the neutral point potential balance, so the switching between the neutral point balanced modulation strategy and the optimal efficiency GDPWM strategy is required. The neutral point potential offset is used as the determination condition for switching, and the hysteresis comparison method is used for switching. As shown in Figure 8, when $|U_{d1} - U_{d2}|$ is larger than $\Delta U_{dmax}$, it switches to the neutral point balance modulation method, and when $|U_{d1} - U_{d2}|$ is smaller than $\Delta U_{dmin}$, it switches to the optimal efficiency GDPWM strategy.

5.2. Vector action time and switch transmission sequence

The action time of the three switch vectors can be calculated from the principle of amplitude-second balance. The transmission of the switch adopts a five-segment type. Due to the continuous switching of the switch vector, the vector transmission sequence of the modulation strategy is performed by dynamic adjustment. After the switch vector is determined, the three switch states in the current switch cycle and the last state of the last switch cycle are compared together to determine the switch transmission sequence with the least change in the switch.

5.3. General Flow of GDPWM Modulation Strategy Considering neutral point Potential Balance

General Flow of GDPWM Modulation Strategy Considering neutral point Potential Balance is as follows. Firstly, according to the method described in Section 4.1, the DC neutral potential is used to determine whether to switch the modulation strategy, and then determine the modulation strategy. Secondly, the vector space region is determined according to the reference voltage. If the modulation strategy used is an optimal efficiency GDPWM modulation strategy, the switching vector is determined according to the method of Section 3.1; If the modulation strategy used is neutral point potential balance DPWM, the switch vector is determined according to the method of Section 2.3. Finally, after determining the switching vector, the vector action time and vector transmission sequence are calculated as shown in Section 4.2. This completes a modulation process.

6. Simulation and experimental analysis

6.1. Simulation analysis

In order to verify the effectiveness of the proposed modulation strategy, a three-level converter model using APF control mode was built using PSCAD. The model simulation parameters are shown in Table 2. R1 and R2 are used to simulate the leakage currents of the analog capacitor. The reason for setting the imbalance of the two resistors is to increase the imbalance of the neutral point potential, and then verify the effectiveness of the modulation strategy.

| parameters                  | value | parameters                  | value |
|-----------------------------|-------|-----------------------------|-------|
| power voltage, Un/V         | 380   | Capacitor C1 shunt resistorR1/Ω | 150   |
| DC side voltage, Udc/V      | 700/1400 | Capacitor C2 shunt resistorR2/Ω | 50/150 |
| Grid side filter inductor, L/μH | 325   | DC side support capacitor, C1,C2/mF | 15    |

Set the DC side voltage to 1400V, that is, MI<0.57. At this time, the reference voltage vector is completely in the internal subspace, and is always clamped to the phase where the absolute value of the current is the largest. The simulation waveform under the condition of no neutral point potential balance control strategy is shown in Figure 9. Figure 9(a) shows the mean value of the fundamental period of
the neutral point voltage offset. The neutral point voltage offset gradually increases to a maximum of 108.3V. Figure 9(b) shows the waveform of phase A current and voltage during [1.9s, 2s]. During the period of [1.9s, 2s], the THD was 8.25%, and the second harmonic content was 7.52%, which accounted for the highest proportion.

The simulation waveform of adding the neutral point potential balance control strategy switching under low MI is shown in Figure 10. The hysteresis parameter $\Delta U_{dcm\max}$ is set to 10V and $\Delta U_{dcm\min}$ is set to 0.1. Figure 10(a) shows the mean value of the fundamental period of the neutral point voltage offset. The neutral point potential fluctuates within 10V, indicating that the neutral point balance control strategy plays a role. Since the simulation amplifies the neutral point offset factor, the modulation strategy is frequently switched, and the neutral point potential fluctuates greatly. During the period of [1.9s, 2s], the THD was 3.12%, and the second harmonic content was 0.5%. It can be seen that the second harmonic due to the excessive shift of the neutral point potential is eliminated. The above two simulation results verify the effectiveness of the neutral point potential balance control strategy.

The simulated waveform with a DC voltage of 700V and an R2 of 150Ω is shown in Figure 11. The upper and lower diagrams of Figure 11 are the three-phase current waveform and the output voltage waveform of the a-phase converter. At this time, MI>0.57, a part of the reference voltage vector will fall in the outer sector with only two clamping modes, so a part of the clamp region falls on the phase where the absolute value of the current is the second largest. It can be seen that the clamp mode in the figure is consistent with the theoretical analysis.

![Simulation waveforms of low MI without neutral-balancing method](image1)
![Simulation waveforms of low MI with neutral-balancing method](image2)
![Simulation waveforms of high MI](image3)

The simulation waveform diagram of the case where the DC voltage is 1400V, the resistors R1 and R2 are adjusted to the same 150Ω, and the converter emitting 5th harmonic current is shown in Figure 13. The upper and lower diagrams of Figure 12 show the three-phase current value and the output voltage of the a-phase converter, respectively. It can be seen that the a-phase voltage clamp is at the 0 level when the absolute value of the A-phase current is the maximum of the three phases. In a fundamental period, since the emitted current is a 5th harmonic current, the clamp interval is divided into 10 segments.

The above simulation results verify the effectiveness of the proposed modulation strategy in reducing switching losses and neutral point potential balance. The simulation results are consistent with the theoretical analysis.
In order to further verify the correctness of the theoretical analysis and simulation results, the experimental analysis was carried out on the 100A capacity NPC three-level APF prototype experimental platform. The prototype uses Altera's Cyclone IV E: EP4CE115F23C8 FPGA as the control system. The experimental platform is shown in Figure 13, and the experimental system parameters are shown in Table 2. There is no capacitor parallel resistance, the switching frequency is 10k, the DC side voltage is 800V, and the neutral point voltage offset is limited to 20V.

The experimental waveform of the fundamental reactive current generated by the prototype using the GDPWM control strategy proposed in this paper is shown in Figure 14. Since \( MI > 0.57 \), most of the clamped area of \( U_a \) is the area with the largest absolute value of \( I_a \), and a part of the clamped area is the area with the second largest absolute value of \( I_a \). The above results are consistent with the simulation results.

The experimental waveform of the fifth harmonic current generated by the prototype using the GDPWM control strategy proposed in this paper is shown in Figure 15. The current in the figure is synthesized by the fifth harmonic and the compensated active fundamental current. From the waveform of \( U_a \), it can be seen that the clamp mode is related to the absolute value of the current. Since \( MI > 0.57 \), most of the clamped area of \( U_a \) is the area with the largest absolute value of \( I_a \), and the part of the clamped area is the area with the second largest absolute value of \( I_a \). The above results are consistent with the simulation results.

7. Conclusion
In this paper, a GDPWM strategy considering the neutral point potential balance is proposed to reduce the switching loss of the three-level converter under various operating conditions. The modulation strategy selects the optimal level clamp method by comparing the magnitude of the current flowing...
through the converter while ensuring the balance of the neutral point potential. In turn, the converter achieves minimal switching losses under various operating conditions. This control strategy is particularly effective in reducing the switching losses in the case where the current flowing through the converter changes greatly or is difficult to predict. Simulation and experimental results verify the correctness of the theoretical analysis and the effectiveness of the modulation strategy.

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References
[1] Oleg Vodyakho, Chris C. Mi. Three-Level Inverter-Based Shunt Active Power Filter in Three-Phase Three-Wire and Four-Wire Systems[J]. IEEE Transactions on Power Electronics, 2009, 24(5): 1350–1363.
[2] H. R. Teymour, D. Sutano, K. M. Muttaqi, et al. Solar PV and Battery Storage Integration Using a New Configuration of a Three-level NPC Inverter with Advanced Control Strategy[J]. IEEE Transactions on Energy Conversion, 2014, 29(2): 354–365
[3] Lucian Asiminoaei, Pedro Rodriguez, Frede Blaabjerg. Application of Discontinuous PWM Modulation in Active Power Filters[J]. IEEE Transactions on Power Electronics, 2008, 23(4): 1692-1706.
[4] Wang Hongyan, Deng Yan, Zhao Rongxiang, et al. Switching Loss Minimizing PWM Method for Flying Capacitor Multilevel Inverter[J]. Proceedings of the CSEE, 2004, 24(8): 51-55.
[5] Zhe Zhang, Ole C. Thomsen, Michael A. E. Andersen. Discontinuous PWM Modulation Strategy With Circuit-Level Decoupling Concept of Three-Level Neutral-Point-Clamped (NPC) Inverter[J]. IEEE Transactions on industrial electronics, 2013, 60(5): 1897~1906.
[6] AN Shaoliang, SUN Xiangdong, CHEN Yingjuan, et al. A New Generalized Implementation Method of Discontinuous PWM[J]. Proceedings of the CSEE, 2012, 32(24): 59–66.
[7] REN Kangle, ZHANG Xing, WANG Fusheng, et al. Optimized Design of Discontinuous Pulse-width Modulation and Output Filter for Medium-voltage Three-level Grid-connected Inverter[J]. Proceedings of the CSEE, 2015, 35(17): 4494~4504.
[8] J. D. Barros, J. F. A. Silva, E. G. A. Jesus. Fast-predictive Optimal Control of NPC Multilevel Converters[J]. IEEE Transactions on industrial electronics, 2013, 60(2): 619–627.
[9] June-Seok Lee, Swungjong Yoo, Kyo-Beum Lee. Novel Discontinuous PWM Method of a Three-Level Inverter for Neutral-Point Voltage Ripple Reduction[J]. IEEE Transactions on industrial electronics, 2016, 63(6): 3344–3354.
[10] SUN Qingsong, WU Xuezhi, TANG Fen. Three-level Inverter Discontinuous Pulse-width Modulation Strategy Considering Neutral Point Potential Balance[J]. Proceedings of the CSEE, 2017, 37(0): 1–9.
[11] CHEN Jun, HE Yingjie, WANG Xinyu, et al. Research of the Unity Theory Between Three-level Space Vector and Carrier-based PWM Modulation Strategy[J]. Proceedings of the CSEE, 2013, 33(9): 71-78.