On the applicability of two-bit carbon nanotube through-silicon via for power distribution networks in 3-D integrated circuits

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Abstract
This study investigates the possibility of the carbon nanotube (CNT)-based through-silicon vias (TSVs) for improving power integrity of 3-D integrated circuits (3-D ICs). The circuit model is developed for 2-bit CNT TSV and validated through the full-wave electromagnetic simulator HFSS simulations. The 2-bit CNT TSV is applied to power distribution networks (PDNs) by combining the validated equivalent-circuit model and that TSV-based PDN impedance is compared with the traditional one. By virtue of the large capacitance and low inductance of the 2-bit CNT TSV, the PDN impedance of the 3-D IC can be suppressed significantly and the anti-resonant frequency can be increased.

1 | INTRODUCTION

3-D integrated circuits (3-D ICs), as a promising solution to keep pace with the scaling of Moore's law, have aroused interests from researchers worldwide [1,2]. Compared with conventional 2-D ICs, 3-D ICs can provide enormous advantages in high density, multifunction and heterogeneous integration by stacking chips vertically. To promote the development of 3-D ICs, through-silicon via (TSV), as the key technology connecting chips directly through the substrate, has been investigated extensively in the past decade [3–5].

Although TSVs can significantly reduce the interconnect length and improve the system bandwidth, they would induce high upper impedance peaks, which may be the simultaneous switching noise generators integrated circuit power distribution network (PDN) [6,7]. To suppress the TSV inductance effect, the power/ground (P/G) vias should be placed as close as possible [8]. However, to guarantee the yield, the holes should be etched uniformly. To date, different TSV array arrangements and decoupling capacitor techniques have been explored to resolve the power integrity issues [9–14]. Furthermore, to reduce the burden of on-die decoupling capacitors, an n" contact surrounding the power TSV was proposed to enhance its parasitic capacitance at high frequencies [15].

Recently, carbon nanotube (CNT) was proposed to be an alternative filling material of TSV to improve the TSV reliability [16–19]. Moreover, the implementation of CNT TSVs is beneficial for heat dissipation of 3-D ICs due to their high thermal conductivity. In this study, the concept of 2-bit CNT TSVs is utilized for 3-D IC PDN applications. Section 2 details the geometries and circuit models of the CNT TSVs and on-chip grids. In Section 3, simulation results for 3-D IC PDN based on 2-bit CNT TSVs are discussed. Some conclusions are finally drawn in Section 4.

2 | ELECTRICAL MODEL

The concept of 2-bit CNT TSVs (see Figure 1a), which were realized by placing two discrete metal pads on the surfaces of the CNT TSVs, were firstly proposed by Vaisband [2]. Thanks to the electrical anisotropy of the CNTs, that is, the lateral conductivity of the CNT is usually seven orders lower than the radial conductivity, the signal is generally transmitted vertically rather than laterally. It is worth noting that the CNT kinetic inductance, which denotes the kinetic energy of electrons in the nanotube, is much larger than the magnetic inductance, and therefore cannot be simply neglected in high-frequency
analysis [19]. However, the influence of the CNT kinetic inductance is neglected in previous study of 2-bit CNT TSVs [2]. To resolve this issue, the modified equivalent-circuit model of 2-bit CNT TSV is proposed, as shown in Figure 1b, with the consideration of the CNT kinetic inductance. The related geometrical parameters are listed in Table 1.

The mutual conductance can be further suppressed by introducing semiconducting CNTs in the middle [20]. Two parts of CNT forests are metallic, and serve as power and ground vias. The circuit model of the 2-bit CNT TSV is presented in Figure 1b, where the mutual capacitance between P/G vias is given by

\[ C_m = 2\pi r_{TSV} h_{TSV} / w_s \]

where \( \varepsilon \) denotes the effective permittivity of medium between P/G vias. \( R \) and \( L \) represent the effective resistance and inductance of the 2-bit CNT TSV, and can be obtained using the partial-element equivalent-circuit method [21]. As shown in Figure 2, the circuit model is verified against the HFSS simulation results with a good agreement observed. In the simulation, the TSV filling conductor and the middle medium are assumed as Cu and SiO\(_2\) as CNTs are unable to simulate in HFSS.

Figure 3a shows the schematic of on-chip grids, and its size is \( 1.03 \times 1.03 \times 0.02 \) mm\(^3\). The on-chip grids are embedded in a \( 1.09 \times 1.09 \times 0.06 \) mm\(^3\) inter-dielectric layer. The power and ground wires are arranged alternatively to reduce the PDN impedance, with other geometrical parameters presented in Table 2. According to the location, the on-chip grids can be decomposed into three types of unit structures, that is, corner, edge and inner units, as shown in Figure 3b. The unit structures can be characterized as the circuit model in Figure 3c by substituting the geometrical parameters into the extraction of circuit elements. The series resistance of the wire can be calculated as

\[ R_s = \frac{l}{\sigma W H} + \frac{(1 + j)l}{2(W + H)} \sqrt{\frac{\pi \mu_0 f}{\sigma}} \]

where \( W, H \) and \( l \) denote the width, thickness and length of the wire, respectively, \( \sigma \) is the conductivity, \( \mu_0 \) is the permeability in vacuum and \( f \) is the frequency. As the power and ground wires are arranged alternatively, the series inductance is given as

![Figure 1](image1.png)  
**Figure 1** (a) Geometry and (b) circuit model of the 2-bit carbon nanotube (CNT) through-silicon via (TSV)

| Parameter | Definition | Value |
|-----------|------------|-------|
| \( r_{TSV} \) | TSV radius | 15 |
| \( h_{TSV} \) | TSV height | 300 |
| \( t_{ox} \) | Oxide thickness | 4 |
| \( w_s \) | Distance between two pads | 0.2 |

Abbreviation: TSV, through-silicon via.

![Figure 2](image2.png)  
**Figure 2** (a) \( S_{11} \) and (b) \( S_{21} \) parameters of the 2-bit carbon nanotube through-silicon via. The geometry is as follows: \( r_{TSV} = 15 \) \( \mu \)m, \( h_{TSV} = 300 \) \( \mu \)m, \( t_{ox} = 4 \) \( \mu \)m and \( w_s = 0.2 \) \( \mu \)m

![Figure 3](image3.png)  
**Figure 3** (a) Geometry and (b) circuit model of the 2-bit carbon nanotube through-silicon via. The geometry is as follows: \( r_{TSV} = 15 \) \( \mu \)m, \( h_{TSV} = 300 \) \( \mu \)m, \( t_{ox} = 4 \) \( \mu \)m and \( w_s = 0.2 \) \( \mu \)m

![Figure 4](image4.png)  
**Figure 4** Geometry and (b) circuit model of the 2-bit carbon nanotube through-silicon via. The geometry is as follows: \( r_{TSV} = 15 \) \( \mu \)m, \( h_{TSV} = 300 \) \( \mu \)m, \( t_{ox} = 4 \) \( \mu \)m and \( w_s = 0.2 \) \( \mu \)m
\[ L = L_s - 2L_m \]  

where the self- and mutual inductances are calculated by

\[ L_s = \frac{\mu_0 l}{2\pi} \left[ \ln \left( \frac{2l}{W+H} \right) + 0.4983 \right] \]  

\[ L_m = \frac{\mu_0 l}{2\pi} \left[ \ln \left( \frac{l}{P} + \sqrt{1 + \left( \frac{l}{P} \right)^2} \right) - \sqrt{1 + \left( \frac{P}{l} \right)^2 + \frac{P}{l}} \right] \]  

The capacitance \( C_{OA} \) can be obtained by Cheng et al. [13].

\[ C_{OA} = 2WC_M + C_{wtr} - \frac{\varepsilon_{\infty} W^2}{H_1} \]  

where the capacitance between the upper power (ground) wire and bottom ground (power) wire and the wall-to-wall capacitance are calculated by

\[ C_M = \varepsilon_{\infty} \left[ \frac{1.15W}{H_1} + 2.8 \left( \frac{H}{H_1} \right)^{0.222} \right] \]  

\[ C_{wtr} = 20\varepsilon_{\infty} \left( 1.1 + 1.6e^{-\frac{W}{H_1}} \right) H_1 \left( \frac{l-W}{l-W+2H_1} \right)^{2.4} \]

By virtue of the circuit model of the unit structures, the complete model of the on-chip grids can be obtained. According to the ports in Figure 3a, the magnitudes of Z-parameters are obtained and depicted in Figure 4. It is evident that the circuit model results agree well with the HFSS simulation results. In general, the parasitic effects
between on-chip grids and TSVs are negligible, and the impedance of the whole 3-D IC PDN can be obtained by combining the models of on-chip grids and TSVs [13]. In this way, the PDN impedance of the whole structure shown in Figure 5a can be obtained and compared with the simulated results (see Figure 5a,b).

3 | RESULTS AND DISCUSSION

Based on the circuit models, the 3-D IC PDN based on 2-bit CNT TSVs can be investigated. Here, it is assumed that the CNTs are single-walled CNTs with identical diameter, and they are closely packed in the via. The semiconducting single-walled CNTs are in the middle to prevent lateral conduction, while the metallic CNTs are connected with the pads to provide conduction path. The effective complex conductivity of the CNT bundle is employed by Zhao et al. [17].

\[ \sigma_{CNT} = \frac{2h_{TSV}}{\sqrt{3}(D + \delta)^2} \cdot \frac{1}{Z_{CNT}} \]  

(Figure 4 (a) Z_{11} and (b) Z_{21} parameters of the on-chip grids. The geometry is as follows: W = 30 μm, H = 5 μm, P = 100 μm, W_1 = 30 μm and H_1 = 10 μm.

(Figure 5 (a) Schematic of 3-D integrated circuit power distribution network based on 2-bit carbon nanotube (CNT) through-silicon via (TSV), and its (b) Z_{11} and (c) Z_{21} parameters. The geometrical parameters are same with those used for producing Figures 2 and 4.

\[ \sigma_{CNT} = \frac{2h_{TSV}}{\sqrt{3}(D + \delta)^2} \cdot \frac{1}{Z_{CNT}} \]
\[ Z_{\text{CNT}} = \frac{R_{\text{mc}}}{N_{cb}} + \frac{b}{2q^2N_{cb}} \left( 1 + \frac{b_{TSV}}{\lambda} + \frac{j\omega b_{TSV}}{2\nu_F} \right) \]  

where \( D \) is the CNT diameter, \( \delta = 0.34 \text{ nm} \) is the distance between adjacent CNTs, and \( Z_{\text{CNT}} \) is the self-impedance of an isolated single-walled CNT, that is,

where \( R_{\text{mc}} \) denotes the imperfect contact resistance and is neglected as it highly depends on the fabrication process. 

\( N_{cb} = 2 \) is the number of conducting channels, and \( \lambda = 1000D \) is the effective mean free path. \( b \) is the Planck's constant, \( q \) is the electron charge, \( \nu_F \) is the Fermi velocity and \( \omega \) is the angular frequency. The relative permittivity of the CNT forest is adopted as 36 according to Liu et al. [22].
As the 2-bit CNT TSV can assemble the power and ground vias in one hole, it has much smaller inductance than conventional TSV pair. Moreover, its large mutual capacitance between the P/G vias can provide timely and effective power to nearly transistors, thereby producing a low impedance path to high-frequency signals. To validate the related, a set of two-stacked chip-PDNs connected by a pair of P/G Cu-filled TSVs is studied, as shown in Figure 6a. For easy of comparison, the hole size is kept unchanged, while the CNT forests are inserted into two holes to form a pair of 2-bit CNT TSVs. Figure 6b,c compares the PDN impedances in two cases, and it is evident that the implementation of 2-bit CNT TSVs can not only significantly suppress the impedance, but also put forward the anti-resonant frequency. It is worth noting that large capacitance and small inductance possessed by such 2-bit TSV are oriented from its unique structure. The benefits of suppressing the PDN impedance can also be achieved by using Cu as the filling conductor. However, it would be difficult to implement such 2-bit TSV using Cu as it is not an anisotropic material, while further effort is required in future to investigate fabrication process of such 2-bit SWCNT-based TSVs.

Finally, the influence of the 2-bit CNT TSV density on the PDN impedance is investigated. As shown in Figure 7a–c, three cases of TSV arrays are considered, and it is evident that with the increasing number of TSVs, the capacitance would be increased significantly, whereas the resistance and inductance are reduced [6]. As shown in Figure 7d, both the PDN impedance and the upper peak are reduced dramatically with the increasing TSV density.

4 | CONCLUSION

Although TSVs can enable 3-D heterogeneous integration, the TSV inductance effect would produce high upper peaks of PDN impedance. To improve the power integrity, the 2-bit CNT TSVs were employed in the 3-D IC PDN applications. The large capacitance of the 2-bit CNT TSV can provide timely and effective current and power to devices nearly, thereby reducing the burden of on-die decoupling capacitors.
Moreover, the mutual inductance between power and ground vias in a 2-bit CNT TSV can effectively reduce the total inductance. It was demonstrated that 2-bit CNT TSVs can not only suppress the PDN impedance, but also increase the anti-resonant frequency, indicating that the implementation of the 2-bit CNT TSVs would be helpful for improving the power integrity of the 3-D ICs.

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