Development of readout chain for CBM Projectile Spectator Detector at FAIR

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Abstract. The Compressed Baryonic Matter (CBM) experiment at FAIR needs a detector to measure the nucleus-nucleus collision centrality and orientation of the reaction plane. The Projectile Spectator Detector (PSD) as a sampling lead/scintillator forward hadron calorimeter with transverse and longitudinal segmentation will be used for this purpose. The PSD consist of 44 modules with 10 longitudinal sections in each. Electronics of PSD consist of MPPCs boards mounted directly on detector and readout ADC interface with ADC FPGA board installed into crate distanced on 50m from detector part. ADC has 14-bit resolution and 125MHz digitization rate, Kintex-7 FPGA is placed on the board. Concept of PSD Front End Electronics (FEE) is already designed and most crucial parts including ADC FPGA board already tested and confirmed to be operational. One PSD module ("mini PSD" or mPSD) has been installed into the "mini CBM" (mCBM) assembled at SIS18 accelerator in GSI, Darmstadt, Germany in the framework of the FAIR Phase-0 program. ADC FPGA readout board has been integrated into common DAQ experiment and tested. Details of the mPSD FEE design and test results are shown.

1. Introduction
The aim of the future Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) is to explore the Quantum Chromodynamics (QCD) phase diagram in the region of high baryon densities [1]. The beam energy range of 2 - 11 AGeV and heavy ion interaction rates up to 10 MHz will be achieved at the CBM experiment.

The PSD (Projectile Spectator Detector) is the forward hadron compensating lead/scintillator calorimeter, which will be used in the CBM experiment to measure the collision centrality and the reaction plane orientation in heavy-ion collisions [2]. The PSD has transverse and longitudinal segmentation. The light readout performed via micropixel photodetectors is used at the PSD, one Hamamatsu MPPC S12572-010P (Multi-Pixel Photon Counter) with active area 3x3mm² is used as photodetector for each section of the module [3][4].

2. PSD readout concept
The PSD electronics architecture consists of two major parts: a set of radiation-hard front-end boards and a readout rack, as shown in figure 1. Front-end boards are mounted directly onto The PSD modules, and are exposed to the particle flux generated by the experiment. Readout rack is located in a radiation-safe environment and is connected to the front-end part via 40m long signal cables.
2.1. The FEE boards
The FEE boards are mounted directly onto PSD modules and host MPPCs, a temperature sensor (PTC thermistor), optical calibration LED, cable connectors and optical crosstalk protection hardware. These boards provide direct load of the MPPCs into 50 Ohm coaxial cables. FEE boards are fully designed (see figure 2) and are in production.

2.2. Service board
Service board is a multi-functional unit, designed to serve the PSD needs, that are not related to the signal chain. Service board hosts a high voltage supply for biasing the MPPCs, as well as monitoring of the MPPCs current with automatic protection against overcurrent, temperature sensor interface through resistance-to-digital converters, optical calibration LED pulse generator and drivers. Operation of the board may be controlled directly through manual switches or remotely via a slow control interface. Control commands and configuration from DCS translated with single GBT link to ADC board and rerouted to MCU mounted on service board via I2C interface. An evaluation version of the Service board has been developed (see figure 3), manufactured and is undergoing verification and firmware development. Evaluation board may be easily scaled into a full-scale version.
2.3. Readout module

Readout module is an assembly of the ADC interface board and the ADC board itself (presented in figure 4). The ADC board was initially designed for the ECAL detector of PANDA experiment [5]. The 64-channel board is based on two Kintex 7 FPGA (field-programmable gate array) and LTM9011 ADC (analog-to-digital converter) with digitization rate up to 125Msps and 14-bit digitization resolution. To meet the requirements of CBM DAQ, GBT FPGA[6] transceiver was integrated into the firmware.

The ADC interface board and the ADC board are connected directly and are mounted together into the readout rack. ADC interface board hosts single-ended to differential converters with adjustable input and output zero level, as well as high voltage correction circuit through common mode compensation: board may apply a DAC-controlled DC voltage onto a signal line, adjusting the common 80V MPPC supply for each of the channels individually, leaving the AC signal unaffected. Both of the boards are designed and are in production. An evaluation version of the Readout module has been tested during beam tests runs at mCBM@SIS18 at the end of 2019 and beginning of 2020 [4].

3. The first mPSD beam test at mCBM

At the end of 2019 and beginning of 2020, beam tests at mCBM@SIS18 were carried out with Au and Pb ions at 1.01 - 1.22 AGeV energy range. The main goal was to test detectors subsystems, DAQ and online data aggregation procedure. Test of the mPSD as a part of mCBM experiment
allows to approve and verify the feasibility of the PSD readout concept. The prototype of the PSD readout includes such crucial parts as addon prototype board and ADC FPGA readout board. MPPC S12572-010P with active area 3x3mm\(^2\) photodetectors used as light sensors for readout.

One of the most important features of the ADC board is the ability to process signals on-the-fly in the FPGA. Waveform fitting will improve the time and amplitude resolution and will allow to perform pile-up selection. The figure 5 shows the waveform for one MIP amplitude measured with 80 MHz digitization rate. The black dots correspond to the waveform measured by the ADC, and the red line is based on a two-exponential fit of the waveform using the Prony LS method \[7\]. To recognize pile-ups at expected high load rate up to 1MHz at CBM experiment, digitization rate of ADC will be increased to 120MHz with firmware upgrade.

Components related to the signal chain, as well as firmware and software parts have been tested and confirmed to be operational during beam test runs at mCBM@SIS18 at the end of 2019 and beginning of 2020\[4\].

![Figure 5. mPSD waveform example. Black dots - waveform points, measured by sampling ADC, red line - graph based on two-exponential fitting function by Prony LS method.](image)

4. Conclusions

Concept of the PSD FEE has been designed including on-detector photo-sensors board, cable system, ADC readout board and service board. Most crucial parts including ADC FPGA board with prototype of interface board was already tested at mCBM experiment in March 2020 and confirmed to be operational. Most of the components required to assemble a full-size PSD electronics architecture are either engineered or in undergoing manufacturing. Prototype of readout chain of the PSD will be tested at the mCBM.

References

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