1. Introduction

The performance of a digital system owes its competence to the selection of highly reliable components and the use of proven methods for their interconnection. The system requires an extensive verification of the logic design, code and final hardware using simulation, diagnostic and functional tests in the expected environmental conditions.

In spite of these reliability assurance techniques, the system may still fail during normal operation due to uncontrollable or undetectable faults that are caused by undetected design errors, random failures of components or interconnections and externally induced malfunctions during the operation of the system.

The emergence of nanometre VLSI technology drastically increases the circuit density and clock speed but at the same time significantly decreases the supply voltage and the amount of charges. As a consequence of this most crucial and conflict transformation in process technology, the modern VLSI circuits exhibit substantially high Soft Error Rates [SERs] [1, 2].

The permanent and temporary faults turn out to be the main sources of operational errors in digital systems. The permanent faults represent irreversible changes in the logic values of the components of a digital system in consequence of long time in service. The temporary faults classify themselves as transient and intermittent faults. The transient nature of faults erupts due to external environmental conditions like cosmic rays and electromagnetic interference whereas intermittent faults arise on account of unreliable internal operating conditions.

The stuck-at-faults that tend to appear frequently in digital systems cause the impaired signal lines to be stuck at either logic 0 or 1, regardless of the inputs. They categorize themselves as either intermittent or permanent faults due to the fact that they appear on account of tightly constrained internal operating conditions or wear and tear of the components after a long period in service.

The elaborate role of digital circuits in critical applications further emphasizes to incorporate healing facility to attach a sense of reliability in their performance. Thus, the ability to manage inconsistent resources and service desperate user requirements has been an imperative necessity.

The philosophy of fault tolerance defines itself as the ability of the system to provide fault free services in the presence of faults [3]. A key factor in the design

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BLACK BOX MODEL-BASED SELF HEALING SOLUTION FOR STUCK-AT-FAULTS IN COMBINATIONAL CIRCUITS

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The paper unveils a black box model-based self healing strategy to suppress the ill effects of stuck-at-faults occurring in combinational circuits. The primary theory endeavours to attach a sense of reliability in the performance of digital systems and makes them insensitive to the negative impact of faults present in the system. The proposed methodology employs a dynamic fault tolerant approach to protect digital systems from the incursion of stuck-at-faults and enables the system to come up with fault free outputs. The simulation results affirm the authenticity of the proposed strategy to cancel out the influence of faults and facilitate the system to heal itself. The work utilizes the attributes of an FPGA to demonstrate the practical viability of the proposed approach. The performance analysis endorses the definite dominance of the proposed healing scheme over the traditional Triple Modular Redundancy [TMR] in terms of fault coverage and area overhead.

Keywords: black box model, FPGA, reliability, self healing, stuck-at-faults, VHDL

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of fault tolerant digital systems owes its ability to address issues of dependability requirements [4].

The concept of redundancy serves to improve the reliability of dependable systems and remains the integral aspect of fault tolerance [5, 6]. It helps the system to achieve fault recovery in the sense they enable the system to conceal the presence of faults, suppress their effects and continue to provide immaculate services.

The fault injection procedure endeavours to inculcate the system under test with a sense of responsibility to forecast the faults and provide way for fault tolerance. It enlivens the role of testing strategies through the natural introduction of faults at the preferred locations in order to evaluate the dependability requirements of the system [7, 8].

The rest of the paper organizes itself under five main sections that include the literature review, design methodology, simulation results, hardware implementation and finally conclusion.

2. Literature review

Based on VHDL descriptions, the implementation of separable codes for Concurrent Error Detection (CED) within VLSI circuits has been described in [9]. Four different schemes for CED have been analyzed and implemented in FPGA and Complex Programmable Logic Device (CPLD) technologies and results concerning area overhead and operating speed reported.

A suitable approach for generating two level combinational circuits with concurrent error detection capability based on three different techniques has been proposed in [10]. The amount of area overhead and the variation in operating speed related to the three schemes have been reported for seven combinational circuits of standard architecture.

The differences among permanent, transient and intermittent faults have been discussed with the emphasis on malfunction causes, from manufacturing residues to ultra-thin oxide breakdown, together with timing violations presented in [11, 12]. The error signatures, specific to intermittent faults have been provided through failure analysis results.

A detailed survey on fault injection techniques has been carried out in [13] with a purpose to bring out the relative merits and demerits of the various methodologies developed to inject faults into a system prototype or model.

A VHDL based fault injection tool has been described in [14] and its effectiveness verified through various fault injection experiments carried out using different parameters. During the fault injection campaign, a wide range of transient and permanent faults have been injected through the tool for the signals and variables of the chosen model using simulator commands.

A detailed analysis of the impact of intermittent faults has been carried out utilizing the merits of the simulated fault injection technique in [15]. The intermittent faults have been injected into the VHDL model of a microcontroller using some faults observed in real computer systems.

An efficient approach for testing, detecting and tolerating single stuck-at-faults at interconnect levels of digital circuits has been proposed in [16]. The possible interconnect faults for wiring channels have been considered and signal routing in the presence of faulty interconnect resources analyzed at both circuit level and design level.

A generalized modular redundancy scheme has been presented in [17] to consider the probability of occurrence of each combination at the output of a circuit. The redundancy has been then added to only protect those combinations that have high probability of occurrence while the remaining combinations left unprotected to save area.

Different TMR-based majority voter designs have been analyzed and realized using a cutting edge 32/28 nm CMOS technology in [18]. Further, a new voter design has been presented with improved fault tolerant ability against both single and multiple stuck-at-faults that occur either internally or externally to the voter circuit. A number of standard-cell-based majority voter designs relevant to TMR architectures have been presented and their power, delay and area parameters estimated based on physical realization using a 32/28 nm CMOS process in [19].

A new hybrid fault-tolerant architecture has been laid to improve robustness of digital CMOS circuits and systems in [20]. The architecture has been embodied with information redundancy for error detection, timing redundancy for transient error correction and hardware redundancy for permanent error correction.

An in-depth review of the literature related to self-healing along with a detailed survey and synthesis has been presented using the developed taxonomy in [21]. A self-healing architecture based on human immune system suitable for VLSI based digital systems has been proposed in [22]. The error in the digital circuit has been treated as an antigen by the system and a distributed defence mechanism evolved to heal itself from the effect of the error.

A new tool for the automatic insertion of fault tolerant structures in synthesizable VHDL descriptions has been proposed in [23] and the techniques to automatically apply hardware redundancy and information redundancy to a VHDL design shown.

3. Design methodology

The central theme of the scheme assures to negate the effect of stuck-at-faults present at the interconnect lev-
Black Box Model-Based Self Healing Solution for Stuck-At-Faults in Combinational Circuits

els of combinational circuits and bring out the expected behaviour. The work acquires the services of simulated fault injection technique to verify the authenticity of the strategy through the intentional introduction of faults into the VHDL model of the Circuit Under Test [CUT] during the course of simulation. The choice of a decoder as the CUT owes to its influential presence in almost all digital circuits and the fact that the philosophy can easily relate to other circuits. The algorithm provided enumerates the steps involved in the process of building the self-healing design being able to come up with fault free output in the presence of manually injected stuck at faults.

Algorithm:

1. Determine the primary inputs and primary outputs of the CUT
2. Develop the CUT with built-in healing facility
3. Simulate and verify the functional correctness of the design
4. Inject stuck-at-faults manually on the randomly selected interconnects
5. Simulate and substantiate the self-healing ability of the design

The expressions given below establish the relationship between the inputs and the desired outputs of the 2:4 decoder in the fault free state.

\[
\begin{align*}
D_{\text{out}}(0) &= (D_{\text{in}}(0) \text{ and } D_{\text{in}}(0)), \\
D_{\text{out}}(1) &= (\overline{D_{\text{in}}(0)} \text{ and } D_{\text{in}}(0)), \\
D_{\text{out}}(2) &= (D_{\text{in}}(0) \text{ and } \overline{D_{\text{in}}(0)}), \\
D_{\text{out}}(3) &= (\overline{D_{\text{in}}(0)} \text{ and } \overline{D_{\text{in}}(0)})
\end{align*}
\]

When the CUT operates in fault free state, it produces the output as expected for a given input combination in accordance with its input – output relationship. On the other hand, the appearance of stuck-at-faults at the intermediate lines causes the circuit to generate faulty output.

Figure 1 depicts one such turbulent state of the CUT in which the interconnect level \(D_{\text{in}}(0)\) stuck at one and the Table 1 displays the faulty operating condition of the circuit in consequence of the presence of stuck-at-fault occurred at one of the interconnect levels.

The work seeks to engage the extant Triple Modular Redundancy [TMR] technique alongside the pro-

![Diagram of a 2:4 decoder with stuck at 1 fault]

**Fig. 1.** The CUT in the presence of stuck at 1 fault

| \(D_{\text{in}}(1)\) | \(D_{\text{in}}(0)\) | \(D_{\text{in}}(1)\) | \(D_{\text{in}}(0)\) | \(D_{\text{out}}(0)\) | \(D_{\text{out}}(1)\) | \(D_{\text{out}}(2)\) | \(D_{\text{out}}(3)\) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1* | 0 | 0 | 1 | 1* |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1* | 1 | 0 | 0 | 0 |

1* – Stuck at 1

**Table 1.** Faulty operating condition of the CUT

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posed Black Box Model [BBM] scheme with a view to substantiate its ascendancy over the former in terms of fault coverage and area overhead needed to implement the design.

3.1. Triple modular redundancy-based healing approach

The expressions presented below represent the operational behaviour of the TMR-based self-healing approach which houses three identical copies of the CUT along with the constituent components of the voting system. Though the TMR design exhibits excellent resilience to single stuck-at-faults and possesses the ability to provide the correct values on the primary output lines, it gives in to multiple bit faults.

3.2. Black box model-based healing scheme

The scheme incorporates a built-in healing mechanism which eliminates the harmful impact of stuck-at-faults present at the interconnect levels of a digital system and produce true values on its primary output lines thereby making it a self-healing system by its very nature. The inherent heal facility attached to the formulation enables to reach out the fault free output of the system even in the presence of multiple faults.

The proposed scheme reaps the benefits of combining the traits of both hardware redundancy and information redundancy to build the controller for fault detection and correction. Thus, it possesses the capability to survive turbulent situations and continues to behave as it did prior to disruption. The methodology treats the CUT as a black box and constructs a dynamic redundancy-based healing procedure to tolerate multiple bit faults.

In general, testing forays to verify the behaviour of design under test and it may either be a black box test or a white box test or the combination of both called as grey box test. The black box test does not possess any prior knowledge over the internal structure and functions of the system but thoroughly knows that a particular input will bring out a certain invariable output. The procedure utilizes this fact to build the output prediction unit which picks the desired output based on the already established input-output relationship of the system regardless of the presence of faults at the interconnect levels of the system.

Though the BBM scheme appears to be similar to Dual Modular Redundancy [DMR] technique, it distances itself from the latter in the sense the DMR technique suits only for error detection but not for correction. Further, the probability for the occurrence of faults in the duplicate module of the DMR approach stands high whereas the output prediction unit of the BBM scheme does not provide faulty outputs since it cleanses itself through information redundancy. The redundant code inculcates the output prediction unit to pick the correct output for a given input combination and mandates it to perform the role of the soft core reference module of the CUT.

The functional block diagram of the proposed BBM based healing scheme shown in Fig. 2 strategically deploys the built-in control mechanism which includes a diagnostic unit comprising as many EX-OR gates as the number of primary outputs of the CUT and a healing unit consists of number of NOT gates equal to the number of primary outputs. The CUT and the

Fig. 2. Functional block diagram of the BBM based healing scheme
output prediction unit developed through information redundancy act as the source of actual and reference inputs, respectively, to the controller in fault detection pursuit.

The desired output picked by the predictor for the given input together with the corresponding eventual outcome from each of the output lines of the CUT form the inputs to each of the EX-OR gates. The diagnostic unit of the controller keeps track of the outputs generated at the interconnects of the system for a given input combination and senses the presence of faults by comparing the actual outcome at the interconnects and the desired output for the given input produced by the output prediction unit. It localizes the origin of the fault through the logic states of the EX-OR gates in the sense a logic high output indicates the presence of fault in the signal line. The healing unit thereafter assumes control and manipulates the logic state of one or more erroneous interconnect lines with the help of its constituent components in the form of NOT gates, thereby enabling the CUT to operate in fault tolerant state.

The built-in control mechanism attached to the system facilitates meticulous monitoring of the flow of signals and takes the corrective action on the fly in the presence of faults in its effort to keep the system truly fault tolerant. The power of the scheme to restore the normal operation of the system through dynamic fault detection and correction authenticates its self-healing concept.

![Fig. 3. Output of the TMR-based decoder without faults](image1)

![Fig. 4. Fault free output of the TMR-based decoder with single stuck-at-fault](image2)
4. Simulation results

The strategy avails the portals of Modelsim platform to illustrate the strength of the TMR-based approach through the VHDL description developed for the fault tolerant 2:4 decoder. The Modelsim-based simulation results presented in Fig. 3 exhibit the normal operating state of the TMR-based decoder in the absence of faults.

The results in Figs 4 and 5 explicate the ability of the TMR strategy to retain the decoder in its fault tolerant state. The insertion of stuck-at-faults as seen in Figs 4 and 5 exhort the fault injection campaign in the sense at the 500th ns the least significant bit of the first decoder “d1” is made to be stuck at logic 1 and at the 1000th ns the most significant bit of the third decoder “d3” to be stuck at logic 0, respectively.

On the contrary, the flow of signals seen in Fig. 6 exposes the weakness of the TMR approach in the sense it succumbs to the invasion of faults and carries the faulty signal to its primary output lines when the most significant bits of the two decoders “d1” and “d3” suffer from stuck at 0 fault concurrently at the 1500th ns.

The Modelsim based simulation results presented in Fig. 7 exhibit the normal operating state of the BBM based decoder in the absence of faults whereas results available in Figs 8 and 9 elucidate the ability...
of the BBM scheme to retain the decoder in its fault tolerant state.

The introduction of stuck-at-faults as seen in Figs 7 and 8 kicks off the fault injection campaign in the sense at the 500th ns the most significant bit of the interconnect signal int(3) is made to be stuck at logic 0 and at the 1000th ns the least significant bit of the interconnect signal int(0) to be stuck at logic 1, respectively.

Despite the introduction of faults, the circuit continues to generate the correct information on its primary output lines thanks to the innate ability of the

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**Fig. 7.** Output of the BBM-based decoder without faults

**Fig. 8.** Fault free output of the BBM-based decoder with single stuck-at-fault

**Fig. 9.** Fault free output of the BBM-based decoder with multiple stuck-at-faults
healing mechanism inherently associated with it. The simulation results clearly show that the proposed self-healing architecture exhibits excellent resilience and meets the design specifications even in turbulent situations.

5. Hardware implementation

The FPGA in light of its inherent run time reconfigurable ability and design independent stature proclaims its suitability for the implementation of fault tolerant designs. The target technology view of the BBM-based self-healing decoder shown in Fig. 10 obtained using Xilinx foundation series ISE 9.2i exhibits the interconnection among the resources of the target Xilinx XC3S500E FPGA employed to endorse the practical applicability of the scheme. The real time implementation using FPGA validates the simulated performance of the design attained on Modelsim platform. The picture in Fig. 11 portrays the experimental setup engaged to validate the truthfulness of the BBM-based self-healing scheme under various operating states.

5.1. Performance analysis

Table 2 ascertains the impeccable merits of the BBM-based self-healing strategy over the TMR-based approach in terms of fault coverage and the amount of resources utilized during real time implementation which in turn provides an idea over the area overhead.

The chart in Fig. 12 highlights the supremacy of the BBM-based self-healing architecture over the TMR approach as it renders total fault coverage against single as well as multiple bit errors and significantly lowers the area overhead needed to construct the healing mechanism.

The output of the TMR-based healing approach in any case does not guarantee to be reliable because if two or all the three of its inputs turn out to be faulty, the voter permits the faulty signal to proceed further in the system. On the contrary, the BBM scheme sur-

![Fig. 10. The target technology view of the BBM-based self-healing decoder](image-url)
vives single as well as multiple faults under any circumstances owing to its built-in self-healing property. The other important issue concerning the TMR approach relates to extremely high area overhead which rises as high as 466.67% since it requires two exact replicas of the CUT together with the voter circuit whereas the BBM scheme needs relatively very few redundant components for implementation which

| Scheme | Fault coverage (%) | Area overhead | No. of slices | No. of LUTs | No. of IOBs |
|--------|---------------------|---------------|---------------|-------------|-------------|
| BBM    | 100                 | 2             | 4             | 6           |
| TMR    | 33.33               | 9             | 16            | 22          |

![Fig. 11. Experimental validation of the BBM-based self-healing scheme](image)

![Fig. 12. Comparative chart](chart)
in turn reduces the area overhead to as low as 133.33%. The entries in Table 2 proclaim this fact with a significantly lower number of slices, LUTs and IOBs utilized by BBM-based scheme compared to TMR-based approach.

6. Conclusion

A BBM-based in-situ control strategy has been coined to negate the impact of stuck-at-faults occurring in digital circuits. The special traits of the procedure have been utilized to sense the possible occurrence of faults in combinational circuits and correct them to produce the desired output. The simulation results obtained for the VHDL model of the 2:4 decoder reiterates the self-healing ability of the scheme to produce true outputs in the presence of single as well as multiple stuck-at-faults and the real time implementation of the scheme employing XC3S500E FPGA on the Xilinx foundation series ISE 9.2i platform stands as the proof of the concept. The comparative analysis made with the traditional TMR-based healing approach brought the ultimate benefits of the scheme to the fore as it comprehensively outplays the TMR in terms of fault coverage and area overhead.

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