1. Introduction

Modern artificial intelligence (AI) systems using neural network (NN) structures have shown remarkable performance in various tasks from image recognition\textsuperscript{[1–3]} to human-beating gameplay.\textsuperscript{[4,5]} A crucial contributor to this recent success is efficient hardware for massively parallel computing systems,\textsuperscript{[6]} which comprises NN. As multiply-and-accumulate (MAC) operation comprises most NN operations, introducing MAC-specialized hardware, which uses data parallelism, greatly boosts the efficiency. For this reason, the graphical processing unit\textsuperscript{[7,8]} or tensor processing unit\textsuperscript{[9]} is mainly used for high-performance AI-directed hardware neural network (HNN) systems. However, all these systems still rely on the von Neumann architecture, which consumes considerable energy for data transfer between the memory module and processors.\textsuperscript{[10]}

In this regard, the crossbar array (CBA), which uses resistive switching random access memory (ReRAM), is a potential candidate for the next-generation HNN.\textsuperscript{[11–15]} It can accelerate the MAC operation by a single-step physical calculation using Ohm’s law and simultaneous readout through multiple bit lines (BLs). Furthermore, the nonvolatility of the ReRAM device saves energy for data retention and enables in-memory computing, which reduce the abovementioned data transfer bottleneck.\textsuperscript{[16–18]}

A large-sized CBA with a selection device is preferred to maximize MAC operation efficiency.\textsuperscript{[12,19]} To this end, stacking one selector and one ReRAM, referred to as the 1S1R device\textsuperscript{[20–23]} in this work, allows CBA to maximize its merits of minimum feature size and the potential of 3D stackability.\textsuperscript{[24]} Many reports in this field have made significant improvements in the new HNN platform.\textsuperscript{[25–27]} However, they have also revealed several challenges that need to be overcome to use 1S1R CBA practically. Among them, the issues related to 1R have been dealt with extensively,\textsuperscript{[12]} but the problems related to voltage drop, the so-called IR drop, along the interconnection wires (word line [WL] and BL), have been less focused on. Adding 1S to each memory cell further complicates the problem, as it also partakes in the applied voltage. The less focus on this issue can be ascribed to two reasons. The first is that the analytical treatment of this issue with such an extremely parallel circuit configuration in CBA is challenging. Thus, in most cases, a numerical simulation approach using the simulation program with integrated circuit emphasis (SPICE)-type package has been used.\textsuperscript{[28,29]} The other is that the problem can be mitigated when the resistance value

This work provides a comprehensive analytical analysis of one-selector-one-resistor (1S1R) crossbar array (CBA) device for hardware neural network (HNN) applications. Simplified analytical device models are prepared from a particular 1S1R device to validate the analysis. The read margin (RM) analysis results show that the V/3 voltage scheme and reduced selector leakage are necessary to maximize the RM and maximum operable size N of the CBA, where N indicates the number of wires (word line or bit line). The write margin (WM) analysis results show that the unwanted switching of the unselected cell during the write operation is unlikely in the 1S1R CBA even with a large N value, despite a voltage drop along the interconnection wire. The analysis of simultaneous multiply-and-accumulate operations is conducted using the analytical method to examine the influence of voltage drop according to the wire and memory cells in HNN applications. Reducing the wire resistance and on-state conductance increases the available N value when the selector operates near the threshold conditions. The proposed analytical model can estimate the maximum accuracy degradation of the HNN through the involvement of the unintentional voltage drop.
of the ReRAM cell is much higher than the sum of the wire resistances, which diminishes the urgent requirement of an analytical model. However, as the integration density, or CBA size, increases and the critical dimension decreases, the numerical simulation of the circuits takes considerable time. In addition, there can be cases in which the operating current is quite high, as for the filamentary-type ReRAM cell, where the IR drop becomes even more serious. If such an IR drop is not addressed appropriately, the output current can deviate significantly from the correct value during the inference step. In several cases, even unwanted switching can occur during the training step. The highly nonlinear current–voltage (I–V) characteristics of the selector devices render the experimental results deviating from the simple calculations based on Ohm’s law and Kirchhoff’s law.

Several studies have reported the IR drop effects for a feasible operation of ReRAM CBA with selection devices,[23,30] but none of them have estimated these adverse effects (IR drop and selector nonlinearity) simultaneously in a quantitative manner. In addition, these issues have been discussed for applying ReRAM-based CBA to the standard memory, where only a few WLs and BLs are selected and biased. However, they become even more serious when a large-sized CBA is used for HNN applications. This is because the MAC operations in HNN require the simultaneous application of bias voltages, even with different values, at different lines. This results in an even higher IR drop, which can incur an even reversed current flow along the selected path, which seriously undermines the HNN accuracy.

This work provides two critical improvements in this regard. First, an analytical model that calculates the read margin (RM) and write margin (WM) of 1S1R CBA is presented. This reveals the relation between material factors and the maximum operable size of 1S1R CBA. Second, an analytical circuit model is provided, which accurately calculates the deviation of the cell bias voltage from the desired value during the worst-case MAC operations, where different voltages are simultaneously applied to all WLs. This model elucidates the crucial design factors that should be considered when fabricating 1S1R CBA for HNN applications.

2. Results and Discussion

2.1. Single-Cell RM of 1S1R CBA for Write-and-Verify Scheme

Before discussing the array-level circuit models, the I–V models of the 1S1R device are defined as follows

\[ i_{1S1R}(V_{1S1R}) = \begin{cases} \alpha e^{\beta V_{1S1R}}, & 0 < |V_{1S1R}| < |V_{th}| \\ G^*(V_{1S1R} - V_{th}), & |V_{1S1R}| > |V_{th}|, \quad (G_0 \leq G^* \leq G_1) \end{cases} \]

where \( i_{1S1R}(V_{1S1R}) \) indicates the voltage-dependent current and \( V_{1S1R} \) indicates the voltage applied to the entire 1S1R device. \( V_{th} \) is a threshold voltage that corresponds to a specific \( V_{1S1R} \) over which 1S1R shows a useful memory window. When \( V_{1S1R} \) is lower (higher) than \( V_{th} \), the selector (memory) determines \( i_{1S1R}(V_{1S1R}) \). For the selector-dominant case, the I–V relation \( (i_{1S1R}(V_{1S1R})) \) can be represented by \( \alpha e^{\beta V_{1S1R}} \), where \( \alpha \) and \( \beta \) are appropriate constants, with dimensions of current and 1/V, respectively. For the memory-dominant case, \( i_{1S1R}(V_{1S1R}) \) can be approximated as \( G^*(V_{1S1R} - V_{th}) \), assuming a linear I–V relation for ReRAM, where \( G^* \) is the conductance of ReRAM in the 1S1R device. To represent the multiple conductance levels of ReRAM, \( G^* \) is set as an available conductance of ReRAM. For example, ReRAM with two levels, \( G^* \), has \( G_0 \) and \( G_1 \) as the high- and low-resistance state, respectively. ReRAM with four levels, \( G^* \), has \( G_0, G_{1/3}, G_{2/3}, \) and \( G_1 \), where \( G_{1/3} \) and \( G_{2/3} \) are the intermediate levels between \( G_0 \) and \( G_1 \) (\( G_0 < G_{1/3} < G_{2/3} < G_1 \)).

When the exponential I–V relation of the 1S device is approximated by a linear function, the following equation can be used.

\[ i_{1S1R}(V_{1S1R}) = \begin{cases} G_0 V_{1S1R}, & \left| V_{1S1R} \right| < \left| V_{th} \right|, G_0 \ll G_0 \\ G^*(V_{1S1R} - V_{th}), & \left| V_{1S1R} \right| > \left| V_{th} \right|, (G_0 \leq G^* \leq G_1) \end{cases} \]

Equation (2) assumes that the selector has a constant conductance \( G_s \), where \( G_0 \ll G_s \leq G_1 \). This work fundamentally assumes offline training and inference, meaning that the memory cell is programmed to the desired weight value following the previously calculated values by software-based simulation. In this case, write-and-verify and cell initialization may be required, depending on the switching mechanism of the ReRAM device. Therefore, only the selected cell within the given CBA must be accessed during the training step (cell writing and reading). In contrast, the simultaneous access of many cells sharing BLs is required during the inference step.

The success of these operations depends on the adopted voltage scheme and CBA size (numbers of WLs and BLs). Note that the same number of WLs and BLs, which is referred to as \( N_N \), is most effective in suppressing the unwanted sneak current issue.[24] Therefore, this work assumes that \( N_S \) is the total number of memory cells in a CBA and examines the material parameters and optimized voltage scheme to maximize the \( N_N \) value while ensuring the desired operations.

Among the voltage schemes used for the single-cell readout, the floating scheme is selected to investigate how other material factors and circuit designs affect the correctness of the readout. In the floating scheme, the floated wire works as a sneak current path, making the readout current deviate from the correct value.[24] The topology of the circuit with possible current paths is shown in Figure 1a. The conductance of the farthest cell from the WL/BL sources (gray cell in Figure 1a) is set to \( G_0 \), and it was attempted to read it to examine the worst case in the floating scheme. The other cells are set as \( G_1 \), maximizing the sneak current.[29] The amount of sneak current is much higher for CBA with ReRAM only (1R CBA) than that for 1S1R CBA. The circuit shown in Figure 1a can be converted into the equivalent circuit shown in Figure 1b, which facilitates the sneak current calculation. For simplicity, no wire resistance is assumed in this case. As shown in Figure 1b, the sneak current of 1R CBA with the floating scheme is calculated, as shown in Equation (3).

\[ I_{sneak} = (N - 1)G_1 \frac{N - 1}{2N - 2} V_s = \frac{2}{2N - 1} G_1 V_s \]
cell. Because no wire resistance is assumed, $V_s$ has the same value as $V_{1R}$. The RM, defined in Equation (4), is used to estimate the correctness of the readout.

$$RM = \frac{I_{\text{read}}}{I_{\text{read,0}}}
$$

where $RM$ indicates the ratio of the ideal readout current $I_{\text{read,0}}$, which is free from any spurious effects, including the IR drop and sneak current, other than the value determined by the cell conductance, and the measured readout current $I_{\text{read}}$ compared with the specified target current $I_{\text{read,0}}$. For a two-level ReRAM cell, $I_M = (I_0 + I_1)/2 = (G_0 + G_1)V_{1R}/2$. For a multilevel ReRAM cell, however, it can be the median value of the two neighboring states. For $I_{\text{read}} = I_{\text{read,0}}$, $RM = 1$, but for the large sneak current, RM approaches 0. In this work, the minimum level of RM is set to 0.1 for a reasonable read operation. From $I_{\text{read,0}} = G_0V_{1R}$ and $I_{\text{read}} = I_{\text{sneak}} + I_{\text{read,0}}$, Equation (4) can be rewritten as Equation (5) using the material parameters ($G_0$, $G_1$) and circuit design factors ($N$, $I_{\text{read,0}}$).

$$RM = 1 - \frac{(N - 1)^2}{2N - 1} \frac{G_1V_s}{I_M - G_0V_s}
$$

The analysis in Equation (5) shows that 1R CBA is operable only when $N \leq 2$, which means that 1R CBA is impractical, as explained next. For $I_M = (G_0 + G_1)V_{1R}/2$, irrespective of how high the memory window is ($G_1 \gg G_0$), RM becomes $1 - (N - 1)^2/2N$. This indicates that the maximum $N$ for a positive RM value is less than 2. Therefore, a selector is inevitable to read a cell state in a CBA irrespective of how small $N$ is.

A similar analysis can be performed for a 1S1R CBA. For this analysis, it is assumed that the high voltage is applied to the selected cell only, so $|V_{1S1R}| > |V_{th}|$, whereas all other cells are subjected to low voltage, so $|V_{1S1R}| < |V_{th}|$. To apply the desired read voltage $V_{1S1R}$ to the selected cell, a voltage $V_s$ having the same value as $V_{1S1R}$ is applied to WL #1 in Figure 1a. Under this circumstance, the 1S1R CBA circuit can be converted to the equivalent circuit shown in Figure 1c. Using Figure 1c and the model $i_{1S1R}(V_{1S1R})$, two equations for the forward-bias $V_f$ and reverse-bias $V_r$ applied to the 1S1R cells can be built as Equation (6) and (7).

$$2V_f + V_r = V_s
$$

$$\langle N - 1 \rangle a_1 e^{b_1 V_f} = \langle N - 1 \rangle^2 a_1 e^{b_1 V_r}
$$

Equation (6) represents Kirchoff’s voltage law (KVL) through the sneak current path, and Equation (7) shows Kirchoff’s current law through all sneak current paths, whose schematic diagrams are shown in Figure 1d. Equation (8) and (9) can be derived from Equation (6) and (7), respectively, to determine the unique values of $V_f$ and $V_r$ for the given material parameters ($a_1$, $a_2$, $b_1$, and $b_2$) and $N$.

$$V_f = \frac{b_1 V_s + \log(N - 1) - \log(\frac{a_1}{a_2})}{2b_1 + b_2}
$$

$$V_r = \frac{b_1 V_s - 2 \log(N - 1) + 2 \log(\frac{a_1}{a_2})}{2b_1 + b_2}
$$

Using Equation (8) and (9), the RM and maximum $N$ of 1S1R CBA can be written as Equation (10)–(12).

$$RM = 1 - \frac{(N - 1)}{I_M - G_0(V_s - V_{th})}
$$
Equation (11) is a rearrangement of Equation (10) to relate \( N \) to the given design factors. Equation (12) is the approximated version of Equation (11) when \( N \gg 1 \), showing the independence between \( N \) and \( V_f \). This approximation originates from the condition that \( V_s > 0 \), which justifies the presence of the reverse-biased cell irrespective of how large the value of \( N \) is. This condition requires that the upper bound of \( V_f \) should be \( V_s/2 \).

Using Equation (10)–(12), the relation between \( N \) and other design factors can be determined. One example is the number of weights per cell (or possible level numbers). Accommodating more data per cell helps maximize the data density and fast MAC operation; however, the gap between the current values of the neighboring states decreases. When a 1S1R device has a total number of linearly split \( P \) states, discerning a specific \( G_i \) from its neighbor \( G_i + G_{i+1} \) is required. This requirement corresponds to \( V_{th} = (G_0 + 0.5 \frac{G_1 - G_0}{P}) (V_{1S1R} - V_{th}) \). From this, Equation (12) can be rewritten as Equation (13).

\[
N \approx \frac{(1 - \text{RM})0.5(G_1 - G_0)(V_s - V_{th})}{(P - 1)q_e e^{h \frac{V_f}{T}}}
\]  

Equation (13) indicates that aggressive current scaling is necessary for the multilevel 1S1R CBA to be used in HNN. For example, 1S1R CBA for ternary HNN (\( P = 3 \)) can accommodate halved \( N \) compared with the binary (\( P = 2 \)) case when the other design factors are the same.

Meanwhile, a similar method can be applied to other voltage schemes, such as the \( V/n \) scheme (\( n = 2, 3 \)). Under this scheme, the sneak current originates from the electrical sources at WL \#2 to \#N, which can be effectively suppressed when \(|V_{th}| > |V_s/2|\). Because the total sneak current is \((N - 1)a_q e^{h \frac{V_f}{T}}\), RM and \( N \) of the \( V/n \) scheme can be expressed as Equation (14) and (15), respectively.

\[
N = 1 + \frac{(1 - \text{RM})(I_M - G_0(V_s - V_{th}))}{q_e e^{h V_f}}
\]

\[
N \approx \frac{(1 - \text{RM})(I_M - G_0(V_s - V_{th}))}{q_e e^{h V_f}}
\]

\[
\text{RM} = 1 - \left( N - 1 \right) \frac{a_q e^{h \frac{V_f}{T}}}{I_M - G_0(V_s - V_{th})}
\]

\[
N \approx \frac{(1 - \text{RM})(I_M - G_0(V_s - V_{th}))}{a_q e^{h \frac{V_f}{T}}}
\]

The forms of RM and \( N \) of the two schemes differ only in the voltage term in the exponent. The comparison between the floating and \( V/n \) schemes for the RMs can be found in Equation (16) and (17).

\[
1 - \text{RM}_{\text{float}} = \frac{a_q e^{h V_f}}{a_q e^{h \frac{V_f}{T}}} = e^h (V_f/2) < e^h V_f (1/3)
\]

\[
e^{-\frac{h}{N} \left( \log^2 (\frac{2}{3}) \right)} < e^h (V_f/2) < e^h V_f (1/3)
\]

When the floating and \( V/2 \) schemes are compared using Equation (16), the RM of the floating scheme is always higher for a given \( N \). Equation (17) shows the upper and lower bounds of the ratio of the RMs between the floating scheme and \( V/3 \) scheme, where the upper and lower bounds are determined from Equation (16) and minimum of Equation (8) with \( N = 2 \), respectively. The lower bound of Equation (17) shows that the RM of the \( V/3 \) scheme mostly exceeds that of the floating scheme. For example, adopting the selector device with symmetric \( I-V \) \((a_1 = a, b_1 = b)\) makes the lower bound 1. For a particular asymmetric selector, the lower bound of the ratio can be smaller than 1. However, increasing \( V_f \) for a large \( N \) increases the RM ratio, whose upper bound is determined by Equation (17). These analyses show that the \( V/3 \) scheme becomes more desirable for the CBA with a larger \( N \) for a given RM.

The proposed model was compared with the numerically simulated RM using the HSPICE package to validate the abovementioned analytical RM model. All numerical simulations were based on the experimental \( I-V \) curve of the 1S1R device, as shown in Figure 2a. The 1S1R device was fabricated with the HfO2-based resistive switching layer and TiO2-based nonlinear selector, the details of which are included in the online Supporting Information (SI). The 1S1R device sets and resets in the negative- and positive-bias regions, respectively. Four levels of conductance values were obtained by varying...
the maximum reset voltage during the reset sweep in the positive-bias direction. In Figure 2a, the thin lines indicate the experimental data, and the thick lines indicate the curves obtained from the numerical model. In the negative-bias region, \( V_{th} \) was \( \approx -1.7 \text{ V} \), so \( I_{th} \approx \alpha \left| V_{1S1R} - V_{th} \right| \) for \(-2.2 \text{ V} < V_{1S1R} < -1.7 \text{ V}\), as shown in Figure 2b (thick straight lines), using the conductance values indicated in the figure.

The nonlinear portion of the \( I-V \) curve at \(-1.3 \text{ V} < V_{1S1R} < -0.6 \text{ V}\) was fit using \( I_{1S1R} \approx \alpha_{f} V_{1S1R} \) with the parameters shown in Figure 2c for the forward and reverse biases. The linear \( I-V \) model of 1R can be constructed with the identical conductance values shown in Figure 2b but with no involvement of \( V_{th} \).

Figure 3a shows the calculated RM from the analytical and numerical models with three different voltage schemes. The conductance of the selected cell was set to \( G_{0} \), and its current was read, where the read current must follow the black curve shown in Figure 2a if the sneak current effect is minimized. As mentioned previously, the \( V/3 \) scheme shows the largest RM compared with the other voltage schemes for the given design factors, suggesting that the \( V/3 \) scheme should be used to accurately determine the read current from a larger CBA.

Four virtual numerical models with different selector parameters were built to evaluate the relation between RM and the leakage current of the selector. For these numerical simulations, the parameter that determines the selector leakage current of the original numerical model was varied, and the dotted \( I-V \) curves in Figure 3b correspond to the numerical simulation results. Then, the analytical model was used to fit the numerical curves for \( |V_{1S1R}| < |V_{th}| \) by varying the \( \alpha \) and \( b \) values, whose appropriate values are included in the inset table in Figure 3b. The required applied voltage to WL #1 (\( V_{f} \)) is different for different cases to match the magnitude of the readout current. Figure 3c shows that the calculated RM values from both the analytical and numerical models match well, demonstrating the analytical model’s accuracy. The device with a higher leakage current (or larger \( \alpha_{f} \)) has a smaller \( N \) value while guaranteeing the desired RM for the given design factors. The relation between \( \alpha_{f} \) and \( N \) can be explained mathematically by the partial derivative \( \frac{\partial N}{\partial \alpha_{f}} = -\left( N - 1 \right) \frac{1}{V_{th}} \), which can be derived from Equation (14).

This value is always negative for all combinations of \( N, V_{f}, \) and \( n \), suggesting that the increased sneak current reduces the RM even when a small \( V_{s} \) is used. In addition, although decreasing the \( \alpha_{f} \) may enhance the RM, a larger \( V_{s} \) is required to ensure a sufficient read current, which is necessary for the rapid readout. Therefore, there is an inevitable tradeoff between the achievable RM and the involved energy consumption when modulating the selector parameters.

Three other virtual numerical models with different current variations were built to evaluate the relation between RM and the current variation of the selector. Although the device variation modeling is complicated, the variation of RM can be predicted, and it can be used to control the nonidealities of the 1S1R device and CBA. The detailed simulation methods and results are included in the online Supporting Information.

### 2.2. Single-Cell WM of 1S1R CBA for Write-and-Verify Scheme

The IR drop becomes a much more severe problem for write access. Even single-cell access can be a problem because ReRAM requires a higher operating current during writing than reading. The probable write failure originates from the fact that the \( V_{s} \) of the WL connecting the selected cell should be increased to apply the desired switching voltage (\( V_{sw} \)) to the selected cell. The difference between \( V_{s} \) and \( V_{w} \) originates from the IR drop over the wires. When the \( V_{s} \) is too large, a bias applied to the unselected cell (\( \Delta V_{us} \)) also increases, and if it exceeds the switching voltage (\( V_{sw} \)) of the unselected cell, the cell undergoes unwanted switching. WM can be defined as Equation (18).

\[
WM = \frac{|V_{sw}| - |\Delta V_{us}|}{|V_{w}|} \tag{18}
\]

When \( \Delta V_{us} \) approaches \( V_{sw} \), WM approaches 0. To analyze the WM quantitatively, the nonselected cell representing the

![Figure 3. Comparison of RM results from both the analytical and numerical 1S1R models. a) Curves of RM with different voltage schemes. The data from both the analytical model (line) and numerical simulation (dots) are shown. b) Curves of four hypothetical numerical 1S1R models. Both \( G_{1} \) (hairline) and \( G_{0} \) (dotted line) curves are shown. The inset table shows the fitted parameters of the analytical model that match the corresponding numerical model. c) Curves of RM with different \( b_{f} \) values drawn from the inset table in (b). The data obtained from both the analytical model (line) and numerical simulation (dots) are shown.](image-url)
The worst-case circumstance should be focused on. The position of the worst-case unselected cell and the type of \( V_{sw} \) depend on the type of voltage scheme used.\(^\text{[23]}\) In this work, the same weight mapping method is used for the RM evaluation case and floating voltage scheme. Under this circumstance, the selected cell is supposed to be set, and the cell at the intersection of WL #N and BL #1 (coordinate \((N,1)\)) is most vulnerable to the unwanted reset switching.\(^\text{[30]}\) Therefore, \( V_w, V_{sw}, \) and \( \Delta V_{us} \) correspond to the set voltage, reset voltage, and applied voltage to the cell at coordinate \((N,1)\), respectively.

Without the IR drop, the weight mapping and voltage scheme for this circumstance is the same as the settings for Equation (9). \( \Delta V_{us} \) is the same as \( V_s \) in Equation (9). \( \Delta V_{us} \) can be expressed as follows.

\[
\Delta V_{us} = \frac{b_t}{2b_t + b_f} V_s - \frac{2(\log(N - 1) - \log(\frac{a_t}{a_f}))}{2b_t + b_f}
\]

Equation (21) indicates that \( \Delta V_{us} \) will have a minimum value with an increasing value of \( N \), because the increase in \( V_s \) is proportional to that in the \( N^2 \) term shown in Equation (20), which has a more significant influence than the \( \log(N) \) term shown in Equation (21).

To validate the proposed WM model, it was compared with the numerically simulated WM using HSPICE. The settings for all simulations were the same as those for the RM simulations. \( r_{cc} \) is set as 0.5 \( \Omega \), which is sufficiently large to examine the IR drop-related problems. The \( r_{cc} \) is dependent on the type of metal and its thickness.\(^\text{[23,30,31]}\) The set and reset voltages of the 1S1R device were set as -2.8 and 1.8 V, respectively, as determined from the I-V data shown in Figure 2a.

Figure 4b shows the variation in the required \( V_s \) to apply the set voltage of \(-2.8 \) V to the selected cell (gray cell in Figure 1a), calculated by both the proposed analytical model (line) and the corresponding numerical model (red squares). The coincidence between the two results validates the proposed analytical model.

2.3. Sneak Current in Fully Biased 1S1R CBA Considering HNN Applications

In the previous discussion, the read and write functions were assumed to be conducted in a cell-by-cell manner, which is appropriate for a standard memory operation and minimizing the IR drop effect. However, this is not the case for inferencing in HNN, where the read voltages must simultaneously be applied to multiple WLs to accomplish the MAC operation. The inference can be accelerated by reading currents through multiple BLs, representing the sum of the multiplications of inputs and optimized weight values. In this case, the IR drop along the wires becomes more serious as the total current increases, which deteriorates the inference accuracy of HNN and even fails the HNN operation if it becomes too large. An analytical model that can calculate the voltage distribution and current flow across the entire 1S1R CBA for such a circumstance is introduced in this section. A representative circumstance is shown in Figure 5a, where the number 5 images are taken as the input. Most images have different intensities of the input signals in each pixel. When an image is converted into a 1D input vector, as shown in the right portion of Figure 5a, the input intensities...
are represented by the voltage. The strong WL signals near the BL voltage source can induce a high IR drop through the BL. Depending on the relative voltage values of the different WLs, the readout current may significantly deviate from the correct value.

Figure 5b shows the worst-case example of the voltage application. In this case, a large voltage \( V_{w} \), representing the intense signal of the input pixel, is applied to WL #2 to #N, while a small voltage \( V_{s} \), representing the background of the input image, is applied to WL #1. \( V_{w} \) increases the potential of BL at nodes far from the BL voltage sources (ground). Under this circumstance, the voltages of the cells connected to WL #1 are severely distorted, and the cell at the intersection of WL #1 and BL #N (gray cell at the lower-right corner in Figure 5b) experiences the highest distortion. The distortion can be modeled using the design parameters, including wire resistance, and the model can be used to improve the performance of the CBA-based HNN by optimizing the circuit parameters.

The analytical model used for such circumstances is first settled in 1R CBA to simplify the problem, which is impractical, as stated in the RM analysis section. Then, the analysis is extended to the 1S1R CBA case, which is practical. In this analysis, the current passing through the cell intersecting WL #M and BL #N is defined as \( I_{M,N} \), and all these values are solved using the sets of KVL equations, as shown in Equation (22) and (23).

\[
V_s - r_{cc}(I_{1,1} + I_{1,2} + \ldots + I_{1,N}) = \frac{I_{1,1}}{G_1} - r_{cc}(NI_{1,1} + (N - 1)I_{2,1} + \ldots + I_{N,1}) = \overline{\sigma}
\]  

\[
V_s - r_{cc}AX_1 = -\frac{1}{G_1}X_1 - r_{cc}(NX_1 + (N - 1)X_2\ldots + (N - 2)X_3\ldots + 1X_N) = \overline{\sigma}
\]  

Equation (22) represents the KVL of the current path from WL #1 to BL #1, indicated by the red arrow in Figure 5b. Along this path, the sources of the IR drop are the memory cells and wire slices, that is, the term \( r_{cc}(I_{1,1} + I_{1,2} + \ldots + I_{1,N}) \) represents the IR drop through the single WL slice connecting the WL #1 source and top of the cell between WL #1 and BL #1. The term \( r_{cc}NI_{1,1} \) represents the total IR drop along the entire BL #1 induced by \( I_{1,1} \). The term \( r_{cc}(N-1)I_{2,1} \) represents the IR drop along the \((N-1)\) slices of BL #1 induced by \( I_{2,1} \) and so on.

Equation (23) is an \( N \)-by-1 matrix expression of Equation (22), representing the KVL of all current paths that start from the WL #1 source. For example, the second and last terms of Equation (23) represent the KVL of the path from WL #1 to BL #2 (the green arrow in Figure 5b) and #N (the blue arrow in Figure 5b), respectively. The term \( X_3 \) is an \( N \)-by-1 vector, which comprises \( I_{3,1}, I_{3,2}, \ldots, I_{3,N} \); \( V_s \) is an \( N \)-by-1 vector that comprises only \( V_{s} \); \( I \) is an \( N \)-by-\( N \) identity matrix; \( A \) is an \( N \)-by-\( N \) matrix defined as \( A_{ij} = \min(i,j) \), representing the IR drop through the WL slices; and \( \overline{\sigma} \) is an \( N \)-by-1 zero vector. As mentioned above, all ReRAM cells are assumed to be at \( G_1 \) for the worst-case IR drop and calculation simplicity. Other matrix equations for all current paths that start from
Figure 5. Schematic and calculation results of the CBA scheme with fully biased WLs and BLs. a) Schematics of transformation of 2D MNIST image into 1D voltage vector for resistive CBA. b) Schematics of N-by-N resistive CBA with fully biased lines. c) Five numerical models of 1R (dashed line) and 1S1R (hairline) devices that have different $G_1$ values. d) Calculated $\Delta V_{1,N}$ with different WL #1 source voltages in fully biased 1R CBA. The data from both the analytical model (Equation (26) (hairline)) and numerical simulation (dots) are shown. e) Calculated $\Delta V_{1,N}$ with different WL #1 source voltages in fully biased 1S1R CBA. The data from both the analytical model (Equation (28) (hairline)) and numerical simulation (dots) are shown.

The other WLs can be constructed similarly as Equation (24) and (25).

$$\begin{align*}
\nabla_w - r_{cc} A \Delta X_2 &= \frac{1}{G_1} \Delta X_2 - r_{cc} ((N - 1)X_1 + (N - 1)X_2 + (N - 1)X_N) = 0 \\
\nabla_w - r_{cc} A \Delta X_N &= \frac{1}{G_1} \Delta X_N - r_{cc} (1X_1 + 1X_2 + 1X_3 + \ldots + 1X_N) = 0
\end{align*}$$

Equation (24) and (25) represent the KVL of all current paths that start from WL #2 and WL #N sources, respectively. Solving the $N$ matrix equations, including Equation (23)–(25), results in the new equation of $\Delta X_N$ using $\Delta X_1$, and plugging the approximated solution of $\Delta X_N$ to the new equation, renders the new equation represented by $\Delta X_1$ without involving $\Delta X_2, \ldots, \Delta X_N$. After that, the desired $\Delta V_{1,N}$, which is the voltage across the selected cell, can be achieved by dividing $\Delta X_1$ by $G_1$. If the calculated $\Delta V_{1,N} < 0$, the current passing through the cell is reversed, which should be avoided.

The process of deriving $\Delta V_{1,N}$ in the analytic form is explained in detail in the online Supporting Information. The final form of $\Delta V_{1,N}$ is shown in Equation (26).

$$\begin{align*}
\Delta V_{1,N} &= V_w \left( \frac{4/\pi}{1 + c_0} \left( 1 - F_N \left( \frac{k}{\sqrt{1 + c_0}}, N \right) \right) \right) \\
&\quad - \frac{4/\pi - 1}{(1 + c_1)} \left( 1 - F_N \left( \frac{k}{\sqrt{1 + c_1}}, N \right) \right) \\
&\quad - (V_w - V_s)(1 - F_N(k, N))
\end{align*}$$

$F_N(k, N) = \left( \frac{\cos h(k(0.5 + N))}{\cos h(k(0.5k)) \cos h(k(0.5k))} \right)$

where $k = \sqrt{r_{cc} G_1}$, $c_0 = \left( \frac{2hN}{\pi} \right)^2$, $c_1 = \left( \frac{2hN + 1.613}{\pi} \right)^2$.

Although Equation (26) appears quite complicated, $c_0$, $c_1$, and $F_N$ are the functions of $k$. If $r_{cc} = 0$, $k = 0$, all functions that depend on $k$ become 0, and $\Delta V_{1,N}$ becomes $V_s$, which corresponds to the ideal value of $\Delta V_{1,N}$. The variation in $\Delta V_{1,N}$ with increasing $N$ for $r_{cc} > 0$ will be explained later.

The term $\Delta V_{1,N}$ for 1S1R CBA under the same circumstance can be derived similarly, considering the nonlinear conductance of the 1S1R device. As all cells in the CBA are applied with a voltage close to the read voltage, the $i_{1S1R}(V_{1S1R})$ model in Equation (2) is used to reflect the selector behavior near the read voltage. It is assumed that a high $V_{1S1R}$ voltage with $|V_{1S1}| > |V_{1R}|$ is applied to the cells intersecting WL #1, whereas
a lower $V_{1S1R}$ voltage with $|V_{1S1R}| < |V_{th}|$ is applied to all other cells. These assumptions can be justified by the fact that $V_r$ has a smaller magnitude than $V_w$, and $V_i$ is sufficiently close to the $V_{th}$.

$$
\Delta V_{1,N} = (V_w - V_{th}) \left( 4 \left( \frac{1 - g}{1 - (1 + c_0)g} (1 - F_N(\sqrt{gk}, N)) + \frac{-c_0}{1 - (1 + c_0)g} \right) \right) + (V_w - V_i)(1 - F_N(\sqrt{gk}, N))
$$

where $g = \frac{C_0}{C_1}$, and all values and functions are equivalent to their counterparts of Equation (26) and (27). The detailed derivation processes of Equation (28) are included in the online Supporting Information.

To validate the calculated $\Delta V_{1,N}$ from Equation (26) and (28), $\Delta V_{1,N}$ was compared with the numerically simulated $\Delta V_{1,N}$ using the HSPICE package. For these calculations, the necessary $I-V$ curves for the 1S1R and 1R devices were depicted by the thick line and dashed line curves, respectively, in Figure 5c. The analytical model was prepared by setting the resistance of 1R to induce the current value of the numerical 1S1R model in Figure 2a. This model was also used for the numerical simulation of 1R CBA. In the case of 1S1R CBA, the analytical model was prepared using Equation (2) with the given parameters. The ReRAM-dominant region was prepared similarly to the analytical 1R model, and the selector-dominant region was represented as $G_s = 0.01G_1$. For the numerical simulation of 1R CBA, the numerical model in Figure 2a was used.

Figure 5d,e shows the $\Delta V_{1,N}$ obtained by the calculations performed out using the analytical and numerical models in 1R CBA and 1S1R CBA cases, respectively. Both figures validate the proposed analytical models. In the case of 1R CBA, $\Delta V_{1,N}$ increases from the settled negative $V_i$ values ($-0.05$, $-0.1$, and $-0.2$ V) toward the positive values as $N$ increases. When the $V_i$ values are $-0.05$ and $-0.1$ V, the $\Delta V_{1,N}$ value becomes even positive when $N > 60$ and $110$, respectively. The reversed sign of $\Delta V_{1,N}$ indicates that the read current cannot be flown into the sensing circuit, suggesting a serious malfunction of the circuit.

In the case of 1S1R CBA, however, no such voltage sign reversal is observed for all tested $V_i$ values up to $N = 200$, as shown in Figure 5e. This finding demonstrates the importance of adopting the appropriate selector again. The magnitude of $\Delta V_{1,N}$ variation is similar for both 1R and 1S1R CBA up to $N = 200$ and decreases with a decrease in $V_i$.

Changing the factors in Equation (26) and (28) reveals how they affect the deviation of $\Delta V_{1,N}$ from the intended value. The most crucial factor is $k = \sqrt{r_{cc}G_s}$, which frequently appears in both equations. The functional form of $k$ indicates that decreasing the wire resistance and $G_s$ have similar significance in determining the IR drop. Figure 6a,b shows the relation between $N$ and $\Delta V_{1,N}$ in 1R CBA and 1S1R CBA, respectively. For these calculations, the $G_i$ and $k$ values included in the inset table of Figure 5c are used. Given the limitation that $r_{cc}$ should be decided by the material of metal wire and design rule, it is convenient to control $G_s$ to suppress the undesirable IR drop effect.

It can be understood that decreasing $G_s$ of the ReRAM device is highly beneficial to avoid the increase in $\Delta V_{1,N}$. However, there can be a limitation of the achievable range of $G_s$, depending on the specific ReRAM type.

Figure 6c shows $\Delta V_{1,N} - V_s$ as a function of $N$ with different $b_1$ values of $1S1R$, and a list of $b_1$ values is shown in the inset table in Figure 6c. It is expected that $\Delta V_{1,N} - V_s = 0$, when $V_{1S1R}$ is applied with no circuit artifacts. Under the adverse circuit effect, such as $r_{cc}$, however, $\Delta V_{1,N}$ becomes smaller than $V_s$. Note that the appropriate $V_i$ varies with $b_1$ to render the read current identical among 1S1R models with varying $b_1$, as mentioned in the previous section.

The shape of $\Delta V_{1,N} - V_s$ graph is independent of the selection of $b_1$ when $|V_{1S1R}| > |V_{th}|$. This is because the selector parameter, $b_1$, plays a role only for $|V_{1S1R}| < |V_{th}|$. For $|V_{1S1R}| > |V_{th}|$, the circuit current should be governed by the memory cell and not the selector.

Figure 6d shows the variation in $\Delta V_{1,N}$ calculated by Equation (28) when varying the value of $G_s$ (thick lines). It also shows that $\Delta V_{1,N}$ becomes similar to the numerical simulation results (black square data) as $G_s$ decreases, demonstrating the accuracy of the analytical model. Note that varying the conduction values of 1S and 1R results in an opposite influence on the voltage behavior.

The $\Delta V_{1,N}$ model can be used to quantitatively understand how the design parameter affects the performance of CBA-based HNN, although it can be conjectured that increasing $r_{cc}$ deteriorates the accuracy of the programmed HNN. The next section describes how this model can be used to estimate the accuracy of the MAC operation in the CBA-based HNN.

2.4. Application of Analytical $\Delta V_{1,N}$ Model

To demonstrate the usefulness of the analysis, two single-layer CBAs with 196 and 324 WLs, respectively (left and right panels of Figure 7a), were assumed, both of which were programmed with externally trained weights for the Modified National Institute of Standards and Technology Database (MNIST) dataset identification. As the MNIST dataset has only ten classes, the CBA with 196-by-10 or 324-by-10 sizes should be used for the single-layer HNN. However, the developed analytical model
assumes N-by-N CBA, so the assumed CBA had a square shape, as shown in Figure 7a. To accommodate the discrepancy, the trained weight values were programmed at the farthest positions (BL #187 to #196 for the former and BL #315 to #324 for the latter) from the WL voltage source, as shown in Figure 7a, which shows the maximum influence of the IR drop and sneak current. In this case, all unprogrammed cells (sharing the BL #1 to #186 for the former and BL #1 to #314 for the latter) were assumed to have the lowest conductance ($G_0$), where the four levels of conductance ($G_0$, $G_{1/3}$, $G_{2/3}$, and $G_1$ in Figure 2b) were selected for the trained weight values.

After that, the HNN inference was simulated using HSPICE with different $r_{cc}$ values to monitor the test accuracy. Figure 7b shows the simulated test accuracy of HNN with the programmed weights in Figure 7a for the different $r_{cc}$ values. When $r_{cc}$ (or $k$) is zero, the test accuracy is $\approx 84\%$ and $87\%$ for the 196 and 324 WL cases, respectively. These values are not sufficiently high because only a single-layer HNN structure is adopted. However, this study focuses on examining the $r_{cc}$ effect, and thus, only the degradation of this value is significant in this study. When $r_{cc}$ increases to $\approx 0.3\Omega$ for $G_0$ of $1.21 \times 10^{-5}$ S ($k \approx 2 \times 10^{-5}$), the test accuracy deteriorates significantly by $\approx 5\%$. For these simulations, all input vectors have different $V_w$ and $V_s$ values in each case, making the quantitative analysis of allowable $N$ complicated and the related understanding difficult.

Therefore, the analytical model for calculating $\Delta V_{1,N}$ discussed in the previous section was used under the assumption that $V_w = -2.2$ V, $V_s = -1.7$ V, and $G_0 = 1.038 \times 10^{-5}$ S. This is the worst-case calculation; as such unfavorable WL voltage application rarely occurs.

Figure 7c shows the variation in $\Delta V_{1,N}$ as a function of $k$, where $\Delta V_{1,N}$ is $\approx 0.03$ V when $k \approx 2 \times 10^{-5}$, the value at which the accuracy degrades by $\approx 5\%$, as shown in Figure 7b. Therefore, $\Delta V_{1,N}$ of 0.03 V can be used as a criterion for CBA to efficiently conduct the MAC operation without involving a significant performance degradation. Figure 7d,e shows the variation in $N$ with increasing $r_{cc}$ for the different values of $G_0$ of the memory cell and $G_s$ of the selector, respectively, indicated in each figure, when $\Delta V_{1,N}$ is 0.03 V. Figure 7d shows that $N > 100$ requires $r_{cc} < 0.7\Omega$ for all $G_0$ values smaller than $\approx 10^{-5}$ S, demonstrating
the importance of a low IR drop again. Figure 7e shows that to not hamper the performance improvement by decreasing the memory cell conductance, $G_s$ should be $<0.1G_0$. It also indicates that the $G_s$ in influence does not significantly vary once it becomes $<0.05G_0$. By comparing the maximum $N$ obtained from the WM and RM of a single cell, the fully biased RM becomes the size-limiting factor of 1S1R CBA.

Other HNN test accuracy analyses were conducted by changing $G_0$ and $b$ of the 1S1R model. The $\Delta V_{1,N}$ model verifies that the relation between HNN test accuracy and $G_0$ is equivalent to that between test accuracy and $r_{cc}$. The $\Delta V_{1,N}$ model can also explain the independence between the test accuracy and $b$. The detailed simulation methods and results are included in the Supporting Information.

3. Conclusion

This work presents an analytical circuit model for CBA with a high $N$ value ($>100$) for an efficient evaluation of the device parameters on the training and inference performances of an HNN composed of 1S1R bipolar ReRAM cells. For offline training, the optimized weight values, represented by the conductance of the ReRAM cell, calculated in the software using backpropagation, are programmed through the write-and-verify method. In this method, evaluations of the WM and RM are necessary for a device model of 1S1R and the given wire resistance. The CBA composed of only 1R memory cells cannot provide any meaningful WM or RM due to the severe interference caused by the unwanted switching and high sneak current. In contrast, 1S1R provides useful device performance, especially when the $V/3$ scheme is used. In general, a higher source voltage is necessary to render the selected cell voltage reach the desired value when a voltage drop occurs along the wires due to their finite resistance. Interestingly, the WM increases with $N$ because of the higher voltage drop across the wires, which practically decreases the magnitude of the unwanted reverse voltage at the unselected cell, despite the increased source voltage. Therefore, the write-and-verify method can practically be used for weight assignment in a CBA-based HNN.

The concurrent application of the input voltages to all WLs at the inference stage for MAC operation makes the analytical modeling of the CBA-based HNN extremely challenging. Such a problem becomes even more severe as the $N$ value increases beyond 100, rendering the numerical simulation using HSPICE impractical. An analytical model can be used to solve the voltage
equation at the worst node of the CBA under the given bias condition. Because of the finite voltage drop over the wires, even a reverse bias can be applied to the worst-case node, which severely interferes with the accurate inference. The 1S1R-type device is mandatory in this regard, and lower wire resistance and cell conductance values further help the precise estimation of the sum of the output currents in the CBA with high N numbers. A quantitative analysis of the unwanted voltage effect in the worst-case voltage applications reveals that $r_{cc} < 0.7 \, \Omega$ for a reasonable memory cell conductance of $\approx 10^{-3} \, \text{S}$ is required to secure the accurate operation of CBA with $N > 100$.

4. Numerical Simulation Method

HSPICE was used as an analog circuit simulator to implement a numerical simulation of the 1S1R device. In the simulator, the numerical simulation of the 1S1R device was expressed as a serial combination of the ReRAM model and selector model. The ReRAM model comprises a single nonlinear resistor to represent the high-range voltage where the memory window appears. The selector model comprises multiple nonlinear resistors to represent the low- and midrange voltages of the 1S1R device. The ReRAM model has a state parameter whose value is set between 0 and 1 to express the intermediate states of the 1S1R model.

Curve fitting was conducted in order of selector model and ReRAM model to the numerical simulation to mimic the measurement data in Figure 2a. Two numerical 1S1R models were developed to represent positive- and negative-biased devices, respectively. The training process of optimized weights for offline HNN training is included in the online Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

J.K. designed the device models and conducted simulations using the models. H.W. designed and fabricated the one-selector-one-resistor devices and analyzed electrical data. T.J. and J.-H.C. supported the analysis of the algorithms. C.S.H. directed the whole work and prepared the manuscript.

Data Availability Statement

Research data are not shared.

Keywords

crossbar arrays, IR drop, neural networks, one selector–one resistor, simulation models

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[1] A. Krizhevsky, I. Sutskever, G. E. Hinton, Adv. Neural Inf. Process. Syst. 2012, 25, 1097.
[2] K. Simonyan, A. Zisserman, in 3rd Int. Conf. on Learning Representations, ICLR 2015—Conf. Track Proc., 2015, p. 1.
[3] K. He, X. Zhang, S. Ren, J. Sun, in Proc. IEEE Conf. Computer Vision and Pattern Recognition, IEEE, Piscataway, NJ 2016, pp. 770–778.
[4] V. Mnih, K. Kavukcuoglu, D. Silver, A. Graves, I. Antonoglou, D. Wierstra, M. Riedmiller, arXiv Prepr. arXiv1312.5602, 2013.
[5] D. Silver, A. Huang, C. J. Maddison, A. Guez, L. Sifre, G. Van Den Driessche, J. Schrittwieser, I. Antonoglou, V. Panneershelvam, M. Lanctot, S. Dieleman, D. Grewe, J. Nham, N. Kalchbrenner, I. Sutskever, T. Lillicrap, M. Leach, K. Kavukcuoglu, T. Graepel, D. Hassabis, Nature 2016, 529, 484.
[6] Y. Lecun, Y. Bengio, G. Hinton, Nature 2015, 521, 436.
[7] R. Raina, A. Madhavan, A. Y. Ng, in Proc. 26th Annual Int. Conf. Machine Learning, 2009, pp. 873–880.
[8] D. Ciregan, U. Meier, J. Schmidhuber, in 2012 IEEE Conf. Computer Vision and Pattern Recognition, IEEE, Piscataway, NJ 2012, pp. 3642–3649.
[9] N. P. Jouppe, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers, in Proc. 44th Annual Int. Symp. on Computer Architecture, 2017, pp. 1–12.
[10] J. Backus, Commun. ACM 1978, 21, 613.
[11] M. Prezioso, F. Merrih-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, D. B. Strukov, Nature 2015, 521, 61.
[12] M. Hu, J. P. Strachan, Z. Li, E. M. Grafals, N. Davila, C. Graves, S. Lam, N. Ge, J. J. Yang, R. S. Williams, in Proc.—Design Automation Conf. 2016, p. 1.
[13] C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, Q. Xia, Nat. Commun. 2018, 9, 7.
[14] Z. Wang, C. Li, W. Song, M. Rao, D. Belkin, Y. Li, P. Yan, H. Jiang, P. Lin, M. Hu, J. P. Strachan, N. Ge, M. Barnell, Q. Wu, A. G. Barto, Q. Qiu, R. S. Williams, Q. Xia, J. J. Yang, Nat. Electron. 2019, 2, 115.
[15] P. Yao, H. Wu, B. Gao, J. Tang, Q. Zhang, W. Zhang, J. J. Yang, H. Qian, Nature 2020, 577, 641.
[16] D. S. Jeong, K. M. Kim, S. Kim, B. J. Choi, C. S. Hwang, Adv. Electron. Mater. 2016, 2, 1600090.
[17] S. Yu, Proc. IEEE 2018, 106, 260.
[18] Z. Wang, H. Wu, G. W. Burr, C. S. Hwang, K. L. Wang, Q. Xia, J. J. Yang, Nat. Rev. Mater. 2020, 5, 173.
[19] R. M. Radway, A. Bartolo, P. C. Jolly, Z. F. Khan, B. Q. Le, P. Tandon, T. F. Wu, Y. Xin, E. Vianello, P. Vivet, E. Nowak, H. S. P. Wong, M. M. S. Aly, E. Beigne, M. Wootters, S. Mitra, Nat. Electron. 2021, 4, 71.
[20] Y. Yang, J. Lee, S. Lee, C.-H. Liu, Z. Zhong, W. Lu, Adv. Mater. 2014, 26, 3693.
[21] B. J. Choi, J. Zhang, K. Norris, G. Gibson, K. M. Kim, W. Jackson, M. X. M. Zhang, Z. Li, J. J. Yang, R. S. Williams, Adv. Mater. 2016, 28, 356.
[22] S. G. Kim, J. C. Lee, T. J. Ha, J. H. Lee, J. Y. Lee, Y. T. Park, K. W. Kim, W. K. Ju, Y. S. Ko, H. M. Hwang, in 2017 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2017, pp. 1–2.
[23] Y. Kim, Y. J. Kwon, J. Kim, C. H. An, T. Park, D. E. Kwon, H. C. Woo, H. J. Kim, J. H. Yoon, C. S. Hwang, Adv. Electron. Mater. 2019, 5, 1.

[24] J. Y. Seok, S. J. Song, J. H. Yoon, K. J. Yoon, T. H. Park, D. E. Kwon, H. Lim, C. H. Kim, D. S. Jeong, C. S. Hwang, Adv. Funct. Mater. 2014, 24, 5316.

[25] T. Kim, H. Kim, J. Kim, IEEE Electron Device Lett. 2017, 38, 1228.

[26] J. Woo, X. Peng, S. Yu, in Proc.—IEEE Int. Symp. Circuits Systems, IEEE, Piscataway, NJ 2018, p. 18.

[27] W. Wang, A. Bricalli, M. Laudato, E. Ambrosi, E. Covi, D. Ielmini, in Technical Digest—Int. Electron Devices Meeting, IEDM, 2019.

[28] B. Liu, H. Li, Y. Chen, X. Li, Q. Wu, T. Huang, in Proc.—Design Automation Conf. 2015.

[29] S. Jain, A. Sengupta, K. Roy, A. Raghunathan, IEEE Trans. Comput. Des. Integr. Circuits Syst. 2021, 40, 326.

[30] K. J. Yoon, W. Bae, D. K. Jeong, C. S. Hwang, Adv. Electron. Mater. 2016, 2, 1.

[31] G. H. Kim, K. M. Kim, J. Y. Seok, M. H. Lee, S. J. Song, C. S. Hwang, J. Electrochem. Soc. 2010, 157, G211.