Small signal modelling and stability analysis of internal ramp compensated constant on-time controller with improved output voltage accuracy for point of load application

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Abstract
This paper investigates a constant on-time controller (COT) with internal ramp compensation and improved output voltage accuracy for point of load applications. The pulse width modulation (PWM) output is generated based on internal ramp: by sensing the regulated output voltage and comparing it to an internal reference target, an error signal is generated. This error signal is used to generate a reference for an added ramp signal, which is compared against an error voltage to generate a PWM trigger signal. An adaptive constant on-time scheme ensures a fairly constant switching frequency over a wide range of input and output voltages. This COT control algorithm is able to achieve high accuracy regulation (±0.5% of target) and fast transient response during load step change. A frequency domain small signal model is proposed, and an open loop gain transfer function is developed for this COT control system. The proposed small signal model and design analyses are verified with SIMPLIS simulations and experimental results.

1 | INTRODUCTION

The popularity of constant on-time (COT) control architecture continues to increase for point of load (POL) applications. Compared with conventional voltage-mode and current-mode control schemes, constant on-time control has the following advantages: (1) fast transient response with direct voltage feedback; (2) simple implementation and small component count; and (3) high efficiency at light loads [1–22]. For a conventional voltage mode regulator, when the load transient happens, the system needs to wait for the next PWM switching cycle to make a correction; however, for COT architecture, the response is almost instantaneous. In general, COT control can be implemented in different ways. Output voltage ripple and internal or external generated ramp can be used to generate a PWM signal [6, 7, 9, 10, 13–15, 16, 18–20, 22]. In Figure 1(a), a conventional ripple-based COT regulator is presented [1, 2]. The control loop is very simple with the output ripple voltage directly fed back and compared with a fixed reference voltage. The output of the comparator is used to trigger a new PWM cycle. The “On-time,” Ton, is generated through a timer whose duration is a function of the input and output voltages. Unfortunately, this simple output voltage ripple-based control is susceptible to jitter and subharmonic oscillations due to the phase lag of the output capacitor voltage ripple with low ESR output capacitors. For POL applications, the output capacitance usually can reach several hundred µF, while the output voltage ripple is only several millvolts. This requires the PWM trig comparator to have an ultra-fast response and sensitivity. Utilizing external circuitry to inject artificial inductor current ramp information into the voltage feedback path is the most common method to eliminate jitter and subharmonic oscillations. As shown in Figure 1(b), additional inductor current information is introduced by adding an inductor current ramp to increase current feedback strength and reduce the influence of the capacitor voltage ripple. Note that the inductor current feedback changes the output feedback impedance, resulting in undesirable output voltage droop. Another drawback of this ramp injection technique is the low-noise tolerance due to the high sensitivity of current sensing. Moreover, as the current ramp is used for PWM generation, cycle by cycle current sensing is required. This adds system design complexity and additional challenges for integration.
Figure 1  (a) Output voltage ripple-based COT-controlled buck converter; (b) COT-controlled buck converter with inductor current ramp added; (c) COT-controlled buck converter with internal ramp added

The second method of adding internal ramp (see Figure 1(c)) is widely used in industry. The internal ramp is added to the output capacitor ESR ripple during off-time durations, thereby reducing the feedback delay of the output capacitor voltage ripple. Several published papers analyse the stability criterion and subharmonic impacts of this COT regulator technique. The approach in [13–16] derives the critical stability point of the COT regulator and the effect of the compensated ramp based on time domain analysis. However, it can only predict critical stability conditions while the design guidelines ensure stability margins cannot be provided using this approach. An accurate model used in [17–19] for stability analysis is developed in the frequency domain by calculating the closed-loop response. This is done by injecting a small sinusoidal perturbation into the control input and calculating the mathematical transfer function between the output voltage and the control input. Note that typically the control input is not accessible outside the POL IC, and this approach cannot be used for practical stability measurements. Therefore, it is important to derive an open-loop small signal model for constant on-time control stability analysis to understand the effect of the compensating ramp.

Although constant on-time control has extensive applications in industry due to its fast transient response, easy implementation, and high efficiency at light loads, conventional COT regulators have poor output voltage regulation accuracy. As mentioned above, conventional constant on-time implementations are reliant on the output voltage ripple, which can be smaller in magnitude than the environmental noise floor, especially when low ESR ceramic output capacitors are utilized, resulting in PWM jitter.

A novel constant on-time control technique is proposed, to reduce the dc offset of output voltage regulation while offering fast transient response with reduced jitter sensitivity when using ceramic capacitors. An extensive investigation of this novel constant on-time control system is demonstrated, including derivation of an open-loop small signal model enabling stability analysis.

The paper is organized as follows: In Section 2, a constant on-time control strategy with improved output regulation accuracy is proposed and supported with a small signal model and loop analysis. Section 3 presents SIMPLIS simulation verification results with small signal characteristics of the proposed control architecture. Section 4 shows the experimental verifications on the proposed control strategy and the small signal model. Finally, conclusions are provided in Section 5.

2 | PROPOSED CONTROL STRATEGY AND ANALYSIS

Figure 2 shows the circuit diagram of the proposed control scheme, where Q1 and Q2 represent two power MOSFETs, L is the output inductor, Cout is the output capacitor, Resr is the output capacitor equivalent series resistance (ESR), and Rload represents the system load. From the diagram, there are several differences compared to other constant on-time control methods. First, note that there is a ramp floor amplifier circuit (A1), which regulates the floor of the ramp. The internal ramp can boost up the signal-to-noise ratio, which helps the comparator C1 to generate the PWM_trig signal without a large Vout ripple. The accuracy of the circuit is dominated by this Ramp floor generation amplifier, A1. Compared to the traditional hysteresis comparator based on COT architecture, the accuracy of the
output voltage can be achieved more easily because both comparator and amplifier have input referred offset, which can be more than 10 mV over different process corners. The auto zeroing technical for the non-linear hysteresis comparator is more complex compared to a linear amplifier regulator. Moreover, as there is a compensation loop around the A1, the DC gain can be designed large, which ensures output voltage accuracy.

The second difference to notice is the output voltage is sensed directly without the use of a resistor divider, which can impact system loop performance when considering gains and parasitic nodal capacitance. In this proposed design, the output voltage is sensed by the analogue front-end stage (AFE), generating a signal called Error_sig, which is the sum of \( V_{\text{ref}} \) and the regulation error. The output voltage feedback is also provided to a compensation block for the generation of a floor voltage of an artificial ramp. The COT comparator, C1, compares the generated internal ramp signal to the Error_sig to initiate a new cycle of a COT PWM. When the output voltage changes due to the load transient or input voltage variation, the duty cycle changes immediately since the control modulator directly senses the output error signal at comparator C1. Because the Error_sig is directly used to generate the PWM signal, it should exhibit very fast transient response without delays from high order compensation networks and PWM clock timing latencies. Figure 3 shows the typical waveforms of the proposed constant on-time control. The red curve is Error_sig, which is compared against the blue ramp signal that is referenced to the green ramp floor signal, while the purple trace represents the resulting PWM signal. The PWM signal is produced with a fixed on-time every time the Error_sig falls below the ramp signal. The high side switch remains on until the fixed on-time expires, after which the high side switch remains off until a minimum off-time expires and the signal Error_sig falls below the ramp again. The minimum off-time is introduced to limit the maximum operating frequency during extended low Error_sig events.

During a transient load release, the ramp floor signal reduces inversely to the output voltage overshoot, resulting in increased off-time durations and reduced switching frequency. Conversely, a transient load step increase results in an initial output voltage decrease, which is corrected by the ramp floor signal increase such that the off-time decreases, thereby transferring more energy to the load to correct the output voltage decrease. The maximum switching frequency during this type of transient response is based on the minimum off-time setting. For example, because the load step is large with maximum slew rate, the drop of the Error_sig may cause the Ramp floor to increase to the level of the Error_sig or even above. During this condition, the switching period is only a function of fixed Ton time plus the preset minimum off-time. For applications with 12 V input voltage and 1.2 V output voltage programmed at 800 kHz steady state switching frequency, if the minimum off-time is set to be around 200 ns, the maximum frequency can reach 3 MHz. The minimum frequency during transient condition depends on the step of load drop step and its slew rate. There is an internal clamp level of the ramp voltage. During a large and fast load drop condition, the voltage difference between Error_sig and Ramp floor will increase beyond the internal ramp clamp level, there should be no PWM pulse during this condition (refer to Figure 3).

Figure 4 provides a detailed view of the Ramp_floor voltage generation circuit block, which utilizes a voltage mode amplifier with feedback circuitry, \( R_{f1}-R_{f5} \) and \( C_{f2} \), used to optimize stability of the floor amplifier. The circuit in Figure 4 is a zoomed in version of amplifier A1 and its peripheral components shown in Figure 2. A programmable zero is introduced to the circuit.
for stability purpose. For simplicity, $R_{i6}$ and $C_{i1}$ are used to represent the zero point. The transfer function of this circuit is derived as follows:

$$\hat{I}_{\text{Ramp}_{\text{floor}}} = \frac{R_{i5} (1 + R_{i6} C_{i2} s) + [(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5}] C_{i2} s}{[(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5}] C_{i1} s + R_{i1} (1 + R_{i4} C_{i1} s)} (1 + R_{i6} C_{i2} s)$$  (1)

$$f_{p1} = \frac{1}{2\pi R_{i6} C_{i2}}$$  (2)

$$f_{p2} = \frac{R_{i1}}{2\pi [(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5} + R_{i1} R_{i4}]} C_{i2}$$  (3)

$$f_{z1} = \frac{1}{2\pi R_{i6} C_{i1}}$$  (4)

$$f_{z2} = \frac{R_{i5}}{2\pi [(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5} + R_{i1} R_{i4}]} C_{i2}$$  (5)

The transfer function is shown in Equation (1), and the pole and zero locations are shown in Equations (2–5). By programming the values of resistors and capacitors, the transfer function can be tuned to have a large dc gain but a weak ac response. The purpose of this response characteristic is to ensure the output voltage accuracy with high dc gain, while the low ac gain can prevent the output voltage ripple from being amplified and accompanied on the Ramp_floor signal. Since there is no output feedback resistor divider, the second zero can be tuned to the frequency range around the system crossover frequency, which will boost the overall phase margin of the voltage regulator.

$$\hat{T}_s = \frac{C_{\text{ramp}}}{I_{\text{ramp}} (\hat{I}_{\text{Error}_{\text{sig}}} - \hat{I}_{\text{Ramp}_{\text{flat}}})} = \frac{C_{\text{ramp}}}{I_{\text{ramp}}} \hat{I}_{\text{Error}_{\text{sig}}} \left\{1 + \frac{R_{i5} (1 + R_{i6} C_{i2} s) + [(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5}] C_{i2} s}{[(R_{i1} + R_{i5}) (R_{i2} + R_{i3}) + R_{i1} R_{i5}] C_{i1} s + R_{i1} (1 + R_{i4} C_{i1} s)) (1 + R_{i6} C_{i2} s)} \right\}$$  (7)

Error_sig voltage is around 600 mV if the output voltage is equal to the target. During transient conditions, or any situation that output voltage is deviated from the target value, the variation of Ramp_floor shows an opposite trend compared to that of the Error_sig voltage. When the output voltage is higher than the target value, the Error_sig voltage will increase. At the same time, the Ramp_floor voltage will decrease, as regulated by the voltage amplifier A1 with feedback circuit. This will reduce the switching frequency and deliver less energy to the output. The transfer function of this ramp generation circuit is derived as shown in the following equations:

$$V_{\text{Ramp}_{\text{floor}}} + \frac{I_{\text{ramp}}}{C_{\text{ramp}}} T_s = V_{\text{Error}_{\text{sig}}}$$  (6)

As shown in the Figure 5, the Ramp is generated based on the Ramp floor signal, and the added signal is used to compare with Error_sig in order to trig a new PWM pulse. The switching period can be derived in Equation (6). This steady-state equation along with Equation (1) can be used to derive a small signal model between the switching period $T_s$, $V_{\text{Ramp}_{\text{floor}}}$, and Error_sig.

$$V_{\text{Error}_{\text{sig}}} = V_{\text{out}} - \text{VID} + V_{\text{ref}}$$  (8)

Figure 5 illustrates the ramp waveform. The ramp is generated through a fixed current $I_{\text{ramp}}$ charging ramp capacitor $C_{\text{ramp}}$. This ramp sits on Ramp_floor voltage and is compared to Error_sig voltage. At the trig of each PWM cycle, the ramp will be reset. In steady-state operation, the Ramp_floor signal should always be around 50 mV below the Error_sig. The

$$\hat{T}_{\text{Error}_{\text{sig}}} = \hat{T}_{\text{out}}$$  (9)

$$D = \frac{T_{\text{on}}}{T_s}$$  (10)

By definition, duty cycle is a function of $T_{\text{on}}$ and $T_s$, so the small signal model is derived with combination of
is presented in Figure 6. The overall control open loop has four small signal model of the proposed constant on-time control as follows: input voltage

Equation (7).

Equations (6–11) show the transfer functions of the internal ramp generation circuit. Aligning with Equations (1–5), the small signal model of the proposed constant on-time control is presented in Figure 6. The overall control open loop has four poles and three zeroes. The term \( c^{\Delta T_{\text{off}}} \) does not affect the magnitude, representing the leading phase characteristic of constant on-time control.

For a conventional COT converter, bode plot open loop gain/phase measurements may lead to inaccurate results and incorrect stability conclusion because the injected small signal can disturb the output ESR ripple and affect the dc operation point. Therefore, the small signal models published for COT regulators are developed by calculating the control to output transfer function, which is a closed-loop analysis. Unfortunately, the control signal is typically not accessible outside the IC chip, so these models are not practical methods to evaluate the loop stability for engineers. Unlike the conventional COT control, the proposed COT method separates the ramp from the output feedback signal. As shown in Figure 7, the input and output of this control block are \( V_{\text{out}} \) and \( \Delta \), similar to voltage mode control. Therefore, the small signal open loop gain can be measured using classical bode plot gain/phase measurement.

3 | CIRCUIT SIMULATION

To verify the proposed COT control strategy and its small signal characteristics, the circuit simulation results are presented in the following figures. The circuit parameters are given as follows: input voltage \( V_{\text{in}} = 12 \text{ V} \), output target voltage \( V_{\text{out}} = 1.26 \text{ V} \), switching frequency \( f_{\text{sw}} = 600 \text{ kHz} \), output capacitor \( C_o = 47 \mu \text{F} \times 10 \), power inductor \( L_o = 150 \mu \text{H} \). Figure 8(a,b) shows the simulated output voltage under a load transient (15–30 A, 2.5 A/\mu s slew rate). It can be seen that the output voltage dc accuracy is within \( \pm 0.5\% \), transient undershoot is about 6.7 mV, and transient overshoot is about 11.8 mV, which is an excellent transient response behaviour. Figure 8(c,d) shows simulation results with key waveforms about ramp generation. As shown in Figure 8(c), the AFE output voltage falls below the ramp and a new fixed on-time is generated, resulting in a rise of the inductor current. If the output voltage is not recovered, the ramp floor voltage continues to rise and another on-time is generated after a minimum off-time period until the output voltage returns to the target value. In Figure 8(d), when a load release occurs, excess energy in the inductor transfers to the output capacitors, resulting in an output voltage rise. As a result, the AFE output voltage rises above the target while the ramp floor voltage reduces, resulting in a COT comparator initiation of a fixed on-time while the off-time is dynamically extended.

The load transient of the SIMPLIS simulation with the above ramp design is given in Figure 9. The purpose of using the SIMPLIS model is to verify that the systematic design is robust and to provide proof of the design concept. Compared to a cadence simulation, the SIMPLIS circuit model is focused on system stability, all the application corners for this proposed design, and the circuit parameters are the same as above. The SIMPLIS simulation results are very similar to the IC simulation results.

In order to verify the loop analysis, the small signal model and SIMPLIS simulation are compared with different output
capacitances and duty cycles. In the simulation, input voltage is 12 V, switching frequency is 800 kHz, and inductor is 150 nH. As shown in Figure 10(a–d), the proposed small signal model can accurately predict the system behaviour with different output capacitances and duty cycles at half of switching frequency. Table 1 shows the comparison of loop crossover frequency and phase margin between the SIMPLIS simulation and the model calculation with various output capacitances and duty cycles. The model matches cross over frequency and phase margin compared to the top level systematic level SIMPLIS simulation results over wide operational region.

| Output cap (µF) | Duty cycle | SIMPLIS simulation | Model calculation |
|----------------|------------|---------------------|-------------------|
|                |            | $F_c$ (kHz)         | $PM$ (°)          | $F_c$ (kHz) | $PM$ (°) |
| 470            | 0.083      | 108.2               | 52.3              | 101.5      | 56.7     |
| 470            | 0.1        | 129.7               | 57.1              | 114.6      | 72.2     |
| 470            | 0.3        | 236.8               | 53.3              | 202.2      | 76.3     |
| 910            | 0.1        | 94.7                | 44.6              | 100.3      | 75.5     |
EXPERIMENTAL RESULTS

The proposed constant on-time controller was fabricated utilizing a CMOS technology. The entire controller, including analogue front-end amplifier, ramp floor amplifier, and power MOSFETs, is integrated into a silicon power IC chip. Figure 11 shows the prototype of the COT buck converter with the proposed constant on-time control technique. The specifications of the buck converter are listed in Table 2. The measured load transient response is shown in Figure 12 with 28.5 mV undershoot and 54.6 mV overshoot during 15 A load step-up and step-down transient, respectively.

Figure 13 shows the output voltage with different load currents and input voltages. The measured output voltage is very close to the regulated target voltage (<0.3% error), showing
TABLE 3  Comparison with other studies regarding transient performance

| Specifications       | This work | Ref. [20] 2019 | Ref. [21] 2019 | Ref. [5] 2018 | Ref. [22] 2017 | Ref. [23] 2017 | Ref. [25] 2016 | Ref. [25] 2016 | Ref. [26] 2016 | Ref. [27] 2016 | Ref. [28] 2009 |
|---------------------|-----------|----------------|----------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Input voltage range (V) | 12        | 12             | 30             | 12           | 8.5           | 19            | 12            | 15            | 6             | 3.3           | 5             |
| Output voltage (V)     | 1.05      | 1.05           | 15             | 1.05         | 3.3           | 0.9           | 1.1           | 5             | 3.3           | 2.5           | 1.6           |
| Inductance (µH)        | 0.15      | 1.5            | 55             | 0.47         | 10            | 0.47          | 0.47          | 10            | 10            | 0.82          | 1.1           |
| Output Capacitance (µF) | 900      | 22             | 297            | 734          | 470           | 220           | 600           | 100           | 470           | 200           | 250           |
| Load step (A)          | 15        | 4              | 4.5            | 17Δ          | 3.2           | 10            | 5             | 3.6           | 4.85          | 5             | 8             |
| Maximum load (A)       | 40        | 5              | 6              | 17Δ          | 3.2           | 11            | 8             | 4.6           | 7             | 5.5           | 8             |
| Overshoot (mV)         | 54.6      | 36             | 150*           | 90           | 161.1         | 65            | 150           | 60            | 90*           |               |               |
| Undershoot (mV)        | 28.4      | 30             | 150*           | 40           | 17.24         | 20*           | 70*           | 150           | 40            | 60*           |               |
| Testing fsw (kHz)      | 800       | 700            | 100            | 600          | 200           | 413           | 300           | N/A           | 200           | 600           | 500           |

*The overshoot/undershoot value is not directly reported; data were extracted from reported waveforms. ΔThe test is based on two phase; total current for a two-phase circuit is 34 A, and each phase is assumed to handle 17 A load step.

FIGURE 13  Output voltage accuracy with different \( V_{in} \) and \( I_{load} \), \( V_{out} = 1.05 \) V

an excellent output voltage accuracy performance. In Table 3, the transient performance is compared with previous studies [5, 20–28]. These studies were chosen based on either similar circuit applications or similar design of architecture. Reference [26] and [28] are circuit designed for point of load application, while references [5, 20, 23, 24] and [26] are modified constant on-time circuits designed recently. The remaining studies use a hysteresis-type of architecture design, which is also suitable for fast load transient applications. Compared to other research, the proposed constant on-time circuit presented good undershoot

FIGURE 14  Verification of small signal open loop transfer function (left: silicon Bode plot measurement results; right: Mathcad model calculation): (a) \( L = 150 \) nH, \( C_{out} = 784 \) µF, (b) \( L = 150 \) nH, \( C_{out} = 1254 \) µF, (c) \( L = 82.5 \) nH, \( C_{out} = 784 \) µF, (d) \( L = 82.5 \) nH, \( C_{out} = 1254 \) µF.
FIGURE 15  Bode plot measurement: (a) high phase margin, (b) low phase margin

FIGURE 16  Experimental waveform measurement: $L = 150 \text{ nH}$, $C_{out} = 784 \mu \text{F}$, (a) SW node jitter, (b) load transient output voltage

FIGURE 17  Experimental waveform measurement: $L = 1 \mu \text{H}$, $C_{out} = 314 \mu \text{F}$, (a) SW node jitter, (b) load transient output voltage
and overshoot performance with large load step. Moreover, the load step used in this test has a 40 A/µs slew rate, which is much faster than most of the other designs, further proving the proposed design.

To verify the small signal model and loop analysis, Figure 14(a) shows the comparison with an open loop transfer function with 150 nH inductance and 784 µF output capacitance. The measurement result shows good matching with the small signal loop model. Similarly, as shown in Figure 14(b–d), there is good correlation between the small signal open loop transfer function and the experimental verification with other different power inductances and output capacitances. Table 4 exhibits the comparison of loop crossover frequency and phase margin between experimental measurement and model calculation with various output capacitance and inductance combinations.

To verify the correlation between small signal loop analysis and dynamic performance, two cases with different phase margins are shown as Figures 15–17. Figure 15 shows measured bode plots for case 1 (L = 150 nH, Cout = 784 µF, Fc = 153.9 kHz and PM = 62.7°) and case 2 (L = 1 µH, Cout = 314 µF, Fc = 90.3 kHz, and PM = 27.5°). Figure 16 shows the SW node jitter and load transient output voltage for case 1, and Figure 17 shows the SW node jitter and load transient output voltage for case 2. From the results, more SW node jitter can be discovered, and also the output voltage load transient is underdamped when the phase margin is lower, indicating the predictability of the proposed small signal model for loop stability analysis.

### 5 Conclusion

A novel constant on-time control architecture with internal ramp compensation for POL applications is proposed. In order to improve the output accuracy, a ramp floor amplifier is utilized in the control loop to correct output DC error. A small signal model of a constant on-time controlled converter based on internal ramp is described. This small signal model is developed based on open control loop techniques where the open loop gain can be validated using open loop gain/phase bode plot measurements. The simulation and experimental results verify the small signal characteristics of the constant on-time control architecture. The model accurately predicts the system behavior up to half of the switching frequency. The experimental results show very good correlation of phase margin, transient load response, and switching node jitter. The transient performance has also been compared with other relevant research studies. This proposed design presents a good overshoot and undershoot at large load step transient with fast slew rate.

### Table 4: Comparison of loop crossover frequency and phase margin at various conditions

| Output cap (µF) | Power L (nH) | Silicon Fc (kHz) PM (°) | Model Fc (kHz) PM (°) |
|-----------------|-------------|------------------------|----------------------|
| 150             | 784         | 153.9 62.7             | 155.5 69.3           |
| 150             | 1254        | 103.4 78.7             | 105.2 80.1           |
| 82.5            | 784         | 244.7 64.1             | 186.8 79.7           |
| 82.5            | 1254        | 216.4 86.3             | 192.3 90.2           |

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