Smooth Variational Graph Embeddings for Efficient Neural Architecture Search

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Abstract—Neural architecture search (NAS) has recently been addressed from various directions, including discrete, sampling-based methods and efficient differentiable approaches. While the former are notoriously expensive, the latter suffer from imposing strong constraints on the search space. Architecture optimization from a learned embedding space for example through graph neural network based variational autoencoders builds a middle ground and leverages advantages from both sides. Such approaches have recently shown good performance on several benchmarks. Yet, their stability and predictive power heavily depends on their capacity to reconstruct networks from the embedding space. In this paper, we propose a two-sided variational graph autoencoder, which allows to smoothly encode and accurately reconstruct neural architectures from various search spaces. We evaluate the proposed approach on neural architectures defined by the ENAS approach, the NAS-Bench-101 and the NAS-Bench-201 search space and show that our smooth embedding space allows to directly extrapolate the performance prediction to architectures outside the seen domain (e.g. with more operations). Thus, it facilitates to predict good network architectures even without expensive Bayesian optimization or reinforcement learning.

Index Terms—representation learning, neural architecture search, graph neural network, deep learning

I. INTRODUCTION

Recent progress in computer vision is to a large extent coupled to the advancement of novel neural architectures [1], [2]. In this context, the automated search of neural architectures [3]–[5] is increasingly important, as it removes the fatiguing and time-consuming process of manual trial-and-error network design. Neural Architecture Search (NAS) is intrinsically a discrete optimization problem and can be solved effectively using black-box methods such as reinforcement learning [4], [6], evolution [5], [7], Bayesian optimization (BO) [8]–[10] or local search [11]. However, finding a good solution typically requires thousands of function evaluations, which is infeasible without company-scale compute infrastructure. Recent research in NAS focus as well on efficient methods via continuous relaxations of the discrete search space and weight-sharing [12]–[15]. However, such methods yield efficient yet oftentimes sub-optimal results [16].

Therefore, we argue in favor of NAS on learned graph embeddings using encoder-decoder graph neural networks (GNN) [17]–[19]. Zhang et al. [20] recently showed good performance with such a model, D-VAE, on the ENAS search space [13] in neural architecture performance prediction and BO - proving its ability to learn smooth continuous graph representations. D-VAE aggregates information in the architecture GNN alternatingly in the forward pass and in the backward pass to encode the neural network information flow. However, the D-VAE model imposes strong constraints on the graph structure, which limit its applicability to search spaces beyond ENAS. In addition, it has very long training times. In this paper, we propose a two-sided variational encoder-decoder GNN to learn smooth embeddings in various NAS search spaces, which we call Smooth Variational Graph embedding (SVGe). In contrast to D-VAE, SVGe aggregates node representations in the forward and backward pass separately and consequently decodes their joint representation into forward and backward pass separately (see Fig. 1). This yields a very high reconstruction ability without imposing any constraints on the search space and allows for a more efficient training.

Inheriting from variational autoencoders [21], it places structurally similar graphs close to one another in the embedding space and thus facilitates efficient black-box optimization to find high-performing architectures. The proposed model is not only three times faster than D-VAE but also shows improved BO results on the ENAS search space. In contrast to D-VAE, it can be directly applied to other search spaces.
such as NAS-Bench-101 [22] and NAS-Bench-201 [23].

Moreover, it allows to learn architecture performance prediction in a supervised way and extrapolate from the space of observed architectures at test time. This way, high performing architectures even outside of the original search space can be proposed at very low costs.

In summary, we make the following contributions: (i) We introduce a novel graph variational autoencoder, SVGe, that builds a structurally smooth variational graph embedding by learning accurate representations of neural architectures (Sec. III-A and III-B). (ii) We discuss theoretical properties of our approach (Sec. III-D). (iii) We conduct extensive evaluations on the ENAS [13], NAS-Bench-101 [22] and NAS-Bench-201 [23] search spaces and show that our approach allows for competitive BO results in all three search spaces. Our experiments show that SVGe is able to extrapolate to larger unseen architectures. It finds an architecture with a best accuracy of 95.18% when learning from the NAS-Bench-101 search space. This improves over the best architecture within this space. In addition, our top 1 found architecture improves over comparable architectures in terms of validation and test accuracy, when transferring to ImageNet16-120 [24] (Sec. IV).

II. RELATED WORK

a) Graph Generative Models.: Recent years have shown huge progress in representation learning for graph-based data with Graph Neural Networks (GNNs) [18], [25]–[27]. GNNs follow a message passing scheme, where node feature vectors aggregate information from their neighbors [28] and capture local structural information. To obtain a graph-level representation these feature vectors are pooled [29]. GNNs differ in their neighborhood node information as well as in their graph-level aggregation procedure [18], [25], [27], [30]–[33]. Graph generation can be addressed globally by relaxing the adjacency matrix [34], [35] or sequentially by adding nodes and edges alternately using recurrent networks [36], [37] or GNNs [38]. Our decoder model is similar to [38] in the aggregation procedure. Yet, while [38] treat forward and backward pass equally, our model aggregates node information for both separately to account for the order of network operations and the information flow. Zhang et al. [20] propose a less efficient, alternating message passing scheme for this purpose and reinstall the validity of decoded architectures using a heuristic which employs prior knowledge on the search space. The proposed method differs in both encoder and decoder. Our encoder employs an efficient bi-directional model and the proposed bi-directional decoding facilitates highly accurate reconstructions without constraining the search space.

b) Neural Network Performance Prediction.: Predicting the performance of neural networks based on features such as the network architecture, training hyperparameters or learning curves has been exploited previously via MCMC methods [39], Bayesian neural networks [40] or regression models [41], [9] and [42] manually construct features to regress neural networks or support vector regressors.

More recent work utilizes GNN encodings by adapting message passing to simulate operations in either edges or nodes in the graph [43] or using a semi-supervised approach by training GNNs on relation graphs in the latent space [44]. [45] train a GNN surrogate performance prediction model and show the ability of zero-shot performance prediction.

c) Neural Architecture Search via Bayesian Optimization.: To apply Bayesian Optimization (BO) for NAS, high dimensional and discrete architecture configurations need to be embedded into continuous search spaces. [8] use a distance metric obtained through an optimal transport program to enable Gaussian process (GP)-based BO. [9] encode architectures with a high-dimensional path-based scheme and employ BO on an ensemble surrogate. [10] propose a graph kernel with GP-based BO to capture the topological structure of architecture graphs. GNN-based encodings have been used in [20], [46] to fit a Bayesian linear regressor as a surrogate in BO. Very recently, Yan et al. [47] learn neural architecture representations using [33] in combination with a multilayer perceptron graph decoder. The model employs a combination of the adjacency matrix and a one-hot operation encoding matrix as input for the encoder and improves over previous approaches to NAS though. Their results indicate that highly informed encoding is crucial for the task. Our model focuses on learning an accurate architecture mapping into a smooth latent space using GNNs. It allows competitive performance to highly optimized approaches using BO [47]. Due to its smoothness, it can further directly extrapolate the performance prediction outside the space of seen architectures and thus to propose high-performing, deeper networks without using BO.

III. STRUCTURAL GRAPH AUTOENCODING

We aim to learn a structurally smooth latent representation of neural network architectures, which we cast as directed acyclic graphs (DAGs) with nodes representing operations (like convolution or pooling) and edges representing information flow. This enables to (i) accurately predict the accuracy of an unseen graph from training samples and (ii) draw new samples which are structurally similar to previously seen ones.

Our model is a variational autoencoder (VAE) [21]. First, the VAE encoder \( q_\phi(z|G) \) maps the input data \( G \) (a finite number of i.i.d. samples from an unknown distribution) onto a continuous latent variable \( z \) via a parametric function \( q_\phi \). Then a probabilistic generative model \( p_\theta(G|z) \) (the decoder) decodes the latent variables \( z \) to the original representation. The parameters \( \phi \) and \( \theta \) of the encoder and decoder are optimized by maximizing the evidence lower bound (ELBO):

\[
\mathcal{L}(\theta, \phi; G) = \mathbb{E}_{q_\phi(z|G)} \left[ \log p_\theta(G|z) \right] - \text{KL} (q_\phi(z|G)\|p(z))
\]

(1)

where the first term is the reconstruction loss and enforces high similarity between input data and generated data, while the second term is the Kullback-Leibler divergence which regularizes the latent space. From the trained VAE, new data can be generated by decoding latent space variables \( z \) sampled from the prior distribution \( p(z) \).
Below, we provide details on the proposed GNN encoder and decoder models. For NAS, we have to pay particular attention to isomorphic graphs. As they are functionally identical yet represented via distinct adjacency matrices, it is not obvious to guarantee a correct mapping and unique decoding. Motivated by [33] (see Sec. III-D), we chose our model to allow for injective encoding and unique decoding.

A. Encoder

Here, we describe the encoder of our GNN-based SVGe. Let $G = (V, E)$ be a directed acyclic graph, with nodes $v \in V$ and edges $e \in E$. Each node $v$ has an initial node feature embedding $h_v^{(0)}$. Standard GNNs can be seen as a two-step procedure. In the first step the GNN learns a representation for each node $v \in V$, by iteratively aggregating the representations of neighboring nodes using an aggregation function $\mathcal{A}(\cdot)$. Then it updates the representation with the update function $\mathcal{U}(\cdot)$. After $K$ rounds of iterations, the final representation of each node $v$ is computed. The second step computes a graph representation $h_G$ by aggregating the node representations.

Since our objective is to learn a structurally smooth graph representation, we need to capture the structure and the information flows of the graphs. Thus, our model consists of two encoding modules, where the messages are passed in the direction of the network’s forward pass in the forward encoder (green) and in the direction of the back-propagation in the backward encoder (red) visualized in Fig. 1 (left). Our variant of GNN formulates the aggregation function $\mathcal{A}(\cdot)$ as the sum of node message passing modules and uses a single gated recurrent unit (GRU) [48] as the update function $\mathcal{U}(\cdot)$ for both forward and backward encoder. The forward message passing module $\overrightarrow{f}(\overrightarrow{h}_u^{(k)}, \overrightarrow{h}_v^{(k)})$ computes a message vector from node $u$ to node $v$ in the $k$-th iteration, while $\overleftarrow{f}(\overleftarrow{h}_v^{(k)}, \overleftarrow{h}_u^{(k)})$ is the backward message passing module from node $v$ to $u$, with $h_v^{(k)}$ being a feature vector representation of node $v$ at iteration $k$. Each graph information direction is aggregated individually:

$$\overrightarrow{a}_v^{(k)} = \sum_{u \in \mathcal{V}^{\text{in}}(v)} \overrightarrow{f}(\overrightarrow{h}_u^{(k-1)}, \overrightarrow{h}_v^{(k-1)})$$

$$\overleftarrow{a}_v^{(k)} = \sum_{u \in \mathcal{V}^{\text{out}}(v)} \overleftarrow{f}(\overleftarrow{h}_v^{(k-1)}, \overleftarrow{h}_u^{(k-1)}),$$

where $\mathcal{V}^{\text{in}}(v) = \{ u \in V \mid (u, v) \in E \}$ is the set of adjacent nodes to $v$ in the DAG, specifying the network input to $v$ during inference and $\mathcal{V}^{\text{out}}(v) = \{ u \in V \mid (v, u) \in E \}$ are the adjacent nodes to $v$ in the networks backward pass, i.e. in the DAG with reversed edges. Also, instead of using one-hot encoded node labels, we employ a learnable embedding table $L_e$ on the node types, which stores embeddings (feature vectors) for our initial node embeddings $\overrightarrow{h}_v^{(0)}$, $\overleftarrow{h}_v^{(0)}$. The functions $\overrightarrow{f}$ and $\overleftarrow{f}$ are implemented using a single fully connected layer (fc). After the final iteration, we combine the forward and backward node embeddings $(\overrightarrow{h}_v^{(K)})_{v \in V}, (\overleftarrow{h}_v^{(K)})_{v \in V}$ of node $v$ by concatenation:

$$(h_v^{(K)})_{v \in V} = \left(\text{CONCAT}(\overrightarrow{h}_v^{(K)}, \overleftarrow{h}_v^{(K)})\right)_{v \in V}.$$  

By combining these two information sets, we capture not only the topology but also the information paths in the graph.

From the node representations, we compute a graph representation using a gated sum:

$$h_G = \sum_{v \in V} \phi(h_v^{(K)}) \odot \psi(h_v^{(K)}),  \quad (4)$$

with the sigmoid activated fc layer $\phi = \sigma(\text{fc}(\cdot))$ as a gating function, the linear activated fc layer $\psi$, and $\odot$ denoting the Hadamard product. Since we use this encoder in a variational autoencoder setting, we add an extra graph aggregation layer equal to (4) to obtain $h_G^{var}$. Thus, the outputs of our encoder are the parameters of the approximate posterior distribution $q_\phi = \mathcal{N}(h_G, \Sigma)$, with $h_G$ being the mean and $h_G^{var}$ the diagonal of the variance-covariance matrix $\Sigma$ of the multivariate normal distribution. Sec. III-D discusses the properties of this encoder w.r.t. injectivity and isomorphic graphs.

B. Decoder

The SVGe decoder $p_\theta(G|z)$ takes a latent point $z$ as input and reconstructs $G$ simultaneously from two directions (start-to-end and end-to-start node), see Fig. 1 (right). As in the encoder, the model explicitly learns a neural architecture’s forward and backward pass, allowing for highly accurate reconstructions of graphs without “loose ends”. The directional graph generation starts from the input node $v_0$ for forward decoding and the output node $v_T$ for backward decoding. Each graph is built iteratively in a sequence of operations that add nodes and edges until the end node is generated, similar to [20]. The union of both, forward and backward graph, builds the output graph.

1) Directional Decoding: The directional graph generation starts from an initial node with type “InputType” for the forward decoding and with type “OutputType” for the backward decoding. The input node and all generated nodes $v_t$ are embedded according to the initNode module:

$$h_t = f_{\text{initNode}}(z, h_{G(t)}, \text{Ld[type]}),  \quad (5)$$

with $f_{\text{initNode}}$ being a two-layer fc with ReLU activation. It takes as input the sampled point $z$, the partial graph embedding $h_{G(t)}$ and the learned node type embedding $\text{Ld[type]}$. If the node $v_t$ is either the input or the output node, Eq. (5) simplifies to $h_t = f_{\text{initNode}}(z, \text{Ld[type]}).$ Given the start node $v_0$, its embedding $h_0$ and the partial graph embedding $h_G = z$, a graph is generated by iterating over a sequence of modules whose weights are shared across iterations until an end node, e.g. of type OutputNode in the forward decoder, is drawn.

In every iteration, a new node is created and added to the graph and its node type (i.e. operation in the network architecture) is selected by the addNode module. It takes as input the representation of the partial graph $h_{G(t)}$ and the sampled point $z$ and determines the next missing node

$$\text{NodeType} \sim \text{Categorical}(s^{(t+1)}_{\text{addNode}}), \quad (6)$$

where

$$s^{(t+1)}_{\text{addNode}} = f_{\text{addNode}}(z, h_{G(t)}). \quad (7)$$
distribution with diagonal covariance structure. This can be
approximated by a multivariate Gaussian
form of the
edge losses over all iterations for both decoding directions;
\( G \) does not accumulate throughout iterations. To compute the overall
loss \( L \) to compute a node-level loss
(Eq. (8)) during training. We use this ground truth
of the outputs of
the DAG, which we discuss in Sec. III-D, we know the
embedding \( h \)
of a node, which is again a two-layer fc layer with ReLU activation.

After adding the edges, the concatenated node embeddings
\( h \) are aggregated and updated in the
module (Eq. (5)) and
an edge-level loss
(Eq. (8)) during training. We use this ground truth to compute a node-level loss \( L \) and an edge-level loss \( L' \) at each iteration \( t \). Additionally, we replace the model output by the ground truth such that possible errors will not accumulate throughout iterations. To compute the overall reconstruction loss for a graph \( G \), we sum up node losses and edge losses over all iterations for both decoding directions;
\( L_{rec} = L_{V} + L_{E} \) and \( L'_{E} \). Following [21], we assume the posterior by a multivariate Gaussian distribution with diagonal covariance structure. This can be written as log \( g_{\phi}(z|G) = \log \mathcal{N}(z; h_{G}, \Sigma) \) and ensures a closed form of the KL divergence
\[
D_{KL} = -\frac{1}{2} \sum_{j=1}^{J} \left( 1 + \log(h_{G}^{var})_{j} - (h_{G})_{j}^{2} - (h_{G}^{var})_{j} \right). \tag{9}
\]
Thus, the overall loss from Eq. (1) becomes:
\[
L = L_{rec} + \alpha D_{KL}. \tag{10}
\]
Following [49] and [20], we set \( \alpha = 0.005 \).

D. Discussion on Theoretical Properties

In the following, we discuss SVGe in the context of
isomorphic input graphs. Intuitively, if isomorphic graphs, i.e. graph representations of the same neural architecture, are mapped to distinct latent points, the latent space is intrinsically
redundant. This hampers an efficient embedding of structural similarity. Conversely, if non-isomorphic graphs are mapped to the same latent point, their performance can neither be correctly predicted nor their structure reconstructed. Thus, a suitable graph encoder has to map any two isomorphic graphs to the same latent point (ISO). A suitable decoder decodes each latent point to a unique graph and preserves the difference between non-isomorphic graphs (INJ).

a) Unique Latent Space Representation.: Here, we discuss the proposed SVGe encoder w.r.t. properties (ISO) and (INJ). Theorem 3 in [33] gives sufficient conditions on injectivity (INJ) of the GNN’s node aggregation module and its update module. However, the required existence of an appropriate injective aggregation function operating on multisets can only be guaranteed theoretically on countable input feature spaces. Even then, [33] gives no explicit construction but they argue that it can be approximated via MLPs. Thus, we verify empirically that SVGe maps isomorphic graphs to the same embedding (ISO) in an experiment on 11,606 isomorphic graph pairs of length 7 from the NAS-Bench-101 search space. 100% of such isomorphic pairs were mapped onto the same point. The mapping of distinct graphs to distinct latent representations (INJ) is a prerequisite for accurate reconstruction and therefore validated in the reconstruction ability in Sec. IV-A.

b) Decoding from the Latent Space.: We now discuss how the decoder handles isomorphic DAGs w.r.t. (INJ). Since isomorphic graphs are mapped onto the same latent point by the encoder (see above), it suffices for the decoder to decode them uniquely, i.e. deterministically. It can be easily seen that this is the case for SVGe. Yet, how can the decoder be trained efficiently to decode one out of several isomorphic graphs from the same latent point, when decoding graph \( G_1 \) instead of an isomorphic graph \( G_2 \) leads to significant reconstruction loss? Isomorphic graphs can be created from one another by permuting nodes in the adjacency matrix. Thus, to ease the decoder into the learning process we bring the graphs in a unified form. Towards a unique representation, we limit the training data to upper triangular matrices. The remaining isomorphic graphs are removed from the training set as in [22], since we need a unique representation for each graph. Note, this only removes duplicate architectures. For the ENAS and the NAS-Bench-201 search space, the adjacency matrices are unique, given the upper triangular representation.

Given such clean training data, the choice of the VAE decoder is still crucial. For good reconstruction from the latent space, we introduce a two-sided decoder, which captures the information flow from the input to the output node and vice versa. Specifically, nodes generated in the forward pass that are not connected to the output are connected to their predecessor in the backward decoder, and vice versa. The union of both forward and backward decoded graphs will therefore likely contain all missing edges from both single decoders. D-VAE [20] overcomes this problem of possible trailing nodes by incorporating a heuristic “post-processing” step employing prior knowledge on the search space: It connects each non-output node with out-degree zero to the output node.
IV. Experiments

We evaluate the proposed SVGe on three different, commonly used search spaces from the NAS literature.

a) NAS-Bench-101: NAS-Bench-101 [22] is a tabular benchmark that consists of a cell-structured search space containing 423k unique architectures evaluated for 4, 12, 36 and 108 epochs on the CIFAR-10 image classification task. The cell structure is limited to a number of nodes $|V| \leq 7$ (including the input and output node) and edges $|E| \leq 9$. The nodes represent an operation from the operation set $O = \{1 \times 1 \text{conv.}, \ 3 \times 3 \text{conv.}, \ 3 \times 3 \text{max pooling}\}$. In our experiments, we use 90% of the 423k (architecture, accuracy) pairs as training examples and 10% as validation ones.

b) ENAS Search Space: The ENAS [13] search space consists of architectures represented by a DAG with $|V| = 8$ nodes (including the input and output node) and 6 operation choices on each of the non-input and non-output nodes. As [20], we sample 19,020 architectures from this space.

c) NAS-Bench-201: NAS-Bench-201 [23] is a tabular benchmark, employing a cell-structured search space, with 15,625 unique, sampled architectures trained and evaluated on CIFAR-10, CIFAR-100 and ImageNet-16-120 [24] for image classification. NAS-Bench-201 differs from NAS-Bench-101 in the cell representation: the nodes represent the sum of feature maps and the edges represent an operation from $O = \{1 \times 1 \text{conv.}, \ 3 \times 3 \text{conv.}, \ 3 \times 3 \text{avg pooling}, \text{skip, zero}\}$. The DAG representing a NAS-Bench-201 architecture has $|V| = 4$ nodes and $|E| = 6$ edges.

While the NAS-Bench-101 benchmark provides the true performance of all fully trained architectures, ENAS does not provide any such value. Therefore, we use the weights of the optimized one-shot model as a proxy for the validation/test performance of the sampled architectures during optimization. We split the (architecture, accuracy) pairs into 90% training and 10% test examples. On NAS-Bench-201, we evaluate abilities of the proposed autoencoder and show the transferability of our BO and extrapolation results.

After testing its autoencoder abilities, we evaluate SVGe on performance prediction, Bayesian optimization and search space extrapolation. In all our experiments, we set $h \in \mathbb{R}^{250}$ for the concatenated node dimension and $h_G \in \mathbb{R}^{36}$ for the latent space dimension. All the algorithms and routines are implemented using PyTorch [50] and PyTorch Geometric [51].

$¹$We provide our implementation at https://github.com/jovitalukasik/SVGe

A. Autoencoder Abilities.

Following previous work [20], [49], we evaluate SVGe by means of reconstruction accuracy, validity, uniqueness and novelty. We evaluate these abilities on the ENAS, NAS-Bench-101 and NAS-Bench-201 search spaces and compare to [20] and [47]. As an ablation on ENAS, NAS-Bench-101 and NAS-Bench-201, we also adapted the generative model from [38], DGMG, as a VAE with a single decoder to assess our encoder architecture. We train the models on 90% of the dataset and test it on the 10% held-out data.

Table I shows the results. D-VAE [20] and all our model variants show reasonable performance w.r.t. the reconstruction accuracy, on ENAS. On NAS-Bench-101 and 201, our approaches perform equally well and are comparable to arch2vec [47], while D-VAE performs poorly on NAS-Bench-101 and diverges on NAS-Bench-201. We hypothesize that D-
VAE’s hard constraints on the graph decoding are not suitable for NAS-Bench-101 and NAS-Bench-201. The resulting latent space cannot capture all relevant information.

The validity measures how many of the decoded samples are valid DAGs. Again, we see good overall performance on ENAS. On NAS-Bench-101 SVGe, DGMG and D-VAE perform comparably, while the validity for arch2vec is low, indicating that their decoder is not suited for graph generation. This trend is less severe yet observable on NAS-Bench-201.

The uniqueness ability measures the unique share of the valid decoded graphs. We argue that it can be seen as a measure for the latent space smoothness, which is particularly important for any kind of extrapolation from the training data. If the uniqueness is small, distinct and potentially distant latent points are decoded to the same output. This indicates that the latent space is heavily folded and non-smooth. While all approaches could be improved w.r.t. uniqueness, SVGe performs better than previous models.

The novelty indicates the portion of graphs from the valid graph set which have not been observed during training. Here, values on ENAS are high and non-informative since only a small portion of the search space is covered by training data. On the two NAS-Bench variants, D-VAE and our models perform on par while the numbers for arch2vec are higher. The direct comparison of these values is impaired since arch2vec issues an overall lower number of valid graphs.

We conclude that SVGe shows the best trade-off between accuracy, validity and uniqueness over all three search spaces.

B. Latent Space Smoothness Observations

In Fig. 3 and 2, we visualize the smoothness of the SVGe graph embedding in the NAS-Bench-101 search space. Fig. 3 (left) visualizes the SVGe embedding. We plot equidistant points within a $[-0.3, 0.3]$ grid, given a 2D subspace of our training data with a validation accuracy above 75% spanned by the first two principal components. Architectures with similar accuracies are close to each other and high accuracy architectures form clusters. Fig. 2 shows a unit circle in a randomly chosen orthogonal direction in the SVGe embedding space. We start from a flat net encoding in the latent space and randomly pick 14 equidistant datapoints along the hypersphere returning to the start point. These datapoints are decoded and visualized as architectures. As one can see they change smoothly with changing only few operations and edges at each step.

### TABLE II

| Method | 1,000 | 10,000 | 100,000 |
|--------|-------|--------|---------|
| Assess. [44] | 0.0031 ± 0.0003 | 0.0026 ± 0.0002 | 0.0016 ± 0.0002 |
| D-VAE [20] | 0.0039 ± 0.0003 | 0.0026 ± 0.0002 | 0.002 ± 0.001 |
| DGMG [38] | 0.0037 ± 0.0001 | 0.0027 ± 0.0001 | 0.0022 ± 0.0001 |
| SVGe | **0.0026** ± 0.0002 | **0.0023** ± 0.00004 | **0.002** ± 0.0003 |

### TABLE III

| Method | Test Acc.(%) | Val Acc.(%) | Runtime |
|--------|-------------|-------------|---------|
| ENAS | D-VAE [20] | 94.80 | - | 16 |
| SVGe | **95.11** | - | **5** |
| NB101 | DGMG [38] | 93.51 | 94.08 | - |
| SVGe | 93.88 | 94.60 | - |

C. Performance Prediction from Latent Space

Next, we evaluate SVGe in terms of performance prediction on NAS-Bench-101 architectures. This allows for direct comparison to the recent work [44]. We train SVGe on 90% of all 423k datapoints in NAS-Bench-101 for reconstruction to obtain the latent space. Then, we fine-tune the unsupervised trained model for performance prediction using a regressor, which is a four-layer MLP with ReLU non-linearities. The SVGe model and the regressor are trained jointly for performance prediction on 1/10/100k randomly sampled architectures with test accuracies from NAS-Bench-101. For comparison we also train D-VAE and DGMG in the same setting. We compare the ability to predict performances accurately on the validation set. Table II shows the MSE, which denotes the empirical squared loss between the predicted and ground truth data, and the standard deviation of 3 runs.

Our proposed SVGe has a slightly lower MSE compared to [44], which focuses precisely on this subproblem, when few annotated datapoints are given. This is important in particular for NAS, since every training sample corresponds to a fully evaluated architecture and is thus expensive. D-VAE and DGMG show high MSE for this small amount of training data. We expected this behavior for D-VAE because it already showed poor abilities in Sec. IV-A on NAS-Bench-101. The low prediction accuracy for DGMG hints to potential overfitting in the autoencoder. In Fig. 3 (right), we plot the performance prediction ability of our model trained on 1k sampled architectures from Table II for high-performing architectures (above 80% test accuracy). This shows a strong correlation between predicted and true accuracies.

D. Bayesian Optimization

We have seen in the previous experiments that the proposed SVGe generates a latent space which enables to interpolate from seen labels/performances and outperforms D-VAE and DGMG significantly. Next, we perform NAS via BO in the ENAS search space, in order to allow a fair comparison to D-VAE [20] by exchanging only the D-VAE generative model with our SVGe and using exactly the same setup as in [20]. We perform 10 iterations of batch BO (with a batch size of 50) and average the results across 10 trials based on a Sparse Gaussian Process (SGP) [52] with 500 inducing points and expected improvement [53] as acquisition function.
We select the best 15 architectures w.r.t. their weight-sharing accuracies and fully train them from scratch on CIFAR-10. As shown in Table III, SVGe’s best found architecture achieves an accuracy of 95.11%, which is 0.31 percent points better than the best found architecture using the D-VAE embedding. Table III also reports compute times for model training on ENAS. It shows that SVGe can be trained more efficiently than D-VAE.

Additionally, we perform BO on the NAS-Bench-101 search space with our SVGe model and optimize on validation accuracies. We train the SGP initially on 1k randomly sampled architectures in each trial. Because of its low performance prediction on NAS-Bench-101, D-VAE is expected to perform poorly in this setting. To assess our results, in Table III, we report as oracle the best NAS-Bench-101 architecture in terms of validation accuracy and its test accuracy. BO on SVGe yields a model with 94.60% validation and 93.88% test accuracy, improving over the best found architecture using DGMG in terms of both validation and test accuracy. When using all our training data (90% of NAS-Bench-101) to train the SGP, SVGe’s best found architecture achieves a validation accuracy of 94.67%. This architecture yields a test accuracy of 94.26% on NAS-Bench-101 which is higher than the test accuracy of the best NAS-Bench-101 architecture in terms of validation accuracy. Note that the best oracle test accuracy would be 94.45% (at only 94.87% validation acc.).

Since the D-VAE training diverges on the NAS-Bench-201 search space, we can not conduct a direct comparison. Yan et al. [47] perform BO in their latent space, using DNGO [54] instead of SGP, and define the current state-of-the-art. DNGO is suited for low-dimensional embedding spaces while it performs less well on high dimensional spaces as ours. Conversely, using SGP on low-dimensional embedding spaces is sub-optimal. Therefore, a direct comparison to arch2vec in terms of BO should be taken with caution. Performing BO in the SVGe generated latent space yields a test accuracy of 93.38% on the CIFAR-10 image classification task. In comparison arch2vec yields a mean test accuracy of 94.18%, which only leaves a small gap. Thus, SVGe is able to find well-performing architectures in all three search spaces.

### E. Extrapolation Ability

Finally, we show that our smooth embedding space enables to find better architectures than the ones mentioned above even without dedicated optimization approaches by simple extrapolation from the labeled dataset. We employ the ability of SVGe to predict neural architectures’ performances on CIFAR-10 with more nodes and edges than seen at training time in both NAS-Bench-101 and ENAS search spaces.

On the NAS-Bench-101 search space, we generate graphs (cells) containing 8 nodes. Note that our SVGe model has never seen such architectures during training (NAS-Bench-101 is limited to cells with up to 7 nodes). To generate these new graphs, we pick the best performing graph from NAS-Bench-101 based on the validation accuracy and expand it to graphs with 8 nodes, maintaining the upper triangular matrices structure (1,384 graphs in total). From these graphs, we select 5 samples with the highest predicted validation accuracy using SVGe (see Sec. IV-C, trained on 1k graphs). These models are trained from scratch on CIFAR-10 using the training pipeline from [22]. As shown in Table IV, the architectures found by extrapolating using our SVGe model achieve a top-1 validation accuracy of 95.18% and a test accuracy of 94.92% for graphs of length 8, which improves over 0.83% in test accuracy over the best 7-nodes architecture test accuracy.

On the ENAS search space, we evaluate SVGe on the macro architecture containing a total of 14 nodes (layers, including the input and output node) compared to architectures with 8 nodes used during the SVGe training. We further fine-tune the embedding space by sampling 1k architectures from the training set and train the SVGe together with the performance predictor. Note that this performance predictor uses the weight-sharing accuracies as proxy for the true accuracy of the fully trained architectures. We select top 5 architectures based on the predicted validation performance and again fully train them on CIFAR-10, using the settings from [20]. As shown in Table IV, the best found architecture in the ENAS search space achieves a validation accuracy of 96.09% which is close to the one found by D-VAE. Note, D-VAE [20] used a Bayesian optimization approach as in Sec. IV-C to find this architecture, whereas SVGe can achieve similar results by direct extrapolation (aka zero-shot prediction).

Last, we test the transferability of the architectures found by our model. For that purpose, we train the best found architecture in the BO experiment and the top 1 architecture found via extrapolation on ImageNet16-120 [24] in the training scheme from [23]. As shown in Table V both architectures improve over a comparably deep ResNet architecture [55] and the best NAS-Bench-201 architecture by a significant margin.

### V. Conclusion

In this paper, we proposed SVGe, a Smooth Variational Graph embedding model for NAS. We give empirical results on SVGe encoding abilities and show that it applies more
easily to new search spaces than previous approaches [20]. We present results on the NAS-Bench-101, NAS-Bench-201 and ENAS search spaces and show good results for performance prediction surrogate models and Bayesian optimization in the smooth embedding space. Furthermore, we demonstrate the extrapolation abilities of SVGe to larger unseen graphs and the smooth embedding space. Furthermore, we demonstrate hierarchy graph representation learning with differentiable pooling, in NeurIPS, 2018.

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