Modular packaging concept for MEMS and MOEMS

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Modular packaging concept for MEMS and MOEMS

Vanessa Stenchly¹, Wolfgang Reinert¹, Hans-Joachim Quenzer¹
¹ Fraunhofer Institute for Silicon Technology, Itzehoe, Germany
vanessa.stenchly@isit.fraunhofer.de

Abstract. Wherever technical systems detect objects in their environment or interact with people, optical devices may play an important role. Light can be relatively easily produced and spatially and temporally modulated. Laser can project sharp images over long distances or cut materials in short distances. Depending on the wavelength an invisible scanning in near infrared for gesture recognition is possible as well as a projection of brilliant colour images. For several years, the Fraunhofer ISIT develops Opto-Packaging processes based on the viscous reshaping of glass wafers: First, hermetically sealed laser micro-mirror scanners WLP with inclined windows deflect in the central light reflex of the window out of the image area. Second, housing with lateral light exit permits hermetic sealing of edge-emitting lasers for highest reliability and durability. Such systems are currently experiencing an extremely high interest of the industry in all segments, from consumer to automotive through to materials processing. Our modular Opto-Packaging platform enables fast product developments. Housing for opto mechanical MEMS devices are equipped with inclined windows to minimize distortion, stray light and reflection losses. The hot viscous glass forming technology is also applied to functionalized substrate wafers which possess areas with high heat dissipation in addition to thermally insulating areas. Electrical contacts may be realized with metal filled vias or TGV (Through Glass Vias). The modular system reduces the development times for new, miniaturized optical systems so that manufacturers can focus on the essentials in their development, namely their product functionalities.

1. Motivation and concept
Miniaturized components must be generally protected against external influences, but not always, a polymer encapsulation is possible - mechanically moving elements or optical components must remain free, so that a cavity is required. The sticking of a package is not acceptable in many applications, because water vapor can pass the adhesive-seal and condense in the cavity which usually leads to a failure of the component [1]. Then the hermetic sealing of the entire assembly by welding or soldering with metallic-solder or glass frit is the only option. A hermetic package is inevitable, if special demands are made on the atmosphere in the assembly, for example, a defined vacuum, an inert gas filling or the complete absence of hydrocarbons [2]. The wafer-level packaging (WLP) has now become a standard technology in the field of micro-mechanical sensors; the packaging of optical components and systems on wafer level is still relatively rare. This is mainly due to the so far limited opportunities to make small optical housing by functional aspects or to meet all the requirements of optics, electronics and thermal management. This point is where the modular packaging system of Fraunhofer ISIT becomes important. The aim is to develop a "kit" for the production of hermetically sealed, application specific wafer level (WL) housing for the construction of optical and mechanical components and systems. The production of the glass cover is hereby based on high temperature
viscous glass micromachining with glass and silicon wafers [3], the micromechanical glass processing and a series of sequential bonding steps of glass and silicon wafers. This technology tool set enables the production of differently oriented, integrated windows on full 200 mm (8") wafers. However, the glass flow technology also enables the production of substrates with integrated electrical feedthroughs (Through-Glass Via, TGV) of highly conductive silicon (TGV A) or the introduction of heat sinks. Figure 1 illustrates the different possible combinations of different cap wafers and TGV Substrates and their applications.

Figure 1: Schematic of different optical housing constructions supported by the modular packaging system.

2. Technology of different cap wafers
A new process has been developed for the fabrication of complete 8" cap wafer with a plurality of inclined optical surfaces for hermetic sealing of micro mirrors with the benefit of the elimination of disturbing reflections [4]. Figure 2 shows a schematic of the fabrication process flow in a cross sectional view. At first, deep cavities are etched into two silicon wafers with a DRIE process step (a). One of these two structured silicon wafers is anodically bonded on a borosilicate glass wafer (b). For this step it is necessary that all wafers are very clean and particle free. After anodic bonding a grinding step follows to define a pattern of silicon islands. The grinding process introduces residual stress in the silicon; a short stress relief step eliminates the surface stress in the silicon elements. Otherwise the stress in the silicon islands causes a warpage in the optical windows areas. This glass wafer with silicon structures on one side is finally bonded on a third silicon wafer, which provides pre-defined cavities wherein the silicon islands are inserted (c). The third silicon wafer is also structured by a DRIE etch process step. During the anodic bonding a nitrogen atmosphere with pre-adjusted pressure of about 950 mbar is enclosed in the cavities. After the anodic bonding the second silicon island wafer is bonded on the wafer stack (d). Then a last grinding step follows to define the islands on the outside of the glass wafer (e). That composite wafer is then annealed above the softening point of the glass material (f). By the thermally induced pressure difference between the cavities and the oven atmosphere above 680°C the silicon glass stacks inside the cavities are extruded within a defined time period. A non-centric arrangement of the silicon islands leads to an inclination of the silicon-glass stacks. Finally, the silicon is selectively removed in a KOH wet etch step (g). The final bonding of the processed glass wafer with the micro mirror wafer is done by the seal glass bonding. In Figure 3 a finished glass wafer with inclined windows is shown.
Today laser diodes are packaged in TO housings that are not SMD compatible. Mobile applications require a much more economical and small factor package solution for light sources. We present a solution that realizes flat glass packages with vertical emission window for laser diodes on 8” silicon substrates. The new process uses a high temperature glass forming process with a combination of two different glasses each having different melting points. Figure 4 shows a schematic of the fabrication process flow for the optical cap with vertical emission window. At first, cavities are etched into a silicon wafer with a DRIE process step (a). After anodic bonding of this structured silicon wafer with a borosilicate glass wafer (b), a mechanical dicing step follows from the silicon side along the DRIE etched silicon structures to define the pinboard (c) wherein the high melting glass window can be inserted later (d). The height of the silicon islands is predetermined by the wafer thickness of the starting material and also defines the cavity height. After a cleaning step to remove silicon residuals the high melting glass stripes can be applied (e). Because the stripes were previously separated from a wafer by mechanical dicing, they have to be annealed in a separate step to take out the moisture that accumulates in the diced edges. When the stripes will be inserted in the pinboard they have to be turned upright 90°, so the polished and smooth surface is arranged perpendicular to the substrate surface. After a further silicon wafer is applied, the complete stack is rotated. In the next step the glass-edge of the peripheral area is to be depressed in vacuum, so the glass is hermetically sealed with the silicon. Thereby the glass seals with the silicon uniformly and without air pockets, a ROBAX®-ring coated with boron nitride is placed on the stack to work as a downholder (f). Here, it is important
that the annealing is performed under the transformation temperature of the high melting glass (g). In a second step, the stack is annealed under atmospheric pressure at the same temperature until the glass is completely flown or pressed down by the pressure difference in-between the silicon structures and fuses with the high melting point glass window sections (h). The annealing duration is highly dependent on the design and the aspect ratio of the silicon structures. Finally, the silicon is selectively removed in a KOH wet etch step (i). After releasing the complete silicon from the cap wafer a two sided grinding step follows. The front side has to be planarized to enable the following processes. A grinding step on the lower side must be carried out, because the borosilicate glass does not completely wet the high-melting glass. This resulting gap prevents subsequent hermetic sealing. After this planarization an anti-reflective coating is applied. In the next step a plating base is deposited with a shadow mask on the bond frames of the cap wafer (Fig. 5).

![Diagram](image_url)

**Figure 4:** Schematic of the process flow for the glass wafer with vertical windows.

![Image](image_url)

**Figure 5:** Left: Silicon wafer with inserted glass stripes after second annealing. Right: Detail view of a glass cap wafer with vertical emission windows.

### 3. Technology of the Through Glass Vias Wafer

To keep the entire component as small as possible, electrical contacts may be realized by Through-Glass-Vias. The schematic in Figure 6 (left) shows our process flow which limits the waferbow to less than 100 µm [5]. At first, deep cavities with a high aspect ratio are etched into a silicon wafer with a DRIE process step (a). After anodic bonding with a glass wafer (b) an annealing step follows where the glass is completely pressed in the small structures (c). To eliminate the unevenness of the wafer surface, the wafer is grinded until the silicon contacts are opened (d). Then the backside of the wafer is
also grinded to remove the silicon. Finally the TGV is polished to remove the surface roughness. In Figure 6 (right) a part of a glass substrate wafer with silicon vias is shown.

![Figure 6](image)

**Figure 6:** Schematic of the process flow for TGV-wafer (left) and view on glass substrate wafer with silicon vias (right).

### 4. Examples of packaged laser diodes and MEMS mirrors

The cap wafers with inclined windows are typically bonded to micro mirror wafers by using glass frit sealing (Fig. 7, left). Figure 7 (right) shows a cross section of an X-Ray photograph of a fully caped mirror device. The inclined optical window and the surrounding socket are clearly visible. The integrated cavity ensures the free movement of the enclosed micro mirror and the bonding of an additional spacer wafer could be avoided.

The first processed glass cap wafers with a vertical emission window for laser diodes (side looking) and the glass cap wafers with inclined windows for micro mirrors were built up without the TGV-wafer. The packaged laser diode demonstrators were assembled on silicon based wafer substrates. AuSn metallized solder pads and metal seal frames enable an eutectic submount- and laser diode soldering. An active solder was used for hermetic bonding of the single glass cap with the silicon substrate (Fig.8).

![Figure 7](image)

**Figure 7:** Close up of a wafer level vacuum packaged mirror with an inclined window with a size of 3.3 x 4.5mm (left) and a X-Ray cross section through a full-caped-mirror-device (right).
Figure 8: Detail view of the glass cavities within an 8" wafer with vertical emission windows (left) and a X-Ray cross section through a housed laser diode (right).

5. Conclusion
The first processed glass cap wafers for laser diodes and micro mirrors demonstrate the capabilities of the new developed glass forming technologies. Recently the first laser diodes and micro mirrors have been successfully packaged with the developed glass caps. The actual work is focused on the integration of the TGV wafer and the expansion to further glass cap processes.

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Patents pending
The presented technologies are patented under US 7,416,951 B2 and US 14,361,392.

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