Module development for the HL-LHC ATLAS ITk Pixel upgrade

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ABSTRACT: For the Large Hadron Collider (LHC) Phase 2 upgrade ATLAS will replace its current inner detector with an all-silicon Inner Tracker (ITk) to achieve high performance in a very high occupancy and radiation environment. The ITk consists of strip and pixel modules. Here the focus is placed on the assembly and testing procedures needed to assure the quality of the pixel modules to be installed in the detector. Ongoing developments and activities are discussed, e.g. with a special focus on the effect of mechanical stress in the connection of sensor and readout chip in the module due to thermal effects.

KEYWORDS: Hybrid detectors; Particle tracking detectors; Particle tracking detectors (Solid-state detectors)
1 Introduction

Starting in 2024, the Large Hadron Collider (LHC) at CERN will be upgraded to the High-Luminosity LHC (HL-LHC). With this upgrade, the instantaneous luminosity will be increased from $2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ to $5-7 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$. A total of 4000 fb$^{-1}$ of data is foreseen to be collected. At this luminosity, there will be more collisions per bunch crossing, up to 200 pile up events. This leads to an increased occupancy and fluence, especially in the innermost layer of the ATLAS detector where a value of $26 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$ will be reached. To keep high tracking performance under these conditions the ATLAS inner detector (ID) is foreseen to be replaced with a fully silicon based Inner Tracker (ITk) [1].

2 ATLAS ITk

In figure 1(a), a schematic layout of the active components of the ITk is shown. A complete description can be found in the ATLAS ITk Pixel TDR [2]. The ITk consists of silicon detectors with four layers of strip modules and five layers of pixel modules. As the entire ID will be replaced by these layers, the area instrumented with silicon detectors will increase to around 173 m$^2$ from the 62 m$^2$ of the present detector. A selected list of parameters is compared for the current and future setup in table 1. The important parameters for the physics performance are the increased track coverage in pseudorapidity of $|\eta| \leq 4$, which allows for studies of very forward events in the detector, and the overall higher trigger rate of the full detector.

Focusing on the Pixel Detector part, there are three main topics that have to be addressed for a high performance detector under the HL-LHC conditions. For the readout, a low hit occupancy in every module is needed to reduce the used bandwidth and for the tracking to be able to distinguish
particle tracks. A pixel size of $50 \times 50 \mu m^2$ or $25 \times 100 \mu m^2$ is therefore chosen for a high granularity. In simulations a maximum channel occupancy of 0.16% in the innermost layer was computed.

An increased granularity leads to more channels to be read out. Within the RD53 project [4] at CERN, ATLAS and CMS experiments have developed a new readout chip, also known as RD53A [5]. It has a pixel size of $50 \times 50 \mu m^2$ and a readout speed of up to $4 \times 1.28 \text{ Gb/s}$. All pixel layers will use the same readout chip that will be likely a derivation of the RD53A chip. Towards the end of this year, ATLAS will submit a new version of the chip named ITKpixV1. In the meantime, the first prototype (RD53A) is available for tests. This chip is only half of the expected final size. However, due to the limited availability, most of the prototyping tests for various stages of building the ITk are carried out with the FE-I4 readout chip from the ATLAS IBL [6]. The main differences to the ITKpixV1 are the larger pixel size ($50 \times 250 \mu m^2$), lower radiation hardness and lower bandwidth availability.

In figure 1(b), the neutron equivalent fluence in the Pixel Detector is displayed for the full runtime ($4000 \text{ fb}^{-1}$). Different pixel sensor technologies are used in the different layers to cope with the radiation damage. In the innermost layer, 3D sensors of $150 \mu m$ active thickness are used; for the other layers, planar sensors with $100 \mu m$ ($150 \mu m$) thickness are expected in the second (third and fourth) layer. Because the radiation damage is too high for the readout chip in the two inner

Figure 1. (a): schematic layout of one quadrant of the ATLAS ITk in beam direction $z$ and radial direction $r$ with silicon strip modules in blue and pixel modules in red [3]. (b): 1 MeV neutron equivalent fluence in the Pixel Detector normalised to $4000 \text{ fb}^{-1}$ [2].

Table 1. Comparison of ATLAS inner detector with the ITk.

|                      | LHC Run2 ID | HL-LHC ITk |
|----------------------|-------------|------------|
| Si area Pixel $[m^2]$| 1.9         | 13         |
| Si area Strips $[m^2]$| 60         | 160        |
| Channels Pixel       | $\approx 9.2 \times 10^6$ | $\approx 5 \times 10^9$ |
| Channels Strips      | $\approx 6 \times 10^6$ | $\approx 50 \times 10^6$ |
| $|\eta|/ \text{ coverage}$ | 2.5 | 4.0 |
| Pixel size $[\mu m^2]$ | $50 \times 400$ and $50 \times 250$ | $50 \times 50$ or $25 \times 100$ |
| L1 Trigger rate $[kHz]$ | 100 | 1000 |
layers, it is foreseen that this region will be replaced after half of the runtime, hence accumulating only the fluence of $13 \times 10^{15}$ $n_{eq}/cm^2$. To cope with the high level of leakage current after radiation, the Pixel Detector will be cooled to $-25^\circ$C via CO$_2$ cooling.

Further features of the ITk layout are inclined modules in the barrel layers to minimize the material and maximize the acceptance in these areas. Material minimization is also aimed for by connecting the modules to serial powering chains and by that reducing the cable material in the detector volume.

3 Pixel modules

All pixel modules are hybrids of a sensor connected to a readout chip via bump bonds, forming the so called bare module. On top of the sensor a flexible PCB, short flex hybrid or flex, is glued. Wire bonds to the flex connect the readout chips and the sensor of the module to the off-detector electronics such as the readout system or the bias voltage supplies. The wire bonds are encapsulated for mechanical stabilisation and protection from corrosion; see a schematic in figure 2.

![Schematic of the hybrid pixel modules](image)

Figure 2. Schematic of the hybrid pixel modules [2].

The 3D and planar modules are built into pseudo-triplets and quad chip modules, respectively. For the triplets, three single bare modules are combined into one module with one flex. Four readout chips are bump bonded to one large sensor in case of the quad chip module. A common flex is used in all barrel layers and endcaps for the quad chip modules to simplify the production. Locally, the connection from the flex to the support structure of the detector is adapted to the specific layout needs.

3.1 Module assembly

The module assembly consists of two parts: gluing the flex to the bare module and wire bonding the readout chip to the flex with encapsulation of the bonds afterwards. The use of a semi-automatic wire bonder drives the precision of the alignment of flex and bare module. Current tolerances on the position of the flex are $\pm 50\mu m$ whilst $25\mu m$ is required in flatness of the flex. To achieve such precision, a common tooling is being developed by the collaboration. In figure 3 a first schematic of the components is shown. The bare module is positioned at edges on the jig and held there by vacuum. The flex is placed on dowel pins on a second jig and fixated also by vacuum. Cut outs in the jig leave room for the components on the flex. Then the glue is applied with a stencil on the flex. The stencil assures an even distribution and glue at the important regions as below the wire bond pads. With the glue applied to the flex, the flex is aligned to the bare module by dowel pins and holes in the jigs.

After the glue is cured the readout chip and the flex are connected with wire bonds. The wire bonds are then encapsulated for protection against mechanical damage and corrosion.
Many modules with FE-I4 are already built with this kind of tooling. For the upcoming module building with RD53A readout chips the design is adapted to the dimensions of the used components.

4 Quality control and assurance

During the ITk production phase, the quality of every module will be controlled. Not only the final module will be tested: starting from wafer level of sensors and readout chips, over intermediate stages of the assembly, tests will be carried out. In this way, the use of only good quality components is ensured, and bad ones are sorted out as early as possible. In this paper, the focus is placed on describing tests at the module level and on module performance at the detector level.

The first type of tests are visual inspections for the size and flatness of the module, and mass measurements. As the clearance between modules in some parts of the detector is about 200 μm, controlling the size of each module and staying within the design envelope of the module is very crucial.

The second type of tests are electrical function tests of sensor and readout chip. These are carried out both at room temperature and at the detector operational temperature (−25°C on the module).

The sensor current voltage (IV) characteristic and the long-term stability of current at high voltages are measured. Small leakage currents in the order of nano- to micro-ampere are important to keep the noise in the module and the power consumption low.

The gain and the threshold of every pixel of the readout chip have to be calibrated. Threshold settings are tuned by iterative adjustment of registers based on occupancy measured at the target charge created using an internal injection circuitry.

Particles from radioactive sources and X-rays are used to test the pixel quality. Most importantly, the connection of the sensor pixel to the readout and the signals of the particles are assessed. Only a small fraction of the pixels are allowed to be disconnected or not functioning, otherwise the module is discarded from installation in the detector.

The modules are built from different materials such as silicon, tin-silver or indium bump bonds, glue, and the flex material. Assembled at room temperature but operated at −25 °C, the different thermal expansion coefficients (CTE) will induce mechanical stress in the module. To test this behaviour, thermal cycles are foreseen of each module.
Figure 4. Example prototype of a module test system with a brass cooling block connected to a chiller, and a holder for radioactive sources motorised in two axis. For radiation protection the system is set in a steel box with interlock system for the doors.

The module test systems need to be automatised and parallelised to a certain extent to ensure the throughput of modules for the given timeline. They need to have cooling capabilities to $-25 \, ^\circ\text{C}$ on the modules. Environmental control and monitoring of temperature and humidity is needed to protect against icing and condensation effects during low temperature tests. For exposure of the modules to particles, a motorised holder for a radioactive source is needed. In figure 4, a prototype of a test system with one cooling block for one module connected to a chiller and a source holder on a two axis stage is shown. Similar systems based on peltier elements instead of chillers are also in development.

Common procedures for the tests have been defined. Uniformity of test procedures across participating sites is ensured via comparison of tests made with identical “traveller modules”.

A different kind of test should ensure not only the quality of each module but, on a more general level, also the quality of the production mechanisms. To monitor the quality assurance, some of the modules per production batch are tested in much more detail. Here the focus will be on the already mentioned mechanical stress in the modules.

4.1 Mechanical stress in the modules

During operation, the detector is expected to be cooled down and warmed up hundreds of times. The components of the module have different CTE values, as shown in table 2. Therefore, temperature changes from the assembly temperature induce mechanical stress in the module. The most probable point of failure under these forces is the bump bond connection of the sensor to the readout chip.

To test this behaviour, the modules are subjected to thermal cycles. For quality control and assurance, the parameters for temperature range, heating/cooling rate, and number of cycles are under discussion for the different tests. The test presented here is conducted in the temperature range of $-55 \, ^\circ\text{C}$ to $60 \, ^\circ\text{C}$ with a temperature slope of $2 \, ^\circ\text{C}/\text{s}$. This range is covering extreme failure scenarios such as the breaking of a coolant pipe with $\text{CO}_2$ spilling onto the modules or an interlock failure causing a module to stay on without cooling. This is a larger range than the standard detector operation range. It is expected that failures in the module occur after fewer cycles but the general behaviour is assumed to be the same.
Table 2. The thermal expansion coefficient of the materials. The module is fixed to a rigid support with CTE = 0 K\(^{-1}\). The summary of the simulation as the maximum stress in the bump bonds for the normalised thickness of copper is shown in figure 6. Lower copper content in the flex reduces the stress in the bump bonds. For a copper thickness around 25 \(\mu m\), the expectation is that the module should survive the thermal cycling for a longer period because the stress is less than the ultimate tensile strength of solder.
Table 2. Material properties of the module components, and flex copper compositions used in the stress simulations.

| Material                  | Young modulus [GPa] | CTE $10^{-6}$K$^{-1}$ |
|----------------------------|---------------------|------------------------|
| Copper                     | 110                 | 18                     |
| Kapton substrate           | 2.5                 | 20                     |
| Glue (Araldite 2011)       | 1.9                 | 85                     |
| Silicon                    | 188                 | 2.6 (temp. dep.)       |
| Bump bonds                 | 10                  | 21                     |

|                     | Copper layer 1 | Copper layer 2 |
|---------------------|----------------|----------------|
| thickness [µm]      | coverage [%]  | thickness [µm] | coverage [%]  |
| Model 1             | 35–10          | 100            | 35–10         | 100            |
| Model 2             | 35–10          | 70             | 35–10         | 100            |
| Model 3             | 35–10          | 50             | 35–10         | 100            |
| Model 4             | 35–10          | 50             | 10            | 100            |

Figure 6. Maximum stress in the bump bonds depending on the normalised thickness of copper in the flex from simulating the models in table 2.

In addition, further simulations will investigate low CTE flex base materials. The next generation of flexes will be based on the studies and will be used for the first assembly of modules with RD53A readout chips.

4.2 Demonstrator projects

Not only modules are tested but also larger structures like staves and rings with modules. With these demonstrators, many steps of the detector production process can be practised: starting with assembling the modules and building the support structure, and combining both by loading the modules on them. Every piece can be tested at intermittent steps, and in the end the full system can be tested. For example, the new serial powering scheme of the modules is investigated whilst the voltage drop across the power line is optimised. The ability to test on many connected modules in parallel is also important for the development of both hardware and software of the readout system. At the moment these demonstrators are based on modules with the FE-I4 readout chip, but in the near future there will be similar studies with the RD53A chip as more modules are assembled.
5 Summary and outlook

The upgrade project of the ATLAS inner detector to the ITk for HL-LHC is nearing the production phase for the Pixel Detector. Despite the fact that module assembly and testing processes are well defined and advanced, they will need to be adjusted once the final module dimensions and readout systems are known. Possible solutions for the reduction of mechanical stress in the bump bonds to avoid disconnections during thermal cycles are under test and results are expected soon.

The first assembling of modules with RD53A readout chip will start at the end of 2019. Shortly after, a large scale test systems will be built with the new modules. With this, the project is on its way for installing ITk in ATLAS in the long shut down 3 of the LHC (2024–2026).

Acknowledgments

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