Temperature dependence of the electrical properties of MOS devices constructed by sol gel deposited BaTiO₃ films on p-Si

N Konofaos¹,*, Z Wang², Th K Voilas¹, S N Georgia³, C A Krontiras³, M N Pisanias³, J Sotiropoulos³ and E K Evangelou⁴

¹Computer Engineering & Informatics Department, University of Patras, GR-26500 Patras, Greece
²Department of Chemical and Nuclear Engineering, University of New Mexico, 1001 University Blvd. SE, Advanced Materials Laboratory, Albuquerque, NM, 87106, USA
³Physics Department, University of Patras, GR-26500 Patras, Greece
⁴Physics Department, University of Ioannina, P.O.Box 1186, 45110 Ioannina, Greece

*E-mail: nkonofao@ceid.upatras.gr

Abstract. The electrical properties of MOS devices with high-k insulating BaTiO₃ sol gel films fabricated onto p-Si substrates, were investigated by a variety of electrical techniques. The aim was to identify the temperature dependence of the electrical properties of the MOS devices. All samples exhibit a typical MOS behaviour. The density of interface states Dit was found to decrease with decreasing temperature and lies between 1x10¹¹eV⁻¹cm⁻² at near midgap and 3x10¹²eV⁻¹cm⁻² near the gap edges. The bulk-trapped charges were calculated to be between 40 and 120nCbcm⁻². The samples depicted high dielectric constants reaching values of 120. The results revealed that the sol-gel technique creates effective microelectronic devices.

1. Introduction
Barium titanate (BaTiO₃) and the other perovskite-type materials have been extensively studied for their potential commercial applications in microelectronics, due to their desirable dielectric properties [1-3]. Many methods, such as rf sputtering, laser-ablation, MOCVD (metalorganic chemical vapour deposition) and sol-gel techniques, have been used to grow thin films. Metal-Oxide-Semiconductor (MOS) devices with BaTiO₃ (BTO) films as gate material, have been reported and analysed together with applications in circuits such as DRAMs [4]. In all cases, reliability issues have risen due to process related defects, leakage currents or abnormal behaviour of the dielectric.

The polymeric precursor method [3] is a chemical technique that offers low cost, good compositional homogeneity, high purity, relatively low processing temperatures and the ability to coat large substrate areas. In this technique, the desired metal cations are chelated in a solution using a hydroxycarboxylic acid as the chelating agent. The solution is mixed with a polyhydroxyalcohol and heated to promote esterification reactions in the solution, while the metals remain homogeneously distributed in the polymeric network.

In this paper, the electrical properties of MOS devices constructed by the deposition of BTO films on p-Si by the polymeric precursor method are reported. Issues such as the leakage current, the capacitive and conductive response of the devices and the electrical characterisation of the BTO/Si interface are examined, revealing values of the interface states density, the bulk trapped charges and...
the dielectric constant. Temperature dependence measurements allowed the derivation of the traps distribution for various biases in depletion region in conjunction with their temperature response.

2. Experimental
The BaTiO$_3$ films were prepared by the sol-gel technique. Initially, Ti (IV) isopropoxide was added into a citric acid solution (60–70 °C) to form titanium citrate. After homogenization of the Ti-citrate solution, a stoichiometric amount of BaCO$_3$ was slowly added under stirring. Ammonium hydroxide was also added to promote the complete dissolution of BaCO$_3$ (the final pH of the solution was 7–8). After homogenization of the solution, ethylene glycol was added to promote citrate polymerization by polyesterification reactions. The molar ratio of Ba/Ti was 1:1, the citric acid/Ba molar ratio was fixed at 1.00, and the citric acid/ethylene glycol ratio was fixed at 60/40 (mass ratio). Polymerization was performed at 90 °C for 12 h in an open-mouthed 500 ml beaker (evaporated water was compensated from time to time), after which the solution’s viscosity was adjusted by controlling the amount of water left. The solution was deposited onto $p$-type Si (100) wafers with resistivity in the range of 100-500 Ohm·cm, by spin-coating at a spin rate of 3000 rpm for a period of 30 s. Following deposition, the films were dried on a hot plate at ~150 °C for 2 min to remove residual solvents. Heat treatment was carried out in a furnace under air at atmospheric pressure with a preset temperature and all samples were treated at 450 °C for 2 h. Al metal electrodes were evaporated on top of the BTO films via a mask allowing the creation of 3mm dots in diameter, as well as at the back of the Si substrate in order to form ohmic contacts. Thus devices with the Al/BTO/p-Si (MOS) structure were fabricated.

For the electrical measurements, the samples were kept in a cryostat under a controlled reduced He atmosphere. The measurements were performed at different temperatures from 230K to 330K, set by an Oxford ITC503 Temperature Controller with a resolution of ±0.01K. The I-V curves were taken using a Keithley 617 programmable electrometer connected with an Oltronix power supply. The C-V, G-V and admittance spectroscopy $Y$-$\omega$ measurements were performed using a Novocontrol Alpha-N Dielectric Response Analyzer suitably controlled by the WinDeta software package.

3. Results and discussion
The electrical techniques include temperature dependent current-voltage measurements (I-V) in order to account for leakage currents, and C-V, G-V measurements, at different temperatures, in order to identify the MOS behaviour. In addition, admittance spectroscopy was used to measure the interface state density ($D_{it}$) at the BTO/p-Si interface and the bulk trapped charges.

The leakage currents through the BTO dielectric were measured for the whole temperature range. Previous published work [1,2] suggests that the origin of this leakage current is primarily attributed to either space charge limited currents or Poole-Frenkel related effects. Recently obtained results [5] on BTO films at room temperature reveal that the prevailing conduction mechanism is Poole-Frenkel. The same behavior was observed in the whole temperature region investigated in the present work. The effects of the leakage currents on the device characteristics, were taken into account and all measurements reported hereafter have been corrected for such dc leakage currents.

Figure 1 depicts the C-V characteristics of the Al/BTO/p-Si devices at different temperatures for a frequency of 100kHz. The overall behaviour is indeed that of an MOS device, with the distinct regions of accumulation-depletion-inversion clearly shown. In order to account for a dispersion observed in the accumulation region, the data were treated according to the method proposed by Vogel et al [6]. The value of the dielectric constant was calculated to be as high as 120, by using the RT curve at accumulation. Moreover, bulk defects were identified in the form of trapped charges. The values of these charges were found between 40 and 120 nCcm$^{-2}$.

Figure 2 presents parallel conductance curves versus frequency ($G_p/\omega$ vs $\omega$) obtained by admittance spectroscopy as a function of applied bias voltage at 0°C. It is obvious that as the bias voltage becomes more negative, the corresponding curve shifts to higher frequencies with concurrent increase of the peak value of $G_p/\omega$. This behaviour reflects a uniform distribution of the interface states [7].
Parallel conductance curves versus frequency (Gp/ω vs ω) are presented in figure 3 as a function of temperature for a bias voltage V=-1.0V. For clarity reasons only selected temperatures are presented.

As it is observed form figure 3, each curve shifts to higher frequencies as the temperature increases with concurrent increase of the peak value of Gp/ω. This behaviour further verifies a uniform distribution of the interface states allowing in addition, the investigation of their density and time constant distribution over a wider energy range within the semiconductor gap [7].

The analysis of the curves followed the statistical model proposed by Nicollian [7]. This analysis allows the calculation of both the density of interface states (Dit) and the traps time constant (τ). The results are depicted in table 1 and can be summarised as follows. The traps allocation depicts a smooth and uniform distribution in the semiconductor gap, showing that the deposition method used created an electrically smooth interface. The Dit values were found to range between 1x10^{11} eV^{-1}cm^{-2} at near midgap and 3x10^{12} eV^{-1}cm^{-2} near the gap edges. The trap time constant was calculated to be of the order of 10^{-3}s for states located close to the Si mid-gap, with corresponding densities not being high enough to pin the substrate Fermi level in which case they would prevent the creation of an effective MOS device.
Table 1. Values of Dit and $\tau$ for $V=-1.0V$ at various temperatures.

| Temperature $^\circ$C | Density of states ($D_\text{it}$) eV$^{-1}$ cm$^2$ | Time constant ($\tau$) sec |
|-----------------------|-----------------------------------------------|---------------------------|
| 20                    | 3.0 x 10$^{12}$                              | 1.2 x 10$^{-3}$            |
| 10                    | 8.2 x 10$^{11}$                              | 1.6 x 10$^{-3}$            |
| 0                     | 4.5 x 10$^{11}$                              | 9.7 x 10$^{-2}$            |
| -10                   | 2.0 x 10$^{11}$                              | 9.0 x 10$^{-2}$            |
| -20                   | 1.3 x 10$^{11}$                              | 8.2 x 10$^{-2}$            |
| -40                   | 1.2 x 10$^{11}$                              | 8.2 x 10$^{-2}$            |
| -60                   | 1.0 x 10$^{11}$                              | 8.1 x 10$^{-2}$            |

Compared to recently published results on sputtered BTO films on Si, the devices constructed by this sol-gel technique, show very similar characteristics [1-4]. Despite the fact that the chemical method requires a lot of sample treatment, the samples prepared by the sol-gel technique exhibit electrical behaviour comparable to that observed in samples prepared by sputtering.

4. Conclusions
The electrical properties of MOS devices constructed by high-k insulating BaTiO$_3$ (BTO) sol gel deposited films onto p-Si substrates were investigated by electrical techniques at various temperatures. The aim of this work was to identify charges residing at the BTO/Si interface and the bulk of the insulating film. The results showed that the density of states was not high enough to pin the Fermi level of the Si substrate allowing thus the creation of an MOS device. This was further verified by the fact that the temperature dependence measurements showed that for a wide temperature range, these values remained well below an upper limit of 10$^{14}$ eV$^{-1}$ cm$^2$. Moreover the values of the $D_\text{it}$ are directly comparable to those reported for sputtered films. The distribution of the traps is uniform, thus the sol-gel technique creates an electrically smooth interface. As a consequence it is proposed that the sol-gel technique produces high quality BaTiO$_3$ films suitable for microelectronic applications. Future work involves the investigation of samples prepared by different methods.

5. References
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