Design and Optimization of 22 nm Gate Length High-k/Metal gate NMOS Transistor

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Abstract. In this paper, we invented the optimization experiment design of a 22 nm gate length NMOS device which uses a combination of high-k material and metal as the gate which was numerically developed using an industrial-based simulator. The high-k material is Titanium dioxide (TiO2), while the metal gate is Tungsten Silicide (WSi). The design is optimized using the L9 Taguchi method to get the optimum parameter design. There are four process parameters and two noise parameters which were varied for analyzing the effect on the threshold voltage (Vth). The objective of this experiment is to minimize the variance of Vth where Taguchi’s nominal-the-best signal-to-noise ratio (S/N Ratio) was used. The best settings of the process parameters were determined using Analysis of Mean (ANOM) and analysis of variance (ANOVA) to reduce the variability of Vth. The results show that the Vth values have least variance and the mean value can be adjusted to 0.306V ±0.027 for the NMOS device which is in line with projections by the ITRS specifications.

1. Introduction

The replacement of Silicon Dioxide (SiO2) as the gate dielectric with a high dielectric (high-k) material in future complementary metal-oxide-semiconductor (CMOS) technology is being widely studied nowadays. A number of different high-k materials have been proposed and analyzed to achieve the future trends in semiconductor where the decrease in the size of devices causes the decrease in the size and the thickness of the dielectric gate. As the physical thickness of SiO2 - based gate oxides approaches 2 nm, a number of fundamental problems occur such as the increment of gate leakage current, oxide breakdown, boron penetration from the polysilicon (poly-Si) gate electrode and channel mobility problem [1, 2]. Each one of these phenomenon is important for device operation. In other words, the conventional device-scaling scenario involving scaling down of SiO2 - based dielectrics up to below 1 nm becomes impractical now[1].

During early high-k dielectric development, material incompatibility between high-k and the poly gate electrode was discovered [3, 4]. One of the issues was the high defect rates at the interface of high-k and poly-Si causing the device’s lower electrical mobility. The latter was attributed to charge scattering, which is intrinsic to the physics of an integrated poly and high-k device [5]. Therefore, self-aligned silicide (SALICIDE) technology has been widely used to reduce the sheet resistance (Rsh) of poly-Si gates [6].
Then there is another solution by replacing poly-Si with a metal gate electrode. Replacing poly-Si gate materials with metal is the answer to the compatibility issues between the high-k dielectric and poly electrode. Significant effort and research was focused on finding metal electrodes with the correct work function [7]. However, the metal work functions are needed to adjust the NMOS and PMOS devices' threshold voltage (V\text{th}).

Current research efforts are focused on metal oxide materials with high-k values (e.g., ZrO\text{2}, HfO\text{2}, Al\text{2}O\text{3}, Y\text{2}O\text{3}, La\text{2}O\text{3}, and TiO\text{2}) since their introduction produce a physical thicker oxide, causes reduction in gate leakage current and in the same time maintaining a large gate capacitance [8]. From previous research, the scaled down design of 22 nm gate length NMOS device from 32 nm gate length was a success [9]. This paper is the continuation from the previous work where the device design is optimized using Taguchi’s L9 orthogonal array. The results show that a 22 nm gate length NMOS transistor with V\text{th} value of 0.306V that is well within ITRS 2011 prediction can be produced numerically [10].

2. Materials & methods

The fabrication process steps are as follows. The substrate used for the experiment was a p-type silicon with a <100> orientation. It is then followed by growing an oxide layer, at the top of the bulk silicon using dry oxygen. P-well implantation process was done, using this oxide layer as a mask. This was done using Boron as dopant with a dose of 3.75x10\text{12} ions/cm\text{2}. The silicon wafer then underwent the annealing process at 900 °C in a Nitrogen environment, and followed by dry oxygen in order to ensure that boron atoms are being spread properly in the wafer. The next step was to produce a Shallow Trench Isolator (STI) of 130 Å thickness [11]. In order to form the STI layer, the wafer was oxidized in dry oxygen for 25 minutes. Then, a 1000 Å nitride layer was deposited on top of the oxide layer by applying low pressure chemical vapour deposition process (LPCVD), followed by a photo resist deposition with a thickness of 1.0µm. The trench depth of 3200 Å was achieved. Thereafter, a sacrificial oxide layer was grown and then etched followed by a sacrificial nitride layer whereby the trench is then completed.

Then the high-k material, TiO\text{2} was deposited for thickness of 2 nm [12] followed by etching to get the desired thickness and was adjusted to produce a 22 nm gate length. The next step was to implant the N well active area, in order to adjust the threshold voltage, V\text{th} value. The dosage for boron was 6.98x10\text{12} atom/cm\text{2}. Tungsten silicide (WSi\text{x}) will then be deposited on the top of the bulk device with thickness of 8nm and etched accordingly to produce the gate contact point as desired [13]. Later on, Halo implantation was performed in order to get an optimum performance for the NMOS device where Indium was implanted with the dose of 12.76x10\text{12} ions/cm\text{2}. The dosage was varied in order to get the optimum value [6, 14]. Then spacers were formed at each of the polysilicon sides, namely the source and drain regions respectively. Side wall spacers were used as a mask for source and drain implantation [15]. Then, there are source-drain implantations where Arsenic was firstly implanted with a dose of 5.1x10\text{13} ions/cm\text{2} followed by phosphorous with a dose of 1.5x10\text{12} ions/cm\text{2}, to ensure the smooth current flow in the device. The next process was the development of 0.5 µm Borophosphosilicate Glass (BPSG) layer [16]. This layer acts as a pre metal dielectric (PMD). After Borophosphosilicate Glass (BPSG) deposition, the wafer undergoes annealing process at a temperature of 950 °C [16].

The next process was compensation implantation using phosphorous, with a dose of 3.71x10\text{13} ions/cm\text{2} [17]. Then, aluminium layer was deposited on top of the structure and then it was etched accordingly to form the metal contact for the source and drain. At this stage the transistor design is completed. Figure 1(a) and Figure 1(b) shows the overall device structure and the enlarged figure of the 22 nm gate length of the high k/metal gate NMOS transistor respectively. Figure 2 shows the net doping profile of the device that was successfully designed. Then, the transistor undergoes electrical characteristic measurement in order to find the threshold voltage (V\text{th}) in reference to ITRS 2011 [10].
The Taguchi orthogonal L9 array method requires 4 process parameters and two noise factors were also chosen to complete the design of four sets of experiments consisting of 36 runs. The noise factors are included in order to get a more accurate design and to make the process parameters insensitive to variation. All these values of the process parameters of each levels and noise factors are listed in Table 1 and Table 2 respectively.
Table 1. Process parameters and their levels

| Symbol | Process Parameter       | Unit       | Level 1      | Level 2      | Level 3      |
|--------|-------------------------|------------|--------------|--------------|--------------|
| A      | Halo Implant            | atom/cm³   | 1.270e¹³ (A1)| 1.275e¹³ (A2)| 1.280e¹³ (A3)|
| B      | S/D Implant             | atom/cm³   | 5.100e¹³ (B1)| 5.150e¹³ (B2)| 5.200e¹³ (B3)|
| C      | Compensation Implant    | atom/cm³   | 3.650e¹³ (C1)| 3.700e¹³ (C2)| 3.750e¹³ (C3)|
| D      | V_{th} Adjust Implant   | atom/cm³   | 6.940e¹² (D1)| 6.960e¹² (D2)| 6.980e¹² (D3)|

Table 2. Noise factors and their levels

| Symbol | Noise Factor            | Unit      | Level 1 | Level 2 |
|--------|-------------------------|-----------|---------|---------|
| X      | Sacrificial Oxide layer | °C        | 900     | 902     |
| Y      | P-well Implantation Temperature | °C | 850     | 852     |

3. Result and discussion

The optimized results from Taguchi Method were used to verify the predicted optimal design. The results of V_{th} were analyzed and processed in order to get the optimal design of the device.

3.1. Analysis for 22nm NMOS Device

The L9 Taguchi method analysis which consists of nine experiments is specified in the orthogonal array table. Four specimens were simulated for each of the parameter combinations. The completed response for V_{th} data is shown in Table 3

Table 3. V_{th} values for NMOS device

| Exp. No | Threshold Voltage (Volts) |
|---------|---------------------------|
|         | X1Y1 | X1Y2 | X2Y1 | X2Y2 |
| 1       | 0.319202 | 0.317181 | 0.319114 | 0.317094 |
| 2       | 0.295836 | 0.295111 | 0.295804 | 0.295079 |
| 3       | 0.283015 | 0.282119 | 0.282976 | 0.282079 |
| 4       | 0.309481 | 0.307376 | 0.309391 | 0.307286 |
| 5       | 0.288823 | 0.287997 | 0.288787 | 0.287961 |
| 6       | 0.30077 | 0.300098 | 0.300741 | 0.300069 |
| 7       | 0.31957 | 0.317453 | 0.319484 | 0.317367 |
| 8       | 0.349681 | 0.347745 | 0.349603 | 0.347667 |
| 9       | 0.31119 | 0.308995 | 0.311102 | 0.308907 |
Based on the experiment results, the control factor that has the most effect on the device characteristics can be determined. The Signal-to-noise (S/N) ratio is used to discover the optimal process parameters when analyzing the experimental data. The $V_{th}$ analysis in this experiment uses S/N ratio of nominal-the-best [18, 19].

The utilization of S/N Ratio for each level of process parameters is to make the design more accurate. Regardless of the category of the performance characteristic, the larger the S/N Ratio resulted the better the performance characteristic. Therefore, the optimal level of the process parameters is the level with the highest S/N Ratio [20, 21].

The S/N Ratio is selected in order to obtain a threshold voltage value which is close or equal to the given target value (0.306V), which is also known as nominal value according to ITRS specification [22]. The S/N Ratio (Nominal-the-best), $\eta$ can be expressed as [19]:

$$\eta = 10 \log_{10} \frac{\mu^2}{\sigma^2}$$  \hspace{1cm} (1)

Where:

$$\mu = \frac{Y_1 + \ldots + Y_n}{n}$$  \hspace{1cm} (2)

$$\sigma^2 = \frac{\sum_{i=1}^{n} (Y_i - \mu)^2}{n-1}$$  \hspace{1cm} (3)

Where $n$ is number of tests, $Y_i$ is the experimental value of the threshold voltage, $\mu$ is mean and $\sigma$ is variance. For nominal-the-best analysis, there are two types of factor of interest which are the dominant and the adjustment factors. By applying (2)-(4), the $\eta$ for each device were calculated and given in Table 4 [19].

| Exp No. | Mean     | Variance   | S/N Ratio (Mean) | S/N Ratio (Nominal-the-Best) |
|---------|----------|------------|------------------|-------------------------------|
| 1       | 3.18E-01 | 1.36E-06   | -9.95E+00       | 48.71                        |
| 2       | 2.95E-01 | 1.76E-07   | -1.06E+01       | 56.97                        |
| 3       | 2.83E-01 | 2.68E-07   | -1.10E+01       | 54.73                        |
| 4       | 3.08E-01 | 1.48E-06   | -1.02E+01       | 48.08                        |
| 5       | 2.88E-01 | 2.28E-07   | -1.08E+01       | 55.62                        |
| 6       | 3.00E-01 | 1.51E-07   | -1.04E+01       | 57.77                        |
| 7       | 3.18E-01 | 1.50E-06   | -9.94E+00       | 48.31                        |
| 8       | 3.49E-01 | 1.25E-06   | -9.15E+00       | 49.87                        |
| 9       | 3.10E-01 | 1.61E-06   | -1.02E+01       | 47.76                        |

Referring to Table 4, rows 2, 3, 5 and 6 gives a S/N Ratio value of 56.97 dB, 54.73 dB, 55.62 dB and 57.77 dB respectively. This indicates that the process parameter combinations in these rows give the best insensitivity for the response characteristics. Since the experimental design is orthogonal, the effect of each process parameter on the S/N Ratio at different levels can be separated out.

The S/N Ratio for each level of the process parameters are summarized in Table 5. In addition, the total mean of the S/N Ratio for the experiments are also calculated and listed in Table 5.
Table 5. S/N ratio for the threshold voltage

| Symbol | Process Parameter           | S/N Ratio (Mean) | Total Mean S/N | Max - Min |
|--------|-----------------------------|------------------|----------------|-----------|
| A      | Halo Implantation           | 53.47 53.82 48.65 | 51.98          | 5.17      |
| B      | S/D Implantation            | 48.37 54.15 53.42 | 5.78           |
| C      | Compensation Implantation   | 52.12 50.94 52.89 | 51.98          | 1.95      |
| D      | $V_{th}$ Adjust Implantation| 50.70 54.35 50.90 | 3.65           |

The factor effect graph for the S/N Ratio of the experiments is shown in Figure 3. The dashed line in the graph represents the values of the overall-mean of the S/N Ratio. While the line of the graphs at the top and bottom represents the S/N Ratio (Nominal-the-best) and the S/N Ratio (Mean) respectively. In the S/N Ratio analysis, the larger the S/N Ratio resulted the better the quality characteristic for the threshold voltage. Referring to the graph, from the left, the slopes correspond to the Halo Implantation (Factor A), followed by S/D implantation (Factor B), Compensation Implantation (Factor C) and lastly $V_{th}$ Adjust Implantation (factor D) respectively. The slopes show that the Halo implantation (Factor A) dose has found to be dominant factor because it has the maximum S/N ratio since the slope is the sharpest and highest compared to the others. While the Compensation Implantation (Factor C) was found to be the adjustment factor because it has small effect on the S/N Ratio (Nominal-the-best) and in the same time has large effect on S/N Ratio (Mean).

![Figure 3. S/N graph for threshold voltage](image)

3.2 Analysis of Variance (ANOVA)

The priority of the process parameters with respect to the $V_{th}$ was investigated to determine the accuracy of the optimum combinations. The result of ANOVA for the NMOS device is presented in Table 6. The percent factor effect on S/N Ratio indicates the priority of a factor (process parameter) to reduce variation. The high percentage of a factor effect on mean contributes to the greatest influence on the stability of $V_{th}$ with respect to the noise parameters.
Table 6. Result of ANOVA

| Symbol | Process Parameter                  | Degree of Freedom | Sum of Square | Mean square | Factor Effect on S/N Ratio (%) | Factor Effect on Mean (%) |
|--------|-----------------------------------|-------------------|---------------|-------------|-------------------------------|---------------------------|
| A      | Halo Implantation                 | 2                 | 50            | 25          | 36                           | 46.20                     |
| B      | S/D Implantation                  | 2                 | 60            | 30          | 42                           | 16.38                     |
| C      | Compensation Implantation         | 2                 | 6             | 3           | 4                            | 34.06                     |
| D      | $V_{th}$ Adjust Implantation      | 2                 | 25            | 13          | 18                           | 3.36                      |

Obviously the results show that the Halo implantation with a percentage of 46.20% has the most dominant impact to the threshold voltage of the device, followed by compensation implantation at 34.06% while 16.38% and 3.36% is owned by S/D implantation and $V_{th}$ adjust implant respectively.

3.3 Confirmation of Optimum Run

Based on all the analyzed data, it can be deduced that, the compensation implantation is said to be as an adjustment factor because it has a small effect on the S/N Ratio (Nominal-the-best) and has a large effect on the mean. As a result the value of this factor can be adjusted. The adjustments are done to get the threshold voltage as close as possible to the nominal value or the target value. The values of the control factors are varied in compliance to Taguchi method until the best result is achieved. The best predicted setting by Taguchi method for the process parameters for the device is shown in Table 7.

Table 7. Best setting of the process parameters

| Symbol | Process Parameter                  | Unit    | Level | Best Value            |
|--------|-----------------------------------|---------|-------|-----------------------|
| A      | Halo Implantation                 | atom/cm$^3$ | 2     | 1.275e13              |
| B      | S/D Implantation                  | atom/cm$^3$ | 1     | 5.1e13                |
| C      | Compensation implantation         | atom/cm$^3$ | -     | Sweep (3.65 e13 to 3.75e13) |
| D      | $V_{th}$ Adjust Implantation      | atom/cm$^3$ | 3     | 6.98e12               |

Using the above parameters, the final simulation was performed to verify the accuracy of the prediction. By setting the Halo Implantation to Level 2, S/D Implantation to Level 2, $V_{th}$ Adjust Implantation to Level 2, the value of compensation implantation was adjusted to fall within the range of 3.65x10$^{13}$ to 3.75x10$^{13}$ in order to obtain a $V_{th}$ value that is closer to 0.306 V. The sweep that was done with the Compensation Implantation resulted in the best parameter setting of 3.67x10$^{13}$ atom/cm$^3$. These final parameters were then simulated with the noise factors to get the optimal result as noted in Table 8.

Table 8. Results of Confirmation Experiment with Added Noises

| $V_{th1}$ (n1,n1) | $V_{th2}$ (n1,n2) | $V_{th3}$ (n2,n1) | $V_{th4}$ (n2,n2) | SNR (Mean) | SNR (Nominal-the-best) |
|-------------------|-------------------|-------------------|-------------------|------------|-------------------------|
| 0.305901          | 0.303762          | 0.305811          | 0.303672          | 0.304787   | 47.8                    |

Finally, the experiment has resulted in the achievement of mean $V_{th}$ value of 0.304787 V with the S/N Ratio of 47.8 dB. The values are in line with projections by ITRS 2011.
4. Conclusion
As a conclusion, the Taguchi method is a reliable method in achieving the optimum solution in fabricating nanoscale CMOS devices. The $V_{th}$ is the main response in determining the functionality of the device. The numerical fabrication of a 22 nm gate length high-k/metal gate NMOS transistor was achieved successfully. In this experiment, the Halo implantation dose was the strongest effect and identified as the dominant factor while the Compensation Implantation as an adjustment factor where the threshold voltage is the main response studied in this experiment. By adding noise factors to the design, a more robust device design can be attained.

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