An Analog Signal Processing EIC-PIC Solution for Coherent Data Center Interconnects

Shivangi Chugh, Rakesh Ashok, Punit Jain, Sana Naaz, Aboobackkar Sidhique, and Shalabh Gupta

Abstract—Data center interconnects (DCIs) will have to support throughputs of 400 Gbps or more per wavelength in the near future. To achieve such high data rates, coherent modulation and detection is used, which conventionally requires high-speed data conversion and signal processing in the digital domain. Alternatively, high-speed signal conditioning and processing could be carried out in co-designed photonic and electronic integrated circuits, in the optical and electrical analog domains, respectively, to achieve reduced power consumption, latency, form factor, and cost. A few demonstrations of analog domain processing electronic integrated circuits (EICs), including those of equalizer and carrier phase recovery (CPR) modules showcase progress in this direction in the literature. In this brief, for the first time, we present integration of a silicon photonic integrated coherent receiver (ICR) module with a CPR module, as a part of a complete coherent receiver solution. A phase shifter in the ICR (fabricated in a 220 nm silicon on-insulator technology) receives feedback from a CPR EIC, and the combination compensates for the time varying phase offset between the modulated signal and the unmodulated carrier in the closed loop configuration. In this proof-of-concept demonstration, we present experimental results obtained from the stand-alone silicon photonic ICR along with its system level integration with CPR chip, for QPSK signals. The technique can be extended to a higher-order modulation format, such as 16-QAM, for data rate scaling. The proposed scheme is suitable for homodyne systems, such as polarization multiplexed carrier based self-homodyne links.

Index Terms—Silicon photonic integrated circuits, integrated coherent receiver, analog signal processing, SiGe integrated circuits, phase shifter, phase detector.

I. INTRODUCTION

There has been a growing interest towards using coherent modulation and detection in data center interconnects (DCIs) for supporting the ever growing Internet traffic [1,2], due to the inherent advantages of the coherent techniques [3]. Even though the coherent links possess a multitude of advantages, they also pose major challenges associated with dispersion, laser phase/frequency offsets, and non-zero laser linewidth. The impairments due to these effects are conventionally overcome using digital signal processing. However, the severity of the impairments introduced in the DCIs is not as significant as that in the long-haul links. Therefore, the power hungry data conversion and digital signal processing based approach can be avoided and substituted by optical domain processing and analog signal processing (ASP) for considerable power, complexity, form-factor, and latency reduction [4]. The enhanced energy efficiency and reduced complexity in the ASP approach are attributed to the omission of analog to digital converters (ADCs) and massive number of operations in digital signal processors (DSPs). In the literature, all-analog coherent receiver solutions compensating for dispersion and laser offsets are presented in [1,3,5-7]. When projected to the 400ZR standard, the ASP approach implemented in a 7 nm FinFET technology can save ~3.6 W compared to its digital counterpart [5].

Major requirements for next-generation DCIs include high power efficiency, high bandwidth, high reliability, small form factor, low latency, and low cost. A photonic integrated circuit (PIC) comprising optical components along with electronics integrated on a chip can make the entire solution very efficient. Monolithic integration on silicon is lately gaining popularity, mainly due to low-cost manufacturing and maturity of CMOS fabrication processes [8]. The combination of a silicon photonic integrated circuit (SiPIC) with analog electronic integrated circuits (EICs) is expected to bring down the form-factor, power consumption, and cost of transceivers in coherent DCIs.

Earlier, a 16-QAM coherent DCI transmitter demonstrated in [9], has an integrated PIC designed in silicon-on-insulator (SOI) with EIC designed in SiGe BiCMOS platforms supports 552 Gb/s/λ. A 56 Gb/s SiPIC transmitter in 3D-Integrated PIC25G and ST-55 nm SiGe BiCMOS technology is presented in [10]. An SiPIC coherent receiver comprising all optical components and trans-impedance amplifiers (TIAs) on the same chip for dual-polarization QPSK links has been demonstrated in [11,12]. A quasi-coherent optical receiver, designed in 130 nm SiGe BiCMOS technology with major components being PIN detectors, TIAs, envelope detectors, and limiting amplifiers for 28 Gbaud has been demonstrated in [13].

This work presents the demonstration of a SiPIC integrated coherent receiver (ICR) in a Costas loop with carrier phase recovery (CPR) chip (the stand-alone CPR chip has been fabricated in a 220 nm silicon-on-insulator technology) receives feedback from a CPR EIC, and the combination compensates for the time varying phase offset between the modulated signal and the unmodulated carrier in the closed loop configuration. In this proof-of-concept demonstration, we present experimental results obtained from the stand-alone silicon photonic ICR along with its system level integration with CPR chip, for QPSK signals. The technique can be extended to a higher-order modulation format, such as 16-QAM, for data rate scaling. The proposed scheme is suitable for homodyne systems, such as polarization multiplexed carrier based self-homodyne links.

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presented earlier in [5]). Functional validation of the EIC-PIC receiver has been performed for the QPSK homodyne link. This Costas loop aims at removing the time varying phase offset between the modulated and local oscillator signals, for reliable recovery of data in coherent homodyne systems, especially in a polarization multiplexed carrier based self-homodyne (PMC-SH) links [14]. The EIC-PIC ASP based coherent receiver exhibits an essential step in the direction of achieving highly efficient DCIs.

II. SYSTEM DESIGN AND OVERVIEW

The proposed conceptual ASP receiver architecture that can be monolithically integrated for providing a complete solution for PMC-SH based DCI is shown in Fig. 1. A generic ASP receiver architecture for polarization division multiplexed system with laser phase/frequency offset is detailed in [1] [5]. The modulated signal (S) and unmodulated carrier (LO) from the received signal are separated with the aid of an adaptive polarization controller consisting of an electronic polarization controller, polarization beam splitter, power splitter, photodetector, and adaptive polarization control circuit [14]. The polarization segregated optical signals S and LO are given to the ICR. The electrical signals from the ICR output after the TIAs are given to the analog processing and control unit. Laser offsets, dispersion, and clock misalignments are corrected using CPR, equalizer, and clock and data recovery circuits, respectively, which are the major constituents of the analog processing and control unit. For longer channel lengths, equalization can be used prior to CPR for correcting the massive dispersion introduced.

The architecture of the ASP coherent receiver is shown in Fig. 2. The system comprises an SiPIC ICR and an SiGe analog domain CPR EIC. The ICR receives a modulated signal \( S = \exp \{ j(\omega_s t + \phi_m(t) + \phi_s(t)) \} \) and an unmodulated carrier \( \text{LO} = \exp \{ j(\omega_{\text{LO}} t + \phi_{\text{LO}}(t)) \} \) at the S and LO ports, respectively. Here, \( \omega_s, \phi_m, \phi_s, \omega_{\text{LO}}, \) and \( \phi_{\text{LO}} \) denote frequency of the carrier laser, message phase, random phase fluctuations of the carrier laser, frequency of the LO laser, and random phase fluctuations of LO laser, respectively. These signals are given to the 90\(^\circ\) optical hybrid and electric fields at various nodes of 90\(^\circ\) optical hybrid are \( E_1 = S/\sqrt{2}, \) \( E_2 = -jS/\sqrt{2}, \) \( E_3 = -j\text{LO}/\sqrt{2}, \) \( E_4 = \text{LO}/\sqrt{2}, \) \( E_5 = -j\text{LO}/\sqrt{2}, \) \( E_6 = (S + \text{LO})/2, \) \( E_7 = (S - \text{LO})/2, \) \( E_8 = (S + j\text{LO})/2, \) and \( E_9 = (S - j\text{LO})/2. \) The outputs of the hybrid are given to the photodetectors for generating the (normalized) photocurrents \( I_1 = 1 + \cos((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)), \) \( I_2 = 1 - \cos((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)), \) \( I_3 = 1 + \sin((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)), \) and \( I_4 = 1 - \sin((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)). \) The balanced photodetector (BPD) stage removes DC (from \( I_1 \) to \( I_4 \)) and provides differential currents, which are subsequently converted into voltage signals \( I_1 = \cos((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)) \) and \( I_4 = \sin((\omega_s - \omega_{\text{LO}})t + \phi_m(t) + \phi_s(t) + \phi_{\text{LO}}(t)). \) These signals are given to the CPR comprising a cross-correlator phase detector (PD) and the inputs to the PD are \( I_O = \cos[\phi_m(t) + \phi_{\text{err}}(t)] \) and \( Q_O = \sin[\phi_m(t) + \phi_{\text{err}}(t)], \) where \( \phi_{\text{err}}(t) = (\omega_s - \omega_{\text{LO}})t + \phi_s(t) + \phi_{\text{LO}}(t) \) denotes the cumulative phase error in \( I_O \) and \( Q_O. \)

In the case of frequency synchronized links, such as PMC-SH links, \( \omega_s = \omega_{\text{LO}}. \) The PD output, \( V_{pd} \approx \phi_{\text{err}}(t) \) for \( \phi_{\text{err}}(t) \in (-\pi/4, \pi/4). \) The \( V_{pd} \) signal is given to the phase shifter (PS) of SiPIC in \( L_O \)’s path through a loop filter (LF) so that the phase delay \( (\phi_{\text{pd}}) \) added to \( L_O \) by the PS is equal and opposite to \( \phi_{\text{err}}(t). \) In the closed loop, \( \phi_{\text{pd}}(t) = -\phi_{\text{err}}(t) = -|\phi_s(t) + \phi_{\text{LO}}(t)|, \) thus compensating for the phase error. The LF averages \( V_{pd} \) and stabilizes the loop. Under the closed loop condition, at steady state, \( I_O = \cos[\phi_m(t)] \) and \( Q_O = \sin[\phi_m(t)], \) which are the desired message phases after phase error correction and are used for data recovery in further steps using equalizer and clock and data recovery circuits.

III. EIC AND PIC DESIGN

The presented scheme comprises two application-specific integrated circuits: an SiPIC ICR and an SiGe CPR EIC, the details of which are provided in the following subsections.
The SiPIC ICR is designed and fabricated in IMEC’s ISIPP50G process, which is an SOI technology and is a suitable candidate for monolithic integration with EIC technologies [15]. The micrograph of the ICR is shown in Fig. 2(b). The chip comprises multiple designs, among which ICR is focused in this work. Here, the SiPIC design is specific for C-band transverse electric electric operation. Major building blocks of SiPIC ICR are vertical grating couplers (VGCs), 90° hybrid, and BPDs. SiPIC uses VGCs for surface coupling of optical signals to the chip. The PS, an important section of the ICR, is characterized using an interferometer structure shown in Fig. 3(a). The PS has a half-wave voltage \( V_{th} \) of \( \sim 6 \) V, corresponding to the minimum output power, as shown in the characterization result in Fig. 3(a). The 90° optical hybrid is made up of two 1×2 multi-mode interferometers (MMIs), a PS, and two 2×2 MMIs. The salient features of the components used in the design are summarized in Table I. A 50 Ω load resistor is provided at the output of each BPD pair to convert the photocurrent into voltage and to enable matching for high frequency signaling. The ICR structure has two RF ports for each in-phase and quadrature-phase signal, arranged in ground-signal-ground format. Supply, ground, and bias DC pads are wire bonded on a printed circuit board (PCB).

**Characterization of SiPIC ICR:** The experimental setup used for characterizing the proof-of-concept SiPIC ICR is shown in Fig. 5. A 1550 nm laser output is split using a power splitter, one of the outputs of which is QPSK modulated by 4 Gbaud electrical signals generated by an arbitrary waveform generator (AWG), while other acts as LO. The S and LO’ signals are mixed in SiPIC ICR to generate I and Q electrical signals shown in Fig. 5(a). The PS is not biased as the feedback is not essential in this characterization. The data rate, in this case, is mainly constrained by the probes used to extract electrical signals from the ICR. The I and Q signals recorded through oscilloscope are subjected to post-processing through behavioral carrier phase recovery and compensation and equalization in sequence and the corresponding results are shown in Figs. 6(b) and (c), respectively.

### A. SiPIC ICR chip

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![SiPIC ICR chip diagram](image)

### B. SiGe CPR chip

The micrograph of analog domain CPR chip designed in ST-130 nm BiCMOS \( (f_i = 230 \text{ GHz and } f_{max} = 280 \text{ GHz}) \) is shown in Fig. 4(c). The chip occupies an area of 1.2 mm \( \times \) 1.2 mm consisting of a total number of 36 pads. The chip is designed for 25 Gbaud QPSK and 16-QAM modulation formats with all the individual circuits to have a bandwidth (BW) of at least 0.7 times the desired baud rate and 400 mVpp differential swing. The major constituents of this chip are SSB mixer and PD, which in turn comprise limiting amplifiers, delay cells, multipliers, adders, buffers, and biasing circuits, the key characteristics of which with 50 Ω load are presented in Table II. The schematics of these differential circuits (made up of BJTs and MOSFETs), design, and simulation results are detailed in [16]. The cross-correlator PD generates a voltage proportional to the phase error in the input signals. The PD of the CPR chip, which is the effective section of the chip used for the demonstration, consumes \( \sim 412 \) mW power. The PD is characterized using the setup shown in Fig. 3(b) by feeding 1 Gbaud QPSK modulated data with a frequency offset of 1 MHz. The PD output has saw-tooth characteristics with a phase periodicity of \( \pi/2 \) and gain of 0.16 V/rad, as shown in Fig. 3(b). The input and output differential high frequency signals are arranged in ground-signal-ground format with \( \sim 100 \) Ω differential source and load impedances supporting 25 Gbaud signaling. This chip’s functionality with discrete components and commercial InGaAs ICR has been demonstrated in [16] [17].
IV. PROOF-OF-CONCEPT DEMONSTRATION

The proposed EIC-PIC ASP coherent receiver is validated for proof-of-concept, at 2 GBaud with QPSK homodyne optical link. Figure 7(a) shows the experimental setup used for demonstrating the proposed approach. A C-band, continuous wave, single frequency, and external cavity laser output is split using a 3-dB power splitter to provide a carrier to the IQ modulator at the transmitter and an LO for coherent detection at the receiver for ensuring no frequency offset and drift between S and LO. The $I_{data}$ and $Q_{data}$ (PRBS-7) message signals generated by an AWG modulate the carrier using an IQ modulator. The modulated optical signal is transmitted over a 10 m SMF channel, which results in time varying phase offset between S and LO. The modulated signal’s polarization is adjusted using a polarization controller (PC) and applied to the S port of the SiPIC ICR through VGC. The unmodulated carrier is applied to the LO port using another VGC through PC to control the polarization. The receiver comprises SiPIC ICR, amplifiers, balanced to unbalanced lines (baluns), SiGe CPR chip, and LF arranged in a feedback loop structure. LO is given to the hybrid through a PS to control its phase in the closed loop. The PS in the hybrid is biased to provide a phase shift of $\pi/2$ to the LO. Outputs from the hybrid are given to the BPD pairs, biased with $-1$ V and $1$ V supply to generate photocurrents comprising details of message phase, message amplitude, and cumulative phase error. Interconnection of SiPIC ICR and SiGe CPR with their corresponding test PCBs is illustrated in Fig. 7(b).

The SiPIC experimental setup on a probe station is shown in Fig. 7(c). The optical signals are coupled to the ICR through a fiber array while the electrical signals are wire-bonded on SiPIC PCB. The coupling of the S and LO optical signals from the fiber array is controlled through a mechanical probe arm, which is monitored manually. The in-phase (I) and quadrature-phase (Q) outputs of SiPIC have a swing of $\sim 5$ mV$_{pp}$ with corresponding maximum BPD photocurrents of $\sim 300$ µA.

The electrical I and Q signals obtained at the output of SiPIC ICR are amplified (using an amplifier of gain $\approx 25$ dB) and then converted into differential signals using baluns (insertion loss $\approx 3$ dB) that give out unbalanced outputs, which are 3 dB below both I and Q signals. The amplification and balanced to unbalanced conversion are essential as the CPR chip requires a minimum differential swing of 50 mV$_{pp}$ at its inputs for its operation.

Figure 7(d) shows the experimental setup of the CPR chip. The aluminum pads of the CPR chip are (gold) wire bonded to electroless nickel immersion gold tracks on a four-layer PCB fabricated on an FR-4 substrate. The high frequency input/output signals are fed/extracted through subminiature version-A connectors while supply, ground, and bias connections are provided through berg-stick connectors. The differential signals $I_1$ ($= I_{op} - I_{on}$) and $Q_1$ ($= Q_{op} - Q_{on}$) are fed to the CPR chip. The chip gives output $I_O$ ($= I_{op} - I_{on}$), $Q_O$ ($= Q_{op} - Q_{on}$), and $V_{pd}$ ($= V_{pdn} - V_{pdf}$). The $V_{pd}$ signal is given to the PS through the LF, which translates the voltage levels of $V_{pd}$ to voltage levels required for PS, averages $V_{pd}$, and stabilizes the loop. The voltage waveforms at the CPR chip output are recorded in open loop and closed loop conditions.

Figure 8 presents the constellation and eye-diagrams of experimental results obtained with the proposed architecture. The open loop constellation points shown in Fig. 8(a) rotate...
with time due to continuously varying phase offset between $S$ and $LO$. The constellation settles when the receiver loop is closed as the phase offset between $S$ and $LO$ is corrected, as shown in Fig. 8(b). The closed loop signals are equalized to compensate for the frequency dependent losses and hence reduce the error vector magnitude through post-processing, as shown in Fig. 8(c), which are further used for data recovery. Eye diagrams of the measured quadrature-phase signals are presented in Figs. 8(d)–(f) and similar plots can be obtained for in-phase signals too. The eye is closed in open loop condition (Fig. 8(d)) due to time varying phase offsets, while it gets opened in the closed loop condition (Fig. 8(e)) after the phase offset correction. Horizontal and vertical eye openings are increased post-equilalization, as shown in Fig. 8(f). Single stage analog domain equalizers [18] or their cascade combination can be used for the equalization. The data rate of measurement was constrained by the limited constant gain frequency range of the amplifiers connecting the ICR and baluns. The baluns made up of transformers are wire bonded to the PCBs, which have inherent parasitic inductances, limiting the frequency of operation. These factors retrain the data rate of the demonstration even though the SiPIC ICR and SiGe CPR are designed to operate for 50 Gbaud and 25 Gbaud, respectively. Although both the chips are compatible with 16-QAM modulation scheme, signal to noise ratio (SNR) of the PIC restricts the operation of the chip to QPSK modulation format. With the aid of linear TIAs (currently not shown in Fig. 7(a)) at the output of ICR, the cumulative SNR of the system can be improved and hence higher order modulation formats and data rate can be attained. The data rate of the assembly can be enhanced by using high gain wide frequency range amplifiers, broadband baluns, efficient optical coupling, and flip-chip bonded ICs. In addition, the overall baud rate of the EIC can be enhanced by designing the circuits in advanced CMOS/FinFET technology nodes.

V. Conclusion

We have presented an EIC-PIC codesigned analog coherent receiver solution for near-future DCIs. The proof-of-concept demonstration results of SiPIC ICR integrated with CPR chip at system level for QPSK modulation scheme are promising. Since both the ICs are designed to function with 16-QAM for higher data rates, the throughput per wavelength per polarization per channel can be increased by system level optimization. Electronic and photonic integration on a single chip or in a single package can result in compact and energy efficient solutions for high-speed data center interconnects.

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