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Tunnel field-effect transistor with two gated intrinsic regions

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In this paper, we propose and validate (using simulations) a novel design of silicon tunnel field-effect transistor (TFET), based on a reverse-biased p+p-n-n+p structure. 2D device simulation results show that our devices have significant improvements of switching performance compared with more conventional devices based on p-i-n structure. With independent gate voltages applied to two gated intrinsic regions, band-to-band tunneling (BTBT) could take place at the p-n junction, and no abrupt degenerate doping profile is required. We developed single-side-gate (SSG) structure and double-side-gate (DSG) structure. SSG devices with HfO2 gate dielectric have a point subthreshold swing of 9.58 mV/decade, while DSG devices with polysilicon gate electrode material and HfO2 gate dielectric have a point subthreshold swing of 16.39 mV/decade. These DSG devices have ON-current of 0.255 μA/μm, while that is lower for SSG devices. Having two nano-scale independent gates will be quite challenging to realize with good uniformity across the wafer and the improved behavior of our TFET makes it a promising steep-slope switch candidate for further investigations. © 2014 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License. [http://dx.doi.org/10.1063/1.4889889]

I. INTRODUCTION

Power consumption is one of the major challenges blocking further development of complementary metal-oxide-semiconductor (CMOS) technologies, since the subthreshold leakage current increases exponentially with decreasing supplying voltage due to the 60 mV/decade limit of subthreshold swing at room temperature. TFET is one of the most promising candidates to replace CMOS devices in low-power and low-standby-power application because of small subthreshold swing and low OFF-state leakage current.1–3 Current of TFETs is controlled by tunneling mechanism between source and channel which is not sensitive to temperature, so TFETs are more immune to short-channel effects than CMOS devices4 and they can be used at high temperature.1, 2

For conventional TFETs based on p-i-n structure, abrupt degenerate doping profile on the source side is critical for sufficient large tunneling probability and good gate modulation of the current.4, 5 The materials can be deposited by chemical vapor deposition (CVD), or some expensive techniques such as molecule beam epitaxy (MBE) and vapor phase deposition (VPD). Problems such as high thermal budget, random dopant fluctuation (RDF) and defects make it not easy to create the abrupt junction and degenerate doping profile.4, 6, 7

In 2011, Li et al. introduced a twin-gate electrically doped TFET on silicon nanowire where two gates surrounding the silicon nanowire are separated by oxide.8 The p-n junction is not abrupt because of the gate-to-gate oxide separation. Carrier concentration near the junction is reduced due to gate electric field interference. Therefore, this twin-gate TFET can hardly realize small subthreshold swing.

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In this work, we report a novel $p^+\text{-}p\text{-}n\text{-}n^+$ TFET design, and explain how it functions in Section II. Section III shows the device characteristics in terms of subthreshold swing and ON-current. We also compare our device with other steep subthreshold devices reported in the literature.

II. DEVICE STRUCTURE AND OPERATION

The device investigated here is a lateral $p^+\text{-}p\text{-}n\text{-}n^+$ TFET built on a thin silicon layer as schematically shown in FIG. 1. There are two gated lightly doped regions ($p$ and $n$) and two regions with higher doping concentration on the side ($p^+$ and $n^+$). The doping levels were $1 \times 10^{18}$ atoms/cm$^3$, $1 \times 10^{16}$ atoms/cm$^3$, $1 \times 10^{16}$ atoms/cm$^3$, $1 \times 10^{18}$ atoms/cm$^3$ for $p^+$, $p$, $n$, and $n^+$ regions, respectively. The thicknesses of silicon and dielectric layer were 5 nm and 1 nm, and the length of each region was 50 nm. SiO$_2$ or HfO$_2$ was used as gate dielectric material.

Similar to the $p$-$i$-$n$ TFET, our device operates when the $p$-$n$ junction is reverse-biased. Without an appropriate gate voltage the energy barrier width between the two intrinsic regions is large, and the device is in the OFF-state. As the magnitude of the positive gate voltage applied to the $n$ region and the negative gate voltage applied to the $p$ region increases, the energy bands in the $n$ region are lowered and the ones in the $p$ region are raised. There is neither a gap nor an overlap between the horizontal positions of the two gate electrodes, so abrupt $p$-$n$ junction can be obtained. Gate electric field is enhanced by having gate voltage with different polarity on the opposite side of the ultra-thin silicon body. Thus, high carrier concentration can be achieved at the $p$-$n$ junction. As a result, the tunneling barrier becomes narrower and band-to-band tunneling (BTBT) takes place at the $p$-$n$ junction between the two lightly doped regions. The names of device terminals follow that of MOSFET. For NMOS, drain voltage is positive, source is grounded, and current starts from drain and goes into source. Thus the $p^+$ region is named as “source”, and $n^+$ region is named as “drain”. The $n$ and $p$ region are “gate 1” and “gate 2”, respectively.

2D simulations were performed using Synopsis’s device simulator Sentaurus. The simulations were performed using the drift-diffusion transport model, where the electrostatic Poisson equation and the carrier continuity equations for both electrons and holes were solved. The doping-dependent mobility model, the Shockley–Read–Hall (SRH) recombination model, and the Auger recombination model were activated. Fermi statistics was used, because of high carrier concentration. Tunneling current was simulated using dynamic nonlocal path band-to-band tunneling model. The position-dependent electron and hole generation rate were different, since electrons and holes were generated nonlocally at the end of the tunneling path, and generation rate was obtained from the integration of nonlocal path. Gate leakage was neglected, and quantum confinement effect was not included in the simulation.

The gated regions are fully depleted without gate voltages. Therefore, the device performances will be the same as long as these two regions are only lightly doped or even not doped. The carrier concentration in these regions is decided by the gate voltages instead of the initial doping concentration. Two gate bias voltages are used to separate the energy bands of the $n$ and $p$ regions and accumulate carriers, which reduces the tunneling width effectively, as shown in FIG. 2(a). In order to operate the device, the $p$-$n$ junction should be reverse-biased. When the source is grounded.
and drain voltage is positive, the separation of the energy bands of the intrinsic regions becomes more significant, then the tunneling width is further reduced. The small enough tunneling width (less than 10 nm) allows tunneling current to flow, enabling the electrons in the p region to tunnel into the empty states of the n region, which is shown in FIG. 2(b).

III. RESULTS AND DISCUSSION

A. Equivalent tunnel diode behavior

Our TFETs realize BTBT at the junction between the two independent gated p and n regions without abrupt degenerate doping on the source side. The device behaviors highly depend on the gate voltages. The $I_D$-$V_D$ curves under different gate bias are provided in FIG. 3. When $V_{G1}$ is 2 V and $V_{G2}$ is -2 V, large number of electrons and holes accumulate in n and p regions respectively. In other words, degenerate n-type and p-type semiconductor are formed electrically by applying gate voltages. Under forward-biased ($V_{DS} < 0$ V), electrons can tunnel from the conduction band of the n region to the valence band of the p region, and this produces maximum tunneling current. When forward bias continues to increase, the overlap between the filled states on the n side and empty state on the p side becomes smaller, and the current drops, which is called negative differential resistance (NDR) region. In reverse-biased region ($V_{DS} > 0$ V), electrons can tunnel from the valance band of the p region into the empty states in the conduction band of the n region, which generates a large tunneling current that increases with the reverse voltage. However, when gate voltages are zero, the drain current increases exponentially before it saturates under forward bias ($V_{DS} < 0$ V), and it is very small under reverse bias ($V_{DS} > 0$ V), which indicates that the device behaves like a classical p-n diode.

B. Device characteristics

To obtain small subthreshold swing, both gate voltage sweep simultaneously. FIG. 4 shows the $I_D$-$V_{GS}$ characteristics where $V_{G1}$ and $V_{G2}$ have the same magnitude but different polarity ($V_{G2} = -V_{G1}$). Compared with devices with SiO$_2$ gate dielectric, the ones with HfO$_2$ gate oxide have even smaller subthreshold swing (as low as 9.58 mV/decade), because high-k dielectric material increases gate capacitance and then the electrical coupling between the gate and the tunneling junction is improved, which helps to further reduce subthreshold swing.
FIG. 3. $I_{DS}$-$V_{DS}$ for a SSG device with SiO$_2$ gate dielectric. The device shows tunnel diode IV characteristics with sufficient gate voltages applied (red line), while it presents classical p-n diode behaviors without gate voltages (blue line).

FIG. 4. Simulated device transfer characteristics for a SSG device with SiO$_2$ gate dielectric (dotted lines), compared with a device with HfO$_2$ gate dielectric (dashed lines), $V_S = 0$, $V_{G51} = V_{G1} - V_S = V_{G1}$ and $V_{G52} = V_{G2} - V_S = V_{G2} = -V_{G1}$.

With fabrication technology such as silicon-on-insulator and silicon-on-nothing, thin film silicon body with several nanometer thickness can be achieved. Thicker silicon body provides larger cross section, but tunneling rate drops dramatically as presented in FIG. 5. As shown in FIG. 6, when the silicon layer gets thicker, drain current drops and the subthreshold swing becomes larger. Therefore, we keep silicon body thickness as 5 nm for the following part of this paper.

For the simulation mentioned above, we assumed there is no work function difference between the gate electrode and the semiconductor. In order to increase the ON-current, DSG structure and HfO$_2$ gate dielectric were used, n$^+$ and p$^+$ doped polysilicon were chosen as gate electrode material for n and p regions respectively, and all other parameters were kept the same as the SSG device. The schematic diagram of DSG TFET is shown in FIG. 7.

On each side of the silicon body, one gate is applied with positive voltage and the other one is applied with negative voltage. The p-n junction cannot be ideally abrupt because of the gap separating two gates on the same side of silicon. Hence there is a tradeoff between higher ON-current and small subthreshold swing, as shown in FIG. 8. FIG. 9 presents the subthreshold swing for devices...
FIG. 5. Band to band generation rate for SSG devices with HfO2 gate oxide and varied silicon layer thickness, $V_{DS} = 1$ V, $V_{GS1} = -V_{GS2} = 1.5$ V.

FIG. 6. $I_{DS}$-$V_{GS1}$ curve as a function of silicon layer thickness for SSG devices with HfO2 gate oxide $V_{DS} = 1$ V, and $V_{GS2} = -V_{GS1}$.

with different structures and different gate dielectric materials. The average subthreshold swing is define as: 

$$S_{avg} = \frac{V_t - V_{off}}{\log I_t - \log I_{off}}$$ 

(1)
FIG. 7. A schematic diagram of the DSG p+–p-n-n+ TFET. On each side of silicon body, two gates applied with different voltages are separated by 1nm gap.

FIG. 8. Comparison of the simulated device transfer characteristics for SSG devices with SiO2 gate dielectric (dotted lines), SSG devices with HfO2 gate dielectric (dash lines), and DSG device with HfO2 gate dielectric (solid lines).

FIG. 9. Point and average subthreshold swing as a function of drain-to-source voltage for devices with different structures and different gate dielectric materials.
where threshold voltage $V_t$ is the gate voltage corresponding to drain current of $1 \times 10^{-9}$ A/μm, $V_{off}$ is the OFF-state voltage, and $I_{off}$ is the OFF-state drain current. The ratio $I_{on}/I_{off}$ is about $4 \times 10^{10}$ at $V_{DD} = 1$ V, where $I_{on}$ is defined as the drain current when $V_{GS1} = -V_{GS2} = V_{DD}$.

C. Discussion

In FIG. 10, we compare transfer characteristics for different silicon TFET from simulation and experiment with the magnitude of drain-to-source voltage equals to 1 V.\textsuperscript{1, 5, 7, 12–14} The DSG n++-n-p-p+ device with HfO$_2$ gate dielectric proposed in this paper provides a small subthreshold swing. Here, we need to notify that device simulation using nonlocal BTBT model of Silvaco Altas could have overestimated ON-current by two or more order of magnitude, but it can provide a good relative results for varied parameters.\textsuperscript{2} Also, simple BTBT model of Sentaurus predicts a nonzero generation rate even in equilibrium, which will cause current to be incorrectly estimated.\textsuperscript{9} That’s why some simulations of TFET give higher current.

For 5 nm crystalline silicon layer the quantum confinement effect is weak and it is not necessary to be include in the simulation. We can calculate the magnitude of band gap given as\textsuperscript{15}

$$E_{Gap}(D) = E_{Gap}(\infty) + \frac{A}{D^2} \text{eV} \cdot \text{nm}^2,$$

where the band gap of the bulk silicon material $E_{Gap}(\infty) = 1.12$ eV, $D$ is the thickness of silicon layer, and $A = 0.35$ for silicon. When the silicon layer is 5 nm, the band gap of the confined layer is 1.134 eV, so the band gap expansion is small compared to the thermal energy of 26 meV and it can be neglected.

Fabrication process of double-gate TFETs such as vertical double-gate TFET achieved by MBE growth gives us an insight into the fabrication of our device.\textsuperscript{16} Although it is challenge to realize the two nano-scale independent gates, our TFETs have potentials for low-power analog, digital and RF application.\textsuperscript{17–19}

IV. CONCLUSION

We proposed p+-p-n-n+ TFETs with two gated regions, discussed the operation and the simulation. Two independently controlled gate regions provide more flexibility and significant improvement of the switching performance. With SiO$_2$ gate dielectric, the point subthreshold swing of our SSG TFET is much lower than 60 mV/decade thermal limit of MOSFET. With HfO$_2$ gate dielectric...
dielectric, our simulated SSG TFET has a point subthreshold swing as low as 9.58 mV/decade at \( V_{DS} = 1 \) V, while the DSG device has a point subthreshold swing of 16.39 mV/decade, depending on how the two gate voltages are applied. The improved behavior of our TFETs makes them promising for low-power and low-standby-power applications.

1 A. M. Ionescu and H. Riel, *Nature* **479**, 329 (2011).
2 K. Boucart, Ph.D. thesis, École Polytechnique Fédérale de Lausanne, 2010.
3 Lingquan Wang, E. Yu, Taur Yuan, and P. Asbeck, *Electron Device Letters*, *IEEE* **31**, 431 (2010).
4 M. J. Kumar and S. Janardhanan, *IEEE Trans. Electron Device* **60**, 3285 (2013).
5 V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, *IEEE Trans. Electron Device* **55**, 1013 (2008).
6 S.-Y. Park, R. Anisha, Paul R. Berger, R. Loo, Nguyen Ngoc Duy, S. Takeuchi, and M. Caymax, *IEEE Electron Device Lett.* **30**, 1173 (2009).
7 K. Boucart and A. M. Ionescu, *IEEE Trans. Electron Device* **54**, 1725 (2007).
8 Li Xiang, Chen Zhixian, Shen Nansheng, D. Sarkar, N. Singh, K. Banerjee, Lo Guo-Qiang, and Kwong Dim-Lee, *Electron Device Letters*, *IEEE* **32**, 1492 (2011).
9 Sentaurus Device User Guide (Synopsys Inc., Santa Clara, CA, 2013).
10 *Simulation of a Simple GaAs Tunnel Diode for Multijunction Solar Cells.* (Synopsys Inc., Santa Clara, CA, 2013).
11 Ben G. Streetman and Sanjay Kumar Banerjee, *Solid State Electronic Devices*, 6th ed. (Prentice Hall, Upper Saddle River, New Jersey, 2005), pp. 508–512.
12 C. Hu, D. Chou, P. Patel, and A. Bowonder, in *Proceedings of the 2008 International Symposium on VLSI Technology, Systems and Applications* (2008), pp. 14–15.
13 K. Jeon, Ph.D. thesis (University of California, Berkeley, 2012).
14 C. Le Royer and F. Mayer, in *Proceedings of the 10th International Conference on Ultimate Integration of Silicon* (March 2009), pp. 53–56.
15 E. G. Barbacigiani, D. J. Lockwood, P. J. Simpson, and L. V. Goncharova, *J. Appl. Phys.* **111**, 034307 (2012).
16 A. Tura, Zhenning Zhang, Liu Peichi, Ya-Hong Xie, and J. C. S. Woo, *Electron Devices, IEEE Transactions on* **58**, 1907 (2011).
17 A. R. Trivedi, S. Carlo, and S. Mukhopadhyay, in *Proceeding of the 50 th Design Automation Conference* (DAC) (2013), pp. 1–6.
18 Liu Huichu, S. Datta, and V. Narayanan, in *Proceeding of 2013 IEEE International Symposium on Low Power Electronics and Design (ISLPED)* (2013), pp. 145–150.
19 Y. Khatami and K. Banerjee, *Electron Devices, IEEE Transactions on* **56**, 2752 (2009).