Well-Posed Models of Memristive Devices

Tianshi Wang and Jaijeet Roychowdhury
Department of EECS, University of California, Berkeley
Memristor: the missing element

- 1971: postulated by Leon Chua
- 2008: “invented” by Stan Williams et al, HP Labs
Memristive Devices & Applications

**devices**
UMich, Stanford, HP, HRL Labs, Micron, Crossbar, Samsung, ...

**applications**
- nonvolatile memories
- FPAAs
- neuromorphic circuits
- oscillators

**Compact Models**
- Linear/nonlinear ion drift models
  Biolek (2009), Jogelkar (2009), Prodromakis (2011)
- UMich RRAM model (2011)
- TEAM model (2012)
- Simmons tunneling barrier model (2013)
- Yakopcic model (2013)
- Stanford/ASU RRAM model (2014)
- Knowm "probabilistic" model (2015)

none works in DC

Verilog-A problems
idt(), $bound_step, $abstime, @initial_step, $rdist_normal, ...
Verilog-A problems

DC failures

- problematic physics
- poor understanding of VA
- ill-posed models
Good Compact Models

• “Simulation-ready”
  - run in all analyses (DC, AC, TRAN, homotopy, PSS, …)
  - run in all simulators consistently

• Well-posed
  - a solution exists
  - the solution is unique
  - the solution's behavior changes continuously with the initial conditions.

https://en.wikipedia.org/wiki/Well-posed_problem
Challenges in Memristor Modelling

- hysteresis
  - internal state variable
- model internal unks in Verilog-A
  - use potentials/flows
- upper/lower bounds of internal unks
  - physical distance
  - clipping functions
- smoothness, continuity, finite precision issues, ...
How to Model Hysteresis Properly

\[ ipn = f(vpn) \]

\[ ipn = f_1(vpn, s) \]

\[ \frac{d}{dt}s = f_2(vpn, s) \]

Example:

\[ f_1(vpn, s) = \frac{vpn}{R} \cdot (1 + \tanh(s)) \]

\[ f_2(vpn, s) = vpn - s^3 + s \]

multiple stability and abrupt change in DC sols

internal state variable “memory”
How to Model Hysteresis Properly

Template:

\[ \text{ipn} = f_1(\text{vpn}, s) \]

\[ \frac{d}{dt}s = f_2(\text{vpn}, s) \]

ModSpec:

\[ \text{ipn} = \frac{d}{dt}q_e(\text{vpn}, s) + f_e(\text{vpn}, s) \]

\[ 0 = \frac{d}{dt}q_i(\text{vpn}, s) + f_i(\text{vpn}, s) \]

\[ 0 = \frac{d}{dt}\begin{cases} f_1 & \text{if } s > 0 \\ -s & \text{if } s < 0 \end{cases} \]

![Electrical circuit diagram](image1)

![Graphs showing hysteresis behavior](image2)
How to Model Hysteresis Properly

homotopy

top

side

T. Wang, J. Roychowdhury, University of California at Berkeley

Slide 9
**Internal Unknowns in Verilog-A**

**Template:**
\[
\begin{align*}
\text{ipn} &= f_1 (\text{vpn}, s) \\
\frac{d}{dt}s &= f_2 (\text{vpn}, s)
\end{align*}
\]

**Example:**
\[
\begin{align*}
f_1 (\text{vpn}, s) &= \frac{\text{vpn}}{R} \cdot (1 + \tanh(s)) \\
f_2 (\text{vpn}, s) &= \text{vpn} - s^3 + s
\end{align*}
\]

**DO NOT**
- declare internal unks as "\texttt{real}" variables
- code time integration inside model
  \(\rightarrow\) with $\texttt{abstime}$, \texttt{@initial_step} and memory states
- use \texttt{idt()}
- use implicit contributions
  \(\rightarrow\) unless you know what you are doing
\[ \text{ipn} = \frac{\text{vpn}}{R} \cdot (1 + \tanh(s)) \]

\[ \frac{d}{dt}(\tau \cdot s) = \text{vpn} - s^3 + s \]

Internal Unknowns in Verilog-A

1 `include "disciplines.vams"
2 module hys(p, n);
3     inout p, n;
4     electrical p, n, ns;
5     parameter real R = 1e3 from (0:inf);
6     parameter real k = 1 from (0:inf);
7     parameter real tau = 1e-5 from (0:inf);
8     real s;
9
10     analog begin
11         s = V(ns, n);
12         I(p, n) <+ V(p, n)/R * (1+tanh(k*s));
13         I(ns, n) <+ V(p, n) - pow(s, 3) + s;
14         I(ns, n) <+ ddt(-tau*s);
15     end
16 endmodule
**RRAM Model**

**Template:**

\[
ipn = f_1(vpn, s) \quad \text{RRAM:} \quad f_1(vpn, Gap) = I_0 \cdot e^{-\text{Gap}/g^0} \cdot \sinh(vpn/V_0)
\]

\[
\frac{d}{dt} s = f_2(vpn, s) \quad f_2(vpn, Gap) = -v_0 \cdot \exp(-\frac{E_a}{V_T}) \cdot \sinh\left(\frac{vpn \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T}\right)
\]

Jiang, Z., Wong, H. (2014). Stanford University Resistive-Switching Random Access Memory (RRAM) Verilog-A Model. nanoHUB.

\[
\text{minGap} \leq \text{Gap} \leq \text{maxGap}
\]

**Diagram:**

- If \(\text{gap} < \text{minGap}\), set \(\text{gap} = \text{minGap}\);

**Hybrid model**
RRAM Model

Template:

\[
\begin{align*}
\text{ipn} &= f_1(\text{vpn}, s) \\
\frac{d}{dt}s &= f_2(\text{vpn}, s)
\end{align*}
\]

RRAM:

\[
\begin{align*}
f_1(\text{vpn}, \text{Gap}) &= I_0 \cdot e^{-\frac{\text{Gap}}{g_0}} \cdot \sinh(\text{vpn}/V_0) \\
f_2(\text{vpn}, \text{Gap}) &= -v_0 \cdot \exp(-\frac{E_a}{V_T}) \cdot \sinh(\frac{\text{vpn} \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T}) \\
&\times F_{\text{window}}(\text{Gap})
\end{align*}
\]

Biolek, Jogelkar, Prodromakis, UMICH, TEAM/VTEAM, Yakopcic, etc.
RRAM Model

Analogy: MEMS switch
Zener diode voltage regulator

Guan X, Yu S, Wong H S. A SPICE compact model of metal oxide resistive switching memory with variations[J]. IEEE electron device letters, 2012.

Vourkas I, Sirakoulis G C. Memristor-Based Nanoelectronic Computing Circuits and Architectures[M]. Springer, 2015.
Memristor Models

Another (deeper) problem with $f_2$

TEAM/VTEAM, Yakopcic models

$$f_2 = \begin{cases} 
  k_{off} \cdot (\frac{v_{pn}}{v_{off}} - 1) \alpha_{off}, & \text{if } v_{pn} > v_{off} \\
  k_{on} \cdot (\frac{v_{pn}}{v_{on}} - 1) \alpha_{on}, & \text{if } v_{pn} < v_{on} \\
  0, & \text{otherwise}
\end{cases}$$

where

$$v^* = (1 - s) \cdot v_{off} + s \cdot v_{on}$$
Memristor Models

\[
\frac{d}{dt} s = f_2 (\text{vpn}, s)
\]

\[
ipn = f_1 (\text{vpn}, s)
\]

Available \( f_2 \):

1. linear ion drift
   \[
f_2 = \mu_v \cdot R_{on} \cdot f_1 (\text{vpn}, s)
   \]
2. nonlinear ion drift
   \[
f_2 = a \cdot \text{vpn}^m
   \]
3. Simmons tunnelling barrier
   \[
f_2 = \begin{cases} c_{off} \cdot \sinh \left( \frac{i}{i_{off}} \right) \cdot \exp \left( - \exp \left( \frac{\frac{s-a_{off}}{w_c} - \frac{1}{b}}{w_c} \right) \right), & \text{if } i \geq 0 \\ c_{on} \cdot \sinh \left( \frac{i}{i_{on}} \right) \cdot \exp \left( - \exp \left( \frac{i_{on} - s}{w_c} + \frac{1}{b} \right) - \frac{s}{w_c} \right), & \text{otherwise,}
   \end{cases}
   \]
4. TEAM model
5. Yakopcic model
6. Stanford/ASU
   \[
f_2 = -v_0 \cdot \exp \left( - \frac{E_a}{V_T} \right) \cdot \sinh \left( \frac{\text{vpn} \cdot \gamma \cdot a_0}{t_{ox} \cdot V_T} \right)
   \]

Available \( f_1 \):

1. \[
f_1 = (R_{on} \cdot s + R_{off} \cdot (1 - s))^{-1} \cdot \text{vpn}
   \]
2. \[
f_1 = \frac{1}{R_{on}} \cdot e^{-\lambda \cdot (1 - s)} \cdot \text{vpn}
   \]
3. \[
f_1 = s^n \cdot \beta \cdot \sinh (\alpha \cdot \text{vpn}) + \chi \cdot (\exp(\gamma \cdot) - 1)
   \]
4. \[
f_1 = \begin{cases} A_1 \cdot s \cdot \sinh (B \cdot \text{vpn}), & \text{if } \text{vpn} \geq 0 \\ A_2 \cdot s \cdot \sinh (B \cdot \text{vpn}), & \text{otherwise.}
   \end{cases}
   \]
5. \[
f_1 = I_0 \cdot e^{-\frac{\text{Gap}}{g_0}} \cdot \sinh \left( \frac{\text{vpn}}{V_0} \right)
   \]

- set up boundary
- fix \( f_2 \) flat regions
- smooth, safe funcs, scaling, etc.
Memristor Models

A collection of 30 models:
- all smooth, all well posed
- not just RRAM, but general memristive devices
- not just bipolar, but unipolar
- not just DC, AC, TRAN, but homotopy, PSS, ...

PSS using HB
Challenges in Memristor Modelling

- hysteresis
  - internal state variable

- model internal unks in Verilog-A
  - use potentials/flows

- upper/lower bounds of internal unks
  - filament length, tunneling tap size
  - clipping functions

- smoothness, continuity, finite precision issues, ...
  - use smooth functions, safe functions
  - GMIN
  - scaling of unks/eqns
  - SPICE-compatible limiting function (the only smooth one)