A 103 dB DR Fourth-Order Delta-Sigma Modulator for Sensor Applications

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Received: 31 August 2019; Accepted: 24 September 2019; Published: 26 September 2019

Abstract: This paper describes a fourth-order cascade-of-integrators with feedforward (CIFF) single-bit discrete-time (DT) switched-capacitor (SC) delta-sigma modulator (DSM) for high-resolution applications. This DSM is suitable for high-resolution applications at low frequency using a high-order modulator structure. The proposed operational transconductance amplifier (OTA), used a feedforward amplifier scheme that provided a high-power efficiency, a wider bandwidth, and a higher DC gain compared to recent designs. A chopper-stabilization technique was applied to the first integrator to remove the 1/f noise from the transistor, which is inversely proportional to the frequency. The designed DSM was implemented using 0.35 μm complementary metal oxide semiconductor (CMOS) technology. The oversampling ratio (OSR) was 128, and the sampling frequency was 128 kHz. At a 500 Hz bandwidth, the signal-to-noise ratio (SNR) was 100.3 dB, the signal-to-noise distortion ratio (SNDR) was 98.5 dB, and the dynamic range (DR) was 103 dB. The measured total power dissipation was 99 μW from a 3.3 V supply voltage.

Keywords: delta-sigma modulator; feedforward architecture; operational transconductance amplifier; biomedical sensor

1. Introduction

The biomedical market is expanding rapidly in response to the increasing interest in human healthcare. Wireless biomedical sensing systems require a low-power wireless transmitter and a high-resolution analog-to-digital converter (ADC) [1,2]. A delta-sigma modulator (DSM) architecture is more appropriate for biomedical sensing applications than many other ADCs because it can achieve a high resolution in low-frequency domains [1–3].

There are two types of DSMs that can be implemented: continuous-time (CT) and discrete-time (DT) structures. CT DSMs are highly sensitive to process variations because the CT DSM coefficients depend on the capacitors and resistors. Clock jitter and excess loop delay also degrade CT DSM performance [4]. DT DSMs are typically implemented as switched-capacitor circuits, which are not sensitive to process variations. The DT DSM is also more robust to clock jitter and excess loop delay problems.

Electromyograms, which record electrical activity in skeletal muscles, are widely used in medical research, rehabilitation medical science, and sports science because they can diagnose functional abnormalities in muscles. The bandwidth of a DSM is 500 Hz, which is appropriate for measuring electromyogram signals within a signal band of 500 Hz [5].

Figure 1 shows an example of an analog front end (AFE) for sensing biomedical signals [6]. Each channel has a set comprised of a preamplifier, a low-pass filter, and a sample and hold circuit. The multiplexer selects one of the channel outputs and transfers the channel output to the ADC. The electromyogram signal has a very small voltage amplitude ranging from approximately 0.1–5 mV [5]. Due to the small magnitude of the electromyogram signal, an amplifier must be used to amplify the
electromyogram signal so that the ADC can process it, as shown in Figure 1. Recording electromyogram data without saturation from large motion artifacts requires a wide dynamic range [7]. The designed DSM has a high resolution and a wide dynamic range (DR) at a low frequency due to oversampling and its noise-shaping characteristics compared to other ADCs. Using a high-resolution DSM can decrease an AFE’s power dissipation by removing the amplifier or reducing the power of the amplifier that amplifies the input signal.

This paper is organized as follows. Section 2 explains the circuit design and implementation of the fourth-order cascade-of-integrators with feedforward (CIFF) DSM. Section 3 presents the experimental results of the designed DSM chip. Section 4 concludes.

2. Circuit Design and Implementation

2.1. Fourth-Order CIFF DSM

Figure 2 illustrates the architecture of the fourth-order CIFF DSM. The fourth-order DSM is designed to achieve a high resolution. The DSM architecture types can be divided mainly into CIFF architecture and cascade-of-integrators with feedback (CIFB) architecture [8,9]. CIFF architecture was selected for the DSM in this paper. The main difference between CIFF architecture and CIFB architecture is that the former is transferred directly to the quantizer through the feedforward path of the input and output signals. The output voltage swing of each integrator is reduced through the feedforward path of the modulator. Therefore, the requirement for the voltage headroom and slew rate of the operational transconductance amplifier (OTA) is relaxed, which represents an advantage over the CIFB architecture in terms of power efficiency [8,9].

Internal feedback ($g_1$) was added between the third integrator and the fourth integrator in the loop filter. Internal feedback reduces noise power to improve the signal-to-noise ratio (SNR) because it creates a value of zero near the signal band in the noise transfer function (NTF) [9].
Table 1 summarizes the coefficients of the modulator in Figure 2. The coefficients were determined using MATLAB/Simulink modeling, and Cadence Spectre simulation was used for the circuit-level simulation. The NTF of Figure 2 was calculated as follows:

\[
\text{NTF} = \frac{(z - 1)^4}{(z^2 - 1.492z + 0.5646)(z^2 - 1.1702z + 0.787)}.
\] (1)

For stable operation, the NTF maximum gain over all the frequencies must be lower than 1.5. However, for moderate-order modulators (third-order or fourth-order), a slightly higher value may be tolerable, whereas the values for very high-order modulators are more conservative. In Equation (1), the NTF maximum gain is 1.5.

| Table 1. Coefficients of the modulator shown in Figure 2. |
|------------------------------------------------------------|
| **Input Coefficients** | **Feedforward Coefficients** | **Integrator Coefficients** |
| \(b_1 = 0.2\) | \(a_1 = 4\) | \(c_1 = 0.2\) |
| \(b_2 = 1\) | \(a_2 = 3\) | \(c_2 = 0.5\) |
| | | \(c_3 = 4/9\) |
| | | \(c_4 = 0.1\) |
| | | \(g_1 = 0.0003\) |

Figure 3 shows a schematic of the fourth-order CIFF DSM. The differential input signal is sampled by the sampling capacitors \(C_{S1}\) as shown in Figure 3. To prevent degradation due to thermal noise, the thermal noise level should be lower than the quantization noise level. Therefore, the thermal noise should be considered when calculating the sampling capacitor \(C_{S1}\) value of the first integrator [8]. The first-integrator sampling capacitor equation is as follows:

\[
C_{S1} = \frac{8 \times k \times T \times DR}{VDD^2 \times M},
\] (2)

where \(k\) is the Boltzmann constant, \(T\) is the absolute temperature, \(VDD\) is the supply voltage, and \(M\) is the oversampling ratio. In the present design, the oversampling ratio \(M\) was 128; the DR was set to 110 dB for a design margin. The required capacitance was calculated as 2.3 pF for the power supply \(VDD\) of 3.3 V. With the extra noise margin, the final sampling capacitance was 2.5 pF. The capacitor values used in the DSM are summarized in Table 2.

| Table 2. Capacitor values used in the DSM (units are in pF). |
|--------------------------------------------------------------|
| **Sampling Capacitor** | **Integrating Capacitor** | **Feedforward Capacitor** |
| \(C_{S1} = 2.5\) | \(C_{F1} = 12.5\) | \(C_{FF1} = 1\) |
| \(C_{S2} = 0.5\) | \(C_{F2} = 1\) | \(C_{FF2} = 0.4\) |
| \(C_{S3} = 0.8\) | \(C_{F3} = 1.8\) | \(C_{FF3} = 0.3\) |
| \(C_{S4} = 0.1\) | \(C_{F4} = 1\) | \(C_{FF4} = 0.15\) |
| \(C_{DAC} = 2\) | | \(C_{FF5} = 0.15\) |
Figure 3. A schematic of the fourth-order CIFF single-bit switched-capacitor DSM.
As shown in Figure 3, the low-frequency noise of the amplifier itself was removed by applying a chopper-stabilization technique between the input and output of the first integrator’s OTA. The chopper-stabilization technique prevents the performance degradation induced by the offset voltage and 1/f noise [12,13]. Because 1/f noise is more dominant than thermal noise at a low frequency, the removal of 1/f noise is essential to achieving a high resolution in low-frequency applications. A chopper-stabilization technique consists of switches that are connected to both the amplifier’s input path and output path in a cross shape [13]. These switches are synchronized to a chopping clock, and the positive and negative paths continuously switch to each other. The offset voltage and 1/f noise move to an out-of-band chopping frequency. The input signal is demodulated after modulation and is not affected by chopping. As a result, the offset and 1/f noise can be efficiently removed without altering the input signal [12]. The OTA input switches used an n-channel metal-oxide semiconductor (NMOS), and the OTA output switches used a transmission gate in which NMOS and a p-channel metal-oxide semiconductor (PMOS) transistors were connected in parallel to increase the voltage swing range [14]. The chopping frequency of the DSM in this paper was 8 kHz, which was 1/16 of the sampling frequency. The chopper frequency was generated by four d flip-flops.

Figure 4 shows the noise simulation of the first OTA in the log scale. The dotted line represents what occurred when the chopper-stabilization technique was not applied. The noise at 0.1 Hz was 2.85 mV/√Hz, and the noise at 100 Hz was 50 μV/√Hz. The solid line represents what occurred when the chopper-stabilization technique was applied. The noise at 0.1 Hz was 0.49 mV/√Hz, and the noise at 100 Hz was 58 μV/√Hz. The noise reduction was confirmed for the frequency range below 100 Hz.

![Figure 4. Noise simulation results of the first operational transconductance amplifier (OTA).](image)

As will be demonstrated in the experimental results, the noise power decreased at a low frequency when the chopper-stabilization technique was applied.
2.2. Proposed Feedforward OTA and Common-Mode Feedback (CMFB) Circuit

The OTA is the most critical block in the DSM. In particular, the OTA in the first integrator has the most important effect on the modulator’s performance [15,16]. Therefore, an OTA structure that has a strong performance and high-power efficiency is necessary when designing a DSM. The feedforward OTA [15] was designed by trying to achieve a high-power efficiency via broadening the bandwidth through the feedforward path. In this study, a new feedforward OTA was proposed to further enhance performance of the DSM.

Figure 5 shows a schematic of the proposed OTA, which was applied to the first integrator. A transconductance enhancement scheme was used for the amplifier of the main path (−gm1, −gm2) [16]. A large gain with an increased output impedance was obtained through the use of a cascode structure in the output stage of the proposed OTA. The headroom limit of the cascode output was not a problem in this DSM because a CIFF structure was used. The feedforward path was implemented via a gmf block, as shown in Figure 5. By creating a value of zero inside the unity-gain bandwidth (UGBW) through control of the M11 current, the UGBW was efficiently broadened with only a slight increase in power consumption. The proposed OTA has an 84.8 dB DC gain and a 19 MHz bandwidth at a total power consumption of only 47.5 µW, with 8 µW of the power consumed by the gmf block.

For a better conceptual understanding of the proposed OTA, Figure 6a shows the topology of the feedforward OTA. In Figure 5, −gm1, −gm2, and gmf in the boxes with the dotted line correspond to −gm1, −gm2, and gmf in Figure 6a, respectively. RO1 and RO2 are the output impedance of the −gm1 and −gm2 blocks, respectively. Cp is a parasitic capacitor, and CL is the load capacitor (including both the parasitic capacitance and the sampling capacitance of the next integrator). Figure 6b shows the AC simulation results of the circuit in Figure 5. Both the parasitic and load capacitors were included in the AC simulation. Cases both with and without the feedforward scheme were simulated for comparison. As shown in Figure 6b, the UGBW of the proposed OTA was higher (19 MHz) than the UGBW of the conventional OTA (8 MHz). As discussed above, the extra power needed for this additional amplification was only 8 µW, whereas the bandwidth increased by more than a factor of two.

Figure 7 shows a schematic of the switched-capacitor common-mode feedback (CMFB) circuit [17]. The same switched-capacitor CMFB circuit was used for all the OTAs. The switched-capacitor CMFB circuit had the advantages of low power consumption and fast linear operation. The operation was as follows. During the integration phase (Φ2), capacitance C1 was charged to the desired common-mode levels, which were half of the supply voltage and a bias voltage of the M15 and M16 transistor, respectively. The charge on C2 was refreshed during the sampling phase (Φ1) by connecting the C1 and
C2 capacitors together between the outputs of the OTA and the gate of transistor M15 and M16. If the common-mode level was too high, the gate voltage of transistors M15 and M16 also increased, reducing the common-mode level of the outputs. The S1 switches used the transmission gate to increase the voltage swing range.

![Diagram of OTA topology](image)

**Figure 6.** Proposed OTA topology. (a) Block diagram; (b) comparison of bode plots.

![Diagram of switched-capacitor CMFB circuit](image)

**Figure 7.** A schematic of the switched-capacitor common-mode feedback (CMFB) circuit.

The simulation results of the first-integrator’s OTA and other OTAs are summarized in Table 3. Other OTAs were designed as folded-cascode amplifiers with a basic structure [18]. The effective load capacitance was calculated, including the effect of the parasitic components [19].

| Parameter                      | First-Integrator’s OTA | Other OTAs |
|--------------------------------|------------------------|------------|
| Supply voltage (V)             | 3.3                    | 3.3        |
| Power consumption (µW)         | 14.4                   | 5          |
| DC gain (dB)                   | 83                     | 74         |
| Phase margin (degree)          | 62                     | 89         |
| Load capacitor (pF)            | 2.2                    | 0.9        |
| UGBW (MHz)                     | 18                     | 2.6        |

### 2.3. Single-Bit Quantizer

The single-bit quantizer consisted of a comparator and a set/reset (SR) latch, as shown in Figure 8. The quantizer input INP and INN were connected to the output of the adder circuit. The left part was the comparator, and the right part was the SR latch. In the single-bit DSM, the comparator did not have a significant effect on performance; therefore, a simple comparator with low power consumption was used [18]. When \( \Phi_{1d} \) was low, the inputs of the not-AND (NAND) SR latch were high, and the comparator output did not change. When \( \Phi_{1d} \) was high, the gate voltage difference between M1 and M2 produced either a high or low comparator output through a positive feedback loop.
2.4. Clock Generator

A schematic of the clock generator is shown in Figure 9. It generated $\Phi_1$, $\Phi_{1d}$, $\Phi_2$, and $\Phi_{2d}$ clock signals. In this circuit, the delay and non-overlap times could be adjusted via the inverters marked with asterisks. The clock was applied using an external function generator. Non-overlap was required to prevent the $\Phi_1$ and $\Phi_2$ switches from turning on at the same time. Delayed clocks ($\Phi_{1d}$ and $\Phi_{2d}$) were generated to reduce the linearity problem caused by charge injection. As shown in Figure 9, this delay occurred only at the falling edges of the clock phases. In order to efficiently use the short clock period, the falling clock edges were delayed, and the rising clock edges were synchronized.

![Figure 9. A schematic of the clock generator.](image-url)
3. Experimental Results

The fourth-order CIFF single-bit DT switched-capacitor DSM was designed and fabricated using a single-poly, four-metal, 0.35 μm standard complementary metal oxide semiconductor (CMOS) process. Figure 10 shows a microphotograph of the DSM chip for the biomedical application. The size of the chip was 0.27 mm². In order to improve the performance of the modulator, the layout was considered as follows:

- The analog, digital, and mixed-signal parts were separated from each other to reduce attenuation caused by noise interference. Guard rings were also used for each part.
- Separate power supplies were used for the analog, digital, and mixed-signal parts, each with their bonding pad and chip package pin for the analog, digital, and mixed signal parts as well as the guard rings [19]. Separate power supplies were used for the analog, digital, and mixed-signal parts of the test board.
- The layout used a differential technique to reduce common mode interference [19]. The differential input transistors of the OTA were applied using the common centroid layout technique in order to improve matching performance.

![Figure 10. Chip microphotograph.](image)

Figure 11 shows the test bench of the DSM chip. A signal generator, a function generator, a power supply, a logic analyzer, and a PC were used for the measurements. Fully differential input sinusoidal waves (up to 200 kHz) were generated with a signal generator (Audio Precision SYS-2712, Test Equipment Solutions Ltd, Aldermaston, UK). The clock signal was generated with a function generator (Agilent 33250A, Keysight, Santa Rosa, CA, USA). The generated clock frequency was 128 kHz. The digital output was stored in the memory of the logic analyzer (Agilent 16801A, Keysight, Santa Rosa, CA, USA) and then transferred to a PC for processing in MATLAB.

Figure 12 shows the measured output spectrum of the chip. The two waveforms were compared to show the performance improvement from the chopper stabilization. The dotted line occurred when the chopper-stabilization technique was not applied, and the solid line occurred when the chopper-stabilization technique was applied. As the results show, when the chopper-stabilization technique was applied, the noise floor was lowered below about 100 Hz. By applying the chopper-stabilization technique, the SNR and SNDR were improved by approximately 6 dB. The number of samples was 131,072, and the frequency of the input signal was 108.4 Hz.
The peak SNR was 100.3 dB, the peak SNDR was 98.5 dB, and the DR was 103 dB. The peak SNDR was achieved at $-5.6$ decibels relative to full scale (dBFS) of the sinusoidal input. Table 4 summarizes the measured performance of the DSM. The performance for the 700 Hz bandwidth was also measured, demonstrating the good noise-shaping characteristics of the designed DSM.
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Figure 13 shows a graph that compares the SNR and signal-to-noise distortion ratio (SNDR) according to the input amplitude. The full-scale range, which is marked as 0 dB in Figure 13, was the supply voltage level in the measurement. The peak SNR was 100.3 dB, the peak SNDR was 98.5 dB, and the DR was 103 dB. The peak SNDR was achieved at $-5.6$ decibels relative to full scale (dBFS) of the sinusoidal input. Table 4 summarizes the measured performance of the DSM. The performance for the 700 Hz bandwidth was also measured, demonstrating the good noise-shaping characteristics of the designed DSM.

Table 4. Performance summary.

| Parameter               | Value |
|-------------------------|-------|
| Supply voltage (V)      | 3.3   |
| Signal bandwidth (Hz)   | 500   |
| Sampling frequency (kHz)| 128   |
| Power consumption ($\mu$W) | 14.4 |
| Peak SNR (dB)           | 100.3 |
| Peak SNDR (dB)          | 98.5  |
| Dynamic range (dB)      | 103   |

Figure 14 contains the details of the chip’s power consumption. The majority of the power consumption was from the OTAs. Further, the OTA in the first integrator was the most critical to the chip’s performance, as it consumed the highest portion of the total power.

Table 5 compares the performance of the designed DSM with that of other DSMs with similar bandwidths. A general figure-of-merit (FOM) formula is used for the comparison [19]:

$$FOM = \frac{P}{2.BW} \times 2 \times BW.$$ (3)

In the FOM formula, BW and P refer to the signal bandwidth and power consumption, respectively. As shown in Table 5, the designed DSM demonstrated good performance compared to the other DSMs in low-frequency applications.

Figure 14. Power breakdown.
Table 5 compares the performance of the designed DSM with that of other DSMs with similar bandwidths. A general figure-of-merit (FOM) formula is used for the comparison [19]:

$$FOM = \frac{P}{2^{\frac{SNDR - 1.76}{6.02} \times 2 \times BW}}.$$  \hspace{1cm} (3)

In the FOM formula, BW and P refer to the signal bandwidth and power consumption, respectively. As shown in Table 5, the designed DSM demonstrated good performance compared to the other DSMs in low-frequency applications.

| Paper | This Work | Reference [20] | Reference [21] | Reference [22] |
|-------|-----------|----------------|----------------|----------------|
| Type | 1 bit DT | 1 bit DT | 1 bit DT | 1 bit DT |
| Bandwidth (Hz) | 500 | 128 | 2000 | 2000 | 25,000 |
| Sampling frequency (kHz) | 128 | 2000 | 10,000 | 20,480 |
| Peak SNDR (dB) | 98.5 | 98 | 100.2 | 46.3 | 60.8 |
| DR (dB) | 100.3 | 107.6 | 56 | 70.1 |
| VDD (V) | 3.3 | 3.3 | 1.8 | 5 |
| Power consumption (µW) | 99 | 3200 | 684 | 43.4 |
| Process (µm) | 0.35 | 0.35 | 0.18 | 0.5 |
| FOM (pJ/step) | 1.44 | 1.08 | 9.5 | 13.2 | 1.21 |

4. Conclusions

This study presented a fourth-order CIFF single-bit DT switched-capacitor (SC) DSM for electromyogram signal sensing. The first integrator was the most important block; it also had the greatest power consumption. For this reason, this study improved the performance of the first integrator by using the new proposed feedforward OTA. Both the SNR and SNDR were improved by removing the 1/f noise, which becomes problematic when designing low-frequency circuits, by applying the chopper-stabilization technique to the first integrator. The DSM was designed using a 0.35 µm CMOS process with a 100.3 dB SNDR and 103 dB DR in a 500 Hz bandwidth. The total power dissipation was 99 µW from a 3.3 V supply voltage.

Author Contributions: Conceptualization, J.L., S.S. and J.R.; methodology, J.L. and S.S.; data curation, J.L., S.S.; writing—original draft preparation, J.L.; supervision, J.R.

Funding: This research received no external funding.

Acknowledgments: This research was supported by the MOTIE (Ministry of Trade, Industry and Energy; project number 10080488) and the KSRC (Korea Semiconductor Research Consortium) support program for the development of future semiconductor devices. This research was also supported by the MSIT (Ministry of Science and ICT), Korea, under the ITRC (Information Technology Research Center) support program (IITP-2019-2018-0-01421) supervised by the IITP (Institute for Information and Communications Technology Promotion). This work was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (No. 2019R1A2C2085189).

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

- ADC: analog-to-digital converter
- DSM: delta-sigma modulator
- CT: continuous-time
- DT: discrete-time
- AFE: analog front-end
- DR: dynamic range
- CIFF: cascade-of-integrators with feedforward
- CFIB: cascade-of-integrators with feedback
OTA operational transconductance amplifier
SNR signal-to-noise ratio
NTF noise transfer function
NMOS n-channel metal-oxide semiconductor
PMOS p-channel metal-oxide semiconductor
SNDR signal-to-noise and distortion ratio
UGBW unity-gain bandwidth
CMFB common-mode feedback
CMOS complementary metal oxide semiconductor
SR Set/Reset
NAND Not-AND
dBFS decibels relative to Full Scale

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