Logics execution in a multi-layers memristor array

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Abstract. Memristor stateful logic based on a two-dimensional (2D) memristor crossbar array (MCBA) has been proved to be an effective approach to break the von Neumann bottleneck. But the three-dimensional (3D) array which has an inherent high storage density is less investigated in logic computation field. In this work, we implemented the whole linearly separable binary Boolean logic functions completely by using the stateful logic circuits configured in a multi-layer memristor crossbar array. This circuit primitive can execute multi-gates parallelly inside layer or the interlayer of 3D MCBA. This work provided a significant reference for the achievement of real processing in memory (PiM) in a high-density array.

Keywords: memristor, logic design, crossbar, three-dimension.

1. Introduction

In recent years, the memristor, a nonvolatile two-terminal device, has aroused renewed interest which is regarded as the potential device to achieve real “processing in memory” (PiM). The resistant state can be switched by the voltage applying across it [1], [2]. Fig. 1(a) shows the typical structure of bipolar memristor (based on the interlayer materials of HfOx and Al₂O₃) [3] and its typical I-V behavior. A forward voltage from the top electrode (TE) to the bottom electrode (BE) can switch the memristors from the high resistance state (HRS) to the low resistance state (LRS), when the amplitude higher than \(V_{set}\) (the so-called SET voltage). Inversely, the device is switched from LRS to HRS once the applying opposite voltage is smaller than \(V_{reset}\) (the so-called RESET voltage). Two stable resistance states can be used to represent logical 0 and 1 respectively, which makes the memristor be potential as a physical nonvolatile memory [4]. Besides, another important parameter to describe the character of memristors is the memory window that defied as the ratio of high resistance and low resistance. The normal memory window regularly is more than 10 times[5].

Thanks to its simple device structure, the memristor can be easy to integrate as a crossbar array structure. Connecting the same electrodes of memristors, a two-dimensional (2D) memristor crossbar...
array (MCBA) is created. A three-dimensional (3D) crossbar is fabricated by folding (Fig. 1(b)) the 2D array to improve the storage density greatly. Furthermore, the 3D structure can relieve the interconnect resistance and the interconnects delay which are serious problems in 2D structure [4].

Figure 1. (a) The simplified structure of HfO$_x$ – Al$_2$O$_3$ based memristor and its I-V character. (b) The structure of folded 3D MCBA. (c) The front view and (d) top view and (e) left view of 3D MCBA. To guarantee the memristors participating the calculation connect to the CL, the memristors of gate1 and gate2 (circled by the blue dash lines) have to been located in the single layer while the memristors of gate5 (circled by the orange dashed lines) can be scattered in the adjacent layers. The gate1 and gate2 can be executed parallelly with the appreciate voltage applied to $V_{in1}$, $V_{in2}$, $V_{out}$, and $V_s$. (f) The concluded connection relationship of memristor in 3D folded MCBA. The memristors connect to the CL through BE or TE, respectively, demonstrated by the upper and lower schematics.

Based on Kirchhoff’s law, Ohm’s law, and the memristor switching character, the memristor stateful logic, as a memristor-based Boolean logic, can be executed in a memristor crossbar array by changing the voltages across memristors [6]. This way, the storage and calculation of information are both completed in the same memristor cell, and the PiM is realized. In the last decade, there are many memristor stateful logic systems are proposed [3], [6]–[12]. Reference [6] firstly, reported the material implication (IMP) logic utilizing the resistant switching character while changing the input memristors state which coursed the input losing problem. A neural network-based method to realize the whole 14 lineal separable Boolean logics in one step is advised in [12]. But these investigations are based 2D memristor crossbar array that cannot be configured in the 3D array without considering the actual location relationships of memristors for 3D MCBA. Reference [9] shown the IMP and AND realization. But this primitive also aroused the input losing problem.

In this scenario, a method is presented to achieve 14 out of 16 binary Boolean logics with just one calculation pulse in a 3D MCBA. The relationship of memristor character and peripheral circuit is revealed to guiding the selection of circuit parameters according to the real devices. Besides, the papalism between multi-gates is achieved inter the layer and inside the adjacent layers. These stateful logic primitives in a three-dimensional crossbar improved the space utilization rate and exploited the inside and interlayer parallelism of calculation without the input losing problem, enabling the real PiM within the high-density memristor crossbar array.
2. The primitive circuit configuration in a 3D crossbar array

A folded three-dimensional memristor crossbar with three rows and three columns and three layers is shown in Fig.1(b). 27 memristors are located in the cross points which are fabricated by 6 word lines (WL) and 6 bit lines (BL). A grounded consistent resistor with the conductance \( G_S \) is connected to the tail of WL or BL to adjust the potential. The devices participating in the calculation should connect to a common line (CL) to transmit the information that they stand for as presented in Fig. 1(c) and (e). The relationship of locations is concluded in Fig. 1(f). The logic inputs are stored in memristor pair (IN1, IN2) or (IN3, IN4) which are connected to the CL through BE or TE, respectively. Similarly, the logic output can be presented by the final state of OUT1 or OUT2. In this work, we take (IN1, IN2, OUT1) combination as a sample to present our work. As symmetry, the voltages applied are the opposite number when the memristors connect to CL through TE. Before the logic execution, memristors IN1 and IN2 are initialized as the logic inputs while OUT1 is initialized HRS (logical “0”).

In Fig. 1(f) (top), the potential of common line CL is presented as Eq. 1

\[
V_{CL} = \frac{\sum_i V_i G_i}{\sum_i G_i}.
\]  

Figure 2. The lineal programming models of six basic logics. (a)-(f) The schematic of the linear programming models. (g) The parameter of the linear programming models.

\[
F_{OUT1} = \sum_i (V_{OUT1} - V_i - V_{set}) G_i \quad (\omega_i = V_{OUT1} - V_i - V_{set})
\]

is the equivalent current sign to control the state of output memristor changed or not. The output memristor will be set to LRS if
$F_{\text{OUT}} > 0$ or else, kept at HRS. Similarly, the equivalent currents $F_{\text{IN1}}$ and $F_{\text{IN2}}$ following the format of Eq. 3 and Eq. 4 are the signs to control the maintenance of input memristors states,

$$F_{\text{IN1}} = \sum_i (|V_{\text{IN1}} - V_i| - V_{\text{min}}) G_i . 
(3)$$

$$F_{\text{IN2}} = \sum_i (|V_{\text{IN2}} - V_i| - V_{\text{min}}) G_i . 
(4)$$

Here, $V_{\text{min}}$ is the minimum of SET voltage and the absolute value of RESET voltage, e.g., $V_{\text{min}} = \min\{|V_{\text{set}}|, |V_{\text{reset}}|\}$. The absolute value acts as the synthetical factor regardless of the locations of input memristors. Changing the weight of the conductivities of devices by adjusting the voltages applied, all of the linear separable logic functions can be implemented in one pulse [12].

3. Design of stateful logic

The binary Boolean logic can be regarded as the linear programming problem [12]. Fig. 2(a)-(f) illustrate the linear programming models of six basic linear separable logics. The X-axis and Y-axis present the value of logic inputs $A$ and $B$, respectively. The plane represents logic output, namely $C'$, and is divided into two parts according to the output value. The blank circles are interspersed among the region presenting logic 0 while the filled ones are among the logical 1 region. The separator between the logical 0 region and logical 1 region follows the pattern shown as Eq. 5:

$$l : A + mB - n = 0 . 
(5)$$

As logical 1 and 0 can be presented by LRS and HRS, respectively, the logical value can be expressed by the conductance. That is to say, the separator is equal to

$$l : G_A + mG_B - nG_{\text{LRS}} = 0 
(6)$$

where $G_{\text{LRS}}$ is the conductance of memistor in LRS. To guarantee the switching margin to be the largest, the values of $m$ and $n$ are summarized in Fig. 2(g)[12]. Besides, the region representing logical 1 for the specific logic is expressed by the relationship between $l$ and 0.

By comparing the expression of logical 1 region in Fig. 2(g) with the condition $F_{\text{OUT}} > 0$, the relationship of peripheral circuit parameters guaranteeing the output switched is obtained. With $g_{\text{SL}} = \frac{G_S}{G_{\text{LRS}}}$ and $g_{\text{HL}} = \frac{G_{\text{HRS}}}{G_{\text{LRS}}}$ describing the offset of $G_S$ and $G_{\text{HRS}}$ compared to $G_{\text{LRS}}$, the relationship of peripheral circuit parameters is demonstrated by equations (7)-(9).

$$V_{\text{S}} = 0 . 
(7)$$

$$V_{\text{B}} = \frac{g_{\text{SL}}}{g_{\text{SL}} + n} V_{\text{A}} + \frac{g_{\text{HL}} (1 - m)}{g_{\text{SL}} + n} V_{\text{set}} . 
(8)$$

$$V_{\text{C}} = \frac{n}{g_{\text{SL}} + n} V_{\text{A}} + \frac{g_{\text{SL}} + n + g_{\text{HL}}}{g_{\text{SL}} + n} V_{\text{set}} . 
(9)$$
The voltage pair \( (V_A, V_B) \) is applied to the input memristors according to the logic inputs. And \( (V_C, V_S) \) are assigned to the output memristor and resistor, respectively.

Given that the output has been switched alright, the voltage range is limited by the condition that \( F_{IN1} < 0 \) and \( F_{IN2} < 0 \) to maintain the state of input memristors. The relationship of peripheral circuit parameters for IMP logic is demonstrated in Table 1. Here, the normalized coefficient \( V_{sat}/V_{min} \) and \( g_{HL} \) are the arguments to demonstrate the influence of threshold voltage and memory window on the peripheral circuit for Boolean logics, respectively. To ensure reliability, \( g_{HL} \) is defined as the reciprocal of the minimum memory window of all the memristors. Generally speaking, \( g_{HL} \) is less than 0.1 [5].

### Table 1. The relationship of IMP between peripheral circuit and the memristors character.

| RELATIONSHIP OF PERIPHERAL CIRCUIT | VOLTAGE RANGE |
|------------------------------------|---------------|
| \( V_A = 0 \)                      | \( V_{sat}/V_{min} = \frac{2g_{HL} + 1}{2g_{HL}^2 + 3g_{HL} + 4g_{HL}^2} \left\{ \frac{1}{2g_{HL} + 1} V_{sat} + 2g_{HL} + 1 V_{sat} \right\} \) |
| \( V_B = \frac{2g_{HL} - 1}{2g_{HL} + 1} V_A + \frac{4g_{HL}}{2g_{HL} + 1} V_{sat} \) | \( \max \left\{ \frac{2g_{HL} + 1}{2g_{HL}^2 + 3g_{HL} + 4g_{HL}^2} \left\{ \frac{1}{2g_{HL} + 1} V_{sat} + 2g_{HL} + 1 V_{sat} \right\}, \frac{2g_{HL} + 1}{2g_{HL}^2 + 5g_{HL}} \left\{ \frac{1}{2g_{HL} + 1} V_{sat} + 2g_{HL} + 1 V_{sat} \right\} \right\} \) |
| \( V_C = \frac{1}{2g_{HL} + 1} V_A + \frac{2g_{HL} + 1}{2g_{HL} + 1} V_{sat} \) | \( \min \left\{ \frac{2g_{HL} + 1}{2g_{HL}^2 + 3g_{HL} + 4g_{HL}^2} \left\{ \frac{1}{2g_{HL} + 1} V_{sat} + 2g_{HL} + 1 V_{sat} \right\}, \frac{2g_{HL} + 1}{2g_{HL}^2 + 5g_{HL}} \left\{ \frac{1}{2g_{HL} + 1} V_{sat} + 2g_{HL} + 1 V_{sat} \right\} \right\} \) |

14 out of 16 lineal sparable binary Boolean logics can be achieved in one execution pulse while the non-linear sparable logics, XOR and XNOR, need two sequential steps. The XOR logic is synthesized by cascading NIMP and CNIMP, while XNOR logic is composed of AND and NOR.

![Figure 3](image-url)

**Figure 3.** The relationship between peripheral circuit parameters and the threshold voltage on the condition of memory window is 100, 40, and 10, respectively. (a)-(c) The valid range of \( G_{LS}/G_{RS} \) effected by the memristors character. (d)-(f) Given that \( G_{LS}/G_{RS} = 2 \), the valid range of \( V_A \).
In [13], the authors reported the principle of parallel operation for logic execution in a 2D memristor crossbar. In a 3D structure, parallelism can be not only executed within the same layer but also in the adjacent layers. In Fig. 1(c), the input-output of gate1 and gate2 are stored in the memristor set \((G_{11}^{in}, G_{12}^{in}, G_{1out})\) and \((G_{21}^{in}, G_{22}^{in}, G_{2out})\), respectively. As all of the memristors connect to the CL through BE, gate1 and gate2 which are located in the adjacent layers can execute parallelly with the voltage set \((V_{in1}, V_{in2}, V_{out}, V_S)\) applied. On the other hand, Fig. 1(d) demonstrated the parallelism inside the same layer. With the voltage set \((V_{in1}, V_{in2}, V_{out}, V_S)\) applied, gate3 and gate4 can be executed parallelly. The parallelism in the adjacent layers further improved the space utilization rate.

4. Result and discussion

The valid range of constant resistor \(G_S\) is illustrated by the regions circled by the specific lines for different logics in Fig. 3(a)-(c). And the valid \(V_A\) ranges are presented in Fig. 3(d)-(f). Despite the \(\frac{G_S}{G_{LRS}}\) becomes more cramped with the enlargement of \(\frac{V_{set}}{V_{min}}\), the trend of the relationship between \(V_A\) range and \(\frac{V_{set}}{V_{min}}\) is approximate for an arbitrary value of \(\frac{G_S}{G_{LRS}}\). Without loss of generality, the discussion for \(V_A\) is based on the condition that \(\frac{G_S}{G_{LRS}}\) is set as 2.

As every picture in Fig. 3 reveals, with the voltage ratio \(\frac{V_{set}}{V_{min}}\) increased, the limit of \(G_S\) and \(V_A\) becomes more stringent. This is because that as the voltage ratio increases, the margin which guaranteed output memristor switched and input memristor retention decreases. Another truth can be made out that with the increment of conductance ratio \(\frac{G_{HRS}}{G_{LRS}}\), that is, decreased memory window, the limit of \(G_S\) and \(V_A\) become more permissive. That is because the input memristors with high resistance are more likely to be changed. Therefore, the smaller window slows this changing process and benefits the state's keeping. However, the small window will introduce difficulties to distinguish of resistance state and affect the reading out of information.

5. Summary

In conclusion, the stateful logic based on the three-dimensional memristor crossbar array is the potential approach for high-density processing in memory. In this work, we reported a general method for logic execution in a 3D memristor array that can achieve the logic either in the inside layer or interlayer of the 3D structure. This work is appreciated for the general memristor systems and offers the reference for the real logic in memory for the 3D MCBA.

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