OpenSEA:
Semi-Formal Methods for Soft Error Analysis

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Abstract—Alpha-particles and cosmic rays cause bit flips in chips. Protection circuits ease the problem, but cost chip area and power, and so designers try hard to optimize them. This leads to bugs: an undetected fault can bring miscalculations, the checker that alarms about harmless faults incurs performance penalty. Such bugs are hard to find: circuit simulation with tests is inefficient since it enumerates the huge fault time-location space, and formal methods do not scale since they explore the whole inputs. In this paper, we use formal methods on designer’s input tests, while keeping time-location open. This idea is at the core of the tool OpenSEA. OpenSEA can (i) find latches vulnerable to and protected against faults, (ii) find tests that exhibit checker false alarms, (iii) use fixed and open inputs, and (iv) use environment assumptions. Evaluation on a number of industrial designs shows that OpenSEA produces valuable results.

I. INTRODUCTION

In 1965 Moore’s law was born [1]: chips density doubles every few years. Aside from good things like improving performance, increasing chips density also increases sensitivity to cosmic radiation and alpha-particles [2]–[4]. These external influences can cause bit flips — the sudden change of internal memory values — that can lead to hardware misbehaviours [5]. Such errors are called soft errors, because the hardware is not harmed permanently.

There are ways to protect the circuit against soft errors [6]–[9]. Triple modular redundancy copies the circuit three times, computes three results in parallel, and chooses the result by majority vote, thus overcoming soft errors. Error correcting codes (ECCs) introduce spare bits that are used to restore the original values after the bit flip happens [10]. Parity computations [11] can detect bit flips.

But such protection methods are too expensive, since often circuits are intrinsically protected [12], for example, when the computation will not be used (think of branch predictions in processors). Thus, designers carefully optimize the protection logic to save area and power, which is difficult and error-prone.

We present tool OpenSEA to help the designer to verify and optimize the protection circuit. We assume that the protection circuit has a special output “alarm” (risen when a fault is detected), and consider only single fault scenarios [13].

OpenSEA provides three kinds of algorithms. First, it searches for vulnerable latches. Roughly, a latch is vulnerable if the fault in it can escape to the user without being alarmed. Second, OpenSEA searches for protected latches. Roughly, a latch is protected if the fault in it is always alarmed or recovered from before propagating to the user. Third, OpenSEA searches for spurious alarms. Roughly, an alarm is raised spuriously when the fault is always recovered from without being noticed. Spurious alarms hurts performance.

The idea behind the algorithms is to compare a fault-free circuit with a modified circuit where we model a fault, see Fig. 1. For example, if run a given test case on two circuits, inserting a fault into the second circuit, and check if the outputs can diverge without the alarm, then we get, roughly, the simulation based algorithm. Such two-circuits-comparison check can be offloaded to a SAT solver. Then, we can keep the fault location and time “symbolic” (“free”), thus asking a SAT solver if there is a fault latch and time that can escape without raising the alarm. Such approach is not new and was explored in [14]–[16], but to our knowledge no tools are available. Also, we allow the designer to use fixed tests, partially fixed tests (with some inputs left open), or completely open tests. Thus, our algorithm ranges from model checking to simulation. We call such approach semi-formal.

We evaluated OpenSEA on made-up examples, and started evaluation on industrial designs.

The source code and benchmark results are available at https://extgit.iai.tugraz.at/scos/soft-error-analysis/.

II. PRELIMINARIES

A. Faults, Vulnerable and Protected Latches, Alarm

A (transient) fault is a nondeterministic change of the latch value for one time step. We assume there can be at most one transient fault in a circuit during the execution. We do not consider other types of faults (stuck-at-zero, byzantine, etc.).

We assume a circuit has a special output alarm: alarm = true means a fault has been detected, and a higher-level service handles it (e.g., it restarts the computation).

Consider an execution where a fault happens in latch x at moment t. The fault escapes if outputs diverge at some moment t’ and the alarm is not raised before or at t’. The fault is alarmed if alarm is risen in the fault moment or later. Note that a fault can escape and yet be alarmed (too late).

A latch is vulnerable if there is an execution with an escaping fault in the latch. Otherwise, the latch is protected. I.e., a latch is protected if on all executions, a fault in the latch is either always detected before or at the moment when the outputs diverge, or the outputs never diverge.

Consider an execution with a fault at moment t in latch x. An alarm is spurious at moment ≥ t if the circuit states converge on all evolutions of that execution from t.
A. Searching for Vulnerable Latches and Spurious Alarms

OpenSEA supports several variations of the algorithms:

- Input test case is a file that contains input vectors. An input test case is a list of input vectors.
- Optionally, you can provide the environment assumptions circuit, which is a file that contains input vectors.
- You can annotate the test inputs. Lines 8–13 are specific to vulnerable latches (we later change them for spurious alarms): we encode that the outputs differ while the alarm is low, and use a SAT solver to incrementally find all vulnerable latches (Lines 10–13). SAT($F\land A$) denotes a SAT call: it returns 0 if the formula is unsatisfiable, otherwise it returns a satisfying assignment for variables $\overline{f}$ and $\overline{c}$. On algorithm termination, vulnerable contains vulnerable latches.

**Algorithm 1** Searching for vulnerable latches

1: procedure FINDVULNERABLE(test case $(\bar{I}_1, ..., \bar{I}_m)$)
2: vulnerable := \{
3: set $\bar{x}_1$ and $\bar{x}_1$ to $(0, ..., 0)$
4: $F := (\sum_{i\in[n]} c_i) = 1$
5: for $s = 1$ to $m$ do
6: $F \land= \bigwedge_{j<s}(f_s \rightarrow \neg f_j)$
7: $F \land= T(\bar{x}_1, \bar{i}, \bar{s}, a, \bar{x}') \land \neg a \land
\neg T'(\bar{x}_1, \bar{i}, f_s, \bar{c}, \bar{s}', a_s, \bar{x}_{s+1})$
8: $F \land= \neg a_s$
9: $A := (\sigma_s \neq \sigma_s')$
10: while $(\bar{f}, \bar{c}) := SAT(F \land A)$ do
11: vulnerable.add with $\bar{c}[i] = 1$ \text{ or } $i$ is unique
12: $F \land= \neg c_i$
13: end while
14: end for
15: end procedure

To search for spurious alarms, OpenSEA uses the modified Algorithm 1 where lines 8–13 are replaced by:

$$F \land= (\sigma_s = \sigma_s') \land \neg a_j \land A := (\bar{x}_{s+1} = \bar{x}_{s+1}) \land \bigvee_{j<s} a_j \land \text{outputs are equal} \land \text{states converge, but alarm is raised}$$

while $(\bar{f}, \bar{c}) := SAT(F \land A)$ do

spurious.add with $\bar{c}[i] = 1$ \text{ or } $i$ is unique

end while

On termination, the variable spurious contains the latches whose faults can lead to spurious alarms (initially empty).

1) Implementation: We implemented these algorithms in OpenSEA. The relevant to these checks tool’s arguments are:

- Circuit is in the AIGER format [17]. Optionally, you can provide the environment assumptions circuit, which purpose is to filter out traces not interesting for testing.
- Input test case is a file that contains input vectors. An inputs value can be left open by writing "?".
- OpenSEA supports several variations of the algorithms:
  - stla: fault time and location are symbolic (Alg. 1).
  - stfa: only fault time is symbolic while latches are enumerated in the for-loop.
  - sim (vulnerability only): enumeration of fault time and location, and of symbolic inputs.
  - bdd (vulnerability only): Algorithm 1 using BDDs.
- OpenSEA outputs: vulnerable latches (or latches causing spurious alarms) and the witnessing traces.

B. Transition Relations

**Notation.** We assume the reader is familiar with the notions of literal, clause, cube, CNF, DNF, sequential circuit. Tuples of Boolean variables are usually overlined, e.g., $\bar{x} = (x_1, ..., x_n)$, while tuples of their values are also bolded, e.g., $\bar{x} = (1, 0, ..., 1)$. We assume $\bigwedge_i(...) \text{ is true when } j < i$.

Consider Fig. 1: the top boxed area “Circuit” represents the circuit under test: it is divided into latches (the rectangle) and the combinational part (the cloud), it has inputs, outputs “Output 1”, and the special output “Alarm 1”.

A circuit can be represented as a Boolean formula $T(\bar{x}, \bar{i}, \bar{s}, a, \bar{x}')$ over variables $\bar{x}, \bar{i}, \bar{s}, a, \bar{x}'$, called transition relation. Given values $\bar{x}, \bar{x}', \bar{i}, \bar{s}, a$, $T(\bar{x}, \bar{i}, \bar{s}, a, \bar{x}')$ is true if the circuit, starting with latch values $\bar{x}$ and reading inputs $\bar{i}$, outputs $\bar{s}$, alarms $a$, and updates latch values to $\bar{x}'$. Latch values are called circuit state.

To model the faults, we introduce new inputs $\bar{f}$ (where $|\bar{f}| = |\bar{c}|$) and $f$, and use $T'(\bar{x}, \bar{i}, f, \bar{s}, \bar{c}, a, \bar{x}')$ defined as:

$$T(\bar{x}, \bar{i}, \bar{s}, a, \bar{x}')[x_i' \leftrightarrow x'_i] \land \bigwedge_{i}(x_i' \leftrightarrow x'_i) \oplus (f \land c_i).$$

Intuitively, $T'$ flips the original $x_i'$ when $c_i$ and $f$ are set; $f$ encodes whether or not to inject a fault, and $c_i = \text{true}$ means that the latch $i$ should be flipped. The single-fault assumption is modelled later.

III. CLASSIFICATION ALGORITHMS

In this Section we describe two algorithms used by OpenSEA. The first one searches for vulnerable latches and spurious alarms: it can accept (fixed or open) tests. The second algorithm searches for protected latches. Both algorithms are sound but incomplete: the classification of the latches they produce is correct, but some latches may be unclassified.

A. Searching for Vulnerable Latches and Spurious Alarms

Algorithm 1 searches for vulnerable latches. The input is a test case $(\bar{I}_1, \bar{I}_2, ..., \bar{I}_t)$ of length $t$, the output is the set of vulnerable latches, and $F$ is the main Boolean formula. Conceptually, $F$ encodes signal “vuln_check” on Fig. 1. We initialize the latches to 0, then in Line 4 and 6 add to $F$ the constraints ensuring the single-fault assumption. The for-loop incrementally unrolls (Line 7) the transition relations of the non-faulty and faulty circuits up to the length of the test, while reading the test inputs. Lines 8–13 are specific to vulnerable latches (we later change them for spurious alarms): we encode that the outputs differ while the alarm is low, and use a SAT solver to incrementally find all vulnerable latches (Lines 10–13). SAT($F\land A$) denotes a SAT call: it returns 0 if the formula is unsatisfiable, otherwise it returns a satisfying assignment for variables $\overline{f}$ and $\overline{c}$. On algorithm termination, vulnerable contains vulnerable latches.
Cactus plot in Fig. 2 shows how the algorithm variations perform on tests with no open inputs, where, surprisingly, the simulation approach is the fastest (in this experiment setup). But the stla variation scales much better with the increasing of open inputs: freeing inputs turned out to have almost no effect on performance, while it exponentially increases the simulation time. In the extreme of all inputs open: we compared stla with model checking approach, where we created the circuit in Fig. 1 and passed it to a model checker (BLIMC) — they perform comparably. Also, with the increasing length of test cases, the simulation approach scales linearly, while stla roughly exponentially. Thus, the designer can choose the appropriate algorithm variation depending on the tests at hand.

As for spurious alarms algorithm variants, stla and stla, the first version performed several orders faster.

B. Searching for protected latches

A latch \( i \) is 1-step protected if the formula

\[
T((x_1, \ldots, x_i, \ldots, x_n), \bar{\tau}, \bar{a}, \bar{x}') \land \lnot a
\]

\[
\land T((x_1, \ldots, \bar{x_i}, \ldots, x_n), \bar{\tau}, \bar{a}', \bar{x}')
\]

is unsatisfiable. Such a check means: no matter in which state the circuit is and no matter which inputs are used, if latch \( i \) flips its value, the error is either already gone in the next time step and the outputs are equal, or the alarm is raised.

Some error-detection and correction methods may take more than one clock cycle to raise an alarm or to recover, making this check too conservative. Hence we similarly define a \( k \)-protected latch by unrolling the transition relation for \( k \) steps.

Another source of over-conservativeness is that the check allows the circuit to start from any state, including unreachable. We use formula \( \text{approx} \) to restrict the starting states \( \tau_1 \): for \( j \geq 0 \),

\[
\text{approx}(j) := \bigwedge_{i=1}^{j} T(\tau_{i-1}, \bar{\tau}_{i-1}, \bar{a}_{i-1}, \bar{a}, \tau_{i-1}) \land \lnot a
\]

\[
\lor \tau_1 = \text{reach}(\bar{\tau}, j)
\]

where \( \text{reach}(\bar{\tau}, j) \) encodes all states reachable from the initial state \( \bar{\tau} \) within \( j \) time steps, the term in parentheses encodes all reachable states from any state after exactly \( j \) steps. Thus, in Eq. 1 we can replace the starting states \( \tau_1 \) by \( \tau_1 \) and conjunct it with \( \text{approx}(j) \). This way we can define a \( jk \)-protected latch where \( j \geq 0, k \geq 1 \).

Algorithm 2 finds all \( jk \)-protected latches. It uses the above two ideas, but instead of checking every latch, it checks them all incrementally (this happened to be faster). This algorithm starts by assuming that all latches are \( jk \)-protected. Line 4 encodes the single-fault assumption. Lines 5–7 encode whether it is possible, without raising the alarm, to diverge the outputs within \( k \) steps or states at step \( k+1 \). If yes, then the SAT solver returns latch \( i \) which leads to divergent outputs or states, and we exclude it from \( \text{protected} \). We repeat this until the formula becomes unsatisfiable, whereupon declare the remaining latches \( jk \)-protected.

Algorithm 2 Searching for Protected Latches

1: procedure \text{FINDPROTECTED}(j \geq 0, k \geq 1)
2: protected := all latches
3: \( F := \text{approx}(j) \)
4: \( F \land \bigwedge_{i=1}^{j} (\bigwedge_{c \in \text{inputs}} c_i = 1) \)
5: \( F \land \bigwedge_{s=1}^{n} T(\tau_{s-1}, \bar{\tau}_{s-1}, \bar{a}_s, \tau_{s+1}) \land \lnot a_s \)
6: \( F \land \bigwedge_{s=1}^{n} T^*(\tau_{s-1}, \bar{\tau}_{s-1}, \bar{a}_s, \tau_{s+1}) \)
7: \( F \land (a_1 \land \tau_1 \neq \tau_0) \land \cdots \land (a_k \land \tau_k \neq \tau_k) \)
8: \( \text{while } \bar{c} := \text{SAT}(F) \text{ do} \)
9: \( \text{protected.remove}(i) \text{ with } \bar{c}[i] = 1 \land i \text{ is unique} \)
10: \( F \land \neg c_i \)
11: \text{end while}
12: \text{end procedure}

1) Implementation: For searching protected latches, OpenSEA accepts a circuit, numbers \( j \) and \( k \). It does not accept neither test cases nor an environment model. We experimented with made-by-us triple module redundancy adder, whose latches are 10-protected (thus, \( j = 1, k = 10 \)). Search of 10-protected latches took \( \approx 100 \) times longer than that of 1-protected latches.

IV. EXPERIMENTS ON INDUSTRIAL DESIGNS

We present preliminary OpenSEA experiments on circuits from IBM microprocessor. We start with some preliminaries definitions and then describe our experiments.

Macros: Large industrial designs are usually divided into sub-components, called macros, and in many cases the protection logic spans over more than one macro. E.g., the parity check may reside in one macro while the parity generation resides in a neighboring macro. For example, in Fig. 3 the parity generation associated with data bus \( D2 \) is performed in a neighboring macro.

Gating: In high performance designs in majority of the cases a fault has no effect on the application [18], since the affected
We run OpenSEA’s vulnerability and spurious alarms check on 15 macros of varying functionality and sizes from 500 to 7k latches. All the experiments were finished within 30min.

We ran tests in which all inputs were kept open. The advantage of keeping the inputs open is that this way OpenSEA can be executed as soon as there is a compiled RTL, and a full functional simulation environment is not required. Table I shows for a few macros the number of latches identified by IBM’s tool as not-protected and also as vulnerable by OpenSEA. This is mainly for validation of the new OpenSEA technology—it demonstrates that OpenSEA indeed detects a significant fraction of the not-protected latches.

| not-protected (I) | not-protected (I) \(\land\) vulnerable (O) |
|------------------|--------------------------------------------|
| 162              | 119                                        |
| 32               | 19                                         |
| 1851             | 535                                        |
| 279              | 109                                        |
| 133              | 110                                        |
| 807              | 606                                        |
| 274              | 111                                        |

Table II presents the number of latches that are identified as protected by IBM’s tool but as vulnerable by OpenSEA. From a practical point of view, this table is significant since its content could indicate a bug in the circuit protection mechanism. However, some of the detected cases are actually irrelevant: cases in which the parity bit was generated externally and passed as input and the vulnerability is due to a mismatching value of this parity bit, which as input was left open. For these cases the tool should be re-executed and analyzed in a larger scope; also, environment assumptions supported by OpenSEA could help to filter out such results. Thus, the last column omits these cases and presents latches that have gating on the way to the alarm and OpenSEA gives an indication that these gating are over-gating. These cases indicate a potential bug and should be reviewed by the design team, along with the counter example provided by the tool.

| protected (I) | protected (I) \(\land\) vulnerable (O) | protected (I) \(\land\) vulnerable (O) \(\land\) non-trivial |
|--------------|----------------------------------------|----------------------------------------------------------|
| 202          | 52                                     | 21                                                       |
| 548          | 174                                    | 110                                                      |
| 151          | 54                                     | 54                                                       |
| 834          | 206                                    | 90                                                       |
| 1932         | 208                                    | 199                                                      |
| 104          | 27                                     | 4                                                        |
| 615          | 80                                     | 26                                                       |
| 1320         | 133                                    | 91                                                       |

Vulnerable latches due to over gating: Latches that are detected as protected by InsightER, but whose flipped value propagates to the macro output due to over gating. Such latches may cause silent data corruption.

Latches causing spurious alarms: Latches for which the alarm rises, although their flipped values do not propagate to the macro output. Such latches may cause redundant recoveries, impairing the circuit performance.

In the second batch of experiments we used OpenSEA to find spurious alarms. Namely, cases in which the alarm is being raised even though the output is not being affected.
The results are in Table III. At first, we found many spurious alarms. But many of them were irrelevant due to injecting faults into protection circuit itself. OpenSEA allows one to configure latches into which to inject faults. When we excluded the latches of the protection circuit, the number of spurious alarms dropped. Each case left is a potential performance/power issue which may indicate that the existing gating is not tight enough and should be improved. This indication is not provided by IBM’s internal tool or by any other tool we are familiar with.

| protected (I) | spurious alarm (O) | spurious alarm (O): excl. protection logic |
|---------------|-------------------|------------------------------------------|
| 202           | 86                | 57                                       |
| 660           | 244               | 122                                      |
| 1932          | 4                 | 4                                        |
| 2104          | 3                 | 0                                        |
| 439           | 51                | 28                                       |

TABLE III: The number of latches whose faults can cause spurious alarms found by OpenSEA (written “spurious alarm (O)” and protected by InsightER (written “protected (I)”)). For spurious alarms, we run OpenSEA only on the latches found to be protected by InsightER.

Finally, Table IV presents the time consumption of OpenSEA’s search algorithms for vulnerable latches and for spurious alarms. Obviously, time consumption is very low.

| # latches | Time: searching vulnerable latches | Time: searching spurious alarms |
|-----------|-----------------------------------|--------------------------------|
| 434       | 7.45 sec.                         | <1 sec.                        |
| 582       | 9.65 sec.                         | 1.84 sec.                      |
| 590       | 9 sec.                            | 2 min. 23 sec.                 |
| 7061      | 22 min. 23 sec.                   | 2 min. 31 sec.                 |

TABLE IV: Timings of OpenSEA algorithms

V. RELATED WORK

Fey, Frehse and Drechsler [14] classify components into (i) vulnerable, (ii) protected, (iii) dangerous, and (iv) unknown. To this end, they use a bounded model-checking based technique to compute the circuit robustness, which is the ratio of the protected latches to all the latches. Furthermore, by under- and over- approximating the reachable states they can compute upper and lower bounds on the robustness. Our approach for computing vulnerable and protected latches is very similar to theirs. The differences are: (i) we can use real test cases, while they consider only symbolic test cases, (ii) moreover, we study the question of false alarms, (iii) furthermore, we introduce the notion of “environment model” which is handy for checking practical designs, (iv) in contrast, they study ATPG-based algorithms and consider optimization “dominator”.

A year later, the same three authors together with Arbel and Yorav in [15] proposed a more efficient approach to classify the components. This time, they use interpolation for an over-approximation of the reachable state space and compute fixed-points. This way, only states that are relevant to the property to prove are considered.

In 2006, Krautz et al. [16] proposed a way to evaluate the coverage of error detection logic using BDDs. They used a fault injection model similar to our BMC based approach in which they compare a fault-free device with a faulty one. The output of their fault injection model is defined by a property checker that defines multiple properties by comparing primary outputs of both circuit copies. A sequential equivalence check of this circuit is performed up to a defined number of time steps by creating a BDD representation. The number of input combinations that make properties true are counted. Among other properties, they count a property similar to our definition of vulnerabilities and the number of injected faults. A coverage is computed using these numbers.

Holcomb et al. [20] showed another way to compute the failure in time rate by performing a system-level analysis. In contrast to our algorithms, their methods rely on formal specifications. Our approaches only need to know which output is the alarm output.

In 2014, Arbel, Koyfman, Kudva and Moran published a structural approach to detect parity-protected memory elements [19]. For this purpose, they first search for potential error detection circuits and for latches that are potentially protected by those using functional analysis. Afterwards, they use SAT-calls to prove that these latches are indeed protected by the parity net. The unique characteristic of their method is that they analyze a circuit locally rather than looking at the behavior of the entire system. Their method can be applied whenever error checker latches are present, which is not always the case though.

Finally, methods that systematically construct robust systems [21] might make our work and all methods to verify error detection and error correction obsolete one day. However, as long as these intelligent compilers are not yet perfect (if they will ever be) verification of circuits will stay important.

VI. CONCLUSION

In this paper, we presented soft-error analysis framework OpenSEA to find vulnerable latches, protected latches, and to find spurious alarms. OpenSEA supports many variations of the algorithms—SAT-based, BDD-based, and enumerative—and many SAT solvers as a back end. The algorithms can use symbolic, semi-symbolic, and concrete tests. In the experiments, we run OpenSEA on industrial macros from IBM to search for spurious alarms, vulnerable, and protected latches. We explained why not all the bugs found are real and described the OpenSEA features to avoid such spurious bugs. The source code, benchmarks, and documentation can be found at [https://extgit.iaik.tugraz.at/scos/soft-error-analysis/]

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