**Phase difference analysis technique for parametric faults BIST in CMOS analog circuits**

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**Abstract:** Detection of parametric faults is a crucial issue due to the large variation of the fabrication process, which provide a range of acceptable parameter deviations in analog circuits. This paper presents a phase difference analysis technique, which is sensitive to the parametric deviations and allows a tolerance band of passive analog components. Test operations can be simply achieved by comparing the phase difference between a reference clock signal and a reconfigured circuit-under-test (CUT) as an oscillator. The difference of phase characteristics between the two signals can be utilized as an indicator for a fault signature, which can be characterized by a compact digital circuit comprising a counter and logic components. Simulation of faults detection reveals a high faults coverage, high-speed testing, and tolerance band controllability. The proposed technique has offered a fully on-chip BIST in 0.18-µm CMOS standard technology with no external test equipment required.

**Keywords:** built-in self-test, oscillation-based test, parametric faults detection, analog low-pass filter

**Classification:** Integrated circuits

**References**

[1] J. W. Jeong, et al.: “Robust amplitude measurement for RF BIST applications,” IEEE European Test Symposium (ETS) (2015) 1 (DOI: 10.1109/ETS.2015.7138762).

[2] W. San-Um and T. Masayoshi: “Impulse signal generation and measurement technique for cost-effective built-in self test in analog mixed-signal systems,” IEEE Int. Midwest Symp. Circuits and Systems (2009) 1195 (DOI: 10.1109/MWSCAS.2009.5235949).

[3] G. Hu, et al.: “Oscillation test strategy for analog filters by monitoring output voltage and supply current,” Tsinghua Sci. Technol. 12 (2007) 78 (DOI: 10.1016/S1007-0214(07)70088-3).
1 Introduction

Analog circuits are the interface between natural signals and the digital processing. This role has rapidly gained a significance due to the need for high accuracy sensors and converters in modern systems. Nowadays, the nanometer-scale technology brings the feasibility of integrating analog circuits together with digital circuits into the same chip. The integration density is rapidly increased as well as the complexity of circuits, resulting in the greater demand for a suitable testing strategy. However, testing such a system is cumbersome especially, in the analog part. Owing to the very large variations in property, structure, and performance, designing the analog testing methods become a challenge. Moreover, characterization of the parametric deviations is difficult due to the allowable of the tolerance bands in the specification margins. Therefore, testing methods of the analog circuits are costly, time-consuming and may encounter issue of reduced performance due to the introduction of additional circuit components.

Built-In Self-Test (BIST) received considerable attention as a means of reducing testing time while also eliminating the need for costly and time-consuming from...
using external test equipment. Several BIST techniques for analog and digital circuits have been proposed in the last decade. Meanwhile, most of BIST techniques for the digital circuits are designed to be a fully on-chip, there is still less common approach for built-in testing hardware in analog circuits. Several approaches have focused on the monitoring of circuits parameter such as amplitude [1, 2], current [3], and DC-offset error [4]. These methods provide an accurate measurement, however typically requires a high-precision test stimulus such as a linear-ramp generator [5], sinusoidal waveform [6] as well as pseudo-random patterns [7], which is relatively difficult to generate on-chip. In addition, detection the parametric variation is usually rather crucial. A fast-Fourier transformation (FFT) is used in [8] in order to analyze the circuit specifications error. High sensitivity for parametric deviation is the feature of this technique but requires an external response analyzer. Recently, an oscillation-based test (OBT) method is widely gained the attention in the analog and mixed-signal circuits. The underlying idea is to eliminate the need for external testing generation. In other words, the CUT can be transformed into the oscillator by applying slight modifications. Afterwards, the frequency characteristic is simply observed such as amplitude, a center frequency, and distortion. The oscillator-based BIST for the analog filters is proposed in [9, 10], the DC gain, ripple, and the cut-off frequency are measured with high faults coverage. However, the pass/fail decision is based on monitoring and observing technique. The hardware-based pass/fail decision for OBT is presented in [11, 12]. In this case, a simple comparator and counters are employed in order to convert the frequency into a number that represents a faults signature. Although, this technique achieves an on-chip pass/fail decision and contributes the tolerance bands in analog circuits, the small deviation in phase and frequency may lead to undetectable faults.

Consequently, the BIST based on a phase difference analysis technique for the analog circuits is presented in this paper. The test operation is achieved through the detection of phase shifting between two signals (i.e. the circuit-under-test and the reference clock). The faults signature is simply generated, and diagnosed by digital circuits, including a counter and basic logic components. The test stimulus generation and pass/fail decision are accomplished entirely on-chip, and also offers the range of tolerance in the passive analog components with eliminating the need for the external test equipment.

2 Phase difference analysis technique

In general, there is no monotonic testing design for the analog circuits due to the large variation of the structure, performance, and specifications. The practical way is to search for methods that improve the observability of the testing process. Such methods can be performed by BIST system, which the testing process can be modified depending on the features of a circuit-under-test (CUT). The main purpose of BIST is detecting all the possible faults in CUT for both catastrophic and parametric faults. Fig. 1 illustrates the demonstration of the faults signature generation using the phase difference detection. The signal $Q_A$ and $Q_B$ are compared by the reference clock signal. It can be clearly seen that even though
these two signals are slight variation in frequency, the output responses are largely different. This feature reveals the sensitivity to the phase shifting, which cannot be occurred by the frequency or amplitude detection, and suitable for the BIST in oscillation system.

2.1 The proposed technique for the BIST
Fig. 2 depicts the block diagram of the proposed BIST technique. The system comprises a clock generator, two counters, the digital logic components and the Exclusive OR (XOR) gate as a basic phase detector circuit. Oscillation reconfiguration technique is used in order to transform the CUT into the oscillator in the test operation. Then, the phase shifting of the modified CUT and the reference clock is compared together by the XOR gate, which provides the signature for any circuits characteristic. The faults signature is subsequently accumulated by the digital counter 1 in the binary number format, which is typically characterized by the digital logic components. Additionally, the testing operation period can be determined by the digital counter 2 that stores the number of the reference clock pulse, therefore, the test response (Pass/Fail) of the system is exposed automatically.

2.2 Faults detection
According to the Section 1, Due to the small deviation in parametric components values and the tolerance bands in the specification margins, pass/fail decision in
analog circuits is relatively cumbersome. The method that determines whether the circuit is fault-free or faulty is important for achieving the testability feature. As mentioned, the small deviation of phase shifting between two signals can provide an identical output response as the faults signature. For this reason, the simplest way to identify the correlation of signature is by converting into the binary number format and comparing each bit in the same period. The on-chip pass/fail decision circuit is shown in Fig. 3 comprises two counters and the digital logic gates. While the 8-bit counters are used in order to transform the phase correlation into the binary number, another 4-bit counter determines test operation period, according to the amount of reference clock pulses. Furthermore, this technique offers allowable tolerance bands, which indicates by “don’t care” in the three least significant bits. Otherwise, the large correlation in phase shifting will cause the extremely difference number that indicates only on the most significant bits (5–7). For example, the 50 kHz clock reference and 2 ms testing time are defined, so the binary number in counter 2 implies “0101”. In this period, the binary number in counter 1 will indicate the testing response and be compared to the fault-free signature, in this case is “01111XXX” (X means “don’t care”).

3 The system architecture

3.1 A modified Sallen-Key low pass filter as the oscillator

In order to detect the phase variation, it is necessary to design the self-oscillation topology for the CUT. The Sallen-Key second-order active low-pass filter is utilized as illustrated in Fig. 4. The circuit is operated as its designed in the normal condition. In the test condition, the circuit is converted into the oscillator based on the Barkhausen criterion as follows

\[ |A(j\omega_0)H(j\omega_0)| = 1 \]  \hspace{1cm} (1)

\[ \angle A(j\omega_0) + \angle H(j\omega_0) = 0 \]  \hspace{1cm} (2)

where \( A(j\omega_0) \) and \( H(j\omega_0) \) are the transfer function of the system and feedback loop, respectively. This criterion implies that the oscillation feature can occur if there are no attenuation and phase shift in the feedback system. For this reason, the additional inverter is applied in order to perform the feedback loop, represented in the shaded area. Note that, when the test operation is enabled, the filter is a self-oscillation system with 183 kHz frequency at the fault-free condition.
3.2 An operational amplifier

The two-stage operational amplifier (Op-Amp) with RC frequency compensation circuit is used for the low-pass filter. Fig. 5 depicts a schematic of the Op-Amp consists of a differential input stage represented by transistors N1 and N2, current mirror source represented by transistors P2 and P3, and a PMOS amplifying represented by transistors P4. This circuit is operated by single power supply \( V_{DD} \) and current source P1. The required gain and bandwidth of the amplifier are defined by the simulation. The DC gain and power dissipation can be expressed as

\[
A_V = \frac{2g_{mN2}g_{mP4}}{I_{N5}(\lambda_{N2} + \lambda_{P3})(\lambda_{N5} + \lambda_{P4})} 
\]

\[
P_{\text{diss}} = (I_{N3} + I_{N4} + I_{N5})(V_{DD} + |V_{SS}|)
\]

where \( g_m \) and \( \lambda \) are the N/P-transconductance and channel length modulation of MOS transistors, respectively. In addition, simulation results from HSPICE software imply that the designed Op-Amp can achieve a unity gain bandwidth (GBW) more than 60 MHz with a load capacitance of 1 pF and phase margin of 57°. The DC gain of the Op-Amp is higher than 75 dB at 30 µA bias current and the
measured power dissipation is approximately 190 µW. The transistor aspect ratio of the Op-Amp is also shown in Table I.

4 Simulation results

This section describes the simulation of testing results when the CUT is operated in the test mode. Several catastrophic faults were injected, including short, open, gate-drain-short (GDS) and gate-open (GO). While the short circuits can be realized as bridging defects between two metal lines in an integrated circuit that can be simply modeled by a low resistance connecting between nodes. The open defects represent a line opening and floating inputs, which is usually replaced by inserting a parallel combination of a large resistance and a small capacitor over the possible signal paths. The parametric faults are modeled by varying the components value based on the acceptable range for the specification violation. In this case, the fault tolerance band is determined to ±20% of the overall passive components. Fig. 6 shows the output waveform in transient of the fault-free and +10% resistor values of the faulty circuit. It is clearly seen that the small parameter deviation can produce the phase difference (shaded region), which lastly detected by the 8-bit binary number. The 20 kHz reference clock is employed and 0.8 ms of the test period is determined. At

| MOS Transistors | Aspect Ratio (W/L) |
|-----------------|-------------------|
| N₁–N₂           | 60                |
| N₃–N₄           | 30                |
| N₅              | 180               |
| P₁              | 30                |
| P₂–P₃           | 40                |
| P₄              | 45                |

Table I. Transistor aspect ratio of the operational amplifier

![Fig. 6. The output waveform in transient between the fault-free and faulty circuit.](image-url)
this period, the values of the counter indicate at 199 with two least significant bits, so the tolerance band of this system is in the range of ±3 (i.e. “10001XX”). Table II summarizes the simulation results of the proposed technique. It is apparent that those catastrophic faults injected into the CUT were totally detected. This is caused by the extremely failure in the filter, which is clearly indicated by the counter. Most of the injected parametric faults were also captured (83.3%) with only two undetectable cases (R2 and C1). This may imply that these components are less sensitive to the phase and frequency of the system. In addition, the undetectable tolerance band in the values of passive components was also evaluated, as summarized in Table III. In order to reduce these tolerance bands, we suggest that the number/amounts of don’t care bits should be reduced, while clock frequency and the testing time should be adjusted to the appropriate value. Fig. 7 also shows the overall circuit layout diagram in 0.18-µm standard technology.

Table II. Summary of faults detectability of the proposed system

| Circuits | Fault Types | Details | Injected | Detected | Faults Coverage |
|----------|-------------|---------|----------|----------|-----------------|
| Op-Amp   | CF          | Short   | 10       | 10       | 100%            |
|          | CF          | Open    | 10       | 10       | 100%            |
|          | CF          | GDS     | 8        | 8        | 100%            |
|          | CF          | GO      | 8        | 8        | 100%            |
| Filter   | CF          | Short   | 6        | 6        | 100%            |
|          | CF          | Open    | 6        | 6        | 100%            |
|          | PF          | ±20% Res. | 8   | 7        | 87.5%           |
|          | PF          | ±20% Cap. | 4  | 3        | 75%             |
| Total    |             |         | 60       | 58       | 96.67%          |

CF = Catastrophic Fault, PF = Parametric Fault

Table III. Summary of undetectable bands in the passive components.

| Passive Components | Undetectable Range |
|--------------------|--------------------|
| R1                 | −10%~+5%           |
| R2                 | −20%~+25%          |
| R3                 | −20%~+10%          |
| R4                 | −5%~+10%           |
| C1                 | −20%~+25%          |
| C2                 | −10%~+5%           |

Table IV. Comparison of the testing time.

|                      | Conventional Technique | [12] | This work. |
|----------------------|------------------------|------|------------|
| Time (ms)            | 1.0                    | 2.4  | 0.8        |

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DOI: 10.1587/elex.15.20180175
Received February 16, 2018
Accepted April 2, 2018
Publicized April 13, 2018
Copyedited May 10, 2018
5 Conclusion

The BIST based on a phase difference analysis technique for the analog circuits has been presented. The testing technique is based on the detection of phase shifting between a reference clock signal and a modified circuit-under-test (CUT) as an oscillator, which is represented by the active Sallen-Key low pass filter. This technique has provided faults coverage of 96.67%, where all catastrophic fault of the CUT can be detected and the faults tolerance band of all passive components is determined to ±20%. The implemented BIST can eliminate the need for external test equipment by using a compact digital circuit which can be fully designed on-chip. This work has proposed a significantly high fault coverage and fully on-chip BIST technique for analog circuits as well as the potential of reducing the testing time as shown in Table IV.

Acknowledgment

This work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Cadence Design System, Mentor Graphics, Rohm Corporation and Toppan Printing Corporation.