Energy efficient neural stimulator with dynamic supply modulation

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This paper reports an automatically reconfigurable series–parallel switched-capacitor step-down DC–DC converter for neural stimulation applications, fabricated with a 0.13 \( \mu m \) standard complementary metal oxide semiconductor process. The stimulator chip can generate pre-programmed biphasic or dynamically programmed arbitrary current waveforms, up to \( \pm 127 \mu A \) peak with 7-bit resolution. To improve the power efficiency, the supply voltages of the stimulating current sources are dynamically modulated following the output voltage. The functionality of the stimulator is verified \textit{in vitro} using parylene-based micro-electrode arrays in phosphate-buffered saline.

Introduction: Neural stimulation is currently used as an effective treatment in patients suffering from certain neurodegenerative diseases (e.g., epilepsy). In a chronic implantation of such systems in the human body, the battery replacement is an invasive procedure. Therefore, both the energy efficiency and form factor play critical roles in the viability of an implantable integrated system. Even though switched capacitors may be used to deliver charges to the neural tissue with high precision, they require large off-chip capacitors to handle charges [1]. A compact neural stimulator usually consists of a controllable current source, mostly realized as a current digital-to-analog converter (IDAC). Since the stimulation current range and resolution of the IDAC depends on the target application, the power consumption of the stimulator depends mainly on the supply voltage. In a conventional current stimulation circuitry, the supply voltages are fixed and set by the highest voltage value that is expected to be created across the neural tissue [2]. In other words, even if the voltage created across the tissue is small, the supply voltage remains at a high value; therefore, the power or energy consumption of the current stimulator will be unnecessarily high. To overcome this issue, supply modulation using charge pumps was introduced to improve the stimulator efficiency [3]; however, the charge-pump circuitry itself suffers from a low conversion efficiency (<60\%). An alternative architecture is a series–parallel switched-capacitor DC–DC converter, which can achieve high conversion efficiencies (>80\%). In this paper, a dynamically reconfigurable series–parallel DC–DC converter for efficient current stimulation is reported.

System and circuit design: The proposed neural stimulator chip, targeting retinal stimulation of rats for experiments in visual cortex/mid-brain and hippocampal plasticity, consists of a 7-bit current DAC capable of supplying up to \( \pm 127 \mu A \) current with a variable supply voltage driven by a reconfigurable switched-capacitor DC–DC converter within \( \pm 3 \) V (Figure 1). An array of comparators monitors the electrode voltage continuously and determines the appropriate conversion ratio such that a minimum of 150-mV voltage headroom is maintained across the IDAC transistors. The clock signals \( \phi_1 \) and \( \phi_2 \) for the DC–DC converter are created using on-chip relaxation oscillators and non-overlapping clock generator circuits.

The current DAC is realized as a parallel array of binary-weighted NMOS and PMOS transistors. The channel length of each transistor is large (\( 5 \mu m \)) to increase the output resistance without requiring cascode to increase the voltage headroom and efficiency. An additional current source with half the size of unit cell is added to improve the linearity and compensate for the supply jumps during specific DAC current transitions. The schematic and measured linearity performance of the 7-bit current DAC are shown in Figure 2. The unit element currents \( I_{LSB,p} \) and \( I_{LSB,n} \) are generated on chip using bandgap voltage and reference current circuits. The chip can generate a biphasic current waveform, whose parameters can be programmed and stored on the chip, as well as any generic current waveform that is dynamically loaded into the chip.

A reconfigurable switched-capacitor DC–DC voltage converter is designed to generate the necessary DC power supplies (Figure 3). It accommodates voltage conversion ratios of 5:1, 3:1, 2:1, 3:2 and 6:5 to step down positive rail (VDD = 3 V) when \( \phi_a \) is active (anodic phase) and negative rail (VSS = –3 V) when \( \phi_c \) is active (cathodic phase). A total of 34 switches are used in this scheme to choose the proper series–parallel configuration of the flying capacitors to achieve the required conversion ratio. \( S_1, S_{12}, S_{34}, S_{56}, S_{78}, S_{910} \) are PMOS switches, while \( S_2, S_4, S_6, S_{11}, S_{12}, S_{14} \) are NMOS switches and the remaining switches are transmission gates (TG). As shown in Figure 4, to achieve conversion ratios of 6:5 and 5:1, five independent flying capacitors, each 50 pF, are used, while these capacitors are combined for other conversion ratios to boost the efficiency. The switching frequency, size of the switches, and the flying capacitors are optimized for minimizing the bottom-plate capacitance and gate-drive losses. The output capacitor value is chosen as 500 pF to reduce the ripple to less than one LSB.

System measurement results: The neural stimulator chip was fabricated in a 130 nm CMOS process (Figure 5a). The chip was interfaced with an Arduino microcontroller board for programming the stimulation waveforms. The measured power efficiency of the current stimulator for a resistive load value of \( R = 17.26 \) k\( \Omega \) confirms the improvement over conventional approaches with a constant supply voltage (Figure 5b). A
maximum of 20% improvement was observed for a 30 μA output current. Figure 5c shows the DC–DC converter output levels for different conversion ratios. The DC–DC converter maintains an efficiency above 60% (85% peak) in its range of operation.

Figure 6a demonstrates the electrode voltage in response to a periodic balanced biphasic and a sinusoidal current waveform, along with the dynamically changing supply voltage value. The functionality of the neural stimulator interfaced with parylene-based microelectrodes was also investigated. The platinum electrode diameter was 160 μm and it was immersed in a 1X phosphate-buffered saline (PBS) solution. Biphasic (±5 μA) and sinusoidal (30 μA peak, 40 Hz frequency) current waveforms were generated and electrode voltages were recorded (Figure 6b).

**Conclusion:** A neural stimulator chip, capable of supplying pre-programmed biphasic or dynamically programmed arbitrary current waveforms having peak values of ±127 μA with 7-bit resolution, featuring dynamic supply modulation for power efficiency improvement, is demonstrated in a 130 nm CMOS technology.

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