The Issues on Time Synchronization Technology in Time Triggered Ethernet

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Abstract. Based on the idea of time-triggered, global unified high precision time synchronization is the foundation of network deterministic communication. In the process of time synchronization, clock synchronization algorithm, transmission delay, clock drift and so on will affect the accuracy of clock synchronization. It is a great technical challenge to realize high precision and reliable clock synchronization. This paper collates and analyses the relevant literature, first introduces the time-triggered Ethernet, then analyses the time synchronization protocol that can be used for high-precision clock synchronization, reviews the development status of time synchronization technology and makes an overall analysis. Finally summarizes the clock synchronization difficulty and prospects the development trend of the time synchronization technology.

1. Introduction

In recent years, with the continuous development of avionics technology, Distributed Integrated Modular Architecture (DIMA) system has become the main development direction of future avionics systems due to its high flexibility due to its distributed computation [1]. The distributed deployment of hardware modules and processing resources of DIMA system allows heterogeneous processing modules to carry out parallel execution of functional tasks through the interconnection network, so higher requirements are put forward for the real-time, deterministic, reliable and fault-tolerant capability of communication network [2].

Time-triggered Ethernet combines the real-time and deterministic communication with traditional Ethernet, which can effectively improve the real-time and reliability of communication system and meet the demand of network communication of distributed avionics system. The idea of time trigger is to communicate according to the pregenerated task scheduling table based on the global unified time. Communication events can be reasonably arranged during the generation of scheduling table to avoid network conflicts and other problems, improve network utilization and have strong determinism. Therefore, the high-precision time synchronization of each terminal node in the network is particularly critical, which is a prerequisite for the normal communication between terminal nodes. Moreover, any error in the global clock may cause the system to fail. The accuracy of time synchronization directly affects the communication efficiency. If the synchronization error is large, the impact of maximum error on the system should be considered when generating the schedule table, thus reducing the communication efficiency. TTE is a distributed switching network in which time synchronization information needs to be forwarded by switch equipment. In the process of synchronization, factors such as node forwarding delay, clock drift, network delay and time synchronization algorithm all affect the precision of time synchronization. Therefore, it is very difficult to realize high precision and high reliability of time synchronization in the network.
Time synchronization is the basis of time-triggered Ethernet technology and has important research value. In this paper, relevant literature is sorted out and analyzed, the time synchronization technology is introduced in detail, the development process of the technology is roughly described, and the main ideas of various time synchronization methods are introduced and briefly summarized.

2. TTE Overview
Time-triggered Ethernet [3] is a time-triggered network protocol added on the basis of IEEE802.3 Ethernet, which supports time-triggered communication as well as traditional Ethernet communication. The traditional Ethernet is driven by event trigger and only communicates when the network has communication demand. It has good flexibility, but it is difficult to guarantee the real-time and deterministic performance of the system when the link load is heavy. The time trigger mechanism synchronizes the time of all nodes in the network to ensure the global time consistency, and then communicates on time according to the task scheduling table generated in advance. In the design of scheduling table, communication tasks can be reasonably arranged to avoid multiple communication tasks being sent at the same time in a certain period, resulting in excessive network load, queuing or conflicts, which will affect the network communication efficiency. Contrast the following.

| Type          | TT  | ET   |
|---------------|-----|------|
| Communication | Time| Demand |
| The real time | Strong | Not sure |
| Deteministic  | Strong | Weak  |
| Flexibility   | Poor | Good  |
| Reliability   | High | Low   |
| Complexity    | High | Low   |

TTTech offers a number of mature commercial products that are already used in aerospace and automotive electronics. The US Orion manned spacecraft adopted a 1000base-CX physical layer and double-redundant configuration TTE network integrated interconnection scheme [4]. The European Space Agency's Ariane 6 launch vehicle and Lockheed Martin's Sikorsky S-97 helicopter have also been used [5]. In 2008, TTTech released the TTEThernet specification, and the SAE AS6802 Time-triggered Ethernet standard was formed and released by SAE in November 2011 [6].

With the application and development of TTE, related research work has been carried out in China. Due to the late start in China and the influence of foreign blockade information, most of them are theoretical research and simulation experiments. However, technical progress has been made recently. The TTE switch and terminal system developed by the School of Communication Engineering at Xidian University has been applied to the Long March 5B carrier rocket and has completed the on-orbit test of the "Time Triggered Ethernet Spaceborne Prototype System" for the first time. It has laid a solid foundation for the follow-up research of large and complex spacecraft technology in China.

3. The Time Synchronization Technologies
In deterministic time-triggered communication, clock synchronization is the prerequisite for the system to communicate normally. After the establishment, the synchronization mechanism of devices will run periodically to ensure that the clocks between devices do not generate large offset.

3.1. Time Synchronization Protocol
At present, Ethernet time synchronization technology is mainly based on NTP [7], IEEE1588 [8], AS6802 time synchronization protocol to achieve time synchronization. NTP protocol is mainly used in traditional Ethernet, and its synchronization accuracy can reach the millisecond level. However, with the rise of real-time network research, the demand of aerospace and other fields is no longer satisfied with the synchronization accuracy at the millisecond level. Compared with NTP protocol,
IEEE 1588 and AS6802 time synchronization protocols can achieve sub-microsecond time synchronization accuracy, which can meet higher precision time synchronization.

The IEEE 1588 protocol is a kind of master-slave time synchronization. Precision Timing Protocol (PTP). IEEE 1588 protocol is generally implemented by combining hardware and software, synchronization algorithm is implemented by software, and timestamp is acquired by hardware. The protocol is divided into two parts to realize time synchronization: 1. The optimal master clock algorithm is adopted to select the best master clock, and the master-slave topology is established, and then the synchronization system is established in the whole network; 2. Calculate the time deviation between slave nodes and master nodes through the exchange of synchronous messages between master and slave nodes, and correct the synchronization between local clock and master clock. Synchronization with the master node through its principle from the node to send and receive data frames, record synchronization request frame, the following message, delay frame and delayed response frame between two nodes of the delivery and arrival time, calculate according to the four time information from node link transmission delay and the local clock time deviation with the master node, and the unknown link transmission delay and time deviation, then time deviation correction from the local clock of node, to achieve the time synchronization between the master-slave node. The synchronization process is as follows:

Perform local clock correction from the node according to the calculated time deviation offset.

It can be found that the above formula holds on the premise that the round-trip delay of the master and slave nodes is equal. However, in practical application, even if the master and slave nodes are directly connected, the downlink delay and uplink delay are not equal at the order of nanoseconds. If other network devices are passed in the transmission, this asymmetry can be extended to the order of microseconds or even milliseconds. Additional asymmetric algorithms are required to compute and compensate link delays. Secondly, the low reliability makes it impossible to conduct fault-tolerant isolation on potential failure nodes in the network. The precision of time synchronization is too dependent on the master node. If the master node clock fails or the data is lost during transmission, the result of synchronization will be greatly affected, which has certain limitations. When the number of nodes in the network is large, the optimal master clock algorithm requires a large amount of computation, which not only consumes more system resources, but also requires high data operation and processing capacity.

Compared with the 1588 protocol, the AS6802 protocol does not select the time of a certain network device as the best master time when implementing the time synchronization between various devices in the network but adopts the distributed time synchronization method. At the same time, in
the process of time synchronization, the fault-tolerant mechanism is added. When a limited number of nodes fail in the network, the other nodes with the same priority can still achieve reliable high-precision clock synchronization, which ensures the stability and reliability of time synchronization. The AS6802 protocol establishes and maintains the clock synchronization of the global network through protocol control frame periodic interaction between node devices and the cure algorithm, compression algorithm, transparent clock, etc. Cluster detection algorithm is used to monitor the synchronization status of the current network. It provides a strong foundation and guarantee for the realization of high precision and high reliability time synchronization service.

The synchronization process is as follows: The synchronization master (SM), the synchronization client (SC) and the compression master (CM), according to the role of each node in the time synchronization process. First by the SM send CM protocol control frame, CM after received by multiple SM protocol control frame, by maintaining a algorithm guarantees the PCF CM received frame sequence order of consistent with the order of the SM send PCF, and then according to the PCF frame of transparent clock and the time of arrival of the PCF frame points through the compression algorithm to select the appropriate point in time, such as the local clock correction. A new PCF frame is then generated and sent out. The SM and SC receiving the new PCF frame correct the local clock according to the PCF frame to complete the time synchronization.

![Figure 2. AS 6802 two-step synchronization method](image)

For a cluster with a large number of nodes, if the synchronization method of AS6802 is used to realize the time synchronization of all nodes, it needs to be divided into multiple sub-clusters. For such a network with a large number of nodes, the computation of maximum link delay is large, and the accuracy of transparent clock is low. It is difficult to realize, takes up a lot of resources, and the synchronization process is more complicated. Compared with IEEE1588 protocol, AS6802 protocol has better deterministic and fault-tolerant capabilities and can achieve higher synchronization accuracy. However, corresponding implementation methods are also more complex.

### 3.2. The Research Status

IEEE1588 protocol has attracted much attention and been widely recognized since it was proposed. So far, many versions have been developed. The most widely used version is IEEE 1588v2 [9], and its synchronization accuracy is also the highest. Many foreign manufacturers have developed their own products based on IEEE 1588 protocol. More Than IP company and Arasan company have successively launched the MAC module supporting IEEE 1588 protocol, which can realize clock synchronization with an accuracy of 50ns [10]. Hirschmann USES FPGA chip to realize IEEE1588 message detection and timestamp capture, with synchronization accuracy up to 60ns [11]. The domestic application of IEEE 1588 is also being gradually promoted, and some manufacturers in related fields have produced equipment that can implement the 1588 protocol.

In terms of time synchronization, literature [12] analysed some of the main factors affecting synchronization accuracy in the network system and proposed to improve and test the system through crystal compensation and OffsetTime filtering, and finally achieve a high-precision synchronization
effect. Literature [13] considered the impact of time stamp accuracy on the synchronization accuracy of the IEEE1588 protocol, and estimated the frequency offset and time offset between the slave clock and the master clock through the Kalman filter algorithm, and then corrected it to improve the synchronization accuracy. Literature [14] uses FPGA to implement the clock synchronization module in the form of a digital circuit, and accurately captures the message timestamp through hardware and dynamically compensates for crystal frequency drift. And it is verified through experiments that its synchronization accuracy can reach sub-microsecond level.

Literature [15] analysed and studied the TTE time synchronization mechanism before the SAE AS6802 standard was formed and proposed a method to generate a schedule. And in the construction of a specific network scene, it was simulated and verified. Literature [16] designed and simulated the clock synchronization process and key algorithms based on the AS 6802 protocol. The measured synchronization accuracy can reach 10 ns. Literature [17] proposed a FPGA-based AS6802 protocol + IEEE1588 protocol implementation, and carried out board-level debugging, but it failed to consider the actual delay introduced on the PHY side during the board-level debugging process. And the lack of TTE network communication scenario verification. Literature [18] does not use SM or CM PCF frame to obtain information, but uses a self-designed measuring device to obtain PCF frame, and calculates the key parameter calculation cost when the CM runs the compression function based on the information carried in the PCF frame. Literature [19] improved the multi-domain clock synchronization method of TTE. In a large-scale deterministic network, each sub-function module is divided into a synchronization domain, and an independent synchronization clock is run, which also ensures the security of each sub-module clock source. Designed a multi-priority communication rule under multiple synchronization domains and verified its accuracy and safety. Based on AS6802 protocol, literature [20] proposed that in the synchronization algorithm compression stage, different weights should be given to clocks with different crystal oscillator accuracy to improve the network synchronization accuracy. Reference [21] proposed the method of compensating the clock with progressive clock compensation after filtering clock noise with TT based on spatial application and proved its feasibility. Literature [22] proposed a TTE clock compensation algorithm based on robust regression. Through the algorithm, the local time and global time of the node are estimated and dynamically compensated to solve problems such as direct compensation for possible clock jumps.

Literature [23] researched the fault-tolerant mechanism defined in the AS6802 protocol, designed a set of time-triggered Ethernet fault-tolerant clock synchronization mechanism, and completed simulation verification. Literature [24] proposes to partition processing according to the type of traffic in the network and adds message security control to ensure communication security. Literature [25] uses Bayesian networks to analyse the system reliability of TTE in ring topology, mesh topology and star topology. The star topology has the highest reliability in the case of redundancy.

4. Conclusions

Clock synchronization is an important basis for time-triggered Ethernet deterministic communication. This article discusses the research progress of TTE time synchronization protocol and related algorithms in recent years, and fully analyses the principles, advantages and disadvantages of each time synchronization protocol. Although the synchronization accuracy of the 1588 protocol can reach the nanosecond level, its synchronization result is too dependent on the master clock, and its reliability and fault tolerance are poor, which makes its application in avionics system networks have certain limitations. The AS6802 protocol is a time synchronization protocol specified by TTE, with better synchronization accuracy and fault tolerance, but it is more complex. Most of the current research work is limited to simulation experiments. How to implement it in the airborne network or other real environments requires more in-depth research in the future.

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