Design and Investigation of F-shaped Tunnel FET with Enhanced Analog/RF Parameters

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Abstract
In this manuscript, a novel physically doped single gate F-shaped tunnel FET is simulated and optimized. The designed configuration is well optimized and analyzed for different source thickness, source length, drain length with different lateral tunneling lengths between the source edge and gate dielectric. Also, we optimized some stand-points like threshold voltage, $I_{ON}$ to $I_{OFF}$ current ratio, ambipolar conduction range, sub-threshold swing and various capacitance to rectify the analog/RF performance of single gate F-shaped TFET. Regarding this, we concurrently optimize the lateral tunneling length between source and gate with optimization of source thickness. The variation in lateral tunneling length, the potential and strength of electric field at fixed $V_{gs}$ voltage is varied which leads to effective change in the ON-current, average sub-threshold swing, and turn ON-voltage. Another side, as well as the source thickness vary, the electric field variation takes place near the edge of source, which leads to variation in the ON-current and ON-voltage. The performance parameters of single gate F- TFET is compared with single gate L-TFET, which is the incentive of this submitted work. The optimized single gate F-TFET have 0.30 V turn ON-voltage with 7.4 mV/decade average sub-threshold swing and high $I_{on}/I_{off}$ ratio approx $10^{13}$. Besides, a significant reduction in parasitic capacitance is beneficial to enhanced RF performance with better controllability on channel.

Keywords Ambipolar conduction · Sub-threshold conduction · Band-to-Band-Tunneling · F-shaped channel · L-shaped channel

1 Introduction
To get the better of MOSFET, Tunnel FET (TFET) has been brought in as an auspicious candidate for a low power application because its sub-threshold swing (SS) can be scaled down than 60 mV/dec [1, 2]. At the initial, the Si-based single gate Tunnel FET experience very low $I_{ON}$ with high ambipolar conduction because of approximately same band-to-band (B2B) tunneling on both drain/channel and source/channel interface [3]. Furthermore, Dual-Gate TFET (DG-TFET) was introduced for better channel controllability to improve the $I_{ON}$ current but again the ambipolar conduction is a major issue [4]. Likewise, various type of techniques and strategies have been proposed to overcome the ambipolar behavior of Tunnel FET device [5–7]. Furthermore, there is some limited research article that has improved $I_{ON}$ and suppressed ambipolar conduction with reduced average sub-threshold swing ($SS_{avg}$) by increasing BTBT region [8, 9]. Some of them, various structure/shape of TFET has been proposed to achieve the improved result in comparison to the previous one [10–12]. As well as the new structure came into existence, some parameter optimization also came into the picture like Threshold voltage ($V_T$), gate-to-drain capacitance ($C_{gd}$), gate-to-source capacitance ($C_{gs}$), cut-off frequency ($f_t$), Gain Bandwidth product (GBP), transit time etc.

For the low power application, we need low $V_{ON}$, which is defined as minimum gate-to-source voltage ($V_{gs}$) at which a transition path has been created between the source and drain region [13]. A novel device structure for low power application named as single gate F-shaped TFET (SG-F-TFET) has been proposed and optimize which consists highly doped source enclosed by a lightly doped silicon
region. With the help of the electric field crowding effect, the SG-F-TFET is supposed to minimize $V_{\text{ON}}$ as the source thickness is decreased [14, 15]. 2D TCAD tool is used to simulate and analyses the analog/RF properties of the SG-F-TFET.

2 Schematic and Specifications of Designed Device

The 2D schematics of DG-TFET, Hetero Material DG-TFET (HMDG-TFET), Single Gate L-shaped TFET (SG-L-TFET), and Single Gate F-shaped TFET (SG-F-TFET) are set out in Fig. 1a-d respectively. Table 1 lists the basic device dimension parameters used for carrying out TCAD simulations. The simulated structures uses physical doping techniques to introduce the dopants in the device. In Fig. 1a, a low-k gate oxide ($SiO_2$) based homo double gate TFET structure is shown which consist Si/Si/Si semiconductor material for source, channel, and drain respectively with $L_S = 55\, \text{nm}$, $L_C = 50\, \text{nm}$, $L_D = 55\, \text{nm}$ and $t_{\text{OX}} = 1\, \text{nm}$. Further, in Fig. 1b, a schematic of high-k gate oxide based hetero double gate TFET shown which consist Si/GaAs/GaAs semiconductor material for source/channel/drain region respectively. The higher bandgap material (GaAs) is used in channel and drain region to eradicate the ambipolar conduction. For further analysis, SG-L-TFET is simulated with source thickness $35\, \text{nm}$ and drain thickness is set to $6\, \text{nm}$ with oxide thickness $1\, \text{nm}$, considering these the ambipolar conduction is suppressed but the turn ON-voltage is quite high (Fig. 1c). So, a new device structure, SG-F-TFET is proposed to decimate the limitation of all previous simulated devices.

A physical doping-based SG-F-TFET is simulated and analyzed for the various device and analog parameters. This simulated structure called “F-shaped” because its channel resembles the finger like source and its 2-D cross sectional view shown in Fig. 1d. Different colors are shown in Fig. 1d define gate oxide, drain, source, channel, and electrodes. SG-F-TFET resembles an ultra-thin highly doped source that is enclosed by lightly doped silicon regions. For analysis and simulations, the doping levels were $1x10^{20}\, \text{cm}^{-3}$, $1x10^{18}\, \text{cm}^{-3}$ and $1x10^{15}\, \text{cm}^{-3}$ for the source, drain, and channel regions respectively with $4.5\, \text{eV}$ gate work function ($W_{FG}$).

The simulation of designed devices is carried out on 2D device simulator TCAD tool [16]. To appropriate internal operation of devices, nonlocal band to band (B2B) tunneling model is used to incorporate the quantum tunneling phenomena at SCIn (source/channel interface)
Table 1 Description of the basic design variables used for the TCAD simulation

| Parameters                          | Abbreviations | DG-TFET | HMDG-TFET | SG-L-TFET | SG-F-TFET |
|-------------------------------------|---------------|---------|-----------|-----------|-----------|
| Gate oxide thickness                | $T_{OX}$      | 1 nm    | 1 nm      | 1 nm      | 1 nm      |
| Gate oxide material (k-value)       | $SiO_2$ (k=3.9) | Hf $O_2$ (k=22) | $SiO_2$ (k=3.9) | $SiO_2$ (k=3.9) |
| Total device length                 | $L_d$         | 160 nm  | 160 nm    | 160 nm    | 160 nm    |
| Thickness above and below source    | $T_2$         | –       | –         | –         | Variable (12.5 nm) |
| Channel thickness at bottom of device | $T_1 = T_D + T_{OX}$ | –       | –         | 7 nm      | 7 nm      |
| Total device thickness              | $T_H$         | 12 nm   | 12 nm     | 42 nm     | 42 nm     |
| Lateral tunneling length            | $L_I$         | –       | –         | 4 nm      | Variable (4 nm) |
| Source thickness                    | $T_S$         | 10 nm   | 10 nm     | 35 nm     | Variable (10 nm) |
| Source length                       | $L_S$         | 55 nm   | 55 nm     | 67 nm     | Variable (67 nm) |
| Gate length                         | $L_G$         | 50 nm   | 50 nm     | 20 nm     | 20 nm     |
| Gate thickness                      | $T_G = 2T_2 + T_S$ | –       | –         | 35 nm     | 35 nm     |
| Channel thickness                   | $2T_2 + T_1 + T_S$ | 10 nm   | 10 nm     | 42 nm     | 42 nm     |
| Channel length (upper)              | $L_{C1}$      | 50 nm   | 50 nm     | 71 nm     | 71 nm     |
| Channel length (bottom)             | $L_C$         | 50 nm   | 50 nm     | 92 nm     | 92 nm     |
| Drain length                        | $L_D$         | 55 nm   | 55 nm     | 68 nm     | 68 nm     |
| Drain thickness                     | $T_D$         | 10 nm   | 10 nm     | 6 nm      | 6 nm      |
| Gate work-function                  | $W_{FG}$      | 4.5 eV  | 4.5 eV    | 4.5 eV    | 4.5 eV    |
| N-type drain doping concentration   | $N_D$         | $10^{18}$ cm$^{-3}$ | $10^{18}$ cm$^{-3}$ | $10^{18}$ cm$^{-3}$ | $10^{18}$ cm$^{-3}$ |
| P-type channel doping concentration | $N_C$         | $10^{15}$ cm$^{-3}$ | $10^{15}$ cm$^{-3}$ | $10^{15}$ cm$^{-3}$ | $10^{15}$ cm$^{-3}$ |
| P-type source doping concentration  | $N_S$         | $10^{20}$ cm$^{-3}$ | $10^{20}$ cm$^{-3}$ | $10^{20}$ cm$^{-3}$ | $10^{20}$ cm$^{-3}$ |

and DCIn (channel/drain interface) by defining quantum tunneling region (qt region) for accurate tunneling process of charge carriers at both interfaces. Excluding this, FERMI and FERMI.NI models are also used to satisfy the Fermi Dirac distribution characteristics. During the simulation, the Shockley-Read-Hall (SRH) recombination, auger, CONMOB, BGN, and FLDMOB models were implemented in addition to the trap assistant tunneling model.

3. Device Analysis Procedure and Analog/RF Parameters

3.1 Device Analysis Procedure

The vertical and lateral device dimension is chosen carefully during simulation process to compare the proposed device performance w.r.t to other simulated devices which were optimized earlier by researchers. In addition with, fine meshing is defined near drain/channel and source/channel interface where B2B tunneling takes place. Mesh size near B2B tunneling interface is set to $1 \times 10^{-4}$ μm and mesh size $= 5 \times 10^{-3}$ μm far of interface. The nonlocal B2B tunneling model was applied with Newton’s numerical method based on iteration (up to 25 iterations) for better convergence of current [4, 17]. Excluding this, to analyze RF functioning, a small signal AC analysis was performed by setting frequency at 1 MHz. The generalized decision making flow chart for device simulation is shown in Fig. 2.

3.2 Details of Device Analog/RF Parameters

This sub-section is considered for a concise front matter about analog/RF performance parameters e.g. Transconductance ($g_m$), $f_1$, GBP, Transconductance Generation Factor (TGF), Transconductance Frequency Product (TFP), Transit time ($\tau$), and parasitic capacitance ($C_{gd}$ and $C_{gs}$) [18].

$$C_{gd} = \frac{\partial Q_s}{\partial V_{gd}}$$ (1)

$$C_{gs} = \frac{\partial Q_s}{\partial V_{gs}}$$ (2)

A mathematical expression of $C_{gd}$ and $C_{gs}$ has given in Eqs. 1 and 2 which play a pivotal role to extract device performance and responsible for parasitic oscillation at various operating frequencies. The first order differentiation of drain current ($I_{ds}$) w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$, convey in Eq. 3. The value of $g_m$ w.r.t. $V_{gs}$ is known as $g_m$. Faster switching response of device [19].

$$g_m = \frac{\partial I_d}{\partial V_{gs}}$$ (3)
Another important device parameter is $f_t$, it is the max. frequency at which a given device works properly without any performance debasement. $f_t$ is also interpreted as an operating frequency at which short circuit gain becomes equal to unity. To analyses, the $f_t$ parameter of device w.r.t to parasitic capacitances, the relation between both is given in Eq. 4.

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$  \hspace{1cm} (4)

The mathematical expression for GBP is given by Eq. 5. As per equation, it is directly in proportion to $g_m$ value and inversely proportional to $C_{gd}$ value of the device [20, 21]. A high value of GBP is required for superior high frequency performance.

$$GBP = \frac{g_m}{2\pi C_{gd}}$$  \hspace{1cm} (5)

TGF and TFP are substantial parameters to account for device efficiency and the trade-off between power dissipation and operating bandwidth respectively. Both device parameter values should be high for low power circuit operation with high speed. The mathematical equations of TGF and TFP are given by Eqs. 6 and 7 respectively [5, 22, 23].

$$TGF = \frac{g_m}{I_d}$$  \hspace{1cm} (6)

$$TFP = \frac{g_m f_t}{I_d}$$  \hspace{1cm} (7)

Another crucial operational factor for RF analysis is transit time which is defined as the time requires to charge carriers to be shifted from source to channel, given by Eq. 8. According to this mathematical equation, transit time is inversely proportional to $f_t$. If the $f_t$ value increases the transition time decreases [24].

$$\tau = \frac{1}{2\pi f_t}$$  \hspace{1cm} (8)

4 Simulation Results and Observations

4.1 Performance Analysis of Devices

This section edifies the impact of the shape of source and channel regions on the performance of physically doped TFET. For this, the effect can be observed on alignment of energy bands and strength of electric field. At room temperature (T = 300 K), energy band alignment at source/channel interface (SCIn) is approximately close for all simulated device structures for OFF-state condition because weak electric field is present without $V_{gs}$ application (Fig. 3a). On the other hand, at T = 300 K, $V_{gs} > 0V$ is applied (ON-state condition), the source’s VB (Valence band) and channel’s CB (Conduction band) get aligned. From Fig. 3b, band alignment for DG-TFET and HMDG-TFET is close enough. Similarly for the SG-L-TFET and proposed device. Along with, a relative electron and hole concentration of all devices are shown in Fig. 4a at same doping levels. The electric field strength at SCIn is different for all devices because of the change in shape of source and the use of hetero material (Fig. 4b). The electric field strength for proposed device is significantly large compared to other simulated devices. This effect is reflected in terms of high ON-current with low $V_{ON}$ for the SG-F-TFET, as shown in Fig. 5.

4.2 Analog and High Frequency Performance with Parametric Variation

4.2.1 Impact of Lateral Tunneling Length ($L_T$)

The initially designed SG-F-TFET was simulated by varied the $L_T$ from 10 nm to 2 nm, to analyze the impact on $I_{ON}/I_{OFF}$ ratio, ambipolar current ($I_{amb}$), $V_{ON}$ voltage and analog/RF parameters. Figure 6a shows the EBD for different $L_T$ along the channel direction at thermal equilibrium condition. In this Fig. 6a, the steepness of tunneling junction in not significantly affected by $L_T$ variation but at other hand the electric field strength at SCIn diminished as well as $L_T$ value is increases. Due to
Fig. 3 Analysis of EBD (Energy band-diagrams) (a) OFF-state, $V_{ds} = 0.7$ V with $V_{gs} = 0.0$ V and (b) ON-state, $V_{ds} = 0.7$ V with $V_{gs} = 1.5$ V at SCIn for the schematic mention in Fig. 1

Fig. 4 Device schematic corresponds to Fig. 1 (a) Comparison of charge carrier concentration and (b) Electric field at SCIn and room temperature

Fig. 5 Comparison of simulated SG-F-TFET transfer characteristics with DG-TFET, HMDG-TFET, and SG-L-TFET, all the devices have $T_{ox} = 1$ nm $L_{tt} = 120$ nm
increment in $L_T$ value the surface potential at fixed gate to source voltage is decrease which impact shown in term of reduced electric field (up to $2.3 \times 10^6$ V/cm) (Fig. 6b). This can effect the $I_{ON}$ range because a high electric field helps to achieve better B2B tunneling rate [25, 26]. In this concern, a comparison between $I_{ds} - V_{gs}$ characteristics for different values of $L_T$ is presented in Fig. 7. For significant observation related to ON-current variation, $I_{ds} - V_{gs}$ curve is plotted on linear axis (Fig. 7, Y-axis, Right-hand). Along with, $I_{ds} - V_{gs}$ curve also plotted on log scale (Fig. 7, Y-axis, Left-hand) for extraction of $SS_{avg}$ and $V_{ON}$ of proposed device.

The $I_{ds} - V_{gs}$ curve of proposed device is shifted towards the lower $V_{gs}$ value on X-axis, which indicates that $V_{ON}$ is reduced with miniaturization in lateral tunneling length because of potential value at fixed $V_{gs}$ is reduced [27, 28]. Along with, the steepness of $I_{ds} - V_{gs}$ curve also improved as $L_T$ reduces, it is imputed to the smaller tunneling width at 2 nm and 4 nm $L_T$. Likewise, $I_{ON}$ increases as $L_T$ decreases (Fig. 7), because of decreased tunneling width for ON-state condition. The $I_{ambi}$ of proposed device is not much affected by the $L_T$ because ambipolar behavior of TFET mainly depends on the drain/channel interface (DCIn) [29] and $L_T$ does not affect this interface in this proposed work.

The gate-gate capacitance is mainly composed of two capacitances $C_{gd}$ and $C_{gs}$, shown in Fig. 8 [24]. A significant reduction in capacitances is reflected with decrease $L_T$ because of high tunneling effect which reduces the carrier accumulation rate. The $C_{gd}$ is a dominant capacitance due to the accumulation of the electron of channel-source and collected by the drain region [30, 31]. The finger like source helps to reduce the capacitances by reducing the accumulation of opposite type charge carrier near channel-source and channel-drain interfaces. The reduced value of $C_{gd}$ helps to attain superior gate controllability over the channel region. The $C_{gd}$ value of SG-F-TFET is reduced up to 0.5 fF at $L_T = 2$ nm and 4 nm because of reduced drain-channel interface (6 nm), as shown in Fig. 8a. As shown in Fig. 8b, the reduced value of $L_T$ reflected in terms of decreased $C_{gs}$ because of high tunneling at SCIn. In addition to $C_{gd}$ and $C_{gs}$ are also a parameter of interest for high-frequency introspection of device operations.

From Fig. 9a, the SG-F-TFET achieves a higher transconductance ($g_m$) value at the higher $V_{gs}$ for $L_T = 2$ nm and 4 nm due to high steepness of $I_{ds} - V_{gs}$ curve, whereas $g_m$ starts decreasing after achieving the peak because of less variation in $I_{ds}$ w.r.t $V_{gs}$ as mention in Eq. 3. The high frequency performance of the proposed device was analyzed by $f_t$ and GBP [32]. The $f_t$ can be evaluated by the ratio of $g_m$ to $C_{gg}$ ($C_{gd} + C_{gs}$) as mention in Eq. 4. A higher range of $f_t$ is achieved for $L_T = 2$ nm and 4 nm at higher value of $V_{gs}$ due to high $g_m$ at higher $V_{gs}$ and reduced total capacitance ($C_{gg}$) in comparison to other high values of $L_T$, mention in Fig. 9b. After attaining its maximum value, $f_t$ graph starts decreasing because of the higher value of $C_{gd}$ for $V_{gs} > 1.25$ V [27, 33, 34]. Along with, GBP is higher.
for the $L_T = 2$ nm and 4 nm by the effect of lower $C_{gd}$ (Fig. 8a) value as shown in Fig. 10a.

Another remarkable RF analysis performance parameter is transit time, which is inversely proportional to $f_t$ value. The transit time is decreased when $f_t$ increases. For a lower value of transit time, speed of the device is improved [2]. From Fig. 10b, it can be analyzed that, transit time is very less for $L_T = 2$ nm for lower $V_{gs}$. But for the higher $V_{gs}$ value, it is similar for all $L_T$ variations.

The TFP and TGF curve with $L_T$ variation is shown in Fig. 11. For $L_T = 2$ nm and 4 nm we get very high TFP, which helps to enhance the device speed with low power consumption [35]. Figure 11b communicate the TGF variation for all $L_T$ value. For 2 nm and 4 nm of $L_T$, TGF is maximum in sub-threshold region for $V_{gs} > 0.8$ V. So proposed device with $L_T = 2$ nm or 4 nm can be used effectively for switching applications. Considering the above analysis based on $L_T$ variation, the optimum $L_T$ is set to either 2 nm or 4 nm, since the increase in $I_{ON}$, $V_{ON}$, $SS_{avg}$ with improved analog/RF parameter. To select the optimum value of $L_T = 2$ nm or 4 nm. We have performed further analysis on the source thickness by setting $L_T = 2$ nm and 4 nm.

**4.2.2 Impact of Source Thickness ($T_S$) at 2 nm $L_T$**

In the previous section, we analyzed the effect of lateral tunneling length on SG-F-TFET. We will examine the impact of source thickness on the proposed device performance by considering two cases:

I. Source Thickness ($T_S$) at 2 nm $L_T$
II. Source Thickness ($T_S$) at 4 nm $L_T$

In this section, the consequences of $T_S$ variation on analog/RF parameters are analyzed at $L_T = 2$ nm. Figure 12 shows the $I_{ds} - V_{gs}$ curve depending on $T_S$ and $L_T$ set to 2 nm. From this graph, we can see that, as $T_S$ is increasing, the $I_{ON}$ is decreasing with a very small variation in $I_{ambi}$ and $V_{ON}$. The $I_{ON}$ decreases because of electric field crowding effect at the edges of the source regions decreases as well as the $T_S$ increases i.e., the electric field at SCIn is the sum of two component, field at corner of source region ($E_C$) and the flat region of source ($E_F$). As the $T_S$ increases, the effect of $E_C$ field component is minimized, so a significant reduction can be seen in the $I_{ds}$ value, as mention in Fig. 12.

Figure 13 shows the capacitances for various $T_S$ values. The $C_{gd}$ curve is increasing from low to high $V_{gs}$ (0 -
Fig. 10 Data plot of (a) GBP and (b) Transit time ($\tau$) for different $L_T$ values at $T_S = 10$ nm for proposed device.

Fig. 11 (a) TFP and (b) TGF data plot for different $L_T$ values at $T_S = 10$ nm for proposed device.

Fig. 12 Simulated SG-F-TFET transfer characteristics for different $T_S$ values at $L_T = 2$ nm. Inset: a zoomed graph of $I_{ds}$ vs $V_{gs}$ curve for clear verification of impact of $T_S$ at fixed $L_T$. 
1.5 V). As the TS increases, the accumulation of electron carriers is increased at SCIn which are collected by the drain region. So, the Cgd increases as source thickness increases, as revealing in Fig. 13a. Apart from this, the same effect is reflected in the Cgs capacitance data plot as shown in Fig. 13b.

The gm value of a device depends on the change in Ids w.r.t Vgs. The change in Ids is higher for lower gate voltage, for the decreasing value of TS. Hence, the improved gm achieved at 3 nm source thickness, shown in Fig. 14a. The high frequency performance is investigated by using two important parameters ft and GBP. The higher ft archives at 3 nm source thickness due to the high gm at higher Vgs as well as the reduced value of Cgs (Fig. 14b). The GBP is also high, when TS is set to 3 nm by the effect of reduced Cgd for TS = 3 nm, mention in Fig. 15a.

The transit time is used to verify the device speed and it is inversely related to ft. From Fig. 15b, transit time reduces as well as TS is minimized. When TS is set to 3 nm, we obtain lowest transit time due to high ft, as mention in Fig. 14b. For TS variation, TFP and TGF curves are shown in Figs. 16a and b respectively. Both the parameter directly proportional to gm. Hence, both the parameters obtain a high value at 3 nm TS.

### 4.2.3 Impact of Source Thickness (TS) at 4 nm LT

In this section, the consequence of TS variation on different device parameters is analyzed when LT is set to 4 nm. In the previous section, we had analyzed the impact of source thickness variation w.r.t 2 nm LT, but in this case, LT is set to 4 nm due to this the tunneling width at SCIn is increased. This effect reflects in terms of increased or decreased device parameters values. From Fig. 17, for Ion, Von, and steepness of Ids − Vgs curve at 3 nm TS, the considerable deviation can be observed. Along with, for 5 nm to 20 nm of TS, Ion is decreased compared to 2 nm LT, as described earlier in Fig. 12. As the tunneling width increase, the dominating capacitances like Cgd and Cgs also deliberate. When TS and LT are set to 3 nm and 4 nm respectively, the lowest Cgd obtain and it will increase for high TS value (Fig. 18a). Similarly, the Cgs is decreased as the TS reduced w.r.t Vgs, as depicted in Fig. 18b.

Another critical device performance parameter is gm, which represents the amplification quality of the device. The gm is initially increased and strikes the maximum value and then starts decreasing because, at higher Vgs, Cgd is dominating parameter, as shown in Fig. 19a. The increased tunneling width does not produce any significant effect on

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**Fig. 13** Analysis of (a) Cgd and (b) Cgs for TS = 3 nm to 20 nm at LT = 2 nm for proposed device

**Fig. 14** Analysis of (a) gm and (b) f for TS = 3 nm to 20 nm at LT = 2 nm

**Fig. 15** Analysis of (a) gm and (b) f for TS = 3 nm to 20 nm at LT = 2 nm

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This section provides a detailed analysis of the impact of source thickness on various parameters of a device under different gate and tunneling widths. The variations in capacitance, transconductance, high frequency performance, and device speed are discussed in detail. The results highlight the importance of optimizing the source thickness for improved device performance.
Fig. 15  Analysis of (a) GBP and (b) Transit time for $T_S = 3$ nm to 20 nm at $L_T = 2$ nm

Fig. 16  (a) TFP and (b) TGF curve for $T_S = 3$ nm to 20 nm at $L_T = 2$ nm for proposed device

Fig. 17  Comparison of $I_{ds}$ w.r.t $V_{gs}$ for different $T_S$ values at $L_T = 4$ nm
$g_m$ value. For frequency analysis, $f_t$ and GBP are crucial parameters. From Fig. 19b, $f_t$ values increase at high $V_{gs}$ for various $T_S$, and it attains peak value at lower $V_{gs}$ because $g_m$ is dominating parameter. But, after attaining the peak value, it starts decreasing due to the high value of ($C_{gd} + C_{gs}$).

Figure 20a shows GBP versus $V_{gs}$ graph for different $T_S$. The simulation results indicate increased GBP with increased $V_{gs}$ and the peak point is shifted towards lower gate voltage as $T_S$ decreases. At $L_T = 4$ nm, the device transit delay is increased for low gate voltage compared to $L_T = 2$ nm for $T_S$ variation, as display in Fig. 20b.

TFP determines the device performance at the operating frequency. It shows the relationship between power and bandwidth for high speed device applications. Ultra thin source (3nm) produces high TFP (Fig. 21a) when $L_T$ is set to 4 nm. Further, to examine the device’s ability to convert power into speed, we can evaluate the TGF parameter. The higher value of TGF rewired for high speed of the device. Hence the appropriate TGF value is selected at 3nm source thickness, as shown in Fig. 21b.

To clarify and to select the optimized value of $L_T$ (2 nm or 4 nm) with optimized source thickness, a comparative analysis is performed w.r.t $SS_{avg}$ and $V_{ON}$ at different $T_S$ values. The lowest value of $V_{ON}$ is achieved at $T_S = 3$ nm and $L_T = 4$ nm, but as well as the $T_S$ increases the $V_{ON}$ is higher for 4 nm $L_T$ as compared to 2 nm of $L_T$, mention in Fig. 22a. Same way, the $SS_{avg}$ of the device examines at different $T_S$ when $L_T$ set to 2 nm and 4 nm. From Fig. 22b, we can see that $SS_{avg}$ is minimum for $T_S = 3$ nm and $L_T = 4$ nm. But, the $SS_{avg}$ for higher source thickness is high for $L_T = 4$ nm.

### 4.3 Optimization of Device Lateral Length

For future aspect, it is influential to analyze the scaling perceptiveness of SG-F-TFET. The channel length ($L_C$ and $L_{C1}$) is already selected very carefully to get superior performance of proposed device, but the drain and source lateral length is consider w.r.t. comparative analysis. So, the down scaling is performed on $L_S$ and $L_D$ to optimize the total device length without affecting its performance.

#### 4.3.1 Down Scaling of Source Lateral Length ($L_S$)

In this sub-section, we will figure out the optimal value of the $L_S$ such that the characteristics of the device are not severely affected. Figure 23a and b shows the electric field...
Fig. 20  Analysis data plot of (a) GBP and (b) Transit time for \( T_S = 3 \text{ nm to 20 nm} \) at fixed \( L_T = 4 \text{ nm} \)

![Graph](image1)

Fig. 21  (a) TFP and (b) TGF analysis curve for different values of \( T_S \) when \( L_T \) set to 4 nm for proposed device

![Graph](image2)

Fig. 22  A grouped bar diagram of (a) \( V_{ON} \) and (b) \( SS_{avg} \) at \( L_T = 2 \text{ nm} \) and \( L_T = 4 \text{ nm} \) w.r.t source thickness variation from 3 nm to 20 nm

![Graph](image3)
Fig. 23  Source length optimization of SG-F-TFET (a) Electric field strength analysis curve (at SCIn) and (b) $I_{ds}$ w.r.t $V_{gs}$ at fixed $L_T = 4$ nm, $T_S = 3$ nm, $L_D = 68$ nm, and $SiO_2$ selected as gate oxide. Inset: an enlarged $I_{ds} - V_{gs}$ graph to improve the visibility for better analysis.

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Fig. 24  (a) $C_{gd}$ and (b) $C_{gs}$ curves at various $L_S$ to optimize the proposed device lateral length. Inset: an magnified $C_{gd} - V_{gs}$ and $C_{gs} - V_{gs}$ graph to improve the visibility for better analysis.

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Fig. 25  Drain length optimization of SG-F-TFET (a) Electric field strength analysis curve (at DClx) w.r.t x-axis position and (b) $I_{ds}$ w.r.t $V_{gs}$ at fixed $L_T = 4$ nm, $T_S = 3$ nm, $L_D = 40$ nm, and $SiO_2$ selected as gate oxide. Inset: an enlarged $I_{ds} - V_{gs}$ graph to improve the visibility for better analysis.
strength at SCIn and $I_{ds} - V_{gs}$ curve of the SG-F-TFET w.r.t. changes in the $L_S$ from 60 nm to 35 nm. Figure 22a shows that as the $L_S$ decreased up to 40 nm, there is no effect on the electric field strength. However, as $L_S$ is decreased below 40 nm, the electric field start decreasing. Because of this decrement in electric field the $I_{ON}$ current of the device also start decreasing with increased $V_{ON}$, as shown in Fig. 23b. The impact of down-scaling of source lateral length also analyzed on the capacitances like $C_{gd}$ and $C_{gs}$. From Fig. 24a and b, we can see that for $L_S$ lower than 40 nm the capacitances are increased because of the very high accumulation of carrier near the SCIn with application of the high gate voltage. So, considering the above observation related to source lateral length optimization, we conclude that $L_S = 40$ nm is needed for the optimal performance of SG-F-TFET (proposed device).

### 4.3.2 Down Scaling of Drain Lateral Length ($L_D$)

In this sub-section, we will find out minimum value of $L_D$ such that the device characteristics are un influenced significantly. Initially, the drain lateral length set to 58 nm in proposed device. Figure 25a shows the electric field variation at DCIn of proposed device, it is remain unchanged until $L_D$ value goes below 38 nm. For 38 nm $L_D$, change in electric field strength not significant. On the other hand, the $I_{ON}$ is not significantly change from 58 nm to 38 nm of $L_D$. But,lower than 38 nm, i.e., for $L_D = 35$ nm, the $V_{ON}$ and $I_{ON}$ decreased which are considerable change to degrade the device performance (Fig. 25b).

To examine the effect of down-scaling of $L_D$ on device performance with respect to capacitances of device, we also analyze the $C_{gd}$ and $C_{gs}$ for different range of $L_D$. The $C_{gd}$ remain unchanged up to $L_D = 38$ nm, after this its value suddenly become very high (Fig. 26a) because the carrier collected from the channel become very high near the DCIn region which are responsible for the gate to drain capacitances. But, the opposite effect can be seen for $C_{gs}$, it is remain unchanged until $L_D$ scaled down to 38 nm and after this its value sudden fallen down in the range of 0.19 fF. The down scaling of $L_D$ shows opposite impact on the $C_{gd}$ and $C_{gs}$. As we know, the impact of $C_{gd}$ is more dominant than $C_{gs}$ on device performance. Hence, the optimum value of $L_D$ is determined as 38 nm.

### 5 Optimized SG-F-TFET

In Section 4.2, we have optimize the parameters ($L_T$, $T_S$), which can affect the electric field crowding effect (Electric field strength at edges of source region). Along with, in Section 4.3 lateral length optimization have been performed and $L_S$ and $L_D$ are optimized. SG-F-TFET can achieve the higher drain current ($A/\mu m$) and improved analog/RF parameters as source thickness ($T_S$) and lateral tunneling length ($L_T$) decreases, as mention in figures which are listed in Section 4.2 and 4.3. The optimized SG-F-TFET consists, $L_T = 4$ nm, $T_S = 3$ nm, $L_D = 38$ nm, $L_S = 40$ nm and $T_{OX}$ set to 1 nm, SiO$_2$ as gate oxide material. The $WF_G$ set to 4.5 eV and $N_S$, $N_C$ and $N_D$ is $10^{20}$ cm$^{-3}$, $10^{15}$ cm$^{-3}$ and $10^{18}$ cm$^{-3}$ respectively. Considering the above optimum parameters related to dimensions, final $L_{HI}$ of device is 103 nm with $T_{HI} = 42$ nm. The analog/RF parameters of optimized SG-F-TFET are listed in Table 2.

#### Table 2 Optimized analog/RF parameters of proposed device (SG-F-TFET)

| Parameters | $I_{ds}(A/\mu m)$ | $g_m(\mu S)$ | $C_{gd}(fF)$ | $C_{gs}(fF)$ | $f_t$(GHz) | GBP(GHz) | TGF(MV$^{-1}$) | TFP(GHz/V) | Transit time($\mu s$) |
|------------|------------------|-------------|-------------|-------------|------------|----------|-------------|------------|-----------------|
| SG-F-TFET  | $4.36 \times 10^{-4}$ | 825         | 0.31        | 0.24        | 370        | 176      | 0.684       | 0.36       | 215             |

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6 Conclusion

A new SG-F-TFET is designed and its fundamental physics of devices and working principle are investigated in detail using the 2D TCAD simulator. The proposed modification in SG-F-TFET improves ON-state current and reduced $V_{ON}$ with increased $SS_{avg}$ (below 9 mV/decade), ambipolar current suppress drastically (10$^{-1}$ order) correspond to the DG-TFET. The results confirm that SG-F-TFET can achieve a relatively lower $V_{ON}$ (approximately 0.3 V) with $LT = 4$ nm and $TS = 3$ nm. Along with these advantages, proposed device also consist low $C_{gd}$ and $C_{gs}$ which are causative for improved device controllability. We have also demonstrated that SG-F-TFET device is exempt to reduction in $LS$ and $LD$ up to 40 nm and 38 nm respectively.

For analog/RF parameters such as $C_{gs}$, $C_{gd}$, $g_m$, $f_t$, GBP, TFP, TGF and transit time are analyzed to determination the feasibility of the SG-F-TFET for high frequency application with low power operation. It was found that when the $LT$, $TS$, $LS$ and $LD$ set to 4 nm, 3 nm, 40 nm and 38 nm respectively, SG-F-TFET shows the better performance for high frequency parameters. At the last, SG-F-TFET is expected to be fabricated by self-aligned processes. So, optimized SG-F-TFET can be utilized as promising alternative for low power high frequency applications.

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Author Contributions

- Prabhat Singh: Conceptualization, data curation, formal analysis, methodology, investigation, writing – original draft.
- Dharmendra Singh Yadav: Supervision, validation, visualization, writing – review & editing.

Data Availability The data and material concerned to the manuscript may be made available on request.

Declarations

- The manuscript follows all the ethical standards, including plagiarism.
- Consent to participate Yes.
- Consent for Publication Yes.
- Conflict of Interests No conflicts of interest.

References

1. Avci UE, Morris DH, Young IA (2015) Tunnel field-effect transistors prospects and challenges. IEEE J Electron Devices Soc 3(3):88–95
2. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy-efficient electronic switches. Nature 479(7373):329–337
3. Boucart K, Ionescu AM (2007) Double-gate tunnel fet with high-k gate dielectric. IEEE Trans Electron Devices 54(7):1725–1733
4. Toh E-H, Wang GH, Chan L, Samudra G, Yeo Y-C, physics Device (2007) guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction. Appl Phys Lett 91(24):243505
5. Raad BR, Sharma D, Kondekar P, Nigam K, Yadav DS (2016) Drain work function engineered doping-less charge plasma tfet for ambipolar suppression and rf performance improvement: a proposal, design, and investigation. IEEE Trans Electron Devices 63(10):3950–3957
6. Mallik A, Chattopadhyay A, Guin S, Karmakar A (2013) Impact of a spacer–drain overlap on the characteristics of a silicon tunnel field-effect transistor based on vertical tunneling. IEEE Trans Electron Devices 3(60):935–943
7. Yadav DS, Sharma D, Raad BR, Bajaj V (2016) Dual workfunction hetero gate dielectric tunnel field-effect transistor performance analysis. In: 2016 International conference on advanced communication control and computing technologies (ICACCTR), IEEE, pp 26–29
8. Villalon A, Le Carval G, Martinie S, Le Royer C, Jaud M-A, Cristoloveanu S (2014) Further insights in tfet operation. IEEE Trans Electron Devices 61(8):2893–2898
9. Garg S, Saurabh S (2020) Exploiting within-channel tunneling in a nanoscale tunnel field-effect transistor. IEEE Open J Nanotechnol 1:100–108
10. Abdi DB, Kumar MJ (2014) In-built n+ pocket npn tunnel field-effect transistor. IEEE Electron Device Letters 35(12):1170–1172
11. Tirkey S, Raad BR, Gedam A, Sharma D (2018) Junction-less charge plasma tfet with dual drain work functionality for suppressing ambipolar nature and improving radio-frequency performance. Micro Nano Lett 13(1):18–23
12. Sao W, Yao C, Jiao G, Huang D, Yu H, Li M-F (2011) Improvement in reliability of tunneling field-effect transistor with pnn structure. IEEE Trans Electron Devices 58(7):2122–2126
13. Naran R, Saxena M, Gupta R, Gupta M (2012) Assessment of ambipolar behavior of a tunnel fet and influence of structural modifications. JSTJS: J Semicond Technol Sci 12(4):482–491
14. Yun S, Oh J, Kang S, Kim Y, Kim JH, Kim G, Kim S (2019) F-shaped tunnel field-effect transistor (tfet) for the low-power application. Micromachines 10(11):760
15. Fossum J, Yang J-W, Trivedi V (2003) Suppression of corner effects in triple-gate mosfets. IEEE Electron Device Lett 24(12):745–747
16. Manual AU (2016) Silvaco international inc, Santa Clara, CA USA
17. Tirkey S, Sharma D, Raad BR, Yadav DS (2017) A novel approach to improve the performance of charge plasma tunnel field-effect transistor. IEEE Trans Electron Devices 65(1):282–289
18. Imenabadi RM, Saremi M, Vandenberghe WG (2017) A novel npnn-like z-shaped tunnel field-effect transistor with improved ambipolar behavior and rf performance. IEEE Trans Electron Devices 64(11):4752–4758
19. Tirkey S, Yadav DS, Sharma D (2017) Controlling ambipolar behavior and improving radio frequency performance of hetero junction double gate tfet by dual work-function, hetero gate dielectric, gate underlap: Assessment and optimization. In: 2017 International conference on information, communication, instrumentation and control (ICICIC), IEEE, pp 1–7
20. Deb Nath RG, Baruah K, Baishya S (2020) Dc and analog/rf performance analysis of gate extended u-shaped channel tunnel field effect transistor. Microsys Tech 26(9):2793–2799
21. Pandey C, Dash D, Chaudhury S (2020) Improvement in analog/rf performances of soi tfet using dielectric pocket. Int J Electron 107(11):1844–1860

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22. Yadav DS, Sharma D, Raad BR, Bajaj V (2016) Impactful study of dual work function, underlap and hetero gate dielectric on tfet with different drain doping profile for high frequency performance estimation and optimization. Superlattices Microstruct 96:36–46
23. Shekhar D, Raman A (2020) Design and analysis of dual-gate misalignment on the performance of dopingless tunnel field effect transistor. Appl Phys A 126:1–9
24. Guenifi N, Rahi S, Larbi M (2020) Suppression of ambipolar current and analysis of rf performance in double gate tunneling field effect transistors for low-power applications. Int J Nanoparticles Nanotech 6:033
25. Yadav DS, Raad BR, Sharma D (2016) A novel gate and drain engineered charge plasma tunnel field-effect transistor for low sub-threshold swing and ambipolar nature. Superlattices Microstruct 100:266–273
26. Abraham N, James RK (2020) An improved tunnel field-effect transistor with an l-shaped gate and channel. J Comput Electron 19(1):304–309
27. Saurabh S, Kumar MJ (2010) Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. IEEE Trans Electron Devices 58(2):404–410
28. Shekhar D, Raman A (2021) Tweaking the performance of dopingless nano-tfet with misaligned sandwiched dual-gate structure. Silicon 1–11
29. Joshi T, Singh B, Singh Y (2020) Controlling the ambipolar current in ultrathin soi tunnel fets using the back-bias effect. J Comput Electron 19(2):658–667
30. Kim SW, Kim JH, Liu T-JK, Choi WY, Park B-G (2015) Demonstration of l-shaped tunnel field-effect transistors. IEEE Trans Electron Devices 63(4):1774–1778
31. Kao K-H, Verhulst AS, Vandenberghen WG, Soree B, Magnus W, Leonelli D, Groeseneken G, De Meyer K (2012) Optimization of gate-on-source-only tunnel fets with counter-doped pockets. IEEE Trans Electron Devices 59(8):2070–2077
32. Anghel C, Chilagani P, Amara A, Vladimirescu A (2010) Tunnel field effect transistor with increased on current, low-k spacer and high-k dielectric. Appl Phys Lett 96(12):122104
33. Saurabh S, Kumar MJ (2016) Fundamentals of tunnel field-effect transistors. CRC press
34. Yang Z (2016) Tunnel field-effect transistor with an l-shaped gate. IEEE Electron Device Lett 37(7):839–842
35. Zhu Y, Hudait MK (2013) Low-power tunnel field effect transistors using mixed as and sb based heterostructures. Nanotechnol Rev 2(6):637–678

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