A simple proof of three properties on Simpson’s 4-slot Algorithm

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Abstract

In this paper we present an invariance proof of three properties on Simpson’s 4-slot algorithm, i.e. data-race freedom, data coherence and data freshness, which together implies linearisability of the algorithm. It is an extension of previous works whose proof focuses mostly on data-race freedom. In addition, our proof uses simply inductive invariants and transition invariants \[^6\] whereas previous work uses more sophisticated machinery like separation logics, rely-guarantee or ownership transfer.

Keywords: Wait-free algorithm, Linearisability, Inductive invariant, Transition invariant, Correctness proof, Formal verification

1. Introduction

In this paper we are going to give a new proof of properties on Simpson’s four-slot algorithm \[^8\]. The proof consists of two parts: one for the property of data-race freedom and the other for the properties of data coherence and data freshness \[^2\]. In conjunction, they implies the linearisability \[^3\] of the Simpson’s asynchronous communication mechanism between a reader and a writer \[^3\]; that is, behaviourally and abstractly the mechanism acts as if it is a single atomic register (with linearisability semantics) shared between the two parties. The work is inspired by and builds on previous works tackling the same problem by others using a variety of different techniques \[^2\] \[^1\] \[^4\] \[^9\].

In a nutshell, data-race freedom means that concurrent read and write operations on the set of (non-atomic) data variables of asynchronous communication mechanism will not race on any member of the set; race on a data variable means there is a state on which there exists two threads accessing the same variables simultaneously and incomaptably (e.g. read-write or write-write). The data variables in question consists of a 2x2
array of buffer variables with non-atomic semantics (i.e., the four slots) allocated for storing the contents of the communication. It is due to the wait-freedom requirement of the algorithm that four copies (of the slot variables) are used in order to implement one copy of the abstract shared register. They are in contrast to the remaining variables of the algorithm which are the (atomic) control ones being put in place to coordinate and synchronize concurrent accesses to data variables for the sake of data-race avoidance.

Data freshness, on the other hand, means that if the duration of a write operation $A$ (also called the round of $A$ operation in the sequel) precedes the duration of a read operation $B$, then the contents read by $B$ should be at least as fresh as that written by $A$. Note that the data freshness of all the write operations are linearly ordered in the case of the four slot algorithm since it has only one writer; and similarly all the read operations are linearly ordered due to its use of only one reader.

Finally, data coherence means that the order of data writings by the writer should be consistent with the order of data viewing (i.e., readings) by the reader. That is, given a pair of read operations $R_1$ and $R_2$ reading from the write operations $W_1$ and $W_2$ resp., if $R_1$ is (linearly) ordered before $R_2$, then $W_2$ cannot be possibly (linearly) ordered before $W_1$.

2. Simpson’s 4-slot Algorithm

Now we borrow some exposition from [9] to explain the Simpson’s four-slot algorithm.

Simpson’s algorithm [8], as shown in Figure 1, uses four control bits and two pairs of slots as shared variables to achieve asynchronous communication between two threads. In addition to the shared variables, the two threads also use two pairs of local variables, e.g., the pair $wp$ and $wi$ for the writer.

The reader thread is an (imaginary) loop that repeatedly calls procedure $\text{read()}$ while the writer thread repeatedly calls procedure $\text{write}(w)$. Commands of the form $c$ in the code of $\text{read()}$ and $\text{write}(w)$ are atomic commands in which $c$ will be executed in one indivisible step. The four control bits are assumed to be atomic registers; thus statements like writing and reading of control bits are atomic commands. The two pairs of slots are assumed to be non-atomic registers, and their assignment and reading are not atomic command.

The cleverness of Simpson’s algorithm lies in that the reader and writer can coordinate, via the four atomic control bits, to channel simultaneous requests on the slots to different copies. Thus the accesses to one slot will look as if serial and non-atomic registers will suffice to implement the slots.

In $\text{write}(w)$ the local variables $wp$ and $wi$ act as pointers pointing to resp. a pair and a slot in the pair. Collectively they identify the slot the writer is going to write to. The values of these pointers depends on the values of control bits $r$ and $li$. $r$ is a pointer used by the reader to publish the pair it is going to read from, while $li$ are two pointers pointing to resp. the slots holding the freshest value in each pair. The strategy of the writer, upon each invocation of $\text{write}(w)$, is to move away from the pair the reader is working on and select the slot not holding the freshest value to write to. After writing to the slot, the writer updates the relevant pointer in $li$ (to point to the new freshest) and publish its latest location (i.e., the pair it just worked on) in $l$. 

2
shared d[2][2] = ((v_{0,0}, v_{0,1}), (v_{1,0}, v_{1,1})), \begin{align*} \textit{li}[2] &= (0, 0), \textit{l} = 1, \textit{r} = 0 \end{align*}

local \; \textit{wp} = 1, \; \textit{wi} = 0; \quad \text{local} \; \textit{rp} = 0, \; \textit{ri} = 0, \; y = \bot;
\begin{align*}
\text{write}(w) &= \begin{cases} a - 2: & \textit{wp} := 1 - \textit{r}; \\
a - 1: & \textit{wi} := 1 - \textit{li}[\textit{wp}]; \\
a: & d[\textit{wp}][\textit{wi}] := w; \\
a + 1: & \textit{li}[\textit{wp}] := \textit{wi}; \\
a + 2: & \textit{l} := \textit{wp}; \\
\end{cases} \\
\text{read()} &= \begin{cases} b - 3: & \textit{rp} := l; \\
b - 2: & \textit{r} := \textit{rp}; \\
b - 1: & \textit{ri} := \textit{li}[\textit{rp}]; \\
b: & y := d[\textit{rp}][\textit{ri}]; \\
b + 1: & \text{return } y; \\
\end{cases}
\end{align*}

Figure 1: The four-slot algorithm

Similarly, in \textit{read()} \textit{rp} and \textit{ri} point to the slot the reader is going to read from. The strategy of the reader is to track the latest location of the writer (by reading \textit{l}) and read the freshest value in the location (as pointed to by \textit{li}). However, notice that the reader updates \textit{r} before the read starts, while the writer updates \textit{l} and \textit{li} after the write is finished. The order in which the control variables are updated in each thread is very crucial for achieving asynchronous communication.

Data-race freedom is mainly achieved in the writer’s strategy, data freshness is mainly achieved in the reader’s strategy; and data coherence is achieved by the collaboration of the two.

**Semantics of non-atomic variable access.** In this paper, instead of using a non-atomic semantic model that interprets the execution of a non-atomic action as an interval (e.g. a pair of transitions), we will use atomic interleaving model to give semantics to the four-slot algorithm, where we assume all action (i.e. command) executions are atomic. The rationale here is that the latter is faithful to the former on all execution sequences up to the first non-atomic data access.

If furthermore the data-race freedom can be proved in the atomic model of the four-slot algorithm, we can show the two models coincide. Our argument is as follows.

We say a state \( s \) is as-if atomic if for all data variables there is at most one thread in that state that is accessing the data variable. Then, for all execution sequences of the program in the atomic model, the first state encountered that is enabled with a non-atomic action in Simpson’s algorithm will be as-if atomic (due to the data-race freedom and 1-reader and 1-writer nature of the algorithm). All non-atomic accesses in an as-if atomic state can be treated as atomic; and then inductively it can be shown that the second and all subsequent non-atomic accesses can be treated as atomic. So data-race freedom with atomicity assumption implies data-race freedom without such assumption, and the two models coincide.

3. Semantic basis of induction and deduction rules

**Transition system.** Given a set of states \( S \), we can built a state-transition system \( TS = (S, S_0, \Delta) \) s.t. \( S_0 \subseteq S \) is the set of initial states and \( \Delta \) is a set of small-step transitions (aka indivisible transitions).

For \( TS \), we use \( S_0^R \) to denote the set of reachable states in \( TS \) from \( S_0 \), \( \Delta^R \) to denote the set of reachable transitions in \( TS \), and \( \Delta^+ \) to denote the transitive closure
of $\Delta$; and we call $(s,s') \in \Delta^+$ a big-step transition (aka divisible transition) of $TS$ since $s$ needs to traverse a non-trivial chain of small-step transitions to reach $s'$.

3.1. State invariants and transition invariants

**Predicate and program.** We assume a state $s \in S$ denotes a valuation over a set $X$ of variables, where $X'$ is the set of primed counterparts of $X$. We use $s(x)$ to denote the value held by the variable $x \in X$ at state $s$. A state predicate $p$ (over $X$) denotes a subset $[p]$ of $S$. A state-pair predicate $pp$ (over $X$ and $X'$) denotes a subset $[pp]$ of $S \times S$.

We use $p[X'/X]$ to denote the substitution of $X$ variables occurring in $p$ by their primed counterparts from $X'$. A command $c$ in a program $PG$ can be written as a state-pair predicate whilst the initialisation init of $PG$ can be written as a state predicate.

**Invariant.** A state predicate $p$ is an invariant (for $TS$) iff the set of states it denotes, i.e. $[p]$, is a superset of $S^R$; and furthermore it is an inductive invariant iff $S_0 \subseteq [p]$ and $\Delta([p]) \subseteq [p]$, where $\Delta([p])$ is the image produced by the relation $\Delta$ when its domain is restricted to $[p]$.

**Transition invariant.** A state-pair predicate $pp$ is a (global) transition invariant, i.e. invariant for big-step transitions in $TS$, iff the set of state pairs it denotes, i.e. $[pp]$, is a superset of $(\Delta^R)^+$ (i.e. the set of reachable big-step transitions); and $pp$ is an inductive transition invariant iff $\Delta \cap (S_0 \times S) \subseteq [pp]$ and $[pp] \circ \Delta \subseteq [pp]$, where $[pp] \circ \Delta$ stands for relation composition of $[pp]$ and $\Delta$ (being an extension of function composition).

3.2. Induction and deduction rules for invariance reasoning

The invariance principle of assertional reasoning for concurrent programs lies in the use of invariants of various forms (e.g. state- or transition- invariants) to express everything, from properties and specifications to actions and programs. The reasoning consists of decomposing complex invariants into simple ones and finding inductive invariants from which these simple invariants can be deduced. Below we use $Inv(PG)$ to denote the set of all state- or transition- invariants for program $PG$, and use $inv \in Inv(PG)$ to mean the (state- or state-pair-) predicate $inv$ is a state- or transition- invariant.

An invariant of a concurrent program is a condition that holds true on all reachable global state of the program. The most effective way to establish an invariant is by induction on the initialisation init and all commands of the program, which gives rise to the so-called inductive invariants.

\[
\begin{align*}
\text{init} & \implies p \\
\forall c \in PG : p \land c & \implies p[X'/X] \\
p & \in Inv(PG)
\end{align*}
\]  

(IINDUCTION-S)

Similarly we have inductive transition invariants:

\[
\begin{align*}
\forall c \in PG : (pp[X'/X'] \land c[X'/X]) & \implies pp \land \exists p \in Inv(PG) : (p \land c \implies pp) \\
pp & \in Inv(PG)
\end{align*}
\]  

(IINDUCTION-T)
In order to simplify our proof, we introduce a new technique we call *inductive subject to*. For instance, given a supporting set of invariants \( I \), we say a state predicate \( p \) is an *inductive invariant subject to* \( I \), iff it can be established inductively by checking that, for all \( c_i \) in \( PG \), there exists some (state- or transition-) invariant \( inv_i \in I \) s.t.

\[
p \land inv_i \land c_i \implies p[X'/X]
\]

holds. The same is true for the inductive subject-to technique for transition invariants.

\[
\text{init} \implies p \quad \forall c_i \in PG : \exists inv_i \in Inv(PG) : p \land (inv_i \land c) \implies p[X'/X]
\]

\[
\tag{SUBJECT-S}
\]

\[
\forall c_i \in PG : \exists inv_i \in Inv(PG) : (pp[X'/X'] \land (inv_i \land c_i) \implies pp) \quad \land \quad (\exists p_i \in Inv(PG) : p_i \land (inv_i \land c_i) \implies pp)
\]

\[
\implies pp \in Inv(PG)
\]

\[
\tag{SUBJECT-T}
\]

After the establishment of all the inductive invariants, we often use implication and conjunction to obtain new state- and transition- invariants, which are not necessarily inductive.

\[
pp, pp' \in Inv(PG) \quad pp[X'/X'] \land pp'[X'/X] \implies pp''
\]

\[
\implies pp'' \in Inv(PG)
\]

\[
\tag{COMPOSITION}
\]

\[
inv' \implies inv \quad inv' \in Inv(PG)
\]

\[
\implies inv \in Inv(PG)
\]

\[
\tag{CONSEQUENCE}
\]

\[
inv, inv' \in Inv(PG)
\]

\[
\implies inv \land inv' \in Inv(PG)
\]

\[
\tag{CONJUNCTION}
\]

4. An inductive invariant proof of data-race freedom

In this section, we present our simple proof of data-race freedom, which is based on the invariance principle of assertional reasoning for concurrent programs\(^3\). That is, to establish an invariant, we decompose complex invariants into simple ones and then find inductive invariants to which these simple invariants are consequences.

We can formalise the property of data-race freedom as follows:

\[
\alpha = a \land \beta = b \implies (wp \neq rp \lor wi \neq ri)
\]

\[
\tag{RACE-FREEDOM}
\]

where \( \alpha \) and \( \beta \) are program counters respectively for the writer and for the reader.

The invariant says that if there is a global state (i.e. a value assignment to all the local and shared variables of the programs including program counters) in which the

\(^3\)The proof was first found by the second author in \([10]\).
reader is reading a slot and the writer is writing a slot, then the two slots must be different, i.e. \( wp \neq rp \lor wi \neq ri \), which is essentially the freedom of data races on the slots. **RACE-FREEDOM** can be further strengthened to **RACE-FREEDOM-EX**:

\[
\alpha \in \{a, a+1\} \land \beta \notin \{b-2, b-1\} \implies (wp \neq rp \lor wi \neq ri) \quad \text{(RACE-FREEDOM-EX)}
\]

which is easier to prove by decomposition into three conditions:

\[
\alpha \in \{a, a+1\} \implies wi \neq li[wp] \quad \text{(COND1)}
\]
\[
\beta \notin \{b-2\} \implies r = rp \quad \text{(COND2)}
\]
\[
\alpha \in \{a-1, a, a+1\} \land \beta \notin \{b-2, b-1\} \implies (wp \neq r \lor ri = li[rp]) \quad \text{(COND3)}
\]

where it can be deduced that **COND1 \land COND2 \land COND3 \implies RACE-FREEDOM-EX**.

**COND1** is an inductive invariant, which can be established by checking initialisation as well as all command \( c \) in the four-slot program. Actually, the check is trivial for all commands except for \( a - 1 : \ wi := 1 - li[wp] \) which update \( \alpha \) from \( a - 1 \) to \( a \) since for the other commands either the antecedents of the implications remain invalid or the commands do not update the variables \( wi \) and \( li[wp] \).

**COND2** is an inductive invariant whose check holds trivially for initialisation and all commands except for \( b - 2 : \ r := rp \) and \( b - 1 : \ ri := li[rp] \). With the use of rule **CONSEQUENCE**, we know **COND2** is an invariant.

Similarly, **COND3** is an inductive invariant, whose check holds trivially for initialisation and all commands except for:

\[
\begin{align*}
 a - 2 : & \quad wp := 1 - r \\
 a - 1 : & \quad wi := 1 - li[wp] \\
 b - 1 : & \quad ri := li[rp]
\end{align*}
\]

5. An inductive proof of data coherence and data freshness

Our proof of data freshness and coherence demands the decoration of the original program with auxiliary variables. In this paper we add timestamps to the original program. That is, \( wtm \) is a counter used to timestamp each round of the write operation by the writer so that all writes of shared variables in the same round are decorated with the same timestamp. For instance, variable \( li[x] \) becomes variable \( LI[x] \), which can be understood as a record datatype consisting of two fields: \( LI[x].val \) and \( LI[x].tm \); the former holds the value (say \( v \)) originally held by \( li[x] \) while the latter holds the timestamp marking the exact round at which \( v \) is written into \( li[x] \). Similarly, \( D[x][y] \) are decorated version of \( d[x][y] \).

All the write operations (defined by the procedure \( \text{write}(w) \)) are linearly ordered and it is the same for all the read operations (i.e. the procedure \( \text{read()} \)), giving rise to a pair of linear orders. Within one linear order, we have relations like (linearly) **ordered after** and **immediately ordered after**.
shared \( \mathcal{D}[2][2] = (((v_{00}, 0), (\bot, \bot)), ((v_{10}, 1), (\bot, \bot))) \), \( \mathcal{L}I[2] = ((0, 0), (0, 1)) \), \( l = 1, r = 0, \ wtm, rtm = 1, 0 \) in

local \( \wp = 1, \ wi = 0; \)
\( \text{write}(w) = \)
\( a - 2 : \ wtm := 1 - r; \ wp := 1 - r; \)
\( a - 1 : \ wi := 1 - \mathcal{L}I[\wp].val; \)
\( a : \mathcal{D}[\wp][\wi] := (w, \ wtm); \)
\( a + 1 : \mathcal{L}I[\wp] := (\wi, \ wtm); \)
\( a + 2 : \ l := \wp; \)

local \( \rp = 0, \ ri = 0, y = \bot; \)
\( \text{read}() = \)
\( b - 3 : \ r := l; \ rp := \rp; \)
\( b - 2 : \ r := \rp; \)
\( b - 1 : \ (ri, \ rtm) := \mathcal{L}I[\rp]; \)
\( b : \ (y, \ rtm) := \mathcal{D}[\rp][\ri]; \)
\( b + 1 : \text{return } y; \)

Figure 2: The four-slot algorithm with timestamps

Between linear orders, we say an operation \( A \) from one linear order \( O \) precedes an operation \( B \) from another linear order \( O' \) iff in an interleaved execution of the concurrent programs, the last command in \( A \) are executed before the first command in \( B \); \( A \) overlaps \( B \) iff neither \( A \) precedes \( B \) nor \( B \) precedes \( A \); and \( A \) immediately precedes \( B \) iff \( A \) precedes \( B \) and there is no other operation \( A' \) ordered after \( A \) in \( O \) such that \( A' \) precedes \( B \).

5.1. The proof of data coherence

In this subsection we present a series of state- and transition- invariants for the Simpson’s four slots program in order to prove the main lemma of this paper.

**Lemma 1 (Location monotonicity).** For all timestamped variable \( x \in \{ \mathcal{L}I[p], \mathcal{D}[p][i] \mid p, i \in \{ 0, 1 \} \} \), the transition invariant below holds:

\[ x.tm \leq x'.tm \]

**Proof.** \( x.tm \leq x'.tm \) is an inductive transition invariant subject to the inductive invariant \( \forall x \in \{ \mathcal{L}I[p], \mathcal{D}[p][i] \mid p, i \in \{ 0, 1 \} \} : x.tm \leq wtm. \)

**Lemma 2 (Reader monotonicity).** The transition invariant below holds:

\[ rtm \leq rtm' \]

**Proof.** \( rtm \leq rtm' \) is an inductive transition invariant subject to the invariants:

\[ \beta = b \implies rtm = D[rp][ri].tm \quad \text{(COND)} \]
\[ \beta \in \{ b - 2, b - 1 \} \implies rtm \leq LI[rp].tm \quad \text{(COND')} \]

The COND is an inductive invariant subject to the invariant a) \( \forall p \in \{ 0, 1 \} : \mathcal{L}I[p].tm = D[p][\mathcal{L}I[p].val].tm \), the inductive invariant \( \beta \notin \{ b - 2, b - 1 \} \implies ri = li[rp] \) and the RACE-FREEDOM-EX. The a) is an inductive invariant subject to the COND1 (i.e. \( \alpha = a \implies wi \neq LI[wp].val \) and the inductive invariant \( \alpha = a + 1 \implies wtm = D[wp][wi].tm. \)
The CondB is an inductive invariant subject to the location monotonicity and the invariant \( \beta = b - 3 \implies rtm \leq LI[\text{rp}].tm \leq LI[l].tm \), which is a consequence of the conjunction of the inductive invariant \( \beta \notin \{b - 2, b - 1\} \implies rtm \leq LI[\text{rp}].tm \) (subject to the location monotonicity and the CondA) and the transition invariant 1) \( LI[l].tm \leq LI'[l'].tm \). The 1) is an inductive invariant subject to the location monotonicity and the inductive invariant \( \alpha = a + 2 \implies LI[\text{wp}].tm = wtm \) and \( \forall i \in \{0, 1\} : LI[i].tm \leq wtm \).

**Data coherence:**

If a read operation is ordered before another read operation, the former cannot read from a slot which is strictly more fresh than the one read by the latter.

**PROOF.** Use the reader monotonicity lemma above.

## 5.2. The proof of data freshness

**Data freshness:**

A read operation \( R \) can only read from a write operation overlapping \( R \) or immediately preceding \( R \).

**PROOF.** We need to prove two cases: \( R \) precedes \( W \) implies \( R \) cannot read from \( W \) and \( W \) immediately precedes \( R \) implies \( R \) cannot read from \( W \) ordered before \( W \).

The first case is implied by the transition invariant \( \beta' = b - 2 \land \beta = b + 1 \implies rtm < wtm' + 1 \). It is an inductive transition invariant subject to the inductive invariant e) \( \forall p, i \in \{0, 1\} : D[p][i].tm < wtm + 1 \), the inductive invariant f) \( \beta \in \{b, b+1\} \implies rtm = D[ri][\text{rp}].tm \) (subject to the Race-freedom and CondA), and the reader monotonicity.

The second case is implied by \( \beta = b - 3 \land \beta' = b \implies rtm' \geq wtm - 1 \). It is a consequence of the composition of the reader monotonicity and the invariant k) \( \beta = b - 3 \land \beta' = b \implies rtm' \geq wtm - 1 \). The k) is a composition of the invariants \( LI[l].tm \geq wtm - 1 \) (which can be established by sequential deduction on the writer’s thread only), \( \beta = b - 3 \land \beta' = b - 2 \implies LI'[\text{rp}].tm \geq LI[l].tm \) (inductive subject to \( LI[l].tm \leq LI'[l'].tm \) and location monotonicity), the location monotonicity, and \( \beta = b - 1 \land \beta' = b \implies rtm' \geq LI[\text{rp}].tm \) (inductive subject to the location monotonicity).

The invariant \( LI[l].tm \leq LI'[l'].tm \) can be established by sequential deduction on the writer’s thread only.

## 6. Discussion

Our work differs significantly from existing works on four-slot algorithm verification \([2, 7, 11, 8]\). \([7]\) uses model checking whilst the others, like us, uses theorem proving. \([7]\) encodes and verifies all three properties directly or indirectly whilst the theorem proving works focus mostly on the verification of the data-race freedom.
On the semantic modelling of non-atomic data access, [7] uses ‘random’ variables with non-deterministic assignment whilst we use more a reductionist strategy to collapse such data access to atomic actions.

Lastly, our proof adopts the global approach of assertional reasoning whilst the previous work [1, 9] uses more thread-local approach with rely/guarantee, separation logics and ownership transfer.

7. Conclusion

We have given a simple proof of data-race freedom, data coherence and freshness on Simpson’s four-slot algorithm, which, in conjunction, implies linearisability. It uses only the inductive state- and transition- invariants for the proof of the three properties, which significantly simplified previous works (mostly focusing on data-race freedom) that uses separation logics, rely/guarantee, ownership transfer or their combinations for the same purpose.

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