FlashCam: A fully digital camera for CTA telescopes

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Abstract. The future Cherenkov Telescope Array (CTA) will consist of several tens of telescopes of different mirror sizes. CTA will provide next generation sensitivity to very high energy photons from few tens of GeV to >100 TeV. Several focal plane instrumentation options are currently being evaluated inside the CTA consortium. In this paper, the current status of the FlashCam prototyping project is described. FlashCam is based on a fully digital camera readout concept and features a clean separation between photon detector plane and signal digitization/triggering electronics.

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THE FLASHCAM CONCEPT AND CAMERA ARCHITECTURE

The FlashCam approach is unique amongst the camera projects pursued inside CTA, because signal processing inside the camera is fully digital. Signal digitization and trigger processing are jointly performed in one single readout chain per camera pixel. For a group of pixels, such a chain consists of Flash ADCs and a Field-Programmable Gate Array (FPGA) module, both commercially available at low cost. A camera-wide event trigger is subsequently computed from the digitized signals. The camera data are transferred from the camera front-end to a camera server using a high-performance Ethernet network protocol. Such a fully digital approach using state-of-the-art components provides accurate and flexible triggering and an easily scalable architecture in a cost-effective way. It also permits to cover the full dynamic range per pixel with only one readout channel, respectively, using compression of high amplitude signals in the preamplifier and recovery of the charge through signal processing in the FPGA.

The architecture of FlashCam is based on the concept of a horizontal integration of its components. Here, the photon detector plane (PDP) is a self-contained unit, consisting
of photon detectors, high voltage supplies, preamplifiers, and control logic, which are sustained by a monolithic mechanical carrier. The signal digitization and triggering electronics are organized in boards and mini-crates, which are separated from the photon detector plane. Such an approach allows adaption of various photon detectors and pixel pitches and minimizes the amount of electronics directly at the focal plane, thereby reducing weight and cooling issues there, and also results in cost savings compared to other approaches. The electronics crates are kept either at the rear side of the camera body (in case of a photo-multiplier-(PMT)-based PDP), or could be completely detached from a very compact focal-plane instrument that is based e.g. on Si-PMTs.

In Fig. 1, right, a preliminary mechanical concept for a medium-sized telescope (MST) 1764 PMT pixel camera is shown. The PDP is passively cooled, while crates are cooled by air ventilation. Options for heat exchange to the camera exterior – assuming a near-sealed camera – are being evaluated. Development work towards a Si-PMT-based camera using the FlashCam concept and electronics is being pursued in parallel.

**SIGNAL DIGITIZATION, TRIGGER, AND DATA TRANSMISSION**

The entire FlashCam electronics is based on commercially available microchips, in essence FADCs for signal digitization and FPGAs for further signal and trigger processing. The key point of the concept is to perform all pixel signal processing purely with digitized information. In particular, the trigger decision is computed solely from the digitized signals. For such a camera, low power (<0.5 W/channel) 12bit FADCs are currently available with sampling speeds of up to ∼250 MHz. Through extensive simulations (including realistic time jitter and night sky background conditions) it could be shown that trigger performance as well as the pixel amplitude and timing resolution of such a system is fully competitive with higher (e.g. 1 – 2 GHz) sampling speed systems.

The FlashCam readout and trigger electronics is based on the development of one motherboard with a Spartan-6 FPGA, which carries either FADC digitizer, trigger interface, or clock/master trigger mezzanine (“daughter”) boards (Fig. 1, left). The expected data rate of such a system (∼700 MB/s for a 1764 pixel camera and a trigger and readout rate of 10 kHz) allows the full pixel event information to be transmitted over standard gigabit Ethernet infrastructure without any data reduction. The up to 96 FADC boards have a 1 Gbit Ethernet connection each, which will be routed through one or two 10 Gbit Ethernet lines for data transmission to the camera server. The transmission protocol is raw Ethernet to avoid any overhead of higher level protocols. Current tests of the data transmission routinely operate at rates of up to 1.8 GByte/s, well beyond requirements.

**PMT-BASED PHOTON DETECTOR PLANE MODULES**

The FlashCam PDP concept for PMTs is based on mechanical modules of 12 pixels (Fig.2, left). Each module contains PMTs, preamplifiers, HV supply, and a microcontroller for slow control and monitoring. Each module weighs about 1.1 kg and dissipates only 2.3 W. Two such PDP modules are served by one FADC electronics board. The analogue signals of the PMTs are transmitted via CAT 5/6 cables (four differential
FIGURE 1. **Left:** FlashCam motherboard (14 layers PCB stack), with one backplane connector (32 1 Gb/s LVDS pairs) and two daughter board connectors (99 1 Gb/s LVDS pairs each). Two 12 channel FADC daughter boards (10 layers PCB stack), with 3 RJ45 connectors for analogue signals and a 400 pin motherboard connector, can be mounted on the motherboard (semi-transparent insets). **Right:** Drawing of a possible implementation of a FlashCam-based MST camera. Front and rear doors are open, isolation panels as well as light guides are not shown. A human can enter the camera body and can access the rear of the photon detector plane as well as all electronic crates, for installation and in case of repair work.

![FlashCam motherboard and MST camera diagram](image)

FIGURE 2. **Left:** Front view of the FlashCam 12-pixel PDP module. PMTs are from Hamamatsu (R11920, the current baseline option for CTA). **Right:** Simulated (lines) and measured (data points) pixel amplitude resolution. Simulations and measurements are for 240 MHz night sky background (NSB), for the CTA PMT, and using a search window of ±1 ns and an integration window of 8 ns. Air shower light was emulated with a fast (FWHM < 300 ps) laser and a filter wheel, and NSB with a light bulb.

![FlashCam PDP module and amplitude resolution plot](image)

Through one additional (9-pin D-sub) connector, CAN-bus control and 24 V power supply are provided to each PDP module. Low (±5 V) and high voltage are generated on the module, thereby avoiding expensive HV-rated connectors.

The HV regulation features a separation into two bias supply lines (−1500 V and −500 V) and supplying the last three dynodes via an emitter follower PNP transistor circuit. Compared to conventional designs, power consumption is considerably reduced here. Pixels are individually controllable (HV off, HV −700 V, .. −1500 V). A HV design with even lower cost and power consumption is currently being evaluated as well.
FLASHCAM PIXEL PERFORMANCE

The FlashCam concept foresees the use of preamplifiers with non-linear gain characteristics, instead of splitting the signal into two separate channels with different (low and high) gains. This allows cost to be reduced (the low gain channel can be saved), and permits full flexibility should future simulations result in a dynamic range requirement below the currently anticipated 3000 photoelectrons (pe) per pixel. The baseline design is to run an operational amplifier with a high input resistor (1-2 kΩ instead of 50 Ω). High amplitude signals (≳ 200 pe) saturate the output of the amplifier, but the input signal can be restored since the output signal broadens with a defined recovery time. The analysis of the digitized signal therefore runs in two regimes: Below 200 pe, the full time-resolved signal can be stored (with a window of ~60-80 ns), and digital filtering performed at server level allows the signal amplitude to be computed. Above 200 pe, the signal is reconstructed directly in the FPGA from an integration over ~200 ns.

The system was verified under realistic conditions, using a FlashCam PDP module and a demonstrator board with 250 MHz sampling speed. Comparisons of the measured data with simulated performance expectations (e.g. Fig. 2, right) show that the system is fully understood. The achieved values are well within requirements for CTA cameras.

CAMERA-WIDE EVENT TRIGGER AND PERFORMANCE

In FlashCam, the event trigger is derived from the digitized pixel signals processed in FPGAs. The digitized signals are sent from the eight FADC boards via backplane to the trigger board in the same crate. Each trigger board has an interface of 226 differential signal pairs connected to the FADC boards. Each of these lines can receive up to 1 Gbit/s of data. The total transmission capacity of 12 trigger boards is around 2.7 Tbit/s.

The trigger algorithm is freely programmable by the FPGA firmware in each FADC and trigger board. Various trigger algorithms can be exploited and improved even during run-time of the experiment. Simulations show that a pre-grouping of pixel trigger into pixel “patch” information can be used to reduce bandwidth requirements (number of pins) without significant loss of sensitivity. A patch size of three pixels provides excellent spatial trigger homogeneity and sensitivity combined with high versatility and thus is used for the design of the MST-scale FlashCam prototype. The 3-pixel-patch information can contain up to 8 bit of information and allows to code multiplicity and/or summed amplitude triggers (clipped sum trigger). Simulations show that the performance of this bandwidth is almost indistinguishable from full-bandwidth trigger data transmission. The patch information is sent at each clock cycle (4 ns) to the trigger cards. There, a trigger decision from 3, 7, or 19 of these patches is computed. The final patches have a roundish form and can be computed around each 3-pixel-patch individually.

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