A device for paired zeroing of numbers in a residue system

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Abstract. The paper studies the problem of developing a high-speed number correction device
in computing systems operating in the basis of non-positional arithmetic in residual classes. The
 topicality of the problem is necessitated by the search of solutions allowing reducing the time
for digital processing of signals in non-positional neuroprocessors. The device allows correcting
errors with single and multiple control bases of the residue system. The work presents the
structure of the unit that realizes the paired zeroing on numbers in the system of residual classes.
It was demonstrated that the suggested solutions allow appreciably reducing the time
consumption by digital processing of signals in neuroprocessors destined for operations of
summation and multiplication.

1. Introduction

Large amount of calculations necessary for processing telemetry of oil and gas wells, modeling of
bottom-hole zone treatment under complex geological conditions requires new solutions for reliable and
fast implementation of basic arithmetic operations of summation and multiplication. The development
of a non-positional neuroprocessor considerably accelerates the calculations. However, the provision of
reliable calculations is still a challenge. The paper considers the synthesis of a device for error correction
on the basis of the modified method of paired zeroing of numbers in the system of residual classes.

In [1], the authors consider the introduction of the term zeroing of numbers. Outstanding works allow
developing the theory of error correction in a non-positional system of residual classes and suggesting
a method of paired zeroing of numbers in a residue system. The peculiarity of the method is its focus on
cutting time consumption for correction of single and multiple errors. The authors have solved a problem
of device development functioning according to the said method.

2. Materials and Methods

Zeroing is one of the methods for determining the correctness of a number. It involves conversion of
initial number \( A = (\alpha_1, \alpha_2, ..., \alpha_n, \alpha_{n+1}) \) into number \( A^{(0)} = (0, 0, ..., 0, y_{n+1}) \) using the transformation
sequence that does not allow a single escape from working range \( M = (m_1 \times m_2 \times ... \times m_n) \), where \( m_i \)
are the bases of the moduli of residual class system [1–3].
The process of number zeroing envisages consecutive subtraction of constants from this number.

\[(m_{11}, m_{21}, \ldots, m_{n+1}), m_{11} = 1, 2, \ldots, m_1 - 1;\]

\[(0, m_{22}, \ldots, m_{n+2}), m_{22} = 1, 2, \ldots, m_2 - 1;\]

\[(0, 0, \ldots, m_{nn}, m_{n+1}), m_{nn} = 1, 2, \ldots, m_n - 1.\]

In this case, number \(A = (\alpha_1, \alpha_2, \ldots, \alpha_{n+1})\) is consecutively transformed into \(\hat{A} = (0, \alpha'_2, \ldots, \alpha'_{n+1}),\)
then into \(A'' = (0, 0, \alpha''_2, \ldots, \alpha''_{n+1}),\) and so on.

After \(n\) iterations, we get \(A^{(H)} = (0, 0, \ldots, 0, y_{n+1}).\)

If \(y_{n+1} = 0,\) then the initial number is correct (lies within interval \([0, M]\); if \(y_{n+1} \neq 0,\) then the number is incorrect and lies within interval \([M, (j+1)M]\) for \(j=1,2,\ldots, m_{n+1} - 1.\) The value of interval number \((j+1),\) where gets operand \(\hat{A}\) is determined from

\[j = \left[\frac{\Delta_0 \times m_{i} \times m_{n+1}}{m_i}\right] (\text{mod } m_{n+1}) + \Delta_0,\]

where \(\Delta_0\) takes on either value 0, or 1.

Error \(\Delta A\) can lead a correct number \(A,\) lying in interval \([0, M)\), only one of the two intervals.

Let \(\hat{A} = A + \Delta A,\) or \(\hat{A} = (\alpha_1, \alpha_2, \ldots, \alpha_{n+1}) + (0, 0, \ldots, \Delta a_i, \ldots, 0).\)

Then, evidently, \(\Delta A\) lies not in the first interval \([0, M),\) because number \(A_0 = (0, 0, \ldots, 0)\) lies in the first interval.

Let \(\Delta A\) lie in the \(k\)-th interval:

\[(k - 1)M \leq \Delta A < kM.\]

In the system of inequalities, let us

\[
\begin{align*}
0 & \leq A < M \\
(k - 1)M & \leq \Delta A < kM
\end{align*}
\]

sum up

\[(k - 1)M \leq A + \Delta A < (k + 1)M.\]

Let us assume \(j = k - 1,\) then we can write \(jM \leq \hat{A} < (j + 2)M,\) i.e. an error can turn correct operand into incorrect one lying only in one of the two intervals, \([jM, (j + 1)M]\) or \([(j + 1)M, (j + 2)M]\).

The obtained result is applied for determining an alternative combination of numbers in the system of residual classes by the method of zeroing.

The time of zeroing is determined as \(T = 2\pi \tau_\Sigma,\) where \(\tau_\Sigma\) is time of zeroed number summation with zeroing constant. The number of zeroing constants equals

\[k = \sum_{i=1}^{n} m_i - n,\]

while the number of digits of the storage of the constants in the non-positional neuroprocessor equals

\[c = \left(\sum_{i=1}^{n} m_i - n\right) (n - i)\]

Obviously, the most important of the strong points of the system of residual classes—high operation speed of modular operations—is lost during zeroing. The time of operation implementation is comparatively high, which lowers the efficiency of residue system application.

However, there is the method of paired zeroing of numbers in the system of residual classes [4-6]. According to the method, at each step, the zeroing is performed simultaneously in two bases. Zeroing time decreases twofold and equals \(T = n \tau_{C\Sigma \hat{A}}.\)

The total number of zeroing constants equals

\[k = \sum_{i=1}^{n} m_i m_{n-i+1} - n/2,\]

while the number of digits of zeroing constants equals

\[c = \left(\sum_{i=1}^{n/2} m_i m_{n-i+1} - n/2\right) (n - 2i).\]

### 3. The study

In the method of paired zeroing of numbers with preliminary sampling of digits, the operations of summing and sampling of the next zeroing constant are combined in certain time cycles. In addition, the
sampling of the next constant is performed with preparation of values of numbers that will be used at the next zeroing stage to select a subsequent zeroing constant for the number.

\( 0, \ldots, 0, \alpha_i, \alpha_{i+1}, \ldots, \alpha_{n-i}, \alpha_{n-i+1}, 0, \ldots, \beta_{n+1} \).

Values \( \alpha_i \) and \( \alpha_{n-i+1} \) in an elementary member working in bases \( m_{i+1} \) and \( m_{n-i} \) can be used to prepare values \( \alpha_{i+1}' \) and \( \alpha_{n-i}' \) that will be exploited at the next zeroing stage to sample the constant. Indeed, values \( \Delta \alpha_{i+1} \) and \( \Delta \alpha_{n-i} \) that will be subtracted from \( \alpha_{i+1} \) and \( \alpha_{n-i} \), correspondingly, are determined only by values \( \alpha_i \) and \( \alpha_{n-i+1} \). During constant sampling using values \( \alpha_i \) and \( \alpha_{n-i+1} \) from corresponding tables in a single cycle values \( \alpha_{i+1}' \) and \( \alpha_{n-i}' \) can be used. In this case, it is unnecessary to have digits in bases \( m_{i+1} \) and \( m_{n-i} \), which will allow decreasing the capacity of zeroing constants

\[
C = \left( \sum_{i=1}^{n/2} m_i m_{n-i+1} - n/2 \right) (n - 2i - 2).
\]

The number of summations in suggested zeroing variant equals \( \left( \frac{n+1}{2} \right) \), since the zeroing is simultaneously performed in all informational bases of the system of residual classes in pairs. After every two summations, one additional cycle is required for the formation of the next address and reference to the storage of the zeroing constants. In this connection every two summation cycles \( (\tau_S = T_0) \) correspond to one cycle without summation. If conventional paired zeroing at \( n = 5 \) (summation of two zeroing constants) requires four conditional time cycles \( 4T_0 \), then the considered method requires three cycles \( 3T_0 \).

Generally, the analytical dependence of the zeroing time on the number of information bases of the system of residual classes can be represented as

\[
T = \left[ \frac{n+1}{2} \right] \tau_S + \left[ \frac{n+1}{2} + 1 \right] \tau_{mem},
\]

where \( [x] \) is the integral part of \( x \), that does not exceed \( x \), \( \tau_{mem} \) is the time of reference to the storage (table memory) of zeroing constants.

The device for method realization is depicted in Fig 1. The device includes OPERATING REGISTER and MEMORY REGISTER, DECODERS, SWITCHES, TABLE OF ZEROING CONSTANTS, ERROR CONSTANTS TABLE, summing device (\( \Sigma \)), VALVES, KEYS and SWITCHBOARDS [6].

The detection and correction of errors in the device is implemented in steps (cycles). At step one, into OPERATING REGISTER and MEMORY REGISTER, the initial number \( A = (\alpha_1, \alpha_2, \ldots, \alpha_n, \alpha_{n+1}) \) is input.

At step two, from OPERATING REGISTER, operand \( A \) is read that goes into the input of summing device (\( \Sigma \)). Simultaneously, using values \( \alpha_1 \) and \( \alpha_n \) a zeroing constant is selected from the TABLE OF ZEROING CONSTANTS. In the first and \( (n-1) \) DECODERS, values \( \alpha_1, \alpha_2 \) and \( \alpha_n, \alpha_{n-1} \) are used to determine corresponding values \( \alpha_2' \) and \( \alpha_{n-1}' \). \( \alpha_2' \) and \( \alpha_{n-1}' \) is used at the next step to determine the next zeroing constant. At step three, the chosen zeroing constant is subtracted from the contents of summing device (\( \Sigma \)). Concurrently, values \( \alpha_2' \) and \( \alpha_{n-1}' \) are used to reference to the TABLE OF ZEROING CONSTANTS).
Figure 1. Error correction device in non-positional neuroprocessor with preliminary sampling.

At step four, the contents of summing device (Σ) gets into the OPERATING REGISTER; then, through overwrite bus, together with zeroing constant it returns to summing device (Σ) for consecutive summation. Concurrently, in the second and \((n-2)\) SWITCHBOARDS, corresponding values \(\alpha_3'\) and \(\alpha_{n-2}'\) are determined.

Thus, the zeroing process continues unless in all \(\alpha_k = 1, \overline{n}\) stand zeros. Then, the signal from the second middle DECODER (at even \(n\)) or from the second output of any of middle DECODERS (at odd \(n\)) opens corresponding VALVES. Through VALVES from MEMORY REGISTER, value \(A = (\alpha_1, \alpha_2, \ldots, \alpha_n, \alpha_{n-1})\) gets into summing device (Σ). Concurrently, value \((\gamma_{n+1} \neq 0)\) is sent to ERROR CONSTANTS TABLE, where necessary constant is chosen. On its turn, the selected constant gets to summing device (Σ) and is calculated from \(A\). The number corrected in such a way gets to the output of
the device through respective KEYS. If there is no error, i.e. $\gamma_{n+1} = 0$, then number $A$ is sent directly to device output.

4. Conclusions
In the above we have developed a device implementing the method of paired zeroing of numbers in the system of residual classes with preliminary sampling of digits. The developed error correction unit has high signal processing speed and will allow appreciably increasing the calculation reliability of a non-positional neurocomputer. The high error correction speed is achieved through the displacement (paralleling) of several operations in time. The practical application of the studies is aimed at the solution of problems described in [7–10].

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