The Generalized Metastable Switch Memristor Model

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Abstract—Memristor device modeling is currently a heavily researched topic and is becoming ever more important as memristor devices make their way into CMOS circuit designs, necessitating accurate and efficient memristor circuit simulations. In this paper, the Generalized Metastable Switch (MSS) memristor model is presented. The Generalized MSS model consists of a voltage-dependent stochastic component and a voltage-dependent exponential diode current component and is designed to be easy to implement, computationally efficient, and amenable to modeling a wide range of different memristor devices.

I. INTRODUCTION

Many memristive materials have recently been reported, and the trend continues. Memristor models are also being developed and incrementally improved upon [1], [2], however most models to date have shortcomings, especially when used to model the type of devices we are interested in using to build neuromorphic processors such as Thermodynamic-RAM [3], [4], [5]. Additionally, most memristors seemingly display some measure of stochastic behavior, while most models assume a deterministic device. Naous et al. recently proposed another model, which can add stochasticity to any existing model [6]. We felt that a stochastic model built from the ground up was a more natural fit to actual devices and designed it to satisfy several requirements: (1) It should accurately model the device behavior including stochastics, (2) it should be computationally efficient, (3) and it should model as many different devices as possible.

II. GENERALIZED MSS MODEL

In our proposed semi-empirical model, the “generalized metastable switch (MSS) memristor model”, the total current through the device comes from both a memory-dependent current component, \( I_m \), and a Schottky diode current, \( I_s \) in parallel:

\[
I = \phi I_m(V,t) + (1 - \phi) I_s(V)
\]

(1)

where \( \phi \in [0,1] \). A value of \( \phi = 1 \) represents a device that contains no Schottky diode effects. The Schottky component, \( I_s(V) \), follows from the fact that many memristive devices contain a Schottky barrier formed at a metal–semiconductor junction. The Schottky component is modeled by forward bias and reverse biased components as follows:

\[
I_s = \alpha_t e^{\beta_t V} - \alpha_r e^{-\beta_r V}
\]

(2)

where \( \alpha_t, \beta_t, \alpha_r, \) and \( \beta_r \) are positive valued parameters setting the exponential behavior of the forward and reverse exponential current flow across the Schottky barrier.

The memory component of our model, \( I_m \), arises from the notion that memristors can be represented as a collection of conducting channels that switch between 2 states of differing resistance. Modification of device resistance is attained through the application of an external voltage gradient that causes the channels to transition between high and low conducting states. As the number of channels increases, the memristor will become more incremental as it acquires the ability to access more states. We treat each channel as a metastable switch (MSS) and the conductance of a collection of metastable switches captures the memory effect of the memristor.

The probability that a single MSS will transition from the B state to the A state is given by \( P_A \), while the probability that the MSS will transition from the A state to the B state is given by \( P_B \). The transition probabilities are modeled as:

\[
P_A = \alpha \frac{1}{1 + e^{\beta(V - \Delta \phi)}} = \alpha \Gamma (V;V_A)
\]

(3)

and

\[
P_B = \alpha (1 - \Gamma (V;V_B))
\]

(4)

where \( \beta = \frac{e}{kT} = (V_T)^{-1} \). Here, \( V_T \) is the thermal voltage and is equal to approximately 26 mV at \( T = 300 K \), \( \alpha = \frac{\Delta \phi}{t_c} \) is the ratio of the time step period \( \Delta t \) to the characteristic time scale of the device, \( t_c \), and \( V \) is the voltage across the device. The probability \( P_A \) is defined as the positive-going direction, so that a positive applied voltage increases the chances of occupying the A state. Each switch has an intrinsic electrical conductance given by \( G_A \) and \( G_B \). The convention is that \( G_B > G_A \). Note that the logistic function \( \frac{1}{1 + e^{-\beta}} \) is similar to the hyperbolic-sign function used in other memristive device models. Our use of the logistic function follows simply from the requirement that probabilities must be bounded between 0 and 1.

Up until this point we have only considered a single MSS being in the A or B state and its probability of it changing states given external stimuli. We now model a memristor as a collection of \( N \) MSSs evolving in discrete time steps, \( \Delta t \). The total memristor conductance is given by the sum over each MSS:
The change in the memristor conductance is thus given by:
\[
\Delta G_m = \Delta N_A \cdot G_A - \Delta N_B \cdot G_B
\]
(7)
and the memory-dependent current is thus:
\[
I_m = V \left( G_m + \Delta G_m \right)
\]
(8)
where \(V\) is the voltage across the memristor during the time-step.

III. RESULTS AND DISCUSSION

Figure 1 shows the hysteresis curve of a fitted model for a raw Tungsten Ag-chalcogenide device data driven at 500 Hz with a sinusoidal voltage of 0.5 V amplitude. Reducing the number of MSSs in the model reduces the averaging effects and causes the memristor to behave in a more stochastic way. Note that as the number of MSSs becomes small, the normal approximation to the binomial distribution also breaks down. In this case, one could use the binomial distribution directly if so desired. An addition of a Schottkey diode current response seen in many memristor devices is illustrated by changing \(\phi\), \(\alpha\), and \(\beta\).

The generalized metastable switch memristor model presented does an excellent job at modeling the hysteresis behavior of a W-Ag-chalcogenide device with a quick manual fitting procedure. Not shown here is additional satisfactory modelling under a diverse set up simulations: triangle drive waveforms, pulses, positive and negative voltages, two devices connected in series, and additional memristor types. Future work includes porting the model over to Verilog and SPICE. Source code for the model and simulations is available upon request.

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