An LDO regulated DC-DC converter with voltage ripple suppression and adaptive dropout voltage control

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Abstract: This paper presents a low dropout regulator (LDO) regulated DC-DC converter with suppressed voltage ripple and enhanced light load efficiency. In this proposed hybrid system, an adaptive dropout technique, where DC-DC converter takes the gate of LDO’s power transistor as the feedback point to combine DC-DC converter and LDO in one control loop, is adopted to make LDO’s dropout voltage adaptive to load current rather than fixed value. Owing to the cascaded LDO and the adaptive dropout technique, the hybrid system obtains a small voltage ripple with improved overall efficiency, especially in light load. The chip was implemented in 130 nm CMOS process. The voltage ripple is reduced to 3 mV at the load current of 40 mA. The overall efficiency of the proposed hybrid system is 60.74% in 30 mA light load and is improved by 15.6% compared with conventional fixed dropout voltage architecture.

Keywords: DC-DC converter, LDO, voltage ripple, conversion efficiency, adaptive dropout voltage

Classification: Power devices and circuits

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1 Introduction

The development of Internet of Things (IoT) and wearable devices has become an important trend in consumer electronics. IoT electronics works in standby mode most of the time and activates when entering data transmission operation, thus requiring both high light load efficiency and load-adaptive efficiency for power management integrated circuit (PMIC). What’s more, noise-sensitive analog circuits integrated in system-on-chips (SoCs) need small output ripples capacity for PMIC. Switched mode DC-DC converter (e.g. inductive buck converter, switched-capacitor DC-DC converter) with high conversion efficiency suffers from remarkable output voltage ripples owing to the switching principle [1], which is a problem for supplying noise-sensitive analog/RF circuits. To address this problem, a hybrid system cascading DC-DC converter and LDO is commonly used to reduce voltage ripple for LDO’s superior noise characteristic. The DC-DC converter provides high efficiency as the first stage and the cascaded LDO provides an almost ripple-free output as the second stage. Several hybrid systems with different architectures [2, 3, 4, 5, 6, 7, 8, 9, 10] have been investigated. In conventional hybrid systems [2, 3, 4], a separate LDO is connected directly in series with a separate DC-DC converter. Thus, LDO’s dropout voltage is fixed to a sufficiently large value based on maximum load to ensure a proper working region of LDO’s power transistor. When load current decreases, this large dropout voltage is excessive, which results in degradation of efficiency. Improved hybrid systems with load-adaptive dropout voltage are presented in literatures [6, 7, 8, 9, 10]. In these improved systems, a
load current sensing circuit is adopted to replicate the load current and feedbacks the current information to the control loop to generate adaptive dropout voltage. However, the current sensing circuit is complex to guarantee the accuracy of current sensing and both duplicated transistor and current sensing circuit will increase silicon area and power loss.

Motivated by the previous research and the existing issues, a new combined structure of DC-DC converter and LDO with adaptive dropout technique is proposed in this paper. Through taking the gate of LDO’s power transistor as the feedback point, the LDO is embedded in the DC-DC converter’s control loop, which rents the dropout voltage to be dynamically adjusted according to load current without adding extra auxiliary circuits. Owing to this adaptive dropout voltage technique, output voltage ripple is effectively suppressed by the LDO and a load-adaptive enhanced efficiency is obtained simultaneously.

2 Architecture of DC-DC converter with embedded LDO

The architecture of proposed DC-DC converter with embedded LDO is shown in Fig. 1. It consists of a digital controlled inductive buck converter, an LDO, a loop reference generator and off-chip components including inductor and capacitors. The DC-DC converter used is digitally controlled [11] and operates in pulse width modulation (PWM) mode over the entire load range. Pulse frequency modulation (PFM) mode or pulse skip modulation (PSM) mode in light load [12] can be added to further improve efficiency in future work. Different from two independent loops in conventional hybrid systems with fixed dropout architecture [2, 3, 4], the digital controlled DC-DC converter in this proposed architecture takes the gate of LDO’s power transistor, instead of the output of DC-DC converter, as the feedback point in combining the separate loops of DC-DC converter and LDO into a whole control loop to obtain an adaptive dropout voltage. This adaptive dropout architecture lowers the output voltage of DC-DC converter, thus lowering the LDO’s dropout voltage when load current is lower than maximum load.

Owing to the combined control loop, the gate voltage $V_{\text{gate}}$ of LDO’s power transistor is approximately equal to the loop reference voltage $V_{\text{ref,dcdc}}$ in steady state. Therefore, when load current changes, $V_{\text{gate}}$ maintains constant so that the DC-DC converter’s output voltage $V_{\text{out,dcdc}}$ changes accordingly, which leads to the load-adaptive dropout voltage. The LDO’s power transistor is designed to work in the saturation region. Therefore, in steady state, the LDO’s dropout voltage is given by:

$$V_{\text{dropout}} = \sqrt{\frac{2I_{\text{load}}}{W}} + |V_{\text{shp}}| + V_{\text{ref,dcdc}} - \beta V_{\text{ref,LDO}}$$

where $I_{\text{load}}$ is the load current, approximately equal to the current passing through power transistor; $\beta$ is the feedback coefficient.

From Eq. (1) it is observed that the LDO’s dropout voltage follows the load current by a square root law. Therefore, as the load current decreases, a smaller dropout voltage is obtained to reduce the excessive conduction loss on power
transistor and enhance efficiency while ensuring proper function of the power transistor for good voltage ripple suppression.

3 Small signal analysis of proposed hybrid system

As mentioned before, in order to make LDO’s dropout voltage adaptive to load current, LDO is embedded in the control loop of DC-DC converter. To guarantee the stability of combined control loop, the small signal model of proposed hybrid system and the open-loop transfer function of combined control loop need to be analyzed first.

The complete small signal model of proposed hybrid system is illustrated in Fig. 2 (neglecting the loop delay resulting from the sampling and computing operations), where $V_{\text{ref}_\text{dcdc}}$ is the reference voltage of combined control loop; $V_{\text{ref}_\text{LDO}}$ is the reference voltage of LDO; $H$ is the feedback coefficient; $g_m$ is the transconductance of LDO’s power transistor; $Z_0$ is the output impedance of LDO.

Neglecting the equivalent series resistor of output capacitor and the dc resistor of inductor, the control-to-output transfer function of DC-DC converter is given by:

$$G_{\text{vd}}(s) = \frac{V_{\text{in}}}{LC_{\text{dcdc}}s^2 + s \frac{L}{R} + 1}$$  \hspace{1cm} (2)

In this hybrid system, the output load of DC-DC converter is LDO so that R in this formula should be replaced by LDO’s input impedance $Z_{\text{in,LDO}}$.

The transfer function of the digital pulse-width modulator (DPWM) is given by (neglecting the delay between the time the DPWM input is updated and the time the switch duty-ratio changes):

$$K_{\text{DPWM}} = \frac{1}{2^{N_{\text{DPWM}}}} - 1$$  \hspace{1cm} (3)

The transfer function of ADC is given by (neglecting the delay of sampling operation):

Fig. 1. Architecture of proposed DC-DC converter with embedded LDO
where \( V_q \) is the resolution of ADC.

The transfer function of LDO’s error amplifier is \( A(s) \). Since the bandwidth of LDO’s error amplifier is much higher than the bandwidth of hybrid system, \( A(s) \) can be replaced by its DC gain A within the bandwidth of hybrid system. A PID compensator is designed to give an appropriate crossover frequency with phase margin \( \phi_m > 60^\circ \) and the very high DC gain. The typical transfer function of PID compensator is given by:

\[
G_{\text{comp}}(s) = K_{\text{comp}} \frac{1}{s} + \frac{s}{Q_{\text{comp}} \omega_z} + \left( \frac{s}{\omega_z} \right)^2
\]  

By breaking the combined closed-loop at the gate of LDO’s power transistor, the open-loop transfer function of hybrid system can be derived by Mason’s Law:

\[
T(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{g_{mp}Z_oHA}{1 + g_{mp}Z_oHA} \times K_{\text{ADC}}G_{\text{comp}}(s)K_{\text{PWM}}G_{\text{vd}}(s)
\]  

The second part \( K_{\text{ADC}}G_{\text{comp}}(s)K_{\text{PWM}}G_{\text{vd}}(s) \) of Eq. (6) is almost the same form as the open-loop transfer function of independent DC-DC converter. The first part of Eq. (6) can be written in other format after replacing LDO’s output impedance \( Z_o \) with specific value:

\[
\frac{g_{mp}Z_oHA}{1 + g_{mp}Z_oHA} = \frac{g_{mp}R_{\text{load}}HA}{1 + g_{mp}R_{\text{load}}HA} \times \frac{1}{1 + s \frac{C_{\text{LDO}}}{1 + g_{mp}HA}}
\]  

In this formula, \( g_{mp}R_{\text{load}}HA \) is the DC loop gain of LDO and obviously it is much larger than 1, so that Eq. (7) can be simplified as:

\[
\frac{g_{mp}Z_oHA}{1 + g_{mp}Z_oHA} \approx \frac{1}{1 + s \frac{C_{\text{LDO}}}{g_{mp}HA}}
\]  

The pole Eq. (8) introduced is \( g_{mp}HA/C_{\text{LDO}} \) and it is much higher than the bandwidth of hybrid system for large value of error amplifier’s gain A. So that the effect of this pole can be neglected within the bandwidth of hybrid system. Therefore, after neglecting the first part of Eq. (6), the open-loop transfer function of hybrid system can be simplified:
\[ T(s) \approx K_{ADC}G_{comp}(s)K_{DPWM}G_{vd}(s) \]
\[ = \frac{1}{V_q} \times \frac{1}{2^{N_{PWM}}} - 1 \times \frac{V_{in}}{s^2L\left(C_{dcdc} + \frac{C_{LDO}}{K}\right) + s\frac{L}{K_{R_{LDO}}} + 1} \times \frac{1}{s} \frac{1}{Q_{comp}\omega_c} + \left(\frac{s}{\omega_c}\right)^2 \]

where \( K = \frac{4H_{comp}}{1 + \frac{1}{1 + G_{comp}}} \) is an extremely large value.

The specifications of this hybrid system are as follows: \( V_{in} = 2.5 \text{ V}, V_{out} = 1.2 \text{ V}, V_q = 6 \text{ mV}, N_{PWM} = 9, L = 4.7 \mu\text{H}, C_{dcdc} = 10 \mu\text{F}, C_{LDO} = 4.7 \mu\text{F}. \) Based on these circuit parameters, the open-loop transfer function of hybrid system after being compensated to 200 kHz crossover frequency and 70° phase margin under the load current of 100 mA is given by:
\[ T(s) = \frac{5.425 \times 10^{-5}s^2 + 11.981s + 6.618 \times 10^5}{4.706 \times 10^{-11}s^3 + 1.066 \times 10^{-9}s^2 + s} \]  

(10)

The bode plot of Eq. (10) is depicted in Fig. 3. As illustrated in Fig. 3, after compensation the bandwidth of hybrid system is about 187.9 kHz and the phase margin is about 79.3°, which satisfy the stability requirement.

### 4 Loop reference voltage generator

As shown in Fig. 1, there is a circuit block named Reference Generator in the architecture of this proposed hybrid system. The function of this circuit block is to generate reference voltage for the combined control loop. This section will explain the setting principle of loop reference voltage and the complete circuit of loop reference voltage generator.

In this proposed hybrid system, the loop reference voltage determines the dropout voltage and the PSRR of LDO at the same time. The relationship between the operating region and the dropout voltage of power transistor is depicted in Fig. 4(a). In addition, the relationship between the dropout voltage and the PSRR is depicted in Fig. 4(b) [9].
When LDO operates with smaller dropout voltage, its power transistor works in triode region with the acquisition of higher efficiency and lower PSRR. This condition occurs because small dropout voltage eliminates the conduction loss on the power transistor to enhance efficiency. Simultaneously, the power transistor in the triode region exhibits a resistive characteristic rather than voltage control current source in the saturation region so that the noise from the input is almost delivered directly to the output without suppression. By contrast, larger gate voltage results in larger dropout voltage across power transistor so that can obtain higher PSRR for working in the saturation region while deteriorating efficiency for excessive conduction loss on power transistor.

In order to achieve optimal tradeoff between output voltage ripple and conversion efficiency, LDO’s power transistor is designed to operate in the critical condition between triode region and saturation region.

The complete circuit of loop reference voltage generator is shown in Fig. 5. This circuit is composed of two parts: the left part is a simple LDO, which is used to generate a voltage equal to the system’s output voltage $V_{\text{out,LDO}}$, the right part is to obtain the threshold voltage of duplicated unit $M_c$ to substitute the threshold voltage of LDO’s power transistor. $M_c$ is placed in the same environment and is also well-matched in layout with LDO’s power transistor. Current source $I_{\text{source}}$ provides a small current to make $M_c$ operate in the critical conduction state, so that the voltage difference between gate and source of $M_c$, which is also equal to the voltage drop on resistor $R_1$, is approximately equal to the threshold voltage of $M_c$. The ratio of current mirror $M_4$ and $M_5$ is 1:1 and the resistance of resistor $R_1$ and $R_2$ is equal, so that the voltage drop on resistor $R_2$ is also approximately equal to the threshold voltage of $M_c$. Therefore, the output voltage of this circuit is:

$$V_{\text{out}} = V_{\text{out, LDO}} - |V_{\text{thp}}|$$  \hspace{1cm} (11)

This output voltage is used as loop reference voltage $V_{\text{ref,cdc}}$. In steady state, the gate voltage of LDO’s power transistor is fixed to this reference voltage $V_{\text{out, LDO}} - |V_{\text{thp}}|$. So that the voltage difference between gate and drain is almost equal to the threshold voltage of power transistor. Therefore, the LDO’s power transistor operates in the critical condition between triode region and saturation region.
5 Measurement results and comparison

5.1 Measurement results

The conventional hybrid system with fixed dropout voltage and the proposed hybrid system with adaptive dropout voltage were respectively fabricated in 130 nm CMOS process. The input voltage of hybrid system ranges from 2 V to 3.5 V. The output voltage of LDO is 1.2 V. The load current of LDO ranges from 0 to 100 mA. The switching frequency of inductor-based buck converter is 1 MHz. The off-chip inductor for buck converter is 4.7 µH and the off-chip output capacitors for buck converter and LDO are 10 µF and 4.7 µF respectively. The chip photomicrograph is shown in Fig. 6. Its total die area is about 1.76 mm².

Fig. 6. Chip photomicrograph of the proposed hybrid system

Fig. 7 shows the output voltage waveforms of DC-DC converter and LDO at the load current of 90 mA and 60 mA, respectively. In Fig. 7(a), the average output voltage of DC-DC converter is about 1.62 V and the voltage ripple of DC-DC converter is about 10.5 mV at the load current of 90 mA. In Fig. 7(b), the average output voltage of DC-DC converter is about 1.51 V and the voltage ripple of DC-DC converter is about 15 mV at the load current of 60 mA. For these two loads, the voltage ripple of LDO is about 5 mV and 4 mV, respectively. Hence, the output voltage ripple can be effectively reduced through cascaded LDO’s suppression.

Fig. 8 shows the dropout voltage and output voltage ripples at DC-DC converter and LDO of proposed hybrid system. The dropout voltage ranges from...
110 mV to 470 mV and it lowers when load current decreases owing to the combined control loop. Voltage ripple can be reduced at each load and the minimum output voltage ripple is 3 mV from a 40 mA load current because of the advantage of ripple suppression.

Efficiency curves across the entire load range for DC-DC converter, LDO and the hybrid system of conventional fixed dropout architecture and proposed adaptive dropout architecture are depicted in Fig. 9. The DC-DC efficiency is almost the same in conventional architecture and proposed architecture. The LDO’s efficiency of conventional one (green dotted line) is almost fixed over the whole loading condition whereas the LDO’s efficiency of proposed one (green solid line) increases with the decrease of load current for the reduction of dropout voltage. Consequently, the overall efficiency of hybrid system with adaptive dropout architecture...
increases with the decrease of load current and is improved by 15.6% at 30 mA light load compared with conventional fixed dropout architecture.

5.2 Performance comparison

The performance comparison of this proposed design with prior DC-DC converter + LDO hybrid systems [2, 4, 7, 9] is listed in Table I. LDO’s dropout voltage in the designs [2, 4] is constant across the entire load range whereas dropout voltage in the designs [7, 9] is adaptive to load current as this work using other methods. Although designs [7, 9] can also adjust LDO’s dropout voltage dynamically corresponding to load current and improve overall efficiency at light load, they both need a duplicated transistor and a current sensing circuit to sense the load current, which will increase the complexity of circuits, chip area and power loss. By contrast, this proposed hybrid system doesn’t need any auxiliary current sensing

![Efficiency for DC-DC converter, LDO and the hybrid system of conventional and improved one](image)

**Fig. 9.** Efficiency for DC-DC converter, LDO and the hybrid system of conventional and improved one

| Table I. Comparison with prior cascaded DC-DC converter and LDO |
|-------------|-------------|-------------|-------------|-------------|-------------|
| Process     | [2] 2010    | [4] 2016    | [7] 2016    | [9] 2014    | This work   |
| Topology    | Buck+LDO   | CP+LDO      | Buck+LDO   | Buck+LDO   | Buck+LDO   |
| $V_{out}$   | 3.3 V      | 1 V         | 3.7 V      | 1.8 V      | 1.2 V      |
| $I_{load}$  | 100 mA     | 30 mA       | 300 mA     | 200 mA     | 100 mA     |
| L or C      | 80 µH      | 0.54 nF     | NA         | 4.7 µH     | 4.7 µH     |
| $C_{dcdc}/C_{LDO}$ | 10 µF/NA | -/0.26 nF   | NA         | 4.7 µF/<100 pF | 10 µF/4.7 µF |
| $f_{sw}$    | 500 kHz    | 90 MHz      | NA         | NA         | 1 MHz      |
| Dropout voltage (mV) | Constant 300 | Constant 50 | Adaptive 150–400 | Adaptive 50–400 | Adaptive 110–470 |
| $\eta_{dcdc}$ | 87.01%     | 80.3%       | 87.0%      | 91%        | 90.61%     |
| $\eta_{dcdc+LDO}$ | 79.6%     | 76.2%       | 79.1%      | 72%        | 65.74%     |
| $V_{out}$ Ripple | 50 mV     | 2 mV        | NA         | 5 mV       | 3 mV       |
circuit. For designs [2, 7, 9], the output voltage is higher than this work so that the LDO’s efficiency is theoretically high. For design [4], the full load range is only 30 mA so that its dropout voltage can be as low as 50 mV to increase efficiency. Consequently, this work effectively reduces the output voltage ripple down to the level that is comparable to or even superior than the prior designs while maintaining a comparable high and load-adaptive overall efficiency.

6 Conclusion

This paper proposes a hybrid system of LDO regulated DC-DC converter with small voltage ripple and adaptive dropout voltage corresponding to load current. The DC-DC converter in proposed hybrid system takes the gate of LDO’s power transistor as the feedback point to embed LDO in the control loop of DC-DC converter, so that the combined control loop can dynamically adjust LDO’s dropout voltage based on load current. Consequently, the almost ripple-free output voltage and improved overall efficiency especially at light load can be obtained simultaneously. Measurement results demonstrate that the output voltage ripple is suppressed to 3 mV at a load of 40 mA and the overall efficiency is improved by 15.6% compared with conventional fixed dropout architecture in light load.

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