Novel single-armed modular multilevel converter for reducing total converter capacitance

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Abstract
During normal operation of a conventional Modular Multilevel Converter (MMC), half of its capacitors remain bypassed at any time instant, increasing the total required capacitance for converter operation, and in turn leading to a larger size and volume MMC for a target capacitor voltage ripple limit. This paper presents a novel MMC topology that utilizes all converter capacitors at all times during the operation. Therefore, the total required capacitance for generating a voltage waveform with the same number of levels and the same target capacitor voltage ripple limit is greatly reduced compared to conventional MMCs. The new topology inherits all the desirable features of conventional MMCs such as modularity, reliability, and scalability, and is compatible with many of the previously proposed control techniques for conventional MMCs. The process of synthesizing the proposed MMC topology and a new voltage balancing scheme as well as the dynamic model and capacitor sizing procedure for the proposed MMC are reported in the paper. Furthermore, experimental results are presented to evaluate the performance of the proposed converter.

1 | INTRODUCTION

Multilevel converters are a prominent family of power-conversion topologies. Cascaded multilevel converters [1], flying capacitor converters [2], neutral point clamped converters [3], and Modular Multilevel Converters (MMCs) [4] are the most popular type of multilevel converters. MMCs are the current state-of-the-art multilevel converters used for medium to high-power applications [5]. MMCs benefit from features such as relying on a single DC bus, staircase AC output voltage with improved THD, modularity, and scalability, making them suitable for high voltage and high power applications such as High Voltage Direct Current (HVDC) power transmission, renewable energy generation, and electric motor drives [6].

MMCs comprise several Sub-Modules (SMs), each constructed using a number of power switches and a floating capacitor. In the current designs, SMs’ size and mass is largely governed by their large capacitors [7–9], which are in turn essential for reducing SMs’ voltage ripples [10, 11]. Hence, reducing the required capacitance has become a challenge, in pursuit of minimizing the overall physical dimensions and weight of the SMs [7]. To that end, numerous studies have been conducted. These efforts can be categorized in: (a) reducing capacitor voltage ripples using new control methods and innovative voltage balancing algorithms, and (b) modifying the MMC topology.

The works in the first category employ advanced control methods and new voltage balancing algorithms to dampen the capacitor voltage fluctuations. One of the prominent works in this category proposed a control method which imposes current harmonics to the circulating currents to minimize the voltage ripples and limit the circulating currents [12]. The performance of this method was later analyzed when the MMC is connected to an unbalanced grid [13]. Another notable work injects a common-mode voltage to the ac-side voltage and a circulating current in the phase-legs of the MMC [14] to suppress the low-frequency capacitor voltage fluctuations. Similarly, a new control scheme is proposed in [15] that reduces the total required capacitance for a full-bridge SM based MMC used in an HVDC transmission system by an energy storage optimization capacitance design method. In the second category, new topologies, that require less total capacitance for generating same output voltages, are proposed. In [10], the traditional
MMC is modified by employing a middle module in each phase with the aim of reducing the number of modules without changing the produced voltage levels. This topology was further modified in [11] by connecting the capacitors of the top and bottom SMs using two accessorial cables to reduce second-order capacitor voltage ripples by 14%. Furthermore, in [16] a double-submodule circuit for SMs was introduced to improve the capacitor voltage balancing at low switching frequencies. This method resulted in 18% reduction of the peak-to-peak capacitor voltage ripples. A new MMC topology with modified SMs was also introduced in [7], where the stacked switched capacitor architecture was utilized for reducing the total capacitance by 40% while the total number of switches was tripled. In [17], a new MMC based inverter was proposed that could produce the same levels of output voltages with reduced number of SM capacitors. This was done by introduction of an extra middle arm to the conventional MMC and four medium-voltage low-frequency switches. Recently, an active power decoupling method for MMCs was introduced in [18] that equips the SM with a buck-type filter which absorbs the low-frequency ripples. This technique can significantly reduce the overall required capacitance depending on the SM voltage ripples. The capacitance reduction however comes with the cost of doubling the total number of the MMC switches and adding an inductor to each SM that is required by the local active power controller.

One crucial issue overlooked by both hardware-based and software-based approaches in the literature is related to the fact that MMCs utilize only half of their capacitors for power conversion process at any time instant during the operation. This increases the required total capacitance for MMCs greatly and unnecessarily. Therefore, the motivation of this work is that devising hardware or software-based methods for MMCs that can engage more capacitors in the power conversion process at any time instant can potentially lead to reducing the required total capacitance of MMCs. Accordingly, this work proposes a novel MMC topology that always utilizes all converter capacitors during the operation. The proposed MMC topology is called a Single-Arm MMC (SAMMC), due to merging of two the arms of the conventional MMCs for synthesizing the new topology.

The proposed SAMMC utilizes all of the SM capacitors at all time instants that consequently eliminates half of the capacitors. This will lead to a substantial reduction in size and volume of the converter. Furthermore, as discussed in Section 4, the voltage and current equations for each arm of the proposed SAMMC will turn out to be very similar to that of a conventional MMC. Therefore, aside from a more involved voltage balancing scheme, advantageously, several previously developed control methods for \(N+1\) modulation scheme in the literature for conventional MMCs are applicable to the proposed SAMMC with minimal effort. Additionally, based on the provided discussion in Section 5 for the capacitor sizing of the SAMMC, it will be demonstrated that for a given number of AC voltage levels and desirable capacitor voltage ripple percentage, the SAMMC SMs require up to 52% the capacitance of the SMs in a conventional MMC. Given that the number of the capacitors is also reduced by half, the total capacitance required by SAMMC is cut to 26% of a conventional MMC. Since the size of SM is mainly determined by size of its capacitors, the proposed topology significantly improves the overall size and weight of the converter. This makes SAMMC suitable for low-voltage and medium-voltage converters that require compact packaging such as space and avionics applications.

To the best of authors’ knowledge, the only family of multi-level converters proposed in the literature with a single arm and a single DC source are the flying capacitor multilevel converters [19–22], which rely on the stacked multilevel converter (SMC) topology. SMCs, however, do not offer many of the advantages of the proposed SAMMC such as modularity and uniform capacitor voltage levels. Furthermore, although the concept of four-terminal SMs for MMCs has been previously explored in the literature to some extent [23–31], none of the proposed SM topologies offer the capability of switching the cells’ capacitors between the two branches (arms in conventional MMC).

The remainder of the paper is organized as follows: The synthesizing procedure and topology of SAMMC is explained in Section 2. The switching states of the SAMMC and its proposed voltage balancing scheme is provided in Section 3. The dynamic model of SAMMC is derived in Section 4. The capacitor sizing procedure and comparison of total required capacitance to conventional MMC is reported in Section 5. The experimental results from a prototype SAMMC are provided in Section 6 to verify the theoretical outcomes, followed by the conclusions in Section 7.

## 2 | PROPOSED SINGLE-ARMED MMC TOPOLOGY

One downside of conventional MMC-based multilevel topologies is the large ratio of number of required SMs to the number of realizable voltage levels. In general, conventional MMC-based topologies require \(2N\) SMs for generating \(N+1\) voltage levels. For example, a conventional MMC with eight cells per leg can only generate a five-level output voltage. In this case, the upper arm and lower arm of MMC each consist of four SMs. Assuming the dc-link voltage is 4 p.u. and the capacitor voltages are set to 1 p.u. each, then the possible output voltage levels are \(-2\), \(-1\), 0, +1, and 2 p.u. For generating \(-2\) p.u. level, all the SMs in the lower arm are bypassed while all the SMs in the upper arm are inserted into the circuit. For generating \(-1\) p.u. level, one SM in the lower arm and three SMs of the upper arm are inserted (remaining SMs are bypassed). For generating 0 p.u. level, two SMs of the lower arm and two of the upper arm are inserted. To generate \(+1\) p.u. level, three SMs of the lower arm and one SM of the upper arm are inserted, and finally to generate \(+2\) p.u. level, all four SMs in the lower arm are inserted while all SMs in upper arm are bypassed. Therefore, for generating any voltage level, a conventional MMC always inserts and thus utilizes only half of its SMs at any time instant. In other words, at any instance during the operation, half of the SM capacitors in a conventional MMC are not engaged in the power conversion process. This work addresses this issue by introducing a new MMC topology that makes use of the entire capacitance of the
MMC can insert SM capacitors in either the upper arm or the lower arm of the MMC at any moment during the operation. Therefore, unlike the conventional MMC, using the proposed topology SM capacitors are not physically hard wired to either an upper arm or a lower arm of a leg the converter; rather, their place in the circuit can be switched between the two arms based on the output voltage level and the voltage balancing scheme.

Figure 1a illustrates one leg of a conventional MMC with four SMs in each arm while the SMs of the lower arm are folded over their AC side terminals in order to bring together the upper and lower arm capacitors and match their voltage polarities. Subsequently, each pair of SMs facing each other can be fused at their capacitor terminals, resulting in one leg of the proposed MMC topology, with four new four-terminal SMs as shown in Figure 1b. The new four-terminal SMs only use one capacitor each, but require two additional switches, for example, \( S_{a13} \) and \( S_{a14} \) in Figure 1b. Therefore, each leg of the proposed topology comprises four SMs and four capacitors. Since the two arms of the conventional MMC are merged to devise the new proposed topology, this topology is called a Single-Arm MMC (SAMMC) hereinafter. As depicted in Figure 1b, each leg of the proposed SAMMMC comprises two branches, that is, the upper branch and the lower branch, rather than two arms as is the case for a conventional MMC. The proposed SAMMMC topology can insert any of its capacitors in either branches at
any time instant during the operation, thus enabling continuous engagement of all capacitors in power conversion process. As a result, for generating a given number of voltage levels, SAMMC requires half the number of SMs and capacitors needed by conventional MMC. A complete three-phase SAMMC is illustrated in Figure 2. The $L_{ac}$ and $R_{ac}$ in this figure are line inductance and resistance, respectively; $R_o$ is equivalent internal resistance of each branch; and $L_o$ is the inductance of each branch.

### 3 | OPERATION AND VOLTAGE BALANCING

#### 3.1 | Switching states of SAMMC topology

As illustrated in Figure 1b, each SM in each phase’s arm of SAMMC comprises six power switches and one capacitor. As mentioned before, to enable capacitor sharing in SAMMC, each SM can insert its capacitor in either the upper branch or the lower branch of the arm. Therefore, two modes of operation for SMs are defined, referred to as the “upper mode” and the “lower mode” hereinafter. In the upper mode, the SM inserts its capacitor in the upper branch and bypasses the lower branch, while in the lower mode, the SM inserts its capacitor in the lower branch and bypasses the upper branch. The status of conduction of the switches of an SM for realizing the lower and upper modes for positive and negative directions of the conducted currents and SM voltages are shown in Figure 3. As pictured, the switches $S_{j11}$, $S_{j23}$, $S_{j5}$ are always turned ON and OFF simultaneously and complementary to $S_{j22}$, $S_{j4}$, $S_{j6}$ which are also turned ON and OFF simultaneously. Each switch is represented as $S_{jk}$ where $i \in \{1, 2, ..., n\}$ is the index of SMs in each arm with $n$ being the total number of SMs in each phase, $j = \{a, b, c\}$ is the index of phases of SAMMC, and $k \in \{1, 2, ..., 6\}$ is the index of switch number in each SM. The direction of the branch currents $i_{ja}$ and $i_{jb}$ passing through the SMs in each mode can be positive or negative because at any moment the ON switches or their antiparallel diodes can conduct the current. The upper and lower voltages of the SMs in each mode, $v_{ua}$ and $v_{ub}$, as a function of the capacitor voltage are depicted in this figure as well.

Redundant switching schemes available in conventional MMC can be used for voltage balancing of SM capacitors [38]. According to Figures 3 and 4, various combinations of SMs in an upper mode or a lower mode can be used to realize different voltage levels at each phase of SAMMC. $n_{aj}$ and $n_{bj}$ are defined as the number of inserted SMs in the upper and lower branch of phase $j$, respectively. Some voltage levels can be generated using more than one switching combination, providing redundant switching capacity for the SAMMC operation. Table 1, as an instance, tabulates the status of conduction of switches and mode of operation of each SM of five-level SAMMC for generation of each voltage level. The mode of operation of each SM in Table 1 is denoted as U/L, where U/L represents the SM to be inserted in upper/lower branch. It must be noted that since in each SM the conduction state of the switches $S_{j11}$ and $S_{j5}$ are the same as $S_{j1}$, and the conduction states of the switches $S_{j22}$, $S_{j4}$, and $S_{j6}$ are complimentary to $S_{j1}$, in Table 1, the voltage levels are listed only as a function of status of conduction of $S_{j1}$ for the sake of brevity. A “0” in this table indicates an OFF switch while a “1” indicates an ON switch. The status of conduction of the SAAMC switches are denoted as,

$$S_{jk} = \begin{cases} 
1 & \text{Switch is ON} \\
0 & \text{Switch is OFF} 
\end{cases} \quad (1)$$

In this table, it is assumed that all capacitor voltages are regulated to their target voltage of $V_{dc}/4$, and the output voltage $V_o$ is referenced to the imaginary point “O” at the midpoint of the source dc voltage as shown in Figure 1b. Table 1 also demonstrates the redundant switching states for generating a specific voltage level. Voltage levels of $-V_{dc}/4$ and $V_{dc}/4$ can
be realized using four combinations of switching states, while voltage level 0 can be realized using six combinations of switching states. As explained below, the redundant switching states will be utilized for implementing the voltage balancing scheme. The conduction path of one leg of SAMMC for generation of $-V_{DC}/4$ voltage level is illustrated in Figure 5 as an example. The switching states employed in Figure 5 are from the second row of Table 1. It can be seen that capacitors of SMs 1 to 3 are inserted into the upper branch of SAMMC, while the capacitor of SM 4 is inserted into the lower branch.
TABLE 1  Switching states of SAMMC for generating different voltage levels

| $n_{ua}$ | $n_{lb}$ | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $V_d$ |
|----------|----------|----------|----------|----------|----------|-------|
| 4        | 0        | 1        | 1        | 1        | 1        | $-\frac{V_{dc}}{2}$ |
| 3        | 1        | 1        | 1        | 0        | L        | $-\frac{V_{dc}}{4}$ |
| 3        | 1        | 1        | 1        | 0        | L        | 1        |
| 3        | 1        | 1        | 0        | L        | 1        | 1        |
| 3        | 0        | 1        | 1        | 1        | 1        | 1        |
| 2        | 2        | 0        | 0        | L        | 1        | 1        |
| 2        | 2        | 0        | 1        | 0        | L        | 1        |
| 2        | 2        | 1        | 0        | L        | 1        | 1        |
| 2        | 2        | 1        | 0        | L        | 0        | L        |
| 1        | 3        | 0        | L        | 0        | L        | 1        |
| 1        | 3        | 0        | L        | 0        | L        | 0        |
| 1        | 3        | 0        | L        | 1        | U        | 0        |
| 1        | 3        | 1        | U        | 0        | L        | 0        |
| 0        | 4        | 0        | L        | 0        | L        | 0        |

3.2 Proposed voltage balancing scheme

MMCs require a voltage balancing scheme to regulate and balance their capacitor voltages [6]. In case of the proposed SAMMC, at any time instant, each capacitor is inserted either in a lower branch or an upper branch of a leg. Capacitor voltages need to be regulated to their nominal level after the converter control system determines the number of SMs that need to be inserted into upper/lower branches. To achieve this goal, illustrated in Figure 6, a new voltage balancing is proposed for the SAMMC topology.

Generating each voltage level requires $n_{ua}$ number of SMs in an SAMMC leg to be in the upper mode while the remaining $n_{lj}$ SMs are in the lower mode ($n = n_{ua} + n_{lj}$ is the total number of SMs in one leg). Due to switching redundancies illustrated in Table 1, however, there is a high degree of flexibility for choosing which $n_{ua}$ SMs specifically to command to the upper mode (the remaining $n_{lj}$ SMs will be commanded to lower mode). This degree of flexibility is used to implement the voltage balancing scheme. The proposed voltage balancing scheme uses the information about the polarity of upper and lower branch currents, that is, $i_{ua}$ and $i_{lj}$, and the voltage of each SM capacitor to decide on which SMs to put on upper/lower modes. According to Figures 3b and 4a, in case $i_{ua}$ is positive and $i_{lj}$ is negative, inserting an SM capacitor in the upper branch will charge that capacitor and increase its voltage (Figure 3b), while inserting a SM capacitor in the lower branch will discharge the capacitor and decrease its voltage (Figure 4a).

Therefore, the voltage balancing scheme will choose the $n_{ua}$ SMs with the lowest capacitor voltages and commands them to an upper mode to increase their capacitor voltages, while the remaining $n_{lj}$ SMs will be inserted in the lower branch to decrease their capacitor voltages. Similarly, if $i_{ua}$ is negative and $i_{lj}$ is positive as in Figures 3c and 4c, inserting an SM capacitor in the upper/lower arm will decrease/increase the capacitor voltage. Therefore, $n_{ua}$ SMs with highest capacitor voltages will be inserted in the upper branch, and the rest will be inserted in the lower branch. If both $i_{ua}$ and $i_{lj}$ are positive, however, as in Figures 3a and 4a, regardless of which branch they are inserted into, SM capacitor voltages will increase. In this case, the voltage balancing scheme will try to charge the SM capacitors with the highest voltages with the smaller branch current and charge SMs with the lowest voltage levels with the larger branch current. Therefore, in this case, if $i_{ua}$ is larger than $i_{lj}$, then $n_{ua}$ SMs with highest capacitor voltages will be inserted in the upper branch, while if $i_{ua}$ is smaller than $i_{lj}$ then $n_{ua}$ SMs with lowest capacitor voltages will be inserted in the upper branch (the remaining capacitors will be inserted in the lower branch). Similarly, if both $i_{ua}$ and $i_{lj}$ are negative as in Figures 3d and 4d, capacitor voltages will decrease regardless of which branch they are inserted into. Therefore, if $i_{ua}$ is larger/less than $i_{lj}$, then $n_{ua}$ SMs with highest/lowest capacitor voltages will be inserted in upper branch, and the rest will be inserted in the lower branch.
According to Figure 1b, Kirchhoff’s Voltage Law (KVL) can be used to formulate the voltages of the lower and upper branches ($V_{uj}$ and $V_{lj}$ respectively) of each phase $j$ as,

$$V_{uj} = \sum_{i=1}^{n} (S_{ji} S_{ji} S_{ji} S_{ji}) V_{Cji},$$  

(2)

$$V_{lj} = \sum_{i=1}^{n} (S_{ji} S_{ji} S_{ji} S_{ji}) V_{Cji},$$  

(3)

where $V_{Cji}$ is the voltage of the capacitor of the $j^{th}$ SM ($SM_{ji}$).

The equivalent circuit of phase $a$ of SAMMC is shown in Figure 7, where node $O$ is the virtual DC-side ground point. The branch currents of SAMMC ($i_o$ and $i_l$ in Figure 7 for phase $a$) consist of half of the AC-side current ($i_a$) and the entire circulating current for phase $a$ ($i_{cij}$). Similarly for the three phases, the currents of upper ($i_{u_j}$) and lower ($i_{l_j}$) branches of SAMMC in Figure 1b can be written as

$$i_{u_j} = i_{cij} + \frac{1}{2} i_j,$$  

(4)

$$i_{l_j} = i_{cij} - \frac{1}{2} i_j,$$  

(5)

where $i_j$ is the AC-side current obtained using Kirchhoff’s Current Law (KCL) at connection terminal of SAMMC and AC grid,

$$i_j = i_{uj} - i_{lj},$$  

(6)

The circulating current can be found by summing (4) and (5) as,

$$i_{cij} = \frac{1}{2} (i_{uj} + i_{lj}).$$  

(7)

The terminal voltages of the SAMMC can be found using KVL in the upper and lower branches of each phase $j$ in Figure 2,

$$v_{uj} = \frac{V_d}{2} - v_{uj} - R_{oiuj} - L_o \frac{dv_{uj}}{dt},$$  

(11)

$$v_{lj} = \frac{V_d}{2} + v_{lj} + R_{oiuj} + L_o \frac{dv_{lj}}{dt},$$  

(12)

respectively. By summing (11) and (12), the output voltage of phase $j$ is found as,

$$v_{lj} = \frac{1}{2} \left[ (v_{lj} - v_{uj}) - R_{ojj} - L_o \frac{dv_{lj}}{dt} \right].$$  

(13)

Using KVL for the lower and upper branches of each phase in Figure 2, while denoting the grid voltage of each phase as $v_{fj}$,
the dynamic model of each SAMMC arm can be formulated:

$$\frac{V_{dc}}{2} - v_{uj} - v_{fj} = L_o \frac{di_{uj}}{dt} + R_o i_{uj} + I_{ac} \frac{di_j}{dt} + R_{ac} i_j, \quad (14)$$

$$\frac{V_{dc}}{2} - v_{lj} + v_{fj} = L_o \frac{di_{lj}}{dt} + R_o i_{lj} - I_{ac} \frac{di_j}{dt} - R_{ac} i_j. \quad (15)$$

Subtracting (14) from (15), and substituting $i_{uj}$ and $i_{lj}$ from (4) and (5), yields the AC-side current dynamic equation,

$$\frac{di_j}{dt} = -R_o + \frac{2R_{ac} L_o}{I_o + 2I_{ac}} - \frac{2v_{fj}}{I_o + 2I_{ac}}. \quad (16)$$

Summing (15) and (14), and substituting $i_{uj} + i_{lj}$ from (4) and (5), the internal circulating current dynamic equations for each SAMMC branch can be found,

$$\frac{di_{circj}}{dt} = -R_o \frac{V_{dc}}{I_o} + \frac{V_{dc}}{2I_o} - \frac{v_{uj} + v_{lj}}{2I_{ac}}. \quad (17)$$

### 4.1 Simulation result with change in the load

It must be noted that the voltage balancing algorithm is independent of the nature of the load. To investigate this, four different cases of (1) SAMMC feeding pure resistive load, (2) SAMMC feeding pure inductive load, (3) SAMMC feeding resistive-inductive load, (4) step change in load had been investigated. The output voltage, output current, and SM capacitor voltages are recorded at each scenario. In all scenarios, it is assumed that the dc link voltage is 1 kV, and there are four SMs per phase in SAMMC. The reference voltage of the SM capacitors then equals to 250 V. It had been seen that the SM capacitors will follow the reference voltage at each scenario, which proves the effectiveness of proposed voltage balancing algorithm. Due to the page length concern, only the case number 4 with step change in load is shown in Figure 8. Initially, the SAMMC is feeding a resistive-inductive load ($R-L = 10 \Omega - 20 mH$). At $t=0.6$ a step change in load is applied where another 10 $\Omega - 20 mH$ load is paralleled to the existing load. Hence the load will be changed from 10 $\Omega - 20 mH$ to 5 $\Omega - 10 mH$. It can be seen from Figure 8 that output current is doubled and voltage ripple of the SMs capacitors have increased.

### 5 CAPACITOR SIZING

The fundamental harmonic component of the SAMMC output voltage and current can be expressed as,

$$v_{1j} = v_{m1j} \cos \omega t, \quad (18)$$

$$i_{1j} = i_{m1j} \cos(\omega t + \varphi_0), \quad (19)$$

where $v_{m1j}$ and $i_{m1j}$ are the amplitude of fundamental components of voltage and current for phase $j$, respectively; $\varphi_0$ is phase displacement between fundamental harmonic component of the SAMMC output voltage and current; and $\omega$ is the angular frequency. Using KVL in the upper and lower branches of each phase of SAMMC yields

$$v_{ij} = \frac{V_{dc}}{2} - v_{fj}, \quad (20)$$

$$v_{ij} = -\frac{V_{dc}}{2} + v_{uj}. \quad (21)$$

Rearranging (21) and (21) and substituting (18), (19) yields

$$\begin{align*}
v_{11j} &= \frac{V_{dc}}{2} - v_{11j} = \frac{V_{dc}}{2} \left(1 - m \cos \omega t\right), \\
v_{11j} &= \frac{V_{dc}}{2} + v_{11j} = \frac{V_{dc}}{2} \left(1 + m \cos \omega t\right),
\end{align*} \quad (22)$$

where modulation index ($m$) is defined as [32],

$$m = \frac{v_{m1j}}{V_{dc} / 2} = \frac{2v_{m1j}}{V_{dc}} \quad 0 \leq m \leq 1. \quad (23)$$

The current coefficient $k$ is also defined as,

$$k = \frac{3}{2} \frac{i_{m1j}}{I_{dc}} \leq k. \quad (24)$$
Using this terminology, the power delivered by the left and right branches can be formulated as

\[ P_{ij} = v_{ij} \times i_{ij} = \frac{V_{dc}}{2} (1 - m \cos \omega t) \times \frac{i_{dc}}{3} \left[ 1 + k \cos (\omega t + \varphi) \right] \]
\[ = \frac{P_{dc}}{6} \left[ k \cos (\omega t + \varphi) - m \cos \omega t + \frac{mk}{2} \sin (2\omega t + \varphi) \right], \tag{25} \]

\[ P_{rj} = r_{rj} \times i_{rj} = \frac{V_{dc}}{2} (1 + m \cos \omega t) \times \frac{i_{dc}}{3} \left[ 1 - k \cos (\omega t + \varphi) \right] \]
\[ = \frac{P_{dc}}{6} \left[ -k \cos (\omega t + \varphi) + m \cos \omega t + \frac{mk}{2} \sin (2\omega t + \varphi) \right], \tag{26} \]

where \( P_{dc} = i_{dc} V_{dc} \) is the power delivered by the DC source.

The size of SM capacitors is directly proportional to the energy fluctuations in SAMMC [34]. First, the SAMMC delivered apparent power as \( S \) with considering phase of \( \varphi_0 \). Also, the maximum energy fluctuation is obtained by choosing \( n = 1 \). So, by considering phase inside from power of the DC branch that is injected to phase and power of AC that delivered from each phase, the instantaneous power of each phase, \( P_{\varphi,j} \), can be written as:

\[ P_{\varphi,j} = P_{dc} - P_{ac} = P_{dc} - \frac{\sqrt{2}}{2} V_{dc} \cos(\omega t + \varphi_0) \cos(\omega t) \]
\[ = \frac{1}{3} |S| \cos(\varphi_0) - \frac{\sqrt{2}}{2} |V_{dc}| \cos(\omega t + \varphi_0) \cos(\omega t). \]
\[ = |S| \left[ \frac{1}{3} \cos(\varphi_0) - \frac{\sqrt{2}}{2} \cos(\omega t + \varphi_0) \cos(\omega t) \right] \tag{27} \]

Then, the maximum energy fluctuation of each phase is

\[ \Delta E_{\varphi,j} = \int_{t_a}^{t_b} P_{\varphi,j} dt, \tag{28} \]

where \( t_a \) and \( t_b \) are the roots of (27) calculated as in (29) for \( \varphi > 0 \) and in (30) for \( \varphi > 0 \):

\[
\begin{align*}
 t_a &= \frac{1}{\omega} \arccos \left( \frac{\sin(\varphi)}{\sqrt{6}} \right) \sqrt{2 \cot(\varphi) + 3 + \sqrt{-2 + 6 \sqrt{2} \cot^2(\varphi) + 9}} \\
 t_b &= \frac{1}{\omega} \arccos \left( -\frac{\sin(\varphi)}{\sqrt{6}} \right) \sqrt{2 \cot^2(\varphi) + 3 - \sqrt{-2 + 6 \sqrt{2} \cot^2(\varphi) + 9}} \\
 t_a &= -\frac{1}{\omega} \arccos \left( \frac{\sin(\varphi)}{\sqrt{6}} \right) \sqrt{2 \cot(\varphi) + 3 + \sqrt{-2 + 6 \sqrt{2} \cot^2(\varphi) + 9}} \\
 t_b &= -\frac{1}{\omega} \arccos \left( -\frac{\sin(\varphi)}{\sqrt{6}} \right) \sqrt{2 \cot^2(\varphi) + 3 - \sqrt{-2 + 6 \sqrt{2} \cot^2(\varphi) + 9}} . \tag{29} \end{align*}
\]

Then, the maximum energy variation of each phase is:

\[ \Delta E_{\varphi,j} = |S| \left( \frac{4 - 6 \sqrt{2}}{12 \omega} \cos(\varphi) \omega t - 3 \sqrt{2} \sin(2\omega t + \varphi) \right)_{t_a}^{t_b}, \tag{31} \]

By considering \( n \) SM in each phase of SAMMC, the average of maximum energy fluctuation in each SM is:

\[ \Delta E_{SM} = \frac{1}{n} \Delta E_{\varphi,j}. \tag{32} \]

For each SM we have:

\[ E_{SM} = \frac{1}{2} C_{SM} V_{SM}^2 \omega \Delta v, \tag{33} \]

Hence, the maximum capacitor value of each SM of SAMMC is obtained in

\[ C_{SM} = \frac{2 \Delta E_{\varphi,j}}{n V_{SM}^2 \omega \Delta v} = \frac{|S|}{6 \omega n V_{SM}^2 \Delta v} \]
\[ \times \left( (4 - 6 \sqrt{2}) \cos(\varphi) \omega t - 3 \sqrt{2} \sin(2\omega t + \varphi) \right)_{t_a}^{t_b}, \tag{34} \]

where \( V_{SM} \) is the mean value of capacitor voltage, and \( \Delta v \) is voltage ripple percentage of the capacitors. In a similar scenario, the capacitor of MMC is calculated in the literature [33, 34] as:

\[ C_{MMC} = \frac{|S|}{3 \pi \omega n V_{MMC}^2 \Delta v} \left( 1 - \left( \frac{\cos(\varphi)}{2} \right)^2 \right)^{3/2} . \tag{35} \]

The total capacitance of SAMMC ratio to the MMC is \( n C_{SM} \ MMC / 2 \pi n C_{MMC} \ MMC \) shown in Figure 9. As the figure shows, the SAMMC total capacitance is reduced up to 26% that of the MMC.
EXPERIMENTAL RESULTS

To investigate the operation of the proposed SAMMC and validate the effectiveness of the discussed voltage balancing scheme, a laboratory-built prototype SAMMC is utilized. The experimental setup is shown in Figure 10a. As pictured, the prototype SAMMC comprises four SMs in each phase. A DC voltage source is connected to DC side of the SAMMC and the AC side is connected to the three-phase grid through AC line inductors. The overall control system for this converter is shown in Figure 10b. The SAMMC delivered active and reactive power is controlled via regulating its output currents. In the controller block, two PI controllers are employed for regulating $d$ and $q$ currents to control output active and reactive power [35]. A Phase-Locked Loop (PLL) is utilized to synchronize SAMMC output currents with the grid. The Pulse Width Modulation (PWM) block compares reference signals with carrier waves and decides on the number of capacitors to be inserted in the upper and lower branches of each SAMMC leg, that is, $n_{uj}$ and $n_{lj}$. Among the several PWM techniques for multilevel converters [36], this work utilizes Phase Disposition-based PWM (PD-PWM) method [37]. The capacitor voltage balancing block decides which capacitors should be inserted in the upper or lower branches.

The SAMMC control is performed in the reference frame rotating synchronously with the grid voltage. The reference active power and reactive power can be formulated as,

$$P_{ref} = \frac{3}{2} u_d i_d,$$

$$Q_{ref} = \frac{3}{2} u_q i_q.$$

The detailed control system is shown in Figure 10c. The output of the controller block will be the three-phase voltage references. These three-phase voltage references are then fed to the PWM block.

Phase-disposition PWM has been used in this paper. The three-phase voltage references are normalized between 0 and 1 before being compared with carrier signals. Figure 10d shows the voltage reference of phase “a” as an example. Since four SMs are used in each phase in the results section, four carriers are used. By comparing the reference signals with carrier signals, the number of inserted capacitors in the upper branch ($n_{uj}$) and lower branch ($n_{lj}$) is found. $n_{uj}/n_{lj}$ is the output of the PWM block which will be fed and used in “Capacitor voltage balancing

| System parameters                  | Values  |
|-----------------------------------|---------|
| DC link voltage                   | 400 V   |
| Grid frequency                    | 60 Hz   |
| Capacitor of SM                   | 1.2 mF  |
| Number of SMs per phase           | 4.0     |
| Branch inductance                 | 1.0 mH  |
| Branch resistance                 | 0.2 Ω   |
| AC line inductance                | 4 mH    |
| AC line resistance                | 1.0 Ω   |
| Grid voltage (RMS)                | 110 V   |
| Carrier frequency                 | 2.0 kHz |

FIGURE 9 Comparing SAMMC and MMC total capacitance

FIGURE 10 The experimental setup and the controller: (a) The experimental setup for verification of results, (b) Overall SAMMC controller; (c) Detailed “controller” block; (d) Phase-disposition with four carriers

TABLE 2 Circuit parameters of experiment
algorithm” block as shown in Figure 5. The control system is implemented using a digital signal processor (DSP) from Texas Instruments (TMS320F28379D). A Phase-Locked Loop (PLL) algorithm is implemented for synchronization of inverter voltages with the grid voltage. The SAMMC and grid parameters for the experiments are given in Table 2. The sampling time for the controller is set to $500\mu s$. Three experiments are conducted to investigate the steady-state operation and dynamic behaviour of the SAMMC, while using the proposed control system. The first experiment evaluates the steady state operation of SAMMC while injecting 2000 W active power at unity power factor into the grid. Figures 11 and 12 illustrates the experimental waveforms of SAMMC in this scenario. The measured quantities are

**FIGURE 11** Steady-state operation of SAMMC: (a) Lower and upper branch and inverter phase voltages for phase $a$; (b) the branch and phase currents for phase $a$; (c) three phase inverter voltages

**FIGURE 12** Steady-state operation of SAMMC: (a) AC side currents; (b) injected active and reactive power ($P: 500$ W/div, $Q: 500$ VAR/div, $t: 10$ ms/div); (c) SM capacitor voltages for phase $a$ (the cursor is at 100 V, $V: 2$ V/div, $t: 20$ ms/div)
FIGURE 13 Transient response of SAMMC to an active power reversal command: (a) Lower and upper branch and inverter phase voltages for phase $a$; (b) the branch and phase currents for phase $a$; (c) three phase inverter voltages, the lower and upper branch voltages and currents, the inverter phase voltage and injected current for phase $a$, three phase AC-side inverter voltages and injected currents, and SM capacitor voltages for phase $a$. The active and reactive power are also calculated from measured voltages and currents using MATLAB and are shown in Figure 12. Figure 11a illustrates the SAMMC branch voltages of phase $a$. As pictured, inverter phase $a$ voltages are reaching all the anticipated voltage levels expressed by (14). Figure 11b illustrates the branch and phase currents for phase $a$, verifying (6). Figures 11c and 12a demonstrate generated balanced three phase inverter voltages and currents,
respectively. The calculated Total Harmonic Distortion (THD) of output currents is less than 5%. The control system is successfully maintaining the steady-state operation of the converter at the desired active and reactive power references as shown in Figure 12b. The voltage of SM capacitors for phase \( a \) are shown in Figure 12c, which verifies the effectiveness of proposed voltage balancing method. Regarding the SM capacitors voltages, the voltage reference of the capacitors is equal to link voltage divided by number of SMs in the leg (\( \approx 100 \) V in Figure 12c). It must be noted that the cursor is at 100 V in Figure 12c. The peak-to-peak ripples on capacitor voltage is around 2 V, which is equal to 2% of the reference voltage. This value is usually set below 10% for conventional MMC. The results of this
experiment demonstrate a satisfactory steady state response for the SAMMC and the proposed control system.

The second experiment investigates the transient response of SAMMC while using the proposed control system. A reversal active power step command from 2000 to $-2000$ W is issued to the control system at $t = t_0$, while the reactive power has been maintained at zero. Figure 13a–c is the same as Figure 11. According to Figure 14, the controller can effectively regulate the inverter currents, and thus active power, to the new reference even in the case of such drastic power reversal command. Figure 14a more clearly depicts the inverter current transients during the power reversal. Figure 14c confirms that the voltage balancing algorithm can maintain voltage balance after the power transient.

The third experiment is similar to the previous experiment, but it investigates the system’s response to a reactive power reversal command. For this experiment, the reactive power is commanded to step down from 1000 to $-1000$ Var at $t = t_1$ while maintaining the active power at 1500 W. The results are shown in Figures 15 and 16. Similar to the previous experiment, the results demonstrate an appropriate overshoot, rise time, and transient response by the converter system.

7 CONCLUSION

This paper proposed a novel Single-Armed MMC topology. The main advantage of the proposed SAMMC is the reduction of total required capacitance of the converter in comparison with conventional MMCs in the same operational conditions. The dynamic model and circuit equations for the SAMMC were derived. Due to similarity of the developed model and equations with those of conventional MMC, it was concluded that previously developed control paradigms for conventional MMCs are applicable to the proposed SAMMC. Experimental results were provided to verify the theoretical outcomes.

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