Phasor Based Analysis and Design of Single Phase SRF d-q Controller for Dynamic Voltage Restorer

D. N. Katole1, M.B. Daigavane2
Research Scholar, Dept. of Electrical Engg. 1 Principal2
G.H.R.C.E 1 G.H.R.I.E.T. 2 Hingna, Nagpur
R.T.M. N.U, Nagpur, Maharashtra, India
dn_katole@rediffmail.com1 , mdai@rediffmail.com2

Abstract
This paper proposes an effective control concept for single phase dynamic voltage restorer (DVR) and overall analysis is performed based on the restoration of load voltage without phase change. The proposed controller is based on conventional proportional integral (PI) controller to compensate single phase voltage sag by synchronous reference frame (SRF) theory incorporating d-q concept. A detailed phasor analysis of voltage injection identical to pre-sag compensation strategy has been carried out with the consideration of unlock phase lock loop (PLL) at the sag initiation point and accordingly a controller is designed. The digital simulation has been performed using MATLAB Simulink to prove the effectiveness of the proposed control. The simulation results for linear and nonlinear load shows that this generalized proposed method can compensate single phase voltage sag effectively.

Key words : Power quality, voltage sag, single phase DVR, SRF d-q based phasor controller.

1. Introduction
Most of the power quality (PQ) problems are related to voltage such as voltage sag/swell, distorted supply etc. [1]. Voltage sag is generally considered as the most common and costly PQ problem. Voltage sag is characterized by momentary decrease in rms voltage magnitude lasting between half a cycle and several seconds. It is caused mainly by upstream faults at the feeder connected parallel to common coupling point (PCC). Custom power devices such as dynamic voltage restorer (DVR) plays major role in medium and low power system for power quality improvement [2]. Sags are often nonsymmetrical and accompanied by a phase jump. Most of the three phase control strategies for DVR have been addressed in [2] to [4] which tightly control the terminal voltage, \( V_{L} \) and \( i_{L} \) represents source and load current. During voltage sag, DVR restores the sensitive load by injecting voltage \( V_{inj} \) through coupling transformer. This is initiated by controlling VSI along with DC-link capacitor with capacity \( C_{dc} \) and voltage \( V_{dc} \) with a passive \( \pi \) (\( L_{f} C_{f} L_{f} \)) filter.

This injected voltage depends on magnitude of voltage sag \( V_{inj} \) and power factor of load \( PF_{L} \). The injected active power \( P_{inj} \) is the difference of load and source power given as

\[
P_{inj} = P_{L} - P_{S} = V_{L} I_{L} \cos \theta_{L} - \left( \frac{V_{L}}{V_{s}} \right) \cos \theta_{s}
\]

Where \( \cos \theta_{L} \) and \( \cos \theta_{S} \) are load and supply power factor.

With the consideration of load apparent power and load voltage on per unit base quantities, the injected power can be rewritten as

\[
P_{inj} = P_{L}F_{L} - V_{L} \cos \theta_{L}
\]

This paper mainly concentrates on SRF d-q based controller for single phase system. The controller is based on conventional Proportional integral (PI) with decoupled feed-forward and feedback loop. The successful implementation of DVR for mitigating the voltage sag proves the effectiveness of the controller.

II. DVR Structure and Operation
A typical single -phase DVR consist of H - bridge voltage source inverter (VSI) structure consisting of four switches ( \( S_{1} \) to \( S_{4} \) ) with self-supporting DC link connected in series with single phase transformer as shown in Fig. 1. The system is represented with \( V_{s} \) as a source voltage, \( V_{L} \) as load voltage and \( V_{inj} \) as terminal voltage, \( i_{s} \) and \( i_{L} \) represents source and load current.

Fig. 1 Single Phase Dynamic Voltage Restorer with H-Bridge VSI.
The injected power can be minimized by maintaining unity power factor on supply side.
\[
\cos \theta_s = 1
\]  

The aim of DVR is to maintain load voltage magnitude to its desired value say 1pu despite voltage sag \( V_{\text{sag}} \) at supply end. It gives
\[
V_i = 1 - V_{\text{sag}}
\]

Using (2), (3), and (4) the minimum injected active power can be written as
\[
P_{\text{sag}}^{\text{inj}} = V_{\text{sag}} - (1 - PF_i)
\]

From (5) it is clear that when \( V_{\text{sag}} \leq (1 - PF_i) \), load voltage restoration is possible without active power injection.

Otherwise, it needs the support of active power to restore the load voltage. To handle power quality problems in single phase, several control strategies are available in case of shunt compensation without energy storage device like active power filter [6] but less reported in case of series compensation. The DVR effectively supply reactive power but active power is fulfilled by energy storage device [7]. In general, the active and reactive power flow are controlled by regulating the angle between injected voltage and the line current. The effective solution for maintaining exact magnitude of voltage at load without any phase change, as like a voltage before sag is pre-sag compensation method. This method leads to less distortion at the load side resulting in no transients and circulating currents. Most of the controllers earlier designed, are based on this method where locking of PLL is necessary at sag initiation point. Whereas in this paper a phasor analysis of pre-sag method has been done to obtain the magnitude and angle of injected voltage without locking the PLL. The proposed controller based on this analysis has been discussed below.

**III. Proposed control system**

The complete phasor analysis for the design of controller is based on SRF as shown in Fig. 2. Generation of SRF \( d-q \) component in single phase system needs creation of one fictitious phase which is considered as \( \beta \) phase along with the originally present \( \alpha \) phase as given in [6]. Accordingly this \( \alpha \) and \( \beta \) instantaneous values are transformed into SRF \( d-q \) components [3]. Constant \( d-q \) component in the steady state of system representing dc value, becomes variable in nature due to harmonic contents in nonlinear load. The variable value of \( d-q \) components of voltage can achieve constant value with the application of moving average filter (MAF) [8]. Inverse transformation of this constant \( d-q \) value represents fundamental positive sequence voltage which is necessary for mitigation of sag in nonlinear load. Considering sinusoidal supply voltage in healthy condition, only \( d \)-axis component of voltage \( V_{\text{dpre}} \) is present as illustrated in Fig. 2. At fault instant, voltage drops to \( V_{\text{sag}} \) and the controller injects voltage \( V_{\text{inj}} \) at an angle \( \alpha \). As per the vector diagram, the value of \( V_{\text{inj}} \) and \( \theta_{\text{inj}} \) are obtained as

\[
V_{\text{inj}} = \sqrt{(V_{\text{dpre}} - V_{\text{dsag}})^2 + (V_{\text{qpre}} - V_{\text{qsag}})^2}
\]  

\[
\theta_{\text{inj}} = \text{Arc tan} \left( \frac{V_{\text{qpre}} - V_{\text{qsag}}}{V_{\text{dpre}} - V_{\text{dsag}}} \right)
\]

The phasor controller is based on combined feed-forward and feed-back strategy to obtain better transient and steady state response. The block diagram of the proposed phasor based controller for DVR is shown in Fig. 3. Here, Clarke’s and then park transformation is implemented on single phase where the reference angle \( \theta_{\text{ref}} \) is obtained through single phase phase lock loop (PLL). The fundamental frequency component of load voltage is restored by phasor based Load voltage controller. This controller works on two different loops, one as feed-forward loop for faster transient response and other as feedback loop for zero steady state error. Each of these above mentioned phasor control loop is comprised of magnitude control loop and phase angle control loop. Both these loops are independent of each other and completely decoupled. Here the injected voltage phasor is the complex difference of supply voltage and pre-sag supply voltage phasors. The magnitude of \( V_{\text{inj1}} \) and \( V_{\text{inj2}} \) (the feed forward and feedback voltage phasors) are calculated by subtracting fundamental \( V_{\text{dq}} \) values from actual reference value of supply voltage and load voltage in SRF. Two PI controller are used to eliminate the steady state errors of the magnitude and phase angle of load voltage. The parameters of PI controller are set simply by trial and error method so as to get zero steady state error in dc signal in order to achieve fast response without any overshoot. The outputs of the PI controllers are added to outputs

![Fig. 2 Phasor representation of proposed control strategy for DVR.](image-url)
of feed-forward loop to achieve reference injected voltage phasor. The difference of reference injected voltage and actual injected voltage gives the reference injected voltage signal. SPWM technique has been applied on this injected voltage signal to get the pulses required for operation of voltage source inverter (VSI).

IV. Simulation Results and Discussion

The single phase system considered consists of a source, a bus, and two parallel loads as shown in Fig. 4 for simulation in MATLAB Simulink environment [20]. To verify the performance of aforementioned controller, the LG fault is created in other feeder parallel to sensitive nonlinear load, resulting in voltage sag at PCC. The extensive simulations are performed, results of which are shown in Figs. 5-6 and in Figs. 7-8 for linear and nonlinear load respectively. The parameters under consideration for simulation is given in appendix I. Due to fault the PCC voltage experience sag of 58% from instant 0.05sec to instant 0.30sec which nearly covers up to 12-13 cycles as shown in Fig. 5(a). It can be clearly stated from Fig. 5(b) that the DVR is restoring the load voltage to its desired value without any phase change represented in Fig. 5(c). It is clearly noted that the controller is initiated with approximately one cycle delay because of quarter cycle delay in \( \beta \) component generation. From the overall scenario of results, it can be further stated that the load voltage is tightly restored to its reference value. The DC-link voltage is maintained constant to its reference value given in Fig. 6(a), load current and generation of fundamental \( \alpha \beta \) component of load current from nonlinear current is shown in Fig. 8(c).

For further judgment half bridge diode rectifier is connected across load to make it nonlinear. The Fig. 8(b) indicates the nonlinear nature of load current. The \( \alpha \beta \) component of nonlinear load current has been generated by quarter cycle time delay method represented in Fig. 8(c). Fig. 7(a) depicts approximately 12 cycles sag generation for the same time instants as discussed for linear load. With the application of proposed modified controller for DVR, results for injected voltage and restored load voltage are shown in Fig. 7(b) and Fig. 7(c). It can be clearly notified that in case nonlinear load there is no delay observed in reference load voltage restoration. From the overall observation and discussion of results, it can be further stated that the load voltage is maintained at its rated RMS value. The load voltage is observed to be satisfactory due to exact voltage injection by DVR resulting in exact restoration of load voltage to its reference value of 200 V. The DC-link voltage is maintained constant to its reference value of 300 V in Fig. 8(a), generation of fundamental \( \alpha \beta \) component of load current from nonlinear current is shown in Fig. 8(c).
Appendix I

System Parameter

|                                |                                                           |
|--------------------------------|-----------------------------------------------------------|
| Power Supply                   | 1phase, 215V(RMS), 50Hz                                   |
| Line impedance                 | 0.2ohm, 1mH                                               |
| Other load Voltage             | 230Vrms, P=800W, Q=200VAR                                 |
| Critical load Voltage          | 230Vrms, P=200W, Q=800VAR                                 |
| Series transformer             | 500VA, 230/230Vrms, X_L=0.8%                              |
| LC ripple filter               | L_f = 2mH, C_f = 15uF                                     |
| DC Link rated voltage          | V_d = 200V                                                |
| DC-link Capacitor              | C_d = 5mF                                                  |
| Switching Frequency            | 8KHz                                                      |

V. Conclusion

The single phase SRF theory based d-q controller has been proposed, analyzed, designed and simulated for linear load and nonlinear load. The proposed controller validates the mitigation of voltage sag at the load end. In this controller no freezing of PLL is required to get the information of phase value prior to occurrence of fault. This reduces the complexity of the controller. The performance of proposed controller of DVR has been found better which tightly compensate sensitive load against voltage sag.

The results demonstrated proves the efficacy of the proposed controller. The controller shows the several benefits over the other existing controllers such as

- The proposed controller can be used in three phase system if phase sequence is properly taken care by the PLL.
- It energizes only one phase which reduces the switching losses and increases the time of compensation.

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