Investigation of the effect of annealing on Si(100) substrate modified by Ga⁺ focused ion beam

M M Eremenko¹, N A Shandyba¹, N E Chernenko¹, S V Balakirev¹, L S Nikitina¹, M S Solodovnik¹ and O A Ageev¹,²

¹Institute of Nanotechnologies, Electronics and Equipment Engineering, Southern Federal University, Taganrog 347922, Russia
²Research and Education Center “Nanotechnologies”, Southern Federal University, Taganrog 347922, Russia

larnikitina@sfedu.ru

Abstract. In this work, we studied the effect of annealing the silicon surface on the morphology of focused ion beam modified areas. It was found that an increase in the ion beam accelerating voltage during surface treatment significantly affects the morphology and the appearance of the implanted material on the surface or its absence/evaporation during annealing. It is shown that an increase in number of ion beam passes leads to the formation of holes on the surface of the modified areas, which is a sign that significant damage to the substrate material has occurred.

1. Introduction
Today, silicon technology is the leader in the global micro- and nanoelectronics market. The use of silicon substrates makes it possible not only to obtain structures with a high performance, but also to reduce the cost of manufacturing devices based on them. However, obtaining high-quality emitting devices based on silicon still remains an unsolved problem due to the indirect gap of the semiconductor [1-4]. Therefore, recently, interest has increased in possible solutions to this problem, namely, monolithic integration of III-V on Si, which would allow combining the advantage of both technologies - high mobility of charge carriers (data reception and transmission) and high-performance data processing [3, 5-8].

This hybrid solution is expected to increase energy efficiency, package density, and reduce the final cost of the devices [6, 8]. However, achieving the desired low level of defectiveness and, as a consequence, high-performance structures remains a challenge. To date, a large number of methods are used to reduce the number of defects during monolithic integration of III-V on Si [1-4, 9-12], but studies of the initial stage are still crucial for understanding the formation of subsequent grown layers, and will also make it possible to obtain modes with the lowest density defects, most of which are assumed to be localized in the lower layers.

2. Experimental procedure
In this work, we investigated the effect of initial annealing on modified silicon areas. Silicon substrates were modified with a focused ion beam (FIB) (Ga⁺) at various accelerating voltages and beam passages. The accelerating voltages varied from 5 kV to 30 kV, the number of passes was 5 and 200. Annealing
was carried out at temperatures of 600 and 800°C for 30 minutes with and without an additional arsenic flux.

3. Results and discussion
Analysis of the results showed that a decrease in the accelerating voltage from 30kV to 5kV (Figure 1) led to the disappearance of Ga droplets in almost all ranges of the considered modifications and temperatures, except for 200 beam passes at a temperature of 800°C (Figure 1b). We believe that this is due to the intense evaporation of the material from the surface, which does not lie deeply, and this process is more advantageous when modifying the surface with beams with a low accelerating voltage and annealing at high temperatures. On the other hand, with an increase in the accelerating voltage on the surface of the modified areas, the implanted material emerges on the surface already from 5 beam passes. We explain its presence by the fact that at a high accelerating voltage, the depth of the material is high and the material gradually comes out to the surface and does not have time to completely desorb from the surface during annealing. However, it should be noted that during processing with an accelerating voltage of 30kV and 200 beam passes (Figure 1d), holes were left on the surface of the modified areas, without the presence of droplets of implanted Ga. The presence of such holes is apparently caused by a large deformation of the Si surface during processing by focused ion beams.

Figure 1. SEM images of modified Si areas after annealing at $T = 800^\circ$C and various accelerating voltages and beam passes, respectively: (a) 5kV and 5, (b) 5kV and 200, (c) 30kV and 5, (d) 30kV and 200.

However, a study of the effect of annealing temperature showed that a decrease in the annealing temperature to 600°C (Figure 2) resulted in no droplets of implanted Ga on the modified area (Figure 2a-c). The observed situation is similar to the mechanism of the evaporation of FIB-implanted Ga during annealing at 800°C, except that Ga droplets are observed only in the areas treated at 30kV and 200 passes (Figure 2d). With a “softer” processing of the substrate than 30kV and 200 passes, the absence of droplets on the surface is explained by the fact that it is not energetically favorable for the material to come to the surface and evaporate at 600°C, when, as a large damage to the surface during processing of 30kV and 200 passes, implanted Ga is collected in large droplets, and part of it evaporates leaving holes in its place.
Figure 2. SEM images of modified Si areas after annealing at $T = 600^\circ$C and various accelerating voltages and beam passes, respectively: (a) 5kV and 5, (b) 5kV and 200, (c) 30kV and 5, (d) 30kV and 200.

Figure 3. SEM images of modified Si areas with Ga$^+$ ions at an accelerating voltage of 30 kV and after annealing with additional arsenic flux at various temperatures and beam passes, respectively: (a) $T = 600^\circ$C and 5, (b) $T = 600^\circ$C and 200, (c) $T = 800^\circ$C and 5, (d) $T = 800^\circ$C and 200.
Next, we studied the effect of an additional arsenic flux on the annealing of modified silicon areas (Figure 3). It is shown that crystallization of implanted Ga occurs. Moreover, a larger number of small crystallized nanostructures is observed than in the case of annealing without arsenic. This suggests that arsenic reduces the evaporation of Ga from the surface and reduces the probability of droplet coalescence (Figure 1c and Figure 3c). From the cases presented in Figure 2d and Figure 3b, it can be understood that the additional flux of arsenic during annealing at a temperature of $T = 600^\circ C$ favorably influenced the formation of crystalline GaAs nanostructures, which can subsequently act as nucleation centers for subsequent grown GaAs layers. However, the use of an additional arsenic flux did not help to reduce evaporation from the surface of the “hard” modified silicon area (Figure 3d). This surface morphology was influenced by two factors: a high annealing temperature, at which GaAs evaporates from the surface with a high probability, and severe damage to the surface during FIB-treatment.

4. Conclusions

Thus, according to the studies carried out, it can be concluded that not only the initial FIB treatment of the silicon surface with Ga ions affects the morphology of the resulting areas, but also such annealing parameters as the temperature and arsenic flux. It is assumed that obtaining optimized annealing parameters together with nucleation layers will make it possible to localize the largest number of defects in the lower layers of structures required for monolithic integration of GaAs on Si. Therefore, in the future, it is planned to study these samples using Raman spectroscopy in order to confirm or disprove our theories.

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