Identifying and Exploiting Sparse Branch Correlations for Optimizing Branch Prediction

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ABSTRACT
Branch prediction is arguably one of the most important speculative mechanisms within a high-performance processor architecture. A common approach to improve branch prediction accuracy is to employ lengthy history records of previously seen branch directions to capture distant correlations between branches. The larger the history, the richer the information that the predictor can exploit for discovering predictive patterns. However, without appropriate filtering, such an approach may also heavily disorganize the predictor’s internal mechanisms, leading to diminishing returns. This paper studies a fundamental control-flow property: the sparsity in the correlation between branches and recent history. First, we show that sparse branch correlations exist in standard applications and, more importantly, such correlations can be computed efficiently using sparse modeling methods. Second, we introduce a sparsity-aware branch prediction mechanism that can compactly encode and store sparse models to unlock essential performance opportunities. We evaluated our approach for various design parameters demonstrating MPKI improvements of up to 42% (2.3% on average) with 2KB of additional storage overhead. Our circuit-level evaluation of the design showed that it can operate within accepted branch prediction latencies, and under reasonable power and area limitations.

1. INTRODUCTION & MOTIVATION
Superscalar pipelined processors rely profoundly on speculative and out-of-order (OoO) execution to keep their pipeline busy, hiding latency with instruction- and memory-level parallelism (ILP and MLP). Branch prediction (BP) is the key mechanism that drives speculative execution by steering the front end of the pipeline, each time predicting the instructions that follow in the stream. Working on the correct code path is paramount to performance since recovering from a branch misprediction and refilling the processor’s instruction reservoirs (ROB, instruction/issue queue, etc.) after a pipeline restart can cost dozens of cycles [1]. Notably, as the misprediction penalty gets larger due to the increasing pipeline depth and width [19,24,30], modern processors have come to rely on incredibly accurate branch predictors.

Today, virtually all branch predictors in high-end processors are highly-engineered variants of TAGE [29] and Perceptron [17]. Over the past 15 years, branch prediction has been primarily focused on these two designs, resulting in some highly sophisticated branch predictors that can overall achieve remarkably high prediction accuracy [18,28]. However, recent studies demonstrate that the missing accuracy gap limits substantially the performance scalability of future processors [4,22]. As the further enhancement of BP methods is becoming increasingly challenging, performance improvements have stagnated the recent years. Lately, the focus has been concentrated on improving the prediction accuracy of a specific class of branches that are regularly mispredicted. In this work, we argue that there are still uncapped opportunities that can unveil key improvements in branch prediction not by strictly focusing on what is classified as “hard-to-predict” (H2P), but by exploring vital control-flow properties that have been systematically overlooked.

More specifically, despite extensive differences in their prediction mechanisms, state-of-the-art branch predictors learn correlations between branches through the use of large hardware tables and long histories of previous branch outcomes (taken/not-taken), with efficacy strongly associated with the amount of storage available. An essential observation made from both TAGE- and Perceptron-based predictors is that predictive signatures in branch history occur with varying lengths. That is, long histories may be able to expose important branch patterns that shorter ones fail to and vice versa.
As such, modern BP designs are built with a set of input features that are based on branch histories with different lengths (in number of bits) [1, 12].

Ultimately, longer histories can elicit correlations with the more distant past, but in the general case, the correlation of a branch with a large history is rather sparse, i.e., only a few selective parts of the history are eventually informative of the branch outcome [6, 7]. As an example, in Fig. 1, we demonstrate the sparsity of branch correlations in two SPECint2017 applications (xz and leela) with the highest branch misprediction rate [21]. To characterize sparsity, we use linear regression analysis methods. In particular, we perform Lasso logistic regression [16] over all the static\(^1\) branches in our dataset, and we build sparse linear functions (models) that predict branches based on the branch-outcome history (128-bit long). We choose to employ linear models as they lend themselves well to a pragmatic hardware implementation. We only consider sparse models of over 99% accuracy that relate to branches that are not highly biased towards a specific direction. Rows in Fig. 1 correspond to a few such branches per application, while each mark indicates the existence of correlation between their outcome and the corresponding history location.

As illustrated, the screened branches are correlated with at most 20 sparse history locations, and in some cases, only with a single one. Nonetheless, modern history-based branch predictors do not employ methods for discarding the non-informative (noisy) parts of the branch history during prediction (TAGE-based) or they attempt to identify them online (i.e., at run-time) with weight balancing (Perceptron-based). This fundamental design decision leads to a catastrophic explosion of the number of table entries required for tracking all the observable history patterns since such number grows exponentially with the history length [9]. As branch predictors are traditionally anticipated to be trained online, designers resort to various heuristics trying to workaround this issue. Yet, the focus has been mainly on achieving a high enough accuracy per bit of storage capacity rather than on revising rigorously the key prediction principles [32].

Our work aims to fill this gap by attending to only the few important bits in the branch history vectors, while discarding the non-informative ones. To properly filter the branch history at this granularity, it is necessary to adopt more detailed training algorithms through additional compiler support, otherwise dubbed “offline training”. Fortunately, in the era where data center/cloud applications surge, the otherwise overwhelming cost of offline training can be amortized through economies of scale. In this work, we employ an “offline-training/online-inference” paradigm, as detailed by Lin & Tarsa [22], for introducing sparsity-aware branch prediction. Specifically, our contributions are as follows:

1. Effective detection of sparsely correlated branches.

   We demonstrate that in practical workloads there exist branches whose direction (i.e., taken/not-taken) can be modeled with a sparse linear mapping from their history. In particular, we employ an offline methodology for determining sparse linear model parameters per branch that we call “sparsity hints”.

2. Novel sparsity-aware branch prediction design. We show that sparsity hints improve prediction accuracy using a compact storage. We present a detailed microarchitectural design of a branch predictor, dubbed Sparse Linear Branch Inference Unit (SLBIU), that uses sparsity hints for a few selected branches, operating as an auxiliary component alongside a primary branch predictor. Overall, our scheme improves the prediction accuracy on CBP-5 [3] and SPECint2017 [31] benchmark suites, compared to TAGE-SC-L 8KB with 2KB of storage overhead. Moreover, our design can operate within the latency acceptable by the CPU front-end for branch prediction, while remaining under reasonable area and power limitations.

2. CURRENT PREDICTORS LIMITATIONS

State-of-the-art branch predictors, such as TAGE [29] and Perceptron [17], are tabular and history-based, i.e., they identify predictable branch patterns by mapping recent branch-outcome histories to internal state machines (saturating counters or weights) stored in table-entries. Most commonly, they use various formations of the local (previous outcomes of a static branch) and the global history record (prior outcomes of any branch) and the branch program counter (PC). Intuitively, branch histories are expressed as a sequence of consecutive binary events (taken/not-taken) leading to a branch. For example, the global history is a k-bit sequence representing the k branch directions before a certain branch. As such, history-based predictors attempt to identify predictable patterns in the form of thick series of events, even when branches correlate sparsely with them. Ideally, a separate table-entry will be allocated for each observable pattern. As the number of patterns grows exponentially with the history length, the required number of entries becomes quickly too large.

Current branch predictors use astonishingly large branch histories. TAGE-SC-L [28], the most recent TAGE variant and winner of the last BP championship (CBP-5) [3], tracks histories with lengths up to 3,000 bits, whereas the Multiperspective Perceptron predictor [18] (ranked second in CBP-5), uses several features acquired by tracking similarly sized histories. As the employed histories become longer, more previous branch directions can be looked up, and thus, the chances of identifying correlation with more distant branches increases. Nonetheless, so does the amount of sparsity and variation of the predictive signatures.

Consider the simple case of two if-type branches A and B with dependable conditions, where branch A precedes branch B in the program order. In such a scenario, the outcome of B correlates with the one of A. If there are M other if-type branches between A and B with independent conditions that change directions constantly, there will be at least \(2^{M+1}\) different patterns that the predictor needs to distinguish to predict B accurately. These intermediate M branch-outcomes can be considered as “noise” in the history, since B can be predicted accurately by solely monitoring A. This noise burdens the predictor with superfluous increase of entries allocations for tracking all the observable patterns. Under

\(^1\)A static instruction (either branch or not) is uniquely identified by its PC (program counter) address and might be executed dynamically more than once for a specific program execution, e.g., in a loop.
As we will show, sparse linear modeling effectively captures Although branch predictors employ various storage-saving heuristics to generally mitigate entries allocation, they miss sparsity by tracking history patterns in a quite dense form. TAGE predictors are based on the PPM data compression scheme [5]. They employ a plurality of tables that are indexed using overlapping history slices of increasing lengths, hashed (XOR-ed) with the branch address. Table entries contain (partially) tagged saturating counters that model the prediction. The matching entry that is accessed with the longest history provides eventually the prediction. As in PPM, the intuition is that longer histories should be used when shorter ones fail to be accurate. Yet, even when the correlation of a branch with the history is sparse, TAGE predictors need to allocate storage for tracking all the possible patterns, since the histories are used in a compact way, i.e., without an explicit mechanism for disregarding the non-informative parts. Glimpsing at Tab. 1 (detailed in Sec. 3) demonstrates the effects of the excessive entries allocation when histories are noisy. Especially under the storage pressure of 8KB, TAGE-SC-L repeatedly "forgets" and "relearns" branch patterns, inducing a much higher number of mispredictions than at 64KB.

Perceptron predictors are loosely based on the homonymous learning algorithm. Their prediction mechanism receives a vector of inputs with corresponding weights and computes their dot product, which is then thresholded to provide the prediction. Input weights are trained and adapted according to the correctness of the produced predictions. Initial proposals used only the global history [17], while in the latest Perceptron predictors, the input vector consists of several different hashes (organizations) of the branch history [18,33]. Still, without filtering the branch history a priori, Perceptron suffers from significant aliasing among noisy histories and their synthetic formations.

As in our dataset (see Sec. 5.1), Perceptron predictors achieve lower accuracy than TAGE predictors, we employ the latest TAGE-SC-L models [28] for our study (explained in Sec. 5.1). In next section we explore the application of sparse modeling in BP for capturing the sparse correlations between branches and recent history. We specifically focus on sparse linear models, dropping the non-linear ones that can induce excessive storage and computational overheads. As we will show, sparse linear modeling effectively captures branches’ correlation with a commonly used set of features, namely the global and local branch history, and inherently identifies its sparsity.

### 3. Sparse Branch Correlations

We start our exploration by outlining in Tab. 1 a few examples that demonstrate the opportunity behind sparse branch-history correlations. Interestingly, the reported branch examples are not “hard to predict” for TAGE-SC-L (around a 1% misprediction ratio). However, the average number of entries that TAGE-SC-L allocates for these branches is far from optimal since it has to replicate them exponentially per every noisy uncorrelated event (branch outcome) in the history. For example, TAGE-SC-L 64KB allocates 1K entries on average for a branch that could be predicted accurately with a single sparse signature (LONG-MOBILE-1 / 548221168352). TAGE-SC-L 8KB requires 443.5 entries on average for the same branch and, more importantly, induces around 51× mispredictions by not being able to suppress the effects of destructive aliasing in such a limited storage budget.

This storage efficiency issue is in line with previous work that exposed it by examining TAGE-SC-L 64KB with large code-footprint applications [22]. Storing only sparse correlations could therefore generally improve the performance of state-of-the-art branch predictors by eliminating the need to represent irrelevant features in their storage, thereby reducing the predictor’s footprint. Nonetheless, identifying and exploiting sparsity effectively is a grand challenge for branch predictors. By historically performing training solely online, typical branch-prediction designs are quite cumbersome for applying powerful sparse modeling. The next section provides a brief background of sparse linear modeling, revealing its interconnection with branch prediction.

#### 3.1 Sparse Linear Modeling

In supervised learning prediction tasks, often, only a small subset of input variables contributes to the prediction outcome. In the case of linear models where we focus, the problem is well-studied in literature with various synonyms, i.e., sparse modeling, sparse signal recovery, and Lasso regression [16]. In our study, we apply these techniques in the context of BP. Due to the binary nature of branch outcomes, BP resembles a classification problem. Thus, we opt to employ the Lasso logistic regression model, i.e., $\ell_1$ regularized logistic regression. Our main focus is on offline linear methods to understand the limitations and opportunities that

| Trace / branch      | Oracle Sparse Prediction | TAGE-SC-L Misses | TAGE-SC-L Entries (avg) | Allocations |
|---------------------|--------------------------|------------------|------------------------|-------------|
|                     | History bits | Misses  | 8KB | 64KB | 8KB | 64KB | 8KB | 64KB |
| SHORT-SERVER-225 / 5564716 | 1 | 45,794 | 103,383 | 74,393 | 311.7 | 159.9 | 3,022.14 | 1,131.9 |
| SHORT-SERVER-60 / 50044 | 7 | 711 | 66,516 | 54,686 | 61.9 | 75K | 601.9 | 421.7 |
| SHORT-MOBILE-60 / 50044 | 7 | 711 | 66,310 | 54,976 | 69.3 | 71K | 834.5 | 479K |
| SHORT-MOBILE-59 / 50044 | 9 | 879 | 64,126 | 33,102 | 73.5 | 40K | 421.7 | 421.7 |
sparsity could present in BP. However, in Sec. 7, we also examine the promising yet challenging case of online sparse linear modeling.

Assume a collection of input feature-vectors and target pairs: \((x_1, y_1), (x_2, y_2), \ldots, (x_m, y_m)\) where \(x_i \in \mathbb{R}^l\) is the \(i\)-th input feature-vector and \(y_i \in \{0, 1\}\) is the corresponding target. Lasso logistic regression seeks for a linear logistic function \(f(x) := \sigma(b + w^\top x)\) where \(\sigma(a) := 1/(1 + \exp(-a))\) is the sigmoid function, \(b\) is the model bias/intercept, \(w^\top x\) denotes the dot-product and \(w\) is the vector of model weights. The parameters \((w, b)\) that define \(f(x)\), are determined by optimizing the following objective:

\[
\min_{b \in \mathbb{R}, w \in \mathbb{R}^l} \left\{ \frac{1}{m} \sum_{i=1}^{m} L(y_i, f(x_i)) + \lambda \|w\|_1 \right\}
\]

for some \(\lambda \geq 0\), \(L(a, b)\) being the logistic loss and \(\|w\|_1 = \sum_{j=1}^l |w_j|\) the \(\ell_1\)-norm. The hyperparameter \(\lambda\) enforces a trade-off between the model’s sparsity and prediction performance. That is, in the special case where \(\lambda = 0\), Equation (1) corresponds to logistic regression (no model sparsity enforced). On the other extreme, it can be shown that \(w\) is the all-zero vector for a large enough value of \(\lambda\). Setting an appropriate \(\lambda\) value is not a trivial task, although methods such as coordinate descent [10] can compute the full regularization path of \(\lambda\) values. Such methods are also guaranteed to converge to a globally optimal solution [36]. In our experiments, we observed that a binary search approach on the range of \(\lambda \in [10^{-4}, 1.0]\) with a stopping criterion of 99% accuracy allows us to fine-tune \(\lambda\) efficiently. Finally, we should note that there are several methods that can compute an optimal solution of Equation (1) [16].

### 3.2 Sparse Linear Models on Branch History

Branch predictors correlate the behavior of branches with the recent history of previous branch outcomes, expressed, most commonly, through the global and the local history records (GHR/LHR). To leverage the sparsity of branches’ correlations, we construct sparse linear models that can express branch outcomes based on the branch history. In particular, we aim to define the parameters (bias and sparse weights) of a logistic regression model \(f_{pc}(x) := \sigma(b + w_1 x_1 + \cdots + w_K x_l)\) so that \(f_{pc}(x) \approx y\), where \(x\) is the branch history with branch directions represented as \(\{\pm 1\}\), and \(y\) is the modeled branch outcome. \(f_{pc}(x)\) returns the prediction probability that the branch identified with its PC will be taken. To simplify the inference, we replace the sigmoid function with a sign check. If the sign is negative, the branch outcome is predicted not-taken and taken otherwise.

During training, once the history is sufficiently populated, we collect training samples in the form of \((x_i, y_i)\) where \(x_i\) is the history vector and \(y_i\) is the sampled branch outcome. Equipped with the above modeling configuration, Equation (1) can be optimized for every static branch. After training, based (mainly) on the accuracy and the sparsity of the resulting models of all the screened branches, it is defined which of them follows a sparse linear model. Sec. 4.1.2 makes an in-depth analysis of this process.

Based on this setup, we now perform sparsity analysis on traces of SPECINT2017 [31] applications described in Sec. 5.1. The branch history we use is the concatenation of a 512-bit GHR and a 512-bit LHR, i.e., \(l := 1024\) and \(x := [\text{ghr}_1, \ldots, \text{ghr}_{512}, \text{lhr}_1, \ldots, \text{lhr}_{512}]\). We perform Lasso logistic regression on all the branches of each trace (with a few exceptions) to show that sparse linear correlations can be efficiently modeled. To strengthen our confidence in the statistical properties of the computed models, we exclude branches that are highly biased towards a single direction, i.e., those with a taken rate less than 2% or greater than 98%, and branches that appear less than 10K times in a trace. As the crux of our work is to design effective sparsity-aware branch predictors, we also set a rigid 99% accuracy threshold, only above which, a sparse model is considered sufficiently accurate. In Fig. 2 we plot the distribution of all the sufficiently accurate and non-highly-biased branches according to the number of the non-zero (nnz) weights of their model, as returned by sparse modeling. Note that per application, some branches may be counted more than once if they appear in multiple traces of the application.

As illustrated, most branches have a sharp decaying distribution based on the number of their non-zero (nnz) weights. Furthermore, the majority of them requires a fairly small number of non-zero weights in proportion to the employed history length (1024-bit long), bounded at 35. Consider that for clarity we have also dropped the first histogram bin grouping branches of one single non-zero weight, as it was fairly

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**Figure 2:** Distribution based on non-zero weights.

**Figure 3:** Average entries vs non-zero weights.
we show numerous cases of branches. We found very few branches with highly-accurate sparse models, as TAGE-SC-L 8KB is plagued largely by such cases. In Fig. 3 shown by Fig. 2.

4. SPARSE PREDICTOR ARCHITECTURE

We now present our sparsity-aware BP scheme outlined in Fig. 4. Our proposal assumes a deployment scenario where predictions are generated at runtime after an offline training phase, as also considered in the work of Lin & Tarsa [22]. Offline training is necessary to capture the predictive statistics of the otherwise hardly detectable sparse correlations. It consists of three major steps, starting with sparse linear modeling for extracting the branch models, then compression of such models and eventually filtering. Branch models are filtered according to certain microarchitectural design constraints that facilitate their use by a dedicated component called Sparse Linear Branch Inference Unit (SLBIU) for runtime prediction. SLBIU is the BP mechanism that stands at the core of our scheme, specialized to predict branches with offline-prepared sparse models. We envision SLBIU as an auxiliary element of the branch prediction unit (BPU), complementing the functionality of the primary branch predictor that is traditionally trained solely online. In the rest of this section, we describe all the details of our model, including offline processing, microarchitectural modifications and certain system requirements of our deployment scenario.

4.1 Offline Training Process

The offline stage requires a set of branch traces collected by profiling target applications in a post-compilation phase. Such traces undergo Sparse Modeling through Lasso logistic regression (as described in Sec. 3.2) that produces the Sparsity hints: a set of per-branch sparse linear models that are attached to the program binary. Sparsity hints essentially materialize into a collection of weights and history-indices pairs. Each weight expresses the correlation of the screened branch with the branch at the respective history index. The sparsity hints are loaded to the SLBIU using a dedicated SW/HW API and used to perform BP by using the dynamic history as input. The SLBIU functionality and API are described in Sec. 4.2. As such, it is crucial to keep storage requirements and complexity in reasonable levels without compromising performance. To do so, we perform two necessary optimizations on sparsity hints before deployment, denoted as Compression and Selection routines in Fig. 4.

4.1.1 Compression

Weights Quantization: Sparse linear model training is performed in floating point arithmetic with a high-enough precision able to express small parameter updates during models’ optimization. However, once sparse models are trained, weights can be represented with fewer bits for use during inference. We quantize the model weights to $Q(f_i,f) \times 2^{lhr+}\{s\}$ fixed precision format [13] by rounding each weight to its nearest representable signed number [11]. As we will show, 8-bit weights are sufficient for our models expressed in Q3.4.

History Deduplication: We observed that, quite often, branch histories lead to (conceptually) duplicated inputs. For example, in a loop-type branch with $s$ iterations, local history satisfies $lhr_{o+2} = lhr_{o+2s} = lhr_{o+3s} = \ldots $ for a positive offset $o$. For such a branch, Lasso will assign arbitrary weights in the full history set. However, if there is indeed some correlation with any of these history indices, only one of them is sufficient to express it. To detect these duplicates, we leverage ElasticNet, a generalization of Lasso that assigns approximately the same weight on highly correlated or duplicated features [42]. In this way, we manage to keep only one instead of multiple identical non-zero weights for branches with such a “strided” local-history.

4.1.2 Selection

The set of sparsity hints produced after compression contains a sparse model for every static branch of the target program. However, evidently, sparse models are not efficient for all static branches. Essentially, the number of static branches per application that are predicted more accurately with a sparse model than a state-of-the-art predictor is conveniently small. In our evaluation, we show that the number of finally selected sparsity hints does not exceed 13, for a storage overhead of 2KB. Still, by removing the burden of predicting such sparsely-correlated branches from the primary predictor, enables important improvements, as we discuss in Sec. 6.

As it appears, it is necessary to employ a selection method to filter out the non-promising cases or otherwise to define the cases where it is effective to employ a sparse model. Such selection method needs to solve an optimization problem: identify the subset of branches that are predicted with bet-

\[ o + lhr_{o+1} + lhr_{o+2} + lhr_{o+3} = \ldots \]
ter accuracy through sparse models under certain storage constraints. We consider two dimensions to express storage constraints, the maximum permitted number of sparsity hints, denoted by $n$, and the maximum permitted number of non-zero weights per selected hint, denoted by $nnz$. Our selection method follows three steps. First, we employ a specific score function $S$ that assigns a scalar score-value to each hint. Positive scores indicate a potential improvement and negative scores a potential drop in performance. Second, the hints with negative scores or with more than $nnz$ weights are discarded. Finally, the remaining hints are ranked based on their score and the top $n$ (at most) are selected.

We define two different score functions: independent and relative. In the independent score function, hints with relatively low-accuracy (< 99%) are dropped a priori. The remaining hints are assigned with a score equal to the number of their correct predictions solely during the offline analysis. Scores are always positive and they do not consider the performance of the primary predictor. In the relative score function, scores are defined as the difference between the number of correct predictions made by the respective sparse models offline, and the number of correct predictions (estimation with sampling) made by the primary predictor. Both score functions are based on counts of correct predictions instead of accuracy rates to prioritize hints that relate to branches with a greater impact, i.e., hints that achieve high accuracy for branches of very few invocations will have less priority.

### 4.2 Sparse Linear Branch Inference Unit

As mentioned above, the deployment scenario of our scheme involves an offline training phase that produces the sparse prediction models of branches in the form of hints. Sparsity hints are models that receive branch histories as input and provide accurate predictions for the corresponding branches. SLBIU, the "Sparse Linear Branch Inference Unit", is the hardware mechanism that enables the runtime prediction of branches based on these sparse models which are trained offline. In the rest of this section, we describe the structure and functionality of SLBIU and explain all the microarchitectural modifications required by our sparsity-aware branch prediction scheme.

#### 4.2.1 SLBIU Structure

Fig. 5 depicts in detail the building blocks of SLBIU, along with all their essential design parameters described in Tab. 2. SLBIU is abstractly divided in two main parts, the Sparse-Model Storage, that is a content-addressable memory (CAM) space, and the Prediction Engine, that is an arithmetic logic circuitry. The CAM space is fully associative PC-based and holds the sparsity hints and the local histories of the (static) branches selected during the offline training process. Recall that sparsity hints represent sparse models. We use the Coordinate storage format (COO) to encode the sparsity hints, for keeping a fixed size per hint-vector (zero padding) and for allowing a convenient hardware implementation.

SLBIU can store up to $n$ hint-vectors in its CAM space. Each hint-vector includes the $q$-bit wide $nnz$ weights and their respective history indices. Indices are $\lceil \log_2 (gh + lh) \rceil$ bits wide as they encode a history position in the range $[0, gh + lh - 1]$. The intercept values (one per sparse model) and the weights are reduced to $q$ bits after the quantization step discussed in Sec. 4.1.1. Considering all the design parameters listed in Tab. 2 ($lh, gh, n, nnz, q, p$), the amount of storage space required by SLBIU is defined as:

$$\text{Storage} = n(p + q + nnzq + nnz \cdot \lceil \log_2 (lh + gh) \rceil + lh). \quad (2)$$

As it appears, the SLBIU storage scales logarithmically with the global history length ($gh$). Considering that current branch predictors already employ global histories of the order of thousands previous branch outcomes (bits), such logarithmic relation essentially discharges the history length from typically being the major limiting factor. On the other hand, the linear relation of the required storage with the number of branches with sparse models ($n$) and with the number of their non-zero weights ($nnz$), makes both $n$ and $nnz$ the most crucial parameters. In Sec. 6 we discuss the trade-offs that occur from the non-trivial task of determining the optimal values of $n$ and $nnz$ under certain storage budgets.

#### 4.2.2 SLBIU Functionality

As outlined by Fig. 4, in our design, SLBIU does not represent a standalone branch predictor. Essentially, the utility of SLBIU is revealed when coupled with the primary branch predictor of a CPU design through the improvement of the prediction of sparsely correlated branches. In our deployment scenario, SLBIU is informed of the branches with accurate sparse models after an offline analysis. That is, we assume that SLBIU is initialized before a program’s execution phase starts. Initialization includes loading all the sparse model parameters of the selected branches trained offline (intercept value, $nnz$ weights and history indices, as shown in Fig. 5) and resetting all the respective LHR fields to zero. Nevertheless, the potential of performing sparse modeling purely online is not generally excluded. In Sec. 7 we briefly discuss the feasibility of such an implementation scenario, although we keep it out of the scope of this work.

Eventually, SLBIU contains one sparse model per each static branch that has been selected at the end of the offline training phase. When branches are routed for prediction in BPU, SLBIU is probed based on the branch PC in parallel with the primary branch predictor. When discovering that a branch possesses an entry in SLBIU ("hit"), the main branch predictor is signaled to halt any update of its internal state related to that branch, i.e., entries allocations and/or update of entries state machines. Thereafter, the prediction of that branch happens exclusively by SLBIU. In that sense, the selected sparsely correlated branches are offloaded to SLBIU, since they do not require resources by the primary predictor anymore. However, any branch history organization that is

| Parameter | Definition |
|-----------|------------|
| $lh$      | Local history length (in bits) |
| $gh$      | Global history length (in bits) |
| $n$       | Number of branches with sparse models |
| $nnz$     | Maximum number of non-zero weights |
| $q$       | Weights bit-width |
| $p$       | Branch PC bit-width |

Table 2: SLBIU architecture knobs.
weights signs, while 3 taken/not-taken we interpret with the per-branch maintained LHR are the two main inputs we describe the prediction and update process in SLBIU. We couple SLBIU with TAGE-SC-L 8KB that uses GHR (S(ELECT-FI GHN) - IGN) - usually expressed with \{0, 1\} values resulting in a respective set of trained sparse models. Therefore, we obtain multiple traces representing different phases of a program’s execution (using SimPoint [15] intervals) resulting in a respective set of trained sparse models. These models pass the selection and compression steps individually so they may each focus on a different subset of branches that dominate each specific program phase. Even if a branch appears in different models, its weights may differ, representing its localized behavior.

The sparse models are stored in the binary as program metadata. According to our experiments (as seen on Section 6.1), the binary size overhead is expected to be minimal, since, per execution phase, sparse models that account for less than 2KB of storage space suffice to capture effectively the majority of mispredictions from sparse branches. For the on-chip delivery of model parameters, the binary can be annotated with trigger points that will indicate the passing of program phases. The application will then be responsible for unpacking the sparse model of each phase to memory and, using dedicated instructions (ISA extensions), to populate the SLBIU weights from that memory range. Given that the storage overhead of each model is small and the phases represented are multiple billions of instructions each (depending on Simpoint representativeness), the overall loading time is a simultaneous update of LHRs alongside the retrieval of model parameters for prediction, we implement a dual-ported CAM storage space, i.e., a single-bit port for writing and an entry-wide port for reading.

4.3 SW/HW Interface for Sparsity Hints

In this paper, we advocate the use of offline training for more accurate and focused sparse modeling. Our scheme relies on a sparsity analysis performed at compilation over traces that contain branch outcomes recorded from normally running the application. The traces can be generated through a profile-guided optimization (PGO) phase [14]; through manual workload optimization; or through a JIT analysis [2]. Recent work also suggests that PGO may be performed over a wide corpus of other applications using ML techniques [27].

In their previous work [22], Lin and Tarsa indicate that acquiring several traces from a single program allows to effectively refine training over specialized programs statistics. Therefore, we obtain multiple traces representing different phases of a program’s execution (using SimPoint [15] intervals) resulting in a respective set of trained sparse models. These models pass the selection and compression steps individually so they may each focus on a different subset of branches that dominate each specific program phase. Even if a branch appears in different models, its weights may differ, representing its localized behavior.

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also assumed to be negligible. We leave a more detailed analysis and evaluation of the requirements of such a SW/HW interface for sparsity hints or other alternative approaches to future work.

5. EVALUATION METHODOLOGY

5.1 Experimental Setup & Benchmarks

We have implemented the full process of offline training as a software module that receives branch traces and produces the set of selected branch sparse models. Sparse modeling is performed through Lasso logistic regression. Training on branches with roughly 10 million dynamic executions and 1,024-bit long branch history features takes around 3 – 4 minutes in a commodity server.

To evaluate our sparsity-aware BP scheme, we implemented SLBIU and the interface for initialization with the offline-produced sparse models in the CBP-5 trace-based framework [3]. TAGE-SC-L predictors are configured to ignore the branches that hit in SLBIU. TAGE-SC-L and SLBIU work in tandem based on a common GHR. We also model the program-phase adaptation of sparse models by initializing SLBIU before each trace simulation, assuming that each trace represents a program phase with different sparse models. As we perform simulations in CBP-5 framework, we evaluate our BP model exclusively based on MPKI measurements. In this way, we are able to gauge the improvement of state-of-the-art BP independently from the various design-specific artifacts of a modern CPU. Nonetheless, this paper includes all the necessary details for a full-scale evaluation.

We evaluate our microarchitectural model over a rich set of traces that undergo sparse modeling before simulation. Our trace pool includes the publicly available set of CBP-5 [3] traces and a set of traces recorded from running the 10 SPECINT2017 Rate benchmarks [31] using the ref input-set. SPEC traces are obtained for each of the 100M-instructions long Simpoints that we identify per benchmark (20 on average). Therefore, in our experiments, SLBIU is reconfigured every 100M instructions for SPECINT2017 and every 400M instructions on average on CBP-5 traces, i.e., once per trace. In total, we use 382 CBP-5 traces, after dropping some duplicated and corrupted traces and also a few that are already highly optimized by TAGE-SC-L 8KB (< 0.01 MPKI). For SPEC benchmarks with traces from several inputs (x86, x264, perlbench, gcc) we report average metrics with ranges. Note that all our measurements concern the total trace simulation, i.e., no warm-up phase exists. As we are interested in cases where storage pressure is high, we couple SLBIU with TAGE-SC-L 8KB and we report the relative difference in the obtained MPKI. As such, we (arguably) emulate scenarios where large predictors are cornered by applications with extensive working sets. By lacking such cases in our dataset, we do not observe significant differences when coupling SLBIU with TAGE-SC-L 64KB. Therefore, we do not present quantitative analysis for the 64KB variant of TAGE-SC-L. Yet, the 8KB configuration of TAGE-SC-L that we study resembles closely a practical BP design for today’s common CPU resource budgets, as also considered by previous work [22].

5.2 Physical Implementation

We implemented SLBIU as presented in Section 4.2 with an industry-grade technology library and compiler tools. The place-and-route was performed at typical corner (0.8 V, 25°C). We use retiming to balance the 3 pipeline stages, automatic clock gating, and manual clock gating based on the hit signal to avoid switching in the history select and compute logic. The CAM is a fully-associative lookup table implemented as a register file of \( n \) entries of \( p + q + mnz \cdot (q + |\log_2(lh + gh)| + lh) \) bits each.

The power is evaluated based on the switching activities (VCD) extracted from timing-annotated (SDF) post-place & route gate-level simulations running a synthetic benchmark sweeping over different scenarios of branch ratio and branch offloading rate. A scenario consists of a randomly generated trace and a set of random sparsity hints. The scenarios are parameterized by “branch frequency” (ratio between the number of dynamic branches and the number of all dynamic instructions), and by “offloaded branch ratio” (ratio between the number of offloaded sparsity hints and the total number of static branches in the trace). Instructions are scheduled uniformly across the trace, while hints’ weights and indices are drawn from a uniform distribution. Using synthetic scenarios allows us to explore various extreme cases of read/write intensity to our proposed SLBIU circuit.

The simulation of SLBIU is embedded in a cocotb-based [26] testbench, which begins with the sparsity hints initialization (the entire CAM is always filled with hints) and followed by the execution of the 10K-long trace, fetching an instruction every clock cycle. For each branch instruction of the trace the corresponding inputs are applied to SLBIU (PC, GHR and Predict signals), the prediction output is compared with the expected result to verify correctness, and the LHR is updated based on branch resolution.

6. RESULTS & ANALYSIS

We start our analysis by quantifying the effects of various design parameters, then, we continue with an overall evaluation of our approach, and finally, we demonstrate the effectiveness we observe at the circuit level. In all our experiments, TAGE-SC-L 8KB, as implemented in CBP-5 [3], is the primary branch predictor coupled with the respective SLBIU configuration that is examined. All evaluations are relative to the standalone TAGE-SC-L 8KB. Overall, our results demonstrate that our design can achieve noticeable MPKI improvements with insignificant storage overheads.

6.1 Sensitivity to Design Parameters

We distinguish 4 main factors that can affect the performance of our design: the amount of available storage, the method of hints selection, the length of branch histories and the quantization degree of models’ weights. As these design parameters are interdependent, to identify their impact, we define a specific range of cases to experiment, and then, we perform MPKI evaluation by simulating our SPEC traces. Eventually, after experimenting with several combinations, we analyze the most interesting and representative cases.

In particular, we choose to experiment with 3 different storage budgets, the smallest being 0.5KB, a moderate option equal to 2KB, and the largest at 8KB. We perform Sparse
Figure 6: Impact of design parameters (higher is better). The MPKI of baseline TAGE-SC-L 8KB is on top x-axis.

Figure 7: Effect of hints quantization (higher is better). The MPKI of baseline TAGE-SC-L 8KB is on top x-axis.

Modeling (as described in Sec. 5.1) and we prepare a set of branch sparse models for two different history sizes, $lh = gh = 64$ and $lh = gh = 512$. In our first set of experiments, to fully capture the potential of branch sparse models, we allow full-precision floating point weights (32-bit wide) without quantization. Thereafter, we run our two methods for hints selection, independent and relative, to identify the optimal sets of sparsity hints that satisfy the three storage budgets examined. In practice, each selected set defines the actual dimensions $n, nnz$ of SLBIU’s CAM space. Eventually, the $n, nnz$ pair we choose is the one with the highest sum of scores. We configure SLBIU according to the chosen $n, nnz$ pair and we simulate our SPEC trace-set.

Fig. 6 depicts the results of our analysis in two distinct columns, left side for independent and right side for relative selection. Horizontal figure-pairs represent the three storage budgets we examine comparing the two different history sizes used in SLBIU. Unsurprisingly, the relative selection consistently outperforms the independent selection by being able to prioritize only the hints that are guaranteed to im-

prove TAGE-SC-L. Noticeable improvements can be seen in almost all the benchmarks, except from mcf, with leela demonstrating the largest uplift in all cases. As expected, the benefit increases for larger storage budgets where more sparse models can be employed, as validated by Tab. 3 listing the chosen $n, nnz$ pairs. The maximum amount of offloaded branches increases almost linearly with the available storage, while sparsity remains steadily high. The 8KB SLBIU configuration features the maximum $nnz$, that of 43, whereas for both the other storage configurations, $nnz$ does not exceed 34.

| Independent | Relative |
|-------------|----------|
| 0.5KB       | $lh=gh=64$ | $lh=gh=512$ |
| 0.5KB       | $lh=gh=64$ | $lh=gh=512$ |
| 2KB         | (5,16)    | (5,16)    |
| 2KB         | (5,16)    | (5,16)    |
| 8KB         | (50,29)   | (46,32)   |
| 8KB         | (50,29)   | (46,32)   |

Table 3: Chosen pairs of $(n,nnz)$ for Fig. 6.

Furthermore, the set of 512-bit histories account for higher improvements, with a few exceptions in gcc and leela at 0.5KB, and exchange2 at 8KB, where 64-bit histories perform better. Therefore, larger histories broaden the scope of sparse models and allow them to capture effectively correlations that are found in the quite distant past. Even more so, as illustrated in Tab. 3, they achieve that by requiring storage for only the quite few important segments of the history. As our experiments dictate, in the rest of our analysis we will focus on sparsity hints over $lh = gh = 512$-bit histories, filtered with the relative selection method. Next, we explore the impact of quantization, the 4th important performance factor of our design. We evaluate the effectiveness of our model with 8- and 16-bit quantization degrees using Q3.4 and Q3.12 signed fixed-point formats, respectively. To do so, we simulate our SPEC traces using the two most promising SLBIU configurations of 2KB and 8KB. In Fig. 7 we plot the MPKI improvements obtained with quantized models, comparing them with full-precision. According to our results, MPKI improvements are successfully sustained after quantization, although no significant gains are observed. More specifically, for the 2KB SLBIU configuration, the benefits are mostly higher at Q3.4 (8-bit) than at Q3.12 (16-bit) format, manifesting the available quantization headroom. With 8KB SLBIU,
such trend is observed only in gcc and deepsjeng. In most benchmarks, improvements tend to saturate along all precision formats, with the exception of per1bench, where the Q3.12 format performs marginally better. Naturally, quantization enables storage savings that can allow more branches to be offloaded to SLBIU. Our evaluation reveals that such opportunity is more important in lower storage budgets. That is, quantization appears to be necessary for minimizing storage requirements without compromising prediction accuracy.

In Tab. 4 we present the \(n,nnz\) pairs chosen in our experiment, confirming the increase of \(n\) from full-precision to quantized models. More importantly, Tab. 4 shows that sparsity levels remain comparable; \(nnz\) is equal to 36 and 42 for the configurations of 2KB and 8KB, respectively. That is, despite the \(4 \times \) relation of available storage, offloaded branches satisfy well a similar sparsity threshold. Recall that \(nnz\) specifies the maximum number of weights per offloaded branch by defining the width of SLBIU’s CAM (see Fig. 5). As such, configuring SLBIU efficiently for exploiting most of the underlying opportunity appears to be feasible. In next section, we explore this aspect by evaluating the effectiveness of specific SLBIU designs over our large set of traces.

### 6.2 Large-scale MPKI Evaluation

We evaluate the performance of the two best performing configurations from our previous experiments over our full trace set (described in Sec. 5.1). In particular, we compare SLBIU of 2KB and 8KB for 512-bit histories, where sparse-models’ weights are quantized to 8 bits (Q3.4 format) and the set of offloaded branches is selected with the relative method, satisfying the \(n,nnz\) dimensions in Tab. 4, i.e., there can be up to \(n\) selected branches per execution phase (trace) with less than \(nnz\) weights.

Fig. 8 depicts an S-curve of MPKI for the 392 traces of our evaluation set (x-axis) sorted according to TAGE-SC-L 8KB MPKI. We refer to the improvements of the 2KB/8KB configurations in 3 MPKI ranges. In the high range of above 5 MPKI (128 traces) our configurations reduce on average 0.13/0.15 MPKI (1.3%/1.6%). In the middle range of 1-5 MPKI (141 traces) our configurations reduce on average 0.05/0.07 MPKI (2.1%/2.7%). In the low range of 0.01-1 MPKI (123 traces) our configurations reduce on average 0.012/0.014 MPKI (3.4%/3.7%). Note, that across various MPKI ranges we also observed 47 traces (for both designs) where no branches were offloaded to SLBIU resulting in no fluctuation in MPKI. Interestingly, in 23 traces the 2KB configuration achieves (marginally) the best performance. Essentially, such phenomenon exposes the importance of the selection method in large storage budgets, that needs to be optimized adequately for balancing storage exploitation and performance. It also shows that the 2KB SLBIU configuration can be a highly effective design.

Table 4: Chosen pairs of \((n,nnz)\) for Fig. 7

|       | FP32 | Q3.12 | Q3.4 |
|-------|------|-------|------|
| 2KB   | (8,34) | (11,34) | (13,36) |
| 8KB   | (27,43) | (33,53) | (53,42) |

Fig. 9 compares the mean MPKI improvements of the two SLBIU configurations for different groups of traces. Although the storage budget of 8KB gives a higher improvement across all groups of traces, it is only 0.38% higher than of the 2KB. This demonstrates that large storage budgets are not necessary to capture effectively the underlying opportunity.

### 6.3 Circuit-level Evaluation

We evaluate the two SLBIU configurations \((lh = gh = 512, n = 13, nnz = 36, q = 8)\) and \((lh = gh = 64, n = 20, nnz = 29, q = 16)\) that achieved the best MPKI improvement on SPECINT2017 under a 2KB storage budget, for the long and the short history lengths, respectively. The evaluation is in terms of timing, area and power with respect to 28 nm technology. We also provide a rough estimate of this evaluation with respect to a 7 nm technology, for which we use the following scaling factors from 28 nm to 7 nm: 0.4x power@same speed, 1.8x speed@same power, 3.4x area [35, 39].

**Timing.** Both designs run at 750/790 MHz in 28nm, (1.4 GHz in 7 nm). The 3 pipeline stages are balanced, with the critical path dictated by the adder tree (3rd stage) due to the 16-bit operands in the short history configuration, and by the history selection (2nd stage) in the long history configuration. Note that in 7nm same 3-cycle latency can also be retained under certain frequency requirements [40, 41].

**Area.** For both designs, the standard cell-based content-addressable memory (CAM) is dimensioned to 2 KB and thus, it dominates the area breakdown (98%/88%). Nonetheless, CAM occupies just 0.34 mm² of area (0.1 mm² in 7nm).

**Power.** Fig. 10a shows the power for both modules for various offloading ratios and branch frequencies. At full utilization (100%/100%), the two candidate modules consume 15 or 40 mW (i.e., up to 28 mW at 1.3 GHz in 7 nm), where at zero utilization requires just 220 or 240 µW thanks to the high switching reduction achieved by our manual clock gating scheme. Importantly, the SLBIU spends only negligible power for the lookups in its CAM that result in a miss (purple line in Fig. 10a). Conversely, the power is effectively spent only in the cases of a hit. Fig. 10b shows a breakdown of power consumption of each component of SLBIU (CAM, Adder Tree, etc.) at the most aggressive, yet realistic scenario with 100% branch frequency (the unit queried every clock cycle) and over varying offloaded branch ratios. Most power is spent in the history-select unit (50%/13%) and the CAM register file (39%/56%). Despite the same storage, the power consumption is smaller for the 64-bit history configuration due to the 16× smaller history select unit and narrower CAM.

### 7. ONLINE SPARSE MODELING

In our study, we have shown that sparse correlations of branches with branch history can be detected efficiently off-line with sparse modeling. In this section, we briefly argue that such sparsity can be detected also with online training.

To that end, we implemented sparse linear modeling in an online setting, where model parameters are updated after predictions are resolved during trace simulation. We employ 512-bit long global and local histories for comparing online with offline findings from Tab. 1. We experimented with several optimization methods and we found stochastic gradient
descent with cumulative penalty (SGD-L1) [37] as the most efficient. We improved SGD-L1 by adapting the hyperparameter $\lambda$ with online binary search, i.e., starting with $\lambda = 0.01$ and halving it or doubling it within the range $[1e^{-5}, 0.1]$ to keep the number of non-zero model weights at most 50.

Table 5: Number of mispredictions with online and offline sparse linear modeling for branches from Tab. 1.

| Trace / PC               | Online (nnz) | Offline (nnz) |
|-------------------------|--------------|---------------|
| LONG-MOBILE-1 / 548221168352 | 921 (1.2)    | 6,118 (1)    |
| SHORT-MOBILE-16 / 1566871128   | 2,085 (34.1) | 3,697 (7)    |
| SHORT-SERVER-225 / 5564716    | 44,966 (28.5) | 45,794 (1)  |
| SHORT-MOBILE-60 / 50044      | 2,375 (27.0) | 711 (7)      |
| SHORT-MOBILE-24 / 50044      | 2,584 (35.9) | 711 (7)      |
| SHORT-MOBILE-59 / 50044      | 3,152 (35.83)| 879 (9)      |

The hardware implementation of SGD-L1 is challenging, since it requires two additional 32-bit floats per history bit, one for the trainable model weights and one for the cumulative $\ell_1$ penalty. Nonetheless, specific accuracy restrictions, can be used for tracking only a certain subset of static branches with a reasonable entries count and adapt adequately. Similar approaches have already been used during the past in commercial products for learning complicated correlations at runtime, such as Perceptron’s training in IBM’s z15 [1].

In Tab. 5, we present the number of mispredictions of SGD-L1 against the offline sparse linear model of Sec. 3.2. Within parentheses, we show the average number of non-zero weights that SGD-L1 maintains over its execution. As illustrated, such number never exceeds 36, and thus, a unit similar to SLBIU can be efficiently tuned for predicting branches based on the the trained models timely, as we demonstrated in Sec. 6.3. Note that online training is not able to learn the sparsity patterns exactly as in the offline setup, with the pleasant exception of the first branch in Tab. 5. However, online sparse modeling does learn an enlarged set of each sparsity pattern. Furthermore, the number of mispredictions are comparable with the ones offline. These early findings suggest that online sparse linear modeling is a promising research direction.

8. OTHER RELATED WORK

Evers et al. investigated branch correlations and showed that most of the branches can be predicted efficiently by considering a selective history of only a few previous branches. Essentially, our study corroborates the early findings of Evers et al. employing sparse linear modeling to specify the informative branch-history locations. The findings of Evers et al. motivated also the Spotlight branch predictor [38]. Similarly to our work, Spotlight identifies the important parts of the history offline that are then used by a gshare-like predictor [23]. During profiling, global-history segments that lead to a branch are analyzed exhaustively to discover the combination that provides higher accuracy. On the contrary, in
our work we employ non-exhaustive training methods based on sparse modeling to build a dedicated linear model for predicting each screened branch efficiently by a specialized hardware unit. Fern et al. [9] proposed a decision-tree-based branch predictor with dynamic feature selection to decrease the number of input features, thereby reducing the storage of a tabular branch predictor. Some recent studies [13, 20] focused on the implementation of Neural-Network-based predictors that can be trained online, similarly to the online sparse modeling concept we briefly discussed in Section 7. BranchNet [40] and the work of Tarsa et al. [34] train offline convolutional neural networks for branches that are hard-to-predict for TAGE. Our work differs in the simplicity of the linear models we deploy and in targeting a fundamental control-flow property, the sparsity of branch correlations, that is independent from the predictor’s mechanism. Similarly to the above works, however, our model does not target data-dependent branches which have been recently addressed using compiler support by SLB-predictor [8] or using aggressive run-ahead execution as in Branch Runahead [25].

9. CONCLUSIONS & FUTURE WORK

This study stimulates the development of sparsity-aware branch prediction for improving accuracy by exploiting a fundamental property of programs control-flow, the sparsity of branch correlations. We analyzed several traces derived from SPECINT2017 benchmarks and CBP-5 by capitalizing on sparse modeling methods. Our results demonstrated the existence of numerous sparsely correlated branches. Such branches impede the effectiveness of common branch predictors by putting them under an unnecessary pressure for entries allocation. To eliminate their effects, we propose to employ offline sparse modeling for producing the respective sparse models of branches that will be used for runtime prediction. To that end, we introduce SLBIU, a hardware mechanism specialized to predict branches with offline-prepared sparse models. SLBIU works auxiliary to the primary branch predictor of a CPU design and improves significantly the prediction of sparsely correlated branches. In particular, when combined with TAGE-SC-L 8KB, SLBIU accounts for up to 42% (2.3% on average) of MPKI improvements with 2 KB of storage overhead. Furthermore, our circuit-level evaluation with 28nm technology showed that SLBIU is able to deliver predictions in 3 clock cycles at 740 MHz by requiring no more than 40 mW of power and as little as 0.34 mm² of area. Essentially, our results demonstrate the important benefits in branch prediction from identifying and exploiting sparsity effectively. Our study unlocks several other topics for exploration, mainly related to the optimization of offline training of sparse models. In future work, we plan to investigate the effectiveness of other algorithms from the quiver of sparse modeling and also study their runtime adaptability.

REFERENCES

[1] N. Adiga, J. Bonanno, A. Collura, M. Heizmann, B. R. Prasky, and A. Saporito, “The ibm z15 high frequency mainframe branch predictor industrial product,” in International Symposium on Computer Architecture (ISCA), 2020, pp. 27–39.

[2] M. Berndt and L. Hendren, “Dynamic profiling and trace cache generation,” in International Symposium on Code Generation and Optimization, 2003. CGO 2003., 2003, pp. 276–285.

[3] CBP-5, “Championship branch prediction,” In conjunction with the International Symposium on Computer Architecture (ISCA), 2016. [Online]. Available: https://www.jilp.org/cbp2016/

[4] A. Chauhan, J. Gaur, Z. Sperber, F. Sala, L. Rappoport, A. Yozay, and S. Subramoney, “Auto-prediction of critical branches,” in International Symposium on Computer Architecture (ISCA), 2020, pp. 92–104.

[5] J. Cleary and I. Witten, “Data compression using adaptive coding and partial string matching,” IEEE Transactions on Communications, vol. 32, no. 4, pp. 396–402, 1984.

[6] M. Evers, “Improving branch prediction by understanding branch behavior,” Ph.D. dissertation, University of Michigan, USA, 2000.

[7] M. Evers, S. J. Patel, R. S. Chappell, and Y. N. Patt, “An analysis of correlation and predictability: What makes two-level branch predictors work,” in International Symposium on Computer Architecture (ISCA), 1998, p. 52–61.

[8] M. U. Farooq, Khubaib, and L. K. John, “Store-load-branch (slb) predictor: A compiler assisted branch prediction for data dependent branches,” in 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA), 2013, pp. 59–70.

[9] A. Fern, R. Givan, B. Falsafi, and T. Vijaykumar, “Dynamic feature selection for hardware prediction,” ECE Technical Reports, Purdue University, 2000.

[10] J. Friedman, T. Hastie, and R. Tibshirani, “Regularization paths for generalized linear models via coordinate descent,” Journal of Statistical Software, vol. 33, no. 1, pp. 1–22, 2010.

[11] D. Golovin, D. Sculley, B. McMahan, and M. Young, “Large-scale learning with less ram via randomization,” in International Conference on International Conference on Machine Learning (ICML), vol. 28, no. 2, 2013, pp. 325–333.

[12] B. Grayson, J. Rupley, G. Z. Zuraski, E. Quinnell, D. A. Jiménez, T. Nakra, P. Kitchin, R. Hensley, E. Brekelbaum, V. Sinha, and A. Ghiya, “Evolution of the samsung exynos cpu microarchitecture,” in International Symposium on Computer Architecture (ISCA), 2020, pp. 40–51.

[13] P. Gupta, “Neural methods for resolving hard-to-predict branches,” Ph.D. dissertation, Georgia Institute of Technology, 2021.

[14] R. Gupta, E. Mehofer, and Y. Zhang, “Profile guided compiler optimizations,” 2002.

[15] T. Hastie, R. Tibshirani, and M. Wainwright, Generalized Linear Models via Coordinate Descent,” Journal of Instruction Level Parallelism, vol. 7, no. 4, pp. 1–28, 2005.

[16] T. Hastie, R. Tibshirani, and M. Wainwright, Statistical Learning with Sparsity: The Lasso and Generalizations. Chapman & Hall/CRC, 2015.

[17] D. A. Jiménez and C. Lin, “Dynamic branch prediction with perceptrons,” in International Symposium on High-Performance Computer Architecture (HPCA), 2001, pp. 197–206.

[18] D. A. Jiménez, “Multiperspective perceptron predictor,” in Proc. 5th Championship on Branch Prediction, https://www.jilp.org/cbp2016/, 2016.

[19] T. S. Karkhanis and J. E. Smith, “A first-order superscalar processor model,” in International Symposium on Computer Architecture (ISCA), 2004, pp. 338–349.

[20] J. Lafiandra, “Brat: Branch prediction via adaptive training,” Master’s thesis, Georgia Institute of Technology, 2021.

[21] A. Limaye and T. Adegbija, “A workload characterization of the spec cpu2017 benchmark suite,” in 2018 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2018, pp. 149–158.

[22] C. Lin and S. J. Tarsa, “Branch prediction is not a solved problem: Measurements, opportunities, and future directions,” in IEEE International Symposium on Workload Characterization (IISWC), 2019, pp. 228–238.

[23] S. Mcfarling, “Combining branch predictors,” Digital Equipment Corporation, Western Research Lab, Tech. Rep., 1993.

[24] P. Michaud, A. Seznec, and S. Jourdan, “An exploration of instruction fetch requirement in out-of-order superscalar processors,” in International Journal of Parallel Programming vol. 29, pp. 35–58,
2001.

[25] S. Pruett and Y. Patt, “Branch runahead: An alternative to branch prediction for impossible to predict branches,” in MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture, 2021, pp. 804–815.

[26] B. J. Rosser, “Cocotb: a python-based digital logic verification framework,” 2018.

[27] N. Rotem and C. Cummins, “Profile guided optimization without profiles: A machine learning approach,” 2021. [Online]. Available: https://arxiv.org/abs/2111.14679

[28] A. Seznec, “TAGE-SC-L branch predictors again,” in Proc. 5-th Championship on Branch Prediction, 2016. [Online]. Available: https://www.jilp.org/cbp2016/

[29] A. Seznec and P. Michaud, “A case for (partially) TAgged GEometric history length branch prediction,” Journal of Instruction Level Parallelism, vol. 8, 2006. [Online]. Available: http://www.jilp.org/vol8

[30] E. Sprangle and D. Carmean, “Increasing processor performance by implementing deeper pipelines,” in International Symposium on Computer Architecture (ISCA), 2002, p. 25–34.

[31] Standard Performance Evaluation Corporation, “The SPEC CPU 2017 Benchmark Suite,” in http://www.spec.org, 2017.

[32] D. Suggs, M. Subramony, and D. Bouvier, “The amd “zen 2” processor,” IEEE Micro, vol. 40, no. 2, pp. 45–52, 2020.

[33] D. Tarjan and K. Skadron, “Merging path and gshare indexing in perceptron branch prediction,” ACM Trans. Archit. Code Optim., vol. 2, no. 3, p. 280–300, Sep. 2005.

[34] S. J. Tarsa, C.-K. Lin, G. Keskin, G. Chinya, and H. Wang, “Improving branch prediction by modeling global history with convolutional neural networks,” arXiv:1906.09889, 2019.

[35] Team VLSI, “Tsmc 7nm, 16nm and 28nm technology node comparisons,” https://www.teamvlsi.com/2021/09/tsmc-7nm-16nm-and-28nm-technology-node.html, 2021.

[36] P. Tseng, “Convergence of a block coordinate descent method for nondifferentiable minimization,” J. Optim. Theory Appl., vol. 109, no. 3, p. 475–494, 2001.

[37] Y. Tsuruoka, J. Tsujii, and S. Ananiadou, “Stochastic gradient descent training for l1-regularized log-linear models with cumulative penalty,” in Proceedings of the Joint Conference of the 47th Annual Meeting of the ACL and the 4th International Joint Conference on Natural Language Processing of the AFNLP, vol. 1, 2009, p. 477–485.

[38] S. Verma, B. Maderazo, and D. M. Koppelman, “Spotlight - a low complexity highly accurate profile-based branch predictor,” in International Performance Computing and Communications Conference, 2009, pp. 239–247.

[39] WikiChip, “7 nm lithography process,” https://en.wikichip.org/wiki/7_nm_lithography_process, 2021.

[40] S. Zangeneh, S. Pruett, S. Lym, and Y. N. Patt, “Branchnet: A convolutional neural network to predict hard-to-predict branches,” in Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020, pp. 118–130.

[41] J. Zhao, A. Gonzalez, A. Amid, S. Karandikar, and K. Asanović, “Cobra: A framework for evaluating compositions of hardware branch predictors,” in 2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS). IEEE, 2021, pp. 310–320.

[42] H. Zou and T. Hastie, “Regularization and variable selection via the elastic net,” Journal of the Royal Statistical Society: Series B (Statistical Methodology), vol. 67, no. 2, pp. 301–320, 2005.