High-Throughput Flexible Belief Propagation List Decoder for Polar Codes

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Abstract—Owing to its high parallelism, belief propagation (BP) decoding is highly amenable to high-throughput implementations and thus represents a promising solution for meeting the ultra-high peak data rate of future communication systems. However, for polar codes, the error-correcting performance of BP decoding is far inferior to that of the widely used CRC-aided successive cancellation list (SCL) decoding algorithm. To close the performance gap to SCL, BP list (BPL) decoding expands the exploration of candidate codewords through multiple permuted factor graphs. From an implementation perspective, designing a unified and flexible hardware architecture for BP decoding that supports various PFGs and code configurations presents a big challenge. In this paper, we propose the first hardware implementation of a BPL decoder for polar codes and overcome the implementation challenge by applying a hardware-friendly algorithm that generates flexible permutations on-the-fly. First, we derive the graph selection gain and provide a sequential generation (SG) algorithm to obtain a near-optimal PFG set. We further prove that any permutation can be decomposed into a combination of multiple fixed routings, and we design a low-complexity permutation network to satisfy the decoding schedule. Our BPL decoder not only has a low decoding latency by executing the decoding and permutation generation in parallel, but also supports an arbitrary list size without any area overhead. Experimental results show that, for-length-1024 polar codes with a code rate of one-half, our BPL decoder with 32 PFGs has a similar error-correcting performance to SCL with a list size of 4 and achieves a throughput of 25.63 Gbps and an area efficiency of 29.46 Gbps/mm² at SNR = 4.0 dB, which is 1.82× and 3.33× faster than the state-of-the-art BP flip and SCL decoders, respectively.

Index Terms—polar codes, high-throughput, belief propagation list (BPL) decoding, permuted factor graph, permutation, automorphism ensemble, hardware implementation.

I. INTRODUCTION

POLAR codes, proposed by Arıkan in [1], have become an integral part of 5G new radio (NR), where they were ratified as the standard codes for the control channels of 5G enhanced mobile broadband (eMBB) scenarios [2]. Along with the invention of polar codes, Arıkan introduced successive cancellation (SC) decoding and belief propagation (BP) decoding. Following the evolution of communication scenarios, both SC and BP decoding led the development of polar decoding algorithms and implementations, which were extended into a series of advanced polar decoders such as SC list (SCL) [3]–[9], BP list (BPL) [10]–[18], and BP flip (BPF) [19]–[22] decoders.

While the original SC decoding algorithm can achieve channel capacity at infinite code lengths, it shows poor error-correcting performance with practical finite code lengths. To improve the error-correcting performance of SC decoding, SCL decoding was proposed in [3] to keep a list of up to L candidate codewords. Additionally, when concatenated with cyclic redundancy check (CRC) codes [4], polar codes with SCL decoding outperform low-density parity-check (LDPC) and Turbo codes in terms of the error-correcting performance [23]. To satisfy the low-latency and high throughput requirements of eMBB scenarios, node-based fast SCL decoders [5]–[9] focus on exploiting special constituent codes [24]–[28], which help to avoid traversing the lower stages of the decoding tree to provide a significant reduction in decoding latency compared to conventional bit-wise SCL decoders. The state-of-the-art (SOA) node-based SCL decoder [9] with a list size \( L = 8 \) achieves a throughput of more than 2.94 Gbps, which fits the reliability, latency, and throughput requirements of eMBB scenarios. However, when considering the ultra-high peak data rate requirements of future communication systems [29], SC-based decoders become impractical due to the serial processing inherent in these algorithms [5]–[9].

In contrast to SC-based decoding, BP decoding is an inherently parallel algorithm. BP decoding can thus be implemented easily in a multi-stage factor graph in pursuit of a much higher throughput [30]. Additionally, BP decoding has the potential to realize iterative detection and decoding to achieve better system performance than separate detection and decoding [31], [32], which further raises the interest in BP decoding for academia and industry. Though the error-correcting performance of BP decoding improves as the iteration number increases, it is still far behind the SCL performance. BPF decoding [19]–[22] and BPL decoding [10]–[18] are two advanced BP algorithms that can approach the performance of SCL by expanding the exploration of candidate codewords. BPF decoding guesses the positions of error-prone bits and sequentially corrects them in additional decoding attempts. Unfortunately, online identification of error-prone bits [20]–[22] through sorting and post-processing of channel messages increases the hardware complexity and degrades the maximum operating frequency [22]. Alternatively, BPL...
we can deploy the SC, SCL, or BP decoding on multiple PFGs, where the number of possible PFGs is \( n! (n = \log_2 N) \) for length-\( N \) polar codes. Decoding schedules of BPL can be divided into parallel [11]–[14] and serial schedules [17], respectively. In parallel BPL decoding, \( L \) independent BP decoders operate in parallel (each BP decoder works on a unique PFG) and the optimal codeword with the minimum Euclidean distance to the received signals is selected from the \( L \) identified candidate codewords. However, parallel BPL decoding has very poor hardware utilization, especially for large list sizes. To avoid the high hardware consumption caused by the parallel architecture, the authors of [17] proposed a serial BPL decoding schedule, in which shuffling the input LLRs can be substituted for permutations of the factor graph stages. This hardware-friendly decoding strategy allows BPL decoding to reuse a single BP decoder at the cost of merely shuffling the input LLRs into a specific order for each PFG.

To improve the error-correcting performance of BPL decoding, numerous researchers have explored methods of optimizing the PFG selection, including empirical methods [11], [17], [33] and analytical methods [14]–[16]. It is noteworthy that the authors of [14] first derived the permutation gain for parallel BPL decoding, which provides the inspiration for analytically solving the optimal PFG selection. In view of hardware implementations, many works of BP decoders have been presented in [30], [34]–[39]. Compared to the classical single-column BP architectures [30], the SOA double-column bidirectional-propagation architecture [39] instantiates two processing element (PE) arrays and propagates the left-to-right and right-to-left messages simultaneously to improve the throughput. Moreover, the most challenging task for the BPL decoder is the implementation of flexible permutations since the PFG selection algorithms [14]–[16], [40] are generally dynamic, corresponding to varying code configurations or channel environments. Even if based on area-efficient serial decoding, the BPL decoder still needs to support the generation of flexible permutations by shuffling the input LLRs into a specific order for each PFG. A straightforward method is to utilize the Beneš network [41], [42], which is an optimal non-blocking network that can achieve any arbitrary permutation. However, the design space of permutations is \( n! \) instead of \( N! \) for length-\( N \) polar codes, and the control signals of the Beneš network are difficult to generate on-the-fly for each PFG. It is not efficient to adopt the Beneš network in the BPL decoder. In summary, there are thus two critical problems for the BPL decoder:

- How to select the optimal PFG set from \( n! \) PFGs for length-\( N \) polar codes?
- How to efficiently implement flexible permutations for BPL decoding in hardware?

It is further noteworthy that BPL decoding is a particular case of a generalized automorphism ensemble (AE) decoding, in which we can deploy the SC, SCL, or BP decoding on multiple PFGs to achieve ML performance of polar or Reed-Muller (RM) codes [43], [44]. Hence, the solutions to these two problems are significant for both BPL and for generalized AE decoding.

**Contributions:**

In this paper, we present the first BPL implementation, which solves the aforementioned two problems, i.e., the use of near-optimal PFG sets and the generation of flexible permutations. Our contributions comprise the following:

- We derive the block error probability of serial BPL decoding and present a criterion for determining the best PFG set. Then, we propose a sequential generation (SG) algorithm that can efficiently obtain a near-optimal PFG set. Simulations show that our BPL decoder with \( L = 32 \) achieves similar error-correcting performance to SCL with \( L = 4 \).
- We propose a hardware-friendly algorithm using low-complexity matrix decomposition to generate flexible permutation routings for all PFGs. To this end, we provide a mathematical model for permutations and demonstrate that the permutation routing of each PFG can be decomposed into a combination of \( n - 1 \) fixed subroutines. This decomposition process can be done online.
- We present the first hardware architecture of a BPL decoder, based on the double-column bidirectional-propagation scheme [39], that incorporates the aforementioned flexible permutation generator. To improve the throughput of the BPL decoder, we adopt a decoupled strategy that enables BP decoding and permutation generation to be executed simultaneously. It is noteworthy that our decoder can increase the list size arbitrarily without any additional area overhead. Synthesis results show that, for \( L = 32 \), our decoder can achieve a throughput of 25.63 Gbps with an area efficiency of 29.46 Gbps/mm\(^2\) at \( \text{SNR} = 4 \text{ dB} \), which outperforms the SOA BP and BPF decoders [20], [21], [38], [39], [45].

The remainder of this paper is organized as follows. Section II reviews the background of polar codes, BP decoding, and BPL decoding. Section III analyses the permutation gain for serial BPL decoding and presents a graph selection algorithm for a near-optimal PFG set. In Section IV, a hardware-friendly algorithm for any permutation generation is proposed. Section V presents our BPL decoder architecture with several advanced techniques. Section VI provides our implementation results and compares them with the SOA polar decoders. Finally, Section VII concludes this paper.

**II. Preliminaries**

**Notation:** Throughout this paper, we use the following symbol definitions. Boldface lowercase letters \( \mathbf{u} \) denote vectors, where \( u_i \) means the \( i \)-th element of \( \mathbf{u} \) and \( \mathbf{u}' \) denotes the sub-vector \( \{u_i, u_{i+1}, \ldots, u_j\}, i \leq j \). If \( i > j \), \( \mathbf{u}' = \emptyset \). Boldface uppercase letters \( \mathbf{B} \) denote matrices, where \( B_{ij} \) and \( b_j \) denote the element at the \( i \)-th row and \( j \)-th column of \( \mathbf{B} \) and the \( j \)-th column of \( \mathbf{B} \), respectively. In terms of the factor graph for polar codes with length \( N = 2^n \), we use \( \pi_o \), \([m_0, m_1, m_2, \ldots, m_{n-1}]\), and \([0, 1, 2, \ldots, n-1]\) to represent the original factor graph (OGF), its stages, and its stage order, respectively. Similarly, we use \( \pi \), \([m_{\pi_0}, m_{\pi_1}, m_{\pi_2}, \ldots, m_{\pi_{n-1}}]\), and \([\pi_0, \pi_1, \pi_2, \ldots, \pi_{n-1}]\) to denote any other PFG, its stages, and its stage order, respectively. If \( \mathcal{L} \) is a set of \( L \) PFGs
candidates, \( \{ \pi_0, \pi_1, \ldots, \pi_{L-1} \} \), \( |\mathcal{L}| = L \) means its cardinality. Note that all indices related to decoding start from 0. The hard decision function is defined as \( \text{HD}(x) = 1 \) if \( x < 0 \) and \( \text{HD}(x) = 0 \) if \( x \geq 0 \). We adopt the following parameters for polar codes, \( N \) is the code length, \( K \) is the number of message bits, \( R = K/N \) the code rate, \( P \) the number of CRC bits, \( K' = K + P \) the number of information bits with the CRC bits attached. The frozen and unfrozen bit set indices are denoted as \( \mathcal{F} \) and \( \mathcal{A} \), respectively, and we refer to a code as an \((N, K)\) polar code. As in this work we only consider polar codes that are concatenated with CRC codes, we use the term SCL decoding to refer to CRC-aided SCL decoding for brevity.

A. Construction and Encoding of Polar Codes

Given an input bit sequence \( u \), the encoded vector \( x \) is generated by \( x = u \cdot G_N \), where \( G_N = F^{\otimes n} \) denotes the Kronecker power of the kernel \( F = [1 \ 1] \). Based on the principle of channel polarization [1], the \( N \) bits in \( u \) correspond to \( N \) coordinated bit channels with different reliabilities, where the \( K' \) most reliable bit channels transmit unfrozen bits with CRC attached and the remaining \( N - K' \) bit channels transmit frozen bits, typically set to a value of 0. Note that the metric used to determine the bit channel reliability has an impact on \( \mathcal{A} \) and influences the performance of polar codes. For 5G NR [46], a universal reliability sequence is applied to formulate \( \mathcal{A} \) with \( K' \) bits for uplink (UL) and downlink (DL) channels. Besides, a novel polar code construction framework tailored to a given decoding algorithm based on a genetic algorithm (GenAlg) was introduced in [47], where populations of unfrozen sets evolve based on the error-correcting performance of a given decoder.

B. BP Decoding of Polar Codes on the Factor Graph

The BP algorithm is a classical iterative algorithm to calculate the marginal probability by the sum-product (SP) equations on a factor graph [48]. Motivated by BP decoding for RM codes, Arıkan first proposed BP decoding for polar codes on the generator matrix-based factor graph [49]. The OFG structure with three stages \([m_0 \ m_1 \ m_2]\) is shown in Fig. 1. Namely, an \((N, K)\) polar code is represented as an \( n \)-stage factor graph, and each stage has \( N/2 \) PEs. Two types of LLR messages (left-to-right \( R \) and right-to-left \( L \)) are propagated over PE candidates, \( \{ \pi_0, \pi_1, \ldots, \pi_{L-1} \} \), \( |\mathcal{L}| = L \) means its cardinality. Note that all indices related to decoding start from 0. The hard decision function is defined as \( \text{HD}(x) = 1 \) if \( x < 0 \) and \( \text{HD}(x) = 0 \) if \( x \geq 0 \). We adopt the following parameters for polar codes, \( N \) is the code length, \( K \) is the number of message bits, \( R = K/N \) the code rate, \( P \) the number of CRC bits, \( K' = K + P \) the number of information bits with the CRC bits attached. The frozen and unfrozen bit set indices are denoted as \( \mathcal{F} \) and \( \mathcal{A} \), respectively, and we refer to a code as an \((N, K)\) polar code. As in this work we only consider polar codes that are concatenated with CRC codes, we use the term SCL decoding to refer to CRC-aided SCL decoding for brevity.

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Reuse a BP decoder based on the OFG. This can be done as follows

\[ [m_0, m_1, \ldots, m_{p-1}, m_{p}, \ldots, m_{n-1}], \quad 0 \leq p \leq n, \quad (2) \]

where \( p \) denotes the number of fixed left stages. It is noticeable that the size of the design space of PFGs is reduced from \( n! \) to \((n-p)!\), which facilitates our derivations in Section III.

D. Permutation by Shuffling the Input LLRs

In [17], it is demonstrated that a one-to-one mapping exists between permutation of the factor graph stages and shuffling of the bit indices in the codeword. If we consider a node \( \oplus \) as a ‘0’ and a node \( \Leftarrow \) as a ‘1’ on the factor graph, we can derive the ‘0/1’ sequences that describe the factor graph from the binary expansion of the bit-index \( i \) for \( u_i \) and \( x_i \), as shown in the OFG of Fig. 1. Subsequently, Fig. 3 depicts the permutation of a PFG \( \pi_1 = [m_2, m_0, m_1] \) based on the input shuffling. Note that by permuting the factor graph stages, the positions of the nodes \( \oplus \) and \( \Leftarrow \) have been changed, i.e., the binary expansions of the bit indices for the input LLRs also have been changed. We can instantiate a routing based on these binary expansions to shuffle the input LLRs, which replaces permutations of the factor graph stages. After the above input shuffling, we use a single BP decoder based on the OFG to decode on different PFGs. Due to the varying optimal \( \mathcal{L} \) for different code configurations, it is significant for a BPL decoder to support generating the flexible input shuffling, which is discussed in Section IV.

III. PROPOSED GRAPH SELECTION ALGORITHM BASED ON THE GRAPH SELECTION GAIN

In this section, we derive the block error probability of serial BPL decoding and further propose the SG algorithm to obtain a near-optimal PFG set. Numerical results show that BPL decoding with the SG algorithm and \( \mathbb{L} = 8 \) can yield a similar performance as SCL with \( \mathbb{L} = 2 \) under different code rates of 5G NR polar codes. Subsequently, to fully show the potential of BP decoding, we employ the construction using the GenAlg [47] to allocate bit channels for BP decoding and apply the proposed near-optimal set. Simulations for this case illustrate that BPL decoding with \( \mathbb{L} = 32 \) achieves the error-correcting performance of SCL decoding with \( \mathbb{L} = 4 \).

A. Permutation Gain Analysis for BPL Decoding

Due to the introduced detection module in Fig. 2, the individual block error probability \( \Pr(E_i) \) for the \( l \)-th PFG \( \tilde{\pi}_l \in \mathcal{L} \) combines the miss rate \( \Pr(M_l) \) and the error-detection rate \( \Pr(D_l) \), which can be expressed as follows

\[ \Pr(E_i) = \Pr(M_l) + \Pr(D_l). \quad (3) \]

Considering the serial decoding schedule, we modify the derivation for the block error probability of BPL decoding \( \Pr(E_{\text{BPL}(\mathcal{L})}) \) in [14], as illustrated in (4)

\[ \Pr(E_{\text{BPL}(\mathcal{L})}) = \sum_{i=1}^{\mathbb{L}-1} \left( \Pr(M_i) \sum_{k=0}^{l-1} \Pr(D_k) \right) + \Pr(M_0) + \Pr(D_0), \quad (4) \]

where the list error probability \( \Pr(D_0) \) reveals the improvement in the error-correcting performance from list decoding. From (4) we also see that the probability of this term \( \Pr(D_0) \) decreases as the number of PFG candidates \( \mathbb{L} \) increases. If \( \mathbb{L} = 1 \), \( \Pr(E_{\text{BPL}(\mathcal{L})}) = \Pr(M_0) + \Pr(D_0) \). In serial BPL decoding, the detection module performs the CRC detection [52] rather than the minimum Euclidean distance used in parallel BPL decoding [11]. Note that the CRC detection makes the output codeword not necessarily maximum-likelihood decodable and it introduces the miss probability as discussed in (4).

Most PFG selection algorithms in [15–17], [40] are only concerned with developing an efficient metric to identify PFGs with the minimum \( \Pr(D_1) \). However, as indicated in (4), the list error probability is determined by the joint block error probability of the selected PFGs, rather than the individual \( \Pr(D_l) \) of each chosen PFG. Therefore, the task of finding the optimal \( \mathcal{L}^* \) that yields the lowest block error probability \( \Pr(E_{\text{BPL}(\mathcal{L})}) \) has transformed into an optimization problem to minimize (4), as shown in (5)

\[ \mathcal{L}^* = \arg \min_{\mathcal{L}} \Pr(E_{\text{BPL}(\mathcal{L})}), \text{ s.t. } |\mathcal{L}| = \mathbb{L}. \quad (5) \]
It is noteworthy that $\Pr(M_i)$ of (4) is a constant decided only by the CRC polynomial and is independent of the PFG index $l$. Therefore, we refer to them as $\Pr_M$ in the following discussion. To streamline the optimization problem in (5), as mentioned in Section II.C, we empirically default $\bar{\pi}_0 = \pi_o$ since the OFG always yields the lowest block error probability. We then reformulate (4) based on probabilities that are conditioned on $\Pr(D_0)$ to reflect the PFG selection gain in (6)

$$\Pr(E_{\text{BPL}(\mathcal{L})}) = \Pr_M + \Pr(D_0).$$

$$\Pr_M \cdot \sum_{l=1}^{L-1} \Pr \left( \bigcap_{k=1}^{l-1} D_k \bigg| D_0 \right) + \Pr \left( \bigcap_{l=1}^{L-1} D_l \bigg| D_0 \right) \quad (6)$$

Subsequently, we use $\mathcal{L}' = \mathcal{L}\setminus \pi_o$ to denote the remaining PFG set and further simplify (7) into (5) based on (6)

$$L' \approx \arg\min_{L'} \Pr(E_{\text{BPL}(\mathcal{L})}|D_0) \approx$$

$$\arg\min_{\mathcal{L}'} \left( \Pr_M \cdot \sum_{l=1}^{L-1} \Pr \left( \bigcap_{k=1}^{l-1} D_k \bigg| D_0 \right) + \Pr \left( \bigcap_{l=1}^{L-1} D_l \bigg| D_0 \right) \right)$$

where $\Pr_M(\mathcal{L}')$ is a constant $\Pr_M$ if $L = 2$. In order to obtain the optimal $\mathcal{L}'$ that minimizes (7), we factorize $\Pr_M(\mathcal{L}')$ and $\Pr_{\text{PFG}(\mathcal{L}')}$, as shown in (8), where $\Pr_M(\mathcal{L}')$ and $\Pr_{\text{PFG}(\mathcal{L}')}$, both have a similar sequential structure. In the case of $L = 2$, (7) is simplified to $\Pr(D_1|D_0) + \Pr_M$, and we find $\bar{\pi}_1$ by minimizing $\Pr(D_1|D_0)$. As $L$ increases from 2 to 3 and we reserve the selected $\{\bar{\pi}_0 \bar{\pi}_1 \bar{\pi}_2\}$, we can consecutively obtain $\bar{\pi}_2$ by minimizing $\Pr(D_2|D_0, D_1)$. Note that when $L = 3$, $\{\bar{\pi}_0 \bar{\pi}_1 \bar{\pi}_2\}$ selected by the above method is only an approximation of (7), which implies that we sequentially obtain $\bar{\pi}_1$ and $\bar{\pi}_2$ following a greedy algorithm.

$$\Pr_{M(\mathcal{L}')} = \Pr_M:\left( 1+\Pr(D_1|D_0) \cdot \left( 1 + \Pr \left( D_{L-2} \bigg| \bigcap_{l=0}^{L-3} D_l \right) \right) \right),$$

$$\Pr_{\text{PFG}(\mathcal{L}')} = \Pr(D_1|D_0) \cdots \Pr \left( D_{L-1} \bigg| \bigcap_{l=0}^{L-2} D_l \right),$$

(8)

In conclusion, we employ a greedy algorithm applied to the sequential structure of (8) when selecting the $l$-th PFG for $L$. Specifically, we always choose the $\bar{\pi}_1$ that can minimize $\Pr(D_l|D_0, D_1, \ldots, D_{l-1})$, based on the previous $l-1$ selected PFGs, $l \in [1, L]$. This method decomposes the issue of minimizing the joint block error probability into $L-1$ consecutive minimization problems of conditional probabilities, which provides a near-optimal result solution for (7).

**B. Sequential Generation (SG) Algorithm for Graph Selection**

In this section, we propose a graph selection algorithm called SG, which can sequentially perform $\arg\min_{\mathcal{L}} \Pr(D_l|D_0, D_1, \ldots, D_{l-1})$ to obtain $\bar{\pi}_l$ for $\mathcal{L}$, $l \in [1, L]$. In addition, by incorporating the conditional probability $\Pr(D_0)$ from (4) to (7), we observe that $\Pr(E_{\text{BPL}(\mathcal{L})}|D_0) \approx \Pr(E_{\text{BPL}(\mathcal{L})})$. Thus, we can use a relatively small dataset to determine the remaining near-optimal $\bar{\pi}_l$ using Monte-Carlo simulations.

To realize the SG algorithm, we first generate a dataset $\mathcal{D}$ containing $|\mathcal{D}|$ received vectors $y$ that fail to pass the CRC detection under BP decoding on $\pi_o$. Let $P$ denote the search space of PFGs. As mentioned in Section II.C, the authors of [17] found that the PFGs which fix more left stages and only permute the right-most side of the graph tend to have a
better error-correcting performance. Hence, we adjust $p$ in (2) to reasonably decrease the design space of $\mathcal{P}$ to $(n-p)!$ PFGs and simplify computational complexity. Subsequently, for each PFG candidate, we evaluate its block error rate (BLER) performance in BPEvaluate() for all received words in $\mathcal{D}$. The current frame is recorded as ‘1’ in $\mathbf{T}$ if decoding fails, and $\mathbf{T}$ is a dynamic matrix with the initial dimension of $(|\mathcal{P}| \times |\mathcal{D}|)$. In Algorithm 1, the first element of $\mathcal{L}$ is set to $\pi_0$. For the $i$-th PFG in $\mathcal{P}$ and the $j$-th received codeword in $\mathcal{D}$, the success/failure of the CRC detection is marked as ‘0/1’ in $\mathbf{T}(i, j)$ depending on if decoding succeeded or not. In order to further populate $\mathcal{L}$, we use the function selectBestList() to return the index $i^\ast$ that corresponds to the minimum weight row in $\mathbf{T}$, which is equivalent to minimizing $\Pr(D_l|D_0, \ldots, D_{l-1})$. After storing $\mathcal{P}(i^\ast)$ into $\mathcal{L}(l)$, the function updateDataset() dynamically updates $\mathbf{T}$ and $\mathcal{D}$ by deleting the columns corresponding to the 0s in $\mathbf{T}(i^\ast,:)$ and corresponding samples in $\mathcal{D}$ to only keep the erroneous cases. The above operations (lines 4 – 7 in Algorithm 1) are repeated for $L - 1$-times until filling $\mathcal{L}$.

**Algorithm 1: SG Process**

| Input: $\mathcal{D}$, $\mathcal{P}$, $L$ |
| Output: $\mathcal{L}$ |
| // default $\pi_0$ is the 0-th element of $\mathcal{L}$ |
| $\mathcal{L}(0) \leftarrow \pi_0$; |
| for $i = 0$ to $|\mathcal{P}| - 1$ do |
| // record the failed frames as 1s |
| $\mathbf{T}(i,:)$ ← BPEvaluate($\mathcal{P}(i), \mathcal{D}$); |
| // generate the $\mathcal{L}$ |
| for $l = 1$ to $L - 1$ do |
| // find the minimum $\Pr(D_l|D_0, \ldots, D_{l-1})$ |
| $i^\ast$ ← selectBestList($\mathcal{P}$); |
| $\mathcal{L}(l)$ ← $\mathcal{P}(i^\ast)$; |
| // delete the corrected errors |
| $\{\mathbf{T}, \mathcal{D}\}$ ← updateDataset($\mathbf{T}$, $\mathcal{D}$, $i^\ast$); |

C. Numerical Results of the Proposed Algorithm

Fig. 4 compares the BLER performance of BP decoding, permuted BP (PBP) decoding [17], SCL decoding [53], and the proposed BPL decoding with the SG algorithm (BPL-SG) for 5G UL polar codes with $N = 1024$ and $R \in \{\frac{1}{4}, \frac{1}{2}, \frac{3}{4}\}$, where all iterative decoders have the same $I_{\text{max}} = 50$. In all following captions, the tailored “-L” denotes the employed list size. For each case (i.e., SNR = -1 dB for $R = \frac{1}{4}$, SNR = 2.5 dB for $R = \frac{1}{2}$, and SNR = 5.5 dB for $R = \frac{3}{4}$), we generate a relatively small dataset $\mathcal{D}$ with $10^6$ samples that fail to pass the CRC detection under BP decoding on $\pi_0$. However, as length-1024 polar codes contain 10! PFGs, it is impractical to simulate all of them. In order to make a reasonable trade-off between computational complexity and performance, we set $p = 4$ in (2) and fix the left stages as $[m_0 \ m_1 \ m_2 \ m_3]$ to reduce the cardinality of $\mathcal{P}$, which now contains only 720 PFG candidates. Numerical results from simulating over AWGN channels with binary phase-shift keying (BPSK) modulation show that BPL-SG-32 provides a 0.1 dB improvement in comparison with PBP-32 at BLER $= 10^{-3}$, and this improvement increases to 0.2 dB for $R = \frac{1}{4}$. When $L$ increases to 128, BPL-SG further approaches the performance of SCL-4. To show the advantage of a serial schedule in terms of computational complexity, we compare the average number of iterations $I_{\text{avg}}$ for two schedules that both use the SG algorithm in Fig. 5. Note that there is no termination within each single BP decoder to make a fair comparison. For $L = 128$, a serial architecture can reduce around 99.2% of the iterations, demonstrating the superiority of the serial schedule for hardware implementation.

$$g_{\text{CRC-11}}(x) = x^{11} + x^{10} + x^9 + x^5 + 1.$$ (9)

In addition to the 5G NR code construction that is unfriendly to BP decoding, we also consider the GenAlg construction [47] to fully show the potential of BP decoding. Fig. 6 illustrates...
the BLER performance of BP, SCL, and BPL-SG decoding for (1024,512) polar codes with the GenAlg and 5G NR constructions. The CRC-11 polynomial from the 5G NR standard, as shown in (9), is adopted for both constructions. BPL-SG-32 under the GenAlg construction approaches the performance of SCL-4, and BPL-SG-128 under the GenAlg construction surpasses SCL-4 by 0.2 dB at BLER = \(10^{-4}\).

IV. PROPOSED ALGORITHM OF FORMULA-BASED PERMUTATION GENERATION

As mentioned in Section II.D, permutations of the factor graph stages can also be substituted efficiently by only shuffling the input LLRs to avoid instantiating multiple BP decoders with different factor graph architectures and greatly facilitates the hardware implementation. However, since a variety of shuffling patterns need to be generated to realize a single shuffling set \(\mathcal{L}\) and since different code configurations require different shuffling sets, the implementation of the corresponding flexible LLR routing is challenging. In this section, we propose a hardware-friendly algorithm to generate these flexible routings (i.e., permutations). We prove that the routing of any PFG can be decomposed into a combination of \(n-1\) fixed sub-routings, as shown in Fig. 7. The complicated hardware routing issue can thus be optimized as a matrix decomposition.

A. Mathematical Model for Permutations

First, we create a model for permutations to solve the hardware routing problems with a matrix decomposition. For length-\(N\) polar codes, if the nodes \(\oplus\) and \(\boxdot\) in PFGs are represented by ‘0’ and ‘1’ respectively, any PFG can be mapped into a unique \(N \times n\) binary matrix, in which the ‘0/1’ sequence in each row corresponds to the binary expansion of the bit-index for the input LLRs. For example, we use \(B = [b_{n-1} b_{n-2} \ldots b_1 b_0]\) to denote the OFG of Fig. 1 (contrary to its stage order \([0 1 2 \ldots n-1]\)), and \(b_i\) is a length-\(N\) binary column vector expanded as

\[
b_i = \begin{bmatrix} 2^{n-i-1} \text{ pairs of } [0 1] \\ 1 \times 2^i \end{bmatrix}, \quad i \in [0, n),
\]

where each 0 or 1 is an all-0 or all-1 row vector of length-\(2^i\). For any PFG \(\pi\), the corresponding binary matrix \(B_\pi\) can be written as \(B_\pi = [b_{\pi_{n-1}} b_{\pi_{n-2}} \ldots b_{\pi_1} b_{\pi_0}]\), and (11) shows the examples of \(\pi_0\) and \(\pi_1\) of Fig. 1 and Fig. 3.

\[
B = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}, \quad B_{\pi_1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}.
\]

Consequently, the model for permutations based on the input shuffling can be derived as follows

\[
B_\pi^T \cdot V_\pi = B^T \rightarrow \begin{cases} b_{\pi_{n-1}}^T \cdot V_\pi = b_{n-1}^T, \\ \vdots \\ b_{\pi_1}^T \cdot V_\pi = b_1^T, \\ b_{\pi_0}^T \cdot V_\pi = b_0^T. \end{cases}
\]

where \(V_\pi\) is the shuffling matrix to represent the targeted routing in hardware. Namely, as shown in Fig. 7, \(B_\pi\) can be multiplied by the corresponding \(V_\pi\) to obtain \(B\). Hence, the above problem has been modelled as how to use a unified mathematical formula to express \(V_\pi\).

B. Decomposition and Properties of \(V_\pi\)

Theorem 1. For any PFG \(\pi\), the shuffling matrix \(V_\pi\) which satisfies \(B_\pi^T \cdot V_\pi = B^T\) can be decomposed into a combination of \(n-1\) fixed sub-shuffling matrices \(V_{i-1,i}, i \in [1, n)\) for length-\(N\) polar codes.

First, we provide the explicit expression for \(n-1\) sub-shuffling matrices \(V_{i-1,i}, i \in [1, n)\) for length-\(N\) polar codes.
where \( V_{i-1,i} \) divides the input \( b \) into \( 2^{n-i-1} \) groups of equal length \( 2^{i+1} \) and shuffles based on 4 sub-vectors within each group. For an intuitive understanding of Theorem 1, we use Fig. 8 to illustrate a straightforward example of length-16 polar codes, which comprises 3 sub-shuffling matrices \( \{V_{0,1}, V_{1,2}, V_{2,3}\} \) and 4 binary column vectors \( \{b_0, b_1, b_2, b_3\} \) corresponding to (10) and (13). Each sub-shuffling matrix describes a unique sub-routing in hardware. Note that, due to the recursive construction of polar codes, \( n-1 \) sub-routings for length-\( N \) polar codes can be decomposed into two independent copies of \( n-2 \) sub-routings for length-\( N/2 \) polar codes, as shown in Fig. 8. Before the proof of Theorem 1, it is useful to introduce additional lemmas.

**Lemma 1.** \( \forall i \in [1, n), V_{i-1,i} \) is an involutory matrix, i.e., \( V_{i-1,i} = V_{i-1,i} \), \( V_{i-1,i} \cdot V_{i-1,i} = 1_n \).

Based on the features of (13), the proof is straightforward.

Then, we can further derive (14) as implied in Fig. 8

\[
\begin{align*}
\begin{pmatrix}
b^T_i \cdot V_{i-1,i} & = b^T_i, \\
\end{pmatrix} & \forall i \in [1, n].
\end{align*}
\]

**Lemma 2.**
\[
\begin{align*}
b^T_i \cdot V_{i,j} = b^T_j, & \forall i, j \in [0, n).
\end{align*}
\]

**Proof.** We define \( V_{i,j} = V_{i,i+1} \cdot V_{i+1,i+2} \cdot \ldots \cdot V_{j-1,j}, \forall i, j \in [0, n), i < j \) and let \( V_{i,j} = I_N, \forall i, j \in [0, n), i = j \). Based on (14), it can be verified that \( b^T_i \cdot V_{i,j} = b^T_i \cdot V_{i,i+1} \cdot V_{i+1,i} = b^T_i \cdot V_{i+1,j} = \ldots = b^T_j \). For \( i \geq j \), a similar proof can be formulated.

**Lemma 3.** \( \forall i, j, k \in [0, n), i \neq j, k \neq i, (16) \) holds.

\[
b^T_k \cdot V_{i,j} = \begin{cases} b^T_i & \text{if } k \notin [\min(i,j),\max(i,j)], \\
\begin{pmatrix} b^T_{k+\text{sgn}(i-j)} \\ 0 \end{pmatrix} & \text{if } k \in [\min(i,j),\max(i,j)].
\end{cases}
\]

An intuitive example for Lemma 3 is visible from Fig. 8: Using Lemma 2, when calculating \( b^T_0 \cdot V_{0,2} = b^T_0 \cdot V_{0,1} \cdot V_{1,2} \), we can simply permute \( b^T_0 = [0 \ldots 0 \ldots 1 \ldots 1]^T \) through \( V_{0,1} \) and \( V_{1,2} \) and find the result still equals to \( b^T_0 \) since \( 3 \notin [0, 2] \). Besides, using Lemma 1 and 2, \( b^T_i \cdot V_{0,2} = b^T_i \cdot V_{0,1} \cdot V_{1,2} = b^T_0 \cdot V_{1,2} = b^T_0 \) since \( 1 \in [0, 2] \) and \( \text{sgn}(0 - 2) = -1 \).

**Proof.** If \( k \notin [\min(i,j),\max(i,j)] \), Lemma 3 can be verified by Lemma 1, (10), and (13). If \( k \in [\min(i,j),\max(i,j)] \), we need to distinguish two cases: for \( i < j \), \( b^T_k \cdot V_{i,j} \) can be represented by (17) and therefore

\[
b^T_k \cdot V_{i,j} = b^T_k \cdot V_{i,i+1} \cdot V_{i+1,i+2} \ldots V_{j-1,j} = b_{k-1} \cdot V_{k,k+1} \ldots V_{j-1,j} = b^T_{k-1}.
\]

For \( i > j \), the proof for \( b^T_k \cdot V_{i,j} = b^T_{k+1} \) is similar.

**Lemma 4.** For any \( B_\pi \), after the matrix multiplication by \( V_{i-1,i}, \forall i \in [1, n), B_\pi \) never contains two identical columns.

**Proof.** \( \forall i \in [1, n), let i - 1 = \pi^1, i = \pi^0 \), using Lemma 1 and Lemma 3, it is apparent that

\[
\begin{align*}
B_\pi^T \cdot V_{i-1,i} & = \left[ b_{\pi^1}^T \ldots b_{\pi^0}^T \ldots b_{\pi^1}^T \ldots b_{\pi^0}^T \right] \cdot V_{i-1,i} \\
& = \left[ b_{\pi^1}^T \ldots b_{\pi^0}^T \ldots b_{\pi^1}^T \ldots b_{\pi^0}^T \right] \end{align*}
\]

Hence, for any \( \pi \), the matrix multiplication by any \( V_{i-1,i}, i \in [1, n) \) is equivalent to swapping two columns of \( B_\pi \).

**Lemma 5.** For any \( B_\pi \), if executing a right-to-left column-wise transformation to realize \( B_\pi \to B \), the previously matched columns are never influenced by the current shuffling matrix.

**Proof.** \( \forall i \in [0, n) \), there are \( i \) matched columns on the right and \( n - i \) un-matched columns on the left of \( B_\pi \) compared with \( B \), as shown in (19)

\[
B_{\pi_{ij}} = \begin{pmatrix} [b_{\pi^0_j} \ldots b_{\pi^0_1} b_{\pi^1_j} \ldots b_{\pi^1_0}] \\
\end{pmatrix} \]

\[
\begin{pmatrix} \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \end{pmatrix}
\]

In accordance with Lemma 4, the un-matched columns in \( B_\pi \) never contain any element of \( [b^T_{k-1} \ldots b^T_0] \). Therefore, we can derive that \( \pi^1_{ij} > i - 1 \) and \( b_{\pi^1_{i-1}} \cdot B_{\pi_{ij}} \cdot V_{\pi^1_{ij},i} = b_{\pi^1_{i+1}} \cdot B_{\pi_{ij}} \cdot V_{\pi^1_{ij},i} \) always holds. Besides, combined with Lemma 1, we further obtain \( b_{\pi_{i+1}}^T \cdot V_{\pi_{ij},i} = b_{\pi_{i+2}}^T \) and let \( \pi_{i+1} \) denote the original \( \pi \) after \( i + 1 \) transformations. Hence, the proof of Lemma 5 has been completed.

In conclusion, combined with the aforementioned Lemma 1-5, the proof of Theorem 1 is provided below.

**Proof of Theorem 1.** The decomposition process of any permutation is illustrated in (21), which clearly presents how to generate the shuffling matrix \( V_\pi \).

\[
\begin{align*}
B_{\pi_{i+1}}^T \cdot V_{\pi^0_{i+1},0} & = B_{\pi_{i+1}} = \begin{pmatrix} b_{\pi^0_{i+1}} \ldots b_{\pi^0_1} b_{\pi^0_0} \end{pmatrix} \\
B_{\pi_{i+1}}^T \cdot V_{\pi^1_{i+1},1} & = B_{\pi_{i+2}} = \begin{pmatrix} b_{\pi^1_{i+1}} \ldots b_{\pi^1_2} b_{\pi^1_1} b_{\pi^1_0} \end{pmatrix} \\
& \ldots \\
B_{\pi_{n-1}}^T \cdot V_{\pi_{n-1},n-1} & = B^n = \begin{pmatrix} b_{n-1} \ldots b_1 b_0 \end{pmatrix}.
\end{align*}
\]
where we rewrite $\pi^0$ as $\pi_s^0$ to obtain a unified mathematical notation and further simplify the process of (21) by (22)

$$B^{T}_{s} \cdot V_{\pi} = B^{T}_{s} \cdot V_{\pi}^{0,0} \cdot V_{\pi,s_{1},1} \cdots V_{\pi,n-1,n-1}$$

$$= B^{T}_{s} \cdot \prod_{i=0}^{n-1} V_{\pi,i,i}$$

in which we obtain the final expression for $V_{\pi}$ as

$$V_{\pi} = \prod_{i=0}^{n-1} V_{\pi,i,i}$$

where $V_{\pi,i,i}$ can be expressed as a product from $n-1$ sub-shuffling matrices $V_{i-1,i}, i \in [1,n]$, defined in (13) are loaded to it. The vector $s$ stores the sequences of sub-shuffling indices that generate $\pi^i_s$, as in (23) and are found during the decomposition of the shuffling. To fill $s$, we run a for loop in lines 3 – 8 of Algorithm 2 to perform the right-to-left column-wise transformation as shown in (21). Performing the $i$-th loop is equivalent to updating the PFG by $V_{\pi,i,i}$ (i.e., $B_{\pi_s,i} \rightarrow B_{\pi_{s+1,i}}$ in (21)). The functions of Lemma 2 and Lemma 3 are implemented by the updateStage() function as shown in Algorithm 3. Note that for length-$N$ polar codes, we can fill $s$ completely within $n$ steps to generate $V_{\pi}$.

Subsequently, we run subRouting() as shown in Algorithm 4 to permute the input LLRs $R_0$ (or $L_n$) based on the stored $s$. This function multiplies $R_0$ by $V_{\pi,i,i}$ that can be decomposed into a product of $|\pi^i_s - i|$ sub-shuffling matrices. Finally, we transmit the permuted $R_0$ to the BP decoder based on the OFG. The corresponding implementation is further explained in Section V.B.

C. A Hardware-Friendly Algorithm by Matrix Decomposition

Note that the above derivation in Section IV.B helps to interpret how to generate $V_{\pi}$ from an algorithm perspective. From a hardware perspective, the generation process is useful as it enables the BPL decoder to gradually permute the input LLRs into a specified order that is equivalent to multiplying by $V_{\pi}$ of (23). An intuitive example is shown in Fig. 9: To generate $\pi_1 = [m_2, m_0, m_1]$ of length-$8$ polar codes, we get $V_{\pi_1} = V_{1,2} \cdot V_{0,1}$ based on (23). Then, we permute $u$ and $x$ through two routings corresponding to an application of $V_{1,2}$ followed by $V_{0,1}$, which is equivalent to directly passing through the routing of Fig. 3. Herein, the generation of $V_{\pi}$ and the process of shuffling the input LLRs are summarized in Algorithm 2.

Algorithm 2: Generation of Permutations by A Matrix Decomposition

Input: $R_0$, PFG = $[\pi^0, \pi^1, \ldots, \pi^{n-1}]$, and OFG = $[0:1, \ldots, n-1]$

Output: $R_0$

// initialization
1 $s \leftarrow \{0\}$; // store $\pi^0_s$, $\pi^1_s$, ..., $\pi^{n-1}_s$
2 $n-1$ sub-shuffling matrices
3 $V_{\pi} = \{V_{0,1} V_{1,2}, \ldots, V_{n-2,n-1}\}$
4 // generate $V_{\pi}$
5 for $i = 0$ to $n-1$
6 $s = \text{PF}_G[i]$; // current column $\pi^i_s$
7 $e = \text{OFG}[i]$; // aimed column $i$
8 // update PFG by $V_{\pi,e}$
9 for $j = i$ to $n-1$
10 $\text{PF}_G[j] \leftarrow \text{updateStage}(\text{PF}_G[j], s, e)$
11 $s[i] = s$; // store the current $\pi^i_s$
12 // execute $V_{\pi}$ to permute input LLRs
13 for $i = 0$ to $n-1$
14 $R_0 \leftarrow \text{subRouting}(R_0, V_{\pi}, s[i], \text{OFG}[i])$

Algorithm 3: updateStage()

Input: $\pi^{in}, s, e$

Output: $\pi^{out}$

1 if $\pi^{in} = s$
2 $\pi^{out} = e$; // Lemma 2
3 else if $\pi^{in} \in \{\min(s,e), \max(s,e)\}$ and $s \neq e$
4 $\pi^{out} = \pi^{in} + \text{sgn}(s - e)$; // Lemma 3
5 else
6 $\pi^{out} = \pi^{in}$; // keeps constant

Algorithm 4: subRouting()

Input: $R_0$, $V_{\pi}$, $s, e$

Output: $V_{\pi}$

1 if $s < e$
2 for $i = s$; $i <= e - 1$; $i + +$
3 $R_0[i] = R_0[T^T_s \cdot V_\pi[i]]$
4 else if $s > e$
5 for $i = s - 1$; $i <= e$; $i - -$
6 $R_0[i] = R_0[T^T_s \cdot V_\pi[i]]$

Fig. 9. Shuffling the input LLRs based on a matrix decomposition for $\pi_1 = [m_2, m_0, m_1]$. 

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V. PROPOSED BPL DECODER ARCHITECTURE

In this section, we present the architecture of our BPL decoder, which is the first hardware implementation of a BPL decoder for polar codes to the best of our knowledge. Fig. 10 illustrates the overall hardware architecture, which comprises a double-column bidirectional-propagation BP unit (BPU) [39], a permutation generator unit (PGU) as proposed in the previous section to generate flexible permutations, a termination and detection unit (TDU), a recovery module, and a controller.

A. Architecture Overview

For the underlying BPU, we employ the SOA double-column bidirectional-propagation architecture [39]. The dataflows of R- and L-messages are performed simultaneously, which means that R-messages at the j-th stage and L-messages at the (n−j)-th stage are calculated in the same clock cycle (CC). We store the input LLRs R0 and Ln in the memory RO and the memory LN, respectively. The PGU shuffles the input LLRs according to Algorithm 2 to generate the shuffled input LLRs R0’ and LN’ for L PFGs. Same as [39], the proposed decoder reduces the number of CCs per internal iteration from n to n−1 by removing the calculation of RN and LN messages. Besides, we use a sign-assisted (SA) termination strategy [22], [37] to check the sign convergence of the internal results. The SA strategy terminates decoding when hard decisions in the BPU are identical in three consecutive iterations, as shown in the termination module on the right side of Fig. 10. Finally, a detection module performs the CRC detection to judge whether output the current decoded û or decode on a new PFG further, which is discussed in Section V.C.

B. Permutation Generation Unit (PGU)

1) Hardware Architecture

Based on the shuffling matrix derived in Section IV, we implement a low-complexity permutation network PGU for the BPL decoder, which comprises a basic shuffling unit (BSU), two registers for R0 and Ln, and some MUXes. For the BSU shown in Fig. 11, we instantiate n−1 fixed sub-routings (Vn−1,i, i ∈ [1, n)) to realize all the required basic shuffling. All the stage orders of the proposed near-optimal PFG set \( L ([\pi^0_0, \pi^1_1, \ldots, \pi^{n-1}_i], i \in [0, L_n]) \) from the SG algorithm in Section III.B) is generated offline and stored in the PFG memory. The inputs of the BSU are the NQ-bit initial input LLRs (R0 or Ln, and each LLR is quantized as Q bits) to be shuffled and the PFG index l of the selected PFG. First, the controller of the BSU uses n CCs to obtain the set s of Algorithm 2 based on the output from the PFG memory, i.e., the stage orders of \( \pi_l \). Subsequently, the BSU executes Algorithm 4 step by step and controls the MUX to store the correct shuffled results into registers. Note that, in order to make a trade-off between the hardware complexity and the latency of the permutation, we only perform one sub-routing per CC to shuffle the input LLRs. For example, to realize V1,5, we decompose it as V1,2, V2,3, V3,4, and V4,5 to sequentially perform the desired permutations in 4 CCs. This decomposition process means that the latency for the permutation generation of any PFG is varying, as shown in (24),

\[ L_\pi = \sum_{i=0}^{n-1} |\pi^i_{s_i} - i| + n, \]  

(24)

where \( \pi^i_{s_i} \) comes from (23). The maximum latency of the BSU is \( L_\pi = n \cdot (n-1) / 2 + n \) CCs when the PFG is \([n-1 n-2 \ldots 1 0]\).

2) Comparison With the Beneš Network

To highlight the advantage and significance of our permutation network, we reproduce a classical Beneš network [41] illustrated in Fig. 12 to make a fair comparison. The number of inputs for a regular Beneš network is a power of two (N = 2^n). It has 2n−1 stages, each with N/2 switches of size 2 × 2. However, due to lack of an explicit method to generate control signals for PFGs in the Beneš network on-the-fly, for each \( \pi_l \) in \( L \), one would need to store \( N \cdot (2n-1) / 2 \) bits in the control memory to configure the ‘BAR’ or ‘CROSS’ states of each 2 × 2 switch, as shown in dashed red lines in Fig. 12. It is obvious to see that the area of the control memory in the Beneš network linearly grows with the maximum list size.

Synthesis results show that in Table I, for length-1024 polar codes, the area overhead of our flexible permutation generator under different list sizes is only 0.076 mm^2 using 28 nm FD-SOI. This network can support and generate an arbitrary number...
of PFG candidates without any area overhead. Compared to the Beneš network, our work has an \{86.9\% 96.3\%\} smaller area when \(L = 8\) and \(L = 32\), respectively. In terms of the permutation latency, the average \(L_\pi\) of all \(10^9\) PFGs is 32.5 CCs, and the maximum \(L_\pi\) is 55 CCs, which is higher than that of the Beneš network. However, to alleviate this issue, we propose an optimized decoupled decoding schedule well-suited for the serial architecture, which is discussed in detail in Section VD.

C. Termination and Detection Module (TDU)

The TDU is integrated into the decoder and responsible for terminating the decoding once it has converged and for performing the CRC detection between BP decoding. As described in Section V.A, we adopt the SA strategy [22], [37] to terminate the decoding if the hard decisions in the BPU are identical in three consecutive iterations. Subsequently, if passing the termination module in Fig. 10 or achieving \(I_{\text{max}}\) (as the green SA shows in Fig. 13), the BPL decoder requires 1 CC to calculate the final HD results \(\hat{u}'\). Since the decoded codeword \(\hat{u}'\) is permuted, to perform the CRC detection, we transform \(\hat{u}'\) to \(\hat{u}\) with the natural order in the recovery module. Note that this transformation is only the inverse process of the permutation generation in Section V.B, but the bit-width of this permutation network is only \(N\)-bit instead of \(NQ\)-bit. The latency of recovering \(\hat{u}\) is \((L_\pi - n)\) CCs. If the CRC detection succeeds, \(\hat{u}\) is output from our BPL decoder.

D. Optimized Decoding Schedule

To improve the throughput of the BPL decoder, we need to avoid the influence of the latency from the proposed permutation network. To this end, we propose an optimized decoding schedule which decouples the BPU, PGU, and the recovery modules with pipeline registers to allow them to work in parallel. First, when the BPU works on \(\tilde{\pi}_i, l \in [0, L - 1]\), the PFG is activated to shuffle the input LLRs for the next PFG \(\tilde{\pi}_{i+1}\). Since there are two kinds of the input LLRs in BP decoding (\(R_0\) and \(L_n\)). We use the module in Fig. 11 to shuffle \(R_0\) and \(L_n\) one after another in the same hardware. The detailed timing schedule of the proposed BPL decoder is illustrated in Fig. 13. To distinguish the shuffled input LLRs for different PFGs, we denote \(R_0, \tilde{\pi}_i, L_n, \tilde{\pi}_{i+1}\) as the permuted input signals \(R_0'\) and \(L_n'\) for \(\tilde{\pi}_i\). When the BPL decoder performs BP decoding on \(\tilde{\pi}_i, l \in [0, L - 1]\), after the PFG has already generated \(R_0, \tilde{\pi}_{i+1}\) and \(L_n, \tilde{\pi}_{i+1}\), these two signals are temporarily stored into the register \(R_0\) and the register \(L_n\) that are marked with a dark grey background in Fig. 10. Once BP decoding on \(\tilde{\pi}_i\) passes the termination module, the memory \(R_0\) and the memory \(L_n\) are updated by the register \(R_0\) and the register \(L_n\) to output \(R_0, \tilde{\pi}_{i+1}\) and \(L_n, \tilde{\pi}_{i+1}\) as \(R_0'\) and \(L_n'\) for the next BP decoding on \(\tilde{\pi}_{i+1}\).

Moreover, as said in Section V.C, the recovery from \(\hat{u}'\) to \(\hat{u}\) also harms the throughput of the BPL decoder, since the inverse permutation operations come at the cost of \(L_\pi - n\) CCs. To deal with this issue, we further decouple the recovery module from the decoding schedule. This decoupled decoding schedule allows the BPU, the PGU, and the recovery modules with pipeline registers to allow them to work in parallel. First, when the BPU works on \(\tilde{\pi}_i\) in parallel. Once \(\tilde{\pi}_i\) passes the CRC detection on \(\tilde{\pi}_k\) in Fig. 13. When passing the CRC detection on \(\tilde{\pi}_k\), the BPL decoder terminates the decoding on \(\tilde{\pi}_{k+1}\) and the permutation generation on \(\tilde{\pi}_{k+2}\).

VI. IMPLEMENTATION RESULTS

In this section, we present the synthesis results for our BPL implementation. All synthesis results are based on 28 nm FD-SOI technology in the typical-typical corner, and we use timing constraints that are not achievable to maximum the operating frequency for our design. A comparison with the SOA polar decoders is also provided.

A. Quantized Performance

In Fig. 14, under the GenAlg construction, we present the BLER performance and \(I_{\text{avg}}\) of our BPL decoder using floating-point and fixed-point (2’s complement). Let \(Q_n, q_f\) denote a fixed-point number with one sign-bit, \(q_i - q_f - 1\) integer bits, and \(q_f\) fractional bits. We adopt \(Q_{7.2}\) for the LLRs in Fig. 14. Numerical results show that \(Q_{7.2}\) almost approaches the floating-point performance of OMS polar decoding with \([\tilde{\beta}_1, \tilde{\beta}_2] = [0.25, 0]\) providing a well-balanced trade-off between the error-correcting performance and hardware complexity. For the \(I_{\text{avg}}\) of our BPL decoder, the influence of the list size is mainly reflected in the low SNR regions, which achieves 47.8 and 98.5 iterations for \(L \in \{32, 128\}\) at \(SNR = 2.0\) dB, respectively. However, as SNR increases, the \(I_{\text{avg}}\) of the BPL decoder converges rapidly to that of the BP decoder, which achieves \(I_{\text{avg}} = 5.81\) for \(L \in \{32, 128\}\).
Fig. 13. Timing schedule of the proposed BPL decoder, which decodes successfully on $\hat{\pi}_k$.

Fig. 14. BLER comparison between floating-point and fixed-point and $I_{\text{ave}}$ of the BPL decoder equipped with the proposed near-optimal set for (1024, 512) polar codes, $L \in \{8, 32, 128\}$, and $I_{\max} = 50$.

Fig. 15. Latency distribution for permuting $R_0$ or $L_n$ of all PFGs for length-1024 polar codes, based on the proposed permutation network.

B. Latency Analysis

Fig. 15 shows the latency distribution for permuting $R_0$ and $L_n$ of all PFGs for length-1024 polar codes (i.e., $p = 0$) based on the PGU. For any PFG, the latency of the PGU is denoted by $\mathcal{L}_\pi$ in (25)

$$\mathcal{L}_\pi = 2\mathcal{L}_\pi - n = 2 \sum_{i=0}^{n-1} |\pi_{s_i} - i| + n, \quad (25)$$

where the multiplication with 2 is due to the reuse of the BSU module in Fig. 10 to shuffle $R_0$ and $L_n$. This latency distribution presents an approximately normal distribution trend: the minimum is 10 CCs and the maximum is 100 CCs. Note that, for all 10! PFGs, $\mathcal{L}_\pi$ of 96% PFGs is lower than 80 CCs. Subsequently, when combined with the aforementioned BPL-SG algorithm, if we set $p = 4$ in (2) (left stages fixed as $[m_0, m_1, m_2, m_3]$) to efficiently decrease the search space of PFGs, the dynamic range of the $\mathcal{L}_\pi$ distribution rapidly narrows, i.e., the maximum $\mathcal{L}_\pi$ has a 60% reduction from 100 CCs to 40 CCs, as shown in Fig. 15.

Consequently, the whole decoding latency of our BPL decoder is calculated by (26), where $I_{\hat{\pi}_l}$ denotes a practical iteration number of $\hat{\pi}_l$ and $k$ is the index of the first PFG that delivers a successfully decoded codeword. Note that, to satisfy the uniformity of (26), we set $\mathcal{L}_{\hat{\pi}_l} = 0$, $\mathcal{L}_{\hat{\pi}_{l+1}} = 0$, and $\mathcal{L}_{\hat{\pi}_{l}} = 0$. The max operation represents how the proposed decoupled decoding schedule alleviates the influence of the permutation latency and of the recovery latency. If we keep $I_{\max}$ relatively large, the decoding latency on $\hat{\pi}_l$ is always dominating in the max term. Numerical results show that when $I_{\max} \geq 15$, (26) can be simplified as

$$\mathcal{L}_{\text{BPL}} \approx \sum_{l=0}^{k} ((n-1) \cdot I_{\hat{\pi}_l}) + k + 1 + \mathcal{L}_{\hat{\pi}_k} - n, \quad (27)$$

where $k \in [0, L)$. The average latency of our BPL decoder for (1024, 512) polar codes with $L = 32$ and $I_{\max} = 50$ is only 53.25 CCs at SNR = 4 dB.

C. Comparisons With Previous Works

In Table II, we present the implementation results of the proposed BPL decoder using 28 nm FD-SOI and compare them with the SOA architectures in [6], [20], [21], [38], [39], [45], [54]. To ensure a fair comparison, we also implement our work based on 65 nm CMOS technology since most published polar decoders use this process. For $L = 32$, our decoder with a near-optimal PFG set can achieve the error-correcting performance of BLER = $10^{-4}$ at SNR = 2.65 dB, which is similar to that of Fast-SSCL-4 in [6] and better than other BP and BPF works. In terms of implementation results, our work has no advantage in terms of worst-case throughput, which is a common problem for a serial architecture. However, our BPL decoder has an average throughput of 25.63 Gbps, which is 1.44×, 1.82×, 4.48×, and 4.33× higher than the SOA BP [39], BPF [20], SC flip (SCF) [54], and SCL decoders [9], respectively. Our area
TABLE II

COMPARISON WITH THE SOA POLAR DECODERS FOR (1024, 512) POLAR CODES

| Decoders | This work | [SSCL'22] [45] | [TCAS-I'19] [39] | [TVLSI'17] [38] | [TCAS-II'20] [20] | [TCOM'20] [21] | [TSP'17] [6] | [TCAS-I'20] [54] | [TSP'20] [55] | [TSP'22] |
|----------|-----------|----------------|-------------------|-----------------|------------------|----------------|-------------|-----------------|----------------|-----------|
| Algorithm | BPL\(\dagger\) | BP | BP | BP | EBPF | GBPF-MS | Fast-SSCl | Fast-SNCF | Fast-SCLF | SR-List |
| Process [nm] | 28 | 65 | 40 | 40 | 65 | 65 | 40 | 65 | 65 | 90 | 28 |
| Quantization [bit] | 7 | 6 | 5 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| List/Attempt | 8 | 128 | 20 | 20 | 4 | 20 | 4 | 128 | 4 | 4 | 6 |
| Avg Iter./Attempt | 13.1 | 11.7 | 11.8 | 11.1 | 11.2 | 11.3 | 11.4 | 11.5 | 11.6 | 11.7 | 11.8 |
| Area [mm\(^2\)] | 0.87 | 2.39 | 2.07 | 0.704 | 1.60 | 3.11 | 0.946 | 1.822 | 0.56 | 2.83 | 0.286 |
| Frequency [MHz] | 13.33 | 352 | 150 | 500 | 334 | 319 | 806 | 840 | 455 | 615 | 1255 |
| Worst-Case T/P [Gb/s] | 0.37 | 0.09 | 0.12 | 0.16 | 1.12 | 1.36 | 0.02 | 0.06 | 1.61 | 0.076 | 0.012 | 3.62 |
| Coded T/P [Gb/s] | 25.63\(\dagger\) | 6.76\(\dagger\) | 1.85\(\dagger\) | 7.61\(\dagger\) | 10.71\(\dagger\) | 3.72\(\dagger\) | 4.19 | 1.61 | 1.51 | 1.52 | 3.62 |
| Area Eff. [Gbps/mm\(^2\)] | 29.46\(\dagger\) | 2.83\(\dagger\) | 0.89\(\dagger\) | 10.81\(\dagger\) | 6.687 \(\dagger\) | 1.20 \(\dagger\) | 4.43 | 0.883 | 2.71 | 0.535 | 12.67 |

Normalized to 65 nm, 1.0 V\(\dagger\).  
\(\dagger\) Average results reported at SNR = 4.0 dB.  
* Worst-case results estimated at \(I_{\text{max}} = 50\) for BP-based decoders.  
† This work employs the double-column bidirectional-propagation architecture.  
§ Identical to the parameters for the 28 nm results.  
‡ Normalized to 65 nm technology: area \(\propto s^2\) and frequency \(\propto 1/s\), where \(s\) is the scaling factor to 65 nm.

This work employs the double-column bidirectional-propagation architecture. Identical to the parameters for the 28 nm results.

In this paper, we present an efficient BPL decoder implementation, which supports flexible permutation generation. In terms of the algorithmic contributions, we propose a sequential generation algorithm to obtain a near-optimal PFG set. Subsequently, we propose a hardware-friendly algorithm to generate flexible routings for permutations in hardware on-the-fly by a matrix decomposition. On the architecture level, we present the BPL decoder with several optimizations to significantly reduce the hardware complexity and decoding latency, such as the flexible permutation generator and decoupled decoding schedule. Synthesis results show that our BPL decoder can achieve a throughput of 25.63 Gbps and an area efficiency of 29.46 Gbps/mm\(^2\) at SNR = 4.0 dB, which outperforms other existing SOA BP and BPF decoders. Moreover, our BPL decoder efficiently implements the decoding on multiple PFGs and provides inspiration for the optimizations of long codes and the implementation of generalized AE decoding.

VII. CONCLUSION

In this paper, we present an efficient BPL decoder implementation, which supports flexible permutation generation. In terms of the algorithmic contributions, we propose a sequential generation algorithm to obtain a near-optimal PFG set. Subsequently, we propose a hardware-friendly algorithm to generate flexible routings for permutations in hardware on-the-fly by a matrix decomposition. On the architecture level, we present the BPL decoder with several optimizations to significantly reduce the hardware complexity and decoding latency, such as the flexible permutation generator and decoupled decoding schedule. Synthesis results show that our BPL decoder can achieve a throughput of 25.63 Gbps and an area efficiency of 29.46 Gbps/mm\(^2\) at SNR = 4.0 dB, which outperforms other existing SOA BP and BPF decoders. Moreover, our BPL decoder efficiently implements the decoding on multiple PFGs and provides inspiration for the optimizations of long codes and the implementation of generalized AE decoding.

REFERENCES

[1] E. Arıkan, “Channel polarization: A method for constructing capacity-achieving codes,” IEEE Trans. Inf. Theory, vol. 55, no. 7, pp. 3051–3073, Jul. 2009.
[2] Chairman’s Notes of Agenda Item 7.1.5 Channel coding and modulation, 3GPP TSG RAN WGI Meeting #87 R1-1613710, Nov. 2016.
[3] I. Tal and A. Vardy, “List decoding of polar codes,” IEEE Trans. Inf. Theory, vol. 61, no. 5, pp. 2213–2226, Mar. 2015.
[4] K. Niu and K. Chen, “CRC-aided decoding of polar codes,” IEEE Commun. Lett., vol. 16, no. 10, pp. 1668–1671, Sep. 2012.
[5] S. A. Hashemi, C. Condo, and W. J. Gross, “A fast polar code list decoder architecture based on sphere decoding,” IEEE Trans. Circuits Syst. I, vol. 63, no. 12, pp. 2368–2380, Dec. 2016.
[6] S. A. Hashemi, C. Condo, and W. J. Gross, “Fast and flexible successive-cancellation list decoders for polar codes,” IEEE Trans. Signal Process., vol. 65, no. 21, pp. 5756–5769, Aug. 2017.
[7] M. Hanif, M. H. Ardaši, and M. Arдаši, “Fast list decoding of polar codes: Decoders for additional nodes,” in Proc. IEEE Wireless Commun. Netw. Conf. (WCNC), 2018, pp. 37–42.
[8] Y. Shen, Y. Ren, A. T. Kristensen, A. Balatsoukas-Stimming, X. You, C. Zhang, and A. P. Burg, “Fast sequence repetition node-based successive cancellation list decoding for polar codes,” in Proc. IEEE Int. Conf. Commun. (ICC), 2022, pp. 1–7.
[9] Y. Ren, A. T. Kristensen, Y. Shen, A. Balatsoukas-Stimming, C. Zhang, and A. Burg, “A sequence repetition node-based successive cancellation list decoder for 5G polar codes: Algorithm and implementation,” IEEE Trans. Signal Process., vol. 70, pp. 5592–5607, 2022.

\[ L_{\text{BPL}} = \sum_{l=0}^{k} \max \left( \begin{array}{c} \text{decoding on } \vec{x}_l \text{ permutation on } \vec{x}_{l+1} \text{ recovery on } \vec{x}_{l-1} \\ \text{calculate } u^* \end{array} \right) + k + 1 + L_{\vec{x}_l} - n, k \in [0, L] \]
Fig. 16. SNR of FER at $10^{-4}$ vs. area efficiency (normalized to 65 nm) for various SOA decoders for polar codes.