A 10-bit 10-MS/s single-ended asynchronous SAR ADC with CDAC boosting common-mode voltage and controlling input voltage range

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Abstract A capacitor digital-to-analog converter (CDAC), which boosts the common-mode voltage and controls the input voltage range, is proposed to improve the dynamic range and linearity of a single-ended successive approximation register (SAR) analog-to-digital converter (ADC). The 10-bit 10-MS/s single-ended asynchronous SAR ADC using the proposed CDAC is implemented by using a 180-nm CMOS process with a supply voltage of 1.8 V. Its active area and power consumption are 0.207 mm² and 2.29 mW, respectively. The measured DNL and INL are +0.93/-0.51 LSBs and +0.61/-0.81 LSBs, respectively. The measured ENOB is 9.04 bits for the analog input signal with Nyquist frequency.

key words: successive approximation register, analog-to-digital converter, capacitor digital-to-analog converter

Classification: Integrated circuits (analog)

1. Introduction

Natural analog signals and signals from various electronic devices are still measured with respect to the ground in the form of single-ended signals. Despite this form of signal measurement, differential analog-to-digital converters (ADCs) are mainly used for high-resolution sensor interfaces. Therefore, a signal-to-differential converter is additionally used in sensor interfaces for differential ADCs. However, as the demand for low-power sensor interfaces has increased, single-ended successive approximate register (SAR) ADCs with capacitor digital-to-analog converters (CDACs) are being used for data conversion of signals with dynamic ranges of approximately 60 dB [1-4]. Although the input signal of the SAR ADC is generally a single-ended analog signal, a differential SAR ADC with a middle reference 

(VREFM) for one of the two input signals is commonly used to increase the noise immunity of the ADC circuit [5-12]. In this case, the dynamic range of the single-ended SAR ADC can be reduced to half of that of a differential SAR ADC. To achieve the full dynamic range of the single-ended SAR ADC with a rail-to-rail input signal range, additional references with different voltage levels compared to VDD and VSS are required for the top and bottom references (VREF and VREFB). In addition, the supply of a single-ended signal to the differential CDAC of the single-ended SAR ADC deteriorates the performance of the comparator following the differential CDAC due to changes in the common-mode voltage of the differential output of the CDAC. This can degrade the linearity performance of the single-ended SAR ADC [13-15].

In this letter, a 10-bit 10-MS/s single-ended asynchronous SAR ADC is proposed for low-power sensor interfaces. The dynamic range and linearity of the single-ended SAR ADC are improved using the proposed CDAC that boosts the common-mode voltage while controlling the input voltage range. The additional capacitor in the proposed CDAC enables implementation of the single-ended SAR ADC with full dynamic range of 10-bit resolution without further reference requirement by controlling the input voltage range in the half rail-to-rail mode operation. Furthermore, it improves the linearity of the single-ended SAR ADC by boosting the common-mode voltage of the CDAC to a value higher than the middle-reference voltage.

2. Proposed single-ended asynchronous SAR with CDAC boosting common-mode voltage and controlling input voltage range

The proposed 10-bit 10-MS/s single-ended asynchronous SAR ADC consists of a CDAC boosting a common-mode voltage, a comparator, an internal reference driver, and a SAR logic, as shown in Fig. 1(a). The proposed single-ended SAR ADC uses an asynchronous architecture to increase the sampling rate without increasing the frequency of the external clock, compared with a typical SAR ADC [16-22]. The binary search operation of the SAR logic, shown in Fig. 1(b), is sequentially performed by using a valid signal of the comparator, which informs the completion of the comparison operation in the comparator. At the rising edge of EX_CLK, which is the synchronous clock signal of the SAR ADC, the sampling process in the single-

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ended SAR ADC is completed and the data conversion process for a 10-bit resolution starts. The operation of the CDAC and comparator is performed asynchronously ten times by controlling the SAR logic for data conversion of the sampled analog signal. After this conversion, the single-ended SAR ADC samples the new analog signal until the next rising edge of $EX_{\text{CLK}}$. The operation sequence of the proposed single-ended SAR ADC is independent of the duty cycle ratio of $EX_{\text{CLK}}$ because the proposed single-ended SAR ADC only uses the rising edge of $EX_{\text{CLK}}$.

In this work, the proposed single-ended SAR ADC uses a half rail-to-rail mode operation [23, 24] to implement the full dynamic range without additional references with different voltage levels. The half rail-to-rail mode operation in a single-ended SAR ADC effectively reduces the input voltage range in half compared with the input voltage range of a differential SAR ADC. In addition, the CDAC boosts the common-mode voltage of its differential output signal to improve the linearity deteriorated by the changes in the common-mode voltage in the single-ended SAR ADC. These two functions are implemented by adding capacitors in the CDAC. To reduce the total capacitance of the CDAC that is increasing because of the boosting of the common-mode voltage and the control of the input voltage range, the proposed CDAC uses a $V_{\text{CM}}$-based switching architecture [25-27]. To implement the single-ended SAR ADC with no dynamic range degradation although $V_{\text{REF}}$ and $V_{\text{REFB}}$ have voltage levels corresponding to $V_{\text{DD}}$ and $V_{SS}$, the CDAC controls the connection of the added capacitor $C_{\text{BOOST}}$, as shown in Fig. 1(a), according to the half rail-to-rail mode operation. The value of $C_{\text{BOOST}}$ is twice that of $C_8$. The capacitors from $C_8$ to $C_{0A}$ in the CDAC are switched for a 10-bit resolution, as shown in Fig. 1(b). To reduce the effect of the reference voltage in half for the half rail-to-rail mode operation, $C_{\text{BOOST}}$ and $C_{0B}$ are operated only for the sampling and $V_{\text{CM}}$-based CDAC operation.

When the differential signal with the input voltage range from $V_{\text{REFB}}$ to $V_{\text{REF}}$ is supplied to the CDAC, the common-mode voltage of the CDAC is generally determined to be $1/2(V_{\text{REF}}+V_{\text{REFB}})$, the common-mode voltage of the differential signal. However, because $V_{\text{REFM}}$ is supplied as the negative input of the CDAC for the operation of the single-ended SAR ADC, the common-mode voltage of the CDAC is changed according to the voltage level of the input signal of the single-ended SAR ADC. Fig. 2 shows the differential output waveform of the CDAC according to the progress of data conversion when the node $V_{\text{CM}}$ of the CDAC is set to the middle voltage of the single-ended input signal. When the input signal of the single-ended SAR ADC is $V_{\text{REF}}$ and $V_{\text{REFB}}$, the common-mode voltages of the CDAC converge to $3/4V_{\text{REF}}+1/4V_{\text{REFB}}$ and $1/4V_{\text{REF}}+3/4V_{\text{REFB}}$, respectively, as shown in Fig. 2(a).

In this case, a comparator with a wide input voltage range connected in parallel with the NMOS and the PMOS input stages is required to compare this...
Fig. 3. Operation waveform of proposed CDAC for single-ended ADC (a) sample for input signal of single-ended SAR ADC (b) first CDAC conversion for VCM-based CDAC operation (c) second CDAC conversion for proposed CDAC operation (@ VIP < VREFM) (d) second CDAC conversion for proposed CDAC operation (@ VIP > VREFM).

differential signal with a change in the common-mode voltage [28-31]. However, the input offset voltage difference between the two input stages generated owing to process mismatch that degrades the linearity performance of the single-ended SAR ADC. The proposed CDAC boosts the common-mode voltage of its differential output signal by connecting to VREF the capacitor C BOOST used for the half rail-to-rail mode operation when the common-mode voltage of the CDAC converges to a voltage level lower than 1/2(VREF+VREFB). Fig. 2(b) shows that the common-mode voltage of the CDAC converge to 1/2(VREF+VREFB) finally through this process when VIP and VIN are VREF and VREFM, respectively. Therefore, the proposed SAR ADC reduces the linearity error caused by the input voltage dependent offset voltage of the comparator by using the letter with only NMOS input stage [23, 32-33]. Fig. 3 shows the operation of the proposed CDAC according to the input voltage level of the single-ended SAR ADC. The single-ended SAR ADC samples a voltage level of VREFB in all capacitors of the CDAC shown in Fig. 3(a). During the sampling phase, the two output nodes of the CDAC, VDACP and VDACM, are not driven to a specific reference to reduce additional power consumption in the reference driver. The voltage at these two nodes is determined by charge sharing of the CDAC as the center voltage between the two analog input signals. The capacitor C BOOST in the CDAC is first switched to the node VCM for the VCM-based CDAC and half rail-to-rail mode operation, as shown in Fig. 3(b). Subsequently, the most significant bit (MSB) B[9] is determined to be low by performing the first comparison in the comparator. Owing to the result of the MSB B[9], the connection of the capacitor C BOOST is maintained at VCM for the remaining data conversion process, as shown Fig. 3(c). When the voltage level of VREF is sampled by the single-ended SAR ADC, the MSB B[9] is determined to be high after the first conversion of the CDAC, as shown in Fig. 3(b). From this result, the common-mode voltage of the CDAC is expected to converge to a voltage level lower than 1/2(VREF+VREFB). In this case, the two capacitors C BOOST are all switched to VREF whereas the two capacitors C8 are switched by the result of the MSB B[9] in the second conversion of the CDAC, as shown in Fig. 3(d). Owing to this CDAC operation, the two outputs of the CDAC are determined using Eqs. (1) and (2). The last term is the voltage boosted by the proposed CDAC. The common-mode voltage of the CDAC is determined using Eq. (3). The connection of the two capacitors C BOOST to VREF is maintained for the remainder of the switching process of the CDAC. The final common-mode voltage of the CDAC is also expressed using Eq. (3) when the single input signal VIP is VREF.

\[
V_{DACP} = -V_{IP} + \frac{7}{4}V_{CM} + \frac{1}{4}V_{REF} + \frac{1}{4}(V_{REF} - V_{REFB})
\]  
(1)

\[
V_{DACM} = -V_{IN} + \frac{7}{4}V_{CM} + \frac{1}{4}V_{REFB} + \frac{1}{4}(V_{REF} - V_{REFB})
\]  
(2)

\[
\frac{(V_{DACP} + V_{DACM})}{2} = \frac{1}{2}V_{REF} + \frac{1}{2}V_{REFB}
\]  
(3)

Figure 4 shows the simulated static performances of the single-ended SAR ADC depending on the boosting of the common-mode voltage of the CDAC. When the analog input voltage supplied to the conventional single-ended SAR ADC increases to a value higher than VREFM, the output common-mode voltage of the conventional CDAC becomes lower than VREFM. In this case, the comparator consists of only the NMOS input stage cannot accurately compare the two output signals of the CDAC. Therefore, as the digital output code of the SAR ADC increases, the linearity of the conventional single-ended SAR ADC degrades, as shown in Fig. 4(a). The proposed CDAC, which can boost the common-mode voltage, improves the integral nonlinearity (INL) of the single-ended SAR ADC from +0.37° to 1.31° least significant bits (LSBs) to +0.16° to 0.16 LSBs, as shown in Fig. 4(b). As the performance of the comparator is affected by the input common-mode voltage, it has a greater effect on the performance improvement of the single-ended SAR ADC as the supply voltage is lower.
3. Chip Implementation and measurement results of proposed single-ended SAR

The proposed 10-bit 10-MS/s single-ended asynchronous SAR ADC was implemented by using a 180-nm CMOS process with a supply voltage of 1.8 V. Its active area and power consumption including the reference driver are $530 \mu m \times 390 \mu m$ and 2.29 mW, respectively, as shown in Fig. 5.

The measured differential nonlinearity (DNL) and INL shown in Fig. 6 are $+0.93/-0.51$ LSBs and $+0.61/-0.81$ LSBs, respectively. In the center code, the DNL has a relatively large value of $+0.93$ LSBs, which is not related to the common-mode boost of the proposed CDAC, and it is due to the capacitor mismatches of the CDAC. The jumping points in the measured INL were also generated because of the mismatches of the binary-weighted capacitors for MSBs above $C_7$ in the CDAC. However, the proposed CDAC, which can boost the output common-mode voltage, eliminated the degradation of INL in the digital output codes above “800”, as shown in Fig. 4(a) due to the increase in the input common-mode voltage of the single-ended SAR ADC. The measured effective number of bits (ENOBs) are 9.22 bits and 9.04 bits for the analog input signals with low and Nyquist frequencies, respectively, as shown in Fig. 7.

4. Conclusion

The proposed 10-bit 10-MS/s single-ended asynchronous SAR ADC was designed using a 180-nm CMOS process with a supply voltage of 1.8 V. The proposed CDAC, which boosts the common-mode voltage and controls the input voltage range, was proposed to eliminate the degradation of dynamic range and linearity caused in the single-ended SAR ADC. The proposed CDAC improved the INL of the simulated static performances of the single-ended SAR ADC from $+0.37/-1.31$ LSBs to $+0.16/-0.16$ LSBs. The measured ENOBs was 9.22 bits for the analog input signals with Nyquist frequencies. The power consumption, including the reference driver, was 2.29 mW.
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