CPS-SPWM Implementation Based on Multi-Controller Collaboration

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Abstract. In order to improve the modularization degree of cascaded H-bridge converter and reduce the development cost, a modularized carrier phase shifted sine pulse width modulation (CPS-SPWM) based on multi-controller is proposed in this paper, which can easily increase or decrease the number of submodules in cascaded H-bridge. In order to solve the problem of coordination in multi-controller structure, a two-stage control structure is proposed, which uses the master controller to carry out closed-loop control for multiple slave controllers, and uses the approximate natural sampling method to realize digital CPS-SPWM modulation, which reduces computation and makes full use of controller resources. The experimental result shows that the stepped voltage waveform output by the proposed method at the AC side is of high quality and H-bridge submodule is easy to be increased and decreased.

1. Introduction
High power and high voltage power electronic equipment is widely used in industry. The traditional two-level converter is no longer suitable for large capacity, medium and high voltage scenarios. New converter topology and modulation methods must be used to improve the converter capacity [1-2].

Modular multi-level converter has the advantages of easy expansion, modular design, reducing switching loss and capacity upgrading. It has a very broad application prospect in the fields of large capacity and high voltage DC transmission, renewable energy grid connection, island power supply and wind power [3-8]. It can improve the efficiency of power production and transmission, which ensure the safe and reliable operation of electrical equipment and power grid [9].

At present, CPS-SPWM technology is used as the main modulation method in CHB multilevel converter, which has low harmonic distortion rate and high equivalent switching frequency. This is suitable for dozens of sub modules in each phase. The existing implementation schemes are DSP + FPGA and single DSP. The former uses the high-speed computing ability of DSP and many pins and resources of FPGA. Its disadvantages lie in the difficulty of communication between DSP and FPGA, the complexity of FPGA programming. The latter uses several groups of advanced pulse width modulation EPWM modules in DSP. Its disadvantage is that the number of output pulses of EPWM module in DSP is small, and it can not realize the expansion of more cascaded H-bridges. What’s more, only using EPWM module in DSP does not make full use of the chip[10-12].

Aiming at the problems of the above scheme, this paper proposes to realize CPS-SPWM by multi controller cooperation. A new digital modulation method is proposed. Finally, an experimental platform is built for experimental verification and the results are analyzed. Compared with the traditional scheme, the proposed scheme integrates the idea of modular design, which is convenient for the expansion of cascaded H-bridge and provides the possibility for the implementation of larger...
capacity converter. The digital modulation method reduces the amount of calculation, the requirement of CPU and the development cost of hardware and software. The economic benefit is remarkable and has a good application prospect.

2. Principle of CPS-SPWM modulation
The topology of n-stage cascaded H-bridge multilevel converter is shown in Figure 1. For the convenience of analysis and discussion, only phase a was analyzed. Firstly, the lower voltage switch and capacitor are connected in parallel to form a sub module. The cascaded H-bridge is composed of sub modules in series. Each submodule H-bridge has an independent DC power supply.

![Topology of cascaded H-bridge multilevel converter](image)

Using CPS-SPWM technology, the switches of each sub module can work together. Finally, the AC side of cascaded H-bridge presents the voltage waveform of step sine wave. In the converter with L number of half bridges, each half bridge unit adopts a common sinusoidal modulation wave. The triangular carrier phases of each half bridge unit are mutually staggered by 1 / L times of the triangular wave period T, i.e:

\[ \phi_{n+1} = \phi_n + \frac{2\pi T}{L} \]  

The L-channel CPS-SPWM signal is obtained by comparing L-channel triangular carrier wave with sinusoidal modulation wave. The n channel (n < L / 2) signal and its complementary signal are used to control the left half arm of an H-bridge module, and the N + L / 2 signal and its complementary signal are used to control the right half arm.

3. CPS-SPWM implementation method
In order to generate step level on AC side, each H-bridge sub module needs two SPWM signals. When 8-stage cascading, each phase needs 16 SPWM signals. To achieve three-phase output, 36 SPWM signals need to be generated at the same time. At present, the commonly used digital chips, such as TMS320F2812, can provide up to 16 channels of SPWM signals, while STM32F407VET6 can only provide 6 channels of SPWM signals. In order to obtain more signal outputs, realize high voltage and large capacity inverter, improve the modularity of H-bridges, and increase or decrease the number of sub modules, this paper proposes a CPS-SPWM implementation method with master-slave structure and multi controllers working together. Taking five level as an example, the working principle is shown in Figure 2.
The master controller uses the internal timer to send the start pulse from GPIO regularly, and uses the external interrupt trigger mode to start the slave controllers one by one. Because the three slave controllers control the three-phase cascaded H-bridge respectively, the output SPWM signals between the slave controllers should be 120° different from each other, so the time for the master controller to send the start pulse should be appropriate, and the phase difference between the slave controllers should be ensured as far as possible.

Temperature, humidity and other environmental factors will have a certain impact on the chip, integrated circuit, etc., the main controller pulse time, interrupt time from the controller response will appear error, and then lead to the output signal phase difference between the slave controllers deviated by 120 degrees. In order to ensure that the phase difference of three-phase output is fixed, the first SPWM signals from three slave controllers are fed back to the main controller. The main controller uses the pulse capture function to detect the phase between the slave controllers, and adjusts the starting pulse sending time according to the deviation.

According to the preset information, the slave controller uses the digital CPS-SPWM modulation method proposed in this paper to modulate, and configures its own timer, GPIO and other modules. This method can make full use of the GPIO of the slave controller. The modulation process is shown in Figure 3. A sine wave period is divided into n points to generate a sine wave array of N and a triangle wave array of the same size. CPS-SPWM array is obtained by an approximate natural sampling method, and then the frequency division coefficient and counting period of the timer are determined. In the timer interrupt, the array value is output from the IO port.

3.1. Generate sine wave array
There are many methods to calculate the sinusoidal value directly by using single chip microcomputer, such as Taylor series approximation, CORDIC algorithm, look-up table method, etc. Taylor series and CORDIC algorithm have a large amount of calculation, CPU burden, look-up table method is relatively simple, but the accuracy is not enough. In this paper, cubic spline interpolation method is used to interpolate sine table. The FPU is used to perform interpolation calculation. FPU (floating point unit) is a floating-point operation unit, and its operation speed is tens of times faster than CPU.

Firstly, the number N and amplitude um of a periodic sine wave are determined, and then the value of each point is calculated according to formula 2 and stored in the sine array.

\[ S[n] = U_n \sin \frac{2 \pi n}{N} \quad (n = 0, 1 \ldots N-1) \]
3.2. Generating triangle wave array

Triangle wave array is essentially an array composed of several arithmetic sequences. First of all, it is necessary to determine the number $P$, tolerance $T$ and triangle wave amplitude $U_C$ of quarter triangle wave period. It should be noted that the synchronous modulation is adopted in this paper, so the $p$-carrier wave ratio $D$ should be equal to the number of sine wave $n$, so as to ensure that there is no phase difference between the triangular wave and the sine wave in each cycle, and the value of $U_C$ should be greater than $u_m$, so as to avoid over modulation. Then calculate the value of each point of a triangle wave period according to formula (3), and copy the value of this period $d$ times. After the first phase triangular wave is generated, the array is shifted to the right circularly to obtain the remaining triangular waves.

\[
\begin{align*}
T[n] &= n \cdot T \\
T[n + P] &= U_C - n \cdot T \\
T[n + 2P] &= -n \cdot T \\
T[n + 3P] &= -U_C + n \cdot T
\end{align*}
\]

3.3. Approximate natural sampling method

The natural sampling method uses sine wave and isosceles triangle wave to compare, and controls the switching device on and off at the time of natural intersection of two wave. The advantage of this method is that the output SPWM waveform is closest to sine wave. However, because its pulse width expression is a transcendental equation, the calculation is cumbersome, so it is very difficult to find its numerical solution on single chip microcomputer. This paper presents an approximate natural sampling method.

As shown in Figure 4 is the schematic diagram of this method, the black dot represents the value of triangular wave number group, the red dot represents the value of sine wave array, and the blue dot represents the real intersection point of triangular wave and sine wave. According to the natural sampling method, the on-off of the switch device should be controlled at $t_1$, but due to the complexity of changing the point, the approximate natural sampling method in this paper chooses to control the on-off of the switch device at $t_2$, The maximum value of time error is shown in formula (4), where $f_m$ is the frequency of sinusoidal modulation wave. Therefore, when the frequency of modulation wave is fixed, the more points taken in a period, the smaller the error between this method and natural sampling method.

\[
E_{\text{MAX}} = \frac{1}{f_m \cdot N}
\]

4. Experimental result

In the experiment, STM32F429IGT6 is used as the master controller, STM32F407VET6 as the slave controller, and MX1508 as the H-bridge. In order to ensure the independence of each H-bridge sub module, DC-DC isolation module is used to isolate the power supply of H-bridge, and optocoupler is used to isolate the control signal of MCU. The load on AC side is resistive load with resistance of 60 $\Omega$ and inductance of 2$mH$.

Use logic analyzer to observe the output signal of single chip microcomputer. The four CPS-SPWM obtained by approximate natural sampling method is shown in Figure 5. Channel 0 and
channel 2 are the driving signals of the upper tubes on the left and right arms of one H-bridge, and channels 1 and 3 are the driving signals of the upper tubes on the left and right arms of another H-bridge.

Figure 5 Two or more references

Use the oscilloscope to observe the AC measurement waveform, the input impedance is 10mΩ, and the result is shown in Figure 6. Figure 6 (a) shows the voltage waveform of three-level cascaded H-bridge AC side. It can be seen that the voltage has three levels and the frequency is 50 Hz. Figure 6 (b) shows the voltage waveform of five level cascaded H-bridge AC side. The voltage has five levels, the frequency is 50 Hz, and the waveform is sinusoidal. The experimental results show that the CPS-SPWM method proposed in this paper works well and the waveform quality of step voltage is high.

(a)Three level cascaded H-bridge                (b)Five level cascaded H-bridge

Figure 6 Experimental result

5. Conclusions

This paper analyzes the existing CPS-SPWM implementation methods, and proposes a two-level control structure for its shortcomings, which has high modularity and good versatility. The digital CPS-SPWM modulation is realized by using approximate natural sampling method, which is simple to calculate, easy to implement and practical. This method can be used not only in carrier phase shifted modulation, but also in other modulation processes. Finally, three-level and five level cascaded H-bridge converters are tested. The results show that the proposed method is effective and reliable. The cascaded H-bridge can generate high-quality step voltage waveform at the AC end, and it is easy to expand.

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