Discontinuous conduction/current mode analysis of dual interleaved buck and boost converters with interphase transformer

Ding Wu, Gerardo Calderon-Lopez, Andrew John Forsyth

School of Electrical and Electronic Engineering, University of Manchester, Manchester, UK
✉ E-mail: Andrew.forsyth@manchester.ac.uk

Abstract: A comprehensive and unified analysis is presented for the discontinuous conduction/current mode operation of dual interleaved buck and boost converters with an interphase transformer or coupled inductors. By exploiting the symmetry in the current waveforms between the buck and boost modes of operation, detailed operating maps are derived showing the seven separate discontinuous operating patterns in each circuit. Boundary conditions and overall conversion characteristics are presented along with validation results from simulations and measurements on high-power prototypes.

Nomenclature

- $A_1, A_2, B_1, B_2$: power transistors
- $A_{D1}, A_{D2}, B_{D1}, B_{D2}$: anti-parallel diodes
- $B_1, B_2$: region boundaries
- $C_v, C_2$: filtering capacitors
- $D$: duty ratio
- $D_h$: boundary duty ratio
- $f_n$: di/dt of phase current in sub-circuit $n$
- $f_n'$: normalised di/dt of phase current in sub-circuit $n$
- $I_{base}$: base current
- $i_{diff}$: interphase transformer (IPT) differential current
- $i_{11}, i_{22}$: IPT phase currents
- $I_{peak}$: peak of IPT phase current
- $I_{fi}$: filter inductor current
- $I_{f-avg}$: average filter inductor current
- $L_f$, $L_{1}$, $L_{2}$: IPT winding self-inductance
- $L_{diff}$: filter inductance
- $L_{r}$: differential inductance to filter inductance ratio
- $M$: load to high side voltage ratio
- $n$: load sub-circuit number
- $R$: load resistance
- $T$: period
- $V_1$: low side voltage
- $V_2$: high side voltage
- $v_{com}$: IPT common point voltage
- $v_{diff}$: IPT differential voltage
- $v_{fi}$: filter inductor voltage
- $v_{11}$, $v_{22}$: IPT winding terminal voltage

1 Introduction

Interleaving techniques are often used in multi-kW DC–DC converter applications to reduce the size and weight of the input and output filters [1, 2], however, the resultant topologies can have a multiplicity of discontinuous operating patterns under reduced load conditions, which can be difficult to analyse. Typical applications include the power train on-board an electric vehicle where a number of DC systems with different voltages must be interconnected such as fuel-cells, batteries, super-capacitors, auxiliary equipment and traction drive [1, 3, 4]. Other applications include renewable energy systems such as photovoltaic generators. Power levels can range up to 100 kW with voltages up to 600 V. Dual interleaved buck and boost converters have been described for these applications by numerous authors, sometimes with the two inductors replaced by a single inductor and an interphase transformer (IPT) as this arrangement can yield further size and weight reductions [5–7]. Furthermore, single integrated magnetic components have also been suggested [8]. Interleaved converters with higher number of phases have also been suggested [3, 4, 9–11], but the increased circuit complexity can limit the potential gains in size and weight. Whilst there is little published work on the optimum number of phases, most research is focused on two-phase systems. Other research has proposed a range of more complex topologies that, for example, provide larger step-up/down conversion ratios [12–15], soft-switching capability [4, 12, 13] and galvanic isolation [16, 17]. However, the increased component count and increased peak voltage and current levels in these circuits tend to restrict them to low-power applications; furthermore, they are not always extendable to bi-directional power flow. The simpler buck and boost circuits therefore tend to be preferred for high-power (multi-kW) applications such as within a vehicle power train [6, 13, 18, 19].

Discontinuous conduction/current mode (DCM) arises under reduced load in many converters, often producing more complex switching patterns and new modes of operation which can modify the overall conversion characteristics, often in a non-linear manner. Whilst DCM is sometimes preferred in low-power converters, for example, to limit diode reverse recovery or simplify the control in power factor correction applications, its use at high powers tends to be avoided due to the higher peak currents that usually occur. However, in applications with a high peak-to-average load profile such as a vehicle power train, converters can often operate at reduced load in DCM for significant periods of time. An understanding of this mode of operation is therefore important for these applications. Very few publications have examined the behaviour of the dual-interleaved buck and boost converters under discontinuous conduction conditions and these papers typically only consider a sub-set of the possible discontinuous operating patterns [2, 5, 7, 20–23]. A more comprehensive analysis of DCM modes is given in [24] for the dual interleaved boost converter, where ten DCM patterns are presented and the boundary conditions are presented in a flowchart.

This paper presents a comprehensive analysis of the DCM operation of two-phase interleaved buck and boost converters including an IPT, which could be applied to other dual-interleaved
The converter topologies including uncoupled [20], directly coupled [2] and inversely coupled [11]. No detailed analysis of the DCM operation of the dual interleaved buck converter with an IPT has been previously published. The symmetry between the buck and boost mode operating waveforms is used to simplify the analysis. A voltage ratio against duty-ratio operating map is created for buck and boost modes comprising seven sub-regions, which are characterised by individual discontinuous waveform patterns. Expressions for the sub-region boundary conditions are derived. Section 2 shows the general converter analysis and explains the symmetry characteristics. Section 3 presents the detailed operating characteristics of average input/output current against duty ratio in both boost and buck modes. Section 5 presents the simulation and experimental results to validate the analysis.

2 Circuit configurations and symmetry relations

The boost and buck versions of the dual interleaved converter are shown in Fig. 1. The converter consists of a filter inductor, a 1:1 turns ratio IPT [19] and filter capacitors C1 and C2. Transistor-diode pairs A2, D3 and B2, D1 provide boost operation whilst A1, D2 and B1, D3 are the buck devices. The devices would be combined together in a bi-directional converter with A2, B2 enabled for boost operation and A1, B1 operated for buck operation. Alternatively, both transistors in each leg could be switched continuously in a complementary manner in which case discontinuous conduction operation would not occur.

The transistors in each leg of the converter are switched in an interleaved manner with equal duty ratios. The IPT is assumed to consist of two ideal, inversely coupled inductors L1 and L2 which have equal values. Therefore, the total inductance of the IPT between the ends of the windings, nodes for v1 and v2 in Fig. 1, is 4L1 (or 4L2) and is denoted as L_in, the differential inductance [19]. The filter inductor current iL2 is assumed to divide equally between the two halves of the IPT due to the operation of a current mode controller, and the phase currents iL1 and iL2 are given in the following equation

\[ i_{L1,2} = i_{L2} \pm i_{\text{diff}} \]  

2.1 Converter analysis

Depending on the current path, eight converter sub-circuits can be identified as shown in Fig. 2, covering both boost and buck modes of operation. The bottom four will only occur in the DCM. An additional sub-circuit exists, when both the phase currents are zero, denoted as sub-circuit 0. The positive directions of currents in Fig. 2 correspond to boost mode operation and are reversed in the buck mode. The boost and buck mode sub-circuits share the same numbering, however, those for buck mode are underlined in the later text for differentiation.

A large number of operating patterns arise in the converter under discontinuous conditions and to aid in the explanation of these, the symmetry in the waveforms between the buck and boost modes is exploited. The description of operation focuses on one of the phase currents in the IPT since all aspects of the discontinuous operating patterns are evident in these waveforms. The \( \frac{di}{dt} \) in the phase current (\( \frac{di}{dt} \)) is key to determining the waveform shape and is used to illustrate the symmetry.

The expressions for \( \frac{di}{dt} \) in each sub-circuit may be written as

Boost:

\[ \frac{di}{dt} = f_n(M, V_2) = \left( A_n \cdot M + B_n \right) \cdot \frac{V_2}{L_i} \]  

Buck:

\[ \frac{di}{dt} = f_n(M, V_2) = -\left( A_n \cdot M + B_n \right) \cdot \frac{V_2}{L_i} \]  

where M is the voltage ratio \( V_1/V_2 \) and the terms \( A_n \) and \( B_n \) (or \( A_2 \) and \( B_2 \)) are given in Table 1. \( L_i \) is defined as the ratio \( L_\text{in}/L_i \).

By inspection, the symmetry between the \( \frac{di}{dt} \) expressions in the two modes of operation may be expressed by

\[ \frac{di}{dt} = f_n(M, V_2) = \left\{ \begin{array}{ll} f_n(1 - M, V_2), & \text{for } n \in \{1, 3, 5, 7\} \\ f_n(M, V_2), & \text{for } n \in \{2, 4, 6, 8\} \end{array} \right. \]  

The symmetry is illustrated diagrammatically by the plots of \( f_1 \) (boost mode) and \( f_2 \) (buck mode) in Fig. 3. The functions are plotted against M and are normalised by the term \( V_1/L_i \). For example, by considering the arbitrary value of \( M = M_0 \), the symmetry stated in (4) is clearly evident in Fig. 3 as indicated by the dotted lines.

Two of the sub-circuit \( \frac{di}{dt} \) functions (5 and 6) are seen in Fig. 3 to exist only over a limited range of voltage ratio M. This arises due to the limited range of conditions over which the current \( i_{L2} \) remains at zero. Current will start to flow in the winding when the voltage \( V_2 \) of the non-conducting node tends to fall below zero or increase above \( V_2 \), at which points sub-circuits 5 and 6 transit into sub-circuits 3 and 4, respectively.

For example, considering sub-circuit 5 in the boost mode, voltage \( V_{i2} \) may be expressed as

\[ V_{i2} = \frac{2ML_\text{in} + 4V_2}{L_i} \]  

resulting in the condition for sub-circuit 5 to exist

\[ 0 < \frac{2ML_\text{in} + 4V_2}{L_i} < V_2 \]  

The lower inequality is always satisfied, but the upper inequality results in the condition

\[ M < \frac{0.5 + 2/L_i}{L_i} \]  

Fig. 1 Dual interleaved boost and buck topologies

a Boost  
b Buck
In a similar manner, the condition for sub-circuit 6 to exist in the boost mode may be expressed as

\[ M > 0.5 - \frac{2}{L_r} \]  

(8)

In a similar way, considering the \( i_{L_2} \) waveform, identical existence conditions may be determined for sub-circuits 7 and 8.

3 Operating regions

The existence conditions for sub-circuits 5 and 6, (7) and (8) start to define the boundaries between the various operating regions in the discontinuous mode. Through detailed circuit analysis and simulation, the complete set of discontinuous operating regions

![Diagram of converter sub-circuits](image)

**Fig. 2** Complete set of converter sub-circuits

| Sub-circuits | 1 (or 1) | 2 (or 2) | 3 (or 3) | 4 (or 4) | 5 (or 5) | 6 (or 6) | 7 (or 7) | 8 (or 8) |
|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| \( A_n \) (or \( A_0 \)) | 1/2 | 1/2 | 1/2 | 1/2 | 4/(\( L_r + 4 \)) | 4/(\( L_r + 4 \)) | 0 | 0 |
| \( B_n \) (or \( B_0 \)) | 0 | -1/2 | (4 - \( L_r \))/4\( L_r \) | -(4 + \( L_r \))/4\( L_r \) | 0 | -4/(\( L_r + 4 \)) | 0 | 0 |

**Table 1** List of \( A_n \) and \( B_n \) parameters for different sub-circuits

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have been identified and are summarised on the voltage ratio \( M \) against duty ratio \( D \) graph in Fig. 4a for boost mode operation and Fig. 4b for buck mode operation. In both figures, the thick lines represent the boundary for continuous conduction/current mode (CCM) operation where \( M = 1 - D \) (boost mode), and \( M = D \) (buck mode), whereas the triangular area is the DCM operating region. \( D \) is the duty ratio of the active transistors: \( A_2, B_2 \) in the boost mode and \( A_1, B_1 \) in the buck mode.

The DCM operation areas in Fig. 4 are divided into seven major regions labelled as I to VII, characterised by the different waveforms of phase current \( i_L \), as shown in Fig. 5. The buck and boost modes have the same number of regions and identical phase current waveforms, but different sub-circuit sequences. For example, region I in the boost mode has an identical phase current waveform to region I in the buck mode, but the boost mode sub-circuit sequence is 32604280 whilst in the buck mode it is 41503170 as shown in Figs. 4 and 5. Five of the discontinuous regions are divided into two sub-regions depending on the current slopes, however, the sub-circuit sequence is unchanged. The associated waveforms in Fig. 5 are denoted by sub-scripts ‘a’ and ‘b’.

The symmetry between the boost and buck modes of operation is evident in the operating region maps where the location of the individual operating regions is reflected around the \( M = 0.5 \) line between the boost and buck modes. For example, region I appears at the top left in the boost mode map (Fig. 4a) but is located at the bottom left in the buck mode map (Fig. 4b). Similar positional mappings are seen to occur for the other operating regions between the buck and boost modes in Figs. 4a and 4b.

The boundaries between the seven major operating regions in Fig. 4 are either the \( M \) boundaries previously identified by the existence conditions of sub-circuits 5 and 7 and 6 and 8 in (7) and (8), or ones which depend on duty ratio \( D \). In Figs. 4a and b, duty-ratio-dependent operating mode boundaries are labelled as B1–B5. Fig. 6 summarises the boundaries, the typical phase current waveforms and the expressions for duty ratio at the boundary, \( D_b \). The dotted lines in the waveform sketches in Fig. 6 indicate the locus of the peak phase current as the boundary is crossed. The expressions for the boundary duty ratios \( D_b \) in Fig. 6 are seen to be related between the buck and boost modes through the substitution \( M = 1 - M \).

4 Conversion characteristics

A detailed analysis has been undertaken of the characteristic phase current waveforms shown in Fig. 5. In each case, the expressions for \( di_L/dt \) listed in Table 1 were used to solve for the unknown sub-circuit durations in terms of duty ratio, voltage ratio, inductor ratio, filter inductor and switching period. Expressions were then derived for the peak value of the phase current \( i_{L,\text{peak}} \) and the average value of the filter inductor current \( i_{L,\text{avg}} \). The resultant expressions are listed in Appendix in a normalised form \( i_{L,\text{avg}}' \) using a base current \( I_{\text{base}} = V_1T/L_f \) for the boost mode of operation and the corresponding expressions for the buck mode may be obtained by simply substituting \( M = 1 - M \) due to the symmetry relationship between the buck and boost modes.
To illustrate the overall pattern of the conversion characteristics in the discontinuous conduction mode, a set of plots was generated for the normalised average inductor current $I_{L_{\text{avg}}}'$ against duty ratio for a number of different values of voltage ratio $M$. The plots are shown in Figs. 7 and 8 for the boost and buck modes of operation.

Three special cases are shown: $M = 0.5 - 2/Lr$, $M = 0.5$ and $M = 0.5 + 2/Lr$. Each curve is split into sections by round dots to identify the different operating patterns, which correspond to the DCM sub-regions defined in Fig. 4a. The vertical part of the curves indicates the CCM operation (in shadow) where any inductor current value above the minimum set by the DCM boundary may be achieved for a given value of $D$ and $M$. The curved sections of the plots are parabolas due to the $D^2$ terms in the average current expressions. The CCM/DCM boundary for the boost mode has been derived in [19], or can be derived by substituting $M = 1 - D$ into the DCM $I_{L_{\text{avg}}}'$ expression for region II when $D < 0.5$ and into the expression for region VII for $D \geq 0.5$, (9), since the CCM/DCM boundary is on these two regions as shown in Fig. 4.

Moreover, the relative position of the curves and the region boundary points in Figs. 7 and 8 will change depending on the $Lr$ value, as indicated on the axes of the plot. In some circumstances, the curves may cross over each other as seen in one place in Fig. 7, which could be problematic in a closed-loop system. Furthermore, the horizontal sections of the characteristics (when $M \leq 0.5 - 2/Lr$) may also be problematic from a control perspective, indicating regions of $D$ over which the current is insensitive to the value of $D$.

## 5 Simulation and experimental validation

The DCM operating modes have been validated by simulation and practical experiments using two dual-interleaved converter prototypes. The parameters of the two converters are given in Table 2. The converters used a peak current mode controller to ensure equal current sharing between the two halves of the IPT [19, 25], however, other forms of control could be used instead such as analogue or digital average current mode control, or other approaches such as predictive control [25]. The simulation results for comparison purposes were obtained from an idealised Saber model which used lossless components.

### 5.1 Switching cycle waveform examination

Figs. 9–11 show a selection of the DCM operating waveforms both in simulation and experiment to illustrate the operating regions analysed. The boost mode operation uses the converter A in Table 2, a DC power supply at the low voltage side $V_1$ and a resistor bank of $R=120\Omega$ at the high voltage side. The high resistance value ensures a light load condition so that DCM mode can be easily observed. The results presented here have the same...
output voltage $V_2$ of 530 V, whereas the input power supply voltage is varied to achieve the different conversion ratios.

Fig. 9 shows the waveforms when the converter is operating in region IIb with the sub-circuit sequence of 135147. From top to bottom are the drive signals for switches $A_2$ and $B_2$, the filter inductor voltage $v_L$, and the differential voltage across the IPT $v_{\text{diff}}$, one of the IPT phase currents $i_L$, and the filter inductor current $i_L$. The average filter inductor current $i_{\text{Lavg}}$ is predicted using the equation in Table 3 for comparison with the corresponding values from the simulation and experimental measurements. The values are shown in the figure title under each set of results. In this case, they are $13.6$, $13.4$ and $12.5$ A for the theoretical calculation, simulation, and experimental measurement. The agreement is generally very good with the experimental value being slightly lower due to the effects of circuit losses.

The two measured voltages $v_L$ and $v_{\text{diff}}$ match well with those from simulation except in the intermediate voltage levels where a parasitic ringing effect is present. The oscillation occurs in the DCM sub-circuits (5 and 7) when one of the IPT windings ceases conduction and is due to the interaction between the device output capacitances and the inductance in the circuit (both the IPT and the filter inductor). The simulation shows that the phase current $i_{\text{L}}$ is virtually zero in sub-circuit 7 between 1.423 and 1.433 ms, which accompanies the oscillation in the experimental results. The same effect happens in the other half cycle when the other phase current $i_{\text{L}}$ is zero, that is, sub-circuit 5. However, a small current oscillation of the same frequency as the voltage oscillation is observed in the filter inductor and IPT currents. The oscillation frequency, 429 kHz, is approximately equal to the natural frequency of the combined output capacitance of the devices in the non-conducting leg (2.2 nF) combined with the effective inductance of the IPT and filter inductor, which is 52 μH due to the voltage divider operation of the IPT.

Fig. 10 shows the results when the operating mode is in region IIa, with a sub-circuit sequence of 326428 as labelled in the figure. Similar to the results in Fig. 9, the voltages and currents have oscillations during the DCM sub-circuit periods. The ringing
frequency has changed to 398 kHz in this case, which is thought to be due to the change of voltage level on the devices and the associated change in the device output capacitance.

The buck mode operation uses the converter B (Table 2), a DC power supply at the high voltage side to provide a constant voltage of $V_2 = 100$ V and resistors connected at the output voltage $V_1$ side as the load. Fig. 11 shows the result when the duty ratio is 19.3%, and the converter is working in region V with a sub-circuit sequence of 63808460. The currents $i_{L1}$ and $i_{LF}$ have negative parts and match fairly well with the simulation except for the ringing.

The transistor voltage $v_{A1}$ in the second plot is heavily distorted by the parasitic oscillations, and there are periods when one of the anti-parallel diodes is brought into conduction by the oscillations resulting in the voltage being clamped to zero or the input level of 100 V.

5.2 Average current examination

The average inductor current characteristic has been validated using a lossless Saber model as previously described for examining the

![Fig. 8 Buck mode normalised average current characteristics](image)

![Fig. 9 Boost mode, region VIIb, converter A, D = 55.4%, V_1 = 200 V, V_2 = 530 V, I_{L_f,avg} = 13.6, 13.4 and 12.5 A (from theoretical, simulation and measurement, respectively), R = 120 Ω](image)
Fig. 10  Boost mode, region IIa, converter A, $D = 22.3\%$, $V_1 = 300 \text{ V}$, $V_2 = 530 \text{ V}$, $I_{Lf-avg} = 8.7, 8.7$ and $8.2 \text{ A}$ (from theoretical, simulation and measurement, respectively), $R = 120 \Omega$

Fig. 11  Buck mode, region V, converter B, $D = 19.3\%$, $V_1 = 62 \text{ V}$, $V_2 = 100 \text{ V}$, $I_{Lf-avg} = 0.44, 0.44$ and $0.52 \text{ A}$ (from theoretical, simulation and measurement, respectively), $R = 120 \Omega$
waveform patterns. Fig. 12\(^a\) (for boost mode) and Fig. 13\(^a\) (for buck mode) show the comparison between the theoretically calculated normalised average filter inductor current \((I_{\text{base}} = V_1 T/L_f)\) using equations in Table 3 (solid lines) and the Saber simulation results (discrete markers) for \(L_r = 71\). A constant input voltage \(V_1 = 100 \text{ V}\) was used and the output voltage \(V_2\) was set at the required level by a second voltage source/sink. An excellent match is seen between the theory and simulation over all conditions. The differences are typically <1\% and were attributed to rounding errors in the calculations and simulation results processing. A similar validation exercise was undertaken for the peak phase current expressions, and very close agreement was again found with the Saber simulation. The results are shown in Figs. 12\(^b\) and 13\(^b\).

### 6 Conversion ratio examination

In the interests of experimental expediency, the overall conversion characteristics of the prototype (converter B) were measured in the buck mode with a fixed source voltage of 100 V and a fixed 120 \(\Omega\) load resistor, allowing an output voltage against duty-ratio graph to be plotted. A theoretical prediction was generated by multiplying the average inductor current expression from Appendix by the fixed load resistance value and the two sets of data are plotted in Fig. 14 along with the operating region boundaries from Fig. 4. Overall, close agreement is seen between the measured and predicted data apart from the discrepancy found in region VI, where the experimental result is lower than the theoretical one. This was attributed to a small imbalance in the phase currents due to a slight asymmetry in the analogue pulse-width-modulation circuit, which has a proportionally greater effect on the characteristics in region VI.

| Parameter, units | Converter A | Converter B |
|------------------|-------------|-------------|
| switching frequency \(1/T\), kHz | 24.0 | 24.7 |
| filter inductor \(L_p\), \(\mu\)H | 13.6 | 15.4 |
| differential inductance of the IPT \(L_{\text{diff}}\), \(\mu\)H | 976 | 540 |
| self-inductance and self-inductance of the IPT | 244 | 135 |
| \(L_i = L_p\), \(\mu\)H | 71.7 | 35.1 |
| minimum low voltage port voltage \(V_1\), V | 190 | 220 |
| nominal high voltage port voltage \(V_2\), V | 600 | 600 |
| nominal filter inductor current \(I_{\text{avg}}\), A | 170 | 260 |
| nominal output power, kW | 50 | 58 |

Fig. 12  Comparison of inductor currents between the calculated values (solid lines) and Saber simulation results (markers), \(V_1 = 100 \text{ V}\), \(V_2 = 150 \text{ V}/195 \text{ V}/205 \text{ V}/300 \text{ V}\), \(L_f = 13.6 \mu\text{H}\), \(L_r = 71.7\), 24 kHz, boost mode, rated current \(I_{\text{base}} = 306 \text{ A}\)

\(a\) Normalised average filter inductor current

\(b\) Normalised peak phase current

Fig. 13  Comparison of inductor currents between the calculated values (solid lines) and Saber simulation results (markers), \(V_1 = 100 \text{ V}\), \(V_2 = 150 \text{ V}/195 \text{ V}/205 \text{ V}/300 \text{ V}\), \(L_f = 13.6 \mu\text{H}\), \(L_r = 71.7\), 24 kHz, buck mode, rated current \(I_{\text{base}} = 306 \text{ A}\)

\(a\) Normalised average filter inductor current

\(b\) Normalised peak phase current
7 Conclusions

By recognising the symmetry pattern in the circuit waveforms between the buck and boost operating modes of the dual interleaved converter with IPT, a comprehensive and unified analysis has been presented of the seven discontinuous mode sub-regions. The sub-regions have been identified on a voltage ratio against duty-ratio map along with the associated boundary conditions. On the basis of the individual sub-region operating patterns, expressions are presented for the average inductor current and peak phase current, allowing the overall conversion characteristics to be plotted.

The observed DCM operating patterns and the equations derived for the average and peak currents have been validated through extensive Saber simulation of an idealised converter where excellent agreement is achieved for both boost and buck modes. Furthermore, the boost and buck mode operation waveforms have been validated by experiments using two different converter prototypes, although parasitic ringing between the device output capacitances and circuit inductances was seen to modify the waveforms in some circuit configurations.

The overall conversion characteristics that have been derived provide an understanding of converter behaviour in the discontinuous mode and could form the basis for a supervisory controller, for example, to linearise the converter response in a battery charge/discharge regulator application.

8 Acknowledgment

The authors gratefully acknowledge the contributions of Dr Frank Bryan in the experimental work.

9 References

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Fig. 14  Buck mode, fixed input voltage $V_2 = 100 \text{ V}$ and variable output voltage $V_1$ against duty ratio $D$
10 Appendix

See Table 3.

Table 3  Average inductor current and peak current expressions for the boost mode DCM regions

| Region | Boost mode |
|--------|------------|
| I      | $I_{\text{L-f-avg}} = \frac{K_0 D}{4(1 - M) M}$ | $I_{\text{L-f-peak}} = \frac{K_0 D}{4M}$ |
| II     | $K_2 D^2$ | $K_0 D/4M$ |
| III    | $4D^2/K_1 L (1 - M)$ | $4D/K_1 L_r$ |
| IV     | $\frac{4 K_2 L_r D^2 - 2 K_2 K_3 L_r D + 4 K_2 (1 - M)}{K_4 L_r^2}$ | $\frac{2 K_2 D + K_3 (1 - M)}{K_4 L_r}$ |
| V      | $\frac{64 D^2}{K_1 K_4 L_r^2}$ | $4D/K_4 L_r$ |
| VI     | $\frac{4}{K_1 L_r^2}$ | $1/L_r$ |
| VII    | $(2D - K_3)^2/4K_4$ | $(2D - K_3)/4$ |

where $K_1 = 1 + 4/L_r$; $K_2 = 1 - 4/L_r$; $K_3 = 2M - K_2$; $K_4 = K_4 - 2M$; $I_{\text{base}} = V_1 T/L_r$