Seed Layer Engineering for Crack-free Sol-gel Alumina Deposition on GFETs

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Abstract—Low cost and low thermal budget based spin-coated sol-gel Alumina was explored as a dielectric/passivation layer for GFET. Post thermal annealing, the crack was observed in sol-gel Alumina layer exactly above the graphene channel. The possible mechanism of crack could be graphene lateral restoring movement due to (i) Thermal Expansion Coefficient (TEC) difference between graphene and adjacent layers and (ii) shrinkage stress generated during the solvent removal process. Based on the crack formation phenomenon, a combination of different annealing schemes (low thermal budget DUV annealing) and seed layer engineering (thickness and different deposition schemes) were carried out. Finally, a novel two-step seed layer deposition method with DUV annealing was proposed and demonstrated to resolve the crack issue successfully and also able to retain the Dirac point in the electrical characteristics.

Index Terms—Monolayer graphene, GFET, sol-gel, Seed layer engineering, Dirac point, DUV annealing

I. INTRODUCTION

The uniqueness in the properties of graphene like ambipolar transport, high carrier mobility [11], exceptional mechanical strength [2], thermal properties [3] and flexible nature [4] have paved the way for the RF applications over conventional materials [5]. Dielectric materials plays an important role of gate dielectric and passivation layer for any FET devices. There are different techniques like PVD [6], [7] and ALD [8]–[11] to deposit high quality dielectric layers. On the other hand there are reports of solution based deposition techniques through spin or spray coatings for dielectric materials [12]. These techniques have advantages of high deposition rate, no vacuum requirement, low cost method, tuning of the precursor composition [13] and can be used for flexible applications [14]. But there are also several challenges in using solution based deposition techniques like (i) adhesion of spray or spin coated layer with the underneath layer and (ii) need to anneal layers post deposition to remove solvent from the layer, which leads to stress in the films.

The most commonly used dielectrics for the GFETs are Si3N4 [15], HfO2 [16] and Al2O3 [17]. Among them, the Al2O3 has proven to be the best passivation layer due to its high thermal stability, appreciable permeability barrier and reduced hysteresis in transfer characteristics in FET devices [18]. The presence of the Al2O3 monolayer does not introduce interface states and electron-hole puddles in graphene [19]. Recently the sol-gel Alumina (Al2O3) has been extensively used in the solar cells as a field-effect passivation layer [20] due to its good interface quality and dielectric breakdown. Park et.al [21], [22] and Bae et.al [23] have explored sol-gel Alumina on the graphene transistors as dielectric layer and pH sensing membrane.

Before sol-gel Alumina spin coating, the surface of graphene needs to be made hydrophilic for its proper adhesion. There are few techniques like plasma exposure [24], functionalisation [25], seed layer deposition [21], [26] explored for wetting the graphene surface. Techniques such as O2 plasma exposure, UV-O3 irradiation and functionalization would create lattice damage [27] and doping to the graphene [25]. On the other hand, the seed layer deposition does not create any lattice damage and also won’t create any P-type doping [10], [28], [29]. The deposition of the seed layer is usually carried out by the e-beam evaporation technique as it provides structural and morphological control of films and offers low resistivity [30]. The e-beam lacks uniform deposition in the inner surface of 3D complex geometries due to the shadowing effect caused by line of sight deposition [31]. Sputtering can also be used as an alternative for deposition of a seed layer for conformal coverage of steps and trenches [32]. The problem associated with sputtering was that it can damage the underlying surface with plasma.

The proper densification of sol-gel thin film requires an annealing process to remove the solvent and also some trapped byproducts from the oxide network [21], [23]. The conventional method i.e thermal annealing mostly requires elevated temperature which can cause strain [33] and unintentional doping [34] in graphene devices. Also, during the annealing of the sol-gel solution, the drying stress due to the differential shrinkage (capillary forces) of the gel will be present [13], [35]. But at high temperatures, the films are prone to
undergo in-plane stress i.e. tensile stress during the heating and compressive stress after cooling [36], [37]. To reduce annealing temperature, techniques such as Deep Ultra Violet (DUV) annealing [38]–[40], O$_3$ annealing [41], Microwave annealing [22], [26], [42], [43]. High pressure annealing [44] are mostly used. Among these DUV annealing process was the most explored and readily available technique for sol-gel Alumina [39].

In this work, we report fabrication of sol-gel alumina based GFET devices. We discovered crack formation in the sol-gel Alumina layer post annealing. We explored seed layer engineering and different annealing techniques (Thermal and DUV) based on understanding different phenomenons to resolve the crack issue. Finally we propose novel two step method to resolve the crack issue.

II. EXPERIMENTAL

A. Synthesis of sol-gel Alumina

The synthesis of sol-gel Alumina was carried out by mixing the Aluminum nitrate nonahydrate (Al(NO$_3$)$_3$.9H$_2$O) (from Sigma Aldrich) with CMOS grade Isopropyl alcohol (C$_3$H$_7$OH). The mixture was stirred for 12 hours and the resultant solution was filtered using a membrane filter with a pore size of 0.22 $\mu$m. The molarity of the resultant solution was kept at 0.1 M. The resultant solution was spin-coated on samples at 5000 rpm for 45 seconds. Thermal [21] and DUV annealing [39] techniques have been used to remove solvent from spin-coated sol-gel Alumina.

B. Fabrication of GFETs

The fabrication flow of graphene-based transistor with a seed layer and passivation layer is shown in Figure 1. To fabricate the graphene transistors, CVD-grown graphene monolayer on copper foil were purchased from Graphenea Inc. These copper foil was cut into pieces and coated with 2% PMMA 950K. Next, the pieces were immersed in the Copper etchant solution. The isolated graphene layers were carefully transferred to a thermally oxidized 2-inch silicon substrate with a resistivity of 0.002-0.005 ohm-cm. The thickness of the SiO$_2$ was kept at 90 nm to make the transferred graphene layer optically visible [45]. The backside oxide was etched using 7:1 buffered Hydrofluoric (BHF) acid solution for the substrate contact. Then, a graphene monolayer was patterned for the graphene channels using the optical lithography followed by the oxygen plasma exposure. The device dimensions used are width (W = 5-7$\mu$m) and length (L = 20-30$\mu$m). After channel definition, the source and drain contacts were made by using the electron beam evaporation (e-beam) of 10 nm Nickel and 40 nm Gold followed by the lift-off process. Thereafter, the Aluminum seed layer engineering was carried out as shown in Figure 1. Subsequently, the deposited seed layers were subjected to natural oxidation in the ambient atmosphere for one day. Next, the synthesized sol-gel Alumina was spin-coated followed by the thermal/DUV annealing. Finally, the densified sol-gel Alumina film was patterned to complete the device fabrication. The electrical characterization on the respective samples were carried out done using a Keysight B1500A semiconductor device analyzer.

![Figure 1](image_url)  The complete fabrication flow for GFETs with different splits for seed layer engineering

III. RESULTS AND DISCUSSION

A. Thin seed layer deposition by e-beam evaporation

Figure 2 shows the effect of thermal annealing on GFET with a seed layer thickness of 2 nm deposited using e-beam evaporation. The annealing was carried out on a hotplate at 250°C for 2 hours. During the densification by thermal annealing, the crack was observed in the sol-gel Alumina layer of GFET exactly above the graphene channel layer as shown in Figure 2 (a) and (b). The Atomic Force Microscopy (AFM) image (Figure 2 (c)) with profiling (Figure 2 (d)) conforms that crack formation in the sol-gel Alumina layer. The depth profile shows a non-uniformity at the edges of the cracks due to the agglomeration of the Alumina film after densification.

The origin of crack formation was investigated by fabricating the entire device without a graphene layer. It was found that there was no crack formation without a graphene layer.
Figure. 2. (a) Microscope image of GFET after sol-gel densification at 250°C for 2 hours (b) SEM image of the GFET showing the crack on the graphene channel in sol-gel Alumina. (c) AFM image of the crack (d) Depth profiling of the crack (e) Microscope image of sol-gel Alumina without graphene on SiO₂ (f) Transfer characteristics of the GFET of Figure (a). This confirms that the graphene layer plays a major role in crack formation in the sol-gel Alumina layer during the annealing process. There could be the following two phenomenons happening during annealing, (i) solvent removal and (ii) expansion and/or compression of material depending upon the TEC of the material. There are reports of stress generated due to shrinkage of sol-gel Alumina during annealing [13], [46]. Positive TEC leads to expansion of material and negative annealing leads to compression during annealing. Graphene has a negative TEC [47], on other hand SiO₂ substrate and oxidized seed layer has positive TEC [48], [49]. There are reports that when there was a negative TEC graphene on positive TEC SiO₂ substrate, then it leads to slippage (lateral restoring movement) of graphene during annealing due to TEC difference between them [47]. The threshold temperature to cause slippage was reported to be 117°C [50]. Both of the above phenomena might lead to the movement of graphene, as graphene was residing on the substrate with van der Waals forces. The movement of graphene might lead to crack formation in the sol-gel Alumina film.

The Figure 2(f) shows the transfer characteristics of GFET for device Figure 2(a). The output drain current after the thermal annealing of sol-gel Alumina shows the disappearance of the Dirac point and the electron branch. This conforms to the P-type nature of the graphene [51]. This is due to the diffusion of O₂ and H₂O from the ambient atmosphere which will form the redox reaction with the graphene during annealing [11] in addition to the stress. These redox reactions will form the OH⁻ ions at the interface which will act as coulomb scatters.

The TEC component can be reduced by using an annealing technique with a lower thermal budget. There are reports of DUV annealing to reduce thermal budget during annealing [39]. The DUV annealing technique has been applied in this work. The temperature was measured during DUV annealing using thermo-couple and it was found to be close to 70°C. The graphene device fabricated using DUV annealing still exhibits crack formation in the sol-gel layer exactly above the graphene layer as shown in the Figure 3(a). On the other hand, the device without graphene exhibits no crack as shown in the Figure 3(b). Hence it can be concluded that reducing the thermal budget was not sufficient to avoid crack formation. It means that even with DUV annealing the movement of graphene was not restricted.

Figure. 3. (a) Microscope image of GFET after sol-gel densification by DUV annealing for 30 mins with graphene channel (b) Without the graphene channel on SiO₂

B. Seed layer thickness variation

To further reduce graphene movement, different thicknesses (2.5, 3.5, and 5 nm) of seed layers were tried to make a graphene device. As shown in subfigures (i)-(iii) of Figure 4(a) and (b), it can be seen that graphene devices with 2.5 and 3.5 nm exhibit crack formation. On the other hand, 5 nm device does not show any crack formation as shown in Figure 4(c)(i)-(iii). Hence devices with thicker seed layers were able to restrict graphene movement to avoid crack formation. But when the graphene devices with a 5 nm seed layer were electrically tested before and after the sol-gel deposition as shown in the Figure 5(a) and (b). It was found that post-sol-gel deposition, devices show the disappearance of the Dirac point and resulted in the hole doping after the thermal annealing.
In contrast, the drain current after DUV annealing did not show any modulation with gate voltage variation which means that the Aluminum seed layer could not have fully oxidized. Further deeper analysis of fabrication pointed out that a thin seed layer (2.5 nm) was deposited using e-beam evaporation, which was the line of sight deposition and might not lead to side-wall coverage (Figure 6(a)).

(i) first thin seed layer deposition using e-beam evaporation to avoid damage to graphene and (ii) thin seed layer deposition using sputter process to have sidewall coverage. The device was fabricated with a two-step process as shown in Figure 6(b).

Figure. 6. 2-D Schematic of (a) GFET with seed layer type-1 deposited from e-beam evaporation (the lack of seed layer on side walls) (b) GFET with seed layer type-2 deposited in sequence from e-beam (1.5 nm) evaporation and sputter (1.5 nm) (for good side wall deposition)

As shown in the Figure 7 (a) and (b), no cracks were observed in Alumina film on the graphene channel region. The sequential deposition will provide dense, hydrophilic, assist in the faster heat transfer from the metal contacts to the sol-gel Alumina, and also withstands the stress-induced slippage generated by TEC mismatch and stress due to shrinkage of the sol-gel Alumina during annealing as shown in the schematic 6(b).

Figure 7 (c) shows the transfer characteristics for the As fabricated GFET and after the DUV annealing with sequential seed layer deposition. The As fabricated GFET shows the Dirac point at around -6.4 V which was the signature of the n-type doping [51]. This shift could be due to long exposure of the resist stripper during lift-off process [52]. The asymmetry in transfer characteristics was due to the work-function difference between Nickel (Work function - 5.01 eV) and graphene (Work function - 4.5 eV) [53]. However, the GFET retains its Dirac point after the DUV annealing in contrast to thermal annealing but with a slight shift in Dirac point towards negative voltage which is at around -8 V. The mobility of the GFET before and after DUV annealing was calculated using the FTM method [9]. The extracted parameters and their comparison are reported in the table I. The decrease of the mobility in electron and hole branches after DUV annealing could be attributed to the charged impurity scattering [54]. The summary of the entire work is given in table [1].

C. Sequential seed layer deposition

To avoid insufficient oxidation and crack formation issues, we propose a novel two-step seed layer deposition approach.

![Diagram](image_url)

Figure. 4. The study of the crack in Alumina thin film on graphene channel by seed layer thickness variation on GFET before sol-gel deposition. (a), (b) and (c) are three sets used to study the seed layer thickness variation represented by dashed lines. Subfigure (i) in (a), (b), and (c) represent the micrograph of the Aluminum seed layer of thickness 2.5 nm, 3.5 nm, and 5.0 nm. Subfigure (ii) in (a), (b), and (c) represents SEM images after the thermal annealing of Alumina on GFET. The subfigure (iii) in (a), (b), and (c) represents SEM images after the DUV annealing of Alumina on GFET.

![Diagram](image_url)

Figure. 5. Transfer characteristics of graphene FETs after (a) thermal and (b) DUV annealing of sol-gel Alumina with 5 nm seed layer thickness.
Fig. 7. (a) Microscope image of GFET after sol-gel Al2O3 deposition and DUV annealing with seed layer type-2 prior to sol-gel deposition (b) SEM image of GFET after sol-gel Alumina deposition and DUV annealing with seed layer type-2 prior to sol-gel deposition (c) Transfer characteristics of GFET before and DUV annealing of sol-gel Alumina.

### Table I

**Mobility, Residual carrier concentration, Contact resistance extracted using FTM method before and after DUV annealing**

| Parameters                        | As fabricated GFET | After sol-gel deposition + DUV annealing |
|-----------------------------------|--------------------|-----------------------------------------|
|                                   | Hole branch        | Electron branch                         |
| Mobility (cm²/V-sec)              | 4400               | 1174                                    |
| Residual carrier concentration (/cm²) | 5.2e11          | 7.1e11                                  |
| Contact resistance (ohms)        | 1134               | 2084                                    |

### IV. Conclusion

The comparison between with and without graphene channel devices confirms that the crack issue in sol-gel Alumina layer post thermal annealing is due to underneath graphene layer. The possible mechanism for crack formation was thought to be restoring movement of graphene layer due to stress generated because of TEC mismatch amongst layers and shrinkage during annealing. Even though DUV annealing with e-beam evaporated thin seed layer films (2.5 nm and 3.5 nm) were not able to resolve the crack issue. On other hand, 5 nm thick e-beam evaporated seed layer based devices did not show crack formation but, electrical testing confirms that the seed layer was not completely oxidised. Finally, we proposed novel two step seed layer deposition process (1.5 nm from e-beam and 1.5 nm from sputtering) with DUV annealing to cover side wall and restrict graphene movement with reduced shrinkage stress. The novel method not only resolved the crack issue but also retained Dirac point of the transistor.

### Table II

**Summary table for crack and Dirac point for thermal and DUV annealing (**Yes** = Exists, **No** = Absent, and ‘–’ = Unattempted )**

| Seed layer process | Thickness (nm) | Crack Thermal anneal | DUV anneal | Dirac point Thermal anneal | DUV anneal |
|--------------------|----------------|----------------------|------------|---------------------------|------------|
| e-beam             | 2.0 nm         | Yes                  | –          | –                         | –          |
| Thickness variation | 2.5 nm         | Yes                  | Yes        | –                         | –          |
| (e-beam)           | 3.5 nm         | Yes                  | Yes        | –                         | –          |
| (e-beam)           | 5.0 nm         | No                   | No         | No                        | No         |
| Sequential seed layer | 1.5 nm         | –                    | No         | –                         | Yes        |
| (e-beam + Sputter) |                |                      |            |                           |            |

show crack formation but, electrical testing confirms that the seed layer was not completely oxidised. Finally, we proposed novel two step seed layer deposition process (1.5 nm from e-beam and 1.5 nm from sputtering) with DUV annealing to cover side wall and restrict graphene movement with reduced shrinkage stress. The novel method not only resolved the crack issue but also retained Dirac point of the transistor.

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### References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, “Electric field effect in atomically thin carbon films,” *science*, vol. 306, no. 5696, pp. 666–669, 2004.

[2] J. Lee, L. Tao, K. N. Parrish, Y. Hao, R. S. Ruoff, and D. Akinwande, “Multi-finger flexible graphene field effect transistors with high bendability,” *Applied Physics Letters*, vol. 101, no. 25, p. 252109, 2012.

[3] A. A. Balandin, “Thermal properties of graphene and nanostructured carbon materials,” *Nature materials*, vol. 10, no. 8, pp. 569–581, 2011.

[4] S. Park, S. H. Shin, M. N. Yogeesh, A. L. Lee, S. Rahimi, and D. Akinwande, “Extremely high-frequency flexible graphene thin-film transistors,” *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 512–515, 2016.

[5] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, and W. Haensch, “Graphene radio frequency receiver integrated circuit,” *Nature communications*, vol. 5, no. 1, pp. 1–6, 2014.

[6] Y. Wu, P. Ye, M. A. Capano, X. Yuan, Y. Sui, M. Qi, J. A. Cooper, T. Shen, D. Pandey, G. Prakash et al., “Top-gated graphene field-effect transistors formed by decomposition of sic,” *Applied Physics Letters*, vol. 92, no. 9, p. 092102, 2008.

[7] J. Kedzierski, P.-L. Hsu, P. Healey, P. W. Wyatt, C. L. Keast, M. Sprinkle, C. Berger, and W. A. De Heer, “Epitaxial graphene transistors on sic substrates,” *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 2078–2085, 2008.
[43] Y. Kim, D.-H. Cho, S. Ryu, and C. Lee, “Tuning doping and strain in graphene by microwave-induced annealing,” Carbon, vol. 67, pp. 673–679, 2014.

[44] Y. S. Rim, W. H. Jeong, D. L. Kim, H. S. Lim, K. M. Kim, and H. J. Kim, “Simultaneous modification of pyrolysis and densification for low-temperature solution-processed flexible oxide thin-film transistors,” Journal of Materials Chemistry, vol. 22, no. 25, pp. 12491–12497, 2012.

[45] P. Blake, E. Hill, A. Castro Neto, K. Novoselov, D. Jiang, R. Yang, T. Booth, and A. Geim, “Making graphene visible,” Applied physics letters, vol. 91, no. 6, p. 063124, 2007.

[46] B. Gawel, K. Gawel, and G. Øye, “Sol-gel synthesis of non-silica monolithic materials,” Materials, vol. 3, no. 4, pp. 2815–2833, 2010.

[47] D. Yoon, Y.-W. Son, and H. Cheong, “Negative thermal expansion coefficient of graphene measured by raman spectroscopy,” Nano letters, vol. 11, no. 8, pp. 3227–3231, 2011.

[48] W. Bao, F. Miao, Z. Chen, H. Zhang, W. Jang, C. Dames, and C. N. Lau, “Controlled ripple texturing of suspended graphene and ultrathin graphite membranes,” Nature nanotechnology, vol. 4, no. 9, pp. 562–566, 2009.

[49] A. Wilson, “The thermal expansion of aluminium from 0 to 650 c,” Proceedings of the Physical Society, vol. 53, no. 3, p. 235, 1941.

[50] T. Jiang, Z. Wang, X. Ruan, and Y. Zhu, “Equi-biaxial compressive strain in graphene: Grüneisen parameter and buckling ridges,” 2D Materials, vol. 6, no. 1, p. 015026, 2018.

[51] B. Guo, L. Fang, B. Zhang, and J. R. Gong, “Graphene doping: a review,” Insences J., vol. 1, no. 2, pp. 80–89, 2011.

[52] S. Sul, K. Kim, E. Choi, J. Kil, W. Park, and S.-B. Lee, “Reduction of hole doping of chemical vapor deposition grown graphene by photoresist selection and thermal treatment,” Nanotechnology, vol. 27, no. 50, p. 505205, 2016.

[53] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, “Metal/graphene contact as a performance killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance,” in 2009 IEEE International Electron Devices Meeting (IEDM). Ieee, 2009, pp. 1–4.

[54] J.-H. Chen, C. Jang, S. Adam, M. Fuhrer, E. D. Williams, and M. Ishigami, “Charged-impurity scattering in graphene,” Nature physics, vol. 4, no. 5, pp. 377–381, 2008.