Device Design Guidelines of 3-nm Node Complementary FET (CFET) in Perspective of Electrothermal Characteristics

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ABSTRACT
For the first time, device design guidelines for a 3-nm node complementary field-effect transistor (CFET), which vertically stacks n-type and p-type nanosheet MOSFETs with a shared gate, are investigated using calibrated 3-D technology computer-aided design (TCAD). Here, the optimal device dimensions of the CFETs for better inverter performance and thermal characteristics are studied. The electrothermal performance are investigated for various vertical dimension parameters of CFET, such as the number of stacked channels, vertical distance between nanosheet channels ($D_{nsh}$), distance of n/pMOS separation ($D_{n/p}$), and channel thicknesses ($T_{nsh}$). The results show that, unlike conventional CMOS, the reduction of $D_{nsh}$ and $D_{n/p}$ of CFET can effectively improve inverter performance without severe thermal degradation, although other dimensional parameters trigger a severe trade-off between different electrothermal parameters. The reduction of $D_{nsh}$ and $D_{n/p}$ decreases $C_{eff}$ with a lower metal via the height and gate fringing effect. However, the reduction in $D_{nsh}$ and $D_{n/p}$ does not change $R_{eff}$; therefore, both the operation frequency ($f$) and power-product delay (PDP) can be improved. In the case of thermal characteristics, the reduction of $D_{nsh}$ and $D_{n/p}$ slightly increases both $T_{max}$ and $R_{th}$ because of thermal coupling but is negligible. Therefore, the reduction of $D_{nsh}$ and $D_{n/p}$ will be a key technique for the development of sub-3-nm CFET.

INDEX TERMS
Complementary FET (CFET), nanosheet FET (NSHFET), technology computer-aided design (TCAD), 3-nm technology node.

I. INTRODUCTION
Conventional FinFETs, which have recently been scaled down to 5-nm nodes, have almost reached physical limits in reducing fin thickness [1]. Thus, to improve gate controllability, nanosheet FETs (NSHFETs) with gate-all-around (GAA) structures have been actively developed for sub-3-nm nodes [1]–[3]. However, they will continue to face these down-scaling limitations in the future. Therefore, to reduce the number of tracks and layout area to reduce the device footprint, the International Roadmap for Devices and Systems (IRDS) expects that a 3-dimensional structure which stacks multiple NSHFETs vertically can be a strong candidate for future technology nodes [4]–[11]. Thus, one of the most promising devices with a 3-dimensional structure, the complementary field-effect transistor (CFET), which stacks n-NSHFET and p-NSHFET vertically with a shared gate for CMOS inverter operation in one device, has recently been suggested by Intel, Applied Materials, IMEC, and NARLab [4]–[9]. In addition, in a recent study on CFET, it was demonstrated that CFET with NSHFET shows better inverter performance than CFET with FinFET [8].

Recently, NSHFET have been replacing FinFETs for logic devices because of higher inverter operation frequency ($f$). This is owed to the lower effective resistance ($R_{eff}$) of NSHFETs due to better current drivability and gate controllability in the same footprint [1]. However, the large effective capacitance ($C_{eff}$) of NSHFETs disturbs additional improvement of $f$ or power-product delay (PDP). Therefore, a decrement of $C_{eff}$ is an important factor for improving inverter performances. Furthermore, the CFET, which stacks vertically stacked NSHFETs also faces performance
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Degradation by high $C_{\text{eff}}$ because of the additional height of metal via of the vertically stacked structure. Recent studies demonstrated that CFET shows the possibility for better $C_{\text{eff}}$ compared with conventional CMOS with NSHFETs because of fringe electric field overlap triggered by the reduced distance between nMOS and pMOS with the vertically stacked structure [4], [10]. In addition, recent fabrication processes demonstrated by Intel reduced number of metal via by connecting the drain of the nMOS and pMOS with one piece of metal via. This could additionally decrease $C_{\text{eff}}$. However, CFET has a much higher height of metal via compared with conventional CMOS because of the stacked structure of the nMOS and pMOS. Therefore, there is still a risk of the degradation of $C_{\text{eff}}$, and the careful design of CFET is required. Therefore, analyzing $C_{\text{eff}}$ and $R_{\text{th}}$ of the CFET by varying dimensions is required to evaluate $f$ and PDP [3].

In addition, it has been reported that multi-gate transistors such as NSHFETs are vulnerable to the self-heating effect (SHE) because of their confined geometry, which triggers thermal reliability issues [12]–[19]. In particular, it is expected that the high height of CFET makes it difficult for heat to dissipate to the thermal ground. Thus, finding a way to alleviate the SHE in CFET by stacking nNSHFETs and pNSHFETs is important. However, there has been no qualitative analysis of the optimal design of CFETs based on both thermal characteristics and CMOS inverter performances for different dimensions.

For the first time, the device design guideline of the 3-nm node CFET is investigated from the perspective of thermal characteristics and CMOS inverter performance with carefully calibrated 3-D TCAD. First, the CMOS inverter performances of $C_{\text{eff}}$, $R_{\text{eff}}$, $f$, and PDP in the 3-nm node CFET are analyzed by varying the dimensions of the number of stacked channels ($N_{\text{nMOS}}$, $N_{\text{pMOS}}$), distance between the nanosheets ($D_{\text{ns}}$), n/pMOS separation distances ($D_{\text{n/p}}$), nanosheet channel thickness ($T_{\text{ns}}$), and nanosheet width ($W_{\text{ns}}$). Moreover, the maximum lattice temperature ($T_{\text{max}}$) and thermal resistance ($R_{\text{th}}$) is evaluated in terms of different dimensions. Finally, the impact of the device design on the inverter performance and thermal characteristics is analyzed from the perspective of down-scaling.

### II. MODELING METHODOLOGY

The 3-nm node CFET was designed for the front-end-of-line (FEOL) based on the IRDS 2020 high-performance specification in Sentaurus 3-D TCAD vQ 2019. The structure of CFET was based on the experimental reference of Intel [9]. Fig. 1 shows the schematics of the 3-nm node CFET. Fig. 1 (a) shows a 3-D bird’s eye view of the CFET. Fig. 1 (b), (c), (d), and (e) show the cross-sectional view of the 3-nm node CFET and schematics with structural parameters. Table 1 shows the structural parameters used in TCAD, and the reference values of each parameter are underlined. For CFET, nMOS-on-pMOS structure is assumed based on [9]. The physical gate length ($L_g$) was set as 16 nm. For the gate oxide, 2-nm thick HfO$_2$ was used. In addition, gate metal, which has a work function of 4.54 eV and 4.8 eV, is used for nMOS and pMOS of CFET respectively. Fig. 2 shows schematics of the thermal parameters used in TCAD. Thermal modeling is based on the simulation setup of the conventional model suggested by [12]–[19]. As shown in Fig. 2 (a), the CFET locates on a wide silicon substrate and is surrounded by SiO$_2$. Thermal boundaries are then set on the top and bottom surfaces for realistic heat dissipation modeling [12]. The thermal parameters used in the simulation

### TABLE 1. Structural parameters used for 3-nm complementary FET and reference values (underlined).

| Quantity          | Value         | Description                                      |
|-------------------|---------------|--------------------------------------------------|
| $L_{\text{gate}}$ | 16 nm         | Physical gate length                             |
| $T_{\text{oxide}}$| 2 nm          | Gate oxide thickness                             |
| $N_{\text{nMOS}}$ | 1 2 3 4       | Number of stacked n-channel                      |
| $N_{\text{pMOS}}$| 2 3 4 5       | Number of stacked p-channel                      |
| $W_{\text{ns}}$  | 15.17.5 22.5 25 nm | Nanosheet channel width                        |
| $T_{\text{ns}}$  | 6.7 8.9 10 nm | Nanosheet channel thickness                      |
| $D_{\text{ns}}$  | 7.8 10 nm     | Distance between nanosheets                      |
| $D_{\text{n/p}}$ | 20 30 40 50 60 70 nm | n/pMOS separation                             |
| $L_{\text{SD}}$  | 10 nm         | Source/drain (S/D) length                       |
| $L_{\text{sp}}$  | 6 nm          | Spacer length                                   |
| $N_{\text{d}}$   | $5 \times 10^{13} \text{ cm}^{-2}$ (Acceptors) | Interface trap conc. of nMOS                    |
| $N_{\text{a}}$   | $1 \times 10^{18} \text{ cm}^{-3}$ (Donors) | Interface trap conc. of pMOS                    |
| $D_{\text{ns}}$  | $1 \times 10^{18} \text{ cm}^{-3}$ | Substrate doping concentration                  |
| $N_{\text{d}}$   | $1 \times 10^{18} \text{ cm}^{-3}$ | Substrate doping concentration                  |
| $N_{\text{d}}$   | $1 \times 10^{18} \text{ cm}^{-3}$ | Local doping concentration                      |
TABLE 2. Thermal parameters used for 3-nm complementary FET.

| Parameter                        | Value (W/K m) |
|----------------------------------|---------------|
| STI (SiO₂)                       | 1.4           |
| M0 (W)                           | 175           |
| Silicon                          | Reference [10], [11], [12] |
| Metal gate (W)                   | 175           |
| Nitride                          | 18.5          |
| Gate oxide (HFO₂)                | 2.3           |
| Thermal contact resistance       | Value (cm²-K/W) |
| Si/HFO₂ interface                | 9 x 10⁻⁴[10], [11], [12] |
| BEOL                             | 2 x 10⁻³[12], [13] |
| Substrate                        | 5.4 x 10⁻⁴[12], [13] |
| Thermal boundary condition       | 300 K         |

FIGURE 2. (a) 3-D bird’s eye view of the 3-nm node CFET with thermal boundary conditions. (b) Divided regions for setting thermal parameter of 3-nm node CFET in table 2.

are listed in Table 2. Fig. 2 (b) shows the device regions where the thermal parameters are used.

Fig. 3 shows the method of calibration of the TCAD to reference for realistic simulation. The calibration of TCAD is performed for the transfer characteristic and voltage transfer characteristic (VTC) of CFET (Fig. 3 (a) and (c)) from the experimental reference with a gate length of 75 nm [7]. This is the only fabricated CFET with vertically stacked NSHFETs that can operate as inverters with a high on-state current and low SS. Then, a 3-nm node CFET is designed using the IRDS specifications, as shown in Table 1, and the DC performances and inverter performances were calculated as shown in Fig. 3 (b) and (d) [11], [20], [21]. For each device with an nMOS and pMOS, the transfer characteristics of the nMOS and pMOS were used to simulate realistic electrothermal carrier transportation with the parameters listed in Table 2 [12]–[19].

III. RESULTS AND DISCUSSIONS

A. INVERTER PERFORMANCE CHARACTERISTICS OF CFET FOR DIFFERENT DIMENSION PARAMETERS

To investigate the inverter performance characteristics, f, power, C_eff, and R_eff of the 3-nm node CFET were compared for different structures and dimensions, as shown in Figs. 5 and 6. In Fig. 5, f, PDP, C_eff, and R_eff for different numbers of stacked channels of nMOS and pMOS (N_nMOS, N_pMOS) are compared. For N_nMOS and N_pMOS, N_nMOS/N_pMOS of 1/2, 2/3, 3/4, and 4/5 were used to compare inverter performances of the 3-nm node CFET for different N_nMOS and N_pMOS. For each device with N_nMOS/N_pMOS, the transfer characteristics of the nMOS and pMOS were calibrated to obtain the same VTC characteristics. N_nMOS was chosen for a higher number than N_pMOS to match the drain current, because the mobility of nMOS is much lower than that of pMOS. Fig. 5 (a) shows an optimal point that power supply voltage (V_{dd}) is set to 0.7 V by IRDS 2020. For the transient response, the inverter performance is calculated based on the fan-out of the 3 (FO3) logic inverter circuit, as shown in Fig. 4 (a) [20], [21]. Here, C_eff is calculated from the general equation C_eff = total gate capacitance (C_{gg}) + total drain capacitance (C_{dd}) + 3 (number of fan-out devices) x fan-out capacitance (C_{fo}) [20], [21]. C_{fo} is assumed to be the same as C_{gg}; therefore, C_eff can be 4 x C_{gg} + C_{dd}. C_{gg} and C_{dd} are extracted from a single CFET device. Here, C_{gg} includes the gate-to-drain capacitance (C_{gd}), gate-to-source capacitance of nMOS (C_{gs,n}), and gate-to-source capacitance of pMOS (C_{gs,p}). For the performance parameters, f is extracted using the equation shown in Fig. 4 (b). Power is calculated using C_eff x f x V_{dd}², PDP is calculated as power/f, and R_eff is calculated as 1/(C_eff x f) [20], [21].
allows the highest \( f \) to exist. This is because \( C_{\text{eff}} \) and \( R_{\text{eff}} \) have a trade-off relationship, as shown in Fig. 5 (b), where \( f \) is calculated as \( 1 / (R_{\text{eff}} \times C_{\text{eff}}) \). The increment of \( N_{\text{nMOS}} \) and \( N_{\text{pMOS}} \) induces a higher drive current \( (I_{\text{drive}}) \) because of the large effective width and reduces \( R_{\text{eff}} \); however, \( C_{\text{eff}} \) increases as the gate area and height of the metal via increase. Thus, in Fig. 5 (a), the device with \( N_{\text{nMOS}} \) of 2 and \( N_{\text{pMOS}} \) of 3 shows the highest \( f \). PDP is calculated as \( C_{\text{eff}} \times V_{\text{dd}}^2 \) in general; therefore, PDP is proportional to \( C_{\text{eff}} \) \[20\], \[21\]. Thus, the increment in \( N_{\text{nMOS}} \) and \( N_{\text{pMOS}} \) triggers an increment in \( C_{\text{eff}} \), so PDP increases, as shown in Fig. 5 (b).

In Fig. 6, \( f \), PDP, \( C_{\text{eff}} \), and \( R_{\text{eff}} \) are compared for different values of \( D_{\text{nsh}}, D_{\text{nsh}}/p, T_{\text{nsh}}, \) and \( W_{\text{nsh}} \). For \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \), ranges of 7–11 nm and 20–70 nm were used, respectively. In addition, \( W_{\text{nsh}} \) and \( T_{\text{nsh}} \), ranging from 15 to 25 nm and 6 to 10 nm, respectively, were used. For \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \) in Fig. 6 (a) and (c), an increase in \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \) can reduce \( f \) and increase PDP. The changes in \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \) rarely cause a change in \( R_{\text{eff}} \) as the effective width is constant and \( I_{\text{drive}} \) does not change. Therefore, \( C_{\text{eff}} \) dominantly determines \( f \) for the changes in \( D_{\text{nsh}}, D_{\text{nsh}}/p, \) and \( T_{\text{nsh}} \). Here, the reduction of both \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \) triggers a lower \( C_{\text{eff}} \), as shown in Fig. 6 (b) and (d). This is because the gate fringe electric field overlap is triggered between nMOS and pMOS of the CFET with a vertically stacked structure \[4\], \[10\]. In addition, the reduced height of the metal via decreases \( C_{\text{eff}} \) \[10\]. Thus, \( f \) increases with a reduction in \( D_{\text{nsh}}, D_{\text{nsh}}/p \). Since PDP is proportional to \( C_{\text{eff}} \), the reduction in \( D_{\text{nsh}} \) and \( D_{\text{nsh}}/p \) can decrease PDP with lower \( C_{\text{eff}} \). On the other hand, in Fig. 6 (e) and (g), the device with the optimum values for \( T_{\text{nsh}} \) of 8 nm in Fig. 6 (e) and \( W_{\text{nsh}} \) of 20 nm in Fig. 6 (g) is required for the highest \( f \). This is because \( C_{\text{eff}} \) and \( R_{\text{eff}} \) have a trade-off relationship, as shown in Fig. 6 (f) and (h). Both \( T_{\text{nsh}} \) and \( W_{\text{nsh}} \) are related to the effective width of the channel; thus, their increase increases the current and the gate area. Thus, a higher effective width decreases \( R_{\text{eff}} \), and a larger gate area increases \( C_{\text{eff}} \) with increasing \( T_{\text{nsh}} \) and \( W_{\text{nsh}} \). In addition, the increase in \( C_{\text{eff}} \); PDP increases with increasing \( T_{\text{nsh}} \) and \( W_{\text{nsh}} \), as shown in Fig. 6 (f) and (h).

Furthermore, in Fig. 5 and 6, \( C_{\text{eff}} \) changes linearly by different dimensions, but \( R_{\text{eff}} \) changes non-linearly. The reason of \( R_{\text{eff}} \)’s non-linearity is the impact of thermodynamic physics. Increment of current with increment of dimensions increases device temperature. The increased temperature degrades current and increases \( R_{\text{eff}} \). For generated heat, electron joule heat and hole joule heat are calculated by equation as follow \[19\]:

\[
\text{Electron/hole joule heat (}\sim T) = \frac{\overline{J_n}^2}{qn\mu_n} \quad \text{or} \quad \frac{\overline{J_p}^2}{q\mu_p}
\]  

\[(1)\]
are the absolute thermoelectric powers, and \( \nabla \phi \) are the electron and hole quasi-Fermi potentials. The \( P \) occurs by different dimensions.

In equation (2), \( \hat{J}_n \) and \( \hat{J}_p \) which considers lattice temperature affects by lattice temperature (T) which is proportional to \( \hat{J}_n^2 \) and \( \hat{J}_p^2 \) in equation (3). Therefore, non-linearity of \( R_{th} \) occurs by different dimensions.

### B. THERMAL CHARACTERISTICS OF CFET FOR DIFFERENT DIMENSION PARAMETERS

To investigate the electrothermal characteristics, \( T_{max} \) and \( R_{th} \) of the CFET with different dimensions were compared. \( T_{max} \) is the absolute value of the maximum heat generation during device operation. \( R_{th} \) is a general parameter used to compare the heat dissipation ability from the device to the thermal ground between different devices, assuming that they have the same power [12]–[19]. Fig. 7 shows the method for extracting \( T_{max} \) and \( R_{th} \). Fig. 7 (a) shows \( T_{max} \) and the maximum \( I_{drive} \) during inverter operation for different \( V_{in} \) values in the range of 0 V to 0.7 V. In the case of the device temperature during inverter operation, it is well known that it finally converges to the maximum temperature of the DC if the inverter operation pulse is continuously injected. Here, the maximum value of \( T_{max} \) was extracted to calculate \( \Delta T_{max} \), where \( \Delta T_{max} = max(T_{max} - \text{initial temperature} \ (300 \, \text{K}) \). In addition, \( R_{th} \) and \( I_{drive} \) were extracted. \( R_{th} \) shows correlations between power and temperature and is calculated by the equation below [12]–[19]:

\[
R_{th} = \Delta T_{max} / (V_{DD} \times I_{drive})
\]

where, \( V_{dd} \) is the power supply voltage of 0.7 V. Fig. 7 (b) illustrates the visualized lattice temperature distribution of the 3-nm node CFET.

Here, \( T_{max} \) is located at the nMOS’s lower channel and does not change with different dimensions. This is because \( nMOS \) and \( pMOS \) have the same \( I_{drive} \) during inverter operation, but \( nMOS \) has a lower number of stacked channels compared to \( pMOS \), so \( nMOS \) has a relatively high current density and triggers a high temperature. In addition, \( nMOS \)’s lower channel has a longer distance to the thermal ground than the other channels, and thermal coupling severely occurs [12]–[19]. Therefore, \( nMOS \)’s lower channel had the highest temperature.

In Fig. 8, \( \Delta T_{max} \) and \( R_{th} \) of 3-nm node CFET for varying (a) distances between nanosheet \( (D_{nsh}) \), (b) \( n/pMOS \) separation \( (D_{n/p}) \), (c) nanosheet thickness \( (T_{nsh}) \), and (d) nanosheet width \( (W_{nsh}) \).

FIGURE 7. (a) Maximum lattice temperature and drive current of default 3-nm node CFET in DC inverter operation. (b) Visualized lattice temperature distribution of 3-nm node CFET, which shows the region of \( T_{max} \).

FIGURE 8. (a) Net increment of maximum lattice temperature (\( \Delta T_{max} \)) and (b) thermal resistance \( (R_{th}) \) of 3-nm node CFET for different number of stacked channels.

FIGURE 9. \( \Delta T_{max} \) and \( R_{th} \) of 3-nm node CFET for varying (a) distances between nanosheet \( (D_{nsh}) \), (b) \( n/pMOS \) separation \( (D_{n/p}) \), (c) nanosheet thickness \( (T_{nsh}) \), and (d) nanosheet width \( (W_{nsh}) \).
in $D_{nsh}$ and $D_{n/p}$, the heat dissipation ability improves as the thermal coupling weakens because of the large distance between channels or devices, which are sources of heat. Therefore, both $\Delta T_{\text{max}}$ and $R_{\text{th}}$ decrease with increasing $D_{nsh}$ and $D_{n/p}$. However, it is notable that the values of $\Delta T_{\text{max}}$ and $R_{\text{th}}$ for different $D_{nsh}$ and $D_{n/p}$ are much smaller than those of the other parameters and are thus negligible. In Fig. 9 (c), $R_{\text{th}}$ shows turn-around at $T_{\text{sh}} = 8$ nm. With increment of $T_{\text{sh}}$ from 6 nm to 8 nm, impact of increment of $I_{\text{drive}}$ is dominant compared to the impact of increment of gate area which decide heat dissipation. Thus, increased consumed power by increment of $I_{\text{drive}}$ increases $R_{\text{th}}$. However, for $T_{\text{sh}}$ over 8 nm, the impact of the increment in the gate area becomes dominant, so better heat dissipation decreases $R_{\text{th}}$. Thus, $R_{\text{th}}$ shows turn-around at $T_{\text{sh}} = 8$ nm. For $T_{\text{sh}}$, change of gate area is relatively small compared to other dimension parameters as range of $T_{\text{sh}}$ is small from 6 nm to 10 nm, so impact of $I_{\text{drive}}$ can be relatively high and turn-around occurs unlike other dimension parameters. In Fig. 9 (d) of $W_{\text{sh}}$, the increment of $W_{\text{sh}}$ increases $\Delta T_{\text{max}}$ because it induces a high $I_{\text{drive}}$. However, an increased gate area triggers better heat dissipation, and thus, a reduction in $R_{\text{th}}$ occurs.

Considering both inverter performance and thermal characteristics, it is notable that the reduction in $D_{nsh}$ and $D_{n/p}$ of CFET can improve $f$ and PDP without significant degradation in $\Delta T_{\text{max}}$ and $R_{\text{th}}$.

IV. CONCLUSION

For the first time, the inverter performance and thermal characteristics of a 3-nm node CFET with different dimensions were investigated using calibrated 3-D TCAD. In addition, device design guidelines for CFETs to achieve better inverter performance and thermal characteristics were suggested. First, inverter performances by different $N_{\text{nMOS}}$, $N_{\text{pMOS}}$, $D_{\text{nsh}}$, $D_{n/p}$, $T_{\text{sh}}$, and $W_{\text{sh}}$ were investigated. For $N_{\text{nMOS}}$ and $N_{\text{pMOS}}$, with a reduction in the above parameters, $C_{\text{eff}}$ decreases because the gate area decreases and the height of the metal via is reduced. However, $R_{\text{eff}}$ increases with a decrease in the effective width. Therefore, an optimum $N_{\text{nMOS}}/N_{\text{pMOS}}$ ratio of 2/3 is required for the highest $f$ as a trade-off between $C_{\text{eff}}$ and $R_{\text{eff}}$. For $D_{\text{nsh}}$ and $D_{n/p}$, their reduction decreases the height of the metal gate and source/drain metal via, thereby reducing $C_{\text{eff}}$ without changing $R_{\text{eff}}$. Thus, the reduction of $D_{\text{nsh}}$ and $D_{n/p}$ can increase $f$ and decrease PDP. Subsequently, the thermal characteristics by different $N_{\text{nMOS}}$, $N_{\text{pMOS}}$, $D_{\text{nsh}}$, $D_{n/p}$, $T_{\text{sh}}$, and $W_{\text{sh}}$ were investigated. For the different $N_{\text{nMOS}}$ and $N_{\text{pMOS}}$, their reduction decreases the gate area and disturbs the heat dissipation from the devices to the thermal ground, thereby increasing $R_{\text{th}}$. In the case of $D_{\text{nsh}}$ and $D_{n/p}$, their reduction induces a higher $R_{\text{th}}$ because of severe thermal coupling, but the change in $R_{\text{th}}$ is negligible. Considering both inverter performance and thermal characteristics from the perspective of down-scaling, it is notable that the reduction in $D_{\text{nsh}}$ and $D_{n/p}$ of CFET can improve both $f$ and PDP without severe degradation. This is different from the other dimension parameters, which show a severe trade-off between inverter performance and thermal parameters. This study can provide crucial insights into the device design of CFET for a sub-3-nm node.

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