A new method to improve the phase noise performance of the frequency synthesizer for UHF RFID

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Abstract: This paper presents a fractional-N frequency synthesizer for ultra high frequency radio frequency identification (UHF RFID) reader application. With the use of a novel parallel dual inductance resonator in the inductance and capacitance based voltage-controlled oscillator (LC-VCO), the resonator cavity loss was greatly reduced as well as the temperature drift was suppressed. At the same time, the loop linearity is improved by the use of operational amplifier tracking technology. The chip is fabricated in a 0.13\textmu m RF CMOS technology with a single 1.2 V power supply. The synthesizer provides a tuning range from 840 MHz to 960 MHz. The worst phase noise of \(-95\) dBc/Hz in band, \(-110\) dBc/Hz@100 kHz offset, \(-135\) dBc/Hz@1 MHz offset with a reference spur of \(-78\) dBc are measured at a center frequency of 920.125 MHz. A 0.95 ps integrated RMS jitter and an 18.5 mW power dissipation are obtained at a temperature range from 0°C to 85°C.

Keywords: fractional-N frequency synthesizer, LC-VCO, dual inductance resonator

Classification: Integrated circuits

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1 Introduction

As a real-time communication technology, UHF RFID works between 840 MHz and 960 MHz, which is a key technology in the application of Internet of Things (IoT). Compared with other bands of RFID technology, UHF RFID has the advantages of longer reading distance, higher security and lower application cost. UHF RFID system consists of a reader and a tag. Passive tags are the most widely used tags in UHF RFID technology.

During communication, the reader sends a continuous carrier wave to provide energy for the tag and waits for the tag to return a back-scatter signal, thus a communication connection between the reader and the tag is established. Subsequently, the reader sends an ASK modulation signal to the tag through PIE encoding form, and the tag returns an ASK signal through FM0 or Miller encoding form [1].

Like other wireless communication systems, RFID readers need a synthesizer to modulate and demodulate baseband signals. The performance of the synthesizer determines the performance of the RFID reader. In this paper, a fractional frequency division frequency synthesizer for UHF RFID reader chip is proposed. A novel parallel dual inductance resonator in the LC-VCO is adopted to obtain a low noise,
low power consumption and broadband tunable frequency synthesizer. Relevant design details and experimental results are presented in subsequent chapters.

2 System structure

According to the communication mode of the RFID system, while the reader receives the back-scattered signal from the tag, the reader needs to send an unmodulated continuous carrier wave to provide energy for the tag. Due to the same carrier frequency, it’s impossible for the reader’s receiver to filter out the noise introduced by the continuous carrier. Continuous carrier will not only cause the RF front-end saturate, but also enhance the receiving channel signal noise, thus reducing the receiving sensitivity. Continuous carrier is essentially the local oscillator (LO) signal after amplification, so its signal spectrum is the same as the phase noise spectrum of the LO.

The phase noise introduced by continuous carrier is much larger than the thermal noise of devices, so the noise floor of receiver link (Rx) is dominated by the phase noise of the carrier. To reduce the carrier induced noise, either the self-interfere power or its phase noise should be minimized. The transmitter link to receiver link (Tx-Rx) isolation should be maximized to minimize the self-interfere power, but it is restricted to be about 20–30 dB by the poor isolation of the directional coupler. The cost will increase greatly once the double antennas are used. And also, reducing the transmission power will reduce the communication distance. Thus, it is particularly important to reduce the phase noise of the LO [2].

In order to ensure that the reader can meet the requirements of various protocol specifications, the minimum frequency hopping interval of synthesizer is 100 kHz. Therefore, fractional frequency division structure is very suitable for this application. In addition, sigma-delta modulator will randomly distribute the fractional spur of the frequency synthesizer, and apply a high pass shaping effect on the in-band noise, which leads to a better suppression on the in-band noise of the frequency synthesizer [1, 2, 3].

There are adjacent channel interference and self-mixing phenomenon of local oscillator signal in RFID reader. According to European Telecommunication Standards Institute (ETSI) application requirements, the phase noise requirement at 200 kHz offset from carrier is $-116$ dBc/Hz. In fact, if less channel interference is required, better phase noise is needed.

Besides, the phase noise in band will be converted from phase modulation (PM) to amplitude modulation (AM) through a non-linear power amplifier (PA), which will indirectly increase the AM noise of the transmitter and deteriorate the sensitivity of the chip. In order to reduce the AM noise the in band phase noise is below $-95$ dBc/Hz.

Based on the above analysis, Fig. 1 illustrates the system structure of the proposed fractional-N frequency synthesizer for RFID reader chip. It comprises a LC-VCO, a programmable frequency divider controlled by a sigma-delta modulator (DSM), a phase and frequency detector (PFD), a charge pump (CP), a low-pass loop filter (LPF), and an auto frequency calibration (AFC) circuit. The LC-VCO is designed to operate around 3 GHz–4 GHz, which is four times of the LO frequency.
In order to restrain the in-band noise and the noise of sigma-delta modulator, a fourth-order LPF is used.

3 Circuit design & simulation

3.1 VCO design

The out-band noise performance is dominated by the VCO unit. According to the Lesson formula, the phase noise expression can be obtained as Eq. (1) [4].

\[ \varphi_{n-out}^2 = \frac{2kTR}{v_{sig}^2} \cdot \frac{1}{4Q^2} \cdot \left( \frac{\omega_0}{\Delta \omega} \right)^2 = \frac{2kT}{P_{sig}} \cdot \frac{1}{4Q^2} \cdot \left( \frac{\omega_0}{\Delta \omega} \right)^2 \]  

In Eq. (1), \( \varphi_{n-out} \) is the phase noise, \( Q \) is the quality factor of the resonator, \( \omega_0 \) is the oscillation frequency, \( \Delta \omega \) is the offset frequency and \( P_{sig} \) is the power of the oscillation signal. Eq. (1) shows that the phase noise of VCO is squared positive proportional to the oscillation frequency and squared inversely proportional to the Q value, offset frequency and signal power [4]. To improve the phase noise performance of VCO, the direct way is to increase the Q value of the resonator and the power consumption of the oscillator.

The Q value of resonator is determined by the inductance and variable capacitance simultaneously. In CMOS process, the Q value of variable capacitance is very high, but the Q value of inductance is as low as about 20, there is a parallel relationship between them, so the Q value of resonator is dominated by the Q value of inductance. An on chip inductance can be modeled as an ideal inductance with a serial resistance, and the value of Q can be modeled as \( j\omega L_s/R_s \), in which the \( L_s \) is the value of ideal inductance, and the \( R_s \) is the series resistance. As the area of inductance increases faster than its circumference, the value of the ideal inductance increases faster than the series resistance. The larger the inductance value, the higher the Q value. Therefore, when designing a LC VCO, the value of inductance should be increased as much as possible to improve the Q value, but the upper limit of inductance’s value will be affected by the operating frequency range.

The capacitances of the LC VCO are usually composed of switched capacitance arrays to obtain a sufficient oscillation frequency range [4, 5, 6]. If all the capacitances are connected, the frequency is the lowest, and the capacitance is recorded as \( C_{on} \). Conversely, when all the capacitances are turned off, the oscillation frequency is the highest, and the capacitance is recorded as \( C_{off} \). The other capacitances and parasitic capacitances in the circuit are equivalent to be \( C_{fix} \). Then two sets of frequency values can be obtained as follows.

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**Fig. 1.** The system structure of the fractional-N frequency synthesizer
\[ f_{\text{max}} = \frac{1}{2\pi\sqrt{L(C_{\text{fix}} + C_{\text{off}})}} \]  
(2)

\[ f_{\text{min}} = \frac{1}{2\pi\sqrt{L(C_{\text{fix}} + C_{\text{on}})}} \]  
(3)

In ordinary situation, the value of \( C_{\text{off}}/C_{\text{on}} \) is about 20%–30%, the targeted operating frequency range of the VCO is 3 GHz–4 GHz. Assuming that \( C_{\text{off}}/C_{\text{on}} = 25\% \), \( C_{\text{fix}} = 2 \text{pF} \), then a maximum value of inductance can be obtained is about 0.6 nH. A value of 0.5 nH is chosen to leave a 20% margin.

From the above analysis, it can be seen that a large inductance value and a large Q value of the inductance are needed to achieve the low noise, low power consumption requirements. While to obtain a wide tuning range, a smaller inductance value is needed. Therefore, a compromise consideration is needed to meet the above design requirements.

In TSMC013 RF CMOS process, the peak Q value of a 0.5 nH inductance is about 12 at this frequency. Calculated by Eq. (1), the phase noise is difficult to meet the requirements. A novel method of parallel inductance is advised in this paper. As shown in Fig. 2, instead of normal single inductance LC-VCO, two 1 nH inductances are implemented in parallel mode. At this time, the Q value of a single inductance is larger and the peak value is 18.5. Therefore, the Q value of an equivalent resonator is larger than that of a single inductance mode, and the cavity loss is reduced. Compared with the single inductance mode, the phase noise can be increased by 3–6 dB. Moreover, in parallel connection mode, the equivalent inductance value can be reduced while the phase noise remains unchanged, so the tuning range can be greatly increased with a flexible available inductance value.

The design method proposed in this paper can be extended to broadband frequency synthesizer design. In addition, VCO with dual inductance has better frequency-temperature characteristics, which can reduce the frequency drift of the synthesizer.

With the use of a 0.13 µm RF CMOS process, two forms of VCO are compared and simulated. Keeping the parameters of other components in the VCO circuit
unchanged, just changing the inductance realization mode, one is dual parallel inductance based VCO, the other is single inductance based VCO. The main performance indicators of VCO are simulated and the simulation results are shown in the following figure.

Fig. 3a is the simulated phase noise result obtained by single mode, and Fig. 3b is the phase noise curve obtained by dual parallel mode. At a carrier frequency of about 3.6 GHz, the phase noise is $-123.6$ dBc/Hz offset from 1 MHz at a parallel mode, rather than $-118$ dBc/Hz offset from 1 MHz at a single mode. It can be seen that VCO with parallel connection has smaller cavity loss, its phase noise curve behaves about 6 dB better than that with single inductance mode at 1 MHz offset frequency.

Fig. 4a is a temperature drift curve simulated in single mode. Fig. 4b is a phase noise curve obtained in parallel mode. The obtained KVCO is 60 MHz/V, and the frequency drift in the temperature range of $-40^\circ$C to $85^\circ$C in single inductance mode is about 18.83 MHz, while the frequency drift is 8.5 MHz in dual inductance mode. It can be seen that the temperature drift characteristics of VCO can be effectively reduced by using dual inductances. In parallel inductance mode, the L-T curve shows a negative temperature coefficient, while in single inductance mode,
the L-T curve shows a positive temperature coefficient [7, 8, 9]. The curve of the capacitance varies with temperature shows a positive temperature trend. Therefore, the temperature drift in parallel connection mode shows a smaller variation than that in the single connection mode. It does not require the design of additional compensation circuit to suppress temperature drift, which will reduce the difficulty of circuit design.

In order to achieve a broadband tuning range with high linearity, a coarse 7 bit capacitance tuning array with high three-bit binary code and low four-bit thermometer code is applied. And also, constant KVCO technology is applied to improve the linearity of VCO.

3.2 Charge pump design

One of the problems in charge pump design is the mismatch between PMOS current source and NMOS current source. Especially when the output voltage is off center, the limited output impedance of MOS devices leads to a mismatch between UP and DOWN currents, and it is necessary to increase the output impedance of current source as much as possible. An additional operational amplifier is used to make the UP current and the DOWN current track with each other.
As shown in Fig. 5, due to the negative feedback effect of the operational amplifier, the leakage voltage of the bias tube at the output end of the charge pump in the circuit is always equal to that of the bias tube in the reference bias circuit, so the current of UP and DOWN can follow the current of the reference source accurately [10]. As the current flowing through the two bias tubes is always equal, the UP current and the DOWN current will not be affected by the variation of output voltage, thus ensuring good dynamic and static linearity of the charge pump.

3.3 Other circuits

A 3-order MASH structure is implemented in sigma-delta modulator, which has a good stability and noise shaping effect. Its output is connected to the control bits of the programmable divider. The TSPC structure is used as a pre-divider in the programmable divider to obtain a higher operating frequency range. The output carrier is obtained by two cascade divider-by-two circuits [11, 12, 13].

Other modules such as AFC are conventional designs. Since the VCO has good phase noise performance, a fourth-order loop filter with a bandwidth of 50 kHz is applied to suppress the in-band noise. An external capacitance is used for the zero capacitance in the loop filter, and the other zero-pole capacitances are all on chip devices.

4 Experimental results

The frequency synthesizer is fabricated by 0.13 um RF CMOS 1P7M technology with a single power supply voltage of 1.2 V. Fig. 6a shows the layout of the frequency synthesizer and Fig. 6b shows the micro-photo of the die chip, and the area of the die chip is 1.72 mm × 0.95 mm.

Frequency synthesizer provides local oscillator signal to the UHF RFID reader, and the reader transmits continuous carrier through Tx link. The phase noise of the fractional-N frequency synthesizer is measured though the continuous carrier by Agilent E5052B as shown in Fig. 7 [14].

At the temperature of 85°C, the output power is about 6 dBm. Phase noise is measured to be −95 dBc in-band, −110 dBc/Hz at 100 kHz offset and −135 dBc/Hz at 1 MHz offset when the output carrier frequency is 920.125 MHz. The integrated noise is −48 dBc and integrated jitter is 0.95 ps, which can meet the design requirements. As can be seen from the figure, the Tx noise floor has some influence on the far-end phase noise, so the noise floor needs to be subtracted to
achieve a more accurate and better value. For the targeted channel spacing, the fractional spur is suppressed by the long term sigma-delta modulator, a measured reference spur about $-78$ dBc at 24 MHz offset is measured as Fig. 7 depicted.

Fig. 8 shows the measured VCTRL over the whole temperature range when the frequency is 920.125 MHz, without any additional temperature compensation circuit. VCTRL varies from 502 mV to 700 mV over a $-40^\circ$C to $85^\circ$C temperature range, which corresponding to a measured 12 MHz frequency drift. The frequency synthesizer is still locked during temperature variation.

Table I summarizes the measured performance of the frequency synthesizer together with other published fractional-N synthesizers for comparison. The frequency synthesizer proposed in this paper has good noise and power performance.

Fig. 6. a. Layout of the frequency synthesizer  
   b. Micro-photo of the frequency synthesizer
**Fig. 7.** The measured phase noise (85°C)

**Fig. 8.** The measured VCTRL drifts with temperature

**Table I.** Comparison of the proposed frequency synthesizer

| Reference      | Ref [2] | Ref [3] | Ref [8] | Ref [14] | This paper (in worst case) |
|----------------|---------|---------|---------|----------|----------------------------|
| Process        | 0.18 µm | 0.18 µm | 65 nm   | 65 nm    | 0.13 µm CMOS               |
| Operating      | 1.06–1.4| 1.508–1.923 | 2       | 3.0–3.6  | 0.84–0.96 µm CMOS          |
| frequency (GHz)|         |         |         |          |                            |
| Operating      | 0.8     | 1.8     | 1.8/1.1 | 1.1      | 1.2                        |
| voltage (V)    |         |         |         |          |                            |
| Power          | 6.2     | 21      | 70/15   | 77       | 15.5                       |
| consummation (mA) |       |         |         |          |                            |
| Fractional spur (dBc) | −70 | NA      | NA      | −57      | None                       |
| Reference spur (dBc) | −84 | NA      | NA      | −78      |                            |
| Phase noise of the PLL |       |         |         |          |                            |
| @1 MHz         | −121 dBc/Hz | −120.7 dBc/Hz | −136 dBc/Hz | −104 dBc/Hz | −135 dBc/Hz @200 KHz @1 MHz |
| offset         |         |         |         |          |                            |
| RMS jitter (ps) | NA      | NA      | NA      | NA       | 0.95                       |
5 Conclusion

This paper presents a low power, low voltage and wide tuning range frequency synthesizer for RFID reader. A dual inductance structure to reduce the loss of the resonator and an operational amplifier tracking technique are applied to optimize the linearity of the charge pump. The test results show that the frequency synthesizer can achieve a good noise performance. The proposed design method can be applied to other CMOS process frequency synthesizer for the lack of high quality factor inductance.