Wearable and skin electronics benefit from mechanically soft and stretchable materials to conform to curved and dynamic surfaces, thereby enabling seamless integration with the human body. However, such materials are challenging to process using traditional microelectronics techniques. Here, stretchable transistor arrays are patterned exclusively from solution by inkjet printing of polymers and carbon nanotubes. The additive, non-contact and maskless nature of inkjet printing provides a simple, inexpensive and scalable route for stacking and patterning these chemically-sensitive materials over large areas. The transistors, which are stable at ambient conditions, display mobilities as high as 30 cm² V⁻¹ s⁻¹ and currents per channel width of 0.2 mA cm⁻¹ at operation voltages as low as 1 V, owing to the ionic character of their printed gate dielectric. Furthermore, these transistors with double-layer capacitive dielectric can mimic the synaptic behavior of neurons, making them interesting for conformal brain-machine interfaces and other wearable bioelectronics.
Skin-like bioelectronics enables user-imperceptible integration of electronics directly on the body for applications, such as sensing biological signals or enhancing biological functions. Hence, it requires the development of devices with the same form factor, mechanical properties, and chemical characteristics of human skin. This includes large area, softness, stretchability, and biocompatibility. The two main strategies to achieve stretchable electronics are patterning inorganic materials on pre-strained substrates to form in-plane and out-of-plane serpentines or buckles, and the use of intrinsically stretchable materials achieved by molecular engineering, nano-structuring, or the use of composites. Although the former approach often yields higher performance devices owing to the incorporation of inorganic crystalline materials, it entails significant patterning complexity. The latter approach, on the other hand, requires far less complex patterning, and thus possesses superior potential for device interconnection and integration with high device density.

Intrinsically stretchable materials are usually based on organic materials that can be processed from solution. A particularly promising branch of solution-based processing techniques is inkjet printing, which enables scalable additive patterning over large areas, and at low fabrication cost per surface area. By combining printing techniques with liquid inks of functional organic materials, direct additive fabrication of stretchable electronics with these characteristics can be realized.

Although the traits of printing are desirable for skin electronics, printing techniques have seldom been explored for the integration of intrinsically stretchable materials. The lack of overlap between these two fields thus far is due to the challenges associated with the formulation of such new materials into inks able to be patterned and stacked in a reliable way. Current fabrication procedures for skin-like electronics therefore still strongly rely on techniques such as spin coating, photolithography, shadow mask, or evaporation of active materials that restrict devices to small areas, as well as transfer steps that involve complicated alignments.

Among the most commonly used printing techniques, inkjet (IJ) printing stands out due to its good resolution (\(\sim\)µm); tight control of deposited volume; digital, maskless, and additive character (that enables material usage minimization and process flow simplicity); and non-contact nature. Moreover, the simplicity and low cost of commercially available IJ printers for electronics has vastly popularized its usage. However, IJ printers typically use small nozzle size to enable high resolution as well as controlled deposition, with the potential drawback of nozzle clogging. Reliable IJ printing therefore requires careful design of ink formulations. Despite its limitations, many groups have achieved IJ-printed field effect transistors (FETs) on both rigid and flexible (non-stretchable) substrates using inks of organic semiconductors, as well as semiconducting single-walled carbon nanotubes (SC-SWCNTs). Although SC-SWCNTs must be carefully separated from their metallic counterparts and also tend to aggregate strongly in solution, they present greater thermal stability and higher mobility than organic semiconductors (as high as 30 cm² V⁻¹ s⁻¹ with on-current to off-current ratio, I_on/I_off > 10⁴). Moreover, SWCNTs form networks that have been proven to maintain electrical contact under mechanical strain, making them an excellent semiconductor material for skin electronics.

In most of the reported examples of SWCNTs FETs, however, only one or few functional layers of the final device were patterned by printing, with the deposition/patterning of the gate dielectric often being the limiting factor. Notably, fully-printed SC-SWCNTs FETs, which also include printed/patterned gate dielectrics, comprised of BaTiO_3–polymer composites, poly(vinyl phenol)/poly(methyl silsesquioxane) (PVP/pMSSQ) blends, or polyfluorinated electrolytes have been only recently reported. Polyfluorinated electrolyte can form thermally stable and mechanically flexible gate dielectrics. This type of polymers as well as ion gels exhibit the electric double layer (EDL) effect, which results in high gate capacitance even for thick dielectric layers. This high capacitance facilitated low-voltage FET operation of few volts. However, ion gel electrolytes have poor mechanical strength and are sensitive to moisture. The mentioned demonstrations utilized aerosol-jet printing or a combination of roll-to-roll gravure and IJ printing to fabricate devices on glass and plastic substrates. A fabrication scheme exclusively utilizing IJ printing for all the device functional layers would lower processing complexity and further enhance device integration and interconnection.

Here, we report on the additive fabrication of skin-like electronics by simultaneous deposition, patterning, and aligning of stacks of intrinsically stretchable active materials exclusively using IJ printing. Arrays of FETs are prepared by stacking the following materials: stretchable conductive poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) as the source/drain/gate electrodes and interconnects; a network of SC-SWCNTs as the semiconductive channel; and a fluorinated polymer consisting of a solid-state ionic poly(vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP) as the gate dielectric. Our PVDF-HFP offers the low-voltage operation advantages of EDL without the poor mechanical, chemical, and thermal stability of ion gel counterparts. Ultra-low-voltage operation is desirable for wearables that need to be powered by small batteries or energy harvesters, as well as for devices in direct contact with human body. The final devices present excellent electrical performance in ambient conditions, with average mobility of 27 ± 5 cm² V⁻¹ s⁻¹, I_on/I_off > 10⁴ and maximum transconductance of 47 ± 9 μS. Those parameters are superior to the state of the art for flexible/stretchable CNT-based FETs. Moreover, the electrical nature of the SC-SWCNT network and PVDF-HFP gate dielectric make the FETs strain independent because the tube-to-tube charge transport in SCWNT networks is strain and channel geometry independent (after initial cycling), and the EDL-based capacitance per surface area of the PVDF-HFP is thickness independent above the thickness of the EDL (ca. 100 nm). Indeed, the reported devices present mechanical stretchability, with electrical performance insensitive to strains up to 20% both along the direction parallel and perpendicular to the FET channel. These properties make the fabricated circuits suitable for skin-like applications. In particular, we show that each transistor emulates the synaptic behavior of neurons, which situates this system as an excellent candidate for future in vivo neural interfaces. Due to its outstanding mechanical and electrical properties, the system reported here pushes forward the additive and scalable fabrication of large-area, skin-like electronics for bioelectronics applications.

**Results**

**Fabrication process flow.** Arrays of soft and stretchable FETs like the one shown in Fig. 1 were fabricated by layer-to-layer additive deposition and direct patterning of various intrinsically stretchable materials using IJ printing. The process flow (Fig. 2) was specially designed to ensure chemical compatibility between the different layers by using orthogonal solvents and localized deposition. We also target the minimization of thermal stresses by limiting the maximum process temperature to 160 °C first (to anneal the gate dielectric), and to 70 °C later on when more layers were added to the system. The processing flexibility of IJ printing was paramount to enable this process. Owing to the digital and maskless character of IJ printing, the number, layout, and arrangement of the fabricated devices were easily customized by...
modifying the digital file input to the printer. As a proof of concept of our system, we designed transistors with channel width and length of 1 mm and 50–100 μm, respectively, arranged in arrays of different size ranging from 2 × 3 to 3 × 20 devices with a device density of 20 devices cm⁻². The surface area of a single transistor (without interconnections) was of 2 mm², corresponding to the size of dielectric island. Although these devices are relatively large and widely spaced compared to the maximum integration achievable by IJ printing, which is capable of material placement accuracy of ±5 μm, their dimensions are still smaller than most organic and CNT-FETs or arrays of FETs previously reported.⁸,¹⁷,²⁰,²⁴–²⁸

To facilitate the handling of the system throughout the different fabrication steps, a Si wafer was employed as a rigid holder. The wafer was coated with a water-soluble layer of poly (sodium 4-styrenesulfonate) (PSS) used later on as a sacrificial layer for release of the stretchable system from the rigid substrate. Next, a thick ionic gate dielectric (PVDF-HFP) was IJ printed as square islands (step #1). The thickness-independency of our gate dielectric (Supplementary Fig. 1a) enables the elimination of gate current leakage by printing thick gate dielectric films without decreasing the FET channel capacitance value. Due to the typical unevenness of printed layers, the gate dielectric needed to be thicker than 1.75 μm to avoid gate current leakage (Supplementary Fig. 1b). Optimization of the printing parameters was crucial to ensure a smooth dielectric surface (see Methods section and Supplementary Fig. 1c). Silver contact pads were optionally IJ printed onto the PSS layer on positions adjacent to the dielectric islands to facilitate the final external probing of the devices (this step is not shown in the figure, but a silver contact pad connected to the gate electrode can be seen in the picture of step #17). After annealing the gate dielectric (and optionally the silver contact pads) at 160 °C for crosslinking, its surface was activated with trifluoroacetic acid (TFA) in step #5. IJ printing allows for controlled deposition and simultaneous patterning of the SWCNTs network. The inset of Fig. 2 shows how the tube density (number of tubes per surface area) of an IJ-printed SWCNTs network can be increased with the number of printing passes. Denser networks produced higher currents up to a limit at which the substrate was saturated with SWCNTs. Beyond this limit (corresponding to the 10× layer shown the picture), no improvement in current was observed (Supplementary Fig. 2), likely because the extra printed tubes were removed during the sorting polymer removal process.

The layer-to-layer alignment capabilities of IJ printing allowed for printing of the source and drain electrodes on top of the previously-printed electrodes (step #6), sandwiching the SC-SWCNTs in between. This top and bottom double contact configuration is beneficial for reducing contact resistance as it has been demonstrated before.³⁵

Following, in step #7 the channel was partially encapsulated by locally printing PVDF-HFP dielectric on top and annealing at 70 °C. This step improved the FETs performance and was enabled by the non-contact and additive character of IJ. Interestingly, other authors have also reported advantages in electrical performance for CNT-FETs when using fluorinated polymers to cover the CNTs.³⁶ A system-level encapsulation was then produced by spin coating a film of thermoplastic styrene ethylene butylene styrene (SEBS) elastomer from toluene (step #8). We provided the system with the potential to accommodate more complex circuitry in future applications by enabling a second “metallization” layer on the SEBS encapsulation. This layer allows easy interconnection between different transistors in the array.³⁷ IJ printing of pure toluene was then employed to open via holes on the SEBS encapsulation above the source and drain electrodes to access them (step #9). An extra set of vias were also open away from the source and drain, beyond the area occupied by the gate dielectric, to facilitate the final connection of the devices through the backside. The vias were filled with a dimethylformamide (DMF)-based conductive ink containing graphene and unsorted multiwall CNTs (MWCNT) to provide electrical conductivity, and polyacrylonitrile (PAN) polymer to prevent aggregation⁸ (step #10). This material was used to fill the vias instead of PEDOT:PSS due to the hydrophobicity of PAN, which protected the channel from water absorption in subsequent steps involving water immersion. Moreover, the geometry of the vias (roughly
200 μm × 200 μm in cross-section and only ~1 μm in length) leads to low resistance (<kΩ) even for this low conductivity material that contains high concentration of dielectric PAN.

After filling the vias, the encapsulation layer of SEBS was shortly treated with oxygen plasma (step #11) to facilitate the printability of the stretchable ionic PEDOT:PSS traces that interconnect source and drain electrodes with the external vias (step #12). A stretchable substrate (SEBS of 1.5 mm in thickness or Tegaderm™ from 3M of 20 μm in thickness) was then laminated in step #13, followed by soaking in water to dissolve the water-soluble PSS sacrificial layer and release the devices from the rigid Si substrate onto the stretchable substrate (step #14).

Finally, the substrate was flipped (step #15) and subjected to a short oxygen plasma treatment (step #16) before the gate electrode was IJ printed from ionic PEDOT:PSS (step #17). For improved reliability, the gate dielectric can be optionally made thicker in order to prevent leakage by repeatedly printing PVDF-HFP prior to the deposition of the gate electrode (not shown in Fig. 2). Since the gate low-frequency (<10 Hz) capacitance is independent of thickness, making a thicker layer does not impact it. It is worth noting that IJ printing helps saving extra alignment steps when different materials and layouts are sequentially printed without the need of moving the devices from the printer stage. This is the case for printing the CNTs channel in our
system right after defining the PEDOT:PSS source and drain electrodes, or for filling via holes immediately after opening them. Those processes would have required extra alignment if they were carried out with a different fabrication technique. Most importantly, the dimensional stability of soft materials is typically poor. As a result, after thermal annealing, lamination, or releasing steps, significant and unpredictable expansion/shrinkage of the layout may occur, making subsequent accurate mask alignment difficult. This dimensional mismatch becomes more critical for larger circuits or arrays. Contrary to masking techniques, IJ printing allows for quick re-measurement of the features of the system and automatic adjustment of the layout to accommodate for dimensional changes.

Electrical characterization. The fabricated devices displayed excellent transistor behavior in ambient conditions (Fig. 3a), and remain functional after dwelling in ambient conditions for few days (Supplementary Fig. 3). The ratio between on-current and off-current was $>10^4$ for very low gate and drain voltage of 1 and 1.1 V, respectively, and the gate leakage current was negligible. The mobility $\mu$ can be calculated from the FET saturation regime using the curve $(I_{ds})^{1/2}$ vs. $V_{gs}$ in Fig. 3a as follows:

$$\mu = \frac{2L}{W} \frac{1}{C} \left( \frac{\partial (I_{ds})^{1/2}}{\partial V_{gs}} \right)^2,$$

where $W$ and $L$ are the channel width and length (1000 and}
transistors was maintained when stretched up to 20% strain in the directions perpendicular to the current flow across the channel. On the other hand, some current degradation was observed when the stretching was performed parallel to the current flow direction. This degradation was mostly due to irreversible contact damage, as supported by the fact that the current remained unchanged after relaxing back the device to 0% strain (referred as “back to 0%” in the curve). Regarding the threshold voltage, the variations observed between different measurements are attributed to the memory effect induced by the ionic gate dielectric, rather than to the strain. This memory effect makes the threshold voltage dependent on the time and voltage history of the applied voltages (Supplementary Fig. 5). Beyond 20% strain, the devices failed mainly due to cracking of the gate electrode (Supplementary Fig. 6) and interconnections. Although many of the envisaged skin-electronics applications require devices to operate at strains no larger than the 20–30% achievable by human skin, alternative gate materials and encapsulations are currently being researched in order to expand the stretching margin of our devices for other alternative applications such as robotic skin.

**Application as synaptic transistors.** Owing to its mechanical softness of ~7 MPa (Supplementary Fig. 7), stretchability, and operation in ambient conditions, the reported system presents high potential for interfacing with biological systems. Furthermore, compared to other skin-electronic devices, this system can be operated at low voltage and possesses high transconductance as a result of the ionic nature of the gate dielectric. Those characteristics enable these devices to mimic synaptic neuron behavior with the potential for future in vivo interfacing with neurons as artificial synapse. Figure 4a confirms the synaptic behavior of the reported transistors. The drain–source current, \(I_{ds}\), reversibly responds to pulse trains of very small voltage input at the gate (Fig. 4b), reproducing typical excitatory postsynaptic current (EPSC) found in biological dendrites. The low voltage (of tens of mV) applied at the gate emulates the presynaptic action potential spikes fired by a biological axon and a presynaptic membrane. This finding suggests that the migration of the ions in the gate dielectric is comparable to the dynamics of neurotransmitters in the synaptic cleft, which allows chemical transmission but is electrically insulating. The nature of the ionic gate dielectric underlies the mechanism of short-term plasticity (STP) as previously reported in other synaptic devices using ionic gel. 

Synaptic plasticity is defined as the variation in the strength of a synapse’s response over time upon external stimuli. STP can modify a synapse for a time scale from tens of milliseconds to a few minutes and it plays a role in encoding temporal information in auditory and visual signals. In our transistors, as a result of a single gate voltage spike (~80 mV during 20 ms), ions migrate to the dielectric interface, but quickly relax back to their initial equilibrium state when the voltage pulse ends. This produces a channel current that gradually changes in ~ 50 nA and immediately comes back to its initial state in roughly 300 ms. It is known that short-term synaptic enhancement can be attained when several spikes arrive in rapid succession. Upon application of 32 quick consecutive negative voltage pulses (~80 mV) at 25 Hz at the gate of the transistors, the channel current amplitude changes in 500 nA due to the accumulation of ions at the interfaces of the dielectric. Such large concentration of ions at the dielectric interface requires longer time to relax back to equilibrium, and lead to a short-term memory-like channel current that extend ~2 s beyond the application of the pulses. We demonstrated that in agreement with STP, the greater the number of pulses (Fig. 4a), and their period and amplitude (Fig. 4c), the greater the channel current value changes and the time needed to...
relax back to equilibrium. Finally, besides EPSC, these devices are equally capable of symmetrical inhibitory postsynaptic current (IPSC), where positive voltage spikes make the current to shift on the opposite direction than negative voltage spikes (Fig. 4c).

**Discussion**

Stretchable FET arrays and interconnections have been fabricated by IJ printing using intrinsically stretchable electronic materials, namely ionic PEDOT:PSS, ionic PVDF-HFP, and SC-SWCNTs networks. Each functional material was formulated as an ink and deposited/patterned at ambient conditions without the need of any mask.

The devices exhibit good transistor performance in ambient conditions with an average mobility of $27 \pm 5 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, $I_{on}/I_{off} > 10^4$ and maximum transconductance of $47 \pm 9 \mu\text{S}$. The FETs were capable of sub-volt operation owing to the double-layer behavior of its ionic PVDF-HFP gate dielectric. Such behavior provided high capacitance values and low leakage without the challenges associated with fabricating pinhole-free, thin and uniform printed dielectric layers. Owing to the intrinsically stretchable nature of the materials used, the array survived in-plane stretching to up to 20% strain. However, the main components of the FETs should be capable of surviving even greater strains (see refs. 11,29 and Supplementary Fig. 8). Unfortunately, the potential of the system to stretch beyond this limit could not be evaluated for the current architecture due to decreasing yield beyond 10% strain, as a result of interconnected gate electrode cracking (Supplementary Fig. 6). The cracking of the interconnections was especially severe in the direction parallel to the channel length, which was also perpendicular to the dominant printing direction. Further improvements in printing technology (e.g., by allowing equivalent printing in both $x$ and $y$ directions) can reduce the anisotropy of printed layers and the risk of cracking in the direction perpendicular to printing. Likewise, improving the film thickness uniformity and edge straightness of the gate electrode (Supplementary Fig. 6), and/or encapsulating it could also contribute to enhancing the stretchability of the system.

This system is applicable for various scenarios in wearables, skin electronics, or bioelectronics where low operating voltage, high mobility, air/water stability of electrical characteristics,
softness, conformability, or stretchability are required. The main limiting factor for the system is its switching speed, which is impeded by the slow motion of the ions in the polymeric gate dielectric. However, such slow ionic-like response is desirable for other applications such as synaptic transistors, which intend to mimic neuron-to-neuron communication. Indeed, we demonstrated that the ionic nature of the reported gate dielectric accurately emulates STP, both supporting excitatory and inhibitory postsynaptic currents, for very small input voltages of 40 nV. Therefore, this class of devices can potentially be used in direct contact with neurons (especially when considering that PEDOT: PSS has already shown to have very low contact resistance with neurons43), enabling new advances in neuromorphic engineering and brain–machine interfaces.

Methods

Device fabrication. The II printer used was a Dimatix Material Printer DMP-2831 from Fujifilm with 10 pl droplet size cartridges (standard and chemically resistant liquid crystal polymer (LCP) cartridges).

Rigid substrate holder preparation: A solution of SS (Mw ~ 200 kDa, 30 wt% in H2O from Aldrich, CAS: 25704-18-1) was diluted (1:3v) in deionized water, degassed for 5 min, and filtered through a 0.45 µm pore-size nylon filter before spin coating it at ambient conditions at 2000 rpm for 30 s (acceleration 1000 rpm s−1) on a doped Si wafer previously treated with plasma oxygen (Technics Micro RIE series RIE-1000, 200 W). The wafer was then exposed to 5 s of O2 plasma at 50 W (higher power was shown to be detrimental for the SWCNTs). Then, the wafer was annealed in vacuum and darkness for 30 min at 90 °C and cooled down slowly, then they were immersed for 40 s in a bath of toluene:TFA (99:1) and immediately into a second bath of fresh toluene at 100 °C (bath temperature, 32 °C, temperature, 28 °C). Finally, the devices were annealed again in vacuum and darkness for 30 min at 90 °C and cooled down slowly to evaporate residual toluene and TFA and de-dope the SWCNTs.

Elastomer encapsulation: A solution of SEBS (H1062Z from Kraton® G Polymers) was prepared in toluene (80 mg ml−1, stirred at 50 °C for 30 min), degassed for 5 min, and filtered through a 0.2 µm pore-size PTFE filter before spin coating it at ambient conditions at 1000 rpm for 30 s (acceleration 500 rpm s−1).

Vias opening: Toluene was filtered through a PTFE 0.2 µm pore-size filter and used to fill a standard printer cartridge. The printer parameters were as follows: 30 °C substrate temperature, 28 °C printing head, 4.5 in. H2O meniscus vacuum set point, 20 µm drop-to-drop spacing, 2 nozzle, 6–8 passes, and ~30 V applied voltage to the printer nozzles (the applied waveform details can be found in the supplementary information, Supplementary Fig. 9).

Vias filling (adapted from ref. 38): For the formulation of solution A, multiwall carbon nanotubes (MWCNTs) (Sun Innovations SN7689): PAN (Mn = 130 kDa, Aldrich, CAS: 25014-41-9) (3.11w) were dispersed in N,N-dimethylformamide (DMF) (Aldrich 87-06-6) (11.88w). The mixture was sonicated (Ultrasonicator 750W at 30% of maximum power) for 30 min. Then, the mixture was poured on a doped Si wafer previously treated with plasma oxygen (Technics Micro RIE series RIE-1000, 200 W). The wafer was then exposed to 5 s of O2 plasma at 50 W (higher power was shown to be detrimental for the SC-SWCNTs). The resulting ink was sonicated (Branson 2510 ultrasonic bath) and injected into a standard printer cartridge. The printer parameters were as follows: 50 °C substrate temperature, 33 °C printing head, 4.5 in. H2O meniscus vacuum set point, 30 µm drop-to-drop spacing, 4 nozzles, 65 passes with interlayer waiting time of 30 s, and ~30 V applied voltage to the printer nozzles (the applied waveform details can be found in the supplementary information, Supplementary Fig. 9). PEDOT:PSS can also be used to fill the vias using 4 nozzles and 15 passes, a drop-to-drop spacing of 10 µm, and 35 °C substrate temperature.

Bridges and interconnects: The same ink and parameters used for S/D were employed, except for: 35 °C substrate temperature, 30 µm drop-to-drop spacing, 3 nozzle, and 15 passes. Prior to printing, the surface was exposed to 5 s of O2 plasma at 60 W (higher power was shown to be detrimental for the SC-SWCNTs).

Substrate lamination and transfer process: A film of SEBS was fabricated by coating a solution (150 mg ml−1 SEBS/Toluene) on a microscope slide and letting drying at ambient conditions for 24 h or Tegaderm™ (3M) was laminated on top of the devices. Air bubbles were expelled by gently pushing with a roll. The system was heated up at 50 °C to improve adhesion and cooled down slowly before immersion in deionized water for 5–10 min until the rigid Si holder detached. The system was dried at 70 °C in vacuum and darkness for 30 min and cooled down slowly.

Gate: The same ink and parameters used for S/D were employed, except for: 4 nozzles and 20 passes. Prior to printing, the surface was exposed to 5 s of O2 plasma at 50 W (higher power was shown to be detrimental for the SC-SWCNTs).

Device FET characterization. FET electrical characterization: It was performed using a Keithley 4200-SCS semiconductor parameter analyzer in ambient conditions using a gate voltage sweeping rate of 0.1 V s−1. The mobility has been calculated in the saturation regime as the derivative of the curve (−dx/dVg)1/2 vs. Vg according to Eq. (1). The value for each device is calculated as the average of this saturation regime from the threshold voltage Vth, which is defined as the voltage at which the threshold voltage Vth. To extract the threshold voltage, Vth, we successively applied a rolling linear fitting to each 5-point segment of the curve (−dx/dVg)1/2 vs. Vg. Then, Vth was assumed to be the Vg point where the fitting line with the maximum slope cut the x axis. For the forward and backward voltage sweep, the threshold voltage, Vth, was −0.23 ± 0.032 and 0.332 ± 0.023 V, respectively. As depicted in Fig. 3a, (−dx/dVg)1/2 vs. Vg is roughly linear only for the forward voltage sweep, which makes this value the most reliable one. The final value of saturation-regime mobility and Vth reported in the manuscript correspond to the mean value extracted from 13 single devices with the standard error. Likewise, the mobility has been calculated in the linear regime according to Eq. (2) as the mean of the derivative of the curve (−dx/dVg)1/2 vs. Vg for Vg > 0 (see Supplementary Fig. 4b), using Vth = −1 V and a threshold voltage Vth = 0.2 V, which corresponds to the value extracted for forward sweeping in the saturation regime. The final value of linear regime mobility reported in the manuscript is the mean value of the averaged mobility extracted from nine devices with nine different characteristic of the FETs under strain has been done using a stretchy instrument consisting of two clamps where the extremes of the sample were held and a

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micrometer screw to control the distance between the two clamps while the samples are being stretched. The transconductance, $g_{m}$, was calculated as the maximum of the derivative $-I_{D}$ vs $V_{G}$ (Eq. (3)) for each forward and backward sweeping. The final reported value is the average from 13 devices with the standard error.

**Synaptic behavior of the FETs.** It has been tested using a Keithley 4200-SCS semiconductor parameter analyzer and a pulse measure unit. Prior to the gate voltage stimulation, the device was biased at $V_{G} = -0.6$ V, well beyond the threshold voltage $V_{TH}$, to ensure the complete formation of the channel and a high level of transconductance. The signals shown in the main text are the result of letting the signal stabilize on time for more than 40 s (see transient data in Supplementary Fig. 10), and filtering out the 60 Hz electrical noise using the function goslayfill of MATLAB.

**FET channel capacitance value in quasi-DC mode.** It has been calculated from the charge–discharge equation of a parallel-plates capacitor as explained in ref. 31. A constant voltage was applied with a Keithley 2400 source meter across the capacitor connected in series with a known resistor, while the voltage increase across the capacitor was measured using a Keithley 2636A source meter.

**Mechanical characterization.** The stress–strain curves were obtained using an Instron pull tester at a strain rate of 10% strain min$^{-1}$.

**Data availability**

The authors declare that all data supporting the findings of this study are available within the paper and its supplementary information files. The rest of the data are available from the corresponding author upon reasonable request.

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Author contributions
F.M.-L. and Z.B. conceived the project. F.M.-L. carried out the device fabrication, most of the material preparation, and the electrical characterization. T.Z.G. prepared the SWCNT and unsorted MWCNT inks and assisted in the devices fabrication and FET characterization. U.K. prepared the PEDOT:PSS ink and designed the vias process. C.Z., T.O. and S.W. assisted with the fabrication process. R.P. measured the EDL capacitance. V.R.F. performed the pull tests of the system. Y.K. helped with the electrical characterization of the devices as synaptic FETs. Y.Y. and Z.B. supervised the project.

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