SliT: A Strip-sensor Readout Chip with Subnanosecond Time-walk for the J-PARC Muon $g - 2$/EDM Experiment

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Abstract—A new silicon-strip readout chip named “SliT” has been developed for the measurement of the muon anomalous magnetic moment and electric dipole moment at J-PARC. The SliT is designed in the Silterra 180 nm CMOS technology with mixed-signal integrated circuits. An analog circuit incorporates a conventional charge-sensitive amplifier, shaping amplifiers, and two distinct discriminators for each of 128 identical channels. A digital part includes storage memories, an event building block, a serializer, and LVDS drivers. A distinct feature of the SliT is utilization of the zero-cross architecture, which consists of a CR-RC filter followed by a CR circuit as a voltage differentiator. This architecture enables to generate hit signals with subnanosecond amplitude-independent time walk, which is the primary requirement for the experiment. The test results show the time walk of $0.38 \pm 0.16$ ns between 0.5 and 3 MIP signals. The equivalent noise charge is $1547 \pm 75 \text{ e}^-$ (rms) at $C_{\text{det}} = 33 \text{ pF}$ as a strip-sensor capacitance. Other functionalities such as a strip-sensor readout chip have also been proven in the tests. The SliT128C satisfies all requirements of the J-PARC $g - 2$/EDM experiment.

Index Terms—silicon-strip, CMOS, ASIC, time-walk, low-noise, J-PARC, Muon, $g - 2$, EDM

I. INTRODUCTION

The anomalous magnetic moment ($g - 2$) and the electric dipole moment (EDM) of the muon are sensitive probes of new physics beyond the Standard Model (SM). The SM is a well-tested physics theory, however, there exists a discrepancy in the muon $g - 2$ between the SM prediction [1, 2] and its most precise measurement by the E821 collaboration at Brookhaven National Laboratory (BNL) by more than three standard deviations [3]. The experiment to improve the precision of the muon $g - 2$ is ongoing at Fermilab which uses the upgraded apparatus and plans to increase statistics [4]. On the other hand, another measurement of the muon $g - 2$/EDM is currently under preparation based on a different experimental approach to make a definitive conclusion. This experiment applies an innovative technique using a reaccelerated thermal muon beam at the Japan Proton Accelerator Research Complex (J-PARC) [5].

A primary goal of the experiment is to measure the muon $g - 2$ with a precision of 0.1 parts per million (ppm), which corresponds to the improvement by a factor of five compared to the BNL experiment. At the same time, we seek for the muon EDM with a sensitivity of $10^{-21} \text{ cm}$. The reaccelerated thermal muon beam with a repetition rate of 25 Hz to be used at J-PARC is produced from a thermal muonium source, followed by laser ionization and acceleration. The reaccelerated muons with a momentum of 300 MeV/c are stored under a 3 T magnetic field. The muon makes the orbital cyclotron motion on the mid-plane of the muon storage magnet. A positron tracking detector is placed in the inner region of the muon storage ring for detection of positrons from the muon decay, i.e., $\mu^+ \rightarrow e^+ \nu_e \bar{\nu}_\mu$. Figure 1 shows the concept of the muon storage ring and positron detector in the experiment. The 40 sensor vanes are aligned radially in the detection volume. Each vane consists of single-sided p-on-n type silicon-strip sensors [6] with mutually orthogonal strips on both sides. A two-dimensional position of a positron track is therefore determined by two layers of the strip sensors. Circular positron tracks are reconstructed by connecting two-dimensional positions. The measurement will be performed in an interval following a fill of 33 $\mu$s, which is five times longer than the lifetime of the muon with the momentum of 300 MeV/c.

An integrated circuit with a fast response and high granularity is used to readout data from the silicon strip detectors. The integrated circuit is equipped with a deep buffer memory to store the data for a beam spill. The stored data is readout before the next beam bunch coming. To meet the experimental requirements, a series of custom front-end readout chips named “SliT” has been developed in 180 nm CMOS (Complementary Metal-Oxide Semiconductor) technology. We have newly developed a full module chip named “SliT128C”, and its performance has been tested in the laboratory. In this paper, we describe the ASIC (application-specific integrated circuits) design in section II, report the evaluation setup and the performance test results in section III, and finally give conclusions in section IV.
II. ARCHITECTURE OF THE ASIC

A. Experimental Requirements and Developmental Background

The readout ASIC was implemented in the Silterra 180 nm CMOS technology. Table I summarizes the technological parameters. The front-end ASICs for silicon-strip sensors are demanded to tolerate a high hit rate up to 1.4 MHz per strip with a stability to dynamically changing hit rates by a factor of 150 from the beginning to the end of measurements. In order to minimize the pileups, a pulse width for a typical minimum-ionizing particle (MIP) signal has to be smaller than 100 ns. Here, the pulse width is defined from 1 MIP output, whose width intersects a threshold set at 0.3 MIP. For precise detection of circular positron tracks from the muon decays, a subnanosecond time walk is of critical importance in analog processing blocks of the readout ASIC. The experimental requirements translated to concrete circuit specifications are summarized in Table II.

AC-coupled single-sided p-on-n type silicon-strip sensors with a double-metal structure were made by Hamamatsu Photonics K.K. [6]. The sensor thickness is 320 µm. In this paper, the most probable value of the MIP charge is defined as 3.84 fC, which corresponds to an input charge of about 24,000 e−. A sensor capacitance is approximately 17 pF, and the total detector capacitance $C_{\text{det}}$ seen from an input of the ASIC is estimated to be less than 30 pF. This value includes the parasitic capacitance coming from Flexible Printed Circuits (FPCs), which connect strip sensors with ASICs. The equivalent noise charge (ENC) of less than 1600 e− at $C_{\text{det}} = 30$ pF is required.

In the previous studies, we started from a small-scale analog prototype in Silterra 180 nm CMOS technology. Then we fabricated module-prototype chips named “SliT128A” [7] and “SliT128B” [8]. The module-prototype ASICs included 128 readout channels, buffer memories, and other digital processing circuits to store and cope with timing information from the strip sensors. Since the time-walk performance was measured as ~17.2 ns in SliT128A, we introduced an additional CR block after the semi-Gaussian band-pass filter in SliT128B. As a result, the time walk improved to ~2 ns, however, it was still larger than the requirement. A new readout chip named “SliT128C” improves the overall analog performance, e.g., the ENC, time walk, and jitter, by optimizing all transistor parameters of SliT128B.

Figure 3 shows the photograph of SliT128C. Inputs of 128 channels are aligned in staggered pads with a pitch of 100 µm. The incident signals are processed from the left analog block to the right digital block. Power supply is provided from the top and bottom pads only, and digital outputs are accessed on the right-hand side. To suppress the digital cross talks, the analog and digital blocks are enclosed in distinct deep N-well islands.

| TABLE I | TECHNOLOGICAL PARAMETERS |
|---------|--------------------------|
| Technology | Silterra 180 nm CMOS, 6 metals |
| Process options | Deep NWELL, MIM cap. (4 fF/µm²) high resistive p+ poly (1050 Ω/sq.) |
| Chip size | 6.54 mm × 7.2 mm |
| Thickness | 381 µm |
| Supply rail | 1.8 V (core/IO) |

B. Analog Processing Block

Figure 3 shows the signal processing chain of each channel. The strip sensor is AC-coupled to an input of the charge-sensitive amplifier (CSA), while test pulses can be injected via an AC-coupling capacitor of 100 fF. The incident signals are processed from the left analog block to the right digital block. Power supply is provided from the top and bottom pads only, and digital outputs are accessed on the right-hand side. To suppress the digital cross talks, the analog and digital blocks are enclosed in distinct deep N-well islands.

Figure 3 shows the signal processing chain of each channel. The strip sensor is AC-coupled to an input of the charge-sensitive amplifier (CSA), while test pulses can be injected via an AC-coupling capacitor of 100 fF. The CSA is based on a folded cascade configuration with a p-channel input transistor $(W/L = 8 \mu m/180 \mu m)$. In terms of noise performance, we increased the folding number of the input transistor to $M = 250$, which are placed in parallel. The feedback capacitor $C_f$ was implemented by a metal-insulator-metal structure with a value of 170 fF. A transfer gate type FET was employed for the CSA DC-feedback component.

The CSA output is fed into a CR-RC shaping amplifier composed of a pole-zero cancellation circuit (PZC) and a
of input charges. This method corresponds to the so-called shape becomes bipolar, which traverses the baseline given by signals. By differentiating the semi-Gaussian shape, the output threshold. By implementing the differentiator after the CR-RC below the requirement of 1 ns, even after the fine tuning of the ability to reduce the time walk of the discriminator rising edge and a single discriminator. This method, however, was not able to reduce the time walk of the discriminator rising edge from the first-order CR-RC shaper with a peaking time of 50 ns. The shaper output is amplified by an inverting amplifier and connected to a discriminator. Baseline tuning is required after the inverting amplifier, the output affect timing accuracy. After the inverting amplifier, the output is fed into two signal paths, one of which is buffered by a factor of two. This function is selectable with a CMOS technology. The chip size is 6.54 mm × 7.2 mm with a memory area density of 40%.

The shaper output is amplified by an inverting amplifier by a factor of two. This function is selectable with a CMOS switch on the outside chance that voltage slopes of the shaper output affect timing accuracy. After the inverting amplifier, the output is fed into two signal paths, one of which is buffered and connected to a discriminator. Baseline tuning is required to adjust the thresholds that is performed by two sets of 7-bit current DACs (Digital-to-Analog Converters) and resistors. The other signal path is connected to the additional CR circuit, which functions as a voltage differentiator.

In the previous chip, SliT128A, the hit timing was produced from the first-order CR-RC shaper with a peaking time of 50 ns and a single discriminator. This method, however, was not able to reduce the time walk of the discriminator rising edge below the requirement of 1 ns, even after the fine tuning of the threshold. By implementing the differentiator after the CR-RC shaper, we improved the time walks between 0.5 and 3 MIP signals. By differentiating the semi-Gaussian shape, the output shape becomes bipolar, which traverses the baseline given by \( V_{\text{base}} \) in Fig. 3. The traversing timing becomes independent of input charges. This method corresponds to the so-called “zero-cross” architecture and the traversing timing locates at a peaking time of the preceding CR-RC filter. As a result, the discriminator rising edge from the differentiator path remains less than 100 ns, and at the same time, the time walk can be considerably improved.

The noise level after the voltage differentiator becomes worse than the ENC of the CR-RC shaper, and thus, we preserved the CR-RC shaper path and used both information to define the final pulses by making an AND operation. The leading-edge timing of the final output is determined from the differentiator, while the trailing-edge timing is determined from the CR-RC shaper. The monitor lines were also implemented to examine analog waveforms at each processing point, e.g., the CSA, CR-RC shaper, differentiator etc. The 20-bit control registers are implemented to enable switches, i.e., a test pulse injection, the inverting amplifier, distinct discriminators, monitor lines, and tuning DACs for each channel.

C. Digital Processing Block

Figure 4 (a) shows the block diagram of the digital part. It consists of a signal interface (I/F), a memory controller, a serializer, a timing generator, and a parameter controller. The timing generator block provides the “Write Start” and “Read Start” signals to the memory controller, which are synchronized with an external 200 MHz clock. The parameter controller block is a slow control circuit for the registers of both the analog and digital parts. The signal interface block receives the discriminator outputs from the analog part. D-type flip-flops sample these signals by the external 200 MHz clock. After the first flip-flops, subsequent two D-type flip-flops resample these signals by 100 MHz clocks which are 180 degrees out of phase. This is because the sampling frequency of 200 MHz is close to the maximum clock frequency of logic circuits in the Silterra technology.

Figure 4 (b) shows the block diagram of the memory controller. The memory controller block receives two kinds of data, which are synchronized by different 100 MHz clocks, from the signal I/F block. When the memory-write controller block receives the “Write Start” signal, it starts to store data in SRAMs (Static Random Access Memory). The memories have 8192 word depths for each channel, and the data can be stored within 40.96 \( \mu \text{s} \) (= 8192 × 5 ns). The storing process continues until SRAMs are full. When the memory-read controller block receives the “Read Start” signal, it reads out all of the data from memories and sends them to the serializer block. The data is then sent out by the LVDS (Low Voltage Differential Signaling) drivers with a 50 MHz clock. The data are synchronized by the same 50 MHz clock in the backend electronics, e.g., an FPGA board in our applications, with the DDR (Double Data Rate) mode.

III. PERFORMANCE TESTS

A. Experimental Setup

The performance of the SliT128C was evaluated with a test pulse from a function generator. A dedicated printed circuit board (PCB) was designed for performance testing. Figure 5 shows the experimental setup. A bare die is directly

Fig. 2. Photograph of the ASIC fabricated in the Silterra 180 nm CMOS technology. The chip size is 6.54 mm × 7.2 mm with a memory area density of 40%.
Fig. 3. Signal processing chain for each channel. The capacitance values are $C_I = 170 \, \mu F$, $C_{pe} = 8 \times C_I$, $C_{sh1} = 154 \, \mu F$, $C_{sh2} = 40.5 \, \mu F$, $C_{diff1} = 54.5 \, \mu F$, $C_{diff2} = 5 \times C_{diff1}$. The resistance values are $R_{sh1} = 255 \, k \Omega$, $R_{sh2} = 85 \, k \Omega$, $R_I = 100 \, k \Omega$, $R_g = 2 \times R_I$, $R_{diff1} = 70 \, k \Omega$, $R_{diff2} = 5 \times R_{diff1}$. $R_I$ and $R_{pe}$ are within the range of several $M \Omega$ adjusted by the gate voltage $V_{GE}$. The resistance values are $R_{diff1} = 255 \, k \Omega$, $R_{diff2} = 5 \times R_{diff1}$.

Fig. 4. Block diagrams of (a) the digital part and (b) the memory controller.

Fig. 5. Setup for tests of SliT128C performance. A bare die is mounted on the dedicated PCB (right side), which is connected with a commercial FPGA board of the Nexys Video (left side) via an FMC connector.

B. Analog Waveform and Dynamic Range

The response of the monitor outputs was investigated to evaluate the analog waveform and dynamic range. Figure 6 shows typical analog output signals, when a test pulse with 1 MIP charge was injected. The outputs of discriminators are overlaid in black. All monitor lines are functioning as designed. The peaking time and pulse width were 64.2 ns and 99.2 ns, respectively. Comparing with the values from a SPICE simulation (35.1 ns and 75 ns) as shown in Table I, we observed larger values due to a finite output-buffer performance to drive a large capacitive load of the bonding wire, ~5 cm microstrips on the PCB, and the probe capacitance of ~3.9 pF. The actual pulse width at the discriminator must be shorter than the monitor values, and can be estimated only from the discriminator pulse width described in the following section.

Figure 7 shows a pulse height of the CR-RC output as a function of injected charges. The wide dynamic range is needed to avoid the saturation for high hit-rate environment.
The integrated non-linearity was measured as less than 1% and 3.8% in the ranges from 1.92 fC to 20 fC and from 1.92 fC to 30 fC, respectively. The integrated non-linearity of 5% is sufficient for our application. The corresponding dynamic range is larger than 7.8 MIP. We also confirmed that the channel-to-channel variation of offset voltages is within the amplitude of a 1.5 MIP charge that is reasonable to be compensated by 7-bit DACs.

C. S-curve scan and Equivalent Noise Charge

The noise performance was evaluated by scanning the threshold with different injected charges (s-curve scan). First, we enabled only the discriminator in the CR-RC filter, and performed the threshold scans. Figure 8 shows a counting efficiency as a function of the threshold DAC, a so-called s-curve for a typical channel. The counting efficiency was calculated from the digital outputs. By fitting a complementary error function, i.e., integrated Gaussian function, to the data, we obtained the center value and the standard deviation of the Gaussian function. The center value corresponds to the pulse height. The standard deviation indicates the noise level. One least significant bit (LSB) step size of the threshold DAC for the CR-RC shaper is equivalent to the input charge of 0.043 fC. We repeated this measurement for 32 readout channels, and plotted the ENC distribution as shown in Figure 9. The average equivalent noise charge is measured to be 1547 ± 75 electrons at $C_{\text{det}} = 33$ pF, where the uncertainty indicates the channel-to-channel variation. If we assume the simulated ENC dependence on the detector capacitance (31 electrons/pF), we obtain the ENC to be 1454 electrons at $C_{\text{det}} = 30$ pF, which satisfies the requirement for the noise performance. The simulated ENC is 1210 electrons at $C_{\text{det}} = 30$ pF. The ENC difference between the measurement and simulation can arise due to various factors: parasitic input capacitance, digital crosstalk, and noise injection from the power supplies.

D. Time walk

Based on the above results, we set the threshold voltage of the CR-RC shaper to match 1.53 fC which corresponds to the 0.3 MIP charge level in each channel. Then the threshold voltage for the voltage differentiator was adjusted to minimize the time walk. Figure 10 shows the hit timing vs. threshold voltages of the voltage differentiator in a typical readout channel. The hit timing is defined as the leading-edge timing of the final output, which is determined by the differentiator. A plateau appeared in the hit timing by giving a proper threshold voltage to the differentiator. The time walk of our application is defined as a maximum timing variation in the range from 0.5 MIP to 3.0 MIP. Figure 11 shows the time-walk distribution for the 32 readout channels. This result satisfies the requirement for the time walk and the mean value of the
Entries 32
Mean 1547
Std Dev 74.93

Fig. 9. ENC distribution for 32 readout channels.

time walk was $0.38 \pm 0.16$ ns, where the uncertainty indicates the channel-to-channel variation. We note that the hit timing over the injected charges of 3 MIP is increasing, however, we confirmed the plateau can be expanded up to 5 MIP by further tuning the bias of the shaping amplifiers.

E. Time over Threshold and Timing Jitter

The time-over threshold (ToT) as a function of injected charges is shown in Figure 12 (top). The reconstruction quality of the positron tracks can be improved by filtering events based on the ToT information. As described in section II, the leading edge of the hit signal is determined either from the voltage differentiator or the single CR-RC shaper by the register setting. We compared the performance at the normal operating conditions, i.e., using outputs from both CR-RC and voltage differentiator in discriminators, in the case that the CR-RC path only is used to get the ToT values. Both cases are labeled as CRRC&DIFF (red) and CRRC (blue) in the figure. Averaged ToT of 32 channels at 1 MIP were determined as $34.1 \pm 0.6$ ns (CRRC&DIFF) and $74.5 \pm 1.6$ ns (CRRC).

We note that the ToT value at 1 MIP of the CRRC case (74.5 ns) can be compared with the simulation value of the pulse width (75 ns) as shown in Table II. The measurement results are close to the designed performance. The ToT of the CRRC&DIFF becomes flat above 15 fC. Non-saturation region can be expanded up to 20 fC by tuning the bias of the shaping amplifiers.

Figure 12 (bottom) shows the timing jitter ($\sigma$) as a function of the injected charge. The timing jitter becomes worse for smaller signals, since the leading edge of the hit signal is directly affected by the electrical noise. The average timing jitter at 1 MIP for 32 channels was $2.9 \pm 0.1$ ns for the CRRC&DIFF case and $2.5 \pm 0.1$ ns for the CRRC case. The jitters at 0.5 MIP was $4.8 \pm 0.2$ ns for the CRRC & DIFF, and $4.5 \pm 0.2$ ns for the CRRC. They are comparable with the sampling interval of 5 ns.

F. Power Consumption

We supplied 1.8 V for an analog circuit and 1.8 V for a digital one. An additional dedicated bias voltage of 1.1 V is applied to the input transistors in the CSA for noise optimization and avoiding IR-drops. By measuring the current at each power line, power consumption was determined to be 0.13 W, 0.11 W, and 0.06 W for the analog, the digital, and the CSA, respectively. The total power consumption was 0.30 W per chip.

IV. Conclusions

We have developed a series of the silicon-strip readout chips named SliT with the 180 nm CMOS technology. The SliT is designed for the precise measurement of the muon $g-2$/EDM, which is planned at J-PARC in Japan. The main objective of the SliT is to provide the timing information for positron tracks from silicon-strip sensors, with amplitude-independent
TABLE II
SUMMARY OF THE SliT128C PERFORMANCE

| Requirement                      | Simulation       | Measurement      |
|----------------------------------|------------------|------------------|
| Peaking time                     | < 75 ns          | 35.1 ns          | 74.5 ns          |
| Pulse width at 1 MIP             | < 100 ns         | 75.0 ns          | 74.5 ns          |
| Dynamic range                    | > 4 MIP          | 8 MIP            | > 7.8 MIP        |
| ENC                              | < 1, 600 e⁻@Cdet = 30 pF | 1210 e⁻@Cdet = 30 pF | 1547 ± 75 e⁻@Cdet = 33 pF |
| Time-walk (0.5-3.0 MIP)          | < 1 ns           | 0.4 ns           | 0.38 ± 0.16 ns   |
| Jitter at 0.5 MIP                | < 5 ns           | 4.89 ns          | 4.9 ns           |
| Power consumption                | 0.64 W/chip      | N.A.             | 0.30 W/chip      |

* Outputs measured from the monitor which include delays due to the parasitic capacitance and finite buffer drive strength.

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Fig. 12. Time-over threshold (top panel) and timing jitter (bottom panel) as a function of the injected charge for the 32 readout channels. The result with normal operation, in which both comparators for the CR-RC shaper and the differentiator are enabled, is shown by solid red circles. The result with operation, in which a comparator is enabled for the CR-RC shaper only, is shown by open blue circles. The threshold voltage of the CR-RC shaper was set to be at the 0.3 MIP charge level. The threshold voltage of the differentiator was adjusted to minimize the time walk. The error bars indicate the channel variation.

time walks. We have also developed a new readout chip named “SliT128C”. In this chip, the leading edge is generated from the timing of baseline-crossing by the bipolar waveforms. This zero-cross architecture is implemented by adding the voltage differentiator at the output of the CR-RC shaper. As a result, the time-walk effect is suppressed to subnanosecond (0.38 ± 0.16 ns). The equivalent noise charge is 1547 ± 75 e⁻ with $C_{\text{det}} = 33$ pF. The SliT128C consists of 128 channels, which are completely functional. Other evaluated performance results are also summarized in Table II The SliT128C satisfies all requirements of the J-PARC muon $g - 2$/EDM experiment.