Apparent high mobility ~30 cm²/Vs of amorphous In–Ga–Zn–O thin-film transistor and its origin

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Amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) annealed in ozone at 250°C exhibited a good subthreshold swing (S) of 123 mV/decade and a saturation mobility (μsat) of ~10 cm²/Vs, but a bit large threshold voltage (Vth) of 11.6 V. Further oxygen annealing at 200°C resulted in high apparent μsat of ~30 cm²/Vs and deteriorated characteristics such as a large S value and large hysteresis. The high apparent μsat values were attributed to the electrical discharge between the gate and source electrodes. Reasonably actual μsat values ~10 cm²/Vs were obtained using the actual capacitance calculated from the discharge characteristics.

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1. Introduction

Amorphous oxide semiconductor (AOS) possesses many advantages such as large electron mobilities for amorphous semiconductor >10 cm²/Vs, high transparency in the visible region, low-temperature process compatibility down to room temperature (RT), and good uniformity over large area. Therefore, it is expected for a channel material of a thin-film transistor (TFT) in next-generation flat-panel displays such as electronic papers, organic light-emitting-diode displays, liquid-crystal displays (LCD), flexible displays, and transparent displays. Among the AOS materials, amorphous In–Ga–Zn–O (a-IGZO) is the most widely-investigated AOS and most close to a wide commercialization; indeed, a-IGZO TFT is commercialized in a retina display of new iPad in March, 2012. A-IGZO TFT is expected also for green technology because a-IGZO TFT may be fabricated at low temperatures including RT, operates at a very low voltage 1.5 V, exhibits a low off current, and contributes to better aperture ratio of LCD, lower power consumption, and non-volatile memory devices.

Post-deposition annealing at e.g. ≥300°C is an effective way to improve the a-IGZO TFT performance and stability. On the other hand, a low temperature process e.g. at ≤200°C is required for future applications such as those employing plastic substrates. However, we found that such low-temperature annealing in air/O₂ causes serious negative threshold voltage (Vth) shift and does not work well. Recently, we reported that the ozone annealing is more effective than O₂ annealing to improve the TFT operation characteristics at ≤200°C; while TFTs annealed in O₂ at a high temperature e.g. 300°C exhibited a significant deterioration and bistable behavior. On the other hand, Hall mobilities (μhall) and field-effect mobilities (μFE) of a-IGZO TFTs with the chemical composition of In:Ga:Zn~1:1:1 in atomic ratio are reported to be 10–15 cm²/Vs, but some reports have provided much larger mobilities. Based on the device physics, μFE should be smaller than drift mobility (~μhall) because μFE include the deterioration effects by electron traps in the band gap and carrier scattering at the channel–gate insulator interfaces; actually, we have confirmed that μFE of our a-IGZO TFTs are close to or a little bit smaller than μhall.

In this work, we investigated the effects of an O₂ and ozone- (O₃-) annealing combined process on characteristics of a-IGZO TFTs, and observed a high saturation mobility (μsat) of ~30 cm²/Vs. However, these TFTs showed large charging/discharging currents in the gate-to-source current (Igs). It was found that extra gate-to-source capacitance (Cgs) is formed under the combined annealing conditions, which caused overestimation of the apparent μFE values. The μFE values corrected by the actual Cgs provided reasonable μFE values around 10 cm²/Vs.

2. Experimental

Bottom-gate top-contact a-IGZO TFTs (as shown in the inset of Fig. 1) were fabricated by the following process. A heavily-doped single-crystal n⁺-Si wafer was used as the substrate and the gate electrode. A 150-nm-thick SiO₂ grown by thermal oxidation was used as the gate insulator. A-IGZO channels (40 nm in thickness) were deposited by radio-frequency (RF) magnetron sputtering at an optimized condition of RF power of 70 W, total pressure of 0.55 Pa, a gas flow rate ratio of Ar/O₂ = 19.4:0.6 in standard cc per minute, and RT. Then the n⁺-Si/SiO₂/a-IGZO samples were annealed in O₂ at 250°C for 1 h. The O₂ molecules were generated by a silent discharging ozonizer with a pure O₂ gas, and the O₂ concentration was measured to be 3.74 g/m³. Some n⁺-Si/SiO₂/a-IGZO samples were further annealed in O₂ at 200°C for different durations (additional O₂ annealing). Finally, Ti/Au bilayers were deposited by electron-beam evaporation in this order and used as the source and drain.

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electrodes. The a-IGZO and Ti/Au layers were patterned by photolithography and lift-off processes. The channel width (W) and length (L) were 300 and 50 μm, respectively.

3. Results

Figure 1 shows the transfer curves (I_DS−V_GS characteristics) of (the black line) the a-IGZO TFTs annealed solely in O3 at 250°C for 1 h and (the other lines) those additionally annealed in O2 at 200°C for 2–8 h. The TFT parameters extracted from the transfer curves are summarized in Fig. 2. The TFT solely annealed in O3 (corresponding to the O2-annealing time of 0 h) exhibited a good subthreshold swing (S = dV_GS/d log10 I_DS, where I_DS denotes the drain-to-source current) of 123 mV/decade and μ_sat of ~10 cm²/Vs, but a bit large V_th of 11.6 V (determined as the V_GS-axis cross-section of I_DS^1/2−V_GS plots as will be explained later on). For the TFTs additionally annealed in O2, the transfer curves exhibited much smaller turn-on voltages (V_on, defined as V_GS where I_DS = 0.5 pA) but they show strange shapes with clear inflexion points around I_DS = 10−11−10¹10 A. Then, the I_DS increased with a small and nearly constant S slope in the subthreshold region (i.e., V_GS ≪ V_th) and consequently exhibited a very large S of ~1700 mV/decade. The V_th decreased slightly from 11.6 to 9.8 V as the additional O2 annealing time further increased from 2 to 8 h. The μ_sat were much improved to 29.8 cm²/Vs after the further O2 annealing for 8 h. However, we should note that these μ_sat values were far larger than the μ_Hall values of corresponding a-IGZO films (10−15 cm²/Vs), and the μ_sat values should be overestimated.

Figure 3 shows the hysteresis curves in the transfer characteristics of the a-IGZO TFTs additionally annealed in O2 for 8 h, swept for 3 cycles of V_GS between ~20 to 20 V. These transfer curves exhibited very large hysteresis loops, indicating that the TFT characteristics were deteriorated by formation of electron traps by the additional oxygen annealing; i.e., the electrons induced by the large positive V_GS are captured by traps, the charged traps are energetically relaxed to an energy deeper than the Fermi level, and the V_on is increased in the backward V_GS sweep measurements. A similar behavior is observed by 300°C O3 annealing, but that is different from the present case because the high-V_th state was stable at least for 12 h in that case; on the other hand, the high-V_on state is quickly recovered to the initial small-V_on state and the same forward-sweep characteristics are observed also in the 2nd and 3rd cycle measurements. That is, the clock-wise hysteresis suggests that the a-IGZO channel layer contains electron traps with a fast recovery time.

4. Discussion

Here, we should consider whether the large μ_sat values obtained from the transfer curves in the saturation regime are real values or not. As shown in Fig. 4, we observed a large negative gate-to-source current (I_GS) occurred in the large positive V_GS region where the large μ_sat values were estimated (the hatched
area in Fig. 4); while no such $I_{GS}$ was observed for any other cases with reasonable $\mu_{sat}$ values.

Based on the standard device physics and analysis procedure,[14] we estimate $\mu_{sat}$ from a transfer characteristic using the following relation:

$$I_{GS} = \frac{\mu_{sat} W C_G^0}{2L} (V_{GS} - V_{th})$$  \hspace{1cm} (1)

where $C_G^0$ is the gate insulator capacitance per unit area. For the present case (150 nm-thick a-SiO$_2$), $C_G^0$ was calculated to be $2.3 \times 10^{-4}$ F/m$^2$ using the static relative dielectric constant of a-SiO$_2$, 3.9. However, we observed the discharge current in $I_{GS}$ (Fig. 4), which indicates the existence of extra gate capacitance and its contribution should be considered. Then, the actual capacitance $C_G^{act}$ is estimated by the following equation:

$$C_G^{act} = \frac{Q}{WL(V_{GS,peak} - V_{th})}$$  \hspace{1cm} (2)

where $Q$ is the total charge of the discharge current calculated by integrating $I_{GS}$ with respect to the measuring time, and $V_{GS,peak}$ is the $V_{GS}$ where $I_{sat}$ takes the maximum as shown in Fig. 4. The calculated $C_G^{act}$ values, as shown in Table 1, were 2.0–3.3 times as large as $C_G^0$. As a result, the above-obtained $\mu_{sat}$ values were overestimated by a factor of $C_G^{act}/C_G^0$ and should be ‘apparent’ values ($\mu_{sat}^{app}$). The actual $\mu_{sat}$ values ($\mu_{sat}^{act}$) were calculated to be 8.9–12.2 cm$^2$/Vs which are reasonable values for a-IGZO TFTs.

There would be several plausible origins of the extra gate capacitance; e.g., (i) the gate insulator thickness became thinner than expected, (ii) charge traps in the gate insulator, (iii) charge traps at the gate insulator-channel interface, (iv) charge traps in the a-IGZO layer, and (v) extra capacitance originating from the wider area of the a-IGZO layer than the channel area. We consider that the possibilities (i) and (ii) are not likely because we employed the thermally-oxidized a-SiO$_2$ on a Si wafer, and the additional thermal annealing at 200°C would not change its thickness and quality. The possibilities (iii) and (iv) are difficult to distinguish. As discussed in the previous section for Fig. 3, we observed a large clockwise hysteresis, which is consistent with the existence of electron traps in the a-IGZO channel. Further, we detected similar bistable electron traps in 300°C O$_3$ annealed a-IGZO TFTs11 (note that the exact origin should be different from the present case because of the different recovery-time constants as discussed at the end of the previous section). Therefore, we cannot exclude this possibility. On the other hand, however, this model cannot explain the larger actual capacitance because the gate capacitance is limited by the geometrical capacitance of the a-SiO$_2$ gate insulator if we consider neither its thinning nor quality alternation [i.e., the possibilities (i) nor (ii)]. The possibility (v) comes from the present TFT structure that the a-IGZO channel layer is much larger than the gate insulator area; i.e., the charges induced by $V_{GS}$ inside the channel region diffuse to the extra a-IGZO area outside the channel region, and the extra area also contributes to $I_{GS}$. On the other hand, the aspect ratio of the channel is as small as $L/W = 50/300$ and appears to be difficult to produce the extra capacitance 2.0–3.3 times as large as $C_G^0$. At present, we consider that the combination of the last two would be most plausible, but further study is required to determine the real origin.

5. Conclusions

We have investigated the effect of additional oxygen annealing at 200°C after O$_3$ annealing at 250°C on the characteristics of a-IGZO TFTs. The additionally annealed TFTs exhibited deteriorated characteristics such as large $S$ values and serious hystereses. These TFTs exhibited apparent high $\mu_{sat}$ of $\sim 30$ cm$^2$/Vs which resulted from the extra gate capacitance. This was verified by the result that all the $\mu_{sat}^{act}$ values corrected by the $C_G^{act}$ fell in the reasonable values around 10 cm$^2$/Vs.

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