Novel Multiple-Valued Logic Design Using BiCMOS-Based Negative Differential Resistance Circuit Biased by Two Current Sources

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SUMMARY The paper demonstrates a novel multiple-valued logic (MVL) design using a three-peak negative differential resistance (NDR) circuit, which is made of several Si-based metal-oxide-semiconductor field-effect-transistor (MOS) and SiGe-based heterojunction bipolar transistor (HBT) devices. Specifically, this three-peak NDR circuit is biased by two switch-controlled current sources. Compared to the traditional MOS-HBT-NDR circuit made of resonant tunneling diode (RTD), this multiple-peak MOS-HBT-NDR circuit has two major advantages. One is that the fabrication of this circuit can be fully implemented by the standard BiCMOS process without the need for molecular-beam epitaxy system. Another is that we can obtain more logic states than the RTD-based MVL design. In measuring, we can obtain eight logic states at the output according to a sequent control of two current sources on and off in order. 

key words: multiple-valued logic, negative differential resistance, BiCMOS process

1. Introduction

The negative differential resistance (NDR) devices have attracted a great deal of interest in many analog and digital circuits owing to their unique folded current-voltage (I-V) characteristic [1], [2]. In particular, the multiple-peak NDR circuits provide the convenience to implement the multiple-valued logic (MVL) circuit [3]–[5]. Compared to traditional binary logic, the MVL can transfer more information with fewer interconnects between devices and circuits. The MVL provides lots of simplifying opportunities for implementation of sophisticated algorithms in computational process than traditional binary logic. It can offer more compact solutions for these problems and better functional capabilities in information process [2]. The advantage of MVL using multiple-peak NDR circuit is that we can design the applications with decreased interconnect complexity and reduced device numbers as compared to the conventional CMOS technologies [6].

The popular device applied to the NDR-based circuits is the resonant tunneling diode (RTD). The RTD basically consists of one or multiple quantum wells and can be fabricated using an advanced epitaxy growth technique such as molecular-beam epitaxy (MBE), which is not easily to be compatible with mainstream ULSI technology such as CMOS or BiCMOS process. However, some scholars have presented the Si/SiGe-based resonant interband tunneling diodes (RITD), which have shown great potential for integrating with CMOS technology [7], [8]. But they still require the MBE system to accomplish the whole application. This will limit the development and application of RTD circuits. Therefore, if the NDR-based applications can be completely fabricated by the standard CMOS or BiCMOS process, it can provide some useful and attractive ideas for circuit designers.

Recently, our research group has demonstrated two novel NDR circuits composed of Si-based metal-oxide-semiconductor field-effect-transistor (MOS) and SiGe-based heterojunction bipolar transistor (HBT) devices, which are named as MOS-NDR and MOS-HBT-NDR circuits. We have successfully demonstrated their possible application in the multiple-valued memory circuit [9], logic circuit [10], and multiplexer [11]. The fabrication of such NDR-based applications could be implemented by the standard CMOS and BiCMOS techniques.

This paper focuses on demonstrating a novel MVL design using a three-peak BiCMOS-based NDR circuit. Compared to the traditional RTD-based MVL design, one can obtain only four logic states using a load device to bias the three-peak NDR circuit. However in this work, we utilize two switch-controlled current sources to bias the three-peak NDR circuit at different current levels. By controlling the switches on and off alternatively, we can obtain a total of eight logic states at the output. This MVL circuit is implemented by the standard 0.35 µm SiGe BiCMOS process provided by the Taiwan Semiconductor Manufacturing Company (TSMC) foundry.

2. Multiple-Valued Logic Design

Most of the NDR-based MVL circuits utilize the RTD as the basic device. As it is known, the RTD is made of compound semiconductors, so the fabrication process is complicated and the cost is expensive compared to the standard CMOS or BiCMOS process. Besides, the RTD is difficult to combine with other devices and circuits to achieve the system-on-a-chip (SoC).

Figure 1 shows the concept figure of load-line analysis for the three-peak NDR I-V characteristics. The obvious
method to bias this three-peak NDR circuit into the multiple stable states is utilizing a resistor or a constant current source to serve as a load device. The constant current source can be designed with a current mirror structure. When two electrical components are connected vertically, the upper component can be treated as a load to the pull-down driver. We regard the three-peak NDR circuit as the driver here. The load lines, which are represented by the dashed lines, are the I-V characteristics of load device. The I-V characteristics of the driver device are shown by the solid lines. The intersection point between two lines under a bias is the stable operating point. As shown, the load line will intersect the positive differential resistance (PDR) regions with four operation points from Q1 to Q4 consecutively. Therefore, we can obtain four logic states in this MVL circuit.

The advantage of using a resistor as a load is a direct and easy design. The voltage to be stored is provided by enabling the $V_S$ as a pulse signal [4]. We require a positive triggering pulse to transfer the logic state from the first initial operating point to the second stable operating point. After that we input another higher triggering pulse to transfer the logic state from the second operating point to the third operating point, and so on. But these higher triggering pulses may exceed the limit of voltage tolerance of the devices. Therefore, this MVL circuit will have the problem of burning down or wasting too much power dissipation in transferring the logic states.

Another method is using a constant current source as the load to bias the three-peak I-V characteristics. This kind of MVL circuit possesses a better noise margin because the load current could be adjusted to a value approximately halfway between the peak and valley currents of the three-peak NDR circuit. However, this MVL circuit requires an extra read/write circuit with a pulse control gate and a saw-tooth wave at the input terminal to obtain the multiple states at the output [5]. But the applied voltage could be controlled under a safe and suitable condition.

However in this paper, we created a novel MVL design using two switch-controlled constant current sources to bias the three-peak NDR circuit with different current levels, as shown in Fig. 2. For the traditional RTD-based MVL circuit, one can also obtain the combined multiple-peak I-V characteristics by connecting two or more devices in series. However, the three-peak NDR circuit here is made of two Λ-type and one N-type MOS-HBT-NDR circuits connected in parallel. Details of the operation principle of this MOS-HBT-NDR circuit had been discussed in Ref. [11].

This NDR circuit also can be implemented by the CMOS-based Λ-type NDR device [12], but our BiCMOS process possesses many advantages over the CMOS technique, such as higher switching speed, better noise performance, and better high frequency characteristics. Besides, the BiCMOS follows almost the same scaling curve as the CMOS technology resulting in explosive growth in BiCMOS product growth in the future.

The I-V characteristics of the NDR1 and NDR2 circuits are Λ types, and that of the NDR3 circuit is N type. The combined current of this parallel-connected NDR circuit will be the sum of currents passing through the NDR1, NDR2, and NDR3 circuits. Devices MNS1, and MNS2 along with MNS3 are used to shift the turn-on voltages of NDR2 and NDR3, respectively. Therefore, we can obtain three peaks and valleys in the combined I-V curve. The gate widths of the MOS devices are designed as $W_{MNS1}(W_{MNS2}, W_{MNS3}) = 3 \mu m$, $W_{MNS1}(W_{MNS2}, W_{MNS3}) = 50 \mu m$, $W_{MNS3} = 5 \mu m$, and $W_{MNS1}(W_{MNS2}, W_{MNS3}) = 100 \mu m$. The gate lengths of all MOS devices are fixed at 0.35 μm. The HBT uses the $lt_{02}$ cell provided by the TSMC foundry.

For the Λ-type NDR1 circuit, the magnitude of $V_{gg}$ value should be higher than the sum of threshold voltage of the MN11 and turn-on voltage of the HBT1.
The $V_{GS}$ voltage of the MN11 device is affected by this $V_{gg}$ value. If the $V_{gg}$ voltage is increased, the equivalent resistance of MN11 will be decreased. Therefore, the $V_{DS}$ voltage of the MN12 device will be increased. Then the drain current of HBT1 will be increased. Finally, we can obtain higher peak current by increasing the $V_{gg}$ value.

The MN11 is connected like a diode and always turns on during the circuit operation. The MN12 is operated as a variable resistor by increasing the $V_{S}$ gradually. The MN11 and MN12 are constructed a voltage divider, where the magnitude of the voltage affects the operation situation of HBT1. As for the operation of the N-type NDR3 circuit, the operations of MN31, MN32, and HBT3 are the same as the A-type NDR circuit. But, the gate width of the MN33 will affect the magnitude of second PDR segment.

This NDR circuit is connected in parallel, so each peak current of this three-peak NDR circuit can be independently adjusted by the corresponding $V_{gg}$ voltage, from $V_{gg1}$ to $V_{gg3}$, respectively. Because the $V_{gg}$ is located at the third external voltage terminal, yet the peak current can be modulated even though the IC has been tape-out. This special characteristic makes the MOS-HBT-NDR circuit interesting and attractive for circuit application. When the $V_{S}$ voltage is set at zero, the initial operating state for the HBT device is saturated. We can realize that there exists a reverse current back to the $V_{S}$ terminal. When we further increase the voltage, this reverse current will reach to zero first and then become a positive current gradually. Therefore, the cut-in voltage with respect to the zero current will not be located at zero voltage. The magnitude of the cut-in voltage is mainly determined by the parameters of the HBT device.

Two gates C1 and C2 are used to control the path of the current sources I1 and I2, respectively, which can bias the three-peak MOS-HBT-NDR circuit with suitable operating points. For convenience, two current values are designed the same way. The peak-to-valley ratio (PVCR) is one of the figure-of-merits used to evaluate the $I$-$V$ performance of a NDR circuit. For the MVL circuit, the optimization of the PVCR of each peak should be higher than 10. Because the three-peak NDR circuits are biased by two constant current sources, the three peak currents should meet the condition as $I_{P1} < I_{P2} < I_{P3}$. Therefore, the three control voltages are designed as $V_{gg1} < V_{gg2} < V_{gg3}$.

Figure 3 shows the load-line analysis of this MVL circuit. The parameters for three $V_{gg}$ values are designed as $V_{gg1} = 1.65$ V, $V_{gg2} = 1.75$ V, and $V_{gg3} = 1.85$ V. The magnitudes of three peak current are about $I_{P1} = 0.6$ mA, $I_{P2} = 0.9$ mA, and $I_{P3} = 1.15$ mA. The magnitudes of three valley current are about $I_{V1} = 0.035$ mA, $I_{V2} = 0.07$ mA, and $I_{V3} = 0.07$ mA. Therefore, the PVCRs for three peaks are 17.1, 12.9, and 16.4, respectively. These values are higher than those shown in Ref. [3]–[5].

For the current I1, it can intersect the PDR segments of the three-peak $I$-$V$ curve with four stable operating points from Q1 to Q4. The combined currents of I1 and I2 can intersect the combined $I$-$V$ curve with three stable operating points from Q5 to Q7. Because the cut-in voltage of this three-peak NDR circuit is not located at zero voltage, we can obtain eight operating points from Q0 to Q7. Therefore, we can obtain MVL states at the output by controlling the two switches on and off alternatively.

3. Results and Discussion

This MVL circuit is implemented by the standard 0.35 µm SiGe BiCMOS process provided by the TSMC foundry. The area is about $92 \times 125$ µm$^2$. A saw-tooth wave is applied to the input with amplitude of 3.3 V. Its period is about 60 µS. The voltage to be stored is provided by Vin signal and loaded to the main circuit by enabling the write clock in order. We use a square wave as the write clock that can turn the MN1-MOS on and off, alternately. When the write clock is operated from on to off state, the voltage across the three-peak NDR circuit will be set to the nearest stable operating point. Therefore, the corresponding voltage level will be transferred to the output terminal in sequence. Figure 4 shows the waveforms of Vin signal, write clock, and on and off sequences of C1 and C2 gates, which is extracted from the oscilloscope. Two control gates are constructed by PMOS devices. The control gate state “0” means the load current can pass through the NDR circuit.

Figure 5 shows the measured results Vout of this MVL circuit. The output gives clearly eight logic states from V0 to V7. The V0 to V7 levels are the corresponding voltage values with respect to the operating points from Q0 to Q7, respectively. When both C1 and C2 logic states occur at high level, there exists only one state V0, which is the cut-in voltage of the three-peak MOS-HBT-NDR circuit. When C1 gate is low and C2 gate is high, there should be four voltage levels from V1 to V4. When both C1 and C2 gates are low, there will be three voltage levels from V5 to V7. These values are $V0 = 0.05$ V, $V1 = 0.25$ V, $V2 = 0.85$ V, $V3 = 1.55$ V, $V4 = 2.45$ V, $V5 = 1.05$ V, $V6 = 1.8$ V, and
we want to obtain three stable states without overlapping the V5 states, we should input three clock pulses at this region.

The noise margin of each state was defined as the minimum value of the current difference between the operating point and peak (or valley). Referring to Fig. 3, the noise margin for states V1, V2, V3, V4, V5, V6, and V7 are estimated to be 0.2, 0.36, 0.315, 0.21, 0.12, 0.45, and 0.33 mA, respectively. The smallest noise margin occurs at Q5 point. Therefore, the noise margin of this circuit is equal to 0.12 mA. This noise margin can be improved by inputting a higher \( V_{pe2} \) value. For example, if we set the \( V_{pe2} \) value as 1.85 V, the \( I_P \) value will be increased from 0.9 to 1.15 mA. The noise margin for V5 state will be increased from 0.12 to 0.37 mA. Then the noise margin of this circuit will be 0.2 mA for V1 state at this moment. However, this method will consume more power. But, the easy modulation of each peak current through the external voltage terminal makes the MOS-HBT-NDR circuit interesting and attractive for circuit applications.

### 4. Conclusions

Compared to the traditional three-peak RTD-based MVL circuit, one can at most obtain four logic stable states using one current source as the load. However, we propose this novel three-peak MOS-HBT-NDR-based MVL circuit using two switch-controlled current sources as the load. We can obtain eight stable states for a complete circle of switch. Because this MOS-HBT-NDR circuit is made of the combination of MOS and HBT devices, we can fabricate this NDR-based MVL application using the standard SiGe-based BiCMOS technique.

This NDR circuit can provide a substantial improvement in the integration with standard Si-based MOS devices and fabrication process. It also means that the design is easier and the fabrication cost is cheaper than those of the RTD circuit. In order to achieve higher speed and frequency characteristics, we can use further scaled-down BiCMOS process or nanostructure of MOS and HBT devices in the future.

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