A 2.5 Gbps, 10-Lane, Low-Power, LVDS Transceiver in 28 nm CMOS Technology

Xu Bai 1,2,*, Jianzhong Zhao 1, Shi Zuo 1,2 and Yumei Zhou 1,2

1 Smart Sensing R&D Centre, Institute of Microelectronics of Chinese Academy of Science, Beijing 100029, China; zhaojianzhong@ime.ac.cn (J.Z.); zuoshi@ime.ac.cn (S.Z.); ymzhou@ime.ac.cn (Y.Z.)
2 Institute of Microelectronics, University of Chinese Academy of Sciences, 19A Yuquan Rd., Shijingshan District, Beijing 100049, China
* Correspondence: baixu@ime.ac.cn; Tel.: +86-152-2230-6300

Received: 16 January 2019; Accepted: 16 March 2019; Published: 22 March 2019

Abstract: This paper presents a 2.5 Gbps 10-lane low-power low voltage differential signaling (LVDS) transceiver for a high-speed serial interface. In the transmitter, a complementary MOS H-bridge output driver with a common mode feedback (CMFB) circuit was used to achieve a stipulated common mode voltage over process, voltage and temperature (PVT) variations. The receiver was composed of a pre-stage common mode voltage shifter and a rail-to-rail comparator. The common mode voltage shifter with an error amplifier shifted the common mode voltage of the input signal to the required range, thereby the following rail-to-rail comparator obtained the maximum transconductance to recover the signal. The chip was fabricated using SMIC 28 nm CMOS technology, and had an area of 1.46 mm². The measured results showed that the output swing of the transmitter was around 350 mV, with a root-mean-square (RMS) jitter of 3.65 ps@2.5 Gbps, and the power consumption of each lane was 16.51 mW under a 1.8 V power supply.

Keywords: LVDS; high-speed serial interface; transmitter; receiver; low-power

1. Introduction

While scaled CMOS technology continues to enhance on-chip operating speeds, the power dissipation also increases at the same time. This means that reducing power consumption is critical for battery-powered systems to extend battery life. Low voltage differential signaling (LVDS), as one of the data transmission standards, is now pervasive in communication networks and is used extensively in applications such as laptop computers [1], office imaging [2,3], and medical [4] and automotive [5,6] applications. It features a low-voltage swing (250–400 mV) and achieves a high data rate (up to several gigahertz per single pair) with less power dissipation. A typical LVDS serial link [7,8] point-to-point communication is shown in Figure 1, and involves a single transmitter (TX) and receiver (RX) pair. A current source (Is) is derived from the TX, and the output amplitude is formed by the current source flowing through the terminated resistor (R_T) to establish voltage in the input of RX. By changing the current direction, the same amplitude with the opposite polarity is created to generate the logic of zeros and ones. The simple termination, low-power, and low-noise characteristics have gradually made LVDS the technology of choice for gigabit-per-second serial transmission. In addition, the wide common mode input of LVDS makes its devices easily interoperable with other differential signaling technologies [9–11].
The paper is organized as follows: Section 2 describes the architecture of the proposed LVDS transceiver, and presents some related simulation results. In Section 3, the measurement results are discussed. Finally, a summary and the conclusions are outlined in Section 4.

2. Architecture Design

In general, the architecture of LVDS drivers is divided into fully-differential NMOS-only style [12], fully-differential PMOS-only style [13] and complementary MOS style [14–16]. As shown in Figure 2, all configurations consist of four MOS switches arranged in an H-bridge structure. The NMOS-only style LVDS driver, shown in Figure 2a, works well if the supply voltage (VDD) is 2.5 V or greater [17]. However, when the supply voltage is scaled down (1.8 V for 28 nm CMOS technology), it is not applicable, as there is not enough voltage headroom. According to the LVDS standard specifications [18], a 1.125–1.325 V common mode voltage range and 250–400 mV output swing of the output signals is required, which would cause the transistors (M1a and M2a) to cut off. To overcome the supply voltage headroom issues, PMOS-only (shown in Figure 2b) and complementary MOS (shown in Figure 2c) LVDS drivers need to be addressed. A benefit of PMOS-only style drivers is that they can work without the body effect. However, the inherent speed limitation in PMOS devices precludes their use in high speed data communication. To achieve the same speed as CMOS style drivers, the size of the transistors must be increased. Consequently, the area cost and power consumption will also increase. Comparing the above-mentioned LVDS drivers, the complementary MOS style driver is the optimum choice for LVDS transmission systems operating under low supply voltage, as it is not only compatible with the LVDS standard, but also faster than the other options.

In this paper, a 2.5 Gbps 10-lane low-power LVDS transceiver is presented. The transceiver can operate at a data rate up to 2.5 Gbps, and is fully compatible with ANSI/TIA/EIA-644-A standards. The paper is organized as follows: Section 2 describes the architecture of the proposed LVDS transceiver, and presents some related simulation results. In Section 3, the measurement results are discussed. Finally, a summary and the conclusions are outlined in Section 4.

Figure 2. Simplistic circuit of LVDS output driver: (a) NMOS-only style; (b) PMOS-only style; (c) Complementary MOS style.
CMOS H-bridge output driver with a common mode feedback (CMFB) circuit, a high-speed level shifter (LS) and pre-emphasis (PE) driver. In addition, two bandgap references (BGR) are embedded in the scheme to provide proper DC bias for receivers and transmitters, respectively. In the design, the differential data are firstly addressed by the receiver, then the transmitter deals with the data and sends them out in accordance with specified requirements. Therefore, only if both the receiver and transmitter are operated properly can the transmitted signals be output. The detailed implementation of the transceiver will be expatiated in the following sections.

![Simplistic circuit of 10-lane LVDS transceiver.](image)

### 2.1. Receiver

According to LVDS specifications [18], a receiver is required to operate in a wide input common mode voltage range of 0.05–2.35 V. Therefore, with the 1.8 V supply voltage, the receiver firstly needs to achieve the common mode voltage conversion. Figure 4 shows the simplistic circuit of a pre-stage common mode voltage shifter, which includes a current regulator and an error amplifier. The error amplifier detects the common mode voltage difference between input data (INP and INN) and reference voltage (VREF) and amplifies the voltage difference to control the current regulator by injecting or extracting currents from resistors R1 and R2. As a result, voltage drops across R1 and R2 are generated, and the common mode voltage is shifted [19]. It is obvious that the shifted common mode voltage is affected by VREF. Thus, the value of VREF was set at 0.9 V for the following rail-to-rail comparator to obtain a higher gain.

![The input common mode voltage shifter.](image)

A simple rail-to-rail comparator [20,21], as shown in Figure 5, was constructed as a composite of P and NMOS pairs. The amplifier with rail-to-rail input identifies the voltage difference from the input data (OP and ON) and converts them into currents through the input trans-conductor cell (M1–M4). After this, the currents are both mirrored and summed up at the node N1, before the data is reinstituted and reshaped by the last-stage shaping buffer.
BGR

OP ON Vout

Iref

Rail to rail comparator Shaping buffer

M1 M3 M4 M2

A cascade current mirror (M9–M12) is utilized to provide high precision current bias at a 1.8 V voltage supply.

As Figure 7 shows, the output stage of the driver uses the PMOS and NMOS configuration. A simple common mode feedback (CMFB) circuit [24,25], with transistors M5–M8, is used to stabilize the output common mode voltage (Vcm), and is less dependent on PVT. The two differential output voltages (Voutp and Voutn) are averaged to form a common mode voltage (Vcm) by two resistors (R1 and R2), which is compared with the designed reference common mode voltage (Vbg). The difference is then amplified and converted into the common mode current to adjust the common mode voltage (Vcm), and is less dependent on PVT. The two differential output voltages (Voutp and Voutn) are averaged to form a common mode voltage (Vcm), and is less dependent on PVT. The two differential output voltages (Voutp and Voutn) are averaged to form a common mode voltage (Vcm), and is less dependent on PVT.

Figure 5. Schematic of the rail-to-rail comparator.

2.2. Transmitter

In this paper, the transmitter contained three parts: a high-speed level shifter, a pre-emphasis driver and an output driver. The high-speed level shifter [22,23] was introduced to achieve the different voltage domain conversion in the pre-stage of the transmitter, whose circuit is presented in Figure 6. A pair of NMOS devices (M3 and M4) receive the low-voltage input signals (Dp_L and Dn_L) and convert them into high-voltage signals through the positive feedback transistors (M1 and M2). Then, the buffer chain with several inverters reshapes the output signals under the high-voltage (VDDH) supply.

Figure 6. Simplified schematic level shifter.

Figure 7 shows the proposed transmitter output driver based on the CMOS H-bridge structure. As Figure 7 shows, the output stage of the driver uses the PMOS and NMOS configuration. A simple common mode feedback (CMFB) circuit [24,25], with transistors M5–M8, is used to stabilize the output common mode voltage (Vcm), and is less dependent on PVT. The two differential output voltages (Voutp and Voutn) are averaged to form a common mode voltage (Vcm) by two resistors (R1 and R2), which is compared with the designed reference common mode voltage (Vbg). The difference is then amplified and converted into the common mode current to adjust the common mode voltage (Vcm). In addition, an Rc and Cc pole-zero compensation network is exploited to obtain an adequate phase margin of CMFB under the conditions created by the PVT variations. Meanwhile, a cascade current mirror (M9–M12) is utilized to provide high precision current bias at a 1.8 V voltage supply.

In addition, a pre-emphasis driver with a simple pulse-width modulation (PWM) technique [26,27] is used in the transmitter to enhance signal integrity. A simplistic circuit of this pre-emphasis driver is presented in Figure 8. The pre-emphasis driver exploits the timing relationship between signals and delay signals to establish the signal-related pulse (UP and DN), which is only enabled at the rise and fall of the signal [28,29]. During the signal transition, the pre-emphasis driver adds a current to the output node, and also extracts the current from the output node by the UP and DN pulses, so that the...
rise and fall time is decreased. Figure 9 shows the eye diagram of the transmitter after the channel, which operates at 2.5 Gbps. Figure 9a presents the simulated results of the eye diagram without a pre-emphasis driver, while the simulated results of the eye diagram with a pre-emphasis driver are shown in Figure 9b. As shown, the pre-emphasis driver is not only able to shorten the rise time but also improves the amplitude of the output signal.

![Figure 7. The architecture of the output driver.](image)

![Figure 8. Simplified schematic of the pre-emphasis driver.](image)

![Figure 9. Simulated result of the eye diagram (a) without and (b) with the pre-emphasis driver.](image)

### 3. Measured Result Analysis and Discussion

Figure 10 shows a chip microphotograph of the 10-lane LVDS transceiver. The entire chip was fabricated with SMIC 28 nm CMOS technology and the total area was 1.46 mm². The area of each TX/RX lane was 0.0333 mm², where TX and RX occupy 0.0306 mm² and 0.0027 mm², respectively. In multi-lane high-speed serial links, crosstalk and interference of lanes are important issues that deteriorate the performance of output signals. In this paper, two lanes of the transceiver shared supply voltage to improve the power integrity, and the BGR utilized a pair of individual supply voltages to provide the dependable DC bias for TX and RX, respectively. Plentiful on-chip decoupling capacitors were also inserted in the empty area to enhance signal integrity. These methods simply and effectively suppressed output jitter.
An Agilent pulse generator 81134A was used to produce $2^{31}-1$ pseudorandom bit sequence (PRBS) data patterns to the receiver, while a Tektronix MSO71604C mixed signal oscilloscope was used to detect the differential output eye diagram of the transmitter. A 22-inch coupled micro-strip line on the testing PCB acted as the transmission channel, the channel loss of which is shown in Figure 11. The channel loss was 2.2 dB at 625 MHz, and 1.8 dB at 1.25 GHz.

According to the measured results, the maximum data rate of the transceiver reached 2.5 Gbps. Figure 12a,b shows the single lane of transmitter differential output eye diagrams with $2^{31}-1$ PRBS patterns and data rates of 1.25 Gbps and 2.5 Gbps. Both output swings of the two operating data rates were around 350 mV, and the root-mean-square (RMS) jitters were 5.48 ps and 3.65 ps, respectively. Figure 12c,d show transmitter differential output eye diagrams of 1.25 Gbps and 2.5 Gbps for multi-lane transmission communication. Similarly, their output swings were around 350 mV, but their performance was degraded. This is due to the lane-to-lane interference of signals and power lines, which introduced higher deterministic jitter (DJ) that deteriorated the signal integrity of the output signals. The total power dissipation of the two operating data rates were 8.72 mW and 16.51 mW at a 1.8 V power supply for each lane.
lane transmission communication. Similarly, their output swings were around 350 mV, but their performance was degraded. This is due to the lane-to-lane interference of signals and power lines, which introduced higher deterministic jitter (DJ) that deteriorated the signal integrity of the output signals. The total power dissipation of the two operating data rates were 8.72 mW and 16.51 mW at a 1.8 V power supply for each lane.

Figure 12. Measured output eye diagrams for different data rates (a) 1.25 Gbps of single lane; (b) 2.5 Gbps of single lane (c) 1.25 Gbps of multi-lane (d) 2.5 Gbps of multi-lane.

Table 1 summarizes the comparison of the performance of the previously reported LVDS transmitters. This LVDS transmitter, based on a complementary MOS H-bridge, had excellent noise immunity performance, with an RMS jitter of 3.65 ps with a data rate up to 2.5 Gbps. The proposed LVDS transmitter also had superior power consumption performance of 16.51 mW at a data rate of 2.5 Gbps, with a figure of merit (FOM) of 6.6 mW/Gbps.

Table 1. Comparison with previous works.

| Ref. | [9] * | [15] ** | [30] * | [31] ** | This Work ** |
|------|-------|---------|--------|---------|-------------|
| Year | 2016  | 2011    | 2014   | 2018    | 2019        |
| Technology (nm) | 28 CMOS | 180 CMOS | 40 CMOS | 28 CMOS | 28 CMOS |
| Supply voltage (V) | 1.8/1 | 2.5 | 1.8/1 | 1.8/1 | 1.8/0.9 |
| Output swing (mV) | 350 | 313 | 320 | 348 | 350 |
| Data rate (Gbps) | 1 | 2 | 1 | 1 | 2.5 |
| RMS jitter (ps) | 2.2 | 7.65 | 4 | 9.8 | 3.65 |
| Power(mW) | 8.7 | 15.41 | 7 | 7.9 | 16.51 |
| Area (mm$^2$) | 0.009 | 0.061 | 0.0168 | 0.085 | 0.0306 |
| FOM # (mW/Gbps) | 8.7 | 7.705 | 7 | 7.9 | 6.60 |

*: Simulated result; **: Measured result; #: FOM = Power (mW)/Data rate (Gbps).

4. Conclusions

In this paper, a 2.5 Gbps, 10-lane, low-power, LVDS transceiver was presented. In the receiver, a pre-stage common mode voltage shifter was introduced to implement the common mode voltage conversion, and a rail-to-rail comparator embedded with a shaping buffer was utilized to recover the input signal. Compared with the characteristics of previous LVDS driver architectures, a complementary MOS LVDS driver using a CMFB circuit was exploited to provide the required output common mode voltage and differential output swing at 1.8 V supply voltage. In addition, a high-speed level shifter was designed for voltage domain conversion, and a pre-emphasis driver with PWM technique was employed to reduce the signal transition time. Further, the proposed LVDS transceiver was compatible with ANSI/TIA/EIA-644-A standards. The transceiver is easy to interoperate with other differential signaling technologies, and can be embedded in other chips as an IP core, which
makes it suitable for use in portable electronics. The whole circuit was fabricated with SMIC 28 nm CMOS technology, with a total chip area of 1.46 mm$^2$. The measured results show that the proposed low-power LVDS was able to be properly operated at 2.5 Gbps, with an RMS jitter of 3.65 ps and an FOM of 6.6 mW/Gbps.

Author Contributions: Conceptualization, X.B.; formal analysis, X.B. and J.Z.; data curation, X.B. and Y.Z.; writing—original draft preparation, X.B. and S.Z.; writing—review and editing, X.B. and S.Z.; visualization, X.B. and S.Z.; supervision, J.Z.; project administration, Y.Z.

Funding: This research was funded by National Science and Technology Major Project of China, grant number 2014ZX0302002.

Acknowledgments: The authors would like to thank the National Science and Technology Major Project of China for their support.

Conflicts of Interest: The authors declare no conflict of interest.

References
1. Park, J.; Chae, J.H.; Jeong, Y.U.; Lee, J.W.; Kim, S. A 2.1-Gb/s 12-channel transmitter with phase emphasis embedded serializer for 55-in UHD intra-panel interface. *IEEE J. Solid-State Circuits* 2018, 53, 2878–2888. [CrossRef]
2. Yousefzadeh, A.; Jabłoński, M.; Iakymchuk, T.; Linares-Barranco, A.; Rosado, A.; Plana, I.A.; Temple, S.; Serrano-Gotarredona, T.; Furber, S.B.; Linares-Barranco, B. On multiple AER handshaking channels over high-speed bit-serial bidirectional LVDS links with flow-control and clock-correction on commercial FPGAs for scalable neuromorphic systems. *IEEE Trans. Biomed. Circuits Syst.* 2017, 11, 1133–1147. [CrossRef] [PubMed]
3. Jiang, B.J.; Pan, Z.B.; Qiu, Y.H. Study on the key technologies of a high-speed CMOS camera. *Optik-Int. J. Light Electron Opt.* 2017, 129, 100–107. [CrossRef]
4. Shi, Z.; Tang, Z.A.; Feng, C.; Cai, H. Improvement to the signaling interface for CMOS pixel sensors. *Nuclear Instrum. Methods Phys. Res. Sect. A Accel. Spectrometers Detect. Assoc. Equip.* 2016, 832, 77–84. [CrossRef]
5. Jayshree; Verma, S.; Chatterjee, A. A methodology for designing LVDS interface system. In Proceedings of the IEEE Sixth International Symposium on Embedded Computing and System Design, Patna, India, 15–17 December 2016; pp. 284–288. [CrossRef]
6. Gilbert, A.; Mehmet, R.Y.; Jean-Michel, R. An integrated LVDS transmitter-receiver system with increased self-immunity to EMI in 0.18-µm CMOS. *IEEE Trans. Electromagn. Comput.* 2016, 58, 231–240. [CrossRef]
7. Gupta, H.S.; Hari, S.G.; Parmar, R.M.; Dave, R.K. High speed LVDS driver for serdes. In Proceedings of the IEEE International Conference on Emerging Trends in Electronic and Photonic Devices & Systems, Varanasi, India, 22–24 December 2009; pp. 92–95. [CrossRef]
8. Ning, H.W.; Zhen, G.Y.; Ren, Y.F. An optimal design of LVDS interface. In Proceedings of the IEEE International Conference on Computer Science and Network Technology, Harbin, China, 24–26 December 2011; pp. 2024–2026. [CrossRef]
9. Graceffe, G.A.; Gatti, U.; Calligaro, C. A 400 Mbps radiation hardened by design LVDS compliant driver and receiver. In Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, Bordeaux, France, 11–14 December 2016; pp. 109–112. [CrossRef]
10. Sun, Z.Y.; Zhang, D.; Fang, W. A ASIC chip with pipeline ADCs for CCD sensor imaging system. *Sens. Actuators A Phys.* 2018, 279, 284–292. [CrossRef]
11. Xu, H.Y.; Wang, J.; Lai, J.M. Design of a power efficient self-adaptive LVDS driver. *IEICE Electron. Express* 2018, 15. [CrossRef]
12. Li, S.; Zhang, Q.; Zhao, X.; Liu, S.; Yuan, Z.; Zhang, X. Dynamic data transmission technology for expendable current profiler based on low-voltage differential signaling. *Geosci. Instrum. Methods Data Syst.* 2017, 6, 263–267. [CrossRef]
13. Marar, H.W.; Abugharbieh, K.; Al-Tamimi, A.K. A power efficient 3 Gbps 1.8 V PMOS-based LVDS output driver. In Proceedings of the 19th IEEE International Conference on Electronics, Circuits, and Systems, Seville, Spain, 9–12 December 2012; pp. 240–243. [CrossRef]
14. Traversi, G.; De Canio, F.; Liberali, V.; Stabile, A. Design of LVDS driver and receiver in 28 nm CMOS technology for associative memories. In Proceedings of the IEEE International Conference on Modern Circuits and Systems Technology, Thessaloniki, Greece, 4–6 May 2017; pp. 1–4. [CrossRef]

15. Lv, J.; Ju, H.; Yuan, L.; Zhao, J.; Zhang, F.; Wu, B.; Jiang, J.; Zhou, Y. A high speed low jitter LVDS output driver for serial links. *Analogue Integr. Circuits Signal Process*. 2011, 68, 387–395. [CrossRef]

16. Chen, M.; Silva-Martinez, J.; Nix, M.; Robinson, M.E. Low-voltage low-power LVDS drivers. *IEEE J. Solid-State Circuits* 2005, 40, 472–479. [CrossRef]

17. Lee, S.S.; Lee, L.; Kung, F.W.; Saad, A.; Tan, G.H. A fully integrated and high precision 350 mV amplitude regulated LVDS transmitter compensating PVT variations. *Microelectron. J.* 2018, 81, 192–199. [CrossRef]

18. Telecommunications Industry Association. *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*; Standard ANSI/TIA/EIA-644-A (2001); Telecommunications Industry Association: Arlington, VA, USA, 1996.

19. Louis, L.; John, C.; Jeffrey, D. A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications. *IEEE Trans. Circuit Syst. II Analog Digit. Signal Process.* 2000, 47, 363–369. [CrossRef]

20. Divide, M.; Gaetano, P.; Salvatore, P. A new compact low-power high-speed rail-to-rail Class-B buffer for LCD applications. *J. Disp. Technol.* 2010, 6, 184–190. [CrossRef]

21. Nagy, L.; Arbet, D.; Kovac, M.; Potocny, M.; Stopjakova, V. Design and performance analysis of ultra-low voltage rail-to-rail comparator in 130 nm CMOS technology. In Proceedings of the IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits and Systems, Budapest, Hungary, 25–27 April 2018; pp. 51–54. [CrossRef]

22. Pritt, G.; Ujwala, G. Design of voltage level shifter for multi-supply voltage design. In Proceedings of the International Conference on Communication and Signal Processing, Melmaruvathur, India, 6–8 April 2016; pp. 853–857. [CrossRef]

23. Lanuzza, M.; Corsonello, P.; Perri, S. Low-Power Level Shifter for Multi-Supply Voltage Designs. *IEEE Trans. Circuits Syst. II Express Briefs* 2012, 59, 922–926. [CrossRef]

24. Ahmed, N.; Edgar, S.-S.; Jose, S.-M. A fully balanced pseudo-differential OTA with common mode feedback and inherent common mode detector. *IEEE J. Solid-State Circuits* 2003, 38, 663–668. [CrossRef]

25. Basu, J.; Mandal, P. Effect of switched-capacitor CMFB on the gain of fully differential OP-Amp for design of integrators. In Proceedings of the IEEE International Symposium on Circuits and System, Florence, Italy, 27–30 May 2018; pp. 1–5. [CrossRef]

26. Ševčik, B.; Brančik, L. Time-domain pre-emphasis technique based on pulse-width modulation scheme. In Proceedings of the IEEE International Conference on Telecommunications and Signal Processing, Budapest, Hungary, 18–20 August 2011; pp. 483–486. [CrossRef]

27. Gilbert, A.; Huang, H.Y. Equalization and pre-emphasis based LVDS transceiver. *Analogue Integr. Circ. Signal Process.* 2013, 75, 109–123. [CrossRef]

28. Jawed, S.A.; Asghar, A.; Khan, K.; Abbasi, S.; Naveed, M.; Siddiqi, Y.; Siddiqi, W. A configurable 2-Gbps LVDS transceiver in 150-nm CMOS with pre-emphasis, equalization, and slew rate control. *Int. J. Circuit Theory Appl.* 2017, 45, 1369–1381. [CrossRef]

29. Xu, Y.; Sun, T.Q.; Zhao, F.; Hu, C. A full-integrated LVDS transceiver in 0.5 μm CMOS technology. In Proceedings of the IEEE Conference on Industrial Electronics and Applications, Hangzhou, China, 9–11 June 2014; pp. 1672–1675. [CrossRef]

30. Ayyagari, R.; Gopal, K. Low power LVDS transmitter design and analysis. In Proceedings of the IEEE The Asia-Pacific Conference on Communication, Ishigaki, Japan, 1–3 October 2014; pp. 42–45. [CrossRef]

31. Traversi, G.; De Canio, F.; Liberali, V.; Stabile, A. Characterization of an LVDS link in 28 nm CMOS for multi-purpose pattern recognition. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 43–47. [CrossRef]