Current Mode Neuron for the Memristor based synapse

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Abstract—Due to many limitations of Von Neumann architecture such as speed, memory bandwidth, efficiency of global interconnects and increase in the application of artificial neural network, researchers have been pushed to look into alternative architectures such as Neuromorphic computing system. Memristors (memristive crossbar memory RCM) are used as synapses due to its high packing density and energy efficiency and CMOS blocks as neurons. The increase in the terminal resistance of the RCM can degrade its energy efficiency and bandwidth. A more energy efficient current mode neuron has been proposed in this paper which can operate at lower voltages as compared to conventional voltage mode neuron circuit.

I. INTRODUCTION

The increasing demand for computation and decreasing size of transistors have led to the integration of multiple cores and memory on a single chip. The number of buses as well as the resistance per unit length of metal wire on the chip has increased. These factors have put restriction on the speed of computation. In recent years, the popularity of the Neural Network has grown due to the increase of its application in image processing, etc. Computation (such as dot product) at the sensor level can reduce the number of buses, high-speed data converters and interface circuits. The memristor crossbar array is used to build an analog neural network which can compute dot products which are widely used in the image processing application. One of the important modules of the neural network is the activation function like sigmoid function which is used in clustering and pattern recognition problems. Mostly the sigmoid function is implemented in voltage mode, but in this paper, we have proposed a more efficient current mode neuron for memristor-based synapse and compared it with the voltage mode neuron in terms of power, bandwidth, input impedance and robustness. With current mode processing, one can work with lower values of voltages, as has been shown in previous work. This presents the possibility of achieving significant reduction in power consumption.

This paper is organized into the following sections: Section II introduces us to the memristor crossbar array, the relation between input current or voltage with the output current and the effect of parasitic and terminal resistance on power, bandwidth and accuracy. Section III contains voltage mode CMOS sigmoid activation function circuit for meristors with its simulation result and compares it with other sigmoid function circuits in voltage mode. Section IV contains the proposed current mode sigmoid activation function circuit for memristors with the detailed simulation results and compares the low input impedance stage (current to voltage converter) used in this paper with another current to voltage stage. Section V compares the voltage mode circuit with the proposed current mode circuit.

II. RCM Computation

A memristor, as proposed by Prof. Leon Chua in 1971, is a passive two-terminal fundamental element, in addition to the existing resistor, capacitor, and inductor. It follows a non-linear relation between terminal voltage \( v(t) \) and resultant current \( i(t) \), given by

\[
i(t) = G_m(x).v(t)
\]

\[
\frac{\partial x}{\partial t} = i
\]

where \( G_m(x) \) is not a constant but a state dependent transconductance. A memristor has two regions—high concentration dopant region of resistance \( R_{on} \) and low concentration dopant region of resistance \( R_{off} \). The total resistance which is a sum of \( R_{on} \) and \( R_{off} \) can be changed by applying a voltage bias. Hence the net transconductance is given by

\[
G_m(x) = G_{moff}(1-x) + G_{mon}x
\]

A specific amount of energy (or threshold voltage) is required to change the stage of a memristor, and below the threshold voltage, memristor behaves as a constant transconductance or resistance. A memristor crossbar array has very high density, low power consumption, and variable transconductance. These properties make it suitable to be used as synapses in an Artificial Neural Network or dot product operation which is heavily computed in Image processing.

A \( N \times N \) memristor crossbar array consists of horizontal \( i \) and vertical \( j \) metal lines which are connected by memristors of conductance \( g_{mi} \). These metal lines contribute to the parasitics which can be modeled as parasitic resistance \( R_p \), between two nodes and parasitic capacitance \( C_p \) between a node and ground. In voltage mode (Fig. 1), \( V_1, V_2, ..., V_i, ..., V_N \) voltages are applied to the corresponding horizontal lines \( i \) and vertical lines \( j \).
resultant currents \( I_j \) from the vertical lines \( (j) \) are converted into voltages by using opamp circuits. The resultant current in a vertical line \( (j) \) is given by

\[
I_j = \sum_{i=1}^{n} g_{m_{ij}} V_i \tag{4}
\]

Similarly, in the current mode (Fig. 2), \( I_1, I_2, \ldots, I_i, \ldots, I_N \) input currents are applied to the corresponding horizontal lines \( (i) \) and the resultant current in the vertical line is given by

\[
I_j = \sum_{i=1}^{n} I_i \frac{g_{ji}}{g_{ii} + g_{2i} + \ldots + g_{ji} + \ldots + g_{Ni}} \tag{5}
\]

Equations (4) and (5) are valid provided that the input impedance (Terminal Resistance \( R_t \)) of the current sensing circuit is very low. The conductance of the last memristor has to be set in such a way that the sum of the memristor conductance i.e \( g_{1i} + g_{2i} + \ldots + g_{ji} + \ldots + g_{Ni} \) is same for every \( i^{th} \) row.

### A. Simulation Results

The effect of parasitic \( R_p \) and terminal resistance \( R_t \) on bandwidth, energy, and accuracy of the dot product through numerical analysis performed on MATLAB are shown in Figure 3. In Figure 3(a), we observe that the bandwidth of the RCM network decreases with an increase in the terminal resistance. Figure 3(b) and Figure 3(d) show the deterioration in the accuracy of the dot product operation with increasing \( g_m \) (conductance of memristor) and decreasing \( g_t \) (inverse of terminal resistance \( R_t \)). The effect of increasing terminal resistance on the energy per computation is shown in Figure 3(c). We observe that beyond a critical \( R_T \), the energy consumption increases linearly with terminal resistance, i.e., the input impedance of the neuron circuit. Hence, it's crucial to keep low input impedance (or terminal resistance \( R_t \)).

### III. Voltage Mode Sigmoid Neuron

The circuit consists of a current to voltage converter followed by a single stage differential amplifier in negative feedback and an inverter in negative feedback. Input impedance is approximately equal to the feedback resistance \( R \) divided by the gain of the opamp. The opamp used here is a compensated (Compensation capacitor = 200fF and phase margin = 60) two-stage differential amplifier where the first stage is differential with current mirror loading and the second stage is a common source stage. The sigmoid function is given by the below expression

\[
y = \frac{a}{1 + e^{b(x-c)}} \tag{6}
\]

Fig. 3: (a) Bandwidth vs \( R_t \) (b) Error in dot product vs \( g_m \) (c) Energy Consumption vs Computation (d) Error in dot product vs \( g_t \)

Fig. 4: Voltage Mode Sigmoid Activation Function

The output of the single stage differential amplifier in negative feedback provides an approximate sigmoid function and gain
TABLE I: Sigmoid function parameter in Voltage mode

|   | a                | b               | c               |
|---|-----------------|-----------------|-----------------|
|   | 1.754 (1.723, 1.785) | -2.13 \times 10^6 \text{(-2.36 \times 10^6, -1.89 \times 10^6)} | 4.963 \times 10^{-6} (4.903 \times 10^{-6}, 5.024 \times 10^{-6}) |
| RMSE | 0.06422          |                 |                 |

is controlled by the inverter in negative feedback [2]. In this case, parameter c depends on reference voltage ($V_{\text{ref}}$) and b depends on the gain of the opamp stage (i.e. $-R_3/R_4$) and gain of the inverter stage (i.e. $-R_2/R_1$). The inverter stage is used to obtain rail to rail voltage swing as the opamp stage has restricted output voltage swing. The voltage swing decides the value of the parameter a.

A. Simulation Results

All the circuit simulation results are performed in Cadence Virtuoso using TSMC 180nm library. In figure 5, dots represent the sigmoid transfer characteristic obtained and it is fitted to an ideal transfer characteristic (as shown). The parameters with 95% confidence bound are (Table I)

![Fig. 5: Sigmoid Transfer Function obtained from Voltage Mode Neuron](image)

The variation of the sigmoid function parameters (Monte Carlo Simulation with 200 samples) on scaling VDD

| VDD (V) | a         | Std % | b         | Std % | c         | Std % |
|---------|-----------|-------|-----------|-------|-----------|-------|
| 1.8     | 1.7489    | 1.13% | -2.25 \times 10^6 | 8.4%  | 4.95 \times 10^{-6} | 1.16% |
| 1.5     | 1.4979    | 3.52% | -2.28 \times 10^6 | 11.2% | 4.94 \times 10^{-6} | 1.87% |
| 1.0     | 0.9525    | 9.08% | -1.44 \times 10^6 | 13.32%| 4.72 \times 10^{-6} | 5.96% |

TABLE II: The variation of the sigmoid function parameters (Monte Carlo Simulation with 200 samples) on scaling VDD

The bandwidth of the voltage based neuron is 50Mhz. The maximum current consumption of the circuit is 56µA (Power = 100.8µW). On scaling down the voltage, the power consumption of the circuit will decrease proportionally. Input impedance is 243Ω with zero at 78KHz. On scaling down the voltage, the gain of the opamp will decrease slightly which results in a slight increase in the input impedance to 307Ω.

In one of the papers, the sigmoid circuit is implemented by the current buffer followed by a sigmoid circuit (Power 160µW) [5] and in another paper, they have proposed memristor based sigmoid activation function (Power = 0.244mW) [4]. The transfer function of sigmoid (reported in this paper) is not symmetric with respect to central horizontal axis [4].

IV. CURRENT MODE SIGMOID NEURON

The circuit consists of a low input impedance stage followed by a differential stage (Fig.8). The input impedance is given by the following expression.

$$R_{in} = \frac{r_{ds7}}{1 + g_m7 \cdot r_{ds7} \cdot A}$$

Where $g_m7$ and is the transconductances of $M_7$, $r_{ds7}$ is the small signal resistance of $M_7$, and $A$ is the gain of the opamp. Here opamp has a single stage differential amplifier with a diode connected NMOS load. Parameter b of the sigmoid function depends on the transconductance of $M_3/4$, and $1/g_m$ of $M_6/7$. $I_{BIAS2}$ of the right current mirror and $I_{BIAS3}$ decides the value of parameters c and a respectively. $C_c$ is the compensation capacitor and $R_c$ is the resistance.

A. Simulation Results

The value of $C_c$ and $R_c$ is 100fF and 10KΩ respectively to have 63° Phase Margin.

![Fig. 7: Monte Carlo Simulation with 200 samples at VDD = 1.8](image)
TABLE III: Sigmoid function Parameter with 95% confidence bound

| VDD | $Z_{th}(\Omega)$ | Bandwidth (MHz) | Power ($\mu W$) |
|-----|----------------|----------------|---------------|
| 1.8 | $2.06(344)$    | 6.25           | 40.5          |
| 1.5 | $1.26(130)$    | 5.2            | 33.75         |
| 1.0 | $274(266)$     | 10             | 12.5          |

TABLE IV: Input Impedance, Power and Bandwidth Variation on scaling voltage

| VDD (in V) | $Z_{th}(\Omega)$ | Bandwidth (MHz) | Power ($\mu W$) |
|------------|----------------|----------------|---------------|
| 1.8        | $2.06(344)$    | 6.25           | 40.5          |
| 1.5        | $1.26(130)$    | 5.2            | 33.75         |
| 1.0        | $274(266)$     | 10             | 12.5          |

TABLE V: The variation of the sigmoid function parameters (Monte Carlo Simulation with 200 samples) on scaling VDD

| VDD (V)  | a    | b    | c    |
|----------|------|------|------|
| 1.8      | $4.917 \times 10^{-6}$ | $-2 \times 10^{4}$ | $2.618 \times 10^{-6}$ |
| 1.5      | $4.917 \times 10^{-6}$ | $-2.01 \times 10^{4}$ | $-1.99 \times 10^{4}$ |
| 1.0      | $2.618 \times 10^{-6}$ | $-2.615 \times 10^{6}$ | $-2.62 \times 10^{6}$ |

RMSE = $8.506 \times 10^{-9}$

In this paper, we have shown the degradation in the performance of RCM for dot product operation due to terminal resistance which is the input impedance of the neuron circuit. Error in the dot product operation increases with increase in the terminal resistance and decrease in the mem-resistance. To avoid this degradation, we have proposed current mode neuron which has low input impedance and more power efficient compared to the existing neuron.

Power Consumption of Current Mode Neuron is half compared to voltage mode neuron at VDD = 1.8. Current mode neuron is much faster compared to voltage based neuron. On applying full input swing, the time required for the output to saturate is 4ns and 40ns in current and voltage mode respectively. Voltage mode has higher bandwidth compared to current mode neuron, but we cannot operate at such high frequency because input impedance is large at that frequency and the equation (4) is no longer valid. The current mode neuron circuit does not require any large resistor, so it is more area efficient. The sigmoid transfer characteristic (Fig. 9) obtained from current mode neuron matches more perfectly with an ideal sigmoid function, while a deviation is observed in the voltage mode transfer characteristic (Fig. 5). From II and V, we observe that current mode neuron can be operated at lower VDD with less variation in parameters a, b, and c of the sigmoid function.

V. Conclusion

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