Analysis and Verification of a Wide Input Voltage PWM Converter with Variable Windings

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Abstract: A three-leg pulse-width modulation converter with auxiliary windings is provided and investigated to realize wide voltage operation and zero voltage switching characteristics on power switches. The presented converter has three converter legs on the input-side and two sets of winding turns on the output-side. Owing to the on/off states of the three converter legs and the two sets of secondary winding turns, the proposed converter can be operated under three different equivalent circuits to have wide input voltage operation from 30V ~ 240V ($V_{\text{in,max}} = 8V_{\text{in,min}}$). Compared with the multi-stage converters to realize wide input voltage operation, the proposed circuit topology has fewer circuit components and a simple control algorithm. Conventional duty cycle control with phase-shift between each converter leg is adopted to regulate load voltage and also accomplish zero voltage switching on active switches. The presented three-leg converter is tested with a laboratory circuit. Finally, experiments testify to the performance and validity of the presented converter.

Keywords: pulse-width modulation; zero voltage switching; power converters; three-leg converters

1. Introduction

Renewable energy sources are widely developed and investigated to lessen fossil fuel demand and reduce air pollution. From many renewable power sources, solar or wind power is more attractive due to the cost effectiveness. Power electronics play a more and more important role to convert the unstable input voltage from solar panels and wind generators to a stable direct-current (DC) or alternative-current (AC) voltage. Power electronics have been developed for low power (such as personal computer power units, battery chargers, consumer electronics, and solid-state lighting systems) and medium power applications (such as server power units, DC micro grid power conversion, and renewable energy power conversion). Due to the wide deviation of wind speed or solar intensity, the output voltage of wind generators or photovoltaic panels is not constant. The maximum output voltage versus minimum output voltage of the solar panels may be greater than 4:1. Conventional DC converters with wide voltage operation [1–7] for wind and solar power conversion are based on the circuit topologies of series-parallel connection or multi-stage conversion. However, the multi-stage circuit structure will result in low circuit efficiency and reliability. The wide voltage DC converters were studied in [8–12] to have soft switching operation and high efficiency. However, the complicated control scheme is the main drawback for these circuit topologies. The series and parallel resonant converters have been developed for lighting and industry applications [13,14]. The switching frequency of the resonant converters are dependent on the load conditions. The power switches turn on under zero voltage. Therefore, the switching losses are improved under high frequency operation. Compared with series or parallel resonant converters, the LLC (inductor-inductor-capacitor) resonant converters [15–18] are more attractive in consumer and industry applications such as server power and power units in personal computers and plug-in hybrid electric vehicles. Unfortunately, the narrow voltage range and...
wide switching frequency range are the main drawbacks of the LLC converters. For photovoltaic and fuel cell power applications, the solar panel or fuel cell output is a variable voltage that is related to the solar intensity. The low power units of railway systems, the input voltage of DC converters for motor drive controllers, lighting systems, electric door systems, and braking systems may be varied from 24 V to 110 V. For hybrid electric vehicle or electric vehicle systems, the output voltage of battery chargers is varied between 200 V and 450 V. Therefore, the wide voltage DC converters [19–21] have been developed as the interface circuits to convert the solar power to electric power. In [21], the PWM converter was presented with two transformers and one alternating current switch to achieve 4:1 \( (V_{in,max} = 4V_{in,min}) \) input voltage operation capability. Four operating circuits can be controlled [21] to realize wide voltage operation. However, the control algorithm in [21] was not easy to implement with the commercial analog integrated circuit. For remote control demand in stand-alone solar power systems, the wide voltage DC converter is needed to supply the necessary power for the control system, and the input voltage range of power units for controller demand is normally more than 4:1 \( (V_{in,max} \geq 4V_{in,min}) \). Therefore, the circuit topologies in [19–21] cannot achieve this wide voltage demand.

This paper proposes a three-leg DC converter with auxiliary winding turns to accomplish low switching loss and wide voltage operation \( (30 \text{ V} \sim 240 \text{ V}) \). According to the different winding turns, there are three sub-circuits in the present converter to obtain three different voltage gains. Thus, the wide voltage operation is achieved in the presented pulse width modulation (PWM) converter. Three converter legs are used on the high voltage side to achieve 4:1 voltage range operation, and two secondary winding sets are used on the low voltage side to realize the other 2:1 voltage range operation. Two voltage comparators are employed in the control circuit to select the different primary and secondary turns and voltage gains. The reference voltages of the two voltage comparators are designed at 60 V and 120 V. Therefore, the presented converter can achieve 8:1 \( (30 \text{ V} \sim 240 \text{ V}) \) wide voltage operation. Compared with the former wide voltage DC converter, the presented converter has a wider voltage range operation and is easier to implement with an analog or digital control circuit. The description of the presented circuit is discussed in Section 2. Three operation ranges of the presented circuit are provided in Section 3. The circuit characteristics and design procedures of the studied converter are demonstrated in Section 4. Experimental verifications are demonstrated in Section 5. Finally, the conclusions are discussed in Section 6.

2. Description of the Presented Converter

The proposed circuit topology is provided in Figure 1. As can be noted, three converter legs and one AC switch (two MOSFETs (metal–oxide–semiconductor field-effect transistor) connected by a back-to-back structure) are used on the input-side, and two sets of secondary winding turns and two AC switches are used on the output-side. The magnetic transformer with two primary turns \( n_p \) and two different secondary turns \( n_{s1} \) and \( n_{s2} \) is used in the proposed circuit topology. Switch \( S_1 \) is on or off to select the full-bridge circuit with the larger primary turns \( 2n_p \) \( (S_1 \text{ on, } Q_3 \text{ and } Q_4 \text{ off}) \) or less primary turns \( n_p \) \( (S_1, Q_5, \text{ and } Q_6 \text{ off}) \) on the input-side. Two AC switches \( S_2 \) and \( S_3 \) are on/off on the output-side to select the secondary turns \( n_{s1} \) or \( n_{s1}+n_{s2} \) connected to the output inductor. According to the on/off states of \( S_1 \sim S_3 \) and \( Q_1 \sim Q_6 \), the presented three-leg PWM converter has three different equivalent circuits (Figure 2) under three voltage ranges: low voltage range \( (V_{in,min} \sim 2V_{in,min}) \), medium voltage range \( (2V_{in,min} \sim 4V_{in,min}) \), and high voltage range \( (4V_{in,min} \sim 8V_{in,min}) \). For low voltage operation, the equivalent circuit is given in Figure 2a. It can be seen that switches \( S_1, S_2, Q_5, \) and \( Q_6 \) are off and \( S_3 \) is on. Since the phase-shift PWM scheme is adopted to generate the PWM signals of \( Q_1 \sim Q_4 \), the equivalent full-bridge converter \( (Q_1 \sim Q_4, L_1, T, D_{3}, D_{4}, L_2, \text{ and } C_o) \) with transformer turns-ratio \( N_L = n_p/(n_{s1}+n_{s2}) \) is operated to achieve high voltage gain \( G_L = V_o/V_{in,L} = 2d_{eff}/N_L \), where \( V_{in,L} \) denotes \( V_{in} \) in the low input voltage range and \( d_{eff} \) is the effective duty cycle of the full-bridge converter. Figure 2b gives the equivalent circuit of the proposed converter under the medium input voltage range \( V_{in,M} = 2V_{in,min} \sim 4V_{in,min} \). \( Q_3, Q_4, \) and \( S_2 \) are in the off-state, and \( S_1 \) and \( S_3 \) are in the on-state. The equivalent circuit with components \( Q_1, Q_2, Q_5, Q_6, L_{r1}, L_{r2}, D_{3}, D_{4}, L_2, C_o, \) and \( T \) with turns-ratio
\( N_M = \frac{2n_P}{n_s_1 + n_s_2} \) is adopted for the medium voltage range to achieve the low voltage gain \( G_M = \frac{V_o}{V_{in,M}} = 2d_{eff}/N_M \). Figure 2c provides the equivalent circuit for high voltage range operation \( (V_{in,H} = 4V_{in,min} - 8V_{in,min}) \). The switches \( Q_3, Q_4, \) and \( S_3 \) are in the off-state, and \( S_1 \) and \( S_2 \) are in the on-state. The equivalent circuit shown in Figure 2c has voltage gain \( G_H = \frac{V_o}{V_{in,H}} = 2d_{eff}/N_H \), where \( N_H = \frac{2n_P}{n_s_1} \). According to the above discussion, the proposed converter can be operated at three different input voltage ranges by proper selection of the on/off states of \( Q_1-Q_6 \) and \( S_1-S_3 \) to achieve wide voltage operation from \( V_{in,min} \) to \( 8V_{in,min} \).

**Figure 1.** Circuit structure of the developed converter.

**Figure 2.** Equivalent circuit of the proposed converter for (a) low voltage range, (b) medium voltage range, and (c) high voltage range.
3. The Principle of Operation

3.1. Low Voltage Operation ($S_3$ on; $Q_5$, $Q_6$, $S_1$, $S_2$ off)

When $V_{in,min} \leq V_{in} < 2V_{in,min}$, the active switches $Q_5$, $Q_6$, $S_1$, and $S_2$ are off and $S_3$ is on. The proposed converter has $n_p$ primary winding turns and $n_s_1 + n_s_2$ secondary winding turns in Figure 2a. In the presented circuit, it is assumed that $L_{m_1}$ and $L_{m_2} \gg L_{r_1}$ and $L_{r_2}$, $C_{Q_1} = \ldots = C_{Q_6} = C_{oss}$, and $n_s_1 = n_s_2$. Figure 3a demonstrates the main voltage and current waveforms under low voltage operation. The voltage gain of the presented converter for low voltage operation is $G_L = 2d_{off}/N_L = 4n_s_1d_{off}/n_p$. There are ten operation modes in every one switching period. Figure 3b–k gives these ten equivalent operating circuits. Since the PWM waveforms are symmetrical between Modes 1–5 and Modes 6–10, only the circuit operations of Modes 1–5 are examined in the following discussion.

Mode 1 [$t_0$, $t_1$]: Mode 1 begins at $t = t_0$ when $Q_1$ and $Q_4$ ($Q_2$ and $Q_3$) are active (inactive) on the input-side and $D_3$ conducts on the output-side. The input current flows through the components $Q_1$, $T$, $L_{r_1}$, and $Q_4$, and the output current flows through the components $T$, $D_3$, $L_o$, and $C_o$. The magnetizing voltage $v_{Lm_1} \approx V_{in}$ (due to $L_{m_1} \gg L_{r_1}$) and $v_{L_o} \approx V_{in}/N_L - V_o$. Thus, $i_{Lr_1}$ and $i_{L_o}$ are calculated as:

$$i_{Lr_1}(t) = i_{Lr_1}(t_0) + (V_{in} - N_L V_o)(t - t_0)/(N_L^2 L_o)$$

$$i_{L_o}(t) = i_{L_o}(t_0) + (V_{in}/N_L - V_o)(t - t_0)/L_o$$

Therefore, $i_{Lr_1}$ and $i_{L_o}$ increase in Mode 1, and $v_{CQ_2} = v_{CQ_3} = V_{in}$ and $v_{D4} = 2V_{in}/N_L$.

Figure 3. Cont.
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Therefore, the output capacitors $C_{Q1}$ and $C_{Q2}$ of switches $Q_1$ and $Q_2$ charge from 0 V and discharged from $V_{in}$, respectively. If the inductor energy $(L_{r1} + N_1^2 L_0)J_{L1}(t_1)$ is greater than the capacitor energy $2C_{Q3}V_{in}^2$, then the capacitor $C_{Q2}$ is discharged to zero voltage at $t = t_2$. The time interval of this mode is given in Equation (3).

$$\Delta t_{12} = 2C_{Q3}V_{in}/i_{L1}(t_1) = 2N_1C_{Q3}V_{in}/i_{L0}(t_1)$$  \hspace{1cm} (3)

The dead time $t_d$ between the PWM signals of $Q_1$ and $Q_2$ must be greater than $\Delta t_{12}$ to accomplish the soft switching turn-on of $Q_2$.

Mode 3 [$t_2$, $t_3$]: The inductor current $i_{L1} > 0$, and $v_{Q2} = 0$ at $t_2$. The body diode $D_{Q2}$ of switch $Q_2$ is conducting, and $Q_2$ can be turned on after time $t_2$ to achieve soft switching turn-on. The primary current $i_{L1}$ is flowing the components $Q_2$, $T$, $L_{r1}$, and $Q_4$, and $v_{L_{in1}} = 0$. The secondary-side diodes $D_3$ and $D_4$ are both conducting, $v_{i_0} = -V_o$, and $i_{i_0}$ decreases in this mode. The inductor currents are given as:

$$i_{L1}(t) \approx i_{L1}(t_2) - (V_{Q2,drop} + V_{Q4,drop})(t - t_2)/L_{r1}$$  \hspace{1cm} (4)

$$i_{i_0}(t) = i_{i_0}(t_2) - (V_o)(t - t_2)/L_o$$  \hspace{1cm} (5)

where $V_{Q2,drop}$ and $V_{Q4,drop}$ are the voltage drop on switches $Q_2$ and $Q_4$, respectively. The diode currents $i_{D3}$ ($i_{D4}$) decrease (increase), and the slopes of the diode currents are calculated as:

$$di_{D4}(t)/dt = -di_{D3}(t)/dt = N_1(V_{Q2,drop} + V_{Q4,drop})/2L_{r1}$$  \hspace{1cm} (6)

Mode 4 [$t_3$, $t_4$]: Mode 4 starts at time $t_3$ when the lagging switch $Q_4$ turns off. The primary current $i_{L1}$ at time $t_3$ is positive. Therefore, the output capacitor $C_{Q3}$ ($C_{Q4}$) of switch $Q_3$ ($Q_4$) is discharged (charged) from $V_{in}$ (0V). Due to $D_3$ and $D_4$ conducting in Mode 4, it can obtain $v_{L_{in1}} = 0$. If the inductor energy $L_{r1}^2J_{L1}(t_3)$ is greater than the energy $2C_{Q3}V_{in}^2$, then it can obtain $v_{CQ3}(t_4) = 0$. The time interval of this mode is given in Equation (7).

$$\Delta t_{34} = 2C_{Q3}V_{in}/i_{L1}(t_3)$$  \hspace{1cm} (7)

The dead time $t_d$ between the PWM signals of $Q_3$ and $Q_4$ must be greater than $\Delta t_{34}$ to accomplish soft switching turn-on of $Q_3$.

Mode 5 [$t_4$, $t_5$]: At $t = t_4$, $i_{L1} > 0$, and $v_{CQ3} = 0$. The body diode $D_{Q3}$ of the lagging-leg switch $Q_3$ is forward biased. After time $t_4$, $Q_3$ turns on under zero voltage. The $D_3$ and $D_4$ are still conducting...
in this mode. The leg voltage \( v_{ab} = -V_{in} \) and the inductor voltage \( v_{Lr1} \approx -V_{in} \), so that \( i_{Lr1} \) decreases. In Mode 5, \( i_{D3} (i_{D4}) \) decreases (increases). The slopes of \( i_{D3} \) and \( i_{D4} \) are expressed as:

\[
di_{D4}(t)/dt = -di_{D3}(t)/dt \approx N_L V_{in}/2L_{r1}
\]

The diode current \( i_{D3} \) is decreased to zero at time \( t_5 \), and the time duration of Mode 5 is calculated as:

\[
\Delta t_{45} = 2L_{r1}I_o/(N_L V_{in})
\]

The duty cycle loss in this mode is obtained as:

\[
d_{loss,5} = \Delta t_{45}/T_{sw} = 2L_{r1}I_o/(N_L V_{in} T_{sw})
\]

where \( T_{sw} \) is the switching period of PWM waveforms. After the time \( t_5 \), the converter operation goes to the next half switching period.

3.2. Medium Voltage Operation (\( S_1, S_3 \) on; \( Q_3, Q_4, S_2 \) off)

When \( V_{in} \) is in the medium voltage range (\( 2V_{in,min} \leq V_{in} < 4V_{in,min} \)), \( S_1 \) and \( S_3 \) are in the on-state and \( Q_3, Q_4, \) and \( S_2 \) are in the off-state (Figure 2b). The proposed converter has \( 2n_p \) primary winding turns and \( n_{s1} + n_{s2} \) secondary winding turns in Figure 2b. The voltage gain for medium voltage operation is \( G_m = 2d_{off}/N_M = 2n_{s1}d_{off}/n_p \). Comparing the voltage gains \( G_L \) and \( G_M \), it can be noted that \( G_L = 2G_M \). Figure 4a demonstrates the main voltage and current waveforms under medium voltage operation. There are ten operation modes in every one switching period. Figure 4b–k gives these ten equivalent operating circuits. Since the PWM waveforms are symmetrical for each half switching cycle, only the circuit operations of Modes 1–5 are discussed in the following.

Mode 1 \([t_0, t_1]\): \( Q_1, Q_6, \) and \( D_3 \) conduct at time \( t_0 \). The input current flows through \( Q_1, T, L_{r1}, L_{r2}, \) and \( Q_6, \) and the output current flows through \( T, D_3, L_o, \) and \( C_o. \) The magnetizing voltage \( v_{LM1} + v_{LM2} \approx V_{in} \) due to \( L_{m1} + L_{m2} \gg L_{r1} + L_{r2} \). Since \( v_{L0} \approx V_{in}/N_M - V_o > 0, \) \( i_{Lr1} \) and \( i_{Lo} \) both increase linearly, and \( i_{Lr1}(t) = i_{Lr2}(t) \approx i_{L0}(t)/N_M. \) The drain-to-source voltages of \( Q_2 \) and \( Q_5 \) are equal to \( V_{in}, \) and the diode voltage \( v_{D4} = 2V_{in}/N_M. \)

![Figure 4. Cont.](image-url)
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Figure 4. PWM waveforms and equivalent circuits at medium voltage range operation: (a) PWM voltage and current waveforms for (b) Mode 1, (c) Mode 2, (d) Mode 3, (e) Mode 4, (f) Mode 5, (g) Mode 6, (h) Mode 7, (i) Mode 8, (j) Mode 9, and (k) Mode 10.

Mode 2 \([t_1, t_2]\): At time \(t = t_1\), the leading-leg switch \(Q_1\) is turned off. \(i_{Lr1}\) is positive, and \(C_{Q2}\) is discharged from \(V_{in}\). If the inductor energy \((L_{r1} + L_{r2} + N_H^2 I_{Lr1})^2 L_{r1}\) at time \(t_1\) is greater than the capacitor energy \(2C_{oss}V_{in}^2\), then \(C_{Q2}\) can be discharged to zero voltage at time \(t_2\).

Mode 3 \([t_2, t_3]\): Since \(v_{CQ2}(t_2) = 0\) and \(i_{Lr1}(t_2) > 0\), the body diode \(D_{Q2}\) conducts, and the leading-leg switch \(Q_2\) can be turned on under zero voltage. The leg voltage \(v_{ac} = 0\) and the primary-side and secondary-side voltages of transformer \(T\) are zero voltage. Thus, \(D_3\) and \(D_4\) both conduct. Therefore, \(v_{Lo} = -V_o\), and \(i_{Lo}\) is decreasing.

Mode 4 \([t_3, t_4]\): Since \(Q_6\) is turned off at time \(t_3\) and \(i_{Lr1}(t_3) > 0\), \(C_{Q5}\) is discharged. The magnetizing voltages \(v_{Lm1} = v_{Lm2} = 0\). If the inductor energy \((L_{r1} + L_{r2})^2 L_{r1}(t_3) > 2C_{oss}V_{in}^2\), then \(v_{CQ5}\) will reach zero voltage at time \(t_4\).

Mode 5 \([t_4, t_5]\): Since \(v_{CQ5}(t_4) = 0\) and \(i_{Lr1}(t_4) > 0\), the body diode \(D_{Q5}\) conducts, and \(Q_5\) can turn on at time \(t_4\) under zero voltage. In this mode, \(v_{ac} = -V_{in}\) and \(v_{Lm1} = v_{Lm2} = 0\) due to \(D_3\) and \(D_4\) conducting. \(v_{Lr1} + v_{Lr2} = -V_{in}\), and \(i_{Lr1}\) decreases. At time \(t_5\), \(i_{D3}\) is decreased to zero. Then, the converter operation goes to the next half switching period.

3.3. High Voltage Operation \((S_1, S_2\ on; Q_3, Q_4, S_3\ off)\)

When \(4V_{in,min} < V_{in} < 8V_{in,min}\), \(S_1\) and \(S_2\) are turned on and \(Q_3, Q_4\ and \(S_3\) are turned off (Figure 2c). This equivalent circuit has \(2n_p\) primary turns and \(n_s_1\) secondary turns, and the voltage gain \(G_H = 2d_{eff}/N_H = n_{s2}d_{eff}/n_p\). Comparing the voltage gains \(G_L, G_M,\) and \(G_H\), it can be noted that \(G_L > G_M > G_H\). Figure 5a demonstrates the main voltage and current waveforms under high voltage operation. Figure 5b–k gives these ten equivalent operating circuits. Since the PWM waveforms are symmetrical for each half switching cycle, only the circuit operations of Modes 1–5 are discussed in the following.
Figure 5. Cont.
Figure 5. PWM waveforms and equivalent circuits at high voltage range operation: (a) PWM voltage and current waveforms for (b) Mode 1, (c) Mode 2, (d) Mode 3, (e) Mode 4, (f) Mode 5, (g) Mode 6, (h) Mode 7, (i) Mode 8, (j) Mode 9, and (k) Mode 10.

Mode 1 \([t_0, t_1]\): At \(t = t_1\), \(D_1\), \(Q_1\) and \(Q_6\) conduct. \(i_{LR_1}\) flows through \(Q_1\), \(T\), \(LR_1\), \(LR_2\), and \(Q_6\) on the primary-side of transformer \(T\). \(i_{LR_2}\) flows through \(D_1\), \(L_o\), and \(C_o\) on the secondary-side of \(T\). Since \(v_{io} \approx V_{in}/N_H - V_o > 0\), \(i_{LR_1}\) and \(i_{LR_2}\) both increase linearly in this mode. The drain-to-source voltages \(v_{CQ2} = v_{CQ5} = V_{in}\), and the diode voltage \(v_{D2} = 2V_{in}/N_H\).

Mode 2 \([t_1, t_2]\): \(Q_1\) turns off at time \(t_1\). Due to \(i_{LR_1}\) being positive, \(i_{LR_1}\) discharges \(C_{Q2}\) from \(V_{in}\). If the inductor energy \((L_r + L_s + N_H^2 L_o) \dot{I}_{LR_1}^2\) at \(t_1\) is greater than the capacitor energy \(2C_{os} V_{in}^2\), then \(v_{CQ2}\) will be decreased to zero voltage at \(t_2\).

Mode 3 \([t_2, t_3]\): Since \(v_{CQ2}(t_2) = 0\) and \(i_{LR_1}(t_2) > 0\), the body diode \(D_{Q2}\) is forward biased. Thus, the leading-leg switch \(Q_5\) turns on at time \(t_2\) under zero voltage. In this mode, \(v_{ac} = 0\), and the primary winding and secondary winding voltages equal zero voltage. The diodes \(D_1\) and \(D_2\) both conduct so that \(v_{i,o} \leq -V_o\) and \(i_{io}\) is decreased.

Mode 4 \([t_3, t_4]\): At time \(t_3\), the lagging-leg switch \(Q_6\) turns off. \(i_{LR_1}(t_3)\) discharges \(C_{Q5}\) from \(V_{in}\). Since \(D_3\) and \(D_4\) still conduct, it can obtain \(v_{Lm1} = v_{Lm2} = 0\). If the energy \((L_r + L_s) \dot{I}_{LR_1}^2(t_3) > 2C_{os} V_{in}^2\), then \(V_{CQ5} = 0\) at the end of this mode.

Mode 5 \([t_4, t_5]\): At time \(t_4\), \(v_{CQ5} = 0\). \(i_{LR_1}(t_4) > 0\), and the body diode \(D_{Q5}\) conducts. The lagging-leg switch \(Q_5\) can be turned on at time \(t_4\) under zero voltage. Since \(v_{ac} = -V_{in}\) and \(v_{Lm1} = v_{Lm2} = 0\), \(i_{LR_1}\) is decreased. At \(t_5\), \(i_{D1}\) = 0. Then, the converter operation goes to the next half switching period.
4. Converter Characteristics and Design Considerations

According to the different turns-ratio of the transformer, the presented converter has three equivalent circuits. Three back-to-back MOSFETs are used in the presented circuit to have wide input voltage operation. Based on the flux balance on the output inductor, the load voltage is calculated in Equation (11).

\[
V_o = \begin{cases} 
2d_{\text{eff}} V_{\text{in}}(n_1 + n_2)/n_p, & V_{\text{in,min}} < V_{\text{in}} < 2V_{\text{in,min}} \\
4d_{\text{eff}} V_{\text{in}}/n_p, & 2V_{\text{in,min}} < V_{\text{in}} < 4V_{\text{in,min}} \\
d_{\text{eff}} V_{\text{in}}/n_p, & 4V_{\text{in,min}} < V_{\text{in}} < 8V_{\text{in,min}}
\end{cases}
\]

The average diode currents \(I_{D1} = \ldots = I_{D4} = I_o/2\). The voltage ratings of \(D_1 \sim D_4\) are \(V_{D1,\text{rating}} = V_{D2,\text{rating}} = (V_{\text{in,max}}n_1)/n_p\) and \(V_{D3,\text{rating}} = V_{D4,\text{rating}} = V_{\text{in,max}}(n_1 + n_2)/n_p\). The voltage ratings of \(Q_1 \sim Q_6\) and \(S_1 \sim S_3\) are \(V_{Q1,\text{rating}} = \ldots = V_{Q6,\text{rating}} = V_{\text{in,max}}, V_{S1,\text{rating}} = V_{\text{in,max}}n_2/(2n_p),\) and \(V_{S2,\text{rating}} = V_{\text{in,max}}n_1/2(2n_p).\) The average switch currents \(I_{S2,\text{av}} = I_{S2,\text{av}} = I_o\). If the maximum duty cycle loss in Equation (10) is given, then the maximum primary inductances \(L_{r1}\) and \(L_{r2}\) are derived as:

\[
L_{r1} = L_{r2} < n_p V_{\text{in,min}} d_{\text{loss},5,\text{max}} T_{\text{sw}} / 4n_3 I_o
\]

The inductance \(L_o\) is derived in Equation (13) under the maximum input voltage and minimum effective duty cycle.

\[
L_o = (V_{\text{in,max}} / N_H - V_o)d_{e,\text{min}} T_{\text{sw}} / \Delta i_{L_o} = V_o(0.5 - d_{e,\text{min}}) T_{\text{sw}} / \Delta i_{L_o}
\]

A 420 W prototype is illustrated as a design example to obtain the circuit parameters. The operating low input voltage range \(V_{\text{in,L}}\) is from 30 V to 60 V; the medium input voltage range \(V_{\text{in,M}}\) is from 60 V to 120 V; and the high voltage range \(V_{\text{in,H}}\) is from 120 V to 240 V. The output voltage \(V_o\) is 12 V. The PWM switching frequency of \(Q_1 - Q_6\) is 100 kHz. If 30 V \(\leq V_{\text{in}} < 60 V, S_1, S_2, Q_5,\) and \(Q_6\) are off and \(S_3\) is on. The voltage gain of the converter is \(G_L = 4d_{\text{eff}} n_{S1}/n_p.\) If 60 V \(\leq V_{\text{in}} < 120 V, S_2, Q_3,\) and \(Q_4\) are off and \(S_1\) and \(S_3\) are on. The voltage gain of the converter is \(G_M = 2d_{\text{eff}} n_{S1}/n_p.\) If 120 V \(\leq V_{\text{in}} < 240 V, S_3, Q_3,\) and \(Q_4\) are off and \(S_1\) and \(S_2\) are on. The voltage gain of the proposed circuit is \(G_H = d_{\text{eff}} n_{S1}/n_p.\) In order to prevent the control signal oscillation at the transition voltages 60 V and 120 V, the Schmitt trigger circuits with \(\pm 5 V\) voltage tolerance are used between three input voltage ranges. Thus, the actual voltage ranges are \(V_{\text{in,L}} = 30 V-65 V, V_{\text{in,M}} = 55 V-125 V,\) and \(V_{\text{in,H}} = 115 V-240 V.\) The circuit efficiency is assumed 90% at minimum input voltage and full road condition, and the maximum duty cycle \(d_{\text{max}}\) and maximum duty cycle loss \(d_{\text{loss},5,\text{max}}\) are assumed to be 0.45 and 0.15, respectively, at minimum input voltage. Therefore, the maximum effective duty cycle \(d_{\text{eff, max}} = d_{\text{max}} - d_{\text{loss},5,\text{max}} = 0.3.\) The primary inductances \(L_{r1}\) and \(L_{r2}\) can be estimated as:

\[
L_{r1} = L_{r2} = \eta V_{\text{in,min}}^2 d_{\text{loss},5} d_{\text{eff, max}} T_{\text{sw}} / 4P_o \approx 0.9 \mu H
\]

From Equation (11), the turns-ratio \(N_L\) is calculated as:

\[
N_L = n_p / 2n_{s1} = 2d_{\text{eff, max}} V_{\text{in,min}} / V_o \approx 1.5
\]

In the laboratory prototype, the primary and secondary turns of transformer \(T\) are \(n_p = 12\) and \(n_{s1} = n_{s2} = 4.\) The magnetizing inductances \(L_{m1} = L_{m2} = 820 \mu H.\) Under the low input voltage range, it can obtain the minimum effective duty cycle \(d_{\text{eff,min}}\) in Equation (16) at \(V_{\text{in}} = 65 V.\)

\[
d_{\text{eff,min}} = d_{\text{eff, max}} V_{\text{in,L, min}} / V_{\text{in,L,max}} \approx 0.14
\]
The assumed ripple current $\Delta i_{lo} = 3.5$ A (10% of the rated load current) at $V_{in,L,max} = 65$ V. The output inductance $L_o$ is obtained as:

$$L_o = \frac{d_{\text{eff}, \text{min}} T_{\text{sw}} (V_{in,L,max} / N_L - V_o)}{\Delta i_{lo}} \approx 17 \mu H$$

(17)

The output inductance $L_o = 20$ $\mu H$ is used in the prototype circuit. The maximum root-mean-squared (rms) currents of $Q_1$ – $Q_6$ are approximated as $I_{o,\text{rated}} / (n_L \eta \sqrt{2}) \approx 18$ A.

The maximum rating voltage of $Q_1$ – $Q_6$ is equal to $V_{in,max} = 240$ V. Therefore, the MOSFETs IXTN80N30L2 with the 300 V/80 A/30 m$\Omega$ rating are used for switches $Q_1$–$Q_6$ and $S_1$. The MOSFETs STD100N10F7 with 100 V/80 A/6.8 m$\Omega$ ratings are used for switches $S_2$ and $S_3$. The synchronous rectifiers MOSFETs IXFH80N25X3 with 250 V/80 A/16 m$\Omega$ ratings are used for diodes $D_1$–$D_4$ to further reduce conduction losses. The output capacitance $C_o = 470$ $\mu F/35V$. The PWM generator UCC3895 is used to provide the PWM waveforms for $Q_1$–$Q_6$. The voltage regulator TL431 is used to regulate load voltage. The Schmitt comparators and logic gates are used to produce the on/off signals of $S_1$–$S_3$. Figure 6 provides the control blocks in the prototype circuit.

**Figure 6.** Control block of the studied converter.

5. Experimental Verifications

The components of the prototype circuit were obtained in the previous section. The experimental results are verified in this section to demonstrate the converter effectiveness. Figure 7 demonstrates the test waveforms for low voltage operation. The PWM waveforms $v_{Q1,g}$ – $v_{Q4,g}$ at $V_{in} = 30$ V are provided in Figure 7a. The gate voltages of AC switches $S_1$–$S_3$ under $V_{in} = 30$ V are given in Figure 7b. One can observe that $S_1$ and $S_2$ are off and $S_3$ is on. Therefore, only the full-bridge converter with $Q_1$–$Q_4$ and diodes $D_3$ and $D_4$ are operated. Figure 7c provides the experimental results of $v_{ab}$ and $i_{Lr_1}$ under $V_{in} = 30$ V input. The secondary-side diode currents at $V_{in} = 30$ V are shown in Figure 7d. It can be obtained that $D_1$ and $D_2$ are in the off-state in the low input voltage operation. Similarly, the PWM waveforms $v_{Q1,g}$ – $v_{Q4,g}$, $v_{S1,g}$ – $v_{S3,g}$, $v_{ab}$, $i_{Lr_1}$, and $i_{D1}$ – $i_{D4}$ at $V_{in} = 63$ V input are demonstrated in Figure 7e–h. From the test results in Figure 7c,g, one can observe that the leg voltage $v_{ab}$ has a large
duty cycle at $V_{in} = 30$ V compared to $V_{in} = 63$ V. Therefore, the output inductor current $i_{Lp}$ has less ripple current $\Delta i_{Lp}$ at 30 V input voltage than 63 V input voltage. This large ripple current at 63 V input can be observed in $i_{Lr}$ in Figure 7g and $i_{D3}$ and $i_{D4}$ in Figure 7h. Figure 8 provides the measured waveforms of the converter for the medium voltage range operation and the rated power. For the medium input voltage range, $S_1$ and $S_3$ are conducting, $S_2$, $Q_3$, and $Q_4$ are turned off, and $D_1$ and $D_2$ are reverse biased. The gate voltages $v_{Q1,g}$, $v_{Q2,g}$, $v_{Q5,g}$, and $v_{Q6,g}$ are given in Figure 8a, and the gate voltages of $S_1$–$S_3$ are shown in Figure 8b under $V_{in} = 57$ V. The measured waveforms of $v_{ac}$, $i_{Lr}$, and $i_{D1} - i_{D4}$ are demonstrated in Figure 8c,d under $V_{in} = 57$ V. Similarly, the measured waveforms of $Q_1$, $Q_2$, $Q_5$, $Q_6$, $S_1$–$S_3$, $v_{ac}$, $i_{Lr}$, and $i_{D1} - i_{D4}$ are provided in Figure 8e–h under $V_{in} = 123$ V. The measured results for the high voltage range are provided in Figure 9. For the high voltage range operation, $S_1$ and $S_2$ are on, $S_3$ is off, PWM switches $Q_3$ and $Q_4$ are off, and $D_3$ and $D_4$ are off. The turns-ratio $2n_p/n_s$ of the transformer $T$ is operated in the high input voltage range. Figure 9a–d gives the test results of $Q_1$, $Q_2$, $Q_5$, $Q_6$, $S_1$–$S_3$, $v_{ac}$, $i_{Lr}$, and $i_{D1} - i_{D4}$ at $V_{in} = 117$ V. Similarly, the measured waveforms under $V_{in} = 240$ V are demonstrated in Figure 9e–h. The measured waveforms of $Q_1$ (leading-leg switch) are illustrated in Figure 10. From the test results in Figure 10, it is clear that the leading-leg switch $Q_1$ has the zero voltage switching turn-on characteristic from minimum to maximum input voltage and from 20% power to the rated power. Figure 11 gives the measured waveforms of $Q_3$ (lagging-leg switch) under 30 V input and 50% and 100% rated power. From Figure 11, it can be observed that $Q_3$ (lagging-leg switch) turns on under zero voltage from 50% rated power to full rated power. $Q_3$ and $Q_6$ are operated under medium and high input voltage ranges. Figure 12 gives the measured waveforms of $Q_5$ (lagging-leg switch) under $V_{in} = 240$ V and 50% and 100% rated power. One can observe that the leading-leg switch $Q_5$ turns on under zero voltage from 50% rated power to full rated power. Figure 13 demonstrates the measured efficiencies for different voltage ranges. Compared to the high input voltage range, the converter has large primary current and conduction losses under low input voltage range. Figure 14a gives the test results of the input voltage $V_{in}$ and the switching signals $v_{Q3,g}$ and $v_{Q4,g}$ between $V_{in} = 30$ V and $V_{in} = 80$ V under full load operation. When $30 V < V_{in} < 60$ V, the converter is operated in the low input voltage range. The switches $Q_3$ and $Q_4$ are activated, and switch $S_1$ is off. When $V_{in} > 60$ V and $< 80$ V, the converter is operated at the medium input voltage range. Therefore, $S_1$ is on, and $Q_3$ and $Q_4$ are off. Figure 14b provides the test results of $V_{in}$ and $S_2$ between $V_{in} = 65$ V and $V_{in} = 150$ V under full load operation. When $V_{in}$ is increased from 65 V and greater than 120 V, the switch $S_2$ is turned on. Then, the converter is operated under the high input voltage range. If the $V_{in}$ is decreased from 150 V and less than 120 V, the switch $S_2$ is turned off, and the converter is operated under the medium input voltage range. Figure 14c shows the test waveforms of input and output voltages under full load. The input voltage is varied between 30 V (low input voltage range) and 200 V (high input voltage range). It is obvious that the load voltage is stable at 12 V output voltage.
Figure 7. Measured results under the low voltage range and full load: (a) switch waveforms $v_{Q1g} \sim v_{Q4g}$ at $V_{in} = 30$ V, (b) AC switch waveforms $v_{S1g} \sim v_{S3g}$ at $V_{in} = 30$ V, (c) $v_{ab}$ and $i_{Lr1}$ at $V_{in} = 30$ V, (d) $i_{D1} \sim i_{D4}$ at $V_{in} = 30$ V, (e) switch waveforms $v_{Q1g} \sim v_{Q4g}$ at $V_{in} = 63$ V, (f) AC switch waveforms $v_{S1g} \sim v_{S3g}$ at $V_{in} = 63$ V, (g) $v_{ab}$ and $i_{Lr1}$ at $V_{in} = 63$ V, and (h) $i_{D1} \sim i_{D4}$ at $V_{in} = 63$ V.
Figure 8. Experimental waveforms under medium input voltage range and full load: (a) switch waveforms $v_{Q1g}$, $v_{Q2g}$, $v_{Q5g}$, and $v_{Q6g}$ at $V_{in} = 57$ V, (b) AC switch waveforms $v_{S1g}$, $v_{S3g}$ at $V_{in} = 57$ V, (c) $v_{ub}$ and $i_{Lr1}$ at $V_{in} = 57$ V, (d) $i_{D1} - i_{D4}$ at $V_{in} = 57$ V, (e) switch waveforms $v_{Q1g}$, $v_{Q2g}$, $v_{Q5g}$, and $v_{Q6g}$ at $V_{in} = 123$ V, (f) AC switch waveforms $v_{S1g}$, $v_{S3g}$ at $V_{in} = 123$ V, (g) $v_{ub}$ and $i_{Lr1}$ at $V_{in} = 123$ V, and (h) $i_{D1} - i_{D4}$ at $V_{in} = 123$ V.
Figure 9. Experimental waveforms under high input voltage range and full load: (a) switch waveforms $v_{Q1g}$, $v_{Q2g}$, $v_{Q5g}$, and $v_{Q6g}$ at $V_{in} = 117$ V, (b) AC switch waveforms $v_{S1g}$ to $v_{S3g}$ at $V_{in} = 117$ V, (c) $v_{ab}$ and $i_{Lr1}$ at $V_{in} = 117$ V, (d) $i_{D1}$ to $i_{D4}$ at $V_{in} = 117$ V, (e) switch waveforms $v_{Q1g}$, $v_{Q2g}$, $v_{Q5g}$, and $v_{Q6g}$ at $V_{in} = 240$ V, (f) AC switch waveforms $v_{S1g}$ to $v_{S3g}$ at $V_{in} = 240$ V, (g) $v_{ab}$ and $i_{Lr1}$ at $V_{in} = 240$ V, and (h) $i_{D1}$ to $i_{D4}$ at $V_{in} = 240$ V.
Figure 10. Experimental waveforms of $Q_1$ at (a) $V_{in} = 30$ V and 20% load, (b) $V_{in} = 30$ V and 100% load, (c) $V_{in} = 240$ V and 20% load, and (d) $V_{in} = 240$ V and 100% load.

Figure 11. Experimental waveforms of $Q_3$ at (a) $V_{in} = 30$ V and 50% load and (b) $V_{in} = 30$ V and 100% load.

Figure 12. Experimental waveforms of $Q_5$ at (a) $V_{in} = 240$ V and 50% load and (b) $V_{in} = 240$ V and 100% load.
Figure 13. Circuit efficiencies under (a) low voltage range ($V_{in} = 30\, \text{V} \sim 63\, \text{V}$), (b) medium voltage range ($V_{in} = 57\, \text{V} \sim 123\, \text{V}$), and (c) high voltage range ($V_{in} = 117\, \text{V} \sim 240\, \text{V}$).

Figure 14. Measured waveforms under full load (a) $V_{in}$, $v_{S1,g}$, $v_{Q3,g}$, $v_{Q4,g}$, (b) $V_{in}$, $v_{S2,g}$, and (c) $V_{in}$, $V_o$. 
6. Conclusions

To overcome the limited input voltage range operation of conventional PWM converters for solar power conversion, a novel three-leg PWM converter with an adjustable transformer turns-ratio was proposed and implemented to realize soft switching turn-on with wide input voltage operation. According to the input voltage range, the proposed three-leg converter had two equivalent circuits with variable primary winding turns on the input-side. On the secondary-side, the proposed converter also had two equivalent circuits by using variable secondary winding turns to achieve different voltage gains. Thus, the proposed three-leg converter had three equivalent circuits operated at different input voltage ranges to provide a stable DC output voltage. Each equivalent circuit using PWM operation could be operated to achieve 2:1 input voltage range operation. Thus, the proposed circuit could realize 8:1 ($V_{in,\text{in}} \sim 8V_{in,\text{min}}$) wide input voltage range operation. The Schmitt voltage comparators were adopted to generate the signals of the three voltage range selection. The proposed three-leg converter could work as the first stage of photovoltaic (PV) power converters with a wide range of voltage variation. Experiments from a laboratory prototype confirmed the theoretical converter characteristics with wide voltage range operation.

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