Hysteresis Behavior of the Donor–Acceptor-Type Ambipolar Semiconductor for Non-Volatile Memory Applications

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Abstract: Donor–acceptor-type organic semiconductor molecules are of great interest for potential organic field-effect transistor applications with ambipolar characteristics and non-volatile memory applications. Here, we synthesized an organic semiconductor, PDPP-TT, and directly utilized it in both field-effect transistor and non-volatile memory applications. As-synthesized PDPP-TT was simply spin-coated on a substrate for the device fabrication. The PDPP-TT based field-effect transistor showed ambipolar electrical transfer characteristics. Furthermore, a gold nanoparticle-embedded dielectric layer was used as a charge trapping layer for the non-volatile memory device applications. The non-volatile memory device showed clear memory window formation as applied gate voltage increases, and electrical stability was evaluated by performing retention and cycling tests. In summary, we demonstrate that a donor–acceptor-type organic semiconductor molecule shows great potential for ambipolar field-effect transistors and non-volatile memory device applications as an important class of materials.

Keywords: organic semiconductors; donor–acceptor-type molecules; ambipolar field-effect transistors; non-volatile memory; charge trapping

1. Introduction

Organic molecule-based electronic device applications are of great interest with a wide range of materials for selection and their great potential for use in transparent, flexible device applications in large scales and memory device applications due to their solution processability in large areas with high spatial uniformity on arbitrary substrates [1–7]. Among the material lists, semiconducting organic molecules have been more extensively investigated to apply as a channel material for organic field-effect transistors (OFETs). A general structure of the semiconducting organic molecules consists of electron-rich donor or electron-deficient acceptor blocks as a donor–acceptor-type semiconductor (e.g., thiophenes [8] and selenophenes [9] are in the type of electron-rich donors, and isoindigos [10,11], benzothiadiazoles [12], and naphthalene dicarboximide [13] are in the type of electron-deficient acceptors, respectively).

As one of the electron-deficient acceptor blocks, diketopyrrolopyrrole (DPP)-based polymers have been given more attention due to their relatively good electrical properties, including charge carrier mobilities compatible to 1 cm²/Vs [14–16]. The high carrier mobilities mainly originate from the strong π−π interactions between DPP moieties [17,18].
Additionally, such DPP-based semiconductors often exhibit ambipolar transfer characteristics due to their highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) levels being close to the Fermi level of OFET electrodes. Furthermore, DPP derivatives such as DPP-thieno(3,2-b)thiophene (PDPPT) have also been extensively studied due to their excellent solution processability and improved charge carrier mobilities for OFET applications [15,19,20].

In this paper, we report the synthesis of a DPP-based organic semiconductor, poly(2,5-(2-decyltetradecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno(3,2-b)thiophene)) (PDPPT-TT). The electrical characterizations of the PDPPT-TT based transistors were evaluated by the fabrication of OFETs with a spin-coated PDPPT-TT layer, which showed the ambipolar electrical characteristics with a hole mobility of 0.037 cm²/Vs. Additionally, this OFET exhibits the evolution of hysteresis loop window as the applied gate voltage sweep range increases for the potential in non-volatile memory device applications. However, the memory device performance was not ideal with the conventional OFET structure due to the shallow trap-induced short retention time. To improve the non-volatile memory device performance, including the stable retention time and cycling of programed/erased states, a gold nanoparticle (AuNP)-embedded dielectric layer was introduced as an efficient charge-trapping layer. The resulting AuNP-embedded dielectric layer incorporated PDPPT-TT-based OFETs, exhibiting optimized non-volatile memory performance with high stability.

2. Materials and Methods

2.1. Synthesis of PDPPT-TT

As a semiconducting channel material, we synthesized poly (2,5-(2-decyltetradecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno(3,2-b)thiophene)), or PDPPT-TT in short. In Figure 1a, the molecular structure of PDPPT-TT is illustrated with a highly planar well-conjugated polymer backbone. This polymeric semiconductor was synthesized followed by the sequence: (i) the synthesis of 3,6-Di(thiophen-2-yl)pyrrolo[3,4-c]pyrrole-1,4 (2H,5H)-dione (DBT-H) and 3,6-bis (5-bromothiophen-2-yl)-2,5-bis (2-decyltetradecyl) pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione (M-24) was followed from previous reports [15,19,20]; (ii) 0.1613 g of dibromo-DPP M-24, 0.07 g of 2,5-bis(trimethylstannyl)thieno(3,2-b)thiophene, and 3.7 mg of tri(o-tolyl)phosphine were mixed in a 50 mL dry flask. The dry flask was purged with ultra-high purity (UHP) Ar gas three times to remove the residual O2. In the mixture, 13 mL of anhydrous chlorobenzene and 2.8 mg of tris-(dibenzyldieneacetone)dipalladium(0) (Pd2dba3) were added and the mixture was stirred at 130 °C for 3 d in an Ar atmosphere. Then, the mixture was naturally cooled to room temperature and 0.5 mL of 2-bromothiophene was added. The mixture was heated to 130 °C for 2 h with stirring. Once the reaction was stopped, the mixture was cooled to room temperature again, and the resulting polymers were purified and filtered via precipitation in methanol. Lastly, ~150 mg of PDPPT-TT was obtained after Soxhlet extraction with acetone and hexane to remove the residual organic impurities and oligomers having low molecular weight, subsequent extraction with chloroform, and drying under high vacuum [14].

2.2. PDPPT-TT-Based Transistor Fabrication

A heavily doped 300 nm-thick SiO2/Si substrate was cleaned by dipping in a piranha solution for 30 min at 100 °C and rinsed with deionized water. To avoid the charge trapping at the interface between the SiO2 substrate and the PDPPT-TT channel due to the presence of the hydroxyl group, a self-assembled monolayer of octadecyltrichlorosilane (ODTS, purchased from Gelest Inc.) was formed on the SiO2 surface. After the ODTDs treatment, the semiconducting PDPPT-TT layer was formed on the substrate by spin-coating of a 0.2 wt.% solution in chloroform. The surface roughness of the PDPPT-TT layer was characterized by using atomic force microscopy (AFM), as shown in Figure 1a. The spin-
coated PDPPT-TT layer was dried for 24 h and annealed at 200 °C for 30 min in a vacuum chamber. Lastly, source and drain electrodes were formed on the PDPPT-TT layer by a thermal deposition of 50 nm-thick Au. To demonstrate non-volatile memory performance, gold nanoparticles (AuNPs) were introduced between the SiO₂ and the PDPPT-TT layer. A 1 nm-thick Au layer was thermally deposited and subsequently annealed at 100 °C for 10 min to form the AuNPs. Subsequently, a cross-linked poly (4-vinylphenol) (c-PVP) was formed by spin-coating PVP with a cross-linking agent, poly (melamine-co-formaldehyde) (PMF) in a weight ratio of 2:1, and the entire sample was annealed at 150 °C for 1 h. The fabricated devices were measured in a vacuum probe station (~10⁻⁶ Torr). The device structure is illustrated in Figure 1b.

![Molecular structure and atomic force microscopic image](image)

**Figure 1.** (a) Molecular structure of as-synthesized PDPPT-TT and atomic force microscopic image of as-coated PDPPT-TT layer; (b) schematic of the PDPPT-TT-based thin-film transistor containing c-PVP/AuNPs layers for non-volatile memory applications.

3. Results and Discussion

3.1. Electrical Properties of PDPPT-TT

The electrical properties of the semiconducting PDPPT-TT were characterized without incorporation of the c-PVP/AuNP layer (i.e., the PDPPT-TT layer prepared on the ODTSc-treated SiO₂/Si substrate) as shown in Figure 2a. Figure 2b shows transfer characteristics of the transistors with different gate voltage (Vg) sweep ranges from ±20 V to ±100 V with a step of 20 V. The PDPPT-TT-based transistor exhibited ambipolar behavior at a drain voltage (Vd) of ~1 V. During the forward and reverse bias sweeps, the formation of hysteresis loop motivated us to explore the memory device applications based on the organic semiconductor. The hysteresis behavior of the OFETs could originate from the charge transport in the PDPPT-TT layer or the charge trapping at the interface of the PDPPT-TT layer and the ODTS/substrate. Although the memory hysteresis loop was not observable at the Vg sweep from +20 to ~20 V (black symbols), the loop became more obvious as the Vg range increased from ±40 V (red symbols) to ±100 V (gray symbols). This trend of the hysteresis loop evolution with respect to the applied Vg range was summarized by plotting the threshold voltages (Vth) of each forward and reverse sweep direction; the memory window changes are determined by the Vth shift between the forward and reverse sweeps (Figure 2c). As described in the transfer characteristics, the memory windows described by the Vth difference between the forward and reverse sweeps were negligible with the sweep voltage range (|V|) of 20 V. However, the memory windows were clearly defined as the sweep voltage range increased from 40 to 100 V. By applying the |V| of 100 V, the retention time was evaluated to characterize the operation stability. As shown in Figure 2d, however, the memory performance of this device architecture was not ideal due to the shallow trap-induced charge leakage, resulting in the short retention time.
Figure 2. (a) Schematic of a PDPPT-TT-based transistor; (b) transfer characteristics of the device exhibiting ambipolar behavior; (c) summarized plot of the memory windows defined as the threshold voltages of forward and reverse biases; (d) retention time of the device with application of gate voltage of ±100 V.

3.2. Non-Volatile Memory Behavior of PDPPT-TT-Based Device

To demonstrate the organic semiconductor PDPPT-TT-based non-volatile memory behavior, a AuNP-embedded c-PVP layer was incorporated as a charge trapping layer in between the PDPPT-TT layer and the SiO₂ layer, as illustrated in Figure 3a. It is noted that the ODTs layer was not used for the non-volatile memory device applications due to the shallow trap which induced a relatively short retention time while the memory windows exceeded ~150 V (Figure S1). The transfer characteristics of the AuNP-incorporated PDPPT-TT device exhibited more obvious formation of the memory hysteresis loop (Figure 3b) as the Vc sweep range increased from 20 V to 100 V than those of device without the AuNP-embedded c-PVP layer. In comparison with the ambipolar transfer characteristics of the PDPPT-TT with a hole mobility of 0.037 cm²/Vs (Figure 2b), the AuNP-incorporated PDPPT-TT device showed a lower hole mobility of 0.023 cm²/Vs and negligible electron contributions (i.e., unipolar p-type transistor behavior). These mainly originated from an increased number of electron trap sites when the AuNP-embedded c-PVP layer was incorporated. Figure 3c exhibits the Vth of the forward and reverse biases with respect to the Vc sweep voltage range. In the range of ±20 V, the Vth difference, or the memory window, was almost negligible, similar to that of the device without the AuNP-embedded c-PVP layer. As the sweep voltage range increased to ±100 V, the Vth difference became more obvious up to ~70 V. To characterize the operational stability of the memory device, the retention and cycling tests were performed as shown in Figure 3d,e, respectively. In Figure 3d, the retention time was plotted after the various Vc was applied as 100 V (blue symbol), 60 V (green symbol), 40 V (red symbol), and −100 V (black symbol). Regardless of the applied Vc, the retention time exceeded 10⁴ s after the Vc was applied. As shown in Figure 3e, a cycling test was performed to demonstrate the operational stability of the programmed and erased states while the Vc was applied repeatedly with a switching speed of 1 s. Under the application of arbitrary Vc, the states were maintained after at least 50 cycles. These results indicate that the AuNP-embedded c-PVP layer-incorporated PDPPT-TT-based devices have non-volatile memory performances with good operational
stability and reversibility. To further elucidate the role of AuNPs, a control device geometry was fabricated, as shown in Figure S2. This geometry exhibits that the retention time is very short although the memory window was as large as ~150 V.

![Device Schematic](image)

**Figure 3.** (a) Schematic of a non-volatile memory device by incorporating the AuNP-embedded c-PVP layer; (b) transfer characteristics of the memory device with respect to the gate voltage sweep range; (c) summarized plot of the memory windows defined as the threshold voltages of forward and reverse biases; (d) retention time of the device with different applied gate voltages; (e) cycling test of the device (the read voltage as $V_C = 0$ V).

### 4. Conclusions

In this work, we have demonstrated successful synthesis of an organic semiconductor PDPPT-TT for non-volatile memory device applications. The electrical properties of the semiconducting PDPPT-TT were evaluated by fabricating field-effect transistors. It showed ambipolar transfer characteristics and increased hysteresis loop windows as the gate voltage sweep range increased. However, the retention time of the programmed and erased states was not ideal for the non-volatile memory device applications. To solve the issue, a AuNP-embedded c-PVP layer was incorporated as an efficient charge trapping layer in between an SiO$_2$/Si substrate and the semiconducting PDPPT-TT layer. The AuNP-embedded c-PVP layer-incorporated device showed unipolar transfer characteristics with negligible electron contributions due to a relatively larger number of the electron trapping sites; hence, the device exhibited an obvious memory window of ~70 V and the retention time of both programmed and erased states exceeded $10^4$ s with high repeatability once the controlled gate voltage was applied. This work provides a solution-processable organic semiconductor-based electrical device applications including ambipolar transistors and non-volatile memory devices.

**Supplementary Materials:** The following are available online at www.mdpi.com/2072-666X/12/3/301/s1, Figure S1: electrical characteristics of the device with the incorporation of OTIS and AuNP-embedded c-PVP layers, Figure S2: electrical properties of the device with the identical structure without AuNPs.

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**References**

1. Chua, L.L.; Zaumseil, J.; Chang, J.F.; Ou, E.C.W.; Ho, P.K.H.; Sirringhaus, H.; Friend, R.H. General observation of n-type field-effect behaviour in organic semiconductors. *Nature 2005*, *434*, 194–199.

2. Yan, H.; Chen, Z.H.; Zheng, Y.; Newman, C.; Quinn, J.R.; Dotz, F.; Kastler, M.; Facchetti, A. A high-mobility electron-transporting polymer for printed transistors. *Nature 2009*, *457*, 479.

3. Zaumseil, J.; Sirringhaus, H. Electron and ambipolar transport in organic field-effect transistors. *Chem. Rev. 2007*, *107*, 1296–1323.

4. Anthony, J.E.; Facchetti, A.; Heeney, M.; Marder, S.R.; Zhan, X.W. n-type organic semiconductors in organic electronics. *Adv. Mater. 2010*, *22*, 3876–3892.

5. Zhang, X.T.; Dong, H.L.; Hu, W.P. Organic semiconductor single crystals for electronics and photonics. *Adv. Mater. 2018*, *30*, 1801048.

6. Heremans, P. Semiconductor electronics-organic crystals at large. *Nature 2006*, *444*, 828.

7. Arias, A.C.; MacKenzie, J.D.; McCulloch, I.; Rivnay, J.; Salleo, A. Materials and applications for large area electronics: Solution-based approaches. *Chem. Rev. 2010*, *110*, 3–24.

8. Bronstein, H.; Chen, Z.Y.; Ashraf, R.S.; Zhang, W.M.; Du, J.P.; Durrant, J.R.; Tuladhar, P.S.; Song, K.; Watkins, S.E.; Geerts, Y.; et al. Thiieno[3,2-b]thiophene-Diketopyrrolopyrrole-containing polymers for high-performance organic field-effect transistors and organic photovoltaic devices. *J. Am. Chem. Soc. 2011*, *133*, 3272–3275.

9. Crouch, D.J.; Skabara, P.J.; Lohr, J.E.; McDouall, J.J.W.; Heeney, M.; McCulloch, I.; Sparrowe, D.; Shkunov, M.; Coles, S.J.; Horton, P.N.; et al. Thiophene and selenophene copolymers incorporating fluorinated phenylene units in the main chain: Synthesis, characterization, and application in organic field-effect transistors. *Chem. Mater. 2005*, *17*, 6567–6578.

10. Lei, T.; Cao, Y.; Zhou, X.; Peng, Y.; Bian, J.; Pei, J. Systematic investigation of isoidingo-based polymeric field-effect transistors: Design strategy and impact of polymer symmetry and backbone curvature. *Chem. Mater. 2012*, *24*, 1762–1770.

11. Mei, J.G.; Kim, D.H.; Ayzen, A.L.; Toney, M.F.; Bao, Z.A. Siloxane-terminated solubilizing side chains: Bringing conjugated polymer backbones closer and boosting hole mobilities in thin-film transistors. *J. Am. Chem. Soc. 2011*, *133*, 20130–20133.

12. Tsao, H.N.; Cho, D.M.; Park, I.; Hansen, M.R.; Mavrinskiy, A.; Yoon, D.Y.; Graf, R.; Pisula, W.; Spiess, H.W.; Mullen, K. Ultra-high mobility in polymer field-effect transistors by design. *J. Am. Chem. Soc. 2011*, *133*, 2605–2612.

13. Guo, X.G.; Kim, F.S.; Seger, M.J.; Jenekhe, S.A.; Watson, M.D. Naphthalene diimide-based polymer semiconductors: Synthesis, structure-property correlations, and n-channel and ambipolar field-effect transistors. *Chem. Mater. 2012*, *24*, 1434–1442.

14. Chen, S.Y.; Meng, Y.Z.; Li, Y.N.; Qu, B.; Zhou, D.X. Effect of the length and branching point of alkyl side chains on DPP-thieno[3,2-b]thiophene copolymers for organic thin-film transistors. *Org. Mater. 2019*, *88*, 500–507.

15. Kang, W.; Jung, M.; Cha, W.; Jang, S.; Yoon, Y.; Kim, H.; Son, H.J.; Lee, D.K.; Kim, B.; Cho, J.H. High crystalline dithienosilole-coated small molecule semiconductor for ambipolar transistor and nonvolatile memory. *ACS Appl. Mater. Inter. 2014*, *6*, 6589–6597.

16. Zhang, Y.; Kim, C.; Lin, J.; Nguyen, T.Q. Solution-processed ambipolar field-effect transistor based on diketopyrrolopyrrole functionalized with benzothiadiazole. *Adv. Funct. Mater. 2012*, *22*, 97–105.

17. Chen, H.Y.; Hou, J.H.; Hayden, A.E.; Yang, H.; Houk, K.N.; Yang, Y. Silicon atom substitution enhances interchain packing in a thiophene-based polymer system. *Adv. Mater. 2010*, *22*, 371.

18. Welch, G.C.; Bakus, R.C.; Teat, S.J.; Bazan, G.C. Impact of regiochemistry and isoelectronic bridgehead substitution on the molecular shape and bulk organization of narrow bandgap chromophores. *J. Am. Chem. Soc. 2013*, *135*, 2298–2305.

19. Li, Y.N.; Singh, S.P.; Sonar, P. A high mobility P-type DPP-Thieno[3,2-b]thiophene copolymer for organic thin-film transistors. *Adv. Mater. 2010*, *22*, 4862.

20. Sun, B.; Hong, W.; Aziz, H.; AbuKheir, N.M.; Li, Y.N. Dramatically enhanced molecular ordering and charge transport of a DPP-based polymer assisted by oligomers through antiplasticization. *J. Mater. Chem. C 2013*, *1*, 4423–4426.