CMOS-compatible Ising and Potts Annealing Using Single Photon Avalanche Diodes

William Whitehead, Zachary Nelson, Kerem Y. Camsari and Luke Theogarajan

1*Electrical & Computer Engineering Dept., University of California, Santa Barbara, CA, 93106, U.S.A.

*Corresponding author(s). E-mail(s): lusthe@ucsb.edu; Contributing authors: williamwhitehead@ucsb.edu; znelson@ucsb.edu; camsari@ucsb.edu;

Abstract
Massively parallel annealing processors may offer superior performance for a wide range of sampling and optimization problems. A key component dictating the size of these processors is the neuron update circuit, ideally implemented using special stochastic nanodevices. We leverage photon statistics using single photon avalanche diodes (SPADs) and temporal filtering to generate stochastic states. This method is a powerful alternative offering unique features not currently seen in annealing processors: the ability to continuously control the computational temperature and the seamless extension to the Potts model, a \( n \)-state generalization of the two-state Ising model. SPADs also offer a considerable practical advantage since they are readily manufacturable in current standard CMOS processes. As a first step towards realizing a CMOS SPAD-based annealer, we have designed Ising and Potts models driven by an array of discrete SPADs and show they accurately sample from their theoretical distributions.

Keywords: Ising Machine, Potts Model, SPAD, Boltzmann Machine

1 Introduction
Resource-intensive computing tasks are often off-loaded to specialized processors to accelerate execution. One such task is simulated annealing [1], a probabilistic method of finding solutions to hard optimization problems occurring in a variety of fields such as chip floor planning [2] and logistics [3]. These optimization problems typically require exploration over an exponentially large solution space in order to find acceptable answers, and simulated annealing prescribes an efficient probabilistic method of searching over this solution space but is computationally expensive. While simulated annealing may take many forms, current processors dedicated to the acceleration of simulated annealing have exclusively focused on the Ising model [4, 5]. The Ising model is preferred due to its simplicity, enabling easy emulation in hardware, and universality, since it can represent any discrete optimization problem [4]. Each variable is usually mapped directly to its own emulating circuit in an annealing processor to achieve the highest possible computational speed and efficiency [6–9]. This direct emulation is preferred over more sequential Ising model processor architectures [10, 11] usually designed for machine learning purposes, since optimization problems require substantial computation on relatively small graphs. Scaling the Ising model to large networks requires efficient design of the emulation circuit, commonly referred to as the neuron or spin.
There are multiple approaches to the problem of constructing simulated annealers [5], but no clear best method has emerged so far. Computationally, Ising machines require the multiply and accumulate operation for calculating the Hamiltonian (see equation 1), followed by calculating the probability of flipping the state, usually via the tangent hyperbolic function and a uniform random number generator. Proposed designs can be placed in several categories, including FPGA implementations, various ASICs, and novel device designs. Novel device designs leverage specific stochastic microelectronic devices to calculate the probability of a state flip by one small device. A prime example in this category is the use of magnetic tunnel junctions, which stochastically exist in one of two magnetization states with a probability tunable by a bias input [6]. Three-terminal memristors have been designed for similar operation [12], and a variety of devices have been used in other ways [13–15]. ASIC designs have been proposed based on both digital and analog methods. Digital CMOS annealers have reduced the size of individual neuron circuits through optimized digital design [16] and trading compactness for precision, such as reducing arithmetic to only a few bits and replacing hyperbolic tangent and random number generation with simpler circuits demonstrating random behavior [7, 8]. Analog computation is naturally able to pack complex functions such as hyperbolic tangent activation into simple circuits, but many analog circuit designs search for solutions using mean-field behavior rather than Gibbs sampling [17, 18]. FPGA Ising machine implementations often take advantage of the scale of modern FGPAIs and utilize efficient graph implementation techniques, such as sparsification [9].

The proposed SPAD-based design showcases a novel stochastic computational device offering the ability to be readily integrated with current CMOS technology. We present a method of using single-photon avalanche diodes (SPADs) as neuron circuits in simulated annealing processors, with a number of features unavailable in existing designs, such as the ability to simulate the Potts model in addition to the Ising model. We show results from a hardware realization of this approach and demonstrate its ability to reproduce the theoretical distribution via Gibbs sampling. The design consists of 8 Ising neurons or 4 Potts neurons implemented using a 4x4 silicon photon multiplier array (each element is an array of SPADs), see Figure 1. The variable rate SPAD circuit (VRSC) is the central element enabling the use of the SPAD as a stochastic element in an Ising or Potts model. Briefly, the random current pulses of the SPAD are converted into an amplitude via a filtering circuit and compared to a reference proportional to the computational energy of the network. The resulting pulse rate is proportional to the exponential of the negative computational energy (see section 2.2). The rate is subsequently converted into a state using a latching circuit yielding a stochastic node following Boltzmann statistics. In the next few sections following a brief introduction to the Ising and Potts models, we describe the architecture, theory of operation and discuss experimental results of our SPAD enabled Ising/Potts solvers.

1.1 Implementing Ising and Potts Models

Both Ising and Potts models allow the mapping of the NP complete problem class to a hardware structure capable of finding approximate solutions in polynomial time [4, 5, 19, 20]. A major difference between the Ising and Potts models is the representational ability of each neuron or spin. The Ising model utilizes binary valued neuron as opposed to the Potts model, which can be in one of $q$ possible states. Typically, the Potts neurons are represented by a one-hot encoded $q$-state vector. A central contribution of this work is to enable hardware realizations of the Potts model. The Potts model provides a more natural representation of many optimization problems making it more efficient in finding solutions [21–23]. Graph coloring with $q$ colors can be mapped directly to Potts model neurons with $q$ states, but mapping to the Ising model requires splitting each problem node across $q$ different Ising neurons [24]. However, this increase in representational ability comes at the expense of requiring more weights. Ising model requires single weights between each pair of neurons. Potts neurons on the other hand require $(q - 1)^2$ weights between each pair of neurons. Unlike the Ising model, where the weights encode the degree of (anti)correlation, each weight in the Potts model encodes the cost of each of $q^2$ possible joint neuron configurations.

The Ising and Potts models are best understood in the language of statistical mechanics [19, 20]. The collection of variables $\{n_1, ..., n_N\}$ in a system form a joint state $s$ with energy $E$. This energy depends on the interaction of the individual neuron states $n_i, n_j$ through the model weights $w_{ij}$. For the Ising
and Potts models, the energy of a state is defined as

\[ E_{\text{Ising}}(s = \{n_1, \ldots, n_N\}) = - \left( \frac{1}{2} \sum_{i=1}^{N} \sum_{j=1}^{N} w_{ij} n_i n_j + \sum_{i=1}^{N} h_i n_i \right) \]  

(1)

\[ E_{\text{Potts}}(s = \{n_1, \ldots, n_N\}) = - \left( \frac{1}{2} \sum_{i=1}^{N} \sum_{j=1}^{N} W_{i,j}(n_i, n_j) + \sum_{i=1}^{N} h_i(n_i) \right) \]  

(2)

The energy of the Potts model is also often expressed using the delta function formulation; the two forms are equivalent. As a statistical mechanical model, the energy determines the probability of each joint
state according to the Boltzmann distribution. While optimization algorithms based on Ising and Potts models need not produce a Boltzmann distribution, most are designed to do so in order to take advantage of the understanding conferred by statistical mechanical theory. In particular, when the energy of either an Ising or Potts model is the cost function of an optimization problem, the optimal solution is known to be the most likely solution (even if that probability is vanishing small). In addition, the Boltzmann distribution provides the concept of temperature, which is essential for the simulated annealing process. As with annealing of physical materials, slowly lowering the temperature allows the Ising or Potts model to settle into low energy configurations; as annealing to zero temperature is drawn out, the probability of the optimal state tends towards one [25]. In order for an Ising or Potts model to correctly sample from the Boltzmann distribution, state updates must conform to Gibbs sampling [26]. Gibbs sampling dictates that if neurons are updated sequentially (no linked neurons are updated at the same time) and each update is according to the conditional Boltzmann distribution, then the joint distribution will be the Boltzmann distribution. Alternative methods of finding solutions on Ising and Potts models that do not yield samples from the Boltzmann distribution but are nonetheless effective in some cases include mean-field approximations [21], deterministic evolution as in Hopfield neural networks [17], and inexact probabilistic updating [7, 8]. Although these annealing processors do not perform exact Gibbs sampling, their neuron update circuits consist of nearly the same set of computational stages as those required for Gibbs sampling.

The popularity of the Ising model stems from its relatively simple, hardware friendly, feed-forward structure. During an update there are only two possibilities (±1) to choose from, and therefore it is sufficient to only consider the difference in energy ΔE between the two states, and the probability of
being in one state or the other can be expressed compactly using the hyperbolic tangent function:

\[ P(n_i = +1) = \frac{1 + \tanh(-\Delta E/2T)}{2} \]

Randomly generating a $\pm 1$ state according to this distribution can be accomplished by simply comparing the calculated probability to a uniformly generated random number and latching the result. For exact sampling, conditionally dependent neurons must be updated on different clock cycles. However, this constraint is often relaxed in order to achieve a higher level of parallelism. This computational process, consisting of an energy sum, hyperbolic tangent activation, random number generation, comparison, and state latch is shown in figure (2). This design is a reference implementation of the Ising model which correctly samples from the Boltzmann distribution. In contrast, there is no equivalent design for Potts model neurons, since calculating a distribution and taking a random sample over many possibilities cannot be done so easily using feed-forward computational blocks. The hardware resource consumption of even the Ising neuron reference design becomes problematic when scaling to designs with thousands of neurons, a limitation prompting a great deal of interest in building efficient hardware implementations of Ising machines.

2 Results

The single-photon avalanche diode (SPAD) is at first glance a natural candidate for addressing some of the shortcomings of existing designs. SPADs are diodes biased beyond their reverse breakdown voltage, allowing amplification of single photons into detectable signals. Under constant dim illumination the random arrival of photons makes a SPAD a source of random events, a feature that can be used for making true random number generators [27, 28]. SPADs can also be currently integrated into CMOS with no process modifications, and are frequently designed into chips for imaging [29, 30]. The random behavior of a SPAD makes it appear to be another device around which compact neuron-update circuits can be built, similar to magnetic tunnel junctions and memristors, but with the added benefit of being implementable in a standard CMOS process. However unlike MTJs and memristors, SPADs contribute random events, not a random state, and therefore must be used slightly differently. SPADs could be incorporated simply as random number generators, by replacing the RNG block in the standard Ising neuron design with a SPAD random number generator [27, 28]. However these random number generators require a lot of additional circuity, and from the standpoint of scaling down the area of individual neurons, this use of SPADs provides no benefits. Instead we demonstrate a better method of using SPADs that turns the random events into an advantage and places the SPADs in a more central role.

Our proposed SPAD-based annealing design relies on two key design ideas, and provides a set of features unseen in any other annealing processor design. The first design feature is the coupling of SPAD pulses to a latch, bridging the worlds of random events and random states. The second is the construction of variable-rate SPAD circuits, which are SPAD-based circuits producing pulses (events) with a Poisson distribution and an input dependent mean frequency. When combined, these two functions emulate a continuous-time Markov chain (CTMC), lending the name SPAD CTMC neurons. A SPAD CTMC neuron may function just as a magnetic tunnel junction or three-terminal memristor: it has a stochastic output state whose distribution is controlled by an analog input. In addition to presenting this functionality for Ising neurons, a SPAD CTMC neuron can also be constructed with more than two states, enabling the emulation of the Potts model with large $q$. While annealing designs for the Potts model have been proposed before, none are as practical or as capable as the proposed SPAD-based design. Hybrid approaches for annealing Potts models on Ising hardware have been described [23, 31, 32], but introduce significant overhead and do not fundamentally operate as Potts models; a theoretical proposal to use Bose-Einstein condensate [33] is a discretization of the XY model that is not capable of encoding typical optimization problems. The SPAD CTMC neuron also allows for tuning the effective temperature of the Boltzmann distribution: temperature may be controlled by setting the illumination and bias conditions of the SPADs. In the remainder of this paper we explain and demonstrate all of these features.
Fig. 3: Proposed circuits for Ising (a, b, e) and Potts (c, d, f) model computation. Analog energy sums $E$ (which may be calculated in any way) control the rate at which variable-rate SPAD circuits (VRSCs) produce random events which in turn controls how much time the output latches spend in any one state. The system is best modeled as continuous-time finite state Markov chains (e, f). The rate at which the FSM transitions to a state (regardless of starting state) is the rate at which the associated SPAD circuit produces events.

2.1 SPAD CTMC neuron architecture

The architecture of SPAD CTMC neurons is best understood if the design of variable-rate SPAD circuits is considered separately. The operation of both Ising and Potts neurons starts with the calculation of conditional energies for each possible state, as shown in the figure 2. The multiply-accumulate (MAC) calculation required for this step may be done in many ways but is most compactly performed in the current domain, either using digital weights [34] or memristive analog weights; since SPAD CTMC neurons are designed for CMOS integration, charge-trapped transistors (CTTs) [35] would be a good choice since they are also CMOS devices. Once analog signals representing energy are calculated, they are used to control the variable-rate SPAD circuits. Lower calculated energy (indicating a more favorable
state) causes a variable-rate SPAD circuit to produce pulses more often. At this stage the design of Ising and Potts neurons differentiates.

A neuron in the Ising model consists of two variable-rate SPAD circuits and an RS latch, configured as in figure 3a. When a SPAD circuit produces a pulse, the neuron transitions to a state corresponding to the respective SPAD. The distribution of the neuron’s state is controlled by the relative rate with which the two SPADs trigger. If the SPADs trigger at the same rate, the neuron will spend equal time in the +1 and −1 states, regardless of the common mode event rate. Changing the distribution requires adjusting the event rate of one or both SPADs. Figure 3a shows a symmetric solution in this regard, with the two SPADs adjusted in opposite directions, based on a single differential input sum representing the energy difference between the two states. Natural variability in the SPAD event rate can be compensated for using a bias term, but does not present an overhead since it is a necessary term to encode optimization problems in the Ising model. If two biases are included, one for each variable-rate SPAD as in figure 3a, the common-mode event rate may be controlled independently as well. This may or may not be needed in a design since small variations in the common mode rate between neurons in a network do not affect the statistical operation of the annealer. However, the overall rate must be set low enough such that neuron state updates have time to propagate to other neurons before the next event. Alternative energy sum arrangements to achieve the Ising model are also possible. For example, arranging the weights as in the $q = 2$ Potts model would obviously work, however the single differential energy sum method described here takes advantage of the simplifications possible in the Ising case, allowing more compact circuits than $q = 2$ Potts model neurons.

The circuit for the Potts model, shown in figure 3c, requires individual sums and SPADs for each possible state, and requires more complex latching circuitry (see supplementary material). The behavior is similar to the Ising model where each SPAD attracts the neuron state to its index when it produces an event. The probability of each state is controlled by the relative event rates of the SPADs, which in turn are controlled by energy sums. The event-based nature of the SPAD seamlessly lends itself to constructing this design. Since a simple RS-latch will no longer maintain a one-hot neuron state between SPAD events, a new latching design is required. Similar in spirit to winner-take-all circuits [36], one of the $q$ latch outputs needs to be active at any time, and needs to indicate which SPAD circuit most recently pulsed. A potential design outlined in figure 3c uses a lateral message-passing design where any element that is ‘set’ will simultaneously pass a ‘reset’ signal to all other elements through a daisy-chain. While this design creates a delay proportional to the number of stages through which the message must be passed, it has the benefit of having $O(N)$ complexity and may be partitioned. A string of 20 connected elements could for instance be arranged as a single $q = 20$ neuron, or as four $q = 5$ neurons, allowing for versatile hardware. A logical implementation of this latch is available in the supplementary material. Using this SPAD CTMC neuron architecture, it is possible to build an annealing processor with configurable neuron dimensionality $q$ with similar complexity as Ising annealing processors. The proposed approach is widely applicable beyond SPAD based neurons.

2.2 Theory of Operation

The operation of each individual neuron is best modeled as a continuous-time Markov chain, since the latching circuit in SPAD CTMC neurons is a finite state machine transitioning randomly each time a variable-rate SPAD pulses. Each neuron is naturally modeled as a CTMC since Boltzmann machines are known to be Markov random fields. While the following analysis is tailored to the Potts notation it is equally applicable to the operation of Ising nodes. As long as the pulse timing is memoryless, then the pulse rates are a sufficient description of how the CTMC neurons transition between states. The transition rate from state $i$ to state $j$ is the event rate of SPAD $j$, since each SPAD attracts the neuron state to itself regardless of the prior neuron state. The balance equation, which equates the rate $r_j$ at which a state is entered to the rate $\sum_{j \neq i} r_j$ at which a state is left, is used to find the probability $P_i$ of state $i$ in this CTMC and can be written as follows:

$$P_i \sum_{j \neq i} r_j = (1 - P_i) r_i$$  \hspace{1cm} (4)
Which is easily manipulated into the form,
\[ P_i = \frac{r_i}{\sum_{j=1}^q r_j} \tag{5} \]

The probability of each state in the CTMC now has a similar form to that required by Gibbs sampling. In Gibbs sampling each time the neuron \( n_i \) updates it must select from its allowed states according to the energy \( E_Q \) of each state \( Q \), conditioned on the rest of the network \( \{ n_j : j \neq i \} \):
\[ P(n_i = Q) = \frac{e^{-E_Q/T}}{\sum_{Q'} e^{-E_{Q'}/T}} \tag{6} \]

Therefore, in order for the CTMC to sample from the Boltzmann distribution, the transition rate \( r_Q \) must be equal to the exponential of the state's energy,
\[ r_Q = e^{-E_Q/T} \tag{7} \]

If the event rate of a SPAD is an exponential function of some energy-representing control input, the Ising or Potts machine will correctly sample from the Boltzmann distribution. The remaining challenge is constructing a variable rate SPAD circuit achieving this exponential transfer function.

2.3 Variable-rate SPAD circuits

SPADs have two physical controls for their detection rate, and further control over their effective detection rate can be created by filtering circuits. The first physical control is the illumination incident upon the SPAD, which provides a large dynamic range for how often the SPAD triggers; the second is the reverse bias of the SPAD, which can tune the dark count rate and the photon detection efficiency [37]. Since illumination can easily be controlled across an entire chip but not locally, it is suitable for temperature control but not for controlling the rate of individual SPADs. Controlling the reverse bias can be done for each SPAD individually, but the effect of changing the SPAD bias is dependent on the exact SPAD design; some SPAD designs demonstrate bias effects exponentially altering the dark count rate [38], while others do not [39]. For these reasons a filtering and comparison circuit, shown in figure 4, is used for the current design instead. By filtering the output of a SPAD on a time scale close to the SPAD’s avalanche rate, the filtered output \( V_{\text{random}} \) or \( I_{\text{random}} \) continues to pulse at each photon detection but with a magnitude that is now variable, depending on the history of SPAD avalanches. The variable-height pulses can then be compared to a threshold, yielding a decreasing detected pulse rate as the threshold is increased. Whether or not the resulting detected pulse rate is suitable for construction of a CTMC neuron depends on the distribution of the random filtered signal, which in general is hard to predict exactly, especially if there is nonlinear filtering. One tractable scenario is the limit as the filtering timescale \( \tau_f \) becomes much longer than the photon arrival timescale \( \tau_p \). In this case the sum of pulses may be simply treated as an infinite sum of random variables, and the central limit theorem indicates the filtered signal will be Gaussian. Since thresholding integrates the tail of the filtered distribution, the threshold to pulse rate transfer function will be proportional to the complementary error function, \( r \propto \text{erfc}(E/T') \). While not the desired transfer function, it may still be used as a rough approximation to an exponential transfer function. Fortunately, experimental and simulated results show when \( \tau_p \approx \tau_f \) this filtering concept can yield the exponential transfer function required by equation 7, and the interval between detected pulses is still nearly a Poisson process as required by the CTMC analysis.

We simulated a CMOS version of the filtered SPAD design based on a model of SPADs in a CMOS process [40]. The SPAD model produces avalanches of identical magnitude which when processed by a Gm-C filter, as shown in figure 4b, produces an exponential distribution of current pulses. A sample of the filtered pulses is shown in figure 4d, and the threshold-rate transfer function is shown in figure 4g. This design is provided as an example, and there are undoubtedly other filtering methods capable of yielding an exponential distribution of pulse heights.

Our experimental variable rate event generators operate on another implementation of the filtering principle. Due to sourcing constraints, we physically realized variable rate event generation using silicon
Fig. 4: Design of variable-rate SPAD circuits. Two designs are shown, an experimental design (a) made of discrete components for which we have measured results and a simulated design (b) meant to establish that the variable-rate behavior is not dependent on the specific characteristics of SiPMs. For both designs, the pulse rate can be controlled with an exponential transfer function (e, g) in accordance to equation 7 and the interval between pulses is shown to be an exponential (f, h), a defining feature of Poisson processes.

photonmultipliers (SiPMs) rather than SPADs. As an array of SPADs, SiPMs perform the same key function but have additional behaviors, such as some built-in filtering and the possibility of simultaneous avalanches. Despite these differences, a SiPM is not fundamentally different from a single SPAD if filtering is involved. Our experimental SiPM circuit, including internal SiPM filtering elements, is shown in figure 4a. This circuit was found to have a sufficiently exponential transfer function under a range of SPAD bias and illumination conditions, with a few cases shown in figure 5a. At high illumination the transfer function looks less like an exponential and more like the tail of a complementary error function, as expected when the SPAD avalanche rate becomes much faster than the filtering time constant; nonetheless, the exponential is still a close fit and under high illumination the Ising and Potts models still produce
Fig. 5: Control and uniformity of variable-rate SPAD circuit transfer functions. (a) The slope of the transfer function can be controlled by the bias voltage $V$ and the illumination $I$. At high illumination, the transfer functions fit the complimentary error function better than an exponential. (b) The transfer functions of the 16 variable rate SPADs in the test setup, showing threshold variation but identical slopes.

accurate statistics. Another key feature visible in figure 5a is the variation in the transfer function slope as the illumination and bias are changed, which allows the computational temperature of an Ising or Potts model to be easily controlled in real time. Unlike many current designs the model weights do not need to be reconfigured. While the transfer function slopes of each SPAD can be easily controlled, they are also quite stable between SPAD circuits under the same operating conditions. Figure 5b shows a simple offset term can match the 16 different experimental variable-rate SPAD circuits.

2.4 Experimental Demonstrations

The first step in assembling the Ising and Potts models is calibration of individual neurons, which in the Ising case can be verified by comparing the transfer function of each neuron to equation 3. Calibration serves to compensate for differences in slope and offset in the exponential transfer functions of each variable-rate SPAD, although for our experimental variable rate event generators, slope compensation was not needed since the slopes of the transfer functions in figure 5b are all nearly the same. Calibration is performed for each SPAD circuit individually. A target event rate is picked, and for each SPAD the energy bias yielding that event rate is determined to be the zero operating point for that SPAD circuit. When assembled into Ising neurons, the calibration and the performance of the CTMC neuron as a whole is verified by measuring the neuron’s transfer function. The differential energy sum is treated as an input, and the probability with which the neuron is in its +1 state is treated as an output. Most proposed stochastic bit designs are evaluated this way [6, 12]. Since the output of the neuron transfer function is a probability, it is measured by averaging many states as the input energy is held constant, and the input is then changed and the procedure is repeated. Figure 6a shows the measured transfer function for eight Ising nodes, constructed out of an array of 16 variable rate SiPM circuits. Transfer functions are shown for four combinations of illumination and SPAD bias, which manifests as different computational temperatures (tanh slopes). While the variable rate SPAD circuit produces a complementary error function transfer function under high illumination rather than an exponential, the Ising model transfer function is still accurate showing the high resilience of the CTMC architecture to imperfections. Fits of equation 3 are included for each illumination condition, which also yields the computational temperature which we later use to generate matching theoretical distributions for evaluation of full Ising and Potts models. Unfortunately no similar, simple verification applies to Potts model neurons, but the quality of both Ising and Potts neurons is demonstrated indirectly by the performance of the complete models.
(a) Ising neuron probabilities

(b) Probabilities of a model with random weights

(c) Annealing in the Ising model

(d) Implementation

Fig. 6: Experimental methods (d) and measured results. SPAD CTMC neurons demonstrate highly accurate statistical behavior, both at the level of individual Ising neurons (a) and when used to form complete Ising and Potts Boltzmann machines (b). (c) Annealing can be easily controlled by adjusting the illumination on the SPADs.

The complete Ising and Potts machines comprise an FPGA portion and a custom PCB portion, shown in figure 6d. This arrangement is similar to that used in other demonstrations [6, 12]. The FPGA takes SPAD pulses as inputs, implements the latching circuits, digitally calculates energy summations, and writes the energy summations back to the variable rate SPAD circuits as an analog value using digital to analog converters. The custom PCB has a 4x4 array of SiPMs which are coupled to 16 comparators, yielding 16 variable-rate SPAD circuits. Since latching is performed in the FPGA and is programmable, we use the 16 variable-rate SPAD circuits to demonstrate fully-connected networks of either eight Ising nodes or four \( q = 4 \) Potts nodes. Other configurations are also possible using the same hardware. Since the number of states is small, the statistical correctness of the models can be directly established. We chose to work with arbitrary models with random weights, which is the most straightforward way to use all available neurons and weights. In this case the interaction between neurons is maximized so that any issues in statistical sampling are more likely to appear. Furthermore, since the number of states \( 2^8 = 4^4 = 256 \) in the Ising demonstration and the Potts demonstration are the same, the Ising and Potts models can be configured to sample from the same distribution which allows comparison to each other as well as to the ideal theoretical Boltzmann distribution. First weights and biases for the Ising model are selected uniformly from the integers on \([-8, 8]\), and then the Ising model weights are converted to equivalent Potts model weights (see supplementary material). For a given set of SPAD illumination and
bias conditions, the theoretical Boltzmann distribution is calculated from the Ising network weights and the computational temperature found in figure 6a. Five million samples each are measured from the Ising and Potts machines to determine the experimental distributions. Figure 6b compares calculated, Ising, and Potts distributions at two different temperatures, all with the same set of random weights. To illustrate that the Ising and Potts models sample from a Boltzmann distribution, each of the 256 states are plotted according to their energy and measured probability, fitting to a straight line on a logarithmic plot. In this format it is easy to tell that the SPAD CTMC Ising and Potts models match the desired distribution, achieving a Kullback-Leibler divergence of 0.01. While states are not sampled exactly as often as they should be, any significant difference in energy between states is reflected in their probability and the lowest energy states are universally the most probable. This statistical correctness establishes that SPAD CTMC neurons will be able to find the lowest energy configuration of any real-world problem.

The computational temperature of SPAD CTMC neurons can be controlled continuously using several methods, including changing the illumination on the SPADs. Normally, a gradual decrease in computational temperature allows an annealing processor to gradually settle into a single low energy state. Our SiPM CTMC neurons allow a factor of two temperature change in response to illumination, however since the demonstration network is limited to eight Ising neurons or four Potts neurons, the model does not lock into a single state at the lower temperature, and the lowest energy state can easily be reached even during sampling at higher temperatures. Nonetheless, by gradually decreasing the illumination and thus the computational temperature, the average energy that the model samples from can be seen to decrease. Figure 6c shows the energy and time-averaged energy of the sampled states during the annealing schedule defined by the illumination, demonstrating the inherent annealing capability of SPAD CTMC neurons. In contrast to the distribution measurements taken at different temperatures, during annealing the CTMC neurons can only be calibrated once for a single temperature; fortunately the calibration is roughly applicable across temperatures. However, there are some limitations, such as an inability to approach zero computational temperature. In addition it can be difficult to independently control the temperature and the mean event rate of the SPADs. However, as an analog neuron, the temperature of the SPAD CTMC neuron may be controlled by other methods as well such as a global analog weight scaling factor. Regardless of the exact design, there are several simple temperature control options when using SPAD CTMC neurons that can be applied continuously without pausing the operation of the annealing processor.

3 Discussion

A proof-of-concept for using single-photon avalanche diodes (SPADs) as the main computational element in annealing processors has been presented. Since SPADs produce random events rather than random states, they must be coupled to latching circuitry to form Ising and Potts nodes. The resulting circuits form stochastic finite state machines whose state is a continuous-time Markov chain (CTMC). While this is schematically more complex than other proposed designs for hardware Ising nodes, it allows for much better control over the behavior of each node and is the key enabler of Potts model annealing in addition to the usual Ising model annealing. SPAD CTMC neurons are additionally compatible with CMOS fabrication processes and offer many options for temperature control. CMOS integration requires a few considerations since SPAD designs have been mainly optimized for imaging applications which have different constraints compared to annealing processors. A prime example is the dark count rate which needs to be relatively low for imagers but not for annealing processors, relaxing some of the design constraints for CTMC SPAD neurons and improving scaling[41]. One area of future work is re-imagining the Annealing processor architecture to make effective use of the Potts model, since the weight configuration options for the Potts model are far greater than for the Ising model. When these issues are addressed, annealing processors based on SPAD CTMC neurons will be able to solve more complex optimization problems than current annealing processors do, via both scaling to a greater number of nodes and the step improvement in representational ability bestowed by the Potts model.
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CMOS compatible Ising and Potts annealing using single-photon avalanche diodes: Supplementary material

William Whitehead, Zachary Nelson, Kerem Camsari, Luke Theogarajan
1 Scalable one-hot latching circuit

The one-hot latch required for Potts model CTMC neurons can be implemented as in figure S1. This circuit is composed of a chain of repeating elements (blue rectangle; two are shown). Each circuit has a pulse input that when high, sends an ‘inhibition’ signal cascading through all connected elements which sets the output of all elements to zero. Meanwhile, the output of the latching element with the pulse input is set to high (and sees no inhibition signal); thus for \( q \) connected elements, one will always have a high output and the rest will have low outputs. Additionally, each element can come equipped with a configuration input that can block or pass the inhibition inputs. When the inhibition signals can pass, the two adjacent elements (and their corresponding variable-rate SPADs) competitively participate as a single Potts node; when the inhibition signals are blocked, the two adjacent elements (and all elements to each side) do not compete; this can effectively convert a string of \( q \) latching elements into two strings of smaller size. In this way a bank of SPADs and latching elements may be configured into any number of CTMC neural configurations, allowing a single Potts annealer to operate with any combination of Potts model node sizes.

As an asynchronous circuit with potentially many stages of gates, two concerns arise regarding timing: the behavior under coincident pulse inputs and effects on the annealing algorithm as the latch is transitioning and the one-hot constraint is momentarily not met. In the first case, near-coincident pulse inputs have the capability to leave the one-hot latch with no high outputs. This would occur if the falling edges of two pulses were coincident, leaving an inhibitory signal in all elements but no excitation signals. Since pulse events are stochastic by design, it is inevitable that this will happen sometimes. Similarly, delay in the inhibitory signal means that there will usually be brief instances during a normal transition during which multiple outputs are hot. Both of these phenomena will be felt at the algorithmic level as intermittent inaccuracy of the energy calculations, which may or may not be problematic depending on the optimization problem. In general however the incorrect energy calculation will be minimal: if a CTMC neuron changes state at roughly 100 MHz, and the delay through each latching stage is only 10 or 20 ps, a \( q = 10 \) latch would be 100x faster than its input and would spend a similarly small portion of time in an incorrect state.
2 Mapping an Ising model to a Potts model

During testing we matched a single theoretical distribution to the samples from both the Ising and Potts Boltzmann machines. This required mapping from an eight-neuron Ising model to a Potts model with four four-state neurons. Ising states, biases, and weights will be denoted as $I_n$, $I_h$, and $I_w$ respectively; the Potts states, biases, and weights will be $P_n$, $P_h$, and $P_w$. Each state of each Potts neuron is assigned a pair of states from two Ising neurons, shown in table S1. The bias of each Potts state is the energy that state represents intrinsically, without interacting with other neurons in the Potts model; it includes the biases of the two Ising neurons that it is representing, and also the interaction energy between those two Ising neurons since they are subsumed within the single Potts neuron, also shown in table S1.

| $P_n_i$ | $I_{n_{2i-1}}$ | $I_{n_{2i}}$ | $P_h_i(P_n_i)$ |
|---------|----------------|--------------|----------------|
| 1       | -1             | -1           | $-I_{h_{2i-1}} + I_{w_{2i-1,2i}}$ |
| 2       | -1             | +1           | $-I_{h_{2i-1}} + I_{h_{2i}} - I_{w_{2i-1,2i}}$ |
| 3       | +1             | -1           | $+I_{h_{2i-1}} - I_{h_{2i}} - I_{w_{2i-1,2i}}$ |
| 4       | +1             | +1           | $+I_{h_{2i-1}} + I_{h_{2i}} + I_{w_{2i-1,2i}}$ |

Table S1: Defining one Potts neuron based on two Ising neurons.

Since a weight between two Potts neurons represents the interaction between four Ising neurons, there are four Ising weights that each Potts weight must account for (the two additional Ising weights found in a network of four Ising neurons are accounted for in the biases in table S1). Thus when mapping from the Ising model to the Potts model, each Potts weight is based on four terms,

$$P_{w_{i,j}}(P_i, P_j) = \pm I_{w_{2i-1,2j-1}} \pm I_{w_{2i-1,2j}} \pm I_{w_{2i,2j-1}} \pm I_{w_{2i,2j}}$$

(1)

The sign of each term is determined by the corresponding signs of $I_{n_{2i-1}}$, $I_{n_{2i}}$, $I_{n_{2j-1}}$ and $I_{n_{2j}}$. There are 16 combinations of signs, and 16 weight values connecting Potts neurons $i$ and $j$. 


3 Hardware Implementation

All experimental data demonstrating SPAD CTMC neurons was collected using the hardware setup shown in figure S2. The setup consisted of 16 variable-rate SPAD circuits implemented on a custom PCB and an FPGA development board (Zedboard). Asynchronous pulses from the variable rate SPADs (ON Semi ARRAYJ-30020-16P-PCB, using 16x LMH6629 for transimpedance sense amplifiers) were captured by the FPGA and used to control either binary RS latches (forming Ising neurons) or four-way latches (forming Potts neurons). The latch states controlled adder trees inside the FPGA which calculated values (energies) to be written to the DAC of each variable-rate SPAD. Due to the evolutionary nature of research, the DACs exist on an add-on PCB attached to the back of the main PCB. Each time one of the neural state latches changed, all 16 DACs were updated; since the DACs could only be written over a serial interface (4x AD7226; 8-bit parallel, 50 MHz, 16 cycles to update all 16 DAC outputs), SPAD pulses were ignored until the DAC update completed in order to maintain correct sampling statistics. In a scaled CMOS implementation, this delay would not be present. The DACs set the thresholds on comparators (16x MAX40026) in each variable-rate circuit, affecting the pulse rate of each SPAD and in turn controlling the distribution of latch states held in the FPGA, forming a Boltzmann machine. The behavior of this system was studied using the accompanying processor on the Zedboard’s ZYNQ 7020 SoC, which ran Ubuntu with the PYNQ software layer, allowing fast collection of large quantities of data from a Jupyter Notebooks interface. Illumination of the SiPM array was controlled by driving an LED with a DAC; the LED light was attenuated before reaching the SiPMs, and the scale of the illumination intensity was not measured. Thus the illumination intensity is only reported in arbitrary units (corresponding to the value set on the DAC).
4 Sampling methods

Many measurements of the behavior of CTMC neurons, from the transfer function of single variable-rate SPADs to distributions of complete Ising and Potts annealers, required statistical sampling. In general enough samples were accumulated such that deviations from ideal behavior could be attributed to the system itself rather than the distribution of the sample mean.

4.1 Variable-rate SPAD transfer functions

Two different sampling methods were used to measure the threshold-to-pulse-rate transfer functions of variable rate SPADs; both methods gave the same results. The first method, which was only applied to the experimental variable-rate SPAD circuits, was to directly count the pulse edges received from the comparators by the FPGA. In this case a threshold was physically set using the DACs and the resulting pulse edges were counted over a 100 ms time period by the FPGA; this was done iteratively over the full range of the 8-bit DACs, yielding 256-point transfer functions.

The second method was a computational analysis of the filtered SPAD outputs shown in figures (xx), obtained either from simulation or directly measured from the transimpedence amplifier using an oscilloscope. In this method the comparator component of the variable-rate SPADs was performed computationally: using a single trace, positive crossings of a set threshold were counted, and the threshold was iteratively set to different values to measure a transfer function. Performing this measurement on raw traces yielded higher event rates than (but the same exponential relationship as) the first method; this discrepancy was due to high-frequency sequential threshold crossings that were filtered out by the actual hardware. Performing a low-pass filtering operation before computationally measuring the variable-rate SPAD transfer functions brought the magnitude of the rates in line with those obtained directly from hardware.

The computational approach to measuring transfer functions was required especially for the simulation circuit results. Otherwise a few hundred nearly identical simulations, each with a different threshold, would have been required; this would have been computationally prohibitive. Instead computational time was spent on simulating a longer single trace, so that the tail of the transfer function could be measured with greater accuracy.

Table S2 lists measurement conditions and associated sampling uncertainty for the various variable-rate SPAD transfer function measurements. The uncertainty depends on how many pulses were recorded during the sampling period, with higher pulse rates resulting in lower uncertainty. The table lists the lowest measured pulse rates and associated number of detected pulses, from which a worst-case relative measurement error is determined. The measurement quantity (number of pulses over the measurement timeframe) is modeled as a Poisson distribution.

| circuit        | threshold     | figures | sampling time | min. count @ rate | relative error |
|----------------|---------------|---------|---------------|-------------------|----------------|
| simulated      | computational | 5g, 5h  | 242 µs        | 242 @ 1 MHz       | 0.064          |
| experimental   | computational | 5e, 5f  | 10 ms         | 100 @ 10 kHz      | 0.100          |
| experimental   | en vivo       | 6       | 100 ms        | 1K @ 10 kHz       | 0.031          |

Table S2: Relative sampling error in variable-rate SPAD transfer function measurements

4.2 Tanh Ising neuron transfer curves

The transfer function of Ising neurons, which were only measured for the experimental demonstration of SPAD CTMC neurons, was directly done en vivo by sweeping the biases $h_i$ of each neuron while leaving the weights $w_{ij}$ unused. This was done after calibrating the rates of the individual variable-rate SPADs to be equal (by introducing bias offsets to each SPAD circuit). With a set $h_i$ bias $10^5$ samples of the neuron states were collected, and the fraction of samples in the +1 state were tabulated for each Ising neuron. This process was repeated for each integer bias value in the range $[-75, 75]$, representing the full usable input range of each neuron. Since updates in a SPAD CTMC neuron are not clocked but occur whenever a SPAD circuit produces a pulse, samples were taken at a relatively slow 200 kHz so that successive samples were not too correlated. Thus each point on the measured neuron transfer function represents the mean of $10^5$ roughly
I.I.D. samples of a Bernoulli random variable, yielding a worst-case measurement uncertainty of $7 \times 10^{-4}$ at neutral bias.

### 4.3 Ising and Potts model distributions

The distribution of samples produced by SPAD CTMC Ising and Potts models was measured by setting up a network configuration (weights, biases, and computational temperature) and then recording 5 million samples of the network state. As with the measurement of individual Ising neuron transfer characteristics, consecutive samples are not independent. For full Ising and Potts models the issue is even more acute, since it can take many updates for the collective model state to transition between regions of its state space; this is often referred to as the mixing problem, and its severity further depends on the particular configuration of weights and biases. In addition, samples were recorded on a 50 MHz clock even though DAC update pausing (see Hardware Implementation) prevented the state from updating faster than 2 MHz. In light of these obfuscations we present empirical evidence of measurement uncertainty instead of performing any rigorous bounding. The 5 million samples were collected in 50 sub-batches, and after each batch the Kullback-Leibler (KL) divergence between the measured distribution (cumulative across previously captured samples) and the theoretical distribution was calculated, shown in figure S3. This figure shows that rather than continuing to decrease, the KL divergence plateaus, indicating that the difference between the measured and theoretical distributions is real and not an artifact of measurement uncertainty - otherwise the KL divergence would continue to decrease as more samples were recorded. From this we can conclude that the measurement uncertainty of the Ising and Potts distributions is less than the visible deviations from the ideal distribution, and that, unsurprisingly, the SPAD-based Boltzmann machine does slightly deviate from ideal behavior.

![Figure S3: Kullback-Leibler divergence of distributions sampled from Ising and Potts SPAD CTMC neurons, in reference to the theoretical distribution.](image-url)