Barrel Shifter Physical Unclonable Function Based Encryption

Yunxi Guo  
Department of Electrical and Computer Engineering  
Iowa State University  
Ames, IA 50011  
Email: yunxig@iastate.edu

Timothy Dee  
Department of Electrical and Computer Engineering  
Iowa State University  
Ames, IA 50011  
Email: timdee@iastate.edu

Akhilesh Tyagi  
Department of Electrical and Computer Engineering  
Iowa State University  
Ames, IA 50011  
Email: tyagi@iastate.edu

Abstract—Physical Unclonable Functions (PUFs) are circuits designed to extract physical randomness from the underlying circuit. This randomness depends on the manufacturing process. It differs for each device enabling chip-level authentication and key generation [1] applications. We present a protocol utilizing a PUF for secure data transmission. Parties each have a PUF used for encryption and decryption; this is facilitated by constraining the PUF to be commutative. This framework is evaluated with a primitive permutation network - a barrel shifter [2]. Physical randomness is derived from the delay of different shift paths. Barrel shifter (BS) PUF captures the delay of different shift paths. This delay is entangled with message bits before they are sent across an insecure channel. BS-PUF is implemented using transmission gates; their characteristics ensure same-chip reproducibility, a necessary property of PUFs. Post-layout simulations of a common centroid layout [3] 8-level barrel shifter in 0.13 \( \mu m \) technology assess uniqueness, stability and randomness properties. BS-PUFs pass all selected NIST statistical randomness tests [4]. Stability similar to Ring Oscillator (RO) PUFs under environment variation is shown. Logistic regression of 100,000 plaintext-ciphertext pairs (PCPs) failed to successfully model BS-PUF behavior.

I. INTRODUCTION

Encryption/decryption algorithms form the backbone of modern public key infrastructure which supports a broad set of activities such as e-commerce and digital currency. Mathematical cryptosystems such as RSA [5] can take millions of clock cycles. Even symmetric encryption/decryption through AES takes 10-20 clock cycles. Moreover, even though their security is predicated on a hard mathematical problem such as prime number factoring, a mathematical model exists for an adversary [6]. Physical unclonable functions (PUFs) source physical randomness of a silicon foundry with a potential appeal of unmodelable, physical functions. They have been used to generate unique physical identities, and to seed key generation. Such PUFs offer both inter-chip variability and same-chip reproducibility. The variability ensures that distinct devices produce different outputs given the same input. Reproducibility, on the other hand, is valuable for predictability and determinism in the device authentication behavior. As a result, PUFs based on complex physical systems provide significantly higher physical security over the traditional systems which rely on storing secrets in nonvolatile memory. In addition, special manufacturing processes are not required to produce PUF devices. This advantage makes PUF devices a cost-effective and reliable alternative to mathematical randomness sources.

So far, the use of PUFs in cryptography is somewhat limited - the most common being key generation or random number generation. Chen used analog circuits to support cryptography with some elements of PUF like randomness [7]. Choi et al. deployed a variant of arbiter PUF to replace symmetric encryption in RFID domain as an authentication mechanism [8]. This was based on the earlier work of Suh et al. [9] that deployed PUFs for anti-counterfeiting in RFIDs [10]. Che et al. described another authentication protocol based on PUFs [11]. [12] developed an IoT communication protocol based on PUFs. [13] developed a code encryption engine based on PUFs for supporting a secure execution environment similar to AEGIS [14]. The key difference between a processor secure execution environment and general encryption is that for the former scenario the processor platform is both the source and destination for the communication. In a processor secure execution environment, both the sender and receiver have access to the same physical PUF on the same platform. However, for general encryption, this assumption is violated. Both the sender and receiver possess distinct and different PUFs. We show a general communication protocol based on commutative PUFs.
The key contributions of this paper are: (1) We explore several PUFs based information exchange protocols which serve to encrypt/decrypt information, find the best protocol through analysis; (2) this protocol requires PUFs to be physically commutative. We develop a framework for physically commutative PUFs based on permutation networks; (3) We evaluate permutation networks based physically commutative PUF framework with a primitive permutation network using barrel shifters. Barrel shifters have symmetric input to output path delays. Hence if two different paths within the same barrel shifter generate randomly uncorrelated delays, it is a strong lower bound for randomness in general permutation networks with more skewed path delays; (4) The results show good same chip, same path delay reproducibility; good differentiation between different chip, same path delay and same chip, different path delay; delays within 1-bit accuracy for the logic high and logic low propagation through the same path demonstrates physical commutativity; and good pseudo-random number generator properties for delay.

This paper is organized as follows. Section II introduces communication protocol. Section III illustrates commutative PUF encryption protocol. Section IV shows the schematic of barrel shifter PUF. Section V presents the detailed circuit implementation of barrel shifter PUF. Variability/reproducibility and commutativity test results based on post-layout simulations are presented in Section VI. Performance of BS-PUFs based encryption protocol is evaluated in Section VII. Sections VIII and IX discuss future work and conclusions.

II. COMMUNICATION PROTOCOL

Fig. 1 depicts Bob as the sender and Alice as the receiver. Both Bob and Alice have their own PUF. If Bob encrypts his message \( m \) with his PUF as \( f_{Bob}(m) \), Alice has no way to decrypt it except to ask Bob to decrypt it for her. The following protocol overcomes this asymmetry.

1) Bob encrypts the message \( m \) with \( f_{Bob} \).
2) Bob sends \( f_{Bob}(m) \) to Alice.
3) Alice encrypts \( f_{Bob}(m) \) with \( f_{Alice} \). (At this point, Alice does not know the message \( m \).)
4) Alice sends \( f_{Alice}(f_{Bob}(m)) \) to Bob.
5) Bob decrypts \( f_{Alice}(f_{Bob}(m)) \) with \( f_{Bob}^{-1} \) and obtains \( f_{Alice}(m) \).
6) Bob sends \( f_{Alice}(m) \) to Alice.
7) Alice decrypts \( f_{Alice}(m) \) with \( f_{Alice}^{-1} \) and obtains the message \( m \).

Message confidentiality is maintained by entangling message bits with physical randomness. The entangling process must be commutative so that the order of \( f_{Alice} \) and \( f_{Bob} \) can be changed. Decryption of entangled messages requires reversibility. The entangled message \( m' \) must exhibit a non-linear relationship with \( m \); this makes it hard for an eavesdropper to learn \( m \) by examining intermediate messages.

The circuit design and encryption protocol enable the commutative, invertible, and non-linear relationship properties of messages. Section III describes a mechanism for BS-

![Fig. 2. Cipher block chaining methods are used to encrypt (a) and decrypt (b) messages. This prevents the adversary from identifying plaintext patterns; it ensures identical blocks of plaintext encrypt to different ciphertext.](image)

III. ENCRYPTION PROTOCOL

Encryption must entangle the physical randomness of BS-PUF with the message. Physical randomness is extracted by measuring the delay of message bits along a shift path. An XOR of the message bits and delay accomplishes entanglement; this allows for commutativity and reversibility.

A. Encrypting Large Messages

A BS-PUF uses an \( n \)-bit key as shift amount. This allows for a \( 2^n \)-bit BS-PUF challenge (message) resulting in a \( 2^n \)-bit BS-PUF response. Alternately, one could view \((n - bit \ key, 2^n - bit \ message)\) as a challenge. We take the former \( 2^n \)-bit challenge view in this paper. For a barrel-shifter, practical values for \( n \) are limited to be in the range \( 7 - 10 \) bits leading to a message block size of \( 128 - 1024 \) bits. This means that a method of entanglement/encryption for plaintexts greater than \( 2^n \) bits is needed.

Entanglement could occur by serializing the blocks of plaintext at BS-PUF input and concatenating the generated ciphertexts. However, this approach reveals patterns in the plaintext; the same plaintext will always encrypt to the same ciphertext. This leaks information by allowing an adversary to identify plaintext patterns.

The technique of cipher block chaining (CBC) is typically applied in block ciphers such as AES [14]. Like AES, BS-PUF encrypts a fixed number of plaintext bits. Thus, it can be viewed as a block cipher. A practical barrel-shifter or permutation network implementation could consist of 128-1024 bit blocks.
It could be generated with any PUF, e.g. SRAM PUFs [15].

Asymmetric Key Encryption: Encrypting without a shared key is ideal.

Section I dictates invertibility and commutativity as communication protocol requirements.

PUF \( f \) must be a one-to-one function to achieve encryption and invertibility for decryption. Many classical PUFs, such as RO-PUFs [16], [17], [18], [19] and arbiter PUFs [20], [21], cluster the challenges into equivalence classes on a set of attributes resulting in the same response per challenge equivalence class. Arbiter PUF uses relative bit arrival time as the clustering attribute. RO PUF uses relative oscillator frequencies. The end result is that this makes these PUFs not invertible, since the mapping is many-to-one.

Further note that physical invertibility is distinct from logical invertibility. A mathematical one-to-one function has logical invertibility, but may not be physically invertible. Physical invertibility is applicable to the PUF physical attribute measurement process. In the forward computation, inputs traverse the computation paths to the output; physical measurements may take place at various points along these paths. In the inverse computation, output bits travel to the inputs through the identical computation paths in reverse. The physical measurements of the same physical attribute occur in the inverse computation. These forward and inverse physical measurements need to be reproducible at all measurement points from input to output.

Permutation functions provide the necessary one-to-one relationship. Permutations create a non-linear relationship from input bits to output bits. Due to this property, an adversary cannot create a useful mathematical model describing the input, output relationship. For a \( n \)-bit data, there exist \( N = n! \) permutations denoted by \( \pi_0, \pi_1, ..., \pi_{N-1} \). Each \( \pi_i \) captures some permutation \( (i_0, i_1, ..., i_{n-1}) \), where bit \( k \to i_k \). In other words, the bit at 0 is routed to bit position \( i_0 \) in the output. A key \( K \) is used to select this mapping. We call this

\[
\begin{align*}
\text{Message sent by Bob: } & f_{\text{Bob}}(x) \\
\text{Message received by Alice: } & f_{\text{Alice}}(f_{\text{Bob}}(x)) \end{align*}
\]

Fig. 3. (1) Bob applies \( f_{\text{Bob}} \) and (2) sends the result to Alice. (3) Alice applies \( f_{\text{Alice}} \) and (4) sends the result to Bob. (5) Bob applies \( f_{\text{Bob}}^{-1} \) and (6) returns the result to Alice. (7) Alice applies \( f_{\text{Alice}}^{-1} \) hoping to recover the message. Unfortunately, \( f_{\text{Bob}}^{-1} \) does not subtract delay from the correct bit in (5), (7); the correct message is not received by Alice. This scheme fails to be commutative.

\[
\begin{align*}
\text{Message sent by Bob: } & c_i = BS - PUF(p_i, K) \\
\text{Message received by Alice: } & c_i' = BS - PUF(p_i, K)
\end{align*}
\]

Fig. 4. Sharing a key allows both parties to perform the same permutation. This ensures the delay is subtracted from the correct bit when performing the inverse \( f_{PUF_i}^{-1} \) for \( l = 1, 2 \). Entropy is added into public message by bit shifting.

\[
\begin{align*}
\text{Message sent by Bob: } & c_i = BS - PUF(p_i, K) \\
\text{Message received by Alice: } & c_i' = BS - PUF(p_i, K)
\end{align*}
\]
a keyed PUF: \( R_{i, K} = f(K, P_i) \). The PUF response is derived from the shift path delay.

The protocol requires the entanglement procedure to be commutative. Entanglement adds a bit from the delay of each path to the plaintext. Thus, entanglement is expressed as \( f(K_{Bob}, P_i) = P_i \oplus D_{Bob} \). This is commutative because \( \oplus \) is commutative. Note that the entanglement between the physical delay attribute and logical bits can occur at multiple points during the flight of message bits from input to output; each measurement point is also an entanglement point.

Our first version of encryption protocol is based on invertible and commutative PUFs. Invertibility requires using a raw physical property like delay. The reversible computation principle states that any information loss makes a process irreversible [22]. Many PUFs derive their response through the comparison of physical properties. Arbiter PUF uses a race between two paths, RO-PUF uses a frequency comparison. These comparisons produce reproducibility by including a wide margin of noise before comparison output changes, but information is lost.

The proposed PUF is based on a barrel shifter. Constructing it with precisely sized transmission gates makes its delay independent of bit state 0 or 1. Bit propagation delay for forward path and inverse path is remarkably stable and consistent regardless of bit state. This is due to symmetric physical structure of MOSFET’s source and drain. As we discuss in the following, physical commutativity and invertibility in our protocol is only achieved if the physical delay on the paths is bit state independent. The Step 5 of Fig. 1, when Bob computes \( f_{Bob}^{-1} \) is dealing with a different bit pattern at the output of Bob’s PUF than what was computed in Step 1 at Bob’s PUF’s output. This is because the Step 5 bit pattern has an additional permutation applied to it by Alice, which is not known to Bob. An alternative implementation could have used pass transistors. However, it is hard to equalize the delay for 0 and 1 through a pass transistor. Thus, transmission gates are used to make the delay plaintext independent.

Asymmetric key encryption protocol in Section II is based on invertible and commutative BS-PUFs; which are defined as follows:

- **Invertible PUF**: An invertible keyed PUF \( f \) on input \( x \) and key \( K \) is \( f(x, K) = y \iff f^{-1}(y, K) = x \), where \( f^{-1} \) is computed on the same PUF in the reverse direction. Note that the PUF function \( f \) entangles a logical component and a physical component, and both need to be invertible.

- **PUFs designed to be used directly for encryption need two input sequences**: (1) key for response function selection as in a permutation selector, (2) plaintext to be encrypted.

- **Commutative PUF**: Assume there is a composition of two commutative PUFs \( PUF_1 \) and \( PUF_2 \). This means \( PUF_2(PUF_1(x)) = PUF_1(PUF_2(x)) \). Note that both logical and physical commutativity are needed for such a commutative PUF. For BS-PUF, the entanglement function must be commutative for physical commutativity in addition to the physical measurements being the same in \( PUF_2(PUF_1(x)) \) and \( PUF_1(PUF_2(x)) \); this requires the physical measurements to be invariant of the bit state. The physical measurements are completely defined by the key \( K \) for a given PUF.

2) **Protocol Without Permutation**: In the first version of design, each PUF \( f_{PUF_1} \) and \( f_{PUF_2} \) is a permutation network keyed by \( key_1 \) and \( key_2 \) respectively. Key \( key_1 \) selects a permutation \( \pi_{key_1} \) from a large set of possible permutations -
Keccak permutation [23], [24] could be used for instance. The implementation, however, needs to be physically and logically reversible consisting of transmission gates. We assume that for a permutation $\pi_{\text{key}}$ which maps ith input bit to the i'th output bit and jth input bit to j'th output bit, we capture the exact delays for each input-output path. Let $D(i, i')$ denote the delay of the path from input i to output i' for $\pi_{\text{key}}$ in $f_{\text{PUF}}$. Let $D(j, j')$ be defined likewise. We will describe how we can capture these delays by using timer capture and edge detector functions in Section V.

For each PUF, the output bit $y_i$ can be expressed as an entanglement function $e(x_{\pi^{-1}_{\text{key}}}(j), D(\pi_{\text{key}}^{-1}(j), j))$. Here $e$ is an entanglement function between the bit routed to output j ($x_{\pi^{-1}_{\text{key}}}(j)$) and the delay of this path from $\pi^{-1}_{\text{key}}(j)$ to j.

The delay $D(\pi^{-1}_{\text{key}}(j), j)$ can be quantized to any resolution of k bits. If we use all of the k bits of $D(\pi^{-1}_{\text{key}}(j), j)$ to do encryption at the jth output bit, we expand the n-bit input to an nk-bit output. Assuming we want to retain the same output resolution of n-bits, one option would be to perform an XOR ($\oplus$) of the nth bit of $D(\pi^{-1}_{\text{key}}(j), j)$ with the input bit $x_{\pi^{-1}_{\text{key}}}(j)$ to generate $y_j$ leading to the entanglement function $y_j = e(x_{\pi^{-1}_{\text{key}}}(j), D(\pi_{\text{key}}^{-1}(j), j))$. XOR is a good choice because it is commutative and associative. Since the least significant bit (LSB) and 2nd LSB of $D(\pi^{-1}_{\text{key}}(j), j)$ is likely least correlated with other paths, we have used them in entanglement. The corresponding simulation results are shown in Section VI.

Let us assume that the delays of the permutation function $\pi_{\text{key}}$ in $f_{\text{PUF}}$ are denoted by $D(\pi_{\text{key}}(j), j)$ for a path from input $\pi^{-1}_{\text{key}}(j)$ to output j and the delays of the permutation function $\pi_{\text{key}}$ in $f_{\text{PUF}}$ are denoted by $d(j, \pi_{\text{key}}(j))$ for a path from input j to output $\pi_{\text{key}}(j)$. Assume that $\pi^{-1}_{\text{key}}(j) = i$, $\pi_{\text{key}}(j) = k$, then the output $z_k = (x_i \oplus D(i, j)) \oplus d(j, k)\text{mod}m$ is generated. The nth least significant bit of PUFG's delay captured by the d function is XORed with $f_{\text{PUF}}$'s output.

Clearly, the RHS of expression $z_k = (x_i \oplus D(i, j)) \oplus d(j, k)\text{mod}m$ is commutative due to commutativity of operator $\oplus$ - it does not matter whether $f_{\text{PUF}}$ is applied first or $f_{\text{PUF}}$ is applied first. However, this commutativity statement is only correct for a specific bit routing, but incorrect for encrypted data.

Consider $PUF_1$ with $\pi_{\text{key}} = (0 \mapsto 1, 1 \mapsto 2, 2 \mapsto 3, 3 \mapsto 0)$ for a 4 bit input $x_0, x_1, x_2, x_3$ and $PUF_2$, with $\pi_{\text{key}} = (0 \mapsto 2, 1 \mapsto 3, 2 \mapsto 0, 3 \mapsto 1)$. Composition of $f_{\text{PUF}} = f_{\text{PUF}_2} \circ f_{\text{PUF}_1}$ is $((0 \mapsto 1, 1 \mapsto 2, 2 \mapsto 3, 3 \mapsto 0) \circ (0 \mapsto 2, 1 \mapsto 3, 2 \mapsto 0, 3 \mapsto 1)) = (0 \mapsto 3, 1 \mapsto 0, 2 \mapsto 1, 3 \mapsto 2)$. By going over the communication protocol in Fig. 1 step by step, a defect becomes apparent. The complete verification process is shown in Fig. 2.

In the following analysis, permutations are abbreviated according to output positions for simplicity. For instance, $\pi_{\text{key}} = (0 \mapsto 1, 1 \mapsto 2, 2 \mapsto 3, 3 \mapsto 0)$ is abbreviated to $\pi^{-1}_{\text{key}}(1, 2, 3, 0)$. Assume $\pi_{\text{PUF}_1} = (1, 2, 3, 0)$ and $\pi_{\text{PUF}_2} = (2, 3, 0, 1)$.

**Step 1:** Apply $f_{\text{PUF}_2}$ to $(x_0, x_1, x_2, x_3)$ resulting in $(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$, which equals $(x_3 \oplus D(3,0))m, x_0 \oplus D(0,1)m, x_1 \oplus D(1,2)m, x_2 \oplus D(2,3)m$.

**Step 3:** Apply $f_{\text{PUF}_2}$ to $f_{\text{PUF}_1}$'s output as in $(2, 3, 0, 1)(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$. This equals $(x_1 \oplus D(1,2)m \oplus D(2,0)m, x_2 \oplus D(2,3)m \oplus D(3,1)m, x_3 \oplus D(3,0)m \oplus D(0,2)m, x_0 \oplus D(0,1)m \oplus D(1,3)m)$.

**Step 5:** Now invert the output. Apply $f_{\text{PUF}_1}^{-1}$ to $(2, 3, 0, 1)(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$. $f_{\text{PUF}_1}^{-1}$ results in $(1, 2, 3, 0)^{-1}(2, 3, 0, 1)(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$ which equals $(x_2 \oplus D(2,3)m \oplus D(3,1)m \oplus D(0,1)m, x_1 \oplus D(1,2)m \oplus D(2,3)m \oplus D(3,0)m, x_0 \oplus D(0,2)m \oplus D(1,3)m)$. $D(i, i')$ denotes the backward path delay from output i to input i'. According to post-layout simulations, $D(i, i')$ is always equal to $D(i, i')$ in BS-PUFs.

**Step 7:** Further applying $f_{\text{PUF}_2}^{-1}$ as in $(2, 3, 0, 1)^{-1}(1, 2, 3, 0)^{-1}(2, 3, 0, 1)(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$ results in $(x_0 \oplus D(0,1)m \oplus D(1,3)m \oplus D(2,3)m \oplus D(0,2)m, x_1 \oplus D(1,2)m \oplus D(2,0)m \oplus D(3,0)m, x_3 \oplus D(3,0)m \oplus D(0,2)m \oplus D(1,2)m)$. This logical result is correct in routing $x_i$ back to the rth bit position, but the physical delay terms are completely mixed up and do not cancel each other.

3) Protocol With Permutation: In order to ensure the correct routing and commutativity, we modify the original permutation protocol by adding a permutation after each PUF. The primary function of this permutation is routing $x_i$ back to the rth position from position $\pi_{\text{key}}(i)$ before sending the message at the end of Step 1. The complementary key, $\overline{\pi}_{\text{key}}$, that results in the permutation $\pi_{\text{key}}^{-1}$ is used; it routes bits back to their original position. Mathematically, $(\pi_{\text{key}} \circ \pi_{\text{key}}^{-1}) = 1$ where 1 is the identity permutation. Bit shifting
to restore the original message bit order is the only function of this permutation. No delay is added.

An example of this protocol is shown in Fig. 5 with the following detailed description.

- **Step 1:** $f_{Bob}$ permutes $x_0, x_1, x_2, x_3$ as in $(1, 2, 3, 0)(x_0, x_1, x_2, x_3)$. It computes the physical delay encrypted bit vector, $(x_3 ⊕ D(3, 0)_m, x_0 ⊕ D(0, 1)_m, x_1 ⊕ D(1, 2)_m, x_2 ⊕ D(2, 3)_m)$. Before sending it to Alice, Bob’s complementary permutation, called permutator in Fig. 5, is applied to generate $(x_0 ⊕ D(0, 1)_m, x_1 ⊕ D(1, 2)_m, x_2 ⊕ D(2, 3)_m, x_3 ⊕ D(3, 0)_m)$. In this new permutation protocol, the logical permutation does not add to the confusion at all unlike in AES or Keccak protocols. Confusion is achieved from the permuted physical delay properties of the PUF. Which Path delay bits are combined with each input bit is still hidden (through confusion) from the adversary through $key$ driven $\pi$.

- **Step 3:** $f_{Alice}$ is applied as $(2, 3, 0, 1)(x_0 ⊕ D(0, 1)_m, x_1 ⊕ D(1, 2)_m, x_2 ⊕ D(2, 3)_m, x_3 ⊕ D(3, 0)_m)$, resulting in $(x_2 ⊕ D(2, 3)_m ⊕ d(0, 2)_m, x_3 ⊕ D(3, 0)_m ⊕ d(3, 1)_m, x_0 ⊕ D(0, 1)_m ⊕ d(0, 2)_m, x_1 ⊕ D(1, 2)_m ⊕ d(1, 3)_m)$. Applying Alice’s complementary permutation results in $(x_0 ⊕ D(0, 1)_m ⊕ d(0, 2)_m, x_1 ⊕ D(1, 2)_m ⊕ d(1, 3)_m, x_2 ⊕ D(2, 3)_m ⊕ d(2, 0)_m, x_3 ⊕ D(3, 0)_m ⊕ d(3, 1)_m)$. Decryption follows a similar process. However, the direction of message transmission is reversed and the inverse permutations are used. This is where physical in invertibility helps recover the original forward delay vector in the reverse direction.

Thus, $(1, 2, 3, 0)(2, 3, 0, 1)(x_0, x_1, x_2, x_3))$ is rearranged by Bob’s permutator first. This is $(x_3 ⊕ D(3, 0)_m ⊕ d(3, 1)_m, x_0 ⊕ D(0, 1)_m ⊕ d(0, 2)_m, x_1 ⊕ D(1, 2)_m ⊕ d(1, 3)_m, x_2 ⊕ D(2, 3)_m ⊕ d(2, 0)_m)$. This rearranged result is given to $PUF_2$ resulting in $(x_0 ⊕ D(0, 1)_m ⊕ d(0, 2)_m ⊕ D(0, 1)_m, x_1 ⊕ D(1, 2)_m ⊕ d(1, 3)_m ⊕ D(1, 2)_m, x_2 ⊕ D(2, 3)_m ⊕ d(2, 0)_m ⊕ D(2, 3)_m, x_3 ⊕ D(3, 0)_m ⊕ d(3, 1)_m ⊕ D′(3, 0)_m)$. Transmission gates show symmetric delays for forward and backward paths; $D(i, j)$ always equals $D′(i, j)$. Thus, the delay terms cancel. The result after applying $f_{Bob}^{−1}$ is equal to $(x_0 ⊕ d(0, 2)_m, x_1 ⊕ d(1, 3)_m, x_2 ⊕ d(2, 0)_m, x_3 ⊕ d(3, 1)_m)$.

- **Step 7:** $f_{Bob}^{−1}$ is applied. First, Alice’s permutator will rotate the bits giving $(x_2 ⊕ d(2, 0)_m, x_3 ⊕ d(3, 1)_m, x_0 ⊕ d(0, 2)_m, x_1 ⊕ d(1, 3)_m)$. Rotated bits are then given to $PUF_2$ in the reverse direction resulting in $(x_0 ⊕ d(0, 2)_m, x_1 ⊕ d(1, 3)_m, x_2 ⊕ d(2, 0)_m, x_3 ⊕ d(3, 1)_m)$. The delay terms cancel. Alice receives the original message $(x_0, x_1, x_2, x_3)$ sent by Bob.

### 4) Symmetric Key Encryption:

The original protocol in Section III-B2 subtracted the delay from the incorrect bit in the inverse permutation. The protocol shown in Section III-B3 solves the original problem. However, it contains a fatal flaw; Using ⊕ for entanglement creates a linear relationship between messages in-flight between Bob and Alice. An eavesdropper can retrieve the original message from the in-flight messages.

Consider Fig. 5 as an example. The first bit in original message is $x_0$. The encrypted first bit sent from Bob to Alice in Step 2 is $B′ = x_0 ⊕ D(0, 1)$. Then from Alice to Bob in Step 4, $B″ = x_0 ⊕ D(0, 1) ⊕ d(0, 2)$. The decrypted first bit sent from Bob to Alice in Step 6 is $B‴ = x_0 ⊕ D(0, 1) ⊕ d(0, 2)$.

$B′$, $B″$ and $B‴$ are all public messages. An eavesdropper can extract the original message by:

1. Inferring Bob’s PUF’s delay information by taking XOR of $B″$ and $B‴$. $B″ ⊕ B‴ = x_0 ⊕ D(0, 1) ⊕ d(0, 2) ⊕ x_0 ⊕ d(0, 2) = D(0, 1)$.

2. Then the original message can be extracted by an XOR of $B′$ and Bob’s PUF’s delay. $B′ ⊕ D(0, 1) = x_0 ⊕ D(0, 1) ⊕ D(0, 1) = x_0$.

In order to eliminate this problem, BS-PUF must permute bits in public messages, which we could not do and yet preserve commutativity and invertibility. One possible solution that allows permuted public messages while preserving commutativity and invertibility is to let Bob and Alice share
the shared key is $\pi$ with the same key. The corresponding protocol is shown in Fig. 2.

In the shared key protocol, Bob permutes the input message with $\pi_K$ entangling it with his delay. Alice reverses the permutation using $\pi_K^{-1}$ entangling it with her delay. Note that the shared key is $K$. The bits are in their original positions in the message sent to Bob for decryption. Note that the entanglement with both PUFs’ delays protects this message. The delay will be un-entangled from the correct bits in the subsequent decryption steps. The bit order is different in the message from Bob to Alice versus in the message from Alice to Bob. This avoids linear leakage of information in XOR based equations on these two messages.

Details of the shared key scheme presented in Fig. 4 are as follows.

- **Step 1:** Bob permutes $x_0, x_1, x_2, x_3$ with $\pi = (1, 2, 3, 0)$ and gets $(x_2 \oplus D(3,0)_m, x_0 \oplus D(0,1)_m, x_1 \oplus D(1,2)_m, x_2 \oplus D(2,3)_m)$. It is sent to Alice without any further bit level routing; this achieves bit-level confusion of the public message.

- **Step 3:** $f_{Alice}$ performs the reverse permutation $\pi^{-1}$ of $f_{Bob}$ and simultaneously applies Alice’s delay ($\pi^{-1} = (3,0,1,2)$). After $f_{Alice}$ is applied, all bits are rotated back to their original position but each bit is encrypted with two physical delay values. In this example, after applying $f_{Alice}$ we get $(x_0 \oplus D(0,1)_m \oplus d(0,0)_m, x_1 \oplus D(1,2)_m \oplus d(2,1)_m, x_2 \oplus D(2,3)_m \oplus d(3,2)_m, x_3 \oplus D(3,0)_m \oplus d(0,3)_m)$.

- **Step 5:** $f_{Bob}$ is applied. Permutation $\pi$ is applied again and delay added in Step 1 is cancelled by XOR. Then message sent to Alice is converted to $(x_3 \oplus D(3,0)_m \oplus d(0,3)_m, x_0 \oplus D(0,1)_m \oplus d(1,0)_m \oplus D(0,1)_m, x_1 \oplus D(1,2)_m \oplus d(2,1)_m \oplus D(2,3)_m, x_2 \oplus D(2,3)_m \oplus d(3,2)_m \oplus D(2,3)_m)$ which is $(x_3 \oplus d(0,3)_m, x_0 \oplus d(1,0)_m, x_1 \oplus d(2,1)_m, x_2 \oplus d(3,2)_m \oplus d(2,1)_m, x_3 \oplus d(3,2)_m \oplus d(0,3)_m)$.

- **Step 7:** $f_{Alice}$ is applied, bit positions are rotated back again, and delay added in Step 3 is cancelled by XOR. The message from the previous step is converted to $(x_0 \oplus d(1,0)_m \oplus d(1,0)_m, x_1 \oplus d(2,1)_m \oplus d(2,1)_m, x_2 \oplus d(3,2)_m \oplus d(3,2)_m, x_3 \oplus d(0,3)_m \oplus d(0,3)_m)$, which equals the original message $x_0, x_1, x_2, x_3$.

Evaluating all messages crossing the insecure channel, $M' = (x_3 \oplus D(3,0)_m, x_0 \oplus D(0,1)_m, x_1 \oplus D(1,2)_m, x_2 \oplus D(2,3)_m), M'' = (x_0 \oplus D(0,1)_m \oplus d(1,0)_m, x_1 \oplus D(1,2)_m \oplus d(2,1)_m, x_2 \oplus D(2,3)_m \oplus d(3,2)_m, x_3 \oplus D(3,0)_m \oplus d(0,3)_m), M''' = (x_3 \oplus d(0,3)_m, x_0 \oplus d(1,0)_m, x_1 \oplus d(2,1)_m, x_2 \oplus d(3,2)_m)$, no linear relationships exist among any pairs of messages that yield information to a man-in-the-middle. No duplicate delays appear at any bit position. There is no way to retrieve original message from the in flight messages without the shared key and access to Bob and Alice’s PUFs.

All messages are protected while traversing the insecure channel. The permutation applied by Bob protects the first message as it travels to Alice. Entanglement with both Alice and Bob’s delay protects Alice’s response. The permutation then protects the final message from Bob to Alice.

**IV. BARREL SHIFTER PUF DESIGN**

We evaluate a barrel shifter as a potential invertible and commutative PUF. The block diagram of a barrel shifter is shown in Fig. 5. For simplicity, only two shift levels are shown. Output Logic is added to capture path delay $D(i, k)$. A Event Counter is initialized to 0. The RST signal simultaneously starts the Event Counter and releases the input message. The delay is captured by reading the Event Counter when the Output Logic detects a transition. Finally, the entanglement
Each shift stage is logically similar to an arbiter PUF stage.

Key bits determine the shift amount $s = \sum_{i=0}^{k} (key_i \times 2^i)$. Thus, $key_i$ is applied from LSB to MSB, from left to right.

The key determines the shift amount. For example, in diagram $key = \{0, 1\}$ encodes for right shift by 2 in the second stage. Consequently, $Input_0$ traverses a different path; provides a different delay results with different keys.

The delay variation is generated by transistor-level mismatch and doping variability. Variation accumulates over several stages. It is then significantly large to be detected by the Output Logic.

BS-PUF must be invertible; this property facilitates decryption. Consequently, the physical delay measurements must not depend on the bit state; they should be a function only of the path.

V. CIRCUIT IMPLEMENTATION

A commutative PUF based on a barrel shifter is implemented in hardware. Transmission gates implement the shift paths. The circuit is subdivided into 3 components: input logic, shift unit and output logic.

A. Input logic

Input logic is used to trigger the delay test system. It is a 3-input, 1-output circuit that connects the input signal $S$ or its inverse $\overline{S}$ to output terminal (Fig. 7). Input logic consists of three transmission gates. $RST$ (reset) is used to control ON/OFF status of the first transmission gate. When $RST$ is high, $Input$ travels through the first gate and arrives at an intermediate node. Otherwise, it is blocked. $REV$ (reverse) determines whether $Input$ is inverted. $Input$ will be inverted when $REV = 1$. The function definition for input logic is:

$$output = RST \cdot (REV \oplus input).$$

B. Shift unit

Shift units implement the path selection and form shift stages. Shift unit size determines the magnitude of delay. We construct a barrel shifter with 8 shift stages for testing. Each layer 256 contains shift units. Each stage shifts by either $2^{7-n}$ or 0 where $n$ is the stage index.

Each shift unit is a 4-input, 1-output circuit show in Fig. 8. Either $inputA$ or $inputB$ is mapped to output. The mapping is determined by the key. A key value of 1 causes the upper transmission gate to open; output then becomes $inputA$. Otherwise, output becomes $inputB$.

The path delay value should vary depending on the shift path. Path delay primarily depends on shift units’ transmission gates. Adding additional load capacitance after each transmission gate or accumulating variation over several stages of transmission gate enlarge the delay; it becomes detectable by the path delay counter.

In BS-PUFs, PUFs uniqueness depends on how much delay variation could be provided by same path on different chip. Modifying transistor area is the main method for increasing the inter-chip variation. Transistor delay variation is inversely proportional to transistor area. Sizing transistors smaller results in increased delay variation. However, BS-PUF requires plaintext independent path delay. Path delay for a 1-valued bit compared to a 0-valued bit differs for minimum transistor sizes. Hence larger transistors are used in shift units.

C. Output logic

Output logic measures/captures path delay. Output logic for each bit contains 3 parts: counter, edge detector trigger generator and entanglement logic (Fig. 9(d)).

Counter takes $CLK$ and $RST$ as input producing a 10-bit output; it counts the number of rising edges of $CLK$. Setting $RST$ high resets the counter to 0. The path delay is expressed as $(input\ clock\ period) \times (counter\ value)$.

Edge detector trigger generator generates a pulse in response to a transition at its input. It includes an edge detector (Fig. 9(b)) and a positive edge trigger generator (Fig. 9(c)). Edge detector converts a rising or falling edge into a rising edge at its output. Positive edge trigger generator converts the rising edge from edge detector into a pulse.

The output logic works as follows. First, a rising/falling edge at input produces a pulse at edge detector trigger generator output. This pulse enables the transmission gate in Fig. 9(d) for a short time period. During this time, counter output is captured; it must not change while being captured. Thus, enable time period must be shorter than clock period. Entanglement logic extracts the $m$th LSB of delay $D(i, \bar{i})$. Computing XOR of this bit with the input signal $x_i$ results in the entangled output bit.

The output logic works by detecting a transition. An transition occurring depends on the previous output value. Thus, the output logic is incapable of detecting unchanging output values. An output transition is forced by providing $\pi_i$ before $x_i$ at the input.

D. Path Delay Testing

The input logic, shift unit and output logic work together to capture the path delay. The following five steps are necessary.

1) Set $\pi_i$ as input and reset input logic.
2) Wait for $\pi_i$ to arrive at output logic.
3) Reset input logic and clock counter, set $x_i$ as input.
4) Wait as $x_i$ travels the path determined by key triggering a transition at the output logic.
5) Encrypt using the captured counter value.

VI. POST-LAYOUT SIMULATION RESULT

The entanglement logic utilizes a 1-bit result from the path delay. The path delay capture logic provides a multiple-bit delay counter. One bit must be chosen; it must be shown to have the requisite properties for BS-PUF: (1) inter-chip variability, (2) intra-chip reproducability, (3) randomness, (4) commutativity.
Cadence Spectre simulations are used to generate raw delay data. Delay variability assessment is conducted by $3\sigma$ Monte Carlo sampling over process parameters. This test uses IBM 130 nm PDK. A common centroid layout is employed to reduce linear gradient errors [29].

We construct an 8-level barrel shifter accepting a 256-bit input with a 256-bit output. Output logic similar to input capture logic in [30] detects output voltage changes. Voltage transitions send a control signal to a counter. Path delay is captured at the resolution of the counter’s clock period; a period of 4ns is used. Delays must be a reasonable multiple of the clock period to express variation.

In the following experiments, we primarily focus on raw data: (1) Monte Carlo sampling 200 times on the path from input 0 to output 16 (2) Monte Carlo sampling 200 times on all 256 paths with no shifting.

**A. Inter-chip Variability**

Shift path delay is a function of the silicon fabrication process; it potentially exhibits PUF properties. Each shift path terminates with entanglement logic requiring one bit. A bit from the delay counter must be selected. The chosen bit must exhibit sufficient variation.

Monte Carlo simulation captures single path delay variability as a proxy for inter-chip delay variability. As shown in Fig. [II] in 200 Monte Carlo samples for process parameters performed on path $x_0 \rightarrow y_{16}$, the delay ranges from 85 ns to 145 ns with an average around 120 ns. It is a $\pm25\%$ ($\pm30$-ns) variation. Counter output varies about $\pm8$. This indicates that roughly the least significant 3 bits of delay have significant entropy in inter-PUF measurements. Thus, the LSB, 2nd LSB, and 3rd LSB are candidates for entanglement.

**B. Inter-chip Uniqueness**

The chosen path delay bit must exhibit inter-chip uniqueness. This requires significant variance between responses on different chips. Pair-wise hamming distance (HD) is a criterion that measures variability.

The HD of 200 path delay samples of 256-bit responses is computed. Table [III] shows distribution of inter-chip HD for LSB. Similar figures are given for 2nd LSB in Table [IV]. For LSB, the mean HD is 127.99 bits with a standard deviation of 8.04 bits. For 2nd LSB, these values are 128.01 bits and 7.99 bits, respectively. HD 128 means roughly 50% of the response bits differ. It is maximally unlikely that two BS-PUFs will generate the same output.

**C. Intra-chip Reproducibility**

The usefulness of a single PUF relies on it producing a consistent response to a challenge; they should be independent from the environment. Tests are performed subjecting BS-PUF to: (1) temperature variation (2) voltage supply variation. The frequency of response bit flips is quantified.

Bit flip rate is frequency a bit changes from 0 $\rightarrow$ 1 or 1 $\rightarrow$ 0. It is computed relative to some baseline response. Gathering responses at common room temperature (25°C) and supply voltage ($5V$) establishes this baseline. The percentage of path delays where a bit flips is the bit flip rate. For example, the LSB flipping in 64/256 paths represents a 25% bit flip rate.

BS-PUF retains a bit flip rate smaller than 18% under environment variation. This is similar to the flip rate of traditional RO PUFs [31].

**1) Temperature Variation:** Temperature is varied from 0 to 50°C. Path delay of all 256 bit paths are gathered with Monte Carlo sampling at 0°C, 10°C, 20°C, 25°C, 30°C, 40°C and 50°C. The maximum path delay variation is $-4ns$ to $5ns$. The
counter logic increments at 4ns frequency; a ±1 bit change in path delay is expected.

Knowing how temperature variation affects the chosen entanglement bit is ideal; bit flip rate quantifies this. It is computed in response to temperature variation, shown in Fig. [12]. Vertical bars represent bit flips for LSB (blue) and 2nd LSB (green). 2nd LSB flip rates is under 12% while LSB’s flip rate is significantly higher. Thus, the 2nd LSB provides better reproducibility.

2) Voltage Supply Variation: Supply voltage varies under realistic conditions. Path delay of all 256 bit paths are gathered with Monte Carlo sampling at supply voltages of 4.64V, 4.70V, 4.76V, 4.82V, 4.88V and 4.94V.

Bit flip rate is computed in response to voltage variation, shown in Fig. [13]. Flip rates for the 2nd LSB is under 18% while LSB rates are significantly higher. The 2nd LSB again provides better reproducibility; it is the best candidate for the entanglement bit.

A higher order bit could be selected. It would have comparatively better flip rates, but reduced variability. Many mature techniques exist to compensate for temperature and voltage variation [32, 33]. These techniques operate at the flip rates expressed by LSB and 2nd LSB. Thus, the advantage of choosing a higher order bit is minimal.

D. Randomness

Output of a good PUF should look like a pseudo-random number generator so that an attacker cannot model it easily. Assessing randomness performance of BS-PUF uses data from Monte Carlo sampling of path delays. Delay values are converted to binary responses by extracting the nth LSB bit from the delay. Each 256-bit response (one bit from each path) is examined using NIST statistical test suite.

Table I and Table II give the detailed test results for LSB and 2nd LSB of the BS-PUFs output. The minimum pass rate for each statistical test is 193 for a sample size of 200 binary sequences according to NIST documentation. Thus, both LSB and 2nd LSB pass the randomness test; a proportion greater than 193 is achieved on all tests.

E. Commutativity

Encryption and decryption rely on function composition. Decrypting a message encrypted by both self and another party is required. The other party may have changed the bit values (0 or 1). Thus, Delay variation must be independent of the bit value. An input of 1 must have the same path delay as an input of 0.

BS-PUF path delays depend only on the permutation key. Shift units are sized to achieve balanced pullup and pulldown resistance. Transmission gate NMOS sizing is \( W/L \) and 2/3 PMOS sizing is \( W_p/L_p = 1/1 \), where \( L_n = L_p \).

Two tests are performed to verify pullup and pulldown variability.

1) Testing rising/falling edge delay in four different (FF, FS, SF, SS) process corners. Transmission time difference for 0 and 1 must be smaller than the counter period (4ns).

2) Performing Monte Carlo sampling of path delay for inputs 0 and 1. Delays are recorded for all paths without bit shifting. No bit flips should occur in the path delay. Maximum transmission time difference for 0 and 1 is 2.34ns; this is much smaller than the 4ns clock period. Consequently, no path delay bits flip in Monte Carlo sampling.

VII. Performance Evaluation

A. Modeling Attack

According to [34], all examined Strong PUFs under a given size can be modeled with machine learning with success rates above their stability in silicon. Consider the barrel shifter in our communication protocol to be a black box. Attackers know nothing about the key and physical delay of barrel shifter. An attacker should not be able to model the relationship from
response with a variety of training sets with different sizes. Machine learning prediction decreases with the size of training set: however, it does not apply when voltage supply and temperature are considered.

Simulating BS – PUF(P, K) requires computationally expensive Cadence Spectre simulations. An efficient method for computing R, given K, is needed. Thus, we apply Monte Carlo Sampling to create a delay matrix, D, modeling the delay of all shift paths. The delay of each shift unit is recorded. Path delay is then computed by: (1) summing the delay of all shift units along a path, (2) dividing it by 4ns capture logic resolution, (3) extracting LSB or 2nd LSB. Thus, D enables computations of path delays given K. For example, Eq. (1) is a sample delay matrix for 4 inputs, 2 stage BS-PUFs. d_{i,j} represents exact delay value of top and bottom transition gates in i th row, j th column shift unit.

\[
D = \begin{bmatrix}
(d_{0,0,0}, d_{0,0,1}, d_{0,1,0}, d_{0,1,1}) \\
(d_{1,0,0}, d_{1,0,1}, d_{1,1,0}, d_{1,1,1}) \\
(d_{2,0,0}, d_{2,0,1}, d_{2,1,0}, d_{2,1,1}) \\
(d_{3,0,0}, d_{3,0,1}, d_{3,1,0}, d_{3,1,1})
\end{bmatrix}
\]  

(1)

Plaintext-ciphertext pairs (PCP) are computed using D. For the delay matrix in Eq. (1) using a key 1 = \{1, 0\} encoding for right shift in the first stage, the plaintext \( (i_0, i_1, i_2, i_3) \) generates the response in Eq. (2).

\[
R = \begin{bmatrix}
i_3 \oplus ((d_{0,0,0} + d_{0,1,1})/4) \\
i_0 \oplus ((d_{1,0,0} + d_{1,1,1})/4) \\
i_1 \oplus ((d_{2,0,0} + d_{2,1,1})/4) \\
i_2 \oplus ((d_{3,0,0} + d_{3,1,1})/4)
\end{bmatrix}
\]  

(2)

This process makes extraction of all possible PCP feasible. For a BS-PUF with an input message length of 256-bit, there are 2^{256} possible input messages. There are 8 stages with 2^8 possible keys. It is infeasible to generate all 2^{264} PCPs. Linear Regression (LR) is performed with a training set of size \( n = \{10,100,1000\} \) PCPs per key. To obtain a representative sample of PCPs, responses are computed with 100 keys and 10,000 plaintexts. PCPs not part of the training set are used for cross-validation. Scalability experiments are conducted on a 6-stage, 64-bit input BS-PUF; delay matrix of this BS-PUF is the top left 64 \times 6 sub-matrix of the 8-stage delay matrix.

![Fig. 12. Percentage of bit flips under temperature variation. Flip rates demonstrate signal-to-noise ratio (SNR) under different temperatures. Flip rates of LSB are shown in blue. Flip rates of 2nd LSB are shown in green.](image)

![Fig. 13. Percentage of bit flips under voltage variation. Flip rates of LSB are shown in blue. Flip rates of 2nd LSB are shown in green.](image)

| Method | Bit Length | Prediction Rate | PCPs | Training Time |
|--------|------------|-----------------|------|---------------|
| LR     | 64         | 17.5%           | 800  | 0.0203 sec    |
|        |            | 28.6%           | 8,000| 0.3580 sec    |
|        |            | 58.3%           | 80,000| 1.3157 sec   |
| LR     | 256        | 9.1%            | 1000 | 0.0186 sec    |
|        |            | 18.3%           | 10,000| 0.3670 sec   |
|        |            | 25.5%           | 100,000| 2.3212 sec  |

**TABLE V**

LR ON LSB WITH 6 AND 8 STAGES BS-PUFs
TABLE VI
LR ON 2ND LSB WITH 6 AND 8 STAGES BS-PUFs

| ML Method | Bit Length | Prediction Rate | PCPs | Training Time |
|-----------|------------|-----------------|------|---------------|
| LR        | 64         | 43.2%           | 800  | 0.0315 sec    |
|           |            | 52.6%           | 8000 | 0.1658 sec    |
|           |            | 79.5%           | 80000| 1.0104 sec    |
| LR        | 256        | 32.4%           | 1000 | 0.0157 sec    |
|           |            | 41.0%           | 10000| 0.4620 sec    |
|           |            | 62.8%           | 100000| 1.6245 sec   |

acquired from Monte Carlo Sampling. The number of CRPs $N_{CRP}$ that are required to learn a $k$-stage arbiter PUF with error rate $\epsilon$ is $0.5 \times (k+1)/\epsilon$ [44]. Thus, for a 6 stage BS-PUF, we also scale down $n$ to 8, 80, and 800 PCPs per key.

Table V and Table VI show the prediction accuracy of LR on LSB and 2nd LSB. LR is implemented by an iterative program written in Matlab. The regression coefficients’ initial values are set to (0, 0) in all LR applications. Silicon stability of BS-PUFs is 75%. Thus, all modeling reaching a higher prediction rate should be considered a success.

LSB provides better result than 2nd LSB. LR achieves 79.5% prediction rate for 6-stage BS-PUF 2nd LSB output. If 2nd LSB is used as the delay bit, then LR can successfully model 6-stage BS-PUF with sufficient number of PCPs. On the other hand, with the same modeling process, LSB cannot be modeled even with a large number of training samples. This is expected as the LSB is inherently more variable. Consequently, the choice to use LSB or 2nd LSB for the delay bit presents a tradeoff between security and reproducibility; LSB provides the former while 2nd LSB provides the latter.

B. Speed Performance

One of the most important advantages of BS-PUFs based encryption is its faster encryption than other traditional symmetric encryption schemes, such as AES. In this section, comparison is made between BS-PUFs encryption and AES.

BS-PUF based encryption outperforms conventional AES implementations. Some exceptions relying on high-speed crypto processors and architectures exist [39]. Performing AES Encryption on a modern Intel Pentium Pro processor requires 18 clock cycles per byte. Decryption takes even more cycles with a conservative estimate of 36 clock cycles per byte for encryption/decryption round-trip. This time increases as the block size increases. Comparatively, BS-PUF-based encryption (1.6 clock cycles per byte per BS-PUF resulting in 6.4 clock cycles for both encryption/decryption) is an order of magnitude improvement. In addition, BS-PUF-based encryption scales better, because encryption delay is near-constant ($\log n$ delay for block size $n$) regardless of block length.

This work proposes a protocol for data transmission using BS-PUF. It necessitates multiple-message round transaction between sender and receiver. This incurs transmission overhead.

The BS-PUF protocol has advantages over AES in encryption speed.

C. Area Needs

BS-PUF does very little mathematical computation; protection is provided by the physical properties of the encryption device. Little area is required due to this simplicity. In comparison, AES performs many more computations requiring greater area.

According to [40], 32-bit FPGA-based AES encryption contains 8,300 2-input NAND gate equivalents. A 32-bit BS-PUF requires 2,400 transistors, which is 600 2-input NAND gate equivalents. This evaluation is not technology dependent.

VIII. Future Work

Much needs to be addressed to establish the practicality of commutative PUFs. An evaluation of PUFs based on more relevant permutation families such as Keccak sponge family [23], [24] is needed. Overhead of reversible implementations, which also offer invertibility, of these functions need to be assessed. With invertibility, asymmetric encryption is also feasible. We are exploring asymmetric encryption direction. Another important research direction is quantification of security offered by BS-PUF vs AES.

The impact of PUF noise requires more discussion. The proposed design uses raw PUF responses; it will therefore be noisier than traditional PUFs. An error coding scheme using helper data and some form of fuzzy extraction is required.

Once we have designs for a realistic permutation family, similar evaluations are needed for their robustness. Path delay distributions across chips need to show variability and uniqueness; within the same PUF different paths need to show variability and randomness; temperature and supply voltage caused delay variation needs to be small enough. In addition, resource needs for these implementations need to be evaluated in terms of area, time and energy. The timer for input capture may impose an insignificant overhead. Its accuracy plays a central role in feasibility of BS-PUFs.

IX. Conclusions

In this work, we explore variety of encryption protocols based on commutative PUFs and propose a circuit implementation of the required commutative PUFs (BS-PUF). Commutativity relies on symmetric delays in forward and backward paths regardless of the message bit state. Spectre Monte Carlo simulations indicate only less than 1 bit delay offset is introduced by plaintext bit state variation. This ensure the commutativity of the system. Simulation shows that inter-chip variability (up to $\pm 25\%$ chip-to-chip variation) is acceptable. These encryption PUFs have potential to root the encryption in hardware, hence increasing robustness beyond current software only solutions.

Asymmetric encryption methods are valued for their ability to establish a secure communication channel in the absence of a priori shared secret. Such methods require complex
computations resulting in low throughput compared to symmetric encryption. BS-PUF has the potential to provide an asymmetric encryption method with performance similar to AES (symmetric encryption).

Basing encryption in hardware limits the attack surface. An adversary cannot retrieve the message even when both encryption key and ciphertext are known; information about the PUF behavior is not available to them. The behavior of the encryption function becomes a secret. Thus, more entropy is added to the system. Besides, BS-PUF based encryption provides much better speed and area performance than AES.

REFERENCES

[1] G. E. Suh and S. Devadas, “Physical unclonable functions for device authentication and secret key generation,” in Proceedings of the 44th annual Design Automation Conference. ACM, 2007, pp. 9–14.

[2] I. Hashmi and H. M. H. Babu, “An efficient design of a reversible barrel shifter,” in HLSI Design, 2010. VLSID’10. 23rd International Conference on, IEEE, 2010, pp. 93–98.

[3] Q. Ma, E. F. Young, and K.-P. Pun, “Analog placement with common centroid constraints,” in Computer-Aided Design, 2007. ICCAD 2007. IEEE/ACM International Conference on. IEEE, 2007, pp. 579–585.

[4] A. Rukhin, J. Soto, J. Nechvatal, E. Barker, S. Leigh, M. Levenson, D. Banks, A. Heckert, J. Dray, S. Vo et al., “Statistical test suite for random and pseudorandom number generators for cryptographic applications, nist special publication,” 2010.

[5] T. Takagi, “Fast rsa-type cryptosystem modulo p k q,” in Advances in CryptologyCRYPTO’98. Springer, 1998, pp. 318–326.

[6] D. Boneh et al., “Twenty years of attacks on the rsa cryptosystem,” Notices of the AMS, vol. 46, no. 2, pp. 203–213, 1999.

[7] Q. Chen, G. Csaba, X. Ju, S. Natarajan, P. Lugli, M. Stutzmann, G. Bertoni, J. Daemen, M. Peeters, and G. Van Assche, “The keccak sponge function family,” Technical Report, 2016.

[8] K. Fruhashi, M. Shiozaki, A. Fukushima, T. Murayama, and T. Fujino, “The arbiter-puf with high uniqueness utilizing novel arbiter circuit with delay-time measurement,” in Circuits and Systems (ISCAS), 2011 IEEE International Symposium on. IEEE, 2011, pp. 2325–2328.

[9] K. Loefstrom, W. R. Daasch, and D. Taylor, “Ic identification circuit using device mismatch,” in Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International. IEEE, 2000, pp. 372–373.

[10] N. S. Ronan, A. Martinez, A. R. Brown, J. R. Barker, and A. Asenov, “Current variability in si nanowire mosfets due to random dopants in the source/drain regions: A fully 3-d nefg simulation study,” IEEE Transactions on electron devices, vol. 56, no. 7, pp. 1388–1395, 2009.

[11] C. M. Bishop, “A 8-bit avr microcontroller with 128kb in-system programmable flash, atmega 128,” Technical Report, 2006.

[12] M. Gao, K. Lai, and G. Qu, “A highly flexible ring oscillator puf,” in Proceedings of the 51st Annual Design Automation Conference. ACM, 2014, pp. 1–6.

[13] R. Kumar, V. C. Patil, and S. Kundu, “On design of temperature invariant physically unclonable functions based on ring oscillators,” in VLSI (VLSI), 2012 IEEE Computer Society Annual Symposium on. IEEE, 2012, pp. 165–170.

[14] V. Vivekraj and L. Nazhandali, “Feedback based supply voltage control for temperature variation tolerant puf,” in VLSI Design (VLSI Design), 2011 24th International Conference on. IEEE, 2011, pp. 214–219.

[15] U. Rühmair, F. Sehne, J. Sölter, G. Dror, S. Devadas, and J. Schmidhuber, “Modeling attacks on physical unclonable functions,” in Proceedings of the 17th ACM conference on Computer and communications security. ACM, 2010, pp. 237–249.

[16] C. M. Bishop, Pattern recognition and machine learning, springer, 2006.

[17] T. Back, “Evolutionary algorithms in theory and practice: evolution strategies, evolutionary programming, genetic algorithms,” Oxford university press, 1996.

[18] ——, Evolution and optimum seeking: the sixth generation. John Wiley & Sons, Inc., 1993.

[19] C. P. Robert, Monte carlo methods. Wiley Online Library, 2004.

[20] X. Zhang and K. K. Parhi, “High-speed vlsi architectures for the aes algorithm,” IEEE transactions on very large scale integration (VLSI) systems, vol. 12, no. 9, pp. 957–967, 2004.

[21] P. Hamalainen, T. Alho, M. Hannikainen, and T. D. Hamalainen, “Design and implementation of low-area and low-power aes encryption hardware core,” in Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on. IEEE, 2006, pp. 577–583.