Effects of ageing on the electrical characteristics of Zn/ZnS/n-GaAs/In structure

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Effects of ageing on the electrical characteristics of Zn/ZnS/n-GaAs/In structure

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Abstract. Zn/ZnS/n-GaAs/In structure has been fabricated by the Successive Ionic Layer Adsorption and Reaction (SILAR) method and the influence of the time dependent or ageing on the characteristic parameters are examined. The current-voltage (I-V) of the structure have been measured immediately, 1, 3, 5, 15, 30, 45, 60, 75, 90, 105, 120, 135, 150 and 165 days after fabrication of this structure. The characteristics parameters of this structure such as barrier height, ideality factor, series resistance are calculated from the I-V measurements. It has been seen that the changes of characteristic parameters such as barrier height, ideality factor and series resistance of Zn/ZnS/n-GaAs/In structure have lightly changed with increasing ageing time.

1. Introduction
Metal-semiconductor contacts (MS) have been extensively studied on GaAs which is already largely used in industry and laboratories [1-3]. MS contacts are the basis of large number of compound semiconductor electronic devices, including microwave diodes, field-effect transistors (FETs), solar cells, photo detectors. In addition, the thermal stability of metal-semiconductor contacts is of great importance in device technology because they usually have to be subjected to elevated temperatures at some stage of manufacture of the device [3-6].

The SILAR method [7,8] is based on successive adsorption and reaction of species on the substrate surface from aqueous solutions. In the SILAR method, the substrate is immersed into separate cation and anion precursor solutions and rinsed with purified water after each immersion. The SILAR method is suitable for growing thin multilayer structure due to low deposition temperature since diffusion of ions in the thin film is low. Also among various deposition techniques, SILAR method is simple, less expensive and less time consuming for preparation of thin semiconductor chalcogenide films.

In this study Zn/ZnS/n-GaAs/In structure has been fabricated directly on n-GaAs semiconductor by the SILAR method. After the device fabrication, its performance and stability depending on time are important matters in the device manufacturing. Therefore, the purpose of this paper is to characterize how the I-V characteristics parameters such as barrier height, ideality factor, series resistance and so on of Zn/ZnS/n-GaAs/In structure have changed with increasing ageing time. The I-V measurements of the structure have been carried out under laboratory conditions in dark at room temperature.

2. Experimental process and data analysis
The Zn/ZnS/n-GaAs/In structure used in this study were fabricated using n-type single crystal n-GaAs wafer with (100) surface orientation and 2.5x10¹⁷ cm⁻³ carrier concentration. n-GaAs wafer was sequentially cleaned with trichloroethylene (CHCl₃CCl₂), acetone (CH₃COCH₃) and methyl alcohol (CH₃OH), etched in a sequence of sulfuric acid (H₂SO₄) and hydrogenperoxide (H₂O₂) and finally de-ionized water of resistivity of 18MΩ cm for a prolonged time, before the Zn/ZnS/n-GaAs/In structure fabrication process. During to each cleaning step, the wafer was rinsed thoroughly in de-ionized water. After surface cleaning of n-GaAs, high purity in was coated with at a pressure about 10⁻⁵ Torr in high vacuum system. To perform the ohmic contact, n-GaAs wafer was annealed at 425 °C for 3 min. After ohmic contact was made, the ohmic contact side and the edges of the n-GaAs semiconductor substrate was covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed...
to the cationic precursor solution employed for SILAR method. To deposit ZnS one SILAR growth cycle involves the following four steps: A well-cleaned glass substrate is immersed in the first reaction vessel containing aqueous cation precursor 0.1M ZnCl2 solution at pH 5.5. After the cation immersion, the substrate is moved to the rinsing vessel where it is washed with purified water. The sulfide ions were adsorbed from an aqueous 0.05 M Na2S solution with pH 12. After anion immersion the substrate was washed as described above, thus the first SILAR growth cycle is finished. The above cycle was repeated and the optimized dipping was 45 dipping times to get enough film thickness. Zn dots with diameter of about 1.0 mm were evaporated on the ZnS thin film in vacuum coating unit at about 10-5 torr. In this way, Zn/ZnS/n-GaAs/In sandwich structure was obtained.

The I-V characteristics of this structure were measured immediately using a HP 4140B picoampermeter and a HP model 4192A LF impedance analyser, respectively, at room temperature in the dark. The measurements were also repeated 1, 3, 5, 15, 30, 45, 60, 75, 90, 105, 120, 135, 150 and 165 days after fabrication of the Zn/ZnS/n-GaAs/In structure in order to observe the effect of the ageing.

3. Results and discussion

Figure 1 shows the forward and reverse bias I-V curves measured immediately, 1, 3, 5, 15, 30, 45, 60, 75, 90, 105, 120, 135, 150 and 165 days after fabrication of the Zn/ZnS/n-GaAs/In structure. A standard Schottky barrier theory can explain with I-V curve, where the forward current is due to the injection of majority carriers from the semiconductor into the metal, while the reverse current is due to the thermal emission of electrons over the barrier $\Phi_b$ from metal to the conduction band of the semiconductor and can be given by a simple equation [1]

$$I = I_s \exp \left[ \frac{qV}{nkT} - 1 \right]$$

(1)

where $I$ is the current density, $V$ the voltage, $q$ the electronic charge, $k$ the Boltzmann constant, $n$ is the ideality factor and $I_s$ is the saturation current. In Schottky theory, $I_s(T)$ is mainly determined by the barrier height $\Phi_b$ and the effective Richardson constant $A^*$:

$$I_s = AA^*T^2 \exp \left( -\frac{q\Phi_b}{kT} \right)$$

(2)

and hence

$$\Phi_b = \frac{kT}{q} \ln \left( \frac{AA^*T^2}{I_s} \right)$$

(3)

The slope of linear portion of the ln(I-V) curve gives the ideality factor and can be express as below [1]

$$n = \frac{q}{kT} \ln \left( \frac{dV}{d \ln I} \right)$$

(4)

The barrier height value of Zn/ZnS/n-GaAs/In structure was calculated with the help of Eq. (2) from the y-axis intercepts of the semilog-forward bias I–V plots, and the value of the ideality factor $n$ was obtained using Eq. (3) from the linear region of these plots.
**Figure 1.** The forward and reverse bias current–voltage characteristics of Zn/ZnS/n-GaAs/In structure as a function of ageing time.

**Figure 2.** The ideality factor and barrier height versus the increasing ageing time of Zn/ZnS/n-GaAs/In structure.
The values of $n$ and $\Phi_b$ parameters versus ageing time are shown in Figure 2. While $n$ decreases with an increase in ageing time, $\Phi_b$ increases, as seen from Figure 2. The ideality factor, $n$, is introduced to take into account the deviation of the experimental I-V data from the ideal TE model. This can be attributed to the interfacial layer of ZnS layer on the n-GaAs surface. For MS contacts it is known that the contact characteristics are controlled by Fermi level pinning due to the interface states. That is, it can be concluded that the barrier height determined from the I-V characteristics is controlled by the interface states in equilibrium with the semiconductor [9].

Norde proposed a method to determine value of the series resistance. The following function has been defined in the modified Norde’s method [10]:

$$F(V) = \frac{V}{\gamma} - kT \frac{\ln \left( \frac{I(V)}{A A^* T^2} \right)}{e}$$

(5)

where $\gamma$ is the first integer (dimensionless) greater than $n$. factor, $I(V)$ is current obtained from the I–V curve and the other parameters are described above. From Norde’s functions, the effective barrier height and $R_s$ value can be determined as

$$\Phi_b = Fm + \left[ \frac{(\gamma - n)}{n} \right] \left[ \frac{V_m}{\gamma} - \frac{kT}{e} \right]$$

(6)

$$R_s = (\gamma - n) \left( \frac{kT}{e I_m} \right)$$

(7)

![Figure 3. Experimental F(V)–V curves of Zn/ZnS/n-GaAs/In sandwich structure with increasing ageing time](image-url)
Figure 4. Series resistance versus the increasing ageing time of Zn/ZnS/n-GaAs/In structure.

Figure 3 shows the $F(V)$–$V$ plots of the Zn/ZnS/n-GaAs/In structure as a function of ageing time. From the $F(V)$–$V$ plots, the some parameters of the Zn/ZnS/n-GaAs/In sandwich structure, ($\Phi_b$, $R_s$) have been determined. It is seen that the values of the series resistance have increased with ageing time in Figure 4. The reason of this increase is that the doping agent in ZnS is gradually replaced by oxygen, which leads to a slow decrease of its conductivity. In addition to the ZnS layer, the time scale of the ageing may partly suggest an ionic activity within the thin film on n-GaAs semiconductor surface and it can be attributed to the migration of charged ions through the thin layer [9].

In this study, Zn/ZnS/n-GaAs/In structure has been fabricated by the Successive Ionic Layer Adsorption and Reaction (SILAR) method. The I-V characteristics of Zn/ZnS/n-GaAs/In structure have been investigated as a function of the ageing time. The characteristic parameters such as barrier height, ideality factor, series resistance of structure are calculated from the I-V measurement. The ageing effect has been attributed to anionic activity within the thin film on n-GaAs.

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