Advancing the State-of-the-Art in Hardware Trojans Design

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Abstract—Modern electronic systems heavily use third party IP (intellectual property) cores as their basic building blocks. An IP core is a reusable block of logic, tailored to perform a particular operation in an efficient manner, that is an intellectual property of one party. Optimized for area and performance, the IP cores are essential elements of design reuse in electronic design automation (EDA) industry and save a lot of resources to redesign the components from scratch. UARTs, DSP units, Ethernet controllers and PCI interfaces etc. are some examples of the IP cores [1].

The IP cores are typically offered either in a hardware description language (e.g., Verilog or VHDL) as synthesizable RTL (also called ‘open source’ IPs) or as generic gate-level netlists (also called ‘closed source’ IPs). These IP cores give rise to a critical security problem: how to make sure that the IP core does not contain a Hardware Trojan (HT)? A (compromised) IP core vendor acting as an adversary could implant a malicious circuitry in the IP core for privacy leakage or denial of service attacks.

A significant amount of research has been done during the past decade to design efficient tools for HT detection. Hicks et al. [2] proposed Unused Circuit Identification (UCI) which centers on the fact that the HT circuitry mostly remains inactive within a design, and hence such minimally used logic can be distinguished from the other parts of the circuit. However later works [3, 4] showed how to design HTs which can defeat the UCI detection scheme. Zhang et al. [5] and Waksman et al. [6] proposed detection schemes called VeriTrust and FANCI respectively and showed that they can detect all HTs from the TrustHub [7] benchmark suite. Yet again, the most recent technique called DeTrust [8] introduces new Trojan designs which can evade both VeriTrust and FANCI.

The reason behind this cat-and-mouse game between attackers and defenders is that the current HT detection tools offer critically low HT coverage and typically only cover a small constant set of publicly known HT benchmarks such as TrustHub. Whereas an adversary may design new HTs which are different from the publicly known HTs in that they can bypass the detection tool, as demonstrated by DeTrust [8]. It is unclear to what extent the existing HT detection tools are effective for publicly unknown HTs.

The first and foremost challenge in designing an effective HT detection technique is to define the scope of the countermeasure on the landscape of HTs. The HT taxonomies can be used for this purpose. Bhunia et al. [9] presents a taxonomy of HTs based on an extensive survey of the existing literature. The trigger based HTs are subdivided into digital and analog categories where digital HTs have two general models, combinational and sequential HTs. Combinational HTs are those whose trigger circuitry is simply a comparator whereas sequential HTs have memory elements as well in their trigger circuitry. Trojans are also classified based on payloads, i.e. digital, analog and others such as denial of service.

Since we are talking about digital IP cores, in this paper we limit ourselves to trigger activated digital HTs which have digital payloads. The Trojans that are always active...
and/or exploit side channels for their payloads are out of scope of this paper.

Even though existing HT taxonomies, such as the one mentioned above, provide significant knowledge about the HT properties, yet this information is quite fundamental and does not provide detailed characteristics vital for the HT countermeasures to provide strong security guarantees. This limitation may lead to uncertainties and potentially misleading information about the detection coverage that a HT countermeasure can provide.

This paper introduces four crucial properties ($d$, $t$, $\alpha$, $l$) of a large and complex class $H_D$ of trigger activated and deterministic digital HTs. These properties, determining the stealthiness of HTs, lead to a much more detailed classification of such HTs and hence assign well defined boundaries to the scope of the existing and new countermeasures on the huge landscape of HTs. In our model, $H_D$ represents the HTs which are embedded in a digital IP core whose output is a function of only its input, and the algorithmic specification of the IP core can exactly predict the IP core behavior. A brief highlight of the properties of $H_D$ is as follows:

- **$d$: Trigger Signal Dimension** represents the number of wires used by HT trigger circuitry to activate the payload circuitry in order to exhibit malicious behavior. Large $d$ shows a complicated trigger signal, hence harder to detect.

- **$t$: Payload Propagation Delay** is the number of cycles required to propagate malicious behavior to the output port after the HT is triggered. Large $t$ means it takes a long time after triggering until the malicious behavior is seen, hence less likely to be detected during testing.

- **$\alpha$: Implicit Behavior Factor** represents the probability that given a HT gets triggered, it will not (explicitly) manifest malicious behavior; this behavior is termed as implicit malicious behavior. Higher probability of implicit malicious behavior means higher stealthiness.

- **$l$: Trigger Signal Locality** shows the spread of trigger signal wires of the HT across the IP core. Small $l$ shows that these wires are in the close vicinity of each other. Large $l$ means that these wires are spread out in the circuit, hence the HT is harder to detect.

Based on the above mentioned parameters, we introduce a new stealthy HT, coined the XOR-LFSR, which cannot be efficiently detected by ordinary means (design knowledge of the HT itself needs to be incorporated in the detection tool). We also show that the current publicly known HTs have small $d$ (mostly $d = 1$ for TrustHub) and hence they are the simplest ones. Fig. 1 depicts a pictorial representation of the HT class $H_D$ that includes TrustHub. Although VeriTrust and FANCI can detect TrustHub HTs, it is unclear what security guarantees they offer outside TrustHub.

The rest of this paper is organized as follows. Section 2 introduces several advanced properties of this class which lead to new HT design methodologies.

## 2 Background & Definitions

A digital IP core can fall under one of the following three categories, as shown in Fig. 2 based on its level of conformity to the design specifications; (1) containing A Hardware Trojan, or (2) containing An Exploit, or (3) exhibiting Normal Behavior.

### 2.1 Hardware Trojan

A Hardware Trojan (HT) is malicious extra circuitry embedded inside a larger circuit, which results in data leakage or harm to the normal functionality of the circuit once activated. We define extra circuitry as redundant logic added to the IP core without which the core can still meet its design specifications. A trigger activated HT activates upon some special event, whereas an always active HT remains active all the time to deliver the intended payload.

Trigger activated HTs typically consist of two parts: a trigger circuitry and a payload circuitry. The trigger circuitry is implemented semantically as a comparator which compares the value(s) of certain wire(s) of the circuit with a specified boolean value called trigger condition. The HT trigger circuitry sends its comparator’s output to the payload circuitry over certain other wire(s) called the trigger signal. Once the trigger signal is asserted, the payload circuitry performs the malicious operation called ‘payload’ as intended by the adversary.

2. Design specifications can also cover the performance requirements of the core, and hence pipeline registers etc. added to the core only for performance reasons can also be considered as ‘necessary’ to meet the design specifications and will not be counted towards ‘extra’ circuitry.
**Definition 1. Trigger condition** refers to an event, manifested in the form of a particular boolean value of certain internal/external wires of the circuit, which activates the HT trigger circuitry.

**Definition 2. Trigger signal or Trigger State** refers to a collection of physical wire(s) which the HT trigger circuitry asserts in order to activate the payload circuitry once a trigger condition occurs.

The trigger signal must not be confused with trigger condition; trigger condition is an event which causes the HT activation, whereas trigger signal is the output of trigger circuitry which tells the payload circuitry to show malicious behavior.

Fig. 3 shows an example of a simple HT embedded in a half adder circuit. The HT-free circuit in Fig. 3a generates a sum $S = A \oplus B$ and a carry $C = A \cdot B$. The HT, highlighted in red in Fig. 3b, triggers when $A = B$ and produces incorrect results i.e. $S = B$ for $A = B$ and $S = A \oplus B$ for $A \neq B$. Notice the difference between the trigger condition $A = B$, and the trigger signal $Sel$ which only becomes 1 when the trigger condition is satisfied.

The Trojan affected circuit in Fig. 3b produces a malicious output $S = 1$ for trigger condition $A = B = 1$ which is distinguishable from otherwise normal output ($S = 0$). However, the same circuit produces a (so called) malicious output $S = 0$ for trigger condition $A = B = 0$ which is the same as otherwise normal output and cannot be distinguished from the ‘normal’ behavior of the circuit. This observation leads us to the definition of *explicit* vs. *implicit* malicious behaviors:

**Definition 3. Explicit malicious behavior** refers to a behavior of a HT where the HT generated output is distinguishable from a normal output.

**Definition 4. Implicit malicious behavior** refers to a behavior of a HT where the HT generated output is indistinguishable from a normal output.

Notice that an adversary may exploit the implicit malicious behavior to bypass functional testing based detection tools during the testing phase. Once the infected circuit has passed the testing and is deployed, it can then manifest explicit malicious behavior to actually deliver the payload. In other words, implicit malicious behavior can lead to a false negative.

**Definition 5. False Negative** refers to a scenario when a HT detection tool identifies a circuit containing a HT as Trojan-free or transforms a circuit containing a HT into a circuit which still allows the HT to express implicit or explicit malicious behavior.

Clearly, all existing dynamic analysis (i.e. functional testing) based approaches which assume that a HT is never triggered during the functional testing phase can suffer from false negatives because of the implicit malicious behavior. Neglecting the implicit malicious behavior could lead to devastating consequences in a security critical application, e.g. if an adversary designs a HT to significantly increase the probability of implicit malicious behavior and thus alleviates the existing HT detection techniques.

### 2.2 An Exploit

An exploit refers to a loophole in the specifications or implementation of an IP core which allows an adversary to manipulate it beyond its intended specifications. Notice that an exploitable IP core does not have ‘extra’ circuitry like a Hardware Trojan. Depending upon the nature of the exploits, they can also deliver the payloads like Hardware Trojans such as privacy leakage or denial of service etc. Some examples of exploits are as follows: a wireless connection that can be overloaded may lead to a denial of service, a broken AES module due to a predictable key, recent OpenSSL Heartbleed bug etc. This paper only focuses on rigorous reasoning about Hardware Trojans (not exploits).

### 3 Characterization of Hardware Trojans

In this section, we characterize the trigger activated HTs based on their following fundamental characteristics that lead to a clear distinction between the deterministic $H_D$ and non-deterministic $H_{ND}$ types.

#### 3.1 $St$ vs. $Si$ Hardware Trojans

Hardware Trojans are first grouped based on the payload channels they use once activated as shown in Fig. 4. $St$ refers to the Trojans using only standard I/O channels (this includes LED outputs etc.) whereas $Si$ represents the Trojans which also use side channels to deliver the payload. I/O channels are generally used to communicate binary payloads $b_j$ at certain times $t_j$ for the duration of the execution of the IP core. In this sense the view of an I/O channel can be represented as a sequence $(b_1, t_1), (b_2, t_2), \ldots, (b_N, t_N)$. Its information is decomposed in three channels: the binary channel corresponding to $(b_1, b_2, \ldots, b_N)$, the timing channel corresponding to $(t_1, t_2, \ldots, t_N)$, and the termination channel $N$ which reveals information about the duration.
of the execution of the IP core. If a Trojan delivers some of its payload over the timing channel (or other side channels), then we define it to be in $St$. If a Trojan delivers all of its payload using the standard usage of I/O channels (the binary and termination channels), then we define it to be in $St$. E.g., a HT causing performance degradation in terms of slower response/termination times due to slower computation (denial of service in the most extreme case) is in $St$.

3.2 $H_D$ vs. $H_{ND}$ Hardware Trojans

We further refine our description of $St$ Trojans by subdividing them in $H_D$ and $H_{ND}$ groups based on the IP core behavior in which they are embedded and their algorithmic specifications.

**Definition 6.** $H_D$ Trojans are the ones which are:
1) Embedded in an IP core whose output is a function of only its input – i.e., the logical functionality of the IP core is deterministic, and
2) The algorithmic specification of the IP core can exactly predict the IP core behavior.

If any of the two above mentioned conditions is not satisfied for a $St$ type HT then we consider the HT to be in $H_{ND}$. A true random number generator (TRNG), for example, is a non-deterministic IP core whose output cannot be predicted and verified by logic testing against an expected output. Any $St$ Trojan in such a core is considered $H_{ND}$. A pseudo random number generator (PRNG), on the other hand, is considered a deterministic IP core as its output depends upon the initial seed and is therefore predictable by a logic based testing tool (hence $H_D$). Similarly, if the algorithmic specification allows coin flips generated by a TRNG then we consider the Trojan to be $H_{ND}$. On the other hand, if the coin flips are generated by a PRNG then we regard the Trojan as $H_D$.

The non-deterministic behavior of IP cores and/or their functional specification which accepts small probabilistic fluctuations within some acceptable range allows a covert channel for $H_{ND}$ Trojans to embed some minimal malicious payload in the standard output without being detected by an external observer. The external observer considers these small fluctuations as part of the functional specification. Hence, the non-deterministic nature of $H_{ND}$ Trojans prohibits the development of a logic testing based tool to detect these Trojans with overwhelming probability.

4 Advanced Properties of Class $H_D$

In the following discussion, we introduce some crucial properties of $H_D$ Trojans that characterize their complexity and stealthiness.

4.1 Trigger Signal Dimension $d$

When a trigger condition of a hardware Trojan occurs, regardless of the other subsequent user interactions, its trigger circuitry gets activated and outputs a certain binary value on a certain trigger signal $Trig$ to activate the payload circuitry which manifests malicious behavior. A trigger signal $Trig$ is represented as a labeled binary vector of one or more wires/registers/flip-flops (each carrying a 0 or 1), e.g., in the example circuit of Fig. 3, $Sel = 1$ is a trigger signal. In other words, $Trig$ represents a trigger state of the circuit through which the circuit must have passed before manifesting malicious behavior. Notice that the trigger state(s) can be associated back to the occurrence of the respective trigger condition(s). Hence a HT can be represented by a set of trigger states $T$; i.e. the states which always lead to malicious behavior (implicit or explicit).

**Definition 7.** A set $T$ of trigger states represents a HT if the HT always passes through one of the states in $T$ in order to express implicit of explicit malicious behavior.

Notice that $T$ is not unique. For example, $T$ could be $\{(Sel = 1)\}$, or if $Sel$ is somehow independent of $A$ and $B$, then it could also be $T = \{[(A, B) = (1, 1)], [(A, B) = (0, 0)]\}$ etc.

We define the trigger signal dimension $d$ of a HT represented by a set of trigger states $T$ as follows:

**Definition 8. Trigger Signal Dimension** $d(T)$ of a HT is defined as $d(T) = \max_{Trig \in T} |Trig|$.

In other words, the trigger signal dimension shows the width of the widest trigger signal bit-vector of a HT. E.g. for the HT from Fig. 3b. $d(T) = 1$ since the set of trigger states $T = \{(Sel = 1)\}$ only has the signal $Sel$ that activates the payload circuitry is only 1-bit wide (and hence easy to detect). In the next section, we show that one can design HTs with high dimensional trigger signals. Obviously, it becomes difficult to detect HTs which only have high dimensional sets of trigger states, i.e. large trigger signals. The set of possible values of a given trigger signal $Trig$ grows exponentially in $d = |Trig|$ and only one value out of this set can be related to the occurrence of the corresponding trigger condition. Clearly, since in theory $d$ can be as large as the number of wires $n$ in the IP core, $H_D$ represents an exponentially (in $n$) large class of possible HTs.

4.2 Payload Propagation Delay $t$

For a set $T$ which represents a HT, we know that if the HT manifests malicious behavior, then it must have transitioned through a trigger state $Trig \in T$ at some previous clock cycle. Therefore, we define the payload propagation delay $t$ as follows:

**Definition 9. Payload Propagation Delay** $t(T)$ of a hardware Trojan represented by a set of trigger states $T$ is defined as the maximum number of clock cycles taken to propagate the malicious behavior to the output after entering a trigger state in $T$.

I.e., the number of clock cycles from the moment when a trigger signal is asserted till its resulting malicious behavior shows up at the output port. E.g., consider a counter-based HT where malicious behavior immediately (during the same clock cycle) appears at the output as soon as a counter reaches a specific value. Then, $t(T(\{Trig\})) = 0$ for the trigger signal $Trig$ which represents the occurrence of the specific counter value (i.e. trigger condition). However, notice that any counter value $j$ clock cycles before reaching the ‘specific...
value’ can also be considered as a trigger signal $Trig$ with $t(\{Trig\}) = j$, because eventually after $j$ cycles this $Trig$ manifests the malicious behavior.

To detect a HT with a large value of $t(T)$, the memory requirement and complexity of logic testing based detection tool is increased. However, for any HT, typically there exists a set of trigger signals which represents the HT and which has a small $t$ because of a small number of register(s) between the trigger signal and the output port.

### 4.3 Implicit Behavior Factor $\alpha$

In addition to previously discussed properties of Trojans, the IP core in which the Trojan is embedded plays a critical role in its stealthiness. According to the definition of implicit malicious behavior, it may not always be possible to distinguish a malicious output from a normal output just by monitoring the output ports. Consequently, the implicit malicious behavior adds to the stealthiness of the HT since it creates a possibility of having a false negative under logic testing based techniques. We quantify this possibility by defining the implicit behavior factor $\alpha$ as follows:

**Definition 10. Implicit Behavior Factor $\alpha(T)$ of a HT**

represented by the set of trigger states $T$ is defined as $\alpha(T) = \max_{Trig \in T} \alpha(Trig)$ where $\alpha(Trig)$ shows the probability that, given the trigger state $Trig$ occurs, it will lead to implicit malicious behavior.

In other words, the higher the value of $\alpha$, the lower the chance of detection by logic testing even if the HT gets triggered and hence the higher the overall stealthiness of the HT. E.g. for the HT from Fig. 5(a) with the trigger condition $A = B$, if $(A,B) = (1,1)$ then the malicious output $S = 1$ is distinguishable from the normal output (i.e. $S = 0$). However for $(A,B) = (0,0)$, the malicious output $S = 0$ is indistinguishable from the normal output (i.e. $S = 0$), i.e. the implicit malicious behavior comes into the picture. Hence, given that this particular HT activates, the probability that the HT-generated (malicious) output is indistinguishable from the normal output is $\alpha(T) = 0.5$ which represents the implicit behavior factor of this HT.

### 4.4 Trigger Signal Locality $l$

We notice that the individual wires of a HT trigger signal of dimension $d$ are logically/physically located in the close vicinity of each other in the circuit netlist/layout. This is because eventually these wires need to coordinate (through some combinational logic) with each other to perform the malicious operation. Based on this observation, we introduce the idea of locality in gate level circuits, similar to the region based approach in [10].

Consider the simple combinational circuit from Fig. 5(a) whose nodes represent the wires of the circuit and each edge between any two nodes represents connectivity of the corresponding two wires through a combinational logic level. In other words, each logic gate of the circuit is replaced by multiple edges (three in this case) in the graph which connect together the nodes corresponding to its inputs and the output. For any two nodes (i.e. wires) $i$ and $j$ in a locality graph, we define $dist(i,j)$ as the shortest distance between $i$ and $j$. In other words, $dist(i,j)$ represents the minimum number of basic combinational or sequential logic levels (e.g. logic gates and/or flip flops) between wires $i$ and $j$. E.g. $dist(E,B) = dist(E,C) = 1$, whereas $dist(E,O) = dist(E,A) = 2$.

**Definition 11. Trigger Signal Locality $l(T)$ of a HT represented by the set of trigger states $T$ is defined as:**

$$l(T) = \max_{Trig \in T} \left( \max_{0 \leq i,j < |Trig|} \text{dist}(Trig[i],Trig[j]) \right)$$

where $Trig[i]$ represents the label of the $i_{th}$ wire in $Trig$.

A low value of $l(T)$ shows that the trigger signal wires of the HT are in the close vicinity of each other and vice versa. Having a notion of locality can significantly reduce the computational complexity of logic testing based HT detection tools.

### 4.5 Achievable Quadruples $(d,t,\alpha,l)$

A Hardware Trojan can be represented by multiple sets of trigger states $T$, each having their own $d$, $t$, $\alpha$, and $l$ values. The collection of corresponding quadruples $(d,t,\alpha,l)$ is defined as the achievable region of the Hardware Trojan.

The choice of parameters $d$ and $t$ significantly affects $\alpha$ of the HT. $\alpha$ as a function of $t$ and $d$ is decreasing in both $t$ and $d$. Reducing $t$ means that explicit malicious behavior may not have had the chance to occur, hence, the probability $\alpha$ that no explicit malicious behavior is seen increases. Similarly, reducing $d$ can increase $\alpha$ since as a result of smaller $d$, there may not exist a set of trigger signals $T$ that represents the HT and satisfies $d(T) \leq d$. Increasing $t$ or $d$ only decreases $\alpha$ down to a certain level; the remaining component of $\alpha$ represents the inherent implicit malicious behavior of the HT.
It can be seen in Fig. 6b that all individual wires related to the HT circuitry are continuously showing transitions without activating the HT during several clock cycles before reaching to the trigger condition (i.e. cycle 14). Therefore, clearly those existing logic testing based HT detection techniques which only look for simplistic one-dimensional HT (i.e. \( d = 1 \)) trigger signals do not see any ‘suspicious’ wire which is stuck at 0 or 1, and hence this HT is not detected unless it gets activated in a long testing phase. This shows that this HT has a trigger signal dimension \( d = 2 \) since two wires \( W_1 \) and \( W_2 \) together constitute the trigger signal. Since counter based HTs can have large counters, it may not always be feasible to activate them during testing. Consequently, in order to efficiently detect such HTs, the knowledge of such design parameters must be incorporated while designing the HT countermeasures.

5.2 An Advanced \( H_D \) Trojan: \( k\)-XOR-LFSR

Fig. 7 depicts \( k\)-XOR-LFSR, a counter based Trojan with the counter implemented as an LFSR of size \( k \). The Trojan is merged with the circuitry of an IP core which outputs the XOR of \( k \) inputs \( A_j \).

Let \( r^i \in \{0, 1\}^k \) denote the LFSR register content at clock cycle \( i \) represented as a binary vector of length \( k \). Suppose that \( u \) is the maximum index for which the linear space \( L \) generated by vectors \( r^0, \ldots, r^{u-1} \) (modulo 2) has dimension \( k - 1 \). Since \( \dim(L) = k - 1 < k = \dim(\langle 0, 1 \rangle^k) \), there exists a vector \( v \in \{0, 1\}^k \) such that, (1) the inner products \( \langle v, r^i \rangle = 0 \) (modulo 2) for all \( 0 \leq i < u - 1 \), and (2) \( \langle v, r^u \rangle = 1 \) (modulo 2). Only the register cells corresponding to \( v_j = 1 \) are being XORed with inputs \( A_j \).

Since the \( A_j \) are all XORed together in the specified logical functionality to produce the sum \( \sum_j A_j \), the Trojan changes this sum to

\[
\sum_j A_j \oplus \sum_{j:v_j=1} r^j = \sum_j A_j \oplus \langle v, r^i \rangle.
\]

I.e., the sum remains unchanged until the \( u \)-th clock cycle when it is maliciously inverted.

The trojan uses an LFSR to generate register values \( r^i \in \{0, 1\}^k \) for each clock cycle \( i \) and we assume in our analysis that all vectors \( r^i \) behave like random vectors from a uniform distribution. Then, it is unlikely that \( u \) is more than a small constant larger than \( k \) (since every new vector
r^i\ has\ at\ least\ probability\ 1/2\ to\ increase\ the\ dimension\ by\ one).\ Therefore,\ u \approx k,\ hence,\ the\ register\ size\ of\ the\ trojan\ is\ comparable\ to\ the\ number\ of\ clock\ cycles\ before\ the\ trojan\ is\ triggered\ to\ deliver\ its\ malicious\ payload.\ This\ makes\ the\ trojan\ somewhat\ contrived\ (since\ it\ can\ possibly\ be\ detected\ by\ its\ suspiciously\ large\ area\ overhead).

Since\ inputs\ A_j\ can\ take\ on\ any\ values,\ any\ trigger\ signal\ Trig\ must\ represent\ a\ subset\ of\ the\ LFSR\ register\ content.\ Suppose\ t(\{Trig\}) = j.\ Then\ Trig\ must\ represent\ a\ subset\ of\ r^{u-j}.\ We\ will\ proceed\ with\ showing\ a\ lower\ bound\ on\ d(\{Trig\}).\ Consider\ a\ projection\ P\ to\ a\ subset\ of\ d\ register\ cells;\ by\ r P\ we\ denote\ the\ projection\ of\ r\ under\ P,\ and\ we\ call\ P\ d-dimensional.\ If\ r^{u-j}\ \exists\ P \in \{r^i|P : 0 \leq i < u - j\},\ then\ the\ wire\ combination\ of\ the\ d\ wires\ corresponding\ to\ r^{u-j}\ \exists\ P\ cannot\ represent\ Trig\ (otherwise\ t(\{Trig\}) > j):\ if\ this\ is\ the\ case\ for\ all\ d\ dimensional\ P,\ then\ Trig\ cannot\ represent a\ subset\ of\ r^{u-j}.\ The\ probability\ that\ r^{u-j}\ \exists\ P \in \{r^i|P : 0 \leq i < u - j\}\ is\ at\ least\ equal\ to\ the\ probability\ that\ r^i|P : 0 \leq i < u - j\} = \{0,1\}^d,\ which\ is\ (by\ the\ union\ bound)

\[\geq 1 - \sum_{w \in \{0,1\}^d} Prob(\{r^i|P : 0 \leq i < u - j\} \subseteq \{0,1\}^d \setminus \{w\})\]

\[= 1 - \sum_{w \in \{0,1\}^d} (1 - 1/2^d)^{u-j} \approx 1 - 2^d e^{-(u-j)/2}d\]

Since\ there\ are\ \binom{d}{u} \leq k^d/d!\ projections,\ Trig\ cannot\ represent\ a\ subset\ of\ r^{u-j} with\ probability

\[\geq (1 - 2^d e^{-(u-j)/2}d)^k/d!\]

(1)

For\ d \leq \log(u-j) - \log(\log(u-j) \log k + \log \log k),\ this\ lower\ bound\ is\ about\ \geq 1/e.\ Since\ u \approx k\ and\ after\ neglecting\ the\ term\ \log \log k,\ this\ shows\ an\ approximate\ lower\ bound\ on\ d(\{Trig\}),\ i.e.,

\[\geq \log(k - t(\{Trig\})) - \log(\log(k - t(\{Trig\})) \log k)\]

This\ characterizes\ the\ stealthiness\ of\ the\ k-XOR-LFSR.

In\ other\ words,\ the\ stealthiness\ of\ k-XOR-LFSR\ can\ be\ increased\ with\ k\ within\ the\ acceptable\ area\ overhead\ limits.\ Fig. 8\ shows\ the\ lower\ bounds\ on\ d\ for\ this\ HT\ for\ fixed\ values\ of\ k\ and\ t;\ if\ t(\{Trig\}) = 0,\ then\ d(\{Trig\}) \geq \log k - 2 \log \log k.\ The\ HT\ can\ be\ designed\ for\ any\ point\ in\ the\ region\ above\ the\ lower\ bound.\ For\ the\ HT\ shown\ in\ Fig. 8\ clearly\ \alpha(Trig) = 0\ since\ it\ always\ produces\ incorrect\ output\ immediately\ once\ the\ HT\ gets\ triggered.

6 CHARACTERIZING TRUSTHUB BENCHMARKS

Trusthub [7] benchmark suite includes a wide variety of Hardware Trojans including trigger-activated and always-active Trojans; Trojans that use standard IO channels as well as side channels. In this section, we analyze the TrustHub benchmarks with respect to our definitional framework. As mentioned earlier, our \(D\) class of HTs covers majority of the relevant benchmarks from TrustHub. Here we present the values of design parameters (d, t, \(\alpha\)) for these benchmarks which provide a deeper insight about the stealthiness of these well known HTs.

TABLE 1 shows the relevant benchmarks from Trusthub categorized according to our framework. St-D group (i.e. \(D\) Trojans) is further subdivided based on the properties (d, t, \(\alpha\)). All these Trojans happen to be represented by a single trigger of dimension \(d = 1\) (i.e., the trigger is a single wire); whereas their corresponding \(t\) and \(\alpha\) values are listed in TABLE 1.

To determine \(t\) values of these trojans, we simply count the minimum number of registers between the trigger signal wires(s) and the output port of the IP core. Since precisely calculating \(\alpha\) can be almost impossible for large circuits, we estimate \(\alpha\) values through experiments. We argue that these estimated values closely represent the corresponding actual values of \(\alpha\), hence TABLE 1 fits the definition of \(\alpha\). In order to estimate \(\alpha\) values, we first find the smallest chain of logic gates starting from the trigger signal wire(s) till the output port of the IP core (ignoring any registers in the path). Then for each individual logic gate, we compute the probability of propagating a logic 1 (considering that the trigger wire(s) get a logic 1 upon a trigger event), e.g. an AND gate has

5. Not all of the benchmarks from TrustHub are listed in TABLE 1 because some of them have no payload, such as RS232-T200. Similarly the payloads of some other benchmarks are harmless which will be removed by synthesis tools. E.g. RS232-T1800, which just adds three inverters to waste energy.

6. \(\alpha\) values show estimated upper bounds on probabilities.
the probability 1/4 of propagating a logic 1, whereas an XOR gate has the probability 1/2. Finally we compute an aggregate probability of propagation by multiplying all the probabilities of each logic gate in the chain, which gives the value 1 − α.

Notice that all these St-D Trojans have a very low value of d (particularly d = 1) which reflects their low stealthiness, and hence the fact that these publicly available benchmarks represent only a small subset consisting of simple Trojans. Even though some of these benchmarks have high values of α (e.g. s38584-T100 and s38417-T200), however in practice, having a very high value of α may not always be useful for the adversary. Ideally, on one hand, the adversary wants the Trojan to be triggered in the logic testing phase only once, and remain undetected (i.e. by having high α) so that the Trojan trigger is whitelisted. On the other hand, after the testing phase, he wants the Trojan to deliver the payload by disrupting the normal output (i.e. by having low α), otherwise the Trojan is not useful for him. Therefore, the adversary would like to have a sweet spot between the high and low ends of α values.

St-ND (i.e. $H_{ND}$ group) and Si Trojans are out of scope of this paper. In our model, some TrustHub benchmarks, e.g. MC8051 series, are considered to be in $H_{ND}$ group because of their flexible design specifications. The specification of a processor is relatively flexible about the timing/ordering of outputs (e.g. instructions execution) due to some unpredictable factors like interrupt requests etc. This flexibility, however, makes it harder for logic testing based tools to verify the functional correctness of the design. However, if there exists a precise and strict model for these cores, such HTs can still be analyzed in our model.

7 RELATED WORK

Hardware trojans have recently gained significant interest in the security community [11, 12, 13]. The works [12] and [13] showed how malicious entities can exist in hardware, while Skorobogatov et al. [14] showed evidence of such backdoors in military grade devices. Nefarious designs have also been deployed and detected in wireless communications devices [15]. Recent works have mostly focused on detection [16] and identification schemes [17], which assess to what extent the pieces of hardware may be vulnerable, and how related trojans can be classified. State of the art HT detection schemes include UCI [2], VeriTrust [3], FANCI [3] and DeTrust [3]. Typically, HT detection techniques only show their detection capabilities for HTs from the TrustHub benchmarks suite, in which all trojans are explicitly triggered. This explicitness forgoes the lack of implicitness, due to which all the above schemes are able to detect the benchmarked trojans. These schemes, however, do not cater for higher dimensional ($d > 1$) trojans or the added stealthiness because of the implicit malicious behaviors (i.e. α). DeTrust presents a trojan example which bypasses other existing countermeasures, and interestingly it happens to have the dimension $d = 2$. However, this property has not been noticed or analyzed in that paper. We fill these gaps by providing a detailed and rigorous framework to reason about HT characteristics and their impact on the detection schemes.

Further works construct and detect HTs that use side channels [18, 19, 20]. Such HTs remain implicitly on, and have usually no effect on the normal functionality of the circuit. Side channels include power based channels [21], as well as heat based channels [22]. Power based HTs force the circuit to dissipate more and more power to either damage the circuit, or simply waste energy. Heat based HTs leak important information via heat maps [23], where highs and lows in heat dissipation can be interpreted as logic 1’s and 0’s. Our work only focuses on HTs that perturb standard I/O channels; analyzing side channel models/frameworks is out of scope of this paper.

8 Conclusion

We provide the first rigorous framework of Hardware Trojans within which “Deterministic Trojans”, the class $H_D$ is introduced. We discover several stealthiness parameters of the Hardware Trojans from $H_D$ which lead us to design a much more stealthy XOR-LSFR Hardware Trojan. This shows that the current publicly known Hardware Trojans are the simplest ones in terms of stealthiness, and hence they represent just the tip of the iceberg at the huge landscape of Hardware Trojans.

We conclude that our framework allows the Hardware Trojan research community to rigorously reason about the stealthiness of different Hardware Trojans and the effectiveness of existing countermeasures. The Hardware Trojan design principles introduced in this paper encourage and assist in designing new and even stronger countermeasures for highly stealthy and sophisticated Hardware Trojans.

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