Compressed optimization of device architectures

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Recent advances in nanotechnology have enabled researchers to control individual quantum mechanical objects with unprecedented accuracy, opening the door for both quantum and extreme-scale conventional computing applications. As these devices become larger and more complex, the ability to design them for simple control becomes a daunting and computationally infeasible task. Here, motivated by ideas from compressed sensing, we introduce a protocol for Compressed Optimization of Device Architectures (CODA). It leads naturally to a metric for benchmarking device performance and optimizing design devices, and provides a scheme for automating the control of gate operations and reducing their complexity. Because CODA is both experimentally and computationally efficient, it is readily extensible to large systems. We demonstrate the CODA benchmarking and optimization protocols through simulations of up to eight quantum dots in devices that are currently being developed experimentally for quantum computation.

Nanoscale devices are challenging to control in part because their size makes them susceptible to even the smallest materials defects. Quantum devices are especially challenging because their energy spectra and tunnel couplings both require fine tuning. Here we focus on quantum bits (qubits) formed of electron spins in electrostatically-gated quantum dot and donor. Such devices could potentially be be scaled up to large arrays by leveraging the mature semiconductor processing industry. Working in a variety of systems, researchers have already demonstrated complete control and excellent decoherence properties of devices with up to four quantum dot, as well as impurities coupled to electronic reservoirs.

Processing quantum information in semiconductors requires fine control of the energies and tunnel rates of the individual electrons. Voltages are simultaneously tuned on many top-gates to precisely shape the electrostatic potential landscape within a device. Unfortunately, gate geometries that work well for 1-2 qubits are not necessarily well suited for larger arrays. For example, gates designed to control a given dot will also affect its neighbors via capacitive crosstalk. While voltage compensation methods are used to manage crosstalk in smaller devices, hand tuning becomes impractical for larger arrays. Recent methods have been proposed to help automate this process, including optimized randomized benchmarking for immediate tune-up (ORBIT) and real-time Hamiltonian estimation. While promising, these schemes are software based, and are therefore constrained by the capabilities of the quantum device hardware.

In this paper, we aim to make the software problem more tractable through hardware optimization. We show how to systematically modify dot properties, such as occupations, energies, and tunnel rates, while changing as few voltages as possible – a strategy we refer to as control sparsity. The scheme relies on results and methods used for compressed sensing in the signal processing literature, in which the decoding of signals can be greatly optimized by exploiting their sparseness. To demonstrate these concepts, we implement the CODA protocol using realistic simulations of several quantum dot devices. We show that CODA yields solutions that are simultaneously sparse and spatially localized near the relevant dot – an extremely desirable property for scale-up. Moreover, formulating effective control as an optimization problem allows us to directly compare the effectiveness of different gate architectures, enabling optimization of the device designs themselves.

Our method is sketched in Fig. 1. For qubit applications, typical properties we wish to control are the quantum dot occupations and the tunnel rates between the dots, although other properties may also be of interest. Such properties are referred to as operational targets. Generally, an operational target could be composed of several physical attributes; we therefore represent it as a vector $t$ in a vector space of outputs $T$. The outputs are determined by the voltages applied to the electrostatic top-gates. A given set of voltages is referred to as a control setting, represented as a vector $c$ in a vector space of controls $C$. A physical system is represented as a function that maps the controls to the targets: $\hat{S} : C \rightarrow T$. Although this mapping is generally nonlinear, we can make the assumption that device operations typically occur near a desired working point, allowing us to linearize $\hat{S}$ around that point. In general, many different $c$ can yield a desired $t$. Our goal is to identify solutions that involve as few voltage changes as possible.

This problem is exactly suited to compressed sensing techniques: we are given an underdetermined linear map-
FIG. 1. Illustration of the CODA procedure for characterizing and optimizing nanoscale device designs. a. The physical device determines the response of the operational targets to the physical controls. As an example, we show a schematic of a Si/SiGe electrostatically defined quantum dot qubit device. Metal control gates on the device surface are used to accumulate and control a two-dimensional electron gas (2DEG) in the Si quantum well, forming a double quantum dot. The gate voltages are adjusted to tune the device to a predetermined working point of experimental interest. b. Linearized model. Once a working point is determined, the configuration is probed by varying the control gate voltages and noting the response of target variables of interest (e.g. quantum dot occupations and tunnel couplings). This yields a cross-covariance matrix describing the linear response of the system about the working point. c. Optimal control vector. Since there are more controls than targets, the inverse problem yields a subset of valid control vectors for every operational target. By imposing L1 regularization, we can identify solutions that are both local and sparse. This regularization provides a metric for comparing different gate designs.

Results from compressed sensing show that the control vectors produced by this method are indeed sparse, however the question of locality has not been addressed. We first give an intuitive argument for why CODA yields solutions that are local, and then provide a numerical demonstration of the fact. We consider a classical scenario in which the dot couplings are purely capacitive. Since the capacitive coupling between a dot and a gate decays inversely with separation, gates that are far away tend to require large voltage changes to achieve the same response as closer gates. The L1 norm in Eq. (2) suppresses such changes in favor of small voltages changes. Therefore CODA naturally favors solutions that are local as well as sparse.

Figure 2 gives a numerical demonstration of the emergence of local solutions when CODA is applied to an accumulation-mode 8-dot device in a Si/SiGe heterostructure with four capacitively coupled double quantum dot qubits. Figure 2a shows the device design. We model the device using the semiclassical Thomas-Fermi approximation to compute electron densities and potentials, as described in Methods. The space of operational targets is defined by the eight dot occupations and the four intra-qubit tunnel rates. Our working point is chosen so there are between 1 and 2 electrons per dot, and the intra-qubit Wentzel-Kramers-Brillouin (WKB) transmission coefficients are of order 0.1, corresponding roughly to GHz tunnel rates (see Supplemental Information for details about the simulation parameters). The simulated potential energy landscape for a conductance band electron is shown in Fig. 2a.

We then calculate small changes in the dot occupations and tunnel rates when gate voltages are varied near the working point, obtaining the cross-covariance matrix

\[
\mathbf{c}_0 = \arg \min_c \| \mathbf{c} \|_0, \text{ subject to } \hat{\mathbf{S}}(\mathbf{c}) = \mathbf{t}_0, \quad (1)
\]

where \(\| \cdot \|_0\) is the L0 pseudonorm which counts the number of non-zero elements in the vector. This type of constrained optimization is known as \textit{regularization}. Unfortunately, regularization with respect to the L0 norm is known to be an NP-hard problem, so finding a solution is not computationally feasible for large systems. Compressed sensing avoids this difficulty by regularizing the problem using the L1 norm (the sum of the absolute values of the entries of the vector), which is computationally efficient. In addition, regularizing with the L1 norm tends to achieve sparse solutions, while regularizing with the L2 norm (the square root of the sum of the squares of the entries of the vector) does not.

This approach to constrained optimization is known as basis pursuit denoising or the least absolute shrinkage and selection operator (LASSO) method. In the present work, we solve the related, unconstrained problem

\[
\mathbf{c}_0 = \arg \min_c \left( \| \hat{\mathbf{S}}(\mathbf{c}) - \mathbf{t}_0 \|_2^2 + \alpha \| \mathbf{c} \|_1 \right), \quad (2)
\]

where \(\| \cdot \|_2\) is the L2 norm, and \(\alpha\) is a positive weighting parameter. In this form, LASSO mediates a tradeoff between error in the target (the L2 norm) and sparsity (the L1 norm) through the tuning parameter \(\alpha\). Here, if \(\mathbf{t}_0\) is measured as a desired change relative to some operating point, \(\mathbf{c}_0\) is the change required in the control. Alternately, \(\mathbf{t}_0\) can be measured from zero, in which case \(\mathbf{c}_0\) is the total, rather than relative, required control.
FIG. 2. Locality emerging from the CODA protocol applied to an octuple quantum dot, comprising four double-dot qubits. 

a, Device schematic, with metal gates colored yellow (lower level) and green (upper level). The operational target is to increase the occupation of the right-most quantum dot (indicated by an arrow) by one electron. A top-down view of the lower layer of gates is shown in the inset. 
b, The effective potential energy landscape seen by a conduction band electron at the device working point, chosen such that each quantum dot contains 1-2 electrons, the intra-qubit WKB transmission coefficients are $\sim 0.1$, and the inter-qubit transition coefficients are zero (see Supplemental Information for details about the simulation parameters). 
c, Error vs. $L_1$ norm. Results are obtained by solving equation (2) for a range of $\alpha$, which controls the tradeoff between solution accuracy and the magnitude of voltage changes needed to achieve the operational target. 
d-g, Visualization of the voltage variations corresponding to the four solutions indicated in c, plotted on a logarithmic color scale. As the $L_1$ norm increases, the voltage changes spread across the device, farther and farther from the target dot, demonstrating that the $L_1$ norm provides an effective metric for device design by enhancing the local control.

that describes the effective linear response of the system. Once the cross-covariance matrix is determined, we may specify a desired output. Here, we focus on the operational target of adding one electron to the right-most quantum dot, while holding all the other tunnel rates and dot occupations constant. We solve equation (2), for different values of the tuning parameter $\alpha$, to obtain the solutions shown in Fig. 2c. The top-left corner of Fig. 2c corresponds to solutions for large $\alpha$, which have very good sparseness (small $L_1$ norms), but large errors. In contrast, the bottom-right corner of the graph corresponds to solutions for small $\alpha$, which are very accurate but have large $L_1$ norms. In this context, “error” refers to the sum of the absolute difference between the actual and ideal target output vectors. We express the error in units of electron number; since our target output differs from our operating point by one electron, the initial error is one electron. The total error also includes errors in the tunnel coupling, such that a transmission coefficient error of 0.1 is scaled to have the same weight as an occupation error of one electron.

Figures 2d-g show a colormap of the voltage changes on the electrical gates corresponding to the four solutions indicated in Fig. 2c. It should be noted that both of the extreme cases, Fig. 2d and Fig. 2g, are not practical solutions. The solution in Fig. 2d, though local and sparse, has a large error of nearly one electron. In contrast, the solution in Fig. 2g, though relatively accurate, is neither local nor sparse. As the $L_1$ norm increases, voltage changes spread to gates that are farther and farther from the target location. Hence, we confirm that the $L_1$ norm is an effective proxy for local control, and that
FIG. 3. Improving double quantum dot designs through CODA. a-c, Three designs for double quantum dots. The insets show the lower layer of electrostatic control gates, with the main distinguishing features highlighted in color. In the larger images on the left, an extra layer of top-gates is also shown. In a and b, the top layer includes small square “paddles” used to accumulate electrons in the 2DEG below. In device c, the accumulation paddles have been moved to the lower layer where they are much closer to the quantum dots. Devices b and c have additional red gates directly above the tunnel barriers, which are otherwise difficult to control. d-f, Electrostatic potential energy landscapes corresponding to the working points for the devices shown in panels a-c. g-h, Total voltage ($L_1$ norm) vs. error of CODA for all three designs. In both panels, the black curve corresponds to device a, the red curve to device b, and the blue curve to device c. In g, the operational target corresponds to adding one electron to the left quantum dot, while in h, the target corresponds to increasing the interdot transmission coefficient from 0.1 to 0.2. In both cases, the remaining targets are specified to be held fixed. We find that devices a-b behave comparably, while device c provides better control of both targets.

CODA is a practical tool for tuning a device, because it picks out control solutions that are both sparse and local while achieving a specified operational target.

We now show how CODA can be used to compare different device designs objectively. We focus on single qubit “unit cells,” such as those shown in Figs. 3a-c, which contain modules that can be combined to form a multi-qubit device. Since CODA automatically localizes the control voltages, using it to design a high-quality unit cell leads naturally to multi-qubit devices that are locally controllable.

Figure 3a shows a typical gate design for an accumulation-mode Si/SiGe double quantum dot structure. This design has two principal shortcomings: the gates controlling the tunnel barriers and the dot occupations are relatively far away from the dot, which reduces their selectivity and increases their crosstalk. To address these issues, we consider the alternative gate designs shown in Figs. 3b and c, with the distinguishing features highlighted in the insets. In Fig. 3b, we introduce red gates directly over the tunnel barriers we wish to control. In Fig. 3c, we move the blue accumulation paddles from the upper layer of gates to the lower layer, which is much closer to the 2DEG. We again use the semiclassical Thomas-Fermi approximation to model the devices, with operating points similar to those used for the 8-dot device. The resulting potential energy landscapes of the operating points are shown in Figs. 3d-f.
In Figs. 3g and h, we apply the CODA protocol to assess the performance of the three designs. Here, the black curves correspond to device a, the red curves correspond to device b (with gates over the tunnel barriers), and the blue curves correspond device c (with gates over the tunnel barriers and lowered accumulation paddles). Figure 3k shows CODA results for the operational target of adding one electron to the left quantum dot while keeping the right dot occupation and the interdot transmission coefficient fixed. We find that devices a and b behave similarly, with b providing slightly lower errors for a given \( L_1 \) norm. However, device c shows much better error levels over most of the operating range. In hindsight, this result makes intuitive sense, because the lower paddles are more closely aligned with the quantum dots in device c, which should enhance the local control and reduce the required voltage variations; however, such designs are not yet widespread in the literature.

In summary, we have introduced a protocol for Compressed Optimization of Device Architectures, which applies an \( L_1 \) regularization scheme to a linearized model of device operation. We have demonstrated the effectiveness of this scheme by considering its application to semiconductor nanoelectronic quantum dot systems. As devices continue to grow in complexity, such automated control schemes will be essential for design and operation. Our protocol is computationally and experimentally efficient to implement, and it provides a systematic approach for achieving local and sparse control. Through realistic semiclassical simulations of double-dot devices, we have illustrated how the CODA scheme can be used for quantitative benchmarking and device development. This method provides a path toward the rational design and operation of scalable quantum nanodevices.

**Methods**

We perform semi-classical Thomas-Fermi calculations using the COMSOL Multiphysics software package to solve a nonlinear Poisson equation in three dimensions. We assume the following heterostructure profile for all the modeled devices, consistent with the accumulation-mode devices described in refs. 8 and 18: a 1 nm Si cap layer, 10 nm of Al\(_{2}\)O\(_{3}\) (with dielectric constant \( \varepsilon = 13.19 \)), a 12 nm Si quantum well (\( \varepsilon = 11.7 \)), 32 nm of Si\(_{0.7}\)Ge\(_{0.3}\), a 1 nm Si cap layer, 10 nm of Al\(_{2}\)O\(_{3}\) (\( \varepsilon = 9.0 \)), a 10 nm layer of metallic gates, 80 nm of Al\(_{2}\)O\(_{3}\), and a second 10 nm layer of metallic gates.

The occupations of the dots and the leads are found by integrating the induced charge density over the accumulation regions. The transmission coefficients are calculated by applying the WKB approximation over the potential energy landscape calculated by the self-consistent solver. By changing the voltage on the gates, the relevant occupations and transmission coefficients can be altered to achieve a desired working point, which in this case consists of 1-2 electrons per dot and transmission coefficients of about 0.1. Small (~1 mV) voltage perturbations are then applied to each gate, and the resulting changes in the operational targets are computed. These data are used to calculate the cross-covariance matrix in equation (2). For additional simulation details, see the Supplemental Information.

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**Author Contributions**— All the authors conceived the device operation protocol. AF and JKG performed the numerical simulations and analyzed the data. AF, JKG, MF, SNC, and DRW wrote the manuscript and prepared the figures, with input from all the authors.

**Competing financial interests**— JKG, DRW, MAE, MF, and SNC are co-inventors on a patent application related to some of the nanostructure designs described in this Letter.

**Additional Information**— Supplementary information accompanies this paper. Correspondence and requests for materials should be addressed to John King Gamble (jkgambl@sandia.gov).

### I. SUPPLEMENTAL INFORMATION

#### A. CODA procedure

Here, we provide further details about the CODA protocol sketched in Fig. 1 of the main text. Suppose that we have \( m \) operational targets and \( n \) controls, and that \( n > m \), so the system is underconstrained. We first identify an operating point of experimental interest \( (c_{\text{op}}, t_{\text{op}}) \) and assume that perturbations of the device from the working point are small. We then linearize the mapping \( \hat{S} : C \to \mathcal{T} \) around \( (c_{\text{op}}, t_{\text{op}}) \); we express the resulting linear map as a matrix \( \hat{S}_{\text{op}} \). The underconstrained nature of the problem then allows us to choose a solution with the desired balance between accuracy and sparsity.

The protocol for CODA is specified as follows:

1. Identify an working point \( (c_{\text{op}}, t_{\text{op}}) \) satisfying \( \hat{S}_{\text{op}} = t_{\text{op}} \). In practice, \( \hat{S} \) represents the action of some physical device, and \( t_{\text{op}} \) is the computed target vector corresponding to the input control \( c_{\text{op}} \).
2. Consider a set of linearly independent control variations \{δc₁, δc₂, ..., δcₙ\} about the working point. (We took each δcᵢ to correspond to a small voltage change on a single gate.) Then perform \( n \) simulations or experiments of the form

\[
\hat{S}(c_{\text{op}} + δcᵢ) \approx \hat{S}_{\text{op}}(c_{\text{op}} + δcᵢ) = t_{\text{op}} + δtᵢ. \tag{3}
\]

By linearity, we have \( \hat{S}_{\text{op}} δc = δt \).

3. For a desired target variation \( δt₀ \), identify the control variation \( δc₀ \) that satisfies the CODA metric. First define the error \( ϵ(δc) = \| \hat{S}_{\text{op}} δc - δt₀ \|/2 \). (These are the errors reported in Figs. 2c, 3g, and 3h of the main text.) Then perform the convex optimization

\[
δc₀ = \underset{δc}{\text{arg min}} [ϵ(δc) + α \| δc \|_1]. \tag{4}
\]

Here, the tuning parameter \( α \) determines the balance between the final error \( ϵ(δc₀) \) and the corresponding sparseness, defined by \( \| δc \|_1 \).

**B. Simulation details**

We perform semi-classical Thomas-Fermi calculations using the COMSOL Multiphysics software package to solve a nonlinear Poisson equation in three dimensions. Within the Si quantum well, we define a plane of charge with the charge density given by

\[
n_{\text{2D}}(x, y) = 2 \times 2 \times \frac{e m_{\text{eff}} U(x, y)}{2 \pi \hbar^2}, \tag{5}
\]

where \( e \) is the charge of an electron, \( m_{\text{eff}} = 0.19 m_{\text{electron}} \) is the transverse effective mass of a conduction electron in silicon, and \( U(x, y) \) is the strength of the electrostatic potential energy as a function of position. The two prefactors account for the spin and valley degeneracies. The transmission coefficients are calculated by applying the WKB approximation along an integration path. The path is chosen by first applying a water-shedding algorithm that partitions the potential energy landscape into regions of charge accumulation. We then choose the straight line that yields the largest WKB transmission coefficient over a given barrier.

The details of the working point used in the analysis of the 8-dot device are given in Table I. The physical attributes are listed first. The dot occupations are expressed in electron numbers, and the tunneling coefficients are dimensionless. Voltages are given for each electrical gate, with the following labeling convention defined with respect to Fig. 2a of the main text. Beginning with the upper layer of gates, Gate 1 is in the lower-right corner of the schematic, and the ordering proceeds clockwise. In the lower layer of gates, Gate 5 is in the lower-right corner, and the ordering again proceeds clockwise.

**TABLE I. 8-dot device working point**

| Dot 1 (electrons) | Dot 8 (electrons) | Dot 7 (electrons) | Dot 6 (electrons) | Dot 4 (electrons) | Dot 3 (electrons) | Dot 2 (electrons) | Dot 1 (V) | Dot 2 (V) | Dot 3 (V) | Dot 4 (V) | Dot 5 (V) | Dot 6 (V) | Dot 7 (V) | Dot 8 (V) |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| 1.54280546055    | 1.7360956756     | 0.932755895659   | 1.1642909277     | 1.23681771562    | 1.2427297902     | 1.23777492      | 1.57231061782 |

Qubit 4 tunneling (dimensionless) 0.0645361384122
Qubit 2 tunneling (dimensionless) 0.0128057451715
Qubit 3 tunneling (dimensionless) 0.064321550336
Qubit 4 tunneling (dimensionless) 0.0735760909303

Gate 1 (V) 0.4
Gate 2 (V) 0.4
Gate 3 (V) 0.4
Gate 4 (V) 0.4
Gate 5 (V) 0.06
Gate 6 (V) 0.02
Gate 7 (V) 0.0015
Gate 8 (V) 0.02
Gate 9 (V) 0.02
Gate 10 (V) 0.002
Gate 11 (V) 0.02
Gate 12 (V) 0.02
Gate 13 (V) 0.002
Gate 14 (V) 0.02
Gate 15 (V) 0.02
Gate 16 (V) 0.0015
Gate 17 (V) 0.02
Gate 18 (V) 0.06
Gate 19 (V) 0.1
Gate 20 (V) 0.04
Gate 21 (V) 0.1
Gate 22 (V) 0.06
Gate 23 (V) 0.025
Gate 24 (V) 0.05
Gate 25 (V) 0.025
Gate 26 (V) 0.1
Gate 27 (V) 0.025
Gate 28 (V) 0.05
Gate 29 (V) 0.025
Gate 30 (V) 0.1
Gate 31 (V) 0.025
Gate 32 (V) 0.05
Gate 33 (V) 0.025
Gate 34 (V) 0.1
Gate 35 (V) 0.025
Gate 36 (V) 0.05
Gate 37 (V) 0.025
Gate 38 (V) 0.06
Gate 39 (V) 0.1
Gate 40 (V) 0.04
Gate 41 (V) 0.1

Similar details for operating points on the devices shown in Fig. 3 are given in Table I. As before, the dot occupations are given in numbers of electrons and the tunneling coefficients are dimensionless. Here, the labeling convention for the electrical gates begins with the upper layer at the gate in the upper right corner of the
schematic and proceeds clockwise. On the lower layer of
gates, the labeling begins at the gate in the upper-right
corner and proceeds clockwise.

Our CODA procedure requires the various terms in
Eq. (2) of the main text to have the same units, and
comparable magnitudes. The operational targets consid-
ered in our simulations were electron occupations and
transmission coefficients. To make these quantities com-
parable for the devices studied here, we multiplied the
transmission coefficients by a factor of 10, since their
typical values were roughly 10 times smaller than typ-
ical values for the dot occupations.

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|                       | Device a | Device b | Device c |
|-----------------------|----------|----------|----------|
| Left dot (electrons)  | 1.8031629171 | 1.79170096855 | 1.65404765024 |
| Right dot (electrons) | 1.76165415121 | 1.83732742447 | 1.49176692676 |
| Left lead (electrons) | 959.841161504 | 277.020541467 | 851.625779039 |
| Right lead (electrons)| 959.999149112 | 276.969726865 | 845.352130792 |
| Inter-dot tunneling (dimensionless) | 0.0843761548862 | 0.050126478576 | 0.226974245312 |
| Left dot-lead tunneling (dimensionless) | 0.0619619806628 | 0.0120033288761 | 0.0367450239271 |
| Right dot-lead tunneling (dimensionless) | 0.0696762660153 | 0.00947050628551 | 0.0316318017733 |
| Gate 1 (V)            | 1.0      | 0.4      | 0.4      |
| Gate 2 (V)            | 0.62     | 0.274    | 0.4      |
| Gate 3 (V)            | 1.0      | 0.4      | 0.4      |
| Gate 4 (V)            | 0.78     | 0.425    | -0.1     |
| Gate 5 (V)            | 0.78     | 0.425    | 0.041    |
| Gate 6 (V)            | -0.5     | -0.1     | -0.017   |
| Gate 7 (V)            | -0.497   | -0.01    | -0.003   |
| Gate 8 (V)            | -0.5     | -0.01    | -0.01    |
| Gate 9 (V)            | -0.4     | -0.01    | -0.015   |
| Gate 10 (V)           | -0.45    | -0.1     | 0.041    |
| Gate 11 (V)           | -0.6     | -0.4     | -0.1     |
| Gate 12 (V)           | -0.8     | -0.3     | -0.1     |
| Gate 13 (V)           | -0.6     | -0.18    | -0.1     |
| Gate 14 (V)           | -0.45    | -0.001   | -0.1     |
| Gate 15 (V)           | -0.4     | -0.18    | -0.1     |
| Gate 16 (V)           |          | -0.3     |          |
| Gate 17 (V)           |          | -0.4     |          |