Synaptic Behaviors in Ferroelectric-Like Field-Effect Transistors with Ultrathin Amorphous HfO₂ Film

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Abstract
We demonstrate a non-volatile field-effect transistor (NVFET) with a 3-nm amorphous HfO₂ dielectric that can simulate the synaptic functions under the difference and repetition of gate voltage (V_G) pulses. Under 100 ns write/erase (W/E) pulse, a memory window greater than 0.56 V and cycling endurance above 10⁶ are obtained. The stored information as short-term plasticity (STP) in the device has a spiking post-synaptic drain current (I_D) that is a response to the V_G input pulse and spontaneous decay of I_D. A refractory period after the stimuli is observed, during which the I_D hardly varies with the V_G well-emulating the bio-synapse behavior. Short-term memory to long-term memory transition, paired-pulse facilitation, and post-tetanic potentiation are realized by adjusting the V_G pulse waveform and number. The experimental results indicate that the amorphous HfO₂ NVFET is a potential candidate for artificial bio-synapse applications.

Keywords: FET, HfO₂, Oxygen vacancy dipole, Memory, Synapse

Background
The need for high density, high performance, and low power consumption has necessitated the development of novel memory devices. Because of their compact structure, non-destructive read-out operation, and multi-bit storage, non-volatile transistors such as ferroelectric field-effect transistors (FeFETs), floating-gate transistors, and IGZO memristors have attracted much attention for embedded memories, computing-in memory, and neuromorphic synapse applications [1–5]. The stimulus is applied to the gate electrode of the transistors for synaptic operation, and the drain side current is the post-synapse current [6, 7].

Recently, non-volatile field-effect transistors (NVFETs) utilizing amorphous Al₂O₃ and ZrO₂ gate insulators were experimentally realized, which was attributed to the switchable polarization (P) induced by the voltage-modulation of the oxygen vacancy (V_O²⁺)-related dipoles [8–11]. The mechanism of voltage-modulation of V_O²⁺ in ferroelectric tunnel junctions was also demonstrated, which improved the tunneling electroresistance ratio of the device [12]. Compared to the polycrystalline doped-HfO₂ FeFETs, NVFETs with amorphous dielectrics exhibited significantly lower operation voltage and better linearity for multi-threshold voltage operation [9]. These characteristics make them a promising candidate for low-power neuromorphic devices that closely mimic biological behaviors, which are not to be investigated yet.

In this work, biological synapse behaviors such as short-term plasticity (STP), long-term potentiation (LTP), the transition from short-term memory (STM) to long-term memory (LTM), and spike-timing-dependent plasticity (STDP) are emulated based on the single amorphous HfO₂ NVFET, without using additional circuit elements.
Methods
The process flow in [9] was used to fabricate the NVFETs with an amorphous HfO$_2$ gate insulator on 4-inch n-type Ge(001). After the pre-gate cleaning, the substrate was loaded into an atomic layer deposition (ALD) chamber to deposit the HfO$_2$ at 300 °C. Then, a 100-nm-thick TaN gate electrode was deposited by the reactive sputtering. After the gate electrode patterning and etching, the source/drain (S/D) regions were implanted by BF$_2^+$. 20-nm thick nickel (Ni) S/D metal electrodes were formed by a lift-off process. Finally, the repaid thermal annealing (RTA) at 350 °C was carried out to improve the interface quality and form the Ni germanium silicide S/D contacts.

The schematic of the fabricated NVFET is shown in Fig. 1a. Figure 1b shows a 3-nm-thick amorphous HfO$_2$ imaged with high-resolution transmission electron microscopy (HRTEM). Figure 1c depicts the measured ferroelectric-like $P$ vs. voltage ($V$) behavior in the amorphous HfO$_2$ capacitor at a frequency of 1 kHz. The underlying mechanism for the ferroelectric-like behaviors in this amorphous HfO$_2$ devices is similar to that for those devices in Refs. [8, 9]. The extracted evolution of the remnant $P$ ($P_r$) and coercive voltage ($V_c$) for the device during the endurance test is shown in Fig. 1d. No wake-up or imprint is observed over $10^6$ cycles. A positive-up and negative-down (PUND) test is used to extract the switching current component of the device by isolating the non-switching charge (Fig. 1e), demonstrating the true $P$.

Results and Discussion
In contrast to the trapping/detrapping process [13–15], a ferroelectric-like clockwise hysteresis loop is observed for the DC sweeping of the drain current ($I_D$) as a function of gate voltage ($V_G$) curves for the transistor with the amorphous HfO$_2$ gate insulator, as shown in Fig. 2a. The non-volatile memory function is induced by the ferroelectric-like $P$ switching in the gate stack. Figure 2b shows the initial $I_D$ vs. $V_G$ curve for the device and those underwent with 100 ns, 1 μs, 10 μs, 100 μs, and 1 ms write/erase (W/E) pules at ±3 V voltage providing a non-volatile memory function, respectively. The device has a gate length ($L_G$) of 3 μm and a gate width ($W$) of 80 μm. The write (erase) operation is achieved by applying positive (negative) voltage pulses to the gate of the HfO$_2$ FET, to raise (lower) its threshold voltage ($V_{TH}$). Figure 2c plots the $V_{TH}$ values for different W/E pulse widths. As the pulse width increases from 100 ns to 10 μs, the MW increases to 1.2 V; but when the W/E pulse width further increases, the MW decreases. Trapping/detrapping process is thought to cause the degradation of $V_{TH}$ under the 100 μs to 1 ms W/E pulses. Here, $V_{TH}$ is the $V_{TH}$ difference between the two states, and $V_{TH}$ is defined as $V_G$ at $I_D=100$ nA.$W/L_G$.

As shown in Fig. 2d, a stable MW is maintained over $10^6$ W/E cycles. Figure 2e shows that a stable MW of the amorphous HfO$_2$ device can be maintained over several hundred seconds. The limitation retention time of the device is mainly due to the smaller $P_r$ and large depolarization field. Recent studies have shown that the non-volatile devices with limited retention time can be alternative candidates for high-density and lower power DRAM architectures [16, 17].

Synapse is a basic unit of the human neural network to realize the information transmission from the pre-synaptic neuron to the post-synaptic neuron. The STP is a key factor that affects the biographic performance of the NVFET synapse in the neural system [18]. Figure 3 shows the STP characteristics of a HfO$_2$ NVFET under the single $V_G$ pulse with a fixed pulse magnitude of -3 V. The $V_G$ pulse width varies from 1 μs to 10 ms and the base voltage varies from 0.5 V to −1.5 V. As a three-terminal device, the STP performance can be modulated by changing the base voltage, magnitude, and width of the $V_G$ pulses. Underwent an applied $V_G$ stimulus, the post-synaptic $I_D$ of the device increases to a high $I_D$ state and decays to a low $I_D$ state when the $V_G$ pulse ended. For all the measurements, the devices are in the same relaxed pre-state.

![Diagram of NVFET with amorphous HfO$_2$ gate insulator](image)
As shown in Fig. 3a, underwent a 1 μs \( V_G \) pulse, the device exhibits a lower post-synaptic \( I_D \) under the base voltage of \(-1.5 \) V and \(-1.0 \) V compared to the cases under \(0 \) V and \(-0.5 \) V \( V_G \) base. It is speculated that this could be due to the smaller difference between base and pulse \( V_G \) voltages. As the \( V_G \) pulse is widened to ms, the post-synaptic \( I_D \) no longer depends on the base voltage (Fig. 3c, d). In general, the post-synaptic \( I_D \) of the device is improved with widening the stimulus \( V_G \) pulse.

According to Fig. 3, there is a refractory period after the \( V_G \) pulse. The \( I_D \) barely varies with the \( V_G \), which accurately simulates the bio-synapse with the external stimulating signal. The refractory period of the NVFET synapse is approximately 10–100 \( \mu \)s, which does not depend on the \( V_G \) pulse width or magnitude. Figure 4 depicts the post-synaptic \( I_D \) of the transistor that underwent multiple \( V_G \) input pulses within the refractory period. During this period, \( I_D \) is excitable by the \( V_G \) pulse, but its value is less than that for the initial pulse firing. After the refractory period, the post-synaptic \( I_D \) increases with time to a saturate state, and values of post-synaptic \( I_D \) in saturation increase with the decrease in the base voltage.

Besides the width and magnitude of the pulse, the stimulation rate also influences the memory formation of the device. To examine the effects of the stimulation rate on the transistor, the ten cycles \((N = 10)\) of stimuli/read \( V_G \) are applied to the gate electrode. As shown in Fig. 5a, during the stimuli or read, the amplitude and time of the \( V_G \) pulse are fixed, and the cycle period \( T \) is changed by varying the interval parameter. The \( I_D \) of the transistor was read at low voltage immediately after each stimulation pulse, which is denoted by \( I_1, I_2, \ldots, I_{10} \) \cite{19}.

The dynamic change in the \( I_D \) of the amorphous HfO\(_2\) NVFET under a series of \( V_G \) pulses with the different \( T \) at a \( V_{DS} \) of \(-0.5 \) V is shown in Fig. 5b. The \( I_D \) (i.e., \( \Delta I_D/I_I \)) of the device increases with the stimuli \( T \) numbers to mimic the memory behavior in the biological system. Here, \( \Delta I_D \) is calculated by \( I_N - I_I \), \((N = 1, 2, \ldots, 10)\). Note that the \( I_D \) of the device increases, i.e., \( \Delta I_D/I_I \) with the reduced \( T \). With a high stimulation rate being the most effective and
a low stimulation rate being the least effective for transforming from STM to LTM.

Figure 5c plots the \((I_2 - I_1)/I_1\) and \((I_{10} - I_1)/I_1\), which represent the experimental conditions for paired-pulse facilitation (PPF) and post-tetanic potentiation (PTP) used in biological studies, respectively [20, 21]. The PPF and PTP phenomena in our amorphous HfO2 synaptic transistor can be compared to synapses in biology. If be former, the synaptic response is enhanced when one stimulus is followed by the same stimulus soon after; if be latter, the synaptic transmission gradually increases with the number of stimuli when a series of stimuli are received [20–22]. These verify the feasibility of the amorphous HfO2 device in realizing the transformation of simulated biological memory. The error bars reflect the standard deviation when repeating the measurement a few times to prove the correctness of the data and minimize fluctuations in data.

The temporal relationship of activity between the pre- and post-synaptic neurons is another important aspect of the synapse. We define \(t_{\text{PRE}}\) and \(t_{\text{POST}}\) as the arrival times of the pre-spike and the post-spike, respectively. The change in synaptic weight (\(\Delta w\)) is a function of the \(\Delta t\) (\(\Delta t = t_{\text{PRE}} - t_{\text{POST}}\)) between pre- and post-synaptic activity [23]. For a given stimulation, LTD will occur if \(\Delta t > 0\), while LTP will occur if \(\Delta t < 0\). STDP is defined as the change in synaptic weight of the \(\Delta t\) between pre- and post-synaptic activity. By utilizing the waveforms adopted in Fig. 6a, b, the STDP curves for the amorphous HfO2 NVFET-based synapse are extracted with 100 ns spikes and shown in Fig. 6c. The pre-and the post-spike resembling the output of the leaky integrate-and-fire neurons are constitutive of an initial negative pulse followed by a sequence of positive pulses with the decreased amplitude. As shown in Fig. 6c, the amorphous HfO2 NVFET can stimulate the STDP learning

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**Fig. 3** Base voltage varies from 0.5 to -1.5 V. The widths of \(V_G\) pulses in a–d are 1 μs, 100 μs, 1 ms, and 10 ms, respectively.

**Fig. 4** Post-synaptic \(I_o\) of the device underwent multiple \(V_G\) input pulses within the relative refractory period.

**Fig. 5** a \(V_G\) pulse waveform with the different \(T\). b The \(I_o\) increase as a function of the gate stimulus number plots with the different \(T\). c Extracted \((I_2 - I_1)/I_1\) and \((I_{10} - I_1)/I_1\), representing PPF and PTP behaviors, respectively, of the transistor.
rule successively with spiking period time $T_{\text{STDP}}$ varying from 170 to 210 ns. The HfO$_2$ NVFET obtains a steeper conductivity change around $\Delta t = 0$ at the $T_{\text{STDP}} = 190$ ns compared to the other $T_{\text{STDP}}$ conditions, which is possibly due to the better matching between the spike waveform shape applied at the gate electrode and the non-volatile characteristics induced by ferroelectric-like behavior of the device.

Conclusions

In this work, we report an ultrathin amorphous HfO$_2$ NVFET to emulate the bio-synapse. An MW of 0.56 V with an endurance above 10$^6$ cycles is experimentally demonstrated under the $\pm 3$ V and 100 ns W/E pulses. Furthermore, various synaptic behaviors including STP under different stimuli, transitioning from STM to LTM, PPF, PTP, and STDP performance are realized in the device.

Abbreviations

TaN: Tantalum nitride; $P_r$: Remnant polarization; $E_c$: Coercive electric field; Ge: Germanium; ALD: Atomic layer deposition; BF$^+$: Boron fluoride ion; HfO$_2$: Hafnium oxide; GeO$_x$: Germanium oxide; HRTEM: High-resolution transmission electron microscope; Ni: Nickel; RTA: Rapid thermal annealing; MW: Memory window; $I_D$: Drain current; $\Delta w$: Synaptic weight; $V_G$: Gate voltage; $V_{TH}$: Threshold voltage; NVFET: Non-volatile field-effect transistor; T: Period; FeFET: Ferroelectric field-effect transistor; STDP: Spike-timing-dependent plasticity; STP: Short-term plasticity; LTP: Long-term potentiation; STM: Short-term memory; LTM: Long-term memory; PPF: Paired-pulse facilitation; PTP: Post-tetanic potentiation.

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Authors’ contributions

YP carried out the experiments and drafted the manuscript. YP, WWX, and GQH designed the experiments. GQZ helped to measure the device. GQH and YL helped to revise the manuscript. YH supported the study. All the authors read and approved the final manuscript.

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Availability of data and materials

The datasets supporting the conclusions of this article are included in the article.

Declarations

Competing interests

The authors declare that they have no competing interests.

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