Probabilistic Analysis of Dynamic Power and Area in Network on Chip

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Abstract. The power used by digital integrated circuits has become a key restriction for the design and development of VLSI as the device complexity and transistor density increase. Clock-gate synthesis methods are applied to circuits to prune changes in registers by modifying the next-state register functions in order to reduce complex power dissipations. Therefore, a sequential inspection of the circuits is needed for testing this form of synthesis. A new design to increase the efficiency of network-on-chip buffers and minimize the overall area and power consumption of the router is proposed. The non-uniform use of buffers in the network is leveraged, and control is used in unusual buffers. A part of the buffer is turned on instead of shutting down the buffer completely. For some recent studies, power-gating inactive components have been used as a promising approach to minimize static and dynamic power consumption, although its disadvantages, like wake-up delay and power overhead, should also be properly addressed. Throughout this work, a probabilistic experiment was carried out to estimate the power-gating performance and a control unit was proposed to handle the confirmation of the sleep signal to buffer entries based on the results of the study. The analysis results show an average increase in static power savings. For the research community to tackle the Contest of improved power performance and efficiency, including control gate, operating insulation, storage slicing, power gate and intensity scaling, respectively. The analysis is also examined other systems and strategies for optimization built to reduce power further without noticeable loss of performance.

Keywords: Buffer, Density, Efficiency, Network on chip, Optimization, System control methods

1. Introduction

The Traditional chip system (SoCs) is based on bus, cable delay, noise, power dissipation problems, and signal synchronization problems. With an on-chip communication interconnect architecture is called Network on Chip, which offers a high-performance networking infrastructure [1]. Networks-on-Chip has all the requirements needed to be potential SoCs. It is constructed in a coordinated way by a collection of interconnecting routers and point-to-point channels. Traditional computer network considers collision between packets to be an unavoidable problem, and the ultimate aim of computer networks is to reduce the likelihood of collision, but the possibility of dropped packets is very small in on-chip networks. This is related to the fact that the router's communication links within a Network on
chip are shorter than those in computer networks, thereby allowing tight router synchronization. Some of an on-chip network's characteristics are low power consumption, small area (in routing nodes [5]), cheap cables and low interconnect latency. Though traditional computer network characteristics are long wires, high communication latency, and a lot of complex routing nodes.

2. Related works
All of them are based on the routing algorithm. For example, using a dynamic routing algorithm, we can minimize power, but it adds complexity to the design. Several works in the chip network have focused on the architecture of the topology [1, 2]. Pointed out that eliminating some linkages between the core nodes could effectively prevent the flow of data from the core nodes, thus reducing traffic congestion[3], found that removing some linkages between the large Internes nodes could also reduce congestion[4], considered both the transmission capability of the node and the bandwidth constraints, and found that allocation of resources based on algorithm [5].

Several recent works have proposed the chip network, in [1,2,3] the non-uniformity of the usage of the buffer is leveraged through the network and the power gating is extended to rarely used buffers. Instead of turning off the buffers entirely, the buffer part is switched on [4]. This design option has a major performance advantage since the virtual channel buffer is still capable of receiving network packets [5-12]. The usage of buffers in a Network on chip differs considerably across the network and buffers that are rarely used can be turned off through a power gate [13-17]. Power-gating consists of switching off the NMOS footer linked in series with logic to reduce leakage current flow. Design and implementation of a configurable virtual channel in the router intended as a dedicated Network on chip support module in an FPGA is presented. The router is built using crossbar switching and is used to interconnect routers in the communication protocol [17-18]. Chip Network interconnects IP to reduce the power consumption and die size for consumer electronics, mobile, automotive and other applications on chip (SoC) devices. In addition, only leakage savings and network on chip efficiency are recorded in several recent works, while aspects such as the area and the leakage of the power gate are addressed in our proposed system.

3. Proposed system
Primarily, focus on techniques that are designed to reduce the Area and Dissipation of power by modifying the virtual channels in the input ports of router from [3] connecting the network to the chip as well as by routers and network interfaces, and their subscription is expected to rise as per current technologies. In particular, designed a Set of data correction programs running at flit rate but on an end-to-end base system that could allow us to minimize the changing activity and the switched coupling activity together. Communication complexity is the virtual channel Classification area throughout the flits, which adds a lot of bits to the flit contents. data between the nodes must also be shared on a virtual channel basis. The nodes should also contain information per virtual channel condition. The transmission node holds state information such free buffer count, virtual channel allocation, and packet priority. The receiving node also maintains virtual channel designation, input and output pointers for each path buffer and channel status. Suggested the computational level and are evaluated by simulation on synthesis and actual traffic situations. The inquiry considers many aspects and metrics of the architecture of the system in the information sharing subsystem, and also the gate area, power dissipation and energy usage. Outcomes have shown that using suggested error correction schemes in the communications system, energy and power could be saved with little or no significant deterioration in performance but with an area operational costs in the Network
FIFO Flexibility Controller: A new add-on module is responsible for determining some appropriate FIFO available on the network to carry a received packet. Finally, it is accountable for communicating with both the output ports to pass the obtained packet to their downstream routers according to the route method used.

FIFO buffer: A FIFO here can accept packets from the explicitly attached upstream router as the Base routers FIFOs, but from other input ports. Forwarding logic: Apply the routing algorithm to decide the path of the packets in order to select the correct output port. The activity of the Versatile router is the same as the operation of the Base router, but it will be unique in the event of a conflict. As far as contention is concerned, the Versatile router does not delay until the demanded full FIFO has one or more free slots like the Base router does, yet the FFC does look for a free slot in any appropriate not full FIFO throughout the router by Asking for FIFOs that are not complete in other input ports, and when it finds a free slot, it returns the application to the upstream router. The package is then moved to the chosen FIFO. Following that, the Robust Router should work exactly the same as Base Router.

A proper sizing of the sleep transistor is required for effective use of power gating, as it affects the output of all the connected gates. A big one means an significant overhead in area and an ineligible capacity (i.e., capacity and delayed) for ON-OFF transitions while an unacceptably small transistor slows the circuit down in active mode because of its high resistance. Another problem is that the cumulative current injected into the sleep transistor is calculated via the sleep transistor drain-source route and consequently leads to deterioration of the sleep delay during active operation shown in fig 1.
This finer technique is referred to as the insertion of the clustered sleep transistor, a very efficient solution that connects many cell subsets, i.e. clusters, to dedicated transistors in the entire organized sleep network. Cylindered energy gating is not new in the low-power design area and a large number of clustering solutions have been suggested. The solution for groups of gates with mutually exclusive discharge patterns allows for optimal sleep transistor dimensions. Instead, the authors demonstrate a timely clustering technique that can manage the time and the region simultaneously.

For efficient use of power electricity, the sleep transistor needs to be properly designed. In addition, even though the circuit in active mode can be slowed by a small sleep transistor due to its high resistance, a larger one requires a wide area and a substantial energy cost for driving. Designers typically establish an IR-drop threshold (for example 10% of VDD) as a limit to be met by the sleep resistance size transistor. Eq can be used for the measurement of the average sleep channel resistance.

\[
\frac{R_{\text{st}} \cdot D V_{\text{DD}}}{I_{\text{on}}} \cdot \text{drop}
\]

When the VDD remainder of the sleep transistor is allowed to decrease the voltage, expressed as a percentage of the voltage supply, while the ion is the highest discharge current.

Power-gated cells insert in the active mode into the sleep transistor. Estimating the active current is not an easy task. An incorrect estimation of \( I_{\text{on}} \) actually indicates a sleep transistor size that is sub-optimal and can increase the area and power or, worse yet, timing violations during active mode. The sleep transistor is working in a stable region with knowledge of \( R_{\text{st}} \) and its size must be measured correctly.

The size and physical efficiency of the sleep transistor is strongly affected by carrier mobility, threshold voltage, and the gate duration. Consequently, the type of MOS device is needed for the proper sleep transistor size nMOS. While both devices can be used without distinction as power switches (i.e. retaining the same reduction in leakage), nMOS is typically better suited. Transistors are more suitable. PMOS devices are generally less leaky than nMOS devices, but have a lower carrier range, reducing the ongoing current. Consequently, pMOS sleep transistors require more silicon area than nMOS, to ensure a certain current efficiency.

Power gating is indeed a widely recognized method for raising the loss potential of unused electronic circuitry products. In order to efficiently introduce energy gating to a digital loop, the inactive duration of both the circuit must be large enough yet to account for both the energy of the wake-up below. While Network on chips are designed to allow strong inter-node connections to prevent congestion performance, actual-world implementations generally experience steady traffic, contributing under-utilized on-chip properties. Our review of mesh topology benchmarks reveals that on average, 92.7% of routers are inactive during runtime applications. Entirely, the power gating is essential to Network on chips due to the inclusion of its leak capacity to overall processor capacity but, secondly, this appears to be encouraging due to the abundance of indolence in the modules.

![Figure 1b. Tail current in different modes](image)
Various sleep transistor modes for one cell are shown in Figure 1b. The sleep saving leakage and the data retention modes are in spite of the circuit leakage. The penalty for power gating (energy and time delay) is increased by the circuit leakage, shown by the use of the can gate in the GND. Fig 1c indicates the wake up time and energy exhaustion.

![Figure 1c. Wake up energy and wake up time](image)

The parallelizing view of the network breaks down the data forwarding phase in a few short steps. Standard flow control techniques, such as wormhole routing, first allocate a buffer and keep it from the time the data flit moves away the current node to the time the flow control signal returns to notify the current node that the buffer can be released. The buffer can also be reused after this turn-around time. And the credit turns around the time of the buffer is at least the amount of the delay in the spread of the data flit in forward direction and the flow control back.

![Figure 2. Virtual channel planning](image)
The approach presented in the paper addresses overhead with respect to the optimization of the buffer. Complex distribution of these buffers to various virtual channels must be considered. It would also improve the efficiency of the buffer usage, as not all virtual channels need the same amount of buffering. Getting dynamic virtual channels provides a basic structure for the implementation of various schemes. Dynamic buffer allocation to virtual channels is more complicated and hence needs more overhead in terms of control logic complexity. Such complex schemes aim to optimize buffer performance. Neighboring routers, however, should also be informed about a power-closed router, then they may send packets that are tossed out of the network. Therefore, handshake alerts are needed to warn the neighbor if the router is switched down. Throughout this scenario, that competitor marks relevant outlet ports as being worked off and makes this inaccessible while assigning a change. Likewise, neighboring routers want handshake signals that alert the router when sending a message. The router on the right is power gated but alerts its neighbors when using PG signals. As a result, the former neighbors tag the corresponding actual output safety buffer as either power-off. Nearby routers are encouraging this router to be operated by a wake-up message.

4. Results and discussion
The accuracy of both the gate is largely limited by the precision of all its based timing mechanisms and the energy-based modules. The gate itself is specifically modeling the actions of the Network on chip power gate.

| Parameters                          | Existing method | Proposed method |
|-------------------------------------|-----------------|-----------------|
| Area of consumption of virtual channel | 38.94%          | 27.4%           |
| Power consumption of virtual channels | 55.73%          | 43.6%           |
| Network topology                    | Mesh            | Mesh            |
| Routing algorithm                   | XY              | XY              |

Almost every idle time cycle produced somewhere in Garnet is still controlled and otherwise reported as a power cycle even if certain conditions have been met and the static and dynamic power of each Network on chip element is taken into account shown in the table 1. given that the dependent control modules correctly model the energy consumption of the modules. One disadvantage in a gate was that the specificity of the power gate is at the per router stage. Although older Network on chip power-gating works explored the potential for power-gating of individual elements within a router given the difficulty of handshaking and command, the most famous works favor power-gating to specificity per router.
The area and power consumption of virtual channels in proposed method is 27.4% and 43.6% when compared to existing method [3] 38.94% and 55.73% respectively.

Figure 4. Power consumption of proposed method

The best possible optimization rates for various cell topologies, 6 T, 8 T, 9 T and 10 T are taken. The reduction in power of design, stability and loss of time is thoroughly investigated. Where the average area and power of the router can be possibly improved by around 11% without having a major effect on the overall Performance which is compared to [3], shown in table 1 and figure 3, future work can be undertaken to help to reduce the latency using power-gating method.

5. Conclusion
The Virtual channel flow control is one of the most common flow control methods used in interconnecting networks due to its various advantages powerful buffer usage, maximum throughput, low latency and network capacity regardless of the number of stages. Throughout this paper, we addressed the importance of the allocation of buffer for virtual channel flow control. Various different buffer allocation strategies that are valid at node and network level have been addressed. Higher buffer utilization one should suggest using schemes such as flit-reservation flow control, this system completely avoids idling buffer utilization due to credit turnaround period. Power-gating is a reasonable way of minimizing NoC static power but may result in a large output penalty. Within this paper we discuss the essential problem of simulating NoC power management systems correctly and efficiently. In order to achieve accuracy and efficiency of the simulation we define main requirements which should be fulfilled by a No C power-gating simulator. Power-gating as a symbolic low-power technique can be added to Network on chip to reduce this increase in leak capacity. Nevertheless, the cancellation issue significantly limits the power gate to be used effectively due to its negative effect on efficiency. In this paper, we suggest a creative limited power-gating solution to avoid the issue of power-gated separation in Network on chip.

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