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ECM modeling and performance tuning of SpMV and Lattice QCD on A64FX

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Summary

The A64FX CPU is arguably the most powerful Arm-based processor design to date. Although it is a traditional cache-based multicore processor, its peak performance and memory bandwidth rival accelerator devices. A good understanding of its performance features is of paramount importance for developers who wish to leverage its full potential. We present an architectural analysis of the A64FX used in the Fujitsu FX1000 supercomputer at a level of detail that allows for the construction of Execution-Cache-Memory (ECM) performance models for steady-state loops. In the process we identify architectural peculiarities that point to viable generic optimization strategies. After validating the model using simple streaming loops we apply the insight gained to sparse matrix-vector multiplication (SpMV) and the domain wall (DW) kernel from quantum chromodynamics (QCD). For SpMV we show why the CRS matrix storage format is not a good practical choice on this architecture and how the SELL-C-σ format can achieve bandwidth saturation. For the DW kernel we provide a cache-reuse analysis and show how an appropriate choice of data layout for complex arrays can realize memory-bandwidth saturation in this case as well. A comparison with state-of-the-art high-end Intel Cascade Lake AP and Nvidia V100 systems puts the capabilities of the A64FX into perspective. We also explore the potential for power optimizations using the tuning knobs provided by the Fugaku system, achieving energy savings of about 31% for SpMV and 18% for DW.

KEYWORDS:
ECM model, A64FX, sparse matrix-vector multiplication, lattice quantum chromodynamics

1 | INTRODUCTION

The processor architectures used in HPC systems have been dominated for a long time by general-purpose commodity off-the-shelf processors (CPUs). Increasing clock speeds in the past and steadily increasing core counts in the last decade resulted in an attractive price-performance ratio at moderate power consumption. Traditional HPC-oriented architectures such as vector computers have almost been superseded. As power constraints and technology scaling limits became more pressing, a strong trend towards diversification in processor architectures for HPC started. General-Purpose Graphics Processing Units (GPGPUs) provide new levels of price-performance and energy-per-flop efficiency and therefore have become very attractive for several application fields such as classical molecular dynamics, fluid dynamics or linear solvers as well as artificial intelligence.
Large initiatives have started to design custom HPC processors addressing the performance characteristics of a broad range of applications from computational science and engineering. They make use of new memory technologies or modular instruction sets and implement HPC-specific hardware concepts such as fast on-chip synchronization or specific on-chip accelerators. The Post-K and the European Processor Initiative (EPI) projects are two such well-known endeavors. The former has already delivered the Fujitsu A64FX processor, which powers the fastest machine on the Top500 list as of November 2020, Fugaku.

The A64FX CPU is the second design (after Intel’s Xeon Phi Knights Landing) that connects a classic cache-based multicore processor to high bandwidth memory (HBM). While the use of HBM is established on GPGPUs with their massively threaded programming and execution model, it is an interesting question if standard CPU-oriented programming models (e.g., OpenMP) in combination with the limited thread- and data-level parallelism of the CPU hardware can also exploit the potential of HBM. Several other features such as hardware barrier and sector cache have been implemented in the A64FX to address the needs of HPC as well as artificial intelligence (AI) applications. At the same time, a strict power budget had to be kept, enforcing compromises in the design of cores, caches and the chip. Finally, the application performance of the A64FX critically depends on the quality of its rather new software ecosystem, in particular compilers and numerical libraries. This complex situation requires a careful analysis of existing well-optimized CPU codes, e.g., to what extent they may exploit the benefits of the new design and how the new concepts implemented in the A64FX interfere with code-optimization techniques, parallelization strategies and data layouts.

In this paper we use analytical performance modeling and the Execution-Cache-Memory (ECM) performance model to investigate and understand basic performance capabilities and new performance and power-saving features of the A64FX with a focus on streaming loops. In view of the CPU’s high memory bandwidth (> 800 Gbyte/s) and moderate core count (48), the ECM model’s capability to identify single-core performance contributions will be of central importance. We choose two case studies for in-depth application performance analysis representing important fields with moderate to low computational intensities: a sparse matrix-vector multiplication (SpMV) kernel and a Lattice QCD domain wall kernel. Our analytical modeling approach allows us to pinpoint inefficiencies of the hardware design and the existing software ecosystem and provides recommendations on code optimization and data layouts. We further compare the performance characteristics of the A64FX with a high-end commodity server CPU system (Intel Cascade Lake AP) and a GPGPU (NVIDIA V100). The V100 uses a comparable HBM technology.

Outline
The paper is organized as follows: Section 2 describes the basic benchmarking methodology together with the compilers and libraries used. It further briefly summarizes the relevant performance characteristics of the standard CPU and GPGPU systems chosen for comparison. A detailed architectural analysis of the A64FX-based Fujitsu FX1000 used in the Fugaku system is provided in Sec. 3. Strong focus is put on the in-core analysis, including a discussion of the capabilities of Arm’s Scalable Vector Extension (SVE) and the out-of-order back end. Furthermore we discuss an additional feature set of the Fugaku system: the zero fill instruction which prevents write-allocate transfers, the hardware barrier and the sector cache. In Sec. 4 we establish the ECM machine model for the A64FX and validate it for a broad range of streaming kernels. An analysis of SpMV performance on the A64FX is presented in Sec. 5. Starting with a standard CPU-friendly SpMV data format we identify shortcomings on the single-core level through the ECM model. We investigate the use of a vector-friendly data layout and of sector cache to fully exploit the available bandwidth. In Sec. 6 we address the large application field of Lattice QCD focusing on the domain wall kernel. The ECM model again guides the investigation of potential performance gains through code-optimization strategies and appropriate choices of data layout. The impact of A64FX’s power-saving mechanisms and performance comparisons with standard CPU and GPGPU are presented in Secs. 5 and 6 for both case studies. In Sec. 7 we summarize our findings and put our work in the context of existing literature.

Extended version of workshop short paper
The work presented here is an extended version of a short paper published at the PMBS 2020 workshop [1]. The short paper investigated the basics of the ECM model and briefly demonstrated the benefit of a vector-friendly data layout for the A64FX processor used in the QPACE 4 (Fujitsu FX700) system. Both topics have now been investigated on the FX1000 system used in Fugaku. More importantly, we have substantially increased the scope of both topics, e.g., by improving the ECM model considering the impact of page sizes and by presenting a detailed ECM model and performance-tuning strategies for SpMV. Topics presented here but not covered in [1] include the case study of the Lattice QCD kernel, the investigation of power-saving mechanisms and specific hardware features of the A64FX and the comparison with state-of-the-art CPUs and GPGPUs.
TABLE 1 Key specifications of the A64FX CPU in the FX1000 system. “⊕” represents an exclusive OR.

| Specification                          | Value                                      |
|----------------------------------------|--------------------------------------------|
| Supported core frequency               | 2.0/2.2 GHz                                |
| Number of CMGs                         | 4                                          |
| Cores/threads per CMG                  | 12/12                                      |
| Instruction set                        | Armv8.2-A+SVE                              |
| Max. SVE vector length                 | 512 bit                                    |
| Peak flop rate                         | 3379.2 Gflop/s                             |
| Cache line size                        | 256 bytes                                  |
| L1 cache capacity                      | 48×64 KiB                                  |
| L1 bandwidth per core (b_{Reg→L1})     | 128 B/cy LD ⊕ 64 B/cy ST                   |
| L2 cache capacity                      | 4×8 MiB                                    |
| L2 bandwidth per core (b_{L1→L2})      | 64 B/cy LD ⊕ 32 B/cy ST                    |
| Memory configuration                   | 4×8 GiB HBM2                               |
| CMG TRIAD bandwidth                    | 213 Gbyte/s                                |
| CMG read-only bandwidth                | 227 Gbyte/s                                |
| Full chip TRIAD bandwidth              | 841 Gbyte/s                                |
| Full chip read-only bandwidth          | 859 Gbyte/s                                |
| L1 translation lookaside buffer        | 16 entries                                 |
| L2 translation lookaside buffer        | 1024 entries                               |

2 TESTBED AND EXPERIMENTAL METHODOLOGY

The majority of this work was done on the Fugaku supercomputer. The system is running the Red Hat Enterprise Linux (RHEL) 8.3 operating system. The CPU supports two core clock frequencies, 2.0 GHz and 2.2 GHz. The clock frequency was fixed to 2.2 GHz unless specified otherwise. The key specifications can be found in Table 1 and will be discussed in more detail in Sec. 3.

All code was compiled with the GNU gcc (GCC 10.2.0) and Fujitsu tcsds 1.2.30 (FCC 4.4.0a) compilers. For GCC we used the -march=armv8.2-a+sve and -Ofast flags in combination with huge pages for compilation. For FCC there exist two modes of compilation, Trad and Clang mode. We used Trad mode with -Kfast and -Khpctag for all the runs, except for the domain wall QCD code where we used Clang mode with -Ofast due to the incompatibility of Trad mode with GCC attributes. Possible deviations from the default compiler flags stated above will be mentioned in the relevant sections.

All benchmarks were run in double precision so that a vector length (VL) of 512 bits corresponds to eight real or four complex elements. In general, SVE vector intrinsics (ACLE [2]) were employed to have better control over code generation. All arrays were aligned to OS page boundaries, for which best performance was observed in the experiments. In order to minimize statistical variations we repeated every benchmark loop for an overall runtime of at least one second. We do not show the statistical fluctuations if they were below 5%.

For benchmarking individual machine instructions we employed the ibench [3] framework and cross-checked our results with the A64FX Microarchitecture Manual [4]. The LIKWID [5] tool suite in version v5.1.0 [6] was used, specifically likwid-perfctr for counting hardware events and likwid-pin to pin the threads to cores. The Power API framework [7] v2.0 installed on Fugaku was used for setting the power tuning knobs and measuring the energy consumption.

To put the results in relation to state-of-the-art hardware currently available, experiments were also run on an Intel Cascade Lake (CLX-AP) and an NVIDIA V100 GPU system. The CLX-AP experiments were conducted on a dual-socket Intel Xeon Platinum 9242 node with 96 cores and a STREAM TRIAD bandwidth of 464 Gbyte/s. For compilation the Intel compiler version 19.1.3 was used. The GPU experiments were performed on an NVIDIA Tesla V100 connected via PCI-Express. The GPU kernels were compiled using CUDA v10.2 with GCC 8.1.0 as host compiler. The V100 GPU achieves a STREAM TRIAD bandwidth of 840 Gbyte/s, similar to that of A64FX.
ARCHITECTURAL ANALYSIS

3.1 In-core

To get a better understanding of the in-core behavior of the A64FX microarchitecture, a schematic block diagram of one core’s front-end and back-end components is shown in Fig. 1. Instructions are fetched from the L1 instruction cache with a bandwidth of 32 byte/cycle. Each core’s front end has an instruction buffer with 6×8 entries, which can feed six instructions, also called macro-operations (MOP), per cycle to the decoder. The decoder feeds up to four micro-operations (μ-ops) per cycle to the different reservation stations (RS), which then schedule the μ-ops to the corresponding execution pipelines. The reservation stations RSA0 and RSA1 are used for address generation and load units and have ten entries each, while reservation stations RSE0 and RSE1 are used for arithmetic execution and store units and have 20 entries each. The reservation station RSBR with its corresponding pipeline is only used for branching and has 19 entries. Excerpts of the execution units of the residual pipelines FL[A|B], PR, EX[A|B], EAG[A|B] are shown in boxes below the pipeline name. While RSA0 and RSA1 can schedule instructions to both EAG pipelines, all other RS are limited to their corresponding pipelines, even if an execution unit with equivalent functionality exists in a pipeline outside their scope. Load (LD) and store (ST) instructions are fed to the fetch port and store port, respectively, which execute the requests in parallel to the operation flow.

The small capacity of the reservation stations in combination with high instruction latencies can result in inefficient out-of-order (OoO) execution, which emphasizes the importance of a compiler that is capable of exploiting the in-core performance by intelligent code generation. While these hardware constraints cannot be overcome completely, their impact can be alleviated by techniques such as loop unrolling, consecutive addressing and interleaving of different instruction types. These techniques have been beneficial in our benchmarks, see Secs. 4 and 5 for details. Neither the open-source GCC compiler (version 10.2.0) nor Fujitsu’s proprietary FCC compiler (version 4.4.0a) currently generate code that fully overcomes the hardware constraints, which is why we employed SVE intrinsics for our benchmarks.

To create an accurate in-core model of the A64FX microarchitecture, we analyze different instruction forms, i.e., assembly instructions in combination with their operand types, based on the methodology introduced in [8, 9]. Table 2 shows a list of instruction forms relevant for this work. Standard SVE load (ld1d) instructions have a reciprocal throughput of 0.5 cycle (cy), while stores (st1d) have 1 cy. The throughput of gather instructions depends on the distribution of addresses: “simple” access

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1 See [github.com/RRZE-HPC/OSACA](https://github.com/RRZE-HPC/OSACA) for a full set of measured instruction forms and the A64FX port model used in this work.
TABLE 2 In-core instruction throughput and latency (if applicable) for selected instruction forms.

| Instruction                  | Reciprocal Throughput [cy] | Latency [cy] |
|------------------------------|----------------------------|--------------|
| ld1d (standard)              | 0.5                        | 11           |
| ld1d (gather, simple stride) | 2.0                        | ≥ 11         |
| ld1d (gather, complex stride)| 4.0                        | ≥ 11         |
| simple gather + standard load| 3.5                        | –            |
| complex gather + standard load| 5.5                        | –            |
| st1d (standard)              | 1.0                        | –            |
| fadd                         | 0.5                        | 9            |
| fmad                         | 0.5                        | 9            |
| fmla                         | 0.5                        | 9            |
| fmul                         | 0.5                        | 9            |
| fcadd                        | 1.0                        | 15           |
| fcm1a                        | 2.0                        | 16           |
| fadda (512 bit)              | 18.5                       | 72           |
| faddv (512 bit)              | 11.5                       | 49           |
| while{le|lo|ls|lt}           | 1.0                        | 1            |

patterns are stride 0 (no stride), 1 (consecutive load) and 2, while larger strides and irregular patterns are considered “complex.” The former have lower reciprocal throughput and latency than the latter. However, when occurring in combination with a standard LD for loading the index array, we can observe an increase of reciprocal throughput by 1.5 cy instead of the expected 0.5 cy. This is caused by the dependency of the gather instruction on the preceding index load operation, which the OoO execution cannot hide completely. Note also the rather long latencies for arithmetic operations such as MUL, ADD and FMA compared to other state-of-the-art architectures (e.g., on Intel Skylake or AMD Zen2 these are between 3 cy and 5 cy).

The SVE instruction set introduced a “while{cond}” instruction to set predicate registers according to the elements in vector registers in a length-agnostic way in order to eliminate remainder loops. Although it is used extensively for SVE code, a port-conflict analysis revealed that this instruction does not collide with floating-point instructions or data transfers.

3.2 Chip topology and memory hierarchy

The chip is divided into four core memory groups (CMG) of twelve cores each. Every CMG is its own cache-coherent non-uniform memory access (ccNUMA) domain. The 64 KiB L1 cache is core-local, while 8 MiB of L2 are shared among the cores of a CMG. We refer to Table 1 for architectural details of the A64FX processor in the Fugaku system.

While parallel load/store from and to L1 cache is possible for general-purpose and NEON registers, different types of SVE data-transfer instructions in L1 cannot be executed in one cycle: Using SVE, one A64FX core can either load up to 2 × 64 byte/cy or store 64 byte/cy from/to L1. The L2 cache can deliver 64 byte/cy to one L1 but tops out at 512 byte/cy per CMG. The L1-L2 write bandwidth is half the load bandwidth, i.e., 32 byte/cy per core, and is capped at 256 byte/cy per CMG. Finally, the measured main-memory bandwidth per CMG is 227 Gbyte/s for read-only and 213 Gbyte/s for STREAM TRIAD. The memory bandwidth scales almost linearly with the CMGs and reaches a full-chip read-only bandwidth of 859 Gbyte/s and STREAM TRIAD bandwidth of 841 Gbyte/s. These measured bandwidths will be used as baselines for the memory-transfer bandwidth in the ECM model.

3.3 Special features of A64FX

The A64FX processor has some special hardware capabilities to improve the performance of some codes. In this section we look into three features, i.e., zero fill, hardware barrier and sector cache. Currently only the FCC compiler supports these features on high-level code.
3.3.1 Zero fill

A cache write miss causes a write-allocate transfer, i.e., the cache line must be read before it can be modified. However, this increases the memory traffic, thus reducing the effective bandwidth available to the application. Most processors therefore have a mechanism to avoid this additional traffic. On the A64FX processor a similar mechanism exists and is called zero fill. The zero fill instruction DC ZVA directly writes a cache line filled with zeros to the L2 cache. Therefore, the processor can load the cache line from L2 through L1 avoiding the read operation from main memory. This effectively increases the measured application bandwidth.

For simple codes the FCC compiler is capable of automatically detecting the arrays which only have write operations and will use the DC ZVA instruction. In order to enable this the -Kzfill compiler flag has to be used. Figure 2 shows the increase in application bandwidth when using zero fill for the STREAM TRIAD (a[i]=b[i]+s*c[i]) benchmark. The benchmark reads two double-precision arrays and writes to one array. The bandwidth reported by the benchmark assumes 24 bytes of data traffic per iteration (byte/it), which in reality is obtained only if the write-allocate operation is avoided. Without zero fill there would be an additional read operation costing an extra 8 byte/it, and thereby we only observe 3/4 th of the actual bandwidth. This difference can be seen in the figure.

3.3.2 Hardware barrier

Another feature of the A64FX processor is the hardware barrier. The hardware barrier allows for fast synchronization of threads using dedicated system registers. With the FCC compiler the hardware barrier can be activated by setting the environment flag FLIB_BARRIER to HARD.

To determine the cost of the barrier we measured the difference in time between two variants of a computationally intensive kernel (calculating the exponential of a number), one with omp barrier and the other without. Figure 3 compares the cost (in cycles) of hardware barrier and different types of software barriers for varying number of threads. The cost of the default software barrier used by the GCC and FCC compilers is shown in blue and red, respectively. We see that FCC has a small advantage here. However, when we direct FCC’s software barrier to use a spin waiting loop by setting the environment variable OMP_WAIT_POLICY to active, we see that the cost of the barrier drops further by 20%. The cost of GCC’s software barrier did not change by setting this environment variable. We see that the hardware barrier performs best and requires only 550 cy within one CMG. Going beyond the CMG (12 cores) the cost increases to almost 2200 cy. This is because the hardware barrier is only implemented within a CMG, while between CMGs a software barrier is used. Note that the results shown here are the statistics from ten runs as the run-to-run fluctuations in this experiment were higher than 5% for some cases.
3.3.3 Sector cache

Sector cache is a mechanism to partition a cache into different sectors of varying size. The application can then tag its data structures to be directed to one of the sectors. This allows for more control of the cache space allocated for each data structure in the code. For example, in case of a code with reuse on one array and streaming patterns on other arrays, one could direct the streaming arrays to a small sector of the cache to avoid polluting the cache space that could be used by the array having reuse. The sector size can be controlled with a granularity of cache ways. With the FCC compiler, pragma directives are used to activate the sector cache and to tag the arrays.

Figure 4 shows the impact of sector cache on a DAXPY-style dense matrix-vector multiplication (DMVM), for which the inner loop traverses a column of the matrix (see Listing 1). The DMVM kernel performs a multiplication of matrix $A$, stored in column-major format, with vector $x$ and writes the result into vector $y$. The matrix array $A$ does not have any reuse and therefore can be directed to one small sector of the cache. On the other hand, the vector array $x$ is reused all the time, and the vector array $y$ is reused if its size is small enough to fit in the cache. In the experiment we fix the number of rows to 192 and vary the number of columns, i.e., $x$ is fixed to length 192 and the length of $y$ is variable. In Fig. 4a we plot the performance as a function of the size of $y$. The different lines in the figure correspond to the different sizes of the cache sector allocated for matrix array $A$. The black line corresponds to the case without any use of sector cache. It can be seen that as the size of the vector $y$ increases to about 2 MB the performance starts to drop as the vector $y$ can no longer be kept in L2. The drop in performance can be correlated with an additional memory data traffic of 16 bytes (see Fig. 4b) due to the read and write of vector $y$. However, if we restrict the space available to matrix $A$, the vector $y$ has more cache space available, and therefore the kernel can sustain the high performance level until almost 5 MB. Restricting the cache available to matrix $A$ to a very small size of 1 cache way is, however, not optimal since this leads to an early eviction of the prefetched elements of the matrix $A$. Obviously, the performance is also worse if we allocate almost all cache space (12 out of 14 allocatable ways) of L2 to the matrix $A$. Note that due to the high cost of the initial invocation of the sector cache (almost 500 milliseconds) the first call to the DMVM kernel is not included in the performance results.

4 CONSTRUCTION OF THE ECM MODEL

Given the information about in-core execution and data traffic across all data paths in the memory hierarchy gathered in Secs. 3.1 and 3.2, a performance model for the A64FX can be constructed. The Execution-Cache-Memory (ECM) model is an analytical performance model for streaming loop kernels with regular data-access patterns and equal amount of work per loop iteration, using first principles and machine-dependent constraints. As opposed to the roofline model, the ECM model can identify execution and data transfer bottlenecks for single-threaded programs and predict the scaling behavior of loops across the cores of a multicore chip. It also allows one to take into account overlapping or non-overlapping data transfers within the cache hierarchy. The roofline model always assumes full overlap of all time contributions.
FIGURE 5 Runtime of SVE loop kernels vs. problem size, comparing no unrolling (black) and eight-way unrolling (blue). Both versions are using 2 MiB huge pages. Arrays were aligned to 1024-byte boundaries. While huge pages were used by default, the extra green line denotes the usage of standard 64 KiB pages. The orange line in (a) shows the TLB misses on 2 MiB pages. For the 2D5PT stencil the outer and inner dimension was set at a ratio of 1:2.

4.1 Time contributions

The ECM model of the A64FX contains four different time contributions:

1. \(T_{c\_OL}\): execution time for in-core instructions that can overlap with data transfers. These are all instructions except loads. This also includes the cycles generated by the store instructions on the FLA and EXA pipelines.

2. \(T_{L1\_LD}\): time for in-core load data traffic between registers and L1 cache.

3. \(T_{L1\_ST}\): time for in-core store data traffic between registers and L1 cache.

4. Data transfer time between any other memory hierarchy levels: \(T_{L2}\) for data between L1 and L2, and \(T_{Mem}\) for data between L2 and main memory.

Combining these contributions, the single-core runtime prediction for the A64FX is defined as

\[
T_{ECM} = \max \left( T_{c\_OL}, f(T_{L1\_LD}, T_{L1\_ST}, T_{L2}, T_{Mem}) \right),
\]

where \(f\) is a combination of sum and max operators depending on the overlap hypothesis, which will be discussed in Sec. 4.2

For \(T_i\) with \(i \in \{c\_OL, L1\_LD, L1\_ST\}\) the time contributions are determined by a static analysis of the assembly code using the OSACA tool. For \(T_i\) with \(i \in \{L2, Mem\}\) the time contributions are given by

\[
T_i = V_i / b_i,
\]

where \(V_i\) is the data volume transferred and \(b_i\) is the bandwidth between memory hierarchy level \(i\) and the next lower level\(^\dagger\). The \(V_i\) include write-allocate transfers due to store misses where applicable. Latency effects are neglected.

4.2 Overlap hypothesis

Depending on the architecture the data transfer contributions may or may not overlap, i.e., the function \(f\) in Eq. (1) has to be determined. In order to find out which of the time contributions for data transfers through the cache hierarchy overlap, measurements for a test kernel are compared with predictions based on different hypotheses, see [10] for an in-depth description of this iterative process. If a hypothesis works for the test kernel, it is tested against a collection of other kernels with different characteristics to validate or invalidate the hypothesis.

Here we use the STREAM TRIAD kernel, \(a[i] = b[i] + 8* c[i]\), to narrow down the possible overlap scenarios. This kernel has two LD, one ST and one FMA instruction per SVE-vectorized iteration, which corresponds to eight high-level iterations.

\(^\dagger\)Lower means closer to the cores, e.g., L1 is lower than L2.
Figure 5a shows performance in cycles per VL for different code variants: “u=1” denotes no unrolling (apart from SVE) and “u=8” is eight-way unrolled on top of SVE. Some level of manual unrolling (typically eight-way) is usually required for best in-core performance. This is even more important in kernels where dependencies cannot be resolved easily by the out-of-order logic. Measurements of the STREAM TRIAD kernel with 64 KiB pages show performance degradation starting at 64 MiB due to TLB (translation lookaside buffer) misses after all 1024 entries of the L2 data TLB are used. The Fujitsu compiler suite uses 2 MiB large pages (also called huge pages) by default (-Klargepage option). For other compilers, the software environment on the Fugaku system provides the LIBMPG library and a custom linker script. TLB measurements of the STREAM TRIAD kernel with 2 MiB pages in Fig. 5a show a rise in TLB misses when the working set size exceeds 2 GiB. Despite the occurrence of TLB misses, there is no observable drop in performance. For all further measurements in this work, a page size of 2 MiB is used.

Figure 6 compares four overlap scenarios (a), (b), (c) and (d) with measured cycles per VL (e). Note that there is a large number of possible overlap hypotheses, and we can only show a few here. The one leading to the best match with the STREAM TRIAD data (shown in Fig. 6d) is the following:

- L1 is partially overlapping: Cycles in which STs are retired in the core can overlap with L1-L2 (or L2-L1) transfers, but cycles with LDs retiring cannot.
- L2 is fully overlapping: Cycles in which the memory interface reads and writes data from and to memory can entirely overlap with transfers between L2 and L1.

The overlap hypothesis (d) implies that the function $f$ in Eq. (1) has the form

$$f(T_{L1,LD}, T_{L1,ST}, T_{L2}, T_{Mem}) = \max(T_{L1,LD} + \max(T_{L1,ST}, T_{L2}), T_{Mem}).$$

The overlap hypothesis (c) was used in previous work [1] and applies for standard 64 KiB pages.

In Fig. 5b we show performance data and ECM model for a 2d five-point stencil, where SVE vectorization alone (without further unrolling) seems unable to resolve dependencies via OoO execution, leading to up to 2× slower code than the eight-way unrolled kernel despite the lack of loop-carried dependencies. Figure 5c shows performance data and ECM model for a sum reduction, $s+=a[i]$, which requires eight-way modulo variable expansion (MVE, see Sec. 5.2) on top of SVE in order to hide the large latency of the floating-point ADD instruction.

### 4.3 Multicore

For multiple cores within a CMG, the naive scaling hypothesis of the ECM model assumes perfect bandwidth scaling across all cores of the CMG until the main memory bandwidth bottleneck $b_{Mem,CMG}$ of the CMG is hit. If only a single core is active the memory bandwidth attained by a certain application $\frac{V_{Mem}}{T_{ECM}}$ is

$$B(1) = \frac{V_{Mem}}{T_{ECM}}.$$

Assuming linear scaling of the memory bandwidth with the number of active cores, the number $N_s$ of cores required to attain the full bandwidth $b_{Mem,CMG}$ of one CMG is thus

$$N_s = \left\lfloor \frac{b_{Mem,CMG}}{B(1)} \right\rfloor.$$

Therefore, the ECM prediction can be extended to a function of a variable number $n$ of cores,

$$T_{ECM}(n) = \frac{T_{ECM}(1)}{\min(n, N_s)}.$$

For $b_{Mem,CMG}$ we use the read-only bandwidth of 227 Gbyte/s if the application is dominated by loads and the STREAM TRIAD bandwidth of 213 Gbyte/s otherwise. If the application cannot saturate $b_{Mem,CMG}$, $N_s$ will be larger than 12.

Going beyond a single CMG we again assume linear scaling since each CMG constitutes its own ccNUMA domain and each domain is connected to its own HBM stack. The full-chip memory bandwidths $b_{Mem}$ for read-only and TRIAD are given in Table 1.

### 4.4 Validation of the ECM model for streaming kernels

With the in-core and data-transfer models in place we can now test the ECM model against a variety of loop kernels. Table 3 shows a comparison of predictions and measurements. For each kernel, three numbers represent the cycles per VL with the data

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*We use lowercase characters for architectural parameters and uppercase for observed or predicted quantities.*
FIGURE 6 Comparing different overlap scenarios (a), (b), (c) and (d) for data transfers in the memory hierarchy with measured cycles per VL (e) on the STREAM TRIAD kernel. Note that (c) is the appropriate overlap hypothesis for standard (64 KiB) pages.

TABLE 3 ECM model predictions and measurements in [cy/VL] for different streaming kernels on a single core. Red color indicates a deviation from the model of at least 15%. The optimal unrolling factor for each measurement is shown as a subscript.

| Kernel | Predictions | Measurements |
|--------|-------------|--------------|
| COPY (a[i]=b[i]) | {1.5 [4.5] 4.6} | (1.612 [4.413] 4.63) |
| DAXPY (y[i]=a[i]*x+y[i]) | {2.0 [5.0] 5.1} | (2.18 [4.716] 4.712) |
| DOT (sum+=a[i]*b[i]) | {1.0 [3.0] 3.1} | (1.78 [3.24] 3.34) |
| INIT (a[i]=s) | {1.0 [3.0] 3.1} | (1.013 [2.913] 4.01) |
| INIT4 (a[i]=s) | {4.0 [12.0] 12.3} | (4.12 [10.616] 10.616) |
| LOAD (load(a[i])) | {0.5 [1.5] 1.5} | (0.710 [2.34] 1.51) |
| LOAD4 (load(a[i])) | {2.0 [6.0] 6.1} | (2.54 [5.816] 5.91) |
| TRIAD (a[i]=b[i]+s*c[i]) | {2.0 [6.0] 6.1} | (2.18 [5.611] 5.71) |
| SUM (sum+=a[i]) | {0.5 [1.5] 1.5} | (1.111 [2.015] 2.31) |
| SCHÖNAUER (a[i]=b[i]+c[i]*d[i]) | {2.5 [7.5] 7.7} | (2.614 [7.04] 7.04) |
| 2D5PT - LC satisfied | {3.5 [6.5] 6.5} | (5.810 [6.56] 6.56) |
| 2D5PT - LC violated in L1 | {3.5 [8.5] 8.7} | (5.810 [8.67] 8.48) |
| 2D5PT - LC violated | {3.5 [8.5] 8.7} | (5.810 [8.67] 8.48) |

The results have been obtained by running each kernel with unrolling factors from 1 to 16 and taking the best result. Entries in red color have a deviation from the model of 15% or more. The strongest deviations occur in L1: Even with massive MVE, SUM

set in L1, L2 and memory, respectively. INIT4 and LOAD4 are versions of INIT and LOAD with four independent data streams. In case of the 2d five-point stencil, three cases are shown: layer conditions (LC) satisfied at L1, broken at L1 and broken at L2.

The results have been obtained by running each kernel with unrolling factors from 1 to 16 and taking the best result. Entries in red color have a deviation from the model of 15% or more. The strongest deviations occur in L1: Even with massive MVE, SUM

\(^1\)See [11] for a comprehensive coverage of layer conditions in the context of the ECM model and Sec. 6.3.1 below.
cannot achieve the architectural limit of 0.5 cy/VL. A similar deviation can be observed for the stencil kernels. We attribute this failure to insufficient OoO resources: A modified stencil code without intra-iteration register dependencies achieves a performance within 10% of the prediction. Deviations from the model with L2 and memory working sets occur mainly with kernels that have a single data stream. In fact, we can observe that the ≥ 15% deviation for both LOAD and INIT in L2 and memory, respectively, decreases to 3% and 14% when using four streams.

We now move from single-core to multicore analysis within one CMG. Figure 7 shows a comparison of the ECM-model predictions and measurements for the STREAM TRIAD, 2D5PT and SUM kernels. While STREAM TRIAD matches the prediction perfectly, for SUM it is evident that insufficient MVE (as shown in the “u=1” data) is the root cause for non-saturation of the memory bandwidth due to the long ADD latency. For the stencil kernel, saturation is possible even without unrolling, but more cores are needed.

5 | CASE STUDY: SPARSE MATRIX-VECTOR MULTIPLICATION

Sparse matrix-vector multiplication (SpMV) is arguably one of the most relevant numerical kernels in computational science. With the help of the insights gained in the construction of the ECM performance model, we are now going to analyze and optimize the performance of SpMV kernels on the A64FX. We restrict ourselves to general matrices without the option of exploiting symmetries or dense substructures.

Due to its low computational intensity of at most 1/6 flop/byte [12] (assuming double precision and four-byte indexing), SpMV is typically expected to be memory bandwidth bound on all modern computer architectures if the matrix does not fit into cache. Hence, the OpenMP-parallel kernel (i) should exhibit the typical saturating scaling characteristics of a memory-bound code across the cores of a CMG, (ii) should be able to exhaust the available memory bandwidth and (iii) should preferably show the maximum possible computational intensity as derived in [13].

In most algorithms, a left-hand-side vector $y$ is updated in the course of the SpMV operation: $y = y + Ax$. Due to the lack of store misses, zero fill instructions are thus unable to improve the performance here. However, since there is no cache reuse in the access to the matrix data but only in the right-hand-side vector, the sector-cache feature may be able to restrict the cache usage of the matrix, leaving more cache for the vector and thus helping to get close to the maximum intensity.

5.1 | Motivation

In order to provide a baseline for experiments with realistic sparse matrices, we start with a “tall and skinny” dense rectangular (dRECT) matrix stored in the Compressed Row Storage (CRS) format, also called Compressed Sparse Row (CSR) format. CRS
is the most popular sparse-matrix format, and it is usually well-suited for cache-based multicore CPUs. Listing 2 shows the corresponding high-level loop code. The dRECT matrix poses no challenges in terms of load balancing and right-hand-side access. The black line with symbols in Fig. 8a shows performance scaling on one CMG for a dRECT matrix with 4000 columns, using GCC with plain C code. It saturates at about 37 Gflop/s, which translates to a memory bandwidth of about 220 Gbyte/s assuming the maximum intensity of 1/6 flop/byte. Hence, we observe the expected pattern, although almost all cores are needed for saturation. In Fig. 8b we show a scan of the single-core SpMV performance with the dRECT matrix with respect to the number of nonzeros per row. The sharp drop towards small \( N_{nzr} \) reflects the inefficiency of short inner loops, which we will elaborate on later.

Unfortunately, the dRECT case is not representative of most realistic sparse matrices, even for those with “benign” structures. The red line in Fig. 8a shows performance scaling for the HPCG matrix (problem size \( 128^3 \), \( N_{nzr} = 27 \)). In this case, the single-core performance is only about half of that for the dRECT matrix, thus bandwidth saturation cannot be achieved. The cause of this failure is the generated assembly code: Although the compiler can vectorize the inner kernel along the matrix row, it accumulates the results into a single target register, which incurs the full fma latency of 9 cy in every SIMD loop iteration. At \( N_{nzr} = 27 \), the inner loop has four iterations. Together with the latency of the required horizontal add instruction (faddv) of 49 cy, one row requires \( 4 \times 9 + 49 \approx 85 \) cy to execute. Assuming again the maximum computational intensity, this translates into a maximum full-CMG bandwidth of

\[
12 \text{ (cores)} \times 2.2 \text{ Gcy/s} \times 27 \times 12 \text{ byte/85 cy} \approx 101 \text{ Gbyte/s}
\]

(a) Strong scaling of SpMV with the dRECT matrix \( (N_{nzr} = 4000) \) and the HPCG matrix (problem size \( 128^3 \)) using the CRS format across the cores of a CMG.

(b) Single-core performance of SpMV with the dRECT matrix versus \( N_{nzr} \). The ECM model prediction is shown for reference. The working set size for the matrix was kept constant at 500 MiB.

**FIGURE 8** Performance of SpMV with CRS format, compiled using GCC.
and a maximum performance of 16.8 Gflop/s. Note that we did not consider the data transfers through the memory hierarchy since the overlapping part of the in-core execution dominates strongly. In practice, successive row executions can overlap slightly, which explains our measurement of 20 Gflop/s. Clearly the accumulation of partial sums into a single register is part of the problem. A solution to this problem will be discussed next.

5.2 | Modulo Variable Expansion (MVE)

MVE [14] accumulates partial sums into several registers, allowing for substantial overlapping of successive `fmla` instructions. The downside is that the computation of the final per-row result becomes more expensive since the reduction involves more registers. The FCC compiler can automatically employ MVE and produces two code paths, with and without MVE. Which path is taken is determined at runtime depending on the inner loop length. The GCC compiler does not employ modulo variable expansion (MVE) even when a `#pragma unroll` directive is used. Hence, from now on we revert to compiler intrinsics for all unrolled kernels to exert more control over the code generation.

We start by investigating the dRECT case. Figure 9a shows performance scaling at \( N_{nzr} = 4000 \). Unrolling by two or three with MVE clearly helps to boost the single-core performance and thus achieves stronger saturation\(^8\) at around eight cores with GCC. As can be seen in Fig. 9b, this optimization is effective only if \( N_{nzr} \) is not too small, because the additional overhead for the final reduction cannot be amortized if the number of iterations in the inner loop is small. At an intensity of 1/6 flop/byte, a single-core performance of about 3 Gflop/s is required to saturate the CMG memory bandwidth with all cores. This becomes possible starting at \( N_{nzr} \gtrsim 50 \), but a significantly higher number is necessary to achieve strong saturation. Consequently, the CRS format is unable to yield best performance for matrices from many application fields: Fig. 9c shows performance scaling with and without MVE for the HPCG matrix (\( N_{nzr} = 27 \)). Saturation is not within reach.

The fundamental dilemma with the CRS format on A64FX is that SIMD vectorization and MVE must both be implemented within the inner loop. As a result, the inner loop becomes too short for effective in-core latency hiding on realistic matrices. Other storage formats such as SELL-C-\(\sigma\) can mitigate this problem.

5.3 | SELL-C-\(\sigma\)

SELL-C-\(\sigma\) [13] is a sparse-matrix storage format suited for a broad range of architectures with wide SIMD or SIMT units. To convert a matrix to SELL-C-\(\sigma\), its rows are first sorted within blocks of \(\sigma\) rows (the sorting range) according to the number of

\(^8\)Strong saturation means saturation at a number of cores much smaller than the total number of cores.
FIGURE 10 A sparse matrix with $N_r = 24$ rows (left) and the SELL-6-12 data structure generated from it (right). The blue boxes are nonzero entries, and the gray boxes are the zero fill-in. The arrows indicate the storage order. For illustration purposes, a column of nonzero entries is marked in dark blue in the SELL-6-12 figure; the corresponding entries are shown in the original matrix as well. Note that the permutation is applied to row and column indices alike.

nonzero entries. Within each block of sorted rows, the nonzeros are stored in column-major format in chunks of height $C$ (the chunk size). The columns of each chunk are zero-padded if necessary so that each row within a chunk has the same length. See Fig. 10 for an illustration.

The inner loop of the corresponding SpMV code goes over one column of a chunk of height $C$ (see Listing 3). This means that $C$ should be a (small) multiple of the SIMD width, but large enough so that successive iterations of the loop, which accumulate into different target registers, can fill the bubbles in the fma pipeline. Furthermore, no expensive horizontal reductions (faddv) are required. Due to the chunk padding, remainder loops cannot occur and all SIMD lanes are filled. The second-innermost loop goes over the columns of a chunk and is as long as the chunk width, i.e., $N_{nzr}$ on average. Disadvantages of the SELL-$C$-$\sigma$ format include possible excessive zero fill-in for very irregularly-shaped matrices, and a potential impact of the row sorting on the access to the right-hand-side vector.

Figure 11a shows SpMV performance versus $N_{nzr}$ using the dRECT matrix, comparing the CRS format (with the FCC compiler), SELL-8-1 with GCC, and SELL-16-1 with GCC and FCC. We also give the ECM-model predictions for the SELL cases. SELL-$C$-$\sigma$ is able to keep close to the model even for small $N_{nzr}$, owing to the advantages shown above. Even with $C = 8$, which does not allow for mitigation of the pipeline stall on the fma instruction, the performance loss at low $N_{nzr}$ is small because of the absence of an expensive reduction after the loop across the chunk. At $C = 16$ the stall penalty is cut in half and leads to a significant performance boost. Note also that there is a distinctive drop in performance for the CRS format at $N_{nzr} \approx 4000$, which is caused by the right-hand-side vector not fitting in the L1 cache anymore. No such drop is visible for SELL-$C$-$\sigma$ because the vector elements are reused along the columns of a chunk.

Figure 11b shows performance scaling of SpMV for the HPCG matrix, comparing the same setups as in Fig. 11a. As expected, the fastest single-core version (SELL-16-1) also exhibits the strongest saturation at nine cores. SELL-8-1 is also able to saturate but requires all cores on the CMG.

Finally, we compare the SELL-$C$-$\sigma$ format with CRS on a range of matrices on the full A64FX chip (four CMGs) in Fig. 12. Table 4 lists the properties of the test matrices. The matrix-specific memory-bound roofline limit, i.e., assuming optimal reuse of the right-hand-side vector [13], is shown for reference. We used three tuning parameters to find the best per-matrix performance: (i) Reverse Cuthill-McKee (RCM) reordering, (ii) row-based vs. nonzero-based load balancing and (iii) $\sigma$ in the range of 1 to 4096.

SELL-$C$-$\sigma$ provides superior performance to CRS for almost all matrices. Exceptions exist where the access pattern to the right-hand-side vector changes for the worse compared to CRS. The difference between $C = 8$ and $C = 16$ is generally small.
(a) Single-core SpMV performance with the dRECT matrix versus $N_{nzr}$, comparing the CRS format (gray, using FCC) with SELL-8-C-σ using different values of $C$ and compilers.

(b) Strong scaling of SpMV within a CMG with the HPCG matrix.

\[ \text{FIGURE 11} \] SpMV performance with SELL-C-σ.

\[ \text{FIGURE 12} \] Influence of the sparse-matrix storage format on the SpMV performance for CRS, SELL-8-σ, and SELL-16-σ on the full A64FX chip (48 cores). The best value of $\sigma$ was determined by exhaustive search in the range 1, …, 4096 for each matrix separately. Matrices are sorted from left to right in ascending order according to the number of nonzeros. The sector-cache feature was not used. Diamonds show the matrix-specific roofline limits (RLM).

The significant gaps between measurement and model have a variety of reasons: Some matrices, such as scail and scai2, have a small $N_{nzr}$ and a structure that leads to cache-unfriendly access patterns, thereby inhibiting saturation. In other cases, such as kkt-power, the matrix exhibits a strong imbalance of row lengths, making load balancing hard especially across CMGs (i.e., ccNUMA domains).
TABLE 4 Details of the benchmark matrices. \( N_r \) is the number of rows, \( N_{nz} \) is the number of nonzeros, and \( N_{nzr} \) is the average number of nonzeros per row. Most matrices were taken from the SuiteSparse Matrix Collection [13]. The matrices with \* come from other research projects.

| Index | Matrix name             | \( N_r \) | \( N_{nz} \) | \( N_{nzr} \) |
|-------|-------------------------|-----------|-------------|--------------|
| 1     | scircuit                | 170,998   | 958,936     | 5.61         |
| 2     | qcd5_4                  | 49,152    | 1,916,928   | 39.00        |
| 3     | pdb1HYS                 | 36,417    | 4,344,765   | 119.31       |
| 4     | Hamrle3                 | 1,447,360 | 5,514,242   | 3.81         |
| 5     | G3_circuit              | 1,585,478 | 7,660,826   | 4.83         |
| 6     | shipsec1                | 140,874   | 7,813,404   | 55.46        |
| 7     | pwtk                    | 217,918   | 11,634,424  | 53.39        |
| 8     | kkt_power               | 2,063,494 | 14,612,663  | 7.08         |
| 9     | Si41Ge41H72             | 185,639   | 15,011,265  | 80.86        |
| 10    | bundle_adj              | 513,351   | 20,208,051  | 39.36        |
| 11    | msdoor                  | 415,863   | 20,240,935  | 48.67        |
| 12    | scai1*                  | 3,405,035 | 24,027,759  | 7.06         |
| 13    | Fault_639               | 638,802   | 28,614,564  | 44.79        |
| 14    | af_shell10              | 1,508,065 | 52,672,325  | 34.93        |
| 15    | HPCG-128-128-128        | 2,097,152 | 55,742,968  | 26.58        |
| 16    | Serena                  | 1,391,349 | 64,531,701  | 46.38        |
| 17    | bone010                 | 986,703   | 71,666,325  | 72.63        |
| 18    | audikw_1                | 943,695   | 77,651,847  | 82.28        |
| 19    | channel-500x100x100-b050| 4,802,000 | 85,362,744  | 17.78        |
| 20    | rrze3*                  | 6,201,600 | 92,527,872  | 14.92        |
| 21    | nlpkkt120               | 3,542,400 | 96,845,792  | 27.34        |
| 22    | delaunay_n24            | 16,777,216| 100,663,202 | 6.00         |
| 23    | ML_Geer                 | 1,504,002 | 110,879,972 | 73.72        |
| 24    | FreeFermionChain-26*    | 10,400,600| 140,616,112 | 13.52        |
| 25    | Spin-26*                | 10,400,600| 145,608,400 | 14.00        |
| 26    | scai2*                  | 22,786,800| 160,222,796 | 7.03         |

5.4 | SpMV and the sector cache

The sector-cache feature is expected to have a positive effect on the SpMV performance in cases where the cache is too small to ensure perfect reuse of the right-hand-side vector after it is loaded from memory. Restricting the number of cache ways used for the matrix data leaves more space for the vector, possibly increasing the computational intensity. Since invoking the sector cache comes with considerable overhead (see Sec. 3.3.3) we activate it outside the repetition loop. This is compatible with the structure of many sparse algorithms, where the same matrix is applied repeatedly to different vectors. Best results were obtained by allotting four ways of L2 and one way of L1 to the matrix data (nonzeros and index structures). The tuning space of Sec. 5.3 was enlarged by the chunk size \( (C \in [1, 128]) \).

In Fig. 13 we show the impact of the sector cache on SpMV performance for the test matrices, comparing with the FCC compiler without sector cache and with GCC (which does not support sector cache). The largest benefit is observed with medium-sized matrices, where the additional cache space makes a difference for the right-hand-side-vector data reuse. Matrices like qcd5-4, which just about fit in the L2, suffer because the restricted cache space forces the matrix data into memory.

We include the GCC data in the plot because, although GCC does not support the sector cache on the A64FX, it produces better code from the intrinsics than FCC, which can be observed for some of the smaller matrices.
5.5 Comparison with the Fujitsu SSL library

Fujitsu provides the “C-SSL II Thread-Parallel Capabilities” library, which contains SpMV routines for a variety of formats: Compressed Sparse Columns (CSC, function `c_dm_vmvscc`), ELLPACK (function `c_dm_vmvse`), and Diagonal (DIA) storage. Since DIA is only suited for matrices with diagonal structures, we ignore it here. Figure 14 compares our SELL-C-σ and CRS implementations with the C-SSL library. The tuning space of Sec. 5.4 was enlarged by the sector-cache setting (on/off, same number of ways as in Sec. 5.4). The results show that the SpMV implementations in the current version of the C-SSL library are not competitive.
FIGURE 15 Comparison of the effects of different power settings on node performance and energy consumption for SpMV, reporting the median (bars), minimum and maximum (whiskers) over all benchmark matrices. The power dissipation varies between 130 W and 190 W for the “hottest” setting (eco = 0 and f = 2.2 GHz) and between 76 W and 133 W for the “coolest” setting (eco = 2, f = 2.0 GHz).

5.6 Power consumption and tuning knobs

We explored two of the tuning knobs provided by the FX100 system to optimize the energy consumption of the A64FX processor: the clock speed (2.0 GHz or 2.2 GHz) and the “eco” setting, which can be 0 (disabled), 1, or 2. For a strongly memory-bound code like the SELL-C-σ variant of SpMV on “benign” matrices, we expect that lowering the clock speed will have a negligible impact on the performance but at least a proportional influence on the power consumption (depending on the voltage scaling, for which details are undisclosed). Enabling eco mode, which includes disabling the FLB floating-point unit, should also be inconsequential for performance but probably advantageous for power.

Figure 15 shows the median, maximum and minimum performance and node energy consumption (in nJ/flop) for SpMV over all benchmark matrices, comparing all six combinations of the three eco settings and the two clock speeds. As expected, all settings have a minor impact on the performance. The low-clock-speed setting reduces the performance median by 2.7% but lowers the energy consumption by about 13%. The “eco=2” mode can additionally reduce the energy consumption by another 21%, for a total average of 31%. In light of the fact that not all SpMV executions are memory bandwidth bound, these are surprisingly large savings. Although the actual energy measurements fluctuate significantly because of the wide range of performance numbers, the general trend is the same even for the “hottest” and “coolest” cases.

Note that all measurements were taken on a single node of Fugaku. Significant statistical variations across nodes are expected, but a full coverage is beyond the scope of this paper.

5.7 Comparison with other architectures

We choose one contemporary, high-end GPU and CPU architecture each to provide context for the SpMV performance of the A64FX: an NVIDIA V100 GPU and an Intel Cascade Lake AP (CLX-AP) node. On the V100 we use the GHOST library [16] for an efficient implementation of the SELL-C-σ format. The search space of Sec. 5.5 was extended on A64FX by the choice of compilers, GCC vs. FCC.

Figure 16 shows the results on all three systems, separately for “small” and “large” matrices, the boundary being defined by the aggregate L2/L3 cache size of the CLX-AP. Unsurprisingly, the CLX-AP performs best for most small working sets. On in-memory matrices, Fugaku and the V100 show an approximate 1.6× – 2× speedup with respect to CLX-AP for “benign” matrices, which is in accordance with the memory-bandwidth ratio[**]With irregular matrices (e.g., Hamrle3, kkt_power, scai1/2, **Note that a Cascade Lake SP system has only half the memory channels of CLX-AP, so we expect the speedup to double in that case.
FIGURE 16 Comparison of SpMV performance on A64FX with other architectures. Note the different range of the vertical axis for the two graphs.

Spin-26, or FreeFermionChain-26), the GPU has a clear advantage due to its more effective latency hiding. The bundle-adj matrix has low performance on V100 due to GHOST only supporting row-based load balancing.

6 | CASE STUDY: LATTICE QCD DOMAIN WALL KERNEL

6.1 | Introductory remarks

Understanding the strong interaction, one of the four known fundamental forces in nature, is one of the major challenges in physics. Quantum Chromodynamics (QCD) is the quantum field theory of the strong interaction, which describes the interaction of quarks and gluons. Lattice QCD is a computer-friendly version of QCD, in which simulations are carried out on a regular lattice in Euclidean space-time. State-of-the-art research in Lattice QCD requires supercomputers such as Summit or Fugaku.

A significant part of the CPU time in Lattice QCD simulations is spent on solving a linear system of equations using iterative (multi-grid) techniques. The key computational kernel is the application of the lattice Dirac operator to a quark-field vector $\Psi$.

The quark field $\Psi(n,a)$ defined at lattice site $n$ in a four-dimensional volume $V_4 = L_x \times L_y \times L_z \times L_t$ carries a spinor index $a = 1, 2, 3, 4$ and a color index $a = 1, 2, 3$. The interaction is represented by SU(3) matrices $U_\mu(n)$, $n \in V_4$, carrying color indices. This matrices are defined on the links between adjacent sites $n$ and $n + \hat{\mu}$, where $\hat{\mu}$ is the unit vector in direction $\mu$.

Multiple formulations of quarks on the lattice exist. In this work we focus on the domain wall (DW) fermion formulation [17], in which the physical quark field $\psi(n,s,a)$ lives on the four-dimensional boundary of a five-dimensional space-time lattice with volume $V_4 \times L_s$. The formulation involves a fermion field $\psi(n,s,a)$ that lives in five dimensions and carries an additional index $s = 1, \ldots, L_s$. The interaction $U_\mu(n)$ does not depend on the fifth dimension and is replicated along the $s$-direction. The performance-relevant part $D$ of the domain wall Dirac operator acts on the fermion field as follows.

$$\psi'(n,s,a) = (D\psi)(n,s,a) = \sum_{\mu=1}^{4} \sum_{\beta=1}^{4} \sum_{b=1}^{3} \left\{ U_\mu(n)_{ab}(1 + \gamma_\mu)_{ab}(\psi(n + \hat{\mu},s)_{\beta b} + U_\mu^T(n - \hat{\mu})_{ab}(1 - \gamma_\mu)_{ab}\psi(n - \hat{\mu},s)_{\beta b} \right\}. \quad (8)$$

Here, the $\gamma_\mu$ are constant $4 \times 4$ Dirac matrices carrying spinor indices. The result of the projection $(1 \pm \gamma_\mu)\psi$ is a four-component spinor for each color. Up to multiplicative factors only two components each are independent. The number of input operands per

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*The full operator is given in [18], Eqs. (2.5)–(2.7). Our $D$ corresponds to their $D^{(0)}$ with $M = 4$.\footnote{\textsuperscript{17}}*
FIGURE 17 Illustration of RIRI and RRII data layouts for a 512-bit SIMD width. R’s refer to real and I’s to imaginary parts of double-precision complex numbers.

Listing 4 Simplified view of the domain wall kernel. \( L_x, L_y, L_z \) and \( L_t \) are the lattice sizes in the \( x, y, z \) and \( t \) dimensions, respectively, and \( s \) is the innermost fifth dimension with extent \( L_s \).

site is \( 8 \times 9 \) for the \( U \)-fields and \( 8 \times 12 \) for the \( \psi \)-fields. The number of output operands is \( 1 \times 12 \) for the \( \psi^\dagger \)-field per site. All these operands are complex numbers.

Grid [19] is a Lattice QCD software framework written in C++ with OpenMP and MPI parallelization. A variety of architectures are supported, including all Intel x86 SIMD extensions, Arm NEON and 512-bit SVE [20, 21] and GPGPUs. Grid achieves 100% SIMD efficiency on all architectures by combining template meta-programming and intrinsics where available. The data layout for complex numbers interleaves real and imaginary parts, i.e., the numbers are stored as RIRI, where R/I stands for a real/-imaginary part (see Fig. 17a). Using the SVE instruction set, hardware processing of these operands are complex numbers.

In this work we study the performance of the DW kernel for different compilers. We also compare the interleaved data layout with an alternative “split” layout, where the real and imaginary parts are stored as RRII such that the R’s and I’s end up in separate vector registers. For example, double precision and a 512-bit SIMD width, we have eight consecutive R’s as shown in Fig. 17b. We use a subset of Grid [23], which we extended for studying CLX-AP and the A64FX [24]. CLX-AP only supports real arithmetics, therefore the interleaved layout implies permutations. On the A64FX we use hardware support for the computation of the interleaved layout and real arithmetics otherwise.

6.2 Code analysis

The domain wall kernel Eq. (8) is a radius-1 star-shaped stencil [25] without the center element. The input and output of the stencil operation are the fermion fields \( \psi(n, s) \) and \( \psi^\dagger(n, s) \), respectively. The interaction matrices \( U_\mu(n) \) and their inverses \( U^\dagger_\mu(n) \) can be considered as variable stencil coefficients. Listing 4 shows a simplified version of the DW kernel omitting color and spinor indices as well as boundary conditions. The stencil code loops over the four dimensions \( x, y, z \) and \( t \), and the fifth dimension \( s \). The input fermion \( \psi(n, s) \) is stored in the array \( I \), and the output fermion \( \psi^\dagger(n, s) \) in the array \( O \). The interaction matrices \( U \) and \( U^\dagger \) are stored in \( U \) for the forward and backward directions in \( x, y, z \) and \( t \). Application of \( (1 \pm \gamma_\mu) \) to \( \psi \) is arranged in two parts:
spinor projection $P$ and spinor reconstruction $R$.‡‡ The operations $P$ and $R$ are hard-coded and do not need any operands from memory. For each direction, the following computational sequence is applied:

1. $P$ projects the $(4 \times 3)$-component input fermion field in $I$ to a $(2 \times 3)$-component fermion field, where 2 means half-spinor and 3 is the number of colors.

2. Two matrix-vector multiplications are applied, one for each component of the half-spinor from step 1, using the same $3 \times 3$ matrix in $U$.

3. Reconstruction $R$ of the $(4 \times 3)$-component fermion field and addition to the output fermion field in $O$ (if applicable), which are combined in one step.

The sum of all projections in step 1 contributes 96 flops. Each matrix-vector multiplication in step 2 requires $3 \cdot 3 = 9$ complex multiplications and $2 \cdot 3 = 6$ complex additions. Each of the complex multiplications is worth six flops, and a complex addition is worth two flops. Considering two matrix-vector multiplications in step 2 we have $2 \cdot (9 \cdot 6 + 6 \cdot 2) = 132$ flops per direction. Since there are eight directions we have a total of $8 \cdot 132 = 1056$ flops. Reconstruction and summation of intermediate results in step 3 adds another $7 \cdot 4 \cdot 3 \cdot 2 = 168$ flops. Thus, the theoretical total flop count is $96 + 1056 + 168 = 1320$. The actual flop count depends on the code implementation. However, all performance results reported in this study will be based on 1320 flops per lattice site update (LUP).

The flop count along with the data traffic to and from main memory can be used to construct a roofline model (RLM) performance limit. Figure 18 shows the main-memory data traffic of a baseline implementation of the DW kernel measured using the likwid-perfctr tool. This baseline implementation uses RIRI layout, ACLE intrinsics and no prefetching. It can be seen that for the DW kernel we need approximately 1500 byte/LUP. The code intensity of the kernel can thus be estimated as $I = \frac{1320}{1500}$ flop/byte $= 0.88$ flop/byte. According to the roofline model, the performance estimate is given as $\min(p_{\text{peak}}, I \cdot b_{\text{Mem}})$, where $p_{\text{peak}}$ is the peak flop rate and $b_{\text{Mem}}$ is the saturated main-memory bandwidth of the hardware. For the A64FX, $p_{\text{peak}} = 3379.2$ Gflop/s and $b_{\text{Mem}} = 859$ Gbyte/s (see Table 1). The RLM thus predicts a memory-bound performance maximum of 756 Gflop/s.

Figure 18 shows the performance of the DW kernel on the full chip in comparison with the roofline prediction. The data structure in this version of the kernel uses the interleaved (RIRI) complex array layout. The code attains a performance close to 350 Gflop/s with GCC and 440 Gflop/s with FCC. The measurements fall short of the RLM limit by a factor of $2.1 \times$ and $1.7 \times$, respectively. In the following sections we will investigate the reasons for this significant deviation and explore optimization strategies.

‡‡ See [26] for the details of projection and reconstruction.

§§ The SVE instruction set supports complex multiply-add ($z_1 + z_2 \cdot z_3$), but lacks complex multiplication ($z_1 \cdot z_2$). Therefore, each matrix-vector multiplication requires three complex multiply-add instructions for each row, including one multiplication adding zero ($0 + z_1 \cdot z_2$). The latter implies an additional $2 \cdot 3 \cdot 2 \cdot 8 = 96$ flops on top of the 1320 flops per LUP for the RIRI implementation.
6.3 | ECM analysis, layer conditions and optimizations

The roofline model predicts that the main-memory bandwidth is the performance bottleneck for the DW kernel, but we observe almost linear scaling up to 48 cores (not shown here), indicating bottlenecks at the single-core level. The single-core performance is 8.2 and 10.3 Gflops using GCC and FCC, respectively. We use the ECM performance model discussed in Sec. I.2 to investigate this issue. To construct the model, we first need the ECM contributions $T_{c,OL}$, $T_{L1,LD}$, $T_{L1,ST}$, $T_{L2}$ and $T_{Mem}$ (see Sec. I.1). These must be combined using the overlap hypothesis described in Sec. I.2.

The L1-to-register contributions $T_{L1,LD}$, $T_{L1,ST}$ and the in-core computational contribution $T_{c,OL}$ can be estimated by analyzing the assembly code with the OSACA tool. For the data delays in the memory hierarchy, i.e., $T_{L2}$ and $T_{Mem}$, we need the data volume $V_i$ transferred over each data path $i$ and the corresponding hardware bandwidth $b_i$ (see Sec. I.1) to plug into Eq. (2). The data traffic can be modeled analytically, which can be done for stencil codes using layer conditions [27, 11, 28]. Comparison of the prediction with performance counter measurements helps to validate the model and can reveal bottlenecks due to the code implementation and/or compiler code generation.

6.3.1 | Layer conditions

Layer conditions (LC) provide important information about which cache can hold which elements of the stencil and about the amount of data that must be transferred from and to a cache. The concept is based on reuse distance analysis, i.e., the distance after which a certain element of the stencil is reused. Since stencils have a well-defined regular access pattern, this reuse distance can be determined analytically. The LC analysis assumes caches with infinite associativity and least recently used (LRU) replacement policy. Real caches, such as on the A64FX, have finite associativity and might only implement a pseudo-LRU policy. However, it has been shown in [11, 29] that for most stencil codes these assumptions do not hamper the quality of the predictions. For simplicity we assume in the following that the lattice is sufficiently large such that the working set does not fit into cache.

Data traffic analysis

To construct the LC we need to analyze the data access patterns in the stencil code (Listing 4). We can neglect projections $P$ and reconstructions $R$ since these do not contribute to data traffic. The innermost loop is along the $s$ dimension, followed by the $x$, $y$, $z$, and $t$ dimensions. The elements of the array $U$ are $3 \times 3$ matrices, whose entries are of type double complex (16 bytes), while the elements of the arrays $I$ and $0$ are $4 \times 3$ double complex matrices. Within a LUP and without data reuse we need to load eight $U$ elements of dimension $3 \times 3$ each and eight $I$ elements of dimension $4 \times 3$ each, and then store one $0$ element of dimension $4 \times 3$. In total, we touch $(8 \cdot 9 + 8 \cdot 12 + 12) \cdot 16 = 2.88$ kB in each LUP.

The elements of $U[[x] [t] [z] [y] [x]]^T$ are independent of the $s$ loop and are touched again after a single LUP. Therefore, if a cache $i$ of size $s_i$ can hold all the elements required to compute a single lattice site, i.e., if $s_i > 2.88$ kB, then these elements can be reused in the cache $i$. In this case, the next higher memory hierarchy level $j$ has to deliver eight $U$ elements only once per traversal of the $s$ loop, and therefore the data traffic $V_j$ will correspond to $(8 \cdot 9 / L_s + 8 \cdot 12 + w \cdot 12) \cdot 16$ byte/LUP. Here, $w$ is the write-allocate factor: We have $w = 2$ if write allocation applies, which is the case in our implementations because there is neither a zero fill intrinsic nor a compiler built-in function. The condition of optimal reuse in the $s$ dimension is labeled $LC_s$ in the following.

Once all the elements in the innermost $s$ loop are traversed, the next loop is along the $x$ dimension. Reuse of the element $I[[x] [z] [y] [x-1] [s]]$ can happen in this loop, since it was touched two $x$ iterations ago. In order to satisfy this reuse condition, a cache has to hold all the elements touched in the $s$-loop iteration for two iterations of the $x$ loop. Therefore the $LC_x$ condition reads $s_j > 2 \cdot L_s \cdot (8 \cdot 9 / L_x + 8 \cdot 12 + 12) \cdot 16$ bytes. If this condition is satisfied by cache $j$ then memory level $j$ only has to transfer seven elements of the array $I$ instead of eight, translating to $V_j = (8 \cdot 9 / L_x + 7 \cdot 12 + w \cdot 12) \cdot 16$ byte/LUP.

The other conditions $LC_y$, $LC_z$ and $LC_t$ are constructed along the same lines. A summary of LC along each dimension is shown in Table 5 (see the scalar code column).

Serial code and vectorization

Stencil codes are typically vectorized along the innermost dimension. However, in the Grid Lattice QCD framework [19], vectorization is implemented along the 4d space-time dimensions for two reasons: First, the extent $L_x$ of the fifth dimension would have to be a multiple of the vector length (VL=4 for the RIRI layout in double precision), which imposes restrictions on

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[11] Here $s$ refers to all eight directions.

[28] Higher means farther away from the core, e.g., L2 is higher than L1.
TABLE 5  LC for the DW kernel for scalar and vectorized code. To determine the data traffic from a certain cache $i$, its size $s_i$ (in bytes) has to be compared with each condition starting from the bottom row ($LC_j$) to top row (no reuse). The first condition that is met by the cache $i$ determines the layer condition it satisfies, and the next higher hierarchy level $j$ has a data transfer volume of $V_j$. In our case the write-allocate factor is $w = 2$. The $d$ factor accounts for the data layout and will be discussed in Sec. 6.3.4. For the RIRI (RRII) layout we have $d = 1$ ($d = 2$).

| Name  | $V_j$ in byte/LUP | $s_j >$ |
|-------|-------------------|---------|
| no reuse | $(8 \cdot 9 + 8 \cdot 12 + w \cdot 12) \cdot 16$ | 0 |
| $LC_t$ | $(8 \cdot 9/s_t + 8 \cdot 12 + w \cdot 12) \cdot 16$ | 2880 |
| $LC_s$ | $(8 \cdot 9/s_s + 7 \cdot 12 + w \cdot 12) \cdot 16$ | $2 \cdot L_z(8 \cdot 9/L_z + 8 \cdot 12 + 12) \cdot 16$ |
| $LC_y$ | $(8 \cdot 9/s_y + 5 \cdot 12 + w \cdot 12) \cdot 16$ | $2 \cdot L_z \cdot L_y(8 \cdot 9/L_y + 7 \cdot 12 + 12) \cdot 16$ |
| $LC_z$ | $(8 \cdot 9/L_z + 3 \cdot 12 + w \cdot 12) \cdot 16$ | $2 \cdot L_z \cdot L_y \cdot L_z(8 \cdot 9/L_z + 5 \cdot 12 + 12) \cdot 16$ |
| $LC_i$ | $(8 \cdot 9/L_i + 1 \cdot 12 + w \cdot 12) \cdot 16$ | $2 \cdot L_z \cdot L_y \cdot L_z \cdot L_i(8 \cdot 9/L_i + 3 \cdot 12 + 12) \cdot 16$ |

For scalar code: $s_j > 0$.

For 512-bit vectorized code: $s_j > d \cdot 8 \cdot L_z(8 \cdot 9/L_z + 8 \cdot 12 + 12) \cdot 16$.

The highlighted factors in Table 5 becomes $s_j > 4 \cdot 2 \cdot L_x \cdot L_y \cdot (L_z/2) \cdot L_z \cdot (8 \cdot 9/L_z + 3 \cdot 12 + 12) \cdot 16$ bytes. The highlighted factors 4 and 2 reflect the changes due to vectorization. LC for scalar and vectorized code are shown in Table 5. It can be seen that this kind of vectorization makes the layer conditions more stringent. However, compared to the traditional inner-loop vectorization approach it does not imply redundant L1-to-register loads and/or shuffle operations.

FIGURE 19 Illustration of the vectorization scheme for a lattice of size 8 each in the outermost dimensions $t$ and $z$. Complex elements from four different partitions are packed into one SIMD register. The ordering of lattice sites is shown with numbers.

FIGURE 20 Illustration of data sharing between four cores attached to the same shared cache for a local (virtual) lattice size of 8 each in the outermost dimensions $t$ and $z$ with periodic boundary conditions. Each color represents a different core. The dark-colored elements show the stencil accesses at a specific time. We observe that two cores access the same element in the $t$ direction.

the choice of $L_x$ that are specific to the underlying hardware architecture. Second, other Lattice QCD kernels do not use a fifth dimension and use the vectorization scheme in 4d space-time dimensions.

An MPI-style partitioning scheme is applied to define the mapping of lattice sites to SIMD registers. One 512-bit SIMD register of the A64FX can hold four complex numbers in double precision; therefore, the lattice is divided into four partitions. This is realized by cutting the outermost two dimensions in the 4d space-time in half, i.e., each of the four local (virtual) partitions has a size of $L_x \times L_y \times L_z/2 \times L_i/2 \times L_x$. Figure 19 illustrates the partitioning of the lattice and the mapping of lattice sites to SIMD registers. Note that the site numbering is not lexicographic: Adjacent elements of a SIMD register belong to different partitions. Therefore, a change in site numbering implies a change in the data access pattern, which must be taken into account in the construction of the LC. Access to all four partitions is identical, and we can account for this by only considering the access pattern within one local partition and multiplying the number of elements touched at each access by a factor of four. For instance, the $LC_i$ condition in Table 5 becomes $s_j > 4 \cdot 2 \cdot L_x \cdot L_y \cdot (L_z/2) \cdot L_z \cdot (8 \cdot 9/L_z + 3 \cdot 12 + 12) \cdot 16$ bytes. The highlighted factors 4 and 2 reflect the changes due to vectorization. LC for scalar and vectorized code are shown in Table 5. It can be seen that this kind of vectorization makes the layer conditions more stringent. However, compared to the traditional inner-loop vectorization approach it does not imply redundant L1-to-register loads and/or shuffle operations.
Figure 21 shows the LC effect by changing the lattice size $L_x$ on a single core, keeping the extent of the other dimensions constant. For $L_x = 4$ the L2 cache satisfies $LC_z$. As $L_x$ increases, the L2 cache violates the $LC_z$ condition (see the linear dependence between $LC_z$ and $L_x$ in Table 5).

Multicore layer conditions

The basic LC principle applied to serial code also holds for multicore. However, care should be taken when the cache $i$ under consideration is a shared cache. In this case, the per-core cache size $s_i$ and possible sharing of data between cores has to be taken into account. The first aspect is easily integrated into LC by dividing the size $S_i$ of the shared cache by the number of active cores $n$, i.e., $s_i = S_i/n$. Proper handling of data sharing among cores requires knowledge of the loop-scheduling technique and the lattice dimensions. For the DW kernel, thread parallelization is done via default OpenMP static scheduling along the outermost loop over the collapsed 4d space-time dimensions (see Listing 4). Thus in most cases there is no data sharing among the cores. However, the data traffic can be reduced by sharing of elements of the stencil array $I$. This is the case, e.g., when the lattice dimensions are chosen to be a small multiple of the number of cores that share the same cache. Figure 20 illustrates data sharing between cores. In the outermost direction $t$ two cores share a stencil element. These sharing effects have to be taken into account when adapting the LC to the multicore environment.

Figure 21b shows the influence of the number of cores on the LC due to the shared L2 cache. The lattice size is $24^4 \times 8$, i.e., a local (virtual) partition has a size of $24 \times 24 \times 12 \times 12$ in the 4d space-time dimensions. Using only a single core, the L2 satisfies $LC_y$. As the number of cores increases, the available cache per core decreases. At five cores, $LC_y$ is violated for L2, and only $LC_x$ is satisfied. This explains the increase in the traffic between main memory and L2. At six cores, the traffic decreases due to sharing of the data between cores as the local outermost dimension (12) is a small multiple of six and a condition similar to Fig. 20 applies. For seven to eleven cores there is no more sharing and the traffic stays at the level corresponding to $LC_x$. At twelve cores it decreases again due to sharing. Note that the model (shown with dotted lines) suffers some loss in accuracy especially at the boundaries of LC transitions. This is due to the assumptions made in the model, i.e., infinite cache associativity with LRU and perfectly synchronized “lockstep” execution across cores.

6.3.2 Initial optimizations

Before diving into ECM performance predictions we first look into initial optimizations based on the LC and the insights gained from the microarchitecture analysis (see Sec. 3.1).

Prefetching

Figures 22a and 22b compare the measured L2 and main memory traffic of the vectorized serial code with the LC predictions (shown as dashed lines). For the baseline implementation the memory traffic is in line with the prediction. However, the measured
L2 traffic exceeds the prediction by about 2×. A closer inspection reveals that the increase in traffic is due to the hardware prefetchers not moving the correct elements into the cache. The DW kernel has a complex access pattern, which repeats only after all the elements in the innermost loop were accessed, i.e., after the computation of one site. This requires access to 2.88 kB of data for scalar code and about 11.5 kB for vectorized code. It is extremely difficult if not impossible for the prefetchers to correctly predict the next elements.

The deficiencies of the hardware prefetching mechanics can be overcome by software prefetching. This decreases the L2 traffic, which is now within 30% of the prediction (see Fig. 22a). The single-core performance improves by a factor of 1.3× for both GCC and FCC as seen in Fig. 22c. For the following discussions we assume that software prefetching is applied.

**Instruction order**

In Sec. 3.1 we showed that the out-of-order window of the A64FX is small and suffers from inefficiencies in instruction reordering. Therefore the compiler has to support the hardware in hiding instruction latencies by proper instruction ordering. For the DW kernel implementation guidance is given to the compiler at the level of the source code (by explicit reuse of variables and ordering of operations). However, we noticed that GCC rearranges the intended order of instructions in a manner that deteriorates performance and also introduces unnecessary register spills. In order to mitigate these undesired effects we apply optimization flag -O1 instead of -Ofast. This keeps the intended order of instructions intact and also minimizes spilling. The performance improves by 1.3× as can be seen in Fig. 22c. FCC -O1 and -Ofast arrange the instructions as intended and performance is comparable to GCC -O1.

**6.3.3 ECM-model prediction for interleaved RIRI layout**

Using the LC we can estimate the data traffic $V_i$ and derive $T_i$ using Eq. (2). Along with the in-core contributions $T_{c,OL}$, $T_{L1,LD}$ and $T_{L1,ST}$ obtained using the OSACA tool, we can assemble the contributions using the overlap hypothesis (see Sec. 4.2) to finally determine the expected performance.

For a lattice size of $24^4 \times 8$ we can see from Table 5 that the A64FX satisfies $LC_i$ in the L1 cache, which means $V_{L2} = 2064 \text{byte/LUP}$, out of which 1872 byte/LUP is due to loading data from L2 to L1 and 192 byte/LUP is due to storing data from L1 to L2. The L2 load throughput is 64 byte/cy and the store throughput is 32 byte/cy (see Table 1), which results in $T_{L2} = (1872/64+192/32) \text{cy/LUP} = 35.25 \text{cy/LUP}$. The $T_{Mem}$ contribution can be derived in a similar fashion. All contributions are summarized in Table 6. They can be combined with the overlap hypothesis (d) in Fig. 6 to finally arrive at the ECM prediction.
TABLE 6 ECM contributions in cy/LUP to the DW kernel implementations for lattice size $24^4 \times 8$. We used the -O1 compiler flag.

| Implementation | $T_{c\_OL}$ | $T_{L1\_LD}$ | $T_{L1\_ST}$ | $T_{Mem}$ | $T_{ECM}$ | $T_{c\_OL}$ | $T_{L1\_LD}$ | $T_{L1\_ST}$ | $T_{L2}$ | $T_{Mem}$ | $T_{ECM}$ |
|----------------|-------------|--------------|--------------|-----------|-----------|-------------|--------------|--------------|-----------|-----------|-----------|
| RIRI-prefetch  | 168.0       | 25.6         | 3            | 35.3      | 15.9      | 168.0       | 33           | 3            | 35.3      | 15.9      | 168.0     |
| RRII-prefetch  | 70.8        | 34.4         | 20.4         | 35.3      | 15.9      | 70.8        | 45.2         | 37.3         | 35.3      | 15.9      | 85.5      |

(a) Strong scaling performance.

(b) Memory traffic.

FIGURE 23 Scaling performance and main-memory traffic of the RIRI and RRII implementations as a function of the number of active cores (GCC option -O1). The lattice size is $24^4 \times 8$.

$T_{ECM}$: Irrespective of the compiler we find

$$T_{ECM} = \max (168, f(25.6, 3, 35.3, 15.9)) \text{ cy/LUP} = 168 \text{ cy/LUP}. \quad (9)$$

The $T_{ECM}$ runtime corresponds to a single-core performance of 17.3 Gflop/s. However, we see from Fig. 22c that the measured single-core performance falls short of the prediction by 20% and only attains about 13.6 Gflop/s. The deviation from the ECM model can be expected on the A64FX. The model assumes that the out-of-order execution overlaps multiple loop iterations and hides all latencies. However, as the DW kernel takes almost 170 cy per LUP it is not possible for the out-of-order logic to sufficiently overlap the iterations (see Sec. 3.1). On a single CMG we would thus attain a performance of $12 \cdot 13.6 = 163.2$ Gflop/s, which is the measured throughput shown in Fig. 22c. The corresponding throughput attained by the code on a single CMG is $163.2 \cdot V_{Mem}/1320 = 184$ Gbyte/s, which does not saturate the CMG memory bandwidth of 227 Gbyte/s (see Table 1).

In order to achieve saturation we have to improve the single-core performance by at least 15%, which warrants a closer look at the current bottleneck. As can be seen in Table 6, the bottleneck of the RIRI implementation is the in-core overlapping part $T_{c\_OL}$. OSACA reveals that this is predominantly due to high occupation of floating-point ports on the A64FX caused by the high cost of SVE instructions for complex arithmetics (fcmla and fcadd). These instructions block the floating-point ports for three and two cycles, respectively. Furthermore, the fcmla instruction is imbalanced between the FLA and FLB ports; two out of the three cycles are scheduled to the FLA port. OSACA indicates that FLB has a 35% lower occupancy than FLA. One option to mitigate the pipeline imbalance is to avoid the SVE complex instructions and to use ordinary floating-point instructions instead.

In this case the cost would only be two cycles for a complex FMA and one cycle for a complex ADD operation. We discuss the implementation of this option in the next subsection.

6.3.4 Split RRII layout

Balanced pipeline usage is achieved by a change of the data layout. Instead of using the interleaved RIRI layout, we switch to the split RRII layout. In the case of 512-bit wide registers and in double precision we store eight real parts in memory, followed by eight imaginary parts (see Fig. 17b). Vectorized code operates on eight sites in parallel instead of four sites as in the RIRI layout (see Fig. 19). This has to be factored into the LC analysis. The necessary modifications to the layer conditions are shown
in Table 5 \[ d = 2 \] \( (d = 1 \) for the RIRI layout\). This leads to tighter conditions and LC breaking earlier when scaling up the number of cores. This is shown in Fig. 23a where LC breaks earlier with RRII than with RIRI.

The implementation of the RIRI layout guides the compiler to efficiently use the 32 floating-point vector registers without spilling. However, for the RRII layout the number of registers is insufficient and spilling of intermediate results occurs. This is reflected in the L1-to-register contributions \( T_{L1, LD} \) and \( T_{L1, ST} \) shown in Table 6. GCC minimizes register spills when using \(-O1\). FCC produces almost 2x more spills than GCC, resulting in lower performance (see Fig. 22c). We therefore exclude FCC from further analysis.

The RRII implementation still outperforms RIRI despite the register spills. This is because the overlapping in-core time \( T_{c, OL} \), which is the bottleneck of the RIRI layout, reduces by more than a factor of two (see GCC in Table 6). The lower cost of ordinary (non-complex) floating-point instructions and the balanced pipeline usage are the main reasons for this reduction. Still, the single-core performance falls short of the model prediction by at least a factor of 2. We speculate that this gap is caused partly by in-core inefficiencies rooted in the dependencies between loads and stores [4, Sec. 7.5], which are not taken into account in the model. This can be corroborated by the fact that for GCC with fewer spills the model deviates by a factor of 2.3x, while for FCC the deviation is 3.1x. Beyond the dependencies between loads and stores, the inefficient OoO execution also contributes to this deviation. To test the actual limit of the in-core execution for the code we constructed a benchmark with the same instruction dependency chain as the GCC code and measured the runtime while keeping all the data in the L1 cache. This yielded 113 cy/LUP, which is 1.6x higher than the in-core prediction seen in Table 6.

Using GCC, the RRII implementation already saturates the main-memory bandwidth using eight cores (see Fig. 23a). The sudden increase in performance when using 12 cores is due to sharing of the data in L2 among cores (discussed in Sec. 6.3.1). It correlates with a drop in main-memory traffic as seen in Fig. 23b. We also observe a decrease in main-memory traffic for the RIRI implementation, but it is not accompanied by an increase in performance because this version cannot saturate the memory bandwidth.

On one CMG the RRII implementation achieves 182 Gflop/s, which corresponds to a memory bandwidth of almost 205 Gbyte/s. On the full chip (four CMGs) we attain 712 Gflop/s, which is a 12% improvement over RIRI.

6.4 Energy consumption and tuning knobs

Figure 24 shows the performance and energy consumption applying the power knobs described in Sec. 5.6 to the DW kernel. For the highest performance setting \( (eco = 0 \) and \( f = 2.2 \) GHz) we see that the energy consumption of the RIRI implementation is almost 20% higher than for RRII. Furthermore, the energy consumption of RRII can be reduced further without significant loss in performance by lowering the clock frequency and switching on eco mode. However, for RIRI the performance drops drastically when eco mode is activated since here the bottleneck is the FLA pipeline (see Sec. 6.3.3). Eco mode turns off the FLB pipeline, which increases the load on FLA and hence the runtime. Regardless of the implementation, the power consumption of the DW kernel is about 205 W at the highest power and frequency settings. It reduces to about 145 W with \( eco = 2 \) and \( f = 2.0 \) GHz.

6.5 Comparison with other architectures

In this section we briefly compare the DW kernel performance among the A64FX, an Intel Cascade Lake CPU (CLX-AP) and a V100 GPU. Figure 25 shows this comparison for various lattice sizes. The size of the lattice is varied only along the innermost dimension \( x \). The experiments on the V100 were conducted using the Grid Lattice QCD framework. We used our own implementations [24] on the other architectures. For CLX-AP and V100 we used the RIRI layout. This layout performs best on CLX-AP. For the V100 this is the only layout currently available in Grid. The results are qualitatively similar to that of the SpMV performance comparison shown in Sec. 5.7 as both kernels are bandwidth bound. For smaller lattice sizes the CLX-AP has the advantage of large caches, while for larger lattice sizes both the A64FX and V100 have a \( 1.5 \)× performance advantage due to the higher memory bandwidth. The A64FX has a slight performance advantage over the V100, however, we did not do a detailed inspection and analysis of the V100 code to see if there are any optimization opportunities.

6.6 Further optimization options

The LC analysis suggests further optimization opportunities. For example, cache blocking minimizes LC violations and facilitates data reuse in the caches. Thread scheduling techniques increase data sharing between cores. Zero fill instructions could be used to
FIGURE 24 Comparison of performance and energy consumption of DW kernel implementations for different power and frequency settings on a full chip of Fugaku. The lattice size is $24^4 \times 8$. The energy consumption of the RIRI implementation is almost 20% higher than RRII. The energy consumption of RRII can be reduced without significant loss in performance by lowering the clock frequency and switching on eco mode.

FIGURE 25 Performance comparison of the DW kernel on Fugaku, Intel Cascade Lake AP and NVIDIA V100 for various lattice sizes with $L_z = 8$.

reduce the data traffic by avoiding write-allocate transfers. Another potential improvement is to first cut the inner dimensions ($s$ and $x$) for vectorization rather than the current approach of cutting outermost dimensions. This will further relax the LC. However, these optimizations involve architecture-specific tuning parameters and code paths and thus impact code maintainability.

We have not yet investigated the use of single precision, which is often sufficient depending on the algorithm in which the kernel is embedded. This will be the subject of future work.
7 | CONCLUSIONS

7.1 | Summary and outlook

We have further improved the ECM machine model for the A64FX CPU introduced in [1] and showed its applicability to the Fugaku processor. We validated the model with simple streaming kernels and could observe a high accuracy for in-memory data sets. The memory hierarchy is partially overlapping, allowing for a substantial single-core memory bandwidth with optimized code. Long floating-point instruction latencies and limited out-of-order execution capabilities were identified as the main culprits of poor performance and lack of bandwidth saturation. Vector intrinsics and manual unrolling are often required to achieve high performance.

Further, we applied the ECM model to sparse matrix-vector multiplication to identify the impact of A64FX proprietary performance features like the sector cache and power-related tuning knobs. The SELL-C-$\sigma$ matrix storage was shown to achieve performance and memory-bandwidth saturation superior to the standard CRS format. A comparison with state-of-the-art CPU and GPU architectures showed that for large, memory-bound SpMV datasets, the A64FX can outperform Intel’s CLX-AP by a factor of two and is on par with NVIDIA’s V100.

Finally, we used the ECM model for a comprehensive analysis of the Lattice QCD domain wall kernel in a subset of the Grid framework. We showed that both compilers used for this work (FCC and GCC) exhibit a lack of quality in code optimization. A change of the data layout can achieve a better balance of the port pressure and thus increase the performance significantly. When comparing the energy consumption of data layouts, the split RRII data layout proved to be almost 20% more energy efficient without a noticeable loss in performance. The A64FX shows a speedup of 1.5× over the CLX-AP for problem sizes exceeding both architectures’ last-level cache and comparable performance to a V100.

The present work opens up many interesting opportunities for future research. For example, load-balancing issues together with the ccNUMA characteristics of the A64FX warrant further investigation. The insight gained from the SpMV analysis can be applied to applications such as Chebyshev filter diagonalization or linear solvers. Further optimizations to the QCD kernels have already been discussed in Sec. 6.6. Last but not least a more detailed analysis of the mechanisms for power tuning is of great interest to all applications.

7.2 | Related work

Since the A64FX CPU is a very recent design, the amount of performance-centric research is limited. Dongarra [30] reported on basic architectural features, HPC benchmarks (HPL, HPGC, HPL-AI) and the software environment of the Fugaku system. Poenaru and McIntosh-Smith [31] presented results on the effect of using wide vector registers and compared the performance and cache behavior of the A64FX for HPC benchmarks to the ThunderX2 platform. Both Odajima et al. [32] and Jackson et al. [23] investigated benchmarks, full applications and proxy apps in comparison to Intel and other Arm-based systems but did not use performance models for analysis. Gupta et al. [34] and Brank et al. [35] investigated stencil codes, proxy applications, SpMV and memory-bound fluid solvers on several Arm-based platforms including A64FX but did not provide detailed and validated performance models. Heybrock et al. [36] and Jôô et al. [26] analyzed data traffic properties and data layout options for QCD kernels on the Intel Xeon Phi architecture. Kodama et al. [37] studied a comprehensive set of power-tuning knobs for STREAM and DGEMM kernels on Fugaku.

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DISCLAIMER

The results obtained on the evaluation environment in the trial phase do not guarantee the performance, power and other attributes of the supercomputer Fugaku at the start of its public use operation.

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