Probing the Field-Effect Transistor with Monolayer MoS$_2$ Prepared by APCVD

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Abstract: The two-dimensional materials can be used as the channel material of transistor, which can further decrease the size of transistor. In this paper, the molybdenum disulfide (MoS$_2$) is grown on the SiO$_2$/Si substrate by atmospheric pressure chemical vapor deposition (APCVD), and the MoS$_2$ is systematically characterized by the high-resolution optical microscopy, Raman spectroscopy, photoluminescence spectroscopy, and the field emission scanning electron microscopy, which can confirm that the MoS$_2$ is a monolayer. Then, the monolayer MoS$_2$ is selected as the channel material to complete the fabrication process of the back-gate field effect transistor (FET). Finally, the electrical characteristics of the monolayer MoS$_2$-based FET are tested to obtain the electrical performance. The switching ratio is $10^3$, the field effect mobility is about 0.86 cm$^2$/Vs, the saturation current is $2.75 \times 10^{-7}$ A/µm, and the lowest gate leakage current is $10^{-12}$ A. Besides, the monolayer MoS$_2$ can form the ohmic contact with the Ti/Au metal electrode. Therefore, the electrical performances of monolayer MoS$_2$-based FET are relatively poor, which requires the further optimization of the monolayer MoS$_2$ growth process. Meanwhile, it can provide the guidance for the application of monolayer MoS$_2$-based FETs in the future low-power optoelectronic integrated circuits.

Keywords: monolayer MoS$_2$; FET; mobility; Raman spectrum; photoluminescence (PL) spectrum

1. Introduction

The field effect transistors (FETs) are the basic unit of very large scale integrated circuits [1,2]. The feature size of the transistor has reached the physical limit with the integration of integrated circuits increases. Therefore, it is necessary to find the suitable semiconductor materials to improve the electrical performance of transistor [3,4]. Many researchers have focused on the two-dimensional materials with the single layer of atomic thickness [5]. The two-dimensional material is used as the channel material compared to the traditional bulk material, which can not only help to suppress the short channel effect, but also effectively reduces the static leakage current [6,7]. In addition, the two-dimensional materials also have the higher specific surface area, excellent mechanical strength, higher optical transparency, and various excellent photoelectric characteristics, so it can be widely used in the gas sensors [8], flexible electronics [9], and photodetectors [10]. Compared to the Si material, there are no dangling bonds in the low-dimensional transition metal sulfur compound materials when the transistor size is at the zoom limit [11]. The molybdenum disulfide (MoS$_2$) has the semiconductor characteristics, excellent physical and chemical properties, and unique microstructure, which can directly construct the field effect transistor. Therefore, the MoS$_2$ has become the very promising channel material in the process of the transistor scale.

As we all know, the thickness of the MoS$_2$ sample obtained by the mechanical peeling is larger, and the MoS$_2$ sample is smaller and irregular, so the MoS$_2$ is grown on the SiO$_2$/Si substrate by the...
atmospheric pressure chemical vapor deposition (APCVD) [12]. There are many factors that affect the continuity and uniformity of the MoS₂ deposition while using the APCVD method to obtain the MoS₂, such as the growth temperature, growth time, the amount of S powder and MoO₃ powder, and the gas flow rate. The band gap of MoS₂ changes with the number of layers, the bulk MoS₂ has the moderate electron mobility and an indirect band gap of 1.29 eV, whereas the monolayer MoS₂ is a direct bandgap material with a band gap of 1.8 eV. The MoS₂ is a promising material for the flexible and transparent substrates, which can be applied in the logic circuits and optoelectronic devices [13]. The size and quality of MoS₂ have a great influence on the performance of the device. Therefore, we can improve the continuity and uniformity of the MoS₂ deposition by adjusting the growth process parameters and treating the SiO₂/Si substrate with the graphene quantum dot solution [14]. The FETs with the direct bandgap monolayer MoS₂ have the larger switching ratio and the lower off-state current. However, the mobility and on-state current of the FETs are very lower, so it is very meaningful to optimize and enhance the electrical performance, which can provide the application reference of the monolayer MoS₂-based FETs.

The paper is composed of five parts: First, the large-area high-quality monolayer MoS₂ is prepared by the APCVD to facilitate the fabrication of FETs [15]. Then, the monolayer MoS₂ is confirmed and characterized by the high resolution microscopy, Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy. Next, the main preparation process of monolayer MoS₂-based FET is described. Subsequently, the electrical performance of the back-gate FET is measured. Finally, the conclusion of this paper is summarized. The following are the electrical performance parameters of the prepared monolayer MoS₂-based FET in this paper, the electrical performance parameters have increased by improving the electrode contact and channel material [16]. The switching ratio is as high as 10⁷, the field effect mobility is about 0.86 cm²/Vs, the saturation current is 2.75 × 10⁻⁷ A/μm, and the lowest gate leakage current is 10⁻¹² A. Besides, the monolayer MoS₂ can form the ohmic contact with the Ti/Au electrode. Although the electrical performance of monolayer MoS₂-based FETs is not ideal, we have mastered the fabrication process of monolayer MoS₂-based FETs, and the growth process of monolayer MoS₂ needs further optimization, which can provide the reference for the preparation of high quality monolayer MoS₂-based FETs [17].

2. The Growth and Characterization of Monolayer MoS₂

2.1. The Growth Process of Monolayer MoS₂

In this paper, the monolayer MoS₂ on SiO₂/Si substrate was grown by APCVD. First, the solid sulfur powder and MoO₃ powder could be melted into the gas state under the high temperature. Then the argon gas with a purity of 99.999% was passed as the carrier gas, and the sulfur gas was transferred to the vicinity of the SiO₂/Si substrate. At the same time, there was a certain concentration of MoO₃ vapor in the vicinity of the SiO₂/Si substrate. Finally, the sulfur gas could react with MoO₃ gas on the surface of the SiO₂/Si substrate to form the MoS₂. The specific growth experiment process of monolayer MoS₂ was as follows: The SiO₂/Si substrate was selected as the growth substrate of MoS₂, wherein 300 nm SiO₂ was the back gate dielectric layer of FET [18]. Before the growth experiment of MoS₂, the 1 cm × 1 cm SiO₂/Si substrate was first subjected to the oxygen plasma treatment. The vacuum tube furnace of the MoS₂ growth experiment was TF55035C-1, and the front end is equipped with a heater that could be heated to 400 °C, which could help to assist the evaporation of sulfur powder. First, the quartz boat with 100 ± 5 mg sulfur powder (Alfa Aesar, Shanghai, China, 99.5%) was placed in the middle zone of the heater. Then, the quartz boat with 2 ± 0.1 mg MoO₃ powder (Alfa Aesar, Shanghai, China, 99.95%) and SiO₂/Si substrate was placed in the middle of the tube furnace. Next, the argon gas with 200 sccm was introduced into the tube furnace for 10 min to eliminate the air of the tube furnace. Subsequently, the temperature of the sulfur powder was heated to 200 °C, and the MoO₃ powder was heated to 750 °C. During the growth of MoS₂, the argon gas with a flow rate of 40 sccm was continuously provided and the growth temperature was maintained for
Finally, the growth reaction of MoS$_2$ was completed, and the MoS$_2$ sample was taken out while the temperature of the tube furnace was cooled to room temperature.

2.2. The Test Characterization Conditions of Monolayer MoS$_2$

The MoS$_2$ sample could be obtained by the APCVD. At the same time, the MoS$_2$ could be systematically characterized by optical microscopy, Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy to further determine the layer number and quality of the MoS$_2$ sample. The Raman model was LabRam HR Evolution with a laser wavelength of 532 nm (HORIBA JobinYvon, Paris, France) [20]. The specific test conditions of the Raman spectrometer were the 100× objective lens, 1800 groove/mm grating, the spot size of 532 nm laser was 342 nm, and the incident laser power density was 140 µW/µm$^2$. Besides, the field emission scanning electron microscopy (FESEM, JSM-6700F, Hitachi, Tokyo, Japan) was also used at the accelerating voltage of 5 kV.

The monolayer MoS$_2$ and the SiO$_2$ of SiO$_2$/Si substrate could interfere with the light, so there was a reflection enhancement effect on the visible light wavelength of 532 nm. Figure 1a,b respectively show the 50× and 100× objective optical micrograph of monolayer MoS$_2$, the pink and blue patches in the optical images respectively represents the monolayer MoS$_2$ on SiO$_2$/Si substrate and the scale, it could be observed by the optical microscope that monolayer MoS$_2$ on SiO$_2$/Si substrate exhibited the bright blue color. As shown in Figure 1c, the typical FESEM image of monolayer MoS$_2$ clearly exhibited the quasi-equilateral triangles, which was consistent with the crystal structure. Besides, the Raman mapping was tested to observe the film formation quality and uniformity of the triangular MoS$_2$. It can be seen from the Figure 1d that the color of MoS$_2$ mapping was relatively uniform, which could indicate that the sample was the high-quality uniform monolayer MoS$_2$.

There were two characteristic peaks in the Raman spectrum of MoS$_2$, the layer number of MoS$_2$ sample could be measured by the Raman spectrum between the E$_{12g}$ mode and the A$_{1g}$ mode. It could be found by observing Figure 2a that the distance $\Delta k$ between the E$_{12g}$ characteristic peak and A$_{1g}$ mode. It could be found by observing Figure 2a that the distance $\Delta k$ between the E$_{12g}$ characteristic peak and A$_{1g}$ characteristic peak was 18 ± 0.1 cm$^{-1}$, and the ratio of A$_{1g}$/E$_{12g}$ was about 1.043, which indicates that the MoS$_2$ sample was a monolayer [21]. Figure 2b shows the photoluminescence spectrum of the
monolayer MoS$_2$ sample at different points. The photoluminescence spectrum of monolayer MoS$_2$ on SiO$_2$/Si substrate had I and B exciton peaks, the strongest I exciton peak position of monolayer MoS$_2$ was at $684.6 \pm 0.5$ nm, which could be explained by the direct exciton excitation [22]. The corresponding electron volt was at $1.82 \pm 0.02$ eV through the conversion relationship between wavelength and electron volts, which was consistent with the direct band gap width of monolayer MoS$_2$. In addition, there was also the B exciton peak at $1.97 \pm 0.02$ eV due to the 3d orbital electron interaction of Mo atoms, which could further prove that the sample was the large-area high-quality monolayer MoS$_2$.

**Figure 2.** (a) The Raman spectrum of monolayer MoS$_2$ at the different test points; (b) the PL spectrum of monolayer MoS$_2$ at the different test points; (c) the Power Raman spectrum of monolayer MoS$_2$; and (d) the Power PL spectrum of monolayer MoS$_2$.

In Figure 2c, the Raman spectrum intensity of monolayer MoS$_2$ increased with the laser power increase. There was a blue shift of the E$_{12g}$ characteristic peak when the laser power increased, and the A$_{1g}$ characteristic peak position did not change. This was because the MoS$_2$ on the SiO$_2$/Si substrate was an n-type doped semiconductor material [23]. Figure 2d shows the power photoluminescence spectrum of monolayer MoS$_2$. The peak intensity of the photoluminescence spectrum increased when the laser power increased. At the same time, the relative positions between the I exciton peak and B exciton peak were red-shifted to some extent when the laser power increased. The reason was that the MoS$_2$ on SiO$_2$/Si substrate was the n-type doped material [24]. It is known from the above Raman spectrum and photoluminescence spectrum that the MoS$_2$ sample was a monolayer.

3. The Discussion of Electrical Performance Results

The field effect transistor is the most basic electronic component in the digital logic circuits, which consists of the channel, a source electrode, a drain electrode, and the gate dielectric layer [25]. It can control the channel internal carrier density and the source-drain current by adjusting the gate voltage, which can achieve the current amplification and power amplification.

3.1. The Fabrication Process of Monolayer MoS$_2$-Based FET

The monolayer MoS$_2$-based back-gate FET can be fabricated by the photolithography, electron beam evaporation, and lift-off micromachining processes, the above steps used the polymethyl methacrylate (PMMA) resist process. The following is the specific process flow schematic diagram of monolayer MoS$_2$-based FET [26]. First, the high-quality triangular monolayer MoS$_2$ is grown on the surface of Si/SiO$_2$ substrate by APCVD, as shown in Figure 3a; in Figure 3b, the pre-baking, gluing,
exposing, and developing processes were performed to complete the photolithography, then using the photoresist as a mask, and the Ar plasma etching process was performed to remove the exposed MoS\textsubscript{2} film, the photoresist was removed by the acetone solution, the ethanol solution was cleaned to determine the source and drain windows of monolayer MoS\textsubscript{2}-based FET; Subsequently, the 20 nm Ni/70 nm Au were used as the source-drain metal contact by the electron beam evaporation, as shown in Figure 3c; Next, the photoresist was dissolved in the acetone solution, and the metal solution was removed by the ethanol solution, as shown in Figure 3d.

![Figure 3](image)

**Figure 3.** The main preparation process schematic diagram of the monolayer MoS\textsubscript{2}-based field effect transistor (FET; (a)) the growth process of the high-quality triangular monolayer MoS\textsubscript{2}; (b) the photolithography and the Ar plasma etching process; (c) the electron beam evaporation process; and (d) the cleaning process of the photoresist.

Finally, the device was annealed in the vacuum environment of 180 °C for 2 h to remove the photoresist residue and decrease the contact resistance between the Ti/Au metal and monolayer MoS\textsubscript{2}. The fabrication of monolayer MoS\textsubscript{2}-based FET was completed, and the electrical performance of monolayer MoS\textsubscript{2}-based FET was analyzed and tested by the multi-function probe station and the B1500A semiconductor parameter analyzer (Santa Clara, CA, USA).

Figure 4a–c respectively show the 10×, 50×, and 100× objective optical microscope images of the monolayer MoS\textsubscript{2}-based back-gate FET, and the pink and blue patches in the optical images respectively represents the monolayer MoS\textsubscript{2} on SiO\textsubscript{2}/Si substrate and the scale, it can be found that the area of monolayer MoS\textsubscript{2} was usually 10–30 \(\mu\)m, and the size of the triangular monolayer MoS\textsubscript{2} was relatively smaller compared to the metal electrodes, so the source and drain metal electrodes were divided into an electrode lead and the pad. The electrode lead (line width of 5 \(\mu\)m) was directly in contact with monolayer MoS\textsubscript{2}, and the pad of the source and drain metal electrodes was a square of 100 \(\mu\)m × 100 \(\mu\)m, which was for the electrical performance tests on the multi-function probe station [27]. The FESEM image of the monolayer MoS\textsubscript{2}-based back-gate FET is given in Figure 4d, it can be seen that the uneven brightness and blurred focus appeared on the surface of monolayer MoS\textsubscript{2}, which was affected by the charging effect of the SiO\textsubscript{2}/Si substrate during the FESEM scanning.
Figure 4. (a) The 10× objective optical microscope image; (b) the 50× objective optical microscope image; (c) the 100× objective optical microscope image of the monolayer MoS$_2$-based back-gate FET; and (d) the FESEM image of the monolayer MoS$_2$-based back-gate FET.

3.2. The Electrical Properties of Monolayer MoS$_2$-Based FET

Figure 5 shows the electrical test structure schematic diagram of the monolayer MoS$_2$-based back-gate FET. The gate oxide of the back gate electrode was 300 nm SiO$_2$, and monolayer MoS$_2$ was used as the conductive channel material. To decrease the contact resistance, the source/drain metal electrodes were made of 20 nm Ti/70 nm Au. The 20 nm Ti metal acted as the adhesion layer between monolayer MoS$_2$ and the Au, which could prevent the Au metal falling off from the MoS$_2$ film [28]. Besides, the Ti metal could also facilitate the formation of the ohmic contact between the monolayer MoS$_2$ sample and the Au electrode.

Figure 5. The electrical test structure of the monolayer MoS$_2$-based back-gate FET.

The transfer and output characteristics of monolayer MoS$_2$-based back-gate FET are shown in Figure 6. It can be seen by observing Figure 6a that the on-state current of the FET increased with the source–drain voltage increase. When the source–drain voltage was 0.9 V, the on-state current was about $2.75 \times 10^{-7}$ A/µm, which was far from the application requirement of the high-performance FET [29]. In Figure 6b, the gate voltage could effectively regulate the channel resistance and the source-drain current, which exhibited the better switching characteristics. The source–drain current decreased when the back-gate electrode was at the negative voltage, whereas the source–drain current increased when a forward voltage was applied to the back-gate electrode, so the monolayer MoS$_2$-based FET was the $n$-type transmission, and the switching ratio could reach $10^3$. The reason was that monolayer
MoS$_2$ had the smaller grain size and the relatively poor quality, which had a major effect on the device performance.

**Figure 6.** The monolayer MoS$_2$-based back-gate FET. (a) The $I_{ds}$–$V_{bg}$ transfer curve; (b) the $I_{ds}$–$V_{bg}$ transfer curve with the ordinate semi-logarithmic coordinate; (c) the $I_{ds}$–$V_{ds}$ output curve; and (d) the hysteresis loop of MoS$_2$ FET under different $V_{ds}$.

Based on the $I_{ds}$–$V_{gs}$ transfer curve, the field effect mobility can be calculated by using the following equation [30]:

$$\mu = \frac{dI_{ds}}{dV_{gs}} \frac{L}{W(\varepsilon_0 \varepsilon_r / d)V_{ds}}$$  \hspace{1cm} (1)

The channel length of device $L = 10 \mu$m, the channel width of device $W = 10 \mu$m, the source and drain voltage $V_{ds} = 0.9$ V, vacuum dielectric constant $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, the relative dielectric constant of SiO$_2$ $\varepsilon_r = 3.9$, the thickness of SiO$_2$ $d = 300$ nm, $dI_{ds}/dV_{gs}$ is the slope of the transfer curve. Therefore, when the $V_{ds}$ is 0.9 V, the field effect mobility is approximately $0.86 \pm 0.05$ cm$^2$/Vs according to the slope of the linear region between 40 V and 100 V. This is because the lattice structure of MoS$_2$ grown by APCVD is not complete. There are the lattice defects, which can deteriorate the mobility of monolayer MoS$_2$-based FET. Due to the large forbidden band width of monolayer MoS$_2$, the lowest gate leakage current of MoS$_2$ FET is at the $10^{-12}$ A when the gate voltage gradually increase from −100 to 100 V, so it is suitable for the low-power logic circuits. The lower gate leakage current can effectively decrease the leakage power, which can help to improve the lifetime of the device [31]. As shown in Figure 6c, the output curve of monolayer MoS$_2$ FET was linear, the gate voltage could well control the output current, and the output current increased with the gate voltage increase, which indicates that the monolayer MoS$_2$-based FET was an $n$-type carrier transmission. For the monolayer MoS$_2$-based back-gate FET, the current was proportional to $V_{ds}$ in the linear regime at the small source-drain voltage, and the $I_{ds}$–$V_{ds}$ curve of FET device exhibited the odd function characteristic with the good linearity and central symmetry when the $V_{ds}$ increased from −2 to 2 V. Moreover, the $V_{gs}$ had a significant regulation effect on the slope of the output curve, which indicates that the monolayer MoS$_2$-based back gate FET could form the good ohmic contact between the Ti/Au metal and MoS$_2$ channels. It can be found from Figure 6d that the transfer characteristic curve had the obvious hysteresis phenomenon. This is due to the fact that the channel material used monolayer MoS$_2$, which was very sensitive to the environmental change [32]. The monolayer MoS$_2$-based FET could absorb the moisture and impurity gases from the air, which would have the important impact on the electrical performance of the monolayer MoS$_2$-based FET.
4. Conclusions

In this paper, the monolayer MoS$_2$ on SiO$_2$/Si substrate was grown by APCVD, and the MoS$_2$ sample was characterized by the high resolution microscope, the Raman spectroscopy, photoluminescence spectroscopy, and field emission scanning electron microscopy, which could prove the existence of monolayer MoS$_2$. In order to evaluate the quality of monolayer MoS$_2$ systematically, the monolayer MoS$_2$ was used as the channel material of the FET, and the back gate FET was fabricated on the monolayer MoS$_2$. It could be found from the electrical parameters of FET that the ohmic contact could be formed between monolayer MoS$_2$ and Ti/Au metal electrode, the gate leakage current and static power consumption were lower. At the same time, the on-state current was about $2.75 \times 10^{-7}$ A/µm when the source-drain voltage was 0.9 V, both the switching ratio and the mobility increased to some extent, which still need further improvement. The growth process of MoS$_2$ was optimized to obtain the higher quality monolayer MoS$_2$, so that the monolayer MoS$_2$-based FET could be applied to the future low-power optoelectronic integrated circuits.

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