A Design of fast-setting on-chip Charge Pump Circuit

Yannan ZHAI1,a, Ling Gao1, Jingquan Li, Qangli Qiu1

1Aviation University Air Force, 130022 Changchun Jilin China

Abstract: A circuit of fast-setting charge pump on-chip is designed based on the Dickson circuit. The charge pump circuit, which is improved, increases the initial node voltage. With the consideration of the current mismatch, the accurate clock of the duty circle below 50% is proposed. The HSPICE simulation result indicates that the settling time from 0V to 20V only needs 51.650μs for the charge pump, and it is faster than the traditional Dickson charge pump 26.03μs. In summary, the settling time of the output voltage of the charge pump is prominently decreased and the performance of the charge pump is obviously improved.

1. Introduction

With the rapid development of integrated circuits, the requirements of various devices for power supply are also increasing. As an internal power supply, on-chip charge pump is also widely used. It is used in the fields that need high voltage, such as serial communication circuit, EEPROM, dynamic random access memory and so on. In EEPROM, the charge pump is used to write or erase the suspended gate device. If the charge pump pumping speed is slow, EEPROM cannot realize high-speed data rewriting, and the data may be lost and mistransmitted, affecting the device performance. Therefore, reducing the voltage rise time has become the focus of the design of on-chip charge pump.

Now most charge pumps are based on Dickson charge pump circuit [1], which uses charge to accumulate in capacitance to produce high voltage. When the capacitor is charged and discharged, the current mismatch leads to the low voltage of the first stage of the charge pump, which will seriously affect the boost speed of the charge pump. Therefore, starting with the study of reducing the initial voltage of the charge pump, a 16 stage Dickson charge pump boost circuit is designed in this paper. The circuit improves the traditional Dickson charge pump and is driven by a clock signal with a duty cycle of less than 50% to achieve the purpose of fast boost.

2. Dickson charge pump analysis

Fig. 1 is a circuit of Dickson charge pump and its clock signal. In Fig. 1, the input signal of the charge pump is the power supply voltage VDD, Vout is the output voltage, φ and φ/ is a two-phase non-overlapping clock signal. In microelectronic technology, the diode is difficult to manufacture, so the gate drain short circuited NMOS tube is used instead of the diode.
2.1 static analysis

The operation process of Dickson charge pump is the process of charging and discharging the capacitor with the help of the driving signal with opposite polarity. It continuously pushes the power supply and the charge of the previous stage into the next stage, so that the potential of the latter stage is higher than that of the previous stage, so as to obtain high voltage at the last stage. Clock phase \(\phi\). At low level, diode D1 is turned on and \(V_{\text{IN}}\) charges \(C_1\) until the voltage of node 1 becomes \(V_{\text{IN}} - V_d\). When \(\phi\) jumps to \(V_{\phi}\), the voltage of node 1 becomes \(V_{\text{IN}} + (V_{\phi} - V_d)\), causing diode D2 to turn on and charge \(C_2\) until the voltage of node 2 becomes \(V_{\text{IN}} + (V_{\phi} - V_d) - V_d\). When \(\phi\) becomes low level once again, and the voltage of node 2 jumps to \(V_{\text{IN}} + 2(V_{\phi} - V_d)\). In this way, the charge is transferred from the left to the right. Due to the unidirectional conductivity of the diode, the charge cannot return from the right to the left. With the increase of the number of charge pump stages, the charge is continuously transferred from the power supply to the output, so as to obtain the required high voltage. After stage \(n\), the output voltage is:

\[
V_{\text{out}} = V_{\text{IN}} + N \cdot (V_{\phi} - V_d) - V_d
\]  

(1)

2.2 dynamic analysis

However, when Dickson charge pump is working, there is a loss of charge in the process of transfer, and the output voltage is not constant. The Dickson charge pump is dynamically analyzed \[29-31\], and the output voltage value of each clock cycle is obtained:

\[
V_{\text{out}}(j) = (N+1)V_g - NV_g \beta^j
\]

(2)

\[
\beta = \frac{1}{1 + \frac{C}{NC_{\text{load}}}}
\]

(3)

If the rise time of the output voltage \(V_{\text{out}}(j)\) from \(V_G\) to \(V_{PP}\) is represented by \(T_r\), \(T_r\) satisfies \(V_{\text{out}}(T_r) = V_{PP}\). So \(T_r\) can be expressed as:

\[
T_r = \ln \left[ 1 - (V_{PP} - V_g) / NV_g \right] / \ln \beta
\]

(4)

Where \(n\) is the number of stages of the charge pump and \(V_G\) is the maximum voltage gain of each stage. Since equation (4) is represented by the number of cycles of the clock, in practice, equation (4) should be multiplied by the cycle of the driving clock. If used \(\alpha\) representing the influence of the body
effect on the transmission transistor, it can be deduced that the boost time of the output voltage rising from VG to VPP is:

\[
T_r = \ln \left[ 1 - \left( V_{pp} - V_g \right) \left\{ \sum_{i=1}^{N+1} \alpha^i - 1 \right\} V_g \right] / \ln \beta
\]  

(5)

According to the above analysis and equation (2), equation (4), equation (5) and equation (5), whether the Dickson charge pump connected with diode or the Dickson charge pump connected with MOS tube, the rise time of their output voltage is related to the power supply voltage, transmission tube threshold voltage, charge pump stage, coupling capacitance, load capacitance. The period of the driving clock and the initial voltage of the node are closely related.

Therefore, reasonable setting of power supply voltage, transmission tube threshold voltage, charge pump stage, coupling capacitance, load capacitance and other parameters is very important to reduce the voltage rise time. Designing a high-performance clock generation circuit to output a clock signal with high frequency will also reduce the voltage rise time. The initial voltage of the node is very low during the initial boost cycles of the charge pump. Only by increasing the initial voltage of the node and reducing the number of clock cycles required for voltage rise can the voltage rise time be reduced.

In this paper, the above factors are considered in order to reduce the boost time. According to the previous theoretical analysis of Dickson charge pump, the initial voltage of the node has a great impact on the voltage rise time. According to equation (2), without considering the volume effect, the voltage of each node can reach the following ideal value only when the number of clock cycles is large:

\[
V_{out}(\infty) = (N + 1)V_g
\]  

(6)

In the first clock cycle, i.e. \( J = 1 \), the voltage \( V_{out}(1) \) at each node can only reach

\[
V_{out}(1) = (N + 1)V_g - NV_g \beta
\]  

(7)

It can be seen that the voltage of each node needs a certain clock cycle to reach the theoretical value. If the initial voltage value of each node is increased, the voltage rise time can be significantly reduced.

3. circuit design

3.1 improved charge pump model

NMOS precharge tube [2-12] is added to each stage of MOS charge pump to precharge the voltage of each node to a certain value, which can reduce the time when the node voltage reaches the theoretical value. However, the circuit with precharge tube also has some defects, that is, it increases the area of the circuit too much.

Simulation results show that adding an even number of precharges can improve the boost speed. In this paper, the 16 stage MOS Dickson charge pump is simulated by adding different even number of precharges, and the effect of the number of precharges on the boost time is studied. The voltage rise time of each charge pump from 0V to 20V is shown in table 1.

Table 1 The relationship between the number of precharging FET and rise time

| Number of precharge tubes | Rise time(μm) | Number of precharge tubes | Rise time(μm) |
|--------------------------|---------------|--------------------------|---------------|
| 0                        | 77.680        | 10                       | 67.402        |
| 2                        | 73.610        | 12                       | 66.643        |
| 4                        | 70.346        | 14                       | 65.905        |
| 6                        | 69.472        | 16                       | 65.385        |
| 8                        | 68.514        |                          |               |
Therefore, this paper improves the Dickson charge pump and proposes a charge pump model that only adds a precharge tube in the first four stages of the circuit, which not only improves the boost speed, but also saves the circuit area. The improved Dickson charge pump model is shown in Figure 4-20

When the input signal Vin is high, the precharge tube is turned on and the node voltage is charged to a certain value. The working principle of the charge pump core is exactly the same as that of the traditional Dickson charge pump.

3.2 improve the drive clock signal

The traditional Dickson charge pump uses a two-phase non overlapping clock driving signal with a duty cycle equal to 50%. Each time the signal changes, the charging current and discharge current of the capacitor turn on at the same time, which will undoubtedly cause adverse factors such as charge leakage and charge discharge current mismatch.

Therefore, this paper proposes to use a clock signal with a duty cycle equal to 30% as the drive of the charge pump, as shown in Fig. 3.

3 Simulation Analysis

0.35 is adopted in this paper μ M CMOS process model, the designed charge pump circuit is simulated with HSPICE software. The simulation environment is set as follows: the simulation temperature is 25 ℃, the power supply voltage is 5V , and the simulation time is 700 μ s.

Firstly, the Dickson charge pump shown in Fig. 1 is simulated to obtain the clock signal φ and φ/ Is a non overlapping clock with a duty cycle of 50%. The simulation results are shown in Figure 4. The figure (a) shows the initial waveform of the simulation, VA is the voltage of the first node of the charge pump, VB is the voltage of the second node of the charge pump, and VH is the output voltage of the charge pump. The figure (b) shows the complete waveform of the simulation. The figure (c) shows the amplified waveform of VH.

As can be seen from figure (a), in the first clock cycle (J = 1), the clock φ Is high level, VA (1) = 5.640v, VB (1) = 3.710v.

As can be seen from figure (b), when φ and φ/ At low level, the charge pump is turned off, and VH
and VA are 5V; When φ and φ/ When it is a two-phase non overlapping clock, the charge pump is turned on, VA and VB oscillate and rise, and the output voltage VH also rises gradually.

As can be seen from figure (c), VH is at 65 μ When VH rises to 20V, the boost speed is very slow and almost stable. From the reading, VH is 142.680 μ W when it reaches 20V at s, it takes 77.680 for VH to boost from 0V to 20V μ s.

The optimized Dickson charge pump shown in Figure 2 is simulated, and the clock signal φ and φ/ The duty cycle is 30%. The simulation results are shown in Figure 5. The figure (a) shows the initial waveform of the simulation. VA is the voltage of the first node of the charge pump, VB is the voltage of the second node of the charge pump, and VH is the output voltage of the charge pump. The figure (b) shows the amplified waveform of VH.

As can be seen from figure (a), in the first clock cycle (J = 1), the clock φ Is high level, VA (1) = 6.74v, VB (1) = 4.58v. Compared with the traditional charge pump shown in Fig. 4 (a), the initial voltage is about 1V higher. It can be seen that the introduction of precharge tube on the basis of traditional circuit can improve the initial voltage.
As can be seen from figure (b), VH is at 65 μ When VH rises to 20V, it almost reaches stability. From the reading, VH is 116.650 μ When it reaches 20V at s, it takes 51.650 for VH to boost from 0V to 20V μ s. From 5V to 20V, the improved charge pump boosts 26.03 faster than the traditional charge pump μ s. It can be seen that the charge pump circuit can speed up the boost speed by using the clock signal with a duty cycle of 30%.

![Simulation waveform of improved charge pump](image)

4. conclusion
A stable charge pump boost circuit structure applied to EEPROM is designed. The circuit uses a stable reference voltage to drive the oscillation circuit to produce an accurate clock with a duty cycle less than 50%, which greatly improves the boost speed of the charge pump; A precharge tube structure is added to the first two stages of the charge pump core, which further improves the boost speed of the charge pump; The combination of charge pump and voltage regulating circuit stabilizes the output voltage and reduces it to the required value. Under the working voltage of 5V, it only takes 56.256 for the charge pump to boost to the high voltage of 15.962v μ s. And can achieve stable high-voltage output. The simulation results show that the charge pump has fast boost speed and high reliability, and can provide stable voltage for EEPROM reading, writing and erasing.

Reference
[1] Dickson J F. On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique [J]. IEEE J Sol Sta Circ, 1976;11(3) : 374-378.
[2] Jong-shin Shin, In Yong Chung , Young June Park, etal. A new charge pump without degradation in threshold voltage due to body effect [J] . IEEE J Solid State Circuits, 2000; 35 (8): 1 227-1 230.
[3] RICHARD J F, SAVARIA Y. High Voltage Charge Pump Using Standard CMOS Technology [J]. IEEE Regular Session G: High Voltage Techniques & Continuous Time Filtering, 2004: 317-320.

[4] Mantooth H A, Duliere J L. A Unified Diode Model for Circuit Simulation [J]. IEEE Trans. on Power Electronics, 1997, 12(5): 816-823.

[5] Shin Jongshin, CHUNG In-Young, Young June Park, Hong Shick Min. A New Charge Pump without Degradation in Threshold Voltage Due to Body Effect [J]. IEEE Journal of Solid-State Circuits, 2000, 35(8): 1227-1230.

[6] JOHAN S Witters, GUIDO Groeseneken. Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits [J]. IEEE Journal of Solid-State Circuits, 1989, 24(5): 1372-1380.

[7] MARTINE J Silva. A Switched Capacitor Double Voltage Generator [J]. IEEE Proc. Mid-West Symp. Circuits and Systems, 1994, 1: 177-180.

[8] FAVRAT P. High-Efficiency CMOS Voltage Doubler [J]. IEEE Journal of Solid-State Circuits, 1998, 33(3): 410-416.

[9] TORU Tanzawa, TOMOHARU Tanaka. A Dynamic Analysis of the Dickson Charge Pump Circuit [J]. IEEE Journal of Solid-State Circuits, 1997, 32(8): 1231-1240.

[10] ZHANG Ming, LLASER Nicolas. Dynamic Analysis of Dickson Charge Pump Circuits with a Resistive Load [J]. IEEE ICECS, 2003: 431-434.

[11] Zhu Y, Sang X, Kim YH. Analysis and Design of an Exponential Charge Pump. Advanced Materials Research, 2021, vol 753-755, 1483-1488.

[12] Ngueya WS, Mellier Julien, Ricard Stephane. Ultra Low Power Charge Pump with Multi-Step Charging and Charge Sharing. IEEE International Memory Workshop, 2016.