Message passing in fault tolerant quantum error correction

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Inspired by Knill’s scheme for message passing error detection, here we develop a scheme for message passing error correction for the nine-qubit Bacon-Shor code. We show that for two levels of concatenated error correction, where classical information obtained at the first level is used to help interpret the syndrome at the second level, our scheme will correct all cases with four physical errors. This results in a reduction of the logical failure rate relative to conventional error correction by a factor proportional to the reciprocal of the physical error rate.

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I. INTRODUCTION

The effort to design and build a quantum computer is motivated by the discovery of a number of quantum algorithms that are more efficient than their best known classical equivalents [1,2,3,4]. Some practical benefit could arise from these algorithms with a quantum computer of only tens or hundreds of qubits, but a quantum computer with thousands of logical qubits will be required to outperform the most powerful classical computers [5]. To mitigate the effects of decoherence and systematic imprecision it is expected that fault tolerant error correction [6,7,8] will be required at the expense of additional quantum resources. Motivated by the fact that a limited amount of resources can be allocated to error correction, here we present a new method for error correction which uses message passing to achieve lower error rates than conventional methods that incur the same resource cost.

With the notable exceptions of topological quantum computing [9] and the surface code [10,11], most methods for error correction involve concatenation. Our result is in this context and so we briefly review this approach.

First, information represented by the state of a single physical qubit is encoded in the states of several physical qubits, which together form the logical qubit of an error correction code. Using error correction circuitry constructed from physical operations (including state preparation, measurement, and quantum logic gates such as Hadamard and controlled-NOT) some number of errors affecting the data qubits that make up the logical qubit can be detected and corrected. Typically this is done by interacting the data qubits with some ancillary qubits and then measuring the ancillary qubits to extract a syndrome from which errors are diagnosed. Then, to form a concatenated quantum code, this process is applied recursively - that is, logical qubits are used to encode higher level logical qubits and logical operations are used to construct higher level error correction circuits.

It is known that by concatenating a quantum code, an arbitrarily accurate and arbitrarily large quantum computation can be performed efficiently with faulty components provided that the failure rate of all physical operations is below some threshold [8,12]. With each level of concatenation the failure rate of the logical operations reduces double-exponentially, however both the number of physical qubits to encode each logical qubit and the time required to perform each logical operation increase exponentially. This increase in resources makes it impractical to use more than just a few levels of concatenation.

Conventional implementations of quantum error correction implicitly assume that errors are equally likely on all data qubits and so the correction is always to apply the fewest possible bit or phase flips required to return the state to the code space. Error correction at each level of concatenation operates independently in this way. However, not only does error correction reduce the probability of a logical error, it also gives some indication of the likelihood that an error has occurred at a higher level of encoding - a logical error is more likely to have occurred if a correction was applied during error correction than if a correction was not applied. If this classical information is passed from lower levels of error correction to higher levels it is possible to correct a larger set of errors. Message passing in quantum computation was first considered in the context of an error detection code, where errors at the level below would become located errors at the next level up and thus be corrected [13]. The idea was also applied to an error correction code in the context of communication across a noisy channel [14].

Here we extend this idea by applying message passing to fault tolerant error correction under the nine-qubit Bacon-Shor subsystem code [13,16]. In particular we present a method for error correction at the second level of concatenation which uses both the regular syndrome and messages from the first level of concatenation. We refer to this method as message passing error correction (MPEC). Using simulations we find that MPEC will correct all cases with four physical errors, whereas conventional error correction can only guarantee success with up to three physical errors. We also show that MPEC retains fault tolerance and so for physical error rates well below the threshold the use of this method can lead to...

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In this paper we focus entirely on improving the performance of the second level of concatenated error correction using the $[[9,1,3]]$ Bacon-Shor code. The Bacon-Shor error correction circuits we use are shown in Fig. II.15.

In the $[[9,1,3]]$ code a logical failure can occur if at least two of the data qubits have errors. When the error correction circuit measures a non-zero syndrome we know that at least one of the data qubits has an error and that any additional error may cause failure. To have a logical error and observe no syndrome requires at least three physical errors. Therefore logical errors are of order $1/p^2$ more likely at logical circuit locations which measured non-zero syndrome. At these level-1 locations, which have detected an error at the physical level, we raise a flag to indicate an increased probability of level-1 error. These flags are simply classical information that can be tracked through the quantum circuit.

Bit (X) and phase (Z) errors can be treated independently. There will be $X$ flags and $Z$ flags each indicating increased probability of the respective errors. Since the X and Z error correction circuits are similar the same rules apply independently to both X and Z correction. Table II shows the four possible outcomes of a level-1 error correction block.

Using conventional concatenation each level of error correction works independently. The $n^{th}$ level of error correction can correct any single gate failure at the level below. All gates in the error correction circuit are assumed to be equally likely to fail, and so when a non-trivial error syndrome is measured the lowest possible number of errors is assumed and the corresponding correction is applied. Information about the syndrome and the corrections applied is then thrown away. In our method we use this same information to estimate the relative probability of gate failures at a higher level. The key ideas are that more errors can be corrected if the locations of the errors are known and that logical failure is more likely when a non-trivial correction is applied. That is, there is a significant correlation between flags and logical failure.

Codeword states with two errors share the same set of syndromes as codeword states with single errors. However, with the additional flag information, is it possible to distinguish between a larger set of errors. We call the combined information of the flags and the measured syndrome the super syndrome. At the second level of error correction, the syndrome of a single FF may be indistinguishable from that of two FFs, and so without message passing, four physical errors (if they result in two FFs) can cause a logical error at level 2. When the full super syndrome is considered one FF is distinguishable from two FFs and so we can attempt to correct two level-1 errors at once. Cases with two FFs can be accurately diagnosed and corrected. $UF+2FS$ may share the same super syndrome with two $FF$, but $UF+2FS$ is weight 5 in terms of the physical error rate. It turns out that all weight 4 cases can be corrected using MPEC.

When the error correction circuitry itself is made from

![FIG. 1: a) The nine data qubits of the Bacon-Shor code can be thought of as the vertices of a 3x3 grid. b) X syndrome extraction circuit. The qubit labels indicate that this circuit performs the same operations on each row of data qubits in parallel. Z syndrome extraction has a similar circuit (CNOT gates are reversed and measurement and preparation are in the conjugate basis) which operates on the columns of data qubits.](image-url)
FIG. 2: Physical errors during a level-1 two-qubit gate can result in many different combinations of flags and failures on the two logical qubits depending on where the errors occur. In this example there are two physical errors, one of the errors affects both level-1 qubits and the other error only affects the bottom level-1 qubit. Both of the trailing EC boxes will see a non-zero syndrome and so each will raise its flag. In this case the final result will be flagged success on the top qubit and a flagged failure on the bottom qubit. In general, each physical error can affect one or both logical qubits. Any combination of $US, FS, FF$ and $UF$ is possible as long as the error weight one each logical qubit is not more than the number of physical errors.

Noisy gates the problem is significantly more complicated. The error correction circuits are designed to be fault tolerant - a fault at any given physical location will not spread to multiple data qubits in the same logical qubit. However, this type of fault tolerance does not guarantee the protection of the properties that make message passing assisted error correction superior. For example, consider an encoded level-1 CNOT that is part of a level-2 error correction circuit. A single physical error during this CNOT could result in a flag being raised on one or both of the qubits depending on the location of the error. Two physical errors could result in $US + FF, US + FS, FS + FS, FF + FF, etc.$ (Fig. 2). With three physical errors, all combinations of flags and failures are possible. Therefore not all two $FF$ cases are weight 4 for example. This effect complicates the process of interpreting the super syndrome and ensuring fault tolerance. We found that not all fault tolerant circuits for conventional error correction can be readily adapted to MPEC.

To provide the best possible error correction, we aim to apply a correction corresponding to the most likely cause of the super syndrome. We assume a low physical error rate, and so the most likely cause is the one with the fewest physical errors.

Here is an overview of how our scheme works: The error correction circuit used is shown in Fig. 1. X and Z error correction are treated separately. There are X flags and Z flags, which represent potential X and Z errors respectively. A flag is raised on a level-1 qubit whenever lower level error correction measures a non-zero syndrome. Each flag has its own identity. The propagation of each flag is tracked through the circuit as if it were an actual error, spreading through CNOT gates. X flags copy downwards through CNOT gates and Z flags copy upwards. When the second level syndrome is measured we look for combinations of one, two, or three flags on the ancilla which if corresponded to actual errors would produce the syndrome that was measured. Such a combination is called a flag match. (For examples of this see figures in Appendix A.) If a flag match is found, we apply corrections to the data qubits that share the same flags as used in the flag match. Some super syndromes have more than one flag match, in these cases we preference the match which implies the fewest errors and results in the fewest corrections to the data qubits. If no flag match is found, we fall back to the default error correction action; i.e. we correct based on the syndrome alone. After error correction, all flags found on the ancillary qubits at the point of measurement are cleared from the data qubits - these flags have either been established to be $FF$ (and have been corrected) or $FS$, so they are of no further use.

Note that although $3FS + UF$ has equal weight to $3FF$, triple flag matches must still be preferred over the default correction to avoid particular cases in which four physical errors would otherwise cause level-2 failure due to certain combinations of 2-qubit gate failures. (See Appendix A.)

Further levels of concatenated error correction will compound the benefits of MPEC. However, making use of message passing at all levels is not so easy. Finding a flag scheme that works at all levels is non-trivial, and so for this paper we have focused on just two levels of error correction. A simple method for concatenation beyond level 2 is to alternate between error correction that provides flags for the next level, and error correction that uses flags from the previous level but provides no flags. For this alternating sequence the number of physical errors required for logical failure at increasing levels of concatenation is $1, 2, 5, 10, 25, 50, 125; in contrast with the regular scaling, 1, 2, 4, 8, 16, 32, 64$, for the same physical resources.

III. FAULT TOLERANCE

The procedure described in the previous section ensures that no combination of four physical errors will result in a level-2 logical error. This is an improvement over conventional concatenation which can only guarantee the correction of three physical errors at level-2. However, to show that our scheme is effective for large circuits we must show that an arbitrary length chain of level-2 locations will not fail for any combination of four physical errors in each level-2 extended rectangle. An extended rectangle is defined to be an encoded gate with error correction before and after $S$.

Usually, fault tolerance of error correction circuits is considered from the point of view that all levels act independently. The basic rule is that a single error should not spread to multiple errors on the same data qubit. For MPEC the fault tolerant condition is more complicated. Since corrections are based on the entire super syndrome
we must take into account the error weight of each of the possibilities in Table I rather than just counting the failures.

To ensure fault tolerance, an MPEC box must satisfy the following condition:

\[ a + b \leq 4 \Rightarrow c \leq b \]  

(1)

where \( a \) is the error weight of the state entering the MPEC box, \( b \) is the weight of errors occurring inside the box, and \( c \) is the error weight of the state leaving the box after any corrections have been applied. Error weights are calculated according to Table I. Evidence that the MPEC scheme satisfies the condition can be found in Appendix A. A proof that this condition guarantees the performance of the error correction can be found in Appendix B.

IV. SIMULATION

To test our message passing error correction we simulate a level-2 CNOT extended rectangle. We compare the failure rates with and without message passing. The failure rate of this circuit is meant to approximate the failure rate of the level-2 CNOT which might be an algorithmic location.

To simulate the error correction circuit we need only simulate the propagation of errors that occur during the circuit [19]. This avoids having to store the complete state of the computer which we assume is an arbitrary codeword state perturbed by the errors. The circuit is deemed to fail if a readout of the data qubits at the end of the circuit in either the \( X \) or \( Z \) basis would not produce the correct output. Equivalently, a circuit is defined to have succeeded if an errorless error correction cycle applied to its output state would produce the correct state.

For \( p > 4 \times 10^{-5} \) we perform many simulations of the entire two level circuit with a fixed error rate and tally the failures. At each physical circuit location we apply an error with probability \( p \). For all single qubit locations (preparation, measurement, memory) the error is a randomly selected single qubit Pauli error, \( X, Y, \) or \( Z \). For two-qubit locations (CNOT) the error is a randomly selected two-qubit Pauli error (\( X \otimes I, X \otimes X, X \otimes Y, \) etc.) Errors at all locations are independent.

For error rates below \( 4 \times 10^{-5} \) the number of trials required to generate sufficiently accurate statistics directly is too large; so we use an alternative approach. Instead of giving each circuit location some probability of error, we simulate the circuit with exactly \( i \) errors placed randomly. This is repeated many times for \( i = [4, 12] \) to generate the probability \( r_i \) that the circuit fails given that there were \( i \) errors. These conditional probabilities can be combined to give the failure rate of the circuit as a function of \( p \),

\[ p(2) = \sum_{i=0}^{N} r_i \binom{N}{i} p^i (1-p)^{N-i}, \]  

(2)

where \( N \) is the number of locations in the entire circuit, 72657.

To ensure randomness over the large number of trials required we use the SIMD-oriented Mersenne Twister pseudo random number generator [20]. The results of the simulations are in Fig. 3. Note that Eq. 2 is truncated after \( i = 12 \) after which \( r_i \) is set to equal zero. This is why the curves drop to zero at higher error rates. A second set of lines connect the direct data points taken above \( p = 4 \times 10^{-5} \).

Our simulations indicate that all combinations of four errors are corrected by MPEC. This is in contrast to standard error correction which fails for some four error combinations. For values of \( p \) close to the threshold, \( p_{th} \), the failure rate is not significantly reduced, but for \( p < p_{th} \) the failure rate is reduced by a factor of

\[ \frac{p_{std}(2)}{p_{mp}(2)} \approx \frac{r_{5}^{std}}{r_{5}^{mp}} \frac{5}{Np} \approx 10^{-4} \frac{p}{p}. \]  

(3)

The superscripts indicate standard error correction and message passing error correction.

V. CONCLUSIONS AND FURTHER WORK

In the region of interest - for physical error rates where two or three levels of error correction is sufficient for logical computation - MPEC is significantly better than standard quantum error correction. We emphasize that this benefit is achieved only at the cost of additional classical processing. For more than two levels of error correction the benefit can be compounded, but the problem
of finding an optimal and general flagging scheme (one that can be applied at all levels) is an open question and the subject of further work. Also of interest is that the complexity of correctly interpreting the super syndrome appears to depend on the circuits that are used to extract the syndrome. Can MPEC work fault tolerantly for other codes such as the Steane code \[7\] and if so is it compatible with the most compact Steane circuits \[21\]?

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APPENDIX A

The primary purpose of this section is to demonstrate that the circuits and rules described in Section II satisfy the fault tolerance condition, Eq. 1. In doing so we also give examples of flag propagation and flag matching which could be useful for a general understanding of the MPEC scheme.

\begin{equation}
\text{CNOT.}X_{\text{ctrl}} \psi = X_{\text{ctrl}} \cdot X_{\text{targ}} \cdot \text{CNOT} \psi
\end{equation}

\begin{equation}
\text{CNOT.}Z_{\text{ctrl}} \psi = Z_{\text{ctrl}} \cdot \text{CNOT} \psi
\end{equation}

\begin{equation}
\text{CNOT.}Z_{\text{targ}} \psi = Z_{\text{targ}} \cdot \text{CNOT} \psi
\end{equation}

Flags represent potential errors and so they are propagated in the same way that the errors are. Each flag that is raised is given a unique identity, but they can be copied to multiple qubits by CNOT gates in the same way that errors are. For the diagrams in this section the flags are distinguishable by their patterns.

A set of flags is said to match the syndrome if identifying these flags as errors can exactly describe the measured syndrome. When testing for a flag match, each ancillary qubit has its flags added in binary, flags that
are not part of the set to be tested are ignored, if the result of all the ancillary qubits is identical to the syndrome then the set of flags is a match.

The figures shown in this section depict the propagation of flags and errors on the second level of error correction. It is implicit that at every circuit location there is a lower level of error correction being performed which can raise flags. These flags are indicated by the flags drawn on the circuits. Crosses indicate a level-1 error (or correction at the end of the circuit). The propagation of the errors is shown using bold lines. At the end of the circuit, the figures show the values of the syndrome measurements and the flags that have propagated onto the ancilla. The flags used in a flag match are highlighted and corrections are shown by crosses at the end of the circuit.

The flags and crosses result from physical errors during the lower level error correction. The error weights of these locations can be inferred from Table I. Errors during the CNOT gates can result in flags and errors on both qubits (Fig. 2). In these cases the number of physical errors during the CNOT limit the error weight of each logical qubit.

To demonstrate that Eq. 1 is satisfied (ie. that the error weight of the output from an EC box is no greater than the number of errors occurring inside the box) we reason on a case by case basis with cases grouped according to the weight of the incoming errors.

1. Failures cases, $a+b \geq 5$

To understand how MPEC succeeds on a case by case basis, it is instructive to first examine the typical failure cases.

Fig. 4 shows how a single $FS$ can cause failure by masking the flags of two $FF$s. For this failure to occur, the two $FF$s and the $FS$ must each affect different qubit lines (rows for $Z$ errors, columns for $X$ errors).

Fig. 5 shows that a pair of $FS$s can match the syndrome of a $UF$ and thus cause the wrong correction to be applied. Again, each of the $FS$s and the $UF$ must affect different qubit lines. If there is a flag from an $FS$ that follows the same path as a $UF$, the combination of the $UF$ and the $FS$ is equivalent to an $FF$.

It is worth noting that no number of $FS$s alone can ever cause failure.

2. Cases with $a = 4, b = 0$

All incoming flags will be passed down to the ancillary qubits and hence, by the rules of MPEC, be cleared from the data after the syndrome measurement.

Any incoming $UF$ will be corrected by conventional error correction rules, as a single $FS$ is not enough to interfere.

Two incoming $FF$s is the exact case that MPEC was designed to deal with. The flags will match the syndrome and both errors will be corrected.

A single incoming $FF$ cannot be masked by one or two $FS$s. The two $FS$s can be positioned to make a two-flag match, but MPEC will always prefer to use the single flag match which is provided by the $FF$.

3. Cases with $a = 3, b \leq 1$

This time, we have the freedom to place a single $FS$ anywhere within the circuit. But this doesn’t affect any of arguments given for $a = 4$. An $FS$ cannot interfere with the correction of a single incoming $FF$ or $UF$ no matter where it is placed. One of the important properties of the EC circuit we have chosen is that no single $FS$ can mask an error to prevent its correction, because each incoming error on the data will affect two of the ancillary qubits. This property is not a feature of all (conventionally) fault tolerant circuits.
An FS on the data towards the end of the circuit will cause a the FS to be passed out of the EC box.

4. Cases with $a = 2, b \leq 2$

With the up to two errors within the circuit we now have the ability to make an FF, or even a pair of FFs at a CNOT.

In the worst case there is an incoming FF and a pair of FFs that arise from errors during a level-1 CNOT (Fig. 6); to successfully correct this we must use a triple flag match.

CNOT errors can that result in $FF + FS$ pairs in addition to an incoming FF (Fig. 7), but not in any configuration that will cause problems. The FS and FF from CNOT failure can be thought of as an effect on the same data qubit line. With this in mind it is clear that no situation like Fig. 4 can occur without extra errors.

An FF on the data towards the end of the circuit will be passed out of the EC box.

5. Cases with $a = 1, b \leq 3$

With $a = 1$ there must an incoming FS on one of the data qubits. Three physical errors inside the EC box is still only enough to cause failure at one location, but this time there may be a UF.

If flag from the FS matches the syndrome, this will result in successful correction. There can be a UF that produces a syndrome with no flag match. When there is no flag match MPEC falls back to the conventional Bacon-Shor error correction rules for this circuit. This will either result in a successful correction of the failure (if it occurs before or during the first set of CNOTs) or a parity mismatch on the syndrome and hence no correction. With $b = 3$ it is acceptable to let a UF or FF leave the EC box, eg. Fig. 8

6. Cases with $a = 0, b \leq 4$

With $b = 4$ there can either be two separate flagged failure locations, or one UF location and one FS location. As we have already seen, the UF cases are all work in the same way as they do for conventional error correction. The worst case is shown in Fig. 9 where two pairs of physical errors case two FF pairs. When this happens there will be a two flag match which will not correct all of the errors but will not cause logical failure. Since $b = 4$ it is acceptable for the EC box to let through a single UF or even two FFs.

With $b = 4$ there are still not enough errors to affect two data qubits with errors and have a flag on the third line (Fig. 4) or to have a UF on one data qubit that matches misleading flags on the other two qubit lines (Fig. 4).
FIG. 9: Two FF + FF pairs from CNOT failures result in a two-flag match which corrects only one of the errors on the data qubits. Since all flags that appear on the ancillary qubits are cleared after error correction there will be a UF leaving this EC box.

APPENDIX B

Having demonstrated in Appendix A that Eq. 1 is satisfied, in this section we aim to prove that improved failure rate scaling for MPEC extended rectangles found in Section IV carries over to arbitrary length logical computation. For simplicity we consider only identity gates at the logical level, but it is not hard to extend this proof to an arbitrary logical circuit given standard requirements of fault tolerant circuits, which are already satisfied by the Bacon-Shor code (eg. transversal gates).

The probability that a logical circuit will fail can be bounded by the probability that each level-2 extended rectangle in the circuit has at most four physical errors.

An error correction box is defined to have succeeded if an errorless error correction cycle applied to its output state would produce the correct state, i.e. if an EC box succeeded then any errors remaining on the output can be corrected. Let $a_n$ be the physical error weight of the input state to the $n$th EC box, and $b_n$ be the number of physical errors occurring inside the $n$th EC box. Let $S_n$ denote the success of the $n$th EC box. Then the success condition can be written as

$$(b_n+1 = 0 \Rightarrow a_{n+2} = 0) \Rightarrow S_n.$$  \hspace{1cm} (B1)

**Theorem B.1** *Given that there are no errors on the initial state and that all level-2 extended rectangles have at most four physical errors, all extended rectangles will succeed.*

**Proof** No initial errors:

$$a_0 = 0.$$  \hspace{1cm} (B2)

All extended rectangles have at most four errors, that is, the sum of the errors in any two adjacent EC boxes is no more than 4:

$$b_n + b_{n+1} \leq 4.$$  \hspace{1cm} (B3)

MPEC is fault tolerant, as described in Section III and demonstrated in Appendix A:

$$(a_n + b_n \leq 4) \Rightarrow (a_{n+1} \leq b_n).$$  \hspace{1cm} (B4)

The first extended rectangle will have no more than four errors and there are no errors in the initial state (Eq. B2 and Eq. B3), therefore

$$a_0 + b_0 \leq 4.$$  \hspace{1cm} (B5)

Suppose $a_n + b_n \leq 4$, then $a_{n+1} + b_{n+1} \leq b_n + b_{n+1}$ by the fault tolerance rule, Eq. B4 (with $b_{n+1}$ added to both sides). Therefore, using Eq. B3 we have

$$(a_n + b_n \leq 4) \Rightarrow (a_{n+1} + b_{n+1}) \leq 4.$$  \hspace{1cm} (B6)

With Eq. B5 and Eq. B6

$$a_n + b_n \leq 4$$ \hspace{1cm} (B7)

is true by induction. With Eq. B4 we then have

$$a_{n+1} < b_n$$ \hspace{1cm} (B8)

for all $n$. Therefore

$$(b_{n+1} = 0) \Rightarrow (a_{n+2} = 0),$$ \hspace{1cm} (B9)

which with Eq. B1 means success for all EC boxes. \(\square\)