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Low voltage adiabatic flip-flops based on power-gating CPAL circuits

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Abstract

This paper presents low voltage adiabatic flip-flops with power-gating techniques. The flip-flops are realized by CPAL (Complementary Pass-Transistor Adiabatic Logic) circuits with DTCMOS (Dual Threshold CMOS) techniques. The designs of adiabatic sequential circuits with power-gating techniques are described. Voltage scaling for power-gating adiabatic mode-8 counter is verified. All circuits are simulated using NCSU PDK 45nm technology by varying supply voltages. Based on the simulation results, the power-gating DTCMOS adiabatic flip-flops that operate on medium-voltage region can not only keep reasonable speed but also reduce greatly energy consumptions.

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1. Introduction

As portable device’s developing, power dissipation has become a critical concern in high performance applications. It is well known that power consumption is composed of three main components: short-circuit, leakage, and dynamic switching power dissipations [1]. Due to the continued scaling of the CMOS technology and threshold voltage, leakage dissipation has potentially become a dominant component of total power dissipations in nanometer CMOS circuits [2].

Adiabatic computing can effectely reduce dynamic dissipations by recycling the energy stored in the nodes of circuits. However, energy dissipation occurs even for constant input signals in adiabatic circuits, because their output nodes are always charged and discharged by power-clocks [3]. Moreover, as the continued scaling of the CMOS technology, leakage dissipations of adiabatic circuits have also become a dominant component of total power dissipations similar to conventional CMOS logic circuits. In order to reduce dynamic and leakage power, power-gating techniques for adiabatic circuits was proposed by

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shutting down the adiabatic units during idle states. Because clocking schemes and signal waveforms of adiabatic circuits are different from the conventional CMOS circuits. Power-gating switches and circuits for turning off power-clocks should be different. Several power-gating schemes for adiabatic circuits have been proposed [3, 4].

Voltage scaling is an effective method to reduce the power in static CMOS and the adiabatic circuits, because energy dissipation scales quadratically as supply voltage scales down. Scaling supply voltage to medium-voltage region is an attractive approach especially for mid performances (f =5MHz to 100MHz) [5]. Several near-threshold adiabatic circuits have been proposed recently. However, the previously reported near-threshold computing for adiabatic circuits are only used for basic adiabatic circuits without power-gating.

This work presents low voltage adiabatic flip-flops with power-gating techniques. The flip-flops are realized by CPAL (Complementary transmission door adiabatic logic) circuits with DTCMOS (Dual Threshold CMOS) techniques. The designs of adiabatic sequential circuits with power-gating techniques are described. A near-threshold power-gating adiabatic mode-8 counter with DTCMOS (Dual Threshold CMOS) techniques is verified. All circuits are simulated using NCSU PDK 45nm technology by varying supply voltages. Based on the simulation results, the power-gating adiabatic flip-flops that operate on medium-voltage region can not only keep reasonable speed but also reduce greatly energy consumptions.

2. Power-Gating CPAL Circuits with DTCMOS Techniques

The basic two-phase CPAL buffer/inverter is shown in Fig. 1 (a) [3]. It is mainly composed of two parts: logic function circuit that consists of four NMOS transistors (N5-N8) with complementary pass-transistor logic (CPL) function block, and the load drive circuit that consists of a pair of transmission gates (N1, P1 and N2, P2). The clamp transistors (N3 and N4) ensure stable operation by preventing from floating of output nodes. The simulated waveforms for the two-phase CPAL and its two-phase power clocks are also shown in Fig. 1 (a).

![Fig. 1. Basic and DTCMOS two-phase CPAL buffers](image-url)
The most straightforward application of the DTCMOS (Dual Threshold CMOS) techniques is simply to partition a logic cell into critical and non-critical regions, and then to only use fast low-$V_T$ devices in critical paths to meet performance goals. A DTCMOS CPAL buffer is in Fig. 1(b). The part enclosed with dotted lines is the non-critical region, and the rest is the critical region in the buffer. The two transistors (N3 and N4) use high-$V_T$ device to reduce their leakage currents.

The power-gating scheme for two-phase CPAL circuits is shown in Fig 2 [3]. The power-gating switches shown in Fig. 2(a) are inserted between power-clocks ($clk$) and virtual power-clock ($pc$). They are used to disconnect the adiabatic logic block from the power-clocks during idle periods. In active mode, the power-gating control signal ($Active$) is high, thus the virtual power-clocks ($clk_1$ and $clk_2$) follow the power-clock ($pc_1$ and $pc_2$). In sleep mode, $Active$ is low level, so that the power-gated adiabatic logic block is shut down. In the power-gating switches, the two transistors (N9 and N10) are added to make the un-driven node ($X$ or $Xb$) grounded, since the node $X$ or $Y$ would be light bootstrapped even if the output $pc$ or $pcb$ is low level because of large sizes of bootstrapped NMOS transistors (N1, N2) [3],

![Fig. 2: Two-phase CPAL power-gating switch and power-gating scheme](image)

3. Voltage Scaling for Power-Gating DTCMOS CPAL Circuits

Voltage scaling is an effective method to reduce the power in the adiabatic circuits. Taken as an example, a mode-8 adiabatic counter based on two-phase DTCMOS CPAL using the power-gating techniques is verified, as shown in Fig. 3. The circuit consists of the three $T$ flip-flops and combinational logic block (an OR/NOR gate). The Boolean expressions for $Q_0$, $Q_1$ and $Q_2$ are given by

$$Q_0^{new} = \overline{Q_0}, \quad T_0 = 1 \quad (1)$$
$$Q_1^{new} = \overline{Q_1} \cdot Q_0 + \overline{Q_1} \cdot \overline{Q_0}, \quad T_1 = Q_0 \quad (2)$$
$$Q_2^{new} = \overline{Q_2} \cdot (Q_1 \overline{Q_0}) + \overline{Q_2} \cdot (Q_1 \overline{Q_2}) \cdot Q_2, \quad T_2 = Q_1 Q_2 \quad (3)$$

For proper synchronizing, the middle signals from $T$ flip-flop are used as inputs to the combinational logic block (the OR/NOR gate). For the CPAL gates of the mode-8 counter and power-gating switches, all devices sizes in PMOS, and NMOS transistors are taken with $W/L= 18\lambda/2\lambda$ and $3\lambda/2\lambda$, respectively.
The simulated waveforms for the mode-8 counter based on two-phase DTCMOS CPAL with power-gating scheme are shown in Fig. 4 at 0.7V source voltage. Energy dissipations of the mode-8 counter based on two-phase CPAL at a normal source voltage (1.0V) are shown in Fig. 5.

Fig. 3. Mode-8 counter based on two-phase DTCMOS CPAL with power-gating scheme

Fig. 4. Simulated waveforms for the mode-8 counter based on two-phase DTCMOS CPAL with power-gating scheme

Fig. 5. Energy dissipations of the mode-8 counter based on two-phase CPAL at a normal source voltage
Fig. 5 (a) shows energy dissipation comparisons of the basic and DTCMOS two-phase CPAL mode-8 counters without power-gating scheme in different frequencies. Fig. 5 (b) shows energy dissipation comparisons of DTCMOS two-phase CPAL mode-8 counters with power-gating (activity = 0.5) and without power-gating scheme in different frequencies. The two-phase DTCMOS CPAL mode-8 counters with power-gating achieves considerable energy savings.

In order to investigate the performances of the flip-flops based on DTCMOS CPAL circuits with power-gating in near-threshold region, the mode-8 counters are simulated by source voltage ranging from 0.7V to 1.1V with 0.1V step based on 45nm NCSU PDK-1.3 technology, as shown in Fig. 6.

Fig. 6. Maximum operation frequencies and energy dissipations of the mode-8 counter based on two-phase DTCMOS CPAL with power-gating in different source voltages

4. Conclusions

Voltage scaling is an effective method to reduce the power in the adiabatic circuits. The power-gating DTCMOS adiabatic flip-flops that operate on medium-voltage region can not only keep reasonable speed but also reduce greatly energy consumptions.

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