Design and Performance of a Phase Angle Control Method Based on Digital Phase-locked Loop

Bin Yi*, Zhao Wei, Min Luo, Jinling Meng & Kai Deng

Electric Power Research Institute of Guangdong Power Grid Corporation, Guangzhou, Guangdong, China

Xin Lin
Guangzhou Yueneng Power Technology Development Co., Ltd., Guangzhou, Guangdong, China

ABSTRACT: Controlling of the phase angle of the output current or voltage of the resonant inverter is crucial for the proper operation of the power converters in the application of energy engineering. This paper proposed a novel phase angle control method based on digital phase-locked loop (DPLL). The new method features accurate phase control and flexible phase adjustment. Also we established a mathematical model of the DPLL based on the analysis of the operating characteristic of each module. Several experiments were also implemented to verify the effectiveness of the proposed phase angle control method in the end.

Keywords: phase angle; digital phase-locked loop; mathematical model; resonant inverter

1 INTRODUCTION

Series and/or parallel resonant inverters have been widely used in industrial applications like induction heating, high frequency alternating current power distribution system and medium frequency rotating magnetic system. This kind of resonant converter usually consists of a switching network and a resonant tank. The resonant tank designed for the harmonic filter also provides zero voltage switching conditions. The switching network converts the DC voltage to a quasi-square waveform. The phase angle of the output voltage of the switching network is manipulated by adjusting the driving pulses for the switching network.

For some special applications, controlling of phase angle of the output current or voltage of the resonant tank is crucial for the proper operation of the power converters. The authors of [2]-[4] introduced a new zone-control induction heating system (ZCIH). The ZCIH system consists of multiple split working coils and multiple inverter units. It has to control each phase angle of the current to be in phase to suppress circulating current among the inverter units. The phase controller presented in [2] detects the phase angle of each coil current and manipulates the phase angles of the voltage to adjust current phase angle to the internal reference phase angle. This method requires knowing the transient behaviour of the current phase angle to determine the control parameters in the phase angle controller. However, it is difficult to obtain the transient behaviour of the phase angle in some application conditions. The author of [2] proposed a decoupling control algorithm to overcome the mentioned disadvantage in [4]. But the control algorithm seems to be complex and the circuit parameters are needed in order to achieve a better control performance.

For the mentioned high frequency alternating current (HFAC) power distribution system (PDS) in [1], [5]-[6], the phase angle control of the output voltage is also very important. In general, the source side of HFAC PDS consists of several resonant inverters in parallel connection. It is required to simultaneously accomplish the synchronization of magnitude and the phase of the output voltage in each unit. In [5], the authors developed a new phase-shift modulation with which the phase angle of the output voltage of full-bridge resonant inverter is independent of the voltage magnitude modulation signal. However, because of the unavoidable discrepancy of load parameters of each power unit, the phase angles of the load impedance are different. The controller should be capable to adjust the phase of the output voltage inde-
pendently. The authors of [6] designed an independent phase-angle control loop consisting of a phase-angle detector, a phase controller, and a pulse-phase modulator. This offers a freedom of control of the phase-angle discrepancy among inverter modules in a multiple resonant inverters system. The author of [1] combined the methods in [5] and [6] and provided a novel phase-shift modulation, which integrated the regulations of phase and magnitude to achieve optimized synchronization and advanced current sharing control in the parallel single-stage resonant inverter. But the phase modulation signal is generated by multiplying the measured output voltage with the reference signal and filtering the ac term out. The controller is implemented based on discrete device.

According to above phase angle control scheme, the goal of the control is to make the phase of voltage or current keep in phase with a phase reference signal. This is quite similar to the function of a phase-locked loop, which is a simple yet effective tool that can synthesize a signal whose phase angle is locked to that of a given input signal ([7]). This paper will propose a phase angle control method based on a novel digital phase-locked loop (DPLL). The proposed method features accurate phase control and flexible phase adjustment. Modelling and analysis of the proposed DPLL is presented to guide the design of the parameters of the phase controller in order to obtain a better performance. Tests to validate the proposed phase angle control method are implemented in the end.

2 PROPOSED PHASE CONTROL SCHEME

Figure 1 presents a general block diagram for multiple series resonant converters system. The magnitude and phase angle of the output resonant current should be controlled to the reference signals of each unit respectively. The current phase control path is independent from the current magnitude control path. The phase controller in Figure 1 can be the type proposed in [2], or the one presented in [1]. By comparison, the former seems easier to implement digital control. A basic method to obtain the phase information of the output current is to detect the zero crossing points of the measured current signal and convert it into a binary signal (or square signal). If the setting phase reference signal is also a binary signal, the phase controller needs to make the phase signal of the actual output current keep in phase with the setting phase reference signal by manipulating the phase angle of the inverter output voltage. It is known that the resonant current lags or leads the output voltage of the inverter bridge with a constant angle when the switching frequency of the bridge is unchanged. In another word, the phase controller has to synthesize a signal whose phase angle is locked to that of the setting phase reference signal. Based on the synthesizing signal of the phase controller, the driving circuit can make the inverter output a voltage with a specific phase angle, which enables the resonant current to have a phase same with the setting phase reference signal. If the output signal of the phase controller has the same phase with the output voltage of the inverter bridge, the resonant branch is like a phase shift network.

Figure 1. A general block diagram for multiple series resonant converters.

Figure 2. Phase controller based on DPLL.

If we make use of phase-locked loop (PLL), another effective scheme for the design of the phase controller can be taken into consideration, which is shown in Figure 2. The proposed phase control scheme consists of two major parts, the DPLL and the switching network. The latter detects the amplitude and phase of the resonant output current, and chooses the appropriate phase feedback signal for the DPLL. When the magnitude of the current is bigger than that of the internal constant inside the comparator in Figure 2, the comparator controls the switching network to select the detected current phase as the phase feedback. Otherwise, the comparator enables the switching network to select DPLL’s output as the phase feedback. In our design, the DPLL’s output has the same phase with the H-bridge output voltage. The accuracy of the detected current phase declines when the magnitude of the current is very small by using the zero-crossing detecting technique. The switching network protects the controller from operating with an inaccurate phase feedback signal. For the voltage-source series-resonant inverter, the H-bridge output voltage has a constant phase relationship with the resonant current at a fixed working frequency. Therefore, the transition
of the phase feedback signal can be regarded as a phase jump at the switching moment.

The details of the proposed DPLL are shown in Figure 3. The clock \( f_s \) is determined by the system clock \( f_x \) and the clock divider. In Figure 3, JK edge-triggered flip-flop, which has a reference input and a feedback input, is the DPD. It is sensitive to the positive edges of its input signals. The output of the JK edge-triggered flip-flop is a Boolean high-low pulse, which represents the phase error between the two inputs of the DPD. The K modulus controller outputs the modulus K by evaluating the phase error between the two inputs of the DPD. The random walk filter is used to suppress the jitter of the input signal. The major part of the random walk filter is an up-down counter with a modulus of \( 2K \), which is controlled by the K modulus controller in Figure 3. The initial value of the counter is K. When the error signal from the DPD is high, the up-down counter counts up by the number of pulses of the clock \( f_s \). An advance pulse is produced if the counter counts up to \( 2K \). When the error signal is low, the counter counts down. A retard pulse is produced if the counter counts down to zero. The counter is reset to be K when its count is equal to 2K or zero, and counts up or down again. Then, the phase error is converted into \( n_e \), which is the synthesis value of advance and retard pulses in one control period. The PI controller is actually the DLF. Its output \( \Delta n \) and the central divider \( N_0 \) control the DCO output frequency by varying the divider ratio \( N \). The DCO output is sent to generate the modulation pulses for the inverter as well as fed back to the PI controller to work as an updating control signal.

\[ \theta_r (k+1) = \theta_r (k) + \omega_r (k) T_s \]  

Where, \( T_s = 1/f_s \) is the sampling period. Similarly, the phase angle \( \theta_f \) is given by the integration of the frequency \( \omega_f \) of the phase feedback signal.

\[ \theta_f (k+1) = \theta_f (k) + \omega_f (k) T_s \]  

The DPLL can be modelled as a subtractor ([8]). Therefore, the phase error \( \theta_e \) between the input phase reference and the phase feedback signal in each sampling cycle can be expressed as:

\[ \theta_e (k) = \theta_r (k) - \theta_f (k) \]  

The synthesis value \( n_e \) of the number of advance and retard pulses has a linear relationship with the phase error \( \theta_e \) in each control cycle, which is:

\[ n_e (k) = \frac{2 \theta_e (k)}{K T_s \omega_o (k)} \]  

Where, \( \omega_o \) is the frequency of the DCO output. It must to be noted that frequency \( \omega_f \) is equal to \( \omega_o \) in fact. The output of the PI controller is related to the synthesis value \( n_e \) as follows:

\[ \Delta n (k) = k_p n_e (k) + k \sum_{i=0}^{n_e} n_e (i) \]  

Then, the frequency \( \omega_o \) of the DCO output is given by:

\[ \omega_o (k) = \frac{2 \pi}{\left[ N_0 + \Delta n (k) \right] T_s} \]  

In our design, the central frequency of the DCO is actually equal to the frequency of the phase reference signal. And during the operation of the overall system, the switching frequency of the H-bridge is close to the natural resonant frequency of the resonant load. Therefore, we can assume that the DPLL always operates around the steady point. The linear model of the DPLL can be obtained through the linearization of (1)–(6). Let the Z-transformation of a discrete time sequence \( x(k) \) be denoted using its capital letter as \( X(z) = \mathcal{Z}[x(k)] \), and then the linear mode of the DPLL can be obtained. When the DCO output is fed back to be the phase feedback signal, the block diagram of the linear model of the DPLL is derived as shown in Figure 4. With the help of this linear model, the error transfer function relating the phase error \( \theta_e \) to the input phase reference \( \theta_r \) is:

![Diagram](image.png)
\[
G(z) = \frac{\delta_1(z)}{\delta(z)} = \frac{K N_1 (z-1)^2}{K N_1 z^2 + 2(k_p + k_i - K N_0) z + K N_1 - 2 k_p} \quad (7)
\]

Figure 4. The block diagram of the linear model for the DPLL.

To keep the closed system given by (7) stable, the following inequalities must hold true by using Jury’s stability test ([9]):

\[ k_p > 0, \quad k_i > 0 \quad \text{and} \quad 2 k_p + k_i < 2 K N_0. \]

If the sampling frequency is defined, the dynamic performance of the DPLL is determined by the parameters: \( k_p, k_i, \) and \( K. \) The different value of \( N_0 \) implies different input phase reference frequency. Figure 5 shows the input/error step response of the DPLL with different parameters. From Figure 5, we can conclude that: 1) the bigger \( k_p \) can improve the lock-in speed and stability of the DPLL; 2) the smaller \( k_i \) can increase the stability margin but decelerate the system response; 3) if the modulus \( K \) of the random walk filter decreases, the response time of the DPLL will be shortened and the effect of the jitter suppression will be degraded; 4) the larger the value of \( N_0 \) (the lower the input phase reference frequency) is, the longer the lock-in time is. As denoted above, the performance of the DPLL can be satisfactory if parameters are properly designed in the real application.

4 VERIFICATION EXPERIMENTS

The proposed phase control scheme has been successfully applied to the two phase power converter system as shown in Figure 6. The phase controller is implemented based on Field Programmable Gate Array (FPGA) using Verilog HDL. Figure 8 shows the details of the phase controller and the realization of the controller.

Figure 6. Two phase power converter systems with series resonant converters.
The performance of the proposed DPLL with different parameters is studied by using the designed phase controller. Figure 8 illustrates the testing results of the power system using the designed phase controller. In Figure 8, $i_{o1}$ and $i_{o2}$ are the output current of the power unit #1 and unit #2, respectively. The two power supply units are operated simultaneously. The magnitude of the two output currents are almost the same, equaling to 4.5 kA. The frequency of the output currents is 1.05 kHz. In Figure 8 (a), the preset phase difference $\delta_{\text{ref}}$ is 90°, while the preset phase difference $\delta_{\text{ref}}$ is -90° in Figure 8 (b). To evaluate the phase control accuracy, time-phase analysis of the output currents of the two units has been done. For the both cases presented in Figure 8, the phase control error $\delta - \delta_{\text{ref}}$ ranges from -1° to +1°, which implies that the designed phase controller has the very high accuracy under any preset phase difference condition. With the aid of the proposed phase controller, flexible phase adjustment can be realized.

5 CONCLUSION

According to the requirement of phase control for the multi-phase power system with series resonant converters, an optimized phase control method is presented in this work. The phase control scheme is based on the proposed DPLL, which makes the design simple and effective. The designer just has to focus on the performance of the DPLL without considering the characteristics of load during the design of the feedback control of the load current phase. A linear mathematical model is also derived to guide the design of the parameters of the DPLL in order to obtain a better performance of the proposed phase control scheme. It is found that the designed phase controller has very high accuracy and good dynamic/ steady performance in the practical test. With the help of the design phase controller, the current phase difference of the multi-phase power system with series resonant converters can be adjusted easily and accurately.

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