TRACTABLE BOOLEAN AND ARITHMETIC CIRCUITS

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ABSTRACT

Tractable Boolean and arithmetic circuits have been studied extensively in AI for over two decades now. These circuits were initially proposed as “compiled objects,” meant to facilitate logical and probabilistic reasoning, as they permit various types of inference to be performed in linear-time and a feed-forward fashion like neural networks. In more recent years, the role of tractable circuits has significantly expanded as they became a computational and semantical backbone for some approaches that aim to integrate knowledge, reasoning and learning. In this article, we review the foundations of tractable circuits and some associated milestones, while focusing on their core properties and techniques that make them particularly useful for the broad aims of neuro-symbolic AI.

1 INTRODUCTION

Tractable circuits, both Boolean and arithmetic, have been receiving an increased attention in AI and computer science more broadly. These circuits represent Boolean and real-valued functions, respectively. They are called tractable because they allow one to answer some hard queries about these functions in polytime, typically through a linear-time, feed-forward pass through the circuit structure. The foundations of these circuits have been developed within the area of knowledge compilation, which aims to compile knowledge into tractable representations for the goal of facilitating efficient reasoning. This area of research has a long tradition in AI; see, e.g., [15] and [73, 95, 46, 41, 49, 107, 43]. A turning point, however, has been the work of [46] which presented a comprehensive theory of knowledge compilation based on tractable Boolean circuits, which are deep representations, in contrast to earlier efforts which focused on flat representations based on conjunctive and disjunctive normal forms; see, e.g., [73, 95]. Another turning point has been the work of [36, 37] which employed tractable Boolean circuits in probabilistic reasoning, giving birth to an extensive line of work on tractable arithmetic circuits. The literature on tractable circuits has enjoyed a number of additional and exciting developments over the years, which have broadened and extended their applications from reasoning, to learning and more recently to neuro-symbolic AI; an area that is concerned with integrating neural and symbolic approaches to AI [56, 89, 10]. These developments have also raised key questions, and in some cases confusions, particularly on tractable arithmetic circuits and their relationship to tractable Boolean circuits and the now prevalent technique of weighted model counting [21]. The goal of this article is to discuss the foundations of tractable Boolean and arithmetic circuits, to clarify their relationships, and to highlight some of the key developments that have contributed to the growing interest surrounding tractable circuits today. But first, we find it pertinent to further elaborate on how and why the role of tractable circuits has evolved over the years.

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The original motivation behind knowledge compilation and tractable circuits was based on the following observation. In many reasoning tasks, one is typically interested in posing a large number of queries so the (high) cost of offline compilation can be amortized over the large number of online queries. Today, however, tractable circuits are playing a significantly broader role for a number of reasons. First, these circuits have been providing a systematic methodology for computation, particularly for problems beyond NP which include important tasks in probabilistic reasoning and machine learning; see [43] for a recent survey. Second, reasoning with tractable circuits is not only efficient but can almost always be conducted using linear-time algorithms that traverse these circuits in a feed-forward fashion like neural networks. Moreover, tractable circuits are differentiable. In fact, backpropagation has been performed on these circuits, both Boolean [35] and arithmetic [37], as early as two decades ago when the derivatives were first employed in reasoning tasks. These properties of tractable circuits made them very suitable for integration with modern pipelines for machine learning and neuro-symbolic AI; see, for example, [51, 112, 111, 70, 22, 72, 92, 54, 59, 53] where tractable circuits have been recently employed in and/or integrated with neural networks, deep reinforcement learning, Bayesian network classifiers and (deep) probabilistic logic programs. Even the traditional offline/online divide that originally motivated knowledge compilation for reasoning is now being exploited in modern settings as it is aligned with the training/inference divide that governs modern AI systems; see, e.g., [51]. As such, a recent trend has emerged in which tools and techniques that were initially envisioned for reasoning tasks are now being employed to facilitate learning and its integration with knowledge and reasoning. A few additional milestones have contributed to broadening the applications of tractable circuits and their expanded role today. First is the learning of tractable arithmetic circuits from data, starting with [71]; see also [91]. Second is handcrafting the structure of these circuits, which started with [88]. These developments have significantly expanded the utility of tractable circuits as they provided other modes of usage, beyond compilation from models. They also triggered modern treatments of the theory of tractable arithmetic circuits that are independent of compilation, starting with [24] that we shall discuss later. Another milestone is the integration of tractable Boolean and arithmetic circuits, starting with [67], which provided a profound, new formalism for integrating symbolic knowledge into circuits that perform probabilistic reasoning.

This article is organized as follows. We first treat tractable Boolean circuits in Section 2, followed by tractable arithmetic circuits in Section 3. We then discuss algorithms that compile knowledge into tractable circuits in Section 4 and close with some remarks in Section 5. We do not treat the rich subjects of handcrafting and learning (the structure of) tractable arithmetic circuits as this is beyond the scope of this article.

2 TRACTABLE BOOLEAN CIRCUITS

The theory of tractable Boolean circuits is based on Negation Normal Form (NNF) circuits. These are Boolean circuits that have three types of gates: and-gates, or-gates and inverters, except that inverters can only feed from the circuit variables; see figure on the right. NNF circuits are not tractable. However, by imposing certain properties on them we can attain different degrees of tractability. A comprehensive, but now incomplete,
treatment of tractable NNF circuits was given in [47], in which these circuits were studied across the two dimensions of tractability and succinctness. As we increase the strength of properties imposed on NNF circuits, their tractability increases by allowing more queries to be performed on them in polytime. This typically comes at the expense of succinctness as the size of circuits gets larger. We will next review some classes of tractable Boolean circuits, with increasingly stronger properties, which will allow us to efficiently solve decision problems (and their functional variants) that are complete for the complexity classes \( NP \subseteq PP \subseteq \text{PP}^P \); see also [43]. The algorithms for these increasingly complex problems all take time linear in the circuit size, and operate by traversing the circuit in a feed-forward fashion like neural networks. In the following discussion, we will omit inverters from NNF circuits and use \( \neg X \) instead to represent an inverted variable \( X \).

**Decomposability** One of the simplest properties that make NNF circuits tractable is decomposability [34]. According to this property, circuit fragments that feed into an and-gate cannot share variables. Figure 1 illustrates this property by highlighting two fragments (shaded) that feed into an and-gate. The fragment on the left feeds from variables \( K \) and \( L \). The one on the right feeds from variables \( A \) and \( P \). NNF circuits that satisfy the decomposability property are known as DNNF circuits. \( \text{Sat} \), an \( NP \)-complete problem [32], can be decided in linear time on DNNF circuits [34]. In this context, \( \text{Sat} \) is the problem of deciding whether the circuit has a satisfying input (generates output 1).

**Determinism** The next property we consider is determinism [35], which applies to or-gates in an NNF circuit. According to this property, at most one input for an or-gate can be high under any circuit input. Figure 1 illustrates this property when all circuit variables \( A, K, L, P \) are high. Examining the or-gates in this circuit, under this circuit input, one sees that each or-gate has either one high input or no high inputs. This property corresponds to mutual exclusiveness when an or-gate is viewed as a disjunction of its inputs. NNF circuits that are decomposable and deterministic are known as d-DNNF circuits [35] and they are exponentially less succinct than DNNF circuits [13].\(^4\) The \( PP \)-complete problem \( \text{MajSat} \) [63] can be decided in polytime on d-DNNF circuits. In this context, \( \text{MajSat} \) is the problem of deciding whether the majority of circuit inputs satisfy the circuit. If d-DNNF circuits are also smooth [35], a property that can be enforced in quadratic time, these circuits allow one to perform \( \#\text{Sat} \) [108] in linear time; that is, counting the number of satisfying circuit inputs, also known as model counting. If one assigns a weight to each variable value, one can define a weight for each circuit input as the product of weights assigned to its variable values. One can then sum the weights of satisfying circuit inputs also in linear time, a problem that is known as weighted model counting (WMC) [21].

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\(^3\) The size of a circuit is defined as the number of its edges.

\(^4\) That is, there are Boolean functions that can be represented using DNNF circuits of polynomial size but their d-DNNF circuits must have exponentially size.
**Smoothness** This property requires all circuit fragments feeding into an or-gate to mention the same variables; see illustration on the right. Enforcing smoothness can introduce trivial gates into the circuit, such as the bottom or-gate in the illustration. One can enforce smoothness in quadratic time [35] and sometimes more efficiently [105]. An example of model counting using a d-DNNF circuit is depicted in Figure 2 (left). Every literal in the circuit, whether a positive literal (\(A\)) or a negative literal (\(\neg A\)), is assigned the value \(\varepsilon\). Constants \(\top\) and \(\bot\) are assigned the values \(\varepsilon\) and \(\nu\), respectively. We then propagate these numbers upwards, multiplying numbers assigned to the inputs of an and-gate and summing numbers assigned to the inputs of an or-gate. The number we obtain for the circuit output is the model count. In this example, the circuit has 9 satisfying inputs out of 16 possible ones. We can also obtain model counts under variable settings in linear time. For example, if we wish to count the number of satisfying circuit inputs in which \(A = \varepsilon\) and \(K = \nu\), we simply assign \(\nu\) to literals \(A\) and \(K\) instead of \(\varepsilon\) and then propagate counts as just discussed. This is illustrated in Figure 2 (right), which shows that 2 out of the 9 satisfying circuit inputs have \(A = \varepsilon\) and \(K = \nu\). If our goal is to find the model counts under each setting of a single variable, then all such counts can be obtained using a second pass on the smooth d-DNNF circuit. This pass performs backpropagation to compute partial derivatives which can be used to obtain these counts [35]. To perform weighted model counting, we simply assign a weight to a literal instead of the value \(\varepsilon\) and propagate the counts as usual. Model counting is a special case of weighted model counting when each literal weight is \(\varepsilon\).

**Decision** There are stronger versions of decomposability and determinism which give rise to additional, tractable NNF circuits. A stronger version of determinism is known as the decision property. It requires each or-gate \(g\) to have the form \(g = (X \land \alpha) \lor (\neg X \land \beta)\), where \(X\) is a circuit variable known as the decision variable of gate \(g\) (this or-gate will then satisfy the determinism property). NNF circuits that satisfy decomposability and decision are known as Decision-DNNF circuits [61] and they are exponentially less succinct than d-DNNF circuits [35, 7]. Suppose we split the circuit variables into \(X\) and \(Y\). We will say that the Decision-DNNF is \(X\)-constrained if no or-gate with a decision variable in \(X\) can appear below an or-gate with a decision variable in \(Y\) [87]. These circuits allow us to solve E-MajSAT and its functional variant in time linear in the circuit size. E-MajSAT is a decision problem that is \(\text{NP}^{\text{PP}}\)-complete [110]. It asks: is there an instantiation \(x\) under which the majority of instantiations \(y\) yield a satisfying circuit input \(xy\)? The functional version of E-MajSAT includes the computation of most likely partial instantiations in probabilistic reasoning [81, 87]. The corresponding feed-forward algorithm performs summation at or-gates with decision variables in \(Y\), maximization at or-gates with decision variables in \(X\), and multiplication at and-gates [87].

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5 The following time-stamped video link provides an intuitive explanation of the role of smoothness in model counting: https://youtu.be/kdMzmgyLFqs?t=1586

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**Figure 2:** Model counting through linear-time circuit traversal. Left: counting the number of satisfying circuit inputs. Right: counting the number of satisfying circuit inputs with \(A = 1\) and \(K = 0\). Unsatisfiable subcircuits always generate a count of 0 even if not smooth, so we can exclude them when checking smoothness.
Ordered Binary Decision Diagrams (OBDDs) [14] are perhaps one of the most studied, tractable representations of Boolean functions. OBDDs are a special case of Decision-DNNF circuits even though they are notated differently as shown on the right. Each internal node in an OBDD is labeled with a variable and has two outgoing edges: a low edges (usually dotted) and a high edge (usually solid). The leaf nodes of an OBDD are labeled with $0$ ($\bot$) or $1$ ($\top$). Variables must follow the same order on any path from the root to a leaf in an OBDD. Consider the root node in the OBDD on the right, which is labeled with variable $A$. This node has a low child $\alpha$ and a high child $\beta$. If we replace this node with the or-gate $\land (\alpha \land \beta)$ and repeat the same process recursively for OBDDs $\alpha$ and $\beta$, we obtain a Decision-DNNF circuit. That is, we obtain an NNF circuit that satisfies the decomposability and decision properties [46]. Free Binary Decision Diagrams (FBDDs) [57] generalize OBDDs by relaxing the variable ordering requirement while keeping a weaker property known as test-once: each variable must appear at most once on any path from the root to a leaf. FBDDs are also a special case of Decision-DNNF circuits once we adjust for notation and there is a quasipolynomial simulation of Decision-DNNF circuits by equivalent FBDDs [6]. Hence, while FBDDs are less compact than Decision-DNNF circuits, they are not exponentially less succinct. OBDDs are exponentially less succinct than FBDDs though [57] so they are also exponentially less succinct than Decision-DNNF circuits.

Structured Decomposability This is a stronger version of decomposability which is stated with respect to a full binary tree whose leaves are in one-to-one correspondence with the circuit variables [86]. Three such trees are depicted in Figure 3, which are known as vtrees. Structured decomposability requires each and-gate to have exactly two inputs $i_1$ and $i_2$, and to have a corresponding node $v$ in the vtree such that the variables of subcircuits feeding into $i_1$ and $i_2$ are in the left and right subtrees of node $v$. The DNNF circuit in Figure 1 is structured according to the vtree on the left of Figure 3. For example, all and-gates below the root or-gate conform to vtree node $v=1$ in Figure 3 (left).

Partitioned Determinism Structured decomposability and a stronger version of determinism, known as partitioned determinism, yield a class of NNF circuits known as Sentential Decision Diagrams (SDDs) [40]. These circuits allow one to solve MAJMAISAT and its functional variant in linear time. MAJMAISAT is a decision problem that is $\text{P}^{\text{PP}}$-complete and is also based on splitting the circuit variables into $X$ and $Y$. It asks: is there a majority of instantiations $x$ under which the majority of instantiations $y$ yield a satisfying circuit input $xy$? The functional variant of MAJMAISAT includes the computation of expectations such as $\text{[31]}$. To illustrate partitioned determinism, consider Figure 4 and the highlighted circuit fragment. This fragment corresponds to the Boolean expression $(p_1 \land s_1) \lor (p_2 \land s_2) \lor (p_3 \land s_3)$, where each $p_i$ is called a prime and each $s_i$ is called a sub (primes and subs correspond to subcircuits). Partitioned determinism requires that under any circuit input, precisely one prime will be high (i.e., the primes form a partition). In Figure 4, under the given circuit input, prime $p_2$ is
Figure 4: Illustrating the partitioned determinism property of NNF circuits. Dotted lines are high wires. Solid lines are low wires. Precisely one of $p_1$, $p_2$, and $p_3$ will be high for any circuit input.

high while primes $p_1$ and $p_3$ are low. This means that this circuit fragment, which acts as a multiplexer, is actually passing the value of sub $s_2$ while suppressing the values of subs $s_1$ and $s_3$. As a result, the or-gate in this circuit fragment is guaranteed to be deterministic: at most one input of the or-gate will be high under any circuit input. SDD circuits result from recursively applying this multiplexer construct to a given vtree (the SDD circuit in Figure 4 is structured with respect to the vtree on the left of Figure 3).\footnote{6 The vtree of an SDD is ordered: the distinction between left and right children matters.} Recall that MAiMAISat, the prototypical problem for the complexity class $\text{PP}^{\text{PP}}$ [110], is stated with respect to a split of circuit variables into $X$ and $Y$. If the vtree is constrained for $Y \subseteq X$, then this problem and its functional variant can be solved in linear time on the corresponding SDD [78]. Figure 3 illustrates the concept of a constrained vtree. When an SDD is structured with respect to a right-linear vtree, the result corresponds to an OBDD after adjusting for notation as discussed earlier. Figure 3 illustrates the concept of a right-linear vtree. In this case, every circuit fragment will have the form $(X \land \alpha) \lor (\neg X \land \beta)$ where literals $X$ and $\neg X$ are primes, and where $\alpha$ and $\beta$ are subs. OBDDs are therefore a subset of both FBDDs and SDDs and they are exponentially less succinct than SDDs [12]. SDDs and FBDDs are not comparable though in terms of succinctness [8, 11].\footnote{7 SDDs can be exponentially less succinct than FBDDs for some Boolean functions [8] and FBDDs can be exponentially less succinct than SDDs for some other functions [11] so these circuit types are not comparable. Hence, SDDs and Decision-DNNFs are not comparable either since FBDDs are a subset of Decision-DNNFs and can simulate them quasipolynomially [6]. However, both SDDs and Decision-DNNFs are exponentially less succinct than d-DNNF circuits since FBDDs are exponentially less succinct than d-DNNF circuits [35].}

We have covered in this section only a subset of the tractable Boolean circuits known today, but ones that provide the basis for many of the further refinements and additions; see, e.g., [69] and [96] for some recent additions and [107] for a relatively recent tutorial that covers more circuit types and discusses further the relative succinctness of these circuits. The circuit properties we covered also form a basis for the most influential types of tractable arithmetic circuits. We shall cover these circuit types in the next section.

3 TRACTABLE ARITHMETIC CIRCUITS

We saw in the previous section how counting the models of a tractable Boolean circuit is done through the application of arithmetic operations at Boolean gates: additions at or-gates and multiplications at and-gates. This counting task induces an arithmetic circuit that shares the structure of underlying Boolean circuit as shown in Figure 5, therefore inheriting its properties such as decomposability, determinism and smoothness. Decomposability and smoothness, being structural properties, maintain their exact definitions when moving from the Boolean to the arithmetic side. However, determinism ends up being phrased slightly differently as we shall see later.
Figure 5: Computing the weighted model count of a tractable Boolean circuit, where $w(\ell)$ represents the weight of literal $\ell$. This computation induces an arithmetic circuit that is superimposed on the Boolean circuit.

Figure 6: Constructing arithmetic circuits through a compilation process.

The above connection between tractable Boolean and arithmetic circuits originated from [36, 37], which compiled Bayesian networks into tractable arithmetic circuits to enable linear-time probabilistic reasoning on the compiled circuits; see Figure 6. According to this proposal, the Bayesian network is first encoded into a Boolean formula with literal weights, allowing one to reduce probabilistic reasoning into weighted model counting. The Boolean formula is then compiled into a tractable Boolean circuit (deterministic, decomposable and smooth), from which a tractable arithmetic circuit known as an AC is finally extracted. This approach is implemented by the ACE system, which was recently evaluated in [1] and shown to exhibit state-of-the-art performance; see also [52].

A more direct and modern account of tractable arithmetic circuits is given in [24], which reconstructed the proposal in [37] so it is independent of Bayesian networks, model compilation and weighted model counting. This modern treatment was motivated by two influential lines of developments. The first line, which started with [71], utilized arithmetic circuits in the context of learning, in contrast to reasoning. The second line of developments, initiated by [88], handcrafted the structure of arithmetic circuits instead of compiling them from models and dropped the property of determinism while keeping the circuits tractable for certain computations. These developments raised key questions but also broadened the applications of tractable arithmetic circuits significantly. We will next present the modern treatment of [24] which will allow us to also explain more recent classes of tractable arithmetic circuits, such as Sum-Product Networks (SPNs) [88] and Probabilistic Sentential Decision Diagrams (PS-DDs) [67]. As we shall see, the treatment in [24] is based on a key distinction between arithmetic circuits, which can lookup values, and tractable arithmetic circuits, which can also reason. As in the Boolean case, the degree to which an arithmetic circuit is tractable and, hence, its ability to conduct various forms of reasoning, depends on the specific properties that the circuit satisfies.

8 http://reasoning.cs.ucla.edu/ace/
which defines the quantities that these circuits are supposed to compute. The latter circuits lack such a reference point which can cause issues when stating and evaluating claims. The theory in [24] starts by defining the reference point of an arithmetic circuit, regardless of where the circuit originates from. This reference point is the notion of a factor: a generalization of a Boolean function that maps complete variable instantiations into non-negative numbers; see Figure 7 (a distribution is one type of a factor).

An arithmetic circuit is based on a set of discrete variables, which define a key ingredient of the circuit: the indicators. For each value \( x \) of a variable \( X \), we have an indicator \( \lambda_x \). The arithmetic circuit will then have constants and indicators as its leaf nodes (inputs) with adders and multipliers as its internal nodes; see Figure 7. The factor of an arithmetic circuit (the reference point) is obtained by evaluating the circuit at complete variable instantiations. To evaluate the circuit at an instantiation \( e \), we replace each indicator \( \lambda_x \) with 1 if the value \( x \) is compatible with instantiation \( e \) and with 0 otherwise [37]. We then evaluate the circuit bottom-up in the standard way. The factor \( f(A, B) \) in Figure 7 has four rows which correspond to the four instantiations of variables \( A \) and \( B \). Evaluating the circuit in this figure at each of these complete instantiations yields a value for each instantiation and therefore defines the reference factor. We say in this case that the arithmetic circuit computes this factor. We also say that this circuit can lookup the values of this factor. For example, in Figure 8 (left), the circuit evaluates to 12 under the complete variable instantiation \( A = \hat{a}, B = \hat{b} \) by setting the indicators to \( \lambda_a = 0, \lambda_{\hat{a}} = 1, \lambda_b = 0, \lambda_{\hat{b}} = 1 \). An arithmetic circuit can be evaluated at a partial variable instantiation using the same procedure, but the value returned may not be meaningful unless the circuit is tractable (i.e., unless the circuit satisfies certain properties). For example, Figure 8 (right) evaluates the circuit at partial instantiation \( A = a \) by setting the indicators to \( \lambda_a = 1, \lambda_{\hat{a}} = 0, \lambda_b = 1, \lambda_{\hat{b}} = 1 \) leading to a value of 8. However, this value is not meaningful since the circuit is not tractable so it cannot reason about the factor. This is a subject that we shall discuss in depth next.

The central question posed and treated in [24] is the following. Suppose we have an arithmetic circuit that computes a factor (i.e., looks up its values). Can this circuit reason about the factor and why? Constructing an arithmetic circuit that computes a factor can be done efficiently even when the factor is defined implicitly as a product of other factors (e.g., when the factor is defined by a probabilistic graphical model). Consider the factors and arithmetic circuit in Figure 7. Factor \( f(A, B) \) is the product of factors \( f_1(A) \) and \( f_2(A, B) \). The arithmetic circuit computes factor \( f(A, B) \) and is obtained by multiplying circuits \( \lambda_a + 2 \lambda_{\hat{a}} \) and \( 3 \lambda_a \lambda_b + 4 \lambda_{\hat{a}} \lambda_{\hat{b}} + 5 \lambda_a \lambda_b + 6 \lambda_{\hat{a}} \lambda_{\hat{b}} \), which compute factors \( f_1(A) \) and \( f_2(A, B) \), respectively.
Figure 8: An arithmetic circuit $\mathcal{A}C_1$, evaluated at complete variable instantiation $A=a$, $B=b$ and partial variable instantiation $A=a$. This circuit computes factor $f(A,B)$ in Figure 7: it can lookup the values of factor $f$. This circuit is not decomposable but is smooth and deterministic.

Figure 9: An arithmetic circuit $\mathcal{A}C_2$, the factor it computes, and evaluations of the circuit under the partial variable instantiations $A=a$ and $B=b$. This arithmetic circuit computes the factor marginals.

This can always be done and the size of resulting circuit is linear in the size of multiplied factors, not the size of their product which can be exponential.\(^9\)

The interest, however, is in tractable arithmetic circuits that can reason about a factor, not ones that can only look up its values. One fundamental reasoning task is that of computing the value of a partial variable instantiation, known as the marginals (MAR) problem [82]. Another fundamental reasoning task is that of identifying and computing the value of a most likely, complete variable instantiation, known as the MPE problem [82]. For factors that are induced by models such as Bayesian networks, the decision variant of MPE is NP-complete [106], the decision variant of MAR is PP-complete and its functional variant is \#P-complete [90], making these hard reasoning tasks.\(^10\)

Consider again the factor $f(A,B)$ in Figure 7 and the partial instantiation $A=a$. The marginal for this instantiation, $f(a)$, is the sum of values assigned to rows that are compatible with instantiation $A=a$: $f(a) = f(a,b) + f(a,\bar{b}) = 3 + 4 = 7$. This computation is quite fundamental as it corresponds to computing marginal probabilities when the factor represents a distribution. Interestingly enough, while the arithmetic circuit $\mathcal{A}C_1$ of Figure 7 does compute the factor, it does not compute its marginals. That is, it can lookup values of rows but cannot sum them up (i.e., cannot reason). A counterexample is shown on the right of Figure 8, where the circuit evaluates to 8 instead of 7 at instantiation $A=a$.

Figure 9 depicts another arithmetic circuit, $\mathcal{A}C_2$, which computes the same factor computed by $\mathcal{A}C_1$ of Figure 7. Unlike $\mathcal{A}C_1$ though, $\mathcal{A}C_2$ does compute the factor marginals. Figure 9 depicts example evaluations of $\mathcal{A}C_2$ to be contrasted with the evaluations of $\mathcal{A}C_1$ in Figure 8.

\(^9\) To see this, define the depth-two arithmetic circuit of factor $f_i(X)$ as follows: $\sum_x f_i(x) \prod_{x \notin X} f_x$, where $x \sim x$ means that value $x$ of variable $X \in X$ is compatible with instantiation $x$ of variables $X$. This arithmetic circuit has one layer of multipliers followed by a layer with one adder, and computes factor $f_i(X)$. If a factor $f$ is defined as the product of factors $f_1, \ldots, f_n$, then multiplying the depth-two circuits of factors $f_i$ yields a circuit that computes their product factor $f = f_1, \ldots, f_n$; see [24] for details.

\(^10\) MPE stands for Most Likely Explanation. A related problem is that of identifying and computing the value of a most likely instantiation of a partial set of variables, which is known as the MAP problem [82]. The decision variant of this problem is NP\(^{PP}\)-complete [81]; see also [39]. MAP stands for Maximum a Posteriori Hypothesis. Sometimes, MAP and partial MAP are used instead of MPE and MAP to denote these problems.
Figure 10: A factor, an arithmetic circuit $\mathcal{A}_C$ that computes this factor, and the corresponding maximizer circuit $\mathcal{M}_C$. This maximizer circuit computes the factor MPEs.

Figure 11: A factor, an arithmetic circuit $\mathcal{A}_C'$ that computes the factor marginals, and a maximizer circuit $\mathcal{M}_C'$ that does not compute the factor MPEs.

The question now is: Why did $\mathcal{A}_C$ compute marginals, and hence reason about the factor, while $\mathcal{A}_{C_1}$ could not? Before we answer this question, let us first examine another example of reasoning about a factor: computing the value and identity of a most likely, complete variable instantiation (MPE).

Consider Figure 10 which depicts $\mathcal{A}_C$ again and the factor it computes. The figure shows another circuit, $\mathcal{M}_C$, obtained by replacing the adders of $\mathcal{A}_C$ with maximizers. This is called a maximizer arithmetic circuit, introduced in [17]. If we evaluate this circuit at the empty variable instantiation by setting all indicators to 1, we obtain a value of 12 which is the maximal value attained by any row of the factor; see the right of Figure 10. If we further evaluate this maximizer circuit at instantiation $B=b$, we obtain a value of 10 which is the maximal value attained by any row of the factor that is compatible with instantiation $B=b$. One can verify that this maximizer circuit will compute the factor MPEs correctly for any variable instantiation, whether complete or partial.

Consider now Figure 11 which depicts a third arithmetic circuit, $\mathcal{A}_C'$, and the factor it computes. This circuit computes the factor marginals but does not compute the factor MPEs. The figure shows a counterexample where the maximizer circuit fails to correctly compute the MPE under the empty variable instantiation (all indicators set to 1). Why did $\mathcal{M}_C'$ not compute the factor MPEs while $\mathcal{M}_C$ did, even though both $\mathcal{A}_C$ and $\mathcal{A}_C'$ compute the marginals of their factors? We are almost ready to address this question, but we first need to introduce another fundamental notion to provide a profound answer.

**Complete Subcircuits**

The fundamental notion of a complete subcircuit was first introduced and utilized in [17]. We obtain a complete subcircuit by traversing a circuit top-down. When visiting an adder (or maximizer) node, we choose a single child of the node. When visiting a multiplier node, we choose all its children. Figure 12 depicts two examples. A complete subcircuit has a term and a coefficient. The term is the subscripts of indicators appearing in the subcircuit. The coefficient is the product of numbers appearing in the subcircuit. In Figure 12, the left subcircuit has term $\bar{a}, \bar{b}$ and coefficient 12. The right subcircuit has term $\bar{a}, \bar{b}$ and coefficient 10. If a maximizer circuit computes the factor MPEs, we can identify a most likely, complete variable instantiation by constructing a complete subcircuit as proposed by [17]. The procedure is...
Figure 12: Two complete subcircuits (highlighted edges) with their terms and coefficients.

simple and illustrated on the right of Figure 10. We traverse the circuit top-down. When visiting a maximizer node, we choose a single child that has the same value as the node. When visiting a multiplier node, we choose all its children. The complete subcircuit selected in Figure 10 has term $\bar{a}, \bar{b}$ and coefficient $e$. This means that $\bar{a}, \bar{b}$ is a most likely, complete variable instantiation and $e$ is its value.

From Lookup to Reasoning: The Source of Tractability

Suppose we have an arithmetic circuit that can lookup factor values (i.e., computes the factor). As discussed earlier, it is generally efficient to construct such circuits (e.g., for the factors specified by probabilistic graphical models). The fundamental question addressed by [24] is the following. Under what conditions, and why, will this circuit attain the ability to reason about the factor (e.g., compute its marginals or compute its MPEs)?

The answer rests in the properties satisfied by the arithmetic circuit: decomposability, determinism and smoothness. We already defined these properties for Boolean circuits. Decomposability and smoothness have identical definitions on arithmetic circuits when viewing adders/multipliers as or/and gates and indicators $\lambda_x$ as literals $X=x$. Determinism is defined as having at most one non-zero input for each adder node, when the circuit is evaluated under any complete variable instantiation. We already knew from about two decades ago that if the arithmetic circuit is deterministic, decomposable and smooth, it will compute marginals [37]. We also knew later that such a circuit will compute MPEs [17]. It was further observed about a decade ago that determinism is not needed for computing marginals, leading to a class of arithmetic circuits, known as Sum-Product-Networks (SPNs) [88], which are only decomposable and smooth ([88] referred to smoothness as completeness). We also came to know recently that relaxing determinism can lead to an exponential reduction in the size of an arithmetic circuit [24].

While determinism is not needed for computing factor marginals, it is needed for the correctness of the linear-time MPE algorithm of [17] that we discussed earlier. This was missed in some earlier works [88], which used this algorithm on non-deterministic arithmetic circuits (i.e., SPNs) without realizing that it is no longer correct. This oversight was noticed in later works [84, 74], which also showed the hardness of computing MPEs without determinism [84]. The property of determinism was later called selectivity in the works on SPNs, initially in [83], leading to what has been called Selective SPNs. Since these are arithmetic circuits that satisfy determinism, decomposability and smoothness, they do compute both marginals and MPEs as was already known earlier [37, 17]. As we shall see later, determinism plays another important role even when computing MPE is not of interest as this property allows the compilation of arithmetic circuits from models such as Bayesian networks without the need to search for circuit parameters (constants).

Some of the key insights provided in [24] related to why the properties of decomposability, determinism, and smoothness make arithmetic circuits tractable, particularly their ability to perform reasoning through linear-time circuit traversal. The fundamental notion here is that...

11 SPNs placed further structure on the location of circuit parameters, attaching them to the edges/inputs of adder nodes such that these inputs are multiplied by the corresponding parameters before being added.
of a complete subcircuit which we discussed earlier. Consider Figure 13 which depicts an arithmetic circuit, \( \mathcal{AC}_3 \), the factor \( f(A, B) \) it computes, and two complete subcircuits of \( \mathcal{AC}_3 \). As mentioned earlier, each complete subcircuit has a term \( x \) and a coefficient \( c \) and will be called an \( x \)-subcircuit. Both of the highlighted subcircuits in Figure 13 have \( \bar{a}, \bar{b} \) as their term and these are the only \( (\bar{a}, \bar{b}) \)-subcircuits. Their coefficients are 15 and 63, which add up to 78. This is the value assigned by factor \( f \) to the variable instantiation \( \bar{a}, \bar{b} \) = \( \bar{a}, \bar{b} \) of the complete subcircuit is consistent: it does not have conflicting variable values. Moreover, smoothness ensures that every variable is instantiated in the term of a complete subcircuit. Hence, decomposability and smoothness ensure that the term of a complete subcircuit is a complete variable instantiation. Furthermore, for a complete variable instantiation \( x \), adding up the coefficients of \( x \)-subcircuits leads to the value \( f(x) \) assigned by factor \( f \) to instantiation \( x \). Finally, when evaluating an arithmetic circuit at a partial variable instantiation \( e \), the circuit is simply adding up the coefficients of all \( x \)-subcircuits where \( x \) is compatible with \( e \), which yields the correct marginal for that instantiation, \( f(e) \) [24]. These results provided the first formal and semantical explanation of why these properties enable an arithmetic circuit that computes a factor to also reason about that factor, therefore making the circuit tractable.

We now get to the property of determinism. As shown in [24], determinism (with decomposability and smoothness) ensures a one-to-one correspondence between complete subcircuits and complete variable instantiations.\(^{12}\) Moreover, the coefficient \( c \) of an \( x \)-subcircuit corresponds to the value assigned by the factor to complete instantiation \( x \) \( : f(x) = c \). Figure 14 depicts an arithmetic circuit that is deterministic, decomposable and smooth. This circuit has four complete subcircuits, highlighted in the figure, which are in one-to-one correspondence with the instantiations of variables \( A \) and \( B \). In the order shown in Figure 14, the subcircuits have terms \( a, b; a, \bar{b}; \bar{a}, b; \bar{a}, \bar{b} \) and coefficients 3; 4; 10; 12 which match the rows of the factor computed by the circuit.

What determinism does is ensure that each row of the factor (a complete variable instantiation and its value) is represented by a single, complete subcircuit. This is essential for the linear-time MPE algorithm of [17] to work properly. Consider Figure 11 where this algorithm

\(^{12}\) Assuming no zeros in the circuit or factor; otherwise, the statement of this result is more refined.
This result was shown in Theorem 6 of [24] for circuits that compute Boolean factors $f(X)$. The parameters $\Theta = \{0, 1\}$ are complete for these factors since each row has a value in $\{0, 1\}$. If the circuit is decomposable and smooth but not deterministic, then some row $x$ with $f(x) = 1$ must be split over at least two $x$-subcircuits with non-zero coefficients. Since the coefficients of these $x$-subcircuits must add up to 1, there must exist an $x$-subcircuit whose coefficient is in the open interval $(0, 1)$ so the circuit must have a parameter not in $\{0, 1\}$.
the Bayesian network parameters. It is also exponentially sized so it is mostly of theoretical
interest such as illustrating the result we just discussed. Existing compilation algorithms
construct more compact arithmetic circuits without searching for parameters, assuming the
model parameters are known. When the model parameters are not known, these algorithms
compile arithmetic circuits with symbolic parameters that can be easily replaced with numeric
parameters that may be learned from data. This is a topic we shall discuss in Section 4.

It is worth noting that the original treatment of arithmetic circuits in [37] started where
our current treatment has ended in the previous paragraph. That is, the starting point of [37]
was the notion of a network polynomial which fully captures a distribution. The notion of
an arithmetic circuit was then introduced as a tool that can be used to compactly represent
the exponentially-sized network polynomial. This formulation was facilitated by the fact
that [37] also started by assuming the existence of a model (a Bayesian network), which fully
defines the network polynomial. This can no longer be assumed when handcrafting circuits
or learning them from data, which prompted the modern treatment in [24]. We finally note
that arithmetic circuits which compute distributions and their marginals can be used to reason
about uncertain evidence, also called soft evidence, in addition to evidence about continuous
variables with local, univariate densities. This can be done by setting the circuit indicators to
appropriate real values as discussed in [16] and [39, Section 3.7], respectively.

Circuits that Reason about Constrained Factors

We now turn to a fundamental class of arithmetic circuits, known as PSDDs, which can
reason about constrained factors [67]. These are factors in which some rows have fixed
zero values so they define mappings from a subset of variable instantiations into non-negative
numbers; see Figure 16. Constrained factors, particularly ones representing distributions, have
many applications. For example, when learning arithmetic circuits that represent distributions
from data, one may have domain knowledge that rules out certain states of the world so we
need to ensure that any learned circuit will assign a zero probability to such infeasible
states. One may also want to induce or learn distributions over combinatorial (or structured)
objects such as total and partial rankings [29], graphs [77], game plays [28], routes on a
map [70, 28, 27, 99, 101] and subsets of objects [99]. Distributions over these kind of objects
have been captured using constrained factors and reasoned about using PSDDs as done in the
works mentioned in the previous sentence.

For an example of how constrained factors can be used to model combinatorial and struc-
tured objects, consider Figure 17 where the goal is to define a distribution over routes from
source s to destination t. Each edge on the map is modeled by a binary variable, A, . . . , H.
A route can be modeled using a variable instantiation that sets the variables of its edges to 1
and all other variables to 0. Clearly, some variable instantiations do not correspond to valid
routes so these get assigned probability 0; see the right of Figure 17. The corresponding
constrained factor is then guaranteed to induce a distribution over only valid routes from
source s to destination t. Similar techniques can be used to represent other combinatorial or

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14 For another theoretical result with substantial practical implications, we note that the polynomial partial derivates
with respect to indicators and parameters correspond to useful probabilistic quantities which can be computed by
backpropagation on any equivalent arithmetic circuit. These quantities correspond to marginals of additional variable
instantiations. They allow one to avoid further evaluations of the circuit which can lead to significantly more efficient
reasoning; see [37] for details.

15 Consider a variable X with values x1, . . . , xn. Uncertain evidence on variable X can be modeled as certain (hard)
evidence on some noisy sensor 𝑦 that is connected to variable X, where the noise is specified by the likelihoods
of 𝑦 given 𝑥𝑖. Pr(𝑦|𝑥𝑖) is then guaranteed to induce a distribution over only valid routes from source s to destination t. Similar techniques can be used to represent other combinatorial or

16 PSDD stands for Probabilistic Sentential Decision Diagram. A PSDD represents a probability distribution but can
also be used to represent and reason about general factors [98].
Figure 16: Left: A PSDD and the constrained factor it computes. The factor computed by this PSDD will always assign zero values to rows in which \( C = f \), regardless of how the PSDD is parameterized. Right: A PSDD fragment and its corresponding arithmetic circuit fragment. Boolean variables and their negations in the PSDD (e.g., \( A \) and \( \neg A \)) are converted to indicators in the arithmetic circuit (\( \lambda_A \) and \( \lambda_{\neg A} \)).

Figure 17: Modeling routes between source \( s \) and destination \( t \) as variable instantiations that satisfy some conditions. Each edge between two locations is modeled using a Boolean variable which is set to 1 if the edge is on a route and set to 0 otherwise. The variable instantiation on the left corresponds to a valid route. The variable instantiation on the right corresponds to an invalid (disconnected) route.

structured objects as long as one can define the conditions that specify variable assignments which correspond to the objects of interest.

A constrained factor is defined by specifying feasible variable instantiations and their values. The main insight behind PSDDs is to specify feasible instantiations using an SDD, which is a tractable Boolean circuit that we discussed in Section 2; see Figure 16 (left). The SDD should evaluate feasible instantiations to 1 and infeasible instantiations to 0 and is normally obtained through a compilation process of domain constraints. A distribution over the feasible instantiations can then be defined by assigning (local) distributions to the inputs of or-gates in the SDD, leading to a PSDD as shown in Figure 16.

The PSDD is a highly structured arithmetic circuit that comes with strong guarantees. We can convert a PSDD into an arithmetic circuit as shown in Figure 16 (right) by removing reference to the underlying SDD circuit. The resulting arithmetic circuit is guaranteed to not only satisfy determinism, decomposability and smoothness but to also satisfy the stronger properties of structured decomposability and partitioned determinism which are forced by the underlying SDD circuit which satisfies these properties. As a result, the induced arithmetic circuit enjoys many desirable properties. First, the circuit is guaranteed to produce a zero value for any infeasible variable instantiation regardless of how we set the PSDD parameters. Figure 18 depicts example evaluations of a PSDD circuit that can be used to gain insights into this guarantee. Moreover, the PSDD can compute marginals and MPEs by virtue of being deterministic, decomposable and smooth [67]. With an appropriate vtree for the SDD circuit, it can also compute expectations [78]. One can also learn the maximum-likelihood parameters of a PSDD in closed form when the data is complete [67]. An EM algorithm has also been developed for learning PSDD parameters from incomplete data, including highly structured data in which examples can be specified using Boolean constraints, not just variable instantiations [29]. PSDDs also play a key role in probabilistic reasoning as shown in [98].

Another key development has been the introduction of conditional PSDDs, which can compute and reason about factors that are conditionally constrained [100]. These are factors
Figure 18: Evaluating a PSDD at different variable instantiations (complete and partial). The PSDD will evaluate to 0 at any variable instantiations that does not satisfy the underlying SDD circuit. This is guaranteed regardless of how the PSDD is parameterized.

Figure 19: A conditional PSDD composed of an SDD circuit and two PSDDs that share structure. The SDD defines two constrained factors over variables $X$ and $Y$ depending on the state of variables $A$ and $B$. These constrained factors are specified by PSDDs that share structure.

in which variables are partitioned into two sets, $X$ and $Y$, where the infeasible instantiations of $Y$-variables are conditioned on the state of $X$-variables. Conditional PSDDs allow one to integrate conditional constraints into tractable arithmetic circuits. For example, which routes are feasible in a neighborhood may be conditional on how we enter and exit that neighborhood [101]. Figure 19 depicts a conditional PSDD, which is composed of an SDD circuit and a set of PSDDs that share structure.

Further Extensions

The theory of tractable arithmetic circuits has been developed and explored in various additional ways. For example, additional classes of arithmetic circuits have been studied using further combinations of tractable circuit properties, such as the combination of structured decomposability and smoothness [33]. Other reasoning tasks have also been considered which are enabled by the different properties of tractable circuits; see, e.g., [109]. Some of the new extensions and works have referred to arithmetic circuits as probabilistic circuits, while reserving the term “arithmetic circuits” to deterministic, decomposable and smooth circuits. This is in contrast to earlier treatments such as [98, 24] which did not tie this term to specific properties or exclusively to probability distributions. A fundamental new extension has been the class of Testing Arithmetic Circuits (TACs) which select their parameters dynamically, based
on circuit inputs through the inclusion of tests in the arithmetic circuit [25, 30]. Tractable arithmetic circuits represent multilinear functions (of indicators) [37]. Testing arithmetic circuits represent piecewise multilinear functions so they are universal function approximators like neural networks [30]. This new class of arithmetic circuits can be used to recover from some modeling errors that lead to compiled circuits that may not be expressive enough to fit the data generated by a mechanism that has been modeled incorrectly [102]. Recent theoretical results have shown that full recovery from some modeling errors is possible under certain conditions [60]. We finally note that some of the key properties of tractable circuits, including decomposability and determinism, have been exploited for tractable reasoning and learning in a more general, semiringing setting; see, e.g., [65, 66, 55, 9].

4 COMPILING MODELS INTO TRACTABLE CIRCUITS

We will next provide an overview of methods for constructing tractable circuits through a process of compilation. We will provide a brief summary of methods for tractable Boolean circuits and elaborate more on methods for tractable arithmetic circuits.

Tractable Boolean circuits are normally compiled from Boolean formulas that represent logical knowledge or constraints. This is done using systems known as knowledge compilers, such as D4 [68], c2d [38], CUDD, MINI-c2d [79, 80], DSHARP [76] and the SDD library [23]. Knowledge compilers can be categorized as top-down or bottom-up. Top-down compilers are based on keeping a trace of the exhaustive DPLL algorithm [61] and they generally incorporate advanced SAT techniques [93, 80]. These compilers normally operate on Boolean formulas in conjunctive normal form, tend to have better space complexity, and include D4, c2d and DSHARP which yield Decision-DNNFs, and MINI-c2d which yields SDDs. Bottom-up compilers incrementally compile a formula, by first compiling its components and then combining these compilations. They tend to operate on more general classes of Boolean formulas, demand more space, and include CUDD and the SDD library, which yield OBDDs and SDDs, respectively.

Turning next to the compilation of tractable arithmetic circuits, we first note that PSDDs, which represent distributions, are somewhat special as these arithmetic circuits are based on SDDs, which are Boolean circuits. Hence, the structure of a PSDD is obtained by first compiling a Boolean formula into an SDD, which is then parameterized to yield a PSDD. The PSDD parameters are typically obtained through a learning process based on complete or incomplete data [67, 29]. The Boolean formula that triggers this compilation process usually defines feasible states of the world, or characterizes structured (combinatorial) objects such as routes, graphs, and rankings.

Arithmetic circuits that satisfy determinism, decomposability and smoothness, also known as ACs, are typically compiled from probabilistic models such as Bayesian networks and probabilistic logic programs. We will only discuss the former but see [72, 54, 53] for some examples of the latter. Recall again that the structure of arithmetic circuits that satisfy only decomposability and smoothness (i.e., SPNs) is normally handcrafted or learned from data since relaxing determinism complicates the compilation of these structures from models as discussed in the previous section.

The compilation of Bayesian networks (and probabilistic graphical models more generally) is done either directly, or indirectly as shown in Figure 6. Indirect methods are based on reductions to weighted model counting [21]. The model is first encoded into a Boolean formula with weights on literals, as initially proposed in [36, 37]. The Boolean formula is then compiled into a smooth d-DNNF circuit (a tractable Boolean circuit), from which a tractable arithmetic circuit is extracted. The size of the final arithmetic circuit depends on the

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17 D4: http://www.cril.univ-artois.fr/kc/d4; c2d: http://reasoning.cs.ucla.edu/c2d; CUDD: https://davidkebo.com/cudd; MINI-c2d: http://reasoning.cs.ucla.edu/minic2d; DSHARP: https://bitbucket.org/haz/dsharp; SDD library: http://reasoning.cs.ucla.edu/sdd. A Python wrapper of the SDD library is available at https://github.com/wannesm/PySDD and an NNF-to-SDD circuit compiler, based on PySDD, is available at https://github.com/art-ai/nnf2sdd.

18 See https://github.com/art-ai/pypsdd, http://reasoning.cs.ucla.edu/psdd; and https://github.com/hahaXD/hierarchical_map_compiler for some related tools.
Figure 20: Compiling the Bayesian network $B \leftarrow A \rightarrow C$ into tractable arithmetic circuits. The circuit on the left computes the probability of (partial) evidence on variables $A$, $B$ and $C$. The circuit on the right computes the distribution of variable $B$ given (partial) evidence on variables $A$ and $C$ (after normalization); this circuit targets a particular query, $P(B|.)$. In both cases, the circuit parameters correspond to Bayesian network parameters so they can be fetched from the Bayesian network, if known; otherwise, they can be learned from data.

size of compiled Boolean circuit, which is determined by the quality of used encoding scheme and knowledge compiler. These encoding schemes capture both the global structure of the model (its topology) and its local structure (parameters). Their efficacy relies particularly on how well they encode local structure; that is, the extent to which they capture the properties of model parameters. The first encoding scheme [36] was somewhat basic in nature, but it was later followed by more refined and potent encodings in [94, 18, 19]. A comparative discussion of various encoding schemes, including some more recent ones, is given in [52]. The above approaches have traditionally used top-down compilers of Boolean formulas into tractable Boolean circuits; for example, the ACE system [21] used the top-down $c2d$ knowledge compiler. More recently, bottom-up compilation approaches have also been proposed, which are based on compiling the factors of a probabilistic graphical model into tractable circuits and then combining these compiled circuits in a bottom-up fashion [26, 98].

Direct methods for compiling models into tractable arithmetic circuits are simpler but they tend to be less effective, with some exceptions. These methods include the extraction of a tractable arithmetic circuit from the structure of a jointree for the model [37]. They also include methods based on the variable elimination algorithm [20, 42]; see also [39, Chapter 12]. The most recent of these methods [42] is based on variable elimination and stands out for a number of reasons. First, the method compiles circuits that target a specific class of queries, specified by evidence variables (input) and a query variable (output), which is meant to facilities supervised learning from labelled data; see Figure 20. Second, this recent method compiles arithmetic circuits in the form of computation graphs in which nodes represent tensor operations instead of arithmetic operations, allowing parallelization during parameter learning and inference. Third, this method computationally exploits a new type of local structure: functional dependencies whose identities are unknown. We have a functional dependency between a node and its parents in the Bayesian network when the state of the node is a function of the states of its parents (i.e., there is no uncertainty). A functional dependency is unknown when we do not know the identity of this function. This is significant in a learning context where the goal is to learn such functions from data. This is also significant for causal inference where functional dependencies are known as causal mechanisms which are typically unknown [44]. This latest algorithm [42] was motivated by the use of tractable arithmetic circuits for supervised learning, as in neural networks, but where the structure of the circuit is compiled from a model instead of being handcrafted as is normally the case with neural networks. Recent results [22] have shown the promise of this approach to supervised learning as it provides a principled method for embedding background knowledge into the learning process (independence constraints, logical constraints, known parameters, and unknown functional dependencies).

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19 See also [85, 75] for related representations of circuits with handcrafted or learned structures.
We close this section by the following remark on the interplay between the compilation of circuit structure and the learning of circuit parameters. Initially, the goal of compilation algorithms was to facilitate reasoning since various forms of inference can be performed in linear time on the compiled circuits. In this context, the assumption was that one already knows the model parameters before the compilation process starts. Later, however, these compilation algorithms were used to compile only the circuit structure and then coupled with additional algorithms that learn the circuit parameters from data. The key observation which permits this expanded role is that the compilation process can be conducted even if we do not know the model parameters. In particular, the substitution of model parameters into the compiled circuit can be postponed to the extraction phase of Figure 6. Hence, if a parameter is unknown, it can be kept in symbolic form during the extraction phase and then learned from labeled or unlabeled data after the compilation process is concluded; e.g., as in [42, 22] and [67, 29], respectively. This is possible since determinism (with decomposability and smoothness) allows one to compile circuits with parameters that correspond to model parameters as discussed in the previous section; see also the circuits in Figure 20 and [44] for a recent exposition of how this is done. Interestingly enough, determinism also facilitates the learning of circuit parameters, allowing one to learn parameters in closed form under complete data, in addition to allowing a linear-time evaluation of the EM update equations under incomplete data.\(^{20}\) This further highlights the importance of determinism, which also holds for tractable arithmetic circuits with handcrafted or learned structures.\(^{21}\)

## 5 CONCLUDING REMARKS

Tractable Boolean and arithmetic circuits have been evolving into a computational and semantical backbone for modern approaches that aim to combine knowledge, reasoning, and learning. The different modes of constructing these circuits—through compilation, handcrafting and learning—have further contributed to their versatility and positioned them as valuable tools for serving the objectives of neuro-symbolic AI. We provided an overview of tractable circuits in this article, while focusing on their foundations, their salient properties, and some of the key developments and milestones that have contributed to their current status in the field. There is much more to say about tractable circuits beyond what has been covered in this treatment. This includes the various handcrafted architectures, the learning of circuits structures (and parameters) from data, and the compilation of these circuits from higher-level models and other forms of knowledge.

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\(^{20}\) For complete data, this follows directly from the same result for Bayesian networks. For incomplete data, a second pass (backpropagation) on the circuit provides marginals over families (variables and their parents)\(^{37}\) which is all that one needs to evaluate the EM update equations\(^{39, Eq \text{17.7}}\).

\(^{21}\) For arithmetic circuits with handcrafted or learned structures, determinism can also facilitate parameter learning if these parameters are properly located as in [83] and [67]. For further perspective, see [113] for a treatment of parameter learning when the arithmetic circuit does not satisfy determinism.
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