This paper presents a scalable deep learning model called Agile Temporal Convolutional Network (ATCN) for high-accurate fast classification and time series prediction in resource-constrained embedded systems. ATCN is a family of compact networks with formalized hyperparameters that enable application-specific adjustments to be made to the model architecture. It is primarily designed for embedded edge devices with very limited performance and memory, such as wearable biomedical devices and real-time reliability monitoring systems. ATCN makes fundamental improvements over the mainstream temporal convolutional neural networks, including residual connections to increase the network depth and accuracy, and the incorporation of separable depth-wise convolution to reduce the computational complexity of the model. As part of the present work, two ATCN families, namely T0, and T1 are also presented and evaluated on different ranges of embedded processors - Cortex-M7 and Cortex-A57 processor. An evaluation of the ATCN models against the best-in-class InceptionTime and MiniRocket shows that ATCN almost maintains accuracy while improving the execution time on a broad range of embedded and cyber-physical applications with demand for real-time processing on the embedded edge. At the same time, in contrast to existing solutions, ATCN is the first time-series classifier based on deep learning that can be run bare-metal on embedded microcontrollers (Cortex-M7) with limited computational performance and memory capacity while delivering state-of-the-art accuracy.

**Keywords** Temporal Convolutional Networks (TCN), Recurrent Neural Networks (RNN), Real-time Edge Computing

## 1 Introduction

The rapid growth in deep learning algorithms has changed how embedded and cyber-physical systems (CPS) process the surrounding environment and has significantly improved the overall CPS performance on delivering their assigned tasks. Time series analysis and forecasting are important applications that can significantly benefit from the deep learning paradigm on a broad range of smart IoT and embedded edge devices. Few pronounced examples are wearable health monitoring devices [1][2][3], on-board predictive maintenance [4][5][6], machine translation [7][8], and smart transportation systems [9][10][11]. These applications all demand real-time accurate processing of time series on edge devices with limited computational resources.

For most deep learning practitioners, recurrent networks and especially two elaborated models, namely, LSTM [12] and GRU [13], are synonymous with time series analysis due to its notable success in sequence modeling problems such as machine translation, language processing, and device health monitoring. These models interpolate the output based on the current and temporal information, which is learned and propagated across the hidden states sequen-
The propagation chain of hidden states causes two major issues [14]: 1) gradient instability such as vanishing/exploding gradients and 2) fewer levels of parallelization due to existing dependencies across the cells.

Temporal Convolutional Networks (TCN) were first proposed based on an adaptation of WaveNet [15] and Time-Delay Neural Network [16]. It orchestrates dilated convolutions in Encoder-Decoder architecture to have a unified framework for action segmentation. Later, Bai et al. [14] designed a Generic TCN (GTCN) architecture for sequence modeling, which outperforms LSTM on time-series and sequence modeling tasks. However, the GTCN suffers from two main drawbacks: 1) the size of dilation increases exponentially by the layer, which prevents the designer from increasing the depth of the network, 2) it uses two standard convolutions per each layer, which is computationally expensive for resource-constrained embedded systems. Overall, there is a lack of high-accurate lightweight deep learning solution that can be used for robust processing of time series on embedded edge devices for a broad range of embedded applications.

This article proposes an Agile Temporal Convolutional Network (ATCN) which is a novel algorithmic solution for real-time deep learning processing of time series on embedded and edge devices. ATCN presents a family of fast network architectures with various scaling knobs to meet a variety of design constraints. In ATCN, mirrored Spectral-Temporal Convolution Blocks (STCB) are chained in the form of Encoder-Decoder segments. In each block, residual connections are utilized to deepen the network, while separable depthwise convolutions are used to reduce the computational cost.

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2 The source code of the ATCN model will be publicly available at https://github.com/TeCSAR-UNCC/ATCN
putational complexity. Fig. 1 illustrates the pairwise accuracy-latency of T0 (Fig. 1(a)-1(b)) and T1 (Fig. 1(c)-1(d)) versus MiniRocket [17] which is the State-of-the-Art (SotA) network on 70 benchmarks from the UCR 2018 dataset [18]. The latency as explained in detail in Section 5 is reported based on running benchmarks on Cortex-A57. While T0 is 1.4× faster than MiniRocket on average, it has better or equivalent accuracy for 30 benchmarks. In terms of accuracy, T1 and MiniRocket do not differ significantly from each other, but T1 does improve the latency for an average of 6%. However, MiniRocket cannot be run on the Cortex-M7 microcontroller, T0 and T1 can be compiled and executed natively on bare-metal M7. Our experimental results also indicate that the T0 configuration reduces the MACs and model size by 102.38× and 16.84× over InceptionTime [19], respectively. T1 also has a 73.59× reduction in MACs, and a 14.23× reduction in model size over InceptionTime.

Overall, the key contributions of this article are:

- Proposing T0 and T1 as two members of the ATCN family network whose computation complexity and model size are extremely low. Additionally, the T1 model accuracy difference is statistically insignificant when compared to those of SotA networks.
- Automating the creation and training of different configurations of ATCN based on the complexity of the problem in terms of accuracy.
- Demonstrating the significant benefits of ATCN over SotA networks when it comes to execution on embedded IoT microcontrollers and microprocessors (ARM Cortex-M7, and Cortex-A57).

The rest of this article is structured as follows: Section 2 presents the literature review, while Section 3 provides background on generic TCN and its architecture. In Section 4, we elaborate on the Temporal-Spectral block, the ATCN architecture, and its hyperparameters. Section 5 presents the experimental results including comparison with existing approaches, and finally Section 6 concludes this article.

2 Related Works

Traditional convolutional neural networks have been primarily used in computer vision applications due to their success in capturing spatial features within a two-dimensional frame. Recently, research has shown that specialized CNNs can recognize patterns in data history to predict future observations. This gives researchers interested in time-series forecasting options to choose from over RNNs, which have been regarded in the community as the established DNN for time-series predictions. In one such case, Dilated Convolutions (DC) have been shown to achieve state-of-the-art accuracy in sequence tasks. In the first use of DC, WaveNet [15] was designed to synthesize raw audio waveform, and it outperforms the LSTM. Later, Lea et al. [20] proposed TCN, a unified network based on WaveNet DC, for video-based action segmentation. In the same trend, the gated DC was used for the sequence to sequence learning [21]. The proposed approach beats deep LSTM in both execution time and accuracy.

GTCN [14] is a generic architecture designed for sequence modeling. The design of GTCN was based on two main principles: 1) there shouldn’t be any information leakage from future to past, 2) the network should be able to receive any arbitrary input length similar to RNN. Since the main fundamental component of GTCN is based on variable-length DC, it brought higher parallelization and flexible receptive field in comparison to RNN. Also, since the gradient flow of GTCN is different from the temporal path of RNN, it is more resistant to the problem of gradient instability. Recent approaches have taken advantage of GTCN benefits or similar architectures in their works. In the work of [22], a modified version of GTCN with depth-wise convolution has been used to enhance the speech in the time domain. The DeepGLO [23] is another work that used a global matrix factorization model regularized by a TCN to find global and local temporal in high dimensional time series.

InceptionTime [19] is an ensemble of CNN blocks called Inception Module and proposed as a solution for the Time Series Classification (TSC) problem. The network architecture was constructed based on the Inception-v4 [24] structure, and it employed a larger kernel size to beat enormous and complex models such as the HIVE-COTE [25]. Another research article based on deep learning methodology called Elastic Matching-CNN (EM-CNN) [26] aims at enhancing famous vision CNNs, such as Inception, and ResNet, with matching convolution (MConv) to outperform SotA solutions such as HIVE-COTE for time series classification. Nonetheless, they are still exceedingly heavy for the microcontroller with limited resources, such as ARM Cortex-M series, or even embedded ARM Cortex-A series microprocessors.

Both HIVE-COTE and Rocket [27] are current non-deep learning methods that are regarded as SotA for time series classification. Rocket consists of a linear classifier and signal transformers that map inputs into features by convolving them through various and random kernels. To classify the inputs, the extracted features are passed through the linear layer. MiniRocket is a variant of Rocket that minimizes training time while ensuring accuracy by reducing exploration
space and using kernels with almost deterministic values to minimize transformer complexity. However, due to the non-deep learning characteristics of their models, they still suffer from the lack of standard tools and libraries to map and execute on bare-metal embedded microcontrollers.

On top of algorithmic design, pruning [28, 29, 30], quantization [31, 29, 32], and knowledge distillation [33] are orthogonal compression methods to enable implementation and optimization of deep learning algorithms on tightly resources constrained edge devices. McFly [34] is another independent research line, which is a brute force algorithm that finds hyperparameters for existing models such as InceptionTime and ResNet to explore design and training knobs to find optimal network configuration. This paper proposes ATCN for embedded and resource-constrained hardware to address time-series domain problems, which is on par with InceptionTime in terms of accuracy performance. The unique Encoder-Decoder structure of ATCN with the use of depthwise convolution and residual connection helps the model have a better or similar performance in respect to the InceptionTime without putting a burden on final hardware. We have put ATCN on test in Section 5 by comparing ATCN against InceptionTime over 70 benchmarks from UCR time-series datasets. Additionally, we have reported the execution profile of the Cortex-M7 and Cortex-A57 when running ATCN families. We have shown that ATCN improves or maintains the overall system accuracy for these three cases while minimizing computational complexity and model size. In the next section, we study the structure of DC in-depth to prepare the ground for introducing ATCN in Section 4.

3 Background: Temporal Neural Networks

GTCNs are designed around two basic principles: 1) the convolutional operations are causal, i.e., predictions are made based only on current and past information; 2) the network receives an input sequence of arbitrary length and maps it to an output sequence of the same length [14]. Based on principle number 2, in order to map the final output to an arbitrary size, the output of the last DC output can be connected to a linear layer. This adds flexibility by allowing a final output length to be independent of the input length. The naive causal convolutions, which have a dilation rate of 1, are inherently inefficient as their sequence history scales with a size linear to the depth of the network.

The solution here incorporates dilated convolutions to exponentially scale the receptive field, as shown in Fig. 2. The kernel of a dilated convolution is stretched to cover a larger area of the input. In order to accomplish this, holes (zeroes) are placed between the kernel elements. The dilation rate defines the number of spaces that will be inserted between kernel elements, which determines the level of enlargement. The dilation rate of \( d \) is generally expressed in \( d - 1 \) spaces. Fig. 2 shows dilated convolutions applied on input vector \( X = [x_0, x_1, x_2, ..., x_{t-1}] \). The dilation rate for layer 0 is 1, equivalent to a standard convolution. When the depth increases, the dilation rate increases to 2 and then to 4, as 1 and 3 holes are inserted in the respective kernels. The first convolution with dilation rate \( d=1 \) maps the input vector \( X \) to the higher dimension. Then, GTCN increases the \( d \) for the next convolutions exponentially to increase the receptive field. The minimum output sequence length, before mapping to the linear layer, can be determined by calculating its receptive field: \( rf \):

\[
rf = 1 + \sum_{l=1}^{L} [k(l) - 1] \times d(l),
\]  

Figure 2: Dilated Causal Convolution.
where \( l \in \{1, 2, 3, \ldots, L\} \) is the layers, \( k \) is the kernel size, and \( d(l) \) is the dilation rate at layer \( l \). This means that as the depth of the network increase, so does the receptive field. The dilated convolution of \( F \) on element \( s \) of a sequence \( X \) is given as:

\[
F(s) = (X *_{d} f)(s) = \sum_{i=0}^{k-1} f(i) \cdot x_{s-d\cdot i},
\]

where \( X \in \mathbb{R}^{n} \) is a 1-D input sequence, \( *_{d} \) is dilated convolution operator, \( f : \{0, \ldots, k-1\} \in \mathbb{R} \) is a kernel of size \( k \) and \( d \) is the dilation rate \([14, 35]\). For applications requiring a very large \( rf \), it is also essential to provide stability in the later layers subject to the vanishing gradient problem. A popular technique in traditional CNN architectures, the residual block \([36]\), provides a “highway” free of any gated functions, allowing information to flow from the early layers to the last layers unhindered. These connections can be seen in the final GTCN architecture shown in Fig. 5.

The GTCN consists of \( L \) hidden layer and an optional linear layer to map the input size \( i \) to arbitrary output size. In order to increase the capacity of the network to absorb more features from its input, each hidden layer of GTCN has two regular convolutions and two ReLU activation functions. There can also be an upsampling unit, such as point-wise convolution, in the first hidden layer of GTCN to map 1-D input sequence to a higher dimension to guarantee the element-wise addition receives tensor of the same dimension.

4 ATCN: Agile Temporal Convolutional Networks

In this section, we introduce the architecture of ATCN. At first, we discuss the essential components, and then we elaborate on the hyper-parameters, and in the end, we present the ATCN architecture and its model builder.

4.1 Network Structure

At the core, the architecture of ATCN is a chain of Spectral-Temporal Convolution Blocks (STCB). Each STCB is composed of a pointwise (expansion), a group, and a pointwise (projection) convolution. We visualized the STCB in Fig. 4(a). The MaxPooling layers are optional. It lets architects downsample temporal information to minimize computational complexity while embedding that information in higher or lower dimensions. The extreme case of STCB is when the group size and its input channel size are equal. In this case, the group-convolution is set to depthwise, and the ATCN network synthesizer will remove the maximum pooling and add a skip-line between element-wise addition and the STCB input. The final architecture of ATCN is shown in Fig. 4(b). The ATCN is a mirrored residual dilated convolutional neural network. It starts with mapping the \( n \)-dimensional input, which is generally 1-D for the time series, to a higher dimension at the first layer. Then, it encodes the data to lower dimensions. At decoder part, the data will be decoded to a higher dimension again. Based on the final application, the output of the decoder
can be used for regression or classification problems. In the rest, we discuss the details of STCB and the network hyper-parameters.

The first layer of ATCN is standard convolution with an optional MaxPooling for downsampling the input. A padding unit is also added before standard convolution and expansion convolution in STCB to ensure that the input and output tensors of the block have the same size to satisfy principle number 2 of GTCN. The 2p zeros are added symmetrically by padding unit, where p is given by:

$$ p = \left\lceil \frac{(o - 1) \times s + (k - 1) \times (d - 1) - i + k}{2} \right\rceil, $$

where $o$ is the output size, $i$ is the input size, $s$ is the stride, $k$ is the kernel, and $d$ is the dilation. After each convolution, 1D batch normalization and a non-linear activation function is also added. In this paper, we used Swish by padding unit, where $f$ is given by:

$$ Swish(X) = X \odot Sigmoid(X), $$

where $\odot$ is Hadamard or element-wise multiplication. Fig. 5(a) shows how different activation functions perform on the validation loss of the MNIST digits classification problem. It should be noted that based on the complexity of the application and available memory and hardware computational power, the activation function of ATCN can be changed.

The STCB consists of expansion, followed by a group and another projection convolution. The task of expansion convolution is to map input channel size, $c_{in}$, to higher or same dimension, $c_{exp}$, where $c_{exp} = \alpha \times c_{in}, \alpha \geq 1$. On the contrary, pointwise projection embeds and maps the feature extracted from the group convolution to the block output size, $c_{out}$. For the case of depthwise convolution, we set group, which manages the connection between input and output, to $c_{exp}$. For this case, the convolution weight shape changes from $(c_{out}, c_{in}, k)$ to $(c_{out}, 1, k)$, where $k$ is the kernel size. We designed the network synthesizer so that if $c_{in} = c_{out}$, the skip line is automatically created from input to the elementwise addition. Then, the input will be added to the residual output from the pointwise
The residual connection helps the designers increase the network’s depth without being worried about the vanishing gradient problem. The model synthesizer considers group convolution rather than depthwise for the case that MaxPooling is selected. The reason for doing so is based on this observation that for downsampling the input, which has an activated max-pooling unit, group convolution helps to better map temporal information to a higher dimension without drastically increasing computation complexity and the model size. The only constraint imposed by group convolution is that its output channel size, \( c_{\text{out}}^{\text{gc}} \), should be divisible by \( c_{\text{out}}^{\text{exp}} \). The two extreme G-CNN cases are when \( \text{group} = c_{\text{in}}^{\text{gc}} \) and \( \text{group} = 1 \). In the former case, the group convolution is a depthwise convolution, and in the latter, it is a standard convolution. Formally, the weight shape for group convolution is \((c_{\text{out}}, c_{\text{in}}^{\text{group}}, k)\). We depict the effect of altering the \( \text{group} \) values in Fig. 5(b) for MNIST digit classification. As we can see, reducing the \( \text{group} \) value increases the network capacity to minimize the validation loss.

![Effect of different non-linearity activation function on validation loss.](image)

![Dilated Causal Convolution.](image)

Figure 5: The effect of different non-linearity activation function, \( \sigma \), and \( \text{group} \) value on final validation loss.

4.2 The Receptive Field of an ATCN

To maintain the receptive field of an ATCN network at different network depths, two knobs must be adjusted: 1) kernel size, and 2) dilation rate. We elaborate on each of them in detail in the rest of the article.

4.2.1 Dilation rate

For a fixed input size, if we increase the number of layers, based on the GTCN architecture guideline, we need to increase the dilation rate exponentially. This decision will help the network have a higher receptive field; however, based on principle number 2, we need to pad the features excessively to have the same input and output size. This unnecessary padding results in 1) more computation and 2) CNN performance degradation. We observed linear growth for dilation would help the network with more than six layers to have better feature representation. Although the dilation rate can be defined as a function of layer number, we increased it after each block with activated downsampling in the experimental results. This decision helps design a deep ATCN for the cases where input size, \( i \), is small.

4.2.2 Kernel size

It is recommended that the kernel size, \( k \), is large enough to encompass enough feature context based on the problem complexity. However, based on Eq. 3, it is a good practice to decrease the kernel size for higher layers to ensure \( p \) is not growing exponentially. By contrast, if we increase the dilation rate, based on Eq. 1 the kernel size can be reduced without concern for the receptive field. Embedded devices gain two crucial advantages from this decision: it reduces 1) the computational complexity and 2) the model size.

Similar to the dilation rate, if we need to increase the network’s depth to enhance its capacity, it is recommended to gradually decrease kernel size and have a linear growth for dilation. We can alter both after each block with downsampling units. This decision helps the final structure to have enough receptive field to cover feature context without increasing the MAC operations and model sizes.
4.3 ATCN Model Synthesizer

We depict the inputs of ATCN Model Synthesizer and the framework for its training in Fig. 6. The ATCN Model Synthesizer receives Output Channels, Kernel Sizes, Dilation Rates, Input Ratios, and finally, the first Input Channel Size to design the ATCN network architecture. The model synthesizer automatically configures the STCBs and sequences them to generate the final network model based on the ATCN configurations, such as kernel size, and dilation rate. The model will be trained based on the provided dataset and training hyperparameters, such as learning rate and weight decay. Compression algorithms such as online quantization and pruning are orthogonal to ATCN models. Therefore, the training phase of the synthesizer can be expanded to compress the model online or offline after the training phase. The trained ATCN model can be exported as Open Neural Network Exchange (ONNX) so it can be deployed on embedded edge devices. The trained model cannot be reconfigured during the run-time as the training phase is required again to fine-tune the revised model. Ultimately, the agility of ATCN comes from the model synthesizer, which can quickly generate the ATCN model and configure the training framework to shrink design time. In the rest, we explain each of the ATCN Model Synthesizer inputs in detail.

4.3.1 Output Channels

: It is a vector of size \( L \), where \( L \) is the number of layers (blocks). The \( c_{\text{out}}^l \) defined in \( C_{\text{out}} = [c_{\text{out}}^1, c_{\text{out}}^2, \ldots, c_{\text{out}}^L] \), decides the output channel for layer \( l \). For this research, the values in vector \( C_{\text{out}} \) are descending-ascending (Auto-Encoder architecture) to code the feature to lower dimension to extract temporal correlation and then maps to a higher dimension to represent extracted features for final stages.

4.3.2 Kernel Size

: The vector \( K, K = [k^1, k^2, \ldots, k^L] | k^l \in \mathbb{N} \), defines the kernel sizes for each layer. Based on the discussion of Section 4.2.2, it is suited to decrease the \( k \) to minimize both model size and required computational complexity.

4.3.3 Dilation Rates

: The vector \( D, D = [d^1, d^2, \ldots, d^L] | d^l \in \mathbb{N} \), defines the dilation rates per each layer. On the contrary to \( K \), it is necessary to increase \( d \) to achieve a higher or same receptive field at deeper levels.

4.3.4 Input Size Ratios

: The \( R = [r^1, r^2, \ldots, r^L] \mid 0 < r^l \leq 1 \), defines the input ratios. For the value of \( r^l < 1, l > 1 \), the ATCN Model Synthesizer configures the STCB block with max-pooling unit. For the case of \( l = 1, r < 1 \), the max-pooling will be added after standard convolution; otherwise, the input and out of standard convolution will have the same size. For this research, the \( r^l \) can only be defined as \( \frac{1}{2} \) or 1. For other ratios, the synthesizer can be modified to change the stride of max-pooling to satisfy the targeted ratio.

Figure 6: ATCN model synthesizer and training framework.
4.4 ATCN Families

We introduce two ATCN families by assigning values to the $C$, $K$, $D$, and $R$ for UCR time series classification. Table 1 summarizes the configuration of T0 and T1 as two candidates. We assign the output channels, $C_{out}$, in descending-ascending format to encode features to lower dimensions, then decode them to higher dimensions to represent them for the final dense layers and classifier. We have reduced the kernel size $K$ due to the increased dilation rate, $D$. As a result, MACs and model parameters are reduced without compromising receptive field size. The values assigned in Table 1 per each hyperparameter of the $C$, $K$, $D$, and $R$ are considered based on input characteristics of UCR 2018 benchmarks and the resources available on targeted hardware platforms. Therefore, they can be fitted in hardware memory and executed based on available computation power while having a comparable accuracy in respect to SotA time series classifiers. Based on the hyperparameter trade-off explained in Section 4.2, the designer can explicitly increase the network capacity and define the ATCN models as server-class solutions. Table 2 compares the average FLOPS and number of model parameters of candidates and InceptionTime based on seventy benchmarks from the 2018 UCR time series classification, which are explained in detail in Section 5. We were not able to calculate the MACs and FLOPS of MiniRocket with the aid of standard libraries due to the non-deep learning characteristics of MiniRocket. The T0 configuration reduces the MACs and model size by 102.38× and 16.84× over IT, respectively. T1 has also 73.59× reduction in MACs, and a 14.23× reduction in model size over IT. The algorithmic accuracy of these models and training methods of these models are explained in Section 5.

| Models | Configurations |
|--------|----------------|
| $C_{out}$ | $D$ | $K$ | $R$ |
| T0 | [32, 16, 16, 8, 8, 16, 16, 32] | [1, 2, 2, 4, 4, 6, 6, 8] | [32, 16, 16, 8, 8, 4, 4, 2] | [1 2, 1 1, 1 1, 1 1, 1 1] |
| T1 | [32, 16, 16, 8, 8, 16, 16, 32] | [1, 2, 2, 4, 4, 6, 6, 8] | [64, 32, 32, 16, 16, 8, 8, 4] | [1 2, 1 1, 1 1, 1 1, 1 1] |

Table 2: FLOPS and number of parameters for T0, T1, and InceptionTime.

| Metric | Models |
|--------|--------|
| FLOPs  | T0     | T1     | InceptionTime |
|        | 2,377,840 | 3,329,008 | 240,430,566 |
| Params#| 24,816   | 29,424   | 422,498      |

5 Experimental Results

In this section, we demonstrate the capabilities of two different ATCN families by applying them to problems of UCR time series classification. T0 and T1 are compiled and utilized on both ARM Cortex-M7 microcontroller and Cortex-A57 microprocessor. A report on RAM utilization, flash usage, and inference time is also provided. In following Demvsar's recommendation [37], we used an open-source tool [38] to repeat the comparison setup explained in [39] to practice the Friedman test [39] and use Wilcoxon signed-rank test [40] with Holm’s alpha (5%) correction [41] to compare the accuracy and latency of each model among the benchmarks for Fig. 8 and Fig. 9. We reported Top-1 accuracy as the final model accuracy and the latency is the combined delay between an input and its classification output when the batch size is one.

5.1 Dataset

The experiments were conducted on 70 benchmarks [3] publicly available from UCR Time Series Classification 2018, which vary in time length, number of classes, dataset type, and sample size. As our article focuses on embedded devices, we chose benchmarks based on the fact that they are typically observed on edge devices. Therefore, we selected benchmarks whose types are image, spectrum, ECG, or sensors while covering a wide range of input lengths and the number of classes.

Available at: https://github.com/hfawaz/cd-diagram
A list of the benchmarks are mentioned in Appendix A and will also be available online for the sake of reproducibility.
5.1.1 Data augmentation

For benchmarks whose training size is small, such as ECGFiveDays, we applied four types of data augmentation: jittering [42], magnitude warping [43], window warping [44], and scaling. In Fig. 7 each approach is shown in relation to the observed signal, $X$.

![Data augmentation diagrams](image)

(a) Jittering  
(b) Magnitude Warping  
(c) Window Wraping  
(d) Scaling

Figure 7: Different data augmentation applied on UCR dataset. $X$ is observed signal and $\hat{X}$ is the augmented data.

5.2 Implementation details

The models are implemented in PyTorch and trained on an Nvidia Tesla V100 GPU using the ADAM optimizer with a Learning Rate (LR) of 0.001, a gradient clip of 0.25, and a weight decay of 0.001. We also reduce the LR by the factor of 0.1 when the validation loss stagnates for eight epochs. In the case of datasets with two classes, Binary Cross-Entropy (BCE) loss function is used, and Cross-Entropy is used for all other datasets.

5.3 Execution Comparison

In order to evaluate the performance of models on bare-metal embedded devices, we selected STM32F746ZGT6, which has Cortex-M7 running at 216 MHz with 320 KB of RAM and 1 MB of flash memory as a microcontroller. The networks have been compiled and 8-bit quantized with the aid of network compiler provided by STM32CubeIDE. Our goal was to run the models on M7 without any support for Real-Time Operating Systems (RTOS) and memory management. We compared the execution performance and hardware utilization of all four classifiers in Table 3. The 8-bit quantized InceptionTime model could not be executed due to its higher RAM and flash requirements. Furthermore, we cannot use standard Cortex-M7 compiler tools to map MiniRocket to the microcontroller as it relies on Numba as a high-performance Just-In-Time (JIT) Python compiler and Thread Building Block (TBB) library. The results are extracted by a running model trained on Coffee benchmark. Compared to the T1 configuration, the T0 can reduce both RAM and flash utilization by 7.5% and 1.47%, respectively, while improving inference time by 21.42%. As a result of the low memory and computational resources requirements, ATCN models were the only ones capable of running on tiny microcontrollers.

For Cortex-A57, we have Ubuntu 18.04 set up as the operating system with 4GB RAM and 64GB flash memory. In addition, we used onnxruntime 1.4.0 to run ATCN ONNXes for all seventy benchmarks. The CPU is set as the execution engine for the onnxruntime module. To run MiniRocket on A57 processors, we compiled LLVM 10.0.1 and oneAPI TBB 2021.4 for the Aarch64 architecture since MiniRocket relies on the Numba JIT Python compiler. We resampled the latency 100 times per benchmark and skipped the first 5 iterations as a warm-up, and the averaged latency of over 95 iterations was considered. According to Fig. 8 T0 ranked first because it outperformed T1 and MiniRocket in all seventy benchmarks.
select the Pareto points for the sake of clarity. To demonstrate how the three models can provide optimal implementations, we modified based on application requirements. Fig. 10 illustrates the final 4 solutions and we have not shown all 144 results, we calculated the Pareto front with the constraint that accuracy must be at least 55%. This constraint can be higher than T0, and T1 in both FLOPS and model size metrics. To ensure each model generates meaningful models. InceptionTime is ignored in this section since its accuracy is less than MiniRocket and its model complexity.

In this section, we draw the accuracy-latency Pareto front based on the performance of T0, T1, and MiniRocket

| Description                  | Models        |
|------------------------------|---------------|
| M7 Ram utilization (%)       | T0  | T1   | MiniRock | InceptionTime |
| 48.89                        | 56.39 | -    | -        |
| M7 Flash utilization (%)     | 14.13 | 15.89 | -        | -            |
| M7 inference time (ms)       | 165   | 210  | -        | -            |

Figure 8: Mean rank of T0 and T1 in terms of latency against MiniRocket over 100 resamplings of running seventy benchmarks from UCR 2018 on Cortex-A57. T0 outperformed the other two models and ranked first in all seventy benchmarks.

5.4 Algorithmic Comparison

In Fig. 9 we show the critical difference diagram of discussed classifiers. The connected classifiers by a thick line indicate that they do not have a significant difference statistically based on the Friedman test. In terms of accuracy, MiniRocket outperforms T0, T1, and InceptionTime; however, it shows similar performance to InceptionTime and T1 statistically. Likewise, T0, T1, and InceptionTime have similar performance. Fig. 9 also indicates that T0 and T1 have similar or better accuracy than MiniRocket for some of the benchmarks as the MiniRocket does not outperform these models in all seventy benchmarks. Since T0 and T1 have a lower latency, we need to extract the Pareto optimal designs to have efficient models in terms of latency and accuracy.

Figure 9: Mean rank of T0, T1, InceptionTime, and MiniRocket. The diagram represents the overall average ranking of the classifiers, with a thick horizontal line indicating a group of classifiers that are not significantly different from each other in terms of accuracy. Consequently, T1, InceptionTime, and MiniRocket are not significantly different.

5.5 Pareto solutions

In this section, we draw the accuracy-latency Pareto front based on the performance of T0, T1, and MiniRocket models. InceptionTime is ignored in this section since its accuracy is less than MiniRocket and its model complexity is higher than T0, and T1 in both FLOPS and model size metrics. To ensure each model generates meaningful results, we calculated the Pareto front with the constraint that accuracy must be at least 55%. This constraint can be modified based on application requirements. Fig. 10 illustrates the final 4 solutions and we have not shown all 144 Pareto points for the sake of clarity. To demonstrate how the three models can provide optimal implementations, we select the DodgerLoopDay benchmark. We can see how three models can generate three different solutions for the DodgerLoopDay based on distinct accuracies and latencies. Table 4 summerizes the contribution of each model to provide the overall 144 optimal points. When a model provides equivalent or higher accuracy and less latency than all other models, we assign it to the Unique set. Those solutions provided by a model that meet the defined constraints and are part of the Pareto front make up the Total set of the model. On 144 Pareto solutions, T0 contributed 66 points, and it outperformed T1, and MiniRocket in 15 benchmarks. Fig. 10 shows Lightning2, Ham, and ECGFiveDays, which were selected from T0 unique solutions. As we can see, for all T0 selected unique solutions, not only does T0 have better accuracy than MiniRocket and T1, but it is also faster. While T1 and MiniRocket each contribute 39 points, MiniRocket managed to beat T0 and T1 for two benchmarks named RefrigerationDevices and EOGVerticalSignal. Due to T0 and T1 accuracy being less than 55% for both benchmarks, the T0 and T1 solutions were omitted.
Figure 10: The accuracy-latency Pareto front of four sample benchmarks for three models, T0 (+), T1 (▼), and MiniRocket (×). Three examples of T0 unique solutions include Lightning2, Ham, and ECGFiveDays. As can be seen, T0 produces results with higher or equal accuracy while its latency is lower than the other two models. As a result, T1 and MiniRockets do not fall under Pareto solutions. The DodgerLoopDay benchmark is also used as an example where all three models have Pareto solutions.

Table 4: The performance of three T0, T1 and MiniRocket in contribution of 144 Pareto solutions.

| Description | Models |
|-------------|--------|
|             | T0     | T1     | MiniRocket |
| Contribution| Total Unique | Total Unique | Total Unique |
| 66          | 15     | 39     | 0          | 39 | 2 |

5.6 Architectural configuration study

In this section, we examine the effects of altering the kernel and channel sizes. In order to accomplish this, the ATCN model $T_β$ is defined as having a channel size that is twice as large as T1 per layer, however, the kernel size is half the size. Due to this configuration, $T_β$ has greater model complexity than T1, both in terms of FLOPS and model size, while still achieving the same accuracy. Table 5 summarizes the $T_β$ network configuration, FLOPs, and the number of parameters. It can be seen that $T_β$ has the same $D$, and $R$ as T1, but $C_{out}^{β} = 2 \times C_{out}^{T1}$ and the kernel size per block is half. Despite a greater model complexity than T1, both FLOPs and model size, the results depicted in Fig. 11 show that overall T1 and $T_β$ achieve very similar accuracy. As an aid to understanding this behavior, we depict the inputs and Class Activation Mapping (CAM) [45] of two benchmarks in Fig. 12 and Fig. 13. When the model correctly classified the input signal, CAMs are calculated by multiplying the input of global average pooling by the weight matrices of the correct class index.

Table 5: Model configuration and accuracy performance of $T_β$

| Model | Parameters |
|-------|------------|
|       | $C_{out}$ | $D$  | $K$  | $R$  | FLOPs | Params# |
| $T_β$ | [64, 32, 16, 16, 32, 32, 64] | [1, 2, 2, 4, 4, 6, 6, 8] | [32, 16, 16, 8, 8, 4, 4, 2] | [1.5, 1.1, 1.1, 1.1, 1.1] | 7,303,136 | 86,240 |

The activation heatmaps for class 0, shown in Fig. 12, have the lowest value around the input signal magnitude. Consequently, for class 0, the probability of output approaches zero. However, we can observe the activation heatmaps
Figure 11: Pairwise accuracy of T1 versus $T_\beta$.

Figure 12: GunPointOldVersusYoung dataset

for class 1 have the highest value around the signal magnitude, which leads to the output probability being one. For multiclass classification problems depicted in Fig. [13] we can see models activate based on the perceived nuances of signal shapes. For instance, the T0 model, Fig. [13(a)], classifies the input as class 0 based on the form observed in sequence $\sim$10 to $\sim$80, as class 1 based on unique transition observed in the middle of the sequence, and as class 2 based on the curve recognized in $\sim$70 to $\sim$150. In respect to $T_\beta$, this model shows a coarse-grained transition, note sequence $\sim$20 to $\sim$60 in Fig. [12(f)] and $\sim$150 to $\sim$240 in Fig. [13(g)]. This indicates that $T_\beta$ has a lower receptive field compared to T1. As a result of the higher receptive field of T1, the model is able to predict the classes more precisely, although it has less model complexity in both forms of FLOPS and the number of parameters.

6 Conclusion

This article proposed ATCN which is a novel family of networks for real-time processing of time-series on embedded and edge devices. In order to reduce the number of MAC operations and model size, we introduced STCB as a main computational block. STCB blocks are able to be sequenced in a variety of configurations to build scalable ATCNs. We also presented a framework, called ATCN Model Synthesizer, to build different ATCN models. The result of ATCN Model Synthesizer is a family of compact networks with formalized hyper-parameters that allow the model architecture to be configurable and adjusted based on the application requirements. Through the use of model
synthesizer and ATCN reconfigurability, we have developed two fast while accurate models, T0, T1 which can be executed on ARM Cortex-M7 microcontrollers. The experimental results over 70 benchmarks of 2018 UCR time classification dataset indicate that the T0 configuration can reduce the MACs and model size by 102.38× and 16.84× over InceptionTime, respectively. T1 also has a 73.59× reduction in MACs, and a 14.23× reduction in model size over InceptionTime. In addition, we compared the performance of T0 and T1 against MiniRocket as a benchmark for a fast and accurate non-deep learning time series classifier. According to our results, the T0 model outperforms MiniRocket across 15 benchmarks and provides 66 optimal solutions out of 144 Pareto points, while MiniRocket only contributes 39 points.

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A Bar graph Comparison of Models

Fig. 14 compares the accuracy and latency of the T0, T1, and MiniRocket models across all seventy benchmarks. As explained in Section 5, latency values are obtained by running benchmarks on Cortex-A57. In Fig. 14 we sorted the results based on T0 latency.

Figure 14: Comparison of accuracy and latency of three models on a Cortex-A57 processor. Results are sorted by T0 latency.