MC²RAM: Markov Chain Monte Carlo Sampling in SRAM for Fast Bayesian Inference

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Abstract—This work discusses the implementation of Markov Chain Monte Carlo (MCMC) sampling from an arbitrary Gaussian mixture model (GMM) within SRAM. We show a novel architecture of SRAM by embedding it with random number generators (RNGs), digital-to-analog converters (DACs), and analog-to-digital converters (ADCs) so that SRAM arrays can be used for high performance Metropolis-Hastings (MH) algorithm-based MCMC sampling. Most of the expensive computations are performed within the SRAM and can be parallelized for high speed sampling. Our iterative compute flow minimizes data movement during sampling. We characterize power-performance trade-off of our design by simulating on 45 nm CMOS technology. For a two-dimensional, two mixture GMM, the implementation consumes $\sim 91 \mu W$ power per sampling iteration and produces 500 samples in 2000 clock cycles on an average at 1 GHz clock frequency. Our study highlights interesting insights on how low-level hardware non-idealities can affect high-level sampling characteristics, and recommends ways to optimally operate SRAM within area/power constraints for high performance sampling.

Index Terms—Inference; in-memory computing; Markov chain Monte Carlo (MCMC) sampling.

I. INTRODUCTION

Markov chain Monte Carlo (MCMC) is an extensively used statistical sampling technique for generating samples from high-dimensional probability density functions even when these functions can not be defined analytically [1], [2]. Especially, in recent years, as various machine learning (ML) platforms are proliferating for real-time decision-making, MCMC is being combined with Bayesian ML models to perform efficient inference [3], [4]. Unlike classical inference, Bayesian inference can capture uncertainties in the outcomes for risk-aware decision making [5] as shown in Fig. 1. Moreover, there is a growing interest to operate ML-based prediction models at the edge itself [6], [7]. A low power/area MCMC platform is, therefore, becoming imperative along with low power ML implementation.

Prior works have discussed low power MCMC implementations using FPGAs, and have achieved an accuracy similar to their software counterparts, while being more energy-efficient. An FPGA-based hardware accelerator [8] was designed for variational inference of Bayesian neural networks (BNNs). Conversely, in this work, we present MC²RAM – a customized implementation of MCMC within SRAM where we co-locate and co-optimize functional units, control flow, and data flow to address critical bottlenecks in high-speed MCMC-based sampling. Our compute flow exploits the Markov chain property where successive chain outputs lie in the proximity minimizing the necessary computing load in each iteration. While MCMC in prior works [8], [9] is limited to Gaussian functions, MC²RAM expands this to Gaussian mixture models (GMMs). A GMM can model any density arbitrarily closely with enough mixture components, making our implementation vastly more applicable. We develop interesting insights about the interaction between low-level hardware non-idealities and high-level sampling characteristics in MC²RAM. Our detailed design and operating power space exploration can lead to efficient design methodologies for SRAM-based sampling.

The paper is organized as follows. Section II discusses the background on MCMC and provides an overview of MC²RAM. Section III discusses density function computation and sampling in MC²RAM. Section IV discusses the results and implications of various sources of non-idealities in MC²RAM on sampling. Section V concludes this paper.

II. MCMC FOR BI AND PROPOSED MC²RAM

In ML models and methods that employ Bayesian inference (BI), the expectation of the predicted outcome (or other quantity of interest) is obtained by solving $\int M(I,w) \times P(w|D)dw$, where $M(I,w)$ is the model (say, a neural network) with the input $I$ and parameters/weights $w$, and $P(w|D)$ is the posterior density of weights given training data $D$. In such computations, an analytical integration is often intractable since the density function of the random variable (RV) and/or the function to be integrated, e.g., $P(w|D)$ and $M(I,w)$ in BI, are too complicated. A Monte Carlo approach, therefore, becomes necessary to numerically compute these quantities. Monte Carlo approach reduces an integral over a function of RV, $x$, as

\[ \int f(x)dx \approx \frac{1}{N} \sum_{i=1}^{N} f(x_i) \]

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\[
\int G(x) \times F(x) dx \approx \frac{1}{T} \times \sum_{t=1}^{T} G(x, F(x_t))
\] (1)

Here, \( G(x) \) is the function to be integrated, \( F(x) \) is the density function of \( x \), and \( x_t, F(x_t) \) is an independent and identically distributed (i.i.d.) sample drawn from \( F(x) \). The law of large numbers guarantees an asymptotic convergence of the summation to the exact integral as the number of samples \( T \) increases. In BI, \( F(x) \) is the posterior density \( P(w|D) \), which can be numerically extracted using the Bayesian formula \( P(w|D) \propto P(D|w) \times P(w) \), but cannot always be defined analytically. Therefore, MCMC overcomes this critical problem by defining an ergodic Markov chain. Among the MCMC methods for sampling we choose Metropolis-Hastings (MH) sampling \( \square \) that provides a middle ground in terms of acceptance/rejection complexity of the samples and the average time needed to generate a candidate sample. The algorithmic steps for MH-based MCMC are demonstrated in Fig. 2. A candidate sample at step \( t \), \( x_t^{\text{cand}} \), is determined from the previously accepted sample \( x_{t-1} \) and a randomly generated sample, \( R \), as \( x_t^{\text{cand}} = R + x_{t-1} \); here, \( R \) follows the statistics of the proposal distribution \( P \) (e.g., Uniform or Gaussian) typically centered at zero. The statistics of \( R \) controls the search radius and sample search behavior in MCMC. The candidate sample is accepted when the ratio of the density of \( x_t^{\text{cand}} \) to that of \( x_t-1 \), i.e., \( F(x_t^{\text{cand}})/F(x_{t-1}) \), is greater than a random threshold, \( U \), which is generated uniformly between zero and one.

Fig. 3 shows the overall architecture of MC \(^2 \)RAM. An SRAM array stores the GMM parameters for the density function of the RV, i.e., mean, variance, and mixture weights \( \mu, \sigma, \text{and } p \). Since the dimension of the sampling density can be high, \( \mu, \sigma, \text{and } p \) vectors are stored appropriately in multiple SRAM banks as shown in the figure. SRAM arrays are also integrated with random number generators (RNG). Using RNGs and a previous sample of the chain \( x_{t-1} \), a candidate sample \( x_t^{\text{cand}} \) is generated within the SRAM. For \( x_t^{\text{cand}} \), SRAM arrays partially compute the density of the candidate sample, i.e., \( F(x_t^{\text{cand}}) \), in parallel by following single instruction multiple data (SIMD) style execution. Central processing layer receives the partial terms for density computation from SRAM arrays and applies Metropolis-Hastings-based sample acceptance criteria to accept/reject \( x_t^{\text{cand}} \). Using the accepted \( x_t \), the chain iterates to find the next sample \( x_{t+1} \).

The key complexities of MCMC illustrated via Fig. 2 are: (i) computations of \( F(x_t^{\text{cand}}) \) for a candidate sample \( x_t^{\text{cand}} \) since the dimension of \( x_t^{\text{cand}} \) can be high and/or density function

III. IN-SRAM DENSITY COMPUTATION AND SAMPLING

The density of a GMM, \( F(x_t) \), for a candidate sample \( x_t^{\text{cand}} \) is given by

\[
F(x_t^{\text{cand}}) = \sum_{j=1}^{M} p_j \times N(x_t^{\text{cand}}; \mu_j, \sigma_j)
\] (2)

where each Gaussian mixture component is approximated by its mean and covariance, \( \mu_j, \sigma_j \), and \( p_j \) is the mixture weight. In approximating a density function \( F(x) \) using GMM, mixture Gaussians with only diagonal covariance can be used (this is called as mean-field approximation \( \square \)). The density of \( N(x_t^{\text{cand}}, \mu_j, \sigma_j) \) depends on its exponent \( E_j \) as

\[
E_j = \sum_{i=1}^{N} \left( \frac{x_t^{\text{cand}} - \mu_{ij}}{\sigma_{ij}} \right)^2
\] (3)

Here, \( x_t^{\text{cand}}, \mu_j, \text{and } 1/\sigma_{ij} \) are each \( N \)-dimensional and expanded using the subscript \( i \) as in the above equation. The overall GMM density in log-domain can be computed from the exponents \( E_j \) using the identity \( \ln(e^a + e^b) = a + \ln(1 + e^{e^b-a}) \) and a look up table (LUT) for \( \ln(1+e^x) \). The density of \( N(x_t^{\text{cand}}, \mu_j, \sigma_j) \) can be further simplified by exploiting the sampling property of the MCMC sample \( x_{t-1} \). Thus, \( E_j(t) \) at \( x_t^{\text{cand}} \) can be computed from \( E_j(t-1) \) at \( x_{t-1} \) by

\[
E_j(t) = E_j(t-1) + \left( \frac{R}{\sigma_j} \cdot R \right) + 2 \cdot \left( \frac{R}{\sigma_j^2} \right) \cdot (x_{t-1} - \mu_j)
\] (4)

Here, \( R \) is a generated random number from the proposal distribution \( P \) within SRAM, which is used to search the next MCMC sample. \( R/\sigma_j^2 \) is an \( N \)-dimensional vector obtained by dividing each element of \( R, \sigma_j \), with the corresponding \( \sigma_{ij}^2 \). We apply SRAM to compute scalar products \( R \cdot \sigma_j \) and \((x_{t-1} - \mu_j) \cdot R/\sigma_j^2 \) within SRAM array to evaluate (4). For the scalar product of two vectors \( V \) and \( W \), i.e., \( V \cdot W \), \( W \) is stored in the 8-T SRAM cell-array and \( V \) is copied to
the DAC-operand buffer shown in Fig. 5. An 8-T SRAM cell is shown in Fig. 4(a) which has an additional scalar product port as shown in red in the figure. SRAM columns store \( W \) in \( n \)-columns with \( n \)-bit precision. Digital-to-analog converter (DAC) converts the input \( V \) into corresponding analog-mode current vector \( I_c \) and applies to the product word line \( W/L_p \) of the cells. The basic approach for the scalar product is to use memory cells as current-mode AND gate. If an SRAM cell \( j \) stores bit ‘1’, it allows the row DAC current \( I_c \) to flow to its bit-line \( B_{L_j} \). The currents from each active cell in the column add up and follow \( V.W \) as shown in Fig. 4(c). The column multiplexer selects only one column at a time and the selected column-current will be read by an analog-to-digital converter (ADC) as shown in Fig. 4(d) and (e) that converts column current to digital bits representing \( V.W_i \), where \( W_i \) is the \( i \)th precision binary vector of \( W \). The column current is passed to an OP-AMP with a resistive feedback to convert the column current to corresponding analog voltage. The resistance value, \( R \), is designed to match the operating range of ADC. OP-AMP in Fig. 4(d) serves two purposes. It stabilizes the potential of the tail-end of the column, and it also biases the column tail potential to zero. The hold cell in Fig. 4(d) samples the output potential of OP-AMP and retains it after the OP-AMP is disconnected and bias-current of row DACs is turned off to save biasing power. The current of all \( n \)-columns are converted using ADC and combined with digital scaling to compute \( V.W \). We use two-step flash ADCs [13], [14] that optimally balances area/power constraints without incurring excessive delay.

For the proposed implementation in 45nm CMOS, Fig. 6(a) shows HSPICE simulation for the scalar product using 32-row SRAM cell array matching the ideal. The current-mode processing in the proposed design gives significant advantages. The SRAM cells either act as current buffers or block the input current so that the variability in SRAM cell transistors has minimal impact to the accuracy of scalar product that posed challenge in [15]. Also, the \( V_{TH} \) variability of cell transistors does not affect the scalar product when DAC reference currents are sufficiently higher than SRAM leakage. Fig. 6(b-c) illustrate the variability analyses on the operation of SRAM. In Fig. 6(b), the column current follows a Log-Normal distribution when considering process variability due to SRAM transistors. In Fig. 6(c), with \( \sigma(V_{TH}) = 30 \text{ mV} \) (black curve), the variation in column current is 1.43 (normalized against mean) that corresponds to the DAC reference current of 5 nA. Upon increasing the DAC current, the variability of column current reduces when normalized against the mean value.

DAC in Fig. 4(b) displays two critical non-idealities that affect the scalar product accuracy: (i) Channel length modulation (CLM) in the mirroring transistors that affects the scalar product accuracy posing dependence to \( W/L_p \) potential and (ii) non-ideal mirroring ratio due to process variability. We address CLM-induced precision degradation by reducing the turn-ON voltage of select switches in DAC to limit source-to-drain voltage of mirroring transistors, which improves the accuracy as shown in Fig. 4(d). To minimize process variability-induced non-ideal mirroring ratio in DAC, a set of calibrating transistors with small width \( W_c \) relative to mirroring transistors are added to DAC in Fig. 4(b). DAC mirror current is read against a reference to add \( W_c \) until the current meets the desired level.

In MC²RAM, storage of density function (\( F(x) \)) parameters and sample generation \( R \) is collocated within the same array by integrating RNG cells with SRAM cells. Since in a high-dimensional weight space many \( R \) end up being rejected, colocating the operations with the same SRAM array minimizes overheads and data movement. Fig. 4(f) shows the RNG cell based on cross-coupled inverters [16]. The differential ends \( Q \) and \( Q_B \) are pre-charged to \( V_{DD} \) when \( CLK = 0 \). When \( CLK = 1 \), the thermal noise resolves the meta-stability to generate a random bit. The random bits, stored in DAC operand buffer, can further be scaled with \( \sigma^2 \) within DAC as shown in Fig. 4(g). The scaled \( R/\sigma^2 \) is used for density...
Fig. 6: (a) $V.W$ scalar product simulated in 45nm CMOS for density computation. (b) Effect of $V_{TH}$ variability in MC$^2$SRAM transistors to scalar product current ($\sigma(V_{TH}) = 30$ mV). (c) Current variability in MC$^2$SRAM controlled by DAC. (d) Effect of CLM in mirror transistors of DAC on scalar product accuracy. (e) Contribution of MC$^2$RAM peripherals to power consumption per sampling iteration.

Fig. 7: (a) Sampling distribution with 8-bit precision DAC, 6-bit precision ADC, VDD = 1V and mean distance = 1. (b) Sampling distribution with mean distance = 5. (c) KL divergence between ground truth (contour) and sampled distribution with sweeps performed on ADC bits-precision, DAC bits-precision and mean distance between GMM components. (d) KL divergence over a range of GMM dimensions.

computation based on (4).

IV. RESULTS AND DISCUSSIONS ON SAMPLING

We analyze simulated distribution with respect to the ground truth using scatter plots and KL divergence [17]. The KL divergence between two discrete probability density functions $\mathcal{F}(x)$ and $\mathcal{G}(x)$ is measured as

$$D_{KL}(\mathcal{F}||\mathcal{G}) = \sum_x \mathcal{F}(x) \log \left( \frac{\mathcal{F}(x)}{\mathcal{G}(x)} \right).$$

We considered a sample GMM, GMM$_T$, with $\mu = [1, -1; -1, 1], \sigma = [1, 0; 0, 1], \text{ and } p = [0.5, 0.5].$ We also considered 500 samples to be sufficient to eliminate any statistical errors in KL divergence. We discard the first 50 samples as burn-in samples. For GMM$_T$, Fig. 7(a) shows the sampling trajectory and distribution when the precision of DAC/ADC is 8 bits with 1 volt power supply. The contour lines in the figure represent ground truth GMM and the scattered dots in blue represent simulated distribution of samples from MC$^2$RAM. The trajectory of samples as shown in red in the figure corresponds to 75 random walks. Fig. 7(b) illustrates sampling when mean distance parameter $d$ in $\mu = [d; -d; -d, d]$ between GMM components is set to 5. Fig. 7(c) shows DAC/ADC imprecision tolerance limit in MC$^2$RAM which allows DAC and ADC to be low power/area. Sampling deviates from ground truth for ADC below 5-bit precision. Whereas, reduction in DAC precision has no significant impact in KL divergence. This also justifies our choice of using a low precision two-step flash ADC in MC$^2$RAM which has lower overhead for low to moderate precision design. Also, for fixed sampling iterations KL divergence is high for large separation between GMM components. As we go for higher dimensions, the deviation of samples from ground truth increases as shown in 7(d). For a two-dimensional, two mixture GMM, the implementation consumes $\sim 91\mu$W power per sampling iteration and produces 500 samples in 2000 clock cycles on an average at 1 GHz clock frequency. The pie chart in Fig. 6(e) shows SRAM cells and DAC together contributing to 18% of power consumption whereas the remaining 82% is due to the ADC. The 10 comparators in the 2-step sub-ranging flash ADC constitute 60% of the power consumed by the ADC, however, the delay associated with flash ADC is 2 clock cycles, which improves sampling throughput in MC$^2$RAM.

V. CONCLUSION

We have presented a novel framework MC$^2$RAM that is a key to accelerate Markov chain Monte Carlo (MCMC) sampling for Bayesian Inference (BI). We exploit MC$^2$RAM to store parameters of posterior density of weights in BI and random number generation for high throughput Metropolis-Hastings (MH) based sample acceptance/rejection. The framework samples at low precision and power with tolerance to process variation thus removing latency/energy/safety bottlenecks associated with traditional von Neumann architecture that has spatially distant memory and processing elements.
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