Vector In Memory Architecture for simple and high efficiency computing

Marco A. Z. Alves† Sairo Santos‡+ Aline S. Cordeiro† Francis B. Moreira§ Paulo C. Santos§ Luigi Carro§
†Department of Informatics – Federal University of Paraná – Curitiba, Brazil
‡Department of Exact Sciences and Information Technology – Federal Rural University of the Semi-arid – Angicos, Brazil
§Informatics Institute – Federal University of Rio Grande do Sul – Porto Alegre, Brazil
Email:†{ascordeiro, mazalves}@inf.ufpr.br ‡{sairo.santos@ufersa.edu.br} §{pccsjunior, carro}@inf.ufrgs.br

Abstract—Data movement is one of the main challenges of contemporary system architectures. Near-Data Processing (NDP) mitigates this issue by moving computation closer to the memory, avoiding excessive data movement. Our proposal, Vector-In-Memory Architecture (VIMA), executes large vector instructions near 3D-stacked memories using vector functional units, and uses a small data cache to enable short-term data reuse. It provides an easy programming interface and guarantees precise exceptions. When executing stream-behaved applications using a single core, VIMA offers a speedup of up to 26× over a CPU system baseline with vector operations in a single-core processor while spending 93% less energy.

I. INTRODUCTION

The Von Neumann architecture is the basic design of all modern computers. It requires that any data necessary for computation be placed within the processor before it can be processed. This design has been successful for many decades, but as memory technology advancements lagged behind processor technology within the last few years, the “memory wall” [1] has become an issue. Simultaneously, applications that deal with enormous volumes of data have become more common and relevant. Since moving data between main memory and CPU incurs high latency and energy, the traditional design falters for such applications [1]–[3].

Most current computers try to mitigate the latency and energy issues by placing a cache hierarchy close to the processor. These cache memories store data that has been recently used and may be reused in the future. This approach assumes locality and data-reuse patterns, which can benefit many applications that meet such patterns. However, this cannot be applied for a set of current data-streaming applications, as they present a non-temporal, data-centric streaming-like behavior [4]–[7]. Traditional systems present poor speed, and high energy consumption for such applications as the high cost of retrieving data from the main memory becomes unavoidable. In this scenario, one could argue that prefetchers could solve such a problem. Prefetchers would require aggressive policies to exploit full parallelism on the main memory, resulting in massive data movements and cache pollution. Thus, such aggressiveness might harm the performance of multiple applications [8].

Aiming to solve this issue, NDP is a concept that arises from Processing-In-Memory (PIM). This idea flips the way the computer deals with data-processing by performing the operations near where the data is stored. The recent development of 3D-stacked memories enables NDP 3D-stacked memories are a novel main memory design that stacks up multiple layers of Dynamic Random Access Memories (DRAMs) on top of a layer that features processing capabilities [9]. Such a design enables the processor to trigger and execute these operations on processing elements inside the memory chip, thus reducing off-chip data movement that would otherwise be inevitable. Due to the 3D layout, these memory chips offer high parallelism and low-latency access to the stored data. NDP proposes placing additional logic processing elements on the logic layer to leverage these desirable capabilities to process the portions of applications that most benefit from them [10].

A NDP design can still follow the von Neumann model by placing complete processors near the data. This approach, however, may increase complexity and cause temperature issues in a computer system. Another possible approach is to extend the model by placing only Functional Units (FUs) near data, which avoids those issues and allows processors to continue handling tasks they excel at, such as decoding instructions, predicting the outcome of branches, among other functions.

This paper proposes VIMA, an NDP mechanism that extends the von Neumann model by adding vector functional units near-data, thus avoiding memory-to-processor data movement by performing vector computations near-data. Moreover, VIMA builds on similar proposed mechanisms [11], [12] by including a small data cache within the memory chip, enabling short-term reuse of vectorized data (i.e., instructions’ operands). VIMA advances also include: multi-threading capabilities, easy-to-program interface, extensible design, precise exceptions and interrupts, while being dead-lock free and maintaining high performance and low power consumption.

Our simulation results indicate a speedup of up to 26× in comparison with traditional x86 architectures for seven evaluated kernels. Compared to the state-of-the-art approach, VIMA is on average 14% faster.

II. NEAR-DATA PROCESSING

NDP has emerged as an accelerator that counterpoints classical architectures. In this approach, a processing element is attached to the same chip as the memory, mitigating data movement between memory and processor. Thus, NDP improves performance and reduces energy consumption by using high parallelism and ensuring low average latency for applications when it highly demands data [13], [14]. Illustrated on the right
side of Figure 1, 3D-stacked memories provide several DRAM layers and an additional processing logic layer. Such scenario exploits the low-latency and high-bandwidth access capabilities provided by the internal parallelism [9], [15]–[17] achieved by its multiple independent vaults (similar to channels). Compared to Double Data Rate (DDR) memory technology, these devices require the same voltage level on average while achieving higher memory bandwidth, reaching up to 320 GB/s [18], [19], making them more energy-efficient [20].

III. VIMA: DATA REUSE INSIDE THE MEMORY

Our proposal is called Vector-In-Memory Architecture (VIMA). This architecture adds general-purpose vector operation capabilities to 3D memories to explore the data access parallelism inherent to this architecture. Figure 1 shows VIMA inside a 3D-stacked memory. The main physical addition of VIMA compared to related work is a small cache memory that enables data-reuse of data vectors. At the same time, it maintains most of the performance improvements compared to related PIM strategies. One could perceive this cache addition as a minor change. However, VIMA enables significant improvements due to its new operation rationale, as improved short-term data re-use, easy-to-program interface, precise exceptions, extensible design, dead-lock free architecture, and multi-threading, all discussed in the following sub-sections.

Similar to other NDP approaches, VIMA obtains data from several independent memory vaults in parallel [11], [12], [21]. In this paper, we have compared our work with HMC Instruction Vector Extensions (HIVE) [11], given that their full-stack development environment is available.

![Fig. 1. 3D-stacked memory module with the VIMA architecture.](image)

A. VIMA’s Overview

Like in other vector Instruction Set Architecture (ISA) extensions, such as Streaming SIMD Extensions (SSE) Advanced Vector Extensions (AVX) and NEON, VIMA instructions are inserted into the application by the compiler. During execution, VIMA instructions traverse the processor pipeline up to the execution stage like a regular memory instruction. They are then sent for execution in the 3D-stacked chip, avoiding data movement between memory and processor. VIMA instructions operate over data vectors of 8 KB. An 8 KB vector enables the full parallelism of a 3D-stacked memory chip with 32 vaults and at least eight banks per vault. The small cache memory of 64 KB inside VIMA stores up to eight 8 KB vectors enabling fast reuse of vector operands. Our flexible design also allows the usage of smaller or larger data vectors, reducing or increasing the parallelism inside the memory, respectively. Due to space constraints, this design exploration is out of the scope of this paper.

B. Programming Interface and Binary Generation

VIMA is composed of vector units providing an ISA based on ARM NEON vector instructions [22]. Nevertheless, vendors could adapt for their ISA extensions. To program for the VIMA ISA, we developed Intrinsics-VIMA, a library inspired by Intel/ARM intrinsics [23] available in C/C++ language. Any intrinsic library enables low-level code optimization through routine calls written in assembly. When the program calls any of these routines, the compiler embeds their Single Instruction Multiple Data (SIMD) instructions directly into the assembly code [24], [25]. Intrinsics-VIMA routines provide signed and unsigned operations represented in 32 and 64-bit for integer and floating-point single and double precision representations.

Previous work requires programmers to fine-tune the code to use the available registers or carefully allocate data inside specific memory banks and vaults. Intrinsics-VIMA simplifies the programming burden by allowing developers to include VIMA function calls on the main code, as it works with any C/C++ library. VIMA requires existing applications to be adapted and recompiled. Nevertheless, VIMA could easily be supported by NDP-aware compilers such as PRIMO [26].

C. Processor Required Modifications

In our design, the traditional processor triggers the new VIMA instructions extension to be executed near-data. Thus, VIMA instructions pass through the pipeline like regular memory instructions. All VIMA instructions are placed inside the Memory Order Buffer (MOB) and sent into the memory system upon traversing the pipeline. Once VIMA returns a signal informing the execution status of an instruction (similar to what happens on AVX instructions), the processor reacts to this signal. If it was successfully executed, the processor commits the instruction. Otherwise, it flushes the pipeline, raising an exception and takes the necessary steps to handle it.

The processor achieves precise exceptions by dispatching one VIMA instruction at a time (it dispatches the next instruction after committing the last preceding one). This stop-and-go leads to two sources of performance reduction. First, if VIMA uses smaller vector sizes, it will be unable to use the memory’s internal parallelism fully. For instance, VIMA using 256 B vectors performs, on average, 74% worse than 8 KB. Besides, the second impact of precise exceptions is the execution gap between instructions. The impact of such pipeline bubbles is small for VIMA varying between 2% and 4%. Every VIMA instruction generates at least one load or store operation into the memory. Therefore, these memory
addresses are translated by the Translation Look-aside Buffer (TLB) and go through permission checks like any memory operation. We assume hardware support for huge TLB pages, a common feature in modern processors [27]. VIMA instructions bypass the cache hierarchy. The memory addresses touched by any VIMA instruction are written back from the system’s cache to the main memory before execution to guarantee cache coherence. The traditional cache coherence protocol must be VIMA-aware. It must write back dirty lines and invalidate cache belonging to the pages on which VIMA will operate. These instructions then move into the VIMA instruction sequencer inside the 3D-memory, where the actual data access happens.

D. VIMA Instruction Sequencing, Vector Units and Cache

VIMA requires adding three elements to the 3D-memory: a set of vector functional units, an instruction sequencer, and a cache memory. This paper considers a memory with 32 vaults, 8 independent banks per vault, and 256 B row buffer size, but other layouts are also feasible. VIMA operates over vectors of 8 KB (32 × 256B) utilizing the vault parallelism. One instruction can operate over 2048 × 32-bit elements (e.g., integer) or 1024 × 64-bit elements (e.g., floating-point). We used 256 parallel vector units, which means that eight extra cycles are required to fully process the 2048 elements in a pipelined fashion. This decision reduces the number of wires between the VIMA cache and the vector units.

VIMA executes instructions in-order. Instruction executes as soon as the required data is fetched from the memory vaults and available in the VIMA cache memory. If the data is available in the cache, 1 cycle is required for a tag-check, while another 8 cycles are required for 8 data transfers. These transfers and the functional units are fully pipelined, enabling complete parallelism. As most functional units require two operands, our design uses 2 cache ports to complete the operation in 8 cycles (required by the data transfers) plus the number of cycles required the last pipelined operation.

Once an instruction finishes executing, a status signal is sent to the processor regarding completion or exception (similar to x86 AVX instructions). Before the execution, the sequencer checks the cache for the data that is required by each instruction. In case of a cache hit, the operation starts immediately. The operation ends by writing the results into a fill buffer. When VIMA sends a signal to the processor, it also writes from this buffer into the cache. This effectively hides the write operation inside the gap created by the “stop-and-go” approach. As we write one entire VIMA cache line at once, no Read-to-Modify operation is required. Whenever the VIMA cache evicts this dirty line, it will write the line back to the main memory. During a miss, VIMA cache uses a Least Recently Used (LRU) policy to evict a line. VIMA cache splits each vector access into 128 sub-requests to the vault controllers (for 8 KB vectors, considering 64 B cache lines). Sub-requests guarantee minimal changes inside the DRAM devices as we are using the same cache line granularity. Besides, they are issued to different vaults and banks to increase parallelism.

Regarding the VIMA’s cache coherency, during VIMA’s operation, all data are fetched exclusively from this cache. During processor loads, VIMA’s cache provides data if available. During processor writes, it writes back and invalidates the respective entry. We consider that such cache could be gated-vdd during long periods of inactivity.

E. Comparison Between VIMA and Related Work

Most NDP related work [11], [12], [21], enables data reuse by using a register bank. VIMA’s design is extensible, as it can use larger cache memories, while the code does not require modifications to use any extra storage for data-reuse. Besides, HIVE relies on transactions to maintain coherence inside its register bank, which requires locking and unlocking the register bank for each thread during execution, writing NDP code as transactions. Thus, HIVE programmers must perform a lock and fetch the necessary data into the register bank before executing operations. Moreover, it must also write back all the registers’ data to the main memory before unlocking to keep consistency, possibly leading to overheads during loop executions. Nevertheless, these additional lock/unlock instructions also overhead the processor pipeline stages and structures. Meanwhile, VIMA does not require any lock/unlock eliminating potential dead-lock and process starvation scenarios, and it performs write-back as needed without a prefixed deadline. At the same time, we enable a multi-threaded environment by not locking any structure.

![Speedup of HIVE and VIMA normalized to baseline AVX with a single thread (higher is better).](image)

**Figure 2.** Speedup of HIVE and VIMA normalized to baseline AVX with a single thread (higher is better).

While HIVE improves over AVX, the speedup is modest. Nevertheless, HIVE outperforms VIMA in two out of three datasets.

Although VIMA provides vector operations, traditional vector extensions (e.g., AVX, SSE) are still valid for non-data-streaming programs to benefit from the usual cache hierarchy.

IV. EXPERIMENTAL EVALUATION OF VIMA

This section presents our methodology and results for VIMA evaluation. We refer to AVX and VIMA when discussing applications that use Intel AVX 512 and VIMA respectively.
Due to the programming complexity, this section will not bring [HIVE] results. Please refer to Figure 2 for a direct comparison between [HIVE], [VIMA], and [AVX] evaluating applications made available by the authors.

A. Methodology

We used SiNUCA [28], a cycle-accurate simulator, to evaluate the architecture. The simulation parameters are similar to Intel’s Sandy Bridge microarchitecture. Simulation parameter details are disclosed on Table I.

We used 7 integer and floating-point kernels as workload. The integer kernels are Memory Copy and Memory Set, which generate most of the data movement in big data applications and typical consumer workloads [7]. The floating point kernels are Vector Sum, Matrix Multiplication, k-Nearest Neighbors, Multi-Layer Perceptron, and Stencil convolution, which represent applications like neural networks and computational fluid dynamics processing. For all applications (except MatMul), we used data sets of 4 MB, 16 MB, and 64 MB. We obtained the application traces using Pin [29] tool, using VIMA Intrinsics (see section III-B). Below we describe each application:

MemSet: sets all positions of a vector to a specific value.
MemCopy: copies the contents of a vector to a new vector in a different memory location.
VecSum: sums up each element of two input vectors storing the result in an output vector.
Stencil: convolution using a 5-points stencil over a matrix storing the result in an output matrix.
MatMult: multiplies two square matrices and stores the results in an output matrix. Due to the long simulation time of this application, we adopted smaller matrix sizes, resulting in total footprints of 6 MB, 12 MB, and 24 MB.

kNN: classifies 256 test instances in an n-dimensional space. We used K to equal 9, 32768 training instances, varying the number of characteristics (32, 128, 512).
MLP: neural network inference step. We used 32768 test instances, varying the number of characteristics (64, 256, 1024).

B. Results

In this section we present speedup and energy results of our proposal compared to AVX, varying the number of threads, and a design space exploration of VIMA cache size.

1) Single Thread Speedup: Figure 3(a) shows the speedup results for the benchmarks using VIMA compared to AVX as baseline, while varying the input size. Speedup on integer benchmarks MemSet and MemCopy happens mainly because of the superior use of parallelism in the memory when fetching data without any data reuse. Still, it is partially limited because each VIMA instruction generates only a single VIMA cache miss at a time. In contrast, whenever VIMA requires two operands (generating two vector misses), both are requested leveraging the bank parallelism inside each vault. VIMA presents a similar execution time for these two applications, while AVX presents faster execution for MemSet that have a smaller memory footprint.

| Speedup | 4MB | 16MB | 64MB |
|---------|-----|------|------|
| MemSet | 1.67 | 2.67 | 2.17 |
| MemCopy | 1.00 | 1.00 | 1.00 |
| VecSum | 0.64 | 0.62 | 0.59 |
| Stencil | 0.59 | 0.57 | 0.55 |
| kNN | 0.25 | 0.25 | 0.25 |
| MLP | 0.6 | 0.6 | 0.6 |

The execution of VecSum using VIMA offers significant performance improvements by making good use of parallelism in the main memory. Namely, by fetching two large vectors in parallel, VIMA outperforms AVX by over 7× for this benchmark with the largest input size.

The Stencil algorithm offers good opportunities for reuse of vectorized data and thus also shows significant speedup. Here, data fetches with a single element stride are expected and can be served by the cache. Results vary according to input size and matrix size, considering whether the dataset fits inside the last level cache of the baseline system and how efficiently the algorithm deals with different matrix dimensions. These factors cause the smaller speedup for the 4 MB input size and the increase of speedup between the 16 MB and 64 MB datasets.

Results for kNN and MLP using VIMA present no speedup whenever the data set used fits in the cache hierarchy of the baseline system (4 and 16 MB cases). For these cases, the processor cache hierarchy provides quick access to all the data necessary for processing. However, the speedup is considerable when the input size exceeds the size of the last level cache. VIMA is up to 4× faster than AVX for the 64 MB datasets, when the x86 cache presents no help.

The MatMul application uses a total of 6 MB, 12 MB, and 24 MB, considering the three matrices. For a straightforward, clear comparison of the memory access performance, we used
the same algorithm for AVX and VIMA which led to higher gains for VIMA. However, in our tests a tiled algorithm for AVX can result in up to $4 \times$ improvements. In such scenario, VIMA would still over 6.5 x faster for the 24 MB problem size.

2) Multi-Threaded Speedup and Energy: In comparison to multithreaded AVX, our discussion considers only the largest sizes of benchmarks Stencil, VecSum, and MatMult. Figure 4 compares VIMA with an AVX implementation using up to 32 cores. The percentages above the plot indicate the energy consumption of each execution relative to AVX single-threaded execution, in the respective order.

![Speedup and energy of VIMA and AVX multithreaded normalized to baseline AVX with a single thread](image)

Considering these results, VIMA offers both superior performance and significant energy savings when compared to a single-threaded execution. It continues to outperform the baseline system for VecSum when these are executed with up to 16 cores in parallel, at a very small fraction of the consumption of energy. For Stencil and MatMult applications VIMA presents better performance even compared to AVX with 32 threads. For such applications VIMA benefits from the internal 3-D-memory parallelism, while the VIMA cache provides necessary data reuse to enable gains. At the same time, VIMA does not rely on multiple cache levels, which would add extra latency to the memory latencies during a sequence of misses.

![Speedup of VIMA with different cache sizes normalized to baseline AVX with a single thread](image)

3) VIMA Cache Size Speedup: Previous results consider only a fixed VIMA cache size of 64 KB. In this subsection we present how different cache sizes would affect performance of VIMA processing. Figure 5 presents speedup results over a single-threaded baseline for the largest dataset of the Stencil, VecSum and MatMult benchmarks.

We expected small gains for larger VIMA caches as we designed the algorithms to use fewer VIMA cache lines as possible. On average, for all seven applications used in this paper, 6 lines would be enough to achieve most of the presented performance. However, more complex kernels might benefit from larger VIMA caches, storing temporary data. Nevertheless, we should be aware that VIMA does not intend to replace traditional processors, but provide an efficient accelerator for streaming applications with low data reuse behavior.

V. RELATED WORK

Researchers in several distinct areas have explored the PIM capabilities of 3D-stacked memories. Xie et al. [30] moved a portion of the computations necessary to render 3D images to the logic layer of a 3D-stacked memory. The authors aimed to reduce data traffic during some of the more memory-intensive portions of graphics processing algorithms. Korikawa et al. [31] used PIM in Network Function Virtualization (NFV) environments to speed up packet processing by leveraging bank interleaving and channel parallelism of 3D-stacked memories.

Numerous research efforts in NDP address big data application requirements, which are particularly susceptible to data movement pitfalls. Lee et al. [32] identified data redundancy in data centers and proposed a PIM accelerator for inline Data Deduplication (DU) that significantly reduced latency and power consumption in comparison to traditional DU tools. Some NDP research efforts include placing Accelerated Processing Units (APUs) or ARM cores on the logic layer of a 3D-stacked memory. These works focus on Machine Learning (ML) training functions [33], large-scale graph processing [34], and in-memory network frameworks [35]. These require ARM cores in conjunction with a TLB and rely on routers for vault communication. VIMA is simpler as it does not add cores to the system or rely on vault communication to enhance performance.

Other proposals add specific-purpose cores to the 3D-stacked memory. For instance, NIM [36], a reconfigurable Neural Network (NN) accelerator, like VIMA is a NDP architecture that allows for vector operations, features processing units and a sequencer, and is attached to the crossbar switch. However, it is much more complex and expensive as it requires one register bank per vault, while VIMA stores data in a cache that is accessible from all vaults and enables reuse. Several other efforts applied similar principles and offer features like deactivating FUs on-demand and enhancing the execution of Convolutional Neural Networks (CNNs). However, these required adding modules to each vault of a 3D-stacked memory, making them more expensive and complicated than VIMA.

Several PIM techniques do not rely on 3D-stacked memories to propose modifying conventional DRAM memories and repurposing some of its internal circuits to achieve computation capabilities [37-42]. While this is generally not an expensive approach, it is a lot trickier to program and error-prone than VIMA as often programmer must take care of low-level implementation details.

VI. CONCLUSIONS

This paper introduced VIMA, an NDP mechanism that enables the reuse of data vectors within 3D-stacked memories through a small cache memory. We have shown that VIMA is an efficient approach to reduce data movement, and thus presents...
itself as an energy-efficient option for a computational system. \textbf{VIMA} improves the execution time of well-known application kernels that present streaming behavior by up to 26×, while also reducing energy consumption by up to 93%. Even when executing advanced machine learning application kernels, such as k-Nearest Neighbors and Multi-Layer Perceptron, \textbf{VIMA} outperforms traditional processor with AVX512 by up to 6×.

In our analysis with stream-like applications, traditional processors require, on average, 16 cores to reach the same performance level of \textbf{VIMA}. Thus, \textbf{VIMA} efficiently provides high performance consuming a fraction of AVX energy.

In the future, we would like to expand the usage of \textbf{VIMA} on applications with non-spatial data locality. Planning also a compiler pass for automatic conversion of AVX into \textbf{VIMA} instructions, creating a transparent programming interface.

\section*{References}

[1] W. A. Wulf and S. A. McKee, “Hitting the memory wall: Implications of the obvious,” ACM SIGARCH Computer Architecture News, vol. 23, 1995.
[2] R. Balasubramonian, J. Chang, T. Manning, J. H. Moreno, R. Murphy, R. Nair, and S. Swanson, “Near-data processing: Insights from a micro-46 workshop,” IEEE Micro, vol. 34, 2014.
[3] M. Hashemi, E. Ebrahimi, O. Mutlu, Y. N. Patt, et al., “Accel-erating dependent cache misses with an enhanced memory controller,” in Int. Symp. on Computer Architecture. 2016.
[4] P. Xie, G. Sun, F. Wang, and G. Luo, “V-pim: An analytical overhead model for processing-in-memory architectures,” in Non-Volatile Memory Systems and Applications Symp., 2018.
[5] M. K. Qureshi, A. Jaleel, Y. N. Patt, S. C. Steely, and J. Emer, “Adaptive insertion policies for high performance caching,” ACM SIGARCH Computer Architecture News, vol. 35, 2007.
[6] M. K. Qureshi, M. A. Suleman, and Y. N. Patt, “Line distillation: Increasing cache capacity by filtering unused words in cache lines,” in Int. Symp. on High Performance Computer Architecture. 2007.
[7] A. Boroumand, S. Ghose, Y. Kim, R. Ausavarungnirun, E. Shiu, et al., “Google workloads for consumer devices: Mitigating data movement bottlenecks,” in Int. Conf. on Architectural Support for Programming Languages and Operating Systems, 2018.
[8] E. E. et al., “Coordinated control of multiple prefetchers in multi-core systems,” in Int. Symp. on Microarchitecture, 2009.
[9] Hybrid Memory Cube Consortium. Hybrid memory cube specification 2.1, [http://www.hybridmemorycube.org/] 2014.
[10] D. Lee, S. Ghose, G. Pechmenko, S. Khan, and O. Mutlu, “Simultaneous multi-layer access: Improving 3d-stacked memo-ry bandwidth at low cost,” ACM Trans. on Arch. and Code Optimization, vol. 12, 2016.
[11] M. A. Z. Alves, M. Diener, P. C. Santos, and L. Carro, “Large vector extensions inside the hmc,” in Design, Automation & Test in Europe Conf., 2016.
[12] P. C. Santos, G. F. Oliveira, D. G. Tomé, M. A. Z. Alves, E. C. Almeida, and L. Carro, “Operand size reconfiguration for big data processing in memory,” in Design, Automation & Test in Europe Conf., 2017.
[13] D. Patterson, T. Anderson, N. Cardwell, R. Fromm, K. Keeton, C. Kozyrakis, R. Thomas, and K. Yelick, “A case for intelligent ram,” IEEE Micro, vol. 17, 1997.
[14] D. G. Elliott, M. Stubnum, W. M. Snelgrove, C. Cojocaru, and R. McKenzie, “Computational ram: Implementing processors in memory,” Design & Test of Computers, vol. 16, 1999.
[15] O. Mutlu, S. Ghose, J. Gómez-Luna, and R. Ausavarungnirun, “Enabling practical processing in and near memory for data-intensive computing,” in Design Automation Conf., 2019.
[16] J. Jeddoloh and B. Keeth, “Hybrid memory cube new DRAM architecture increases density and performance,” in Symp. on VLSI Technology, 2012.
[17] J. T. Pawlowski, “Hybrid memory cube (hmc),” Hot Chips, vol. 23, 2011.
[18] Transcend, DDR comparison, [https://www.transcend-info.com/Support/FAQ-296], [01-Jul-2019], 2014.
[19] AMD, DDR5 and HBM comparison, [https://www.amd.com/system/files/documents/high-bandwidth-memory-hbm.pdf] [01-Jul-2019], 2015.
[20] J. Hrusca, PIM comparison, [https://www.extremetech.com/computing/197720-beyond-ddr4-understand-the-differences-between-wide-io-hbm-and-hybrid-memory-cube] [01-Jul-2019], 2015.
[21] D. G. Tomé, P. C. Santos, L. Carro, E. C. Almeida, and M. A. Z. Alves, “Hipe: Hmc instruction predication extension applied on database processing,” in Design, Automation & Test in Europe Conf., 2018.
[22] ARM, Arm cortex-a57 technical reference manuals, 2020.
[23] C. Lomont, “Introduction to intel advanced vector extensions,” Intel White Paper, 2011.
[24] I. Coorp., Intel 64 and ia-32 architectures optimization reference manual, 2009.
[25] A. S. Cordeiro, T. R. Kepe, D. G. Tomé, E. C. Almeida, and M. A. Z. Alves, “Intrinsics-hmc: An automatic trace generator for simulations of processing-in-memory instructions,” Smp. em Systemas Computacionais de Alto Desempenho, 2017.
[26] H. Ahmed, P. C. Santos, J. P. C. Lima, R. F. Moura, M. A. Z. Alves, A. C. S. Beck, and L. Carro, “A compiler for automatic selection of suitable processing-in-memory instructions,” in Design, Automation & Test in Europe Conf., 2019.
[27] Y. Kwon, H. Yu, S. Peter, C. J. Rossbach, and E. Witchel, “Coordinated and efficient huge page management with in-gens,” in USENIX Symp. on Operating Systems Design and Implementation, 2016.
[28] M. A. Z. Alves, C. Villavieja, M. Diener, F. B. Moreira, and P. O. A. Navaux, “Simuca: A validated micro-architecture simulator,” in Int. Conf. on High Performance Computing and Communications, 2015.
[29] M. Bach, M. Charney, R. Cohn, E. Demikhovsky, T. Devor, K. Hazelwood, A. Jaleel, et al., “Analyzing parallel programs with pin,” Computer, vol. 43, 2010.
[30] C. Xie, S. L. Song, J. Wang, W. Zhang, and X. Fu, “Processing-in-memory enabled graphics processors for 3d rendering,” in Int. Sym. on High Performance Computer Architecture, 2017.
[31] T. Korikawa, A. Kawabata, F. He, and E. Oki, “Packet processing architecture using last-level-cache slices and interleaved 3d-stacked dram,” IEEE Access, vol. 8, 2020.
[32] Y. S. Lee, K. M. Kim, J. H. Lee, J. H. Choi, and S. W. Chung, “A high-performance processing-in-memory accelerator for in-line data deduplication,” in Int. Conf. on Computer Design, 2019.
[33] J. Liu, H. Zhao, M. A. Ogliari, D. Li, and J. Zhao, “Processing-in-memory for energy-efficient neural network training: A heterogeneous approach,” in Int. Symp. on Microarchitecture, 2018.
[34] J. Ahn, S. Hong, S. Yoo, O. Mutlu, and K. Choi, “A scalable processing-in-memory accelerator for parallel graph processing,” in Int. Symp. on Computer Architecture, 2015.
[35] M. Gao, G. Ayers, and C. Kozyrakis, “Practical near-data processing for in-memory analytics frameworks,” in Int. Conf. on Parallel Arch. and Compilation, 2015.
[36] G. F. Oliveira, P. C. Santos, M. A. Z. Alves, and L. Carro, “Nim: An hmc-based machine for neuron computation,” in Int. Sym. on Applied Reconfigurable Computing, 2017.
[37] D. Gao, T. Shen, and C. Zhuo, “A design framework for processing-in-memory accelerator,” in Int. Workshop on System Level Interconnect Prediction, 2018.
[38] Q. Deng, L. Jiang, Y. Zhang, M. Zhang, and J. Yang, “Dracc: A dram based accelerator for accurate cnn inference,” in Design Automation Conf., 2018.

[39] S. Li, D. Niu, K. R. Malladi, H. Zheng, B. Brennan, and Y. Xie, “Drisa: A dram-based reconfigurable in-situ accelerator,” in Int. Symp. on MicroArch., 2017.

[40] Q. Deng, Y. Zhang, M. Zhang, and J. Yang, “Lacc: Exploiting lookup table-based fast and accurate vector multiplication in dram-based cnn accelerator,” in Design Automation Conf., 2019.

[41] J. Sim, H. Seol, and L.-S. Kim, “Nid: Processing binary convolutional neural network in commodity dram,” in Int. Conf. on Computer-Aided Design, 2018.

[42] C. Sudarshan, J. Lappas, M. M. Ghaffar, V. Rybalkin, C. Weis, M. Jung, and N. Wehn, “An in-dram neural network processing engine,” in Int. Symp. on Circuits and Systems, 2019.