High-efficiency concurrent dual-band class-E power amplifier with extended maximum operating frequency

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Abstract This paper presents a method for designing high-efficiency concurrent dual-band (DB) class-E power amplifier (PA) that operate above the theoretical maximum frequency (fmax). The excess output capacitances at the two desired frequencies can be compensated using the proposed output matching network without separate design of harmonic compensation network, thus the fundamental and harmonic impedances for DB optimum class-E operation are achieved above the fmax, considering the parasitics of the packaged transistor. For demonstration, the fabricated DB class-E PA using GaN HEMT features the maximum power-added efficiency (PAE) of 74.1% and 72.6% at 1.9 and 2.5 GHz, while the output power is 40.3 and 40.7 dBm, respectively.
key words: power amplifier, high-efficiency, class-E, dual-band, GaN HEMT
Classification: Microwave and millimeter wave devices, circuits, and hardware

1. Introduction

The rapid development of modern wireless/mobile communication has raised the demand for multistandard and multiband transceiver systems [1]. Accordingly, as the key component of the RF front-end, the power amplifiers (PAs) should also operate in multiband to meet these communication requirements [2-3]. Meanwhile, since the PAs strongly influence the overall system power consumption, one of the major challenges is to design the high-efficiency PAs [4]. Recent years, various efficiency improvement strategies of PAs have been proposed, such as class-E [5-7], class-F [8-10], class-EF [11-13], and so on. Among them, class-E PAs have become very popular in the RF front-end due to its simplicity and high-efficiency. The maximum theoretical drain efficiency of the class-E PA reaches 100% [14-16]. Therefore, as the basic realization of multiband PAs, the design of high-efficiency DB class-E PAs attracts increasing attentions.

However, the DB class-E PAs introduced in [17-18] were not compensated the excess output capacitances at the two desired bands, or the parasitic parameters of the package transistor were not considered, which deteriorate the efficiency of those amplifiers. To extend the fmax of DB class-E PA, a harmonic compensation network proposed in [19] was used to compensate the excess output capacitances at harmonics. Nevertheless, the output matching network can be further simplified to satisfy the impedance conditions when considering the parasitics of the transistor for optimum class-E operation above the fmax.

In this paper, a new method to design high-efficiency DB class-E PA at microwave frequencies is presented. The proposed output matching network can avoid the separate design of harmonic compensation circuit, and it is allowed for the optimum class-E operation above the fmax by satisfying the optimum output fundamental and harmonic impedances at package reference plane at the two desired bands.

2. Analysis and design of DB class-E PA

2.1 Class-E PA with extended fmax

The basic circuit schematic of the idealized class-E PA is shown in Fig.1 [15].

![Fig.1. The schematic of idealized Class-E PA.](image-url)

The class-E PA uses zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions to obtain high efficiency [16]. As shown in Fig.1, when the switching frequency of the transistor is f at the fundamental frequency, the impedances of the output...
matching network are found to be [20].

\[
Z_E = \begin{cases} 
0.28 \frac{1}{2\pi f C} (1 + j * \tan(45.05^\circ)) @ f \\
@nf, \ n > 1
\end{cases}
\]  

(1)

In practice, an open-circuit termination at the second harmonic (2f) i.e. \(Z_{E(2f)} = \infty\), is sufficient to obtain Class-E operation [20].

For a prescribed output power \(P_{out}\) and supply voltage \(V_D\). The maximum operating frequency \(f_{max}\) of the class-E PA is strictly constrained by the transistor output capacitance \(C_{out}\), as described by [21].

\[
f_{max} = 0.0507 \frac{P_{out}}{C_{out} V_D^2}
\]  

(2)

It can be seen from Eq. (2) that \(f_{max}\) is inversely proportional to \(C_{out}\). When the class-E PAs operate in the microwave frequency, the operating frequency is much higher than \(f_{max}\), and the \(C_{out}\) will exceed the required shunt capacitance \(C\) for the optimum class-E synthesis, resulting in an excess capacitance \(C_X = C_{out} - C\), as shown in Fig.2. Thus the class-E PAs don’t meet the boundary conditions of ZVS and ZVDS. In order to make the class-E PAs operate above the \(f_{max}\), it is necessary to compensate \(C_X\) at fundamental and harmonic frequencies [19].

![Fig.2. The schematic of Class-E PA with excess capacitance.](image)

2.2 Class-E PA considering the parasitics of transistor

Practically, as shown in Fig.3, the multiple impedance solutions are derived at class-E reference plane, while the output matching networks are conducted on the package plane. By using the S-parameters \(S^P\) extracted from the approximated equivalent network of the parasitic model at device output [22], the optimal impedances \(Z_E = [Z_{E(0)} \ Z_{E(2f)}]\) at class-E reference plane can be transformed to the package plane \(Z_{pkg} = [Z_{pkg(0)} \ Z_{pkg(2f)}]\), which are calculated by [22].

\[
\Gamma_{pkg} = \frac{Z_{pkg} - S^P}{S_{11}^P S_{12}^P - S_{11}^P S_{22}^P + S_{22}^P \Gamma_E}
\]  

(3)

It should be noted that the reference plane of the \(S^P\) obtained here has been transformed to the class-E reference plane by eliminating the effect of the required shunt capacitance \(C\). Hence, the \(Z_{pkg}\) obtained at the package plane is also optimum even though the class-E is operated above the \(f_{max}\), since the effect of the excess capacitance \(C_X\) and the parasitics of the transistor have been considered simultaneously.

![Fig.3. The optimal impedances under class-E operation considering the parasitics of transistor.](image)

2.3 Design of DB class-E PA with novel output matching network

Fig. 4 shows the proposed output matching network of the DB class-E PA. The DB harmonic control circuit consist of \(T_1\), \(T_2\), \(T_3\) and \(T_4\). The DB fundamental matching circuit consist of \(T_5\), \(T_6\), \(T_7\), \(T_8\) and \(T_9\). The DB biasing line in the PA design provides DC power supply only without affecting RF performance at the two desired frequencies, whose design procedures are given in [23].

![Fig.4. Proposed output matching network of the DB class-E PA.](image)

In order to simplify the problem, it is assume that the series line \(T_1\) and \(T_3\) have the same characteristic impedances: \(Z_1 = Z_3 = 50 \ \Omega\); the open-circuit stub \(T_2\) and \(T_4\) have the same characteristic impedances: \(Z_2 = Z_4 = 80 \ \Omega\). First, \(T_2\), the electronic length of which is 45° at \(f_2\), can provide short-circuit at \(2f_2\). Then, the series line \(T_1\) is used to match the optimum second-harmonic impedance at \(2f_2\) at the package plane, the electronic length \(\theta_1\) of \(T_1\) can be calculated by Eq. (4) and (5).

\[
jZ_1 \tan\left(2m\theta_1\right) = jX_{P(2f_2)}
\]  

(4)

\[
\theta_1 = \frac{1}{2m} \arctan \frac{X_{P(2f_2)}}{Z_1} + a\pi
\]  

(5)

where \(m = (f_2/f_1) > 1\), \(a\) is an integer greater than 0.

Second, \(\theta_3\) of the open-circuit stub \(T_4\) is 45° at \(f_1\), and it provides a short-circuit termination to the series line \(T_3\). The short-circuit series line \(T_3\) combined with the open-circuit stub \(T_2\) and the series line \(T_1\), which are used to match the optimum second-harmonic impedance at \(2f_1\) at the package plane. Hence, \(\theta_3\) can be determined by Eq. (6) and (7).
\[
Y_{\text{pkg}(2f_1)} = Y_1 + jY_1 \tan 2\theta_1
\]
\[
Y_{\text{in}} = j \left[ Y_2 \tan \left( \frac{\pi}{2m} \right) - \frac{Y_3}{\tan \theta_3} \right]
\]
where \( Y_{\text{pkg}(2f_1)} = 1/Z_0 \), \( Y_1 = 1/Z_1, Y_2 = 1/Z_2, Y_3 = 1/Z_3 \).

After finishing the DB harmonic control circuit, it is also very essential to compensate \( C_{X1} \) and \( C_{X2} \) at the fundamental of the two desired bands for the DB class-E PA. The optimal fundamental impedances of the two frequencies are changed after point A due to the harmonic control circuit. We can also use the S-parameters extracted from the harmonic control circuit to obtain the optimal fundamental impedances \( Z_i \) after point A at the two desired bands. In the DB fundamental matching circuit design, the series line \( T_5 \) are used to transform \( Z_i \) (i.e. \( Z_{i1} = R_{i1} + jX_{i1} \) at \( f_i \), \( Z_{i2} = R_{i2} + jX_{i2} \) at \( f_i \)) to a pair of conjugate complex impedances \( Z_{i1}^* \) (i.e. \( Z_{i1}^* = R_{i1}^* + jX_{i1}^* \) at \( f_i \), \( Z_{i2}^* = R_{i2}^* + jX_{i2}^* \) at \( f_i \)) at the two desired bands. Hence, the electrical length \( \theta_1 \) and characteristic impedance \( Z_5 \) can be calculated according to Eq. (8) and (9) as follows [24]
\[
Z_5 = \frac{\sqrt{R_{i1}^2|Z_{i2}|^2 - R_{i2}^2|Z_{i1}|^2}}{R_{i2} - R_{i1}}
\]
\[
\theta_1 = -\frac{b\pi + \arctan \frac{Z_{11}^*(R_{i1} - R_{i2})}{X_{11}R_{i2} - X_{i2}R_{i1}^*}}{m + 1}
\]
where \( b \) is an integer greater than 1.

Then, the open-circuit stub \( T_6 \) and short-circuit stub \( T_7 \) are used to transform the \( Z_{i1}^* \) and \( Z_{i2}^* \) to a real impedance \( R \). It is assumed that
\[
Y_{i1}^* = \frac{1}{Z_{i1}^*} = G_{i1}^* + jB_{i1}^*
\]
\[
Y_{i2}^* = \frac{1}{Z_{i2}^*} = G_{i2}^* + jB_{i2}^*
\]
The simultaneous equations are required to evaluate the parameters [25].
\[
\tan \theta_6 - \frac{1}{Z_6 \tan \theta_7} = -B_{i1}^*
\]
\[
\tan (m\theta_6) - \frac{1}{Z_6 \tan (m\theta_7)} = B_{i1}^*
\]
Eq. (12) and (13) involve four design parameters. Thus, two of the four parameters can be freely set to ensure that the parameters of \( T_6 \) and \( T_7 \) are not negative, extremely high, or extremely low [25].

Once the series line \( T_5 \), the open-circuit stub \( T_6 \) and the short-circuit stub \( T_7 \) has been determined, the matching method between the real impedance \( R \) and the load \( Z_0 \) are summarized as follow [26]
\[
\theta_8 = \theta_9 = \pi \frac{m + 1}{m + 1}
\]
\[
Z_8 = \frac{RZ_0^2}{Z_9^2}
\]
Therefore, the compensation of \( C_{X1} \) and \( C_{X2} \), as well as the optimal impedance conditions of class-E operation at the two desired bands are realized, considering the parasitics of the transistor.

3. DB class-E PA implementation and performance

To verify the feasibility of the proposed matching network, a commercial 10W CGH40010 GaN HEMT nonlinear model provided by Inc. Cree, is adopted to enable the design of DB class-E PA. The output parasitic model of this transistor is illustrated in [27], where the \( C_{\text{out}} = 1.22 \) pF. Based on the class-E theory, the maximum theoretical frequency for this transistor is: \( f_{\text{max}} = 0.53 \) GHz. The optimum shunt capacitance and the excess capacitance at 1.9 GHz are: \( C_L = 0.34 \) pF and \( C_{X1} = 0.88 \) pF, while \( C_2 = 0.3 \) pF and \( C_{X2} = 0.92 \) pF at 2.5 GHz. However, the intrinsic parasitics are usually nonlinear (voltage dependent), which might result in an accuracy degradation of this model in the high power case [22]. Fortunately, a high-accuracy nonlinear model of this transistor is available from the manufacturer. Therefore, the load-pull simulation is conducted on the GaN transistor using ADS in order to find a more accurate load impedance. As shown in Fig. 5, the optimum load impedances at the package reference are achieved.

The designed complete schematic of proposed DB class-E PA is shown in Fig. 6. A Rogers 4350B substrate with relative dielectric constant 2.2 and a plate thickness of 0.762 mm is chosen. The drain voltage is set as 28V and the gate bias voltage is set as -3.0 V, respectively. Fig. 7 (a) and (b) show the simulated voltage and current waveforms at the intrinsic drain plane at 1.9 and 2.5 GHz respectively. Compared to the ideal waveforms, the
simulated results show a similar shape while the difference is mainly due to nonideal switching effect, which leads to degraded efficiency performances.

Fig. 6. Complete circuit schematic of proposed DB class-E PA.

Fig. 7. De-embedded intrinsic drain waveforms of voltage and current from ADS simulation: (a) 1.9 GHz, (b) 2.5 GHz.

Fig. 8 shows the photograph of the fabricated DB class-E PA. The large-signal continuous-wave (CW) performance was measured by a power spectral analyzer Rohde & Schwarz FSV40. Fig. 9 (a) and (b) show the measured output powers, gains, and PAE versus the input powers at the two required frequencies. For the measurements, the peak PAEs at 1.9 GHz and 2.5 GHz reach 74.1% and 72.6%, and the corresponding output powers reach 40.3 dBm and 40.7 dBm, respectively. Fig.10 gives the measured and simulated output powers gain and PAE across the testing frequencies from 1.7 GHz to 2.7 GHz. For each test, the input power is fixed as 28 dBm. As depicted in Fig.10, the PAE curves reach the peak positions at 1.9 GHz and 2.5 GHz.

Table I gives a performance comparison with recent published high-efficiency DB PAs [19, 28, 29, 30]. Among these performance indices, FE refers to frequencies-weighted average efficiency, which helps to evaluate frequency together with the PA efficiency [19]. Obviously, the proposed DB class-E PA exhibits a comparable FE at the two frequencies with a simple output matching circuit.

Table I. Performance summary of high-efficiency DB power amplifiers with packaged devices

| Reference | Frequency (GHz) | Pout (dBm) | PAE (%) | FE (%) |
|-----------|-----------------|------------|---------|--------|
| [19]      | 1.72/2.14       | 40.5/40.9  | 74.9/75.9 | 85.5/91.8 |
4. Conclusion

This paper presents an output matching network for the high-efficiency concurrent DB class-E PA. The proposed circuits avoid the separate design of harmonic compensation network, which realize the fundamental and harmonic impedance conditions for optimum class-E operation at the two desired frequencies above the $f_{\text{max}}$, considering the parasitics of the transistor. One prototype is designed and fabricated for demonstration. Measurement results show that the proposed DB class-E PA is achieved at 1.9 and 2.5 GHz with peak PAE of 74.1% and 72.6%, and the output power reaches 40.3 and 40.7 dBm, respectively.

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