Optimization of 10nm Bi-GFET Device for higher I\textsubscript{ON}/I\textsubscript{OFF} ratio using Taguchi Method

Ameer F Roslan\textsuperscript{1}, K E Kaharudin\textsuperscript{1}, F Salehuddin\textsuperscript{1}, A S M Zain\textsuperscript{1}, I Ahmad\textsuperscript{2}, Z A N Faizah\textsuperscript{2}, H Hazura\textsuperscript{1}, A R Hanim\textsuperscript{1}, S K Idris\textsuperscript{1}, A M Zaiton\textsuperscript{1}, N R Mohamad\textsuperscript{1}, Afifah Maheran A Hamid\textsuperscript{1}

\textsuperscript{1}MiNE, Centre for Telecommunication Research and Innovation (CeTRI), Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka
\textsuperscript{2}College of Engineering, Universiti Tenaga Nasional (UNITEN), 43009 Kajang, Selangor, Malaysia

Abstract. The simulation and statistical modeling are conducted using Silvaco TCAD tools and L\textsubscript{9} orthogonal array (OA) of Taguchi method respectively to design a proposed layout of 10 nm gate length (L\textsubscript{g}) Bilayer Graphene Field Effect Transistor (Bi-GFET). The investigated process parameters are halo implant dose, halo implant energy, source/drain (S/D) implant dose and source/drain (S/D) implant energy, while the noise factors are halo implant tilt angle and source/drain (S/D) implant tilt angle. The process parameters and the noise factors are optimized using the L\textsubscript{9} orthogonal array (OA) of Taguchi method to achieve the highest possible I\textsubscript{ON}/I\textsubscript{OFF} ratio. Utilizing both signal-to-noise ratio (SNR) and analysis of variance (ANOVA), the most dominant process parameters upon I\textsubscript{ON}/I\textsubscript{OFF} ratio are identified as S/D implant energy and S/D implant dose with 56% and 37% factor effects on SNR respectively. The largest factor effects on SNR of S/D implant energy shows that it has dominantly affected the I\textsubscript{ON}/I\textsubscript{OFF} ratio. The final results indicate that the 1.99 x 10\textsuperscript{13} atom/cm\textsuperscript{3} of halo implant dose, 174 keV of halo implant energy, 1.63 x 10\textsuperscript{14} atom/cm\textsuperscript{3} of S/D implant dose, 17 keV of S/D implant energy, 24\textdegree{} of halo implant tilt angle and 9\textdegree{} of S/D implant tilt angle are the best parameter setting in obtaining the highest I\textsubscript{ON}/I\textsubscript{OFF} ratio of the device which is measured at 4.811 x 10\textsuperscript{5}.

1. Introduction
For decades, the field effect transistor (FET) shrinkage has been the key progress in integrated circuits. The FET scaling has enabled the integrated circuits become compact, leading to significant improvements in performance and the decreases in price per transistor [1]. Due to the high complexity of ICs fabrication process, semiconductor fabrication plants has become extremely expensive. Furthermore, the scaling alone requires performance improvements from one generation of ICs to the next, thus motivating the chip-designers to introduce devices based on the fundamentally different physics or materials other than silicon [2]. It will be necessary to introduce new materials, device concepts and optimization approaches to ensure that the device performance continues to be improved. The significant discovery of graphene [3] has evoked serious research works to study the electrical properties of two-dimensional (2D) graphene...
field effect transistor (GFET). Enormous field-effect mobility as high as 15,000 cm²/V-s and a Fermi velocity of ~108 cm/s have been reported at room temperature [4]. These excellent properties imply graphene as a possible candidate for future transistor technology. The significant benefit of graphene is emphasized on the superior electron/hole mobility compared to other semiconductors. However, the lack of bandgap limits the usage of two dimensional graphene for digital switching in which the high \( I_{ON}/I_{OFF} \) ratio is necessary. Graphene FETs require an energy band gap of at least 400 meV to be a promising alternative of Silicon [5]. Both theoretical, and experimental results show that the maximum achievable energy gap induced by electric field in bilayer graphene is about 300 meV. Bilayer graphene was extensively being modelled theoretically and experimentally simulated in [6-9] and is proven to be thermodynamically stable. The bilayer graphene is the only known material having a tunable band gap. Therefore, bilayer graphene offers possibilities of designing novel types of 2D FET devices inaccessible with the use of conventional semiconductor based 2D. The bandgap opening in bilayer graphene by vertical symmetry breaking has been achieved in two main flavors; either by creating a transverse electric field between the layers, i.e., electrostatic gating, or by external dopants. Hence, controllability of implant dopants in graphene channel becomes an important design consideration of Bi-GFETs to widen the gap between \( I_{ON} \) and \( I_{OFF} \) for better power consumption. Taguchi method has become a useful tool to improve the productivity during research and development. Taguchi method has been proven to produce high quality products in a short period of time and at the lowest cost [10]. Salehuddin et al. (2012) proved that Taguchi method was able to identify the process parameters which have the strongest effect on the response characteristics [11]. The threshold voltage (\( V_{TH} \)) of MOSFET device was then optimized closer to ITRS specification by adjusting an adjustment factor [12]. Afifah Maharan et al. (2013) had utilized Taguchi method to reduce variation of threshold voltage (\( V_{TH} \)) in High-k/Metal gate MOSFET. The best settings of the process parameters were determined by using analysis of variance (ANOVA). The process parameters which had least variance and most mean value were adjusted to be in line with the desired value. This paper attempts to describe the simulation design and modeling of four process parameters which are known as halo implant dose, halo implant energy, S/D implant dose and S/D implant energy with halo implant tilt angle and source/drain (S/D) implant tilt angle as the noise factors for obtaining the highest value of \( I_{ON}/I_{OFF} \) ratio of the proposed 10nm gate length semi-analytical Bi-GFET.

2. Process Simulation

A 10nm planar n-channel Bi-GFET was simulated using ATHENA module of Silvaco TCAD tools. The initial step was to deposit aluminum as a backgate of the device. Next, the 20nm thickness of buried oxide (BOX) layer was developed on the top of the backgate. The BOX was used in order to control junction leakage, thereby mitigating short channel effects (SCEs) [13]. Then, the 7nm thickness of silicon was deposited on top of the BOX. The silicon substrate was doped with 7 x 10\(^{14}\) atom/cm\(^3\) of boron. The thin silicon under the channel was fully depleted of mobile charges to avoid the floating body effect. The gate oxide (SiO\(_2\)) was growth at temperature of 815°C. The doped bilayer graphene was growth on the top of SiO\(_2\) using a conformal method. For this study, the doped bilayer graphene is assumed to be have no defects and operate at the ballistic transport [14], thereby the channel width is neglected. The high-k dielectric material used in this study is hafnium dioxide (HfO\(_2\)). The 1nm thickness of HfO\(_2\) was then deposited on the top of bilayer graphene, followed by 10nm gate length (Lg) of tungsten silicide (WSi\(_x\)). The metal-gate workfunction of 4.5eV was applied to the WSi\(_x\) gate [15]. The correct metal-gate workfunction was required to be tuned in order to stabilize the \( V_{TH} \) characteristic. The halo implant process was then performed by doping the substrate with 1.95 x 10\(^{13}\) atom/cm\(^3\) of indium at 170 keV and tilted at 22º. Halo doping is necessary for the ultra-small transistors to reduce the SCEs. The process was then followed by nitride spacer deposition. The S/D implant was performed by implanting arsenic with the dose of 1.63 x 10\(^{14}\) atom/cm\(^3\) at 13 keV and tilted at 7º. This process allows the accumulation of the Schottky tunneling of the S/D region that allow only electrons or holes being injected into the bilayer
graphene channel. The aluminum layer was deposited on the top structure’s surface and any unwanted aluminum was etched to develop the contacts. Figure 1 shows the detailed flowchart of 10nm Lg of Bi-GFET development via ATHENA module of Silvaco TCAD tools. The completed cross section of 10nm Lg of n-channel Bi-GFET is depicted in Figure 2.

ITRS 2015 has predicted that the threshold voltage ($V_{TH}$) for the 19 nm gate length is within 0.461V to 0.510V [18]. The physical modelling of the nano-scaled device is acquired through simulation using Silvaco TCAD. Orientation of <100> is used in this design’s main substrate which is a P-type silicon alongside an oxide layer grown on the top of the silicon bulk. By doing so, it acts as a mask during the P-well implantation process. This is followed by an injection of $1 \times 10^{17}$ atom/cm$^3$ of Boron into the silicon substrate. Since the gate terminal can be separated from the source and drain terminal aside from its conductive channel through a dielectric layer, gate oxide is grown at 875°C in the dry oxygen environment in 3% HCL at 1 atmospheric pressure. Meanwhile, the threshold voltage adjustment implantation is implemented in the channel region through approximately $1.95 \times 10^{13}$ atom/cm$^3$ of Boron at an energy of 5 keV. Significant changes can be observed once a slight adjustment being made towards the gate concentration and thus making it suitable to be considered as one of the parameter variations before the ones with most significant changes are opting. Polycrystalline silicon is then deposited on the semiconductor wafer as multi-layered structure is formed through the conformal polysilicon deposition. Meanwhile, as p-type impurities ion is implanted in the substrate that allows the formation of the n-type Source/Drain areas, indium is then doped with $1.17 \times 10^{13}$ atom/cm$^3$ of dose with an implant energy of 1 keV in the halo implantation for which is able to reduce the SCE. The layer of nitride Si$_3$N$_4$ is produced on the surface of the silicon and polysilicon in sidewall spacer production. $1.22 \times 10^{18}$ atom/cm$^3$ of arsenic dose with an implant energy of 3 keV is implanted in order to perform Source/Drain implantation before the side capacitance is minimized through compensate implantation. The first formation of the contact window in the Source/Drain region along with aluminium deposition and patterning has allowed the metallization process to be performed before structure mirroring process and electrode definition is made.
3. Results and Procedures

The electrical characterization of the 10nm n-channel Bi-GFET was performed using an ATLAS module of Silvaco TCAD tools. The optical and electrical properties of the bilayer graphene was predefined in the ATLAS script. The operation was presumed to be executed at room temperature (T=300 K). The bilayer graphene was modeled as a semi-metal with a bandgap of 0.55 eV [16]. The bilayer graphene dielectric constant and effective field (Eeff) were set to 2.4 and 0.4 MV/cm respectively [17]. The graphene’s 2D electron and hole densities of states were measured at room temperature using:

\[ N_C = \frac{8\pi n_e kT}{h^2} \ln(1 + e^{-(E_F-E_C)/kT}) \]  

\[ N_V = \frac{8\pi n_h kT}{h^2} \ln(1 + e^{-(E_F-E_V)/kT}) \]  

The effective masses of electrons and holes in graphene were set \( m_e \approx 0.06 m_0 \) and \( m_h \approx 0.03 m_0 \) where \( m_0 \) is the free electron mass [8,14,18]. Figure 3 shows the contour mode of the proposed Bi-GFET, displaying the tabulation of silicon, WSi\( x \), HfO\( 2 \), bilayer graphene, silicon nitride (Si\( 3 \)Ni\( 4 \)), SiO\( 2 \) and aluminum. The effective channel length (Leff) was observed to be 32nm. Figure 4 depicts the drain current (I\( D \)) versus gate voltage (V\( G \)) curve at drain voltage V\( D \) = 1.0 V for the Bi-GFET. The initial value of I\( ON \), I\( OFF \) and I\( ON \)/I\( OFF \) ratio were observed to be 310.4 µA/µm, 2.501 pA/µm and 1.241 x 10^5 respectively.

![Figure 3. Contour Mode of 10nm n-channel Bi-GFET device](image)

![Figure 4. Graph of subthreshold I\( D \) vs. V\( G \) before optimization](image)

3.1 Selection of the Process Parameters and the Orthogonal Array

The variance decomposition which is the analysis of variance (ANOVA) allows the effect of different process parameter on the output response to be acquired. Meanwhile the percentages of factor effect on S/N ratio indicates the relative power of a factor to reduce variation, that being said the performance is greatly influenced by a factor with high contribution percentage. The optimum condition for all the output responses have been compared to choose the optimization value for the responses due to the percentages
of the factor effect on S/N ratio that indicates the priority of a factor to reduce the variation. The influence of Halo implant dose, halo implant energy, S/D implant dose and S/D implant energy towards $I_{ON}/I_{OFF}$ ratio were investigated in this study. Each of them were represented by alphabetical symbols: A, B, C and D. Two noise factors, halo implant tilt angle and S/D implant tilt angle were utilized to extract four different readings of $I_{ON}/I_{OFF}$ ratio. The value of the process parameters and the noise factors at different levels are listed in Table 1 and Table 2.

| Symbol | Process Parameter | Units  | Level 1  | Level 2  | Level 3  |
|--------|-------------------|--------|----------|----------|----------|
| A      | Halo Implant Dose | atom/cm$^3$ | 1.95E13  | 1.97E13  | 1.99E13  |
| B      | Halo Implant Tilt Angle | keV   | 170      | 172      | 174      |
| C      | S/D Implant Dose  | atom/cm$^3$ | 1.63E14  | 1.65E14  | 1.67E14  |
| D      | S/D Implant Tilt Angle | kev   | 13       | 15       | 17       |

| Symbol | Noise factor | Units | Level 1 | Level 2 |
|--------|--------------|-------|---------|---------|
| U      | Halo Implant Tilt Angle | degree | 22      | 24      |
| V      | S/D Implant Tilt Angle   | degree | 7       | 9       |

The OA of the design of experiments (DoE) totally depends on the sum of degrees of freedom (DF) of the involved process parameters. Since each process parameter consists of three levels of value, the total sum of the DF for the process parameters is equal to eight. Basically, the DF for the OA should be greater than or at least equal to those for process parameters. Hence, the $L_9$ (3$^4$) OA which consists of four columns and nine rows has been selected for this study.

3.2 Signal-to-noise Ratio (SNR) Analysis

The signal-to-noise ratio (SNR) was executed to measure the sensitivity of tested process parameters towards the $I_{ON}/I_{OFF}$ ratio. The aim of SNR analysis is to distinguish the highest SNR among all the experimental $I_{ON}/I_{OFF}$ ratio. The factor (process parameter) with the highest SNR implies that it has a higher signal than the random effects of the noise factors. In this study, the higher-the-better quality characteristic type was selected to achieve the highest possible $I_{ON}/I_{OFF}$ ratio. The SNR (Higher-the-better), $\eta$ are expressed as [19]:

$$\eta = -10 \log_{10} \left[ \frac{1}{n} \sum_{i=1}^{n} \frac{1}{y_i^2} \right]$$

(3)

where $n$ is number of tests and $y_i$ is the experimental values of the $I_{ON}/I_{OFF}$ ratio. Table 3 tabulates the experimental results for the $I_{ON}/I_{OFF}$ ratio and their corresponding SNR using equation (2). Since the experimental design is orthogonal, the effect of each process parameter can be separated out [20]. The SNR (Higher-the-better) for each level of process parameters with an overall mean of SNR were summarized in Table 4.
Table 3. Results for I_{ON}/I_{OFF} Ratio Based on L_9 OA of TAguchi Method

| Exp no | (U_1V_1) (x 10^5) | (U_1V_2) (x 10^5) | (U_2V_1) (x 10^5) | (U_2V_2) (x 10^5) | Mean SNR (Higher-the-better) (dB) |
|--------|------------------|------------------|------------------|------------------|----------------------------------|
| 1      | 1.241            | 1.317            | 3.443            | 3.674            | 3.46E-11 104.61                  |
| 2      | 1.255            | 1.328            | 2.408            | 2.561            | 3.82E-11 104.18                  |
| 3      | 1.402            | 1.493            | 2.830            | 3.027            | 2.98E-11 105.26                  |
| 4      | 1.621            | 1.725            | 4.538            | 4.839            | 2.02E-11 106.95                  |
| 5      | 1.044            | 1.110            | 1.989            | 2.125            | 5.51E-11 102.59                  |
| 6      | 1.552            | 1.643            | 3.180            | 3.378            | 2.43E-11 106.14                  |
| 7      | 1.153            | 1.221            | 3.198            | 3.409            | 4.02E-11 103.96                  |
| 8      | 2.173            | 2.314            | 4.355            | 4.637            | 1.24E-11 109.05                  |
| 9      | 1.292            | 1.373            | 2.631            | 2.812            | 3.50E-11 104.56                  |

Table 4. SNR of each level of Process Parameters

| Process Parameter | SNR (Higher-the-better) in dB | Overall mean SNR (dB) |
|-------------------|-------------------------------|-----------------------|
|                   | Level 1 | Level 2 | Level 3 |
| A                 | 104.68  | 105.23  | 105.86  | 105.26                  |
| B                 | 105.17  | 105.27  | 105.32  |                         |
| C                 | 106.60  | 105.23  | 103.94  |                         |
| D                 | 103.92  | 104.76  | 107.09  |                         |

Figure 5 shows the SNR response graph for the I_{ON}/I_{OFF} ratio. The higher the SNR of a process parameter is, the lower variance will be around the optimal value. From the graph, it is clearly shown that factor A_3, B_3, C_1 and D_3 were the optimum process parameter’s level for the highest I_{ON}/I_{OFF} ratio. However, the relative significance among the process parameters towards the I_{ON}/I_{OFF} ratio are still needed to be distinguished. This will be discussed in the next section using the analysis of variance (ANOVA).

Figure 5. Factor effects graph for SNR (Higher-the-better)

4.2 Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is conducted in order to determine which is the most significant process parameters towards the I_{ON}/I_{OFF} ratio. Table 5 shows the results of pooled ANOVA for I_{ON}/I_{OFF} ratio. The F-ratio was computed based on 95% level of confidence. Based on the results, factor D (S/D implant energy) and factor C (S/D implant dose) were identified as the most dominant process parameters that influenced the I_{ON}/I_{OFF} ratio due to their highest factor effect on SNR, 56% and 37% respectively.
Factor A (halo implant dose) was considered as a significant factor with 7% factor effect on SNR. Finally, factor B (halo implant energy) was considered neutral factors as it did contribute no effect on SNR.

Table 5. Results of ANOVA

| Factor | DF | SSQ | MS | F-value | Factor effect on SNR (%) | Dominant/ Significant/ Neutral |
|--------|----|-----|----|---------|--------------------------|--------------------------------|
| A      | 2  | 2   | 1  | 4       | 7                        | Significant                    |
| B      | 2  | 0   | 0  | 0       | 0                        | Neutral                        |
| C      | 2  | 11  | 5  | 18      | 37                       | Dominant                       |
| D      | 2  | 16  | 8  | 28      | 56                       | Dominant                       |

3.3 Confirmation Test

The 10nm Bi-GFET device was re-simulated using the optimized process parameter’s levels predicted by L9 OA of Taguchi method as listed in Table 6. Table 7 shows the simulation results which indicate that the highest recorded value of $I_{on}/I_{off}$ ratio was $4.811 \times 10^5$ with SNR of 109.09 dB. The optimized $I_{on}/I_{off}$ ratio was the highest among all the SNRs in Table 4, implying that the L9 OA of Taguchi method had successfully optimized all the process parameters. Figure 6 depicts the graph $I_D$ versus $V_G$ at drain voltage $V_D = 1.0$ V after the optimization. It can be observed that the $I_{on}/I_{off}$ ratio was improved by 74.2% if compared to the $I_{on}/I_{off}$ ratio before the optimization in Figure 4.

Table 6. Optimized Process Parameters Predicted using L9 OA of Taguchi method

| Symbol | Process Parameter      | Units      | Best Value |
|--------|------------------------|------------|------------|
| A      | Halo Implant Dose      | atom/cm$^{-3}$ | 2.89E13    |
| B      | Halo Implant Tilt Angle| degree     | 24         |
| C      | S/D Implant Dose       | atom/cm$^{-3}$ | 2.27E18    |
| D      | S/D Implant Tilt Angle | degree     | 77         |

Table 7. Confirmation results for $I_{on}/I_{off}$ ratio using L9 OA of Taguchi Method

| $I_{on}/I_{off}$ ratio | SNR (Higher-the-better) in dB |
|------------------------|--------------------------------|
| (U1V1)                 | 2.165E5                        |
| (U1V2)                 | 2.305E5                        |
| (U2V1)                 | 4.520E5                        |
| (U2V2)                 | 4.811E5                        |
|                        | 109.09                         |

Figure 7 depicts the comparison of $I_{on}/I_{off}$ ratio of Bi-GFET with other research results [7,21,22]. It is observed that the $I_{on}/I_{off}$ ratio can be optimized by utilizing the L9 OA of Taguchi method. It can be concluded that the external dopant profiles in the graphene channel can be modeled via Taguchi method in order to achieve higher $I_{on}/I_{off}$ ratio of the Bi-GFET.
4. Conclusion

As conclusions, the $I_{ON}/I_{OFF}$ ratio of 10nm n-channel Bi-GFET has successfully been optimized by using $L_0$ OA of Taguchi method. The most significant process parameters identified from the ANOVA method were S/D implant energy and S/D implant dose with 56% and 37% factor effects on SNR accordingly. The highest $I_{ON}/I_{OFF}$ ratio resulted from the $L_0$ OA of Taguchi method was $4.811 \times 10^5$. There was a significant improvement of 74.2% compared to the $I_{ON}/I_{OFF}$ ratio before the optimization. The final results have proved that the $L_0$ OA of Taguchi method is capable of finding the robust dopant profiles in the graphene channel for higher $I_{ON}/I_{OFF}$ ratio of 10nm Bi-GFET device. For future work, several more process parameters will be added in the statistical model in order to further increase the $I_{ON}$ characteristic of the device.

5. References

[1] I. Ferain, C. A. Colinge, and J. Colinge 2011 Multigate Transistors as the Future of Classical Metal-oxide-semiconductor Field-effect Transistors Nature vol. 479 pp 310–316
[2] F. Schwierz 2010 Graphene transistors Nat. Publ. Gr. vol. 5 no. 7 pp 487–496
[3] K. S. Novoselov, A. K. Geim, S. V. Morosov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov 2004 Electric Field Effect in Atomically Thin Carbon Films Science (80 ) vol. 306 pp 666–669
[4] A. K. Geim and K. S. Novoselov 2007 The Rise of Graphene Natural Material vol. 6 p 183
[5] C. Nanmeni Bondja, Z. Geng, R. Granzner, J. Pezoldt, and F. Schwierz 2016 Simulation of 50-nm Gate Graphene Nanoribbon Transistors Electronics vol. 5 p 3
[6] M. Cheli, G. Fiori, and G. Iannaccone 2009 A semianalytical model of bilayer-graphene field-effect transistor IEEE Trans. Electron Devices vol. 56 no. 12 pp 2979–2986
[7] F. W. Chen, H. Ilatikhameneh, G. Klimeck, R. Rahman, T. Chu, and Z. Chen 2015 Achieving a higher performance in bilayer graphene FET - Strain engineering in International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2015) no. September pp 177–181
[8] Faizah Z. A. N., I. Ahmad, P. J. Ker, and P. S. Menon 2016 Process Characterization of 32nm Semi Analytical Bilayer Graphene-based MOSFET in MATEC Web of Conferences vol. 78 pp 1–6
[9] Wessely P. J., F. Wessely, E. Birinci, B. Riedinger, and U. Schwalke 2013 Transfer-free grown bilayer graphene transistors for digital applications Solid. State. Electronics vol. 81 pp 86–90

[10] Mohammad N., F. Salehuddin, H. A. Elgomati, I. Ahmad, N. A. A. Rahman, M. Mansor, Z. Mansor, K. E. Kaharudin, A. S. M. Zain, and N. Z. Haron 2013 Characterization & Optimization of 32nm P-Channel MOSFET Device J. Telecommun. Electron. Comput. Eng. vol. 5 no. 2 pp 49–54

[11] Salehuddin F., I. Ahmad, F. A. Hamid, A. Zaharim, A. M. A. Hamid, P. S. Menon, H. A. Elgomati, B. Y. Majlis, and P. R. Apte 2012 Optimization of process parameter variation in 45nm p-channel MOSFET using L18 orthogonal array in 2012 10th IEEE International Conference on Semiconductor Electronics (ICSE 2012) pp 219–223

[12] Salehuddin F., I. Ahmad, F. A. Hamid, A. Zaharim, U. Hashim, and P. R. Apte 2011 Optimization of input process parameters variation on threshold voltage in 45 nm NMOS device Int. J. Phys. Sci. vol. 6 no. 30 pp 7026–7034

[13] Suseno J. E. and Ismail R 2012 Design of Double Gate Vertical MOSFET using Silicon On Insulator ( SOI ) Technology Int. J. Nano Devices, Sensors Syst. vol. 1 no. 1 pp 34–38

[14] N. F. Z. A, I. Ahmad, P. J. Ker, and P. S. Menon 2016 Transistor Characteristics of Semi Analytical 14 nm Gate Length Bi- GNMOS J. Fiz. Malaysia vol. 37 no. 1 p 2016

[15] Hong Z., A. Bodkhe, and S. Tzeng 2014 Method for Forming A Low Resistivity Tungsten Silicide Layer for Metal Gate Stack Applications

[16] Nemes-Ince P., Z. Osváth, K. Kamarás, and L. P. Biro 2008 Anomalies in thickness measurements of graphene and few layer graphite crystals by tapping mode atomic force microscopy Carbon N. Y. vol. 46 pp 1435–1442

[17] Guo B., L. Fang, B. Zhang, and J. R. Gong 2011 Graphene Doping: A Review Insciences J. vol. 1 no. 2 pp. 80–89.

[18] Ferrari C., J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and a. K. Geim 2006 Raman spectrum of graphene and graphene layers Phys. Rev. Lett. vol. 97 December 2006

[19] M. S. Phadke 2001 Quality Engineering Using Robust Design. Pearson Education

[20] Kaharudin K. E., F. Salehuddin, A. S. M. Zain, M. N. I. A. Aziz, and I. Ahmad 2016 Application of Taguchi Method with the Interaction Test for Lower DIBL in WSi x /TiO 2 Channel Vertical Double Gate NMOS ARPN J. Eng. Appl. Sci. vol. 11 no. 11 pp 7093–7103

[21] Majumdar K., K. V. R. M. Murali, N. Bhat, F. Xia, and Y. M. Lin 2010 High on-off ratio bilayer graphene complementary field effect transistors Tech. Dig. - Int. Electron Devices Meet. IEDM pp 736–739

[22] Verma J 2016 Graphene based tunnel FET Int. Res. J. Eng. Technology vol. 3 no. 4 pp 2525–2528

Acknowledgments
The authors would like to thank to the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE, CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.