Non-binary digital calibration for split-capacitor DAC in SAR ADC

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Abstract: A non-binary digital calibration scheme is proposed for split-capacitor digital-to-analog converter (DAC) in successive approximation register (SAR) analog-to-digital converter (ADC). This calibration scheme improves linearity without additional analog circuits and relaxes the requirement of the comparator offset. Furthermore, it allows bigger settling error for each capacitor in MSB array in normal operation. It is utilized in the design of a 10b 50 MS/s SAR ADC in 65 nm CMOS technology with the calibration circuitry integrated. Measurement results show a peak SNDR of 56.2 dB, while consuming 0.82 mW from 1.2 V supply. The FOM is 31.1 fJ/conv.-step and the ADC occupies 0.057 mm² active area, which proves the proposed scheme compared with our previous work without calibration.

Keywords: SAR, split-capacitor DAC, redundant capacitor, digital calibration

Classification: Integrated circuits

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1 Introduction
In medium-to-high-resolution successive approximation register (SAR) analog-to-digital converter (ADC), the split-capacitor digital-to-analog converter (DAC) is
preferable due to significant area reduction of the capacitive digital-to-analog converter (DAC). However, this structure suffers from the non-linearity problem resulted from parasitic capacitor in the top plate of least significant bit (LSB) array, across the bridge capacitor, and mismatch of the bridge capacitor [1].

Several calibration schemes have been presented [2, 3] to solve this problem. An analog calibration scheme is presented in [2], in which a programmable capacitor array is used to adjust the total weight of the LSB array, and a comparator with offset-cancelation is required to guarantee correct capacitive DAC calibration. In [3], a digital calibration is presented, in which the margin of the parasitic capacitance on the LSB top plate is very stringent due to the traditional split-capacitor DAC. That digital calibration scheme requires a offset-cancelation comparator, too.

In this work, a non-binary digital calibration scheme is proposed. It resolves the nonlinearity problem due to parasitic capacitor in the top-plate of LSB array, across the bridge capacitor, and mismatch of the bridge capacitor. It also relaxes the requirement of the comparator offset and gives bigger tolerance for DAC settling error for each capacitor in most significant bit (MSB) array. A comparator without offset-cancelation is used in this work, which benefits designs that operate at higher sampling rate.

2 Proposed digital calibration scheme

A split-capacitor DAC is depicted in Fig. 1(a), which is composed of L-bit LSB array, M-bit MSB array, and a bridge capacitor \(C_b\). In [1] \(C_b\) is chosen to be one unit capacitor. Let’s denote the top-plate of MSB array as \(V_M\), and the top plate of LSB array as \(V_L\). In Fig. 1(a) \(C_{PM}, C_{PB},\) and \(C_{PL}\) are the parasitic capacitors in node \(V_M\), across the bridge capacitor \(C_b\), and in node \(V_L\), respectively. The random mismatch of \(C_b\) and the parasitic capacitor \(C_{PB}\) and \(C_{PL}\) deteriorate linearity of the capacitive DAC.

In the proposed calibration scheme, each bit in MSB array is multiplied by an equivalent weight instead of binary weight \(2^L\). In Fig. 1(b), \(C_r\) and that 0.5\(C_u\) are redundant capacitors. That 0.5\(C_u\) is used to reduce digital truncation error. It is similar to the traditional pipeline calibration [4], thus the max DNL is 0.5 least significant bit (LSB). The equivalent weight of one unit capacitor in MSB array is found in Eq. (1).

\[
C_u = \frac{wC_u(C_b + C_{PB})}{(2^L - 0.5)C_u + C_r + C_b + C_{PL} + C_{PB}}
\]

It derives into

\[
w = \frac{C_{LSB} + C_B}{C_B}
\]

where \(C_{LSB} = (2^L - 0.5)C_u + C_r + C_{PL}\), and \(C_B = C_b + C_{PB}\).

The equivalent weight of one unit capacitor in MSB array, \(w\), must not be less than \(2^L\) to guarantee the resolution of ADC.

\[
(2^L - 1)C_B \leq C_{LSB}
\]
In calibration, the equivalent weight $w$ is found. As shown in Fig. 2(a), node $V_M$ is disconnected from the input $V_{IN}$, the bottom plate of all capacitors are connected to $V_{cm}$, the switch $S_1$ are close. Then switch $S_1$ are open and the bottom-plate of $C_u$ in MSB array is connected to $V_{DD}$ as shown in Fig. 2(b). Now the voltage contribution of $C_u$ in MSB array to node $V_M$ is measured using LSB array. The voltage of node $V_M$ is compared with $V_{cm}$. The corresponding bit is set to 1 and the capacitor is connected to $GND$ if the comparator output is one. The corresponding bit is set to 0 and the capacitor is connected to $V_{DD}$ if the comparator output is zero. This procedure is repeated for the capacitors from right to left one by one in LSB array. Then the weight code of one unit capacitor in MSB array is retrieved. Since the comparator has a offset $V_{OS}$ as shown in Fig. 2(b), the measured weight code is

$$w_p = \frac{C_{LSB} + C_B}{C_B} + \frac{V_{OS}}{V_{DD}} \frac{C_{MSB}C_{LSB} + C_{MSB}C_B + C_BC_{LSB}}{C_u C_B}$$ (4)

where $C_{MSB} = (2^M - 1)C_u + C_{PM}$.

One more weight code $w_n$ in (6) is acquired with similar method, but those switches in DAC array is connected as shown in Fig. 2(c) instead of Fig. 2(b).

$$w_n = -\frac{C_{LSB} + C_B}{C_B} + \frac{V_{OS}}{V_{DD}} \frac{C_{MSB}C_{LSB} + C_{MSB}C_B + C_BC_{LSB}}{C_u C_B}$$ (5)

Obviously, the weight code $w$ of $C_u$ in the MSB array is half of the difference of $w_p$ and $w_n$.

$$w = 0.5(w_p - w_n)$$ (6)

In order to measure the equivalent weight of one unit capacitor in MSB array, $w_p$ and $w_n$ must be measured correctly when the comparator has offset as shown in Fig. 1.

Fig. 1. Split-capacitor digital-to-analog converter (DAC)
(a) Split-capacitor DAC with parasitic capacitors
(b) Split-capacitor DAC with redundant capacitor and parasitic capacitors.
Fig. 2. Obviously, \(|w_p|\) and \(|w_n|\) cannot be greater than the number of unit capacitors in LSB array excluding \(C_{PL}\).

\[ |w_p| \leq \frac{C_{LSB} - C_{PL}}{C_u} \]  

Substitute Eq. (4) into Eq. (7), it derives into

\[ |V_{OS}| \leq V_{DD} \frac{(C_{LSB} - C_{PL} - C_u)C_B - C_{LSB}C_u}{C_{MSB}C_{LSB} + C_{MSB}C_B + C_BC_{LSB}} \]  

Because \(|V_{OS}| \geq 0\),

\[ C_B \geq \frac{C_{LSB}C_u}{C_{LSB} - C_{PL} - C_u}. \]  

Thus \(C_B\) needs to be greater than \(C_u\). Calculate \(C_{PL}\) from Eq. (9),

\[ C_{PL} \leq (C_B - 1)(2^L - 0.5) + C_t - C_u. \]  

Given \(C_B\) and \(C_t\), the maximum allowed value of \(C_{PL}\) is determined by Eq. (10).

In normal operation, the effective redundant capacitance in LSB array is

\[ C_{teff} = (C_{LSB} - C_{PL} - wC_u) \frac{C_B}{C_{LSB} + C_B}. \]
Substituting Eq. (2) into Eq. (11) gives

\[
C_{\text{r,eff}} = \frac{(C_{\text{LSB}} - C_{\text{PL}})C_{\text{B}}}{C_{\text{LSB}} + C_{\text{B}}} = C_u. \tag{12}
\]

The voltage contribution of \(C_{\text{r,eff}}\) to node \(V_M\) decides the maximum allowed DAC settling error \(V_{\text{err}}\) when the bottom-plate voltage of capacitors in MSB array toggle.

\[
V_{\text{err}} = V_{\text{DD}} \frac{C_{\text{err}}}{C_{\text{MSB}} + \frac{C_{\text{LSB}}C_{\text{B}}}{C_{\text{LSB}} + C_{\text{B}}}} \tag{13}
\]

Substituting Eq. (12) into Eq. (13) gives

\[
V_{\text{err}} = V_{\text{DD}} \frac{(C_{\text{LSB}} - C_{\text{PL}} - C_u)C_{\text{B}} - C_{\text{LSB}}C_u}{C_{\text{MSB}}C_{\text{LSB}} + C_{\text{MSB}}C_{\text{B}} + C_{\text{B}}C_{\text{LSB}}} \tag{14}
\]

\(V_{\text{err}}\) in Eq. (14) is equal to \(V_{\text{OS}}\) in Eq. (8). The DAC settling error when the bottom-plate voltage of capacitors in MSB array toggle can be corrected if it is not greater than \(V_{\text{OS}}\) in Eq. (8). Thus the capacitor DAC settling time is shortened, which is beneficial to the ADC conversion speed [5].

### 3 Behavioral simulation

A 10-bit SAR ADC prototype is shown in Fig. 3, adopting 5-bit MSB array and 4-bit LSB array. It is implemented in a split-capacitor \(V_{\text{cm}}\)-based cap-switching scheme to reduce the switching energy [1]. The most significant bit of capacitor DAC is split into a binary array to reduce power consumption [1]. The bridge capacitor \(C_{\text{B}}\) is equal to 1.5\(C_u\) instead of conventional \(C_u\), and the redundant capacitor \(C_{\text{r}}\) is equal to 8\(C_u\). According to Eq. (10), the maximum allowed \(C_{\text{PL}}\) is 10\(C_u\) in order to keep max DNL less than 0.5 LSB with the proposed calibration scheme. Behavioral simulation result is shown in Fig. 4 to Fig. 6. In Fig. 4, max DNL is not greater than 0.5 LSB due to the digital truncation error if \(C_{\text{PL}}\) is not greater than 10 \(C_u\). The relation of dynamic performance to \(C_{\text{PL}}\) is shown in Fig. 5, which is acquired with 65536-point FFT. Signal-to-noise and distortion ratio (SINAD) is greater than 61 dB if \(C_{\text{PL}}\) is not greater than 10 \(C_u\). The relation of max allowed comparator offset \(V_{\text{OS}}\) to \(C_{\text{PL}}\) is shown in Fig. 6. The curve in Fig. 6 is the max allowed settling error \(V_{\text{err}}\) of each capacitor in the MSB array, too. If \(C_{\text{PL}}\) is greater than 10 \(C_u\), the calibration scheme is no longer effective, just as the aforementioned analysis. Simulation proves the proposed scheme, which greatly enlarges the margin on the parasitic capacitors and mismatch of the bridge capacitor in a split-capacitor DAC. The proposed scheme relaxes the requirement on the input referred offset of the comparator. It is feasible to adopt a comparator without offset cancelation in split-cap SAR ADC now.
4 Implementation and measurement results

The prototype is fabricated in a 65 nm CMOS process with MIM capacitors. Fig. 7 shows the chip micrograph and a zoomed view of the ADC core, which occupies 260 × 220 µm² with the calibration circuitry occupying 0.003 mm² only. Fig. 8 shows the DNL and INL of 0.60LSB and 1.16LSB, respectively. Fig. 9 and Fig. 10 show the measured dynamic performance at 50 MS/s, indicating 80 MHz ERBW and 56.2 dB peak SINAD. This ADC consumes 0.82 mW from 1.2 V supply. It achieves the FOM of 31.1 fJ/conv.-step.

Table I compares this work with other state-of-the-art split-CDAC ADCs [1, 2, 3]. The FOM of this work is better than those of other calibrated CDAC ADCs [2, 3]. It shows a great improvement in both dynamic and static performance at a little expense of speed due to the redundant steps, compared with our previous work [1], which adopts the same unit capacitor and sub-circuits without calibration. Demonstrated by the 10-bit ADC in this paper, the proposed scheme alleviates the nonlinearity problem of the split-CADC in SAR ADCs successfully.
Fig. 7. Chip micrograph.

Fig. 8. Measured DNL and INL at 50 MS/s.

Fig. 9. Measured 65536-point output spectrum with 10.8 MHz input at 50 MS/s.

Fig. 10. Measured dynamic performance vs. input frequency at 50 MS/s.
5 Conclusion

A digital calibration scheme with redundant capacitors in LSB array is proposed. It overcomes nonlinearity due to the parasitic capacitors on the top plate of LSB array, across the bridge capacitor, and mismatch of the bridge capacitor. When the bridge capacitance is greater than one unit capacitance, the tolerance of maximum parasitic capacitance on the top-plate of LSB array is greatly relaxed. The comparator is not required to cancel offset in order to calibrate accurately. Only if the parasitic capacitance on the top-plate of LSB array is less than the maximum allowed value, this capacitive DAC structure can operate with bigger settling error for each capacitor in MSB array.

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Table I. Comparison with the state-of-the-art results

| Specifications       | [2] | [3]   | Previous [1] | This work |
|----------------------|-----|-------|--------------|-----------|
| Technology (nm)      | 65  | 130   | 65           | 65        |
| Supply Voltage (V)   | 1.2 | 0.5   | 1.2          | 1.2       |
| Sampling Rate (MS/s) | 50  | 0.01  | 70           | 50        |
| Resolution (bit)     | 8   | 11    | 10           | 10        |
| Unit Cap (fF)        | 11  | 100   | 15           | 15        |
| SNDR (dB)            | 45.6| 61.8  | 53.2         | 56.2      |
| ENOB (bit)           | 7.3 | 9.93  | 8.54         | 9.04      |
| INL/DNL (LSB)        | 0.3/0.3| 0.98/0.97| 1.65/1.01| 1.16/0.60 |
| FOM (fJ/conv.step)   | 232 | 74.8  | 36.8         | 31.1      |
| Active Area (mm²)    | 0.03| 0.582 | 0.048        | 0.057     |