High Step-up Voltage Gain Converter with Ripple-free Input Current for Renewable Energy Sources

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Abstract: High step-up voltage gain nonisolated DC-DC converter have attracted much attention in photovoltaic, fuel cells and other renewable energy system applications. In this paper, by combining input current ripple-free boost cell with coupled-inductor voltage-doubler cell, an input current ripple-free high voltage gain nonisolated converter is proposed. In addition, passive lossless clamp circuit is adopted to recycle the leakage inductor energy and to reduce the voltage spike across the power switch. By utilizing voltage-doubler cell consisting of diode and capacitor, the voltage stress of switch is further reduced and the resonance between the leakage inductor and the stray capacitor of the output diode is eliminated. A low switch-on-resistance low-voltage-rated MOSFET can therefore be employed to reduce the conduction loss and cost. The reverse recovery loss of output diode is reduced, and the efficiency of converter can be improved. Furthermore, the proposed converter can achieve nearly zero input current-ripple and make the design of electromagnetic interference (EMI) filter easy. Steady state analysis and operation mode of the converter is performed. Finally, experimental results are presented to verify the analysis results of the proposed converter.

Keywords: input current ripple-free; boost converter; coupled-inductor; voltage-doubler cell; passive lossless clamp circuits; high voltage gain; renewable energy

1. Introduction

With the exhaustion of the global resources and the environmental pollution, the research on the renewable energy sources [1-7] such as fuel cells and photovoltaic cells has been gradually increased in industrial fields. Generally, the renewable energy sources generate low-voltage energy, thus power conditioning system (PCS) for renewable energy sources are required to regulate the output voltage for commercial, industrial, residential application. A typical renewable energy conversion system [8-10] is shown in fig.1, frond-end dc-dc converter is used to get high voltage dc bus for utility grid. In this application, Boost converter[11] can provide high dc voltage gain when operates at extremely high duty cycle, however, it increases the input current ripple of the converter, the conduction losses and the turned-off losses of power switch. Its transient response is also affected due to narrow turned-off time of power switches. In addition, output diode reverse-recovery problem is serious, which results in large conduction losses of power device and also increases the rating of power devices. Furthermore, the voltage stress of the power switch equals to the output voltage, and hence a high-voltage rating power switch with high on-resistance should be employed, generating high conduction losses. Consequently, the conversion efficiency is degraded and the electromagnetic interference (EMI) problem is severe under this situation.
To achieve a high conversion ratio and to avoid operating at extremely high duty cycles, many nonisolated converter topologies have been studied [1-6,8-18]. By using switched capacitor or switched inductor cell, high voltage gain of converter can be achieved [12-14]. However, it makes the switch suffer from high transient current and large conduction losses. Furthermore, many switched capacitor or switched inductor cells are indispensable to obtain extremely high step-up conversion, which increases the circuit complexity. Quadratic boost converter [15] using a single active switch is another interesting topology for extending the voltage gain, where the voltage conversion ratio is given as a quadratic function of the duty ratio. However, the voltage gain of this converter is moderately since the output voltage level is determined only by the duty cycle, and due to the cascade structure, it causes lower efficient of the converter.

The coupled inductor or isolated transformer-based converters [3,4,9,15-19] are other solutions to realize high step-up gain, where the turns ratio of the coupled inductor can be employed as a design freedom to extend the voltage gain. However, the inherent leakage inductance of the coupled inductor may not only cause high voltage spikes across the switch when it is turned off, but also produce large energy losses. A resistor–capacitor–diode (RCD) snubber circuit can suppress the voltage stress of the power switch, but the leakage energy is dissipated. Also, active clamp scheme or passive clamp circuit are utilized to recycle the leakage inductor energy and absorb voltage spike of the power switch [18]. Unfortunately, the input current of coupled inductor-based converter is discontinuous. Specially, as the turn ratio of the coupled-inductor or tapped-inductor is increased to extend the voltage conversion ratio, the input current ripple becomes larger.

Actually, current harmonics in fuel cell stack or photovoltaics makes the control of maximum efficiency point difficult, and also generates excessive losses and overheating [20,21], i.e. input current ripple of power converter greatly impact its power conversion efficiency. Thus, high boost-ratio converters with continuous input current are highly preferred. Current-fed converter exhibits continuous input current and boost-ratio gain characteristics, reducing the input filter capacitor and conduction loss, thereby enhancing the performance of the converter. By using a mirror ripple circuit, a zero input current ripple Boost converter for fuel cell applications is proposed in [22], however, additional active switch is required, which increases the complexity of the converter. The transformer-less high-gain boost converter proposed in [23] can achieve input current ripple cancelation at a selectable duty cycle. A passive ripple cancelling circuit is proposed in [24]-[26], however, it increase design complexity of magnetic component.

In this paper, a zero input current ripple high voltage gain nonisolated DC-DC converter is presented. By using coupled-inductor cell, high voltage gain of the proposed converter is achieved by adjusting turns ratio of coupled-inductor. To relieve voltage spikes of the power switch induced by leakage inductor of coupled inductor, a passive lossless snubber circuit with a diode and a capacitor is utilized, and the leakage inductor energy is also recycled. In addition, voltage-doubler cell is used to further extend voltage gain of converter to avoid operating at extremely duty cycle. Furthermore, voltage oscillations of the output diode due to resonance of parasitic capacitance of output diode and secondary leakage inductance of coupled inductor are eliminated.

The paper is organized as follows. In Section 2, operating mode of the proposed converter is discussed. The operating characteristics analysis, i.e. the condition of input current ripple-free, the input-output voltage gain ratio, the voltage stress, and the performance comparison, are performed in Section 3. Experimental results are given in Section 4 and the conclusion is given in Section 5.
2. Operating principle of the proposed converter

2.1. Circuit description

Fig. 2(a) shows the proposed input current ripple-free high voltage gain nonisolated converter with voltage-doubler cell and coupled inductor, with its corresponding equivalent circuit as shown in Figure 2(b). In Fig.2 (b), the coupled inductor is modeled by an ideal transformer with turns ratio of np: ns =1:n, a magnetizing inductor \( L_m \) and a leakage inductor \( L_s \). Passive lossless clamp circuit, consisting of diode \( D_c \) and capacitor \( C_c \), is utilized to recycle leakage inductor energy and absorb voltage spike of switch \( S_1 \) when switch \( S_1 \) is turned-off. The coupled inductor voltage-doubler cell consists of secondary of ideal transformer, capacitor \( C_2 \) and regenerative diode \( D_1 \). The voltage-doubler cell, consisting of capacitor \( C_2 \) and diode \( D_1 \), can further enhance the voltage gain and reduce voltage stress across switch \( S_1 \) and output diode \( D_o \). \( C_1 \) is intermediate storage capacitor, \( L_a \) is input filter inductor, \( C_o \) is output filter capacitor and \( R_o \) is load resistance. To simplify the analysis, following assumptions are made:

a) Power switch \( S_1 \) is ideal except its anti-paralleled diode and output capacitor;

b) Capacitors \( C_1, C_2 \) and \( C_o \) are so large that voltages \( V_{c1}, V_{c2} \) and \( V_o \) can be considered as constants in a switching cycle.

\[ V_{c1} - V_{c2} + V_o = 0 \]

2.2 Operating Mode Analysis

Fig. 2(a) shows the proposed input current ripple-free high voltage gain nonisolated converter with voltage-doubler cell and coupled inductor. There are seven main subintervals during one switching cycle. The key waveforms are shown in Fig. 3 and the corresponding equivalent circuits for each operation mode are shown in Fig. 4. At the beginning of each switching cycle, magnetizing inductor current \( i_m \) is greater than zero and output diode \( D_o \) is conducted to provide freewheeling current path.

Mode 1 [\( t_0 \sim t_1 \)]: At \( t_0 \), driving pulse \( V_{gs1} \) is applied to switch \( S_1 \), the parasitic capacitor of switch \( S_1 \) resonant with leakage inductor of coupled-inductor to discharge energy to the load through capacitor \( C_1 \). Output diode \( D_o \) is conducted to provide the path for magnetizing inductor current \( i_m \). Diode \( D_o \) is turned off and capacitors \( C_2 \) and \( C_o \) transfer energy to the load through output diode \( D_o \). The time interval of this mode is very short as capacitance of \( C_{c1} \) is very small.

Mode 2 [\( t_1 \sim t_2 \)]: At \( t_1 \), parasitic capacitor of switch \( S_1 \) is discharged completely and \( S_1 \) is turned on. At the same time, current flowing through output diode \( D_o \) is great than zero and \( D_o \) is still conducting. This mode ends when the current \( i_{do} \) flowing through output diode decreases to zero.

Mode 3 [\( t_2 \sim t_3 \)]: At time \( t_2 \), output diode current \( i_{do} \) falls to zero, and output diode \( D_o \) is turned off at zero current. At the same time, the secondary current of coupled-inductor \( i_s \) decreases to zero and...
diode $D_1$ is turned on to provide current flowing path for $i_s$. Secondary voltage of coupled-inductor is clamped to $V_{c2}$, magnetizing inductor current $i_m$ increases linearly

$$i_m(t) = i_m(t_2) + \frac{V_{c2}}{nL_1} (t - t_2)$$

(1)

where $n$ is turns ratio of coupled inductor. Leakage inductor current $i_p$ is equal to the current flowing through switch $S_1$

$$i_{s1}(t) = i_p(t) = i_p(t_2) + \frac{V_o - V_{c1} - V_{c2}}{L_s} \frac{t - t_2}{n}$$

(2)

Secondary current of coupled-inductor can be expressed as

$$i_s(t) = -i_{s1}(t) = \frac{i_m(t) - i_p(t)}{n}$$

(3)

Mode 4[$t_3$-$t_4$]: At time $t_3$, switch $S_1$ is turned off, parasitic capacitor of switch $S_1$ is charged and the voltage across power switch increases, and secondary current $i_s$ continues flowing through diode $D_1$. When switch current $i_{s1}$ decrease to zero, this mode ends. The time interval in this mode is very short due to small capacitance of $C_{s1}$.

Mode 5[$t_4$-$t_5$]: At $t_4$, capacitor $C_{s1}$ is charged completely and switch $S_1$ is turned off. In order to provide flowing path for leakage inductor current $i_p$, diode $D_c$ is turned on. At the same time, capacitor $C_c$ is charged by $i_p$. Leakage inductor current $i_p$ decreases linearly

$$i_{s2}(t) = i_p(t) = i_p(t_4) - \frac{V_{c1} + V_{c2}}{L_s} \frac{t - t_4}{n - V_o}(t - t_4)$$

(4)

Voltage $V_{c2}/n$ is applied to inductor $L_1$, which makes $i_m$ increase. The current flowing through the secondary side of coupled inductor decreases rapidly. When diode current $i_{s1}$ decreases to zero, this operation mode ends.

Mode 6[$t_5$-$t_6$]: At $t_5$, $i_{s1}$ decreases to zero, and diode $D_1$ is turned off at zero current, which eliminates the reverse recovery losses of diode $D_1$. At the same time, $i_s$ increases to zero and continue to increase, output diode $D_o$ is conducted to provide current flowing path of $i_s$. Leakage inductor releases energy to capacitor $C_c$ through diode $D_c$. Secondary voltage of coupled inductor is clamped at $V_{c2} + V_{c1} - V_o$, magnetizing inductor current $i_m$ and leakage inductor current $i_p$ can be expressed as

$$i_m(t) = i_m(t_5) - \frac{V_o - V_{c1} - V_{c2}}{nL_1} (t - t_5)$$

(5)

$$i_p(t) = i_p(t_5) - \frac{V_{c1} + V_{c2} + V_{c2} - V_o}{L_s} \frac{t - t_5}{n - V_o}(t - t_5)$$

(6)

When leakage inductor current $i_p$ decreases to zero, this mode ends.

Mode 7[$t_6$-$t_7$]: At $t_6$, leakage inductor current $i_p$ decreases to zero, and then capacitor $C_c$ in series with capacitor $C_s$ transfer energy to the load through output diode $D_o$. Primary magnetizing inductor current $i_m$ is freewheeled through the secondary side of coupled inductor, diode $D_o$, and capacitors $C_c$ and $C_2$. Magnetizing inductor current $i_m$ decreases linearly until the beginning of next switching cycle.
Fig. 3  Operation modes of the proposed converter
3. Performance Analysis

3.1. Condition of ripple-free input current

According to above operation mode analysis in one switching cycle, voltage across input filter inductor $L_a$ can be expressed as

$$ V_{la} = L_a \frac{di_{la}(t)}{dt} = V_i - V_o + V_{c1} $$

(7)

As intermediate storage capacitor $C_1$ and output filter capacitor $C_o$ are so large that their ripple voltages can be neglected, the voltages across $C_1$ and $C_o$ can be considered as constant in one switching cycle. Therefore, the voltage across inductor $L_a$ is almost constant. Furthermore, in order to achieve ripple-free zero input, inductor current $i_{la}$ should remain constant, i.e. $di_{la}/dt = 0$, in this case, the voltage across intermediate capacitor $C_1$ can be expressed as

$$ V_{c1} = V_o - V_{in} $$

(8)

As long as eq. (8) is satisfied, ripple-free input current of the proposed converter can be achieved. It can be seen that for the proposed converter, the ripple-free input current has no relation with the other circuit parameters and the duty cycle [25,26]. Furthermore, the proposed converter has only one power switch, without increases the cost and control complexity. To achieve ripple-free input current, only larger capacitance of capacitor $C_1$ is required.
3.2. Voltage Gain

It can be seen from above analysis that the time interval of mode 1, 2 and mode 4, 5 are so short that their effects on the proposed converter can be ignored in steady-state analysis. Fig. 5 shows the simplified key waveforms, where $D$ is duty cycle of switch $S_1$, $D_1$ is duty cycle of diode $D_c$ and $T_s$ is switching period.

During on-state interval of switch $S_1$, inductor $L_m$ is in series with leakage inductor $L_s$. Let $k = L_m / (L_s + L_m)$, then the voltage across inductor $L_m$ is

$$v_{L1} = kV_{in}$$

Moreover, the voltage across the secondary winding of the ideal transformer can be represented as

$$v_{L2} = nV_{L1} = nkV_{in}$$

![Fig. 5 Simplified waveforms of the proposed converter.](image)

When switch $S_1$ is turned on as shown in the mode 3, the voltage across the secondary winding of the ideal transformer equals to capacitor voltage $V_{C2}$, thus

$$v_{L2} = V_{C2} = nkV_{in}$$

When switch $S_1$ is turned off as shown in the mode 6, the voltages across magnetizing inductor can be denoted as

$$v_{L1} = k(V_{in} - V_{Cc}) = \frac{V_{Cc} + V_{C2} - V_o}{n} = \frac{V_{C2} - V_{C1}}{n + 1}$$

When switch $S_1$ is turned off, diode $D_c$ is turned on to provide current flowing path for leakage inductor current $i_p$, i.e. time interval $[t_4 \sim t_6]$ as shown in Fig.4. In this time interval, leakage inductor current $i_p$ decreases linearly, and output diode current $i_{Do}$ increase linearly. When $i_{Do}$ increases to magnetizing inductor current $i_m$, the energy stored in leakage inductor is released completely and diode current $i_{Do}$ decreases to zero. In the time interval $[t_6 \sim t_7]$, output diode current $i_{Do}$ equals to current flowing through capacitor $C_c$. The duty cycle of diode $D_c$ can be expressed as

$$D_1 = \frac{2}{n + 1}(1 - D)$$

When switch $S_1$ is turned on, voltage across the primary inductor is $V_{C2}/n$; the switch $S_1$ is turned off, magnetizing inductor voltage equals to $(V_{Cc} + V_{C2} - V_o)/n$. According to volt-second balance of inductor $L_m$, it can be seen that

$$\frac{V_{C2}}{n}DT_s + \frac{V_{Cc} + V_{C2} - V_o}{n}(1 - D)T_s = 0$$
From eqs. (8), (11), (12), (14), it can have
\[ V_o = \frac{nk+1}{1-D}V_{in}, \quad V_{c1} = \frac{nk+D}{1-D}V_{in} \]
\[ V_{cc} = -\frac{1}{1-D}V_{in}, \quad V_{c2} = nkV_{in} \]  
(15)

Thus the voltage gain of the converter can be expressed as
\[ M = \frac{V_o}{V_{in}} = \frac{nk+1}{1-D} \]  
(16)

Fig. 6 shows the voltage gain of the proposed converter with \( k = 1 \), and the turns ratio of the transformer as \( n = 1, 3, 5 \). From Fig. 6, with the increase of duty cycle \( D \) and transformer turns ratio \( n \), the voltage gain of the converter increases. Fig. 7 shows voltage gain of the proposed converter with different leakage inductance of coupled inductor. It can be seen from Fig. 7 that with the increase of leakage inductance \( L \), the voltage gain of the converter decreases slightly.

Fig. 6  Gain Curves of the proposed converter at \( k=1 \)

Fig. 7  Gain Curves of the proposed converter at \( n=3 \)

3.3. Voltage Stress on Power Devices

From above operation mode analysis, it can be known that when switch \( S_1 \) is turned off, the voltage stress across power switch is clamped to \( V_{cc} \)
\[ V_{d1,max} = V_{cc} = \frac{1}{1-D}V_{in} \]  
(17)

Voltage stress across diode \( D_o \), \( D_1 \), \( D_c \) can be obtained as
\[ V_{do,max} = V_o - V_{cc} = \frac{nk}{1-D}V_{in} \]  
(18)
\[ V_{D1,max} = V_{Dc,max} = \frac{n k}{1 - D} V_{in} \]  
\[ V_{Dc,max} = V_{Cc} = \frac{1}{1 - D} V_{in} \]

Fig. 8 shows normalized critical voltage stress of the proposed converter with input voltage \( V_{in} \). From Fig. 8, it can be seen that voltage stresses of switch \( S_1 \), capacitor voltage \( C_1 \), \( C_2 \), and diode \( D_o \) are lower than output voltage, although voltage stress of diode \( D_o \), \( D_1 \) is relate to transformer ratio \( n \).

4. Experimental results

4.1. Design Example

In order to verify above analysis results, a experimental prototype is established with the key parameters of the converter as: output power \( P_o = 80W \), input voltage \( V_{in} = 24V \), output voltage \( V_o = 200V \), input inductance \( L_a = 50\mu H \), energy storage capacitor \( C_1 = C_2 = C_c = 4.7\mu F \), output filter capacitor \( C_o = 220\mu F \) and switching frequency \( f_s = 100kHz \).

With these converter parameters, the voltage gain of the converter can be obtained as \( V_o/V_{in} = 200/24 = 8.33 \). As the leakage inductance will decrease the voltage gain of the converter, considering leakage inductance of coupled inductor is less than 5% of magnetizing inductance of the transformer, and high turns ratio produces higher voltage stress of output diode, design the turns ratio of transformer \( n = 2.8 \). According to eq. (16), duty cycle can be obtained as \( D = 0.56 \). The primary magnetizing inductance of the transformer is \( L_1 = 40\mu H \), by selecting ETD34 core, primary and secondary turns ratio of 14T: 40T. Thus, the voltage stress of capacitor \( C_1 \) and \( C_2 \) can be given as \( V_{C1} = 176V \), \( V_{C2} = 72V \), and voltage stress of capacitor \( C_c \) as \( V_{Cc} = 54.5V \). From eqs. (17)-(20), voltage stress of both diode \( D_1 \) and \( D_o \) are 145V, voltage stress of the switch \( S_1 \) is 54.5V. Therefore, switch \( S_1 \) is a MOSFET STP19NF20 (\( VDSS = 200V \), \( RDS (on) = 0.16\Omega \)), the diodes \( D_o \) are STPS3150, and the STTH302 is selected for \( D_1 \) and \( D_o \).

4.2. Experimental Results

Fig.9~Fig.16 show experimental results of the proposed converter at full load. Fig. 9 shows voltage and current waveforms of power switch \( S_1 \). The voltage stress across the switch is about 56V. However, there exists small voltage spike across switch \( S_1 \) due to resonance of parasitic capacitance of the switch \( S_1 \) and diode \( D_1 \). Fig. 10 shows voltage and current waveforms of output diode \( D_o \), it can be seen that the voltage stress of output diode \( D_o \) is clamped to 145V and voltage oscillations of diode voltage is eliminated. Fig.11 illustrates diode current \( i_{D1} \) and the current flowing through capacitor \( i_{Cc} \). Fig. 12 depicts leakage inductor current \( i_L \) and secondary current flowing through coupled inductor \( i_c \). Figs. 13~16 show input current \( i_{in} \), output voltage \( V_o \) and clamped capacitor voltage \( V_{Cc} \), energy-storage capacitor voltage \( V_{C1} \), capacitor voltage \( V_{C2} \), respectively. It can be seen...
from Fig.13 that zero input current ripple of the proposed converter is nearly achieved. Also, the measured voltage stress in Fig.14 − Fig.16 are consistent with the theoretical analysis.

Fig. 9  Voltage and current switch $S_1$

Fig. 10  Voltage and current of diode $D_o$

Fig. 11  Current of passive lossless snubber $D_c$ and $C_c$

Fig. 12  Primary current of the coupled inductor
Fig. 13  Input current $i_L$ flowing through inductor $L$.

Fig. 17 shows efficiency comparison of the proposed zero input current ripple high step-up voltage gain converter and the converter proposed in [12]. It can be seen from Fig.17, the proposed converter in this paper can achieve maximum efficiency of 94.5%, and 94% efficiency at full load. The coupled-inductor-based Boost converter proposed in [12] can achieve maximum efficiency of 93.5%.

The power conversion efficiency improvement of the converter proposed in this paper is achieved due to following reasons: 1) by adjusting turn ratio of coupled-inductor, extreme duty cycle operation can be avoided in the converter proposed in this paper, therefore, improve the efficiency of the converter; 2) by utilizing voltage-doubler cell to extend the voltage gain, the voltage stress of switch is further reduced and the resonance between the leakage inductance and the stray capacitor of the output diode is eliminated. Thus, reverse recovery loss of the output diode $D_o$ can be reduced to improve the efficiency of the converter. In addition, the proposed converter has zero input current ripple, which reduces design complexity of input filter.

Fig. 14  Output voltage and clamped capacitor voltage

Fig. 15  Energy-storage capacitor voltage $V_{C1}$
4. Conclusion

This paper presents an input current ripple-free high voltage gain nonisolated converter with coupled-inductor and voltage-doubler cell. The operating principle and operating characteristics of the proposed converter are analyzed in detail. Experimental results show that the proposed converter has inherent characteristic of zero input current ripple, and turns ratio of the coupled inductor can be employed as another design freedom to extend the voltage gain. Meanwhile, voltage stress of the switch is far less than output voltage, reduce cost and losses. Passive lossless snubber circuit can effectively recycle the leakage inductance energy and absorb voltage spike stress of the switch. In addition, resonance the parasitic capacitance of the output diode with the secondary side leakage inductance is eliminated by using voltage-doubler cell. Thus, the output diode voltage stress is reduced. Based on the above advantages, the proposed converter is suitable for photovoltaic, fuel cells applications.

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