10-bit segmented current steering DAC in 90nm CMOS technology

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Abstract. This special project presents a 10-Bit 1Gs/s 1.2V/3.3V Digital-to-Analog Converter using 1 Poly 9 Metal SAED 90-nm CMOS Technology intended for mixed-signal and power IC applications. To achieve maximum performance with minimum area, the DAC has been implemented in 6+4 Segmentation. The simulation results show a static performance of ±0.56 LSB INL and ±0.79 LSB DNL with a total layout chip area of 0.683 mm². The segmented architecture is implemented using two sub DAC’s, which are the LSB and MSB section with certain number bits. The DAC is designed using 4-Bit Binary Weighted DAC for the LSB section and 6-Bit Thermometer-coded DAC for the MSB section. The thermometer-coded architecture provides the most optimized results in terms of linearity through reducing the clock feed-through effect especially in hot switching between multiple transistors. The binary-weighted architecture gives better linearity output in higher frequencies with better saturation in current sources.

1. Introduction
Data conversion gives the link between the analog world and the digital system and is performed by means of sampling circuits, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs). Such applications like present and future communication systems including high-speed modems and broadband wired and wireless communication subsystems require increasingly higher performance D/A converters. The key issues of these applications are low power consumption, higher conversion rate, high resolution and small die area.

Particularly all the high speed D/A converters are based on the current steering architecture due to its capability of driving resistive loads without buffering. This architecture also provides good static characteristics with reduced power dissipation and area. But the main disadvantage with this architecture is the rapid increase in harmonic distortion caused by the glitches generated from the current switches when the signal frequency is increased.

The current steering architecture can be implemented by either binary or unary architecture. In this paper, an attempt has been made to optimize the segmentation between the unary and binary implementation in this architecture to achieve a good linearity with reduced power and area.

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Furthermore, the so-called segmented current-steering architecture is employed to achieve fast, constant output impedance, and to compensate glitch energy, nonlinearity and overall layout area.

In this project, a design for a 10-bit, 1GS/s segmented current-steering DAC is developed, implemented with a behavioral MATLAB Simulink model and Synopsys Custom design tool. It attempts to show a rigorous analysis of the performance of Segmented DAC architecture.

2. Design architecture

Figure 1 shows the functional block diagram of the proposed project. The DAC is divided into two sub-DACs, which consist of the four least significant bits (LSBs) using binary array current cells and the six most significant bits (MSBs) with thermometer-coded unary array.

![Functional block diagram of 10-bit segmented current-steering DAC.](image1)

Now, the segmented current-steering DAC undergoes through a swatch array which consists of latches, drivers and differential switches. It then undergoes through resistive networks that have been known as a method of providing local interaction between cells with minimum requirement in terms of space and interconnection.

In order to enhance the design of the DAC, modifications are made which include the application of a segmented topology with row and column matrix type array to improve INL and the reduction of the number of cells. The DAC consists of a column and a row decoder: 63 cells for the thermometer-coded DAC, 16 cells for the binary-weighted DAC, switches, latches, level shifters, a bias and clock block.

2.1. Segmented DAC architecture

The design will make use of a commonly used segmented DAC architecture for high resolution which is a hybrid between the binary-weighted and the thermometer-coded DAC. In this N-bit architecture, the M more significant bits are encoded into a thermometer code and the M-N less significant bits are binary weighted. There is a need of an encoder for the MSBs, which takes an M-bit input signal and generates one-bit output signals. When increasing M, the size of the encoder grows exponentially and a larger amount of switches and interconnection is needed.

![An N-bit Segmented DAC where M MSBs are thermometer coded.](image2)
2.2. Percentage of segmentation
A theoretical analysis of method of proper segmentation is presented. A fully binary-weighted design is referred to as 0% segmented, whereas a fully thermometer-coded design is referred to as 100% segmented. This analysis discusses the minimization of the chip area, under the constraints of 10-bit DC performance, while simultaneously trying to optimize the frequency domain performance.

In this present application, 60% segmentation is chosen which implies 6 MSBs are implemented by thermometer coded DAC and 4 LSBs are implemented with binary weighted DAC.

2.3. Binary weighted sub-DAC
The general architecture of a binary weighted current-steering DAC is shown in Figure 3. The switches are controlled by the input bits, where N is the number of bits. B0 is the LSB and the corresponding current source has the DC value ILSB. The source controlled by bit bi, i.e., the i–the LSB current source, is preferably formed by connecting \(2^{-i}\) LSB current sources (unit current sources) in parallel, hence the MSB current source has the DC value IMSB = \(2^{N-1}\)ILSB.

![Figure 3. An N-bit current-steering binary weighted DAC.](image)

2.4. Thermometer-coded subDAC
In the thermometer coded DAC, the reference elements are all equally large and the matching of the individual elements becomes simpler than for the binary case. The total sum of all weights is \(2^N-1\). The transfer function of the thermometer coded converter is monotonic and the DNL and INL is improved compared to the binary version. The requirements on element matching are also relaxed. In fact, if the matching is within a 50% margin, the converter is still monotonic.

In this design 6 MSBs have been implemented by unary architecture, so a thermometer decoder with 6 binary inputs and 63 thermometer coded output is required. For a more systematic design the MSB current sources are implemented in unit current matrix structure, and the thermometer decoder is divided into two parts, a row and a column decoder with each part having 3 inputs and 8 outputs, also called a 3-bit thermometer decoder. Figure 4 shows the logic behind the decoder.

![Figure 4. Thermometer decoder (a)row, (b)column.](image)

3. Matlab behavioural simulation
To understand the behavior of the D/A block, a behavioral model is developed for segmented current-steering DAC using MATLAB SIMULINK® environment. Simulation results confirm the accuracy of the model.
The figure 6 below shows the linear ramp response of both the binary-weighted and the thermometer-coded sub-DACs showing step resolution linearity. Figure 7 shows the reconstructed sinewave output.

4. Cell based implementation using synopsys

4.1. Current source and switch
The basic unit of the DAC is the current cell which is composed of a cascade PMOS which comprises the analog part and a differential switch that uses inversion-mode PMOS varactors to reduce the effect of channel charge, which comprises the digital part. It is very important to test the switch first for its compatibility with the current.
4.2. Voltage bias
Furthermore, all bias voltages and testbench voltages driving the system must be properly defined. The supply voltage for the analog and digital blocks are 3.3 V and 1.2 V, respectively.

![Voltage bias simulation](image)

**Figure 9.** Voltage bias simulation.

4.3. D-latch
D-latches also play a vital role in this project since they are responsible for the synchronization or the timing of the differential switches.

![D-latch simulation](image)

**Figure 10.** D-latch simulation.

The figure above is the simulated D-latch which is used for the whole system. It has delays that vary from 85-150 ps.

4.4. Thermometer decoder
The thermometer decoder, which is divided into row and column, plays an essential part in the thermometer coded sub-DAC. The logic behind the thermometer decoder is different from that of an ordinary decoder. Since the digital inputs pass through this block, it is very important to design this properly.

![3x8 Row Decoder Output](image) ![3x8 Column Decoder Output](image)

**Figure 11.** 3x8 Row Decoder Output.  **Figure 12.** 3x8 Column Decoder Output.
4.5. *Four-bit binary-weighted sub DAC*

Given a pulse input for every bit, the output of the DAC will show a staircase waveform that must have equal time steps. For a 4-LSB binary-weighted DAC shown in Figure 13, the number of steps must be $2^4 - 1 = 15$. For a desired $V_{ref}$ of 1 V, the step size of a 4-bit binary weighted (LSB) must be $1/(2^4-1) = 0.9775$ mV. Therefore, the voltage swing must be $0.9775$ mV multiplied by the number of time steps. Hence, the voltage swing is $0.9775$ mV * 15 = 14.66 mV.

4.6. *Six-bit thermometer-coded sub DAC*

Given a pulse input for every bit, the output of the DAC will show a staircase waveform that must have equal time steps. For a 6-MSB thermometer coded DAC, the number of steps must be $2^6 - 1 = 63$.

Figure 14 gives the staircase waveform for the 6-bit thermometer coded DAC. As observed, it is monotonic with almost negligible glitches and with a voltage swing of approximately 1.04 V. However, for a 6-bit thermometer-coded (MSB) with desired $V_{ref}$ of 1 V, the step size must be $1/(2^{10} - 1)^{2^n}$ where $n$ is the number of bits for the binary-weighted (LSB). Thus, the step size must be $16/1023 = 15.64$ mV. Thus, the voltage swing must be $15.64$ mV * 63 time steps = 0.985 V.

4.7. *Overall 10-bit segmented current-steering DAC output*

Figure 15 shows the total and combined waveform of the 2 sub-DACs. This is now the final output of the 10-bit segmented current-steering DAC with a voltage swing of approximately 1.04 V + 15.2 mV = 1.0552 V.

Figure 16 shows the total reconstructed output with its LSB and MSB components. The LSB output is the same as that of the behavioral model output. The same also goes for the MSB component. The
post-simulation result turns out to be spiky with a maximum glitch of approximately 1.5 mV. This is due mainly by the latch where it is responsible for the switching synchronization and yet it obtained large amount of delay. Another contributing factor of this result is the routing of the MOS, wherein more parasitic capacitances are created by often using 2 consecutive metal types (i.e., metal 1 and metal 2 or metal 2 and metal 3, etc.). Furthermore, the filter design used is only a first order RC filter.

5. Layout floor plan
The layout size is illustrated in the figure below. Including the dummy MOS, the chip layout area is \(0.7179 \times 0.95187 = 0.683 \text{ mm}^2\). Excluding the dummy MOS, the total layout area would be just 0.605 mm\(^2\).

![Design lay-out](image)

**Figure 17.** Design lay-out.

6. References

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