Implementation of Tunable G\textsubscript{m}-C High-pass Filter using Linearized Transconductor

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1. Introduction

Now a day there is an increase demand for higher linear circuits in a wireless communication system. The linear circuit provides better support for wireless communication. To process the signals and remove unwanted block or interferers, the transmitting end and receiving end must consist of highly linearity circuit. A tunable G\textsubscript{m}-C high-pass filter implemented using linearized transconductor circuitry, is proposed in this paper. By employing a dual path feed forward technique, the transconductor circuitry cancels the term G\textsubscript{m3} thus acting a good linear Voltage-to-Current conversion. This design consists of a voltage buffer which uses only inverters, which can drive transconductor with differential inputs. A higher order admittance method is utilized to synthesize the filter. The high pass filter is implemented in 180nm UMC CMOS technology. Further, the harmonic distortion analysis revealed that the input-referred third-order intercept point (IIP3) is +25.84 dBm with a 1-dB compression point being +9.35 dBm. A filter linearity of less than one percent (<1%) shows that the proposed design has better linearity. The simulation results validate that the filter design is highly linear, thus an efficient linearization technique is proposed. Further, this design methodology can be adapted for transconductors having varied differential inputs, and also provides design feasibility for multiple processes.

\textbf{Keywords:} G\textsubscript{m}-C Filter, High Pass Filter, Linearization Technique, Transconductance
component, the aspect ratios and the bias voltage must be fine-tuned to find the best operating point, which results in MGTR sensitivity towards bias variations. On the other hand, linearity can also be enhanced by utilizing feed-forward technique 3. In this paper, any one of the two methods can be employed to actively remove the nonlinearity. In extension, proper scaling ratios must be maintained between the signals of the main and the feed-forward paths to perform the exact cancellation. However, scaling circuitry for both paths is not provided in 3. A technique of attenuation-predistortion 4 also uses main path and auxiliary path for improving the linearity. In this method, the auxiliary path has an attenuated input signal and a digitally adjusted phase shifter. This method overcomes the mismatches and the Process Voltage-Temperature (PVT) variations. Alternatively, an active-RC filter 5 can also be used for achieving good linearity, however, switching capacitors and resistors that controls the cut-off frequency gives a discrete frequency tuning. Another possible avenue of improving the linearity is to employ a basic \( G_m \)-C filter 2. Even though, its linearity lower than active-RC, it can be improved by continuously tuning the bias current. The block diagram of the proposed design is shown in Figure 1.

In this paper, a tunable \( G_m \)-C high-pass filter implemented by using linearized transconductor circuit is proposed.

A feed-forward technique that actively removes the \( G_m \) component of the transconductor is employed in the proposed design. The \( G_m \) cancellation technique is explained in section II. In section III, high-pass filter design which is tunable to various tuning range to achieve linearized transconductor is presented. In section IV, obtained simulation results were discussed and the validated and section V concludes the paper.

2. Linearization Method

Operational transconductance amplifier (OTA) is an essential building block for the design of various analog CMOS circuitry, analog systems, digital systems and signal processing micro-systems. Most of these applications demands highly linear amplifiers for the purpose of amplifications. Specifically, these applications require highly linear voltage to current converters, which is commonly known as operational transconductance amplifier. OTA, generally have a differential pair as the input stage. An OTA that employs feed-forward techniques greatly enhances the performance of the target application. In many instances these feed-forward loops are employed to minimize nonlinear effects in amplifiers and the filters that incorporate OTA. Further, frequency compensation can also be achieved in OTAs with a feed-forward path.

The transfer characteristics of a OTA expressed as a voltage controlled current source can be given by

\[ I_{out} = G_m V_{d} \]  
\[ I_{out} = G_m(V_1 - V_2) \]  

Hence, the output current is given by the differences of the input voltage, with an ideally constant transconductance \( G_m \). Therefore \( G_m \) is the proportionality factor between the two of the input voltage. The transconductance can hence be concluded as the function of the input differential voltage. An ideal OTA has two differential voltage inputs with input impedance being infinite, which leads to zero input current. Ideal common mode input range is also infinite, whereas the differential signal controls an ideal current source. Therefore it is evident that the differential output current does not depend on the differential output voltage for a fully differential OTA. \( G_m \) being the proportionality factor between output current and input differential voltage is called transconductance 4.

Using Taylor expansions, the drain current of the MSFET devices be given as 4:

\[ I_d = g_{m1} V_{gs1} + g_{m2} V_{gs2}^2 + g_{m3} V_{gs3}^3 + \ldots \]  

where, \( V_{gs} \) is the voltage across the gate to source of the device, and \( g_{mn} \) is the n-th order derivatives of the drain current \( I_d \) with \( V_{gs} \). Similar to a MOSFET device, the entire transconductor circuit can be modeled using the

![Figure 1. Block diagram of the proposed transconductor linearization method.](image-url)
Taylor’s expansion in (3). The output drain current of the circuit consists of a polynomial of the gate input voltage $V_{in}$ and the transconductance $G_m$, which becomes:

$$I_{out} = g_{m1} V_{in} + g_{m2} V_{in}^2 + g_{m3} V_{in}^3 + \ldots$$

(4)

For linearization in a V to I conversion, the $I_{out}$ term should include the term $G_{m1}$ and $V_{in}$ alone. Generally, in a differential input pair the even order coefficients get eliminated; hence by (4) only $G_{m3}$ contributes to nonlinearity. Based on these assumptions a transconductor circuit can be modeled as:

$$I_{out} \approx G_{m1} V_{in} + G_{m3} V_{in}^3$$

(5)

Hence it is evident that the linearization can be enhanced by eliminating the $G_{m3} V_{in}^3$ component. The proposed linearization enhancement technique for the transconductor includes main and auxiliary paths. Different $G_m$ values are designed for the transconductors that are located in the main and auxiliary path. The output currents $I_1$ and $I_2$ of the main and auxiliary paths respectively can be modeled with (3). The third-order intermodulation distortion (IMD3) components of both main and auxiliary path are designed so that they are subtracted and eliminated in the output current $I_{out}$. Figure 2 shows the unit transconductor circuit.

Figure 4 shows the linearized OTA used for the linearization purpose. The input voltage of the main path is $V_{in}$, and the transconductance of this path is designed to be $2G_m$, this implies that both the transconductors are in parallel. On the other hand, the input voltage of the auxiliary path transconductor is $(-\sqrt{2}V_{in})$, whereas, its transconductance is designed to be only $G_m$. It can be noted that the auxiliary path is nothing but a unit transconductor. Due to the opposite polarities between the input and the output at the amplifier output is inverted. $I_{out}$ with the influence of feed forward auxiliary path can be given by:

$$I_1 = 2G_{m1} V_{in} + 2G_{m3} V_{in}^3$$

(6)

$$I_2 = -\frac{3}{2} G_{m1} V_{in} - \frac{1}{2} G_{m3} V_{in}^3$$

(7)

$$I_{out} = I_1 + I_2$$

(8)

$$I_{out} = (2 - \frac{3}{2}) G_{m1} V_{in}$$

(9)

Hence, a linear voltage to current conversion is achieved. The linear conversion is obtained by minimizing the power consumption and of $G_{m3}(2 - \sqrt{2})$.

For perfect cancellation of the $G_{m3}$ component, gate input voltages of $V_{in}$ and $(-\sqrt{2} V_{in})$ must be applied to each input of a transconductor. Therefore, for achieving an input voltage of $(-\sqrt{2} V_{in})$, the linear voltage amplifier circuit is designed as shown in Figure 3. The voltage amplifier consists of a driving and a loading inverters. A self-biased inverter is employed that can act as voltage buffer circuit. This designed buffer amplifies the input voltage linearly.

A linear voltage amplifier designed with a gain of (-1), is included in the main path so as to reduce the phase mismatch of main and auxiliary path, thus achieving a perfect cancellation. To get opposite polarities in the two paths transconductor circuits with differential inputs are used. A basic CMOS differential pair with a current mirror load is implemented to obtain a differential to single-ended conversion. The tail current can be varied to set a desired transconductance. This is achieved by designing a separate inverter that mirrors the current of an
external reference current source. The proposed circuits are shown in Figures 4, 5 and 6.

The original transconductance is no way altered by active $G_{m3}$ cancelling architecture; hence, this technique can implemented in most of the transconductors with differential inputs. Further, this linearization technique is independent of the bias variations of the transconductor. The gain of the designed linear voltage amplifier can be given by the $G_{m3}$ of the inverters and $R_{fb}$. Hence, the ratio of the main and auxiliary paths is insensitive to the bias voltages variation, this implies that any value of the $G_{m3}$ component can be cancelled, whereas, the main and auxiliary paths maintain a voltage amplification ratio of $1: \sqrt{2}$.

3. Tunable High-pass Filter

In a radar system frequency modulated continuous wave (FMCW)$^9$, the distance between the target and the baseband frequency proportional to each other. To reject the antenna coupling a filter is necessary in the receiver end baseband of through wall FMCW radar system$^{10}$ and wall reflected waves. In a situation where the target is present at the other end beyond the wall, a high-pass filter can be employed to attenuate the unwanted wall-reflected waves. A tunable cutoff frequency high-pass filter is necessary, as there is always a variable distance from the through-the-wall radar to the wall. A tunable Gm-C high-pass filter in $^{11,12}$ is designed using the linearized transconductors.

The N-th order high-pass filter with high-order admittance element integrated, making the transfer function from input to output as follows.

\[
H(s) = \frac{\text{Vout}}{\text{Vin}} = \frac{1}{s^n + G_{m1} + G_{m2} + \ldots + G_{m(n-1)} + G_{m}}
\]

The cascaded second order high pass filters are employed to make the higher order filter to maintain linearity in all ranges. The second-order high-pass filter with the same Gm values has transfer function as given below

\[
H(s) = \frac{\text{Vout}}{\text{Vin}} = \frac{s^2}{s^2 + c_{1}S + c_{2}}
\]

The fifth order high pass filters are cascaded to make higher order filter not to fall from the linearization. The fifth order high-pass filter with the similar Gm values has transfer function3.

\[
H(s) = \frac{\text{Vout}}{\text{Vin}} = \frac{s^5}{s^5 + c_{1}s^4 + c_{2}s^3 + c_{3}s^2 + c_{4}s + c_{5}}
\]

The designed filters is implemented with differential inputs and outputs. To prevent loading effect on the frequency response of the filter, a voltage buffer is designed as the output stage.

4. Simulation Results

The simulations and analysis are carried out using the Cadence CAD tool and is implemented in UMC 0.18-µm
CMOS technology. The observed large power consumption is mostly due to the CMOS inverters in the linearization circuit. This can be overcome by reducing the size of the inverters in the voltage amplifier. Figure 7 shows the simulation output of the 5th order high-pass filter. The enhanced linearity of the 5th order high-pass filter is validated using the parameter IIP3 value and 1-db compression point. In this figure the intersection point of input power versus output power shows at which point the amplifier has saturated. This has been analyzed using 1-db compression point.

Figure 7. IIP3 measurement of 5th order high-pass filter.

The simulation results of second order high pass filter is shown in Figure 8. It depicts the IIP3 values of two tone frequency. The input signals of 2.5 MHz and 3 MHz tones were applied to the input and the IIP3 is determined. A moderate IIP3 value of +25.85 dBm shows that the linearity has been enhanced. The single tone linearity for 1-db compression point is observed as +9.35 dBm, which further validates the linearity.

The comparison of second and fifth order high-pass filter performance with the other research work is shown in Table 1.

Table 1. Comparison of results

| parameters          | [3]  | [5]  | [6]  | This work (for 2nd order filter) | This work (for 5th order filter) |
|---------------------|------|------|------|----------------------------------|----------------------------------|
| Technology (µm)     | 0.18 | 0.18 | 0.18 | 0.18                             | 0.18                             |
| Filter topology     | RC-Gm-C low-pass | Gm-C low-pass | Active Gm-C low-pass | Gm-C high-pass | Gm-C high-pass |
| Linearization Technique | MGTR | Attenuation predistortion | - | Feed forward | Feed forward |
| Supply Voltage (V)  | 1.8  | 1.8  | 1.8  | 1.8                              | 1.8                              |
| Filter order        | 3    | 2    | 4    | 2                                 | 5                                |
| Cutoff frequency (MHz) | 50–200 | 200 | 11.3 | 0.15–0.75                         | 0.15–0.75                         |
| Power Consumption (mW) | 23.4  | 20.8 | 3.5  | 14.2–40.32                        | 14.2–40.32                        |
| P1 dB (dBm)         | -    | -    | 0.5  | +9.35                             | -                                |
| IIP3 (dBm)          | 17.3 | 14   | 10   | +25.85                            | 11.5                             |
5. Conclusion

A linearization transconductor circuitry is thus proposed. Using voltage buffer, which incorporates inverters and copied unique transconductors, linearization is effectively enhanced. This technique effectively cancels the $G_m^3$ component of transconductor by employing the feed-forward technique. The designed inverter-based linearization circuit is found to be insensitive to the bias variation, and the ratio of both main and auxiliary path is scaled to desired value accurately. To implement the linearization technique, a tunable Gm-C high-pass filter is proposed designed and validated using Cadence Specter simulator. The filter is integrated using a high-order admittance element. The measurement results show a highly linear filter operation as well as that the linearization technique is efficient. This technique can be adjusting to transconductors with differential inputs, and it has an advantage in process scaling.

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7. References

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