ON ARCHITECTURE TO ARCHITECTURE MAPPING FOR CONCURRENCY

Soham Chakraborty
Department of Computer Science and Engineering
IIT Delhi
Delhi 110016, India
soham@cse.iitd.ac.in

ABSTRACT

Mapping programs from one architecture to another plays a key role in technologies such as binary translation, decompilation, emulation, virtualization, and application migration. Although multicore architectures are ubiquitous, the state-of-the-art translation tools do not handle concurrency primitives correctly. Doing so is rather challenging because of the subtle differences in the concurrency models between architectures.

In response, we address various aspects of the challenge. First, we develop correct and efficient translations between the concurrency models of two mainstream architecture families: x86 and ARM (versions 7 and 8). We develop direct mappings between x86 and ARMv8 and ARMv7, and fence elimination algorithms to eliminate redundant fences after direct mapping. Although our mapping utilizes ARMv8 as an intermediate model for mapping between x86 and ARMv7, we argue that it should not be used as an intermediate model in a decompiler because it disallows common compiler transformations.

Second, we propose and implement a technique for inserting memory fences for safely migrating programs between different architectures. Our technique checks robustness against x86 and ARM, and inserts fences upon robustness violations. Our experiments demonstrate that in most of the programs both our techniques introduce significantly fewer fences compared to naive schemes for porting applications across these architectures.

1 Introduction

Architecture to architecture mapping is the widely applicable concept of converting an application that runs over some architecture X to run over some different architecture Y. For example, binary translators [notaz 2014, Chernoff et al. [1998], which recompile machine code from one architecture to another in a semantic preserving manner. Such translation is facilitated by decompilers [Bougacha, Bits, Yadavalli and Smith [2019], avast, Shen et al. [2012], which lift machine code from a source architecture to an intermediate representation (IR) and compile to a target architecture. Emulators implement a guest architecture on a host architecture. For instance, QEMU [QEMU emulates a number of architectures (including x86 and ARM) over other architectures, the Android emulator [Android-x86] runs x86 images on ARM, while Windows 10 on ARM emulates x86 applications.

Architecture to architecture mapping is essential for application migration and compatibility. An application written for an older architecture may need upgraded to execute on latest architectures, while an application primarily targeting a later architecture may need to preserve backward compatibility with respect to older one. For example, Arm discusses the required measures to port an application from ARMv5 to ARMv7 including synchronization primitives. Besides its practical uses, formally mapping between architectures is helpful in the design process of future processors and architectures, as it allows one to compare and relate subtle features like concurrency, which vary significantly from one architecture to another.

A key feature that has been overlooked in these mappings is concurrency, which is crucial for achieving good performance with modern multicore processors. To emulate or port a concurrent application correctly requires us to
map the concurrency primitives of the source to those of the target, taking into account the subtle differences in their concurrency models. Such semantic differences appear not only between architectures (e.g., x86 and ARM), but also between different versions of the same architecture (e.g., ARMv7 and ARMv8 [Pulte et al. 2018]).

In this paper, we address the challenge of developing correct and efficient translations between relaxed memory concurrency models of x86, ARMv8, and ARMv7. We approach the problem from multiple angles.

First, we develop correct mapping schemes between these concurrency models, using the ARMv8 model as an efficient intermediate concurrency model for mapping between x86 and ARMv7.

This naturally leads to the question whether ARMv8 model can also serve as a concurrency model for IR in a decompiler. Decompilers typically (1) raise the source machine code to an IR, (2) optimize the IR, and (3) generate the target code. Thus, if the IR follows the ARMv8 concurrency model, steps (1) and (3) can be performed efficiently to facilitate translations between x86 and ARM concurrent programs. For step (2), we evaluate common optimizations on ARMv8 concurrency and observe that a number of common transformations are unsound. The result demonstrates that to achieve correct and efficient mapping by all steps (1,2,3) we require to come up with a different concurrency model. We leave the exploration for such a model for future research.

Next, we focus on optimizing the direct mappings further. The issue is that for correctness direct mappings introduce fences in translating stronger accesses to weaker ones. The introduced fences can be often redundant in certain memory access sequences and can be eliminated safely. We identify conditions of safe fence elimination, prove safe fence elimination, and based on these conditions we propose fence elimination algorithms.

In addition to fence elimination, we apply memory sequence analysis to check and enforce robustness for a class of concurrent programs. Robustness analysis checks whether a program running model demonstrate only the behaviors which are allowed by a stronger model. The behaviors of a robust program are indistinguishable on stronger model from an weaker model and therefore the program can seamlessly migrate from one architecture to another as far as concurrent behaviors are concerned. If a program is not robust we insert fences to enforce robustness against a stronger model. It is especially beneficial in application porting and migration [Barbalace et al. 2020, 2017] where it is crucial to preserve the observable behaviors of a running application.

Contributions & Results. Now we discuss the specific contributions and obtained results.

- In §4 we propose the mapping schemes ($\rightarrow$) between x86 and ARMv8, and between ARMv8 and ARMv7 as shown in Fig. 1. We do not propose any direct mapping between x86 and ARMv7, instead we consider ARMv8 as an intermediate model. We achieve x86 to ARMv7 mapping by combining x86 to ARMv8 and ARMv8 to ARMv7 mapping. Similarly, ARMv7 to x86 mapping is derived by combining ARMv7 to ARMv8 and ARMv8 to x86 mappings. We show that the direct mapping schemes would be same as these two step mappings through ARMv8. We also show that these mapping schemes are efficient; each of the leading and/or trailing fences used in mapping with the memory accesses are required to preserve correctness.

- We show that multicycle-atomicity (MCA) (a write operation is observable to all other threads at the same time) does not affect the mapping schemes between ARMv8 and ARMv7 though it is a major difference between ARMv8 and ARMv7 [Pulte et al. 2018] as ARMv7 allows non-MCA behavior unlike ARMv8. To demonstrate the same we propose ARMv7-mca in §4 which restricts non-MCA behavior in ARMv7 and show that the mapping scheme from ARMv8 to ARMv7-mca is same as ARMv8 to ARMv7 (Fig. 13a) and the mapping scheme of ARMv7-mca to ARMv8 is same as ARMv7 to ARMv8 mapping (Fig. 12a) respectively.

- In §4.2 and in §4.6 we propose alternative schemes for x86 to ARMv8 and ARMv8 to ARMv7 mapping where the respective x86 and ARMv8 programs are generated from C11 concurrent programs. In these schemes we exploit the catch-fire semantics of C11 concurrency [ISO/IEC 9899 2011, ISO/IEC 14882 2011]. We do not generate additional fences for the load or store accesses generated from non-atomic loads or stores unlike the x86 to ARMv8 and ARMv8 to ARMv7 mappings.
On Architecture to Architecture Mapping for Concurrency

\[ X[1] = 1; \quad a = X[1]; \quad c = Y[1]; \quad Y[1] = 1; \quad \Rightarrow \quad X[1] = 1; \]

\[ a = X[1]; \quad c = Y[1]; \quad Y[1] = 1; \]

\[ b = Y[a]; \quad d = Z[c]; \]

\[ Y[1] = 1; \]

(a) Initially \( X[1] = Y[1] = 0 \) and behavior in question: \( a = c = 1, \quad b = d = 0 \).

St(\( X[1] \), 1) \hspace{1cm} St(\( Y[1] \), 1)

\[ \text{Ld}(X[1], 1) \quad \text{Ld}(Y[1], 1) \]

\[ \text{addr} \quad \text{addr} \]

\[ \text{Ld}(Y[1], 0) \quad \text{Ld}(X[1], 0) \]

(b) Disallowed in ARMv8

St(\( X[1] \), 1) \hspace{1cm} St(\( Y[1] \), 1)

\[ \text{Ld}(X[1], 1) \quad \text{Ld}(Y[1], 1) \]

\[ \text{R} \]

\[ \text{Ld}(Y[1], 0) \quad \text{Ld}(X[1], 0) \]

(c) Allowed in ARMv7. \( R = \text{ctrl}_{\text{isb}} \cup \text{addr} \)

Figure 2: LDR \( \mapsto \) LDR; CBISB in ARMv8 to ARMv7 mapping is unsound.

- In §5 we study the reordering, elimination, and access strengthening transformations in ARMv8 model. We prove the correctness of the safe transformations and provide counter-examples for the unsafe transformations.
- The mapping schemes introduce additional fences while mapping the memory accesses. These fences are required to preserve translation correctness in certain scenarios and otherwise redundant. In §6 we identify the conditions when the fences are redundant and prove that eliminating the fences are safe. Based on these conditions we define fence elimination algorithms to eliminate redundant fences without affecting the transformation correctness.
- We define the conditions for robustness for an (i) ARMv8 program against sequential consistency (SC) and x86 model, (ii) ARMv7/ARMv7-mca program against SC, x86, and ARMv8 model, and (iii) ARMv7 program against ARMv7-mca model in §7 and prove their correctness in Appendix D. We also introduce fences to enforce robustness for a stronger model against a weaker model. To the best of our knowledge we are the first to check and enforce robustness for ARM programs as well as for non-SC models.
- In §8 we discuss our experimental results. We have developed a compiler based on LLVM to capture the effect of mappings between x86, ARMv8, and ARMv7. Next, we have developed fence elimination passes based on §6. The passes eliminate significant number of redundant fences in most of the programs and in some cases generate more efficient program than LLVM mappings.

We have also developed analyzers to check and enforce robustness in x86, ARMv8, and ARMv7. For a number of x86 programs the result of our SC-robustness checker matches the results from Trencher et al. [2013] which also checks SC-robustness against TSO model. Moreover, we enforce robustness with significantly less number of fences compared to naive schemes which insert fences without robustness information.

In the next section we informally explain the overview of the proposed approaches. Next, in §3 we discuss the axiomatic models of the respective architectures which we use in later sections. The proofs and additional details are in the supplementary material.

2 Overview

In this section we discuss the overview of our proposed schemes, related observations, and the analysis techniques.

2.1 Alternatives in x86 to ARMv8 mapping

In x86 to ARMv8 mapping we considered two alternatives for mapping loads and stores: (1) x86 store and load to ARMv8 release-store (\( \text{WMOV} \mapsto \text{STLR} \)) and acquire-load (\( \text{RMOV} \mapsto \text{LDAR} \)) respectively. (2) x86 store and load to ARMv8 regular store and load accesses with respective leading and trailing fences as proposed in Fig. 9a, that is, \( \text{WMOV} \mapsto \text{DMBST}; \text{STR} \) and \( \text{RMOV} \mapsto \text{LDR}; \text{DMBLD} \) respectively. We choose (2) over (1) for following reasons.

In the next section we informally explain the overview of the proposed approaches. Next, in §3 we discuss the axiomatic models of the respective architectures which we use in later sections. The proofs and additional details are in the supplementary material.
ARMv8 to ARMv7 mapping in Fig. 13a introduces a trailing control fence (CBISB) is not enough for correctness. Consider the mapping of the program from ARMv8 to ARMv7 in Fig. 2a. The execution is disallowed in ARMv8 as it creates an observed-by (ob) cycle as shown in Fig. 2b. However, when mapping to ARMv7, if we map LDR → LDR; CBISB and rest of the instructions are mapped following the mapping scheme in Fig. 13a then the execution would be allowed as shown in Fig. 2c. Therefore LDR → LDR; CBISB is too weak and we require a DMB fence after each load as well as RMOV for the same reason.

2.2 ARMv8 to ARMv7 mapping: ARMv7 LDR is significantly weaker than ARMv8 LDR

ARMv8 to ARMv7 mapping in Fig. 13a introduces a trailing DMB fence for ARMv8 LDR and LDR accesses as introducing a trailing control fence (CBISB) is not enough for correctness. Consider the mapping of the program from ARMv8 to ARMv7 in Fig. 2a. The execution is disallowed in ARMv8 as it creates an observed-by (ob) cycle as shown in Fig. 2b. However, when mapping to ARMv7, if we map LDR → LDR; CBISB and rest of the instructions are mapped following the mapping scheme in Fig. 13a then the execution would be allowed as shown in Fig. 2c. Therefore LDR → LDR; CBISB is too weak and we require a DMB fence after each load as well as RMOV for the same reason.

2.3 Multicopy atomicity does not change the mapping from ARMv8

In ?? we strengthen the ARMv7 model to ARMv7-mca to exclude non-multicopy atomic behaviors. However, even with such a strengthening an LDR mapping requires a trailing DMB fence.

Load access mapping without trailing fence is unsound in ARMv8 to ARMv7-mca mapping. Consider the example in Fig. 3 where the ARMv8 to ARMv7-mca mapping does not introduce trailing fence for a load access and therefore we analyze the same execution in ARMv8 and ARMv7-mca. The shown behavior is not allowed in ARMv8 as there is a dependency-ordered-before (dob) relation from the reads to the respective writes due to data; coi relation.

Reordering is restricted. x86 allows the reordering of independent store and load operations accessing different locations [Lahav and Vafeiadis 2016]. ARMv8 also allows reordering of different-location store-load pairs, but restricts the reordering of a pair of release-store and acquire load operation as it violates barrier-ordered-by (bob) order [Pulte et al. 2018]. Thus scheme (1) is more restrictive than (2) considering reordering flexibility after mapping.

Further optimization. (2) generates certain fences which are redundant in certain scenarios and can be removed safely. Consider the mappings below; the generated DMBST is redundant in (2) and can be eliminated safely unlike mapping (1).

(1) RMOV; WMOV → LDAR; STLR
(2) RMOV; WMOV → LDR; DMBLD; DMBST; STR → LDR; DMBLD; STR

x86 → ARMv8 → ARMv7 would introduce additional fences To map x86 to ARMv7, if we use ARMv8 as intermediate step then scheme (1) introduces additional fences unlike (2) as follows.

(1) WMOV → STLR → DMB; STR; DMB
(2) WMOV → DMBST; STR → DMB; STR
Consider the example mapping and the execution in Fig. 4. The execution in ARMv8 has ordered-by (ob) cycle and hence not consistent. The LDR ↔ LDR; CBISB mappings would result in respective ppo relations in the execution, but these ppo relations do not restrict such a cycle. As a result, the execution is ARMv7 or ARMv7-mca consistent. Hence LDR ↔ LDR; CBISB is unsound in ARMv8 to ARMv7-mca mapping.

Trailing control fence is not enough. Consider the example mapping and the execution in Fig. 4. The execution in ARMv8 has ordered-by (ob) cycle and hence not consistent. The LDR ↔ LDR; CBISB mappings would result in respective ppo relations in the execution, but these ppo relations do not restrict such a cycle. As a result, the execution is ARMv7 or ARMv7-mca consistent. Hence LDR ↔ LDR; CBISB is unsound in ARMv8 to ARMv7-mca mapping.

2.4 Mapping schemes for programs generated from C11

In §4.2 §4.6 and §4.8 we study C11 ↔ x86 ↔ ARMv8, C11 ↔ ARMv8 ↔ ARMv7, and C11 ↔ ARMv8 ↔ ARMv7-mca mapping schemes respectively. In these mappings from stronger to weaker models, we consider that the source architecture program is generated from a C11 program following the mapping in map. We use this information to categorize the accesses in architectures as non-atomic (NA) and atomic (A), and exploit two aspects of C11 concurrency; first, a program with data race on non-atomic access results in undefined behavior. Second, C11 uses atomic accesses to achieve synchronization and avoid data race on non-atomics. Considering these properties we introduce leading or trailing fences in mapping particular atomic accesses and we map non-atomics to respective accesses without any leading or trailing fence.

Pros and Cons C11 ↔ x86 ↔ ARMv8 scheme has a tradeoff; in case of non-atomics it is more efficient than x86 ↔ ARMv8 as it does not introduce additional fences whereas an atomic store mapping requires a leading full fence or a pair of DMBLD and DMBST fences. Consider the mapping of the sequence: LdNA; StNA; StREL → RMOVNA; WMOVNA; WMOV_A → LDR; STR; DMBFULL; WMOV_A.

In this case the C11 non-atomic memory accesses cannot be moved after the release write access. Hence we introduce a leading DMBFULL with WMOV_A in C11 ↔ x86 ↔ ARMv8 to preserve the same order. Consider the C11 to x86 to ARMv8 mapping of the program below.

```
|   |   |   |   |   |
|---|---|---|---|---|
| a = XNA; | Y = 1; | c = YNA; |
| YNA = 1; | Z = 1; |
| ZREL = 1; |
```

The C11 program is data race free as it is well-synchronized by release-acquire accesses on Z and the outcome where r = c = 1 is disallowed in the program. The generated ARMv8 program disallows the outcome, without the DMBFULL in the first thread the outcome would be possible. It is because a DMBLD or DMBFULL fence is required to preserve bob relation between Ld(X, 2) and St(Z, 1) events. Note that a DMBLD is not sufficient to establish bob relation between St(Y, 1) and St(Z, 1) and hence we require a DMBST or DMBFULL fence. Therefore we have to introduce a leading pair of DMBLD and DMBST fences or a DMBFULL fence for WMOV_A mapping.

As a result Fig. 5 provides more efficient mapping for RMOVNA and WMOVNA accesses, but incurs more cost for WMOV_A by introducing a leading DMBFULL instead of a DMBST fence. After the mapping we may weaken such a DMBFULL fence whenever appropriate.

The C11 → ARMv8 → ARMv7 scheme does not introduce fence for mapping non-atomics and therefore more efficient than ARMv8 → ARMv7. Note that C11 StREL generates an STLR in ARMv8 and ARMv8 STR is generated only from C11 StRELX which does not enforce any such order.

2.5 ARMv8 as an intermediate model for mappings between x86 and ARMv7

Now we move to mappings between x86 and ARMv7. We do not propose direct mapping schemes, instead we use ARMv8 concurrency as an intermediate concurrency model as x86 → ARMv7/ARMv7-mca and ARMv7/ARMv7-mca → x86 would be same as x86 → ARMv8 → ARMv7/ARMv7-mca and ARMv7/ARMv7-mca → ARMv8 → x86 respectively.

x86 → ARMv7 vs x86 → ARMv8 → ARMv7 We derive x86 → ARMv8 → ARMv7 by combining x86 → ARMv8 (Fig. 9a) and ARMv8 → ARMv7 (Fig. 13a) as follows.
ARMv8 (Fig. 12a) and ARMv8 to x86 (Fig. 12b) as follows. Note that the mapping does not introduce any fence the introduced fences are necessary and sufficient. Demonstrate the necessity of the introduced fences. The introduced fences only allow reordering of an independent data dependency. The correctness proofs of the x86 to ARMv8 and ARMv8 to ARMv7 mapping schemes in Fig. 9a and Fig. 13a demonstrate the necessity of the introduced fences. The introduced fences only allow reordering of an independent store-load access pair on different locations which is similar to the allowed reordering restriction of x86. Therefore the introduced fences are necessary and sufficient.

ARMv7 → x86 vs ARMv7 → ARMv8 → x86. We derive ARMv7 → ARMv8 → x86 by combining ARMv7 → ARMv8 (Fig. 12a) and ARMv8 to x86 (Fig. 12b) as follows. Note that the mapping does not introduce any fence along with the accesses and therefore optimal.

```
MFENCE → DMBFULL → DMB  RMW → DMBFULL; RMW; DMBFULL → DMB; RMW; DMB
RMV → LDR; DMBLD → LDR; DMB  WMOV → DMBST; STR → DMB; STR
```

The correctness proofs of the x86 to ARMv8 and ARMv8 to ARMv7 mapping schemes in Fig. 9a and Fig. 13a demonstrate the necessity of the introduced fences. The introduced fences only allow reordering of an independent store-load access pair on different locations which is similar to the allowed reordering restriction of x86. Therefore the introduced fences are necessary and sufficient.

2.6 Common optimizations in ARMv8 concurrency

We consider ARMv8 as a concurrency model of an IR and find that many common compiler optimizations are unsound in ARMv8.

- **ARMv8 does not allow store-store and load-store reorderings** Consider the program and the execution in Fig. 5. In this execution there are `addr; [Ld; po; [5t]; po; [5t]]` relations in the first and second threads respectively which result in dob relations and in a turn an ob cycle. Therefore the execution is not ARMv8 consistent and the outcome `a = b = 1` is disallowed. However, load-store reordering `c = Y[a]; Z = 1 ⇝ Z = 1; c = Y[a]` or store-store reordering `V[b] = 1; Z = 1 ⇝ Z = 1; V[b] = 1` remove the respective dob relation(s) and enable `a = b = 1` in the target. Thus store-store and load-store reorderings are unsafe in ARMv8.

- **Overwritten-write (OW) is unsound.** Consider the program and its outcome `a = 1, b = 2` in Fig. 6a. In the respective execution the first thread has `data; coi ⊆ dob` from `Ld(X, 1)` to `St(Y, 2)`. The other thread has a `dob` relation due to `DMBFULL` fence which in turn create an `ob` cycle. Hence the execution is not ARMv8 consistent and the outcome `a = 1, b = 2` is disallowed. Overwriting `Y = a` in the first thread removes the `dob` relation and then `a = 1, b = 2` becomes possible.

- **Read-after-write (RAW) is unsound.** We study the RAW elimination in Fig. 6b which is performed based on dependence analysis. Before we go to the transformation, we briefly discuss dependence analysis on the access sequence `a = X; Y[a * 0] = 1`. In this case there is a false dependence from load of `X` to store of `Y[a * 0]` as `a * 0 = 0` always. ARMv8 does not allow to remove such a false dependence [Pulte et al. 2018]. However, we observe that using a static analysis that distinguishes between true and false dependencies is also wrong in ARMv8. In this example we analyze such a false dependence and based on that we perform read-after-write elimination on the program, that is, `Y[a * 0] = 1; b = Y[0] ⇝ Y[a * 0] = 1; b = 1`.

The source program does not have any execution `a = 1, b = 1, c = 0` as `addr; rfi; addr ⊆ dob` and in the other thread there is a `dob` relation which together create an `ob` cycle. In the target execution there is no `dob` relation from the load of `X` to the load of `c = Z[b]` and therefore the outcome `a = 1, b = 1, c = 0` is possible. As a result, the transformation is unsound in ARMv8.

2.7 Fence eliminations in ARMv8

The mapping schemes introduce leading and/or trailing fences for various memory accesses. However, some of these fences may be redundant can safely be eliminated. Consider the x86 → ARMv8 mapping and subsequent redundant fence eliminations below.

```
RMV; MFENCE; WMOV → LDR; DMBLD; DMBFULL; DMBST; STR → LDR; DMBLD; STR
```

Figure 5: Load-store or store-store reorderings introduce `a = b = 1` outcome and are unsound in ARMv8.
Consider the execution in Fig. 8, the execution allows the cycle and violates SC robustness. Therefore, ARMv7 model.

2.8 Analyzing and enforcing robustness

There are existing approaches [Lahav and Margalit 2019, Bouajjani et al. 2013] which explores program executions to answer such queries. We propose an alternative approach by analyzing memory access sequences. In this analysis

1. We identify the program components which may run concurrently. Currently we consider fork-join parallelism and identify the functions which create one or multiple threads. Our analysis considers that each of such functions creates multiple threads. Therefore analyzing these functions \( f_1, \ldots, f_n \), we analyze all programs of the form \( f_1 \parallel \cdots \parallel f_1 \parallel f_n \parallel \cdots \parallel f_n \).

2. Next, we analyze the memory access sequences in \( f_1, \ldots, f_n \) to check whether the memory access pairs in these functions may create a cycle.

3. In case a cycle is possible, we check if each access pair on a cycle is ordered by robustness condition. If so, then all \( K \) consistent executions of these programs are also \( M \) consistent.

Consider the example in Fig. 7. We analyze the access sequences in thread functions \( SB \), \( SB' \), and \( SB'' \) and derive a graph by memory access pairs which contains a cycle by the memory access pairs in \( SB \) and \( SB' \). These pairs on the cycle have intermediate \( MFENCE \) operations which enforce interleaving executions only irrespective of the number of threads created from \( SB \), \( SB' \), \( SB'' \). Our analysis reports these x86 programs as SC-robust. Using this approach we check \( M \)-robustness against \( K \) where \( K \) is an weaker models than \( M \).

Enforcing robustness. If we identify robustness violation for a program then we identify memory access pairs which may violate a robustness condition. For these access pairs we introduce intermediate fences to enforce robustness against a stronger model.

ppo does not suffice to enforce robustness in ARMv7. In addition to fences, ppo relations also orders a pair of accesses on different locations. However, we observe that ppo relations are not sufficient to ensure robustness for ARMv7 model.

Consider the execution in Fig. 8, the execution allows the cycle and violates SC robustness. Therefore ppo cannot be used to order epo relations to preserve robustness.
3 Formal Models

Syntax Instead of delving into the syntactic notations in each instruction set, we use common expressions and commands which can be extended in each architecture.

\[
E ::= r | v | E + E | E * E | E \leq E | \cdots \quad (Expr)
\]

\[
C ::= \text{skip} | C ; C | r = E | r = X | X = E | r = \text{RMW}(X, E) | r = \text{RMW}(X, E) | \cdots
\quad | \text{br label} | \text{br label label} \quad (Cmd)
\]

\[
P ::= X = v ; \cdots X = v ; \{ C | \cdots | C \} \quad (Program)
\]

In this notation we use \( X \in \text{Locs}, r \in \text{Reg}, \text{and} \ v \in \text{val} \) where Locs, Reg, val denote finite sets of memory locations, registers, and values respectively. A program \( P \) consists of a set of initialization writes followed by a parallel composition of thread commands.

Semantics We follow the per-execution based axiomatic models for these architectures. In these models a program’s semantics is defined by a set of consistent executions. An execution consists of a set of events and relations among the events.

Given a binary relation \( R \) on events, \( R^-, R^0, R^+ \), and \( R^* \) represent inverse, reflexive, transitive, and reflexive-transitive closures of \( R \) respectively. \( \text{dom}(R) \) and \( \text{codom}(R) \) denote its domain and its range respectively. Relation \( R \) is total on set \( S \) when \( \text{total}(S, R) \triangleq \forall a, b \in S. a = b \lor R(a, b) \lor R(b, a) \). We compose binary relations \( R, S \subseteq E \times E \) relationally by \( R ; S \). \( [A] \) denotes an identity relation on a set \( A \). We write \( R|_{\text{loc}} \) to denote \( R \) related event pairs on same locations, that is, \( R|_{\text{loc}} \triangleq \{(e, e') \in R | e_.loc = e'.loc\} \). Similarly, \( R|_{\not\text{loc}} \triangleq R \setminus R|_{\text{loc}} \) is the \( R \) related event pairs on different locations.

Definition 1. An event is of the form \( \langle \text{id}, \text{tid}, \text{lab} \rangle \), where \( \text{id}, \text{tid} \in \mathbb{N} \) and \( \text{lab} \) are the unique identifier, thread id, and the label of the event based on the respective executed memory access or fence instruction. A label is of the form \( \langle \text{op}, \text{loc}, \text{rval}, \text{wval} \rangle \).

For an event \( e \), whenever applicable, \( e_.\text{lab}, e_.\text{op}, e_.\text{loc}, e_.\text{rval} \), and \( e_.\text{wval} \) to return the label, operation type, location, read value, and written value respectively. We write \( \text{ld}, \text{st}, \text{u}, \text{and} \ F \) to represent the set of load, store, update, and fence events. Moreover, load or update events represent read events \( (\text{R}) \) and store or update events are write events \( (\text{W}) \), that is \( \text{R} = \text{Ld} \cup \text{U} \) and \( \text{W} = \text{St} \cup \text{U} \). We write \( \llbracket i \rrbracket \) to represent the generated event in the respective model from an instruction \( i \). For example, in x86 \( \llbracket i \rrbracket \in \text{St} \) holds when \( i \) is a \( \text{RMW} \) instruction. We also overload the notation as \( \llbracket P \rrbracket_M \) to denote the set of execution of program \( P \) in model \( M \).

In an execution events are related by various types of relations. Relation program-order(\( \text{po} \)) captures the syntactic order among the events. We write \( a.b \) to denote that \( b \) is immediate po-successor of event \( a \). Reads-from (\( \text{rf} \)) associates a write event to a read event that justifies its read value. Relation coherence-order (\( \text{co} \)) is a total-order on same-location writes (stores or updates). The from-read (\( \text{fr} \)) relation relates a pair of same-location read and write events. We also categorize the relations as external and internal relations and define \( \text{extended-coherence-order (eco)} \). Relation modification order (\( \text{mo} \)) is a total-order on writes, updates, and fences such that \( \text{mo} \subseteq O \times O \) where \( O = \text{St} \cup \text{U} \cup \text{F} \).
Note that the co relation is included in the mo relation. The mo relation is used in x86 model only; the ARM models do not use mo in their definitions.

**Definition 2.** An execution is of the form $X = \langle E, po, rf, co, mo \rangle$ where $X,E$ denotes the set of memory access or fence events and $X,po, X,rf, X,co,$ and $X,mo$ denote the set of program-order, reads-from, coherence order, and modification order relations between the events in $X,E$.

### 3.1 Concurrency models of x86, ARMv7, ARMv7-mca, and ARMv8

We now discuss the architectures and follow the axiomatic models of x86 and ARMv7 from Lahav et al. [2017], and ARMv8 axiomatic model from Pulte et al. [2018]. We also present ARMv7-mca; a strengthened ARMv7 model with multicopy atomicity (MCA).

**x86.** In x86 MOV instruction is used for both loading a value from memory as well as for storing a value to memory. To differentiate these two accesses we categorize them as WMOV and RMOV operations. In addition, there are atomic update operations which we denote by RMW. x86 also provides MFENCE which flushes buffers and caches and ensure ordering between the preceding and following memory accesses.

In x86 concurrency WMOV, RMOW, and MFENCE generate St, Ld, and F events respectively. A successful RMW generates U and otherwise an Ld event. We derive x86-happens-before (xhb) relation from program-order and reads-from relations:

$$ xhb \triangleq (po \cup rf)^+ $$

An x86 execution $X$ is consistent when:

- $X,xhb$ is irreflexive.
- $X,mo; X,xhb$ is irreflexive.
- $X,fr; X,xhb$ is irreflexive.
- $X,fr; X,mo$ is irreflexive.
- $X,fr; X,mo; X,rfe; X,po$ is irreflexive.
- $X,fr; X,mo; [X,U \cup X,F]; X,po$ is irreflexive.

**ARMv7.** It provides LDR and STR instructions for load and store operations, and load-exclusive (LDREX) instructions to perform atomic update operation RMW where $RMW \triangleq L : LDREX ; mov ; teq \{ L \} ; STR ; teq L \{ L \}$. ARMv7 provides full fence DMB which orders preceding and following instructions. There is also lightweight control fence ISB which is used to construct CBISB $\triangleq$ cmp; bc; ISB to order load operations.

In this model load (Ld), store (St), F events are generated from the execution of LDR and LDXR, STR and STXR, and DMB instructions respectively. Fence ISB is captured in ctrl$_{ISB}$ (similar to ctrl$_{sync}$ in Lahav et al. [2017]) and in turn ppo relation, but does not create any event in an execution.

ARMv7 defines preserved-program-order (ppo) relation which is a subset of program-order relation.

We first discuss the primitives of ppo following §F.1 in Lahav et al. [2017]: ppo is based on data ($\subseteq Ld \times St$), control ($\subseteq Ld \times E$), and address ($\subseteq Ld \times (Ld \cup St)$) dependencies. Moreover, ISB fences along with conditionals introduce ctrl$_{ISB}$ $\subseteq$ ctrl preserved program order. Finally, ctrl; po $\subseteq$ ctrl and ctrl$_{ISB}$; po $\subseteq$ ctrl$_{ISB}$ holds from definition.

Based on these primitives ARMv7 define read-different-writes (rdw) and detour (detour) relations as follows.

$$ rdw \triangleq (fre; rfe) \subseteq po \quad detour \triangleq (coe; rfe) \setminus po $$

**read-different-writes (rdw)** relates two reads on same location in a thread which reads from different writes and detour captures the scenario where an external write takes place between a pair of same-location write in the same thread, and the read reads-from that external write.

Based on these primitives ARMv7 defines ii, ci, ic, cc relations where each of these relations can be derived from the following sequential compositions and the constraints.

$$ xy \triangleq \bigcup_{n \geq 1} x^1y_0^1 ; x^2y_0^2 ; \cdots x^ny_0^n $$

where
ARMv7-mca. We strengthen the ARMv7 model and define ARMv7-mca model to support multicopy atomicity. To do so, following [Wickerson et al.][2017], we define write-order relations to order a pair of intra-thread events. Finally Based on these primitives ARMv8 defines coherence-after (ca), observed-by(obs), and atomic-ordered-by (aob) relations on same-location events. ARMv8 also defines dependency-ordered-before (dob) and barrier-ordered-by (bob) relations to order a pair of intra-thread events. Finally Ordered-before (ob) is a transitive closure of obs, aob, dob, and bob relations.

| x86       | ARMv8         |
|-----------|---------------|
| RMOV      | LDR; DMBLD    |
| WM0V      | DMBST; STR    |
| RMW       | DMBFULL; RMW; DMBFULL |
| MFENCE    | DMBFULL      |

(a) x86 to ARMv8

| C11 to x86 | ARMv8         |
|------------|---------------|
| RMOKA      | LDR           |
| WMOKA      | STR           |
| RMOKA      | LDR; DMBLD    |
| WMOKA      | DMBFULL; STR  |
| RMW        | DMBFULL; RMW; DMBFULL |
| MFENCE     | DMBFULL      |

(b) C11 to x86 to ARMv8

Figure 9: Mapping schemes from x86 to ARMv8.

- \( x, y, x^1 \ldots x^n, y^1 \ldots y^n \in \{ i, c \} \).
- If \( x = c \) then \( x^1 = c \).
- For every \( 1 \leq k \leq n - 1 \), if \( y^k = c \) then \( x^{k+1} = c \).
- If \( y = i \) then \( y^n = i \).

Finally ARMv7 defines ppo as follows: \( ppo \triangleq [Ld]; ii; [Ld] \cup [Ld]; ii; [St]. \) ARMv7 also defines fence, ARM-happens-before (ahb), and propagation (prop) relations as follows.

\[
\begin{align*}
\text{fence} & \triangleq [Ld \cup St]; po; [F]; po; [Ld \cup St] \\
\text{ahb} & \triangleq ppo \cup \text{fence} \cup \text{rfe} \\
\text{prop} & \triangleq \text{prop}_1 \cup \text{prop}_2 \text{ where} \\
\text{prop}_1 & \triangleq [St]; \text{rfe}^*; \text{fence}; ahb^*; [St] \text{ and} \\
\text{prop}_2 & \triangleq (\text{coe} \cup \text{rfe})^*; \text{rfe}^*; (\text{fence}; ahb^*)^*; \text{fence}; ahb^*
\end{align*}
\]

These relations are used to define the consistency constraints of an ARMv7 execution \( X \) as follows:

- \( X, \text{co} \) is total
- \( \langle X, \text{po} \rangle_{\text{loc}} \cup X, \text{rf} \cup X, \text{fr} \cup X, \text{co} \) is acyclic
- \( X, \text{fr} \); \( X, \text{prop} \); \( X, \text{ahb}^* \) is irreflexive.
- \( (X, \text{co} \cup X, \text{prop}) \) is acyclic.
- \( [X, \text{rmw}]; X, \text{fr} ; X, \text{coe} \) is irreflexive
- \( X, \text{ahb} \) is acyclic

**ARMv8.** provides load (LDR), store (STR) for load and store operations, load-exclusive (LDXR) and store-exclusive (STXR) instructions to construct RMW similar to that of ARMv7. In addition, ARMv8 provides load-acquire (LDAR), store-release (STLR), load-acquire exclusive (LDAXR), and store-release exclusive (STLXR) instructions which operate as half fences. In addition to DMBFULL and ISB, ARMv8 provides load (DMBLD) and store (DMBST) fences. A DMBLD fence orders a load with other accesses and a DMBST orders a pair of store accesses.

Based on these primitives ARMv8 defines coherence-after (ca), observed-by(obs), and atomic-ordered-by (aob) relations on same-location events. ARMv8 also defines dependency-ordered-before (dob) and barrier-ordered-by (bob) relations to order a pair of intra-thread events. Finally Ordered-before (ob) is a transitive closure of obs, aob, dob, and bob relations.

\[
\begin{align*}
\text{ca} & \triangleq \text{fr} \cup \text{co} \\
\text{obs} & \triangleq \text{rfe} \cup \text{fre} \cup \text{coe} \\
\text{aob} & \triangleq \text{rmw} \cup [\text{range(rmw)}]; \text{rfi}; [A] \\
\text{dob} & \triangleq \text{addr} \cup \text{data} \cup \text{ctrl}; [St]; \text{ctrl} \cup \text{addr}; [ISB]; \text{po}; [Ld] \\
& \cup \text{addr}; \text{po}; [St] \cup \text{ctrl}; \text{data}; \text{coi} \cup \text{addr} \cup \text{data}; \text{rfi} \\
\text{bob} & \triangleq \text{po}; [F]; \text{po} \cup [L]; \text{po}; [A]; \cup [Ld]; \text{po}; [F]; \text{po} \cup [A]; \text{po} \\
& \cup [St]; \text{po}; [F]; \text{po} \cup [L] \cup \text{po} \cup [L]; \text{coi} \\
\text{ob} & \triangleq (\text{obs} \cup \text{dob} \cup \text{aob} \cup \text{bob})^+
\end{align*}
\]
On Architecture to Architecture Mapping for Concurrency

Finally an ARMv8 execution $X$ is consistent when:

- $X.pm|oc \cup X.ca \cup X.rf$ is irreflexive. (internal)
- $X.ob$ is irreflexive (external)
- $X.rmw \cap (X.fre; X.coe) = \emptyset$ (atomic)

4 Architecture to Architecture Mappings

We propose correct and efficient mapping schemes between x86 and ARM models. These schemes may introduce leading and/or trailing fences while mapping memory accesses from one architecture to another. We show that the fences are necessary by examples and prove that the fences are sufficient for correctness. To prove correctness we show that for each consistent execution of the target program after mapping there exists a corresponding consistent execution of the source program before mapping with same behavior.

4.1 x86 to ARMv8 mapping

The mapping scheme from x86 to ARMv8 is in Fig. 9a. The scheme generates a DMBFULL for an MFENCE. While mapping x86 memory accesses to that of ARMv8, the scheme introduces a leading DMBST fence with a store, a trailing DMBLD fence with a load, and leading as well as a trailing DMBFULL fences with an update. We now discuss why these fences are required.

Leading store fence In an x86 execution a pair of stores is ordered unlike that of ARMv8 execution. A pair of store events ($St$) in ARMv8 execution are bob ordered when there is intermediate $F_{ST}$ or $F$ event, that is $[St]; po; [F_{ST} \cup F]; po; [St] \subseteq bob$. To introduce such a bob order we require at least an intermediate $F_{ST}$ fence event. Therefore the scheme generates a leading DMBST fence with a store which ensures store-store order with preceding stores in ARMv8.

Trailing load fence We know a load-store or load-load access pair is ordered in x86. To preserve the same access ordering we require a $F_{L0}$ fence between a load-load or load-store access pair. Therefore the scheme generates a trailing DMBLD fence with a load which ensures such order.

Leading and trailing fence for atomic update Consider the x86 programs and $a = b = 0$ outcome.

No x86 execution would allow $a = b = 0$ in the two programs in Figs. 10 and 11. However, if we translate these programs without intermediate DMBFULL fences between each pair of store and RMW accesses then $a = b = 0$ would
be possible in these two programs in ARMv8 as shown in the corresponding executions. As a result, the translations from x86 to ARMv8 would be unsound. The leading and trailing DMBFULL fences with RMW accesses provide these intermediate fences in the respective program to disallow \( a = b = 0 \) in both programs.

**Mapping correctness** These fences suffice to preserve mapping correctness as stated in Theorem 1 and proved in Appendix A.1.

**Theorem 1.** The mappings in Fig. 9a are correct.

### 4.2 C11 to x86 to ARMv8 mapping

In this mapping from x86 to ARMv8 we exploit the C11 semantic rule: data race results in undefined behavior. The mapping scheme is in Fig. 9b. In this scheme we categorize the x86 load and store accesses by whether they are generated from C11 non-atomic or atomic accesses. If we know that a load/store access is generated from a C11 non-atomic load/store then we do not introduce any trailing or leading fence. We prove the correctness of the scheme (Theorem 2) in Appendix A.2.

**Theorem 2.** The mapping scheme in Fig. 9b is correct.

In §2.4 we have already demonstrated the tradeoff between the x86 \( \rightarrow \) ARMv8 and C11 \( \rightarrow \) x86 \( \rightarrow \) ARMv8 mapping schemes.

### 4.3 ARMv8 to x86 mapping

The mapping scheme is in Fig. 12b. In this scheme an ARMv8 load or load-acquire is mapped to an x86 load and a store is mapped to an x86 store operation. The scheme generates a trailing MFENCE with a store in x86 for ARMv8 release-store as \( L; p; A \subseteq b \) whereas in x86 store-load on different locations are unordered. Consider the example below.

```
L(X, 1)       St(X, 1)       St(Y, 1)
\downarrow     \uparrow        \uparrow
A(Y, 0)       \downarrow     \downarrow
fre
L(Y, 1)       \uparrow
A(X, 0)
fre
\uparrow
Ld(Y, 0)
\uparrow
Ld(X, 0)
```

(a) Disallowed in ARMv8

(b) Fences disallow the execution in x86

The scheme also maps an atomic access pair to an atomic update in x86. The DMBLD, DMBST, and ISB fences are not mapped to any access.

**Theorem 3.** The mapping scheme in Fig. 12b is correct.

**Proof Strategy** To prove Theorem 3 we first define corresponding ARMv8 execution \( X_e \) for a given x86 consistent execution \( X_t \). Next we show that \( X_e \) is ARMv8 consistent. To do so, we establish Lemma 1 and then use the same to establish Lemma 2 on x86 consistent execution. Next, we define \( x86\)-preserved-program-order (\( xppo \)) and then based on \( xppo \) we define \( x86\)-observation (\( obx \)) on an x86 execution and establish Lemma 3. Finally we prove Theorem 3 using Lemma 2 and Lemma 3. The detailed proofs of Lemmas 1 to 3 and Theorem 3 are discussed in Appendix A.3.

\[ obx \triangleq rfe \cup coe \cup fre \cup [U] \cup xppo \]

where \( xppo \triangleq s_1 \cup s_2 \cup s_3 \cup s_4 \cup s_5 \cup s_6 \cup s_7 \cup s_8 \)

12
the first thread along with other relations disallows this behavior. Consider the following example.

Consider Leading and trailing fences for release-store mapping necessary for the same reasons.

The mapping scheme is in Fig. 13a. Now we show that the fences along with memory accesses are necessary to prove Theorem 4. The detailed proofs of Lemma 4, helper lemmas, and Theorem 4 are in Appendix A.5.

Based on Lemma 4 along with other helper lemmas we prove the mapping soundness Theorem 4. The detailed proofs of Lemma 4 helper lemmas, and Theorem 4 are in Appendix A.5.

4.4 ARMv7 to ARMv8 mappings

The mapping scheme in Fig. 12a from ARMv7 to ARMv8 is straightforward as no fence is introduced along with any memory access.

Theorem 4. The mappings in Fig. 12a are correct.

To prove Theorem 4 we relate preserved-program-order (ppo) in ARMv7 to Ordered-before (ob) relation in ARMv8. In ARMv7 ppo relates intra-thread events and in ARMv8 dob, bob, and aob relates intra-thread event pairs. Note that ARMv8 dob, bob, and aob relations together are not enough to capture the ARMv7 ppo relation as the detour component of ppo involves inter-thread relations. However, ARMv7 detour relation implies obs relation in ARMv8 and therefore we can relate ppo and ob relations. Considering these aspects we state the following lemma.

Lemma 3. Suppose X = ⟨E, po, rf, mo⟩ is an x86 consistent execution. For each obx path between two events there exists an alternative ⟨X, xhb U X, fr U X, co⟩+ path between these two events which has no intermediate load event.

4.5 ARMv8 to ARMv7 mapping

The mapping scheme is in Fig. 13a. Now we show that the fences along with memory accesses are necessary to preserve mapping soundness. In [4][8][2], we have already shown that LDR → LDR; CBISB is unsound and therefore LDR → LDR; DMB is necessary for correctness. Similarly, LDAR → LDR; CBISB is unsound and LDAR → LDR; DMB is necessary for the same reasons.

Leading and trailing fences for release-store mapping Consider po; [L] ⊆ bob in ARMv8. The bob relation in the first thread along with other relations disallows this behavior. Consider the following example.
Suppose Lemma 8. Using Lemma 7 we establish the acyclicity of write-order in ARMv7-mca source execution.

The mapping schemes, ARMv8 to ARMv7-mca and C11 to ARMv8 to ARMv7-mca, are shown in Fig. 13. The soundness proofs are same as Theorems 5 and 6 respectively. We have already discussed in §2.3 why mapping of a load access requires a trailing DMB fence to preserve correctness.

**Theorem 5.** The mappings in Fig. 13a are correct.

To prove Theorem 5 we relate ARMv8 and ARMv7 consistent executions in Lemma 5 and Lemma 6 as intermediate steps. Lemma 5, Lemma 6, and Theorem 5 are proved in Appendix A.6.

**Lemma 5.** Suppose $X_s$ is an ARMv8 consistent execution and $X_o$ is ARMv7 execution following the mappings in Fig. 13a. In this case $X_o, ob \implies (X_t, fre \cup X_t, coe \cup X_t, fre \cup X_t, rmw \cup X_t, fence)^+$. (a) Disallowed in ARMv8

**Lemma 6.** Suppose $X_s$ is an ARMv7 consistent execution and $X_o$ is ARMv8 execution following the mappings in Fig. 13a. In this case either $X_s, ob \implies ((X_t, E \times X_t, E)|_{loc} \setminus |E|)$ or $X_s, ob \implies (X_t, co; X_t, prop \cup X_t, prop)^+$. (b) Fences disallow the execution in ARMv7

**4.6 C11 to ARMv8 to ARMv7 mapping**

Similar to C11 → x86 → ARMv8 we propose C11 to ARMv8 to ARMv7 mapping scheme in Fig. 13b. The proof is discussed in detail in Appendix A.7. In §2.4 we already show that this mapping scheme is more efficient than ARMv8 to ARMv7 mapping.

**Theorem 6.** The mapping scheme in Fig. 13b is correct.

**4.7 ARMv7-mca to ARMv8 mapping**

The mapping scheme for ARMv7-mca to ARMv8 is same as the ARMv7 to ARMv8 mapping scheme as shown in Fig. 12a. To prove the mapping soundness we relate an ARMv7 consistent execution to corresponding ARMv8 execution as follows.

**Lemma 7.** Suppose $X_s$ is an ARMv8 consistent execution and $X_o$ is corresponding ARMv7 consistent execution. In that case $[X_s, Ld]; X_s, ppo; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \implies [X_t, Ld]; X_t, ob; [X_t, St]$

Using Lemma 7 we establish the acyclicity of write-order in ARMv7-mca source execution.

**Lemma 8.** Suppose $X_s$ is a target ARMv8 consistent execution and $X_o$ is corresponding ARMv7 consistent execution. In this case $X_s, wo \implies$ is acyclic.

The detailed proof of Lemma 7 are Lemma 8 are discussed in Appendix A.8. The mapping correctness theorem below directly follows from Lemma 8.

**Theorem 7.** The mappings in Fig. 12a are correct for ARMv7-mca.

**4.8 ARMv8 to ARMv7-mca and C11 to ARMv8 to ARMv7-mca mappings**

The mapping schemes, ARMv8 to ARMv7-mca and C11 to ARMv8 to ARMv7-mca, are shown in Fig. 13. The soundness proofs are same as Theorems 5 and 6 respectively. We have already discussed in §2.3 why mapping of a load access requires a trailing DMB fence to preserve correctness.
On Architecture to Architecture Mapping for Concurrency

5 Common Compiler Optimizations in ARMv8

In this section we study the correctness of independent access reordering, redundant access elimination, and access strengthening in ARMv8 model. We prove the correctness of the safe transformations in Appendix B.

Reorderings. We show the safe (√) and unsafe (X) reordering transformations of the form \( a \cdot b \rightarrow b \cdot a \) in Fig. 14 where \( a \) and \( b \) represent independent and adjacent shared memory accesses on different locations. We prove the correctness of the safe reorderings in Appendix B.1.

In Fig. 5 we have already shown that we cannot move a store before any load or store in. Same reasoning extends to release-store and acquire-load. It is not safe to move a store before any fence as it may violate a do relation. Similarly a load cannot be moved before an acquire load, DMBLD, or DMBFULL operation as it may remove a bo relation. However, reordering with a DMBST is safe as the ordering between them do not affect any component of ob relation. A release-store may safely reorder with a preceding fence as it does not eliminate any bo relation. Similarly moving a load, store, or DMBST after an acquire-read is allowed as it does not eliminate any existing bo relation. We may safely reorder acquire-read with DMBFULL as it does not affect the ob relations among the memory accesses. A DMBLD between a load and a load or store creates bo relation. Hence moving a load after DMBLD may eliminate a bo and therefore disallowed.

Finally reorderings fences are safe as it preserves the bo relations between memory accesses.

Redundant access elimination In §2.5 we have shown that overwritten-write and read-after-write transformations are unsound. However, a read-after-read elimination is safe in ARMv8 as enlisted in Fig. 14. We prove the correctness of the transformation in Appendix B.2.

Access strengthening Strengthening memory accesses and fences may introduce new ordering among events and therefore the strengthening transformations enlisted in Fig. 14 hold trivially.

6 Fence Optimizations

In this section we prove the correctness of various fence eliminations and then propose respective fence elimination algorithms. More specifically, the proposed mapping schemes in §4 may introduce fences some of which are redundant in certain scenarios and can safely be eliminated. To do so, we first check if a fence is non-eliminable. If not, we delete the fence.

6.1 x86 fence elimination

In x86 only a store-load pair on different locations is unordered. Therefore if a fence appear between such a pair then it is not safe to eliminate the fence. Otherwise we may eliminate a fence.

Theorem 8. An MFENCE in an x86 program thread is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

An MFENCE elimination is safe when it is not non-eliminable.

We prove the theorem in Appendix C.1. This fence elimination condition is particularly useful after ARMv8 to x86 mapping following the scheme in Fig. 12b as it introduces certain redundant fences. For instance, ARMv8 to x86 mapping STLR; STR \( \rightarrow \) WMOV; MFENCE; WHOV results in an intermediate MFENCE which is redundant and can be safely deleted as stores are ordered in x86.
6.2 ARMv8 fence elimination (after mapping)

We identify non-eliminable DMFULL, DMB, and DMBST fences and then safely eliminate rest of the fences. We prove the correctness of these fence eliminations in Appendix C.2.

For instance, considering the Fig. 9a mapping scheme, the DMBLD fence after RMOV; WMOV \(\rightarrow\) LDR; DMBLD; DMBST; STR mapping suffices to order the load and store access pair and the DMBST is not required. However, we cannot immediately conclude that such a DMBST fence is entirely redundant if we consider a mapping WMOV; RMOV \(\rightarrow\) DMBST; STR; LDR; DMBLD; DMBST; STR where the second DMBST orders the two stores and therefore non-eliminable.

**Theorem 9.** Suppose an ARMv8 program is generated by x86 \(\rightarrow\) ARMv8 mapping (Fig. 9a). A DMFULL in a thread of the program is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

A DMFULL elimination is safe when it is not non-eliminable.

While fence weakening can be applied on any ARMv8 program, it is especially applicable when ARMv7/ARMv7-mca to ARMv8 mapping. ARMv7 has only DMB fence (except ISB) to order any pair of memory accesses and these DMB fences translates to DMFULL fence in ARMv8. In many cases these DMFULL fences can be weakened and then we can eliminate DMBLD and DMBST fences which are not non-eliminable.

**Theorem 10.** A DMFULL in a program thread is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

For such a fence DMFULL \(\rightarrow\) DMBST; DMBLD is safe.

6.3 Fence Elimination in ARMv7

In ARMv7 we safely eliminate repeated DMB fences. ARMv7 DMB fence elimination is particularly useful after ARMv8 to ARMv7/ARMv7-mca mappings. For example, LDR; STLR \(\rightarrow\) LDR; DMB; DMB; STR; DMB generates repeated DMB fences and one of them can be safely eliminated.

**Theorem 11.** A DMBST in a program thread is non-eliminable if it is placed on a program path between a pair of stores in the same thread which access different locations and there exists no other DMFULL or DMBST fence on the same path.

A DMBST elimination is safe when it is not non-eliminable.

**Theorem 12.** A DMBLD in a program thread is non-eliminable if it is placed on a program path from a load to a store or load access in the same thread which access different locations and there exists no other DMFULL or DMBLD fence on the same path.

A DMBLD elimination is safe when it is not non-eliminable.

We first check if a fence is *non-eliminable* based on the access pairs and fence locations on the program paths. We perform this analysis on the thread’s control-flow-graph \(G = (V, E)\) where \(G, V\) denotes the program statements including the accesses and \(G, E\) represents the set of edges between pair of statements. Next, we delete a fence if it is not non-eliminable.

In Fig. 15 we define a number of conditions which we use in fence elimination. Condition Reach\((G, i, j)\) holds if there is a path from instruction \(i\) to instruction \(j\) in \(G\) and Path checks if there is any path from \(i\) to \(j\) through a fence \(f\). mpairs\((G, a, b)\) is a set of \((a \times b)\) memory access pairs in \(G\). We compute mpairs\((G, a, b)|_{\not\text{loc}}\); the set of memory access pairs on different locations based on must-alias analysis. FDELETE deletes a set of fences. Procedure GETNFs updates the set of non-eliminable fences considering the positions of other fences between the access pairs. Given a fence \(f\) and an access pair \((i, j)\), we check if there is a path from \(i\) to \(j\) through \(f\) without passing through already identified non-eliminable fences \(B\). If so, fence \(f\) is also non-eliminable.
reach \( (G, i, j) \triangleq (i, j) \in [G, V]; G, E^+; [G, V] \) \nach \( \text{Path}(G, i, f, j) \triangleq \text{Reach}(G, i, f) \land \text{Reach}(G, f, j) \)

\[
\text{ReachWO}(G, i, j, F) \triangleq \text{Reach}((G, V \setminus F, G, E \setminus B), i, j) \quad \text{where} \quad B = (G, V \times F) \cup (F \times G, V)
\]

\( \text{NFS}(G, i, f, j, F) \triangleq \text{Path}((G, V \setminus F, G, E \setminus B), i, f, j) \quad \text{where} \quad B = (G, V \times F) \cup (F \times G, V) \)

\[\text{mpairs}((G, a, b) \triangleq \{(i, j) \mid [i] \in a \land [j] \in b \land \text{Reach}(G, i, j)\} \]

\[\text{mpairs}((G, a, b) \mid \#_{\text{loc}} \triangleq \{(i, j) \mid \text{mpairs}(G, a, b) \land \neg \text{mustAlias}(i, j)\} \]

\[\text{mpairs}((G, a, b) \mid \#_{\text{loc}} \triangleq \{(i, j) \mid \text{mpairs}(G, a, b) \land \text{mustAlias}(i, j)\} \]

\[\text{FDelete}(G, F) \triangleq ((G, V \setminus F, G, E \setminus ((G, V \times F) \cup (F \times G, V))) \]

\begin{figure}[h]
\begin{algorithmic}[1]
\Procedure{\text{GetNFS}}{(G, PR, F, B)}
\For\( f \in F \)
\For\( (i, j) \in PR \)
\State \( G' \leftarrow \text{FDelete}(G, B) \)
\If\( \text{Path}(G', i, f, j) \)
\State \( B \leftarrow B \cup \{f\} \)
\State \text{break}; \quad \text{// inner loop}
\EndIf
\EndFor
\EndFor
\Return \( B \)
\EndProcedure
\end{algorithmic}
\caption{Helpers conditions and functions}
\end{figure}

\begin{figure}[h]
\begin{algorithmic}[1]
\Procedure{\text{FW}eak\text{en}}{(G, F)}
\For\( f \in F \)
\State \( V_1 \leftarrow G, V \cup \{a, b \mid [a] \in F_{\text{ID}} \land \{b\} \in F_{\text{ST}}\} \)
\State \( E_1 \leftarrow G, E \cup \{(f, a, (a, b))\} \)
\State \( E_2 \leftarrow E_1 \cup \{(e, a) \mid G, E(f, e)\} \)
\State \( E_3 \leftarrow E_2 \cup \{(e, b) \mid G, E(f, e)\} \)
\State \( G', V \leftarrow V_1 \setminus \{f\} \)
\State \( G', E \leftarrow E_3 \setminus ((G', V \times \{f\}) \cup (\{f\} \times G', V)) \)
\EndFor
\EndProcedure
\end{algorithmic}
\caption{Fence elimination algorithms after mappings.}
\end{figure}

Fence elimination in x86, ARMv7, and ARMv8. In Fig. 16 we define x86, ARMv8, ARMv7 fence elimination procedures. For instance, in x86FELIM we first identify store-load access pairs on different locations and the `MFENCE` operations in a thread. Then we identify the set of non-eliminable fences `nfs` using `getNFS` procedure. In this case we consider the positions of atomic updates along with fences as atomic updates also act as a fence. Finally `FDelete` eliminates rest of the fences.

Procedure `ARMv8FELIM` works in multiple steps for each of the fences. Note that while mapping to ARMv8 we do not use release-write or acquire-load accesses. Therefore we use the same `ReachWO` condition to check if a fence is non-eliminable. Moreover, in case of x86 to ARMv8 we eliminate `DMBFULL` fences. In this case `DMBFULL` elimination is safe as it introduces other `DMBLD` and `DMBST` fences. However, we do not eliminate `DMBFULL` when it is generated from ARMv7 as it may remove order between a pair of accesses. In this case or in general we can weaken a `DMBFULL` fence and then eliminate redundant `DMBST` and `DMBLD` fences.

In ARMv7 a F is redundant when it appears between a pair of same-location load-load, store-store, store-load, and atomic load-store accesses. Such redundant fences appear in ARMv7 program after mapping ARMv8 programs...
Based on this observation we check and enforce external-program-order (would have no weaker behavior and would be given program. An x86A execution is SC-robust when all  
epo results in mo shown in Fig. 18 for robustness analyses. In this model there is no as well. To avoid this complexity, we use the x86A model following Alglave et al. [2014], Alglave and Maranget as between writes on different locations and in that case we have to consider a possible through different location writes  
epo memory accesses of the memory models: these involved po  
epo relations are appropriately ordered then such a cycle would not be possible. As a result the program  
epo relations fullly to preserve SC robustness. We do not use fences by ARM  
V LDR results in a sequence  
Fence Checking robustness in x86. A subtle issue in checking SC-robustness against x86 is mo relation may take place between writes on different locations and in that case we have to consider a possible through different location writes as well. To avoid this complexity, we use the x86A model following [Alglave et al., 2014], [Alglave and Maranget as shown in Fig. 18 for robustness analyses. In this model there is no mo relation and unlike x86 an update operation results in rmw ⊆ po_loc relation instead of an event similar to ARM models. In Fig. 18 we also define SC model [Alglave et al., 2014], [Alglave and Maranget for robustness analysis.

Robustness conditions In Fig. 17 we define the conditions which have to be fulfilled by epo in all executions for a given program. An x86A execution is SC-robust when all epo relations are fully ordered as defined in (SC-x86A). In ARMv8 model condition (SC-ARMv8) preserves order for all epo relations. Condition (x86A-ARMv8) orders all epo relations except non-RMW store-load access pairs on different locations similar to x86A. ARMv7 model uses po_loc and fence to order epo relations fully to preserve SC robustness. We do not use ppo in these constraints as it violates robustness as shown in the example in Fig. 18. To preserve x86A robustness, ARMv7 orders all epo relations except
Theorem 14. A program $\mathcal{P}$ is $M$-robust against $K$ if in all its $K$ consistent execution $X$, $X.epo \subseteq X.R$ holds where $R$ is defined as condition (M-$K$) in Fig. 17.
ReachWO(G, i, j, F) ≜ Reach((G \ V \ F, G, E \ B), i, j) where B = (G \ V \ F) \cup (F \times G) \ V

RA(i, Rel, Acq) ≜ \{a | \neg ReachWO(G, i, a, Rel) \land a \in Acq\}

isSt(i) ≜ [i] \in St

isSC(i) ≜ [i] \in St \cap \text{dom}(rmw)

isLd(i) ≜ [i] \in Ld

isAcq(i) ≜ [i] \in A

isLL(i) ≜ [i] \in Ld \cap \text{dom}(rmw)

isW(i) ≜ [i] \in St \cup L

isR(i) ≜ [i] \in Ld \cup A

1: procedure ORDERED(G, i, j)
2: \text{FF} \leftarrow \{f \mid f \in G.V \land [f] \in F\};
3: \text{FL} \leftarrow \{f \mid f \in G.V \land [f] \in F.LD\};
4: \text{A} \leftarrow \{a \mid a \in G.V \land [a] \in A\};
5: switch(i, j)
6: Case mustAlias(i, j):
7: Case isSt(i) \land isLd(j) \land \neg ReachWO(G, i, j, B);
8: Case (isRel(i) \lor isAcq(i)) \land isSt(i) \land isLd(j):
9: Case isLd(i) \land isLd(j) \land \neg ReachWO(G, i, j, B \cup FL);
10: Case isLd(i) \land isSt(j) \land \neg ReachWO(G, i, j, B \cup FL \cup Lcoi(G, j));
11: Case isSt(i) \land isSt(j) \land \neg ReachWO(G, i, j, B \cup FL \cup Lcoi(G, j));
12: Case (isLL(i) \lor isLd(i)) \land (isSt(j) \lor isSC(j)): return true;
13: return false;

(a) Checking order for pairs

1: procedure SCROBUSTARMv8(\mathbb{P}, N)
2: \ell \leftarrow St \cup Ld \cup L \cup A
3: A \leftarrow \bigcup_{i \in N} \text{mpairs}(P(i), \ell, \ell);
4: O \leftarrow \emptyset
5: for (a, b) \in \text{OnCyc}(A) do
6: \text{B} \leftarrow \text{GETB}(\text{getG}(b))
7: if \neg \text{Ordered}(\text{getG}(b), a, b) then
8: \text{O} \leftarrow O \cup \{(a, b)\}
9: if O == \emptyset then return true;
10: else \text{INSERTDMBv8}(\mathbb{P}, O);
11: end procedure

(b) SC-robust against ARMv8

1: procedure X86ROBUSTARMv8(\mathbb{P}, N)
2: \ell \leftarrow St \cup Ld \cup L \cup A
3: A \leftarrow \bigcup_{i \in N} \text{mpairs}(P(i), \ell, \ell);
4: O \leftarrow \emptyset
5: for (a, b) \in \text{OnCyc}(A) do
6: s \leftarrow \text{getG}(b)
7: B \leftarrow \text{GETB}(G)
8: C \leftarrow isW(i) \land isR(j) \land (isSC(i) \land isLL(j))
9: if \neg (C \lor \text{Ordered}(G, a, b)) then
10: O \leftarrow O \cup \{(a, b)\}
11: if O == \emptyset then return true;
12: else \text{INSERTDMBv8}(\mathbb{P}, O);
13: end procedure

(c) x86 robust against ARMv8

Figure 21: Robustness analysis of ARMv8 programs

7.1 Checking and enforcing robustness

When an execution is K-consistent but violates M consistency then it forms a cycle which violates certain irreflexivity condition. Such a cycle contain events on different locations and therefore two or more edge edges where given such an edge edge (a, b) there exists other edge edge(s) (p, q) and (r, s) such that a and b access the same locations as p and s respectively as (b, p), (s, a) ∈ eco.

We lift this semantic notion of robustness to program syntax in order to analyze and enforce robustness. We first identify the memory access pairs in all threads as these are potential edge edges. Next, we conservatively check if the memory access pairs would satisfy the robustness conditions in Fig. 17 in all its K consistent executions. If so, we report the program as M-robust against K. To enforce robustness we insert appropriate fences between the memory access pairs.

We perform such an analysis in Fig. 19 to check and enforce SC-robustness against in x86 programs by procedure SCROBUSTX86 using a number of helper conditions. ReachWO(G, i, j, F) checks if there is a program path from access i to access j without passing through the fences F in G. Ordered(G, (i, j), F) checks if (i, j) access pair...
Finally, given a set of memory access pair $A$ which in turn ensure SC-robust for the program conditions. The mayAlias result in $\text{epo}$ on $\text{x86}$. Otherwise, we insert fences between unordered pairs using $\text{SCR OBUSTX}$ to enforce robustness. Similar to SCROBUSTX86 we also define procedures in Fig. 21 and Fig. 22 respectively to check and enforce robustness in ARMv7 programs.

Figure 22: Robustness analysis of ARMv7 programs

ordered in respective models. For example, in Fig. 19 it checks if $i$ and $j$ access same location using mustAlias or on all paths from $i$ to $j$ there exists a at least a fence from $F$ by ReachWO.

Finally, given a set of memory access pair $A$, OnCyc($A) \subseteq A$ identifies the set of memory access pairs which may result in epo edges in an execution. SCROBUSTX86 checks if all such store-load access pairs appropriately ordered which in turn ensure SC-robust for the program $\mathbb{P}$ having $N$ thread functions. If so, we report SC-robustness against x86. Otherwise, we insert fences between unordered pairs using INSERTF procedure to enforce robustness. Similar to SCROBUSTX86 we also define procedures in Fig. 21 and Fig. 22 respectively to check and enforce robustness in ARMv8 and ARMv7 programs.

8 Experimental Evaluation

Based on the obtained results we have implemented arachitecture to architecture (AA) mapping schemes defined in Figs. 9, 12 and 13 followed by fence elimination algorithms described in Fig. 16. We have also developed robustness analyses for x86, ARMv8, and ARMv7 programs following the procedures in Figs. 19, 21 and 22.

We have implemented these mappings, fence eliminations, and robust analyses in LLVM. To analyze programs for fence elimination and checking robustness, we leverage the existing control-flow-graph analyses, alias analysis, and memory operand type analysis in LLVM. The CFG analyses are used to define $\text{mpairs}$, $\text{Path}$, Reach, and ReachWO conditions. The mayAlias and mustAlias functions are defined using memory operand type and alias analyses.
We have experimented these implementations on a number of well-known concurrent algorithms and data structures which use C11 concurrency primitives extensively. These programs exhibit fork-join concurrency where the threads are created from a set of functions. In these programs the memory accesses are relaxed accesses in general and for wait loops we use release/acquire accesses. Some of the programs have release-acquire/TSO/SC versions. These programs assume the program would run on the respective memory models.

### 8.1 Mapping Schemes

We have modified the x86, ARMv7, and ARMv8 code generation phases in LLVM to capture the effect of mapping schemes on C11 programs. For example, in original LLVM mapping a non-atomic store (St,rel) results in WMOV and STR accesses in x86 and ARMv8 respectively. Following the AA-mapping in Fig. 9a, WMOV results in DM suspense; STR in ARMv8. Therefore to capture the effect of x86 to ARMv8 translation we generate DM suspense; STR in ARMv8 instead of a STR for a C11 non-atomic store access. We modify the code lowering phase in LLVM to generate the required leading and trailing fences along with the memory accesses. The AA-mapping schemes introduce additional fences compared to original mapping in all mapping schemes which is evident in Figs. 23a, 23b, 24a and 24b in ‘Orig’ and ‘AA’ columns respectively.

We have modified the x86, ARMv7, and ARMv8 code generation phases in LLVM to capture the effect of mapping schemes on C11 programs. For example, in original LLVM mapping a non-atomic store (St,rel) results in WMOV and STR accesses in x86 and ARMv8 respectively. Following the AA-mapping in Fig. 9a, WMOV results in DM suspense; STR in ARMv8. Therefore to capture the effect of x86 to ARMv8 translation we generate DM suspense; STR in ARMv8 instead of a STR for a C11 non-atomic store access. We modify the code lowering phase in LLVM to generate the required leading and trailing fences along with the memory accesses. The AA-mapping schemes introduce additional fences compared to original mapping in all mapping schemes which is evident in Figs. 23a, 23b, 24a and 24b in ‘Orig’ and ‘AA’ columns respectively.

#### x86 to ARMv8 mappings (Fig. 23a)

In Fig. 23a we show the numbers of different fences resulted from C11 → ARMv8 (Orig), x86 → ARMv8 (AA in x86), and C11 → x86 → ARMv8 (AA in C-x-v8). Both x86 → ARMv8 and C11 → x86 → ARMv8 mapping schemes generate more fences compared to the original C11 → ARMv8 mapping. x86 → ARMv8 (x-v8) generates more DM suspense fences compared to C11 → x86 → ARMv8 (C-x-v8) as the earlier scheme generates trailing DM suspense fence for non-atomic loads. However, the number of DM suspense fences are more in C-x-v8 compared to x-v8 as atomic stores introduce leading DM suspense fences instead of DM suspense. For the same reason there is no DM suspense in C-x-v8 column.

#### ARMv8 to x86 mappings (Fig. 23b)

As shown in Fig. 23b the number of atomic updates and fence operations in AA-mapping varies from Orig due to the mapping of C11 St,SC and St,REL accesses. In original mapping St,SC → RM suspense and St,REL → WMOV whereas in AA-mapping St,REL[SC] → STR suspense WMOV; MFENCE. As a result, the number of
atomic updates are less and the number of fences are more in AA-mapping compared to the original x86 mapping in LLVM. We can observe the tradeoff between \( \text{x86} \rightarrow \text{ARMv8} \) and \( \text{C11} \rightarrow \text{ARMv8} \) considering the number of generated DMBLD and DMBFULL fences. For example, in Barrier program \( \text{x86} \rightarrow \text{ARMv8} \) generates more DMBLD than \( \text{C11} \rightarrow \text{x86} \rightarrow \text{ARMv8} \) as it generates DMBLD fences for non-atomic loads. On the other hand, \( \text{C11} \rightarrow \text{x86} \rightarrow \text{ARMv8} \) generates DMBFULL fences for relaxed atomic stores instead of DMBST fences.

**ARMv8 to ARMv7 mappings (Fig. 24a)** We show the number of DMB fences in Fig. 24b due to \( \text{C11} \rightarrow \text{ARMv8} \) (Orig), ARMv8\( \rightarrow \)ARMv7 (AA in v8-v7), \( \text{C11} \rightarrow \text{ARMv8} \rightarrow \text{ARMv7} \) (AA in C-v8-v7) mappings. Both ARMv8\( \rightarrow \)ARMv7 and \( \text{C11} \rightarrow \text{ARMv8} \rightarrow \text{ARMv7} \) generate more fences than \( \text{C11} \rightarrow \text{ARMv8} \) mapping. Moreover, \( \text{C11} \rightarrow \text{ARMv8} \rightarrow \text{ARMv7} \) generates less number of fences than ARMv8\( \rightarrow \)ARMv7 as we do not generate trailing DMB fences for non-atomic loads.

**ARMv7 to ARMv8 mappings (Fig. 24a)** The result is in Fig. 24a where The original \( \text{C11} \rightarrow \text{ARMv8} \) mapping generates DMBFULL, release-store, and acquire-load operations for these programs whereas the AA-mapping generates respective DMBFULL fences only as ARMv7 does not have release-store, and acquire-load operations.

### 8.2 Fence elimination

The fence optimization passes remove significant number of fences as shown in the 'fd' columns in Figs. 23a, 23b, and 24b. We have implemented the fence elimination algorithms as LLVM passes and run the pass after AA-mappings to eliminate redundant fences. The pass extends LLVM MachineFunctionPass and run on each machine function of the program. The precision of our analyses depend upon underlying LLVM functions which we have used. For example, we apply alias analysis and memory operand analysis to identify the memory location accessed by a particular access. Consider a scenario where we have identified an HFENCE between a store-load pair. If we precisely identify that the store-load pair access same-location then we can eliminate the fence. Otherwise we conservatively mark the fence as non-eliminable.

**Fence elimination after x86 to ARMv8 mapping.** The fence elimination algorithms have eliminated a number of redundant fences after the mapping. In some scenarios original C11 to ARMv8 mapping is too restrictive as it generates
release-store and acquire-load accesses for C11 release-store and acquire-load accesses respectively. In our scheme we prefer to generate fences separately and fence elimination eliminates those extra fences.

Fence elimination after C11 to x86 to ARMv8 mapping. In this case we first weaken the DMBFULL fences to a pair of DMBS and DMBLD fences whenever appropriate and then perform the fence elimination. Therefore it introduces some DMBS fences in the ‘fd’ column in C-x-v8.

Fence elimination after ARMv8 to x86 mapping. The mapping generates MFENCE for release-store mapping and the fence elimination safely eliminate these fences whenever possible.

Fence elimination after ARMv7 to ARMv8 mapping. In this case the mapping introduce DMBFULL fences in ARMv8 from ARMv7 DMB fences. We eliminate the repeated fences if any and then weaken the DMBFULL fences to DMBS and DMBLD fences, and further eliminate redundant fences.

Fence elimination after ARMv8 to ARMv7 mapping. ARMv8 to ARMv7 mapping generates extra fences in certain scenarios such as LDR; STLR $\rightarrow$ LDR; DMB; DMB; STR; DMB where we can safely remove a repeated DMB fence. Similar scenario takes place for LDR; STLR mapping in C11 to ARMv8 to ARMv7 mapping.

8.3 Robustness analysis

We implement the robustness analysis as LLVM passes following the procedures in Fig. 19 as well as following Figs. 21 and 22 in the appendix after instruction lowering in x86, ARMv8, and ARMv7. We report the analyses results on the concurrent programs in Fig. 25. In these results we mark both robustness checking and robustness enforcement results. We have also included the results from Lahav and Margalit [2019] about two other robustness checker: Trencher Bouajjani et al. [2013] and Rocker Lahav and Margalit [2019].

Now we discuss the robustness results of the benchmarks programs which are marked by $\checkmark$ or $\times$. Among these programs spinlock, spinlock4, seqlock, ticketlock (tlock), and ticketlock4 (tlock4) provide robustness in all models. These

| Prog. | x86A | ARMv8 | ARMv7 | Rocker (RA) | Trencher (TSO) |
|-------|------|-------|-------|-------------|---------------|
|       | SC   | x86A  | v8    | mca         | SC            |
| barrier | 8/101 | 12/6X | X5    | 12/10X1     | (2)           |
| dekker-tso | 20/4  | 20/8X | X6    | 20/8X8      | (2)           |
| dekker-sc | 20/0  | 20/4X12 | X9    | 20/4X12     | (2)           |
| pn-ra | 12/4 | 12/4X12 | X7    | 12/4X8      | (2)           |
| pn-ra-b | 10/0  | 12/10X2 | X2    | 12/12X2     | (2)           |
| pn-ra-d | 10/0  | 12/4X8 | X8    | 12/6X8      | (2)           |
| pn-tso | 12/2  | 12/2X9 | X9    | 12/2X10     | (2)           |
| pn-sc | 12/0  | 12/0X11 | X11   | 12/0X10     | (2)           |
| lmprt-ra | 19/4X8 | 18/13X7 | X4    | 19/13X6     | (2)           |
| lmprt-tso | 17/2X6 | 16/9X11 | X10   | 17/9X8      | (2)           |
| lmprt-sc | 17/0  | 16/7X14 | X13   | 17/7X10     | (2)           |
| spinlock | 8/0   | 10/8   | X3    | 12/8        | (2)           |
| spinlock4 | 16/0  | 20/16  | X2    | 24/24       | (2)           |
| tlock | 10/0  | 10/6   | X3    | 12/8        | (2)           |
| tlock4 | 20/0  | 20/6   | X3    | 24/16       | (2)           |
| seqlock | 7/0   | 11/8X3 | X3    | 11/8X1     | (2)           |
| abw | 15/0  | 18/2X12 | X12   | 20/1X10     | (2)           |
| rcu | 27/0X10 | 25/10X16 | X12   | 27/10X18    | (2)           |
| rcu-off | 30/4X7 | 33/14X27 | X25   | 36/19X17    | (2)           |
| cilk-tso | 11/2  | 28/6X8 | X8    | 29/10X7     | (2)           |
| cilk-sc | 11/0  | 28/4X9 | X9    | 29/18X8     | (2)           |
| cldq-ra | 9/3   | 11/5X3 | X3    | 11/5X3     | (3)           |
| cldq-tso | 9/1   | 11/3X5 | X5    | 11/3X5     | (3)           |
| cldq-sc | 9/0   | 11/2X6 | X7    | 11/2X6     | (3)           |

Figure 25: Robustness analyses. Entry (a/b/ $\checkmark$) where a: # fences inserted by naive scheme excluding the existing fences, b: #fences inserted to enforce robustness, [c] #fences inserted by naive scheme excluding the existing fences to enforce robustness. Rocker and Trencher robustness results (for #k number of threads) are taken from Lahav and Margalit [2019]. Our SC-robustness against x86A analysis matches Trencher in a number of cases. ARMv8 and ARMv7 is weaker than RA and therefore we report non-robustness in these programs.
results also match the results from both Trencher and Rocker; both SC-robustness checkers. In rest of the programs we observe robustness violations due to various unordered accesses sequences. For example, (St-Ld) violates SC-robustness in all architectures, (SC-St/Ld) violate x86A robustness in ARMv8 and ARMv7, and (Ld-Ld) violate all robustness in ARMv8 and ARMv7 models.

**Robustness of x86 programs.** We first focus on SC-robustness against x86A and compare the result with Trencher. Our analysis precisely analyze robustness and agrees to Trencher in all cases except lamport-ra (lmprt-ra), lamport-tso (lmprt-tso), and cilk-sc. Both lamport-ra and lamport-tso has (St-Ltd) sequence in different thread functions. As a result, our analysis reports SC-robustness violation which is a false positive as in actual executions these access pairs never execute in concurrence. In cilk-sc we report SC-robustness as the program has store-load sequences of the form \( a = \text{Ld}_{RLX}(T); \text{St}_{RLX}(T, a-1); \text{Ld}_{RLX}(H) \). In this case the \( \text{St}_{RLX}(T, a-1); \text{Ld}_{RLX}(H) \) may not violate SC behavior during an execution which is reported by Trencher and Rocker. However, LLVM combines the load and store of \( T \) into an atomic fetch-and-sub operation, that is, \( a = \text{Ld}_{RLX}(T); \text{St}_{RLX}(T, a-1) \Rightarrow a = \text{fsub}(T, 1) \). As a result the program turns into SC-robust against x86 in LLVM as reported by our analysis.

**Robustness of ARMv8 programs.** Next, we study SC-robustness and x86A-robustness against ARMv8 for the benchmark programs. ARMv8 allows out-of-order executions of memory accesses on different locations which do not affect dependencies. Therefore many of these programs in ARMv8 are not SC or x86A robust. Also our robustness analyzer do not rely on do ordering as it performs the analysis before the ARMv8 machine code is generated during the code lowering phase. Therefore LLVM may perform optimizations after the analysis which may remove certain dependencies and in that case our analysis would be unsound and may report false negative.

As ARMv8 is weaker than x86A, the program which are not SC-robust in x86A are also not SC-robust in ARMv8. Programs like barrier, peterson-ra-Bartosz (pn-ra-b), peterson-sc (pn-sc), lamport-tso/sc, rcu, rcu-offline (rcu-offl), and chase-lev-dequeue-tso/sc (cldq-tso/sc) are in this category. There are programs which are SC-robust in x86 but not in ARMv8 such as dekker-tso and so on. These programs violate both SC and x86A robustness due to unordered (Ld-Ld) or (SC-St/Ld) pairs.

**Robustness of ARMv7 programs.** Now we move to the robustness analysis in ARMv7. Except spinlock, spinlock4, and seqlock programs, all other programs violate SC-robustness due to the similar pattern as discussed in ARMv8 robustness. Among these programs SC-robustness is violated in barrier due to (St-Ld) unordered sequence. This access pattern is allowed in x86A, ARMv8, and ARMv7-mca and therefore these ARMv7 programs are robust in these models. Program rcu has unordered (St-St) pairs which violates SC and x86A robustness. However, these pairs does not violate ARMv8 and ARMv7-mca robustness. Rest of the programs exhibit certain (Ld-Ld) pairs which result in x86, ARMv8, and ARMv7-mca robustness violations.

### 8.3.1 Enforcing robustness

Whenever we identify a program as non-robust we insert appropriate fences to enforce respective robustness. For example in Fig. 19 we identify the different-location store-load access pairs which may violate robustness. We introduce leading MFENCE operations for the load operation in the pair as required.

A naive scheme does not use robustness information. It first eliminates existing fences in concurrent threads and then insert fences after each memory accesses except atomic update in x86 and load-exclusive accesses in ARM models to restrict program behavior. In both naive scheme and our approach we do not insert fences for atomic update. In ARMv8 we insert DMBLD and DMBFULL trailing fences for load, and store and store-exclusive respectively when they are unordered with a successor. In ARMv7 we insert DMBFULL trailing fences for load, store, and store-exclusive when they are unordered with a successor.

In Fig. 25 we report the number of fences required in the naive scheme, robustness analyses results in our proposed approach along with the number of introduce fences to enforce robustness. We compare our result to the naive schemes as explained in Fig. 25 and find that our approach insert less number of fences in major instances. However, our fence insertion is not optimal; we leave the optimal fence insertion for enforcing robustness for future investigation.

### 9 Related Work

**Architecture to architecture mapping** There are a number of dynamic binary translators [Ding et al. 2011, Wang et al. 2011, Hong et al. 2012, Lustig et al. 2015, Cota et al. 2017] emulate multithreaded program. Among these earlier translators such as PQEMU [Ding et al. 2011, COREMU [Wang et al. 2011, HQEMU [Hong et al. 2012] and so on do not address the memory consistency model mismatches. AR MOR [Lustig et al. 2015] proposes a specification format to define the ordering requirements for different memory models which is used in translating between architectural
concurrency models in dynamic translation. The specification format is used in specifying TSO and Power architectures. Cota et al. [2017] uses the rules from ArMOR in Pico dynamic translator for QEMU. Our mapping schemes provide the ordering rules which can be used to populate the ordering tables for x86 and ARM models. Moreover the ARMv8 reordering table in Fig. 14 demonstrates that reordering certain independent access pairs are not safe if they are part of certain dependency based ordering. In addition to the QEMU based translators, LLVM based decompilers Bougacha, Bits, Yadavalli and Smith [2019], avast, Shen et al. [2012] raise binary code to LLVM IR and then compiles to another architecture. These decompilers do not support relaxed memory concurrency.

**Fence optimization** Redundant fence elimination is addressed by Vafeiadis and Zappa Nardelli [2011], Elhorst [2014], Morisset and Nardelli [2017]. Vafeiadis and Zappa Nardelli [2011] performs safe fence elimination in x86, Elhorst [2014] eliminate adjacent fences in ARMv7, and Morisset and Nardelli [2017] perform efficient fence elimination in x86, Power, and ARMv7. However, none of these approaches perform ARMv8 fence elimination.

**Robustness analysis.** Sequential consistency robustness has been explored against TSO Bouajjani et al. [2013], POWER Derevenetc and Meyer [2014], and Release-Acquire Lahav and Margalit [2019] models by exploring executions using model checking tools. Alglave et al. [2017] proposed fence insertion in POWER to strengthen a program to release/acquire semantics which has same preserved-program-order constraints between memory accesses as TSO. On the contrary, we identify robustness checking conditions in ARMv7 and ARMv8 where we show that preserved-program-order is not sufficient to recover sequential consistency in ARMv7 models. Identifying minimal set of fences is NP-hard Lee and Padua [2001] and a number of approaches such as Shasha and Smir [1988], Bouajjani et al. [2013], Lee and Padua [2001], Alglave et al. [2017] proposed fence insertion to recover stronger order, particularly sequential consistency. Similar to Lee and Padua [2001] our approach is based on analyzing control flow graphs without exploring the possible executions by model checkers. Though in certain scenarios we report false positives, our approach precisely identifies robustness for a number of well-known programs.

### 10 Conclusion and Future Work

In this paper we propose correct and efficient mapping schemes between x86, ARMv8, and ARMv7 concurrency models. We have shown that ARMv8 can indeed serve as an intermediate model for mapping between x86 and ARMv7. We have also shown that removing non-multicopy atomicity from ARMv7 does not affect the mapping schemes. We also show that ARMv8 model cannot serve as an IR in a decompiler as it does not support all common compiler optimizations. Next, we propose fence elimination algorithms to remove additional fences generated by the mapping schemes. We also propose robustness analyses and enforcement techniques based on memory access sequence analysis for x86 and ARM programs.

Going forward we want to extend these schemes and analyses to other architectures as well. We believe these results would play a crucial role in a number of translator, decompilers, and state-of-the-art systems. Therefore integrating these results to these systems is another direction we would like to pursue in future.

### References

C/C++11 mappings to processors. [https://www.cl.cam.ac.uk/~pes20/cpp/cpp0xMappings.html](https://www.cl.cam.ac.uk/~pes20/cpp/cpp0xMappings.html)

J. Alglave and L. Maranget. herd7 consistency model simulator. [http://diy.inria.fr/www/](http://diy.inria.fr/www/)

J. Alglave, L. Maranget, and M. Tautschnig. Herding cats: modelling, simulation, testing, and data-mining for weak memory. *ACM Trans. Program. Lang. Syst.*, 36(2):7:1–7:74, 2014. doi: 10.1145/2627752.

J. Alglave, D. Kroening, V. Nimal, and D. Poetzl. Don’t sit on the fence: A static analysis approach to automatic fence insertion. *ACM Trans. Program. Lang. Syst.*, 39(2):6:1–6:38, 2017.

Android-x86. [https://www.android-x86.org/](https://www.android-x86.org/)

Arm. Migrating a software application from armv5 to armv7-a/r application. [http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dai0425/chapterIntendReader.html](http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dai0425/chapterIntendReader.html)

avast. A retargetable machine-code decompiler based on llvm. [https://github.com/avast/retdec](https://github.com/avast/retdec)

A. Barbalace, R. Lyerly, C. Jelesnianski, A. Carno, H. Chuang, V. Legout, and B. Ravindran. Breaking the boundaries in heterogeneous-isa datacenters. In *ASPLOS 2017*, pages 645–659, 2017. doi: 10.1145/3037697.3037738.

A. Barbalace, M. L. Karaoui, W. Wang, T. Xing, P. Olivier, and B. Ravindran. Edge computing: the case for heterogeneous-isa container migration. In *VEE’20*, pages 73–87, 2020. doi: 10.1145/3381052.3381321.

L. Bits. Framework for lifting x86, amd64, and aarch64 program binaries to llvm bitcode. [https://github.com/lifting-bits/mcsema](https://github.com/lifting-bits/mcsema)
A. Bouajjani, E. Derevenetc, and R. Meyer. Checking and enforcing robustness against TSO. In ESOP 2013, pages 533–553, 2013. doi: 10.1007/978-3-642-37036-6_29.

A. Bougacha. Binary translator to llvm ir. https://github.com/repzret/dagger.

A. Chernoff, M. Herdeg, R. Hookway, C. Reeve, N. Rubin, T. Tye, S. Bharadwaj Yadavalli, and J. Yates. Fx32 a profile-directed binary translator. IEEE Micro, 18(2):56–64, 1998.

E. G. Cota, P. Bonzini, A. Bennée, and L. P. Carloni. Cross-isa machine emulation for multicores. In CGO’2017, page 210â ˘A¸ S220. IEEE Press, 2017.

E. Derevenetc and R. Meyer. Robustness against power is pspace-complete. In ICALP’14, volume 8573 of LNCS, pages 158–170, 2014. doi: 10.1007/978-3-662-43951-7_14.

J. Ding, P. Chang, W. Hsu, and Y. Chung. PQEMU: A parallel system emulator based on QEMU. In ICPADS’11, pages 276–283, 2011. doi: 10.1109/ICPADS.2011.102.

M. Docs. How x86 emulation works on arm. https://docs.microsoft.com/en-us/windows/uwp/porting/apps-on-arm-x86-emulation.

R. Elhorst. Lowering C11 atomics for ARM in LLVM. In European LLVM Conference, 2014.

D.-Y. Shen, J.-Y. Chen, W.-C. Hsu, and W. Yang. Llbt: An llvm-based static binary translator. In CASES 2012, page 51â ˘A¸ S60, 2012. doi: 10.1145/2380403.2380419.

V. Vafeiadis and F. Zappa Nardelli. Verifying fence elimination optimisations. In SAS’11, volume 6887 of LNCS, pages 146–162. Springer, 2011. doi: 10.1007/978-3-642-23702-7_14.

Z. Wang, R. Liu, Y. Chen, X. Wu, H. Chen, W. Zhang, and B. Zang. COREMU: a scalable and portable parallel full-system emulator. In C. Cascaval and P. Yew, editors, PPOPP’11, pages 213–222, 2011. doi: 10.1145/1941553.1941583.

J. Wickerson, M. Batty, T. Sorensen, and G. A. Constantinides. Automatically comparing memory consistency models. In POPL’17, pages 190–204. ACM, 2017. doi: 10.1145/3009837.3009838.

S. B. Yadavalli and A. Smith. Raising binaries to llvm ir with metcoll (wip paper). In LCTES 2019, page 213â ˘A¸ S218, 2019. doi: 10.1145/3316482.3326354.
A Proofs of Mapping Schemes

A.1 \textit{x86} to ARMv8 Mappings

We first restate Theorem 1.

\textbf{Theorem 1.} The mappings in Fig. 9 are correct.

To prove Theorem 1 we prove the following formal statement.

\[ \forall X_t \in [\text{ARMv8}], \exists X_s \in [\text{x86}]. \text{Behavior}(X_t) = \text{Behavior}(X_s) \]

Given an ARM execution $X_t$ we define corresponding x86 execution $X_s$ where

1. $[X_t.\text{St} \cup X_t.\text{F}]; X_t.\text{ob}; [X_t.\text{St} \cup X_t.\text{F}] \Rightarrow X_s.\text{mo}$
2. $[X_t.\text{St} \cup X_t.\text{F}]; X_t.\text{po}; [X_t.\text{St} \cup X_t.\text{F}] \Rightarrow X_s.\text{mo}$
3. $[X_s.\text{F}]; X_t.\text{po}; X_t.\text{fr} \Rightarrow X_s.\text{mo}$
4. $X_t.\text{co} \Rightarrow X_s.\text{mo}|_{\text{loc}}$

We know that $X_t$ is ARMv8 consistent. Now we show that $X_s$ is x86 consistent.

\textbf{Proof.} We prove by contradiction.

\textbf{(irrHB)}

Assume $X_s$ has an $X_s.\text{xhb}$ cycle.

It implies a $(X_s.\text{po} \cup X_s.\text{rfe})^+$ cycle.

Considering the possible cases of $X_s.\text{po}$ edges on the cycle:

\textbf{Case} $[X_s.\text{Ld}]; X_s.\text{po}; [X_s.\text{W}]$:

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{po}; [X_t.\text{F}_\text{Ld}]; X_t.\text{po}; [X_t.\text{W}]. \]

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{bob}; [X_s.\text{W}] \]

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{ob}; [X_s.\text{W}] \]

\textbf{Case} $[X_s.\text{U}]; X_s.\text{po}; [X_s.\text{W}]$:

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{rmw}; X_t.\text{po}; [X_t.\text{F}]; X_t.\text{po}; X_t.\text{rmw}; [X_t.\text{St}] \]

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{ob}; X_t.\text{bob}; X_t.\text{bob}; [X_t.\text{St}] \]

\[ \Rightarrow [X_t.\text{Ld}]; X_t.\text{ob}; [X_t.\text{St}] \]

Thus in both cases $X_s.\text{xhb} \Rightarrow (X_t.\text{ob} \cup X_t.\text{rfe})^+ \subseteq X_t.\text{ob}$. However, $X_t$ is ARM consistent and $X_t.\text{ob}$ is irreflexive. Hence a contradiction and $X_s.\text{xhb}$ is irreflexive.

\textbf{(irrMOHB)}

Assume $X_s$ has an $X_s.\text{mo}$; $X_s.\text{xhb}$ cycle.

However, from definition, $[X_s.\text{W} \cup X_s.\text{F}]; X_s.\text{xhb} [X_s.\text{W} \cup X_s.\text{F}]$

Considering the po and rfe from xhb:

\textbf{Case} $[X_s.\text{W} \cup X_s.\text{F}]; X_s.\text{po}; [X_s.\text{W} \cup X_s.\text{F}]$:

We know,

$[X_s.\text{W} \cup X_s.\text{F}]; X_s.\text{po}; [X_s.\text{W} \cup X_s.\text{F}]$
Considering the subcases:

**Subcase** \([X_s.St \cup X_s.F]; X_s.po; [X_s.St \cup X_s.F]\):
It implies \([X_s.St \cup X_s.F]; X_s.po; [X_s.St \cup X_s.F]\).
From definitions, \([X_s.St \cup X_s.F]; X_s.po; [X_s.St \cup X_s.F]\) \(\implies X_s.mo \land \neg X_s.mo^{-1}\).

**Subcase Otherwise:**
Possible scenarios are \([X_s.U]; X_s.po; [X_s.W \cup X_s.F]\) or \([X_s.W \cup X_s.F]; X_t.po; [X_t.U]\).
Now, \([X_s.U]; X_s.po; [X_s.W \cup X_s.F]\)

\(\implies X_t.rmw; X_t.po; [X_t.F]; X_t.po; [X_t.W \cup X_t.F]\)
\(\implies X_t.ob\)
\(\implies X_t.po; [X_t.F]; X_t.po; [X_s.W]\)
\(\implies X_t.ob\)
\(\implies X_t.ob\)

From definitions, \([X_t.StX_t.F]; X_t.ob; [X_t.StX_t.F]\) \(\implies X_s.mo \land \neg X_s.mo^{-1}\).

**Case** \([X_s.W \cup X_s.F]; X_s.rfe; [X_s.W \cup X_s.F]\):
It implies \([X_s.W]; X_s.rfe; [X_s.U]\)

\(\implies (\{X_t.Ld; X_t.rmw\} \cup \{X_t.St\}; X_t.rfe; [X_t.Ld]; X_t.rmw; [X_t.St] \text{ following the mappings.}\)
\(\implies (\{X_t.Ld; X_t.aob\} \cup \{X_t.St\}; X_t.obs; [X_t.Ld]; X_t.aob; [X_t.St] \text{ or } [X_t.St]; X_t.ob; [X_t.St] \text{ following the mappings.}\)
From definitions we know that \([X_s.St]; X_t.ob; [X_t.St] \implies X_s.mo \land \neg X_s.mo^{-1}\).
Therefore \(X_s.xhb \implies X_s.mo\) and hence \(X_s.mo; X_s.xhb\) is acyclic and \(X_s\) satisfies (irrMOHB).

(irrFRHB)
Assume \(X_s\) has a \(X_s.fr; X_s.xhb\) cycle.
We already know that \(X_s.xhb \implies X_t.ob\) holds.
Considering the cases of \(X_s.fr\):

**Case** \(X_s.fre\):
In this case \(X_s.fre \implies X_t.fre \implies X_t.obs\).
In this case there exists a \(X_t.obs; X_t.ob\) cycle which violates (external) in \(X_t\).
Hence a contradiction and \(X_s\) satisfies (irrFRHB).

**Case** \(X_s.fri\):
Following the mappings \(X_s.fri \implies X_t.bob\).
In this case there exists a $X_t \cdot bob; X_t \cdot ob$ cycle which violates (external) in $X_t$.
Hence a contradiction and $X_s$ satisfies (irrFRHB).

(irrFRMO)
Assume $X_s$ has a $X_s \cdot fr; X_s \cdot mo$ cycle.
It implies a $X_s \cdot fr; X_s \cdot co$ cycle and in consequence a $X_t \cdot fr; X_t \cdot co$ cycle which violates (internal) in $X_t$.
Hence a contradiction and $X_s$ satisfies (irrFRMO).

(irrFMRP)
Assume $X_s$ has a $X_s \cdot fr; X_s \cdot mo; X_s \cdot rfe; X_s \cdot po$ cycle.
It implies a $X_s \cdot rfe; X_s \cdot po; X_s \cdot fr; X_s \cdot mo$ cycle.
Now we consider a $X_s \cdot rfe; X_s \cdot po; X_s \cdot fr$ path.
Thus $[X_s, W] ; X_s \cdot rfe; X_s \cdot po; X_s \cdot fr; [X_s, W]$

$$\implies [X_s, W] ; X_s \cdot rfe; X_s \cdot po; [X_s, R] ; X_s \cdot fre; [X_s, W]$$
$$\quad \cup [X_s, W] ; X_s \cdot rfe; X_s \cdot po; [X_s, R] ; X_s \cdot fri; [X_s, W]$$

$$\implies [X_t, St]; X_t \cdot rfe; [X_t, Ld]; X_t \cdot po; [X_t, F_{LD} \cup X_t, F]; X_t \cdot po; [X_t, Ld]; X_t \cdot fre; [X_t, St]$$
$$\quad \cup [X_t, St]; X_t \cdot rfe; [X_t, Ld]; X_t \cdot po; [X_t, F_{LD} \cup X_t, F]; X_t \cdot po; [X_t, Ld]; X_t \cdot fri; [X_t, St]$$

$$\implies [X_t, St]; X_t \cdot obs; [X_t, Ld]; X_t \cdot bob; [X_t, Ld]; X_t \cdot obs; [X_t, St]$$
$$\quad \cup [X_t, St]; X_t \cdot obs; [X_t, Ld]; X_t \cdot bob; [X_t, Ld]; X_t \cdot bob; [X_t, St]$$

$$\implies [X_t, St]; X_t \cdot ob; [X_t, St] \cup [X_t, St]; X_t \cdot ob; [X_t, St]$$
$$\implies [St]; X_t \cdot ob; [X_t, St]$$

However, we know $[X_t, St]; X_t \cdot ob; [St] \implies [X_s, W] ; X_s \cdot mo; [X_s, W]$.
Thus $[X_s, W] ; X_s \cdot rfe; X_s \cdot po; X_s \cdot fr; [X_s, W] \implies X_s \cdot mo \land \neg X_s \cdot mo^{-1}$.
Hence a contradiction and thus $X_s$ satisfies (irrFMRP).

(irrUF)
Assume $X_s$ has a $X_s \cdot fr; X_s \cdot mo; [X_s, U \cup X_s, F]; X_s \cdot po$ cycle.
It implies $[X_s, U \cup X_s, F]; X_s \cdot po; [X_s, R] ; X_s \cdot fr; [X_s, W] ; X_s \cdot mo$ cycle.
Now, we consider a $[X_s, U \cup X_s, F]; X_s \cdot po; [X_s, R] ; X_s \cdot fr; [X_s, W]$ path.
Considering possible cases:

Case $[X_s, U] ; X_s \cdot po; [X_s, R] ; X_s \cdot fr; [X_s, W]$

$$\implies [X_t, Ld]; X_t \cdot po; [X_t, F]; X_t \cdot po; [X_t, Ld]; (X_t \cdot fre \cup X_t \cdot fri); [X_t, St]$$

$$\implies [X_t, Ld]; X_t \cdot po; [X_t, F]; X_t \cdot po; [X_t, Ld]; X_t \cdot fre; [X_t, St]$$
$$\quad \cup [X_t, Ld]; X_t \cdot po; [X_t, F]; X_t \cdot po; [X_t, Ld]; X_t \cdot fri; [X_t, St]$$

30
From definition we know

Hence a contradiction and

Therefore the mapping scheme in Fig. 9b is sound.

Hence

Case $[X_s, F]; X_s, po; X_s, fr; [X_s, \mathcal{W}]$:

$\Rightarrow \ [X_s, F]; X_s, po; X_s, fr; [X_s, \mathcal{W}]$ following the mappings.

$\Rightarrow \ X_s, mo \land \neg X_s, mo^{-1}$ following the definition.

Therefore $[X_s, U \cup X_s, F]; X_s, po; X_s, fr; X_s, mo$ does not have a cycle.

Hence a contradiction and $X_s$ satisfies (irrUF).

From definition we know $X_i.co \Rightarrow X_s.mo|_{loc}$ and therefore $\text{Behavior}(X_s) = \text{Behavior}(X_i)$ holds.

\[ \square \]

A.2 Correctness of C11 to x86 to ARMv8 Mapping

We restate the theorem and then prove the same.

Theorem 2. The mapping scheme in Fig. 9d is correct.

Proof. The mapping can be represented as a combination of following transformation steps.

1. $\mathbb{P}_{C11} \mapsto \mathbb{P}_{x86}$ mapping from $\text{map}$
2. $\mathbb{P}_{x86} \mapsto \mathbb{P}_{ARMv8}$ mappings from Fig. 9a
3. Fence strengthening DMBST; STR $\mapsto$ DMBFULL; STR in $\mathbb{P}_{ARMv8}$.
4. Elimination of leading DMBFULL and trailing DMBLD fences in following cases.
   (a) DMBFULL; STR $\mapsto$ STR where $\text{WOV}_{NA} \mapsto$ STR.
   (b) LDR; DMBLD $\mapsto$ LDR where $\text{RMV}_{NA} \mapsto$ LDR.

We know (1), (2), (3) are sound and therefore it suffices to show that transformation (4) is sound.

Let $X_s$ and $X'_s$ be the consistent execution of $\mathbb{P}_{ARMv8}$ before and after the transformation (3). Let $X$ be correspondin C11 execution $\mathbb{P}_{C11}$ and we know $\mathbb{P}_{C11}$ is race-free. Therefore for all non-atomic event $a$ in $X$ if there exist another same-location event $b$ then $X hb^=(a, b)$ holds.

Now we consider x86 to ARMv8 mapping scheme in Fig. 9a.

Considering the $hb$ definition following are the possibilities:

Case $[E_{NA}]; X, po; [\mathcal{W}_{RLX}]$:

$\Rightarrow \ [E]; X_a, po; [\mathcal{F}_{0)]; X_a, po; [E]$  

$\Rightarrow \ [E]; X'_a, po; [E]$  

$\Rightarrow \ [E]; X'_a, bob; [E]$  

Case $[R_{RLX}]; X, po; [E_{NA}]$:

$\Rightarrow \ [Ld]; (X_a, rmw; X_a, F \cup X_a, po; [F, Ld]); X_a, po; [E]$  

$\Rightarrow \ [E]; X'_a, bob; [E]$  

Hence $X'_a, bob = X_a.bob$ and the transmation is sound for x86 to ARMv8 mapping.

As a result, the mapping scheme in Fig. 9b is sound.

\[ \square \]
A.3 ARMv8 to x86 Mappings

We restate Lemma [1]

Lemma 1. Suppose \( X \) is an x86 consistent execution. In that case \( X.\text{po}|_{\text{loc}}; X.fr \implies X.fr \cup X.co \).

Proof. We consider two cases in \( X \):

Case \([X.Ld]; X.\text{po}|_{\text{loc}}; X.fr; [X.W]\):
Let \((r, e) \in [X.Ld]; X.\text{po}|_{\text{loc}}; [X.R], (e, w') \in [X.R]; X.fr; [X.W]\) holds.
Also consider \( X.rf(w_e, e) \) and \( X.rf(w, r) \) holds.
We show by contradiction that \( X.co(w, w') \) and in consequence \( X.fr(r, w') \) holds.
Assume \( X.co(w_e, w) \) holds. Therefore \( X.fr(e, w) \) holds. However, from definition, \( X.xhb(w, e) \) holds. It is not possible in a x86 consistent execution as it violates irreflexive(\( X.fr; X.xhb \)) condition. Hence a contradiction and \( X.co(w, w_e) \) holds.
We also know that \( X.co(w_e, w') \) holds as from definition \( X.rf(w_e, e) \land X.fr(e, w') \).
As a result \( X.co(w, w') \) holds.
Therefore \( X.fr(r, w') \) holds.
Thus \([X.Ld]; X.\text{po}|_{\text{loc}}; X.fr; [X.W] \implies X.fr \).

Case \([X.W]; X.\text{po}|_{\text{loc}}; X.fr; [X.W]\):
Let \((w, w') \in [X.W]; X.\text{po}|_{\text{loc}}; X.fr; [X.W]\) and
\((w, r) \in [X.W]; X.\text{po}|_{\text{loc}}; [X.R] \land (r, w') \in [X.R]; X.fr; [X.W]\) holds.
Two subcases:

Subcase \( X.rf(w, r) \): 
In this case \( X.co(w, w') \) holds by definition.

Subcase \( X.rf(w_r, r) \): 
In this case \( w \neq w_r \).
We show \( X.co(w, w_r) \) holds by contradiction.
Assume \( X.co(w_r, w) \) holds. In that case \( X.fr(r, w) \) holds. This violates irreflexive(\( X.fr; X.xhb \)) constraint and hence a contradiction.
Therefore, \( X.co(w, w_r) \) holds and in consequence \( co(w, w') \) holds.
Thus \([X.W]; X.\text{po}|_{\text{loc}}; X.fr; [X.W] \implies X.co \).

We restate Lemma [2]

Lemma 2. Suppose \( X = \langle E, \text{po}, rf, mc \rangle \) is an x86 consistent execution. For each \( (X.\text{po}|_{\text{loc}} \cup X.fr \cup X.co \cup X.rf)^+ \) path between two events there exists an alternative \( (X.xhb \cup X.fr \cup X.co)^+ \) path between these two events which has no intermediate load event.

Proof. Consider a load event \( r \) on \( (X.\text{po}|_{\text{loc}} \cup X.fr \cup X.co \cup X.rf)^+ \) path. Considering the path, the possible incoming edges to \( r \) are \( X.rf, X.\text{po}|_{\text{loc}} \), and the outgoing edges are \( X.fr, X.\text{po}|_{\text{loc}} \).
Let \( a \) and \( b \) be the source and destination of the incoming and outgoing edges on the path.
Possible cases:
On Architecture to Architecture Mapping for Concurrency

Case $X.\text{rf}(a, r) \land X.\text{fr}(r, b)$:
From definition $X.\text{co}(a, b)$ holds.

Case $X.\text{rf}(a, r) \land X.\text{po}_{\text{loc}}(r, b)$:
From definition, $X.\text{xhb}(a, b)$.

Case $X.\text{po}_{\text{loc}}(a, r) \land X.\text{fr}(r, b)$:
From Lemma 3, $X.\text{fr}(a, b) \lor X.\text{co}(a, b)$ holds.

Case $X.\text{po}_{\text{loc}}(a, r) \land X.\text{po}_{\text{loc}}(r, b)$:
From definition, $X.\text{xhb}(a, b)$ holds.

We restate Lemma 3.

Lemma 3. Suppose $X = \langle E, \text{po}, \text{rf}, \text{mo} \rangle$ is an x86 consistent execution. For each obx path between two events there exists an alternative obx path which has no intermediate load event.

Proof. Consider a load event $r$ on $X$.obx path. Considering the path, the possible incoming edges to $r$ are $X.\text{rf}$, $X.\text{xppo}$, and the outgoing edges are $X.\text{fr}$, $X.\text{xppo}$.

Let $a$ and $b$ be the source and destination of the incoming and outgoing edges on the path.

Possible cases:

Case $X.\text{rf}(a, r) \land X.\text{fr}(r, b)$:
From definition $X.\text{mo}(a, b)$ holds.

Case $X.\text{rf}(a, r) \land X.\text{xppo}(r, b)$:
From definition $X.\text{xhb}(a, b)$ holds as $\text{xppo} \subseteq \text{po}$.

Case $X.\text{po}(a, r) \land X.\text{po}(r, b)$:
From definition $X.\text{hb}(a, b)$ holds as $\text{xppo} \subseteq \text{po}$.

Case $X.\text{xppo}(a, r) \land X.\text{fr}(r, b)$:
Considering the subcases of $a$:

Subcase $a \in (W \cup F)$:
We show $X.\text{mo}(a, b)$ holds.

In this case following the definition of $\text{xppo}$ we know $(a, r) \in [\text{St}]; \text{po}; [F]; \text{po}; [Ld]$. Let $c \in F$ such that $X.\text{po}(a, c) \land X.\text{po}(c, r)$ holds.

We show $X.\text{mo}(c, b)$ holds by contradiction.
Assume $X.\text{mo}(b, c)$ holds.

In this case $X.\text{fr}(r, b) \land X.\text{mo}(b, c) \land c \in F \land X.\text{po}(c, r)$ creates a cycle. Hence a contradiction as $X$ is x86 consistent. Therefore $X.\text{mo}(c, b)$ holds.

We also know that $X.\text{mo}(a, c)$ holds as $X.\text{mo}(c, a)$ would lead to a $X.\text{mo}; X.\text{xhb}$ cycle which is a contradiction. As a result, $X.\text{mo}(a, c) \land X.\text{mo}(c, b)$ implies that $X.\text{mo}(a, b)$ holds.
The scenarios are as follows:

**Subcase** \( a \in \text{Ld} \):

Let \( X, rf(w, a) \). We consider two scenarios based on whether there is an intermediate fence:

**Subsubcase** \((a, r) \in [\text{Ld}]\mid X, po; [F]; X, po; [\text{Ld}]\):

Let \( c \in F \) be the intermediate fence event.

It implies \((a, c) \in X, xppo\) following \( s_6 \) and \( X, mo(c, b) \) holds. (see earlier subcase)

Thus there is a \( X, obx \) path from \( a \) to \( b \) without passing through \( r \).

**Subsubcase** Otherwise:

In this case \((a, r) \in [\text{Ld}]\mid X, po; [\text{Ld}] \wedge \exists e. X, po(a, e) \wedge X, po(e, r)\).

Let \( c \) be the event such that \((c, r) \in X, po \cap X, obx \) and there is no such \( c' \) in between \( c \) and \( r \).

The scenarios are as follows:

1. \( c \in U \cup F \).
   
   In this case \( X, mo(c, b) \) holds as otherwise \( X, mo(b, c) \) creates a \( X, fr; X, mo; [U \cup F]; X, po \) cycle which results in a contradiction.

   Thus \( X, obx \) path between the same events does not pass through \( r \).

2. \( c \in \text{St} \).

   Following the definition of \( xppo \), there is an intermediate fence event \( d \in F \) such that \( X, po(c, d) \wedge X, po(d, r) \) holds. In this case \( X, mo(d, b) \) holds and also \( X, mo(c, d) \) holds. Hence \( X, mo(c, b) \) also holds.

   Thus \( X, obx \) path between the same events does not pass through \( r \).

3. \( c \in \text{Ld} \).

   Let \( w \in \forall \) be the event on the \( X, obx \) path and \( X, rfe(w, c) \) holds.

   In this case we show by contradiction that \( X, mo(w, b) \) holds.

   Assume \( X, mo(b, w) \) holds.

   In that case \( X, fr(r, b) \wedge X, mo(b, w) \wedge X, rfe(w, c) \wedge X, po(c, r) \) creates a cycle which violates x86 consistency for \( X \). Hence a contradiction and \( X, mo(w, b) \) holds.

   Thus \( X, obx \) path between the same events does not pass through \( r \).

We restate the theorem.

**Theorem 3.** The mapping scheme in Fig. 12b is correct.

To prove Theorem 3, we prove the following formal statement.

\[
\mathcal{P}_{\text{ARMv6}} \models \mathcal{P}_{\text{x86}} \implies \forall X_i \in [\mathcal{P}_{\text{x86}}]. \exists X_s \in [\mathcal{P}_{\text{ARMv6}}]. \text{Behavior}(X_i) = \text{Behavior}(X_s)
\]

**Proof.** Given an x86 execution \( X_i \) we define the corresponding ARM execution \( X_s \).

We know that \( X_i \) is x86 consistent. Now we show that \( X_s \) is ARM consistent. We prove by contradiction.

(internal)

Assume \( X_s \) contains \( X_s, po|_{loc} \cup X_s, ca \cup X_s, rf \) cycle.

It implies a \( X_s, po|_{loc} \cup X_s, ca \cup X_s, rf \) cycle following the mappings.

In that case we can derive a \((X_s, xhb \cup X_s, fr \cup X_s, co)^+\) cycle with no load event in \( X_i \) following Lemma 3.
Thus the cycle contains only same-location write events.

In that case \( X_t, fr \implies X_t, co \) and \( (X_t, W) \cup (X_t, xhb) \cup [X_t, W]) \implies X_t, co \) which implies a \( X_t, mo \) cycle as \( X_t, co \subseteq X_t, mo \). However, we know \( X_t, mo \) is has no cycle and hence a contradiction.

Therefore the source execution \( X_s \) in ARMv8 satisfies (internal).

(external)

We prove this by contradiction. Assume \( X_s \) contains a \( ob \) cycle. In that case \( X_t \) contains a \( obx \) cycle. In that case, from Lemma 3, we know that there exists a \( X_t, obx \) cycle which has no load event. Therefore the cycle contains only \( W \cup F \) events and thus there is a \( X_t, mo \) cycle. However, \( X_t \) is \( x86 \) consistent and hence there is no \( X_t, mo \) cycle. Thus a contradiction and \( X_s \) has no \( ob \) cycle. Therefore the source execution \( X_s \) in ARMv8 satisfies (external).

(atomic)

We prove this by contradiction. Assume \( [X_s, rmw] \cap X.t, fre \cap X.s, coe \neq \emptyset \).

In that case there exists \( u \in X_t, u \in X_t, W \) in \( x86 \) consistent execution \( X_t \) such that \( X_t, fre(u, w), X_t, coe(w, u) \) hold.

It implies there is a \( X_t, fr \cap X_t, mo \) cycle as \( fre \subseteq fr \) and \( coe \subseteq mo \) hold.

However, \( X_t, fr \cap X_t, mo \) cycle is not possible as \( X_t \) is consistent. Hence a contradiction and therefore \( [X_s, rmw] \cap X.t, fre \cap X.s, coe = \emptyset \).

Thus \( X_s \) is ARMv8 consistent as it satisfies (internal), (external), and (atomic) constraints.

\( \square \)

### A.4 ARMv7-mca to ARMv8 Mappings

In Appendix A.5, we have already shown all the relevant consistency constraints. It remains to show that \( mca \) holds for ARMv7-mca to ARMv8 mappings.

We restate Lemma 7 and then prove the same.

**Lemma 7.** Suppose \( X_t \) is an ARMv8 consistent execution and \( X_s \) is corresponding ARMv7 consistent execution. In that case \( [X_s, Ld]; X_s, ppo; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \implies [X_t, Ld]; X_t, ob; [X_t, St] \)

**Proof.** We start with

\[ [X_s, Ld]; X_s, ppo; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \]

Considering the final incoming edge to \([X_s, Ld]\), we consider following cases:

**Case** \([X_s, Ld]; X_s, ppo^2; [X_s, E]; X_s, addr; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \)

It implies \([X_s, Ld]; X_s, ppo^2; [X_s, E]; X_s, addr; X_s, po|_{loc}; [X_s, St] \)

\[ \implies [X_t, Ld]; X_t, ob^2; [X_t, E]; X_t, dob; [X_t, St] \text{ from Lemma 4} \]

\[ \implies [X_t, Ld]; X_t, ob; [X_t, St] \]

**Case** \([X_s, Ld]; X_s, ppo^2; [X_s, E]; X_s, rdw; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \)

It implies \([X_s, Ld]; X_s, ppo^2; [X_s, E]; X_s, coe; X_s, rfe; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \)

\[ \implies [X_s, Ld]; X_s, ppo^2; [X_s, E]; X_s, coe; X_s, coe; [X_s, St] \]

\[ \implies [X_t, Ld]; X_t, ob^2; [X_t, E]; X_t, obs; X_t, obs; [X_t, St] \text{ from Lemma 4} \]

\[ \implies [X_t, Ld]; X_t, ob; [X_t, St] \]

**Case** \([X_s, Ld]; X_s, ppo; [X_s, St]; X_s, rfi; [X_s, Ld]; X_s, po|_{loc}; [X_s, St] \);
It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; (X_s.ctrl \cup X_s.data \cup X_s.addr); [X_s.St]; X_s.co; [X_s.St] \) as \(X_s\) satisfies (sc-per-loc).

\[ \implies [X_s.Ld]; X_s.ppo; [X_s.Ld]; (X_s.ctrl \cup X_s.data); [X_s.St]; X_s.co; [X_s.St] \]

\[ \cup [X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.addr; X_s.po; [X_s.St] \]

\[ \implies [X_s.Ld]; X_t.ob; [X_t.Ld]; X_t.dob; [X_t.St] \]

\[ \implies [X_t.Ld]; X_t.ob; [X_t.St] \]

**Case** \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl_{SSB}; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \): It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.St] \) as \(ctrl_{SSB}; po \subseteq ctrl\) and \(ctrl_{SSB} \subseteq ctrl\).

\[ \implies [X_s.Ld]; X_t.ob; [X_t.Ld]; X_t.dob; [X_t.St] \]

\[ \implies [X_t.Ld]; X_t.ob; [X_t.St] \]

**Case** \([X_s.Ld]; X_s.ppo; [X_s.St]; X_s.detour; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \): It implies \([X_s.Ld]; X_s.ppo; [X_s.St]; X_s.co; [X_s.St]; X_s.re; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \) from the definition of detour.

\[ \implies [X_s.Ld]; X_s.ppo; [X_s.St]; X_s.co; [X_s.St]; X_s.co; [X_s.St] \]

\[ \implies [X_s.Ld]; X_t.ob; [X_t.St]; X_t.obs; [X_t.St]; X_t.obs; [X_t.St] \]

\[ \implies [X_t.Ld]; X_t.ob; [X_t.St] \]

**Case** \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \): It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.St] \) as \(po \subseteq ctrl\).

\[ \implies [X_s.Ld]; X_t.ob; [X_t.Ld]; X_t.dob; [X_t.St] \]

\[ \implies [X_t.Ld]; X_t.ob; [X_t.St] \]

**Case** \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.addr; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \): It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.addr; X_s.po_{loc}; [X_s.St] \)

\[ \implies [X_t.Ld]; X_t.ob; [X_t.Ld]; X_t.dob; [X_t.St] \]

\[ \implies [X_t.Ld]; X_t.ob; [X_t.St] \]

Now we show that \(X_s\) satisfies (mca). We restate \(\text{Lemma} 8\) and then prove the same.

**Lemma 8.** Suppose \(X_t\) is a target ARMv8 consistent execution and \(X_s\) is corresponding ARMv7 consistent execution. In this case \(X_{s.wo}\) is acyclic.

**Proof.** Following the definition of \(X_{s.wo}\):

\[ X_{s.wo} \triangleq ((X_s.re; X_s.ppo; X_s.re^{-1}) \setminus [X_s.E]) \setminus X_s.co \]

It implies

\[ X_s.re; X_s.ppo; [X_s.Ld]; X_s.fri; [X_s.St] \cup X_s.re; X_s.ppo; [X_s.Ld]; X_s.re; [X_s.St] \]

\[ \implies X_s.re; [X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \cup X_s.re; X_s.ppo; X_s.re \text{ from definitions.} \]

\[ \implies X_t.dob; [X_t.Ld]; X_t.ob; [X_t.St] \cup X_t.fri; [X_t.Ld]; X_t.ob; [X_t.St] \text{ from Lemma 7.} \]

\[ \implies X_t.obs; [X_t.Ld]; X_t.ob; [X_t.St] \cup X_t.obs; [X_t.St] \text{ from Lemma 9.} \]
⇒ \( X_t\.ob \).
Thus \( X_s\.wo^+ \implies X_t\.ob \cup X_t\.ob \implies X_t\.ob \).
We know \( X_t\.ob \) is acyclic.
Therefore \( X_s\.wo^+ \) is acyclic.

We restate Theorem 7 and then prove the same.

**Theorem 7.** The mappings in Fig. 12a are correct for ARMv7-mca.

We formally show
\[
\mathcal{P}_{\text{ARMv7-mca}} \leadsto \mathcal{P}_{\text{ARMv8}} \implies \forall X_t \in [\mathcal{P}_{\text{ARMv8}}]. \exists X_s \in [\mathcal{P}_{\text{ARMv7-mca}}]. \text{Behavior}(X_t) = \text{Behavior}(X_s)
\]

**Proof.** Follows from Theorem 4 and Lemma 8. Moreover, \( X_s\.co \iff X_t\.co \) holds. Therefore \( \text{Behavior}(X_t) = \text{Behavior}(X_s) \) also holds.

A.5 ARMv7 to ARMv8 Mappings

We restate Theorem 4.

**Theorem 4.** The mappings in Fig. 12a are correct.

We prove the following formal statement.
\[
\mathcal{P}_{\text{ARMv7}} \leadsto \mathcal{P}_{\text{ARMv8}} \implies \forall X_t \in [\mathcal{P}_{\text{ARMv8}}]. \exists X_s \in [\mathcal{P}_{\text{ARMv7}}]. \text{Behavior}(X_t) = \text{Behavior}(X_s)
\]

Given an ARMv8 execution \( X_t \) we define the corresponding ARMv7 execution \( X_s \) such that \( X_t\.po \iff X_s\.po \), \( X_t\.rf \iff X_s\.rf \), and \( X_t\.co \iff X_s\.co \) hold.

We know that \( X_t \) is ARMv8 consistent. We will show that \( X_s \) is ARMv7 consistent.

First we relate the \( X_s \) and \( X_t \) relations.

**Lemma 9.** Suppose \( X_s \) is an ARMv7 consistent execution and \( X_t \) is corresponding ARMv8 execution. In that case \( X_s\.fre \implies X_t\.obs \) and \( X_s\.rf \implies X_t\.ob \).

**Proof.** Follows from definition.

**Lemma 10.** Suppose \( X_s \) is an ARMv7 consistent execution and \( X_t \) is corresponding ARMv8 execution. In that case \( X_s\.fence \implies X_t\.bob \).

**Proof.** \( X_s\.fence \implies X_t\.po \cup \{X_s\.F\}; X_t\.po \implies X_t\.bob \).

**Lemma 11.** \((i_i_0 \cup c_i_0 \cup c_c_0); [St]; rfi \implies ob\)

**Proof.** We know \( rfi \subseteq i_i_0 \) and \( ppo \) does not have \( c_c_0 \); \( i_i_0 \) subsequence following the constraint. Therefore we show \((i_i_0 \cup c_i_0); [St]; rfi \implies ob\). It implies \( (addr \cup data \cup ctrl_{ibb}); [St]; rfi \implies (addr \cup data); rfi \cup ctrl; [St] \implies dob \cup dob \implies ob\).

Let \( dobc_0 = data \cup ctrl; [St] \cup addr \cup addr; po; [St] \) and \( ndobcc_0 = ctrl; [Ld] \cup addr; po; [Ld] \). Therefore \( cc_0 = dobc_0 \cup ndobcc_0 \).

**Lemma 12.** \( cc_0^+ = dobc_0 \cup ndobcc_0 \)

**Proof.** From definition \( cc_0^+ = (dobcc_0 \cup ndobcc_0)^+ \)
Consider the following cases:

- \( dobc_0; dobc_0 \)
  \( \implies addr; addr \implies addr; po; [St] \cup addr; po; [Ld] \implies dobc_0 \cup ndobcc_0 \)
Therefore $cc_0^+ = dobcc \cup ndobcc$.

Now we restate Lemma 4 and then prove the same.

**Lemma 4.** Suppose $X_s$ is an ARMv7 consistent execution and $X_t$ is corresponding ARMv8 execution. In that case $X_s.ppo \implies X_t.\text{ob}$.

**Proof.** From the definition of $\text{ppo}$ and Lemma 12

$[Ld]; X_s.ppo \implies [Ld]; (X_s.\text{ctrl} \cup X_s.\text{ci0} \cup X_t.dobcc; ci_0^0 \cup X_s.ndobcc; X_t.ci_0) +$

$\implies [Ld]; (X_s.\text{ctrl} \cup X_s.\text{ci0} \cup X_t.dobcc; X_t.\text{ci0}) +$

$\implies [Ld]; (X_s.\text{addr} \cup X_s.\text{data} \cup X_s.\text{rdw} \cup X_s.\text{ob} \cup X_s.\text{ctrllsb} \cup X_s.\text{detour} \cup X_s.\text{dobcc}; ci_0^0 \cup X_s.ndobcc; ci_0) +$ by reducing the $rfr$ edges following Lemma 11

$\implies [Ld]; (X_s.\text{ob} \cup X_s.\text{ndobcc}; ci_0) +$ as

- $X_s.\text{addr} \cup X_s.\text{data} \cup X_s.\text{ctrllsb} \subseteq X_s.\text{ob}$
- $X_s.\text{rdw} = X_s.\text{fre} \cup X_s.\text{rfe} \subseteq X_s.\text{ob}$
- $X_s.\text{detour} = X_s.\text{coe} \cup X_s.\text{rfe} \subseteq X_s.\text{ob}$
- $X_s.\text{dobcc} = (X_s.\text{data} \cup X_s.\text{ctl}) \cup X_s.\text{addr} \cup X_s.\text{rdw}; X_s.\text{po}; [St]) \subseteq X_s.\text{ob}$

Now, $X_s.\text{ndobcc}; X_s.\text{ci0} = (X_s.\text{ctrl}; [Ld] \cup X_s.\text{addr}; X_s.\text{po}; [Ld]); (X_s.\text{ctrl} \cup X_s.\text{detour})$ from definition.

$\implies (X_s.\text{ctrl}; [Ld]; X_s.\text{ctrllsb} \cup X_s.\text{addr}; X_s.\text{po}; [Ld]); X_s.\text{ctrllsb})$ as dom$(X_s.\text{detour}) \not\subseteq Ld.$

$\implies (X_s.\text{dob} \cup X_s.\text{dob})$ as dom$(X_s.\text{detour}) \not\subseteq Ld \implies X_s.\text{ob}$

$\implies [Ld]; (X_s.\text{ob} \cup X_s.\text{ndobcc}; X_s.\text{ci0}) + \implies X_s.\text{ob}$.

Therefore $X_t.\text{ppo} \implies X_t.\text{ob}$.

**Lemma 13.** Suppose $X_s$ is an ARMv7 consistent execution and $X_t$ is corresponding ARMv8 execution. In that case (i) $X_s.\text{ahb} \implies X_t.\text{ob}$ and (ii) $X_s.\text{prop} \implies X_t.\text{ob}$.

**Proof.** (i) $X_s.\text{ahb} \implies X_s.\text{ppo} \cup X_s.\text{fence} \cup X_s.\text{rfe} \implies X_t.\text{ob} \cup X_t.\text{bob} \cup X_t.\text{obs}$ from Lemma 9, Lemma 10 and Lemma 4.

(ii) We know $X_s.\text{prop} = X_s.\text{prop}_1 \cup X_s.\text{prop}_2$ from definition.

Now,

$X_s.\text{prop}_1$

$\implies [X_t.\text{W}]; X_t.\text{rfe}; X_t.\text{fence}; X_t.\text{ahb}^*; [X_t.\text{W}]$

$\implies X_t.\text{obs}; X_t.\text{bob}; (X_t.\text{dob} \cup X_t.\text{bob} \cup X_t.\text{obs}) ; [X_t.\text{W}]$

$\implies X_t.\text{ob}$

Also $X_s.\text{prop}_2$

$\implies ((X_t.\text{coi} \cup X_t.\text{fr}) \setminus X_t.\text{po})^?; X_t.\text{rfe}; (X_t.\text{fence}; X_t.\text{ahb}^* )^?; X_t.\text{fence} ; X_t.\text{ahb}^*$

$\implies (X_t.\text{coi} \cup X_t.\text{coi} \cup X_t.\text{fr} \cup X_t.\text{fre}) \setminus X_t.\text{po})^?; X_t.\text{rfe}; (X_t.\text{fence}; X_t.\text{ahb}^* )^?; X_t.\text{fence} ; X_t.\text{ahb}^*$
Hence $X$. We know

Moreover, Hence $X$

It implies there is a $X$. In this case each of $X$. Thus a $X$. We know

Assume there is a $X$. (propagation)

It implies a $X$. We show $X$. (total-mo), (sc-per-loc), (atomicity) hold on $X$. Therefore, $X$. However, we know that $X$. Considering the relations above,

We show

Now we prove Theorem 3.

Proof. We show $X$ is ARMv7 consistent by contradiction.

$(\text{total-mo}), (\text{sc-per-loc}), (\text{atomicity})$ hold on $X$ as they hold on $X_t$. It remains to show that $(\text{observation})$ and $(\text{propagation})$ hold on $X$.

(observation)
Assume there is a $X, \text{fre}; X, \text{prop}; X, \text{ahb}^*$ cycle.
Considering the relations above,

$X, \text{fre}; X, \text{prop}; X, \text{ahb}^* \implies X, \text{obs}; X, \text{ob}; (X, \text{dob} \cup X, \text{bob} \cup X, \text{obs})^* \implies X, \text{ob}$.

However, we know that $X, \text{ob}$ is irreflexive and hence a contradiction.
Therefore, $X, \text{fre}; X, \text{prop}; X, \text{ahb}^*$ is irreflexive and $X$ satisfies (observation).

(propagation)
Assume there is a $X, \text{co} \cup X, \text{prop}$ cycle.

It implies a $X, \text{co} \cup X, \text{ob}$ cycle.
We know $X, \text{co}; X, \text{co} \implies X, \text{co}$ and $X, \text{prop}; X, \text{prop} \implies X, \text{prop}$.
Thus a $X, \text{co} \cup X, \text{ob}$ cycle can be reduced to a $X, \text{co} \cup X, \text{ob}$ cycle where $X, \text{co}$ and $X, \text{prop}$ take place alternatively.
In this case each of $X, \text{prop} \subseteq (X, \mathcal{W} \times X, \mathcal{W})|_{\text{loc}} \subseteq X, \text{co}$.
It implies there is a $X, \text{co}$ cycle which is a contradiction.
Hence $X, \text{co} \cup X, \text{prop}$ is acyclic and $X$ satisfies (propagation).
Therefore $X$ is ARMv7 consistent.
Moreover, Behavior($X_t$) = Behavior($X$) holds as $X, \text{co} \iff X, \text{co}$.

A.6 ARMv8 to ARMv7 Mappings

We restate Lemma 5 and then prove the same.

Lemma 5. Suppose $X_t$ is an ARMv7 consistent execution and $X_s$ is ARMv8 execution following the mappings in Fig. 13a. In this case $X_s, \text{ob} \implies (X_t, \text{fre} \cup X_t, \text{coe} \cup X_t, \text{fre} \cup X_t, \text{rmw} \cup X_t, \text{fence})^*$.

Proof. (1) $X_s, \text{obs} \implies X_s, \text{fre} \cup X_s, \text{coe} \cup X_s, \text{fre}$

$\implies X_t, \text{fre} \cup X_t, \text{coe} \cup X_t, \text{fre}$ from definition.

(2) We know $X_s, \text{dob} \subseteq [X_s, \text{Ld}] \cup X_s, \text{po} \cup [X_s, \text{E}]$.

$\implies [X_t, \text{Ld}] \cup X_t, \text{po} \cup [X_t, \text{F}] \cup X_t, \text{po} \cup [X_s, \text{E}]$ following the mappings in Fig. 13a.
\[ \Rightarrow [X_t.Ld] ; X_t.fence ; [X_t.E] \text{ from the definition.} \]

(3)
We know \( aob \triangleq \text{rmw} \cup [\text{range} \{ \text{rmw} \}] ; \text{rfi} ; [A] \)
Hence \( X_s.\text{rmw} \cup [\text{range} \{X_s.\text{rmw}\}] ; X_s.\text{rfi} ; [X_s.A \cup X_s.Q] \)
\[ \Rightarrow X_t.\text{rmw} \cup [\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{rfi} ; [X_t.Ld] ; X_t.\text{po} ; [X_t.F] \]

(4)
Following the definition of \( X_s.\text{bob} \), we consider its components:

- \( X_s.\text{po} ; [X_s.F] ; X_s.\text{po} \)
  \[ \Rightarrow X_t.\text{po} ; [X_t.F] ; X_t.\text{po} \]
  \[ \Rightarrow X_t.fence \]
- \( [X_s.\text{STLR}] ; X_s.\text{po} ; [X_s.\text{LDAR}] \)
  \[ \Rightarrow [X_t.F] ; X_t.\text{po} ; [X_t.\text{St}] ; X_t.\text{po} ; [X_t.F] ; X_t.\text{po} ; [X_t.Ld] \]
  \[ \Rightarrow X_t.fence \]
- \( [X_s.\text{Ldar}] ; X_s.\text{po} \)
  \[ \Rightarrow [X_t.Ld] ; X_t.\text{po} ; [X_t.F] ; X_t.\text{po} \]
  \[ \Rightarrow X_t.fence \]
- \( [X_s.\text{St}] ; X_s.\text{po} ; [X_s.\text{St}] ; X_s.\text{po} ; [X_s.\text{St}] \)
  \[ \Rightarrow [X_t.\text{St}] ; X_t.\text{po} ; [X_t.F] ; X_t.\text{po} ; [X_t.\text{St}] \]
  \[ \Rightarrow X_t.fence \]
- \( X_s.\text{po} ; [X_s.\text{STLR}] \)
  \[ \Rightarrow X_t.\text{po} ; [X_t.F] ; X_t.\text{po} ; [X_t.\text{St}] \]
  \[ \Rightarrow X_t.fence \]
- \( X_s.\text{po} ; [X_s.\text{STLR}] ; X_s.\text{coi} \)
  \[ \Rightarrow X_t.\text{po} ; [X_t.F] ; X_t.\text{po} ; [X_t.\text{St}] ; X_t.\text{po} \]
  \[ \Rightarrow X_t.fence \]

Thus \( X_s.\text{bob} \Rightarrow X_t.fence \).
Therefore \( X_s.\text{ob} \Rightarrow \)
\[ (X_t.\text{rfe} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.fence \cup X_t.\text{rmw} \cup [\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{rfi} ; [X_t.Ld] ; X_t.\text{po} ; [X_t.F])^+ \]
Considering the outgoing edges from \( \text{Ld} \) event in \([\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{rfi} ; [X_t.Ld] ; X_t.\text{po} ; [X_t.F] \) we consider two cases:

- **case** \([\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{rfi} ; [X_t.Ld] ; X_t.\text{po} ; [X_t.F] ; X_t.\text{po} \)
  \[ \Rightarrow X_t.fence \]

- **case** \([\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{rfi} ; [X_t.Ld] ; X_t.\text{fre} \)
  \[ \Rightarrow [\text{range} \{X_t.\text{rmw}\}] ; X_t.\text{coe} \text{ by definition of } \text{fre}. \]

Therefore \( X_s.\text{ob} \Rightarrow (X_t.\text{rfe} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.fence \cup X_t.\text{rmw})^+ \).
We restate the Lemma 6 and then prove the same.

**Lemma 6.** Suppose $X_t$ is an ARMv7 consistent execution and $X_s$ is ARMv8 execution following the mappings in Fig. [13a]. In this case either $X_s.\text{ob} \implies (X_t.E \times X_t.E)|_{\text{loc}} \setminus [E]$ or $X_s.\text{ob} \implies (X_t.co; X_t.prop \cup X_t.prop)^+$.

**Proof.** We know $X_s.\text{ob} \implies (X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw \cup X_t.fence)^+$ from Lemma 5.

**Scenario (1):** $(X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw \cup X_t.fence)^+$ has no $X_t.fence$.

In this case $(X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw)^+ \implies (X_t.E \times X_t.E)|_{\text{loc}} \setminus [E]$ from the definitions.

**Scenario (2):** Otherwise

In this case $X_s.\text{ob} \implies ((X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw)^+; X_t.fence)^+$

Now we consider following cases:

- **Case (RR):**
  
  $[X_t.Ld]; (X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw)^+; [X_t.Ld]; X_t.fence$
  
  $\implies [X_t.Ld]; (X_t.rfe \cup X_t.coe \cup X_t.fre \cup X_t.rmw)^+; [X_t.Ld]; X_t.rfe; [X_t.Ld]; X_t.fence$
  
  $\implies [X_t.Ld]; X_t.fre; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence$ as $X_t$ satisfies (sc-per-loc).
  
  $\implies [X_t.Ld]; X_t.fri; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence \cup [X_t.Ld]; X_t.fre; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence$
  
  $\implies [X_t.Ld]; (X_t.rmw \cup X_t.fence); [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence \cup X_t.prop_2$

  following the mapping of Fig. [13a] and definition of $prop_2$.

  $\implies [X_t.Ld]; X_t.rmw; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence$

  $\cup [X_t.Ld]; X_t.fence; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence \cup X_t.prop_2$

  $\implies [X_t.Ld]; X_t.ppo; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence$

  $\cup [X_t.Ld]; X_t.fence; [X_t.St]; X_t.rfe; [X_t.Ld]; X_t.fence \cup X_t.prop_2$

  as $X_t.rmw \implies X_t.ppo$.

  $\implies [X_t.Ld]; X_t.ahb; X_t.fence$

  $\cup [X_t.Ld]; X_t.fence; [X_t.St]; X_t.ahb; [X_t.Ld]; X_t.fence \cup X_t.prop_2$

  from definition of $prop_2$.

  $\implies X_t.prop_2 \cup prop_2 \cup prop_2$

  $\implies X_t.prop$

**Case (RW):**
Thus (in Case (WW))

\[ X_s.\text{ld}; (X_t.\text{fre} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.\text{rmw})^+; [X_t.\text{st}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{ld}]; X_t.\text{fr}; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{ld}]; X_t.\text{fr}; X_t.\text{fence} \cup [X_t.\text{ld}]; X_t.\text{fre}; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{ld}]; X_t.\text{fence} \cup [X_t.\text{ld}]; X_t.\text{fre}; X_t.\text{fence} \]

\[ \Rightarrow X_t.\text{prop}_2 \cup X_t.\text{prop}_2 \text{ from definition of prop}_2. \]

\[ \Rightarrow X_t.\text{prop} \]

Case (WR):

\[ [X_t.\text{st}]; (X_t.\text{fre} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.\text{rmw})^+; [X_t.\text{ld}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{st}]; (X_t.\text{fre} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.\text{rmw})^*; [X_t.\text{st}]; X_t.\text{fre}; [X_t.\text{ld}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fre}; [X_t.\text{st}]; X_t.\text{fence} \text{ as } X_t \text{ satisfies (sc-per-loc).} \]

\[ \Rightarrow X_t.\text{co}; X_t.\text{prop}_1 \text{ from definition.} \]

\[ \Rightarrow X_t.\text{co}; X_t.\text{prop} \text{ as prop}_1 \subseteq \text{prop} \]

\[ \Rightarrow [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fre}; [X_t.\text{ld}]; X_t.\text{fence} \cup [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fre}; [X_t.\text{ld}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fre}; [X_t.\text{st}]; X_t.\text{fence} \cup X_t.\text{prop}_2 \text{ from definitions} \]

Case (WW):

\[ [X_t.\text{st}]; (X_t.\text{fre} \cup X_t.\text{coe} \cup X_t.\text{fre} \cup X_t.\text{rmw}); [X_t.\text{st}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fence} \]

\[ \Rightarrow [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fence} \cup [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fence} \]

\[ \Rightarrow X_t.\text{fence} \cup [X_t.\text{st}]; X_t.\text{co}; [X_t.\text{st}]; X_t.\text{fence} \]

\[ \Rightarrow X_t.\text{prop}_2 \cup X_t.\text{prop}_2 \text{ from definition of prop}_2. \]

\[ \Rightarrow X_t.\text{prop} \]

Thus (in Scenario-II) \( X_s.\text{ob} \implies (X_t.\text{co}; X_t.\text{prop} \cup X_t.\text{prop})^+ \).

Finally we restate Theorem 5 and then prove the same.

**Theorem 5.** The mappings in Fig. 13a are correct.

To prove Theorem 5 we prove the following formal statement.

\[ P_{ARMv8} \sim P_{ARMv7} \iff \forall X_t \in [P_{ARMv7}]. \exists X_s \in [P_{ARMv8}]. \text{Behavior}(X_t) = \text{Behavior}(X_s) \]

**Proof.** We know that \( X_t \) is ARMv7 consistent. Now we show that \( X_s \) is ARMv8 consistent. We prove by contradiction.

Case (internal): We know that (sc-per-loc) holds in \( X_t \). Hence (internal) trivially holds in \( X_s \).

Case (external): Assume there is a \( X_s.\text{ob} \) cycle.

From Lemma 6 we know that \( X_s.\text{ob} \implies ((X_t.\text{r}) \times X_t.\text{r})_{\text{loc}} \setminus [\mathcal{E}] \cup (X_t.\text{co}; X_t.\text{prop} \cup X_t.\text{prop})^+ \).

We know both \( ((X_t.\text{r}) \times X_t.\text{r})_{\text{loc}} \setminus [\mathcal{E}] \) is acyclic as \( X_t \) satisfies (sc-per-loc) and \( (X_t.\text{co}; X_t.\text{prop} \cup X_t.\text{prop})^+ \) is acyclic as \( X_t \) satisfies (propagation).

Case (atomic):
We know that (atomic) holds in $X_i$. Hence (atomic) trivially holds in $X_s$.

Therefore $X_s$ is consistent. Moreover, as $X_s.co \iff X_i.co$ holds, Behavior($X_s$) = Behavior($X_i$) also holds.

A.7 Proof of correctness: C11 to ARMv8 to ARMv7

We restate the theorem and then prove the correctness.

**Theorem 6.** The mapping scheme in Fig. 13b is correct.

**Proof.** The mapping can be represented as a combination of following transformation steps.

1. $F_{C11} \mapsto F_{ARMv8}$ mapping from Fig. A.5
2. $F_{ARMv8} \mapsto F_{ARMv7}$ mappings from Fig. A.5
3. Elimination of leading DMB fences for LDR$_{NA} \mapsto$ LDR mapping, that is, LDR$_{NA}$ $\mapsto$ LDR; DMB $\mapsto$ LDR.

We know (1), (2) are sound and therefore it suffices to show that transformation (3) is sound.

Let $X_s$ and $X'_s$ be the consistent execution of $F_{ARMv8}$ before and after the transformation (3). Let $X$ be corresponding C11 execution $F_{C11}$, and we know $F_{C11}$ is race-free. Therefore for all non-atomic event $a$ in $X$ if there exist another same-location event $b$ then $X_hb = (a, b)$ holds.

Now we consider ARMv8 to ARMv7 mapping scheme.

Considering the hb definition following are the possibilities:

Case $[E_{na}]; X.po; [F_{rel}]; X.po; [W_{rel}]$ \cup $[E_{na}]; X.po; [W_{rel}]$:

$\implies [E]; X_a.po; [F]; X_a.po; [St \cup rmw]$  
$\implies [E]; X'_a.po; [F]; X'_a.po; [E]$  
$\implies [E]; X'_a.fence; [E]$  

Case $[R_{rel}]; X.po; [E_{na}] \cup [R_{rel}]; X.po; [F_{acq}]; X.po; [E_{na}]$:

$\implies [Ld]; X_a.po; [F]; X_a.po$  
$\implies [E]; X'_a.fence; [E]$  

Therefore $X'_a.fence = X_a.fence$ and the transformation is sound for ARMv8 to ARMv7 mapping.

A.8 ARMv7-mca to ARMv8 Mappings

In Appendix A.5 we have already shown all the relevant consistency constraints. It remains to show that (mca) holds for ARMv7-mca to ARMv8 mappings.

We restate Lemma 7 and then prove the same.

**Lemma 7.** Suppose $X_i$ is an ARMv8 consistent execution and $X_s$ is corresponding ARMv7 consistent execution. In that case $[X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.po_{loc}; [X_s.St] \implies [X_i.Ld]; X_i.ob; [X_i.St]$

**Proof.** We start with $[X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.po_{loc}; [X_s.St]$

Considering the final incoming edge to $[X_s.Ld]$, we consider following cases:

Case $[X_s.Ld]; X_s.ppo; [X_s.E]; X_s.addr; [X_s.Ld]; X_s.po_{loc}; [X_s.St]$  

It implies $[X_s.Ld]; X_s.ppo; [X_s.E]; X_s.addr; [X_s.po]; [X_s.St]$
\[
\Rightarrow [X_s.Ld]; X_s.ppo; [X_s,E]; X_s.rdwr; [X_s.Ld]; X_s.po|loc; [X_s.St];
\]

Case \([X_s.Ld]; X_s.ppo; [X_s,E]; X_s.rdwr; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s,E]; X_s.co; X_s.rfe; [X_s.Ld]; X_s.po|loc; [X_s.St]\)

\[
\Rightarrow [X_s.Ld]; X_s.ppo; [X_s,E]; X_s.co; X_s.co; [X_s.St];
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.E]; X_s.obs; [X_s.St] \text{ from Lemma 4}
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.St]
\]

Case \([X_s.Ld]; X_s.ppo; [X_s,St]; X_s.rfi; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; (X_s.ctrl \cup X_s.data \cup X_s.addr); [X_s.St]; X_s.co; [X_s.St]\) as \(X_s\) satisfies (sc-per-loc).

\[
\Rightarrow [X_s.Ld]; X_s.ppo; [X_s.Ld]; (X_s.ctrl \cup X_s.data); [X_s.St]; X_s.co; [X_s.St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.addr; X_s.po; [X_s.St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.St] \text{ from Lemma 4}
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.St]
\]

Case \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl_{ISB}; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.St] \text{ as } ctrl_{ISB}: po \subseteq ctrl_{ISB} \subseteq ctrl\).

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.Ld]; X_s.ob; [X_s.St] \text{ from Lemma 4}
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s.St]
\]

Case \([X_s.Ld]; X_s.ppo; [X_s,St]; X_s.detour; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s,St]; X_s.co; X_s.rf; [X_s.Ld]; X_s.po|loc; [X_s.St]\) from the definition of detour.

\[
\Rightarrow [X_s.Ld]; X_s.ppo; [X_s,St]; X_s.co; [X_s.St]; X_s.co; [X_s.St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]; X_s.obs; [X_s,St]; X_s.obs; [X_s,St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]
\]

Case \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.ctrl; [X_s.St] \text{ as } ctrl: po \subseteq ctrl\).

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]
\]

Case \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.addr; X_s.po; [X_s.Ld]; X_s.po|loc; [X_s.St]\):

It implies \([X_s.Ld]; X_s.ppo; [X_s.Ld]; X_s.addr; X_s.po; [X_s.St]\)

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]
\]

\[
\Rightarrow [X_s.Ld]; X_s.ob; [X_s,St]
\]

Now we show that \(X_s\) satisfies (mca). We restate Lemma 8 and then prove the same.
**Lemma 8.** Suppose $X_t$ is a target ARMv8 consistent execution and $X_s$ is corresponding ARMv7 consistent execution. In this case $X_s . w o^+ $ is acyclic.

**Proof.** Following the definition of $X_s . w o$:

$$ X_s . w o \triangleq ((X_s . rfe; X_s . ppo; X_s . rfe^-1) \setminus [X_s . E]) ; X_s . c o $$

It implies

$$ X_s . rfe; X_s . ppo; [X_s . Ld]; X_s . fri; [X_s . St] \cup X_s . rfe; X_s . ppo; [X_s . Ld]; X_s . fre; [X_s . St] $$

$$ \implies X_s . rfe; [X_t . Ld]; X_s . ppo; [X_s . Ld]; X_s . ppo; [X_s . St] \cup X_s . rfe; X_s . ppo; X_s . fre $$

from definitions.

$$ \implies X_t . rfe; [X_t . Ld]; X_t . ob; [X_s . St] \cup X_t . rfe; X_t . ob; X_t . fre $$

from Lemma 7.

$$ \implies X_t . obs; [X_t . Ld]; X_t . ob; [X_s . St] \cup X_t . obs; X_t . ob; X_t . ob $$

from Lemma 9.

$$ \implies X_t . ob. $$

Thus $X_s . w o^+ \implies X_t . ob \cup X_t . ob \implies X_t . ob$.

We know $X_t . ob $ is acyclic.

Therefore $X_s . w o^+ $ is acyclic.

We restate Theorem 7 and then prove the same.

**Theorem 7.** The mappings in Fig. 12a are correct for ARMv7-mca.

We formally show

$$ \forall X_t \in [P_{ARMv8}]. \exists X_s \in [P_{ARMv7-mca}]. Behavior(X_t) = Behavior(X_s) $$

**Proof.** Follows from Theorem 4 and Lemma 8. Moreover, $X_s . c o \iff X_t . c o$ holds. Therefore $Behavior(X_t) = Behavior(X_s)$ also holds. 

\[\square\]
On Architecture to Architecture Mapping for Concurrency

B Proofs and counter-examples for Optimizations in ARMv8

B.1 Proofs of Safe reorderings

We prove the following theorem for safe reorderings in Fig. 14.

$$P_{src} \rightsquigarrow P_{tgt} \implies \forall X_t \in [P_{tgt}] \exists X_s \in [P_{src}] \text{. Behavior}(X_t) = \text{Behavior}(X_s)$$

Proof. We know $X_t$ is ARMv8 consistent. We define $X_s$ where $a \cdot b \rightsquigarrow b \cdot a$.

$X_s.E = X_t.E$

$X_s.po = (X_t.po \setminus \{(b, a)\} \cup \{(a, b)\})^+$

$X_s.rf = X_t.rf$

$X_s.co = X_t.co$

We show that $X_s$ is ARMv8 consistent.

(Internal)

We know that $X_t.po|_{loc} = X_s.po|_{loc}$, $X_s.rf = X_t.rf$, $X_s.fr = X_t.fr$, $X_s.co = X_t.co$ hold. We also know that $X_t$ satisfies (internal). Therefore $X_s$ also satisfies (internal).

(External)

We relate the ob relations between memory accesses in $X_t$ and $X_s$. Let $M = St \cup Ld \cup L \cup A$.

- $St(x)/L(x) \cdot Ld(y) \rightsquigarrow Ld(y) \cdot St(x)/L(x)$. In this case $X_s.aob = X_t.aob$, $X_s.bob \subseteq X_t.bob$, and $X_s.dob = X_t.dob$ hold.
- $Ld(x) \cdot Ld(y) \rightsquigarrow Ld(y) \cdot Ld(x)$. In this case $X_s.aob = X_t.aob$, $X_s.bob = X_t.bob$, and $X_s.dob = X_t.dob$ hold.
- $F_{ST} \cdot Ld(y) \rightsquigarrow Ld(y) \cdot F_{ST}$. In this case $X_s.aob = X_t.aob$, $X_s.bob = X_t.bob$, and $X_s.dob = X_t.dob$ hold.
- $St(x)/Ld(x)/F_{ST} \cdot A(y) \rightsquigarrow A(y) \cdot St(x)/Ld(x)/F_{ST}$. In this case $X_s.aob = X_t.aob$, $X_s.bob \subseteq X_t.bob$, and $X_s.dob = X_t.dob$ hold.
- $F_{LD}/F_{ST}/F \cdot L(y) \rightsquigarrow F_{LD}/F_{ST}/F \cdot L(y)$. In this case $X_s.aob = X_t.aob$, and $X_s.dob = X_t.dob$ hold. We also know that $[M]; X_s;bob; [X_s]; [L]; X_s;bob; [M] \subseteq [L]; X_t;bob; [M]$ hold.
- $A(x)F_{LD}/F_{ST}/F \cdot F \cdot A(x)F_{LD}/F_{ST}/F$. In this case $X_s.aob = X_t.aob$, $X_s.bob; [M] \subseteq X_t.bob; [M]$, and $X_s.dob = X_t.dob$ hold.
- $St/L/A/F \cdot F_{LD} \rightsquigarrow F_{LD} \cdot St/L/A/F$. In this case $X_s.aob = X_t.aob$, $[M]; X_s;bob; [M] \subseteq X_t.bob; [M]$, and $X_s.dob = X_t.dob$ hold.
- $F_{LD}/A/F \cdot F_{ST} \rightsquigarrow F_{ST} \cdot F_{LD}/A/F$. In this case $X_s.aob = X_t.aob$, $[M]; X_s;bob; [M] = [M]; X_t;bob; [M]$, and $X_s.dob = X_t.dob$ hold.

Hence $[M]; X_s;obi; [M] \subseteq [M]; X_t;obi; [M]$ holds.

We also know that $X_s.rf = X_t.rf$ and $X_s.co = X_t.co$ hold.

We also know that $irr(X_t.ob)$ holds.

Therefore $irr(X_t.ob)$ also holds.

We know that $X_t.rmw = X_s.rmw$, $X_s.rf = X_t.rf$, $X_s.fr = X_t.fr$, $X_s.co = X_t.co$ hold. We also know that $X_t$ satisfies (atomic). Therefore $X_s$ also satisfies (atomic).

We already know $X_s.co = X_t.co$ and therefore $\text{Behavior}(X_s) = \text{Behavior}(X_t)$.

\[\square\]
B.2 Safe eliminations

We prove the following theorem for (RAR), (RAA), and (AAA) safe eliminations in Fig. 14(a).

\[ \mathbb{P}_{\text{src}} \sim \mathbb{P}_{\text{tgt}} \implies \forall X_i \in [\mathbb{P}_{\text{tgt}}] \exists X_s \in [\mathbb{P}_{\text{src}}]. \text{Behavior}(X_i) = \text{Behavior}(X_s) \]

**Proof.** We know \( X_i \) is ARMv8 consistent. We define \( X_s \) where \( a \cdot b \sim a \) where

(RAR) \( a = \text{Ld}(X, v') \) and \( b = \text{Ld}(X, v) \) or

(RAA) \( a = \text{A}(X, v') \) and \( b = \text{Ld}(X, v) \) or

(AAA) \( a = \text{A}(X, v') \) and \( b = \text{A}(X, v) \).

\[
X_s, E = X_t, E \cup \{b\} \\
X_s, \text{po} = (X_t, \text{po} \cup \{(a, b)\})^+ \\
X_s, \text{rf} = X_t, \text{rf} \cup \{(w, b) \mid X_t, \text{rf}(w, a)\} \\
X_s, \text{co} = X_t, \text{co} \\
\]

Moreover, \([\{a\}; X_s, \text{po}_{\text{imm}}; \{\{b\}; X_s, \text{dob} = \{\{a\}; X_t, \text{dob.} \]

We show that \( X_s \) is ARMv8 consistent.

Assume \( X_s \) is not consistent.

(internal)

Asume a \( X_s, \text{po}_{\text{loc}} \cup X_s, \text{ca} \cup X_s, \text{rf} \) cycle.

It implies a \( X_t, \text{po}_{\text{loc}} \cup X_t, \text{ca} \cup X_t, \text{rf} \) cycle as \([\{b\}; X_s, \text{fr} \) implies \([\{a\}; X_s, \text{fr}, \) and \([\{a\}; X_t, \text{fr}. \)

Therefore a contradiction and \( X_s \) satisfies (internal).

(external)

We know \( \text{dom}(X_s, \text{dob}); \{\{b\} \implies \text{dom}(X_s, \text{dob}); \{\{a\} = \text{dom}(X_t, \text{dob}); \{\{a\} \) hold.

Moreover, \([\{b\}; X_s, \text{dob} = \{\{a\}; X_t, \text{dob.} \]

Also in case of (AAA), \( \text{codom}([\{b\}; X_s, \text{bob}) = \text{codom}([\{a\}; X_s, \text{bob}) \setminus \{b\} = \text{codom}([\{a\}; X_t, \text{bob) hold. \)

Hence \( X_s, \text{ob} \subseteq X_t, \text{ob.} \)

We know \( \text{irr}(X_t, \text{ob}) \) holds.

Therefore a contradiction and \( X_s \) satisfies (external).

(atomicity)

From definition \( X_s, \text{rmw} = X_t, \text{rmw}, X_s, \text{coe} = X_t, \text{coe}, \) and \( X_s, \text{fre} = X_t, \text{fre} \) hold.

Therefore \( X_s \) preserves atomicity as \( X_t \) preserves atomicity.

Moreover, \( \text{Behavior}(X_s) = \text{Behavior}(X_t) \) holds as \( X_s, \text{co} = X_t, \text{co} \) holds.

\[ \square \]

B.3 Access strengthening

We prove the following theorem for (R-A) from Fig. 14(a).

\[ \mathbb{P}_{\text{src}} \sim \mathbb{P}_{\text{tgt}} \implies \forall X_i \in [\mathbb{P}_{\text{tgt}}] \exists X_s \in [\mathbb{P}_{\text{src}}]. \text{Behavior}(X_i) = \text{Behavior}(X_s) \]

**Proof.** We know \( X_i \) is ARMv8 consistent. We define \( X_s \) where \( a \sim b \) where \( a = \text{Ld}(X, v) \) and \( b = \text{A}(X, v) \).

\[
X_s, E = X_t, E \cup \{a\} \setminus \{b\} 
\]
\( X_s.p = \{ (e, a) \mid X_t.p(e, b) \} \cup \{ (a, e) \mid X_t.p(b, e) \} \)

\( X_s.rf = \{ (w, a) \mid X_t.rf(w, b) \} \)

\( X_s.co = X_t.co \)

We show that \( X_s \) is ARMv8 consistent.

Assume \( X_s \) is not consistent.

(internal)

Assume a \( X_s.p_{\text{loc}} \cup X_s.ca \cup X_s.rf \) cycle.

It implies \( X_t.p_{\text{loc}} \cup X_t.ca \cup X_t.rf \) cycle which is a contradiction and hence \( X_s \) satisfies (internal).

(external)

We know \( \text{dom}(X_s.ob) = \text{dom}(X_t.ob) \) and \( \text{codom}(X_t.po) = \text{dom}(X_t.bob) \).

Hence \( X_s.ob \subseteq X_t.ob \).

We know \( \text{irr}(X_t.ob) \) holds.

Therefore a contradiction and \( X_s \) satisfies (external).

(atomicity)

From definition \( X_s.rmw = X_t.rmw, X_s.coe = X_t.coe, \) and \( X_s.fre = X_t.fre \) hold.

Therefore \( X_s \) preserves atomicity as \( X_t \) preserves atomicity.

Moreover, \( \text{Behavior}(X_s) = \text{Behavior}(X_t) \) holds as \( X_s.co = X_t.co \) holds.

\( \square \)
C Fence Elimination

C.1 Fence Elimination in x86

We restate the theorem on x86 fence elimination.

**Theorem 8.** An MFENCE in an x86 program thread is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

An MFENCE elimination is safe when it is not non-eliminable.

**Proof.** We show:

\[ \mathbb{P}_{\text{src}} \rightarrow \mathbb{P}_{\text{tgt}} \implies \forall X_i \in [\mathbb{P}_{\text{tgt}}] \exists X_s \in [\mathbb{P}_{\text{src}}]. \text{Behavior}(X_i) = \text{Behavior}(X_s) \]

Given a \( X_i \in [\mathbb{P}_{\text{tgt}}] \) we define \( X_s \in \mathbb{P}_{\text{src}} \) by introducing the corresponding fence event \( e \) such that for all events \( w \in X_s, \mathcal{W} \cup X_s, F, \)

- if \((w, e) \in X_s.\text{mo}; X_s.\text{xhb}\) holds then \(X_s.\text{mo}(w, e)\).
- Otherwise \(X_s.\text{mo}(e, w)\).

We know \( X_i \) is consistent. Now we show \( X_s \) is consistent.

We prove by contradiction.

(irrHB) Assume \( X_i \) has \( X_i.\text{xhb} \) cycle. We know the incoming and outgoing edges to \( e \) are \( X_i.\text{po} \) edges and therefore \( X_i.\text{xhb} \) already has a cycle. However, we know \( X_i.\text{xhb} \) is irreflexive. Hence a contradiction and \( X_i.\text{xhb} \) is irreflexive.

(irrMOHB) Assume \( X_s \) has \( X_s.\text{mo}; X_s.\text{xhb} \) cycle. We already know that \( X_i.\text{mo}; X_i.\text{xhb} \) is irreflexive. Therefore the cycle contains \( e \). Two possibilities:

**Case** \( e \in \text{dom}(X_s.\text{xhb}) \) **and** \( e \in \text{codom}(X_s.\text{mo}) \):

Suppose \( X_s.\text{xhb}(e, w) \) and \( X_s.\text{mo}(w, e) \). However, from definition we already know \( X_s.\text{xhb}(e, w) \implies X_s.\text{mo}(w, e) \) when \( w \in X_s, \mathcal{W} \cup X_s, F \). Hence a contradiction and \( X_s.\text{mo}; X_s.\text{xhb} \) is irreflexive in this case.

**Case** \( e \in \text{codom}(X_s.\text{xhb}) \) **and** \( e \in \text{dom}(X_s.\text{mo}) \):

Suppose \( X_s.\text{xhb}(w, e) \) and \( X_s.\text{mo}(e, w) \). However, from definition we already know \( X_s.\text{xhb}(w, e) \implies X_s.\text{mo}(w, e) \) when \( w \in X_s, \mathcal{W} \cup X_s, F \). Hence a contradiction and \( X_s.\text{mo}; X_s.\text{xhb} \) is irreflexive in this case.

(irrFRHB) We know \( X_i \) does not have a \( X_i.\text{fr}; X_i.\text{xhb} \) cycle. We also know \( fr \subseteq (\mathcal{W} \times \mathcal{W}) \) and hence event \( e \in F \) does not introduce any new \( X_s.\text{fr}; X_s.\text{xhb} \) cycle. Therefore \( X_s.\text{fr}; X_s.\text{xhb} \) is irreflexive.

(irrFRMO)

We know \( X_i \) does not have a \( X_i.\text{fr}; X_i.\text{mo} \) cycle. We also know \( fr \subseteq (\mathcal{W} \times \mathcal{W}) \) and hence event \( e \in F \) does not introduce any new \( X_s.\text{fr}; X_s.\text{mo} \) cycle. Therefore \( X_s.\text{fr}; X_s.\text{mo} \) is irreflexive.

(irrFMRP)

Assume \( X_s \) has a \( X_s.\text{fr}; X_s.\text{mo}; X_s.\text{rfe}; X_s.\text{po} \) cycle in \( X_s \) cycle.

In that case the cycle is of the form:

\([X_s.\mathcal{R}]; X_s.\text{fr}; [X_s.\mathcal{W}]; X_s.\text{mo}; [X_s.\mathcal{W}]; X_s.\text{rfe}; [X_s.\mathcal{R}]; X_s.\text{po}; [X_s.\mathcal{R}]\).

We know \( e \in F \) and therefore does not introduce this cycle in \( X_s \).

In that case \( X_s \) already has a \( X_s.\text{fr}; X_s.\text{mo}; X_s.\text{rfe}; X_s.\text{po} \) cycle which is a contradiction.
Hence $X_s.fr; X_s.mo; X_s.rfe; X_s.po$ cycle in $X_s$ is irreflexive.

(irrUF)
Assume $X_s$ has a $X_s.fr; X_s.mo; [X_s.U \cup X_s.F]; X_s.po$ cycle.
Two possibilities

Case $X_s.fr; X_s.mo; [X_s.U]; X_s.po$:
It implies a $X_s.fr; X_s.mo; [X_s.U]; X_s.po$ cycle.
However, we know $X_s$ satisfies (irrUF) and hence a contradiction.

Case $X_s.fr; X_s.mo; [X_s.F]; X_s.po$:
It implies a $[X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [X_s.F]; X_s.po; [X_s.R]$ cycle created by the introduced event $e \in F$.
It implies $[X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R]$
From definition, we know $[X_s.W]; X_s.mo; [\{e\}]$ when $[X_s.W]; X_s.mo; [\{e\}]$ holds.
Thus $[X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R]$
\[\Rightarrow [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R] \]
\[\Rightarrow [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}] \cup [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R] \]
\[\Rightarrow [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}] \cup [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R] \]
Now we consider two subcases:

Subcase $[X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [X_s.W]; X_s.xhb; [X_s.W]; X_s.rfe; X_s.po; [X_s.R]$
\[\Rightarrow [X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [X_s.W]; X_s.xhb; [X_s.W]; X_s.rfe; X_s.po; [X_s.R] \]
This is a contradiction as $X_s$ satisfies (irrFMRP).

Subcase $[X_s.R]; X_s.fr; [X_s.W]; X_s.mo; [\{e\}]; X_s.po; [X_s.R]$
Now we consider the $[X_s.W]; X_s.po; [\{e\}]; X_s.po; [X_s.R]$ subsequence.
Possible cases:

Subsubcase $[X_s.St]; X_s.po; [\{e\}]; X_s.po; [X_s.Ld]$
It implies $[X_s.St]; X_s.po; [X_s.F]; X_s.po; [X_s.Ld]$ from the definition.
\[\Rightarrow [X_s.St]; X_s.po; [X_s.F]; X_s.po; [X_s.Ld] \]
In that case there exists a $X_s.fr; X_s.mo; [X_s.F]; X_s.po$ cycle.
This is a contradiction as \( X_e \) satisfies (irrFMRP).

**Subsubcase** \( [X_e, W]; X_e, po; [\{ e \}]; X_e, po; [X_e, U] : \\)
It implies \( [X_e, W]; X_e, po; [X_e, U] \).
It implies \( [X_e, W]; X_e, mo; [X_e, U] \) as \( X_e \) satisfies (irrMOHB).
In this case \( [X_e, R]; X_e, fr; [X_e, W]; X_e, mo; [X_e, po; \{ e \}]; X_e, po; [X_e, R] \)
\( \Rightarrow [X_e, R]; X_e, fr; X_e, mo; [X_e, U] \)
Hence a contradiction as \( X_e \) satisfies (irrFRMO).

**Subsubcase** \( [X_e, U]; X_e, po; [\{ e \}]; X_e, po; [X_e, Ld] : \\)
It implies \( [X_e, U]; X_e, po; [X_e, Ld] \) and in consequence a \( [X_e, Ld]; X_e, fr; [X_e, W]; X_e, mo; [X_e, U]; X_e, po; [X_e, Ld] \) cycle.
Now, \( [X_e, Ld]; X_e, fr; [X_e, W]; X_e, mo; [X_e, U]; X_e, po; [X_e, Ld] \)
\( \Rightarrow [X_e, Ld]; X_e, fr; X_e, xhb; [X_e, Ld] \cup [X_e, Ld]; X_e, fr; X_e, mo; [X_e, U]; X_e, po; [X_e, Ld] \)
Hence a contradiction as \( X_e \) satisfies (irrFRHB) and (irrUF).

\[
\text{Behavior}(X_e) = \text{Behavior}(X_e) \text{ holds as } X_e, mo|_{loc} = X_e, mo|_{loc}.
\]

**C.2 Fence Elimination in ARMv8**

**Observation.** Let \( P \) be an ARMv8 program generated from an x86 program following the mappings in Fig. 9a. In this case for all consistent execution \( X \in [P] \) the followings hold:

1. A non-RMW load event is immediately followed by a \( F_{LD} \) event.
2. A non-RMW store event is immediately preceded by a \( F_{ST} \) event,
3. An RMW is immediately preceded by a \( F \) event,
4. An RMW is immediately followed by a \( F \) event,

We restate Theorem 9.

**Theorem 9.** Suppose an ARMv8 program is generated by x86 \( \rightarrow \) ARMv8 mapping (Fig. 9b). A DMBFULL in a thread of the program is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

A DMBFULL elimination is safe when it is not non-eliminable.

To prove Theorem 9 we show:

\[
P_{src} \Rightarrow P_{tgt} \quad \Rightarrow \quad \forall X_e \in [P_{tgt}] \exists X_s \in [P_{src}]. \text{Behavior}(X_e) = \text{Behavior}(X_s)
\]

**Proof.** Given a target execution \( X_e \in [P_{tgt}] \) we define a source execution \( X_s \in P_{src} \) by introducing the corresponding fence event \( e \in F \).

We know target execution \( X_e \) satisfies (internal) and (atomic). From definition, source execution \( X_s \) also supports (internal) and (atomic) as the respective relations remain unchanged.

We now prove that \( X_s \) satisfies (external).
We prove by contradiction.
Assume \( X_s \) violates (external).
As a result,

This is a contradiction and hence

It implies

Case\((a, b) \in [X_s.Ld] \times [X_s.E]\): Two subcases:

Subcase\(a \notin \text{dom}(X_s, \text{rmw})\):

It implies \((a, b) \in [X_t.Ld]; X_t.p; [X_t,F_{LD}]; X_t.p; [X_t.E]\) from Observation (1) in Appendix C.2

\[\implies (a, b) \in [X_t.Ld]; X_t.bob; [X_t.E]\]

Hence a contradiction and \(X_s\) violates (external).

Subcase\(a \in \text{dom}(X_s, \text{rmw})\):

It implies \((a, b) \in [X_t.Ld]; X_t.p; [X_t.F]; X_t.p; [X_t,E]\)

\[\implies (a, b) \in [X_t.Ld]; X_t.bob; [X_t.E]\]

Hence a contradiction and \(X_s\) violates (external).

Case\((a, b) \in [X_s.St] \times [X_s.St]\):

\[\implies [X_t.St]; X_t.p; [X_t,F_{ST}]; X_t.p; [X_t.E]\] from Observation (2) in Appendix C.2

\[\implies [X_t.St]; X_t.bob; [X_s.St]\]

This is a contradiction and hence \(X_s\) satisfies (external).

Case\((a, b) \in [X_s.St] \times [X_s.Ld]\):

It implies \((a, b) \in [X_t.St]; X_t.p; [X_t.F]; X_t.p; [X_t.Ld]\) from the condition in ??.

\[\implies [X_t.St]; X_t.bob; [X_s.Ld]\]

This is a contradiction and hence \(X_s\) satisfies (external).

As a result, \(X_s\) also satisfies (external) and is ARMv8 consistent.

Moreover, we know that \(X_s.co = X_t.co\). Hence \(\text{Behavior}(X_s) = \text{Behavior}(X_t)\). 

\[\square\]

We restate Theorem 11.

**Theorem 11.** A DMBST in a program thread is non-eliminable if it is placed on a program path between a pair of stores in the same thread which access different locations and there exists no other DMBFULL or DMBST fence on the same path.

A DMBST elimination is safe when it is not non-eliminable.

To prove Theorem 11 we show:

\[\mathbb{P}_{\text{src}} \rightarrow \mathbb{P}_{\text{tgt}} \implies \forall X_t \in \llbracket \mathbb{P}_{\text{tgt}} \rrbracket \exists X_s \in \llbracket \mathbb{P}_{\text{src}} \rrbracket . \text{Behavior}(X_t) = \text{Behavior}(X_s)\]

**Proof.** Given a target execution \(X_t \in \llbracket \mathbb{P}_{\text{tgt}} \rrbracket\) we define a source execution \(X_s \in \mathbb{P}_{\text{src}}\) by introducing the corresponding fence event \(e \in F\).

We know target execution \(X_t\) satisfies (internal) and (atomic). From definition, source execution \(X_s\) also supports (internal) and (atomic) as the respective relations remain unchanged.

We now prove that \(X_s\) satisfies (external) by showing \(X_s.ob = X_s.ob\).
From definition we know that $X_t\text{.obs} = X_s\text{.obs}, X_t\text{.dob} = X_s\text{.dob}, X_t\text{.aob} = X_s\text{.aob}$.

In that case there exists events $(a, b) \in X_s\text{.bob}$ but $(a, b) \notin X_t\text{.bob}$.

Considering possible cases of $a$ and $b$:

**Case** $(a, b) \in [X_s\text{.Ld}] \times [X_s\text{.E}]$:

It implies $(a, b) \in [X_t\text{.Ld}] \times [X_t\text{.po}] \times [X_t\text{.F} \cup X_t\text{.F}] \times [X_t\text{.E}]$ from Observation (1) and (4) in Appendix C.2

$$\implies (a, b) \in [X_t\text{.Ld}] \times [X_t\text{.bob}] \times [X_t\text{.E}]$$

Hence a contradiction and $X_s$ violates (external).

**Case** $(a, b) \in [X_s\text{.St}] \times [X_s\text{.St}]$:

$$\implies [X_t\text{.St}] \times [X_t\text{.po}] \times [X_t\text{.F} \cup X_t\text{.F}] \times [X_t\text{.po}] \times [X_t\text{.St}] \times [X_t\text{.St}]$$

This is a contradiction and hence $X_s$ satisfies (external).

**Case** $(a, b) \in [X_s\text{.St}] \times [X_s\text{.Ld}]$:

It implies $(a, b) \in [X_s\text{.St}] \times [X_s\text{.F}] \times [X_s\text{.po}] \times [X_s\text{.Ld}]$ as $X_s\text{.bob}(a, b)$ holds.

It implies $(a, b) \in [X_s\text{.St}] \times [X_s\text{.F}] \times [X_s\text{.po}] \times [X_s\text{.Ld}]$

$$\implies [X_t\text{.St}] \times [X_t\text{.bob}] \times [X_s\text{.Ld}]$$

This is a contradiction and hence $X_s$ satisfies (external).

We restate Theorem 13

**Theorem 13.** A DMB in a program thread is non-eliminable if it is the only fence on a program path between a pair of memory accesses in the same thread.  

A DMB elimination is safe when it is not non-eliminable.

To prove Theorem 13 we show:

$$\forall x_t \in [\text{P}_{\text{src}}] \exists x_s \in [\text{P}_{\text{src}}]. \text{Behavior}(x_t) = \text{Behavior}(x_s)$$

**Proof.** From the mapping scheme and the constraint in Theorem 13 in all cases there is a pair of F fences between the access pairs and therefore one of the fences is eliminable.  

**C.3 Fence Weakening in ARMv8**

We restate Theorem 10

**Theorem 10.** A DMBFULL in a program thread is non-eliminable if it is the only fence on a program path from a store to a load in the same thread which access different locations.

For such a fence DMBFULL $\sim$ DMBST; DMBLD is safe.

To prove Theorem 10 we show:

$$\forall x_t \in [\text{P}_{\text{src}}] \exists x_s \in [\text{P}_{\text{src}}]. \text{Behavior}(x_t) = \text{Behavior}(x_s)$$

**Proof.** Given a target execution $X_t \in [\text{P}_{\text{tgt}}]$ we define a source execution $X_s \in \text{P}_{\text{src}}$.

From definition we know that $X_t\text{.obs} = X_s\text{.obs}, X_t\text{.dob} = X_s\text{.dob}, X_t\text{.aob} = X_s\text{.aob}$.

We know target execution $X_t$ satisfies (internal) and (atomic). From definition, source execution $X_s$ also supports (internal) and (atomic) as the respective relations remain unchanged.

We now prove that $X_s$ satisfies (external).

We consider following possibilities:
Case \((a, b) \in [L_d] \times [E]\):

In this case \((a, b) \in [X_s.L_d]; X_s.po; [X_s.F]; X_s.po; [X_s.E]\)
and \((a, b) \in [X_t.L_d]; X_t.po; [X_t.F_L]; X_t.po; [X_t.E]\).

It implies both \(X_s.bob(a, b)\) and \(X_t.bob(a, b)\) hold.

Case \((a, b) \in [S_t] \times [S_t]\):

In this case \((a, b) \in [X_s.S_t]; X_s.po; [X_s.F]; X_s.po; [X_s.S_t]\)
and \((a, b) \in [X_t.S_t]; X_t.po; [X_t.F_S]; X_t.po; [X_t.S_t]\).

It implies both \(X_s.bob(a, b)\) and \(X_t.bob(a, b)\) hold.

We know that \(X_t.ob\) is acyclic and hence \(X_s.ob\) is also acyclic.

As a result, \(X_s\) also satisfies (external) and is ARMv8 consistent.

Moreover, we know that \(X_s.co = X_t.co\). Hence \(\text{Behavior}(X_s) = \text{Behavior}(X_t)\).

\(\square\)
D Proofs and Algorithms of Robustness Analysis

D.1 SC robust against x86

Theorem 14. A program $\mathcal{P}$ is $M$-robust against $K$ if in all its $K$ consistent execution $X$, $X.epo \subseteq X.R$ holds where $R$ is defined as condition $(M-K)$ in Fig. 17.

In this case $R = [R]; po \cup po; [\mathcal{W}] \cup po|_{loc} \cup po; [F]; po$.

Proof. Both x86A and SC satisfies atomicity.
It remains to show that $(X.po \cup X.rf \cup X.fr \cup X.co)$ is acyclic by contradiction.
Assume $(X.po \cup X.rf \cup X.fr \cup X.co)$ creates a cycle.
It implies $(X.po; X.eco)^+$ creates a cycle.
It implies $((X.epo \cup X.epo) \cup fence; X.epo)^+$ has a cycle.
Considering incoming and outgoing $eco$ edges to $po|_{loc}$:

- $X.rf; [Ld]; X.po|_{loc}; [Ld]; X.fre \implies X.co$
- $[\mathcal{W}]; X.po|_{loc}; [Ld]; X.fre \implies X.co$
- $X.rf; [Ld]; X.po|_{loc}; [\mathcal{W}] \implies X.co$

It implies $((po \setminus WR \cup fence \cup co \cup fre) \cup fence)$ has a cycle.
It implies $(po \setminus WR \cup fence \cup fre \cup co \cup fre)$ has a cycle as $coi \cup fri \subseteq po \setminus WR$.
However, we know $(po \setminus WR \cup fence \cup co \cup fre)$ is acyclic and therefore a contradiction.
Hence $X$ satisfies acy($X.po \cup X.rf \cup X.fr \cup X.co$).

D.2 SC, x86 robustness against ARMv8

Theorem 14. A program $\mathcal{P}$ is $M$-robust against $K$ if in all its $K$ consistent execution $X$, $X.epo \subseteq X.R$ holds where $R$ is defined as condition $(M-K)$ in Fig. 17.

In this case $R = po|_{loc} \cup (aob \cup dob \cup bob)^+$.

Proof. Both SC and ARMv8 satisfies atomicity.
It remains to show $(X.po \cup X.rf \cup X.fr \cup X.co)$ is acyclic by contradiction.
Assume $(X.po \cup X.rf \cup X.fr \cup X.co)$ creates a cycle.
If the cycle has one or no $epo$ edge then the cycle violates (sc-per-loc).
Otherwise, the cycle contains two or more $epo$ edges.
It implies $(X.epo; X.eco)^+$ creates a cycle.
It implies $((X.po|_{loc} \cup (X.aob \cup X.bob \cup X.bob)^+); X.eco)^+$ creates a cycle.
Considering $X.po|_{loc}$ with incoming and outgoing $X.eco$, possible cases:

1. $[Ld]; X.po|_{loc}; [Ld]; X.fre; [St] \implies [Ld]; X.fre$
2. $[St]; X.po|_{loc}; [Ld]; X.fre; [St] \implies [St]; X.co$
3. $[St]; X.rf; [Ld]; X.po|_{loc}; [St] \implies [St]; X.co$
4. $(X.co; X.fre; [St]; X.po|_{loc}; [St] \implies X.co \cup X.fre$

Therefore a $((X.po|_{loc} \cup (X.aob \cup X.bob \cup X.bob)^+); X.eco)^+$ cycle implies $((X.aob \cup X.bob \cup X.bob)^+; X.eco)^+$ cycle.
It implies an X.ob cycle which violates (external) and therefore a contradiction.

\[ \text{D.3 Proof of x86A robustness against ARMv8} \]

**Theorem 14.** A program \( P \) is M-robust against K if in all its K consistent execution \( X, X.e_{po} \subseteq X.R \) holds where \( R \) is defined as condition (M-K) in Fig. 7.7

In this case \( R = po|_{loc} \cup (aob \cup bob \cup dob)^+ \cup WR \)

**Proof.** Suppose \( ((X.po \ \setminus \ WR) \cup fence \cup X.rf \cup X.co \cup X.fr) \) is a cycle. It implies \( ((X.po \ \setminus \ WR) \cup fence \cup X.rf \cup X.co \cup X.fr) \) is a cycle as \( coi \subseteq (X.po \ \setminus \ WR) \) and \( fri \subseteq (X.po \ \setminus \ WR) \). It implies \( (X.po \ \setminus \ WR); eco \cup X.fence; X.eco; \cup X.WR|_{loc}; X.eco \cup X.WR|_{\neg loc}; X.eco \) cycle. Now \( X.WR|_{\neg loc} \Rightarrow [St]; (X.po \ \setminus \ WR); [St]|_{\neg loc}; X.eco \). Therefore it implies \( ((X.po \ \setminus \ WR); X.eco \cup X.fence \cup X.WR|_{loc}; X.eco) \) cycle.

Following the definition of epo

It implies \( ((po|_{loc} \cup (X.aob \cup X.dob \cup X.bob)^+); X.eco)^+ \) cycle.

Considering the incoming and outgoing edges for \( X.po|_{loc} \): \( [Ld]; X.po|_{loc}; [Ld]; X.fre \Rightarrow [Ld]; X.fre \)

\( [St]; X.rf; [Ld]; X.po|_{loc}; [St] \Rightarrow [St]; X.co \)

\( (X.fre \cup X.co); [St]; X.po|_{loc}; [St] \Rightarrow (X.fre \cup X.co) \)

\( [St]; X.po|_{loc}; [Ld]; X.fre \Rightarrow [St]; X.co \)

It implies \( (X.aob \cup X.dob \cup X.bob)^+; X.eco)^+ \) creates a cycle.

It implies X.ob creates a cycle which is a contradiction.

Therefore X is x86A consistent.

\[ \text{D.4 SC, x86A, ARMv8, ARMv7-mca robust against ARMv7} \]

**Theorem 14.** A program \( P \) is M-robust against K if in all its K consistent execution \( X, X.e_{po} \subseteq X.R \) holds where \( R \) is defined as condition (M-K) in Fig. 7.7

\[ \text{D.4.1 SC-robust against ARMv7} \]

In this case \( R = po|_{loc} \cup fence \).

**Proof.** Both SC and ARMv7 satisfies atomicity.

It remains to show that \( (X.po \cup X.rf \cup X.fr \cup X.co) \) is acyclic by contradiction.

Assume \( (X.po \cup X.rf \cup X.fr \cup X.co) \) creates a cycle.

If the cycle has one or no epo edge then the cycle violates (sc-per-loc).

Otherwise, the cycle contains two or more epo edges.

It implies \( (X.epo; X.eco)^+ \) creates a cycle.

It implies \( ((X.po|_{loc} \cup X.fence); X.eco)^+ \) creates a cycle.

Considering the incoming and outgoing edges for \( X.po|_{loc} \):

\( [Ld]; X.po|_{loc}; [Ld]; X.fre \Rightarrow [Ld]; X.fre \)

\( [St]; X.rf; [Ld]; X.po|_{loc}; [St] \Rightarrow [St]; X.co \)

\( (X.fre \cup X.co); [St]; X.po|_{loc}; [St] \Rightarrow (X.fre \cup X.co) \)

\( [St]; X.po|_{loc}; [Ld]; X.fre \Rightarrow [St]; X.co \)
It implies \((X.\text{fence}; X.\text{eco})^+\) creates a cycle.

Now we consider \([\text{codom}(fence)]; X.\text{eco}; [\text{dom}(fence)]\) path.

Possible cases:

**Case** \([\text{Ld}]; X.\text{eco}; [\text{Ld}]\):

It implies \(X.\text{fre}; X.\text{rfe}\).

**Case** \([\text{Ld}]; X.\text{eco}; [\text{St}]\):

It implies \(X.\text{fre}\).

**Case** \([\text{St}]; X.\text{eco}; [\text{St}]\):

It implies \(X.\text{coe}\).

**Case** \([\text{St}]; X.\text{eco}; [\text{Ld}]\):

It implies \(X.\text{coe}; X.\text{rfe}\).

Thus an \((X.\text{fence}; X.\text{eco})^+\) cycle implies

a \(((X.\text{coe} \cup X.\text{fre}); X.\text{rfe}^2; X.\text{fence})^+\) cycle.

It implies a \(\text{prop}^+\) cycle which violates (propagation).

Hence a contradiction and therefore SC is preserved.

\[\square\]

**D.4.2 x86A robust against ARMv7**

**Theorem 14.** A program \(\mathbb{P}\) is \(M\)-robust against \(K\) if in all its \(K\) consistent execution \(X, X.\text{epo} \subseteq X.\text{R}\) holds where \(R\) is defined as condition \((M-K)\) in Fig. [7]

In this case \(R = \text{po}|_{\text{loc}} \cup \text{fence} \cup \text{WR}\).

**Proof.** Suppose \(((X.\text{po} \setminus \text{WR}) \cup X.\text{rfe} \cup X.\text{co} \cup X.\text{fr})\) is a cycle.

It implies \(((X.\text{po} \setminus \text{WR}) \cup X.\text{rfe} \cup X.\text{co} \cup X.\text{fr})\) is a cycle.

It implies \(((X.\text{po} \setminus \text{WR}) \cup X.\text{fence} \cup X.\text{rfe} \cup X.\text{co} \cup X.\text{fre})\) is a cycle as \(\text{coi} \subseteq \text{WW}\) and \(\text{fri} \subseteq (X.\text{po} \setminus \text{WR})\).

It implies \(((X.\text{po} \setminus \text{WR}) \cup X.\text{eco} \cup X.\text{fence}; X.\text{eco} \cup X.\text{rfe} \cup X.\text{WR}|_{\text{loc}}; X.\text{eco} \cup X.\text{WR}|_{\not= \text{loc}}; X.\text{eco})\) cycle.

Now \(X.\text{WR}|_{\not= \text{loc}} \Rightarrow \text{[St]}; (X.\text{po} \setminus \text{WR})\) \(\text{[St]}|_{\not= \text{loc}}; X.\text{eco}\).

Therefore it implies \(((X.\text{po} \setminus \text{WR}) \cup X.\text{eco} \cup X.\text{fence}; X.\text{eco} \cup X.\text{WR}|_{\text{loc}}; X.\text{eco})\) cycle.

It implies \(((\text{po}|_{\text{loc}} \cup \text{fence}) \cup X.\text{eco})^+\) cycle following the definition of epo.

Considering the incoming and outgoing edges for \(X.\text{po}|_{\text{loc}}\):

\( [\text{Ld}]; X.\text{po}|_{\text{loc}}; [\text{Ld}]; X.\text{fre} \Rightarrow [\text{Ld}]; X.\text{fre} \)

\( [\text{St}]; X.\text{rfe}; [\text{Ld}]; X.\text{po}|_{\text{loc}}; [\text{St}] \Rightarrow [\text{St}]; X.\text{coe} \)

\( (X.\text{fre} \cup X.\text{coe}); [\text{St}]; X.\text{po}|_{\text{loc}}; [\text{St}] \Rightarrow (X.\text{fre} \cup X.\text{coe}) \)

\( [\text{St}]; X.\text{po}|_{\text{loc}}; [\text{Ld}]; X.\text{fre} \Rightarrow [\text{St}]; X.\text{coe} \)

It implies \((X.\text{fence}; X.\text{eco})^+\) creates a cycle.

It implies \(X.\text{prop}\) creates a cycle which is a contradiction.

Therefore \(X\) is x86A consistent.

\[\square\]

57
D.4.3 ARMv7 robust against ARMv8

**Theorem 14.** A program $P$ is $M$-robust against $K$ if in all its $K$ consistent execution $X$, $X.epo \subseteq X.R$ holds where $R$ is defined as condition $(M-K)$ in Fig. [7].

In this case $R = po\mid_{loc} \cup [St]; po \cup$ fence.

*Proof.* We show $X$ is ARMv8 consistent.

(internal) Assume a $(X.po\mid_{loc} \cup X.fr \cup X.co \cup X.rf)$ cycle. However, $X$ satisfies (sc-per-loc) and hence a contradiction. Therefore, $X$ satisfies (internal).

(external) Assume a $X.ob$ cycle. It implies $(X.obs; (X.aob \cup X.bob \cup X.dob))^+$ creates cycle. From the definition, $(X.aob \cup X.bob \cup X.dob) \subseteq po\mid_{loc} \cup fence \cup [St]; po and therefore ((X.rfe \cup X.coe \cup X.fre); (X.po\mid_{loc} \cup fence))^+$ creates cycle. It implies prop creates a cycle which violates (propagation). Therefore a contradiction and $X$ satisfies (external).

(atomicity) ARMv7 execution $X$ satisfies (atomicity). Therefore $X$ has only ARMv8 execution.

D.4.4 ARMv7-mca robust against ARMv7

**Theorem 14.** A program $P$ is $M$-robust against $K$ if in all its $K$ consistent execution $X$, $X.epo \subseteq X.R$ holds where $R$ is defined as condition $(M-K)$ in Fig. [7].

In this case $R = [Ld]; po\mid_{loc} \cup fence; [Ld]$.

*Proof.* We show that $X$ satisfies (mca). Assume $X$ violates (mca) and therefore a $wo^+$ cycle. It implies a $(X.rfe; [Ld]; X.ppo; [Ld]; X.fre)^+$ cycle. However, $[Ld]; X.ppo; [Ld] \subseteq po\mid_{loc}$ violates (sc-per-loc) and therefore a contradiction. Otherwise it implies a $(X.rfe; [Ld]; X.fence; [Ld]; X.fre)^+$ cycle. It implies a $X.prop$ cycle which violates (propagation) Therefore a contradiction and hence $X$ is ARMv7-mca consistent.