LETTER

An effective DC offset calibration method combined with analog and digital circuits for direct conversion receivers

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Abstract This paper presents a DC offset calibration (DCOC) method combined with analog and digital circuits for direct conversion receivers. To work effectively, the LNA is shut off for better isolation and replaced by an equivalent resistance to keep the same transfer function of DC offset between calibration and operation. This method adopts DACs to compensate DC offset, then averages and eliminates the residual DC offset in the digital domain. Measurements show that this DCOC method achieves 0.44 mV DC offset and improves IM2 by 10dB. The DCOC circuits occupy 0.23 mm² in 40nm CMOS and consume 124uA at 1.3V supply.

key words: DC offset calibration, direct conversion receiver, DAC

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the rapid development of wireless communication systems, software defined radio (SDR) has been more attractive to support various applications such as WIFI, WCDMA, GSM, short-wave radio and radar [1, 2, 3]. Direct conversion receiver (DCR) architecture is the most common solution to SDR for its flexibility and reconfigurability [4]. However, the performance of DCR has been limited by 1/f noise, I/Q mismatch, and DC offset. With the trend of technology scaling down in advanced CMOS technology, the DC offset becomes the most serious problem, which will deteriorate the linearity performance and the SNR [4, 5, 6], especially for some high precision applications like biomedical imaging based on Doppler radar [6]. Although the DC offset can be removed by traditional analog methods like ac coupling [7] or LPF feedback loop [8, 9, 10, 11], these methods take up a large area and have long pulse response time [9, 12, 13, 14]. With the development of digital signal processing, many digital-assisted methods adopt DACs to compensate DC offset combined with digital logic.

However, these methods usually need to short or disconnect the input of LNA, which have low isolation from the antenna [4, 15]. Besides, some methods operate in real time and eliminate DC offset through digital filter. These methods suffer from signal distortion and large consumption of digital resources [16, 17]. This paper proposes an effective DC offset calibration method combined with analog and digital circuits. In order to obtain better isolation, the LNA is shut off rather than simply disconnected from the antenna. To keep the same transfer function of DC offset between calibration and operation, the power-off LNA is replaced with an equivalent resistance when calibrating. After cancelling the DC offset through DACs from the Mixer to the LPF in the analog domain, this method averages the residual DC offset at the output of ADC and subtracts it during operation. This calibration process works only during startup which has no loss to the received signal during operation. And the digital part of this method reduces the design requirement for the analog circuits such as the resolution of DACs and the mismatch of comparators.

This paper is organized as follows: Section 2 characterizes the architecture of the receiver and analyzes the mechanism of the DC offset in the DCR. Section 3 describes the implementations of the proposed DCOC method and circuits. Section 4 reports the measured results. The conclusion is drawn in Section 5.

2. Receiver architecture and DC offset mechanism

2.1 Architecture of the receiver

The detailed block diagram of the receiver is shown in Fig. 1. A broadband LNA using resistance feedback suppresses the noise from the following stage [18, 19]. The current driven passive Mixers (I/Q) as proposed in [20, 21] convert the signals down to the baseband. The output baseband signal of each Mixer is fed into a 4-order Chebyshev LPF which serves as a channel selector [22]. Finally, all the baseband signals are digitized in ADCs. The DCOC circuits consist of 4 DACs to compensate the DC offset, 4 hysteresis comparators to observe the DC offset in the analog domain, and 2 digital averaging circuits to detect the residual DC offset in the digital domain. The DCOC are carried out combined...
with successive approximation (SAR) algorithm and the calibration results are stored in the memories.

In order to satisfy various applications, the specifications of the receiver are summarized in Table I.

| RF Bandwidth   | 0.2-2.7GHz |
|----------------|------------|
| IF Bandwidth   | 1-32MHz    |
| Gain Range     | 5-65dB (LNA:5-15dB, Mixer:0-27dB, LPF:0-23dB) |
| Noise Figure   | <5dB       |

**Table I. Specifications of the receiver**

2.2 DC offset mechanism

The DC offset in the DCR is divided into two components: the time-invariant DC offset resulting from device mismatches in the signal path, and the time-varying DC offset caused by LO-leakage and self-mixing [15]. In this paper, only the time-invariant DC offset is taken into account for the following reasons. Firstly, due to high attenuation and absorbance of the reflected signals at multi-GHz frequencies (2.7GHz in this receiver), the time-varying DC offset is much smaller (less than 10mV) compared to the dynamic range of the receiver [23]. Secondly, the layouts of the Mixer and the LO paths are metal-shielded to achieve better isolation. Thus the influence of the LO-leakage and self-mixing is effectively suppressed. Finally, the problem of device mismatches becomes more serious with the deeply scaled devices (40nm minimum channel length in this design).

As shown in Fig. 2, the output impedance of the transconductance stage is given by:

\[
Z_{outRF} = \left( \frac{1}{2\pi f_{LO} C_1} + R_{out} \right) \left( \frac{1}{2\pi f_{LO} C_2} \right) \left( \frac{1}{2\pi f_{LO} C_3} \right) \left( \frac{1}{2\pi f_{LO} C_4} \right) \left( \frac{1}{2\pi f_{LO} C_5} \right) \left( \frac{1}{2\pi f_{LO} C_6} \right)
\]

(1)

\( R_{out} \) represents the output impedance of the LNA, and changes with the gain of the LNA. \( C_1, C_2 \) are the parasitic capacitances of the circuits. \( G_m \) is the transconductance of the Mixer.

Through the switching of the passive mixer, these capacitances are converted to an equivalent resistance at the output of the passive mixer, which is similar to a classical switched capacitor circuit [24, 25, 26]. The value of the equivalent output resistance \( R_{outRF} \) is proportional to \( Z_{outRF} \) and decreases dramatically as the LO frequency increasing [22].

If \( V_{osin} \) is the equivalent input DC offset voltage of the differential operation amplifier (OPAMP), \( R_f \) is the feedback resistance of the trans-impedance amplifier. \( I_n, I_p \) are the compensation currents of the differential DAC. The output DC offset voltage \( V_{osout} \) can be expressed as follows [22, 27, 28]:

\[
V_{osout} = \left( 1 + \frac{R_f}{R_{outRF}} \right) V_{osin} + (I_n - I_p) R_f
\]

(2)

Based on the above analysis, the variation of \( R_{out} \) should be kept as small as possible during calibration and operation, especially at multi-GHz frequencies. As a result, the equivalent output resistance \( R_{outRF} \) and the transfer function of DC offset will stay the same during calibration and operation. And the DCOC method should be repeated according to the LO frequency and the gain at a selected temperature [17, 23].

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**Fig. 1** The detailed block diagram of the receiver

**Fig. 2** Schematic of the Mixer
3. The method of DCOC and circuits design

3.1 DCOC method
This DCOC method as shown in Fig. 3 is carried out as follows. Initially, the DAC is set in the middle code to inject one more least significant bit (LSB) current to one of the balanced branches. Combined with Fig. 1, the LNA is shut off for better isolation from the antenna rather than simply disconnected or shorted at the input side. Then, a two-way switch $S_1$ is added in serial at the output of LNA. And during calibration, $S_1$ is switched from the LNA side to a programmable resistance $R_{LNA}$. $R_{LNA}$ is introduced to replace the output impedance of the LNA and obtain the same transfer function of DC offset between calibration and operation. The magnitude of the $R_{LNA}$ depends on the structure of the LNA and is tuned according to the LNA’s gain. With typical parameters, the variation $\pm 20\%$ of the $R_{LNA}$ can be tolerated. Next, the DCOC method in the analog domain compensates the DC offset in the Mixer stage. It sets the DAC combined with SAR algorithm according to the output of the comparator. For accurate results, the DAC changes 1 LSB in the opposite direction after the LSB of the DAC is set. And this checking procedure is executed repeatedly until the opposite results of the comparator are achieved between the adjacent steps. Because of the checking procedure, one calibration cycle in the Mixer stage takes at least 10 clock cycles through an 8-bit DAC. The reference clock is programmed according to the bandwidth of the baseband. Then, the same DCOC procedure is carried out in the LPF stage.

After the analog part of DCOC is completed, the output signals of the ADC will be averaged for a programmable length in the time domain to estimate the residual DC offset. Then, the residual DC offset will be eliminated by subtracting the estimated result when operation. The codes of the DACs and the average result of the ADC are stored in the memory. Till now, the DCOC method for one gain step is accomplished.

A DCOC procedure of LPF in the analog domain is shown in Fig. 4. The $8^{th}$ -$10^{th}$ steps guarantee that the calibration result is affected little by the noise. With temperature variation, the DC offset can be recalibrated by the processor according to the temperature sensor which integrated in the transceiver on chip.

![Fig. 3 The flow diagram of the DCOC method](image)

![Fig. 4 A DCOC procedure of LPF in the analog domain](image)
3.2 Circuits design
The range and resolution of the DCOC in the analog domain depend on the full scale and the LSB current of the DAC [29].

Combined with Fig. 2 and Eq. (2), the LSB current $I_{lsb1}$ and the full scale of the DAC $I_{total1}$ in the Mixer stage can be derived as follows [30]:

\[ I_{lsb1} = \frac{|V_{osout, min}|}{R_f} \] (3)

\[ I_{total1} = \left( \frac{1}{R_f} + \frac{1}{R_{out1}} \right) |V_{osin}| \] (4)

$|V_{osout, min}|$ stands for the same resolution of the DCOC at the output of the Mixer and the LPF in the analog domain. $I_{lsb1}$ is inversely proportional to $R_f$ to obtain the same resolution after re-calibration at different temperatures. Similarly, if the OPAMP is shared by the Mixer and LPF, the LSB current $I_{lsb2}$ and the full scale of the DAC $I_{total2}$ in the LPF stage are given by:

\[ I_{lsb2} = \frac{|V_{osout, min}|}{R_f R_4 R_5} \] (5)

\[ I_{total2} = \frac{1}{R_1} |V_{dc}| + \left( \frac{1}{R_2} + \frac{1}{R_4} \right) + \left( 1 + \frac{R_3}{R_4} \right) \frac{1}{R_2} |V_{osin}| \] (6)

$|V_{dc}|$ stands for the residual DC offset of the Mixer. $\frac{R_2}{R_4}$ and $\frac{R_3}{R_5}$ represent the gain of the first and second stage of the LPF.

In order to obtain the full scale of the DAC, the input equivalent DC offset of the OPAMP is simulated using Monte Carlo simulation. The results (including temperature variation: -40-80°C) are shown in Table II [30]. To meet the system requirements like noise, power consumption, and linearity, the detailed parameters of the receiver are given in Table III.

| Table II. Simulation results of the DC offset of the OPAMP |
| --- |
| Mean | Max | Variance |
| 0.529mV | 1.819mV | 0.394mV |

| Table III. Parameters of the receiver |
| --- |
| The FIA of Mixer | The 1st stage of LPF | The 2nd stage of LPF |
| Gain range | 15-27dB | Gain range | 0-18dB | Gain range | 0-5dB |
| $R_f$ (Ω) | 500-2000 | $R_1$ (Ω) | 100-800 Max BW | $R_2$ (Ω) | 340-600 Max BW |
| $R_2$ (Ω) | 400-3200 Min BW | $R_3$ (Ω) | 1360-2400 Min BW |

Combined with the above conditions, an 8-bit current-steering DAC which is adopted in both Mixer and LPF stage is shown in Fig. 5. Missing codes are not allowed in SAR algorithm [17]. So the differential nonlinearity (DNL) of the DAC must be less than 1 LSB. This thermometer-coding DAC achieves the minimum DNL in a limited area [32]. And the LSB current of the DAC is 120mA to achieve 1.4 mV (~50dBFS relative to the full scale of the ADC: 6.5dBm) residual DC offset ($|V_{osout, min}|$) after DCOC in the analog domain.

Fig. 5 The block diagram of DAC

Fig. 6 The block diagram of comparator

The hysteresis comparator added with clock is shown in Fig. 6.

4. Measurement result
This chip is fabricated in 40nm CMOS and the microphotography is shown in Fig. 7. The whole receiver (except ADC) occupies 1.15 mm² and dissipates 126mA at 1.3V. And the DCOC circuits occupy only a small area of 0.23 mm² and consume 124μA.

Fig. 7 Layout and chip microphotograph

The measured result of DCOC (@ maximal bandwidth, 2.7GHz RF frequency) is shown in Fig. 8. When the DCOC is carried out in the analog domain, the DC offset is reduced from -20dBFS (40mV) to -50dBFS (1.4mV). Then, with the assistance of the digital calibration, the
residual DC offset is reduced to -60dBFS (0.44mV). The measured results show that the DC offset varies little through time. Fig. 9 shows the measured results of DCOC (@ maximal bandwidth) according to different LO frequencies.

In order to measure the linearity performance (@ maximal bandwidth, minimum gain, 1.5GHz RF frequency), two tones with a frequency offset of 4 MHz are applied. As the FFT results shown in Fig. 10, the 2nd order inter-modulation (IM2) decreases from -82.8dBFS (without DCOC) to -92.6dBFS (with DCOC).

The performance of the receiver is summarized in Table IV with the comparison to other DCOC methods. Compared with others, this DCOC method achieves an excellent calibration result of residual DC offset (less than 0.44mV). And it works effectively with the maximum bandwidth.

| Table IV. Measured performance and comparison |
|-----------------------------------------------|
| Technology | [16] | [27] | [33] | This Work |
| Supply (V) | 1.2 | 1.5 | N/A | 1.3 |
| RF (GHz) | 0.86-0.96 | N/A | N/A | 0.2-2.7 |
| IM2 (MHz) | 1.28 | 12.1 | N/A | 32 |
| Residue DC (mV) | 7 | 5 | 63.7 | 0.44 (from 40mV) |
| IM2 | N/A | 64dBm (OIP2) | N/A | -92.3dBFS (min gain) |
| DCOC method | Analog foreground | Analog foreground | Analog foreground | Analog foreground |
| DCOC area (mm²) | N/A | 0.03 (DAC only) | 0.13 | 0.23 |
| DCOC power (mW) | N/A | 0.23 (DAC only) | 0 | 0.16 |
| Total area (mm²) | 1.69 | 1.2 | 1.77 | 1.15 |
| Total power (mW) | 24.3 | 43.5 | N/A | 160 |

* [33] and this work include I&Q paths.

5. Conclusion

A DCOC method combined with analog and digital circuits for DCR is proposed in this paper. The DCOC method calibrates the DC offset of each stage through DACs and reduces the residual DC offset in the digital domain. By shutting off the LNA and replacing it with a resistance during calibration, the DCOC method obtains better isolation from the antenna and works effectively in the whole RF bandwidth. And the design requirement for analog circuits such as DACs and comparators is reduced due to the assistance of the digital part of the DCOC. The measured results indicate that the DCOC method obtains -60dBFS (0.44mV) DC offset reduction and improves the IM2 by 10dB. The receiver is implemented in 40nm CMOS technology and the DCOC circuits occupy 0.23mm² with a power consumption of 124uA under the supply of 1.3V.

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