A Physic-Based Explicit Compact Model for Reconfigurable Field-Effect Transistor

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ABSTRACT
In this paper, a compact model for the double-gate Reconfigurable Field-Effect Transistor (RFET) is presented. Firstly, the physics-based surface potential model is derived by solving Poisson’s equation at different channel regions. Then an explicit expression of drain current is analytically obtained based on the theory of band-to-band tunneling at the Schottky junction. The proposed model shows excellent agreement with TCAD simulations which have been calibrated with experimental data. Finally, the compactible model is implemented in Verilog-A language without convergence problem, and proven by the RFET-based logic circuit.

INDEX TERMS
Reconfigurable field-effect transistor, analytical model, surface potential, drain current, Verilog-A.

I. INTRODUCTION
With the rapid development of neuromorphic computing, high-throughput data put forward with substantial requirements for downscaling and power-efficient electronic circuits. However, it becomes increasingly challenging to simply reduce the size of devices based on conventional complementary metal-oxide-semiconductor (CMOS) technology due to their physical limitations. The reconfigurable field-effect transistors (RFET) have emerged as a promising candidate for the single device with tunable polarity [1]–[4]. Instead of conventional physical doping, feature gated Schottky junctions of the RFETs can controllably inject electrons or holes into the channel. In this case, the RFETs can provide both n- and p-FET device patterns by adjusting the bias of the polarity gate [5]–[8]. When one gate injects electrons into the channel, and the other gate stops the holes, then the n-type RFETs are obtained. Similarly, the p-type can also be obtained by reversed bias. By increasing the number of functions per transistor rather than reducing the size of the device [9]–[11], the RFETs are expected to provide reliable and reprogrammable CMOS operation, which are beneficial to pave the way to silicon circuits that go beyond Moore’s law.

Recently, several RFETs have been fabricated based on top-down or bottom-up processes [12]. The experimental results show a high on/off ratio (∼10⁹) and extremely low gate leakage (∼10⁻¹⁴ A), which make such a device concept desirable for energy-efficient circuit applications. Besides, a high-density synaptic device based on RFET has been proposed to build XNOR binary neural network [13]. Besides, the impact of work-function modulation, gate/spacer-channel underlap have been investigated through numerical simulations [14], [15].

To further understand the mechanism of the RFET, optimize its device characteristics and perform circuit design, it is essential to develop a physics-based compact model. An analytical surface potential and drain current model is reported in [16] by solving drift-diffusion equation in the channel with Schottky tunneling at the source/drain contact. However, the drain current of this model is expressed as an implicit function of quasi-fermi potentials. The complex computational process may cause convergence issues during circuit simulation. Besides, for low drain biases, the model results mentioned in [16] are not in good agreement with the simulations. Thus, the major objective of this paper is to provide a compact model that has no convergence and
In this paper, a closed-form surface potential-based model for the double-gate RFET is put forward, which is performed in the x and y two-dimensional plane. The silicon channel is divided into three regions to solve the 2D Poisson’s equation. To begin with, the surface potential model is developed using several boundary conditions. Then the charge density model is derived from the current continuity equation. Finally, the drain current model for the RFET is given based on the theory of band-to-band tunneling induced by the Schottky junctions. After Taylor expansion and proper approximation, an explicit analytical compact drain current model is developed. The accuracy of the proposed model is validated by numerous TCAD simulations after calibration with the experimental data. Besides, the explicit nature of the model makes it suitable to be a SPICE compatible model, which is beneficial for circuit simulations.

The remainder of this article is organized as follows. Section II describes the device structure and the simulation environment. Section III introduces the derivation of explicit surface potential, charge density and drain current model for the RFET. In Section IV, the implementation of the proposed compact model in Verilog-A is discussed, which is useful for RFET-based circuit simulations. Finally, Section V concludes this article.

II. DEVICE STRUCTURE AND SIMULATION SETUP

Fig. 1 shows the structure of the double-gate RFET. To note that, the source/drain contacts are metallic (typically NiSi$_2$) to induce lateral Schottky junctions, which is also beneficial to decrease the parasitic capacitance and resistance. In order to modulate the device polarity electrically, the control gate (gate1) and polarity gate (gate2) are applied. Simulations are performed by technology computer-aided design (TCAD) simulations [17]. Based on the experimental data reported in [4], the same structure of RFET is employed to calibrate the simulation setup. Carrier recombination includes Band-to-Band recombination, Shockley-Read-Hall (SRH) recombination and Auger combination. The Wentzel-Kramers-Brillouin (WKB) approximation is employed for the band-to-band tunneling (BTBT) model, with electron and hole tunneling masses as 0.3 $m_0$ and 0.2 $m_0$ [16]. The thermionic-field emission model has been applied at the (S/D) Schottky junctions, and the Schottky barriers for electrons and holes are considered to be 0.58 eV and 0.54 eV respectively [18]. Besides, the quantization effects are taken into consideration by introducing electronic quantum potential and hole quantum potential. Besides, high-field Saturation model, Lombardi mobility model, and Philips unified mobility model are included in the Mobility model. It can be observed from Fig. 2 that the transfer characteristic curves plotted with the TCAD simulator agree well with the experimental results, which proves the validity of our simulation environment. In the following studies, the parameters used in this work are presented in Table 1.

III. MODEL DEVELOPMENT

A. SURFACE POTENTIAL MODEL

As shown in Fig. 1, the silicon channel is divided into three regions. Region 1 and Region 2 are Schottky-gated with
gate1 and gate2, while Region 3 is not modulated with an external gate. Firstly, the two-dimensional (2D) Poisson’s equation can be solved to obtain the surface potentials in Region 1 and Region 2.

\[
\frac{\partial^2 \phi_{1/2}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_{1/2}(x, y)}{\partial y^2} = \frac{qN_C}{\varepsilon_{Si}} \tag{1}
\]

where \(\phi_{1/2}(x, y)\) refers to the electrostatic potential of Region 1 or Region 2. \(\varepsilon_{ox}\) and \(\varepsilon_{Si}\) are the permittivities of silicon dioxide and silicon respectively. \(N_C\) is the doping concentration of the silicon channel.

The boundary conditions along \(y\)-direction (channel thickness) can be given as

\[
\begin{align*}
\frac{\partial \phi_{1/2}(x, y)}{\partial y} \bigg|_{y=0} &= \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \phi_{1/2}(x, 0) - V_{\text{geff}} \tag{2a} \\
\frac{\partial \phi_{1/2}(x, y)}{\partial y} \bigg|_{y=L_{Si}} &= \frac{\varepsilon_{ox}}{\varepsilon_{Si}} V_{\text{geff}} - \phi_{1/2}(x) \tag{2b}
\end{align*}
\]

where \(V_{\text{geff}} = V_{g1/g2} - V_{FB}\), \(V_{g1/g2}\) is the voltage applied on gate1 or gate2, and \(V_{FB}\) is the flat band voltage.

Using the parabolic approximation [19], the electrostatic potential for Region 1 or Region 2 can be written as

\[
\phi_{1/2}(x, y) = p(x) + q(x)y + r(x)y^2 \tag{3}
\]

Assuming \(\phi_{1/2}(x, 0) = \phi_{1/2}(x, t_{Si}) = \phi_{1/2}(x)\), the surface potential for Region 1 \((\phi_1(x))\) and Region 2 \((\phi_2(x))\) can be solved and expressed as

\[
\begin{align*}
\phi_1(x) &= C_1 \exp\left(\frac{x}{\lambda}\right) + D_1 \exp\left(-\frac{x}{\lambda}\right) + P_1 \tag{4a} \\
\phi_2(x) &= C_2 \exp\left(\frac{x}{\lambda}\right) + D_2 \exp\left(-\frac{x}{\lambda}\right) + P_2 \tag{4b}
\end{align*}
\]

where \(\lambda = \sqrt{\frac{2\varepsilon_{ox}t_{Si}}{qN}\frac{\varepsilon_{Si}}{\varepsilon_{Si}}}\), \(P_1 = V_{g1} - \frac{qN_C}{\varepsilon_{Si}}\varepsilon_{Si}\), and \(P_2 = V_{g2} - \frac{qN_C}{\varepsilon_{Si}}\varepsilon_{Si}\).

The boundary conditions along \(x\)-direction (channel length) can be expressed as

\[
\begin{align*}
\phi_1(0) &= V_s + (-1)^k \frac{X - W_m}{q} \tag{5a} \\
\phi_2(L_c) &= V_d - (-1)^k \frac{X - W_m}{q} \tag{5b}
\end{align*}
\]

where \(X\) is the electronic affinity, \(W_m\) is the metal work-function, \(V_d\) and \(V_s\) are the voltage applied on the drain and source respectively. Besides, \(k\) is an even number for the n-program and an odd number for the p-program.

Using the boundary conditions Equations (5a) and (5b), the constants \(C_1, D_1, C_2, D_2\) can be derived.

\[
\begin{align*}
C_1 &= \frac{q\phi_{L1} + M \exp\left(\frac{-L_1}{L}\right)}{2q \sinh\left(\frac{L_1}{L}\right)} \tag{6a} \\
D_1 &= -\frac{q\phi_{L1} + M \exp\left(\frac{L_1}{L}\right)}{2q \sinh\left(\frac{L_1}{L}\right)} \tag{6b} \\
C_2 &= \frac{q\phi_{L2} \exp\left(-\frac{L_2}{L}\right) + N \exp\left(-\frac{L_2}{L}\right)}{2q \sinh(L_2 - L_c)} \tag{6c} \\
D_2 &= -\frac{q\phi_{L2} \exp\left(\frac{L_2}{L}\right) + N \exp\left(\frac{L_2}{L}\right)}{2q \sinh(L_2 - L_c)} \tag{6d}
\end{align*}
\]

where \(\phi_{L1} = \phi_{L1}, \phi_{L2}(L_c) = \phi_{L2}, M = (-1)^k(W_m - \chi) - qV_s + qP_1, N = (-1)^k(W_m + \chi) - qV_d + qP_2\).

In order to obtain the potential distribution in Region 3, the gradual channel approximation is employed. The surface potential for Region 3 can be expressed as

\[
\phi_3(x) = \frac{\phi_{L2} - \phi_{L1}}{L_2 - L_1}(x - L_1) + \phi_{L1} \tag{7}
\]

Because of the continuity of the surface potential and its first derivative, the boundary conditions can be given as

\[
\begin{align*}
\phi_1(L_1) &= \phi_3(L_2) = \phi_{L1} \tag{8a} \\
\phi_2(L_2) &= \phi_3(L_2) = \phi_{L2} \tag{8b} \\
\frac{\partial \phi_1(x)}{\partial x} \bigg|_{x=L_1} &= \frac{\partial \phi_3(x)}{\partial x} \bigg|_{x=L_1} \tag{8c} \\
\frac{\partial \phi_2(x)}{\partial x} \bigg|_{x=L_2} &= \frac{\partial \phi_3(x)}{\partial x} \bigg|_{x=L_2} \tag{8d}
\end{align*}
\]

Using the boundary conditions mentioned above, the surface potential \(\phi_{L1}\) and \(\phi_{L2}\) are solved for both n- and p-type RFETs, as shown in Fig. 4.

**B. CHANNEL CHARGE DENSITY MODEL**

Based on the surface potential, the electric field \(E\) of the channel surface along the \(x\)-direction can be calculated.

\[
\begin{align*}
E_m(x) &= -\frac{d}{dx} \phi_m(x) \tag{9a} \\
E_p(x) &= -\frac{d}{dx} \phi_p(x) \tag{9b}
\end{align*}
\]
The model and simulation results are shown in Fig. 5 for both n- and p-type RFETs.

Then the relationship between the carrier mobility (\(\mu\)) and the surface electric field can be given as

\[
\mu_{n/p} \propto \begin{cases} 
E_{n/p}(x)^{-\frac{1}{2}}, & 10^3 < E < 10^5 \text{V/cm} \\
E_{n/p}(x)^{-1}, & E > 10^5 \text{V/cm} 
\end{cases}
\] (10)

A kind of continuity equations which describe charge conservation is shown below

\[
\nabla \cdot J_n = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{11a}
\]

\[
\nabla \cdot J_p = -qR_{net,p} - q\frac{\partial p}{\partial t} \tag{11b}
\]

where \(R_{net,n}\) and \(R_{net,p}\) are the electron and hole net recombination rates, respectively.

In addition, by solving the current continuity equation, the current density in the n-type and p-type channel can be expressed as

\[
J_n = q\mu_n n(x) |E_n(x)| \tag{12a}
\]

\[
J_p = -q\mu_p p(x) |E_p(x)| \tag{12b}
\]

When the channel reaches its equilibrium state, the carrier concentration does not change, so \(\frac{\partial n}{\partial t}\) and \(\frac{\partial p}{\partial t}\) are considered to be zero. By combining Equations (11a) and (12a), (11b) and (12b), the charge densities of both n-type and p-type channels are derived, which are shown in Fig. 6.

C. DRAIN CURRENT MODEL

Using the Kane’s model [20], the band-to-band generation rate \(G_{BTB}\) can be derived as

\[
G_{BTB} = A(E_{avg})^{D-1} \exp \left(-\frac{B}{E_{avg}}\right)E \tag{13}
\]

The band-to-band tunneling probability is used to calculate the drain current across the Schottky barrier nearby the source.

\[
I = q \int G_{BTB}dV = Aq \int (E_{avg})^{D-1} \exp \left(-\frac{B}{E_{avg}}\right)EdV \tag{14}
\]
where $A$, $B$ and $D$ are Kane’s tunneling parameters given by [21]. $E_{xy} = E_g/q_x$ refers to the electric field on average, $E_g$ is the bandgap of silicon, and $x$ is the tunneling path from $x_1$ to $x_2$ shown in Fig. 3(a) and (b). $x_1$ represents the starting point of the tunneling, and $x_2$ represents the ending point of the tunneling.

The expressions of $x_1$ and $x_2$ can be calculated by [22]

$$x_1 = \lambda \ln \left( \frac{\theta_a + \sqrt{\theta^2_a - 4C_1D_1}}{2C_1} \right) \quad (15a)$$

$$x_2 = \lambda \ln \left( \frac{\theta_b + \sqrt{\theta^2_b - 4C_1D_1}}{2C_1} \right) \quad (15b)$$

where $\theta_a = E_g + \frac{\phi_i}{q} + \frac{\beta}{\alpha}$, $\theta_b = E_g + \frac{\phi_s}{q} + \frac{\beta}{\alpha}$, $\alpha = \frac{1}{2}$, $\beta = -qN_c^{-\frac{3}{2}} - \frac{V_{bi}}{x_0}$, $\Phi_1 = E_{\text{Source}} - E_{\text{F}}$, and $\Phi_2 = E_{\text{V}} - E_{\text{Channel}}$.

Besides, the electric field is obtained by

$$E = \sqrt{E_x^2 + E_y^2} = \left[ -\frac{\partial}{\partial x} \psi_1(x) \right]^2 + \left[ -\frac{\partial}{\partial y} \psi_1(x, y) \right]^2 \quad (16)$$

The expression of $E_x$ and $E_y$ can be obtained from (4a) and (3), respectively. The electric field can be given as

$$E = \left[ -\frac{1}{\lambda} C_1 \exp \left( \frac{\lambda}{x} \right) \right] + \frac{1}{\lambda} D_1 \exp \left( -\frac{\lambda}{x} \right) + \left( -q(x) - 2r(x)y \right)^2 \quad (17)$$

The unary Taylor expansion is applied to the $E_x$ and subsequently binary Taylor expansion is applied to $E$, the expression can be simplified as

$$E = \eta + \frac{ab}{\lambda^3} x + 2q(x)r(x)y \quad (18)$$

where $a = C_1 + D_1$, $b = C_1 - D_1$, $\eta = \sqrt{2\pi + q(x)^2}$.

Applying the interval of integration for both $x$-direction and $y$-direction, the expression of the drain current is obtained. (Here the width of the device is considered to be 1 $\mu$m and the parameter D is considered to be 2 for the direct tunneling process).

$$I = Aq \int_{x_1}^{x_2} \int_{0}^{l_0} \left( \eta + \frac{ab}{\lambda^3} x + 2q(x)r(x)y \right) E_g \frac{q_x}{q} \exp \left( -\frac{qB}{E_g} x \right) dx dy \quad (19)$$

After calculating the integration rearranging, the drain current for the RFET is finally obtained

$$I = Aq \left\{ \left[ \frac{E_g \eta S_i q}{q} + \frac{q(x)r(x)q^2}{\eta q} \right] [\xi(x_2) - \xi(x_1)] \right.$$  

$$- \frac{ab\eta S_i}{\lambda^3 q^2 \eta B} [\xi(x_2) - \xi(x_1)] \right\} \quad (20)$$

where $\xi(x)$ and $\eta(x)$ are given by

$$\xi(x) = \ln |x| + \sum_{i=1}^{\infty} \left( -\frac{qB}{E_g} x \right)^i \quad (21a)$$

$$\eta(x) = \exp \left( -\frac{qB}{E_g} x \right) \quad (21b)$$

In equation (20), the parameters a and b explicitly contain the drain voltage $V_d$, the source voltage $V_s$, and the gate voltages, which shows the explicit nature of this model.

The transfer characteristic ($I_d - V_g$) characteristics of the RFETs are plotted in Fig. 7 with different channel doping concentrations. For the band to band tunneling, the value of drain current depends on the tunneling probability of carriers. When the applied voltage ($V_{g1}$) increases, the electric field intensity in the barrier area increases, which shortens the tunnel length. Thus, the carriers are more likely to tunnel. As a result, the current becomes larger. When $V_{g1}$ is small, the electric field in the barrier area under different channel doping concentrations is considered to be approximately equal, which leads to almost the same $I_{OFF}$. For a given voltage that is large enough, the RFET with high channel doping concentration has higher electric field intensity in the barrier area, which makes carriers tunnel more easily. As a result, higher channel doping concentration leads to larger saturation current.

From Fig. 8, the transfer characteristic curves of the RFET at different temperatures are depicted. As the temperature rises, the energy of the carrier increases, so the probability of tunneling increases. When $V_{g1}$ is small, the tunneling of carriers largely depends on temperature, and thus the leakage current increases accordingly with temperature.

As the gate voltage goes up, the electric field intensity in the barrier area gradually plays a leading role. When the voltage rises to a certain value, the impact of the evaluated temperature is weakened, and the drain current is mainly determined by gate voltage. In this case, the electric field intensity generated by the voltage ($V_{g1}$) in the barrier region is the same even at different temperatures, which means that the carriers have almost the same probability to tunnel. Thus, as the gate voltage is high enough, the change
of drain current at different temperatures tends to be small. In the calculation processes mentioned above, the Fermi level \( E_{\text{Source}} \) strongly depends on the value of temperature, so parameter \( 4 \) is influenced by the temperature. As a result, the impact of temperature on the drain current is very significant.

The output characteristics curves of the RFET are shown in Fig. 9. It also shows that the model is in good agreement with TCAD simulations for both n- and p-type RFET.

**IV. RFET-BASED LOGIC GATE CIRCUITS**

As the polarity gate and control gate are located at two Schottky junctions of the RFETs, it has the potential for high-density integration and low cost, which are suitable for future applications in large-scale integrated circuits.

For circuit validation, the proposed model is implemented in Verilog-A. Here, an RFET-based inverter logic gate circuit is simulated by Cadence Virtuoso. To form an inverter, two RFETs are connected in series between the supply and ground, and the value of the capacitance is 10 fF, as shown in Fig. 10. One is biased at n-type and the other is biased at p-type. Fig. 11 plots the transient simulation result of an inverter. It can be seen that the proposed INV performs the function successfully. Besides, it shows fast switching speed and full swing output, which performs better performance than conventional CMOS logic operations.

**V. CONCLUSION**

In this paper, we have presented a compact physics-based model for the surface potential, charge density and drain current of the reconfigurable field-effect transistors (RFETs). The model shows excellent agreement with TCAD simulation data over broad bias. Finally, RFET-based circuit simulation is performed in Verilog-A, which demonstrates that the proposed model is suitable to be a SPICE compatible model.

**APPENDIX**

For equation (16), the total electric field intensity is equal to the vector sum of the transverse and vertical electric fields, which means \( E = \sqrt{E_x^2 + E_y^2} \). The relationship between the electric field and the potential in the tunneling region is obtained as

\[
E_x = -\frac{\partial}{\partial x} \varphi_1(x) = -\frac{1}{\lambda} C_1 \exp\left(\frac{x}{\lambda}\right) + \frac{1}{\lambda} D_1 \exp\left(-\frac{x}{\lambda}\right) \quad (S1)
\]

\[
E_y = -\frac{\partial}{\partial y} \varphi_{1/2}(x, y) = -q(x) + 2r(x)y \quad (S2)
\]
where $E_x$ and $E_y$ are the transverse electric field and vertical electric field respectively. Substitute them into equation $E = \sqrt{E_x^2 + E_y^2}$, equation (17) can be obtained.

The Taylor expansion applied to equation (17) is shown below. By applying unary Taylor expansion to the $E_x$, $E_y$ can be expressed as

$$E_x = -\frac{1}{\lambda} [C_1 - D_1 + \frac{1}{\lambda} (C_1 + D_1)x + \frac{1}{2\lambda^2} (C_1 - D_1)x^2]$$

(S3)

Assuming $C_1 - D_1 = b$ and $C_1 + D_1 = a$, the total electric field can be obtained.

$$E = \sqrt{\left(\frac{1}{\lambda}(b + ax + \frac{b}{2\lambda^2}x^2)\right)^2 + \left[q(x) + 2r(x)y\right]^2}$$

(S4)

In order to simplify the calculation, the coefficient $-1$ is ignored here. Next, the computational process of binary Taylor expansion is shown below.

$$E_{\mid(0,0)} = \frac{b^2}{\lambda^2} + q(x)^2$$

(S5)

$$\frac{\partial E}{\partial x} \mid_{(0,0)} = \frac{ab}{\lambda^3} \sqrt{\frac{b^2}{\lambda^2} + q(x)^2}$$

$$\frac{\partial E}{\partial y} \mid_{(0,0)} = \frac{2q(x)r(x)}{\sqrt{\frac{b^2}{\lambda^2} + q(x)^2}}$$

$$E = E_{\mid(0,0)} + \frac{\partial E}{\partial x} \mid_{(0,0)} x + \frac{\partial E}{\partial y} \mid_{(0,0)} y$$

$$= \frac{b^2}{\lambda^2} + q(x)^2 + \frac{ab}{\lambda^3} x + 2q(x)r(x)y$$

(S6)

Equation (17) is obtained.

To prove the validity of the integration mentioned in equation (20), we will provide a detailed integral process in this section.

$$I = Aq \int_0^{\eta E_g} \frac{\eta E_g}{q} \left[ \frac{qB}{E_g} \exp(-\frac{qB}{E_g}x) + \frac{abE_g^2}{\lambda^3 q^2} \exp(-\frac{qB}{E_g}x) \right] dx$$

$$+ \frac{2p(x)q(y)E_g y}{\eta q x} \exp(-\frac{qB}{E_g}y) dx$$

(S7)

$$I = Aq \int_0^{\eta E_g} \left( \frac{\eta E_g}{q} + \frac{2p(x)q(y)E_g y}{\eta q x} \right) \cdot \int_{x_1}^{x_2} \exp(-\frac{qB}{E_g}x) dx$$

$$+ \frac{abE_g^2}{\lambda^3 q^2} \left[ \exp(-\frac{qB}{E_g}x_2) - \exp(-\frac{qB}{E_g}x_1) \right]$$

(S8)

After integrating the variable $y$, the integration can be expressed as

$$I = Aq \left\{ \left[ \frac{E_g \eta \xi q}{q} + \frac{q(x)r(x)y^2}{\eta q} \right] \cdot \int_{x_1}^{x_2} \frac{1}{x} \left\{ \exp(-\frac{qB}{E_g}x) \right\} dx \right\}$$

(S9)

by using some approximations, it can be calculated that

$$\int_{x_1}^{x_2} \frac{1}{x} \exp(ax) dx = \ln|x_1| + \sum_{i=1}^{\infty} \frac{(ax)^i}{i!} - \ln|x_2| - \sum_{i=1}^{\infty} \frac{(ax)^i}{i!}$$

(S10)

Now equation (20) can be obtained.

REFERENCES

[1] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, “Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs,” in IEDM Tech. Dig., Dec. 2012, pp. 8.4.1–8.4.4.

[2] M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick, and A. Kumar, “Designing efficient circuits based on runtime-reconfigurable field-effect transistors,” IEEE Electron Device Lett., vol. 35, no. 8, pp. 880–882, Aug. 2014.

[3] W. M. Weber, A. Heinzig, J. Trommer, M. Grube, F. Kreupl, and T. Mikolajick, “Reconfigurable nanowire electronics-enabling a single CMOS circuit technology,” IEEE Trans. Nanootechnol., vol. 13, no. 6, pp. 1020–1028, Nov. 2014.

[4] J. Trommer, A. Heinzig, S. Slesarek, T. Mikolajick, and W. M. Weber, “Elementary aspects for circuit implementation of reconfigurable nanowire transistors,” IEEE Electron Device Lett., vol. 35, no. 1, pp. 141–143, Jan. 2014.

[5] J. Zhang, X. Tang, P.-E. Gaillardon, and G. De Micheli, “Reconfigurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 10, pp. 2851–2861, Oct. 2014.

[6] D. Martin, A. Heinzig, M. Grube, L. Geelhaar, T. Mikolajick, H. Riechert, and W. M. Weber, “Direct probing of Schottky barriers in Si nanowire Schottky barrier field effect transistors,” Phys. Rev. Lett., vol. 107, no. 21, p. 216807, Nov. 2011.

[7] C. Pan, C.-Y. Wang, S.-J. Liang, Y. Wang, T. Cao, P. Wang, C. Wang, S. Wang, B. Cheng, A. Gao, E. Liu, K. Watanabe, T. Taniguchi, and F. Miao, “Reconfigurable logic and neuronorphic circuits based on electrically tunable two-dimensional homojunctions,” Nature Electron., vol. 3, no. 7, pp. 383–390, Jun. 2020.

[8] H. Yoo, M. Ghittorelli, E. C. P. Smits, G. H. Gelinck, H.-K. Lee, F. Torricelli, and J.-J. Kim, “Reconfigurable complementary logic circuits with ambipolar organic transistors,” Sci. Rep., vol. 6, no. 1, pp. 1–11, Oct. 2016.

[9] A. Bhattacharjee and S. Dasgupta, “Impact of gate/spacer-channel underlap, gate oxide EOT, and scaling on the device characteristics of a DG-RFET,” IEEE Trans. Electron Devices, vol. 64, no. 8, pp. 3063–3070, Aug. 2017.

[10] A. Bhattacharjee, M. Saikiran, A. Dutta, B. Anand, and S. Dasgupta, “Spacer engineering-based high-performance reconfigurable FET with low OFF current characteristics,” IEEE Electron Device Lett., vol. 36, no. 5, pp. 520–522, May 2015.

[11] S. Rai, J. Trommer, M. Raitza, T. Mikolajick, W. M. Weber, and A. Kumar, “Designing efficient circuits based on runtime-reconfigurable field-effect transistors,” IEEE Trans. Very Large Scale Inte (VLSI) Syst., vol. 27, no. 3, pp. 560–572, Mar. 2019.

[12] M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick, and W. M. Weber, “Top-down fabricated reconfigurable FET with two symmetric and high-current on-states,” IEEE Electron Device Lett., vol. 41, no. 7, pp. 1110–1113, Jul. 2020.

[13] J.-H. Lee, “Reconfigurable field-effect transistor as a synaptic device for analog-based (A-B) digital signal processing,” IEEE Electron Device Lett., vol. 37, no. 1, pp. 23–25, Feb. 2016.

[14] J.-H. Bae, H. Kim, D. Kwon, S. Lim, S.-T. Lee, B.-G. Park, and J.-H. Lee, “Reconfigurable field-effect transistor as a synaptic device for XNOR binary neural network,” IEEE Electron Device Lett., vol. 40, no. 4, pp. 624–627, Apr. 2019.

[15] X. Li, Y. Sun, Z. Liu, X. Li, Y. Shi, T. Wang, and J. Xu, “Analysis of metal work-function modulation effect in reconfigurable field-effect transistor,” IEEE Trans. Electron Devices, vol. 67, no. 9, pp. 3745–3752, Sep. 2020.
A. Bhattacharjee, M. Saikiran, and S. Dasgupta, “A first insight to the thermal dependence of the DC, analog and RF performance of an S/D spacer engineered DG-ambipolar FET,” IEEE Trans. Electron Devices, vol. 64, no. 10, pp. 4327–4334, Oct. 2017.

A. Bhattacharjee and S. Dasgupta, “A compact physics-based surface potential and drain current model for an S/D spacer-based DG-RFET,” IEEE Trans. Electron Devices, vol. 65, no. 2, pp. 448–455, Feb. 2018.

Sentaurus TCAD (Version 2016.03) Manuals, Synopsys Inc., Mountain View, CA, USA, 2016.

G. Darbandy, M. Claus, and M. Schroter, “High-performance reconfigurable Si nanowire field-effect transistor based on simplified device design,” IEEE Trans. Nanotechnol., vol. 15, no. 2, pp. 289–294, Mar. 2016.

R.-H. Yan, A. Ourmazd, and K. F. Lee, “Scaling the Si MOSFET: From bulk to SOI to bulk,” IEEE Trans. Electron Devices, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

E. O. Kane, “Theory of tunneling,” J. Appl. Phys., vol. 32, no. 1, pp. 83–91, 1961.

M. Gholizadeh and S. E. Hosseini, “A 2-D analytical model for double-gate tunnel FETs,” IEEE Trans. Electron Devices, vol. 61, no. 5, pp. 1494–1500, May 2014.

N. Bagga and S. Dasgupta, “Surface potential and drain current analytical model of gate all around triple metal TFET,” IEEE Trans. Electron Devices, vol. 64, no. 2, pp. 606–613, Feb. 2017.

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