Implementation of Chua’s chaotic oscillator with an HP memristor

Muratkhan Abdirash, Irina Dolzhikova, Student Member, IEEE, Alex Pappachen James, Senior Member, IEEE, Electrical and Computer Engineering Department, Nazarbayev University, Astana, Kazakhstan

Abstract—This paper proposes an innovative chaotic circuit based on Chua’s oscillator. It combines traditional realization of a non-linear resistor in Chua’s chaotic oscillator with a promising memristive circuitry. This mixed implementation connects old research works that were focused on diodes with relatively new research papers that are, now, concentrated on memristors. As a result, more reliable chaotic circuit with an HP memristor is obtained that could be used as a source of randomness. Dynamic behavior of the circuit is studied by obtaining fft analysis, different chaotic attractors and Lyapunov exponent spectrum. The results show that the addition of a memristor enhances chaotic behavior of the circuit while maintaining the same power dissipation.

Index Terms—HP memristor, Chua’s chaotic circuit, chaotic attractor, non-linear resistor.

I. INTRODUCTION

Memristor as a concept was introduced in 1971 by Leon Chua. He entitled memristor as ”the missing fourth element”, considering it as one of the basic circuit components along with a resistor, capacitor and an inductor. It was stated that a memristor would link charge with flux, completing the symmetrical dependence between the four fundamental variables of any electrical circuit: current, voltage, charge and flux.

However, the existence of a memristor was questionable until 2008. Only at that time, laboratories at Hewlett-Packard (HP) were finally able to experimentally demonstrate a working memristor.

After this discovery, memristors have become one of the most heavily researched topics across the world. This is, mainly, because a memristor has two main characteristics that make it extremely attractive for scholars. First, its ability to function as a memory device, which potentially can revolutionize IC industry. Second, its ability to function as a non-linear memristor. This property would be the main focus of the paper - utilizing memristor’s non-linear behavior to create chaotic circuits.

Chaotic circuits containing memristors are not something new; there have already been plenty of research on this topic. For example, in source a memristor, modeled with quadratic I-V characteristics, was used in building Chua’s chaotic circuit. A very simple chaotic oscillator was proposed in which a memristor was implemented as an active device connected in series to just an inductor and a capacitor. While in another source, memristor with a cubic I-V dependence model was used as a non-linear element for Chua’s circuit. As it can be seen, several attempts have been made in creating a chaotic circuit with a memristor. One common thing among all these papers is that a memristor was integrated to, specifically, Chua’s chaotic circuit in one way or another. This is, because, firstly, Chua’s circuit is very simple and, secondly, it contains a mandatory non-linear element which is what, essentially, memristor is.

What sets apart this paper from others is that it proposes a circuit that combines two currently most popular non-linear elements, namely an HP memristor and a diode. This combination is special due to two reasons. Firstly, it makes use of two diodes in antiparallel, which have been proven many times as the most traditional and reliable realization of a non-linear element in Chua’s circuit. Secondly, it contains an HP memristor, which is, now, recognized as one of the newest realizations of a non-linear resistor. Moreover, integrating, specifically, an HP memristor, being the first ever physically realizable memristor, adds one more layer to reliability and feasibility of the circuit. It is further strengthened by using a realistic mathematical model of an HP memristor as suggested in source . The proposed circuit exhibits chaotic behavior, whose output signal can then be used to generate random number sequences.

The remainder of this paper is organized in the following way. Section II provides theoretical background about the HP memristor and Chua’s chaotic circuit. The methodology is given in Section III. Section IV demonstrates the results. This is followed by discussion in Section V. Finally, Section VI concludes the paper.

II. BACKGROUND

A. HP Memristor

An HP memristor is a thin film made of TiO$_2$. It is doped with oxygen vacancies and bounded between two platinum plates that act as metal contacts. Its internal structure can be viewed from Fig. 1 as described in . Here, $D$ is a length of the whole memristor and $w$ is a length of the doped region.

Figure 1. Internal Structure of an HP Memristor

Resistances of the doped and undoped regions are known as $R_{OH}$ and $R_{OFF}$, respectively. From this it follows that a...
memristor can be modeled as a series connection of two different resistances. The only complication here is that a length of the doped region changes depending on the amount and direction of the current passing through a memristor. Intuitively, when a positive current keeps on flowing through a device, the doped region expands and, the total resistance decreases. It is the opposite with a negative current resulting in the increase of a total resistance [11]. Mathematical equations describing the behavior of an HP memristor, as taken from source [11] are presented below. First, I-V equation of an HP memristor is given by Eq. 1, where \( w(t) \) is a width function of memristor’s doped region.

\[
v(t) = (R_{on} \frac{w(t)}{D} + R_{off}(1 - \frac{w(t)}{D}))i(t) \quad (1)
\]

Secondly, \( w(t) \) can range from 0 (when the total resistance is \( R_{off} \)) to \( D \) (when the total resistance is \( R_{on} \)), and is related to current through Eq. 2, where \( \eta \) is a polarity and \( \mu_v \) is a mobility of dopants.

\[
w'(t) = \eta \frac{\mu_v R_{on}}{D} i(t) \quad (2)
\]

However, it was discovered that Eq. 1 and Eq. 2 cannot fully describe the operation of an HP memristor. It happens, because a high degree of non-linearity is observed in boundary conditions \( (w \rightarrow 0 \) and \( w \rightarrow D) \), which are far more complicated than Eq. 1 and Eq. 2 [11]. For more comprehensive description of the model, window functions were introduced. In this paper, Biolek window is utilized since it performs better than Joglekar, but is not as complicated as other window functions [11]. Modified Eq. 2 with window function is represented by Eq. 3, where Biolek window is defined by Eq. 4. In Eq. 4, \( stp(i) = 1 \) for \( i > 0 \), and \( stp(i) = 0 \) for \( i < 0 \).

\[
w'(t) = \eta \frac{\mu_v R_{on}}{D} i(t)F\left(\frac{w(t)}{D}\right)i(t), \quad (3)
\]

\[
F_B(x, i, p) = 1 - (x - stp(-i))^2p, \quad (4)
\]

B. Chua’s Chaotic Circuit

Chua’s oscillator is the simplest circuit that can generate chaos [10]. It is demonstrated on Fig. 2 and, it is, indeed, very simple comprising of only five elements in total: two capacitors, one inductor, one resistor and a non-linear active resistor.

Yet it is considered as a very powerful circuit that defines and sets chaotic requirements for all the other complex circuits out there. Moreover, Chua’s circuit is autonomous, meaning that it produces a time-varying output without a time-varying input [10]. Having all these characteristics it establishes necessary conditions for a certain circuit to exhibit chaos it should have, at least 3 storage elements, one active local resistor and a non-linear resistor.

Output of any circuit based on Chua’s oscillator should satisfy two conditions to be recognized as chaotic [10]:

1) Circuit variables (current and voltage) as measured from any node of the circuit should be chaotic and random. In other words, time plots of variables should look like a noisy signal.

2) Chaotic attractors (plot of voltage across one capacitor versus voltage across another) should be shaped as a double scroll or come close to it.

III. METHODOLOGY

A. Analysis of traditional design of Chua’s circuit

A lot of sources refer to diode implementation of Chua’s circuit as the most popular one. For this reason, investigating how that circuit operates would be a good starting point toward the final design. It was, indeed, beneficial since the proposed circuit is, essentially, based on that classical model with diodes. Simulation files of Chua’s circuit with diodes on LTspice were available on this open source [13].

The most important component in traditional Chua’s circuit is a non-linear resistor implemented as two antiparallel diodes. This is because, ideally, memristor should be able to either replace or enhance those diodes and produce equally, if not more, random signal. To find out how exactly those diodes contribute to the overall chaotic behavior, DC sweep analysis on LTspice was performed. The circuit for DC sweep can be found in the appendix.

After running the test circuit, I-V curve of the diodes was obtained (Fig. 3). It perfectly matches what is described in many sources including [10], which call this type of non-linear IV relationship as piecewise linear. The two branches with positive slope on the right and left can be ignored right...
now for the purpose of the analysis. The middle part of the curve in Fig. 3 comprises of three line segments with different negative slopes. The negative slopes are coming from a negative impedance op amp attached in parallel to the diodes, so that in combination they function as one locally active non-linear resistor. This I-V curve demonstrates a very simple way to achieve a non-linear relationship, just by changing the slopes of a straight line. Obviously, there are other ways to achieve that - quadratic, cubic, etc.

There is one more condition to obtain chaos - specific values of $R$, $L$ and $C$ parameters in the circuit. Slight changes in the values of these parameters may cause chaotic circuit to behave as a periodic oscillator [10].

B. Integrating an HP memristor to Chua’s chaotic oscillator

LTspice model for an HP memristor with Biolek window was downloaded from [?]. The first attempt at including a memristor to the circuit was by replacing one of the diodes in antiparallel. After removing the diode, adding an HP memristor and choosing appropriate values for $R$, $L$ and $C$ parameters, simulation was run. However, the output chaotic signal was decaying too fast compared to the original circuit. In other words, it produced a transient chaotic signal for a relatively short period of time. That is why, it was decided to keep the both diodes.

Finally, the proposed circuit’s schematic can be viewed in Fig. 4. There are three components that make the non-linear resistor for Chua’s chaotic oscillator in the final design of the circuit: two diodes in antiparallel connected to an HP memristor in parallel. To confirm that the proposed circuit functions as desired, i.e. produces chaotic signals, several analysis were performed.

First of all, the output random signal of the new circuit is shown in Fig. 5 for 90 ms of the simulation, performed using a transient analysis in LTspice. The signal is taken as the voltage across capacitor $C_2$. Visually, it is reassuring that $V_{out}$ is, indeed, random, since it behaves like a very noisy signal with no pattern whatsoever.

Secondly, IV curve of these complex non-linear elements was obtained using DC sweep analysis in LTspice. The result is shown in Fig. 6 and, it can be seen that an IV curve is, in fact, non-linear having different slopes and even greater number of slopes than the original circuit. This indicates how the addition of the memristor has enhanced the overall non-linearity of the circuit.

Thirdly, to prove the output signal’s randomness or noisiness, FFT analysis was done. The results are presented in Fig. 7. As expected, there are a lot of frequency components with different amplitudes, which is exactly what is required from a random signal.

The next checking point was to plot the chaotic attractor of the system. As it was mentioned earlier, chaotic system should have an attractor shaped like a double scroll. Chaotic attractor is plotted as one circuit variable against another. In this case, voltage across capacitor $C_2$ was plotted against the current in the inductor $L_1$. It is shown in Fig. 8 and, it is shaped as a double scroll and satisfies the condition for chaotic system.

Lastly, to make sure, that randomness is coming from both diodes and memristor, the currents in each component are shown in Fig. 9. It is clear, that each component is equally contributing to the randomness.
IV. Results

A. Derivation of differential equations governing the circuit

To study the dynamics of Chua’s circuit, one must derive the differential equations governing the behavior of that circuit. Here, dynamics means the response of the circuit under changing parameter values. Obviously, parameters refer to R, L and C values integrated to the circuit. The process of deriving those equations is described in source [10] and all the proceeding equations are based on that.

1) I-V Mathematical Relationship: I-V curve of the non-linear element of the proposed circuit is presented in Fig. 6. As it can be seen, there are four regions with different negative slopes in the I-V graph.

2) Slope 1: Point 2: (-6.1799 V, 3.2334 mA); Point 1: (-1.2700 V, 0.9300 mA);
   \[ A = \frac{(3.2334 - 0.9300) \times 10^{-3}}{-6.1793 + 1.2700} = -0.4691 mS \]

3) Slope 2: Point 2: (-1.2700 V, 0.9300 mA); Point 1: (0 V, 0 mA);
   \[ B = \frac{(0.9300 - 0) \times 10^{-3}}{-1.2700 - 0} = -0.7323 mS \]

4) Slope 3: Point 2: (0 V, 0 mA); Point 1: (1.2300 V, -1.1500 mA);
   \[ C = \frac{(0 + 1.1500) \times 10^{-3}}{0 - 1.2300} = -0.9350 mS \]

5) Slope 4: Point 2: (1.2300 V, -1.1500 mA); Point 1: (6.1820 V, -4.4850 mA);
   \[ D = \frac{(-1.1500 + 4.4850) \times 10^{-3}}{1.2300 - 6.1820} = -0.6735 mS \]

6) I-V Equation: It is clear from Fig. 6 that I-V relationship is piece-wise linear and, equation will be in accordance to that (only considering negative slopes of the graphs):

   \[ i_R = \begin{cases} 
   \frac{A v_R - 1.27(A - B)}{C}, & v_R \leq -1.27 \\
   \frac{B v_R}{C}, & -1.27 \leq v_R \leq 0 \\
   \frac{C v_R}{C}, & 0 \leq v_R \leq 1.23 \\
   \frac{D v_R + 1.23(C - D)}{D}, & v_R \geq 1.23 
   \end{cases} \] (5)

where \( i_R \) and \( v_R \) are the current in and the voltage across the non-linear element, respectively. Meanwhile, \( A, B, C \) and \( D \) are the slopes of the I-V curve.

7) Differential Equations: Following the guidelines from source [10]: let us indicate as \( v_1, v_2 \) and \( i_L \) the voltage across capacitor C1, the voltage across capacitor C2 and the current in the inductor L, respectively. By applying the Kirchhoff’s circuit laws and considering I-V dependence formulas for a capacitor and an inductor, the state equations can be derived as follows:

   \[ \frac{dv_1}{dt} = \frac{1}{C_1} \left( \frac{v_2 - v_1}{R} - i_R \right) \] (6)

   \[ \frac{dv_2}{dt} = \frac{1}{C_2} \left( \frac{v_1 - v_2}{R} + i_L \right) \] (7)

   \[ \frac{di_L}{dt} = -\frac{1}{L} v_2 \] (8)
B. Lyapunov Exponents

To experimentally verify chaos, the Lyapunov exponents should be calculated. This type of exponents may be computed using the time series method as suggested by [9]. There can be several Lyapunov exponents and, as long as any of them is positive, the system is said to be chaotic [9].

Prior to obtaining the Lyapunov exponents, all of the differential equations describing the system are scaled by \( \sqrt{L_1C_2} \). It is required since the Lyapunov exponent algorithms numerically converge for, particularly, these time factors. At lower time constant coefficients, very small step sizes are needed to solve the differential equations, which, in turn, leads to unnecessary computing complications. It does not only take a lot of time, but sometimes may result in considerable errors [9].

![Figure 10. Dynamics of Lyapunov exponents](image)

The result is shown in Fig. [10] where the red curve corresponds to the largest Lyapunov exponent. This line is above the x-axis for almost 1.7 time series simulation, meaning it is positive for just enough time. Referring back to the first paragraph in this section, the condition for chaos is satisfied.

C. Power Calculations

Since both the current in the inductor and the voltage across it are random, their product, i.e. power, is also random. To resolve this issue, average of all the instantaneous power values during 300 ms will be referred as "power absorbed by a particular element". It should be noted that the average value would still vary depending on the duration of the simulation. Very small negative power shows that inductor does not consume much of the energy and, thus, is not an issue from a power perspective.

Table I demonstrates the summary of the power consumed be the proposed and original Chua’s circuit. Total power consumed by the proposed circuit during 300 ms of simulation is, then, 42.5781 mW. As it can be seen from the results, the most power is absorbed by the negative resistor components, which is constructed using Opamp. Consumption by energy storage elements, not including resistor \( R_8 \), is so negligible that can be ignored. They do not present a problem from a power perspective for, particularly, this circuit, although they usually take up a lot of area in a chip.

Original circuit differs from the proposed circuit in the following way:

1) It has a memristor in-between the diodes to enhance the non-linearity and, hence, the overall randomness;
2) The parameter values (\( C_1, C_2, L_1, \) etc.) differ.

If the results are to be compared, the total power absorbed by the original circuit is greater by 0.8459 mW. This means that the proposed circuit with an HP memristor is 1.95 per cent more efficient than the original circuit in terms of the power consumption. Even if it is a small difference, it can be stated that the proposed circuit outperforms the original one.

V. Discussion

Simulation results confirm that the proposed circuit is, indeed, giving a random output signal as expected. FFT analysis show that there are many frequency components with different amplitudes in the output signal. This randomness is, essentially, coming from transient behavior of the circuit. Double scroll chaotic attractor also confirms that the system’s behavior is chaotic. However, to further study the dynamics of the circuit, Bifurcation diagrams should be constructed, which also help to determine at what exact values circuit becomes chaotic.

VI. Conclusion

This paper has suggested one way of making a chaotic random number generator with an HP memristor. The proposed circuit was based on the classical implementation of Chua’s circuit - two diodes as a non-linear element. It kept both of the diodes and integrated an HP memristor. As a result, it was able to maintain chaos and randomness exhibited by the circuit. This is what makes it special: mixing a classical implementation (diodes) of a non-linear element with a modern one (memristor). Since the circuit generates chaotic random signal, its output, potentially, can be used in applications such as image encryptions, secret communications and other various information safeties.

There are two future suggestions:

1) The output signal of the circuit decays as time passes and loses its randomness. This should be fixed, since ideally the circuit should remain chaotic forever;
2) Statistical tests should be conducted on the values of obtained random output signal to ensure that the circuit can be used in security applications.
REFERENCES

[1] L. Chua, Memristor—The missing circuit element, IEEE Transactions on Circuit Theory: vol. 18, num. 5, September 1971.
[2] D.B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, The missing memristor found, Nature Publishing Group, vol. 453, num. 7191, p.80, 2008.
[3] L. Chua, The fourth element in Memristor Networks. Springer p.1-13, 2014.
[4] A. James, Memristor and Memristive Neural Networks, Intech, 2018, DOI: 10.5772/6653.
[5] A. Irmanova and A. P. James, Multi-level Memristive Memory with Resistive Networks, arXiv preprint arXiv:1709.04149, 2017.
[6] A. Irmanova and A. P. James, Neuron inspired data encoding memristive multi-level memory cell, Analog Integrated Circuits and Signal Processing, Springer, p.1-6, 2018.
[7] M. Inoh and L. Chua, Memristor oscillators, International Journal of Bifurcation and Chaos, World Scientific, v.18, num.11, p.3183-3206, 2008.
[8] P. Jin, G. Wang, Guangyi and S. Jiang, Design of PN sequence generator based on memristor oscillator, 2015 IEEE 16th International Conference on Communication Technology (ICCT), IEEE, p.51-55, 2015.
[9] B. Muthuswamy, Implementing memristor based chaotic circuits, International Journal of Bifurcation and Chaos, World Scientific, v.20, num. 05, p.1335-1350, 2010.
[10] F. Luigi, and F. Mattia, and Gabriella, M. Xibilia, Chua’s Circuit Implementations: Yesterday, Today And Tomorrow, World Scientific, v.65, 2009.
[11] A. Buscarino, and L. Fortuna, and F. Mattia Frasca and L. V. Gambuzza A chaotic circuit based on Hewlett-Packard memristor, Chaos: An Interdisciplinary Journal of Nonlinear Science, v.22, nu. 2, 023136 2012.
[12] G. Wang, and S. Zang, and X. Wang, and F. Yuan and H. H.-C. Iu Memcapacitor model and its application in chaotic oscillator with memristor, Chaos: An Interdisciplinary Journal of Nonlinear Science, v.27, nu. 1, 013110 2017.
[13] Jim, SIMULATING CHUA’S CIRCUIT WITH LTSPICE, [Online] Available: urlhttp://www.chaotic-circuits.com February 2018.
[14] T. Michea, nowm/memristor-models-4-all, [Online] Available: urlhttps://github.com/knowm/memristor-models-4-all February 2018.