A 0.6 V temperature-stable CMOS voltage reference circuit with sub-threshold voltage compensation technique

Zhikuang Cai¹,² and Chao Chen²a)
¹ College of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China
² National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China
a) ccnavy@163.com

Abstract: This paper presents a CMOS reference circuit which can work properly under the near-threshold voltage of 0.6 V. It is based on the temperature characteristic of NMOS&PMOS transistors in the sub-threshold region. The temperature curve of the NMOS quasi-PTAT current and the PMOS quasi-PTAT current can be adjusted to have the same slope factor. Thus a temperature-stable reference voltage can be achieved by subtracting the quasi-PTAT voltage generated by the NMOS and PMOS circuits. It can be used under the supply voltage of 0.6 V, under which a traditional bipolar-based band gap reference cannot work properly. The circuit is designed and implemented in SMIC 65 nm CMOS process. It provides a nominal reference voltage of 154 mV, a average temperature coefficient of 87 ppm/°C in [−10°C~80°C] under a 0.6 V supply voltage. The total power consumption is 60 µW and the chip area is 345 um * 182 um.

Keywords: reference circuit, near-threshold, low-supply voltage

Classification: Integrated circuits

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1 Introduction

The reference circuit is one of the most fundamental building blocks in analog circuits. CMOS technology has developed rapidly into a new era of high integration and ultra-low power consumption. In order to reduce power consumption, reducing supply voltage is one of the direct approaches. Some of the studies predict that the supply voltage of RF and analog circuits will drop to 0.5 V–0.7 V in the future. However, with the limit of the semiconductor process and the leakage current, the threshold voltage of CMOS transistors maintains above 350 mV, which brings a great challenge to the design of RF and analog circuits under low voltage.

The traditional reference circuit is the bandgap reference structure [1]. The basic principle is to use the negative temperature characteristics of the bipolar device PN junction to neutralize with the positive temperature characteristic of the voltage difference between two PN junctions. However, in the application of the near threshold voltage of 0.6 V, which is below the normal voltage drop of the PN junction, the traditional bipolar bandgap reference circuit is no longer suitable. This letter proposes a CMOS reference circuit working in 0.6 V supply voltage and covers −10°C–80°C temperature range in 65 nm SMIC CMOS technology. The temperature-stable reference voltage is realized by subtracting the quasi-PTAT voltage generated by the NMOS and PMOS circuits.
2 Circuit design

The proposed reference uses the temperature characteristics of CMOS transistors in sub-threshold region as the temperature elements. In the conventional bandgap reference circuits, the PTAT current is generated by collecting the difference of VBE between two bipolar devices [2, 3, 4, 5, 6]. The temperature coefficient of the difference of VBE is proportional to the temperature. The voltage can be converted to PTAT current through the resistor. It is noted that, the characteristic of the MOS transistors working in the sub-threshold region are similar to the characteristic of the bipolar devices. As a result, the PTAT current can also be generated in CMOS circuit.

The NMOS PTAT current the PMOS PTAT current are generated respectively as shown in Fig. 1, (a) is the circuit of NMOS PTAT current and (b) is the circuit of PMOS PTAT current. P1, N1, P21 and P4, N4, P22 are the start-up circuits of NMOS PTAT current circuit and PMOS PTAT current circuit respectively.

![Circuit diagram](image)

**Fig. 1.** The circuits of NMOS PTAT current and PMOS PTAT current

The start-up circuits are used for avoiding the deadlock situation after power on. Take the NMOS PTAT current circuit as an example. On the early time when the circuit is powered on, the VGS of N1 is zero. The transistor P21 is on and will pull down the gate voltage of the transistor P2 and P3, the PTAT current begins to establish. At the end of the setting process, the gate voltage of N1 is high and P21 will cut off. At this time, the current extracted from the PTAT current is zero. As a result it does not affect the normal operation of the circuit.

In Fig. 1. (a), transistors N2, N3 work in the sub-threshold region. The width to length ratio of N2 is K times of N3. The gate of N2 and N3 are connected together, there is a resistor R1 connected between the source of N2 and the ground. PMOS transistors P2 and P3 compose the current mirror to make sure that the currents of N2 and N3 are the same. As a result, the NMOS PTAT current is constant. The current of N2 and N3 is indicated by eq. (1).

\[
I_{D2} = \left( \frac{W}{L} \right)_2 I_{D0} \exp \left( \frac{V_{GS2}}{\sqrt{V_T}} \right) \\
I_{D3} = \left( \frac{W}{L} \right)_3 I_{D0} \exp \left( \frac{V_{GS3}}{\sqrt{V_T}} \right)
\]  

(1)
In which, \((W/L)\) is the width to length ratio of the transistor, \(ID0\) is related to the process, \(Vgs\) is the gate to source voltage of the transistor, \(\xi\) is the sub-threshold slope factor, \(VT\) is the thermal voltage.

The current mirror P2 and P3 makes \(ID2 = ID3\). Considering \(Vgs2 + VR1 = Vgs3\), the current of resistor \(R1\) can be expressed by eq. (2).

\[
I_{R1} = \frac{(V_{gs3} - V_{gs2})}{R1} = \xi V_T \left( \ln \left( \frac{ID3}{(W/L)3ID0} \right) - \ln \left( \frac{ID2}{(W/L)2ID0} \right) \right)
\]

\[
= \xi V_T \left( \ln \left( \frac{(W/L)2}{(W/L)3} \right) \right) = \xi V_T \ln(K)
\]  

(2)

From eq. (2), it is obvious that the current is proportional to the temperature. The slope of the current curve with temperature variation can be adjusted by the width to length ratio.

Adopting the same method, the PMOS PTAT current can also be derived as eq. (3):

\[
I_{R2} = \frac{(V_{gs6} - V_{gs5})}{R1} = \xi' V_T \left( \ln \left( \frac{ID6}{(W/L)6ID0} \right) - \ln \left( \frac{ID5}{(W/L)5ID0} \right) \right)
\]

\[
= \xi' V_T \left( \ln \left( \frac{(W/L)5}{(W/L)6} \right) \right) = \xi' V_T \ln(K')
\]  

(3)

By adjusting the width to length ratio of the transistors and the current copy ratio, the temperature curves of the NMOS PTAT current and the PMOS PTAT current can eventually have the approximation slope. These two PTAT currents can be subtracted and converted into a reference voltage through a resistor with low temperature coefficient. The positive temperature coefficient can be compensated and the subtracted current is with low temperature coefficient.

The simulation result of the temperature characteristic curve of the output voltage reference is shown in Fig. 2. The slope of the NMOS and the PMOS PTAT current are approximately equal. As can be seen from the figure, the whole curve has the temperature characteristic of the first order compensation and shows the shape of a parabola.

The overall circuit schematic is shown in Fig. 3, including the start-up circuit and the reference core. As can be seen in the main circuit, only two transistors are stacked at most, so the circuit can operate normally under the 0.6 V power supply voltage which is near the threshold.
Resistor R1, NMOS transistors N2, N3 and the PMOS transistors P2, P3 compose the NMOS PTAT current generating circuit. The resistor R2, PMOS transistors P5, P6 and NMOS transistors N5, N6 compose the PMOS PTAT current generating circuit. The two PTAT current are subtracted through current subtraction circuit composed by P7, N7, P8. The subtracted current is converted to the reference voltage with the help of resistor R4 and the temperature coefficient introduced by the resistor previously is neutralized.

![Circuit schematic of the near threshold CMOS current/voltage reference.](image)

The current reference generating circuit is composed of the low-voltage master-slave error amplifier A1 [7], the PMOS transistor P17, the off-chip resistor Rs and the series RC network R3 and C1. The output of the error amplifier is connected to the gate of P17. In the case of the negative feedback loop, combined with the high loop gain, the voltage of the resistor Rs can be equal to the output reference voltage by adjusting the current of P17. The off-chip resistor Rs is the film resistor with low temperature coefficient. So the temperature coefficient of the current through Rs is determined by the output reference voltage. It can be approximated as a constant current source.

### 3 Measurement results

The proposed CMOS reference circuit near the sub-threshold region is designed and fabricated in SMIC 65 nm CMOS process. The temperature is measured from −10°C to 80°C, the maximum range of variation of the output voltage is less than 1 mV.

Fig. 4 shows the micro-photograph of the proposed reference. The chip area of the reference circuit is 345 μm * 182 μm. The total power consumption is 60 μW. The measurement result of the reference voltage versus temperature is shown in Fig. 5. The variation of the reference voltage in [−10°C~80°C] is only 1 mV. Fig. 6 shows the measured reference current generated by the core voltage and the OTA based buffer. The peak of the current curve versus temperature is not at 45 degree, which is different from the voltage curve. The reason might be that the systematic offset of the OTA which is used to perform the V-I conversion varies with the temperature. Fig. 7 illustrates the measured PSRR versus frequency. The PSRR is
below $-35$ dB at 100 Hz. The loop gain in the circuit decreases with frequency and cause the degradation of the PSRR. At high frequencies, the decoupling capacitors help to filter out the output fluctuations caused by the supply voltage and pull down the PSRR to below $-30$ dB at frequencies above 100 MHz.

Table I compares important design parameters and performance of some previous works found in the literature [8, 9, 10, 11, 12, 13]. Limited by the supply voltage, most of the works use sub-threshold characteristic to compensate the temperature coefficient. The supply voltage of this work is much lower than [8, 9, 10, 11]. Meanwhile, a balanced temperature coefficient is achieved. Reference [12]
presents an excellent reference circuit with ultra-low temperature coefficient. Reference [13] realizes the lowest supply voltage while this work is better at temperature coefficient.

Table I. Comparison with other designs

| Technology (µm) | [8] | [9] | [10] | [11] | [12] | [13] | This work |
|----------------|-----|-----|------|------|------|------|-----------|
| Architecture   | Sub-BG Vth Vth Sub-threshold Sub-threshold Sub-threshold Sub-threshold |
| Supply Voltage (V) | 1.1–3.3 | 1 | 0.95 | 1.5 | 0.6 | 0.45 | 0.6 |
| TC (ppm/°C)     | 394 | 238 | 39 | 11.5 | 2.5 | 142 | 87 |
| Temp. range (°C) | –20–80 | –40–120 | –20–80 | –20–120 | –20–80 | 0–125 | –10–80 |

4 Conclusion

A CMOS reference circuit that can work properly near the threshold supply voltage 0.6 V is proposed in this paper. It exploits the characteristic of the transistors working in the sub-threshold region. The output current reference has low temperature coefficient. The output voltage reference can be adjusted by the off-chip resistor which is a film resistor with low temperature coefficient. The simulation results show that this circuit can work properly near the sub-threshold supply voltage. The circuit has low temperature coefficient. The temperature coefficient is 87 ppm/°C in –10°C to 80°C. The measured
reference output voltage is around 154 mV. This circuit is suitable for low voltage applications.

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