Ultralow-power switching via defect engineering in germanium telluride phase-change memory devices

Pavan Nukala\textsuperscript{1}, Chia-Chun Lin\textsuperscript{1}, Russell Composto\textsuperscript{1} & Ritesh Agarwal\textsuperscript{1}

Crystal-amorphous transformation achieved via the melt-quench pathway in phase-change memory involves fundamentally inefficient energy conversion events; and this translates to large switching current densities, responsible for chemical segregation and device degradation. Alternatively, introducing defects in the crystalline phase can engineer carrier localization effects enhancing carrier–lattice coupling; and this can efficiently extract work required to introduce bond distortions necessary for amorphization from input electrical energy. Here, by pre-inducing extended defects and thus carrier localization effects in crystalline GeTe via high-energy ion irradiation, we show tremendous improvement in amorphization current densities (0.13–0.6 MA cm\textsuperscript{-2}) compared with the melt-quench strategy (\sim 50 MA cm\textsuperscript{-2}). We show scaling behaviour and good reversibility on these devices, and explore several intermediate resistance states that are accessible during both amorphization and recrystallization pathways. Existence of multiple resistance states, along with ultralow-power switching and scaling capabilities, makes this approach promising in context of low-power memory and neuromorphic computation.
Phase-change materials (PCMs), which rapidly and reversibly transform from crystalline to amorphous phase, are viable alternatives to the relatively slow non-volatile flash memory technology\(^1\) with random access capability. One of the problems with PCMs is the use of high programming currents (and current densities) during the crystal–amorphous transformation (RESET) achieved conventionally via the melt-quench pathway\(^2\); and reducing the active device volumes has been pursued as a potential solution to mitigate this problem\(^3\)-\(^5\).

While reports on phase-change line and bridge devices demonstrated lower RESET currents by shrinking the volume of the PCM directly\(^6\)-\(^8\), works on PCM devices with carbon nanotube electrodes\(^9\) showed very low RESET currents (\(\sim 5\) \(\mu\)A) by minimizing the contact areas and hence the active device volumes (\(3 \times 3 \times 3\) nm\(^3\)). Alternative approaches to reducing the RESET currents include lowering the melting point of the PCM by doping them with nitrogen or silicon\(^9\),\(^10\). Although these approaches illustrate intelligent device designs based on geometry and chemical doping, none of them have been able to reduce the high amorphization current densities (\(\sim 50\) \(\text{MA} \cdot \text{cm}^{-2}\)) that are responsible for device degradation issues owing to chemical segregation and heat\(^1\), thus precluding the widespread commercialization of PCM technology.

In the melt-quench pathway, work required to amorphize a crystal is extracted from the heat generated by input electrical energy via inelastic carrier–phonon scattering; and this involves several fundamentally inefficient energy conversion events\(^12\) manifested as large writing current densities. Engineering carrier localization effects by pre-inducing extended defects in crystalline PCM enhances carrier–lattice coupling\(^13\), enabling efficient exchange of energy back and forth between the carriers and the lattice\(^14\),\(^15\). The input electrical energy, hence, can directly perform work on the lattice with minimal loss in the form of heat (wasteful energy) and introduce critical bond distortions required for amorphization\(^16\), potentially lowering the writing current densities.

Here we select crystalline GeTe (R3m), a simple binary PCM system, to demonstrate drastic improvement in amorphization current (and power) densities achieved by introducing carrier localization near the Fermi level (\(E_F\)). All known phases of crystalline GeTe show \(p\)-type metallic conduction owing to the presence of large concentration (order of \(10^{20}\) \(\text{cm}^{-3}\)) of intrinsic Ge vacancies (\(p\)-type dopants)\(^17\). The carriers near the Fermi level (\(E_F\)), which participate in transport, are delocalized and couple weakly with the lattice. By pre-inducing extended defects using high-energy \(\text{He}^+\) ion irradiation, we show for GeTe devices in the crystalline phase that the carriers at \(E_F\) can be localized, and hence strongly couple with the lattice\(^14\),\(^15\). These devices transformed to an amorphous phase via the defect-based pathway\(^13\),\(^18\), at current densities (\(j_s\)) of 0.13–0.5 \(\text{MA} \cdot \text{cm}^{-2}\) significantly lower than \(j_s = 50\) \(\text{MA} \cdot \text{cm}^{-2}\) observed in the melt-quench pathway\(^6\),\(^7\). Furthermore, we illustrate scaling of switching currents with device volumes, and reversible and repeatable low-power switching from defect-engineered crystalline states to amorphous phase.

**Results**

**Inducing carrier localization in single-crystalline GeTe nanowires.**

Single-crystalline GeTe nanowires were synthesized using the vapour–liquid–solid mechanism\(^19\), and multiple electrode devices were fabricated using electron-beam lithography, and encapsulated with 30 nm of \(\text{SiO}_2\) (Fig. 1a, inset; Methods)\(^13\). All devices were irradiated using 2 MeV \(\text{He}^+\) ions, in a Rutherford backscattering set-up, at different dosages, and beam currents not exceeding 30 nA (ref. 20; Methods; Supplementary Note 1). Our stopping and range of ions in matter calculations (Supplementary Note 1) showed that there is a 2\% loss in the incident energy upon the penetration of \(\text{He}^+\) ions through our nanowires, ensuring extended defect formation via knock-on damage and dismissing any role of ion implantation (\(\text{He}^\text{bubble} or \text{void formation}\))\(^21\). To understand the effect of pre-induced defects on the transport characteristics in nanowire devices, we performed temperature-dependent resistivity measurements after ion-beam exposure at various dosages. Resistivity was evaluated as \(\rho = R_{\text{NW}}A/L\), where \(R_{\text{NW}}\) is the resistance of the nanowire obtained by subtracting the contact resistance measured in a multiple probe configuration (Fig. 1a, inset) from the total device resistance. \(L\) and \(A\) are the length and cross-sectional area of the nanowire device, respectively (see Supplementary Note 2, raw data shown in Supplementary Fig. 1). At dosages up to 700 \(\mu\text{C} \cdot \text{cm}^{-2}\), the resistivity of all our devices increased linearly with increasing temperature above 30 K and exhibited a saturation value (\(\rho_0\)) below 30 K. This behaviour is typical of metals, where dominant contribution to resistivity at low temperatures is from temperature-independent carrier-defect scattering and carrier-phonon scattering at high temperatures\(^13\). \(\rho_0\) depends on the defect density; and conversely can be used as a measurable metric for the same in the metallic state. As illustrated for representative devices (labelled nanowires 1–4 in Fig. 1a, \(\rho_0\) increased with increasing dosage (from 0 to 700 \(\mu\text{C} \cdot \text{cm}^{-2}\)), consistent with increasing pre-induced defect density in the material.

Another quantity that is sensitive to the defect concentration in metallic state is the slope of temperature–resistivity plots in the linear increase regime (temperature coefficient of resistivity, TCR), which decreases with increasing defect density\(^22\),\(^23\), nevertheless remaining positive. Positive TCR is a characteristic of transport via delocalized carriers in a metal, which can be described by Boltzmann transport equation\(^24\). In all our devices (representative devices nanowires 1–4 shown in Fig. 1b), although TCR showed an initial increase with dosage up to 50 \(\mu\text{C} \cdot \text{cm}^{-2}\) (for reasons see Supplementary Note 3 and Supplementary Fig. 2), subsequently up to 700 \(\mu\text{C} \cdot \text{cm}^{-2}\) it showed a decreasing trend to a less positive value, consistent with increasing defect density. More importantly, TCR remained positive, suggesting that at these low dosages (<700 \(\mu\text{C} \cdot \text{cm}^{-2}\)) carrier localization effects are insignificant.

At higher dosages (1,800–3,600 \(\mu\text{C} \cdot \text{cm}^{-2}\)), however, the resistivity of all the tested devices showed a non-linear decrease with increasing temperature (TCR is negative but cannot be uniquely defined), which is a signature of localized carriers at \(E_F\) participating in transport\(^25\). This demonstrates an electronic transformation of crystalline GeTe from a metallic state to dirty metallic (\(\rho_0\) is finite) or insulating states (\(\rho_0 \rightarrow \infty\))\(^15\). The exact dosage at which this transformation occurred varied from device to device, but all devices showed localization effects in transport above a dosage of 3,600 \(\mu\text{C} \cdot \text{cm}^{-2}\). For instance, the device nanowire 1 (Fig. 1c) transformed to an insulating state demonstrating variable range hopping (VRH) conduction (Fig. 1c, inset) at a dosage of 1,800 \(\mu\text{C} \cdot \text{cm}^{-2}\). Devices nanowires 2 and 3 (Fig. 1d) transformed to dirty metal state at 3,600 \(\mu\text{C} \cdot \text{cm}^{-2}\), demonstrating a power law conduction (\(\sigma\) varying as \(T^{0.3}\)), a characteristic of disordered metals showing weak localization effects (Fig. 1d, inset)\(^25\). The stability of these defect-engineered states was tested by heating the devices to 200 °C and monitoring the change in resistance with time; and they showed no change in resistance for 36 h (Supplementary Fig. 3), suggesting that they are thermodynamically stable (Supplementary Note 4).

To understand the structural nature of the radiation induced defects, we performed transmission electron microscopy (TEM) on nanowire devices assembled on TEM compatible platform\(^18\).
and exposed to different dosages of He$^+$ ion irradiation. At modest dosages (40–100 μC cm$^{-2}$), where the devices remain metallic, we observed the formation of dislocation loops, two-dimensional defects (stacking faults) and defect tetrahedra—formed due to vacancy/interstitial supersaturation following knockout of atoms (Fig. 2a–c). The spatial distribution of these defects along the nanowire is sporadic. For irradiation at higher dosages (1,800 μC cm$^{-2}$), the entire nanowire became replete with intersecting two-dimensional defects (as illustrated in different regions of a representative nanowire in Fig. 2d–g), still being single crystalline (Fig. 2d, inset), and this stage corresponds to electronic states where carrier localization dominates transport.
Amorphization behaviour of defect-engineered nanowire devices. To verify the idea that pre-inducing defects and engineering carrier localization effects is beneficial for power reduction for amorphization, we studied the switching (crystal–amorphous) and volume scaling properties of the devices as a function of radiation dosage. We amorphized our devices in crystalline phase exposed to different dosages of ion irradiation, by applying a train of voltage pulses (50 ns) of increasing amplitude, separated by 1 s (to allow complete thermalization between pulses), until resistance increased abruptly by at least two orders of magnitude (see Supplementary Note 6 and Supplementary Fig. 5 for pulse shapes, and dynamic currents measured from a pulse). The crystal–amorphous transformation in all these devices occurred via a defect-based mechanism, where heat shock from an electrical pulse first creates extended defects (full and partial dislocations)\textsuperscript{13,18}. The pre-induced defects, along with the defects created by electrical pulses, migrate with the hole-wind force and accumulate at a region of local inhomogeneity creating a defect template with intersecting defects, along which amorphization takes place beyond a critical defect density\textsuperscript{13,18}. To understand the size scaling of RESET currents \(j_s\) in this defect-based mechanism, and the influence of pre-induced defects on them, we compared RESET current densities \(j_d\) as a function of device length \(l_d\) at various dosages (Fig. 2; Supplementary Fig. 6a). These plots encompass complete information on size (length and cross-sectional area) dependence of \(j_d\). At dosages up to 700 \(\mu\text{C} \text{cm}^{-2}\), where no carrier localization effects were present, we observed that \(j_d\) increased with increasing dosage for any particular device length (Supplementary Fig. 6a–d). This illustrates that pre-induced defects can be detrimental for \(i_s\) (\(j_d\)), if they do not induce any significant localization effects in transport (see Supplementary Note 7 for analysis of switching behaviour at low dosages).

However, at higher dosages (>1,800 \(\mu\text{C} \text{cm}^{-2}\)), where the localization effects dominated transport (Fig. 1a–d), \(j_s\) (and \(i_s\)) were drastically lowered (Fig. 3). At a dosage of 3,600 \(\mu\text{C} \text{cm}^{-2}\), \(i_s\) of the device (referred as D1) with active volume as large as 100 × 100 × 750 nm (see Supplementary Note 8) was as low as 26 \(\mu\text{A}\) (\(j_s\): 0.26 \(\text{MA cm}^{-2}\)); and for a smaller device (80 × 80 × 320 nm, referred as D2), \(i_s\) was 8 \(\mu\text{A}\) (\(j_s\): 0.13 \(\text{MA cm}^{-2}\)). The current densities and power densities for amorphizing these defect-engineered devices were \(\sim\)300 and 10\(^5\) times smaller, respectively, than those required by the melt-quench pathway\textsuperscript{5} (\(i_s\): 5 \(\mu\text{A}\), \(j_s\): 50 \(\text{MA cm}^{-2}\); Supplementary Note 8, Supplementary Table 1). With volume scaling also demonstrated on these devices, the absolute power required for switching very small volumes of active PCM\textsuperscript{19} is significantly lowered in this approach, and this can potentially mitigate issues such as thermal cross-talk and chemical segregation\textsuperscript{11}. Furthermore, the importance of carrier localization and the role of lattice–carrier coupling in efficiently converting input electrical energy into the work required for amorphization resulting in significant lowering of switching powers are highlighted by these results.

Demonstration of metastable intermediate states. The defect-engineered crystalline states where carrier localization dominates transport, structurally corresponds to the entire nanowire device being replete with intersecting extended defects, or defect
follows we will refer to the representative electronic states in 20-ns pulses (Supplementary Fig. 10). For the discussion that measurement on the recrystallized phase (intermediate states were observed in all the other devices exposed in Supplementary Note 9 and Supplementary Fig. 9). Similar stability of intermediate and amorphous phases is discussed increasing defect concentration at the template (thermal Fig. 8 for TEM data) whose resistance increases with metastable states in the crystalline phase (see Supplementary controlled defect accumulation and access to several intermediate concentration at a region in the defect template. However, with 20-ns pulses, less energy is transferred to the defects, resulting in controlled defect accumulation and access to several intermediate metastable states in the crystalline phase (see Supplementary Fig. 8 for TEM data) whose resistance increases with increasing defect concentration at the template (thermal stability of intermediate and amorphous phases is discussed in Supplementary Note 9 and Supplementary Fig. 9). Similar intermediate states were observed in all the other devices exposed to a dosage of 3,600 μC cm−2 upon programming them with 20-ns pulses (Supplementary Fig. 10). For the discussion that follows we will refer to the representative electronic states in D1 in the crystalline phase with resistances of ~10, 40 and 70 kΩ as states 1, 2 and 3, respectively (Fig. 5a).

To understand whether these intermediate resistance states can be reversibly obtained starting from the amorphous phase, we recrystallized the amorphized device D1, via d.c. I–V sweeps, setting a very low compliance current (Ic) of 5 μA. As shown in Fig. 5b, upon a voltage sweep from 0 to 1 V (green data), the amorphous phase first transformed to an intermediate resistance state (70 kΩ, state 3). Upon a second voltage sweep from 0 to 1 V on state 3, we observed a sudden drop in current at 0.02 V, followed by a switching event to another intermediate state (red data in Fig. 5b) with resistance of 40 kΩ, state 2. Another voltage sweep from 0 to 1 V on state 2 showed a similar drop in current at 0.02 V, followed by a switching event to the starting electronic state, state 1 (10 kΩ, blue data in Fig. 5b). To ensure reliability in the formation of all the demonstrated states, we switched these devices for 160 cycles, where every cycle involved the following steps: switching state 1 to a high-resistance amorphous phase by the application of a 100 ns, 26 μA pulse, and switching back to state 1 from the amorphous phase via sweeping d.c. voltage from 0 to 1 V, multiple times, if necessary (depending on the value of Ic). We changed the Ic between cycles to confirm the dependence of formation of intermediate states on Ic (Fig. 5c).

When Ic was set to 50 μA, we observed only two states: a high-resistance amorphous state (>1 MΩ), and state 1, a low-resistance crystalline state (~10 kΩ). However, when Ic was 10 μA, we consistently observed amorphous state first transforming into an intermediate resistance state (~40 kΩ) with the first voltage sweep, and then to state 1 with another voltage sweep from 0 to 1 V. Upon further reducing Ic to 5 μA, we observed...
amorphous phase to state 1 transformation in every cycle requiring three voltage sweeps from 0 to 1 V, with the first two voltage sweeps accessing two intermediate resistance states (between 35 and 80 kΩ with some variability), and the final sweep transforming these intermediate states to state 1. It must be noted that the variability of resistance of the intermediate states (Fig. 5c) upon cycling (with \( I_c = 5 \mu A \)), may not currently conform to commercial standards for multistate memory applications, and need to be addressed and improved in further studies. Nevertheless, these findings provide a proof of concept that intermediate states can reliably obtained starting from both crystalline phase and an amorphous phase, with the controlling parameters being the pulse width and \( I_c \) (Joule heating following threshold switching), respectively.

From these results, the mechanism for amorphous–crystal transformation in the defect-based pathway becomes clear. Following amorphization, the nanowire has a background density of pre-induced defects, and a local region has a higher defect concentration (defect template). The amorphous region is a part of this template where the defect concentration exceeds a critical value, and it cuts across the cross-section of the nanowire\(^{13,18}\) (Supplementary Fig. 11a–c for TEM images). Transformation from the amorphous phase to any crystalline state involves threshold switching followed by recrystallization of the amorphous region, and subsequently a reduction of defect concentration in the rest of the template through homogenization of defects (to the background concentration) via Joule heating. Thus following recrystallization, the degree of defect homogenization can be controlled via \( I_c \), and this provides access to several intermediate resistance states in the crystalline phase (Supplementary Note 10).

**Amorphization of intermediate resistance states via d.c. current.** Another subtle feature in d.c. I–V switching behaviour of intermediate states (states 2 and 3 of D1) is the sudden drop in current (increase in resistance) at very low currents (0.1 \( \mu A \) in Fig. 5b, red and blue curves). This event corresponds to intermediate states first transforming to an amorphous phase, a permanent structural change (Supplementary Fig. 12a,b). It is consistent with the understanding that the momentum (and energy) transfer from carriers to defects at 0.1 \( \mu A \) is sufficient to migrate more defects to the already existing defect-template region in the intermediate states, thus increasing the defect concentration beyond a critical limit to nucleate the amorphous phase. These

**Figure 5 | Accessing intermediate resistance states on GeTe nanowire devices defect engineered into insulating crystalline phase.**

(a) Programming curve on D1 for the RESET operation. When 50-ns pulses were applied, the transformation to the amorphous phase was sudden. With 20-ns pulses, the transformation happened gradually accessing several intermediate resistance states. Low-voltage, 20-ns pulses accumulates defects at a local region creating an intersecting defect template. Subsequent controlled addition of defects with higher amplitude pulses to this template increases the resistance of the device creating intermediate resistance states. States 1, 2 and 3, and amorphous phase (increasing order of resistance) are boxed. (b) Voltage sweep from 0 to 1 V (green) demonstrating a threshold-switching event of the amorphous phase to state 3 at <1 V with compliance current \( (I_c) \) set at 5 \( \mu A \). A second sweep starting from state 3 (red), revealing a drop in current at 0.01 V corresponding to amorphization event, and the amorphous phase subsequently transformed to state 2 after a threshold-switching event to state 2. Another voltage sweep from 0 to 1 V starting with state 2 (blue), again showing a drop in the current at 0.01 V, signifying amorphization (Supplementary Fig. 12a)—and the amorphous phase subsequently threshold switched and transformed to state 1. The arrows in the figure correspondingly indicate carrier-wind force assisted amorphization and threshold-switching events (c). Repeatable switching measurements, with every cycle consisting of a 100-ns, 26-\( \mu A \) pulse transforming state 1 to amorphous phase, followed by I-V sweeps until state 1 is eventually retrieved; and between every cycle \( I_c \) was randomly set to 50, 10 or 5 \( \mu A \). For the first 60 cycles, \( I_c \) was set to 50 \( \mu A \), for the next 10 cycles \( I_c = 10 \mu A \). From 70 to 82 cycles, \( I_c = 5 \mu A \), followed by 50 \( \mu A \) from 83 to 150 cycles. Further up to 160 cycles, \( I_c = 10 \mu A \). When \( I_c = 50 \mu A \), amorphous phase always switched to state 1 directly, and when \( I_c = 5 \) and 10 \( \mu A \) intermediate metastable states became accessible. Here the intermediate resistance states were created by controllably removing defects from the defect-templated region.
length (or increase in $z$) or a decrease in $N(E_F)$ or both. On the other hand, the conduction characteristics of the amorphous phase (Fig. 6b) showed VRH behaviour at high temperatures ($>150$ K), with $A = 5.1 \times 10^{-25}$, and deviated from VRH behaviour (log($S$) proportional to $T^{-0.25}$) at low temperatures (Supplementary Fig. 13). This behaviour is different from that of typical melt-quench amorphous phase, which shows activated conduction via emission of carriers into delocalized states at high temperatures and VRH at low temperatures\(^{29}\) (Supplementary Note 12). It will be an interesting future direction to rigorously study the nature of the observed amorphous phase and understand device-related issues such as resistance drift in comparison with the conventional melt-quench amorphous phase.

The schematics of band structure shown in Fig. 6c explain the observed conduction characteristics (Fig. 6a,b) of various representative states. In state 1, $E_F$ is above the mobility edge ($E_m$) surrounded by a large density of single-electron traps $N(E_F)$. Progression from state 1 to state 3 by adding more defects either shifts the $E_F$ towards the mid-gap, which reduces $N(E_F)$ and localization length, or creates more paired trap centers, which reduces $N(E_F)$. Finally, in the amorphous phase, $E_F$ is pinned to the mid-gap\(^{30,31}\), with $N(E_F)$ at its minimum value. In the reverse process (SET), by controlled homogenization (removal) of defects from the defect-template region via Joule heating, $E_F$ moves back towards the mobility edge, and $N(E_F)$ starts to increase, accessing all the crystalline intermediate resistance states. Pulse width (Fig. 5a) and compliance current (Fig. 5c) can be used to control the addition and homogenization of defects respectively. It is important to note here that multiple resistance states in PCM reported in earlier works\(^{30–34}\) were created by controlling the relative volumes of the amorphous and crystalline states, the only two physically different states, and are fundamentally different from the multiple resistance states in this work.

Discussion

We demonstrated that defect-engineered crystalline GeTe with dominant carrier localization effects transforms to an amorphous phase at current and power densities significantly lower than some of the best reported low-power devices operated through melt-quench strategy\(^6\). These results emphasize the importance of carrier–lattice coupling in the insulating state in carrying out energy efficient amorphization. Our devices displayed good reversibility and endurance, suggesting new strategies for potentially mitigating the issue of chemical segregation and heat-based device degradation problems, common in melt-quench approach\(^11\). The recent discoveries of localization effects\(^{35}\) and defect-templated amorphization\(^{18}\) in Ge–Sb–Te alloys suggests that defect-engineering approach could be applied to other well-known PCMs too. In addition, with our demonstration of scaling of switching properties in the defect-based approach and multistate switching, we believe that nanoscale PCM structures (mushroom, sidewall, pillar or confined architectures)\(^{5,36}\) engineered into electronic states in crystalline phase that show localization behaviour in transport will be promising for ultralow-power memories and novel computation strategies\(^{29,30}\).

Methods

Synthesis of GeTe nanowires. GeTe nanowires were synthesized using metal catalyst-mediated vapour–liquid–solid process, where bulk GeTe powder (99.9%, Alfa Aesar, melting temperature, 724 °C) was placed at the centre of a tube furnace. Silicon oxide substrate evaporated with Au film (8 nm) and subsequently annealed at 720 °C for 10 min was placed on the downstream side of the furnace (~15 cm away from the middle). The furnace was heated to 400 °C at a carrier gas (Ar) flow rate of 100 s.c.c.m. and a pressure of 10 torr, and maintained so for 10 h before the furnace was slowly cooled to room temperature.
**Device fabrication.** Multiple electrode devices were fabricated using electron-beam lithography. Nanowires were dry transferred onto an insulating substrate with pre-patterned markers. Three layers of PMMA 495 A4 and three layers of PMMA 950 A2 were spin coated and baked (180 °C) following which electron-beam lithography, metallization (Ti/Au: 50/100 nm) and lift-off procedure were performed. The devices were subsequently annealed at 350 °C, and a 30-nm SiOx film was conformally deposited by plasma-enhanced chemical vapour deposition.

**Ion irradiation.** The devices thus fabricated were irradiated with 2 MeV He$^+$ ions, (beam area: 5 × 5 mm) in a tandem accelerator (NIEC minitandem ion accelerator). Substrates were aligned perpendicular to the beam, and ion bombardment was performed until a cumulative prescribed dosage was reached, with ion current maintained below 30 nA (as measured from picoammeter). Dosage was calculated as IA/t, where I is the instantaneous ion current, t is the time of exposure and A is the area of the beam area (5 × 5 mm). We verified using SRIM (Stopping and Range of Ions in Matter) software that He$^+$ ion exposure and knock-on damage is uniform throughout the nanowire devices (Supplementary Note 1).

**Electrical testing.** Temperature–resistance measurements were performed in the Lakeshore TTPX cryogenic probe station, and resistance measurements were carried out via I–V sweeps at very low bias (~ 2 to 2 mV) using Keithley 2,602 (I–V analyser/source meter). Switching and endurance tests were performed using Keithley 3,401 for pulse generation, 2,602 (I–V analyser) for resistance measurement after the application of the pulse and Keithley 2,700 as the data acquisition system. The shapes of the voltage pulses generated and dynamic current response produced were verified using a 500 MHz Tektronix DPO3052 digital oscilloscope. Applied voltage pulse was measured by connecting the device in parallel to the 50Ω input channel 1 of the oscilloscope. The current response was measured by measuring the voltage drop across a 50Ω resistor connected in series with the device, and in parallel with a second 50Ω input channel of the oscilloscope.

**References**

1. Wong, H.-S.P. et al. Phase change memory. Proc. IEEE 98, 2201–2227 (2010).
2. Bez, R. & Pirovano, A. Non-volatile memory technologies: emerging concepts and new materials. Mater. Sci. Semicond. Process. 7, 349–355 (2004).
3. Pirovano, A. et al. in IEDM ’03 Technical Digest IEEE International Electron Devices Meeting (Washington, DC, USA, 2003).
4. Chen, Y. C. et al. in IEDM ’06 International Electron Devices Meeting, 1–4 (San Francisco, CA, USA, 2006).
5. Lankhorst, M. H., Ketelaars, B. W. & Wolters, R. A. Low-cost and nanoscale non-volatile memory concept for future silicon chips. Nat. Mater. 4, 347–352 (2005).
6. Xiong, F., Liao, A. D., Estrada, D. & Pop, E. Low-power switching of phase-change materials with carbon nanotube electrodes. Science 332, 568–570 (2011).
7. Xiong, F. et al. Self-aligned nanotube–nanowire phase change memory. Nano Lett. 13, 464–46902 (2012).
8. Lee, H.-J., Jung, Y. & Agarwal, R. Highly scalable non-volatile and ultra-low-power phase-change nanowire memory. Nat. Nanotech. 2, 626–630 (2007).
9. Hwang, Y. N. et al. in IEDM ’03 Technical Digest, IEEE International Electron Devices Meeting, 893–896 (Washington, DC, USA, 2003).
10. Qiao, B. et al. Effects of Si doping on the structural and electrical properties of Ge$_2$Sb$_2$Te$_5$ films for phase change random access memory. Appl. Surf. Sci. 252, 8406–8410 (2006).
11. Kim, C. et al. Direct evidence of phase separation in Ge$_2$Sb$_2$Te$_5$ in phase change memory devices. Appl. Phys. Lett. 94, 193504 (2009).
12. Moran, M. J., Shapiro, H. N., Boettner, D. D. & Bailey, M. B. Fundamentals of Engineering Thermodynamics 8th edn (John Wiley & Sons, 2014).
13. Nukala, P. et al. Direct observation of metal-insulator transition in single-crystalline germanium telluride nanowire memory devices prior to amorphization. Nano Lett. 14, 2201–2209 (2014).
14. Mott, N. F. Metal-Insulator Transitions 2nd edn (Taylor & Francis, 1990).
15. Mott, N. F. & Davis, E. A. Electronic Processes in Non-Crystalline Materials Vol. 2 (Oxford Univ. Press Inc., 1979).
16. Kolobov, A. V., Krbal, M., Fons, P., Tominga, I. & Uruga, T. Distortion-triggered loss of long-range order in solids with bonding energy hierarchy. Nat. Chem. 3, 311–316 (2011).
17. Edwards, A. H. et al. Electronic structure of intrinsic defects in crystalline germanium telluride. Phys. Rev. B 73, 045210 (2006).
18. Nam, S. W. et al. Electrical wind force-driven and dislocation-templated amorphization in phase-change nanowires. Science 336, 1561–1566 (2012).
19. Lee, S.-H., Ko, D.-K., Jung, Y. & Agarwal, R. Size-dependent phase transition memory switching behaviour and low writing currents in GeTe nanowires. Appl. Phys. Lett. 89, 232116 (2006).
20. Compston, R. J., Walters, R. M. & Genzer, J. Application of ion scattering techniques to characterize polymer surfaces and interfaces. Mater. Sci. Eng. Rep. 38, 167–188 (2002).
21. Ikawari, H., Yasunaga, K., Morishita, K. & Yoshida, N. Microstructure evolution in tungsten during low-energy helium ion irradiation. J. Nucl. Mater. 283, 1134 (2000).
22. Mook, J. H. Electrical conduction in concentrated disordered transition metal alloys. Phys. Stat. Sol. 17, 521–530 (1973).
23. Park, M.-A., Savran, K. & Kim, Y.-J. Weak localization and the Mooij rule in disordered materials. Phys. Stat. Sol. 237, 500–506 (2003).
24. Harris, S. An Introduction to the Theory of Boltzmann Equation (Dover Publications, 1999).
25. Lee, P. A. & Ramakrishnan, T. V. et al. Disordered electronic systems. Rev. Mod. Phys. 57, 287–337 (1985).
26. Yu, K. Y. et al. Radiation damage in helium ion irradiated nanocrystalline Fe. J. Nucl. Mater. 2012, 140–146 (2012).
27. Pirovano, A., Lacaita, A. L., Benvenuti, A., Pellizzier, F. & Bez, R. Electrical switching in phase-change memories. IEEE Trans. Electron Devices 51, 452–459 (2004).
28. Zallen, R. The Physics of Amorphous Solids (John Wiley & Sons, 1983).
29. Longeaud, C., Luckas, J. & Wuttig, M. Some results on the germanium telluride density of states. J. Phys. Condens. Mat. 140–146 (2002).
30. He, Q. et al. Continuous controllable amorphization ratio of nanoscale phase change memory cells. Appl. Phys. Lett. 104, 223502 (2014).
31. Kuzum, D., Jeyasingh, R. G., Lee, B. & Wong, H. S. NANOELECTRONIC PROGRAMMABLE SYNAPSES BASED ON PHASE CHANGE MATERIALS FOR BRAIN-INSPIRED COMPUTING. Nano Lett. 12, 2179–2186 (2012).
32. Wright, C. D., Hosseini, P. & Diosdado, J. A. V. Beyond von-Neumann computing with nanoscale phase-change memory devices. Adv. Funct. Mater. 23, 2248–2253 (2013).
33. Jie, F. et al. Design of multi-states storage medium for phase change memory. Jpn J. Appl. Phys. 46, 5724–5727 (2007).
34. Skelton, J. M., Loke, D., Lee, T. H. & Elliott, S. R. Understanding the multistate SET process in Ge-Sb-Ta based phase-change memory. J. Appl. Phys. 112, 064901 (2012).
35. Siegrist, T. et al. Disorder-induced localization in crystalline phase-change materials. Nat. Mater. 10, 202–208 (2011).
36. Hudgens, S. & Johnson, B. Overview of phase-change chalcogenide nonvolatile memory technology. MRS Bull. 29, 829–832 (2004).

**Acknowledgements**

This work was supported by NSF (DMR-1002164 and 1210503), Penn-MRSEC (DMR05-20020), Materials Structures and Devices Center at MIT, NSF/MRSEC-DMR 11-20901, and partially from the NSF Polymer Program DMR09-07493 and NSF Materials World Network DMR-120379. Ion irradiation and electron microscopy were performed at the Nanoscale Characterization Facility at the University of Pennsylvania.

**Author contributions**

P.N. and R.A. conceived the concepts, designed experiments and co-wrote the manuscript. P.N. carried out synthesis, device fabrication, TEM characterization, transport measurements and data analysis. C.C.L. carried out ion-irradiation experiments. C.C.L. along with R.C. carried out SRIM calculations, and subsequent analysis on ion penetration in GeTe nanowire devices. P.N., C.C.L., R.A. and R.C. discussed all the data and their interpretations.

**Additional information**

**Supplementary Information** accompanies this paper at http://www.nature.com/naturecommunications

**Competing financial interests:** The authors declare no competing financial interests.

**Reprints and permission** information is available online at http://npg.nature.com/reprintsandpermissions/

**How to cite this article:** Nukala, P. et al. Ultra low-power switching via defect engineering in germanium telluride phase-change memory devices. Nat. Commun. 7:10482 doi: 10.1038/ncomms10482 (2016).