Design of multi-channel digital correlator in SAMR

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Abstract. Synthetic Aperture Microwave Radiometer (SAMR) can be carried on the satellite to realize the global large-scale measurement of ocean salinity and soil moisture. As a key component of SAMR, the multi-channel digital correlator has been introduced in this paper from three aspects: an improved method to implement multi-channel correlation, the correlator design and the test results of the correlator. The improved method which effectively reduces the FPGA resource utilization and system complexity is applied to the multi-channel digital correlator system which consists of three signal collectors and one signal processor. The design of multi-channel digital correlator can ensure the real-time signal sampling and processing of 144 ADC channels. The results demonstrate that the measurement accuracy of correlation coefficient can exceed 0.99.

1. Introduction
Either soil moisture or ocean salinity plays important role in global water cycle. They are key parameters for monitoring the global climate change[1]. Synthetic aperture microwave radiometer will measure global sea surface salinity with 50-km spatial resolution and soil moisture with 25-km spatial resolution, so it can provide a very important environmental guarantee for economic activity and agricultural production[2]. Synthetic aperture microwave radiometer is a 2-D aperture synthesis radiometer working at L band and its dual Y-shaped arrays containing 23 L-band antennas per arm plus one in the center in L-band array[3].

The digital correlator is the key part of SAMR and it can obtain the vertical and horizontal visibility function and Stokes parameter by correlation processing. By using digital technology such as digital filtering and digital Hilbert, it achieves an excellent performance. The main function of digital correlator is the synthetic aperture correlation processing, which is to multiply and integrate the signal of two channels. And then the visibility function of horizontal polarization and vertical polarization can be obtained by complex correlation.

2. Multi-channel digital correlation implementation method

2.1 Key point of multi-channel digital correlator
In order to obtain high resolution, microwave radiometers usually adopt the two-dimensional synthetic aperture technique[4]. The number of the existing 2d synthetic aperture array is 144, so the number of correlation operation units required is \( \sum_{i=1}^{2} C_{144}^2 = 20592 \). Table 1 shows the indicator requirements of digital correlator. To reduce the computation complexity, the digital correlator uses two-order quantization to calculate the correlation coefficient. Still, thousands of correlation operations consume a lot of hardware resources. Taking XC5VFX130T FPGA as an example, using the traditional
multiplication and accumulation method, 20,592 correlation operations should be carried out at the same time, at least 6 pieces of FPGA are needed. So the complexity, power consumption and volume of digital correlator are greatly increased. All these make the hardware design, software debugging, performance testing and other aspects of digital correlator more difficult.

Table 1  Digital correlator indicator

| Indicator              | Requirement          |
|------------------------|----------------------|
| Center frequency       | 75Mhz                |
| Number of channels     | 144                  |
| Bandwidth              | 30MHz                |
| Sample frequency       | 60MHz                |
| Sample jitter          | <20ps                |
| Synchronization        | <150ps               |
| ENOB                   | >8bit                |
| Integration time       | 1s                   |
| Measurement accuracy   | correlation coefficient >0.99 |

In general, the difficulties of multi-channel digital correlator are mainly focused on how to realize tens of thousands of correlation calculations within the limited FPGA hardware resources. According to the actual demand, there is a large amount of computation in signal processing, and the resource occupancy rate of FPGA is close to the upper limit, which increases the difficulty of FPGA placing and routing.

2.2 An improved multi-channel digital correlation method

Digital correlation operation is essentially multiplication and accumulation. In FPGA, multiplication and accumulation operation can be realized in two ways: one is SLICE and the other is DSP48E. Although DSP48E has advantages in terms of speed and power consumption, the number of DSP48E operation units in FPGA is usually relatively limited due to its high cost. Taking XC5VFX130T FPGA as an example, the number of DSP48E is 320, and the number of SLICE is 20480 [5]. For the synthetic aperture array receiving system, the number of DSP48E and SLICE cannot meet the processing requirements. At the same time, a large number of block ram resources inside FPGA are not effectively used, so an innovative correlation implementation method is proposed. Its essence is to use the block ram resources of FPGA to replace SLICE resources and increase the processing capacity of correlator. Figure 1 illustrates the block diagram of the improved correlation method.
The correlation implementation method first groups a large number of correlation cells, and 32 correlation processing units are divided into a group. Figure 1 shows the method of a group of correlation operations. The correlation calculation module is implemented using the Binary Counter IP core[6], the 32-bit adder is implemented using DSP48E, and the RAM stores the accumulated calculation results. The MUX, (multiplexer) controlled by 4bit counter1, polls the binary accumulator output and then add the polling result and the data stored in RAM before placing them into RAM. In this method, the multiplication and addition of large bit width in traditional digital correlation operation are replaced by binary counter, adder and block RAM with small bit width, which makes full use of RAM resources inside FPGA and greatly improves processing efficiency.

In order to verify the improved method, Modelsim 10.1 is used to simulate the FPGA code. FPGA operating clock is 60MHz and simulation integration time is 100ms for convenience. If the inputs are identical signals, the output value should be 6000000, actually the output value is 5996600. This is because the RAM data needs to be output every 1ms, and the RAM writing operation is stopped at this time. The 34 clock cycles consumed in this process are not calculated, so the accumulated value of 3400 clock cycles is missing within the integral time of 100ms. This deviation is a fixed value, which can be corrected in the subsequent processing and does not affect the correlation accuracy.

2.3 Evaluation of the improved implementation method

In order to further demonstrate that the above method can improve the processing efficiency of FPGA for mass input data, the experiment uses the traditional correlation method and the improved correlation method to accomplish 6144 channels of digital correlation processing. The programming language is VHDL, the compilation tool is ISE12.4, and the hardware platform is XC5VFX130T FPGA. Using the two methods, the comparison of resource occupancy after placing and routing is shown in table2.

| Table2 | Utilization of the improved correlation method |
|--------|------------------------------------------------|
| resource type | traditional method | correlation | improved method | correlation |
| SLICE | 18756 | 91% | 8017 | 39% |
| BLOCK RAM | 2 | 1% | 128 | 42% |

It can be seen from Figure 3 and Figure 4 that the improved correlation implementation reduces the resource utilization of SLICE from 91% to 39%, which greatly reduces the complexity of the system when the input becomes 144 channels of signal.

3. Design of multi-channel digital correlator

Multi-channel digital correlator composed of three signal collectors and one signal processor is designed to implement 144 channel correlation. Each of the collector completes 48 channels of signal sampling and digital filtering, Hilbert transformation, two-order quantization and 48 bits self-correlation. The processor calculates 144 channels of correlation, packages the calculation results and provides the AD reference clock, timing control signals and instructions for collectors. Figure 2 is the Digital correlator block diagram.
3.1 Signal sampling board design

The signal sampling board uses XC5VFX130T FPGA as the processing chip, and the clock chip is AD9516. AD9516 has multi-channel output clock distribution function, subpicosecond jitter and low phase noise characteristics. Considering the non-ideal of AD9516, transmission lines and interfaces, the clock to each AD may still be different, so the fine delay adjust function of AD9516 can be used to ensure that the phase difference of each AD clock signal meets the requirements[7]. AD9254 is a single channel 14-bit AD converter chip with low power consumption, low cost and high ENOB, suitable for the application of this correlator[8]. AD sampling rate is 60MHZ, and the isolation degree between different channels can reach 90dB. The GTX high-speed interface inside FPGA is used to transmit 1 bit quantized data, and 8B/10B encoding is adopted, with a line rate of 2.4Gbps[9]. Every sampling board uses two GTXs to transmit the same data to different FPGAs on the processing board. LVDS transmission module is used to receive the timing control signal from the signal processing board, and RS485 module is used to receive the control instruction and send the telemetry information such as self-correlation results. Figure 3 illustrates the block diagram of signal sampling board[10].

Fig.2 Digital correlator block diagram

Fig.3 Block diagram of signal sampling board
3.2 Signal processing board design

The main processing unit of the signal processing board is three XC5VFX130T FPGAs, and the method in chapter 2.2 is used to calculate the correlation coefficient of 144 channels. Each FPGA receives GTX data from different collectors and calculates the correlation. The GTX interconnection relationship between the FPGAs on the processing board and the signal collectors is shown in figure 4. The correlation coefficient between 144 channels of three collectors can be calculated by three FPGAs. The correlation coefficient between two different signals M and N is calculated as follows

\[ P_{MN} = \frac{\text{MI} \cdot \text{NQ} + \text{MQ} \cdot \text{NI}}{\sqrt{\text{MI}^2 + \text{MQ}^2} \sqrt{\text{NI}^2 + \text{NQ}^2}} \]

Where MI and MQ are the I and Q components of channel M signal and NI is the I component of the channel N signal\[11\]. Figure 5 illustrates the block diagram of signal processing board.

The main functions of the signal processing board are as follows:

1) Receive 288 IQ data through GTX high-speed serial interface and calculate the correlation coefficient;
2) Package the correlation results and send them to the computer through RS485 interface;
3) Send instructions to 9 signal sampling boards;
4) Distribute the output clock of the oscillator, and send clock to 9 sampling boards;
5) Generate timing control signals for synchronization and send them to 9 signal sampling boards.

4. The test of multi-channel digital correlator

4.1 Synchronization and ENOB test of ADC

Synchronization and ENOB are critical to the system performance. In the experiment, a sine-wave signal with the frequency of 63M is divided into 16 same signals through the power divider and sent to 16 ADs of a signal sampling board. Chipscope software is used to capture the AD data, and the waveform are shown in the figure 6. In order to analysis the synchronization of each AD, the sampling data is saved and imported to MATLAB software. By using the Fourier transform, the phase difference between the 16 ADs can be calculated at the peak frequency point and converted to the
difference in the time domain. The results show that the unconsistency between 16 AD channels in each signal sampling board is less than 100ps, which meets the requirements. ENOB is calculated with the formula: $\text{ENOB} = \frac{(\text{SINAD}-1.76)}{6.02}$ [12]. Figure 7 illustrates the signal frequency analysis and it is demonstrated that ENOB of AD is greater than 8.5 bits.

![Signals’ digital waveforms](image1)

Fig. 6 Signals’ digital waveforms

![Signal frequency analysis](image2)

Fig. 7 Signal frequency analysis

### 4.2 test of correlation result
Considering the huge number of data associated with the 144 channels, the testing process can be time-consuming. Since the three signal collectors adopt exactly the same design, this paper uses a signal collector and a signal processor to verify the correlation coefficient test results between the 48 channels. The inputs are sine-wave signals in the band by an interval frequency of 2Mhz. Figure 8 illustrates the correlation result at different frequency.

![Correlation coefficient at different frequency](image3)

Fig. 8 Correlation coefficient at different frequency.

### 5. Conclusion
The correlator is the core part of the 2-D synthetic aperture microwave radiometer system. Because of its huge computation volume, it is necessary to study an efficient digital correlator to meet the real-time processing requirements. In this paper, an efficient correlation method is proposed, which can effectively improve the FPGA work efficiency, save hardware resources, and simplify the complexity of digital correlator system.

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