Improved Contacts to Synthetic Monolayer MoS$_2$ – A Statistical Study
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Abstract— Two-dimensional (2D) semiconductors are promising candidates for scaled transistors because they are immune to mobility degradation at the monolayer limit. However, sub-10 nm scaling of 2D semiconductors, such as MoS$_2$, is limited by the contact resistance. In this work, we show for the first time a statistical study of Au contacts to chemical vapor deposited monolayer MoS$_2$ using transmission line model (TLM) structures, before and after dielectric encapsulation. We report contact resistance values as low as 330 ohm-um, which is the lowest value reported to date. We further study the effect of Al$_2$O$_3$ encapsulation on variability in contact resistance and other device metrics. Finally, we note some deviations in the TLM model for short-channel devices in the back-gated configuration and discuss possible modifications to improve the model accuracy.

Keywords—MoS$_2$, contact resistance, 2D semiconductors, transition metal dichalcogenide, transistor

I. INTRODUCTION

To retain electrostatic control with sub-10 nm gates, the channel body thickness should be scaled below 2 nm [1]. Si mobility degrades significantly at thicknesses below 4 nm, whereas two-dimensional (2D) semiconductors such as transition metal dichalcogenides (TMDs) retain good mobility even at the monolayer limit (< 1 nm thick), making them attractive for use in scaled channels [2]. TMDs such as MoS$_2$ have been extensively studied for use in scaled field-effect transistors because its significant band gap (~1.5 to 2.5 eV) can enable lower leakage power compared to other low-dimensional semiconductors. TMDs can also be directly grown on Si CMOS substrates, without requiring transfer steps like other low-dimensional materials [3], [4], making them attractive for 3D integration.

However, monolayer TMDs are severely limited by contact resistance, characterized by a Schottky-barrier at the metal-semiconductor interface in sub-100 nm channels. This is due to the pinning of the metal Fermi level at the MoS$_2$ interface below the conduction band edge [5]. Au contacts have been shown to make good contacts to 1L MoS$_2$ [2], [6], [7]. However, a systematic statistical study of variation in contact resistance has yet been done. In this work, we study variation in Au contacts to chemical vapor deposited 1L MoS$_2$ and discuss the effects of atomic layer deposited (ALD) Al$_2$O$_3$ encapsulation on contact resistance. We observe that encapsulation reduces the contact resistance as well as its variability. We report the lowest contact resistance ($\approx 330 \pm 24 \Omega \mu$m) on 1L MoS$_2$ to date and also discuss the accuracy of the TLM model as it is applied to back-gated 2D transistors.

II. EXPERIMENTAL METHODS

A. MoS$_2$ growth

Continuous 1L MoS$_2$ films are grown at 750 °C on 50 nm SiO$_2$ thermally grown in dry O$_2$ on p$^{++}$ Si substrates by solid source chemical vapor deposition (CVD). The growth technique utilizes solid sulfur and molybdenum trioxide precursors with nucleation aided by a perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) seed layer [3]. The number of MoS$_2$ layers is confirmed by the Raman spectrum shown in Fig. 1 (b).

B. Device Fabrication

We fabricated TLM structures [8] consisting of back-gated transistors with channel lengths ranging from 100 nm to 1 µm as shown in the scanning electron microscope (SEM) image in Fig 1(a). All patterning steps were done using e-beam lithography. Contact probe pads were first patterned followed by etching away MoS$_2$ in the exposed contact regions using XeF$_2$ vapor. 2 nm Ti / 40 nm Au was deposited by e-beam evaporation at a base pressure of $\approx 10^{-7}$ Torr. This was followed by overnight liftoff in acetone. Rectangular channels 2 µm wide were then patterned and etched by XeF$_2$. In the same step, the contact pads were isolated from the rest of the MoS$_2$ film by etching away the MoS$_2$ around the pads. Fine contacts were then patterned and 50 nm Au was deposited at a rate of 0.5 A/s by e-beam evaporation at $\approx 10^{-7}$ Torr base pressure. The metal was lifted off in acetone. Finally, the sample was annealed at 250 °C for 2 hours in vacuum in a Janis vacuum probe station to remove adsorbates from the MoS$_2$ surface [2].

C. Dielectric Encapsulation

The chips were encapsulated with atomic layer deposited (ALD) Al$_2$O$_3$. First, a seed layer of 1.5 nm Al was deposited by e-beam evaporation. This layer was oxidized into AlO$_x$ by exposing it to the ambient. 20 nm Al$_2$O$_3$ was subsequently deposited by 200 cycles of ALD at 300 °C after a 300 °C anneal for 30 minutes. The final device structure is shown in Fig. 1(c).

![Fig. 1. (a) Scanning electron microscope (SEM) image of a TLM structure with channel lengths ranging from 100 nm to 1 µm. The contact lines are 1.5 µm in width and the MoS$_2$ channel is 2 µm in width. Scale bar is 5 µm. (b) Raman spectrum of 1L MoS$_2$ grown by CVD at 750 °C on 50 nm SiO$_2$/Si. (c) Schematic cross-section of the final device structure after Al$_2$O$_3$ encapsulation.](image-url)
D. Electrical Testing

Electrical testing was carried out in a Cascade Microtech Summit semi-automated probe station with an Agilent B1600A parameter analyzer. After loading the chip, the probe station was purged with N₂ for 30 minutes before starting the measurements to ensure the removal of moisture from the MoS₂ surface. The chip contains 72 TLM structures, each containing 6 channel lengths – 100 nm, 200 nm, 300 nm, 500 nm, 700 nm and 1 µm – a total of 432 transistors. The devices were tested before and after the encapsulation with Al₂O₃.

III. RESULTS AND DISCUSSION

Fig. 2 shows the drain current (I_D) vs gate to source voltage (V_GS) transfer characteristics measured before and after the Al₂O₃ encapsulation for each channel length. The encapsulation results in a threshold voltage (V_T) shift, indicating that the Al₂O₃ layer causes mild n-type doping in the channel. Fig. 3(b) also shows the V_T shift in 100 nm channels due to encapsulation. Previous works have shown that defective ALD Al₂O₃ deposited at low-temperatures cause n-type doping in sulfur-based TMDs [6], [9], [10].

Because Al₂O₃ is used here for purposes of encapsulation only, Al₂O₃ was deposited at a higher temperature of 300 °C which leads to a relatively less defective film, therefore reducing the doping effect. Significant on-off ratio is retained as well without any post-encapsulation anneal [6].

For each TLM structure, the contact resistance was extracted from the I_D-V_GS characteristics by first aligning the threshold voltages of all the channels in that TLM structure and then carrying out linear regression of the total resistance versus channel length. The MoS₂ film shows spatial variation across the chip in grain size, film coverage and proportion of bilayer island regions [11]. Therefore, it is important to have each TLM structure spatially localized to minimize the variation across its channel lengths. Fig. 3 shows the cumulative density function (CDF) plot of the extracted contact resistances for all TLM structures, extracted at a carrier density n = 8.3x10¹² cm⁻². We discarded TLM fits with R-squared less than 0.9 while relatively few TLM structures had R-squared > 0.9 before encapsulation. The median contact resistance is 3.2 kΩ.μm.

The CDF plot shows that encapsulation reduces the average contact resistance as well as the variation across the chip when compared at the same carrier density level. This could be due to two reasons. First, encapsulation improves the sheet resistance at the same carrier density due to improvement in the effective mobility as shown in Fig. 3(c). This improvement in mobility is due to effective screening of charged impurities in MoS₂ by the high dielectric constant Al₂O₃ layer [12], [13]. This leads to a larger proportion of the drain-to-source voltage dropped across the Schottky contacts, which leads to a lower contact resistance. Second, the Schottky barrier height might be reduced due to induced strain in the MoS₂ due to built-in tensile stress from the encapsulation layer. [14], [15], [16]

![Fig. 2. Measured transfer characteristics (I_D - V_GS) for channel lengths (a) 100 nm, (b) 200 nm, (c) 300 nm, (d) 500 nm, (e) 700 nm and (f) 1 µm; blue (red) curves are measured before (after) Al₂O₃ encapsulation. All measurements are done with a V_GS of 0.1 V at room temperature with N₂ purging.](image)

![Fig. 3. Cumulative density function (CDF) plot for various device metrics before (blue) and after (red) encapsulation. (a) CDF plot of contact resistance values extracted from TLM structures at carrier density n = 8.3x10¹² cm⁻². Each datapoint in the curve corresponds to contact resistance extracted from a single TLM structure and the horizontal error bars are obtained from the standard error of the respective linear regression parameters. (b) CDF plot of threshold voltages (V_T) in 100 nm channels shows moderate doping due to Al₂O₃ layer. (c) CDF plot of effective mobility at carrier density n = 8.3x10¹² cm⁻².](image)
on since the effect on  

gate capacitance is significant  

resistance of the various channels using their threshold voltages  

of total resistance. The TLM model requires modifications  

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330 ± 24 Ω.µm at n = 1.4x10^{17} cm^{-2}.  

We achieve a low value of R_c  

2.75 ± 0.16 kΩ.µm.  

fabrication, material characterization were performed at the  

ime to account for the fringing electric field in the back gate capacitor and the effects of contact-gating on extracted V_T. These effects become quite significant in short channel devices.

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