LC-NAS: Latency Constrained Neural Architecture Search for Point Cloud Networks

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Abstract. Point cloud architecture design has become a crucial problem for 3D deep learning. Several efforts exist to manually design architectures with high accuracy in point cloud tasks such as classification, segmentation, and detection. Recent progress in automatic Neural Architecture Search (NAS) minimizes the human effort in network design and optimizes high performing architectures. However, these efforts fail to consider important factors such as latency during inference. Latency is of high importance in time critical applications like self-driving cars, robot navigation, and mobile applications, that are generally bound by the available hardware. In this paper, we introduce a new NAS framework, dubbed LC-NAS, where we search for point cloud architectures that are constrained to a target latency. We implement a novel latency constraint formulation to trade-off between accuracy and latency in our architecture search. Contrary to previous works, our latency loss guarantees that the final network achieves latency under a specified target value. This is crucial when the end task is to be deployed in a limited hardware setting. Extensive experiments show that LC-NAS is able to find state-of-the-art architectures for point cloud classification in ModelNet40 with minimal computational cost. We also show how our searched architectures achieve any desired latency with a reasonably low drop in accuracy. Finally, we show how our searched architectures easily transfer to a different task, part segmentation on PartNet, where we achieve state-of-the-art results while lowering latency by a factor of 10.

1 Introduction

Deep learning is the de facto choice for solving vision related tasks. In particular, Convolutional Neural Networks (CNNs) achieve state-of-the-art results in 2D image classification [13,41], segmentation [4,36], and detection [12,35]. Recent efforts translated this success to 3D point clouds. The seminal PointNet work [33] opened the way to increasingly performing architectures for processing point clouds. Similar to the 2D case, state-of-the-art architectures achieve impressive gains in point cloud classification [25], segmentation [45], and detection [8,37]. However, this success comes at the expense of increased computation. Of particular interest is the computational latency during inference, a factor that is paramount to time-critical applications like self-driving cars, robot navigation,
and mobile applications (Fig. 1). These applications require fast decision making and have access to limited hardware. It is thus imperative to equip them with latency optimized architectures.

One potential avenue to optimize architectures is through Neural Architecture Search (NAS). In an effort to design better deep learning architectures, NAS provides automated approaches to construct these architectures. Early works based on Reinforcement Learning showed promising results in this area [59]. Although encouraging in their results, early NAS approaches were limited by their massive computational needs. Recent works like DARTS [27] and its variants [50, 3, 23, 58, 54, 6] formulate architecture search as a differentiable problem, which greatly alleviates computational complexity. Further advancements are proposed in recent work like SGAS [23], where optimal architectures show better generalization between search and final tasks. SGAS is also the first work to perform NAS on point cloud architectures. Whatever their underlining processes, these NAS techniques optimize architectures that increase accuracy on a specific task. This approach does not take into account other constraints like latency. For point cloud architectures in hardware bounded applications, it is beneficial to have NAS frameworks that constrain the latency of the output models.

Few works exist in the literature that formulate latency constrained NAS frameworks. Some of these works use a lookup table to obtain the latency of each operation, and approximate the total latency as a sum of all individual latencies [3, 18]. However, these methods are only able to predict latency for chain-style architectures since they ignore the architecture’s topology. Other works use more complicated approaches based on reinforcement learning [59]. These approaches
are unsuitable for large and complex search spaces such as directed acyclic graph (DAG) - style architectures. In the DAG space, network latency depends not only on its operations but also on its topology. Therefore, simply aggregating individual latencies is a bad approximation of the total network latency. We alleviate this problem by first introducing a latency regressor that is able to accurately predict a point cloud architecture latency. We then incorporate this regressor as part of a differentiable NAS optimization pipeline. We use a hinge latency loss to constrain the output latency to a desired target. We demonstrate the benefits of our loss formulation compared to other approaches in Section 4. Moreover, our latency aware formulation enables search for point cloud architectures with latencies specific to any desired hardware.

In this work, we propose a framework to constrain point cloud NAS methods in order to increase accuracy and minimize latency. We achieve this by introducing a differentiable latency estimator, which can be used to define targeted latency constraints in NAS pipelines. Since these constraints are targeted, i.e., we can specify a target latency for the optimal architecture, we can now use NAS solutions to search for the best architecture under a given latency constraint. This effectively allows us to move along the trade-off curve between accuracy and latency to an optimal point for any given application. In this paper, we add our latency constraint to SGAS, in order to find latency aware Graph Convolutional Networks (GCNs), that effectively operate on point clouds. We dub this new framework Latency Constrained Neural Architecture Search (LC-NAS). Note that although we use SGAS in this work, our latency constraints can easily be incorporated into most NAS approaches. We show how LC-NAS can create point cloud architectures with a range of targeted latencies, while still maximizing accuracy in the end task (Section 4.2). Although the LC-NAS architectures are optimized for point cloud classification, we show how they successfully transfer to the task of point cloud part segmentation (Section 4.3). Such transferability is a testament to the power of our approach.

Contributions. We summarize our contributions as three-fold. (1) We propose a novel latency constraint to point cloud NAS pipelines. We show how we can incorporate our constraints in LC-NAS, a novel framework on top of SGAS to output GCNs for point cloud processing. LC-NAS can successfully output architectures with a target latency, while increasing the accuracy of a downstream task. (2) We use LC-NAS to search for optimal point cloud classification architectures under a range of target latencies. Our output architectures achieve state-of-the-art results on the ModelNet40 dataset, while significantly reducing latency of the final architecture. (3) We successfully transfer the models learned for classification to the task of part segmentation on PartNet, where we also obtain state-of-the-art results in both accuracy and model latency. To the best of our knowledge, we are the first to propose a latency constrained NAS framework for point cloud tasks.
2 Related Work

NAS. Hand-crafted deep learning architectures have achieved considerable success in a wide range of tasks [13, 15, 18, 20, 38, 40]. These innovations were results of human intelligence and experimentation. Initial works based on reinforcement learning attempted to automate the process of architecture search [59]. NASNet [60] and ENAS [31] proposed to look for neural architectures in a cell-based search space, and applied regularization and weight sharing techniques to increase search efficiency. PNAS [26] used a sequential model-based optimization (SMBO) strategy to search for structures of increasing complexity. PNAS can reduce computational cost by a factor of 8 compared to NASNet. However, it still requires thousands of GPU hours. Many recent works [2, 1, 3] aim to reduce the search time by training a single over-parameterized network with inherited/shared weights. For example, DARTS [27] and its variants [50, 30, 12, 58, 5, 23, 54, 6] relaxed the architecture representation to the continuous domain to make the search differentiable. Recenly, NAS has been explored in 3D [23, 43]. In our study, we pick SGAS [23] as the baseline method to take advantage of its high efficiency and generalization ability.

Resource constrained NAS. Considering the hardware limitation, NAS can be implemented with extra constraints such as FLOPs and latency. SNAS [50] included a resource-constrained regularization in their differentiable optimization. It represented the cost of time by the parameter size, number of FLOPs, and memory access cost (MAC). In ProxylessNAS [3], FBNet [48] and Single-Path NAS [39] approximate the latency of networks as the sum of the latency of every layers by a latency lookup or a learned operation latency predictor. However, these approaches fail to estimate latency for DAG-style architectures. In MnasNet [42], real-world latency of each sampled model is measured by running it on a single-thread big CPU core of Pixel 1 phones in the training phase. In contrast to these methods, LC-NAS learns an end-to-end differentiable latency regressor for DAG-style architectures, and adopts a loss function with a target latency as a soft constraint. More concurrent works also try to address latency constraints for DAG-style architectures [55] or target latency [14].

Deep Learning on Point Clouds. PointNet [33] provided the first solution for deep learning directly on point clouds. PointNet operates on point cloud chunks, computing point features, and later aggregates them with an order-invariant operation like max pooling. Each point feature is computed using an MLP, without including information from its neighborhood. Because of the nature of this computation, PointNet falls into a group of Pointwise Networks. Within this division fall works with more complex aggregation methods, either by looking at more local context [34, 10] or using complex aggregations through RNNs [16, 56]. More recent works define convolution operators based on local spatial relationships. These methods fall under the category of Point Convolution Networks. They use local structure to define more versatile convolutional kernels, and have proven very successful in pushing the state-of-the-art in point cloud tasks [44, 45, 57, 25, 53, 24]. A third type of algorithm leverages the power of Graph Convolutional Networks (GCNs). We choose to work with GCNs in
this paper given their high versatility in designing different operators, and their proven results in previous NAS approaches [23]. Following is a brief survey of GCNs and their applications.

Graph Convolutional Networks (GCNs). Recent years have seen a surge of non-Euclidean data in real-world scenarios. Such representation is prime for GCNs, where convolution operators are designed to work with generic graph representations of data. Several such GCNs exist in the literature for a wide number of applications [17,11,46,32,52]. In the area of point clouds, DGCNN [47] introduced EdgeConv, and used it to conduct dynamic graph convolution on point clouds. Recently, DeepGCNs [22,21] integrated residual/dense connections and dilated convolutions into GCNs for point clouds. These integrations enabled them to successfully train GCNs of up to 112 layers. The operations in DGCNN and DeepGCNs were used in SGAS to search for optimal GCNs, and we similarly apply them in LC-NAS for our latency constrained architectures.

Fig. 2. LC-NAS pipeline. We sample a large number of architecture from our defined search space and measure their latencies. We use these architectures to train a latency predictor. Our predictor takes as input a binary encoding of the architecture and provides a latency measure. We integrate this predictor as a constrain into the NAS loss, where the target latency is part of the loss. We optimize our pipeline to discover point cloud architectures that meet a target latency. With this targeted approach, we can easily trade-off between accuracy and latency, and discovery models specific to a given deployment architecture.
3 Methodology

3.1 Preliminary - Sequential Greedy Architecture Search

In order to calibrate mismatching rankings between architectures during the search phase and the evaluation phase, *Sequential Greedy Architecture Search* (SGAS) [23] proposes to solve the bi-level optimization in DARTS in a sequential greedy fashion. Following DARTS, SGAS searches for cells and composes networks by stacking cells with identical structure. A cell is typically represented as a directed acyclic graph (DAG) with \( N \) nodes including two input nodes, several intermediate nodes and one output node. The \( i \)-th topological ordered node in the DAG is an intermediate feature representation denoted as \( x^{(i)} \). Each directed edge \((i, j)\) in the DAG represents an operation \( o^{(i,j)} \) that transforms \( x^{(i)} \). Each intermediate node \( x^{(j)} \) is computed by summing up the outputs of all the edges from its predecessors, \( x^{(j)} = \sum_{i<j} o^{(i,j)}(x^{(i)}) \). By parameterizing operation \( o^{(i,j)} \) with architectural parameters \( \alpha^{(i,j)} \) over the space of all the candidate operations \( \mathcal{O} \), DARTS turns the architecture search into a differentiable form. During the search phase, the operation \( o^{(i,j)} \) is relaxed as a mixture operation, \( \bar{o}^{(i,j)}(x^{(i)}) = \sum_{o \in \mathcal{O}} \frac{\exp(\alpha^{(i,j)} o)}{\sum_{o' \in \mathcal{O}} \exp(\alpha^{(i,j)} o')} o(x^{(i)}) \). After the search, the discrete architecture is obtained by choosing a non-zero operation with the highest weight for every mixture operations, \( o^{(i,j)} = \arg\max_{o \in \mathcal{O}} \alpha^{(i,j)} o \). However, the discrepancy between the search and evaluation phases and the negative effect of weight sharing in DARTS make the searched architectures fail to generalize in the final evaluation. In order to alleviate these problems, SGAS proposed to determine and prune operations progressively during the search phase in a greedy fashion. Theoretically, we can use any differentiable methods such as DARTS [27] or its variants [5,50,54]. However, we opt to choose SGAS as our base method (as opposed to DARTS for example) for its efficiency and more stable results.

3.2 Latency Constrained Neural Architecture Search

The goal of our work is to automatically design a well-performing GCN architecture that is able to run on a specific hardware platform within a given target latency. To achieve this goal, we need to take the latency constraint into consideration in the optimization during the search phase. As mentioned, previous works either build a lookup table for the latency of each operations and approximate the latency by summing up corresponding latency sequentially, or use reinforcement learning to optimize the latency by treating it as a part of the score. However, none of them is feasible to apply to differential NAS methods with a search space as a DAG, since the latency of a network with a general DAG structure depends on its topology and can not be estimated by simply summing up the latency of each operations. To this end, we propose to first learn a latency regressor that is able to predict the latency of all the possible architectures on a specific device within the search space. And then we incorporate the learned latency regressor as a constraint in the bi-level optimization objective and regularize the architectural parameters \( \mathcal{A} = \{ \alpha^{(i,j)} \mid \forall (i,j) \} \).
**Search Space.** We use the same search space as SGAS. Each edge in our graph convolutional cell has 10 candidate operations including Skip-Connect, Conv-$1\times1$, EdgeConv [47], MRConv [22], GAT [46], SemiGCN [17], GIN [51], SAGE [11], RelSAGE [23] and Zero. Please refer to the original SGAS paper [23] for more details of these GCN operators. K Nearest Neighbours (KNN) is used to take the input vertex/point features of a cell to build a KNN graph by constructing dynamic edges. Obtained edges are then shared with others operations within the cell. Following DeepGCNs [22], dilated graph convolutions with a linearly increasing dilation rate is used in cells. In our experiment, each cell contains $N = 6$ nodes with 3 intermediate nodes and 9 edges during the search phase. For each intermediate node in the DAG, we retain 2 incoming edges after the search process. Therefore, we will obtain a DAG with 6 edges at the end of the search process. There are about 18 million possible architectures in this search space. It is impossible to enumerate or measure the latency of these millions of architectures. Therefore, we propose to train a latency approximator from the data itself. To learn a precise latency regressor, we need to first sample sufficient architectures from the search space and measure their latency to create a dataset. Then we can train a regression network that takes an architecture encoding as input and output the predicted latency.

**Architecture Encoding.** To encode the model architectures, we need to encode the graph convolutional cell, the basic building block in cell-based neural architecture search. Our search space is a DAG with 9 edges and 10 candidate operations for each edge. After the search, 6 edges are retained in total. Thus, we can use a $9 \times 10$ binary encoding matrix $E \in \{0, 1\}^{9 \times 10}$ to represent the cell, where $e_{m,n} = 1$ indicates that the operation $n$ is chosen for the edge $m$. Since we only retain 6 edges, the encoding matrix $E$ a sparse matrix with exactly 6 entries with values of 1.

**Latency Regressor.** In this work, we consider point cloud classification on ModelNet40 as our target task and NVIDIA RTX 2080 as our target hardware platform. We sample and measure 100K random cell-architectures from the search space. We stack the sampled cell 3 times with a channel size of 128. For more details about the model hyper-parameters, please refer to the experiment Section 4.2. The latency is measured by the inference time of the sampled architectures with randomly initialized weights and a random tensor of shape $(\text{batch size} = 1, \text{feature dims} = 3, \text{num of points} = 1024)$. The data is then split into three folds with 60% as the training subset, 20% as the validation subset, and 20% as the testing subset. The latency ranges from 5.9 to 23.5 milliseconds (ms). We leverage a Multi Layer Perceptron (MLP) as our latency regressor (LatReg). Given the encoding matrix $E$, we first vectorize $E$ and feed it into three fully-connected layers. We respectively set 256, 128 and 1 neurons in each of the three layers, interleaved with sigmoid activation functions. Finally, the MLP produces one scalar value as the latency prediction. During training, we normalize the latency by the mean $\mu_{\text{train}} = 15.32\text{ms}$ and the standard deviation $\sigma_{\text{train}} = 2.24\text{ms}$. We train the network from scratch, and set the batch size to 256. We employ Adam optimizer in PyTorch with the default parameters: learning rate equal to 0.001 and betas equal to $(0.9, 0.999)$. We use mean square error
(MSE) as the loss function. From the loss curve of the validation set, we find the model saturated efficiently on the 70-th epoch. The LatReg model reaches an average absolute error of 0.16ms on the test subset.

**Loss function with a Target Latency as Constraint.** The learning procedure of neural architecture search can be formulated as a bi-level optimization problem [27]. Previous resource-aware differentiable NAS methods usually add/multiply the latency loss as a regularizer to the cross-entropy loss [3,4,50]. However, these methods are not able to minimize the architecture to be lower than a certain latency, which is considered to be very important for the deployment on a specific hardware platform. Moreover, the regularization weight is hard to tune. A big regularization weight leads to efficient/fast models but with low capacity. On the other end, a small regularization weight fails to obtain efficient models. Therefore, we propose to use a hinge-loss-like regularization loss for the latency constraint as follows:

$$\min_{\mathcal{A}} \mathcal{L}_{val}(W^*(\mathcal{A}), \mathcal{A}) + \lambda \max(\text{LatReg}(\mathcal{E}(\mathcal{A})) - \text{target}, 0) \quad (1)$$

s.t. $$W^*(\mathcal{A}) = \arg\min_{W} \mathcal{L}_{train}(W, \mathcal{A}) \quad (2)$$

where $\mathcal{L}_{val}$ is the cross-entropy loss on validation set, $\mathcal{L}_{train}$ is the cross-entropy loss on training set, $\mathcal{A}$ is the architectural parameters, $W$ is the network weights, $\lambda$ is the regularization factor, $\text{LatReg}(\cdot)$ is the learned latency regressor, $\text{target}$ is the target latency and $\mathcal{E}(\cdot)$ is a non-differentiable binarized function that take as input continuous architectural parameters $\mathcal{A}$ and output a binarized architecture encoding $\tilde{\mathcal{E}}$. The advantages of this hinge latency loss are as follow: (1) Once the predicted latency is lower than the target latency, the latency loss term is zero and the bi-level optimization reduces into the original objective function. This reduces the risk of harming the model capacity. (2) For the same reason, the regularization factor $\lambda$ becomes less sensitive and easy to tune. (3) Incorporating a target latency into the latency loss makes the architecture search more controllable and deployable on a hardware of desired specific latency. Binarizing the continuous architectural parameters $\mathcal{A}$ before predicting the latency is necessary since $\text{LatReg}(\cdot)$ is trained on binary inputs. If we use $\mathcal{A}$ as input, the latency prediction of $\text{LatReg}(\cdot)$ would in inaccurate due to the discrepancy between continuous architectural parameters and the binary architecture encoding. However, the binarized function $\mathcal{E}(\cdot)$ is non-differentiable since it involves some rules/heuristics to derive a discrete architecture encoding such as choosing 6 edges out of 9 and selecting a non-zero operation with the highest weight. In order to obtain the gradient of the latency loss with respect to architectural parameters $\mathcal{A}$, we introduce an approximated gradient-based approach.

**Optimizing the Latency Constraint.** As mentioned, the binarized function $\mathcal{E}(\cdot)$ is non-differentiable. It mainly includes a softmax operation over architectural parameters, choosing two edges for each intermediate nodes based on pre-defined rules/heuristics and selecting a non-zero operation with the highest weight for the corresponding edge. The parts of choosing edges and operations make $\mathcal{E}(\cdot)$ non-differentiable. One conventional way to update the real-valued weight $\mathcal{A}$ is to use the gradient with respect to its binarized value $\tilde{\mathcal{E}}$ which is
proposed in BinaryConnect \cite{russakovsky2015imagenet} and has also been used ProxylessNAS \cite{liu2018proxylessnas}. However, this approach does not take real-valued weight into consideration while computing the gradient. We propose a modified approximated gradient-based approach to optimize the architectural parameters. We denote the softmax output of $\beta_{m,n} = \text{softmax}(\alpha_{m,n}|\alpha_m) = \frac{\exp(\alpha_{m,n})}{\sum_k \exp(\alpha_{m,k})}$, where $\alpha_{m,n}$ is the architectural parameter of operation $n$ of edge $m$. To compute the gradient of $E(\cdot)$ with respect to $A$, we trust the selection rules/heuristics as a linear operation by approximating with multiplying an element-wise mask $\zeta$, where $\zeta_{m,n} = 1$ if $n = n^*$ and $\zeta_{m,n} = 0$ if $n \neq n^*$. Note that $n^*$ is the chosen operation of edge $m$. Therefore the binarized function becomes $E(\alpha_{m,n}) = \tilde{e}_{m,n} \approx \beta_{m,n} \cdot \zeta_{m,n}$ and the gradient can be obtained. We denote the latency loss term as $L_{\text{lat}}$. We have:

$$\frac{\partial L_{\text{lat}}}{\partial \alpha_{m,n}} = \sum_k \frac{\partial L_{\text{lat}}}{\partial \beta_{m,k}} \cdot \frac{\partial \beta_{m,k}}{\partial \alpha_{m,n}} = \sum_k \frac{\partial L_{\text{lat}}}{\partial \tilde{e}_{m,k}} \cdot \frac{\partial \tilde{e}_{m,k}}{\partial \beta_{m,k}} \cdot \frac{\partial \beta_{m,k}}{\partial \alpha_{m,n}}$$

(3)

where $\frac{\partial \beta_{m,k}}{\partial \alpha_{m,n}} = \beta_{m,n} - \beta_{m,n}^2$ if $n = k$ and $\frac{\partial \beta_{m,k}}{\partial \alpha_{m,n}} = -\beta_{m,n} \cdot \beta_{m,k}$ if $n \neq k$. Since $\frac{\partial \tilde{e}_{m,k}}{\partial \beta_{m,k}} = \zeta_{m,k}$. We obtain the gradient as follows:

$$\frac{\partial L_{\text{lat}}}{\partial \alpha_{m,n}} = \frac{\partial L_{\text{lat}}}{\partial \tilde{e}_{m,n^*}} \cdot \frac{1}{\beta_{m,n^*}} \cdot \frac{\partial \beta_{m,n^*}}{\partial \alpha_{m,n}} = \begin{cases} \frac{\partial L_{\text{lat}}}{\partial \tilde{e}_{m,n^*}} \cdot (1 - \beta_{m,n^*}) & \text{for } n = n^* \\ \frac{\partial L_{\text{lat}}}{\partial \tilde{e}_{m,n^*}} \cdot -\beta_{m,n} & \text{for } n \neq n^* \end{cases}$$

In this way, we can update the architectural parameters $A$ using the gradient above. Therefore, the latency constraint can be optimized during search.

4 Experiments

As mentioned in Section 3.2, our target task is classification on ModelNet40 using NVIDIA RTX 2080. We sample 100K architectures from the search space and measure their latency to build a dataset. Then, we train a latency regressor on the latency dataset. After that, we use the pre-trained latency regressor to constrain the architecture search on ModelNet10 with latency targets on ModelNet40 ranging from 6ms to 18ms. We then evaluate the performance of obtained architectures on ModelNet40 by training from scratch. We also transfer our architectures to a completely different task, part segmentation, to show the generalization of the architectures. Finally, we conduct a thorough ablation study to demonstrate the effects of regularization strength, loss function, and the choice of hyper-parameters for our models.

4.1 LC-NAS on ModelNet10

Dataset. ModelNet \cite{wu20153d} is a classical dataset for 3D point cloud classification, which has two subsets ModelNet10 and ModelNet40 containing objects with 10 and 40 classes respectively. ModelNet10 comprises 4,899 3D models split into 10 classes, with 3,991 models in training and 908 models in testing. ModelNet40
consists of 12,311 models split into 40 classes, with 9,843 models in training and 2,468 in testing. The goal of classification on ModelNet datasets is to classify the category of a 3D model. We first search GCN architectures on ModelNet10 using LC-NAS and evaluate their performance on ModelNet40.

**Training Settings.** During the training of the search phase, 1024 points with only 3D coordinates \((x, y, z)\) are sampled from the 3D models in ModelNet10 as input. We set the regularization factor \(\lambda\) as 0.5 and vary the target latency from 6ms to 18ms with a step of 2ms. The other settings follow those of SGAS. We use 2 cells with 32 initial channels and search for the architectures for 50 epochs with batch size 28. Two different optimizers are used for optimizing model weights \(W\) and \(A\). We use SGD with initial learning rate 0.005, momentum 0.9, and weight decay \(3 \times 10^{-4}\) to optimize the model weights. An Adam optimizer with an initial learning rate \(3 \times 10^{-4}\), momentum \((0.5, 0.999)\), and weight decay \(10^{-3}\) is used for architecture parameters \(A\). We use the same edge selection criterion as SGAS **Criterion 2**. LC-NAS begins to determine one operation for a selected edge every 7 epochs after warming up for 9 epochs. A history window of size 4 is used for **Selection Stability**. We increase the batch size by 4 after each decision. The total time for a search run is around 0.19 GPU days on a single NVIDIA GTX 1080Ti, which is the same for SGAS. This means the extra computation overhead of adding the latency constraint is negligible.

### 4.2 Architecture Evaluation on ModelNet40

After searching on ModelNet10, we get 7 searched cell structures with target latency 6ms, 8ms, 10ms, 12ms, 14ms, 16ms and 18ms respectively. We build a large network for each cell with the same hyper-parameters that are used to generate the architecture for learning the latency regressor. We then train them on ModelNet40 from scratch. We evaluate the performance on ModelNet40 using two metrics: the overall accuracy (O.A.) and class accuracy (Class ACC.).

**Training Settings.** 1024 points with 3D coordinates are used as input. We stack the searched cell 3 times with channel size 128. An MLP with 1024 neurons is used to fuse the concatenation of all the output features of 3 cells. And then, the fused features are aggregated through a max-pooling layer and an average pooling layer. We concatenate the aggregated features from two pooling layers and feed them into a 3-layer MLP classifier with \{512, 256, 40\} neurons to classify the input point clouds into 40 categories. For the first two MLP layers, we use dropout layers with probability 0.5 during training. A drop path is applied with probability 0.2. SGD is used to optimize the model weights with initial learning rate 0.1, momentum 0.9, and weight decay \(1 \times 10^{-4}\). We use a cosine annealing learning rate scheduler with a minimum learning rate of 0.001. Our architectures are all trained for 400 epochs with batch size 32.

**Evaluation Results and Analysis.** We report the best overall accuracy (O.A.) and the corresponding class accuracy (Class ACC.) on the test dataset for all the 7 discovered architectures in Table 1. We observe in Table 1 that LC-NAS is able to meet the target latency in the vast majority of cases (only exception is LC-NAS-10, where the actual latency is only over target by 1ms). We also show
strong accuracy results, and a meaningful trend of dropping accuracy as target latency increases. We also compare our discovered architectures with state-of-the-art results in Table 2. We see how LC-NAS can obtain low latency and still maintain competitive results in terms of accuracy. Particularly, we observe how we drop the baseline latency (SGAS in Table 2) from 16.62ms to 5.47ms with an accuracy drop of less than 3 points. In a real-world scenario, where such architectures need to be deployed in hardware-bounded applications, LC-NAS provides architectures suitable for latency bound scenarios.

Table 1. Evaluation Results on ModelNet40. We show results obtained on ModelNet40 using architectures discovered on different target latencies. We report the target latency, predicted latency by our latency regressor, actual measured latency, and number of parameters. We also show overall accuracy and class accuracy. We observe that our architectures consistently meet the target constraint while achieving high accuracy.

| Method     | Latency (ms) | # Param. | Accuracy |
|------------|--------------|----------|----------|
|            | Target       | Predicted| Measured |
| LC-NAS-18  | 18           | 17.06    | 16.66    | 3.91 | 92.79 | 89.66 |
| LC-NAS-16  | 16           | 13.71    | 13.57    | 3.91 | 92.62 | 90.13 |
| LC-NAS-14  | 14           | 12.64    | 12.41    | 3.91 | 92.42 | 89.16 |
| LC-NAS-12  | 12           | 10.07    | 9.96     | 3.85 | 92.34 | 89.57 |
| LC-NAS-10  | 10           | 11.02    | 11.09    | 3.86 | 92.75 | 90.76 |
| LC-NAS-8   | 8            | 7.84     | 7.51     | 3.71 | 90.40 | 85.36 |
| LC-NAS-6   | 6            | 6.12     | 5.47     | 3.61 | 90.51 | 84.71 |
| Average    | -            | 11.21    | 10.95    | 3.82 | 91.98 | 88.48 |

Table 2. Comparison to state-of-the-art methods. We measure the latencies of state-of-the-art architectures on ModelNet40 with their reported accuracies. SGAS is our baseline since it is equivalent to our approach without any constraints. We show the significant latency reduction of SGAS while maintaining comparable accuracies.

| Method        | Latency (ms) | Overall Acc. |
|---------------|--------------|--------------|
| PointNet [33] | 4.21 ms      | 89.2         |
| PointNet++    | 23.51 ms     | 90.7         |
| DGCNN [47]    | 9.42 ms      | 92.2         |
| PointCNN [25] | 26.79 ms     | 92.2         |
| ShellNet [57] | 9.29 ms      | 93.1         |
| KPConv [45]   | 26.81 ms     | 92.9         |
| SGAS [23]     | 16.62 ms     | 92.9         |
| RS-CNN* [28]  | -            | 92.4         |

*We report the single vote performance for fair comparison.

We visualize in Fig. 3 samples from the resulting discovered architectures. As expected, we observe an increase in the complexity of operations as the target latency increases. For example, with target latency of 6ms (LC-NAS-6), we observe that the majority of operations are $1 \times 1$ convolutions and skip connections...
We show the cell operations of 4 architectures discovered with 4 target latencies, 6ms, 10ms, 14ms, and 18ms (denoted by LC-NAS-6, LC-NAS-10, LC-NAS-14, and LC-NAS-18 respectively). We observe how the operations increasing in complexity as the target latency increases. Low latency architectures favor $1 \times 1$ convolutions and skip connections, while the larger ones go for complex GCN operations like MRConv and EdgeConv.

to satisfy such a low latency budget. As we increase the latency to 18ms, the observed operations become complex and time-consuming like MRConv, GAT, and GIN. Architectures in between mix between simple and complex operations in order to meet the target latency. The results are visual validations that LC-NAS discovers meaningful architectures in line with the required constraints.

4.3 Transferring Searched Architectures to Part Segmentation

The LC-NAS architectures searched on ModelNet10 are transferred for the task of Part Segmentation, in particular on the PartNet benchmark [29].

Dataset. PartNet is composed of 24 object classes with 1, 2 or 3 difficulty levels for each classes. We focus exclusively on the 17 object classes with the highest difficulty level 3. Each model takes point clouds of 10000 points.

Training Settings. We train a model for each object class, as common practice [29], since each object has a different number of parts. We adapted the PyTorch implementation from [21]. We train each model for 500 epochs with an initial learning rate of 0.005 and a decay factor of 0.9 every 50 epochs. We use the PyTorch Adam optimizer with default values.

Evaluation Results and Analysis. We report the performances of our LC-NAS architectures (Part mIOU) and compare with related works in Table 3. LC-NAS achieves state-of-the-art performance on 12 classes, and enjoys an average part mIOU of 48.55%. We outperform the baseline PointCNN [25] by up to 2.06% with $\sim 10 \times$ speedup. PointCNN is not able to scale efficiently due to the numerous KNN operations. SGAS [23] employs a similar network search strategy but is less time-efficient for similar performances. Our method also outperforms PointNet [33] (35.6%) and PointNet++ [34] (42.5%) by a consistent margin.
Table 3. Part Segmentation on PartNet (part mIOU on level 3). Best results in bold. LC-NAS models provide state-of-the-art performances on 12 object classes with faster inference time. Runtimes are averaged on 1000 runs with 10000 input points.

| Method      | (ms)  | Avg. | Bed | Bott | Chair | Clock | Dish | Disp | Door | Ear | Fauc | Knife | Lamp | Micro | Frid | Stora | Table | Trash | Vase |
|-------------|-------|------|-----|------|-------|-------|------|------|------|-----|------|-------|------|-------|------|-------|-------|-------|------|
| PointCNN [25] | 1402  | 46.49 | 41.9 | 41.8 | 43.9  | 36.3  | 58.7 | 82.5 | 37.8 | 48.9 | 60.5  | 34.1  | 20.1  | 58.2 | 42.9  | 49.4  | 21.3  | 53.1  | 58.9  |
| SGAS [23]    | 185   | 48.28 | 43.4 | 50.8 | 41.2  | 38.8  | 61.4 | 82.5 | 37.1 | 48.8 | 56.1  | 49.4  | 21.2  | 56.5 | 44.5  | 49.4  | 29.3  | 54.4  | 56.0  |
| deep LPN [19] | 191   | 38.60 | 29.5 | 29.5 | 42.1  | 34.7  | 33.2 | 81.6 | 34.8 | 49.6 | 53.0  | 44.8  | 28.4  | 33.5 | 122.8 | 41.1  | 36.3  | 43.1  | 57.8  |
| LC-NAS-10    | 143   | 48.10 | 41.4 | 50.5 | 40.7  | 37.8  | 61.1 | 82.5 | 37.4 | 48.4 | 53.6  | 48.5  | 22.3  | 57.8 | 46.6  | 47.9  | 31.1  | 54.8  | 56.0  |
| LC-NAS-14    | 152   | 48.55 | 41.9 | 51.7 | 39.7  | 39.6  | 61.5 | 82.5 | 39.3 | 49.0 | 55.7  | 55.3  | 22.2  | 55.1 | 45.2  | 48.6  | 30.3  | 54.6  | 54.9  |
| LC-NAS-18    | 185   | 46.60 | 40.7 | 50.5 | 39.9  | 39.5  | 59.8 | 82.5 | 35.0 | 44.5 | 53.2  | 44.9  | 22.0  | 54.1 | 41.5  | 45.8  | 31.5  | 53.0  | 54.4  |

Timing. Our LC-NAS architecture targets a specific latency with 1024 points for inputs, but PartNet provides object point clouds with 10000 points each. Our implementation of KNN for PointCNN [25], SGAS [23] and LC-NAS is not optimized hence suffers the large input size scale up. As an example, the latency of PointCNN jumps from 26ms for 1024 points to 1402ms for 10000 points on a NVIDIA GTX2080 with 8GB. Similarly, our models searched for a latency of 10, 14 and 18ms jumps to 143, 152 and 185ms for those larger point clouds. All times reported are averaged over 1000 runs after 50 runs of warm-up (for Pytorch to optimize the CUDNN operations), using one batch of 10000 points.

4.4 Ablation Study on ModelNet40

Ablation on Latency Constraint Loss. In Table 4, we conduct an ablation study on our latency error by experimenting with different regularization factors $\lambda = 0.8$ and $\lambda = 1$ with the same search setting as $\lambda = 0.5$ shown in Table 1. Note that the results shown in Table 7 are trained with the hinge latency loss defined in Equation 4 with $\lambda = 0.5$. The average latency, overall accuracy and class accuracy are 10.95ms, 91.98% and 88.48% respectively when $\lambda = 0.5$. Compared with $\lambda = 0.8$ and $\lambda = 1$, the differences of accuracy and latency are within 0.1% and 0.4ms. Therefore, it is clear that the proposed hinge latency loss function is fairly robust to different strengths of regularization. Furthermore, we perform an experiment by replacing the hinge latency loss with a mean square error (MSE) loss with regularization factor as $\lambda = 0.5$. Architectures searched with MSE loss as the constraint only perform 0.04% better than the hinge latency loss counterpart but have on average 1.08ms more latency. This shows that searching the hinge latency loss obtains more efficient architectures than searching MSE loss.

Ablation on Hyper-parameters of Models. In Table 5, we conduct an ablation study of searched cells with different numbers of cells and different input channels size. It shows that the obtained cells are scalable with different hyper-parameters. Architectures with more cells and a larger channel size usually perform better. For example, architectures with 2 cells and 128 channels outperform those with 1 cells and 128 channels by 0.26% in term of overall accuracy. Small architectures can still achieve state-of-the-art results. LC-NAS-18 with 1 cell and 64 channels reaches 92.30% O.A. with only 7.39ms inference time.
Table 4. Ablation on Latency Constraint Loss on ModelNet40. We show the effect of different $\lambda$ parameters in our constrained hinge loss. We compare these results with Table 7, where $\lambda = 0.5$ and the average latency, overall accuracy, and class accuracy are 10.95 ms, 91.98% and 88.48% respectively. When tweaking $\lambda$ to 0.8 and 1.0, the results change slightly. This shows our hinge loss is robust to different regularization strengths. We also change the hinge loss to MSE and observe a significant increment in average latency. Our hinge loss is better at predicting tighter latency networks.

| Method    | $\lambda = 0.8$ | $\lambda = 1$ | MSE loss |
|-----------|-----------------|----------------|----------|
|           | Latency | O.A. | C.A. | Latency | O.A. | C.A. | Latency | O.A. | C.A. | Latency | O.A. | C.A. |
| LC-NAS-18 | 16.61 ms | 92.83 | 90.31 | 18.35 ms | 92.87 | 90.02 | 17.34 ms | 92.54 | 90.38 |
| LC-NAS-16 | 12.69 ms | 92.38 | 89.24 | 14.41 ms | 92.54 | 89.50 | 14.44 ms | 92.59 | 89.83 |
| LC-NAS-14 | 13.20 ms | 92.71 | 89.88 | 12.33 ms | 92.63 | 90.13 | 13.41 ms | 91.53 | 86.80 |
| LC-NAS-12 | 11.05 ms | 92.54 | 90.94 | 10.69 ms | 92.91 | 89.45 | 14.22 ms | 92.34 | 89.09 |
| LC-NAS-10 | 11.34 ms | 92.30 | 89.95 | 8.29 ms  | 90.88 | 85.15 | 10.58 ms | 92.71 | 89.61 |
| LC-NAS-8  | 7.67 ms  | 90.03 | 84.30 | 6.42 ms  | 90.36 | 84.84 | 7.87 ms  | 92.13 | 88.13 |
| LC-NAS-6  | 6.61 ms  | 90.96 | 85.71 | 5.86 ms  | 90.96 | 85.71 | 6.36 ms  | 90.32 | 85.08 |
| Avg.      | 11.31 ms | 91.96 | 88.62 | 10.91 ms | 91.88 | 87.83 | 12.03 ms | 92.02 | 88.42 |

Table 5. Ablation on Hyper-parameters of Models. We change the number of channels in the operations and the total number of cells used in the networks and evaluation the architectures on ModelNet40.

| Method    | 1 cell, 64 channels | 1 cell, 128 channels | 2 cells, 128 channels |
|-----------|---------------------|----------------------|----------------------|
|           | Latency | O.A. | C.A. | Latency | O.A. | C.A. | Latency | O.A. | C.A. | Latency | O.A. | C.A. |
| LC-NAS-18 | 7.39 ms | 92.30 | 88.13 | 6.36 ms | 92.22 | 89.09 | 11.32 ms | 92.26 | 88.66 |
| LC-NAS-16 | 4.85 ms | 91.77 | 87.85 | 5.14 ms | 92.15 | 89.18 | 10.90 ms | 92.59 | 89.63 |
| LC-NAS-14 | 4.85 ms | 92.02 | 88.04 | 5.58 ms | 92.30 | 89.55 | 8.41 ms  | 92.10 | 89.84 |
| LC-NAS-12 | 3.89 ms | 91.53 | 86.93 | 3.84 ms | 91.49 | 87.26 | 6.83 ms  | 92.10 | 88.82 |
| LC-NAS-10 | 4.21 ms | 92.18 | 88.10 | 4.35 ms | 91.73 | 88.24 | 7.40 ms  | 92.14 | 88.90 |
| LC-NAS-8  | 3.02 ms | 90.11 | 84.63 | 3.12 ms | 90.07 | 84.66 | 6.06 ms  | 90.52 | 85.41 |
| LC-NAS-6  | 2.31 ms | 89.79 | 83.73 | 2.41 ms | 90.23 | 84.90 | 3.92 ms  | 90.32 | 84.99 |
| Avg.      | 4.36 ms | 91.39 | 86.77 | 4.40 ms | 91.46 | 87.55 | 7.83 ms  | 91.72 | 88.04 |

5 Conclusion

We presented an automatic neural architecture search that consider the latency factor in the search. We designed a loss function that constrains the latency to a specific timing for a given hardware. We show with empirical results that our architectures LC-NAS reach the latency it has been designed for on ModelNet10 and generalize on ModelNet40. Moreover, we showed transfer capabilities of LC-NAS for part segmentation, displaying state-of-the-art results on the PartNet benchmark. We envision LC-NAS to be used in time-constrained applications such as autonomous driving, robotics and embedded systems, where latency is of paramount importance for the fulfillment of the vision task. We believe our work will pave the ground for further constrained neural architecture search.
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A Visualization

To optimize the model architecture $\mathcal{A}$ with the latency constraint in an end-to-end fashion, we need the gradient with respect to the binary architecture encoding $\tilde{E} = \mathcal{E}(\mathcal{A})$. However, we compute $\tilde{E}$ from a non-differentiable function $\mathcal{E}(\cdot)$ that involves some rules/heuristics that cannot directly retrieve the gradients. Hence, we approximate the gradient by trusting the selection rules/heuristics as a linear operation from Eq.(3).

We visualize the updating procedure of one training iteration in Fig. 4. The first plot shows the input architecture parameters before this iteration. Besides, the middle plot shows its gradient from the back-propagation on the latency loss. In the last plot, we compare the updated architecture parameters. As explained in paper Section 3.2, the element $(m, n)$ in the plots indicates that the operation $n$ is chosen for the edge $m$. Notably, the second row, EdgeConv column in the Gradient plot is positive, indicating that decreasing the weight of the EdgeConv operation on the second edge will decrease the latency. In the right plot, accordingly, we decrease the weight of the EdgeConv operator on the this edge.

![Fig. 4. Visualization of the updating procedure in one training iteration.](image)
The left and right plots show the architecture parameters before and after one gradient step respectively. The middle plot shows the gradient from the back-propagation on the latency loss.

Fig. 5 visualizes the intermediate variables. Given the architecture parameter $\mathcal{A}$, we use some rules/heuristics to compute its encoding $\tilde{E}$, shown in the first plot. Meantime, we apply softmax on each row of $\mathcal{A}$ to get the second plot. Then, to approximate the gradient, we trust the selection rules/heuristics as linear operation by approximating with multiplying an element-wise mask $\zeta$, shown in the third plot. That is to say, the element-wise multiplication of Soft Alpha and Mask equals to the Architecture Encoding. Finally, the architecture parameters are updated and result in an new encoding in the last plot, where the EdgeConv operation is replaced by a more efficient Skip-Connect operation. We also compare the changes of cells in Fig. 6.
Fig. 5. Visualization of the intermediate variables in training. The four plots respectively show the input architecture encoding, softmax result, mask, and the updated architecture encoding. Eventually, the \textit{EdgeConv} operation on the second edge is replaced by a more efficient \textit{Skip-Connect} operation.

Fig. 6. Visualization of discovered architectures before (top) and after (bottom) one iteration. Please be note that the edge from $c_{k-1}$ to node 0 changes from \textit{EdgeConv} to more efficient \textit{Skip-Connect}.

A.1 More Gradient Visualization

To give a comprehensive study on the quality of the gradient approximation, we randomly choose one model architecture in the test set (shown in Fig. 7), and visualize a approximation with different setups. The measured latency and predicted latency of this architecture are respectively 13.92ms and 14.33ms.

Fig. 7. Visualization of a random selected architecture in the test set. Its measured latency and predicted latency are 13.92ms and 14.33ms respectively.

Gradient Visualization with Hinge Latency loss. We visualize the gradient in Fig. 8 where we use a hinge loss in the latency constraint. When we set the latency targets as 6ms, 10ms, or 14ms, the gradients stay the same. Moreover, the negative gradient direction tends to assign higher value for efficient operations.
such as *Skip-Connect* and *Conv-1×1*, while decrease the value for complex GCN operations like *MRConv* and *EdgeConv*. Besides, when the target latency is 18ms, which is greater to the current model latency 14.33ms, the gradients of the hinge latency loss become zeros.

**Fig. 8. Visualization of the gradient from latency constraint (1).** We apply hinge-loss-like regularization loss to regress the *LatReg* model prediction to four target latencies.

**Gradient Visualization with MSE Latency loss.** We also visualize the gradient in Fig. 9 where we use a mean-square-error (MSE) loss in the latency constraint. When we set the latency targets as 6ms, 10ms, and 14ms, the gradients have the same pattern, but the scales are positively correlated the latency gap between targets and the prediction (14.33ms). Notably, when the target latency is greater to the current model latency, shown in the bottom-right plot, the negative gradient will assign less probability for *Skip-Connect* and *Conv-1×1* (the cheap operations), while increase the probability for time-consuming operations such as *MRConv* and *EdgeConv*. 
We apply \( \text{MSE loss} \) to regress the \textit{LatReg} model prediction to four target latencies.

### B Details in Latency Regressor Model

To train our Latency Regressor (LatReg) model, we sample 100\( \text{K} \) random cell-architectures from our search space and measure their latencies. We show the latency distribution in Fig. 10 \textit{Left}.

We randomly split our architectures into train, validation, and test sets. We use the training set to train our LatReg model, use the validation set to choose the hyper-parameters such as learning rate and training epochs. Then, we evaluate the model on the test set, and the LatReg model reaches an average absolute error of 0.16ms. Fig. 10 \textit{Right} visualized the measured latency and predicted latency of each architecture in the test set. We can find the two variables are linearly dependent to each other and the slope is close to 1.
Fig. 10. LatReg Model data distribution and performance. Left: We show here the distribution of all latencies. Latency values range from 5.9 ms to 23.5 ms, with an average around 15 ms. We randomly split out architectures into train, validation, and test subsets, thus keeping similar distributions on all splits. Right: We can find the measured latency and predicted latency are linearly dependent to each other and the slope is close to 1.

C Ablation Study on Non-targeted Latency Loss

Previous latency-aware differentiable NAS methods \cite{lee2019, taylor2018} usually add the latency loss as a regularizer to the bi-level optimization procedure as follows:

$$\min_{\mathcal{A}} \mathcal{L}_{val}(W^*(\mathcal{A}), \mathcal{A}) + \lambda LatReg(\mathcal{E}(\mathcal{A}))$$

(4)

s.t. \hspace{1cm} \mathcal{L}_{train}(W, \mathcal{A})$$

(5)

where $\mathcal{L}_{val}$ is the cross-entropy loss on validation set, $\mathcal{L}_{train}$ is the cross-entropy loss on training set, $\mathcal{A}$ is the architectural parameters, $W$ is the network weights, $\lambda$ is the regularization factor, $LatReg(\cdot)$ is the learned latency regressor and $\mathcal{E}(\cdot)$ is a non-differentiable binarized function that take as input continuous architectural parameters $\mathcal{A}$ and output a binarized architecture encoding $\tilde{\mathcal{E}}$. This non-targeted latency loss can be regarded as a special case of the proposed hinge latency loss with a target as 0. As we discussed, this form of constrained loss has two main disadvantages (1) It fails to minimize the architecture to be lower than a certain latency. Thus, it is less controllable while using for hardware deployment. (2) The regularization factor $\lambda$ is sensitive and difficult to tune to trade-off the capacity and efficiency of searched models. In Table 6, we experiment non-targeted latency loss with $\lambda$ from 0.5 to 0.0001. We first set $\lambda = 0.5$. The obtained architecture only consists of Skip-Connect, Conv-1×1 (see Fig. 11 (a)) and merely reach 90.24% overall accuracy on ModelNet40. We further decrease the regularization factor $\lambda$ to 0.1 and 0.05. The discovered cells still only consist of Skip-Connect, Conv-1×1. Therefore, the regularization are still considered too strong. Only when $\lambda$ is not greater than 0.001, the searched cells have reasonable performance around 92.5%. However, the value of $\lambda$ does not explicitly guarantee a certain latency constraint which make it hard to tune. The searched cells are visualized in Fig. 11.
Table 6. Ablation on Non-Targeted Latency Loss. We change the regularization factor $\lambda$ from 0.5 to 0.0001. We see that the performance of the discovered networks on ModelNet40 are sensitive to $\lambda$ and the latency of networks is hard to control.

| $\lambda$ | Latency | O.A. | C.A.   |
|-----------|---------|------|--------|
| 0.5       | 6.60 ms | 90.24| 84.70  |
| 0.1       | 6.19 ms | 90.76| 85.37  |
| 0.05      | 6.35 ms | 90.28| 84.90  |
| 0.01      | 9.64 ms | 92.26| 89.00  |
| 0.005     | 8.82 ms | 86.83| 80.65  |
| 0.001     | 14.63 ms| 92.63| 89.98  |
| 0.0005    | 12.08 ms| 92.50| 89.75  |
| 0.0001    | 18.71 ms| 92.50| 89.68  |

Fig. 11. Visualization of searched cells with non-targeted latency loss with different $\lambda$. 