Scaling limits and reliability of SOI CMOS technology
(invited)

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Abstract. As bulk and PD-SOI CMOS approach their scaling limit (at gate length of around 50 nm), there is a renewed interest on FD-SOI because of its potential for continued scalability beyond this limit. In this review the performance and reliability of extremely scaled FD transistors are discussed and an attempt is made to identify critical areas for further research.

1. Introduction

Central to Silicon on Insulator (SOI) CMOS devices and technology is the inherent presence of two opposite channels in each MOSFET (one on each side of the silicon film) and the floating body (Fig.1). These features lead to a host of interesting and unique device properties and phenomena, which have been investigated extensively [1] [2].

Two important advantages of SOI structures, compared to bulk silicon technology, are the improved isolation and reduced parasitic capacitances and many more become apparent as devices are scaled into the deep submicron region and beyond: higher drive current, reduction of short channel effects, etc. In fully depleted (FD) SOI MOSFET’s the silicon film (typically less than 100 nm) is fully depleted during the operation of the device causing the two channels to be electrostatically coupled, such that the device static characteristics (including threshold voltage, subthreshold swing, transconductance and short channel effects) all become dependent on the bias of both gates. In partially depleted (PD) devices the silicon film is thicker than the depletion layer width and the part of it below the depletion
layer remains undepleted during the device operation. This initially neutral, floating film segment can be charged up by impact ionization currents at drain voltages well below the breakdown, which leads to a number of static floating body effects (e.g. current kinks) in PD devices. The floating body (film) also causes premature breakdown of the parasitic source-body-drain BJT in both types (PD and FD) of devices. To complicate matters more, all of the above effects are compounded during dynamic operation of the devices.

In addition to their effects on device operation and performance, the channel coupling and floating body present challenging problems and new possibilities in the measurement of the deep traps, generation lifetime, and interface state density profiles [3]. More recently, as SOI technologies are reaching new levels of maturity, there has been an increased interest to assess and control various reliability issues of SOI MOSFET’s such as hot carriers [3-4], electrostatic discharge protection [5], etc. [6]. Again, the existence of two gates, the nature of the buried oxide, and the possibility of PD and FD device operation make the situation considerably more complicated than for bulk devices. Of significant interest is the fact that stressing one channel can cause damage to the opposite channel.

2. Fully Depleted SOI MOSFET

Because of the inherent electrostatic coupling of the front and back channel, the FD SOI MOSFET was thought to be superior to both PD SOI and bulk MOSFET’s [7]. For example, among other things the drive current is higher in a fully depleted transistors with depleted back interface as can be seen from these expressions [1]: $I_{\text{DSAT}} = \frac{\mu C_{\text{ox}} W}{2L(1+\alpha)} (V_{\text{GS}} - V_{\text{TH}})^2$ where $\alpha = \frac{C_{\text{Si}} C_{\text{BOX}}}{C_{\text{ox}} (C_{\text{Si}} + C_{\text{ BOX}})}$. Here $C_{\text{BOX}}$ is the (often negligible) capacitance of the buried oxide, and $C_{\text{Si}}$ the capacitance of the depleted silicon film, which is larger than the corresponding depletion layer in bulk and PD-SOI MOSFET’s and the reason why the drive current is larger in FD SOI MOSFET’s (often by as much as 30%). However, a closer look at the device physics [8] revealed that this superiority was diminished in the deep submicron range, due to carrier velocity saturation. This and the easier control of the SOI film thickness, explain why PD-SOI has prevailed in industry. However, as bulk and PD-SOI approach their scaling limit (imposed by channel doping limitations), at gate length of around 50 nm, there is currently a renewed interest on FD-SOI [9][10], because of its potential for continued scalability beyond this limit. This continued scalability of FD-SOI is achievable by using new (“exotic”) gate materials to control the threshold voltage and lowly-doped/undoped channels and thinning the silicon film and buried oxide to control the short channel effects.

As the film thickness $t_{\text{Si}}$ is reduced, the effective junction depth (equal to the film thickness) is reduced, which strengthens the front gate’s control of the back-surface potential, improving the short channel effects [11]. An insightful analysis [12] of the 2D channel potential in the subthreshold region obtained a 1D distribution of the surface potential, according to which the impact of the drain voltage on the potential barrier between source and drain is decreased exponentially by the factor $\exp(-L/2\lambda)$. Here $L$ is the channel length, and $\lambda$ the “natural” length scale: $\lambda = \frac{e_{\text{Si}}-e_{\text{ox}}}{\sqrt{e_{\text{ox}}}}$. As an example, using a film thickness of 10 nm and a gate oxide thickness of 1.5 nm, this gives $\lambda=6.7$ nm. Assuming $(L/2\lambda) > 2$, the channel length limit for acceptable subthreshold current control is 27 nm.

Early in the development of SOI technology, the buried oxide film thickness was around 400 nm, which ensured good insulation from the substrate and negligible buried oxide capacitances ($C_{\text{BOX}}$). However as FD technology developed and channel lengths approached the deep submicron range, it was observed that a substantial portion of the source and drain depletion charges terminated in the channel rather than the substrate underneath the buried oxide [11]. This was undesirable, as it deteriorated the short channel effects, and needed to be controlled. A parametric 2D analysis of the potential and field patterns in the structure revealed that as well as reducing the silicon film thickness, reducing the buried oxide thickness moderates this 2D charge sharing through the buried oxide. A recent analysis of this “fringing” field and the mechanisms of controlling it calculated the back surface...
potential shift induced by the applied drain voltage in terms of Si film, gate oxide and BOX thickness \[9\]:

\[
\Delta V_{sb} = \left( \frac{t_{box} (t_{si} + 3t_{ds})}{3L_{eff}^2} \right) V_{ds} (V_{ds})
\]

Here \(V_{ff}(V_{ds})\) is a drain voltage dependent function, and \(L_{eff}\) the effective channel length. Since for FD transistors the front and back channel potentials are electrostatically coupled, it is implied by this expression that for thin silicon film channels the fringing field and related short channel effects can indeed be controlled by reducing the BOX thickness. Scaling \(t_{box}\) will however undermine the FD SOI advantages derived from this electrostatic coupling of the two channels. Instead, it is seen that scaling \(t_{si}\) may also be used to suppress the field fringing and short channel effects, but at the cost of diminishing the ability to use the depletion charge channel doping for threshold voltage control. It would appear then that the best overall solution is to use moderately thick buried oxide and undoped, ultrathin SOI film, and attempt to control the threshold voltage by choosing gate materials of appropriate workfunction value \(\Phi_G\).

Several groups have recently published detailed studies \[9,10\] of high performance (HP) and low operating power (LOP) FD SOI MOSFETs in accordance with the specifications of the International Technology Roadmap for Semiconductors (ITRS):

| Gate length HP (nm) | 37 | 25 | 18 |
|---------------------|----|----|----|
| Operating voltage HP (V) | 1.0 | 0.7 | 0.6 |
| Gate oxide thickness HP (nm) | 1.3 | 0.8 | 0.8 |
| Gate length LOP (nm) | 53 | 32 | 22 |
| Operating voltage LOP (V) | 1.1 | 0.9 | 0.8 |
| Gate oxide thick. LOP (nm) | 1.8 | 1.2 | 1.1 |

These are mostly simulation (and some experimental) studies for channel lengths down to \(L=18\) nm and silicon film to \(t_{si}=5\) nm. Gate workfunction, gate insulator thickness and dielectric constant, silicon film doping and thickness, buried oxide thickness, gate length, spacer width, S/D doping profiles and back gate bias were all considered and their effect on threshold voltage control and \(I_{ON}\) and \(I_{OFF}\) currents were examined. Although there are some differences between the findings of the various groups, it appears that with gate workfunction values within a small window around 4.5 eV and undoped silicon film, ITRS performance targets can be achieved down to technology node of 65 nm (gate length 25 nm for HP, and 32 nm for LOP). For example, Luyken at al \[10\] investigated FD MOSFET’s with widely varying parameters, by employing a drift-diffusion based simulator, which allowed the performance of a large number of parametric studies with moderate computational effort, with reasonable accuracy. They found it to be a valid approach, because the values for the ON and OFF currents predicted by these simulations where within less than 10% to “sample” values obtained by state of the art Monte Carlo simulations including quantum effects. Some of their most typical results for the high performance for gate length 37 nm and film thickness 5nm are shown in Fig. 2.

The main conclusion from these results \[9,10\] is that only a very narrow (almost negligible) design space is available for all parameter combinations in the case 10 nm thick for SOI, but the situation improves considerably if the SOI is thinned down to 5 nm. Similar results were obtained for low operating power devices, and it was thus shown that ITRS targets can be met down to 25 nm gate length for HP devices and 32 nm for LOP devices. To take scaling beyond this limit, either (unrealistically) much thinner SOI films should be used, or new, “non-classical” device structures \[13,14\] (i.e., double gate SOI MOSFET’s”) developed.

### 3. Hot Carrier Reliability

Hot carrier reliability was thought not to be a problem for low power supply voltages, but surprisingly it has been shown to be of concern for voltages well below 1.2 V. This is explained by the relatively recent discoveries that carriers can get hot by a two-step process through electron-electron scattering \[15\] and by thermally assisted impact ionization \[16\] at voltages well below 1.2 V. This possibility
and the complicated nature of hot carrier induced degradation of SOI MOSFET’s suggests that a careful look needs to be taken on the hot carrier reliability of deeply scaled SOI MOSFET’s. For example, stressing one channel may lead to hot carrier injection in the opposite channel [3]. Depending on the case in hand, worst-case stress (WCS) for a given VD may occur with VG set @ VT, VD/2, VD, maxISUB, or maxIG. The situation is very complicated, as WCS is decided through intricate interdependences of stress bias level, floating or grounded body operation, channel-coupling strength and device operation temperature. Temperature is particularly important here because SOI devices are more likely than bulk devices to operate at elevated temperatures because of self-heating.

**Figure 2.** Typical design space for high performance FD transistors with silicon film thickness 5 nm for the parameter values listed and a number of gate work-function values Wf as shown

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Fig. 3 shows some recent data from a 70 nm SOI technology [17], where it is seen that hot carrier degradation of the I-V characteristics does indeed take place (Fig. 3, left) and that the effect of the actual stress conditions and of the temperature can be quite profound (Fig. 3, right). Of particular importance here is the observation that under VG=VD stress the degradation is significantly higher at 100 °C as compared to room temperature (RT).

4. ESD Protection
SOI faces unique challenges with regard to ESD protection due to the geometrical nature of the structure itself: the silicon film is separated from the substrate by the buried oxide layer, which has much lower thermal conductivity than silicon. The active layers are thus both electrically and thermally separated from the substrate, rendering conventional ESD protection circuits such as thick field oxide devices and vertical, large area p-n diodes, unsuitable because of the absence of vertical current and heat flow paths. Here there is a need to form sufficient ESD current and heat flow paths above the active layers, or some other clever solutions must be found that can make use of the substrate for building the ESD protection circuitry underneath the buried oxide. Currently the most popular ESD structure in SOI is the poly-bounded SOI lateral diode (Fig. 4(a)) with poly tied to cathode, anode or floating [5]. Although adequate protection levels have been achieved for state of the SOI technologies, they are about half [18] of what is obtained in comparable bulk CMOS technologies (Fig. 4(b)). The situation with regard to ESD protection will get worse with each subsequent SOI CMOS generation, because of the continuously shrinking SOI silicon film thickness. Structures using vertical current paths will in our opinion became inevitable, where for example holes through the buried oxide will have to be opened in selected locations through which the ESD current will be pushed to the ground.

5. Conclusions
Numerical simulations show that FD SOI technology can meet ITRS targets down to 25 nm channel lengths, by using “exotic” gate materials on ultrathin (~ 5 nm) and undoped SOI wafers. The hot-carrier reliability of these technologies is currently not known: carriers can get hot at very low voltages, and channel coupling and floating body complicate the effects of the induced degradation. ESD I/O protection is also very challenging and uncertain at the moment, and it requires further
research. Finally, scaling beyond the level possible with “classical” FD SOI CMOS, as discussed in the present review, can only continue through progress in the development of various multi-gate structures, currently under vigorous investigation in many research laboratories around the world.

6. Acknowledgements
My sincere thanks are due to all my students, past and present, for making hard work fun, and NSF for supporting our research over many years under several grants, most recently by grant # 0221126.

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