Investigation on Low Power Digital Tree Multipliers

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Abstract - VLSI is the relating to more than one branch of science of utilizing the advanced semiconductor technology to develop various functional units of computational System. The most complex function carried out by ALU is multiplication. Digital multiplication is most extensively used operation particularly in signal processing, System designer has to sacrifice silicon die area in order to make the multiplication as soon as possible. In this paper, various multiplier architectures are simulated and compared with high speed and low power 8x8 Vedic multiplier (Urdhva Triyagbhayam) which uses modified carry select adder for partial product reduction. The design is implementation and simulation has been done by Microwind tool with 90 nm technology. The simulation result shows 58% of power reduction, 65% of delay reduction and 44% of area reduction has been attained.

Keywords - Wallace, Dadda, Vedic multiplier, Partial Product Array Reduction, Power delay product (PDP).

1. Introduction

Digital multiplication is most extensively used operation especially in signal processing. Innumerable schemes have been proposed for realization of the operation of multiplier. They are

1. Serial multiplication  
2. Parallel multiplication

The serial multipliers are primitive with simple architecture (used when there is a lack of dedicated hardware multiplier). In parallel multiplier partial products are generated simultaneously. Parallel multiplications are used for high performance machines, where computation latency needs to be minimized. Multiplier architecture can be divided into three stages, a partial product generation stage, a partial product reduction stage and carry propagate addition stage. The complexity of an array multiplier is O(n) where as that of a tree multiplier is O(log2n), where n is number of bits in operand. Tree algorithm provides high speed multiplication but wiring overhead is major problem. Carry select adder is high speed final stage adder widely used in many data processing units. Carry-Select Adder method provides a good optimal results in cost wise and performance in carry propagation adder design. This work is focused on the optimization of PPA reduction and final stage addition using negative edge triggered D flip flop based Carry Select Adder.

2. Literature Survey

Different multipliers structures are discussed in the literature to achieve reduced PDP. Column compression architecture for fast multiplication proposed by [1] offers a total delay which is proportional to the logarithm of the operand word length of a multiplier. Wallace tree multipliers based on adiabatic 4:2 compressors proposed by [2] achieve considerable amount of energy savings but with increased latency.[3] have proposed high speed decomposed dadda multiplier logic improves speed and parallelism with increase in power delay product. Most of the multiplier design has problem with the structural irregularity [4]. The structural irregularity leads to increased power delay product. In vedic multiplier each step is carefully designed in optimal way to reduce overall PDP [5].

3. Wallace tree and DADDA Multiplier Using higher order Compressor

An 8x8 Wallace tree multiplier based on 7:2 higher order compressors is shown in the Figure 1. This 8x8 Wallace tree multiplier design will results reduce the power consumption but structure become quite complex.

Fig. 1: 8x8 Wallace tree multiplier using Higher Order Compressors (7:2)
The structure of 8x8 Dadda multiplier using 6:2 higher order compressors is as shown in the Figure 2. In this multiplier critical path delay is considered. First critical path elements are compressed to make the PPR structure regular [6]. Critical path column compression technique makes the performance multipliers are faster than other multipliers [7].

**Fig. 2:** 8x8 Wallace tree multiplier using Higher Order Compressors

### 4. Hybrid Multiplier

A Hybrid multiplier design is an optimized column adder tree, this multiplier combines the advantages of popular tree algorithms namely Wallace and Dadda. The generated PP’s are decomposed into four sections [8]. Each section is named as section A, B, C and D respectively and each section incorporates either 8x8 Wallace or Dadda algorithm for compressing partial products and the structure is shown in the Figure 3. The hybrid multiplier incorporates Wallace compression for two groups and other two groups are assigned with Dadda compression. Here final stage addition is carried out by carry propagate adder [9]. Various hybrid multiplier combinations have been constructed and simulated and the results are tabulated [10].

**Fig. 3:** Hybrid Multiplier

### 5. Proposed Vedic Multiplier

In this recent trend various new multiplier design techniques proposed by many researchers [11]. In this paper, we are addressing recent design techniques to find the optimal power structured digital Multipliers [12]. As shown in Figure 5, the proposed 4x4 Vedic Multiplier uses “Urdhva Tiryakbhyam Sutra” (algorithm). In this multiplier, Partial product reduction operation in the column is performed using optimized CSA with negative edge triggered D flip-flop. Speed and power of this proposed Vedic multiplier is improved when compared with existing multiplier techniques. The Aspect ratio of pull up transistor (p-type is modified for power trading. The proposed Vedic multiplier is designed using Micro wind tool and simulation of the multiplier design is done [13]. As shown in Figure 4, the power & delay for recent multiplier designs are compared with proposed Vedic multipliers and the results were tabulated.

**Fig. 4:** 4x4 Vedic Multiplier using are Efficient CSA

Let us assume $A0=4, A1=3, A2=2, A3=1$. Similarly, $B0=1, B1=1, B2=2, B3=2$. Vertically and crosswise multiplication have been carried out in the following steps 2, 3 ,4, 5, 6 and 7 respectively. At same time generated partial products are added, then the carry values will be forwarded to next higher stages. 

- **Stage 1:** $(A0 \times B0) = 4 \times 1 = 4$; Pre carry value = 0; Intermediate sum $4 + 0 = 4$
  - $S0=4; C0=0$

- **Stage 2:** $(A0 \times B1) + (A1 \times B0) = (4\times1) + (3\times1) = (4+3) = 7$; Pre carry value = 0; Intermediate sum $7 + 0 = 7$
  - $S1 = 7; C1 = 0$

- **Stage 3:** $(A0 \times B2) + (B1 \times A1) + (A2 \times B0) = (4\times2) + (1\times3) + (2\times1) = 8+3+2=13$; Pre carry value = 0; Intermediate sum $13 + 0= 13$
  - $S2 = 3; C2 = 1$

- **Stage 4:** $(A3 \times B0) + (A2 \times B1) + (A1 \times B2) + (A0 \times B3) = (1\times1) + (2\times1) + (3\times2) + (4\times2) = 1+2+6+8 = 16$; Pre carry value = 1; Intermediate sum $16 +1 = 17$
  - $S3 = 7; C3 = 1$

- **Stage 5:** $(A3 \times B1) + (A2 \times B2) + (A1 \times B2) + (A0 \times B3) = (4\times1) + (2\times2) + (3\times2) = 4+4+6$; Pre carry value = 1; Intermediate sum $14 +1 = 15$; $S4 = 5; C4 = 1$

- **Stage 6:** $(A2 \times B3) + (A3 \times B2) = 4 + 2 = 6$; Pre carry value = 1; Intermediate sum $6 +1 = 7$
  - $S5 = 7; C5 = 0$

- **Stage 7:** $(A3 \times B3) = 1 \times 2 = 2$; Pre carry value = 0; Intermediate sum $2 + 0 = 2$
  - $S6 = 2; C6 = 0$

Final Product is $C_C, S_5, S_4, S_3, S_2, S_1, S_0 = 2757374$
Fig. 5: 4x4 Line diagram of Vedic Multiplier

6. Result Analysis
The multiplier circuits were simulated using MICROWIND tool with 90nm technology [14]. Power dissipation results are taken based on SPICE simulation, where nodal analysis and loop analysis are performed to calculate voltages and currents respectively. Since SPICE is circuit level simulation, power results are attained are more accurate. Table 1, Table 2, Table 3, Table 4 and Table 5 lists the power and delay results for the Partitioned, decomposed Dadda multiplier, compressor-based Wallace & Dadda multiplier and hybrid multipliers respectively. It infers that an improvement of 58% and 65% in Speed improvement is achieved for proposed vedic multiplier structure [15]. An area reduction of nearly 44% is attained [16-17].

Table 1: 8x8 Compressor Based Dadda Multiplier (3:2 to7:2)

| Adder Technique used in Partial product Array Reduction Stage | 8x8 Compressor Based Dadda Multiplier (3:2 to7:2) |
|--------------------------------------------------------------|--------------------------------------------------|
|                                                              | Total Power Consumption (mw) | Delay (ns) | PDP in X10^{-12} (ws) |
| 14T                                                          | 1.699                          | 6.4        | 10.08               |
| 10T                                                          | 1.482                          | 6.1        | 9.040               |
| GDI                                                          | 0.596                          | 4.6        | 2.626               |
| 8T                                                           | 1.470                          | 4.3        | 6.726               |

Table 2: 8x8 Compressor Based Wallace Tree Multiplier (3:2 to7:2)

| Adders used in PPR Stage | 8x8 Compressor Based Wallace Tree Multiplier (3:2 to7:2) |
|--------------------------|----------------------------------------------------------|
|                          | Total Power Consumption (mw) | Delay (ns) | PDP in X10^{-12} (ws) |
| 14T                      | 2.094                          | 6.2        | 12.98               |
| 10T                      | 1.264                          | 5.7        | 7.204               |
| GDI                      | 1.475                          | 6.1        | 8.887               |
| 8T                       | 1.265                          | 3.4        | 4.297               |

Table 3: 8x8 Partitioned Dadda Multiplier Using Carry Select Adder

| Adder Technique used in Partial product Array Reduction Stage | 8x8 Partitioned Dadda Multiplier Using Carry Select Adder |
|--------------------------------------------------------------|----------------------------------------------------------|
|                                                              | Total Power Consumption (mw) | Total Power Consumption (mw) | Total Power Consumption (mw) |
| 14T                                                          | 3.882                          | 3.882                          | 3.882                          |
| 10T                                                          | 2.682                          | 2.682                          | 2.682                          |
| GDI                                                          | 2.668                          | 2.668                          | 2.668                          |
| 8T                                                           | 2.498                          | 2.498                          | 2.498                          |

Table 4: 8x8 Hybrid multiplier using Wallace and Dadda Method

| Adder Technique used in Partial product Array Reduction Stage | 8x8 Hybrid multiplier using Wallace and Dadda Method |
|--------------------------------------------------------------|----------------------------------------------------------|
|                                                              | Total Power Consumption (mw) | Total Power Consumption (mw) | Total Power Consumption (mw) |
| 14T                                                          | -                          | -                          | -                          |
| 10T                                                          | -                          | -                          | -                          |
| GDI                                                          | 0.325                          | 0.325                          | 0.325                          |
| 8T                                                           | 0.780                          | 0.780                          | 0.780                          |
Table 5: 8X8 Vedic Multiplier using CSA

| Adder Technique used in Partial product Array Reduction Stage | 8X8 Vedic Multiplier Using Carry Select Adder |
|---------------------------------------------------------------|------------------------------------------------|
|                                                               | Total Power Consumption (mw) | Total Power Consumption (mw) | Total Power Consumption (mw) |
| 14T                                                           | -                             | -                             | -                             |
| 10T                                                           | -                             | -                             | -                             |
| GDI                                                           | 0.298                         | 0.298                         | 0.298                         |
| 8T                                                            | 0.458                         | 0.458                         | 0.458                         |

7. Conclusion

Our proposed 8x8 Vedic multiplier using an area efficient carry select adder has been implemented. The results reveal that proposed 8X8 Vedic multiplier structure consume less power. The PDP for proposed structure is least. Hence the multiplier using an area efficient CSA, is best suited for high performance multiply and accumulate units.

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