Design and Analysis of a Micromachined LC Low Pass Filter For 2.4GHz Application

Samruddhi R Saroj¹, Vishal R Rathee², Rajesh S Pande³
¹, ², ³Department of Electronics Engineering, Shri Ramdeobaba College of Engineering and Management, Nagpur – 440013, India

E-mail:¹sarojsr1@rknec.edu, ²ratheevr@rknec.edu

Abstract. This paper reports design and analysis of a passive low pass filter with cut-off frequency of 2.4 GHz using MEMS (Micro Electro-Mechanical Systems) technology. The passive components such as suspended spiral inductors and metal-insulator-metal (MIM) capacitor are arranged in T network form to implement LC low pass filter design. This design employs a simple approach of suspension thereby reducing parasitic losses to eliminate the performance degrading effects caused by integrating an off-chip inductor in the filter circuit proposed to be developed on a low cost silicon substrate using RF-MEMS components. The filter occupies only 2.1 mm x 0.66 mm die area and is designed using micro-strip transmission line placed on a silicon substrate. The design is implemented in High Frequency Structural Simulator (HFSS) software and fabrication flow is proposed for its implementation. The simulated results show that the design has an insertion loss of -4.98 dB and return loss of -2.60 dB.

1. Introduction

Last decade saw a sudden surge in development and advancements in RF VLSI circuits particularly in the fields of wireless communication and radio transceivers due to increased demands in mobile handsets. The RF front-ends are the interface between the antenna and the digital modem of the wireless transceiver and are needed to be highly efficient in terms of detecting signals and transmitting high-power levels at higher frequencies. This essentially requires high performing analog circuits like filters, mixers, etc. The low quality factor (Q) of individual on-chip inductors and capacitors serve as bottleneck for the implementation of on-chip filter. Micromachined filters have gained attention in advanced integrated radio frequency (RF) systems as they offer low insertion loss, higher quality factor in less area, high level of integration, low cost and small sizes. The passive components with high Q and CMOS compatibility are desirable for low-loss lumped element filter [10-12].

The RF MEMS filter using the film bulk acoustic resonator (FBAR) technology and other types of resonator is reaching the physical scaling limit with the increase in the telecommunication frequency despite their ability to provide higher performances in smaller sizes [21]. Thus, various work is done on lumped component filter in the higher frequency range of millimetre and submillimetre wave frequencies [11, 12]. The use of embedded capacitor in between the spiral inductor results in the compact size of the filter that helps in improvement of insertion loss and selectivity [18]. The MEMS switches can be used for tuning the lumped components and make the reconfigurable filter with high tuning range [20]. To improve the performances of the passive components, the techniques to achieve high-resistive substrate are employed like using glass substrate, multilevel interconnection in silicon substrate, oxidized porous silicon on the silicon substrate [22], and using micromachining technique to etch away the silicon underneath the components [23]. A highly conductive metal like silver in the lumped components contribute to the reduced ohmic losses in the filter [11]. The use of oxide instead of nitride in the capacitor can lead to reduced costs [12].

The difference in the occurrence of ripples (variations) in passband and stopband differentiates one filter topology from another. In this work, the Chebyshev response is realized that has the advantage of more stopband attenuation and lesser number of components, at the trade-off of ripples in the passband. The different materials and the component types used in the filter design affects its performance. A
capacitor’s behaviour is almost ideal, compared with other types of components. However, the non-ideal behaviour of an inductor can play a major role in the performance of a filter circuit typically at higher frequencies and needs to be addressed efficiently. Aluminium is proposed in this work which has fair conductivity due to its familiarity and ease in the microfabrication processes with the silicon substrate. This work majorly concerns with the optimization of passive components used in a T configuration 3 Pole LC filter designed using MEMS technology.

2. Design of Filter

2.1. Design Procedure

The desired specifications that the Chebyshev filter to be designed and fabricated should have are passband ripple of 0.25 dB, minimum out-of-band attenuation of 25 dB at frequency 4.8 GHz (2Fc) and 17 dB at frequency 7.2 GHz (3Fc). Using the standard attenuation versus frequency curve for chebyshev filter with a passband ripple of 0.25 dB, it was found that a third order filter satisfies the targeted specifications. The normalized component values for a third order, low-pass, T-section filter is found using the equal load normalized component value tables [1]. Finally, the denormalized component values are found for a cut-off frequency of 2.4 GHz. This is done using the following relationships:

\[ L = \frac{Z \times L_N}{2\pi f_o} \]  
\[ C = \frac{C_N}{2\pi f_o \times Z} \]

This low-pass network configuration with the component values is shown in figure 1. The initial simulations of the network are performed in Agilent ADS with the lumped element models for inductor and capacitor at 2.4 GHz and standard terminations of 50 ohm. The component values are validated by observing the frequency response.

3. Design of lumped components

3.1. Suspended Spiral Inductor

3.1.1. Challenges and Design Considerations: Spiral Inductors are the most commonly used type of inductor in RF and microwave frequency applications today because of their potential in offering high inductance values in relatively smaller areas and shorter metal length as compared with the other inductor types.[2][13]. However, owing to the fact that the inductor consumes a considerable share of space on the entire chip, various researches are exploring ways to design inductors by optimizing topology to achieve good quality inductors in less area. The planar spiral inductors fabricated on Si substrates suffer from poor quality factor due to ohmic or metal losses and substrate losses [5]. The quality factor decreases with increase in finite resistance of the metal layer, more significantly at RF and
the losses in inductors increase due to induced currents and dielectric losses. Due to the low resistivity of silicon substrate, the capacitive coupling occurs between the spiral and the substrate resulting in the flow of conduction current through the substrate. Thus in planar inductors, the problem of parasitic capacitance between the inductor and the ground plane lowers the Quality Factor and Self-Resonance Frequency. Various techniques have been employed to improve them and one such method is micromachining, i.e., etching out the silicon substrate underneath the inductor using front side or backside etching techniques. Another method to achieve reduced substrate parasitic effects is to raise the inductor such that it is suspended in air with the help of metallic pillars above the substrate. The oxide beneath the inductor minimizes the substrate capacitance and should be as thick as possible. This leads to minimal losses and improved self-resonant frequency of the device. The lowering of self-resonant frequency occurs due to inter winding capacitance initially. This can be controlled by increasing the spacing between the windings or turns. Using thick and more conductive metal reduces the losses at low frequencies. The literature review reports that the metal thickness should be around 3 or 4 times the skin depth so as to reduce the conductive losses [3]. With increase in the metal width, skin and DC losses reduce but beyond a certain point eddy current loss dominates and Quality factor deteriorates rapidly with further increase in metal width [6]. In general, somewhat hollow inductors offer better performance as the innermost turns do not contribute much magnetic flux yet significantly contribute resistance and so losses.

3.1.2. Spiral Inductor Design: The initial structural dimensions of inductor were obtained using the ASITIC tool [4]. The spiral inductance is calculated [14] using the equation:

\[ L = 8.5 A^{1/2} n^{5/3} \text{ nH} \]  

where \( A \) is the surface area in cm\(^2\) and \( n \) is the number of turns.

A 5.4 nH spiral inductor was initially designed with more number of turns and later it was optimized to obtain the desired frequency response of low pass filter. This shift of inductor value in the filter circuit can be attributed to the combined effect of lumped components and micro strip transmission line metal resistivity. The change in the length of the micro strip line consequently demands change in the component values. Thus in the process, the moderate tolerance in the changes of component value is adopted.

| Parameters                        | Value  |
|-----------------------------------|--------|
| Number of inductor turns          | 4      |
| Width of inductor metal width     | 30μm   |
| Inductor outer diameter           | 700μm  |
| Spacing between turns             | 10μm   |
| Thickness of Al layer             | 3μm    |
| Height of Al pillars              | 3μm    |
Figure 2 shows the spiral inductor designed with the dimensions as shown in table 1. Aluminium metal is used in the inductor design for its fair conductive nature leading to reduced losses and due its familiarity with the Si based fabrication processes.

Simulating the inductor design, a quality factor of 8.6 was obtained at 2.4 GHz whereas the self-resonance was observed at 3.76 GHz as shown in figure 3.

3.2. MIM Capacitor
In RF applications and particularly in the design of mm-wave lumped filters [15], MIM capacitors are preferably used as they result in the lowest losses.

**Table 2. MIM capacitor structural details**

| Parameters                              | Value     |
|-----------------------------------------|-----------|
| Width of Capacitor and dielectric plates | 180μm     |
| Thickness of Al plates                  | 3μm       |
| Thickness of dielectric layer(Silicon Nitride) | 0.5μm    |

The Polysilicon-Insulator-Polysilicon (PIP) capacitors used traditionally exhibits difficulties in RF/AMS ICs due to the depletion effects of polysilicon electrodes while the MIM capacitors are depletion-free, have high conductance electrodes and reduced losses due to capacitive coupling with Si substrate. Silicon Nitride has been popularly used as dielectric in MIM capacitor. Silicon Nitride MIM capacitor provides relatively higher capacitance density than Silicon Dioxide MIM capacitors because...
of their higher dielectric permittivity (κ) of 7 as compared to Silicon Dioxide (~3.9) [17]. The capacitor density can be increased with reduced dielectric thickness, however, it may affect leakage current, breakdown voltage, voltage linearity and linearity issues [16]. This limits the extent of dielectric thickness scaling. The resistance of the capacitor bottom plate can be decreased by increasing the thickness and by using a higher conductivity material. The rectangular shape of the MIM capacitor is the most popular due its ease in drawing the layout, area calculations, and connections [7]. A 1.9 pF capacitor is designed using the dimensions as shown in table 2.

4. Low pass lumped element filter with cut off frequency of 2.4GHz

4.1. Design and Implementation
In the design the basic objective of miniaturization is sought for by incorporating the use of micro machined components. The three factors affecting the Q values of the passive components are substrate losses, metal losses and parasitic substrate capacitance [19] which has been taken care of in this design.

![Figure 4. Top view of Low Pass Filter](image)

A 0.5um silicon dioxide passivation layer is used to provide the electrical isolation and reduce the losses from the substrate. The thickness of Aluminium metal is kept in accordance with the skin depth considerations. The filter is designed with optimised lumped components and with an effort to minimize any impedance mismatch as discussed earlier. Figure 4 shows the designed low pass filter in HFSS.

4.2. Proposed Fabrication Steps
A silicon p-type wafer is to be cleaned through RCA cleaning and 0.5μm SiO₂ layer is to be deposited on the substrate using thermal oxidation. Further two fabrication flows are suggested as follows:

4.2.1. Lift off Technique: This fabrication process is divided into four phases as described below in the figures 5-8:

![Figure 5. Level 1](image)
1) The Level 1 is intended for 1.7µm Aluminum pillars, underpass, connection pads and capacitor bottom plate as shown in figure 5 (Note: The two spirals are identical in figure 5). The minimum thickness of metal is kept at 1.7µm selected as per the skin depth considerations. The photoresist (PPR) of thickness greater than 100 nm has to be deposited using spinner and the photoresist is developed using mask 1 in the optical lithography. The 1.7µm Aluminum is to be deposited then using the thermal evaporation process. Then the lift off process of the PPR is done to form the desired structure.

![Figure 6. Level 2](image)

2) In level 2, the Aluminum pillars and capacitor bottom plate has to be extended to 3µm. This will enable the underpass to be at lower height than the pillars in order to avoid the short connection between the underpass and the inductor turns. This, however, results in addition of one lithographic level. The steps include PPR deposition and development with mask 2, 0.3 µm Aluminum deposition using thermal evaporation and the lift off to extend the Aluminum pillars and the capacitor plate. Refer figure 6.

![Figure 7. Level 3](image)

3) The capacitor dielectric plate is to be formed in level 3. The steps include PPR deposition, 0.5µmSi₃N₄ deposition using Inductively Coupled Plasma Chemical Vapour Deposition (ICPCVD) and the lift off to form the capacitor dielectric plateas shown in the figure 7. A sacrificial layer of 3µmPPR is deposited to achieve the same level of rest of the structure as the pillars and the capacitor. This is done using the mask used in level 2.
4) In level 4, the formation of spiral inductor and the top capacitor plate is to be done as depicted in figure 8. The PPR is deposited and developed using mask 4 in the optical lithography. The Aluminium of 3µm is deposited using thermal evaporation followed by lift off to form the spiral inductor and the capacitor top plate.

4.2.2. Etching Technique: This fabrication process can be done in three phases as described below:

1) The level 1 is for making Aluminium pillars, underpass, connection pads and capacitor bottom plate as depicted in figure 5. The steps include evaporation of 1.7µm Al, Photoresist (PPR) deposition, lithograph for patterning PPR and the chemical etching of PPR and unwanted Aluminium subsequently.

2) The level 2 is for Capacitor dielectric plate formation (Figure 7). A 0.5µm Si₃N₄layer is to be deposited with ICPCVD. The third level lithography is done for patterning PPR followed by chemical etching of PPR and DRIE of unwanted Si₃N₄. With this, the capacitor lower plate remains at 1.7µm. This is one of the limiting case with this fabrication flow.

3) In level 3, initially 1.3µm PPR is deposited to extend pillars so that their height gets higher to that of the underpass (Figure 8). The PPR layer is developed followed by spiral and capacitor top plate deposition with the lift off technique. The PPR layer beneath the inductor provides structural robustness to the design. However the presence of PPR in between the metal layers may affect the behavior of the design. This is the second limiting case with this technique at the stake of reduced fabrication level and structural robustness.

5. Results and Discussion
Figure 9 shows the frequency response curve of the filter circuit. The insertion loss and return loss of the filter are -4.98 dB and -2.6 dB respectively. The losses offered by the filter are moderate and are minimized due to the measures taken to avoid the ohmic and parasitic losses in the lumped components. The roll off of the curve can be improved with the compact design of the filter. Some of the target applications of the 2.4 GHz low pass filter are Bluetooth & Wireless LAN (ISM and 802.11).
6. Conclusion
In this paper, the lumped components are optimally designed to achieve the required values in the three pole chebyshev filter. The length of the microstrip line is kept based on the simulation results at 2.4 GHz. The simulations were also performed with different materials to observe the amount of variations in the performance parameters. It was observed that the insertion loss reduces by 0.6 % with silver in the lumped components. In the process of optimising the inductor, it was observed that the insertion loss of the filter degrades by around 40 % with 50 % drop in the quality factor of the inductor used, giving the further direction of work in the lumped components filter. The MIM capacitor with better dielectric material is used instead of interdigitated or MOM capacitor, which provide higher Q in the same area, and to open the option of tunability in the design. Among the various other filters like filter using SAW, BAW resonators, conventional microstrip line, interdigitated or distributed filters in RF, the lumped components filter can be sought for its area efficiency, ease in including the tunability and its possible dimensional realization at higher frequencies, beyond 2.4 GHz[21]. This work can be extended to improve different performance parameters of lumped components and subsequently the filter using various novel techniques as discussed in section 1. The meander line inductor can be used to decrease one lithographic level in the fabrication. Also use of highly conductive metal like gold, silver or copper and a suspended capacitor can be employed in the filter design to improve its insertion loss. The proposed fabrication steps can be adopted and then filter can be characterized using vector network analyser.

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