Tunable thermal conductivity in defect engineered nanowires at low temperatures

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We measure the thermal conductivity (κ) of individual InAs nanowires (NWs), and find that it is 3 orders of magnitude smaller than the bulk value in the temperature range of 10 to 50 K. We argue that the low κ arises from the strong localization of phonons in the random superlattice of twin-defects oriented perpendicular to the axis of the NW. We observe significant electronic contribution arising from the surface accumulation layer which gives rise to tunability of κ with the application of electrostatic gate and magnetic field. Our devices and measurements of κ at different carrier concentrations and magnetic field without introducing structural defects, offer a means to study new aspects of nanoscale thermal transport.

Thermal transport measurements on semiconducting nanowires (NWs) have attracted a lot of attention in the last few years. Measurements of thermal transport in nanostructures are important as they provide a platform to test the existing descriptions of phonons in confined structures and across complex interfaces[1], and have the potential to result in technological applications as thermoelectric systems[1,2]. Different materials are benchmarked using the thermoelectric figure of merit \( ZT = \frac{S^2 T}{\rho \kappa} \), where \( S \) is the Seebeck coefficient, \( \rho \) is the electrical resistivity, \( \kappa \) is the thermal conductivity and \( T \) is the absolute temperature. \( ZT \) can be increased by appropriate engineering of nanostructures. One of the ways to increase \( ZT \) is by reducing \( \kappa \) without degrading its electrical conductivity and Seebeck coefficient[3]. As a result, an ideal thermoelectric material is a glass for phonons and ordered for electronic transport. Recently, several theoretical models as well as experimental studies have been carried out in different semiconductor NWs like Si, Ge, Bi2Te3 etc.[4,5]. It is found that for Si NWs, the value of \( \kappa \) is reduced by two orders of magnitude compared to bulk values by tuning the roughness of the surface. III-V semiconductors are also known to be good thermoelectric materials, and theoretical studies suggest that InSb and InAs NWs are good candidates for better \( ZT \)[6]. InAs NWs have been studied extensively to probe their charge and spin-transport[7,8]. An aspect of InAs NWs that makes studying their thermal transport, hitherto little explored[9,10], of interest is the ability to tune the density of twin defects and polytypes along its length by varying growth parameters[11,12,16]. Exploiting this control over crystal structure can help synthesize defect-engineered NWs, whose lattice has aperiodic array of twins along its length that modify phonon behavior, without significantly compromising their electrical properties[12,13]. Such NWs satisfy the key criteria for a good thermoelectric material – localization of phonons without localizing electrons.

In this work we explore the \( \kappa \) of suspended InAs NW field effect transistors (FETs); the NWs have high density of aperiodic twins and polytypes perpendicular to their axis[12,16,18]. The random nature of defects suppresses \( \kappa_{ph} \) (the phonon contribution to \( \kappa \)) resulting in reduction of thermal conductivity by 3 orders of magnitude from bulk. Our method also has an advantage which is to study \( \kappa \) as a function of carrier concentration without introducing additional impurities. We observe significant change in the thermal conductivity with the application of gate voltage suggesting finite electronic contribution, and we propose that this contribution comes from the conduc-
tion electrons at the surface accumulation layer which is inherent to low band gap semiconductors like InAs and InN.[23,24] To confirm the role of electronic contribution we apply magnetic field and see considerable changes in the thermal conductivity.

The InAs NWs used to fabricate the devices in this work were grown in a metal organic chemical vapour deposition (MOCVD) system using the vapor-liquid-solid (VLS) technique on a <111> B oriented GaAs substrate. NWs of 100 - 200 nm diameter were used in this experiment. 10-12 µm long NWs were chosen for making four probe suspended devices on a 300 nm thick, SiO2 coated degenerately doped Si wafer, which serves as the back gate (growth and device fabrication details are given in supplementary S1). Fig. 1(a) shows the schematic of the device and the circuit for electrical and thermal measurements. Fig. 1(b) shows a scanning electron microscope (SEM) image of a device. The gold electrodes provide mechanical support and Ohmic contacts with negligible contact resistance to the suspended NW besides thermally anchoring it at four points to the bath temperature T_b. The electrical properties of the device are characterized as a function of gate voltage (V_g) and temperature before detailed thermal transport measurements. Fig. 1(c) shows the resistance (R = V/ω) of a typical device as a function of V_g at a fixed value of T_b. The n-type field effect transistor (FET) behavior of the suspended NW devices is clearly seen. Fig. 1(d) shows the evolution of R as a function of temperature, T, and also the corresponding linear fit in the temperature range 10-50 K.

High resolution transmission electron microscopy (TEM) studies were used to characterize the microstructure of our twin-engineered NWs. Fig. 2(a) shows a large scale TEM image of a NW where we observe an aperiodic arrangement of the twin superlattice perpendicular to its axis. The fact that the lattice has defects but lacks a long-range periodicity is reflected in the Fourier amplitude (seen in Fig. 2(b)) that has no sharp peaks along the length of the NW. Figs. 2(c) & (d) show a detailed view of the twins and polytypes.[26,27] The typical spacing of these defects is ∼3-5 nm. Once electrical and structural characterization is done, we perform simultaneous thermal and electrical measurements.

One method of measuring thermal properties of nanostructures uses a modification of the 3ω technique[23] for κ and specific heat measurement. The modified 3ω technique[23,24] relies on fabricating suspended four probe devices with the conducting NW serving both as a heater and a thermometer. The magnitude of V(3ω) can be related to κ (in the limit ωγ → 0) as[23,24]

\[ V(3\omega) = \frac{4(I(\omega))^3RR'L}{\pi^4\kappa A}, \]  

where ω is the angular frequency of the AC current, I(ω) is its amplitude, R and R' are the resistance and the derivative of resistance with respect to temperature respectively, L is the length of the NW between the two middle probes and A, its cross section.[23,24] For our devices, L is 2 – 4µm and the thermal time constant γ can be estimated to be ∼10^-5s (details of phase information of 3ω signal in the limit of ωγ → 0 are given in the supplementary S1).

To measure κ at each temperature value, we vary the current (I(ω)) and obtain κ from the fitting of Equation 1 to the measured V(3ω) as a function of injected I(ω). Fig. 3(b) shows the evolution of V(3ω) with I(ω) along with the cubic power-law relationship that is essential to ensure that the 3ω technique is applicable within the applied current regime (to eliminate other source that can possibly show cubic scaling see supplementary S2). As we vary the temperature, we also record the resistance. We determine R' from the derivative to the linear fit to the R – T plot (see Fig. 1(d)). The variation of R with T becomes small and non-monotonic above 50-60 K this is the reason we choose the temperature range of 10-50 K in our experiment. The phase of the 3ω signal is measured to be zero at all temperatures (see supplementary Fig. S2). This procedure of fitting the power law given by Equation 1 at each instance of parameter space allows us to extract κ as a function of V_g and temperature. We have calibrated our technique using lithographically fabricated 170 nm wide 75 nm thick gold NWs in the temperature range of our measurement and obtained a Lorenz number around 2.4 x 10^-8 W Ω K^-2 (see supple-
expected to affect the electrical conductance of the semiconducting NW as a function of $V_g$.

However, the effect of electron density variation is not understood yet. We return to a model to understand the origin of large $\kappa_{el}$ we have to first understand the material property of the InAs wire. It is well known that in InAs there is an accumulation of charge at the surface. The resultant downward band bending pins the surface Fermi level above the conduction band minimum. In a geometry where the surface to volume ratio is large, such as NWs, this surface accumulation charge (SAC) plays a major role in the electrical transport. The SAC takes part in the electrical conduction and scatters due to roughness at surface, which is also the reason for low electron mobility in InAs NWs compared to bulk.

We have passivated our devices using (NH$_4$)$_2$S$_x$ but this passivation leads to further enhancement to the surface charge density ($\sim$10$^{12}$cm$^{-2}$) and consequently excellent Ohmic contacts. Fig. 1(c) shows that our device is always in conducting state throughout the gate range with low resistance value, strongly suggesting the presence of the accumulation layer. To estimate the $\kappa_{el}$ we have to consider the thickness of the layer of this SAC since it will reduce the effective cross sectional area through which heat is transported by electrons. The electrons in the bulk and in the accumulation layer can be thought of as two parallel channels conducting heat and we can define a effective layer thickness ($t$) to find out the actual $\kappa_{el}$ from the WF law,

$$\kappa_{el} = \frac{lT_bL_0}{\pi R\{r^2-(r-t)^2\}} \quad (0 < t \leq r) \quad (2)$$

where $l$ and $r$ are length and radius of the wire respectively, $R$ is the electrical resistance at temperature $T_b$ and $L_0 = 2.45 \times 10^{-8}$ WΩ K$^{-2}$ is Lorenz number. We can get a rough estimate of $t$ from above equation by assuming that at lowest temperature the phonon contribution ($\kappa_{ph}$) is small and $\kappa_{el} \sim \kappa$. For the NW of length 2.6 μm and radius 70 nm we get $t$ from our data as $\sim$20 nm and $\sim$10 nm for applied gate voltages of -10V and +10V respectively. Now we use Equation 2 to find $\kappa_{el}$ for all $T_b$, the result is plotted as solid lines in Fig. 3(d). This estimated $\kappa_{el}$ from a simplified picture captures the variation we see in our data with $V_g$. Another confirmation about this non negligible $\kappa_{el}$ comes from our magnetic field measurement. One way to suppress the electronic contribution is to apply a magnetic field, as it will reduce the electronic mean free path for heat transport by deflecting the semiclassical trajectory of electrons. We have done measurement in magnetic field up to 6T and see considerable reduction of thermal conductivity (see in Fig. 3(c)). Magnetic field can affect phonons via electron-phonon interaction, the amount of change in $\kappa_{ph}$ however, is much smaller than the effect we see in our measurement.

The total $\kappa$ is small and it is important to understand the origin of reduction in $\kappa_{ph}$. It is clear from the struc-
FIG. 4. (color online) The plot of measured $\kappa$ as a function of temperature of two different NW samples at 0 $V_g$, along with, the predicted values from two models to understand the reduction in $\kappa_{pol}$ for InAs NWs. Based on CWP model of Cahill et al. and HP model, of Hopkins et al. (denoted by HP model) which explicitly takes into account the role of interfaces for calculating minimum $\kappa$ in layered materials. We have calculated the predicted values of the model of Cahill et al. (denoted by CWP model) and the HP model for InAs (see supplementary S9). There is a range of $\kappa$ measured for devices made from different NW samples (see supplementary S2); data from two such devices at 0 $V_g$ is shown in Fig. 4. Without introducing any free parameters, the predictions of the CWP and HP models result in values that are comparable to the range in $\kappa$ measured in our experiments.

In summary, we demonstrate that thermal conductivity of InAs NWs with twin defects and polytypes is 1000 times smaller than bulk values which will make our devices suitable candidates for good thermoelectric materials. We show the electronic contribution becoming significant due to presence of the surface charge accumulation. The ability to tune thermal conductivity electrostatically can lead to novel ways of probing heat transport in defect engineered nanostructures, and possible device applications.

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