Implementing a LoRa Software-Defined Radio on a General-Purpose ULP Microcontroller

Mathieu Xhonneux, Jérôme Louveaux, and David Bol
ICTEAM, UCLouvain, Belgium

Abstract—Emerging Internet-of-Things sensing applications rely on ultra low-power (ULP) microcontroller units (MCUs) that wirelessly transmit data to the cloud. Typical MCUs nowadays consist of generic blocks, except for the protocol-specific radios implemented in hardware. Hardware radios however slow down the evolution of wireless protocols due to retrocompatibility concerns. In this work, we explore a software-defined radio architecture by demonstrating a LoRa transceiver running on custom ULP MCU codenamed SleepRider with an ARM Cortex-M4 CPU. In SleepRider MCU, we offload the generic baseband operations (e.g., low-pass filtering) to a reconfigurable digital front-end block and use the Cortex-M4 CPU to perform the protocol-specific computations. Our software implementation of the LoRa physical layer only uses the native SIMD instructions of the Cortex-M4 to achieve real-time transmission and reception of LoRa packets. SleepRider MCU has been fabricated in a 28nm FDSOI CMOS technology and is used in a testbed to experimentally validate the software implementation. Experimental results show that the proposed software-defined radio requires only a CPU frequency of 20 MHz to correctly receive a LoRa packet, with an ultra-low power consumption of 0.42 mW on average.

I. INTRODUCTION

The last years have seen the rise of Internet-of-Things (IoT) smart sensing applications, in which low-power sensors running on a microcontroller unit (MCU) periodically send small information packets to the cloud using a low-power wide-area network (LPWAN). Yet, the foreseen massive deployment of IoT applications and its associated ecological footprint may prevent the ICT sector to become truly sustainable, especially when considering that Moore’s law is slowing down [1]. Although IoT sensors have a very low energy consumption, they still own a non-negligible ecological footprint, mainly due to the embodied energy used during their fabrication [2].

Nowadays, IoT MCUs usually consist of generic blocks (processor, memories, ADC, ...), at the exception of the radios. The physical layer (PHY) of LPWAN radios are commonly implemented in hardware and are hence tied to one or several specific protocols. This historical paradigm however features several issues. First, IoT protocols cannot be updated without disposing of the already deployed sensor networks and deploying new devices. Similarly, the re-use of sensors for another application with different communication requirements (e.g., greater range or higher throughput) is impossible. Even more, we argue that the current paradigm hinders the improvement of LPWAN standards due to the need of maintaining retro-compatibility with existing sensors. The most popular LPWAN technologies deployed as of today are LoRa and SigFox [3].

Yet, both the LoRa and the SigFox specifications have barely evolved since their initial rollout in the early 2010s, despite the significant research conducted on LPWANs in the last decade.

IoT sensors with software-defined-radios (SDRs) have the potential to overcome these issues [4], [5]. In an SDR, most of the digital baseband computations are performed in software by a processor (CPU). Such an architecture enables on-the-fly updates of the communication protocol, and therefore allows a radio to switch from one standard to another when the requirements of the application evolve, or simply to follow the latest revisions of a protocol. The flexibility offered by SDRs could therefore help to both extend the lifetime of a sensor and foster innovation at the physical layer of LPWANs.

Nevertheless, the main challenge of IoT SDRs is to transmit and receive packets at the specified signaling rate while preserving a low-power consumption. Two different approaches have been identified to tackle this issue. In [4], the baseband computations are relegated to a custom baseband processor with an instruction set specifically designed for IoT protocols. In [5], the authors observe that LPWANs share very similar characteristics (i.e., the use of small bandwidths in sub-GHz bands), and therefore propose an architecture (shown in Fig. 1) with a single common RF front-end, a reconfigurable digital front-end (DFE) that executes the generic baseband operations (e.g., low-pass filtering), and a general-purpose processor that performs the protocol-specific computations.

In this paper, we follow the latter approach, which is the most flexible in our opinion, to implement a functional LoRa-compliant SDR on a general-purpose ultra-low-power (ULP) MCU. Whereas [5] evaluate in simulation the feasibility of demodulating generic GFSK signals on several processors, we present a real-time LoRa PHY implementation on a custom ULP MCU prototyped in 28nm FDSOI CMOS featuring a
DFE and an ARM Cortex-M4 CPU.

The remainder of this paper is organized as follows. We first briefly describe the LoRa protocol in Section II. We then explain the architecture of our SDR-capable MCU in Section III and we describe our software implementation of the LoRa PHY in Section IV. Finally, the performance of our SDR is experimentally evaluated in Section V.

II. THE LoRA PHYSICAL LAYER

LoRa is an IoT physical layer (PHY) that operates within the unlicensed sub-GHz ISM frequency bands [3]. In this section, we present the different blocks of the LoRa PHY and describe the computations carried out by a typical LoRa transceiver.

A. Modulation and Demodulation

LoRa uses a chirp spread-spectrum modulation, for which each symbol corresponds to a chirp, i.e., a complex phasor whose instantaneous frequency increases linearly with time. The duration $T_S$ of a symbol is $T_S = \frac{2SF}{B}$, where SF is the spreading factor and $B$ is the bandwidth of the chirp. Selecting a large spreading factor increases the symbol period, which in turn decreases the data throughput but enhances the communication range [3]. LoRa transceivers typically sample chirps at the Nyquist frequency $f_S = B$, implying that each symbol contains $N = 2SF$ samples. The range of valid spreading goes from 7 to 12 [3].

LoRa symbols are modulated by selecting the initial instantaneous frequency of the chirp, with $N$ possible different initial frequencies. The complex baseband-equivalent Nyquist-rate representation of a symbol $x_s[n]$ modulated with a symbol $s$ between 0 and $N-1$ is given by

$$x_s[n] = e^{j2\pi \left[ \frac{s}{N} + \left( \frac{n}{N} - \frac{1}{2} \right) \right]}$$

where $n \in \{0, \ldots, N-1\}$ is the sample index [6]. Thanks to time/frequency equivalence properties of the chirps, a LoRa symbol $s$ can be efficiently modulated by performing a cyclic shift of $s$ samples on the base waveform $x_0[n]$ [7]:

$$x_s[n] = x_0[(n-s) \text{ mod } N].$$

A LoRa receiver implements the following steps to demodulate a symbol. Let $y_s[n] = x_s[n] + w[n]$ be the received signal when the receiver is perfectly synchronized in time and frequency, where $w[n]$ is additive white Gaussian noise (AWGN). The receiver processes windows of $N$ samples, with each window containing one symbol. For every window, the sampled signal $\hat{y}_s[n]$ is first multiplied point-wise with $\hat{x}_0[n]$, the complex conjugate of the base waveform. Multiplying the received chirp by $\hat{x}_0[n]$ is called dechirping, as it removes the squared phase component from $y_s[n]$ but leaves the frequency term that depends on $s$ which carries the modulated information. The dechirped signal $\hat{y}_s[n]$ contains a single-tone term of frequency $\frac{s}{N}$ and AWGN such as

$$\hat{y}_s[n] = y_s[n] \cdot \hat{x}_0[n] = e^{j2\pi \frac{s}{N} n} + \hat{w}[n],$$

where $\hat{w}[n] = \hat{x}_0[n] \cdot w[n]$. The maximum-likelihood detector computes the $N$-point discrete Fourier transform (DFT) of $\hat{y}_s[n]$ [6]. Let $Y_k$ be the DFT of the dechirped signal $\hat{y}_s[n]$. In a noiseless scenario with perfect synchronization, $Y_k$ contains a single peak of height $N$ at the index $k = s$. To avoid a tracking of the phase, LoRa receivers commonly implement the non-coherent maximum-likelihood rule, which selects the DFT bin of greatest energy, i.e., $\hat{s} = \arg \max_k |Y_k|$ [6].

B. Synchronization and Preamble Structure

To demodulate a LoRa packet, the receiver first needs to synchronize with the transmitter. The synchronization of a LoRa receiver requires the correction of a carrier frequency offset (CFO) $\Delta f_c$ and a sampling time offset (STO) $\tau$ [8]. A receiver that is not synchronized in time retrieves windows of $N$ samples containing two consecutive partial chirps instead of a single entire chirp. The STO $\tau$ represents the sample-level time offset between the beginning of the window and the first sample of the second chirp in the window. The CFO $\Delta f_c$ represents the difference of carrier frequency between the transmitter and the receiver. Due to specificities of the chirp spread-spectrum modulation, the CFO and the STO can be decomposed into integer and fractional components:

$$\Delta f_c = \frac{B}{N} (L_{\text{CFO}} + \lambda_{\text{CFO}}), \quad \tau = L_{\text{STO}} + \lambda_{\text{STO}},$$

where $L_{\text{CFO}}$, $L_{\text{STO}}$ are integer numbers and $\lambda_{\text{CFO}}, \lambda_{\text{STO}}$ are fractional values in the range $[-0.5, 0.5]$ [8], [9]. Integer offsets shift the peak of a symbol after the DFT, initially located at the index $k = s$, to the bin $k = (s + L_{\text{STO}} + \lambda_{\text{CFO}}) \mod N$. On the other hand, fractional offsets scatter the energy of the symbol previously contained in a single bin over adjacent frequency bins. This scattering reduces the probability of correctly demodulating a symbol in the presence of AWGN [9].

To facilitate the synchronization, all LoRa packets start with a preamble, whose structure is illustrated in Fig. 2 [10]. The preamble contains eight repetitions of an upchirp (the base waveform $x_0[n]$), followed by two network identifier symbols and 2.25 repetitions of a downchirp. Downchirps are chirps whose instantaneous frequency decreases with time, i.e., the complex conjugate $\tau_0[n]$ of the base waveform and can be demodulated similarly to an upchirp by dechirping the sampled signal with its complex conjugate, i.e., an upchirp $x_0[n]$. The joint usage of upchirps and downchirps in the preamble is required to separately estimate the integer offsets [8]. The integer CFO can be estimated by summing the demodulated values $s_{\text{up}}$ and $s_{\text{down}}$ of an upchirp and a downchirp, respectively, and dividing their sum by two. The integer STO is then obtained by subtracting the estimate of $L_{\text{CFO}}$ from $s_{\text{up}}$.

C. Complete Tx and Rx Chains

Besides the modulation and demodulation stages, LoRa transceivers also perform some additional processing, as shown in Fig. 2. At the transmitter, the input payload bits are first whitened with a predefined pseudo-random sequence [10]. A header is also inserted before the whitened payload. This header indicates to the receiver the length of the payload, the chosen coding rate and the presence of an optional 16-bit cyclic redundancy check (CRC) at the end of the packet.
At this point, all bits in the packet are coded using a \((k, n)\) Hamming code with \(k = 4\) and \(n \in \{6, 7, 8\}\). The coded bits are then interleaved using a diagonal interleaver and, finally, the interleaved bits are mapped to symbols with a Gray code. The Rx chain starts when a preamble is detected. The receiver then synchronizes to the transmitter by estimating and correcting its CFO and STO. The received symbols are subsequently demodulated and mapped back to bits. After the reception of the entire packet, the receiver performs the deinterleaving, Hamming decoding and dewhitenining.

### III. MICROCONTROLLER ARCHITECTURE FOR IoT SOFTWARE-DEFINED RADIOS

In this section, we present the architecture of our ULP MCU codenamed SleepRider, illustrated in Fig. 3 which has been designed to run SDR implementations of IoT protocols. The MCU embeds an ARM Cortex-M4 CPU, two high-density 32kB SRAM memories, a Direct Memory Access (DMA) controller, a digital front-end (DFE) and several I/O peripherals. The Cortex-M4 follows a Harvard architecture, i.e., one SRAM acts as a program memory (PMEM) and stores the assembly instructions, whereas the other one is used by the CPU as a data memory (DMEM). Except for the PMEM, the CPU and all other peripherals share a single memory bus to exchange data. SleepRider MCU was designed for ULP in 28nm FDSoI with various techniques including ultra-low supply voltage (0.4V) for its logic.

The Cortex-M4 CPU is a 32-bit processor designed for low-power embedded applications and is a popular choice for commercial IoT MCUs. It features a three-stage pipeline and two single-instruction multiple-data (SIMD) lanes. SIMD instructions notably allow the CPU to efficiently execute DSP computations on pairs of Q16 fixed-point numbers. For instance, the SMUAD instruction performs two multiplications on two pairs of Q16 numbers and returns their sum in a single cycle. Such instructions are particularly useful to speed up complex baseband operations (e.g., FFTs) when complex samples are coded as pairs of Q16 numbers.

Our MCU architecture follows the one from [5], with a DFE that interfaces the RF transceiver with the DMEM. The DFE is a custom digital block that contains separate datapaths and control logic for the Tx and Rx chains. In Rx, the block retrieves digital samples from the RF chain at an oversampled frequency \(RF_S\). The rate at which the DFE retrieves samples, either in Tx or Rx, is hereafter called the DFE frequency. The oversampled samples are first low-pass filtered with a FIR filter and then decimated to the baseband frequency \(f_S\). The oversampling by a factor \(R\) at the input allows to achieve fine-grain time synchronization. When demodulating samples, the CPU selects the decimation index among the \(R\) parallel streams that minimize the sampling time offset. In Tx, the DFE directly transfers samples to the RF front-end without performing upsampling, i.e., the DFE frequency is set to the baseband frequency at which the CPU modulates symbols.

In either transmission or reception, the digital samples retrieved from or sent to the RF chain are complex baseband samples of 24-bit, i.e., the real and imaginary parts are both coded on 12 bits. Since the CPU contains two 16-bit SIMD lanes, these 12-bit words are extended to (resp. truncated from) 16 bits before entering (resp. leaving) the DMEM.

To alleviate the CPU load, the DMA controller is responsible for transferring the 32-bit complex baseband samples between the DMEM and the DFE. The memory transfers are organized as follows. The CPU first defines windows of \(L\) complex samples in the DMEM and indicates the length of these windows to the DFE. In Tx, when the CPU has filled a window with modulated samples, it configures the DMA to transfer the \(L\) 32-bit words to the DFE. The rate of the memory transfers is determined by the DFE frequency, i.e., the DFE processes one complex sample at a time and only requests a new sample to the DMA controller when it has transmitted the previous one to the RF front-end. Similarly, in Rx, the CPU first configures the DMA controller for \(L\) transfers, and the DFE then issues for each new decimated sample a 32-bit transfer request to the controller. When \(L\) samples have been transferred, the DFE raises an interrupt request (IRQ) to the CPU, indicating that the window has been transmitted (in Tx) or is ready to be demodulated (in Rx).

Since the proposed design aims to enable the implementation of multiple IoT protocols with different requirements (e.g., bandwidth, signaling rates), the DFE has been designed to be as flexible as possible. First, the DFE frequency is generated by an external clock, i.e., any frequency can be attained with

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**Fig. 2:** Transmit and receive chains of a LoRa transceiver (in blue), and structure of LoRa packets (in brown).

**Fig. 3:** Architecture of our SDR-capable microcontroller.
a dedicated clock generator. Frequency dividers in the DFE further allow the programmer to divide the external clock to obtain different sampling rates. The decimation rate at the output of the FIR filter can also be configured to obtain a specific baseband sampling frequency. Finally, the weights of the FIR filter are configurable and can be defined following the waveform specifications.

IV. SOFTWARE IMPLEMENTATION OF THE LoRA PHY

In this section, we describe our software implementation of the LoRa PHY for the MCU architecture presented in Section III. Our implementation is coded in C and relies on the ARM CMSIS DSP library, which provides many complex DSP routines optimized for the Cortex-M4. We first explain the Tx chain and then describe the Rx one. The latter is notably more complicated because of the synchronization stage.

A. Tx Implementation

In the Tx chain, all bit-level operations (whitening, Hamming coding, interleaving and Gray mapping) are straightforwardly implemented in C. To modulate LoRa symbols, we use the property given in Eq. (2) with a reference waveform \( x_0[n] \) stored in a buffer in the DMEM. The waveform \( x_s[n] \) of a symbol \( s \) can then be obtained by copying the sequence \( x_0[n] \) with a cyclic shift of \( s \) samples. To transmit symbols in real time, the software relies on two ping-pong buffers. The CPU computes modulated samples and stores them in one buffer, while the DMA controller transfers the samples from the other buffer to the DFE. After the transmission of an entire buffer, the DFE notifies the CPU with an IRQ and the roles of the ping-pong buffers are exchanged. If the CPU fills one buffer before the transmission of the other buffer, it goes to sleep and waits for an IRQ of the DFE. The DFE frequency is set at the Nyquist frequency \( f_S = B \) and the ping-pong buffers hence contain a single LoRa symbol of \( N \) complex samples each. Figure 4 shows the organization of the DMEM, in which all three buffers are stored. The reference waveform \( x_0[n] \) is generated only once in the Q16 fixed-point format, when the Tx chain is initialized.

B. Rx Implementation

Regarding the Rx chain, our receiver notices the arrival of a new packet when it consecutively demodulates three identical symbols \( \hat{s} \) (or its adjacent values \( \hat{s} \pm 1 \)), similarly to \([10]\). To perform a fast demodulation of the received samples, the Rx chain also uses two adjacent ping-pong buffers and a buffer storing \( x_0[n] \), the conjugate of the base waveform, as shown in Fig. 4. The DFE is configured to demodulate the received signal at the Nyquist frequency \( f_S = B \) after the low-pass filtering. When a buffer is full, the DFE notifies the CPU with an IRQ and the processor starts its demodulation by decirping the sampled signal with the sequence \( x_0[n] \) stored in memory and computing the FFT of the decirped symbol. All demodulation computations are executed in Q16 fixed-point to benefit from the SIMD instructions of the CPU. Similarly to the Tx chain, the CPU goes to sleep if it finished the demodulation of the current symbol before the end of the reception of the next one.

After the preamble detection, the receiver synchronizes to the transmitter using the algorithm described in \([9]\). The goal of the synchronization algorithm is to estimate and correct both the CFO and the STO using the preamble. The fractional CFO is first estimated by multiplying the DFT \( Y_k^{(2)} \) with the complex conjugate \( Y_k^{(-1)} \) of the DFT of the previous upchirp \([8]\): \( \hat{\lambda}_{\text{CFO}} = \frac{1}{2\pi} \angle \left( \sum_{i=-2}^{2} Y_k^{(2)} Y_k^{(-1)} \right) \) where \( s = \arg\max_{k} |Y_k^{(2)}| \). Once the fractional CFO estimate \( \hat{\lambda}_{\text{CFO}} \) is obtained, the reference signal \( x_0[n] \) is recomputed to directly include the correction term \( e^{-j2\pi \frac{\hat{\lambda}_{\text{CFO}}}{N}} \). The subsequent symbols are hence demodulated such that the fractional CFO is corrected. The receiver then iteratively estimates the fractional STO using the following estimator from \([9]\):

\[
\hat{\lambda}_{\text{STO}} = -\Re \left[ \frac{e^{-j2\pi \frac{\hat{L}_{\text{STO}}}{N}} Y_{i+1} - e^{-j2\pi \frac{\hat{L}_{\text{STO}}}{N}} Y_{i-1}}{2Y_i - e^{-j2\pi \frac{\hat{L}_{\text{STO}}}{N}} Y_{i+1} - e^{j2\pi \frac{\hat{L}_{\text{STO}}}{N}} Y_{i-1}} \right].
\]

A first estimate \( \hat{\lambda}_{\text{STO}} \) is obtained using Eq. (3) with the DFT \( Y_k^{(4)} \) of the fourth upchirp of the preamble and the approximation \( \hat{L}_{\text{STO}} \approx \arg\max_{k} |Y_k^{(4)}| \), since the integer STO cannot be estimated yet. The fractional STO, i.e., the intra-sample time offset, is corrected by updating the decimation index in the DFE among the \( R \) available polyphas. The receiver selects the decimation index that is the closest to the value \( R\hat{\lambda}_{\text{STO}} \). With both fractional offsets corrected, the remainder of the preamble is demodulated, which allows to retrieve the integer CFO and STO. Once \( \hat{L}_{\text{STO}} \) is estimated, the algorithm recomputes a more accurate estimate \( \hat{\lambda}_{\text{STO}} \) with \( \hat{L}_{\text{STO}} \) using Eq. (3) and updates the decimation index in the DFE.

After the processing of the preamble, the receiver starts the demodulation of the header and the payload. The receiver however needs to be aligned with the boundaries of the first header symbol by correcting the integer STO. To perform this
Fig. 5: Number of CPU cycles required to modulate or de-modulate LoRa symbols for different SFs. The demodulation stage is broken down in three substages: dechirping, FFT and magnitude computation of each FFT bin. The minimum CPU frequency required in Rx is obtained for $B = 125$ kHz.

correction in a simple manner, we treat the two adjacent ping-pong buffers as a single circular buffer of two symbols, as illustrated in Fig. 4. The DSP routines of the CMSIS DSP library required by the demodulation (complex multiplication, FFT and magnitude computation) have been rewritten to properly handle this circular buffer. The processor can hence start the demodulation of a symbol anywhere in the circular buffer, depending on $L_{STO}$. The integer CFO is corrected by subtracting the estimate $\hat{\text{CFO}}$ from the values of the demodulated symbols before the Gray demapping.

After the reception of the entire packet, the received bits are deinterleaved and decoded using a hard-decision Hamming decoder. If the header indicates the presence of a CRC, the CRC value is computed on the payload and checked against the one present at the end of the packet. If no errors are found, the payload bits are finally dewhitened and returned.

We finally note that due to the limited die size of the chip, our MCU design only embeds 32 kB memories. As a consequence, we are unable to run the Rx chain for SFs higher than 9 as the total size of the both the program and FFT tables exceeds the available space in the PMEM. Commercial MCUs however usually embed much larger memories (up to 512 kB).

C. Evaluation of the Minimum CPU Frequency

Finally, we analyze the efficiency of our implementation by determining the minimum CPU frequency needed to process LoRa packets in real-time. Figure 5 shows the number of CPU cycles required to modulate or de-modulate a LoRa symbol for several spreading factors. We observe that the demodulation of a symbol requires a greater number of cycles than the modulation. Whereas the modulation simply consists in copying $N$ samples in memory, demodulating a symbol notably involves an FFT of complexity $O(N \log N)$. Consequently, the demodulation of symbols with higher SFs requires more cycles than for lower SFs. However, the CPU has also more time to perform the FFT as the symbol duration $T_S$ depends on the SF. Hence, the minimum CPU frequency for real-time operation does not vary much with the SF. For $B = 125$ kHz, which is the typical bandwidth used in Europe [3], the minimum required frequency increases from 20.9 MHz to 23.2 MHz when increasing the SF from 7 to 9. Such frequencies are easily attained by ULP MCUs as they commonly have CPU frequencies in the range $32 \sim 180$ MHz [11]. We note that the minimum CPU frequency does not increase monotonically with the SF as the FFT implementation of the CMSIS library is more efficient for FFT sizes with an even power of two.

V. EXPERIMENTAL PERFORMANCE EVALUATION

We prototyped the architecture from Section III within the SleepRider MCU in 28nm FDSOI [12]. The fabricated MCU is integrated in a testbed to experimentally validate the proposed LoRa SDR LoRa and evaluate its performance. The testbed is shown in Fig. 6. Beside the MCU, it also contains a LimeSDR Myriad-RF1 LMS6002D reconfigurable transceiver board and a NI-USRP 2900. The Myriad-RF1 is used as RF front-end and transfers complex baseband samples from or to the MCU on a 12-bit bus with a sampling clock driven by the DFE [13]. The USRP is driven by a computer running the LoRa GNU Radio SDR implementation of [10], which is compatible with commercial LoRa radios.

We validated the functionality of both the Tx and Rx chains in the testbed for the SFs 7 and 8, $B = 125$ kHz and $CR = 4/s$, which gives raw data rates of 3.4 and 1.9 kbps, respectively. The frequency of the CPU is set at 64 MHz (generated internally) and the frequency of the external DFE clock is 2 MHz. In Tx, this clock is divided by 16 to obtain an internal DFE clock at 125 kHz. In Rx, the internal DFE clock is kept at 2 MHz and the decimation stage downsamples the received signal after low-pass filtering by $R = 16$. 

![Testbed with the SleepRider MCU, the Myriad-RF1 reconfigurable transceiver and a NI-USRP 2900 running the LoRa GNU Radio SDR implementation of [10].](image-url)
| Stage                  | % of time | Power (mW) | Energy (mJ) |
|------------------------|-----------|------------|-------------|
| Demodulation           | 30.32%    | 0.87       | 27.19 (62.69%) |
| Synchronization        | 0.44%     | 0.87       | 0.39 (0.91%)  |
| Decoding               | 0.17%     | 0.73       | 0.13 (0.30%)  |
| Wait for Interrupt     | 69.07%    | 0.22       | 15.67 (36.11%) |
| Average Total          | 100%      | 0.42       | 43.38 (100%)  |

TABLE I: Power characterization of the Rx chain when receiving a LoRa packet with a 11-byte payload for $B = 125$ kHz, SF = 8, CR = 4/s and a CPU frequency of 64 MHz.

We first analyze the energy consumption of the MCU when it receives a LoRa packet from the USRP for SF = 8 and a payload length of 11 bytes. The RF front-end is excluded from the power measurements. Table I gives the proportion of time spent and the energy consumed by the MCU in each stage of the Rx chain, including the state when the CPU has finished demodulating the current symbol and waits for an interrupt of the DFE to process the next one. In this breakdown, we include the demodulation of the preamble symbols in the demodulation stage. The synchronization stage thus only contains the additional computations needed for the estimation and correction of the STO and CFO. Overall, the Rx chain consumes an average power of 0.42 mW with a processing energy of 493 µJ/bit.

Finally, we assess the performance of our SDR Rx chain by measuring in the testbed the packet error rate (PER) versus the signal-to-noise ratio (SNR). In this experiment, we generate different SNR values by sweeping the Tx gain of the USRP. 1000 LoRa packets are transmitted per SNR level. The SNR is measured at the receiver side, similarly to [10]. Figure 7 shows both the simulation and experimental PERs as well as the theoretical PER of a perfectly synchronized receiver. The simulation results are obtained in MATLAB by simulating the Rx chain (synchronization, demodulation and decoding) in floating point with realistic CFO and STO values. For a target PER of $10^{-2}$ and both SF = 7 and SF = 8, we observe that our SDR implementation is only 0.2 dB away from the simulation results, and requires only 2.2 dB higher SNR than an ideal receiver. Moreover, the receiver fully benefits from the 2.8 dB spreading gain when increasing the SF from 7 to 8, in accordance with the theory.

VI. Conclusion

Compared to conventional radios implemented in hardware, IoT SDRs are a promising solution to extend the lifetime of IoT sensors. In this work, we demonstrate a ULP MCU embedding a reconfigurable radio digital front-end and a Cortex-M4 CPU that is capable of transmitting and receiving LoRa packets in real-time. Our software implementation of the LoRa PHY only uses the generic SIMD DSP instructions of the CPU to modulate and demodulate symbols. For a symbol bandwidth $B = 125$ kHz and a spreading factor SF = 8, the Rx chain requires a minimum CPU frequency of 20 MHz and consumes only 0.42 mW on average. To the best of our knowledge, this work is the first to experimentally demonstrate a complete and functional sub-mW SDR implementation of a modern LPWAN protocol on a ULP MCU. In future work, we will also implement the SigFox standard.

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