Open Loop Trans-conductance Amplifier design for Neural Signals

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Abstract. Robust neural recording systems require efficient amplification of weak neural signals at very first stage using Operational Trans-conductance Amplifier (OTA) which should consume minimum power, noise and area. However, there exist a tradeoff for improving the power, noise and area simultaneously. Open loop configuration of OTA has inherent property of lesser area due to absence of feedback; it also provides better noise performance under the given power budget as compared to closed loop counterparts. This paper focuses on the design of Open-loop amplifier OTA topology for non-invasive EEG signals. The simulation results show the improvement in the gain performance of the circuit at 180nm technology node while power and noise of the circuit remains comparable with the existing circuits.

1. Introduction
Efficient acquisition and recording of neuroelectric activity in brain provide assistance to identify diseases or uncontrolled state of a patient. Early-stage detection of neural ailments such as epilepsy, Parkinson’s disease, brain stroke, brain injury, brain tumour and autism etc. can support doctors to initiate the treatment for prolific results [1]. From last two decades researchers have developed different ways to measure these signals using invasive or noninvasive electrodes [2]. Table-1 summarises the neural signal modalities, which are measured invasively or noninvasively [3], [4].

| Neural signal modality        | Amplitude (μVpp) | Bandwidth (Hz) | Electrodes/ Invasive or Non-Invasive measurement |
|-------------------------------|-----------------|----------------|-----------------------------------|
| Extracellular action potentials (EAP) | 50 to 500       | 100 to 10k     | Metal/silicon microelectrode  |
| Intracellular action potentials (IAP) | 10,000 to 70,000 | 100 to 10k     | Glass micropipette                |
| Local field potentials (LFP)   | 500 to 5000     | 1m to 200      | Metal/silicon microelectrode  |
| Electroencephalogram (EEG)    | 1 to 100        | 1m to 100      | Surface electrode                |

Enhancement in integrated circuit technology has permitted the dependable non-invasive measurement of neural signals through EEG. EEG signals are an internal correlation of the Local field potential generated by the synchronous activity of thousands of neurons [5]. It is a minute neuroelectric signal having amplitude generally 1-100 μV with the frequency bandwidth 0.5-100 Hz. EEG is recorded regularly in present-day medical practice. Due to non-invasive nature, these signals can be acquired for longer durations without any harmful effects on the patient [6]. Many technical and scientific
achievements in neuroscience, robotics, and artificial intelligence followed after the discovery of the EEG machine in the early 1930s. Numerous methods and devices have been designed with the purpose of studying EEG. Current progression of internet of things technology requires low power and low noise circuits [7]. In neural signal recording systems, every electrode used for acquiring neural signal is followed by dedicated amplifier. Being the first stage of amplification, low-noise is the most important design requirement.

Many researchers have been working on the design of neural amplifier using different configurations. The large majority had used closed loop configurations using conventional amplifier topologies [8]. Very few have highlighted the use of open loop configuration for bio-potential signal amplification though it gives superior noise performance under the given power-budget. The closed-loop circuit architecture has been used frequently because it provides accurate gain, linearity and flexibility. However, the feedback loop increases the area and power consumption. Open-loop configurations offer an attractive solution to restrict power dissipation and area utilisation at the cost of linearity, gain control and low Power Supply Rejection Ration (PSRR), and Common Mode Rejection Ratio (CMRR) [9]. Since the power and noise performance of the entire system depends on the front-end amplifier, this paper focuses on the design of OTA using open-loop configuration.

The open-loop topology has inherent advantages of least area, high gain with low power consumption and even lower noise level [10]. However, achieving low power or low noise objectives simultaneously is difficult to achieve. Hollemen and Otis [9] reported use of a common-source amplifier for amplification of neural signals. The comparison with closed-loop designs underlined benefits of this approach. Frequency response, noise, CMRR, PSRR, the input offset currents, linearity, and crosstalk were given special consideration. The circuit current was restricted to a single common source branch which helped in achieving low power dissipation. Also, current-reuse technique improved the noise performance of the circuit. Chaturvedi and Amrutur [10] have compared both closed loop and open loop mentioned the effect of non-linearity introduced by the pseudo-resistor in feedback loop. In this paper, telescopic configuration was used to implement the OTA with current stealing branches. Other amplifier designs Saberhosseini et al. [11] highlighted the use of telescopic configuration with auxiliary transistors to reduce the current in differential pair; hence, lowering the input referred noise of open-loop OTA.

In this paper, we have examined open-loop OTA configuration using single stage common source amplifier configuration on 0.18µm technology node BSIM3V3 MOS Transistor Model from Cadence Virtuoso. Section 2 discusses the design and implementation of the open-loop OTA. Section 3 presents the results obtained from the sizing and the comparison with the existing literature and Section 4 concludes the paper.

2. Design and implementation of Open-Loop OTA topology

2.1. Low-power operation in sub-threshold region of MOSFET

Power utilisation can be reduced by decreasing either total bias current in the circuit or supply voltage or both. However, decreasing input current affects the dynamic range of the amplifier, whereas reducing the supply voltage moves transistors into a triode or cut-off region. Conversely, the operation of MOSFET in weak inversion (sub-threshold) region has been advantageous for low-power and low-bandwidth biomedical amplifier circuits [12].

In a moderate and weak inversion, the inversion layer charge is an exponential function of gate voltage, which is less than the threshold voltage \( (V_{th}) \) [13] as shown in Fig. 1. The inversion charge exponentially varies with gate potential in the weak inversion region, linearly depends on gate potential in strong inversion and moderate inversion is the transition region between the two. Thus, the transistor operation in the sub-threshold region or moderate region is possible below threshold voltage and current flows is the diffusion current, which helps in low-power operation. However, the reduction in power comes with the reduced speed of operation which turns out to be favourable for Bio-medical circuits where the signal is of very low frequency [4].
2.2. $g_m/I_D$ methodology

The $g_m/I_D$ methodology addresses the challenges in the construction of low power and low noise design and optimises device dimensions of MOSFETs used in OTA [14]. As discussed in previous section, reduction in power consumption can be achieved by operating MOSFETs in weak inversion/ moderate region [15]. Therefore, standard square law equations followed by most of the textbooks cannot be straightforwardly used for defining the MOSFET dimensions. 

Enz Krummenacher Vittoz (EKV) model and Berkley Short-channel MOSFET (BSIM) models exploit the equations in weak and moderate regions [16], [17]. However, solving the complicated equations for obtaining device dimension from these models is not agreeable in case of traditional hand calculations [18]. The $g_m/I_D$ methodology bridges the gap between the hand calculations and simulations obtained from circuit simulator. The dataset generated by the simulation replaces simple inaccurate models sweeps for different values of Length (L) of the MOSFET. Normalized transistor parameters vs. $g_m/I_D$, Figure of Merit vs. $g_m/I_D$ plots are obtained to find the optimised values of aspect ratios ($W/L$). Also, once the data set is generated for $g_m/I_D$ for a given technology node, it can be used again in the form of lookup tables and simplifies the design procedure. A simple MATLAB script can be written to get the graphs of $g_m/I_D$ dataset, and the transistor dimensions can be obtained.

The $g_m/I_D$ methodology has been elaborated in [19]. The same is used to design the EEG amplifier using the open loop topology described in [9]. The procedure and the desired characteristics are kept the same to design low-noise, low-power and minimum area amplifier of EEG signals. The schematic used for Open-loop topology is shown in Figure 2. Nonexistence of feedback loop leads to a lesser number of circuit components in Open-loop topology. Thus, low power consumption is the integral property. According to [10] open loop also introduces larger offset than closed loop amplifiers. But proper compensation and design strategy can overcome these disadvantages.

3. Results & Discussions

To reduce the noise, Holleman and Otis [9] used two strategies while exploiting simple common-source amplifier. First, the number of current branches was reduced, i.e., the amplifier had only one branch which operates at full current, thus reducing power and noise in the circuit. Second, the input was also
attached to the active load device, thus driving both MP1 and MN1; this increases the gain of the amplifier, while the noise remains constant. In this work, same OTA designed for EEG amplification including devices MN2-MN4, which allowed controlling the gain and noise of the amplifier by reducing the aspect ratio at the same $V_{GS}$, thus limiting the gain.

Now, considering the amplification of low frequency EEG signals, bias current of 74 nA was set for the circuit, such that Bandwidth of 1 Hz to 30 Hz, DC gain=100 and Mid-band gain $A_M=40$ dB could be achieved. Value of input capacitors, $C_1=20$ pF and load capacitance, $C_L=50$ pF was considered. As a result, MOSFETs MN1 & MP1 operated in the sub-threshold region. Measurement of Open-loop Gain, Differential Gain, Common Mode Gain, Noise analysis, and power analysis were performed using virtuoso Analog Design Environment (ADE). Minor modifications were made to do stability analysis. The values of W/L were tweaked multiple times to get down to the acceptable measurements for all parameters. Table 2 shows the operating conditions and W/L ratios of all the transistors in the circuit.

Table 2. Operating points of common source open-loop OTA MOSFETs

| Device | $W/L(\mu m)$ | $I_D$ (nA) | $g_m/I_D$ (S/A) | Operating region |
|--------|-------------|------------|----------------|-----------------|
| MN1    | 60/8        | 74         | 22             | Sub-threshold   |
| MP1    | 60/4        | 74         | 17             | Moderate        |
| MP0    | 6/4         | 74         | 21             | Sub-threshold   |
| MN2    | 0.6/8       | 5          | 21             | Sub-threshold   |
| MN3    | 0.6/16      | 2.5        | 22             | Sub-threshold   |
| MN4    | 0.6/20      | 1.8        | 25             | Sub-threshold   |

The simulation results of the gain and phase are shown in Figure 3 (a) & (b) for different gain settings. The gain settings are changed by switching the devices MN2-MN4. A total of seven combinations are considered as G [001, 010,100,011,101,110,111]. At highest gain setting, i.e., G [001,010,100], the amplifier exhibits the gain of 45.88 dB and Unity Gain Bandwidth (UGB) of 0.34 MHz, which is much higher for EEG signal amplification. Intermediate gain at G[011,101,110] of 42.75 dB and lowest gain at G[111] of 38.77 dB is obtained. The flicker noise (1/f noise) dominates in the circuit giving a total integrated input referred noise of 127 µVrms; thus the NEF obtained is 6.2. The total simulated power dissipated by the circuit is 2.39 µW. The operation of the transistors in the subthreshold region lead to the lower power dissipation, however, the higher input referred noise was obtained despite of using large size transistors. Also, considering the lower cut-off frequency of the amplifier to 3mHz for EEG signals, the flicker was very high as given in (1).

$$\n^2_{\text{Flicker}} = \frac{K}{C_{OX}WL} \frac{1}{f}
$$

Figure 3. Simulation results of (a) open loop gain (b) phase with three different gain settings for common source open loop amplifier for EEG

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$$\n^2_{\text{Flicker}} = \frac{K}{C_{OX}WL} \frac{1}{f}
$$

where $K$ is process-dependent constant $= 10^{-25}$ V^2 F, $C_{OX}$ is the oxide capacitance, $f$ is the frequency, $W$ and $L$ are width and length of the transistor. The circuit has to be further optimized for reducing the value of noise.
Table 3 summarizes the simulated results of the open-loop-amplifier and gives the comparison of the Open-loop topology with the existing open-loop topology based neural amplifiers. Also the results are compared with the designed GD-Current-mirror neural amplifier. (9) and (10) are two significant contributions in Open-loop design of neural amplifier. The designed amplifier provides better gain and low frequency cut-off; however, the circuit can still be optimised for improvement in noise and power.

| Reference | Technology node (µm) | Gain (dB) | Bandwidth (Hz) | Noise (µV/√Hz) | Supply Voltage (V) | Power consumption (µW) | PSRR (dB) | NEF |
|-----------|----------------------|-----------|-----------------|----------------|--------------------|------------------------|-----------|-----|
| [12]      | 1.5                  | 39.5      | 0.025-7.2k      | 2.2            | ±2.5               | 0.9                    | >85       | 4.8 |
| [9]       | 0.5                  | 36-44     | 0.3-4.7k        | 3.5            | 1                  | 0.805                  | 5.5       | 1.8 |
| [10]      | 0.13                 | 37        | 5-7k            | 5.5            | 1.5                | 1.5                    | 67        | 2.58|
| [11]      | 0.5                  | 62        | 0–4M            | 0.059          | 3                  | 4.04                   | N/A       | N/A |
| [20]      | 0.13                 | 40.5      | 0.4-8.5k        | 3.2            | 1                  | 12.5                   | 60        | 4.5 |

This work 0.18 38.77-45.88 .003-0.34M 127 1.8 2.39 ≥50 6.2

PSRR: Power Supply Rejection Ratio
NEF: Noise Efficiency Factor

4. Conclusion
In this paper, common-source open-loop amplifier topology was used to realize OTA for EEG amplification. The designed amplifier was simulated using Cadence Virtuoso 180nm technology. Different performance metrics of the designed OTA were evaluated and the gain of 38.77-45.88 dB was obtained for different load setting. The power consumption of the circuit was 2.39 µW and NEF of 6.2 was obtained which can further be improved. Further, the absence of feedback loop makes this amplifier topology suitable for area constrained neural recording systems.

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