A high linearity, 8-GSa/s track-and-hold amplifier in GaAs HBT technology

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Abstract: A high linearity full differential 8 GSa/s track-and-hold amplifier (THA) is presented in this paper. The proposed THA is designed and implemented using 2-µm GaAs HBT technology to be targeted for faster operation in sampling systems at a clock frequency of GHz. In this THA, an alternative switch emitter follower (SEF) is used as a switching stage with a Schottky diode for hold-mode isolation enhancement and high-speed operation. In conjunction with well-designed input buffer allows us to achieve high linearity and comparable dynamic performance. Measured small signal −3 dB bandwidth, and hold-mode isolation are better than 3.6 GHz and 40 dB, respectively. The prototype achieves a spurious-free dynamic range (SFDR) of 43.9 dB at 0.5 GHz and an average total harmonic distortion (THD) below −40 dBc up to a first Nyquist frequency of 4 GHz. This work has the potential for wideband, high speed and low distortion analog to digital converter (ADC) used in the future direct sampling systems.

Keywords: gallium arsenide, high-speed sampling, track-and-hold, non-linear distortion, Schottky diodes, MMICs

Classification: Integrated circuits

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1 Introduction

In modern wireless communication systems, information contents drastically increase, and the need for high data rate transmissions results in an emerging replacement from conventional narrowband sampling receivers to wideband direct sampling counterparts [1]. The front-end RF analog to digital converter (ADC) therein is critical because it directly converts the RF signal from the antenna and hence featuring faster operation. The track-and-hold amplifier (THA) is a key component for a high-speed ADC, it tracks an analog signal and holds it during conversion. THA performance is essential to the overall dynamic performance of ADCs because it must operate full rate to avoid timing mismatch and provide high linearity. Therefore, THA should have a good linearity and a wide dynamic range at high sampling rates. In the existing THA architectures, the switched capacitor stage is the basic way to realize THA circuit, but it suffers from a large timing jitter problem [2]. Moreover, diode-bridge (DB) [3] and switched emitter follower (SEF) stages [4] are widely used in GSa/s THA. However, for the DB stage, the mismatching problems between positive and negative current source or pulse drivers makes it difficult to achieve a good linearity and a wide dynamic range.
In the conventional SEF stage, insufficient isolation cannot minimize the input feedthrough [5] and the emitter follower can also show the ring or oscillation when drives a large capacitor hence resulting in potential instability [6].

In order to achieve a high performance on-chip THA, this paper proposes an alternative THA architecture by adding a series sample diode to the emitter follower of the conventional SEF stage. Here, Schottky diode is used as series sample diode to avoid the electron minority charge storage for high-speed requirement while providing good isolation. Moreover, input buffer in this THA configuration is also well-designed for high linearity requirement. The prototype is implemented in 2-µm GaAs HBT technology. Although many high-speed high linearity THAs have been reported using InP, SiGe and advanced CMOS process [7, 8, 9, 10], GaAs HBT has a number of advantages for fast THA circuits, such as high $g_m$, good $V_{BE}$ matching and commercial maturity. This work detailed the circuit design and measurements of a high linearity 8 GSa/s sampling rates GaAs HBT MMIC THA for future high-speed ADC used in direct conversion receivers.

2 GaAs HBT MMIC THA design

2.1 Circuit topology

![Fig. 1. the schematic of the proposed GaAs HBT THA.](image)

The whole THA transistor level schematic is shown in Fig. 1, which contains a full differential input buffer, an output buffer and two track-hold (T/H) switches. The proposed switching structure is enclosed in the gray box, which consists of Schottky sampling diodes $D_1$ ($D_2$) and the driving circuits with the conventional SEF configuration to switch the new switching stage. GaAs heterojunction bipolar transistors (HBTs) are used here due to their relatively high $f_T$ for high rates and good $V_{BE}$ matching for high linearity [11]. In addition, two feedthrough compensation capacitors $C_F$ are also added to eliminate the hold mode signal feedthrough, theoretically, this feedthrough can be completely cancelled when $C_F$ equals to the base-emitter junction capacitance of switching transistor $Q_2$ ($Q_4$). However, the base-emitter junction capacitance varies with the bias of the transistor, in order to minimize the hold mode feedthrough, a $C_F$ structure shown in Fig. 1 is used [12].
Choice of sampling diode is critical for this THA design. There are substantial minority carriers stored in both the N+ and P+ regions of the base-collector (BC) junction of the GaAs/AlGaAs HBT device when the PN junction is forward-biased, resulting in longer time to recovery. In order to avoid this charge storage from transistor $Q_1$ ($Q_5$), Schottky diode can be used as a sampling diode in this proposed design. Fig. 2 shows a small-signal equivalent circuit model of the Schottky diode [13]. In addition to general junction capacitor $C_{dep}$ and parasitic series resistor $R_s$, in small-signal behaviors, the Schottky diode also has dynamic resistor $r_D$, which is expressed as $r_D \approx kT/q(I + I_S)$, where $I$ and $I_S$ are forward biased current and reverse biased saturation current, respectively. Usually, $I \gg I_S$ hence that $r_D$ is simplified as $r_D \approx kT/qI$. For the Schottky diode with its area of 100 $\mu$m$^2$ in this design, the forward turn-on current is about 6 mA, based on the given device model from Sanan foundry, three model parameters of Schottky diode can be determined, $R_s = 3.74\ \Omega$, $r_D = 4.29\ \Omega$ and $C_{dep} = 207.24\ fF$. In this THA with hold capacitor $C_H$, the $r_D \cdot C_{dep}$ is a key device merit and it is noted that in this diode model, $r_D \cdot C_{dep}$ is about 0.9 ps, a small time constant for a high-speed THA. At the same time, Schottky diode has smaller junction parasitic capacitance to provide higher off-state isolation than SEF’s base-emitter junction, which can improve the performance of THA during hold mode.

![Fig. 2. Small-signal equivalent circuit of Schottky diode.](Image)

### 2.2 Well-designed input buffer

In order to obtain a high linearity performance, a full-differential input buffer has been carefully designed. The distortion analysis procedure is given below. To begin with the simplified half circuit of the input buffer for the track mode, the corresponding ac small-signal model are shown in Fig. 3(a) and (b), respectively. In track mode, the primary distortion sources are the modulation of the base-emitter voltages ($\Delta v_{be1}$, $\Delta v_{be2}$, $\Delta v_{be3}$) of transistors and the forward voltage ($\Delta v_D$) of the sampling Schottky diode arising from currents passing through these junctions. Therefore, the distortion can be modeled with Taylor series at third order ($v_{out} = a_1v_{in} + a_2v_{in}^2 + a_3v_{in}^3$) to obtain the sum of these independent distortion sources at the overall output. With two-tone input signal $v_{in} = V_Acos(\omega_1t) + V_Acos(\omega_2t)$, the third terms will be generated as intermodulation distortion at frequencies $\omega_1$ and $\omega_2$, whose amplitude is $IMD_3$ relative to their linear output and its expression is expressed as $IMD_3 = 3a_3V_A^2/4a_1$. It is noted that the $a_1$ here is the small-signal gain of the circuit in Fig. 3(a), it can be determined by Kirchhoff’s law using the small-signal equivalent circuits in Fig. 3(b). On the other hand, the perturbation technique [14] and the superposition principle can be used to determine the coefficient $a_3$, the steps can be simplified as follows: 1.) Calculating the
It is noted that the linear and second-order term (diode contribution of each distortion source of Eqn. (2)) is the total contribution to the output, where \( \mathbf{a} = [a_1, a_2, a_3, a_4]^T \) is the coefficient vector determined by Fig. 3(b) and \( T \) represents the transpose of a matrix. These small-signal perturbation voltages \( \Delta V_x \) are computed using the small-signal junction currents \( \Delta i_x = [\Delta i_{c1}, \Delta i_{c2}, \Delta i_{c3}, \Delta i_D]^T \) in Taylor series expansion manner. By omitting the linear and second-order term (differential configuration), the distortion perturbation term contains only the third order term, that is,

\[
\Delta V_x^{3rd} = \left[ \frac{1}{3!} \frac{\partial^3 V_{BE}}{\partial I_{DC}^3} \right]^T \cdot \Delta i_x^3
\]

It is noted that \( I_{DC} = I_s \cdot \exp(V_{BE}/V_T) \). On the other hand, the relationship between \( \Delta i_x \) and \( v_i \) is easily obtained according to Kirchhoff's law from Fig. 3(b), which is

\[
\Delta i_x = b \cdot \Delta v_i,
\]

similarly, where \( b = [b_1, b_2, b_3, b_4]^T \) is the coefficient vector. Finally, the total third distortion in the output and coefficient \( a_3 \) are derived as shown in Eqn. (2).

\[
\Delta V_o^{3rd} = v_i^3 \cdot \left( \frac{V_T}{3I_{DC1}^3} a_1 b_1^3 + \frac{V_T}{3I_{DC2}^3} a_2 b_2^3 + \frac{V_T}{3I_{DC3}^3} a_3 b_3^3 + \frac{V_T}{3I_{DCD}^3} a_4 b_4^3 \right)
\]

After some mathematics efforts and considering reasonable design conditions (i.e. \( R_{EE} = R_{EE1} = R_E, \quad I_{DC3} = I_{DC1} = I_{DC}, \quad I_{DC2} = kI_{DC}, \quad I_{DCD} = (k-1)I_{DC}, \quad g_{m3} = g_{m1} = g_m, \quad g_{m2} = kg_m \)), the expression of IMD3 can be obtained as shown in Eq. (3).

\[
IMD3 = \frac{V_T^4}{4I_{DC}^5} \left( \frac{R_L}{1/kg_m} (R_{EE} + 1/g_m)^3 \right) \times \left[ \frac{(Z_L - R_L)^3}{k^3 (Z_L + 1/kg_m)^3} - \frac{1/kg_m + R_L}{R_{EE} + 1/g_m} \frac{(1/kg_m + R_L)^3}{(k-1)^3 Z_L (Z_L + 1/kg_m)^2} \right]
\]

![Fig. 3. (a) Simplified half circuit of the input buffer in track mode. (b) Corresponding ac small-signal equivalent circuit.](image)
where $Z_L = X_C + r_D$, $X_C$ is the impedance of hold capacitor $C_H$ and thermal voltage $V_T \approx 26$ mV at room temperature. Fig. 4 gives the input third-order intercept point ($IIP_3$) value from simulation and Eqn. (3), respectively, it shows that the results calculated from Eqn. (3) have a good consistency with CAD simulation and provide insight into the circuit distortion sources.

Assuming $Z_L$ is ignored and $k$ is equal to 1, it can be proved that $IMD_3$ is the smallest, when $R_{EE} = R_L$. In fact, $R_{EE} \neq R_L$ due to the frequency dependence of $C_H$. The input buffer presented here exhibits a high linearity under some specified design conditions from measurement results (shown in Fig. 10). Above distortion analysis is a part of the small-signal circuit analysis, which can be used to guide high-performance circuits design in a more rigorous way.

2.3 THA layout and fabrication

In this design, the eventual sizes of capacitors, resistors and clock path are determined by simulations and optimizations in Keysight Advanced Design System software in order to prevent from unpredictable crosstalk or spike. The presented circuit has been implemented in a 2-µm GaAs HBT technology. The chip photo of the proposed alternative THA is shown in Fig. 5 with a size of 1.1 cm$^2$. In addition, this prototype has a fully differential input and output structure, so a good symmetrical layout should be considered to suppress even-order components effectively.

3 Measurement results

The proposed alternative THA is measured via on-wafer with 150 µm spacing Infinity GSGSG dual probing arms. All measurements are performed at a single supply voltage of 5 V, provided by HP 6624A dual channel DC power supply, the quiescent current of this THA is 97.8 mA. S-parameters are measured using Agilent PNA-X N5247A Four-port Network Analyzer. The linearity and dynamic characterization have been carried out with a continuous-wave signal using two Agilent...
E8257D analog signal generators and AV4051 Signal Analyzer. Lecroy Wave-Master 820Zi-B oscilloscope is used to display the output waveform. All differential sampling clock signals are generated externally by Agilent N4903B pulse pattern generator. The Hyperlabs HL9405 wideband balun is used to implement the function of converting a differential signal to a single-ended output. In addition, the spectral behavior of this THA also has been evaluated with fast Fourier transformations (FFTs) in MATLAB for more features, such as THD, SNDR, SNR, etc. The whole instrument setup and connections are shown in Fig. 6.

The measured small signal S-parameters are shown in Fig. 7. The track-mode −3 dB bandwidth is from DC to 3.6 GHz. Because Schottky diodes are used as a part of the switching stage, during the hold-mode, this prototype exhibits a good isolation of better than 40 dB over the bandwidth. The differential input signal and THA stable time-domain output voltage waveform are plotted in Fig. 8, where the input frequency is 0.5 GHz with a clock frequency of 8 GHz and tracking periods are marked in gray regions. The corresponding measured spectrum is shown in Fig. 9, in which the SFDR is 43.9 dB and calculated THD is −42.5 dBc. It is
Fig. 7. The measured track-mode gain and hold-mode isolation of the proposed THA.

Fig. 8. Measured 0.5 GHz differential input and THA output signals at a sampling rate of 8 GSa/s.

Fig. 9. The output spectrum with an input signal of 0.5 GHz and a sampling clock of 8 GSa/s.
noted that even harmonics are suppressed due to the full differential structure of this THA.

The measured SFDR, IIP3 and THD performance versus frequencies are plotted in Fig. 10 with a sampling rate of 8 GSa/s. The results indicate that this proposed THA has IIP3 values more than +20 dBm over 0.5–4 GHz input frequency range, which proves that the good linearity is achieved due to the well-designed buffer circuit. The measured average SFDR is better than 40 dB over the first Nyquist input bandwidth of 4 GHz. Based on the measurement data, the calculated results show that the average value of THD is −40.8 dBc.

![Fig. 10. Measurement SFDR, IIP3 and THD of this proposed THA at 8 GSa/s sampling rate.](image)

Measured results are compared to recent literature in Table I. The proposed THA exhibits a relatively wide bandwidth, high sampling rate, and good dynamic performance while showing comparable DC power consumption ($P_{DC}$) performance and die area.

|               | This work | [7] | [8] | [9] | [10] |
|---------------|-----------|-----|-----|-----|------|
| **BW (GHz)**  | 3.6       | 1   | 3   | 2.5 | 15   |
| **fs (Gs/s)** | 8         | 2.8 | 12  | 5   | 1    |
| **SFDR (dB)** | 43.9      | 61  | 40.9| 46  | 45   |
| **THD (dBc)** | −42.5     | −   | −40.6| −43.0| −38.7|
| **P_{DC} (mW)** | 489      | 1400| 197 | 48.8| 2100 |
| **Area (mm²)** | 1.32      | 0.60| 0.90| 1   | 2.24 |

| **Process** | GaAs HBT |
|-------------|----------|
| **SiGe**   | BiCMOS   |
| **Si**     | CMOS     |
| **Si**     | CMOS     |
| **InP**    | HBT      |

### 4 Conclusion

This work has developed a high linearity 8 GSa/s sampling rate track and hold amplifier using the GaAs HBT technology, which demonstrates relatively wide
bandwidth and high linearity performance. Schottky diodes are used as the switching elements of THA to achieve a high hold-mode isolation and a high-speed operation. In addition, a low distortion input buffer is discussed and well-designed with a nonlinear analysis. All above functions are integrated into a MMIC THA with a size of $1.1 \times 1.2 \text{mm}^2$, and the eventual measured results demonstrate a high sampling rate, a wide dynamic range, a good linearity and a relatively wide input bandwidth, compared with the prior art. These results indicate a good performance and a great potential for providing high-speed THA modules used in the future advanced sampling systems.

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