An SIE Formulation With Triangular Discretization and Loop Analysis for Parameter Extraction of Arbitrarily Shaped Interconnects

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Abstract—A surface integral equation (SIE) formulation under the magneto-quasi-static assumption is proposed to efficiently and accurately model arbitrarily shaped interconnects in packages. Through decently transferring all electromagnetic quantities into circuit elements, the loop analysis is used to carefully construct matrix equations with an independent and complete set of unknowns based on graph theory. In addition, an efficient preconditioner is developed, and the proposed formulation is accelerated by the pre-corrected fast Fourier transform (pFFT).

Four practical examples, including a rectangular metallic interconnect, bonding wire arrays, interconnects in a real-life circuit, and the power distribution network (PDN) used in packages, are carried out to validate its accuracy, efficiency, and scalability. Results show that the proposed formulation is accurate, efficient, and flexible to model complex interconnects in packages.

Index Terms—Interconnects, loop analysis, parameter extraction, pre-corrected fast Fourier transform (pFFT), surface integral equation (SIE).

I. INTRODUCTION

INTERCONNECTS are widely used in 2.5-D/3-D packages and integrated circuits (ICs) [1], [2]. The power integrity/signal integrity (SI/PI) is vital to be considered in the design of interconnects in the high-frequency region for its performance [1], [2], [3], [4]. Circuit parameters, such as parasitic resistance and inductance, are essential to the design of SI/PI [2], [5].

To accurately and efficiently extract those parameters of complex interconnects in packages, many efforts have been made in the past few decades. Several volumetric integral equation (VIE) formulations are proposed to extract the wideband resistance and inductance. FastHenry is one popular open-source solver based on the magneto-quasi-static (MQS) VIE formulation in conjugate with a mesh analysis, and currents are assumed to mainly flow in the longitude direction [6]. However, since electric currents significantly crowd toward surfaces of conductors in the high-frequency region, extremely fine meshes are usually required to accurately model the skin effect in highly lossy interconnects. Then, several full-wave VIE formulations are proposed to model interconnects under exterior electromagnetic waves or complex inhomogeneous media [7], [8], [9].

To improve the computational efficiency, surface integral equation (SIE) formulations are proposed to extract parameters of interconnects. Those formulations usually show performance improvements over their volumetric counterparts, since unknowns only reside on the surfaces of interconnects. For example, several full-wave methods based on the SIE formulations are developed in [10], [11], [12], [13], [14], [15], [16], [17], and [18], which can obtain accurate and robust results and solve the complex structures with dielectric and conductors. However, the resource consumption is large for them, especially when complex circuit structures are considered. An open-source full-wave solver, namely, FastImp [19], was also developed to model arbitrarily shaped conductors. The electro-magneto-quasi-static (EMQS) formulation is an approximation of full-wave formulation, in which Green’s function is approximated as static function in free space, like [20], [21], [22], [23]. Especially, the EMQS formulation can be further approximated as the MQS formulation if there is no charge assumption on the surface, like [24] and the commercial solver Ansys Q3D [25]. The quasi-static formulations are more simple and efficient but they have some limitations, especially for the frequency as the dimension of structures should be electrically small. Many SIE and VIE formulations based on a circuit theory, namely, the partial element equivalent circuit (PEEC) methods, are proposed to model circuit structures [26], [27], [28], [29], [30], [31], [32], [33], [34]. In those formulations, electromagnetic quantities are interpreted as circuit elements, and then external excitations are applied for impedance extraction. In quasi-static formulations, the nodal analysis or modified nodal analysis (MNA) [35]
is commonly used to apply the charge conversation condition.

In this article, a novel loop analysis based on the graph theory is proposed to deal with the MPIE [36], [37], [38] formulation under MQS assumption. Through the loop analysis, the dimension of matrix can be reduced significantly and the external voltage sources can be applied conveniently. All the electromagnetic quantities are decently transferred into circuit elements according to the PEEC methods [22], [23].

In addition, the classical pre-corrected fast Fourier transform (pFFT) [39], [40] is successfully tailored to solve the matrix equation, and a new preconditioner is developed to efficiently accelerate the convergence of iterations. We carried out four practical examples from simple to complex structures, including a rectangular metallic interconnect, bonding wire arrays, interconnects in a real-life circuit, and the power distribution networks (PDNs) used in packages, to validate its accuracy, efficiency, and scalability.

This article is organized as follows. In Section II, some background configurations, including the MPIE formulation, MQS assumption, triangular discretization, unnormalized Rao–Wilton–Glisson (RWG), and PEEC method, are introduced. The reasonability of such configurations is explained. In Section III, the loop analysis with the graph theory is detailed to apply the charge conservation condition and voltage sources. The pFFT algorithm is briefly introduced and an efficient preconditioner is developed in Section IV. Then, four numerical examples are carried out to validate the accuracy and efficiency of the proposed loop-analysis method and preconditioner in Section V. Finally, we draw some conclusions in Section VI.

II. SIE FORMULATION FOR LOSSY INTERCONNECTS

A. MQS SIE Formulation

Without loss of generality, external excitations are not included inside interconnects. The electric field in the exterior space can be expressed as

\[ \mathbf{E} = -j \omega \mathbf{A} - \nabla \Phi \]  

(1)

where \( \mathbf{E}, \mathbf{A}, \) and \( \Phi \) are the electric field, the vector potential, and the scalar potential, respectively. \( \omega \) denotes the angular frequency. \( \mathbf{A} \) can be expressed in terms of the electric current density and Green’s function as

\[ \mathbf{A} = \mu_0 \int \mathbf{G}_0(\mathbf{r}, \mathbf{r'}) J(\mathbf{r'}) \, d\mathbf{r'} \].  

(2)

By substituting (2) into (1), we have

\[ \mathbf{E} = -j \omega \mu_0 \int \mathbf{G}_0(\mathbf{r}, \mathbf{r'}) J(\mathbf{r'}) \, d\mathbf{r'} - \nabla \Phi \]  

(3)

which is the well-known MPIE. In this article, we consider that the skin effect is well-developed in the high-frequency region. Therefore, electric currents mainly flow toward the perimeter of interconnects. The surface impedance operator can be used to relate the tangential electric field to the surface current density, which is given by

\[ Z_s = \sqrt{\frac{j \omega \mu}{\sigma}} \]  

(4)

where \( \sigma \) is the conductivity of the interconnect. It should be noted that (4) is only valid in the high-frequency region, where the skin effect is well-developed. When parameters in the low-frequency region are considered, other impedance operators, such as the generalized impedance boundary condition [41], [42], [43], should be used.

By considering lossy effects imposed by (4), (3) can be modified as

\[ \mathbf{Z}_s \mathbf{J}(\mathbf{r}) + j \omega \mu_0 \int \mathbf{G}_0(\mathbf{r}, \mathbf{r'}) \mathbf{J}(\mathbf{r'}) \, d\mathbf{r'} = -\nabla \Phi. \]  

(5)

Equation (5) is the SIE formulation to model lossy interconnects.

Since interconnects in packages are considered in this article, of which the large typical sizes are only several millimeters, the MQS assumption can be safely used. Therefore, the static Green’s function in free space is used in (5), which is given by

\[ \mathbf{G}_0(\mathbf{r}, \mathbf{r'}) = \frac{1}{4\pi |\mathbf{r} - \mathbf{r'}|}. \]  

(6)

Besides static Green’s function, there is no charge density on the surface under MQS assumption, which implies the electric charge conservation condition, namely, \( \nabla \cdot \mathbf{J} = 0 \). In Section III, the loop analysis will be introduced to enforce it.

B. Surface Discretization Through Triangles

Generally, volumetric or surface elements, such as tetrahedron, filament, triangle, and panel, are used to divide interconnects into small ones to calculate numerical results. Volumetric elements are usually applied in VIEs, such as filaments in FastHenry [6], voxels in VoxHenry [44], and tetrahedrons in [7], which lead to prohibitively large modeling errors of complex structures or computational cost in terms of runtime and memory to model the well-developed skin effect. For surface elements, rectangular panels with pulse basis functions are developed in [20] and [21], in which currents are assumed to flow in the longitude direction. Currents in arbitrary directions are not easy to be supported.

The triangular discretization is commonly used in the extraction of parameters [15], [22], since arbitrarily shaped interconnects can be easily discretized with considerably small modeling errors. In addition, the RWG functions can be used to support currents in arbitrary direction. Therefore, triangles are much more preferred for complex interconnects.

C. Construction of Matrix Equations Through Unnormalized RWG Basis Functions

The method of moments (MoM) is chosen to solve the electric current density in (5). Once triangle meshes on the surface of interconnects are constructed, the unnormalized RWG functions [45] are used to discretize surface current
density \( \mathbf{J} \), which can be expressed as

\[
f_n(r) = \begin{cases} 
\frac{1}{2A_n} \rho_n^+(r), & \text{r in } T^+_n \\
\frac{1}{2A_n} \rho_n^-(r), & \text{r in } T^-_n \\
0, & \text{otherwise.}
\end{cases}
\] (7)

Compared with the traditional RWG basis function in [46], it should be noted that the edge length does not exist for (7) in our implementation. Then, the current density \( \mathbf{J} \) can be expanded using the unnormalized RWG functions

\[
\mathbf{J}(r) = \sum_{i=1}^{N_e} I_b \phi_i(r)
\] (8)

where \( N_e \) is the total number of edges. The expansion coefficient \( I_b \) denotes the current flows across the edge \( i \) from the triangle \( T^+_n \) to \( T^-_n \). In addition, the pulse functions are used to expand \( \Phi \), which is expressed as

\[
\Phi(r) = \sum_{i=1}^{N_t} \phi_i \Pi_i(r)
\] (9)

where \( N_t \) is the overall number of triangles, and \( \Pi_i(r) \) is 1 on the \( i \)th triangle and 0 outside it, respectively.

We substitute (8) and (9) into (5), and the Galerkin scheme can be expanded using the unnormalized RWG functions

\[
\mathbf{Z}_b \mathbf{I}_b = \mathbf{V}_b
\] (10)

where

\[
[Z_b]_{ij} = \frac{j\omega \mu}{4\pi} \int_{S_i} f_i(r) \int_{S_j} f_j(r') \frac{dr dr'}{|r - r'|} + Z_s \int_{S_i} f_i(r) f_j(r') dr
\]

(11)

\[
[V_b]_i = \phi_i^+ - \phi_i^-
\] (12)

where \( \mathbf{V}_b \) is a vector that collects all the unknowns in a column vector. Here, we use the unnormalized RWG functions rather than the traditional normalized functions. If the normalized RWG function is used, the coefficient \( I_b \) in (8) represents the electric current density flowing past the edge \( i \) [46]. The usage of the unnormalized RWG function can adjust the coefficient and make it directly denote the electric current. Similarly, if the unnormalized RWG functions are used to test \( \nabla \Phi \) in (5), the results directly represent the potential difference without any scaling as shown in (12).

To accurately solve (10), the MNA [35] or the mesh analysis [6] is required to enforce the charge conversation condition. In this article, a novel loop analysis is proposed to enforce it. This part will be introduced in Section III.

D. Physical Interpretation of (10) in the View of Circuit Theory

In fact, under MQS assumption, (10) can be completely interpreted through the circuit theory, which makes it easy and convenient to enforce the charge conservation condition and external excitations. To make the derivation clear, we introduce two domains: the electromagnetic domain and the circuit domain. As shown in Fig. 1, each triangle is treated as one circuit node in the circuit domain, and one edge between two triangles represents a circuit branch between two nodes. Under these intuitive interpretations, \( \mathbf{I}_b \) and \( \mathbf{V}_b \) can be regarded as branch currents and voltages in the circuit domain, respectively.

In (11), \( \mathbf{Z}_b \) can be separated into two parts: the first term \( \mathbf{L}_b \) and the second term \( \mathbf{R}_b \). The equivalent circuits for Row \( i \) of \( \mathbf{Z}_b \) are in Fig. 1. In the circuit domain, \( \mathbf{L}_b \) \( (j = 1, 2, \ldots, n, i \neq j) \) denotes the voltage-controlled voltage sources (VCVSs), and the four terms of \( \mathbf{R}_b \) \( (i \neq j) \) are treated as four current-controlled voltage sources (CCVSs) [22]. The self-term \( \mathbf{Z}_b \) \( (i = j) \) represents an impedance, which is resistive and inductive at the same time. The interpretation for the self-term is different from that in [22] and [26], since \( Z_s \) is a complex number and the second term of (11) has both resistive and inductive. Table I summarizes the relationship between quantities in the electromagnetic domain and their corresponding physical concepts or elements in the circuit domain.

Fig. 1 gives a simple example, which is a prism-shaped interconnect. Eight triangular patches are used to construct its surface, which are marked through black numbers with circles. There are 12 edges in total and the red numbers with squares are used to mark them. The equivalence in Table I is applied to this interconnect, and a planar circuit is obtained as shown in Fig. 2. Therefore, to this point, it is fully interpreted as a circuit. In Section III, we will use the graph theory to select an independent unknown set, and then solve it.

III. LOOP ANALYSIS

In Section II, (10) is derived to describe the relationship between the branch current and voltage. To solve it, additional
constraints are required in the practical applications, such as the charge conservation law and external excitations. The MNA [35], which enforces Kirchoff’s current law, was widely used in many applications [22]. For each node (triangle), summation of currents flowing into and out of one circuit node should be zero, which leads to an additional matrix equation upon branch currents. Therefore, unknowns in the MNA include branch currents and node voltages. The dimension of the final matrix equation is the summation of the number of edges and triangles. Another option is to use the mesh analysis, which can enforce Kirchoff’s voltage law and leads to a much smaller matrix equation compared with that from the MNA. However, the mesh analysis is only applicable for planar circuit, which is not true for practical complex interconnects. To overcome this issue, we propose to use the loop analysis to enforce those additional conditions for general applications.

**A. Graph Theory in the Circuit Analysis**

This section briefly introduces some essential concepts used in our analysis, and then uses them to solve (10). When all the elements of the equivalent circuit in Fig. 2 are removed, a graph of its topological connection can be obtained as shown in Fig. 3. Our following analysis is based on this graph. According to the graph theory [47], each connected graph can construct a tree, which is defined by all the nodes connecting through branches, but without including any closed loops. Once a tree for the circuit is generated, all the branches in the graph are divided into two groups: those in or not in the tree. Branches in the tree are called twigs, and the other branches are called links. It should be noted that the tree for a graph may have many possibilities. Fig. 4 shows one possible tree for the graph in Fig. 3, in which twigs are in red solid lines and links are in block dash lines.

Obviously, if there are $n$ nodes and $b$ branches for a graph with one degree of separation, the overall count of twigs should be $(n - 1)$ and the overall count of links is $(b - n + 1)$. The degree of separation is the number of completely separated parts, which denotes the number of fully separated conductors without any physically connection. Therefore, the overall counts of twigs and links are $(n - s)$ and $(b - n + s)$ for a graph with $s$ degree of separation, respectively.

In the loop analysis, loop currents rather than branch currents are required to be solved. The loops cannot be arbitrarily chosen, and the set of loops should be independent and complete. Generally, one possible choice is to generate the fundamental loop, which is a loop consisting of only one link and several connected twigs (see Fig. 5). Therefore, the overall count of fundamental loops is equal to that of links. It is found that if loop currents are defined on the fundamental loops, they are independent of each other, and a set including all the fundamental loops is complete. Therefore, we can easily construct such set through a tree for the graph. In Fig. 5, all the black solid circles consist of such set.

**B. Transfer Branch Quantities to Loop Counterparts**

To get loop currents and voltages, Kirchoff’s voltage law is applied in each fundamental loop. For each loop, the summation of branch voltages must be equal to the loop voltage, which is expressed as

$$\mathbf{AV}_b = \mathbf{V}_l$$

where $\mathbf{A}$ transfers the branch voltage $\mathbf{V}_b$ to the loop counterpart $\mathbf{V}_l$. Generally, the loop voltage is zero if there are no additional voltage sources in the corresponding loop. The
The dimension of $A$ is $l \times b$, where $b$ is the overall count of branches and $l = (b - n + s)$ is the number of links. Its entries are $-1$ or $1$, which corresponds to the direction of loops and branch voltage drops. Fig. 5 gives elements of $A$ for the corresponding loops. $A$ is a sparse matrix and can be efficiently stored through the compressed column storage (CCS) or compressed row storage (CRS) format.

The transfer matrix from loop currents to branch counterparts is the transpose of $A$, which is given by

$$A^T I_l = I_b \quad (14)$$

where $I_l$ is a column vector including all the loop currents. By substituting (13) and (14) into (10), we have

$$Z_l I_l = V_l \quad (15)$$

where $Z_l = A \Delta A^T$.

Using $A$ and $A^T$, branch quantities are replaced by their corresponding loop counterparts, and the dimension of the matrix equation significantly reduces from $(b + n)$ to $(b - n + s)$. Therefore, compared with the MNA, the loop analysis requires fewer unknowns if the additional sources are not considered. It should be noted that in the article, circuits without sheets or wires are considered.

### C. Apply Voltage Sources to the Circuit

Generally, a voltage port is defined between two terminals. In the EM domain, a terminal is the representation of a surface or the combination of several surfaces. The terminal with higher voltage is called the source and that with lower voltage is the sink. The voltage on the source or sink should be equal. If there is only one triangle on terminal as shown in Fig. 6, only one voltage source should be added between two terminals. Under normal circumstances, the port is applied through several independent voltage sources, since each terminal contains multiple triangles. As shown in Fig. 7, we, respectively, select one triangle from the source and sink, and add an independent voltage source with 1 V. For the other triangles on the source or sink, several voltage sources with 0 V are applied between them and the selected triangle. It should be noted that the tree of the circuit does not need to be modified. It is also true for twigs, because no additional circuit nodes are added. The only difference is that several additional links are generated. Therefore, several new fundamental loops should be considered. The dimension of matrix in (15) is $(b - n + s + p)$ if external voltage sources are considered, where $p$ is the overall number of exterior voltage sources. If there is a port between Triangle #1 and #2 for the model in Fig. 1, which is the simplest situation as there is only one triangle on each terminal, a new fundamental loop can be constructed as shown in Fig. 6. Therefore, an additional row should be added to $A$, and the modified matrix is shown in Fig. 6.

Once the loop analysis is carried out, and the external voltage source is attached to the circuit, the final matrix equation is expressed as

$$A \Delta A^T I_l = V_l \quad (16)$$
IV. PRECONDITIONING

When large-scale interconnects are considered, (16) have to be solved with iterative algorithms. The generalized minimal residual method (GMRES) [48] is used to solve (16) in our implementation. To speed up its convergence, a preconditioner is carefully designed and the pFFT is implemented to accelerate the matrix–vector multiplication. This section introduces the preconditioning matrix.

To reduce the overall iteration number and accelerate the convergence, an efficient preconditioner is required. In this article, the preconditioner is defined as

\[ \mathbf{P} = \mathbf{A} \mathbf{Z}^N_b \mathbf{A}^T \]  

where \( \mathbf{Z}^N_b \) is a diagonal matrix and its entries are the diagonal elements from \( \mathbf{Z}_b \) defined by (11). It should be noted that \( \mathbf{Z}^N_b \) is directly available when the pFFT algorithm is used as the near block interaction is calculated. \( \mathbf{A} \) and \( \mathbf{A}^T \) are the transfer matrices and they are all sparse matrices. Therefore, \( \mathbf{P} \) is a symmetric matrix. The left preconditioning technique is applied to (15), and (18) can be obtained as

\[ \mathbf{P}^{-1} \mathbf{Z}_l \mathbf{I}_l = \mathbf{P}^{-1} \mathbf{V}_l. \]  

It is obvious that the inverse of \( \mathbf{P} \) should be effectively calculated when the GMRES is used to solve (16). Fortunately, since \( \mathbf{A} \) and \( \mathbf{A}^T \) are sparse matrices and \( \mathbf{Z}^N_b \) is a diagonal matrix, \( \mathbf{P} \) is a sparse matrix. A direct factorization algorithm can be used to efficiently calculate the inverse of \( \mathbf{P} \), such as the PARDISO solver in MKL [49].

Three matrix–vector products are required to be calculated for (18). It should be noted that \( \mathbf{I}_l = \mathbf{Z}_l \mathbf{I}_l \) is very time-consuming, since \( \mathbf{Z}_l \) is a full matrix. However, it is easy to calculate \( \mathbf{P}^{-1} \mathbf{V}_l \) and \( \mathbf{P}^{-1} \mathbf{I}_l \) because \( \mathbf{P}^{-1} \) can be effectively calculated. \( \mathbf{Z}_b \) can be separated into two parts mentioned in Section II-B. It can be expressed as

\[ \mathbf{Z}_b = \mathbf{R}_b + \mathbf{L}_b \]  

where \( \mathbf{R}_b \) is the second term of (11), which is a sparse matrix, and \( \mathbf{L}_b \) is the first term, which is a full matrix. Therefore, we only need to accelerate \( \mathbf{A} \mathbf{L}_b \mathbf{A}^T \mathbf{I}_l \). In this article, the pFFT algorithm is applied to accelerate the calculation of it, which is introduced in Appendix B.

V. NUMERICAL RESULTS AND DISCUSSION

In this section, four numerical examples are computed using the proposed formulation and the industrial solver Ansys Q3D. Ansys Q3D uses the same formulation as (3) and the first term of it is set to zero. Therefore, the solution is more efficient but can lead to the inductance independent of frequency. This approximation is reasonable when the highly lossy conductor is considered at high frequency. The resistance and inductance are calculated, and the results are compared with those from Ansys Q3D. In addition, the effectiveness of the pFFT algorithm and the proposed preconditioner is discussed and verified. Our in-house solver is developed with C++ without any parallel computations, and all the simulations are carried out on the workstation with a 3.2-GHz CPU and 1-TB memory.

A. One Rectangular Interconnect

The first structure is a rectangular copper interconnect with the size of 5 \( \mu \text{m} \times 7.5 \ \mu \text{m} \times 200 \ \mu \text{m} \) as shown in Fig. 8. The conductivity of it is 5.7 \( \times 10^7 \) S/m. A voltage source is added between two ends of this interconnect, and the surface with red arrows is the source, which has higher potential compared with that at the far end of the interconnect and indicates that currents flow into the interconnect. The corresponding surface with the blue arrow is the sink and has the lower potential compared with that on the source and represents that currents flow out of the interconnect. In Section II-A, it is mentioned that the surface impedance operation should be used in a limited frequency range, and it works well when the skin depth is less than 1/3 thickness of interconnects in general.
Therefore, its wideband properties between 10 and 150 GHz were studied, where the surface impedance operator can well represent the relationship between the surface current density and the tangential electric field. The average length of edges was kept as 1/1000 wavelength, which means that the mesh size reduces with the increase in frequency. Fig. 9 shows the resistance and inductance calculated by Ansys Q3D and the proposed formulation. For the resistance, two results are in good agreement in the whole frequency region. It can be noted that the inductance does not vary with frequency for Ansys Q3D.

The effectiveness of the pFFT algorithm is discussed through the runtime and memory consumption as shown in Fig. 10. We discretized the interconnect using the mesh with different sizes and recorded the runtime and memory consumption, in which the frequency increased with the decrease in the mesh sizes and the average length of edges was kept as around 1/1000 wavelength. The runtime and memory increase as the number of loops increases. Curves versus the runtime and memory consumption approximately match $O(N \log N)$ and $O(N)$.

In addition, the convergence property in the GMRES solver is very important for efficient parameter extraction. Therefore, we investigated the number of iterations with and without the preconditioner $P$ in (17) for the convergent tolerance of $10^{-3}$. As shown in Fig. 11, the top subfigure shows the number of iterations when the frequency is set to 100 GHz. As the dimension of the system matrix increases, the number of iterations also increases with or without the preconditioner. However, the preconditioner can approximately reduce the number of iterations by one order when the number of unknowns is large enough. In the bottom subfigure of Fig. 11, we used 428 triangles to discretize the interconnect, and the number of iterations with different frequencies was recorded. Similarly, the proposed preconditioner can significantly reduce the overall iteration number, and hence accelerate the convergence.

In Fig. 8, the distribution of electric potential and the magnitude of surface current are illustrated. The branch current can be calculated by (14) since we have obtained the loop current. Similarly, the branch voltages are obtained through (13). In our simulation, the electric potential on the surfaces of sinks is set as zero, and then the electric potential on each triangular panel can be calculated through the branch voltages.

**B. Bonding Wire Array**

The bonding wire array consisting of 52 copper interconnects with the conductivity of $5.7 \times 10^7$ S/m is considered here. The dimension of this structure is $1.2 \text{ mm} \times 1.2 \text{ mm} \times 0.15 \text{ mm}$, and the thickness of each interconnect is $10 \mu\text{m}$. The ports are defined on the ends of two adjacent bonding
Fig. 15. Number of iterations for GMRES with and without the preconditioner versus the frequency and meshes.

Fig. 16. Bottom view and top view of a real-life circuit with several vias and the excitation configuration.

Fig. 17. Self- and mutual resistance and inductance obtained from Ansys Q3D and the proposed formulation.

To demonstrate the accuracy, we swept the frequency from 0.5 to 30 GHz and calculated the resistance and inductance, in which 13,041 loops are found to construct the matrix equations. In Fig. 13, the results calculated by the proposed formulation and Ansys Q3D are compared with each other. For both the self-inductance and mutual inductance, the two solvers show excellent agreement with each other for all the sampling frequencies, and the relative error is less than 2%. The self-resistance also agrees well for the two solvers, but a large difference occurs for mutual resistance, which is about 25%. In fact, the mutual resistance contributes little to the loop resistance due to their small values. The resource consumption including the runtime and memory is illustrated as shown in Fig. 14. As the number of loops increases, the runtime and memory consumption also approximately match $O(N \log N)$ and $O(N)$.

To demonstrate the effectiveness of the preconditioner, the number of iterations as the number of loops and frequency is recorded and illustrated in Fig. 15. As the number of loops increases, the number of iterations also increases with and without the preconditioner. However, the number of iterations increases very slowly when the preconditioner is used. For example, there are nine iterations for 3,470 loops and 13 iterations for 967,909 loops. In general, frequency has very little effect on the number of iterations. The overall number of iterations slightly decreases without the preconditioner and slightly increases with it when the frequency increases. In addition, as shown in Fig. 12, the distribution of surface current and electric potential are illustrated when Port#2 is excited by a voltage source. The scenario of the accumulation of current on the edges can be observed.

C. Interconnects in a Real-Life Circuit

In this example, a real-life circuit with complex interconnects is considered and two ports are defined. The material
of it is copper with the conductivity of $5.7 \times 10^7 \text{ S/m}$. The sources are defined on the facets at the end of bonding wires extending from the circuit, and Source#1 consists of 1st, 4th, 5th, 7th, and 10th facets, while Source#2 is composed by others. The sinks are set on the ubumps at the bottom of the circuit as shown in Fig. 16. We excited two ports in turn and calculated the self- and mutual resistance and inductance in the frequency range of 0.2–10 GHz. In all, 77,352 triangular facets are used to discretize the surface, and 39,220 loops are required to construct the matrix equations. Fig. 17 shows the results obtained from the proposed formulation and Ansys Q3D. For the self- and mutual resistance and inductance, the results calculated by two solvers show excellent agreement with each other.

Fig. 18 shows the runtime and memory consumption when different meshes were used and the working frequency was fixed at 10 GHz. It can be found that the runtime approximately matches $O(N \log N)$, but it is slightly larger than $O(N \log N)$ as the unknowns increase. The main reason is that the runtime may match the complexity of $O(N \log N)$ for each iteration in the GMRES, but the number of iterations increases with the number of unknowns, which leads to a slightly larger runtime. As for memory consumption, further optimization for our in-house solver is still required to be carried out to match $O(N)$ well for large-scale problems.

Similar to the previous two examples, the effectiveness of the preconditioner is investigated by the number of iterations, and we set the convergent tolerance as $10^{-3}$. The top subfigure of Fig. 19 focuses on the number of iterations over meshes when the frequency is fixed at 10 GHz. The bottom subfigure relates the number of iterations to the frequency. There are 39,220 loops to construct the matrix. It can be found that the preconditioner significantly accelerates the convergence of GMRES. Especially, the number of iterations increases very slowly when the number of unknowns increases if the preconditioner is applied. There are 38 iterations with preconditioner and 123 iterations without it for 26,256 unknowns. However, the scenario with the preconditioner requires 48 iterations for 1,938,754 unknowns, while 310 iterations are required for the same unknowns without it. In addition, as shown in Fig. 20, we calculated the magnitude of surface current and the distribution of electric potential when a voltage source is applied on Port#2. It can be found that the current accumulates on the slender bonding wires. Therefore, the electric potential goes down very fast on them.

**D. Large-Scale PDN Modeling**

In this example, the PDN is considered to verify the scalability of the proposed formulation. As shown in Fig. 16, the cross rectangular interconnects with four ubumps on the top and one pad on the bottom are considered, and the structure has a dimension of $16 \mu m \times 16 \mu m \times 8.2 \mu m$. The interconnects of different layers are connected through a number of vias and the pad is coupled to the interconnects through a slender via. All these parts are copper with the conductivity of $5.7 \times 10^7 \text{ S/m}$.
TABLE II
SIMULATION CONFIGURATION, RESOURCE CONSUMPTION, LOOP RESISTANCE, AND INDUCTANCE OBTAINED FROM THE PROPOSED FORMULATION AND ANSYS Q3D

|   | $f = 30$ GHz, tol $= 10^{-3}$ |   |   |   |
|---|-------------------------------|---|---|---|
|   | 1×1 | 2×2 | 4×4 | 6×6 |
| Num. triangles | 62,590 | 261,928 | 1,051,950 | 1,933,368 |
| Num. Loops | 33,047 | 138,735 | 558,084 | 1,025,824 |
| Num. iterations with preconditioner | 21 | 31 | 44 | 54 |
| Num. iterations w/o preconditioner | 230 | 423 | 804 | 1,811 |
| Runtime (s) | 485 | 3,566 | 18,401 | 47,220 |
| Memory (Mb) | 1,307 | 9,948 | 104,186 | 225,494 |
| $R_o$-proposed (ohm) | 0.68 | 0.17 | 0.043 | 0.020 |
| $L_o$-proposed (nH) | 0.083 | 0.020 | 0.0050 | 0.0022 |
| $R_o$-Ansys Q3D (ohm) | 0.70 | 0.18 | 0.045 | 0.021 |
| $L_o$-Ansys Q3D (nH) | 0.083 | 0.021 | 0.0052 | 0.0022 |

The structure in Fig. 21 is considered as a unit and we extend it to 2×2, 4×4, and 6×6 arrays. The sources are defined on the bumps on the two contactless parts and the sinks are set on the bottom of pads as shown in Fig. 22. The resistance and inductance were calculated at 30 GHz. The simulation configuration, results, and resource consumption are presented in Table II.

The first two rows record the overall number of triangles and loops used to construct the PDN. Next, the runtime, memory, and number of iterations with and without the preconditioner are presented when the convergent tolerance is set to $10^{-3}$, in which we summed the number of iterations for two solutions to Port#1 and Port#2. The preconditioner still works very well for this example, and it significantly reduces the number of iterations by one order. In addition, the loop resistance and inductance are calculated by the proposed formulation and Ansys Q3D, which are defined as $R_o = R_{11} - 2R_{12} + R_{22}$ and $L_o = L_{11} - 2L_{12} + L_{22}$. For the loop inductance, the proposed formulation shows excellent agreement with that from Ansys Q3D, and the relative error is less than 4% for the four cases. The loop resistance has a slightly larger error, still only 7%. Fig. 23 gives the illustration of the PDNs with different dimensions and the distribution of electric potential is shown, in which 1×1 and 2×2 arrays are excited on Port#1 and 4×4 and 6×6 arrays are excited on Port #2. There is little change in electric potential for the upper part of PDNs, and the electric potential goes down very fast on the vias connected to the pads.

VI. CONCLUSION

In this article, an MQS-SIE formulation with the loop analysis is proposed to model interconnects in packages at high frequencies. The triangle discretization is used to support the surface current flowing in any direction. The graph theory in circuit analysis is introduced to construct independent and complete loop equations. By transferring the branch quantities to loop quantities, the dimension of the system matrix can reduce by about 80%. In addition, the pFFT algorithm is successfully carried out for the proposed formulation, and an efficient preconditioner is developed to speed up the convergence in GMRES. The numerical examples verify the scalability and effectiveness of the proposed formulation, and accurate results can be obtained compared with those from the industrial solver Ansys Q3D.

However, the uniform grid option required by the traditional pFFT algorithm will cause the waste of computational resource, especially for the multiscale structures. Therefore, optimization of the pFFT algorithm, like the hierarchical algorithm, will be our future work.
APPENDIX A
COMPLEXITY OF LOOP ANALYSIS

The complexity of constructing the tree for a graph is analyzed in this appendix. The array is commonly used to describe a tree, in which the unique parents for each node are stored. Therefore, the constructing of a tree is equal to the process to find parents of each node. In the implementation of MoM, the generation of RWG functions, which are defined on the edges shared by two triangles, is necessary. Therefore, the connection between the edges and triangles has been known. Based on this point, the flow to construct a tree can be shown as follows.

1) Customize a triangle as the root node, which is the first layer of this tree.
2) Find three nodes (triangles) connecting to the root, and set the root as the parent of these three nodes. The second layer is generated by the three nodes.
3) Let these three nodes as the root in turn.
4) For each root, find the connecting three nodes. For these three nodes, assume that there are \( n_1 (\leq 3) \) nodes without parents and set the corresponding root as their parent.
5) Collect nodes without parents in Step #4, and there are \( N = \sum n_i \) nodes in the next layer.
6) Let these \( N \) nodes as the root in turn and repeat the operation in Step#4–#6 until there are parents for all the nodes except the initial one.

Through the steps above, the tree can be constructed layer by layer. It should be noted that the operation to find the three connecting nodes in Step#2 and Step#4 is very easy because the connection between edges and triangles is known. In the flow above, there are \( 3N_l \) operations in total, where \( N_l \) is the number of triangles. Therefore, the time complexity should be linear, which is \( O(3N_l) \).

To find the fundamental loops, it is equivalent to find the shortest path between two nodes of one link. The path can be constructed through finding the nearest common root of these two nodes. By considering the worst situation, if two nodes are both at the bottom of the tree and their nearest common root is at the top, the number of operations to find the root should be \( 2 \times N_{la} \), where \( N_{la} \) is the number of layers for this tree. Therefore, the complexity of finding the fundamental loops should be less than \( O(2N_{la}N_l) \), and \( N_l \) is the number of loops. In fact, \( N_{la} \) is very small because the number of nodes in each layer increases exponentially.

APPENDIX B
PFFT ALGORITHM

For a Toeplitz matrix, the matrix–vector multiplication can be efficiently computed using the pFFT algorithm, which implies that the time complexity can be reduced from \( O(N^2) \) to \( O(N\log N) \), and the memory cost is reduced to \( O(N) \). By assuming uniformly distributed grids in the 3-D space as shown in Fig. 24, \( G_{op}(r, r') \) is a three-level Toeplitz matrix because Green’s function is shift-invariant in the 3-D space. Therefore, the FFT can be used to efficiently accelerate the matrix–vector multiplication.

In the pFFT algorithm, the whole computation domain can be categorized into two parts: near- and far-field regions. The pFFT algorithm consists of four steps as follows.

1) Construction of the project matrix from a triangle pair to its nearby grids.
2) Construction the convolution matrix to efficiently calculate the potential between grid points through the FFT algorithm.
3) Construction of the interpolation matrix from the nearby grids to the desired triangle.
4) For near-field regions, the entries are directly calculated.

Through the above four steps, the matrix–vector multiplication \( A_{lab}A_{lab}^T \), can be calculated, and therefore, the time complexity can be reduced to \( O(N\log N) \).

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