Design of a New Multiplexer Structure Based on a New Fault-Tolerant Majority Gate in Quantum-Dot Cellular Automata

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Abstract

Quantum-dot Cellular Automata (QCA) technology is believed to be a good alternative to CMOS technology. This nanoscale technology can provide a platform for design and implementation of high performance and power efficient logic circuits. However, the fabrication of QCA circuits is susceptible to faults appearing in this form of missing cells, additional cells, rotated cells, and displaced cells. Over the years, several solutions have been proposed to address these problems. This paper presents a new solution for improving the fault tolerance of three input majority gate. The proposed majority gate is then used to design 2-1 multiplexer and 4-1 multiplexer. The proposed designs are implemented in QCA Designer. Simulation results demonstrate significant improvements in terms of fault tolerance and area requirement.

1. Introduction

Today, metal-oxide superconductor technology has extensive application in the production of digital circuits and chips. This technology, like many others, involves making a tradeoff between speed and power consumption. New technologies such as carbon nanotube field-effect transistor (CNTFET) and quantum dot cellular automata (QCA) have been able to facilitate the fabrication of faster, more compact, and more energy-efficient circuits with parallel processing capabilities[1,2].

QCA is a nanotechnology computing architecture originally developed by Dr. Craig Lent and his colleagues in 1993[1]. In this architecture, some concepts of quantum mechanics such as tunneling are utilized in the fabrication of potential barriers for cellular automata[3,4]. The core idea of QCA originates from the concept of artificial semiconductor atoms, which allows for the implementation of digital components in the nanoscale[13,14].

There are however several challenges in implementing QCA technology, which include fabrication faults appearing as missing cells, additional cells, cell displacements, and cell rotations. Missing cell refers to the absence of one or more cells from the grid. Cell displacement refers to the situation where one or more cells are not exactly in their expected position. Rotation cell refers to when a cell rotates in its place [5-12,16,17,22,29].

This article is mainly focused on the challenge of addressing missing cells. In the remainder of this article, the principles of QCA are introduced in Section 2. The existing solutions for dealing with missing cells are reviewed in Section 3. The proposed design for a fault tolerant three input majority gate is presented in Section 4. In Section 5, two 2-1 and 4-1 multiplexers developed based on the proposed majority gate are introduced. And finally, discussions and conclusions are presented in Section 6.

2. Principles Of Qca

Principles of QCA were first introduced in 1993[1]. To have a system of information processing based on the position of electrons, there must be a space for holding electrons in place. In the QCA literature, this
space is called a cell. Each cell is a Nano-sized square space with four holes called quantum dots in its four corners which hold two electrons. The cells allow free electrons to tunnel between neighboring quantum dots (Figure 1)[15].

Since the two electrons within each cell repel each other until reaching the lowest energy state, as shown in Figure 2, there could only be two stable states for each cell[15].

In the base state when there is no external force, the Coulomb repulsion of the electrons pushes them into opposite corners of the QCA cell, where they will be as far as possible from each other. Hence, there are only two possible states for a QCA cell. As shown in Figure 2, these two states are known as $P = +1$ or $P = -1$ and represent the binary values of “1” and “0” respectively [1,16-19].

The basic building blocks of QCA circuits are wires, majority gate (vector), and inverter. There are two types of wire in QCA circuits: 90° and 45°. The 45° wire is a wire of base cells that are rotated at 45° (Figure 3)[16].

In Figure 4 shown the typical layouts of majority gate and inverter[15].

In QCA circuits, the movement of electrons inside the cells is controlled by the Clock. This component makes sure that the data is flowing in the right direction and also synchronizes the combination of data incoming from different branches. In other words, in conjunctions where multiple inputs should be combined to produce an output, the clock holds the data that arrive earlier in place until all data necessary for the combination arrive at the conjunction. Each clock consists of four phases (Figure 5)[15-17,20,21,30]:

1. Switch: the cell becomes depolarized and gradually transforms according to the state of the input or preceding cell.
2. Hold: the cell maintains a high energy level and remains active to serve as an input for the subsequent cell.
3. Release: with a gradual decrease in the energy level, the cell loses its effect on its adjacent cells.
4. Relax: the cell loses all of its energy and reaches a stable state.

QCA circuit fabrication faults

The faults that typically occur in the fabrication of QCA circuits include [5-12,16,17,22]:

1. Missing cell (Figure 6-a)
2. Additional cell (Figure 6-b)
3. Cell displacement (Figure 6-c)
4. Rotation cell (Figure 6-d).

3. Related Works
In this section, we briefly review the existing solutions for improving the fault tolerance of majority gate circuits. The designs previously proposed for this purpose are displayed in Figure 7. These designs have used different methods to improve fault tolerance. In most of these solutions, fault tolerance is improved by adding additional cells to strategic positions within the majority gate. Other solutions have repositioned inputs or output or have used cell rotation to improve fault tolerance.

4. Proposed Majority Gate Design

This section introduces the proposed majority gate design developed for improved fault tolerance. After the introduction, the simulation results are presented and the design outputs in different states are examined. The proposed majority gate design is shown in Figure 8.

The proposed gate consists of 11 cells and requires an area of 0.0096 $\mu m^2$. In this gate, three cells called A, B and C are inputs, the cell called OUT is output, and the remaining cells are intermediate cells. The proposed structure was simulated with the parameters listed in Table 1 using the software QCA Designer.

Table 1: Simulation parameters used in QCA Designer

| Parameter                  | Value               |
|----------------------------|---------------------|
| Cell Size(nm)              | 18 * 18             |
| Cell Separation(nm)        | 2                   |
| Number Of Samples          | 12800               |
| Convergence Tolerance      | 0.001000            |
| Radius of effect(nm)       | 65.000000           |
| Relative Permittivity      | 12.900000           |
| Clock High                 | 9.8000000e-022      |
| Clock Low                  | 3.8000000e-023      |
| Clock Shift                | 0.0000000e+000      |
| Clock Amplitude Factor     | 2.000000            |
| Layer Separation           | 11.500000           |
| Maximum Iterations Per Sample | 100                |

Figure 9 presents the simulation results of the proposed three input majority gate. The AND and OR gates developed based on the proposed structure are shown in Figures 10-a and 10-b. The results of the simulation of these gates are presented in Figure 11.
The proposed design has 100% tolerance to the fault of a single missing cell (Table 2-a) and 71.43% tolerance to the rotation of one cell (Table 2-b). The tolerance of the design to cell displacement is described in Table 3. Also, addition a cell fault to the grid will make no change in the output of the proposed majority gate. Tables 4 and 5 demonstrate the physical fault tolerance of the design for the state shown in Figure 12.

**Table 2: Simulation results of the proposed structure for the faults of (a) a single missing cell and (b) a single rotation cell**

*a*

| Removed Cell | Output |
|--------------|--------|
| 1            | MV3    |
| 2            | MV3    |
| 3            | MV3    |
| 4            | MV3    |
| 5            | MV3    |
| 6            | MV3    |
| 7            | MV3    |

*b*

| Rotation Cell | Output |
|---------------|--------|
| 1             | B      |
| 2             | A      |
| 3             | MV3    |
| 4             | MV3    |
| 5             | MV3    |
| 6             | MV3    |
| 7             | MV3    |

**Table 3: Effect of a cell displacement on the output of the proposed majority gate**
Rightward | Leftward | Upward | Downward | Cell |
---|---|---|---|---|
<3 | <3 | <18 | | A |
<3 | <3 | <18 | | B |
<7 | <4 | <4 | | C |
<8 OR >15 | | | | 1 |
<8 OR >15 | | | | 2 |
<7 OR >17 | | | | 6 |
<7 OR >17 | | | | 7 |
<2 | <4 OR (>18 AND <31) | <4 OR (>18 AND <31) | | OUT |

Table 4: Energy calculations for the output cell of Figure 12-b

| Energy of electron x (Joules) | Energy of electron y (Joules) |
|------------------------------|------------------------------|
| $U_1 = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20}$ | $U_1 = \frac{23.04 \times 10^{-29}}{55.17 \times 10^{-9}} = 0.42 \times 10^{-20}$ |
| $U_2 = \frac{23.04 \times 10^{-29}}{40.05 \times 10^{-9}} = 0.58 \times 10^{-20}$ | $U_2 = \frac{23.04 \times 10^{-29}}{44.72 \times 10^{-9}} = 0.52 \times 10^{-20}$ |
| $U_3 = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} = 1.15 \times 10^{-20}$ | $U_3 = \frac{23.04 \times 10^{-29}}{22 \times 10^{-9}} = 1.05 \times 10^{-20}$ |
| $U_4 = \frac{23.04 \times 10^{-29}}{43.86 \times 10^{-9}} = 0.53 \times 10^{-20}$ | $U_4 = \frac{23.04 \times 10^{-29}}{43.86 \times 10^{-9}} = 0.53 \times 10^{-20}$ |
| $U_5 = \frac{23.04 \times 10^{-29}}{29.73 \times 10^{-9}} = 0.77 \times 10^{-20}$ | $U_5 = \frac{23.04 \times 10^{-29}}{40.05 \times 10^{-9}} = 0.58 \times 10^{-20}$ |
| $U_6 = \frac{23.04 \times 10^{-29}}{55.17 \times 10^{-9}} = 0.42 \times 10^{-20}$ | $U_6 = \frac{23.04 \times 10^{-29}}{61.35 \times 10^{-9}} = 0.38 \times 10^{-20}$ |
| $U_7 = \frac{23.04 \times 10^{-29}}{10.19 \times 10^{-9}} = 2.26 \times 10^{-20}$ | $U_7 = \frac{23.04 \times 10^{-29}}{35.23 \times 10^{-9}} = 0.65 \times 10^{-20}$ |
| $U_8 = \frac{23.04 \times 10^{-29}}{22.36 \times 10^{-9}} = 1.03 \times 10^{-20}$ | $U_8 = \frac{23.04 \times 10^{-29}}{39.05 \times 10^{-9}} = 0.59 \times 10^{-20}$ |
| $U_{Tx} = 7.55 \times 10^{-20}$ | $U_{Tx} = 5.77 \times 10^{-20}$ |

$U_T = 13.32 \times 10^{-20}$

Table 5: Energy calculations for the output cell of Figure 12-c
In Table 6, the proposed majority gate is compared with the existing designs in terms of the number of cells, area requirement, and fault tolerance. As Table 5 demonstrates, the proposed design enjoys a better performance than the existing designs.

Table 6: Comparison of the proposed majority gate with the existing designs

| Single-cell fault tolerance | Area requirement ($\mu m^2$) | Number of cells | Gate |
|-----------------------------|-------------------------------|-----------------|------|
| 66.70                       | 0.0096                        | 13              | Figure 6-a[23] |
| 81.25                       | 0.0139                        | 20              | Figure 6-b[11] |
| 82.25                       | 0.0096                        | 21              | Figure 6-c[24] |
| 60.00                       | 0.0135                        | 19              | Figure 6-d[10] |
| 100                         | 0.0076                        | 16              | Figure 6-e[17] |
| 64.29                       | 0.0210                        | 32              | Figure 6-f[25] |
| 80.95                       | 0.0096                        | 25              | Figure 6-g[21] |
| 97.44                       | 0.0388                        | 43              | Figure 6-h[26] |
| 100                         | 0.0144                        | 27              | Figure 6-i[16] |
| 100                         | 0.0096                        | 11              | Proposed design |

\[ U_T = 10.16 \times 10^{-20} \]
5. New Multiplexer Based On The Proposed Majority Gate

This section first reviews the existing multiplexer designs, then presents a 2-1 multiplexer and a 4-1 multiplexer designed based on the proposed majority gate. At the end of the section, the proposed multiplexer compared with the existing designs. The existing designs for 2-1 multiplexers are shown in Figure 12.

Figure 13 presents the 2-1 multiplexer designed based on the proposed majority gate. The output function of this multiplexer is shown in equation 1:

Eq. (1) : \( F=S'A + SB \)

The proposed 2-1 multiplexer consists of 41 cells and requires an area of 0.066 \( \mu m^2 \). This multiplexer has 95.24% tolerance to the fault of a single missing cell. The simulation results obtained for this multiplexer are presented in Figure 14.

The 4-1 multiplexer designed based on the proposed majority gate is shown in Figure 15. This multiplexer has 85.71% tolerance to the fault of a single missing cell.

In Table 7, the proposed 2-1 multiplexer is compared with the existing designs. As the simulation results presented in Table 7 demonstrate, the proposed 2-1 multiplexer exhibits significant superiorly over the existing designs in term of the number of cells, area requirement, and fault tolerance.

| Fault tolerance | Area requirement (\( \mu m^2 \)) | Number of cells | Multiplexer design |
|-----------------|----------------------------------|-----------------|-------------------|
| 48.14           | 0.039204                         | 45              | Figure 14-a[27]   |
| 33.33           | 0.035244                         | 45              | Figure 14-b[27]   |
| 64.45           | 0.051084                         | 65              | Figure 14-c[10]   |
| 94.02           | 0.158404                         | 137             | Figure 14-d[26]   |
| 86.96           | 0.078684                         | 98              | Figure 14-e[16]   |
| 95.24           | 0.063516                         | 41              | Proposed design   |

6. Conclusion

In this article, we first provided a brief introduction to QCA technology and challenges in the fabrication of QCA circuits and discussed the existing solutions for resolving these challenges. We then presented a new solution for improving the tolerance of three input majority gate to the faults of single missing cell, single additional cell, single cell rotation, and single cell displacement. The proposed idea was then used to design new 2-1 multiplexer and 4-1 multiplexer. The simulation results demonstrated the significantly
improved fault tolerance of the proposed solution for three input majority gate compared to the existing designs. The multiplexer designed based the proposed majority gate also showed significant superiority over the existing designs in terms of fault tolerance and area requirement. In future works, the proposed majority gate can be incorporated into the design of flip-flops, decoders, hybrid circuits, and sequential circuits. The proposed multiplexer can be used in the design of memory cells for RAMs.

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Figures

![Figure 1](image_url)

A single QCA cell
Figure 2

Possible states of a QCA cell

Figure 3

a) 90° QCA wire b) 45° QCA wire
Figure 4

a) three input majority gate
b) two types of inverter

Figure 5
Figure 6

Typical QCA circuit fabrication faults – a) missing cell b) additional cell c) cell displacement d) cell rotation
Figure 7

Existing solutions for improving fault tolerance in majority gates. a[23], b[11], c[24], d[10], e[17], f[25], g[21], h[26], i[16]
Figure 8

Proposed majority gate design

|   |   |   |   |
|---|---|---|---|
| A | B | C | OUT |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 |

max: 9.80e-022  
CLOCK 0  
min: 3.80e-023

Figure 9
simulation results of the proposed majority gate

Figure 10

Proposed structures for (a) AND gate and (b) OR gate
Figure 11

Simulation results of the proposed AND gate (a) and OR gate (b)
Figure 12

a) Radius of effect in the proposed design
b,c) Possible states of the QCA cells within the radius of effect
Figure 13

Existing 2-1 multiplexer designs. a[27], b[27], c[10], d[26], e[16]
Figure 14

2-1 multiplexer designed based on the proposed majority gate
Figure 15

Simulation results of the 2-1 multiplexer designed based on the proposed majority gate
Figure 16

4-1 multiplexer designed based on the proposed majority gate