Al-Oxynitride interfacial layer investigations for Pr$_x$O$_y$ on SiC and Si

K Henkel, K Karavaev, M Torche, C Schwiertz, Y Burkov and D Schmeisser

Brandenburgische Technische Universität Cottbus, Angewandte Physik-Sensorik, K.-Wachsmann-Allee 17, 03046 Cottbus, Germany

henkel@tu-cottbus.de

Abstract. We investigate the dielectric properties of Praseodymium based oxides Pr$_x$O$_y$ by preparing MIS (metal insulator semiconductor) structures consisting of Pr$_x$O$_y$ as a high-k insulating layer and silicon (Si) or silicon carbide (SiC) as semiconductor substrates. The use of a buffer layer between Pr$_x$O$_y$ and the semiconductor is necessary as we found deleterious reactions between these materials such as silicate and graphite formation. Possessing a higher permittivity value ($\varepsilon_r$) than silicon dioxide (SiO$_2$) and good lattice matching in conjunction with similar thermal expansion coefficient to SiC, we focus on aluminum oxynitride (AlON) as a suitable buffer layer for this high-k/wide-bandgap system. In our spectroscopic investigations we found a decrease or indeed prevention of silicon diffusion into the oxide and an increased Pr$_x$O$_y$ fraction after deposition. In electrical characterizations of Pr$_x$O$_y$/AlON stacks we found considerable improvements in the leakage current by several orders on both substrates, especially on silicon where we obtain values down to $10^{-7}$ A/cm$^2$ at a CET (capacitance equivalent thickness) of 4nm. We observed interface state densities in the range of $5 \times 10^{11}$-$1 \times 10^{12}$/eVcm$^2$ and $1 \times 10^{12}$/eVcm$^2$ on Si and SiC, respectively.

1. Introduction

Pr$_x$O$_y$ is one of the candidates for both realizing the further shrinkage of the equivalent oxide thickness (EOT) in microelectronic devices and for electric field scaling at the interface between semiconductor and insulator in high power applications [1]. However, the chemical reactivity of the Pr$_x$O$_y$/SiC and Pr$_x$O$_y$/Si interfaces causes a deleterious interaction yielding graphite and silicate formation after direct deposition of Pr$_x$O$_y$ onto SiC and Si, respectively [2], [3]. This leads to high leakage currents [4] as well as causing a limitation in the reduction of the EOT due to an interfacial layer with small permittivity values. Furthermore, high-k materials tend to cause decreased values of the band gap by increasing their k-values [5], leading to lower band offsets [6]. The reported values for permittivity and band gap of Pr$_x$O$_y$ are quite different and range from 15-30 [7], [8] and 2-5.5eV [8], [9], respectively. So a buffer layer between semiconductor and insulator is needed to hinder charge injection from the semiconductor into the insulator on the one hand and on the other hand, it should prevent diffusions from the semiconductor into the insulator resulting in unintentional interfacial layer formation. Our approach is to use a buffer layer with a higher permittivity value than that of SiO$_2$, because the lower permittivity value of the buffer layer decreases the total permittivity value of the stack. We focus on a hetero-oxide structure consisting of aluminum nitride (AlN) next to SiC or Si and Pr$_x$O$_y$ on the top. The bandgap of AlN ($E_g=6.2$eV[10]) and its permittivity value ($\varepsilon_r \sim 9$ [11]) as well as small lattice mismatch ($\Delta a/a \sim 1\%$) and nearly equal thermal expansion coefficients

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(AIN: 4.15x10^7/K, SiC: 4.2x10^9/K) to hexagonal SiC [12, [13] indicate that this material might combine a good interface quality with a high-k property. In previous studies we reported on spectroscopic investigations of Al-oxynitride, and we recognized a stable AlON/3C-SiC interface even for annealing steps up to 900°C [14]. In this contribution we combine spectroscopic (XPS: X-ray photoelectron spectroscopy) and electrical investigations (CV: Capacitance-Voltage, IV: Current-Voltage, GV(ω): AC-Conductance) of Pr_3O_y samples with different thickness, and will further discuss whether the AlON buffer layer can improve the electrical characteristics.

2. Experimental

(001) p-type and n-type silicon wafers having a doping concentration in the range of 10^{15}-10^{19} cm^{-3} as well as epi-layers of n-type 4H-SiC(0001) (1.1x10^{19}cm^{-3}) on highly doped n-type 4H-SiC(0001) substrates (8nmQcm, 8° off, Fa. Cree, provided by SiCED GmbH Erlangen) were used in these experiments. The wafers were cleaned by a HF (hydrofluoric acid) dip (5% HF, 10 seconds). Pr_3O_y layers were prepared by electron beam evaporation in ultra high vacuum (UHV) from Pr_3O_y powder [15]. AlON was prepared by sputtering an aluminum source with nitrogen ions and oxygen atoms, from residual oxygen in the vacuum sputtering unit [14]. Annealing was performed ex situ in an oven (Lora Raetz) at temperatures around 800°C in flowing nitrogen.

XPS measurements were carried out using Mg Kα radiation and an EA125 electron analyzer made by Omicron NanoTechnology GmbH. Thickness was either estimated by the attenuation of Si2p core level [16] or determined by profilometry (talystep Rank Taylor Hobson). For electrical characterization MIS capacitors were prepared using gate electrode stacks of titanium (Ti) on top of the oxide followed by aluminum (Al) with diameter 400-800um. Here the Ti acts as a diffusion barrier against Al diffusion into the oxide [15]. Al layers were thermally evaporated while Ti layer was deposited by sublimation. CV and GV(ω) measurements have been carried out at room temperature by an Agilent 4284 LCR meter. IV characteristics have been recorded using Agilent E3649A, HP34401, PREMA4001 and/or Keithley487 respectively. Permittivity and CET values were deduced from the oxide capacitance of the CV plot in accumulation. Densities of interface states (D_i) were determined by AC conductance maxima [17].

3. Results and discussion

3.1. XPS investigations of Pr_3O_y thickness series with and without AlON

First we report on XPS investigations of Pr_3O_y/Si and Pr_3O_y/1nmAlON/Si stacks with different oxide thickness. The spectra were recorded for as-deposited samples and for samples which have been annealed in nitrogen at 800°C. The O1s core level spectra are summarized in figures 1a and 1b.

![Figure 1](image-url)

Figure 1: XPS measurements of Pr_3O_y/Si and Pr_3O_y/1nmAlON/Si stacks with different Pr_3O_y thickness for as deposited and annealed (800°C, N_2) samples: a) O1s of Pr_3O_y/Si, b) O1s of Pr_3O_y/1nmAlON/Si, and c) Si2p of Pr_3O_y/Si.

The curves of the as-deposited-Pr_3O_y/Si samples show a similar shape with a dominant silicate peak in the full range of thicknesses investigated, while after annealing a clear phase separation to
SiO$_2$ and Pr$_2$O$_3$ can be observed for thicker samples. The related Si2p spectra are shown in figure 1c. Here we can see a clear outward diffusion of silicon after annealing up to a thickness of 9nm. The outgoing silicon might support the phase separation by taking oxygen from the silicate and creating SiO$_2$. However, we do not observe this silicon out-diffusion in the Si2p levels of the samples consisting of the AlON buffer layer (not shown here). But in the O1s spectra of these samples (figure 1b) we still find the phase separation which can be observed at room temperature for thicker samples. Here, after annealing, the layers became much thinner (e.g. 54nm to 32nm) and the Pr$_2$O$_3$/SiO$_2$ ratio is higher for thicker samples (>19nm) compared to the samples without AlON buffer layer. It is probable that the oxygen of the AlON diffuses through the oxide and supports the phase separation. An alternative argument could be that the emissions at around 533 eV and 534 eV in the O1s are related to oxygen rich defects which might be influenced by the interaction with silicon and oxygen. Nevertheless, by using AlON as a buffer layer we find a decrease or indeed a prevention of silicon out-diffusion into the oxide and an increased Pr$_2$O$_3$ fraction after deposition.

3.2. Electrical characterization of MIS stacks on silicon

Next we report on electrical characterization of Pr$_2$O$_3$/Si and Pr$_2$O$_3$/AlON/Si stacks on silicon. In figure 2a a significantly reduced leakage current by using the buffer layer is shown. Here a 10nmPr$_2$O$_3$/1.5nmAlON/Si stack is compared with a much thicker 45 nm Pr$_2$O$_3$ film directly deposited on Si. An improvement by more than 7 orders of magnitude down to values in the range of 10$^{-7}$ A/cm$^2$ and 10$^{-9}$ A/cm$^2$ is found for CET values of 4 nm and 7 nm respectively. Compared to the Pr$_2$O$_3$/AlON line, the IV dependence of the pure 1.5 nm AlON film on Si suggests that after successful buffer layer integration, further decrease of leakage current is fulfilled by the Pr$_2$O$_3$ film. This might be due to a better band alignment as well as to reduced interfacial reactions. The samples consisting the buffer layer show generally an irreversible breakthrough, for the sample presented here electric fields of 6 MV/cm (AlON, $\varepsilon$=9) and 3 MV/cm (Pr$_2$O$_3$, $\varepsilon$=18) can be estimated at this point. The films shown in figure 2a have not been annealed but we have already reported the need of the post deposition annealing (PDA) in terms of reduced hysteresis and flat band voltage shifts in the CV characteristics [4]. The next important argument for the PDA step is delivered by the $D_{\varepsilon}$ plot presented in figure 2b. This shows that the introduction of the AlON buffer layer combined with subsequent annealing in nitrogen at 800°C results in the decreasing of the $D_{\varepsilon}$. Values of 5x10$^{-11}$-1x10$^{-7}$/eVcm$^{-2}$ are observed. Nitrogen incorporation leading to a passivation of dangling bonds and the above described phase formations after annealing might be responsible for this improvement of 1 to 1.5 orders compared to unannealed samples as well as to annealed samples without buffer layer.

![Figure 2](image_url)

Figure 2: a) IV-measurements of unannealed samples: 45nmPr$_2$O$_3$/Si, 1.5nmAlON/Si and 10nmPr$_2$O$_3$/1.5nmAlON/Si. b) Interface state density of Pr$_2$O$_3$/Si with annealing and Pr$_2$O$_3$/AlON/Si with and without annealing. c) CET versus thickness of Pr$_2$O$_3$ for as deposited Pr$_2$O$_3$/Si and Pr$_2$O$_3$/AlON/Si stacks and of annealed Pr$_2$O$_3$/Si samples.

In figure 2c we will discuss the interfacial layer formation and the permittivity values by a plot of the CET versus the physical thickness of Pr$_2$O$_3$. Results of Pr$_2$O$_3$/Si series with and without annealing and of some unannealed samples consisting of approximately 1nm AlON as the buffer layer are
shown. Using a simple model of capacitors in series and taking into account that we measure and plot the sum of Pr$_x$O$_y$ ($t_{PrO}$) and interfacial layer ($t_{IF}$) thickness, we can develop the following equation:

\[
CET = \frac{3.9}{\varepsilon_{Pr}} t_{Pr} + \frac{3.9}{\varepsilon_{IF}} t_{IF} = \frac{3.9}{\varepsilon_{Pr} + \varepsilon_{IF}} (t_{Pr} + t_{IF})
\]

(1),

where $\varepsilon_{Pr}$, $\varepsilon_{IF}$ are the permittivity values of the buffer, the interfacial, and the Pr$_x$O$_y$ layers. In the case that no buffer layer is used, the first term in equation (1) vanishes, $t_{Pr}$ represents the thickness of the buffer layer. Using this formula we performed linear fits ($y=n+m*x$). The slope m of this fit gives the $\varepsilon$ value of Pr$_x$O$_y$ and the extrapolated intersection with y-axis at $x=0$ ($n=t_{IF}$) delivers the CET of the interfacial layer (and of the buffer layer in the case where it was inserted). In the legend of figure 2c the results of these fits are summarized. They show similar $\varepsilon$ values for all series in the range of 17-20; for the annealed 58nmPr$_x$O$_y$/Si sample a $\varepsilon$ value of around 30 is calculated (marked by a circle in the diagram), and has not been taken into account for the fit. It is possible that after annealing the layers show some phase change in the volume. The spectroscopic results on these layers support this idea. A strong reduction of the $t_{IF}$ to 1.3 nm is shown by using the buffer layer. It must be pointed out that this value already contains the buffer layer thickness (see equation 1), so the unintentional interfacial layer thickness is even smaller. The series without buffer layer display much higher values of 3.4-3.9 nm. Assuming a permittivity value of 5.7 for SiO$_2$-rich Pr-silicate [18], this would result in a physical thickness of this interface of 7.5-8 nm, underlining again the need for interface engineering because this interface is a serious drawback of further EOT reduction.

Summarizing; the insertion of the buffer layer shows improved leakage current and $D_e$ values as well as a huge reduction of the CET of the interfacial layer. This might be due to a reduced thickness of this layer but an increased value of its permittivity could also contribute.

### 3.3. Electrical characterization of MIS stacks on silicon carbide

Here we report on our first electrical characterizations using an AlION buffer layer between the Pr$_x$O$_y$ layer and the 4H-SiC(0001) epi-layer.

![Image](image_url)

**Figure 3:** High-frequency-CV (filled symbols) and -GV (open symbols) (fig. 3a) and IV-measurements (open symbols, fig. 3b) of 70nmPr$_x$O$_y$ (stars), and of 1.1nmAlION/80nmPr$_x$O$_y$ (circles) and 5nmAlION/32nmPr$_x$O$_y$ (triangles) stacks on 4H-SiC(0001).

Figure 3a presents CV and GV plots of Pr$_x$O$_y$ and Pr$_x$O$_y$/AlION stacks on 4H-SiC. A wide range of permittivity values between 10-30 have been determined previously by single measurements. Here, in order to characterize the thickness dependence, several series have to be measured to obtain more reliable results. $D_e$ values near the conduction band edge of 1.5-4.7x10$^{-3}$/eVcm$^2$ have been calculated roughly by the GV peak maxima. If we look, however, to the width of the GV peak (interface
broadening, [17]), we recognize a significant smaller one in the case of the two Pr$_2$O$_5$/AlON/SiC
stacks; so, the effective interface state density might be smaller compared to the system without a
buffer layer. Additionally, initial improvements of the leakage current by 1-1.5 orders of magnitude by
using the 1.1nm AlON buffer layer is observed and by increasing the buffer thickness to 5nm the
leakage is further reduced by more than 2.5 orders (total thickness for this sample is only half that of
the others, fig 3b).

4. Conclusion and Outlook

We conclude that AlON provides a suitable buffer layer between high-k Pr$_2$O$_5$ and wide bandgap
SiC as well as between Pr$_2$O$_5$ and Si. This is evident from our spectroscopic investigations (decreased
silicon out-diffusion, higher Pr$_2$O$_5$ fractions, stable interface [14]), and from improved electrical
parameters (decreased values of leakage current, D$_i$, and interfacial layer thickness).

We will further investigate thickness dependence on a series of Pr$_2$O$_5$ on SiC substrates and a series
of stacks consisting of buffer layer with PDA steps. Furthermore we will improve our preparation
system in order to gain the ability to produce the full MIS stack in situ.

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