A SIPM PHOTON-COUNTING READOUT SYSTEM FOR ULTRA-FAST ASTRONOMY

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ABSTRACT

Very little work has been done searching for astrophysical transient optical emission in the millisecond to nanosecond regime with significant sensitivity. We call this regime “Ultra-Fast Astronomy”, or UFA. To investigate transients on as short time scales as possible, we developed our own customized readout system for a silicon photomultiplier (SiPM)-based UFA camera, intended for use on conventional astronomical telescopes. SiPMs, available in array packages for imaging a field, are capable of time-tagged single-photon detection in the visible wavelength range. Our readout system consists of 16 channels of 14-bit data logging. Each channel includes a 50-dB gain pre-amplifier, signal shaping circuits, an analogue front end, an analogue to digital converter, and a Xilinx UltraScale+ Field Programmable Gate Array Multipurpose System on Chip (FPGA-MPSoC) board for data-logging. We show that our system successfully read out the data from SiPM at 16 ns intervals with a maximum power consumption of 300 mW per channel and capability to perform concurrent 16 channels readout.

1. INTRODUCTION

Silicon Photomultipliers (SiPMs) are a type of solid-state photon-counting Geiger-mode avalanche diode offered commercially. These devices are gaining popularity in scientific research due to their robustness, immunity to magnetic fields, lack of high-voltage, and excellent photon resolving ability compared to photomultiplier tubes (PMTs). The output from a SiPM is charge pulses of 100 ns time scale, and the total charge within the pulse is proportional to the detected photon counts arriving within this time. In our Ultra-Fast Astronomy (UFA) Program, we wish to develop a SiPM-based camera to explore astronomy at time scales shorter than milliseconds which is not easily accessible via traditional CCD or CMOS sensors (Li et al. 2019; Denissenya and Linder 2021).

For most SiPM readout systems, application-specific integrated circuits (ASICs) are used to provide timing down to picosecond (ps) accuracy. However, such ASICs usually adopt a peak-locking architecture for reading both timing and charge information (Auger et al. 2016). Peak-locking architecture freezes the readout system when a photon triggers the circuit, introducing a restoring dead time of typically microseconds after each trigger. For UFA, we would like to retrieve information from every detected photon, so the dead time should be eliminated (Lau et al. 2020; Shafiee et al. 2021). Also, the system should be low-cost to allow scaling up to large arrays in the future. Here we summarise the main requirements of the system:

- 16-channel SiPM readout on a single readout board
- Low development and production cost of < 40 USD per channel
- Working temperature of −40°C to 85°C for harsh mountain observatory conditions
- < 20ns sampling time interval for photon arrival time recording
- Discrimination of SiPM signal from 0 to 10+ SiPM photoelectrons
- No readout-induced dead time
- On-board data processing system

From the above requirements, we designed a SiPM readout system consisting of a front-end board made from commercially available integrated circuit (IC) components, and a board to format and further process digitized pulses, an entry-level Field Programmable Gate Array Multipurpose System on Chip (FPGA-MPSoC). We describe these two boards in more detail below.
2. FRONT-END BOARD DESIGN

2.1. Overview and supporting circuits

Our front-end board incorporates two stages of pre-amplifiers (using an INA-03184 and a PGA5807a), a customized signal shaper based on an OPA4820, and ADC readout based on an AFE5818. We choose the pre-amplifiers to provide minimal noise with reasonable circuit complexity and power requirements. The OPA4820 used in the signal shaper provides a high gain-bandwidth product to ensure linearity at high frequency, and the AFE5818 ADC provides maximum flexibility via a high-speed ADC readout with a programmable gain.

This front-end board is designed on a single four-layer PCB with impedance control to ensure low-cost PCB fabrication. A rendering of the PCB design is shown in Fig. 1, with components grouped by function. Ungrouped components are currently unused.

![Fig. 1.— Rendering of the front-end board PCB design. The major circuit components and functional component groups are indicated.](image)

The system obtains +12V and +3.3V supplies from FPGA Mezzanine Card Low Pin Count (FMC-LPC) interface, which are supplied to the different ICs through the conversion paths given in Table 1.

| $V_{IN}$ | Function grouping | Conversion path | $V_{OUT}$ |
| --- | --- | --- | --- |
| 12V | Pre-amplifier INA-03184 | TPS82130 $\rightarrow$ TPS7A20 | 5V |
| 3.3V | Pre-amplifier PGA5807A | TLV758P | 3.2V |
| 12V | Signal Shaper | TPS82130 $\rightarrow$ TPS7A20 | 5V |
| 12V | AFE5818 analog power | TPS82130 $\rightarrow$ TPS7A20 | 5V |
| 3.3V | AFE5818 analog power | TLV758P | 3.2V |
| 1.8V | AFE5818 analog power | TPS73601 | 1.75V |
| 1.8V | AFE5818 digital power | LF5912 | 1.2V |
| 1.8V | AFE5818 digital power | TPS22919 | 1.8V |

2.2. Pre-amplifiers

The charge pulses from SiPM are first converted to voltage pulses via a 50Ω resistor and are transmitted through 50Ω coupling SMA cables to the readout board. The signal is then amplified by two-stages of pre-amplifiers, a low-noise amplifier INA-03184 followed by an PGA5807A amplifier, on the readout board. The INA-03184, from Hewlett Packard, is a silicon bipolar monolithic microwave integrated circuit amplifier with a low noise figure (2.5dB), a low power consumption (50mW per channel) and a simple circuit. It provides a flat 26dB gain up to 2GHz (hpa ND).
The second stage pre-amplifier is a Texas Instruments PGA5807A, with eight channels tunable from 12dB to 30dB gain up to 75MHz. This amplifier has a low pass filter active above 75MHz, eliminating thermal noise at higher frequencies. The power consumption of this amplifier is 60mW per channel. Since the PGA5807A is designed to work on differential signals, while we have only a single signal channel, half of the signal amplitude (6dB) is lost (PGA 2013). From this amplifier chain, the SiPM signal can be amplified by at most 50dB. The signal will then be fed into the signal shaper for further processing.

2.3. The signal shaper

A signal shaper performs analogue integration of the pulse (and the result is proportional to the charge in a SiPM pulse). This component replaces a high-speed digital integration algorithm in the FPGA downstream.

We use a "leaky" integrator design for our shaper, based on an OPA4820 op-amp IC. the OPA4820 provides four channels of high speed (650MHz gain-bandwidth product) amplifiers on a single rail 5V power supply (OPA 2008). The shaper consists of an op-amp integrator, with negative feedback from a 30pF capacitor and a 20kΩ resistor on as shown in Fig. 2. The resistor in the feedback line causes the signal to gradually decay with a time constant of ∼ 600ns. Such a "leaky" characteristic ensures that the shaper will not encounter saturation. Compared to a traditional op-amp integrator with a reset switch, the "leaky" design ensures no dead-time signal shaping.

The circuit is simulated using the Simulation Program with Integrated Circuit Emphasis (SPICE) program TINA-TI, as shown in Fig. 2. The simulation result (AC Bode plot) shows that the shaper has an integration band from 1MHz to 100MHz (gain plot slope -20dB per decade) without ring features. The plot also shows that the shaper provides an additional gain of ∼ 10dB on a 10MHz signal, which is the typical frequency of most SiPM pulses.

The OPA4820 consumes at most 6mA quiescent current per channel with a 5V supply, with maximum power consumption of 50mW under a large signal input.

2.4. Analog to Digital conversion

After shaping, the analogue signal is ready for digital conversion, with a signal on the order of mV. This is achieved using a medical analogue front end IC AFE5818 from Texas Instruments. The AFE5818 has 16 channels of 14bit analogue to digital conversion (ADC), at 65 mega samples per second (Mmps) (AFE 2015). However, due to the limitation of the FPGA Low Voltage Differential Signal (LVDS) interface limitation (16bit serialization, 1Gbps maximum), we set the ADC speed to 62.5Mmps.

The AFE5818 also performs internal signal amplification and shaping, providing an internal gain tunable from -4 to 54dB. In addition, the AFE5818 has a tunable 3rd-order, linear-phase low pass filter from 10MHz to 50MHz and a high pass filter tunable from 15kHz to 200kHz, allowing the removal of unwanted high-frequency noise and baseline fluctuation. The power consumption of the AFE5818 is 140mW per channel maximum.

3. FPGA+ARM MPSoC-BASED DIGITAL PROCESSOR SYSTEM DESIGN

We selected a Xilinx UltraScale+ MPSoC (model xczu3cg-1sfvc784e) development board from Alinx Inc. for processing the digital data coming from the ADC. (Boppana et al. 2015). First, the LVDS output from the AFE5818 ADC passes through FPGA Mezzanine Card Low Pin Count (FMC-LPC) interface to the high-performance I/O pins of the FPGA. The FPGA then performs deserialization and 16-bit word alignment to obtain ADC digitized data. Finally, the ADC digitized data are transmitted to the ARM core running a petalinux system through an Advanced eXtensible Interface 4 Direct Memory Access (AXI4-DMA) with a first-in first-out (FIFO) buffer. The petalinux system running on ARM core format the data and prepare them for post-processing. An image of the system (without heat-sinks, single channel equiped) is shown in Fig. 3.

A diagram of the data flow and control is shown in Fig. 4. Collected data are sent to a host computer via a Gigabit ethernet connection.
4. SIPM SIGNAL EXPERIMENTAL RESULTS

We assembled the readout system described above, and connected it to a Hamamatsu S14520-3050VS SiPM for testing. The detector was kept at room temperature, 25 ± 0.5°C on a metal block as heat reservoir and monitored by
a NTC-10k thermistor. The breakdown voltage of the SiPM was measured to be 39.47 V with the overvoltage kept at 3V, i.e. the power supply voltage = 39.47 + 3 = 42.47V. The manufacturer specifications for these conditions give a SiPM photon gain of $2.8 \times 10^6$ and a dark count of 600 kcps (kilo-counts per second) (Yamamoto et al. 2019). The temperature coefficient of breakdown voltage is 34 mV/°C. We can safely assume the thermal fluctuation of SiPM gain is $\pm 0.5 \times 0.034 / 3 \sim \pm 0.5\%$ with gain linear proportional to overvoltage.

The internal gain of the AFE5818 ADC was set to 0dB, the high pass filter frequency to 150kHz, and low pass filter frequency to 50MHz.

The system was placed in a dark grounded Faraday cage made with aluminum board, and dark counts of the SiPM were measured through the readout system, as shown in Fig. 5. The rise time of each count is about $\sim 50\text{ns}$. Taking trigger on $\frac{1}{4}$ p.e. level (10mV) and assuming a linear rising, the time uncertainty from signal arrival to trigger will be less than 20ns. With a 16ns sampling interval, the final photon arrival time logging accuracy of $\pm 16\text{ns}$ can be achieved.

The decay tail of photon pulses are $\sim 500\text{ns}$ long, corresponding to the time constant of the signal shaper. The height of the recorded readout pulses should be linear with the charge pulse within the SiPM (yielding about 30mV / photoelectron), because of the properties of the integrator. The number of concurrent incoming photons can therefore be determined by the readout pulse height. Since the ADC has a full range of $\pm 1\text{V}$, it is possible to detect more than 30 concurrent photoelectrons without saturation.

![Fig. 5.— Dark count signal captured by SiPM readout system](image)

From the figure, some noise can be seen on the SiPM pulse. This noise could possibly come from a ground loop from an external power supply, through the SiPM board to the readout system, as indicated in Fig. 6. To remove this noise, we implemented a Symlets 4 wavelet filter in Matlab (Chavan et al. 2011; Shafiee et al. 2016) as shown by the reddish line in Fig. 5.

Limited by the single-pass AXI4-DMA transfer size of $512kB$, we run the readout system for $16\text{ns} \times 512 \times 1024 / 2 = 4.194\text{ms}$ (each sample takes 2 bytes, 16ns sampling time). This limit will be eliminated in the future by adding a FIFO buffer based on DDR4 memory. In total, 2184 dark counts were detected with a detection threshold of 15mV, indicating a darkcount rate of $520\text{kcps}$, similar to the manufacturer specification of 600 kcps. The pulse height distribution is plotted as a histogram in Fig. 7. The plot shows two noticeable peaks: the first one (corresponding to a single electron) at $\sim 30\text{mV}$ and the second one (two electrons) at $\sim 60\text{mV}$. The second peak has $\sim 5\%$ count of the first one, matching the 5% crosstalk specification of S14520-3050VS SiPM (Yamamoto et al. 2019). This demonstrates the system’s ability to distinguish photon counts from the output signal from the SiPM.

5. SUMMARY AND FUTURE WORK

A novel, low-cost SiPM readout system has been developed for the UFA project. The readout system incorporates analogue processing and digitization ICs, data collection through FPGA and communication to host computer through Ethernet linkage. The readout system provides SiPM signal logging with $\pm 16\text{ns}$ photon arrival time logging accuracy, and photon counts are recovered in post-processing algorithm.

The readout board (without FPGA) takes at most $50 + 60 + 50 + 140 = 300\text{mW}$ per channel with a per-channel cost of less than 20USD. The readout board is built with industrial standards (working temperature from $-40\degree C$ to $85\degree C$) for harsh weather at the observatory.

We plan to build on our success in making a fast, low-cost per channel system by decreasing noise, increasing readout capabilities, and improving imaging. In order to accomplish this, we plan to begin work immediately on the following tasks:
Fig. 6.— Schematic of testing setup. The proposed ground loop path is indicated by the blue arrow.

Fig. 7.— Pulse height distribution plot of dark counts.

- Move the SiPM powering circuit onto the front-end PCB to reduce ground loop noise
- Simplify the analog amplifier chain by utilizing the internal amplifier in the AFE5818
- Perform low-temperature testing in the laboratory and replace failed board and components for upcoming field tests
- Add a DDR4 memory-based FIFO buffer for continuous data collection
- Integrate photon count recovery post-processing algorithm into FPGA logic
- Implement imaging by using a position-sensitive SiPM and a position-decoding algorithm within the FPGA.

The goal of this work is to produce an astronomical camera that can be used for transient searches on all ~ sub-second time scales down to our limiting time scale, and for searches for high frequency non-random signal patterns, from ultra-short periodicity to SETI signals. With the additional work listed, the readout system should be fully capable of supporting this goal.
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