Role of ALD Al$_2$O$_3$ surface passivation on the performance of p-type Cu$_2$O thin film transistors

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Abstract

High-performance p-type oxide thin film transistors (TFTs) have great potential for many semiconductor applications. However, these devices typically suffer from low
hole mobility and high off-state currents. We fabricated p-type TFTs with a phase-pure polycrystalline Cu$_2$O semiconductor channel grown by atomic layer deposition (ALD). The TFT switching characteristics were improved by applying a thin ALD Al$_2$O$_3$ passivation layer on the Cu$_2$O channel, followed by vacuum annealing at 300 °C. Detailed characterisation by TEM-EDX and XPS shows that the surface of Cu$_2$O is reduced following Al$_2$O$_3$ deposition and indicates the formation of 1–2 nm thick CuAlO$_2$ interfacial layer. This, together with field-effect passivation caused by the high negative fixed charge of the ALD Al$_2$O$_3$, leads to an improvement in the TFT performance by reducing the density of deep trap states as well as by reducing the accumulation of electrons in the semiconducting layer in the device off-state.

Introduction

Metal-oxide thin film transistors (TFTs) have attracted increasing interest especially in display technologies owing to their optical transparency and high mobility, low processing temperatures and material costs, and mechanical flexibility. This has led to the development of high-performance n-type semiconducting oxide materials, such as amorphous indium-gallium-zinc-oxide (IGZO) with electron mobility of several tens of cm$^2$V$^{-1}$s$^{-1}$. However, the full utilisation of oxides in p-n junction based electronics and complementary metal oxide semiconductor (CMOS) integrated circuits, is still hindered by the lack of high performance p-type oxides. The reason for the challenges in achieving feasible hole conductivity are the differences in the electronic structures of the n- and p-type oxides. The transport path of holes in p-type oxides, valence band maximum (VBM) consists typically of localised anisotropic oxygen 2p orbitals, which results in large hole effective mass and low mobility. In addition, the concentration of holes in oxides is often limited by the high formation energy of the cation vacancies, as well as the annihilation of holes due to the low formation energy of the oxygen vacancies. In case of cuprous oxide Cu$_2$O, however, the valence band is formed by the hybridisation of the O 2p and Cu 3d orbitals, resulting in a less localized
VBM and pathway for hole transportation for holes formed via copper vacancies ($V_{Cu}$) as acceptor states. Such special configuration and high hole mobility have made Cu$_2$O an extensively studied p-type oxide for TFTs, and due to its other advantageous properties, such as material abundance and solar absorbance, it has also been investigated as a potential candidate for multiple device applications ranging from photovoltaics to sensors.

Cu$_2$O layers for TFTs are traditionally fabricated by physical vapour deposition (PVD) methods, such as pulsed lased deposition (PLD) and sputtering. Solution-based processing methods have also been used, such as spin coating, electrodeposition and inkjet printing. For scalable device applications it is crucial to be able to deposit films with uniform and controllable thickness and composition over large areas, preferably at low or moderate temperatures. Atomic layer deposition (ALD) has been proven invaluable for the fabrication of modern microelectronics, where it is used to produce ultra-thin high-quality dielectric films for devices including metal-oxide semiconductor field effect transistors (MOSFET) and dynamic random access memories (DRAM). ALD has the potential to be extended in production of active device layers. It has already shown to be capable of depositing n-type semiconducting films, such as IGZO, with properties compatible with what has been achieved by PVD techniques. The successful application of ALD grown n-type semiconducting oxides in TFTs has been demonstrated both on rigid and flexible substrates. Development of ALD processes for p-type materials (NiO, CuO$_x$, SnO) has been mostly of interest for photovoltaics, especially in perovskite and tandem solar cells, where they can be used as electron-blocking and hole transport layers. However, some examples of other electronics applications, such as p-type TFTs with ALD grown semiconductor channels have been published. For example, high performing TFTs with ALD grown CuO$_x$ films (consisting of both Cu$_2$O and CuO phases) have been reported by Maeng et al. Their devices showed an unusually high field effect mobility of $\mu_{FE} = 5.6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, which is higher than the $\mu_{FE}$ of any reported CuO$_x$ device in the literature. Unfortunately, to our best knowledge, these results have not yet been consistently reproduced, nor are there other reports of
the use of ALD Cu$_2$O in TFTs. However, ALD was used to demonstrate high-performance p-type TFTs with SnO channel. There it was observed that applying an Al$_2$O$_3$ channel passivation significantly improves the TFT performance via the reduction of trap states at the interface.

Here, we investigate the influence of an ALD Al$_2$O$_3$ passivation layer on the performance of p-type TFTs with an ALD grown Cu$_2$O channel. We show that passivation and subsequent vacuum annealing improve the transistor performance metrics. In addition to device measurements, the Al$_2$O$_3$/Cu$_2$O interface was characterised in detail by using x-ray photo-electron spectroscopy (XPS) and transmission electron microscopy (TEM) to obtain more information of the surface reactions taking place during the deposition of the Al$_2$O$_3$ on the Cu$_2$O and how the passivation layer and the oxide interface affect device performance.

**Results and discussion**

**Cu$_2$O film characterization**

The X-ray diffraction pattern of a 40 nm thick Cu$_2$O film is presented in Fig. 1(a). The GIXRD revealed that the films were polycrystalline Cu$_2$O, with the most intense reflections associated to the (200), (111), and (220) planes of the cubic Cu$_2$O. No trace of CuO or Cu were detected, indicating that the films were phase-pure Cu$_2$O, with crystallite size of ca. 30 nm. The crystalline structure of the films was visible also by AFM (see example Fig. 1(b)) showing the films to have distinct grains in the morphology with a high surface roughness of ca. 4.5 nm (RMS). Despite the high film roughness, we can assume the films to be continuous, based on the detailed growth analysis of corresponding ALD Cu$_2$O films reported by Iivonen et al. in Ref.23 Hall effect measurements confirmed the p-type conductivity of the films, with a resistivity of $\rho = 300 \ \Omega$cm, hole density of $N = 10^{16} \ \text{cm}^{-3}$ and Hall mobility $\mu_H = 0.6 \ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$. The Hall hole mobility is somewhat lower than what has been reported earlier for Cu$_2$O films. However, as-deposited films processed at lower temperatures generally
pose a lower hole mobility, in the order of few cm\(^2\)V\(^{-1}\)s\(^{-1}\)\(^{15,10,12,24,25}\) as a maximum, than films deposited and/or treated at high temperatures, in which the mobility can reach tens of cm\(^2\)V\(^{-1}\)s\(^{-1}\)\(^{13}\) but the variation between different reports is vast. In our case the low hole mobility may be due to low film thickness, which, combined with small grain size and high surface roughness, limits the conduction. Han et al. have investigated the role of the Cu\(_2\)O film morphology on the charge carrier characteristics, and they concluded that nanocrystalline structure of thin Cu\(_2\)O films can suggest the presence of potential energy barriers at grain boundaries, leading to effects such as grain boundary scattering, which hinders the hole transport in the thin films.\(^{26}\) This is further enhanced by the formation of a conductive CuO layer onto the grain surfaces.\(^{27}\)

![XRD pattern and AFM image](image)

**Figure 1:** a) XRD pattern of the as-deposited, phase-pure polycrystalline Cu\(_2\)O film and the ICCD cards for both Cu\(_2\)O and CuO, used for indexing. b) 3D AFM image of 2 \(\mu\)m \(\times\) 2 \(\mu\)m area of the corresponding film. The film roughness (RMS) is 4.5 nm.
**TFT performance**

The Cu$_2$O films were tested as p-channels in simple bottom-gate thin film transistor devices with Au source and drain electrodes and p-Si substrate acting as a common gate (see inset in Fig. 2). The switching characteristics of the as-deposited films without the Al$_2$O$_3$ passivation layer were negligible as shown in Fig. 2. With a 10 nm Al$_2$O$_3$ layer deposited on the Cu$_2$O channel the off-state drain current ($|I_{DS}|$) at positive gate voltage $V_{GS}$ decreased by three orders of magnitude and switching with $I_{on}/I_{off} \approx 30$ was measured. It has been shown that the gap state density in oxide semiconductor TFTs can be affected by the ambient moisture and oxygen adsorption on the top channel surface, which can be suppressed by the passivation layer.\cite{28} However, for this effect the type or fabrication method of the passivation layer seems not to be critical, as improvements in the performance of n- and p-type TFTs have been reported with different ALD and solution-processed oxide films as well as with organic passivation layers.\cite{22,29-31}

![Figure 2: Gate transfer characteristics of a TFT device with 40 nm ALD Cu$_2$O p-channel, with and without Al$_2$O$_3$ passivation, shown as black and dark-red curves, respectively. In both cases the device is measured with drain voltages ($V_{DS}$) of -10.0 V (dashed lines) and -1.0 V (solid lines). Inset shows the schematic of the TFT device with Al$_2$O$_3$ passivation layer.](image)

To further improve TFT performance, the devices were annealed for 10 mins in 1.5 mbar N$_2$ directly after Al$_2$O$_3$ deposition. A low vacuum environment was chosen to prevent phase
transitions of the Cu$_2$O layer into CuO or Cu. As seen in Fig. 3(a) the transfer characteristics of the devices started to improve after annealing at 250 °C, but the most significant effect was gained at 300 °C, with output characteristics shown in Fig. 3(b). At higher annealing temperatures transfer characteristics begun to deteriorate. In the devices annealed at 400 °C no switching was observed, and a positive $I_{DS}$ was recorded (data not shown). In the unpatterned Al$_2$O$_3$/Cu$_2$O film reference sample on glasss the 400 °C annealing caused color changes visible to the naked eye, potentially indicating a partial reduction into metallic Cu. The same effect was observed also when the annealing was performed in 1 atm Ar atmosphere at the same temperature.

Despite the increase in the switching ratio of up to $I_{on}/I_{off} = 5 \cdot 10^3$ in the sample annealed at 300 °C, the carrier mobility remained low, with field-effect mobility for the as-deposited and annealed devices being $\mu_{FE} \approx 1.5 \cdot 10^{-3}$ cm$^2$V$^{-1}$s$^{-1}$, which was calculated as $\mu_{FE} = (g_m L) / (W C_{ox} V_{DS})$, where $g_m$ is the transconductance ($g_m = \delta I_{DS} / \delta V_{GS}$), $L$ and $W$ the channel length and width, respectively, ($L=50$ µm, $W=1000$ µm), and $C_{ox}$ the gate dielectric capacitance per unit area, calculated using a dielectric constant of 3.9 for SiO$_2$ gate oxide. Additionally, high operating voltages were required for switching, even for devices with enhanced characteristics, with a threshold voltage $V_{TH}$ and subthreshold swing SS of -19.8 V and 11.5 V dec$^{-1}$, respectively. The corresponding $V_{TH}$ and SS of the as-deposited device with Al$_2$O$_3$ passivation were -13.0 V and 29.2 V dec$^{-1}$, respectively.

The characteristics of the TFTs without the Al$_2$O$_3$ layer were not improved upon annealing, and Hall effect measurements showed there to be no change in the carrier density of the annealed Cu$_2$O samples (Fig. S1 in the Supporting Information). Therefore, it can be concluded that the Al$_2$O$_3$ passivation is the reason for the improved performance. Similar effects have been reported for p-type TFTs with passivated SnO channels. Kim et al. showed an improvement in devices with ALD SnO channel passivated with ALD Al$_2$O$_3$, which was further enhanced by subsequent annealing. Similar observations were made by Qu et al., who passivated sputtered SnO channels by ALD Al$_2$O$_3$ as well as with organic
Figure 3: (a) Transfer characteristics of the Cu$_2$O TFTs with Al$_2$O$_3$ passivation, annealed in low-vacuum at different temperatures. Measured with $V_{DS}=-1.0$ V. (b) Output characteristics of a device annealed at 300 °C.

Our results are consistent with these findings, both reporting an increase in the $I_{on}/I_{off}$ ratio and a decrease in SS upon ALD Al$_2$O$_3$ passivation. These changes can be associated with a reduction in the trap state density at the channel surface. It seems that the ALD Al$_2$O$_3$ passivation has more impact on reducing the deep trap state density, both in the Cu$_2$O and SnO, indicated by the reduction in the SS. On the other hand, the shallow traps (tail states near the valence band), are less affected, as the carrier mobility does not increase significantly. Interestingly, it has been reported that passivation of n-type oxide TFTs by ALD Al$_2$O$_3$ increases the mobility and SS which is opposite to what has been observed for the p-type devices.
The low field-effect mobility in the order of $\mu_{FE} = 10^{-3} - 10^{-2}$ cm²V⁻¹s⁻¹ is typical for Cu₂O TFTs processed at low/moderate temperatures and with thin channel layer of few tens of nm, regardless of the deposition technique. However, there are some reports where orders of magnitude higher $\mu_{FE}$ values, up to 6 cm²V⁻¹s⁻¹ have been achieved, even with a room-temperature processing and mixed phase Cu₂O-CuO films. The limited mobility in Cu₂O thin films is typically associated with the high density of subgap trap states and grain boundary scattering. Additionally, it has been shown that a CuO layer can form at the Cu₂O/SiO₂ interface already at 300 °C, which further increases the trap density and, hence, has a negative impact on the transfer characteristics. Therefore, it has been suggested that replacing SiO₂ with a high-k dielectric may result in better performance.

We also tested devices with a 75 nm thick ALD Al₂O₃ gate oxide, and observed switching in the devices with a decreased SS (7.5 V dec⁻¹) and a $V_{TH}$ of 10.6 V (See Fig. S2), indeed indicating a reduction in the trap states at the dielectric/semiconductor interface. However, in this case the Al₂O₃ gate oxide had a lower breakdown voltage than the 100 nm SiO₂, which meant that the channel was not yet fully depleted when the gate modulation was lost, limiting both the I_on/I_off ratio and the mobility.

To investigate the effect of annealing on the Al₂O₃/Cu₂O stack in detail, a high-temperature GIXRD measurement was performed. 10 nm Al₂O₃ was deposited on a 40 nm Cu₂O sample and the diffraction patterns were collected at 150–600 °C in 20 mbar N₂ (Fig. 4). It was observed that at 250 °C the (111) and (200) reflections shift towards larger 2θ angles, indicating a decrease in the unit-cell parameters, possibly due to stress relaxation when the annealing temperature exceeds the deposition temperature. As seen in the samples annealed earlier, signs of metallic Cu appeared also in the passivated sample. These changes, seen as reflections at ca. 43° and 50.5°, take place just above 300 °C. At 475°C the Cu reflections disappear and features corresponding to formation of CuO become visible. These changes in the film structure upon annealing could explain the observed narrow annealing temperature window for optimal TFT performance.
Moreover, when annealed under similar conditions, a Cu$_2$O film without the Al$_2$O$_3$ layer undergoes oxidation to CuO already at 300 °C (Fig. S3), showing the importance of the Al$_2$O$_3$ layer to the phase-stability of the films during annealing. This behaviour of both the bare ALD Cu$_2$O and the Al$_2$O$_3$Cu$_2$O film stack differ from what has been shown for Cu$_2$O films and devices fabricated by physical deposition methods such as PLD and sputtering. There a high temperature deposition or annealing at 500–800 °C, both in vacuum and inert gas atmosphere have shown to improve the device performance significantly by reduction of the CuO phases on the grain boundaries and increase in the Cu$_2$O crystallite and grain sizes, while the Cu$_2$O phase remains stable. Though the film thickness may have an effect on the film behaviour during the annealing, it does not fully explain the observed differences between PVD and ALD deposited Cu$_2$O. One explanation is that the grain boundaries of the nanocrystalline ALD Cu$_2$O contain a higher density of hydroxyl groups, which then accelerate the film reduction, despite the presence of the passivation layer, and the partial oxidation into CuO is later initiated by the oxygen diffusion from both the Al$_2$O$_3$ layer as well as the SiO$_2$ gate oxide. However, this remains inconclusive.
Al₂O₃/Cu₂O interface characterisation

Our results and the previous studies on the passivation of TFTs with oxide semiconductor channels show that quality of the interface between the channel oxide and the passivation layer can have a significant impact on the device performance. Especially, in the case of passivation by chemical routes, such as ALD, it can be assumed that the interface is further modified by the surface chemistry taking place during the layer deposition. It has been shown that exposure to certain ALD metal precursors, namely alkyl compounds, can reduce a surface oxide layer if the reactions are energetically favourable. For instance, for surface reactions of diethylzinc, commonly used as a precursor for ALD ZnO, the Gibbs free energies for reduction reactions of Cu₂O surface into metallic Cu are $\Delta G_r = (-300)$–$(-200)$ kJ mol$^{-1}$ (T = 373 K). The reactions between TMA and Cu₂O can be assumed to be even more favourable due to higher reactivity of the TMA. The reduction of oxidised Cu surface during the first Al₂O₃ cycles has been verified both numerically and experimentally. Gharachorlou et al. investigated the TMA and hydroxyl-free oxidised copper surface reactions and presented that the TMA is adsorbed and dissociates at the Cu₂O surface and in those reactions consumes oxygen from the Cu₂O (or CuO), thus reducing the oxidised Cu$^+/Cu^{2+}$ surface to the metallic Cu$^0$ state. Additionally, their results indicated formation of a CuAlO₂ interface during the first three Al₂O₃ cycles with TMA and O₂. Their proposed overall reaction is:

$$2\text{Cu}_2\text{O} + \text{Al(CH}_3)_3 \rightarrow \text{CuAlO}_2 + 3\text{Cu} + 2\text{CH}_4(g) + \text{CH}_{ads}.$$ (1)

Using a process with H₂O as a reactant leads to surface hydroxyl groups forming during deposition. However, it can be assumed that the mechanism described above is still valid, because it has been calculated that the hydroxyl coverage does not affect the TMA dissociation on the surface, but only on growth efficiency.

The formation of a CuAlO₂ interface could be beneficial to TFT performance, because
it is a known p-type material with low $V_{Cu}$ formation energy. In order to investigate in detail the reduction of $Cu_2O$ by TMA, and the formation of the $CuAlO_2$ interface layer, samples were prepared for XPS and TEM. XPS was used to analyse $Cu_2O$ films with and without the $Al_2O_3$ passivation and subsequent annealing at 300 °C. To minimize the need of $Ar^+$ etching to reach the $Al_2O_3/Cu_2O$ interface, only 20 cycles i.e. ca. 2 nm of $Al_2O_3$ was deposited on samples for XPS measurements. The XPS of as-deposited $Cu_2O$ without the $Al_2O_3$ layer confirmed the films to be phase-pure $Cu_2O$ seen both in the $Cu$ 2p and Cu LMM spectra, with a minor $CuO$ content present at the film surface, as well as a high content of hydroxyl groups, as seen in the measured O 1s spectra (See Fig. S4).

The effect of the annealing on the $Cu_2O$ film was investigated by measuring a sample annealed at 300 °C. No changes to the film composition were observed (Fig. S6). Figure 5 shows the XPS spectra of the $Al_2O_3/Cu_2O$ films, before and after annealing at 300 °C. As seen in Fig. 5(a) the $Cu$ 2p spectra of the both films show the absence of the $CuO$ phase. However, the differentiation of between the $Cu^+$ and $Cu^0$ states cannot be done from the $Cu$ 2p spectrum. The complementary Cu LMM spectra of the samples in Fig. 5(b) show the significant broadening of the Auger electron peak compared to the $Cu_2O$ sample without the $Al_2O_3$ layer. This corresponds to the presence of the metallic $Cu^0$ at the $Al_2O_3/Cu_2O$ interface, confirming the reduction of the $Cu_2O$ due to TMA exposure. This $Cu^0$ can remain metallic even after the subsequent pulsing of $H_2O$, as the oxidation reactions into $Cu_2O$ or $CuO$ are not thermodynamically favourable (Tab. S1(a) and (b)). However, the oxidation by residual $O_2$ in the deposition reactor is possible (Tab. S1(b) and (c)).

The O 1s spectra were also recorded from both samples. The deconvoluted spectra in Fig. 5(c) and (d) show the oxygen in lattice $Cu_2O$ at 530.2 eV, a minor $CuO$ contribution at 529.8 eV, and $Al_2O_3$ bound oxygen at 531.6 eV, as well as the presence of high hydroxyl concentration ($\sim$532 eV). This is contributed by both the persistent surface hydroxyl groups on the $Cu_2O$ as well as the remaining -OH species in the $Al_2O_3$ from the TMA + water process at relatively low deposition temperature of 150 °C. There is a small difference
in the O 1s spectra of the as-deposited and annealed samples, namely in the Al₂O₃ related O content, which may indicate a partial diffusion of the Al into the Cu₂O film or a densification of the film upon annealing, which would lead to a slightly different etching rate during the Ar ion sputter cleaning.

However, the measured ex-situ XPS data can not be reliably used to confirm the presence of the CuAlO₂ phase at the Al₂O₃/Cu₂O interface, as the related changes are too subtle to be distinguished from the Al₂O₃ and Cu₂O signals within the probed volume. Moreover, we measured the valence spectra of the annealed Cu₂O and Al₂O₃/Cu₂O samples. Deuermeier et al. reported a shift in the binding energy of a Cu₂O during the ALD of Al₂O₃. In their in situ XPS experiments on ALD Al₂O₃ growth on sputtered Cu₂O surface the position of the valence band edge (E_F − E_VB) of the Cu₂O increased from original 0.4 eV to 0.6 eV after the first Al₂O₃ ALD cycle indicating a formation of Cu/Cu₂O Schottky junction. Though our core level LMM spectrum showed the formation of the Cu, similar indication of a Schottky junction formation was not observed in the valence spectra and 0.9 eV E_F − E_VB was measured for both the original Cu₂O as well as for the Al₂O₃/Cu₂O interface (See Fig. S5). However, this does not exclude the potential Fermi level pinning at the interface due to the reasons explained above.

To obtain more evidence on the proposed CuAlO₂ interface layer formation, a sample with 10 nm Al₂O₃ deposited on Cu₂O, annealed at 300 °C, was imaged with TEM and TEM-EDS elemental mapping was recorded from the film interface (Fig. 6). Figure 6(a) shows a low magnification image of the film stack, with a Cu₂O film sandwiched between two 10 Al₂O₃ films on SiO₂/Si. In Fig. 6(b) the higher magnification shows the polycrystalline Cu₂O and with the conformal, amorphous Al₂O₃ on top. The EDS measurement of the interface region (6(c)) reveals a 1–2 nm region at the interface with a mixed Al and Cu oxide composition (Fig. 6(d)). Though the actual composition of this region cannot be reliably determined from the TEM-EDS data, it is in qualitative agreement with the observations by Gharachorlou et al. of a formation of a CuAlO₂ layer during the first Al₂O₃ cycles according
Figure 5: XPS spectra of the Al$_2$O$_3$/Cu$_2$O interface region, measured after 90 s 0.5 keV Ar$^+$ sputtering, (a) Cu 2p of the as-deposited (black) and annealed (dark red) samples. (b) Cu LMM Auger electron spectra, corresponding spectrum of a Cu$_2$O film without the Al$_2$O$_3$ passivation layer shown by dashed grey line as a reference. The O 1s spectra of the (c) as-deposited and (d) annealed sample. The deconvoluted peaks correspond to oxygen in Cu$_2$O (dark red), CuO (orange), hydroxyl -OH (blue), and Al$_2$O$_3$ (green).
Figure 6: Transmission electron microscopy (TEM) micrographs (a)-(c) of a Cu$_2$O thin film sample with 10 nm Al$_2$O$_3$ passivation layer, annealed in 1.5 mbar N$_2$ for 10 min. (d) a corresponding TEM-EDS mapping of Al and Cu at the sample interface depicted in (c).

to Eq. 1.

This reduction mechanism and possible formation of the CuAlO$_2$ does not fully explain the significant improvement in the TFT performance. We tested the effect of the Al$_2$O$_3$ film thickness on the TFT transfer characteristics and observed that when the Al$_2$O$_3$ thickness was only 2–5 nm the device performance was similar to TFTs without the Al$_2$O$_3$ passivation and the improvement in the TFT transfer characteristics was detected only with a thicker, 10 nm Al$_2$O$_3$ layers (See Fig. S6). This indicates that the formation of the interface layer by the TMA exposure during the first couple of tens of deposition cycles is not sufficient in improving the device performance, but thicker coverage with the Al$_2$O$_3$ layer is required. Therefore the key to the improved characteristics are likely in the properties of the ALD Al$_2$O$_3$ film itself.

A plausible reason for the observed behaviour is the high negative fixed charge density ($Q_f = 10^{-13}$ cm$^{-2}$) of the ALD Al$_2$O$_3$, which has traditionally been utilised in c-Si solar
cells where it reduces the recombination losses on the Si surface via surface defect density reduction and by field-effect passivation. The field-effect passivation is based on the reduction of electron or hole concentrations on the surface/interface by the means of an intrinsic internal electric field. The field-effect passivation is based on the reduction of electron or hole concentrations on the surface/interface by the means of an intrinsic internal electric field. In our measured TFT data the impact of the field-effect passivation is indicated by the negative shift in the $V_{TH}$ and the reduction in the $I_{off}$. It has previously been reported by Han et al. that the high off-state current in the Cu$_2$O TFTs is due to accumulation of minority charge carriers (electrons) at positive gate voltage regime. The application of the field-effect passivation by ALD Al$_2$O$_3$ on the Cu$_2$O channel and subsequent annealing can be an effective way in reducing the accumulation via electrostatic shielding, which leads to the orders of magnitude lower off-state current and, hence, improves the performance of TFTs with Cu$_2$O p-channels.

Conclusions

p-Type thin film transistors with ALD grown phase pure polycrystalline Cu$_2$O channel layer were fabricated. The TFTs with as-deposited films showed only limited switching performance, due to the unoptimised film properties and processing parameters, but the characteristics were improved by depositing an 10 nm ALD Al$_2$O$_3$ passivation layer on the Cu$_2$O channel and by subsequent annealing at 300 °C in low vacuum. The analysis of the transfer characteristics indicates that the improvement is due to the reduced number of trap states at the channel. The detailed investigation of the Al$_2$O$_3$/Cu$_2$O interface by XPS and TEM showed a partial reduction of the Cu$_2$O and possible formation of a 1-2 nm thick CuAlO$_2$ layer. The p-type CuAlO$_2$ layer with a low Cu vacancy formation energy can be beneficial to the device operation, but cannot solely explain the better performance of the Al$_2$O$_3$ passivated TFTs. Hence, we conclude that the main benefit of the Al$_2$O$_3$ passivation comes from its high negative fixed charge density that reduces the accumulation of electrons in the Cu$_2$O channel when positive gate voltage is applied and, thus, reduces the $I_{off}$ of the
devices. While the field-effect passivation may not be applicable to tradition nanoscale Si-based CMOS devices, as it influences the $V_{th}$ and the transport of charge carriers in ways that can be detrimental to the circuit operation, it can be an useful tool in the development of alternative approaches that utilise p-type oxide semiconductors with moderate charge carrier density.

**Experimental**

The Cu$_2$O films were grown on 5 cm × 5 cm substrates of thermally grown SiO$_2$ on p-Si (resistivity 0.001 Ωcm, Si-Mat) by atomic layer deposition at 200 °C in an ASM F-120 reactor. Copper(II) acetate Cu(OAc)$_2$ with source temperature of 185 °C, and water vapor were used as precursors. Each Cu$_2$O ALD cycle consisted of 2 s Cu(OAc)$_2$ pulse / 2 s purge / 1.5 s H$_2$O pulse / 1.5 s purge, which resulted a growth per cycle of 0.011 nm. A fluorine-free precursor was chosen because residual fluorine impurities can affect the electrical properties of the films, F being a known n-type dopant, and, additionally lead to poor adhesion of the films due to the accumulation of the fluorine into the interfaces. Details of the growth chemistry and materials characterisation are published by Iivonen et al. in Ref. No further optimisation of the Cu$_2$O film processing or thickness was done regarding the device operation. Bottom gate TFT structures, with the Si substrate acting as a common gate and thermally grown 100 nm thick SiO$_2$ as a gate dielectric, were fabricated with a standard photolithography and nanofabrication methods to test the performance of the Cu$_2$O films. The 40 nm Cu$_2$O films were patterned by wet etching using diluted (0.025 M aq.) HCl, and 100 nm thick Au source and drain electrodes were deposited by thermal evaporation (Edwards Coating System E306A), with a base pressure of 10$^{-6}$ mbar. After electrode patterning, the Cu$_2$O channel was passivated by a 10 nm Al$_2$O$_3$ film grown by ALD (Cambridge Nanotech (Veeco) Savannah S100) at 150 °C with trimethylaluminium (TMA, Sigma Aldrich) and water vapour. Finally, the devices were annealed in 1.5 mbar N$_2$ at 200–400 °C for 10 minutes.
Film thickness was determined with x-ray reflectivity (XRR) using a PANalytical X’Pert Pro MPD diffractometer, which was also used for x-ray diffraction (XRD) measurements. The measurements were performed in the grazing incidence (GIXRD) geometry at an incidence angle of 1°. The same geometry was used with the high-temperature GIXRD measurements, where Anton-Paar HTK1200N furnace was used for sample heating in 20 mbar N₂ (N₂ flow 40 sccm) and data were collected at 150–600 °C with 15 °C intervals. Atomic force microscopy (AFM) images were taken with Bruker Multimode 8. The electrical properties of the Cu₂O films were characterised by Hall-effect measurements using van der Pauw configuration with a magnetic field of 0.2 T at room temperature (MMR Technologies Hall System). Thin film transistors were measured using a Cascade probe station and Agilent B1500A semiconductor device parameter analyser. The electrical characterisations were performed in dark to suppress the film photoconductivity. In the interface examinations Escalab (Thermo Fisher Scientific) x-ray microprobe was used for x-ray photoelectron spectroscopy (XPS), and the results were analysed using CasaXPS processing software. Transmission electron microscopy (TEM) imaging was done using FEI TALOS T200X operated at 200 kV with EDS for elemental mapping.

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Supporting Information Available

Supporting Information is available from the Wiley Online Library or from the author.

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