Development of Analog Behavioural Model of BiMOSFET

Harini. V, Mahesh Acharya, A. Vijayakumari

Abstract: Behavioural modelling of a power semiconductor device offers many advantages to an application engineer as it is possible to model the device from the available datasheet without a detailed knowledge of the fabrication process. The development of an analog behavioural model for a BiMOSFET is undertaken here by using the Hammerstein model. The Hammerstein model is developed with static and dynamic block sub-blocks and is designed to respond for varying temperatures. The datasheet values of Ic and Vce are utilized to derive the static linear block, while the dynamic block is modelled as Hammerstein current source. The developed model of the BiMOSFET has been verified for its terminal characteristics through OrCAD simulations and hardware testing. The developed model of BiMOSFET exhibits fast simulation times with reasonable accuracy. The hardware testing is carried out with BiMOSFET IXBF55N300 by observing its currents and voltages under the variation of gate voltage at constant collector emitter voltage and variation of collector emitter voltage at constant gate voltage.

Keywords: Analog Behavioural Model, BiMOSFET

I. INTRODUCTION

Power electronic systems are the key enablers and the most ubiquitous systems in today’s era of ‘Green Engineering’ due to the evolution of power semiconductor devices catering towards increasing conversion and volumetric efficiencies [1, 2]. Simultaneously, high penetration of electrical circuit simulation software such as SPICE in industries has also become possible owing to increased computing power enabling complex system developments. A successful power electronic design is the result of a proper combination of power devices, circuit topology, and control circuitry. At the application level, the external steady state and transient characteristic of the device is more important than the fundamental physics-based equations [3]. For high power devices, vendor-based or intrinsic SPICE models are often not available necessitating development of device modelling techniques [3]. Semiconductor device modelling can be classified into four types: behavioural modelling, structural modelling, code modelling and analog modelling in HDL (Hardware Definition Language) [4]. Behavioural model has low simulation accuracy and neglects static and dynamic non-linear effects. However, the usage of piece wise linear and linear elements in modelling ensures convergence and a reduced simulation time. Structural models have higher accuracies. But, the generated discontinuous non-linear curves cause convergence problems. Code modelling implements the device equations in a subroutine. However, it is not portable and requires simulator recompilation on each model addition. Analog HDL models have high accuracies and mid-level simulation times. However, they require many parameters which are not available in datasheets and are not SPICE portable [5]. Analog Behavioural Models (ABM) are SPICE compatible user-friendly extensions of behavioural models. It allows for the direct implementation of the device non-linear equations. Also, the non-linear characteristic is linearized by piece wise linear approximation [5]. Various ABM for SPICE are proposed in literature for IGBT [6-10, 12]. One among the earliest model was the Hefner Model which exhibited good computation times with reasonable accuracy. The model was first designed for SABER and then subsequently adapted to SPICE [6, 7]. The Hefner model is suitable only for constant temperature simulations [8]. Conversely, the Hammerstein model consisting of a static block (linear characterization) and dynamic block (non-linear characterization) [9, 10], with its behaviour closely resembling the physics-based model in [11] overcomes the limitations of Hefner model. However, these models have been simulated using Saber Software which are not Spice compatible. Semiconductor devices undergo five basic phenomena viz. charge storage, resistivity modulation, electrothermal behaviour, MOS-capacitance and breakdown limits, which are very important even for a BiMOSFET. Most accurate models will have to incorporate all these effects precisely [12]. The BiMOSFET introduced by IXYS is a reverse conducting switch which is an intermediate between the MOSFET and IGBT. It exhibits the advantages of both these devices viz. fast switching times of MOSFET and power levels of IGBT [13, 14]. This work attempts to simulate an ABM of BiMOSFET by modifying the Hammerstein model in [9] and subsequent verification through simulation studies. The device characteristics are obtained through OrCAD simulations and also verified with an experimental setup.

II. DEVELOPMENT OF ABM OF BIMOSFET

Any analog behavioural macro-modelling starts with the development of a set of integral and differential equations describing the device behaviour followed by the formulation of the electrical equivalent circuit using controlled current and voltage sources.
The BiMOSFET is constructed on a DMOS (Diffusion Mosfet) structure and is hence comprised of a MOSFET and BJT. However, its base is homogeneous and the shorted N+ region in the BiMOSFET decreases the PNP transistor gain. This is also responsible for the appearance of an intrinsic diode across the collector and emitter during turn off of the device [13, 14]. Thus, the equivalent circuit of a BiMOSFET is represented as a Darlington pair of BJT and MOSFET with a turn off diode as shown in Fig. 1. The model is developed by using the MOSFET equations in linear and saturation regions, BJT in the active region and diode in cut off and saturation regions.

The collector current of BJT can be expressed as

\[ I_{c1} = (1 + \beta)I_d \]  

Where, \( \beta \) is the dc current gain of BJT and \( I_d \) are the BJT base current and MOSFET drain current.

The saturation voltage of MOSFET defines the boundary for transition from its linear region.

\[ V_{ds(sat)} = V_{th} - V_{ds} \]  

where, \( V_{th} \) denotes the threshold voltage of the MOSFET with \( V_{ds} > V_{ds(sat)} \) the MOSFET operates in the linear region while \( V_{ds} < V_{ds(sat)} \) make it operate in the saturation region.

Hence, from equations (1) and (2), the MOSFET drain current \( I_d \) is expressed as [9]:

\[ I_d = \begin{cases} k_p \left( (V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \right) & \forall V_{ds} < V_{ds(sat)} \\ k_p (V_{gs} - V_{th})^2 & \forall V_{ds} > V_{ds(sat)} \end{cases} \]  

Thus,

\[ I_{c1} = k_1 \left( (V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \right) \]  

Where \( k_1 \) represents the transconductance and

\[ k_1 = k_p (1 + \beta) \]

If \( V_d \) denotes the voltage drop of BJT across its base and emitter then, the voltage across collector and emitter can be expressed as

\[ V_{ce} = V_d + V_{ds} \]

Thus, the BJТ collector current can be expressed as

\[ I_{c1} = \begin{cases} k_1 \left( (V_{gs} - V_{th})V_{ce} - V_d - \frac{(V_{ce} - V_d)^2}{2} \right) & \forall V_{ce} < V_{gs} + V_d - V_{th} \\ k_1(V_{gs} - V_{th})^2 & \forall V_{ce} > V_{gs} + V_d - V_{th} \end{cases} \]  

The diode current is expressed as,

\[ I_{c2} = I_{ces}e^{(\frac{qV_j}{kT} - 1)} \]

From Fig. 1, \( I_c = I_{c1} - I_{c2} \) where, \( I_{ces} \) denotes the leakage current, \( q \) denotes the charge on electron, \( V_j \) is the diode junction drop, \( T \) is the temperature (25 °C) and \( k \) is the Boltzman constant. The saturation voltage of device can be given by

\[ V_{ce(sat)} = V_{gs} + V_d - V_{th} \]

However, the relationship between \( V_{ce(sat)} \) and \( V_{gs} \) is non-linear necessitating the use of two correction functions \( g_1 \) and \( g_2 \).

\[ g_1 = \frac{V_{ce(sat)}}{g_2} = V_{gs} + V_d - V_{th} \]  

\[ g_2 = \frac{I_{c1(sat)}}{k_2} = k(V_{gs} - V_{th})^2 \]  

\[ g_3 = x_0 + x_1V_{ge} + x_2V_{ge}^2 \]  

\[ g_4 = y_0 + y_1V_{ge} + y_2V_{ge}^2 \]

The values of \( x_0, y_0, x_1, y_1, x_2 \) and \( y_2 \) are determined from the output characteristics of the datasheet through the solution of three simultaneous equations with three unknown variables. Hence, the corrected collector current is expressed as

\[ I_{c1} = g_2k \left( (V_{gs} - V_{th})(V_{ce} - V_d) - \frac{(g_2V_{ce} - V_d)^2}{2} \right) \]

### Table I: Correction function values for corrected collector current

| \( x_0 \) | 1.507 |
| \( y_0 \) | -0.762 |
| \( x_1 \) | -0.131 |
| \( y_1 \) | 0.289 |
| \( x_2 \) | 0.03 |
| \( y_2 \) | -0.006 |

### III. VERIFICATION OF ABM OF IXBF55N300

IXBF55N300 is a 3 kV, 34 A BiMOSFET. The behavioural model of IXBF55N300 is developed using Fig. 1 and replaced in Fig. 2. The terminal characteristics of IXBF55N300 are simulated in OrCAD using the test circuit in Fig. 2. At First the value of \( V_s \) is kept constant and the voltage across the switch, \( V_{ce} \) and current through resistor \( R_s \) represented as \( I_s \) is observed by varying \( V_c \). Subsequently, the value of \( V_s \) is kept constant and by varying \( V_b \), the variation of \( V_{ce} \) and \( V_{gs} \) are observed.
Fig. 2 Test circuit of BiMOSFET

The output characteristics of the BiMOSFET for different $V_g$ values of 3 V, 6 V, 10 V and 15 V are depicted in Fig. 3, while Fig. 4 represents the variation of $V_{ce}$ with $V_g$ at constant values of $V_s$ at 5 V, 10 V, 15 V and 20 V. Fig. 5 depicts the transfer characteristics of the BiMOSFET under test.

Fig. 3 $I_C$ vs $V_s$ characteristic at constant $V_g$

Fig. 4 $V_{ce}$ vs $V_s$ characteristic at constant $V_g$

The test circuit in Fig. 2 has been verified practically with the experimental setup of Fig. 6. The circuit parameters of test circuit is used in Fig. 6.

Table II: Observed values in practical circuit for constant $V_g$ testing

| $V_{ge}$ (V) | $V_s$ (V) | $V_{ce}$ (V) | $I_C$ (mA) |
|--------------|-----------|--------------|------------|
| 4            | 0         | 0            | 0          |
| 5            | 4.75      | 0.22         | 0          |
| 10           | 9.74      | 0.23         | 0          |
| 20           | 19.67     | 0.26         | 0          |
| 6            | 0         | 0            | 0          |
| 5            | 0.08      | 4.91         | 0          |
| 10           | 0.97      | 9.80         | 0          |
| 20           | 1.4       | 19.59        | 0          |
| 10           | 0         | 0            | 0          |
| 5            | 0.08      | 4.88         | 0          |
| 10           | 0.96      | 9.82         | 0          |
| 20           | 1.3       | 19.64        | 0          |
| 15           | 0         | 0            | 0          |
| 5            | 0.07      | 4.95         | 0          |
| 10           | 1.14      | 9.82         | 0          |
| 20           | 1.32      | 19.65        | 0          |

Table III: Observed values in practical circuit for constant $V_s$ testing

| $V_s$(V) | $V_{ge}$ (V) | $V_{ce}$ (V) | $I_C$ (mA) |
|----------|--------------|--------------|------------|
| 0        | 0            | 0.03         | 0          |
| 5        | 0            | 0.03         | 0          |
| 10       | 0            | 0.02         | 0          |
| 15       | 0            | 0.03         | 0          |
| 5        | 0.08        | 4.97         | 0          |
| 10       | 1.48        | 10.02        | 0          |
| 15       | 1.38        | 14.97        | 0          |
| 10       | 0            | 0            | 0          |
| 5        | 0.06        | 4.96         | 0          |
| 10       | 1.29        | 9.97         | 0          |
| 15       | 1.14        | 14.98        | 0          |
| 20       | 0            | 0            | 0          |
| 5        | 0.32        | 4.97         | 0          |
| 10       | 1.32        | 9.96         | 0          |
| 15       | 1.23        | 14.97        | 0          |
| 0        | 0.41        | 0            | 0          |
| 5        | 0.42        | 4.98         | 0          |
| 10       | 1.21        | 9.97         | 0          |
| 15       | 1.13        | 14.99        | 0          |
From figures 3 and 4, it can be inferred that the device has a on state drop in the range of 1 V –1.2 V when conducting currents in the range of 0 mA to 20 mA. From figures 3, 4 and 5, it is observed that the simulated device conducts for values of $V_{ge}> 5.4$ V and $V_{ce}> 1$ V. A similar trend in the practical device behaviour is observed from Tables II and III. The actual device conducts for values of $V_{ge} \geq 5$ V and $V_{ce} \geq 4.23$ V. The on state drop in the circuit is found to be between 1.14 V to 1.18 V practically. The on state drop of the device decreases with increase in gate voltage as observed in fig.4 which is consistent with all power devices. However, at any particular value of $V_g$, it is expected that $I_D$ should vary with variation in device drops to satisfy KVL of the circuit. This deviation is due to the inadequacy of the modelling technique which needs higher tolerances for assured convergence causing error in computed value. From Table III, it can be concluded that the behaviour of the BiMOSFET model is accurate in the saturation and cutoff regions across the simulated, hardware experimental and the manufacturers’ values. However, the model exhibits inaccuracies in the transition from cut-off to saturation i.e. near saturation region.

**IV. CONCLUSION**

The analog behavioural model for a commercial BiMOSFETIXBF55N300 has been developed using Hammerstein model and implemented in OrCAD simulations and in hardware experiments. The terminal characteristics of the BiMOSFET is verified from the simulation results and correlated with the hardware results and the compliance confirmed. The terminal characteristics are simulated in OrCAD and implemented using a basic dc test circuit. The model has been found to exhibit fast convergence and shown reasonable accuracies in the saturation and cut-off regions. However, the model performance at the near saturation region has been observed to be poor due to approximations and reduced model considered. The model is verified by comparing the simulated and tested values with the datasheet.

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**Authors profile**

**Harini V.** received the B.Tech Degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad in 2016. She is currently pursuing her M. Tech degree in Power Electronics from Amrita Vishwa Vidypapeetham, Coimbatore.

**Mahesh Acharya** received the B.E. degree in electrical engineering from Rajasthan University, Jaipur. He also received M.Tech in engineering physics from Homi Bhabha National Institute, RRCAT, Indore. He joined Raja Ramanna Centre for Advanced Technology in 2006. His research interests include pulsed power technology, solid state pulse modulators, RF engineering, power electronics and their applications in particle accelerators. He has authored several papers in various national and international journals.

**Vijayakumari** received the B.E. and M.E. degrees in electrical and electronics engineering from Bharathiar University, Coimbatore, India in 1991 and 2001, respectively, and the Ph.D. degree in electrical engineering from the Anna University in 2014. From 1995 to 1999 she is with Govt. College of Engineering, Coimbatore as a Guest Lecturer and in 2001 joined in Amrita School of Engineering, Coimbatore, Amrita Vishwa Vidyapeetha, as Lecturer and presently serving as an Associate Professor.