An approximate CNTFET 4:2 compressor based on gate diffusion input and dynamic threshold

Mahmood Rafiee,1 Yaqhoub Sadeghi,2 Nabillah Shiri,1,3,5 and Ayoub Sadeghi1
1Department of Electrical Engineering, Shiraz Branch, Islamic Azad University, Shiraz, Iran
2Department of Electrical Engineering, Qatar University, Doha, Qatar
3Email: shiri.nabi@iaushiraz.ac.ir

Introduction: Owing to the ability of error tolerability in applications such as multimedia, machine learning, and digital signal processing (DSP), the concept of digital approximate arithmetic circuits has become a focal concentration area for designers [1]. Significant advances in this area have led to energy efficiency improvements in modern systems on chip. Full adders (FAs) and compressors are the main cores of sophisticated integrated circuits (ICs) such as multipliers and digital filters, and they are well known for a high rate of energy consumption [2]. Therefore, the approximate concept can be used to solve the mentioned defects.

Approximate 4:2 compressors with appropriate compression capability can be mentioned as one of the most vital cells for various applications [3]. Numerous approximate 4:2 compressors have been proposed in the literature [1–7]. Unlike exact compressors (Figure 1a) [8], which ignore one of the inputs, most of the approximate designs in this area have ignored Cin and Cout (Figure 1b,d) as an effective methodology for efficient design [1, 6]. Two well-known 4:2 approximate compressors are shown in Figures 1b [1] and 1c [7], which benefit privileged trade-off between preciseness and circuitry performance. Figure 1b is implemented based on XNOR and NOR logics, while Figure 1c uses the stacking circuit concept and an FA. Although both circuits have a proper error rate, they suffer from high area occupation of the complementary metal-oxide-semiconductor (CMOS) technique, and a high short circuit and dynamic currents at switching time, which causes high power consumption. Therefore, it is expected that by reducing the area for energy saving, a circuit with lower preciseness will be achieved based on majority logic as Figure 1d [6]. In this circuit ignoring one of the inputs, X1, along with the Cin and Cout has caused area reduction while increasing the error rate. Here, a new 4:2 approximate compressor is presented with reliable and solid performance. The gate diffusion input (GDI) technique is used to reduce area and power. The

Here, a new 4:2 approximate compressor is presented by the gate diffusion input (GDI) technique. Although GDI cells suffer from threshold voltage drop, the dynamic threshold approach and carbon nanotube field-effect transistors are merged to overcome the mentioned problem. The proposed cell has full-swing outputs, while its error and power delay product are at low rates. Therefore, low voltage multipliers that are used in image processing can benefit from the proposed compressor.

Proposed circuit: Considering the emerging paradigm as Figure 2a, accessibility of a new reliable 4:2 approximate is feasible. In recent years, to achieve smaller area occupation, the GDI technique has been used instead of the CMOS because as shown in Figure 2b, it is possible to form different gates with only two transistors. So, the high complexity of the previous compressor circuits can be solved. However, in the GDI technique, to solve the non-full-swing outputs, the carbon nanotube field-effect transistor (CNTFET) technology of Figure 2c is used. The CNTFET technology has excellent electrical characteristics, high ballistics transportation, and excellent Vth controllability, along with the high potential of using the body bias dynamic threshold (DT) technique [9]. Using the body bias method drives the threshold voltages of the CNTFET to be changed dynamically by the input voltage at the gate terminal. When Vg = 0 'body' terminal voltages of P-type and N-type transistors are low. Therefore, Vbody-source-P-type = −VD and Vbody-source-N-type = 0 while otherwise, Vbody-source-P-type = 0 and Vbody-source-N-type = VDD [9]. So, the output becomes less influenced by threshold drop and will be full-swing. For instance, in the GDI-based AND gate the P-type transistors are weak for low voltage generation, so the DT-CNTFET technique can overcome this problem, as illustrated in Figure 2d. Here, the output of the AND gate is connected to fan-out. To optimize this effect, the Vth regulation feature in CNTFETs has also been considered. Unlike other techniques, in CNTFET-based GDI cells, pull-up and pull-down network dimensions can be considered identical. The chirality vectors of these transistors can be considered (38,0) so that the values of CNT diameter (D_CNT) and Vth are equal to 2.97 nm and 0.144 V, respectively.

The proposed gate-level circuit of the 4:2 approximate compressor is shown in Figure 3a which operates according to (1) and (2).

\[
\text{Sum} = (X_1 \oplus X_2) + (X_3 \oplus X_4),
\]

\[
\text{Carry} = X_1(X_2 \oplus X_3) + X_3(X_1 \oplus X_4). (2)
\]

Here, the sum producer is similar to [1] which is based on XNOR and OR gates, but the carry generator is different and can be separated into two parts. In the first part, the stacking circuit of Figure 1c is used to produce the essential signals for the second part which is a multiplexer (MUX). Table 1 gives a comparison between the proposed compressor with [1, 6], and [7] circuits. Here, the circuits of [7] and [6] with two and eight errors, respectively, have the smallest and the largest errors of the outputs.

Although the proposed circuit is a combination of [1] and [7] with a new implementation which is using a MUX instead of a FA along with GDI and DT-CNTFET techniques composition, it exhibits 5 errors, which is more than [1] with 4 errors and less than [6] with 7 errors. An important issue with the proposed circuit, unlike other circuits, is the

![Fig. 1 Exact and approximate 4:2 compressors. (a) Conventional structure of compressors. (b) Compressor with XNOR-NOR gates [1]. (c) Compressor with stacking circuit [7]. (d) Compressor with majority logic [6]](image)

![Fig. 2 Used methodologies. (a) An emerging paradigm to attain a new 4:2 approximate compressor. (b) Basic GDI cell with DT connections. (c) Used CNTFET technology. (d) GDI-based AND gate by DT-CNTFET concept](image)
The new aspect of this cell is the decomposition of functionality which is based on the GDI technique and implemented by 18 CNTFETs. Each other's impact. In this regard, the other errors, will be problematic when placed in larger structures such as a multi-

presence of false output with an error distance (ED) value of +2, which will be problematic when placed in larger structures such as a multiplier. In this regard, the other errors, +1 and −1, mutually lessening each other's impact.

The transistor level of the proposed circuit is shown in Figure 3b which is based on the GDI technique and implemented by 18 CNTFETs. The new aspect of this cell is the decomposition of functionality of the

\[ \text{ED}_K = \frac{1}{2^{22}} \sum_{k=1}^{22} |E_D|, \]  

where \( N \) is the bit length of the 4:2 compressor. The error results are shown in Table 5. In applications that deal with the human senses, the difference between the exact and approximate results (i.e. the exact and inexact colours in a pixel) is more important than their relative difference. Hence, the most important parameter in Table 5 is NMED. It is

Table 2. Parameters of the used technology

| Parameter        | Value        | Definition                      |
|------------------|--------------|---------------------------------|
| \( L_{ch} \)     | 32 nm        | Physical channel length         |
| \( L_{eff} \)    | 100 nm       | Mean free path: Intrinsic CNT  |
| \( L_{ext} \)    | 32 nm        | Source side extension regions   |
| \( L_{dd} \)     | 32 nm        | Length of doped CNT drain       |
| \( K_{gate} \)   | 16           | Gate dielectric constant        |
| \( T_{ox} \)     | 4 nm         | Oxide thickness                 |
| \( C_{sub} \)    | 40 pF/m      | Coupling capacitance between channel and substrate |
| \( E_{F} \)      | 0.6 eV       | The Fermi level of the doped S/D tube |
| Pitch            | 5 nm         | The distance between tube centres |
| Chirality vector | (38.0)       | Arrangement of carbon atoms angle |
| Tubes            | 8            | For each transistor             |

Table 3. Circuitry performance of the 4:2 compressors

| Designs       | Power (μW) | Delay (ns) | PDP (fJ) | #Tra. | PDAP      | Year |
|---------------|------------|------------|----------|-------|-----------|------|
| [1]           | 3.1542     | 8.1282     | 25.638   | 26    | 5332.704  | 2015 |
| [2] Design1   | 2.5841     | 4.0198     | 10.387   | 13    | 1080.248  | 2017 |
| [2] Design2   | 3.4913     | 4.1021     | 14.322   | 26    | 2978.976  | 2017 |
| [3]           | 10.651     | 4.0998     | 43.669   | 36    | 12576.67  | 2017 |
| [4]           | 13.055     | 4.1033     | 53.569   | 30    | 12856.56  | 2018 |
| [5]           | 1.2283     | 8.1293     | 14.899   | 16    | 1907.072  | 2019 |
| [6]           | 0.9618     | 12.109     | 11.647   | 12    | 1118.112  | 2019 |
| [7]           | 2.5535     | 4.1067     | 10.487   | 26    | 2181.296  | 2020 |
| Proposed      | 0.6637     | 4.1396     | 2.7475   | 18    | 395.64    | 2021 |

Circuitry performance and error rates: The parameters of Table 2 are used to simulate reference circuits and the proposed cell by HSPICE software, while the technology is 32 nm MOSFET-like single-walled carbon nanotubes (SWCNTs).

Table 3 shows that the proposed cell with 18 transistors has significant power and power delay product (PDP) reduction compared to other designs, specifically based on the CMOS. The closest rival in terms of power to the proposed cell is the [6], while for PDP it is the [7]. The main problem related to [6] is its high delay. Regarding the power and PDP, the proposed cell shows 44.91% and 3.81 × improvements compared to [6] and [7], respectively. Since some circuits have a higher or lower number of transistors compared to the proposed circuit, a figure of merit as PDP-area product (PDAP) which is PDP × (transistors × tubes) can be used. The circuits of [6], [2]-Design2, and [3], respectively have fewer transistors than the proposed circuit, but the proposed circuit has a dramatic reduction of power and PDP. The main point to consider is the considerable difference between the PDAP of the proposed cell with other designs.

More illustrative metrics such as the mean ED (MED), normalized error distance (NED) [10], and normalized mean error distance (NMED) [11] are used to distinguish the accuracy of the circuits more properly (3).

\[ \text{NMED} = \frac{1}{2^{22}(2^{22} - 1)} \sum_{k=1}^{22} |E_D|, \]  

More illustrative metrics such as the mean ED (MED), normalized error distance (NED) [10], and normalized mean error distance (NMED) [11] are used to distinguish the accuracy of the circuits more properly (3).
notable that the compressor designs of [2–4, 7], provide lower NMEDS with high energy consumption and transistor count costs compared to the proposed cell.

To make a trade-off between preciseness and energy efficiency, a practical figure of merit (FoM1) as (4) [6] is used, whose results are shown in Figure 4a.

\[ \text{FoM}_1 = \frac{\text{PDAP}}{(1 - \text{MED})} \]  

also, the power-delay-MED-product (PDMP) is used which is presented as normalized values (NPDM) in Figure 4b. NPDM is calculated as (5) [11].

\[ \text{NPDM} = \frac{\text{PDMP}}{\text{PDMP}_{\text{max}}} \]  

Where \( i \) indicates the desired circuit to be evaluated and max is the circuit with the highest PDMP, which here is [4].

According to the results, the smaller the FoM1 the better the hardware-accuracy trade-off is. In this case, the proposed cell has excellent performance compared to other cells which shows 2.68% better results compared to [2]-Design1. On the other hand, the proposed cell with a higher rate of MED and lower considerable value of PDP compared to [7] still has the best results of NPDM. Although the proposed cell only has a 1.25% improvement compared to [7] the efficiency of the proposed circuit is more visible when it is compared to other cells, specifically those that are not based on CMOS or have lower transistors counts. Here, the performance of the proposed cell is 71.46% and 83.49% better compared to [2]-Design1 and [6] with 13 and 12 transistors, respectively.

Conclusion: To attain energy-efficient digital systems, approximate computing is used as an emerging approach. In this research, a new 4:2 approximate compressor with its significant role in low accuracy applications is presented. The cell is based on the GDI technique. It has 18 transistors and the outputs are full swing. Due to the emerging dynamic threshold (DT) feature and CNTFET technology with the GDI concept, the circuit performance of the presented 4:2 compressor is highly efficient. Also, reduced complexity and significant power reduction with an acceptable error rate (ER) of outputs lead the proposed circuit as a great alternative for previous designs.

© 2021 The Authors. Electronics Letters published by John Wiley & Sons Ltd on behalf of The Institution of Engineering and Technology

This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

Received: 7 January 2021    Accepted: 27 April 2021
doi: 10.1049/ell2.12221

References
1 Momeni, A., et al.: Design and analysis of approximate compressors for multiplication. IEEE Trans. Comput. 64(4), 984–994 (2015)
2 Akbari, O., et al.: Dual-Quality 4:2 compressors for utilizing in dynamic accuracy configurable multipliers. IEEE Trans. Very Large Scale Integr. VLSI Syst. 25(4), 1352–1361 (2017)
3 Venkatachalam, S., Ko, S.: Design of power and area efficient approximate multipliers. IEEE Trans. Very Large Scale Integr. VLSI Syst. 25(5), 1782–1786 (2017)
4 Ha, M., Lee, S.: Multipliers with approximate 4–2 compressors and error recovery modules. IEEE Embedded Syst. Lett. 10(1), 6–9 (2018)
5 Ahmadiannejad, M., Moiayeri, M.H., Sabetzadeh, F.: Energy and area efficient imprecise compressors for approximate multiplication at nanoscale. AEU - Int. J. Electron. Commun. 110, 152859 (2019). https://doi.org/10.1016/j.aeue.2019.152859
6 Sabetzadeh, F., Moiayeri, M.H., Ahmadiannejad, M.: A majority-based imprecise multiplier for ultra-efficient approximate image multiplication. IEEE Trans. Circuits Syst. Regul. Pap. 66(11), 4200–4208 (2019)
7 Strollo, A G M., et al.: Comparison and extension of approximate 4:2 compressors for low-power approximate multipliers. IEEE Trans. Circuits Syst. Regul. Pap. 67(9), 3021–3034 (2020)
8 Chang, C.-H., Gu, J., Zhang, M.: Ultra low-voltage low-power CMOS 4–2 and 5–2 compressors for fast arithmetic circuits. IEEE Trans. Circuits Syst. Regul. Pap. 51(10), 1985–1997 (2004)
9 Assaderaghi, S.F., et al.: Dynamic threshold-voltage MOSFET (DT-MOS) for ultra-low voltage VLSI. IEEE Trans. Electron Devices. 44(3), 414–422 (1997)
10 Liang, J., Han, J., Lombardi, F.: New metrics for the reliability of approximate and probabilistic adders. IEEE Trans. Comput. 62(9), 1760–1771 (2013)
11 Yang, Z., Han, J., Lombardi, F.: Transmission gate-based approximate adders for inexact computing. In: Proceedings of the 2015 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH’15), Boston 8–10 July 2015

Table 4. Error rate percentage comparison for approximate 4:2 compressors

| Designs | Sum Carry | Error rate % | Error rate % |
|---------|-----------|--------------|--------------|
| [1] Design 1 | 3.3125 0.2821 | 0.2535       | 0.2455       |
| [2] Design 2 | 2.8750 0.2188 | 0.2044       | 0.1955       |
| [3] Design 3 | 2.5000 0.1625 | 0.1535       | 0.1455       |
| [4] Design 4 | 2.2500 0.1250 | 0.1165       | 0.1075       |
| [5] Design 5 | 2.0000 0.0875 | 0.0785       | 0.0695       |
| [6] Design 6 | 1.7500 0.0500 | 0.0415       | 0.0325       |
| [7] Proposed | 1.5000 0.0250 | 0.0165       | 0.0075       |

Table 5. Error performance of the 4:2 compressors

| Designs | MED | NED | NMED |
|---------|-----|-----|------|
| [1] | 3.3125 | 0.2821 | 0.2535 |
| [2] Design 1 | 2.8750 | 0.2188 | 0.2044 |
| [3] Design 2 | 2.5000 | 0.1625 | 0.1535 |
| [4] Design 3 | 2.2500 | 0.1250 | 0.1165 |
| [5] Design 4 | 2.0000 | 0.0875 | 0.0785 |
| [6] Design 5 | 1.7500 | 0.0500 | 0.0415 |
| [7] Proposed | 1.5000 | 0.0250 | 0.0165 |

Fig. 4 Comprehensive comparison between the approximate compressors. (a) FoM1 factor. (b) NPDM factor.