Universal logic-in-memory cell enabling all basic Boolean algebra logic

Eunwoo Baek1, Kyoungah Cho2 & Sangsig Kim1,2*  

Among the promising approaches for implementing high-performance computing, reconfigurable logic gates and logic-in-memory (LIM) approaches have been drawing increased research attention. These allow for improved functional scaling of a chip, owing to the improved functionality per unit area. Although numerous studies have been conducted independently for either reconfigurable logic or LIM units, attempts to construct a hybrid structure based on reconfigurable logic and LIM units remain relatively rare. In this study, we merge reconfigurable logic gates and LIM units to achieve a universal logic-in-memory (ULIM) cell for enabling all basic Boolean logic operations and data storage in a single cell. A ULIM cell consisting of silicon memory devices with reconfigurable n- and p-program modes can reconfigure logic operations within the complete set of Boolean logic operations. Moreover, the ULIM cell exhibits memory behaviors for storing output logic values without supply voltages for a certain period, resulting in zero static power consumption. Hence, this study provides a way to realize high-performance electronics by utilizing the silicon devices with a hybrid function of reconfigurable logic and LIM.

Abbreviations
LIM Logic-in-memory  
ULIM Universal logic-in-memory  
CMOS Complementary metal–oxide–semiconductor  
FBRAM Feedback random access memories  
PG Program gate  
CG Control gate  
VIN Input voltage  
LG Gate length  
L GAP Separation between the gates  
LD Drain length  
LS Source length  
T Si Channel thickness  
T OX Oxide thickness  
VPG Programming voltage  
V CG Control gate voltage  
IDS Drain current  
V DS Drain-to-source voltage  
V DD Common drain voltage  
V SS Common source voltage  
V OUT Output voltage  
VA Input voltage A  
VB Input voltage B  
SUP Supply voltages  

The demand for high-performance electronic hardware with high energy efficiency has been increasing, owing to the data explosion caused by the spread of artificial intelligence technologies1. However, conventional von Neumann-based computing architectures inevitably cause data bottlenecks due to the speed gap between the
processor and memory units, and this data bottleneck intensifies as the amount of data increases. Aiming to overcome the limitations of conventional computing, numerous novel computing methods for replacing the von Neumann architecture have been researched in recent years. Among them, reconfigurable logic gates and logic-in-memory (LIM) approaches have been of great interest as promising candidates for next-generation computing.

Unlike complementary metal–oxide–semiconductor (CMOS) logic circuits, reconfigurable logic gates implement various logic operations in the same circuit structure, using elements capable of switching the channel type. This device-level reconfiguration enables the implementation of functionally improved logic gates with fewer resources, thereby providing innovative solutions for performance improvements in traditional CMOS-based hardware facing limitations in dimensional scaling. Whereas reconfigurable logic focuses on diversifying the functions in logic blocks, the scope of LIM research encompasses both logic and memory blocks and aims to merge logic calculations and data storage into one space. This architectural convergence offers the possibility of high-performance hardware platforms suitable for large-capacity data processing, e.g., by increasing the integration density and eliminating the power consumption and latency caused by data movement between the processor and memory units.

Research on reconfigurable logic gates and LIM has mainly been conducted based on emerging memories such as resistive random-access memories (ReRAMs), magnetic RAMs (MRAMs), ferroelectric field-effect-transistors (FeFETs), or two-dimensional (2D) material transistors. Reconfigurable logic gate and LIM concepts have been researched actively and independently from devices to architecture. Nevertheless, attempts to integrate these two concepts have generally been lacking. Thus, there is a need for research on silicon-based technologies capable of merging reconfigurable logic gates and LIM units.

In this study, we merge reconfigurable logic gates and LIM units to construct a universal logic-in-memory (ULIM) cell for performing all basic logic operations and memorizing the output logic in a single cell. Triple-gate feedback random access memories (FBRAMs) are used to construct the ULIM cell, and each device has a p–i–n silicon nanowire structure with three gates for implementing the channel reconfiguration. A positive feedback mechanism, i.e., the operating principle of the triple-gate FBRAM, allows the device to act as a memory element based on the accumulation of charge carriers in the channel. The ULIM cell can perform eight Boolean logic operations (including those of XNOR and XOR logic gates) in one cell by using the channel reconfiguration characteristics of the triple-gate FBRAMs. Moreover, the ULIM cell exhibits excellent memory characteristics; for example, it maintains an output logic value for a certain period under zero supply voltages. We demonstrate the logic reconfiguration and LIM operations of the proposed ULIM cell through a mixed-mode technology computer-aided simulation, demonstrating the potential for realizing high-performance electronics with this novel structure.

Methods

All simulations for a single device and mixed-mode simulations were conducted based on the 2D structure of the triple-gate FBRAM using a commercial device simulator (Synopsys Sentaurus). The physics model for the triple-gate FBRAM included the Fermi–Dirac statistics and Slotboom bandgap narrowing. The recombination mechanism followed Shockley–Dirac statistics and Shockley–Read–Hall recombination, with a doping dependency and Auger recombination. To analyze the silicon region, we used high-field saturation mobility and inversion and accumulation layer mobility models to consider the doping and transverse-field dependencies for the 2D Coulomb impurity scattering. Additionally, we added surface Shockley–Read–Hall recombination to the interface between the silicon and Al2O3 in the triple-gate FBRAM.

Results and Discussions

Design and electrical characteristics of triple-gate feedback random access memory (FBRAM). Figure 1A shows a schematic of the triple-gate FBRAM, which acts as a basic element of the ULIM cell. The triple-gate FBRAM has a p–i–n silicon nanowire structure, in which one control gate (CG) electrode is located between two program gate (PG) electrodes and can switch between n- and p-program modes depending on the polarity of the voltages applied to the PGs. The CG performs as a switching gate for turning the device on or off, and the logic input voltage (V_IN) is input to the CG when extended to the circuit level. The gate length (L_G) is 50 nm for all three gates, and the separation between the gates (L_GAP) is 10 nm. The drain and source lengths (L_D and L_S) are 50 nm, and the channel and oxide thicknesses (T_OX and T_GAP) are 10 nm and 2 nm, respectively. The p+ drain and n+ source regions are heavily doped with $1 \times 10^{20}$ cm$^{-3}$ and the intrinsic channel region is lightly p-type doped with $1 \times 10^{15}$ cm$^{-3}$. The work function of all gate electrodes is set to 4.8 eV. The device and circuits are designed and simulated based on a 2D structure, using a commercial device simulator (Synopsys Sentaurus). The triple-gate FBRAM operates in the n-program (p-program) mode when a positive (negative) programming voltage ($V_{PG}$) is applied to the PG. To differentiate between the devices in accordance with the program mode more clearly in the circuit diagrams, circuit symbols have been devised for the triple-gate FBRAMs operating in the n- and p-program modes, as shown in Fig. 1b. As the two PGs are electrically coupled, the bias line for the PGs is expressed as one line in the circuit symbols. The symbol for an unprogrammed mode with a program voltage ($V_{PC}$) of 0.0 V is illustrated in Supplementary Fig. 1(a).

Figure 1c shows the transfer characteristics of the triple-gate FBRAM as operating in n- and p-program modes when various supply voltages are applied. $V_{PC}$ values of 3.0 V and −3.0 V are applied to operate the device in the n- and p-program modes, respectively. In both program modes, the triple-gate FBRAM exhibits bistable and steep switching characteristics, owing to the operating principle of the positive feedback loop. When sweeping the control gate voltage ($V_{CG}$) in the n-programmed (p-programmed) device from −3.0 V (3.0 V) to 0.0 V, a rapid increase in the drain current ($I_{DS}$) occurs at a specific $V_{CG}$; this is defined as a latch-up voltage, due...
to the generation of a positive feedback loop. At an absolute drain-to-source voltage ($V_{DS}$) value of 1.0 V, the device has extremely low subthreshold swings of $2.66 \times 10^{-3}$ mV/dec for the n-program mode and $4.53 \times 10^{-2}$ mV/dec for the p-program mode at the latch-up voltages. The device switches from the off state to the on state after the latch-up phenomenon and exhibits high on/off current ratios of over $10^{11}$ for the n-program mode and over $10^{10}$ for the p-program mode at $|V_{DS}| = 1.0$ V. When sweeping $V_{CG}$ from 0.0 V to the initial voltage values, $I_{DS}$ decreases rapidly in both program modes at a specific $V_{CG}$; this $V_{CG}$ is referred to as a latch-down voltage. The latch-down phenomenon results from the elimination of the positive feedback loop. Here, the latch-up voltages are different from the latch-down voltages, and this voltage difference is defined as the memory window. When $|V_{DS}|$ increases, the latch-up/down voltages move in the negative (positive) voltage direction in the n-program (p-program) mode. Correspondingly, the memory window width increases, because the change in the latch-down voltage is substantially larger than that in the latch-up voltage. Moreover, the on current increases while the off current before the latch-up does not change, leading to an increase in the on/off current ratio. The n-programmed device exhibits a slight increase of the off current after the latch-down because of the remained carriers inside the device; however, the difference is less than ~10 times which is negligible in further applications or possible to be improved by optimizing the device structure. The width difference in the memory window in the n- and p-program modes originates from the mobility differences between electrons and holes. Figure 1d shows the output characteristics of the triple-gate FBRAM in the n- and p-program modes. When $|V_{CG}| = 3.0$ V, the devices in both the n- and p-program modes remain in the off state while $|V_{DS}|$ increases from 0.0 V to 2.0 V. For $|V_{CG}| = 1.5$ V, the devices show the bistable and steep switching characteristics, owing to the generation and elimination of the positive feedback loop. In contrast, the output characteristics exhibit the behaviors similar to those of a conventional p–i–n diode when $|V_{CG}| = 0.0$ V, because the value of $V_{CG}$ is not sufficient to build the potential barriers and wells for triggering the positive feedback loop

Operating principle of the triple-gate FBRAM. Referring to Fig. 2, we can provide detailed explanations of the device characteristics based on energy band diagrams of the triple-gate FBRAM in the n- and p-program modes. As shown in Fig. 2a, when $V_{CG} = -3.0$ V in the n-program mode with $V_{PG} = 3.0$ V and the drain-to-source voltage ($V_{DS}$) = −1.6 V, potential barriers and wells are built in the energy bands in the form
of p‘–n‘–i–n‘–n‘. Thus, the device is in the off state. n‘ indicates that the corresponding channel region is electrostatically doped as an n-channel, owing to the positive $V_{PG}$. Despite having the same $V_{PG}$, each n‘ region has different energy levels, because the electrons injected from the source region further increase the energy level in the n‘ region adjacent to the source region. Notably, the energy levels of the corresponding n‘ region cannot be higher than those of the source region, owing to the channel-pinning phenomenon. While increasing the $V_{CG}$ from $-3.0 \, V$ to $3.0 \, V$, electrons in the source region flow into the channel region, as the potential barrier height for the electrons becomes lower. The accumulation of electrons inside the channel lowers the potential barrier height for the holes and allows the holes to flow from the drain region into the channel. The accumulation of holes in the channel lowers the potential barrier height for the electrons, and further activates the injection of electrons into the channel. This continuous reduction in the potential barrier height owing to the accumulation of charge carriers results in a positive feedback loop. Owing to this positive feedback loop, the device switches to the on state. To generate the latch-down phenomenon for switching the device to the off state, the elimination of the positive feedback loop is required. This can be accomplished by applying a voltage sufficient to remove the charge carriers stored inside the channel. Because the device maintains the on state before eliminating the positive feedback loop, it has a memory window in the I–V curve. Therefore,
the storage of the charge carriers inside the channel based on the positive feedback loop plays a key role in the functioning of the triple-gate FBRAM as a memory device.

**Universal logic-in-memory (ULIM) cell demonstrating XNOR/XOR logic gate operations.** The triple-gate FBRAM acts as a multifunctional device with memory behaviors and reconfigurable characteristics. Therefore, these multiple functions can be utilized more diversely when extended to the circuit level beyond a single element. In the ULIM cell, two serial connections consisting of two triple-gate FBRAMs are symmetrically connected based on the output node, as shown in Fig. 3. We considered a parasitic capacitance of 1fF when simulating the circuit behaviors.

The circuit diagram before programming each triple-gate FBRAM is shown in Supplementary Fig. 1(b). The value of \( V_{PG} \) is 3.0 V for the n-programmed device, and \(-3.0 \text{ V} \) for the p-programmed device, whereas \( V_{DD} \) and \( V_{SS} \) are maintained at 2.0 V and \(-2.0 \text{ V} \), respectively. The voltages for the input logic values of '1' or '0' are 3.0 or \(-3.0 \text{ V} \), respectively, and apply to the input nodes of A and B (\( V_A \) and \( V_B \)). By altering the combinations of \( V_{PG} \) and \( V_{IN} \), the ULIM cell can perform all basic Boolean logic operations (such as NOT, YES, AND, OR, NAND, NOR, XOR, and XNOR) in a single cell. Herein, the XOR and XNOR logic operations are described as representative examples. As shown in Fig. 3(a,b), the XNOR/XOR logic gate operations are implemented by programming transistor networks located at the top and bottom of the output node and applying input voltages. The other logic gate operations are performed equally under the XNOR/XOR logic gate
DD and top network create a path between can be implemented by programming individual cells. For an ULIM cell array, the combinational logics such as a half-adder and a decoder by simply changing the electrical signals. This logic reconfiguration capability presents the potential of the ULIM our ULIM cells can implement logic operations with fewer devices and can freely reconfigure logic operations of CMOS logic circuits that require over 20 transistors each to implement XNOR and XOR logic gate operations, are needed to eliminate the mismatch. The logic cascading issue remains in our future research. In contrast to cell, which lowers the ability of the ULIM circuit to drive the next circuit. A voltage amplifier or other devices embedded within the channel. However, the voltages of the logic input and output were mismatched in the ULIM cell, which lowers the ability of the ULIM circuit to drive the next circuit. A voltage amplifier or other devices are needed to eliminate the mismatch. The logic cascading issue remains in our future research. In contrast to CMOS logic circuits that require over 20 transistors each to implement XNOR and XOR logic gate operations, our ULIM cells can implement logic operations with fewer devices and can freely reconfigure logic operations by simply changing the electrical signals. This logic reconfiguration capability of the ULIM cell that can be utilized as a function unit in hardware-level programmable arrays with excellent energy efficiency and functionality per chip. For an ULIM cell array, the combinational logics such as a half-adder and a decoder can be implemented by programming individual cells.

In Fig. 3, the $V_{\text{OUT}}$ becomes zero in the middle of the transition from one output logic into another. For the FBRAMs in the ULIM cell (at $V_{\text{DD}} = 2.0 \, \text{V}$ and at $V_{\text{SS}} = -2.0 \, \text{V}$), the generation of the positive feedback loop (at $V_{\text{IN}} = 3.0 \, \text{V}$) stimulates the charging (accumulation) of charge carriers in the channels and the elimination of the positive feedback loop (at $V_{\text{IN}} = -3.0 \, \text{V}$) leads to the discharging (extinction) of the charge carriers from the channels. The accumulation of charge carriers in the channels and the extinction of the charge carriers from the channels create the on and off states of the FBRAMs, respectively. For the FBRAMs, the discharging time is longer than the charging time when $V_{\text{DD}}$ and $V_{\text{SS}}$ are maintained at 2.0 V and $-2.0 \, \text{V}$, and thereby the switching from the on state into the off state takes a longer time than that from the off state into the on state. Consequently, during the XOR and XNOR logic operations, the states of all the FBRAMs in the ULIM cell become the on state in the middle of the transition from one output logic to another. The FBRAMs in the on state have the internal channel resistance and thereby the programming transistor networks located at the top and bottom of the output node have the same resistance when the states of all the FBRAMs in the ULIM cell become the on state. Therefore, the $V_{\text{OUT}}$ becomes zero in the middle of the transition from one output logic into another.

**Logic-in-memory (LIM) operation of the ULIM cell.** Recently, the study of quasi-nonvolatile memories utilizing a device operated by positive feedback loops has been proposed with high speed and long retention time of 100 s under the zero supply voltages. Accordingly, it is crucial to check the memory characteristics as well as the logical operation of the ULIM cell. We can examine the LIM operations of the ULIM cell by repeating the logic and hold operations. The timing diagrams in Fig. 4 show the LIM operations of the ULIM cells for the XNOR and XOR logic gates. The logic calculations are performed by applying the supply voltages ($V_{\text{SUP}}$, $V_{\text{PG}}$, $V_{\text{IN}}$, and $V_{\text{OUT}}$) for 1 ms; these supply voltages have the same voltage values as the aforementioned logic operations. Subsequently, the hold operations for verifying the memory behavior of the ULIM cell are retained for 3 ms by setting $V_{\text{OUT}}$, $V_{\text{PG}}$, $V_{\text{IN}}$, and $V_{\text{SS}}$ to zero. The LIM operations for other logic gates are shown in Supplementary Fig. 3. The cell programmed as an XNOR logic gate calculates the corresponding output logic values of ‘1’, ‘0’, ‘0’, and ‘1’ when the input logic values of ‘00’, ‘01’, ‘10’, and ‘11’ are applied, respectively. After the logic operation, the output voltages are maintained at a level comparable to that of the initial output logic value during the hold operation, thereby manifesting memory behavior. For the XOR logic gate operation, the cell provides the corresponding output logic values of ‘0’, ‘1’, ‘1’, and ‘0’ when the input logic values of ‘00’, ‘01’, ‘10’, and ‘11’ are applied, respectively. The ULIM cell retains the output voltages at levels comparable to those of the initial output logic values during the hold operation, without any external bias. This output logic retention characteristic of the ULIM cell is owing to the excellent charge storage capability of triple-gate FBRAM, i.e., the basic element of the cell. The charge carriers injected during the logic calculations remain within the channel region even under zero external bias conditions, allowing the triple-gate FBRAM to operate as a memory device for a certain period under zero supply voltages. Accordingly, the $V_{\text{OUT}}$ of the ULIM cell can be maintained during the hold operation, owing to the quasi-nonvolatile characteristics of the single device. Because of the logic retention capability from storing the logic states as the value of $V_{\text{OUT}}$, the power consumption of the ULIM cell during the hold operation is zero. Additionally, the short-circuit current of around $5 \times 10^{-14} \, \text{A}$ flows through the circuit on average while transitioning the logic state. Therefore, the dynamic power consumption of ULIM cell is calculated as an average of around 2 pW to calculate each output logic for the input logic.

In Fig. 4, the $V_{\text{OUT}}$ does not come back to zero, owing to the hold operation (at $V_{\text{DD}} = 0.0 \, \text{V}$ and at $V_{\text{SS}} = -0.0 \, \text{V}$) prior to the transition from one output logic to another (see Fig. 3). For the FBRAMs, the switching time from the on state in the hold operation into the off state is shorter than that from the on state (at $V_{\text{DD}} = 2.0 \, \text{V}$ and at
V_{SS} = -2.0 \text{V}) into the off state. And the switching times from the on state in the hold operation into the off state is not longer than that from the off state in the hold operation into the on state. Thus, the case that the states of all the FBRAMs in the ULIM cell become the on state in the middle of the transition from one output logic in the hold operation to other output logic does not happen. Consequently, during the XOR and XNOR logic operations, the programming transistor networks located at the top and bottom of the output node have the different resistance, and the V_{OUT} does not come back to zero.

Logic retention characteristics of the ULIM cell. We can confirm the change in V_{OUT} while increasing the measurement time of the hold operation to 1000 s, to determine the extent to which the output logic of the ULIM cell is retained. Each output logic value of the XNOR and XOR logic gate operations is calculated by applying input logic values with the same voltage conditions as the previous logic operations for 1 ms. After calculating the output logic values, all applied voltages including V_{SUP}, V_{PG}, V_{A}, and V_{B} become zero. As shown in Fig. 5, the ULIM cell maintains half of the initial output logic value even at approximately 1000 s for both the XNOR and XOR logic gate operations, revealing an exceptional logic retention capability. The data for other the logic gates (except for XNOR and XOR) provided in Supplementary Fig. 4 also exhibits similar tendencies. Among the silicon-based LIM studies that are fully compatible with existing CMOS processes, no studies with such quasi-nonvolatile characteristics have been proposed thus far. Also, unlike the conventional memory devices that exhibit their memory state when reading voltage is applied, the ULIM cell represents the calculated logic data directly to the voltage value of V_{OUT} and retains it for a certain period before the new input is applied, and therefore does not require the sensing voltages for reading. Thus, our ULIM cells suggest the possibility of implementing a new LIM architecture for enabling energy-efficient computing while using existing CMOS processes.
Conclusions
Through technology computer-aided design simulations, we demonstrated that the proposed ULIM cell can perform all the basic Boolean logic calculations, as well as memory behavior. The triple-gate FBRAMs constituting the ULIM cell can reconfigure the program mode according to the $V_{PG}$, and this reconfigurable characteristic at the device level enables the ULIM cell to perform any logic operation from a complete set of two-input or one-input Boolean logic operations. By showing eight different basic Boolean logic operations according to various combinations of $V_{PG}$ and $V_{IN}$, we proved that our ULIM cell functions as a universal logic cell with a high logic functionality per cell area. Furthermore, the ULIM cells have memory characteristics that can maintain the output logic values based on the excellent carrier storage capability of the triple-gate FBRAMs. These memory characteristics have been demonstrated under a zero-supply voltage, suggesting that the ULIM cells have great potential as energy-efficient hardware.

Data availability
All data generated or analyzed during this study are included in this published article and its supplementary information files. The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

Received: 4 August 2022; Accepted: 17 November 2022
Published online: 22 November 2022

References
1. Merolla, P. A. et al. A million spiking-neuron integrated circuit with a scalable communication network and interface. Science 345, 668–673. https://doi.org/10.1126/science.1254642 (2014).
2. Le Gallo, M. et al. Mixed-precision in-memory computing. Nat. Electron. 1, 246–253. https://doi.org/10.1038/s41928-018-0054-8 (2018).
3. Sebastian, A., Le Gallo, M., Khaddam-Aljameh, R. & Eleftheriou, E. Memory devices and applications for in-memory computing. Nat. Nanotechnol. 15, 812–812. https://doi.org/10.1038/s41565-020-0756-8 (2020).
4. Lemini, D. & Wong, H. S. P. In-memory computing with resistive switching devices. Nat. Electron. 1, 333–343. https://doi.org/10.1038/s41928-018-0092-2 (2018).
5. Zhou, F. et al. Low-voltage, optoelectronic CH3NH3PbI3–xClx memory with integrated sensing and logic operations. Adv. Funct. Mater. 28, 1800080. https://doi.org/10.1002/adfm.201800080 (2018).
6. Shulaker, M. M. et al. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature 547, 74–78. https://doi.org/10.1038/nature22994 (2017).
7. Lv, C. et al. Phase-change controlled magnetic tunnel junction for multifunctional in-sensor computing. IEEE Electron. Device Lett. 43, 482–485. https://doi.org/10.1109/LED.2022.3148765 (2022).
8. Liang, F. et al. Infrared gesture recognition system based on near-sensor computing. IEEE Electron. Device Lett. 42, 1053–1056. https://doi.org/10.1109/LED.2021.3078157 (2021).
9. Pan, C. et al. Reconfigurable logic and neuromorphic circuits based on electrically tunable two-dimensional heterojunctions. Nat. Electron. 3, 383–390. https://doi.org/10.1038/s41928-020-0433-9 (2020).
10. Wu, P., Reis, D., Hu, X. B. S. & Appenzeller, J. Two-dimensional transistors with reconfigurable polarities for secure circuits. Nat. Electron. 4, 45–53. https://doi.org/10.1038/s41928-020-00511-7 (2021).

Figure 5. Logic retention characteristics of ULIM cell. $V_{OUT}$ versus time during the hold operation for (a) XNOR and (b) XOR logic gate operations.
11. Luo, Z. C. et al. Reconfigurable magnetic logic combined with nonvolatile memory writing. Adv. Mater. 29, 1605027. https://doi.org/10.1002/adma.201605027 (2017).
12. Marega, G. M. et al. Logic-in-memory based on an atomically thin semiconductor. Nature https://doi.org/10.1038/s41586-020-2861-0 (2020).
13. Xiong, X. et al. reconfigurable logic-in-memory and multilingual artificial synapses based on 2D heterostructures. Adv. Funct. Mater. https://doi.org/10.1002/adfm.201909645 (2020).
14. Jeloka, S., Akeab, N. B., Sylvester, D. & Blaauw, D. A 28 nm configurable memory (TCAM/BCAM/SRAM) using push-rule 6t bit cell enabling logic-in-memory. IEEE J. Solid-St. Circ. 51, 1009–1021. https://doi.org/10.1109/Jssc.2016.2515510 (2016).
15. Seshadri, V. et al. Ambit: In-Memory Accelerator for Bulk Bitwise Operations Using Commodity DRAM Technology. In 50th Annual IEEE/Acm International Symposium on Microarchitecture (Micro), 273–287. doi: https://doi.org/10.1145/3123939.3124344 (2017).
16. Mikolajick, T. et al. 20 Years of reconfigurable field-effect transistors: From concepts to future applications. Solid State Electron. https://doi.org/10.1016/j.sse.2021.108036 (2021).
17. Rai, S. et al. Designing efficient circuits based on runtime-reconfigurable field-effect transistors. Ieee T Vlsi Syst 27, 560–572. https://doi.org/10.1109/Tvlsi.2018.2884646 (2019).
18. Weber, W. M. et al. Reconfigurable nanowire electronics: A review. Solid State Electron. 102, 12–24. https://doi.org/10.1016/j.sse.2014.06.010 (2014).
19. Trommer, J., Heinzig, A., Slesazeck, S., Mikolajick, T. & Weber, W. M. Elementary aspects for circuit implementation of reconfigurable nanowire transistors. IEEE Electr. Device Lett. 35, 141–143. https://doi.org/10.1109/LED.2013.2290555 (2014).
20. Orji, N. G. et al. Metrology for the next generation of semiconductor devices. Nat. Electron. 1, 662–662. https://doi.org/10.1038/s41928-018-0167-0 (2018).
21. Shaf, J. The future of computing beyond Moore’s Law. Phil. Trans R Soc. A. https://doi.org/10.1098/rsta.2019.0061 (2020).
22. Wilson, P. R., Ferreira, B., Zhang, J. & DiMarino, C. IEEE ITRW: International technology roadmap for wide-bandgap power semiconductors an overview. IEEE Power Electron. 5, 22–25. https://doi.org/10.1109/MPel.2018.2821938 (2018).
23. Li, S. C. et al. Pinabuto: A Processing-in-Memory Architecture for Bulk Bitwise Operations in Emerging Non-volatile Memories. In In 2016 Acm/Educ/ieee Design Automation Conference (Dac). doi: https://doi.org/10.1145/2807937.2898064 (2016).
24. Santoro, G., Turvani, G. & Graziano, M. New logic-in-memory paradigms: An architectural and technological perspective. Micromachines https://doi.org/10.3390/mi10060368 (2019).
25. Jang, B. C. et al. Memristive logic-in-memory integrated circuits for energy-efficient flexible electronics. Adv. Funct. Mater. https://doi.org/10.1002/adfm.201707425 (2018).
26. Mittal, S. A survey of ReRAM-based architectures for processing-in-memory and neural networks. Mach. Learn. Know. Extr. 1, 75–114. https://doi.org/10.3390/make1010005 (2019).
27. Kang, W., Wang, H. T., Wang, Z. H., Zhang, Y. G. & Zhao, W. S. In-memory processing paradigm for bitwise logic operations in STT-MRAM. IEEE Trans. Magn. https://doi.org/10.1109/Tmag.2017.2703863 (2017).
28. Angizì, S., He, Z. Z., Awad, A. & Fan, D. L. MRIMA: An MRAM-based in-memory accelerator. IEEE Trans. Comput. Aid. Des. Integr. Circ. Syst. 59, 1123–1136. https://doi.org/10.1109/TCad.2019.2907886 (2020).
29. Lee, Y. T. et al. Ferroelectric nonvolatile nanowire memory circuit using a single ZnO nanowire and copolymer top layer. Adv. Mater. 24, 203020–203025. https://doi.org/10.1002/adma.201201051 (2012).
30. Yin, X. Z., Chen, X. M., Niemier, M. & Hu, X. S. Ferroelectric FETs-based nonvolatile logic-in-memory circuits. IEEE Trans. VLSI Syst. 27, 159–172. https://doi.org/10.1109/Tvlsi.2018.2871119 (2019).
31. Breyer, E. T. et al. Compact FeFET circuit building blocks for fast and efficient nonvolatile logic-in-memory. IEEE J. Electron. Devices Soc. 8, 748–756. https://doi.org/10.1109/leds.2020.2987084 (2020).
32. Liu, C. S. et al. Small footprint transistor architecture for photoswitching logic and in situ memory. Nat. Nanotechnol. https://doi.org/10.1038/s41565-019-0462-6 (2019).
33. Padilla, A., Yeung, C. W., Shin, C. W., Hu, C. M. & Liu, T. J. K. Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages. In IEEE International Electron Devices Meeting. 171–174 (2008).
34. Cho, J., Lim, D., Woo, S., Cho, K. & Kim, S. Static random access memory characteristics of single-gated feedback field-effect transistors. IEEE Trans. Electron. Devices 66, 413–419. https://doi.org/10.1109/Ted.2018.2881965 (2019).
35. Sentaurus Device User Guide. Synopsys, Mountain View (2018).
36. Lim, D., Son, J., Cho, K. & Kim, S. Quasi-nonvolatile silicon memory device. Adv. Mater Technol. 5, 2000915 (2020).
37. Bhatia, R. & Gill, S. In IOP Conference Series: Materials Science and Engineering. 012042 (IOP Publishing).

Acknowledgements
This research was supported by a National Research Foundation of Korea (NRF) grant as funded by the Korean government (MSIT; 2020R1A2C304538 and 2022M317A3046571), the Brain Korea 21 Plus Project of 2022 through the NRF funded by the Ministry of Science, ICT & Future Planning, and a Korea University Grant.

Author contributions
Eunwoo Baek, Kyoungah Cho and Sangsig Kim provided conceptualization and methodology. Eunwoo Baek and Kyoungah Cho verified and investigated. Eunwoo Baek analyzed the results and wrote the manuscript; Sangsig Kim supervised the research. All authors edited the manuscript and have given approval to the final version of the manuscript.

Competing interests
The authors declare no competing interests.

Additional information
Supplementary Information The online version contains supplementary material available at https://doi.org/10.1038/s41598-022-24582-y.
Correspondence and requests for materials should be addressed to S.K.
Reprints and permissions information is available at www.nature.com/reprints.
Publisher’s note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.
