The amazing improvement of silicon heterojunction technology: ready for a true mass market launch

Christophe Ballif¹,², Mathieu Boccard¹, Matthieu Despeisse²

¹. Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering (IMT), Photovoltaics and Thin-Film Electronics Laboratory (PV-Lab), Rue de la Maladière 71b, 2000 Neuchâtel, Switzerland
². CSEM, PV-Center, Jaquet-Droz 1, 2002 Neuchâtel, Switzerland

Abstract — Silicon heterojunction solar cells have less manufacturing steps and have allowed achieving higher efficiency than PERC cells. However the market has been slow in taking up the technology. Here we discuss some of the obstacles that have been overcome in the last 10 years and show why the technology is now more ready than ever for a mass market launch. This bases on improvements at the device level reaching 24% with few process steps, on the availability of high-quality low cost n-type c-Si wafers, on improved metallization solutions, and on the availability of production solutions.

Index Terms — silicon, heterojunctions, solar panels.

I. INTRODUCTION

Silicon heterojunction cells (SHJ) base on the simple structure and typical processes described in figure [1]. It aims at taking the best of both the c-Si world (perfect absorber) and of the thin film world (coatings on large area). Panasonic was the first to introduce mass manufacturing. Several obstacles remained for a full mass introduction, in-line the with production costs expectations of current manufacturing. We describe some of them here below, why they have been overcoming, which explains the high number of new entrants in the field of SHJ cell manufacturing.

II. OBSTACLES

A. Material quality

For a long time, many thought it was impossible to get good quality low cost n-type wafer. Hence additional processing such as gettering or hydrogenation would be required. The situation has dramatically changed:

- There has been a strong material improvements over the last 10 years through O control and controlled pulling techniques (also beneficial to p-type).
- Today state-of-the-art n-type c-Si does not require gettering or thermal donor killing, which simplifies the SHJ process.
- At 180 μm thickness such n-type wafers are now typically 5-8% more expensive than p-type. The difference comes in particular from the limited number of pulling with the same crucible to avoid excess impurities.
- Wafer producers can now offer of -1.5c/s/wafer per 10um less thickness.

In consequence of this, high-quality n-type 130-140 μm wafers are equivalent in price or even cheaper than 170-180 μm standard wafers used e.g. for PERC cell production.

B. Metallization and interconnection

The first low temperature pastes had limited conductivity, and simple busbars approach lead to strong Ag paste usage. Things have now changed.

- Strong improvements were made to low T Ag paste. ρ is now down to 5 μΩcm for the best pastes.
- Alternatively, one can substitute Ag by plating Cu. This can also be combined with shingling approaches. Several companies and research institutes demonstrated the validity of such approaches (Fig. 2).
- Solutions with multi-wire are now certified (e.g. Smart-wire) using wire with no Indium coating, reducing to a minimum amount the required Ag.

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Fig. 1. (a) schematics of the process flow for standard SHJ. The PECVD and PVD steps can be performed each in a single tools (e.g. PVD from both sides). (b) schematics of the standard front emitter cell.
• Multi-bus bars approach (5 to 10 bus bars) can also be implemented, with gluing or soldering of the ribbons.

As an example, the smart-wire approach, which consists of typically 18 to 24 wires embedded in a thin encapsulant foil allows a minimum amount of printed Ag paste for the front and rear metallization (25-40 mg per face with possibility to go down to 10 mg). The modules based on this technique passes several times all accreditation tests [2].

In conclusion, certified metallization and interconnection approaches with no expensive materials are now available.

![Smart Wire](image)

Fig. 2. (a) new generation smartwire. (b) 24.15% certified (DA, 225) plated SHJ cells, 4 busbars.

C. Process complexity

The base process has been thought to be difficult to control and it bases on equipments/processes not familiar to the traditional c-Si community. The following points are worth noting:

• From thin film solar, flat panel displays and glass coating, low cost per m² from PECVD (e.g. parallel plate reactor) and PVD have been shown to be possible and compatible with mass manufacturing low costs.
• The technology has the lowest number of process steps, 5-7 depending on tools and processes.
• They are alternative deposition techniques available (hot wire, TCO by plasma assisted evaporation).
• It is easy to control homogeneity with good tool design, and the process are robust again e.g. layer thickness variations.
• They are now > 20 research institutes and (pilot) lines with above 23% efficiency cells (6 inches).

Indeed a well configured set of tool, will lead in the first days cell well over 20% efficiency, and a continuous process improvement will rapidly lead to efficiency >> 22%.

D. Manufacturing equipments and supply chain

More and more sets of equipments are now available for production. The following elements are worth considering.

- The equipement price is going down with competition and will go down with volume.
- Even extra capex of 4-5 MS/100 MW (cell+module) would lead to only 0.8 cts/W extra costs, when depreciated over 6 years which should be the case in a sustainable business (i.e. if capital is available and survival chances are considered longer than 3 years).
- The slightly higher capex should be more than compensated by efficiency gain at cell level and by energy yield gain at system level (next section).
- Based on such arguments, they are now more and more actors in the field and several 50-200 MW lines been put in operation, several producing on a 24/24 basis.
- GW lines have been announced by several manufacturers, some in constructions.

Production yield reported by manufacturers or in pilot are reported at high level. There will be a need of volume, as with all c-Si technologies, to compete with the absolute lowest manufacturing costs at $/W level. At intermediate production level (100-500 MW), energy yield should be considered, still giving space for a market entry.

E. LCOE

They are several intrinsic advantages of the technology

- Low temperature coefficient (-0.2-0.27%/C)
- No PID
- High bifaciality.

These features should ensure the highest energy yield and lowest LCOE, in particular in hot climate region [5]. This is illustrated in Fig.3 where PERT bifacial and SHJ bifacial modules are compared in the EAU [6].

![Field data from PERT bifacial and SHJ smart-wire bifacial modules](image)

Fig. 3. Field data from PERT bifacial and SHJ smart-wire bifacial modules. Source: Courtesy A. Richter, Meyer Burger.
F. Upside potential.

SHJ can evolve towards ultimate products:
- Add one tool to realize back-contacted cells with 5-8% relative efficiency increase. For instance Fig. 4a shows 25 cm² cells made with the Tunnel Junction process [7]. Such device structure holds the world record for c-Si based PV [8].
- Serve as a bottom cell in multijunction devices. SHJ was used in the record 4 terminals III-V on Si (32.8% two junctions, and 35.9% three junctions) [9].
- It serves as an ideal bottom cells for perovskite tandem devices (Fig. 4b), with recent certified efficiency at 25.24% demonstrated [10].

III. FROM LAB TO FAB

A. Typical lab devices.

Table I shows some of the most recent 2x2 screen printed devices made by CSEM/EPFL. Efficiency of 24.1% and 23.76% for n and p-type devices are achieved respectively (data measurements) using the simple process flow of Fig. 1. The results on p-type are certified. For n-type, similar results are obtained on Cz-Wafers. The high current/low voltage is explained by the usage of thick wafer (230 microns).

B. Cells in pilot and production lines

At 6" cell level, several pilot lines reach efficiency in the range of 22.5 to 24%. For instance Fig. 2c shows cells with 24.14% after plating (4 busbars measurements). In its demo line in Germany, Meyer Burger demonstrated runs at average efficiency 23.65% and certified 24% efficiency best cells in the busbarless mode (=not taking into account BB shading and the low finger losses) [4]. With line optimization and further improvement in printing and TCO efficiency close to 24.5-25% should be targeted. Hence lab results can readily be transferred to production tools. Certified modules with 335 and 407W for 60 cells of standard size are achieved, with FF reaching 79.7%, showing the maturity of the technology.

IV. CONCLUSIONS

Over the last 10 years, significant improvements in
- processes compatible with industrial production,
- efficiency achieved on production tool,
- metallization and interconnections
- material quality
- and tools for production
have been made. If, and when, capital is available heterojunction is now one of the most attractive technology. It is hence ready for true mass production launch.

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