Improved quality of InSb-on-insulator microstructures by flash annealing into melt

To cite this article: Heera Menon et al 2021 Nanotechnology 32 165602

View the article online for updates and enhancements.
Improved quality of InSb-on-insulator microstructures by flash annealing into melt

Heera Menon¹,2, Lasse Södergren¹,2, Robin Athle¹,2, Jonas Johansson²,3, Matthew Steer⁴, Iain Thayne⁴ and Mattias Borg¹,2

¹ Electrical and Information Technology, Lund University, Lund, Sweden
² NanoLund, Lund University, Lund, Sweden
³ Solid State Physics, Lund University, Lund, Sweden
⁴ School of Engineering, University of Glasgow, Scotland, United Kingdom

E-mail: heera.menon@eit.lth.se

Received 19 October 2020, revised 3 December 2020
Accepted for publication 23 December 2020
Published 29 January 2021

Abstract
Monolithic integration of III–V semiconductors with Silicon technology has instigated a wide range of new possibilities in the semiconductor industry, such as combination of digital circuits with optical sensing and high-frequency communication. A promising CMOS compatible integration process is rapid melt growth (RMG) that can yield high quality single crystalline material at low cost. This paper represents the study on ultra-thin InSb-on-insulator microstructures integrated on a Si platform by a RMG-like process. We utilize flash lamp annealing (FLA) to melt and recrystallize the InSb material for an ultra-short duration (milliseconds), to reduce the thermal budget necessary for integration with Si technology. We compare the result from FLA to regular rapid thermal annealing (seconds). Recrystallized InSb was characterized using electron back scatter diffraction which indicate a transition from nanocrystalline structure to a crystal structure with grain sizes exceeding 1 μm after the process. We further see a 100× improvement in electrical resistivity by FLA annealed sample when compared to the as-deposited InSb with an average Hall mobility of 3100 cm² V⁻¹ s⁻¹ making this a promising step towards realizing monolithic mid-infrared detectors and quantum devices based on InSb.

Supplementary material for this article is available online

Keywords: Insb, rapid melt growth, flash lamp anneal, Hall mobility, heterointegration

(Some figures may appear in colour only in the online journal)

1. Introduction
Si complementary metal oxide semiconductor devices (CMOS) is the foundation for the semiconductor industry we have today. However, further scaling of Si CMOS is becoming increasingly challenging due to increase in the leakage currents, difficulties in controlling the device electrostatics and short channel effects [1]. This as well as the emergence of the Internet-of-Things has pushed research to find ways to enhance the functionality of the electronic chips, such as adding optical sensors, quantum devices, wireless communication and integrated memories [2, 3] on top of the digital circuits. Many of these devices can be better realized in other materials than Si, in particular III–V semiconductors with direct bandgap, high electron mobility and strong spin–orbit coupling are excellent candidates for heterointegration [4, 5]. It is however critical that these materials can be integrated with high-quality, low thermal budget and in a compatible process, to be viable for large scale use. Several techniques for integrating III–V on Si have been reported, such as direct epitaxial growth using thick buffer layer [6].
wafer bonding [7, 8] aspect ratio trapping (ART) [9], nanowire epitaxy and template assisted selective epitaxy (TASE) [10, 11]. While especially ART and TASE are CMOS-compatible processes that give high quality material, the lateral size of the integrated structures is limited to a few microns at most.

Rapid melt growth (RMG) is a technique to integrate III–V’s on Si to obtain high quality single crystalline structures, tens to hundreds of micrometers in lateral dimension while down to tens of nanometer in thickness [12–14]. In RMG a low-quality film is deposited on an insulator and with only a small contact area to the crystalline substrate. The film is structured and contained within a dielectric capping layer (crucible). After which it is annealed until melting. Upon cooling the melt crystallizes rapidly starting from the contact point of the crystalline substrate, leading to a single crystalline film of high quality. RMG of Ge [15] material has become a well-established process with successful device implementations such as FinFETs [16, 17] and photodetectors [18]. There are also some reports of RMG of common III–V semiconductors like InAs [19], GaSb [20], and GaAs [21], with very promising material characteristics.

InSb has the smallest direct bandgap (0.17 eV) and highest electron mobility (77 000 cm² V⁻¹ s⁻¹) among the III–V semiconductors. InSb has attracted growing attention in the field of integrated mid-infrared optoelectronics [22] and for topological quantum devices [23]. However, heterointegration of InSb [24–26] with any common semiconductor substrate is challenging due to its relatively large lattice parameter, a lattice mismatch of 19% to Si, resulting in a higher density of defects when integrated by common epitaxial techniques. InSb high electron mobility transistors [27] and monolithic InSb photodetectors [28] integrated on Si were realized through the use of thick buffer layers. Our aim in this work is to explore the possibility of integrating InSb microstructures on Si, through the RMG technique, despite the huge 19% lattice mismatch. We expect a high crystal quality if the nucleation of InSb is limited to a single nucleation event in a patterned Si seed area that confines the defects generated due to the lattice-mismatch [29]. Liquid phase epitaxy of InSb quantum dots on GaAs results in roughly one nucleation event per 100 × 100 nm² area, indicating that it is feasible to achieve the same here [30]. Thus in this paper we present a study on the integration of ultra-thin InSb-on-insulator microstructures on Si substrates using RMG and specifically compare the effect of flash lamp annealing (FLA) versus regular rapid thermal annealing (RTA). Although epitaxial growth of InSb was interfered by the presence of an interfacial layer our results indicate the transformation of amorphous nanocrystalline material to polycrystalline InSb with a few large grains upon annealing, with 10 to 100× improvement in the device resistivity for varying annealing conditions. The process was designed to have a low thermal budget and to be compatible with InSb integration on top of already processed CMOS circuits.

2. Experimental procedure

Sample fabrication started with 3 inch Si (100) wafers, onto which a 40 nm silicon nitride (Si₃N₄) layer was deposited by inductively coupled plasma plasma-enhanced chemical vapor deposition (ICP PECVD) (MicroSystems MS200) at 300 °C using SiH₄ and N₂ precursors. Openings in the Si₃N₄ layer 50 µm long and 70 nm wide were formed using electron beam lithography (EBL) (Raith Voyager) and inductively-coupled reactive ion etching (ICP-RIE) (PlasmaTherm Apex SLR) using CHF₃:N₂ 15:85 sccm at 10 mTorr. These openings were intended to enable contact points between the Si and InSb, which we denote as seed areas. A V-groove were formed in the Si in the seed areas by first removing the native oxide layer with a quick buffered oxide etch (BOE) followed by etch in TMAH (25%) at 60 °C. Amorphous InSb (1:1), 30 nm thick, was then deposited using molecular beam epitaxy (MBE) with the substrate held at a temperature of 300 °C at an estimated growth rate of 0.1 ML/s (0.324 Å s⁻¹), based on single crystal growth rates obtained from RHEED oscillations of InAs on InAs substrates. Just prior to deposition the substrate was held at 850 °C for 1 h in the MBE chamber with the aim to evaporate any native oxide in the Si seed area. As InSb is sensitive to the hydroxide-based chemicals used in common lithography processes, the InSb film was covered with a 3 nm Al₂O₃ layer by atomic layer deposition (Cambridge Nanotech) at 200 °C to protect it from the subsequent processing. The InSb layer was patterned into structures 10 µm long with different widths (400 nm, 600 nm, 800 nm, 1000 nm and 1200 nm) using EBL and ICP-RIE (PlasmaTherm Apex SLR) using CH₄/H₂/Ar (6:5:6.5:1) chemistry. The structures were defined so as to overlap the seed area in their central part, resulting in a seed area defined by the intersecting area between the trench and the InSb structure, as is illustrated in figures 1(a) and (b). Structures wider than 400 nm were designed with a narrower region around the trench to limit the seed area width to 400 nm. After resist removal and thorough cleaning the structures were capped by 10 nm additional Al₂O₃ followed by a 950 nm Si₃N₄ layer deposited using PECVD. A schematic of the final sample structure is presented in figure 1(c).

To melt and recrystallize the InSb, the samples were annealed above the melting temperature of InSb (527 °C) using two techniques: RTA (UniTemp RTP) and FLA (Rovak FLA 50/100 AS). The RTA treated sample was annealed to a peak temperature of 530 °C for 1 s, whereas the FLA-treated samples was preheated to a temperature in the range 236 °C–413 °C after which it was exposed to a broad spectrum light flash with a duration of nominally 1.5 ms, and pulse energy of 19.5 J cm⁻². The temperature of the RTA system was calibrated by use of the well-defined eutectic temperature of the Si/Au and Si/Al system and any offsets in the measured temperature were taken into account [31]. Temperature measurements in FLA is non-trivial as the flash only heats up the front side of the sample [32–34]. Instead the temperature profile across the sample depth was modeled by
finite-element simulation estimating the peak temperature in this process as reaching 492 °C–700 °C, depending on the chosen preheating temperature (figure 2). The assumptions of the model were verified by pyrometer measurements of the backside temperature (see supporting information available online at stacks.iop.org/NANO/32/165602/mmedia)).

After annealing, the Si₃N₄ capping layer was removed using RIE (Trion Sirus T2 Plus) with SF₆ and O₂ chemistry and the crystallinity and crystal orientation were characterized using scanning electron microscopy (SEM) (Zeiss Gemini SEM 500) equipped with an electron backscattering diffraction (EBSD) detector (Oxford Symmetry).

For electrical characterization, contacts to InSb structures were fabricated by a lift-off process using EBL of the contact patterns followed by passivation in (NH₄)₂S (20%) and H₂O 1:40 for 90 s at 40 °C. Contact metal with of 20 nm Ni and 120 nm Au was evaporated followed by a lift-off of the resist.

3. Results and discussions

Figure 3 illustrates the first pronounced difference between the RTA and the FLA annealed samples. When heating above the melting temperature using RTA it was observed that large voids are formed in the InSb structures (figure 3(c)), which could indicate loss of material from the crucible during the melting process. Contrary, the samples annealed using FLA had intact InSb structures with no voids visible in the bulk of the structures. On the edges, there are still some loss of material. We attribute the formation of voids to loss of In and Sb by diffusion through the dielectric crucible during the time that the InSb is held in a liquid state above the melting temperature. The markedly smaller degree of material loss for the samples processed by FLA can be explained by the nearly 1000 times shorter time that the sample is held above the melting temperature. Despite that In and Sb diffusion through stoichiometric Si-based dielectrics such as SiO₂ and Si₃N₄ should be negligible at these temperatures there is evidence of enhanced In diffusion if the films contain hydrogen or have low density [35]. Indeed, our Si₃N₄ films are deposited by ICP-CVD at 300 °C, and despite efforts to optimize its stoichiometry they likely contain >10% hydrogen, based on their relatively high etch rate in BOE 1:10 of 2.8 nm min⁻¹ and density of 2.6 g cm⁻³ [36]. It is thus plausible that given sufficient time In and Sb could penetrate the crucible in their liquid state. The loss of material at the edges is attributed to a worse quality of the dielectric capping layer at the step edge, as indicated by an enhanced BOE etch rate in these regions. Thus, having excellent dielectric layer quality is essential and
3.1. Structural characterization

To study the crystallinity and the crystal orientation of the annealed InSb structures, EBSD measurements were performed. The EBSD reconstructed maps of the FLA processed samples with different preheating temperatures are shown in figure 4. Figure 4(a) presents the SEM image of the 354 °C preheated sample. The colors in the EBSD maps of figures 4(b)–(f) and (i) represent a specific InSb zinc-blende crystal orientation, given by the legend in figure 4(g). From the data in these maps one can thus extract the InSb grain orientation, shape, and size. The EBSD measurement does not discriminate between InSb and the Si seed area which has [001] orientation, visible as a red vertical line on the left side of the maps. Figure 4(b) displays the sample annealed with a preheating temperature of 236 °C (T_{peak} = 492 °C). The EBSD map exhibits single pixel grains (<50 nm), indicating no observable crystallinity at the current measurement resolution. This sample thus appears to have the same amorphous nature as the InSb film after MBE deposition.

In contrast, the samples annealed with the preheating temperature ranging from 265 °C to 413 °C (T_{peak} = 527 °C–709 °C) (figures 4(c)–(f)) consist of only a few large grains with grain size mostly exceeding 1 μm. It is thus evident that heating above the melting temperature results in recrystallization. Figure 4(h) displays the EBSD orientation map (z direction) of an InSb structure on a sample annealed to 530 °C using RTA. Similar to the FLA process, the RTA samples also resulted in grains exceeding 1 μm in size.

Although we expected crystallization to originate from the Si seed area and result in a single epitaxial structure [13, 14], this is not what we observe. The Si seed is visible as a red line at the left edge of the EBSD maps corresponding to Si (100) orientation. We do not see any relation between this and the rest of the InSb material in any of the measured structures, indicating that crystallization has not been preferential at this interface. Indeed, we observe by high-resolution TEM the presence of an unintentional interfacial layer that isolates the InSb from the Si substrate (see supplementary information). Having had no preferential nucleation site, the InSb melt has instead nucleated at random (unseeded) elsewhere in the crucible. Future experiments will have to ensure to avoid the interfacial layer to realize epitaxial InSb. Here we use this opportunity to explore the nucleation properties on the inside of the crucible that must be controlled to enable epitaxy later on.

In order to analyze the EBSD measurement more thoroughly the measurement area was reconstructed using a spline filter and the grain size, defined as the longest diameter of a grain, and the number of grains in each sample area was calculated. Figure 5 shows the grain density for varying FLA

![Figure 4](image-url)

**Figure 4.** (a) SEM image of the FLA annealed sample corresponding to EBSD Z map(e). (b)–(f) EBSD Z orientation map of 1.5 ms 19.5 J cm⁻² FLA annealed samples with preheating temperatures (b) 236 °C (c) 265 °C (d) 295 °C (e) 354 °C (f) 413 °C (g) color code representation of orientation of crystal in EBSD map (h) SEM image of 530 °C RTA annealed sample (i) EBSD Z orientation map of RTA annealed structure.
preheating temperatures. Overall, we can see a decline in the number of grains per area (figure 5(a)) with rise in preheating temperature. As the preheating temperature increases, the peak temperature achieved by the flash also increases. The overall declining trend of grain density may be due to fewer nuclei and an increase in growth time with increase in preheating temperature as shown in figure 2.

Figures 5(b) and (c) displays the distribution of grain diameters of FLA annealed samples with $T_{\text{peak}} = 709 \degree C$ and RTA annealed samples, respectively. This particular FLA sample was chosen because it had the lowest grain density among the FLA samples. It was observed that grain size ranging from 1 to 4 $\mu m$ was obtained through both the processes. The average grain diameter for FLA and RTA annealed samples were 1.5 $\mu m$ and 1.6 $\mu m$, respectively. The similar grain sizes indicate the possibility to achieve the same conditions for unseeded nucleation both in FLA and RTA. With the FLA, the temperature spike leading to melting and return to a much lower equilibrium temperature occurs in the millisecond time frame, after which, a much slower gradual reduction in temperature occurs similar to regular RTA. We hypothesize that unseeded nucleation on the inside of the crucible occurs in this slower cooling phase, which can explain the observed grain size similarity between FLA samples with highest $T_{\text{pre}}$ and the RTA sample.

### 3.2. Growth modeling

To verify the hypothesis given above, and to aid the understanding of the unseeded nucleation and growth process we model the homogeneous nucleation rate, heterogeneous nucleation rate on the crucible wall and the expected melt growth rate of InSb using the thermodynamic model introduced by Liu et al [37]. After annealing, when the liquid InSb is cooled, InSb transforms into its solid phase by one of the following process: by heterogeneous nucleation on the inner walls of the crucible (Al$_2$O$_3$ or Si$_3$N$_4$) or by homogeneous nucleation within the InSb liquid itself. Epitaxial nucleation on the crystalline seed (Si surface) is not considered here because of the interfacial layer in the seed area.

The homogeneous nucleation rate [37] is given by:

$$I_{\text{hom}} = \frac{1}{V_A} v_0 4\pi (r^*)^2 \frac{N}{n^*} \exp \left( - \frac{\Delta G_{M}^*}{kT} \right) \left( - \frac{\Delta G^*}{3\pi kT} \right)^\frac{1}{2} \times \exp \left( - \frac{\Delta G^*}{kT} \right).$$

where $r^*$ is the critical radius of the nucleus, $N$ is the total number of atoms in the liquid, $n^*$ is the number of critical sized nucleus for homogeneous nucleation, $\Delta G_{M}^*$ is the activation free energy of an atom jumping across liquid nucleus interface, $\Delta G^*$ is the critical free energy change for homogeneous nucleation.

Similarly, the heterogeneous nucleation rate is given by:

$$I_{\text{het}} = \frac{1}{V_A} v_0 2\pi (r^*)^2 \frac{V_A}{n_{\text{het}}} \left( \frac{\Delta G_{\text{het}}^*}{3\pi kT} \right)^\frac{1}{2} (1 - \cos \theta) \times \exp \left( - \frac{\Delta G_{\text{het}}^*}{kT} \right) \exp \left( - \frac{\Delta G_{M}^*}{kT} \right).$$

where, $n_{\text{het}}$ and $\Delta G_{\text{het}}^*$ are the number of atoms in a critical sized nucleus and the free energy change for the heterogeneous nucleation which is given by the equation:

$$\Delta G_{\text{het}}^* = \Delta G^* S(\theta),$$

$$n_{\text{het}} = n^* S(\theta)$$

where $S(\theta) = \frac{1}{2} (2 + \cos \theta)(1 - \cos \theta)^2$ and $\theta$ is the contact angle between a spherical cap-shaped nuclei and the crucible wall [37].

After nucleation of an initial crystallite template, atoms can either get attached to the template from the liquid phase or the atoms in solid phase may dissolve in the liquid. The difference of this forward and backward rate gives the growth rate [37]:

$$U = a_0 v_0 \exp \left( - \frac{\Delta G_{M}^*}{kT} \right) \left[ 1 - \exp \left( - \frac{\Delta g_0}{kT} \right) \right].$$

where $a_0$ is the interatomic spacing, $v_0$ is the vibrational frequency of an atom $\Delta G_{M}^*$ is the kinetic barrier of an atom to jump across the liquid crystal interface, $\Delta g_0$ is the energy
change per atom. All input values are available in the supplementary information table 2.

Simulation results of growth velocity and the nucleation rates are given in figure 6 for an InSb structure 30 nm thick, 1 μm wide and 5 μm long, corresponding to one side of the fabricated InSb structures in this work. It is evident that as the temperature decreases below the melting point, homogeneous nucleation does not become important until around 255 °C, while heterogeneous nucleation becomes important around 343 °C. The rate of InSb crystal growth from the super-cooled melt increases below the melting temperature at 527 °C and reaches a peak of near 30 m s⁻¹ at 375 °C. Because the unseeded nucleation rates do not become appreciable until below 343 °C, in the current case in which epitaxial nucleation at the Si seed area is not possible, it is likely that neither nucleation or growth occur until the temperature of the super-cooled melt drops below roughly 340 °C and a first nucleation event on the inner walls becomes probable. This can explain the similar grain sizes observed in both RTA and FLA; although the temperature in FLA cools much faster above and close to the InSb melting temperature, the temperature quickly equilibrates as seen in figure 2. For the samples with the highest $T_{pre}$ the cooling rates are thus similar to RTA around 343 °C leading to similar nucleation and growth rates. To obtain an epitaxial single crystal, it is important that the continued growth after epitaxial nucleation should not be interrupted by unseeded nucleation. We thus observe that there is a process window between approximately 343 °C and 527 °C where both homogeneous and heterogeneous nucleation are insignificant allowing for epitaxial growth to dominate. If the goal is to achieve a single crystal, it is thus vital that the time within this temperature window is sufficient to grow the crystal throughout the whole structure. As the growth rate is very high (m s⁻¹) in this window we estimate that both RTA with seconds of cooling time and FLA with millisecond cooling time should be sufficient to at least grow InSb crystals hundreds of micron in size, as was previously demonstrated for Ge [15, 38]. The modeling presented here thus gives confidence that it will be possible to realize epitaxial single crystalline InSb structures sufficiently large to realize large quantum wire networks (100 × 100 μm²) and large area InSb photodetectors (10 × 10 μm²).

3.3. Electrical characterization

Characterization of the electrical resistivity of the InSb structures was carried out by three different techniques: transition line measurements, four probe measurements and Van der Pauw measurements. Importantly, the resistivity values extracted from all three measurement techniques correlate well with each other. It was also observed that the resistivity values were the same regardless of the width of the structure ($p = 0.001$).

Figure 7 shows the comparison of resistivity of as-deposited and annealed InSb structures. The as-deposited InSb exhibits high resistivity with an average of 3.2 $\Omega \cdot cm$ with small device to device variation. The RTA processed InSb exhibit a much larger variation between devices, with mean resistivity of 1.2 $\Omega \cdot cm$. However, the devices which were FLA processed exhibit a reduced resistance when compared to the RTA processed devices. There is a radical shift in the average resistivity between samples with $T_{pre} = 236$ °C and 265 °C which is yet another indication of the effect of achieving full melting and recrystallization of the InSb material. It is also observed that the resistivity of the sample annealed closest above the melting point ($T_{pre} = 265$ °C) has the lowest resistivity with an average of 40 m$\Omega \cdot cm$ when compared to the $T_{pre} = 295$ °C and $T_{pre} = 354$ °C samples with average resistivity of 0.15 $\Omega \cdot cm$ and 0.12 $\Omega \cdot cm$, respectively. Remarkably, despite being polycrystalline material the average resistivity of the $T_{pre} = 265$ °C sample is similar to the resistivity of single-crystalline InSb nanowires grown by vapor–liquid–solid growth with resistivity ranging 45–93 m$\Omega \cdot cm$ [39]. Although
the observed grain sizes are similar regardless of using RTA or FLA for annealing, the much higher resistivity and larger device-to-device variation resulting from RTA could be due to the high density of voids appearing after the RTA process. Other contributing factors could be surface non-stoichiometry and surface roughness, which is expected to impact the electron transport in these thin InSb layers.

The carrier Hall mobility was measured on Hall cross devices from the FLA samples with $T_{\text{pre}} = 265$ °C and 354 °C, and the RTA annealed sample using a Hall measurement set up with variable magnetic field (max 1 T) at room temperature. Three devices from the $T_{\text{pre}} = 265$ °C FLA sample were measured giving an average electron mobility $\mu_e = 3143 \, \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ with an average carrier concentration of $1.89 \times 10^{17} \, \text{cm}^{-3}$, whereas two devices in the $T_{\text{pre}} = 354$ °C FLA sample gave $\mu_e = 57$ and $139 \, \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ with an average carrier concentration of $7.01 \times 10^{17} \, \text{cm}^{-3}$. The mobility of a device on the RTA annealed sample was similar, $63 \, \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ with a lower carrier concentration of $6.5 \times 10^{16} \, \text{cm}^{-3}$. The reason for the much higher mobility for the sample with $T_{\text{pre}} = 265$ °C (and $T_{\text{peak}}$ just above melting) is yet unclear, but we speculate that the much shorter time in the melted state ($T < 343$ °C after ~5 ms, see figure 2) for this sample maintains a better InSb surface that otherwise could limit the electron mobility in these thin devices for which significant electron confinement is expected in InSb [40]. See supplementary information for raw data of Hall measurement on $T_{\text{pre}} = 265$ °C FLA sample and a SEM image of a Hall cross device.

4. Conclusion

In this paper we present the integration of ultra-thin InSb on insulator microstructures on to Si by a RMG process using FLA and RTA techniques. EBSD and electrical measurements indicate the transition from amorphous InSb to crystalline structure upon annealing above the melting temperature, with average grain size above 1 μm. We find that FLA provides significantly less loss of material during the RMG process, and markedly lower resistivity and higher electron mobility compared to RTA. The FLA sample annealed closest above the InSb melting point has an average resistivity of 40 mΩcm and an average electron mobility of $3143 \, \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$. The results of this study are thus promising for realizing high-quality InSb-on-insulator devices on Si for optoelectronic and quantum applications using RMG.

Acknowledgments

This work is supported by Swedish Foundation for Strategic Research, Nano Lund, Craford Foundation and Royal Physiographic Society of Lund. The authors would like to thank Dr C J D Hetherington for HRTEM analysis.

ORCID iDs

Heera Menon @ https://orcid.org/0000-0002-7365-1256
Jonas Johansson @ https://orcid.org/0000-0002-2730-7550
Mattias Borg @ https://orcid.org/0000-0003-1217-369X

References

[1] Frank D J et al 2001 Device scaling limits of Si MOSFETs and their application dependencies Proc. IEEE 89 259–87
[2] Persson K M et al 2020 Cross-point arrays with low-power ITO-HfO2 resistive memory cells integrated on vertical III–V nanowires Adv. Electron. Mater. 6 2–7
[3] Kopp C et al 2011 Silicon photonic circuits: on-CMOS integration, fiber optical coupling, and packaging IEEE J. Sel. Top. Quantum Electron. 17 498–509
[4] Del Alamo J A 2011 Nanometre-scale electronics with III–V compound semiconductors Nature 479 317–23
[5] Kazior T E 2014 Beyond Cmos: heterogeneous integration of III–V devices, RF MEMS and other dissimilar materials/devices with Si CMOS to create intelligent Microsystems Phil. Trans. R Soc. A 372 20130105
[6] Chen S et al 2014 InAs/GaAs quantum-dot superluminescent light-emitting diode monolithically grown on a Si substrate ACS Photonics 1 638–42
[7] Daix N et al 2016 Towards large size substrates for III–V co-integration made by direct wafer bonding on APL Mater. 2 086104
[8] Derendorf K et al 2013 Fabrication of GaNP/GaAs/Si solar cells by surface activated direct wafer bonding IEEE J. Photovoltaics 3 1423–8
[9] Waldron N et al 2016 Replacement fin processing for III–V on Si: from FinFets to nanowires Solid State Electron 115 81–91
[10] Schmid H et al 2017 Monolithic integration of multiple III–V semiconductors on Si 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3) 2018 (Piscataway, NJ: IEEE) pp 1–3
[11] Borg M et al 2015 Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si J. Appl. Phys. 117 144303
[12] Liu Z et al 2018 Research progress of Ge on insulator grown by rapid melt growth J. Semicond. 39 061005
[13] Liu Y, Deal M D and Plummer J D 2004 High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates Appl. Phys. Lett. 84 2563–5
[14] Toko K et al 2011 Single-crystalline (100) Ge networks on insulators by rapid-melting growth along hexagonal mesh-pattern Appl. Phys. Lett. 98 0–1
[15] Hashimoto T et al 1882 Fabrication of local Ge-on-insulator structures by lateral liquid-phase epitaxy: effect of controlling interface energy between Ge and insulators on lateral epitaxial growth Appl. Phys. Express 6 066502
[16] Feng J et al 2007 P-channel germanium FinFET based on rapid melt growth IEEE Electron Device Lett. 28 637–9
[17] Feng J et al 2008 High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al2O3 gate dielectric and self-aligned NiGe contacts IEEE Electron Device Lett. 29 805–7
[18] Assefa S et al 2010 CMOS-integrated high-speed MSM germanium waveguide photodetector Opt. Express 18 4986
[19] Yuan Z et al 2013 Optimal device architecture and heterointegration scheme for III–V CMOS 2013 Symposium on VLSI Technology pp T54–5
[20] Chen Y H et al 2018 GaSb MSM photodetectors on Si waveguides by rapid melt growth method IEEE Photonics Technol. Lett. 30 1013–5
[21] Chen S L, Griffin P B and Plummer J D 2010 Single-crystal GaAs and GaSb on insulator on bulk Si substrates based on rapid melt growth IEEE Electron Device Lett. **31** 597–9

[22] Chen H et al 2009 Infrared detection using an InSb nanowire 2009 IEEE Nanotechnol Mater Devices Conf. NMDC 2009 pp 212–6

[23] Yang Z et al 2020 Spin transport in ferromagnet-InSb nanowire quantum devices *Nano Lett.* **20** 3232–9

[24] Chyi J I et al 1989 Molecular beam epitaxial growth and characterization of InSb on Si *Appl. Phys. Lett.* **54** 1016–8

[25] Jia B W et al 2018 Growth and characterization of InSb on (1 0 0) Si for mid-infrared application *Appl. Surf. Sci.* **440** 939–45

[26] Mori M et al 2010 InSb films grown on the V-grooved Si(001) substrate with InSb bilayer *Phys. Proc.* **3** 1335–9

[27] Turitsyna E G and Webb S 2005 Simple design of FBG-based VSB filters for ultra-dense WDM transmission *Electron. Lett.* **41** 40–1

[28] Jia B W et al 2018 Monolithic integration of InSb photodetector on silicon for mid-infrared silicon photonics *ACS Photonics* **5** 1512–20

[29] Borg M et al 2014 Vertical III–V nanowire device integration on Si(100) *Nano Lett.* **14** 1914–20

[30] Krier A, Huang X L and Hammiche A 2001 Liquid phase epitaxial growth and morphology of InSb quantum dots *J. Phys. D: Appl. Phys.* **34** 874–8

[31] Diagram E 1983 The Au–Si (gold–silicon) system *Bulletin of Alloy Phase Diagrams* **4** 190–8

[32] Rebohle L et al 2018 Determination of the thermal cycle during flash lamp annealing without a direct temperature measurement *Int. J. Heat Mass Transfer* **126** 1–8

[33] Prucnal S, Rebohle L and Skorupa W 2017 Doping by flash lamp annealing *Mater. Sci. Semicond. Process.* **62** 115–27

[34] Rebohle L, Prucnal S and Skorupa W 2016 A review of thermal processing in the subsecond range: semiconductors and beyond *Semicond. Sci. Technol.* **31** 103001

[35] Chang R et al 2009 Diffusion of indium implanted in silicon oxides *Japan. J. Appl. Phys.* **48** 056501

[36] Parsons G N, Souk J H and Batey J 1991 Low hydrogen content stoichiometric silicon nitride films deposited by plasma-enhanced chemical vapor deposition *J. Appl. Phys.* **70** 1553–60

[37] Liu Y, Deal M D and Plummer J D 2005 Rapid melt growth of germanium crystals with self-aligned microcrucibles on Si substrates *J. Electrochem. Soc.* **152** G688

[38] Littlejohns C G et al 2015 Next generation device grade silicon-germanium on insulator *Sci. Rep.* **5** 8288

[39] Thelander C et al 2012 Electrical properties of InAs1−xSbx and InSb nanowires grown by molecular beam epitaxy *Appl. Phys. Lett.* **100** 232105

[40] Nguyen C T et al 2012 Electron distribution and scattering in InAs films on low-k flexible substrates *Appl. Phys. Lett.* **100** 1–5