A Novel Capacitor Voltage Balancing Method for MMCs with Less Computation and Lower Switching Frequency

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Abstract. Aiming at the computation complexity and high switching frequency existing in conventional voltage balancing method of high-level modular multilevel converters (MMCs), a novel capacitor voltage balancing method based on insertion priorities of sub-modules (SMs) is proposed. Instead of sorting the voltage values of SMs, an Allowable Capacitor Voltage Distribution Band (ACVDB) is applied to constrain the fluctuation range of capacitor voltages. And the insertion priorities of SMs in current control cycle are determined by comparing their voltage values in last control cycle with the upper and lower limits of ACVDB respectively. The effectiveness of the proposed method is validated by a 41-level MMC model in MATLAB/Simulink R2017a. Simulation results demonstrate that the switching frequency can be reduced significantly with an allowable deviation of capacitor voltages in both steady state and transient process.

1. Introduction
The modular multilevel converter (MMC) has been widely applied for high-voltage and high-power direct current transmission, renewable energy power generation, asynchronous ac grid interconnection, and high-power motor drive applications in the past two decades[1]–[3]. Compared with the two-level converter and three-level neutral-point diode-clamped converter, the MMC has the following advantages as described in [4]–[6]: 1) lower switching frequency and higher efficiency; 2) no direct series of power switches and lower manufacturing difficulty; 3) less or no need for ac filters; and 4) distributed locations of capacitive energy storages. Due to its overwhelming advantages, the MMC has become one of the most preferred voltage source converter topologies in HVDC applications.

The capacitor voltage-balancing control is a vital factor for the safe operation of MMC, which has attracted researchers’ interest. Numerous control methods have been proposed in literatures focusing on the capacitor voltage balancing. The conventional voltage balancing method, which is the most commonly used technique to carry out the capacitor voltage-balancing task of an MMC, is based on the voltage sorting and the direction of the arm current[7]–[8]. If the arm current is positive, the SMs with the lowest voltages are switched ON and the others are switched OFF. On the contrary, if the arm current is negative, the SMs with the highest voltages are selected to switch ON and the others are turned OFF. Due to the sorting algorithm in each control cycle the capacitor voltage is balanced but unnecessary switching transitions among the SMs occur. Even if the required number of on state SMs within one control cycle with respect to its previous control period does not change, the insertion and bypass of SMs may occur. Due to this, the switching frequency or loss of the MMC is increased.

To avoid unnecessary insertion/bypass of SMs within each control cycle and without compromising the capacitor voltage-balancing task, the voltage-balancing technique with reduced switching frequency of the SMs is proposed in [9]–[11]. Reference [9] proposed a method for the MMC switched

at grid frequency with reduced losses and does not rely on the arm current. By assigning the low-frequency pulses with different pulse widths, the capacitor charge transfer in the MMC can be controlled for keeping the capacitor voltage balancing in the MMC. Reference [10] introduced the balancing adjusting number (BAN) to ensure the low-switching frequency, and SM switching frequency calculation method is also presented with different BANs. Reference [11] made a trade-off between the switching losses and the balancing effect through a closed-loop control of the alternating number of the SMs, which is based on the analysis of the relationship between the switching frequency and the capacitor voltage deviation.

This paper presented a novel capacitor voltage balancing method for MMCs with less computation and lower switching frequency by introducing the Allowable Capacitor Voltage Distribution Band (ACVDB). Instead of sorting the voltage values of sub-modules (SMs), the insertion priorities of SMs in current control cycle is determined by comparing their voltage values in previous control cycle with the upper and lower limits of ACVDB respectively. Simulation results based on MATLAB/Simulink R2017a demonstrate that the switching frequency can be reduced significantly with an allowable deviation of capacitor voltages in both steady state and transient process.

2. MMC: basic structure and operation principle
2.1 Basic structure

The basic structure of a three-phase MMC consists of six arms, as illustrated in Figure 1. Each arm is constituted by \( N \) sub-modules connected in series and an arm inductor \( L_{\text{arm}} \), and the upper and lower arms of each phase are combined to form a phase unit. \( R_{\text{arm}} \) is the arm equivalent resistance. The function of the inductor \( L_{\text{arm}} \) is to limit the circulating current and compensate the voltage difference between the upper and lower arm. Each SM contains a dc storage capacitor \( C \) and a half-bridge that is made up of two power switch devices (T1 and T2) with freewheeling diodes (D1 and D2). When T1 switches on and T2 turns off, it is defined as ON state and the output voltage is \( u_{C} \). On the contrary, when T1 turns off and T2 switches on, it is defined as OFF state and the output voltage is zero. In Figure 1, \( u_{dc} \) and \( i_{dc} \) are the dc-link voltage and current; \( u_{nj} \) and \( i_{nj} \) are the converter output voltage with respect to the neutral point \( o \) and \( i_{pj} \) is the converter output current; \( u_{pj} \) and \( u_{nj} \) are the upper and lower arm currents, respectively; \( u_{pj} \) and \( u_{nj} \) are, respectively, the total voltages of SMs in the upper and lower arms of phase \( j \) (\( j = a, b, c \)).

\[
\begin{align*}
& \text{Figure 1. The basic structure of a three-phase MMC.} \\
& \text{Figure 2. Single phase equivalent circuit of the MMC.}
\end{align*}
\]
2.2 Operation principle

Figure 2 shows the single phase equivalent circuit diagram of the MMC. According to the Kirchhoff’s voltage and current law, the upper and lower arm voltages can be written as

\[
\begin{align*}
\frac{du_{pj}}{dt} + L_{arm} \frac{di_{pj}}{dt} + R_{arm}i_{pj} + u_{pj} &= \frac{u_{dc}}{2} \\
\frac{du_{nj}}{dt} - L_{arm} \frac{di_{nj}}{dt} - R_{arm}i_{nj} - u_{nj} &= -\frac{u_{dc}}{2}
\end{align*}
\]  

(1)

The upper and lower arm currents can be written as

\[
\begin{align*}
i_{pj} - i_{nj} &= i_{vj} \\
i_{pj} &= \frac{1}{2}i_{vj} + i_{comj} \\
i_{nj} &= -\frac{1}{2}i_{vj} + i_{comj}
\end{align*}
\]  

(2)

Where \(i_{comj}\) is the inner current of the phase \(j\), which flows through both the upper and lower arms, consisting of the dc component \((i_{dc}/3)\) and the circulating current \(i_{cirj}\).

\[
i_{comj} = \frac{1}{2}(i_{pj} + i_{nj}) = \frac{1}{3}i_{dc} + i_{cirj}
\]  

(4)

Based on (1) and (2), the differential equation representing the dynamic characteristics of the MMC can be obtained.

\[
u_{vj} = e_{j} - L_{arm} \frac{di_{vj}}{dt} - R_{arm}i_{vj}
\]  

(5)

\[
e_{j} = \frac{1}{2}(u_{vj} - u_{pj})
\]  

(6)

Where \(e_{j}\) is the inner emf generated in the phase \(j\).

Typical modulation strategies, such as PSC-PWM, SHE-PWM and nearest level control (NLC), are all widely applied. Compared with other strategies, NLC is more suitable for MMC with numerous SMs series connected in each arm. The proposed method in this paper is developed based on the NLC strategy. The reference voltage of phase unit can be generally expressed as

\[
u_{ref, phase} = \frac{1}{2}mU_{dc}\cos(\omega_{0}t + \delta_{0})
\]  

(7)

Where \(m\) is the modulation index, \(\omega_{0}\) is the fundamental angular frequency, and \(\delta_{0}\) is the initial phase angle. According to (1), the reference voltages of the upper and lower arms can be expressed as

\[
u_{ref, arm} = \frac{1}{2}U_{dc}\left(1 + m\cos(\omega_{0}t + \delta_{0})\right)
\]  

(8)

So the reference number of SMs to switch ON in the arm can be calculated as

\[
n_{ref, arm} = \text{round}\left[\frac{1}{2}U_{dc}\left(1 + m\cos(\omega_{0}t + \delta_{0})\right)\right]
\]  

(9)

Where \(U_{CN}\) is the nominal value of capacitor voltages in each arm; \(\text{round}[\cdot]\) is the nearest integer approximation function.

3. Proposed voltage balancing method

The purpose of capacitor voltage-balancing control is to keep the capacitor voltages of SMs relatively consistent rather than identical, thereby to reduce the dispersion of capacitor voltages among the SMs in each arm. In addition, the consistency of capacitor voltages is contradictory to the switching frequency of power devices. Excessive emphasis on the consistency of capacitor voltages will inevitably lead to a sharp increase in the switching frequency, and blind reduction of switching
frequency will certainly lead to poor balance effect of capacitor voltages. Therefore, the requirement of the consistency of capacitor voltages can be appropriately relaxed to reduce the switching frequency of power devices, so that a coordination suitable for engineering applications can be achieved. Based on the above problems, a voltage balancing method with less calculation is proposed, which can not only reduce the switching frequency, but also ensure good capacitor voltage balancing effect.

3.1 Implement of the proposed method

The basic principle of the proposed method is to determine the insertion priority of the SM based on the direction of current, the instantaneous value of capacitor voltage and the SM state (i.e. insertion or bypass). Figure 3 shows the flow chart of the proposed voltage-balancing method, which involves the five major steps. In Figure 3, \( N \) is the number of SMs in each arm; \( U_c \) is the vector of instantaneous capacitor voltages of SMs in the arm; \( V_{pri,old}/V_{pri,new} \) is the insertion priority vector of SMs in last/this control cycle; \( V_{state,old}/V_{state,new} \) is the state vector of SMs in last/this control cycle; \( ON_{pri,old}/OFF_{pri,old} \) is the insertion priority vector of SMs in the IN/OUT state group in last control cycle.

![Figure 3. The flow chart of the proposed capacitor voltage-balancing method.](image)

1) Pretreatment. Calculate the number of SMs \( N_m \) to be switch IN in this control cycle according to the reference voltage for this arm. If \( N_{m}=0 \), switch OUT all SMs in the arm and set each element of \( V_{state,new} \) equals to 0, i.e. \( V_{state,new}(i)=0 \); If \( N_{m}=N \), switch IN all SMs in the arm and set each element of \( V_{state,new} \) equals to 1, i.e. \( V_{state,new}(i)=1 \). At the same time, the insertion priorities of SMs in this control cycle remain unchanged from the last control cycle, that is, \( V_{pri,new}=V_{pri,old} \). If \( 0<N_{m}<N \), the in-depth analysis needs to be performed in the following steps.

![Figure 4. Division of insertion priorities of SMs.](image)
2) Introduction of the Allowable Capacitor Voltage Distribution Band (ACVDB). Measure the instantaneous capacitor voltages in the arm and calculate the corresponding average voltage $U_{c, \text{avg}}$.

$$U_{c, \text{avg}} = \frac{1}{N} \sum_{i=1}^{N} U_{c}(i)$$

(10)

Superimpose the Allowable Capacitor Voltage Distribution Band on the curve of the average voltage to constrain the fluctuation range of capacitor voltages. The width of the ACVDB is determined by the expected dispersion threshold of capacitor voltages (i.e., $\sigma_m$), which needs to be given in advance. The upper and lower limits of the ACVDB can be expressed as

$$U_{c, \text{upper}} = U_{c, \text{avg}} + \frac{\sigma_m}{2} \times U_{c,N}$$

$$U_{c, \text{lower}} = U_{c, \text{avg}} - \frac{\sigma_m}{2} \times U_{c,N}$$

(11)

Where $U_{c, \text{upper}}$ is the upper limit of the ACVDB; $U_{c, \text{lower}}$ is the lower limit of the ACVDB.

3) Determination of insertion priorities of SMs in this control cycle. Obtain the serial number of SM by accessing each element of $V_{\text{pri_old}}$ sequentially and divide it into the IN state group of SMs (represented by $ON_{\text{pri_old}}$) or the OUT state group of SMs (represented by $OFF_{\text{pri_old}}$) based on the state of corresponding SM, which is stored in $V_{\text{state_old}}$. By comparing capacitor voltages of SMs whose serial number belongs to $ON_{\text{pri_old}}$ and $OFF_{\text{pri_old}}$ in last control cycle with the upper and lower limits of ACVDB respectively, the insertion priorities of SMs in this control cycle are determined.

4) Selection of the SMs to be switched IN in this control cycle. The serial numbers of SMs are rearranged according to the order of insertion priorities from high to low, and the new insertion priority vector $V_{\text{pri_new}}$ in this control cycle is formed. The SMs corresponding to the first $N_{\text{on}}$ serial numbers of $V_{\text{pri_new}}$ are selected to be switched IN and the remaining SMs are selected to be switched OUT in this control cycle. Then the state vector of SMs in this control cycle is updated as (12).

$$V_{\text{state_new}}(V_{\text{pri_new}}(i)) = 1 \quad i = 1, 2, \ldots, N_{\text{on}}$$

$$V_{\text{state_new}}(V_{\text{pri_new}}(j)) = 0 \quad j = N_{\text{on}} + 1, N_{\text{on}} + 2, \ldots, N$$

(12)

5) Preservation of information in this control cycle. $V_{\text{pri_new}}$ and $V_{\text{state_new}}$ are saved to facilitate the use of the next control cycle, that is, $V_{\text{pri_old}} = V_{\text{pri_new}}$ and $V_{\text{state_old}} = V_{\text{state_new}}$.

3.2 The specific division of insertion priorities of SMs

Figure 4 shows the determination of insertion priorities of SMs in different current directions and the results are presented in Table 1. For each insertion priorities in Table 1, the smaller the value, the higher the priority, as written in (13), and the greater the possibility that the corresponding SMs are switched IN. For the SMs in the same priority layer (i.e. I, II, III), the insertion priority of the SM in the IN state group is always higher than that of the SM in the OUT state group.

$$I-1 > I-2 > II-1 > II-2 > III-1 > III-2$$

(13)

**Table 1.** The division results of insertion priorities of SMs

| $u_c$ | $i_{\text{arm}>0}$ | $i_{\text{arm}<0}$ |
|-------|-----------------|-----------------|
| $u_c > U_{c, \text{upper}}$ | $ON_{\text{pri_old}}$ | $ON_{\text{pri_old}}$ |
| $U_{c, \text{lower}} \leq u_c \leq U_{c, \text{upper}}$ | $II-1$ | $II-2$ |
| $u_c < U_{c, \text{lower}}$ | $I-1$ | $I-2$ |
| $ON_{\text{pri_old}}$ | $ON_{\text{pri_old}}$ |
| $ON_{\text{pri_old}}$ | $ON_{\text{pri_old}}$ |

4. Simulation results

To evaluate the performances of the 41-level single-terminal MMC system that operates on the base of the conventional voltage-balancing strategy and the proposed voltage-balancing strategy in this paper, some simulations are conducted with software MATLAB/Simulink R2017a. The system parameters are given in Table 2.
Table 2. Main parameters of the simulation system

| Parameter                     | Value         |
|-------------------------------|---------------|
| Power rating \( P_n \)        | 500 MW        |
| AC system voltage \( U_{ac} \) | 220 kV        |
| Fundamental frequency \( f_0 \) | 50 Hz         |
| Transformer ratio \( k \)     | 220kV/210kV   |
| Transform leakage inductance \( L_0 \) | 0.1 pu |
| DC-link voltage \( U_{dc} \)  | \( \pm 200 \) kV |
| Number of SMs per arm \( N \) | 40            |
| Nominal capacitor voltage \( U_{CN} \) | 10 kV  |
| Capacitance in SM \( C_0 \)   | 1700 uF       |
| Arm inductance \( L_0 \)      | 78 mH         |
| Control cycle \( T_{ctrl} \)  | 100 \( \mu \)s |

4.1 Simulation results in the steady state

Employing the conventional strategy and the proposed strategy respectively, the simulation results are shown in Figure 5 and Figure 6. In the proposed method, \( \sigma_{cap} \) is set to 8\%. That is, the greatest capacitor voltage deviation is limited to 0.8\( \)kV, which is little enough that it is acceptable absolutely.

Figure 5. Simulation results of conventional voltage balancing method.

Figure 6. Simulation results of the proposed method in this paper.

Figure 5(a) and Figure 6(a) show the capacitor voltages of 40 SMs in the upper arm of phase A. As shown in Figure 6(a), the capacitor voltages are tightly bound in the Allowable Capacitor Voltage Distribution Band. If the capacitor voltage of SM crosses the upper and lower limit of ACVDB, the state of the corresponding SM will be changed to prevent its capacitor voltage from exceeding the limits continuously. Figure 5(b) and Figure 6(b) present the comparison of gate signals of the power
device T1 of the 20th SM in the upper arm of phase A with different voltage balancing techniques, obviously, the pulse density of proposed strategy is much less than that of conventional strategy. Figure 5(c) and Figure 6(c) show the switching times of 40 sub-modules in the upper arm of phase A. The average switching frequency of the conventional voltage balancing is 1900.8 Hz while in the proposed voltage balancing technique is 115.3 Hz.

4.2 Simulation results in transient process

4.2.1 The start-up charging process. The start-up simulation with two stages (i.e. the uncontrolled and controllable charging stage) is carried out to confirm the effectiveness of the proposed voltage-balancing strategy in the charging process, and the simulation results as shown in Figure 7. Figure 7(a) shows the reference and actual values of DC-link voltage, in which $U_{dc_{-}ref}$ is a slope signal with the changing rate equal to 200kV/s and the upper limit equal to 400kV. Figure 7(b) shows the voltage waveforms of capacitors in the upper arm of phase A. It can be seen that capacitor voltages gradually diverge from $t=1.5$ s, but are always controlled within the allowable capacitance voltage distribution band. In addition, the charging current on the AC side has never exceeded 400A during the start-up process, as shown in Figure 7(c).

4.2.2 The power stepping process. To demonstrate the dynamic response of the system, the active power is adjusted from 300MW to 500MW and the reactive power is adjusted from 100MW to 0, which occur at $t=5.1$s. Figure 8(a) and Figure 8(b) show the corresponding active and reactive power flowing from MMC to AC grid. Figure 8(c) shows the response of capacitor voltages in the upper arm of phase A. As it can be seen, the capacitor voltages can be well balanced at the average value under the transient condition.

![Figure 7](image1)  ![Figure 8](image2)

**Figure 7.** Simulation results of capacitor voltage balancing during start-up charging process

**Figure 8.** Simulation results of capacitor voltage balancing during power stepping process

5. Conclusion

In this paper, a novel capacitor voltage-balancing method without voltage sorting algorithm is presented, the basic principle of which is to determine the insertion priorities of SMs in each control cycle by comparing its capacitor voltage with the upper and lower limits of Allowable Capacitor
Voltage Distribution Band respectively. Performances of the proposed voltage-balancing method, which includes reduced switching frequency and capacitor voltage balancing, are validated in the MATLAB/Simulink, and the following conclusions can be obtained:

- The proposed method has only one control parameter, i.e. $\sigma_m$, which allows the designer to select how much the difference is desired among capacitor voltages.
- The proposed method can reduce the switching frequencies of power devices to several times of fundamental frequency, and keep the capacitor voltage balance with a tolerable voltage deviation.
- The proposed method can be applied both in the steady state and the transient process.

In addition, the proposed method is computationally less complex, and easy to implement by using digital controllers.

6. References

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