Flexible and Printed Electronics

PAPER

Screen printed digital circuits based on vertical organic electrochemical transistors

Peter Andersson Ersman, David Westerberg, Deyu Tu, Marie Nilsson, Jessica Åhlin, Annelie Eveborn, Axel Lagerlöf, David Nilsson, Mats Sandberg, Petronella Norberg, Magnus Berggren, Robert Forchheimer and Göran Gustafsson

1 Dept. of Printed Electronics, RISE Acreo AB, Bredgatan 33, SE-60221, Norrköping, Sweden
2 Dept. of Electrical Engineering, Linköping University, SE-58183 Linköping, Sweden
3 Laboratory of Organic Electronics, Dept. of Science and Technology, Linköping University, SE-60174 Norrköping, Sweden
4 RISE SICS East, Linköping University, SE-58183 Linköping, Sweden

E-mail: peter.andersson.ersman@ri.se

Keywords: electrochemical transistor, printed electronic circuit, PEDOT:PSS, electrolyte, SPICE model, hybrid electronics

Abstract

Vertical organic electrochemical transistors (OECTs) have been manufactured solely using screen printing. The OECTs are based on PEDOT:PSS (poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid)), which defines the active material for both the transistor channel and the gate electrode. The resulting vertical OECT devices and circuits exhibit low-voltage operation, relatively fast switching, small footprint and high manufacturing yield; the last three parameters are explained by the reliance of the transistor configuration on a robust structure in which the electrolyte vertically bridges the bottom channel and the top gate electrode. Two different architectures of the vertical OECT have been manufactured, characterized and evaluated in parallel throughout this report. In addition to the experimental work, SPICE models enabling simulations of standalone OECTs and OECT-based circuits have been developed. Our findings may pave the way for fully integrated, low-voltage operating and printed signal processing systems integrated with e.g. printed batteries, solar cells, sensors and communication interfaces. Such technology can then serve a low-cost base technology for the internet of things, smart packaging and home diagnostics applications.

1. Introduction

The field of printed electronics has evolved rapidly during recent decades and is today a mature and vast research field, as evidenced by the increasing number of companies that are operating globally with this technology integrated into various products. One example of such an application is the smart temperature sensor labels that currently are being developed and launched onto the market [1]. These smart sensor labels typically contain a variety of printed electronic components, e.g. memories [2], solar cells [3], batteries [4], supercapacitors [5], diodes [6], sensors [7], transistors [8] and display devices [9]. Organic field-effect transistors (OFETs) have been extensively developed during the last 25 years, where the main target of these devices has been to replace silicon-based counterparts in order to minimize the manufacturing cost as well as to enable transistor circuitry on unconventional and flexible substrates [10]. However, OFETs exhibit a number of disadvantages, mainly related to the challenge of forming pinhole-free dielectric thin-film gate insulators, poor on-currents, drift of device parameters due to bias-stress, non-robust device structures and high-voltage operation. On the contrary, OECTs include a gate electrolyte, which can be relatively much thicker compared to the gate insulator in OFETs and still provide low-voltage operation. This means that pinholes, which cause electrical short-circuits between the gate and the transistor channel, are less likely to be formed. Also, this offers the possibility to build OECTs using a relatively much more robust structure and different vertical and lateral architectures, or combinations, can be used. This freedom is also reflected in that one can choose between a wide array of manufacturing tools for the manufacturing of OECT devices and circuits [11]. Further, the relatively much lower drain currents
in OFETs are explained by the fact that only the first few monolayers of the organic semiconductor, which is in direct contact with the gate dielectric layer, serve as the active channel. Instead, the current that flows between the source and the drain contacts in OECTs utilizes the complete bulk of a conducting polymer (PEDOT and PSS). A material combination that forms the electrically conducting polymer PEDOT:PSS, which can be processed by different coating and printing techniques from water-based emulsions (the chemical structures of PEDOT and PSS are shown in figure 1(a)). The inherent conducting property of PEDOT:PSS also implies that the resulting OECT device is said to operate in depletion mode, i.e. the transistor channel is conducting at zero gate voltage.

The OECT can be designed according to different architectures, as shown in figures 1(b) and (c); lateral configurations are often preferred when the transistors are used in sensor applications [12] or when the number of processing steps must be kept at a minimum, while a vertically stacked OECT is advantageous when parameters such as switching time and footprint are of higher importance, for example in printed circuits. In the past, circuits and devices based on lateral OECT configurations have been manufactured solely using screen printing [13]. The manufacturing of devices and circuits based on a vertically arranged OECT configuration, which inevitably implies smaller footprint as compared to the lateral configuration, has so far required either photolithographic steps and/or thermally evaporated source and drain electrodes [14] or lamination of e.g. the gate electrode layer [15]. Here, all-printed OECT devices and digital circuits are reported, wherein all layers of the vertical OECT devices are deposited by the very same screen printing equipment. Two different designs of vertical OECT are being evaluated in parallel throughout this report; PEDOT:PSS serves as the channel in both designs, and it also serves as the source and drain contacts in the OECT design denoted P-P, while the source and drain contacts are replaced by carbon in the OECT design denoted C-C. The resulting devices exhibit low-voltage operation (~1 V), on/off-ratios in the range \(10^3\)–\(10^4\), switching times in the range 20–300 ms, small footprint and high manufacturing yield. The relatively long switching time of OECT devices surely rule out a direct replacement of their silicon
counterparts. However, the intention of the development of vertical OECTs and circuits is rather aimed at utilizing logic circuits based on silicon and OECTs in a complementary manner. Hence, silicon-based electronics should be used for communication and computational purposes, while OECTs should be used for e.g. multiplexers, decoders and display drivers, in various kinds of smart labels within the internet of things and similar applications, in order to minimize the number of contact pads on the silicon chip. Contact pads represent a great fraction of the entire Si-chip area in internet-of-things (and similar) applications. Therefore, there is a great desire to reduce the number of contact pads, thus leading the way for low-cost Si-chips that will enable digital and electronic communication and functionality also in price-sensitive applications. With OECT-based digital circuits forming decoders and multiplexers, and thereby complementing the Si-chip, the same pad on the Si-chip can now be used for multiple purposes [16].

2. Materials and methods

2.1. Device manufacturing

All materials were deposited by flatbed sheet-fed screen printing equipment (DEK Horizon 03iX) on top of plastic substrates originating from polyethylene terephthalate (PET), for example Polifolia Bias purchased from Policrom Screen. The screen printing tools were based on standard polyester mesh. A schematic of the screen printing process to obtain the two OECT designs is illustrated in figure 1(d). Conductors and contact pads based on silver (Ag 5000 purchased from DuPont) were first deposited on top of the flexible plastic substrate (denoted I in the figure). The contact pads serve as the probing surfaces. PEDOT:PSS, Clevios SV3 purchased from Heraeus, which serves as the electrochemically active transistor channel, is then patterned between the silver contact pads (II), followed by the deposition of carbon electrodes (7102 conducting screen printing paste purchased from DuPont) on top of a respective side of the previously deposited PEDOT:PSS transistor channel (III). The silver, the PEDOT:PSS and the carbon inks are all dried at 120 °C for 5 min. Subsequently, an insulating layer (e.g. 5018 purchased from DuPont) is deposited and UV-cured, in which openings define the area of the following electrolyte deposition (IV). The opening of the insulating layer covers the area of PEDOT:PSS that is targeted to become the active transistor channel in both the C-C and the P-P OECT designs, but in C-C OECTs, the opening extends also on top of the previously deposited carbon-based source and drain electrodes. The electrolyte (AFI VV009 provided by RISE Acero) was deposited in the following process step (V). The electrolyte layer, which was cured by UV light exposure, enables the current modulation by providing the ions that are required for the switching mechanism to occur between the transistor channel and the gate electrode. Finally, the OECT device is completed by the deposition of PEDOT:PSS (Clevios SV3 purchased from Heraeus) serving as the gate electrode layer (VI). The resistors used in the circuit designs consisted of a carbon-based ink (7082 purchased from DuPont). Additionally, the electronic vias that were required in decoders and multiplexers were created by the deposition of the insulating 5018 ink followed by the deposition of Ag 5000 on top of the insulating ink to complete the conductor crossings.

2.2. Electrical characterization

All measurements are performed in a controlled environment at a temperature of ~20 °C and at a relative humidity of ~45%RH. Output, transfer and dynamic switch measurements were performed by using a semiconductor parameter analyzer (HP/Agilent 4155B) and a function generator (Agilent 33120A). In the output measurements, V G was stepped from 0 V to 1.2 V in steps of 400 mV, V D was stepped from 0 V to −3 V in steps of 50 mV and medium integration time was used. In the transfer measurements, V G was stepped from 0 V to 2 V in steps of 50 mV, V D was constant at −1.5 V and medium integration time was used. In the dynamic switch measurements, V G was supplied from a function generator as a square wave alternating between 0 V and 1.2 V with a frequency of 1 Hz and a duty cycle of 50%, while V D was constantly supplied at −1.5 V. The time between samples was 1.04 ms and a total of 5000 samples were acquired, except for the measurements in figures 3(g) and (h) where V D was lowered to −1 V and the cycle was prolonged to 60 s. Short integration time was used. The printed circuits were characterized by using a data acquisition card (DAQCard-6036E from National Instruments). The DAQ card supplied +/−3 V to the printed circuits, and the input signal (V G) was switched between 0 V and 1 V, or sometimes between 0 V and 1.2 V.

3. Results and discussion

To establish an all-printed version of the vertical OECT does not only require a printable electrolyte, it must also be sufficiently cured and/or orthogonal with the solvent of the subsequently deposited gate electrode. Additionally, the wetting properties of the electrolyte and the gate electrode material must also be compatible with each other. These requirements have therefore, until now, prevented the utilization of all-printed vertical OECT devices. However, once these requirements have been met, the manufacturing process of the vertically configured PEDOT:PSS-based OECT devices is straightforward since screen printing is the only required deposition method; this is further illustrated in figure 1(d).
PEDOT:PSS is a versatile material that has been explored in many different printed electronic applications throughout the years. The polymer exhibits high ionic conductivity due to the inclusion of a large amount of PSS, which enables functionality and short response time in e.g. ion pumps [17] and electrochromic displays [18]. The OECT relies on the same kind of switching mechanism as compared to an electrochromic display, and the ionic conductivity is therefore a prerequisite in order to achieve acceptable switching performance. However, even though the ionic conductivity is advantageous from a switching point of view, it also implies a disadvantage in that the cations that are ingressed into the conducting polymer upon electrochemical reduction migrate laterally in the film, outside the electrolyte edge, by the potential gradient caused by the applied drain-source voltage. This phenomenon has been reported previously, and it is commonly known as a reduction front [15, 19, 20]. The reduction front does not correspond to permanent degradation of this particular OECT device, here denoted P-P OECT design, but it is more of a temporary degradation causing a non-symmetric switching behavior; the on-to-off switching time is much shorter as compared to the off-to-on switching time. The non-symmetric switching behavior occurs independently of whether the lateral or vertical OECT is utilized, but there are ways to circumvent this; for example, by the introduction of a drain contact material, and possibly also a source contact material, that is in contact with the PEDOT:PSS in the transistor channel and the electrolyte layer. The relative inertness to electrochemical reactions of such material, for example by the introduction of carbon as the drain and source contacts, helps to prevent, or at least minimize, the reduction front; the transistor architecture here denoted C-C OECT design [15]. In this report, the P-P and the C-C vertical OECT designs will be evaluated in the following section, both in standalone OECT components as well as in various printed circuits.

3.1. Standalone OECTs

All-printed standalone OECTs based on the two different vertical architectures were evaluated initially, before characterizing all-printed vertical OECT-based circuits. In one of the OECT architectures, the P-P OECT design, PEDOT:PSS, serves as both the transistor channel as well as the drain and source contacts. In other words, the transistor channel is defined by the area of the printed PEDOT:PSS stripe that is in contact with the electrolyte layer, see figure 2(a). This architecture typically results in lower off-current, and hence higher on/off-ratio, but it also suffers from prolonged switching time due to the reduction front mentioned above. The other OECT architecture, the C-C OECT design, contains source and drain contacts based on screen printed carbon, and the electrolyte is in contact with the PEDOT:PSS representing the transistor channel as well as the source and drain contacts, see figure 2(b). The reduction front is thereby minimized by the potential gradient being equilibrated by the source and drain contacts, i.e. the lateral migration of reduced PEDOT:PSS outside the electrolyte edge is prevented. The two OECT architectures were originating from three different plastic sheets and were characterized by output, transfer and dynamic switch measurements.

The results of the OECT characterization are shown in figure 3. The upper graphs are summaries of the output measurements of the C-C (a) and the P-P (b) OECT devices, respectively. This is followed by the transfer measurements of the C-C (c) and the P-P (d) OECT devices, respectively. The dynamic switch measurement of a pristine C-C and P-P OECT device is shown in (e) and (f), respectively; the duration of these measurements is only 5 s. Similar dynamic switch measurements were recorded after a few minutes of device operation of another C-C (g) and P-P (h) OECT device, respectively, but the measurement duration was prolonged to 60 s. Table 1 provides an overview of on- and off-current levels, on/off-ratios and switching times from the dynamic switch measurements shown in figures 3(e) and (f). The on-current for P-P OECTs as compared to C-C OECTs; an effect caused by more efficient pinch-off within the channel for \( V_G = 0 \) V. The off-current for P-P OECTs is much lower compared to the off-current in C-C OECTs. This is due to the fact that the exposed carbon electrodes in the C-C OECT design results in a larger leakage current, thus the on/off-ratio is higher for P-P OECTs than for C-C OECTs. However, P-P OECTs suffer
Figure 3. Summary of output, transfer and dynamic switch measurements. The graphs in (a) and (b) show the output measurements of six C-C and P-P OECTs, respectively; the devices originated from three different sheets. $V_G = 0, 0.4, 0.8$ and 1.2 V were applied in the output sweeps. The graphs in (c) and (d) show the transfer measurements of five C-C and six P-P OECTs, respectively; the devices originated from three different sheets. $V_{DS} = -1.5$ V was applied in the transfer sweeps. The graphs in (e) and (f) show the dynamic switch measurement of one of the C-C and one of the P-P OECTs, respectively. $V_{DS} = -1.5$ V was applied in these dynamic switch measurements, and $V_G$ varied between 0 and 1.2 V at a frequency of 1 Hz. The graphs in (g) and (h) show the dynamic switch measurement of one of the C-C and one of the P-P OECTs, respectively, during 60 s of operation. The P-P OECT design is severely affected by the reduction front, despite the fact that $V_{DS}$ was lowered to $-1$ V in this particular measurement, while the performance of the C-C OECT design remains throughout the measurement cycle. Note that only the initial 10 s and the final 5 s of the measurements are shown in the graphs.
Table 1. The average values from the dynamic switch measurements based on C-C OECTs and P-P OECTs chosen from three different plastic substrates. $V_{DS} = -1.5$ V was applied in the dynamic switch measurements, and $V_G$ varied between 0 and 1.2 V at a frequency of 1 Hz.

| Design   | On-current (A) | Off-current (A) | On/off ratio | Switching time on-to-off, 90%–10% (ms) | Switching time off-to-on, 10%–90% (ms) |
|----------|----------------|-----------------|--------------|----------------------------------------|----------------------------------------|
| C-C OECT | $4.93 \times 10^{-4}$ | $8.65 \times 10^{-7}$ | 733          | 24.7                                   | 193                                    |
| P-P OECT | $1.93 \times 10^{-4}$ | $1.92 \times 10^{-8}$ | 11 097       | 22.3                                   | 286*                                   |

* Note that the off-to-on switching time of the P-P OECT design is dependent on amplitudes and pulse lengths of the measurement. This particular switching time originates from the data in figure 3(f), but it would be prolonged to several seconds in case of determining the switching time in the end of the measurement shown in figure 3(h).

The SPICE model delivers similar current-voltage characteristics as compared to the measured data (figure 3) for both P-P and C-C OECTs, as shown in figure 5. The same parameters were used in the models of the two different OECT architectures: $R_1 = 500 \, \Omega$, $R_2 = 200 \, \Omega$, $C_1 = 0.2 \, \mu F$, the saturation current of $D_1$ was set to $0.1 \, \mu A$, and the transconductance of $R_{MOS-P-Dep}$, $k_p$, was set to $1 \times 10^{-5} \, S$. The main difference between the two OECT architectures is that a few different parameters related to the source and drain contacts were used, such as the leakage resistors $R_3 = R_4 = 2 \, M \Omega$ for the C-C OECTs, while the same resistors were $200 \, M \Omega$ for the P-P OECTs. The source and drain contact resistances of $R_{MOS-P-Dep}$, $r_s$ and $r_d$, were set to $0.4 \, \Omega$ for the C-C OECTs, while the contact resistances were set to $3 \, k \Omega$ for the P-P OECTs. Moreover, the threshold voltage of $R_{MOS-P-Dep}$, $v_{to}$, was set to 1.2 V for the P-P OECTs, while it was shifted to 0.8 V for the C-C OECTs. The steep transition in the transfer curves, as shown in figure 5(a), is due to the intrinsic small slope swing of silicon MOS transistors. The OECTs usually exhibit a larger slope swing due to the slower doping/dedoping process.

Figure 4. An OECT SPICE model: The symbol is shown in (a) and the equivalent sub-circuit is shown in (b).

from prolonged switching times caused by the reduction front [15]. This is demonstrated in figures 3(g) and (h), in which the C-C and P-P OECT designs are operated at $V_{DS} = -1$ V and $V_G$ is cycled between 0 and 1.2 V at a frequency of 1 Hz. The on-current level of the C-C design is more or less unaffected after 60 s, while the reduction front temporarily has disabled the transistor functionality in the P-P OECT design within a few tens of seconds. In other words, it would only be possible to use a switching frequency of 1 Hz for a limited period of time in the case of the P-P OECT design, which makes P-P OECT design difficult to use in printed circuits.

3.2. Simulations of standalone OECTs

In order to enable the design and simulation of OECT-based circuitry, SPICE models of the OECTs have been developed in B2 SPICE (EMAG Technologies Inc.). The symbol of the three-terminal OECT device is shown in figure 4(a). The model is built as an equivalent sub-circuit comprising one silicon MOS transistor (MOS_P_Dep), one diode ($D_1$), four resistors ($R_1$, $R_2$, $R_3$, and $R_4$), and one capacitor ($C_1$), as shown in figure 4(b). Since the OECTs are operated in depletion mode, a typical p-type depletion MOSFET model (level = 1) in B2 SPICE is utilized here. To represent the asymmetric and slower switching response of the OECTs, as compared to their silicon counterparts, two resistors ($R_1$ and $R_2$), one capacitor ($C_1$), and one diode ($D_1$) are used in the sub-circuit. The resistor $R_3/R_4$ between the gate electrode and the drain/source contact of the silicon transistor (MOS_P_Dep) determines the main leakage current from the gate electrode to the drain/source contact, respectively.

The SPICE model delivers similar current-voltage characteristics as compared to the measured data (figure 3) for both P-P and C-C OECTs, as shown in figure 5. The same parameters were used in the models of the two different OECT architectures: $R_1 = 500 \, \Omega$, $R_2 = 200 \, \Omega$, $C_1 = 0.2 \, \mu F$, the saturation current of $D_1$ was set to $0.1 \, \mu A$, and the transconductance of the MOS_P_Dep, $k_p$, was set to $1 \times 10^{-5} \, S$. The main difference between the two OECT architectures is that a few different parameters related to the source and drain contacts were used, such as the leakage resistors $R_3 = R_4 = 2 \, M \Omega$ for the C-C OECTs, while the same resistors were $200 \, M \Omega$ for the P-P OECTs. The source and drain contact resistances of the MOS_P_Dep, $r_s$ and $r_d$, were set to $0.4 \, \Omega$ for the C-C OECTs, while the contact resistances were set to $3 \, k \Omega$ for the P-P OECTs. Moreover, the threshold voltage of the MOS_P_Dep, $v_{to}$, was set to 1.2 V for the P-P OECTs, while it was shifted to 0.8 V for the C-C OECTs. The steep transition in the transfer curves, as shown in figure 5(a), is due to the intrinsic small slope swing of silicon MOS transistors. The OECTs usually exhibit a larger slope swing due to the slower doping/dedoping process.
NAND gates are the building blocks that have been used when designing the relatively more advanced 2-to-4 decoder and 4-to-1 multiplexer circuits, the former circuit contains 14 OECTs (four two-input NANDs and six inverters) and the latter circuit contains 18 OECTs (four three-input NAND, one four-input NAND and two inverters). All-printed circuits reported herein, inverters, NAND gates, decoders and multiplexers, are supplied with $+/-3\text{ V}$, and all circuits are also relying on the voltage divider circuit based on three resistors, simply due to the fact that the OECT is operated in depletion mode. The area of the screen printed OECT, inverter and two-input NAND gate, when also including conductors and contact pads, is 16 $\text{mm}^2$, 82 $\text{mm}^2$ and 123 $\text{mm}^2$, respectively. This corresponds to a footprint reduction of two to three times lower in the P-P OECTs. This is explained by that the same resistor values are put of the P-P OECT-based inverter is only observed by comparing the high digital states; the output voltage levels obtained in the inverter circuit shown in Figure 7. Furthermore, the output voltage follows the targeted values of the low and high output voltage levels of the printed circuits equal approximately 0.2–0.3 V and 0.95–1.05 V, respectively. There are two reasons for targeting $\sim 0.25\text{ V}$ as the low output voltage level; to prevent over-oxidation of the transistor channel by ensuring that $V_G$ always remains positive [21] as well as that only minor current modulation occurs below $\sim 0.25\text{ V}$, as can be observed by the transfer curves. Both circuits show approximately the same low digital states ($\sim 0.2\text{ V}$) and similar time response, that is, there is no temporary exhaustive behavior caused by the reduction front in the P-P OECT-based inverter during this measurement. This is explained by the fact that no cycling of the circuit was performed prior to this measurement, and also because of the relatively short duration of the measurement. The major difference between the two circuits can be observed by comparing the high digital states; the output of the P-P OECT-based inverter is only $\sim 0.85\text{ V}$. This is explained by that the same resistor values are used in both circuits, but the on-current level is about two to three times lower in the P-P OECTs (see figure 3 and table 1).

Figure 8 shows the results of the characterization of 2-input NAND gates based on either C-C or P-P OECTs. The voltage levels of the low and high digital states of the 2-input NAND are comparable with the voltage levels obtained in the inverter circuit shown in Figure 7. Furthermore, the output voltage follows the

3.3. Printed circuits based on OECTs

The previous section covered measurements on all-printed OECTs that were manufactured as standalone devices on the plastic substrates; however, various kinds of logic circuits were also included in the same layout. More specifically, the layout also included inverters, two-, three- and four-input NAND gates, 2-to-4 decoders and 4-to-1 multiplexers. All of these circuits were fabricated in two versions based on the C-C OECT design and the P-P OECT design, respectively. As mentioned in the introduction, the purpose of establishing a platform containing all-printed OECTs is not to compete with silicon-based electronics; the former should be used in multiplexers, decoders and display drivers in e.g. smart sensor labels, in order to cut the cost of the silicon chip by minimizing the number of contact pads, while the latter still should be used for communication and computational reasons. Figure 6 shows the schematics of two examples of the printed circuits that have been evaluated; an inverter and a two-input NAND gate. The inverter is the most trivial logic gate containing only one OECT. Further, by connecting additional OECTs in parallel, it is possible to create NAND gates with a desired number of inputs; one OECT corresponds to one input of the NAND gate. Inverters and

Figure 5. Simulated transfer curves (a) and dynamic switching characteristics (b) of the P-P (black line) and C-C (dashed red line) OECTs. A voltage of $-1.5\text{ V}$ was applied between the drain and source contacts in both (a) and (b), and the applied gate voltage in (b) was a $0/1.2\text{ V}$ pulse with a frequency of 1 Hz.

Inverters, two-, three- and four-input NAND gates, two to three times lower in the P-P OECTs.
truth table well, i.e. the output voltage is low only when both input voltage levels are high. Both circuits show approximately the same digital states and similar time response. The lack of temporary exhaustive behavior in the P-P OECT-based two-input NAND gate is yet again explained by the fact that no initial cycling of the circuit was performed, and because of the short duration of the measurement. The high digital state of the P-P OECT circuit is slightly improved when compared with the inverter circuit shown in figure 7, at least when both input voltages are low. This can be explained by the fact that two OECTs are connected in parallel, hence their total resistance is lowered and a better match with the printed resistors is obtained.

Figure 9 shows the results of the characterization of 2-to-4 decoder circuits based on either C-C or P-P OECTs. Decoder circuits are used in various electronic applications, and the most obvious example in the
context of printed electronics, and more particularly smart sensor labels, would be to utilize the output voltage signals \(\text{V}_{\text{OUT1}}-\text{V}_{\text{OUT4}}\) of the decoder circuit as addressing signals in a printed electrochromic display having multiple segments. Each decoder circuit contains 14 OECTs, and both designs are performing according to the truth table. However, the voltage versus time behavior indicates that the circuit based on C-C OECTs performs better, as evidenced by less distortion of the output voltage signal with respect to time and more well-defined voltage levels of the digital states, as compared to the design relying on the P-P OECTs. The difference in time response is explained by the propagating reduction front prolonging the off-to-on transition time of the P-P OECTs, while the mismatch between the on-state of the P-P OECT channels and the printed resistors explains the less well-defined voltage levels of the digital states.

Figure 10 shows the results of the characterization of 4-to-1 multiplexer circuits based on either C-C or P-P OECTs. Keeping the smart sensor label application in mind, in which a multiple number of sensors typically are desired, a multiplexer circuit is the most obvious choice in order to select which sensor input...
that should be activated and thereafter analyzed. The 4-to-1 multiplexer is the most complex circuit within this report, partially because of the 18 OECTs that are required to complete the circuit, but also due to the fact that NAND gates with varying number of inputs are used, which can potentially create a mismatch between the OECTs and the printed resistors. Additionally, it becomes even more obvious that the P-P OECTs are suffering from the reduction front. The control signals (VC1 and VC2) select which input voltage signal (VIN1-VIN4) that should pass through to the voltage output (VOUT). VOUT of the circuit based on C-C OECTs follows the frequency of the chosen VIN relatively well, more or less independently of the combination of the control signals. On the contrary, the multiplexer based on the P-P OECTs follows VIN of the two signals having the highest frequency, denoted VIN1 and VIN2, while the switching time of VOUT is prolonged as the frequency of VIN is lowered; again, an effect of the reduction front discussed earlier. Lower frequency implies a longer time for the propagation of the reduction front, hence the front moves further outside the electrolyte edge, which inevitably prolongs the off-to-on transition time of P-P OECTs.

In general, the performance of all circuits demonstrated herein can be slightly improved by increasing the gate voltage (also denoted input signal or control signal) from 1 V to 1.2 V, since this will result in shorter switching times. However, this typically also shortens the operational lifetime of the transistors, in particular the C-C OECTs.

3.4. Simulations of circuits based on OECTs

By utilizing the developed OECT SPICE models, it is possible to simulate the characteristics of circuits based on the OECTs. Figure 11 presents the simulations of the printed circuits that have been evaluated; inverter, two-input NAND, 2-to-4 decoder and 4-to-1 multiplexer. The simulations give the correct voltage levels for all the logic circuits when comparing with the measured data, which is of major importance. However, the fluctuating waveforms that are observed in the measurements are not included in the simulated graphs; this is due to the fact that the complex electrochemical kinetics of the OECTs are essentially different from the silicon depletion mode MOS transistors. Additionally, the switching response of the OECTs is slower in the circuits, as compared to the measured transistor characteristics of the standalone OECTs shown in figure 3. This is explained by the resistors that are used in the circuits to define the voltage output level; the larger resistor values, the slower switching response of the OECT-based circuit, while the
Figure 10. The characteristics of two printed 4-to-1 multiplexers (MUX) are shown. The circuits are based on either the C-C OECT design (left) or the P-P OECT design (right). The frequency of the output voltage follows the frequency of the selected input voltage signal in the case of the C-C design. However, for the P-P OECT design, the output voltage signal is clearly delayed when $V_{IN3}$ and especially $V_{IN4}$, the input voltage signals having the lowest frequencies, were selected.

Figure 11. SPICE simulations of the OECT-based circuits: Inverters (a), the two-input NAND gates (b), the 2-to-4 decoder based on the C-C OECT design (c), and the 4-to-1 multiplexer (MUX) based on the C-C OECT design (d).
standalone OECTs are characterized without any resistors.

4. Conclusions

The possibility to manufacture electronic circuits based on vertically arranged OECTs solely using screen printing equipment has been demonstrated. Two different device architectures were used when printing standalone OECTs as well as various kinds of circuits, and it is concluded that the two architectures behave relatively similarly during short periods of operation. However, for longer cycling periods it become more obvious that the P-P OECT design suffers from the reduction front, as evidenced by the prolonged switching time. On the other hand, the C-C OECT design is more sensitive to gate voltages above 1 V, which results in a shorter operational lifetime. Hence, there is a trade-off when comparing the two OECT designs, and the requirement of each specific application will eventually serve as guidance on choosing the most appropriate OECT design. Low-voltage operation and high manufacturing yield are promising parameters that could enable fully integrated printed electronic systems in e.g. smart sensor label applications. Concurrent with printing trials and device characterization, SPICE models were also developed. These models will simplify future circuit designs through simulations.

Acknowledgments

This work was supported by EUREKA Eurostars (PROLOG, Project ID: 7301) and the Swedish Foundation for Strategic Research (Silicon-Organic Hybrid Autarkic Systems, Reference number: SE13-0045).

ORCID iDs

Peter Andersson Ersman  https://orcid.org/0000-0002-4575-0193

References

[1] Smart Label Sensors—Thin Film Electronics (accessed: 17 July 2017) http://thinfilm.no/products-sensor-platform
[2] 2017 ThinFilm Memory—Thin Film Electronics (accessed: 17 July 2017) http://thinfilm.no/products-memory/
Digital Labels—Xerox (accessed 17 July 2017) https://xerox.com/en-us/insights/digital-labels
[3] Zhao W, Qian D, Zhang S, Li S, Ingaņās O, Gao F and Hou J 2016 Adv. Mater. 28 4743
Krebs F C 2009 Sol. Energy Mater. Sol. Cells 93 394
[4] Gaikwad A M, Arias A C and Steingart D A 2015 Energy Technol. 3 305
[5] Pettersson F, Keskinen J, Remonen T, von Hertzen L, Jansson E, Tappura K, Zhang Y, Wil C E and Österbacka R 2014 J. Power Sources 271 298
[6] Sani N et al 2014 Proc. Natl. Acad. Sci. USA 111 11943
[7] Mattana G and Briand D 2016 Materials Today 19 88
[8] Choi C H, Lin L Y, Cheng C-C and Chang C-H 2015 ECS J. Solid State Sci. Technol. 4 3044
Kim S H, Hong K, Xie W, Lee K H, Zhang S, Lodge T P and Frisbie C D 2013 Adv. Mater. 25 1822
Kang B, Lee W H and Cho K 2013 ACS Appl. Mater. Interfaces 5 2302
Tobjörk D, Kählhvirts NJ, Mäkelä T, Pettersson F S and Österbacka R 2008 Org. Electron. 9 931
[9] Acreo Display—RISE Acreo (accessed: 17 July 2017) https://acreo.se/expertise/acreo-display
[10] Sirringhaus H 2014 Adv. Mater. 26 1319
[11] Zhang M, Lin P, Yang M and Yan F 2013 Biosimilacs et Biophysica Acta (BBA)—Gen. Subjects 1830 4402
Rothlander T, Hutter P C, Renner E, Gold H, Haase A and Stadlober B 2014 IEEE Trans. on Electron Devices 61 1515
Mannerbo R, Ranlof M, Robinson N D and Forchheimer R 2008 Synth. Met. 158 536
Hutter P C, Fian A, Gatterer K and Stadlober B 2016 ACS Appl. Mater. Interfaces. 8 14071
Scheiblin G, Alane A, Strakosas X, Curto V F, Coppard R, Marchand G, Owens R M, Mailely P and Malliaras G G 2015 MRS Com Show. 5 507
Kawahara J, Andersson Ersman P, Katoh K and Berggren M 2013 IEEE Trans. on Electron Devices 60 2052
Zhang S, Hubis E, Tomasellos G, Soliveri G, Kumar P and Cicoira F 2017 Chem. Mater. 29 3126
[12] Zhang Q, Majumdar H S, Kaisti M, Prabhu A, Ivaska A, Österbacka R, Rahman A and Levon K 2015 IEEE Trans. Electron Devices 62 1291
[13] Hutter P C, Rothlander T, Scheipl G and Stadlober B 2015 IEEE Trans. Electron Devices 62 4231
[14] Khodagholy D, Gurfinkele M, Stavrinidoue E, Leleux P, Herve T, Sanaur S and Malliaras G G 2011 Appl. Phys. Lett. 99 163304
[15] Andersson Ersman P, Nilsson D, Kawahara J, Gustafsson S and Berggren M 2013 Org. Electron. 14 1276
[16] Berggren M, Simon D T, Nilsson D, Dreykele P, Norberg P, Nordlander S, Andersson Ersman P, Gustafsson G, Wikner J J, Hederen J and Hentzell H 2016 Adv. Mater. 28 1911
[17] Isaksson J, Kjäll P, Nilsson D, Robinson N D, Berggren M and Richter-Dahlfors A 2007 Nat. Mater. 6 673
[18] Argun A A, Aubert P H, Thompson B C, Schwendeman I, Gaupp C L, Hwang I, Pinto N J, Tanner D B, MacDiarmid A G and Reynolds J R 2004 Chem. Mater. 16 4401
[19] Inal S, Rivnay J, Hofmann A I, Uguz I, Mumtaz M, Katsiannopoulou S, Brochon C, Cloutet E, Hadziioannou G and Malliaras G G 2015 J. Polym. Sci. B 54 147
[20] Johansson T, Persson N-K and Ingaņās O 2004 J. Electrochem. Soc. 151 E119
[21] Berggren M, Forscheheimer R, Bobacka J, Svensson P-O, Nilsson D, Larsson O and Ivaska A 2008 PEDOT·PSS-Based Electrochemical Transistors for Ion-to-Electron Transduction and Sensor Signal Amplification Organic Semiconductors in Sensor Applications (Berlin: Springer)