Acceleration of tensor-product operations for high-order finite element methods.

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Abstract

This paper is devoted to GPU kernel optimization and performance analysis of three tensor-product operators arising in finite element methods. We provide a mathematical background to these operations and implementation details. Achieving close-to-the-peak performance for these operators requires extensive optimization because of the operators’ properties: low arithmetic intensity, tiered structure, and the need to store intermediate results inside the kernel. We give a guided overview of optimization strategies and we present a performance model that allows us to compare the efficacy of these optimizations against an empirically calibrated roofline.

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1 Introduction

State-of-the-art high-order finite element method (FEM) based simulation codes now execute calculations on parallel machines with up to a million CPU cores. For example, the Nek5000 incompressible fluid flow simulator has successfully scaled up to a million CPU cores using an MPI distributed computing model ((Fischer et al., 2015)). The current shift towards greater on-chip parallelism makes it imperative to focus on finer grain parallel implementation of high-order operators on next generation accelerators, such as Graphics Processing Units (GPUs). Efficient high-order finite element implementations rely heavily on tensor-product contractions ((Deville et al., 2002)). These elemental tensor-product operations are memory bound and require repeated sweeps through the data for each finite element operation. In this work we demonstrate that despite their complexity, it is possible to achieve nearly maximum throughput on a current generation GPU.

In this paper we focus in particular on GPU implementations of three common place matrix-vector multiplications (further abbreviated as matvecs) arising in finite element codes: mass matvec (BP1.0), stiffness matvec (BP3.5), and stiffness matvec that involves de-aliasing integration (BP3.0). These problems have been formulated as a part of CEED co-design effort ((CEED, 2017)). BP1.0, BP3.5, and BP3.0 appear to be potentially well-suited for fine-grain parallelism but they are challenging to fully optimize. These benchmarks are characterized by low arithmetic intensity, namely that the ratio of floating point operations (FLOPS) to data transfer is low. The benchmarks also require non-unitarily strided memory access patterns since all threads that are processing a single element need the data computed by other threads that process this element. Finally, the operations consist of several concatenated tensor-product contractions and all threads simultaneously process the contractions in a prescribed order.

We detail several strategies that are collectively applied to maximize the computational throughput of these operations. In a sequence of computational experiments we progressively optimize the operations by varying the amount of global memory accesses, shared memory usage, register variable usage, data padding, and loop unrolling.

To guide the optimization process we construct a performance model that serves as a tool to evaluate the efficiency of the kernels. Because of the nature of the finite element operations, the performance of our kernels is limited by the bandwidth of the data streaming from both the global device memory and shared memory as well as finite register file and shared memory capacity. While a theoretical performance roofline, as presented by (Lo et al., 2014), gives an upper bound on the capability of the hardware under ideal circumstances, we instead rely on an empirically calibrated roofline model that provides a realistic estimate of the best achievable performance.

1.1 Overview of published literature

Early optimization studies of FEM operations date back to 2005 when (Gödeke et al., 2005) and (Gödeke et al. 2007) solved elliptic PDEs on two-dimensional domains using a cluster equipped with GPU accelerators. In later work, (Gödeke et al., 2009) focused mostly on accelerating the Navier-Stokes solver for lid driven cavity and laminar flow over a cylinder. The study presented by (Fu et al., 2014) targeted the entire FEM pipeline using the elliptic Helmholtz problem to show how the FEM codes are ported to the GPU. In addition, (Fu et al., 2014) discussed strategies for
accelerating conjugate gradient and algebraic multigrid solvers.

Other authors usually choose to work on improving the performance of one part of the FEM pipeline. For example, (Cecka et al., 2011) and (Markall et al., 2013) focused on the global assembly phase of FEM and showed how to optimize this phase for GPU execution. Markall and co-authors emphasize that the choice of the most efficient algorithm strongly depends on the available hardware and selected programming model. In their work, Markall and co-authors considered the CPU and the GPU with OpenCL and CUDA parallel implementations. Moreover, (Markall et al., 2010, 2013) argue that making the code portable between different threading systems (such as many-core and multi-core architectures) requires a high-level programming language.

In all of the above work the greatest concern was efficiently pipelining GPU execution of FEM with low-order discretizations. In contrast, (Remacle et al., 2016) present algorithms for solving elliptic equations using high-order continuous hexahedral finite elements on the GPUs. The issues associated with efficiently handling the greater complexity of high-order FEM operations highlighted in that work are amplified in the current paper and refined with the use of a new roofline model.

The evaluation of the \texttt{matvec} typically accounts for the highest cost of the elliptic FEM solver (Remacle et al., 2016 Table 2, Table 3). Optimization of \texttt{matvec} performance on the GPUs appears in the literature mostly in the context of general applications. Yet a few papers focused directly on the low-order FEM \texttt{matvec}. For example, (Dziekonski et al., 2017) used a conjugate gradient solver and optimized \texttt{matvec} product as its important part. (Dehnavi et al., 2010) and (Grigoras et al., 2016) present similar findings and provided optimization strategies. However, in our case the action of the operator is local to the element. We never assemble the global matrix and we perform the element-wise \texttt{matvec}. In the literature this approach is known as \textit{matrix-free} approach.

The \texttt{matvecs} used in this paper can be expressed as a concatenation of tensor contractions. Related work on efficient implementation of tensor contractions for the GPUs consists of several papers. (Nelson et al., 2015) applied high level language to formulate tensor contractions and used GPU code auto-tuning to enhance the performance of the code. The findings were tested using several benchmark problems, including a problem derived from Nek5000 (see (Paul F. Fischer and Kerkemeier, 2008)). Optimized code reached 120 GFLOPS/s on a Maxwell class GPU. (Abdelfattah et al., 2016) published similar work where, in addition to specifying high-level language to formulate tensor contractions, the authors introduced a performance model based on both the number of floating point operations and the number of bytes of global memory that need to be read and written. The performance results were compared to CUBLAS and to CPU code executed using 16 CPU cores. The most efficient version of the code reaches 180 GFLOPS/s on NVIDIA Tesla K40 GPU. While two previously mentioned papers focused on small tensor contractions, (Liu et al., 2017) optimized large tensor contractions, also using auto-tuning for performance optimization. The paper explained the details of the implementation and reported the global memory usage.

The performance model in this paper is rooted in earlier work by several authors, originating from the \textit{roofline model} in (Lo et al., 2014). (Stratton et al., 2012) and (Zhang and Owens, 2011) who modeled the GPU performance using benchmarks. These efforts focused on a semi-automatic way of identifying performance bottlenecks. Acquiring a more complete understanding of the performance of the code on the GPU and designing benchmark specifically to reveal the underlying hardware properties frequently appears in the literature due to lack of available complete GPU hardware documentation. At the same time, hardware organization strongly impacts the performance ((Volkov and Demmel, 2006)).
Table 1: The notation used in in the paper. The first column shows the symbols used in pseudocode listings and the second column shows the symbols used in the derivations.

| Symbol       | Code | Math        | Meaning                                                                 |
|--------------|------|-------------|-------------------------------------------------------------------------|
| N            | N    | N           | Degree of the polynomial used in the interpolation                      |
| Nq           | Nq   | Nq          | Number of Gauss-Lobatto-Legendre (GLL) quadrature nodes: Nq = N + 1       |
| Np           | Np   | Np          | Number of GLL nodes in a hexahedral element: Np = Nq^3                  |
| glnNq        | NGLq | NGLq        | Number of Gauss-Legendre (GL) quadrature nodes: NGLq = N + 2             |
| glnNp        | NGLp | NGLp        | Number of GL nodes in a hexahedral element. NGLp = (NGLq)^3              |
| I            | I^1D | I^1D        | (N + 2) × (N + 1) interpolation matrix from GLL nodes to GL nodes       |
| D            | D^1D | D^1D        | (N + 1) × (N + 1) differentiation matrix used in BP3.5, see (9)          |
| glD          | D^1D | D^1D        | (N + 2) × (N + 2) differentiation matrix, used in BP3.0                 |
| NElements    | Nel  | Nel         | Number of elements in the mesh                                           |

2008 and Volkov 2010 employed a different approach; they optimized matrix-matrix multiplication on the GPU and aimed to explain the code performance while improving the implementation. In his 2010 paper, Volkov pointed out that, contrary to a common belief, high GPU occupancy is not necessary to obtain close the peak performance declared by the GPU manufacturer. This observation is important for the current paper. Our most efficient kernels are characterized by high usage of registers and shared memory, thus the achieved occupancy can often be as low as 10% even though the performance of these kernels is close to the empirical roofline. Volkov observation that the aggregate number of shared memory accesses per thread should be reduced to avoid bottlenecks motivates a final optimization for the high-order FEM operations considered in this work. We exploit the intrinsic structure of the interpolation and differentiation tensors used in the construction of the action of the mass and stiffness matrices to improve throughput by reducing the aggregate number of shared memory accesses.

The remainder of this paper is organized as follows. We first present the mathematical description of the three benchmark problems mentioned earlier. We then introduce the performance model we use to evaluate our kernels. We continue by explaining the implementation and optimization choices for each of the benchmark problems. Finally, we gives some concluding remarks and future goals.

2 Notation

The notation used throughout this paper is shown in Table 1. In addition, we define

\[ 1 \text{ TFLOPS} = 10^{12} \text{ FLOPS} \]

The floating point throughput rates for compute kernels in this paper are reported using TFLOPS/s. We use double precision arithmetic in all the tests.
3 Hardware and software

All computational studies in this paper were performed on a single Tesla P100 (Pascal class) PCI-E GPU with 12 GB RAM and maximum theoretical bandwidth of 549 GB/s. The GPU is hosted by a server node equipped with Intel Xeon E5-2680 v4 processor, 2.40 Ghz with 14 cores. The code was compiled using the gcc 5.2.0 compiler and the nvcc CUDA compiler release 8.0, V8.0.61 managed by the OCCA library (see (Medina et al., 2014)).

We compute the reference times (needed for copy bandwidth in roofline plots) using CUDA events. The kernels are timed using MPI_Wtime.

In our experiments, we test the code on two hexahedral cube-shaped meshes. The small mesh consists of 512 elements and the large mesh consists of 4096 elements.

4 Problem description

The three benchmark problems we consider below were formulated by the Center for Efficient Exascale Discretizations (see (CEED, 2017)). These problems are motivated by considering the numerical approximation of the screened Poisson equation

\[-\nabla^2 u + \lambda u = f,\]

by a high-order finite element method on hexahedral elements. In the equation, \(f\) is a given forcing function and \(\lambda\) is a constant. To begin we consider an unstructured mesh of a domain \(D \subset \mathbb{R}^3\) into \(K\) hexahedral elements \(D^e\), where \(e = 1, \ldots, K\), such that

\[D = \bigcup_{e=1}^{K} D^e.\]

We assume that each hexahedral element \(D^e\) with vertices \(\{x_n, y_n, z_n\}_{n=1}^{8}\) is the image of the reference bi-unit cube \(\hat{D}\) under a tri-linear map. We take the reference cube to be the bi-unit cube, i.e.

\[\hat{D} = \{(r, s, t) : -1 \leq r, s, t \leq 1\}.

On each element we consider the variational form of the screened Poisson problem (1) on element \(D^e\) by requiring that \(u\) satisfies

\[\int_{D^e} \nabla v \cdot \nabla u \, dV + \lambda \int_{D^e} vu \, dV = \int_{D^e} vf \, dV.\]

for all test functions \(v \in H^1(D^e)\). We map the integrals to the reference cube \(\hat{D}\) in order to write the variational form as

\[\int_{\hat{D}} \nabla v^T G^e \nabla u^e \, dV + \lambda \int_{\hat{D}} v u^e \, |J^e| \, dV = \int_{\hat{D}} v f^e \, |J^e| \, dV.\]

where \(|J^e|\) is the determinant of the Jacobian \(J^e\) of the mapping from element \(D^e\) to the reference cube \(\hat{D}\) and \(G^e = |J^e|(J^e)^T J^e\) is the scaled elemental metric tensor. The \(\nabla\) operators in these integrals are now understood to be in \((r, s, t)\)-space.
On the reference cube $\hat{D}$ we construct a high-order finite element approximation of the function $u$, denoted $u^e$, which is a degree $N$ polynomial in each dimension. We denote the space of all such polynomials as $Q^N(\hat{D})$. As a polynomial basis of $Q^N(\hat{D})$ we choose the tensor product of one-dimensional Lagrange interpolation polynomials $\{l_i\}_{i=0}^{N}$ based on $N+1$ Gauss-Lobatto-Legendre (GLL) nodes on the interval $[-1,1]$. We denote the GLL nodes in $[-1,1]$ by $\{r_i\}_{i=0}^{N}$, and use an analogous notation for the GLL nodes in the $s$ and $t$ dimensions. Using a multi-index, we define the multi-dimensional basis polynomials $l_{ijk}(r,s,t)$ to be the tensor product of the one-dimensional Lagrange interpolating polynomials, i.e. $l_{ijk}(r,s,t) = l_i(r)l_j(s)l_k(t)$, for all $0 \leq i,j,k \leq N$. Consequently, the coefficients $u^e_{ijk}$ are the nodal values of the polynomial $u^e$ at the GLL interpolation points $(r_i,s_j,t_k)$, i.e., $u^e_{ijk} = u^e(r_i,s_j,t_k)$.

Taking the test functions $v$ to be each of the basis Lagrange interpolating polynomials, $v = l_{i'j'k'}(r,s,t)$, and taking the vector $u^e$ to be the vector of the polynomial coefficients of $u^e$, i.e. $u^e = [u^e_{000}, u^e_{001}, \ldots, u^e_{NNN}]^T$, we can write the variational formulation as the following linear system

$$S^e u^e + \lambda M^e u^e = f^e$$

where the local stiffness matrix $S^e$, local mass matrix $M^e$, and local load vector $f^e$ are defined as

$$S^e_{ijk,i'j'k'} = \int_{\hat{D}} (\nabla l_{i'j'k'})^T G^e \nabla l_{ijk} \, dV,$$

$$M^e_{ijk,i'j'k'} = \int_{\hat{D}} l_{i'j'k'} l_{ijk} |J^e| \, dV,$$

$$f^e_{i'j'k'} = \int_{\hat{D}} l_{i'j'k'} f |J^e| \, dV.$$

We concatenate the local stiffness and mass matrix operators as well as local load vectors to form global unassembled versions which we denote, $S$, $M$ and $f$, respectively. Doing so, we form the following a block diagonal system which operators on the global vector of solution coefficients, which we denote $u$,

$$Su + \lambda Mu = f.$$ 

Due to its block diagonal structure, these global stiffness and mass matrix operators can be applied in a matrix-free (element-wise) way and no communication is required between elements.

The benchmarks presented below consider the efficient action of either just the mass matrix $M$ or the complete screened Poisson operator $S + \lambda M$ on each element. Benchmark problem 1.0 and 3.0 consider the case where the integrals (3)-(4) are evaluated using a full Gauss-Legendre (GL) quadrature and benchmark problem 3.5 considers the case where the integrals are approximated using simply a quadrature at the GLL interpolation points.
4.1 Benchmark Problem 1: Mass Matrix Multiplication

The first benchmark we present involves matrix-vector product of the high-order finite element mass matrix $M$ and a corresponding vector. This operation is a component of finite element elliptic operators and some preconditioning strategies. Thus, it serves as a useful initial performance benchmark. The operation requires relatively little data transfers compared with more demanding differential operators which necessitate loading the elemental metric tensor for each node of the element, as discussed in later benchmarks.

Beginning from the integral definition of the entries of the local mass matrix $M_e$ in (4) we use the fact that $\hat{D}$ is the reference cube to evaluate the integral in each dimension separately via an $N_{GL}^q$-node Gauss-Legendre (GL) quadrature. We denote the quadrature weights and nodes in the $r$ dimension as $\{\tilde{w}_a\}_{a=1}^{N_{GL}^q}$ and $\{\tilde{r}_a\}_{a=1}^{N_{GL}^q}$, respectively, and use an analogous notation for quadrature nodes in the $s$ and $t$ dimensions. Thus we can write

$$M_{ijk,ij'k'}^{e} = \sum_{a=1}^{N_{GL}^q} \sum_{b=1}^{N_{GL}^q} \sum_{c=1}^{N_{GL}^q} \tilde{w}_a \tilde{w}_b \tilde{w}_c | J^e(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c) | l_{ij} l_{jk} l_{ik'} | l_{ij'} l_{jk} l_{ik} | l_{ijk}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c).$$  \hspace{1cm} (6)

We can write this expression in matrix form by defining the interpolation operator,

$$I_{abc,ijk} = l_{ijk}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c),$$

for all $i,j,k = 0,\ldots,N$ and $a,b,c = 1,\ldots,N_{GL}^q$, as well as the diagonal matrix $J^e$ of weights and geometric data which gives entries

$$J_{abc,abc}^e = \tilde{w}_a \tilde{w}_b \tilde{w}_c | J^e(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c)|,$$

for all $a,b,c = 1,\ldots,N_{GL}^q$ in order to write the local mass matrix [6] compactly as

$$M^e = I^T J^e I.$$

Note that since the basis interpolation polynomials are a tensor products of one-dimensional polynomials, we can define the one-dimensional interpolation matrix $I^{1D}$ as

$$I_{ai}^{1D} = l_i(\tilde{r}_a),$$

for all $i = 0,\ldots,N$ and $a = 1,\ldots,N_{GL}^q$, in order to express the interpolation operator $I$ as a tensor product of the one-dimensional operators, i.e.

$$I = I^{1D} \otimes I^{1D} \otimes I^{1D}.$$

Thus, the interpolation operation from the GLL interpolation nodes to the GL quadrature nodes can be applied using three tensor contractions, while the projection back to the GLL nodes via the transpose interpolation operator comprises three additional tensor contractions. Since the remaining operation is simply the multiplication by the diagonal matrix $J^e$ no further tensor contractions are required. Since we will make use of the interpolation and projection operations again in BP3.0 below, we detail their pseudo code in Algorithms 1 and 2. We then detail the full matrix free action of the mass matrix in the pseudo code in Algorithm 3.
Algorithm 1. Interpolation from GLL to GL nodes

1: **Data:** (1) $q^e$, size $N_p$; (2) Interpolation matrix $I^{1D}$, size $N_q^{GL} \times N_q$
2: **Output:** $\tilde{q}^e$, size $N_p^{GL}$
3: for $c, a \in \{1, \ldots, N_q\}$, $j \in \{1, \ldots, N_q^{GL}\}$ do
4: $\tilde{q}^e_{cja} = \sum_{b=1}^{N_q} I^{1D}_{jb} q^e_{cba}$ $\triangleright$ Interpolate in $b$ direction
5: end for
6: for $c \in \{1, 2, \ldots, N_q\}$, $i, j \in \{1, 2, \ldots, N_q^{GL}\}$ do
7: $\tilde{q}^e_{cja} = \sum_{a=1}^{N_q} I^{1D}_{ia} q^e_{cja}$ $\triangleright$ Interpolate in $a$ direction
8: end for
9: for $k, i, j \in \{1, 2, \ldots, N_q^{GL}\}$ do
10: $\tilde{q}^e_{kji} = J^e_{kji} \sum_{c=1}^{N_q} I^{1D}_{kc} \tilde{q}^e_{cji}$ $\triangleright$ Interpolate in $c$ direction, save
11: end for

Algorithm 2. Projection from GL to GLL nodes

1: **Data:** (1) $\tilde{q}^e$, size $N_p^{GL}$; (2) Interpolation matrix $I^{1D}$, size $N_q^{GL} \times N_q$
2: **Output:** $q^e$, size $N_p$
3: for $k, i \in \{1, 2, \ldots, N_q^{GL}\}$, $b \in \{1, 2, \ldots, N_q\}$ do
4: $\hat{q}^e_{kbi} = \sum_{j=1}^{N_q^{GL}} I^{1D}_{jb} \tilde{q}^e_{kji}$ $\triangleright$ Project in $b$ direction
5: end for
6: for $k \in \{1, 2, \ldots, N_q^{GL}\}$, $b, a \in \{1, 2, \ldots, N_q\}$ do
7: $\hat{q}^e_{kja} = \sum_{i=1}^{N_q} I^{1D}_{ia} \hat{q}^e_{kbi}$ $\triangleright$ Project in $a$ direction
8: end for
9: for $c, b, a \in \{1, 2, \ldots, N_q\}$ do
10: $q^e_{cba} = \sum_{k=1}^{N_q^{GL}} I^{1D}_{kc} \hat{q}^e_{kba}$ $\triangleright$ Project in $c$ direction, save
11: end for

4.2 Benchmark Problem 3.5: Stiffness Matrix with Collocation Differentiation

For our second benchmark, we consider the matrix-vector product of the full high-order finite element screened Poisson operator $S + \lambda M$ and a corresponding vector. In this benchmark, the operators $S$ and $M$ are evaluated using a collocation GLL quadrature rather than the more accurate GL quadrature used in the other two benchmark problems. This operation is central to many elliptic finite element codes and is usually a part of a discrete operator we wish to invert. For example, incompressible flow solvers such as Nek5000 (see (Paul F. Fischer and Kerkemeier, 2008)) require solving a Poisson potential problem at each time step. Consequently, this *matvec* is potentially evaluated many times in each time step of a flow simulation, making its optimization a significant factor for good performance.

To describe the application of the full screened Poisson operator we begin by describing the local stiffness matrix $S^e$ defined in (3). We evaluate the integral in (3) in each dimension separately, this time using the $N+1$ GLL interpolation nodes as the quadrature. We denote the GLL quadrature weights and nodes in the $r$ dimension as $\{w_a\}_{a=0}^{\lambda=N}$ and $\{r_a\}_{a=0}^{\lambda=N}$, respectively, and use an analogous
Algorithm 3. BP1.0: mass matrix multiplication

1. **Data:** (1) \( q \), size \( N_{el} \cdot N_p \); (2) Interpolation matrix \( I^{1D} \), size \( N^q_{GL} \times N_q \); (3) Scaled Jacobians, \( J \), size \( N_{el} \times N^G_{p} \)
2. **Output:** \( M_q \), size \( N_{el} \cdot N_p \)
3. for \( e \in \{1, 2, \ldots N_{el}\} \) do
   4. \( \tilde{q}^e = \text{Interpolate}(q^e, I^{1D}) \) \( \triangleright \) Interpolate to GL nodes (Algorithm 1)
   5. for \( k, i, j \in \{1, 2, \ldots N^G_{q}\} \) do
      6. \( \tilde{q}^e_{kji} = J^e_{kji} \tilde{q}^e_{kji} \) \( \triangleright \) Scale by Jacobian and integration weights
   7. end for
   8. \( q^e = \text{Project}(\tilde{q}^e, I^{1D}) \) \( \triangleright \) Project to GLL nodes (Algorithm 2)
9. end for

notation for the GLL quadrature nodes in the \( s \) and \( t \) dimensions. Thus we can write

\[
S^e_{ijk,i''j''k''} = \sum_{a=0}^{N} \sum_{b=0}^{N} \sum_{c=0}^{N} w_a w_b w_c (\nabla l_{i'j'k'}(r_a, s_b, t_c))^T G^e(r_a, s_b, t_c) \nabla l_{ijk}(r_a, s_b, t_c).
\] (8)

To write this expression in a more compact matrix form we begin by defining the differentiation operators,

\[
D^r_{abc,ijk} = \frac{\partial l_{ijk}}{\partial r}(r_a, s_b, t_c),
D^s_{abc,ijk} = \frac{\partial l_{ijk}}{\partial s}(r_a, s_b, t_c),
D^t_{abc,ijk} = \frac{\partial l_{ijk}}{\partial t}(r_a, s_b, t_c),
\] (9)

for \( i, j, k, a, b, c = 0, \ldots N \). We then define the gradient operator \( D \) to be the vector of these three derivative operators, i.e. \( D = [D^r, D^s, D^t]^T \). Next, since \( G^e \) is the scaled metric tensor on element \( D^e \) defined by \( G^e = |J^e|(J^e)^T J^e \), we denote the entries of \( G^e \) as

\[
G^e = \begin{pmatrix}
G^e_{rr} & G^e_{rs} & G^e_{rt} \\
G^e_{sr} & G^e_{ss} & G^e_{st} \\
G^e_{tr} & G^e_{ts} & G^e_{tt}
\end{pmatrix},
\]

We define a matrix \( G^e \) of operators where each entry of \( G^e \) is a diagonal matrix of weights and geometric data from \( G^e \). That is, we define

\[
G^e = \begin{pmatrix}
G^e_{rr} & G^e_{rs} & G^e_{rt} \\
G^e_{sr} & G^e_{ss} & G^e_{st} \\
G^e_{tr} & G^e_{ts} & G^e_{tt}
\end{pmatrix},
\] (10)

where each entry, say \( G^e_{rr} \), is defined as a diagonal matrix which has entries

\[
(G^e_{rr})_{abc,abc} = w_a w_b w_c G^e_{rr}(r_a, s_b, t_c),
\]
Algorithm 4. BP3.5: collocation differentiation for 3D hexahedral mesh

1: **Data:** (1) Vector \( q \), size \( N_{el} \times N_p \), (2) differentiation matrix \( D^{1D} \), size \( N_q \times N_q \), (3) geometric factors \( G \), size \( N_{el} \times N_p \times 7 \), (4) parameter \( \lambda \);
2: **Output:** Vector \( S_q \), size \( N_{el} \times N_p \);
\[ \text{▷ Loop over elements ↓} \]
3: for \( e \in \{1, 2, \ldots, N_{el}\} \) do
   4: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do
      5: \( G_{rr} = G_{1:i,j,k}^e \), \( G_{rs} = G_{2:i,j,k}^e \), \( G_{rt} = G_{3:i,j,k}^e \);
      6: \( G_{ss} = G_{4:i,j,k}^e \), \( G_{st} = G_{5:i,j,k}^e \), \( G_{tt} = G_{6:i,j,k}^e \);
\[ \text{▷ Multiply by } D \]
   7: \( qr = \sum_{n=1}^{N_q} D^{1D}_{in} q^e_{kjn} \);
   8: \( qs = \sum_{n=1}^{N_q} D^{1D}_{jn} q^e_{kin} \);
   9: \( qt = \sum_{n=1}^{N_q} D^{1D}_{kn} q^e_{nji} \);
\[ \text{▷ Apply chain rule ↓} \]
   10: \( rqr^e_{ijk} = G_{rr}*qr + G_{rs}*qs + G_{rt}*qt \);
   11: \( rqs^e_{ijk} = G_{rs}*qr + G_{ss}*qs + G_{st}*qt \);
   12: \( rqt^e_{ijk} = G_{rt}*qr + G_{st}*qs + G_{tt}*qt \);
5: end for
   6: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do
      7: \( J = G_{i,j,k}^e \)
   8: \( S_q^e_{ijk} = \lambda q^e_{q_{kji}} + \sum_{n=1}^{N_q} D^{1D}_{in} rqr^e_{kjn} + D^{1D}_{jn} rqs^e_{kin} + D^{1D}_{kn} rqt^e_{nji} \);
5: end for
6: end for

for \( a, b, c = 0, \ldots, N \). We use analogous definitions for the remaining entries of \( G^e \). Using these matrix operators we can write the local stiffness matrix \( [S] \) compactly as follows
\[ S^e = D^T G^e D. \]

To simplify the action of this local stiffness matrix we again use the fact that the basis interpolation polynomials are a tensor products of one-dimensional polynomials. We define the one-dimensional differentiation matrix \( D^{1D} \) as
\[ D^{1D}_{ia} = l_i(r_a), \]
for all \( i, a = 0, \ldots, N \). Using this one-dimensional derivative operator, and the fact that the GLL quadrature nodes collocate with the interpolation nodes using the define the Lagrange basis polynomials \( l_i \), we write the partial derivative matrices \( D^r, D^s, \) and \( D^t \) as tensor products of \( D^{1D} \) and the identity matrix \( I \) as follows
\[ D^r = D^{1D} \otimes I \otimes I, \]
\[ D^s = I \otimes D^{1D} \otimes I, \]
\[ D^t = I \otimes I \otimes D^{1D}. \]
Thus, differentiation along each dimension can be computed using single tensor contractions.
Finally, to write the full action of the local screened Poisson operator $S^e + \lambda M^e$ we note that since we have use the collocation GLL quadrature in the evaluation of the integrals \((3)-(4)\), we can follow the description of the mass matrix operator above to find that no interpolation is required and the mass matrix can be written simply as $M^e = J e$ where the matrix of geometric factors $J e$ is now defined using the GLL weights and quadrature points, i.e.

$$J_{abc;abc}^e = w_a w_b w_c |J^e(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c)|,$$

for $a, b, c = 0, \ldots, N$. Thus we write the local screened Poisson operator as

$$S^e + \lambda M^e = D^T G^e D + \lambda J^e$$

This operator can be applied using only six tensor contractions. First, we apply the $D$ operator by differentiating along each dimension using three tensor contractions. We then multiply by the necessary geometric factors $G^e$ and apply the transpose operator $D^T$ with three more tensor contractions. Finally we add the mass matrix contribution which requires no tensor contractions. We detail the full matrix-free action of the screened Poisson operator in the pseudo code in Algorithm 4.

4.3 BP3.0: Stiffness matrix evaluated with quadrature

The final benchmark we consider is the same matrix-vector product of the high-order screened Poisson operator $S + \lambda M$ as in BP3.5. This time, however, we use the full GL quadrature to approximate the integrals in \((3)\) and \((4)\). This benchmark combines computational elements from BP1.0 and BP3.5 which makes for a more arithmetically intense kernel and maximizing its performance on GPUs is challenging.

We again begin by describing the local stiffness matrix $S^e$ defined in \((3)\). We evaluate the integral in \((3)\) in each dimension separately, this time using the full GL interpolation nodes as the quadrature. Using the notation introduced in BP1.0 above, we write

$$S^e_{ijk,i'j'k'} = \sum_{a=1}^{N_{GL}^q} \sum_{b=1}^{N_{GL}^q} \sum_{c=1}^{N_{GL}^q} \tilde{w}_a \tilde{w}_b \tilde{w}_c (\nabla l_{i'j'k'}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c))^T G^e(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c) \nabla l_{ijk}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c). \quad (11)$$

Note here that the quadrature requires the gradients of the basis polynomials $l_{ijk}$ to be evaluated at the GL quadrature nodes. Were we to simply compose the interpolation and differentiation operators $I$ and $D$ defined in BP1.0 and BP3.5 above we would require nine tensor contractions to evaluate this quantity. Indeed, for each of the $r$, $s$, and $t$ derivatives of $l_{ijk}$, we would require an operation which combines differentiation and interpolation to the GL quadrature along one dimension and only interpolation to the GL quadrature along the remaining two dimensions.

We instead reduce the number of required tensor contractions by considering the Lagrange interpolating polynomials $\tilde{l}_a(r)$ for $a = 1, \ldots, N_{GL}^q$ which interpolate the GL quadrature nodes. We define the tensor product basis polynomials as done for the GLL interpolating basis as

$$\tilde{l}_{abc}(r, s, t) = \tilde{l}_a(r) \tilde{l}_b(s) \tilde{l}_c(t),$$

which
for \( a, b, c = 1, \ldots, N^{GL}_q \). We then define the derivative operators, as done above for the GLL interpolating Lagrange basis functions, on this set of polynomials as follows

\[
\tilde{D}^r_{abc,a'b'c'} = \frac{\partial \tilde{r}^{a'b'c'}}{\partial r}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c),
\]

\[
\tilde{D}^s_{abc,a'b'c'} = \frac{\partial \tilde{r}^{a'b'c'}}{\partial s}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c),
\]

\[
\tilde{D}^t_{abc,a'b'c'} = \frac{\partial \tilde{r}^{a'b'c'}}{\partial t}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c),
\]

for \( a, b, c, a', b', c' = 1, \ldots, N_q \). We can then construct the gradient operation on this set of basis function as \( \tilde{D} = [\tilde{D}^r, \tilde{D}^s, \tilde{D}^t]^T \). Thus, if we view the interpolation operators defined in (7) as transforming a polynomial from the basis of Lagrange interpolating polynomials on the GLL nodes to the basis of Lagrange interpolating polynomials on the GL quadrature then we can use the operator \( \tilde{D} \) to evaluate the derivatives of this polynomial on the GL node basis.

With these derivative operators, we continue as in BP3.5 by defining the matrix of weights and

---

**Algorithm 5.** BP3.0: differentiation for 3D hexahedral elements

1. **Data:** (1) Vector \( \mathbf{q} \), size \( N_e \times N_p \), (2) differentiation matrix \( \tilde{D}^{1D} \), size \( N_q^{GL} \times N_q^{GL} \), (3) interpolation matrix \( I \), size \( N_q^{GL} \times N_q \), (4) geometric factors \( G \), size \( N_e \times N_p^{GL} \times 7 \), (5) parameter \( \lambda \);
2. **Output:** Vector \( \mathbf{Aq} \), size \( N_e \times N_p \);
3. for \( e \in \{1, 2, \ldots, N_e\} \) do
   4. \( \tilde{q}^e = \text{Interpolate}(q^e, I^{1D}) \) \( \triangleright \) Interpolate to GL nodes (Algorithm 1)
5. for \( i, j, k \in \{1, 2, \ldots, N_q^{GL}\} \) do
   6. \( \tilde{r}_{ij}^e = G_{i;kl}^e \tilde{r}_{iq} + G_{i;lj}^e \tilde{r}_{iq} + G_{i;jk}^e \tilde{r}_{iq} \);
   7. \( \tilde{r}_{ij}^e = G_{i;kl}^e \tilde{r}_{iq} + G_{i;lj}^e \tilde{r}_{iq} + G_{i;jk}^e \tilde{r}_{iq} \);
   8. \( \tilde{r}_{ij}^e = G_{i;kl}^e \tilde{r}_{iq} + G_{i;lj}^e \tilde{r}_{iq} + G_{i;jk}^e \tilde{r}_{iq} \);
   9. \( \tilde{r}_{ij}^e = G_{i;kl}^e \tilde{r}_{iq} + G_{i;lj}^e \tilde{r}_{iq} + G_{i;jk}^e \tilde{r}_{iq} \);
10. end for
11. end for
12. for \( i, j, k \in \{1, 2, \ldots, N_q^{GL}\} \) do
13. \( J_{ijkl}^e = G_{i;kl}^e q_{ijkl} + G_{i;lj}^e q_{ijkl} + G_{i;jk}^e q_{ijkl} \);
14. end for
15. end for
16. for \( i, j, k \in \{1, 2, \ldots, N_q^{GL}\} \) do
17. \( \tilde{A}_{ijkl} = \lambda J q_{ijkl} + \sum_{n=1}^{N_q^{GL}} \tilde{D}_{ijkl}^{1D} \tilde{r}_{ijkl}^e + \tilde{D}_{ijkl}^{1D} \tilde{r}_{ijkl}^e + \tilde{D}_{ijkl}^{1D} \tilde{r}_{ijkl}^e ;
18. end for
19. \( \mathbf{Aq}^e = \text{Project}(\tilde{A}^e, I^{1D}) \) \( \triangleright \) Project to GLL nodes (Algorithm 2)
20. end for
geometric data $G^e$ in (10) where this time
$$(G^e_{rr})_{abc,abc} = \tilde{w}_a \tilde{w}_b \tilde{w}_c G^e_{rr}(\tilde{r}_a, \tilde{s}_b, \tilde{t}_c),$$
for $a, b, c = 1, \ldots, N^GL_q$. We use analogous definitions for the remaining entries of $G^e$. Using these matrix operators we can write the local stiffness matrix (8) compactly as follows
$$S^e = I^T \tilde{D}^T G^e \tilde{D} I.$$

Note that, as with the GLL interpolation basis polynomials, we can define the one-dimensional differentiation operator $\tilde{D}$ defined such that
$$\tilde{D}_{ai} = \tilde{l}_i(\tilde{r}_a),$$
for $i, a = 1, \ldots N^GL_q$, so that each differentiation operation in $\tilde{D}$ can be written as a tensor product of $\tilde{D}$ and the identity matrix $I$. Therefore the differentiation operators on the GL Lagrange interpolation basis polynomials along each dimension can be applied using a single tensor contraction.

Finally, to express the full action of the local screened Poisson operator $S^e + \lambda M^e$ we combine the discussion in BP1.0 regarding using the GL quadrature to evaluate the local mass matrix $M^e$ in order to write the local screened Poisson operator as
$$S^e + \lambda M^e = I^T \tilde{D}^T G^e \tilde{D} I + \lambda I^T J^e I,$$
where $J^e$ is defined as in BP1.0 above. This operator can be applied using a total of twelve tensor contractions. We first interpolate to the GL quadrature nodes by applying the interpolation operator $I$ using three tensor contractions. We then differentiate along each dimension by applying the $\tilde{D}$ operator using three tensor contractions. We then multiply by the necessary geometric factors and multiply by the transpose derivative operator using three additional tensor contractions and add the mass matrix contributions. Finally we use three tensor contractions to multiply by the transpose interpolation operator in each dimension to project the result back to the GLL interpolation nodes. We detail the full matrix-free action of the stiffness matrix evaluated with the numerical quadrature in pseudo code in Algorithm 5.

5 Empirical performance model

The performance for all three benchmark problems is limited by global memory bandwidth. In BP3.5 and BP3.0 we load seven geometric factors for every node in the FEM element in addition to loading and storing the field vector $q$ itself. Moreover, as we emphasize in the introduction, for all three operations the data-to-FLOP ratio is high which limits our ability to hide memory latency behind computation.

(Konstantinidis and Cotronis, 2015) proposed a GPU performance model that accounts for the various data-to-flop ratios. However, the kernels used in the model achieve occupancy of around 97% while, for our kernels, extensive use of register file and shared memory results in achieved occupancy rarely exceeding 25%. Hence, we cannot apply this model for our kernels in a meaningful way.

A different idea was presented in (Abdelfattah et al., 2016), where the authors used the size of global memory transfers as a means of comparison. The advantage of such approach is that it
is independent of implementation. In this work, we use a model which is similar to (Abdelfattah et al., 2016). However, we transfer comparatively more data due to the geometric factors. Our model is also based on an assumption that the bandwidth of the global device data transfer is the limiting factor. Thus, we compare the performance of our kernels to the performance of copying data from global GPU memory to global GPU memory. The size of the data transfer we compare to is equivalent to the size of the data moved from and to the global memory in the particular benchmark problems, see Table 2.

For example, for every element in the FEM mesh the BP1.0 code needs to read
\[ R = N_p + N_p^{GL} \]
doubles and needs to write
\[ W = N_p \]
doubles. Hence, the total global memory transfer is
\[ T_{BP1.0} = 2N_p + N_p^{GL}, \]
bytes of data per element. Since the memory bus is bi-directional and a double variable consists of eight bytes of data, we compare the performance of our code for BP1.0 to transferring
\[ 8N_{el} \frac{2N_p + N_p^{GL}}{2} \]
bytes of data. Each data transfer is executed ten times using a standard cudaMemcpy function and the performance in terms of GB/s is measured by taking an average of the ten measurements.

The efficiency of data transfer depends on the size of data, with throughput maximized if sufficiently large amounts of data are being transferred. We therefore expect higher bandwidth for a mesh with more elements, and for higher degree polynomial approximations. We note that for the GPU used in this paper, the NVIDIA Tesla P100 12 GB PCI-E, the mesh containing 512 elements is too small to effectively hide data transfer latencies. To see this, we note that our approach is to parallelize the problem by assigning each element to a thread block. The NVIDIA Tesla P100 has 56 SMs and two blocks of threads can be processed simultaneously on every SM. The GPU is therefore capable of processing 112 blocks of threads concurrently, which for the mesh of 512 elements means only 5 thread blocks are executed per SM. The result of this small work load per SM is that the overhead cost of kernel launch is not offset by the execution time of the kernel itself and also the empirical bandwidths which we observe in these data transfers are noisy due to overhead costs.

Let \( d_r \) denote the number of bytes read from the global GPU memory and \( d_w \) denote the number of bytes written to global GPU memory by a GPU kernel. Let \( B_{gl} \) denote global memory

|       | BP1   | BP3.5 | BP3   |
|-------|-------|-------|-------|
| Read (R) | \( N_p + N_p^{GL} \) | \( 8N_p \) | \( N_p + 7N_p^{GL} \) |
| Write (W) | \( N_p \) | \( N_p \) | \( N_p \) |
| Total bytes (T) | \( 2N_p + N_p^{GL} \) | \( 9N_p \) | \( 2N_p + 7N_p^{GL} \) |

Table 2: The minimum number of doubles read and written to the global GPU memory per element in the three problems considered in this paper.
bandwidth for copying $\frac{d_r+d_w}{2}$ bytes of data. Let $F$ denote the number of floating point operations that must be executed in this kernel. In our model, the maximal GFLOPS/s are estimated using a formula

$$R_{\text{global}} = \frac{B_{\text{gl}} \cdot F}{d_w + d_r}.$$  

For BP1.0, BP3.5 and BP3.0 the roofline $R_{\text{global}}$ is evaluated as a function of polynomial degree $N$. Figure 1 shows maximum TFLOPS/s for BP1.0, BP3.5 and BP3.0, respectively.

Inspired by (Volkov and Demmel, 2008), for several kernels tested for BP1.0 and BP3.0., we devised a supplementary theoretical roofline based on shared memory bandwidth. We observe that in addition to copying the data to/from global memory, we also copy the data to/from shared memory\footnote{Unlike the copy-based empirical streaming roofline, the shared memory performance bound depends on the kernel, not on the problem.}. Since the memory bandwidth of shared memory is lower than the register bandwidth, shared memory transactions can limit performance. We denote the shared memory bandwidth by

Figure 1: Performance roofline bounds for the BP1.0 (top left), BP3.5 (top right), and BP3.0 (bottom) benchmarks. In each chart the upper plot (line with diamond-shaped ticks) shows a theoretical bound obtained using theoretical peak bandwidth of 549 GB/s for the NVIDIA P100 PCI-E 12GB GPU. The lower plots show the empirical peak bandwidth bound obtained using measured bandwidth attained when performing a device memory to device memory copy (upper line for a hexahedral mesh with 4096 elements and lower line for a hexahedral mesh with 512 elements).
Figure 2: 3D vs 2D thread structure. On the left: 3D approach – each thread processes a “slice” of nodes. On the right: 2D approach – each thread processes a vertical “column” of nodes.

\[ B_{sh} = \#SMs \times \text{SIMD width} \times \text{word length} \times \text{clock speed in Ghz}. \]

With this ansatz we estimate that the shared memory for the NVIDIA Tesla P100 12 GB PCI-E GPU is limited to \( B_{sh} = 56 \cdot 32 \cdot 4 \text{ bytes} \cdot 1.328 \text{Ghz} = 9.5191 \text{TB/s} \). The shared memory roofline model is then given by the equation

\[
R_{\text{shared}} = \frac{B_{sh} \cdot F}{s_r + s_w},
\]

where \( F \) denotes the number of floating point operations performed (per thread block), \( s_r \) is the number of bytes read from the shared memory (per thread block) and \( s_w \) is the number of bytes written to the shared memory (per thread block).

6 Optimizing Benchmark Problem 1.0

In this section we describe the sequence of optimization strategies that were applied to the implementation of the BP1 operation.

Kernel design. Recall that the tensor contraction operations for each element in the FEM mesh can be performed independently of other elements. Thus, to parallelize the FEM operations we assign each element to a block of threads on the GPU. In a previous work, (Remacle et al., 2016) associated a single node of an element with a single thread. This is, however, impossible for high-order interpolation because if \( N_q \geq 9 \), we exceed the maximum number of threads per block of threads (currently limited by CUDA to 1024). Hence, for higher-order approximations we need to assign multiple nodes to a thread. We can subdivide the nodes in each element using either use a 3D thread structure or a 2D thread structure. Figure 2 shows two such approaches. For BP1.0, we use a 2D thread structure since we found it more effective. We also investigate a 3D thread structure for \( N_q \leq 9 \) for BP3.5 and \( N_q < 9 \) for BP3.0.

In BP1.0 the action of the mass matrix \( M \) on each element can be applied using six tensor contraction operations. Hence, Algorithm 3 consists of 6 contractions wherein we cycle through the entire \( \mathbf{q}^e \). Block-wise synchronization is needed between the contractions to ensure that the
previous operation has completed. At the minimum, we need to enforce this block synchronize five times. Using a 2D thread structure requires more thread synchronizations because we process only a slice of the nodes at a time.

**BP1.0 thread memory optimization.** Because the one-dimensional interpolation matrix $I^{1D}$ is used by all the threads in the block, we load $I^{1D}$ into the shared memory. For the field variable $q$, we can either load $q^e$ to shared memory, fetch it to registers, or fetch it piece-by-piece from global memory when needed. Note that we also need a placeholder array to store the partial results between the loops. There are several options to choose from, however only a single array of size $N_p^{GL}$ can be stored in shared memory. Storing two such arrays is not feasible since we exceed the limit of 48 KB shared memory for thread block for a large $N$.

**BP1.0 kernel optimization.** We show the performance results of eight GPU kernels in Figure 3. The eight kernels were constructed in sequence beginning from a direct implementation of the pseudo-code in Algorithm 3 and applying successive optimizations. The results shown in Figure 3 help to demonstrate the effect each optimization has on the overall performance of BP1.0. We list below some details of each kernel here as well as any optimization made in that kernel. Unless otherwise noted, Kernel $n$ contains all the optimizations contained in Kernel $n - 1$.

**Kernel 1:** This kernel serves as a reference implementation. It uses a 2D thread structure associated with horizontal $(i,j)$ slices (see right side of Figure 2). We declare two additional global memory variables for storing intermediate results. Kernel 1 only uses shared memory for the interpolation matrix. In all the loops, it reads from and writes to global memory. As a result, the reference kernel is highly inefficient, reaching only 80 GFLOPS/s even for the larger mesh.

**Kernel 2:** In this kernel the global auxiliary arrays are replaced by two shared memory arrays (with $(N_q^{GL})^2$ elements in each array). While processing $q^e$, we read directly from the input arrays, without caching to shared memory or registers. Due to the reduced number of global memory fetches, the performance improves by approximately a factor of two.

**Kernel 3:** In this kernel each thread allocates a register array of size $N_q^{(GL)}$ and copies a section of $q^e$ to the array at the beginning of the kernel. This kernel reaches 1 TFLOP/s in the best case.
Kernel 4: In this kernel all the input variables, except the variable to which the output is saved, are declared as `const`. This yields only a marginal improvement in performance.

Kernel 5: For this kernel, if \( N_q = 8 \), or 16 or \( N_q^{GL} = 8 \), or 16, we pad the shared memory arrays used for storing \( I^{1D} \) and partial results to avoid bank conflicts. There is only a noticeable improvement for \( N = 15 \) for the smaller mesh and \( N = 14 \) for the larger mesh.

Kernel 6: In this kernel all loops, including the main loop in which we process the \((i,j)\) slices are unrolled. Unrolling the \((i,j)\) loop is important for the performance, since it gives the scheduler more freedom and more opportunity for instruction-level parallelism. At this point, the performance exceeds one TFLOP/s for the small mesh and 1.4 TFLOPS/s for the large mesh.

Kernel 7: All kernels presented thus far have required \( 5N_q^{GL} + 1 \) thread synchronizations in a block. For example with \( N = 12 \), for which \( N_q^{GL} = 14 \), the number of synchronizations is 71. In this kernel the number of thread synchronizations is reduced to five by allocate more shared memory. That is, we load the entire \( q^e \) array to shared memory as opposed to only loading \( q^e \) slice-by-slice. Figure 4 illustrates the idea behind reducing synchronizations. Kernel 7 brings the performance up to 2.25 TFLOPS/s,

Kernel 8:: (Volkov, 2010) emphasized that shared memory is much slower than using registers. Hence, reducing total number of read and write requests to/from shared memory and replacing them with register read/write instructions can significantly improve performance. Kernel 8 exploits the structure of the matrix \( I^{1D} \) to reduce the number of shared memory transactions. Specifically, each entry in \( I^{1D} \) appears twice: \( I_{nm}^{1D} = I_{N_q^{GL}+n+1,N_q-m+1}^{1D} \). Exploiting this symmetry lets us halve the number of loads from \( I^{1D} \). This kernel loads the entire \( I^{1D} \) into shared memory and inside each loop an appropriate entry is copied from shared memory to a register once and used twice. Since in BP1.0 we need to multiply by \( I^{1D} \) and by \( (I^{1D})^T \), pre-fetching only a half of matrix \( I^{1D} \) would complicate the code and require a set of additional if-statements, which cause thread divergence. The resulting reduction in shared memory operations brings the measured performance close to the empirical roofline.

BP1.0 results. The performance numbers presented in Figure 3 reveal that the kernels considered can be categorized into three groups. Kernels 1 and 2 form the first group, Kernels 3–6 form the second group and Kernels 7 and 8 form the third group. Between each of these three groups we observe significant performance improvements. The first major improvement occurs for Kernel 3 and is the result of caching \( q^e \) to register arrays prior to contraction. The second significant improvement occurs for Kernel 7 and is due to reducing the number of barriers. The performance of our reference kernel, Kernel 1, in the best case reaches only 80 GFLOPS/s, whereas our best kernel, Kernel 8, achieves 2.5 TFLOPS/s, yielding a 31 fold speedup. To obtain more than two TFLOPS/s, we needed to change the algorithm to account for the limitations intrinsic to the GPU, namely the cost of many thread synchronizations.

To explain the improvement between the Kernels 6-8 we consider the roofline model based on shared memory bandwidth. We generate a new roofline plot by taking a minimum of the empirical roofline based on device to device copy bandwidth (12) and the upper limit computed based on shared memory bandwidth (13). We show these new rooflines in Figure 5. For Kernel 8 this roofline is identical with the global memory roofline as in Figure 3 as the shared memory roofline is higher than the global memory roofline due to eliminating almost a half of shared memory transactions. This indicated that the shared memory bandwidth is not the limiting factor of the performance of Kernel 8 for high \( N \) where performance begins to degrade. For Kernels 6 and 7 however, we see
that this shared memory roofline model indeed provides a reliable performance bound and these kernels are likely limited by shared memory performance.

7 Optimizing Benchmark Problem 3.5

Kernel design. As in BP1.0, we parallelize the action of the screened Poisson operator by assigning each element to a separate thread-block on the GPU. In this optimization procedure we investigate a 2D thread structure as well as test a 3D thread structure for $N < 10$.

The action of the screened Poisson operator presents a difficult optimization challenge. In particular, hiding global memory latency is significantly more important than in BP1.0 because we transfer seven geometric factors ($J^e$ and 6 factors of $G^e$) per node from global memory in every element. The majority of these values are required during the action of the stiffness matrix. To hide global memory latency, we aim to overlap data transfer with computations.

The increased amount of data that we are required to load increases both the number of global memory read transactions and the number of registers needed per thread. In theory, the geometric factors can be computed “on the fly” inside the kernel using the element’s vertices and the each node’s $R_i, s_j, t_k$ coordinates. This approach would reduced the amount of global memory loaded to $18 + 2N_q$ double precision values per block but increases the number of registers. We implemented and extensively tested this approach but concluded that it was impractical. Indeed, it is faster to simply load geometric factors from global memory than use extra registers and FLOPS.

BP3.5 kernel optimization: 2D thread structure We show the performance results of ten GPU kernels in Figure 7. The ten kernels were constructed in sequence beginning from a direct implementation of the pseudo-code in Algorithm 6 and applying successive optimizations. The results is Figure 7 helps to demonstrate the effect each optimization has on the overall performance of BP3.5. As done with BP1.0, we list below some details of each kernel as well as any optimization made in that kernel.

Kernel 1: This kernel is a direct implementation of Algorithm 6. The one-dimensional differentiation matrix $D^{1D}$ is fetched to shared memory at the beginning of the kernel. This kernel also
uses a shared memory array of size $N_p$ to store partial sums. Entries of $q^f$ are fetched from global memory as needed. In the last loop, the partial sums are successively added directly to the global memory array to store the final result. The kernel achieves 200 GFLOPS/s, which is one sixth of the predicted empirical roofline.

**Kernel 2:** In this kernel all the variables, except the array used for storing the final result, are declared using `const`. This optimization has only a marginal influence on the performance for $N \geq 8$.

**Kernel 3:** In this kernel all loops with $k$ are unrolled. Unrolling loops improves the performance for the larger mesh only if $N \geq 8$ and for all $N$ for the smaller mesh. Note that a kernel with unrolled loops uses more registers per thread and, hence, the achieved occupancy decreases. The measured TFLOPS/s increases, however, as shown in Figure 6. This behavior can be explained if unrolling has increased instruction-level parallelism.

**Kernel 4:** In this kernel we place the $k$ loop (lines 7–17 in Algorithm 6) on the exterior of $i$ and $j$ loops. Doing this, $k$ becomes the slowest running index. This loop structure is justified because we iterate through $(i, j)$ slices.

**Kernel 5:** In this kernel the auxiliary shared memory array of size $N_p$ is replaced by two auxiliary shared memory array of size $N_q^2$ each.

**Kernel 6:** In this kernel the field variable $q^f$ is fetched to the shared memory. The overall im-

Figure 5: BP1.0: shared memory rooflines and achieved floating point performance. Top left: kernel 6. Top right: kernel 7. Bottom: kernel 8.
Algorithm 6. BP3.5: starting point of the implementation (2D thread structure)

1: **Data:** (1) Vector $q$, size $N_e \times N_p$, (2) differentiation matrix $\tilde{D}_{1D}$, size $N_q \times N_q$, (3) geometric factors $G$, size $N_e \times N_{GL} \times 7$, (4) parameter $\lambda$;
2: **Output:** Vector $Sq$, size $N_e \times N_p$;
3: for $e \in \{1, 2, \ldots, N_e\}$ do
4:  for each thread $i, j$ do
5:    Load $D_{1D}$ to shared memory variable $s_D$.
6:    Allocate one shared auxiliary array $s_{tmp}[N_q][N_q][N_q]$ and three register arrays: $r_Aq[N_q]$, $r_qt[N_q]$ and $r_tmpt[N_q]$ for storing intermediate results;
7:    $r_qt_k = \sum_{n=1}^{N_q} s_D^{kn} \ast q_e^{kji}$;
8:    for $k \in \{1, 2, \ldots, N_q\}$ do
9:      Load geometric factors to local variables $G_{00}$, $G_{01}$, $G_{02}$, $G_{11}$, $G_{12}$, $G_{22}$, $G_{WJ}$
10:     Declare variables $qr$ and $qs$ and set them to 0.
11:    $qr = \sum_{n=1}^{N_q} s_D^{in} \ast q_e^{kji}$;
12:    $qs = \sum_{n=1}^{N_q} s_D^{jn} \ast q_e^{kni}$;
13:    $Sq_{temp_kji} = G_{00}^{qk} + G_{01}^{qk} + G_{02}^{qk} + r_qt_k$;
14:    $s_{tmps_{kji}} = G_{01}^{qk} + G_{11}^{qk} + G_{12}^{qk} + G_{22}^{qk}$;
15:    $r_tmpt_k = G_{02}^{qk} + G_{12}^{qk} + G_{22}^{qk}$;
16:    $Sq_{kji} = Sq_{kji} + G_{WJ}^{qk} \ast q_e^{kji}$;
17:    $Sq_{e_{kji}} = \sum_{n=1}^{N_q} Sq_{e_{nji}} \ast r_tmpt_k$;
18:    end for                      ▷ Synchronize threads.
19:    for $k \in \{1, 2, \ldots, N_q\}$ do
20:      Declare variables $Sq1$ and $Sq2$ and set them to 0.
21:    $Sq1 = \sum_{n=1}^{N_q} Sq_{temp_{kjn}} \ast s_D^{ni}$;
22:    $Sq2 = \sum_{n=1}^{N_q} Sq_{temp_{kni}} \ast s_D^{nj}$;
23:    $Sq_{e_{kni}} = Sq_{e_{kni}} + Sq1 + Sq2$;
24:    end for                      ▷ Synchronize threads.
25:  end for
26: end for

Kernel 7: This kernel reduces total global memory transactions by caching the necessary data at the beginning of the kernel and only writing the output variable once. This produces a significant optimization and improves performance by about 40%.

Kernel 8: For this kernel, if $N = 7$ or 15, the arrays are padded to avoid shared memory bank conflicts. The improvements are significant for the larger mesh and $N = 15$.

Kernel 9: In this kernel each thread allocates a register array with $N_q$ elements and the field variable $q_e$ is fetched to these registers instead of shared memory. For both meshes, this approach slightly improves the performance, and only for $N = 12$ and $N = 15$.

Kernel 10: This kernel uses three two-dimensional shared memory arrays for partial results and fetches the field variable $q_e$ to register arrays. The achieved TFLOPS/s for this kernel are aligned with the empirical roofline.
Figure 6: BP3.5: Comparison of performance for Kernel 1 and Kernel 2. The only difference between these two kernels is loop unrolling. The number of registers per thread is shown in the bar chart in the background.

**BP3.5 results: 2D thread structure.** Many of the performance improvements we observe when optimizing the kernels for BP3.5 are due to subtle changes in the code, e.g. declaring variables as constant, adding padding, or unrolling the loops. But global and shared memory usage has the biggest impact on the performance. Once we reduce the use of global memory (starting in Kernel 7) the performance improves substantially, especially for larger $N$. Reducing the amount of shared memory and caching the data to registers results in the second most important factor which is visible in Figure 7 for the mesh with 4096 elements and $N \geq 10$.

For the reference kernel, Kernel 1, the performance barely reaches 200 GFLOPS/s whereas the most optimized kernel we present, Kernel 10, achieved up to 1.2 TFLOPS/s. While this is only a six fold speedup, comparison with our empirical roofline model, based on streaming global device memory, shows that the performance of Kernel 10 is comparable to just streaming the minimally necessary data.

**BP3.5 kernel optimization: 3D thread structure.** We show the performance results of six GPU kernels in Figure 7. We again construct these kernels as a sequence of successive optimizations beginning from the the pseudo-code shown in Algorithm 7 which uses a 3D thread structure. we present results for these kernels for $N = 1, 2, \ldots, 9$, since associating one thread with one node as done in this 3D thread structure would require more than the maximum of 1024 threads for
Algorithm 7. BP3.5: collocation differentiation for 3D hexahedral mesh (3D thread structure)

1: **Data:** (1) Vector \( \mathbf{q} \), size \( N_e \times N_p \), (2) differentiation matrix \( \mathbf{D}^{1D} \), size \( N_q \times N_q \), (3) geometric factors \( \mathbf{G} \), size \( N_e \times N_p^\text{GL} \times 7 \), (4) parameter \( \lambda \);  
2: **Output:** Vector \( \mathbf{Sq} \), size \( N_e \times N_p \);  
3: for \( e \in \{1, 2, \ldots, N_e\} \) do  
4: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
5: If \( k=0 \), load \( \mathbf{D}^{1D} \) to shared memory variable \( s_{D} \);  
6: Declare register variables \( r_{qr}, r_{qs}, \) and \( r_{qt} \);  
7: end for \( \triangleright \) Synchronize threads.  
8: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
9: Load \( GwJ; \)  
10: Declare variables \( qr, qs, qt \) and set them to 0.  
11: \( qr = \sum_{n=1}^{N_q} s_{Dn} * q^{k}_{kjn}; \)  
12: \( qs = \sum_{n=1}^{N_q} s_{Dn} * q^{k}_{kni}; \)  
13: \( qt = \sum_{n=1}^{N_q} s_{Dn} * q^{k}_{njk}; \)  
14: Set \( r_{qr} = qr, r_{qs} = qs \) and \( r_{qt} = qt; \)  
15: \( Sq^{k}_{kji} = GwJ* \lambda * q^{k}_{kj}; \)  
16: end for \( \triangleright \) Synchronize threads.  
17: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
18: Load \( G00, G01, G02; \)  
19: \( Sq^{k}_{kji} = G00*r_{qr} + G01*r_{qs} + G02*r_{qt}; \)  
20: end for  
21: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
22: \( Sq^{k}_{kji} = Sq^{r}_{kji} + \sum_{n=1}^{N_{k}} s_{Dn} * Sq^{k}_{kj}; \)  
23: end for \( \triangleright \) Synchronize threads.  
24: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
25: Load \( G10, G11, G12; \)  
26: \( Sq^{k}_{kji} = G10*r_{qr} + G11*r_{qs} + G12*r_{qt}; \)  
27: end for \( \triangleright \) Synchronize threads.  
28: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
29: \( Sq^{k}_{kji} = Sq^{r}_{kji} + \sum_{n=1}^{N_{k}} s_{Dn} * Sq^{k}_{kni}; \)  
30: end for \( \triangleright \) Synchronize threads.  
31: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
32: Load \( G10, G11, G12; \)  
33: \( Sq^{k}_{kji} = G20*r_{qr} + G21*r_{qs} + G22*r_{qt}; \)  
34: end for \( \triangleright \) Synchronize threads.  
35: for \( i, j, k \in \{1, 2, \ldots, N_q\} \) do  
36: \( Sq^{k}_{kji} = Sq^{r}_{kji} + \sum_{n=1}^{N_{k}} s_{Dn} * Sq^{k}_{nji}; \)  
37: end for \( \triangleright \) Synchronize threads.  
38: end for

higher-degree polynomials. We list below some details of each kernel as well as any optimization made in that kernel.  

**Kernel 1:** This kernel serves as an initial reference kernel and is a direct implementation of Algorithm 7. The differentiation matrix \( \mathbf{D}^{1D} \) is loaded into shared memory and partial sums are stored in global arrays. The performance of this kernel reaches 300 GFLOPS/s in the best case.  

**Kernel 2:** In this kernel all variables, except the output variable, are declared using \texttt{const}. All
Figure 7: BP3.5: Performance of 2D thread array kernels in various stages of optimization. The red line marked with crosses is the empirically determined roofline based on achievable device to device memory copies on an NVIDIA P100 PCI-E 12GB GPU. Left: TFLOPS/s for cubical mesh with 512 elements. Right: TFLOPS/s for cubical mesh with 4096 elements.

Loops with index $n$ are unrolled. The overall improvement is modest.

**Kernel 3**: In this kernel the geometric factors are stored in registers and fetched only once from global memory. This reduces the number of global memory loads from nine to seven. This kernel reaches about 350 GFLOPS/s for the larger mesh. In case of the smaller mesh, performance of this kernel is similar to Kernel 2.

**Kernel 4**: Instead of writing the result directly to $A_q$, in this kernel the partial results are accumulated in a register variable. The performance of this kernel is only slightly better than that of Kernel 3.

**Kernel 5**: In this kernel the field variable $q^e$ is cached to shared memory. The same shared array is used to store the partial result, hence there is no need to use $S_{qtemp}$. The performance increases significantly and reaches 610 GFLOPS/s.

**Kernel 6**: In this kernel, partial results are stored in three shared memory arrays of size $N_p$ each. This strategy reduces occupancy but allows the kernel to use less synchronizations (the number of synchronizations reduced to two). However, there is almost no performance difference between this and the previous kernel due to extensive use of shared memory.

**BP3.5 results: 3D thread structure.**

The kernels adapting 3D thread structure form two groups. First group consists of Kernels 1–4 and the second one consists of Kernels 5 and 6. The largest performance jump appears between Kernels 4 and 5. It is a result of caching the field variable to shared memory. Kernel 5 appears to be the best performing kernel. As a result of successively reducing the number of shared memory fetches, we improved performance by a factor of two, from approximately 300 GFLOPS/s to around 600 GFLOPS/s.
Figure 8: BP3.5: Performance of 3D kernels in various stages of optimization. The red line marked with crosses is the roofline computed based on device to device copies measured on an NVIDIA P100 PCI-E 12GB GPU. Left: TFLOPS/s for cubical mesh with 512 elements. Right: TFLOPS/s for cubical mesh with 4096 elements.

8 Optimizing Benchmark Problem 3.0

BP3.0 Kernel Design. BP3.0 can be considered a fusion of BP1.0 and BP3.5. This benchmark shares its interpolation/projection steps with BP1.0 and the stiffness matrix action with BP3.5. Hence, BP3.0 inherits all the optimization challenges we have discussed thus far for BP1.0 and BP3.5. In particular, the kernel for this problem needs to synchronize threads multiple times and needs to load a large amount of data from global memory. Furthermore, compared to either BP1.0 or BP3.5 this benchmark requires even more shared memory usage in order to store partial results. Since differentiation is performed using a denser set of nodes, we also transfer more data per thread block compared with BP3.5.

The action of the screened Poisson operator in this benchmark can be written as three distinct parts: interpolation to GL nodes, stiffness and mass matrix actions, and projection back to GLL nodes. Therefore it is possible to split the implementation into three kernels. This approach reduces memory requirements per kernel and makes the code more readable. We investigate this approach with 3D thread structure.

BP3.0 kernel optimization: 2D thread structure. We begin as in BP3.5 by first investigating a kernel implementation using a 2D thread structure. The performance results for nine separate kernel are presented in Figure 9. As in the previous benchmarks we present a sequence of kernels and detail what optimizations we performed in each kernel.

Kernel 1: This kernel serves as a reference implementation. In this kernel there are four shared memory arrays: one for $I^{1D}$, one for $D^{1D}$ and two arrays with $(N_q^{GL})^2$ elements for storing partial sums. Each thread also allocates an additional register array to store additional partial sums that do not require sharing between threads in a thread block. The field variable $q^e$ is read directly from global memory when needed. This kernel reaches approximately 280 GFFLOPS/s.

Kernel 2: In this kernel all the input variables, except the pointer used for storing the final results, are declared as const. Each thread allocates a register array of size $N_q$ and caches a column of entries of $q^e$ to the register array. The performance for $N \geq 12$ for the larger mesh improves to
over 1.25 TFLOP/s

**Kernel 3:** In this kernel all internal loops are unrolled. The performance improves to 600 GFLOPS/s for the smaller mesh and to 1.4 TFLOP/s for the larger mesh.

**Kernel 4:** In this kernel we add padding to all the shared memory arrays to avoid bank conflicts. In particular, in case $N_q^{GL} = 8$ or $N_q^{GL} = 16$, the arrays with size $N_q^{GL} \times N_q^{GL}$ change their size to $N_q^{GL} \times (N_q^{GL} + 1)$. Padding helps only for the smaller mesh.

**Kernel 5:** This kernel adapts the most efficient interpolation strategy devised for BP1.0 (see BP1.0: Kernel 7 and Figure 4). For the larger mesh, the performance reaches 1.5 TFLOP/s.

**Kernel 6:** In this kernel the field variable $\mathbf{q}^e$ is loaded to a shared memory array. This kernel implements more efficient differentiation (as in BP3.5: Kernel 9). The improvement is very modest since in order to use this type of differentiation we need to combine it with less efficient interpolation.

**Kernel 7:** A version of Kernel 6 with one less shared memory array. We use only one shared memory array to store the partial result at a cost of additional synchronizations. Kernel 7 performs better than Kernel 6, however in most cases, it is not more efficient than Kernel 5.

**Kernel 8:** This kernel is a version of Kernel 7 with both $\mathbf{D}^{1D}$ and $(\mathbf{D}^{1D})^T$ fetched to shared memory. Now all the threads can access shared memory column-wise. Performance is very similar to Kernel 6.

**Kernel 9:** The kernel uses the same strategy as in the last kernel implemented for BP1.0, i.e., it fetches each repeating entry of the interpolation matrix $\mathbf{I}^{1D}$ only once. The performance of this kernel is the best that we present here as it reaches 1.6 TFLOPS/s.

**BP3.0 Results: 2D thread structure.** For this benchmark problem, our best performing kernel for high-order FEM approximations, Kernel 10, performs approximately four times as the reference kernel, Kernel 1. Although we did not achieve the peak performance as predicted by our empirical roofline model using global memory bandwidth, for the 4096 element mesh and $N \leq 12$ our kernels are very close to that peak.

As in BP1.0 we can obtain a better understanding of the performance of our kernels by considering the roofline model based on shared memory bandwidth. Figure 10 shows updated rooflines for Kernels 8 and 9 in which we see that this shared memory bandwidth bound yields a better estimate for the achieved performance of these kernels with $N \geq 10$.

**BP3.0 3D thread structure.** We perform analogous tuning process using a 3D thread structure for $N < 9$. Figure 11 shows the performance of these kernels presented below.

**Kernel 1:** This kernel starts from a direct implementation of the pseudo-code given in Algorithm 5, which is executed as three separate CUDA kernels. The field variable $\mathbf{q}^e$ is read directly from global memory and partial results are stored in global memory as well. The code reaches approximately 280 GFLOPS/s in the best case.

**Kernel 2:** This kernel combines the three separate kernels as one CUDA kernel. There is almost no difference between Kernel 1 and Kernel 2. This suggests that the cost of additional kernel launches is small compared with the cost of data transfer.

**Kernel 3:** In this kernel all internal loops are unrolled. Unrolling loops would appear to be more important for 2D thread structure as for 3D thread structure it has only a marginal influence on performance.
Kernel 4: This kernel differs from Kernel 2 by loading the geometric factors once and avoiding redundant reads. The gain in performance is small because of large amount of global memory transactions that have not yet been eliminated.

Kernel 5: While we access the field variable $q^e$ directly from global memory in the interpolation and projection parts, $q^e$ is fetched to a shared array in the differentiation step.

Kernel 6: This kernel is a version of Kernel 5 with intermediate results stored in registers in the differentiation step. Kernels 5 and 6 are approximately 1.5 times faster than Kernel 4.

Kernel 7: In this kernel we store the partial results in shared memory and registers everywhere except between interpolation, first and second differentiation, and projection.

Kernel 8: In this kernel there is no intermediate global storage. All intermediate results are accumulated either in shared memory or in registers.

Kernel 9: In this kernel we declare three additional shared memory arrays (size $N_p$ each) for storing intermediate results. As a result, the performance reaches 900 GFLOPS/s.

BP3.0 Results: 3D thread structure. Unlike in the case of BP3.5, in BP3.0 we observe a very gradual improvement in performance. However, as for BP3.0 the largest improvements appear when removing additional global memory transactions. It is interesting to note that the difference between kernel 7 and 8 is rather small, despite the fact that Kernel 7 reads and writes three vectors of size $N_{el} \cdot N_p$ to the global memory and Kernel 8 reads and writes only once. The lack of significant improvement may be a result of the additional synchronizations enforced in Kernel 8. In Kernel 7, the global write serves as synchronization.

9 Conclusions and future work

In this paper we described the GPU optimization of three FEM-specific benchmark problems which have significant relevance in real world large scale code bases. We detailed how reducing factors
such as global memory transactions and reducing pressure on shared memory usage can lead to efficient GPU kernels for these FEM operators. For BP3.5, the most tuned kernel is aligned with the empirical roofline bound and its performance is limited only by global memory bandwidth. We obtained similar results for the two remaining problems but their performance does not scale perfectly for \( N \geq 13 \). For each of the problems we used a sequence of optimizations. One might argue that multiple authors (see, for example (Garvey and Abdelrahman, 2015), (Abdelfattah et al., 2016), (Nelson et al., 2015)) consider automatic performance tuning and our efforts should rather be replaced by a computational tuning process. However, in each of the benchmarks we consider large performance improvements are gained by changing the algorithm itself, which is not an automatic process. While the performance bottlenecks such too many barriers in BP1.0 and high data fetch to flop ratio in BP3.0 and BP3.5 are often not hard to identify, they can be troublesome to remove. We use a mixture of standard optimization strategies such as splitting the data between registers and shared memory and more advanced strategies, which resulted in redesigning the algorithm to make it more well-suited for fine-grain parallelism.

An obvious question remaining is how much more performance can be obtained in each of these benchmarks. In this paper we provide contributions towards the answer. Unlike (Abdelfattah et al., 2016), we consider the limitation of shared memory bandwidth in our approach. By no mean our model is exhaustive and our future work involves introducing a more advanced performance model that accounts for register use and other factors but retains the similarity of the original model. The source code for all kernels and benchmarks considered in this paper is publicly available at: http://github.com/tcew/CEED

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Figure 11: BP3.0: Performance of 3D kernels in various stages of optimization. The red line marked with crosses is the roofline computed based on device to device copies on a single NVIDIA P100 PCI-E 12GB GPU. Left: TFLOPS/s for cubical mesh with 512 elements. Right: TFLOPS/s for cubical mesh with 4096 elements. Note: almost all kernels fail for $N = 3$ on the smaller mesh.

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References

Ahmad Abdelfattah, Marc Baboulin, Veselin Dobrev, Jack Dongarra, Christopher Earl, Joel Falcou, Azzam Haidar, Ian Karlin, Tz Kolev, Ian Masliah, et al. High-performance tensor contractions for GPUs. *Procedia Computer Science*, 80:108–118, 2016.

Cris Cecka, Adrian J Lew, and Eric Darve. Assembly of finite element methods on graphics processors. *Int J Numer Methods Eng.*, 85(5):640–669, 2011.

CEED. Ceed benchmark problems. [http://ceed.exascaleproject.org/bps/](http://ceed.exascaleproject.org/bps/) 2017.

Maryam Mehri Dehnavi, David M Fernández, and Dennis Giannacopoulos. Finite-element sparse matrix vector multiplication on graphic processing units. *IEEE Trans. Magn.*, 46(8):2982–2985, 2010.

Michel O Deville, Paul F Fischer, and Ernest H Mund. *High-order methods for incompressible fluid flow*, volume 9. Cambridge university press, 2002.

A Dziekonski, M Rewienski, P Sypek, A Lamecki, and M Mrozowski. GPU-accelerated LOBPCG method with inexact null-space filtering for solving generalized eigenvalue problems in computational electromagnetics analysis with higher-order FEM. *Comm. Comput. Phys.*, 22(4):997–1014, 2017.

Paul F Fischer, Katherine Heisey, and Misun Min. Scaling limits for PDE-based simulation. In *22nd AIAA Computational Fluid Dynamics Conference*, page 3049, 2015.
Zhisong Fu, T James Lewis, Robert M Kirby, and Ross T Whitaker. Architecting the finite element method pipeline for the GPU. *J Comput Appl Math*, 257:195–211, 2014.

J. D. Garvey and T. S. Abdelrahman. Automatic performance tuning of stencil computations on GPUs. In *2015 44th International Conference on Parallel Processing*, pages 300–309, 2015.

Dominik Göddeke, Robert Strzodka, and Stefan Turek. *Accelerating double precision FEM simulations with GPUs*. Univ. Dortmund, Fachbereich Mathematik, 2005.

Dominik Göddeke, Robert Strzodka, Jamaludin Mohd-Yusof, Patrick McCormick, Sven H. M. Buijssen, Matthias Grajewski, and Stefan Turek. Exploring weak scalability for FEM calculations on a GPU-enhanced cluster. *Parallel Comput.*, 33(10-11):685–699, November 2007. ISSN 0167-8191. doi: 10.1016/j.parco.2007.09.002. URL [http://dx.doi.org/10.1016/j.parco.2007.09.002](http://dx.doi.org/10.1016/j.parco.2007.09.002).

Dominik Göddeke, Sven HM Buijssen, Hilmar Wobker, and Stefan Turek. GPU acceleration of an unmodified parallel finite element Navier-Stokes solver. In *High Performance Computing & Simulation, 2009. HPCS’09. International Conference on*, pages 12–21. IEEE, 2009.

Paul Grigoraş, Pavel Burovskiy, Wayne Luk, and Spencer Sherwin. Optimising sparse matrix vector multiplication for large scale FEM problems on FPGA. In *Field Programmable Logic and Applications (FPL), 2016 26th International Conference on*, pages 1–9. IEEE, 2016.

Sunpyo Hong and Hyesoon Kim. An analytical model for a GPU architecture with memory-level and thread-level parallelism awareness. *SIGARCH Comput. Archit. News*, 37(3):152–163, 2009.

Elias Konstantinidis and Yiannis Cotronis. A practical performance model for compute and memory bound GPU kernels. In *Parallel, Distributed and Network-Based Processing, 23rd Euromicro International Conference on*, pages 651–658. IEEE, 2015.

Victor W. Lee, Changkyu Kim, Jatin Chhugani, Michael Deisher, Daehyun Kim, Anthony D. Nguyen, Nadathur Satish, Mikhail Smelyanskiy, Srinivas Chennupaty, Per Hammarlund, Ronak Singhal, and Pradeep Dubey. Debunking the 100x GPU vs. CPU myth: An evaluation of throughput computing on CPU and GPU. *SIGARCH Comput. Archit. News*, 38(3), 2010.

Bangtian Liu, Chengyao Wen, Anand D Sarwate, and Maryam Mehri Dehnavi. A unified optimization approach for sparse tensor operations on gpus. *arXiv preprint arXiv:1705.09905*, 2017.

Yu Jung Lo, Samuel Williams, Brian Van Straalen, Terry J Ligocki, Matthew J Cordery, Nicholas J Wright, Mary W Hall, and Leonid Oliker. Roofline model toolkit: A practical tool for architectural and program analysis. In *International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems*, pages 129–148. Springer, 2014.

GR Markall, A Slemmer, DA Ham, PHJ Kelly, CD Cantwell, and SJ Sherwin. Finite element assembly strategies on multi-core and many-core architectures. *Int. J. Numer. Methods Fluids*, 71(1):80–97, 2013.

Graham R Markall, David A Ham, and Paul HIJ Kelly. Towards generating optimised finite element solvers for GPUs from high-level specifications. *Procedia Comput. Sci.*, 1(1):1815–1823, 2010.
David S. Medina, Amik St.-Cyr, and Timothy Warburton. OCCA: A unified approach to multi-threading languages. *CoRR*, abs/1403.0968, 2014. URL http://arxiv.org/abs/1403.0968.

T. Nelson, A. Rivera, P. Balaprakash, M. Hall, P. D. Hovland, E. Jessup, and B. Norris. Generating efficient tensor contractions for GPUs. In *2015 44th International Conference on Parallel Processing*, pages 969–978, 2015.

James W. Lottes Paul F. Fischer and Stefan G. Kerkemeier. nek5000 Web page, 2008. http://nek5000.mcs.anl.gov.

J-F Remacle, R Gandham, and Tim Warburton. GPU accelerated spectral finite elements on all-hex meshes. *J. Comput. Phys.*, 324:246–257, 2016.

John A. Stratton, Christopher Rodrigues, I-Jui Sung, Nady Obeid, Li-Wen Chang, Nasser Anssari, Geng D. Liu, and Wen-mei W. Hwu. Parboil: a revised benchmark suite for scientific and commercial throughput computing. Technical report, University of Illinois at Urbana-Champaign, 2012.

Vasily Volkov. Better performance at lower occupancy. In *Proceedings of the GPU technology conference, GTC*, volume 10, page 16. San Jose, CA, 2010.

Vasily Volkov and James W Demmel. Benchmarking GPUs to tune dense linear algebra. In *High Performance Computing, Networking, Storage and Analysis, 2008. SC 2008. International Conference for*, pages 1–11. IEEE, 2008.

H. Wong, M. M. Papadopoulou, M. Sadooghi-Alvandi, and A. Moshovos. Demystifying GPU microarchitecture through microbenchmarking. In *2010 IEEE International Symposium on Performance Analysis of Systems Software (ISPASS)*, pages 235–246, 2010.

Y. Zhang and J. D. Owens. A quantitative performance analysis model for GPU architectures. In *2011 IEEE 17th International Symposium on High Performance Computer Architecture*, pages 382–393, 2011.