Parity-Based Concurrent Error Detection Schemes for the ChaCha Stream Cipher

Viola Rieger and Alexander Zeh
Research and Development Center
Infineon Technologies AG, Munich, Germany
{viola.rieger, alexander.zeh}@infineon.com

Abstract—We propose two parity-based concurrent error detection schemes for the Quarterround of the ChaCha stream cipher to protect from transient and permanent faults. They offer a trade-off between implementation overhead and error coverage. The second approach can detect any odd-weight error on the in-/output and intermediate signals of a Quarterround, while the first one requires less logic.

I. INTRODUCTION

The ChaCha stream cipher was introduced by Bernstein in 2008 [1] as a successor of the Salsa cipher family [2]. Both algorithms are based on pseudorandom functions using ADD, ROTATE and XOR (ARX) operations. In order to provide confidentiality, authenticity and integrity for data, Associated Data (AEAD) takes on greater significance and realization in hardware for embedded systems seems fruitful. With the authenticator Poly1305, Bernstein proposed a software optimized Message Authentication Code (MAC, [3]), that is well suited to be used in combination with the ChaCha algorithm. Concurrent Error Checking (CED, [4], [5]) was developed to detect faults within functional or logical building blocks of embedded circuits, such as ALUs, adders or individual gates. CED enables an efficient, testable and robust design. Parity-based CED was applied to substitution-permutation networks in [6] and, e.g., applied to AES by Bertoni [7] and Natale [8]. To our knowledge, no CED scheme has been proposed for ChaCha so far.

This paper is structured as follows: we recall preliminaries on parity codes and the parity-bit prediction for basic operations on binary vectors in Section II. Section III contains basic operations of the ChaCha-Poly1305 AEAD scheme and intermediate signals in a Quarterround of ChaCha are defined. The transformation of a Quarterround into a code-disjoint circuit based on a single parity-bit prediction is described in Section IV. Thm. 4 gives the expression for the overall parity-bit and the error coverage is proven in Thm. 10. Our second group-based parity prediction is described in Section V and Thm. 13 proves its error coverage.

II. PRELIMINARIES

Let \( \mathbb{F}_q \) denote the finite field of order \( q \). For two integers \( a, b \) with \( b > a \), we denote by \([a, b]\) the integer set \( \{i \in \mathbb{Z} : a \leq i \leq b\} \) and let \([b]\) be the shorthand notation for \([1, b]\). Similarly, \([n, k, d]_q\) denotes the parameters of a \( q \)-ary linear code of length \( n \), dimension \( k \), and minimum Hamming distance \( d \). A generator matrix of a linear \([n, k, d]_q\) code \( C \) over \( \mathbb{F}_q \) is a \( k \times n \) matrix whose rows form a basis of \( C \). The binary \([n, n-1, 2]_2\) parity code is defined as the code with generator matrix \( G = (I_{n-1}) \), where \( I \) is the \((n-1) \times (n-1)\) identity matrix and \( 1_{n-1} = (1 \cdots 1)^T \). It is well-known, that any error \( e \in \mathbb{F}_2^n \) of odd Hamming weight added to a codeword \( c \) of an \([n, n-1, 2]_2\) parity code \( C \) results in a vector \((c+e) \not\in C \) that is detectable. In the following we use the calculation of the one-bit redundancy of a parity code. The bitwise XOR of two binary vectors \( a, b \in \mathbb{F}_2^n \) is denoted by \( a \oplus b \) and \( a \boxplus b \) is the addition of \( a \) and \( b \) in \( \mathbb{F}_2^n \).

A parity-bit of \( x = (x_0 \ x_1 \ \cdots \ x_{n-1}) \in \mathbb{F}_2^n \) is defined as the Boolean function \( p : \mathbb{F}_2^n \mapsto \mathbb{F}_2 \), where \( p(x) \equiv \bigoplus_{i=0}^{n-1} x_i \). Let \( a, b \in \mathbb{F}_2^n \), then we have:

\[
    p(a \oplus b) = p(a) \oplus p(b). \tag{1}
\]

The parity-bit of the sum of two binary vectors is:

\[
    p(a \boxplus b) = p(a) \oplus p(b) \oplus p(cv(a, b)), \tag{2}
\]

where \( c = cv(a, b) \in \mathbb{F}_2^n \) is the so-called carry vector associated with \( a \) and \( b \) and obtained during the calculation of their sum. The entries of \( c \) are given by

\[
    c_i = \begin{cases} 
        0, & \text{for } i = 0, \\
        a_i b_i \lor (a_i \oplus b_i) c_{i-1}, & \forall i \in [1, n-1]. 
    \end{cases} \tag{3}
\]
The addition $a \oplus b$ of two vectors $a, b$ requires more logic gates than the XOR $a \oplus b$ and is therefore more error-prone. Hence, a variety of self-checking adders were developed such as, e.g., a parity-checked carry look-ahead adder introduced by Nicolaidis in [9].

III. STREAM CIPHER CHACHA

The ChaCha algorithm transforms a 512-bit state matrix $V \in \mathbb{F}_{2^{128}}^{4 \times 4}$ into a unique and irreversible 512-bit output block. Encryption and decryption are performed by calculating the XOR of the keystream and the input data. ChaCha operates on 32-bit words, and makes use of a 256-bit key $K = (\text{key}_0, \text{key}_1, \cdots, \text{key}_7)$ and a 64-bit nonce $N^* = (\text{nonce}_0, \text{nonce}_1)$ (in several specifications 96 bits are reserved for the nonce and 32 bits for the counter). The constant $CST = (\text{cst}_0, \text{cst}_1, \text{cst}_2, \text{cst}_3)$.

Algorithm 1: ChaCha($N, K, CTR, N^*$)

\begin{algorithmic}
  \State \textbf{Input} : ROUNDS $N \in \{8, 12, 20\}$,
  \hspace{1em} Key $K = (\text{key}_0, \text{key}_1, \cdots, \text{key}_7) \in \mathbb{F}_{2^{128}}^{4}$,
  \hspace{1em} Counter $CTR = (\text{ctr}_0, \text{ctr}_1) \in \mathbb{F}_{2^{32}}^{2}$,
  \hspace{1em} Nonce $N^* = (\text{nonce}_0, \text{nonce}_1) \in \mathbb{F}_{2^{64}}^{2}$.
  \State \textbf{Output:} Updated matrix $V \in \mathbb{F}_{2^{128}}^{4 \times 4}$.
  \State (cst$_0$, cst$_1$, cst$_2$, cst$_3$) $\leftarrow$
  \hspace{1em} $\langle 0:61707865 \ 0x3320646E \ 0x79622D32 \ 0x6B206574 \rangle$;
  \State $M \leftarrow$
  \hspace{1em} $\langle \text{cst}_0 \quad \text{cst}_1 \quad \text{cst}_2 \quad \text{cst}_3 \rangle$; \hspace{1em} // Init.
  \State $V \leftarrow M$;
  \For{$i \leftarrow 0 \ \text{to} \ N/2 - 1$}
    \State $QR(0,0, v_{1,0}, v_{2,0}, v_{3,0})$
    \State $QR(0,1, v_{1,1}, v_{2,1}, v_{3,1})$
    \State $QR(0,2, v_{1,2}, v_{2,2}, v_{3,2})$
    \State $QR(0,3, v_{1,3}, v_{2,3}, v_{3,3})$
    \State $QR(0,0, v_{1,0}, v_{2,1}, v_{3,1})$
    \State $QR(0,1, v_{1,2}, v_{2,2}, v_{3,2})$
    \State $QR(0,2, v_{1,3}, v_{2,3}, v_{3,3})$
    \State $QR(0,3, v_{1,0}, v_{2,1}, v_{3,2})$
  \EndFor
  \State $V \leftarrow V \oplus M$; \hspace{1em} // Entry-Wise 32-bit Sum
  \State \Return $V$;
\end{algorithmic}

where cst$_0 = 0x61707865$, cst$_1 = 0x3320646E$, cst$_2 = 0x79622D32$ and cst$_3 = 0x6B206574$ is predefined. The counter $CTR = (\text{ctr}_0, \text{ctr}_1)$ corresponds to the message block index $i$. In order to process the $i$-th message block, the initial state matrix $M$ is transformed in a series of $N$ rounds, where according to [1] $N$ is suggested to be set to 8, 12 or 20 (see Algorithm 1). The ChaCha algorithm allows to process two rows of $V$. In this, even-numbered rows affect the columns of the matrix $V$, while odd-numbered rows modify the diagonal elements of $V$. Both transformations apply the nonlinear Quarterround function shown in Algorithm 2. Each Quarterround $QR(a, b, c, d)$ is based on four additions in $\mathbb{F}_{2^{32}}$, four XORs and four rotations which operate on the 32-bit input words $a, b, c$ and $d$. A Quarterround updates each input word twice, allowing each input word to affect the other words.

Algorithm 2: $QR(a, b, c, d)$

\begin{algorithmic}
  \State \textbf{Input} : $a, b, c, d \in \mathbb{F}_{2^{32}}^{4}$
  \State \textbf{Output:} $a, b, c, d \in \mathbb{F}_{2^{32}}^{4}$ (Updated Values).
  \State $a \leftarrow a \oplus b$; \hspace{1em} // $a^0 \leftarrow a \oplus b$
  \State $d \leftarrow (d \oplus a) \ll 16$; \hspace{1em} // $d^0 \leftarrow d \oplus a, d^1 \leftarrow d^0 \ll 16$
  \State $c \leftarrow c \oplus d$; \hspace{1em} // $c^0 \leftarrow c \oplus d$
  \State $b \leftarrow (b \oplus c) \ll 12$; \hspace{1em} // $b^0 \leftarrow b \oplus c, b^1 \leftarrow b^0 \ll 12$
  \State $a \leftarrow a \oplus b$; \hspace{1em} // $a^0 \leftarrow a \oplus b$
  \State $d \leftarrow (d \oplus a) \ll 8$; \hspace{1em} // $d^2 \leftarrow d^3 \oplus a, d' \leftarrow d^2 \ll 8$
  \State $c \leftarrow c \oplus d$; \hspace{1em} // $c' \leftarrow c^0 \oplus d'$
  \State $b \leftarrow (b \oplus c) \ll 7$; \hspace{1em} // $b^2 \leftarrow b^3 \oplus c', b' \leftarrow b^2 \ll 7$
  \State \Return;
\end{algorithmic}

IV. PARITY-BASED CODE-DISJOINT CIRCUIT

In this section we describe a parity-based code-disjoint circuit [10] for the Quarterround (Algorithm 2), which is the essential part of ChaCha [1]. We investigate its resistance against transient and permanent faults, that can affect the input signals $a, b, c, d \in \mathbb{F}_{2^{32}}^{4}$, as well as the intermediate signals $a^0, b^0, c^0, d^0, b^1, b^2, d^1, d^2 \in \mathbb{F}_{2^{32}}^{4}$ given in the comments of Algorithm 2.

For the following analysis we consider the data path of a Quarterround as illustrated on the left side of Fig. 1. The right side of Fig. 1 shows our group-based parity prediction, which is part of Section V. The input of the data path is $a, b, c, d \in \mathbb{F}_{2^{32}}$ and the output are the vectors $a', b', c', d' \in \mathbb{F}_{2^{32}}^{2}$. The following four intermediate signals in $\mathbb{F}_2$ are defined as

$$
\alpha \overset{\text{def}}{=} p(cv(a, b)), \quad \beta \overset{\text{def}}{=} p(cv(c, d^1)),
\gamma \overset{\text{def}}{=} p(cv(a^0, b^1)), \quad \delta \overset{\text{def}}{=} p(cv(b^0, d^1)),
$$

(4)

where $cv(a, b)$ denotes the carry vector of $a$ and $b$ given in (3). The four intermediate bits $a, \beta, \gamma, \delta$ defined in (4) will, in addition to $a, b, c, d \in \mathbb{F}_{2^{32}}^{4}$, be used to transform a Quarterround into a code-disjoint circuit. Further on, they are used for our group-based parity approach (GBPP) (described in Section V).

A parity-based code-disjoint circuit [10] extends the classical parity prediction by additionally encoding the inputs of a given circuit into codewords of the parity code. Hence, we first develop a parity prediction for one Quarterround.

**Definition 1 (Parity Prediction).** Let $f$ be a function with input $x \in \mathbb{F}_2^m$ and output $y \in \mathbb{F}_2^n$. A parity prediction $pp_f$ of $f$ is a function, such that

$$pp_f(x) = p(f(x)) = p(y), \quad \forall x \in \mathbb{F}_2^m.$$  

The design of the parity prediction $pp_f$ for a given function $f$ can be optimized in terms of, e.g., gate count and/or error coverage.

Now, we develop a parity prediction for Algorithm 2, where $m = n = 128$, $x = (a \ b \ c \ d)$ and $y = (a' \ b' \ c' \ d')$ according to Def. 1. Therefore, we calculate four parity bits for each component of the output vector $(a' \ b' \ c' \ d')$.

**Lemma 2 (Parity Prediction of $a'$).** Consider the output $a' \in \mathbb{F}_2^{32}$ of a Quarterround given in Algorithm 2. Its parity bit is

$$p(a') = p(b) \oplus p(c) \oplus p(d) \oplus \beta \oplus \gamma.$$  

**Proof:** With (2) for the output signal $a' = a^0 \oplus b^1$, we have

$$p(a') = p(a^0) \oplus p(b^1) \oplus \gamma = p(a^0) \oplus p(b) \oplus p(c) \oplus p(d) \oplus \beta \oplus \gamma,$$

and with $p(c') = p(c) \oplus p(d')$, we obtain

$$p(a') = p(a^0) \oplus p(b) \oplus p(c) \oplus p(d) \oplus \beta \oplus \gamma. \quad (5)$$

Inserting $p(d^0) = p(a^0) \oplus p(d)$ in (5) leads to

$$p(a') = p(a^0) \oplus p(b) \oplus p(c) \oplus p(a^0) \oplus p(d) \oplus \beta \oplus \gamma,$$

where $p(d) = p(d) \oplus \beta \oplus \gamma.$

**Lemma 3 (Parity Prediction of $b', c', d'$).** Consider the outputs $b', c', d' \in \mathbb{F}_2^{32}$ of a Quarterround given in Algorithm 2. Their parity bits are

$$p(b') = p(a) \oplus p(b) \oplus p(c) \oplus \alpha \oplus \beta \oplus \gamma \oplus \delta,$$

$$p(c') = p(b) \oplus p(d) \oplus \gamma \oplus \delta,$$

$$p(d') = p(a) \oplus p(c) \oplus \alpha \oplus \beta \oplus \gamma.$$  

**Proof:** Similar to the proof of Lemma 2.

**Theorem 4 (Parity Prediction of a Quarterround).** Let $(a' \ b' \ c' \ d') \in \mathbb{F}_2^{128}$ be the output of a Quarterround given in Algorithm 2. Its parity bit is

$$pp_{QR}(a, b, c, d) = p(b) \oplus p(c) \oplus \beta.$$  

**Proof:** Due to space limitations, we omit the proof.

Note that the direct calculation of the parity bit of a Quarterround as given by Thm. 4 can be realized by 64 gates to determine the parities of the inputs, i.e., 31 XOR gates for the calculation of $p(b)$ (resp. $p(c)$), and two XOR gates to calculate $p(b) \oplus p(c) \oplus \beta$. Another 127 gates are needed to calculate the parities of the output $(a' \ b' \ c' \ d')$ and one XOR gate to compare the parities. This results in 192 two-input XOR gates.

The following corollary states the circuit for transforming a Quarterround into a code-disjoint circuit as proposed in [10]. In addition, it allows to detect an odd-weight error affecting the input $(a \ b \ c \ d)$.

**Corollary 5 (Single Output Code-Disjoint Circuit).** Let the input and output as well as the parity prediction be as in Thm. 4. Then

$$p((a' \ b \ c \ d)) \oplus pp_{QR}(a, b, c, d) = p(a) \oplus p(d) \oplus \beta.$$  

To obtain the error coverage, we consider errors $e \in \mathbb{F}_2^{32} \setminus \{0\}$ on the intermediate signals $a^0, b^0, b^1, b^2, c^0, c^1, d^0, d^1, d^2$ of Algorithm 2. Therefore, we define the following two notations of affected vectors.

**Notation 6 (Erroneous Vector).** Let $a \in \mathbb{F}_2^{32}$ and $e \in \mathbb{F}_2^{32} \setminus \{0\}$. An erroneous vector $\tilde{a}$ is defined as $\tilde{a} = a \oplus e$.

**Notation 7 (Potentially Error-Affected Vector).** Let $a \in \mathbb{F}_2^{32}$ and $e_c \in \mathbb{F}_2^{32}$. A vector, that can be affected by an error is denoted as $\tilde{c} = c \oplus e_c$.

Using Notation 6 and 7 and for $c = p(a \oplus b)$, the parity bit of the modulo addition as in (2) with erroneous input $\tilde{a}$ is

$$\tilde{c} = p(\tilde{a} \oplus b) = p(\tilde{a}) \oplus p(b) \oplus p(cv(\tilde{a}, b)), \quad (6)$$

where $cv(\tilde{a}, b) = cv(a, b) \oplus e_c$. The weight of $e_c \in \mathbb{F}_2^{32}$ can be different from the weight of $e$ (it can even be zero).

**Lemma 8 (Detectable Errors Affecting $b^0$).** Assume an error $e \in \mathbb{F}_2^{32}$ with odd Hamming weight is added to the intermediate signal $b^0$ in the data path of a Quarterround (Algorithm 2). Then, the parity prediction as in Thm. 4 will detect it.

**Proof:** The initially corrupted vector is $b^0 = b^0 \oplus e$ and affects $b^1$ and the output signal $b'$. Possible corrupted intermediate signals are $\gamma, \delta, b^2$, and the output signals $a', b', c', d'$. The parity bit of $b'$ calculated by Algorithm 2 is as follows:

$$p(b') = p(\tilde{b}^0) \oplus p(c'), \quad (7)$$
and for $\overline{d}'$, we have
\[ p(\overline{d}') = p(\overline{a}') \oplus p(d^1). \] (8)

Clearly, for the calculated parity we have:
\[ p((\overline{a}' \overline{b}' \overline{c}' \overline{d}')) = p(\overline{a}') \oplus p(\overline{b}') \oplus p(\overline{c}') \oplus p(d') \] (9)
and inserting (7) and (8) into (9) gives:
\[ p(\overline{a}') \oplus p(\overline{b}') \oplus p(\overline{c}') \oplus p(d') = p(\overline{a}') \oplus p(\overline{b}') \oplus p(\overline{c}') \oplus p(d') \]
\[ = p(\overline{b}') \oplus p(d'). \] (10)

The calculated parity $p_{GBPP}(a, b, c, d)$ as given in Thm. 4 is not affected by $e$. Hence, the difference between $p_{GBPP}(a, b, c, d)$ and (10) is $p(e)$ and therefore will be nonzero if $e$ has odd Hamming weight.

\section*{Algorithm 3: $GBPP(p(a), p(b), p(c), p(d), \alpha, \beta, \gamma, \delta)$}
\begin{algorithmic}[1]
  \STATE $p(a) \leftarrow p(a) \oplus p(b) \oplus \alpha$;
  \STATE $p(d) \leftarrow p(d) \oplus p(a)$;
  \STATE $p(c) \leftarrow p(c) \oplus p(d) \oplus \beta$;
  \STATE $p(b) \leftarrow p(b) \oplus p(c)$;
  \STATE $p(a) \leftarrow p(a) \oplus p(b) \oplus \gamma$;
  \STATE $p(d) \leftarrow p(d) \oplus p(a)$;
  \STATE $p(c) \leftarrow p(c) \oplus p(d) \oplus \delta$;
  \STATE $p(b) \leftarrow p(b) \oplus p(c)$;
  \STATE return
\end{algorithmic}

\section*{Lemma 9 (Detectable Errors Affecting $e^0$).} Assume an error $e \in \mathbb{F}_2^{32}$ with odd Hamming weight is added to the intermediate signal $e^0$ in the data path of a Quarterround (Algorithm 2). Then, the parity prediction as in Thm. 4 will detect it.

\textbf{Proof:} Similar to the proof of Lemma 8. ■

\section*{Theorem 10 (Error Coverage of Code-Disjoint Circuit for Algorithm 2).} The single output code-disjoint circuit as stated in Corollary 5 for Algorithm 2 detects every odd-weight error $e \in \mathbb{F}_2^{32}$ that affects

\begin{itemize}
  \item \textbf{E1)} the input signals $a, b, c, d$,
  \item \textbf{E2)} the intermediate signals $b^0, c^0, b^1, d^1$, and
  \item \textbf{E3)} the output signals $b', d'$.\end{itemize}

\textbf{Proof:} The statement E1 follows from the properties of a code-disjoint circuit as proven in [10]. The coverage on odd-weight errors on $b^0$ (resp. $c^0$) was proven in Lemma 8 (resp. Lemma 9). From this the coverage for $b^1$ (resp. $b^2$) follows. The coverage of odd-weight errors that affect $d^2$ and the output signal $d'$ is similar: The error that propagates via the addition to the output signal $c'$ is copied to $b'$ and therefore is canceled out in the sum $p(\overline{b}') \oplus p(\overline{c}')$, but the parity of $d'$ is affected and therefore detected. Clearly, an odd-weight error affecting $b'$ (as stated in E3) is covered, because no other output signals are affected.

Note that, errors in the intermediate signals $a^0, d^0, d^1$, and in the output signals $a', c'$ are not detected.

\section*{V. Our Group-Based Parity Prediction}

To further improve the error coverage for hardware implementations of the ChaCha algorithm, we apply the method of parity prediction to the processed 32-bit words. Our approach calculates a parity bit for each of the four 32-bit components $a, b, c, d$ of the input vector of a Quarterround (Algorithm 2) of ChaCha. Fig. 1 illustrates our group-based parity prediction (Algorithm 3). Algorithm 3 outputs updated values of

\begin{figure}[ht]
\centering
\includegraphics[width=\textwidth]{fig1.png}
\caption{Our group-based parity prediction for one Quarterround of ChaCha.}
\end{figure}

\begin{itemize}
  \item $p(a), p(b), p(c), p(d)$ and processes the intermediate signals $a^0, b^0, b^1, d^1$, and
  \item \textbf{E3)} the output signals $b', d'$.
\end{itemize}
Algorithm 3 is the direct translation of Algorithm 2 using (2) and (1) and the fact that the parity-bit is not changed by a bit-wise rotation (marked by \( \ll \) in Algorithm 3).

We prove the error coverage of our approach (Algorithm 3) and give an estimation of the area usage in terms of required gates.

In the following, we analyze the error coverage of the proposed parity prediction scheme (Algorithm 3) for the intermediate signals \( a^0, b^0, c^0 \) and \( d^0 \) (see Lemma 11, 12). The error coverage of the remaining intermediate signals, i.e., \( b^1, b^2, d^1, d^2 \) is then summarized in Thm. 13.

**Lemma 11** (Detectable Errors Affecting \( a^0 \)). Assume an error \( e \in \mathbb{F}_2^3 \) of odd Hamming weight is added to \( a^0 \) in the data path of a Quarterround (Algorithm 2). Then, at least one output of our group-based parity prediction in Algorithm 3 will detect it.

**Proof:** The error \( e \) on \( a^0 \) can affect the intermediate signals \( \beta, \gamma, \delta, b^0, b^1, c^0, d^0, d^1, d^2, b^2 \), as well as all output vectors \( a', b', c' \) and \( d' \). The initially corrupted vector is \( a^0 = a^0 + e \). The parity bit calculation based on the output vector \( d' \) of the data path (Algorithm 2) can be expressed as follows:

\[
p_d(d') = p(a^0) \oplus p(b) \oplus p(c) \oplus p(d^1) \oplus p(\overline{\beta}) \oplus p(\overline{\gamma}) = p(a^0) \oplus p(b) \oplus p(c) \oplus p(d^1) \oplus p(\overline{\beta}) \oplus p(\overline{\gamma}).
\]

(11)

and with \( b^0 = b \oplus d^1 = b \oplus (c \oplus d^1) = b \oplus c \oplus d^1 \oplus \beta \), we obtain from (11),

\[
p_d(d') = p(\overline{\beta}) \oplus p(b) \oplus p(c) \oplus p(\overline{\gamma}) \oplus p(\overline{d^1}) \oplus p(\overline{\beta}) \oplus p(\overline{\gamma}) \oplus p(\overline{d^1}).
\]

(12)

The fourth output bit of our group-based parity prediction can be similarly expressed. In addition, it is possibly affected by the error via \( \beta \) and \( \gamma \), i.e.:

\[
p(d') = p(a^0) \oplus p(b) \oplus p(c) \oplus p(d^1) \oplus p(\overline{\beta}) + p(\overline{\gamma}) \oplus p(\overline{\gamma});
\]

(13)

Therefore the comparison of the calculated parity \( p_d(d') \) of \( d' \) from the data path as given in (12) and our parity prediction given in (13) is

\[
p_d(d') \oplus p(d') = p(e)
\]

and will be nonzero if \( e \) has odd Hamming weight. ■

**Lemma 12** (Detectable Errors Affecting \( b^0, c^0, d^0 \)). Assume an error \( e \in \mathbb{F}_2^3 \) of odd Hamming weight is added to \( b^0 \) or \( c^0 \) or \( d^0 \) in the data path of a Quarterround (Algorithm 2).

**Proof:** Similar to the proof of Lemma 11. ■

**Theorem 13** (Odd-Weight Error on All Intermediate Signals of A Quarterround). Our group-based parity prediction according to Algorithm 3 for the Quarterround (Algorithm 2) detects every odd-weight error \( e \in \mathbb{F}_2^3 \) that affects

E1) the intermediate signals \( a^0, b^0, c^0, d^0, b^1, b^2, d^1, d^2 \)

E2) the intermediate signals \( \alpha, \beta, \gamma, \delta \) and

E3) the output signals \( a', b', c', d' \).

**Proof:** Due to space limitations, we omit the proof. ■

The GBPP requires overall 265 gates. These are: 124 XOR gates for the calculation of the parity of the input words \( a, b, c, d \), another 124 XOR gates for the parity of the outputs \( a', b', c', d' \), 12 additions, and 4 XOR gates in combination with a 4-input OR gate to merge the results of the four parity bit comparisons. With the usage of fault secure adders as proposed in [5], it is possible to detect any odd-weight error on input, output and intermediate signals.

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