Nanoscale silicon field emitter arrays with self-aligned extractor and focus gates

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Abstract

Out-of-plane focusing is essential for electron beam collimation in gated field emission sources. The focus electrode redirects electrons emitted by the tip with a wide angle towards the central axis, resulting in a small focal spot at the anode. Here, we demonstrate for the first time, very high density (10^8 emitters/cm^2) arrays of double-gated field emission electron sources with self-aligned apertures and integrated nanowire current limiters. Release of the emitters after fabrication required the combination of a highly selective dry-etch and an isotropic wet-etch to avoid the loss of the insulator between the two gates. The aperture diameters are ∼360 nm and ∼570 nm for the extractor gate and focus gate, respectively. The turn-on voltage was low (15-20) V and anode currents of 400 nA were measured at 25 V. We compared devices with different extractor gate thicknesses resulting from planarization non-uniformity, and demonstrate the influence of the focus gate on anode current. The focal spot size was measured, using a low energy phosphor screen, to be around 700 µm for a 500 µm device when the V_{FE}/V_{GE} ratio was 0.35.

Keywords: vacuum nanoelectronics, field emission, electron focusing, silicon

(Some figures may appear in colour only in the online journal)

1. Introduction

Spindt cold electron sources, pioneered in 1968, paved the way for a range of applications based on cold field emission including flat panel displays, x-ray sources, neutron generators, microwave tubes and triodes [1–6]. In contrast to thermionic sources, cold electron emitters rely on field emission, whereby electrons tunnel across a potential barrier that has been narrowed using a strong electrostatic field [7,8]. Cold cathodes, therefore, have low operating temperature, instantaneous response to the applied electric field and exponential current-voltage (I-V) characteristics [9,10]. Such electron emitters, however, are limited by non-zero tip radius distribution due to variations in the fabrication process and current fluctuations caused by adsorption/desorption of molecules [11,12]. Several approaches have been developed to improve the tip radius uniformity and the current stability. These include reduction of the tip radius, decrease of the gate aperture, and limiting the maximum emitter current by a voltage-controlled current source [13]. Active current control using a metal-oxide semiconductor field effect transistor (MOSFET) and passive methods using a vertical high aspect ratio nanowire, which functions as a current limiter, have already been demonstrated [14–18]. The latter is usually the preferred method for dense arrays as each emitter tip has its own integrated current limiter [19].

Si-based field emission sources have additional merits such as their compatibility with silicon complementary metal oxide semiconductor (CMOS) processes, maturity of technology and the ease of forming atomically sharp tips using oxidation of silicon [20]. A high aspect ratio Si nanowire, etched immediately after the tip definition, can mitigate early tip burn-out [19,21]. Additionally, with self-aligned gate apertures and a reduced emitter pitch, higher current densities, J, and lower turn-on
voltages, $V_{em}$, are achieved [22–24]. Using a mesa structure surrounded by a thick oxide to isolate electrical pads, can further reduce the gate-emitter capacitance and improve the gate to substrate breakdown voltage [16,25]. Such Si FEAs with 1 $\mu$m pitch with single self-aligned gate apertures (350 nm diameter) have been reported by Guerrera and Akinwande [16], demonstrating values of $J$ exceeding 150 A/cm$^2$ and operating lifetimes longer than 100 hours. In such Si FEAs, however, the horizontal velocity of electrons from the emission surface is non-zero, resulting in an angular spread (cone angle $\sim 12^\circ$) of the electron beam reaching the anode [26,27]. For applications requiring high anode voltages such as x-ray imaging, this beam spread is further exacerbated as the anode needs to be at distances exceeding 1 mm in order to prevent electrical breakdown. With the angular spread, electron trajectories follow a parabolic path to the anode. In higher density arrays, this can lead to cross-talk and therefore, lower resolution of displays, multi-beam lithography and imaging applications, which would often require a trade-off with luminosity [28,29]. It is therefore, crucial to obtain a focused electron beam.

Common methods to collimate the electrons include magnetic focusing, which is used in scanning electron microscopes, but these can only be applied at a global level and are best suited to single emitters [30]. Local focusing of each individual electron source in FEAs cannot be achieved by magnetic field confinement solely. Energized mesh grids focusing of electron beams are potential alternatives, but stray electrons may be intercepted. In addition, aligning the mesh grid with the emitter tips could be challenging and, the grid voltage needs to be large due to its distance from the emitters. Similarly, electron-transparent graphene membranes, reported by Li et al [31], can function as an electron beam focusing structure; although applying a graphene layer on gated field emitter arrays can result in high gate leakage currents due to electron interception. In order to achieve local focusing of each field emitter, an additional out-of-plane gate is therefore, necessary to provide a counter electrostatic force that can reduce the lateral velocity of the electrons [32,33]. This second gate can be further used to control the spot size of the beam to compensate for the widening of the emission spot size due to the increase in tip radius, which may occur when the emitters are operated at high currents continuously over a long time [34].

To achieve low voltage and, to integrate self-aligned focus gates on dense (10$^8$ emitters/cm$^2$) Si FEAs with nanowire current limiters, we fabricated and characterized devices based on the previous work in [16]. The addition of self-aligned out-of-plane focus gate apertures enables this electrode to function as an electrostatic lens. We describe the fabrication process flow, and by characterizing the fabricated devices, we modeled the electrostatic influence of the second gate on the emitter and its effect on electron trajectories. The double-gated Si FEAs are measured electrically and the spot size of the electron beam is estimated using a low-voltage phosphor screen. To our knowledge, this is the densest double-gated Si FEAs fabricated, as compared to previous works [32,35,36].

2. Methods

2.1. Fabrication of double-gated Si field emitter arrays

Double-gated Si FEAs, shown schematically in figure 1, were fabricated on 150 mm diameter and 650 $\mu$m thick $n$-type
(Resistivity, $\rho = 1-4 \ \Omega \cdot \text{cm}$ doped with phosphorus) Si wafers with $\langle 100 \rangle$ orientation.

The key steps in the fabrication were characterized by scanning electron microscope (SEM) (Zeiss Supra 40, Oberkochen, Germany) and are illustrated in figure 2. Mesas with depth of 3 $\mu m$ were first etched (figure 2(a)) and filled with 5 $\mu m$ of plasma enhanced chemical vapor deposition (PECVD) of SiO$_2$. A chemical mechanical planarization (CMP) step was used to planarize the wafers, stopping on the exposed Si mesa. After depositing a 150 nm SiO$_2$ hard mask by PECVD, the emitter arrays (discs of 500 nm diameter and 1 $\mu m$ pitch) were patterned by $i$-line photolithography and dry-etched. A semi-isotropic (aspect ratio 2:1) process using SF$_6$/He chemistry formed cones of approximately 100 nm in width and height of $\sim 200$ nm as shown in figure 2(b). A deep-reactive ion etching process was subsequently used to form high aspect ratio (40:1) Si pillars of 8-10 $\mu m$ in height (figure 2(c)). After removing the hardmask by a timed buffered oxide etch (BOE), sharp tips and narrower pillars were achieved by a dry oxidation at 950 $^\circ$C for 6.5 hours (figure 2(d)). A dielectric matrix consisting of SiN$_x$ and SiO$_2$ was then used to fill the gaps (voids) in between the Si pillars as shown in figure 2(e). This was carried out by the sequential process of depositing undoped poly-Si of 50 nm thickness by low-pressure chemical vapor deposition (LPCVD), dry-oxidation for 6.5 hours at 950 $^\circ$C in O$_2$ and LPCVD of low-stress SiN$_x$ with $\sim 1 $ $\mu m$ thickness. A CMP step was used to planarize the surface followed by wet-etching in hot phosphoric acid at 165 $^\circ$C to form oxide domes of around 300 nm height (figure 2(f)).

An 800 nm thick, and $n$-type doped poly-Si gate was then deposited by LPCVD, and the extractor gate apertures were carefully opened using CMP as shown in figure 2(g) and figure 2(h), respectively. The poly-Si gate was slightly recessed by a selective dry etch using Cl$_2$/HBr/Ar gas combination to form domes of around 100 nm (figure 2(i)) that would be used to define the thickness of the focus gate. Due to the non-uniformity of the CMP process, this step is critical to the position of the tip relative to the extractor gate. To separate the extractor gate from the focusing gate, a 350 nm thick SiO$_2$ was deposited by PECVD and annealed at 950 $^\circ$C in N$_2$ to densify the oxide as illustrated in figure 2(j). Poly-Si

Figure 3. Atomic force microscope (AFM) characterization of the process after the dielectric fill-in step showing the surface profile, three-dimensional view and height profile across the center: (a) nitride deposition, (b) chemical mechanical planarization (CMP) and phosphoric acid etch, (c) first gate deposition, (d) gate aperture opening, (e) gate dry etch, (f) insulator deposition, (g) focus gate deposition, (h) focus gate aperture opening. All scale bars are 1 $\mu m$. 

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(n-type doped) with a thickness of 800 nm was then deposited by LPCVD to form the focus gate (figure 2(k)). The poly-Si layer was planarized carefully to form the second gate aperture as depicted in figure 2(l). The most important part of the process to prevent gate collapse was to perform a partial tip release using a highly selective dry etch of oxide to poly-Si, using CHF$_3$/CF$_4$/Ar chemistry and timed to ensure the tip was not exposed (figure 2(n)). The focus gate, insulator and the extractor gates were patterned and dry-etched sequentially (figure 2(m)). The metal contacts were then patterned using image reversal resist and a metal stack consisting of Ti (10 nm)/Au (200 nm) was deposited at the back of the wafer for the emitter contact. To complete the process, the emitter tips were carefully exposed by a timed wet-etch (approximately 90 s) using diluted (1:10) commercial pad etchant Silox Vapox III (figure 2(o)). Each chip on the wafer was 1.5 cm by 1.5 cm, with 121 (11 by 11) devices of 500 × 500 emitters with emitter pitch of 1 µm, and device pitch of 1 mm.

Critical steps illustrated in figure 2(e)–(l) were also characterized using atomic force microscopy (High resolution scanning probe microscope, Veeco D3100, Plainview, NY, USA) in tapping mode as shown in figure 3. After the deposition of low-stress SiNx, the measured heights were approximately 120 nm (figure 3(a)), which after planarization and etch-back resulted in oxide domes approximately 250 nm in height (figure 3(b)). Figures 3(c)–(e) show the deposition, planarization and etch-back of the first poly-Si layer to fabricate features of approximately 120 nm in height. The deposition of the 350 nm thick oxide insulator reduced the dome height to 100 nm (figure 3(f)). After the deposition of poly-Si for the focusing gate (figure 3(g)), and its planarization (figure 3(h)), the second gate aperture with larger diameter was formed.

### 2.2. Electrical characterization of double-gated Si FEAs

The fabricated arrays of field emitters were characterized using four source-measurement units (SMUs) as a four terminal device in an ultra-high vacuum chamber (UHV) reaching 2 × 10$^{-9}$ Torr. Vacuum was maintained by an ion pump and the pressure was recorded using a Bayard-Alpert ion gauge. Four SMUs (Keithley Instruments model 2657 A) were used for the J-V characterizations, and connected to the device by means of miniature high voltage (MHV) electrical feed-throughs and tungsten micro-manipulator probes. A tungsten ball of (∼0.5 mm in diameter) was used as the anode positioned at approximately 3 mm from the surface of the chip and biased at a voltage of 1.1 kV for the electrical characterization. This anode voltage was chosen to minimize anode heating and hence out-gassing during the sweeps, which could generate energetic ions that erode the tip or damage the gates.

Figure 4. (a) SEM of an array of double-gated Si field emitters, (b) magnified image showing the two self-aligned gates and emitter tip, and (c) histogram and box plots of the measured distribution of 120 apertures.
to produce an observable spot size. A high resolution, CCD (charge-coupled display) camera (Thorlabs Inc, Newton, NJ, USA, model: 8051 C-USB) with 8 MPixel resolution, attached to a long throw microscope, was used to capture the image in a dark room. Images were recorded by focusing the microscope on the phosphor screen and using ThorCam™ software (v3.3.1), with exposure time of 60 s and maximum gain of 1023. The long exposure time and large gain were due to the low photon yield of the phosphor at low bias voltages on the screen. The captured images were then converted to grayscale and the contrast was set to 100% and brightness between 60% to 75% to compare the edge of the spot.

3. Results

3.1. Aperture diameter measurements

Completed double-gated Si FEAs are shown in figure 4(a) and (b). The SEM image of a 500 × 500 array (figure 4(a)) was loaded and analyzed in Fiji [37] to measure the diameters of each aperture. A histogram and box plot of 120 measured aperture diameters are plotted in figure 4(c).

Using the arithmetic mean, μ, and the standard deviation, σ, the aperture diameter was measured to be (361 ± 22) nm and (350 ± 30) nm for the extractor gate and focus gate, respectively. These were close to the median, M, and interquartile, IQ, range (M = 363 nm and IQ = 28 nm for the extractor gate and M = 567 nm and IQ = 43 nm for the focus gate), represented by the box and whisker plot in figure 4(c). The deviation of the aperture focus gate aperture diameter was slightly larger than the extractor gate possibly because of the release step where the focus gate was fully exposed to the dry etch, which increased the non-uniformity in the lateral direction.

3.2. Field factor modeling

To study the effect of the two gates on the emission current, the extractor gate-emitter (V_{GE}) voltage was varied from 0 to 25 V whereas the focus-emitter voltage (V_{FE}) was maintained at a ratio of 1.0, 0.9, 0.8, 0.7 and 1.1, respectively. Focus transfer characteristics of the anode current with were measured by fixing V_{GE} at a constant bias and sweeping V_{FE} from 0 to 30 V.

2.3. Optical characterization of spot size

To measure the spot size of the double-gated Si FEAs, the ball anode was changed to a phosphor screen (diameter of 1 cm and 1 mm thick), which was energized to the maximum output voltage of 3 kV of the SMU, and positioned at approximately 10 mm above the device. The phosphor screen (model P43), which was coated with indium tin oxide (ITO) was purchased from Beam-imaging Solutions Inc (Longmont, CO, USA) with quantum yield of 0.05; low voltage phosphor gives higher resolutions but lower number of photons. For this reason, V_{GE} was carefully increased to approximately 35 V to get anode currents in excess of 1 μA at the phosphor screen

| V_{FE}/V_{GE} | I_{A} [nA] @ 25 V | b_{FN} [V] | \log(\alpha_{FN}) | \beta_{eff} [10^6/cm] |
|----------------|-----------------|----------|-----------------|----------------|
| 1.1            | 429             | 350      | -6.9            | 1.522          |
| 1.0            | 452             | 265      | -10.2           | 2.011          |
| 0.9            | 354             | 324      | -8.2            | 1.661          |
| 0.8            | 260             | 321      | -8.6            | 1.664          |
| 0.7            | 141             | 342      | -8.3            | 1.554          |
superposition, the electric field, $F$, at the tip due to the gate-emitter voltage, $V_{GE}$, and the focus-emitter voltage, $V_{FE}$, is given by (1):

$$F = \beta_{G}V_{GE} + \beta_{F}V_{FE}$$

where $\beta_{G}$ and $\beta_{F}$ are the field factors at the tip due to the gate and the focus electrode, respectively. With a linear fit of $\beta_{eff}$ against $V_{FE}/V_{GE}$, the individual field factors can be extracted with $\beta_{G}$ as the intercept and $\beta_{F}$ as the gradient. Accordingly, by finding the maximum field at the emitter tip for different $V_{FE}/V_{GE}$ ratios in the simulation, the fitted slope and intercept of a linear equation was used to find the individual field factors, as shown in figure 5.

The dependence of $\beta_{eff}$, $\beta_{G}$ and $\beta_{F}$ on $r$ when the apex of the emitter is level ($h = 0$) with the center of the extractor gate were calculated to be (2), (3) and (4), respectively:

$$\beta_{eff}(r, \ h = 0, V_{FE} = V_{GE}) = \frac{3.02 \times 10^{6}}{r^{0.661}}$$

$$\beta_{G}(r, \ h = 0) = \frac{2.82 \times 10^{6}}{r^{0.664}}$$

$$\beta_{F}(r, \ h = 0) = 2.06 \times 10^{5} \rho_{0.627}$$

At all tip radii, $\beta_{G}$ was larger than $\beta_{F}$ by an order of magnitude if the tip was level ($h = 0$) with the center of the extractor gate. However, when the tip was closer to the focus gate, and above the extractor gate ($h > 100$), $\beta_{F}$ increased substantially while $\beta_{G}$ was reduced as shown in figure 5(b). This was because the

Table 2. Extracted FN parameters for different $V_{FE}/V_{GE}$ ratios in the case where the tips are above the extractor gate.

| $V_{FE}/V_{GE}$ | $I_{A} \ [nA] @ 25 \ V$ | $b_{FN} \ [V]$ | $\log(a_{FN})$ | $\beta_{eff} \ [10^{6}/cm]$ |
|-----------------|----------------|----------------|----------------|----------------|
| 1.1             | 6.5            | 526            | -5.2           | 1.012          |
| 1.0             | 5.8            | 478            | -7.2           | 1.105          |
| 0.9             | 3.7            | 533            | -5.6           | 1.000          |
| 0.8             | 2.1            | 539            | -5.7           | 0.986          |
| 0.7             | 1.1            | 592            | -4.3           | 0.900          |

Figure 7. (a) Electrical characteristics measured at different $V_{FE}/V_{GE}$ ratios with anode voltage at $+1100$ V for a device located near the edge of the chip. (b) FN plot of the measured anode current demonstrating FN behavior at $V_{GE} > 20$ V. (c) Average and standard deviation of effective field factor measured for 3 sweeps plotted against $V_{FE}/V_{GE}$ ratio to extract $\beta_{G}$ and $\beta_{F}$.

Figure 8. (a) Transfer characteristics of the focus gate measured at different $V_{GE}$ bias with anode voltage at $+1100$ V and device close to the center of the chip. Inset shows the FN plot of the data. (b) Transfer characteristics of focus gate for device closer to the perimeter of chip, with the inset showing the corresponding FN plots.
emitter tip was less shielded by the extractor gate, and due to the proximity of the emitter to the focus aperture, a larger electric field was exerted on the emitter by the focus gate. At $h > 200 \text{ nm}$, the emitter was above the extractor gate hence, $\beta_F$ exceeded $\beta_G$. The relation between $\beta_G$ and $\beta_F$ with $h$ were non-trivial, and accordingly not derived for simplicity.

### 3.3. Gate and focus transfer characteristics

The anode current, $I_A$, in a single-gated device with $V_{GE}$ based on the Fowler-Nordheim (FN) equation for tunneling across a triangular barrier, is given by (5) [8]:

$$I_A = a_{FN} V_{GE}^2 \exp \left( - \frac{b_{FN}}{V_{GE}} \right)$$  \hspace{1cm} (5)

where $a_{FN}$ and $b_{FN}$ are given by (6) and (7) respectively:

$$a_{FN} = \frac{\alpha A \beta^2}{1.1 \phi} \exp \left[ \frac{B \cdot 1.44 \times 10^{-7}}{\sqrt{\phi}} \right]$$  \hspace{1cm} (6)

$$b_{FN} = \frac{0.95 \cdot B \cdot \phi^{3/2}}{\beta}$$  \hspace{1cm} (7)

where $\alpha$ is the barrier correction factor, $A$ and $B$ are the constants from the FN formulation of electron emission with values of $1.54 \times 10^{-6}$ and $6.87 \times 10^{7}$, respectively, and $\phi$ is the work function of Si, which can be approximated to the electron affinity, $\chi_{Si}$, with value of $4.05 \text{ eV}$ for $n$-type Si [16]. In (5)–(7), it is assumed that the dielectric constant of the semiconductor has a minimal impact on the image force effect and that the work function is not changed by the field due to field penetration. With the focusing electrode in a double-gated structure, $I_A$ from (5) can be extended to include $\beta_{eff}$, given by (8):

$$I_A = a_{FN} V_{GE}^2 \exp \left( - \frac{0.95 \cdot B \cdot \phi^{3/2}}{\beta_{eff} V_{GE}} \right)$$  \hspace{1cm} (8)

where $a_{FN}$ is also modified to include $\beta_{eff}$ as shown in (9):

$$a_{FN} = \frac{\alpha A \beta^2}{1.1 \phi} \exp \left[ \frac{B \cdot 1.44 \times 10^{-7}}{\sqrt{\phi}} \right]$$  \hspace{1cm} (9)

Although the Murphy-Good law has been suggested as a more accurate model for the field emission physics, it has been shown that at large fields ($F > 10^7 \text{ V/cm}$) for materials with work functions larger than $2.6 \text{ eV}$ at room temperature.
(300 K), the Fowler-Nordheim model still provides a reasonable approximation for the field emission $I-V$ characteristics [38–40].

Due to the non-uniformity of the planarization steps, we found that the edges of the chip (inset of figure 6(a)) were over-polished compared to the center of the chip and therefore, the extractor gate was thinner, which caused the emitter to be above the extractor gate. The transfer characteristics of the extractor gate with different $V_{FE}/V_{GE}$ ratios for FEAs (500 × 500) at the center of a chip are shown in figure 6(a), and the corresponding FN plots are illustrated in figure 6(b). By measuring the average of three sweeps, the FN parameters were extracted (table 1) using the slope and the intercept [41,42]. As the $V_{FE}/V_{GE}$ ratio was reduced, $I_A$ also decreased, suggesting a non-negligible effect from the focus gate. The decrease in the value of $\beta_{eff}$ could be either due to the tip burnout causing increase in the tip radius over the different sweeps performed or due to the effect of the focus gate on the tip. The lower $\beta_{GE}$ at $V_{FE}/V_{GE} = 1.1$, however, was most likely due to sharper tips burning out earlier in the electrical characterization as the sweeps were carried out in the sequence where $V_{FE}/V_{GE}$ was 1.0 to 0.7, and lastly 1.1. Using a linear fit of $\beta_{eff}$ against $V_{FE}/V_{GE}$ (figure 6(c)), we obtained values of $1.12 \times 10^5 \text{cm}^{-1}$ and $0.48 \times 10^6 \text{cm}^{-1}$ for $\beta_{GE}$ and $\beta_{F}$, respectively.

At the edges of the chip (inset of figure 6(a)), the anode current was smaller (figure 7) and the $V_{FE}/V_{GE}$ ratios had a stronger impact on the turn-on voltage and the maximum current measured. The extracted data are given in table 2 and demonstrated that by contrast, in the case where the extractor gate was thin, $\beta_{GE}$ and $\beta_{F}$ were $4.9 \times 10^5 \text{cm}^{-1}$ and $6.7 \times 10^5 \text{cm}^{-1}$, respectively. The larger value of $\beta_{F}$ was characteristic of a device having the tip above the extractor gate, which would lead to a strong influence from the focus electrode.

The transfer characteristics of the focus gate at different $V_{GE}$ bias, in the case where the tip was lower than the extractor gate, shown in figure 8(a) were very similar to the case where the focus gate functions as a second anode with typical output characteristics. In devices, where the tip was above the extractor gate, the tip electric field due to the focus gate is a significant portion of the total tip electric field, resulting in a decrease of the turn-on $V_{FE}$ when $V_{GE}$ was increased from 17 V to 25 V, as shown in figure 8(b). This increase in $I_A$ with $V_{FE}$ indicated that the focus gate could exert a field high enough for field emission from the tip due to its stronger influence compared to the extractor gate.

3.4. Focal spot size measurements

Optical images of the electron beam for the two thicknesses of extractor gate are shown in figure 9. A current of approximately $2 \, \mu\text{A}$ was recorded for the device with thicker extractor gate at $V_{GE} = 32$ V. The device with thinner gate, was biased at $V_{GE}$ of 35 V due to the drastic current changes. Since the magnification of the camera was kept the same, the scale and dimensions of the image were obtained by measuring the distance of the active area of 500 μm. The minor and major axes of a fitted ellipse were extracted and plotted against $V_{FE}/V_{GE}$ ratios, as demonstrated in figure 9.

In the case of the thick extractor gate, optical images were recorded in 1 V steps. For clarity only images at 2 V steps are shown in figure 9(a). The elongation across the device could be due to the probes as the focus electrode was at a more negative bias than the extractor, which could create an electric field between the two probes. The minor axis, however, may be a better parameter in this case to estimate the spot size. The current was stable while $V_{FE}$ was being decreased as illustrated in figure 9(b). A sharp rise in current at $V_{FE} = 5$ V, was nonetheless observed as perhaps the electrons become more focused towards the anode, and further reducing $V_{FE}$ reduced the anode current and this caused spot size to become circular. The minor axis of the fitted ellipse is plotted in figure 9(c) and showed that a minimum was achieved then $V_{FE}/V_{GE}$ was in the range of 0.3 to 0.4. Conversely, the major axis diameter (figure 9(d)) was constant within this range, although it decreased when $V_{FE}/V_{GE}$ was lower than 0.25.

With devices located at the periphery of the chip, the spot size decreased drastically and the spot became more challenging to measure when $V_{FE}$ was smaller than 20 V, owing to the reduced brightness. The data was therefore taken with voltages up to $V_{FE} = 20$ V only, as shown in figure 9(e). Significant current variations, and a strong influence of $V_{FE}$ were likewise observed as shown in figure 9(f). The diameters of the spot sizes with $V_{FE}/V_{GE}$ ratio are illustrated in figure 9(e) and (f), demonstrating a linear relationship due to larger current and larger contribution of the focus voltage to the field at the emitter. Spot sizes of approximately 200 μm, which were smaller than the FEA width of 500 μm, were measured on both the major and minor axes, implying that electrons emitted from
devices on the perimeter were not focused. Rather, there was a decrease in the effective field at the tip, which therefore, reduced the emission region on the tip.

Electron trajectories of a single emitter with double-gates were also modeled using the particle tracing module in COMSOL Multiphysics, with a 3D structure. The emission area was defined as the radius of the tip and particles (10,000) with the electron mass and electron charge. A uniform particle distribution was selected over this emission surface, in order to map the paths of edge-emitted electrons that may become stray. The initial velocity was set to 0, and the initial direction was set to be the surface normal. First, the electrostatic field was solved by a stationary study, which was used subsequently in a time-dependent study from 0 to 10 ps with 1 fs steps to map the trajectories. The simulation were performed using a parametric sweep of $V_{FE}/V_{GE}$ ratios in 0.1 steps, and with $V_{GE}$ biased at 35 V to be consistent with the experimental work. The modeled electron trajectories and estimated spot size, taken at a cut-plane of 10 μm above the focus gate, are shown in figure 10. With decreasing $V_{FE}/V_{GE}$ ratios, the electrons were focused and at a value of 0.1, the optimal focus was observed (figure 10 (a)). The beam would spread if the ratio was smaller than 0.1 as stray electrons would be directed in opposite directions of the central axis. Spot sizes were measured to be less than 2 μm in diameter for a ratio of 0.1 as illustrated in figure 10 (b), whereas this spot size was much larger for other ratios. Even though we measured optimum focusing at a $V_{FE}/V_{GE}$ ratio of 0.35 in our experiments, compared to a ratio of 0.1 determined by modeling, the spot size demonstrated a similar trends with $V_{FE}/V_{GE}$ ratios both in simulation and measurements.

3.5. Comparison with previous works

Data from previous works based on double-gated field emitter arrays including both metal and semiconductors collected were also compared as shown in table 3. It is demonstrated that this is the densest double-gated structure fabricated with a pitch of 1 μm, and consisting of narrow extractor gate aperture diameters, $d_{G}$, of 360 nm and focus gate aperture diameters, $d_{F}$, of 570 nm. In addition, the double-gated Si FEAs characterized in this work, operate at low voltage bias and have low turn-on voltage compared to previous reports. Focus ratios ($V_{FE}/V_{GE}$) varied significantly among previous reports as the distance from the focusing gate to the emitter and the geometry of the aperture have significant impact on the field required to reduce the spot size of the electron beam [34,43,44].

| Reference | Emitters | Pitch [μm] | $d_{G}$ [μm] | $d_{F}$ [μm] | $I_{max}$ [μA] | $V_{GE}$ [V] | $V_{FE}/V_{GE}$ | $V_{ON}$ [V] |
|-----------|----------|------------|-------------|-------------|---------------|-------------|----------------|-------------|
| †         | 250 000  | 1          | 0.36        | 0.57        | 2             | 32          | 0.35           | 15          |
| [14]      | 25       | 20         | 2.00        | 3.00        | 0.2           | 90          | 0.09           | 45          |
| [27]      | 100      | 10         | 0.40        | 1.20        | 3             | 60          | 0.25           | 20          |
| [32]      | 25       | 10         | 0.40        | 1.20        | 2.5           | 50          | 0.24           | 20          |
| [33]      | 10 000   | 10         | 1.00        | 8.00        | 3             | 60          | 0.00           | 37          |
| [34]      | 19       | 5          | 0.50        | 1.00        | 4             | 60          | 0.08           | 22          |
| [34]      | 37       | 5          | 0.50        | 0.75        | 8             | 60          | 0.08           | 22          |
| [35]      | 2809     | 5          | 1.10        | 3.00        | 31            | 80          | 0.00           | 40          |
| [43]      | 100      | 10         | 1.20        | 2.20        | 1             | 70          | 0.07           | 40          |
| [44]      | 3500     | 2          | 0.30        | 1.70        | 30            | 45          | 0.30           | 25          |

4. Discussion

The results we obtained herein, show that a double-gated structure can focus electrons emitted at a wide angle and the positions of the gates relative to the emitter tip are essential to achieve the optimum focus. In I-V measurements, a larger current and larger $\beta_{FE}$ were measured for devices with thicker extractor gate, which allowed the tip to form either within or below the aperture of this gate. This was validated in the field factor simulations where we demonstrated that the emitter has to be below or level with the extractor gate to be shielded from the focus electrode. Transfer characteristics obtained by varying the focus gate voltage while maintaining a constant extractor gate voltage, also confirmed that the second gate may act as the extractor gate when the emitter was closer to it. Hence, additional optimization is necessary to ensure the emitter is always below the extractor gate and further from the focus electrode, while improving the uniformity on a large scale. This could be carried out by modifying the fabrication process to enable a thicker insulator to separate the two gates. Substituting oxide for nitride as the insulator between the two gates may also simplify the tip release step and enable even higher density emitters. The oxide cap, which was used for the isotropic etch of the tip, would have to be kept during the process in order to realize this type of device. However, we found that this oxide cap could break from the emitter, during either the cleaning steps before oxidation or the dielectric matrix the fill-in process.

Despite the fact that the spot size was shown to vary as a function of the $V_{FE}/V_{GE}$ ratio in both simulation and experiment, the $V_{FE}/V_{GE}$ ratio for optimum focus was different, possibly due to several factors. The dielectric between the two gates could be charging when stray electrons are emitted, which could cause focusing at smaller $V_{E}$, hence larger $V_{FE}$. 

Also, the electrostatic repulsion between the beams from arrays of emitters were not considered in the model, but this could be non-negligible at higher currents. This is because electron beams in proximity may start interacting causing an increase in the spot size. Ideally, measuring single emitters or smaller arrays could demonstrate smaller spot sizes; yet smaller arrays require significantly larger \( V_{GE} \) to emit measurable currents, which might cause early dielectric breakdown between the two gates. A high voltage phosphor screen would also be necessary in this case to provide brighter spots at lower currents. The trade-off between brightness and focal spot remains an issue that would require further optimization for applications requiring high current such as displays and imaging. In such cases, a global focusing mechanism such as magnetic focusing could be added to operate at high currents; a low current would reduce the spot size but at the expense of a lengthy image display/acquisition. Nonetheless, the device shown here could be utilized for low current applications such as multi-beam electron lithography, low-power rf amplifiers and imaging where the acquisition time is not critical.

5. Conclusion

We demonstrated the fabrication and characterization of nanoscale high-density self-aligned double-gated Si FEAs with \( 1 \mu m \) pitch and integrated nanowire current limiter. To our knowledge, this is the densest fabricated Si FEAs incorporating self-aligned extractor and focus gates with diameters smaller than \( 1 \mu m \) and an integrated current limit. The key fabrication step was the nano-machining of the emitter tip using a combination of selective dry-etch and wet-etch to prevent the loss of the insulator separating the gates, and eventual collapse of the focus electrode. Aperture diameters of approximately 350 nm and 550 nm were measured for the extractor and the focus electrode, respectively, giving field factors larger than \( 10^6 \) \( \text{cm}^{-1} \). The double-gated Si FEAs had low turn-on voltages of less than 20 V and currents exceeding 1 \( \mu A \) above 30 V. Spot sizes obtained using a low voltage phosphor anode indicated that focusing was achieved at a \( V_{FE}/V_{GE} \) ratio of around 0.35. These double-gated Si FEAs have potential applications in compact focused electron microscopes, multi-beam lithography, flat-panel x-ray imagers, microwave tubes and rf amplifiers.

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References

[1] Spindt C A 1968 J. Appl. Phys. 39 3504–5
[2] Basu A, Swanwick M E, Fomani A A and Velasquez-Garcia L F 2015 J. Phys. D: Appl. Phys. 48 225501
[3] Cheng S, Hill F A, Heubel E V and Velasquez-Garcia L F 2014 J. Microelectromech. Syst. 24 373–83
[4] Johnson B B, Schwoebel P R, Holland C E, Resnick P J, Hertz K L and Chichister D L 2012 Nucl. Instrum. Methods Phys. Res. A 663 64–74
[5] Whaley D R, Duggal R, Armstrong C M, Bellew C L, Holland C E and Spindt C A 2008 Operation of a low-voltage high-transconductance field emitter array TWT IEEE Int. Vacuum Conf. (IEEE) 2008 https://doi.org/10.1109/ivelec.2008.4556424
[6] Spindt C A 1993 J. Vac. Sci. Technol. B 11 468
[7] Gomer R 1961 Field emission and field ionization (Cambridge: Harvard University Press)
[8] Fowler R H and Nordheim L 1928 Proc. R. Soc. A 119 173–81
[9] Hunt C E, Trujillo J T and Orvis W J 1991 IEEE Trans. Electron Devices 38 2309–13
[10] Spindt C A, Brodie L, Humphrey L and Westerberg E R 1976 J. Appl. Phys. 47 5248–63
[11] Ding M, Sha G and Akinwande A I 2002 IEEE Trans. on Electron Devices 49 2333–42
[12] Karaulac N, Rughoobur G and Akinwande A I 2020 J. Vac. Sci. Technol. B 38 023201
[13] Gomer R 1994 Surf. Sci. 299-300 129–52
[14] Itoh J, Hirano T and Kanemaru S 1996 Appl. Phys. Lett. 69 1577–8
[15] Kanemaru S, Hirano T, Tanoue H and Itoh J 1997 Appl. Surf. Sci. 111 218–23
[16] Guerrera S A and Akinwande A I 2016 Nanotechnology 27 295302
[17] Takemura H, Tomiharu Y, Futurake N, Matsuno F, Yoshiki M, Takada N, Okamoto A and Miyano S 1997 A novel vertical current limiter fabricated with a deep trench forming technology for highly reliable field emitter arrays Int. Electron Devices Meeting IEDM Technical Digest (IEEE) p 709–12
[18] Hong C Y and Akinwande A I 2005 IEEE Trans. Electron Devices 52 2323–8
[19] Guerrera S A, Velasquez-Garcia L F and Akinwande A I 2012 IEEE Trans. Electron Devices 59 2524–30
[20] Temple D, Palmer W D, Yadon L N, Mancusi J E, Velenga D and McGuire G E 1998 J. Vac. Sci. Technol. A 16 1878–85
[21] Fomani A A, Guerrera S A, Velasquez-Garcia L F and Akinwande A I 2014 IEEE Trans. Electron Devices 61 2538–46
[22] Jensen K L, Zaidman E G, Kodis M A, Goplen B and Smithie D N 1996 J. Vac. Sci. Technol. B 14 1942
[23] Dvorson L, Ding M and Akinwande A I 2001 IEEE Trans. Electron Devices 48 134–43
[24] Pfug D G, Schattenburg M, Smith H I and Akinwande A I 2001 Field emitter arrays for low voltage applications with sub 100 nm apertures and 200 nm period Int. Electron Devices Meeting Technical Digest (Cat. No.01CH37224) (IEEE) 8.5.1–8.5.4
[25] Rughoobur G and Akinwande A I 2018 Arrays of Si Field Emitter Individually Regulated by Si Nanowires High Breakdown Voltages and Enhanced Performance 31st Int. Vacuum Conf. (IVNC) (https://doi.org/10.1109/ ivnc.2018.852086)
[26] Chen L Y and Akinwande A I 2006 J. Vac. Sci. Technol. B 1878 1878–85
[27] Chen L Y and Akinwande A I 2007 IEEE Trans. Electron Devices 54 601–8
[28] Dvorson L and Akinwande A 1999 SID Symp. Digest of Technical Papers vol 30 926
[29] Dvorson L, Ding M and Akinwande A I 2001 IEEE Trans. Electron Devices 48 144–8
[30] Kesling W D and Hunt C E 1995 IEEE Trans. Electron Devices 42 340–7
[31] Li C et al 2013 Adv. Funct. Mater. 24 1218–27
[32] Dvorson L, Kymissis I and Akinwande A I 2003 J. Vac. Sci. Technol. B 21 486
[33] Tsujino S, Kanungo P D, Monshipouri M, Lee C and Miller R J D 2016 Nat. Commun. 7 13976
[34] Soda T, Nagao M, Yasumuro C, Kanemaru S, Sakai T, Saito N, Neo Y, Aoki T and Mimura H 2008 Japan. J. Appl. Phys. 47 5252–5
[35] Lee J H 1998 J. Vac. Sci. Technol. A 16 811
[36] Itoh J 1995 J. Vac. Sci. Technol. B 13 1968
[37] Schindelin J et al 2012 Nat. Methods 9 676–82
[38] Murphy E L and Good R H 1956 Phys. Rev. 102 1464–73
[39] Forbes R G 2019 R. Soc. Open Sci. 6 190912
[40] Dionne M, Coulombe S and Meunier J L 2008 J. Phys. D: Appl. Phys. 41 245304
[41] Persaud A 2013 J. Appl. Phys. 114 154301
[42] Smirnov I U, Kolosko A G, Filippov S V, Yudkina N A and Popov E O 2016 Journal of Physics: Conf. Series 741 012031
[43] Toma Y, Kanemaru S and Itoh J 1996 J. Vac. Sci. Technol. B 14 1902
[44] Py C, Gao M, Das S R, Grant P, Marshall P and LeBrun L 2000 J. Vac. Sci. Technol. A 18 626–9