Low-Cost Floating-Point Processing in ReRAM for Scientific Computing

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ABSTRACT

Resistive random access memory (ReRAM) is a promising technology that can perform low-cost and in-situ matrix-vector multiplication (MVM) in the analog domain. ReRAM-based accelerators are successful in deep learning thanks to the low precision fixed-point or integer formats. High-precision floating point processing is required in scientific computing. Performing floating-point computation in ReRAM is challenging because it consumes much higher hardware cost and execution time than fixed-point due to the larger value range.

In this paper, we propose ReFLOAT, a data format and an accelerator architecture, for low-cost and high-performance floating-point processing in ReRAM for scientific computing. ReFLOAT reduces bit number for floating-point representation and processing to achieve a smaller number of ReRAM crossbars and processing cycles for floating-point matrix-vector multiplication. In the ReFLOAT data format, for scalars of a matrix block, an exponent offset is derived from an optimized base, and then an exponent offset is reserved for each scalar and fraction bit numbers are reduced. The exponent base optimization is enabled by taking advantage of the existence of value locality in real-world matrices. After defining the ReFLOAT data format, we develop the conversion scheme from default double-precision floating-point format to ReFLOAT format, the computation procedure, and the low-cost high-performance floating-point processing architecture in ReRAM. With ReFLOAT, we find that for all 12 matrices only 3 bits for matrix exponent, matrix fraction and vector exponent, and 8 or 16 bits for vector fraction are sufficient to ensure convergence on solvers CG and BiCGSTAB. It translates to an average speedup of 20.10× / 24.59× on CG / BiCGSTAB compared with a GPU baseline and an average speedup of 18.86× / 54.00× on CG / BiCGSTAB compared with a state-of-the-art ReRAM-based accelerator for scientific computing.

1. INTRODUCTION

With the impending end of Moore’s Law [82] and Denard scaling [32], general-purpose computing platforms such as CPUs and GPUs will no longer benefit from integrating more and more cores [25]. Thus, the domain-specific architectures are critical for improving performance and energy efficiency of various applications. Rather than relying on conventional CMOS technology, the emerging non-volatile memory technology such as resistive random access memory (ReRAM) is considered as a promising candidate for implementing processing-in-memory (PIM) accelerators [5, 10, 15, 27, 41, 43, 48, 74, 78, 79, 94] that can provide orders of magnitude improvement of computing efficiency. Specifically, ReRAM can both store data and perform in-situ matrix-vector multiplication (MVM) operations in analog domain. Most current ReRAM-based accelerators focus on machine learning applications, which can accept a low precision, e.g., less than 16-bit fixed-point, thanks to the quantization in deep learning [19, 36, 38, 42, 57].

Scientific computing is a collection of tools, techniques and theories required to solve science and engineering problems represented in mathematical systems [34], where the underlying variables in scientific computing are continuous in nature, such as time, temperature, distance, density, etc. One of the most important aspects of scientific computing is modeling a complex system with partial differential equations (PDEs) to understand the natural phenomena in science [39, 46], or the design and decision-making of engineered systems [13, 68]. Most problems in continuous mathematics modeled by PDEs cannot be solved directly. In practice, the PDEs are converted to a linear system $Ax = b$, and then solved through an iterative solver that ultimately converges to a numerical solution [7, 73]. To obtain an acceptable answer where the residual is less than a desired threshold, intensive computing power [26, 77] is required to perform the floating-point sparse matrix-vector multiplication (SpMV)—the key computation kernel.

Due to the prevalent floating point operations in scientific computing, leveraging ReRAM to achieve parallel in-situ floating-point SpMV is desirable. When using ReRAM crossbar to perform SpMV, the matrix is partitioned into blocks, of which each matrix element is encoded as the ReRAM cell conductance, the input vector is converted to wordline voltage through Digital-to-Analog Converters (DACs). Thus, the bitline will output the results of the dot-product between the current input vector bits and matrix elements mapped in the same crossbar column. Each bit in the output is connected to a sample and hold (S/H) unit. After all input bits are processed, the results of the SpMV are available at the output.
of S/H unit, which is converted to multi-bit digital values by Analog-to-Digital Converters (ADCs). Due to the technology constraints, the number of bits can be stored in each memory cell is limited. We make a very conservative assumption that each cell represents one bit. For multi-bit fixed-point values, multiple cells are concatenated, leading to increased hardware cost. In general, the number of cycles to perform an SpMV is determined by the number of bits in the input vector and the matrix, while the number of crossbars is determined by the number of bits representing matrix elements.

We examine mapping the floating-point SpMV by leveraging the same principle used in MVM. Take 64-bit double-precision number as an example, each floating-point number consists of a 1-bit sign ($s$), an 11-bit exponent ($e$), and a 52-bit fraction ($f$). The value is interpreted as $(-1)^s \times (1.b_{51}b_{50}...b_{0}) \times 2^{e-1023}$, yielding a dynamic data range from $±2.2 \times 10^{-308}$ to $±1.8 \times 10^{308}$. The number of crossbars for a matrix $M$ increases exponentially with the bits number of the exponent ($e_M$) and linearly with the bits number of the fraction ($f_M$). Directly representing floating-point values with huge number of crossbars incurs prohibitive cost.

To reduce the overhead, Feinberg et al. [27] proposes to truncate the higher bits in exponents, e.g., using the low 6 bits or module 64 of the exponent to represent each original value, while keeping the number of fraction bits unchanged (52 bits). This ad-hoc solution does not ensure the convergence of iterative solves (see Table 1 and Section 6.2 for details). In addition, as shown in Figure 9, it may unnecessarily incur the hardware and execution time cost for the full precision, even when we assume ESCMA [27] functions correctly.

In this paper, we propose ReFLOAT. a principled approach based on a flexible and fine-grained floating-point number representation. The key insight of our solution is the exponent value locality among the elements in a matrix block, which is the granularity of computation in ReRAM. If we consider the whole matrix, the exponent values can span a wide range, e.g., up to 11 for a matrix, but the range within a block is smaller, e.g., at most 7 for the same matrix. It naturally motivates the idea of choosing an exponent base $e_b$ for all exponents in a block, and storing only the offsets from $e_b$. For a matrix block, although the absolute exponent values may be large, the variation is not. For most blocks, by choosing a proper $e_b$, the offset values are much smaller than the absolute exponent values, thereby reducing the number of bits required.

Instead of simply using the offset as a lossless compression method, ReFLOAT aggressively uses less number of bits for exponent offsets ($e$) than the required number of bits to represent them. The error is bounded by the existence of value locality in real-world matrices. Moreover, the error is refined due to the nature of iterative solver. Starting from an all-zero vector, an increasingly accurate solution is produced in each iteration. The iterative solver stops when a defined convergence criteria is satisfied. Because the vector from each iteration is not accurate anyway, the computation has certain resilience to the inaccuracy due to floating-point data representation. It is why [27] can work in certain cases. In ReFLOAT, when an offset is larger (smaller) than the largest (smallest) offset represented by $e$ bits, the largest (smallest) value of $e$ bits is used for the offset. With $e$-bit exponent offset, the range of exponent values is $[e_b - 2^{(e-1)} + 1, e_b + 2^{(e-1)} - 1]$. Selecting $e_b$ becomes an optimization problem that minimizes the difference between the exponents of the original matrix block and the exponents with $e_b$ and $e$-bit offsets.

To facilitate the proposed ideas in a concrete architecture, we define the ReFLOAT format as ReFLOAT($b, e, f$)($e_b, f_b$), where $b$ denotes the matrix block size—the length and width of a square matrix block is $2^b$. $e$ and $f$ respectively denote the exponent and fraction bit lengths for the matrix, and ($e_b, f_b$) denotes the exponent and fraction bit lengths for the vector. With $e_b$ for each block, all matrix elements in the block can be represented. We develop the conversion scheme from default double-precision floating-point format to ReFLOAT format and the computation procedure based on it. Based on ReFLOAT format, we design the low-cost high-performance floating-point processing architecture in ReRAM. Our results show that for 12 matrices evaluated on iterative solvers (CG and BiCGSTAB), only 3 bits for exponent and 8 or 16 bits for fraction are sufficient to ensure convergence. In comparison, [27] uses 6 bits for exponent and 51 bits for fraction without guaranteeing convergence. It translates to an average speedup of $20.10 \times / 24.59 \times$ on CG / BiCGSTAB compared with a GPU baseline and an average speedup of $18.86 \times / 54.00 \times$ on CG / BiCGSTAB compared with a state-of-the-art ReRAM-based accelerator [27] for scientific computing.

2. BACKGROUND

2.1 In-situ MVM Acceleration in ReRAM

ReRAM [3, 90] has recently demonstrated tremendous potential to efficiently accelerate the computing kernel, i.e., MVM, in machine learning. Conceptually, each element in a matrix $M$ is mapped to the conductance state of a ReRAM cell, while the input vector $x$ is encoded as voltage levels that are applied on the wordlines of the ReRAM crossbar. In this way, the current accumulation on bitlines is proportional to the dot-product of the stored conductance and voltages on the wordlines, representing the result $y = M \times x$. Such in-situ computation significantly reduces the expensive memory access in MVM processing engines [41], and most importantly, provides massive opportunities to exploit the inherent parallelism in an $N \times N$ ReRAM crossbar.

ReRAM-based MVM processing engines are fixed-point hardware in nature due to the fact that the matrix and the vector are respectively represented in discrete conductance states and voltage levels [90]. If ReRAM is used to support floating-point MVM operation, a large number of crossbars will be provisioned for fraction alignment, resulting in very high hardware cost. We will illustrate the problem in Section 3 to motivate ReFLOAT design. Nevertheless, the fixed-point precision requirement is acceptable for machine learning applications thanks to the low-precision and quantized neural network algorithms [20, 36, 42, 45, 52, 96]. Many fixed-point based accelerators [5, 10, 15, 33, 48, 74, 78, 94] are built with the ReRAM MVM processing engine and achieve reasonably good classification accuracy.

2.2 Iterative Scientific Computing

Scientific computing is an interdisciplinary science that solves computational problems in a wide range of disciplines
including physics, mathematics, chemistry, biology, engineering, and other natural sciences [6, 30, 35]. Those complex computing problems are normally modeled by systems of large-scale PDEs. Since it is almost impossible to directly obtain the analytical solution of those PDEs, a common practice is to discretize continuous PDEs into a linear model $Ax = b$ [7, 73] to be solved by numerical methods. The numerical solution of this linear system is usually obtained by an iterative solver [23, 65, 89].

Code 1 illustrates a typical computing process in iterative methods. The vector $x$ to be solved is typically initialized to an all-zero vector $x_0$, followed by three steps in the main body: (1) the residual (error) of the current solution vector is calculated as $r = b - Ax$; (2) to improve the performance of the estimated solution, a correction vector $p$ is computed based on the current residual $r$; and (3) the current solution vector is improved by adding the correction vector as $x = x + p$, aiming to reduce the possible residuals produced in the next calculation iteration. The iterative solver stops when a defined convergence criteria is satisfied. Two widely used convergence criteria are (1) that the iteration index is less than a preset threshold $\tau$, or (2) that the L-2 norm of the residual $(\text{res} = |b - Ax|^2)$ is less than a preset threshold $\tau$. Notably, all the values involved in Figure 1 are implemented as double-precision floating-point numbers to meet the high-precision requirement of mainstream scientific applications.

The various iterative methods follow the above computational steps and differ only in the calculation of the correction vectors. Among all candidate solutions, Krylov subspace approach is the standard method nowadays. In this paper, we focus on two representative Krylov subspace solvers – Conjugate Gradient (CG) [40] and Stabilized BiConjugate Gradient (BiCGSTAB) [81]. The computational kernels of these two methods are large-scale sparse floating-point matrix-vector multiplication $y = Ax$, which requires the support of floating-point computation in ReRAM. This imposes significant challenges to the underlying computing hardware.

2.3 Fixed-Point and Floating-Point Representations

We use 8-bit signed integer and the IEEE 754-2008 standard [17] 64-bit double-precision floating-point number as examples to compare the difference between fixed-point and floating-point numbers. They refer to the format used to store and manipulate the digital representation of data. As shown in Fig. 2 (a), fixed-point numbers represent integers—positive and negative whole numbers—via a sign bit followed by multiple (e.g., $i$-bit) value bits, yielding a value range of $-2^i$ to $2^i - 1$. IEEE 754 double-precision floating-point numbers shown in Figure 2 (b) are designed to represent and manipulate rational numbers, where a number is represented with one sign bit ($s$), 11-bit exponent ($e$), and 52-bit fraction ($b_{51} b_{50} \ldots b_0$). The value of a double-precision floating-point number is interpreted as $(-1)^s \times (1.b_{51} b_{50} \ldots b_0) \times 2^{e-1023}$, yielding a dynamic data range from $\pm 2.2 \times 10^{308}$ to $\pm 1.8 \times 10^{308}$.

Many efficient floating point formats as shown in Figure 2 have been proposed because the default format incurs high cost for conventional digital system. However, the applications such as deep learning do not require a very wide data range. The representative examples include IEEE 32-bit single-precision floating point (FP32), Google bfloat16 [85], Nvidia TensorFloat32 [51], Microsoft ms-fp9 1 [16], and block floating point (BFP) [11, 53]. Accordingly, the specialized hardware designs or/and systems are also proposed to amplify the benefits of the efficient data formats. For example, Google bfloat is associated with TPU [1, 2, 50], Nvidia TensorFloat is associated with tensor core GPUs, Microsoft floating-point formats are associated with Project Brainwave [16], and BFP are favorable for signal processing on DSPs [24] and FPGAs [18].

However, the floating point representations favored by deep learning may not benefit scientific computing. For deep learning, weights can be retrained to a narrowed/shrunk space, even without floating point [19, 42, 59, 72, 97]. In scientific computing, data cannot be retrained and the shrunk formats cannot capture all values. For example, $1.0 \times 10^{-40}$ falls out of range for FP32, bfloat16, TensorFloat32 and ms-fp9 because of narrow range representation. Two values $1.0 \times 10^{-40}$ and $1.0 \times 10^{-30}$ can not be captured by a BFP block because of non-dynamic range representation within a block. The narrow or non-dynamic range may lead to non-convergence in scientific computing.

In general, double-precision floating-point is a norm for high-precision scientific computations because it can support a wide range of data values with high precision, but the processing demands low hardware cost and high performance.

3. MOTIVATION AND REFLOAT IDEAS

The layout is inferred from the description in [16]. No public specifications on ms-fp are available.
by utilizing ReRAM-based MVM engines with single-bit precision. Before computation, the decimal integers in both the matrix and the vector are converted to binary bits, where we set the precision for the matrix and input vector to 4-bit. The matrix is bit-sliced into four one-bit matrices and then mapped to four crossbars, i.e., M-b3, M-b2, M-b1 and M-b0. The input vector is bit-sliced into four one-bit vectors, i.e., V-b3, V-b2, V-b1 and V-b0. The multiplication is performed in pipeline. Each crossbar has a zero initial vector S0. In the first cycle C1, the most significant bit (MSB) vector V-b3 is applied on wordlines of the four crossbars, and the multiplication results of V-b3 with M-b3, M-b2, M-b1 and M-b0 are obtained in parallel, denoted by O0. In cycle C2, S0 is right-shifted by 1 bit to get S1, and V-b2 is input to the crossbars to get the multiplication results O1. Similar operations are performed in C3 and C4. After C4, we get S4, the multiplication results of the input vector with four bit-slices of the matrix. In the following three cycles C5 to C7, we shift and add S4 from the four crossbars to get the final multiplication result. For the fixed-point multiplication of an $N_M$-bit matrix with an $N_v$-bit vector, the processing cycle count is $C_{int} = N_v + (N_M - 1)$.

In this section, we explain in detail the hardware cost, i.e., the crossbar number $C$, and the performance, i.e., the cycle number $T$, of ReRAM-based floating-point MVM. Note that $C$ correlates with the ability to execute floating-point MVMs in parallel with a given number of on-chip ReRAMs [27, 74, 79]: the smaller $C$, the more parallelism can be explored. A smaller $T$ directly reflects a higher performance of one ReRAM-based MVM on a matrix block. A smaller $T$ and a smaller $C$ reflects a higher performance of one SpMV on a whole matrix.

**Crossbar number.** Suppose we compute the multiplication of a matrix block $M$ and a vector segment $v$. In the matrix block $M$, the number of fraction bits is $f_M$ and the number of exponent bits is $e_M$. In the vector segment $v$, the number of fraction bits is $f_v$ and the number of exponent bits is $e_v$. To map the matrix fraction to ReRAM crossbars, we need $(f_M + 1)$ ReRAM crossbars because the fraction is normalized to a value with a leading 1. For example, $(52+1)$ crossbars are needed to represent the 52-bit fraction in double floating-point precision in [27]. To map the matrix exponent to ReRAM crossbars, we need $2^e_M$ ReRAM crossbars for $e_M$-bit exponent states, which is called padding in [27] where 64-bit paddings are needed for an $e_M = 6$. Thus, $C$ is calculated as

$$C = 4 \times (2^{e_M} + f_M + 1),$$

where the leading multiplier 4 is contributed from sign bits of the matrix block and the vector segment.

**Cycle number.** We conservatively suppose the precision of digital-analog converters is 1-bit as that in [27, 74]. The number of value states in a vector segment is $(2^{e_v} + f_v + 1)$. For each input state, we need $(2^{e_M} + f_M + 1)$ to perform shift-and-add to reduce the partial results from the ReRAM crossbars. To achieve higher computation efficiency, a pipelined input and reduce scheme [74] can be used. Thus, $T$ is calculated as

$$T = (2^{e_v} + f_v + 1) + (2^{e_M} + f_M + 1) - 1.$$  

**High hardware cost and low performance in default double precision.** In the default double-precision floating-point (FP64), 8404 crossbars and 4201 cycles are consumed for one MVM in ReRAM. To understand how bit number affects the hardware cost and performance, we explore the effect of exponent and fraction bit number of matrix and vector on the cycle number on the effect of exponent and fraction bit number of matrix on the crossbar number, illustrated in Figure 4. The crossbar number increases exponentially with $e_M$ while linearly with $f_M$. The cycle number increases exponentially with both $e_v$ and $e_M$, while the latency increases linearly with $f_v$ and $f_M$.

### 3.3 Truncation and Non-convergence

Through the above analysis, it is possible to reduce number of digits by reducing the number of bits of the exponent and fraction, thereby reducing hardware costs, i.e., fewer cycles and crossbars. But the accuracy of the solvers may be significantly degraded, or even cause non-convergence.

The design of the state-of-the-art ReRAM-based accelerator [27] for floating-point SpMV is driven exactly by the conclusion of our analysis—reducing the number of bits for exponent. However, this solution adopts an ad-hoc approach.
3.4 Value Locality

Although reducing the number of exponent bits has a significant impact on decreasing hardware cost and computation cycles, sufficient accuracy of exponents is still required to ensure convergence. We leverage an intuitive observation of matrix element values—exponent value locality—to reduce the number of exponents bits while keeping enough accuracy.

We define the locality as the maximum number of required bits to cover the exponent in all matrix blocks of a large matrix. We illustrate the locality of matrices from SuiteSparse [22] in Figure 4(d). As discussed before, ReRAM performs MVM at the granularity of matrix block, whose size is determined by the size of ReRAM crossbar, e.g., 128 × 128. While exponent values of the whole matrix can span a wide range, e.g., up to 11 for a matrix, but the range is smaller within a block, e.g., at most 7 for the same matrix. The default locality, i.e., 11, is redundant. Naturally, it motivates the idea of using an exponent base \( e_b \) for all exponents in a block, and storing only the offsets from \( e_b \). For most blocks, by choosing a proper \( e_b \), the offset values are much smaller than the absolute exponent values, thereby reducing the number of bits required.

It is important to note we do not simply use the offset as a lossless compression method. While exponent value locality exists for most of the blocks, it is possible that for a small number of blocks the exponent values are scattered across a wide range. If we include enough number of bits for all offsets, the benefits for the majority of blocks will be diminished. Moreover, it is not necessary due to the nature of iterative solvers. As discussed earlier, the vector from each iteration is lost, so the offsets are naturally zeros. Therefore, it is in fact overkill to attempt to represent exponent values precisely.

We can naturally tune the accuracy by the number of bits \( e \) allocated for the offsets which is less than the number of exponent bits necessary to represent the offsets precisely. When an offset is larger (smaller) than the largest (smallest) offset representable by \( e \) bits, the largest (smallest) value of \( e \) bits is used accordingly. With \( e \)-bit exponent offset, the range of exponent values is \( [e_b - 2^{(e-1)} + 1, e_b + 2^{(e-1)} - 1] \). Intuitively, given \( e \) and \( e_b \), this system can precisely represent the exponent values that fall into a “window” around \( e_b \), while the

| exp | 11 | 11 | 11 | 11 | 11 | 11 |
|-----|----|----|----|----|----|----|
| frac | 00 | 00 | 00 | 00 | 00 | 00 |
| #ite | 50 | 50 | 50 | 50 | 50 | 50 |
| exp | 00 | 00 | 00 | 00 | 00 | 00 |
| frac | 00 | 00 | 00 | 00 | 00 | 00 |
| #ite | 50 | 50 | 50 | 50 | 50 | NC |

Table 1: The iteration numbers for convergence under various exp(onent) and fra(ction) bit configurations for matrix crystm03. NC indicates non-convergence.

that simply truncates a number of high order bits in exponent. Specifically, with the lower 6 bits of exponent, it uses module 64 of the exponent to represent each original value. Unfortunately, bit truncation may lead to significantly slower convergence and, more importantly, non-convergence. In Table 1, we show the number of iterations for convergence under various exponent and fraction bit configurations. In default double-precision, it takes 80 iterations to converge. If we fix the exponent bits and truncate fraction bits, a 21-bit fraction takes 27 additional iterations and a fraction less than 21 bits leads to non-convergence. If we fix the fraction bits and truncate exponent bits like [27], 7-bit exponent increases the iteration number from 80 to 20620, and an exponent less than 7 bits leads to non-convergence. Thus, the solution proposed in [27] may break the correctness of the iterative solver. In contrast, the number of bits in fraction has less impact on the number of iterations to converge. For example, Table 1 shows that drastically reducing fraction bits from 52 to 30 only increases the number of iterations by 2×. However, [27] simply kept the number of bits in fraction unchanged, and lost the opportunity to reduce hardware cost and improve performance. To find a better solution to the problem, we are convinced a more principled approach needs to be developed.

![Figure 4](image-url)

- (a) The cycle number of various exponent bit number for vector segment and matrix block,
- (b) the cycle number of various fraction bit number for vector segment and matrix block,
- (c) the crossbar number of various fraction and fraction bit number for matrix block,
- (d) matrix exponent bit number of double-precision floating point (FP64), the locality in 12 matrices, and ReFloat.

Table 2: List of symbols and descriptions.

| Symbol | Description |
|--------|-------------|
| A      | A sparse matrix. |
| b      | The bias vector for a linear system. |
| x      | The solution vector for a linear system. |
| r      | The residual vector for a linear system. |
| a      | A scalar of A. |
| (a)    | The exponent of \( a \). |
| (a)j   | The fraction of \( a \). |
| A      | A block of the sparse matrix. |
| (i)j   | The index for the block A, |
| (iii)jj| The index for the scalar \( a \) in the matrix A, |
| e      | The base for exponents of elements in a block. |
| f      | The number of exponent bits for a vector segment. |
| e_b    | The number of exponent bits for a vector segment. |
| f_b    | The number of fraction bits for a vector segment. |

Symbol Description

\( 2^e \) The size of a square block.
\( e \) The number of exponent bits for a matrix block.
\( f \) The number of fraction bits for a matrix block.
\( A \) A sparse matrix.
\( b \) The bias vector for a linear system.
\( x \) The solution vector for a linear system.
\( r \) The residual vector for a linear system.
\( a \) A scalar of A.
\( (a) \) The exponent of \( a \). \( (a)_j \) The fraction of \( a \).
\( A \) A block of the sparse matrix.
\( (i)j \) The index for the block \( A, \) \( (i)j \) The index for the scalar \( a \) in the matrix A.
\( e_b \) The base for exponents of elements in a block.
\( f_b \) The number of fraction bits for a vector segment.

ReFloat(b,e,f) \( \{e, f_b\} \) ReFloat format notation.
“size of the window” is determined by $2^{(e-1)}$. Then, selecting $e_b$ becomes an optimization problem that minimizes the difference between the exponents of the original matrix block and the exponents with $e_b$ and $e$-bit offsets. Thus, a wide data range but a low hardware cost are achieved simultaneously.

Based on the proposed ideas, we define ReFLOAT, a new floating-point data format, and develop the corresponding accelerator architecture, for low-cost and high-performance floating-point processing in ReRAM for scientific computing. For ReFLOAT, we leverage the value and index similarity in real-word data to compress them into lower bit representation. We present the conversion from default format to ReFLOAT format, and the computation in ReFLOAT format in Section 4, and present a ReRAM accelerator for ReFLOAT format in Section 5.

4. REFLOAT DATA FORMAT

4.1 ReFloat Format

The ReFLOAT format is defined as ReFLOAT $(b, e, f)(e_r, f_r)$, where $b$ determines the matrix block size $2^b$ (the length and width of a square matrix block), $e$ and $f$ respectively denote the exponent and fraction bit lengths for the matrix, and $(e_r, f_r)$ denotes the bit lengths for the vector. The symbols and corresponding descriptions of ReFLOAT are listed in Table 2.

Fig. 5 intuitively illustrates the idea of ReFLOAT. In Figure 5 (a), each scalar is in a 64-bit floating-point format. It requires a 32-bit integer for row index and a 32-bit integer for column index to locate each element in the matrix block. Therefore, we need $8 \times (32 + 32 + 64) = 1024$ bits for storing the eight scalars. With ReFLOAT, assuming we use ReFLOAT $(2, 2, 3)$ format as depicted in Figure 5 (b), we see that: (1) each scalar in the block can be indexed by two 2-bit integers; (2) the element value is represented by a $1 + 2 + 3 = 6$-bit floating point number $^2$; (3) the block is indexed by two 30-bit integers and (4) a 11-bit exponent base $e_b$ is also recorded. Therefore, we only use $8 \times (2 + 2 + 6) + 2 \times 30 + 11 = 151$ bits to store the entire matrix block, which reduces the memory requirement by approximately $10 \times (151 \text{ vs. } 1024)$. This reduction in bit representation is also beneficial for reducing the number of ReRAM crossbars for computation in hardware implementation. Specifically, the full precision format consumes 118 crossbars as illustrated in [27], while only 16 crossbars are needed in our design with ReFLOAT $(2, 2, 3)$ format. Thus, $^2$The elements inside a ReFLOAT block are floating-point, while the elements inside a BFP block are fixed-point.

4.2 Conversion to ReFloat Format

In order to convert the original matrix to a ReFloat $(b, e, f)$ format, three hyperparameters need to be determined in advance. The $b$ defines how the indices of input data are converted, and is determined by the physical size of ReRAM crossbars, i.e., a crossbar with $2^b$ wordlines and $2^b$ bitlines. As demonstrated in Figure 6 (a), the leading 30 bits—$b_{31}$ to $b_2$ of the index $(iii, jjj)$ for a scalar in the matrix $A$—are copied to the same bits in the index $(i, j)$ for the block $A_c$. For each scalar in the block $A_c$, the index $(ii, jj)$ for that scalar inside the block $A_c$ are copied from the last two bits of the index $(iii, jjj)$. The block index $(ii, jj)$ are shared by the scalars in the same block, and each scalar uses less bits for index inside that block. Thus, we also save memory space for indices.

The hyperparameters $e$ and $f$ determine the accuracy of floating-point values. A floating-point number consists of three parts: (1) the sign bit; (2) the exponent bits; and (3) the fraction bits. When converted to ReFLOAT, the sign bit remains unchanged. For the fraction, we only keep the leading $f$ bits from the original fraction bits and remove the rest bits in the fraction, as shown in Figure 6 (b). For the exponent bits, we need to first determine the base value $e_b$ for the exponent. As $e$ means the number of bits for the “swing” range, we need to find an optimal base value $e_b$ to fully utilize the $e$ bits. We formalize the problem as an optimization for find the $e$ to minimize a loss target $L$, defined as

$$L = \sum_{a \in A_c} \left( \log_2 \left( \frac{a}{\langle a \rangle_{eq} \times 2^e} \right) \right)^2 = \sum_{a \in A_c} ((a)_e - e_b)^2. \quad (4)$$

Let $\frac{\partial L}{\partial e_b} = 0$, we can get

$$e_b = \left[ \frac{1}{|A_c|} \sum_{a \in A_c} (a)_e \right]. \quad (5)$$

Thus, in the conversion, we use the original exponent to minus the optimal $e_b$ to get an $e$-bit signed integer. The $e$-bit signed integer is the exponent in ReFLOAT.

We use an example to intuitively illustrate the format conversion. The original floating-point values in Eq. (6) are converted to ReFloat $(x, 2, 2)$ format in Eq. (7),

$$\begin{bmatrix} (-1) \times 1.1111 \times 2^7 & 1.0101 \times 2^5 \\ (-1) \times 1.0000 \times 2^8 & 1.0001 \times 2^9 \end{bmatrix} = \begin{bmatrix} -248.0 & 336.0 \\ -512.0 & 136.0 \end{bmatrix}. \quad (6)$$

Figure 5: Comparison of a matrix block (a) in original full precision format and (b) in ReFLOAT format.

Figure 6: The conversion of index and value in floating-point format to ReFLOAT format.
where $e_y = 8$. Here, we see that $\text{REFLOAT}$ incurs conversion loss for the conversion of floating-point values from the original. However, for scientific computing, the errors in the iterative solver are gradually corrected. Thus, the errors introduced by the conversion will also be corrected in the iteration. Most importantly, with $\text{REFLOAT}$, we can achieve higher performance with low computation cost thanks to $\text{REFLOAT}$ format. We will show the performance and convergence of the iterative solver in $\text{REFLOAT}$ format in Section 6.

4.3 Computation in $\text{ReFloat}$ Format

The matrix $A$ is partitioned into blocks. To compute the matrix-vector multiplication $y = Ax$, the input vector $x$ and the output vector $y$ are partitioned correspondingly into vector segments $x_i$ and $y_i$. The size of the vector segments is $(2^b \times 1)$.

For the $p$-th output vector segment $y_i(p)$, the computation in the default full precision will be

$$y_i(p) = \sum A_i(i, p)x_i(i),$$

(8)

where $A_i(i, p)$ is the matrix block indexed by $(i, p)$ and $x_i(i)$ is the input vector segment indexed by $i$. The matrix blocks at the $p$-th block column are multiplied with the input vector segments for partial sums and then they are accumulated. In the computation for each matrix block, because the original matrix block $A_i(i, p)$ is converted to

$$A_i(i, p) = 2^{g_b(i, p)}\tilde{A}_i(i, p),$$

(9)

and the original vector segment $x_i(i)$ is converted to

$$x_i(i) = 2^{e_b(i)}\tilde{x}_i(i),$$

(10)

thus, the multiplication for the matrix block $A_i(i, p)$ and the vector segment $x_i(i)$ is computed as

$$A_i(i, p)x_i(i) = 2^{g_b(i, p)+e_b(i)}\tilde{A}_i(i, p)\tilde{x}_i(i).$$

(11)

The matrix-vector multiplication for the $p$-th output vector segment in the default format Eq. (8) is then computed as

$$y_i(p) = \sum_t 2^{g_b(i, p)+e_b(i)}\tilde{A}_i(i, p)\tilde{x}_i(i).$$

(12)

Here we see that, with $\text{REFLOAT}$ format, the block matrix multiplication in the default format is preserved. The original high-cost multiplication in full precision $A_i x_i$ is replaced by a low-cost multiplication $\tilde{A}_i \tilde{x}_i$.

5. $\text{REFLOAT}$ Accelerator Architecture

5.1 Accelerator Overview

Figure 7(a) shows the overall architecture of the proposed accelerator for floating-point scientific computing in ReRAM with $\text{REFLOAT}$. The accelerator is organized into multiple banks. Within each bank, ReRAM crossbars are deployed for processing matrix blocks of floating-point MVM. The Input Vector (IV) and Output Vector (OV) buffers are used for buffering the input and output vectors and matrix blocks. The Multiply-and-Accumulate (MAC) units are used to update the vectors. The scheduler is responsible for the coordination of the processing.

5.2 Processing Engine

The most important component in the accelerator is the processing engine for floating-point SpMV in $\text{REFLOAT}$ format. The processing engine consists of a number of ReRAM crossbars and several peripheral functional units. The architecture of the processing engine is shown in Figure 7(b), assuming we are performing the floating-point SpMV on a matrix block with the format $\text{REFLOAT}(b, e, f)$.

The inputs to the processing engine are: (1) a matrix block in $\text{REFLOAT}(b, e, f)$ format; (2) an input vector segment in floating-point with $e_v$ exponent bits and $f_v$ fraction bits and the vector length is $2^b$; and (3) the exponent base bits $e_b$ for each matrix block. The output of a processing engine is a vector segment for SpMV on the matrix block, which is a double-precision floating-point number.

Before the computation, the matrix block is mapped to the ReRAM crossbars as detailed in Figure 7(c). The fraction part of the matrix block in $\text{REFLOAT}(b, e, f)$ represents a number of $1.b_{f-1}...b_0$, then we have $(f+1)$ bits for mapping. The $e$-bit exponent of the matrix block contributes to $2^e$ padding bits for alignment, then we have another $2^e$ bits for mapping. Thus, we map the total $(2^e + f + 1)$ bits to $(2^e + f + 1)$ ReRAM crossbars, where the $i$-th bits of the matrix block is mapped to the $i$-th crossbar $3$. For the input vector segments with $e_v$ exponent bits and $f_v$ exponent bits, a total number of $(2^e + f_v + 1)$ bits $\|A\|$ are applied to the driver.

During processing, a cluster of crossbars are deployed to perform the fixed-point MVM for the fraction part of the input vector segment with the fraction part of the matrix block using the shift-and-add method, as the example in Figure 3. The input bits are applied to the crossbars by the driver and the output from the crossbar is buffed by a Sample/Hold (S/H) unit and then converted to digital by a shared Analog/Digital Converter (ADC). For each input bit to the driver (we assume an 1-bit DAC), as the crossbar size is $2^b$, the ADC conversion precision is $f_v = b$ bits. Then we need to shift-and-add the results $\|A\|$ from all $(2^e + f + 1)$ crossbars to get the results $\|A\|$ for the 1-bit multiplication of the vector with the matrix fraction. Thus, the bits number of $\|A\|$ is

$$f_c = 2^e + f + 1 + b.$$ 

(13)

Next, we sequentially input the bits in $\|A\|$ to the crossbars and shift-and-add the collected $\|A\|$ for each of the $(2^e + f_v + 1)$ bits to get $\|A\|$ which is the result for the multiplication of the matrix block with the input $\|A\|$. The bits number of $\|A\|$ is

$$f_g = f_c + 2^{e_v} + f_v + 1 + b.$$ 

(14)

As shown in Figure 7(b), each matrix block has a sign bit, therefore, it requires two crossbar clusters in a processing engine for the signed multiplication. Each element in the input vector segment also has a sign bit. Thus, we need four $\|A\|$ and subtract them to get $\|A\|$, which is the multiplication results between the matrix block and the vector segment. The number of bits of $\|A\|$ is $(f_g + 1)$, and $\|A\|$ is a signed number due to the subtraction. Next, we convert the $\|A\|$ to a double-precision floating-point $\|A\|$. $e_b$ $\|A\|$ is the exponent base for the matrix block and $e_v$ $\|A\|$ is exponent for the vector segment. We add $\|A\|$ and $\|A\|$ to the exponent of $\|A\|$ to get the $\|A\|$. -- the

\[\text{Here, we assume that the cell precision for the ReRAM crossbars is 1-bit. For 2-bit cells, two consecutive bits are mapped to a crossbar.}\]
to get the exponents of elements in the vector segment. 

The vector converter is responsible for converting a vector segment in default floating-point precision to REFLOAT for processing in next iteration. A the exponents of elements in a vector segment is accumulated by an adder tree and shifted following Eq. (5) to get the vector exponent base $e_{vb}$. An element-wise subtraction is performed on $A$ to get $b$ the exponents of the elements in the vector segment.

### 5.3 Streaming and Scheduling

For the original large-scale sparse matrix, the non-zero elements are stored in either row-major or column-major order. However, the computation in ReRAM crossbars requires accessing elements in a matrix block, i.e., elements indexed by a single window of rows and columns. Thus, there is a mismatch between the data storage format in the original application, e.g., Matrix Merket File Format [9], and the most suitable format for REFLOAT accelerator. Direct access to the elements in each matrix block will result in random access and wasted memory bandwidth. To overcome this problem, we propose a block-major layout, which ensures that most matrix block elements can be read sequentially.

Specifically, the non-zeros of each $2^b \times 2^b$ block are stored consecutively, and the non-zeros of every $P$ blocks among the same set of rows are stored together before moving to a different set of rows, as shown in Figure 8. Here, $P$ is the number of blocks that can be processed in parallel, which is determined by the hyperparameters $b, e$, and $f$ for a given number of available ReRAM crossbars. We follow this zigzag order for blocks instead of the row-major order because it can reduce the buffer requirement for intermediate results. To obtain one output, a dot-product is performed between the input vector and a column of the original matrix. The required buffer size for row-major order is proportional to $2^b$ while in our design it is proportional to $P$.

### 5.4 Accelerator Programming

```plaintext
1 refloat b, e, f, ev, ef
2 double A_mat
3 refloat Ar_mat = (refloat) A_mat
4 double b_vec
5 double x_vec = x0_vec
6 double Ax = Ar_mat * x_vec
7 double r_vec = b_vec - Ax
8 double p_vec = r_vec
9 while (not converge) do
10   double Ap_vec = Ar_mat * (refloat) p_vec
11   double rr = r_vec.T * r_vec
12   double pAp = p_vec.T * Ap_vec
13   double alpha = rr / pAp
14   x_vec = x_vec + alpha * p_vec
15   r_vec = r_vec - alpha * Ap_vec
16   double rnew = rvec.T * r_vec
17   double beta = rnew / rr
18   p_vec = r_vec + beta * p_vec
19 end while
```

Code 2: The pseudo code for CG solver.

Conjugate Gradient (CG) [40] and Stabilized BiConjugate Gradient (BiCGSTAB) [81] are the two Krylov subspace methods used as the iterative solver in this work. We use CG as an example to illustrate how the accelerator is programmed to execute the solver. The pseudo code for the CG solver is listed in Code 2. We use `double` to indicate a variable in 64-bit (double) floating-point precision, and `refloat` to indicate a variable in REFLOAT. The variable name with a `_mat` suffix indicates a matrix, the variable name with a `_vec` suffix indicates a vector, and others are scalars.

In the beginning, the block size $b$, the exponent number for the matrix block $e$, the fraction number for the matrix block $f$, the exponent number for the vector segment $e_v$, and the fraction number for the vector segment $f_v$, in `refloat` are set. Within the accelerator, the crossbars in a bank (subbank) will be configured as clusters with the format parameter for processing SpMV in `refloat`. Then the sparse matrix $A_{mat}$ is converted to `refloat` $Ar_{mat}$ and stored in the block-major layout (Section 5.3) at Line 2 and 3. The bias vector $b_{vec}$ for the linear system and the initial solution $x_{vec}$ are loaded to the accelerator at Line 4 and 5. At Line 6, the SpMV of $Ar_{mat}$ and $x_{vec}$ is performed, where the matrix blocks of $Ar_{mat}$ are streamed to the accelerator and partial results are accumulated to an `double` vector $Ax$. At Line 7 the error vector $r_{vec}$ is computed by the MACs. At Line 8, a precision correction vector $p_{vec}$ is created. Line 9 to 19 are the main body for the CG solver. The SpMV is processed on the matrix and the precision correction vector $p_{vec}$ which is converted into `refloat` before processing at Line 10. From Line 11 to Line 13, a coefficient alpha is calculated. The dot-product of two vector is performed by the MACs. At
Line 14 and Line 15, the coefficient $\alpha$ is used to update the solution vector $x_{-vec}$ and the error vector vector $r_{-vec}$ element-wisely. From Line 16 to Line 18, another coefficient $\beta$ is calculated to update the precision correction vector. The main body continues to run until a desired stop condition (such as that the number of the iterations is larger than a threshold or that the residual $rr$ is smaller than a threshold) is reached.

6. EVALUATION

6.1 Evaluation Setup

We list the configurations for the baseline GPU platform, the state-of-the-art ReRAM accelerator [27] for scientific computing (ESCMa) and our ReFLOAT in Table 3. For the baseline GPU, we use an NVIDIA P100 GPU, which has 3584 cuda cores and a 16GB HBM2 memory. We use cuda 10.1 and cuSPARSE routines in the iterative solvers for the processing on sparse matrices. We measure the running time for the solvers on the GPU. For the two ReRAM accelerators, i.e. ESCMa and ReFLOAT, we use the parameters in Table 3 for simulation. Both the two ReRAM accelerators have 128 Banks and the crossbar size is $128 \times 128$. In ESCMa, we configure 64 clusters for each bank, which is slightly larger than that (56) in the original work [27]. There are 128 crossbars in each cluster. The precision in ESCMa is double floating-point. In ReFLOAT, we configure 128 banks, 128 subbanks per bank, and 64 crossbars per subbank. The precision in ReFLOAT is refloat with a default setting that $e = 3$, $f = 3$, $e_v = 3$ and $f_v = 8$. For the two ReRAM accelerators, the equivalent computing ReRAM is 17.1Gb. The ADC and ReRAM cells for the two accelerators are of the same configurations. We use a 1.5GS/s 10-bit pipelined SAR ADC [54] for conversion. The DAC is 1-bit, which is implemented by wordline activation. We use 1-bit SLC [67] and the write latency is 50.88ns. The computing latency for one crossbar including the ADC conversion is 107ns [27]. In the two ReRAM accelerators, each bank has a 16MB memory for buffering and 128 floating-point MACs for vector processing.

The matrices used in the evaluation are listed in Table 4. We evaluate on 12 solvable matrices from the SuiteSparse Matrix Collection (formerly UF Sparse Matrix Collection) [22]. The size (number of rows) of the matrices ranges from 4,875 to 204,316 and the number of Non-Zero entries (NZ) of the matrices ranges from 105,339 for 1,660,579. NNZ/Row is a metric for sparsity. A smaller NNZ/Row indicates a sparser matrix. NNZ/Row ranges from 4.0 to 27.7. The condition number $\kappa$ ranges widely from 3.6 to 5.74e+5. We also visualize the matrices in Table 4. We apply the iterative solvers CG and BiCGSTAB on the matrices. The convergence criteria for the solvers is that the L-2 norm of the residual vector (we use the term “residual” denoted by $R^2$ for simplicity to call the L-2 norm of the residual vector in this section) is less than $10^{-8}$. The error $|e| \leq \sum |x| = |x - \bar{x}|^2 = |r|^2/|A|^2$, where $|A|$ is a constant.

6.2 Performance

We show the performance of GPU in double and single precision floating-point, ESCMa [27] and ReFLOAT for CG and BiCGSTAB solvers in Figure 9. We evaluate the processing time $t$ for the iterative solver to satisfy that the residual is less than $10^{-8}$. The performance $p$ is defined as $p = \frac{t}{GTU_{\text{double}}/f_r}$. $x = \text{GPU-float}$, ESCMa, ESCMa-fc or ReFLOAT. For ESCMa, we evaluate both function (convergence) and hardware performance. For ESCMa-fc, we assume the function is correctly the same as that of default double. Specifically, we assume ESCMa-fc converges and takes the same iteration number to convergence as that in double and evaluate the hardware performance of ESCMa-fc.

CG solver

Overall, the geometric-mean (GMN) performance of GPU-float, and ReFLOAT are $1.11 \times$ and $20.10 \times$(up to $123.50 \times$) respectively. GPU-double, GPU-float and ReFLOAT converge on all matrices while ESCMa does not converge on 7 out of 12 matrices and the IDs of not converged matrices are 353, 354, 2261, 355, 2257, 2259, and 845. The GMN of ReFLOAT compared to ESCMa on the five converged matrices is $18.86 \times$. GPU-float benefits from faster SpMV on lower bits, but the iteration number is increased. The highest performance of GPU-float 1.20 × for Matrix 2259 and for most matrices the performance gain for switching double to single is less than 1.15 ×. For Matrix 1311, the GPU-float performance is 0.0085 ×, because it takes 1468 additional.
iterations. For most of the matrices, ReFLOAT performs better than the baseline GPU. For matrix 2257, 1848 and 2259, the performance of ReFLOAT is $1.54 \times$, $26.84 \times$ and $1.19 \times$ respectively, however, the performance of ESCMA is even lower, and it is NC. $0.16 \times$ and NC respectively.

The slow down is because the required number of clusters for SpMV is larger than the number available on the accelerators. If the number of clusters for SpMV on one matrix is fewer than the available clusters on an accelerator, the deployed clusters will be only invoked once to perform the SpMV. But, if the number of clusters for SpMV on one matrix is larger than the available clusters on an accelerator, (1) cell writing for mapping new matrix blocks to clusters and (2) cluster invoking to perform part of SpMV will happen multiple times, thus more time is consumed for one SpMV on the whole matrix. In ESCMA, with the default floating-point mapping, i.e., 118 crossbars for a cluster, there are only 2221 clusters available. However, to perform one SpMV on the whole matrix, 209263, 15797, and 381321 clusters are required respectively for matrix 2257, 1848, and 2259. The required cluster number for the two matrix is far larger than the available number in ESCMA, resulting in cell writing and cluster invoking 103, 8, and 187 times respectively for the three matrices. So the performance of ESCMA is lower than the baseline GPU on the two matrices. In ReFLOAT, to perform one SpMV on the whole matrix, the same numbers as that in ESCMA of clusters are required for matrix 2257 and matrix 2259. We configure $e = 3$, $f = 3$ for ReFLOAT, so the available clusters for matrix 2257 and matrix 2259 are 21845. The cell writing and cluster invoking times for matrix 2257 and matrix 2259 are 10 and 18 respectively, which are less than the cell writing and cluster invoking times in ESCMA.

Another reason leading to higher performance of ReFLOAT compared with ESCMA is that fewer cycles are consumed within a cluster. In ESCMA, 233 cycles are consumed for the multiplication even with the assumption that 6 bits are enough for the exponent [27]. In ReFLOAT, 28 cycles are consumed for the multiplication. Notice that with a fewer number of exponent bits and fraction bits, we can get (a) a fewer number of clusters required for a whole matrix, (b) a fewer number of cycles consumed for one matrix block floating-point multiplication within a cluster. The two effects (a) and (b) can lead to higher performance, but we also have a third effect (c) larger number of iterations to reaching convergence, which leads to lower performance. However, effects (a) and (b) is stronger than effect (c), so the performance of ReFLOAT is higher. The number of iterations for the evaluated matrices to reach convergence is listed in Table 5.

**BiCGSTAB solver.**

The geometric-mean(GMN) performance of GPU-float and ReFLOAT are $1.18 \times$ and $24.59 \times$ (up to 110.15 \times) respectively. Notice that matrix 1311 does not converge on GPU-float, and the $1.18 \times$ GMN excludes this matrix. GPU-double and ReFLOAT converge on all matrices while ESCMA does not converge on 8 out of 12 matrices and the IDs of not converged matrices are 353, 354, 2261, 355, 2257, 1848, 2259, and 845. The GMN of ReFLOAT compared to ESCMA on the four converged matrices is $54.00 \times$. The trend for the three platforms on the evaluated matrices are similar to that for CG solver. In each iteration, for BiCGSTAB solver, there are two SpMV on the whole matrix, while for CG solver, there is one SpMV on the whole matrix. From Table 5 we can see, the difference of (+/-) number of iterations to get converge in BiCGSTAB solver is smaller than the gap in CG solver for most matrices. For matrix 355, 2257, 2259 and 845, the difference is negative, which means it takes fewer iterations in refloat compared with that in double.

### 6.3 Accuracy

We show the convergence traces (the residual over each
Table 6: Bit number for exponent and fraction of matrix block and vector segment in Refloat.

| ID  | $c$ | $f$ | $c'$ | $f'$ | $c''$ | $f''$ |
|-----|-----|-----|------|------|-------|-------|
| 353 | 3   | 3   | 3    | 3    | 3     | 3     |
| 1313| 3   | 3   | 3    | 3    | 3     | 3     |
| 354 | 3   | 3   | 3    | 3    | 3     | 3     |
| 2261| 3   | 3   | 3    | 3    | 3     | 3     |
| 1288| 3   | 3   | 3    | 3    | 3     | 3     |
| 1311| 3   | 3   | 3    | 3    | 3     | 3     |
| 1289| 3   | 3   | 3    | 3    | 3     | 3     |
| 355 | 3   | 3   | 3    | 3    | 3     | 3     |
| 2257| 3   | 3   | 3    | 3    | 3     | 3     |
| 1848| 3   | 3   | 3    | 3    | 3     | 3     |
| 2259| 3   | 3   | 3    | 3    | 3     | 3     |
| 845 | 3   | 3   | 3    | 3    | 3     | 3     |

Table 7: Matrix memory overhead of Refloat normalized to ESCMA.

iteration) of the evaluated matrices in double and in refloat for CG and BiCGSTAB solver in Figure 10. The iteration number is normalized by the consumed time for the GPU baseline. The configurations of bit number for matrix block and vector segment in refloat are listed in Table 6. The absolute (non-normalized) iteration number to reaching convergence is listed in Table 5.

For CG solver, from Table 5 we can see, refloat leads to more number of iterations to get converged when we do not consider the time consumption for each iteration. From Figure 10 we can see, with the bit level representation, the residual curves are almost the same as the residual curves in default double. Most importantly, all the traces in refloat get converged faster than the traces in double. For matrix 1288 and matrix 1848, the bit number for fraction of vector segment is 16 because the default 8 leads to non-convergence.

For BiCGSTAB solver, from Table 5 we can see, while refloat leads to more number of iterations to reaching convergence for 5 matrices, the number of iterations to reaching convergence for 4 matrices are even fewer than those in double. We infer that is because lower bit representation helps to enlarge the changes in the correction term, thus leads to fewer iterations. We also notice there are spikes in the residual curves in refloat more frequently than spikes in double, but they finally reach convergence.

6.4 Memory Overhead

In Table 7, we compare the memory overhead for the matrix in refloat normalized to that in double (used in ESCMA [27]). On average, refloat consumes 0.192× memory compared with double. For matrices except 2257 and 2259, refloat consumes less than 0.2× memory compared with double. For matrix 2257 and matrix 2259, the average density within a matrix is relatively lower, thus more memory is consumed for the matrix block index and the exponent base.

7. RELATED WORKS

ReRAM-based accelerators. In recent years, the architecture design of ReRAM-based accelerators have been developed for various applications, including deep learning [5, 10, 15, 43, 44, 48, 74, 78, 94], graph processing [12, 79] and scientific computing [27]. The noise and reliability issues in ReRAM-based computing are significantly alleviated by coding techniques and architectural optimizations [28, 63, 86, 87, 88]. ReRAM-based accelerators are demonstrated on silicon by [14, 62, 83, 91, 92, 93]. Most of existing ReRAM-based accelerators are designed for fixed-point processing, especially for deep learning. Beside ESCMA [27], FloatPIM [43] accelerated floating-point multiplication in ReRAM, but FloatPIM is designed for deep learning in full-precision floating point.

Scientific computing acceleration. Computing routines on general-purpose platforms CPUs and GPUs have been developed for scientific computing, such as CuSPARSE [66], MKL [84], and LAPACK [4]. Architectural and architecture-related optimizations [21, 29, 49, 55, 61, 75, 95] on CPUs/GPUs are explored for accelerating scientific computing. Scientific computing is a major application in high performance computing and heavily relies on general-purpose platforms, but it is a new application domain for emerging PIM architectures and it is challenging because of high cost and low performance of floating-point processing.

Data format. Data formats for efficient computing are explored for CPUs/GPUs [8, 47, 58, 60, 76]. Format and architecture co-optimization includes [31, 37, 80] on conventional CMOS platforms but they are not for emerging PIM architectures and not for scientific computing. Data compression are explored on conventional memory systems [56, 70, 71].

8. CONCLUSION

ReRAM has been proved promising for accelerating fixed-point applications such as machine learning, while scientific computing is an application domain that requires floating-point processing. The main challenges for efficiently accelerating scientific computing in ReRAM is how to support low-cost floating-point SpMV in ReRAM. In this work, we address this challenge by proposing REFLOAT, a data format and a supporting accelerator architecture. REFLOAT is tailored for processing on ReRAM crossbars where the
number of effective bits is greatly reduced to reduce the crossbar cost and cycle cost for the floating-point multiplication on a matrix block. The evaluation results across a variety of benchmarks reveal that the ReFLOAT accelerator delivers an average speedup of 20.10× / 24.59× on CG / BiCGSTAB compared with a GPU baseline and an average speedup of 18.86× / 54.00× on CG / BiCGSTAB compared with a state-of-the-art ReRAM-based accelerator [27] for scientific computing.

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