Single-switch high step-up boost converter based on a novel voltage multiplier

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Abstract: A single-switch high step-up boost converter based on a novel voltage multiplier (VM) has been proposed in this study. Compared to traditional boost converter, not only the voltage conversion ratio has been increased, but also voltage stress across semiconductor devices has been decreased. Moreover, the voltage conversion ratio and voltage stress of the proposed converter can be adjusted by the number of the VM cells. The control and drive circuits for the proposed converter is as simple as boost converter as there are no additional switches. Working principles and performance characteristics of the proposed converter have been analysed in detail. A 200 W experimental prototype with three VMs has been built to validate the theoretical analysis.

1 Introduction

High step-up dc/dc converters have attracted much attention in recent years due to many applications such as photovoltaics or fuel cell power generations [1–3]. In order to acquire high step-up voltage conversion ratio, many topologies have been proposed with the use of transformers, coupled inductors, cascade structures, switch capacitors, voltage multipliers (VMs) or combination of aforementioned techniques [4–6]. However, the use of transformer would increase the overall size and cost of the system in situations where isolation is not required [7]. The leakage inductor energy of the coupled inductor could de-grade the overall efficiency of the converter or lead to complex snubber circuit and high voltage stress across the switching devices [8, 9]. Although the use of cascade converters is the simplest way to achieve a high step-up dc/dc voltage conversion ratio, several stages are required, which not only increases the cost and reduces the efficiency of the system, but also requires high voltage semiconductor components at the output stage [5]. High step-up dc/dc converters based on switched capacitors have some problems such as requirement of numerous switches, pulsating input current and complex driving circuit [10, 11].

A high voltage conversion gain can be achieved by combining VMs with traditional boost converter [12–22]. Towards achieving such a conversion gain, two-phase interleaved boost converters are proposed to be integrated with Dickson voltage multiplier (D-VM) in [12, 13] and Cockcroft-Walton voltage multiplier (CW-VM) in [14–16]. Bipolar D-VM has been used with two-phase interleaved boost converter in [17, 18]. The voltage stress on capacitors of the converters with CW-VM is lower and relatively unifed, but the current stress on these capacitors is not only high but also different from each other. In contrast, the current stress on the capacitors of converters with D-VM is close to each other, while the voltage stress on the capacitors is high and varies significantly. A generalised structure for high voltage gain dc/dc converter based on VM and two-phase interleaved boost (including both non-isolated and isolated boost) converter has been proposed in [19]. Like this generalised structure, some other topologies with various VM circuits have been proposed in [20–22]. With the adoption of such topologies, there are some common advantages like adjustable voltage conversion gain, significantly reduced voltage stress on semiconductor components and simpler control and driver circuits. However, there exist some common disadvantages too. First, at least two-phase interleaved boost converters must be used with the VMs together, second, the sum of the two switches duty cycle requires more than 1, which also results in the minimum voltage conversion ratio of these converters to be greater than 4.

Based on the proposed VM, a novel single-switch high step-up dc/dc converter is presented in this paper, which has the advantages like wide duty cycle range of the switch, requirement of only one switch, simpler control and drive circuits. Topology, operation principles and performance characteristics of the proposed converter are discussed in Sections 2 and 3, respectively. The accuracy of the theoretical analysis and the circuit characteristics are verified by experiments in Section 4.

2 Topology and operation principle of the proposed converter

The general topology configurations of the proposed converter are shown in Fig. 1a. It can be seen that the number of VM cells can be adjusted. And each proposed VM contains two capacitors, one inductor and one diode. Fig. 1b shows the proposed converter with 1 VM.

For the purpose of demonstrating its principle of operation, a simplified analytical process of the proposed converter is presented with only one VM cell as shown in Fig. 1a. Nevertheless, the analytical process can be expanded to arbitrary number of VM cells as desired. The assumptions for the analysis are given as follows:

(i) All devices are ideal and the effects of parasitic parameters are ignored;
(ii) The capacitance values of the capacitors are large enough so that the voltage ripple can be ignored.

The proposed single-switch high step-up dc/dc converter can work both on continuous conduction mode (CCM) and light load mode. There are two modes when the converter is working on CCM, and Fig. 2 shows the key waveforms of the proposed converter during one period. Detailed working process of the proposed converter is presented as follows:

Mode 1 ($t_2$–$t_3$): Switch $S_1$ is turned on. During this stage, the input voltage source charges the inductor $L_i$, the capacitor $C_i$ charges the inductor $L_{1i}$ and the capacitor $C_{1i}$, both inductor currents increase.

$I_{0}$ and the capacitor $C_{11}$ together form a resonant circuit which discharges the capacitor $C_{11}$ during this stage. So the voltage across capacitor $C_{11}$ decreases. When the voltage across capacitor $C_{11}$ decreases to zero, the inductor $L_{11}$ is fully charged while the capacitor $C_{11}$ is discharged. The voltage across the capacitor $C_{11}$ becomes negative. Therefore, the diode $D_{1}$ is conducted and discharging the inductor $L_{11}$ of the proposed circuit begins.

Mode 2 ($t_3$–$t_4$): In this stage, the voltage across capacitor $C_{11}$ is negative, and inductor $L_{11}$ is discharging through the diode $D_{1}$. The voltage across capacitor $C_{11}$ decreases slowly and the diode $D_{1}$ is turned off.

In this stage, the inductor $L_{11}$ is fully discharged, and the capacitor $C_{11}$ is charged by the input voltage source. The total gating time of the switch $S_{1}$ is $t_2$–$t_3$ and the charging time for the input is $t_3$–$t_4$.
linearly, the load is supplied by the capacitor $C_{12}$, all diodes are turned off

$$
\begin{align*}
\begin{cases}
  u_{L1} &= u_{n0} \\
  u_{C11} &= u_{n0} - u_{C12}
\end{cases}
\end{align*}
$$

Mode 2[t1-t2]: Switch $S_1$ is turned off. During this stage, all diodes work on on-state. The inductor current of $L_1$ branches off through three paths; firstly, through $D_1$, $C_1$ and $u_{in}$, secondly through $C_{11}$, $D_{11}$, the output stage ($C_{11}/R_1$) and $u_{in}$ and thirdly through $D_1$, $L_{11}$, the output stage ($C_{11}/R_1$) and $u_{in}$. In this interval, $C_1$ and $C_{12}$ are charged while $C_{11}$ is discharged, inductor currents $i_{L1}$ and $i_{L11}$ are decreased

$$
\begin{align*}
\begin{cases}
  u_{L1} &= u_{n0} - u_{C1} = u_{in} + u_{C11} - u_{C12} \\
  u_{L11} &= -u_{C1} = u_{C1} - u_{C12}
\end{cases}
\end{align*}
$$

3 Performance characteristics

3.1 Voltage conversion ratio

By volt-second balance of the inductors $L_1$ and $L_{11}$ as shown in (1) and (2), the following formula can be obtained:

$$
\begin{align*}
\begin{cases}
  u_{C1} &= \frac{u_{in}}{1-D} \\
  u_{C11} &= \frac{u_{in} - u_{C12}}{1-D} \\
  u_{n0} &= \frac{u_{in} - u_{C12}}{1-D}
\end{cases}
\end{align*}
$$

Based on (3), the voltage conversion ratio ($M$) can be obtained as follows:

$$
M = \frac{u_{n0}}{u_{in}} = \frac{1 + D}{1 - D}
$$

Extending to the proposed converter with $n$ VMs is

$$
\begin{align*}
\begin{cases}
  u_{C1} &= \frac{u_{in}}{1-D} \\
  u_{C11} &= \frac{u_{in} - u_{n0} \cdot n \cdot D}{1-D} \\
  u_{C21} &= \cdots = u_{Cn1} = \frac{u_{in} - u_{n0} \cdot D}{1-D} \\
  u_{n0} &= \frac{u_{in} - u_{n0} \cdot n \cdot D}{1-D}
\end{cases}
\end{align*}
$$

$$
M = \frac{u_{n0}}{u_{in}} = \frac{1 + n \cdot D}{1 - D}
$$

3.2 Voltage and current stress of components

As shown in Fig. 1b, the voltage stress on switch $S_1$, diodes $D_1$ and $D_{11}$ can be expressed as $u_{S1}$, $u_{D1}$ and $u_{D11}$, respectively. Based on (3), they can be obtained as

$$
\begin{align*}
\begin{cases}
  u_{S1} &= u_{D1} = u_{C1} = \frac{u_{in}}{1-D} \\
  u_{D11} &= \frac{u_{C12} - u_{C11}}{1-D}
\end{cases}
\end{align*}
$$

Based on (5), extending the voltage stress of diodes of the proposed converter with $n$ VMs is

$$
\begin{align*}
\begin{cases}
  u_{D1} &= u_{D2} = \cdots = u_{Dn0} = \frac{u_{in}}{1-D}
\end{cases}
\end{align*}
$$

In order to simplify the current stress analysis, the current ripple of $i_{L1}$, $i_{L11}$ and $i_o$ can be ignored, and their dc values are marked as $I_{L1}$, $I_{L11}$ and $I_o$, respectively. Based on capacitor charge balance requirement of $C_{12}$, $C_{11}$ and $C_1$, the average current of diode $D_1$, $D_{11}$ and inductor $L_{11}$ are equal to the output average current $I_o$, which can be expressed as

$$
I_{D1} = I_{D11} = I_{L11} = I_o
$$

(9)

To simplify the analysis, the efficiency of the converter is assumed to be 100%. Thus, the input average current $I_{L1}$ is

$$
I_{L1} = I_o \cdot \frac{1 + D}{1 - D}
$$

(10)
According to Fig. 3a, the average current of switch $S_1$ can be obtained as

$$I_{S1} = (I_{L1} + I_{L11}) \cdot D = I_o \cdot \frac{2D}{1-D} \quad (11)$$

When extending the analysis to the proposed converter with $n$ VMs, the average current of inductors, diodes and switch can be determined by

$$
\begin{align*}
I_{Dh} &= I_{Dh1} = I_{Dh2} = \cdots = I_{Dh1}\  
I_{Lh1} &= I_{Lh2} = \cdots = I_{Lh1} = I_o \\
I_{L1} &= I_o \cdot \frac{1 + n \cdot D}{1 - D} \\
I_{S1} &= I_o \cdot \frac{(n + 1) \cdot D}{1 - D} \\
\end{align*}
$$
\quad (12)

**3.3 Discontinuous current mode (DCM) and boundary condition**

To simply the analysis process of the DCM, assuming $L_1 = L_{11} = L$, that means peak-to-peak current ripples of inductors $L_1$ and $L_{11}$ are equal as shown in (13) according to (1)–(3). As shown in Fig. 4, after $i_{L11}$ decreases to zero at $t_5$, the current direction of the inductor $L_{11}$ is reversed as shown in Fig. 5a. During $t_5$ to $t_6$, $i_{L1}$ increases in the negative direction. When the amplitudes of $i_{L1}$ and $i_{L11}$ are equal at $t_5$ which is denoted as $i_M$, diodes $D_1$ and $D_{11}$ are turned off. During $t_5$ to $t_6$, $i_{L1}$ and $i_{L11}$ are kept constant, and the currents of inductors $L_1$ and $L_{11}$ flow through $u_{in}$, $C_1$ and $C_{11}$

$$\Delta i_{L1} = \Delta i_{L11} = \Delta i_o = \frac{u_{in} \cdot DT_s}{L} \quad (13)$$

By applying the principle of inductor volt-second balance to $L_1$ and $L_{11}$, (14) and (15) can be obtained

$$
\begin{align*}
\frac{u_{C1}}{D + D_M} &= \frac{u_{C11}}{D + D_M} = \frac{u_{in} \cdot D}{D_M} \\
\frac{u_o}{u_{in}} &= \frac{2D + D_M}{D_M} \\
M &= \frac{u_o}{u_{in}} = \frac{2D + D_M}{D_M} \quad (15)
\end{align*}
$$

The duty cycle $D$ is the control signal of the converter, and can be considered known. However $D_M$ is unknown, and hence another equation is needed to eliminate $D_M$ to get the voltage conversion ratio $M$.

By capacitor charge balance of $C_{11}$ and $C_{12}$, the average current of inductor $L_{11}$ is equal to the average output current. Additionally, according to the balance of input and output power of the converter, (16) can be deduced. Based on Fig. 4, the average current of inductors $L_1$ and $L_{11}$ can also be calculated as (17)

$$
\begin{align*}
I_{L1} &= \frac{u_{in} \cdot DT_s}{2L} \cdot (D + D_M) - I_M \\
I_{L11} &= \frac{u_{in} \cdot DT_s}{2L} \cdot (D + D_M) + I_M \\
\end{align*}
$$
\quad (17)

By using (15)–(17), the voltage conversion ratio of the proposed converter in DCM can be obtained as follows:

---

**Fig. 3** Equivalent circuits of the two working states  
(a) State 1,  
(b) State 2

**Fig. 4** Key waveforms of the proposed converter working on DCM

**Fig. 5** Equivalent circuits of the DCM  
(a) State 1,  
(b) State 2
\[
M = \frac{u_o}{u_{in}} = 1 + \sqrt{1 + \left( 4D^2 \cdot T_s \cdot R_L / L \right) / 2}
\]  
(18)

In the boundary condition mode, the voltage conversion ratio of the CCM is equal to that of the DCM, then from (4) and (18), the boundary factor which is defined as \( \alpha \) here, can be obtained by (19). If \( \alpha \) is larger than 1, the converter works on DCM and if \( \alpha \) is smaller than 1, the converter works on CCM

\[
\alpha = \frac{(1 - D)^2 \cdot D \cdot T_s \cdot R_L / L}{ \sqrt{2} \cdot (1 + D)}
\]  
(19)

### 3.4 Comparison of the proposed converter with other structures

Performance comparison among some other high step-up dc/dc converters, boost converter and the proposed converter is given in Table 1. Compared to boost converter, not only voltage conversion ratio of the converter can be improved but also voltage stress on devices of the converter can be decreased by the proposed VM. The voltage conversion ratio of the converters proposed in [13, 15, 21] is higher than that of the converter proposed in this paper when the number of VMs is identical. However, a specific disadvantage of the converters proposed in [13, 15, 21] is that their voltage conversion ratio is limited. Take the number of VMs as 1, for example as shown in Fig. 6, the minimum voltage conversion ratio of the converters proposed in [13, 15, 21] is 4, whereas that of the proposed converter is unity which is consistent with the traditional boost converter. Moreover, the proposed converter needs only one switch. The characteristics of the proposed converter are similar to the converter in [23] when the number of VMs is 2, however, the topology of the converter proposed in [23] is fixed and its high step-up capacity is not adjustable.

### 4 Experimental results

To verify the accuracy of the above theoretical analysis, a 200 W experimental prototype of the proposed converter with three VMs has been built and the specifications of the prototype are shown in Table 2.

![Fig. 6 Voltage conversion ratio and range comparison of the proposed converter and other converters working at CCM](image)

| parameter | values |
|-----------|--------|
| input voltage \( (u_{in}) \) | 20–100 V |
| output voltage \( (u_o) \) | 200 V |
| output power \( (P_o) \) | 200 W |
| switching frequency \( (f_s) \) | 50 kHz |
| switch \( (S_1) \) | IRFB4332 |
| diodes \( (D_1, D_{11}, D_{21}, D_{31}) \) | IDT12S60C |
| capacitors | \( C_{11}, C_{12}, C_{22}, C_{31}: 10 \mu F \) |
| | \( C_{11}, C_{21}: 30 \mu F \) |
| | \( C_{32}: 60 \mu F \) |
| inductors | \( L_{11}, L_{21}, L_{31}: 800 \mu H \) |
| | \( L_1: 300 \mu H \) |
| load resistance \( (R_L) \) | 200 \Omega |

Table 1 Comparison of the proposed converter with other structures

| topology | proposed converter | converter in [13] | converter in [15] | converter in [21] | converter in [23] | traditional boost |
|----------|--------------------|------------------|------------------|------------------|------------------|--------------------|
| number of switches | 1 | 2 | 2 | 2 | 1 | 1 |
| number of diodes | \( 1 + n \) | \( 1 + n \) | \( 2n \) | \( 2 + 2n \) | 3 | 1 |
| number of inductors | 1 | 1 | 1 | 1 | 1 | 1 |
| number of capacitors | \( 1 + 2n \) | \( 1 + n \) | \( 2n \) | \( 1 + 2n \) | 5 | 1 |
| voltage conversion ratio | \( \frac{1 + n \cdot D}{1 - D} \) | \( \frac{1 + n}{1 - D} \) | \( \frac{D \cdot (1 - D)}{1 - D} \) | \( \frac{1 + n \cdot D}{1 - D} \) | \( \frac{1 + 2D}{1 - D} \) | \( \frac{1}{1 - D} \) |
| duty cycle range | 0–1 | 0.5–1 | 0–1 | 0.5–1 | 0–1 | 0–1 |
| switch voltage stress | \( \frac{u_o}{1 + n \cdot D} \) | \( \frac{u_o}{1 + n} \) | \( \frac{u_o}{n} \) | \( \frac{u_o}{1 + n} \) | \( \frac{u_o}{1 + 2D} \) | \( u_o \) |

Table 2 Specifications of the experimental prototype
The experimental waveforms are shown in Fig. 7. Fig. 7a shows the waveforms of \( u_{gs}, u_{in}, u_{o}, \) and \( u_{S1}, \) the conversion gain is \( \sim 10 \) when the duty cycles are near 0.7, which is identical with (6). Voltage waveforms across \( D_1, D_{11}, D_{21} \) and \( D_{31} \) are shown in Fig. 7b, where voltage stresses of the diodes and switch \( S_1 \) are all nearly 65 V which is consistent with (7). Figs. 7c and d show the waveforms of \( u_{C1}, u_{C12}, u_{C22}, u_{C21} \) and \( u_{C31}. \) The dc value of \( u_{C1} \) is about 65 V, \( u_{C12} \) is about 110 V, \( u_{C22} \) is about 155 V, and the dc values of \( u_{C11}, u_{C21} \) and \( u_{C31} \) are all nearly 45 V which are consistent with (5). Fig. 7e shows the current waveforms of \( L_1, L_{11}, L_{21}, \) and \( L_{31}. \) The dc value of \( i_{L1} \) is about 10 A, and the dc values of \( i_{L11}, i_{L21} \) and \( i_{L31} \) are all about 1 A, apparently, the measured results are all consistent with the theoretical analysis.

The efficiency of the proposed converter with different loads and input voltages are shown in Fig. 8a. It is obvious that at the rated power, as the input voltage increases, the efficiency of the prototype increases. Fig. 8b shows efficiency waveforms of the prototype when the output power changes, apparently, the maximum efficiency of 96% is achieved at the output power of 275 W when the input voltage is 100 V.

The calculated loss distribution of the experimental prototype is shown in Fig. 9 when the input voltage is 20 V, the main losses are on switch, diodes and inductors, which are nearly to 8.89, 3.2 and 4.78 W, respectively.

Fig. 6 shows the voltage conversion ratio versus switch duty cycle of the proposed converter and other converters working at CCM under ideal working conditions. In actual working conditions, the voltage conversion ratio of the converter will be affected by parasitic parameters. It can be seen from Fig. 10 that when the duty ratio \( D > 0.7, \) the parasitic parameters have great influence on the voltage conversion ratio of the proposed converter.
5 Conclusion

A single-switch high step-up boost converter based on a novel VM has been proposed in this paper. Compared to the existing high step-up dc/dc converter based on conventional VMs, the proposed circuit has the following advantages: firstly, the proposed converter needs only one switch which makes its control and driver circuit simpler and secondly the duty cycle and voltage conversion ratio of the proposed converter is unlimited. Whereas the disadvantage of each proposed VM is that they are comprised of more components than that of traditional VMs. The above features make the proposed converter more suitable for applications with wide input/output voltages compared to the existing high step-up dc/dc converter based on traditional VMs. The effectiveness of the theoretical analysis of the proposed converter has been verified experimentally.

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7 References

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8 Appendix

The averaged switch model of the proposed converter working in CCM can be obtained by using the circuit averaging method proposed in [24], as shown in Fig. 11. The symbol (\(\wedge\)) shows the dynamic changes of the parameter as shown in (20) and (21). \(T_p\) is transformer primary winding, \(T_{s1}, T_{s2}, \ldots, T_{sn}\) are transformer secondary windings

\[
\begin{align*}
\langle d(t) \rangle & = D + \dot{d}(t) \\
\langle u_{0}(t) \rangle & = U_{in} + \dot{u}_{0}(t) \\
\langle u_{i}(t) \rangle & = U_{i} + \dot{u}_{i}(t) \\
\langle u_{C}(t) \rangle & = U_{C} + \dot{u}_{C}(t) \\
\langle i_{L}(t) \rangle & = I_{L} + \dot{i}_{L}(t)
\end{align*}
\]

(20)

where \(i\) is 1, 11, 12, \ldots, \(n1\) or \(n2\), and \(j\) is 1, 11, 21, \ldots, \(n1\)

\[
\begin{align*}
u_{i} & = \dot{d}(t) \cdot \frac{(n + 1) \cdot U_{in}}{D \cdot D'} \\
i_{i} & = \dot{d}(t) \cdot \frac{I_{in}}{D'}
\end{align*}
\]

(21)