An electrically reconfigurable logic gate intrinsically enabled by spin-orbit materials

Supplementary Information

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S1. Room temperature modeling of the Spin-Orbit Perpendicular-Anisotropy (SOPE) gate

The magnetic dynamics under the effect of the current induced spin-orbit torques at room temperature is governed by the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation,

\[ \frac{dm}{dt} = -\gamma m \times H_{\text{eff}} + \alpha m \times \frac{dm}{dt} + \gamma T_{\text{SOT}}, \]  

where \( m \) is a unit vector along the magnetization, \( \alpha \) is the Gilbert damping factor causing relaxation of the magnetization to its equilibrium state, and \( \gamma = g\mu_B/\hbar \) is the gyromagnetic ratio, where \( \mu_B \) is the Bohr magneton and \( g \) denotes the g-factor. At any instant of time, \( m \) makes an angle of \( \vartheta \) with \( \hat{z} \), while the plane of \( m \) and \( \hat{z} \) makes an angle \( \phi \) with \( \hat{x} \).

The spin-orbit torque comprises a damping-like torque and a field-like torque,

\[ T_{\text{SOT}} = T_{\text{DL}} + T_{\text{FL}} = \hbar \frac{J(t)}{2e M_s t_F} (\zeta m \times (x \times m) + \zeta_\perp m \times x), \]

where \( \zeta \) and \( \zeta_\perp \) denote the efficiency of the current in producing the damping-like and the field-like components, respectively. Since the field-like torque may be negligible in comparison with the damping-like torque\(^2\), the auxiliary effect of the field-like spin-orbit torque is skipped here. \( M_s \) denotes the saturation magnetization and \( t_F \) denotes the thickness of the nanomagnet placed on the spin-orbit channel. \( H_{\text{eff}} \) represents the effective field experienced by the magnetization and is expressed as

\[ H_{\text{eff}} = H_k + H_{dp} + H_d + H_L. \]

Here \( H_k \) denotes the perpendicular magnetic anisotropy field,

\[ H_k = \frac{K_u}{M_s} (m \cdot \hat{z}) \hat{z}, \]

where \( K_u \) is the magnetic anisotropy and \( M_s \) is the saturation magnetization. \( H_{dp} \) is the dipole field exerted by the reference layer. \( H_d \) denotes the demagnetization field.
\[ H_d(\mathbf{m}) = -4\pi M_s(N_i \sin(\vartheta) \sin(\varphi - \Theta) \hat{i} + N_j \sin(\vartheta) \cos(\varphi - \Theta) \hat{j} + N_z \cos(\vartheta) \hat{z}), \] 

where \( N_i, N_j, \) and \( N_z \) are demagnetizing factors and \( N_i + N_j + N_z = 1. \) Here, \( \hat{i} \) and \( \hat{j} \) represent the unit vectors along the length and width of the nanomagnet, respectively,

\[ \hat{i} = -\sin(\Theta)\hat{x} + \cos(\Theta)\hat{y} \]  
\[ \hat{j} = \cos(\Theta)\hat{x} + \sin(\Theta)\hat{y}. \]

Angle \( \Theta \) denotes the tilt angle enclosed by the length of the nanomagnet and current flow as illustrated in Fig. 1(a).

A nonzero temperature introduces thermal fluctuations to the magnetization, which is modeled by the Langevin random field \( H_L = (H_{L,x}, H_{L,y}, H_{L,z}) \). Each component of \( H_L \) follows a zero-mean Gaussian random process whose standard deviation is a function of temperature\(^5\),

\[ \delta = \sqrt{\frac{2\alpha k_B T}{\gamma M_s v_F \Delta t}}. \]

Here \( v_F \) is the volume of the nanomagnet, \( T \) denotes the temperature, and \( \Delta t \) is the duration of the constant effective thermal fluctuation field. As the current flows within the channel, the temperature increases through the Joule heating effect, and is proportional to the square of the current

\[ T(I) = T_0 + kI^2, \]

where \( I \) is the amplitude of the current, \( T_0 \) is the temperature at zero current (room temperature), and \( k \) is the Joule heating parameter which relates the temperature to the current.
Joule heating decreases $M_s$ and $K_u$ as $^2$:

$$M_s(T) = M_{s0}(1 - \beta(T - T_0))$$  \hspace{5cm} (9a)$$
$$K_u(T) = K_{u0}(1 - \eta(T - T_0)),$$  \hspace{5cm} (9b)

where $M_{s0}$ and $K_{u0}$ are, respectively, the saturation magnetization and magnetic anisotropy at temperature $T_0$. Coefficients $\beta$ and $\eta$ represent the change in, respectively, $M_s$ and $K_u$ as the temperature changes by $T - T_0$. Substituting (8) in (9), the saturation magnetization and magnetic anisotropy are proportional to the square of the current amplitude as, respectively,

$$M_s(T) = M_{s0}(1 - \beta kI^2)$$  \hspace{5cm} (10a)$$
$$K_u(T) = K_{u0}(1 - \eta kI^2).$$  \hspace{5cm} (10b)

S2. Channel current control for logic operations

To perform a logic operation, a clock pulse is applied to CLK$_P$, thereby producing a current that flows into the channel underneath $Q$. Depending on the bit stored in $P$ (stable magnetization state of $P$), the magnetic tunnel junction comprising nanomagnets R$_P$ and $P$ (MTJ$_P$) exhibits a low or a high resistance due to the magnetoresistance effect,

$$R_{p1} = R_{p0}(1 + TMR_P),$$  \hspace{5cm} (11)

where $TMR_P$ denotes the tunneling magnetoresistance ratio of MTJ$_P$ and $R_{p1}$ ($R_{p0}$) is the resistance of MTJ$_P$ when $p = 1$ ($p = 0$). Accordingly, the channel current density is

$$J^p_{0(1)} \propto \frac{V_{CLK_P}}{R_{0(1)}^p + R_{eff} + R_c}.$$  \hspace{5cm} (12)

Here $V_{CLK_P}$ is the clock pulse amplitude, $R_c$ is the interconnect resistance, and $R_{eff} = R_s||R_b||R_m$, where $R_s$, $R_b$, and $R_m$ denote the resistance of the spin-orbit layer, resistance of the buffer layer, and shunt resistance of nanomagnet $Q$. The interconnect is made of
a low resistivity metal, such as copper, thus $R_c$ is negligible compared to $R_{0(1)} + R_{eff}$.

Accordingly, from (11) and (12), we have

$$J_p^0 \propto \frac{V_{CLKP}}{R^p_0 + R_{eff}}$$

$$J_p^1 \propto \frac{V_{CLKP}}{R^p_0 \times (1 + TMR_P) + R_{eff}}.$$  \hspace{1cm} (13)

Therefore, to switch the channel current density between $J_p^0$ and $J_p^1$, TMR$_P$ should satisfy

$$TMR_P = \frac{R^p_0 + R_{eff} J_p^0 - J_p^1}{R^p_0}.$$  \hspace{1cm} (15)

For the gate with the switching probability diagram illustrated in Fig. 1, $\frac{J_p^0}{J_p^1} = 1.75$ ensures that $J_p^0$ lies within the $J_n$ region ($J+$ region) when $V_{CLKP}$ is set such that $J_p^1$ lies within the $J-$ region ($J_n$ region). Hence, by setting $R^p_0 = R_{eff}$, $TMR_P = 1.5$ (150%) is sufficient to switch the channel current density between $J_p^1 \in J-$ and $J_p^0 \in J_n$ or between $J_p^1 \in J_n$ and $J_p^0 \in J+.$

**S3. Channel current control for state transferring in cascaded gates**

Taking the same steps as in (11) to (15), and noting that $J_q^1$ is larger than $J_q^0$, the TMR$_{Q_1}$ should satisfy the following constraint so that the channel current density can be switched between $J_q^0$ and $J_q^1$.

$$TMR_{Q_1} \geq \frac{R_1 + R_{eff} J_q^0 - J_q^1}{R_1}.$$  \hspace{1cm} (16)

where $R_1$ is the resistance of MTJ$_{Q_1}$ when $q_1 = 1$ and $R_{eff} = R_s || R_b || R_m$ is the channel resistance seen from $Q_1$. Here, $R_s$, $R_b$, and $R_m$ denote the resistance of the spin-orbit layer, resistance of the buffering layer, and shunt resistance of nanomagnet $P_2$.

**S4. Energy dissipation**

The average energy dissipated by performing a NOR or NAND operation using the
SOPE gate is

\[ E = R_{\text{eff}} I_0^2 \tau_p + (1 + \frac{TMR_P}{2}) R_{\text{eff}} I_1^2 \tau_p, \]  

(17)

where \( I_0 \) and \( I_1 \) denote the amplitude of the current produced by applying a clock pulse with a duration \( \tau_p \) to CLK\(_P\) when \( p \) is, respectively, 0 and 1. By setting \( TMR_P = 1.5 \), from (13) and (14) we have

\[ E = \frac{11}{7} R_{\text{eff}} I_0^2 \tau_p = \frac{11}{7} R_{\text{eff}} (k + 1)^2 \frac{I_{\text{base}}^2}{\zeta^2} \tau_p. \]  

(18)

Here, \( I_{\text{base}} \) is the channel current required to perform the operation when \( \zeta = 1 \), and 
\[ k = \frac{\rho_s/d_s + \rho_b/d_b}{\rho_m/d_m} \]  

is a constant that captures the effect of finite shunt resistance of nanomagnet \( Q \), where \( \rho_m, \rho_s, \) and \( \rho_b \) (\( d_m, d_s, \) and \( d_b \)) demote the resistivity (thickness) of the ferromagnetic layer, spin-orbit layer, and buffer layer, respectively. As illustrated in Fig. S1, the energy dissipation per operation can range from a few aJ to a few fJ.

![Graph showing energy dissipation for performing a NAND or NOR operation using the SOPE gate.](image)

**Figure S1: Energy dissipation for performing a NAND or NOR operation using the SOPE gate.** The length, width, and thickness of the channel (ferromagnetic free layer) are set, respectively, to 45 nm, 65 nm, and 4 nm (72 nm, 24 nm, and 2 nm) and \( \Theta = 60^\circ \). The NAND and NOR operations are performed by a clock pulse with \( \tau_p = 75 \) ps. The
marked points illustrate the energy dissipation obtained using experimentally measured parameters. For the experimental setup 1 (ref. 3), a buffer layer of Ta with a thickness of 0.5 nm is inserted between the spin-orbit channel and the ferromagnet, $\zeta$ is 18.83, and $R_{\text{eff}}$ is 1 kΩ. For the experimental setup 2 (ref. 4), the spin Hall angle $\zeta$ and $R_{\text{eff}}$ are 475 and 3 kΩ, respectively. For both experimental setups $k = 1$, shunting half of the injected current through the ferromagnet.

**S5. The gate size**

Figure S2 illustrates the layout of a standard transistor with four FINs in 14 nm FinFET CMOS technology. The size of the transistor is 212 nm × 240 nm. The size of a minimum-size transistor (a transistor with one FIN) in 14 nm FinFET CMOS technology is 212 nm × 86 nm. Accordingly, the area of a SOPE gate composed of nanomagnets with a width 24 nm, a length 72 nm, and $\Theta = 60^\circ$, as illustrated in Fig. S3, can be $2.5 \times$ smaller than the minimum-size transistor. An standard charge-based NAND or NOR gate in CMOS technology is composed of four transistors. Hence, even by ignoring the size overhead imposed by the minimum metal pitch and spacing within a charge-based NAND or NOR gate, the area of a SOPE gate can be more than $10 \times$ smaller than a charge-based NAND or NOR gate implemented in 14 nm FinFET CMOS technology.
Figure S2: Layout of a standard transistor with four FINs in 14 nm FinFET CMOS technology. Nominal dimension values are indicated in the view.

Figure S3: Top view of a SOPE gate. The length and width of the nanomagnets are set to, respectively, 72 nm and 24 nm, and $\Theta = 60^\circ$. By setting $L_I = 25$ nm, the area of the SOPE gate is $2.5 \times$ smaller the minimum-size transistor in 14 nm FinFET CMOS technology.
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