Through-Silicon via Submount for Flip-Chip LEDs

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A blue light emitting diode (LED) was prepared by a flip-chip (FC) LED and three-dimensional through-silicon via (3D-TSV) technique. The experimental results indicated that the diameter and length of the Si via were about 180 μm and 400 μm, respectively. The Cu was uniformly and high density filled in each TSV, and the average resistance was about 0.14 mΩ. It was also found that the 96.43Sn-3.57Ag bumps were electroplated on the Cu plugs in TSVs of a silicon substrate, and these were smoother at 250°C. After reflow, a 3D blue light emitting diode was prepared by peak bonding at 250°C and 1000 N pressure for 30 min. Compared with the output of the LED at 417.17 mw/λ, that of the 3D LED was 424.67 mw/λ.

The increasing use of light emitting diodes (LED) in products has promoted the development of higher power, greater density, and lower cost devices. Compared with conventional LED, flip-chip (FC) LED have a number of advantages, such as about twice the light output of conventional LED. Flip-chip technology not only shortens the production process, but also significantly reduces thermal resistance and results in a greater heat dissipation rate than seen with the traditional gold wire bonded LED. Moreover, the direct contact of the electrodes or bumps with the package structure can substantially enhance the cooling effect. The flip-chip approach can also remove wire bonding and other wire frame processes, and so these LED can be used with high current drivers. Therefore, FC LED are attracting growing interest due to their greater heat dissipation, better light emission, higher reliability, and more efficient bonding processes than seen with traditional wire bonded LED.

The typical bonding process recommended by chip companies for FC LED is Au/Sn eutectic bonding. However, eutectic Sn–Ag alloy is a promising candidate among the various Pb-free solder materials for use with FC LED, and the resulting Sn–Ag alloy bumps can be easily obtained by annealing the Ag/Sn metal stack. There is also demand for new packaging processes for FC LED. The use of three-dimensional (3D) packaging through-silicon via (TSV) technology allows a high density of vertical interconnects, unlike 2D packaging, as shown in Figure 1. 3D TSV ICs have the following advantages: (1) reduced connection lengths, and thus smaller parasitic capacitance, inductance, and resistance; (2) high-speed low-power interconnects; and (3) a combination of monolithic and multifunctional integration. In this study, a blue LED was prepared using an FC LED and the 3D-TSV technique. We thus propose a new method to achieve 3D LED packing. The detailed fabrication of the TSV and the electro-optical properties of the fabricated are also discussed.

Experimental

Figure 2 presents a schematic diagram of the fabrication process for the 3D LED. A P-type 400 μm thick Si wafer was used as the bottom substrate. Photolithography was used to make a mask for etching the Al layer. A positive type photoresist, AZ-1500, was spin-coated to a thickness of 2 μm with a rotation speed of 500 rpm for 15 s, followed by 3000 rpm for 30 s. The Al layer was etched by wet etching, after using acetone to remove the PR. The TSV structures were formed by SF6 plasma etching. For the TSV process, the SF6 gas flow, O2 gas flow, substrate temperature, etching time, electrode gap, RF power, and chamber pressure were set at 90 sccm, 10.5 sccm, 4 W, and 15 mTorr, respectively.

Before the Cu electroplating process, a SiO2 isolation layer, Ti adhesion layer, and Cu seed layer were deposited on the structure of the silicon via, in this order. A SiO2 isolation layer with a thickness of 1 μm was formed by thermal oxidation. The Ti adhesion layer was deposited by thermal evaporation, with a thickness of 50 nm. The Cu seed layer was also deposited by thermal evaporation, with a thickness of 300 nm. After the Cu electroplating process a negative-type PR was spin-coated on the TSV structure, and then standard photolithography was used to define bumps. For the Cu electroplating process, the solution consisted of CuSO4 and H2SO4. The plating current and temperature were fixed at 0.8 A and 28°C, respectively. After the Cu electroplating was finished, Sn-Ag bumps were co-deposited on the Cu plugs. To electroplate Sn-Ag bumps on the Cu plugs, a direct voltage of 1.65 V was applied for 10 min. After plating Sn-Ag bumps on the Cu plugs the next process was to remove the PR/Ti adhesion layer/Cu seed layer. The samples then reflowed under a vacuum for 5 mins with the reflow temperature set at 250°C. After reflow, the samples were removed from the hotplate and air-cooled to room temperature. Finally, with the bonding of the Si substrate and the FC LED, the whole stacked chips could be joined by the Sn-Ag solder bumped, and the Si substrate and FC LED were bonded at a temperature of 250°C and pressure of 1000 N for 30 min. The experimental LED sample was obtained from Epistar Corporation. Chip wafer and chip size are 4” and 1 mm × 1 mm, respectively.

The morphology, crystallinity, and optical properties were measured using field-emission scanning electron microscopy (FESEM, JEOL JSM-7000F) and energy-dispersive spectroscopy (EDS). The resistance-current (R–I) measurements were conducted using a B1500A semiconductor parameter analyzer and measurement module at room temperature. The current-voltage (I–V) characteristics of the 3D LED were then measured at room temperature using an HP4156 semiconductor parameter analyzer.

Results and Discussion

Figures 3a–3d show a cross-sectional FESEM image of Sn-Ag solder bumps after reflow at 175°C, 200°C, 225°C and 250°C, respectively, for 5 min. Figures 3a–3b show Sn-Ag solder bumps reflow at 175°C and 200. They were found that the reflow temperature is too low to produce. Because that were not reached Sn-Ag melting point. After reflow, Figures 3c–3d show that the temperatures of 225°C and 250°C can lead to the formation of ball-shaped solder bumps, especially, the shape being smoother at 250°C. The inset image of Figure 3d shows the energy-dispersive X-ray (EDX) spectrum, with the signals indicating the presence of Sn and Ag. The atomic percentages of Sn and Ag were about 96.43% and 3.57%, respectively. With regard to the growth mechanism of these Ag-Sn bumps, it is known that the Sn2P2O7 and AgI solution serves as an electrolyte solution, and also
Figure 1. Schematic diagram of two-dimensional packing and three-dimensional packing.

\[ [\text{Sn}(\text{P}_2\text{O}_7)_2]^{2+} + 2e^- \rightarrow \text{Sn} + (\text{P}_2\text{O}_7)^{4+}, \] \[ [\text{Sn}(\text{P}_2\text{O}_7)_2]^{2+} + 2e^- \rightarrow \text{Sn} + (\text{P}_2\text{O}_7)^{4+}, \] \[ \text{AgI (solid)} \rightarrow \text{AgI (dissolved)}, \] \[ \text{AgI (dissolved)} + \sigma \rightarrow \text{AgI (adsorbed)}, \] \[ \text{AgI (adsorbed)} + e^- \rightarrow \text{Ag} + \Gamma^-. \]

Figure 2. A process flow of flip chip LED for 3D-staking.

Figure 3a shows a cross-sectional optical microscope image of a Cu/TSV. The Cu uniformly filled in each TSV. The gap between TSVs is about ∼260 μm. The side length and width of the TSV were about ∼400 μm and ∼180 μm, respectively. The etching mechanism used with the TSV in cryogenic DRIE. SF₆ and O₂ are provided as continuous gas flows inside the reactor. During the process these gases react with silicon and form a solid passivation layer of SiOₓFᵧ at surface temperatures below −110 °C. Due to direct kinetic energy transfer by the ions, the bottom is far more easily cracked than the sidewalls. The cryogenic silicon etching is a passivated etching utilizing SF₆ as the etching gas and O₂ as a catalyst for the passivation layer which was first demonstrated by Tachi et al. We use the SF₆ to create a mixture of SF₆ and F species by plasma ionization. The fluorine ion is the most important element in this splitting because F atom can remove a Si atom. SF₆ is an attaching gas or electronegative element. In other words, the free electrons (e⁻) are readily removed from a discharge by the formation of negative ions in processes. After the free electrons (e⁻) attached to a neutral gas molecule, the passivation layer is formed with O ions and SiFₓ. By lowering the recombination temperature, the Si, F, and O ions were easier to form a thin SiOₓFᵧ layer. Therefore, the DRIE etching reactions for the TSV structure are as shown in Eqs. [15]:

\[ \text{SF}_6 + e^- \rightarrow \text{S}_{6} \text{F}^+ + \text{S}_3 \text{F}^+ + \text{F} + 2e^- \] \[ \text{O}_2 + e^- \rightarrow \text{O}^+ + \text{O} + 2e^- \]

Figure 4a shows a cross-sectional optical microscope image of a Cu/TSV. The Cu uniformly filled in each TSV. The gap between TSVs is about ∼260 μm. The side length and width of the TSV were about ∼400 μm and ∼180 μm, respectively. The etching mechanism used with the TSV in cryogenic DRIE. SF₆ and O₂ are provided as continuous gas flows inside the reactor. During the process these gases react with silicon and form a solid passivation layer of SiOₓFᵧ at surface temperatures below −110 °C. Due to direct kinetic energy transfer by the ions, the bottom is far more easily cracked than the sidewalls. The cryogenic silicon etching is a passivated etching utilizing SF₆ as the etching gas and O₂ as a catalyst for the passivation layer which was first demonstrated by Tachi et al. We use the SF₆ to create a mixture of SF₆ and F species by plasma ionization. The fluorine ion is the most important element in this splitting because F atom can remove a Si atom. SF₆ is an attaching gas or electronegative element. In other words, the free electrons (e⁻) are readily removed from a discharge by the formation of negative ions in processes. After the free electrons (e⁻) attached to a neutral gas molecule, the passivation layer is formed with O ions and SiFₓ. By lowering the recombination temperature, the Si, F, and O ions were easier to form a thin SiOₓFᵧ layer. Therefore, the DRIE etching reactions for the TSV structure are as shown in Eqs. [15]:

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Figure 4. (a) Cross-sectional optical microscopy image of Cu/TSV. (b) Measured resistance of single Cu TSV at various current.

Figure 5. A cross-sectional FESEM image of the 3D LED.

Figure 4b shows the average resistance ($\sim 0.14 \, \Omega \cdot \text{m}$) of a single Cu/TSV measured at various current levels. The calculated resistivity $\rho$ of a single Cu TSV is $1.8 \times 10^{-8} \, \Omega \cdot \text{m}$, which matches the theoretical value of a Cu block ($1.7 \times 10^{-8} \, \Omega \cdot \text{m}$), and indicates that the contact resistance of TSVs and the metal layer was good.

With regard to chip-to-chip bonding, after the solder balls were attached to the silicon chip, a 1 mm $\times$ 1 mm LED chip was bonded to the silicon substrate using a Micro Chip Mounting Machine (LCB1106R). The peak bonding temperature was 250 $^\circ$C, and the pressure was 1000N. The bonding time in which the solder melted was 30 min. The gap between the LED and substrate is $\sim 26 \, \mu\text{m}$, as shown in Figure 5.

Figure 6 shows thermal images of the (a) 3D LED chips and (b) LEDs. It can be clearly seen that the temperature of the 3D LED was lower than that of the LED. Furthermore, it was found that with a 1 A injection current the maximum temperatures were 92.4 $^\circ$C and 119.4 $^\circ$C for the 3D LED and LED, respectively. The TSV structure can thus reduce the temperature of the LED.

Figure 7a is actually voltage–current (V–I) characteristics of the 3D LED chips. When the bias voltage was reduced from $+3 \, \text{V}$ to $-5 \, \text{V}$. The inset of Figure 7a shows the V-I characteristics demonstrate that these devices behave it was found that the reverse current were $-7.2 \times 10^{-9} \, \text{A}$ at $-5 \, \text{V}$. With $2.3 \times 10^{-8} \, \text{A}$ current injection, we obtained forward voltages of 1.87 $\text{V}$. While for the higher turn-on voltage is that one side of the p-n junction becomes a variable resistor when the opposite side is operating at forward bias. Another reason is that the edge effect and interface significantly influence the device characteristics when the p-n junction is shrunk to the nanoscale. Figure 7b shows the external quantum efficiency (EQE) for the 3D LED chips. It can also be seen that the maximum efficiency occurred at 35 mA. Furthermore, it was found that the maximum EQEs were 54.34% for the 3D LED. As we increased the injection current to 700 mA, the EQE reduced to 45.68% for the 3D LED.

With regard to the wafer-to-wafer bonding, Figure 8a shows a photograph of the wafer level. It was found that the 6" silicon wafer completed integration stacking with the 4" LED wafer. We then examined whether the wafers had any ruptures. Figure 8b shows a photograph of the 3D LED lighted in a test. We used a power supply current of 0.5 A to test the LED chip, and the corresponding voltage was 3.2 $\text{V}$. We then randomly selected a 3D TSV and touched it with a probe from the back side, and the LED was illuminated. In other words, a 4" LED wafer was successfully bonded on a 6" TSV Si wafer.

Table I shows the current-voltage (I-V) of the LED chips and 3D LEDs. The measurements were taken at room temperature using a Keithley 2430 Source Meter combined with an integrating sphere. With 1 A current injection to the LED on TSV, it was found that the output was an average of 424.67 mw/w. Then, with 1 A current injection to the LED chip, it was found that the output was an
average of 417.17 mw/w. This shows that the output power characteristics of the LED on TSV were nearly the same as those of the LED chip, and thus this study successfully fabricated the Cu TSV structure.

### Conclusions

In summary, in this study we used a FC LED and 3D-TSV to prepare a blue 3D LED. The use of 3D packaging TSV technology allow a high density of vertical interconnects, unlike 2D packing, as shown in Figure 1. In addition, with silicon substrate used TSV can be internal connection and provide the effect of cooling, it can improve light output power of LED chip, as shown in Figure 6. The results of experiments indicated that the diameter and length of the Si vias were about 180 μm and 400 μm, respectively. The Cu uniformly and high density filled in each TSV, and the average resistance was about 0.14 mΩ. It was also found that 96.43Sn-3.57%Ag bumps were electroplated on the Cu plugged TSVs of a silicon substrate, and the shapes of these were smoother at 250 °C. After reflow, a 3D blue LED was prepared by peak bonding at 250 °C and 1000N pressure for 30 min. While the LED had output of 417.17 mw/w, the figure for the 3D LED was 426.6 mw/w.

### Acknowledgments

The authors thank the Ministry of Science and Technology, Taiwan (104GE05, 103-2221-E-492-047-MY3), for its support for this project, as well as National Nano Devices Laboratories, Tainan, Taiwan.

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