Adapting Scan Based Test Vector for Compression Method Based On Transition Technique

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Abstract

Present complexity of System on Chip (SoC) design is increasing rapidly in the number of test patterns, huge switching activity and its transition time. This large test data volume is becoming one of the major problems in association with huge switching activity and its corresponding response time. This paper considers the problem of huge test pattern in scan based design. This proposed algorithm is based on reducing test pattern on scan shift in operation. This is achieved by identifying test data transition and equally segmenting the scan based test patterns. Each scan test pattern is considered by its transition and segmented into equal necessary blocks. This finally gives the compressed test patterns in reduced test patterns. Theoretical analysis and experimental results on ISCAS89 shows that the proposed method reduces test pattern by 37% when compared to the traditional approaches.

Keywords: Test pattern; Segment blocks; Compression; Transition.

1. INTRODUCTION

Today’s System on Chip (SoC) complexity continues to grow in size, increasing data volume and cost of the manufactured chip testing in the semiconductor industry. This huge integrated complexity challenges the scan based testing of sequential circuits with flip-flops used in scan based design becoming one of the major power consuming devices. Shift operation for loading and observing the test data leads to excessive transition in the corresponding flip-flop. This excessive transition in primary input increases the power consumption and reduces correlation between consecutive test pattern including the unnecessary switching activities of circuit signals.

Test data compression can be classified into four different categories depending upon how test patterns are handled in compression method. If compression occurs on fixed number of test pattern and...
produces fixed number of compressed output, then it belongs to fixed to fixed category. Similarly, if compression occurs on variable test pattern and produces variable number of compressed output, then it belongs to variable to variable category. Other combination techniques such as fixed to variable test pattern and variable to fixed test pattern are also possible.

2. RELATED WORKS

The problem of reducing test patterns for SoC has been attended from several different angles in recent literatures. Many techniques for compressing scan based test pattern have been summarized in [1]. Test patterns reduced through scan chain concealment are discussed in [2], which uses XOR network in scan based design. A customized counter is proposed in [3], which suggests the use of two dimensional test pattern compressions. In the LFSR reseeding base test compression [4] method, the don’t care bits in test pattern are filled with necessary pseudo-random code. It increases reasonable encoding efficiency of LFSR reseeding. Dual speed LFSR was proposed in [5] to reduce test pattern. This deals with two different LFSR. The normal LFSR is used as conventional LFSR reseeding and an additional LFSR is used to mask patterns. This also depends on the test pattern’s transition density. Overlapping slice set technique is used in [6]. This produces no transition in the overlapping block. This scheme is used to reduce the number of specified bits and the number of transitions at the same time.

In this paper, fixed to fixed compression category is proposed. This paper first introduces the basic concept of segmented transition and non-transition test pattern. In later stages of this paper the proposed algorithm is elaborated. The rest of this paper is organized as follows: Section 3 presents the proposed method of segment blocks, transition and non-transition test patterns. The proposed algorithm has also been described in Section 3. Experimental results for large ISCAS89 benchmark circuits are conducted in Section 4. Finally conclusion on this work is preceded in Section 5.

3. PROPOSED WORK

This section explains the proposed method for reducing the number of test patterns in scan base design. The concept of proposed compression method is to identify the number of transition and non-transition test patterns in the design.

A transition based compression methodology to reduce the number of transition in the scan based design is proposed here which is based on segmentation of each and every scan test patterns into necessary blocks. According to the segmentation, the test patterns are classified as transition and non-transition segments. In transition segment the test pattern is a combination of “0” and “1” only. Thus there is a possibility of more transition in scan based test patterns. Non-transition of the test patterns is the combination of “0” with ‘X’ or ‘1’ with ‘X’ or ‘X’ with ‘X’. Thus no transition is performed inside the segmentation.

Following example illustrates the selection procedure of the proposed segment based compression scheme. Given test patterns T1 contain 16 test vectors with the combination of ‘0’, ’1’ and ‘X’. T1 = 0 0 1 0 1 1 X X X X 1 0 0 0 X. For example T1 contains the segment size as 4. Thus 4 segments with each 4 test patterns are separated as shown in this discussion. As per the proposed scheme the final given test pattern is grouped as 1 transition partition (T-P) and 3 non-transitions partition (NT-P). Unspecified values are considered for low transition, by assigning the A-fill method [7].

Test pattern compression is considered after identifying the transition and non-transition segmentation for a given test pattern.
This proposed algorithm is considered for finding segment size vector, filling unspecified bit with adjacent fill technique and finding transition and non-transition test patterns. Length of the scan test pattern (n) is divided with necessary segment values (s). If ‘n’ is divisible by ‘s’ the segment vector (svector) is considered for transition. If ‘n’ is not divisible by proper value, then consider for adding non-transition value (X). This fulfills the segment technique in proper format. Once svector is identified, then fill the remaining unspecified test pattern with adjacent fill. This will minimize more scan transition in the test patterns. Finally consider transition and non-transition test patterns during shift in operation activity.

Algorithm segmentation-transition (testvector, m, n, s, tvector)

Input:
m – Number of test pattern lines
n – Length of each pattern (or) number of bits for each line
testvector – Contains ‘m’ number of lines
s – Number of segments

Output:
tvector – contains ‘m’ number of vectors each vector have ‘s’ no of segments

initialize i=0;
for each line in testvector
1. Find segment size:
   if n%s = 0 then
      split the line in the exactly ‘s’ number of segment. Each consists of exactly n/s number of bits. Store the segment into svector[i]
   else
      split the line into ‘s’ number of segment. Find remaining bits as r = n%s. Set the size for the first (s-1) number of segment as ((n/s) + 1) number of bits. For the last segment append (s-r) number of ‘X’ and make its size as ((n/s)+1). Store the segment into svector[i]
   endif
2. Filling unspecified bit with adjacent fill technique.
3. Finding transition and non-transition test patterns.
4. Calculate Compression ration.

3. EXPERIMENTAL RESULTS

This section describes the experiment performed to asses the efficiency of achieving compression based on scan segmentation method. The proposed method is implemented using C and VHDL language and tested with full scan version of the ISCAS89 benchmark circuits. Test patterns used in these experiments are obtained by using Mintest dynamic compaction algorithm [8] as in Table 1. All the provided test patterns target 100% fault coverage.
Each test pattern was compressed corresponding to scan segment and its transition activity. Scan segment is divided equally to achieve higher compression ratio. Depending up on the occurrence of transition in segment, the test patterns are considered for compression. Figure 1 presents the experimental results of ISCAS-S5378 benchmark with scan segment and transition vector reduction. This shows that number of transition vector reduction depends on huge number of segmentation. This will increase the compression ration of test patterns. Table 2 shows the experimental results for the several ISCAS benchmark which are divided into different segment size. The number of specified segments and the number of transition test patterns are compared with original test patterns. The last four columns represent the transition vector reduction with its corresponding segment size (S). Depending upon the segmentation value the test pattern is reduced significantly.

| ISCAS89 | Mintest | Sequential | Flip | Fop | Primary Input | Primary Output | Faults |
|---------|---------|------------|------|-----|---------------|----------------|--------|
| s5378   | 23754   | 36         | 179  | 35  | 49            | 4603           |        |
| s9234   | 39273   | 26         | 211  | 19  | 22            | 3938           |        |
| s15850  | 76986   | --         | 534  | 77  | 150           | --             |        |

Table 1. Summary of ISCAS89 sequential benchmark circuits [8]

![Transition vector reduction](image)

Figure 1. Experimental results of transition vector reduction for various segment levels

| ISCAS89 | Mintest | S=2 | S=3 | S=4 | S=5 | S=6 |
|---------|---------|-----|-----|-----|-----|-----|
| s5378   | 23754   | 1   | 49  | 64  | 97  | 159 |
| s9234   | 39273   | 4   | 9   | 53  | 66  | 92  |
| s15850  | 76986   | 3   | 82  | 139 | 193 | 245 |

Table 2. Results of the proposed scheme on Transition vector reduction

Figure 2 shows the experimental results for segment size equal to 8. Existing method of Dual LFSR [5] is compared with proposed algorithm. Results show that the rate of reduction in the number of transition is given in percentage. It can be seen that the proposed algorithm achieves much compression ratio and introduces lesser transition than previous methods. Table 3 shows the proposed method of ISCAS89 benchmark has an increase in 7% to 12% when compared with Dual LFSR [5] method.
Figure 2. Results for proposed compression and Dual LFSR [5]

| ISCAS89 | Dual-LFSR [5] | Proposed |
|---------|---------------|----------|
| S5378   | 25            | 32       |
| S9234   | 24            | 18       |
| S15850  | 25            | 37       |

Table 3. Result Comparisons of Dual LFSR [5] with proposed method (%)

4. CONCLUSION

The present challenge of reducing test pattern is one of the most important tasks in SoC design. It is very particularly identified in the field of scan based test patterns. This paper proposes a new algorithm of segmentation technique with transition activity. This proposed algorithm segments each test pattern equally. Thus each segment consists of transition and non-transition test patterns. Compression is considered on non-transition test pattern segments. Experimental results for the ISCAS89 benchmark circuits show that 37% of test pattern is reduced significantly. It can be proved that power and transition time may also be reduced.

REFERENCES

[1] N. A. Tauba. “Survey of Test Vector Compression Techniques”, IEEE transaction Design & Test of Computers, 2006.
[2] I. Bayraktaroglu and A. Orailoglu, “Test Volume and Application Time Reduction Through Scan Chain Concealment”, Proc. of DAC, 2001, pp. 151-155.
[3] H.-G. Liang, et.al, “Two dimensional test data compression for scan-based deterministic BIST”, Proc. ITC., 2001, pp. 894–902.
[4] H.-S. Kim, and S. Kang, “Increasing Encoding Efficiency of LFSR Reseeding-Based Test Compression”, IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, May 2006, ol. 25, No. 5.
[5] P.M. Rosinger, B.M. Al-Hashimi, and N. Nicolici, “Dual Multiple-Polynomial LFSR for Low-Power Mixed-Mode BIST, IEE Proc. Computers and Digital Techniques”, July 2003, 209-217.
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REFERENCES

[1] N. A. Tauba. “Survey of Test Vector Compression Techniques”, IEEE transaction Design & Test of Computers, 2006.

[2] I. Bayraktaroglu and A. Orailoglu, “Test Volume and Application Time Reduction Through Scan Chain Concealment”, Proc. of DAC, 2001, pp. 151-155.

[3] H.-G.Liang, et.al, “Two dimensional test data compression for scan-based deterministic BIST”, Proc. ITC., 2001, pp. 894–902.

[4] H.-S. Kim, and S. Kang, “Increasing Encoding Efficiency of LFSR Reseeding-Based Test Compression”, IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, May 2006, vol. 25, No. 5.

[5] P.M. Rosinger, B.M. Al-Hashimi, and N. Nicolici, “Dual Multiple-Polynomial LFSR for Low-Power Mixed-Mode BIST, IEE Proc. Computers and Digital Techniques”, July 2003, 209-217.

[6] J. Li, Y. Han, and X. Li, “Deterministic and Low Power BIST Based on Scan Slice Overlapping”, IEEE Int. Symposium on Circuits and Systems, Kobe, May 2005, 5670-673.

[7] Anshuman Chandra, Krishnedu chakrabarty, “Low power scan testing and test data compression for system on chip”, IEEE Trans., OnCAD, May 2002.

[8] L.Hamzaoglu and J.H.Patel, “Test set compaction algorithms for combinational circuits”, Proc of CAD. Nov 1998, 283-289.