Linear controller design for a large dc gain converter

Farzin Asadi 1,*, Nurettin Abut 2, Uzeyir Akca 3

1Mechatronics Engineering Department, Kocaeli University, Kocaeli, Turkey
2Electrical Engineering Department, Kocaeli University, Kocaeli, Turkey
3Kocaeli Vocational School, Kocaeli University, Kocaeli, Turkey

A R T I C L E  I N F O

Article history:
Received 10 January 2017
Received in revised form 29 April 2017
Accepted 11 May 2017

Keywords:
Feedback control
Large dc gain converter
Non minimum phase system
State space averaging

A B S T R A C T

Environmental friendly energy sources like solar, fuel or wind cells provide low voltage levels. Grids work with higher voltage levels so step up is required before connecting these new energy sources to grid. Conventional boost converter is not able to provide a large DC gain. There are some topologies available in literature which provides required high DC gain. Without a suitable control system, converter’s output may change due to disturbances like: Input voltage’s changes and output load’s changes. This paper designs a controller for one of the recently proposed high DC gain topologies. Converters dynamical equations are extracted using State Space Averaging (SSA). Controller is designed based on the obtained dynamics. Close loop system has been tested in Simulink® environment. Simulation results showed the performance of designed controller.

© 2017 The Authors. Published by IASE. This is an open access article under the CC BY-NC-ND license (http://creativecommons.org/licenses/by-nc-nd/4.0/).

1. Introduction

Energy has an important role in modern world. Increasing use of fossil energies raises serious environmental concerns. Burning of fossil fuels produces CO₂, one of the greenhouse gases which contribute to global warming. Recently, renewable energy sources have attracted much attention. Sun is one the most important sources of renewable energy (Leyva-Ramos et al., 2013; Danandeh et al., 2012). Conversion of sun radiation to electric power is done by solar panels. According to I-V characteristic of solar panels, a DC-DC converter is required for maximum power point tracking. Also, DC-DC converter increases the low voltage of solar panels to the level required by the load. Used converter must have low input current ripple (Evran and Aydemir, 2013), so converters with an inductor in series with input source like boost converter are preferred. However, boost converter can’t be used to provide a high conversion ratio (Hsieh et al., 2013).

Cascading two or more boost converters can be used to obtain a higher conversion ratio but this method needs a more complex controller (Rahimi and Emadi, 2009). Plenty of high voltage gain topologies has been introduced (Luo and Ye, 2003; Wu et al., 2005; Jang and Jovanovic, 2007; Axelrod et al., 2008; Ismail et al., 2008a; Wu et al., 2008; Fardoun and Ismail, 2010; Choi et al., 2011; Jiao et al., 2011; Luo, 2011; Qian et al., 2012; Rosas-Caro et al., 2013; Li et al., 2015; Yang et al., 2009). Although control engineering has considerable progress over recent decades, most applications use PID controllers, because of their low price and simplicity. Generally speaking, using derivative term is not so common in power electronics converters control. Usually a P or PI controller is all that is required. This paper designs a controller for one of the recently published topologies (Li et al., 2015).

2. Working principles of large DC gain step-up DC-DC converter

Fig. 1 shows the high dc gain step up converter suggested by Li et al. (2015). When switch is closed (Fig. 2), L is charged by voltage source, D₂ is forward bias while D1 and D3 are reverse bias. C1 and C2 are charged very quickly since there is no resistance in their path except of parasitic resistances. When switch is opened (Fig. 3), inductor releases the stored energy to the load.

Voltage stress on the switches is an important issue in high gain converters. High voltage stress limits performance and efficiency of converter. Voltage stress of aforementioned converter is equal to $V_{out}/2$. A comparison between some of the topologies available in literature has been done in Table 1 (Li et al., 2015).
Applying volt-second balance (Mohan et al., 2003) to this circuit leads to Eqs. 1 and 2:

\[ v_{C1} = v_{C2} = \frac{v_{out}}{2} = \frac{1}{1-D} v_s \]  

(1)

and

\[ M = \frac{v_{out}}{v_s} = \frac{2}{1-D} v_s \]  

(2)

3. Small signal model extraction

Equivalent circuit for closed switch is shown in Fig. 4. Using Kirchhoff’s Voltage and Current Law (KVL and KCL), Eq. 3 is obtained.

\[
\begin{bmatrix}
L & -(r_{C1} + r_D + r_{C2})C_1 & 0 & r_{Co}C_o \\
\frac{1}{r_{sw}} & -C_1 & 0 & 0 \\
0 & C_1 & -C_2 & 0 & C_o + \frac{r_{Co}C_o}{R_L} \\
0 & 0 & C_1 & 0 & C_o + \frac{r_{Co}C_o}{R_L}
\end{bmatrix} \cdot \begin{bmatrix}
\frac{di_1}{dt} \\
\frac{dv_{C1}}{dt} \\
\frac{dv_{C2}}{dt} \\
\frac{dv_{Co}}{dt}
\end{bmatrix} = \begin{bmatrix}
0 \\
-\frac{1}{r_{sw}} v_s \\
0 \\
-\frac{1}{R_L} v_{Co}
\end{bmatrix}
\]

(3)

where \( \Delta = -(r_1 + r_L)i_L + v_{C1} + v_{C2} - v_{Co} + v_D + v_S \).

Using matrix inversion, Eq. 3 can be written as:

\[
\begin{bmatrix}
\frac{di_1}{dt} \\
\frac{dv_{C1}}{dt} \\
\frac{dv_{C2}}{dt} \\
\frac{dv_{Co}}{dt}
\end{bmatrix} = \begin{bmatrix}
L & -(r_{C1} + r_D + r_{C2})C_1 & 0 & r_{Co}C_o \\
\frac{1}{r_{sw}} & -C_1 & 0 & 0 \\
0 & C_1 & -C_2 & 0 & C_o + \frac{r_{Co}C_o}{R_L} \\
0 & 0 & C_1 & 0 & C_o + \frac{r_{Co}C_o}{R_L}
\end{bmatrix}^{-1} \cdot \begin{bmatrix}
\delta \\
0 \\
0 \\
0 \\
0
\end{bmatrix}
\]

(4)

Equivalent circuit for opened switch is shown in Fig. 5.

**Table 1: Comparison of the DC gain and voltage stress of available high DC gain converters**

| Converters       | Li et al. (2015) | Axelrod et al. (2008) | Maksimovic (1989) | Jiao et al. (2011) | Ismail et al. (2008b) | Prudente et al. (2008) | Hwu and Yau (2012) |
|------------------|------------------|-----------------------|-------------------|--------------------|------------------------|------------------------|---------------------|
| DC gain          | 1 - D            | 1 - D                 | (1 - D)^2         | 1 - D             | 1 - D                  | 1 - D                  | 1 - D               |
| Maximum voltage  | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) |
| stress on diodes | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) |
| Voltage stress   | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) | \( \frac{v_{out}}{v_s} \) |

Applying KVL and KCL leads to the Eqs. 5 and 6:

\[
\begin{bmatrix}
\frac{di_1}{dt} \\
\frac{dv_{C1}}{dt} \\
\frac{dv_{C2}}{dt} \\
\frac{dv_{Co}}{dt}
\end{bmatrix} = \begin{bmatrix}
L & 0 & -(r_{C2} + r_D)C_2 & 0 & r_{Co}C_o \\
0 & -C_1 & 0 & 0 & C_o + \frac{r_{Co}C_o}{R_L} \\
0 & 0 & -C_2 & 0 & C_o + \frac{r_{Co}C_o}{R_L} \\
0 & 0 & 0 & 0 & C_o + \frac{r_{Co}C_o}{R_L}
\end{bmatrix} \cdot \begin{bmatrix}
\delta \\
i_L \\
i_L - \frac{1}{R_L} v_{Co} \\
-L v_{C1} + v_{C2}
\end{bmatrix}
\]

(5)

where \( \delta = -(r_1 + r_L)i_L + v_{C2} - v_{Co} - v_D + v_S \). Using matrix inversion, Eq. 5 can be written as Eq. 6.

Averaging and small signal linearization is key steps of SSA. Applying the aforementioned steps to Eqs. 4 and 6 is quite tedious, time consuming and error prone for hand analysis.
The following scenario is used to test the close loop system: Input voltage's value changes from 10 V to 10 V at t=1 ms. Output load changes from 514 Ω to 168 Ω at t=200 ms. Test scenario is summarized in Table 2.

Using Routh-Hurwitz table, 0 < k < 0.73 make the close loop unity feedback system stable. Using MATLAB's control system toolbox $K_f = 0.41$ is selected to have no overshoot in step response. Following scenario is used to test the close loop system: Input voltage's value changes from 10 V to 10 V at t=1 ms. Output load changes from 514 Ω to 168 Ω at t=200 ms. Test scenario is summarized in Table 2.

4. Controller design

Tracking step reference signals with zero steady state error is possible if and only if (open) loop transfer function contains at least one integrator. Plant's transfer function contains no integrator so a simple I type controller with the following transfer function is selected (Eq. 15):

$$H = \frac{K_i}{s}$$

Using MATLAB's symbolic math toolbox, following transfer functions are obtained (Eqs. 7-10):

$$\frac{v_{C1}(s)}{d(s)} = \frac{1.212 \times 10^5 s^2 + 4.2 \times 10^{10} s - 5.85 \times 10^{15} s + 4.515 \times 10^{19}}{s^4 + 1.789 s^3 + 6.069 \times 10^5 s^2 + 2.08 \times 10^{11} s + 1.931 \times 10^{17}}$$

$$\frac{v_{C2}(s)}{d(s)} = \frac{1.212 \times 10^5 s^2 + 4.2 \times 10^{10} s - 5.85 \times 10^{15} s + 4.515 \times 10^{19}}{s^4 + 1.789 s^3 + 6.069 \times 10^5 s^2 + 2.08 \times 10^{11} s + 1.931 \times 10^{17}}$$

$$\frac{v_{C0}(s)}{d(s)} = \frac{0.943 \times 10^5 s^2 - 1.48 \times 10^7 s^2 - 1.967 \times 10^5 s^2 + 9.942 \times 10^{13}}{1.055 s^4 + 8.166 \times 10^8 s^3 + 1.531 \times 10^{10} s^2 + 1.931 \times 10^{12} s + 1.931 \times 10^7}$$

Pole-zero diagram of these transfer functions are shown in Figs. 6, 7, 8, 9, and 10.

As shown in Figs. 6, 7, 8, 9, and 10, $\frac{v_{C1}(s)}{d(s)}$, $\frac{v_{C2}(s)}{d(s)}$, and $\frac{v_{C0}(s)}{d(s)}$ are non-minimum phase. Also, there is stable pole-zero cancelation, so Eqs. 7-10 can be simplified to (Eqs. 11-14). Frequency response of $\frac{v_{C0}(s)}{d(s)}$ is shown in Fig. 11.

$$\frac{v_{C1}(s)}{d(s)} = \frac{1.212 \times 10^5 s^2 - 1.311 \times 10^{10} s + 9.932 \times 10^{15}}{s^4 + 1.334 \times 10^5 s^3 + 4.765 \times 10^{11} s^2 + 4.249 \times 10^{11}}$$

$$\frac{v_{C2}(s)}{d(s)} = \frac{1.212 \times 10^5 s^2 - 1.311 \times 10^{10} s + 9.932 \times 10^{15}}{s^4 + 1.334 \times 10^5 s^3 + 4.765 \times 10^{11} s^2 + 4.249 \times 10^{11}}$$

Fig. 6: Pole-zero diagram of $\frac{v_{C1}(s)}{d(s)}$

Fig. 7: Pole-zero diagram of $\frac{v_{C2}(s)}{d(s)}$

Fig. 8: Pole-zero diagram of $\frac{v_{C0}(s)}{d(s)}$

Table 1
decrease to 91 Volts.) while system with controller bypass the disturbances and keeps output voltage constant and has no overshoot.

![Fig. 9: Pole-zero diagram of $i_{L}(s)$ (left) and zooming diagram toward origin (right)](image)

![Fig. 10: Pole-zero diagram of $v_{C}(s)$](image)

![Fig. 11: $v_{C}(s)$ frequency response](image)

![Comparison of open loop and close loop](image)

**Table 2: Test scenario**

| Parameter     | Time  | From | To  | Initial | Final |
|---------------|-------|------|-----|---------|-------|
| Input voltage | 100 ms| 15   | 12  | -25%    |       |
| Output load   | 200 ms| 514 Ω| 168 Ω| -67%    |       |

**5. Conclusion**

Development of renewable energy sources has a great influence on daily life. Connecting these sources to grid needs a high DC gain converter. Disturbances like: Input voltage source’s changes and output load’s changes, may change converter’s output voltage, so a controller is required to keep output voltage constant. This paper designs a linear controller for one of the recently proposed high DC gain topologies. Next step is applying nonlinear techniques.

**List of symbols**

- $i$: Current
- $v$: Voltage
- $i_{Lj}$: $j^{th}$ inductor current
- $v_{Cj}$: $j^{th}$ capacitor voltage
- $r_{L} (r_{C})$: Series resistance of inductor (capacitor)
- $V_{D}$: Diode’s forward voltage drop
- $r_{D}$: Diode’s forward bias resistance
- $r_{sw}$: MOSFET’s on resistance
- $r_{i}$: Input source’s internal resistance
- $R_{L}$: Load resistor value
- $L_{j}$: $j^{th}$ inductor value
- $C_{j}$: $j^{th}$ capacitor value
- $D$: Duty ratio
- $f$: PWM’s switching frequency
- $T$: PWM’s switching period
- $V_{s}$: Input source’s voltage

**References**

Axelrod B, Berkovich Y, and Ioinovici A (2008). Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC-DC PWM converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 55(2): 687-696.
Choi S, Agelidis V G, Yang J, Coutelier D, and Marabees P (2011). Analysis, design and experimental results of a floating-output interleaved-input boost-derived DC-DC high-gain transformer-less converter. IET Power Electronics, 4(1): 166-180.

Danandeh A, Seyedi H, and Babaei F (2012). Islanding detection using combined algorithm based on rate of change of reactive power and current THD techniques. In the Asia-Pacific Power and Energy Engineering Conference (APPEEC’12), IEEE, Shanghai, China: 1-4. https://doi.org/10.1109/APPEEC.2012.6307465

Evran F and Aydemir M T (2013). Z-source-based isolated high step-up converter. IET Power Electronics, 6(1): 117-124.

Fardoun AA and Ismail EH (2010). Ultra step-up DC-DC converter with reduced switch stress. IEEE Transactions on Industry Applications, 46(5): 2025-2034.

Hsieh YP, Chen JF, Liang TJ, and Yang LS (2013). Novel high step-up dc–dc converter for distributed generation system. IEEE Transactions on Industrial Electronics, 60(4): 1473-1482.

Hwu KI and Yau YT (2012). High step-up converter based on charge pump and boost converter. IEEE Transactions on Power Electron, 27(5): 2494-2494.

Ismail EH, Al-Saffar MA, and Sabzali AJ (2008a). High conversion ratio DC-DC converters with reduced switch stress. IEEE Transactions on Circuits and Systems I: Regular Papers, 55(7): 2139-2151.

Ismail EH, Al-Saffar MA, Sabzali AJ, and Fardoun AA (2008b). A family of single switch PWM converters with high step-up conversion ratio. IEEE Transactions on Circuits and Systems I: Regular Papers, 55(4): 1159-1171.

Jang YT and Jovanovic MM (2007). Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end. IEEE Transactions on Power Electronics, 22(4): 1394-1401.

Jiao Y, Luo FL, and Zhu M (2011). Voltage-lift-type switched-inductor cells for enhancing DC-DC boost ability: Principles and integrations in Luo converter. IET Power Electronics, 4(1): 131-142.

Leyva-Ramos J, Lopez-Cruz JM, Ortiz-Lopez MG, and Diaz-Saldivia LH (2013). Switching regulator using a high step-up voltage converter for fuel-cell modules. IET Power Electronics, 6(8): 1626-1633.

Li K, Yin Z, Chung ISH, and Ioinovici A (2015). From a voltage divider to a voltage doubler for a large DC gain converter. In the 17th European Conference on Power Electronics and Applications (EPE’15), IEEE, Geneva, Switzerland: 1–8. https://doi.org/10.1109/EPE.2015.7309239

Luo F (2011). Investigation on split-capacitors applied in positive output super-lift Luo-Converters. In the Chinese Control and Decision Conference, IEEE, Mianyang, China: 2792-2797. https://doi.org/10.1109/CCDC.2011.5968686

Luo F and Ye H (2003). Positive output super-lift converters. IEEE Transactions on Power Electronics, 18(1): 105-113.

Maksimovic D (1989). Synthesis of PWM and quasi-resonant DC-to-DC power converters. Ph.D. Dissertation, California Institute of Technology, Pasadena, California.

Mohan N, Undeland T, and Robbins W (2003). Power electronics devices, converters application and design, John Wiley and Sons, New York, USA.

Prudente M, Pfitscher L, Emmendorfer G, Romaneli EF, and Gules R (2008). Voltage multiplier cells applied to non-isolated DC-DC converters. IEEE Transactions on Power Electronics, 23(2): 871-887.

Qian W, Cao D, Cintron-Rivera JG, Gebben M, Wey D, and Peng FZ (2012). A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count. IEEE Transactions on Industry Applications, 48(4): 1397-1406.

Rahimi AM and Emadi A (2009). Active damping in DC/DC power electronic converters: A novel method to overcome the problems of constant power loads. IEEE Transactions on Industrial Electronics, 56(5): 1428-1439.

Rosas-Caro JC, Mancilla-David F, MayoMaldonado JC, Gonzalez-Lopez JM, TorresEspinosa HL, and Valdez-Resendiz JE (2013). A transformer-less high-gain boost converter with input current ripple cancelation at a selectable duty cycle. IEEE Transactions on Industrial Electronics, 60(10): 4492-4499.

Wu TF, Lai YS, Hung JC, and Chen YM (2005). An improved boost converter with coupled inductors and buck-boost type of active clamp. In the 40th IAS Annual Meeting Conference Record of the Industry Applications, IEEE, Kowloon, Hong Kong, 1: 639-644. https://doi.org/10.1109/IAS.2005.1518374

Wu TF, Lai YS, Hung JC, and Chen YM (2008). Boost converter with coupled inductors and buck-boost type of active clamp. IEEE Transactions on Industrial Electronics, 55(1): 154-162.

Yang LS, Liang TJ, and Chen JF (2009). Transformerless DC-DC converters with high step-up voltage gain. IEEE Transactions on Industrial Electronics, 56(8): 3144-3152.