Simulation of Total Ionizing Dose (TID) Effects Mitigation Technique for 22 nm Fully-Depleted Silicon-on-Insulator (FDSOI) Transistor

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ABSTRACT

Based on 22 nm ultrathin-body fully depleted silicon-on-insulator (UTB-FDSOI) transistors, we propose a novel structure of buried insulator layer aiming at total ionizing dose (TID) effects mitigation. Using technology computer-aided design (TCAD) tools, we focus on the influences of UTB-FDSOI devices with different structures and parameters on TID effects, such as buried oxide (BOX) layer thickness, buried Si\textsubscript{3}N\textsubscript{4} layer, and electron traps. First, we construct four types of UTB-FDSOI N-type metal-oxide-semiconductor (NMOS) devices numerically, in which the novel device features a buried silicon-oxide-nitride-oxide-silicon (SONOS) structure. Then, the transfer characteristics and trapped charge distribution of these devices are studied under different irradiation doses. It is known that a thinner BOX layer could lead to slighter TID effects, and the buried nitride layer and the electron traps could reduce the TID-induced leakage current (I\textsubscript{off}). Employing these optimization structures for TID effects hardness, the innovative transistor shows much better resistance against TID effects compared to the conventional FDSOI transistors. In addition, the threshold voltage of the novel device could be increased by applying appropriate bias conditions, similar to those of programming SONOS memory, so that the I\textsubscript{off} caused by TID irradiation further decreases. These results provide useful guidance for designers to achieve TID effects mitigation of SOI devices.

INDEX TERMS

TID effect, UTB-FDSOI, mitigation, TCAD.

I. INTRODUCTION

Due to the excellent control ability of the short-channel effect, the ultrathin-body fully depleted silicon-on-insulator (UTB-FDSOI) technology is recognized as one of the preferred solutions for nanoscale complementary metal-oxide-semiconductor (CMOS) processes [1]–[3]. Compared with the conventional bulk and partially depleted SOI (PDSOI) MOS devices, UTB-FDSOI transistors show better resistance to single event effects (SEE) due to less sensitive volume [4], [5] and good gate control that provides better electrical properties. Hence, UTB-FDSOI technology is suitable for semiconductor chips with higher performance and higher integration aiming at applications in harsh space environments.

However, there are a large number of cosmic rays, solar electromagnetic radiation, and high-energy charged particles in the space irradiation environment, which have significant impacts on the performance and reliability of electronic devices. In particular, the total ionizing dose (TID) effects can lead to off-state current (I\textsubscript{off}) increase, threshold voltage (V\textsubscript{th}) shift, and reliability degradation [6]–[8]. Therefore, to ensure the long-life and reliable operation of spacecrafts, it is necessary to improve the anti-TID performance of semiconductor devices used in space.

In recent years, many scholars have conducted extensive research on the TID effects of nanoscale electronic devices, including 28 nm bulk transistors, 28 nm FD-SOI transistors,
and 20 nm UTB-FDSOI devices [8]–[11]. Different from conventional planar bulk devices, SOI devices feature an insulating buried oxide (BOX) layer. The TID-induced net trapped positive charge in the BOX layer can cause the inversion of the back-gate channel in N-type transistors, leading to a serious static leakage current. Many mitigation techniques have been proposed to resolve this TID issue [12]–[15]. Marc et al. utilized the Ω-shaped gate structure to achieve efficient electrostatic control of the potential in the device so that it was naturally tolerant to a significant total dose exposure [12]. However, the process of manufacturing Ω-shaped devices is complex and expensive. J. S. Bi et al. constructed a body-under-source (BUS) N-channel device to avoid the formation of back-channel between the source and drain, which is caused by the trapped charge in the BOX layer [14]. For BUS transistors, the source and drain are not interchangeable, which limits the design of the circuit function. These technologies have limitations when used for a complex circuit. Hence, new optimization methods for TID effects hardening need to be proposed.

In this work, we propose a novel structure of UTB-FDSOI device that can be hard to TID irradiation, while maintaining the single-event-transient hardness levels intrinsic to ultra-thin-film SOI technology [4]. We focus on the influences of the buried Si$_3$N$_4$ layer, electron traps, and BOX layer thickness on TID responses of the device through Synopsys Sentaurus technology computer-aided design (TCAD) tools [16]. Three types of UTB-FDSOI devices are set as controls to analyze the excellent anti-TID performance in the innovative device. Moreover, after irradiation, the electrical properties of the novel device, which is programmed by an appropriate bias condition, are investigated, and the related mechanisms are discussed in detail.

II. SIMULATION SETUP

A. SIMULATION THEORY

Two-dimensional (2D) numerical simulations are performed using the Sentaurus Synopsys framework. Physical models, such as nonlocal tunneling, Shockley-Read-Hall (SRH) generation and recombination, radiation, nonlocal barrier tunnelling, and Fermi statistics, are utilized. The quantum effect in the short channel is considered for calibration [4]. The carrier barrier tunnelling masses are zero in the default model, which should be calibrated, whose values are easily found in the Sentaurus application library and other work [16], [20]. The generation of electron-hole (e-h) pairs due to radiation ($G_r$) in Sentaurus is described by (1) and (2) [16].

$$G_r = g_0 D \cdot Y(F)$$

(1)

$$Y(F) = \left(\frac{F + E_0}{F + E_1}\right)^m$$

(2)

where $D$ is the dose rate, $E_0$, $E_1$, and $m$ are constants, $g_0$ is the generation rate of e-h pairs, $F$ is the electric field, and $G_r$ is derived as a linear function of the dose rate. $E_0$, $E_1$, $m$, and $g_0$ are set to 0.1, 1.35 $\times$ 10$^6$, 0.9, and 7.6 $\times$ 10$^{12}$, respectively, which are shown in Sentaurus user guide. The basic radiation mechanisms in SiO$_2$ are depicted in Fig. 1 [17]. The e-h pairs are created during irradiation. Once generated, some e-h pairs can escape the initial recombination process by the electric field. It is generally believed that electrons, which have a much higher mobility than holes in the oxide, are rapidly swept out of the dielectric [18]. The excess holes will undergo polaronic hopping transport through shallow traps in the SiO$_2$. A fraction of these holes may drop into deep traps in the oxide bulk or near the oxide/silicon interface to form a net positive trapped charge. The hole traps may exchange charge with the underlying Si via electron tunneling [19]. Reactions between holes and hydrogen-containing defects or dopant complexes can lead to an interface trap. It means that the higher the $F$ and total irradiation dose, the more trapped charge produced by irradiation.

However, for Si$_3$N$_4$, lots of TID-induced electrons are captured by a large number of electron traps to generate the net negative trapped charge [20]. Additionally, the density and influence of the trapped charge are demonstrated by solving Poisson and drift-diffusion equations during simulations.

B. DEVICE STRUCTURE

2D architectures of the four types of UTB-FDSOI N-type metal-oxide-semiconductor (NMOS) constructed in the TCAD tools are shown in Fig. 2. Device D shows the proposed novel transistor structure. These devices are all based on 22 nm process nodes. The intrinsic channel is used to avoid random distribution of channel impurities, reducing impurity scattering to improve the carrier mobility [21]. The gate length is 22 nm, and the equivalent oxide thickness (EOT) is 8 Å. A 6 nm silicon layer is just above the BOX layer, and the spacer width is 10 nm. The BOX layers of devices A and B are 25 nm SiO$_2$ ($T_{AB}$) and 35 nm SiO$_2$ ($T_{BB}$), respectively. Devices C and D both have a silicon-oxide-nitride-oxide-silicon (SONOS) structure, where a 10 nm Si$_3$N$_4$ film ($T_S$) is sandwiched between the upper 5 nm SiO$_2$ ($T_I$) and the lower 20 nm SiO$_2$ layer ($T_L$). The Si$_3$N$_4$ in device D is rich in electron traps while the nitride in device C is set as an ideal insulator layer without electron traps. To reduce the series resistance of the source and drain, the
FIGURE 2. Cross-section schematics of devices (a) A, (b) B, (c) C and (d) D. The only difference between device A and device B is the BOX layer thickness. $T_{AB} = 25$ nm, $T_{BB} = 35$ nm. Devices B, C and D have the same buried insulator thickness whereas in devices C and D, a 10 nm Si$_3$N$_4$ is sandwiched between the upper 5 nm SiO$_2$ ($T_U$) and the lower 20 nm SiO$_2$ layer ($T_L$). The Si$_3$N$_4$ in device D is rich in electron traps while the nitride in device C is set as an ideal insulator layer without electron traps. Other parameters match those found in Table 1.

local epitaxial process is adopted in the source and drain region. The height of the source and drain ($H_{SD}$) is 21 nm. The substrate doping concentration is $1 \times 10^{18}$ cm$^{-3}$, which can restrain the short-channel effect like drain-induced-barrier-lowering (DIBL) [22]. The detailed geometry parameters for the four types of UTB-FDSOI NMOS are listed in Table 1.

TABLE 1. Structure parameters of UTB-FDSOI devices in Figure 2.

| Parameter | Values |
|-----------|--------|
| Equivalent oxide thickness (EOT) | 8 Å |
| Gate length ($L_g$) | 22 nm |
| BOX thickness in device A ($T_{AB}$) | 25 nm |
| BOX thickness in device B ($T_{BB}$) | 35 nm |
| Upper SiO$_2$ thickness ($T_U$) | 5 nm |
| Lower SiO$_2$ thickness ($T_L$) | 20 nm |
| Sandwiched Si$_3$N$_4$ thickness ($T_S$) | 10 nm |
| Channel doping | Intrinsic |
| Source and drain doping ($A_S$) | $1 \times 10^{20}$ cm$^{-3}$ |
| Substrate doping ($B$) | $1 \times 10^{19}$ cm$^{-3}$ |
| Channel thickness ($T_C$) | 6 nm |
| Source and drain height ($H_{SD}$) | 21 nm |
| Spacer width ($W_{spac}$) | 10 nm |

C. SIMULATION METHODOLOGY

Neutral electron traps are not setup in the ideal Si$_3$N$_4$ layer of device C, while those in the Si$_3$N$_4$ of device D are set up with a density of $1 \times 10^{19}$ cm$^{-3}$ [23], [24] and with an energy level of 1 eV lower than the conduction band [25]. Simulations of $\gamma$-ray irradiation with 0, 200 k, 500 k, 1 M and 10 M-rad(Si) doses are carried out on the four types of devices in the TID experiments. During the simulations, $V_{gs} = 0$ V and $V_{ds} = 1$ V are applied, which is off-state for N-channel transistor. The transfer characteristics, distribution of electric field, and distribution of trapped charges are investigated using fixed $V_{ds}$ of 0.1 V under different radiation doses. The transfer characteristics and leakage current are used to evaluate the TID effects of the device in the present work.

After 10 Mrad(Si) irradiation, the substrate electrode of device D is applied a pulse with different durations up to 7.5 $\mu$s and the same amplitude of 15 V, which is similar to the programming in SONOS devices [26], [27]. The I-V characteristics and distribution of trapped charge of device D are obtained with respect to different pulse durations.

III. RESULTS AND DISCUSSION

A. THE INFLUENCE OF THE BOX THICKNESS

Fig. 3 shows the leakage current of devices A and B with $V_{ds} = 0.1$ V and $V_{gs} = 0$ V for accumulative radiation dose up to 10 Mrad(Si). As can be obtained from the figure, a thicker BOX layer leads to a higher TID-induced off-state current. With the increase of radiation dose to 1 Mrad(Si), the leakage current of device B increases more obviously. The ratios of the $I_{off}$ growth among multiple of devices A and B at 200 k, 500 k and 1 M-rad(Si) are 2.67, 2.96, and 2.95, respectively, which are bigger than 1. However, the $I_{off}$ values of both devices under 10 Mrad(Si) radiation are almost the same and close to the saturation current, which means the circuit functions can be seriously affected.

For planar SOI devices, the $V_t$ shift ($\Delta V_t$) caused by TID effects is extracted in (3) and (4) [28].

$$\Delta V_t = \Delta V_{ot} + \Delta V_{it}$$

$$\Delta V_{ot,it} = -\frac{1}{C_{ox}t_{ox}} \int_{0}^{t_{ox}} \rho_{ot,it}(x) dx$$

where $\rho_{ot,it}(x)$ is a charge distribution of the radiation-induced oxide-trapped or interface-trapped charge, $C_{ox}$ is the oxide capacitance, and $t_{ox}$ is the oxide thickness. According to (3) and (4), the positive trapped charge caused by TID effects, accumulates in the BOX film, namely $\rho_{ot,it}(x) > 0$, results in a negative shift of $V_t$ in the back-gate, which
FIGURE 4. The distribution of the positive trapped charge in devices A and B after 200 krad(Si) and 500 krad(Si) TID irradiation. The curves with smaller values are obtained after 200 krad(Si) radiation while the curves with larger values are illustrated after 500 krad(Si) radiation.

leads to a similar drift in the front gate through the intergate coupling effect [29]. Fig. 4 presents the distribution of the TID-induced positive trapped charge in devices A and B after 200 krad(Si) and 500 krad(Si) TID irradiation. The concentration of the trapped charge increases with the total dose so that the $V_t$ shift and leakage current increase. It can be known from (3), (4), and Fig. 4 that the $V_t$ shift is positively correlated with the thickness of the BOX layer, which is consistent with previous publications [30]. Hence, the anti-TID radiation performance of SOI devices can be improved by using ultra-thin BOX layers. It is easy to speculate that when the irradiation dose is very large, for example, when the dose is more than 1 Mrad(Si), the trapped charge in the BOX layer is saturated, namely the $\rho_{ot}(x)$ growth becomes slow, so that the increase of leakage current becomes smaller, which leads to the hump in leakage current at about 1M rad(Si) radiation and leakage saturation at about 10 Mrad(Si).

FIGURE 5. The pre- and post-TID radiation transfer characteristics in devices A and C. When simulating irradiation, the bias is set as $V_{gs} = 0$ V and $V_{ds} = 1$ V. When extracting the transfer characteristics, the gate voltage is scanned from 0 V to 1 V fixed $V_{ds} = 0.1$ V.

B. THE IMPACT OF THE BURIED Si$_3$N$_4$ LAYER
The pre- and post-TID irradiation transfer characteristics of devices A and C with $V_{ds} = 0.1$ V are depicted in Fig. 5. The total physical thickness of the SiO$_2$ in device C is the same as that in device A, but an ideal Si$_3$N$_4$ without neutral traps is sandwiched between the 5 nm SiO$_2$ and 20 nm SiO$_2$ layers in device C. Before irradiation, the off-state current in device C is slightly higher than that of device A, which is similar to device B. With the increase of radiation dose, the $I_{off}$ values of both devices increase exponentially. After 1 Mrad(Si) radiation, the leakage current of device C increases only 43 times, while device A, with the $I_{off}/I_{on}$ ratio of $10^2$, almost loses switching performance. The growth of $I_{off}$ in device C is much smaller than that in device A. Thus, the higher the radiation dose, the larger the $I_{off}$ difference between devices A and C.

The distribution of trapped charge and electric field in devices A and C with $V_{ds} = 0.1$ V is shown in Fig. 6 after a dose of 500 krad(Si) radiation. The buried insulator layer in device C is thicker compared with device A, so that the electric field in the 20 nm SiO$_2$ is lower than that in device A under the same bias condition. Due to lower electric field strength, fewer carriers caused by TID radiation are generated. Fig. 7 presents the band diagram of device C with $V_{ds} = 1$ V. Because of the barrier between Si$_3$N$_4$ and SiO$_2$, most of the TID-induced electrons, which are not swept out, recombine with holes in the lower 20 nm BOX layer of device C. Hence, there are fewer trapped charges in the BOX layer of device C, as depicted in the lower part of Fig. 6. It is worth noting that, for device C, the hole trapped charge is mainly distributed in the upper 5 nm SiO$_2$ layer. Therefore, the thin upper SiO$_2$ film plays a key role in TID effects. According to (3) and (4), the TID-induced back-gate $V_t$ shift of device C is much smaller than that of device A, meaning that the resistance against TID effects can be greatly improved by sandwiching an insulating layer into the BOX layer. As analyzed above, for stacked BOX later structures, the thinner the upper SiO$_2$, the better the improvement.

C. THE INFLUENCE OF ELECTRON TRAPS
The structure of device D, in which the Si$_3$N$_4$ layer is rich in neutral electron traps, is similar to that of device C. Fig. 8 shows the pre- and post-TID radiation transfer characteristics in devices C and D with $V_{ds} = 0.1$ V. The leakage current...
is $5.15 \times 10^{-9} \text{A}$ in device D and is almost unchanged after 1 Mrad(Si) irradiation. After a dose of 10 Mrad(Si), the $I_{\text{off}}$ of device D is still an order of magnitude lower than that of device C, indicating that device D shows better TID effects hardness.

Fig. 9 presents the distribution of the trapped charge in devices C and D after 1 Mrad(Si) dose irradiation. As mentioned above, the neutral electron traps in the Si$_3$N$_4$ can capture the radiation-induced electrons to form the net negative trapped charge. Contrasting with device C, a large amount of negative trapped charges generated in device D can counteract the effect of the positive trapped charge in the SiO$_2$ referring to (3) and (4). Hence, much better anti-TID properties can be obtained in the FDSOI device with electron traps in the sandwiched layer.

D. THE IMPACT OF BURIED SONOS LAYER PROGRAMMING

Fig. 10 depicts the equivalent circuit diagram of the device D structure, which can be illustrated as a parallel connection of an NMOS transistor and a SONOS transistor. Utilizing the tunneling model of the thin oxide layer and the electron traps of the Si$_3$N$_4$ layer, the SONOS device can be programmed to make the electron traps capture tunneling electrons to form negative trapped charges, resulting in the $V_t$ change in device D due to the inter-gate coupling effect [21], [24]. As depicted in Fig. 11, device D is programmed after 10 Mrad(Si) dose radiation. The pulse amplitude is 15 V with pulse duration ($t_p$) up to 7.5 $\mu$s. The transfer characteristics of device D are shown in Fig. 11 after 10 Mrad(Si) irradiation under different $t_p$. Before programming, namely $t_p = 0$, the leakage current ($I_{\text{off}}$) is $2.89 \times 10^{-6}$ A with $V_t = 188$ mV. As the $t_p$ increases to 2.5 $\mu$s, the on-state current of the device is still saturated with $V_t = 363$ mV, and the $I_{\text{off}}$ decreases to $7.26 \times 10^{-8}$ A, which is close to the pre-radiation value. However, under $t_p = 5 \mu$s, the $I_{\text{on}}$ and $I_{\text{off}}$ decrease simultaneously, and the $V_t$ increases to 418 mV. When $t_p$ is up to 7.5 $\mu$s, the transfer characteristic is the same as that under $t_p = 5 \mu$s.

The distribution of the trapped charge in device D after 10 Mrad(Si) irradiation under different $t_p$ is depicted in Fig. 12. Fig. 13 shows the contour of electron density in device D. With the increase of $t_p$, electron traps capture a large number of tunneling electrons so that the amount of
FIGURE 11. The transfer characteristics of device D after a dose of 10 Mrad(Si) under different pulse durations. The transfer curves after 10 Mrad(Si) radiation are extracted by scanning gate voltage from 0 V to 1 V fixed-$V_{ds} = 0.1$ V. Before programming, the $V_t$ of device D after irradiation is 188 mV, which can be improved to 418 mV due to program.

FIGURE 12. The distribution of the trapped charge in device D after 10 Mrad(Si) dose irradiation under different pulse durations. Net negative trapped charge in the Si$_3$N$_4$ layer increases, as illustrated in Fig. 12. At the same time, the distribution of electrons in the nitride becomes denser while that in the channel is sparser, as shown in Fig. 13. The ability of traps to capture electrons is saturated when $t_p > 5 \mu s$, causing the concentration of negative trapped charge and density of the channel electron to remain the same. By increasing the programming voltage without breaking down the device, it may be possible for the Si$_3$N$_4$ layer to capture more electrons to increase the change window of the $V_t$.

The leakage currents under different total doses and $t_p$ are listed in Table 2. As for the Table 2, it can be obtained that the proposed device, namely device D, has the lowest off-state current compared with other devices under the same irradiation dose, and the higher the radiation dose, the greater the leakage current difference. By programming the buried insulator layer in device D, the anti-TID performance of the device can be further enhanced. In addition, the change of $V_t$ caused by programming gives the device the potential to convert in fast device with low $V_t$ and low power device with high $V_t$.

IV. CONCLUSION

In this work, we propose a novel device with a buried SONOS structure aiming at TID effects mitigation. The influences of the BOX thickness, sandwiched Si$_3$N$_4$, electron traps, and buried insulator layer programming on TID responses, are investigated. The thinner BOX layer, buried Si$_3$N$_4$ film, and electron traps can enhance the resistance of the device against TID effects. Table 3 summarizes TID-induced leakage current in different devices, showing that the innovative device we proposed with optimization structures, which are designed for TID effects hardness, has much better anti-TID effects compared with the conventional devices. Programming the
buried insulator layer can increase the $V_{T}$, which reduces the $I_{off}$ caused by TID radiation. The innovative device shows the potential to convert in fast device and low power device. These results are useful to designers for TID effects mitigation and for designing circuit function.

For the future human tasks of exploring deep space for a long time, the current TID damage of FDSOI-technology-based devices is cumulative and irreversible. On the basis of the novel structure in this paper, we can optimize in real-time to operate suitable pulses on buried SONOS programming, so that the function and performance of the circuit can be restored. Thus, this work is of great guiding significance for the improvement of the survivability of the spacecraft to explore deep space for a long time.

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