Towards a Uniform Architecture for the Efficient Implementation of 2D and 3D Deconvolutional Neural Networks on FPGAs

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Abstract—Three-dimensional deconvolution is widely used in many computer vision applications. However, most previous works have only focused on accelerating 2D deconvolutional neural networks (DCNNs) on FPGAs, while the acceleration of 3D DCNNs has not been studied in depth as they have higher computational complexity and sparsity than 2D DCNNs. In this paper, we focus on the acceleration of both 2D and 3D DCNNs on FPGAs by proposing efficient schemes for mapping 2D and 3D DCNNs on a uniform architecture. By implementing our design on the Xilinx VC709 platform for four real-life 2D and 3D DCNNs, we can achieve up to 3.0 TOPS with high hardware efficiency. Comparisons with CPU and GPU solutions demonstrate that we can achieve an improvement of up to 63.3\times in throughput relative to a CPU solution and an improvement of up to 8.3\times in energy efficiency compared to a GPU solution.

I. INTRODUCTION

Recently, deconvolution has become widely used in the fields of computer vision, such as semantic segmentation\textsuperscript{[1]}, generative models\textsuperscript{[2]}, and high-resolution imaging\textsuperscript{[3]}. Because 3D images exist in most medical data used in clinical practice\textsuperscript{[4]}, 3D deconvolution has proven to be a better method than 2D deconvolution in some applications. Although the computational patterns of 2D and 3D deconvolutions are very similar, the computational complexity and memory requirements of 3D deconvolution are much higher than in 2D deconvolution, making it challenging to design efficient accelerators for them. In addition, deconvolution must insert ‘zero’ into the input image before implementing convolution operations, leading to the sparsity of the input image as well as the introduction of invalid operations (i.e., multiplications of zero). According to our study, the sparsity of the input features of 3D deconvolutional layers is higher than that of 2D deconvolutional layers. As shown in Fig. 1, the sparsity of the deconvolutional layers in an example of 3D deconvolutional neural networks (DCNNs) (i.e., 3D-GAN\textsuperscript{[5]}) is clearly higher than for 2D DCNNs (i.e., DCGAN\textsuperscript{[2]}). Therefore, the sparsity contributes to the processing engine (PE) workload imbalance\textsuperscript{[6]}. Many studies\textsuperscript{[7,9]} have primarily focused on accelerating convolutional neural networks (CNNs) on Field-Programmable Gate Arrays (FPGAs), due to the beneficial high performance and energy efficiency of FPGAs. However, to the best of our knowledge, not much attention has been given to accelerate DCNNs, especially in 3D deconvolution. Given the similarity in the computational patterns of 2D and 3D deconvolutions, this work focuses on accelerating both of them on FPGA with a uniform architecture. The contributions of this work are summarized as follows:

1) We propose a uniform architecture for efficient implementation of 2D and 3D DCNNs on FPGA.
2) We propose a mapping scheme of 2D and 3D DCNNs on the uniform architecture, which can efficiently improve the parallel computational ability and computational efficiency of the accelerator.
3) As a case study, we implement our design on an Xilinx VC709 board for four state-of-the-art 2D and 3D DCNNs: DCGAN, GP-GAN\textsuperscript{[10]}, V-NET\textsuperscript{[4]} and 3D-GAN. Experimental results show that our implementation achieves an improvement of up to 63.3\times and 291.4\times in throughput and energy efficiency relative to CPU, and a 8.3\times energy efficiency gain over GPU.

II. RELATED WORK

Few works have focused on accelerating deconvolutions\textsuperscript{[6,11,12]}. In\textsuperscript{[11,12]}, the researchers addressed the accelerations of the deconvolution in generative adversarial networks (GANs). Yazdanbakhsh et al.\textsuperscript{[11]} introduced a new architecture to alleviate the sources of inefficiency associated with the acceleration of GANs using conventional convolution accelerators by reorganizing the output computations. In\textsuperscript{[12]}, an end-to-end solution was devised to generate an optimized synthesizable FPGA accelerator from a high-level GAN specification, alleviating the challenges of inefficiency and resources underutilization faced by conventional convolutional accelerators. Yan et al.\textsuperscript{[6]} proposed a novel mapping method.
Deconvolution is similar to convolution operations, and the fundamental difference between them is that the original input feature maps of deconvolution requires the insertion of ‘zero’ between the original input activations. Fig. 3 shows the process of 2D and 3D deconvolutions.

As Fig. 3 (a) illustrates, for 2D deconvolution, the original input map is inserted with ‘zero’ shown in white between the original input activations colored in gray. A $K 	imes K$ kernel then performs convolutions with the inserted feature map to generate an $R' 	imes C'$ output map. Observed from Fig. 3 (b), the process of 3D deconvolution is similar to that of 2D deconvolution. The original image is first inserted with ‘zero’ between the rows and columns of the 2D data tiles, which is identical to 2D deconvolution. In addition, it is also necessary to insert ‘zero’ planes (i.e., the M1 plane) between every two 2D planes (i.e., the M2 plane) and a $K 	imes K 	imes K$ kernel then performs convolutions with the inserted feature map to generate an $R' 	imes C' 	imes Z'$ output map.

III. BACKGROUND

The computation engine is the most important component of our accelerator, which consists of a $T_m$ group of PEs. In each group, the PEs are organized as a 3D mesh architecture, which contains $T_z 	imes T_c$ 2D PE planes. In this work, we regard the PE plane as a PE array with $T_z 	imes T_c$ PEs. All PEs have direct connections to the input buffer, while only the leftmost PEs in each row have access to the weight buffer. The leftmost PEs in each row are responsible for collecting the results of the PEs of the same row and then deliver them to the following adder trees. The adder trees handle the additions of the results belonging to different feature maps. $T_m 	imes T_c 	imes T_z \times \log_2 T_n$ adders are integrated in the adder trees to support a higher degree of parallelism.

The architecture of the PE is presented in the right part of Fig. 2. It consists of two register files (i.e., $Ra$ and $Rw$) to buffer the input activations and weights. In addition, three Overlap First-In-First-Outs (FIFOs) (i.e., FIFO-Vs, FIFO-Hs and FIFO-Ds) are designed to deliver the overlaps in the results data from the adjacent PEs. The products yielded by the multipliers are conditionally added with the data from the Overlap FIFOs. Once the current results are determined to be overlaps, they will be sent to the Overlap FIFOs of adjacent PEs, waiting to be added. Otherwise, they will be sent to the local Result FIFOs. The results in the local FIFO of the current PE will be sent to the left PE once they have stored all the local results.

IV. THE PROPOSED ARCHITECTURE

A. Architecture Overview

Fig. 2 presents an overview of our proposed architecture for accelerating 2D and 3D deconvolutions. The accelerator consists of a memory controller, three types of on-chip buffers, a kernel computation engine, and the adder trees. Due to limited amount of on-chip memory of FPGAs, the source data and final results are stored in the off-chip rate memory (i.e., the DDR). The memory controller is used for fetching the input feature maps and weights from the DDR to the on-chip buffers, and storing the results into the DDR when they are available. In addition, one output feature map needs $N_c$ (i.e., input channels) input feature maps, due to the limited on-chip memory, it is difficult to cache all the input data needed for one feature map on chip. Hence, we use blocking to resolve this issue. We adopt three separate on-chip buffers to store input, output and weight blocks.
We divide the dataflow in the PE arrays into three steps:

1. **Loading activations and weights**: Input blocks and weight blocks are firstly fetched into the input and weight buffers, activations and weights are loaded into the leftmost PEs in the 3D PE mesh from the input buffers and weight buffers. When the next column’s PEs are empty, the next group of activations are loaded into the next column’s PEs in the next cycle. The activations in each PE are multiplied by all the weights of the corresponding kernels. The weights are also loaded into the leftmost PEs at the beginning of the process. When the weights are multiplied by activations in PEs, the weights are also sent to the next column’s PEs. The same column’s PEs shares the weights.

2. **Computing**: After the activations and weights are loaded into the PEs, they are immediately sent to the multiplier to yield the products in each PE. The results are then sent to the FIFOs. If the results overlap, they are sent to Overlap FIFOs, else sent to Output FIFOs. Each PE performs $K \times K \times K$ multiplications to produce an output block. When th PEs process the overlapped part of the output blocks, the PEs load the overlapped elements from their FIFOs, and perform additions. When the computation process in the direction of input channels (i.e., $T_n$) is complete, $T_n$ results are accumulated by the adder trees.

3. **Writing Back**: When all the activations of the input blocks are complete and the overlaps are accumulated, the results, i.e., the output feature map is transferred to the output buffers. The results are accumulated until the input channels are complete, and the final outputs of output feature maps are then transferred to the external memory.

To explain this concept in more detail, we illustrate the dataflow of the PE arrays after applying the 3D IOM method on the architecture in Fig. 4. For the sake of simplicity, Fig. 4 only shows the dataflow in a PE array, and the dataflow in other PE arrays are analogous. Table II lists the definitions used in the explanation of the dataflow. At stage 0, the activations $I(0,0,0,0) \sim I(2,0,0,0)$ and weights $W(0,0,0,0,0)$ are sent separately to the leftmost columns of the PEs in the PE array, i.e. $PE_{0,0}^0 \sim PE_{2,0}^0$, and they are multiplied. The overlaps produced from $PE_{1,0}^0 \sim PE_{2,0}^0$ is sent to their FIFO-Vs. At stage 1, activations $I(0,1,0,0) \sim I(2,1,0,0)$ are loaded into $PE_{0,1}^0 \sim PE_{2,1}^0$. $W(0,0,0,0,0)$ are moved to $PE_{0,0}^1 \sim PE_{2,1}^1$, and they are then multiplied by the activations $I(0,1,0,0) \sim I(2,1,1,0,0)$. Meanwhile, $PE_{0,0}^0 \sim PE_{2,0}^0$ performs the multiplication by $W(0,1,0,0,0)$. The
TABLE I

| Parameter | Description |
|-----------|-------------|
| \(W_{1,1}(i_j,k_j,d_j,l_j)\) | input activation from the \(i_j, k_j, d_j, l_j\) input channel |
| \(W_{1,2}(i_j,k_j,d_j,l_j)\) | weight from the \(i_j, k_j, d_j, l_j\) channel of the \(o_{z, t}\) filter |
| \(W_{1,3}(i_j,k_j,d_j,l_j)\) | weight from the \(i_j, k_j, d_j, l_j\) channel of the \(o_{z, t}\) filter |

overlaps produced by \(PE_{0,1}^{1}\) to \(PE_{0,1}^{2}\) are then sent to their FIFO-Hs, and the overlaps produced by \(PE_{0,1}^{1}\) to \(PE_{0,1}^{2}\) are sent to their FIFO-Vs. At stage 2, activations \(I(0,2,0,0)\) to \(I(2,2,0,0)\) are loaded into \(PE_{0,2}^{0}\) to \(PE_{0,2}^{2}\). In the meantime, \(W(0,0,0,0,0)\) and \(W(1,0,0,0,0)\) are moved to \(PE_{0,2}^{0}\) to \(PE_{2,2}^{0}\) and \(PE_{0,1}^{1}\) to \(PE_{2,1}^{1}\), and then multiplied by the corresponding activations. The overlaps produced by \(PE_{0,2}^{0}\) to \(PE_{2,2}^{0}\) are sent to their FIFO-Hs, and the overlaps produced by \(PE_{0,1}^{1}\) to \(PE_{2,1}^{1}\) are sent to their FIFO-Vs.

C. Support for The Accelerations of 2D and 3D DCNNs

Our architecture is able to support the acceleration of both 2D and 3D DCNNs. For 3D DCNNs, \(T_n\) PE arrays are used for the computations of an input feature map. In this way, \(T_n \times T_z\) PE arrays can accelerate the computation of \(T_n\) input feature maps simultaneously. For 2D DCNNs, we map the computations of an input feature map onto a PE array. Since the input feature maps are two-dimensional, we can use \(T_n \times T_z\) PE arrays to compute \(T_n \times T_z\) input feature maps in the meantime, while maintaining the size of the PE arrays (i.e., \(T_r \times T_c\)). In this case, the FIFO-D in each PE is disabled since there is no dataflow between adjacent PE arrays. Note that the dataflow in the PE arrays are identical when mapping 2D and 3D DCNNs on the computation engine. Since few control logics are required for supporting both 2D and 3D DCNNs in each PE, we omit the architecture details in Fig. 2.

V. EXPERIMENTAL RESULTS

As a case study, we evaluate our design using four representative DCNN models: DCGAN, GP-GAN, 3D-GAN and V-Net. All the deconvolutional layers of the selected DCNNs have uniform 3 \(\times\) 3 and 3 \(\times\) 3 filters.

We quantitatively compare our FPGA implementation of 2D and 3D DCNNs with two other platforms: (1) a ten-core Intel E5 CPU (2.8 GHz) and (2) a NVIDIA GeForce GTX 1080 GPU. Our accelerator design is implemented on the Xilinx VC709 clocked at 200MHz, which contains a Virtex-7 690t FPGA and two 4GB DDR3 DRAMs.

Table II illustrates the configuration of the parameters of our benchmarks. Note that we use 16-bit fixed activations and weights for all the benchmarks in our experiment. To avoid the reconfiguration overhead, we use an accelerator with fixed configurations for all the benchmarks. We use \(T_m \times T_n \times T_z \times T_r \times T_c = 2,048\) PEs in total.

Table III reports the resource utilization of our accelerator. The Digital Signal Processors (DSPs) and Look-up Tables (LUTs) dominate the resource consumption, and mainly utilized for implementing multipliers and adders, respectively. Fig. 6 presents PE utilization about the accelerator. Note that the PE utilization is defined as the ratio of the computation time occupied in total time. For all benchmarks, our accelerator can achieve up to 90\% of PE utilization. It demonstrates

TABLE II

| Configurations of the computation engine. |
|-----------------------------------------|
| **Benchmarks** | **\(T_m\)** | **\(T_n\)** | **\(T_z\)** | **\(T_r\)** | **\(T_c\)** | **data width** |
|----------------|-------------|-------------|-------------|-------------|-------------|---------------|
| 2D DCNNs       | 2           | 64          | 1           | 4           | 4           | 16            |
| 3D DCNNs       | 2           | 16          | 4           | 4           | 4           | 16            |

TABLE III

| Resource utilization of Xilinx VC709. |
|--------------------------------------|
| **Resource** | **DSP48Es** | **BRAMs** | **Flip-Flops** | **LUTs** |
|----------------|-------------|------------|----------------|---------|
| Utilization    | 2304        | 712        | 566182         | 292292  |
| percentage(%)  | 64.00       | 48.44      | 65.34          | 67.48   |

Fig. 6. Results for 2D and 3D DCNNs: (a) the PE utilization; (b) throughput.

Fig. 7. Comparisons of CPU, GPU and FPGA solutions: (a) relative performance; (b) relative energy efficiency.

the effectiveness of our mapping and the uniform architecture for 2D and 3D deconvolutions. Note that the fourth layers of DCGAN and GP-GAN are bottlenecked by the memory access, which results in a reduction of PE utilization. In addition, it is also clear from Fig. 6 that we can achieve state-of-the-art performance (1.5TOPS~3.0TOPS) for all the benchmarks. Because the higher sparsity of 3D deconvolution and the large amount of data delivered between PEs, the performance of 3D deconvolution on FPGA outperforms that of 2D deconvolution.

For the benchmarks in our experiment, we compare our work with CPU and GPU, as shown in Fig. 7. The performance of our method on the accelerator outperforms that of the CPU by 22.7\% to 63.3\%. Concerning energy efficiency, our method outperforms the GPU by 104.7\% to 291.4\% and outperforms the GPU by 3.3\% to 8.3\%.

VI. CONCLUSION

In this paper, we proposed a 2D and 3D deconvolution accelerator based on a uniform architecture on FPGA. We employed a mapping scheme of 2D and 3D deconvolutions on this architecture. To the best of our knowledge, this is the first work to implement 2D and 3D DCNNs on FPGA. By exploring the data transference between adjacent PEs without invalid operations, our design achieves an acceleration of 63.3\% compared with CPU implementation, and an energy efficiency improvement of 8.3\% compared with designs running on a GTX 1080 GPU.
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