Design of a Strong-Arm Dynamic-Latch based comparator with high speed, low power and low offset for SAR-ADC

Sounak Dutta
Electronics and Telecommunication
Jadavpur University
Kolkata, India
sounak04@gmail.com

Abstract—Comparators are utilised by Nyquist-rate and oversampling analog to digital converters (ADCs) to accomplish quantization and perhaps sampling. Thus, comparators have a substantial effect on the speed and accuracy of ADCs. This study provides a revised design for a dynamic-latch-based comparator that achieves the lowest latency, maximum area-efficient realisation, reduced power dissipation, and low offset. The proposed circuit has been designed and simulated using Gdsp 45 nm standard CMOS-Process to operate on 100 MHz clock, at 1.2V supply voltage. Design and simulation have been carried out using CADENCE Virtuoso EDA tool. Compared to the original design, the PDP was easily reduced by approximately by 6% with offset voltage reduced by 8 mV without speed trade-off.

Keywords—Comparator; Dynamic Comparator; Latch; Delay; Low Power; Offset-voltage; SAR-ADC.

I. INTRODUCTION

Dynamic latched comparators are highly desirable for several applications, including high-speed analog-to-digital converters (SAR-ADCs) [1], memory sense amplifiers (SAs), and data receivers, owing to their high speed, low power consumption, high input impedance, and full-swing output. These days, dynamic comparators are widely being used because of their low-power consumption. Important design parameters for an ADC are fast speed, low offset, low power dissipation, and reduced chip area [2]. A comparator is a fundamental circuit that converts a signal from the analogue domain to the digital domain. It compares two voltage inputs and generates a binary signal indicating which one is greater. The output goes high if the non-inverting (+) input is higher than the inverting (-) input. The output goes low if the inverting input is higher than the non-inverting input. These days, dynamic comparators are widely being used because of their low-power consumption. In conventional dynamic latched comparators, a positive feedback mechanism (regenerative latch) is used which increases the speed of operation by instantly increasing a small-scale voltage difference at the input terminals to a full-scale digital level. In fact, in these comparators, usually there is no constant (current) path from the supply voltage to $V_{SS}$, and they are controlled by a clock signal [3],[4]. However, the accuracy of these comparators is restricted by an input-referred latch offset voltage arising from threshold voltage $V_{th}$, current factor $\beta = \mu C_{ox} (W/L)$, and parasitic node capacitance and output load capacitance mismatches [5, 6,7]. Utilizing the pre-amplifier before the regenerative output-latch stage will result in a reduced input-referred latch offset voltage and reduced kickback noise [8]. However, owing to ongoing technological scaling, the preamplifier-based comparators experience lower intrinsic gain with decreasing drain-to-source resistance $r_{ds}$ and high - power consumption for a large bandwidth [9].

Therefore, for low power application we prefer Strong-Arm Dynamic Latch based comparator [10]. In [10] the proposed Strong-Arm Dynamic Latch based comparator is modified from Charge Sharing Dynamic Latch Comparator [11] and another Strong-Arm Dynamic Latch based comparator [12] by providing lower power consumption than both [11] and [12], lower offset voltage and less delay than [11] and reduced real estate over the chip than [12]. Although [10] has significantly lower offset voltage than [11], still the offset voltage value is marginally on the higher side if we require accurate comparison without pre-stage amplifier.

In this paper, we proposed a modified Strong-Arm Dynamic Latch comparator for lower offset, lower delay and lower PDP value (Power-Delay product) and compared its performance with the topology of [10]. Section II discusses the technique and design parameters. Section III gives simulation results and compares the design to the referred design, and Section IV concludes the article.

II. METHODOLOGY & DESIGN PARAMETERS

A. Basic Operation: A comparator detects a differential input and produces a logical output based on the input difference's polarity.

The "Strong-Arm” comparator is made up of a regenerative latch pair added on top of a input clocked differential pair. As the cross-coupled latch pairs make strong positive feedback [10], it is able to make decisions quickly. The main advantage of Strong-Arm comparator is 1) it consumes zero static power, 2) it directly produces rail-to-rail outputs, and 3) its input-referred offset arises from primarily one differential pair, so the offset voltage value is also lower.

B. Design: The proposed design of Strong-Arm Dynamic Latch based Comparator is shown in Fig.1. The schematic of [10] has been upgraded to operate with lower offset voltage by connecting two extra pMOS, $S_1$ and $S_2$ which is acting as pre-charge switches [13]. These two pre-charge switches also help to reset the output faster than the reset time measured in [10]. This schematic also makes use of a single, suitably sized clocked nMOS as tail transistor throughout the evaluation.
stage, which slightly decreases the evaluation delay than that of [10].

Switches S1 and S2 serve two purposes: a) they eliminate the prior states at nodes P and Q, therefore reducing dynamic offsets; and b) they provide a starting voltage of \( V_{DD} \) at these nodes, so enabling amplification before \( M_1 \) and \( M_2 \) approach the triode area.

\[ \frac{\Delta V_0}{\Delta V_0} = \ln \left( \frac{V_{DD}}{2} \right) \]

\[ t_i = \frac{C_{load}}{I_{TTH}} \approx 2 \frac{V_{THP}}{C_{load}} \]  

(1)

In (1), for minimal input differential voltage \( \Delta V_{in} \), the drain current may be estimated as constant and it is equivalent to half the tail current. The second term \( t_{reg} \) represents the entire latching delay of two cross coupled inverters. It is estimated that the final output will be half of the supply rail \( \Delta V_{out} = V_{DD}/2 \) depending on \( \Delta V_0 \), the primary voltage differential \([10]\).

The equation for latch evaluation delay \( t_{reg} \) as given in \([15,16]\) is dependent on the primary voltage difference during the commencement of the regeneration phase.

\[ t_{reg} = \frac{C_{load}}{g_{m(eff)}} \ln \left( \frac{\Delta V_{out}}{\Delta V_0} \right) \approx \frac{C_{load}}{g_{m(eff)}} \ln \left( \frac{V_{DD}/2}{\Delta V_0} \right) \]  

(2)

In the above equation \( g_{m(eff)} \) is the effective transconductance of cross-coupled inverters \([12]\).

We know, \( \Delta V_0 = |V_{out}^+ - V_{out}^-|_{t=0} \). Now by using equation (1) we get,

\[ \Delta V_0 = \left| V_{THP} \right| - \frac{I_{D2} t_i}{C_{load}} \]  

(3)

2) Delay Analysis

The delay of the comparator consists of two components, \( t_i \) and \( t_{reg} \) (latch delay). The first term, \( t_i \), represents the time taken by the load capacitor to discharge until the first pMOS transistor becomes ON.

As described in \([10]\), if \( V_{in1} > V_{in2} \) transistors \( M_1 \) and \( M_2 \) discharge \( V_{out}^- \) and activate \( M_4 \). On this basis, the delay may be calculated as follows:
The difference in input current $ΔI_{in}$ between the two branches is considerably less than the individual currents $I_{D1}$ and $I_{D2}$, which can be equivalent to half of $I_{tail}$.

So, now (3) becomes,

$$ΔV_0 = |V_{THP}| \left( \frac{ΔI_{in}}{I_{D1}} \right) \approx 2. |V_{THP}| \left( \frac{ΔI_{in}}{I_{tail}} \right)$$

By solving this we get,

$$ΔV_0 = 2. |V_{THP}| \left( \frac{ΔI_{in}}{I_{tail}} \right) \sqrt{\frac{β_{12}}{I_{tail}}} ΔV_{in} \quad (4)$$

Here, $β_{12} = \mu C_{ox} (W/L)_{12}$ is the gain factor in $\frac{I}{V_d^2}$.

$β_{12}$ represents the input transistor's current factor. The tail current $I_{tail}$ is a function of the supply voltage and the input common mode voltage. By substituting $ΔV_0$ (from (4)) into (2) and the value of $t_1$ from (1), the total delay may be calculated as illustrated in (5).

$$t_{total} = t_1 + t_{reg}$$

$$t_{total} = 2. C_{load} \frac{V_{THP}}{I_{tail}} \frac{C_{load}}{g_{m(\text{eff})}} \ln \left( \frac{V_{DD}/2}{ΔV_{in}} \right) \quad (5)$$

Equation of (5) can be written as:

$$t_{total} = 2. C_{load} \frac{V_{THP}}{I_{tail}} \frac{C_{load}}{g_{m(\text{eff})}} \ln \left( \frac{V_{DD}/2}{2 |V_{THP}| \left( \frac{ΔI_{in}}{I_{tail}} \right) \sqrt{\frac{β_{12}}{I_{tail}}} ΔV_{in}} \right) \quad (6)$$

This is the total analytical delay of the proposed dynamic latch comparator. [10]

2) Power calculation

Basically, to determine the average power wasted from the supply voltage throughout a single comparison time, we use the below equation:

$$P_{avg} = \frac{1}{T} \int_0^T V_{DD} \cdot I_D dt \quad (7)$$

Where $T$ is the period of the comparator clock signal and the total current drawn from supply voltage is denoted by $I_D$. So the above formula can be written as

$$P_{avg} = f_{CLK} \int_0^T V_{DD} \cdot I_D dt = f_{CLK} \cdot V_{DD} \int_0^T I_D dt \quad (8)$$

3) Offset Voltage

The input offset voltage of a comparator is the input voltage at which its output changes from one logic level to the other. It may be caused by device mismatch or may be inherent to the design of a comparator. In other words Offset is the input error range below which the comparator is unable to identify the specified minimum voltage difference. As a result, the comparator's resolution and speed are constrained.

In this circuit the offset voltage is reduced from that of [10] by introducing $S_1$ and $S_2$. In Fig. 1, the pre-charge action of $S_1$, $S_4$ keeps transistors $M_3$, $M_6$ off at first, minimising their offset contribution. Now when referenced to the input mismatches between $M_3$ and $M_4$ in a typical design are divided by approximately a factor of $\lambda V ≈ 4$, and those between $M_5$ and $M_6$ by roughly a factor of 10 (since these transistors switch on only towards the end). As a result, $M_1$ and $M_2$ become the primary contributors [13].

By making use of the fact that any capacitive load difference at the point $P$ and $Q$, $(ΔC = C_P - C_Q)$ induces a shift in the trip point shown by the following first-order equation of (9), the comparator input offset can be programmed.

$$V_{io} = \frac{I_{D1}}{g_{m1}} \frac{ΔC}{C_P} = \frac{V_{av1}}{2} \frac{ΔC}{C_P} \quad (9)$$

Here $V_{io}$ is the input offset voltage, $I_{D1}$ is the average current, $g_{m1}$ is the transconductance of $M_1$, $ΔC$ is capacitive load difference at balanced state, and $V_{av1}$ is the overdrive of $M_1$ and $M_2$ in saturation during the initial drain node discharging phase.

Offset cancellation can be performed by introducing binary-sized array of MOS capacitors on both sides of the comparator, with the ability to digitally change the value of any single capacitance shown in Fig. 3. Now in order to further reduce the offset node $P$ and $Q$ can be equipped with several small unit capacitors but will reduce speed and increase the power dissipation [13,17].

Transistor aspect ratio

In order to begin the process of designing a comparator, the first thing that must be considered is to select an optimal transistor sizes that satisfies the offset requirement, provides less latency, and consumes less power. In this case, the size of the transistors have been optimized to be as low as feasible in order to reduce delay and minimise parasitic capacitance.
TABLE 1: TRANSISTOR ASPECT RATIOS (W, L ARE WIDTH AND LENGTHS OF TRANSISTORS)

| Transistor | [10] W/L | Proposed circuit W/L |
|------------|----------|----------------------|
| M₁ - M₂    | 180nm/45nm | 180nm/45nm |
| M₁₀ - M₂₀  | 180nm/45nm | 180nm/45nm |
| M₃ - M₄    | 180nm/45nm | 210nm/45nm |
| M₇         | 180nm/45nm | 180nm/45nm |
| M₅ - M₆    | 285nm/45nm | 120nm/45nm |
| S₃ - S₄    | 285nm/45nm | 270nm/45nm |
| S₁ - S₂    | -        | 120nm/45nm |

III. RESULTS AND DISCUSSIONS

The design is simulated on the Cadence Virtuoso platform using GDPK 45nm Technology with $V_{DD} = 1.2V$. Throughout the procedure, the CLK frequency is set to 100MHz.

Topology of [10] is also simulated on the same platform. The exemplary screenshot of the simulated waveforms for the proposed system is depicted in Fig. 4(a) and 4(b). The same for the [10] has been removed to prevent and for the sake of concision. After comparing the results of the present design to that of [10], Table II lists the specifications and enhancements of the current design.

Fig. 4(a) and 4(b)’s simulation results show that only one output, $V_{oут}$, is changing states during the evaluation period (CLK= 1), while the other, $V_{out}$, remains high (at $V_{DD}$). This decreases average power consumption. According to Fig. 4(b), the pre-charge (reset) and evaluation periods are 28.9ps and 96.9ps, respectively. Therefore, the obtained average delay is 62.9ps. This value is less than that of [10], which is one of the primary advantage of this circuit.

![Fig 4(a)](image)

![Fig 4(b)](image)

Fig. 4(c). Simulation results of proposed circuit for $V_{DD} = 1.2V$, $V_{in} = 400mV$, $V_{ref} = 300mV$, CLK frequency = 100 MHz

Fig. 4(a) and 4(c)’s simulation results show that the pre-charge (reset) and evaluation times are set to be 27.8ps and 243.8ps, respectively. The evaluation time in the waveform in Fig. 4(c) is prolonged when compared to Fig. 4(b). Due to $V_{in}$ and $V_{ref}$’s proximity to one another, the comparator must compare more bits in order to make a judgement, which increases reaction time [10]. As a result, the average delay is 135.8ps. 4.2732 μW is the average power dissipation.

![Fig 4(c)](image)

Fig. 5. Offset voltage of proposed design

The offset voltage measured from Fig. 5. is 28mV.
### TABLE 2: PERFORMANCE COMPARISON

| Topology          | Average Dynamic Power (μW) | Average Delay (ps) | PDP (fJ) | Offset Voltage (mV) |
|-------------------|---------------------------|--------------------|----------|---------------------|
| KasiBandla et al [10] | 4.237                     | 67.43              | 0.286    | 36                  |
| Proposed circuit  | 4.272                     | 62.9               | 0.268    | 28                  |

## IV. CONCLUSION

In this paper design of a modified strong-arm dynamic latch comparator is presented that can operate at high frequency, consumes low power and has a low offset on a supply of $V_{DD} = 1.2$V. This paper has been evaluated against [10]. Important design parameters are shown in Table 2. Both the original topology and proposed circuit topology have been simulated using CADENCE Virtuoso with GDSP 0.18μm technology. Table 1. Presents the optimized transistor sizes. In the proposed design delay is reduced by 6%. Although the power consumption slightly higher than that of [10] but overall PDP is also improved by nearly 6%. When comparing to [10], the proposed design offers a lower offset value without even a trade off with speed.

## ACKNOWLEDGMENT

Authors would like to thank staffs of IC Centre, Jadavpur University for their valuable support guidance.

## REFERENCES

[1] Ka-Meng, Pui-In Mak, Rui P. Martins, “Systematic analysis and cancellation of kickback noise in a dynamic latched comparator,” Analog Integrated Circuits and Signal Processing, Vol. 77(2) pp. 277–284, Nov., 2013.

[2] Heung Jun Jeon, Yong-Bin Kim, Minsu Choi “Offset Voltage Analysis of Dynamic Latched Comparator,”IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), Aug, 2011.

[3] Rodríguez Vázquez A, Delgado Restituto M, Domínguez Castro R, Medeiro F, De La Rosa JM, “Trade-offs in the design of CMOS comparators,” Trade-Offs in Analog Circuit Design. US: Springer; pp. 407-441, 2002.

[4] Cho TB, Gray PR, “A 10 b, 20 Msample/s, 35 mW pipeline A/D converter,” IEEE Journal of Solid-State Circuits, Volume: 30, No: 3, pp. 166-170, March, 1995.

[5] Pelgrom et.al., “Matching properties of MOS transistors,” IEEE Journal of Solid-State Circuits, vol. 24, No. 5, pp. 1433-1439, Oct. 1989.

[6] Jun He et.al., “Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, No. 5, pp. 911-919, May. 2009.

[7] A. Nikoozadeh and B. Murmann, “An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch,” IEEE Transactions on Circuits and Systems I: Express Briefs, vol. 53, No. 12, pp. 1398-1402, Dec.2006.

[8] Ata Khorami, Mohammad Sharifkhani “A low-power technique for high-resolution dynamic comparators,” Wiley International Journal of Circuit Theory and Applications, Vol. 46, No: 10, pp. 1777-1795, Oct. 2018.

[9] B.Murmann et al., “Impact of scaling on analog performance and associated modeling needs,” IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.

[10] Kasi Bandla, Harikrishnan, Dipankar Pal, “Design of Low Power, High Speed, Low Offset and Area Efficient Dynamic-Latch Comparator for SAR-ADC,” 2020 International Conference On Innovative Trends In Communication & Computer Engineering (ITCE’2020), Feb. 2020.

[11] Ili Shairah Abdul Halim “Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18μm Technology,” IEEE-KSM, 2011.

[12] Jun He, Sanyi Zhan, Degang Chen, “Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, NO. 5, May 2009.

[13] B Razavi, “A Circuit for All Seasons – The Strong Arm Latch,” IEEE Solid State Magazine. pp.12-17, Spring 2015.

[14] Mansoure Yousefirad, Mohammad Yavari, “Kick-back Noise Reduction and Offset Cancellation Technique for Dynamic Latch Comparator,” 2021 29th Iranian Conference on Electrical Engineering, Tehran, Iran, May, 2021.

[15] R.S Gamad, Meena Pachore, “Low Power High Speed CMOS Comparator Design using 0.18μm Technology,” International Journal of Electronic Engineering Research, vol. 2, pp. 71-71, 2010.

[16] Bernhard Goll; Horst Zimmermann, “A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V,” IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 56, No. 11, pp. 810 – 814, Oct, 2009.

[17] Pierluigi Nuzzo, “Fernando De Bernardinis, Pierangelo Terreni, Geert Van der Plas, Noise Analysis of Regenerative Comparators for Reconfigurable ADC Architectures,” IEEE Trans. Circuit and System-II: Regular Papers, Vol. 55, NO. 6, July, 2008.