Symbolic Verification of Cache Side-channel Freedom

Sudipta Chattopadhyay
Singapore University of Technology and Design

Abhik Roychoudhury
National University of Singapore

ABSTRACT

Cache timing attacks allow third-party observers to retrieve sensitive information from program executions. But, is it possible to automatically check the vulnerability of a program against cache timing attacks and then, automatically shield program executions against these attacks? For a given program, a cache configuration and an attack model, our CACHEFIX framework either verifies the cache side-channel freedom of the program or synthesizes a series of patches to ensure cache side-channel freedom during program execution. At the core of our framework is a novel symbolic verification technique based on automated abstraction refinement of cache semantics. The power of such a framework is to allow symbolic reasoning over counterexample traces and to combine it with runtime monitoring for eliminating cache side channels during program execution. Our evaluation with routines from OpenSSL, libfixedtimefixedpoint, GDK and FourQlib reveals that our CACHEFIX approach (dis)proves cache side-channel freedom within an average of 75 seconds. Besides, in all except one case, CACHEx synthesizes all patches within 20 minutes to ensure cache side-channel freedom of the respective routines during execution.

1 INTRODUCTION

Cache timing attacks [23, 24] are among the most critical side-channel attacks [25] that retrieve sensitive information from program executions. Recent cache attacks [31] further show that cache side-channel attacks are practical even in commodity embedded processors, such as in ARM-based embedded platforms [31]. The basic idea of a cache timing attack is to observe the timing of cache hits and misses for a program execution. Subsequently, the attacker uses such timing to guess the sensitive input via which the respective program was activated.

Given the practical relevance, it is crucial to verify whether a given program (e.g., an encryption routine) satisfies cache side-channel freedom, meaning the program is not vulnerable to cache timing attacks. However, verification of such a property is challenging for several reasons. Firstly, the verification of cache side-channel freedom requires a systematic integration of cache semantics within the program semantics. This, in turn, is based on the derivation of a suitable abstraction of cache semantics. Our proposed CACHEx approach automatically builds such an abstraction and systematically refines it until a proof of cache side-channel freedom is obtained or a real (i.e., non-spurious) counterexample is produced. Secondly, proving cache side-channel freedom of a program requires reasoning over multiple execution traces. To this end, we propose a symbolic verification technique within our CACHEx framework. Concretely, we capture the cache behaviour of a program via symbolic constraints over program inputs. Then, we leverage recent advances on satisfiability modulo theory (SMT) and constraint solving to (dis)prove the cache side-channel freedom of a program.

An appealing feature of our CACHEx approach is to employ symbolic reasoning over the real counterexample traces. To this end, we systematically explore real counterexample traces and apply such symbolic reasoning to synthesize patches. Each synthesized patch captures a symbolic condition on input variables and a sequence of actions that needs to be applied when the program is processed with inputs satisfying the condition. The application of a patch is guaranteed to reduce the channel capacity of the program under inspection. Moreover, if our checker terminates, then our CACHEx approach guarantees to synthesize all patches that completely shield the program against cache timing attacks [8, 14]. Intuitively, our CACHEx approach can start with a program \( P \) vulnerable to cache timing attack. Then, it leverages a systematic combination of symbolic verification and runtime monitoring to execute \( P \) with cache side-channel freedom.

It is the precision and the novel mechanism implemented within CACHEx that set us apart from the state of the art. Existing works on analyzing cache side channels [15, 22, 30] are incapable to automatically build and refine abstractions for cache semantics. Besides, these works are not directly applicable when the underlying program does not satisfy cache side-channel freedom. Given an arbitrary program, our CACHEx approach generates patches of its cache side-channel freedom or generates input(s) that manifest the violation of cache side-channel freedom. Moreover, our symbolic reasoning framework provides capabilities to systematically synthesize patches and completely eliminate cache side channels during program execution.

We organize the remainder of the paper as follows. After providing an overview of CACHEx (Section 2), we make the following contributions:

1. We present CACHEx, a novel symbolic verification framework to check the cache side-channel freedom of an arbitrary program. To the best of our knowledge, this is the first application of automated abstraction refinement and symbolic verification to check the cache behaviour of a program.

2. We instantiate our CACHEx approach with direct-mapped caches, as well as with set-associative caches with least recently used (LRU) and first-in-first-out (FIFO) policy (Section 4.3). In Section 4.4, we show the generalization of our CACHEx approach over timing-based attacks [14] and trace-based attacks [8].

3. We discuss a systematic exploration of counterexamples to synthesize patches and to shield program executions against cache timing attacks (Section 5). We provide theoretical guarantees that such patch synthesis converges towards completely eliminating cache side channels during execution.

4. We provide an implementation of CACHEx and evaluate it with 25 routines from OpenSSL, GDK, FourQlib and libfixedtimefixedpoint libraries. Our evaluation reveals that CACHEx can establish proof or generate non-spurious counterexamples within 75 seconds on average. Besides, in most cases, CACHEx generated all patches within...
2 OVERVIEW

In this section, we demonstrate the general insight behind our approach through examples. We consider the simple code fragments in Figure 1(a)-(b) where key is a sensitive input. In this example, we will assume a direct-mapped cache having a size of 512 bytes. For the sake of brevity, we also assume that key is stored in a register and accessing key does not involve the cache. The mapping of different program variables into the cache appears in Figure 1(c). Finally, we assume the presence of an attacker who observes the number of cache misses in the victim program. For such an attacker, examples in Figure 1(a)-(b) satisfy cache side-channel freedom if and only if the number of cache misses suffered is independent of key.

Why symbolic verification? Cache side-channel freedom of a program critically depends on how it interacts with the cache. We make an observation that the program cache behaviour can be formulated via a well-defined set of predicates. To this end, let us assume set(rj) captures the cache set accessed by instruction rj and tag(rj) captures the accessed cache tag by the same instruction. Consider the instruction r3 in Figure 1(a). We introduce a symbolic variable miss3, which we intend to set to one if r3 suffers a cache miss and to set to zero otherwise. We observe that miss3 depends on the following logical condition:

\[ \Gamma(r_3) \equiv \neg (0 \leq \text{key} \leq 127 \land \rho_{13}^{\text{set}} \land \neg \rho_{13}^{\text{tag}}) \land \neg (\text{key} \geq 128 \land \rho_{23}^{\text{set}} \land \neg \rho_{23}^{\text{tag}}) \]

(1)

where \( \rho_{ij}^{\text{set}} \equiv (\text{tag}(r_j) \neq \text{tag}(r_i)) \) and \( \rho_{ij}^{\text{tag}} \equiv (\text{set}(r_j) = \text{set}(r_i)) \). Intuitively, \( \Gamma(r_3) \) checks whether both \( r_1 \) and \( r_2 \), if executed, load different memory blocks than the one accessed by \( r_3 \). Therefore, if \( \Gamma(r_3) \) is evaluated to true, then miss3 = 1 (i.e. \( r_3 \) suffers a cache miss) and miss3 = 0 (i.e. \( r_3 \) is a cache hit), otherwise. Formally, we set the cache behaviour of \( r_3 \) as follows:

\[ \Gamma(r_3) \equiv (\text{miss}_3 = 1); \neg \Gamma(r_3) \equiv (\text{miss}_3 = 0) \]

(2)

The style of encoding, as shown in Equation 2, facilitates the usage of state-of-the-art solvers for verifying cache side-channel freedom.

In general, we note that the cache behaviour of the program in Figure 1(a), i.e., the cache behaviours of \( r_1, \ldots, r_4 \) can be formulated accurately via the following set of predicates related to cache semantics:

\[ \text{Pred}_{\text{cache}} = \{ \rho_{ij}^{\text{set}} \cup \rho_{ij}^{\text{tag}} \mid 1 \leq j < i \leq 4 \} \]

(3)

The size of \( \text{Pred}_{\text{cache}} \) depends on the number of memory-related instructions. However, \( |\text{Pred}_{\text{cache}}| \) does not vary with the cache size.

Key insight in abstraction refinement. If the attacker observes the number of cache misses, then the cache side-channel freedom holds for the program in Figure 1(a) when all feasible traces exhibit the same number of cache misses. Hence, such a property \( \varphi \) can be formulated as the non-existence of two traces \( t_1 \) and \( t_2 \) as follows:

\[ \varphi \equiv \neg \exists t_1, \neg \exists t_2 \text{ s.t. } \left( \sum_{i=1}^{t_1} \text{miss}_i^{(t_1)} = \sum_{i=1}^{t_2} \text{miss}_i^{(t_2)} \right) \]

(4)

where missi(tr) captures the valuation of missi in trace tr.

Our key insight is that to establish a proof of \( \varphi \) (or its lack thereof), it is not necessary to accurately track the values of all predicates in Pred\text{cache} (cf. Equation 3). In other words, even if some predicates in Pred\text{cache} have unknown values, it might be possible to (dis)prove \( \varphi \). This phenomenon occurs due to the inherent design principle of caches and we exploit this in our abstraction refinement process.

To realize our hypothesis, we first start with an initial set of predicates (possibly empty) whose values are accurately tracked during verification. In this example, let us assume that we start with an initial set of predicates Pred\text{init} = \{ r_{13}^{\text{set}}, r_{13}^{\text{tag}}, r_{23}^{\text{set}}, r_{23}^{\text{tag}} \}. The rest of the predicates in Pred\text{cache} \setminus \text{Pred}_{\text{init}} are set to unknown value. With this configuration at hand, CACHEFIX returns counterexample traces \( t_1 \) and \( t_2 \) (cf. Equation 4) to reflect that \( \varphi \) does not hold for the program in Figure 1(a). In particular, the following traces are returned:

\[ t_1 \equiv (\text{miss}_1 = \text{miss}_3 = 1, \text{miss}_2 = \text{miss}_4 = 0) \]

\[ t_2 \equiv (\text{miss}_1 = 0, \text{miss}_3 = \text{miss}_3 = \text{miss}_4 = 1) \]

Given \( t_1 \) and \( t_2 \), we check whether any of them are spurious. To this end, we reconstruct the logical condition (cf. Equation 2) that led to the specific valuations of miss3 variables in a trace. For instance in trace \( t_2 \), such a logical condition is captured via \( \neg\Gamma(r_1) \wedge \neg\Gamma(r_3) \wedge \Gamma(r_4) \). It turns out that \( \neg\Gamma(r_1) \wedge \neg\Gamma(r_3) \wedge \Gamma(r_4) \) is unsatisfiable, making \( t_2 \) spurious. This happened due to the incompleteness in tracking the predicates Pred\text{cache}.

To systematically augment the set of predicates and rerun our verification process, we extract the unsatisfiable core from \( \neg\Gamma(r_1) \wedge \neg\Gamma(r_3) \wedge \Gamma(r_4) \). Specifically, we get the following unsatisfiable core:

\[ \mathcal{U} = \neg \rho_{34}^{\text{set}} \land \rho_{34}^{\text{tag}} \]

(5)

Intuitively, with the initial abstraction Pred\text{init}, our checker CACHEFIX failed to observe that \( r_3 \) and \( r_4 \) access the same memory block, hence, \( \mathcal{U} \) is unsatisfiable. We then augment our initial set of predicates with the predicates in \( \mathcal{U} \) and therefore, refining the abstraction as follows:

\[ \text{Pred}_{\text{cur}} = \{ r_{12}^{\text{set}}, r_{13}^{\text{set}}, r_{13}^{\text{tag}}, r_{23}^{\text{set}}, r_{23}^{\text{tag}}, r_{34}^{\text{set}}, r_{34}^{\text{tag}}, \} \]

CACHEFIX successfully verifies the cache side-channel freedom of the program in Figure 1(a) with the set of predicates Pred\text{cur}. We note that the predicates in Pred\text{cache} \setminus \text{Pred}_{\text{cur}} ≠ \emptyset. In particular, we still have unknown values assigned to the following set of predicates:

\[ \text{Pred}_{\text{unknown}} = \{ r_{12}^{\text{set}}, r_{13}^{\text{set}}, r_{13}^{\text{tag}}, r_{23}^{\text{set}}, r_{23}^{\text{tag}}, r_{34}^{\text{set}}, r_{34}^{\text{tag}} \} \]

Therefore, it was possible to verify \( \varphi \) by tracking only half of the predicates in Pred\text{cache}. Intuitively, \( r_{12}^{\text{set}} \) and \( r_{13}^{\text{tag}} \) were not needed to be tracked as \( r_1 \) and \( r_2 \) cannot appear in a single trace, as captured via the program semantics. In contrast, the rest of the predicates in Pred\text{unknown} were not required for the verification process, as neither \( r_1 \) nor \( r_2 \) influences the cache behaviour of \( r_4 \) - it is influenced completely by \( r_3 \).

Key insight in fixing. In general, the state-of-the-art in fixing cache side-channel is to revert to constant-time programming style [9]. Constant-time programming style imposes heavy burden on a programmer to follow certain programming patterns, such as to ensure the absence of input-dependent branches and input-dependent memory accesses. Yet, most programs do not exhibit constant-time
/* key is sensitive input */
char a[256];
unsigned char key;
char b[256];
if (key <= 127)
r1: load reg2, b[255]
else
r2: load reg2, a[255]
r3: load reg1, a[key]
c1: add reg1, reg2
r4: store reg1, a[key]

Figure 1: A code fragment (a) satisfying cache side-channel freedom, (b) violating cache side-channel freedom. (c) Mapping of variables into the cache. (d) Runtime actions and the execution order for the program in Figure 1(b) to ensure cache side-channel freedom.

If we reconstruct the logical condition that led to the specific valuations of \( \text{miss}_1, \ldots, \text{miss}_4 \) in \( tr_1 \) and \( tr_2 \), then we get the symbolic formulas \( \Gamma(r_1) \land \neg \Gamma(r_2) \land \Gamma(r_3) \land \neg \Gamma(r_4) \) and \( \neg \Gamma(r_1) \land \Gamma(r_2) \land \neg \Gamma(r_3) \land \neg \Gamma(r_4) \), respectively. Both the formulas are satisfiable for the example in Figure 1(b). Intuitively, this happens due to \( r_2 \), which loads the same memory block as accessed by \( r_3 \) only if \( key = 255 \).

We observe that \( tr_2 \) will be equivalent to \( tr_1 \) if a cache miss is inserted in the beginning of \( tr_2 \). To this end, we need to know all inputs that lead to \( tr_2 \). Thanks to the symbolic nature of our analysis, we obtain the exact symbolic condition, i.e., \( \neg \Gamma(r_1) \land \Gamma(r_2) \land \neg \Gamma(r_3) \land \neg \Gamma(r_4) \) that manifests the trace \( tr_2 \). Therefore, if the program in Figure 1(b) is executed with any input satisfying \( \neg \Gamma(r_1) \land \Gamma(r_2) \land \neg \Gamma(r_3) \land \neg \Gamma(r_4) \), then a cache miss is injected as shown in Figure 1(d). This ensures the cache side-channel freedom during program execution, as all traces exhibit the same number of cache misses.

Our proposed fixing mechanism is novel that it does not rely on any specific programming style. Moreover, as we generate the fixes by directly leveraging the verification results, we can provide strong security guarantees during program execution.

3 THREAT AND SYSTEM MODEL

**Threat Model.** We assume that an attacker makes observations on the execution traces of victim program \( P \) and the implementation of \( P \) is known to the attacker. Besides, there does not exist any error in the observations made by the attacker. We also assume that an attacker can execute arbitrary user-level code on the processor that runs the victim program. This, in turn, allows the attacker to flush the cache (e.g., via accessing a large array) before the victim routine starts execution. We, however, do not assume that the attacker can access the address space of the victim program \( P \). We believe the aforementioned assumptions on the attacker are justified, as we aim to verify the cache side-channel freedom of programs against strong attacker models.

We capture an execution trace via a sequence of hits \( h \) and misses \( m \). Hence, formally we model an attacker as the mapping \( O : \{h, m\}^* \rightarrow \mathbb{X} \), where \( \mathbb{X} \) is a countable set. For \( tr_1, tr_2 \in \{h, m\}^* \), an attacker can distinguish \( tr_1 \) from \( tr_2 \) if and only if \( O(tr_1) \neq O(tr_2) \). In this paper, we instantiate our checker for the following realistic attack models:

- \( O_{time} : \{h, m\}^* \rightarrow \mathbb{N} \). \( O_{time} \) maps each execution trace to the number of cache misses suffered by the same. This attack model imitates cache timing attacks [14].
- \( O_{trace} : \{h, m\}^* \rightarrow \{0, 1\}^* \). \( O_{trace} \) maps each execution trace to a bitvector (\( h \) is mapped to 0 and \( m \) is mapped to 1). This attack model imitates trace-based attacks [8].

**Processor model.** We assume an ARM-style processor with one or more cache levels. However, we consider timing attacks only
due to first-level instruction or data caches \cite{8, 14}. We currently do not handle more advanced attacks on shared caches \cite{32}. First-level caches can either be partitioned (instruction vs. data) or unified. We assume that set-associative caches have either LRU or FIFO replacement policy. Other deterministic replacement policies can easily be integrated within CACHEFIX via additional symbolic constraints. Finally, our timing model only takes into account the effect of caches. Timing effects due to other micro-architectural features (e.g. pipeline and branch prediction) are currently not handled. For the sake of brevity, we discuss the timing effects due to memory-related instructions. It is straightforward to integrate the timing effects of computation instructions (e.g. add) into CACHEFIX.

4 ABSTRACTION REFINEMENT

Notations. We represent cache via a triple \((\mathbb{Z}^S, \mathbb{Z}^B, \mathcal{A})\) where \(\mathbb{Z}^S, \mathbb{Z}^B\) and \(\mathcal{A}\) capture the number of cache sets, cache line size and cache associativity, respectively. We use \(\text{set}(r_i)\) and \(\text{tag}(r_i)\) to capture the cache set and cache tag, respectively, accessed by instruction \(r_i\). Additionally, we introduce a symbolic variable \(\text{miss}_j\) to capture whether \(r_i\) was a miss (\(\text{miss}_j = 1\)) or a hit (\(\text{miss}_j = 0\)). For instructions \(r_i\) and \(r_j\), we have \(j < i\) if and only if \(r_j\) was (symbolically) executed before \(r_i\).

4.1 Initial abstract domain

We assume that a routine may start execution with any initial cache state, but it does not access memory blocks within the initial state during execution \cite{22}. Hence, for a given instruction \(r_i\), its cache behaviour might be affected by all instructions executing prior to \(r_i\). Concretely, the cache behaviour of \(r_i\) can be accurately predicted based on the set of logical predicates \(\text{Pred}_{\text{set}}\) and \(\text{Pred}_{\text{tag}}\) as follows:

\[
\text{Pred}_{\text{set}} = \{\text{set}(r_j) = \text{set}(r_i) \mid 1 \leq j < i\}
\]

\[
\text{Pred}_{\text{tag}} = \{\text{tag}(r_j) \neq \text{tag}(r_i) \mid 1 \leq j < i\}
\]

(6)

Intuitively, \(\text{Pred}_{\text{set}}\) captures the set of predicates checking whether any instruction prior to \(r_i\) accesses the same cache set as \(r_i\). Similarly, \(\text{Pred}_{\text{tag}}\) checks whether any instruction prior to \(r_i\) has a different cache tag than \(\text{tag}(r_i)\). Based on this intuition, the following set of predicates are sufficient to predict the cache behaviours of \(N\) memory-related instructions.

\[
\text{Pred}_{\text{set}} = \bigcup_{i=1}^{N} \text{Pred}_{\text{set}}^i; \quad \text{Pred}_{\text{tag}} = \bigcup_{i=1}^{N} \text{Pred}_{\text{tag}}^i
\]

(7)

For the sake of efficiency, however, we launch verification with a smaller set of predicates \(\text{Pred}_{\text{init}} \subseteq \text{Pred}_{\text{tag}} \cup \text{Pred}_{\text{set}}\) as follows:

\[
\text{Pred}_{\text{init}} = \{p \mid p \in \text{Pred}_{\text{tag}} \cup \text{Pred}_{\text{set}} \land |\sigma(r_i)| = 1 \land \forall k \in [1,i], |\sigma(r_k)| = 1 \land \text{guard}_k \Rightarrow \text{true}\}
\]

(8)

\(\sigma(r_i)\) captures the set of memory blocks accessed by instruction \(r_i\) and \(\text{guard}_k\) controls the condition under which \(r_k\) is executed. In general, our CACHEFIX approach works even if \(\text{Pred}_{\text{init}} = \emptyset\). However, to accelerate the convergence of CACHEFIX, we start with the predicates whose values can be statically determined (i.e. independent of inputs). Intuitively, we take this approach for two reasons: firstly, the set \(\text{Pred}_{\text{init}}\) can be computed efficiently during symbolic execution. Secondly, as the predicates in \(\text{Pred}_{\text{init}}\) have constant valuation, they reduce the size of the formula to be discharged to the SMT solver. We note that \(\text{guard}_k\) depends on the program semantics. The abstraction of program semantics is an orthogonal problem and for the sake of brevity, we skip its discussion here.

4.2 Abstract domain refinement

We use the mapping \(\Gamma: \{r_1, r_2, \ldots, r_N\} \rightarrow \{\text{true}, \text{false}\}\) to capture the conditions under which \(r_i\) was a cache hit (i.e. \(\text{miss}_i = 0\)) or a cache miss (i.e. \(\text{miss}_i = 1\)). In particular, the following holds:

\[
\Gamma(r_i) \equiv (\text{miss}_i = 1); \quad \neg\Gamma(r_i) \equiv (\text{miss}_i = 0)
\]

(9)

\(\Gamma(r_i)\) depends on predicates in \(\text{Pred}_{\text{set}}^i \cup \text{Pred}_{\text{tag}}^i\) and the cache configuration. We show the formulation of \(\Gamma(r_i)\) in Section 4.3.

ExecuteSymbolic. Algorithm 1 captures the overall verification process based on our systematic abstraction refinement. The symbolic verification engine computes a formula representation \(\Psi\) of the program \(\mathcal{P}\). This is accomplished via a symbolic execution on program \(\mathcal{P}\) (cf. procedure \text{EXECUTESymbolic}) and systematically translating the cache and program semantics of each instruction into a set of constraints (cf. procedure \text{CONVERT}).

Convert. During the symbolic execution, a set of symbolic states, each capturing a unique execution path reaching an instruction \(r_i\), is maintained. This set of symbolic states can be viewed as a disjunction \(\Psi(r_i) \equiv \psi_1 \lor \psi_2 \lor \ldots \lor \psi_j\), where \(\Psi(r_i) \Rightarrow \Psi\) and each \(\psi_j\) symbolically captures a unique execution path leading to instruction \(r_i\). At each instruction \(r_i\), the procedure \text{CONVERT} translates \(\Psi(r_i)\) in such a fashion that \(\Psi(r_i)\) integrates both the cache semantics (cf. lines 13-14) and program semantics (cf. lines 18) of

\begin{algorithm}
\caption{Abstraction Refinement Algorithm}
\KwIn{Program \(\mathcal{P}\), cache configuration \(\mathcal{C}\), attack model \(\mathcal{O}\)}
\KwOut{Successful verification or a concrete counterexample}

1: /* \(\Psi\) is a formula representation of \(\mathcal{P}\) */
2: /* \(\text{Pred}\) is cache-semantics-related predicates */
3: /* \(\Gamma\) determines cache behaviour of all instructions */
4: \(\langle \Psi, \text{Pred}, \Gamma \rangle \Rightarrow \text{EXECUTESymbolic}(\mathcal{P}, \mathcal{C})\)
5: /* Formulate initial abstraction (cf. Equation 8) */
6: \(\text{Pred}_{\text{init}} := \text{GETINITIALABSTRACTION}(\text{Pred})\)
7: /* Rewrite \(\Psi\) with initial abstraction */
8: \(\text{REWRITE}(\Psi, \text{Pred}_{\text{init}})\)
9: /* Formulate cache side-channel freedom property */
10: \(\varphi := \text{GETPROPERTY}(\mathcal{O})\)
11: /* Invoke symbolic verification to check \(\Psi \land \neg\varphi\) */
12: \((\text{res}, \text{tr}_1, \text{tr}_2) := \text{VERIFY}(\Psi, \varphi)\)
13: while \((\text{res}=\text{false}) \land (\text{tr}_1 \lor \text{tr}_2 \text{ is spurious})\) do
14: /* Extract unsatisfiable core from \(\text{tr}_1\) and/or \(\text{tr}_2\) */
15: \(\mathcal{U} := \text{UNSACORE}(\text{tr}_1, \text{tr}_2, \Gamma)\)
16: /* Refine abstractions and repeat verification */
17: \(\text{Pred}_{\text{cur}} := \text{REFINE}(\text{Pred}_{\text{init}}, \mathcal{U}, \text{Pred})\)
18: \(\text{REWRITE}(\Psi, \text{Pred}_{\text{cur}})\)
19: \((\text{res}, \text{tr}_1, \text{tr}_2) := \text{VERIFY}(\Psi, \varphi)\)
20: \(\text{Pred}_{\text{init}} := \text{Pred}_{\text{cur}}\)
21: end while
22: return \(\text{res}\)
\end{algorithm}
### Procedure 2 Symbolically Tracking Program and Cache States

```plaintext
1: /* symbolically execute \( \mathcal{P} \) with cache configuration \( C^* \)
2: procedure EXECUTE_SYMBOLIC(\( \mathcal{P} \), \( C \))
3: \( i := 1 \); \( \Psi := true \); Pred_set := Pred_tag := \( \emptyset \)
4: \( r_0 := \text{GET_NEXT_INSTRUCTION}(\mathcal{P}) \)
5: while \( r_0 \neq \text{exit} \) do
6:   if \( r_0 \) is memory-related instruction then
7:     /* Collect predicates for cache semantics */
8:     Pred_set \( \cup \) Pred_set\( ^{\text{set}} \); Pred_tag \( \cup \) Pred_tag\( ^{\text{tag}} \)
9:     /* \( \Gamma(r_0) \) determines cache behaviour of \( r_0 \) */
10:    Formulate \( \Gamma(r_0) \) /* see Section 4.3 */
11:    \( \Gamma \cup \{ \Gamma(r_0) \} \)
12:    /* Integrate cache semantics within \( \Psi \) */
13:    \( \Psi := \text{CONVERT}(\Psi, \Gamma(r_0) \Rightarrow (\text{miss}_i = 1)) \)
14:    \( \Psi := \text{CONVERT}(\Psi, \neg\Gamma(r_0) \Rightarrow (\text{miss}_i = 0)) \)
15: end if
16: /* Integrate program semantics of \( r_0 \) within \( \Psi \) */
17: \( \Psi := \text{CONVERT}(\Psi, \varphi(r_0)) \)
18: \( i := i + 1 \)
19: \( r_0 := \text{GET_NEXT_INSTRUCTION}(\mathcal{P}) \)
20: end while
21: return (\( \Psi, \text{Pred_set} \cup \text{Pred_tag} \), \( \Gamma \))
22: end procedure
```

For \( r_0 \). In order to integrate semantics of a memory-related instruction \( r_0 \), \( \Psi(r_0) \) is converted to \( \Psi(r_0) \wedge (\Gamma(r_0) \Leftrightarrow (\text{miss}_i = 1)) \wedge (\neg\Gamma(r_0) \Leftrightarrow (\text{miss}_i = 0)). \) Similarly, the program semantics of instruction \( r_0 \), as captured via \( \varphi(r_0) \), is integrated within \( \Psi(r_0) \) as \( \Psi(r_0) \wedge \varphi(r_0) \). Translating the program semantics of each instruction to a set of constraints is a standard technique in any symbolic model checking [19]. Moreover, such a translation is typically carried out on a program in static single assignment (SSA) form and takes into account both data and control flow. Unlike classic symbolic analysis, however, we consider both the cache semantics and program semantics of an execution path, as explained in the preceding.

**GetInitialAbstraction.** We start our verification with an initial abstraction of cache semantics (cf. Equation 8). Such an initial abstraction contains a partial set of logical predicates \( \text{Pred}_{\text{init}} \subseteq \text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}} \). Based on \( \text{Pred}_{\text{init}} \), we rewrite \( \Psi \) via the procedure \text{REWRITE} as follows: We walk through \( \Psi \) and look for occurrences of any predicate \( p^* \in (\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}) \setminus \text{Pred}_{\text{init}} \). For any \( p^* \) discovered in \( \Psi \), we replace \( p^* \) with a fresh symbolic variable \( V_{\text{p}^*} \). Intuitively, this means that during the verification process, we assume any truth value for the predicates in \( (\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}) \setminus \text{Pred}_{\text{init}} \). This, in turn, substantially reduces the size of the symbolic formula \( \Psi \) and simplifies the verification process.

**Verify and GetProperty.** The procedure \text{VERIFY} invokes the solver to check the cache side-channel freedom of \( \mathcal{P} \) with respect to attack model \( O \). The property \( \varphi \), capturing the cache side-channel freedom, is computed via \text{GETPROPERTY}. For example, in timing-based attacks, \( \varphi \) is captured via the non-existence of any two traces \( tr_1 \) and \( tr_2 \) that have different number of cache misses (cf. Equation 4). In other words, if the following formula is satisfied with more than one valuations for \( \sum_{i=1}^{N} \text{miss}_i \), then side-channel freedom is violated:

\[
\Psi \wedge \left( \sum_{i=1}^{N} \text{miss}_i \right) \geq 0
\]

Here \( N \) captures the total number of memory-related instructions encountered during the symbolic execution of \( \mathcal{P} \).

**Refine and Rewrite.** When our verification process fails, we check the feasibility of a counterexample trace \( \text{trace} \in \{tr_1, tr_2\} \). Recall from Equation 9 that if \( r_i \) is a cache miss if and only if \( \Gamma(r_i) \) holds \( \text{true} \). We leverage this relation to construct the following formula \( \Gamma_{\text{trace}} \) for feasibility checking:

\[
\Gamma_{\text{trace}} = N \sum_{i=1}^{N} \left( \Gamma(r_i), \text{if miss}^{(\text{trace})}_i = 1; \neg\Gamma(r_i), \text{if miss}^{(\text{trace})}_i = 0; \right)
\]

In Equation 11, \( \text{miss}^{(\text{trace})}_i \) captures the valuation of symbolic variable \( \text{miss}_i \) in the counterexample trace. We note that \( \text{trace} \) is not a spurious counterexample if and only if \( \Gamma_{\text{trace}} \) is satisfiable, hence, highlighting the violation of cache side-channel freedom.

If \( \Gamma_{\text{trace}} \) is unsatisfiable, then our initial abstraction \( \text{Pred}_{\text{init}} \) was insufficient to (dis)prove the cache side-channel freedom. In order to refine this abstraction, we extract the unsatisfiable core from the symbolic formula \( \Gamma_{\text{trace}} \) via the procedure UNSATCORE. Such an unsatisfiable core contains a set of CNF clauses \( \bigcup_{k \in [1, N]} \Gamma(r_k) \). We note each \( \Gamma(r_k) \) is a function of the set of predicates \( \text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}} \). Finally, we refine the abstraction (cf. procedure \text{REFINE} in Algorithm 1) to \( \text{Pred}_{\text{cur}} \) by including all predicates in the unsatisfiable core as follows:

\[
\text{Pred}_{\text{cur}} := \text{Pred}_{\text{init}} \cup \{ p^* \mid p^* \in \text{UnsatCore}(\Gamma_{\text{trace}}) \setminus \text{Pred}_{\text{init}} \}
\]

With the refined abstraction \( \text{Pred}_{\text{cur}} \), we rewrite the symbolic formula \( \Psi \) (cf. procedure \text{REWRITE}). In particular, we identify the placeholder symbolic variables for predicates in the set \( \text{Pred}_{\text{cur}} \setminus \text{Pred}_{\text{init}} \). We rewrite \( \Psi \) by replacing these placeholder symbolic variables with the respective predicates in the set \( \text{Pred}_{\text{cur}} \setminus \text{Pred}_{\text{init}} \). It is worthwhile to note that the placeholder symbolic variables in \( (\text{Pred}_{\text{tag}} \cup \text{Pred}_{\text{set}}) \setminus \text{Pred}_{\text{cur}} \) remain unchanged.

### 4.3 Modeling Cache Semantics

For each memory-related instruction \( r_i \), the formulation of \( \Gamma(r_i) \) is critical to prove the cache side-channel freedom. The formulation of \( \Gamma(r_i) \) depends on the configuration of caches. Due to space constraints, we will only discuss the symbolic model for direct-mapped caches (symbolic models for LRU and FIFO caches are provided in the appendix). To simplify the formulation, we will use the following abbreviations for the rest of the section:

\[
\rho^\text{set}_{ij} \equiv (\text{set}(r_i) = \text{set}(r_j)) \quad \rho^\text{tag}_{ij} \equiv (\text{tag}(r_i) \neq \text{tag}(r_j))
\]

We also distinguish between the following variants of misses:

1. **Cold misses:** Cold misses occur when a memory block is accessed for the first time.
2. **Conflict misses:** All cache misses that are not cold misses are referred to as conflict misses.
Formulating conditions for cold misses. Cold cache misses occur when a memory block is accessed for the first time during program execution. In order to check whether \( r_i \) suffers a cold miss, we check whether all instructions \( r \in \{r_1, r_2, \ldots, r_{i-1}\} \) access different memory blocks than the memory block accessed by \( r_i \). This is captured as follows:

\[
\Theta_{cold}^i \equiv \bigwedge_{j \in [1, i)} \left( \neg r_j^{set} \lor r_j^{tag} \lor \neg \text{guard}_j \right)
\] (14)

Recall that \( \text{guard}_j \) captures the control condition under which \( r_j \) is executed. Hence, if \( \text{guard}_j \) is evaluated false for a trace, then \( r_j \) does not appear in the respective trace. If \( \Theta_{cold}^i \) is satisfied, then \( r_i \) inevitably suffers a cold cache miss.

Formulating conditions for conflict cache misses. For direct-mapped caches, an instruction \( r_i \) suffers a conflict miss due to an instruction \( r_j \) if all of the following conditions are satisfied:

\[
\phi_{ji}^{conf, dir} \equiv r_j^{tag} \land r_j^{set}
\]

\[
\phi_{ji}^{rel, dir} \equiv \bigwedge_{j < k < i} \left( \neg r_k^{tag} \lor \neg r_k^{set} \lor \neg \text{guard}_k \right)
\]

Intuitively, \( \phi_{ji}^{rel, dir} \) captures that all instructions between \( r_j \) and \( r_i \) access the same memory block. For instance, consider the memory-access block access sequence \( (r_j : m_1) \rightarrow (r_j : m_2) \rightarrow (r_i : m_2) \), where both \( m_1 \) and \( m_2 \) are mapped to the same cache set and \( r_{i-1} \) accesses the same memory block \( m_2 \) as \( r_i \). This is formally captured as follows:

\[
\phi_{ji}^{rel, dir} = \bigwedge_{j < k < i} \left( \neg r_k^{tag} \lor \neg r_k^{set} \lor \neg \text{guard}_k \right)
\] (16)

Timing-based attacks. In timing-based attacks, an attacker aims to distinguish traces based on their timing. In our framework, we verify the following property to ensure cache side-channel freedom:

\[
\Psi \land \left( \sum_{i=1}^{N} \text{miss}_i \right) \geq 0 \left| \right|_{\text{sol}} \left( \sum_{i=1}^{N} \text{miss}_i \right) \leq 1
\] (19)

\( N \) captures the number of symbolically executed, memory-related instructions. \( \text{sol}(\sum_{i=1}^{N} \text{miss}_i) \) captures the number of valuations of \( \sum_{i=1}^{N} \text{miss}_i \). Intuitively, Equation 19 aims to check that the underlying program has exactly one cache behaviour, in terms of the total number of cache misses.

Trace-based attacks. In trace-based attacks, an attacker monitors the cache behaviour of each memory access. We define a partial function \( \xi : \{r_1, \ldots, r_N\} \rightarrow \{0, 1\} \) as follows:

\[
\xi(r_i) = \begin{cases} 
1, & \text{if } \text{guard}_i \land (\text{miss}_i = 1) \text{ holds;} \\
0, & \text{if } \text{guard}_i \land (\text{miss}_i = 0) \text{ holds.}
\end{cases}
\] (20)

The following verification goal ensures side-channel freedom:

\[
\Psi \land |\text{dom}(|\xi|)\rangle \geq 0 \land \langle |\text{dom}(|\xi|)\rangle \land \text{trace} \geq 0 \left| \right|_{\text{sol}} \left( |\text{dom}(|\xi|)\rangle \right) \leq 1
\] (21)

where \( \text{dom}(|\xi|) \) captures the domain of \( \xi \). \( \| \text{trace} \| \) denotes the number of valuations of the execution trace (with respect to the indexes of \( r_i \)) concatenation operation and \( X = \langle |\text{dom}(|\xi|)\rangle \land \text{trace} \rangle \). Intuitively, we check whether there exists exactly one cache behaviour sequence.

5 RUNTIME MONITORING

CACHEFix produces the first real counterexample when it discovers two traces with different observations (w.r.t. attack model \( O \)). These traces are then analyzed to compute a set of runtime actions that are guaranteed to reduce the uncertainty to guess sensitive inputs. Overall, our runtime monitoring involves the following crucial steps:

- We analyze a counterexample trace \( tr \) and extract the symbolic condition for which the same trace would be generated,
- We systematically explore unique counterexamples with the objective to reduce the uncertainty to guess sensitive inputs,
- We compute a set of runtime actions that need to be applied for improving the cache side-channel freedom.

In the following, we discuss these three steps in more detail.

Analyzing a counterexample trace. Given a real counterexample trace, we extract a symbolic condition that captures all the inputs for which the same counterexample trace can be obtained. Thanks to the symbolic nature of our analysis, CACHEFix already includes capabilities to extract these monitors as follows:

\[
v \equiv \bigwedge_{r_i \in \text{trace}} \left( \Gamma(r_i), \text{if } \text{miss}_i^{(\text{trace})} = 1; \right)
\]

\[
- \Gamma(r_i), \text{if } \text{miss}_i^{(\text{trace})} = 0;
\] (22)

where \( \text{miss}_i^{(\text{trace})} \) is the valuation of symbolic variable \( \text{miss}_i \) in \( \text{trace} \). We note that \( v \Rightarrow \neg \Gamma(r_i) \) for any \( r_j \) that does not appear in \( \text{trace} \) (i.e., \( r_j \notin \text{trace} \)). Hence, to formulate \( v \), it was sufficient to consider only the instructions that appear in \( \text{trace} \).
Once we extract a monitor $\nu$ from counterexample trace, the symbolic system $\Phi$ is refined to $\Phi \land \neg \nu$. This is to ensure that we only explore unique counterexample traces.

**Systematic exploration of counterexamples.** The order of exploring counterexamples is crucial to satisfy monotonicity, i.e., to reduce the channel capacity (a standard metric to quantify the information flow from sensitive input to attacker observation) of $\mathcal{P}$ with each round of patch generation. To this end, CACHEFix employs a strategy that can be visualized as an exploration of the equivalence classes of observations (e.g., #cache misses), i.e., we explore all counterexamples in the same equivalence class in one shot. In order to find another counterexample exhibiting the same observation as observation $o$, we modify the verification goal as follows, for timing and trace-based attacks, respectively (cf. Equation 20 for $\xi$):

$$\Phi \land \neg \left( \bigwedge_{i=1}^{N} \text{miss}_i \neq o \right)$$

$$\Phi \land \neg \left( \bigvee_{r \in \text{dom}(\xi)} \xi(r) \neq \bigvee_{r \in \text{dom}(\xi)} \xi(r) \right)$$

where $[X]_o$ captures the valuation of $X$ with respect to observation $o$ and $N$ is the total number of symbolically executed, memory-related instructions. If Equation 23 is unsatisifiable, then it captures the absence of any more counterexample with observation $o$. We note that $\Phi$ is automatically refined to avoid discovering duplicate or spurious counterexamples. If Equation 23 is satisifiable, our checker provides another real counterexample with the observation $o$. We repeat the process until no more real counterexample with the observation $o$ is found, at which point Equation 23 becomes unsatisfiable.

To explore a different equivalence class of observation than that of observation $o$, CACHEFix negates the verification goal. For $O_{time}$ as an example, the verification goal is changed as follows:

$$\Phi \land \neg \left( \bigwedge_{i=1}^{N} \text{miss}_i = o \right)$$

We note that Equation 24 is satisifiable if and only if there exists an execution trace with observation differing from $o$.

**Runtime actions to improve side-channel freedom.** Our checker maintains the record of all explored observations and the symbolic conditions capturing the equivalence classes of respective observations. At each round of patch (i.e. runtime action) synthesis, we walk through this record and compute the necessary runtime actions for improving cache side-channel freedom.

$O_{time}$. Assume $\Omega = \langle (v_1, a_1), (v_2, a_2), \ldots, (v_k, a_k) \rangle$ where each $a_i$ captures a unique number of observed cache misses and $v_j$ symbolically captures all inputs that lead to observation $o_i$. Our goal is to manipulate executions so that they lead to the same number of cache misses. To this end, the patch synthesis stage determines the amount of cache misses that needs to be added for each element in $\Omega$. Concretely, the set of runtime actions generated are as follows:

$$\left\{ v_1, \left( \max_{i \in [1,k]} a_i - o_1 \right) \right\}, \ldots, \left\{ v_k, \left( \max_{i \in [1,k]} a_i - o_k \right) \right\}$$

In practice, when a program is run with input $I$, we check whether $I \in v_2$ for some $x \in [1,k]$. Subsequently, $\left\{ \max_{i \in [1,k]} a_i - o_k \right\}$ cache misses were injected before the program starts executing.

$O_{trace}$. During trace-based attacks, the attacker makes an observation on the sequence of cache hits and misses in an execution trace. Therefore, our goal is to manipulate executions in such a fashion that all execution traces lead to the same sequence of cache hits and misses. To accomplish this, each runtime action involves the injection of cache misses or hits before execution, after execution or at an arbitrary point of execution. It also involves invalidating an address in cache. Concretely, this is formalized as follows:

$$\langle v_i, \langle c_1, a_1 \rangle, \langle c_2, a_2 \rangle, \ldots, \langle c_k, a_k \rangle \rangle$$

where $v_i$ captures the symbolic input condition where the runtime actions are employed. For any input satisfying $v_i$, we count the number of instructions executed. If the number of executed instructions reaches $c_j$, then we perform the action $a_j$ (e.g. injecting hits/misses or invalidating an address in cache), for any $j \in [1,k]$.

As an example, consider a trace-based attack in the example of Figure 1(b). Our checker will manipulate counterexample traces by injecting cache misses and hits as follows (injected cache hits and misses are highlighted in bold):

$$tr_i'' \equiv (\text{miss}, \text{hit}, \text{hit}, \text{hit}); \quad tr_2'' \equiv (\text{miss}, \text{miss}, \text{hit}, \text{hit})$$

Therefore, the following actions are generated to ensure cache side-channel freedom against trace-based attacks:

$$\langle \text{key} = 255, \langle (0, \text{miss}) \rangle, 0 \leq \text{key} \leq 254, \langle (3, \text{hit}) \rangle \rangle$$

We use string alignment algorithm [6] to make two traces equivalent (via insertion of cache hits/misses or substitution of hits to misses).

**Practical consideration.** In practice, the injection of a cache miss can be performed via accessing a fresh memory block (cf. Figure 1(d)). However, unless the injection of a cache miss happens to be in the beginning or at the end of execution, the cache needs to be disabled before and enabled after such a cache miss. Consequently, our injection of misses does not affect cache states. In ARM-based processor, this is accomplished via manipulating the C bit of CP15 register. The injection of a cache hit can be performed via tracking the last accessed memory address and re-accessing the same address.

To change a cache hit to a cache miss, the accessed memory address needs to be invalidated in the cache. CACHEFix symbolically tracks the memory address accessed at each memory-related instruction. When the program is run with input $I \in v_2$, we concretize all memory addresses with respect to $I$. Hence, while applying an action that involves cache invalidation, we know the exact memory address that needs to be invalidated. In ARM-based processor, the instruction MCR provides capabilities to invalidate an address in the cache.

We note the preceding manipulations on an execution requires additional registers. We believe this is possible by using some system register or using a locked portion in the cache.

**Properties guaranteed by CacheFix.** CACHEFix satisfies the following crucial properties (proofs are included in the appendix) on channel capacity, shannon entropy and min entropy; which are standard metrics to quantify the information flow from sensitive inputs to the attacker observation.
PROPERTY 1. (Monotonicity) Consider a victim program $P$ with sensitive input $K$. Given attack models $O_{time}$ or $O_{trace}$, assume that the channel capacity to quantify the uncertainty of guessing $K$ is $G_{cap}^P$. CacheFix guarantees that $G_{cap}^P$ monotonically decreases with each synthesized patch (cf. Equation 25-26) employed at runtime.

PROPERTY 2. (Convergence) Consider a victim program $P$ with sensitive input $K$. In the absence of any attacker, assume that the uncertainty to guess $K$ is $G_{init}^{G}, G_{init}^{\text{shn}}$ and $G_{init}^{\text{min}}$ via channel capacity, Shannon entropy and Min entropy, respectively. If CacheFix terminates and all synthesized patches are applied at runtime, then the channel capacity (respectively, Shannon entropy and Min entropy) will remain $G_{cap}^{\text{init}}$ (respectively, $G_{\text{shn}}^{\text{init}}$ and $G_{\text{min}}^{\text{init}}$) even in the presence of attacks captured via $O_{time}$ and $O_{trace}$.

6 IMPLEMENTATION AND EVALUATION

Implementation setup. The input to CACHEFIX is the target program and a cache configuration. We have implemented CacheFix on top of CBMC bounded model checker [1]. It first builds a formula representation of the input program via symbolic execution. Then, it checks the (un)satisfiability of this formula against a specification property. Despite being a bounded model checker, CBMC is used as a classic verification tool in our experiments. In particular for program loops, CBMC first attempts to derive loop bounds automatically. If CBMC fails to derive certain loop bounds, then the respective loop bounds need to be provided manually. Nevertheless, during the verification process, CBMC checks all manually provided loop bounds and the verification fails if any such bound was erroneous. In our experiments, all loop bounds were automatically derived by CBMC. In short, if CacheFix successfully verifies a program, then the respective program exhibits cache side-channel freedom for the given cache configuration and targeted attack models.

The implementation of our checker impacts the entire workflow of CBMC. We first modify the symbolic execution engine of CBMC to insert the predicates related to cache semantics. As a result, upon the termination of symbolic execution, the formula representation of the program encodes both the cache semantics and the program semantics. Secondly, we systematically rewrite this formula based on our abstraction refinement process embodied within CacheFix substantially reduces the verification time as opposed to when no refinement process was employed.

Subject programs and cache. We have chosen security-critical subjects from OpenSSL [5], GDK [3], arithmetic routines from libc/libfixedtimepoint and FourQlib [2] to evaluate CacheFix (cf. Table 1). We include representative routines exhibiting constant cache-timing, as well as routines exhibiting variable cache timing. We set the default cache to be 1KB direct-mapped, with a line size of 32 bytes.

Efficiency of checking. Table 1 captures a summary of our evaluation for CacheFix. The outcome of this evaluation is either a successful verification (✓) or a non-spurious counterexample (✗). CacheFix accomplished the verification tasks for all subjects only within a few minutes. The maximum time taken by our checker was 390 seconds for the routine $\text{fix}_\text{pow}$—a constant time implementation of powers (x$^y$). $\text{fix}_\text{pow}$ has complex memory access patterns, however, its flat structure ensures cache side-channel freedom.

To check the effectiveness of our abstraction refinement process, we compare CacheFix with a variant of our checker where all predicates in $\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}$ are considered. Therefore, such a variant does not employ any abstraction refinement, as the set of predicates $\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}$ is sufficient to determine the cache behaviour of all instructions in the program. We compare CacheFix with this variant in terms of the number of predicates, as well as the verification time. We record the set of predicates $\text{Pred}_{\text{tag}}$ considered in CacheFix when it terminates with a successful verification (✓) or a real counterexample (✗). Table 1 clearly demonstrates the effectiveness of our abstraction refinement process. Specifically, for AES, DES and $\text{fix}_\text{pow}$, the checker does not terminate in ten minutes when all predicates in $\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}$ are considered during the verification process. In general, the refinement process reduces the number of considered predicates by a factor of 1.81x on average. This leads to a substantial improvement in verification time, as observed from Table 1.

The routines chosen from OpenSSL library are single path programs. However, AES and DES exhibit input-dependent memory accesses, hence, violating side-channel freedom. The other routines violate cache side-channel freedom due to input-dependent loop trip counts. For example, routines chosen from the GDK library employ a binary search of the input keystroke over a large table. We note that both libfixedtimepoint and FourQlib libraries include comments involving the security risks in $\text{fix}_\text{frac}$ and ecc_point_validate (cf. validate in Table 1).

Overhead from monitors. We evaluated the time taken by CacheFix for counterexample exploration and patch generation (cf. Section 5). For each generated patch, we have also evaluated the overhead induced by the same at runtime (cf. Table 2).

Table 2 captures the maximum and average overhead induced by CacheFix at runtime. We compute the overhead via the number of additional runtime actions (i.e. cache misses, hits or invalidations) introduced solely via CacheFix. In absolute terms, the maximum (average) overhead captures the maximum (average) number of runtime actions induced over all equivalence classes. The maximum overhead was introduced in case of $x_{\text{DES}}$ – 300 actions for $O_{\text{time}}$ and 371 actions for $O_{\text{trace}}$. This is primarily due to the difficulty in making a large number of traces equivalent in terms of the number of cache misses and the sequence of hit/miss, respectively. Although the number of actions introduced by CacheFix is non-negligible, we note that their effect is minimal on the overall execution. To this end, we execute the program for 100 different inputs in each explored equivalence class and measure the overhead introduced by CacheFix (cf. “% actions” in Table 2) with respect to the total
number of instructions executed. We observe that the maximum overhead reaches up to 3.2% and the average overhead is up to 2.1%. We believe this overhead is acceptable in the light of cache side-channel freedom guarantees provided by CacheFix.

Except AES and DES, the cache behaviour of a single program path is independent of program inputs. For the respective subjects, exactly the same number of equivalence classes were explored for both attack models (cf. Table 2). Each explored equivalence class was primarily attributed to a unique program path. Nevertheless, due to more involved computations (cf. Section 5), the overhead of CacheFix in attack model $O_{\text{trace}}$ is higher than the overhead in attack model $O_{\text{time}}$. As observed from Table 2, CacheFix discovers significantly more equivalence classes w.r.t. attack model $O_{\text{trace}}$ as compared to the number of equivalence classes w.r.t. attack model $O_{\text{time}}$. This implies AES is more vulnerable to $O_{\text{trace}}$ as compared to $O_{\text{time}}$. Excluding DES subject to $O_{\text{trace}}$, our exploration terminates in all scenarios within 20 mins.

To explore counterexample and generate patches, CacheFix takes 2.72x more time with $O_{\text{trace}}$ as compared to $O_{\text{time}}$. Moreover, excluding DES, CacheFix explores all equivalence classes of observations within 20 minutes in all scenarios. Finally, the runtime overhead induced by CacheFix is only up to 3.2% with respect to the number of executed instructions.

**Sensitivity w.r.t. cache configuration.** We evaluated CacheFix for a variety of cache associativity (1-way, 2-way and 4-way), cache size (from 1KB to 8KB) and with LRU as well as FIFO replacement policies (detailed experiments are included in the appendix). We observed that the verification time increases marginally (about 7%) when set-associative caches were used instead of direct-mapped caches and does not vary significantly with respect to replacement policy. Finally, we observed changes in the number of equivalence classes of observations for both AES and DES while running these subjects with different replacement policies. However, neither AES nor DES satisfied cache side-channel freedom for any of the cache size and replacement policies tested in our evaluation. The relatively low verification time results from the fact that the total number of predicates (i.e. $|\text{Pred}_{\text{set}} \cup \text{Pred}_{\text{tag}}|$) is independent of cache size and replacement policy. Nevertheless, the symbolic encoding for set-associative caches is more involved than direct-mapped caches. This results in an average increase to the number of predicates considered for verification (i.e. $\text{Pred}_{\text{cur}}$) by a factor of 1.5x. However, such
an increased number of predicates does not translate to significant verification timing for set-associative caches.

7 REVIEW OF PRIOR WORKS

Earlier works on cache analysis are based on abstract interpretation [35] and its combination with model checking [18], to estimate the worst-case execution time (WCET) of a program. In contrast to these approaches, CACHEFIX automatically builds and refines the abstraction of cache semantics for verifying set-channel freedom. Cache attacks are one of the most critical side-channel attacks [8, 14, 25–28, 32, 37, 38]. In contrast to the literature on side-channel attacks, we do not engineer new cache attacks in this paper. Based on a configurable attack model, CACHEFIX verifies and reinstates the cache side-channel freedom of arbitrary programs.

Orthogonal to approaches proposing countermeasures [21, 36], the fixes generated by CACHEFIX is guided by program verification output. Thus, CACHEFIX can provide cache side-channel freedom guarantees about the fixed program. Moreover, CACHEFIX can be leveraged to formally verify whether existing countermeasures are capable to ensure side-channel freedom.

In contrast to recent approaches on statically analyzing cache side channels [15, 22, 29, 30], our CACHEFIX approach automatically constructs and refines the abstractions for verifying cache side-channel freedom. Moreover, contrary to CACHEFIX, approaches based on static analysis are not directly applicable when the underlying program does not satisfy cache-side-channel freedom. CACHEFIX targets verification of arbitrary software programs, over and above constant-time implementations [9, 12]. Existing works based on symbolic execution [11, 34], taint analysis [20, 33] and verifying timing-channel freedom [10] ignore cache attacks. Moreover, these works do not provide capabilities for automatic abstraction refinement and patch synthesis for ensuring side-channel freedom. Finally, in contrast to these works, we show that our CACHEFIX approach scales with routines from real cryptographic libraries.

Finally, recent approaches on testing and quantifying cache side-channel leakage [13, 16, 17] are complementary to CACHEFIX. These works have the flavour of testing and they do not provide capabilities to ensure cache side-channel freedom.

8 DISCUSSION

In this paper, we propose CACHEFIX, a novel approach to automatically verify and restore cache side-channel freedom of arbitrary programs. The key novelty in our approach is two fold. Firstly, our CACHEFIX approach automatically builds and refines abstraction of cache semantics. Although targeted to verify cache side-channel freedom, we believe CACHEFIX is applicable to verify other cache timing properties, such as WCET. Secondly, the core symbolic engine of CACHEFIX systematically combines its reasoning power with runtime monitoring to ensure cache side-channel freedom during program execution. Our evaluation reveals promising results, for 25 routines from several cryptographic libraries, CACHEFIX (dis)proves cache side-channel freedom within an average 75 seconds. Moreover, in most scenarios, CACHEFIX generated patches within 20 minutes to ensure cache side-channel freedom during program execution. Despite this result, we believe that CACHEFIX is only an initial step for the automated verification of cache side-channel freedom. In particular, we do not account cache attacks that are more powerful than timing or trace-based attacks. Besides, we do not implement the synthesized patches in a commodity embedded system to check their performance impact. We hope that the community will take this effort forward and push the adoption of formal tools for the evaluation of cache side-channel. For reproducibility and research, our tool and all experimental data are publicly available: (blinded)

REFERENCES

[1] [n. d.]. CBMC: Bounded Model Checking for Software. (n. d.). http://www.cprover.org/cbmc/ (Date last accessed 23-October-2017).
[2] [n. d.]. FourQLib Library. (n. d.). https://github.com/Microsoft/FourQlib/ (Date last accessed 20-October-2017).
[3] [n. d.]. GDK Library. (n. d.). https://developer.gnome.org/gdk3/3.22/ (Date last accessed 20-October-2017).
[4] [n. d.]. A library for doing constant-time fixed-point numeric operations. (n. d.). https://github.com/kmowery/lbibt8edelim/timedpoint/ (Date last accessed 20-October-2017).
[5] [n. d.]. OpenSSL Library. (n. d.). https://github.com/openssl/openssl/ (Date last accessed 20-October-2017).
[6] [n. d.]. SSW Library. (n. d.). https://github.com/mengyao/Complete-Striped-Smith-Waterman-Library (Date last accessed 23-October-2017).
[7] [n. d.]. Symbolic Verification of Cache Side-channel Freedom. (n. d.). https://github.com/esswek2018/esswek2018/eblob/master/cachefix_supplement.pdf.
[8] Orur Acıncımez and Cetin Kaya Koç. 2006. Traced-cache attacks on AES. In Information and Communications Security. Springer.
[9] Josè Bacelar Almeida, Manuel Barbosa, Gilles Barthe, François Dupressoir, and Michael Emmi. 2016. Verifying Constant-Time Implementations. In USENIX 53–70.
[10] Timos Antonopoulos, Paul Gazzillo, Michael Hicks, Eric Koskinen, Tachiyo Teranishi, and Shiyi Wei. 2017. Decomposition instead of self-composition for proving the absence of timing channels. In PLDI. 362–375.
[11] Michael Backes, Boris Köpf, and Andrey Rybalchenko. 2009. Automatic Discovery and Quantification of Information Leaks. In IEEE S&P. 141–153.
[12] Gilles Barthe, Gustavo Betarte, Juan Diego Campo, Carlos Daniel Luna, and David Pichardie. 2014. System-level Non-interference for Constant-time Cryptography. In CCS. 1267–1279.
[13] Tiyas Basu and Sudipta Chattopadhyay. 2017. Testing Cache Side-Channel Leakage. In FSTTCS. 51–60.
[14] Daniel J Bernstein. 2005. Cache-timing attacks on AES. (2005).
[15] Pablo Cañones, Boris Köpf, and Jan Reineke. 2017. Security Analysis of Cache Replacement Policies. In POST. 189–209.
[16] Sudipta Chattopadhyay. 2017. Directed Automated Memory Performance Testing. In TACAS. 38–55.
[17] Sudipta Chattopadhyay, Moritz Beck, Ahmed Rezine, and Andreas Zeller. 2017. Quantifying the information leak in cache attacks via symbolic execution. In MEMOCODE. 25–35.
[18] Sudipta Chattopadhyay and Abhik Roychoudhury. 2013. Scalable and precise refinement of cache timing analysis via path-sensitive verification. Real-Time Systems 49, 4 (2013), 517–562.
[19] Michael Gruss, Raphael Spreitzer, and Stefan Mangard. 2015. Cache Template Attacks: Automating Attacks on Inclusive Last-Level Caches. In USENIX Security.
[20] Sudipto Guanciale, Hamed Nemati, Christoph Raumann, and Mads Dam. 2016. Cache Storage Channels: Alias-Driven Attacks and Verified Countermeasures. In IEEE Symposium on Security and Privacy. 38–55.
After one round of patch synthesis, assume that the channel capacity to distinguish undue influence is \( \log |O(\mathcal{T}_0)| - \log |O(\mathcal{T}_1)| + 1 \) (27)

Channel capacity \( G_{\mathcal{P}}^{\text{cap}} \) equals to \( \log |O(\mathcal{T}_0)| \) for the original program \( \mathcal{P} \), but it reduces to \( \log |O(\mathcal{T}_1)| \) when the synthesized patches are applied. We conclude the proof as the same argument holds for any round of patch synthesis.

**Property 4. (Convergence)** Let us assume a variant program \( \mathcal{P} \) with sensitive input \( \mathcal{K} \). In the absence of any attacker, assume that the uncertainty to guess \( \mathcal{K} \) is \( G_{\mathcal{P}}^{\text{init}} \). If our checker terminates and all synthesized patches are applied at runtime, then our framework guarantees that the channel capacity (respectively, Shannon entropy and Min entropy) will remain \( G_{\mathcal{P}}^{\text{init}} \) (respectively, \( G_{\mathcal{shn}}^{\text{init}} \) and \( G_{\mathcal{min}}^{\text{init}} \) even in the presence of attacks captured via \( O_{\text{time}} \) and \( O_{\text{trace}} \).

**Proof.** Consider the generic attack model \( O : \{h, m\}^* \rightarrow \mathbb{X} \), mapping each execution trace to an element in the countable set \( \mathbb{X} \).

We assume a victim program \( \mathcal{P} \) that exhibits a set of execution traces \( \mathcal{T}_R \subseteq \{h, m\}^* \). From Equation 27, we know that \( |O(\mathcal{T}_R)| \) decreases with each round of patch synthesis. Given that our checker terminates, we obtain the program \( \mathcal{P} \), together with a set of synthesized patches that are applied when \( \mathcal{P} \) executes. Assume \( \mathcal{T}_R' \subseteq \{h, m\}^* \) is the set of execution traces obtained from \( \mathcal{P} \) when all patches are systematically applied. Clearly, \( |O(\mathcal{T}_R')| = 1 \).

The channel capacity of \( \mathcal{P} \), upon the termination of our checker, is \( \log |O(\mathcal{T}_R')| = \log 1 = 0 \). This concludes that the channel capacity does not change even in the presence of attacks \( O_{\text{time}} \) and \( O_{\text{trace}} \).

For a given distribution \( \lambda \) of sensitive input \( \mathcal{K} \), Shannon entropy \( G_{\mathcal{shn}}^{\text{init}} \) is computed as follows:

\[
G_{\mathcal{shn}}^{\text{init}}(\lambda) = - \sum_{K \in \mathbb{X}} \lambda(K) \log_2 \lambda(K) \quad (28)
\]

where \( \mathbb{X} \) captures the domain of sensitive input \( \mathcal{K} \). For a given equivalence class of observation \( o \in O(\mathcal{T}_R') \), the remaining uncertainty is computed as follows:

\[
G_{\mathcal{shn}}^{\text{final}}(\lambda_o) = - \sum_{K \in \mathbb{X}} \lambda_o(K) \log_2 \lambda_o(K) \quad (29)
\]

\( \lambda_o(K) \) captures the probability that the sensitive input is \( \mathcal{K} \), given the observation \( o \) is made by the attacker. Finally, to evaluate the remaining uncertainty of the patched program version, \( G_{\mathcal{shn}}^{\text{final}}(\lambda_o) \) is averaged over all equivalence class of observations as follows:

\[
G_{\mathcal{shn}}^{\text{final}}(\lambda) = \sum_{o \in O(\mathcal{T}_R')} pr(o) G_{\mathcal{shn}}^{\text{final}}(\lambda_o) \quad (30)
\]

where \( pr(o) \) captures the probability of the observation \( o \in O(\mathcal{T}_R') \).

However, we have \( |O(\mathcal{T}_R')| = 1 \). Hence, for any \( o \in O(\mathcal{T}_R') \), we get \( pr(o) = 1 \) and \( \lambda_o(K) = \lambda(K) \). Plugging these observations into Equation 30 and Equation 29, we get the following:

\[
G_{\mathcal{shn}}^{\text{final}}(\lambda) = \sum_{o \in O(\mathcal{T}_R')} G_{\mathcal{shn}}^{\text{final}}(\lambda_o) = \sum_{o \in O(\mathcal{T}_R')} G_{\mathcal{shn}}^{\text{final}}(\lambda_o) = \sum_{o \in O(\mathcal{T}_R')} \lambda(K) \log_2 \lambda(K) = G_{\mathcal{shn}}^{\text{init}}(\lambda) \quad (31)
\]

Finally, for a given distribution \( \lambda \) of sensitive input \( \mathcal{K} \), the min entropy \( G_{\mathcal{min}}^{\text{init}} \) is computed as follows:

\[
G_{\mathcal{min}}^{\text{init}}(\lambda) = - \log_2 \max_{K \in \mathbb{X}} \lambda(K) \quad (32)
\]

Therefore, min entropy captures the best strategy of an attacker, that is, to choose the most probable secret.

**APPENDIX**

The appendix includes additional cache models (e.g. LRU and FIFO) incorporated within CACHEFIX, the theoretical guarantees and additional experimental results.

**Theoretical Guarantees**

In this section, we include the detailed proof of the properties satisfied by CACHEFIX.

**Property 3. (Monotonicity)** Consider a victim program \( \mathcal{P} \) with sensitive input \( \mathcal{K} \). Given attack models \( O_{\text{time}} \) or \( O_{\text{trace}} \), assume that the channel capacity to quantify the uncertainty of guessing \( \mathcal{K} \) is \( G_{\mathcal{P}}^{\text{cap}} \). CacheFix guarantees that \( G_{\mathcal{P}}^{\text{cap}} \) monotonically decreases with each synthesized patch (cf. Equation 25-26) employed at runtime.

**Proof.** Consider the generic attacker model \( O : \{h, m\}^* \rightarrow \mathbb{X} \) that maps each trace to an element in the countable set \( \mathbb{X} \). For a victim program \( \mathcal{P} \), assume \( \mathcal{T}_R \subseteq \{h, m\}^* \) is the set of all execution traces. After one round of patch synthesis, assume \( \mathcal{T}_R' \subseteq \{h, m\}^* \) is the set of all execution traces in \( \mathcal{P} \) when the synthesized patches are applied at runtime. By construction, each round of patch synthesis merges two equivalence classes of observations (cf. Algorithm 3), hence, making them indistinguishable by the attacker \( O \). As a result, the following relationship holds:

\[
|O(\mathcal{T}_R)| = |O(\mathcal{T}_R')| + 1 \quad (27)
\]

Channel capacity \( G_{\mathcal{P}}^{\text{cap}} \) equals to \( \log |O(\mathcal{T}_R)| \) for the original program \( \mathcal{P} \), but it reduces to \( \log |O(\mathcal{T}_R')| \) when the synthesized patches are applied. We conclude the proof as the same argument holds for any round of patch synthesis.

**Property 4. (Convergence)** Let us assume a victim program \( \mathcal{P} \) with sensitive input \( \mathcal{K} \). In the absence of any attacker, assume that the uncertainty to guess \( \mathcal{K} \) is \( G_{\mathcal{init}}^{\text{shn}} \). We conclude the proof as the same argument holds for any round of patch synthesis.

Finally, for a given distribution \( \lambda \) of sensitive input \( \mathcal{K} \), the min entropy \( G_{\mathcal{min}}^{\text{init}} \) is computed as follows:

\[
G_{\mathcal{min}}^{\text{init}}(\lambda) = - \log_2 \max_{K \in \mathbb{X}} \lambda(K) \quad (32)
\]

Therefore, min entropy captures the best strategy of an attacker, that is, to choose the most probable secret.
Similar to Shannon entropy, for a given equivalence class of observation \( o \in O(\mathcal{TR}') \), the remaining uncertainty is computed as follows:

\[
G_{\text{min}}^{\text{init}}(\lambda_o) = -\log_2 \max_{\mathcal{K} \in \mathcal{K}} \lambda_o(\mathcal{K}) \quad (33)
\]

\( \lambda_o(\mathcal{K}) \) captures the probability that the sensitive input is \( \mathcal{K} \), given the observation \( o \) is made by the attacker.

Finally, we obtain the min entropy of the patched program version via the following relation:

\[
G_{\text{min}}^{\text{final}}(\lambda_{\mathcal{O}(\mathcal{TR}'))} = -\log_2 \sum_{o \in O(\mathcal{TR}')} \max_{\mathcal{K} \in \mathcal{K}} \lambda_o(\mathcal{K}) \quad (34)
\]

Since \( pr(o) = 1 \) and \( \lambda_o(\mathcal{K}) = \lambda(\mathcal{K}) \) for any \( o \in O(\mathcal{TR}') \), we get the following from Equation 34 and Equation 33:

\[
G_{\text{min}}^{\text{final}}(\lambda_{\mathcal{O}(\mathcal{TR}'))} = -\log_2 \sum_{o \in O(\mathcal{TR}')} \lambda(\mathcal{K}) \quad (35)
\]

Equation 31 and Equation 35 conclude this proof.

\[ \square \]

Modeling LRU and FIFO cache semantics

To formulate the conditions for conflict misses in set-associative caches, it is necessary to understand the notion of cache conflict. We use the following definition of cache conflict to formulate \( \Gamma(r_j) \):

**Definition 1.** (Cache conflict) \( r_j \) generates a cache conflict to \( r_i \) if and only if \( 1 \leq j < i \), \( \sigma(r_j) \neq \sigma(r_i) \) and the execution of \( r_j \) can change the relative position of \( \sigma(r_i) \) within the set(\( r_i \))-state immediately before instruction \( r_j \).

Recall that \( \sigma(r_i) \) captures the memory block accessed at \( r_i \) and set(\( r_i \)) captures the cache set accessed by \( r_i \). The state of a cache set is an ordered \( \mathcal{A} \)-tuple – capturing the relative positions of all memory blocks within the respective cache set. For instance, \( \{m_1, m_2\} \) captures the state of a two-associative cache set. The rightmost memory block (i.e., \( m_2 \)) captures the first memory block to be evicted from the cache set if a block \( m \notin \{m_1, m_2\} \) is accessed and mapped to the same cache set.

**Challenges with LRU policy.** To illustrate the unique challenges related to set-associative caches, let us consider the following sequence of memory accesses in a two-way associative cache and with LRU replacement policy: \( (r_1 : m_1) \rightarrow (r_2 : m_2) \rightarrow (r_3 : m_1) \rightarrow (r_4 : m_1) \). We assume both \( m_1 \) and \( m_2 \) are mapped to the same cache set. If the cache is empty before \( r_1 \), \( r_4 \) will still incur a cache hit. This is because, \( r_4 \) suffers cache conflict only once, from the memory block \( m_2 \). To incorporate the aforementioned phenomenon into our cache semantics, we only count cache conflicts from the closest access to a given memory block. Therefore, in our example, we count cache conflicts to \( r_4 \) from \( r_3 \) and discard the cache conflict from \( r_2 \). Formally, we introduce the following additional condition for instruction \( r_j \) to inflict a cache conflict to instruction \( r_i \):

\[ \phi_{ji}^{\text{eqv, lru}} : \text{No instruction between } r_j \text{ and } r_i \text{ accesses the same memory block as } r_j. \]

This is to ensure that \( r_j \) is the closest to \( r_i \) in terms of accessing the memory block \( \sigma(r_j) \). We capture \( \phi_{ji}^{\text{eqv, lru}} \) formally as follows:

\[
\phi_{ji}^{\text{eqv, lru}} = \bigwedge_{j < k < i} \left( \rho_{jk}^{\text{tag}} \lor \rho_{jk}^{\text{set}} \lor \neg \text{guard}_k \right) \quad (36)
\]

Hence, \( r_j \) inflicts a unique cache conflict to \( r_i \) only if \( \phi_{ji}^{\text{eqv, lru}} \), \( \phi_{ji}^{\text{conf, lru}} \), \( \phi_{ji}^{\text{conf, dir}} \), \( \phi_{ji}^{\text{rel, lru}} \), \( \phi_{ji}^{\text{rel, dir}} \) are all satisfiable.

**Challenges with FIFO policy.** Unlike LRU replacement policy, the cache state does not change for a cache hit in FIFO replacement policy. For example, consider the following sequence of memory accesses in a two-way associative FIFO cache: \( (r_1 : m_1) \rightarrow (r_2 : m_2) \rightarrow (r_3 : m_1) \rightarrow (r_4 : m_1) \). Let us assume \( m_1 \), \( m_2 \) map to the same cache set and the cache is empty before \( r_1 \). In this example, \( r_2 \) generates a cache conflict to \( r_4 \) even though \( m_1 \) is accessed between \( r_2 \) and \( r_4 \). This is because \( r_3 \) is a cache hit and it does not change cache states.

In general, to formulate \( \Gamma(r_j) \), we need to know whether any instruction \( r_j \) prior to \( r_i \), was a cache miss. This, in turn, is captured via \( \Gamma(r_j) \). Concretely, \( r_j \) generates a unique cache conflict to \( r_i \) if all the following conditions are satisfied:

\[ \phi_{ji}^{\text{eqv, fifo}} : \text{If } r_j \text{ accesses the same cache set as } r_i, \text{but accesses a different cache-tag as compared to } r_i \text{ and } r_j \text{ suffers a cache miss. This is formalized as follows:}
\]

\[
\phi_{ji}^{\text{conf, fifo}} = \phi_{ji}^{\text{eqv, fifo}} \land \phi_{ji}^{\text{conf, dir}} \land \phi_{ji}^{\text{rel, fifo}} \land \phi_{ji}^{\text{rel, dir}} \quad (37)
\]

\[ \phi_{ji}^{\text{rel, fifo}} : \text{No cache miss between } r_j \text{ and } r_i \text{ access the same memory block as } r_i. \phi_{ji}^{\text{rel, fifo}} \text{ ensures that the relative position of the memory block } \sigma(r_j) \text{ within set}(r_i) \text{ was not reset between } r_j \text{ and } r_i.
\]

\[ \phi_{ji}^{\text{rel, dir}} = \bigwedge_{j < k < i} \left( \rho_{kj}^{\text{tag}} \lor \rho_{kj}^{\text{set}} \lor \neg \text{guard}_k \lor \neg \Gamma(k) \right) \quad (38)
\]

\[ \phi_{ji}^{\text{eqv, fifo}} : \text{No cache miss between } r_j \text{ and } r_i \text{ access the same memory block as } r_j. \phi_{ji}^{\text{eqv, fifo}} \text{ ensures that } r_j \text{ is the closest cache miss to } r_i \text{ accessing the memory block } \sigma(r_j). \text{This, in turn, ensures that we count the cache conflict from memory block } \sigma(r_j) \text{ to instruction } r_j \text{ only once. We formulate } \phi_{ji}^{\text{eqv, fifo}} \text{ as follows:}
\]

\[
\phi_{ji}^{\text{eqv, fifo}} = \bigwedge_{j < k < i} \left( \rho_{jk}^{\text{tag}} \lor \rho_{jk}^{\text{set}} \lor \neg \text{guard}_k \lor \neg \Gamma(k) \right) \quad (39)
\]

**Formulating cache conflict in set-associative caches.**

With the intuition mentioned in the preceding paragraphs, we formalize the unique cache conflict from \( r_j \) to \( r_i \) via the following logical conditions:

\[
\Theta_{i,j}^{+, x} = \left( \phi_{ji}^{\text{conf, x}} \land \phi_{ji}^{\text{rel, x}} \land \phi_{ji}^{\text{eqv, x}} \land \text{guard} \right) \Rightarrow (\eta_{ji} = 1) \quad (40)
\]
where \( x = \{\text{tru}, \text{fals}\} \). Concretely, \( \eta_{ji} \) is set to 1 if \( r_j \) creates a unique cache conflict to \( r_i \) and \( \eta_{ji} \) is set to 0 otherwise.

**Computing \( \Gamma(r_j) \) for Set-associative Caches.** To formulate \( \Gamma(r_j) \) for set-associative caches, we need to check whether the number of unique cache conflicts to \( r_j \) exceeds the associativity (\( A \)) of the cache. Based on this intuition, we formalize \( \Gamma(r_j) \) for set-associative caches as follows:

\[
\Gamma(r_j) \equiv \text{guard}_{\cdot} \land \left( \text{\textit{guard}}_{\cdot}^\textit{old} \lor \left( \sum_{j \in [1..i]} \eta_{ji} \geq A \right) \right)
\]

(42)

We note that \( \sum_{j \in [1..i]} \eta_{ji} \) accurately counts the number of unique cache conflicts to the instruction \( r_j \) (cf. Equation 40-Equation 41). Hence, the condition \( \sum_{j \in [1..i]} \eta_{ji} \geq A \) precisely captures whether \( \sigma(r_j) \) is replaced from the cache before \( r_i \) is executed. If \( r_j \) does not suffer a cold miss and \( \sum_{j \in [1..i]} \eta_{ji} < A \), then \( r_i \) will be a cache hit when executed, as captured by the condition \( \neg \Gamma(r_j) \).

**Detailed Runtime Monitoring**

Algorithm 3 outlines the overall process. The procedure \textsc{Monitoring} takes the following inputs:

- \( \Psi \): A symbolic representation of program and cache semantics with the current level of abstraction,
- \( O \) and \( \varphi \): The model of the attacker (\( O \)) and a property \( \varphi \) initially capturing cache side-channel freedom w.r.t. \( O \),
- \( \text{Pred} \) and \( \text{Pred}_{\text{cur}} \): Cache semantics related predicates (\( \text{Pred} \)) and the current level of abstraction (\( \text{Pred}_{\text{cur}} \)), and
- \( \Gamma \): Symbolic conditions to determine the cache behaviour.

**Additional Experimental Results**

**Sensitivity w.r.t. cache.** Figure 4 outlines the evaluation for routines that violate side-channel freedom and for attack model \( O_{\text{time}} \). Nevertheless, the holds for all routines and attack models. Figure 4 captures the number of equivalence classes explored (hence, the number of patches generated cf. Algorithm 3) with respect to time. We make the following crucial observations from Figure 4. Firstly, the scalability of our checker is stable across a variety of cache configurations. This is because we encode cache semantics within a program via symbolic constraints on cache conflict.

The size of these constraints depends on the number of memory-related instructions, but its size is not heavily influenced by the size of the cache. Secondly, the number of equivalence classes of observations does not vary significantly across cache configurations. Indeed, the number of equivalence classes may even increase (hence, increased channel capacity) with a bigger cache size (e.g. in DES and AES). However, for all cache configurations, \textsc{CacheFix} generated all the patches that need to be applied for making the respective programs cache side-channel free.

The scalability of \textsc{CacheFix} is stable across a variety of cache configurations. Moreover, in all cache configurations, \textsc{CacheFix} generated all required patches to ensure the cache side-channel freedom w.r.t. \( O_{\text{time}} \).

**Algorithm 3 Monitor extraction and instrumentation**

1: \textbf{procedure} \textsc{Monitoring}(\( \Psi, O, \varphi, \text{Pred}, \text{Pred}_{\text{cur}}, \Gamma \))
2: /* If \( \varphi \) captures side-channel freedom, then \( \text{trace} \) is
3: any of the two traces constituting the counterexample */
4: \( \text{res, trace} \) := \textsc{VERIFY}(\( \Psi, \varphi \))
5: \textbf{while} (\( \text{res} = \text{false} \) \land (\( \text{trace} \) \neq \text{spurious})) \textbf{do}
6: /* Extract observation from \( \text{trace} \) */
7: \( \nu \) := \textsc{GetObservation}(\( \text{trace} \))
8: /* Extract monitor from \( \text{trace} \) */
9: \( \nu_{\text{a}} := \nu := \textsc{ExtractMonitor}(\text{trace}) \)
10: /* Refine \( \Psi \) to find unique counterexamples */
11: \( \Psi := \Psi \land \neg \nu \)
12: /* Refine \( \varphi \) to find all traces exhibiting \( \sigma \) */
13: \( \varphi := \textsc{RefineObjective}(\sigma, O) \)
14: /* Check the unsatisfiability of \( \Psi \land \neg \varphi \) */
15: \( \text{res}^{\prime}, \text{trace}^{\prime} \) := \textsc{VERIFY}(\( \Psi, \varphi \))
16: \textbf{while} (\( \text{res}^{\prime} = \text{false} \)) \textbf{do}
17: /* If \( \text{trace}^{\prime} \) is not \( \text{spurious} \) */
18: \( \nu := \textsc{ExtractMonitor}(\text{trace}^{\prime}) \)
19: /* Combine monitors with observation \( \sigma \) */
20: \( \nu_{\text{a}} := \nu_{\text{a}} \lor \nu \)
21: /* Refine \( \Psi \) for unique counterexamples */
22: \( \Psi := \Psi \land \neg \nu \)
23: /* Check the unsatisfiability of \( \Psi \land \neg \varphi \) */
24: \( \text{res}^{\prime}, \text{trace}^{\prime} \) := \textsc{VERIFY}(\( \Psi, \varphi \))
25: \textbf{else}
26: /* Refine abstraction to repeat verification */
27: \textsc{AbsRefine}(\( \Psi, \text{Pred}, \text{Pred}_{\text{cur}}, \text{trace}^{\prime}, \Gamma \))
28: \( \text{res}^{\prime}, \text{trace}^{\prime} \) := \textsc{VERIFY}(\( \Psi, \varphi \))
29: \textbf{end if}
30: \textbf{end while}
31: Let \( \Omega \) holds the set of monitor, observation pairs
32: \( \Omega := \{ (\nu_{\text{a}}, O) \} \)
33: /* Instrument patches for monitor \( \nu_{\text{a}} \) */
34: \textsc{InstrumentPatch}(\( \Omega, O \))
35: /* Refine objective to find new observations */
36: \( \varphi := \neg \varphi \)
37: /* Check the unsatisfiability of \( \Psi \land \neg \varphi \) */
38: \( \text{res, trace} \) := \textsc{VERIFY}(\( \Psi, \varphi \))
39: \textbf{end while}
40: /* Program is still not side-channel free */
41: /* Refine abstraction to repeat verification loop */
42: \textbf{if} (\( \text{res} = \text{false} \)) \textbf{then}
43: \textsc{AbsRefine}(\( \Psi, \text{Pred}, \text{Pred}_{\text{cur}}, \text{trace}, \Gamma \))
44: \textsc{Monitoring}(\( \Psi, O, \varphi, \text{Pred}, \text{Pred}_{\text{cur}}, \Gamma \))
45: \textbf{end if}
46: \textbf{end procedure}
47: \textbf{procedure} \textsc{AbsRefine}(\( \Psi, \text{Pred}, \text{Pred}_{\text{cur}}, \text{trace}, \Gamma \))
48: /* Extract unsatisfiable core */
49: \( \mathcal{U} := \textsc{UnsatCore}(\text{trace}, \Gamma) \)
50: /* Refine abstractions (see Section 4) */
51: \textsc{Pred}_{\text{cur}} := \textsc{Refine}(\text{Pred}_{\text{cur}}, \mathcal{U}, \text{Pred})
52: /* Rewrite \( \Psi \) with the refined abstraction */
53: \textsc{Rewrite}(\( \Psi, \text{Pred}_{\text{cur}} \))
54: \textbf{end procedure}
Figure 3: Overhead of counterexample exploration and patch synthesis

Figure 4: CACHEFIX sensitivity w.r.t. cache