Simplified Space-Vector Modulation Strategy for Indirect Matrix Converter With Common-Mode Voltage and Harmonic Distortion Reduction

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\textbf{ABSTRACT} This paper presents a simple space vector modulation (SVM) strategy for a three-phase indirect matrix converter (IMC) to reduce common-mode voltage (CMV) and output harmonic distortion. To suppress the CMV peak value to 57.7\% of the input phase voltage, three active voltage vectors are used to generate the desired output voltage with arbitrary amplitude and frequency. However, the output waveform quality of the IMC deteriorates due to the absence of zero voltage vectors. To overcome this problem, this paper proposes to redesign control of the rectifier stage by utilizing three active current vectors instead of two, as is common. Consequently, a constant average DC-link voltage is achieved, which can improve the output performance in terms of output voltage and current harmonic distortion. Compared to the existing strategies, the proposed strategy can reduce the CMV and maintain output harmonic distortion without increasing the computation burden. Implementation of the proposed strategy is also straightforward and simple. Simulated and experimental results are provided to verify the effectiveness of the proposed strategy.

\textbf{INDEX TERMS} Indirect matrix converter, space-vector modulation, common-mode voltage, output harmonic distortion.

\section{I. INTRODUCTION}

In general, matrix converter (MC) technology has been discussed as an all-silicon approach for motor drive applications because it lacks a large energy storage system [1]–[3]. After nearly four decades of research efforts, MC technology has received considerable attention as a viable alternative to traditional voltage source inverter (VSI) technology [4]. MC technology provides many advantages, including sinusoidal input/output current waveforms, bidirectional power flow, a controllable input power factor, and a simple and compact power design. MC topology is often classified into direct matrix converters (DMC) and indirect matrix converters (IMC), which correspond to its one-stage and two-stage characteristics, respectively. IMC and DMC have similar input and output performances. However, IMC can offer additional benefits that are not available in DMC, such as simpler clamp circuits for over-voltage protection, zero-current commutation, and flexible structures. Recently, the IMC, as shown in Fig. 1, has received more attention than the DMC [5]–[8].

Despite the advantages of MC technology, its industrial application has not met its potential due to several technical issues. MC technology has suffered from problems associated with common-mode voltage (CMV), like other pulse width modulation (PWM) converters. As reported in

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure1}
\caption{Topology of a three-phase IMC.}
\end{figure}
the literature, CMV with a high frequency and a high \(dv/dt\) will be produced when the PWM technique is used to control the MC. The CMV is the main source of early motor winding failures, motor bearing degradation, and electromagnetic interference [9], [10]. Thus, it is necessary to suppress the CMV in the MC topologies to prevent these problems.

Several modulation methods have been introduced to reduce the CMV for the three-phase IMC drive system. The majority of the methods are based on a near-state PWM technique that can effectively mitigate the peak value of the CMV by 42% of its original value [11]. Nguyen and Lee found that CMV reduction methods are based on replacing the zero voltage vectors with two opposite active voltage vectors and one nearest active voltage vector, respectively [12], [13]. Rahman et al. presented a space-vector modulation (SVM) method to reduce the CMV peak value by properly placing the zero vectors in the rectifier modulation, instead of placing the zero voltage vectors in the inverter modulation [14]. Wang et al. suggested a combination of model predictive control and SVM to decrease the CMV for the three-phase IMC topology [15]. Unfortunately, the quality of the output waveforms also deteriorated due to the absence of zero voltage vectors, which is a common trade-off between CMV reduction and output performance.

More recently, CMV reduction methods have been proposed to address the issues discussed above and to maintain the IMC output performance [16]–[19]. Padhee et al. proposed a modulation technique for CMV reduction and enhanced output voltage distortion by dividing the IMC operation into low and high voltage transfer ratio (VTR) ranges [16]. An additional algorithm is needed to combine the two modulation schemes. To avoid the need to separate the two operation ranges, Tsoupos and Khadikar suggested adding a weighing factor to create a seamless transition between the low and high VTR operation ranges [17]. Tran and Lee proposed a modulation method to reduce the CMV, the output voltage, and current harmonics distortions for a five-leg IMC fed open-end winding load [18]. Li et al. presented a new SVM method based on the concept of an open-current vector to suppress the CMV peak value without degrading the output performance [19]. Although these recent CMV reduction methods preserve the quality of the output voltage and current waveforms, they are also more complex. As a result of these complexities, MC development has been difficult.

To address these issues, this paper proposes a simplified SVM strategy to reduce the CMV and output harmonic distortion without increasing the complexity. In the proposed strategy, a unique three-vector switching technique successfully modulated the rectifier and inverter stages of the three-phase IMC. Three active voltage vectors are used for the inverter modulation to reduce the CMV. Three active current vectors are also used for the rectifier modulation to obtain a constant average DC-link voltage, which can improve the output performance. Consequently, the proposed SVM strategy can not only reduce the CMV but also maintain the output waveform quality and decrease the computational burden compared to existing methods. Simulation and experimental results are provided to evaluate the effectiveness of the proposed SVM strategy.

II. CONVENTIONAL SVM STRATEGY
The SVM strategy widely used to control the IMC was established by Wei and Lipo [20]. Assume that the rectifier stage is connected to a sinusoidal and balanced three-phase voltage source as follows:

\[
\begin{align*}
    v_a &= V_i \cos(\omega t) \\
    v_b &= V_i \cos(\omega t - 2\pi/3) \\
    v_c &= V_i \cos(\omega t + 2\pi/3)
\end{align*}
\]

where \(V_i\) and \(\omega t\) are the amplitude and angular frequency of the input phase voltage, respectively.

The modulation of the rectifier stage is based on the space vector analysis of the input voltage and current under the constraint of the unity input power factor. The space vectors of the input voltage and input current are described as follows:

\[
\begin{align*}
    \vec{v}_i &= \frac{2}{3} \left( v_a + v_b e^{2\pi i/3} + v_c e^{4\pi i/3} \right) = V_i e^{j\beta_i} \\
    \vec{i}_i &= \frac{2}{3} \left( i_a + i_b e^{2\pi i/3} + i_c e^{4\pi i/3} \right) = I_i e^{j\beta_i}
\end{align*}
\]

where \(I_i\) and \(\beta_i\) are the amplitude and phase angle of the input phase current, respectively.

Fig. 2 shows the space vector diagram, sector identification, and DC-link voltage waveform of the rectifier modulation. As shown in Fig. 2(a), the reference input current vector is composed of six active current vectors and three zero current vectors. Each vector represents the switching states of the upper and lower switches to the voltage source. For example, when the current vector \(\vec{i}_{ab}\) is used to synthesize the reference input current vector, the upper switch of phase \(a\), \(S_{ab}\), and the lower switch of phase \(c\), \(S_{cn}\), are connected to the positive pole and negative pole of the DC-link bus voltage, respectively.

To obtain the highest value of the DC-link voltage, the maximum and medium input line voltages are used to generate the DC-link voltage. Accordingly, the two nearest active current vectors are selected to produce the reference input current vector. For clarity, assume that the reference input current vector is in sector 1 \((-\pi/6 \leq \beta_i \leq \pi/6\) as shown in Fig. 2(a). Two vectors, \(\vec{i}_{ab}\) and \(\vec{i}_{ac}\), are then selected to synthesize the reference input current vector \(\vec{i}_i^*\) as follows:

\[
\vec{i}_i^* = d_{ab}\vec{i}_{ab} + d_{ac}\vec{i}_{ac}
\]

The duty ratios of two active vectors are calculated as:

\[
\begin{align*}
    d_{ab} &= m_i \sin \left( \pi / 6 - \beta_i \right) \\
    d_{ac} &= m_i \sin \left( \pi / 6 + \beta_i \right)
\end{align*}
\]

where \(m_i = I_i^*/I_{dc}\) is the rectifier modulation index, and \(I_{dc}\) is the average value of DC-link current.
The rectifier modulation index \( m_1 \) is typically kept at unity, and the zero current vectors are not used for the rectifier modulation to obtain the maximum DC-link voltage. Therefore, the duty ratios are recomputed to complete a switching period as follows:

\[
\begin{align*}
    d_{R1} &= \frac{d_{ab}}{d_{ab} + d_{ac}} = -\frac{\cos (\beta_1 - 2\pi/3)}{\cos \beta_1} = \frac{-v_b}{v_a} \\
    d_{R2} &= \frac{d_{ac}}{d_{ab} + d_{ac}} = -\frac{\cos (\beta_1 + 2\pi/3)}{\cos \beta_1} = \frac{-v_c}{v_a}.
\end{align*}
\]

The average value of the DC-link voltage \( \bar{V}_{dc} \) is calculated as follows:

\[
\bar{V}_{dc} = d_{R1} (v_a - v_b) + d_{R2} (v_a - v_c) = \frac{3V_i}{2\cos \beta_i}.
\]

As demonstrated by equation (6) and Fig. 2(b), the average value of the DC-link voltage \( \bar{V}_{dc} \) varies according to the maximum input line voltage, and its maximum and minimum values are given by:

\[
\bar{V}_{dc(max)} = \sqrt{3}V_i; \quad \bar{V}_{dc(min)} = \frac{3}{2}V_i.
\]

Meanwhile, the traditional SVM of a three-phase VSI while compensating the effect of the DC-link voltage variation can be applied to control the inverter stage. The SVM of the inverter stage is based on the space vector analysis of the output voltage. The space vector of the output voltage is described as follows:

\[
\bar{v}_o = \frac{2}{3} (v_A + v_B e^{2\pi j/3} + v_C e^{4\pi j/3}) = V_o e^{j\alpha_o}
\]

The space vector diagram of the inverter stage is composed of six active vectors (\( \bar{v}_1 \sim \bar{v}_6 \)) and two zero vectors (\( \bar{v}_0, \bar{v}_7 \)), as shown in Fig. 3. Each voltage vector refers to the connection state of the output phase voltage to the DC-link. For clarity, assume that the reference output voltage vector is in sector 1 \( (0 \leq \alpha_o \leq \pi/3) \). In this sector, the active vectors, \( \bar{v}_1, \bar{v}_2 \), and two zero vectors, \( \bar{v}_0, \bar{v}_7 \), are used to generate the desired output voltage:

\[
\bar{v}_o = d_{I1}\bar{v}_0 + d_{I2}\bar{v}_1 + d_{I2}\bar{v}_2 + d_{I7}\bar{v}_7
\]

The corresponding duty ratios are given as follows:

\[
\begin{align*}
    d_{I1} &= \sqrt{3} m_o \sin (\pi/3 - \alpha_o) \\
    d_{I2} &= \sqrt{3} m_o \sin (\alpha_o) \\
    d_{I0} &= d_{I7} = \frac{1}{2} (1 - d_{I1} - d_{I2})
\end{align*}
\]

where \( m_o = V_o/\bar{V}_{dc} \) is the inverter stage modulation index.

In a three-phase IMC topology, the voltage transfer ratio (VTR) is defined as the ratio between the amplitude of the output voltage and the amplitude of the input voltage. As a result, the maximum value of the VTR is given as:

\[
q_{max} = \frac{V_{o(max)}}{V_i} = \frac{V_{o(max)}}{\bar{V}_{dc}} \cdot \frac{\bar{V}_{dc}}{V_i} = \sqrt{3} \cdot \frac{3}{2} = \frac{\sqrt{3}}{2} = 0.866
\]

The IMC switching pattern should satisfy the constraints that minimize the number of commutations in each switching period as well as a symmetrical arrangement to achieve low output harmonic distortion. Furthermore, to obtain a balanced input current and output voltage, the rectifier switching event should be synchronized with that of the inverter. To put these in perspective, the IMC switching pattern is organized as shown in Fig. 4 when the reference input current and output voltage vectors are in sector 1.
The CMV in a three-phase system is defined as the voltage difference between the motor neutral point (N) and the ground point of the power supply (O), as shown in Fig. 5. The leakage impedance, $Z_L$, represents the leakage current path in the AC drive system. The CMV, $v_{cm}$, is expressed as follows:

$$v_{cm} = v_{NO}$$  \hspace{1cm} (13)

Then, CMV is derived from the output load as

$$v_A - v_{cm} = R_iA + L \left( \frac{di_A}{dt} \right)$$
$$v_B - v_{cm} = R_iB + L \left( \frac{di_B}{dt} \right)$$
$$v_C - v_{cm} = R_iC + L \left( \frac{di_C}{dt} \right)$$  \hspace{1cm} (14)

where $v_A$, $v_B$, and $v_C$ are the IMC output phase voltages to the ground, and $R$ and $L$ are the load resistance and inductance, respectively.

Under the balanced three-phase load, the sum of all three output currents becomes zero: $i_A + i_B + i_C = 0$. Therefore, the CMV is given as follows:

$$v_{cm} = \frac{v_A + v_B + v_C}{3}$$  \hspace{1cm} (15)

From equation (15), the CMV magnitude depends on the applied voltage vectors of the inverter modulation, and the CMV peak value is calculated as:

$$V_{cm,peak} = \begin{cases} V_i/\sqrt{3} & \text{group of 6 active vectors} \ (\vec{v}_1 \sim \vec{v}_6) \\ V_i & \text{group of 2 two vectors} \ (\vec{v}_0, \vec{v}_7) \end{cases}$$  \hspace{1cm} (16)

B. PROPOSED SVM FOR INVERTER STAGE TO REDUCE CMV

From equation (16), the CMV of the three-phase IMC is minimized when the group of six active vectors is applied to the inverter modulation. Therefore, if the output voltage is composed by using only active voltage vectors, the CMV will be reduced to its minimum value, or 57.7% of the input phase voltage amplitude. Because two active vectors and two zero vectors are selected in the conventional SVM strategy, it cannot reduce the CMV.

To reduce the CMV of the IMC, non-zero vector approaches are introduced to control the inverter stage. In other words, only active vectors are used to generate the desired output voltage [12], [13], [16], [18]. Among non-zero vector approaches, the near-state PWM technique is preferable over others due to its advantages, such as smaller total harmonic distortion (THD) of the line-to-line output voltage and low switching losses [11]. The near-state PWM technique uses the three nearest active vectors to the reference vector to synthesize the desired output voltage. Thus, the space vector diagram of the proposed strategy for the inverter modulation is redefined as shown in Fig. 6.

Without losing the generality of the analysis, assume that the desired output voltage is located in sector 1 ($-\pi/6 \leq \alpha_o \leq \pi/6$), three active vectors, $\vec{v}_1$, $\vec{v}_2$ and $\vec{v}_6$, are selected to compose the reference output voltage vector:

$$\vec{v}_o = d_{11}\vec{v}_1 + d_{12}\vec{v}_2 + d_{16}\vec{v}_6$$  \hspace{1cm} (17)
The corresponding duty ratios, $d_{l1}$, $d_{l2}$ and $d_{l6}$, are calculated as follows:

$$
\begin{align*}
    d_{l6} &= 1 - \frac{3}{2}m_v \cos(\alpha_o) - \frac{\sqrt{3}}{2}m_v \sin(\alpha_o) \\
    d_{l1} &= -1 + 3m_v \cos(\alpha_o) \\
    d_{l2} &= 1 - d_{l6} - d_{l1}
\end{align*}
$$

(18)

**C. PROPOSED SVM FOR RECTIFIER STAGE TO IMPROVE HARMONIC DISTORTION**

In the conventional SVM of the rectifier stage, the two nearest active current vectors are chosen to synthesize the reference input current vector. Although this method can provide the maximum DC-link voltage, the average value of the DC-link voltage $\bar{V}_{dc}$ changes six times within one input frequency cycle, as shown in Fig. 2. Therefore, if this value is used for the inverter modulation, the conventional strategy cannot provide excellent output performance due to the variability of the average value of the DC-link voltage. Moreover, the proposed SVM for the inverter stage can reduce the CMV effectively, but the output performance of the three-phase IMC declines due to the absence of zero voltage vectors.

To compensate for the degraded output performance, the rectifier stage SVM is redesigned by using three active current vectors to synthesize the reference input current, instead of two used in the conventional strategy. In other words, the average value of the DC-link voltage in the proposed strategy is maintained as a constant by using the three maximum, medium, and minimum input line voltages.

Fig. 7 shows the space vector diagram, sector identification, and the DC-link voltage waveform for the proposed SVM of the rectifier stage. In each sector, the reference current vector is composed of three active current vectors. For clarity, it is assumed that the reference input current vector locates in sector 1 ($0 \leq \beta_s \leq \pi/3$), the three active vectors, $\vec{i}_{ab}$, $\vec{i}_{ac}$, and $\vec{i}_{bc}$, are selected to synthesize the reference input current vector:

$$
\vec{i}_s = d_{ab}\vec{i}_{ab} + d_{ac}\vec{i}_{ac} + d_{bc}\vec{i}_{bc} \\
1 = d_{ab} + d_{ac} + d_{bc}
$$

(19)

The duty ratios of the three active vectors are determined as follows:

$$
\begin{align*}
    d_{ab} &= 1 - m_i \sin(\beta_s + \pi/6) \\
    d_{ac} &= -1 + \sqrt{3} m_i \cos(\beta_s - \pi/6) \\
    d_{bc} &= 1 - m_i \cos(\beta_s)
\end{align*}
$$

(20)

The average value of the DC-link voltage is calculated by:

$$
\bar{V}_{dc} = d_{ab}(v_a - v_b) + d_{ac}(v_a - v_c) + d_{bc}(v_b - v_c) \\
= \frac{3}{2}m_i V_i
$$

(21)

Fig. 7(b) shows the waveform of the DC-link voltage in the proposed SVM strategy, where the average value of the DC-link voltage becomes constant regardless of the input line voltages.

**FIGURE 7.** Proposed SVM of the rectifier stage: (a) Space vector diagram, (b) Sector identification and DC-link waveform.

Fig. 8 shows the switching pattern of the proposed SVM strategy for the three-phase IMC drive system to reduce the CMV and improve the harmonic distortion. The switching pattern is arranged symmetrically to achieve low voltage and current distortion. The switching events of the rectifier and inverter stages are also synchronized to obtain the balanced input current and output voltage. The duty ratios in Fig. 8 are given by:

$$
\begin{align*}
    T_{6ab} &= d_{l6}.d_{ab}.T_s, \quad T_{1ab} = d_{l1}.d_{ab}.T_s, \quad T_{2ab} = d_{l2}.d_{ab}.T_s, \\
    T_{6ac} &= d_{l6}.d_{ac}.T_s, \quad T_{1ac} = d_{l1}.d_{ac}.T_s, \quad T_{2ac} = d_{l2}.d_{ac}.T_s, \\
    T_{6bc} &= d_{l6}.d_{bc}.T_s, \quad T_{1bc} = d_{l1}.d_{bc}.T_s, \quad T_{2bc} = d_{l2}.d_{bc}.T_s.
\end{align*}
$$

(22)

**D. VOLTAGE TRANSFER RATIO**

In the proposed SVM strategy, the VTR is given as follows:

$$
q = \frac{V_o}{V_i} = \frac{\bar{V}_{dc}}{V_i} = \frac{3}{2}m_i m_i
$$

(23)

From equations (18) and (20), the duty ratios of the rectifier and inverter stages must be non-negative and lower than or equal to unity. This constraint leads to the restrictions of the modulation indexes and the VTR of the IMC:

$$
0 \leq m_v \leq 0.577; \quad 0.667 \leq m_i \leq 1; \quad 0.577 \leq q \leq 0.866.
$$

(24)
Based on equation (24), the proposed strategy is suitable to drive the IMC operation at a high VTR range.

E. SIMPLIFICATION IN THE PROPOSED SVM STRATEGY

In the previous approaches to reduce CMV while considering the output quality, the rectifier modulation is modified where the formation of the DC-link voltage is combined with the two switching schemes according to the VTR range [16], [17]. Padhee et al. presented a solution separating the operation of the IMC into two ranges of operation: low and high VTR ranges [16]. In the low VTR range, the two active and one zero current vectors are used for the rectifier modulation, while the active current vectors are used in the high VTR range. The flowchart in Figure 9 combines the two modulation schemes. To avoid the rectifier modulation separation according to the operation range, the approach by Tsoupos and Khadkikar proposed a weighting factor to formulate the DC-link voltage [17]. Whereby the two modulation schemes are merged to form a new SVM that can generate a variable DC-link voltage as follows:

\[
\bar{V}_{dc(Ref)} = d_{Low}\bar{V}_{dc(Low)} + d_{High}\bar{V}_{dc(High)}
\]

\[
d_{Low} = \frac{\bar{V}_{dc(Ref)} - \bar{V}_{dc(Low)}}{\bar{V}_{dc(High)} - \bar{V}_{dc(Low)}}
\]

\[
d_{High} = 1 - d_{Low}
\]

where \(\bar{V}_{dc(Ref)}\), \(\bar{V}_{dc(Low)}\), and \(\bar{V}_{dc(High)}\) are the average DC-link voltage of the modulation [17] and the low and high VTR schemes [16], respectively; and \(d_{Low}\) and \(d_{High}\) are the weighting factors of the low and high VTR schemes, respectively.

As a result, the modulation becomes more complicated in that the approaches described above require more computational burden and a lookup table to synthesize switching patterns. To simplify the modulation strategy with reduced CMV and improve the output harmonic distortion, the proposed SVM strategy uses a unique set of three active vectors for the rectifier and inverter modulations. Accordingly, three active current vectors are used to keep the average DC-link voltage at a constant value, and three active voltage vectors are selected to reduce the CMV of the IMC topology. Therefore, the proposed switching scheme is identical despite the operation range, and no additional manipulation is needed.

FIGURE 8. Switching pattern of the proposed SVM strategy.

FIGURE 9. Flowchart showing combination of two modulation schemes of the CMV reduction approach [16].

TABLE 1. Simulated and experimental parameters.

| Parameter          | Value                      |
|--------------------|----------------------------|
| Power supply       | \(V_i = 100\) V (line-to-neutral) |
| Input frequency    | \(f_i = 50\) Hz            |
| Input filter       | \(L = 1.4\)mH, \(C = 25\)\(\mu\)F, \(R = 20\)\(\Omega\) |
| Load               | \(R = 10\) \(\Omega\), \(L_c = 5\) mH |
| Voltage transfer ratio | \(q = 0.7\) |
| Output frequency   | \(f_o = 60\) Hz            |

FIGURE 10. Simulation results of the CMV and its FFT analysis with: (a) Conventional SVM without CMV reduction, and (b) Proposed SVM strategy.
IV. SIMULATION RESULTS

Simulations are completed using PSIM 9.0 software with a three-phase $R-L$ load to evaluate the effectiveness of the proposed SVM strategy. The simulated parameters are shown in Table 1.

Fig. 10 shows the CMV waveforms and the Fast Fourier Transform (FFT) analyses of the conventional SVM without CMV reduction and the proposed SVM strategy. The conventional strategy cannot reduce the CMV peak value due to the existence of the zero voltage vectors in the switching pattern. By only using the three active voltage vectors to generate the reference output voltage, the proposed SVM strategy reduces the peak value of the CMV from 100 to 57.7 V, which corresponds to $\frac{1}{\sqrt{3}}$ the input phase voltage magnitude. Moreover, the Root Mean Square (RMS) value of the CMV with the proposed SVM strategy is always lower than that with the conventional strategy, as demonstrated in Fig. 11. The reduced CMV leads to a reduction in the leakage current and bearing current.

FIGURE 11. Comparison in RMS value of the CMV between Conventional SVM without CMV reduction and Proposed SVM strategies.

FIGURE 12. Simulation results of input waveforms with: (a) Conventional SVM without CMV reduction, and (b) Proposed SVM strategy.

FIGURE 13. Simulation results of output waveforms with: (a) Conventional SVM without CMV reduction, and (b) Proposed SVM strategy.
FIGURE 14. Comparison in the output performance among Conventional SVM, other Reduced CMV-SVM, and Proposed SVM strategies in terms of: (a) THD of output current, and (b) THD of output line voltage.

Figs. 12 and 13 show the simulation results of the input/output waveforms of the conventional and the proposed SVM strategies at the VTR $q = 0.7$. As can be seen, the quality of the input and output waveforms does not suffer from the proposed SVM strategy. Additionally, the input voltage is in phase with the input current; the proposed SVM strategy can drive the IMC at the unity input power factor. The filtered input current is sinusoidal and leads the input voltage with a little phase angle due to the characteristics of the input filter.

To evaluate the output performance improvement of the proposed SVM strategy compared to the previous reduced CMV-SVM strategies, the total harmonic distortion (THD) of the output current and output line voltage is shown in Fig. 14. The THD values acquired with the proposed SVM strategy are smaller than those achieved with other reduced CMV-SVM strategies. This signifies that the IMC output performance improves significantly as a result of the constant value of the average DC-link voltage, which is achieved by the redesigned rectifier modulation in the proposed SVM strategy.

Fig. 15(a) shows the dynamic responses of the output voltage and current waveforms of the proposed strategy with a load input voltage step change from $q = 0.6$, $f_o = 60$ Hz to $q = 0.8$, $f_o = 30$ Hz, and back. Fig. 15(b) shows the performance of the proposed strategy for the case of a load condition step change from $R = 20$ $\Omega$, $L = 5$ mH to $R = 10$ $\Omega$, $L = 5$ mH, and back. The proposed SVM strategy can maintain sinusoidal output currents and a good dynamic performance even when the load condition changes suddenly.

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed SVM strategy, a prototype of the three-phase IMC is implemented in the laboratory as shown in Fig. 16. The control board is designed with a 32-bit floating-point DSP TMS320F28335 and a CPLD Altera EPM7128SLC84-15 to perform the PWM technique and four-step commutation, respectively. The bidirectional power switches are executed by two discrete IGBT modules IRG4PF50WD. The unidirectional power switches
in the inverter stage are performed by the IGBT module FMG2G150U560. The parameters used in the experiment are the same as those in the simulation shown in Table 1.

Fig. 17 shows the experimental results of the input phase voltage, the CMV waveform, and its FFT analysis using the conventional SVM without CMV reduction and the proposed SVM strategies. The proposed SVM strategy reduced the CMV peak value by 42.3% compared with the conventional strategy. It should be noted that the CMV suppression of the proposed SVM strategy is the same as that of the existing CMV reduction methods. Thus, the problems commonly associated with CMV are significantly decreased with the proposed SVM strategy.

Figs. 18 and 19 show the experimental results of the input and output waveforms of the conventional and proposed SVM strategies at the VTR $q = 0.7$, respectively. The input and output currents are good sinusoidal waveforms. The filtered input current leads the input phase voltage slightly due to the input low-pass filter. These results exactly match the simulation results.

**VI. CONCLUSION**

This paper presents a simple SVM strategy that can reduce the CMV as well as improve the output performance for a three-phase IMC. Using three active current vectors for the rectifier modulation, a constant average DC-link voltage is achieved, which can improve the output performance in terms of the output voltage and current harmonic distortion. To suppress the CMV value to 57.7% of the input phase voltage, the three active voltage vectors are used for the inverter modulation. Due to the unique set of three active vectors for both rectifier and inverter modulations, the proposed SVM strategy can
avoid the increase in computational burden and use of a lookup table for switching patterns synthesis associated with the existing approaches. Simulated and experimental results demonstrate the effectiveness of the proposed SVM strategy.

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