GradPIM: A Practical Processing-in-DRAM Architecture for Gradient Descent

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Abstract—In this paper, we present GradPIM, a processing-in-memory architecture which accelerates parameter updates of deep neural networks training. As one of processing-in-memory techniques that could be realized in the near future, we propose an incremental, simple architectural design that does not invade the existing memory protocol. Extending DDR4 SDRAM to utilize bank-group parallelism makes our operation designs in processing-in-memory (PIM) module efficient in terms of hardware cost and performance. Our experimental results show that the proposed architecture can improve the performance of DNN training and greatly reduce memory bandwidth requirement while posing only a minimal amount of overhead to the protocol and DRAM area.

I. INTRODUCTION

As DNN emerges as one of the most significant applications of the era, neural processing units (NPU) are quickly becoming an important member of computing systems for both of inference and training [24], [25], [26], [27], [36], [49], [80]. Often, the key to achieving the NPU performance is minimizing its memory (usually DRAM) bandwidth requirements. Naively executing DNNs would incur heavy memory traffic caused by repeated memory accesses in the same data. Many NPU architectures [23], [24], [25], [27], [36], [41] utilize different dataflow models in order to handle the data reuse problem by loop reordering and careful address mapping to the PE array. Also, mixed-precision training [33], [73], [74], [98], [102] is a widely used technique which helps reduce both the computation and memory traffic. In addition, minibatch serialization [71], BN fusion and fusion [50], and layer fusion [17] fall into the class of inter-layer optimizations that finds opportunities of data reuse to reduce the amount of memory traffic.

Processing In Memory (PIM) is a surging technique that optimizes memory accesses. By placing logic components and DRAM on the same die (or same stack [82]), the off-chip bandwidth bottleneck can be significantly mitigated as demonstrated by many PIM works [22], [34], [54], [65]. However, despite its huge potential, bringing PIM to the market has always been a tough challenge. One of the major reasons was that making the necessary changes (e.g., ISA extension, memory controller support, etc.) from the CPU side is too disruptive to the current ecosystem. However, we believe it could be far easier to do so on NPUs, as its ecosystem is not fixed yet, and there are numerous vendors trying to design their own NPUs. In such circumstances, NPUs can become a major opportunity to bringing PIMs to the DNN execution ecosystem.

Recently, Kim [55] revealed some practical challenges from the DRAM vendors’ view on what is hindering commercial DRAM products from supporting PIM. He discussed issues such as 3D stacking overhead, limited power/thermal budget, and conflicts with existing protocols. From a similar perspective, we predict that if a PIM technique were to be accepted by commercial products in the near future, it would be incremental to the existing products (e.g., DDR, HBM). In that sense, a practical PIM solution for DNN training should achieve the following three goals:

1) Fixed-function PIM [69], non-invasive to the existing protocol: The technique should preserve the existing protocol as much as possible. The new functions should have deterministic latencies in order to prevent conflict with the current memory controller designs.

2) Simple, memory-intensive functions: To reduce the area overhead and mitigate the thermal/power budget problem while allowing for a large performance gain, the added function should be simple, and memory-intensive.

3) Isolation of PIM components and DRAM cell array: Modifying the cell array would cause radical design changes to the existing product, and should be avoided.

Taking the above goals into careful consideration, we propose
GradPIM, a fixed-function PIM that supports gradient descent logic within the DRAM die. According to our analysis of state-of-the-art data reuse techniques, parameter updates of modern DNN workloads have high memory bandwidth requirements. For example, that of ResNet-18 [44] consumes up to 50% of the total memory traffic during training. This memory-intensive nature of parameter update makes PIM an appropriate solution.

Unlike the other parts of the training, the operations involved in the update phase have been overlooked in many designs. Those operations are relatively simple, and do not have much room for further optimization. However, being both simple and memory-intensive makes them an excellent target for processing-in-memory. In this paper, we propose assisting a mixed-precision accelerator with a PIM-enabled memory specialized for parameter update operations.

Conceptually, we attempt to isolate the memory traffic associated with the parameter update phase within the memory using GradPIM (Fig. 1), just as data reuse techniques isolate the traffics of forward and backward operations within NPUs. We identify the bank group I/O gating as the ideal place for placing the parameter update logic. By placing registers next to the bank group I/O gating, we effectively decouple each bank group from the global DRAM structure. With careful data arrangements, we implement a set of DDR-based PIM operations that can perform parameter updates using the DRAM internal parallelism.

GradPIM is designed to be a simple extension from the existing DDR4 protocol [5] without altering the existing commands. The design is also non-invasive to the DRAM cell arrays and places only a small module along with the peripherals. Those modules are fully controlled by the memory controller using a reserved command (i.e. RFU), and thus GradPIM can be considered as a DDR-compatible device rather than an independent accelerator.

We evaluate GradPIM combined with a contemporary NPU design. We show that the proposed design significantly reduces the total memory bandwidth requirements and the total execution time. Our contributions can be summarized as follows:

- With modern optimizations towards reducing bandwidth requirements, we identify that the update phase during DNN training accounts for a significant portion, and can be an excellent target for a practical PIM design.
- We design a PIM logic that decouples each bank group from the global structures, so that parameter update phase operations can be executed within the DRAM, by utilizing the internal bandwidth of the DRAM.
- We model the proposed PIM logic design by performing a layout under DRAM technologies and analyze the area and power overhead of placement.
- We address the data placement and mapping issue for deploying GradPIM on modern DRAM organizations.

II. MOTIVATION

Most NPU designs are focused on maximizing MAC utilization and minimizing memory traffics during forward and backward passes. Considering the usual training procedures, the traffics from reading activation values from memory dominate the entire memory traffic and the execution time, making the above strategy promising. However, with mixed-precision training (e.g., 8bit gradient/32bit master weights) and a few state-of-the-art data reuse techniques [17], [50], [71], the relative portion of memory accesses from parameter updates dramatically increases. Fig. 2 shows the breakdown of the amount of memory accesses in training a batch of ResNet-18, in MB. The bars are divided into forward pass (Fwd), backward pass activations (Bact), backward pass weights (Bwgt), and parameter updates (Pup) for full-precision training (top) and 8bit/32bit mixed-precision training (bottom). To maximize data reuse, we applied MBS (MiniBatch Serialization) [71] and BNFF (Batch-Normalization Fission and Fusion) [50] to reduce the inter-layer data traffic.

As the network advances to later layers, the portion of the memory traffic caused by parameter updates becomes significant. The weight parameter update phase consumes 22.4% of the total memory accesses during full-precision training. During mixed-precision training, on the other hand, the update phase occupies a total of 45.9%. For the last block (a set of conv5m layers), the parameter update phase takes up as much as 80.5% of memory traffic alone. This observation is partly in line with the analysis in [22] which reports that offloading packing and quantization of data to a PIM module can bring speedup and energy gain on various applications including TensorFlow Mobile [11]. Even though quantization for training is still premature in that it does not always yield full accuracy, it is an active field of research that includes 16bit [33], [74] and 8bit [73], [98], [102] quantizations, and is quickly being adopted by many NPU designs as a promising way of reducing hardware cost [2], [10].

The portion of traffic in the update phase depends on the ratio of activations and weight parameters. As the application...
fields of DNNs expand towards non-CNN workloads such as AlphaGo [94] (a DNN-based boardgame player) or multi-layer perceptrons (MLP) [62] (general problems), we have found that the portion of the weight parameters rises especially for those emerging non-vision DNN applications, which indicates great opportunities for the proposed GradPIM going forward.

III. BACKGROUND

A. DNN Parameter Update Algorithms

Majority of DNNs rely on a family of stochastic gradient descent (SGD) as the parameter update algorithm. In the simplest form of SGD, all parameters in the network are updated towards the negative direction of the gradient at the end of each minibatch execution. The update can be formulated as the following:

$$\theta_{t+1} = \theta_t - \eta g_t$$  \hspace{1cm} (1)

where \(g_t\) is the gradient vector over the current minibatch and \(\eta\) is the learning rate. To gain faster convergence and/or better accuracy, many advanced parameter update algorithms have been proposed. For example, SGD with momentum [84] is formulated as below:

$$v_t = \alpha v_{t-1} - \eta g_t$$  \hspace{1cm} (2)

$$\theta_{t+1} = \theta_t + v_t$$  \hspace{1cm} (3)

where \(\alpha\) is a momentum decaying factor and \(v\) is the momentum. The momentum works as a damping factor, and makes the convergence faster. If weight decay term \(\beta\) is used in addition, Eq 2 becomes

$$v_t = \alpha v_{t-1} - \eta (\beta \theta_t + g_t)$$  \hspace{1cm} (4)

There are a few more parameter update algorithms worth mentioning such as Adam [57], AdaGrad [37], NAG [76] or RMSprop [100].

These algorithms all exhibit element-wise computations and has a relatively low number of computations per element. However, they usually require higher precision especially due to their small hyperparameters (e.g., \(\eta = 0.01\)). Thus, this can easily become the bandwidth bottleneck in the DNN training, especially with mixed-precisions.

B. Modern DRAM Architecture

The modern DRAM architecture is a result of multi-decade effort of increasing cell density and bandwidth at the same time. Fig. 3 shows the modern DDR4 SDRAM architecture. A DRAM is composed of multiple banks, which are 2D arrays of 1T1C cells. To increase the area efficiency, a row of cells in a bank share a wordline (WL), which is used to select the row that should be activated. A vertical set of cells in a bank share a pair of bitlines (BL, BLB) that is used to deliver the data from/to the cells. When a row is activated, the small charge stored within each cell flows out to the bitline and is caught by a row of sense amplifiers. The sense amplifiers restore the cell capacitor to its original value, and this takes tRAS to complete.

To read data from the activated row, a few bits (column) are chosen. After tRCD from the beginning of an activation, data can be read from the activated row. A column is chosen and propagated through the I/O gating and to the off-chip data bus. Even though each bank can operate independently, the I/O gating circuitry is shared among them, and each column read command occupies the I/O gating for tCCD. Therefore a back-to-back column read command has to be spaced with tCCD. Also, the data occupies the off-chip data bus for tBURST. tCCD and tBURST are usually set to be 4 cycles, providing 64 bytes of data in a burst\(^1\). After tCL of latency from the assertion of a read command, the data burst starts on the data bus. In the case of a column write, the data flows in the opposite direction. The memory controller can place the data on the bus tCWL time units after the write command assertion, and the I/O gating is again occupied after tCCD.

If a different row has to be accessed for read or write commands, the current row has to be deactivated and a new row has to be opened. However, if a previous read or write command is on-going on a column, the row has to remain open for tRTP or tWR after the previous read/write command respectively, because the row has to provide the data for a read, or has to wait for the data to be restored for a write.

\(^1\)In fact, multiple chips co-operate as a rank to provide 64 bytes in a 4 cycle burst. We omit the details for brevity.
An important concept introduced since DDR4 [5] is bank groups. To keep up the internal fetch speed with the increasing off-chip data rate, multiple banks (2, 4, or 8) form a bank group, and the I/O gating is partitioned into bank group I/O gating and global I/O gating. The result is that if consecutive column accesses are asserted to two different bank groups, the accesses only share the global I/O gating, and still can be spaced with 4 cycles (≈tCCD_S) as in previous generations (i.e., DDR3 [4]). However, if those accesses are to the single bank group, the data occupies both the bank group I/O gating and the global I/O gating, and the two accesses now have to be scheduled with a longer interval (≈tCCD_L) in-between. Usually, tCCD_L is 25% to 100% longer than tCCD_S.

With the introduction of bank groups, there are two kinds of opportunities for in-DRAM processing-in-memory (PIM) technologies. First, bank-level parallelism exploits the fact that each bank can be independently accessed, and a single bank alone can provide more than half the bandwidth of the off-chip data bus (the ratio depends on tCCD_S/tCCD_L). Thus, a DDR4 SDRAM chip with 16 banks has more than 8x bank-internal bandwidth, multiplied by the number of ranks per channel. On the other hand, each bank group can also provide more than half the bandwidth of the off-chip data bus. Therefore there is more than 2x (for DDR4) or 4x (for DDR5) bank group-internal bandwidth, again multiplied by the number of ranks. Each bank group has access to multiple banks and therefore provides an opportunity to work with multiple open rows in separate banks, which would not have been possible when working only with bank parallelism.

IV. GradPIM

Contrary to many PIM work that perform MAC operation within DRAM [34], [53], [65], we leave the MAC operations entirely to the host NPU. Instead, GradPIM performs the parameter update phase, following the observations from Section II. The remainder of this section describes the in-DRAM structure of GradPIM and how it is organized.

A. GradPIM architecture

Fig. 4 shows the architecture of GradPIM unit. A GradPIM unit is placed at each bank group, next to the local I/O gating (Fig. 3). At the heart of GradPIM is the temporary registers next to the local I/O gating. They decouple the local I/O gating and the global I/O gating, enabling the bank-group level parallelism [93]. We read to or write from the temporal registers, instead of occupying the external data bus. Also, we perform the vector operations required for the update phase.

Another benefit of placing the GradPIM unit next to the bank group I/O gating is that it has access to multiple banks. That means, unlike a few previous PIM approaches [63], [89] which performs operations within a bank, GradPIM can operate on multiple rows concurrently at a time. This is essential for working with multiple arrays of variables, which would otherwise cost expensive row activation each time a column of different array is accessed.

GradPIM logic mainly includes three components: Registers, scaler, and parallel arithmetic unit.

- **Registers** are used to store intermediate results and have the same width of the global sense amplifiers (i.e., 64 Bytes in total for a rank). We place two temporary registers per GradPIM unit to be used for source and destinations of the arithmetic operations, and one quantization register exclusively for storing the quantized values.
- **Scaler** is used to scale the data with pre-defined hyperparameters, e.g., default learning rate. The scaler is placed between the bank group I/O and the registers, and performs element-wise multiplications.
- **Parallel arithmetic unit** is used to perform element-wise computations within the update phase, such as the additions in Eq. 4. In the current version of GradPIM, we support simple additions and subtractions.

B. GradPIM Operations

With the components, the operations that GradPIM perform are classified into three categories as below:

1) **Scaled read** loads a column of data into a register from the cells. While loading the registers, the values are scaled by certain hyperparameters, such as $\eta, \alpha$ or $\beta$ as in Eq. 4. Since those values are mostly fixed constants, we pin four scaler values to an id to each value. To simplify the scaler, we approximate the scaler values in $2^n \pm 2^m$ and implement the scaler with shifters and adders. The values of $n$ and $m$ assigned to each opcode can be programmed with MRW (Mode Register Write) command in case the user needs different set of values.

2) **Parallel operations** perform arithmetic operations from the registers and puts the result into another register similar to AVX-512 VPADD [8] instruction. Currently, we support add, sub, quantization, and dequantization to create the partial terms of Eq. 4 or execute conversion between quantized and dequantized values. Quantization either reads data from one of the temporary registers...
and write to the quantization register, and vice versa for dequantization. Since the quantized values stay longer (four times for 8bit quantization) in the register, using a dedicated register greatly simplifies the data and control path circuit design (see Section 5 for details).

3) Writeback. After the operations for the optimizers are complete, the result has to be written back. This corresponds to the second half of the DDR column write, where the register data is written to the global sense amplifier and to the cells.

C. Timing Considerations

To allow the memory controller to schedule the GradPIM commands along with the existing commands, each GradPIM command has to mingle with the timing parameters. We keep timings for each command as below:

The scaled read is similar to the column read operation in the ordinary DDR protocol [5], but the data is placed to one of the registers instead of the data bus and therefore does not limit the scheduling of other commands with tBURST. In an attempt to maintain close consistency with the existing DDR commands, the memory controller regards the operation as complete after tCCD_L. In DDR protocol, tCCD_L represents the bandwidth that a bank or a bank group is capable of providing. Because the scaled read operation also reads the data from the banks, it is reasonable to assign the same tCCD_L to read data and be stored in the register. Also, tRTP is still preserved since the sense amplifiers need to provide the data from the cells. Please note that the scaled read occupies only the local bank group I/O gating and thus does not interfere with the other scaled read commands in different bank groups.

The parallel arithmetic operations happen completely out of the conventional DRAM logic and is not governed by the existing timing parameters. To account for the parallel ALU being occupied, we introduce an extra timing parameter tPIM, which represents the worst case execution time for the arithmetic operations. This timing parameter does not interfere with any other commands, but prohibits other PIM arithmetic operations from taking place within the same bank group.

Writeback operation can be considered as the latter half of the existing write command. Instead of the data bus, the data comes from one of the registers. Therefore the writeback operation is not affected by tCWL or tBURST, but we keep tCCD_L as in the scaled read as the bank group I/O gating is occupied. tWR has to comply if the row is to be closed after the writeback since the data propagate into the row through the sense amplifiers.

To consider the power budget, we first estimated the maximum power of a DRAM channel as done by [53], by performing sequential reads while keeping the tFAW and tRRD constraints. Then we have scaled tFAW and tRRD so that performing consecutive PIM operations would yield the same maximum power. However, it only added a negligible amount of difference to both timing parameters (<1%).

D. Update Phase Procedure

To execute the update phase with GradPIM, the NPU first writes the gradients to the memory generated by a backward pass on the weights. Then, the parameter update algorithm is executed as shown in Eq. 3 and Eq. 4. After the update, the NPU reads the updated weights for the next step forward pass. To support mixed-precision training, quantization and dequantization are performed before and after the parameter update algorithm, so that GradPIM can work on high-precision data whereas the NPU can work on low-precision data. In this section, we show how these processes are performed sequentially using the operations described in Section IV-B assuming 8bit/32bit mixed-precision. In full-precision training, the quantization/dequantization can be omitted.

1) Dequantization: Fig. 5 (Top) shows the procedure for performing dequantization. We assume the rows for the quantized gradients Q(g) and the dequantized gradients g are already open on different banks within a bank group so that they can be accessed at the same time, and the procedure is as follows: ① A column of Q(g) is loaded into the quantize register. ② A 1/4 of a column of the Q(g) is dequantized and the resulting column is written to a temporary register. The dequantization command specifies which 1/4 of the column

![Fig. 5: Example procedure for quantization/dequantization and momentum SGD algorithm with GradPIM.](image-url)
should be read from the quantize register and which temporary register to write to (please see Section IV-E). Then the gradient \( g \) is written back to the corresponding row, and \( 2 \) is repeated four times until the entire column had been dequantized. The procedure is repeated for the consecutive columns of \( g \).

One thing to note is that because we place a unit in the local I/O of the bank group, the entire procedure does not experience any row buffer miss except for when a new row is opened for next data accesses (like a cold miss in a cache).

2) Parameter Update: Fig. 5 (middle) shows the procedure for conducting the update phase with GradPIM using momentum SGD [84] algorithm as in Eq 3, 4 as a simple example. We assume that the rows for weight parameters \( \theta \), momentum \( v \) and gradients \( g \) are already activated on different banks within a bank group. \( 1 \) A column of \( g \) and \( v_{t-1} \) are loaded to the temporary registers, scaled by \( \eta \) and \( \alpha \) using scaled \( \text{rd} \) operation. \( 2 \) The scaled values in the two registers above are processed with parallel \( \text{add} \). \( 3 \) A column of \( \theta_{t} \) is loaded into a temporary register, scaled by \( \eta \beta \). \( 4 \) Parallel \( \text{add} \) is performed once again, creating \( v_{t} \) in Eq 4. \( 5 \) Writeback is performed from the register with \( v_{t} \) to the open row for \( v_{t} \). \( 6 \) Similarly, a column of \( \theta_{t-1} \) is generated by Eq. 3 and written back to the row storing \( \theta \). Finally, \( 1 \) - \( 6 \) is repeated for consecutive columns of \( g \), \( v \) and \( \theta \) until the entire row has been processed.

This procedure also requires no unnecessary row activations as in the dequantization case. In the case of the more complicated algorithm where more than one momentum is used per weight parameter, the required number of concurrent open rows might increase, but there are four banks per bank group in typical DDR4/5 SDRAMs and it is enough to cover all per-weight values in most of the SGD-based parameter update algorithms to our knowledge.

3) Quantization: Fig. 5 (Bottom) shows the procedure for performing quantization. As the last step, the master weight parameters are quantized to a low precision, so that the NPU can read them during the forward and backward phase. The procedure is similar to dequantization, but the order is opposite. \( 1 \) A column of master weight parameters are loaded to a temporary register, and quantization is performed. It fills a quarter of the quantization register, so this is repeated four times. \( 2 \) Each time the quantization register becomes full, it is written back to the row with \( Q(\theta) \). It is repeated for the consecutive columns of \( \theta \).

E. Commanding GradPIM

We utilize the RFU (Reserved for Future Use) commands in existing DDR4 protocol [5] to realize the GradPIM commands without modifying the existing commands. According to the standard, there are a number of configurable command signals for RFU operations. Since all the commands require addresses for bank groups, banks, rows, and columns, it leaves five signals left for configuring GradPIM commands

\[ \text{TABLE I} \]

| Signal   | Op0 | Op1 | Param0 | Param1 | Src/Dst |
|----------|-----|-----|--------|--------|---------|
| Scaled Read | L   | L   | Scale ID | Dst    |
| DeQuant   | H   | L   | Src Position | Dst |
| Quant     | H   | H   | Dst Position | Src |
| Writeback | L   | H   | L       | Src   |
| Q. Reg    | L   | H   | H       | RD/WR |
| Add       | L   | H   | H       | Dst   |
| Sub       | L   | H   | H       | Dst   |

2 These are A12/BC_n, A17, A13, A11 and A10/AP [5].
The input matrices are partitioned into 256x256 blocks that fit to bank-group and bank conflicts. Except for the simple SGD, device and allows for element-wise operations. are placed within each device. This puts an entire word into a arrangement scheme used in [39], [63] where consecutive bits requires the entire 32bit within a device in order to perform a x4, x8, and x16 device respectively. However, GradPIM to form a data bus with a large data width. 64-bit data are placed in two different bank groups, it requires an inter-bank communication, which occupies the global shared data bus. On the other hand, if the two arrays are placed within a single bank, it is a trivial case of a bank conflict.

Therefore, it is necessary to ensure that the corresponding elements of the arrays are placed within the same bank group, but to different banks. It can be solved by carefully designing the address mapping. Fig. 7 shows the address mapping for GradPIM. To enable maximum bank-group level parallelism, we adopt bank-group interleaving, so that multiple bank groups can operate concurrently. The bank ids within the bank groups are assigned to the MSB of the addresses. This makes sure that multiple different arrays can always be placed in distinct banks. When allocating the arrays such as θ or v, they are aligned to the bank boundary, so that the items at the matching positions always stay within the same bank group.

For the quantized weight parameters, it is impossible to perfectly align them with the non-quantized weight parameters, because their elements differ in width. If they are aligned to the beginning of the array, they will not be present in the same bank group anymore. To solve the problem, we choose to utilize only the first quarter (for 8/32 bit quantization) of the row for the quantized weights. By doing this, even though we might waste the DRAM capacity, we do not waste the off-chip bandwidth. The GradPIM operation will run without a problem because the column id of the elements do not have to match as long as they are placed within the same bank group and different bank. We do not consider multiple channels/ranks in this section, but the channel or rank bits can be placed between the bank group bits and the bank bits as long as they are placed within the same bank group.

In order to avoid the memory traffic explosion due to the im2col scheme, we place a dedicated module for performing im2col. The module creates a block of matrix from the image-format activations in the global buffer and writes to the activation local buffer. The global buffer aggregates a few matrix blocks to form a macroblock so that it can hold the right amount of data at a time. The calculated output blocks coming from the MAC arrays are accumulated in the global buffer. When processing is done for the macroblock, it is sent to the DRAM through the write buffer. In case of the backward phase, a dedicated col2im module is used between the global buffer and the write buffer, performing the inverse of an im2col required for the backward pass.

B. Data Placement

Conventional DRAM subsystems integrate multiple devices to form a data bus with a large data width. 64-bit data are split into 4, 8 or 16 bits and interleaved among devices for a x4, x8, and x16 device respectively. However, GradPIM requires the entire 32bit within a device in order to perform vector operations. We simply follow the non-interleaving data arrangement scheme used in [39], [63] where consecutive bits are placed within each device. This puts an entire word into a device and allows for element-wise operations.

Considerations are needed for the address mapping to avoid bank-group and bank conflicts. Except for the simple SGD, update phase requires more than one value per parameter (e.g., θ and v in Eq 3). Reading them are sequential, but incurs a cumbersome problem for GradPIM. When the two arrays of values are placed in two different bank groups, it requires an inter-bank communication, which occupies the global shared data bus. On the other hand, if the two arrays are placed within a single bank, it is a trivial case of a bank conflict.

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To exploit the effect of data mapping to the programming model, we assume a device-side allocation function supporting separation between data structures is provided, similar to multi-stream features in SSDs [30]. Therefore the user only specifies that each data structure should be stored to different banks, without being directly exposed to the the physical banks or bank groups. In the current setting, we assume that the NPU has its dedicated memory attached with GradPIM. However,
GradPIM can also be used when the host and the NPU share the memory by assigning certain memory region to the NPU, similar to pinned memory in CUDA [77].

An alternative to the aforementioned data placement is to use array-of-structures, where multiple types of parameters form a structure that are repeatedly and sequentially stored in the memory as arrays. While this solves many of the problems such as bank conflict or inter-bank communication for the parameter update phase, it has a critical drawback for the forward and backward phase for having to read unnecessary parts of data within the structure along with the desired ones. We demonstrate its effect in Section VI-B.

C. Memory System Interfacing

Typically, a DDR4 memory chip communicate with its host chip through memory controllers that follows the DDR4 protocol, which are placed on the host chip. Such systems are called direct-attach memory system, and is shown in Fig. 8 (a) (GradPIM-Direct). While it is a popular design choice, our experiments show that the command bus becomes a bottleneck that prevents GradPIM from exploiting the full bank-group level internal bandwidth from the DRAM chips (See Fig. 11).

In light of the fact, we design an alternative version of GradPIM based on buffered memory system as shown in Fig. 8 (b) (GradPIM-Buffered). Often used for high-end servers, buffer devices are placed between the host chip and the memory devices. They usually function as fan-out expander by buffering and repeating signals. The host chip and the buffer device communicate via serial interconnects such as OMI [96] or AMB interface [43]. Buffer devices have separate command buses that can mitigate the command bus bottleneck. High-level commands are defined such as those in HMC [82] in order to reduce the host-to-buffer device command bandwidth.

D. Distributed Learning

Distributed data parallelism [32], [87] allows using multiple nodes to run the exact same model with different parts of the minibatch. This provides another opportunity for GradPIM.

By applying distributed data parallelism, it parallelizes the forward and backward pass of the training, but the parameter update phase is performed independently at each NPU, almost equivalent to the sequential portion of the application.

To support distributed training with multiple NPUs, a dedicated P2P unit is placed, so that it can perform communications to other NPUs via high-speed interconnects similar to GPUDirect [85]. As in many GPU-based distributed learning work [47], [75], we use all-reduce [99] communication pattern. The all-reduce communication includes accumulating the gradient in the every gradient sharing step, which is also mapped to GradPIM similar to the update procedures.

VI. EVALUATION

A. Evaluation Methodology

We evaluate the proposed NPU with an in-house simulator written in SystemC [79]. GradPIM is modeled by extending DRAMSim 3.0 [64], and we faithfully modeled the timing of GradPIM operations as explained in Section IV-C while keeping the existing timings posed by the existing DDR protocol. To verify the NPU, we synthesized the NPU with 8bit datapath and 256×256 MAC-adder trees in Verilog HDL at 1GHz using Nangate 45nm open cell library [59]. We have ensured the timing closure and the functionality of the NPU.

Unless noted otherwise, DRAM devices are based on DDR4-2133 with 4 ranks, 4 bank groups and 4 banks per bank group. We set the bandwidth of the serial interconnect for the buffer devices (when used) to be equal to that of the GradPIM-Direct for a fair comparison. We referred to the energy and timing parameters from [1]. The key parameters are displayed in TABLE II. The overhead of the GradPIM unit within the memory is modeled by conducting a layout at 45nm technology over the DRAM constraint of 3 metal layers and 70% core utilization, which is then scaled to 32nm. The area and energy measured is shown in TABLE III. When implemented in an x8 8Gb DDR4-SDRAM device, GradPIM only incurs 0.01% area overhead to the DRAM, which approximately corresponds to the size of a 1Mb DRAM cell. We followed [78] to model the partial energy needed for read/write within the bank group (IDDpre). For the off-chip link model, we use the DRAM power

| Module | Area ($\mu$m$^2$) | Power (mW) |
|--------|-----------------|------------|
| Adder  | 320.1           | 0.058      |
| Quantize | 275.4            | 0.056      |
| Dequantize | 244.8             | 0.041      |
| Scaler | 606.1           | 0.159      |
| Registers ($\times$3) | 206.7 | 0.04 |
| Total | 8267.8 | 1.74 |

TABLE II: DRAM parameters

| Timing (Cycles) | Value | Current (mA) | Value |
|-----------------|-------|--------------|-------|
| tCK             | 0.94ns| Vdd          | 1.2V  |
| tCL             | 16    | IDD0         | 75    |
| tRCD            | 16    | IDD2P        | 25    |
| tRP             | 16    | IDD2N        | 33    |
| tRAS            | 36    | IDD3P        | 39    |
| tCCD_L          | 6     | IDD3N        | 44    |
| tCCD_S          | 4     | IDD4W        | 225   |
| tRR             | 1     | IDD4R        | 225   |
| tPIM            | 5     | IDDpre       | 98    |

TABLE III: Layout Results
Fig. 9: Normalized execution time of each layer on various networks using GradPIM. The filled parts of the bars represent parameter update phase, and the translucent parts of the bars represent the forward/backward phase.

Fig. 10: Energy consumption of GradPIM and other techniques.

Compared to the baseline, GradPIM-Direct achieves around $2.25 \times$ higher performance for the parameter update phase from utilizing the internal bandwidth of DRAM bank groups. For the entire training, the overall speedup is about $1.38 \times$ in geometric mean as it is governed by the Amdahl’s law. With GradPIM-Direct, the bottleneck is the limited rate command (Section IV-E). TensorDIMM and GradPIM-Buffered alleviate the problem by using buffered DIMMs. TensorDIMM achieves $1.36 \times$ speedup in geometric mean. However, it’s speedup is limited by the amount of rank-level parallelism. GradPIM-Buffered achieves $1.94 \times$ speedup overall, and $8.23 \times$ on parameter update by utilizing the bank group level parallelism.

In Fig. 9, AoS achieves similar speedup on parameter updates, having the same internal bandwidth as the GradPIM-Buffered. However, it reduces the effective bandwidth of Fwd/Bwd to $1/4$, because unnecessary to-be-discarded data will be mixed inside every DRAM burst. As a result, most of the benefit from using GradPIM is diminished.

AoS-PB shows the performance when a GradPIM unit is placed per bank. Putting aside the increased area overhead, the per-bank design can increase the speedup on the parameter update with high bank-level internal bandwidth ($4 \times$ in DDR-4). However, since only one row can be activated at a time, AoS placement is mandatory, from which the model will suffer from the same burst inefficiency. As a result, the $4 \times$ inefficiency in the Fwd/Bwd dwarfs the small benefit of the per bank design.

**Energy Consumption.** The energy consumption from the memory is shown in Fig. 10. Each design is depicted with different colors, while the breakdown between PIM, Write, and Activate are distinguished with the brightness, in the respective order. For TensorDIMM (TD), we show the energy consumption of a PIM unit on a buffer device, assuming a 32nm logic process buffer device. The energy saving is almost...
proportional to the speedup as the saving mostly comes from reduced external bandwidth usage, which translates to less switching. As illustrated in the breakdown, most of the energy reduction comes from the reduced amount of read/write. For the parameter update phase of the non-PIM approach, the NPU reads high precision master weight, performs update, and writes the master weight back to memory, which all incorporates the off-chip bus. On the contrary, GradPIM only requires a one-way transaction of low-precision gradient from the NPU to memory. Therefore, the proposed model benefits from two sources of savings: lower bit-width and reduced memory transaction.

The energy breakdown show that energy consumption of row activation is almost the same across all architectures, since GradPIM does not change the number of data to be read from DRAM. On the other hand, the energy consumption of RD/WR exhibit more variation, especially for AoS and AoS-PB where the increased data access during the Fwd/Bwd phase leads to much higher RD/WR count than GradPIM-Direct and GradPIM-Buffered.

**Bottleneck Analysis.** Fig. 11 (bottom) shows the internal bandwidth consumption of DRAM during the update phase. It shows the bandwidth consumed inside the DRAM dies, and tells us the utilization of the GradPIM units when compared to the peak internal bandwidth (dotted line). The baseline NPU’s external bandwidth consumption during the update phase is around 15GBps, reaching near the theoretical maximum of 17.1GBps. The internal bandwidth of the baseline is trivially the same. On the other hand, the internal bandwidth consumption of GradPIM-Direct on average is 28GBps, far higher than that of the baseline. The benefit comes from each GradPIM unit working independently on each bank group, leading to speedup and decreased energy consumption. However, compared to the theoretical maximum of 181.28 GBps, it represents only 15.4% of the peak bandwidth and the GradPIM unit utilization. We found that the bottleneck is at the command bus, reaching near 100% utilization as shown in Fig. 11 (top). This means that the command bus is blocking any further internal bandwidth increase from GradPIM-Direct. With GradPIM-Buffered, the because commands are generated by the buffer chip, the command bus bottleneck is alleviated. It consumes around 113GBps, almost 4.0 × the internal bandwidth compared to GradPIM-Direct.

**C. Sensitivity Analysis**

**Operations/Bandwidth ratio.** To examine how GradPIM would perform on accelerators in different environments, Fig. 12a shows the speedup sensitivity with respect to the operations/bandwidth ratio in a range that includes a few NPUs [2], [49], [101] and GPUs [3], [9]. The X axis shows the ratio between the operations and the memory bandwidth, using different MAC array sizes (64x64-512x512) and memory data rate (DDR4-2133, 3200 and HBM). The Y axis represents how much speedup is obtained with GradPIM over baseline for each setting, measured from executing AlphaGoZero.
As Operations/Bandwidth of the NPU increases, GradPIM achieves more speedup until the MAC array is too large that the latency to fill the array dominates the execution time, leading to diminished gains. The figure shows that GradPIM achieves meaningful speedups (20-70%) for a range that covers the Operations/Bandwidth of the chosen NPUs, but the speedup diminishes as the ratio approaches that of the GPUs (<20%).

Minibatch size. While the minibatch size does not affect the speedup of GradPIM over the update phase, it directly affects the portion of the update phase in the entire training. Fig. 12b shows the change in the overall speedup coming from the batch size. While the overall speedup with regard to the minibatch size does not change by a large amount, it shows a continuous trend where smaller batch size leads to higher speedup. Thus GradPIM has better potential for speedup with smaller batch sizes. As we will see in Section VI-E, this will help improve the scaling efficiency for distributed deep learning.

Sensitivity to mixed-precision levels. Fig. 12c and 12d shows the difference on speedup and energy consumption when 8/16 bit, 16/32 bit mixed-precision or full-precision (32/32 bit) is used instead of 8/32 bit as in our default setup. While the speedup of GradPIM highly depends on the ratio between the low-precision and the high-precision representations, the setting of 8/16 bit, 16/32 bit, and 32/32 bit systems still provide meaningful speedups of 1.39×, 1.43×, and 1.26×, respectively. Also, Fig. 12d shows the energy consumption, compared to the baseline no-PIM technique on each precision. It shows a similar trend, since most of the advantage on performance and energy both come from reducing the off-chip bus traffic.

8-bit training is still at a premature status, and 16/32 bit mixed-precision training is dominant on the field. Despite this, we anticipate the onset of lower-bit training in the near future, where GradPIM could bring many benefits to mixed-precision training.

D. Layer Characterizations.

To study the relation between the layer characterizations and the speedups obtained by GradPIM, we show the speedups with regard to weight/activation ratio in Fig. 13 with the X axis in log scale. The plot shows a clear correlation between the weight/activation ratio and the speedup. Usually, for the convolutional layers from the earlier stages of the networks, there are large activation fields, with relatively small filters and the speedup for them are generally small. For the layers from the later stages of the networks, the activation maps get smaller due to the result of repetitive pooling and strided convolutions. These convolutional layers and fully-connected layers often exhibit a very high weight/activation ratio, and the speedup gets larger.

E. Distributed Data Parallelism

To find out the potential for GradPIM to work for distributed data parallel distributed learning, we measured the performance gain over the same set of networks, with a modest number of 4 NPU nodes, each taking a quarter of the minibatch as shown in Fig. 14. We assume the nodes are connected in a torus-like network with 100Gbps connections [75] with HW supporting NI as in [67]. The communication time is depicted as Comm. for the baseline and GradPIM in the legend. Due to the smaller effective batch size per node, GradPIM shows much better scalability compared to the baseline, and the performance is almost 2× better than the baseline with distributed training.

VII. RELATED WORK

Placing a logic inside DRAM is not entirely new, and in fact has a long history of work accumulated over a few decades. Starting from execube [60] in the 1990s, there has been much work on integrating processor and memory on a single die [52], [58], [72], [81], but without commercial success.

The idea of PIM revived in mid-2010s, with the aid of 3D stacking technology [14], [15], [68], [83], [104], [105], [107]. By placing a logic die underneath a few memory dies, processing logic could be placed together with the memory cells without having to share the same silicon technology of the memory that slows down the processing speed. Meanwhile, there were attempts to exploit the inherent structure of the existing DDR family to perform a certain class of executions [18], [40], [63], [88], [89], [90]. UpMem [35] has fabricated a processor within a memory die and claims that it can obtain a multifold speedup of the various applications.

DNN as a surging application is another strong driving force towards PIMs. For example, Neurocube [54] executes DNNs using a 3D stacked memory. One major stream of work tries to modify the cell array structure to perform massively parallel DNNs operations within DRAM [34], [48], [65], [92], [97], SRAM [12], [13], [51], [103], and emerging
memories [19], [20], [29], [42], [46], [66], [91], [95]. However, these technologies all require changing the cell structure itself, and implementing on top of the legacy technologies is complicated (e.g., DDR4/5 protocol).

Compared to the solutions above, GradPIM is a cheaper, easily realizable solution. Solutions such as [34], [48], [65], [92], [97] involve re-designing the DRAM core cell array. While these are better at performance, they are much harder to realize as a product. On the other hand, GradPIM only alters the datapath at the global I/O gating, requiring only a small amount of change in the circuitry. We believe approaches similar to GradPIM have more potential to be accepted to the industry in the nearer future as they fit more smoothly to the current DRAM standards.

Bank group-level parallelism (BGLP) [93] is another related work worth mentioning since it exhibits a related idea with our proposal. While not a processing-in-memory work, it decouples the bank group from the other parts of the DRAM. The difference with ours is that they use buffers to relax the scheduling restrictions, and increases the utilization of the internal banks.

Our work is close to TensorDIMM [61], which organizes a specialized DIMM targeting gather and reduction to speedup embedding lookups and tensor manipulations. However, TensorDIMM requires the use of buffer chips to the memory channel, and only utilizes rank internal bandwidth. GradPIM can achieve more speedup as shown in Section VI by utilizing the bank group level parallelism.

VIII. DISCUSSION

Supporting Other Kinds of Parameter Update Algorithms: In this paper, we have demonstrated GradPIM on SGD with momentum and a weight decay term. Some algorithms such as NAG [76] can be supported with GradPIM naturally in the same way. However, there are algorithms that require more complexity, such as a decaying factor [37], [100] or second order momentum [57]. These extra values require access to adjacent rows in a bank group concurrently. Since momentum SGD does not utilize all banks in a bank group at the same time, there is room for these extra parameters to join the computation.

In a rare case where the number of variables is too large (four in our setting), we can run them in multiple passes. In the first pass a separate array is allocated for storing intermediate values, and in the next pass, the row with intermediate values can be accessed with the remaining values. It would slightly degrade the speedup, but the implementation would not be overly complicated. It would require activating and reading the data multiple times, while causing only a small overhead on the overall performance.

Expandability to other applications: In this paper, we have focused on DNN parameter update as the target for GradPIM. However, there are possibilities for supporting other applications without modifying the GradPIM architecture too much. In fact, most of the element-wise applications such as table scan [38], histogram construction [21] or B-trees [31]. It requires change in the ALU of the GradPIM unit and more generalized command supports. We believe those can be handled with new DRAM standards [7], and leave it as a future work.

Learning Rate Scheduling: One could raise question about how to apply learning rate scheduling, as we have assumed a fixed learning rate in this work. GradPIM can be extended to support varying learning rate. Scaling the values each time by 2 can be easily implemented using a shifter. For more complicated scheduling such as cosine [70] or polynomial decay [106], we may choose to approximate the decaying function as computing the exact value of them is expensive. Another way would be to utilize the mode register and let the NPU provide the new learning rate value, at the expense of some performance overhead.

IX. CONCLUSION

We have proposed GradPIM, a practical PIM design based on the extension of the DDR4 protocol for DNN training. We have demonstrated that GradPIM can speed up the update phase of the DNN training up to around $8 \times$, leading to overall $1.94 \times$ performance gain. GradPIM poses only a negligible overhead to the DRAM and is fully controlled by the memory controllers. Even though the proposed design is based on DDR4 SDRAM, we believe similar designs can be adopted to other memories such as HBM, HMC or GDDR. It is expected to show similar speedups or improvement if we exploit more bank group numbers in advanced memory technologies toward high-performance NPU.

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REFERENCES

[1] “8Gb: x4, x8, x16 DDR4 SDRAM.” [Online]. Available: https://www.micron.com/-/media/client/global/documents/products/data-sheet/dram/ddr4/8gb_ddr4_sram.pdf

[2] “Cloud tensor processing units (tpus).” [Online]. Available: https://cloud.google.com/tpu/docs/tpus

[3] “Data sheet: Quadro gv100.” [Online]. Available: https://www.nvidia.com/content/dam/en-zz/Solutions/design-visualization/products/page/quadro/quadro-desktop/quadro-volta-gv100-data-sheet-us-nvidia-704619-r3-web.pdf

[4] “DDR3 SDRAM specification.” [Online]. Available: https://www.jedec.org/sites/default/files/docs/JESD79-3F.pdf

[5] “DDRR SDRAM specification.” [Online]. Available: https://www.jedec.org/sites/default/files/docs/JESD79-4.pdf

[6] “DDR4 SDRAM system-power calculator.” [Online]. Available: https://media-www.micron.com/-/media/client/global/documents/products/power-calculator/ddr4_power_calculator.xlsm?la=en&rev=5e97be39078441a1b619c1858b596b63

[7] “DDR5 full spec draft rev0.1.” [Online]. Available: http://www.softnology.biz/pdf/JESD79-5%20Proposed%20Rev0.1.pdf

[8] “Intel® AVX-512 instructions.” [Online]. Available: https://software.intel.com/en-us/articles/intel-avx-512-instructions
S. Angizi, Z. He, and D. Fan, “ParaPIM: a parallel processing-in-memory platform,” in *ICCAD*, 2015.

Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: A spatial architecture for near-data processing,” in *ISCA*, 2016.

Y.-H. Chen, J. Emer, and V. Sze, “Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks,” in *ISCA*, 2016.

Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: An efficient, reconfigurable, and scalable processor for deep neural networks,” in *IEEE journal of solid-state circuits*, vol. 52, no. 1, pp. 127–138, 2016.

S. Chetlur, C. Woolley, P. Vandermersch, J. Cohen, J. Tran, B. Catanzaro, and E. Shelhamer, “cudnn: Efficient primitives for deep learning,” *arXiv preprint*, 2014.

P. Chu, S. Li, C. Xu, T. Zhang, J. Zhao, Y. Liu, Y. Wang, and Y. Xie, “Prime: A novel processing-in-memory architecture for neural network computation in ream-based main memory,” in *ISCA*, 2016.

C. Choi, “Multi-stream write SSD,” in *Flash Memory Summit*, 2016.

H. Custer, *Inside the windows NT File System*. Microsoft Press, 1994.

D. Das, S. Avancha, D. Mudigere, K. Vaidyanathan, S. Sridharan, D. Kalamkar, B. Kaul, and P. Dubey, “Distributed deep learning using synchronous stochastic gradient descent,” *arXiv preprint*, arXiv:1602.06709, 2016.

D. Das, N. Mellemputdi, D. Mudigere, D. D. Kalamkar, S. Avancha, B. Banerjee, S. Sridharan, K. Vaidyanathan, B. Kaul, E. Georganas, A. Heinecke, P. Dubey, J. Corbal, N. Shustrov, R. Dubtsov, E. Fomenko, and V. O. Pirogov, “Mixed precision training of convolutional neural networks using integer operations,” in *ICLR*, 2018.

Q. Dong, L. Jiang, Y. Zhang, M. Zhang, and J. Yang, “DrAec: A dram based accelerator for accurate cnn inference,” in *DAC*, 2018.

F. Devaux, “The true processing in memory accelerator,” in *HCS*, 2019.

Z. Du, R. Fasthuber, T. Chen, P. Ienne, L. Li, T. Luo, X. Feng, Y. Chen, and A. Heinecke, “Shidiannai: Shifting vision processing closer to the sensor,” in *ISCA*, 2015.

J. Duchi, E. Hazan, and Y. Singer, “Adaptive subgradient methods for online learning and stochastic optimization,” *Journal of machine learning research*, vol. 12, no. Jul, pp. 2121–2159, 2011.

F. Färber, S. K. Cha, J. Primsch, C. Bornhövd, S. Sigg, and W. Lehner, “Sap hana database: data management for modern business applications,” in *ACM Sigmod Record*, vol. 40, no. 4, pp. 45–51, 2012.

A. Farmahini-Farahani, J. H. Ahn, K. Morrison, and N. S. Kim, “NDA: Near-dram acceleration architecture leveraging commodity dram devices and standard memory modules,” in *HPCA*, 2015.

F. Gao, G. Tziantzoulis, and D. Wentzlaff, “ComputeDRAM: In-memory compute using off-the-shelf drams,” in *MICRO*, 2019.

V. Gokhale, J. Jin, A. Dandar, B. Martin, and E. Culurciello, “A 240 g-ops/s mobile coprocessor for deep neural networks,” in *CVP*, 2014.

Q. Guo, X. Guo, R. Patel, E. Ipek, and E. G. Friedman, “AC-DIMM: associative computing with stt-mram,” in *ISCA*, 2013.

J. Haas and P. Vogt, “Fully-buffered dimm technology moves enterprise platforms to the next level,” *Technology*, p. 1, 2005.

K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in *CVPR*, 2016.

N. J. Higham, “The accuracy of floating point summation,” *SIAM Journal on Scientific Computing*, vol. 14, no. 4, pp. 783–799, 1993.

M. Imani, S. Gupta, Y. Kim, and T. Rosing, “Floatpim: In-memory acceleration of deep neural network training with high precision,” in *ISCA*, 2019, pp. 802–815.

J. Ahn, S. Yoo, O. Mutlu, and K. Choi, “PIM-enabled instructions: a low-overhead, locality-aware processing-in-memory architecture,” in *ISCA*, 2015.

M. Alian, S. W. Min, H. Asgharimoghadam, A. Dhar, D. K. Wang, T. Roewer, A. McPadden, O’Halloran, D. Chen, J. Xiong, D. Kim, W. Hwu, and N. S. Kim, “Application-transparent near-memory processing architecture with memory channel network,” in *MICRO*, 2018, pp. 802–814.

M. Alwani, H. Chen, M. Ferdman, and P. Milder, “Fused-layer CNN accelerators,” in *MICRO*, 2016.

S. Angizi and D. Fan, “RedDRAM: A reconfigurable processing-in-DRAM platform for accelerating bulk-wise operations,” in *ICCAD*, 2019.

S. Angizi, Z. He, and D. Fan, “Dima: a depthwise CNN in-memory accelerator,” in *ICCAD*, 2018.

S. Angizi, Z. He, and D. Fan, “ParaPIM: A parallel processing-in-memory accelerator for binary-weight deep neural networks,” in *ASPDAC*, 2019.

A. Ankit, I. E. Hajj, S. R. Chalamalasetti, G. Ndu, M. Foltin, R. S. Williams, P. Faraboschi, W.-m. W. Hwu, J. P. Strachan, K. Roy, and D. S. Williams, “PUMA: A programmable ultra-efficient memristor-based accelerator for machine learning inference,” in *ASPLOS*, 2019.

A. Boroumand, S. Ghose, Y. Kim, R. Ausavarungnirun, E. Shiu, R. Thakur, D. Kim, A. Kuselua, A. Knies, P. Ranganathan, and O. Mutlu, “Google workloads for consumer devices: Mitigating data movement bottlenecks,” in *ASPLOS*, 2018.

S. Chakradhar, M. Sankaradas, V. Jakkula, and S. Cadambi, “A dynamically configurable coprocessor for convolutional neural networks,” in *ISCA*, 2010.

T. Chen, Z. Du, N. Sun, J. Wang, C. Wu, Y. Chen, and O. Temam, “Dianmao: A small-footprint high-throughput accelerator for ubiquitous machine-learning,” in *ASPLOS*, 2014.

Y. Chen, T. Luo, S. Liu, S. Zhang, L. He, J. Wang, L. Li, T. Chen, Z. Xu, N. Hsu, and J. Hsu, “Dadiannao: A machine-learning supercomputer,” in *MICRO*, 2014.

Y.-H. Chen, J. Emer, and V. Sze, “Eyeriss: A spatial architecture for energy-efficient dataflow for convolutional neural networks,” in *ISCA*, 2016.

Y.-H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” *IEEE journal of solid-state circuits*, vol. 52, no. 1, pp. 127–138, 2016.

S. Chetlur, C. Woolley, P. Vandermersch, J. Cohen, J. Tran, B. Catanzaro, and E. Shelhamer, “cudnn: Efficient primitives for deep learning,” *arXiv preprint*, 2014.

P. Chu, S. Li, C. Xu, T. Zhang, J. Zhao, Y. Liu, Y. Wang, and Y. Xie, “Prime: A novel processing-in-memory architecture for neural network computation in ream-based main memory,” in *ISCA*, 2016.

C. Choi, “Multi-stream write SSD,” in *Flash Memory Summit*, 2016.

H. Custer, *Inside the windows NT File System*. Microsoft Press, 1994.

D. Das, S. Avancha, D. Mudigere, K. Vaidyanathan, S. Sridharan, D. Kalamkar, B. Kaul, and P. Dubey, “Distributed deep learning using synchronous stochastic gradient descent,” *arXiv preprint*, arXiv:1902.06709, 2019.

D. Das, N. Mellemputdi, D. Mudigere, D. D. Kalamkar, S. Avancha, B. Banerjee, S. Sridharan, K. Vaidyanathan, B. Kaul, E. Georganas, A. Heinecke, P. Dubey, J. Corbal, N. Shustrov, R. Dubtsov, E. Fomenko, and V. O. Pirogov, “Mixed precision training of convolutional neural networks using integer operations,” in *ICLR*, 2018.

Q. Dong, L. Jiang, Y. Zhang, M. Zhang, and J. Yang, “DrAec: A dram based accelerator for accurate cnn inference,” in *DAC*, 2018.
