Silicon Mode-Selective Switch via Horizontal Metal-Oxide-Semiconductor Capacitor Incorporated With ENZ-ITO

Weifeng Jiang*, Jinye Miao & Tao Li

A silicon mode-selective switch (MSS) is proposed by using a horizontal metal-oxide-semiconductor (MOS) capacitor incorporated with the epsilon-near-zero (ENZ) indium-tin-oxide (ITO). The carrier concentration of the double accumulation-layers in ITO can be adjusted via the applied gate-voltage to achieve the desired switching state. The MOS-type mode of the central MOS-capacitor based triple-waveguide coupler is introduced and optimised by using the full-vectorial finite element method to switch the “OFF” and “ON” states. The thickness of the accumulation layer and the optimal design are studied by using the 3D full-vectorial eigenmode expansion method. The optimised quasi-TE₀ and quasi-TE₁, modes based MSSes are with the extinction ratios of 28.52 dB (19.05 dB), 37.29 dB (17.8 dB), and 37.29 dB (23.7 dB), at “OFF” (“ON”) states for the accumulation-layer thicknesses of 1.5, 5.0, and 10.0 nm, respectively. The operation speed can achieve to be 6.3 GHz, 6.2 GHz, and 6.2 GHz for these three accumulation-layer thicknesses, respectively. The performance of the proposed MSS with a 2.5 V gate-voltage is also studied for preventing the oxide breakdown. The proposed MSS can be applied in the mode-division-multiplexing networks for signal switching and exchanging.

Mode division multiplexing (MDM) technology is of great promise to overcome the communication bottleneck and to achieve a dramatic capacity-enhancement for optical transmission networks. Silicon photonics show attractive characteristics to realise compact, low-cost, and CMOS-compatible optical devices. To build on-chip MDM systems, various silicon based building blocks have been demonstrated, including the mode (de)multiplexers (MD/MUXes), multimode power-splitters, multimode bent waveguides/crossings, and mode-selective switches (MSSes). Among these devices, an MSS is the basic and critical component for flexible mode-routing and switching to achieve a reconfigurable MDM network.

Recently, a few approaches have been reported to build a silicon MSS for reconfigurable MDM networks, including the micro-ring resonators (MRRs), Mach–Zehnder interferometers (MZIs), multimode interference (MMI) couplers, and triple-waveguide couplers (TWCs). Stern et al. firstly demonstrated a 1 × 2 multimode switch based on the MRRs. The mode crosstalk (XT) ranging from −16.8 to −24.0 dB and the measured insertion loss (IL) of 5.4–9.1 dB can be achieved for four different channels. However, the MRRs may degenerate the operating bandwidth due to the critical resonating-condition. In addition, this approach is based on the relatively complicated demultiplexing-switching-multiplexing (DSM) process: the input multimode signals are demultiplexed to the fundamental modes and then switching them by using the single-mode (SM) switches; finally, these SM signals are multiplexed to the desired output modes. Yang et al. proposed a general architecture for on-chip mode switching and demonstrated a thermo-optic (TO) 2 × 2 four-mode switch based on the DSM process. In order to simplify the MSS configuration, Sun et al. presented a 2 × 2 multimode switch, consisting of a pair of 1 × 1 MZI and TO based multimode switches and a pair of MRR based 2 × 2 SM switches. A low IL of <1.2 dB and a low XT of <−16.6 dB can be measured for all channels and the footprint is 433 µm × 433 µm. Another approach could be the use of the MMI couplers to build an MSS. Priti et al. proposed and experimentally demonstrated an MSS based on the MMI couplers and TO phase-shifters. A switching extinction ratio (ER) of >25 dB and a mode XT of <−12 dB were measured over the C-band. Xiong et al. demonstrated a 1 × 2 two-mode switch based on an MZI schematic and the electro-optic (EO) effect. A short switching-time of <2.5 ns and...
In this paper, we propose and optimise a TWC based silicon MSS, consisting of two silicon outer waveguides (WGs) and a central horizontal MOS-capacitor incorporated with the ENZ-ITO, as shown in Fig. 1. A double-carrier-accumulation scheme offers the large phase-change and high switching-efficiency by using the horizontal Si/HfO2/ITO/HfO2/Si MOS-capacitor. This paper is organised as follows. In Section II-A, the schematic and principle of the proposed MSS are described in detail. In Section II-B, we study the electrical properties implemented. However, the vertical stacking structure suffers from the limited design-flexibility and may not be compatible with other on-chip components. In that sense, it would be preferred to design a carrier-accumulation based silicon MSS via a horizontal MOS-capacitor.

In order to increase the light-matter-interaction (LMI) inside the silicon switch, the TWC based configurations incorporated with phase-change materials (PCMs) and transparent conducting oxides (TCOs), including Ge2Sb2Te5 (GST)26, Ge2Sb2Se4Te1 (GSST)19, indium-tin-oxide (ITO)20, have been emerging as a promising approach to achieve an ultra-compact, broadband, and low-loss MSS. A nonvolatile and ultra-low-loss reconfigurable mode (De)MUX/switch has been reported based on a silicon TWC with the GST-PCM19, which can achieve a compact coupling length of only 29.3 μm, a broad bandwidth covering S + C + L band, ultra-low ILs of 0.10 and 0.68 dB, and high mode ERs of 18.98 and 22.18 dB at “OFF” and “ON” states, respectively. Benefitting from the unique property of the epsilon-near-zero (ENZ) effect of the ITO-TCO, a reconfigurable mode (De)MUX/switch was numerically proposed by using a silicon TWC incorporated with a vertical metal-oxide-semiconductor (MOS) capacitor and an ITO layer27. A more compact length of 8.429 μm, an ultra-high switching-speed of 0.781 THz, and a low power-consumption of 11.74 fJ/bit can be achieved based on the carrier accumulation at the ENZ point. A silicon reconfigurable add/drop filter was demonstrated based on a vertical Si–SiO2–graphene capacitor27, which can overcome the need for continuous heating to keep switch on the carrier accumulation state. The vertical MOS-capacitor is based on the vertical multilayers, which can be deposited in sequence and then etched together. The horizontal MOS-capacitor is based on the lateral multilayers, which requires the multi-depositing and multi-etching processes38. The advantages of the vertical MOS-capacitor are as follows: the vertical MOS-capacitor is easier to fabricate and can be operating for the quasi-TM mode as a horizontal slot is implemented. However, the vertical stacking structure suffers from the limited design-flexibility and may not be compatible with other on-chip components. In that sense, it would be preferred to design a carrier-accumulation based silicon MSS via a horizontal MOS-capacitor.

In this paper, we propose and optimise a TWC based silicon MSS, consisting of two silicon outer waveguides (WGs) and a central horizontal MOS-capacitor incorporated with the ENZ-ITO, as shown in Fig. 1. A double-carrier-accumulation scheme offers the large phase-change and high switching-efficiency by using the horizontal Si/HfO2/ITO/HfO2/Si MOS-capacitor. This paper is organised as follows. In Section II-A, the schematic and principle of the proposed MSS are described in detail. In Section II-B, we study the electrical properties of the ITO material to reveal the carrier-accumulation based ENZ effect. In Section II-C, the modal characteristics of the MOs-type mode and the phase-matching condition are investigated for both “OFF” and “ON” states. In Section II-D, the operation and performance of MSS are presented and studied.

Results

Schematic and principle. The schematic diagram of the proposed MSS based on a silicon TWC is shown in Fig. 1(a), consisting of a central horizontal-MOS-capacitor incorporated with ENZ-ITO, an input WG with input port I1 and output port O1, and a bus WG with input/output ports I2/O2. The length of the MOS-capacitor is equal to the coupling length of the TWC, denoted by Lc in Fig. 1(a). In order to minimise the mode XT, an S-bend WG with the offset of Sx × Sy is implemented in between the straight input- and output-sections of the input WG. The length of the straight section of the input WG is denoted by L. The cross-section of the TWC is shown in Fig. 1(b), in which the widths of the input, central, and bus WGs are represented by W1, Wp, and W2, respectively. The gap between the central and input/bus WGs is denoted by g. The whole device is covered with the SiO2 cladding and is based on the rib WG. The heights of the rib WG and the slab are chosen to be h = 220 nm and hslab = 30 nm, respectively. To be clear, only the P and P++ doped silicon slabs are shown in Fig. 1(a). The heavily doped silicon would lead to an increased propagation loss. For the silicon WGs connected to the doped slabs, the
Accordingly, the ITO state would be changed from the dielectric state to the “quasi-metallic” state and finally to it's decreased with the increase of the carrier concentration, while the imaginary permittivity is increased. 1550 nm (solid red line), and 1600 nm (dotted black line), respectively. It can be noted that the real permittivity in Fig. 3 at the wavelengths of 1500 nm (dash-dotted blue line), and 1550 nm (solid red line) is preferred to reduce the propagation loss due to doping. For the slabs connected to the electrodes, the heavily P++ doping concentration of 1 × 10^{18} cm^{-3} is chosen to achieve ohmic contacts with the electrodes. In order to circumvent the influence of the electrodes and P++ doped slabs on the optical performance, they are placed 1.0 μm away from the centre of two outer WGs. As the whole device is covered with the SiO2 cladding, the ITO deposition window is opened using the second e-beam lithography process. An ITO film is then sputtered on the wafer and then the lift-off process is used to remove the ITO outside the deposition window. Finally, the electrical contact for ITO can be formed along with the waveguide. As the width of the ITO section was chosen as W_{ITO} = 50 nm as stated in Section II-C, the mode field in the upper ITO surrounded by cladding is cutoff, thereby the effect to the optical characteristics would be relatively slight. The non-ideal etched sidewalls would induce a strong optical absorption. The sidewalls of the vertical slot waveguides filled with ITO materials should be etched smoothly and accurately to avoid the optical absorption.

The horizontal MOS-capacitor is comprised of the stacked Si/HfO2/ITO/HfO2/Si layers, as illustrated in Fig. 1(b). The refractive indices of the Si, SiO2, and HfO2 are set to be 3.47548, 1.46, and 1.98, respectively. The detailed configuration of the MOS-capacitor is shown in Fig. 2(a). The widths of the ITO, HfO2, and Si layers are denoted by W_{ITO}, W_{HfO2}, and W_{Si}, respectively. When a negative gate-voltage is applied on the ITO layer, electrons accumulate at both the right and left ITO/HfO2 interfaces to form double accumulation-layers (ACLs) and then the carrier density will be correspondingly increased inside two nanometer ACLs in the ITO, as shown in Fig. 2(b). Sequentially, the complex index of the ACLs in the ITO will be changed. It can be noted from Fig. 2(c) that the real part of the refractive index can be reduced to be close to near zero with an optimal applied gate-voltage at “ON” state, which can induce the ENZ effect. The operation principle of the proposed MSS is described as follows. (i) At “OFF” state, the phase-matching condition between three WGs of the TWC can be satisfied without any applied gate-voltage. The input quasi-TE0 mode can be multiplexed to the quasi-TE1 mode; the central MOS-type mode can be achieved due to the ENZ effect and then the phase-matching condition will be destructed. The input quasi-TE_{0} mode will be switched back into the input WG and outputs at port O_{1}. Once the device is in the “ON” or “OFF” state, the capacitive effect does not need electrical current flow to keep the operating state. In addition, the proposed schematic could be exploited as a modulator instead of switch.

**Electrical characteristics of ENZ-ITO.** The electrical characteristics of the ENZ-ITO are critical to the proposed double-carrier-accumulation based silicon MSS. The permittivity of the ITO layer can be calculated by using the well-known Drude-Lorentz model:

\[ \varepsilon = \varepsilon_{\infty} - \frac{\omega_p^2}{\omega(\omega + j\gamma)} \]

\[ \omega_p^2 = \frac{N_e^2}{\varepsilon_0 m^*} \]

where \( \varepsilon_{\infty} = 3.9 \) is the permittivity of the high-frequency ITO; \( \omega \) is the angular momentum in rad/s; \( \gamma = 1.84 \times 10^{14} \text{rad/s} \) is the electron scattering rate; \( \omega_p \) is the plasma frequency; \( \varepsilon_0 \) is the vacuum permittivity; \( e \) is the elementary electron charge; \( m^* = 0.35 m_e \) is the effective mass of the electron; \( m_0 \) is the rest mass of the electron; \( N_e \) is the carrier concentration.

Variations of the real part (left y-axis) and imaginary part (right y-axis) of the complex permittivity of the ITO with the carrier concentration are shown in Fig. 3 at the wavelengths of 1500 nm (dash-dotted blue line), 1550 nm (solid red line), and 1600 nm (dotted black line), respectively. It can be noted that the real permittivity is decreased with the increase of the carrier concentration, while the imaginary permittivity is increased. Accordingly, the ITO state would be changed from the dielectric state to the “quasi-metallic” state and finally to...
Next, both the carrier concentration and the thickness of the ACL are investigated with respect to the applied gate-voltage. The carrier concentration in the ITO-ACL can be estimated by the following formula:

\[
N_c = N_d + \varepsilon_{\text{ITO}} \cdot \frac{\varepsilon_{\text{HfO}_2} \cdot V_g}{\varepsilon_{\text{HfO}_2} \cdot W_{\text{ACL}}} + \frac{\varepsilon_{\text{HfO}_2} \cdot V_g}{\varepsilon_{\text{HfO}_2} \cdot W_{\text{ACL}}}
\]

where \(\varepsilon_{\text{HfO}_2} = 25\) is the DC permittivity of the HfO\(_2\); \(V_g\) is the applied gate-voltage; \(N_d\) is the intrinsic carrier density of the bulk ITO film. In this case, an electron carrier-concentration of \(N_d = 10^{20} \text{ cm}^{-3}\) is chosen for the ITO layer to match its real permittivity with that of its adjacent HfO\(_2\) layer. For the width of the HfO\(_2\) layer, \(W_{\text{HfO}_2}\), it can be noted from Eq. (3) that a thinner HfO\(_2\) layer would induce a lower gate-voltage. However, the MOS capacitance would also be increased with a thinner HfO\(_2\) layer, which would reduce the switching speed. Hence, the width of the HfO\(_2\) layer should be chosen to balance the power consumption and the switching speed. In this work, the width of the HfO\(_2\) layer is chosen to be \(W_{\text{HfO}_2} = 10 \text{ nm}\). \(W_{\text{ACL}}\) is the width of the ACL. There are several papers assuming that the ACL is equivalent to be with the uniform concentration and with the certain ACL-thickness ranging from 1.0 to 10 nm. A thicker ACL would provide a higher switching-efficiency benefiting from the enhancement of the LMI inside the device. Actually, the accurate carrier distribution should be experimentally measured. In this work, different ACL thicknesses, \(W_{\text{ACL}}\), will be studied to reveal their effects on the switching performance.

Variations of the carrier concentration in the ACLs with the applied voltage and ACL thickness, \(W_{\text{ACL}} = 1.5, 5.0,\) and \(10.0 \text{ nm}\), respectively at the wavelength of 1550 nm. The ENZ region is highlighted by the gray area under the ITO real-permittivity in between \(-1.0\) and \(1.0\), corresponding to the carrier concentration in between \(N_c = 4.8 \times 10^{20}\) and \(8.135 \times 10^{20} \text{ cm}^{-3}\).
in between $N_c = 4.8 \times 10^{20}$ and $8.135 \times 10^{20}$ cm$^{-3}$. It can be noted from Fig. 4 that the applied gate-voltage for the ENZ region is decreased with the decrease of the width of the ACL. Hence, the power consumption and the switching-efficiency should be balanced according to the ACL width.

**MOS-Type mode and phase-matching.** The MOS-type mode of the proposed horizontal MOS-capacitor plays a key role in the silicon MSS. In this Section, the isolated modes of the silicon WGs, supermodes of the TWC, and MOS-type mode of the central MOS-capacitor are studied by using the full-vectorial finite element method (FV-FEM). The coupling length, $L_c$, is optimised according to the phase-matching condition at “OFF” state. The effective indices of the isolated silicon rib-WGs are calculated and shown in Fig. 5. The effective index of the quasi-TE$_0$ mode of the input rib-WG with the size of $h \times W_1 = 220$ nm $\times$ 400 nm is calculated to be $n_{eff} = 2.2989$, denoted by a horizontal dashed-black line in Fig. 5. The phase-matched widths are chosen to be 860 nm and 1.32 $\mu$m for the quasi-TE$_1$ and quasi-TE$_2$ modes, respectively. In this case, the MSS for handling the quasi-TE$_0$ and quasi-TE$_1$ modes is considered as an example to explain the operation principle. But, even higher-order modes can also be handled based on the proposed mechanism.

Although the phase-matched widths of the input and bus WGs can be obtained based on the isolated mode-condition, that of the MOS-capacitor based central WG needs to be investigated based on the supermodes and phase-matching condition of the TWC at “OFF” state. The supermodes of the TWC are calculated by using the FV-FEM and the Poynting vector, $P_z(x, y)$ field profiles of the TE-A, TE-B, and TE-C supermodes are shown in Fig. 6. Here, parameters for FV-FEM simulation: $W_1 = 400$ nm, $W_2 = 860$ nm, $W_{ITO} = 50$ nm, $W_{HfO_2} = 10$ nm, $W_{si} = 307.5$ nm, $h = 220$ nm, $h_{slab} = 30$ nm, and $g = 200$ nm.

![Figure 5](#) Variations of the effective index with the width of the silicon rib waveguide. Here, the heights of the slab and the silicon rib waveguide are set as $h_{slab} = 30$ nm and $h = 220$ nm, respectively. The effective index of the input waveguide with size of 220 nm $\times$ 400 nm is calculated to be 2.2989 using FV-FEM, denoted by a horizontal dashed-black line.

![Figure 6](#) Supermode fields of the phase-matched triple-waveguide coupler based on the FV-FEM simulation. Poynting vector, $P_z(x, y)$ field profiles of (a) TE-A, (b) TE-B, and (c) TE-C supermodes. Here, parameters for FV-FEM simulation: $W_1 = 400$ nm, $W_2 = 860$ nm, $W_{ITO} = 50$ nm, $W_{HfO_2} = 10$ nm, $W_{si} = 307.5$ nm, $h = 220$ nm, $h_{slab} = 30$ nm, and $g = 200$ nm.
$N_c = 1 \times 10^{21}$ and $5.5 \times 10^{20}$ cm$^{-3}$ at “ON” state, respectively. In next Section, the carrier concentration will be optimised according to the performance of the optimal design at “ON” state.

In order to further explain the mechanism of the MOS-type mode based MSS, 1D plots of the amplitude of the $E_x$ fields of the supermodes are illustrated in Fig. 8(a,b) for the “OFF” and “ON” states, respectively. As the MOS-type modes are only existed in the TE-A and TE-C supermodes, shown in Fig. 6, the $E_x$ fields of these two supermodes are presented in Fig. 8(a). At “OFF” state, the $E_x$ fields of both supermodes in the MOS-capacitor are mainly confined in two HfO$_2$ layers, as shown in the inset of Fig. 8(a). This can be explained that the $E_x$ field undergoes a large discontinuity due to the big index-difference between the silicon and oxide layers, which can make the field mainly confined in the low-index oxide slot. The oxide slot is comprised of the HfO$_2$/ITO/HfO$_2$ layers. Although an optimal electron carrier-concentration is chosen to match the real index between the HfO$_2$ (1.98) and ITO (1.96 + 0.003i) at “OFF” state, the $E_x$ field still undergoes the discontinuity due to the different imaginary-indices and is mainly confined in the HfO$_2$ layers. It can be noted from Fig. 8(b) that the $E_x$ fields of the TE-A and TE-C supermodes are squeezed into the ACLs at “ON” state. The enlarged view of the $E_x$ fields in the oxide layers is shown in Fig. 8(b) as an inset. As the ACLs turn to the “quasi-metallic” state at “ON” state, the “oxide slot” is comprised of the HfO$_2$/ACL/ITO/ACL/HfO$_2$ layers, which can squeeze the $E_x$ fields into the ultra-low-index ACLs. Therefore, the phase-condition can be significantly changed at “ON” state.

In this case, the device length is depended on the coupling length, $L_c$, which can be calculated based on the formula:

$$L_c = \frac{\lambda}{2(n_A - n_B)}$$

Variations of the coupling length with both the gap and width of the ITO are shown in Fig. 9 under the phase-matching conditions. It can be noted from Fig. 9 that the coupling length is increased with the increases of both gap and W$_{ITO}$. As a compact $L_c$ is preferred, a smaller gap and a narrower width of the ITO layer would be better. The width of the ITO layer is W$_{ITO} = 50$ nm considered in this case.

**Operation and performance of mode-selective switch.** In this Section, the propagation performance of the proposed MSS is studied by using the three-dimensional full-vectorial eigenmode expansion (3D-FV-EME) method. In this case, the mesh size of the MOS-capacitor is extremely critical for the rigorous simulation due
to the thickness of the ACLs in between 1.0 nm to 10 nm. For the HfO$_2$/ITO/HfO$_2$ layers, an extremely small mesh-size of 0.1 nm was applied in the $x$-axis and 10 nm was used for the $y$-axis. For the other regions in the computation window, the mesh sizes in both the $x$- and $y$-axes were set to be 10 nm. An MSS with the gap of $g = 200$ nm is studied firstly and then variations of both the gap and ACL thickness are also investigated in detail.

In order to minimise the mode XT, an S-bend WG with the size of $S_0 \times S_L = 2.0 \mu m \times 15 \mu m$ is implemented in the input WG, as shown in Fig. 1(a). The position of the S-bend WG is optimised according to the mode XT by using the 3D-FV-EME method. Variations of the mode conversion efficiency (left $y$-axis) and normalised residual power in the input WG (right $y$-axis) at “OFF” state with the ratio between the length of the straight input-waveguide-section and the coupling length, $L/L_c$, are shown in Fig. 10 for $g = 200$ nm and phase-matched $W_{si} = 307.5$ nm. It can be noted that the optimal length of the straight section of the input WG is chosen to be $L = 17.0 \mu m$ for the ratio, $L/L_c = 0.52$ close to the midpoint of the input WG. The mode conversion efficiency and the normalised residual-power in the input WG can achieve to be 0.9238 and $1.725 \times 10^{-4}$, respectively. The mode XT, calculated based on $XT = -(ER - IL)^2$, can be dramatically decreased to be $-37.63$ dB by introducing an S-bend WG. The ER and IL are calculated to be 37.29 and $-0.34$ dB, respectively at “OFF” state.

Next, the effects of the ACL thickness, $W_{acc}$, and the gap, $g$, on the switching performance are investigated at “ON” state. Variations of the normalised transmittance with the carrier concentration are calculated by using the 3D-FV-EME method and shown in Fig. 11 for the gap, $g = 200$ nm and phase-matched $W_{si} = 307.5$ nm. It can be noted that the optimal length of the straight section of the input WG is chosen to be $L = 17.0 \mu m$ for the ratio, $L/L_c = 0.52$ close to the midpoint of the input WG. The mode conversion efficiency and the normalised residual-power in the input WG can achieve to be 0.9238 and $1.725 \times 10^{-4}$, respectively. The mode XT, calculated based on $XT = -(ER - IL)^2$, can be dramatically decreased to be $-37.63$ dB by introducing an S-bend WG. The ER and IL are calculated to be 37.29 and $-0.34$ dB, respectively at “OFF” state.

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To achieve the switching performance, the ratio between the length of the straight input-waveguide-section and the coupling length, $L/L_c$, should be adjusted accordingly to meet the phase-matching condition.

Figure 9. Variations of the coupling length with both the gap and width of the ITO under the phase-matching condition based on the FV-FEM. Here, parameters for FV-FEM simulation: $W_{HfO_2} = 10$ nm, $W_1 = 400$ nm, $W_2 = 860$ nm, $h = 220$ nm, and $h_{slab} = 30$ nm. The phase-matched width of the central silicon-section, $W_{si}$, should be adjusted accordingly to meet the phase-matching condition.

Figure 10. Variations of the mode conversion efficiency (left $y$-axis) and normalised residual power in the input waveguide (right $y$-axis) at “OFF” state with the ratio between the length of the straight input-waveguide-section and the coupling length, $L/L_c$. The optimal results with $L = 17.0 \mu m$ are denoted by red dots, which are calculated by using the 3D-FV-EME method.
experimental and theoretical cases. For $W_{\text{acc}} = 5.0 \text{ nm}$ and gap, $g = 200 \text{ nm}$, the mode XT, ER, and IL are calculated to be $-19.21$, $17.8$, and $-1.4 \text{ dB}$ at “ON” state. The propagation electric fields, $|E|$, along $z$-axis at “ON” state is shown in Fig. 12(a), which shows the input quasi-TE0 mode is propagating along the input WG and outputs at port $O_1$. Although the IL is $-1.4 \text{ dB}$ at “ON” state, the power coupled to the bus WG is as small as $1.2\%$. The reason is that the extra power is absorbed by the “quasi-metallic” ACL layers. For the “OFF” state, the propagation field is also calculated and shown in Fig. 12(b). It can be noted that the input quasi-TE0 mode is completely multiplexed to the quasi-TE1 mode of the bus WG. The wavelength dependence of the optimised MSS is calculated by using the 3D-FV-EME method and shown in Fig. 13 for both “OFF” and “ON” states. It can be noted that 3 dB bandwidths are $82.5$ and $100 \text{ nm}$ for the “OFF” and “ON” states, respectively. With the mode XT of $<-15.0 \text{ dB}$, the bandwidth at “OFF” state is calculated to be over $52.3 \text{ nm}$ from $1523.5$ to $1575.8 \text{ nm}$. At “ON” state, the mode XT is lower than $-15.85 \text{ dB}$ over a $100 \text{ nm}$ bandwidth.

Although the performance of the optimised MSS with the ACL-thickness, $W_{\text{acc}} = 5.0 \text{ nm}$ and gap, $g = 200 \text{ nm}$ has been studied, variations of the device performance are also investigated with respect to both the ACL-thickness and gap. Variations of the ER at “ON” state (upper-half of left $y$-axis), IL at “OFF” state (lower-half of left $y$-axis), and the coupling length, $L_c$ (right $y$-axis) with the gap are calculated based on the 3D-FV-EME method for $W_{\text{acc}} = 1.5$, $5.0$, and $10.0 \text{ nm}$, respectively. In the simulation, the carrier concentration was set to be $N_c = 6.0 \times 10^{20} \text{ cm}^{-3}$ and the corresponding gate-voltages are $6.4$, $21.35$, and $42.7 \text{ V}$ for $W_{\text{acc}} = 1.5$, $5.0$, and $10.0 \text{ nm}$, respectively. The parameters of the phase-matched W Si, $L_c$, and $L$ were optimised according to the phase-matching conditions. It can be noted from Fig. 14 that the mode ER is increased with the increase of the gap. The mode ER for $W_{\text{acc}} = 5 \text{ nm}$ is increased from $11.13$ to $62.48 \text{ dB}$ with the gap changing from $g = 100$ to $500 \text{ nm}$. The corresponding propagation electric-fields, $|E|$, are shown as five panels in Fig. 14. However, as the gap is increasing, the coupling length is also going to be longer. The coupling lengths are calculated to be $15.6$, $32.7$, $66.5$, $133.6$, and $267.2 \mu\text{m}$ for $g = 100$, $200$, $300$, $400$, and $500 \text{ nm}$, respectively. Another issue is the IL at...
“OFF” state, which would also be enhanced with the increase of the gap (>200 nm), as shown in the lower-half of left y-axis of Fig. 14. The reason can be explained that with the increased coupling-length for the larger gap, the absorption loss would be increased due to the imaginary index (0.003) of the ITO at “OFF” state. However, for the gap, g = 100 nm, the IL is also slightly increased due to the incomplete coupling-power in the input WG. Therefore, we can state that a large-enough mode ER at “ON” state can be achieved with a wide gap for any ACL-thickness, with the sacrifices of the coupling length and the IL at “OFF” state. It can be noted from Fig. 14 that for Wacc = 1.5 nm, the mode ERs at ON state are 7.22, 13.56, 19.05, and 56.36 dB for gap, g = 200, 300, 400, and 500 nm, respectively. Meanwhile, the IL at “OFF” and “NO” states are −0.34 dB and −3.9 dB, −0.51 dB and −2.1 dB, −1.0 dB and −1.19 dB, −1.3 dB and −0.63 dB for g = 200, 300, 400, and 500 nm, respectively. For Wacc = 5.0 nm, the mode ERs and IL at “ON” state are 17.8 dB and −1.41 dB, 23.9 dB and −0.71 dB, 29.46 dB and −0.38 dB, 62.48 dB and −0.19 dB for g = 200, 300, 400, and 500 nm, respectively. For Wacc = 10.0 nm, the mode ERs and IL at “ON” state are 23.7 dB and −0.76 dB, 29.89 dB and −0.38 dB, 35.4 dB and −0.19 dB, 67.72 dB and −0.1 dB for g = 200, 300, 400, and 500 nm, respectively.

The mode switching speed is limited to the RC delay. The MOS capacitance is calculated based on the formula:

$$C = \frac{\varepsilon_0 \cdot \varepsilon_{\text{HfO}_2} \cdot h \cdot L_C}{W_{\text{HfO}_2}}$$  \hspace{1cm} (4)
The power-consumptions per bit can be calculated from\(^{32}\): \(P_{\text{loss}} = CV_{\text{g}}^2/2\). The resistivity of the HfO\(_2\) doped silicon and ITO are set to be \(10^{12}\), \(2.36\) and \(5 \times 10^{-4}\) \(\Omega \cdot \text{cm}\) according to the reported references\(^{33–35}\). The internal impedances are calculated to be 244.5, 1008.8, and 1008.8 \(\Omega\) for \(W_{\text{acc}} = 1.5, 5.0, \) and 10.0 nm, respectively based on the equivalent RC circuit of our proposed MOS-capacitor. Considering the resistivity and MOS-capacitor structure, the operation bandwidth (BW) can be obtained by \(BW = 1/RC\). The optical and electro-optic performance are summarised in Table 1. For the ACL width, \(W_{\text{acc}} = 5 \) and 10 nm, the gap is chosen to be \(g = 200\) nm for the high optical performance, whereas the gap is increased to be \(g = 400\) nm for \(W_{\text{acc}} = 1.5\) nm. The power-consumptions per bit are increased from tens of fJ/bit for \(W_{\text{acc}} = 1.5\) nm to hundreds of fJ/bit for \(W_{\text{acc}} = 5.0\) and 10.0 nm due to the larger gate-voltage for the wider ACL-width. The operation speeds are calculated to be 6.3, 6.2, and 6.2 GHz for \(W_{\text{acc}} = 1.5, 5.0, \) and 10.0 nm, respectively. Furthermore, the switching speed of our proposed device can be increased via reducing the internal impedance or the MOS capacitance.

The requirement of the higher gate-voltage leads to a great challenge to the HfO\(_2\) layers, which would exceed the breakdown strength and raises the concern of reliability. The performance of our proposed device is also studied with respect to a low \(V_{\text{g}}\) of 2.5 V to prevent the HfO\(_2\) breakdown (5 MV/cm)\(^{36}\). As the applied \(V_{\text{g}}\) was set as 2.5 V, the carrier concentrations of the accumulation layers are calculated to be \(2.4 \times 10^{20}\), \(7.9 \times 10^{20}\), and \(4.45 \times 10^{20}\) \(\text{cm}^{-3}\) for three ACL thicknesses, \(W_{\text{acc}} = 1.5, 5.0, \) and 10.0 nm, respectively. We can note from Fig. 14 that a large-enough mode ER at “ON” state can be achieved with a wide gap, but the coupling length and the IL at “OFF” state would be increased. In order to achieve a reasonably high mode ER, a wide gap of \(g = 600\) nm is chosen as an example for this 2.5 V \(V_{\text{g}}\). The mode ERs at “ON” state are calculated to be 7.7, 7.2, and 6.2 \(\text{GHz}\) for \(W_{\text{acc}} = 1.5, 5.0, \) and 10.0 nm, respectively. The coupling length and the IL at “OFF” state are increased to be \(L = 455\) \(\mu\text{m}\) and \(IL = 1.87\) \(\text{dB}\), respectively. Moreover, the mode ER at “OFF” state is also deteriorated to be 13.0 \(\text{dB}\). In addition, the mode ER at both “ON” and “OFF” states can be further increased via a wider gap between three waveguides, but a longer device would be induced and the loss would also be deteriorated. Hence, a high static permittivity for low power operation and a wide oxide-layer and gap would be preferred to prevent the breakdown and retain a high performance.

### Conclusion

In conclusion, a silicon-MSS has been proposed and optimised based on a horizontal MOS-capacitor incorporated with the ENZ-ITO. The double-carrier-accumulation effect was introduced to enhance the switching efficiency. The permittivity of the ITO as a function of the carrier concentration and the gate voltage has been calculated based on the Drude-Lorentz model. The modal characteristics of the MOS-type mode and supermodes of the TWC have been studied by using the FV-FEM for the phase-matching condition. The propagation performance of the proposed MSS was investigated by using the 3D-FV-EME method. The influence of the ACL-thickness and gap on the device performance has been analyzed. The optimised MSSes for switching the quasi-TE\(_0\) and quasi-TE\(_1\) modes have been achieved for \(W_{\text{acc}} = 1.5, 5.0, \) and 10.0 nm, respectively. With the increase of the gap, any desired mode-ER can be obtained regardless of the ACL thickness. The operation speed and power consumption can reach to 6.3 GHz and 13.32 fJ/bit, 6.2 GHz and 36.29 fJ/bit, 6.2 GHz and 145.2 fJ/bit for Wacc = 1.5, 5.0, and 10.0 nm, respectively. The insertion losses at “OFF” and “ON” states were −0.34 dB, −1.41 dB, and −1.41 dB, −0.34 dB and −0.76 dB for these three ACL thicknesses, respectively. The mode ER at “OFF” state is also deteriorated to be 13.0 dB. In addition, the mode ER at both “ON” and “OFF” states can be further increased via a wider gap between three waveguides, but a longer device would be induced and the loss would also be deteriorated. Hence, a high static permittivity for low power operation and a wide oxide-layer and gap would be preferred to prevent the breakdown and retain a high performance.

### Methods

The electrical characteristics of the epsilon-near-zero indium-tin-oxide (ENZ-ITO) are calculated based on the Drude-Lorentz model. The intrinsic carrier-concentration of \(N_{\text{j}} = 10^{19} \text{cm}^{-3}\) is chosen for the ITO bulk film. The metal-oxide-semiconductor (MOS)-type mode of the proposed horizontal MOS-capacitor is calculated by using the full-vectorial finite element method (FV-FEM). The modal characteristics of the isolated modes of the silicon WGAs and supermodes of the triple-waveguide coupler (TWC) are also calculated based on the FV-FEM. The phase-matching condition of the TWC at “OFF” state is determined by using the FV-FEM. The coupling length is calculated based on the the formulas\(^{38}\): \(L = \pi/2(\beta_{\text{p}} - \beta_{\text{n}})\); where \(\beta_{\text{p}}\) and \(\beta_{\text{n}}\) are the effective indices of the TM-A and TM-B supermodes. The propagation fields, mode crosstalk, mode extinction-ratio, optical bandwidths, and insertion losses of the optimal mode selective switches (MSSes) are obtained by using the three-dimensional full-vectorial eigenmode expansion (3D-FV-EME) method. The operation bandwidth (BW) is calculated by \(BW = 1/RC\). The power-consumptions per bit is calculated from\(^{32}\): \(P_{\text{loss}} = CV_{\text{g}}^2/2\); where \(C\) is the MOS capacitance and \(V_{\text{g}}\) is the applied gate-voltage.

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| \(W_{\text{acc}}\) (nm) | \(W_{\text{acc}}\) (nm) | \(L_{\text{g}}\) (\(\mu\text{m}\)) | IL (dB) | ER (dB) | \(V_{\text{g}}\) (V) | BW (GHz) | E/\(\text{bit}\) (fJ/bit) |
|-----------------|-----------------|-----------------|--------|--------|-----------------|-----------|-----------------|
| 1.5             | 400             | 133.6           | −1.02  | −1.19  | 28.52           | 19.05     | 6.4             | 6.3             | 13.32 |
| 5               | 200             | 32.7            | −0.34  | −1.41  | 37.29           | 17.8      | 21.35           | 6.2             | 36.29 |
| 10              | 200             | 32.7            | −0.34  | −0.76  | 37.29           | 23.7      | 42.7            | 6.2             | 145.2 |

Table 1. Optical and electro-optic performance of the optimised MSS.
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Author contributions

W.F.J. gave the idea and carried out all the simulation work with J.Y.M and T.L. W.F.J. prepared all the figures and wrote up the manuscript text.
Competing interests
The authors declare no competing interests.

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