The Performance of Enhancement MOSFET—The trade-off on Transfer and Output Characteristics

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Abstract. MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is commonly used in electronic devices, and one of its major applications is power switching. The main research topic of the paper is to introduce the principles of functioning of n-channel enhancement MOSFET, discuss the trade-off in MOSFET when one factor is changed in order to improve one aspect of its performance and the method to improve the condition of trade-off. The author analyzes the trade-off problems when improving one of the transfer characteristics and output characteristics of MOSFET, respectively by decreasing the thickness of dielectric layer and changing the length and width of the channel. The author demonstrates the results will occur when decreasing the thickness of dielectric layer and length of channel, and increasing the width of channel; at last author introduces the method to relieve the problems of trade-off by applying third generation semiconductor.

1. Introduction
Currently, the size of the transistor needs to be decreased in order to place more of them into an integrated circuit. An ideal transistor needs to have an excellent performance on its transfer characteristics and output characteristics, high resistance to high voltage and operating temperature. When engineers try to improve one aspect of the devices, there is always a trade-off, meaning that engineers have to make a compromise among the trade-off of all factors.

The first part of the paper analyzes the functioning process of MOSFET from the aspect of its structural design. Then, the paper discusses the transfer and output characteristics of devices, the trade-off for both characteristics when people try to achieve one parameter to an expected magnitude and the side effect occurring respectively when the dielectric layer gets thinner, channel length is decreased, and channel width is increased. At last, the paper introduces the method to improve the trade-off problems by applying third generations semiconductor. The main methods applied in the research are qualitatively analyzing the formula to predict the theoretical change of one factor and comparing the functions using graphs to illustrate the change under different conditions.
2. The Operation of MOSFET

When n-type semiconductor joints with p-type semiconductor, since n-type material contains a large concentration of electrons and few holes (vice versa for p-type material), carrier diffusion occurs, which electrons diffuse to p-side while holes diffuse to n-side and holes diffuse to the opposite direction, leaving p-side fixed negative acceptor ions and n-side positive donor ions near the junction. Thus, space charge region is formed at the junction, and an electric field from n-side to p-side is formed. At the same time, due to this inner electric field, few electrons in p-side drift to n-side and few holes in n-side drift to the p-side, which have the opposite direction with diffusion, causing the space charge region to narrow.

As the process of diffusion and drift reaches balance, the final space charge region is formed, which is also called depletion region, and this region is pn-junction. Pn-junction is commonly used in diode. Under the forward bias, the resistance is low; under the reverse bias, the resistance is extremely high. In MOSFET, two pn-junction are formed between source and substrate and drain and substrate (as the depletion region shown in Fig. 2). When voltage is applied at source and drain, no current flow because there will reverse bias always exist regardless of the direction of otter electric.
However, when there is gate voltage applied, which generates an electric field pointing downwards, the electrons in source and drain will be attracted and flow to the gate. Because of the block of dielectric layer, electrons will concentrate on the channel which is between n+ source and n+ drain. Thus, the current is able to flow through the channel. The gate voltage can control the amount of electrons flows from the source to the drain. This represents the transfer characteristics of MOSFET. The gate voltage should first reach threshold voltage so that transistor has current passing through can leaves off-state; otherwise, even if the gate voltage increases, the drain current is still nearly zero (shown in Fig. 3 as a horizontal line). After threshold voltage is reached, as gate voltage increases, the thickness of channel increases since more electrons are attracted, so the amount of electrons flowing increases; when gate voltage decreases, the thickness of channel decrease, so the amount of electrons flowing decreases. This property of MOSFET is widely used in power switching and resistance control.

Drain voltage also has an effect on channel, and this represents the output characteristic of MOSFET. Under the condition that gate voltage is applied, when a small drain voltage is applied, electrons flows from the source to the drain through the channel. The channel acts as a resistor, and the drain current is proportional to the drain voltage. This can be presented on the graph as linear region (shown in Fig. 4). When the drain voltage increases and reaches saturation voltage, the thickness of the channel near the drain is reduced to zero. This is called the pinch-off point (the red curve in Fig. 4 presents the locus of Vsat vs. Isat). Beyond the pinch-off point, the drain current remains the same. This is the saturation region, where drain current is constant no matter how much the drain voltage increases; In Fig. 4, the saturation region is presented as horizontal lines.

Generally speaking, the keypoints of how n-channel enhancement MOSFET works are that under the control of gate, electrons move from source to drain, and thus current is formed. And the movable carries in MOSFET are attributed to the properties of n-type and p-type semiconductors.
3. Trade-off in MOSFET Devices

3.1. Trade-off for Transfer Characteristics

Nowadays, the transistors are made in the dimension of nanometers, which means each integrated circuit can contain more transistors. Moore’s law points out that the number of transistors placed in an integrated circuit doubles every two years. But problems occur when the size of transistor keeps on decreasing: the dielectric layer in MOSFET will be too thin, which has a negative effect on gate control, and other problems like heat dissipation, leakage current will appear. The limitation to the size of transistor leads to a trade-off problem.

An ideal transistor as a power switching has following characteristics: when power switching is at on-state, it should be switched on immediately and have no power dissipation, meaning the resistance should be zero; when it is at off-state, there’s no leakage current, meaning the resistance should be infinitely high. Let’s first analyze from the aspect of transfer characteristic of an enhancement MOSFET:

As can be seen in Fig. 3, when the VG hasn’t reached VT, the curve is horizontal at where Idrain= 0, this means the power switch can’t be turned to on-state immediately, and there is energy dissipated to turn MOSFET to on-state. Thus, VT should be as small as possible. Below is the formula calculating VT:

\[ V_T = \sqrt{\frac{2\varepsilon q N_s (2\psi)}{C}} + 2\psi \]

Where \( C \), the capacity between the gate and semiconductor, is equal to:

\[ C = \varepsilon \frac{A}{d} \]

When d decrease, C will increase; according to the formula calculating threshold voltage, VT will decrease as a whole. Thus, the horizontal part of the curve in Fig. 3 will be shorter, so the switching frequency can be improved.

However, one problem is that breakdown voltage the layer can stand will be small. Under a relatively big bias, the tunneling current will conduct through dielectric layer, meaning that carriers will move through the layer. According to percolation theory, defects will accumulate in the layer. As this high gate voltage applies for longer time, the higher electric field at gate will give higher energy for carriers. When there will be enough defects to form a chain between the gate and the semiconductor, the breakdown path occurs, and the breakdown of dielectric layer happens. Fig. 5 shows the voltage at gate oxide vs. time to dielectric breakdown for different thickness: for the same thickness, as Vox increases, tDB decreases; for a same value of Vox, the thinner layer can sustain for a longer time. Dielectric breakdown is quite damageable for MOSFET devices it will affect the switching performance of MOSFET and increase the energy wasted. In order to avoid it, dielectric layer in MOSFET must have a certain thickness.

Figure 5. Graph of voltage at gate oxide vs. time to dielectric breakdown for different thickness [5]
The problem of trade-off is obvious: in order to improve MOSFET’s switching frequency, which means having a good transfer performance, the thickness of dielectric layer should be decreased; however, if the layer is too thin, MOSFET can’t sustain a high gate voltage, which may lead to dielectric breakdown. Therefore, when designing a MOSFET, an engineer must make a compromise between high transfer frequency and high gate voltage sustainability.

3.2. Trade-off for Output Characteristics

For the output characteristic of enhancement MOSFET, the ideal situation is that the resistance should be infinitely small so that there won’t be little joule heating, which is the unintended waste of energy. To be presented in graph, the slope at linear region in Fig. 4 should be almost vertical. In order to decrease the resistance, let’s first analyze the formula below calculating resistance:

\[ R = \frac{L}{\rho A} \]

Where \( \rho \) can be considered as the resistivity of MOSFET as a whole, which is a constant not considering the effect of temperature; \( L \) is the length, which can be presented as the distance between drain and source; \( A \) is the cross section area, which can be presented as the width of the channel. Thus, there are two ways to reduce the resistance: increasing \( A \) or decreasing \( L \). However, when \( L \) decreases too much, short channel effect happens, which will lead to the problems like drain-induced barrier lowering (DIBL), surface scattering and so on. In this part, only DIBL and surface scattering will be detailedly discussed.

The first problem is DIBL. In the normal condition, there is a potential barrier to stop electrons flowing from source to drain, and gate voltage controls the height of the barrier to determine the drain current. However, when the source gets too close to the drain, the field of drain and source will cross each other to form a special depletion region called punch-through, and this will lower the barrier height, which means carriers can flow from source to drain with less energy supplied. Thus, there will be a stronger leakage current. Fig. 6 depicts the relationship between drain current ID and gate voltage VG for different channel lengths \( L \) at different drain voltage; for example, for \( L=1.5 \mu m \) and \( 3 \mu m \), as VG approaches to negative axis, ID is relatively higher than for \( L=1.5 \mu m \). That means MOSFET device is less likely to be at “off-state” when the channel length is short.

![Figure 6. The relationship between ID and VG for different channel lengths at VD=1.0V and 0.5V [6]](image_url)

More information can be obtained from the graph. Below is the equation of subthreshold swing:

\[ S = \frac{dV_g}{d \log I_D} \]
Subthreshold swing represents how MOSFET’s performance of the frequency to switch between on and off-state, and the smaller $S$ is, the faster the switching is and vise versa. According to Fig. 6, the inverse of slope for $L=1.5 \ \mu m$ is bigger than that for $L=3 \ \mu m$. Thus, the switching performance of MOSFET is worse when the channel length is small because there is no clear boundary for on and off-state.

The another problem of short-channel effect is surface scattering. When carriers flow in the channel, they are moving under the effect of drain-to-source electric field and gate electric field. Due to this effect, carriers continuous collide with the lattice structure of semiconductor, so they are moving in a Z-path just like Fig. 7 shows.

![Figure 7](image)

**Figure 7.** The moving path of an electron. (a) Random thermal motion; (b) Affected by electric field

When the channel is shortened, drain-to-source field will be strengthened. In order to effectively control the state of MOSFET, a stronger gate voltage is needed. Thus, the collision against the lattice gets fiercer and more frequent, which means the electron mobility $\mu$ decreases. According to the equation:

$$\sigma=n\mu q, \ \rho=1/\sigma$$

where $n$ is electron density, $q$ is the quantity of charges, $\mu$ decreases, $\sigma$ decreases, and $\rho$, the resistivity, increases. Thus, the current-voltage relationship is impacted, and the output characteristics of MOSFET actually can’t reach the people’s original expectation, meaning that the performance is not increasing proportionally as the channel length decreases.

According to the formula calculating the resistance, another way to decrease the resistance is to increase the width of the channel, but a new consideration occurs: when developing better devices, engineers not only need to pay attention to the performance of the devices, but also the cost. The increase in width will surely increase the total size of the transistor, and for the same size of an integrated circuit, there will be fewer components can be placed in it. Facing the trend that people’s electronic devices are getting smaller while have a better function, increasing the width is not a wise choice just in order to improve the current-voltage relationship but ignore the economic benefits.

Thus, the trade-off for output characteristics of enhancement MOSFET is that when people try to decrease the output performance, people need to consider the short-channel effect, which will bring the problems of DIBL, increasing subthreshold swing and surface scattering. And these problems will respectively strengthen the leakage current, make the boundary of on and off-state unclear, worsen transfer performance and inversely decrease the output performance. What’s more, increasing the channel width is not economic efficiency way though the trade-off problem can be relieved.

### 3.3. Method to Relieve the trade-off

Silicon, the first generation semiconductor, is the commonest semiconductor material right now. Silicon, a tetrels (+4), is often doped with elements of triels (+3) and pentad (+5) to create holes and electrons. However, compared to the third generation semiconductor, the first generation is not good enough though. According to Fig. 8, many aspects of silicon are weaker than GaN and SiC, which are two major types of third generation semiconductor materials. Both GaN and SiC generally have the
same performance energy gap, and electron velocity better than Si: higher energy gap represents stronger ability to tie valance electrons; higher electron velocity represents a better current-voltage relationship. Respectively, MOSFET will have a better switching ability and output characteristic. Based on their own properties, engineers can apply either GaN or SiC in different conditions. For example, when the transistors need to work under a high temperature, SiC is a better choice for its high thermal conductivity and melting point; when the transistors need to work under a high electric field, GaN is a better choice for its high breakdown voltage.

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Figure 8. Radar diagram comparing five properties for Si, SiC and GaN [8]

However, widely applying the third generation semiconductor materials is not practical, because the growth and manufacture of the raw materials is very hard, especially for SiC.

4. Discuss about the Improvement
Generally speaking, under the trend that transistors are made in a smaller scale, trade-off problems are inevitable by changing the structure of basic n-channel enhancement MOSFET, meaning that the change in a parameter will negatively affect another. In order to improve the transfer characteristics of MOSFET, the dielectric layer should be thinner; due to the reduce of thickness, the resistance of continuously high gate voltage is weakened, and dielectric breakdown will happen and damage the device.

The first method to decrease the resistance is to shorten the channel length, but as the length decreases to a certain point, short-channel effect occurs, which brings the problems of DIBL, higher subthreshold swing and surface scattering. These problems will respectively strengthen the leakage current, make the boundary of on and off-state unclear, worsen transfer performance and inversely decrease the output performance. Another method is to increase the channel width. Though this approach can relieve the trade-off, but the consideration of economic benefits will rule out this choice.

To solve the problem of trade-off, applying third generation semiconductor materials is a method from the aspect of material. GaN and SiC have a relatively prominent performance on high voltage operation, frequency switching and high temperature application. However, the lack of raw materials is a problem still unsolved.

The trade-off in transfer and output characteristics is inevitable. As the research of relieving the trade-off keeps on going, a more practical way to face this issue is to specialized design the transistors based on their different applications.

5. Conclusion
From the study of n-channel enhancement MOSFET, the author illustrates the working principles of MOSFET, trade-off problems and method to improve the performance. However, several shortages still exist during the research process: all the illustrations are based on theories and only focus on main
parameters that will significantly affect the performance of MOSFET when discussing the trade-off. Thus, some possible factors are ignored in the research, which means the study in the paper is should be brought into experimental condition to test whether other factors may affect MOSFET. In the later study, the main direction should base on observation, and quantitatively describe the phenomena. For example, when studying the relationship between the thickness of dielectric layer and breakdown voltage, control variate should be applied, recording how the time of breakdown varies with the gate voltage for a certain thickness. Generally speaking, the practice to demonstrate the points made in the paper is significant for the following research.

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