50 Ohm Transmission Lines with Extreme Wavelength Compression
Based on Superconducting Nanowires on High-Permittivity Substrates

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We demonstrate impedance-matched low-loss transmission lines with a signal wavelength more than 150 times smaller than the free space wavelength using superconducting nanowires on high permittivity substrates. A niobium nitride thin film is patterned in a coplanar waveguide (CPW) transmission line geometry on a bilayer substrate consisting of 100 nm of epitaxial strontium titanate on high-resitivity silicon. The use of strontium titanate on silicon enables wafer-scale fabrication and maximizes process compatibility. It also makes it possible to realize a 50 Ω characteristic impedance across a wide range of CPW widths, from the nanoscale to the macroscale. We fabricated and characterized an approximately 50 Ω CPW device with two half-wave stub resonators. Comparing the measured transmission coefficient to numerical simulations, we determine that the strontium titanate film has a dielectric constant of 1.1×10^9 and a loss tangent of not more than 0.009. To facilitate the design of distributed microwave devices based on this type of material system, we describe an analytical model of the CPW properties that gives good agreement with both measurements and simulations.

Cryogenic microwave circuitry has garnered increased interest in recent years, driven in part by the field of quantum computing based on superconducting circuits.1–3 It is also important for the development of large-format arrays of cryogenic particle detectors4 and high-speed classical computing using superconducting circuits.5 The size of distributed microwave components—such as filters, resonators, couplers, circulators, and travelling wave parametric amplifiers—is limited by the signal wavelength, which is ≈4 cm at 5 GHz in standard material systems. This large size makes on-chip integration difficult and is one of the major bottlenecks in scaling up cryogenic microwave systems.6–8

For low-loss transmission lines, the characteristic impedance is \( Z_0 = \sqrt{\frac{L}{C}} \) and the phase velocity is \( v_p = \frac{1}{\sqrt{LC}} \), where \( L \) is the inductance per unit length and \( C \) is the capacitance per unit length. The ratio of the signal wavelength on the transmission line to the free space wavelength is the same as the ratio of the phase velocity on the transmission line to the speed of light in free space. Standard transmission lines, such as an RG-58 coaxial cable or a 50 Ω microstrip on FR4 circuit board, have a signal wavelength that is approximately two thirds of the free space wavelength. The signal wavelength can be reduced while maintaining a matched impedance by proportionally increasing both \( L \) and \( C \). Previous work has developed slow-wave transmission lines using conventional materials and increasing \( L \) and \( C \) by manipulating the transmission line geometry.9–11 This approach has been successful in reducing the signal velocity and wavelength by up to an order of magnitude but not further.

Superconducting nanowires made from low carrier density materials can have a kinetic inductance that is two or more orders of magnitude larger than their magnetic inductance.12–14 One such material is niobium nitride (NbN), which has demonstrated inductances per unit length \( \sim 10^2 – 10^3 \) pH/μm in a 100 nm wide, ultra-thin nanowire.12,13 This compares to a magnetic inductance of \( \sim 1 \) pH/μm. The large kinetic inductance naturally leads to a large characteristic impedance, \( \sim 50 \) kΩ, when patterned in a transmission line geometry.15,16 Such large impedances can be useful for decoupling from the electromagnetic environment but create challenges for coupling to standard microwave circuitry, which is commonly designed around a 50 Ω impedance. Incorporating the nanowire in a high permittivity dielectric medium brings down the characteristic impedance and further shrinks the signal wavelength. High permittivity oxides such as hafnium dioxide (dielectric constant \( \varepsilon_r \approx 25 \)) and titanium dioxide (\( \varepsilon_r \approx 80 \)) offer significant enhancement over silicon dioxide (\( \varepsilon_r = 3.9 \)) but do not have a large enough permittivity to offset the extremely large kinetic inductance of a NbN nanowire in order to achieve a 50 Ω characteristic impedance.

Advances in materials science have allowed the synthesis of ceramic materials belonging to the class of perovskites with extremely high relative permittivities. One such material, strontium titanate (SrTiO3, abbreviated as STO), is a quantum paraelectric with an indirect bandgap of 3.25 eV.17 It has been shown to have a relative permittivity exceeding 10^4 in single crystal form at 4 K, a value that decreases upon the application of an external electric field.18 This permittivity is sufficient to achieve a 50 Ω characteristic impedance with a NbN nanowire. However, as the wire width increases, the kinetic inductance decreases, and the extreme permittivity of STO results in macroscale transmission lines with characteristic impedances well below 50 Ω.20

In order to achieve a 50 Ω characteristic impedance at both nanoscale and macroscale dimensions, we have utilized a thin layer of STO grown epitaxially on a bulk silicon (Si) wafer.21,22 At nanoscale dimensions, the STO dominates the effective permittivity, but as the transmission line width increases, the contribution of the STO to the effective permittivity decreases. The use of bulk Si also ensures the ability to fabricate on large-scale substrates, as single-crystal STO...
is generally not available in substrate sizes larger than two inches.\textsuperscript{23} Further, Si is a widely used substrate material, so its use increases process compatibility with other types of cryogenic and superconducting circuitry.

Previous work described CPW resonators made from the high-temperature superconductor $\text{YBa}_2\text{Cu}_3\text{O}_7\text{a}$ on substrates consisting of an STO film on bulk $\text{LaAlO}_3$.\textsuperscript{24,25} This work focused on utilizing the electric field-dependent polarizability of the STO to realize resonator tunability and the devices exhibited only modest compression of the signal wavelength by a factor of 2-3 compared to the free space value.

To demonstrate the potential for extreme wavelength compression using our material system, we fabricated the coplanar waveguide (CPW) double resonator device shown in figure 1. The device maintains a characteristic impedance of approximately 50 $\Omega$, with a CPW that transitions from a center conductor width of 400 $\mu$m and a gap width between the center conductor and the coplanar grounds of 360 $\mu$m at the edges of the chip – large enough to facilitate wirebonding – to a center conductor width of 5 $\mu$m and a gap width of 1.75 $\mu$m in the center of the chip. The transition maintains a constant fractional change in the center conductor width per unit length. In the center section, two half-wave stub resonators connect between the center conductor of the main CPW and ground. The resonators are in a CPW geometry with a center conductor width of 560 nm and a gap width of 120 nm. The length of the longer resonator is 300 $\mu$m and the length of the shorter resonator is 200 $\mu$m. An equivalent circuit model is shown in figure 1a.

The substrate consists of 100 nm of epitaxial (001) STO grown via molecular beam epitaxy (MBE) on a 370 $\mu$m thick high-resistivity (001) Si ($\rho > 1 \text{k}$ $\Omega$cm). The initiation of the heteroepitaxial growth of STO on Si is key to obtaining a crystalline STO film\textsuperscript{22} and involves a controlled sequence of steps that kinetically suppresses the formation of an amorphous oxide layer on Si\textsuperscript{21,22} and reduces the tendency for the STO film to form islands.\textsuperscript{26} Once a thin crystalline STO template was formed with in-plane epitaxial relationship STO [100] parallel to Si [110], the growth conditions were maintained at $\approx 700^\circ \text{C}$ substrate temperature and $\approx 5 \times 10^{-7}$ Torr oxygen background pressure to obtain a 260 molecular-layer thick (100 nm) STO film. Throughout the growth, reflection electron micrograph showing the connection of one resonator to the main CPW. The opposite end of the resonator connects to ground.

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The two half-wave stub resonators have lengths $l_1 = 300 \mu$m and $l_2 = 200 \mu$m. (b) Optical image of the full device chip mounted in a sample holder. The overall chip size is 10 mm x 4 mm. (c) Closeup of the center of the device chip showing the two resonators. (d) Scanning electron micrograph showing the connection of one resonator to the main CPW. The opposite end of the resonator connects to ground.

The transmission coefficient $|S_{21}|^2 = 10\log_{10}(P_{\text{out}}/P_{\text{in}})$ of this device measured at a bath temperature $T = 1.5$ K is shown in figure 2. A schematic of the experimental setup can be seen in the Supplementary Material. The signal power at the device is less than $-70 \text{dBm}$, ensuring that we do not excite nonlinear effects. The data are normalized by measuring a sample with the same CPW geometry but no resonators. The fundamental half-wave resonances occur at 2.80 GHz and 4.20 GHz, corresponding to a signal wavelength on the resonators that is 178 times smaller than the free space wavelength.

Also shown in figure 2 is a simulation of the device using the AXIEM solver in AWR Microwave Office with an appropriately small mesh size. The dielectric anisotropy of STO is ignored in the simulation, and the superconducting NbN is modeled as a complex sheet impedance with a real part of zero and the imaginary part set to $2\pi f L_{K, sq}$ with $f$ the simulation frequency and $L_{K, sq}$ the sheet kinetic inductance.\textsuperscript{15} $L_{K, sq}$ can
be determined from the normal-state sheet resistance $R_{sq}$ using

$$L_{K,sq} = \frac{R_{sq} h}{2\pi^2 \Delta \tanh \left( \frac{\Delta}{2\sqrt{\pi} \tau} \right)}$$  

(1)

where $h$ is Planck’s constant, $\Delta$ is the superconducting energy gap, and $k_B$ is Boltzmann’s constant.\textsuperscript{12} In the limit that the temperature $T$ is much smaller than the superconducting critical temperature $T_C$, $\Delta \approx 1.76k_BT_C$ and the previous equation simplifies to $L_{K,sq} = R_{sq} h / (3.52 \pi^2 k_B T_C)$. In order to measure $R_{sq}$ without possible error due to substrate conductivity, a NbN film was deposited on a thermally-oxidized Si chip at the same time as the deposition on the STO-Si chip. This sample has $R_{sq} = 187 \, \Omega$ per square at 20 K, corresponding to $L_{K,sq} = 21.5 \, \text{pH}$ per square in the low temperature ($T \ll T_C$) limit, which is the value used in the simulation.

The values of the STO dielectric constant and loss tangent are adjusted in the simulation to achieve the best agreement with the data. This leads to a dielectric constant of $1.1 \times 10^5$. The corresponding characteristic impedance of the resonator CPW is 66 $\Omega$, close to the target value of 50 $\Omega$. The CPW gap size could be reduced to bring the impedance closer to the target value. While the STO permittivity is lower than values reported for bulk single crystals, it is comparable to previously reported values for thin-film STO,\textsuperscript{28,29} likely because additional disorder in the thin film material reduces the polarizability. The loss tangent determined from the simulation was $\tan \delta = 0.009$. We note that all other materials in the simulation were assumed to be completely lossless, and hence this value represents an upper bound on the actual loss tangent of the STO. Both resonances have a quality factor $Q = 160$ which is likely limited by material losses.

The demonstrated loss tangent is sufficiently low for many types of microwave devices but can likely be improved. We believe that the losses may be dominated by finite resistivity of the STO arising from oxygen vacancies. In future work, we plan to investigate further optimization of the STO growth to minimize its conductivity and maximize its permittivity.

When performing electromagnetic device simulations, generally one wants to ensure that the simulation mesh is sufficiently small such that further reduction in the mesh size does not change the simulation results. For this material system, we found that satisfying this condition required a considerably smaller mesh size in the vicinity of the CPW gap than is needed for conventional materials. (Further details are provided in the Supplementary Material.) As a result of the fine mesh size, the simulation time and memory requirement become considerable; the simulation results shown in figure 2 took more than 24 hours.

Such a long simulation time poses challenges for iterative device design and optimization. In order to facilitate more rapid device design, we developed an analytical model for CPW transmission lines using this material system. This analytical model uses the established conformal mapping approach for CPW transmission lines made from conventional materials\textsuperscript{30,31} combined with a model based on BCS theory developed by Clem for the kinetic inductance per unit length of a superconducting CPW.\textsuperscript{32}

First the capacitance per unit length $C$ of the CPW geometry is calculated using a Schwarz-Christoffel conformal mapping. This process has been described previously\textsuperscript{30,31} and the details are in the Supplementary Material. While single-crystal STO is an anisotropic dielectric, with the largest low-temperature polarizability in the direction of the (110) crystal axis,\textsuperscript{39} this calculation ignores the anisotropy.

The total inductance per unit length $L_{\mathcal{M}}$ is the sum of the magnetic inductance per unit length $L_M$ and the kinetic inductance per unit length $L_K$. Considering only magnetic inductance, $v_p = c/\sqrt{\varepsilon_{eff}}$ where $c$ is the speed of light in free space and $\varepsilon_{eff}$ is the effective dielectric constant (calculated as described in the Supplementary Material), and hence $L_{\mathcal{M}}$ can be found from:

$$L_{\mathcal{M}} = \frac{\varepsilon_{eff}}{\varepsilon_0 c^2}$$

(2)

For a superconductor with thickness $d < 2\lambda_L$, where $\lambda_L$ is the London penetration depth, the distribution of the current across the width of the wire is no longer governed by $\lambda_L$, but rather by the Pearl length $\lambda_P = 2\lambda_L^2/d$. This is the case for our samples. When the center conductor width $2s \ll \lambda_P$, the current distribution in the center conductor is approximately uniform and the kinetic inductance per unit length $L_K$ is, to a good approximation, equal to the sheet kinetic inductance divided by $2s$. The sheet kinetic inductance $L_{K,sq}$ is found as described previously, with a value of 21.5 pH per square in the low temperature ($T \ll T_C$) limit. $\lambda_L$ can then be calculated from

$$L_{K,sq} = \frac{\mu_0 \lambda_L^2}{d}$$

(3)

where $\mu_0$ is the permeability of free space. This yields $\lambda_L = 507 \, \text{nm}$ and $\Lambda_P = 34.2 \, \mu$m.

A procedure for calculating $L_K$ for all center conductor widths was developed by Clem.\textsuperscript{32} In this approach, $L_K$ is
| Parameter                                | Value       |
|------------------------------------------|-------------|
| NbN thickness                            | 15 nm       |
| NbN normal state sheet resistance         | 187 Ω/sq    |
| NbN critical temperature                 | 12.0 K      |
| NbN sheet kinetic inductance (T ≪ T_C)   | 21.5 pH/sq  |
| NbN London penetration depth (T ≪ T_C)   | 507 nm      |
| NbN Pearl length (T ≪ T_C)              | 34.2 μm     |
| STO relative permittivity                | 1.1 × 10^3  |
| STO thickness                            | 100 nm      |
| Si relative permittivity                 | 11.7        |
| Si thickness                             | 370 μm      |

The parameter $p$ is calculated as described in Clem$^{32}$ but has the following useful approximations:

$$ p \approx 0.63 / \sqrt{\Lambda_P / s} \quad \text{for} \quad \Lambda_P \gg s \quad (6) $$

$$ p \approx 1 - 0.67 \Lambda_P / s \quad \text{for} \quad \Lambda_P \ll s \quad (7) $$

This approach to calculating $\mathcal{L}_K$ gives results that are very close to $\mathcal{L}_K = L_{K, sq} / (2s)$ when $\Lambda_P \gg s$.

Using this analytical approach with the sample parameters summarized in Table 1, we calculate the value of the gap width $g$ that gives a characteristic impedance $Z_0 = 50 \, \Omega$ as a function of the center conductor width $2s$. The results of this calculation are shown in Figure 3. For comparison, we also show the results for the case with an STO substrate of the same total thickness as well as the case with an Si substrate of the same total thickness. We see that the STO-Si bilayer substrate allows us to achieve a 50 Ω impedance over a much wider range of center conductor widths than either a STO or Si substrate. We found agreement to better than 5% between the numerical simulations and the analytical calculations provided that a sufficiently fine mesh size was used in the vicinity of the CPW gap. Because of the long times required for accurate simulations, this analytical model can be very useful for initial device design.

FIG. 3. (a) Analytical calculation of the CPW gap width $g$ required to achieve a characteristic impedance of 50 Ω as a function of the center conductor width $2s$. Results are shown for the bilayer substrate consisting of 100 nm STO (dielectric constant $= 1.1 \times 10^3$) on top of 370 μm Si (dielectric constant = 11.7). Also shown for comparison are the results for a substrate of the same total thickness consisting entirely of STO or Si. (b) Corresponding ratio of the signal wavelength $\lambda$ to the free space wavelength $\lambda_{fs}$, which is also the ratio of the phase velocity $v_p$ to the speed of light in free space $c$.

This extreme wavelength compression facilitates the on-chip integration of many types of distributed microwave devices that would be prohibitively large using conventional material systems, expanding the possibilities for scaling up cryogenic microwave systems.

See the supplementary material for additional details on the STO growth, the experimental setup for device characterization, numerical simulations, and the analytical model.

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Supplementary Material for “50 Ohm Transmission Lines with Extreme Wavelength Compression Based on Superconducting Nanowires on High-Permittivity Substrates”

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I. MBE GROWTH OF STRONTIUM TITANATE ON SILICON

The SrTiO$_3$ (STO) film was grown by molecular-beam epitaxy (MBE) on an (001) oriented extremely low-doped silicon (Si) substrate (3” diameter, n-type (phosphorous), resistivity > 1 kΩcm). The Si substrate was first cleaned under an ultraviolet ozone cleaner for ≈ 20 minutes before loading into the MBE chamber. The initiation of the heteroepitaxial growth of STO on Si is key to obtaining crystalline STO.$^1$ This involves a controlled sequence of steps that kinetically suppresses the formation of an amorphous oxide layer on Si$^{1,2}$ and reduces the tendency for the film to form islands.$^3$ The first step in this process is to remove the native oxide layer on the surface of the Si. This was accomplished in situ using a strontium-assisted thermal deoxidation process;$^4$ depositing ≈ 2 monolayers of strontium metal at a substrate temperature of ≈ 600°C and subsequently heating the substrate to ≈ 800°C, at which temperature the SiO$_2$ layer desorbs, with strontium acting as a catalyst. The oxide removal was observed by the transformation of the amorphous reflection high-energy electron diffraction (RHEED) pattern to one showing characteristic features of a crystalline (001) Si surface (see Fig. S1a). Next, the substrate temperature was reduced to ≈ 300°C for depositing a seed layer of STO.

During each deposition step discussed below, the substrate was continuously rotated. The strontium and titanium fluxes were precisely matched (to within 0.3%) at ≈ $1 \times 10^{13}$ atoms/cm$^2$s. This was achieved by first using a quartz crystal microbalance to obtain source fluxes accurate to within 5% followed by a calibration film grown just prior to the actual film where feedback provided by RHEED patterns was used to fine tune the strontium and titanium fluxes. Specifically, the characteristic surface reconstructions in RHEED due to excess strontium or excess titanium were monitored and the strontium and titanium fluxes were adjusted to avoid these reconstructions.$^1$

With these established parameters, oxygen, strontium and titanium were codeposited to form a 2.5 molecular layer thick STO seed layer at ≈ 300°C. The oxygen flux was carefully adjusted using a piezoelectrically controlled leak valve to give a molecular oxygen flow of approximately $2 \times 10^{16}$ molecules/s during the seed layer deposition which lasted ≈ 2.5 minutes. In this as-grown state, the thin STO seed layer is epitaxial, although the crystal quality was improved by heating in vacuum (less than $2 \times 10^{-9}$ Torr) to ≈ 580°C for ≈ 10 minutes (see Fig. S1b). At this point, further growth of STO is achieved by introducing oxygen to the chamber and codepositing strontium and titanium in an oxygen background pressure of ≈ $2 \times 10^{-7}$ Torr. These starting conditions of ≈ 580°C substrate temperature and ≈ $2 \times 10^{-7}$ Torr oxygen background pressure were
FIG. S1. RHEED images obtained during growth of the STO film on Si. (a) Si [110] azimuth showing surface after native oxide is removed. (b) Surface of 2.5 molecular layer thick STO seed layer along STO [100] azimuth following vacuum anneal to \( \approx 580^\circ \)C. Note that the STO film grows 45° rotated with respect to the Si lattice such that Si [110] azimuth is parallel to STO [100] azimuth. (c) RHEED image along STO [100] azimuth and (d) along STO [110] azimuth at the end of the growth.

RHEED patterns at the end of the growth along the STO [100] azimuth and the [110] azimuth are shown in Fig. S1c and Fig. S1d, respectively, and provide a qualitative measure of the crystalline quality of the STO film.

To minimize oxygen vacancies in the STO film which could lead to increased dielectric losses, the film was cooled down to below 150°C under an oxygen background pressure of \( \approx 5 \times 10^{-7} \) Torr before removing the sample from the MBE chamber. Post-growth x-ray diffraction measurements were carried out to probe the structural quality of the STO film. Rocking curve measurements in \( \omega \) of the out-of-plane STO 002 reflection showed a full-width at half-maximum of \( \Delta \omega = 0.17^\circ \), providing a quantitative measure of crystal quality of the STO film.
II. MEASUREMENT SETUP

A schematic of the experimental setup for the measurement of the double-resonator device is shown in figure S2. The device under test (DUT) is inside the vacuum can of a helium-4 cryostat with a 1K pot. The device temperature can be adjusted between 1.5 K and approximately 20 K. Two semi-rigid coaxial lines (Micro-Coax UT-085-SS) connect between the device and the room temperature electronics. At room temperature, one line connects through the RF port of a bias tee and a -66 dB attenuator to port 1 of a vector network analyzer (VNA). The other line connects through a DC block and a chain of two amplifiers (Minicircuits ZX60-V63+, 0.05 to 6 GHz bandwidth, approximately 20 dB gain per amplifier) to port 2 of the VNA. The VNA outputs a signal power of 0 dBm from port 1 and measures the incoming power in port 2 (i.e. the transmission coefficient). Including line attenuation, the total power reaching the DUT is below -70 dBm. Applying a current between the DC port of the bias tee and ground passes a current through both resonators in parallel.

![FIG. S2. Schematic of the experimental setup for double-resonator device measurement.](image)

Figure S3 shows the measured transmission coefficient of the double-resonator device at $T = 1.5$ K and zero bias current along with the measured transmission coefficient for a device with the same through CPW but no resonators, which is used as a normalization. Increasing the temperature or bias current shifts the resonances to lower frequency, consistent with the temperature- and current-dependence of kinetic inductance, which has been discussed in previous publications.$^{5,6}$
FIG. S3. Measured transmission coefficient of double-resonator device and normalization sample at $T = 1.5$ K and zero bias current.

III. ANALYTICAL CPW MODEL BASED ON CONFORMAL MAPPING

The capacitance per unit length of the CPW geometry can be calculated using a Schwarz-Christoffel conformal mapping. Here we follow the example of Gevorgian et al.\textsuperscript{7} This technique assumes that the dielectric interfaces are perfect magnetic walls and the total capacitance can be found using the partial capacitance approximation. It also assumes that the metal layer can be treated as zero thickness. This has been shown to yield results that are accurate to within 3\% for multilayer substrates.\textsuperscript{8} For the conductor-backed two-layer substrate shown in figure S4, the total capacitance per unit length $C$ is given by

$$C = 4\varepsilon_0 \varepsilon_{\text{eff}} \frac{K(k)}{K(k')}$$

where $\varepsilon_0$ is the permittivity of free space, $K$ is a complete elliptic integral of the first kind, $k = s/(s+g)$, and $k' = \sqrt{1-k^2}$. The effective dielectric constant $\varepsilon_{\text{eff}}$ is given by

$$\varepsilon_{\text{eff}} = 1 + q_1(\varepsilon_1 - 1) + q_2(\varepsilon_2 - \varepsilon_1)$$

where, for our device, $\varepsilon_1 = 11.7$ is the dielectric constant of Si and $\varepsilon_2$ is the dielectric constant of STO, determined experimentally to be $1.1 \times 10^3$.

The factors $q_i$ in equation S2 are given by

$$q_1 = \frac{1}{2} \frac{K(k_1)}{K'(k_1')} \frac{K(k')}{K(k)}$$

$$q_2 = \frac{1}{2} \frac{K(k_2)}{K'(k_2')} \frac{K(k')}{K(k)}$$
FIG. S4. Schematic of the coplanar waveguide (CPW) geometry (not to scale). Below the CPW is a two-layer conductor-backed substrate and above the CPW is free space.

with

\[ k_1 = \frac{\sinh \frac{\pi s}{2h_1}}{\sinh \frac{\pi (s+g)}{2h_1}} \]  
\[ k_2 = \frac{\tanh \frac{\pi s}{2h_2}}{\tanh \frac{\pi (s+g)}{2h_2}} \]  
\[ k_1' = \sqrt{1-k_1^2} \]  
\[ k_2' = \sqrt{1-k_2^2} \]  

The use of the \( \tanh \) function in equation S6 reflects the fact that the bottom dielectric layer is backed by a conductor; if it were not backed by a conductor, \( \tanh \) would be replaced with \( \sinh \) as in equation S5. We note that, when \( s \) becomes much larger than the STO thickness \( h_2 \), the parameter \( k_2 \) approaches zero and the parameter \( k_2' \) approaches 1. Most computational software packages default to storing numerical values using machine precision, which can cause \( k_2 \) to become rounded to zero and \( k_2' \) to become rounded to 1, neglecting the contribution of the STO layer. To prevent this rounding issue and ensure accurate results, it is important that the values of \( k_2 \) and \( k_2' \) are stored with sufficient precision such that the difference between their actual values and 0 and 1, respectively, is preserved in the calculation.

The total inductance per unit length \( \mathcal{L} \) is the sum of the magnetic inductance per unit length \( \mathcal{L}_M \) and the kinetic inductance per unit length \( \mathcal{L}_K \). Considering only magnetic inductance, \( v_P = c/\sqrt{\varepsilon_{\text{eff}}} \) where \( c \) is the speed of light in free space, and hence \( L_M \) can be found from:

\[ \mathcal{L}_M = \frac{\varepsilon_{\text{eff}}}{\varepsilon c^2} \]  

(S9)
The kinetic inductance per unit length $L_K$ is then calculated as described in the main text, resulting in a total inductance per unit length $L = L_K + L_M$. Assuming losses are sufficiently small, the characteristic impedance of the CPW is then $Z_0 = \sqrt{\frac{\mu}{\epsilon}}$ and the phase velocity is $v_p = \frac{1}{\sqrt{LC}}$.

IV. EFFECT OF MESH SIZE ON DEVICE SIMULATIONS

Device simulations were performed using the AXIEM solver in AWR Microwave Office version 15. This solver applies a mesh to the surface of all the conductors in the device geometry. In general, one wants the mesh size to be fine enough such that reducing the mesh size does not change the simulation results. The mesh size is not directly specified by the user but is determined by the software based on a combination of the specified grid size, the conductor geometry, the maximum simulation frequency, and the settings for the mesh density and decimation of each conductor. As the mesh size decreases, the simulation time increases, creating a trade-off between accuracy and time. For our coplanar waveguide (CPW) geometry, we found that this trade-off could be optimized by dividing the grounds into two regions. One region, within a distance of approximately $15g$ from the CPW gap, with $g$ the gap width, was set to a mesh density of high and the remaining ground region was set to a mesh density of low. The CPW center conductor was also set to a mesh density of high.

As an example of the effect of the mesh size on the simulation results, we show in figure S5 the effect of changing the grid size on the simulated characteristic impedance for a straight section of CPW with a center conductor width of 560 nm and a gap width of 40 nm. The overall CPW length is 120 µm and the total width, including the grounds, is 46 µm. Differential ports were used on each end of the CPW. The imaginary part of the niobium nitride sheet impedance is set to $2\pi f L_{K, sq}$, where $f$ is the simulation frequency and $L_{K, sq} = 21.5$ pH per square is the sheet kinetic inductance. The real part of the niobium nitride sheet impedance is set to zero. The substrate consists of 100 nm thick strontium titanate (STO) with a dielectric constant of $1.1 \times 10^3$ and a loss tangent of 0.009 on top of 370 µm thick silicon (Si) with a dielectric constant of 11.7 and a loss tangent of zero. With these same material parameters, the analytical model yields a characteristic impedance of 49.8 Ω. Also shown is a plot of the simulation time for each grid size as well as an image showing one portion of the CPW with the mesh associated with the finest grid size (20 nm). The simulations were performed on a dual-CPU workstation with 24 processor cores and 96 GB of RAM, although the software is limited to using a maximum of 8 processor cores. We see that
FIG. S5. (a) Simulated characteristic impedance versus grid size for a straight CPW with a 560 nm center conductor width and a 40 nm gap width. The dashed line shows the characteristic impedance of 49.8 Ω determined from the analytical model. Decreasing the grid size reduces the mesh size, although the two sizes are not equal. (b) Corresponding simulation times for each grid size. (c) Illustration of the device meshing at the smallest grid size (20 nm).

the simulation result approaches the analytical result for the finest grid size, but at the expense of a significant increase in simulation time. For larger device geometries, the necessary mesh size may result in a prohibitively long simulation time or a prohibitively large memory requirement, making the analytical model especially useful in such cases.

V. COMPARISON TO CIRCUIT BOARD RESONATOR

To illustrate the significant reduction in device footprint enabled by this material platform, we also designed, fabricated, and measured a similar double resonator device using a copper-clad FR4 circuit board. The FR4 has a nominal dielectric constant of 4.47. The circuit board device was designed in a CPW geometry with a uniform 1.0 mm center conductor width and a 0.12 mm gap width, which yields a characteristic impedance of approximately 50 Ω. The device was patterned
FIG. S6. Comparison of double resonator devices. (a) Layout of device made from niobium nitride on bilayer STO-Si substrate. (b) Transmission coefficient of niobium nitride device measured at 1.5 K. (c) Image of device made from a copper-plated FR4 circuit board. (d) Transmission coefficient of circuit board device measured at room temperature.

with photolithography using an overhead transparency as a mask and etched using ammonium persulfate. The two half-wave stub resonators have the same CPW dimensions and lengths of 32 mm and 21 mm, designed to have resonances at approximately 2.8 GHz and 4.3 GHz, respectively. To avoid unwanted slotline modes, wirebonds were used to create air bridges between the grounds on either side of each resonator where the resonator connects to the main CPW. An image of the circuit board device is shown in figure S6, alongside the layout of the niobium nitride device for comparison. Also shown is the measured transmission coefficient \(10\log_{10}(P_{out}/P_{in})\) of both devices. The data for the circuit board device were taken at room temperature while the data for the superconducting device were taken at 1.5 K. The total footprint of the circuit board device is approximately 10,000 times larger than the superconducting device.
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