Conversion Principle and Control Method of Synchro Signal

Wenfa Lv

Jiangsu Automation Research Institute, Shenghu Road NO.18, Lianyungang City, Jiangsu Province, 222006, China
Email: lwf_2001@126.com

Abstract. The synchro is a kind of micromotor used for angle measurement. It can output analog signals containing angle information, which is widely used in the fire control system. In order to facilitate the processing, it is necessary to digitize these analog signals. In this paper, 8255A is used as the main control chip, and high-speed, high-precision digital to analog and analog to digital converters are used for real-time analog acquisition or mathematical conversion of selsyn signals to realize real-time data communication between fire control equipment and external equipment, and selsyn signals are used for real-time data communication. The technology has the characteristics of flexible control, simple circuit, strong real-time, high reliability, and it has been widely used in the fire control system of naval gun, and achieved good results.

1. Introduction
In the fire control system, the fire control equipment needs to collect the navigation equipment's attitude information such as speed and heading, and the position of the artillery. These equipments are generally arranged in different cabins on different decks, with a long distance from each other and a complicated electromagnetic environment in the cabin. In order to ensure that these signals can be transmitted reliably, these signals are generally self-rectifier signals of AC excitation voltage. In order to facilitate computer processing, these AC high-frequency analog signals need to be digitally converted. A control principle and implementation method for the artillery fire control equipment to receive the self-rectifier analog signals of the external device is proposed. An 8255A microcontroller, combined with an SDC analog-to-digital converter and a DSC digital-to-analog converter are used in this method. It is widely used in ship fire control systems with its low cost, strong real-time performance, high reliability, and easy maintenance.

2. Conversion Principle
2.1. SDC Converter and Conversion Principle
The conversion principle is that a three-phase voltage into a two-phase voltage $V_1$, $V_2$ by applying the three-phase voltage into a miniature transformer. $D_1$, $D_2$, $D_3$ of the auto-rectifier signals are input, the shaft angle is $\theta$.

$V_1$ is given by

$$V_1 = KE\sin\theta$$  \hspace{1cm} (1)

$V_2$ is given by

$$V_2 = KE\cos\theta$$  \hspace{1cm} (2)
Where $K$ is the transformation ratio and $E$ is the voltage amplitude. $V_1$ and $V_2$ are added to the high-speed digital sine and cosine multiplier and multiplied by $\cos \varphi$ and $\sin \varphi$ to obtain $V_1'$ and $V_2'$.

\begin{align*}
V_1 &= V_1 \cos \varphi = KE \sin \theta \cos \varphi \\
V_2 &= V_2 \sin \varphi = KE \sin \varphi \cos \theta
\end{align*}

(3) (4)

Where $\varphi$ is the count value of the reversible calculator. Subtract and amplify $V_1'$ and $V_2'$, $\Delta V$ is obtained by

\begin{equation}
\Delta V = V_1' - V_2' = KEK' \sin(\theta - \varphi)
\end{equation}

(5)

Where $K'$ is the amplification factor of error amplifier.

After error processing and voltage-controlled oscillator correction, $\Delta V$ makes the reversible counter count toward the value of $\theta$ and reaches the high-speed sine and cosine multipliers again, then multiplies with $V_1$ and $V_2$ to obtain $V_1'$ and $V_2'$. When $V_1'$ and $V_2'$ are equal, $\Delta V = 0$. At this time, the value $\varphi$ of the reversible counter is equal to the digital quantity corresponding to the angle $\theta$, and the analog-to-digital conversion is realized. The conversion principle is shown in Figure 1.

**Figure 1.** The Principle Diagram of SDC Converter

### 3. DSC Converter and Conversion Principle

The DSC converter consists of a reference signal generator, a high four-bit sine and cosine function generator, a low ten digits function generator, a sine and cosine synthesizer, a power amplifier, and a SCOTT transformer. The roles of the reference signal generator are converting ~115V AC voltage to the low voltage that the semiconductor can work normally and generating the sine or cosine function values of the four special angles in the first quadrant.

The upper 4 digits sine and cosine function generator receives the reference signal and generates a sine function and a cosine function at intervals of 22.5° under the control of the upper four digits of the full input digital angle.

The core of the low 10-bit function generator circuit is to design a circuit parameter $K$. $K$ is a function of the digital angle of the digital-to-synchronizer converter. The lower ten-digit function generator receives the upper four sine and cosine functions and the feedback value of the full-angle sine and cosine function to generate the two functions $K(\sin \theta + \sin \alpha)$ and $K(\cos \theta + \cos \alpha)$.

The sine and cosine synthesizer combines the functions generated by the upper 4 bits and the lower 10 bits, and the synthesis relationship is given by

\begin{align*}
\sin \theta &= \sin \alpha + K(\cos \alpha + \cos \theta) \\
\cos \theta &= \cos \alpha + K(\sin \alpha + \sin \theta)
\end{align*}

(6) (7)

Then, $\sin \theta$ and $\cos \theta$ are given by

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\[ \sin \theta = \frac{1 - K^2}{1 + K^2} \sin \alpha + \frac{2K}{1 + K^2} \cos \alpha \]  
(8)

\[ \cos \theta = \frac{1 - K^2}{1 + K^2} \cos \alpha - \frac{2K}{1 + K^2} \sin \alpha \]  
(9)

Where

\[ \theta = \frac{3 \times 6 \times 0}{2^{1+4}} \sum_{i=1}^{14} A_i \alpha^{14-i} \]  
(10)

\[ \alpha = \frac{3 \times 6 \times 0}{2^{1+4}} \sum_{i=1}^{14} A_i \alpha^{14-i} \]  
(11)

\( K \) is a function of \( \beta \), and the relationship satisfied is

\[ \sin \beta = \frac{2K}{1 + K^2} \cos \beta = \frac{1 - K^2}{1 + K^2} \cos = \frac{1 - K^2}{1 + K^2} \]  
(12)

\[ \beta = \frac{3 \times 6 \times 0}{2^{14}} \sum_{i=1}^{14} A_i \alpha^{14-i} = \theta - \alpha \]  
(13)

The power amplifier is essentially a current amplifier that only amplifies the output current of the operational amplifier, which basically does not affect the conversion accuracy of the entire digital-synchronous machine converter.

The SCOTT transformer realizes the conversion from two phases to three phases, and the phase difference between the output three-phase voltages is 120°.

\[ VS1S3 = 90 \sin \theta \sin (\omega t) (V_{rms}) \]  
(14)

\[ VS3S2 = 90 \sin (\theta+120^\circ) \sin (\omega t) (V_{rms}) \]  
(15)

\[ VS2S1 = 90 \sin (\theta+240^\circ) \sin (\omega t) (V_{rms}) \]  
(16)

The conversion principle is shown in Figure 2.

![Diagram of DSC converter](image)

**Figure 2.** The working principle diagram of DSC converter

### 4. The Control Method

#### 4.1. The Implementation Method of Input Control

The SDC converter outputs 14-bit parallel natural binary code digital quantity. The inhibit signal (/INH) only controls the transmission of the output digital from the reversible counter to the latch. In this way, when the inhibit signal is used, the internal loop operation of the converter is not affected.
When data transmission is needed, the computer can send a logic low level to the /INH terminal, which prevents the latch from being refreshed. When the /INH terminal is set to a low level and the data is stable after a delay of 600ns, the data can be read. After the data is recorded, /INH is released to high level to refresh the latch data.

The internal logic of the SDC converter and the timing of the "/INH" signal are shown in Figure 3, respectively.

The computer system sends control signals through the PC port of the 8255A chip. Among them, PC4 and PC6 are the enable signals of the two 16-bit decoders, which control the decoder to enable or disable decoding respectively. PC0 to PC3 are address translation signals. Select one of the 32 SDC analog-to-digital converters, PC6 is forbidden / allow conversion signal / INH, allow module conversion or prohibit module conversion. When reading the data converted by the module, first make the module forbid conversion and delay for a period time (generally no more than 3us), so that the data read is stable and reliable. Therefore, only the selected module among the 32 conversion modules will start to work. The computer system reads the digital quantity converted through the PA port and PB port of the 8255A chip. By sending different address signals and selecting different conversion modules, digital signals converted by different conversion modules are processed. The block diagram is shown in Figure 4.

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**Figure 3.** The Internal Logic Block Diagram of SDC Converter

The system sends control signals through the PC port of the 8255A chip. Among them, PC4 and PC6 are the enable signals of the two 16-bit decoders, which control the decoder to enable or disable decoding respectively. PC0 to PC3 are address translation signals. Select one of the 32 SDC analog-to-digital converters, PC6 is forbidden / allow conversion signal / INH, allow module conversion or prohibit module conversion. When reading the data converted by the module, first make the module forbid conversion and delay for a period time (generally no more than 3us), so that the data read is stable and reliable. Therefore, only the selected module among the 32 conversion modules will start to work. The computer system reads the digital quantity converted through the PA port and PB port of the 8255A chip. By sending different address signals and selecting different conversion modules, digital signals converted by different conversion modules are processed. The block diagram is shown in Figure 4.

**Figure 4.** The Block Diagram of Input Control

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4.2. The Implementation Method of Output Control

DSC Digital-Secondary Angle Conversion Module is a converter that converts a 14-bit natural binary digital angle to a digital angle / self-resolver / resolver signal output. The 14-bit natural binary digital angle uses LS / CMOS digital latch. The input and output AC signals are isolated by input and output transformers, so that the converter does not need to add an external digital latch, and does not need an
external reference transformer and output transformer. The internal logic of the module is shown in Figure 5.

![Figure 5. The Internal Logic Block Diagram of DSC Module](image)

The computer system first sends the digital quantity to the local bus through the PA and PB ports of the 8255A chip, and then sends the control signal to the DSC conversion module through the PC port. Among them, PC0 to PC3 are address translation signals. One of the 32 conversion modules is selected. PC4 and PC6 are the enable signals of two 16-bit decoders, which control the decoder to enable or disable decoding respectively, so only the selected one of the 32 conversion modules will start to work. The converted analog signal is provided to other devices. By sending different control signals, different conversion modules are selected to realize the conversion from digital signals to analog signals. The schematic block diagram is shown in Figure 6.

![Figure 6. The Block Diagram of Output Control](image)

4.3. The Self-Loop Control of Input and Output

In order to detect whether the data converted by the conversion module of the output channel and the input channel is correct, the computer system of the fire control equipment can add a set of relays between the input channel and the output channel. The computer system will pass the output shooting metadata through the DSC converter. Form the signal of the auto-rectifier, and switch the signal through the relay as the stand signal of the artillery to the SDC converter. The SDC converter converts this signal into a digital signal and sends it to the computer system, so that the computer system can check the correctness of the SDC and DSC channels when the artillery is turn off or is not available and solve problems such as online fault diagnosis and troubleshooting.

PC7 is a self-test control line. When PC7 is 0, the input unit and output unit are in a self-test state, the input unit and output unit form a closed loop, and the output data is returned to the input to verify the correctness of the input and output. The control principle is shown in Figure 7.
5. Control Program

Because the input and output conversion modules are 14-bit, the 8255 PA and PB ports are used as the local bus for a total of 16 bits. When sending output data, the upper 8 bits of the 16-bit data are sent to the PB port and the lower 8 bits are sent to the PA port (the lowest two bits B1B0 are invalid), a total of 14 bits of valid data are sent to the DSC conversion module for conversion. When receiving data, the 8-bit data read by the PB port as the upper 8 bits of the converted data, and the upper 6 bits of the 8-bit data read by the PA port is the lower 6 bits of the converted data (the lower 2 bits B1B0 Invalid). 14-bit converted valid data are formed.

When receiving data, first clear PC5 (/INH) to 0 to disable the conversion of the SDC converter, and then send the decoder enable signal PC6 / PC4 (When the module number is less than 16, first set PC6 to 1, and then set PC4 to 0, otherwise set PC4 to 1, and then set PC6 to 0), and then send the address decoding signal PC3 ~ PC0, so that one of the 32 SDC analog-to-digital converters performs data conversion. During the operation of a certain module, PC6 and PC4 can not be 0 or 1 at any time by bit operation, delay for a short period of time (usually not less than 3us), and then read the data of the PA and PB ports. Combining the data read, removing the lower 2 bits to form 14-bit valid data, setting PC5 to 1 to allow the module to continue conversion, and then sending the next address decoding signal to read the next module conversion data until read the data converted by all modules.

When transmitting data, write the upper 8 bits and lower 6 bits of the transmitted data to the PA and PB ports respectively, and then send the address decoding signals PC3 to PC0 to enable one of the 32 DSC digital-to-analog conversion modules to perform data conversion, Then send the next address decoding signal, send the data to another module, make it perform data conversion, until all data conversion is complete. The control program code:

```
Void Txd_da (int ch, int ot_da) /* Send data */
{
    unsigned char vl,vh;
    vl =(unsigned char)(ot_da&0x00ff) ;
    vh =(unsigned char)(ot_da>>8) ;
    outportb(8255_ba,vl);
    outportb(8255_ba+1,vh);
    outportb(8255_ba+2,ch);
    delay(100);
    outportb(8255_ba+2,0xff);
}
unsigned int Rxd_da(int ch) /* Receive data */
{
    unsigned int in_da;
    unsigned int vl,vh;
```
outportb(8255_ba+7, 0x0a); /* Set PC5 to let the module forbid convert */
outportb(8255_ba+6, (ch|0x40));
delay(100);
vl=inportb(8255_ba+4);
vh=inportb(8255_ba+5);
in_da=((vh<<8) +vl);
outportb(8255_ba+7, 0x0b);
return(in_da);

6. Conclusion
In this paper, a control principle and implementation method of using an 8255A parallel interface chip as the main control chip, combined with SDC analog-to-digital conversion and DSC digital-to-analog converter is proposed to realize the artillery fire control equipment receiving analog signals from the external device self-rectifier. This method has the characteristics of low cost, strong real-time performance, high reliability, and convenient maintenance. It is widely used in fire control equipment of ship fire control system and achieves good results.

7. References
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