Analysis of Current Aggregation in Gate-Control Dual Direction Silicon Controlled Rectifier

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Abstract The current aggregation mechanism created by the gate structure is proposed for electrostatic discharging (ESD). Through device simulation, the size-expanded gate structure in gate-control dual-direction silicon controlled rectifier (GC-DDSCR) is found to aggregate the surface parasitic current path and the main SCR current path. The SCR current path is consequently twisted and extended to increase the holding voltage (Vth). Two GC-DDSCRs are fabricated in a 0.5μm CMOS technology and tested by transmission line pulse (TLP). The Vth increases from 13.84V to 16.44V as the gate size expands from 2.5μm to 4.5μm. The mechanism of current aggregation is verified.

key words: Silicon Controlled Rectifier, ElectroStatic Discharge, CMOS technology

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

With the miniaturization of semiconductor feature size and the advancement of integrated circuits, catastrophic ElectroStatic Discharge (ESD) events can seriously deteriorate chip reliability [1-6]. Conventional diode structures and Gate-Grounded NMOS (GGNMOS) structures always require a large silicon area to achieve a good ESD robustness [7-10]. By contrast, silicon controlled rectifiers (SCRs) have been widely used due to their highest robustness per unit area [11-20]. However, the unique positive feedback loop of the SCR structure makes it have deep snapback characteristics, which cause a low holding voltage. The low holding voltage may lead to the latch-up and the miss-trigger, which are intolerable to integrated circuits.

Increasing the holding voltage of SCR structures through structural modification has been a hot topic in ESD research [21-24] and there are generally three methods. Firstly, the holding voltage can be increased by directly lengthening the dimension between the anode and the cathode of the device, that is, lengthening the ESD current path. Wang et al. [25] designed a lateral double diffused MOSFET silicon controlled rectifier (LDMOS-SCR) for the ESD protection of single-photon detectors. By extending the distance between the anode and the cathode, the holding voltage can be raised from 3.43V to 7.72V due to the increased on-resistance. However, this method requires additional silicon area. Secondly, the holding voltage can be increased by adding parasitic ESD paths to suppress the SCR positive feedback. Bi et al. [26] designed a dual-directional silicon controlled rectifier (DDSCR) with embedded PNP current path in a 0.35μm bipolar complementary-metal-oxide-semiconductor double-diffused-metal-oxide-semiconductor (BCD) process. The embedded PNP structure can form an extra discharging path to shunt the SCR current path and hinder the positive feedback. Hence, the DDSCR-PNP has a higher holding voltage than the traditional DDSCR structure. Thirdly, the holding voltage can be increased by promoting the carrier recombination in the base region of the bipolar junction transistors (BJTs) [27]. The emission efficiency of parasitic BJTs is reduced to increase the holding voltage. However, this method sometimes needs extra process layers. It is of great significance to find a more area-efficient and cost-saving way to increase the holding voltage of the SCR structure.

In recent research, gate structures are widely used to improve the ESD performance of SCR structures [28-30]. It gives us inspiration that we can use the gate structure to create a novel discharging mechanism to increase the holding voltage of the traditional SCR structure. In this paper, a novel electrostatic discharging mechanism of the gate structure is proposed. Two gate-control dual-direction silicon controlled rectifiers (GC-DDSCRs) are fabricated in a 0.5μm CMOS technology and investigated by Silvaco simulations and TLP test. The current aggregation mechanism of GC-DDSCR is experimentally demonstrated to increase the holding voltage.

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2. Device structure and theoretical analysis

Fig. 1 (a) shows the cross-section of the GC-DDSCR and Fig. 1 (b) shows the bidirectional equivalent circuit of the GC-DDSCR.

As shown in Fig. 1 (a), the N+ heavily-doped regions and the P+ heavily-doped regions are arranged at intervals on the device surface. Two symmetrical P-Well regions are surrounded by the Deep N-Well (DN-Well), forming the intrinsic SCR path from anode P+, anode P-Well, DN-Well, cathode P-Well to cathode N+. When the integrated circuit is working normally, the device is in the off-state and will not respond to normal electrical signals in the circuit. However, when an abnormal and dangerous ESD event strikes the anode of the device, the anode P+, and the anode P-Well are raised to the same high potential. The cathode P+ and the cathode P-Well are pulled down to the same low potential. The potential of the floating DN-Well is between the anode P-Well and the cathode P-Well. The voltage difference between the floating DN-Well and the cathode P-Well can reach the reverse breakdown voltage of the parasitic PN junction. The avalanche breakdown occurs in the reverse-biased PN junction. A large number of electron-hole pairs are generated due to carrier multiplication. When the structure is initially triggered, the intrinsic SCR path is not opened. The ESD current is first discharged through the parasitic BJT paths on the device surface. Since the device is initially opened at this time, the gate electric field has little effect on the current path, no matter how large its range is.

When the ESD current in T1 gradually increases, a voltage drop can be generated on the parasitic resistance of the cathode P-Well, turning on the NPN path (T3) consisting of DN-Well, cathode P-Well and cathode N+. The opening of the T3 will increase the voltage drop on \( R_{DNW} \) and further turn on the T1 to a greater extent. In this case, the two coupled transistors enter the positive feedback state. The SCR path is formed to release a large amount of ESD current. When the SCR path is fully formed, the PNPN path becomes the main discharging path and the parasitic BJT paths become the secondary path. At this time, the electric field generated by the gate structure can affect the internal current paths. From the perspective of the equivalent circuit in Fig. 1 (b), the gate electric field does not introduce any additional parasitic paths. The gate structures play an auxiliary enhancement role in the equivalent circuit, bending and lengthening the current path in the equivalent circuit through the vertical electric field.

However, when the gate size is small, the gate structure only covers a small part of the device layout in the top view. The area of the gate electric field is so small that its effect on the internal carriers is limited, even if its intensity is big enough. There will be many parasitic current paths on the surface of the device. And the SCR current will be evenly distributed inside the device. As the gate size increases, the gate structure covers a relatively big portion of the device layout in the top view. At this time, the gate electric field is powerful and wide enough to affect adequate carriers inside the device. The vertical downward electric field at the anode can pull holes downward and pull up free electrons. Macroscopically, the vertical downward electric field can push the surface parasitic current paths to move down and merge into the SCR path, resulting in the current aggregation mechanism. The vertical upward electric field at the cathode can push free electrons downward and pull up holes. Macroscopically, the vertical upward electric field can pull the deep SCR path to the surface, promoting it to be released from the cathode N+. In this way, the SCR discharging path is equivalently twisted and extended. The extended SCR path means a larger on-resistance (\( R_{ON} \) ) of the device structure. According to the formula \( V_{Clamp}=\frac{I_{ESD}}{R_{ON}} \), the clamping voltage of the device will increase accordingly, resulting in a higher holding voltage at the holding point.

3. Two-dimensional device simulation

The gate size of GC-DDSCR1 is 2.5μm and the gate size of GC-DDSCR2 is 4.5μm. The two-dimensional DC simulations of GC-DDSCRs are carried out using Silvaco TCAD software. Fig. 2 (a) and Fig. 2 (b) show the impact ionization of GC-DDSCR1 and GC-DDSCR2 when they are triggered. The DC scanning simulation point in Fig. 2 corresponds to the trigger point in the real TLP curve. It shows that the triggering surfaces of the two devices are both in the reverse-biased PN junction formed by DN-Well and cathode P-Well. The maximum ionization rates of the two devices are nearly equal (23.2 and 23.5 respectively). It indicates that two devices have the same triggering characteristics. Fig. 3 (a) and Fig. 3
(b) show the simulated total current density of GC-DDSCR\textsubscript{1} and GC-DDSCR\textsubscript{2} when they are initially turned on. When the devices are initially turned on, the ESD current is both discharged through the parasitic PNP path consisting of anode P\textsuperscript{+}, anode P-Well, DN-Well, cathode P-Well, and cathode P\textsuperscript{+}. The discharging ability of the two devices is relatively weak. At this time, the PNP current path is not controlled by the gate electric field. There are obvious current distributions under both the anode gate structure and the cathode gate structure. The current aggregation mechanism cannot be observed.

Fig. 4 (a) and Fig. 4 (b) show the simulated electric field in GC-DDSCR\textsubscript{1} and GC-DDSCR\textsubscript{2} when they are fully turned on. The DC scanning simulation point in Fig. 4 corresponds to the test point that is behind the holding point in the real TLP curve. At that point, the device structure has entered into the linear region. The SCR current path is fully turned on, which can fully reflect the influence of gate structure on ESD current paths. There are obvious electric field distributions in the anode gate oxide and the cathode gate oxide. When the gate size is 2.5\textmu m, the range and the intensity of the electric field are limited. The electric field intensity under the anode gate structure of GC-DDSCR\textsubscript{1} is 8.95E+04 V/cm. The electric field intensity under the cathode gate structure of GC-DDSCR\textsubscript{1} is 5.96E+04 V/cm. When the gate size is 4.5\textmu m, the electric field intensity under the anode gate structure of GC-DDSCR\textsubscript{2} is 3.47E+05 V/cm. The electric field intensity under the cathode gate structure of GC-DDSCR\textsubscript{2} is 1.16E+05 V/cm. At this point, the range and the intensity of the electric field in GC-DDSCR\textsubscript{2} are big enough to influence the ESD current paths.

Fig. 5 (a) and Fig. 5 (b) show the simulated total current density of GC-DDSCR\textsubscript{1} and GC-DDSCR\textsubscript{2} when they are fully turned on. The SCR current path of two devices both consists of anode P\textsuperscript{+}, anode P-Well, intermediate-potential DN-Well, cathode P-Well, and cathode N\textsuperscript{+}. However, it can be seen that the current distribution in the two device structures differs from each other. When the gate size is 2.5\textmu m, the current aggregation mechanism is weak due to the limited gate electric field. Total current density is evenly distributed in GC-DDSCR\textsubscript{1}, as shown in Fig. 5 (a). It can be seen that there is a dense current distribution at the anode N\textsuperscript{+} of GC-DDSCR\textsubscript{1}. There are clear parasitic current paths on the device surface. The parasitic current path is mainly a BJT path composed of anode N\textsuperscript{+}, anode P-Well, DN-Well, cathode P-Well, and cathode N\textsuperscript{+}. When gate size increases to 4.5\textmu m, the current aggregation is augmented due to the expanded range of the electric field and the increased intensity of the electric field. In GC-DDSCR\textsubscript{2} of Fig. 5 (b), the current density in the anode N\textsuperscript{+} is significantly reduced compared with GC-DDSCR\textsubscript{1}. The gate structure shorted with anode pushes surface parasitic current paths deep into the device and makes them aggregate with the main SCR path. There is no pronounced current distribution below the anode gate structure.
The gate structure shorted with cathode pulls up SCR current path to the device surface, promoting it to be released from the cathode N+ and making the whole current path display a ‘W’. In this case, the SCR current distance from anode to cathode equivalently increases without consuming additional silicon area or process masks. It leads to a larger $R_{\text{ON}}$. According to the basic Ohm’s law $V_{\text{ESD}}=I_{\text{ESD}}R_{\text{ON}}$, the increase in $R_{\text{ON}}$ will directly increase the $V_{\text{ESD}}$ when the same $I_{\text{ESD}}$ is discharged. Therefore, the holding voltage of the device at the holding point will become larger. The current aggregation mechanism can effectively increase the holding voltage of the device and suppress the latch-up effect. Fig. 6 (a) and Fig. 6 (b) show the simulated lattice temperature of GC-DDSCR$_1$ and GC-DDSCR$_2$ when they are fully turned on. In GC-DDSCR$_1$ of Fig. 6 (a), the hot spot is located at the anode N+ on the device surface. It indicates that there are many parasitic current paths distributed on the device surface, resulting in thermal power dissipation. In GC-DDSCR$_2$ of Fig. 6 (b), the hot spot is located at the inner center of the device. It proves from another perspective that the gate structure promotes the aggregation of the parasitic current paths and the deep SCR current path. So far, the physical principle of the current aggregation mechanism has been revealed.

### 4. TLP test results and discussion

Two GC-DDSCRs are fabricated in a 0.5μm CMOS technology, as shown in Fig. 7 (a). Partial key dimensions of two GC-DDSCRs are listed in Table I. In this work, the TLP test system as shown in Fig. 7 (b) is utilized to measure the ESD performance of devices. The measurement is performed under light-free conditions and the room temperature is 15 degrees Celsius. The rising edge and pulse width of the TLP pulse are set to 10ns and 100ns. Each time the TLP test system sends out a pulse, the measuring equipment tests response waveforms of voltage and current in the time domain. The average values of device voltage and device current within 70%–90% of the entire measurement period are taken to form one coordinate point on the TLP curve.

Fig. 8 shows the TLP test results of two GC-DDSCRs. Table II lists key TLP parameters of two GC-DDSCRs. Trigger voltages ($V_{\text{t1}}$) of GC-DDSCR$_1$ and GC-DDSCR$_2$ are 19.59V and 21.30V, which are almost identical. Trigger currents ($I_{\text{t1}}$) are 0.006A and 0.008A respectively. Due to the same triggering surface, the triggering characteristics of the two devices are basically the same. Holding voltages ($V_{\text{h}}$) of GC-DDSCR$_1$ and GC-DDSCR$_2$ are 13.84V and 16.44V, respectively. The holding voltage significantly increases by 2.60V as gate size expands from 2.5μm to 4.5μm. This is consistent with the theoretical analysis and the simulations. It verifies that the current aggregation mechanism extends the SCR current path, thereby increasing the holding voltage. By using the current aggregation mechanism created by the large-sized gate structure, the holding voltage can be efficiently increased and the latch-up immunity of the device can be improved.

The secondary failure current ($I_{\text{t2}}$) of GC-DDSCR$_1$ is 12.16A. Based on the formula $V_{\text{HBM}}=I_{\text{t2}} \times R_{\text{HIB}}$, the human body model (HBM) level of the ESD device can be calculated. $R_{\text{HIB}}$ is the equivalent impedance of the human body, which is normally 1.5kΩ. The HBM level of GC-DDSCR$_1$ reaches 18.24kV. However, when the gate size increases to 4.5μm, the $I_{\text{t2}}$ is reduced to 5.32A. That is because the current aggregation mechanism of GC-DDSCR$_2$ produces a larger holding voltage, which introduces extra thermal power consumption according to the formula $P_{\text{Device}}=I_{\text{ESD}} \times V_{\text{ESD}}$. The additional thermal power consumption will increase the overall temperature of the device structure and reduce its robustness. In this case, the HBM level of GC-DDSCR$_2$ is 7.98kV. It is consistent with the simulation results as shown in Fig. 6. It can be seen from Fig. 6 that the overall temperature of GC-DDSCR$_2$ is higher than that of GC-DDSCR$_1$ when they are fully turned on.
5. Conclusion

In this paper, a novel current aggregation electrostatic discharging mechanism is proposed based on the GC-DDSCR structure. Two-dimensional TCAD simulation is performed on the Silvaco platform. From the simulation results, the powerful gate electric field is found to generate current aggregation mechanism in GC-DDSCR. The strong gate electric field can aggregate the ESD current paths in the device and twist the main SCR current path. Two GC-DDSCRs with different gate sizes are manufactured in a 0.5μm CMOS technology and measured by the TLP test. The experimental results verify that the expanded gate structure can directly increase the holding voltage. In summary, the current aggregation mechanism is fully analyzed and can provide an idea for the design of the ESD devices.

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