ABSTRACT

Securing deep neural networks (DNNs) is a problem of significant interest since an ML model incorporates high-quality intellectual property, features of data sets painstakingly collated by mechanical turks, and novel methods of training on large cluster computers. Sadly, attacks to extract model parameters are on the rise, and thus designers are being forced to create architectures for securing such models. State-of-the-art proposals in this field take the deterministic memory access patterns of such networks into cognizance (albeit partially), group a set of memory blocks into a tile, and maintain state at the level of tiles (to reduce storage space). For providing integrity guarantees (tamper avoidance), they don’t propose any significant optimizations, and still maintain block-level state.

We observe that it is possible to exploit the deterministic memory access patterns of DNNs even further, and maintain state information for only the current tile and current layer, which may comprise a large number of tiles. This reduces the storage space, reduces the number of memory accesses, increases performance, and simplifies the design without sacrificing any security guarantees. The key techniques in our proposed accelerator architecture, Seculator, are to encode memory access patterns to create a small HW-based tile version number generator for a given layer, and to store layer-level MACs. We completely eliminate the need for having a MAC cache and a tile version number store (as used in related work). We show that using intelligently-designed mathematical operations, these structures are not required. By reducing such overheads, we show a speedup of 16% over the closest competing work.

1. INTRODUCTION

The AI hardware (Neural Processing Unit (NPU)) market was valued at 8 billion USD in 2020 and is expected to grow to 84 billion USD by 2028 [1] (CAGR of 34.15%). Hardware-based AI chips are expected to play a major role in telecommunications [8], mobile vision [34], edge computing [7], augmented/virtual reality [2], health care [17], and autonomous driving [41]. Similar to codes for general-purpose processors, ML models incorporate a lot of high-value intellectual property (IP) that takes a lot of time and effort to collate and develop. For example, even for a mid-size AI project just collecting the raw data using mechanical turks takes upwards of $100K USD [29]; the know-how for the model and training methodology can be worth millions of dollars, and finally it may take many weeks to finally train the model using large cluster computers. Along with these conventional arguments, many a time we don’t realize that even getting access to the training data can be quite challenging with numerous legal hurdles. Therefore, protecting an ML model is of paramount importance, which sadly also makes it an attractive target for hackers.

There are three broad approaches for protecting models as shown in Figure 1. All of them rely on secure CPUs as the baseline technology. To secure CPUs, we rely on Trusted Execution Environments (TEEs) such as Intel SGX [5], AMD SEV [18], and ARM Trustzone [27]. In all these TEEs, the CPU is assumed to be secure; it is within the TCB (Trusted Computing Base). The main contribution of the most elaborate scheme, Intel SGX, is in protecting the off-chip memory and providing confidentiality, integrity, and freshness. The key insight is ensuring that every time a block is written to main memory, it is encrypted with a different key. Since, storing a key for every memory block is too expensive, a more efficient mechanism is used based on AES counter-mode encryption. Every page is associated with a major counter, and every block uses a minor counter (a combination of both guides the encryption/decryption). The counters themselves need to be protected; this is achieved using a Merkle tree, where the root of the tree is guaranteed to be in the TCB. Let us refer to this version of SGX as SGX-Client. Because of the Merkle tree and associated overheads of maintaining counters, the maximum size of the protected memory region is limited to 128-256 MB (same problem with ARM TrustZone). Most ML models and datasets as of today are much larger. As a result, SGX-Client is not the best choice for them.

Keeping in mind these issues, Intel recently discontinued support for SGX-Client in its 11th and 12th generation processors. It replaced it with another version of SGX (referred to as SGX-Server) that simply encrypts memory and foregoes the integrity and freshness guarantees [30] (on the lines of AMD SEV). It can provide up to 512 GB of encrypted memory. We should bear in mind that SGX-Server is far weaker than SGX-Client in terms of the security guarantees that are provided namely integrity and freshness.

ML architecture designers have traditionally opted to use versions of SGX-Client to secure their systems (refer to Figure 1). Several early approaches either proposed optimizations to SGX-Client [5, 30] to reduce its overhead or partition an ML algorithm into a secure portion and unsecure por-
tion that ran on fast hardware such as GPUs [35]. However, these approaches have been superseded by a newer family of approaches that leverage the stable data communication patterns of ML workloads to design bespoke NoCs. Two custom accelerators stand out in this space: TNPU [21] and GuardNN [15]. Their basic ideas are similar: group a set of contiguous memory blocks into tiles and provide freshness guarantees at the level of a tile. Both use a dedicated software module running on the host CPU for managing version numbers (VNs); they are used to encrypt data as well as ensure its freshness. The major difference is that TNPU stores the VNs in an on-chip cache and GuardNN relies on a CPU program to generate all the VNs. The program needs to store all the VNs in use in secure memory, and securely communicate them to the accelerator (a difficult problem in itself). Both still perform integrity checking at the level of individual memory blocks (typically 64 bytes).

Our scheme, Seculator, improves upon these ideas and proposes a natural extension, where we perform freshness and integrity checks at the layer level. Given that no data is stored and no checking is done at the block-level (like previous schemes), there is an associated performance gain (15.6%). Additionally, there is no need to run a VN-generation module on the host CPU using a TEE. To realize this, we thoroughly characterize the memory access patterns of different kinds of ML accelerators, efficiently encode them, and pass the encoding to a small hardware circuit that automatically generates all VNs at runtime (without external intervention). This eliminates the need for storing and managing VNs in on-chip caches or main memory regions. Furthermore, we leverage the insight that the only consumer for the output(s) of a layer are a few layers that it is connected to – random access of output data is not required because these consumers layers access the data in a structured fashion. Hence, computing and storing MACs at the layer-level is good enough as long as the next layer accesses all the data (in any order), which is often the case.

To summarize, the main contributions in this paper are as follows: ① Characterization of traffic in CNNs and popular data pre/post processing algorithms, ② A method to succinctly encode the traffic pattern, ③ A method to generate VNs on the fly using such patterns, ④ A technique to perform integrity checking at the level of layers, and ⑤ A detailed experimental analysis of Seculator that shows a 16% speedup over the nearest competing work. ⑥ Given that the overheads are low, we additionally assess the benefits of interspersing the execution with the running of a dummy network (for the purpose of adding noise) or widening each layer. This helps reduce the possibility of model extraction attacks by utilizing timing or address side channels substantially.

The paper is organized as follows. Section 2 presents the background of TEEs and basic convolution operations in neural networks. Section 3 presents the threat model and the security guarantees provided by Seculator. We characterize the workloads in Section 4, present an analytical model for automatic version number generation in Section 5, and present the architecture of Seculator in Section 6. Finally, Section 7 reports the experimental results, Section 8 presents the related work and we conclude in Section 9.

![Figure 1: A timeline depicting a pragmatic shift from outsourcing execution from an unsecure compute-rich platform to designing an optimized and secure custom TEE for accelerating ML workloads.](image-url)
Integrity and Authenticity Verification using Message Authentication Codes (MACs): MACs are encrypted hashes, that are used to ensure that an adversary does not alter the data stored in an untrusted location. A unique MAC is generated for each data block and the corresponding counter value. When a data block is fetched from main memory, its MAC is also fetched and verified. As the data encryption takes into account the block address, an attacker cannot swap the \((data, MAC)\) pair with another pair. Sadly, these security guarantees come with significant overheads, and thus the size of protected memory is limited to 256 MB.

2.1.2 SGX-Server (11th and 12th Gen Intel CPUs)

Intel recently launched a scalable and efficient TEE [30] for Intel 3rd Gen scalable servers with an additional feature, Total Memory Encryption (TME), to overcome the size limitations of SGX-Client. This feature provides a secure memory size of 512 GB. Sadly, Intel compromised hardware-based integrity and replay protection in order to securely encrypt the entire memory (as mentioned in their documentation [21,30]). SGX-Server uses AES-XTS for performing total memory encryption, which does not rely on per-block counters. With the elimination of counters and the Merkle tree, the need for data caching and tree traversal are also eliminated, thus reducing the associated overheads.

2.2 Convolution

A convolution operation is the heart of a convolutional neural network (CNN) and many other modern ML algorithms such as LSTMs, RNNs, and GANs. The single-image version has a basic 6-loop structure. We iterate through the input and output feature maps \((ifmap and ofmap, resp.)\), and compute the convolutions. For the ease of explanation, we assume that they have the same size (both are referred to as an \( fmap \)) and are 2D matrices (each element is a pixel).

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Listing 1: A basic convolution operation

The loop order in Listing 1 can be written as \( k > c > h > w > r > s \), where the operator \( > \) shows the nesting order. Due to the restricted memory capacity of on-chip buffers, we often group pixels into \( tile \). In this case, an example notation for a tiled execution where the feature maps \((channels)\) are tiled \((rows and columns grouped)\) will be of the form, \( k > c > h > w > r > s > x > b > h > w \); the subscript \( t \) indicates the tile number, and the iterator without a subscript retains its previous meaning (pointing to a single element). Figure 2 shows a generic example, where \( k, c, h, \) and \( w \) are tiled. We will follow a consistent terminology for all iterators, \( e.g., C \) is the number of \( ifmaps \) (input channels), \( C_T \) is the size of a channel tile, \( c_T \) is the iterator for a channel tile, and \( c \) is the iterator of a channel (see Table 1). Note that unless specified otherwise, the term \( tile \) will refer to a group of pixels.
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Figure 2: Graphical representation of a tiled convolution operation. The \( ifmaps, ofmaps, input and output channels \) are tiled.
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2.3 TNPU and GuardNN

We shall compare Seculator with two state-of-the-art proposals: GuardNN [15] and TNPU [21]. A brief description follows (see Section 8 for more details).

In GuardNN, every tile is associated with a version number \((VN)\), which is incremented on every memory write. The VN’s are managed by the scheduler that runs on the host CPU, which has access to a TEE. MACs are generated and maintained per memory block. A variant of GuardNN advocates for a larger block size \((512 B)\); however, that unnecessarily constrains the subsequent layer to read data in that order, which we found to be impractical for modern CNNs where dataflow patterns are different for each layer. TNPU on the other hand, maintains VNs in a Tensor Table that is stored in the host CPU’s secure memory. It is protected by an integrity tree. MACs are maintained per block, and are stored in an on-chip MAC cache. Most architectures in this space including these and Seculator do not use the regular on-chip caches and instead read/write directly to main memory.

3. SYSTEM DESIGN AND THREAT MODEL

We use the same high-level system design and threat model as previous works [15,21].
actions of the NPU, or the NPU could completely take over after the CPU has sent it a few initialization instructions. Our design is unaffected by this choice. Insofar as the NPU is concerned, it needs to securely run an ML model, layer by layer. We only focus on inferencing in this paper (like [21]).

The package comprising the CPU, NPU, and caches is within the Trusted Computing Base (TCB). A hacker can however target the main memory and the CPU-memory bus (used by the NPU as well). A hacker in this case would include the OS, hypervisor, malicious program, or even a person who has physical access to the main memory or memory bus. She can try to read the data (eavesdropping), tamper with the data (integrity attack), replace the contents of memory addresses with old data (replay attack), masquerade as a different entity (authentication attack), read the memory address sequence from the memory bus and try to figure out the model parameters (model extraction attack (MEA)).

Our base version of Seculator protects against all types of aforementioned attacks other than MEA attacks. We shall show in Section 7.5 that it is possible to easily augment our architecture using ideas from Li et al. [23] to also provide security against MEA attacks with a modest overhead. This version will also protect against address-based side-channel attacks. However, we don’t protect against power and EM side-channel based attacks. Finally, like all prior work, we do not consider networks that have value-based pruning.

4. CHARACTERIZATION OF DNN WORKLOADS IN A SECURE ENVIRONMENT

| Parameter       | Value          | Parameter       | Value          |
|-----------------|----------------|-----------------|----------------|
| PE array        | 32 x 32        | Counter cache   | 4 KB           |
| Global buffer   | 240 KB         | (secure NPU)    |                |
| Frequency       | 2.75 GHz       | MAC Cache       | 8 KB           |
| Dual-channel DRAM| DDR 4, 100 cyc (lat) | Write mode | Write back 64 B |

Table 1: NPU configuration, list of benchmarks, and the terminology used in the paper

4.1 Setup and Benchmarks

We characterize the behavior of popular benchmarks on an in-house cycle accurate CNN simulator that has been rigorously validated with ARM SCALE-Sim [31] and native hardware. It relies on a systolic array architecture to perform convolutions. We relied on the Timeloop [26] tool to provide the most optimal dataflow pattern. We show the configuration of the simulated system in Table 1. We simulated a vanilla, unsecure accelerator version as the baseline. The workloads comprise popular neural network benchmarks as shown in Table 1. Layers represents the total number of layers and Parameters represents the total number of tunable model parameters present in a specific benchmark. Additionally, we simulate a secure configuration that is quite similar to SGX-Client (see Section 2.1.1). The MACs and counter values are saved in the 8 KB MAC cache and 4 KB counter cache, respectively (values taken from [21]). All the models fit within the DRAM. Finally, note that performance is defined as the reciprocal of the simulated execution time (appropriately normalized).

4.1.1 Performance Insights

Figure 4 shows the performance results. Secure and TNPU have an 8 KB MAC cache. The secure configuration is 32% slower than the baseline, TNPU is 22% slower, and GuardNN is 44 % slower. Clearly, reducing the size of secure memory helps, and having a MAC cache also helps (as opposed to not having one like in GuardNN).

Figure 5 shows the miss rates for the MAC cache and counter cache, respectively.

Table 1: List of benchmarks (similar to [15,35]) and the terminology used in the paper.
### Table 2: Pattern table for convolution: various possibilities for scheduling the input tiles for input reuse and output reuse. $\alpha_K = \frac{K}{k_T}$; $\alpha_C = \frac{C}{c_T}$; $\alpha_{HW} = \frac{H \times W}{H_T \times W_T}$; $\text{RP} \rightarrow \text{Read pattern}$, $\text{WP} \rightarrow \text{Write pattern}$, $-$ refers to empty or not applicable

| Expression | Possible patterns |
|------------|------------------|
| $[1^{\alpha_k}, 2^{\alpha_k} ... \alpha_C^{\alpha_C}]^{\alpha_{HW}}$ | P1: Multi-step |
| $1^{\alpha_k} ... 2^{\alpha_k} ... \alpha_C^{\alpha_C}$ | P4: Sawtooth $(\alpha_K = 1)$ |
| $1^{\alpha_k}$ | P2: Step |
| $1^{\alpha_k}$ | P3: Linear$(\alpha_K \alpha_{HW} = 1)$ |

| Tiling style | Loop order | Input reuse | RD/WR pattern | Output reuse | Loop order | RD/WR pattern |
|--------------|------------|-------------|---------------|--------------|------------|---------------|
| Partial channel [4, 39] | $h_T > w_T > c$ | $k_T$ | $\text{WP}: [1^{\alpha_k}, 2^{\alpha_k} ... \alpha_C^{\alpha_C}]^{\alpha_{HW}}$ | | $h_T > w_T > k_T$ | $\text{RP}: 1^{\alpha_k}$ |
| Partial-multi-channel [39] | $h_T > w_T$ | $c$ | $k_T$ | | $h_T > w_T > k_T$ | $\text{RP}: 1^{\alpha_k}$ |
| Partial channel [28] | $c$ | $h_T$ | $w_T > k_T$ | | $h_T > w_T$ | $\text{RP}: 1^{\alpha_k}$ |
| Partial-multi-channel [39] | $c$ | $h_T$ | $w_T > k_T$ | | $h_T > w_T > k_T$ | $\text{RP}: 1^{\alpha_k}$ |
| Channel-wise [4] | $c$ | $h_T$ | $w_T > k_T$ | | $k_T$ | $\text{RP}: 1^{\alpha_k}$ |
| Full-channel [37] | $h_T > w_T > k_T$ | $\text{WP}: 1^{\alpha_k}$ | $\text{RP}: -$ | | $h_T > w_T > k_T$ | $\text{RP}: 1^{\alpha_k}$ |

In convolution, there are three possible types of data reuse: input reuse, weight reuse, and output reuse [28]. In all three cases, the output feature maps are updated, hence, let us focus on them.

#### 5.1 Convolution Layer

The primary goal of this scheme is to minimize the number of times an ifmap is accessed. The stages are as follows: (1) The tiled ifmaps are loaded into the GB. (2) The ifmaps are entirely reused in order to compute the corresponding ofmaps. (3) The partially computed ofmaps are stored back to memory. They are retrieved for the next ifmap and updated. Let us look at various patterns generated by scheduling ifmap tiles in different ways [28]. The following text heavily refers to Table 2 that compiles the most popular data flow patterns.

- **Rows 1 and 2 ▶ Partial (multi) channel loading:** Consider the first entry’s loop order with $K_T = 1$: $h_T > w_T > c > k$. We

5
do not show the rest of the iterators because it is assumed that once the data corresponding to a set of input/output tiles is fetched (as per the loop order), the rest of the processing happens within the NPU. We are not concerned with internal aspects of the NPU, we only care about the accesses to main memory. Now, as per this loop order, we consider an input tile, and then we compute the results for a set of ofmaps. We cycle through the ofmaps, and then move to the next ifmap.

Assume, $C = 2$, $K = 3$, and the GB can hold only one ofmap tile at any point of time. Each ifmap tile is reused by three filters ($K = 3$) to generate 3 distinct ofmap tiles. Each ofmap tile is associated with a VN (incremented by 1 when the ifmap is evicted from the GB). After the ifmap tile has been fully utilized, all ofmap tiles will have the same VN, as they are in the same computational stage (only one ifmap channel is processed). This leads to a VN write pattern $1^K$ as seen by the Write-observer. If we group a set of $K_{\text{f}}$ output tiles and consider them together, then this expression will change to $1^K_{a_k}$ where $a_k = K/K_{\text{f}}$.

Thereafter, the next ifmap tile from the next channel is read from memory. These ofmap tiles are again sequentially updated – we increment the VN of all the tiles from 1 to 2 (as they get evicted from the GB) leading to the following pattern: $1^2 2^k$. The operation will repeat until all input channels are processed. After processing all the channels of an ifmap tile, we schedule the input tile movement along the $w$-axis and the aforementioned process will repeat until all $\alpha_{\text{ifmap}} = \frac{H_{\text{ifmap}}}{H_{\text{T}}} \times \frac{W_{\text{ifmap}}}{W_{\text{T}}}$ ifmap tiles are processed. The VN updates will generate a simple deterministic pattern: Multi-step or Sawtooth. Additionally, the ofmap tile’s read pattern will be mostly identical to the write pattern. The only difference is that we will not read the final ofmap. The final ofmap will be read in the subsequent layer. In Row 2, we consider a group of $C$ channels together. The expressions are similar.

Rows 3 and 4 ebooks Movement along the Width/Height: Consider the loop order, $c > H_T > W_T > K_{\text{f}}$. Basically, we first cover an ifmap and then move to the next. This means $\alpha_{\text{ifmap}} = \frac{(H \times W)/(H_{\text{T}} \times W_{\text{T}})}{H_{\text{T}}} \times \frac{W_{\text{T}}}{K_{\text{f}}}$. Each ifmap tile will thus partially generate all the $K$ ofmaps (in groups of $K_{\text{f}}$). All these groups of ofmap tiles will have the same VN. Then we shall move to the next ifmap to update all the partially computed output tiles. We increment the VNs accordingly. The process will repeat until all the ofmap tiles are fully computed.

Rows 5 ebooks Channel-wise:
In this scheme, a single input channel (channel-wise) or a group of input channels (multi-channel) of size $H \times W$ constitute an input tile. Due to the stationary nature of the input tile, it will be reused $\alpha_{\text{ifmap}} = K/K_{\text{f}}$ times to generate all of the $\alpha$ ofmap tiles of size $H \times W$ leading to the pattern ($1^\alpha_{\text{ifmap}}$). These partially computed output tiles are updated when a new ifmap tile is fetched from memory. The operation will be repeated until all input channels are processed.

Rows 6 ebooks Full Channel:
This is a simple scheme in which all the channels required for the generation of an output tile are available. The VN for a tile will be updated only once due to the availability of all the channels, leading to the pattern $1^{\alpha_{\text{ifmap}} \alpha_{\text{ifmap}}}$.

### 5.1.2 Output Reuse (OR)

An output tile is completely computed in this scheme before being sent to memory. Initially, (1) successive channels of the same ifmap are loaded into the GB. (2) The partial ofmap tile is reused until it is fully computed. The write patterns are very simple because there is no write-read-update cycle. They are of the form $1^\alpha$. There is no read pattern because partially computed ofmap data is never read back.

Rows 1 and 2 ebooks Partial(multi) channel loading: Prior to storing an output tile in memory, it must be completely computed. The VN of an output tile of size $H_T \times W_T$ remains the same as it does not leave the GB. Then we proceed to the next output tile. The pattern generated above will repeat for $(H \times W)/(H_T \times W_T)$ times for each of the $(H \times W)/(H_T \times W_T)$ tiles.

| Tiling style | Loop order | Pattern |
|--------------|------------|---------|
| Filter-wise movement | $c_T > k_T$ | $\alpha_{\text{ofmap}}$, $\alpha_{\text{ifmap}}$; $\alpha_{\text{ifmap}} = \frac{H_T}{H} \times \frac{W_T}{W}$; $\alpha_{\text{ifmap}} = K/K_{\text{f}}$; RP: $1^{\alpha_{\text{ifmap}}}$, $2^{\alpha_{\text{ifmap}}}$ ... $(\alpha_{\text{ifmap}}-1)\alpha_{\text{ifmap}}$ |
| Channel-wise movement | $k_T > c$ | $1^{\alpha_{\text{ofmap}}}$; RP: $1^{\alpha_{\text{ofmap}}}$; RP: $-\text{Patterns}$: $P_2$, $P_3$ |
| Full -filter [37] | $k_T$ | $1^{\alpha_{\text{ofmap}}}$; RP: $-\text{Patterns}$: $P_5$ |

Table 3: Pattern table for convolution: Different methods of scheduling weight tiles for weight reuse.

### 5.1.3 Weight Reuse

The steps involved in this process are as follows. Consider the first row. (1) The tiled weight matrix (4D tensor) of size $C_T \times K_{\text{f}} \times R \times S$ is loaded in memory. (2) $C_T$ ifmaps of dimension $H \times W$ are loaded in the global buffer [37]. (3) The weights are reused to compute $K_{\text{f}}$ ofmaps of dimension $H \times W$. The pattern generation methodology is similar to the previous schemes. The generated patterns for all the rows are shown in Table 3.

### 5.2 Other Kinds of Layers

Let us now look at some other kinds of layers in DNNs. Most layers are extensions of simple convolution such as the Fully Connected layer.

**Generative-Adversarial Networks (GANs):** GANs [10] are composed of a discriminator and a generator network. To generate fake images, the generator uses deconvolution (transposed/dilated), whereas the discriminator uses convolution to discern between fake and real images. The pattern generation approaches for general convolution presented in Table 2 will work for any kind of convolution including deconvolution. To convert the input to the needed form, we may need to do some pre-processing.

**Matrix Multiplication:** We also analyze the data access pattern in the case of matrix multiplications as it is extensively used in several ML workloads including transformers [38].
We classify the different tiling scenarios and present our findings in Table 4.

Table 4: Pattern table for matrix multiplication ($R = P \times Q$): Various methods for tiling the input. Dimensions of $P: H \times C$, $Q: C \times W$; $α_C = C / CT$; $α_H = H / HT$; $α_W = W / WT$

| Tiling Style | Loop Order | Pattern |
|--------------|------------|---------|
| Fix $P$ [24] | $h_T > c_T > w_T$ | $W_P: (1^α_H \cdot 2^α_W \cdots α^α_C)_{α_H}$ $R_P: (1^α_H \cdot 2^α_W \cdots (α_C - 1)^α_H)_{α_H}$ |
| Fix $Q$ [24] | $c_T > w_T > h_T$ | $W_P: (1^α_C \cdot 2^α_H \cdots α^α_H)_{α_C}$ $R_P: (1^α_C \cdot 2^α_H \cdots (α_H - 1)^α_C)_{α_C}$ |
| Fix $R$ [24] | $w_T > h_T > c_T$ | $W_P: (1^α_H \cdot 2^α_W)_{α_H}$ $R_P: -$ |

5.2.1 Image Pre-processing/ Pooling

Numerous machine learning applications require the input image to be in a specific format. Additionally, it may be necessary to enhance an image’s features prior to computation. This necessitates an analysis of the data movement patterns generated by various image pre-processing methods.

We divide image pre-processing applications into three computation styles. The output channel is sometimes completely dependent on a single input channel, the scenario is represented as Style-1: $S = T(X)$, where $T$ represents the transformation function, and $X$ represents the input element. Because there is no requirement to store partially computed outputs in memory, the output access pattern will be linear. However, as illustrated in Table 8 (in the Appendix), the number of output tiles will vary. We observe that pooling and Style-1 computations follow a similar pattern. Typically, a window is positioned above the image to perform computations relative to the surrounding pixels in order to generate an output pixel. Style-2 depicts a scenario in which all input channels are merged to form a single output channel $S = T(R, G, B)$, whereas Style-3 depicts a scenario in which all input channels are merged using various transformations to form multiple output channels. Please refer to Table 9 and Table 10 (in the Appendix).

Insight: We note that the pattern of VN updates is highly deterministic and is quite similar across a range of operations. All of the patterns can be expressed using a single master equation: $(1^α_H \cdot 2^α_W \cdots κ^α_C)^ρ$. The triplet $(η, κ, ρ)$.

6. DESIGN OF SECULATOR

6.1 Overview

The Seculator NPU architecture provides a hardware-assisted secure environment for the execution of neural networks. A high-level design of the framework is presented in Figure 6. The host CPU securely delivers instructions (using a shared key) to the accelerator via a PCIe link to execute a layer of the CNN. It also points to the location of the encrypted data stored in memory. Thereafter, the accelerator starts the execution. Initially, all the model parameters and the user input are encrypted and stored in memory. During the processing, the data is transferred to the NPU to perform the convolution operation. The compute engine is made up of a PE array and some local storage (CE). When a layer is completed successfully, the accelerator notifies the host and writes the encrypted data to memory. In the case of a security breach, a system reboot is performed.

A security breach is detected by the security module, which will be in charge of securing the data and protecting it from various threats. To reduce the overheads and memory traffic, we integrate the version number generator with the security module such that the processed versions can be directly consumed. We explain the modules in the following subsections.

6.2 A Deterministic Version Generation Scheme

Seculator encrypts the output data when the data is evicted from the global buffer to memory. To automatically generate the VNs for the output data, we thoroughly analyzed the movement of ofmap tile data in Section 5. An automatic VN generation scheme helps reduce the overheads associated with the storage and management of VNs. Even though the storage requirements per se are not very high (max: 8 KB in prior work [21]), the additional complexity in the design and runtime for reading this table, which is stored in the host CPU’s secure memory, is quite onerous. Seculator overcomes this limitation by generating VNs automatically (once for every group of tiles) as per the master equation in Section 5: $(1^α_H \cdot 2^α_W \cdots κ^α_C)^ρ$.

The triplet $(η, κ, ρ)$ is securely shared with the accelerator by the host CPU along with a session-specific encryption key (to decrypt data for the first time). Subsequently, we generate VNs based on memory accesses and the value of the triplet.

6.3 Details of the Encryption Process

We rely on AES counter-mode encryption (CTR) for encrypting each data block. To encrypt a 64-byte data block, we employ four parallel AES-128 engines. The 128-bit key
is created by concatenating the accelerator’s secret id (embedded within it) with a random number generated prior to execution. This technique ensures that the key is hardware-specific and changes with each execution. The major counter value is created by concatenating the fmap ID and layer ID, whereas the minor counter value is created by concatenating the VN and index of the block within the fmap. This approach ensures that the counter value changes in accordance with the index of the block in an fmap (the same value is encrypted differently). The counters are encrypted using the AES-CTR mode to generate a one-time pad (OTP). This OTP is XORed with the block data to create the ciphertext (standard algorithm).

6.4 MAC Generation

Unlike competing work, we do not maintain per-block MACs, we operate at the layer-level. The reason that prior work maintained per-block MACs is because they wanted to give the freedom to subsequent layers to read data randomly (no pre-specified order). We also give the same freedom, with one caveat, which is that all the ofmaps that have been produced in Layer \(i\) need to be accessed at least once in Layer \(i + 1\). This is a very reasonable restriction.

When we read/write a block, we compute its MAC. The 32-byte MAC is computed as
\[
MAC = SHA_{256}(P||L||F||VN||I||B),
\]
where, \(P\) is the secret id of the accelerator, \(L\) is the layer id, \(F\) is the id of the fmap, \(I\) is the block index within the fmap, and \(B\) is the contents of the data block (64-bytes). || is the concatenation operator.

Let the MAC of a block that is being read/written be denoted by \(MAC_B\). We maintain two 256-bit registers: \(MAC_R\) (for reads) and \(MAC_W\) (for writes). For a block that is read we compute
\[
MAC_R = MAC_R \oplus MAC_B,
\]
where \(\oplus\) is the XOR operator. We do the same in the case of writes, albeit with the register \(MAC_W\). As per Bellare et al. [3], this scheme is quite secure (theoretically similar to chaining).

We need to verify that whatever has been written is also read back without tampering. \(MAC_W\) embodies everything that has been written. If we analyze all the access patterns in Section 5, we observe that in the same layer we read everything back other than data written in the last iteration. This is read back in the next layer. In the next layer, we use one more register \(MAC_{FR}\) (first read) that computes a MAC of all the ifmap data (ofmaps of the previous layer) that is read for the first time. We use the layer id of the previous layer. Note that it is very easy to design a circuit using our master equation to figure out when an input tile is read for the first time (not shown due to a lack of space).

The crucial condition that needs to hold is as follows. This is provable from the equations shown in Section 5.

\[
MAC_W = MAC_{FR} \oplus MAC_R
\]

We can use two pairs of these registers (that alternate across layers) because of the overlaps in terms of usage (need \(MAC_R\) for the previous layer when the current layer is being processed).

Let us now consider read-only data such as inputs and filter weights. Their VN remains the same (it is equal to the last-generated VN in the previous layer for ifmaps and 1 for filter weights). Without loss of generality, consider ifmap data. We maintain a separate \(MAC_{IR}\) register for it. If the same ifmap tile is read an even number of times, the result of all the XOR operations to update \(MAC_{IR}\) should be zero, otherwise it will be equal to the XOR of the MACs – same as the first-read data (\(MAC_{FR}\)). This is because the outputs of the previous layer should be the inputs of the current layer. In either case, the inputs are verified because we are verifying that the “first-read” data for the inputs is correct in Equation 1.

7. EVALUATION

7.1 Setup

We showed the detailed simulation setup and list of benchmarks in Section 4. We evaluate 5 designs as shown in Table 5. They are the baseline design (no security), secure design (ClientSGX), TNPU, GuardNN, and Seculator. We implemented the hardware of the pattern generator circuit, the SHA-256 and AES circuits in Verilog. We used the Cadence Genus Tool to synthesize, place, and route the design in a 28 nm technology (scaled to 8 nm using the results in [16]). TNPU and secure use an 8 KB MAC cache. We conducted simulations for an augmented design, Seculator+, that protects against MEA and bus snooping attacks (details in Section 7.5).

| Configuration | Integrity (MAC) | Encryption (AES) | Anti-Replay | MEA |
|---------------|----------------|-----------------|-------------|-----|
| Baseline      | x              | x               | x           | x   |
| Secure        | per-block      | CTR             | Counters    | x   |
| TNPU          | per-block      | XTS             | VN          | x   |
| GuardNN       | per-block      | CTR             | VN          | x   |
| Seculator     | per-layer      | CTR             | VN          | ✓   |
| Seculator+    | per-layer      | CTR             | VN          | ✓   |

Table 5: Simulated designs

7.2 Verilog Synthesis Results

The overhead associated with the hardware structures is shown in Table 6. We incur a marginal area overhead of 4210 \(\mu m^2\) (area) and a sub-mW power overhead.

| Module   | Area (\(\mu m^2\)) | Power (\(\mu W\)) |
|----------|--------------------|-------------------|
| AES-128  | 3900               | 640               |
| SHA-256  | 270                | 40                |
| VN generator | 40                | 4.4               |

Table 6: Overhead associated with the h/w structures

7.3 Performance Analysis

Figure 7 presents the performance results. The baseline configuration is used to normalize the results.

We reduced the performance overhead by nearly 20% compared to the state-of-the-art scheme TNPU. The fact that
Figure 7: Normalized performance for different workloads

TNPU verifies integrity block-by-block results in a large number of MAC accesses. With TNPU, we observed nearly 35% misses in the MAC cache since streaming data results in a high cache miss rate as described in Section 4. This results in an increase in DRAM accesses as shown in Figure 8 (17% more than Seculator). Additionally, the access to the Tensor Table/tile stored in the secure memory location adds to the overhead. Seculator simplifies the design by computing on-chip versions, thus eliminating the requirement for additional DRAM accesses. Because of direct DRAM accesses, there is a good correlation between the DRAM traffic and the performance.

In GuardNN, the MACs are generated according to the granularity of the accelerator data block (64 bytes). The scheme does not use any MAC cache. All the MACs are stored in an off-chip memory. Each data read or write request is accompanied by a MAC read/write request. This leads to a high memory traffic (40% more than Seculator) with a performance degradation of nearly 37% as compared to Seculator.

7.4 Security Analysis

Seculator provides data confidentiality because all the data outside the TCB is encrypted. It provides security against replay attacks because every memory write is assigned a different VN. It cannot be targeted by man-in-the-middle attacks because no other entity has the secret id or the runtime key of the NPU. Finally, it provides integrity because we only read whatever is written. This holds on a per-block basis and is not dependent on the order of access because we use the commutative XOR function and include the block id (position of the block in the fmap) in the MAC calculation. The cryptographic security guarantees are quite similar to traditional chaining-based solutions [3]. It should also be noted that data blocks with the same content and address produce different ciphertexts over time (because of the VN and the execute-time key). Finally, note that our order-independent MACs can be visualized as hashing read and write sets to 32-byte values. From the master equation and the check in the subsequent layer, we can conclude that the sets are the same (a formal proof not included for lack of space). Both the generated VNs and the MAC verification scheme were rigorously experimentally validated.

Figure 8: Normalized memory traffic for different workloads

7.5 Scalability Analysis: Seculator+

Li et al. [23] suggest many methods to prevent MEA and memory-based side-channel attacks. A key technique is layer widening: increase the size of all layers by padding junk data such that it is not possible to find their real size. To investigate the effect of layer widening, we increase the size of the base layer (32 × 32 × 3) to (56 × 56 × 3), (64 × 64 × 3), (128 × 128 × 3), (160 × 160 × 3) and (192 × 192 × 3) as shown in Figure 9. We observe that Seculator is the most scalable.

8. RELATED WORK

TEEs provide a secure platform for the execution of CNN workloads even in an untrusted environment; additionally, they outperform computationally heavy cryptographic methods such as fully homomorphic encryption [6]. Recent works focus on (1) outsourcing the computation to an untrusted GPU [12, 35]; (2) optimizing a pre-existing TEE such as SGX
8.1 Outsourcing Computations

Slalom [35] and DarkNight [12] focus on providing a hybrid and secure execution platform to users. They split the computations between a TEE and an untrusted GPU. Layers are obfuscated and delegated from the TEE to the GPU. The output from the unsecure GPU is verified using the Freivald’s algorithm [35]. The central insight behind the data obfuscation step is that convolution is a bilinear operation. Instead of directly exposing the inputs to an untrusted third party, the CPU adds controlled noise. The bilinear property will ensure that the noise can later on be removed from the computed result. The overheads associated with input blinding, output verification along with the additional communication overhead due to data transfer from the TEE to the GPU cannot be avoided. Seculator relies on a TEE alone, hence, these overheads are not involved.

HybridTEE [9] divides the computation between a constrained-resource local TEE (ARM Trustzone) and a resource-rich remote TEE (Intel SGX) based on the presence of security-critical features. A separate algorithm is used to detect which parts of the image are security-critical (the SIFT and YOLO algorithms are used). However, executing an auxiliary DNN to find security-critical features might lead to high overheads and may compromise system security.

8.2 Optimizing Intel SGX

Several works such as [19, 22, 36] focus on optimizing the execution of the whole DNN within a TEE. Vessels [19] solves the problem of low memory re-usability and a high memory overhead by creating an optimized memory pool for the TEE. This is done by characterizing the memory usage patterns in a CNN layer. Similarly, Truong et al. [36] propose to partition the layers to minimize the memory usage. In Occlumency [22], the authors proposed a memory-efficient feature map allocation technique and partitioning convolution operation to optimize the CNN execution in SGX.

On the contrary, DeepEnclave [11] aims to secure only the user data. It optimizes the memory utilization by executing the initial few layers inside the secure enclave and the latter outside. It is important to note that these works use the vanilla version of client-side SGX where Merkle trees and eviction trees are maintained for the entire data. However, we should note that such memory optimizations lose their utility in modern server-side SGX-based designs where the enclave size can be as large as 512 GB [30]. The key advantage of our scheme is that we provide all security guarantees without the additional overheads of counters and Merkle trees.

8.3 Designing a Custom TEE

GuardNN [15] and TNPU [21] focus on bringing security guarantees provided by traditional secure processors such as Intel SGX to custom accelerators. The majority of the overheads in a conventional secure processor comes from cache misses and Merkle tree traversals. GuardNN and TNPU both aim to eliminate the Merkle tree and counters with a more sophisticated and efficient VN management mechanism that makes use of a DNN’s extremely deterministic and statically defined memory access patterns.

TNPU needs a “Tensor Table” to keep track of the output tile updates (every update is associated with a new version number). Since input tiles are never updated, the VN’s linked with them are never updated. TNPU divides the secure memory into two regions: the first is protected by the information stored in the Tensor Table (Region 1), while the second 128 KB secure memory region is protected by a system similar to SGX-Client (Region 2). The Tensor Table protects Region 1, and the table itself is stored in Region 2. MACs are generated at the granularity of individual blocks and they are stored in an 8 KB on-chip MAC cache (overflows go to main memory).

GuardNN relies on counter-mode encryption, which requires VNs. For memory writes, the accelerator generates

| Work | Security (via encryption) | Freshness (via VNs) | Integrity (via MACs) | MEA prot. | Tile size |
|------|--------------------------|---------------------|---------------------|-----------|----------|
| Outsourcing computations [9, 12, 35] | Partial | Block | BTm + TM | Block | $BTH$ | × | 64 blocks |
| SGX + Optimizations [19, 22, 36] | Full | Block | BTm + TM | Block | $BTH$ | × |  |

Custom accelerators

| Work | Security (via encryption) | Freshness (via VNs) | Integrity (via MACs) | MEA prot. | Tile size |
|------|--------------------------|---------------------|---------------------|-----------|----------|
| NPUFort [40] | Partial | Block | BTV | – | – | Obscure time* | Depends on resources, scheduling scheme and workload |
| Seal [43] | Partial | Block | BTV | – | – | × |  |
| TNPU [21] | Full | Tile | TV | Block | $BTH$ (on-chip) | × |  |
| GuardNN [15] | Full | Tile | TV | Block | $BTH$ (off-chip) | × |  |
| Seculator | Full | Layer | V | Layer | $O(H)$ (on-chip) | Widen layers |  |

Table 7: A comparison of related work

or Tensorcone [9]; and designing a secure, custom accelerator [15]. We present a brief comparison of related works in Table 7.
| Tiling Style       | Loop order (OR) | Pattern (Style-1) |
|-------------------|-----------------|------------------|
| Channel-wise      | k               | $\text{WP: 1}^{\alpha_k}$ |
| Multi-channel     | $k_T$           | $\text{RP: }$ |
| Partial channel   | $h_T \triangleright k_T$ | $\text{WP: 1}^{\alpha_k \triangleleft w}$ |
| Partial-multi-channel | $h_T \triangleright w_T \triangleright k_T$ | $\text{RP: }$ |
| Full-channel      | $h_T \triangleright w_T$ | $\text{WP: 1}^{\alpha_{w_T}}, \text{RP: }$ |

Table 8: Pattern table for image pre-processing (Style-1)/Pooling ($S_{\alpha} = T_{\alpha}$): Various possibilities for scheduling the output tiles for performing pooling or image pre-processing ($H_T, W_T, C_T$) represents the tiling factor. ($C = K$)

| Tiling Style       | Output Reuse | Loop order (IR) | Rd/Wr Pattern |
|-------------------|--------------|-----------------|---------------|
| Channel-wise      | $c \triangleright k_T$ | $k_T \triangleright c$ | $\text{WP: 1}^{\alpha_K}$ |
| Multi-channel     | $c_T \triangleright k_T$ | $k_T \triangleright c_T$ | $\text{RP: }$ |
| Partial channel   | $h_T \triangleright w_T \triangleright h_T \triangleright c_T$ | $k_T \triangleright h_T \triangleright w_T \triangleright c_T$ | $\text{WP: 1}^{\alpha_{w_T}} \text{RP: }$ |
| Multi channel     | $h_T \triangleright w_T \triangleright k_T$ | $k_T \triangleright h_T \triangleright w_T \triangleright k_T$ | $\text{RP: }$ |
| Partial channel/Multi channel | $- \triangleright -$ | $k_T \triangleright h_T \triangleright w_T \triangleright k_T$ | $\text{WP: 1}^{\alpha_{w_T}} \text{RP: }$ |
| Multi channel     | $- \triangleright -$ | $k_T \triangleright h_T \triangleright w_T \triangleright k_T$ | $\text{RP: }$ |
| Full-channel      | $h_T \triangleright w_T \triangleright k_T$ | $k_T \triangleright h_T \triangleright w_T \triangleright k_T$ | $\text{WP: 1}^{\alpha_{w_T}} \text{RP: }$ |

Table 9: Pattern table for image pre-processing (Style-2: $S = T(R, G, B)$): Different methods of scheduling input tiles ($K=1$)

Table 10: Pattern table for image pre-processing (Style-3: $S_{\alpha} = T_{\alpha}(R, G, B)$)

VNs using on-chip counters, which are managed by the scheduler (running on the host CPU with a secure TEE). For memory reads, VNs are received from the scheduler on the host CPU. GuardNN also generates block-specific MACs which are not stored in an on-chip cache (read directly from main memory).

Due to the high memory requirements of DNNs, generating per-block MACs like GuardNN and TNPU results in high memory overheads. Even if an on-chip cache is used, the situation does not improve significantly because caches are not optimized for streaming data. Seculator addresses these two concerns by significantly reducing the number of MACs required to verify the integrity of a DNN. Additionally, because both GuardNN and TNPU are incapable of providing any additional security guarantees, both are susceptible to model extraction attacks (MEAs), which rely on side-channel leaks such as addresses or memory bus snooping. The Seculator+ architecture is scalable, and can thus be used to implement layer widening very efficiently. This will help protect against the aforementioned class of attacks.

For GPUs, [42] and [25] provide a secure execution environment that is quite similar to GuardNN. They are not specific to neural networks and thus don’t leverage their characteristics. NPUFort [40] is a custom accelerator that encrypts security-critical features similar to HybridTEE. We, on the other hand, focus on full encryption and our system is tailored for neural networks.

9. CONCLUSION

We showed that competing works such as GuardNN and TNPU naturally segue into the Seculator proposal. It is a logical successor in this line of work, where the move to layer-level security checks is complete. For realizing this, it was necessary to mathematically characterize a large number of memory access patterns (with different levels of stationarity) and encode them efficiently. The VN generator coupled with the MAC verifier helped realize layer-level operations. Because of the reduced need for data storage and consequently reduced DRAM traffic, it was possible to reduce wasted cycles, and achieve an additional 16% throughput as compared to TNPU, which is the nearest competing work. We could further show that our mechanism could be tweaked to introduce controlled noise into the execution such that it becomes harder to mount address snooping or side-channel attacks.

APPENDIX

We show the results for image pre-processing (Style-1, Style-2, and Style-3) in Tables 8, 9, and 10.
[42] S. Yuan, A. Awad, A. W. B. Yudha, Y. Solihin, and H. Zhou, "Adaptive security support for heterogeneous memory on gpus."

[43] P. Zuo, Y. Hua, L. Liang, X. Xie, X. Hu, and Y. Xie, "Sealing neural network models in encrypted deep learning accelerators," in \textit{2021 58th ACM/IEEE Design Automation Conference (DAC)}. IEEE, 2021, pp. 1255–1260.