Design and Implementation of a Modified Luo Converter with Higher-Voltage Ratio Gain

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Abstract: This paper presents a new modified of the positive output super-lift Luo (POSL) converter in order to increase the output voltage gain. The conventional elementary Luo converter has a voltage lift cell, which consists of one inductor, one diode and one capacitor. The main drawback of the elementary circuit is near conventional boost converter in terms of lifting output voltage at a higher duty cycle. The novelty of proposed modification provides high-voltage transfer ratio gain by changing the inductor (L) of the basic (POSL) with switched–capacitor–inductor cell, which consists of two diodes, one capacitor and two inductors. The advantages of the proposed converter over elementary circuit are can be increasing the output gain ratio at a lower and higher duty cycle as well as low voltage stress on switch. Pulse width modulation (PWM) as a voltage mode control strategy is used to control the new converter. The new converter works by using one switch to make the control simple, more efficient and more effective. In addition, the equations of voltage and current in continuous and discontinuous conduction modes (CCM) and (DCM) are analyzed at steady-state error. The simulation and practical results show the effectiveness of matching the new converter to the theoretical analysis as well as the proposed converter has higher efficiency is reached to 95.4% as compare with elementary circuit has 94.1%. The simulation is performing by Matlab/Simulink environment.

1. Introduction.
In recent years, the (DC–DC) converters are used in many electrical and industrial devices, such as light emitting diode (LED), power factor correction and portable devices such as mobile phones (smart phones) and portable computers (laptops). The major idea of these converters is to get more reliability and more efficiency. The pulse width modulation (PWM) techniques are responsible for operating the switches of these converters, which are categorized into two types (isolated and non–isolated). The first type is (Isolated DC–DC converters) such as half-bridge, full-bridge, fly-back and push-pull, etc. In this type, High-frequency transformer is used in order to provide high voltage gain by changing turns ratio of the transformer. Moreover, high–frequency transformers have many disadvantages such as high cost, high voltage switching and high losses because of the transformer leakage inductance [1]. Active clamp circuit or (non–dissipative snubber) is used to minimize this problem, which will rise the size and cost of the converter and make the control process more difficult [2]. The second type is (non–isolated DC–DC converters) such as SEPIC, CUK, buck–boost and boost converters, etc. In this type, high–frequency
transformer is not used and therefore, non–isolated (DC–DC) converters have low cost, small size, low losses of switching and higher efficiency [3].

Recently, the family of Luo converter are more widely used because of its simplicity operations and control [4]. (POSL) converter is the most common used in the family of Luo converters [4, 5]. The types of this family include elementary, re–lift and triple circuits [5]. Also, in [5] an expanded analysis of (POSL) converter in the different conditions of operation is introduced. Lately, modern (DC–DC) conversion improvement strategies such as switched-inductor cell (SL), switched-capacitor cell (SC) and voltage–lift (VL) strategies have been proposed in [6, 7]. The switched–capacitor (SC) and switched–inductor (SL) are effective techniques used widely in electronic circuits and the purpose of these techniques is to step–up or step–down voltage transfer ratio gain [8]. Moreover, the voltage–lift (VL) strategy is used widely in electronic circuits and the objective of this method is to get voltage increase and better performance of the conventional (DC–DC) converters [9, 10]. Also, in [11] another form for non–isolated boost (DC–DC) converter depends on (VL) strategy is presented which provides high voltage gain. [12] Indicates for more expanded analysis of (POSL) converter in different forms. Another method of rising the voltage transfer ratio gain by using voltage–lift technique implemented on split–inductor type boost converter. Although, this method succeeded in getting high voltage transfer ratio gain, but this circuit consists of many electrical elements and four switches and as a result, it becomes difficult to control, higher in cost, bigger in size, and needs some modern techniques to control it [13]. In [14], transformless (DC–DC) converter is used to gain high voltage transfer ratio gain by using simple circuit, but the disadvantage of this circuit is that it is unable to supply very high voltage transfer ratio gain.

In [15], another technique of providing high voltage transfer ratio gain is presented. This technique is known as diode capacitor voltage multiplier, which is built on two common schemes (‘Cockcroft–Walton and Dickson’). Also, this technique is added to the boost converter and works at high switching frequency. In [16], a new technique that provides high voltage Boost Converters which depends on Bootstrap Capacitors and Boost Inductors. This technique is formed by changing the anode of the diode connection position. The demerit of this converter is using two different control circuits, which make it more complex, big in size, high in price and producing high losses.

In [17], a modern method of increasing the voltage ratio gain has been proposed by using single switch non–isolated (DC–DC) converter. This converter is formed by integrating the switched–inductor cell (SL), switched–capacitor cell (SC) and extra boost capacitor. In [18], an additional strategy of obtaining high voltage transfer ratio by changing the inductor of (POSL) converter with a switched inductor cell (SL).

All the papers above are presented to show various suggestions of increasing the voltage by using different techniques and different methods.

This paper introduces new design and improved modification of (POSL) converter by changing the inductor of (POSL) with switching capacitor–inductor cell. The cell consists of two inductors, one capacitor and two diodes. An important characteristic of the new converter is using single switch control. In addition, only one control circuit controls the new converter, which is pulse width modulation (PWM) voltage mode control. The study of analysis of the new converter in continuous and discontinues condition modes (CCM) and (DCM) is presented. Furthermore, the new converter provides high–voltage transfer ratio gain.

The organization of this paper is: In section one, new modification of POSL converter is introduced. In section two, analysis of the new converter is introduced. In section three, design of the circuit elements is introduced. In section four, control strategy is presented. In section five, experimental results is presented and section six presents the conclusion.

2. The new modification of POSL converter.

The basic converter (POSL) is presented in (Fig. 1A) and the new converter is introduced in (Fig. 1B). The new converter is formed by changing the inductor (L) of the (POSL) converter with the switched
capacitor–inductor cell which consists of two inductors (\(L_1\) and \(L_2\)), two diodes (\(D_1\) and \(D_2\)) and one capacitor (\(C_1\)). The inductors \(L_1\) and \(L_2\) are magnetically coupled (non–isolated). In order to simplify the DC analysis, the following assumptions should be taken into consideration, i) all passive and active elements are ideal, ii) all capacitors are large enough and thereby the voltage across capacitors is constant, and iii) the DC analysis of converter in steady state which implies the output is constant. Also, in order to more reduce ripple, we assume both inductors are equal.

\[ L_1 = L_2 = L \]

Where \((L)\) is the inductance of the inductors

The transfer ratio of voltage \((M_D)\) of the elementary (‘POS\(L\)’) converter (Fig. 1A) from [18] is as follows:

\[
M_D = \frac{V_o}{V_{in}} = \frac{2 - D}{1 - D}
\]  

\((D)\) is the duty cycle of power switch.

3. The analysis of the new converter.
In this part, analysis of the new converter in the three modes (\(CCM\), \(DCM\)) and the boundary operating conduction mode (\(BCM\)) between \(CCM\) and \(DCM\) modes is presented.
3.1 The analysis in \((CCM)\) mode.

The switching operating of the new converter circuit (Fig. 1B) in a steady-state cycle of the \((CCM)\) is presented in (Figs. 2A, 2B) and the corresponding of its timing switch is presented in (Fig. 3). The operation modes of converter’s switches can be categorized into two modes, mode 1 and mode 2.

1. **Mode 1:** It starts from \(\{t_0, t_1\}\). (Figs. 2A and 3). At \((t_0)\) the switch \((S)\) is turned \((ON)\). Thus, two capacitors \((C_1 \text{ and } C_2)\) and two inductors \((L_1 \text{ and } L_2)\) are connected in parallel to the voltage source \((V_{in})\) by the diodes \((D_1, D_2 \text{ and } D_3)\). In this period, the diodes \((D_1, D_2 \text{ and } D_3)\) are in forward mode and the diode \((D_0)\) is in reverse mode.

2. **Mode 2:** This mode starts from \(\{t_1, t_2\}\), (Figs. 2B and 3). At \((t_1)\), the switch \((S)\) is turned \((OFF)\). Now, the two capacitors \((C_1 \text{ and } C_2)\), the source voltage \((V_{in})\) and the two inductors \((L_1 \text{ and } L_2)\) are series connected with the capacitor \((C_0)\) to the load by the diode \((D_0)\). In this period, the diode \((D_0)\) is in the forward mode and the diodes \((D_1, D_2 \text{ and } D_3)\) are in the reverse mode.

At first, we will explain the voltage transfer gain ratio \((M_D)\) of the new converter circuit in the \((CCM)\) mode.

![Diagram](image-url)

**Figure 2.** Switching steps of the new converter circuit at \((CCM)\), A.: \(t_{on}\), and B.: \(t_{off}\)
Figure 3. The diagram of timing switch of the new converter for CCM

At the switching (ON) period \((t_{on} = D \, T)\)

\[ V_{in} = V_{L1} = V_{L2} \]

\[ V_{in} = V_{C1} = V_{C2} \]

And at the switching (OFF) period \((t_{off} = (1 - D) \, T)\)

\[ V_{in} - V_{L1} - V_{L2} + V_{C1} + V_{C2} - V_o = 0 \]

\( (3) \)
As a result, for the switching (OFF) period we get:
\[ V_{L1} = V_{L2} = \frac{3V_{in} - V_o}{2} \]  
(4)

According to principle of voltage—second balance equation across the inductors (\( L_1 \) and \( L_2 \)) we get:
\[ V_{in} D T + \frac{3V_{in} - V_o}{2} (1 - D) T = 0 \]  
(5)

Therefore, we can express the relation for the voltage transfer ratio from equation (5) as bellow:
\[ \frac{V_o}{V_{in}} = \frac{3-D}{1-D} \]  
(6)

The voltage gain ratio of the new converter circuit in (CCM), (\( M_D \)), is:
\[ M_D = \frac{V_o}{V_{in}} = \frac{3-D}{1-D} \]  
(7)

A comparability of the voltage transfer gain ratio (\( M_D \)) for the elementary (POS L) converter and the new converter is presented in (fig. 4)

![Figure 4](image-url)

**Figure 4.** Comparability of the voltage transfer gain ratio (\( M_D \)) for the elementary (POS L) converter and the new converter

For ideal components, the input power and the output power are equal; therefore, we can obtain the input current as bellow:
\[ I_{in} = \frac{3-D}{1-D} I_o \]  
(8)

The charge (\( Q \)) of capacitor (\( C_0 \)) increases during \( \{ t_1, t_2 \} \) period (switching–OFF) and decreases during \( \{ t_0, t_1 \} \) period (switching–ON). We obtain
\[ Q_{C0+} = I_o D T \]  
\[ Q_{C0-} = I_{C0-off} (1-D) T \]  
(9)

During the switching ON and OFF cycles (\( Q_{C0+} = Q_{C0-} \)). As a result, from equation (9), we get:
\[ I_{C0-off} = \frac{D}{1-D} I_o \]  
(10)

During \( \{ t_1, t_2 \} \) period (switching–OFF), \( I_{D0} = I_{C0} + I_o \). Thus,
\[ I_{D0-off} = I_{C0-off} + I_o \]  
(11)
\[ I_{D0-off} = \frac{1}{1-D} I_o \] (12)

Moreover, during \{ \text{t}_1, \text{t}_2 \} period (switching–\text{OFF}), \(C_1, C_2, L_1 \) and \(L_2 \) are become series connected to discharge their stored energy to the load through \(D_0 \). Therefore,

\[ I_{L1} = I_{L2} = I_{C1-off} = I_{C2-off} = I_{D0-off} = \frac{1}{1-D} I_o \] (13)

In both of the switching cycles, \( Q_{C1+} = Q_{C1} \) and \( Q_{C2+} = Q_{C2} \) Therefore,

\[ I_{C1-on} = \frac{1-D}{D} I_{C1-off} = \frac{1}{D} I_o \] (14)

\[ I_{C2-on} = \frac{1-D}{D} I_{C2-off} = \frac{1}{D} I_o \] (15)

The (peak–peak) current variation of inductor (\(\Delta i_L \)), \(\Delta i_L \) is equal to \((\frac{D TV_{in}}{L})\), where the variation ratio of the current in inductor is \((\zeta_L)\), and since \(L_1 = L_2 = L \). So;

\[ \zeta_L = \frac{\Delta i_L}{i_L} = \frac{D(1-D)}{M_D} \frac{R}{2fL} \] (16)

Therefore, according to the equation (16) the variation ratios of the current in inductors (\(L_1\) and \(L_2\)) are:

\[ \zeta_{L1} = \zeta_{L2} = \zeta_L = \frac{\Delta i_L}{i_L} = \frac{D(1-D)}{M_D} \frac{R}{2fL} \] (17)

The current variation of the output diode (\(\Delta i_{D0} \)) during \{ \text{t}_1, \text{t}_2 \}, (switching–\text{OFF}) period is equal to the current variation (\(\Delta i_L \)) of inductors. Thus, the variation ratio of the output diode current (\(I_{D0} \)) is \((\zeta_{D0})\)

\[ \zeta_{D0} = \zeta_{L1} = \zeta_{L2} = \zeta_L = \frac{\Delta i_{D0}}{i_{D0-off}} = \frac{D(1-D)}{M_D} \frac{R}{2fL} \] (18)

The ripple of inductor current variations that extracted in equations (16–18) during the switching cycle is different due to (\(L_1 \neq L_2 \)). Since, the inductors (\(L_1 \) and \(L_2 \)) are discharge energy in series during the switching–\text{OFF} period. Therefore, if the inductors (\(L_1 \) and \(L_2 \)) are equal, the ripple of inductor current variations will be smaller under high switching frequency.

The (peak–peak) variation of the output voltage (\(\Delta V_o \), \(\Delta V_o \) is equal to \((\frac{D T I_o}{C_o})\)). Therefore, the variation ratio of the output voltage \((\varepsilon_s)\) is equal to:

\[ \varepsilon_s = \frac{\Delta V_o}{V_o} = \frac{D}{2C_o R f} \] (19)

3.2 The analysis in (DCM) mode.

The switching operating of the (DCM) can be divided into three modes, known as mode 1, mode 2 and mode 3.

1. Mode 1: This mode starts from \{ \text{t}_o, \text{t}_1 \}. The switch (\(S\)) is turned (\text{ON}) in this period, as presented in (Fig. 2A) and the corresponding timing diagram is shown in (Fig. 3). In this mode, the operation of (CCM) and (DCM) is the same. The (peak–peak) variation of the current in inductors (\(\Delta i_L \)) in the inductors, \(L_1 \) and \(L_2 \) can be found as: Where (\(I_{LP}\)) is also known as: (peak–peak) variation of the current in inductors and \(L_1 = L_2 = L \)

\[ I_{L1P} = I_{L2P} = \Delta i_L = \frac{D TV_{in}}{L} \] (20)

2. Mode 2: This mode starts from \{ \text{t}_1, \text{t}_2 \}. The switch (\(S\)) is turned (\text{OFF}) in this period, as presented in (Fig. 2B) and the corresponding timing diagram is presented in (Fig. 6). The voltage source (\(V_{in}\), \(C_1, C_2, L_1 \) and \(L_2 \) are series connected to discharge their stored energies to \(C_o \) and to the load. At (\(t = t_2 \)), inductors current \(I_{L1} \) and \(I_{L2} \) become zero. Another form of \(I_{L1P} \) and \(I_{L2P} \) is presented as follows:

\[ I_{L1P} = I_{L2P} = \Delta i_L = \frac{(V_o - 3V_{in})D_2 T}{2L} \] (21)

3. Mode 3: This mode starts from \{ \text{t}_2, \text{t}_3 \}. The switch (\(S\)) is still turned (\text{OFF}) in this period, as presented in (Fig. 5) and the corresponding timing diagram is presented in (Fig. 6). The energies that
stored in $L_1$ and $L_2$ become zero. Therefore, only the energy that stored in $C_o$ is discharged to the load. The period ($D_2$) is calculated at steady state from equal the two equations (20 and 21) as follows:

$$D_2 = \frac{2V_{in}D}{V_o - 3V_{in}}$$

(22)

Figure 5. Steps of switching of the new converter circuit at (DCM)
From (Fig. 6), the average value of the output—capacitor current ($I_{CO}$) during both switching operatio
(ON and OFF) is as follow:

$$I_{CO} = \frac{1}{2} D_2 I_{LP} T - I_0$$

At steady state, $I_{CO}$ becomes zero in equation (23) so we get:

$$I_0 = \frac{1}{2} D_2 I_{LP}$$

Substituting (20) and (22) into (24) and ($I_0 = \frac{V_o}{R}$) we get:

$$\frac{V_o}{R} = \frac{V_{in}^2 D^2 T}{(V_o-3V_{in}) L} = \frac{V_{in}^2 D^2}{(V_o-3V_{in}) L f}$$

Switching frequency ($f$) is equal to ($f = \frac{1}{T}$) and ($\tau_L$) is the normalized time constant of inductors defined
as follows:

$$\tau_L = \frac{L f}{R}$$

Substituting (26) into (25), the voltage gain ratio can be derived as follows:
is the voltage gain ratio of the new converter’s circuit in \((DCM)\) is:
\[
M = \frac{v_o}{V_{in}} = \frac{3}{2} + \frac{D^2}{4} + \frac{D^2}{\tau_L}
\] (27)

3.3 The analysis in \((BCM)\) mode.
Another mode of operating of the new converter known as boundary conduction mode \((BCM)\). If the new converter is operated in this mode, the voltage ratio gains of the \((CCM)\) and \((DCM)\) will be equal. From (7) and (27), the boundary normalized time constant \((\tau_{LB})\) of the inductor can be written as:
\[
\tau_{LB} = \frac{D (1-D)^2}{2 (3-D)}
\] (28)

The boundary between the two modes \((CCM)\) and \((DCM)\) is presented in (fig. 7).

![Figure 7. Boundary line between the two modes \((CCM)\) and \((DCM)\)](image)

4. Design of the circuit elements

4.1. Inductors design
In order to minimize the ripple in the new converter, the inductors values are chosen equal \((L_1 = L_2 = L)\). Therefore, the value of the inductors can be designed by assuming the ripple in current \((\Delta I_L)\) and switch frequency \((f)\) as:
\[
I_{L1} = I_{L2} = \frac{D V_{in}}{f \Delta I_L}
\] (29)

4.2. Capacitor design
The capacitor design depends on the switching frequency \((f)\) and capacitor voltage ripple \((\Delta V_c)\). So, the output capacitor \((C_o)\) can be evaluate from equation (19) as below:
\[
C_o = \frac{D V_o}{f R \Delta V_o}
\] (30)

Also, the value of boost capacitor \((C_1\) and \(C_2)\) can be designed as follows:
\[ C_1 = C_2 = \frac{I_m (1-D)}{2 f \Delta V_c} \]  

(31)

Substituting, eq. (8) in eq. (31), so we get:

\[ C_1 = C_2 = \frac{(3-D) V_o}{2 R f \Delta V_c} \]  

(32)

5. Control strategy (voltage mode control for new converter)

This control technique of the new converter is voltage mode control (VMC). It has advantages such as simple implementation and efficient. The principle operation of this technique relies on comparing the load voltage (output voltage) with constant reference voltage. The difference between the reference voltage and load voltage (output voltage) is called (error). The produced error is applied to the PID controller. The output of PID controller and saturation (‘Limiter’) goes into the (PWM) in order to drive the switch as presented in (fig. 8).

6. Experimental results.

The test parameters of proposed converter were designing according to equations (29, 30, 31 and 32). Therefore, the values of the components used in the design are; \( V_{in} = 12V \), and the switching frequency is \( f = 62kHz \), and \( D = 0.5 \). The parameters of circuit are as follow: \( L_1 = L_2 = 100 \mu H \), \( C_1 = C_2 = 680 \mu F \) and the output resistance is equal to \( R_o = 300 \Omega \). An IRF 250 MOSFT transistor is used. 

Figure 4 shows the superiority of the proposed converter over the elementary circuit in terms of increasing output voltage transfer gain. According to Figure 12, its shows the agreement between theoretical and experimental results that consists a comparison between output and input voltage practically.

Figure 7 shows the boundary point between continuous and discontinuous systems. The waveform of the voltage across inductors is confirmed in Figure 15. 

A simulation results of comparison between output and input voltages for the new converter are presented in (fig. 9). In addition, the output current of the new converter is shown in (fig. 10).
Figure 9. Comparison between output and input voltage.

Figure 10. Output current of the new converter
**Figure 11.** The switching frequency of the MOSFET transistor in simulation

**Figure 12.** The experimental results of the Comparison between output and input voltage practically.
Figure 13. The switching frequency of the MOSFET transistor

Figure 14. The experimental results of voltage across output diode (Dₐ)

Figure 15. The experimental results of voltage across inductors (L₁ and L₂)
7. Conclusion.
This paper presents a new design and implementation of a modified (POSL) converter has been presented. The proposed modified is done by replacing the inductor (L) of the basic (POSL) converter by proposed capacitor—inductor cell in order to allow ultra—increase in the voltage transfer ratio gain. The switched capacitor—inductor cell consists of two inductors, two diodes and one capacitor. In addition, the new converter has been designed, implemented and analyzed in CCM and DCM modes operations. The efficiency of proposed converters is reached to 95.4% but the elementary circuit has 94.1%. The result shows excellent agreement between simulation, practical and mathematical designed equations.

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