PERFORMANCE ANALYSIS OF MOD2N-1adders at schematic and RTL level using Cadence Virtuoso & Encounter tools

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Abstract

RNS has the ability to perform subtraction, addition independently with carry-free propagation. The structure of RNS requires two types of conversion: Forward Conversion and Reverse Conversion. To convert binary to residues, forward conversion is used whereas to convert residues to binary reverse conversion is used. Special moduli set and arbitrary moduli set are the two types of forward conversions. (2ⁿ-1) mod adder is one the important block used to get the special moduli set type of forward conversion. This paper consists of mod (2ⁿ-1) adders for the forward conversion technique and comparison of designs at both schematic level and RTL level. The schematic level designs provides low power than RTL design whereas the delay is reduced in RTL than Schematic design. The designs have been simulated for RTL using NC Launch - Encounter tool standard 90nm Technology. The designs have been simulated using CMOS 90nm virtuoso tool in cadence for schematic designs.

Keywords: Residue Number System, Forward Conversion, Reverse Conversion, Modular adder, Multiplexer.

I. Introduction

Residue Number System (RNS) is an un-positional number system which provides the single step multiplication, carry free addition and borrow free subtraction. RNS is used in the communication system such as image encryption and digital signal processing. To analyze the performance of RNS system, the data conversion and moduli selection are key parameters.

The RNS operation is performed in three stages. They are 1. Forward Conversion, 2. Modulo Channels, 3. Reverse Conversion. The structure of Residue Number system is as shown in Fig.1
Forward Converters are classified based on use of moduli set. They are arbitrary moduli set and special moduli set forward converters. The arbitrary moduli set forward converters are built using look-up tables. The special moduli set converters are based on combinational logic with low cost and it is advantageous in terms of power, speed and area.

The structure of special moduli set forward converter is shown in Fig. 2. The forward converter consists of Mod \((2^n-1)\), Mod \((2^n+1)\) adders as shown in Fig. 2. In this paper \((2^n-1)\) mod adders for forward conversion have been analyzed in terms of two different implementations i.e., RTL and Schematic design.

This paper contains of four sections: Introduction, Modular Addition, Simulation results and conclusion.

II. Modular Addition

Modular addition is one of the basic building block in the forward conversion process. If A and B are two numbers, the resultant expression for the Modular (mod) adder [I] is

\[ |A + B|_m = A + B \quad \text{if} \ A + B < m \]
The General structure of Mod \( m \) adder is shown in Fig. 3 [I]. It consists of two adders and one multiplexer (mux). The limitation of mod \( m \) adder is it only provides correct result for the less than or equal to mod value.

The structure of Mod \( (2^n-1) \) adder is shown in Fig. 4[II]. It has been designed by replacing the ‘\( m \)’ with \( (2^n-1) \) and adding OR gate to the path of multiplexer. The output of OR gate is given as selection input to Multiplexer. This design provides output to all cases except for inputs A and B are ‘111’.

![Figure 3. Structure of Modm adder[I]](image)

![Figure 4. Structure of Mod(2^n-1) adder [2]](image)
The structure which is shown in Figure.4 cannot work for inputs A and B are ‘111’ then, it has been modified [VII] to work for all input cases. The structure of modified Mod(2^n-1) adder is shown in Fig. 5. It contains two adders with Carry input as ‘0’ and ‘1’, two multiplexers and one AND gate.

Figure 5. Structure of modified Mod(2^n-1) adder [II]

This modified design offers low power and high speed because addition operation performed in parallel.

III. Simulation Results and Performance Analysis

The mod (2^n-1) adders are simulated using cadence Virtuoso and NC launch tools. These adders are designed in two different levels as schematic and RTL level.

(i) NC launch – Encounter Tool

The results are simulated in NC Launch simulation analysis environment standard 90nm Technology using cadence. The simulation results of mod (2^n-1) adders Fig.3 to Fig. 5 for n = 3 are shown in Fig. 6 to Fig. 8 respectively. The simulation result of mod m adder shows that the circuit provides correct output for sum less than or equal to m value and wrong output for sum greater than m value. The simulation result of mod (2^n-1) adder provides output to all cases except for both inputs as ‘111’. The simulation result of modified mod (2^n-1) adder provides output to all cases for both inputs as ‘111’ also.
The RTL schematic of mod \((2^n-1)\) adders Fig.3 to Fig. 5 for \(n = 3\) are shown in Fig. 9 to Fig. 11 respectively using NC launch encounter RTL compiler tool.
The schematic of mod \((2^n-1)\) adders Fig.3 to Fig. 5 for \(n = 3\) are shown in Fig. 12 to Fig. 14 respectively. The transient responses of mod \((2^n-1)\) adders Fig.3 to Fig. 5 for \(n = 3\) are shown in Fig. 15 to Fig. 17 respectively. The transient response of mod \(m\) adder shows that the circuit provides correct output for sum less than or equal to \(m\) value and wrong output for sum greater than \(m\) value. The transient response of mod \((2^n-1)\) adder provides output to all cases except for both inputs as ‘111’. The transient response of modified mod \((2^n-1)\) adder provides output to all cases for both inputs as ‘111’ also.
Figure 12. Schematic of mod m adder.

Figure 13. Schematic of mod \((2^n-1)\) adder.

Figure 14. Schematic of modified mod \((2^n-1)\) adder.
The schematic of 1-bit adder block [3] in mod adders is shown in Fig. 18. The operation of mod m, mod \(2^n-1\), and modified mod \(2^n-1\) adders are verified from their results for all cases.

Figure 15. Transient response of mod m adder.

Wrong result '111' case
Correct result sum \(\leq m\)
Wrong result sum > m

Figure 16. Transient response of mod \(2^n-1\) adder.

Wrong result '111' case

Figure 17. Transient response of modified mod \(2^n-1\) adder.
(iii) Performance Analysis

The performance of mod adders using cadence virtuoso generic 90nm CMOS technology & encounter tool standard 90nm are shown in Fig. 19 & Fig. 20.

Figure 19. Power of mod adders using cadence Encounter & virtuoso tools.

The power of mod adders using cadence Encounter & virtuoso tools are shown in Fig. 19. The Delay of mod adders using cadence Encounter & virtuoso tools are shown in Fig. 20. It is observed from Fig. 19 that the power of schematic approach is better than RTL approach but the delay is reduced in RTL design than schematic design from Fig. 20.
IV. Conclusion

In this paper, the mod adders are analyzed using cadence at both RTL and Schematic level. The schematic level approach has low power using virtuoso which is applicable to low power applications of RNS. The RTL level approach has high speed using Encounter tool which is applicable to high speed applications of RNS. These are used in the Forward converters, communication systems, image encryption and cryptography.

References

I. A.Omondi, B. PremKumar, “Residue Number System: Theory and Implementation”, Imperial College Press 2007, ISBN 978-1-86094-866-4.

II. B.Cao, C.H.Chang, T.Srikanthan, “A Residue-to-Binary Converter for a New Five-Moduli Set”, IEEE Trans. on Circuits and Systems-I: Regular Papers, 2007, Vol. 54, pp.1041-1049. doi:10.1109/TCSI.2007.890623.

III. Hamed Naseri and Somayeh Timarchi, “low-power and fast full adder by exploring New XOR and XNOR gates”, IEEE Transactions on very large scale integration systems, Aug. 2018, Vol. 26, no. 8, pp.1481-1493. doi:10.1109/TVLSI.2018.2820999.

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IV. N. S. Szabo, R.I. Tanaka, “Residue Arithmetic and its applications to computer technology”, New York: Mc-Graw Hill, 1967.

V. R. Zimmermann, “Efficient VLSI implementation of modulo addition and multiplication”, in proc. of IEEE Symposium on Computer Arithmetic, Apr. 1999, pp. 158-167. doi:10.1109/ARITH.1999.762841.

VI. Sharma, Neelam. "Analysis of Lactate Dehydrogenase & ATPase activity in fish, Gambusia affinis at different period of exposure to chlorpyrifos." International Journal 4.1 (2014): 98-100.

VII. S. Akhter, R. Gaurav, S. Khan “Analysis and Design of Residue Number System Based Building Blocks”, in proc. of 5th International Conference on signal processing and Integrated Networks, 2018, pp.441-445. doi:10.1109/SPIN.2018.8474204.

VIII. S. J. Piestrak, “A High speed Realization of a residue to binary number system converter”, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 1995, Vol. 42, pp. 661-663. doi:10.1109/82.471401.

IX. T. U. Narendra and et.al, “FPGA based efficient Architecture for conversion of binary to residue number system”, in proc.of Information Technology, Electronics and Mobile Communication conference, Oct 2017. doi:10.1109/IEMCON.2017.8117238.