High-Mobility Tri-Gate $\beta$-Ga$_2$O$_3$ MESFETs With a Power Figure of Merit Over 0.9 GW/cm$^2$

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Abstract—In this letter, fin-shape tri-gate $\beta$-Ga$_2$O$_3$ lateral MESFETs are demonstrated with a high power figure of merit (PFOM) of 0.95 GW/cm$^2$ — a record high for any $\beta$-Ga$_2$O$_3$ transistor to date. A low-temperature un-doped buffer-channel stack design is developed which demonstrates record high Hall and drift electron mobilities in doped $\beta$-Ga$_2$O$_3$ channels allowing for low ON resistances ($R_{ON}$) in $\beta$-Ga$_2$O$_3$ MESFETs. Fin-widths ($W_{fin}$) were 1.2-1.5 $\mu$m and there were 25 fins ($N_{fin}$) per device with a trench depth of $\sim$ 1 $\mu$m. A $\beta$-Ga$_2$O$_3$ MESFET with a source-drain length of 6.4 $\mu$m exhibits a high ON current (187 mA/mm), low $R_{ON}$ (20.5 $\Omega$.mm) and a high average breakdown field (4.2 MV/cm). All devices show very low reverse leakage until catastrophic breakdown for breakdown voltages ($V_{BR}$) scaling from 1.1kV to $\sim$3kV. This work demonstrates the potential of channel engineering in improving $\beta$-Ga$_2$O$_3$ device performance towards lower conduction losses for low-to-medium voltage applications.

Index Terms—Ga$_2$O$_3$, power device, MESFETs, finFETs, MOVPE, regrown contacts, breakdown, kilovolt, power figure of merit, passivation.

I. INTRODUCTION

ULTRA-WIDE bandgap (UWBG) $\beta$-Ga$_2$O$_3$ ($E_g$ = 4.6 - 4.9 eV) material and device technology is maturing rapidly and offers enormous opportunities for next-generation solid-state power switching with improved system-level size, weight, and power (SWaP) efficiency. $\beta$-Ga$_2$O$_3$ is the only UWBG semiconductor that offers the advantage of producing large area native bulk substrates from melt-grown techniques – offering potentially lowered costs for large-scale manufacturing at a much higher device yield and uniformity [1], [2]. Thanks to its compatibility with the established WBG process technology and single crystal growth using standard epitaxial techniques, $\beta$-Ga$_2$O$_3$ material and device performance has improved rapidly with lateral and vertical $\beta$-Ga$_2$O$_3$ devices demonstrating class-leading blocking voltages (up to 8kV) and breakdown field strengths ($> 5$ MV/cm) [3]–[10].

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Fig. 1. (a) 3D schematic of the tri-gate $\beta$-Ga$_2$O$_3$ MESFETs (with a SiNx wrap-around passivation not shown). (b) 2D cross-section schematic of the channel stack.

Although $\beta$-Ga$_2$O$_3$ devices have demonstrated tremendous performance advantages, its performance is still far from its projected intrinsic material limit. $\beta$-Ga$_2$O$_3$ transistors with high breakdown voltages and PFOMs have been realized which have focused mainly on electric field management techniques for improving average breakdown fields and device scaling for improving ON resistances [3], [5], [11]–[13]. However, less attention has been paid to doped channel design and engineering for improving electron mobility toward lowered device ON resistance [14]–[16]. In this letter, we demonstrate an improved channel stack design with low-temperature metalorganic vapor phase epitaxy (MOVPE) grown undoped buffer layers with record high Hall and drift electron mobilities in doped $\beta$-Ga$_2$O$_3$ channels. By fabricating fin-shape tri-gate $\beta$-Ga$_2$O$_3$ MESFETs, PFOM close to 1 GW/cm$^2$ and multi-kV breakdown voltages (over 2kV) are achieved simultaneously.

II. DEVICE GROWTH AND FABRICATION

For the channel design, a hybrid low temperature - high temperature (LT-HT) undoped buffer/doped channel epitaxial stack is grown using MOVPE. The (010) Fe-doped Ga$_2$O$_3$ substrates (NCT, Japan) were cleaned in HF (49%) for 30 mins prior to channel growth [17]. The epitaxial structure was grown using an Agnitron Agilis MOVPE reactor with TEGa, O$_2$ and silane (SiH$_4$) as precursors and argon as carrier gas. An LT (600°C) undoped Ga$_2$O$_3$ buffer (330 nm thick) is grown followed by transition layers to a HT (810°C) Si-doped Ga$_2$O$_3$ channel layers (~200 nm) without growth interruption [18].

Fin-shape MESFETs were fabricated with a channel stack whose Hall mobility, sheet charge (electron density) and $R_{sh}$ were 168 cm$^2$/Vs, $5.8 \times 10^{12}$ cm$^{-2}$ ($\sim 3 \times 10^{17}$ cm$^{-3}$), and 6.4 k$\Omega$.mm, respectively. The channel stack cross-section schematic is shown in Figure 1(b). Fin-shape channels with length ($L_{fin}$) that run from the source to the drain ($L_{fin} \sim L_{SD}$) were formed using Ni/SiO$_2$ mask pattern and SF$_5$-Ar ICP-RIE dry etch with trench depths $\sim 1$ $\mu$m (3D schematic shown in Figure 1(a)) [19]. After the dry etching.
step, wet acid treatments using room temperature diluted HCl (20 mins) and diluted HF (10 mins) were used for dry-etch-induced surface damage recovery. Planar LT-MOVPE regrown ohmic contacts were employed [12]. The estimated electron concentration in the regrown contact layer is around $n \sim 1.4 \times 10^{19}$ cm$^{-3}$. Ti/Au/Ni (20/150/50 nm) ohmic metal was evaporated on the regrown contacts and annealed at 450$^\circ$C for 1.5 mins in N$_2$ ambient [12]. Ni/Au/Ni (30/100/30 nm) gates were evaporated to form the Schottky gates. The whole device was passivated using a $\sim$250 nm PECVD (300$^\circ$C) deposited SiN$_x$ dielectric. Lateral device dimensions were verified by SEM. Fin-widths ($W_{\text{fin}}$) were 1.2-1.5 $\mu$m, trench widths were $\sim$5.3 $\mu$m and there were 25 fins ($N_{\text{fin}}$) per device. The $L_{\text{GS}}$ and $L_{\text{G}}$ were fixed at 2.4 $\mu$m and 1.3 $\mu$m and the $L_{\text{GD}}$ was varied from 2.7 to 16.7 $\mu$m on the same wafer. Concentric Schottky gate CV pads (220 $\mu$m diameter) and fatFETs structures were also fabricated on the same MESFET sample.

III. RESULTS AND DISCUSSIONS

From room temperature (RT) Hall measurements, this stack design is shown to have an effective RT Hall mobility value in the range 162 – 184 cm$^2$/V$s$ for doped channel electron densities of 1.5 – 3.5 $\times$ 10$^{17}$ cm$^{-3}$ measured on multiple samples/substrates. It is hypothesized that the enhanced mobility could be due to lower Fe riding into the channel from the substrate due to the lower growth temperature of the buffer as well as the absence of any low-mobility parasitic channel near the substrate [25], [26]. Further details and characterization of this stack design will be reported elsewhere. These Hall mobility values are record high for any doped Ga$_2$O$_3$ channel to date as it is compared with the state-of-the-art values reported utilizing various growth techniques in Figure 2(a).

Charge profile of the MESFET channel extracted from capacitance-voltage measurement is shown in Figure 2(b). It shows that the buffer is completely depleted and there is no active parasitic channel at the epilayer-substrate interface. These further supports ascribing the measured Hall and drift mobility to only the doped channel layer. The channel mobility of the MESFET was characterized using fatFET devices ($L_G \sim 103$ $\mu$m, $L_{\text{GS}}/L_{\text{GD}} \sim 1$ $\mu$m) in the linear region of the device operation. Under a low drain bias ($V_{\text{DS}} = 0.1$ V), the field-effect mobility $\mu_{\text{FE}}$ can be related to the transconductance as, $\mu_{\text{FE}} = (g_m \times L_G)/(C_G \times V_{\text{DS}})$ where $g_m$, $L_G$, $C_G$, $V_{\text{DS}}$ are the transconductance, gate length, gate-to-channel capacitance and applied drain bias respectively. Figure 2(c) shows the room-temperature depth profile of the extracted $\mu_{\text{FE}}$ in the doped channel. The $\mu_{\text{FE}}$ showed an average value of $\sim$125 cm$^2$/V$s$ with a peak value of 132 cm$^2$/V$s$ which is the highest electron drift mobility value ever reported in a uniformly doped β-Ga$_2$O$_3$ channels.

Figure 3(a) and 3(b) shows the DC output and transfer curves for the fin-shape MESFET with dimensions $L_{\text{GS}}/L_{\text{G}}/L_{\text{GD}} = 2.4/1.3/2.7$ $\mu$m. The ON current and resistance were normalized to the device width ($W_{\text{fin}} \times N_{\text{fin}}$). The devices show clear current saturation and low saturation voltages ($V_{\text{DS, Sat}}$). The maximum ON current measured was 187 mA/mm. The ON resistance ($R_{\text{ON}}$) extracted from the linear region of the output curve was found to be 20.5 $\Omega$.mm. From TLM measurements, the total $R_C$ (contact resistance) to the channel was extracted to be 1.0 $\pm$ 0.2 $\Omega$.mm ($\leq$ 5% of the total device $R_{\text{ON}}$). The devices show sharp pinch off with low sub threshold swing (156 mV/dec) and threshold voltage of $\sim$10 V. From the transfer curves, the devices show low leakage ($\sim$10$^{-11}$A/mm) and high $I_{\text{ON}}/I_{\text{OFF}}$ ratio $\sim$10$^4$. The transistors also exhibit very low gate leakage and high transconductance peak of 12.6 mS/mm. The hysteresis effects seem to be minimal as shown in Figure 3(c) and 3(d) dual sweep I-V curves. These devices exhibit a negligible hysteresis of $AV \sim 0.06$ V. Dynamic performance characterization is required in the future to ascertain any deleterious effect of low temperature buffers and any resultant charge trapping.

Figure 3(e) shows the three-terminal breakdown characteristics (at $V_{\text{GS}} = –35$V) of the MESFETs with various $L_{\text{GD}}$ values. All the breakdown measurements were performed with
the wafer submerged in FC-40 Fluorinert dielectric liquid. The device breakdown was catastrophic (destructive) with negligible reverse leakage until the breakdown occurred. The reverse leakage during the breakdown measurements were limited by the measurement tool (Keysight B1505 with 3kV HV SMU). It is seen in Figure 3(c) that the $V_{BR} = (V_{DS} - V_{GS})$ scaled from 1.1kV to ~3kV as the $L_{GD}$ was scaled from 2.7 to 16.7 $\mu$m.

From the cross-section (xz-plane Figure 4(a,b)) of the 3D TCAD simulated structure (with $L_{GD} = 3 \mu m$, and $V_{DS} = 1130V$) at the gate edge towards drain, it is shown that the peak fields are at the center of the top gate and gate metal corners in the etched region. Hence, in the presence of the UID cap layer and deeper trenches, peak fields are present in the UID cap region and the insulating substrate. When this design is compared with a planar gate structure (Figure 4(d)), the tri-gate exhibits lower peak field at the gate edge (without the need for field plates), improving the $E_{AVG}$ values in the drift region dramatically.

Figure 5(a) shows the variation of $V_{BR}$ and the effective average field ($E_{AVG} = V_{BR}/L_{GD}$) as a function of $L_{GD}$. The maximum $E_{AVG}$ achieved was ~4.2 MV/cm for the smallest device with $L_{GD}$ of 2.7 $\mu$m ($V_{BR} = 1.13$ kV). This is the highest reported average breakdown field for $L_{GD} > 2 \mu m$ [3, 27]. The $E_{AVG}$ decreased monotonously as the $V_{BR}$ increased with increasing $L_{GD}$. For a $V_{BR}$ of ~3 kV and $L_{GD}$ of 16.7 $\mu$m, the $E_{AVG}$ is 1.8 MV/cm. Since this is the first report of LT MOVPE-grown buffers in $\beta$-Ga$_2$O$_3$ devices, further study combining field plates and buffer breakdown structures will be necessary to elucidate on factors limiting the breakdown performance in these devices, especially at higher $L_{GD}$. Nevertheless, the high ON currents (low $R_{ON}$), the high $V_{BR}$, $E_{AVG}$ and low reverse leakage behavior simultaneously demonstrated in these first-generation LT-buffer devices are a significant improvement over the state-of-the-art $\beta$-Ga$_2$O$_3$-based transistors.

Since these devices utilized fin lengths running from source to drain, an effective channel area of $(L_{SD} + 2L_T) \times W_{fin} \times N_{fin}$ was used to normalize the ON resistance. $L_T$, the transfer length, is extracted from TLM structures to be 0.2 $\mu$m. The PFOM values for fin-shape MESFETs are plotted as a function of $L_{GD}$ (Figure 5(b)). The highest PFOM of 0.95 GW/cm$^2$ was calculated for MESFETs with $L_{GD}$ of 2.8 $\mu$m and 7.7 $\mu$m which had $V_{BR}$ of 1.1 kV and 2.2 kV, respectively. The PFOM of the devices with $L_{GD}$ of 12.2 $\mu$m and 16.7 $\mu$m were 0.65 GW/cm$^2$ ($V_{BR} = 2.8kV$) and 0.44 GW/cm$^2$ ($V_{BR} = 3kV$). The PFOM of the large $L_{GD}$ devices were a bit lower due to lower $E_{AVG}$ values compared to the small $L_{GD}$ devices, as discussed earlier. Nevertheless, the PFOM reported for >2 kV devices are still the highest reported values. Figure 5(c) benchmarks the PFOM values of the fin-shape MESFETs with the existing literature reports. It is compared with state-of-the-art $\beta$-Ga$_2$O$_3$-based transistors that include advanced designs like Ga$_2$O$_3$ MOSFETs, AlGa$_2$O$_3$/Ga$_2$O$_3$ HFETs and p-n hetero-junction $\beta$-Ga$_2$O$_3$ FETs. It shows the reported PFOM of 0.95 GW/cm$^2$ is a record high for any $\beta$-Ga$_2$O$_3$ transistor to date. Further improvement can be expected by implementing E-field management techniques like field-plates, planar access regions, gate dielectrics with high breakdown field strengths, higher channel charge, higher channel mobility and lowering reverse leakage simultaneously.

### IV. Conclusion

We demonstrate over 0.9 GW/cm$^2$ PFOM in multi-kV fin-shape $\beta$-Ga$_2$O$_3$ lateral MESFETs – a record high for any $\beta$-Ga$_2$O$_3$ transistor to date. An LT-HT buffer-channel stack is demonstrated using MOVPE with record high RT Hall and drift mobilities in doped $\beta$-Ga$_2$O$_3$ channels. Using trigates, $\beta$-Ga$_2$O$_3$ MESFETs with high ON currents, negligible hysteresis effects and low ON resistances are realized with very low reverse leakage and $V_{BR}$ values of 1.1kV to ~3 kV. These devices show great potential of high-performance $\beta$-Ga$_2$O$_3$ FETs for future power device applications in the low to medium voltage range.

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