TRAINING DNN IoT APPLICATIONS FOR DEPLOYMENT ON ANALOG NVM CROSSBARS

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ABSTRACT

Deep Neural Networks (DNN) applications are increasingly being deployed in always-on IoT devices. However, the limited resources in tiny microcontroller units (MCUs) limit the deployment of the required Machine Learning (ML) models. Therefore, alternatives to traditional architectures such as Computation-In-Memory based on resistive nonvolatile memories (NVM), promising high integration density, low power consumption and massively-parallel computation capabilities, are under study. However, these technologies are still immature and suffer from intrinsic analog nature problems—noise, non-linearities, inability to represent negative values, and limited-precision per device. Consequently, mapping DNNs to NVM crossbars requires the full-custom design of each one of the DNN layers, involving finely tuned blocks such as ADC/DACs or current subtractors/adders, and thus limiting the chip reconfigurability. This paper presents an NVM-aware framework to efficiently train and map the DNN to the NVM hardware. We propose the first method that trains the NN weights while ensuring uniformity across layer weights/activations, improving HW blocks re-usability. Firstly, this quantization algorithm obtains uniform scaling across the DNN layers independently of their characteristics, removing the need of per-layer full-custom design while reducing the peripheral HW. Secondly, for certain applications we make use of Network Architecture Search, to avoid using negative weights. Unipolar weight matrices translate into simpler analog periphery and lead to 67% area improvement and up to 40% power reduction. We validate our idea with CIFAR10 and HAR applications by mapping to crossbars using 4-bit and 2-bit devices. Up to 92.91% accuracy (95% floating-point) can be achieved using 2-bit only-positive weights for HAR.

1 INTRODUCTION

The number of applications relying on Machine Learning (ML) has significantly increased, spurred by two main reasons. Firstly, the amount of data available to be processed has exponentially grown, enabling and data scientist to extract the knowledge behind previously obscured data correlations (Bates et al., 2017). And secondly, current hardware such as GPUs, FPGAs and TPUs, is now able to accelerate the computationally costly Deep Neural Networks (DNNs) algorithms behind the most recent ML breakthroughs (Bates et al., 2017). However, it is the dimensions of this data and the intrinsic flows of the algorithm that make ML applications suffer from the well known data movement problem (Zidan et al., 2018). Moreover, given the exponential grow of the number of devices deployed within Internet of Things (IoT), and more importantly their limited computational capabilities, the efficient deployment of DNNs performing inference at the edge has become a major issue (Kodali et al., 2017; Xu et al., 2018; Whatmough et al., 2019; Fedorov et al.; Chen et al., 2017; 2018). Whether targeting video, image processing or a bio-signal recognition, always-ON inference at the very edge always faces three main problems: limitations on the size of the deployed DNN, the computational load of the algorithm, and the energy consumed in the process. The trade-off between model size, performance and energy consumption leads to algorithm—pruning, quantization (Kodali et al., 2017; Fedorov et al.), system—digital accelerators, vectorized instructions (Zhang et al., 2017; Kodali et al., 2017; Whatmough et al., 2019), and technology solutions. (Hasan et al., 2017; Cai et al., 2019). Computation In Memory (CIM) architectures drastically reduce the number of required data movements (Zidan et al., 2018; Hamdioui et al., 2019), while also taking advantage of the quantization and pruning solutions. Emerging resistive switching technologies such as Phase-Change Memory (PCM) and memristors or Resistive Random Access Memories (RRAM) behaves as analog synapses placed in crossbar arrays (Li et al., 2018b; Rahimi et al., 2017; Ambrogio et al., 2018; Serb et al., 2018; Hamdioui et al., 2019; Joshi et al., 2019). The resistive crossbar computes in parallel vector-matrix multiplications, achieving considerable speedups.
Moreover, as the weights are encoded in the non-volatile resistive elements and not moved from an external memory, energy consumed due to data movement gets massively reduced. This leads to orders of magnitude potential improvement regarding energy and computing efficiency. As seen in the Figure 1, for applications based on low precision MACs (using low precision ADCs), NVM crossbars provide the lowest power consumption, meeting edge-ML energy hard limitations.

However, to fully integrate the processing units and the memory in the same physical location, several technological challenges need to be overcome. Mapping DNNs to crossbars supported by CMOS periphery requires the full-custom design of each one of the algorithm layers, involving finely tuned blocks such as ADC/DACs or current subtract blocks. These problems hinder the applicability of reconfigurable analog accelerators (Serb et al., 2018), and create a huge gap between laboratory prototypes, relying on external probes and analyzers (Li et al., 2018b; Ambrogio et al., 2018; Li et al., 2018a), and market products. Moreover, in order to take advantage of CIM energy/area benefits, architecture related limitations, such as the inability to directly encode negative weights into the NVM crossbar, need to be addressed (Li et al., 2018b; Joshi et al., 2019).

In this work we introduce a framework to train and efficiently map the DNN to the NVM hardware, providing two main contributions. Firstly, our methodology reduces the area and power consumption related to the NVM crossbars and surrounding periphery. Second, we enable the re-use smaller, less power-hungry, uniform HW modules across different layers in the DNN. Therefore area and power benefits come together with shorter design time, while closing the gap between reconfigurable blocks (Li et al., 2018b; Serb et al., 2018) and real reconfigurable solutions.

The NVM-aware training obtains uniform scaling through the layers independently of their morphology and size. Thus it removes the need of per-layer full-custom design, and reduces the peripheral HW. Secondly, for certain applications DNN can be mapped to unipolar weight matrices, removing additional periphery and reducing the total area by $2 \times$.

Figure 1. Energy comparison between a digital MAC accelerator, a crossbar and a sub-threshold Cortex-M0+, describing the energy consumed by each architecture during the computation of an $N \times N$ 4-bit vector-matrix multiplication operation (Myers et al., 2017).

The paper is structured as follows. Section 2 deepens into the motivation behind the presented work. Section 3 describes the proposed methodology and framework, followed by the related results on Section 4. Finally, some conclusions are drawn.

## 2 Related Work

### 2.1 NVM Crossbars as MAC Engines

Machine Learning applications, and more specifically DNN, heavily rely on vector-matrix multiplication operations – also called multiplication-accumulation or MACs. Being MAC a very basic but high cost operation, the implementation of an analog, low power, massively-parallel MACs acceleration block is highly desired. Resistive crossbars composed of NVM elements –PCM, RRAM, MRAM– can immediately compute MAC in constant time with a very promising energy efficiency (Rahimi et al., 2017; Ambrogio et al., 2018; Hamdioui et al., 2019; Joshi et al., 2019).

Two key mechanisms are behind the massively parallel multiplications and additions. Firstly, the conductance of a resistive switching NVM element can be programmed to a discrete conductance $g$ within a known range $g \in [g_{ON}, g_{OFF}]$. This allows to encode one of the multiplication operands (the weight) as a conductance. Should the second operand be encoded as a voltage $v$, the current flowing through the device would be the multiplication of both operands $i = vg$.

Secondly, the crossbar architecture automatically compute the addition of the individual dot-products. As depicted in Figure 2, the set of accurately programmed conductances in the NVM devices conforms the matrix $G = \{g_{ab}\}, a = [1, N], b = [1, M]$. If we encode our input vector as voltages $V = \{v_a\}$, the current flowing through each one of the bitlines $I = \{i_b\}$ corresponds to the accumulation of the partial products $i_b = \sum_{a=1}^{N} v_a g_{ab}$.

Figure 2. Basic NVM accelerator architecture and principle behind the NVM based vector-matrix multiplication. Inputs are encoded as voltages, and enter the crossbar through the horizontal row lines. Bitline currents naturally accumulate the individual products of the input voltages and the NVM conductances and later digitized. In very deep NN crossbars are interconnected digitally.
2.2 NVM Technology Level Challenges

To provide the reader with a better perspective on resistive switching NVMs, but outside of the scope of this work, here we summarize the three key technology challenges faced by these devices (Garcia-Redondo & Lopez-Vallejo, 2017):

- Limited endurance after many writes is one of the main problems that remains unsolved. Though in-crossbar training methods have been proposed (Ambrogio et al., 2018), their applicability to real products is still unclear due to this reduced lifetime. However, always-on inference applications, performing only analog read operations, would not suffer from this problem.
- Variability and crossbar-related errors heavily affect RRAM-CMOS hybrid circuits. Nevertheless architectures as DNNs are naturally robust against the noise that these problems may cause. More over, this defects can be taken into account at training time, getting around device faults (Hasan et al., 2017).
- NVM elements suffer from non-linearities that lead to errors during the weight-to-conductance mapping. However, by engineering the physical device (Woo & Yu, 2019) this problem can be overcome.

As seen, technology problems related to inference ML accelerators built with NVM technologies can be overcome. Next section describes the challenges specific to the deployment of ML algorithms in NVM crossbars.

2.3 NVM For Analog ML Accelerators: Circuit Design Challenges And Opportunity

For both digital and emerging analog accelerator approaches, the precision of the operands and operations involved in the DNN determines the accuracy, latency and energy consumption of the inference operation. In particular, for CIM architectures the precision of the DACs and ADCs involved in the operation computation greatly influences the total area and power consumption (Ni et al., 2017; Xia et al., 2016). Consequently, the quantization of both weights and activations is critical on the design of the accelerated system.

Though 6-bit and 8-bit NVM devices have been demonstrated (Li et al., 2018b), and depending on the technology, variability or analog noise may compromise the encoding of more than 2 to 4 bits per cell, and thus limiting the precision of the analog multiplication. On the other hand, the current accumulation taking place on the column bit-line, taking place in the analog domain, does not suffer from precision related problems. It is later, once the MAC output requires to be converted to the digital domain, that the ADC precision introduces the quantization error. The selection of the DAC/ADC precision (or the design/use of multiple DACs/ADCs exhibiting different bits) is critical for the system efficiency, as it states as the main factor behind the total area and power consumption. Consequently, lower-precision periphery is desired (Li et al., 2018b; Ni et al., 2017; Xia et al., 2016).

Figure 3. Common problems on the deployment of NN layers in NVM crossbars: Scaling issues on a) convolutional layers and b) fully connected layers are often solved using full-custom periphery, while the handling of c) negative weights area and power overcosts.
But precision is not the only concern regarding the periphery design. Figure 3 describes how NN layers are deployed in an NVM crossbar. Convolution kernels are decomposed by channels, and mapped to different columns. Then, the kernels are unrolled and repeated to compute in parallel the convolution operation. However, non-uniform scaling across DNN layers imposes full-custom blocks per stage – Figure 3 a) and b). The number of elements in a layer, and the range of considered inputs, weights and activations, determine the currents flowing through the bitlines. Different voltage or current signals require per-layer full-custom periphery. For positive and negative weights representation – Figure c) (Li et al., 2018b; Joshi et al., 2019) – the number of NVM elements is duplicated, and additional subtractors are required. This problem is in detail described in Section 3.3.

To the best of our knowledge, every offline learning work present in the literature that trains the DNN externally to the NVM crossbar dynamically scale each DNN layer to the available set of conductances in which we can program the device (Hu et al., 2016). This process is independent of the input, weight and activation value ranges of the layers. As we are dealing with real voltage/current signals, this complicates the underlying HW periphery, and limits the system reconconfigurability: though the crossbar weights can be reprogrammed, the full-custom periphery constraints the deployment of different NN graphs to only one. Consider the deployment of two different fully connected layers, A and B of a NN described in Figure 3 b). The number of inputs \(n(A)\) and neurons \(n(B)\) differs from those in layer B. Similarly, their ranges \([x_{A0}, x_{A1}], [y_{A0}, y_{A1}]\) will differ from the respective ones in layer B. And more importantly, the weight matrices \(W_A\) and \(W_B\) differ on their ranges \([w_{A0}, w_{A1}], [w_{B0}, w_{B1}]\). However, both matrices \(W_A\) and \(W_B\) need to be mapped (Hu et al., 2016) to the same available set of conductances the devices can be programmed in, \(G\). If across layers the \(i-th\) weight matrix requires to be translated to the conductances range \([g_{0}, g_{1}]\), the periphery generating the required voltage amplitudes \(v_{ith}\) and sensing the output currents \(i_{ith}\) needs to be scaled accordingly, and therefore be different. Full-custom blocks require higher design time (Giordano et al., 2019), and limits the deployment of different NN in the same HW. Moreover, should the NN weights be updated varying voltage/current ranges, DACs/ADCs would require additional calibration processes.

To take fully advantage of the crossbar, the deployment of convolutional layers requires mapping different filters of the same layer to different columns in the tile. As described in Figure 3 a), per-channel quantization methods (Krishnamoorthi, 2018) lead to different weight/activation ranges. As voltage inputs and ADC elements are shared across the filters, analog and digital scaling stages would be required. Different ADC designs leads to additional area, power consumption, and higher design times (Giordano et al., 2019).

2.3.1 Challenges Related To Weights Polarity

The conductance in a passive NVM element can only be a positive number \(g\) in the range \([g_{OFF}, g_{ON}]\). However, the NN weights, no matter whether \(W \in \mathbb{R}\) or \(W \in \mathbb{Z}\), contain both positive and negative values. Consequently, the use of positive and negative weights involves a problem when mapping to a conductance set with only positive values. To work around this issue, traditionally positive and negative weights are deployed separately in different areas of the crossbar. As depicted in Figure 3 c), using this scheme, we double the crossbar area as per-weight, one column computes the positive contributions, while the other column the negative ones (Li et al., 2018b; Joshi et al., 2019; Cai et al., 2019). Moreover, additional current subtraction blocks are required before the ADC stages (Joshi et al., 2019; Cai et al., 2019).

Alternative solutions as (Hu et al., 2016) shifting the weight matrices usually involve the use of biases dependent on the inputs, and they require additional periphery. Nevertheless, both alternatives involve considerable area&energy overheads.

2.3.2 NN Quantization

As described, precision greatly affects the system characteristics, and thus quantization is actively studied.

Relative to the stage, we identify schemes for quantizing at inference-time, training and post-training (re-train for a short number of steps an already pre-trained floating point NN). Both the characteristics of the NN and desired precision determine the stage at which apply the quantization, and, in some cases, how gradual the quantization stage is (Zhou et al., 2017; Krishnamoorthi, 2018; Baskin et al., 2018; Liu & Mattina, 2019). Focusing on at the tensor quantization itself, different methods as uniform affine, uniform symmetric, stochastic or non-uniform methods can be applied (Louizos et al., 2017; Krishnamoorthi, 2018). In particular, non-uniform quantization methods using Network Architecture Search (NAS) are gaining more attention (Ulichich et al., 2019; Wu et al., 2018). Looking the training quantization graph definition, alternative methods
can be implemented. Figure 4 presents a simplified training graph implementing straight through estimator (STE). While in forward passes (FP) both weights and activations are quantized, the computation of the new weights using the computed gradient during back propagation (BP) stages may or may not use the quantization blocks. STE schemes like the one used in TensorFlow, introduced by Google in Krishnamoorthi (2018), use standard floating point ops to compute the gradient on the BP. On the other hand, schemes like UNIQ (Baskin et al., 2018) or IBM’s (McKinstry et al., 2018) introduce noise on the gradient computation. Finally, alternatives as alpha blending (Liu & Mattina, 2019) proposes different operations in the graph computing quantized and non-quantized paths.

2.3.3 Status of NVM-based Reconfigurable Accelerators

A naive deployment of a particular algorithm into a given crossbar with specific characteristics require the periphery surrounding it to be full-custom designed. Therefore, despite many efforts have been devoted to design NVM based accelerators, most works presented in literature describing different NN experiments rely on HW external to the chip to assist the crossbar as supporting periphery (Hu et al., 2016; Ambrogio et al., 2018; Li et al., 2018a; Joshi et al., 2019).

To solve the issue, the first fully reconfigurable CMOS-NVM processor includes an scaling stage in the form of per-column current dividers, interfacing the ADCs before the conversion takes place (Cai et al., 2019). While maintaining reconfigurability, the system is penalized in terms of area and power consumption. Additionally, the system includes high-precision DACs/ADCs, incurring in noticeable area and power penalties.

3 HARD-CONSTRAINED UNIFORM HW QUANTIZED TRAINING

To address the reconfigurability versus full-custom periphery design, and its dependence on the weights/activation precision, we have developed a framework to aid mapping the DNN to the NVM hardware at training time. The main idea behind it is the use of hard-constrains when computing forward and back-propagation passes. These constraints, related to the HW capabilities, impose the precision used on the quantization of each layer, but more importantly, guarantee that the weight, bias and activation values that each layer can have are shared across layers in the NN. This methodology allows, after the training is finished, to map each hidden layer \( L_i \) to uniform HW blocks sharing:

- a single ADC design performing \( \text{act}() \)
- a single DAC design performing \( \mathcal{V}() \)
- a single weight mapping function \( f() \)
- a global set of activation values \( Y_g = [y_0, y_1] \)

![Figure 5. Simplified version of the proposed quantized graph for crossbar-aware training. We define a control that automatically handles the global variables involve in the quantization process, achieving uniform quantized weight and activation values across layers.](image)

In most cases, but more commonly in classification problems the output layer activation (sigmoid, softmax) does not match the hidden layers activation. Therefore for the DNN to learn the output layer should be quantized using an independent set of values \( Y_o, X_o, W_o, B_o \) that may or not match \( Y_g, X_g, W_g, B_g \). Consequently, the output layer is the only layer that once mapped to the crossbar requires full-custom periphery.

3.1 HW Aware Graph Definition

The NN graphs are generated by Tensorflow Keras libraries. In order to perform the HW-aware training, elements con-
trolling the quantization, accumulation clippings, and additional losses (should additional objectives be introduced in the problem, as defined in Section 3.3), are added to the graph. Figure 5 describes these additional elements, denoted as global variables controlled by global variable control operations. The global variable control blocks present in the training graph manage the definition, updating and later propagation of the global variables. A global variable is a variable used to compute a global set of values $V_g$ composed of the previously introduced $Y_g, X_g, W_g, B_g$ or others. Custom regularizer blocks may also be added to help the training to converge when additional objectives are present.

3.2 HW Aware NN Training

3.2.1 Differentiable Architecture and Variables Updating During Training

Each global variable can be non-updated during training, fixing the value of the corresponding global set in $V_g$ or dynamically controlled using the related global variable control. If fixed, a design space exploration is required in order to find the best set of global variable hyperparameters for the given problem. On the contrary, we propose the use of a Differentiable Architecture (DA) (Liu et al., 2018) to automatically find the best set of global variable values using the back-propagation. We propose defining the global variables as a function of each layer characteristics—mean, max, min, deviations, etc. If complying with DA requirements, the global control elements automatically update the related variables descending through the gradient computed in the back-propagation stage. On the contrary, should a specific variable update not be directly computable by the gradient descent, it be updated in a later step as depicted in algorithm 1.

We also propose the use of DA on the definition of inference networks that target extremely low precision layers (i.e. 2 bit weights and 2–4 bits in activations), to explore the design space, and to find the most suitable activation functions to be shared across the network hidden layers. Algorithm 2 describes the particularization of Algorithm 1 for one of the experiments gathered in Section 4. In this example we explore the use (globally, in every hidden layer) of a traditional relu versus a customized tanh defined as $tanh(x - th_g)$. Our NN training is able to choose the most appropriate activation, as well as to find the optimal parameter $th_g$. The parameter $th_g$ is automatically computed through gradient descent. However, to determine which kind of activation to use, we first define the continuous activations design space as

$$act(x) = a_0 relu(x) + a_1 \tanh(x - th_g),$$  \hspace{1cm} (9)**

where $\{a_0, a_1\} = A_g$. The selected activation $a_s$ is obtained after applying softmax function on $A_g$:

$$a_s = softmax(A_g),$$  \hspace{1cm} (10)**

which forces either $a_0$ or $a_1$ to a 0 value once the training converges (Liu et al., 2018).

3.2.2 Loss Definition

As introduced before, our proposed training scheme considers additional constraints to a traditional NN training, which may lead to non-convergence issues should additional objectives related to the final HW characteristics be introduced (see Section 3.3). In order to help the convergence towards a valid solution, we introduce additional penalization terms in the loss computation that may depend on the training step. The final loss $L_F$ is then defined as

$$L_F = L + L_{L2} + L_{L1} + L_C,$$  \hspace{1cm} (11)**

where $L$ refers the standard training loss, $\{L_{L1}, L_{L2}\}$ refer the standard L1 and L2 regularization losses, and $L_C$ is the custom penalization. An example of this particular regularization terms may refer the penalization of weight

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Algorithm 1 Quantized Training aided by Differentiable Architecture Search (Liu et al., 2018)

**Input:** Set of global variables $V_g = \{X_g, Y_g, W_g, B_g\}$

Initialize $V_g$

while not converged do

  Update weights $W$
  Compute non-differentiable vars in $V_g$
  Update layer quantization parameters

end while

Algorithm 2 Algorithm used in Section 4

**Input:** Set of global variables $V_g = \{X_g, Y_g, W_g, B_g, Th_g, A_g\}$

init $\{x_0, x_1\} = \{\min(X), \max(X)\}$

init $\{y_0, y_1\} = \{\min(Y), \max(Y)\}$

init $\{w_0, w_1\} = \{\min(W), \max(W)\}$

init $\{b_0, b_1\} = \{\min(B), \max(B)\}$

init $\{th_g\} = \{\text{random}_\text{val}\}$

init $\{a_i\} = \{\text{random}_\text{val}\}$

while not converged do

  Update weights $W$ using gradient descent
  Compute vars in $V_g$

  $\{x_0, x_1\} = \{\text{EMA}(\min(X)), \text{EMA}(\max(X))\}$
  $\{y_0, y_1\} = \{\text{EMA}(\min(Y)), \text{EMA}(\max(Y))\}$
  $\{w_0, w_1\} = \{\min(W), \max(W)\}$
  $\{b_0, b_1\} = \{\min(B), \max(B)\}$

  Update layer quantization parameters with $V_g$

end while
values beyond a threshold $W_T$ after training step $N$. This loss term can be formulated as

$$\mathcal{L}_C = \alpha_C \sum_{W} \max(W - W_T, 0) HV(\text{step} - N) \quad (12)$$

where $\alpha_C$ is a preset constant and $HV$ the Heaviside function. If the training would still provide weights whose values surpass $W_T$, $HV$ function can be substituted by a non-clipped function $\text{relu}(\text{step} - N)$. In particular, this $\mathcal{L}_C$ function was used in some of the experiments located at Section 4.

### 3.2.3 Implemented Quantization Scheme

The implemented quantization stage takes as input a random tensor $T = \{t_i\}, t_i \in \mathbb{R}$ and projects it to the quantized space $Q = \{q_0, q_-\}$, where $q_0 = \alpha Q^{2^q}$, $q_- = -\alpha Q^{2^q}$, and $\alpha \in \mathbb{R}$. Therefore the projection is denoted as $q(T) = T_q$, where $T_q = \{t_q\}, t_q \in Q$. For its implementation we use fake_quant operations (Krishnamoorthi, 2018) computing straight through estimator as the quantization scheme, which provides us with the uniformly distributed $Q$ set, which always includes 0. However, the quantization nodes shown in Figure 5 allow the uses of non-uniform quantization schemes. The definition of the quantized space $Q$ gets determined by the minimum and maximum values given by the global variables $V_g$.

Though the Algorithm 2 consider the max/min functions, stochastic quantization schemes can be considered (Louizos et al., 2017; Krishnamoorthi, 2018). Similarly, the quantization stage is dynamically activated/deactivated using a global variable varying within the discrete values $[0, 1]$, with could be easily substituted to support incremental approaches (Zhou et al., 2017). In particular, and as shown in Section 3.3, the use of alpha-blending scheme (Liu & Mattina, 2019) proves very when the weight precision is very limited.

### 3.3 Unipolar Weight Matrices Quantized Training

Mapping positive/negative weights to the same crossbar involve double the crossbar resources and introducing additional periphery. By using the proposed training scheme we can restrict further the characteristics of the DNN graph obtaining unipolar weight matrices, redefining some global variables as

$$W_g \in [0, w_1] \quad (13)$$

and introducing the $\mathcal{L}_C$ function defined by Equation 12.

Moreover, for certain activations (relu, tanh, etc.) the maximum and/or minimum values are already known, and so the sets of parameters in $V_g$ can be constraint even further. These maximum and minimum values can easily be mapped to a specific parameters in the activation function circuit interfacing the crossbar (Giordano et al., 2019). Finally, in cases where weights precision is very limited (i.e. 2 bits), additional loss terms as $\mathcal{L}_C$ gradually move weight distributions from a bipolar space to an only positive space, helping the training to converge.

In summary, by applying the mechanisms described in Section 3, we open the possibility of obtaining NN graphs only containing unipolar weights.

### 4 Experiments and Results

We have evaluated the presented methodology using CIFAR10 and Human Activity Recognition (HAR) applications. CIFAR10 (Krizhevsky, 2009) comprises the classification of 32x32 sized images into 10 different categories. HAR classifies among incoming data from different sensors (accelerometer, gyroscope, magnetometer, 3 channels each) into 12 different activities (run, jump, walk, etc.) To mimic the case of a smartwatch we used real data from sensors placed in only one limb from (Banos et al., 2014) dataset.

Figure 6 describes the architectures used in each case: CIFAR10 problem represents a good example of always-ON medium sized DNNs, including multiple convolutional layers and $310K$ parameters. HAR NN interfaces 9 input channels, with a time-series data input of 100 samples each, followed by 2 fully connected layers with a total of $133K$ parameters.

### 4.1 Hyperparameters Influence On The Proposed Scheme

Quantization related hyperparameters (Krishnamoorthi, 2018; McKinstry et al., 2018) involving global or individual layer precision, learning rate or the moment in which we change from floating point to quantized operations during training (quant_delay) greatly influence the final accuracy. Figure 7 describes how the accuracy of a simple NN quantized with 4-bit activations and 2b-weights varies influenced by the learning rate schedule and quant_delay. Traditionally for high-precision NN (Zhang et al., 2017) late quantization was recommended, but in the figure we can appreciate how if the quantization occurs to late and at lower precisions,
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Figure 7. Learning rate and quant delay effects on the proposed training process. HAR NN was quantized with 2-bit for weights and 4-bit for activations.

On the other hand, we also can see how using the proposed approach, quantization global variables \( w_0 \) and \( w_1 \) adapt to the training conditions, helping the system learn while uniforming the layers.

4.2 Accuracy vs Precision Trade-off Results: CIFAR10

After performing a quantization hyperparameter design exploration we conducted the quantized training of the use case NN using both the standard STE approach in TensorFlow library (Krishnamoorthi, 2018) and the proposed scheme. It is to be noted that TensorFlow’s scheme does not quantize the bias. This means that, when mapped to the crossbars, additional quantization studies would be needed.

Deep convolutional NN also take advantage of the proposed solution. Figure 8 shows the evolution of the DNN learning through the training process. When quantized with 4-bit (weights and activations) our solution gives accuracies only 0.7% away of the state of the art. Moreover, and as described in Table 1 our solution provides a significant reduction in the number of full-custom circuit modules involved in the algorithm-to-HW mapping.

Table 1. CIFAR10 CNN quantization schemes comparison. Our proposal brings a 5.7× reduction on the number of different weights to be considered while maintaining competitive accuracies.

| Scheme     | Accuracy | # Different Uniform Weights | DACs/ADCs |
|------------|----------|-----------------------------|-----------|
| TF, 8-bit  | 88.10%   | 1372                        | No        |
| TF, 4-bit  | 84.43%   | 91                          | No        |
| Proposed, 4-bit | 83.7% | 16                          | Yes       |

4.3 Unipolar Weights vs Accuracy Trade-off: HAR

In this experiment we apply the proposed mechanisms to obtain a NN classifying different HAR activities whose weights take only positive values. Training a NN using only unipolar weight is a significantly hard task involving an extensive exploration of the design space. To that end, quantization hyperparameters and the NN structure itself needs to be adapted.

The DA Algorithm 2 conducted the exploration of the NN design space, determining the NN architecture and parameters set that provided the best accuracy while using only positive weights within the NN. We could obtain similar results performing a more traditional parameterized search of the design space, in which for each experiment the activation type and supporting parameters (\( \theta_{hy} \)) where manually varied. However, the application of DA reduced the computational load involved in the process. To help the NN training to converge, and following graph structure shown in Figure 5, custom regularizers were required to penalize negative weights, and a variation of alpha-blending quantization scheme (Liu & Mattina, 2019) was introduced. Fig-
Each parameter in our NN consumes weight matrices use \( \text{relu} \) (Hamdioui et al., 2019), in which each PCM NVM element. The proposed solution is as competitive as the standard area overhead of 10% consumption and area are gathered in Table 2. The estimates, using a characteristics, we designed in house a for the quantitative power/area estimation, we consider deployment to NVM crossbars.

Figure 9. Comparison between TensorFlow STE quantization and proposed solution. Accuracy levels are indistinguishable even with unipolar weight matrices, while the number of different weights to be mapped to conductances drastically varies.

The proposed solution is as competitive as the standard one, while obtaining the significant benefit of a reduced set of weights and uniform HW. But more importantly, we demonstrate that small NN using only unipolar weight matrices /ADC can correctly perform classifications, aiding the deployment to NVM crossbars.

4.4 Power and Area Benefits

For the quantitative power/area estimation, we consider (Hamdioui et al., 2019), in which each PCM NVM element –each parameter in our NN– consumes \( 0.2 \, \mu \text{W} \), and has a \( 25 \, \mu \text{m}^2 \) area, equivalent to \( 0.075 \, \mu \text{m}^2 \). For the DAC/ADC characteristics, we designed in house 4-bit and 8-bit elements, using a 55 nm CMOS technology. Simulated power consumption and area are gathered in Table 2. The estimation of power/area numbers will consider that the final system should be reconfigurable. Therefore a power and area overhead of 10% over the ADC figure for an integrated adapted current subtractor, element needed in the case bipolar weights are present. Regarding each one of the NN layers, DACs and ADCs will only be multiplexed should the layer maintain uniform scaling with the system. With our proposed approach, all layers share the same input ranges, and only the last layer ADCs would be different from the rest of the system.

4.4.1 Power Estimation

To maximize the throughput per NN layer we consider one DAC (ADC) per column (row). From the power perspective, for each layer the total number of NVM cell reads performing the multiplications (and automatically the additions) would be \( \sum_{i} k_i X_i \) for the convolutional layers and \( X_i Y_i \) for the fully connected ones, where \( X_i, Y_i, K_i \) refer the size of inputs, outputs, and kernel respectively, and \( F_i \) refers the number of filters of the \( i \) – \( th \) layer. Regarding the DACs and ADCs utilization, a total of \( X_i \) and digital to analog and \( Y_i F_i \) analog to digital conversions are required. No analog scaling system is required.

The results describing the power estimation per inference in both CIFAR10 and HAR applications is displayed in Table 3. It can be seen that as bipolar weights were needed in the image solution, and due to the amount of multiplications (> 38 million per inference), the saved power is almost negligible. However, in very low power IoT applications, the proposed solution requires only 60% of the power compared with traditional schemes, mainly due to the unipolar weight matrices encoded in the NVM crossbar.

| Device | Power@10 MHz | @100 MHz | Area |
|--------|--------------|-----------|------|
| DAC 4b | 3.2 \( \mu \text{W} \) | 11.7 \( \mu \text{W} \) | 101 \( \mu \text{m}^2 \) |
| DAC 8b | 4.4 \( \mu \text{W} \) | 13.6 \( \mu \text{W} \) | 440 \( \mu \text{m}^2 \) |
| ADC 4b | 1.28 \( \mu \text{W} \) | 12.56 \( \mu \text{W} \) | 1030 \( \mu \text{m}^2 \) |
| ADC 8b | 1.64 \( \mu \text{W} \) | 16.39 \( \mu \text{W} \) | 7920 \( \mu \text{m}^2 \) |

Table 2. Characteristics of designed ADC and DAC

| CIFAR10 | TF 8 bits | TF 4 bits | Ours 4 bits |
|---------|-----------|-----------|-------------|
| Total Power | 19.13 W | 18.54 W | 18.17 W |
| NVM (+|−) | 77e6 | 15.4 W | 15.4 W |
| DAC ops | 75e3 | 1.01 W | 0.87 W |
| ADC\* ops | 115c3 | 2.63W | 2.2W |
| HAR | TF 8 bits | TF 4 bits | Ours 4 bits |
| CIFAR10 | TF 8 bits | TF 4 bits | Ours 4 bits |
| Total Power | 25 mW | 23 mW | 15 mW |
| NVM (+) | 34e3 | 7 mW | 7 mW |
| NVM (−) | 34e3 | 7 mW | 0 mW |
| DAC ops | 384 | 5 mW | 4 mW |
| ADC\* ops | 268 | 6 mW | 4 mW |

Table 3. Estimated power per inference: number of involved NVM cell reads (positive (+) and negative (−) weights), DAC conversions, ADC together with current subtractor/divider operations.
4.4.2 Area Estimation

From the area perspective, the traditional deployment would use one or more crossbars per layer, and only the amount of ADCs, DACs and supporting periphery needed. That means that if the number of filter on a given layer $L_i$ is $F_i$, $F_i$ full custom different ADCs would be designed and placed for that layer. As we described before, this freezes the full-custom NN for a single particular application.

However, with our proposed scheme we can deploy reconfigurable NN applications in the same hardware, using many smaller and fixed-sized crossbars. We can feed the incoming inputs in batches, reusing the kernels unrolled in the crossbar. Adopting this second scheme for the CIFAR10 example, the largest CNN unrolled layer requires an input of size $32 \times 32 \times 32$. For example, if the crossbar size available in our reconfigurable system is $128 \times 128$, the layer can be batched in 256 operations. If the hardware blocks were composed of $512 \times 128$ elements, the layer could be batched in 64 operations. On the other hand, for smaller FC NN this same hardware could fit entire layers. In our HAR application as each layer can easily fit in one $128 \times 128$ crossbar. For both crossbar size examples, every layer but the last would reuse the 128 DAC/ADC pairs during inference.

Table 4 summarizes the area estimation for both applications, when considering a reconfigurable basic crossbar unit composed of $128 \times 128$ elements (a very conservative approach to avoid technology problems) and assisted by 128 DACs, 128 ADCs and additional periphery. For the traditional approaches, we follow the deployment schemes in the literature, and consider that the number of ADCs present in each layer does not need to match the crossbar column size, saving considerable amount of area but avoiding reconfigurability. On the contrary, by using the proposed solution the DACs and ADCs are multiplexed.

The benefits of the proposed are noticeable: First, we guarantee that the HW is uniform across the NN, ensuring reconfigurability. Second, in very large IoT networks, the solution leads to up to 67% area saving -0.36 mm$^2$ vs 1.1 mm$^2$ for 4 bit accelerators. In the case of small fully connected IoT networks, up to 20% area saving is achieved. When comparing against the traditional 8 bit deployment schemes, this area savings raise up to 97% for the CIFAR10 convolutional NN and 89% for the small HAR NN.

### 5 Conclusions

ML at the edge requires from accelerators that efficiently computes inference in constrained devices, and NVM based analog accelerators are promising candidates due to their low power capabilities. However the full-custom per-layer design of the periphery interacting with the crossbars hinder the reconfigurability of the whole system.

| CIFAR10 | TF 8 bits | TF 4 bits | Ours 4 bits |
|---------|-----------|-----------|-------------|
| Reconfigurable | No | No | Yes |
| Crossbars | 44 | 44 | 44 |
| DACs | 448 | 448 | 128 |
| ADCs | 896 | 896 | 256 |
| Current subtractors | 896 | 896 | 256 |
| Total Area | 8.05 mm$^2$ | 1.1 mm$^2$ | 0.22 mm$^2$ |

| HAR | TF 8 bits | TF 4 bits | Ours 4 bits |
|-----|-----------|-----------|-------------|
| Reconfigurable | No | No | Yes |
| Crossbars | 6 | 6 | 3 |
| DACs | 384 | 384 | 128 |
| ADCs | 268 | 268 | 256 |
| Current subtractors | 268 | 268 | 0 |
| Total Area | 2.51 mm$^2$ | 0.35 mm$^2$ | 0.28 mm$^2$ |

This work has presented the first solution that aids the algorithm deployment in uniform crossbar/periphery blocks, at training time. With no accuracy penalty, the method is able to simplify the design of the crossbar periphery, significantly reducing the overall area and power consumption, and enabling real re-usability and reconfigurability. Moreover, we have demonstrated that DNN with unipolar weight matrices can correctly perform bio-signals classification tasks while solving the negative/positive weights problem inherent to NVM crossbars, and therefore reducing by half the crossbar area/energy and significantly simplifying the periphery design. We validated our solution against two different always-ON sensing applications, CIFAR10 and HAR, obtaining competitive accuracies while simplifying the whole system design.

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A Experiments Supporting Libraries

Located at (Review, 2019), a set of open libraries give support to the proposed methodology within the proposed framework. The experiments shown in this work uses the following quantization scheme:

- Customizable delayed quantization: Start the quantization at a given quant_delay
- Uniform tensor quantization (Krishnamoorthi, 2018) defined by the values given by the global variables present in \( V_g \), and uniform precision across layers

However, the libraries have been written modularly, and therefore the final quantization block (modules represented in light grey in Figures 4 and 5) can be directly replaced with a reference to a different function. With this scheme non-uniform or stochastic quantization schemes can be incorporated. Similarly, the quantization stage is dynamically activated/deactivated using a global variable with could be easily substituted to support incremental approaches (Zhou et al., 2017).

And finally, though the results in Section 4 focus on obtaining uniform layers to take advantage of re-usability and reconfigurability, additional global variables can be incorporated and globally orchestrated through their corresponding global variable control elements to provide multiple-precision schemes across layers following HAQ (Wang et al., 2018) scheme.