Unveiling the impact of the bias-dependent charge neutrality point on graphene based multi-transistor applications

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Abstract

The Dirac voltage of a graphene field-effect transistor (GFET) stands for the gate bias that sets the charge neutrality condition in the channel, thus resulting in a minimum conductivity. Controlling its dependence on the terminal biases is crucial for the design and optimization of radio-frequency applications based on multiple GFETs. However, the previous analysis of such dependence carried out for single devices is incomplete and if not properly understood could result in circuit designs with poor performance. The control of the Dirac point shift (DPS) is particularly important for the deployment of graphene-based differential circuit topologies where keeping a strict symmetry between the electrically balanced branches is essential for exploiting the advantages of such topologies. This note sheds light on the impact of terminal biases on the DPS in a real device and sets a rigorous methodology to control it so to eventually optimize and exploit the performance of radio-frequency applications based on GFETs.

1. Introduction

Research in graphene-based electronics has found in radio-frequency (RF) applications an open and fertile land where to exploit the carbon allotrope superlative transport properties, i.e. ultra-high carrier mobility ($2 \times 10^6$ cm$^2$/V·s) and a high saturation velocity ($\sim 5.5 \times 10^7$ cm·s$^{-1}$) [1–7]. The field-effect transistor (FET) is an important component of any RF circuit embedded in the modern information and communication systems, and thus, improvements of its performance have a critical impact on this field [7–9]. Indeed, very auspicious RF graphene field-effect transistors (GFETs) have already been demonstrated [10–12]. An intrinsic (after a de-embedding procedure) cutoff frequency of 427 GHz measured in a graphene-based FET (GFET) of 67-nm channel length is the highest reported so far [13]. Similarly, an intrinsic maximum oscillation frequency of 200 GHz has been achieved in a GFET of 60-nm length [14]. Although further improvement of the RF device performance is expected [15], the already proven GFET figures of merit (FoMs) allow the design of applications operating at millimeter wave (mmWave) frequencies. Those encompass applications where the GFET leverages either its remarkable high transconductance, e.g., low noise amplifiers (LNAs) [16]; or the graphene ambipolarity such as resistive mixers [17–21]; frequency multipliers [21, 22]; and power detectors [23], all of them demonstrated to properly operate in the gigahertz band.

To push graphene electronics towards higher technology readiness levels (TRLs), and shaping GFETs as the core of novel RF applications, it is first necessary to deeply comprehend those factors that more critically impact the circuit performance [10–12]. Among them, the Dirac point shift (DPS) is crucial in defining the circuit performance. Specifically, applications based on graphene ambipolarity need a tight control of the DPS. To this purpose, the inclusion of a back-gate in the GFET architecture has been the standard strategy followed so far. Numerous examples have been reported such as the polarity-controllable graphene inverter, the voltage...
controlled resistor [24, 25], or the graphene-based frequency tripler [26] and quadrupler [27] successfully implemented thanks to a carefully adjusted voltage separation of two cascaded GFETs. However, a more advanced graphene technology might require to abandon the four-terminal architecture because of the higher complexity inherent to the fabrication process and, more importantly, the appearance of parasitics due to the back gate, seriously compromising the high-frequency performance [28]. Hence, a thorough understanding of the bias-dependent DPS is required for circuit design, an example of which will be presented to obtain frequency multiplication with single-gated GFETs.

On the other hand, the vast majority of experimental GFET-based circuits reported so far are founded on single-transistor stages. However, the better performing circuits to come will rely on multiple-transistor stages, where the direct observations extracted from single devices become inappropriate. This work shows that a careful consideration of the DPS bias dependence is necessary to reach the optimal performance of multi-transistor circuits. Specifically, the DPS experienced by each GFET in a differential topology can ruin the required symmetry, spoiling their performance. This deleterious effect has been reported, e.g., in [29] where a dissymmetry under large drain-to-source biases appeared between the two GFETs comprising a balun. In addition, a different DPS rate from the usually expected, i.e. half of the externally applied drain-to-source bias, has been observed in [30] for two GFETs connected in a complementary-like inverter topology. It is in this forthcoming technological arena where the DPS can hamper the performance of multi-GFET circuits; an issue that we intend to describe and rationalize in this note, which is structured as follows: section 2 presents the theory behind the DPS, by analyzing the electrostatics, and a comparison of the predictions against dc measurements of a GFET reported elsewhere [31]; section 3 describes how to control the impact of the DPS in a multi-transistor circuit while section 4 shows the development of new functionalities making use of a deeper understanding of the DPS phenomenon. Finally, the conclusions are drawn in section 5.

2. Dirac point shift (DPS): theory versus experiment

The Dirac voltage ($V_{\text{Dirac}}$) of a GFET is defined as the gate bias that sets the charge neutrality condition in the graphene channel, namely, the gate bias that results in a minimum conductivity, and therefore, it can be readily located at the vertex of the V-shaped transfer characteristics (TCs) of the GFET. For a well-behaved long-channel GFET, we can estimate $V_{\text{Dirac}}$ by considering same electron/hole mobility as well as symmetrical charge distribution, i.e., same electron/hole concentration at the source and drain edges. These concentrations can be obtained upon application of Gauss’ law along a vertical cut of the GFET structure, i.e., assuming the gradual channel approximation, and after considering the quasi-Fermi levels equal to $V_g$ and $V_d$ at the source and drain terminals, respectively [32]. For ultra-short-channel devices, the 2D Poisson equation should be considered instead [33]. Aiming to get a compact equation that could be easily handled by circuit designers, only the long-channel case has been considered in this work.

Using the abovementioned methodology, the $V_{\text{Dirac}}$-terminal-bias dependence of a four-terminal GFET can be written as:

$$V_{\text{Dirac}} = V_{g0} + \left( C_t + C_b \right) \frac{(V_d + V_s)}{2} - \frac{C_b}{C_t} (V_b - V_{b0}),$$

(1)

where $C_t$ and $C_b$ are the top and bottom oxide geometrical capacitances per unit area, respectively, and $V_g$, $V_s$, and $V_b$ are the gate biases at the source, drain, and back gate, respectively. These quantities embrace work-function differences between the gates and the graphene channel and the possible presence of additional charges due to impurities or doping. The dependence of $V_{\text{Dirac}}$ in equation (1) on $V_d$ and $V_s$ is a unique feature in devices with ambipolar transport [34], and has also been observed in carbon nanotube devices [35, 36]. Indeed, the term $(C_b/C_t)(V_d-V_{b0})$ in equation (1) has been usually used to experimentally obtain the ratio $(C_b/C_t)$ by sweeping $V_b$ while keeping the rest of terminal biases constant [37–39].

If one of the gate capacitances per unit area, e.g. the top-gate, is much larger than the other, i.e. $C_t > C_b$ then the four-terminal GFET can be considered as a three-terminal device and equation (1) simplifies into:

$$V_{\text{Dirac}} = V_{g0} + \frac{(V_d + V_s)}{2}.$$ 

(2)

Most of experimental GFETs found in the literature are either three-terminal devices or four-terminal ones where the condition $C_t \approx C_b$ is met, and therefore, equation (2) commonly applies. Remarkably, the bias dependence of $V_{\text{Dirac}}$ reported in the literature [29, 30, 40–42] is in many cases successfully connected to the external drain and source biases, $V_{d1}$ and $V_{s1}$, respectively, specifically to $(V_{d1} + V_{s1})/2 = V_d/e$, instead of $(V_d + V_s)/2$ predicted in equation (2) (figure 1(a) schematically depicts the difference between external and intrinsic voltages). We have found out the reason of such a coincidence and carried out measurements to demonstrate that equation (2) should be considered instead.

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Figure 1(a) shows the equivalent resistive networks of both three- and four-terminal GFETs with the intrinsic graphene channel resistance \( R_{ch} \) and the extrinsic drain \( R_{d} \) and source \( R_{s} \) resistances. These include the drain and source metal-graphene contact resistances, respectively, which are currently crucial and undesirable elements impacting the RF performance of GFETs. For the sake of simplicity, bias-independent contact resistances have been considered in the device modeling approach of this work. The bias dependence of physical effects at metal-graphene interfaces affecting the carrier transport can be embraced by the channel charge description as incorporated by the device model used here. Assuming that the drain/source extrinsic resistances are similar \( R_{ext} = R_{d,s} \approx R_{c,v} \), then the intrinsic drain and source voltages \( V_d \) and \( V_s \) can be determined as:

\[
\begin{align*}
V_d &= \frac{V_d,e}{2 + x} \left( 1 + \frac{x}{2 + x} \right) \\
V_s &= \frac{V_s,e}{2 + x} \left( 1 + \frac{x}{2 + x} \right)
\end{align*}
\]

where \( x = R_{ch}/R_{ext} \).

Interestingly, from equation (3) we observe, adding up both expressions, that the equality \( (V_d + V_s) = V_{d,e} + V_{s,e} \) holds and as \( V_{d,e} \) is usually shorted to ground, then \( (V_d + V_s) = V_{d,e} \). However, this is not a general case, figure 1(b) shows a proper counterexample: the TCs of a 14-\( \mu \)m length GFET reported in [31] in two scenarios: (Case A) \( V_{d,e} = 0.1V \) and \( V_{s,e} = 0V \); and (Case B) \( V_{d,e} = 1.1V \) and \( V_{s,e} = 1V \); thus keeping in both cases same \( V_{d,e} = 0.1V \), but in case B breaking the condition of \( V_{s,e} \) grounded. As it can be seen, in spite of what has been so far widely reported, the DPS indeed depends on \( (V_d + V_s) \), as the same \( V_{d,e} \) cannot explain these two different DPSs. The inset in figure 1(b) shows the measured TCs after countering the DPS according to the model proposed in equations (2) and (3), supporting the exposed theory and demonstrating a perfect cancellation of the shift.

More importantly, because of the presence of non-negligible extrinsic resistances in GFETs, the potential \( V_s \) cannot be shorted to reference in practice. Indeed, recent studies on contact resistance of GFETs [54, 55] show that the ratio \( x = R_{ch}/R_{ext} \) is lower than 1 for the vast majority of experimental devices, meaning that most of the external \( V_{d,e} \) drops at the extrinsic resistances. Thus any change in either \( V_{d,e} \) or \( V_{s,e} \) would cause a change in \( V_s \), revealing that the DPS needs to be taken into account in the circuit design.
3. A case of practice: impact of DPS on an RF balun

Differential topologies could become attractive candidates for the development of high-performance RF graphene applications as they provide less even-order distortion, immunity to common-mode noise couplings and crosstalk through the substrate and supply rails [56, 57]. However, such topologies are essentially based on the symmetry of the electrically balanced branches and ultimately relied on the symmetry of the transistor outcome. For the specific case of differential pairs, the symmetry has been demonstrated to be essential and analyzed from a mathematical perspective, revealing its impact on the performance of this amplifier topology [58, 59].

The results shown in section 2 lead us to investigate the unavoidable DPS impact on the RF performance of GFET-based applications with symmetry requirements. A paradigmatic example arises when designing a balun. This circuit, shown in figure 2(a), is central for the development of graphene-based differential circuit topologies, exploiting the unique symmetrical and ambipolar behavior of graphene. In most cases, the incoming signals originated in antennas are single-ended and to achieve the differential topology concept, a balun circuit is required to transform the single-ended signal ($v_{in}$, unbalanced) into the differential signals ($V_{out1}$ and $V_{out2}$, balanced, i.e., with a $\pi$-rad phase difference). To take full advantage of differential topologies, the power of both balanced signals should be similar. However, for a graphene-based circuit, the inherent DPS will break the symmetry between both transistors, making mandatory to carefully counter-balance it by continuously applying effective gate biases to each GFET as described by equation (2). Notice that the bias tees have been used in the schematics (figure 2(a)) for pointing out explicitly different dc effective gate bias for each device. However, this would not spoil the dc power consumption because the gate terminals behave ideally as open circuits.

Considering a specific operating bias point, both GFETs could, in this context, be fed by a single power supply through the use of a voltage divider.

The design and analysis of an RF balun based on graphene, requires a physics-based description of the electrical behavior of the GFET. To this purpose, we have embedded into Keysight® ADS, a large-signal model implemented in Verilog-A by some of the authors [53] which has been demonstrated to show good agreement with measurements [60]. The main features of the graphene technology considered are summarized in table 1.

Figure 2(b) depicts the transconductance ($g_m = \partial I_K/\partial V_{G_K}$) of each GFET (labeled 1 and 2) without countering the DPS effect (Case I) at constant $V_{DD} = V_{G_G1} = V_{G_G2}$ and countering the DPS effect (Case II). The control of the DPS can be realized by tuning $V_{G_G1}$ and $V_{G_G2}$. In Case I (figure 2(b)), when $V_{DD}$ is low, the DPS does not substantially break the symmetry and, thus, both transconductances have similar modulus. However, if $V_{DD}$ is large enough, the symmetry between both devices is broken and, for a given $V_{G_G}$ ($g_m$) for each GFET is considerably different, resulting in unbalanced output signals (not shown here) and leading to a useless circuit. As a result, the DPS in Case I limits the use of this circuit only for low drain biases (see figure 2(c)), resulting in strongly attenuated output signals, as exemplified by the $-20$dB gain values obtained by the graphene-based...
This work demonstrates that the DPS in GFETs is proportional to the intrinsic voltages $V_D + V_V$, not accessible in practice, which can be considerably different from the externally applied biases due to the non-negligible metal-graphene contact resistances. It has been shown that the validity of the usual approximation that considers the DPS proportional to $V_{dc,ext}$ is limited and should be avoided.

Thus, a simple analytic equation for long-channel GFETs has been provided in order to evaluate the bias-dependence of DPS that could be compensated by the automatic application of an effective gate bias. As a proof of concept, the operation of a graphene-based balun that harnesses the unique ambipolar characteristic of the DPS is demonstrated in two cascaded GFETs that can be achieved by controlling individually the applied electrical frequency multiplication with single-gated GFETs.

In this section, the previous analysis of the DPS phenomenon allows us to propose a solution to achieve uncontrolled different behaviors in two cascaded GFETs. Figure 3 depicts the proposed single-gated GFET-based frequency multiplier, whose TCs are represented in figure 3(d). Specifically, the W-shaped TC tunability with both the value of the resistor $R_X$ for a given supply bias and the value of the supply bias ($V_{DD}$) for a given $R_X$ are depicted, respectively. These results indicate that the voltage drop originated at $R_X$ causes an increasing separation between the charge neutrality points of both GFETs. Figure 3(d) shows a sketch of the working principle for a frequency tripler and quadrupler based on the W-shaped TC at $V_{DD} = 2V$ with $R_X = 1k\Omega$ (green curve in figure 3(c)). Considering an input frequency of $f_{in} = 1MHz$, the analysis of the output power spectrum (not shown here) indicates that the resulting RF relative power for the frequency tripler is 61.9% at the triple fundamental frequency ($3f_{in}$), while the quadrupler shows a relative power of 38.6% at the quadruple fundamental frequency ($4f_{in}$). Inset in figure 3(d) depicts a comparison between the predicted output signals and pure sinusoids of corresponding frequencies showing an evident distortion. The performance of GFET-based frequency multipliers can be improved by additional matching and stability networks; however, this is out of the scope of this study intended to show the impact of the DPS control at a device level on multi-transistor configurations. Therefore, this design gives insight about how the accurate control of the bias-dependence of $V_{Dirac}$ can be exploited for the development of sophisticated RF applications.

### 4. Exploiting DPS: frequency multiplication based on single-gated multi-GFET stage

In this section, the previous analysis of the DPS phenomenon allows us to propose a solution to achieve frequency multiplication with single-gated GFETs.

The working principle of the frequency tripler [26] and quadrupler [27] is based on a W-shaped TC observed in two cascaded GFETs that can be achieved by controlling individually the applied electrical field dependence of $V_{Dirac}$ of each device (e.g., see figure 3(d)). Up to now, the separated electrostatic control of $V_{Dirac}$ has been demonstrated by the use of dual-gated devices (i.e., by adjusting $V_b$ in equation (1)) [26, 27]. However, according to equation (2), it is also possible to modify the $V_{Dirac}$ of a single-gated device by tuning its source and drain voltages, avoiding the introduction of a fourth terminal. Therefore, the search of W-shaped TCs in single-gated GFETs is of utmost interest, and of partial success in [61] where W-shaped responses were observed, although in an uncontrolled way as illustrated by the fact that devices with the same structure and dimensions presented different behaviors [61]. Here, leveraging the understanding of the DPS behavior aforementioned, we have implemented an original and simplified way to achieve W-shaped TCs in single-gated devices to exploit frequency multiplication based on graphene ambipolarity.

To do so, a lumped resistor ($R_X$) is included between the two cascaded GFETs as shown in figure 3(a) in order to produce a controlled separation of the DPS of each GFET (proportional to the actual voltage drop at $R_X$) giving rise to a W-shaped TC that can be exploited for frequency multiplication.

Figure 3(a) depicts the proposed single-gated GFET-based frequency multiplier, whose TCs are represented in figures 3(b)-(c). Specifically, the W-shaped TC tunability with both the value of the resistor $R_X$ for a given supply bias and the value of the supply bias ($V_{DD}$) for a given $R_X$ are depicted, respectively. These results indicate that the voltage drop originated at $R_X$ causes an increasing separation between the charge neutrality points of both GFETs. Figure 3(d) shows a sketch of the working principle for a frequency tripler and quadrupler based on the W-shaped TC at $V_{DD} = 2V$ with $R_X = 1k\Omega$ (green curve in figure 3(c)). Considering an input frequency of $f_{in} = 1MHz$, the analysis of the output power spectrum (not shown here) indicates that the resulting RF relative power for the frequency tripler is 61.9% at the triple fundamental frequency ($3f_{in}$), while the quadrupler shows a relative power of 38.6% at the quadruple fundamental frequency ($4f_{in}$). Inset in figure 3(d) depicts a comparison between the predicted output signals and pure sinusoids of corresponding frequencies showing an evident distortion. The performance of GFET-based frequency multipliers can be improved by additional matching and stability networks; however, this is out of the scope of this study intended to show the impact of the DPS control at a device level on multi-transistor configurations. Therefore, this design gives insight about how the accurate control of the bias-dependence of $V_{Dirac}$ can be exploited for the development of sophisticated RF applications.

### Table 1. Graphene technology considered for the circuit design.

| $L$ ($\mu$m) | $W$ ($\mu$m) | $R_X$ | $S$ | $5\Omega_{\mu m}$ |
|--------------|--------------|-------|-----|------------------|
| $\mu$ | 0.2 m$^2$ V$^{-1}$s$^{-1}$ | $V_{ge}$ | $V_{sh}$ | 0 V | $R_{d}$ | $R_{s}$ | $4k\Omega$ |
| $C_i$ | 8 fF $\mu$m$^{-2}$ | $C_b$ | $C_s$/231 | $R_g$ | $R_d$ | $200\Omega_{\mu m}$ |

$\mu$ represents the effective carrier mobility and $R_g$ the gate resistance.

balun reported in [57]. On the other hand, when the DPS is counter-balanced (Case II), the balun proper operation is restored given that the recovered symmetry leads to similar $|g_{m}|$ for both GFETs (cf figure 2(b)). In addition, increasing $V_{DD}$ in figure 2(c) leads to the desired voltage gain for both balanced signals through the automatic application of different gate biases (by countering the DPS), e.g., linearly with $V_{DD}$ but keeping opposite slopes as shown in figure 2(d). This way, given that the DPS is under control, the supply bias ($V_{DD}$) offers an additional degree of freedom to tune the desired voltage gain, although at the cost of a higher dc power consumption.
Graphene has been assured by controlling the DPS showing an improved performance. In addition, a frequency tripler/quadrupler based on W-shaped transfer characteristic of two cascaded single-gated GFETs is proposed, evidencing that monitoring the bias-dependence of the DPS is pivotal for the design of RF applications. In summary, this work provides critical insights on DPS phenomenon paving the way towards the development of RF multi-transistor circuits based on graphene technology.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

Conflicts of interest or competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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