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Design of an ultra low power third order continuous time current mode $\Sigma\Delta$ modulator for WLAN applications

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ABSTRACT

This paper presents a third order continuous time current mode $\Sigma\Delta$ modulator for WLAN 802.11b standard applications. The proposed circuit utilized feedback architecture with scaled and optimized DAC coefficients. At circuit level, we propose a modified cascade current mirror integrator with reduced input impedance which results in more bandwidth and linearity and hence improves the dynamic range. Also, a very fast and precise novel dynamic latch based current comparator is introduced with low power consumption. This ultra fast comparator facilitates increasing the sampling rate toward GHz frequencies. The modulator exhibits dynamic range of more than 60 dB for 20 MHz signal bandwidth and OSR of 10 while consuming only 914 $\mu$W from 1.8 V power supply. The FoM of the modulator is calculated from two different methods, and excellent performance is achieved for proposed modulator.

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Introduction

Today, according to progressive extension of digital system applications and abilities, digitizing the environmental analog world is more essential, especially in higher speeds and resolutions. Due to their capabilities to achieve high resolutions with a simple comparator, $\Sigma\Delta$ modulators are the case of interest. Because of their intrinsic oversampling, design of anti-aliasing filter is become more relaxed in $\Sigma\Delta$ modulators and also the size of required capacitances is reduced [1]. $\Sigma\Delta$ Modulators are now trends to cover not only audio [2] and biomedical [3] applications, but also growing through wireless applications such as WLAN, WCDMA, and GSM [4]. These applications require high speed modulators with high speed performance, i.e., wide bandwidth. For example, the required bandwidth for WLAN application is as wide as 20 MHz which the maximum Over Sampling Rate (OSR) is limited by the CMOS process restrictions.

Continuous Time $\Sigma\Delta$ Modulators (CT$\Sigma\Delta$M) have been attained interesting performances in low power [5] and high speed [6] applications. The required bandwidth for CT$\Sigma\Delta$M’s building blocks is more relaxed in comparison with switched capacitor techniques which results a significant reduction in their consumed power. Also, CT$\Sigma\Delta$M requires much simpler anti-aliasing circuits [2]. $\Sigma\Delta$ modulators are designed by switched capacitor techniques and mostly by voltage mode cir-
cuits, but in the result of decreasing transistor feature sizes and hence decreasing the power supply and voltage headroom, these techniques have encountered with several problems in recent years.

Instead, current mode techniques can be suitable alternatives for switched capacitor circuits because of their less sensitivity to voltage headroom. The other benefits of current mode circuits over their voltage mode counterparts are smaller propagation delay and therefore more speed, compatibility with smaller feature sizes, less sensitivity to electrostatic discharge, suitability for sensors and electrodes, and no need for linear capacitances which are very difficult to be implemented in the state-of-the-art digital VLSI technology.

One of the most traditional circuit blocks for implementing of continuous time current mode integrators is current mirror. Because the current output of other circuits, such as current conveyors or OTAs, cannot be shared simply with other circuits, multiple outputs may be required for constructing a filter. But, it is obtained very simply by making as very replica circuits as need by current mirror circuits [7]. This paper proposes a current sharing technique to improve the bandwidth of the current mirror based integrator which also results a much simpler biasing circuitry for the integrator. Also, a novel comparator is introduced based on dynamic latches.

The paper is organized as follows: in Section 2, system design and scaling are described. Section 3 introduces circuit implementation of modulator’s building blocks. Section 4 gives the simulation results followed by a conclusion in Section 5.

Methodology

System level design

A traditional solution for system level design of CTΣΔM problem is starts from equivalent discrete time system and then converting the attained characteristics to their continuous time counterparts by impulse invariant transform [8]. Feedback structure is used for more stability, compatibility with impulse invariant technique to its continuous time equivalence and equalizing it with the resulting NTF from continuous time block diagram, which itself could be calculated from standard signal flow-graph techniques such as Mason method. The method is completely described by Ortmanns and Gerfers [8]. The equivalent continuous time transfer function is:

\[
NTF(s) = \frac{s(s - 0.3184)(s + 0.121)}{(s + 0.4014)(s^2 + 0.4096s + 0.1644)}
\]

As the results, system coefficients are calculated. After defining coefficients, the system is scaled to achieve suitable levels for integrators and quantizer. Power spectrum density and dynamic range diagrams are illustrated in Figs. 3 and 4, respectively. The system exhibits 68 dB of dynamic range and 61 dB of maximum SNDR for Over Sampling Ratio (OSR) of 10 and bandwidth of 20 MHz compatible with WLAN standard. Now, the system is ready to be implemented by transistor circuits.

Circuit level design

Subsequent to system design and optimization, modulator’s building blocks must be implemented in circuit level. All circuit blocks are implemented in 0.18 μm standard CMOS technology. The modulator is comprised of three major building blocks as follows:

Integrator

The most important building block of the ΣΔ modulator is the integrator. Fig. 5 illustrates a simple current mirror continuous time integrator. Neglecting the output impedance of transistors and parasitic capacitances and assuming identical transistors, circuit transfer function can be obtained from:

\[
\frac{i_{op} - i_{in}}{i_{op} - i_{in}} = \frac{-g_m}{C_s}
\]

which determines the continuous time integrating operation of the circuit. From CTΣΔM theory [11], the below conditions must be satisfied:

\[
g_m = \frac{1}{C} \frac{1}{T}
\]

where \( T \) is the sampling period. The more precise transfer function of the circuit, by considering \( ro \) and \( C_{gd} \) is [12]

\[
\frac{i_{op} - i_{in}}{i_{op} - i_{in}} = \frac{A_0 \frac{1 - \frac{z_1}{r_n}}{1 + \frac{z_1}{r_n}}}{2C_{gd}}
\]

where \( z_1 \) is the zero of the circuit and given by

\[
z_1 = \frac{g_m - g_{db}}{2C_{gd}}
\]
also, \( p_1 \) is the system’s pole and \( A_0 \) is the integrator DC gain:

\[
p_1 = \frac{2g_{ds}}{C + 4C_{psd}}
\]

\[
A_0 = \frac{g_m - g_{ds}}{2g_{ds}}
\]

As a rule of thumb, DC gain must be equal with or more than the OSR [13]. The desired values for achieving a modulator with 20 MHz bandwidth and 400 MHz sampling rate are:

\[
A_0 \geq \text{OSR} \rightarrow A_0 \geq 10
\]

Integrating capacitance, \( C \), is defined by technological and layout considerations and chosen to be 0.5 pF. By neglecting \( C_{psd} \) in comparison with \( C \) and choosing the system pole to be smaller than 100 KHz satisfying WLAN standard criterion, \( g_{ds} \) becomes less than 100 nS which is translates to 10 M\( \Omega \) of output resistance. This huge amount of output resistance may not realizable by a single stage current mirror and employing of cascade structure is inevitable. For achieving the desired DC gain, \( A_0 \) must satisfies Eq. (10) and hence \( g_m \geq 15g_{ds} \). This could be attained by cascade structure with low biasing current. Eq. (5) implies that the integrator gain (\( gm/C \)) must be greater than the sampling frequency (e.g., \( 4 \times 10^8 \) here), and hence, \( gm \) must be greater than 200 \( \mu \)S.

One of the most important problems of cascade structures is their biasing circuit complexities. Such circuits need three different bias sources, in addition to the supply source, for proper working which may be difficult to be achieved precisely. In this paper, the cascade circuit is configured to reduce the number of required bias sources to two. Also, by suitable design of transistor sizes, in addition to satisfying all mentioned
conditions, these biasing sources became equal, and hence, the number of biasing sources reduced to one which implies the extremely simple biasing circuit.

A notable characteristic of current mode circuits, which is completely in contrary with their voltage mode counterparts, is their input and output resistances. In addition to loading effects considerations, input resistance should be as low as possible to enhance the integrator dynamic range and bandwidth. Increasing the dynamic range as the result of decreasing the input resistance is justified by this fact that when a specific current inputs the circuit, causes lower variations in the voltage of input node. If these variations are large, the voltage of input node may reach to one of its two extremes (cutting off the input transistors and/or pushing them toward triode region), which degrades the operation of the circuit. Therefore, the smaller the input resistance, the larger the input current need to convey the circuit to its extremes. This fact is implying that the smaller the input resistance, the larger the attained dynamic range. Also, decreasing the input resistance far the higher frequency pole of the integrator to much higher frequencies and hence increase the bandwidth of the integrator.

The proposed integrator is realized by a modified current mirror circuit that drives the integrating capacitors. This method reduces the input resistance of cascade current mirror integrator by diode connecting of cross-connected load PMOS transistors (M55 and M66) as illustrated in Fig. 6. By this technique, the input resistance becomes:

\[ R_{in} \approx \frac{1}{g_{mN}} \parallel \frac{1}{g_{mP}} \approx \frac{1}{2g_{m}} \]  

This is equal to the half of input resistance of traditional cascade current mirror integrators. This approach generates a fast signal path and increases the integrating bandwidth through several GHz which is completely appropriate for high speed and low power applications.

**DAC**

The DAC has a return-to-zero (RZ) structure which results preventing from large errors in consequence of continuously injection of the current. A monobit DAC is employed for ideal linearity (Fig. 7). The switching transistors (Mdf1, Mdf4 and Mdf2, Mdf3) work inversely according to the incoming differential signals from the comparator. This structure could push/pull the current into/from the integrator and produce a proper negative feedback. Nevertheless, this circuit has its own non-idealities such as spiking response and switching problems. Fortunately, these non-idealities are effectively smoothed at the input node of integrator due to low resistance path which
results in negligible changes at the input node and cause no considerable effects on normal operation of the integrator and its linear work.

**Comparator**

The quantizer is based on positive feedback cross-coupled latch [12]. Transistors MC7 and MC8 perform sampling. When the input differential signals applied to the drains of MC3 and MC4, due to the difference between them, regeneration accomplished and the comparator rapidly converges to one of its stable Equilibria. There is a problem encountered with convergence of this type of comparators; if the difference between the input signals be not large enough, the comparator remains at its unstable equilibrium (i.e., metastable point), that is, a value between its two stable points. The smallest perturbation, which moves the state of the comparator toward of its stable equilibrium to one of those stable Equilibria according to the direction of applied perturbation. The required transition time for that movement is translated to propagation delay. Hence, the transient behavior of the latch is achievable by a simple one-dimensional dynamical analysis. By the analysis of the latch and considering the latch as two back-to-back coupled negative amplifiers, the below relation is achieved:

\[ v_{out}(t) = \left( \prod_{j=0}^{(t/\delta t)-1} A(t - j\delta t) \right) v_0 \]  

![Fig. 6 The proposed integrator schematics.](image)

![Fig. 7 The accomplished return-to-zero DAC.](image)

where \( v_{out}(t) \) is the output of each inverter at time \( t \), \( A(t - j\delta t) \) is the gain of the amplifier, \( \delta t \) is the requiring time for inverters to response, and \( v_0 \) is the initial voltage of the amplifier. Decreasing the propagation delay demands to rapidly increasing the \( v_{out}(t) \), which could be done by increasing \( A \) and/or \( v_0 \) and/or decreasing \( \delta t \). Increasing \( A \) and decreasing \( \delta t \) require more power consumption, and hence, the only remaining solution for low power applications is increasing the initial value of input voltage at input of the comparator.

Just before the starting of the regeneration, the input resistance of the comparator is equal with the half of output...
resistance of transistors $M_{C3}$ and $M_{C4}$. This causes the less infusing current into the comparator because the output stage of the integrator connects to this high impedance point and may not be able to push all of its current to the comparator. A current buffer circuit with low input and high output impedances could improve the performance of both integrator (by preventing the returning the current of the output stage of the integrator back to the integrator circuit and saturate its transistors) and comparator (by providing a very high output impedance which is able to steer all of its current into the comparator). Therefore,
this circuit increases the initial voltage of the regenerative comparator and hence according to Eq. (12) decreases the propagation delay of the comparator. Fig. 8 illustrates the proposed comparator and its transient response. All of its Equilibria are notified in the transient analysis. It can be seen that the transient response of the comparator slows down near the unstable equilibrium. This phenomenon is as the result of a bifurcation point around the location of unstable equilibrium (like the unstable equilibrium of the reverse pendulum). Existence of that metastable point is one of the most important sources of the propagation delay in the dynamic latch based comparators. The proposed comparator exhibits about 200 ps of propagation delay for 100 nA of input signal. As mentioned, this delay is short enough for the comparator to handle as fast sampling rate as 1.5 G sample/s.

The dominant source of offset in the latch is the dynamic offset as the result of mismatch between $M_{C1,2}$ and $M_{C3,4}$ and $M_{C5,6}$. But, input referred offset of this part is get divided by the gain of preamplifier (current to voltage convertor). The same procedure is occurred for kickback as well. In addition,

### Table 1 Comparison between the proposed modulator with some works in the literature.

| Ref. | SNDR (dB) | DR (dB) | BW (KHz) | OSR | Power (mW) | Arch. | FoM$_{SNDR}$ (pJ) | FoM$_{DR}$ (dB) |
|------|-----------|---------|-----------|-----|------------|-------|-------------------|-----------------|
| [3]  | 68        | 70      | 4         | 125 | 0.4        | second order | 24.35            | 140             |
| [4]  | 73        | 75      | 1250      | 32  | 12.74      | 2-1             | 1.39             | 154.91          |
| [5]  | 82        | 86      | 100       | 65  | 1.8        | fourth order   | 0.874            | 163.44          |
| [19] | 65        | 50      | 5000      | 50  | 28         | first order    | 1.926            | 132.51          |
| [20] | 57        | 62      | 0.4       | 125 | 0.08       | second order   | 172.8            | 128.99          |
| [21] | 79        | 81      | 100       | 130 | 5          | third order    | 3.432            | 154.01          |
| [22] | 60.96     | 74      | 10000     | 35.8| 31         | third order    | 1.698            | 159.08          |
| [23] | 47.7      | 54.3    | 1000      | 30  | 1          | third order    | 2.522            | 144.3           |
| This work | 56      | 60.7    | 20000     | 10  | 0.914      | third order    | 0.004            | 164.1           |
$M_{C_{1,2}}$ and $M_{C_{3,4}}$ offsets are divided by the voltage gain of latch itself which reduce the input referred offset more.

Fig. 9 illustrates the whole modulator’s circuit. As shown, the modulator is implemented by a relatively simple circuit which is a notable characteristic of the current mode circuits.

Results and discussion

The simulation results of this third order $\Sigma\Delta$ modulator have been executed for a sampling frequency of 400 MHz and oversampling ratio (OSR) of 10 with a signal bandwidth of 20 MHz. The voltage sources of 1.8 V (as the power supply) and 1 V (for biasing circuitry) are employed where the overall consumed power from 1.8 V power supply is about 610 $\mu$W which mentioned an ultra low power modulator.

Figs. 10 and 11 show the in-band and out-of-band power spectrum density, respectively, and show the third order noise shaping. Fig. 12 sketches the SNDR versus input signal level from Eq. (15) is in dB and its larger values are better.

Also, another method for calculating of FoM is proposed by Schreier and Temes [18] based on dynamic range as follows:

$$\text{FoM}_{\text{SDR}} = \frac{\text{Dynamic Range(dB)}}{2 \times \text{BW} \times 2^{\text{ENoB}}}$$

Table 1 compares the performance of the proposed circuit with the literature. It can be seen that the proposed circuit has an excellent performance in the FoM point of view for both calculations.

Conclusions

Third order fully differential continuous time current mode $\Sigma\Delta$ modulator have been designed and simulated in 0.18 $\mu$m standard CMOS technology. By decreasing the input resistance, an integrator with very wide band and proper dynamic range has been achieved. By special design and configuration of the cascode structure, the biasing circuit became very simple and reduced to just one biasing source. A very fast current comparator is proposed with the ability to work in GHz sampling rates and low power consumption. The SNDR of the proposed circuit was about 56 dB and its dynamic range was 60.7 dB for signal bandwidth of 20 MHz by OSR of 10 and sampling frequency of 400 MHz. The proposed circuit exhibits excellent FoM for two different criteria in comparison with related works.

Conflict of interest

The authors have declared no conflict of interest.

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