Unifying Data, Model and Hybrid Parallelism in Deep Learning via Tensor Tiling

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Abstract
Deep learning systems have become vital tools across many fields, but the increasing model sizes mean that training must be accelerated to maintain such systems’ utility. Current systems like TENSORFLOW and MXNET focus on one specific parallelization strategy, data parallelism, which requires large training batch sizes in order to scale. We cast the problem of finding the best parallelization strategy as the problem of finding the best tiling to partition tensors with the least overall communication. We propose an algorithm that can find the optimal tiling. Our resulting parallelization solution is a hybrid of data parallelism and model parallelism. We build the SOYBEAN system that performs automatic parallelization. SOYBEAN automatically transforms a serial dataflow graph captured by an existing deep learning system frontend into a parallel dataflow graph based on the optimal tiling it has found. Our evaluations show that SOYBEAN is 1.5×–4× faster than pure data parallelism for AlexNet and VGG. We present this automatic tiling in a new system, SOYBEAN, that can act as a backend for TENSORFLOW, MXNET, and others.

1. Introduction
Deep neural networks (DNNs) have delivered tremendous improvements across many machine learning tasks, ranging from computer vision [33, 40] and speech recognition [18, 26] to natural language processing [15, 30]. The popularity of DNNs has ushered in the development of several machine learning systems focused on DNNs [2, 4, 13, 22]. These systems allow users to program a DNN model with ease in an array-language frontend, and each also enables training on a GPU for performance.

The power of DNNs lies in their ability to use very large models and to train with huge datasets. Unfortunately, such power does not come for free, as training such networks is extremely time consuming. For example, a single AlexNet training run takes more than a week using one GPU [40]. Compounding the problem, DNN users must completely retrain the model after any changes in the training parameters while fine-tuning a DNN. Given this frustratingly long training process, the holy grail of a DNN system is to deliver good training performance across many devices.

The most widely used method for scaling DNN training today is data parallelism. Traditional DNN training is based on batched stochastic gradient descent where the batch size is kept deliberately small. Within a batch, computation on each sample can be carried out independently and aggregated at the end of the batch. Data parallelism divides a batch among several GPU devices and incurs cross-device communication to aggregate and synchronize model parameters at the end of each batch using a parameter service [20, 43]. DNN models are large and growing. For example, in 2012 AlexNet had ~150MB of model parameters, and a DNN acoustic model from three years later [46] had 1.6GB of parameters. In order to reduce the overhead of synchronizing large models, one must use very large batch sizes, ensuring that computation time dominates over communication time. Data parallelism’s reliance on very large batch size comes at a price: it is known that training using larger batches converges more slowly, hurts accuracy [39], and is more likely to lead to globally-suboptimal local minima [35].

To avoid this batch-size-dilemma of data parallelism, one can divide the model parameters across devices and synchronize the intermediate computation results instead of the model parameters. This scheme is referred to as model parallelism. However, the relative merits of model and data parallelism depend on the batch size, the model size, and the shape of the model in use. Previous work [39] also suggests that different layers of a DNN model should be treated differently to achieve better training speed. Due to this unclear trade-off and the fact that model parallelism requires a more complex implementation, with the exception of an earlier learning system [20], all existing systems focus on data parallelism.

Our insight is that data, model and hybrid parallelism can be unified as approaches to parallelizing tensor operations by dividing the tensor inputs along different dimensions. This insight allows us to cast the challenge of scaling DNN as a problem of “tensor tiling”: along which dimension should one partition each input or intermediate tensor involved in the DNN computation? As the scaling bottleneck of DNN...
training is the communication overhead, we define the corresponding optimization problem on the tensor dataflow graph, and propose an algorithm to find the best tiling strategy that minimizes the communication cost. The resulting tiling strategy is comprehensive. Not only can it partition along any one dimension (thus supporting either data or model parallelism), it also can partition any tensor along more than one dimension (thus supporting a hybrid version of both data and model parallelism). Furthermore, unlike existing approaches that adopt a single partitioning strategy for all tensors involved in the computation, decisions are made separately for each tensor, depending on its size, shape, and the overall DNN model configuration.

Because of the flexibility allowed for tiling, it is difficult to find an optimal strategy. In fact, at its full generality, the tiling problem is known to be NP-complete [27]. Fortunately, many DNN models have the common structure of multiple stacked neuron layers. As a result, we can reorganize the dataflow graph of a DNN training into a chain of layers such that each level only interacts with the adjacent levels. With this formulation, we solve the tiling problem using a novel algorithm that recursively applies dynamic programming to find the optimal tiling solution given any DNN configuration and batch size.

To demonstrate the effectiveness our formulation, we have implemented a prototype system called SOYBEAN as a C++-based backend plugin for an existing DNN system MXNET. The practice can be applied to any dataflow-based DNN systems. We evaluated SOYBEAN on a 8-GPU machine and compared its performance against data parallelism with varying configurations. Our evaluations show that SOYBEAN is 1.5 × to 4 × faster than pure data parallelism for AlexNet and VGG.

2. Background & Challenges

Before introducing SOYBEAN’s approach to efficient deep learning, we must motivate the importance of the problem and the current popular approaches. We first introduce basic DNN concepts, and describe data parallelism and model parallelism. We compare the communication costs of these two approaches with a concrete Multi-Layer Perceptron example, which reveals our core precept: data parallelism, model parallelism, and even hybrid parallelism are just different ways of tiling tensors in the dataflow graph. Finally, we discuss the challenges and our contributions of solving this tiling problem in dataflow graph.

2.1 Background on DNN and Deep Learning Systems

At its heart, deep learning is an optimization problem, like other machine learning algorithms. Training a DNN consists of computing a cost function \(C\) given a set of inputs (forward propagation), computing the gradient of that cost function with respect to the model parameters \(\theta\) (backward propagation), and updating the model parameters using the gradient just calculated. This training method is called Stochastic Gradient Descent (SGD). In practice, training is performed by iterating over the training data many times (i.e., “epochs”) doing SGD in mini-batches, as illustrated in the following pseudocode.

```pseudocode
for (epoch = 1 to N):
    foreach (D, in \{D_1, D_2, \ldots\})
        \(\frac{\partial C}{\partial \theta} = \text{CalculateGradient}(D, \theta)\)
        \(\theta := \theta - \epsilon \frac{\partial C}{\partial \theta} \quad \text{// update model parameters}\)
```

Here, the training dataset \(D\) is partitioned into batches \(\{D_1, D_2, \ldots\}\) and SGD is performed iteratively, updating model parameters \(\theta\) after each batch.

DNN models have a common graphical representation, in which layers of neurons are connected by weighted edges across layers. The weights are the model parameters to be learned. DNN training involves a series of tensor computations along the graph structure. Figure 8(a) shows a Multi-Layer Perceptron (MLP) model with 3 fully connected layers. The weights of neuron connections between successive layers \(l\) and \(l+1\) are represented by matrix \(W_l\), where \(W_{l+1}^T\) is the weight between the \(i\)-th neuron of layer \(l\) and \(j\)-th neuron of layer \(l+1\). The set of weights of all layers \(W_1, W_2, \ldots, W_l\) is referred to as a DNN’s model parameters.

To calculate the cost function, one performs forward propagation to compute the activation of a layer from its preceding layer. Specifically, \(x_{i+1} = f(x_i \cdot W_i)\), where layer \(l\)'s activation vector \(x_l\) is multiplied with the weight matrix \(W_l\) and then scaled using an element-wise non-linear function \(f\). The cost function is \(C = g(x_{i_{out}})\) where \(x_{i_{out}}\) is the activation of the last (out) layer and \(g\) is the loss function. Gradients are computed through backward propagation using the chain rule. The computation proceeds from a higher to lower layer. Specifically, two kinds of matrix computations are involved in each step. One computes the gradient of the activation \(\frac{dC}{dx_l} = df(\frac{dC}{dx_{l+1}})W_l^T\). The other computes the gradient of weight matrix \(\frac{dC}{dW_l} = x_l^T df(\frac{dC}{dx_{l+1}})\). Here, \(df\) is the derivative function of \(f\). The weight matrix \(W_l\) is then
updated using the computed gradient. Our discussion so far performs SGD on one sample only. For batched SGD on $b$ samples, the activation of each layer is represented a matrix of $b$ activation vectors.

Existing deep learning systems such as TENSORFLOW and MXNET offer an array-based frontend for users to express the tensor computation for the forward propagation. Because SGD is such a common computation, these systems automatically derive the computation required for the backward propagation and handle parameter updates. The overall computation for both forward and backward propagation is transformed into a dataflow graph of tensor operators. As shown in Figure 2(b), the dataflow graph for DNN training is mostly serial. Popular DNN systems such as TENSORFLOW and MXNET directly execute this dataflow on their backends. Hence, if a user wishes to parallelize training across devices, he or she must manually express the parallel computation in the user code so that the resulting dataflow graph generated has the required parallelism. Furthermore, users are also expected to explicitly specify placement, i.e. which device should be responsible for executing which portions of the dataflow graph. This is a tedious process.

2.2 Scaling challenges and trade-offs

**Data parallelism** is the widely-used method for scaling DNN training across many devices. It takes advantage of the fact that all training samples in one batch independently contribute to the gradients of the model parameters. Therefore, data parallelism partitions a batch of samples and lets each device compute the gradients of the same model parameters using a different partition. The resulting gradients are aggregated before updating the parameters. The aggregation and update can be done on each device by slicing parameters evenly, or on a separate device called a Parameter Server [20]. [43]. After the model parameters are updated, they will be replicated to all devices for the next iteration. This results in a Bulk Synchronous Parallel (BSP) approach to parallelizing the training algorithm (Figure 2).

Data parallelism has achieved good speedup for some DNN models (e.g. Inception network [4]). However, since the communication overhead of data parallelism increases as the model grows bigger, one must train using a very large batch size to amortize the communication cost across many devices. In fact, for any DNN model, one can always scale the “training throughput” by ever increasing the batch size. Unfortunately, large batch training is known to be problematic such as longer convergence time or decreased model accuracy [35].

**Model parallelism** partitions the model parameters of each layer among devices, so that the update of parameters can be performed locally (Figure 2). Each device can only calculate part of a layer’s activation using its parameter partition, so all devices need to synchronize their activations and activation gradients for each layer during both the forward and backward propagations. Since model parallelism exchanges activations instead of the model parameters, it works well for models with small activation size such as DNN models with large fully-connected layers.

The trade-off between data and model parallelism can be illustrated using an example as follows. Consider a MLP network with five fully-connected layers; each layer has 300 neurons; the batch size is 400. Therefore, all weight matrices are of shape $300 \times 300$ whereas activation matrices are of shape $400 \times 300$ (Figure 3). The model parameter size is $300 \times 300 \times 5 \times 4B = 1.8MB$, and the total activation size of forward propagation $400 \times 300 \times 5 \times 4B = 2.4MB$. When parallelizing training for this network on 16 GPUs, data parallelism needs to first collect all parameter gradients and then synchronize the updated parameters for all devices, so the total communication is $1.8MB \times 16 \times 2 = 57.6MB$, while model parallelism transfers activations and their gradients in both forward and backward propagations, so the total communication is $2.4MB \times 16 \times 2 = 76.8MB$. Data parallelism is better than model parallelism in this particular example because the total activation/gradient size is bigger than the total parameter size and data parallelism exchanges parameters across devices. If the batch size is 300 while the layer size is 400, model parallelism becomes better.

However, an even better strategy for this example is a hybrid of data and model parallelism as follows. The 16 GPUs are divided into four groups. We use data parallelism among groups, while within each group we apply model parallelism. The calculation of communication cost is then also divided into two parts. First, for data parallelism among groups, the communication is $1.8MB \times 4 \times 2 = 14.4MB$. Second, for model parallelism within each group, the communication is $\frac{2.4}{4}MB \times 4 \times 2 = 4.8MB$. Note that the activation size is reduced to $\frac{2.4}{4}MB$ due to data parallelism partitioning on the batch dimension. Finally, because there are four groups, the total communication is $14.4MB + 4 \times 4.8MB = 33.6MB$. This results in communication savings of 41.7% and 56.2% compared with pure data and model parallelism, respectively.

3. Our approach

Our insight to this challenge is that data, model and hybrid parallelism can all be unified as different tensor tiling
4. Finding the Optimal Tiling

Given a dataflow graph, SOYBEAN aims to find a tiling for each tensor in the graph such that the resulting parallel execution incurs minimal communication cost. There are three main challenges that SOYBEAN solves:

- **Optimize based on the dataflow:** In a dataflow graph, a tensor could act as the output of one operator as well as the input of another. Hence, a tiling that results in no communication for some operators may lead to more communications globally. For example, data parallelism requires no communication in forward and backward propagations, but the gradient aggregation part may be costly so that the overall communication cost is not minimized. SOYBEAN solves this by considering operators that share inputs or outputs together when searching for the optimal tiling. We also show that our algorithm could finish in polynomial time thanks to the sequential nature of deep learning algorithm.

- **Determine communication cost:** Given the tilings of the inputs and outputs, SOYBEAN needs to determine the corresponding communication costs. In SOYBEAN, we view communication as tiling conversions. Our core insight is that all the data needs to be fetched to the device before the operator can be executed. The process of fetching data from one location to another is in fact re-organizing the tiles and is thus equal to tiling conversion.

- **Decompose the optimization problem:** The problem of finding the best tiling for $n$ devices has a very large search space depending on $n$. SOYBEAN provides a recursive solution; it first finds the best tiling for partitioning the tensors among two devices. Then it recursively build upon its baseline solution to find tiling for $n > 2$ devices.

In this section, we first discuss the formulation of the tiling problem (Sec 4.1). Next, we describe how to find the optimal tiling across two devices (Sec 4.2) and build upon this baseline solution to tile across are more than two devices (Sec 4.3). We prove the solution’s optimality in Sec 4.4 and discuss extensions in Sec 4.5.

**Figure 3:** Overview of SOYBEAN’s design.

**Figure 4:** (a) Three basic tilings: row tiling, column tiling and replication; (b) Left: compose two basic row tilings into a four-way row tiling; right: compose row tiling and column tiling to partition matrix into four blocks.

We formulate the tiling problem to be solved by SOYBEAN. To ease the discussion, we only consider 2-D tensor (matrix) here. Extension to high-dimensional tensor is straight-forward and will be covered in section 4.5.

We first define the set of supported tiling schemes of a matrix. SOYBEAN only considers even tiling schemes that result in (sub-)tensors of the same shape and size, because...
we want to balance the computation across all devices. There are three basic tilings that divide a matrix computation into two equal parts: row tiling, column tiling and replication, as shown in Figure 4(a). Since all tiles are of the same shape, basic tilings can be applied again on each tile to further partition the matrix. We call this tiling composition. The result of a tiling composition is still an even tiling.

Let \( T^1 = \{R, C, r\} \) be the set that contains all basic tilings of a matrix, where \( R, C \) and \( r \) represent row tiling, column tiling and replication, respectively. We then define a \( k \)-cut tiling set that contains all possible tilings after \( k \) compositions as follows:

**Definition 1.** \( T^k = \{ t_1 t_2 | t_1 \in T^{k-1} \land t_2 \in T^1 \} \), \( \forall k \geq 2 \).

For example, a 2-cut tiling set \( T^2 \) is as follows:

\[
T^2 = \{ RR, RC, Rr, CR, CC, Cr, rR, rC, rr \}
\]

Figure 4(b) shows how 2-cut tilings RR and RC partition the matrix into four pieces. Note that a \( k \)-cut tiling partitions a matrix into \( 2^k \) pieces. To simplify the discussion, we assume the number of workers is \( n = 2^k \).

We then formally define the tiling of a dataflow graph:

**Definition 2.** The \( k \)-cuts tiling of a dataflow graph \( G \) is a function \( T_G : M \rightarrow T^k \) that maps from all the matrices \( M \) in dataflow graph to their tilings.

Given the above definition, we could unify data, model and hybrid parallelisms as different tilings of the dataflow graph (Figure 5). We explain why this is the case using the same MLP example in Figure 8.

- In data parallelism, all activations are partitioned along the batch dimension while all parameters are replicated. Suppose the batch dimension is the row dimension. Then data parallelism on two devices can be described by the following tiling:

\[
T_{data}(m) = \begin{cases}  \text{r} & \text{if } m \text{ is weight matrix,} \\  \text{R} & \text{otherwise.} \end{cases}
\]

- In model parallelism, the weight matrices are partitioned in order to avoid gradient aggregation among devices. For a 2D weight matrix, there are two possible tilings: \( R \) and \( C \). Suppose we choose row tiling. In order to compute the gradient of parameters locally, the activation matrices are partitioned along column while the activation gradients are replicated. Therefore, model parallelism on two devices can be described as following tiling:

\[
T_{model}(m) = \begin{cases}  \text{R} & \text{if } m \text{ is weight matrix,} \\  \text{C} & \text{if } m \text{ is activation,} \\  \text{r} & \text{otherwise.} \end{cases}
\]

- Hybrid parallelism divides all devices into groups. It supports one type of parallelism within a group and a different type across groups. This can be described as a composition of \( T_{data} \) and \( T_{model} \). An example tiling of hybrid parallelism on four devices is as follows. It performs data parallelism across groups and model parallelism within a group.

\[
T_{hybrid}(m) = \begin{cases}  \text{rR} & \text{if } m \text{ is weight matrix,} \\  \text{RC} & \text{if } m \text{ is activation,} \\  \text{rr} & \text{otherwise.} \end{cases}
\]

### 4.2 Tiling across two devices

We first solve the base case problem of finding the best tiling for two devices that minimizes communication. Let us consider the MLP model in Figure 8(b). If there are \( L \) layers, the forward propagation for computing loss value \( \mathcal{L} \) can be simplified as follows:

\[
\mathcal{L} = x_0 \prod_{l=1}^{L} W_l
\]

Here, we ignore the element-wise functions. \( x_0 \) is the input data and \( W_i \) is the weight matrix of layer \( l \). How to assign the tiling schemes for all matrices in this computation to minimize the communication cost? We first explain how to calculate the communication cost of one matrix multiplication given the tilings of its input/output matrices (Sec 4.2.1). Then we give an algorithm to optimize for the cost (Sec 4.2.2).

#### 4.2.1 Calculating the communication cost

Let us first consider only one matrix multiplication, \( X \times Y = Z \). What is the communication cost given the tilings of its inputs \( t_x \) and \( t_y \) and its output \( t_z \)?
the communication cost by computing the conversion costs of different tilings. However, since there are many types of input and output tilings, we do not want to enumerate all possible combinations to calculate the cost. Rather, we find a small set of so-called aligned tiling and reduce all tiling combinations to one of those cases. Aligned tilings may or may not correspond to real tilings. We use them to simplify the conversion cost calculation by drastically cutting down the number of cases we have to consider.

Given the three basic tilings, there are three corresponding aligned tilings, as depicted in Figure 6. For the left most tiling, the two inputs are row-partitioned and replicated, respectively and output is row partitioned. Similarly for the scenario in the middle. There is no communication cost for these two tilings. The third scenario is different in that its output tiling does not correspond to any basic tiling. Rather, the intermediate matrices computed on each device need to be aggregated later using an extra reduction operation. We denote this intermediate tiling as red.

All of the aligned tilings have several properties in common. First of all, they are all correct block matrix multiplications. Second, removing any submatrix product will give wrong results. Therefore, there is no redundant computation. Finally, they are balanced in that the number of submatrix products is equal to the number of devices.

One-cut Communication Cost: Let us define \( c(t_1 \rightarrow t_2) \) as the conversion cost from tiling \( t_1 \) to \( t_2 \). To compute the communication cost of a matrix multiplication, we calculate the minimum cost of converting the given input/output tilings to one of the three aligned tilings in Figure 6. To put it formally, the communication cost \( c(t_1, t_2) \) of a matrix with input tiling \( t_1 \) and output tiling \( t_2 \) is as follows:

\[
\text{min} \left\{ \begin{array}{l}
   c(t_1 \rightarrow r) + c(t_1 \rightarrow r) + c(r \rightarrow t_2), \\
   c(t_1 \rightarrow z) + c(t_1 \rightarrow z) + c(C \rightarrow t_2), \\
   c(t_1 \rightarrow C) + c(t_1 \rightarrow C) + c(red \rightarrow t_2) \\
\end{array} \right. 
\]

(2)

Computing the cost of tiling conversion is straightforward. It is equal to the area required for the local multiplication (which we refer to as “ghost area”) minus the area that already exists on the device. Figure 7(b) illustrates how an unaligned multiplication \( C \times r = R \) is computed through a conversion to an aligned multiplication \( R \times r = R \). The submatrix required for local computation is marked by the dashed line. The submatrix filled by yellow shading on device \( #1 \) needs to be fetched from device \( #2 \). Hence, its area is equal to the amount of communications involved in this tiling conversion.

4.2.2 One-cut tiling algorithm

Given a dataflow graph \( G \), the one-cut tiling algorithm finds a tiling across two devices (or groups), \( T_{\text{min}} : M \rightarrow T^1 \), such that the overall communication cost is minimized:

\[
T_{\text{min}} = \arg \min_T \sum_{o \in O_G} c(T(o_1), T(o_1), T(o_2)) 
\]

(3)
where $O_G$ represents all the matrix multiplications in the dataflow graph $G$, and $a_x$, $a_y$ and $a_z$ represent the input matrices and output matrix of a matrix multiplication $o$.

The central problem in searching optimal tilings is that changing the tiling of one matrix may affect many multiplications. Again, let us look at the MLP example. If we only consider the forward propagation part $L = x_0 \prod_{1 \leq i \leq L} W_i$, we can first calculate the communication cost of $x_1 = x_0 W_1$ under all the possible tilings of $x_0$, $x_1$ and $W_1$. We then proceed to the next multiplication $x_2 = x_1 W_2$, but when choosing $x_1$ to be tiling $t_1$, we should include the minimal cost of $x_1$ to be $t_1$ in the first multiplication. The total communication cost is then the minimal cost after we finish the last multiplication. When further taking the backward propagation part into consideration, two multiplications ($x_i = x_{i-1}W_i$ and $\frac{dC}{dx_{i-1}} = \frac{dC}{dx_i} W_i^T$) should be considered together, because the tiling of $W_i$ affects both multiplications.

Our tiling algorithm exploits an intuitive idea: operators that share inputs or outputs should be considered together. To achieve this, our algorithm first treats the dataflow graph as an undirected graph $G'$, and then uses a breadth-first search on this graph to organize graph nodes into a list of levels $L = \langle l_0, l_1, \ldots, l_n \rangle$. BFS puts nodes that share inputs or outputs in adjacent levels. We then use dynamic programming (DP) to search for optimal tilings:

**Initial condition:**

$$g_0(\tau_0) = \text{level_cost}_0(\phi, \tau_0)$$

**DP equation ($l \geq 1$):**

$$g_l(\tau_l) = \min_{\tau_{l-1}} \{ \text{level_cost}_l(\tau_{l-1}, \tau_l) + g_{l-1}(\tau_{l-1}) \}$$

Here, $\tau_l$ contains the tilings of all matrices that are shared among multiplications in level $l$ and $l + 1$. The level_cost is calculated by summing up the cost of each matrix multiplication in level $l$. The DP state $g_l(\tau_l)$ represents the minimal communication cost after executing all the operators from level zero to level $l$ and also partitioning matrices used by level $l + 1$ by tilings in $\tau_l$.

The algorithm searches for all possible tilings and therefore guarantees optimal. Unfortunately, the running time of the DP algorithm is exponential. Because all the operations are matrix multiplications, the node degree in the undirected graph $G'$ is at most three. According to Moore bound, if there are $N$ nodes in the graph, the diameter is $O(\log N)$. Since the number of BFS levels is equal to the graph diameter, the maximum number of nodes in each level is $O(N/\log N)$. Computing the total cost of each level needs to explore all tiling combinations of the inputs and outputs of the operators in that level. Therefore, the worst-case complexity of calculating level_cost is $|T|^3 O(N/\log N) = O(3^N)$.

The observation that saves us is that deep learning does not have an arbitrary dataflow graph. Rather, its graph usually has a large diameter. This is because training neural network usually involves computing each layer sequentially. For an $N$-layer MLP network, there are $3N$ matrix multiplications (forward, backward and gradient computation) and the diameter is $N$. In this case, the average number of nodes in each level is some constant $c$, so the average running complexity of the whole DP algorithm is linear, $O(3^cN)$.

### 4.3 Tiling across many devices

The $k$-cut algorithm finds the optimal tiling for $n = 2^k$ devices. It is a recursive algorithm. Specifically, we can divide $2^k$ devices into 2 groups, each with $2^{k-1}$ devices. We first use the one-cut algorithm to find the best tiling to partition the computation among the two groups. Within each group, we perform $(k-1)$-cuts to find the optimal tiling. Algorithm 1 shows the pseudocode.

In Algorithm 1, $P_k \circ T_k$ is the composition of two tilings (see Section 4.1). $\delta_k$ is the cost of the $k$-th cut. As each cut partitions computation into two groups, the cost of the subproblem is multiplied by two. The total communication cost is the weighted summation of per-cut costs:

**Theorem 1** (Total communication cost). $c_k = \sum_{i=1}^{k} 2^{k-i} \delta_i$

### 4.4 Proof of Optimality

Due to the limit of space, we only emphasize the key point that leads our proof. The core property that makes the $k$-cuts algorithm optimal is the commutativity of tiling composition because they are orthogonal ways of partitioning. If we let $R^k$ be the $k$-row tiling, then the $T^k$ tiling set could be rewritten as $T^k = \{ R^2, G^2, x^2, RC, Rh, Cr \}$. In fact, we have:

**Theorem 2** (Flattening).

$$T^k = \{ R^k, c^k : x^k | k_r, k_c, k_r \in \mathbb{Z} \land k_r + k_c + k_r = k \}$$

Let $T_k = \{ P_k, P_{k-1}, \ldots, P_1 \}$ be the tiling sequence generated by our $k$-cuts algorithm. We can also prove that the order of the tiling applied will not influence the total communication cost $c_k$. This gives us the following property:
Theorem 3 (Greediness). Let \( \delta_k, \delta_{k-1}, \ldots, \delta_1 \) be the cost of each tiling. We have \( \delta_i \leq 2\delta_{i-1}, \forall 2 \leq i \leq k \).

The greedy theorem means that for any tiling sequence \( T_k \) we can reorder it such that the contribution of the cost of each tiling is increasing. Suppose there is another tiling sequence \( T'_k \) that is not chosen by our algorithm but has \( c'_k < c_k \), we can prove that there must exist a “cross” step such that after that step, the remaining tilings in \( T'_k \) produces larger communication cost than the remaining tilings in \( T_k \). We can prove that by choosing the tiling at the “cross” step in \( T'_k \), it will give smaller cost than the one in \( T_k \) which contradicts to the local optimality of \( k \)-cuts algorithm.

4.5 Extensions to General Dataflow Graph

First, we extend the \( k \)-cuts tiling algorithm to high-dimensional tensors. We change the basic tiling set to \( T^1 = \{P_1, P_2, \ldots, P_d, \forall \} \) where \( P_d \) represents partitioning along \( d \)th dimension. The running complexity of the one-cut algorithm then becomes \( O((d + 1)^k N) \) given \( N \) nodes in the dataflow graph, which is still acceptable provided that \( d \) is usually small.

Second, we discuss how to handle operators beyond matrix multiplications. Recall that the communication cost is equal to the tiling conversion cost. The only information that is tied to operator type is the set of the aligned tilings of an operator. Here, we categorize operators for discussion. For element-wise functions (e.g. non-linear activation function), the only aligned computation method is to have the same tiling for all of the operator’s inputs and outputs. Note that having all of an operator’s inputs and outputs replicated is not allowed due to redundant computation. For convolution, the activation and parameter tensor sizes have four dimensions. Tiling on batch dimension leads to data parallelism while tiling on channel dimensions leads to model parallelism. Tilings on image and kernel dimensions are strictly worse than data parallelism so is ignored in our implementation. Note that the image and kernel sizes are in fact multipliers on the batch size and weight size, respectively. The larger the image size, the larger the activation tensor and thus the better data parallelism is. Finally, for all other operators, we only allow partitioning on the batch dimension, resulting in data parallelism. These changes should be easy since they only focus on the operator semantics while the complicated communication patterns will be automatically deduced by SOYBEAN.

5. Constructing the Execution Dataflow Graph

This section covers how SOYBEAN dispatches operators to different devices and how the semantic dataflow graph is converted to the execution graph given the \( k \)-cuts tiling schemes computed by our algorithm.

5.1 Tile Placement

The first consideration is load balancing. Fortunately, SOYBEAN’s tiling algorithm ensures that all tensors and operators in the dataflow graph are evenly partitioned, which means the workload is perfectly balanced.

Another consideration is the interconnects between devices. For example, GPUs within a single machine can be connected to different CPUs by \\( \text{PCI-e} \). Given the fixed total amount of communications, we want the majority of data transmission to be between GPUs attached to the same CPU to avoid the high latency of QPI connections. When scaling beyond one machine, this becomes more critical since network transmission is even slower. At a high level, the interconnection hierarchy divides devices into groups and encourages communications within each group. The \( k \)-cuts tiling algorithm naturally fits this scenario because each cut partitions the workload into two groups of devices; each group is then recursively partitioned. Theorem 3 indicates that SOYBEAN tends to partition groups such that the majority of communication happens within groups. Therefore, our placement strategy follows the algorithm structure. We map the workloads partitioned by the first cut to the groups connected by the slowest interconnects (e.g. Ethernet or QPI). We then continue mapping workloads within each group to the second slowest interconnects, and so on.

5.2 Connecting Partitioned Operators

The \( k \)-cuts tiling algorithm partitions each operator in the semantic graph into \( 2^k \) sub-operators. The inputs and outputs of these sub-operators are tiles (sub-tensors) of their original inputs and outputs. Therefore, to construct the execution graph is to connect the sub-operators for every connected operators in the semantic graph. Similar to the aligned matrix multiplication, this includes three phases:

1. We need to first convert the input tiling to the aligned tiling for the downstream operator. The tiling conversion dispatches each tile to the location specified by the placement. A simple solution is letting the receiver devices pull from the device that contains the area they need. The situation becomes complicated when the receiver only needs one slice of the sender’s data and needs to concatenate slices from multiple senders. In this case, we transfer the data in three steps. First, the flattening theorem (Theorem 2) allows us to represent each original tensor as a grid of tiles. Therefore, the sender can slice its own tile into shards such that each shard is dispatched to different receiver. Second, the receivers will fetch the shards they need from senders. Finally, the flattening theorem again allows the receiver to directly concatenate the received shards back to tiles.

2. Once the tiling conversions of inputs are done, all sub-operators can be executed locally by the definition of aligned tiling. Moreover, since all sub-operators are identical, we can just connect the input tiles to the sub-operators one by one.
3. The temporary outputs of the sub-operators again should be converted to the output tilings for later computation. This is the same process as the input tiling conversion.

6. Evaluation
In this section, we examine SOYBEAN’s performance. Specifically, we want to answer following questions:

1. Is communication really a bottleneck when using data parallelism with small batch sizes?
2. Can SOYBEAN reduce overall runtime?
3. How well does SOYBEAN accelerate modern DNNs?

6.1 Experimental Setup
We evaluated SOYBEAN on Amazon’s EC2 cluster. We used a p2.8xlarge instance, with 480GB of memory and 32 virtual CPUs as well as 8 NVIDIA GK210 GPUs on the instance. Each of the GPUs has 12GB of memory; they are connected by PCI-e, with a maximum peer-to-peer bi-directional bandwidth of 20GB/s.

6.2 Communication Overhead Evaluation
In this evaluation, we want to know if communication overhead accounts for a large percentage of the overall runtime when the batch size is relatively small or when the weight size is large. We first tested the runtime for data parallelism (DP), model parallelism (MP), and SOYBEAN with different parameters, i.e., batch size and weight size. To see the ratio of the communication overhead to runtime, we also modified MXNET’s backend to skip any communication, and re-ran our experiments. Thus, the runtime measured by the modified backend is solely due to computation. We can then determine the communication overhead by subtracting the computation time from the original runtime. Note that we report communication overhead instead of communication time because communication can be overlapped with computation. As a result, the communication overhead is strictly smaller than the communication time.

Figure 8(a) and Figure 8(b) show the runtime and communication overhead of a 4-layer MLP for different tilings on different numbers of GPUs. Both tests have the same weight size, 8192×8192, but different batch sizes, 512 and 2048, respectively. In Figure 8(a), the communication overhead for data parallelism increases as the number of GPUs increases. This is because a GPU needs to send its data to more GPUs when the total number of GPUs increases. However, the aggregate communication throughput is limited by contention on shared PCI-e resources, so it cannot increase linearly with several simultaneous peer-to-peer connections. As a result, increased GPU-to-GPU communication is slower, even below the PCI-e bandwidth limit.

In these two figures, data parallelism performs sq worse than MP and SOYBEAN. That’s because both communication overhead and computation time in data parallelism are larger than MP and SOYBEAN. We will show why different tilings may result in different computation time in Section 6.3. However, even if the computation time is the same as with MP and/or SOYBEAN, data parallelism is still slower. The key reason is the communication overhead is huge, ∼5× longer than the computation time on 8 GPUs with batch size 512, and ∼2.5× longer on 8 GPUs with batch size 2048.

Figure 8(c) uses the same batch size as Figure 8(b) but with larger weight size, 12288 (12K). Unlike changing the batch size, which significantly affects the ratio of communication overhead to total runtime, changing the weight size from 8K to 12K has little effect on the ratio. This is because when changing the weight size, both communication and computation increase for all parallelism schemes.

The results show that to achieve good performance, one should not use data parallelism when the batch size is small, due to the communication overhead. As the batch size increases, the percentage of the runtime consumed by communication overhead becomes smaller for data parallelism, and a crossover point will be reached when its runtime is lower than model parallelism on the same model and batch size. Because SOYBEAN can use hybrid tilings, it always achieves optimally low communication overhead.

We also performed the same evaluation for convolution neural networks. Figure 9(a) shows results from training a CNN with small (6px×6px) images with a large filter size (2K), while Figure 9(b) shows results from training with larger (24px×24px) images with a small filter size (512). We fixed the batch size to 256 for both experiments. The results show that with the larger image size, data parallelism has better performance than model parallelism. SOYBEAN still outperforms both partitioning schemes due to its ability to cut in different dimensions.

6.3 Can Shape Affect Computation Performance?

| Batch Size | Single GPU | Single GPU w/ SOYBEAN tilings |
|------------|------------|-------------------------------|
| 512        | 0.31s      | 0.19s                         |
| 1024       | 0.56s      | 0.39s                         |
| 2048       | 1.13s      | 0.73s                         |

Table 1: Runtime per batch comparison for a 4-layers MLP network between single GPU and single GPU with SOYBEAN partitions. The weight size is fixed to 8K×8K.

Figure 8 shows that the computation time varies with the tiling approach chosen. Regardless of the tiling, however, the total amount of computed data is the same. Therefore, we suspected that the shapes of matrices might affect the computation performance. To validate this assumption, we partitioned the input matrices into several sub-matrices by using SOYBEAN, but put all of them on single GPU. We achieved better performance with this approach than with using the un-cut matrices to do the same computation on a single GPU, as shown in table 1. We believe the difference
6.4 Scalability

Our goal is to achieve good performance regardless of the model and batch sizes; particularly difficult is good scalability with smaller batch sizes, which data parallelism does not achieve. In this section, we evaluate SOYBEAN’s scalability with two popular image recognition neural networks, AlexNet and VGG on 8 GPUs. We first trained each network on a single GPU to determine the maximum throughput (images/second). Using this throughput as baseline, we then calculated the speedup for different batch sizes.

Figure 10(a) shows the results with AlexNet. SOYBEAN achieves a greater than 7× speedup with a batch size of 256, while data parallelism requires increasing the batch size to more than 1K to achieve the same speedup. AlexNet consists of many convolution layers followed by fully connected layers. As discussed in Section 6.2, data parallelism needs a large batch size to achieve good scalability for fully connected layers. Moreover, Section 6.2 also shows that SOYBEAN can always achieve similar or better performance for convolution layers than data parallelism. As a result, SOYBEAN performs much better than data parallelism. VGG has similar structure to AlexNet but with more layers. Therefore, SOYBEAN can still achieve better scalability than data parallelism as shown in Figure 10(b). One may notice that in Figure 10(a), SOYBEAN can achieve superlinear speedup. This is because some matrix shapes fall into categories that have better computation performance after partitioning, as discussed in Section 6.3.

7. Related Work

How to distribute arbitrary data easily for users while achieving high-performance computation at the same time has been a popular research topic. However, it is difficult to design systems that automatically optimizes locality without knowledge of the underlying data and processing. Relatedly, distributed array programs are increasingly important due to the emergence of machine learning and deep learning. As a result,
significant effort has been expended in optimizing distributed array frameworks.

**Deep learning systems.** Many frameworks, such as TensorFlow [4], MXNet [13], PyTorch [2], Theano [10] and Caffe2 [22] have been proposed to facilitate developing new neural network models. These distributed array frameworks emphasize deep learning and machine learning applications. Besides the common array operations, they also provide many functionalities for neural networks such as automatic differentiation (backpropagation).

Though these frameworks allow users to develop models with both data parallelism and model parallelism, their interfaces are not friendly for utilizing model parallelism. SOYBEAN not only simplifies exploit model parallelism, but can automatically choose correct combinations of various parallelisms to reduce communication. Moreover, because of the similar design approach, performing optimizations over dataflow graphs, SOYBEAN can be implemented in these frameworks as long as they allow customized optimizations.

**General distributed programming frameworks.** Most distributed frameworks target primitives for key-value collections (e.g. MapReduce [19], Dryad [31], Piccolo [57], Spark [66], Ciel [50], Dandelion [61] and Naiad [51]). Some provide graph-centric primitives (e.g. GraphLab [44] and Pregel [47]). It is possible to implement a deep learning framework backend by augmenting an in-memory framework, such as Spark or Piccolo. When doing so, SOYBEAN can be applied to optimize the high-level data-flow graph before lowering the graph to the underlying framework.

**Distributed array frameworks.** Relational queries are a natural layer on top of key-value centric distributed execution frameworks, as seen in systems like DryadLINQ [65], Shark [64], Dandelion [61] and Dremel [48]. Several attempts have been made to build array interfaces on these. MadLINQ [58] adds support for distributed arrays and array-style computation to the dataflow model of DryadLINQ [65]. SciHadoop [12] is a plug-in for Hadoop to process array-formatted data. Google’s R extensions [62], Presto [63] and SparkR [3] extend the R language to support distributed arrays. Julia [1] is a newly developed dynamic language designed for high performance and scientific computing. Julia provides primitives for users to parallel loops and distribute arrays. Theoretically, one can use these extensions and languages to implement any neural network models. However, users have to manually deal with all optimizations provided by deep learning frameworks, like backpropagation (and with SOYBEAN, tiling).

Spartan [27] and Kasen [67] are two distributed array frameworks that perform automatic tiling on general array programs. Both systems provide primitives operating directly on arrays and thus expose the data access pattern of array operations that can be used for tiling optimization. Spartan proves that under such setting, automatic tiling is an NP-hard problem and provides only heuristic algorithms to find the best tiling. By contrast, SOYBEAN specifically targets deep learning systems and observes many fixed graph structures in neural network models. These fixed graph structures allow SOYBEAN to be able to find the optimal solutions in most cases. Moreover, SOYBEAN doesn’t rely on specific primitives, but directly optimizes array operations.

**Distributed array libraries.** Optimized, distributed linear algebra libraries, like LAPACK [5], ScaLAPACK [16], Elemental [56] Global Arrays Toolkit [53] and Petsc [7] expose APIs specifically designed for large matrix operations. They focus on providing highly optimized implementations of specific operations. However, their speed depends on correct partitioning of arrays and their programming models are difficult for use in deep learning.

**Compiler-assisted data distribution.** Prior work in this space proposes static, compile-time techniques for analysis. The first set of techniques focuses on partitioning [29]; the second on data co-location [37, 49, 55]. Prior work also has
examined nested loops with affine array subscript patterns, using different structures (vector [29], matrix [60] or reference [32]) to model memory access patterns or polyhedral model [45] to perform localization analysis. Since static analysis deals poorly with ambiguities in source code [6], recent work proposes profile-guided methods [17] and memory-tracing [54] to capture memory access patterns. Simpler approaches focus on examining stencil code [23–25, 36, 54].

Access patterns can be used to find a distribution of data that minimizes communication cost [9, 21, 28, 29, 59]. All approaches construct a weighted graph that captures possible layouts. Although searching the optimal solution is NP-Complete [34, 38, 41, 42], heuristics perform well in practice [42, 55]. DMLL [11] aims to extend a data-parallel programming mode to heterogeneous hardware. To achieve the goal, DMLL propose a new intermedia language based on common parallel patterns to partition data and distributed across the underlying heterogeneous distributed hardware.

SOYBEAN borrows many ideas from these works, such as constructing a weighted graph. However, unlike prior work that requires language-specific extensions and/or modification to capture parallel access patterns, SOYBEAN is designed to utilize the parallelism exposed by the underlying data-flow graphs, and can be quickly integrated with modern deep learning frameworks.

8. Conclusion

Deep learning systems have become indispensible in many fields, but as their complexities grow, DNN training time is becoming increasingly intractable. We demonstrate effective tiling in SOYBEAN that can achieve performance as good as or better than the best of data parallelism and model parallelism for many types of DNNs on multiple GPUs. With the speed and simplicity provided by SOYBEAN’s backend, users can train networks using frontends like TENSORFLOW and MXNET quickly and easily, making DNNs useful for a larger audience.

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