A Self-Regulated and Reconfigurable CMOS Physically Unclonable Function Featuring Zero-Overhead Stabilization

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Abstract—This paper presents a reconfigurable physically unclonable function (PUF) design fabricated in 65nm CMOS technology. Subthreshold-inverter-based static PUF cell achieves 0.3% native bit error rate (BER) at 0.062 fJ/bit core energy efficiency. A flexible, native transistor-based voltage regulation scheme achieves low-overhead supply regulation with 6 mV/V line sensitivity, making the PUF resistant against voltage variations. Additionally, the PUF cell is designed to be reconfigurable with no area overhead, which enables stabilization without redundancy on chip. Thanks to the highly-stable and self-regulated PUF cell and the zero-overhead stabilization scheme, a 0.00182% native BER is obtained after reconfiguration. The proposed design shows 0.12%±10 °C and 0.057%/0.1 V bit error across military-grade temperature range from -55 °C to 125 °C and supply voltage variation from 0.7 V to 1.4 V. The total energy/bit is 15.3 fJ. Furthermore, the unstable bits can be detected by sweeping body bias instead of temperature during enrollment, significantly reducing the testing costs. Last but not least, the prototype exhibits almost ideal uniqueness and randomness, with a mean inter-die hamming distance (HD) of 0.9986 and a 1020× inter/intra-die HD separation. It also passes both NIST 800-22 and 800-90B randomness tests.

Index Terms—Physically unclonable function (PUF), hardware security, key generation, security primitives, subthreshold, low cost, energy efficiency, voltage regulation

I. INTRODUCTION

Physically unclonable functions (PUFs) are increasingly studied and developed for secure electronic devices, especially for resource-constrained systems like Internet of Things (IoT) [1]-[3]. PUFs harvest intrinsic process variations of integrated circuits to generate keys and IDs unique to each device. It not only provides a low-cost solution to secure key generation and storage, but also offers attractive features such as bonding with specific hardware and tamper evidence, which makes them viable solutions for many emerging hardware security issues on supply chain tracking, counterfeit protection, system attestation, etc.

The generation and storage of secure keys are critical for entity authentication, secure communication, and serving as roots of trust for computing systems. Ubiquitous IoT devices face additional challenges because of varying environmental conditions and physical access by attackers. An ideal solution should exhibit the following three properties. First, non-volatile storage of the keys under voltage and temperature variations is necessary. Second, low cost and energy consumption are essential for IoT devices with constrained resource and battery lifetime. Third, robustness and alertness against physical tampering attacks is highly desired.

Non-volatile memories (NVMs) are the conventional solutions for secret key storage. NVMs include one-time programmable read-only memories (ROMs), fuses, and programmable flash memories. While NVMs provide excellent reliability and long-term data storage, NVM-based key storage solutions suffer from the following drawbacks: (1) Most NVMs require extra fabrication steps, adding to higher fabrication costs; (2) Conventional ROM, fuses and flash memories are all vulnerable to physical attacks, such as optical imaging techniques and direct probing; (3) Software vulnerabilities can also be exploited to gain access to keys stored in NVMs with standard I/O interface.

Physically unclonable function (PUF) is the most promising alternative to conventional NVM and is expected to meet all the desired properties for secure key storage. Firstly, PUFs use intrinsic process variations to generate and store the keys. The keys are stored in device characteristics, rather than direct digital data storage, making it more difficult to directly read out stored keys with tampering attacks. Moreover, PUFs exploit small device variations, which are believed to be sensitive to physical tampering and make PUFs tamper-evident. Secondly, the keys are unique to each chip due to the random and chip-specific nature of process variations during chip manufacturing. Therefore, no key programming is required and a known device is almost impossible, making PUF literally “unclonable”. Thirdly, silicon PUFs are low cost and easy to integrate with modern system-on-chip (SoC), because they only require standard CMOS devices and are easily portable across process nodes. Lastly, PUFs can be designed to be highly area and energy efficient, making them suitable for systems ranging from IoT devices to high-performance SoCs.

Generally, PUFs are categorized into strong and weak ones based on their capabilities. Strong PUFs [4]-[8] provide a large number of challenge-response pairs (CRP) for direct authentication, but existing designs have limited stability and randomness, leading to vulnerabilities against machine learning attacks [9]. Recent works explored circuit nonlinearity to improve resilience against machine learning attacks [6]-[7]. Weak PUFs have smaller capacity, but achieve higher stability against PVT variations and close-to-ideal uniqueness to provide reliable IDs and keys. This work focuses on weak PUFs and we do not differentiate strong and weak PUFs in the rest of the
The NAND chain design and differences

As shown in Fig. 1, a PUF usually comprises of four stages. The random mismatch of transistors or other components, acting as the entropy source, is extracted and digitized into a binary data. The raw PUF responses then go through stabilization process and error-correcting code (ECC) to remove and correct all unstable bits, providing 100% reliable keys for security applications. In theory, all bit errors can be corrected by reserving enough redundant bits for stabilization and ECC under a given bit error rate (BER). However, the redundancy and complexity increase super-linearly with BER. According to [10], the energy requirement for ECC to correct one-bit error in a 256-bit key equals to the energy of accessing over 200 PUF cells. Therefore, achieving higher stability at early stages of the whole PUF processing flow is the key to improve the overall PUF performance, demanding better PUF cell design and stabilization method.

PUF design involves entropy extraction and digitization. Various circuit techniques have been proposed for entropy extraction, including metastable cross-coupled inverters [11], power-up state of SRAM cells [12], delay lines [3], oscillators [5], current mirrors [13], PTAT references [14], and leakage-based transistor pairs [15]. Comparing these PUF designs, circuits with static operations avoid random noise associated with dynamic transients, generally providing more reliable responses. In terms of digitization, comparators shared by one column or the whole array were commonly deployed for lower area overhead, but the comparator must be designed with high gain and accurate offset cancellation, which incurs high power and complexity. Even microvolt offsets lead to biased PUF responses and reduced uniqueness. Moreover, even with optimal offset cancellation, shared comparators suffer from long wires and coupling effects.Comparatively, if the digitizer is integrated into every cell locally [16], comparator offset becomes part of the entropy source and will not affect PUF uniqueness. Complementary current mirror-based monostable PUF design is one of the first implementations to combine static operation and local digitization [13] [17]. This fully static design provides strong resiliency to environmental variations and random noise because of the absence of dynamic switching events, at the expense of higher standby power and larger PUF cell footprint. Another local amplification scheme is proposed in [16], where a NAND gate chain amplifies threshold voltage differences between neighboring stages. This design obtained lowest BER among all reported CMOS PUFs and a compact footprint, but it consumes high short circuit power. In [18], a chain of sub-threshold 2-transistor amplifiers further improves the NAND chain design and achieves best-in-class metrics.

Numerous stabilization techniques have been proposed to correct or discard error bits, which usually comes with area and time overheads. Temporal majority voting (TMV) and spatial majority voting (SMV) filter out random noise by taking multiple bits in time or space domain for a single bit output. While the complexity for TMV and SMV is low, the enhancement of stability is limited. Burn-in through intentional aging [11] [19] improves stability with little area overhead but incurs high testing cost. Another widely used stabilizing technique is to find and filter out unstable PUF cells during enrollment. However, long testing time with temperature sweep are necessary to find all unstable cells. It also requires redundant cells in the PUF array on chip for replacement and on-chip or off-chip storage of masking map. Lastly, ECC such as BCH code [11] [16] is capable of 100% stability at the expense of high computing complexity, high redundancy and long latency.

To further improve PUF stability without extra area, power, and throughput overhead and sacrifice of technology portability, this paper presents a self-regulated and reconfigurable PUF design with zero-overhead stabilization scheme [20]. It features three major advantages:

- Subthreshold inverter-based static and local digitization structure exhibits ultra-low power consumption, state-of-the-art native stability, and compact footprint.
- Native transistor-based regulation provides subthreshold supply voltage for PUF cells with low overhead and further improves PUF’s resistance to voltage variations.
- The proposed in-cell reconfiguration scheme enables 100 times BER reduction with no area overhead on chip.

The remainder of the paper is organized as follows. The proposed PUF circuit is presented in Section II. Section III explains modeling and implementation of the reconfiguration scheme for stabilization. In Section IV, measurement results are presented and discussed. Conclusions are drawn in Section V.

II. PROPOSED PUF CELL DESIGN

In order to achieve high stability with low area and power overhead, the proposed PUF cell employs a 4-stage subthreshold inverter chain for entropy extraction and digitization. The following metrics are evaluated to determine the best PUF design (Fig. 2).

- **Mismatch:** The difference in threshold voltage between neighboring transistors.
- **Digitize:** The process of converting the extracted entropy into a binary format.
- **Stabilize:** The process of correcting and stabilizing the raw PUF responses.
- **ECC:** Error-correcting code used to remove and correct all unstable bits.

The design achieves a high level of entropy extraction and digitization while minimizing area, power, and complexity. The proposed PUF cell topology, comparison of 2-transistor amplifier-based cell and proposed subthreshold inverter-based cell, simulated histogram of voltages at each stage, voltage gain of 2-transistor amplifier and subthreshold inverter in different technology nodes.
amplification, inspired by the static and local digitization designs in [16] and [18]. As shown in Fig. 2, the input and output of first stage is shorted, setting its voltage to a switching point with high gain. Mismatch between switching voltages of successive stages is amplified to full rail after a few stages. This PUF structure eliminates the impacts of non-ideal comparators and noise during dynamic transitions, leading to higher stability. However, the use of NAND gates at nominal VDDs incurs high power consumption and 2-transistor amplifiers are found to be less effective at more advanced technology nodes than 180nm. The following subsections will discuss the use of subthreshold inverters, low-overhead supply regulation of the PUF cell, and system implementation of the PUF module.

A. Subthreshold Inverter Based PUF Cell

The stability of PUFs based on a chain of amplifiers depends on the distribution of switching voltage mismatch and the amplification gain of each stage. Firstly, higher gain improves overall PUF stability over environmental variations because less stages are involved in deciding the final responses. Secondly, larger mismatch variations apparently reduce the probability of having an unstable cell. Thirdly, if the gain around the switching voltage is asymmetrical, the PUF response will be biased towards one value and the overall randomness is affected. It is found that the 2-transistor amplifier in [19] shows reduced voltage gain at more advanced process nodes because of decreased output impedance. Because an off-transistor is used to bias the amplifier, the switching voltage is close to the supply voltage, leading to unbalanced gain and headroom.

As shown in Fig. 2, we propose the use of thick-oxide inverters under sub-threshold supply voltage, which provides higher gain and balanced output while consuming low static power. It is shown in Fig. 2(c) and Fig. 3 that as technology nodes scales, subthreshold inverter consistently yields higher voltage gain than 2-transistor amplifier, and shows symmetrical gain and headroom. Therefore, the proposed PUF cell achieves higher native stability, better randomness, and better portability to different process over the 2T-amplifier design in [19].

B. Voltage Regulation using Native Transistors

Stable and efficient low voltage supply is required for the subthreshold inverter-based PUF cell for stability and low energy consumption. One of the main sources of instability for PUF comes from voltage variation, especially in subthreshold PUF designs [8]. IR drop, EM interference and other incidents can cause fluctuation of supply voltage in PUF cells.

A conventional approach to provide a regulated low supply is to use a low-drop-out regulator (LDO). LDOs have quiescent currents, leading to low efficiency and large area overhead when the load is light. PUFs can be offered in either a large array or as small embedded key registers. Thus, a more scalable and low-overhead supply regulation is desired for our proposed PUF circuits.

Inspired by a threshold-based voltage reference [21], this work utilizes a native transistor to self-regulate supply voltage with low area and power overhead. The voltage regulation works on the basis that the cell is biased in subthreshold region. The first stage consumes most of the current and the rest stages are almost in cutoff region. Therefore only the first stage is considered in the following calculations. The equivalent model is shown in Fig. 4. The subthreshold region currents of $M_0$ and $M_2$ are derived in (1) and (2), according to [21], where $I_{\text{sub}}$ denotes the cell current flowing through $M_0$, $M_1$ and $M_2$ and should be equal in (1) and (2). $V_M$ denotes the switching voltage of stage 1. $V_{DD}$ denotes the regulated virtual supply voltage of the inverters.

$$I_{\text{sub}} = \mu C_{OX} \frac{W_0}{L_0} (m_0 - 1) V_T^2 \exp \left( \frac{V_{OUT} - V_{DD}}{m_0 V_T} \right) \left( 1 - \exp \left( \frac{V_{OUT}}{V_T} \right) \right) \tag{1}$$

$$I_{\text{sub}} = \mu C_{OX} \frac{W_2}{L_2} (m_2 - 1) V_T^2 \exp \left( \frac{V_{OUT} - V_{DD}}{m_2 V_T} \right) \left( 1 - \exp \left( \frac{V_{OUT}}{V_T} \right) \right) \tag{2}$$

$V_{DS}$ in (1) and (2) are by magnitude larger than $V_T$ thus the last terms can be neglected. To simplify the model, it is assumed that $V_M$ is half of $V_{DD}$. In real design, $V_M$ does not necessarily need to be exactly half of $V_{DD}$.

$$V_M = \frac{1}{2} V_{DD} \tag{3}$$

Fig. 3. Comparison of (a) gain and (b) voltage histogram between 2-transistor amplifier and subthreshold inverter.
The equation for $V_{DD}$ can be derived in (4), showing independence of supply voltage. Moreover, since thermal voltage is proportional to temperature and threshold voltage is complementary to temperature. The temperature effects of the transistors on $V_{DD}$ can be cancelled by carefully sizing the native transistor.

$$V_{DD} = \frac{2m_0m_2}{m_0 + m_2} V_T \ln \left( \frac{\mu_C W_0 L_0 (m_0 - 1)}{2 \mu_C W_0 L_0 (m_2 - 1)} \right) + \frac{2m_2}{m_0 + m_2} V_{DHD} + \frac{2m_0}{m_0 + m_2} (V_{BIAS} - V_{TH})$$

(4)

Further area saving is achieved by column-wise sharing of the native regulation transistor in this design. The flexible configuration of the native regulation transistor can adapt to cell-wise, column-wise and array-wise regulation. In the proposed design, each column of 32 cells share a native regulating transistor. The $V_{DD}$ equation for this case is modified as in (5).

$$V_{DD} = \frac{2m_0m_2}{m_0 + m_2} V_T \ln \left( \frac{\mu_C W_0 L_0 (m_0 - 1)}{3 \mu_C W_0 L_0 (m_2 - 1)} \right) + \frac{2m_2}{m_0 + m_2} V_{DHD} + \frac{2m_0}{m_0 + m_2} (V_{BIAS} - V_{TH})$$

(5)

C. System Implementation

The block diagram of this design is depicted in Fig. 5(a). A 32 by 128 array is implemented. SRAM-style peripherals are integrated to allow for parallel and high-speed readout. Each column shares the same virtual supply voltage regulated by a native transistor. Readout process involves BL pre-charging, WL enabling, voltage sensing through a single-ended sense amplifier (SA), and latching of the result. A waveform for reading operations is included in Fig. 5(c).

III. ZERO-OVERHEAD RECONFIGURATION SCHEME

Conventional stabilization methods, as discussed before, could not achieve good balance between overhead and stabilization effect. A zero-overhead reconfiguration scheme is proposed to stabilize the PUF cell. The scheme is based on the specific structure of the proposed PUF cell, and can be enrolled with low testing cost. In this work, the $V_M$ difference between the first two stages is the entropy source. Cell-level reconfiguration involves transistor merging and converting the original cell into a new cell with independent performance.

A. Source of Instability

The entropy source of PUFs is the local mismatch due to process uncertainty. The randomness in dopant distribution, lithography, gate thickness causes variations of transistors. Ideally the switching voltages of two inverters within the same PUF cell should be fixed, leading to a stable ‘1’ or ‘0’ output. However, the actual mismatch can be altered or even flipped under voltage and temperature variations, especially when the original mismatch is small. This is caused by the fact that different transistors exhibit varying environmental sensitivities.

Monte-Carlo simulations of 10,000 proposed PUF cells are performed to investigate the cause of instability. More focus is put on temperature variations because the proposed native voltage regulation suppresses the impacts of voltage variation. Simulation results show that 96 out of 10,000 cells have unstable output under -55 °C to 125 °C temperature sweep. The histogram of switching voltage differences of stage1 and stage2 illustrate that all the 96 unstable cases have switching voltage differences smaller than 3 mV, as shown in Fig. 6. Conclusion can be drawn from above discussions that small mismatch is a necessary condition for an unstable PUF cell.

B. In-Cell Reconfiguration

The reconfiguration process is shown in Fig. 7 to further illustrate the source of instability and explain the proposed stabilization scheme.

An originally unstable cell has small mismatch between the first and second stage. The switching voltages of the first three stages of this cell are denoted by $V_{M1}$, $V_{M2}$ and $V_{M3}$ respectively. $V_{M1}$ and $V_{M2}$ are close to each other in nominal condition and are likely to flip their relative difference under

| Cell Mismatch | Probability | Action | Output |
|---------------|-------------|--------|--------|
| $V_{M1} \neq V_{M3}$ | 0.5*P_n | Stay | ‘1’ |
| $V_{M1} = V_{M2} \neq V_{M3}$ | 0.5*P_n | Stay | ‘1’ |
| $V_{M1} = V_{M2} = V_{M3}$ | 0.5*P_n | Reconfigure | ‘1’ |
| $V_{M1} = V_{M2} < V_{M3}$ | 0.5*P_n | Reconfigure | ‘0’ |
| $V_{M1} = V_{M2} > V_{M3}$ | 0.5*P_n | Reconfigure | ‘0’ |

Fig. 6. (a) Histogram of switching voltage ($V_M$) difference from 10000 Monte-Carlos simulations, (b) from 96 unstable cases.

Fig. 7. (a) Process of in-cell reconfiguration of an unstable cell, (b) the switching voltages of an originally unstable cell before and after reconfiguration.

Fig. 8. Reconfigurable PUF cell in (a) layout, (b) schematic views.
V/T variations. Based on the observation that local mismatch is purely random, the reconfiguration scheme is proposed by combining the first two stages as a new first stage. The output of the reconfigured cell depends on the difference of the combined new stage and the third stage. The subthreshold inverter-based cell has a low bit error rate. Thus, the probability of V_M1 and V_M2 being close is low. For the reconfigured cell, the necessary condition of it being unstable over V/T variations is that V_M1, V_M2 and V_M3 are all close to each other. The probability is extremely low in the proposed design.

Table I describes the probabilistic model of the reconfiguration scheme. P_0 and A_VO denotes the probability of unstable bits and gain for original cell. P_R and A_VF denotes the probability of unstable bits and gain for reconfigured cell. V_M and σ is the mean and standard deviation of a subthreshold inverter switching voltage. The bit error rate and voltage gain have a relationship of f(A_V). The probabilistic model of the process in shown in Table I. The switching voltages of the original cell and reconfigured cell exhibit the following distribution. It is assumed that transistor threshold voltage V_M is independent and identically distributed.

\[ V_{M1}, V_{M2}, V_{M3} \sim N(V_{M0}, \sigma) \]  
(6)

According to [22], the standard deviation of threshold voltage is inversely proportional to transistor area, which leads to equation (7).

\[ V'_{M1} \sim N(V_{M0}, 0.707\sigma) \]  
(7)

V'_{M1} denotes the switching voltage of stage1 in the reconfigured cell. V_{M*} denotes the mean of a combined subthreshold inverter’s switching voltage. The difference of switching threshold voltage between the first two stages can be derived in (8) and (9) for the original and reconfigured cell.

\[ V_{M1} - V_{M2} \sim N(0.141\sigma, \sigma) \]  
(8)

\[ V'_{M1} - V_{M3} \sim N(V'_{M1} - V_{M3}, 1.224\sigma) \]  
(9)

The probability of unstable bits is inversely proportional to the standard deviation of first two stages’ switching threshold voltage difference.

\[ P_0 \propto \frac{f(A_{\text{VO}})}{|\text{Var}(V_{M1} - V_{M3})|^2} \]  
(10)

\[ P_R \propto \frac{f(A_{\text{FO}})}{|\text{Var}(V'_{M1} - V_{M3})|^2} \]  
(11)

From (10) to (11), P_R is estimated to be 1.15 * f(A_VO)/(f(A_VO)*P_0). In measurements, the portion of cells requiring reconfiguration is 4% under -55 °C to 125 °C temperature variation and 0.7 V to 1.4 V supply voltage variation. The reconfigured cell has slightly higher BER than the original cell due to decreased mismatch induced by doubled size of the first stage [22]. Reduced gain due to reduced number of stages also induces higher instability. However, the overall probability for a cell to be unstable is the product of the two probability in theory, which is 0.44% in measurement.

**C. Physical Implementation of Reconfiguration Scheme**

The benefit of the proposed reconfiguration scheme is its low cost in this specific design. To combine the first and the second stage, an NMOS transistor is inserted between the drains of the two NMOS. Fig. 8 depicts the physical insertion of the reconfiguration transistor. In 65nm CMOS process, no area overhead is added under the design rules. In most technologies, the area overhead is also expected to be small. The reconfigure transistor is driven by full swing signal to connect two stages.
IV. MEASUREMENT RESULTS

The chip is fabricated in 65nm CMOS process. The 32 by 128 cells array occupies 0.018 mm². The die micrograph and the layout of the PUF cell are shown in Fig. 10. Each PUF cell measures 0.96 μm by 2.475 μm, or 562 F². Clock generator is integrated to provide high-speed clocking for key access.

The nominal condition for the PUF chip is 27 °C and 1.2 V supply voltage. Golden keys are collected at nominal condition by averaging our random noise with many samples. BER and and works at nominal condition, eliminating the need for expensive and time-consuming temperature sweep.

The comparison of the proposed reconfiguration scheme and conventional methods is listed in Table II. It is highly effective with no on-chip area overhead, while adding low runtime latency and moderate test cost with the help of body bias.

A. Voltage Regulation

The reliability of the proposed native regulation is essential to the quality of the PUF. $V_{DD}$ is measured across supply voltage and temperature sweep to evaluate the efficacy of native regulation. The measured line sensitivity of $V_{DD}$ is less than 6mV/V over supply voltage range of 0.7 V to 1.4 V. Additionally, $V_{DD}$ shows less than 10mV variation across -55 to 125 °C. For testing purpose, bias voltage is provided through off-chip source. For system-level applications, it can be generated by a 2-transistor voltage reference [21] which is also robust against voltage and temperature variations. No extra current is consumed for voltage regulation with the use of native transistor regulation.

B. Native PUF Stability

The bit error rate (BER) and the proportion of unstable bits of 5 chips, measured at nominal condition before and after stabilization, are depicted in Fig. 12. BER denotes rate of bit flips over evaluations compared with golden value and unstable bit denotes percentage of ever-flipped bits. The definitions are adopted from [15]-[18] for fair comparison. It should be noted that the proportion of unstable bits increases as the number of evaluations increases re shown for fair. The native BER reaches
BER is reduced optimizes the stability can be obtained at the cost of higher testing cost. Unstable cells under temperature variation this only achieves 25% BER improvement is achieved with low-overhead TMV11 and in-cell reconfiguration schemes.

C. PUF Stability over Voltage and Temperature Variations

The stability of the proposed PUF is evaluated under the military-grade temperature range from -55 °C to 125 °C. The bit error rate (BER) over temperature sweep is 4.26% before stabilization. TMV and reconfiguration are applied to improve stability. Fig. 14(a) presents BER across temperature variation when different stabilization methods are applied. By detecting unstable bits under room temperature, a portion of bits that will be unstable over temperature variation is filtered out. However, this only achieves 25% BER reduction. Since unstable cells under temperature variation are not necessarily natively unstable cells. Filtering out all unstable cells by sweeping temperature during enrollment achieves the highest stability, reducing BER to 0.44%. The remaining errors are caused by random noise and cannot be stabilized, the stability is still among best in class. For stability-first applications, higher stability can be obtained at the cost of higher testing cost.

The proposed body-bias sweeping approach, named EVB, optimizes the tradeoff between stabilization effect and cost. BER is reduced to 2.27% by sweeping p-well biasing voltages (VPW) from -0.4 V to 0.4 V searching for unstable bits for reconfiguration. The process does not involve temperature sweeping thus has much lower testing cost than searching the full temperature range.

Fig. 15 shows the detection rate and BER improvement of EVB at different VPWs. The detection rate is defined as the ratio of number of truly unstable bits across temperature variation filtered by EVB, over the number of total filtered bits by EVB at one VPW. Higher detection rate is observed for low VPW. This is expected because low VPW filters out cells with small mismatch, which is more likely to flip when temperature changes. Although detection rate lowers as body bias voltage rises, the overall stability still improves as shown in Fig. 15(b). High VPW filters out additional cells with larger mismatch, which will still flip under temperature variation, but with a lower probability. The BER improvement curve shows that positive VPW is more effective for high temperature while negative VPW is more effective for low temperature. This proves the assumption that the main source of entropy is mismatch of threshold voltage. Since positive VPW and high temperature both decrease threshold voltage, and negative VPW and low temperature both increase threshold voltage.

In addition to temperature variation, we also evaluate the PUF’s resistance to supply voltage variation from 0.7 V to 1.4 V. Only 0.4% BER is observed across the voltage range, thanks to the supply regulation based on native transistors.
D. Uniqueness and Randomness

The inter-die and intra-die hamming distance distributions are depicted in Fig. 16. The inter-die hamming distance measured over 10 chips has mean value of 0.4998 which is near-ideal. The mean intra-die hamming distance before stabilization is 0.0047, achieving 106 times separation between inter- and intra-die hamming distances. After stabilization (reconfiguration followed by TMV), the intra-die hamming distance is 0.00049, showing state-of-the-art identifiability. The autocorrelation of 40960 PUF bits with the 95% white noise confidence level at 0.01385 is shown in Fig. 17. The near-ideal hamming distance and autocorrelation results validate the uniqueness of the proposed PUF.

To further evaluate the randomness of PUF responses, NIST 800-90B [23] and 800-22 [24] randomness test suites are performed on 40,960 bits collected from 10 chips. With the limited number of bits, 10 out of 15 subtests in 800-22 are available. NIST recommended settings were used to run the tests. More detailed definition and explanations of the testing parameters can be found in [23] [24]. The PUF bits passed all available sub-tests in the two suites, showing high-quality randomness as shown in Table III and Table IV.

E. Aging Effects

Another factor to consider for PUF stability is aging. Aging degrades PUF stability or completely flip bits. The main sources of aging effects in PUF are NBTI and HCI [14] [17] [25] [26]. To evaluate aging impacts, accelerated aging is applied by stressing the PUF at 150 °C and 1.4 V supply voltage. Every 12 hours, measurement was taken at nominal condition. A stressing of 108 hours in total was applied, resulting in equivalent effects as several years’ aging under nominal condition. Since this design works in subthreshold region, it is expected to suffer minor aging effects. The measured aging-induced instability shown in Fig. 18 is similar to previously best reported results [14] [17].

F. Throughput and Energy Efficiency

The design reaches 8.592 Mb/s readout throughput in high performance (HP) mode and 1.459 Mb/s in low power (LP) mode. This is enabled by SRAM-style array and readout peripheral. The subthreshold operation consumes 0.076 fJ/bit core energy. The total energy including that of core and peripheral circuits is 25.6 fJ/bit in HP mode and 15.3 fJ/bit in LP mode. The throughput and energy efficiency curves versus VDD are depicted in Fig. 19. The throughput and energy efficiency were measured at nominal condition. Since the circuits work in subthreshold region, transistor current
increases with temperature exponentially. Native transistor-based regulation suppresses supply voltage-induced influence on current.

G. Related Works and Comparison Table

As shown in previous sections and Table V, the proposed PUF shows state-of-the-art native stability, area, and energy efficiency. The zero-overhead stabilization method further improves the stability of the PUF without the use of redundancy-based ideal masking and ECC.

Emerging NVM-based PUFs using anti-fuses and RRAMs [27] [28] provides almost zero BER by randomly generating keys and storing them in memories. This class of PUF does not preserve the sensitivity to tampering as in CMOS PUFs and usually require extra fabrication steps and high testing costs. Thus, these designs are not included in the comparison table but they represent a new promising direction in PUF design.

V. Conclusion

In conclusion, this paper presents a self-regulated PUF based on a subthreshold inverter chain, achieving 0.3% native BER and 0.076 fJ/bit energy efficiency. Native regulation provides resistance to supply voltage variation and lead to 0.057 %/0.1 V BER sensitivity against voltage variations. The proposed in-cell reconfiguration scheme reduced native BER by two orders of magnitude to 0.00182% with no area overhead. Moreover, a fast searching method of emulating temperature variation by sweeping body bias is applied to locate unstable bits with low testing cost. The PUF prototype in 65nm occupies only 562 F² per bit. Measured responses from 10 chips pass all applicable NIST 800-22 and 800-90B randomness tests and show 1020 times separation of intra/inter-die Hamming Distances after stabilization. The design achieves best-in-class metrics in all desired properties, making it suitable to provide low-cost, high-performance key generation and storage for a wide range of applications.

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