The High Precision Capacitance Array in 16-bit SAR ADC

Yong-Kai Li, Xu Qi, Ping Yang\textsuperscript{a}, Yuan-Jun Cen\textsuperscript{b}, Da-Gang Li, Zhi-Kai Liao
Chengdu Sino Microelectronics Technology Co., Ltd., Chengdu 610000, China
*Corresponding Author: \textsuperscript{a}yangping217@126.com, \textsuperscript{b}chengduhuawei@126.com

Abstract. In SAR ADC, the capacitance array is a very important unit, it will determine the conversion performance of the whole ADC. In normal semiconductor foundry, the matching precision of the linear capacitor is always about 10 bit, so it is not impossible to realize the 16-bit conversion precision in normal COMS foundry. This paper introduces a new design, for getting a smaller layout area, the main body frame of capacitor array uses the M+N+L bit sectional type; For getting the high matching precision performance, the lower bridging capacitor will be the normalized capacitor; For getting the high conversion precision, all the Upper-Bit in capacitance array will add a sub-calibrated capacitor array. So in this paper, it uses the circuit structure to realize the high precision capacitor array in 16-bit SAR ADC.

1. Introduction
For A/D converter, it can realize the analog signal convert to digital signal. The SAR ADC is a typical high resolution ADC, it’s capacitance array is the most important unit, the conversion performance of this unit will directly determine the whole system’ conversion performance.

For N bit SAR ADC, the typical design of SAR capacitance array is as Fig. 1 [1] [2]

In this paper, for easy to describe, unless otherwise noted, the ADC is almost the SAR ADC, the number of Q always equal to 1, or 2, ..., or N.

In Fig. 1, the amount of unit capacitor in capacitance array is almost $2^N$. In 16-bit SAR ADC, the amount of unit capacitor is almost about $2^{16}$, so it is not impossible in layout area.

From the above all, referring to 16-bit SAR ADC, the design of Fig. 1 can not be realized in detail project design. For giving consideration with performance and layout area, the M+N+L bit sectional type capacitance array is used in 16-bit ADC in this paper. The typical design of M+N+L bit sectional capacitance array is as Fig. 2 [1] [2]

In Fig.2, if the number of L is the biggest number in M, N and L, the whole amount of the capacitors in capacitance array is about $2^L$, it will be more less than $2^{16}$. So in layout design, it is impossible.
In semiconductor foundry, the high matching precision of linear capacitor array should be all constituted by the unit capacitors. But in Fig.2, the Bridging capacitors C_1 and C_2 are all not the unit capacitor, in other word, the capacitors C_1 and C_2 all will be mismatch with theory capacitor. So for getting the 16-bit conversion precision performance, the BIT(M+1) ~ BIT(M+N+L) all need an independent sub-calibrated capacitance array.

In Fig. 2, the matching precision of capacitance array only need M-bit, it is usually less than the best matching precision of linear capacitor in foundry. In other word, the circuit of Fig.2 will not use the advantage of linear capacitor, and the amount of sub-calibrated array will also be too much.

2. The Circuit of Improved Capacitance Array

2.1. The design of normalized bridging capacitance C_1

For normal semiconductor foundry, the nature matching precision is about 10-bit, so in this paper, it makes 5+5+6 bit (M=5, N=5, L=6) sectional type to realize the 16-bit SAR ADC. It means if the Bridging capacitor C_1 is the unit capacitor, there will not need any sub-calibrated array in BIT(1) to BIT(10). So next it will introduce a design to realize C_1 to normalized capacitance.

Referring to 10-bit SAR ADC, the design of Fig. 1 is as Fig. 3.

If it makes M=5, N=5, the design of Fig. 2 is as Fig. 4 [3]

![Figure 3. The typical design capacitance array of 10-bit ADC](image)

![Figure 4. The typical 5+5 bit sectional capacitance array](image)

In Fig. 3 and Fig. 4, if BIT(1) is the LSB, BIT(10) is the MSB, the unit capacitors number of BIT(Q) is Num(Q). Referring to any number of Q, it always should satisfy the follow expression:

\[
(\text{Num}(1)+\text{Num}(2)+\cdots+\text{Num}(Q))/\text{Num}(Q+1)=(2^Q-1)/2^Q
\]

From the Expression (1), it can get the finally design of normalized bridging capacitance. The improved capacitance array is as Fig. 5

![Figure 5. The improved 5+5 bit sectional capacitance array](image)

From the theory calculated, it can easily get:

In Fig. 5, referring to any number of Q, it always satisfies the Expression (1).

2.2. The design of main-capacitance array in SAR ADC

In Fig.5, the capacitors in the array are all the unit capacitor, and the nature matching precision is about 10-bit in normal semiconductor foundry, so the capacitance array in Fig.5 can realize the 10-bit conversion performance without any calibrated unit.

In this paper, for getting the 16-bit conversion performance, it should add the sub-calibrated capacitance array in every 6 MSB, the finally 16-bit capacitance array is as shown in Fig.6.
Figure 6. The improved 5+5+6 bit sectional capacitance array

In Fig.6, the bridging capacitor $C_1$ is the normalized capacitor, the bridging capacitor $C_2$ is equal to 1.03125 times of unit capacitor. For guaranteeing the 16-bit conversion performance, the minimum of calibrated step of sub-calibrated array should be set by 0.25LSB.

2.3. The design of sub-calibrated array
Because the nature matching precision is about 10-bit in normal semiconductor foundry, for getting the 16-bit conversion performance, the 6-MSB all need an independent sub-calibrated array, the minimum calibrated step will be set by 0.25 LSB in sub-calibrated array.

For releasing the unit capacitor in capacitance array, the amount number of BIT(11) will be set by 1 unit capacitor. If the number of $Q$ is 11 ~16, the sub-calibrated array of BIT(Q) is as Fig.7. If the number of $Q$ is equal to 11, the Switch of MSB of BIT(11) is $S_7$, the Switch of LSB is $S_1$ in Fig.7. If the $S_1$ is connect to BIT(11), the equivalent of capacitance of BIT(11) will add $(1/128)*(1/32)$ times of unit capacitor. From the basic analog theory, it means that the conversion precision of BIT(11) will be equal to add 0.25LSB. From the same reason, when $S_7$ is connect to BIT(11), the conversion precision of BIT(11) will be equal to add 16LSB.

When $Q$ is equal to 12 ~ 16, it also can get the similarly conclusion.

From the above all, it can get the follow conclusion:
The minimum of calibrated step of sub-array are all the 0.25LSB at all the BIT(11) ~ BIT(16).
The maximum of calibrated step of sub-array are $2^{11-Q}$ LSB at the BIT(Q).

3. The Simulation and Verification
In order to verify the function of sub-calibrated array, it uses the design of Fig. 6 replacing the capacitance array of a 16-bit SAR ADC. In this paper, it uses the Cadence software to simulate the SNR and SFDR of the ADC schematic. The simulated condition is $V_{DD}=5V$, $V_{GND}=0V$, $V_{REF}=2.5V$, $V_{IN}=0~2.5V$. The 16-bit ADC’ functional block diagram is as Fig. 8.

From the basic analog theory, the maximum mismatch always happens in $C_2$ and BIT(16) in Fig.6, so for verifying the sub-calibrated array, next it should simulate the different situations when $C_2$ and BIT(16) are match or mismatch capacitors.

For easily comparing the conversion performance between match and mismatch capacitance array, it will simulate the SNR, SFDR, DNL in BIT(11) and BIT(16) of ADC in different situation.

Figure 8. The functional block diagram of 16-bit ADC

3.1. The Simulation of no-mismatch capacitors in main capacitance array
In Fig. 6, all the unit capacitors will be set by 434.4f F, the bridging capacitor $C_2$ is 447.975f F.
The SNR of no-mismatch capacitance array is 84.9 dB, the SFDR is 90.3 dB.
The simulation result is as Fig. 9

![Figure 9](image.png)
Figure 9. The dynamic performance of no-mismatch capacitance array

The DNL\textsubscript{BIT11} of not any mismatch capacitance array is about 1 LSB.
The DNL\textsubscript{BIT16} of not any mismatch capacitance array is about 1 LSB.

3.2. The Simulation of mismatch bridging capacitor $C_2$ in main capacitance array
In Fig. 6, all the unit capacitors will be set by 434.4f F, the bridging capacitor $C_2$ is 450.9f F.
The SNR of mismatch bridging capacitor $C_2$ is 66.5 dB, the SFDR is 77.2dB.
The simulation result is as Fig. 10

![Figure 10](image.png)
Figure 10. The dynamic performance of mismatch capacitor $C_2$

The DNL\textsubscript{BIT11} of mismatch bridging capacitor $C_2$ is about 6 LSB.

3.3. The Simulation of calibrated bridging capacitor $C_2$ in main capacitance array
In Fig. 6, all the unit capacitors will be set by 434.4f F, the bridging capacitor $C_2$ is 450.9f F.
Because the value of $C_2$ is bigger than theory number, it should use the sub-calibrated array to calibrate the DNL of BIT(11) to BIT(16), when all DNL number of BIT(11) to BIT(16) are smaller than 1 LSB, the SNR of calibrated bridging capacitor $C_2$ is 82.3 dB, the SFDR is 86.9 dB.
The simulation result is as Fig. 11

![Figure 11](image.png)
Figure 11. The dynamic performance of calibrated bridging capacitor $C_2$

The DNL\textsubscript{BIT11} of calibrated bridging capacitor $C_2$ is about 1 LSB.

3.4. The Simulation of mismatch BIT(16) capacitors in main capacitance array
In Fig. 6, all the unit capacitors will be set by 434.4f F, the bridging capacitor $C_2$ is 447.975f F, the capacitors of BIT(16) is set by 31*434.4f F+430.6f F.
The SNR of mismatch BIT(16) capacitors is 78.5 dB, the SFDR is 84.8 dB. The simulation result is as Fig. 12.

![Figure 12](image)

**Figure 12.** The dynamic performance of mismatch BIT(16) capacitors

The DNL of mismatch BIT(16) capacitors is about 7 LSB.

3.5. *The Simulation of calibrated BIT(16) capacitors in main capacitance array*

In Fig. 6, all the unit capacitors will be set by 434.4f F, the bridging capacitor C2 is 447.975f F, the capacitors of BIT(16) is set by $31 \times 434.4f F + 43.6f F$.

Because the value of BIT(16) capacitors is smaller than theory number, it should use the sub-calibrated array to calibrate the DNL of BIT(16), when the DNL number of BIT(16) is smaller than 1 LSB, the SNR of calibrated BIT(16) capacitors is 83.1 dB, the SFDR is 92.3 dB. The simulation result is as Fig. 13.

![Figure 13](image)

**Figure 13.** The dynamic performance of calibrated BIT(16) capacitors

The DNL of calibrated bridging capacitor C2 is about 1 LSB.

3.6. *The Contrast Results of Simulation*

| Parameter of Simulation | Parameter | Structure | C2 | BIT(16) |
|-------------------------|-----------|-----------|----|---------|
|                         | SFDR (dB) | Match     | 90.3 | 84.9    |
|                         | SNR (dB)  | Match     | 77.2 | 66.5    |
|                         | DNL (LSB) | Calibrated | 86.9 | 82.3    |
|                         |           | Mis-match | 78.5 | 84.8    |
|                         |           | Calibrated | 81.3 | 92.3    |

In Table 1, it can get the conclusions. Comparing the Situation I with Situation II and Situation III, it can get: if the bridging capacitor C2 is mis-matching with theory number, the conversion performance will obviously reduce, but in this situation, through the sub-calibrated arrays can almost get the equal conversion performance.

At the same, if comparing the Situation I with Situation IV and Situation V, it also can get the same conclusion with the above one.
4. The Finished Circuit Test
Through a standard 0.6μm CMOS process, it gets the finished 16 bit A/D converter circuits by the above structure.

In order to measure the conversion performance, it should be measured the Integral Nonlinearity and Differential Nonlinearity of the each A/D converter.

According to the basic analog theory, it can get: If the maximum of Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) is Y, the number of N satisfied $2^N = Y$, the effective resolution of A/D converter is $(16 - N)$ bit [5].

Through testing the finished A/D converters, if it does not use any sub-calibrated array, the effective resolution of ADC is about 12 Bit. But if using the sub-calibrated array to calibrated the NDL number of BIT(11) – BIT(16), the effective resolution will be raising to about 14 Bit.

The main parameters are shown as Table 2.

| Num | The Initial Circuit | Num | The Calibrated Circuit |
|-----|---------------------|-----|------------------------|
|     | DNL | INL | DNL | INL | DNL | INL |
| 1.1  | 12 LSB | 9 LSB | 2.1 | 3.5 LSB | 3.1 LSB |
| 1.2  | 13 LSB | 10 LSB | 2.2 | 3.2 LSB | 2.8 LSB |
| 1.3  | 12 LSB | 10 LSB | 2.3 | 3.6 LSB | 3.2 LSB |
| 1.4  | 11 LSB | 11 LSB | 2.4 | 3.5 LSB | 3.0 LSB |
| 1.5  | 14 LSB | 11 LSB | 2.5 | 3.3 LSB | 2.9 LSB |
| 1.6  | 12 LSB | 9 LSB  | 2.6 | 3.6 LSB | 3.2 LSB |
| 1.7  | 13 LSB | 10 LSB | 2.7 | 3.0 LSB | 2.3 LSB |
| 1.8  | 14 LSB | 12 LSB | 2.8 | 3.3 LSB | 2.8 LSB |

In Table 2, it can easily get: The maximum INL and DNL of the initial circuit is about 14 LSB, the maximum INL and DNL of the calibrated one is about 3.6 LSB.

From the theoretical formula, it can get: The effective resolution of the initial circuit is 12.2 bit, the effective resolution of structure II is 14.15 bit.

From the above all, it can get the conclusion:
Through the layout optimization, the nature match precision of the foundry can reach about 12 bit, for getting more higher conversion precision, it is not possible for not using any calibrated ways. But through the sub-calibrated arrays, the calibrated ADC can get more than 14 bit conversion precision.

5. Conclusion
From the simulation and finally circuit test part, they all can get the conclusions:

The effective resolution of 16-bit SAR ADC without any calibrated ways only can reach to 12-bit conversion precision, but it can use the calibrated array to realize more higher resolution.

From the above all, it can get:
This paper’ calibrated capacitance array’ conversion performance is obviously better than the nature matching one when the capacitance array is mismatching, and it’s highest resolution is determined by sub-calibrated array’ precision rather than the matching precision of foundry.

Acknowledgments
This work was financially supported by Chengdu Sino Microelectronics Technology Co., Ltd. Thanks for Ping Yang and Yuan-Jun Cen, they are responsible for this ADC projection’s design, simulation and verification, they are also responsible for this paper’ submission, revision and calibration. So Ping Yang and Yuan-Jun Cen are all the corresponding author of this paper.

References
[1] B. Razavi, Design of Analog COMS and Intergrated Circuits. Xi’an: Xi’an Jiaotong University Press, 2012.
[2] D. Johns,K. Martin, Analog Integratid Circuit Design. Beijing: China Machine Press,2005.
[3] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design Second Edition. Beijing: Publishing House of Electronics Industry,2011.
[4]  R. Jacob Baker, CMOS Circuit Design, Layout, and simulation. Post & Telecom Press, 2008.
[5]  Robert A. Pease, Analog Circuit: World Class Designs. ISBN: 978-0-7506-8627-3.