Architectural Improvements and Technological Enhancements for the APEnet+ Interconnect System.

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ABSTRACT: The APEnet+ board delivers a point-to-point, low-latency, 3D torus network interface card. In this paper we describe the latest generation of APEnet NIC, APEnet v5, integrated in a PCIe Gen3 board based on a state-of-the-art, 28 nm Altera Stratix V FPGA. The NIC features a network architecture designed following the Remote DMA paradigm and tailored to tightly bind the computing power of modern GPUs to the communication fabric. For the APEnet v5 board we show characterizing figures as achieved bandwidth and BER obtained by exploiting new high performance ALTERA transceivers and PCIe Gen3 compliancy.

KEYWORDS: Data Acquisition Systems; Data Communication; Computer Networks.

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1. Introduction

The APEnet+ project delivered a point-to-point PCIe Gen2 interconnect adapter to be employed in hybrid x86+GPU computing clusters with a 3D toroidal network mesh. APEnet+ high performance and low latency capabilities are the result of a network architecture designed following the Remote DMA paradigm which is tailored to tightly bind the computing power of modern GPUs to the communication fabric. Doing so on the APEnet+ board was possible by employing latest standards for the physical interconnect — SFF-8436 with its QSFP+ modules — and exploit them by means of the large hardware resources provided by a state-of-the-art FPGA platform like the Stratix IV.

Following up with enhancements in these areas — the most significant being an upgraded interconnect standard (SFF-8665) with new zQSFP plugs and the latest generation for the PCIe standard — means employing an evolved FPGA platform able to integrate and exploit these improvements alongside added functionality. This requires a redesign of the NIC to support the new PCIe Gen3 protocol, faster transceivers and a much larger amount of programmable resources. The chosen platform for this redesign exploration is the Stratix V FPGA Development Kit. The APEnet v5 is based on a 28 nm technology FPGA (5SGXEA7K2F40C2N) and offers a PCIe ×8 connector, two HSMC connectors for exporting high bandwidth links over a daughterboard, a QSFP connector with optical cage and an Ethernet PHY 10/100/1000Mbps copper connector. A PLDA-proprietary component — QuickPCIe Expert — was chosen as a Gen3-compliant core interface towards the PCIe bus. With this core, either an Avalon or an AXI bus can be selected as user interface; the choice of implementing the latter gives us room for preparing the APEnet v5 environment to deal with the impact brought by a full-featured ARM processor which is slated to be one of the most significant additions on FPGA platforms of the next generation. The new PLDA core also allows for greater freedom when choosing among different strategies for the DMA channels management.

In section 2 we summarize the main feature of the APEnet+: in section 3 the very latest developments on the APEnet v5 board on a 28 nm technology FPGA are reported — harnessing the complexities of a PCIe Gen3 interface being a so far-reaching work in a GNU/Linux device driver as to deserve a specific and in-depth examination in the dedicated section 4. In conclusion in section 5 preliminary results obtained with the APEnet v5 board are shown.

2. APEnet+ and related work

APEnet+ [1] is a point-to-point, low-latency network controller developed by INFN for a 3D-torus topology integrated in a PCIe Gen2 board based on an Altera Stratix IV FPGA. It is the building block for the QUonG [2] hybrid CPU/GPU HPC cluster and the basis for a GPU-enabling data acquisition interface in the low-level trigger of NA62, a High Energy Physics experiment at CERN [3]. The board provides 6 QSFP+ modules which are directly connected to the Altera FPGA embedded transceivers. Each transceiver is capable of a data rate up to 8.5 Gbps in fully bidirectional mode; a single remote data link — the APElink [4] — is built up by bonding 4 transceivers composing a link operating at up to 34 Gbps. The NIC is also able to directly access the memory of Fermi- and Kepler-class NVIDIA GPUs implementing GPUDirect V2 (peer-to-peer) and the more recent GPUDirect RDMA capabilities [5].
In the field of reconfigurable computing, a fast communication path between GPUs and FPGA-based devices is desirable. In [6] a simpler implementation for connecting GPU and FPGA devices directly via the PCIe bus is described, enabling the transfer of data between these heterogeneous computing units without the intermediate use of system memory. In [7] a GPU-to-GPU communication mechanism via FPGA is described with a different approach to address mapping which does not require specific on-board memory management logic. In [8] is presented an open source framework enabling easy integration of GPU and FPGA resources providing direct data transfer between the two platforms with minimal CPU coordination at high data rate and low latency.

A recent development for major FPGA vendors and board integrators is to come out with development kits and products with updated PCIe Gen3 host interfaces and multiple 10G/40G off-board links. In [9] a PCIe Gen3-compliant NIC with the stated goal of supporting 100 Gbps speeds is presented. However, a lot of work concerning the software device driver and hardware logic is required to exploit the enormous throughput assured by these standards. Research in data acquisition experiments, FPGA accelerators for reconfigurable computing and high speed network interconnect for HPC would benefit from this evolution.

3. APEnet v5 architecture on new generation 28 nm FPGA

APEnet v5 is the name of the latest generation APEnet board based on the Altera DK-DEV-5SGXEA7N development kit (figure 1), a complete design environment featuring a 28 nm FPGA. Two major improvements stem from adoption of the Stratix V: PCIe Gen3 interface and new embedded transceivers with a data rate up to 14.1 Gbps for increased off-board link speed.

The Stratix V FPGA offers a PCIe Gen3 connector supporting a data rate of 8.0 Gbps/lane. The improved 128B130B encoding scheme guarantees a host interface bandwidth enhancement. The total raw bandwidth that can be achieved with a ×8 interface is \( \sim 7.9 \text{ GB/s} \), to compare with the integrated theoretical peak bandwidth of 4.0 GB/s allowed by the Stratix IV on board APEnet++.

As regards off-board connectivity, the Altera board sports a 40G QSFP connector and two HSMC ports. The QSFP connector exploits 4 embedded Altera transceivers from the FPGA device while the HSMC connectors — called port A and port B — provide 8 lanes in port A and 4 lanes in port B with limited data rate transceivers (10.0 Gbps).

The Distributed Network Processor (DNP) is the core of the APEnet v5 architecture [4]. The DNP acts as an offloading engine for the computing node, performing inter-node data transfers. The Torus Link block manages the data flow by encapsulating packets into a light, low-level word stuffing protocol able to detect transmission errors via CRC. It allows for a point-to-point, full-duplex connection of each node with three neighbours. The Router component is responsible for data routing and dispatching, dynamically interconnecting the ports of the cross-bar switch; it is able to simultaneously handle 5 flows @5.6 GB/s applying a dimensioned-ordered routing policy with Virtual Cut-Through [10] algorithm. Finally, the Network Interface is the packet injection/processing logic; it manages data flow to and from either Host or GPU memory. On the receive side, it provides hardware support for the Remote Direct Memory Access (RDMA) protocol [11], allowing remote data transfer over the network without involvement of the CPU of the remote node. An integrated \( \mu \text{C} \) provided by the FPGA allows for straightforward implementation of RDMA semantics.
3.1 PCI Express interface

A redesign of the PCIe interface is mandatory to exploit the Gen3 capabilities provided by the latest Altera FPGA generation. The main components of the interface are the QuickPCIe Expert IP, a PLDA-proprietary component, and an overhauled version of the TX/RX block (figure 3).

The PLDA core wraps around Altera PCI Express Hard IP allowing for access to the PCIe configuration space. It interconnects and arbitrates between input and output flows implementing up to 8 independent DMA Engine modules and converting between the PCIe and AMBA AXI interfaces. Current implementation of the APEnet v5 provides an AXI4-Lite Slave Interface used to access PLDA internal registers, an AXI4-Lite Master Interface for APEnet+ registers, four AXI4 Stream Input Interfaces and two AXI4 Stream Output Interfaces. The AXI interface will simplify the connection of the ARM processor, which could replace our work with the proprietary Altera Nios II microcontroller on future revisions of the device. The AXI4 Memory Mapped slave interface is connected to the DMA_IF inside the TX/RX logic. It programs direct DMA transfers implementing four fully independent DMA Engine Modules in order to take commands used to instantiate memory read transactions, to access the Host/GPU memory and to communicate event completions. It sequentially pops DMA requests and programs DMA transfers writing in PLDA Configuration Space Registers. It is made aware of when transactions are complete by an interrupt which is issued on the AXI domain by the QuickPCIe DMA engines. AXI4 Stream interfaces are used to push/pop data, command and completion word in and out to FIFOs.

3.2 Off-board interface

Stratix V GX FPGAs feature full-duplex transceivers with data rates from 600 Mbps to 14.1 Gbps, offering several programmable and adaptive equalization features.

The Physical Layer of Torus Link block is made up of an Altera Custom IP Core (with the corresponding reconfiguration block) and a proprietary channel control logic (Sync_ctrl block),
as shown in figure 3. The Altera Custom IP Core is a generic PHY which can be customized in order to meet design requirements. The receiving side consists of a Word Aligner, 8B/10B decoder, Byte Ordering Block and RX phase compensation FIFO. Similarly, on the transmitter side, each transceiver includes TX phase compensation FIFO, 8B/10B encoder and Serializer. The Word Aligner restores the word boundary based on an alignment pattern that must be received during link synchronization. A status register asserted by the Altera Avalon interface triggers the Word Aligner to look for the word alignment pattern in the received data stream. The Byte Ordering block looks for the byte ordering pattern in the parallel data: if it finds the byte ordering pattern in the MSB position of the data it inserts pad bytes to push the byte ordering pattern to the LSBByte(s) position. Finally, the RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric clock. The write and read enable signal of the Deskew FIFOs are managed by the Sync_ctrl block: the write signals are asserted for each lane after recognition of 8B/10B keyword /K28.3/, while the read signal, common to all FIFOs, is asserted when all FIFOs are no longer empty. Altera Transceiver Reconfiguration Controller dynamically reconfigures analog settings in Stratix V devices: it is able to compensate for variations due to process, voltage and temperature in 28 nm devices;

| Cable                     | BER     | Data Rate |
|---------------------------|---------|-----------|
| 10 m Mellanox optical cable | < 2.36 E-14 | 11.3 Gbps |
| 1 m Mellanox copper cable  | < 1.10 E-13 | 10.0 Gbps |

Table 1. APEnet+ BER measurements on Altera 28 nm FPGA.

In conclusion, we implemented three bi-directional data channels. The X channel was implemented using the 4 lanes of the 40G-QSFP connector; the Y and Z channels were implemented onto the HSMC interface. Very preliminary BER measurements were performed on the X channel of APEnet v5 (see table 1). The testbed consists of two Stratix V FPGAs connected by InfiniBand cables with different lengths and support media (optical and copper). Copper wires results derive from experiments conducted with 10 Gbps-certified cables; they are expected to improve as soon as they are repeated with commercially available 14 Gbps-certified ones. Moreover, the results are satisfactory, taking into account that no analog parameters fine tuning was applied.
4. PCIe Gen3 Driver Design

All APEnet v5 software is developed and tested on the GNU/Linux x86_64 platform and is available under the GNU GPL Licence. A low-level, custom RDMA API is available, in principle similar to, though much simpler than, Infiniband verbs and the former Myrinet GM. The RDMA APIs are available as a C language library, containing a small set of functions and data types:

- Communication primitives available to applications are: rdma_put/send(). They are asynchronous — simply pushing a command into a queue and returning when data have been read by the NIC — and optionally non-blocking, i.e. they return on the event of a full command queue, requiring to be reissued.
- Memory buffer registration is mandatory for receive buffers and allows memory areas to be reserved for remote node access and to add their addresses (virtual and physical) to the NIC internal buffer table: register_buffer(), unregister_buffer().
- Events are generated on completion of communication primitives, when pre-registered receive buffers are written or when error conditions arise. The wait_event() API call is used to wait for the arrival of an event with an optional time-out.

For both communication and buffer registration APIs, memory buffers are referenced by their virtual address — e.g. rdma_put() call takes as argument the virtual address of the remote memory buffer. As it is usual for the RDMA paradigm, there is no receive primitive as receive buffers are always posted before their effective use — i.e. posting is implicitly done by buffer registration. Buffer registration, which is mandatory and explicit for receive buffers, involves memory-pinning and virtual-to-physical address translation and persists until an explicit buffer deregistration. Pinning and translation are implicitly done for the communication primitives rdma_put/send() as well as for the register_buffer() and unregister_buffer().

4.1 Memory Read (TX) Process

On the TX side the memory read process requires the NIC to be instructed by the driver by passing a DMA descriptor. The descriptor contains all the relevant information to program APEnet v5 data transfer — i.e. where the source data buffer is located and its length, where it must be sent and the instructions to generate the "sent event" completion. The device driver inserts the descriptors in a circular list called tx ring. The DMA-capable memory region containing the tx ring is allocated by the device driver during the initializing phase and the memory start address is sent to the board by updating the APEnet v5 registers.

A mechanism based on updating a tx_ring_read and a tx_ring_write pointer, ensures avoiding the memory overwriting by the device driver and inconsistent data reading by the hardware.

For efficiency reasons, the driver is able to store multiple descriptors before updating tx_ring_write pointer accordingly. In this way, the board will program a single DMA for all the descriptors.

Since virtual memory maps a non-contiguous memory region in a contiguous virtual address space, the buffer could be fragmented all over physical memory. Every transfer larger than a single page — typically 4 KB — is managed by a scatter-gather (SG) list, where every element of the list is a page of the buffer. In this case, each page will be mapped in one tx ring descriptor, i.e. every descriptor has the associated physical address of one page of the buffer.
Data of completion events are maintained in a cyclic queue called **event queue** that is the same for both the "sent" event and the "received" event. Therefore, after updating the tx_ring_write pointer thus having issued a data transfer, the driver starts polling the **event queue** to wait for completion events. Whenever new completion events are found, they are copied into a software queue, ready to be popped by the application process that invokes the "wait_event" library function.

### 4.2 Memory Write (RX) Process

The NIC on the receiving side DMA-writes data packets coming from torus links into host memory. There is no need of intermediate copies from kernel space to user space or driver queries for buffer memory address. This reduces the bus occupancy and the number of switches between kernel space and user space while handling network traffic.

The buffer virtual address is used by the NIC as key to retrieve from the internal table all needed buffer information (primarily the ID of the owner process and the buffer physical address). The first task of the receiving logic is thus scanning the buffers pool registered by a running application to determine whether the destination virtual address actually belongs to any of them – this process is called Buffer Search (BSRC).

If a buffer is found, the pages that compose it are retrieved, their physical addresses are resolved – virtual-to-physical (V2P) translation – and a number of DMA transactions are finally issued targeting these addresses. In APEnet v5 the address translation mechanism is implemented in two ways: in software, as a firmware on the assisting microcontroller, and in hardware, by means of a Translation Lookaside Buffer (TLB) accelerating the BSRC and V2P tasks.

Therefore, the association between virtual and physical address must be registered beforehand to enable the address translation process. In order to accomplish this task, the hardware exposes a set of registers where the driver writes "commands" to register pages and buffers.

Data arrival is signaled by generating a “received” event, which is managed in the same way of “sent” events as described before.

### 5. Preliminary Results

The testbed consisted of a X9DRG-VF SuperMicro server, hosting a Stratix V FPGA development board, and a Tektronix TLA-7012 Gen3 Logic Analyzer.

Two simple programs test the performance of the new architecture: latency (Fig. 5) is measured by sending a packet of fixed size in local-loop and measuring the time required for the “sent” event and the “received” event to arrive; the test is repeated ∼100000 times and the resulting times are averaged. In order to measure the bandwidth (Fig. 6) the test is slightly different from the previous one: we send all the packets in a once and then wait for all the sent and receive events.

Given that the development is still ongoing, latency results being comparable with those achieved with the previous version of APEnet+ is already promising. As regards the achieved bandwidth of 2.3 GB/s, we must observe that the straightforward porting of APEnet+ architecture onto Gen3 does not regress from Gen2 but does not immediately yield significant improvements either. Indeed, a test performed using a reference design exploiting a single DMA engine of the QuickPCIe Expert achieve 5.2 GB/s that represents a target bandwidth for the APEnet v5 board.
In table 2 are reported the resource consumptions for the APEnet v5 firmware synthesized in an Altera Stratix V FPGA. Current design occupies a small fraction of the FPGA, leaving space for more hardware optimizations. For example increasing the size of the TLB can result in better figures for the RX process latency.

Table 2. APEnet v5 resource consumption on an Altera 28 nm FPGA.

| Project  | Board             | ALMs     | Register | Memory [MB] |
|----------|-------------------|----------|----------|-------------|
| APEnet v5 | 5SGXEA7K2F40C2N   | 76747 (33%) | 91447   | 1.55 (24%) |

6. Conclusions

We have presented the work done to advance the tested IP of an FPGA-based, 3D toroidal network card like APEnet+ to a 28 nm, Gen3-compliant FPGA with its initial performance figures.

Due to the immature status of the driver/board communication mechanism and the hardware implementation, the bandwidth is limited at 2.3 GB/s, not showing the gain that should have hopefully resulted from adoption of a PCIe Gen3 platform.

We are however confident to be able to improve on these results once we employ more of the advancements that the new platform has put in place. For example, we mention that in this first version we are not using in parallel the DMA engines that the PLDA QuickPCIe Expert provides; in APEnet+, a similar optimization was introduced in a second stage of development and led to a performance gain of about 40% in bandwidth \( [12] \). Moreover, it is likely that current software implementation of the driver will need significant optimization so as not to become the new bottleneck in reaching peak performance: we are considering moving a number of driver tasks from kernel to user space; for example, offloading memory mapping \texttt{tx\_ring} and \texttt{event\_queue} would reduce the switches between user and kernel spaces and help us reach the Gen3 bandwidths.

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