Use of Magnetoresistive Random-Access Memory as Approximate Memory for Training Neural Networks

Nicolas Locatelli, Adrien F. Vincent and Damien Querlioz
Centre for Nanoscience and Nanotechnology, CNRS, Univ. Paris-Sud, 91405 Orsay, France.
Email: damien.querlioz@u-psud.fr

Abstract—Hardware neural networks that implement synaptic weights with embedded non-volatile memory, such as spin torque memory (ST-MRAM), are a major lead for low energy artificial intelligence. In this work, we propose an approximate storage approach for their memory. We show that this strategy grants effective control of the bit error rate by modulating the programming pulse amplitude or duration. Accounting for the devices variability issue, we evaluate energy savings, and show how they translate when training a hardware neural network. On an image recognition example, 74% of programming energy can be saved by losing only 1% on the recognition performance.

Index Terms—Approximate computing; Spintronics; ST-MRAMs; Approximate storage; Low energy computing.

I. INTRODUCTION

The development of systems implementing machine learning applications, typically relying on artificial neural networks, has become a major goal of microelectronics research [1], [2]. Interestingly, such systems, which require high amounts of memory, demonstrate relative resilience to inaccuracies during computation [3]. Data integrity in memories is ensured with significant costs in energy and performance of VLSI systems [4], [5], and these costs are exacerbated as memory devices move to smaller dimensions, along with increasing process variations [6], [7]. Therefore, the approximate computing paradigm [4], [8]–[11], which proposes to trade off computational accuracy for higher energy efficiency [12], could be a lead for reducing the energy costs related to memory in hardware artificial neural networks.

This idea takes particular meaning as many hardware artificial neural networks propose using emerging types of memories for implementing synaptic weights [2]. In particular, with considerable progress made in recent years, spin torque magnetic random access memories (ST-MRAMs) are highly attractive, as they provide fast programming and outstanding endurance in a compact and non-volatile memory cell, fully embeddable at the core of CMOS [13].

In this work, we explore the unique properties of ST-MRAMs in the framework of approximate computing, and propose how they could be exploited in hardware neural networks. Relying on recently developed analytical models of the ST-MRAMs programming statistics, this work first explores the relation between programming precision and energy expenditure. We show using circuit simulations that the consequences of device variability increase dramatically as the precision requirements become stronger. We then investigate how allowing higher error rates can provide significant energy savings, and show based on an example that this approach suits judiciously to data storage in the context of artificial neural network applications.

II. STOCHASTIC PROGRAMMING OF THE MAGNETIC BIT

The magnetic tunnel junction (MTJ), the core device of MRAM circuits, is composed of a stack of magnetic and non-magnetic materials, implementing a fixed reference magnet and a bi-stable storage magnet sandwiching a tunnel barrier (Fig. 1,a). The resistance of the stack differs for the two relative orientations of the magnets (parallel or anti-parallel), through the tunnel magnetoresistance (TMR) effect. The stability of the memory bits is characterized by the energy barrier $\Delta E$ separating the two states. Here, $\Delta E = 70 k_B T$ is chosen to ensure one Failure In Time rate for a 64 MB array. For this study, we choose values for MTJ parameters reminiscent of a 32 nm node technology based on perpendicular magnetization anisotropy materials [14], [15]: diameter of 32 nm, storage layer thickness of 3.5 nm, saturation magnetization $M_s = 700 kA/m$, resistance-area product of $4 \Omega \cdot \mu m^2$, TMR of 150%, and critical switching voltage of 190 mV.

The state of an MTJ can be switched by passing a current through the stack with appropriate sign and amplitude. The bit programming can be performed by a bidirectional driver circuit (Fig. 1b) applying a pulse to the device, of given voltage amplitude $V_{pulse}$ and duration $T_{pulse}$. One strong particularity of MTJ devices is the stochastic behavior of their programming [7], [16]–[20]. The junction has a non-100% probability $P(V_{pulse}, T_{pulse})$ to switch (Fig. 1c) when a pulse is applied. Switching probability distributions can be described by the gamma distribution, whose mean and skewness are derived as a function of the programming voltage [17]. The full dependence of the two parameters is presented in Fig. 1d. For the purpose of this study, complementary MATLAB and SPICE models of the MTJ are developed, that include the full description of the intrinsic stochastic behavior of the device as well as extrinsic variability between devices.
III. INTERPLAY BETWEEN PROGRAMMING PRECISION AND ENERGY COST

In this study, we use the bidirectional driver circuit (Fig. 1b) to apply pulses with amplitude $V_{\text{pulse}} = 381 \text{ mV} = 2.0 V_c$. Considering no variability in any device of the circuit, we derive from our analytical model that a pulse duration value $T_{\text{pulse}} = 15.0 \text{ ns}$ is requested to ensure programming with a low bit error rate $\text{BER} = 10^{-10}$. The associated single bit programming energy is evaluated to $0.48 \text{ pJ}$. Starting from this high-precision reference point, energy savings can be obtained by increasing the programming error rate, either by reducing the programming pulse amplitude or its duration. The strongest energy savings are obtained by a reduction of the pulse duration while keeping the pulse amplitude constant and as high as possible. Moreover, a pulse duration control strategy can easily be achieved without any modification of the driver circuit or its supply voltage, as it simply requires gating the programming pulse on demand when the application tolerates lower precision storage. Fig. 2 shows the dependence of the programming energy with the target error rate, derived from the model of [17]. Black solid lines are obtained in the case of a perfect MRAM circuit with no device-to-device variability. Relaxing the BER from $10^{-10}$ to $10^{-4}$ allows for a 37% energy reduction. Best energy savings are expected when considering programming with even lower pulse durations, and higher BER $\geq 0.01 \%$. We then observe a rapid decrease of the programming energy with BER, as emphasized by Fig. 2b. Compared to programming with BER = $10^{-10}$, programming with BER = $10^{-3}$ allows a 45% energy saving, and BER = 1% allows a 53% energy saving.

Device variability of both CMOS and ST-MRAMs is a crucial issue that can directly increase the global error rate. To account for these effects, we now simulate the driver circuit using Cadence tools, with the design kit of a 28 nm commercial CMOS technology and our SPICE model of the MTJ devices. Process and mismatch variability on CMOS transistors is considered for Monte Carlo simulations, as well as a 5% variability on resistance and TMR parameters, typical values of ST-MTJ cells variability [7]. The consequence of such

![Image](image_url)
variability on the programming energy is then evaluated. The red dashed curve in Fig. 2 shows the new full dependence of the average programming energy with the target bit error rate. The relative energy increase is also plotted as insets. We see that the consequent raise of the programming energy implied by variability is exacerbated when the target bit error rate is decreased. Ensuring that the BER = 10^{-10} remains unaffected requests to raise the pulse duration up to \( T_{\text{pulse}} = 20.5 \text{ ns} \), implying a programming energy increase by 36.8%, while only a 17.6% increase is necessary for BER = 10^{-4}. This is due to switching probability becoming increasingly sensitive to variations of the programming parameters when target BER is high. These results again show the strong cost of high programming precision, and the interest of finding strategies to consider computing with reduced precision whenever possible.

IV. APPROXIMATE PROGRAMMING IN A NEURAL NETWORK

We now consider the use of ST-MRAM in the framework of approximate computing, taking the example of the training of a neural network for an image recognition task. We consider a simple two-layer formal neural network with tanh activation function, with 784 input neurons, 300 hidden neurons, and 10 output neurons Fig. 3. The network is trained on handwritten digit recognition task using the MNIST dataset, by updating a number of synaptic weights along a learning procedure. We study the case of weights coded as 16-bit fixed point numbers stored using a ST-MRAM circuit. For each learning step, a mini-batch of 10 images is presented to the ANN, and weight updated following the backpropagation algorithm. Learning is performed through five presentations of the full set of 60,000 training images. Five sets of initial weights are used to test the reproducibility and generality of the performance results of the neural network. For every set of parameters of the approximate memory, we show the obtained average recognition rate, as well as error bars presenting the range of recognition rates obtained over the five tests.

In a first phase, we consider programming all the bits of the 16-bit synaptic weights with identical BER. Interestingly, in Fig. 3 we observe that the final recognition rate of 97.2% remains unaffected as the BER is increased up to a large BER = 0.1%, and is only slightly reduced to 96.7% for BER = 1%. Beyond this point, the final recognition rate falls down, and the recognition capabilities become strongly dependent on the initial conditions of the network. Programming the weights with BER = 0.1% or BER = 1% represents an energy saving of respectively 54.4% and 62.7% on the ST-MRAM programming during the learning operation, compared to quasi-deterministic programming (BER = 10^{-10}).

While the energy saving is already substantial, the strategy can be further extended, by choosing different levels of programming precision for each bit, where the memory would prioritize the precision of higher significance bits and progressively increase the BER of lower significance bits. In this second phase, we consider a simple two-stage programming strategy by differentiating high significance bits (HSBs), programmed with a BER of 1%, and low significance bits (LSBs), programmed with higher BER.

![Fig. 4. Final recognition rate of the 2-layer neural network with 16-bit synaptic weights, as a function of the programming BER of the LSBs, for different numbers of LSB. The HSBs are programmed with a 1% error rate.](image)

The results, presented in Fig. 4, show that a substantial increase of the BER for LSBs is possible without critical consequences on the final recognition rate of the ANN. As a reference, results are also given in the case of BER_{LSBs} = 100%, corresponding to fully random, never updated low significance bits, showing that even a 90% BER for the LSBs can substantially increase the performance of the ANN, and discarding the eventuality that LSBs could simply be removed, as can be done in inference-only hardware [21]. It is noteworthy that the ANN is resilient to BER_{LSBs} as high as 90% for up to 8 LSBs, 70% for 10 LSBs, and 10% for 12 LSBs. In the case of 14 LSBs, increasing the BER further that 1% is immediately detrimental to the performances. Again, substantial energy savings can be expected from this strategy. To visualize the trade-off between programming energy and performances, and find the best compromise between an increase of the number of LSBs and an increase in their BER, we also transfered the results

![Fig. 3. Final recognition rate of a 2-layer neural network with 16-bit synaptic weights, as a function of their programming BER, evaluated on the MNIST dataset. Error-bars: dispersion of the results for five different initial conditions.](image)
onto a graph of the ANN final recognition rate versus the total programming energy per synaptic weight, presented on Fig. 5. This graph shows that the implementation of the two-stage strategy, is able to bring an extra reduction of the energy expense without affecting very significantly the performances of the ANN. As emphasized by the high performance window (Fig. 5b), best performance-energy ratios are obtained for 8 to 10 LSBs. For instance, programming the synaptic weights with \( \text{BER}_{\text{10LSBs}} = 1\% \) and \( \text{BER}_{\text{8LSBs}} = 50\% \), while granting a 74.6\% energy saving compared to quasi-deterministic programming, only reduce the recognition rate of the ANN to 96.2\%, i.e. less than 1\% reduction. Final choice should of course be made depending on the tolerance on the final recognition rate.

V. CONCLUSION

In this work, we have studied the energy cost of strong programming precision ST-MRAMs, and evaluated the potential energy saving of the programming operation in the framework of disciplined approximate computing. We highlighted that a control of the programming pulse duration appears as the most efficient handle to tune the programming bit error rate while ensuring the strongest energy reduction. Consequently, we proposed a two-fold BER programming strategy that does not require any modification of driver circuits, allowing the application to control which bits should be programmed inaccurately. Finally, we showed that using this strategy could result in considerable energy savings when training a hardware neural network. Taking the simple example of character recognition, 74\% of the ST-MRAM programming energy can be saved while losing only 1\% of performance in terms of image recognition. These results confirm that approximate computing techniques can be highly attractive for machine learning applications, and that memory can be a good place where approximate computing is especially useful.

ACKNOWLEDGMENTS

This work was supported by the National Research Agency (ANR-10-LABX-0035, ANR-13-JS03-0004-01) and the European Research Council (NANOINFER, ref.: 715872).

REFERENCES

[1] J. Dean, D. Patterson, and C. Young, “A new golden age in computer architecture: Empowering the machine-learning revolution,” IEEE Micro, vol. 38, no. 2, pp. 21–29, 2018.
[2] S. Yu, “Neuro-inspired computing with emerging nonvolatile memories,” Proc. IEEE, vol. 106, no. 2, pp. 260–285, 2018.
[3] G. W. Burr et al., “Experimental demonstration and tolerancing of a large-scale neural network (165 000 synapses),” IEEE Trans. Electron. Dev., vol. 62, no. 11, pp. 3498–3507, 2015.
[4] A. Sampson, L. Ceze, and D. Grossman, “Good-enough computing,” IEEE Spectrum, vol. 50, no. 10, pp. 54–59, Oct. 2013.
[5] K. Palem and A. Lingmannen, “Ten Years of Building Broken Chips: The Physics and Engineering of Inexact Computing,” ACM Trans. Embed. Comput. Syst., vol. 12, no. 2s, pp. 87:1–87:23, 2013.
[6] M. Indaco, P. Prinetto, and E. Vatajelu, “On the impact of process variability and aging on the reliability of emerging memories,” in Proc. ETS, 2014, pp. 1–10.
[7] D. Worledge et al., “Switching distributions and write reliability of perpendicular spin torque MRAM,” in IEDM Tech. Dig., 2010, pp. 12.5.1–12.5.4, 00018.
[8] J. Han and M. Orshansky, “Approximate computing: An emerging paradigm for energy-efficient design,” in Proc. ETS, 2013, pp. 1–6.
[9] J. Kim and S. Tiwari, “Inexact computing for ultra low-power nanometer digital circuit design,” in Proc. NANOARCH, Jun. 2011, pp. 24–31.
[10] C. M. Kirsch and H. Payer, “Incorrect Systems: It’s Not the Problem, It’s the Solution,” in Proc. DAC, 2012, pp. 913–917.
[11] S. Venkataramani, S. Chakradhar, K. Roy, and A. Raghunathan, “Approximate computing and the quest for computing efficiency,” in Proc. DAC, Jun. 2015, pp. 1–6.
[12] V. Chippa et al., “Scalable Effort Hardware Design,” IEEE T. VLSI Syst., vol. 22, no. 9, pp. 2004–2016, Sep. 2014.
[13] N. Locatelli et al., “Spintronic devices as key elements for energy-efficient neuroinspired architectures,” in Proc. DATE, 2015, p. 994.
[14] A. F. Vincent et al., “Basic principles of STT-MRAM cell operation in memory arrays,” J. Phys. D, vol. 46, no. 7, p. 074001, Feb. 2013.
[15] K. C. Chun et al., “A Scaling Roadmap and Performance Evaluation of In-Plane and Perpendicular MTJ Based STT-MRAMs for High-Density Cache Memory,” IEEE JSSC, vol. 48, no. 2, pp. 598–610, 2013.
[16] Z. Wang, Y. Zhou, J. Zhang, and Y. Huai, “Bit error rate investigation of spin-transfer-switched magnetic tunnel junctions,” Appl. Phys. Lett., vol. 101, no. 14, p. 142406, Oct. 2012.
[17] A. F. Vincent, N. Locatelli, J.-O. Klein, W. Zhao, S. Galdin-Retailleau, and D. Querlioz, “Analytical Macrosim Model of the Stochastic Switching Time of Spin-Transfer Torque Devices,” IEEE Trans. Electron Dev., vol. 62, no. 1, pp. 164–170, Jan. 2015.
[18] A. F. Vincent et al., “Spin-transfer torque magnetic memory as a stochastic memristive synapse for neuromorphic systems,” IEEE T. Biomed. Circ. S., vol. 9, no. 2, pp. 166–174, 2015.
[19] A. Ranjan, S. Venkataramani, X. Fong, K. Roy, and A. Raghunathan, “Approximate storage for energy efficient spintronic memories,” in Proc. DAC, Jun. 2015, pp. 1–6, 00002.
[20] F. Sampaio et al., “Approximation-aware Multi-Level Cells STT-RAM cache architecture,” in Proc. CASES, 2015, pp. 79–88.
[21] I. Hubara, M. Courbariaux, D. Soudry, R. El-Yaniv, and Y. Bengio, “Quantized neural networks: Training neural networks with low precision weights and activations,” arXiv preprint arXiv:1609.07061, 2016.