Study of Energy-Efficient Scheduling in Multi-Core Systems in Dynamic Voltage and Frequency Adjustment

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Abstract. In the field of electronic information technology, with the development of the application of multi-core processors, various types such as homogeneous cores and heterogeneous multi-cores have appeared, and the consequent energy consumption problem has been paid more and more attention. For the application of multi-core systems, there are many researches on real-time energy-saving dispatching technology based on dynamic voltage and frequency adjustment (DVFS). This article first introduces the development of energy-saving scheduling technology for multi-core systems, focusing on parallel task model technology, then introduces the advantages of the retiming directed acyclic graph model, and finally proposes a multi-core energy-saving scheduling algorithm based on DVFS, which is a multi-core processing The application research of the processor system in the real-time embedded field provides a reference.

Keywords: Heterogeneous Multicore; Energy-Efficient Scheduling; DVFS; Task scheduling.

1. Introduction
In an embedded computer system, the power consumption of the processor is an important part of the total power consumption. For CMOS processors, energy consumption mainly comes from two parts: dynamic power consumption caused by capacitance switching and static power consumption caused by leakage current. The energy consumption of the processor accounts for about 50% of the energy consumption of the system. The key to the energy-saving design of a real-time multi-core system is how to reduce the energy consumption of the processor so that the energy consumption of the entire system can be optimized. Currently, energy-saving technologies mainly applied in the embedded field include: Dynamic Voltage Frequency Scaling (DVFS) technology and Dynamic Power Management (Dynamic Power Management, DPM) technology. DVFS technology can dynamically adjust the supply voltage and frequency during operation. Because dynamic energy consumption and power supply voltage have a square relationship, this has a significant effect on reducing processor dynamic energy consumption. Processor frequency and system dynamic power consumption have a convex function increasing relationship, Reducing the frequency can significantly reduce the dynamic power consumption, but at the same time the reduction of the execution frequency will cost time and will also affect the static power consumption, which requires a reasonable compromise. DPM is also an
important means to control system power consumption. It can dynamically optimize the opening and closing of idle processor cores (or enter a low-power state) according to changes in load, so that the entire dynamic power consumption and static power consumption of the system are both can be reduced.

Energy-saving scheduling technology is to comprehensively adopt the above control technologies, and make reasonable optimizations and compromises in dynamic power consumption, static power consumption, performance and real-time performance to achieve the optimal system.

2. Related work

Multi-core systems include homogeneous multi-core systems and heterogeneous multi-core systems. All processor cores in a homogeneous multi-core system have the same structure, and any task can be executed on each core in the system at the same execution speed. The processor cores in heterogeneous multi-core systems are different, not all tasks can be executed on any processor core, and the execution efficiency and speed of tasks on a certain processor core depends on the characteristics of the processor core. The above difference determines that the energy-saving scheduling method of a heterogeneous multi-core system is different from a homogeneous multi-core system.

According to different task allocation strategies in multi-core systems, real-time scheduling algorithms include the following three categories: no migration, task-level migration, and task-instance-level migration. Generally, the partition method refers to the scheduling algorithm without migration, and the global method refers to the scheduling algorithm that allows migration. A task is only allocated to one processor for execution, and task migration is not allowed. This algorithm is a scheduling algorithm without migration; task instances can be executed on different processor cores. This scheduling algorithm is a task-level migration scheduling algorithm; allowed each task instance migrates and executes on different processor cores, but parallel execution within tasks is not allowed. This algorithm is a task instance-level migration scheduling algorithm.

2.1. Directed Acyclic Graph

The high performance of multi-core processor comes from task parallelism, and the parallelism of two tasks depends on its scheduling strategy. How to map multiple threads to multiple processor cores to meet the real-time performance of tasks and ensure the overall performance is the focus of real-time scheduling of parallel task model. The existing research on real-time scheduling technology of multi-core systems generally assumes the serial task model of a single thread or a simple parallel model. The previous research results are often based on heuristic and simulation testing [1], or introduce the classical real-time scheduling algorithm into parallel scheduling, without considering more complex parallel processing, and do not consider the mature schedulable testing methods. With the in-depth research of multi-core scheduling technology, new scheduling models are proposed. For example, a stream data oriented task model is a stream based task model; Multi frame task model is used to model tasks with varying execution time; Based on DAG graph task model and conditional branch expression, it becomes a cyclic real-time task model; In the sporadic DAG model [2], each directed acyclic graph represents a cyclic task, which is used to represent the cyclic and sequential constraints of tasks executed on isomorphic multiprocessor platforms; SADF model [3] is composed of multiple patterns and a finite state machine FSM. It is applied to flow applications on multiprocessor platforms. It is a scene sensitive data flow graph model. Directed acyclic graph DAG parallel task model is a widely used multi-core task scheduling model. It can directly express the priority constraints and communication overhead between tasks. It is widely used in multi-core system task scheduling technology.

The research on multi-core energy-saving real-time scheduling based on DAG task model focuses more on the flow control of embedded real-time system. In this kind of application, a large number of single cyclic tasks are allowed to execute exclusively on the specified processor core. This task execution environment puts forward higher requirements for the parallel task model, so the occasional
DAG parallel task model is used to represent the cyclic and sequential tasks executed on the multi-core processor platform. In the accidental DAG parallel task model, a cyclic accidental task is represented as a directed acyclic graph DAG. Each vertex of DAG represents a task, and the edges of DAG represent the sequential relationship between these tasks. Dag needs to complete the execution of all subtasks within the specified relative time limit, and then release them at the same time. The energy-saving real-time scheduling problem of multi-core systems has been proved to be a NP hard problem, which can only be solved by effective approximation.

2.2. Scheduling method based on DVFS

At present, most multi-core energy-saving real-time scheduling takes the directed acyclic graph (DAG) model as the multi-task model. Andrei et al. Proposed a performance mode reordering technology, which is designed for the voltage scheduling generated by the task graph that contains both intra iteration data dependence and inter iteration data dependence. When this method is applied to the directed acyclic graph model, an improved multi task model will be obtained: retiming directed acyclic graph model. In the retimed directed acyclic graph, there is no intra iteration data dependency between all tasks, which provides the possibility for the adjustment of task sequence, which is the key to reduce the voltage conversion time between tasks. In order to produce more relaxation time and save energy, the total voltage conversion time must be compressed. This optimization reduces the voltage conversion time, which is of great significance to the multi-core energy-saving scheduling technology based on dvfs.

Retiming directed acyclic graph can make full use of multi-core structure and give full play to the advantages of pipeline technology. Compared with directed acyclic graph, retiming directed acyclic graph can improve task parallelism, compress scheduling length and reduce energy consumption more effectively[4].

In the demonstration example, any two tasks with dependencies (in the original DAG) are assigned to two different processing cores, the number of cycles required for communication is 1, and the number of cycles required for communication assigned to the same kernel is 0. The problem can be explained by using the number of cycles to represent the execution time of the task. Figure 1-A shows a directed acyclic graph. The number marked next to the node in the directed acyclic graph represents the number of cycles of the corresponding task. The task graph in Figure 1-B is the retiming directed acyclic graph corresponding to a. Table 1 shows the scheduling generated by applying the 4/3 approximation algorithm to the computing tasks in the retimed directed acyclic graph in B. Table 2 shows the scheduling results after the computing tasks in the retimed directed acyclic graph in Figure B are further adjusted. By comparing Table 1 and table 2, it is found that task C has descendant task D, and there is an inter iteration data dependency between them. The last calculation task of processing core 1 is task C. the premise for task d to perform its ith calculation is to obtain the results of the ith-1st calculation of task C. This bus communication process is the communication task C-D *. Readjusting the position of C in the process can reduce the task scheduling length[5].
Performing tasks in descending voltage order can compress the conversion time. Figure 2 is an example. a is a typical discrete voltage schedule with three tasks. The three tasks in a are executed in order of decreasing voltage to get the result of figure b. Comparing the two, it can be found that the tasks are executed in descending voltage order, so that the tasks with the same voltage are executed sequentially, and the voltage conversion during the period is cancelled, thereby reducing the number of voltage conversions. If the voltage conversion time is a fixed constant, in order to reduce the voltage conversion time and thereby produce more relaxation time, you can use the method of decreasing the voltage to perform tasks in order.

**Figure 1.** Example of retimed directed acyclic graph

![Diagram](image-url)
3. Conclusion
The focus of solving the energy-saving real-time scheduling problem for multi-core systems is how to achieve a reasonable compromise of multiple dimensional constraints. The directed acyclic graph model (DAG) is improved, and the parallel task model of the retiming directed acyclic graph is introduced. This model can effectively reduce the voltage conversion time and improve the task parallelism in the DVFS technology. This paper combines multi-core systems, voltage frequency regulation (DVFS) and retiming directed acyclic graphs to carry out the research on energy-saving real-time scheduling of multi-core systems, which has general reference significance for the exploration of multi-core energy-saving scheduling technology.

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