Deep learning with coherent VCSEL neural networks

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Deep neural networks (DNNs) are reshaping the field of information processing. With the exponential growth of these DNNs challenging existing computing hardware, optical neural networks (ONNs) have recently emerged to process DNN tasks with high clock rates, parallelism and low-loss data transmission. However, existing challenges for ONNs are high energy consumption due to their low electro-optic conversion efficiency, low compute density due to large device footprints and channel crosstalk, and long latency due to the lack of inline nonlinearity. Here we experimentally demonstrate a spatial-temporal-multiplexed ONN system that simultaneously overcomes all these challenges. We exploit neuron encoding with volume-manufactured micrometre-scale vertical-cavity surface-emitting laser (VCSEL) arrays that exhibit efficient electro-optic conversion (<5 attojoules per symbol with a π-phase-shift voltage of $V_{\pi} = 4$ mV) and compact footprint (<0.01 mm$^2$ per device). Homodyne photoelectric multiplication allows matrix operations at the quantum-noise limit and detection-based optical nonlinearity with instantaneous response. With three-dimensional neural connectivity, our system can reach an energy efficiency of 7 femtojoules per operation (OP) with a compute density of 6 teraOP mm$^{-2}$ s$^{-1}$, representing 100-fold and 20-fold improvements, respectively, over state-of-the-art digital processors. Near-term development could improve these metrics by two more orders of magnitude. Our optoelectronic processor opens new avenues to accelerate machine learning tasks from data centres to decentralized devices.

Artificial neural networks are computational systems that imitate the way in which biological brains process information. These systems are built to learn, combine and summarize information from large datasets. As a result of the advances in deep neural network (DNN) algorithms and also increases in computing power, DNNs have thrived in recent years and revolutionized information processing in applications including image, object and speech recognition, game playing, medicine and physical chemistry. A deep fully connected neural network is made of $N$ layers (Fig. 1a), where each layer consists of a matrix-vector multiplication and a nonlinear activation. Driven by the need to tackle problems of increasing complexity, the size of machine learning models is increasing exponentially, with some reaching more than 100 billion trainable parameters.

Received: 24 August 2022
Accepted: 16 May 2023
Published online: 17 July 2023
Fig. 1 VCSEL-ONN architecture. a, Representation of a fully connected DNN composed of N layers with an optical tensor processor in each layer. The 'axon' laser oscillator encoding the input vector X is fanned out, allowing for parallel computing with synaptic weight vectors. The weights are generated from a server of laser oscillators and can potentially be broadcast to process multiple inputs in parallel. Multiply-and-accumulate operations are based on homodyne detection and time integration. The integrated values are stored in nearby digital memories (labelled 'M') and subsequently serialized as the input vector to the next layer. b, Homodyne balance detection. Optical interference between two laser fields generates homodyne product f(Xn, Wn). ∑, integrator; M, digital memory.

parameters as of 2020 (ref. 9). In contrast, due to the practical limits on transistor counts and energy consumption in data movement, extending computational capacity with complementary–metal–oxide–semiconductor (CMOS) circuits has become more and more difficult. An alternative approach leveraging qualitatively different technology must be developed to continue the scaling of computing power in the coming decades.

Several critical bottlenecks emerge when designing efficient and scalable neural network accelerators. Table 1 summarizes the key figures of merit, based on several recent studies. State-of-the-art electronic microprocessors, such as graphics processing units (GPUs) and application-specific integrated circuits (ASICs), are optimized for machine learning tasks by means of the energy efficiency (the energy consumption per operation) (C1), e = 1 pJ/OP (refs. 16,17) and the compute density (the number of operations per second for a given chip area), (C2) ρ = 0.35 femtoOP mm−2 s−1 (NVIDIA A100 GPU), limited by the wire capacitance of electronic interconnects.

Optical neural networks (ONNs) hold great promise to alleviate this bottleneck, with orders-of-magnitude improvement in criteria C1 and C2 due to their large optical bandwidth and low-loss data transmission. Recent progress in ONNs has demonstrated fully connected layers with photonic integrated circuits and holographic phase masks, linear matrix operations at high throughput and low-energy optical readout. However, due to the large footprint and high electro-optic (EO) energy cost of the photonic devices (for example, state-of-the-art low-loss EO modulators require VpL > 1 V cm (ref. 30), where L is the device length), simultaneously achieving C1 and C2 remains an unfulfilled challenge. Moreover, incorporating low-energy, all-optical nonlinearity into ONNs is challenging due to the weak photon–photon interaction. Recent advances rely on resonant cavities, laser-cooled atoms and femtosecond pulses in (millimetre-) long waveguides to enhance the nonlinearity, pointing to a promising potential of speed-of-light activation, but these systems are either slow due to the cavity lifetime or limited coupling strength between atomic levels (slow Rabi oscillations), or bulky due to the device and instrument dimensions. Alternatively, most ONNs implement the nonlinear activation function digitally or optoelectronically, resulting in latency or energy constraints. A fast, compact, and low-energy C3 nonlinearity has yet to be developed. Furthermore, to meet the demanding scaling of DNN models, photonic neuromorphic devices should be scalable (C4), with high density, to extend the computing power while reducing fabrication cost. Furthermore, the ONN architecture should be scalable in the number of neurons to support large DNN models (C5).

In this Article, we introduce a compact VCSEL-ONN architecture that achieves all five criteria (C1–C5) simultaneously. We explore the potential of high-speed VCSELs for next-generation ONNs, especially now that VCSEL technology has matured to meet the demanding industrial requirements in three-dimensional (3D) sensing and LiDAR, high-speed optical communications and laser printing. Our ONN system utilizes (i) micrometre-scale VCSEL transceivers for high-speed (gigahertz) data transmission with phase coherence over the entire array via injection locking, (ii) coherent detection for low-energy weighted accumulation and (iii) holographic data movement as optical dendritic fanout for parallel computing. We experimentally achieve the best-in-class ONN with (C1) full-system energy efficiency (including the energy of optics and the proposed digital electronics) reaching 7 femtoOP mm−2 s−1 and (C3) inline nonlinearity based on homodyne detection with instantaneous response. Furthermore, the system is (C4) scalable through existing mature wafer-scale fabrication processes and photonic integration, while high-speed (>gigahertz) time multiplexing enables the system to (C5) freely scale to run models with up to tens of billions of neurons (a model with 79,400 parameters is demonstrated, which is 100 times larger than other integrated ONNs, Supplementary Table III).

Results Schematic

Our VCSEL-ONN architecture consists of a sequence of layers (Fig. 1b). Each layer computes a matrix-vector multiplication Xn(1) = Yn(1) followed by a nonlinear activation function fNL(.). Our scheme imitates the ‘axon-synapse-dendrite’ architecture in biological neurons. As shown in Fig. 1c, we encode the input vector Xn(1) in i time steps to the amplitude or phase of a coherent laser oscillator (labelled ‘axon’), whose beam is dendritically fanned out to copies for parallel processing. We map the weight matrix Wn(1) in i time steps...
with phase encoding $\sin(\phi_X(t)) \propto W_{ij}$ using a ‘weight server’ consisting of laser transmitters. Each weighting laser beats with a copy of the input laser on a photo-receiver, producing the homodyne product between the two laser fields (Fig. 1d), as detailed in Supplementary Section I. The resulting photocurrent is accumulated over $t$ time steps, yielding

$$I_j \propto \sum_i A_{W,ij} \sin(\phi_{W,ij} - \phi_{X,i})$$

where $A_{W,ij}$ and $\phi_{X,i}$, $A_{W,ij}$ and $\phi_{W,ij}$ respectively, are the amplitude and phase of the input and weight lasers. Homodyne multiplication allows linear multiplication $f_{ij}(\cdot) \propto A_{X}(t) \sin(\phi_{X}(t)) = X_{W,ij}$ when the input data is amplitude-encoded $A_{X}(t) \propto X_{ij}$, or the nonlinear operation $f_{ij}(\cdot) \propto \sin(\phi_{X}(t)) - \phi_{X}(t) = W_{ij} - X_{ij} - X_{ij}^2 + W_{ij}^2$ with phase-encoding $\sin(\phi_{X}(t)) \propto X_{ij}^{\text{Methods}}$. The input–output response of the two data modulation schemes is modelled as in Supplementary Fig. I.

With the phase-encoding scheme, we incorporate the detection-based optical nonlinearity in our VCSEL-ONN. As shown in Supplementary Fig. I.b, programming the phase of the weight laser tunes the strength of our homodyne nonlinearity. The effectiveness of our homodyne nonlinearity is verified in neural network training, showing a performance similar to that of the rectified linear unit (ReLU) nonlinear activation in handwritten digit and letter classification, as well as fashion product classification (Supplementary Table I). As homodyne detection relies on the photoelectric effect, where an electron is elevated to the conduction band by the absorbed photon, the process is nearly instantaneous, with a time delay of tens of attoseconds\(^{12}\). The resulting latency is as short as the optical pulse per symbol, which can be a few femtoseconds in principle. This is in contrast to the nanosecond delay with digital\(^{60,62}\) and electro-optic\(^{63,64}\) nonlinearities, and cavity- or atom-based optical nonlinearities\(^{65,66}\). Its implementation with a photodetector is ultracompact, without instrumental complexity (for example, ultrashort laser pulses\(^{67}\)).

Based on space–time multiplexing and fanout data-coping, our system is optimized for computing at high density and energy efficiency. It performs matrix-vector multiplication using $j$ time steps and $f$ coherent receivers. With the axon input laser shared among $f$ channels ($f$-time parallelism), the number of devices scales linearly with $O(f)$, whereas these requirements in CMOS-based microprocessors\(^{68,69}\) and integrated ONN circuits\(^{42,50}\) scale quadratically $O(1 \times f)$. Our system is thus substantially simplified, with reduced device counts. As batch operations are required in many machine learning tasks, the beams in the weight server can be broadcast for processing a batch of $k$ input vectors simultaneously, as in the simplified schematic shown in Supplementary Fig. 7. Matrix–matrix multiplication $X_{i \times j} W_{j \times k} = Y_{i \times k}$ is enabled with $k$ input encoders, $j$ weight transmitters and $t$ time steps. The device count scales with $O(k \times j \times k)$; this would otherwise require $O(i \times j \times k)$ scaling.

**Experimental results**

Our VCSEL-ONN supports a compact 3D hybrid layout (Fig. 2a) with arrays of VCSELs (A2) bonded on a CMOS driver chip (A1) for data transmission, a phase mask (A3) for beam fanout, and detector arrays (A4) for homodyne multiplication.

To implement the scheme, we engineered a scalable, high-density, phase-stable source with individually addressable VCSEL arrays of tunable, coherent outputs. We fabricated $5 \times 5$ VCSELs at high density with semiconductor heterostructure microresonators with equal $x$- and $y$-direction pitches of 80 μm (Fig. 2d; Methods). All the VCSELs are individually addressable with forward biasing above the lasing threshold using a battery. Each VCSEL emits 100 μW of light with a wall-plug efficiency of 25%. The 3-dB bandwidth of our fabricated devices is $\sim 2$ GHz, limited by the photon lifetime at the cavity Q-factor of $10^3$ (Supplementary Fig. 9). We exploit VCSELs for analogue data-encoding at a clock rate of $1$ Giga-symbols per second (GS s\(^{-1}\)) with 8 bits of precision: one-billion neurons are activated in $1$ ms (Fig. 2b).

We note that state-of-the-art VCSELs with a 3-dB bandwidth of 45 GHz (ref. 39) could further improve our computing rates. The emission wavelength of our VCSELs over the $5 \times 5$ array is 974.0 ± 0.1 nm. This excellent wavelength homogeneity enables parallel injection locking over the whole array to a leading laser for coherent detection (Methods). An injection optical power of $1$ μW per VCSEL is sufficient to achieve a stable phase lock, with a locking range of $1.7$ GHz (Fig. 2g).

Tuning the individual VCSEL resonance over the locking range, with varying driving voltages, allows phase tuning in the range $(-\pi/2, +\pi/2)$, with a π-phase-shift voltage, $V_{\phi}$, of $4$ mV (Fig. 2h). Such a low $V_{\phi}$ allows phase-only linear modulation with negligible amplitude coupling\(^{40}\) and negligible crosstalk between neighbouring channels.

We use a single VCSEL array to encode both the input activation and weights. Sharing beam paths improves the interferometric stability in homodyne detection. Among the 25 VCSELs, 24 encode weights forming the weight server, while the corner VCSEL encodes the activations (Fig. 2f). Limited by the large dimension of our diffractive optical element (DOE), the corner laser is separated from the main beams and then fanned out to $9 \times 9$ spots (Methods). This beam separation is not necessary with pitch-size DOEs, as photonic integration of VCSEL arrays with DOEs for fanout beam copying has been matured for volume production in industry\(^{41}\). Each copy of the $X$ beam is superimposed to a weight laser beam $W_{ij}$ with a beamsplitter. The combined beams are received with a 2D fibre-based detector array, where each detector connects to a switch integrator charge amplifier (Methods) that accumulates the homodyne photon currents.

We characterized the computing accuracy of homodyne interference in our neural network implementation (Fig. 3). We utilized two injection-locked VCSELs to construct a vector–vector multiplication unit based on our physical system’s unique nonlinearity $f_{ij}(X_{ij}, W_{ij})$ (Fig. 3c), which differs from conventional multiplication\(^{43}\) due to the complex-valued nature of the VCSEL network’s outputs. We encode two vectors $X_{ij}$ and $W_{ij}$, each with $i = 10,000$ normally distributed random values, to a VCSEL at a clock rate of $R = 1$ GS s\(^{-1}\) with peak-to-peak voltage of $4$ mV. The signals are a.c. coupled to remove the slow thermal drifts (Methods). The experimental time trace agrees well with the calculation in Fig. 3d. The standard deviation of $y$ and $y$ residuals in Fig. 3e,f reveals a computing accuracy of $98\%$ (6 bits of precision), limited mainly by the phase instability of the set-up and the frequency response of the injection-locked VCSELs. The accuracy can be improved in the future with better photonic integration and VCSELs of higher bandwidth, although the present accuracy is sufficient for a wide range of machine learning tasks\(^{44,45}\).

We deployed a neural network inference on our VCSEL-ONN to classify handwritten digits in the Modified National Institute of Standards and Technology (MNIST) database. To this end, we developed a training algorithm with PyTorch using our unique nonlinear weighting function $f_{ij}(W_{ij}, X_{ij})$. Figure 4a shows the trained three-layer model (size $28 \times 28 \rightarrow 100 \rightarrow 10 \rightarrow 10$). Each image, with $28 \times 28$ pixels, is flattened and encoded in 784 time steps to an input VCSEL (Fig. 4b) at a driving voltage of $4$ mV. The 100 weight vectors in the first hidden layer.

Table 1 | Figures of merit of VCSEL-ONN

| Criteria | Description | VCSEL-ONN |
|----------|-------------|------------|
| C1 | Energy efficiency, $\epsilon$ | $71$ fJ/OP |
| C2 | Compute density, $\rho$ | $6$ teraOP mm$^{-2}$ s$^{-1}$ |
| C3 | Inline nonlinearity | Instantaneous response |
| C4 | Hardware scalability | Wafer-scale volume production |
| C5 | Model size | $79,400$ parameters |
are flattened and encoded one weight vector per VCSEL. Ideal spatial multiplexing allows processing of 100 weight channels simultaneously; however, limited by the arbitrary waveform generator (AWG) hardware, the data are taken with multiple acquisitions (five VCSELs per acquisition) at a clock rate of 100 MS s\(^{-1}\), although the VCSEL bandwidth allows homodyne interference at >1 GS s\(^{-1}\) (Fig. 3c). By switching the AWG channels and translating the VCSEL chips to different arrays in the \(x\) and \(y\) directions, a total of 100 VCSEL devices from five arrays are used to compute in the first layer. The interference signal between the image data and a weight vector is compared to the digitally calculated result in Fig. 4b. We obtained ~6 bits of compute precision, similar to the result in Fig. 3b. The signal-to-noise ratio (SNR) in the time trace is 135, limited

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**Fig. 2** Experimental scheme of VCSEL-ONN. a, Proposed architecture with 3D connectivity and photonic integration. In a 2D VCSEL array, the centre (blue) is used as the axon and the others (red) as weight VCSELs. The axon beam is fanned out to \(j\) copies, each overlapping a weighted beam onto a photodetector, generating photon currents corresponding to the homodyne product of the two laser fields. b, Fabricated VCSEL arrays. Arrays of 5 x 5 wire-bonded VCSELs on a GaAs substrate. c, Scanning electron microscopy image of a VCSEL emitter during device processing before adding the top metal connectors. d, Analogue data-encoding with an on-chip VCSEL transmitter operating at 1 GS s\(^{-1}\). The MIT logo in the upper plot is constructed with a time sequence of 400 symbols. A 28 x 28-pixel image with a handwritten digit is flattened and encoded in 784 ns. e, Optical fanout. A single VCSEL emitting data at 1 GS s\(^{-1}\) is fanned out to \(j = 9 \times 9\) spots using a diffractive optical element. A camera at the Fourier plane records the resulting beam grid. f, Experimental set-up of the VCSEL-ONN apparatus. The input data (\(X_n\), highlighted) is encoded onto the corner VCSELs, and the weight matrix \([W_n^1, \ldots, W_n^j]\) is mapped to the other VCSELs. The input VCSEL is separated from the beam arrays using a beam magnifier (L1 and L2) and D-shaped mirror. DOE, diffractive optical element; BS, beamsplitter; PD, photodetector; PBS, polarizing beamsplitter. g, Injection locking range. This is measured by monitoring the beatnote between the leader laser and each VCSEL (Supplementary Section VII). Within the locking range of 1.7 GHz, the VCSELs emit coherently. h, Low-\(V_\pi\) and linear modulation. Driving the VCSEL resonance over the locking range allows a phase shift of (−\(\pi/2, \pi/2\)), \(V_\pi = 4\) mV. 

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**Fig. 3** Homodyne data processing in VCSEL-ONN. a, Measured homodyne interference as a function of laser detuning. The blue-detuned and red-detuned channels are indicated. b, Measured signal-to-noise ratio (SNR) as a function of laser detuning. The SNR increases with increasing laser detuning. c, Measured homodyne interference as a function of laser detuning for different weight vectors. The homodyne interference is higher for the weight vector corresponding to the handwritten digit. d, Measured signal-to-noise ratio (SNR) as a function of laser detuning for different weight vectors. The SNR is higher for the weight vector corresponding to the handwritten digit. e, Measured homodyne interference as a function of laser detuning for different weight vectors. The homodyne interference is higher for the weight vector corresponding to the handwritten digit. f, Measured signal-to-noise ratio (SNR) as a function of laser detuning for different weight vectors. The SNR is higher for the weight vector corresponding to the handwritten digit. g, Measured homodyne interference as a function of laser detuning for different weight vectors. The homodyne interference is higher for the weight vector corresponding to the handwritten digit. h, Measured signal-to-noise ratio (SNR) as a function of laser detuning for different weight vectors. The SNR is higher for the weight vector corresponding to the handwritten digit.
by the photon shot noise (Supplementary Fig. 4). The photocurrent at
each channel is accumulated over time with a custom-made time inte-
grator (Methods). The integrated values from the 100 channels are
serialised, forming an input vector feeding into the second hidden
layer. The weights in the second hidden layer are implemented with
ten weighting VCSELs and the interference signal is integrated.
Figure 4c shows the real-time integration of the interference signal for
processing an image in layer 2. The image classification is read out by
the max integrating voltage of the ten VCSEL channels (Fig. 4c,d). Run-
nning inference over a dataset of 1,000 MNIST test images, with a total
of 158.8 million operations, we obtain an accuracy of (93.1 ± 2.0)%,
which is 98% of the model’s accuracy in the simulation (95.1%).

System performance
Energy efficiency. Our system enables efficient computing with
low-energy VCSEL transmitters and optical parallelism. Supplementary
Table II summarises the energy consumption of each component. The
clock rate of 1 GS s⁻¹ used in the calculation is demonstrated in Fig. 3.
Due to the ultralow $V_p = 4$ mV operation, data-encoding with a VCSEL
modulator consumes less than 4 nW (corresponding to 4 aJ per symbol
at 1 GS s⁻¹), which is six orders of magnitude more efficient than that
of previous ONN schemes with thermal phase shifters, microring
resonators, optical attenuators and EO modulators, which operate with
several milliwatts of electrical power. The main optical energy
consumption in our system is for laser generation, and we note that
VCSEL sources are efficient laser generators with a wall-plug efficiency
of 25% in our demonstration and over 57% in record⁴. Our optical
ergy efficiency, including the electrical power for laser generation
and data modulation, is 2.5 fJ/OP (Methods), which is ~20× higher than that
of its electronic counterparts (Fig. 5), where improving the throughput
density is fundamentally challenging due to limited heat dissipation
per chip area. In other ONN configurations, high throughput density
requires tilting of photonic devices at high density, which often leads
to crosstalk between neighbouring channels and decreased compute
accuracy. The channel crosstalk in our VCSEL-ONN is eliminated with
VCSEL modulators with ultralow $V_p$.⁴

Potential compute density. High compute density is achievable based
on compact and dense VCSEL arrays in the 3D architecture. VCSELs
are excellent candidates for high-density computing, with a pitch of
80 µm per fabricated device. With optimized optoelectronic integra-
tion and pitch matching, the compute density in our system could
reach $\rho = 6$ teraOP mm⁻² s⁻¹ (Methods), which is ~20× higher than that
of its electronic counterparts (Fig. 5), where improving the throughput
density is fundamentally challenging due to limited heat dissipation
per chip area. In other ONN configurations, high throughput density
requires tilting of photonic devices at high density, which often leads
to crosstalk between neighbouring channels and decreased compute
accuracy. The channel crosstalk in our VCSEL-ONN is eliminated with
VCSEL modulators with ultralow $V_p$.⁴

Latency. Ultralow latency for nonlinear activation is achieved by incor-
porating detection-based nonlinearity. In our scheme, each detection
event generates photon currents instantaneously, and the photon
currents are accumulated in the time integrator for $t$ time steps before
being read out. The transit time for photon electrons moving from
the photodiode to the charging capacitor, which leads to latency in
encoded in time steps to the phase of the \( b \). There are 100 and 10 neurons, respectively, in the first and second hidden layers. The weight matrix with 100 VCSEL transmitters. Our benchmarking of digit classification achieved results in matrix-vector multiplication (blue) from 100 readout channels. By harnessing the powerful scalability of the VCSEL platform, we have demonstrated a homodyne-based ONN using more than 100 coherent VCSEL transmitters. Our benchmarking of digit classification achieved an accuracy of 93.1% (over 98% of ground truth). With optimized standard photodetectors, is negligible compared to the integration time. So, the latency due to nonlinear activation is negligible. The processing time is dominated by the data-encoding and time integration, which could be as short as 30 ns for a full-size MNIST image at a clock rate of \( R = 25 \text{ GS} \text{ s}^{-1} \) (Supplementary Fig. 12).
The electronic systems Google TPU, NVIDIA GPU and Graphcore are ASICs optimized for deep learning tasks, with energy efficiency and compute density reaching 1 pJ/OP (Graphcore IPU Gen-2) and 0.35 teraOP mm$^{-2}$ s$^{-1}$ (NVIDIA A100). For the ONN optical performance, the energy efficiency accounts for the electrical power in laser generation and data-encoding, and the compute density is calculated from the chip area for matrix operations. For ONN full-system performance, the energy consumption and compute density account for laser generation, data-encoding, nonlinear activation, data readout, signal amplification, ADCs, DACs and memory access. In this work, the energy bound due to electronics at -1 pJ per neuron is reduced with spatial fanout and time-domain fan-in (Supplementary Table II). The compute densities of this work are potential values, estimated with present-day technology of photonic integration and electronic packaging. The performances of the ONN techniques are summarized in ref. 22 and plotted here. The data in the plot are listed in Supplementary Table IV.

To the ultralow energy consumption of the VCSELs (<5 a per symbol), rapid programmability with high-speed updating of weights in our system is readily applicable to real-time neural network training. Although the exponential scaling of neural network models has outpaced the development of electronic processors, this new type of optoelectronic processor with orders-of-magnitude improvement may enable us to continue the scaling of computing power in the post-Moore’s law age.

Online content
Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41566-023-01233-w.

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Methods

Device fabrication

The VCSEL arrays were fabricated with a small pitch of 80 μm to maximize the device density. The VCSEL cavities are based on semiconductor heterostructure microresonators with two AlGaAs/GaAs distributed Bragg reflectors (DBRs) as cavity mirrors and a stack of InGaAs quantum wells as the gain medium. The 5×5 cavity arrays were patterned by UV lithography and etched by an inductively coupled plasma reactive ion beam. Each cavity, with an outer diameter of 30 μm, was oxidized to an aperture of 4.5 μm to suppress higher-order transverse modes. To improve the laser stability, the entire chip was clad with a polymer layer, and the areas of the VCSEL cavities were reopened. An Au-deposited p-contact of each VCSEL was connected to a signal pad, which was wire-bonded to a printed circuit board linked to external drivers. All the VCSELs share a common ground (golden bars in Fig. 2b). The cross-section of the VCSEL was designed with 1% ellipticity, which allows a polarized laser output with an improved extinction ratio.

Homodyne multiplication

Homodyne interference allows linear and nonlinear operations based on equation (1). The lasers in the weight server are phase-modulated with \( \sin(\phi_w(t)) \propto W_x \). Linear operation is activated when the input vector is amplitude-encoded with \( A_x(t) = X_i \) (Supplementary Fig. 1a). \( A_w \) is constant because the VCSELs for encoding weights are phase-only modulators. When the input and weight lasers are biased in phase (\( \phi_w = 0 \)), the interference signal is simplified to \( \Delta(t) \propto \sin(t) \sin(\phi_w(t)) \sin(\phi_x(t)) \). Nonlinear operation is allowed when the input vector is phase-encoded with \( \sin(\phi_x(t)) \propto X_i \). The generated photocurrent on the detector is \( \Delta(t) \propto \sin(\phi_w(t) - \phi_x(t)) = W_i \sqrt{1 - X_i^2} = \sin^{-1}(X_i) \) when \( W_i \) is large enough. The input–output response of the linear and nonlinear models is simulated in Supplementary Fig. 1b. In linear operation, when both laser fields are phase-only modulated, the non-interference terms are direct currents that can be decoupled from the a.c. terms, so the inference can be detected with an unbalanced single detector for system simplicity.

Injection locking

As shown in Fig. 2f, the beam of the leader laser, passing through a DOE, is reflected to the VCSEL arrays using a polarizing beamsplitter (PBS). At the Fourier plane of the coupling lens, the leader laser splits to a beam grid of spacing equal to the pitch of the VCSELs. The polarization of the PBS is aligned at 45° with respect to that of the VCSELs. So, half of the leader laser power is coupled to the VCSEL cavity, locking the phase of the remaining VCSEL oscillators. The other half, being reflected by the VCSEL front DBR, is rejected by the PBS to avoid falling onto the homodyne detectors and leading to undesired interference. Such an injection-locking technique has been demonstrated recently to achieve a high injection ratio. To simultaneously injection-lock the whole array, we tuned all the VCSELs to the wavelength of the leader laser and placed all partial sums in each layer converge to a mean value around 0, which allows one to maximize the experimental signal level without being bound by the dynamic range limit. We utilize the cross-entropy loss function and retrieve the gradients in each iteration in a model implemented in PyTorch. A large learning rate is set to start the training and is gradually reduced to optimize accuracy and avoid overfitting. The training model was modified to implement training on handwritten letter classification and fashion product classification, to verify the effectiveness of our nonlinearity on different tasks.

Energy efficiency

The VCSEL emits \( P = 100 \mu W \) of optical power while consuming \( P_{\text{DC}} = 400 \mu W \) of electrical power. The injection-lock power is \( P_{\text{INJ}} = 1 \mu W \) per VCSEL. The power for data modulation is \( P_{\text{M}} = V_\pi/R_{\text{VCSEL}} \) (3.6 nW), with \( R_{\text{VCSEL}} = 4.3 \Omega \) and \( V_\pi = 4 \text{ mV} \). The maximum clock rate of the system is \( f = 1 \text{ GS}^{-1} \). With a fanout of \( f = 9 \times 9 \), the optical energy efficiency is \( (P_x + P_{\text{INJ}} + P_{\text{M}})/(2fR_{\text{VCSEL}}) = 2.5 \text{ fJ/OP} \), which is dominated by the laser power. The full-system energy efficiency can reach 7 fJ/OP with the proposed electronic components discussed in Supplementary Table IV.
Potential compute density
The chip area is dominated by the VCSEL transmitters (A2, 80 × 80 μm² per device) because (1) the silicon detector arrays (A4) are compact (for example, detector pixels are commercially available with a pitch size of <0.8 × 0.8 μm² for an image sensor), (2) the integration of phase masks and microlenses (A3) on the VCSEL output facet is a mature technology in the industry²⁹, and (3) an area of 80 × 80 μm² can store 38,000 8-bit digital values (A1) (a useful static random access memory (SRAM) cell). Fourier-transforming the phase-masked beam profile, each VCSEL (NA ≈ 1) metalens at the VCSEL output facet (diameter of ~5 μm) can be implemented with a high-numerical-aperture fanout copying. Focusing the VCSEL output (mode field diameter of ~5 μm) can be improved with weight broadcasting (Supplementary Fig. 8).

Potential system compactness
The 3D system can be compact in volume. The vertical spacing between the VCSEL chip and the detectors is mainly limited by the focal length (f) of the lenses used for (1) focusing each VCSEL output to the corresponding detector pixel and (2) Fourier-transforming the phase-masked beam profile (fanout copying). Focusing the VCSEL output (mode field diameter of ~5 μm) can be implemented with a high-numerical-aperture metalens at the VCSEL output facet (f < 10 μm) (ref. 56). For Fourier-transforming the phase-masked beam profile, each VCSEL beam is fanned out to j copies with a spacing to match the pitch (d = 80 μm) of the VCSELS (Fig. 2a). The diffraction angle of the nth-order beam from the DOE is m × φ, with tan(mθ) = m × d/f. For the fanout factor j = 32 × 32, the DOE diffracts beams of up to m = 116 orders. So a focal length f = md/tan(mθ) = 4.5 mm is required with diffraction angle θ = 1° (diffraction angles θ ranging from 0.1 to 10° are commercially available; Holo/OR). The vertical spacing (on the millimetre scale) is similar to the chip size of 32 × 32 VCSELS. Note that the technology for the photonic integration of VCSELS chips, microlens arrays and DOEs is mature for volume production⁴¹.

Data availability
All the data that support the findings of this study are included in the main text and Supplementary Information. The data are available from the corresponding authors upon reasonable request.

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Acknowledgements
This work is supported by the Army Research Office under grant no. W911NF17-1-0527, NTT Research under project no. 6942193 and NTT Netcast award 6945207. I.C. acknowledges support from the National Defense Science and Engineering Graduate Fellowship Program and National Science Foundation (NSF) award DMR-1747426. L.B. is supported by the National Science Foundation EAGER programme (CNS-1946976) and the Natural Sciences and Engineering Research Council of Canada (PGSD3-510753-2018). L.A. acknowledges support from the NSF Graduate Research Fellowship (grant no. 1745302). S.R. acknowledges financial support from the Volkswagen Foundation via the project NeuroQNet. We thank S. Bandyopadhyay and C. Brabec of MIT and Y. Cui of TUM for comments on the manuscript. We also thank D.A.B. Miller of Stanford University, N. Harris and D. Bunandar of Lightmatter, and S. Lloyd of MIT for informative discussions.

Author contributions
Z.C., R.H. and D.E. conceived the experiments. Z.C. performed the experiment, assisted by A.S., R.D. and I.C. A.S. conducted high-speed measurements on the VCSEL transmitters and developed the integrating electronics. R.D. created the software model for neural network training, I.C. performed electronic packaging on the VCSEL arrays. L.A. assisted with assembling an initial set-up for testing VCSEL samples. A.S. and L.B. assisted with discussions on the experimental data. T.H., N.H., J.A.L. and S.R. designed and fabricated the VCSEL arrays and characterized their performance. R.H. and D.E. provided critical insights regarding the experimental implementation and results analysis. Z.C. wrote the manuscript with contributions from all authors.

Competing interests
Z.C., D.E. and R.H. have filed a patent related to VCSEL ONNs, under application no. 63/341,601. D.E. serves as scientific advisor to and holds equity in Lightmatter Inc. A.S. is a senior photonic architect at Lightmatter Inc. and holds equity. Other authors declare no competing interests.

Additional information
Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41566-023-01233-w.

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Peer review information Nature Photonics thanks Xingyuan Xu and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

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