Modeling of the Output and Transfer Characteristics of Graphene Field-Effect Transistors

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Abstract—We obtain the output and transfer characteristics of graphene field-effect transistors by using the charge-control model for the current, based on the solution of the Boltzmann equation in the field-dependent relaxation time approximation. Closed expressions for the conductance, transconductance and saturation voltage are derived. We found good agreement with the experimental data of Meric et al. [Nature Nanotechnology 3, 684 (2008)] without assuming carrier density-dependent velocity saturation.

Index Terms—Graphene, high field effect, saturation velocity, simulation, transistors.

I. INTRODUCTION

In recent years, graphene has emerged as a novel mono-layer material with exotic physical properties [1, 2] for applications in high performance electronic devices [3, 4]. Namely the relation between the charge carrier energy $E$ and the two-dimensional (2D) wave vector $k = \sqrt{k_x^2 + k_y^2}$ is linear i.e. $E = \hbar v_F k_x$, where $v_F \approx 10^6$ cm/s is the Fermi velocity, thereby reducing the band gap to a single point (Dirac point) [1]. In this framework all carriers have a velocity with the same absolute value that is one order of magnitude larger than in conventional III-V materials [5], making graphene a promising candidate for high-speed nanoelectronics.

Recently, graphene field-effect transistors (GFETs) were successfully fabricated and exhibited $I$-$V$ characteristics similar to conventional silicon MOS transistors [3]. Low field mobilities were however strongly degraded by the presence of coulombic space charge in the neighboring oxides, whereas nonlinearities in the current-voltage characteristics were interpreted as caused by carrier velocity saturation for which the value would depend on the carrier concentration induced by gate voltages in the 2D graphene mono-layer.

In this paper, we developed a charge-control model for GFETs that does not require the assumption of carrier density-dependent saturation velocity to reproduce the experimental characteristics. Our model also provides closed form analytic expressions for the saturation voltage, conductance and transconductance of the device.

II. TRANSISTOR STRUCTURE

Fig. 1 shows a schematic of the GFET, where the graphene mono-layer sits on a thick SiO$_2$ layer with capacitance $C_{\text{back}}$ on top of a back gate that controls the source and drain resistance $R_s$ at the same time as the channel threshold voltage with bias $V_{\text{gback}}$. A top gate of length $L$, separated from the graphene mono-layer by a thinner oxide with capacitance $C_{\text{top}}$, controls the carriers in the channel with $V_{\text{gtop}}$. For the sake of comparison with experiment, we will only consider p-channel device operation, but our model is valid for n-channel
operation as well.

III. MATH

In order to model the transport characteristics of the GFET, we split the carrier distribution function into its even and odd parts so \( f(\vec{k}) = f_{\text{even}}(\vec{k}) + f_{\text{odd}}(\vec{k}) \). Then, it is well known that in the presence of randomizing collisions, and even in high fields, the Boltzmann transport equation can be written as [6]

\[
\frac{eF}{h} \frac{\partial}{\partial k_x} f_{\text{even}}(\vec{k}) = -\frac{1}{\tau_{\text{tot}}(\vec{k})} f_{\text{odd}}(\vec{k})
\]  

with \( \frac{1}{\tau_{\text{tot}}(\vec{k})} = \sum_i \frac{1}{\tau_i(\vec{k})} \) and the \( i \)-index indicates a particular scattering mechanism. \( F \) is the electric field. In the presence of strong inter-carrier scattering for high carrier concentration, the even part of the distribution is thermalized at an electronic temperature \( T_e \), and reads

\[
f_{\text{even}}(\vec{k}) = \frac{1}{1 + \exp \left( \frac{\hbar v_F (k - k_F)}{k_BT_e} \right)}
\]  

where \( k_F = k_F(x) \) defines the carrier concentration along the channel. In p-channel, the current can be calculated as

\[
I = 4e \frac{1}{L} \sum_k v(\vec{k}) f_{\text{odd}}(\vec{k})
\]  

where \( L \) is the channel length, and the factor 4 accounts for the spin and the two-fold degeneracy of the Dirac point [1]. Here \( v(\vec{k}) = v_F (\cos \theta, \sin \theta) \) and \( \theta \) is the angle between the electric field and the vector \( \vec{k} \). Then for \( \hbar v_F k_F \ll k_BT_e \) one can approximate \( \frac{\partial}{\partial k_x} f_{\text{even}}(\vec{k}) \) by a delta function centered around \((k - k_F)\). After integration, and given \( k_F = \sqrt{\pi p} [7] \), the hole current in a 2D graphene layer reads

\[
I = W \frac{2e^2}{\hbar} F v_F \tau(p) \sqrt{\pi p}
\]

where \( W \) is the graphene layer width, \( p \) is the hole concentration and \( \tau(p) \) is the relaxation time for a particular carrier concentration \( p \). In the high field regime, we assume

\[
\tau(p) = \tau_0/(1 + F/F_c)
\]

where \( F_c \) is the critical field for the onset of high energy collisions such as remote phonons [8], for instance, \( \tau_0(p) = \tau_0 \sqrt{p/N_i} \) is the low field relaxation time dominated by scattering with charged impurities with density \( N_i [7] \), and \( \tau_0 \) is a time constant. By setting \( \mu_0 = (e/\hbar) v_F \tau_0 \sqrt{p/N_i} \), one recovers the conventional current expression

\[
I = W e p v(F)
\]

with \( v(F) = \mu_0 F/(1 + F/F_c) \), where the low field conductance \( \sigma_{lf} \propto p \), as observed experimentally [1, 7].

In the charge-control model, close to the Dirac point, one can use the mass action law [9] to get

\[
p(x) = \frac{Q(x)}{2e} + \sqrt{\left( \frac{Q(x)}{2e} \right)^2 + p_0^2}
\]

where \( p_0 \) is the minimum sheet carrier concentration [7] and \( Q(x) \) is the electric charge density along the channel from source to drain given by \( Q(x) = -C_{\text{top}} \left[ V_{g0} - V(x) \right] \) in the gradual channel approximation [10]. Here \( V_{g0} = V_{g_{\text{top}}} - V_0 \) where \( V_0 \) is the threshold voltage of the GFET and is defined as [3]

\[
V_0 = V_{g_{\text{top}}}^0 + \frac{C_{\text{back}}}{C_{\text{top}}} \left( V_{g_{\text{back}}}^0 - V_{g_{\text{back}}} \right)
\]

where \( V_{g_{\text{top}}} \) and \( V_{g_{\text{back}}} \) designate the top and back gate voltages at the Dirac point respectively. However for \( \frac{Q(x)}{2e} \ll p_0 \), which is the case for all bias conditions considered in this analysis, one can write

\[
p(x) = \frac{Q(x)}{e}.
\]

By integrating the current equation (5) from source to drain as in conventional MOS devices [10], and by taking into account the series resistance \( R_s \) at the source and drain [3], one gets

\[
I_d = \frac{W \mu_0 V_c}{2LC_{\text{top}} \left| V_{ds} \right| - \frac{2}{2} \left| I_d \right| R_s + V_c} \left[ Q(L)^2 - Q(0)^2 \right]
\]
where $Q(L) = -C_{top}(V_{g0} - V_{ds} - I_d/R_s)$ and $Q(0) = -C_{top}(V_{g0} + |I_d/R_s|)$. Solving for $I_d$ one obtains a closed expression for the drain current

$$I_d = \frac{1}{4R_s} \left[ V_{ds} - V_c + I_0 R_s + \sqrt{(V_{ds} - V_c + I_0 R_s)^2 - 4I_0 R_s V_{ds}} \right]$$

(10)

where $V_{ds}$ is the drain-source voltage, $I_0 = 2(W/L)\mu_0 V_c C_{top}(V_{gtop} - V_0 - V_{ds}/2)$ and $V_c = F_c L$.

From here, the low drain-source bias conductance is readily calculated by taking the derivative of the current expression (10) with respect to $V_{ds}$ as $V_{ds}$ goes to zero. One gets

$$g_{ds}(V_{ds} \to 0) = \frac{-V_{g0}}{2R_s V_{g0} - R_s V_c}$$

(11)

where $1/R_c = (W/L)\mu_0 C_{top} V_c$, so that $R_c V_c$ is independent on $V_c$, as is the conductance at low drain bias. The low drain-source bias resistance reads

$$R_{ds} = \frac{1}{g_{ds}} = 2R_s - \frac{R_c V_c}{V_{g0}}$$

(12)

which establishes a linear relation between $1/g_{ds}$ and $1/V_{g0}$ with a slope given by $R_c V_c$ (versus proportional to the mobility) and an asymptotic conductance value for large $V_{g0}$ reaching $2R_s$.

In the same context, one obtains the expression for the drain-source saturation voltage as a function of the top gate voltage $V_{g0}$ by solving for $V_{ds}$ after setting the derivative of the current (10) with respect to $V_{ds}$ equal to zero which yields

$$V_{ds(sat)} = \frac{2\gamma V_{g0}}{1 + \gamma} + \frac{1 - \gamma}{(1 + \gamma)^2} \left[ V_c - \sqrt{V_c^2 - 2(1 + \gamma)V_c V_{g0}} \right]$$

(13)

with $\gamma = R_c/R_s$. Substituting the drain-source saturation voltage (13) into the current equation (10) enables us to obtain the expression of the saturation drain current as a function of the top gate voltage which reads

$$I_{d(sat)} = \frac{\gamma}{R_s(1 + \gamma)^2} \left[ -V_c + (1 + \gamma)V_{g0} + \sqrt{V_c^2 - 2(1 + \gamma)V_c V_{g0}} \right]$$

(14)

By taking the derivative of the saturation current with respect to the top gate voltage one derives the expression for the transconductance at saturation,

$$g_{ms}^{sat} = \frac{1}{R_s + R_c} \left[ 1 - \frac{1}{\sqrt{1 - 2(1 + \gamma)V_{g0}/V_c}} \right]$$

(15)

Additionally, the expression for the electric potential as a function of position along the channel length can be derived from the current equation (10) and is given by

$$V(x) = V_{g0} - V_i + \sqrt{(V_{g0} - V_i - I_d R_s)^2 + \frac{2I_d x}{W\mu_0 C_{top}}}$$

(16)

where $V_i = I_d/(W\mu_0 F_c C_{top})$ and the source is located at $x = 0$.

IV. RESULTS

In this section we discuss the results for the case of $V_{gback} = -40$ V ($V_0 = 2.36$ V) and of $V_{gback} = +40$ V ($V_0 = 0.64$ V). In the former, the source and drain regions of the GFET are p-type, while in the latter, they are n-type; we notice that both threshold voltages are positive, and in both cases the top gate is biased negatively to form a p-channel.

A. $V_{gback} = -40$ V

Figs. 2 show the plots of both the low-bias conductance $g_{ds}$ as a function of the top gate voltage, and the low-bias resistance $R_{ds}$ as a function of the inverse of the top gate voltage in the device configuration investigated in [3]. In fig. 2a the solid curve is calculated from (11) with the mobility ($\mu_0 = 550$ cm$^2$/V·s) and source resistance value ($R_s = 700$ $\Omega$) as explicitly given in [3] which gives a good agreement with the experimental data close to the minimum conductance, but underestimate the former by about 20% at high top gate bias. The dashed curve is the best fit of (11) with the experimental conductance with $\mu_0 = 600$ cm$^2$/V·s and $R_s = 500$ $\Omega$, which indicates that the discrepancy with the previous data is essentially due to a different value of the source resistance. In fig. 2b one can see that the experimental resistance values display a linear relation with $1/V_{g0}$ in agreement with (12). While their mobilities have similar values (within 10%) both theoretical curves are shifted from one another by the different values of the source resistance $R_{ds}$. 
Fig. 2. (a) Small-signal source-drain conductance ($g_{ds}$) as a function of the top gate voltage minus the threshold voltage ($V_{g0}$) and (b) the small-signal source-drain resistance ($R_{ds}$) as a function of the inverse of the top gate voltage minus the threshold voltage ($1/V_{g0}$) for $V_{gback} = -40$ V.

In Fig. 3a we display the $I$-$V$ characteristics of the GFET for $V_{gback} = -40$ V. An excellent agreement between experiment and theory (10) is obtained with $\mu_0 = 700$ cm$^2$/V·s, $R_s = 800$ $\Omega$, and $V_c = 0.45$ V for all gate biases, which provides the right current values for high (negative) $V_{ds}$. Our mobility value is 25% higher than Meric's fitted values ($\mu_0 = 550$ cm$^2$/V·s), while the source resistance is within 15% of the measured ones [3]. The up-kick in the drain current attributed to ambipolar transport for $V_{gpp} = 0$ V is simulated by a phenomenological current term proportional to $\left(\frac{V_{ds}}{V_{ds(sat)}} - 1\right)^2$ [11]. For comparison, we also plot the current with the parameter values ($\mu_0 = 600$ cm$^2$/V·s and $R_s = 500$ $\Omega$) that best fit the conductance characteristics in Fig. 2, and for which we use $V_c = 0.5$ V ($F_c = 5$ kV/cm) for all gate biases, which gives the right current values at $V_{ds} = -3$ V but overestimates the current at high (negative) gate and intermediate source-drain biases. The discrepancy between the two sets of fitting parameters are within the 15-25% range, which is not really excessive and may be due to the fact that in the case of the conductance fit, the experimental data are obtained for very low bias, whereas in the case of the $I$-$V$ fit, the mobility $\mu_0$ and source resistance $R_s$ values account for intermediate source-drain biases, which describe different transport processes (warm holes) with the onset of remote phonon scattering [8] at intermediate fields than low-bias transport only limited by impurity scattering [7]. Fig. 4b shows the carrier concentration (left axis) and electric potential (right axis) at the saturation onset ($V_{ds(sat)}$) as functions of position along the channel length with the source located at $x = 0$. One can observe that the channel never experiences pinch-off since the carrier concentration never reaches the minimum sheet carrier concentration given
Fig. 4. (a) Small-signal source-drain conductance \( (g_{ds}) \) as a function of the top gate voltage minus the threshold voltage \( (V_{g0}) \) and (b) the small-signal source-drain resistance \( (R_{ds}) \) as a function of the inverse of the top gate voltage minus the threshold voltage \( (1/V_{g0}) \) for \( V_{gback} = +40 \) V.

Therefore we believe the current up-kick at high source drain bias for \( V_{gtop} = 0 \) V may be due to other effects than electron injection from the drain side, such as impact ionization with carrier multiplication for instance [11].

B. \( V_{gback} = +40 \) V

In figs. 4, we show the comparison between theoretical and experimental results for both the p-channel conductance and resistances. In fig. 4a, the solid curve is obtained from (11) with the parameters \( (\mu_0 = 1200 \text{ cm}^2/\text{V}\cdot\text{s}; R_s = 1200 \Omega) \) given in [3], while the dashed curve uses \( \mu_0 = 400 \text{ cm}^2/\text{V}\cdot\text{s} \) and \( R_s = 1000 \Omega \) to fit the experimental data, which again display the linear relation predicted in (12) for the resistance as seen in fig. 4b. Here, the discrepancy between the two sets of values for \( p_0 = 0.5 \times 10^{12} \text{ cm}^2 \). Therefore we believe the current up-kick at high source drain bias for \( V_{gtop} = 0 \) V may be due to other effects than electron injection from the drain side, such as impact ionization with carrier multiplication for instance [11].

Fig. 5. (a) Drain current \( (I_d) \) as a function of drain-source voltage \( (V_{ds}) \) and (b) hole concentration (left axis) and electric potential (right axis) for \( V_{ds} = V_{drain} \) as functions of position along the channel length (source is on the left) for \( V_{gback} = +40 \) V; \( V_{gtop} = -0.8 \) V, -1.3 V, -1.8 V, -2.3 V and -2.8 V (from bottom to top).

The higher source resistance provides lower current than for the fitting parameters is more dramatic since it affects both the slope (mobility), and to a less extent the asymptotic value of the source resistance.
Fig. 6. Calculated drain-source voltage ($V_{ds(sat)}$) as a function of the top gate voltage ($V_{gtop}$) for two $V_{gback}$ biases. The bars are estimated values from the experimental data [3].

$V_{gback} = -40$ V, despite the higher mobility.

Fig. 5b shows the carrier concentration and electric potential at the saturation onset ($V_{ds} = V_{ds(sat)}$) as functions of position along the channel length for the different gate biases. From a general standpoint, carrier concentrations are lower than for the case with $V_{gback} = -40$ V, because of the lower threshold voltage ($V_0 = 0.64$ V instead of $V_0 = 2.36$ V). Again, it can be seen that the channel never experiences pinch-off since the carrier concentration never reaches the minimum sheet carrier concentration.

C. Transfer Characteristics

In fig. 6 we plot the drain-source saturation voltage as a function of gate bias (13) for the two GFET configurations. The vertical bars on the plot represent the approximate range of the saturation drain-source voltage obtained from the experimental plots [3]. One notices the excellent agreement between theory and experiment, especially for the $V_{gback} = -40$ V condition, whereas the discrepancy for the $V_{gback} = +40$ V configuration is due to the uncertainty in ascertaining the experimental values that fall out of the figure. One also notices the steeper variation of the saturation voltage in the latter case compared to the former case, which is reflected in the larger value of the critical fields to reproduce the experimental data.

In fig. 7 we plot the saturation current as a function of the top gate voltage (14). For the case $V_{gback} = -40$ V, the extraction of the experimental values of the saturation current is straightforward, except for high top gate biases for which the current has not saturated (fig. 3a), and shows an excellent agreement with our model. For the case $V_{gback} = +40$ V the bars are estimates of experimental values because the current does not saturate for all values of $V_{gtop}$ over the range of the source-drain voltage (fig. 5a). For both $V_{gback}$, it can be seen that the relationship between the saturation current and top gate voltage is linear, and an excellent agreement between theory and experiment is obtained with discrepancies occurring at low top gate biases.

We also display the profile of the transconductance at saturation as a function of the top gate voltage ($V_{gtop}$) for two $V_{gback}$ biases.

Fig. 7. Calculated saturation current ($I_{ds(sat)}$) as a function of the top gate voltage ($V_{gtop}$) for two $V_{gback}$ biases. Crosses (+) and bars (I) are estimated from the experimental data [3].

Fig. 8. Calculated transconductance at saturation ($g_{msat}$) as a function of the top gate voltage ($V_{gtop}$) for two $V_{gback}$ biases.
\( V_{\text{gb}} = -40 \text{ V} \) condition. This is due to the \( V_c \) term in (15) since the critical field, and consequently the critical voltage, is much larger when \( V_{\text{gb}} = +40 \text{ V} \).

V. DISCUSSION AND CONCLUSIONS

We provide a coherent model for the output and transfer characteristics of GFETs with two back-gate bias configurations, for which the source and drain contacts are either p- or n-type. For unipolar transport, closed form expressions are obtained for the current, low drain bias conductance, transconductance at saturation, saturation voltages, saturation currents and potential along the channel, which rely on three parameters i.e. low field carrier mobility, source-drain resistance and critical field for the high energy carrier scattering, to reproduce the experimental \( I-V \) characteristics for each back-gate condition. In particular we predict a linear dependence of the low-field resistance versus inverse gate voltage, which is quantitatively confirmed, while we point out a discrepancy between the parameter values used for the \( g_{ds}-V_{\text{gb}} \) plots and the \( I-V \) characteristics, especially for positive back gate voltage, which has not been resolved so far. However the predicted quasi-linear dependence between saturation voltage and gate voltage is well confirmed experimentally.

Let us emphasize that our model relies on only one \( F_c \) parameter to describe the current at high drain biases for all top gate biases, which according to the velocity field relation \( v(F) \) implies a single saturation velocity \( v_{\text{sat}} = 3.2 \times 10^6 \text{ cm/s} \) (1.8 \times 10^7 \text{ cm/s}) for \( V_{\text{gb}} = -40 \text{ V} (+40 \text{ V}) \), unlike Meric's model that requires a concentration dependent saturation velocity to fit the experimental data. In this respect, let us point out that close analysis of the source-drain field profile indicates that the maximum fields achieved in the highest drain biases are only a few times the critical field values \( F_c \), which is far from achieving saturation; it is therefore quite possible that the velocity-field relation acquires a lower slope due to remote phonon scattering rather than saturating [12].

Finally, we also point out that detailed analysis of the charge control model indicates that even for the lowest (negative) top gate bias i.e. \( V_{\text{gtop}} = 0 \text{ V} (-0.8 \text{ V}) \) for \( V_{\text{gb}} = -40 \text{ V} (+40 \text{ V}) \), the channel never reaches pinch-off, which suggests that the current increase at high drain biases may be due to other causes than electron injection [11].

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