Advanced Vertical Interconnect Technology Utilizing Sintered Conductive Paste-Vias for High Density Interconnects

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Abstract

Advanced vertical interconnect technology that combines traditional HDI structures feature micro-vias and conductive paste-vias was developed to fabricate multilayer PWB, owning excellent electrical performance, mechanical reliability and mass productivity at reasonable cost. This advanced multilayer PWB is constituted of high elastic modulus thermosetting dielectric composition (Glass epoxy (FR-4)) with interstitial via holes and/or Cu micro-vias, and sintered conductive paste-vias buried in low elastic modulus thermosetting dielectric composition. The latter composition properly act as mechanical buffering layer of vertical interconnection between upper and lower multilayer PWB.

The first in this paper, manufacturing process condition was discussed the optimum electrical performance at the interface of HDI Cu lands and conductive paste with interposing low elastic modulus dielectric material was achieved. Next, the micro structure and sintering condition at the interface of conductive paste and HDI Cu land was observed and analyzed by using SEM and EDX. In addition, mechanical reliabilities, estimated by applying structural analysis method, and signal transmission properties by way of this buried conductive paste, analyzed by frequency and time-domain simulation, were discussed. From these results, it was found that this advanced vertical interconnect technology with sintered conductive paste and low elastic dielectric shows sufficient mechanical reliability and electrical property for passing high-speed signal up to 15 Gbps.

Keywords: Laminates, Interconnections in Substrate, Sintered conductive paste-vias, Screen printing, Low transmission signal losses

1. Introduction

Vertical interconnect via connection of conventional ultra-multilayer printed wiring board (PWB) is generally composed of plated through holes (PTHs), interstitial via holes (IVHs) and laser Cu-vias. And back drilling process is applied to reduce the signal reflection due to stab branching from the PTHs wiring (Fig. 1 (a)). Manufacturing process, composed of various interconnects, such as PTHs, IVHs, laser Cu-vias and back-drilled PTHs is complicated and process term is very long.

This paper describes advanced vertical interconnect technology, which is actualized by introducing new laminating process to reduce the complicated multilayer fabrication process step. Each laminated-parting unit is segmented, according to the design methodology ensuring mechanical reliability of the Z-axis interconnection. For example, the number of segmented units is two in the case of 10 layers, and three or four in the case of 24 layers. Each unit is formed in a separated unit with difference process technologies, such as PTHs, IVHs and laser Cu-vias. Each

![Fig. 1 Interconnection of ultra-multilayer printed wiring board.](image-url)
unit is laminated and unified at the same time through a vacuum pressing process. In this process, interposing low elastic modulus dielectric materials with conductive paste is applied as bonding material (Fig. 1 (b)). By introduction of this advanced laminating process, it becomes possible to provide quasi-all Cu-via structure, which potentially provides excellent electrical performance without back drilling technology, and offers ultra-high layer counts PWBs with high mechanical reliability, high productivity and production yield at a low cost.

Figure 2 (a) shows ideal HDI structure with all Cu-via technology. This HDI structure cannot be attained by the conventional laser Cu-via process because thickness of PWB increases with lamination step in consequence, lithography equipment with shallow focus depth cannot share. Additionally, in this HDI with all Cu via production lead time is very long because process fabrication is executed sequentially.

Figure 2 (b) shows advanced HDI structures with conductive paste. In the case of PWB structure with all laser Cu filled via stack, internal stress in Cu-vias increases with increasing of Cu layer number.[1] In this literature, the authors indicated that internal stress of Cu-vias was reduced by placing elastic conductive paste between Cu stacked vias. Then we aimed the same stress release effect of sintered conductive paste with interposing low elastic modulus dielectric material.

Recently, for suppressing the DC voltage drop along the wiring at Z-axis interconnection, high electrical conductivity is required at the interconnection in ultra-multilayer PWB with the spread of high speed signal transmission driven by low voltage. With this background, three models are discussed in this paper, i.e. PTH with back drilled, HDI with all stacked Cu vias and advanced HDI structure on electrical simulations.

2. Fabrication Process of Advanced Vertical Interconnection

2.1 Materials of advanced vertical interconnection layer

Sintered conductive paste for advanced vertical interconnection consists of two major elements, metal particles for sintered part and thermosetting resin binder for stress relaxation its own. Sintering temperature of the metal alloy in sintered conductive paste is selected below 200°C, in consideration of heat resistance of the thermosetting binder resin. The metal particles consist of Bi, Ag, Sn, and Cu. Bi contained in metal-alloy decreases the alloying temperature.

Bonding sheet for adhesive layer is formed of thermosetting resin without reinforced glass-cloth and inorganic fillers. Therefore, it can ensure excellent homogeneous electrical characteristics of the resin itself.

2.2 Process of advanced vertical interconnection layer

We manufacture multilayer PWBs with following process.

First, sintering paste is printed on each PWB by screen printing method using metal mask to form cone shape bumps. Designed Cu land diameter is 150 μm, and paste bump diameter is selected 80 μm.[2–4]

Second, cone shaped conductive bumps are pre-cured. This pre-cure temperature is decided by the observation result of the sintering condition and resin cured condition.

Third, low elastic modulus dielectric material covers each printed bumps on bottom side multilayer PWB unit, and each top side PWB unit is aligned on X-ray layup equipment and fastened temporary.

Finally, all PWB units are laminated at once in vacuum press. In this time, PWBs are heated before pressing, in order to fluidize the dielectric resin and prevent resin from remaining between Cu lands and top of conductive paste bumps. Then, pressurization starting when temperature rises higher than 130°C, which is equivalent temperature...
to the lowest point of dielectric resin melt viscosity (Fig. 3). In this time, maximum pressure is approximately 3 MPa. We keep temperature at 130°C for 30 min, and raise to 180°C to cure dielectric resin.

2.3 Mechanism of conductive paste sintering

We consider sintering mechanism of conductive paste with every curing process.

At first, Bi, Ag, Sn, and Cu metal particles are distributed uniformly in thermosetting binder resin in conductive paste.

In the pre-curing process after screen printing, printed bumps are heated at 130–160°C. Such metal particles are sintered scarcely, since printed bumps are not pressed.

In the vacuum press process, we hold temperature at 130°C for 30 min at first to fluidize the dielectric resin, and then raise to 180°C to cure dielectric resin. First, Sn-Bi alloy is growing over the eutectic temperature 139°C, and other alloys are formed one after the other. Besides Sn-Cu alloy is formed especially between Cu lands and conductive paste bumps.

3. Experimental Procedure

3.1 Measurement of bump resistance

We manufactured PWBs including daisy chain connection as shown in Fig. 4. Then, we measured the daisy chain resistance, and then calculated bump resistance.

3.2 Bump cross-section analysis

We observed cross-section of pressed paste-vias to investigate and analyze the microstructure and sintering condition on the interface of conductive paste and Cu land on SEM and energy dispersive X-ray spectrometry (EDX).

3.3 Mechanical reliability analysis by finite element method

We evaluated the reliability of PWBs with the advanced vertical interconnect technology that we proposed in this paper (Fig. 2 (b)). Structures simulated by three-dimensional Finite Element Method (3D-FEM) are illustrated in Fig. 5 where (a) is ideal HDI, (b) is advanced HDI. Material physical properties of the models are listed in Table 1. Cu and Glass/epoxy were modeled with elastic-plastic and anisotropic linear elastic property, respectively. Other portions than Cu and glass/epoxy, were modeled as elastic.

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**Fig. 3** Illustration of vacuum press process.

**Fig. 4** Daisy chain connection for one bump resistance calculation.

**Fig. 5** FEM analysis models.

**Table 1** Dimension value of models.

| Materials                        | Dimension  |
|----------------------------------|------------|
| Glass/epoxy                      | (Thickness)|
| Adhesion insulator               | 70 μm      |
|                                  | 20 μm      |
| Cu Land                          | (Diameter)|
| Cu filled via                    | 150 μm     |
| Sintered conductive paste-vias   | top: 100 μm|
|                                  | bottom: 80 μm|
materials. From these models, Von Mises stress distributions in Cu-filled stacked vias were estimated under the condition after three temperature cycles of −40 to 125°C are applied.

In addition, Table 2 shows mechanical material consists applied in this paper.

### 3.4 Electrical simulations of various interconnect structures

In order to investigate electrical property of advanced HDI, we estimated the electric characteristic of highly stacked PWBs fabricated with 3 types of interconnect technologies on simulation. These PWBs were evaluated on both frequency and time-domain regions.

Interconnection structures evaluated in this simulation were as follows: (a) Ideal HDI, (b) advanced HDI, (c) back-drilled PTH via and (d) PTH via. All the structures simulated in this paper are illustrated in Fig. 6.

We evaluated electromagnetic property on 3D-FEM simulation around interconnection region. The simulation models were shown in Fig. 7 and we examined the electri-

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#### Table 2 Material Properties.

|                         | Unit          | Glass epoxy (FR-4) | Cu | Sintered conductive paste-vias | Adhesion Insulator |
|-------------------------|---------------|---------------------|----|--------------------------------|-------------------|
| Coefficient of thermal expansion | XY ppm/°C     | 13                  | 16.8 | 17.7                          | 38                |
|                         | Z ppm/°C      | 25                  |     |                                |                   |
| Young's Modulus         | XY GPa        | 26.5                | 110 | 58                            | 2.63              |
|                         | Z GPa         | 22.5                |     |                                |                   |
| Yield stress            | MPa           | –                   | 200 | –                             | –                 |
| Poison's ratio          | –             | 0.25                | 0.34 | 0.3                           | 0.35              |

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*Fig. 6 Interconnect structures evaluated in this study, (a) Ideal HDI, (b) Advanced HDI, (c) Back-drilled PTH and (d) PTH.*

*Fig. 7 FEM simulation setup for electromagnetic simulation, (a) Ideal HDI, (b) Advanced HDI, (c) Back-drilled PTH and (d) PTH.*
cal characteristic of interconnection itself. Transmission and reflection characteristics at interconnection were evaluated through S-parameter extracted by these simulations.[5–7]

In addition, 15 Gbps serial random-bits electrical property was also simulated in order to clarify the capability of advanced HDI for the practical high-speed digital applications. In this simulation, not only interconnection but also transmission lines were included in the simulation models. Transmission lines were driven by 50 \( \Omega \) ideal driver and terminated with 50 \( \Omega \) ideal resistor. Both driver and receiver were assembled on the surface (top layer), and connected with 50 \( \Omega \) matched Cu wiring arranged on the 5th layer through two interconnect vias (top-layer to 5th layer and 5th layer to top layer). The dimensions of simulation models applied in this simulation are illustrated in Fig. 6. Total length of transmission line in each model was about 40 mm.

4. Result and Discussion

4.1 Bump resistance and sintering condition of sintered conductive paste-vias

At producing PWB for measuring bump resistance, we evaluated pre-curing temperature, because pre-curing temperature was the most affective condition with sintering reaction. This conductive paste was including Bi. Although Sn-Bi eutectic temperature was 139°C, sintering condition was not unique around 139°C. We considered it was impossible to progress sintering reaction between top of Cu-land and conductive paste over 139°C pre-curing because of Sn-Bi eutectic reaction progress excessively before vacuum press process.

We selected pre-curing temperature of conductive paste bumps as 130°C lower than Sn-Bi eutectic temperature and 160°C higher than Sn-Bi eutectic temperature. Figure 8 shows bump resistance of test PWBs after vacuum press process. We acquired 18 m\( \Omega \) per bump in average under 130°C pre-curing and 11 m\( \Omega \) per bump under 160°C pre-curing. The latter bump resistance was lower to former. We considered it was necessary to add pressure and heat at vacuum press process to progress sintering.

Figure 9 shows cross section analysis data of sintering paste bump. Figure 9 (a) and (b) show the results with pre-cured under 160°C and vacuum pressed, respectively. In Fig. 9 (a), it was found that the conductive paste was not sintered under pre-curing temperature more than Sn-Bi eutectic temperature (139°C). It looked that Ag and Sn in conductive paste matrix did not sinter sufficiently, because Ag and Sn distributed granulously, i.e. these grains were not melted. Figure 9 (b) shows that sintering reaction promoted by heat and pressure in vacuum press. This photograph indicates Ag and Sn were melted each other, and were spread uniformly.

Figure 10 shows cross section analysis result on interface between Cu-land and conductive paste bump. Sn-Cu sintering compound distributed between Cu-land and conductive paste bump. These results indicate that Sn-Cu metal alloy was formed on the interface of conductive paste and Cu-land.

In Fig. 10 (a), resin residue was investigated at the upper interface between conductive paste and Cu-land scarcely. Lower interconnect resistance was obtained under 160°C pre-curing, the bump hardness was sufficient to reduce resin residue.
From these results, we consider interconnect mechanism between sintering conductive paste bump and Cu land is below.

a) This sintering paste sinters insufficiently by heating only it is necessary to add pressure and heat under vacuum press process.

b) The bump hardness is needed to reduce resin residue between Cu-lands and top of conductive paste bumps.

c) It is impossible to progress sintering reaction between top of Cu land and conductive paste under high temperature pre-curing because of Sn-Bi eutectic reaction progresses excessively and the resin in conductive paste is cured excessively before vacuum press process.

Therefore we needed to select best pre-curing condition in addition. Finally we succeeded acquiring 5 mΩ per bump in average with adapting 145°C for 60 min as pre-curing.

4.2 Result of mechanical simulation

Figure 11 shows stress contours after three cycles of thermal cycle test.

Von Mises stress of Cu-via under 125°C after three cycles of TCT was 216 MPa on ideal model and was 208 MPa on advanced model. Cu-via was deformed by tensile stress.

Maximum value of von Mises stress in advanced model was the same as in ideal model. Cu land on the bonding dielectric showed bended concave shape in advanced model. We checked the stress distribution on Cu-via/Cu land interface, and then found stress concentration was not very large. We considered adhesion insulator released stress concentration by bending Cu land. On the other hand, Cu land was not bended in ideal model. In this case the stress concentrated at contact point between Cu land and Cu-via. Thus, we expect bump crack progress is rapid at ideal model.

Therefore we suppose obtained mechanical reliability of Cu-via on conductive paste via at advanced model is superior or equal to ideal model.

4.3 Result of electrical simulation

Analysis results obtained from frequency-domain electromagnetic simulation using 3D-FEM field solver are shown in Fig. 12. These results clearly showed that advanced HDI owns excellent transmission characteristic, which was comparable with ideal HDI structure. Reflective coefficient was effectively suppressed by back-drilling procedure, but its characteristic was inferior to that of ideal and advanced HDI structure.

Figure 13 shows the result of random-bit simulations. The advanced HDI showed widely opened eye diagram,
i.e. it showed excellent performance similar to ideal HDI.
In detail, advanced HDI showed largish attenuation comparing with conventional HDI but the attenuation in advanced HDI was enormously smaller than that of back-drilled TH. Considering with these results, cost-effectiveness and process yields, advanced HDI is thought to be realistic and ideal interconnect technology.

5. Conclusion
We develop advanced vertical interconnection technology with HDI and conductive paste vias. This advanced PWB technology brings in enough mechanical reliability and electrical performance similar to ideal all Cu-filled-vias in measured bump resistance, and mechanical and electrical simulations. By introduction of this advanced technology, it excludes plating through holes (PTH) with back drilling technology in the conventional ultra-multilayer PWB, and offers higher mass productivity with reasonable cost. Besides this advanced HDI technology owns technical potential to apply coreless PWB laminate units, which can become mainstream of the future HDI products.

References
[1] A. Happoya, A. Tanaka, K. Hirohata, and S. Okayama, “Development of All Layer Stuck Vias Printed Circuit Boards Providing Excelled Mechanical Reliability,” Electronics, Information and Correspondence Congress Paper 2009, pp. 703–711.
[2] S. Sagara, I. Miyatani, T. Tsunoda, and S. Amakai, “Development of Thin LSI Embedded Circuit Boards,” 41st International Symposium on Microelectronics (IMAPS) 2008, pp. 52–59.
[3] S. Sagara and M. Tanaka, “The Electrical Characteristics Investigation of the Module-Level Miniaturization with Embedded Device Technology,” Transactions of The Japan Institute of Electronics Packaging, Vol. 2,
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