A Comprehensive Analysis of Different SRAM Cell Topologies in 7-nm FinFET Technology

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Abstract
Complementary metal-oxide-semiconductor (CMOS) device faces various unknown short channel effects (SCEs) such as subthreshold leakage and drain-induced barrier lowering (DIBL) in advanced technologies. This degrades the circuit’s performance, especially SRAM cell, owing to the high demand for large density. Fin-shaped field-effect transistor (FinFET) is one of the trending choices for memory designers, which can improve the stability and minimize the SCEs of the CMOS devices. In this study, different SRAM cell topologies are redesigned and re-simulated by using 7-nm FinFET devices, and then, their performance metrics including the stability, access time, and power are measured at a certain range of supply voltage (VDD) below the nominal value of 0.7 V. Moreover, the layout of these SRAM cells is designed and compared in which the ST12T cell consumes the maximum area due to having a higher count of transistors. Simulated results inferred that the ST11T cell offers the highest RSNM among all the SRAM cells, which can be explained with the use of read decoupling technique and cross-coupled Schmitt-trigger inverters. Moreover, the ST12T cell has the highest WSNM in comparison to other SRAM cells because this cell performs its write operation in fully differential form along with a power-gating write-assist technique. In the view of power consumption, the ST11T and ST12T cell offers the least dynamic and leakage power dissipation, respectively, because the former cell is single-ended bitcell with a low frequency and the latter one has stacked transistors in its cell core in which the path from power VDD to GND is long. An electrical quality metric (EQM) is utilized to assess the overall performance of these SRAM cells, which displays the superiority of the ST12T cell.

Keywords SRAM · Stability · CMOS · Power · FinFET

1 Introduction

Shrinking of the device size leads to a dramatic rise in the demand for handheld devices. These hand devices require random access memory (RAM) as one of the major components. The portable battery-operated systems have the foremost need the efficient designs, which should be stable, power, and area-efficient. Static RAM (SRAM) is one of the best choices for them and complementary metal-oxide-semiconductor (CMOS) is considered as the best choice for SRAM but due to its aggressive scaling, the device performance has degraded due to short channel effects (SCEs).

Scaling imposed physical limitations on CMOS: As scaling is done, it is important to maintain the electric field, the thickness of the gate oxide needs to be reduced which gives rise to the leakage current exponentially as the gate oxide thickness is reduced. The rising tunneling current may affect devices adversely. The smaller channel length is supposed to have faster-switching operations but at the same time it has adverse effects: it rises the OFF-current (I_{off}) which results in punch through and drain-induced barrier lowering (DIBL) [14]. The other factors which are affected by the scaling are the supply voltage and the threshold voltage, though the scaling of the supply voltage leads to a drastic reduction in dynamic power, it lead to degradation of the noise margin. Due to supply voltage scaling the threshold voltage requires to be scaled which results in the operation of the transistor in weak inversion, giving rises to subthreshold leakage current. To minimize short channel effects, an increase in channel doping is required, this raises other effects like the band to band tunneling (BTBT) and slow carrier mobility [9]. For reduction in power consumption, scaling or reducing the supply voltage is one of the utmost accepted solutions, but it leads to degraded stability in
terms of read margin which results in read failure. Also, scaling of supply voltage leads to threshold voltage variations which are further responsible for increasing the leakage current improve the performance, one of them is to move from a single port to multiport SRAM cells. Since the basic 6 T SRAM Cell was the single port cell that suffers from read failure due to scaling of the CMOS. Suggestions to improve the performance were given in the sizing of the transistors ratios which also failed due to aggressive scaling and low supply voltage. In due course of time researchers started thinking for an alternative of a CMOS device that should be nano in size and can combat the process variations. Researchers classified the nanodevices in three categories: (1) “Electric Dependent Nanodevices: These nanodevices may be having either ballistic, tunneling, or electrostatic mechanism. In ballistic transport, the electrons move with no resistivity in the material. As a result of a quantum-mechanical process, electrons flow through a potential energy barrier in tunneling. In electrostatic, the electric field plays an important role as the electrons move in the electric field only. Some of them area carbon nanotube field-effect transistors (CNTFETs), fin-shaped field effect transistors (FinFETs), nanowire field effect transistors (NWFETs), tunnel field effect transistors (TFETs) [13, 24]. (2) Magnetic Dependent Nanodevices: The mode of “Magnetostatic” and “spin transport” comes under this category. Magnetic quantum-dot cellular automata (MQCA) and spin field-effect transistors (spinFETs) are few examples [13, 24]. (3) “Mechanical-Dependent Nanodevices” used conductive polymers. The polymer structure varies when they are activated by the inputs [13], these sorts of devices are being used in field programmable gate arrays (FPGAs) and molecular memory [7] (Cotofana).

All the devices mentioned above possess some advantages over the CMOS. SRAM is more sensitive to the process variations in the physical structure, variation of the threshold voltage because of the dopant fluctuation. So, designing an SRAM that is least affected by these variations is a big challenge in CMOS designs. One of the most favored alternatives found for CMOS was FinFET as it consists of all the features of the CMOS along with the potential to combat the SCEs. The FinFET is preferred as it exhibits excellent gate control, has low switching times, and high current density compared to the CMOS devices. CMOS is a planar device where the gate control is only in one direction while in FinFET the gate is wrapped all around the gate which provides excellent gate control in all directions. The body of the FinFET is very thin due to which the gate capacitance lies close to the channel which helps in controlling the leakage. The device drive current of the FinFET is increased by forming parallel multiple fins connected, so the channel length is not the only parameter for the driving current. Besides, FinFET has the potential to increase carrier mobility using strain technology. It also has a low \( I_{\text{off}} \) current which further helps in reducing the leakage. Therefore, study and evaluation of FinFET performance, as a prominent replacement for CMOS, in digital circuits including SRAM cells is necessary. This paper comprehensively compares different SRAM cell topologies that include the conventional 6 T, conventional 8 T, Schmitt-Trigger-based 10 T (known as ST2), PMOS-PMOS-NMOS-based cell core 10 T (PPN10T), single-ended feedback-cutting 11 T (FC11T), Schmitt-Trigger-based 11 T (ST11T), and Schmitt-Trigger-based 12 T (ST12T) in terms of stabilities, delays, dynamic/leakage power consumption, area, and quality metric. The considered SRAM cells have been redesigned using 7-nm FinFET technology. The attained characteristics of different SRAM cell topologies are summarized as:

1. The ST11T and ST12T have the similar highest HSNM as they use two cross-coupled ST-based inverters pair.
2. The ST11T SRAM cell employing the read decoupling technique and strong cell core offers the highest RSNM.
3. The highest WSNM is related to the ST12T SRAM cell because of the differential writing structure along with utilizing the power-gating write-assist technique.
4. Two conventional 6 T and 8 T SRAM cells show the same lowest write delay due to their simple differential writing structure formed by only one access NMOS pass-gate transistor.
5. The conventional 6 T SRAM cell has the lowest read delay attributed to its differential reading structure including a strong pull-down transistor.
6. The ST11T SRAM cell dissipates the least dynamic power as it has a single-ended structure and relatively low speed.
7. The least leakage power dissipation is related to the ST12T SRAM cell due to the presence of a stacked transistor in its cell core.
8. The conventional 6 T SRAM cell occupies the minimum area among all the considered SRAM cells.
9. The ST12T SRAM cell has the highest electrical quality metric, as a complete metric to estimate the total performance of an SRAM cell.

The rest of this paper is as follows. Section 2 reviews in detail the different SRAM cell topologies considered for comparison in this study, simulation results and analysis are given in section 3. The conclusion of this article is discussed in section 4.

2 Literature Review

The conventional 6 T SRAM cell shown in Fig. 1a) has a simple and compact structure consisting of two cross-coupled inverters pair to form its cell core and two n-type MOS (NMOS) access pass gate transistors to connect two-
Fig. 1 Schematic of the different SRAM cells. a 6T, b 8T, c ST2, d PPN10T, e FC11T, f ST11T, and g ST12T
bit lines (BL and BLB) to the cell. The conventional 6 T SRAM cell uses the same path for performing its read and writes operations, therefore, suffering extremely from conflicting read/write necessities. The conventional 6 T SRAM cell shows poor read static noise margin (RSNM)/write static noise margin (WSNM), as a measure of read stability/writability, in severe low-supply voltage [12]. For the common 6 T SRAM cell, RSNM and WSNM are two conflicting design metrics. Therefore, it is intensely difficult to utilize the 6 T SRAM cell in severe low-supply voltage, especially below the transistor’s threshold voltage.

In [6], a basic 8 T SRAM cell (see Fig. 1b) is proposed to remove the read disturbance in the 6 T SRAM cell. The 8 T SRAM cell uses two NMOS access transistors extra, one read word line, and one read bit line compared to the conventional 6 T SRAM cell to form the isolated read path. During the read operation, data storing nodes are fully decoupled from the read bit line to enhance RSNM. However, this cell suffers from the leakage introduced by the isolated read path, which is further significant with technology scaling. A drastic improvement has been observed with a slight area overhead of 30%.

In [17], to solve the read stability issues, the basic principle of the Schmitt-Trigger (ST) has been used. In this work, the authors proposed two types of ST-based SRAM cells for improving cell stability. The feedback mechanism is used in the ST1 SRAM cell, but the limitation in the ST1 bit cell, is that the feedback is useful till voltage on the storing nodes is maintained, once the voltages start discharging or charging this feedback mechanism is no more effective. The feedback mechanism is useful if the storage node voltages are maintained. To remove this limitation, the ST2 SRAM cell is projected, displayed in Fig. 1c). A separate control signal is used for the improvement in the feedback mechanism. This differential sensing mechanism has been used with two separate word lines (WL and WWL) along with two different bit lines (BL and BLB). This bit cell is effective for low voltage operations, but it has area overhead while the other read/write assist techniques to have a lower area overhead.

A PMOS-PMOS-NMOS-based cell core 10 T (PPN10T) SRAM cell is projected in [22] and shown in Fig. 1d. This cell employs differential writing and single-ended reading structures for its write and read operation, respectively. This cell can improve RSNM/WSNM by using an isolated read path/differential writing path. The leakage power dissipation is reduced by this cell due to the presence of a stacked transistor in its cell core. However, it consumes high dynamic write power attributed to its dual-ended write bit lines.

In [8], a feedback-cutting 11 T FinFET SRAM (namely FC11T) is proposed and shown in Fig. 1e, which is a single-ended robust cell. The FC11T SRAM cell has a single bit line to perform read and write operations, therefore, resulting in dynamic power reduction. This cell can improve both RSNM and WSNM by employing isolated read path and feedback-cutting write-assist technique, respectively. However, these improvements are at the cost of lower reading and writing speed. This cell is found robust for the near subthreshold operation.

Another ST-based SRAM cell employing 11 transistors (ST11T) is proposed in [2] (see Fig. 1f) to improve both RSNM and WSNM and to reduce power consumption. Improvements in the RSNM, WSNM, and power consumption are because of the read decoupling technique, virtual grounded write-assist technique, and single-ended structure, respectively. However, this cell employs the same isolated read path as the conventional 8 T SRAM cell, which shows higher leakage in this path. The layout has been designed at 45 nm technology rules showing an increase of 2X times area in comparison to 6 T SRAM cell.

An 11 T SRAM using FinFET has been proposed in [5], at 16 nm and 20 nm FinFET technology. The proposed cell is designed for subthreshold and super threshold voltages. The proposed cell is suitable for low voltages without degradation in the performance of the memory cell especially the delay and the power. Here, a new SRAM using a header transistor scheme with the LP mode of FinFET has been proposed.

An ST-based 12 T (ST12T) SRAM cell is discussed in [23] (see Fig. 1g), which employs single-ended reading and differential writing structures. This cell still suffers from read disturbance but shows high WSNM, since it uses the power gating write-assist technique. This cell can improve the dynamic read power consumption with the aid of a single-ended reading operation. However, this cell suffers from the area overhead.

3 Simulation Results and Discussions

Different SRAM cell topologies including the conventional 6 T, conventional 8 T [6], Schmitt-Trigger-based 10 T (ST2) [17], PMOS-PMOS-NMOS-based cell core 10 T (PPN10T) [22], single-ended feedback-cutting 11 T (FC11T) [8], Schmitt-Trigger-based 11 T (ST11T) [2], and Schmitt-Trigger-based 12 T (ST12T) [23], as shown in Fig. 1, is investigated in this section. Table 1 compares the cell features of the SRAM cells. These SRAM cells are redesigned using FinFET devices and comprehensively compared in terms of major design metrics like stability factors and delay during the working modes, dynamic power, leakage power, and quality metric. For this reason, various HSPICE simulations at 7-nm predictive technology model multi-gate (PTM–MG) technology (P. T. M. (PTM)). A [19]) has been done at LEVEL = 72, 25 °C temperature, and a certain range of supply voltage (VDD) below the nominal value of 0.7 V, which is from 0.2 to 0.5 V by a linear variation of 0.1 V. The effective width (W) of a FinFET is given in Eq. (1) as follows [18]:

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in which \( H_{\text{fin}} \) is the fin height and \( T_{\text{fin}} \) is the fin thickness.

Transistor sizing plays a vital role in an SRAM cell design, which highly affects the RSNM and WSNM of that cell. This issue becomes significant in the 6 T SRAM cell because of conflicting read/write requirements \[12\]. Therefore, in all the considered SRAM cells, an \( N = 2 \) and an \( N = 1 \) have been chosen for pull-down transistors and other remaining transistors, respectively \[4\]. A comparative analysis of different performance metrics is discussed in the following subsections.

### 3.1 Stability Analysis

The stability is normally estimated as the static noise margin (SNM). The noise margin is characterized by plotting the overlapped voltage transfer characteristics (VTCs) (known as butterfly curves) for the cross-coupled inverters that make the latch of memory cells \[22\]. The length of the biggest square which can be inscribed inside the smaller eye of the butterfly curve provides the noise margin \[11\]. Table 2 gives the SNM of the various SRAM cells in the hold, read, and write modes at \( V_{\text{DD}} = 0.2 \text{ V} \). The ST11T and ST12T show an improvement in HSNM of 1.2x over 6 T and 8 T and 1.26x over PPN10T. The ST11T shows a drastic improvement in RSNM of 2.4x over 6 T SRAM and 1.7x improvement over ST2. For WSNM ST12T has 1.52x improvement over 6 T, 2.39x for 8 T, 1.67x over PPN10T, and 1.32x over FC11T.

#### 3.1.1 Hold Stability

Hold stability of an SRAM cell is gauged by the hold static noise margin (HSNM) and defined as the maximum DC noise voltage that the SRAM cell can stand without altering the data in the hold mode \[15\]. HSNM is the side length of the maximum square that can fit in the smaller wing of the butterfly curve during the hold mode \[10\]. Figure 2 displays the hold butterfly curves of the considered SRAM cells in this study at \( V_{\text{DD}} = 0.2 \text{ V} \). Moreover, Fig. 3 exhibits the HSNM variations of all the tested SRAM cells against linear variations in the \( V_{\text{DD}} \). It is observed from Fig. 3 that the HSNM value increases with the \( V_{\text{DD}} \) increment. SRAM cells including the conventional 6 T, conventional 8 T, and FC11T employ conventional cell core formed by cross-coupled normal inverters pair, and therefore show the same and lower HSNM compared to ST2, ST11T, and ST12T SRAM cells. Although, the PPN10 SRAM cell also uses a conventional cell core, however, it offers the lowest HSNM among all the studied SRAM cells as it has a stacked pull-up structure. The ST2 SRAM cell employing modified Schmitt-Trigger inverter-based cell core uses a stacked pull-down structure and thus, it has the second-best HSNM. Due to the use of a strong cell core consisting of two Schmitt-Trigger inverters, the ST11T and ST12T SRAM cells has equal and highest HSNM compared to all the SRAM cells at all supply voltages.

#### 3.1.2 Read Stability

The read stability of an SRAM cell is estimated by the read static noise margin (RSNM). The maximum DC noise voltage

### Table 1 Feature comparison of various studied SRAM cells

| Cell Feature       | 6 T  | 8 T  | ST2  | PPN10T | FC11T | ST11T | ST12T |
|--------------------|------|------|------|--------|-------|-------|-------|
| Transistor Count   | 6    | 8    | 10   | 10     | 11    | 11    | 12    |
| Read/Write Bitlines| Diff/Diff | SE/SE | Diff/Diff | Diff/Diff | SE/SE | SE/SE | SE/Diff |
|                   | BL-BLB | BL-BLB-RBL | BL-BLB | WLB-WLBL-RBL | BL | BL-RBL | BL-BLB |
| Control signals    | (1)   | (2)   | (2)   | (2)     | (3)   | (2)   | (3)   |
|                   | WL    | WL-WL | WL-WL | WL-WL   | WL-WL-VGND | WL-WL-VGND | WL-WL-RWL |
| Read-disturb-free  | No    | Yes   | No    | Yes     | Yes   | Yes   | No    |
| Half-select-free   | No    | No    | No    | No      | No    | Yes   | Yes   |

### Table 2 A static noise margin of the various SRAM cells during the hold, read, and write operations at \( V_{\text{DD}} = 0.2 \text{ V} \)

| Static noise margin | 6 T | 8 T | ST2 | PPN10T | FC11T | ST11T | ST12T |
|---------------------|-----|-----|-----|--------|-------|-------|-------|
| HSNM (mV)           | 67.1| 67.1| 73.5| 62.4   | 67.1  | 79.2  | 79.2  |
| RSNM (mV)           | 32.8| 67.1| 46.3| 62.4   | 67.1  | 79.2  | 44.1  |
| WSNM (mV)           | 73.4| 46.9| 89  | 67     | 84.5  | 74    | 112.3 |
which an SRAM cell can sustain without changing the data during the read mode is defined as Read Stability [15]. The RSNM is considered as the length of a side of the largest square which is embedded inside the smaller eye of the butterfly curve during the read mode [10]. Figures 4 and 5 show the read butterfly curves at $V_{DD} = 0.2$ V and the RSNM variations versus $V_{DD}$ variations, respectively. The conventional 6 T, ST2, and ST12T SRAM cells suffer from the read disturbance issue, resulting in RSNM degradation. These SRAM cells show the lowest RSNM in comparison to other considered SRAM cells at all $V_{DD}$ values. However, the ST2 and ST12T SRAM cells show considerably higher RSNM in comparison to conventional 6 T SRAM cell due to their Schmitt-Trigger-based inverters. Other remaining SRAM cells such as the conventional 8 T, PPN10T, FC11T, and ST11T employ the read decoupling technique in which data storing nodes are fully isolated from the bitlines during the read operation, results in the same values for RSNM & HSNM. The ST11T SRAM cell displays the maximum RSNM amongst all the SRAM cells due to its strong cell core formed by cross-coupled Schmitt-Trigger-based inverters pair.

### 3.1.3 Writability

Writability of an SRAM cell is determined by the write static noise margin (WSNM), which is the capability of that SRAM cell to pull down/up a ‘1’/‘0’ storage node to a voltage lower/higher than the switching threshold ($V_{th}$) of another inverter ‘0’/‘1’ storing node; consequently, the state of the cell is successfully flipped [11]. To calculate the WSNM of an SRAM cell, first, the read VTC of that SRAM cell is combined with its write VTC, and then, the length side of the smallest square that can be inserted between and lower half of these VTCs gives the WSNM of the corresponding SRAM cell [1]. Figure 6 shows the combined read and write VTCs of the studied SRAM cells at $V_{DD} = 0.2$ V. Furthermore, the WSNM variations of the SRAM cells versus $V_{DD}$ variations
are given in Fig. 7. As V_{DD} increases, the WSNM values also increase. SRAM cells such as FC11T, ST11T, and ST12T use feedback-cutting, power-gating, and floating virtual ground write-assist techniques, respectively, to improve the WSNM. The conventional 8 T and PPN10T SRAM cells show lower WSNM to the 6 T SRAM cell due to their read VTC. In the ST2 SRAM cell, read access transistors also help to write a '0' or '1' into the cell, resulting in WSNM improvement. It is obvious from Fig. 6 that the ST12T cell offers the highest WSNM among all the studied SRAM cells due to the use of a fully differential writing structure along with a power-gating write-assist technique. Moreover, the read VTC also stretches the smallest square to further increase the WSNM.

### 3.2 Access Time or Delay

Access time or delay average of the low-to-high propagation delay (t_{PLH}) and the high-to-low propagation delay (t_{PHL}). These are two kinds of read and write access time [22].

![Fig. 6 WSNM of the various SRAM cells at V_{DD} = 0.2 V](image)

Table 3 reports the read and write access times of the considered SRAM cells in this study. ST11T shows a reduction in read delay by 1.54x from ST2 and 1.35x from FC11T SRAM. ST12T SRAM shows a reduction in read delay by 1.33x from ST2 SRAM. The write delay of ST11T reduces by 1.42x from FC11T while the write delay of ST12T reduces 3.2x times with FC11T SRAM.

#### 3.2.1 Read Access Time or Read Delay

The reading speed of an SRAM cell is gauged by the read delay or access time (T_{RA}). It is defined as the time between the word line activation when the bit line voltage is discharged by 50 mV from the original high value [3, 12]. Figure 8 shows the comparisons of the T_{RA} of the various SRAM cell at different V_{DD} values. From this figure, the 6 T SRAM cell demonstrates the lowest T_{RA} due to its reading path, which includes the strong pull-down transistor with an N = 2. Various SRAM cells like the conventional 8 T, PPN10T, and ST11T employ the same isolated read path made by two access transistors. Therefore, these SRAM cells show higher T_{RA} in comparison to 6 T SRAM cell. In the ST12T SRAM cell, the read path is created by three series-connected access transistors; consequently, this SRAM cell offers higher T_{RA} as compared to the above-mentioned SRAM cells. Because of higher overall bit lines capacitance as a direct consequence of the connection of several access transistors to the same bit lines, the ST2 SRAM cell shows the highest T_{RA} among all the SRAM cells at all V_{DD} values.

#### 3.2.2 Write Access Time or Write Delay

The swiftness of an SRAM cell during the write operation is measured by write access time or write delay (T_{WA}). The T_{WA} is well-defined as the time duration between the word line activation and the time when the storage node Q (QB) reaches 10% (90%) of V_{DD}. The T_{WA} for writing ‘1’ into ‘0’ storing node Q in all the SRAM cells against V_{DD} variations is shown in Fig. 9. The conventional 6 T and 8 T SRAM cells have the same simple differential writing structure formed by a single access transistor. Therefore, these SRAM cells show the same lowest T_{WA} compared to all the SRAM cells. The FC11T and ST12T SRAM cells show the highest T_{WA} among all the compared SRAM cells due to their single-ended writing operation. However, the FC11T SRAM cell offers higher TWA than the ST11T SRAM cell because in the former cell the utilized feedback-cutting write-assist technique changes the cell core to be as two cascaded inverters during the write operation in which one inverter is followed by another one, resulting in T_{WA} increment. In the ST12T SRAM cell, the switching threshold (V_{th}) of Schmitt-Trigger inverters in the cell core is higher than the normal one. This issue increases the T_{WA}. The SRAM cells including ST2 and PPN10T SRAM
cells show almost equally lower TWA than the conventional 6 T SRAM cell.

### 3.3 Dynamic/Leakage Power Consumption

Dynamic/Leakage power consumption of an SRAM cell is the power consumption of the cell when it is accessed in idle mode. Table 4 reports the power consumption of numerous SRAM cells at VDD = 0.2 V. ST11T shows a reduction in dynamic power by 3.69x, 3.98x, 5.93x, 3x, and 2.32x over 6 T, 8 T, ST2, PPN10T, and FC11T respectively. ST12T shows a drastic reduction of 4.834x, 5.37x, 3.74x, 4.58x, and 1.56x over 6 T, 8 T, ST2, PPN10T, and FC11T respectively.

#### 3.3.1 Dynamic Power Consumption

Dynamic power ($P_{Dynamic}$) is the notable portion of the overall power consumed by an SRAM cell. Since the write power is dynamic power, hence dynamic power expression is used for the calculation of write power. The write power of an SRAM cell is thus given by Eq. (3):

$$P_{Dynamic} = \alpha_{write} \times C_{BL} \times V_{DD}^2 \times f_{write}$$  \hfill (3)

where $\alpha_{write}$ is the switching activity factor, $f_{write}$ is defined as writing frequency. The maximum value for write activity factor is considered as 1 [20]. The simulation results of write power are shown graphically in Fig. 10. SRAM cells such as the conventional 6 T, 8 T, ST2, PPN10T, and ST12T employ fully differential writing structure, and therefore their $P_{Dynamic}$ is higher than other SRAM cells with single-ended writing structure. The ST2 SRAM cell consumes the highest $P_{Dynamic}$ among all the SRAM cells due to its higher overall bit line capacitances because of the connection of several access transistors to the same bit lines. Although, the FC11T SRAM cell uses a single-bit line for performing both read and write operations, however, its bit line needs to be discharged to the ground for every write operation, and therefore, its $\alpha_{write}$ is equal to 1 and consumes higher $P_{Dynamic}$. The PPN10T and ST12T SRAM cells show lower $P_{Dynamic}$ than the conventional 6 T SRAM cell due to their lower $f_{write}$. As shown in Fig. 10 and Table 4, the ST11T SRAM cell offers the least $P_{Dynamic}$ in comparison to all the considered SRAM cells in this study. This improvement is due to the fact that the ST11T design is single ended bitcell in nature, which reduces $\alpha_{write}$ to less than half, consequently, the $P_{Dynamic}$ is reduced. The ST11T cell, on the other hand, has a slow write operation (low $f_{write}$). This issue, in turn, minimizes the $P_{Dynamic}$ according to Eq. (3).

#### 3.3.2 Leakage Power Dissipation

The leakage power ($P_{Leakage}$) is the power strained by MOS devices from VDD when the cell lies in standby mode. As an SRAM cell stays the maximum of the time in hold mode, therefore the $P_{Leak}$ is an important factor in total power consumption [12]. Figure 11 compares the $P_{Leakage}$ of the various
SRAM cells at different $V_{DD}$ values. The conventional 8 T SRAM cell displays a higher $P_{\text{Leakage}}$ than the conventional 6 T SRAM cell due to its higher count of bit lines used. Furthermore, this SRAM cell has high leakage in its isolated read path, which becomes significant with technology scaling [3]. The ST2 and PPN10T SRAM cells dissipate lower $P_{\text{Leakage}}$ than the conventional 6 T SRAM cell as stacked transistors are used in their cell core. Although, the ST11T is single-ended and uses stacked transistors, however, this memory cell employs the isolated read path as the 8 T SRAM cell, and therefore, suffers from isolated read path’s leakage. This SRAM cell displays higher $P_{\text{Leakage}}$ in comparison to FC11T and ST12T SRAM cells. The least leakage power dissipation is related to the ST11T cell according to Fig. 11 and Table 4. This is inferred that the ST12T cell uses stacked transistors in its cell core. Moreover, the employment of power gating NMOS and PMOS transistors in the left inverter, to facilitate writing data into the cell, longs the direct path from power $V_{DD}$ to ground. This further reduces the $P_{\text{leakage}}$.

### 3.4 Layout Area

The layouts of the considered SRAM cells in this study, created on the design rules for the FinFET technology given in [21], are demonstrated in Fig. 12. The area for each cell is described in Table 5, where $\lambda$ is the minimum feature size which is considered 1/2 of the gate length [4]. The conventional 6 T SRAM cell displays the minimum layout area because of its simple structure with a minimum count of transistors used among all the considered SRAM cells in this study, the ST12T SRAM cell, on the other hand, consumes the highest layout area, which is attributed to its higher count of transistors utilized in this design.

### 3.5 Electrical Quality Metric

For comprehensive evaluation of the performance of an SRAM cell, an electrical quality metric (EQM) has been proposed in [16] and expressed as Eq. (4) to assess the overall excellence of a cell.

$$\text{EQM} = \frac{HSNM \times RSNM \times WSNM}{T_{RA} \times T_{WA} \times P_{\text{Dynamic}} \times P_{\text{Leakage}} \times \text{Area}} \quad (4)$$

Where, HSNM, RSNM, and WSNM are the static noise margin during the hold, read, and write operations, respectively. $T_{RA}$

| SRAM cells | Height ($\lambda$) | Length ($\lambda$) | Area ($\lambda^2$) | Normalized area |
|------------|-------------------|-------------------|-------------------|-----------------|
| 6 T        | 24                | 39                | 936               | 1×              |
| 8 T        | 24                | 48                | 1152              | 1.23×           |
| ST2        | 24                | 72                | 1728              | 1.84×           |
| PPN10T     | 24                | 61                | 1464              | 1.56×           |
| FC11T      | 34                | 55                | 1870              | 1.99×           |
| ST11T      | 24                | 71                | 1704              | 1.82×           |
| ST12T      | 34                | 60                | 2040              | 2.17×           |
(T_{WA}) is the read (write) access time. P_{Dynamic} is the dynamic write power consumption, P_{Leakage} is the leakage power dissipation, and Area is the layout area. It is observed from Fig. 13, which shows the EQM of all cells at V_{DD} = 0.2 V, that the ST12T/ST2 SRAM cell offers the highest/lowest EQM amid all the considered SRAM cells. It is clear from Eq. (4) that all the performance metrics affect the EQM value. Though the ST12T cell experiences the read-disturbance issue, however, other high SNMs such as HSNM and WSNM compensate for the low RSNM. Therefore, its EQM is the best.

4 Conclusion

A thorough analysis of diverse SRAM cell topologies redesigned using 7-nm FinFET technology is presented...
in this article. The various performance metrics of these SRAM cells such as stabilities, delays, dynamic power, and leakage power have been measured at a certain range of supply voltage from 0.2 V to 0.5 V with a linear variation of 0.1 V and a room temperature of 25 °C. Based on the obtained results, the ST11T SRAM cell offers the highest RSNM and the least dynamic power among all the considered SRAM cell. Furthermore, the ST12T SRAM cell shows the highest WSNM, and the least leakage power compared to other SRAM cells. This cell, on the other hand, occupies the highest area. In terms of speed performance, the conventional 6 T SRAM cell has the best read and write access times due to its simple fully differential structure. To assess the overall performance of these SRAM cells, an electrical quality metric has been utilized, which displays the superiority of the ST12T SRAM cell among all the SRAM given cells in this article.

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Author’s Contributions NA Additional declarations.

Availability of Data and Material (Data Transparency) The associated data will be made available on request.

Code Availability (Software Application or Custom Code) The simulation work has been carried out using HSPICE software.

Declarations

Conflicts of Interest/Competing Interests There is no conflict of interest at any stage.

Ethics Approval NA It is a simulation-based design and analysis. So, it does not produce any environmental hazards.

Consent to Participate Yes, we are ready to participate.

Consent for Publication We are ready for publication with your journal.

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