Circuit Design Method to Improve Cryogenic Buffer Amplifiers Dynamic Parameters on CJFETs

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Abstract. We consider a circuit design method to increase a slew rate increase and transient process setting time decrease in buffer amplifiers (BAs), intended for operation in analog interfaces of physical values sensors and automatic devices at low temperatures. Differentiating transient correction circuits are introduced into the classical circuits of the BAs on complementary field-effect transistors (CJFETs) to improve these dynamic parameters. We investigated two buffer amplifier’s topologies: single-ended and balanced ones. The article shows the practical use of the proposed BA in the output and input stages of the high-speed operational amplifiers.

1. Introduction
Create a cryogenic electronics as analog IP-module that processes signals from the sensors at low-temperatures, is one of the urgent problems of specialized hardware implementation of the automatic control systems for medicine and space instrument. This class of the electronic component base is implemented based on junction gate field-effect (JFET) and complementary metal-oxide-semiconductor (CMOS) transistors [1-3].

A significant problem in the operation of classical buffer amplifiers (BAs) of modern analog interfaces and microcircuits based on complementary field effect transistors (CJFETs) [4,5] is that they have low speed in the mode of a large pulse signal. It is related with small parasitic capacitors $C_1=1-2 \text{ pF}$ [4,5] in output JFETs gates circuits and their non-linear operational modes [6]. This disadvantage is associated with the presence of small parasitic capacitors $C_1=1-2 \text{ pF}$ [4,5] in the output gate circuit CJFETs and non-linear modes of their operation [6].

The purpose and novelty of this article is to develop and research new circuitry solutions for CJFET buffer amplifiers. Today they are used as independent functional units in the tasks of a physical experiment [7-10] and in the structure of low-temperature and radiation-hardened sensor interfaces [11,12].

2. Single-ended CJFET buffer amplifiers
The suggested circuit of low temperature BA (figure 1a) [4] is peculiar because here small through static current $I_{th}$, going through output JFETs is stabilized due to rational selection of resistance R1, when a gate-source voltage M1 transistor achieves maximum values at small (microampere) source currents M1 transistor. It allows setting minimum values of $I_{th}$ in wide temperature range and excluding a dead-band in BA’s amplitude characteristics. The output stage (figure 1a) is characterized by linear characteristic in wide temperature and loading resistance range $R_{load}=2-100 \text{ k}\Omega$ [4] at low static current consumption.
The circuit (figure 1a) forces parasitic capacitor C1 recharging at high negative changes of input voltage. Thus transient setting time \( t_{\text{set}} \) (figure 1b) for specified area of dynamic error (10%) decreases. The BA’s slew rate (SR) for trailing edge increases from 20 V/µs to 150-180 V/µs at step input \( V_{\text{in}} = 3 \text{V} \).

![Circuit Diagram](image)

**Figure 1.** Cryogenic BAs Circuit [4] (a) and its Transient for Output Voltage Trailing Edge (b).

We conducted a computer simulation of the circuit of figure 1a on n-channel (M1 and M3) and p-channel (M2 and M4) transistors of the model library CJFET_5 of JSC "Integral" (Minsk, Belarus), which have a ratio of the gate width to its length is 50 \( \mu \text{m} / 6 \mu \text{m} \) for the p-JFET and 260 \( \mu \text{m} / 6 \mu \text{m} \) for the n-JFET. The following notation are introduced in the figure 1a circuit: + Vcc / -Vee is positive / negative bus power supply; \( C_2 \) is differentiating correction capacitor; \( C_{\text{load}} \) is load capacity; \( i_{\text{load}} \) is load current; \( V_{\text{GS},i} \) is the gate-source voltage of the \( i \)-th M1-M4 transistors.

2.1. Differential stages based on single-ended buffer amplifier

![Differential Stage Diagram](image)

**Figure 2.** CJFet Differential Stage (DS) based on Cryogenic BA figure 1a.
The buffer amplifier (figure 1a) circuit can be the basis of a number of modifications of differential stages operating in class AB mode (figure 2, [13]), which are perspective when developing operational amplifiers (Op-Amps) with high values of slew rate [6].

In the figure 2 circuit the following designations are introduced: \(-V_{ee}\) is negative voltage on power supply bus; Out.i1, Out.i2 is DC current outputs; \(C_1, C_1^*\) is parasitic capacitance; \(C_2, C_2^*\) is differentiating correction capacitors; M1-M8 is n-channels and p-channel CJFETs of JSC "Integral" (Minsk, Belarus); \(I_0\) is the static current; \(V_{GS,i}\) is the gate-source voltage of the \(i\)-th transistors M1-M8.

The transfer characteristic of DS (figure 2) is shown in figure 3. It shows that the DC operates in the class AB mode, which significantly improves the SR and \(t_{set}\) of the Op-Amp [13].

![Figure 3. CJFET Differential Stage’s Transfer Characteristic in LTspice Software at \(R_1=R_1^*=100\ k\Omega, t=-197^\circ C\).](image)

3. Balanced BA with Differentiating Correction Circuit

It is possible to apply the above architecture BA to develop balanced buffer amplifiers [14] (figure 4).

![Figure 4. CJFet Buffer Amplifier (a) and its Transient at High Input Impulse Signal \(V_{in}=V_0\), Comparable to Power Voltage \(V_{cc}\) (b).](image)

The resistor \(R_1\) sets a static mode for transistors M1-M4. The capacitor \(C_3\) forces recharge of parasitic capacitors \(C_1\) and \(C_2\).

When there is a large positive polarity pulse input signal and no capacitor \(C_3\), the transistor M1 of circuit on figure 4a is cut off practically immediately and capacitor \(C_1\) is charged by comparatively low current \(I_0\). It results in slow increase of voltage at BA output with relatively large time constant \(\tau \approx R_1C_1\) (figure 4b).
The parasitic capacitor $C_1$ is charged with additional current through the correction capacitor $C_3$ if the capacitor $C_3$ is turned on, the capacitance of which is selected significantly more than the capacitance $C_1$. In this case the transient processes become significantly faster in the circuit (figure 4b).

The static current through the resistor $R_i$ is determined by equations based on the second Kirchhoff's current law:

$$V_{GS2} - V_{R1} + V_{GS1} = 0,$$

$$I_0 = \frac{V_{GS2} + V_{GS1}}{R_i},$$

where $V_{GS1}, V_{GS2}$ is the gate-source voltage of the field effect transistors M1 and M2, respectively.

The static current of field effect transistors M3 and M4 with identical M2 and M3 (M1 and M4) is determined by the equations, similarly

$$V_{R1} - V_{GS4} - V_{GS3} = 0,$$

$$I_0^* = \frac{V_{GS4} + V_{GS3}}{R_i}.$$

3.1. Computer Simulation for Transient Processes in Balanced Buffer Amplifiers at Cryogenic Temperatures

There are transient processes in BAs (figure 4a) as a result of circuit investigation in LTspice software, using low temperature models of CJFET [15], on figures 5 and figures 6.

Figure 5. The Leading Edge of the Transient BA at a Temperature $-197^\circ$C.

Figure 6. The Trailing Edge of the Transient BA at a Temperature $-197^\circ$C.
The introduction of a differentiating capacitor $C_3$ significantly reduces the time it takes to establish a transient process, this follows from the analysis of the graphs in figure 5 and figure 6.

There is an amplitude characteristic of the suggested BA at low temperatures for different resistances on figure 7.

![Graph showing amplitude characteristics](image)

**Figure 7.** BA Amplitude Characteristics at Temperature $-197^\circ C$.

3.2. High-Speed Bridge Output Stages based on Balanced Buffer Amplifier

The topology of the balanced BA figure 4 discussed above can be applied in bridge output stages (figure 8), in which the load is switched on between two identical BAs (figure 4a) [14].

![Bridge differential stage schematic](image)

**Figure 8.** Bridge Differential Stage on Two BAs [14].

The dependence of the output currents of the bridge BA figure 8, corresponding to the load current $R_{load}$, as well as the output currents of the differential stage based on it, is shown in figure 9. It is
possible to increase maximum values of load currents by changing a number of parallel output transistors in circuit figure 8.

Figure 9. BA Output Currents (figure 8) for Current Outputs \(i_{\text{out.1}}\) and \(i_{\text{out.3}}\) Curve at Input Differential Voltage at Different \(N=1-3\) [14].

4. Conclusion
The article presents a new circuit technique for increasing the speed of cryogenic buffer amplifiers on complementary field-effect transistors with a p-n junction (CJFet technological processes, JSC "Integral", Minsk, Belarus). The proposed circuits are operable at low temperatures (up to -197°C) and have radiation resistance when irradiated with \(^{60}\)Co gamma rays and fast electrons with an energy of 6 MeV at a fluence of up to \(1 \times 10^{16}\) el./cm\(^2\) [15] due to the use of CJFet transistors. The article shows that the proposed circuitry solutions can improve by 5-10 times the slew rate of the output voltage and the transient setting time with a large input pulse signal.

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