Not All Fabrics Are Created Equal: Exploring eFPGA Parameters for IP Redaction

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Abstract—Semiconductor design houses rely on third-party foundries to manufacture their integrated circuits (ICs). While this trend allows them to tackle fabrication costs, it introduces security concerns as external (and potentially malicious) parties can access critical parts of the designs and steal or modify the intellectual property (IP). Embedded field-programmable gate array (eFPGA) redaction is a promising technique to protect critical IPs of an ASIC by redacting (i.e., removing) critical parts and mapping them onto a custom reconfigurable fabric. Only trusted parties will receive the correct bitstream to restore the redacted functionality. While previous studies imply that using an eFPGA is a sufficient condition to provide security against IP threats like reverse-engineering, whether this truly holds for all eFPGA architectures is unclear, thus motivating the study in this article. We examine the security of eFPGA fabrics generated by varying different FPGA design parameters. We characterize the power, performance, and area (PPA) characteristics and evaluate each fabric’s resistance to Boolean satisfiability (SAT)-based bitstream recovery. Our results encourage designers to work with custom eFPGA fabrics rather than off-the-shelf commercial FPGAs and reveals that only considering a redaction fabric’s bitstream size is inadequate for gauging security.

Index Terms—Embedded field programmable gate array (eFPGA), hardware security, intellectual property (IP) redaction.

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I. INTRODUCTION

A S TECHNOLOGY advances, integrated circuit (IC) complexity has grown significantly and led to increased outsourcing of the steps of the design flow to third-party entities in the supply-chain, as shown in Fig. 1(a). Outsourcing and globalization introduce many players in the supply-chain and this presents challenges of intellectual property (IP) theft, reverse-engineering, and malicious manipulation [1]. Consider IC layout design files which are sent to the foundry for fabrication, malicious (or compromised) employees can access these files and reverse-engineer the function to steal the IP of critical design portions or to insert hardware Trojans. Malicious end-users can obtain working ICs to analyze the I/O relationships and reverse-engineer the correct function (in collusion with a malicious foundry) to make unauthorized clones.

In response, researchers have proposed a myriad of solutions that aim to protect the confidentiality of the hardware IP, including design obfuscation and logic locking (see [2], [3], [4], [5], [6], [7], [8], [9], [10], and [11]). All these techniques obscure a design’s function by adding modules whose correct functionality depends on an external key [11] or by withholding information such as algorithm constants that only a legitimate user can later restore [2]. Incorrect keys corrupt the IC’s functionality, rendering the design useless to the malicious party. To date, attacks have overcome the protections. The most notable class of attacks is based on Boolean satisfiability (SAT) [3], [12], [13]. These SAT-based attacks assume an adversary with access to an unlocked implementation (the Oracle). Recently, redacting parts of an IP by using embedded field-programmable gate arrays (eFPGAs), as depicted in Fig. 1(b), has emerged as a promising, SAT-attack resilient defense [5], [7]. The intuition is that even small eFPGAs are insurmountable for SAT solvers because of their complexity and their size when converted into a representation for SAT solving [5]. Prior work has begun to characterize the feasibility of this defense by studying the overhead associated with this technique assuming a fixed FPGA architecture [14].

However, are all eFPGAs the same from a security perspective? To the best of our knowledge, the literature does not yet offer insights on how different eFPGA parameters, such as lookup table (LUT) size, affect the security offered by eFPGA-based redaction. In logic locking approaches, security is distilled into a single parameter: the key size [3]—a designer...
can choose a key size, as a measure of security, and incur follow-on impacts on power, performance, and area (PPA) metrics. In eFPGAs, the counterpart is the configuration bitstream size, which is determined by the conflation of multitudinous design choices, from logic element configuration through to routing channel width (see Section III)—in other words, the eFPGA design space is vast [15]. From a practical standpoint, it is crucial for designers to understand the relationships between security and other design factors. Thus, we address this gap in the literature by performing an empirical study of eFPGA architecture configurations and resistance to bitstream recovery through SAT-attack as the security metric. For insights into eFPGA-based IP redaction, we adapt an open-source FPGA design flow [16] to produce different eFPGAs, with different configurations, and explore how eFPGA parameters affect security. Our contributions are threefold as follows.

1) An analysis of eFPGA architectures that can be used for redaction. We analyze PPA and security effects and explore how the parameter choices of an eFPGA fabric “contribute” to the security provided by it.

2) A formulation of SAT-based attack for bitstream recovery of eFPGAs used for redaction and an experimental evaluation of eFPGA-based defense.

3) Insights into the practical considerations for adopting eFPGA-based redaction and a perspective on the future outlook of this IP protection technique.

In Section II, we present the hardware IP protection problem alongside prior work to tackle this issue. This is followed by an introduction to eFPGA and their architectural parameters in Section III, and architecture settings that we explore. Section IV details our initial attempts at eFPGA bitstream recovery, including threat model and assumptions. Section V revises our approach for eFPGA bitstream recovery, with insights into the security of eFPGA fabrics. We discuss insights from our study in Section VI and then conclude in Section VII.

II. RELATED WORK AND MOTIVATION

A. Key-Based Hardware IP Protection

Logic locking is a popular technique for hardware IP protection [3], [4]. Designers insert additional gates (controlled by an input key) to thwart reverse engineering of the real functionality. The key is known to the design house but unknown to the foundry. The correct key is installed into the chip after fabrication, assuming it is the only one that restores the correct functionality. So, the key is the one and only secret to be protected (by the designers) or retrieved (by the attackers). Attackers may have access to a working chip (called Oracle) for key recovery by analyzing I/O relationships with SAT-based formulations [12], [13], [17], [18], [19], [20]. Otherwise, they can analyze the existence of structural artifacts [21], [22] to guess the correct key bits. Designers need to design locking techniques such that they: 1) protect the semantics of the circuit; 2) guarantee that the key is not easy to retrieve; and 3) minimize hardware overhead.

For protecting essential semantics, locking is applied at register transfer level (RTL), even though these methods incur significant area overhead [2]. Other methods aim at trading off different security metrics, like SAT resilience and corruptibility [23], but these approaches have structural vulnerabilities, leading to key recovery [24]. In all cases, the security of such key-locked design is proportional to the number of key bits. However, the key cannot grow indefinitely because of technological constraints like the size of the tamper-proof memory where it is installed.

B. eFPGA-Based Redaction

IP redaction is an alternative method to logic obfuscation. In this case, designers select specific modules—the ones they want to protect—to conceal and replace them with soft eFPGAs (i.e., reconfigurable fabrics described in RTL and designed using standard-cells with the rest of the chip). The key idea is that only a sub-design gives the design house a competitive market advantage. An eFPGA is a soft IP module that includes configurable logic blocks (CLBs) containing LUTs, flip-flops (FFs), and routing logic that can be fabricated and programmed to implement the desired functionality. The specific configuration of such devices is called bitstream. A bitstream must include the configuration of each configurable module of the eFPGA. When used for redaction, the designer will insert the eFPGA module to replace the “sensitive” parts of the design that are thus unknown to untrusted parties during fabrication. On the contrary, the attacker must recover the complete bitstream to implement the correct functionality in each eFPGA, which is now the “secret” to be protected. eFPGA-based redaction is particularly attracting for thwarting several reverse-engineering attacks. On the one hand, structural attacks are difficult to be applied because the eFPGA is regular and generic, able to implement an arbitrary functionality. On the other hand, the size of the configuration bitstream grows exponentially with the complexity of the eFPGA architecture, significantly enlarging the key space and so thwarting SAT-based attacks [5], [7], [14].

Fig. 2 shows the general flow for eFPGA-based redaction. After selecting the portion of the design to be redact, it goes through the fabric generation step, while the rest of the chip is designed and optimized as usual. The fabric netlist describes the eFPGA architecture and is then recombined with
the rest of the chip to go through the physical design flow. The redacted module is instead compiled into a bitstream to configure the eFPGA after manufacturing. This obfuscation technique is resource-intensive, occupying considerably more area than the baseline design as noted in [14]. The studies by Tan et al. [3] and Chakraborty et al. [25] offer an in-depth analysis of various IP obfuscation methods but not eFPGA-based redaction. Interested readers can check those works for a sense of the drawbacks of non-eFPGA-based techniques. Prior work [14] studied only the eFPGA architecture and restricted the analysis to consider security primarily. While the approach is promising, there are several issues to address. Which module(s) should a designer redact? What is the impact of inserting eFPGAs into ASIC design flow? How can the designer generate the proper eFPGA architecture? Are all eFPGA architectures equally secure? We explore the correlation between overhead and security, considering eFPGA architecture as a variable that designers can tune. By picking the parameters for the eFPGA, we can achieve similar security level with a smaller fabric, minimizing overhead.

When deciding which module(s) to redact, the designer could know the “sensitive” parts of the design, manually driving the selection [5], or use methods based on high-level synthesis (HLS) to identify the logic that differentiates variants of the same design [6]. In all cases, the designer assumes a standard or even off-the-shelf implementation of the eFPGA, incurring significant overheads. Several open-source CAD flows can be used to generate the eFPGA architectures and the corresponding bitstream for the modules to be redacted. Yosys and VTR/VPR can be used to identify the fabric parameters, along with a Chisel-based generator [5]. OpenFPGA is an open-source generator of customizable FPGA architectures that can be combined with logic synthesis flows to generate the proper configuration bitstream [26]. While these approaches allow exploration of fabric parameters, their security and design implications have never been explored in the case of IP redaction. The security of eFPGA-based redaction comes, in principle, with the size of the configuration bitstream rendering SAT-based attacks infeasible [5]. However, the impact of different eFPGA architectures on SAT resilience is unclear; exploring this impact is the topic of our work.

We base our exploration on OpenFPGA, i.e., an open-source eFPGA generator, precisely because we can explore different parameters and produce the corresponding fabrics—specifically for redaction—that are smaller than commercial eFPGAs. In fact, commercial eFPGA fabrics are less flexible, closed, and typically larger as they prioritize other design goals (e.g., FlexLogic fabrics [27] start at ~1 K LUTs). We note as well that redacting parts of an IP with small fabrics can already incur considerable overheads [5]. Next, we will introduce the eFPGA architecture, describing which parameters we consider.

### III. Background on eFPGA

This section provides a brief overview of FPGAs, covering the most crucial parts, i.e., architectural choices and electronic design automation (EDA) toolchains for agile hardware development techniques. These are the essential factors for enabling eFPGA redaction, as explored in this article. We refer the readers to the work of Boutros and Betz [15] for more details on FPGA architectures.

#### A. FPGA Architectures

FPGAs are reconfigurable fabrics that are (re)-programmable “in the field” to implement a specific digital design. Modern FPGAs are designed using a tile-based architecture, where the FPGA comprises repeatable tiles and a “sea” of routing resources, as shown in Fig. 3(1). A $B \times B$ architecture means there are $B$ tiles distributed in horizontal and vertical direction, respectively. For example, Fig. 3(1) shows a $5 \times 5$ FPGA architecture. The predominant tiles in an FPGA are CLB tiles that implement logic functions. An example of a CLB tile is shown in Fig. 3(2); it contains a CLB and blocks for setting the connection between signals within and outside the tile. Modern FPGAs can also include some specialized tiles, such as block RAM (BRAM) or digital signal processing (DSP) tiles. A heterogeneous tile-based FPGA gives the designer flexibility to meet design requirements and also control the PPA aspects of the architecture. Tile-based architectures offer a better trade-off between programmability and efficiency compared to alternatives [15]; designers can also separately focus on the problem of how to route and connect signals within a tile, and problem of interconnecting tiles “globally.” This allows engineers to focus on optimizing the layout of a tile and spend less time on placing and routing tiles at a lower
level of abstraction, the building blocks of an FPGA include the following.

CLBs are used to implement combinational and sequential logic. Fig. 3(➍) shows a detailed CLB architecture, where there are N \textit{basic logic elements (BLEs)} which are connected through a \textit{local routing architecture}. A BLE is the primitive module implementing logic functions and comprises a LUT, an FF, and a two-input multiplexer, as shown in Fig. 3(➎). One can map a K-input single-output Boolean function to a single K-input LUT. By configuring two-input multiplexer, a BLE can operate in either combinational or sequential mode. To route interconnect CLB inputs and BLE inputs and outputs, the local routing architecture, typically implemented as a crossbar, includes a set of programmable multiplexers. The local routing guarantees that BLEs can be fully connected to each other and also to every CLB input pin.

As shown in Fig. 3(➍), the fabric can be configured such that the output from the BLE can be fed back in as an input, creating a possible loop in the design. This concept is further elaborated in Fig. 3(➎), where for various SRAM values, the output from the LUT may reappear as input via some combinations of the bitstream that controls the local routing. In traditional design methodology, such “combinational loops” are avoided to prevent instability. Therefore, when generating a bitstream for the fabric, the tool is mindful to prevent any accidental introduction of combinational loops in the design.

The logic capacity of a CLB is determined by the following parameters: 1) input size of LUTs, K; 2) numbers of BLEs in a CLB, N; and 3) number of inputs to the CLB, I. These parameters are chosen based on the trade-off between the logic capacity and impact on the area, delay, and power. To have better resource utilization in a CLB, for any LUT size, \( I = (K(N+1))/2 \) has been shown to give good PPA [28].

The \textbf{Global Routing Architecture} determines the signal routing outside CLBs, and comprises connection blocks (CBs) and switch blocks (SBs). Both CBs and SBs employ programmable multiplexers for routing. CBs are used to connect the input and output of CLBs to routing tracks (that connect different tiles) and SBs connect routing blocks together for producing longer routes between tiles [15]. Typically, a sparse connection is used for global routing where a routing multiplexer is connected to a subset of routing tracks to have a better trade-off between routing area and routability.

Parameters for routing include: 1) the number of routing tracks grouped together in a channel, \( W \); 2) the fraction of routing track connected to a CLB input, \( F_{c.in} \); 3) the fraction of routing track connected to a CLB output, \( F_{c.out} \); and 4) the number of routing tracks that can be connected to one routing track, \( F_c \). In modern FPGAs, unidirection global routing is preferred over classical bidirectional routing [29], as it can save 25% area and improve delay by 9%. Fig. 4 illustrates an example of a unidirectional global routing architecture, where CLB CLB0 is surrounded by an SB SB0 and CB CB0, with a channel width (\( W \)) of 4. \( F_{c.in} \) of inputs pins IN0, IN1, and IN2 are \( 2/4 = 0.5 \), \( 3/4 = 0.75 \) and \( 4/4 = 1 \), respectively. \( F_{c.out} \) of output pins OUT1 and OUT2 have the same value of \( 2/4 = 0.5 \). Each routing track connects to three other tracks, thus \( F_c \) and \( F_{c.in} \) in SB0. Usually, a routing path starts from a CLB input, and connect to routing track through a CB, and then passes through SB, to finally reach a CLB output through another CB. But, if CLBs are far from each other, the routing may have to go through a number of SBs, increasing the delay. To tackle this, routing tracks are allowed to span multiple CLBs. This parameter is defined as the length of routing track \( L \), i.e., the number of CLBs spanned by a routing track.

The FPGA is configured by loading a \textit{bitstream}, where each bit sets some element of the fabric, such as routing configurations and LUT contents. One can load the bitstream with frame-based [30] and scan-chain based [26], [31] configurations. In this study, we focus on scan-chain-based bitstream programming, where the bitstream is loaded sequentially, one bit per cycle, with a dedicated clock (prog_clk).

\section*{B. Open Source (e)FPGA Design Flows}

Heterogeneous computing has renewed interest in eFPGAs due to their flexibility and adaptability. Commercially, FPGA are coupled tightly to processors in a single-chip so that they can act as a programmable accelerator or...
coprocessor [32], [33], with benefits like increasing the peak performance of a System-on-Chip (SoC) by 3.4× along with a 2.9× power reduction. Different SoCs can be customized with different eFPGA fabrics to best serve a specific application’s requirements, e.g., eFPGAs for machine learning require a high density of DSP blocks, embedded memories, and arithmetic accelerators (such as for multiply and accumulate).

Recently, open-source (e)FPGA prototyping tools have emerged [16], [30], [34]. Fig. 5 illustrates principles of the OpenFPGA framework for prototyping customizable eFPGAs [16]. The framework provides a unified environment for FPGA IP Prototyping and supporting FPGA CAD tools. In the XML-to-layout flow, designers produce fabrication-ready eFPGA layouts by specifying designs with XML-based architecture description languages [35], [36], customizing circuit elements, standard cells, and flexible hardware IPs. The core engine converts the architecture description Verilog netlists (either tech-mapped or synthesizable). The autogenerated netlists are postprocessed [37], with a focus on easing the physical design flow, and then followed by Place and Route (P&R) tools for generating GDSII layouts and design sign-offs. For functional verification, OpenFPGA also produces Verilog testbenches. The testbenches validate the correctness of a generated fabric, simulating a complete process, including bitstream downloading and eFPGA operation. The ability to create custom fabrics is a better fit for redaction compared with off-the-shelf (commercial) eFPGA IP [5]. In the Verilog-to-Bitstream flow, end-users can implement HDL designs on the eFPGAs. HDL designs are first synthesized by Yosys [38] and physically mapped (packed, placed, and routed) on the eFPGA programmable resources using VPR [39] tool. The implemented design is translated to a bitstream which is compatible with the configuration protocols of eFPGAs.

Open-source efforts aim to overcome two major technical barriers of contemporary eFPGA development: 1) the time-consuming physical design process—by leveraging the sophisticated ASIC design tools rather than manual layouts and 2) the increasing design complexity of associated EDA tool-chain—by using well-known open-source FPGA architecture exploration tools, e.g., VPR [39], rather than developing ad hoc, in-house tools. Using the design flows in Fig. 5, the development cycle of a 160k-LUT FPGA layout is ∼24 h and its performance is competitive against commercial products [16], [37]. We thus adopt the OpenFPGA framework to implement eFPGA fabrics [16] for redaction and provide insights into our experience.

C. eFPGA Architecture for this Study

Given the different FPGA architectural parameters, as we described in Section III-A, we are interested in understanding how changing the parameters affects security. As the design space is considerable, we limit our study to exploring the $K$ and $N$ parameters, as these are the factors that have a direct impact on complexity and hardware utilization. In the FPGA fabric netlists, LUTs comprise a tree-of-MUXes, so varying $N$ and $K$ changes the MUX sizes.

To summarize, Table I describes the architecture settings that we explore for generating eFPGA redaction fabrics. For this study, we use a tile-based FPGA to emulate complexity similar to that in a commercial FPGA, and vary the overall fabric size from $4 \times 4$ to $6 \times 6$ tiles. For consistency of results, we use unidirectional routing. These parameters are set on the basis of the prior studies of FPGA designs [15], [28], which showed that these ranges of parameters give the best PPA results. In this work, we first characterize the fabrics’ bitstream size, area, power, and delay, and then evaluate their security in Sections IV and V.

1) Tool Setup for Fabric Design: To generate the fabrics and determine the cost of the redaction fabrics based on area, power, and delay, we synthesize, place, and floorplan fabrics that we generate using the OpenFPGA flow [36]. This flow is depicted in Fig. 2. For synthesis, we use Cadence Genus 18.14 and for layout implementation, we use Cadence Innovus 18.10. The timing, area, and power reports are generated by Innovus. For floorplanning we set utilization to 70% for faster timing closure. We use FreePDK 45-nm library [40] for our study.

2) Bitstream Characteristics: Table II reports the number of bits required for the configuration bitstream, and this can be taken as a measure of the overall “programmability” of the fabric. It is important to note that there are overlaps in bitstream sizes across tile sizes (e.g., $4 \times 4$ K7N8 fabric has more bits in its bitstream compared to $5 \times 5$ K5N7).

3) Area Characteristics: Table III shows how the area is affected by varying $N$ and $K$. For a given $N$ value, as we increase $K$ the number of inputs to the CLB increases (as a result of the relationship between $I$, $K$, and $N$ mentioned in Section III-A); increasing the LUT sizes in the BLEs and also slightly affecting local and global routing. For a given $K$, however, an increase in $N$ has more impact on increasing the area, as entire BLEs are added; this increases the complexity of both local and global routing, as suddenly there is a jump of another $K$ inputs to the CLBs, resulting in added pressure on local routing to route this additional set of inputs to CLBs. This forces the global routing (CBs and SBs) to increase the routing complexity as more inputs are being fed to CLBs.
4) Delay Characteristics: Compared to our study on area, the impact on the critical path delay from varying \(N\) and \(K\) is less obvious, as shown in Table IV. As observed in prior work [15], [28], the impact on delay is not a linear function of \(K\) and \(N\). In our fabrics, we observe that for a given \(N\), the delay values improve as one increases \(K\), where the least delay is generally achieved for the largest \(K\) (\(K = 7\)).

5) Power Characteristics: Power is shown in Table V. Similar to the area, power increases with the complexity of the fabric (increasing \(K\) and \(N\)). If one looks at the two extremes for a given fabric size, \(\{K = 3 \text{ and } N = 2\}\) and the other being \(\{K = 7 \text{ and } N = 8\}\), there is 10\(\times\) increase in power consumption.

D. General Observations

There is considerable variation in bitstream size, area, delay, and power as we vary \(K\) and \(N\), given a fabric size. Given a
module to redact, a designer will naturally be drawn to the fabric configuration with the least area/power/delay that can fit the redaction target. However, let us consider bitstream size as our security parameter (intuition: more bits in the bitstream, more security). Seeing as there are fabrics that have similar configuration bitstream sizes with different fabric sizes, this begs the question: Can we gauge security by considering only the bitstream size? Take, for instance, the 4 × 4 K7N8 fabric uses 6361 bits for its bitstream, does this mean better security compared to the 5 × 5 K5N7 fabric, which ~1000 fewer bits and requires smaller area? In Section IV, we perform a security analysis on all the fabrics to try to see if this is indeed the case.

IV. ASSESSING EFPGA-BASED REDACTION FABRICS

This section describes the threat model and assumptions under which our study operates, outlines our intuitions about the characteristics of eFPGAs generally that contribute to their security, and then presents the results of our experiments. We perform the experiments using high performance computing (HPC), with jobs running in parallel, each on an independent compute node that has an Intel Xeon Platinum 8268 processor running at 2.9 GHz and 256 GB of RAM.

A. Assumptions and Threat Model

For insight into the security offered by using eFPGA-based redaction, we explore SAT-attack resilience of the various fabrics (as described earlier in Section III-C), as this has been used to gauge the security of redaction in prior work [5] and has proven to be a challenge to overcome for prior IP protection approaches [3]. Previous work suggests that large FPGA bitstream lengths make SAT-based attacks impractical [7] and the evaluation results in [5] appear to support this claim.

As we want to investigate how structural variations of the eFPGA contribute to complexity parameters of SAT-based attacks, we perform a security evaluation by launching an SAT-based attack on the fabrics described in Section III-C. In our analyses, we assume that the designers already know which parts of the design must be protected to stay competitive in the market. Hence, this article does not address the selection of the modules to be redacted; we assume that a given fabric is already selected as sufficient for their desired redaction. For worst case analysis, our threat model overwhelmingly favors the attacker. We assume the attacker has access to the redacted IC’s netlist and to a fully scanned1 and fully unlocked design (i.e., access to an Oracle with the bitstream loaded).

The adversary has to overcome three challenges before they can launch an SAT-based attack on eFPGA fabric. First, they have to isolate the eFPGA fabric from the rest of the IP; this is possible since the regular structure of the fabric is distinguishable from the rest of the design. Second, for the Oracle, the adversary should have complete control over the inputs, outputs, and internal FFs, excluding configurable FFs. We endow the attacker with these capabilities although there are orthogonal efforts to mitigate this Oracle-based threat model [11]. Third, the adversary cannot extract the FPGA bitstream [7], i.e., the attacker does not have access to the configuration FFs, so cannot steal the bitstream directly. While there are many attacks on FPGA security [41], we consider such attacks orthogonal to this study. Physical attacks (e.g., optical probing [42]) are out of scope. Our threat model and assumptions are consistent with prior work [5].

B. Security Evaluation Setup

In an eFPGA, the bitstream is loaded into configuration FFs. The configuration FFs are interconnected as a scan-chain driven by a programming clock (prog_clk). To prepare the fabrics that we generated in Section III-C, we need to transform the gate-level netlist and produce a netlist understood by an attack tool, with the configuration bitstream as a set of “key inputs.” To identify the configuration scan chain, we do a depth-first search of the netlist, starting from the scan_in_head port, until we reach the scan_in_tail. All FFs in the traversal path driven by the programming clock (prog_clk) store the configuration bitstream. The order in which the configuration FFs are detected corresponds to the bitstream order. The detected configuration FFs are exposed as primary key inputs to convert the eFPGA netlist into a netlist suitable for SAT attack. This netlist is fed to improved cyclic SAT (IcySAT) [13] to unroll hard loops (as will be explained next). To model an Oracle, we use the same locked netlist, but set the key bits to the configuration values from the bitstream.

1For those unfamiliar with Design-for-Test concepts, a fully scanned design means that all FFs have been replaced with scan FFs that are connected to each other into a long scan chain, essentially acting as a large shift register. A tester is able to scan-in values and then scan-out the combinational logic outputs a clock cycle later, thus deducing the input–output relationship for the logic in the design.
generated in the OpenFPGA flow. The unrolled netlist and the oracle netlist are used with the KC2 attack tool [20].

C. On Combinational Loops in eFPGAs

The SAT-based attack requires an attacker to model a miter circuit featuring the design-under-attack as input to an SAT solver [12]; for an eFPGA fabric, the configuration bitstream is the “key.” There are several factors that make an SAT solver’s task challenging. SAT solvers fail in the presence of combinational loops [19], as these lead to unstable results or repeated distinguishing input patterns (DIPs). Note that, in well-formed designs, circuits with structural combinational loops are usually designed such that the overall design behaves as though it is acyclic. The structure of eFPGAs includes instances of such loops due to the reconfigurable routing network in the fabric. The sequence of reconfigurable logic represented by the chain of LUTs/CLBs interconnected by this network adds a polynomial complexity to an SAT formulation.

To launch an SAT attack on designs with loops, like in eFPGAs, one needs to preprocess the netlist to break the loops and create an acyclic equivalent. Researchers have proposed multiple approaches to modify the SAT attack for cyclic designs [13], [18], [19]. We observe that eFPGAs have hard combinational loops that cyclic SAT (CycSAT) [19] cannot resolve. These hard loops are intertwined such that, when CycSAT breaks a loop to make the circuit acyclic, at least one loop remains. The acyclic constraints generated by CycSAT overlook such loops and live-locks the solver into repeating the same DIPs. Behavioral SAT (Be-SAT) [18] can break such loops by pruning the keys leading to live-lock DIPs. However, it has exponential complexity in key size. IcySAT II [13] is a loop-breaking alternative that finds a subset of feedback nets that, when removed, make the circuit acyclic. The circuit is “unrolled” with respect to these feedback nets, with an unroll factor equal to the size of the feedback set. The unrolled circuit can be fed into an SAT tool.

D. Relating Attack Complexity to eFPGA Parameters

There are several ways to thwart an attacker (or at least, their SAT solver). One is to make the circuit very large, such that its representation as a Boolean formula requires an impractical amount of memory to load for the solver—the need to “unroll” loops increase security in this way, as formula sizes grow due to the need for circuit replication or additional constraining clauses. In fact, the time complexity of the IcySAT attack that we use is directly related to the total number of clauses and variables that needs to be solved by the solver in retrieving the eFPGA bitstream. This complexity can be directly related to the constraints added in a single SAT attack iteration, which is proportional to the unroll factor. eFPGA fabrics are naturally loop-ridden, arising from the sophisticated intra-CLB (local routing) and inter-CLB (global routing) routing networks. Also, another source of variables in the formula is the presence of LUTs within the CLBs, where the contents of LUTs should be determined to reverse-engineer the logic functionality. Prior work [43] explains how programmable logic renders SAT complexity. An SAT solver might encounter difficulties due to the polynomial complexity in solving interdependent clauses despite the number of clauses being nominal, as is the case with the LUTs within the eFPGA fabric.

Table VI gives the attack-time for different $K$ and $N$ in a 4 × 4 tile configuration, and the corresponding bitstream sizes, fabric size (measured as the number of gates after producing an

$^2$IcySAT-II, which we will refer to as IcySAT in this article.

\begin{table}[h]
\centering
\caption{IcySAT Attacks on Architectural Variants of 4 × 4 eFPGA Fabric. TO Represents Time-Out}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
Fabric & Unroll & Bitstream & #Gates & Time & Variables & Clauses \\
\hline
K3N2 & 64 & 601 & 4227 & 127.6 & 551293 & 1433840 \\
K3N3 & 70 & 725 & 5179 & 283.8 & 737293 & 1922216 \\
K3N4 & 79 & 837 & 6355 & 6998.15 & 1019357 & 2681792 \\
K3N5 & 73 & 941 & 7686 & 14035.9 & 1135927 & 306984 \\
K3N6 & 105 & 1154 & 9284 & TO & – & – \\
K3N7 & 85 & 1243 & 10823 & TO & – & – \\
K3N8 & 130 & 1393 & 12405 & TO & – & – \\
K4N2 & 55 & 639 & 4053 & 103.54 & 454039 & 1167026 \\
K4N3 & 57 & 810 & 5439 & 891.65 & 629232 & 1642049 \\
K4N4 & 63 & 1049 & 8230 & TO & – & – \\
K4N5 & 113 & 1316 & 10141 & TO & – & – \\
K4N6 & 112 & 1468 & 12352 & TO & – & – \\
K4N7 & 85 & 1647 & 14616 & TO & – & – \\
K4N8 & 132 & 1849 & 17406 & TO & – & – \\
K5N2 & 65 & 815 & 5185 & 267.8 & 685187 & 1773156 \\
K5N3 & 68 & 1066 & 7235 & 25135.2 & 996664 & 2618621 \\
K5N4 & 105 & 1477 & 11274 & TO & – & – \\
K5N5 & 136 & 1741 & 13817 & TO & – & – \\
K5N6 & 104 & 2012 & 17170 & TO & – & – \\
K5N7 & 144 & 2271 & 20836 & TO & – & – \\
K5N8 & 162 & 2573 & 24635 & TO & – & – \\
K6N2 & 69 & 1125 & 6831 & 2033.91 & 955817 & 2481464 \\
K6N3 & 70 & 1518 & 6976 & TO & – & – \\
K6N4 & 93 & 2089 & 14762 & TO & – & – \\
K6N5 & 93 & 2694 & 20357 & TO & – & – \\
K6N6 & 144 & 2928 & 24089 & TO & – & – \\
K6N7 & 143 & 3347 & 28946 & TO & – & – \\
K6N8 & 164 & 3989 & 34073 & TO & – & – \\
K7N2 & 54 & 1671 & 9559 & TO & – & – \\
K7N3 & 95 & 2434 & 14700 & TO & – & – \\
K7N4 & 93 & 2089 & 14762 & TO & – & – \\
K7N5 & 84 & 3221 & 21285 & TO & – & – \\
K7N6 & 101 & 3917 & 27075 & TO & – & – \\
K7N7 & 146 & 4620 & 34003 & TO & – & – \\
K7N8 & 151 & 5511 & 41913 & TO & – & – \\
\hline
\end{tabular}
\end{table}
equivalent fabric netlist using two-input gates for the attack), and the number of variables/clauses in the Boolean formula for the attack as reported by the kC2 attack tool on a successful attack. We set a time-out of two days. All 6 × 6 and all but one 5 × 5 fabrics timed-out (smallest 5 × 5 fabric, K3N2, bitstream size: 1204, was recovered in 18 190 s).

Focusing on the data from the successful attacks, the unroll factor does not show a monotonous or significant change as one varies K while keeping N constant. This suggests that there is no significant progress/change in the complexity of combinational cycles in increasing the size of LUTs in CLB. A higher K adds higher complexity to local routing while maintaining or decreasing complexity of global routing. In contrast, increasing the N value while maintaining constant K caused a significant monotonic increase in unroll factor for distinct constant K values. Increasing N with constant K increased the global routing complexity while maintaining the local routing complexity. From these experiments, we can infer that the unroll factor, and hence the SAT attack complexity, is related to the complexity of the global routing network.

Fig. 6(a) shows the attack times for different N, with a fixed K = 3 (N = 6 and N = 7 timed-out). These are plotted against the size of the unrolled fabric. This validates our claim that attack time increases with gate size of the unrolled eFPGA fabric netlist. Although the attack timed out for K > 3, we expect the attack complexity trend for K > 3 to continue, given the unrolled gate-size for K > 3 as shown in Fig. 6(b).

Fig. 7(a) shows the attack complexity as a function of K with fixed N = 2. As anticipated, the attack complexity increases with increasing K. Increasing K with fixed N is associated with increasing SAT hardness due to the presence of larger LUTs. Although it also renders more complex local routing, previously we found that local routing does not appear to significantly change the unroll factor and hence does not contribute to the complexity arising from combinational cycles. Hence, we can say that the attack complexity in this case is primarily sourced from SAT hardness of LUTs. For K = 3, the attack time trend in Fig. 7(a) aligns with the trend seen for total two input gate-size shown in Fig. 7(a), which once again validates our claim that SAT attack complexity is directly related to the gate-size of unrolled eFPGA fabric.

Fig. 7(b) shows the total unrolled gate-size for various N, K values. The increase in SAT attack time-complexity due to increasing N dominates vis-a-vis the increase in attack complexity due to increasing K. This result hints at the fact that SAT attack complexity from cyclic networks within the eFPGA fabric contributes more to SAT attack complexity compared to the SAT attack complexity from SAT hardness of LUTs within the fabric.

V. WHAT HAPPENS IF WE PARTIALLY UNROLL?

In Section IV, we found that the complexity of the cyclic network and the associated SAT complexity of the eFPGA fabric is related to the complexity of global routing. The unroll factor required for a complete IcySAT attack is expected
to increase significantly with more complex global routing. Since the unrolled gate-size of the eFPGA fabric is directly proportional to the size of the unroll factor, this is the primary quantifiable parameter to gauge SAT complexity.

A. Unroll Factor

In Shamsi et al.'s original presentation of IcySAT [13], the recommendation is to set the unroll factor equal to the cardinality of the nonoptimal subset of nets that must be broken iteratively to remove the cycles in the circuit. With increasing complexity from cyclic networks in the global routing of eFPGAs, more nets have to be broken to render an acyclic eFPGA netlist. For the general case, Shamsi et al. propose that a circuit should be unrolled unroll factor a number of times to perfectly replicate the functions of a cyclic circuit with an acyclic equivalent. This is based on a worst case assumption that there might exist at least one trace between any pair of broken nets that traverses through all other broken nets, in which case, to perfectly replicate the intended acyclic behavior, the circuit has to be unrolled unroll factor times—we will refer to this as the original IcySAT's “ideal” unroll factor. We contend that this worst case scenario is a rare, at least in the context of eFPGA fabrics, which suggests that a partial unrolling might be sufficient for a successful attack. If we can unroll a circuit partially, the resulting Boolean formula will be smaller, and more easily digested by an SAT solver.

Thus, to investigate the possibility of recovering the bitstream after only unrolling a redaction fabric partially in the preprocessing step, we study the attack under three unroll factors: 10, 20, and 30. From the perspective of an adversary, the recovered bitstream is correct only if the locked netlist is found to be formally equivalent to the functional Oracle by applying the bitstream. The experimental setup is in Section IV.

B. Results

Table VII presents the attack results on partially unrolled variants of $4 \times 4$ and $5 \times 5$ eFPGA fabrics. The attack was incrementally performed for different unroll factors until we recovered a bitstream that rendered the locked fabric netlist formally equivalent to the Oracle netlist. The ✓ in Table VII represents a failed attempt in which the recovered bitstream rendered a nonequivalent fabric, whereas the ✗ represents a correct bitstream solution. Upon getting a correct solution, further unrolling is skipped which is represented by (−). We observed that the bitstream for most of the fabrics in $4 \times 4$ variants could be successfully recovered by partial unrolling, in contrast to the results of Section IV.

The % column in Table VII shows that the adversary could successfully recover the bitstream, even when the unroll factor is as low as 6% compared to the “ideal” unroll factor that would be used in the original IcySAT attack formulation. This demonstrates that the “actual” SAT complexity imparted by the cyclic networks of eFPGAs is lower than the expected complexity suggested by using the typical IcySAT algorithm. Although we do not have data representing the minimum unroll factor required to correctly recover the bitstream for each fabric, the data collected from successful attacks in this partial case might suggest that fabrics with higher “ideal” unroll factor (as determined by the original IcySAT algorithm) but smaller circuit size (in terms of the number of two-input gates in the netlist) are more attack resilient compared to fabrics with lower “ideal” unroll factors but larger circuit size. The fact the bitstreams for so many of our fabrics were recovered in the partial unrolling case does raise concerns about the security of eFPGA redaction and merits further study.

VI. DISCUSSION

A. Gauging Security

Given the results of our security assessment in Section IV, we now revisit the question: can we gauge security by considering only the bitstream size? As we alluded earlier, the bitstream, being the “key” in eFPGA redaction, might be thought of as the security parameter. This is the case in prior work [5] and other attempts at logic locking/obfuscation. In the case of eFPGA-based redaction, however, our experimental results indicate a more complex picture. Fig. 8(c) depicts the attack times for fabrics of different bitstream sizes. Although we can observe that the attack time generally increases with larger bitstream size, the distribution is scattered and hence the relationship between security and bitstream size is not definitive. One can argue that increasing the number of LUTs and LUT inputs makes SAT attacks harder; however, given that designers must also consider PPA overheads, our findings show that the story is more complex when also considering security. We note that the attack time appears better correlated with the total number of gates in the unrolled netlist, which is similar to the trend observed in the product of unroll factor and the gate size of the netlist (see Section IV). For instance, K5N3 with a bitstream size of 1066 is found to have approximately 10× attack time compared to K6N2 with a bitstream size of 1125. When we examine gate size, however, notice that the gate size of the K5N3 fabric is much more than that of K6N2, resulting in more clauses for the SAT attack. This explains the difference in attack time.

To further explore the possible contribution of bitstream toward attack complexity, we examined the bitstream in terms of the number of bits used to configure the different parts of the eFPGA. Since the eFPGAs used for redaction have fixed IO configuration bits, the bitstream has three parts: 1) logic configuration bits that set the contents of LUTs; 2) local routing configuration bits that select the input of the crossbar multiplexer that multiplex the CB outputs to the LUTs; and 3) global routing configuration bits, being the sum of CB and the SB configuration bits. Fig. 8(d)–(f) (where, LR and GR stands for local routing and global routing, respectively) demonstrates how the attack time varies with logic, local routing, and global routing bits.

B. eFPGA Fabric Resource Utilization

The cost of redaction tremendously increases as one move toward a complex or different fabric size as shown in Tables III and V. Thus, a designer should have an idea of how much resources in terms of logic and I/Os are available
in a fabric. This will lead to a better resource use in the fabric when one redacts a module, especially if one adopts an HLS approach [6], [7]. There are two cases limiting the choice of a fabric.

1) Logic: Number of CLBs required to map a design.
2) I/Os: Number of inputs and outputs of a module.

For the first point, one can increase either $K$ and $N$ values in a fixed fabric, to increase its logic capacity rather than moving to bigger fabric sizes. To increase the number of I/Os, one can increase the capacity of I/O tiles, but routing becomes complex, but lower increase in overhead compared to next-sized fabric.

### C. Area Versus Security

Our results from Tables VI and VII suggest that the security of fabric is dependent on multiple parameters like fabric size, unroll factor, and their relative measures. We have shown that, even within a fixed fabric size, by varying $K$ and $N$, the resulting SAT-based attack duration can vary considerably. Hence from a designer’s perspective with a fixed area budget, a smart choice is to choose a fabric with the right size of resources while maximizing security by considering the insights from Sections IV and V. For better visualization, we have plotted the time taken by the successful attacks against the area of the attacked fabric, shown in Fig. 8(a), where one can observe that, for a fixed area, the attack times can significantly differ for different fabric configuration. This implies that the security of a fabric is not solely dependent on the area but on the combination of parameters of the FPGA architecture.

### D. Area-Delay Versus Security

The Area-delay product provides a more general measure of the trade-off between area and delay [28]. As shown
Their implications on security should also be studied. With present knobs that further expand the design space and security parameters.

When we consider attack-time versus area-delay in Fig. 8(b), we have seen similar sort of results (CBs and SBs), where the delay will be quite large compared to intracluster routing. We have seen similar sort of results when we consider attack-time versus area-delay in Fig. 8(b), where one can select a fabric with better area-delay and security parameters.

E. Study Limitations and Future Work

Our study explores the security implications of eFPGA fabrics by varying two parameters: \( K \) and \( N \) from Table I. The study in this article motivates further scrutiny of eFPGA architectures for redaction to better enable better trade-offs between PPA and security. There are more parameters that can be configured in redaction fabric design as our future work. This includes alternative LUT designs, such as fracturable LUTs, which have been shown to facilitate better resource utilization as more than one function can be mapped to a LUT with the cost of only a few gates to separate the different outputs of a LUT. This will somewhat increase the routing complexity (both local and global), with more numbers of input and outputs to consider but could result in only a slight change in the overhead compared to mapping two different functions to separate LUTs in a conventional FPGA design [15], [28]. In future, we will extend the analysis to include BRAMs and DSPs as they represent more points in the design space [15].

For our study, we fixed \( W, F_{e,\text{in}}, F_{e,\text{out}}, F_s, \) and \( L \). These present knobs that further expand the design space and their implications on security should also be studied. With regard to our security evaluation, our partially unrolled IcySAT experiments featured a limited number of unroll factors. In future work, we will find the minimum unroll factor at which a given bitstream can be recovered by more comprehensively sweeping unroll factors. Moreover, for designs where all three unroll factors failed to recover the correct bitstream, note that higher unroll factors and higher time-outs may still recover the correct keys. For instance, the partially unrolled IcySAT could successfully recover the keys for K4N3 variant of \( 4 \times 4 \) eFPGA fabric for an unroll factor of 40. Hence, a wider sweep of unroll factor is required to evaluate the security of fabrics more thoroughly.

VII. Conclusion

This study has presented some of the key characteristics and security inferences of eFPGA architecture that have to be considered while performing redaction-based logic obfuscation. The study was performed by analyzing architectural variants of an eFPGA fabric by varying two parameters of an eFPGA: \( K \) and \( N \) which signifies the size and number of LUTs in the fabric. This gave several inferences on how security parameters relate to architectural parameters. We framed an SAT-based security framework to recover the bitstream of FPGA that used the state-of-the-art IcySAT attack algorithm [13] in the backend. We experimentally concluded that security offered by an eFPGA fabric is primarily sourced from the SAT hardness of LUTs and the cyclic routing networks within the fabric. In contradiction to the assumptions from earlier work which stated that security was directly related to fabric size, we proved that in addition to fabric size, the attack complexity depends upon unroll factor, a parameter of the IcySAT algorithm. We further showed that the primary contribution to an increasing unrolling factor is sourced from the complexity of global routing. We improvised the attack models to verify that existing attack parameters like unroll factor might not reflect the actual security strength of the process. Experiments showed that in most cases in \( 4 \times 4 \) and \( 5 \times 5 \) eFPGA fabrics, the adversary could recover the bitstream with an unroll factor of 7%–36% of the ideal unroll factor. Furthermore, we experimentally disproved the assumption that bitstream size or size of any of its component is directly correlated with the security strength. We finally demonstrated how security strength might not strictly increase in proportion to physical parameters like area.

Given that choice of fabric depends on circumstances, we cannot conclude that there is a single “good” or “best” fabric for redaction. Bigger fabrics do not necessarily imply more SAT resilience; one can achieve a comparable level of security with a similar overhead. If a designer needs to consider overhead, our results point to a need for redesigning to balance overheads and security.

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