Reducing DC-Link Current Harmonics in Dual-Inverter Fed Induction Motor with Lower-Voltage Rating Inverter

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This letter proposes a control method to reduce the high-order harmonics caused by pulse-width modulation (PWM) in the DC-link current in a dual inverter with a floating capacitor topology, which has the same voltage ratings in two inverters. The proposed control method reduces the high-order harmonic current through a six-step operation at the primary inverter. The secondary inverter supplies a sinusoidal voltage to the motor using a low-rated voltage. The validity of the proposed control method is confirmed through an experiment using an open-end winding induction motor. Furthermore, the floating capacitor voltage dependencies of the input current harmonics are analyzed.

Keywords: Open-end winding, voltage rating, dual-inverter, floating capacitor, DC-link current harmonics.

1. Introduction

Recently, in terms of lifetime and efficiency of the motor drive system, a harmonic reduction method focused on a DC-link current is proposed (1)(2). A dual inverter with a floating capacitor topology, which consists of two voltage source inverters (VSIs) and an open-end winding (OEW) motor, have been researched to reduce the harmonics of the DC-link current and buffer capacitor (2). In (2), the reduction of the capacitance of the floating capacitor and switching frequency component of the DC-link current can be achieved by operating the primary side VSI in 6-step. However, a voltage rating of the secondary side VSI is double or more than that of the primary side VSI. In addition, low order harmonics of DC-link current was not investigated well. In this letter, a control method to reduce the high order harmonics of the DC-link current with lower voltage rating at the secondary side VSI is proposed.

2. Circuit Configuration and Control Strategy

A circuit configuration is shown in Fig. 1 (a); The system consists of two 2-level VSIs and an OEW induction motor (IM), in which primary side VSI (INV. 1) having a DC power supply and secondary side VSI (INV. 2) having a floating capacitor are connected to opposite terminals of the OEWIM. Hence, the voltage difference between INV. 1 \( V_1 \) and INV. 2 \( V_2 \) is supplied to the motor winding as follows:

\[ V_m = V_1 - V_2 \]  

(1)

In the floating capacitor topology, INV. 2 has no power supply thus \( V_2 \) lags or leads the motor current \( I_m \). Conventionally, \( V_{dc1} \) is larger than \( V_{dc2} \) because \( V_2 \) lags \( I_m \) to increase the compensation power (see Fig. 1 (b)). In the proposed method, by applying the phase angle of INV. 1 \( \theta_1 \) achieving the vector relation as \( V_2 \) leads \( I_m \) (shown as Fig. 1 (c)), the reduction of the floating capacitor voltage compared with the conventional method is achieved. In addition, by switching INV. 1 6 times in a fundamental period (6-step operation), the harmonics of the carrier frequency component is reduced.

In the dual inverter with floating capacitor topology, DC-link voltage ratio is expressed as follows:

\[ \frac{V_{dc2}}{V_{dc1}} = \frac{M_1 \cos(\alpha + \delta)}{M_2 \cos \delta} \]  

(2)

where, \( M_1 \) is fixed at \( 4/\pi \) in 6-step operation thus the voltage ratio depends on \( \delta, \alpha \), and \( M_2 \). Here, \( \delta \) and \( \alpha \) denote the motor power factor angle (PFA) and the phase angle difference (PAD) between \( V_1 \) and \( V_2 \) respectively. Because an active power is supplied by INV. 1 in the floating capacitor topology, PAD \( \alpha \) is given by:

\[ \alpha = \sin^{-1}\left(\frac{V_m}{|V_1|} \cos \delta\right) \]  

(3)

This equation indicates that PAD only depends on the load condition and INV. 1 setting (3).

Fig. 2 shows a control block diagram and an experimental setup of this proposal, which is based on a control strategy of the reduction of the output voltage harmonics in the dual inverter system (4). In the proposed control method, INV. 1 operates in 6-step thus the INV. 1 voltage reference \( V_{1-ref} \) is defined as:

\[ V_{1-ref} = \frac{V_{dc1}}{2} \frac{\text{sign}(\cos(\omega t + \theta_1))}{\text{sign}(\cos(\omega t - \frac{2\pi}{3} + \theta_1))} \left| \frac{\text{sign}(\cos(\omega t + \frac{2\pi}{3} + \theta_1))}{\text{sign}(\cos(\omega t + \frac{2\pi}{3} + \theta_1))} \right| \]  

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and phase, when the floating capacitor voltage is regulated less than the INV.1 DC-link voltage and the motor phase current changes from 330 V to 210 V, according to (2).

Harmonic components, the low order harmonics when the carrier frequency is 5 kHz to 35 kHz are calculated according to (2). Finally, INV.2 outputs the compensation voltage to supply a sinusoidal voltage in the motor, where discontinuous pulse width modulation (DPWM), which can maximize the modulation index and reduce the number of switching by injecting the zero-sequence component into the sinusoidal reference, is used as modulation method in INV.2.

3. Experimental Results

A general-purpose induction motor (TFO-FK 0.75KW 4P 200V) is used for experiment. In this experiment, a DC power supply regulates the INV.1 DC-link link voltage at 300 V. The OEWIM is controlled at rated speed (50 Hz) and 0.5 Nm (approximately 0.1 p.u. of rated torque). To obtain the characteristic of the DC-link current harmonics, the floating capacitor voltage reference \( V_{dc2} \) is changed from 330 V to 210 V, according to (2).

Fig. 3 shows experimental waveforms of the proposed method when the floating capacitor voltage is regulated at (a) 300 V and (b) 240 V; The results indicate that the floating capacitor voltage is regulated less than the INV.1 DC-link voltage and the motor phase current control is achieved even if \( V_{dc2} \) is changed.

Fig. 4 shows results of the harmonic analysis of the INV.1 DC-link current, which are separated into low order region (300 Hz to 2100 Hz) and high order region (5 kHz to 35 kHz); Comparing each harmonic components, the low order harmonics when \( V_{dc2} = 300 \) V are smaller than that when \( V_{dc2} = 240 \) V; On the other hand, the high order harmonics when \( V_{dc2} = 300 \) V decrease compared with that when \( V_{dc2} = 240 \) V.

Fig. 5 shows a floating capacitor voltage dependency of the INV.1 DC-link current harmonics, which are obtained by sum of each component separated into low order and high order harmonics; The results show that high order harmonics of DC-link current decreases as the floating capacitor voltage decreasing due to the switching ripple in the phase current decreases; On the other hand, the low order harmonics slightly increase as the floating capacitor voltage decreasing.

4. Conclusions

In this letter, a control method that reduces the floating capacitor voltage for low voltage ratings of the switching devices and capacitor in the dual inverter fed OEWIM was proposed and was experimentally demonstrated. The floating capacitor voltage dependency of the input DC-link current was analyzed separately for low order and high order harmonics in this experiment. This result will be useful when selecting DC capacitors and batteries.

References

(1) Z. Huang, T. Yang, P. Giangrande, S. Chowdhury, M. Galea and P. Wheeler, "An Active Modulation Scheme to Boost Voltage Utilization of the Dual Converter With a Floating Bridge," IEEE Transactions on Industrial Electronics, Vol. 66, No. 7, pp. 5623-5633 (2019)

(2) Ren Okumura and Hitoshi Haga, "Reduction of Input Current Harmonics Using Dual Inverter for Motor Drive", IEEJ Journal of Industry Applications, Vol. 10, No. 3, pp. 348-356 (2021)

(3) A. Mizukoshi and H. Haga, "Reduction of Voltage Harmonics in an Open-End Winding Induction Motor Driven by a Dual-Inverter with Floating-Capacitor in the Low-Speed Region," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 2656-2661 (2020).