Voltage Balancing Control of Cascaded Single-Phase VIENNA Converter Based on One Cycle Control With Unbalanced Loads

CONG WANG, HAOYU HU, HONG CHENG, ZHIHAO ZHAO, AND JINQI LIU

School of Mechanical, Electronic and Information Engineering, China University of Mining and Technology, Beijing 100083, China

Corresponding author: Haoyu Hu (hh_hu@foxmail.com)

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ABSTRACT A research study on a type of cascaded single-phase VIENNA converter (CSVC) is presented in this paper. And a type of DC voltage balancing control strategy for each cascaded module of the CSVC based on improved one-cycle control (I-OCC) is proposed, in which voltage balancing signals are added to the conventional OCC (C-OCC) control loop to cause a difference in the modulation signals of each of the cascaded modules, so that the DC voltages of all modules can be quickly balanced under unbalanced loads. At the same time, the average modulation wave maintains a constant value so that the CSVC achieves a unity power factor operation. The operating principle of the I-OCC strategy is discussed in detail, and the corresponding mathematical relationships are derived. In the proposed strategy, the ability to adjust the DC voltages is also analyzed. Finally, the simulation and experiment results are provided to verify the validity and feasibility of this I-OCC-based voltage balancing control strategy. The control strategy proposed by this paper is also applicable to all other cascaded unidirectional rectifiers.

INDEX TERMS Cascaded single-phase VIENNA converter (CSVC), multilevel converter, unbalanced loads, one cycle control (OCC), voltage balancing control.

I. INTRODUCTION

Line-frequency transformerless cascaded multilevel converters (TCMCs) have attracted significant attention in recent years owing to their potential for use in applications such as the next generation medium voltage power conversion system for adjustable AC speed drives or in constructing an advanced grid interface for renewable energy-based distributed generation systems [1]–[8]. By employing a cascaded H-bridge rectifier (CHB) as the front stage, the TCMC can be connected directly to the medium/high voltage power grid without involving a bulky and expensive line-frequency transformer, which is usually used by conventional multilevel converters [9], [10]. However, the CHB in TCMCs requires a large number of fully controlled power switches that render the converter more complicated during control, gate driving and protection circuits. This eventually reduces the system reliability and increases the implementation costs [11].

However, in many industrial applications, such as AC speed regulation with pumps or fans, switching power supplies for telecommunications and electric vehicle (EV) battery chargers for level I, bidirectional power flow is not required [12], [13]. In these applications, unidirectional power converters are usually the preferred choices due to advantages of simple control and fewer fully controlled power switch requirements. In [14], a cascaded single-phase bridgeless rectifier (CBR) is proposed, which contains 2 fully controlled switching devices in each module. In [15], a cascaded single-phase diode H-bridge rectifier (CDHR) is proposed, which contains only 1 fully controlled switching devices in each module. In the two unidirectional cascaded rectifiers, the complexity of the control and the cost of the system are both greatly reduced. However, in each module of the above two unidirectional topologies, the switching devices are required to withstand the whole DC side voltage. In this paper, a type of cascaded single-phase VIENNA converter (CSVC) is proposed as shown in Fig. 1, in which each module adopts one switching device and each device
In [30], an algorithm combining field of OCC, individual PI controller for each cell is used to order of DC voltages, which is another type of category. In the achieved by changing the modulation wave according to the a type of category. In [28], the balance of the DC voltage is controller and the PLL is needed in the algorithm, which is cell [24]. In [25]–[27], each module contains a voltage converters [17]–[20]. When OCC is used in boost-type PWM in controlling single-phase and three-phase alternating current/direct current (AC/DC) pulse-width modulation (PWM) rectifiers, the input current is automatically forced to be in conversion wave of each module is adjusted separately, while the average modulation wave always maintains a constant value determined by the load power. In this way, the duty ratio of the different modules can be adjusted by the different values, so that, the DC voltage of each module with various loads can be quickly balanced. Moreover, all the other abovementioned advantages exhibited by the C-OCC scheme are also retained by the I-OCC scheme. I-OCC has a certain increase in the amount of calculation due to the addition of the voltage balancing part, but it does not cause a large computational burden. For such calculations, such as voltage sequencing, mainstream DSP can be fully competent. In addition, I-OCC can be applied not only to CSVC, but also to other cascaded topologies with unidirectional power flow such as CBR, CDHR.

This paper is organized as follows. In Section II, the core equation of C-OCC applied to the CSVC is derived. Furthermore, the strategy diagram and the PWM modulation diagram of the C-OCC are explained in detail. The principle of voltage regulation on the DC side of the CSVC is briefly illustrated at the end of this section. In Section III, the undistorted condition of the grid side AC current of the CSVC is presented. Based on this condition, the I-OCC is proposed and described in detail. The adjustment ability of this strategy is also discussed. Sections IV and V verify the static and dynamic performance of the proposed I-OCC based on the simulation and experiment results. Finally, Section VI summarizes the conclusions.

II. BASIC PRINCIPLES OF THE CSVC

A. C-OCC FOR CSVC

Applying Kirchhoff’s voltage law (KVL) to the switching-cycle average model for the single-phase VIENNA converter shown in Fig. 2 yields:

$$\tilde{u}_{ab} = \tilde{u}_s - j\omega L \cdot \tilde{i}_L$$

(1)

where $L$ is the input inductor, $i_L$ is the current of $L$, $u_s$ is the grid AC voltage, $\omega$ is the angular frequency of $u_s$, $u_{ab}$ is the voltage between point a and point b, $\tilde{u}_s$, $\tilde{u}_{ab}$ and $\tilde{i}_L$ are the phasors of $u_s$, $u_{ab}$ and $i_L$, respectively. Considering high-power applications, the value of $L$ is very small. Moreover, in a 50 Hz or 60 Hz power grid, the voltage of $L$ ($j\omega L \cdot \tilde{i}_L$) is also very small relative to the grid AC voltage, and thus can be ignored. Equation (1) can be simplified to:

$$u_{ab} = u_s.$$  

(2)
In a single-phase VIENNA converter, the average voltage of $u_{ab}$ in each switching cycle can be written as:

$$u_{ab} = \begin{cases} (1 - d) \cdot \frac{E}{2}, & i_L \geq 0 \\ -(1 - d) \cdot \frac{E}{2}, & i_L < 0 \end{cases}$$

(3)

where $E$ is the output DC voltage of the single-phase VIENNA converter and $d$ is the duty cycle of the switching device $S$ [31]. Equation (3) can be simplified as:

$$u_{ab} = (1 - d) \cdot \frac{E}{2} \cdot \text{sign}(i_L)$$

(4)

where $\text{sign}(i_L)$ is a sign function that represents the sign of inductor current $i_L$:

$$\text{sign}(i_L) = \begin{cases} 1, & i_L \geq 0 \\ -1, & i_L < 0 \end{cases}$$

(5)

Substituting (4) into (2) yields:

$$(1 - d) \cdot \text{sign}(i_L) = \frac{2}{E} \cdot u_s$$

(6)

Considering unity power factor condition, the relationship of $u_s$ and $i_L$ can be expressed as:

$$u_s = R_e \cdot i_L$$

(7)

where $R_e$ is the equivalent resistance of the single-phase VIENNA converter. Combining (6) and (7) gives:

$$V_m \cdot (1 - d) \cdot \text{sign}(i_L) = R_s \cdot i_L$$

(8)

where $R_s$ is the sampling resistance of inductor current $i_L$ and $V_m$ is the output value of proportional integral (PI) controller of the output DC voltage in a single-phase VIENNA converter. $V_m$ can be given by:

$$V_m = \frac{E \cdot R_s}{2 \cdot R_e}$$

(9)

Fig.2 indicates that the grid AC current $i_s$ and the input inductor current $i_L$ are the same current:

$$\begin{align*}
  i_s &= i_L \\
  \frac{i_L}{\text{sign}(i_L)} &= |i_L|
\end{align*}$$

(10)

Applying (10) to (8) yields:

$$V_m \cdot (1 - d) = R_s \cdot |i_s|$$

(11)

Equation (11) is the core control equation of the C-OCC for single-phase VIENNA converter. To make the above equations applicable for CSVC, some symbols are redefined, where $E$ is the total output DC voltage of the CSVC and $R_e$ is the total equivalent resistance of the CSVC.
A phase-shift PWM technique is applied to C-OCC for the CSVC to generate multilevel waves (2N + 1 types). This technique uses N PWM waves with uniformly-spaced phase differences (π/N) to control the switching devices of N cascaded modules in a CSVC.

### B. THE PRINCIPLE OF REGULATION OUTPUT DC VOLTAGE OF CSVC

The N cascaded modules of the CSVC are relatively independent shown in Fig.1. Thus, the principle of regulating the output DC voltage can be separately analyzed through a CSVC module. Referring to Fig.4, when the carrier wave is higher than the modulation wave, the signal of the PWM outputs 1 (high) and the switching device of the corresponding module is in the on state. Therefore, the voltage between point a and point b of the AC input terminal is equipotential and no power flows past the module. The power of the corresponding DC load R is supplied with support capacitors C1 and C2. Thus, the output DC voltage of the module decreases. In contrast, when the carrier wave is lower than the modulation wave, the signal of the PWM outputs 0 (low), and the switching device is in the off state. Therefore, the power of R, C1 and C2 are supplied by the AC grid (when the grid AC current is positive, C1 is charged, otherwise C2 is charged). Thus, the output DC voltage of the module increases.

Therefore, when the value of the modulation wave in each carrier period is increased, the time when the carrier wave is higher than the modulation wave is reduced. Therefore, the time at which the output DC voltage falls decreases. Correspondingly, the time when the carrier wave is lower than the modulation wave is increased. In addition, the time at which the output DC voltage rises increases, the output DC voltage rises to a new steady state value as a whole. In contrast, when the value of the modulation wave in each carrier period is decreased, the output DC voltage decreases to a new steady state value.

According to the actual situation, different modulation waves are used for each single-phase VIENNA module, so that the DC side output voltage of each VIENNA module in the CSVC can be individually controlled. In C-OCC, in addition to a PI controller in the carrier wave part, each module has one to balance the DC voltage, which contains N + 1 PI controllers.

### III. VOLTAGE BALANCING CONTROL STRATEGY BASED ON I-OCC UNDER UNBALANCED LOADS

#### A. UNDISTORTED CONDITION OF THE GRID SIDE AC CURRENT OF CSVC

Section II-B shows that the CSVC can individually control the DC side output voltage of each module by using different modulation waves, which indicates that the CSVC has the ability to balance the DC side output voltages under unbalanced loads. However, while balancing voltages, it must be ensured that the grid side AC current is undistorted.

The modulation wave of the nth VIENNA module is expressed as |Rsi|n, n = 1, 2, · · · , N. Thus, the average modulation wave of each VIENNA module in the CSVC is:

\[
|R_{s|\text{average}}| = \left|\frac{R_{s|n}}{1 + \cdots + |R_{s|n}|} N\right| N
\]

As shown in Fig. 4, in C-OCC, the modulation wave of each VIENNA module in the CSVC is |Rsi|, hence:

\[
|R_{s|\text{average}}| = |R_{s}|1
\]

The I-OCC proposed in this paper adjusts the modulation waves of the VIENNA modules so that they are not always equal |Rsi|. Moreover, the modulation waves must satisfy (13), which ensures that the CSVC still satisfies (11) and guarantees that the grid side AC current is undistorted.

#### B. I-OCC STRATEGY

If there is no voltage balancing control part, when the loads of the CSVC are unbalanced, the DC side output voltages will also be unbalanced. Under the control of the total DC side output voltage PI regulator (in the carrier wave part), the total DC side output voltage of the CSVC remains constant. Therefore, it is assumed that when the DC side output voltage of a VIENNA module is lower than the rated value, there must be another module whose DC voltage is higher than the rated value. In this way, the two VIENNA modules form a control group. In the control group, the higher DC voltage of a module needs to be reduced, and the other one needs to be increased.

![Modulation method of I-OCC diagram.](image)

The modulation waves of the two VIENNA modules in a control group is shown in Fig.5. In addition, |Rsi|pk is the peak value of |Rsi|. For the convenience of discussion, a ratio M is defined as:

\[
M = \frac{|R_{s|pk}|}{V_m}
\]

According to M, the modulation method can be divided into two cases: At 0.5 < M ≤ 1, as shown in (a) and (b) of Fig. 5, the module with a lower DC side output voltage is modulated by the modulation wave |Rsi|max. As seen
from Section II-B, the value of the modulation wave in each carrier cycle is increased, thereby increasing the DC side output voltage. Similarly, the module with a higher DC output voltage uses the modulation wave \(|R_s i_s|_{\text{max}}\) to reduce the voltage. At \(0 < M \leq 0.5\), the modulation waves used in the control group are \(|R_s i_s|_{\text{max}}\) in (c) and \(|R_s i_s|_{\text{min}}\) in (d) of Fig. 5. There are two reasons for using this modulation method:

1) The modulation process must satisfy the undistorted condition of the grid side AC current of the CSVC (III-A). The average value of \(|R_s i_s|_{\text{max}}\) and \(|R_s i_s|_{\text{min}}\) is \(|R_s i_s|\), so the condition is satisfied.

2) To balance the DC side output voltage as quickly as possible, the modulation wave is selected as the limit value under undistorted condition. For instance, at \(0.5 < M \leq 1\) and in the time range \(0 \sim \omega t_1\), if \(|R_s i_s|_{\text{max}}\) is increased by a certain amount and \(|R_s i_s|_{\text{min}}\) has reached the minimum. Thus, the average value of \(|R_s i_s|_{\text{max}}\) and \(|R_s i_s|_{\text{min}}\) will be greater than \(|R_s i_s|\), and distortion of \(i_s\) will occur.

In detail, in (a) and (b) of Fig. 5, at \(0 \leq \omega t < \omega t_1\) and \(\omega t_2 \leq \omega t \leq \pi\), \(|R_s i_s|_{\text{min}} = 0\), this means that the module with voltage drop has no energy input. For the topology with unidirectional energy flow, since energy cannot be fed back, the input without energy is the fastest way to reduce the voltage. Similarly, at \(\omega t_1 \leq \omega t < \omega t_2\), \(|R_s i_s|_{\text{max}} = 1\), this shows that the module is maximizing the input of energy, and the voltage is increased to the maximum speed. At this time, \(|R_s i_s|_{\text{min}} \neq 0\) and has a little energy input, which is to satisfy the formula (13) to achieve one-cycle control while adjusting the DC voltages.

There are \(N\) VIENNA modules in the CSVC. When \(N\) is even, \(N/2\) control groups are formed. When \(N\) is odd, \((N−1)/2\) control groups and a separate VIENNA module are formed. The modulation wave used by this separate module is \(|R_s i_s|\). From the above analysis, the average modulation wave of each control group is \(|R_s i_s|\), then:

\[
\left(\frac{N-1}{2}\right) \cdot |R_s i_s| \cdot 2 + |R_s i_s|/N = |R_s i_s| \tag{15}
\]

Equation (15) shows that under the condition that \(N\) is odd, the I-OCC strategy still satisfies the undistortion condition.

The control groups are allocated, as shown in Fig. 6. When \(U_1, U_2, \ldots, U_N\) and \(U_N\) are the instantaneous values of the DC side output voltages of each module and \(U_{\text{max}}, \ldots, U_{\text{mid}}, \ldots, U_{\text{min}}\) are the voltages of the DC side after sorting, obviously \(U_{\text{max}} \geq \cdots \geq U_{\text{mid}} \geq \cdots \geq U_{\text{min}}\). The voltage adjustment amount is defined as the difference between the instantaneous voltage value and its rated value. To make the voltage adjustment amount of the two VIENNA modules in one control group close to each other, the VIENNA module with the highest voltage and the lowest voltage is combined into one control group, the VIENNA modules with the second highest voltage and the second lowest voltage form a control group, and so on. If \(N\) is odd, the VIENNA module corresponding to \(U_{\text{mid}}\) is independently controlled.

Based on the above discussion, the I-OCC diagram for the CSVC is shown in Fig. 7. Compared with the C-OCC, the carrier wave part, the carrier phase shifting part and the VIENNA module switching part of the I-OCC are still maintained. The difference is that the voltage balancing control part is added, and the number of modulation waves is also increased to \(N\) to separately control of the \(N\) VIENNA modules in the CSVC. It should be noted that I-OCC has only one necessary total DC side output voltage PI regulator, but C-OCC has \(N + 1\) PI regulators. The steps of I-OCC are summarized as follows:

1) Sort of DC side output voltages of the VIENNA modules in the CSVC in real time.
2) Distribute the control group, as shown in Fig. 6.
3) Produce the modulation wave in the control group, as shown in Fig. 5, and calculate the modulation amount \(\Delta |R_s i_s|\) of the modulation wave according to (16):

\[
\Delta |R_s i_s| = \begin{cases} 
V_m - |R_s i_s|, & M > 0.5 \text{ and } \omega t_1 \leq \omega t < \omega t_2 \\
|R_s i_s|, & \text{other conditions.}
\end{cases} \tag{16}
\]
4) Finally, the modulation waves of I-OCC are obtained by subtracting (higher DC side output voltage of all control groups) or adding (lower DC side output voltage of all control groups) \( |R_s i_s| \) on the basis of \( |R_s i_s| \).

\[
|R_s i_s| n = |R_s i_s| \pm \Delta |R_s i_s|
\]

(17)

When \( N \) is odd, the modulation wave of the DC side output voltage sorted in the middle is \( |R_s i_s| \).

C. ADJUSTMENT ABILITY ANALYSIS

In the following, the adjustment ability of the I-OCC is analyzed when the loads are unbalanced. Under I-OCC, the CSVC satisfies (11) and operates at a unity power factor:

\[
\begin{align*}
R_e &= \frac{u_s}{i_s} = \frac{u_s}{i_s} = \frac{U_s}{I_s} \\
P_{in} &= U_s \cdot I_s 
\end{align*}
\]

(18)

where \( U_s \) and \( I_s \) are the root mean square (RMS) values of the grid side AC voltage and current of the CSVC, respectively, and \( P_{in} \) is the input power of the CSVC.

According to (18):

\[
Re = \frac{U_s^2}{P_{in}}
\]

(19)

Substitute (19) into (9):

\[
V_m = \frac{E \cdot R_s}{2U_s} \cdot P_{in}
\]

(20)

The peak value of AC side current of the CSVC is:

\[
|i_{pk}| = \sqrt{2}I_s = \frac{\sqrt{2}}{U_s} \cdot P_{in}
\]

(21)

Combining (20), (21) and (14) yields:

\[
\frac{|R_{lis}|}{V_m} = \frac{2\sqrt{2}U_s}{E} = M
\]

(22)

It is known from (22) that in a given system, \( U_s \), \( E \), and \( R_s \) are determined, so the ratio \( M \) is a constant value regardless of the DC loads. The ratio of \( |R_{lis}| / V_m \) and \( V_m \) is constant.

The adjustment of the DC side output voltage of the CSVC is essentially the redistribution of the output power. Since the RMS of the grid side AC voltage is constant, the magnitude of the RMS value of the grid side AC current can reflect the level of the power by the second equation in (18). From Section II-A, \( |R_s i_s| \) is the average modulation wave in one period and \( R_s I_s \) is the RMS of \( |R_s i_s| \). Additionally, \( R_s \) is determined, and \( R_s I_s \) can also reflect the level of the power.

At \( 0.5 < M \leq 1 \), as shown in Fig.5 (a) and (b), the RMS values of \( |R_s i_s| \) max and \( |R_s i_s| \) min reflect the limit value of the output power in the control group. The maximum regulated power ratio \( Pr_{max} \) is defined as (23), shown at the bottom of this page.

Based on the definition of the RMS, \( RMS (|R_s i_s|) \) max and \( RMS (|R_s i_s|) \) min are calculated by using (24) and (25), as shown at the bottom of this page, respectively. It can be seen that \( R_s I_s \) is eliminated by the mathematical relationship in \( Pr_{max} \) and \( wt_1 \) is actually a function of \( M \):

\[
wt_1 = \arcsin \left( \frac{1}{2M} \right)
\]

(26)

Thus, \( Pr_{max} \) is uniquely determined by \( M \). When the ratio of the output power of two VIENNA modules in a control group is higher than the maximum regulated power ratio \( Pr_{max} \), I-OCC will exceed the adjustment ability. Taking Fig. 8 as an example, in a given CSVC system, the maximum power ratio plane is calculated according to (23). \( R_a \) and \( R_b \)
FIGURE 8. Max power ratio diagram with I-OCC under unbalanced loads condition.

are the DC loads of two VIENNA modules in one control group. Under the control of I-OCC, the DC voltages are balanced, so the magnitude of the DC loads reflects the output power of the VIENNA module, and the actual output power ratio can be calculated. Below the maximum power ratio plane, the actual output power ratio is lower than \( P_{R_{\text{max}}} \), which is the I-OCC controllable area, and the intersection line is the critical area. While above the plane, the actual output power ratio is higher than \( P_{R_{\text{max}}} \), which is the I-OCC uncontrollable area, where I-OCC loses its ability to regulate. To ensure the normal adjustment of the I-OCC, it is necessary to ensure that the actual output power ratio of the two modules in the control group is lower than \( P_{R_{\text{max}}} \), which is called the maximum power ratio condition.

At \( M < 0.5 \), as shown in Fig. 5 (c) and (d), the RMS of \( |R_i|_{\text{min}} \) is 0. Therefore, the maximum regulated power ratio \( P_{R_{\text{max}}} \) tends to infinity. In this case, the I-OCC does not have a maximum power ratio condition.

IV. SIMULATION RESULTS

To verify the correctness and effectiveness of I-OCC, simulation studies have been conducted by using Simulink. Simulation parameters are shown in Table 1.

| Parameter     | Quantity                | Values  |
|---------------|-------------------------|---------|
| \( u_x \)     | grid side input voltage | 220 V   |
| \( U_{in} \)  | rated output voltage of a module | 250 V |
| \( L \)       | number of cascaded modules | 3     |
| \( C_1, C_2 \)| input inductor           | 2.2 mH |
| \( f_{sw} \)  | DC support capacitor     | 4400 \( \mu \)F |
| \( f_{sw} \)  | switch frequency         | 20 kHz  |

Fig. 9 shows the simulation results of the CSVC with the above configuration when the balanced loads are abruptly changed to unbalanced and when the C-OCC without DC voltages balancing part is changed to I-OCC. \( R_1, R_2 \) and \( R_3 \) are defined as the DC side loads of the three VIENNA modules of the CSVC. As shown in Fig. 9 (a), at \( t = 0 \) s and \( R_1 = R_2 = R_3 = 150 \Omega \), C-OCC is applied, and the loads are balanced. At this time, due to the role of carrier phase-shift control, even if the DC side loads are in a balanced state, there are significant differences in the DC side output voltages \( U_1, U_2, \) and \( U_3 \), but they are basically balanced. At \( t = 1 \) s, the DC side loads are changed to unbalanced: \( R_1 = 100 \Omega, R_2 = 150 \Omega, \) and \( R_3 = 200 \Omega \). At this time, the output voltages are severely unbalanced. At \( t = 2 \) s, the control method is changed to I-OCC, and it can be seen that the DC side output...
voltages are quickly adjusted to reach balanced state and follow the rated voltage $U_{av}^*$. The effect of the unbalanced loads along with the carrier phase-shift control on the DC side output voltages is eliminated. Fig. 9 (b), (c) and (d) are the simulation results of the waveform of the grid side AC voltage and current, the AC side voltage simulation waveform and the grid side AC current total harmonic distortion (THD) under an unbalanced load and I-OCC control, respectively.

Fig. 9 (b) illustrates that the I-OCC satisfies the control requirements for the grid side AC voltage and current to achieve unity power factor operation. Fig. 9 (c) shows that I-OCC can generate multilevel voltages by carrier phase shifting. This figure also shows that the CSVC is a type of multilevel converter (MC). Three cascaded modules are used in this simulation, so a total of 7 levels of voltages are produced. Fig. 9 (d) shows that the I-OCC satisfies the requirement for the grid side AC current THD. In this simulation, the THD of grid side AC current is only 2.37%, and the waveform is basically a sine wave.

To further verify the dynamic characteristics of the I-OCC, the DC side loads are continually changed several times. The parameters of DC side loads are shown in Table 2 and the simulation results are shown in Fig. 10. During the adjustment process, the DC voltage of each module is dynamically changed. When the voltage changes, the voltage order also changes, and regroups to change the modulation waves. It can be seen that during the entire process, the DC side output voltages keep in balance, and only slight fluctuations occur when the simulation parameters change, which reflects the excellent dynamic performance of the I-OCC.

To verify the adjustment speed of the I-OCC to the DC side output voltages, the C-OCC with PI-based voltages balancing control part is compared, and the simulation results are shown in Fig. 11. At the same time, parameters of PI controller are selected by using Simplex Method. At $t = 0s$ and $R_1 = R_2 = R_3 = 150\Omega$, the loads are balanced, then both control methods are effective. At $t = 1s$, the DC side loads are changed to unbalanced: $R_1 = 100\Omega$, $R_2 = 150\Omega$, and $R_3 = 200\Omega$. The voltage balancing control with the PI regulator can also finally balance the voltages. However, compared with the I-OCC, it is obvious that the dynamic response is poorer, the adjustment period is longer, and the fluctuation range is larger. Under the control of I-OCC, there is only a slight fluctuation at the moment of the mutation, and the DC side output voltages are quickly adjusted to keep in balance.
V. EXPERIMENT RESULTS

A scaled-down experiment CSVC prototype with three cascaded modules is built to further verify the I-OCC performance. The parameters are shown in Table 3. Fig. 12 shows the prototype and a TMS320F28335 digital signal processor (DSP) is used to achieve the control method.

The experimental design follows the simulation. As shown in Fig. 13(a), the loads are balanced, and the C-OCC without DC voltages balancing control part is applied at the beginning. The difference between output DC voltages is due to the influence of the phase-shift PWM control. At \( t_1 \), the DC output loads are suddenly changed to unbalanced \((R_1 = R_2 = R_3 = 150\Omega \text{ at the beginning, and } R_1 = 100\Omega, R_2 = 150\Omega, R_3 = 200\Omega \text{ at } t_1)\), and the difference becomes more obvious. The DC voltages of the CSVC start to quickly adjust when the I-OCC is used at \( t_2 \). Finally, the voltages are completely balanced at \( t_3 \). Fig. 13(b) shows that unity power factor operation is achieved and the grid side input current is undistorted. As an multilevel converter, the experiment CSVC prototype with three cascaded modules has 7 types of AC side voltages, as shown in Fig. 13(c), and the THD of the grid side input current is low (2.65%), as shown in Fig. 13(d).

Subsequently, the CSVC prototype is always controlled by using I-OCC, as shown in Fig. 14. The loads are suddenly changed at \( t_1, t_2, \text{ and } t_3 \), as shown in Table 2. It can be seen that the output voltages quickly reach a balanced state when there is only a slight fluctuation in the moment of sudden load change. This behavior means that the control of I-OCC is strongly robust.

Fig. 15 shows a comparative experiment of balancing voltages between the I-OCC and C-OCC with PI-based DC voltages balancing control part. Under the same condition \((R_1 = R_2 = R_3 = 150\Omega \text{ at the beginning, and } R_1 = 100\Omega, R_2 = 150\Omega, R_3 = 200\Omega \text{ at } t_1)\), the PI-based control method spends more time balancing the voltages when the loads are changed to the unbalanced state. At the same time, the voltage fluctuation under C-OCC with PI-based DC voltages balancing control is more severe. This severity reflects the rapidity of the I-OCC control method.
I-OCC has satisfied dynamic performance. With PI-based DC voltages balancing control method and other hand, the proposed I-OCC is compared with the C-OCC correctness and effectiveness of the improved strategy. On the is also studied. Simulations and experiments verify the adjustment ability of the improved strategy adds a voltage balancing control part and expands the application capability of one-cycle control, which rapidly balances the voltages of DC loads. The two operating states classified by the ratio M of the CSVC are discussed. In addition, the adjustment ability of the improved strategy is also studied. Simulations and experiments verify the correctness and effectiveness of the improved strategy. On the other hand, the proposed I-OCC is compared with the C-OCC with PI-based DC voltages balancing control method and I-OCC has satisfied dynamic performance.

VI. CONCLUSION
This paper proposes an improved one-cycle control strategy. Based on the conventional one-cycle control, the proposed strategy adds a voltage balancing control part and expands the application capability of one-cycle control, which rapidly balances the voltages of DC loads. The two operating states classified by the ratio M of the CSVC are discussed. In addition, the adjustment ability of the improved strategy is also studied. Simulations and experiments verify the correctness and effectiveness of the improved strategy. On the other hand, the proposed I-OCC is compared with the C-OCC with PI-based DC voltages balancing control method and I-OCC has satisfied dynamic performance.

REFERENCES
[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, “Multi-level voltage-source-converter topologies for industrial medium-voltage drives,” IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, “Recent advances and industrial applications of multilevel converters,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[3] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, “Solid-state transformer and MV grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters,” IEEE Trans. Ind. Appl., vol. 51, no. 4, pp. 3343–3360, Jul. 2015.
[4] N. Chauhan and K. C. Jana, “Cascaded multilevel inverter for underground traction drives,” in Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDS), Bengaluru, India, Dec. 2012, pp. 1–5.
[5] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, “Control of modular multilevel converter with parallel connectivity—Application to battery systems,” IEEE Trans. Power Electron., vol. 32, no. 11, pp. 8381–8392, Nov. 2017.
[6] G. P. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, “Hybrid multilevel inverter with cascaded H-bridge cells for HVDC applications: Operating principle and scalability,” IEEE Trans. Power Electron., vol. 30, no. 1, pp. 65–77, Jan. 2015.
[7] H. Akagi and S. Inoue, “Medium-voltage power conversion systems in the next generation,” in Proc. CES/IEEE 5th Int. Power Electron. Motion Control Conf., Shanghai, China, Aug. 2006, pp. 1–8.
[8] A. Qi Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, and S. J. Dale, “The future renewable electric energy delivery and management (FREEDM) system: The energy Internet,” Proc. IEEE, vol. 99, no. 1, pp. 133–148, Jan. 2011.
[9] L. Tarisciotti, P. Zanchetta, A. Watson, S. Bifaretti, and J. C. Clare, “Modulated model predictive control for a seven-level cascaded H-bridge back-to-back converter,” IEEE Trans. Ind. Electron., vol. 61, no. 10, pp. 5375–5383, Oct. 2014.
[10] Y. Li, Y. Wang, and B. Q. Li, “Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 4, no. 2, pp. 589–605, Jun. 2016.
[11] M. Musavi, M. Edington, W. Eberle, and W. G. Dunford, “Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies,” IEEE Trans. Smart Grid, vol. 3, no. 1, pp. 413–421, Mar. 2012.
[12] X. Liang, N. C. Kar, and J. Liu, “Load filter design method for medium-voltage drive applications in electrical submersible pump systems,” IEEE Trans. Ind. Appl., vol. 51, no. 3, pp. 2017–2029, May 2015.
[13] M. Yilmaz and P. T. Krein, “Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles,” IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2151–2169, May 2013.
[14] C. Wang, Y. Zhuang, J. Jiao, H. Zhang, C. Wang, and H. Cheng, “Topologies and control strategies of cascaded bridgeless multilevel rectifiers,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 5, no. 1, pp. 432–444, Mar. 2017.
[15] X. Jiang, “New cascade diode H-bridge multi-level rectifier,” in Proc. 5th Int. Conf. Electr. Utility Deregulation Restructuring Power Technol. (DRPT), Changsha, China, Nov. 2015, pp. 2326–2330.
[16] K. M. Smedley and S. Cuk, “One-cycle control of switching converters,” in Proc. 22nd Annu. IEEE Power Electron. Specialists Conf. (PESC), Cambridge, MA, USA, Jul. 1991, pp. 888–896.
[17] J. T. de Carvalho Neto, A. O. Salazar, A. S. Lock, and D. A. M. Fonseca, “One cycle control for battery connected standalone photovoltaic systems for DC loads,” IEEE Latin Amer. Trans., vol. 16, no. 7, pp. 1977–1983, Jul. 2018.
[18] D. V. Ghodke, B. G. Fernandes, and K. Chatterjee, “PLL-less one cycle controlled bi-directional high power factor AC to DC converter,” in Proc. 27th IEEE Power Electron. Spec. Conf., Jeju, South Korea, Jun. 2006, pp. 1–6.
[19] E. S. Sreeraj, K. Chatterjee, and S. Bandyopadhyay, “One-cycle-controlled single-stage single-phase voltage-sensorless grid-connected PV system,” IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 1216–1224, Mar. 2013.
[20] A. A. M. Bento, P. K. F. Vieira, and E. R. C. da Silva, “Application of the one-cycle control technique to a three-phase three-level NPC rectifier,” IEEE Trans. Ind. Appl., vol. 50, no. 2, pp. 1177–1184, Mar./Apr. 2014.
[21] C. C. Chan, Z. M. Zhao, C. Qian, and S. Meng, “Comparisons of PWM and one-cycle control for power amplifier with multilevel converter,” IEEE Trans. Ind. Electron., vol. 49, no. 6, pp. 1342–1344, Dec. 2002.
[22] T. K. Jappe and S. A. Mussa, “Discrete-time one cycle control technique applied in single-phase PFC boost converter,” in Proc. IEEE Int. Symp. Ind. Electron., Gdansk, Poland, Jun. 2011, pp. 1555–1560.
[23] L. Wang, X. Han, C. Ren, Y. Yang, and P. Wang, “A modified one-cycle-control-based active power filter for harmonic compensation,” IEEE Trans. Ind. Electron., vol. 65, no. 1, pp. 738–748, Jan. 2018.
[24] W. Cong, Z. Guoeng, C. Hong, and L. Yaopu, “A novel modulation strategy based on two dimensional modulation for balancing DC-link capacitor voltages of cascaded H-bridges rectifier,” in Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Montreal, QC, Canada, Oct. 2012, pp. 116–122.
[25] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, “Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM,” IEEE Trans. Ind. Electron., vol. 55, no. 1, pp. 21–29, Jan. 2008.
[26] K. S. Alam, D. Xiao, D. Zhang, and M. F. Rahman, “Single-phase multicell AC-DC converter with optimized controller and passive filter parameters,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 297–306, Jan. 2019.

[27] W.-L. Ming and Q.-C. Zhong, “Single-phase half-bridge rectifiers with extended voltage ranges and reduced voltage ripples,” in *Proc. IEEE 5th Int. Symp. Power Electron. Distrib. Geners. Syst. (PEDG)*, Galway, Ireland, Jun. 2014, pp. 1–6.

[28] H. Iman-Eini, S. Farhangi, and J. L. Schanen, “A modular AC/DC rectifier based on cascaded H-bridge rectifier,” in *Proc. 13th Int. Power Electron. Motion Control Conf.*, Poznan, Poland, Sep. 2008, pp. 173–180.

[29] S. Ouyang, J. Liu, X. Wang, and F. Meng, “One-cycle control of a delta-connected cascade h bridge rectifier,” in *Proc. Int. Power Electron. Appl. Conf. Expo.*, Shanghai, China, Nov. 2014, pp. 870–874.

[30] H. Miao, J. Mei, J. Zheng, T. Ma, and C. Zhang, “A new MMC control strategy based on one-cycle-control and capacitor voltage balance,” in *Proc. IEEE 2nd Int. Future Energy Electron. Conf. (IFEEC)*, Taipei, Taiwan, Nov. 2015, pp. 1–5.

[31] C. Qiao and K. M. Smedley, “Three-phase unity-power-factor star-connected switch (VIENNA) rectifier with unified constant-frequency integration control,” *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 952–957, Jul. 2003.

**Cong Wang** was born in Beijing, China, in 1955. He received the B.S. degree in electrical engineering from the Taiyuan University of Technology, Taiyuan, China, in 1982, and the M.S. and Ph.D. degrees in electrical engineering from the China University of Mining and Technology, Beijing, in 1984 and 2005, respectively. From 1990 to 1991, he was a Visiting Scholar with the University of Bristol, Bristol, U.K. From 2002 to 2003, he was a Senior Visiting Scholar and a Visiting Professor with The University of Tennessee, Knoxville, TN, USA. He is currently a Professor of power electronics with the School of Mechanical Electronic and Information Engineering, China University of Mining and Technology. His current research interests include high-power multilevel converters, high-frequency soft-switching converters, and power electronics in smart grids.

**HaoYu Hu** was born in Zhangjiakou, China, in 1995. He received the B.S. degree in electrical engineering from the Hebei University of Engineering, Handan, in 2017. He is currently pursuing the M.S. degree with the School of Mechanical Electronic and Information Engineering, China University of Mining and Technology, Beijing, China. His current research interests include VIENNA converters, high-voltage converters, and vector control of the inductor motor.

**Hong Cheng** was born in Jinhua, China, in 1966. She received the B.S. degree in electrical engineering from Beihang University, Beijing, China, in 1988, and the Ph.D. degree in electrical engineering from the China University of Mining and Technology, Beijing, in 1993. She is currently a Professor of power electronics with the School of Mechanical Electronic and Information Engineering, China University of Mining and Technology. Her current research interests include high-power multilevel converters, modeling and control of switching converters, and fault diagnosis of power electronics equipment.

**ZhiHao Zhao** was born in Huainan, China, in 1994. He received the B.S. degree in electrical engineering from the Anhui University of Science and Technology, Huainan, in 2017. He is currently pursuing the M.S. degree with the School of Mechanical Electronic and Information Engineering, China University of Mining and Technology, Beijing, China. His current research interests include VIENNA converters and high-voltage converters.

**JinQi Liu** was born in Taiyuan, China, in 1993. He received the B.S. degree in electrical engineering from the Taiyuan University of Technology, Taiyuan, China, in 2016, and the M.S. degree in electrical engineering from the China University of Mining and Technology, Beijing, in 2019. He is currently pursuing the Ph.D. degree with the School of Engineering, University of Warwick, Coventry, U.K. His current research interests include energy storage hybrid grids and power system multistress optimization control.

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**Zonglin Mao** was born in Taierzhuang, China, in 1962. She received the B.S. degree in electrical engineering from China University of Mining and Technology, Beijing, China, in 1985, and the M.S. degree in electrical engineering from the China University of Mining and Technology, Beijing, in 1999. She is currently a Professor of power electronics with the School of Electrical and Information Engineering, China University of Mining and Technology. Her current research interests include high-power multilevel converters, high-frequency soft-switching converters, and power electronics in smart grids.