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[Technical Paper]

Fabrication Methodology for a Hermetic Sealing Device Using Low Temperature Intrinsic-Silicon/Glass Bonding

Kazuya Nomura*, Akiko Okada*, Shuichi Shoji*, Toshinori Ogashiwa**, and Jun Mizuno*

*Waseda University, 3-4-1 Okubo, Shinjuku, Tokyo 169-8555, Japan
**Tanaka Kikinzoku Kogyo K.K., 2-73 Shinmachi, Hiratsuka, Kanagawa 254-0076, Japan

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Abstract

We propose a novel fabrication methodology for a hermetic sealing device using an O2 plasma-assisted low temperature Intrinsic-Silicon (I-Si) and glass bonding technique. Glass substrates were used as the cap and base wafers, while I-Si was applied selectively to the contact surface of the cap wafer as an interlayer. A 180-μm-deep cavity was formed in the cap glass by wet etching using a double-layer (photoresist/I-Si) etching mask. I-Si/glass bonding was conducted at 200°C using an I-Si layer-covered glass wafer and a bare glass wafer. Water contact angle measurements and tensile test results showed that the bonding strength increased with promoting surface hydrophilicity through O2 plasma pretreatment. Moreover, scanning acoustic microscope observations revealed that I-Si/glass bonding was achieved successfully without significant voids. Our results indicate that the proposed method could become an indispensable technique for future functional hermetic sealing devices.

Keywords: Glass-to-glass Structure, Hermetic Sealing, HF Wet Etching, Intrinsic-silicon/glass Bonding, Low Temperature Bonding

1. Introduction

In recent years, hermetic sealing devices for encapsulating integrated circuits (IC) and microelectromechanical systems (MEMS) have attracted significant research attention.[1–4] In most cases, the hermetic sealing device comprises a cap wafer, a base wafer, and an encapsulated device. A cavity is formed in either of the wafers and the device is placed onto the cavity area. The wafers are bonded under vacuum or in a N2 atmosphere. Hence, the encapsulated device has a longer operating life and more improved characteristics than what is in the atmosphere.[5]

In many hermetic packaging technologies, glass has been widely used as the cap wafer owing to its mechanical sturdiness, chemical stability, and permeability to light and radio frequency (RF) power.[6–10] Moreover, glass is also employed as the base wafer because it has high electrical resistance and a low loss tangent even at high-frequency ranges.[11–15]

Recently, there has also been an interest in side-directional interconnection, which allows signal transmissions or a power supply for MEMS devices, such as microgyroscopes, accelerometers, and pressure sensors.[16] To achieve the interconnection, several bonding methods using insulating interlayers have been reported, including glass frit bonding and adhesive bonding.[17, 18] These methods can provide a very strong bonding strength exceeding 10 MPa while maintaining insulation, but their practical usage is still challenging. Glass frit bonding is generally performed at high temperatures (400–500°C), which may degrade or damage the encapsulating devices.[17] In the case of adhesive bonding, the influence of outgas from the adhesive or the invasion of moisture should be considered.[18] Therefore, in order to overcome these limitations, a novel bonding method with an appropriate insulating material is required for functional hermetic sealing devices.

In this study, we propose the use of intrinsic-silicon (I-Si) as an interlayer for hermetic sealing devices because I-Si has the following three unique features. (1) I-Si exhibits insulation property because no significant impurities such as phosphorus or boron are doped into it. (2) I-Si has a possibility of low temperature bonding by activating its surface.[19–21] (3) The deposition of I-Si is relatively sim-
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ple compared to other interlayers that need electroplating or multilayer deposition,[3, 22, 23] because it doesn’t require the wet etching process and the adhesive layer.

The concept of the hermetic sealing device is illustrated in Fig. 1. The I-Si interlayer is formed on the ring-shaped area of the cap wafer, and I-Si/glass bonding is conducted with the base glass wafer. In the following, we describe three processes involved in the fabrication of the proposed device: evaluating the insulating property of the sputtered I-Si, fabrication of the cap wafer with an I-Si interlayer, and evaluating I-Si/glass bonding.

2. experimental procedure

2.1 insulating property of sputtered I-Si

To evaluate the insulation property of I-Si, resistance measurements were obtained using a four-probe method (Grail 10-5-LV-HTV, Nagase Techno-Engineering Co., Ltd.), as shown in Fig. 2. First, 300 nm I-Si was sputtered onto a 20 × 20 mm² glass substrate (SPC350, CANON ANELVA Corp.). Next, surface silicon dioxide was removed by dry etching using Ar ion and Au electrodes were then arrayed onto the I-Si surface in the same vacuum chamber (M820, Hakuto Co., Ltd.). The diameter and pitch of the Au electrodes were 250 μm and 470 μm, respectively. The sample temperature was controlled from 25°C to 300°C based on considerations of the possible temperature at the time of I-Si/glass bonding.

2.2 fabrication of the cap wafer

Figure 3 shows the fabrication process of the cap wafer with an I-Si interlayer. We employed HF wet etching using a double-layer etching mask to prevent the HF solution from forming pinholes on the glass substrate.[24] First, 1 μm I-Si was sputtered onto both sides of the 50 × 50 mm² non-alkali glass (EN-A1, Asahi Glass Co., Ltd.) and the glass was then annealed for 60 min at 450°C in a N₂ atmosphere (RHL-P610CP, CANON ANELVA Corp.). Next, a positive photoresist (LA-900, Tokyo Ohka Kogyo Co., Ltd.) was applied to both sides of the glass, whereas the I-Si and resist were patterned only on the front side. Wet etching was then carried out with agitation for 2 h to form a cavity using the double-layer (resist/I-Si) as an etching mask. A 12.5 wt% HF solution was used as the etchant. After wet etching, the resist and I-Si were removed with acetone and dry etching (RIE-10NR, SAMCO Inc.) because the HF solution would have degraded the surface condition of the I-Si. The conditions for dry etching are listed in Table 1. Next, masking tape was cut to the size of the cavity and pasted onto the cavity area. This simple patterning method
has limitations in terms of the tape size and accurate alignment, but we considered that they would not affect the subsequent processes. Contamination that remained after removing the tape would be removed easily by ultrasonic cleaning. Finally, the aluminum tape was removed manually. The thicknesses of the cavity and ring-shaped area were measured by a digital micrometer (MH-15M, Nikon Corp.) at 25 and 24 points, respectively, as shown in Fig. 4. In addition, the surface roughness of the ring-shaped area was observed using atomic force microscopy (AFM) (SPM-9600, SHIMADZU Corp.). Table 2 lists the measurement conditions for AFM.

### 2.3 O₂ plasma pretreatment
To clarify whether I-Si/glass bonding was applicable for a hermetic sealing, a bonding evaluation was performed with a non-patterned I-Si layer-covered glass wafer and bare glass wafer. First, we investigated the effect of the O₂ plasma pretreatment on the bonding performance. Table 3 lists the O₂ plasma conditions (PL8, SUSS MicroTec AG.). Untreated wafers and 1 min O₂ plasma treated ones were prepared. Second, the water contact angles were measured using a contact angle meter LCD-400S (Kyowa Interface Science Co., LTD.) for the I-Si surface of both samples.

### 2.4 I-Si/glass bonding
After pretreatment with O₂ plasma, I-Si/glass bonding was conducted (SB6e, SUSS MicroTec AG.). Untreated wafers were also bonded for comparison. These bonding experiments were performed simply to demonstrate the superior performance of the O₂ plasma; therefore, only one sample was prepared for each plasma condition. The bonding conditions are listed in Table 4. Next, the interface between the I-Si and glass was observed using scanning acoustic microscopy (SAM) (SAM300, PVA Tepla Analytical Systems GmbH) with a 210-MHz transducer. Furthermore, a tensile test was performed using a MODEL-1307R (AIKOH ENGINEERING Co., Ltd.) at crosshead speeds of 50 mm/min to determine the strength of I-Si/glass bonding.

### 3. Results and Discussion
#### 3.1 Insulating property of sputtered I-Si
Figure 5 shows the relationship between temperature and the resistance per unit length. The resistance of I-Si decreased as the temperature increased up to a specific temperature range (200–300°C in this study). By contrast, the resistance increased above a turning point because the electrons that contributed to the formation of a covalent

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**Table 1** Condition of dry etching.

| Gas Species | SF₆ |
|-------------|-----|
| Flow Rate   | 30 sccm |
| RF Power    | 100 W |
| Vacuum      | 3.0 Pa |
| Time        | 3 min |

**Table 2** Condition of AFM measurement.

| Observation Mode | Dynamic Mode |
|------------------|--------------|
| Probe            | SSS-NCH (Nanoworld Co., Ltd.) |
| Scanning Area    | 1 μm × 1 μm |
| Scanning Speed   | 1 Hz |

**Table 3** Condition of O₂ plasma pretreatment.

| RF Power | 150 W |
|----------|-------|
| Vacuum   | 5.13 mPa |
| Time     | 1 min |

**Table 4** Condition of I-Si/glass bonding.

| Temperature | 200°C |
|-------------|-------|
| Applied Pressure | 5.0 MPa |
| Vacuum      | 0.50 Pa |
| Time        | 30 min |

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Fig. 4 Measurement points of substrate thickness.

Fig. 5 Resistance vs temperature of I-Si.
bond escaped from the chains of atoms via thermal excitation. Therefore, the electrical resistance of the I-Si decreased up to a specific temperature. However, the influence of lattice scattering becomes large at high temperatures,[25] which caused high resistance. Thus, the resistance increased as the temperature increased. Nevertheless, the resistance with I-Si was in the order of \(10^9\ \Omega/m\) for the samples measured at all temperatures. This result indicates that I-Si maintained its insulation property even after sputtering; thus, the surface-directional insulation property was confirmed. We consider that the sputtered I-Si is an appropriate insulating interlayer because it is expected to have no anisotropic resistivity on both the surface and in the depth of the sputtered I-Si layer. A sufficiency of the insulation would be evaluated when a side directional interconnection is employed.

3.2 Fabrication of the cap wafer

Figure 6 shows the thickness of the cap wafer after HF wet etching. The line numbers on the axes correspond to those in the schematic diagram shown in Fig. 6. The graph shows that there was a difference in thickness between the cavity area and ring-shaped area of more than 180 \(\mu m\). A cross-sectional scanning electron microscope (SEM) image of the point of demarcation between the ring-shaped area and the cavity area is shown in Fig. 7, which demonstrates that the cavity was formed successfully using a double-layer etching mask and with agitation of the etchant solution.

Figure 8 shows a photograph of the fabricated cap wafer, which indicates that the cavity was formed without decreasing the permeability. These results indicate that the employed etching process was useful for patterning a 100-\(\mu m\)-scale cavity structure in the glass substrate. Figure 9 shows the AFM measurements based on observations of the ring-shaped area of the I-Si. In the ring-shaped area, the average root mean square value of the surface roughness was 0.36 nm. This means that the ring-shaped area was protected by the double-layer mask during HF wet etching, and thus a smooth I-Si surface was obtained after sputtering.

3.3 O2 plasma pretreatment and I-Si/glass bonding

Figures 10(a) and 10(b) show the water contact angles on the I-Si layer, which covered a glass wafer, before and after the O2 plasma pretreatment. It can be seen that the contact angle decreased dramatically from 87.4° to less than 5°. This result leads to our presumption that hydroxyl groups were generated by the O2 plasma pretreatment. The reason of this consideration is that an oxide group was
generated on the sputtered Si surface by the O$_2$ plasma. Next, the dangling bonds of the oxide group were bonded to hydrogen when they were exposed to the atmosphere and they formed the hydroxyl group.[26]

Figure 11 shows a SAM image of the I-Si/glass interface at the bonded area. I-Si/glass bonding was mostly carried out. Some small voids caused by contaminations would be removed by improving the environmental conditions. Furthermore, as shown in Fig. 12, the tensile strength of the bonded sample after the O$_2$ plasma pretreatment reached 0.19 MPa, whereas the bonded sample with no plasma pretreatment broke away before evaluation. These results suggest that Si-O-Si bonds were formed during the bonding of wafers, which had hydroxyl groups on their surfaces. In this way, we found out that the generation of hydroxyl groups on the bonded surface by O$_2$ plasma is the most important factor of I-Si/glass bonding. Moreover, it is assumed that a greater bonding strength would be obtained by improving the thickness distribution of the sputtered I-Si. We conclude that I-Si/glass bonding is applicable for the hermetic sealing of IC and MEMS devices.

4. Conclusion

In this study, we reported a novel fabrication methodology for a hermetic sealing device using O$_2$ plasma-assisted low temperature bonding technique of I-Si and glass. The findings of this study are summarized as follows.

1. Resistance measurements showed that I-Si maintained its insulation property even after sputtering.
2. A cap wafer with a 180-μm-deep cavity structure was fabricated successfully, and a smooth I-Si interlayer was formed only on the bonding interface of the cap wafer.
3. I-Si/glass bonding was achieved at 200°C using the O$_2$ plasma pretreatment.

Based on the obtained results, we consider that the proposed fabrication methodology will open a new possibility for a novel hermetic sealing device. We plan to carry out I-Si/glass bonding using the fabricated cap wafer and bare glass wafer, and evaluate the hermeticity of the proposed device. Furthermore, the insulation property of the I-Si interlayer with a side-directional interconnection will be evaluated in our future research.

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Kazuya Nomura was born in Kanagawa Prefecture, Japan, in 1992. He received his BS degree in the field of microsystems from Waseda University in 2015. He is presently Master’s course student at Waseda University. His current interests are MEMS packaging and hermetic sealing.

Akiko Okada was born in Saitama Prefecture, Japan, in 1988. She received her BS and MS degree in the field of microsystems from Waseda University in 2012 and 2014, respectively. She is presently Ph.D. student at Waseda University. Her current research interest is nano fabrication for GaN-based semiconductor devices.

Shuichi Shoji received his Ph.D. degree in electronic engineering from Tohoku University in 1984. He had been a research associate and associate professor at Tohoku University from 1984 to 1992. In 1994, he moved to Waseda University as an associate professor, and he is currently a professor of Department of Electronic and Photonic Systems and Department of Nanoscience and Nanoengineering, Waseda University. His current interests are micro-/nano-devices and systems for chemical/bio applications.

Toshinori Ogashiwa received B.E. and M.E. degrees from Mining College of Akita University in 1982 and 1984, respectively, and Dr.E. degree from Tohoku University in 1994. He has joined Tanaka Kikinzoku Kogyo since 1984, and is a project leader at Technical Division. His research interests include low-temperature bonding technology for electronic devices.

Jun Mizuno received his Ph.D. degree in applied physics from Tohoku University in 2000. He is currently a professor at Waseda University and works at Research Organization for Nano and Life Innovation where is a research institute of nano-science and engineering. His current interests are MEMS-NEMS technology, low temperature bonding technology using plasma activation or excimer laser irradiation, printed electronics, and composite technology for UV or heat nanoimprint lithography combined with electrodeposition.