Enhancement-mode buried strained silicon channel quantum dot with tunable lateral geometry

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We propose and demonstrate a relaxed-SiGe/strained-Si (SiGe/s-Si) enhancement-mode gate stack for quantum dots. The enhancement-mode SiGe/s-Si structure is pursued because it spaces the quantum dot away from charge and spin defect rich dielectric interfaces and minimizes background dopants. A mobility of $1.6 \times 10^5$ cm$^2$/Vs at $5.8 \times 10^{12}$/cm$^2$ is measured in a double-top-gated lateral quantum dot nanostructure. The CB terminates with open diamonds up to $\pm 10$ mV of DC voltage across the device. The devices were fabricated within a 150 mm Si foundry setting that uses implanted ohmics and chemical-vapor-deposited dielectrics, in contrast to previously demonstrated enhancement-mode SiGe/s-Si structures made with AuSb alloyed ohmics and atomic-layer-deposited dielectric. A modified implant, polysilicon formation and annealing conditions were utilized to minimize the thermal budget so that the buried s-Si layer would not be washed out by Ge/Si interdiffusion.

Control over single electrons, their spin and controlled coupling between electrons have reached exquisite levels in model semiconductor systems such as GaAs [1, 2]. The historical success of semiconductors for computation combined with demonstrations of the necessary electronic control of electron spins to do coherent manipulations of the spin state offers the promise that quantum dots might be used for quantum computation.

There continues to be considerable interest in translating the GaAs results into Si, because of the promise that very long spin decoherence times may be achieved [3, 4]. Significant progress in Si has recently been reported, particularly with single spin manipulation [5-8]. However, the long-term chance for success in Si, as well as near-term efforts to move towards controlling more spins coherently (e.g., double dots), will benefit greatly from both as smooth a disorder potential as possible, and minimal inhomogeneity in the local magnetic field.

Common sources of unintentional charges and spins include interface states at semiconductor/dielectric interfaces and background dopants [4, 9]. Common choices for Si quantum dot structures either rely on metal-oxide-semiconductor enhancement-mode configurations [10-12] or SiGe/strained-Si (SiGe/s-Si) modulation-doped configurations [5, 13], both of which intrinsically introduce charge and spin centers near the target spin either through interface defects or a necessary partially ionized supply layer.

In this paper we propose and demonstrate an enhancement-mode SiGe/s-Si stack with a gate-defined quantum dot, which both spaces the quantum dot spin away from interface defects and removes dopants. Enhancement-mode SiGe/s-Si field-effect transistors (FETs) have been demonstrated previously [14, 15] and have recently achieved mobilities as high as $1.6 \times 10^6$ cm$^2$/Vs [16]. Enhancement-mode structures furthermore may provide increased tunability over critical properties such as valley splitting through tuning of the vertical electric field [17]. We report in this letter that low-disorder quantum dots can be formed using a double-top-gated lateral quantum dot nanostructure, defined using deep ultraviolet (DUV) 248 nm lithography and 150 mm-wafer processing. We measure a Hall mobility of $1.6 \times 10^5$ cm$^2$/Vs at 4 K, showing that relatively high mobilities, indicative of low disorder, can be sustained in a foundry process using implanted ohmic contacts and chemical-vapor-deposited (CVD) dielectrics.

The starting material for our devices was a s-Si/relaxed-SiGe/s-Si/relaxed-SiGe epitaxial stack, grown on a SiGe virtual substrate. All epitaxy, done using low-pressure chemical-vapor-deposition (LPCVD) at Lawrence Semiconductor Research Laboratory, started on 5-30 Ωcm, B-doped (100) Si substrates with < 1.0 degree miscut. The virtual substrate consisted of a 3 μm-thick linearly-graded layer and a 1 μm-thick relaxed SiGe layer, which was smoothed by chemical mechanical polishing (CMP). The Ge concentrations of the SiGe layers and the virtual substrate were nominally 30%. Following this, an additional SiGe buffer layer (200nm), a s-Si quantum well (15nm), a SiGe barrier (95nm), and a s-Si cap (2nm) were grown.

In the Sandia National Labs silicon foundry, the device stack was formed with a 50 nm-thick LPCVD Si$_3$N$_4$ layer, a 200 nm-thick As-doped polysilicon layer, and an oxide/nitride/oxide stack capped with a Ti/TiN/W metallization layer. Ohmic contacts were formed with degenerately doped As implants. The polysilicon was patterned using lithography with approximately 180 nm resolution. The first oxide was formed by steam oxida-
TABLE I. Process Flow

| Process Details                  | Thermal Budget |
|---------------------------------|----------------|
| Process Details                 |                |
| Si₃N₄ deposition                | LPCVD          |
| Alignment marks; ohmic implant  | 750°C, 85 min  |
| Amorphous Si deposition         |                |
| Poly implant; recrystallization anneal |          |
| Poly etch; poly reoxidation     |                |
| RTA                             |                |
| Si₃N₄ deposition                |                |
| SiO₂ deposition                 |                |
| CMP; via etch; Ti/TiN deposition; RTA |            |
| W/TiNi deposition; metal etch; window etch; forming gas anneal |            |

Strain relaxation and interdiffusion of Ge into the buried s-Si layer introduce limits on the thermal budget available for device processing. High quality dielectric deposition and dopant activation often use high temperatures, well above the growth temperatures of the SiGe/s-Si stack. Rapid thermal annealing (RTA) at 800°C for 10 seconds activates enough dopants to avoid freeze-out down to the lowest temperature measured, 0.25 K. The resistivity of the implanted regions is 155 Ω/square at 4 K. The thermal budget of the dielectric layer depositions and the activation anneal are indicated in Table I. X-ray diffraction (XRD) of epitaxy on wafers grown under similar conditions as the device wafer indicated a starting s-Si quantum well thickness of 15±2 nm. Cross-sectional transmission electron microscopy (XTEM) of the processed device structure, displayed in Fig. 1(b), shows that the buried s-Si layer is approximately 6 nm thick clearly indicating that the s-Si well does survive the thermal budget. The starting s-Si well thickness was not directly quantified by XTEM, because the entire 150 mm wafer was necessary for fabrication in the silicon foundry, and the final s-Si well thickness was not measured by XRD as it was below the detection limits of the measurement.

We measured the dependence of mobility on density using 100 × 600 µm² Hall bars. The polysilicon layer was used as an enhancement gate in the Hall bar structure. Low-field Hall effect measurements were carried out at 4K using standard lock-in techniques, and the results are shown in Fig. 1(c). The mobility increases with density to 1.6 × 10⁷ cm²/Vs at 5.8 × 10¹¹/cm². Onset of gate leakage limits the maximum density. We observed similar mobilities in a second wafer, identical to the first but for a nominally 80 nm-thick SiGe barrier layer. Ge/Si interdiffusion, expected with this thermal budget, will lead to a less abrupt interface and a thinner quantum well, both of which presumably reduce the mobility. The highest reported mobility [16] is for a case where the highest thermal step is kept at 440 C. Smoother disorder potentials and higher mobilities are therefore possible if desired in this particular stack considering that several thermal steps in the process flow have not yet been optimized.
Nanostructures, fabricated on the same 150 mm wafer, were operated in a double-top-gated configuration. The top metal gate was positively biased to accumulate electrons in the s-Si quantum well globally. In contrast with the Hall bar devices, here the nano-patterned polysilicon gates, below the top metal gate, were negatively biased to isolate the quantum dot region. A schematic drawing of a double-top-gated device is shown in Fig. 2(a). Figure 2(b) displays the design of the quantum dot studied in this work, and a zoom-in of the active region is provided in Fig. 2(c). In this letter, we present transport measurements through the bottom dot formed between the ‘H’, ‘L’, and ‘R’ depletion gates.

The transport experiment was performed in a 3He cryostat with a base temperature of 0.25 K using standard lock-in techniques. The excitation voltage across the dot was 10 μV at 79 Hz. Figure 3(a) shows the conductance with the ‘L’ and ‘R’ gates swept against one another. Periodic resonances are observed in the upper right quadrant of the plot, consistent with Coulomb blockade and quantum dot formation. The slope of the resonances indicates that the dot couples to the two depletion gates with roughly equal capacitance. The slope of the resonances is uniform over the bias range, indicating a well-formed single-dot, without any nearby parasitic dots. To measure the charging energy, we apply a combination of DC and AC voltages on the drain, and measure the differential conductance, shown in Figs. 3(b) and (c). Most of the Coulomb diamonds extend to approximately 300 μeV, though after the last transition observable at zero DC bias, no further transitions are observed up to DC voltages as high as ±10 mV suggesting the dot has low electron occupation.

In summary, we propose and demonstrate a SiGe/s-Si enhancement-mode gate stack for quantum dots. This structure is appealing for quantum computing applications because it is a path towards minimizing background charge and spin defects relative to other Si quantum dot configurations. The devices are fabricated in a 150 mm silicon foundry requiring the use of implanted ohmics and CVD dielectrics, in contrast with previous demonstration of high-mobility SiGe/s-Si enhancement-mode FETs that used AuSb alloyed ohmics and low-temperature atomic-layer-deposition of Al₂O₃ for the gate dielectric. A mobility of 1.6 × 10⁵ cm²/Vs at 5.8 × 10¹¹/cm² at 4K is established in Hall bars. Higher electron densities were limited by leakage in these device structures. Double-top-gated nanostructures using the same process flow show periodic Coulomb blockade. The quantum dot structure uses a remote global gate to induce electrons, polysilicon
gates patterned with DUV lithography and a CVD Si$_3$N$_4$ layer to form the gate dielectric/semiconductor interface. The Coulomb blockade is consistent with a lithographically defined dot with charging energy around 300 $\mu$eV.

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