Silicon strip detectors for LHC: comprehensive process and device analysis

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Abstract

In this paper, the application of technology CAD methodologies to design and optimization of Silicon Microstrip Detectors is described. More specifically, extensive use of both process and device simulation has been made, in order to predict the performance of DC and AC-coupled detectors being fabricated at CSEM SA Neuchatel, Switzerland, in the framework of a CERN R&D collaboration. Such devices, intended to be part of the CMS-project Si-Tracker, have also been extensively tested at the INFN laboratories in Perugia, Italy. Satisfactory agreement between measured and simulated data has been found. This validates the proposed approach, which allows for fast and inexpensive characterization of “virtual” devices.

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Silicon strip detectors for LHC: comprehensive process and device analysis

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In this paper, the application of technology CAD methodologies to design and optimization of Silicon microstrip detectors is described. More specifically, extensive use of both process and device simulation has been made, in order to predict the performance of DC- and AC-coupled detectors being fabricated at CSEM SA Neuchâtel, Switzerland, in the framework of a CERN R&D collaboration. Such devices, intended to be part of the CMS-project Si-Tracker, have also been extensively tested at INFN laboratories in Perugia, Italy. Satisfactory agreement between measured and simulated data has been found. This validates the proposed approach, which allows for fast and inexpensive characterization of “virtual” devices.

1 Introduction

Silicon microstrip detectors have achieved a widespread diffusion in the HEP community, mainly thanks to their reliability and high-resolution properties. Although the basic operating principle remains unchanged, many design options have been investigated in order to improve the detector performance. DC and AC coupling to VLSI read-out circuitry has been proposed, single- as well as double-sided detectors have been produced, and different biasing schemes have been used. Feature-size of such large-area IC’s exceeds by far that of state-of-the-art, conventional integrated circuits; nevertheless, fabrication process is still quite critical to many respects (e.g., detectors reliability, noise performance, manufacturing yield). Accurate design tools and methodologies can thus be profitably borrowed from conventional IC design environments. In this paper, we report on the application of computer-aided methodologies to the design and validation of silicon microstrip detectors fabricated in the framework of CMS project [1].

More specifically, extensive use of numerical process- and device-simulation has been made to predict performance of detectors integrating double-sided readout, AC-coupling capacitors and polysilicon biasing resistors [2]. Joint process and device simulations make it possible to establish a close correlation between fabrication process parameters and detector performance: the analysis has been carried out starting from the knowledge of process recipes and parameters, and accounting for the same photolithographic CAD mask layout used for the actual device production.

Figure 1: Net doping distribution as obtained from process simulation: view of the implanted strip and of the coupling capacitor.

First, a comprehensive tuning of the simulator against experimental results has been carried out, in order to select (among several possible alternatives) the proper set of physical models and numerical algorithms to be used for the simulation. To this purpose, device testing has been performed at CSEM and at INFN laboratories in Pe-
rugia, Italy. Then, the effect of changes in some process parameters (resulting in different values for the oxide charge and doping concentration, for instance) have been investigated. Details on the simulation strategy are given in Sect. 2 below. Simulation results are discussed, and compared with experimental findings, in Sect. 3, whereas some concluding remarks are eventually drawn in Sect. 4.

Figure 2: Electron concentration as computed by device simulation.

2 Simulation outline

All of the simulation activity described in the following has been carried out by using the Virtual Wafer Fab (VWF, [3]) developed by SILVACO. Such a package provides process- and device-simulators, as well as database functions (allowing data exchange among simulators and/or experimental data) and pre- and post-processing graphic utilities. In particular, 2D process-simulation has been performed by the ATHENA program, predicting actual device cross-section, doping profiles, oxide-trapped charge distribution, etc.; a detail of the obtained device structure is illustrated by Fig. 1. Such data are then forwarded to the device simulator ATLAS, which in turn works out the electrical behaviour of the device under investigation; “external” responses (I-V curves, terminal capacitances, for instance) are predicted, which can be compared with measures; moreover, “internal” quantity distributions (e.g., electric field, carrier concentrations) are obtained as well.

A key issue, with respect to device modelling, is that of physical models accounting for many semiconductor properties: since fundamental-physics approach is, at least in our case, computationally prohibitive, a suitable set of models describing carrier statistics, carrier mobilities, generation-recombination rates should be tailored to the specific device at hand.

For the simulation of Si-microstrip detectors, we found it particularly relevant to account for i) a suitable description of carrier mobilities, which has been accounted for by means of a concentration-dependent model [3] and ii), an accurate parameter characterization of the Shockley-Read-Hall generation-recombination model [4]. In particular, carrier lifetimes within high-resistivity silicon have been experimentally determined at CSEM.

3 Simulation results

The simulated device has been characterized with respect to some fundamental parameters: depletion voltage, interstrip resistance and interstrip capacitance.

The interstrip resistance has been estimated by means of DC (steady-state) simulations. Since interstrip resistance depends on the bias voltage, a constraint can be placed on the operating voltage, such that the interstrip resistance is guaranteed to be larger that a specified lower limit. Simulation results are plotted in Fig. 3, and show that at any bias voltage exceeding the depletion voltage an interstrip resistance well in excess of 1 GΩ/cm (i.e., a factor 1000 greater than the bias polysilicon resistance) is obtained.

Depletion voltage $V_d$ can be extracted by looking at the strip capacitance to backplane ($C_b$) which, in turn, can be obtained from AC simulations. Depletion voltage can be inferred from the knee position in the customary $1/C_b^2$ vs. $V_{bias}$ plot (Figs. 4-5).

Figure 3: Interstrip resistance as a function of $V_{bias}$ (throughout the paper, oxide-trapped charge has been expressed as an equivalent interface charge density).

As expected, depletion voltage is quite sensible to the substrate doping concentration, whereas it exhibits a much smaller sensitivity on the amount of oxide-trapped charge. It is worth mentioning that, at first order, radiation damage effects on Si microstrip detectors can be taken into account by proper adjustments of both bulk- and oxide-impurity concentration [5], so that the same kind of analysis can account for irradiated detectors as well.

Strip capacitances plays a dominant role in settling
the noise performance of Si microstrip systems. Optimal strip geometry comes in fact from a trade-off between detector resolution and noise performance. Although strip capacitance depends essentially on device geometry [6], significant non-geometrical contributions come also from the surface charge layers accumulated at the Si/SiO₂ interface. Simulation allows for analyzing the correlation between the amount of oxide-trapped charge and the electron layer build-up. An almost logarithmic dependency on the interface charge-density can be inferred from the plot in Fig. 6. Dependency of the total strip capacitance \( C_{\text{strip}} \) (\( C_{\text{strip}} = C_b + 2(C_{\text{i,n}} + C_{\text{i,n+1}}) \), where \( C_{\text{i,n}} \) denotes the capacitance to n-th neighbours) upon the applied strip bias is illustrated by Fig. 7 (contributions of 3rd and higher-order neighbouring strips turn out to be negligible, since \( C_{\text{i,n}}/C_{\text{i,n+1}} < 1\% \)). Again, different values of the oxide-trapped charge are accounted for: the increase of the latter is shown to result in a capacitance increase and, thus, in a worse S/N ratio. To this respect, hence, simulation allows to predict the operational limits, in terms of accumulated oxide charge, within which the detectors can provide satisfactory performance for their whole life.

In order to compare simulation results with actual silicon microstrip detectors, measurements have been performed on a full-scale AC-coupled detector coming from a CMS test production. Separate capacitance components have been individually measured, following the scheme presented in [6]. Comparisons are given in Fig. 8.

### 4 Conclusions

An extensive set of numerical simulations has been carried out, to investigate several issues concerning design and optimization of integrated silicon microstrip detectors. Joint process- and device-simulation allowed for establishing close correlations between fabrication process parameters and device electrical response. Simulation results have been validated by comparing them with actual device measurements: good agreement has been found in all cases. This illustrates both practicality and reliability of the TCAD approach to the efficient design and optimization of silicon microstrip de-
Figure 8: Fig. 8: Interstrip and backplane capacitance: measurement and simulation result comparison.

The application of conventional numerical simulation technique to wafer-scale IC design appears to be an attractive way to reduce prototipization time and expenses, as well as providing a mean for physical insight of detailed detector operation. Applicability to radiation-tolerance investigations has been proved: future work will indeed mainly develop toward this goal.

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