Hybrid integration of carbon nanotube and amorphous IGZO thin-film transistors

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ABSTRACT
Solution-processed carbon nanotubes (CNTs) have recently attracted significant attention as p-type thin-film transistor (TFT) channels due to their high carrier mobility, high uniformity, and low process temperature. However, implementing sophisticated macroelectronics with a combination of single CNT-TFTs has been challenging because it is difficult to fabricate n-type CNT-TFTs. Therefore, in combination with indium-gallium-zinc-oxide (IGZO), which has excellent electrical performance and has been commercialized as an n-type oxide TFT, we demonstrated various hybrid complementary metal-oxide semiconductor integrated circuits, such as inverters and NOR and NAND gates. This hybrid integration approach allows us to combine the strength of p-type CNT- and n-type IGZO-TFTs, thus offering a significant improvement for macroelectronic applications.

High-performance flexible electronics are highly desirable for wearable, medical, healthcare, and robotics applications.1–3 Carbon nanotubes (CNTs) are promising candidates for high-performance flexible electronics due to their high carrier mobility, high current density, high mechanical flexibility/stretchability, and compatibility with printing processes.4–8 In particular, highly purified semiconducting CNTs have attracted widespread attention for manufacturing diodes, field-effect transistors (FETs), thin-film transistors (TFTs), and integrated circuit (IC) applications.9–12 In addition, TFTs with record-breaking performance have been reported using CNTs achieved from a density-gradient ultracentrifugation method, with semiconducting purity above 99%.13 However, CNT-TFTs typically exhibit p-type properties under ambient conditions due to the adsorption of oxygen and water vapor;14–16 therefore, if the ICs are implemented with only CNTs, they are expected to exhibit poor electrical performance. There have been many efforts to convert p-type operations to n-type operations,17–19 but controllability and stability issues remain difficult to resolve. To overcome the aforementioned issues, new concepts of CNT-based IC applications, such as pseudocomplementary metal-oxide semiconductor (CMOS) combination circuits and diode-based circuits, have been demonstrated.20,21 Nevertheless, complex process steps, low integration, and high manufacturing costs remain.

Recently, as interest in macroelectronic circuits with low static power consumption has increased, hybrid combinations of complementary materials such as CNTs and amorphous indium-gallium-zinc-oxide (IGZO) have widely been studied for various complementary circuits.22–25 IGZO is one of the most promising members in the amorphous oxide semiconductor category, with excellent n-type electrical performance.26,27 In particular, IGZO-based TFTs have been successfully employed in pixel driving circuits, such as liquid crystal displays (LCDs) and organic light emitting diodes (OLEDs), for commercial display applications.28

Here, we demonstrate a hybrid integration based on p-type CNT-TFTs and n-type IGZO-TFTs to achieve hybrid CMOS ICs, which are a potential candidate to replace silicon CMOS technology. We evaluated the electrical performances of devices (CNT- and IGZO-TFTs) and ICs (inverters and NAND and NOR gates). The fabricated CNT- and IGZO-TFTs showed high on-state current ($I_{ON}$), high on/off current ratio [log($I_{ON}/I_{OFF}$)], and high carrier...
mobility ($\mu_{FE}$). By employing these TFTs, the hybrid CMOS inverters exhibited excellent electrical performances with low power consumption and high voltage gains. Finally, we also demonstrate the operations of the two-input NAND and NOR gates fabricated based on the CNT- and IGZO-TFTs. As a result, the logic circuits provide correct logical functions according to input signals. We believe that the hybrid integration approach combines the strength of p-type CNT- and n-type IGZO-TFTs for high-performance CMOS IC designs.

Figure 1(a) illustrates the details of the fabrication processes of a hybrid CMOS inverter based on the CNT- and the IGZO-TFTs, and the two-input NAND and NOR gates also have the same process steps. First, the hybrid device fabrication was initiated on a silicon (Si) wafer with a thermally grown 300-nm-thick silicon dioxide ($\text{SiO}_2$) layer. Next, the titanium (Ti) local bottom gate with a thickness of 20 nm was deposited with an electron-beam (e-beam) evaporator. An aluminum oxide ($\text{Al}_2\text{O}_3$) with a thickness of 40 nm was grown as a gate insulator through atomic layer deposition (ALD) at 80 $^\circ$C, and then, a 10-nm-thick $\text{SiO}_2$ layer was formed using e-beam evaporation for effective semiconducting CNT network formation. At present, the formation of the bottom gate and gate insulator is the same process for p-type CNT- and n-type IGZO-TFTs. To fabricate the p-type CNT-TFT, the surface of the $\text{SiO}_2$ layer was first cleaned by oxygen plasma treatment for 1 min at 30 W. The substrate was functionalized with a poly-L-lysine solution (0.1% w/v in water; Sigma Aldrich) by dropping the solution onto the $\text{SiO}_2$ substrate. Then, Ti and gold (Au) layers (each 5 nm and 200 nm, respectively) were deposited with an e-beam evaporator as the metallization process to serve as the S/D electrodes, followed by a lift-off process. To open the gate contact pad, a photolithography process was performed, and the gate insulator ($\text{Al}_2\text{O}_3/\text{SiO}_2$) was wet-etched in a diluted hydrofluoric acid (HF) solution for 40 s. Next, 200-nm-thick $\text{SiO}_2$ was deposited by plasma enhanced chemical vapor deposition (PECVD) as an interlayer dielectric (ILD) layer, followed by additional photolithography and an oxygen plasma-etching process to define the semiconducting CNT network channel and deposition of a Ti local bottom gate electrode. (II) Formulation of the CNT channel. (III) Deposition of the IGZO channel to fabricate an n-type TFT fabrication after deposition of the $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate insulator. (IV) Sputtering of Ti/Pd S/D electrodes and CNT etching using oxygen plasma to define the semiconducting CNT channels. (V) Deposition of p-type Ti/Pd S/D electrodes and deposition of a Ti local bottom gate electrode. (VI) Au layer metallization process for device-to-device interconnections; thus, hybrid CMOS ICs were completed.
μ from 2 μricated CNT- and IGZO-TFTs ranged from 2 thin-film was 0.3 nm. The age CNT density obtained for 20 min deposition was extracted as 75 images, it is confirmed that the CNT network channel and IGZO p the channels of semiconducting CNT network and the IGZO thin film are shown in Figure 1(b) depicts the optical microscope image of the hybrid CMOS inverter. Atomic force microscopy (AFM) images of the 99% semiconducting CNT network and the IGZO thin film are composed of the amorphous IGZO thin-film channel (oxygen flow rate of 0.1 sccm). (d) Output characteristics (I DS–V DS) with good μ50 μm were chosen as the optimized conditions used in the hybrid CMOS ICs.

Figure 3(a) shows a schematic diagram of a hybrid CMOS inverter based on p-type CNT- and n-type IGZO-TFTs. Figure 3(b) demonstrates the voltage transfer curves (VTCs) of the hybrid CMOS inverter with supply voltages (V DD) of 4 V, 6 V, 8 V, and 10 V. The hybrid CMOS inverter exhibits sharp switching with rail-to-rail output voltage (V OUT) behavior. The logic threshold voltages (V TL) of the hybrid CMOS inverter where the input voltage (V IN) equals V OUT were measured close to V DD/2 due to the optimized device dimensions of the CNT- and IGZO-TFTs. The voltage gains of our hybrid CMOS inverter are 36 V/V, 59 V/V, 70 V/V, and 123 V/V with V DD values of 4 V, 6 V, 8 V, and 10 V, respectively. These results show higher voltage gains at lower V DD than the previously reported hybrid CMOS inverters based on CNT- and IGZO-TFTs due to our optimized process conditions. By controlling the device dimensions and process conditions, we were able to achieve the enhanced performances, regarding log(I ON/I OFF), μ FE, and I ON, which also

FIG. 2. (a) Transfer characteristics (I DS–V GS) of the p-type CNT-TFT with L = 5 μm and W = 10 μm composed of the 99% semiconducting CNT percolated network channel (deposition time of 20 min). (b) Output characteristics (I DS–V DS) of the CNT-TFT for different V GS ranging from 0 V to −6 V in −2 V steps. (c) Transfer characteristics (I DS–V GS) of the n-type IGZO-TFT with L = 5 μm and W = 50 μm composed of the amorphous IGZO thin-film channel (oxygen flow rate of 0.1 sccm). (d) Output characteristics (I DS–V DS) of the IGZO-TFT for different V GS values ranging from 0 V to 6 V in 2 V steps.

FIG. 3. (a) A schematic diagram of a hybrid CMOS inverter consisting of p-type CNT- and n-type IGZO-TFTs. (b) Voltage transfer characteristics (VTCs) of the hybrid CMOS inverter obtained at V DD from 4 V to 10 V by a 2 V step. The inset is an equivalent circuit of a hybrid CMOS inverter. (c) Voltage gain of the hybrid CMOS inverter depending on V DD.
resulted in the enhanced voltage gain of the hybrid CMOS inverter. In addition, the maximum power consumption of the fabricated hybrid CMOS inverter is 9.8 μW at a $V_{DD}$ of 10 V, which indicates low power consumption of our hybrid CMOS inverter. The key metrics of the mentioned CNT- and IGZO-TFTs and hybrid CMOS inverter composed of them are quantitatively summarized in Table I.

Table I. Performance comparison for the CNT- and IGZO-TFTs and hybrid CMOS inverter.

| References | $-I_{ON} \times W/L$ (μA) | $Log(V_T)$ | $\mu_{FE}$ (cm²/V s) | $+I_{ON} \times W/L$ (μA) | $Log(V_T)$ | $V_P$ (V) | $\mu_{FE}$ (cm²/V s) | Supply voltage ($V_{DD}$) (V) | Inverter gain | Power consumption (μW) |
|------------|--------------------------|------------|---------------------|--------------------------|------------|----------|---------------------|-----------------------------|-----------------|-------------------|
| This work  | 3.92                     | 4.78       | −1.1                | 3.38                     | 6.62       | 1.2      | 20.7                | 4                           | 0.06            | 10.29             |
| 16         | 2                        | 5          | −12                 | 7                        | 5.8        | 2.5      | 12.9                | 20                          | 109             | 20                |
| 23         | 1.2                      | 6          | −2                  | 2.83                     | 6          | 1.2      | 8                   | 5                           | 20.9            | 1.8               |
| 24         | 0.2                      | 5          | −2                  | 1                        | 5          | 3        | 4.93                | 5                           | 45              | 0.6               |

Figure 4(a) presents a schematic illustration of a two-input hybrid NOR gate implemented based on p-type CNT- and n-type IGZO-TFTs. The NOR gate is realized by connecting two CNT-TFTs in series and two IGZO-TFTs in parallel. The NOR gate demonstrates a rail-to-rail voltage swing from 0 V to 10 V at a $V_{DD}$ of 10 V. Figure 4(b) shows the output of the NOR gate that correctly returns the output of logic “1” state (10 V) only at the condition when both of the inputs ($V_A$ and $V_B$) are set to logic “0” state (0 V) or when both IGZO-TFTs are turned off. Figure 4(c) shows a schematic circuit diagram of the NAND gates, which are achieved by connecting two CNT-TFTs in parallel and two IGZO-TFTs in series. Figure 4(d) also illustrates the output of the NAND gate returning correctly a signal logic “0” state (0 V) only when both of the inputs are logic “1” state (10 V) or when both CNT-TFTs are turned off. Logic circuits such as NAND and NOR gates return accurate output signals based on their input logics, which are some of the basics in modern digital IC. This allows the design of hybrid CMOS ICs to further explore the possibilities of implementing high-performance digital logic circuits.

In conclusion, we demonstrated a hybrid integration based on p-type CNT- and n-type IGZO-TFTs to implement hybrid CMOS ICs. Individual CNT- and IGZO-TFTs with high $I_{ON}$, high $log(I_{ON}/I_{OFF})$, and high $\mu_{FE}$ were fabricated, and the two TFTs exhibited balanced electrical performance. Furthermore, by employing these TFTs, we implemented a hybrid CMOS inverter with high voltage gain and low power consumption. We also show the operations of the two-input NOR and NAND logic gates fabricated with a combination of CNT- and IGZO-TFTs. As a result, the NOR and NAND gates return correct logical functions according to input signals. We believe that our approach of hybrid integration of CNT- and IGZO-TFTs offers great improvement for various macroelectronic applications.

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