Enabling Automated FPGA Accelerator Optimization Using Graph Neural Networks

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Abstract
High-level synthesis (HLS) has freed the computer architects from developing their designs in a very low-level language and needing to exactly specify how the data should be transferred in register-level. With the help of HLS, the hardware designers must describe only a high-level behavioral flow of the design. Despite this, it still can take weeks to develop a high-performance architecture mainly because there are many design choices at a higher level that requires more time to explore. It also takes several minutes to hours to get feedback from the HLS tool on the quality of each design candidate. In this paper, we propose to solve this problem by modeling the HLS tool with a graph neural network (GNN) that is trained to be used for a wide range of applications. The experimental results demonstrate that by employing the GNN-based model, we are able to estimate the quality of design in milliseconds with high accuracy which can help us search through the solution space very quickly.

1 Introduction
The demand for scalable, high-performance computing is increasing rapidly. However, due to the breakdown of Dennard’s scaling [10], we no longer can address it by scaling the clock frequency. This has led to a growing interest into domain specific computing and exploration into using accelerators such as field-programmable gate arrays (FPGAs) to reduce power consumption while achieving a high performance [1, 26]. On the downside, the FPGAs are more difficult to program compared to CPUs and GPUs. It used to be the case that one only could program an FPGA by writing very low level codes that described the transition of data in register-transfer level (RTL). In the past decades, high-level synthesis (HLS) [6, 47] was introduced to simplify the programming by raising the abstraction level in FPGA design. With HLS, the designer only needs to describe a high-level behavioral description of the design. As a result, HLS has been embraced by both academia and industry [12, 17, 31]. Currently, both FPGA vendors offer their commercial HLS products—Xilinx Vitis [40] and Intel FPGA SDK for OpenCL [13].

The HLS tools let the designers optimize their microarchitecture quickly by inserting a few synthesis directives in the form of pragmas. This feature can potentially help to decrease the turn-around times and shorten the code development cycle. However, because the HLS tools look for the right combination of pragmas for deriving an efficient hardware architecture, not every HLS design has a good quality of results (QoR) [32]. Thus, one often has to explore many design choices for each new application which can negatively impact the design turn-around time.

To speed up design optimization, a new line of research has been created with the focus on automating the microarchitecture optimizations (e.g. [16, 32, 43]). By developing an automated design space exploration (DSE) framework, not only will the hardware designers be free of the design improvement iterations, but other programmers with no knowledge of hardware can also try customized computing. This can in turn result in the growth of the FPGA community and its technology improvement. However, the HLS-based DSE poses the following challenges:

- **The long synthesis time of existing commercial HLS tools**: Using the vendor HLS tools directly for DSE results in a long evaluation time (minutes to hours) for each design candidate and forces us to explore a reduced set of the solution space.
- **The huge solution space**: The solution space grows exponentially by the number of candidate pragmas. Thus, it is important to alleviate the cost of processing different design configurations.
- **Non-smooth impact of design parameters and their correlation**: For example, changing the unroll factor may not lead to the monotone decrease of the latency [24, 32].

Separately, current HLS tools optimize the design based on specific code patterns. Although different applications have different domains, they may share the same code structures for some parts. Thus, it is important to identify the different code patterns and learn their effect to be able to transfer the knowledge we gained from one application to another.

In this paper, we aim to address the challenges mentioned above using graph neural network (GNN) with the support for transfer learning. For this matter, we developed a framework called GNN-DSE\(^1\) to automate the design process. We first build a model to estimate the different objectives of a design quickly, in milliseconds, without the invocation of the HLS tool. Since the HLS tools employ many heuristics to optimize a design and the design parameters affect each other, we let a deep learning model learn their impact. We represent the program as a graph which includes the program semantics in the form of control, data, call, and pragma flows and exploit a GNN to extract the required features of the graph for predicting the objectives. We propose several techniques for improving the accuracy of the model including Jumping Knowledge Network (JKN) [41], node attention [19], and multi-head objective prediction. To demonstrate the effectiveness of our model, we build a DSE on top of it for searching through different combinations of the pragmas to find the Pareto-optimal design points. We show that not only can GNN-DSE find the Pareto-optimal designs for the kernels that were included in its training set, it can also generalize to the kernels outside of its database and detect their Pareto-optimal design points. In this paper, we target Xilinx FPGAs as an example but our approach is tool-independent and extendable to Intel FPGAs as well.

\(^1\)We will open-source the codes once the paper is accepted.
In summary, this paper makes the following contributions:

- We propose a graph-based program representation for optimizing FPGA designs which includes both the program context and the pragma flow.
- We develop a learning model based on graph neural network (GNN) as a surrogate of the HLS tool for assessing a design point’s quality in milliseconds order and propose several techniques for improving its accuracy.
- We create an automated framework, GNN-DSE, to build a database of FPGA designs, train a learning model for predicting the design’s objectives, and run a design space exploration based on the model to close-in on a high-performance design point.
- The experimental results demonstrate that not only can GNN-DSE find the Pareto-optimal design points for the kernels in its database, it can also optimize the unseen kernels by extracting the knowledge it learned from the previously-seen kernels.

2 Background

2.1 Programs as Graphs

A popular way of representing a program as a graph is to extract the control and data flow graph (CDFG) of the program from its intermediate representation (IR) in LLVM [18]. This way, instead of focusing on the grammar of the code, the semantics of the program flow is captured. In a CDFG, the nodes represent the LLVM instructions that are connected to each other based on the control flow of the program. To represent the data flow of the program, a second type of edge is added between the nodes based on the operands of the instructions. Note that a CDFG includes many low-level operations like memory management which makes it a desirable representation for FPGA kernels.

2.2 Graph Neural Networks

Recent years have witnessed an increasing amount of graph data which have motivated the researchers to design powerful models for processing graphs. Among various graph machine learning methods, Graph Neural Networks (GNN) [39] are growing in popularity as seen in wide range of applications, e.g. social network analysis [33], biomedical tasks [44], traffic forecasting [14], etc.

The core idea of a GNN model is to extract the graph information by learning the features (embeddings) of each node in the graph via aggregating information from its neighboring nodes, commonly referred to as “message passing”. A GNN model, like a CNN, pass the node embeddings through a series of layers until it derives the rich information for the graph. The computation of one layer of a typical GNN, in its general form, can be formulated as follows:

\[ h_i' = \sigma (TF(AGG((h_j \in N(i)))))) \]  

where \( h_i \in \mathbb{R}^F \) and \( h_i' \in \mathbb{R}^F \) denote the input and output embeddings of node \( i \) which are a vector of \( F \) (\( F' \)) features, AGG shows the aggregation function which gathers the embeddings of neighbors of each node \( N(i) \), TF represents a transformation function to apply on the aggregated results of each node, and \( \sigma \) is an activation function to introduce non-linearity to the model.

Graph Convolutional Network (GCN) [15] is a popular form of a GNN which adopts a simple aggregation function that performs a weighted summation of the embeddings of neighboring nodes using the degree of a node, \( d_i \), as shown in Fig. 1:

\[ h_i' = \sigma (W \sum_{j \in N(i) \cup \{i\}} \frac{1}{\sqrt{d_i d_j}} h_j) \]  

where \( W \) is a trainable weight matrix for the TF step to act as a filter. Fig. 1 illustrates this operation for a node, i.e., Node 1. It applies a weighted summation on the embeddings of its neighbors (and itself) based on the \( a_{ij} \) values and then multiplies the results with \( W \) for calculating the output embedding.

\[ a_{ij} = \frac{1}{\sqrt{d_i d_j}} \]

**Figure 1: The computation of a GCN layer**

One problem with the GCNs is that the aggregation of features of the nodes are based on a fixed set of weights which are determined by the degree of the nodes. Therefore, the model has no way of prioritizing any of the neighbors to learn better embeddings. To solve this problem, another class of GNN models, Graph Attention Networks (GAT) [36], were introduced to learn the importance of the different neighbors of a node so that they can contribute in updating the node embeddings based on their attention. The computation of a GAT layer can be summarized as below:

\[ h_i' = \sigma (\sum_{j \in N(i) \cup \{i\}} a_{ij} Wh_j) \]  

\( a_{i,j} \)s are the attention coefficients computed by multi-head dot-product attention. The computation for each head is as follows:

\[ e_{i,j} = a^T [Wh_i || Wh_j] \]

\[ \text{LeakyReLU}(y) = \max(\beta y, y), 0 < \beta < 1 \]

\[ a_{i,j} = \frac{\exp \{ \text{LeakyReLU}(e_{i,j}) \}}{\sum_{k \in N(i) \cup \{i\}} \exp \{ \text{LeakyReLU}(e_{i,k}) \}} \]

where || denotes the concatenation operation and \( a \) is a learnable vector controlling the attention that node \( i \) receives from node \( j \). Note that the TF step is the same as GCN and only the AGG step is changed. Fig. 2 shows this computation on a toy graph.

**Figure 2: How the attention coefficient is calculated in a GAT layer**
2.3 The Merlin Compiler

The Merlin Compiler\(^2\) [4, 5] was developed to make FPGA programming easier by raising its abstraction level. Inspired by the programming model of OpenMP [9], it introduces a reduced set of high-level compiler directives in the form of pragmas to optimize the design. Based on these pragmas, it performs source-to-source code transformation and automatically generates the respective HLS code along with the required HLS pragmas to enable the designated optimizations. Table 1 lists the Merlin Compiler’s optimization pragmas. When fine-grained pipelining is enabled (mode fg), the Merlin Compiler tries to pipeline a loop nest while fully unrolling all its sub-loops. The coarse-grained pipelining (mode cg) refers to the case where the Merlin Compiler transforms the code to enable double buffering. Based on these pragmas, the Merlin Compiler automatically employs code transformations to implement memory coalescing, apply memory burst, and cache the required data for enabling the architectural optimizations.

| Keyword | Available Options   | Architecture Structure |
|---------|---------------------|------------------------|
| pipeline| mode=cg/fg           | CG or FG pipelining    |
| parallel| factor=<int>         | CG & FG parallelism    |
| tile    | factor=<int>         | Loop Tiling            |

Table 1: Merlin Pragmas with Architecture Structures

CG: Coarse-grained; FG: Fine-grained

We chose to utilize the Merlin Compiler as the backend of our tool to not only reduce the size of the solution space, but also exploit its code transformations to achieve a better design. Nonetheless, by employing the Merlin Compiler, the GNN model works harder to learn because it needs to decipher when (and where) the Merlin Compiler applies its automated optimizations.

3 Problem Formulation

In this work, we aim to speed up the DSE problem for HLS. For this matter, we first seek to develop a prediction model that can mimic the HLS tool by estimating the quality of design. Then, using our predictive model, we run a DSE on different design parameters (pragmas) to find out the best combination of parameters for optimizing the design. More formally, we propose solutions for the following two problems:

**Problem 1: Build the Prediction Model.** Let \( \mathcal{P} \) be a C program as the FPGA accelerator kernel with \( K \) parameters \((p_i)\) denoting different possible HLS pragma candidates as design configurations \((\theta)\), where \( \mathbb{R}^K_p \) is a set of all the different configurations:

\[
\theta = \{ p_0, p_1, ..., p_K \} \in \mathbb{R}^K_p
\]  (5)

Let \( H \) be a vendor HLS tool that outputs the true execution cycle \( Cycle(H, \mathcal{P}(\theta)) \) and the true resource utilization \( Util(H, \mathcal{P}(\theta)) \) of the program \( \mathcal{P} \):

\[
Q_H(\mathbb{R}^K_p) = \{ (Cycle(H, \mathcal{P}(\theta)), Util(H, \mathcal{P}(\theta))) | \theta \in \mathbb{R}^K_p \}
\]  (6)

Find a prediction function \( (F) \) that approximates the results of \( H \) for any given program \( \mathcal{P} \) with any design configurations \((\theta)\) having any number of parameters:

\[
\min_{F} \text{Loss}(Q_F(\mathbb{R}^K_p), Q_H(\mathbb{R}^K_p))
\]  (7)

In case of a regression task, the loss function is calculated using root mean squared error (RMSE) over all the designs. For the classification task, the percentage of misclassified cases are considered.

**Problem 2: Identify the Optimal Configuration.** Given a C program \( \mathcal{P} \) as the FPGA accelerator kernel with \( K \) parameters along with its design space set \( \mathbb{R}^K_p \), and a prediction function \( F \), find a configuration \( \theta \in \mathbb{R}^K_p \) in a given search time limit so that the generated design \( \mathcal{P}(\theta) \) can fit in the FPGA and the execution cycle is minimized. Formally, our objective is:

\[
\min_{\theta} \text{Cycle}(F, \mathcal{P}(\theta))
\]  (8)

subject to

\[
\theta \in \mathbb{R}^K_p, \quad \forall u \in Util(F, \mathcal{P}(\theta)), u < T_u
\]  (9)

where \( u \) is the utilization of one type of the FPGA on-chip resources and \( T_u \) is a user-defined threshold for that type on the FPGA.

4 Related Work

With FPGA’s synthesis time being a huge bottleneck in its development cycle, a new research domain has been made to explore the solution space more efficiently. Because of the unpredictability of the HLS tool, they treat it as a black-box and invoke the tool each time they want to get a feedback on the quality of design [28, 32, 43]. To explore the space they either make use of the general search heuristics (such as greedy mutation, simulated annealing, and genetic algorithm), or develop their own heuristic which is more suitable for the HLS DSE problem. However, their performance is limited by the runtime of the HLS tool; hence, they can explore only a small fraction of the design choices.

To speed up the search, a number of previous works have developed a model to employ instead of the invocation of the HLS tool. The authors in [48, 50] propose an analytical model to predict the design objectives based on the program’s dependence graph. Their models are independent of the HLS tool and rely on only the behavioral description of the program. This can potentially harm the model’s accuracy as the HLS tools utilize multiple heuristics that can lead to different results than the theoretical ones, so they should also be modeled [29]. To improve the accuracy of the model, a category of the previous studies restrict their application domain to limit their accelerators to either a particular application, a well-defined microarchitecture template, or a specific computation pattern [3, 7, 31, 37, 42, 46, 49]. The downside is that they lose generality and are not applicable to other domains.

A series of other works use a learning algorithm to resemble the HLS tool and predict the design’s objectives. These works iteratively sample the solution space, synthesize the designs using the HLS tool, and adopt a supervised learning algorithm (such as random forest or decision tree) until the model gets to an acceptable accuracy [20, 22, 23]. The drawback of these approaches is that they build a separate learning model per application and the results from one application are not transferred to the other one. Kwon et al. [16] propose a transfer learning approach using a multi-layer perceptron (MLP) network to solve this problem. As the input to the model, they only use the pragma configurations. However, as we shall show in
Section 6.2, not taking the program semantics into account harms the accuracy significantly.

A few of the very recent works have proposed to use GNN for predicting the design quality [34, 38]. Ustun et al. [34] proposes a GNN-based model to learn the operation mapping to FPGA’s resources for delay prediction in HLS. IronMan [38] uses GNN to predict the performance of the program under different resource allocations (DSP or LUT) to the computation nodes. Yet, none of these works include the pragmas in their input representation so their models cannot be used for finding the best design configuration. This paper is the first work to employ a graph representation that captures both the program semantics and the pragmas. Furthermore, we show that our approach is capable of learning from a set of applications, building a single predictive model for all of them, and extending its knowledge to new applications.

5 Our Proposed Methodology

Fig. 3 depicts a high-level overview of GNN-DSE which operates in three modes: training, inference, and DSE. When training is enabled, GNN-DSE takes its training database as the input and trains a predictive model to learn to estimate the design’s objectives. The training database contains designs with various configurations from different applications along with their synthesized results using the HLS tool as the true value of the their objectives (Section 5.1).

Instead of manually analyzing the designs and extracting the features that are useful for estimating the quality of design, we let a neural network model discover them since it is less prone to error and can potentially capture the flaws of the HLS tool. To do this, GNN-DSE represents each design in the database as a graph (Section 5.2). Then, the GNN-DSE’s predictive model assembles a GNN model to learn a graph embedding to be fed into a multi-layer perceptron (MLP) network for estimating the different objectives of the design. When the GNN and MLP are trained together, the model tries to adjust the graph embedding in a way that it includes the highest information for predicting the objectives (Section 5.3).

Once the trainer has optimized the predictive model, it can be used for the inference stage, where GNN-DSE gets a C/C++ code as an input along with the desired design configuration. It then adopts the GNN-DSE’s graph generator to get the graph representation of the design. Finally, it employs the trained predictive model to estimate the design’s objectives. During the DSE phase, each of the design configurations are evaluated using the predictive model as in the inference stage. GNN-DSE continuously accumulates more design points; thus, once the DSE is finished, the top M designs are synthesized using the HLS tool to augment the database with their true objectives. This can help us include better representatives of the space in our database (Section 5.4).

5.1 Database Generation

We adapt a related prior work, AutoDSE [32], to generate the initial database for each of the applications. AutoDSE is also built on top of the Merlin Compiler and, by default, it adopts a bottleneck-based optimizer to reduce the number of iterations needed to close-in on high-performance design points. Fig. 4 demonstrates our approach for generating the database. We follow the same rules as AutoDSE in the design space generator for defining the solution space and augmenting the input code with candidate pragmas. More specifically, each for loop can take three pragmas: pipeline, parallel, and tile except for where a pragma is not applicable (e.g., the tile pragma can only be applied when the loop has an inner loop). Note that the Merlin Compiler automatically inserts the rest of the HLS pragmas (such as array_partition) that are needed to satisfy these optimizations. We also make use of the rules AutoDSE has for pruning a design configuration (e.g., when fine-grained pipelining is applied on a loop, all the pragmas for the inner loops should be set to the default value).

The optimizer in AutoDSE is intended to only explore those designs that are promising to have a high quality, i.e., “good” design configurations. However, this is not enough if we want to train a model to predict the results of the HLS tool. In other words, we
need to have a variety of design points from "bad" to "good" so that the model can learn to distinguish them. Therefore, GNN-DSE’s 
explorer extends AutoDSE to exploit three types of explorers:

- The existing explorer of AutoDSE, bottleneck-based optimizer, which can find high quality designs.
- A hybrid explorer that is a combination of the bottleneck-based optimizer and exhaustive search. It first uses the bottleneck-based optimizer to improve the design quality. When the quality of the best design point is improved by X%, it will evaluate up to P neighbors of the new design point (both X and P are user-defined variables). A neighbor is a point that the option for only one of its pragmas is different from the current point. By employing this explorer, the model can see how a design’s quality is changed by modifying only one of its pragmas.
- A random explorer which may consider those configurations that the previous two explorers would skip.

Once the explorer selects a design point for evaluation, it is passed to the Merlin Compiler which generates the equivalent HLS code with the HLS pragmas and invokes the HLS tool to get the design’s objectives. In parallel, the graph generator (Section 5.2) builds the graph representation of the program with that design configuration. Finally, the graph representation of the program, along with the HLS results, are committed to a common database. The training database gradually collects results from different applications in a shared space to be used for training the model.

5.2 Program Representation

The first step in building a predictive model is to define a representation of the program which not only captures its behavioral flow, but also includes the pragmas. As mentioned in Section 2.1, CDFG is a popular choice for this purpose. On the downside, when building the graph, the CDFGs ignore the precision of the operands and their values, which are crucial in determining design’s objectives. Recently, a newer program representation is proposed, PrograML [8], which extends the CDFG by explicitly assigning separate nodes to operands to retrieve the missing information. PrograML is a language-independent representation of the program semantics that takes the LLVM IR [18] of the design as the input and builds a directed graph containing its control, data, and call flow. As such, we build our program representation by extending PrograML and including the pragma flow.

In GNN-DSE, each of the candidate pragmas are defined in either of the following forms:

```
#pragma accelerate pipeline factor=val
#pragma accelerate parallel factor=val
#pragma accelerate tile factor=val
```

where the `pragma_name` is a placeholder for the variable storing the pragma’s option. The choices for pipeline pragma are (off|cg|fg) where off disables the pragma. The other two pragmas take a numerical value as their option as mentioned in Table 1. When their factor is set to 1, they will be disabled.

For each candidate pragma, we augment the graph generated by PrograML with a node that stores the placeholder pragma. Since the pragmas are applied to the loops, we connect this node to one of the instruction nodes corresponding to the loop: `icmp`. Code 1 shows the code snippet for a toy example having a simple for loop with two candidate pragmas. Fig. 5 depicts its graph representation.

**Code 1: Code snippet of an input toy example to GNN-DSE**

```c
void foo(int input[N]) {
    for (int i = 0; i < N; i++) {
        input[i] += 1;
    }
}
```

As Fig. 5 demonstrates, there are three types of nodes in each graph. The first kind (the blue ones) contains the LLVM instructions that together demonstrate the control flow of the program. The second kind (the red ones) exhibits the constant values and variables that capture the data flow of the program. Note that we have removed some of the instruction and data nodes and kept only the relevant nodes to shrink the graph for illustration purposes. The pragma nodes are presented as purple boxes connecting to the respective `icmp` node. In this graph, in addition to the nodes, the edges also have different kinds which show the different flows of the graph: control (blue), data (red), call (green), and pragma (purple). When there are two or more edges of the same type connected to a node, they are numbered to further distinguish them (see the edges connecting from pragma nodes to the `icmp` node).
block ID of the for loop. More specifically, each of the nodes and edges have the following attributes:

Node = (‘block’: LLVM block ID, ‘full_text’: Full description of the node, ‘key_text’: Node key task, ‘function’: Function ID, ‘type’: Node type)

Edge = (Src node ID, Dst node ID, (‘flow’: Flow type, ‘position’: Position ID))

where the type, flow, and position attributes encode this information:

| type   | 0: instruction | 1: variable | 2: constant value | 3: pragma |
|--------|----------------|-------------|-------------------|-----------|
| flow   | 0: control     | 1: data     | 2: call           | 3: pragma |
| position| 0: tile        | 1: pipeline | 2: parallel       |           |

The full_text attribute stores the complete form of the text each node represents, while the key_text attribute shows a keyword corresponding to that node. Here is an example for each of the control, data, and pragma nodes from the graph in Fig. 5:

Fig. 6 depicts the flow of the graph generator in GNN-DSE. Its input is a C/C++ code, and it first generates the LLVM IR representation of the program, along with its candidate pragmas which are produced based on the same rules as the design space generator in Section 5.1. Then, the graph builder outputs their respective graph. For each design configuration, the auto variables in the pragma placeholders are replaced with their corresponding values. Therefore, among the graphs for different design configurations of the same application, only the attributes of their pragma nodes are different.

5.3 Predictive Model

Fig. 7 depicts our model architecture for predicting the design’s objectives. As the figure shows, it starts with taking the graph representation of the program as the input. Then, it encodes the nodes’ and edges’ attributes (Section 5.2) to create their initial embeddings. To do this, we go over all the design points in our database, build a list of all the available attributes along with the available options for each of the pragmas, and create a one-hot encoding for each of them. Then, for each node/edge, we go over their attributes, encode them, and concatenate them to create the initial embeddings. This encoding helps the model to assign a higher weight to the attributes that contribute more to the prediction of final objectives. Once the initial embeddings are available, the model exploits a GNN encoder (Section 5.3.1) to learn which information of the graph to extract for predicting the design’s objectives. After which, the GNN encoder passes the graph embeddings to a set of MLPs to estimate the outputs (Section 5.3.2).

5.3.1 GNN Encoder: The GNN encoder transforms a graph $\mathcal{G}$ with its initial embeddings into a $D$-dimension embedding, $h_{\mathcal{G}} \in \mathbb{R}^D$. This encoder consists of three stages: (1) sequentially stacked TransformerConv layers which produce node embeddings, (2) a Jumping Knowledge Network which combines the node embeddings from different layers to produce the final node embeddings with dynamic ranges of neighborhoods, and (3) an attention mechanism to aggregate the node-level embeddings to produce the final graph-level embedding.

TransformerConv We reviewed two well-known types of GNN layers for building the node embeddings in Section 2.2: GCN [15] and GAT [36]. One drawback of these layers is that they both overlook the edge embeddings. TransformerConv [30] is a state-of-the-art GNN architecture, which combines Transformer [11, 35] with message passing to update a node’s embedding. Similar to GAT, it builds attention coefficients $(a_{i,j})$ for aggregating the neighbors, but in a different manner inspired by the Transformer model and including the edge embeddings:

$$ a_{i,j} = \text{softmax} \left( \frac{(W_1 h_i)\, (W_2 h_j + W_3 e_{ij})}{\sqrt{D}} \right) $$ (10)

where $W_1$, $W_2$, and $W_3$ are learnable weight matrices, and $e_{ij}$ denotes the embedding of the edge between nodes $i$ and $j$. The fact that it includes the edge attributes in the formulation of the $a_{i,j}$ is a desirable feature for our task since the edges in our graph representation contain useful information (Section 5.2) we would like to utilize when updating the node embeddings. In addition, TransformerConv makes use of gated residual connections when updating the node embeddings that can prevent the model from over-smoothing. Consequently, we adopt TransformerConv as the basic building block of our model. The evaluation results in Section 6.2 show that the TransformerConv indeed reduces the loss by 1.48× under the same number of learning iterations.

Jumping Knowledge Network Each layer of a GNN gathers the embeddings of the first-order neighbors. By adding each layer, the nodes will receive the embeddings from one hop further since their first-order neighbors are now updated with their own first-order neighbors. The different nodes in the graph may need different ranges of neighborhoods for updating their embeddings. For example, in the graph depicted in Fig. 5, both the load and add nodes are affected by the pragma nodes. The load node sees the effect of the pragma node after 3 layers, while the add node is impacted after 4 layers. By employing 4 layers of GNN for both of these nodes, the load node may receive some extra noise from new nodes which can affect its embeddings negatively.

Therefore, to fully leverage the embeddings generated by different layers of the GNN model, we exploit the Jumping Knowledge Network (JKN) [41] which as Fig. 7 illustrates, takes in the output of all the layers to flexibly pick different ranges of neighborhood for each node. A JKN, in its simplest form, exploits max pooling for choosing the final embeddings of each node among its node embeddings from all the previous GNN layers:

$$ h_i = \max \left( h_i^{(1)}, \ldots, h_i^{(T)} \right) $$ (11)

where $h_i^{(k)}$ denotes the embedding of node $i$ after the $k$-th layer.

Node attention-based graph-level embedding generation: To generate one vector representation for the entire graph, one can
where $h_\text{G}$ and $N$ denote the graph-level embedding and the number of nodes in the graph, respectively. However, given the fact that our graph representation contains both the pragma nodes and the program context nodes, it is preferable to introduce attention that learns which node is more important for the prediction tasks. Therefore, we adopt the node attention mechanism proposed in [19] for producing the graph-level embedding:

$$h_\text{G} = \sum_{i=1}^{N} \text{softmax}(\text{MLP}_1(h_i)) \cdot \text{MLP}_2(h_i)$$  \hspace{1cm} (12)$$

where $\text{softmax}$ maps the node embedding from $\mathbb{R}^D$ to $\mathbb{R}$ followed by a global softmax to obtain one attention score per node. The attention scores are then applied to the transformed node embeddings, $\text{MLP}_2(h_i)$, to obtain the final graph-level embedding.

Fig. 8 depicts the graph for a design of the stencil (stencil2d) kernel in Machsuite benchmark [27]. The size of the circle for each node is proportional to the attention that its node embedding receives in building the graph-level embedding. As we expected, the pragma nodes are among the most important nodes. Yet, the model could learn that not all the pragma nodes are equally important. As the figure suggests, the loop trip count (icmp node and 132 node connecting to it) and other contextual information of the loop determines the importance of the loop’s pragmas. The results show that, the model could correctly learn that for the outer-most loop level, pipeline and tile pragmas are more important whereas, for the loop inside it, parallel is the most dominant pragma.

The initial node embeddings in our experiments (which we created by concatenating the encoded version of the node attributes) are 124-D vectors and the final embeddings of our GNN encoder are 64-D vectors. We utilize t-SNE [21] to visualize these vectors by down-projecting them into 2-D space. t-SNE is a powerful technique that can model high-dimensional data by 2-D points in a way that nearby (distant) points model similar (dissimilar) data. Fig. 9(a) depicts the t-SNE plot for the stencil kernel based on its initial embeddings. For each design, we create a graph-level embedding by adding the nodes’ initial embeddings. Each point in the plot corresponds to a design which is color-coded by the design’s latency (cycle counts). Fig. 9(b) demonstrates how the t-SNE plot changes if we use the graph-level embeddings generated by our GNN encoder instead. As the figures suggest, while the initial features show high similarity between two design points with a huge difference in their latency value, the GNN encoder could successfully distinguish them and assign embeddings to the graphs in a way that only the designs with similar latency be clustered together.

5.3.2 MLP Prediction Layers: After the GNN encoder has encoded the graph into a $D$-dimensional representation, further transformation is needed to perform the final prediction task. We have the following two learning tasks for assessing a design point:

- **Classification task for determining whether a design configuration is valid.** First, we check whether the combination of the pragmas create a valid design configuration or not. The source of invalidity can come from many factors such as: 1) the pragma combinations may create a design that is hard for the HLS tool to optimize. If synthesis of a design does not finish in 4 hours, we mark it as invalid; 2) the HLS tool may refuse to synthesize a design due to the use of combined high parallelization factors; 3) a combination of the pragmas may not be feasible in general. For example, the coarse-grained pipelining is implemented by applying double buffering on the loop, which is not parallelizable since at each iteration a batch of data should be transferred from DRAM to BRAM. When an optimization is not applicable, the Merlin Compiler produces a warning for it which we use to mark the design as invalid. Although AutoDSE [32] identifies some of the invalid cases (which we use), it does not cover all of the cases so we let the model learn them.
Regression task to estimate the design’s objectives. Once we identify that a design is valid, we estimate the quality of design by predicting its cycle count and resource utilization which we define as our regression task.

For each of these tasks, we exploit an MLP to do the prediction based on the graph-level embeddings. Note that our regression task is seeking to predict multiple objectives. To achieve this, we can either employ separate models for each of them or use the same GNN encoder as the backbone and adopt a different MLP branch for each target objective, as seen in Figure 7. In the former, each model tries to find the graph-level embedding needed to predict the target objective separately. However, in the latter, they can help each other in extracting the useful graph information for predicting the outputs since the same graph-level embedding is fed into multiple branches. This is a desirable feature for us as our objectives are correlated with each other.

5.4 Design Space Exploration

After building an accurate model for assessing a design point, we can search through the different design choices to pick the best one. For each design configuration, we first run the classification model to determine whether it is valid or not. If it is valid, we then run our regression models to predict the design’s objectives. If, for any of the resources, the utilization is higher than 0.8 (80%), we reject that design due to over-utilization. 80% is an empirical threshold which, when the utilization exceeds it, the design will suffer from frequency degradation and difficulty in mapping. Finally, among the remaining designs, we pick the top 10 designs (with the least latency numbers) to be evaluated using the HLS tool. This means that our model helped us to run the HLS tool only 10 times instead of invoking it for every design.

Since our models can finish in milliseconds, we can explore a large number of design points very quickly. Nevertheless, for enormous solution spaces, we still may not be able to search through the whole space in a timely fashion. Therefore, we set a time limit for running the DSE and employ a heuristic to prioritize searching through the most-promising candidates first. As the HLS tools can implement the fine-grained optimizations better, we sort the pragmas by their loop level so that the pragmas of the inner-most loop levels are evaluated sooner.

For ordering the pragmas, starting with the inner-most loops, we adapt a BFS-like traversal of their pragmas. More specifically, starting from the inner-most loop level of each of the nested loop sections, we pick a pragma to explore first. If there are more than one pragma at that level, we prioritize parallel over pipeline over tile. If the picked pragma has a dependency from the same loop level or one loop level further, we prioritize evaluating that dependency before other pragmas. A pragma has a dependency when we want to prune the invalid design combinations. For example, there is always a dependency between the parallel pragma of one loop level with the pipeline pragma of its upper loop level. This is because fg pipelining completely unrolls the sub-loops so we no longer need the parallel pragma. After evaluating this pragma, we do the same process for the next loop section. We continue to do this until all the pragmas are added to our ordered list. Since there is always a dependency between the parallel pragma of one loop level with the pipeline pragma of its upper level, for the second-inner-most loop level upwards, this ordering results in evaluating the pipeline pragma first before any other optimizations (even before pipelining or tiling of its inner loop). This is desirable since, if this pipelining is successful, it will either result in double buffering or fully unrolling the inner loops. Both options are usually preferred compared to other optimizations on the inner loop.

Since getting the true value of design’s objectives are time-consuming, building the dataset is the main bottleneck of our approach. After building an initial database as explained in Section 5.1, we exploit our DSE to augment the database. Note that the DSE wants to run the model on many of the unseen data points. It can perform well only when there are good representatives of all of the design choices in our database. On the other hand, if our DSE believes that an unseen design point is good even though in reality it is bad, it means that the model does not have a sufficient set of data to generalize for the whole space. Since these data points are the ones that made the model mispredict the results, they are more likely to build a better representation of data in the next round.
6 Evaluation

6.1 Experimental Setup

We choose our target kernels from the commonly-used MachSuite benchmark [27], and the Polyhedral benchmark suite (Polysuite) [45]. To generate the initial database for each of the kernels, we extend the AutoDSE [32] framework as explained in Section 5.1 with the Xilinx Virtex Ultrascale+ VCU1525 as the target FPGA. Our database consists of 9 kernels with different computation intensities including matrix and vector operations, stencil operation, encryption, and a dynamic programming application (nw). We wish to train a model to predict the latency in the form of cycle counts, and the resource utilization for DSP, BRAM, LUT, and FF. Our framework is deployed and trained using PyTorch [25].

Table 2 summarizes the number of pragmas, the total solution space size, the total number of configurations, and the number of valid configurations for each of our target kernels. As we explained in Section 5.4, after running the DSE, we evaluate the top designs generated by the model using the HLS tool and add their true objectives to the database so that the model can refine its predictions. The final row in Table 2 summarizes the number of designs after these additions. In our database, the latency is in the range of 660 to 12,531,777 cycles. DSP counts are in the range of 0 to 28,672. The number of BRAM blocks ranges from 0 to 7,464. The LUT usage ranges from 913 to 2,639,487 and the FF ranges from 0 to 3,831,337.

6.2 Model Evaluation

6.2.1 Pre-processing the Data: We start our training by pre-processing our data to limit their ranges so that they can contribute to the loss equally. For this matter, we normalize the number of resources each design takes by dividing them by the available number of resources on the FPGA. We use the following formula when the objective is latency:

\[ \hat{T}_{\text{latency}} = \frac{\log_2 \text{NormalizationFactor}}{\text{latency}} \]  

(14)

Therefore, the model spends more time on reducing the loss for large values of \( \hat{T}_{\text{latency}} \) which corresponds to low latency values, i.e., the high-performance designs. The \( \log_2 \) factor is used to make the data distribution more even since because of the intrinsic features of this problem, the number of high-performance values are limited and the data is originally biased towards low-performance ones. Although using the \( \log_2 \) factor can amplify the losses in prediction when the data is transformed back to its original range, it does not impact our final task which is to find the best design configuration. Note that, when running the DSE, the relative performance numbers are sufficient for us.

6.2.2 Grouping the Objectives: Fig. 10 depicts the correlation matrix of the objectives in our database with 1 (-1) showing the highest (lowest) correlation. As the figure illustrates, the LUT, FF, and DSP values are highly correlated. The latency value has a weak correlation with each of the LUT, FF, and DSP values but it almost has no correlation with BRAM. As a result, the latency, LUT, FF, and DSP values can help each other to learn a better graph embedding as explained in Section 5.3.2. Consequently, we train two models to learn all the objectives, one is responsible solely to predict the BRAM utilization while the other one predicts the rest of the objectives.

6.2.3 Comparative Studies: To test whether our program representation is beneficial for our training task or not, we first test the performance of two models which only use an MLP network with no considerations for the graph structure. The first one (M1) just uses the pragma settings as the input to an MLP as in [16]. The first layer of the MLP is to encode the pragmas of the design; hence, each application has a separate first layer. The rest of the network is shared among all the applications with a second level of MLP to predict the objectives. The second model (M2) takes all the nodes of the graph with their initial embeddings as the input but does not exploit the GNN techniques for updating the embeddings and rather only uses an MLP. It means that it does not see any of the node relations in the graph for transforming the features. Table 3 summarizes the loss of these models and the breakdown of loss for each of the objectives for the regression task along with the percentage of misclassified cases for the classification task. The losses for the regression task are measured using root mean squared error (RMSE). As the results suggest, including the program context in the input is crucial for improving the accuracy of the model since it wants to predict the objectives across applications with different semantics.

Additionally, we assess the effect of our optimizations applied to the model. More specifically, we first tested our model’s performance when it uses either of the GCN, GAT, or TransformerConv as the GNN layer with normal summation to create the graph-level embeddings (M3 to M5). As Table 3 shows, since these models include the different flows (control, data, call, pragma) of the program using a graph structure in addition to the pragma/program context,
Table 3: Model loss on our database. RMSE is used as the evaluation metric for the regression task. For the classification task, the percentage of misclassified cases are reported.

| Model       | Method                                      | Latency | DSP      | LUT      | FF      | BRAM   | All    | Misclassification |
|-------------|---------------------------------------------|---------|----------|----------|---------|--------|--------|-------------------|
| M1          | MLP-pragma                                  | 3.2756  | 0.5857   | 0.3115   | 0.2483  | 0.3356 | 4.7567 | 49.8%             |
| M2          | MLP-pragma-program context                  | 2.9444  | 0.4650   | 0.2401   | 0.1349  | 0.1597 | 3.9442 | 21.3%             |
| M3          | GNN-DSE- GCN                                | 1.6825  | 0.4265   | 0.1642   | 0.1277  | 0.1593 | 2.5602 | 22.9%             |
| M4          | GNN-DSE- GAT                                | 1.1819  | 0.2557   | 0.1266   | 0.1009  | 0.1178 | 1.7829 | 13.7%             |
| M5          | GNN-DSE- TransformerConv                    | 1.1323  | 0.2540   | 0.1245   | 0.0938  | 0.1231 | 1.7277 | 10.6%             |
| M6          | GNN-DSE- TransformerConv + JKN              | 1.0846  | 0.2521   | 0.1112   | 0.0933  | 0.1012 | 1.6324 | 8.6%              |
| M7          | GNN-DSE (TransformerConv + JKN + node att.) | 0.5359  | 0.1253   | 0.0762   | 0.0632  | 0.0515 | 0.8521 | 6.2%              |

they can decrease the loss. Besides, among the GNN models, the TransformerConv has the best performance due to the reasons mentioned in Section 5.3.1. We further evaluated the performance of our GNN model after adding each of the JKN (M6) and node attention (M7) layers. As the results in Table 3 demonstrate, both of these optimizations are necessary since we are combining different types of nodes in our program representation. This validates our hypothesis that the model not only needs to have a way of deciding which instructions and pragmas are more important for the given application but also should be able to dynamically assign the ranges of neighborhood each node requires for updating its features.

6.3 Results of Design Space Exploration

Using our models, we are able to run 22 inferences per second. As a result, we can exhaustively search through all the design choices for our target kernel, except for mvt, in a few minutes. We set a time limit of one hour for running the DSE, which means we get to explore about 80K design choices. As a result, we adopt the heuristic we proposed in Section 5.4 to search through mvt.

As Table 2 suggests, our initial database has only 0.14% of the total design choices which is a very small fraction. Hence, as we explained in Section 5.4, we run the DSE on all the kernels and evaluate their top 10 designs using the HLS tool. Depending on how it performs, we add a various number of design points with their true objectives to the database. Fig. 11 depicts the speedup each kernel achieved compared to the best design in the initial database for different rounds of DSE. As the figure shows, after 3 rounds of database expansion (the last row of Table 2 summarizes the final number of designs in our database), the DSE can find a better or equal design configuration. The chart’s legend summarizes the average speedup of all the kernels after each round.

6.4 Results of Transfer Learning

The final goal of our approach is to be extensible to the other kernels it has not seen. For testing this, we have chosen two new kernels from Polybench which were not included in our database: 2mm, bicg, and gesummv. The first one consists of two matrix multiplications, the second one is doing two matrix-vector multiplications, and the third one consists of two matrix-vector multiplications and a weighted vector addition. Note that four of the kernels in our database are working with matrix-vector operations, although, in general, they have a different problem size and coding structure.

Figure 11: The speedup of the GNN-DSE compared to the best design in the initial database. After each round of DSE, the top designs are added to the database to refine the predictions.

Table 4 summarizes the number of pragmas and the design configurations for each of these kernels. Since our models run in milliseconds order, the DSE is able to explore all the choices in only 2 (1) minutes for bicg gesummv. We adopt our heuristic explained in Section 5.4 for running the DSE on 2mm, which has more than 492M design choices, for one hour. To measure the quality of top designs generated here, we ran the original explorer of AutoDSE for 21 hours, during which it explored 163/126/131 design points for gesummv/bicg/2mm and achieved a speedup of 18x/26x/350x compared to the design with no optimizations. As the results in Table 4 demonstrate, our approach achieved nearly the same performance for these kernels even though they were not included in the training set. Note that for the bicg kernel, it could achieve an even better performance since it was able to explore the whole space; while AutoDSE only explored 3.6% of the space after running for 21 hours as it is dependent on invoking the time-consuming HLS tool.

Table 4: The performance of our approach on the target kernels that were not included in its database. The speedup numbers are with respect to a prior state-of-the-art work, AutoDSE [32], after running it for 21 hours.

| Kernel   | # pragma | # Design | DSE Runtime (min) | # Explored | Speedup |
|----------|-----------|----------|-------------------|------------|---------|
| gesummv  | 4         | 1.536    | 2                 | 1.536      | 0.99x   |
| bicg     | 1         | 1.536    | 2                 | 1.536      | 1.05x   |
| 2mm      | 14        | 492/237,501 | 60                | 75.6/6     | 0.38x   |

7 Conclusion

In this work, we made our first step in modeling the HLS tool to assess a design’s quality in milliseconds. For this matter, we
developed a push-button framework called GNN-DSE to build a learning model for predicting the design’s objectives. We proposed a graph-based program representation which includes both the program semantics and the candidate pragmas and implemented a GNN-based model to help us extract the required information for estimating our targets. We exploited our model to optimize the target applications by searching through their different design configurations and finding the Pareto-optimal ones. The experimental results show that GNN-DSE can build a model with high accuracy to be used among different domains. They also demonstrate that for each domain, we only need to include a few design configurations in the training set. Using them, GNN-DSE is able to not only find the Pareto-optimal designs quickly for the applications in its database, but also extend the knowledge it gained from them to optimize new applications from its existing domains. In the future, we will expand our tool to cover more domains.

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