Abstract—In this article, we explore a new set of circuits, that incorporate both single-flux-quantum and quantized charge-based complementary quantum logic circuits. Circuits that convert single-flux-quantum voltage pulses to quantized charge pulses and vice versa are introduced that lead to circuits that simplify logic and integration operations of individual flux and charge based logic circuits. These include fan-out circuits that enable single flux input to several charge outputs and control gate circuit with charge input controlling flux output. The operation of these circuits is demonstrated in simulations using WRSPICE. An XOR gate implementation is presented as an example to illustrate the operation of these circuits. The developed complementary quantum logic circuits show promise for higher power efficiency and simpler design in the form of fewer junctions for a given logic implementation, leading to the possibility of higher integration density.

Index Terms—Charge-based logic, Josephson junctions, Quantum phase-slips, Single-flux-quantum logic, Superconducting nanowires.

I. INTRODUCTION

DIGITAL computing based on superconducting circuits is re-gaining interest for high-performance and energy efficient computation due to potential for high clock rates and low energy operation [1], [2], [3] as concerns about scaling to exa-scale computing grow with traditional CMOS based electronic circuits [4], [5]. These superconducting circuits are predominantly based on Josephson junctions (JJs) in the form of single-flux-quantum (SFQ) logic and related variants. Several challenges have been observed in SFQ circuits and attempts have been made to overcome challenges such as increasing power efficiency, reducing static power dissipation, accumulation of jitter, etc. [6], [7]. Nonetheless, issues corresponding to scalability still exist with SFQ based technologies that require large area cells to accommodate magnetic flux [3].

Quantum phase-slip phenomenon has been identified as an exact dual to Josephson tunneling based on charge-flux duality [8]. Several applications of quantum phase-slip junctions (QPSJs) were proposed based on this duality, such as in qubits [9], [10], current standards [11] and other similar applications [12], [13], [14]. We have explored the use of QPSJs in circuits by establishing their operation in producing a quantized charge of $2e$ in the form of a current pulse with constant area during a single switching event, akin to single-flux quantum generation in a JJ [15], [16]. This operation was used to develop digital logic circuits [15], [17] and neuron circuits [16], [18], which may have potential advantages over JJ-based circuits in realizing higher density circuits, and with possibility of higher power efficiency, albeit with multiple challenges that must be addressed. These challenges correspond to practical realization of controlled quantum phase-slip effects in superconducting nanowires. The effects of phase-slip are susceptible to charge and thermal noise and may require lower temperature operation compared to JJ-based circuits.

In this paper, we introduce complementary quantum logic (CQL) circuits that accommodate both charge-based logic circuits using QPSJs [15] and flux-based circuits using JJs [19]. We demonstrate these circuits through simulations in WRSPICE using a SPICE model developed for QPSJs [20]. CQL circuits are intended to combine both flux-based and charge-based circuits in providing an alternative way to perform logic operations with superconducting circuits. In section II, the basic building blocks of CQL circuits are introduced that utilize charge island [15], [17], [16] together with the SFQ loop [19]. Circuits that convert quantized flux from SFQ loop to quantized charge from charge island and vice versa are discussed. The conversion circuits together with an additional QPSJ are used to introduce a simple control circuit. Furthermore, fan-out circuits are introduced to use a flux quantum input to drive multiple quantized charge outputs and to use a flux quantum signal to produce a flux and a charge output. In the section III, an example circuit implementing XOR gate logic that employs several of the basic circuit operations implemented in simulation to demonstrate their application. This is followed by a short discussion of potential advantages and challenges of this technology in section IV and conclusion in section V.

II. COMPLEMENTARY QUANTUM LOGIC CIRCUITS

Complementary quantum logic circuits comprise of both the SFQ pulses encoded in a superconducting loop formed by two JJs and an inductor, as well as the quantized charge pulses encoded on a charge island formed by two QPSJs and a capacitor, as their basic building blocks. The following circuits employ these blocks and the corresponding signals generated, in achieving various operations that are essential in a digital logic family.
Fig. 1. SFQ voltage pulse to quantized charge current pulse conversion circuit designed with an SFQ cell and a QPSJ charge island cell. $I_C(J_1) = I_C(J_2)$, $V_C(Q_1) = V_C(Q_2)$. DC bias $V_{bias} = 1.4V_C$, $I_{bias_1} = I_{bias_2} = 0.7I_C$.

Fig. 2. Simulation results of flux to charge conversion circuit shown in Fig. 1. $I_C(J_1, J_2) = 100\mu A$, $V_C(Q_1, Q_2) = 0.7mV$, $L = 10.4pH$, $C = 0.23pF$. $V_{bias} = 1mV$. Magnitude of pulse input $I_{in} = 150\mu A$. (a) Input current pulses to $J_1$ from $I_{in}$. (b) SFQ pulse output from SFQ loop formed by $J_1$, $J_2$ and $L$ measured at node 1 of Fig. 1. (c) Quantized charge output from the charge island formed by $Q_1$, $Q_2$ and $C$ measured at node 2 of Fig. 1.

A. Flux to charge conversion circuit

The cells corresponding to SFQ loop and charge island can be used in a single circuit to realize flux to charge conversion. The resulting circuit is shown in Fig. 1. The two identical JJs in the circuit are biased with currents that are 70% of their critical currents $I_C$ and the two identical QPSJs are biased using a DC source $V_{bias}$ with a value of 1.4 $x$ critical voltage $V_C$ of the junction. An input pulse current drives junction $J_1$ to its resistive state generating a voltage pulse corresponding to a flux quantum in the loop formed by $J_1$, $L$ and $J_2$, that subsequently switches $J_2$. The critical voltage of the QPSJs are chosen such that the voltage pulse corresponding to flux quantum at $J_2$ can sufficiently drive the QPSJ from its Coulomb blockade state to the conducting state, thereby generating a current pulse of constant area $2e$ at the output. Simulation results of this circuit showing input current pulse, voltage from SFQ loop and the output current pulse from $Q_2$ are shown in Fig. 2.

Fig. 3. Quantized charge current pulse to SFQ voltage pulse conversion circuit designed with an SFQ cell and a QPSJ charge island cell. $I_C(J_1) = I_C(J_2)$, $V_C(Q_1) = V_C(Q_2)$. $I_{bias_1} = I_{bias_2} = 0.7I_C$.

Fig. 4. Simulation results of charge to flux conversion circuit shown in Fig. 3. $I_C(J_1, J_2) = 100\mu A$, $V_C(Q_1, Q_2) = 0.7mV$, $L = 10.4pH$, $C = 0.23pF$. Magnitude of pulse input $V_{in} = 2.8V$. (a) Voltage pulse input to $Q_1$ with high voltage amplitude from $V_{in}$. (b) Current pulse output from charge island formed by $Q_1$, $Q_2$ and $C$ measured at node 1 of Fig. 3. (c) Flux output from the SFQ loop formed by $J_1$, $J_2$ and $L$ measured at node 2 of Fig. 3.

B. Charge to flux conversion circuit

The reciprocal circuit of flux to charge conversion circuit shown in Fig. 1 can be used for charge to flux conversion. The circuit schematic that can achieve such operation is shown in
controls the output current. (e) Current pulse through the QPSJ applied to the junctions single flux quantum. The difference in shape occurs due to with equal areas (under the curve), each corresponding to from the shape of the SFQ pulse observed in Fig. 2(b), but of the SFQ pulse output presented in Fig. 4(c) is different simulation results are shown in Fig. 4. We note that the shape Fig. 3, with the parameters identical to the circuit in Fig. 1. The is high measured at node 2 of Fig. 5.

Fig. 6 with the parameters identical to the circuit in Fig. 1. The simulation results are shown in Fig. 6. We note that the shape of the SFQ pulse output presented in Fig. 3(c) is different from the shape of the SFQ pulse observed in Fig. 2(b), but with equal areas (under the curve), each corresponding to single flux quantum. The difference in shape occurs due to the differences in the current pulses (magnitude and duration) applied to the junctions J1 in each circuit. This also explains the different SFQ pulse shapes that will be shown in the various other circuits discussed in this paper. Furthermore, the current pulse output from the charge island corresponding to quantized charge of 2e is not sufficient to switch large JJs of critical current of 100µA. Therefore, an input pulse of higher voltage amplitude is used to generate a charge pulse corresponding to ~1000 Cooper pairs, which is sufficient to induce an SFQ pulse at the output for circuit components with the specified parameters. Preliminary simulation results show that, in order to generate a single SFQ pulse output with only a single Cooper pair pulse input, a JJ with a considerably smaller critical current (i.e. up to a few micro-amperes) and a QPSJ with a larger critical voltage (i.e. several hundred milli-volts) are necessary. Practical realization of similar circuits may be challenging with existing technologies, but may be possible with the development of suitable devices or circuits (i.e., with QPSJ-based current amplification). We note that circuits such as these can assist with moving information forward in digital circuits.

C. Control gate

The signal flow to the output of the conversion circuits can be controlled using a signal input through a QPSJ similar to control/buffer circuit from [15] resulting in a similar operation. An example control circuit is shown in Fig. 5. The JJs J1, J2, QPSJs Q2, Q3, along with the inductor L and capacitor C together form the flux to charge conversion circuit shown in Fig. 1. An additional QPSJ Q1 is included along with a step
D. Fan-out circuits

Fan-out circuit schematic is useful to drive several gates with charge/flux input connected to a flux/charge outputs. Conversion from flux to charge and vice versa enables using a single input to drive several outputs without decrease in the pulse amplitudes. Furthermore, it is possible to split the input to either charge or flux output in the same circuit. These two operations are demonstrated in the circuits below.

1) SFQ input splitter to multiple quantized charge outputs: The circuit shown in Fig. 9 can be used to split an SFQ pulse input to three quantized charge outputs. This operation can be extended to a higher number outputs by including more charge islands at the output of SFQ loop. Furthermore, there are no restrictions on the junction parameters irrespective of the number of outputs when the islands are biased with sufficient voltage. This is because the voltage drop at node 1 of Fig. 7 due to leakage current through connected charge islands is negligible. The simulation results of the circuit shown in Fig. 7 are shown in Fig. 8. The reciprocal circuit operation, i.e. from charge input to several flux outputs is possible provided the critical currents of JJs are significantly lower (i.e. on the order of a few micro-amperes). Practical realization may be challenging with present technologies, as mentioned in Section II.B., without internally amplifying the charge input.

2) SFQ input splitter to SFQ and charge quantum output splitter: The circuit shown in Fig. 9 can be used to split a single SFQ pulse input to an SFQ pulse output and a quantized charge pulse output. Simulations results illustrating this operation are shown in Fig. 10.

III. LOGIC CIRCUIT EXAMPLE

A two input XOR gate can be implemented using two flux to charge conversion circuits combined with control gates in parallel. Four inputs are applied to the SFQ cells at junctions J1 and J3, and at the junctions Q1 and Q4. The input 1 at junction J1 and the input at Q4 are high at the same time, and the input 2 at J3 and the input at Q1 are high at the same time. This is illustrated in the circuit shown in Fig. 11 and the corresponding simulation results are shown in Fig. 12. During practical implementation, same input signals can be used in these cases with appropriate charge/flux conversion circuits. When both the inputs are '1', QPSJs Q1 and Q4 are switched, therefore the signals generated in both SFQ cells do not travel into the QPSJ charge islands. This results in the output '0'. When only one of the inputs is '1', the SFQ pulse generated in the JJ corresponding to that input is converted to quantized charge at the corresponding island, generating the output '1'. The output is '0' when both the inputs are '0', as none of the junctions are switched, resulting in no SFQ pulses.
and possible solutions may only be evident after sufficient investigation through experiments.

V. Conclusion

A new family of circuits is introduced that combines the SFQ operation of JJs and quantized charge operation of QPSJ based circuits to perform digital logic. These circuits provide an alternative way to perform logic operations that may significantly simplify the design when compared to JJ-based logic families, therefore may improve flexibility when these circuits are scaled to peta and exa-scale computers. Flux to charge conversion circuits and vice versa are presented that can be interfacing circuits between JJ and QPSJ based logic circuits. Logic operations such as an inverter and fan-out to multiple outputs are demonstrated as examples to illustrate the applications of these logic circuits. However, substantial developments in technology are required for physical realization of single QPSJs that exhibit these properties, as well as in testing the circuits discussed in this paper.

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