A Device Design for 5 nm Logic FinFET Technology
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ABSTRACT
In this paper, we proposed a 5 nm FINFET device, which is based on typical 5 nm logic design rules. We have performed an optimization on the process parameters and iterate through device simulation with the consideration of current process capability. Based on our preferred device architecture, we provide our process key dimensions, and simulated device DC/AC performance, and some parasitic parameters. As a part of the final evaluation, Ring Oscillator (RO) simulation result has been checked, which demonstrates that the Performance Per Area (PPA) is close to industry reference 5 nm performance.

INTRODUCTION
As MOSFET scales down, the conventional planar transistor architectures have already reached the fundamental material and process technology limits. Besides, as the size decreases, the device will suffer from the Short Channel Effect (SCE), which can result in severe leakage problem and mobility degradation, so that the effective drive current will drop. The threshold voltage (Vt) will also roll-off. Thus, a high channel doping to control the leakage current is required. However, it has major disadvantages of lower carrier mobility, higher tunneling effect, more degradation in subthreshold performance, and larger parasitic capacitance.

Therefore, the development of small devices with high performance becomes more challenging. Innovative three-dimensional (3-D) structures such as double-, triple-, fin-typed, nanosheet, and nanowire Field Effect Transistors (FET) have been of great interests. FinFET (Figure 1) is one of the most promising device structures to address short-channel effects and leakage issues in deeply nano-scale transistors. FinFET structure mitigates these problems at low channel doping conditions, which also minimizes variations of the Vt, reduces subthreshold leakage current, keeps high carrier mobility, and enhances the drive current. Thus the FinFET structure can be scaled down to 22 nm and beyond. \[1-3\]

![Figure 1. Schematic of FINFET Structure](image)

In this paper, we have developed a 5 nm FINFET structure with TCAD simulation support. In details, we will propose our development procedure, introduce our process optimization (Fin loop), and present a list of key dimensions, and simulated device performance.

DEVICE DEVELOPMENT PROCEDURE
Firstly, we introduce our 5 nm development procedure shown in Figure 2. In the beginning, we set up our device targets through co-work with IMEC and material path-finding study, and then determine the architecture and process conditions. We perform the TCAD simulation with all these conditions ready and get the initial result. Next, combining the above simulation result with Middle-Of-the-Line (MOL) & Back-End-Of-The-Line (BEOL) extracted parasitic parameters, we extract the SPICE model parameters, and take the result into Ring Oscillator (RO) simulation. If the Performance Per Area (PPA) can meet our initial target, then we extract our device data and curves; if not, then as a learning circle, we will continue to optimize our simulation conditions.

![Figure 2. 5 nm device development procedure](image)
PROCESS SIMULATION OF 5nm FINFETS

The Synopsys Sentaurus TCAD simulator was used to perform 3-D simulations, which included the density gradient (DG) solver model with quantum effects. In order to take the high doping concentration of the source and drain region, Band Gap Narrowing (BGN) model was comprised. For the accuracy of the off state current, the Band-To-Band Tunneling (BTBT) model and concentration-dependent Shockley-Read-Hall (SRH) model were considered. The mobility model used in the device simulation were Inversion and Accumulation Layer (IAL) model; Thin layer (TL) model for low-field mobility modulated as very thin Si thickness; ballistic mobility model for compensating small gate-length (below 10 nm); and Matthiessen’s rule mobility model including surface acoustic phonon scattering, surface roughness scattering, and bulk mobility with doping-dependent modification effect. High Field Saturation model was also included in this simulation because the carrier drift velocity is no longer proportional to the electric field. \cite{3}

Figure 3 illustrates the device architecture of the simulated FinFET and cross-section view of the device doping profile.

![Device Architecture](image)

In this simulation, a Fin pitch of 24 nm, a Poly pitch of 50 nm, and a total gate length (LG) of 19 nm have been adopted. We set the top fin-width $W_{\text{top}} = 5$ nm and the fin-height (FH) equal to 50-55 nm, the Fin angle=$89^\circ$ as a standard device; (SiO$_2$+HfO$_2$) were considered as the gate oxide materials and low K dielectric film was used as spacer material to reduce parasitic capacitance. Total spacer length of 8 nm was used. The Epitaxial doping concentration was around $1.0E21$ in the Source/Drain (S/D) region. Around 15 nm contact (CT) dimension was applied. The key dimensions of different parameters for the simulated device are listed in Table I.

| Parameter               | Unit  | Value |
|-------------------------|-------|-------|
| Gate Length             | nm    | 19    |
| Fin Pitch               | nm    | 24    |
| Poly Pitch              | nm    | 50    |
| TFin                    | nm    | 2     |
| EFln                    | nm    | 50-55 |
| Afin                    | nm    | 8     |
| Gate Oxide Thickness    | nm    | 7/12  |
| Spacer Thickness        | nm    | 8     |
| Spacer Dielectric       | nm    | 4.4   |
| Epi Trench Depth        | nm    | 50-50 |
| Source/Drain Spacing    | nm    | 90    |
| CT                      | nm    | 12-19 |

Table I. Process key dimensions used in the simulation

SIMULATION RESULT

In this section, we present our simulated device DC/AC performance in Table II, which indicates that the Drain Induced Barrier Lowering (DIBL) is around ~30mV, Subthreshold Slope (SS) is around 72.7 mV/decade and 67.2 mV/decade for NMOS and PMOS respectively, which are comparable with industry reference performance and demonstrate that our short channel effect has been controlled well \cite{4,6}.

The parasitic parameters, like $R_{\text{ext}}/R_{\text{channel}}$ and capacitance are also acceptable, and further improvement is ongoing.

| Parameter                | UNIT  | Value |
|--------------------------|-------|-------|
| DC Performance           |       |       |
| Vth                      | mV    | 0.128 |
| Ld                        | mV    | 72.7  |
| SS                        | mV/dec| 67.2  |
| Eoff                      | mV    | 41.03 |
| Parasitic Parameters     |       |       |
| Cgd                      | nm/Fin| 0.022 |
| Cgd (Extraction)         | nm/Fin| 0.029 |
| Cgd (Total)              | nm/Fin| 1515  |
| Cgd (Surface)            | nm/Fin| 1859  |

Table II. The simulated device DC/AC performance result

Figure 4 and Figure 5 show the Id-Vd, Id-Vg, Cgg, Cgd curves for the NFET and PFET, respectively.
PROCESS OPTIMIZATION

In the development process, we have done a lot of experiments by simulation. In this chapter, we focus on the analysis of fin loop process optimization.

We set the top fin width $W_{\text{top}} = 5 \text{ nm}$, the fin-height (FH) equal to 50 nm and the gate length $L_{G} = 19 \text{ nm}$ as a standard device. The tapered fin is tilted with an angle of $89^\circ$. Then, we have varied the parameters, such as fin height (FH), fin width ($W_{\text{top}} + W_{\text{bottom}}$), and only $W_{\text{top}}$ to evaluate the impact of these parameters. Afterwards, we analyze the physical properties of the device to understand the behavior and characteristics.

In Figure 6, by increasing the fin-height from 40 nm to 60 nm, it can enhance the on-state current with off current slightly increased, the $I_{\text{eff}}$ improved $\sim 56\%$ and $\sim 43\%$ for NFET and PFET respectively. This strategy is quite effective to enhance the performance, but it will be very difficult to fabrication because the aspect ratio becomes very high, not easy for production $[3]$.

The control of the fin width is essential at a given technology node because the width greatly affects the device performance. The widening of the fin can improve the saturation current. However, it may not be a good choice because a wider fin will make a larger cross section device area for source and drain epitaxy, which will induce more leakage thus may result in the severe short channel effect $[3]$, as Figure 7(a) shows. In Figure 8, we only enlarge $W_{\text{top}}$ ($W_{\text{bottom}}$ is fixed), which demonstrates that the $I_{\text{off}}$ will reduce significantly. This phenomenon reversely verifies that most of the leakage current comes from the fin bottom area. And the current density distribution under off-state condition which shows in Figure 9 has also proved this behavior, so smaller $W_{\text{bottom}}$ and straight Fin profile are preferred.
Considering all above, and to enhance saturation current (see Figure 7(b)), we finally set FH=50 nm, \( W_{top} = 5 \text{ nm} \) and 89° as a typical device fin size.

**RO PPA VERIFICATION**

Finally, to have a comprehensive understanding, we make the RO simulation. In Figure 10, it seems our 5 nm RO PPA performance (red line) is close or even better than published reference 5 nm performance \(^{[5-6]}\). (The 5nm PPA curve of industry reference 1 (Ref 1) is calculated with which published 40% speed gain and 65% power reduction from 14 nm to 7 nm, 15% speed gain and 30% power reduction from 7 nm to 5 nm, respectively; reference 2 (Ref 2) is published only for 5 nm RO performance).

**CONCLUSION**

Product innovation has been the driving force behind the semiconductor industry growth in the past years. Especially with 5G deployment starting in 2019, mobile System on Chip (SoC), High Performance Computing (HPC), and Artificial Intelligence (AI)/Data-center are propelling another period of sustained growth in the next decade. Advanced CMOS logic technology has been the key enabler for semiconductor product innovations. 5 nm technology is one of such advanced logic technology platforms. \(^{[4]}\)

In this paper, we have performed a simulation to study a typical 5 nm FinFET device structure and performance. The result indicates that our device performance is comparable with published reference performance and the short channel effect is controlled well; our ring oscillator simulation demonstrates that the PPA is also close to industry reference. We believe that the FinFET device still has the ability to extend to 5 nm technology node with continued performance gain.

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