Design and error-rate evaluation of RSFQ logic gates comprising a toggle storage loop

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Abstract. We propose an RSFQ digital cell with a toggle storage loop structure for logical NOT operation. Logical NOT operation is a fundamental function of digital circuitry, and hence, it had better be realized with less devices. We demonstrate a simpler and area-halved NOT gate designed as a 40 × 80 μm² cell, which follows to cell-based design methodology. Test circuits were fabricated using a 2.5 kA/cm² Nb integration process. Measurements were executed in a liquid helium bath. We confirmed that the NOT gate comprising a toggle storage loop worked correctly. The error-rate of the NOT gate was less than 8.33 × 10⁻⁶ in the bias voltage range from 2.111 to 3.165 mV, which corresponded to the bias margin from 84.4% to 126.6% of the nominal bias voltage (2.5 mV). We also present that NOR and NAND logic gates can be configured using a toggle storage loop.

1. Introduction
Single-Flux-Quantum (SFQ) circuits are expected to next-generation digital systems because of their high-speed switching and low power dissipation [1]. Several RSFQ-technology-based applications [2, 3] that take advantages of these features have been developed in recent years. There is another advantage that Josephson junctions constructing RSFQ circuits generate precise voltage determined by the physical constant $\Phi_0$ ($2.07 \times 10^{-15}$ Wb) and a repetition frequency of SFQ pulses. Therefore, RSFQ circuits can be also applied for AC voltage standards using digital-to-analog converters based on frequency modulation of SFQ pulse trains [4, 5].

These RSFQ circuits are often designed by cell-based design techniques. The CONNECT library is an example [6]. Cell libraries for RSFQ circuits include various logic cells with Josephson transmission lines (JTLs), logic gates, and flip-flops. Large and complex RSFQ circuits are constructed by combining such cells each of which has a simple function. On the other hand, some problems for circuit operation arise in large-scale RSFQ circuits. Since RSFQ circuits are driven by supplying DC bias current, large bias currents or unexpected magnetic field affect dynamics of the circuits [7]. For example, affected timing parameters make logic cells in wrong operation.

In order to relieve these influences, simplified circuit schematics are preferred. We especially focused on a NOT logic cell, which had rooms for improvement, in the cell library. In this work, we introduce a unique configuration presented in literature [8], where a superconducting loop structure similar to a SQUID is used to switch SFQ propagation. By using this storage loop structure, we realize an RSFQ NOT gate. We also evaluate error-rates of the logic gates in experiments.
2. Design and numerical evaluation of NOT gate comprising a toggle storage loop

Figure 1 shows an equivalent circuit of the RSFQ-NOT gate comprising a toggle storage loop. When an SFQ is transferred to the input terminal, it switches $J_1$ and $J_3$, and be stored in the toggle storage loop including $J_5$, $L_{10}$, $L_9$, $J_4$, $L_7$, and $L_8$. After an SFQ is stored in the loop, an input SFQ from the clock terminal switches $J_4$ and the stored SFQ is annihilated. This operation expresses that the digital "1" input makes the digital "0" output. If the storage loop is empty, an SFQ fed to the clock terminal goes to the output terminal without switching $J_4$. When $J_6$ is switched, an SFQ flows back toward the input terminal. Then, $J_3$ works as an escape junction and the SFQ exits from the circuit. It means that the digital "0" input makes the digital "1" output. In this way, NOT operation is realized.

![Equivalent circuit of the RSFQ-NOT gate with a toggle storage loop.](image)

Figure 1. Equivalent circuit and parameters of the RSFQ-NOT gate with a toggle storage loop. All Josephson junctions are shunted to make the McCumber parameter $c$ be 0.89. Other parameters are as follows. $L_1 = L_4 = 0.83 \text{ pH}$, $L_2 = 2.33 \text{ pH}$, $L_3 = 3.31 \text{ pH}$, $L_5 = 3.55 \text{ pH}$, $L_6 = 2.74 \text{ pH}$, $L_7 = 8.97 \text{ pH}$, $L_8 = 1.01 \text{ pH}$, $L_9 = 0.50 \text{ pH}$, $L_{10} = 0.66 \text{ pH}$, $L_{11} = 2.51 \text{ pH}$, $L_{12} = 5.10 \text{ pH}$, $L_{13} = 3.24 \text{ pH}$, $I_{c1} = 210 \mu\text{A}$, $I_{c2} = 125 \mu\text{A}$, $I_{c3} = 104 \mu\text{A}$, $I_{c4} = 134 \mu\text{A}$, $I_{c5} = I_{c6} = 100 \mu\text{A}$, $I_{c7} = 182 \mu\text{A}$, $R_1 = 21.36 \Omega$, $R_2 = 22.08 \Omega$, $R_3 = 12.85 \Omega$.

Circuit simulation results are presented in figure 2, where a 5 GHz clock signal is assumed. We used the Josephson simulator JSIM [9] for simulation. The NOT logic operation was confirmed in synchronization with the clock pulses. The critical margins for each elements and bias margin gate are presented in figure 3. These margins were calculated using the optimization tool SCOPE2 [11]. The lowest value of the critical margins is ±45.3% and the bias margin ranges from 67.1% to 129.7% of the nominal bias voltage (2.5 mV). These values are acceptable for use in large-scale circuits.

The conventional NOT gate cell in the CONNECT library [6] and the NOT gate cell are compared in table 1. The NOT gate comprising a toggle storage loop has reduced the number of Josephson junctions from 11 to 7 and halved the cell area. Besides, the conventional NOT gate requires the initialization where the first clock is used to store an SFQ in the storage loop, whereas the NOT gate comprising a toggle storage loop requires no initialization, that is, it operates normally at the first clock.

3. Experimental results

3.1. Layout and fabrication

We designed the NOT gate comprising a toggle storage loop in a $40 \times 80 \mu\text{m}^2$ cell to fit the CONNECT cell-based design methodology [6]. In CAD layouts, the inductances were extracted using the induction extraction tool InductEX [12]. Test chips were fabricated by using the Nb standard process STP2 [10] of National Institute of Advanced Industrial Science and Technology.
Figure 2. Simulation waveforms of the NOT gate comprising a toggle storage loop.

Figure 3. Critical margins and bias margin of the NOT gate comprising a toggle storage loop.

Table 1. Comparison of the conventional NOT gate cell in the CONNECT library and the NOT gate cell comprising a toggle storage loop.

|                | Conventional NOT cell | this work     |
|----------------|-----------------------|---------------|
| Area occupancy [μm²] | 80 × 80              | 40 × 80       |
| The number of junctions | 11                   | 7             |
| Initialization          | necessary             | unnecessary   |
| Latency [ps]            | 16.1                  | 15.0          |
| Bias margin             | 60.9% to 139.1%       | 67.2% to 129.7% |
| Critical margins        | 70.3% to 114.1%       | 54.7% to 145.3% |

The measurement setup is illustrated in figure 5. DC/SFQ converters, a SFQ/DC converter, and several JTLs were integrated in order to test a cell. We used a 100-fold low-noise preamplifier to observe SFQ/DC output signals on oscilloscope since the SFQ/DC output voltage amplitude was as small as 0.2 mV. Measurements were executed with a test chip cooled in a liquid helium bath. Figure 4 shows a photomicrograph of a fabricated NOT gate cell.

3.2. Low speed measurement
Figure 6 shows the low-frequency measurement results at 1 kHz clock, in which the input data alternating "1" and "0" are used. We confirmed the correct operation where the output data were inversion of the input data fed between clocks.

3.3. Error-rate evaluation
We evaluated the error-rate of the NOT gate comprising a toggle storage loop using the same setup shown in figure 5. Figure 7 shows the bias voltage versus error-rate plotted on a logarithm scale.

Measurement was performed at the input signal rate of 1 Mb/s, while the bias voltage was changed manually. The waveforms on the digital oscilloscope for 120 ms were acquired to determine whether the NOT operation was correct. The error-rate was calculated by dividing the number of error operations by the number of clocks. Since the number of clock signals $1.2 \times 10^5$, the lowest error-rate in this experiment was $8.33 \times 10^{-6}$. 

We confirmed that the measured error-rates were less than $8.33 \times 10^{-6}$ in the bias voltage range from 2.111 mV to 3.165 mV, which corresponded to the relative range from 84.4% to
126.6% of the nominal bias voltage of 2.5 mV. The experimentally obtained bias margin was not as wide as that in calculation shown in table 1. The margin reduction was probably due to incomplete layout design of inductances. Parasitic inductances and thermal noises that had not been taken into account in calculation could also cause margin reduction.

4. Application to other logic gates
In this section, we propose two logic gates, NOR and NAND, comprising a toggle storage loop.

4.1. NOR cell
The NOR gate consists of a confluence buffer and a toggle storage loop. The equivalent circuit of the NOR gate is shown in figure 8. In the left part (the merge section), an SFQ coming from either the Input-A or Input-B terminal is transferred to the right part (the inversion section). It is stored in the toggle storage loop including $J_{11}$ and $J_{12}$ through $J_{12}$. The inversion section has the same structure as the NOT gate in figure 1. $J_9$ plays two important roles for the correct NOR operation: it prevents an SFQ from flowing backward into the merge section, and it also prevents the second input SFQ from entering the inversion section. As a result, either or both input SFQ signals to the Input-A and/or Input-B is stored in the toggle storage loop and makes the output signal "0". Otherwise, the output becomes "1".

Figure 8. Equivalent circuit and parameters of the NOR gate comprising a toggle storage loop. All Josephson junctions are shunted to make the McCumber parameter $\beta_c$ be 0.89. Other parameters are as follows. $L_1 = L_5 = L_{14} = 0.83\,\text{pH}$, $L_2 = L_6 = 1.90\,\text{pH}$, $L_3 = L_7 = 2.28\,\text{pH}$, $L_4 = L_8 = 1.23\,\text{pH}$, $L_9 = 0.01\,\text{pH}$, $L_{10} = 4.32\,\text{pH}$, $L_{11} = 1.66\,\text{pH}$, $L_{12} = 1.42\,\text{pH}$, $L_{13} = 3.50\,\text{pH}$, $L_{15} = 1.50\,\text{pH}$, $L_{16} = 3.33\,\text{pH}$, $L_{17} = 8.97\,\text{pH}$, $L_{18} = 1.01\,\text{pH}$, $L_{19} = 0.63\,\text{pH}$, $L_{20} = 0.59\,\text{pH}$, $L_{21} = 1.37\,\text{pH}$, $L_{22} = 5.50\,\text{pH}$, $L_{23} = 1.51\,\text{pH}$, $I_{c1} = I_{c4} = 200\,\mu\text{A}$, $I_{c2} = I_{c5} = 195\,\mu\text{A}$, $I_{c3} = I_{c6} = 148\,\mu\text{A}$, $I_{c7} = 165\,\mu\text{A}$, $I_{c8} = 261\,\mu\text{A}$, $I_{c9} = I_{c12} = I_{c13} = 100\,\mu\text{A}$, $I_{c10} = 196\,\mu\text{A}$, $I_{c11} = 143\,\mu\text{A}$, $I_{c14} = 208\,\mu\text{A}$, $R_1 = R_2 = 8.34\,\Omega$, $R_3 = 9.00\,\Omega$, $R_4 = 13.28\,\Omega$, $R_5 = 16.66\,\Omega$, $R_6 = 17.00\,\Omega$

The NOR gate operation was simulated with 5 GHz clock. One of the simulation results is shown in the figure 9. Correct NOR operation is confirmed.

4.2. NAND cell
The NAND gate cell can also be designed using two sub-circuits combining a toggle storage loop with a modified confluence buffer. Figure 10 shows an equivalent circuit of the NAND gate. The $J_2$-$J_3$-$J_7$ and $J_5$-$J_6$-$J_7$ loops are designed to store an SFQ by making the inductance value of $L_{10}$ and the critical current of $J_7$ larger than the NOR cell. Only the doubled loop current generated
by two SFQ signals from both the Input-A and Input-B makes $J_7$ switch. That is, the input signal set of “11” transfers an SFQ to the toggle storage loop, resulting in the NOT operation described above. For the input signal sets of “10” and “01”, either $J_2$-$J_3$-$J_7$ or $J_5$-$J_6$-$J_7$ loop stores an SFQ. Then, a clock signal is transferred to both the output terminal and the input terminals, resulting in the output signal of “1” and the annihilation of the SFQ stored at the Input-A or Input-B. To perform this operation, $J_9$ used in the NOR gate is removed.

The simulation waveforms at 5 GHz clock are shown in figure 11, which demonstrates that the NAND gate comprising a toggle storage loop works correctly.

**Figure 10.** Equivalent circuit and parameters of the NAND gate comprising a toggle storage loop. All Josephson junctions are shunted to make the McCumber parameter $\beta_e$ be 0.89. Other parameters are as follows. $L_1 = L_5 = L_{14} = 0.83$ pH, $L_2 = L_6 = 1.85$ pH, $L_3 = L_7 = 2.64$ pH, $L_4 = L_8 = 1.24$ pH, $L_9 = 0.01$ pH, $L_{10} = 8.72$ pH, $L_{11} = 1.64$ pH, $L_{12} = 1.45$ pH, $L_{13} = 3.07$ pH, $L_{15} = 1.54$ pH, $L_{16} = 3.88$ pH, $L_{17} = 8.95$ pH, $L_{18} = 1.01$ pH, $L_{19} = 0.63$ pH, $L_{20} = 0.59$ pH, $L_{21} = 1.38$ pH, $L_{22} = 6.68$ pH, $L_{23} = 1.49$ pH, $I_1 = I_{c4} = 176$ μA, $I_{c2} = I_{c5} = 182$ μA, $I_{c3} = I_{c6} = 139$ μA, $I_{c7} = 330$ μA, $I_{c8} = 203$ μA, $I_{c10} = 138$ μA, $I_{c11} = 143$ μA, $I_{c12} = I_{c13} = 100$ μA, $I_{c14} = 189$ μA, $R_1 = R_2 = R_3 = 8.34$ Ω, $R_4 = 20.50$ Ω, $R_5 = 16.66$ Ω, $R_6 = 12.27$ Ω

The simulation waveforms at 5 GHz clock are shown in figure 11, which demonstrates that the NAND gate comprising a toggle storage loop works correctly.

5. Conclusion
The area-halved RSFQ-NOT gate cell comprising a toggle storage loop and its application were reported. The NOT gate comprising a toggle storage loop was designed with a simpler schematic with an area of $40 \times 80$ μm². The error-rate of a NOT gate evaluated in experiments was less than $8.33 \times 10^{-6}$ at the bias voltage range between 84.4% and 126.6% of the nominal value.
Figure 11. Simulation waveforms of the NAND gate comprising a toggle storage loop.

(2.5 mV). We also designed NOR and NAND gates by combining a toggle storage loop structure and a modified confluence buffer. Their functions were numerically demonstrated.

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