Low quiescent current capacitor-less LDO regulator with high slew rate super class AB CMOS OTA

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Abstract. This paper presents a low quiescent current capacitor-less low-dropout regulator (LDO) with high slew rate super class AB CMOS operational transconductance amplifier (OTA). The OTA of this design is based on the combination of class AB differential input stages and local common-mode feedback (LCMFB) which provides additional dynamic current boosting, increased gain-bandwidth (GBW) product and slew rate (SR). LCMFB is applied to various class AB differential input stages, leading to different class AB OTA topologies. The design also uses dynamic charging transistor (DCT) to enhance the transient characteristics of the circuit. The presented LDO is fabricated in a 0.18 um standard CMOS process. The circuit consumes a quiescent current of 10 uA at no load, regulating the output at 1.0V with maximum output current of 100mA from a voltage supply of 1.2V. It achieves full range stability from 1mA to 100mA load current at a maximum 100pF load capacitor.

1. Introduction
Power management unit is an important part in the modern electronic systems. The low-dropout regulator is widely used to provide clean and ripple free power supplies in battery-powered and portable applications. To enable fully integrated for system-on-chip, the capacitor-less low-dropout regulator (LDO) have been widely researched [1]. Low power consumption is a very important parameter for biomedical implanted electronics and wearable devices. To prolong the battery life, high power efficiency is required, which is indicated by a low quiescent current and low dropout voltage (VDO). However, since the low quiescent current affects the slew rate at the gate of the power transistor, it is necessary to consider the use of an amplifier with a higher slew rate in designing LDO. So this paper designed LDO with high slew rate OTA and transient processing. The structure and implementation of the transistor circuit will be described in Section 2. Section 3 demonstrates the small-signal analysis of the LDO. The simulation results are shown in the section 4, and the section 5 provides the conclusions of this paper.

2. Proposed LDO Architecture
The transistor-level schematic of the proposed LDO is shown in Figure 1, where M1-M8 with adaptive bias circuit (M9-M12) and LCMFB (R1-R2) constitute a super class AB CMOS OTA. Due to the LCMFB, a boosted dynamic current is generated in its active load. The adaptive bias circuit significantly improve drive ability of OTA, where \( I_B = 1 \) uA. \( M_{DCTn} \) and \( M_{DCTp} \) form the dynamic charging transistors (DCT). \( M_P \) is power transistor (PT), and the resistor feedback network is implemented by \( R_3-R_4 \). \( C_{out} \) is ranged from 0-100 pF in this study.
2.1. OTA
When LDO presented in Figure 1, works, the OTA will generate the differential signal \( v_{id} \), which will then generate the differential current \( I_d = I_1 - I_2 \), \( I_R = I_d / 2 = (I_1 - I_2) / 2 \) will flow through resistor \( R_{1,2} \). Current through \( M_6 \) and \( M_7 \) will be the common-mode current \( I_{cm} = (I_1 - I_2) / 2 \). The above X, Y, Z nodal voltages will be expressed:

\[
\begin{align*}
V_Z &= V_{th} + \frac{2l_{cm}}{\sqrt{\beta_{6,7}}}, \\
V_X &= V_Z + \frac{R_{id}I_d}{2}, \\
V_Y &= V_Z - \frac{R_{id}I_d}{2}.
\end{align*}
\]

(1)

Where \( V_{th} \) and \( \beta_{6,7} = \mu_n C_{ox} W/L \) are the threshold voltage and transconductance factor of transistors \( M_6 \) and \( M_7 \). The first case, a large positive voltage swing takes place at node X for \( v_{id} > 0V \), assuming operation in strong inversion and saturation for \( M_5 \), it leads to a current in \( M_5 \):

\[
I_5 = \frac{\beta_5}{2} \left( V_Z + \frac{R_{id}I_d}{2} - V_{th} \right)^2 = \frac{\beta_5}{2} \left( \frac{2l_{cm}}{\sqrt{\beta_{6,7}}} + \frac{R_{id}I_d}{2} \right)^2.
\]

(2)

Whereas the large negative swing at node Y strongly decreases current through transistor \( M_8 \) below quiescent current \( I_B \). Thus, the output current is \( I_{out} = I_5 - I_0 \approx I_5 \). The second case, a large negative voltage swing takes place at node X for \( v_{id} < 0V \), then \( I_d = I_1 - I_2 < 0A \), the large positive swing at node Y yields a large current in \( M_8 \), given by

\[
I_0 = \frac{\beta_6}{2} \left( V_Z - \frac{R_{id}I_d}{2} - V_{th} \right)^2 = \frac{\beta_6}{2} \left( \frac{2l_{cm}}{\sqrt{\beta_{6,7}}} - \frac{R_{id}I_d}{2} \right)^2.
\]

(3)

In this case \( I_{out} = I_5 - I_0 \approx -I_B \). Combine the above two situations, when \( v_{id} \neq 0V \), a general expression for the output current is

\[
I_{out} = I_5 - I_0 \approx \pm \frac{\beta_{5,6}}{2} \left( V_Z + \frac{R_{id}I_d}{2} - V_{th} \right)^2 \quad \text{or} \quad \pm \frac{\beta_{5,6}}{2} \left( \frac{2l_{cm}}{\sqrt{\beta_{6,7}}} - \frac{R_{id}I_d}{2} \right)^2,
\]

(4)

where \( I_{out} > 0A \), when \( v_{id} > 0V \) and \( I_{out} < 0A \), when \( v_{id} < 0V \).

The adaptive biasing technique of \( M_9 = M_{12} \) and a current source which is shown Figure 1. are adopted Flipped Voltage Followers (FVF). Its role is actually to form two level shifting. FVFs have a low output resistance. Transistors \( M_{10} \) and \( M_{11} \) in the FVF cells provide shunt feedback, and the FVF cell forms a two-pole negative feedback loop. If transistors \( M_1, M_2, M_3, M_4 \) are matched, then the quiescent in \( M_1 \) and \( M_2 \) is the well-controlled bias current \( I_B \) of the FVFs. So the current \( I_1 \) and \( I_2 \) will be

\[
I_1 = \frac{\beta_{1,2}}{2} \left( \frac{2l_B}{\sqrt{\beta_{1,2}}} + V_{ad} \right)^2 \quad I_2 < I_B \quad V_{id} > 0,
\]
\[ I_2 = \frac{\beta_{l2}}{2} \left( \frac{2B}{B_{v2}} - V_{id} \right)^2 \quad I_1 < I_B \quad V_{id} < 0. \]  

(5)

For instance, when \( V_{in} \) decreases, voltage at the source of \( M_1 \) decreases by the same amount whereas the source voltage of \( M_2 \) stays constant. Therefore, current through \( M_2 \) increases whereas current through \( M_1 \) decreases. Very low output impedance DC level shifters are required in order to drive the low-impedance source terminals of transistors \( M_1 \) and \( M_2 \). According to Formula 5, currents \( I_1 \) and \( I_2 \) are not bounded by \( I_B \), showing the class AB operation of the circuit. The common-mode output current \( I_{cm} \) is signal-dependent, another characteristic of class AB topologies. Therefore, the AC small-signal differential current of the input stage is

\[ I_d = I_1 - I_2 \approx \left( 1 + \frac{g_{m10,11}^{-1}}{g_{m10,11}+1} \right) g_{m1} v_{id} \approx 2g_{m1} v_{id}. \]  

(6)

Combine LCMFB technique and the adaptive biasing technique, about the overall amplifier structure that OTA structure as shown in Figure 1. For the and positive \( v_{id} \), from Formula 5, \( I_d \approx I_1 \approx (\beta_{1,2} \approx 2) v_{id}^2 \) and \( I_{cm} \approx I_1 / 2 \). For large negative \( v_{id} \), \( I_d \approx -I_2 \approx -(\beta_{1,2} \approx 2) v_{id}^2 \) and \( I_{cm} \approx I_2 / 2 \). Using Formula 4, the output current is given by

\[ I_{out} \approx \pm \frac{\beta_{B,2}}{2} \left( \frac{B_{v2}}{2B_{v6}} |v_{id}| + \frac{R_3\beta_{B,2}v_{id}}{4} v_{id}^2 \right)^2. \]  

(7)

Formula 7 fully demonstrates that the OTA designed in this paper has the effect of increasing the slew rate and GBW. It is clear that for a large \( v_{id} \) the output current increases with \( v_{id}^4 \), enhancing quadratically the current boosting provided by the class AB input stage. From Formula 4, the factor \( g_{mB} \) \( R_{1,2} \) of the \( \omega_T \) is increased due to the LCMFB technique.

2.2. DCT

The DCT mentioned in this paper is shown in Figure 1. The DCT consists \( M_{DCTn} \) and \( M_{DCTp} \), which form fast nonlinear feedback loops to generate large extra charge (discharge) current \( I_{ch} \) (\( I_{dch} \)) only in large transient steps when the DCT is turned on. When the load current suddenly produces a large current change, then a large charge or discharge current is also generated across the gate capacitance of the power transistor. At this point, a voltage change occurs at the input stage of the amplifier, so node a, b become the control voltage of DCT, this is, the node a, b voltage is a natural sensing transient voltage. When the load current changes from light load to heavy load, the output voltage will suddenly decrease, and the feedback voltage will decrease accordingly. At this time, \( V_n \) will decrease, this is the control voltage that acts as a DCTp that turns the DCTp on, which is originally switched off in a steady state, so that the power transistor is quickly charged. Similarly, when the load current changes from heavy load to light load, the output voltage will increase, and at this time, the voltage at node b will increase, which causes the DCTn transistor to open for rapid discharge. However, for the above situation, the voltage of the DCT transistor select the appropriate trigger voltage to ensure the overall performance of the circuit, and select the minimum size to ensure that the DCT has the smallest parasitic capacitance.

![Figure 2. Small signal model of the proposed LDO](image)

3. Small-signal Analysis

The small-signal model of proposed LDO is shown in Figure 2. in which \( g_{ml}, R_{di}, \) and \( C_{di} \) are the transconductance, output resistance, and capacitance at the drain terminal of transistor \( M_i \), respectively.
Also $R_g - C_g$ and $R_{out} - C_{out}$ are the equivalent resistance and capacitance at the gate and drain terminals, respectively, of $M_p$. When an AC small-signal differential voltage $v_{id}$ is sensed by the OTA, and the OTA generates corresponding currents $i_g = i_z = k g_{m1,2}v_{id}/2$. Assuming $R_{1,2} < r_{o6,7}$, where $r_{o6,7}$ is the small-signal drain-source resistance of $M_6$ and $M_7$, then the current flowing through the resistor $R_1$, $R_2$, $i_q = i_1 = i_z$. This is the voltage for the node $X$, $Y$, $V_X = -V_Y = R_{1,2}i_R = R_{1,2}k g_{m1,2}v_{id}/2$. Therefore, $V_Z = 0V$ and node $Z$ becomes an ac virtual ground, thus eliminating the influence of capacitance of the gate and source of the $M_6,7$. Therefore, the loop transfer function of this model is shown in Formula 8\[1\],

\[
H(s) = \frac{-A_0(1-(s/z_1))}{(1+(s/p_1))(1+(s/p_2))(1+(s/p_3))}.
\]  

Model DC gain and pole and zero are shown in Formula 9,10.

\[
A_0 = (g_{m1}R_Xg_{m4,5R_g} + g_{m2}R_Yg_{m8R_g})g_{mp}R_{out} \approx 2g_{m1}R_Xg_{m8R_g}g_{mp}R_{out}.
\]  

\[
p_1 = \frac{1}{R_gC_g}, p_2 = \frac{1}{R_{out}C_g}, p_3 = \frac{1}{R_XC_X}, z_1 = \frac{g_{mp}}{C_{gdp}}.
\]  

Considering $R_X = R_Y \approx r_{o1,2} \parallel r_{o6,7} \parallel R_{1,2}$, assuming $R_{1,2} < r_{o6,7}$, then $R_X \approx R_{1,2}$, $R_g = r_{o4} \parallel r_{o8}$, $R_{out} = 1/g_{m2} \parallel r_{op} \parallel R_{f1}$. If $C_g, C_{out} \ll C_X, C_{gdp}$, the pole $p_3$ and the zero $z_1$ will be located at frequencies higher than two other poles and unity gain frequency which is shown the Formula 11. The Formula 11 is assuming that the pole 2 is located after $\omega_T$.

\[
\omega_T = A_0|p_1| = \frac{2g_{m1}g_{m8}R_{1,2}g_{mp}R_{out}}{C_g}.
\]  

If the above assumptions are true, this can speculate that the loop phase margin which is given in the Formula 12.

\[
PM = 180° - tan^{-1}\left(\frac{\omega_T}{|p_1|}\right) - tan^{-1}\left(\frac{\omega_T}{|p_2|}\right).
\]  

4. Simulation Results

The proposed LDO is fabricated in a 0.18 um standard CMOS process and has been laid out. The layout is shown as the Figure 3(a). Figure 3(b) shows the simulated open loop AC response of the proposed LDO. The loop phase margin is 50.35 degrees at 1 mA light load and 61.45 degrees at 100 mA heavy load. As it can be seen, even under the worst condition (that is, large output capacitor and light load current) the proposed LDO is stable and has an adequate phase margin.

As shown in Figure 4(b). The post-simulated transient responses for different output capacitors. Similarly, the load current is changed between 1mA to 100mA with the edge time of 1us. When $C_{out}$ changes from 0pF to 100pF, the transient response, undershoot and overshoot of the circuit changes is not obvious. As can be observed from the $I_{ch}$ ($I_{dch}$) waveform in the Figure 4(a). DCT will be fully open in circuit light load and heavy load mutual jump. The recharging current is 23 uA and the discharging current is 12 uA.

In summary, the load regulation of the circuit is 0.14 mV/mA, the line regulation is 4.3 mV/V at the load current is 1mA and 4.4 mV/V at the load current is 100mA. The measured power supply rejection ratio (PSRR) performance of the proposed LDO of -68 and -43.5dB at 1kHz and 10kHz, respectively is achieved by the proposed LDO scheme.

The performance comparison with previously reported LDOs is summarized in Table 1. The figure-of-merit (FOM) in[2], FOM1, FOM2,[3], are adopted to evaluate the different current efficient LDOs. The smaller FOM1 and FOM2 indicate the better performance in terms of the current efficiency and load transient response. $FOM_1 = (k\Delta V_{out}I_Q)/\Delta I_{load}, FOM_2 = (T_{settle}I_Q)/\Delta I_{load}$. 

\[
FOM_1 = \frac{k\Delta V_{out}I_Q}{\Delta I_{load}}, \quad FOM_2 = \frac{T_{settle}I_Q}{\Delta I_{load}}.
\]
Figure 3. (a) Layout of the proposed LDO. (b) Open loop AC response of the proposed LDO.

Figure 4. (a) Dynamic charging transistor transient current for variation on different load current changes. (b) Post-transition simulation.

Table 1 Performance with previously reported LDOs.

| Parameter       | [4]  | [5]  | [6]  | This work |
|-----------------|------|------|------|-----------|
| Simulation type | sim  | sim  | sim  | post-sim  |
| Technology(um)  | 0.11 | 0.18 | 0.065| 0.18      |
| V$_{IN}$(V)     | 2.2  | 1.2  | 1.5-2.5 | 1.2  |
| V$_{OUT}$(V)    | 2.0  | 1.0  | 1.2  | 1.04      |
| Dropout(mV)     | 200  | 200  | 300  | 200       |
| I$_{outmax}$(mA)| 200  | 100  | 10   | 100       |
| I$_{Q}$(uA)     | 41.5 | 100  | 100  | 10.0      |
| C$_{L}$(pF)     | 40   | 100  | 10   | 0-100     |
| T$_{edge}$(us)  | 0.5  | 0.3  | 1    | 1         |
| T$_{settle}$(us)| 0.65 | 1.56 | 1.1  | 2.2       |
| FOM$_{1}$ (V)   | 0.0415 | 0.2000 | 3.0000 | 0.0220  |
| FOM$_{2}$ (ns)  | 0.1349 | 1.5600 | 11.000 | 0.2370  |

5. Conclusion

In this paper, a low quiescent current capacitor-less LDO with high slew rate super class AB CMOS operational transconductance amplifier has been proposed. The DCT effectively reduces overshoot and
undershoot in circuit transient response. The proposed LDO is stable at a load current range from 1mA to 100mA with a maximum allowable $C_L$ of 100pF and without any compensation. It consumes a quiescent current of 10 uA. A settling time of 2.1 us is measured when the load current steps from 1mA to 100mA within 1 us, and the undershoot or overshoot is less than 200 mV.

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References
[1] J. Tang, J. Lee and J. Roh. (2019) Low-Power Fast-Transient Capacitor-Less LDO Regulator with High Slew-Rate Class-AB Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 66(3): 462-466.
[2] J. Guo and K. N. Leung. (2010) A 6-uW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology. IEEE Journal of Solid-State Circuits, 45(9): 1896-1905.
[3] X. Ming, Q. Li, Z. K. Zhou and B. Zhang. (2012) An Ultrafast Adaptively Biased Capacitorless LDO with Dynamic Charging Control. IEEE Transactions on Circuits and Systems II: Express Briefs. 59(1): 40-44.
[4] D. Mandal, C. Desai, B. Bakkaloglu and S. Kiaei. (2019) Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time IEEE Transactions on Circuits and Systems II: Express Briefs, 66(2): 167-171.
[5] X. Ming et al. (2018) A Capacitor-less LDO With Fast-transient Error Amplifier and Push-pull Differentiator. In: 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, pp. 1-5.
[6] X. Tong and K. Wei. (2017) A Fully Integrated Fast-Response LDO Voltage Regulator with Adaptive Transient Current Distribution. In: 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Bochum, pp. 651-654.