Prospects of Terahertz Transistors with the Topological Semimetal Cadmium Arsenide

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Electronic devices that operate at terahertz frequencies will require new materials that exhibit higher carrier velocities than traditional semiconductors. Calculations show that cadmium arsenide, a 3D topological (Dirac) semimetal, is an excellent candidate for field effect transistors that operate at frequencies above 1 THz. Moreover, such transistors have unique advantages that are enabled by the properties of Dirac electrons. These include predictions of an unprecedented linearity of the transconductance and cutoff frequencies over a large operating range and cutoff frequencies that remain above 1 THz at carrier densities as low as $10^{11}$ cm$^{-2}$. The calculations are underpinned by measurements of devices with cadmium arsenide channels. Extremely low contact resistances ($<2 \times 10^{-9}$ Ω cm$^2$), high electron velocities ($>7 \times 10^5$ m s$^{-1}$), and unprecedentedly large current densities (up to 10 A mm$^{-2}$) are demonstrated. Current modulation (>50%) and transconductance already achieved in the early transistors show the potential for large ($>10 \times$) improvements by reducing interface trap densities. The results demonstrate the significant potential of topological semimetals for high-speed transistors operating in the THz regime and open up new opportunities for next-generation RF circuits.

Transistors operating at frequencies in the terahertz (THz) regime are a key requirement for future communication, imaging and sensing applications, such as in next-generation mobile wireless communication systems and autonomous vehicles.[1,2] Terahertz transistors place extreme demands on the channel material. Short gate lengths and high electric fields make intrinsic carrier velocities, rather than low field carrier mobilities, the key to reaching the THz regime. Moreover, the channel material must also accommodate high carrier densities and allow for low contact resistances. While low contact resistances and high velocities have been achieved with III–V semiconductors, the low density of states in the conduction band (‘density of states bottleneck’[3]) severely limits the sheet carrier densities of the transistors. Realization of THz integrated circuits will thus likely require the development of a new generation of electronic materials. One such candidate material is graphene, an atomically thin Dirac semimetal, which is of interest because of its high Fermi velocity.[4–6] To date, however, the performance of graphene transistors has been limited by high contact resistances and extrinsic effects, such as defect scattering.[9]

The discovery of 3D topological semimetals has driven a surge of interest in harnessing their properties.[10–12] Like graphene, they are Dirac materials with intrinsically high carrier velocities. For example, record high Fermi velocities of $2 \times 10^6$ m s$^{-1}$ have been reported for the 3D Dirac semimetal cadmium arsenide (Cd$_3$As$_2$).[13] High-quality thin films of Cd$_3$As$_2$ have been grown by molecular beam epitaxy (MBE) and epitaxial integration of high-mobility Cd$_3$As$_2$ films with III–V semiconductors has been demonstrated.[14–16] Despite this progress, the potential of 3D topological semimetals for high-speed electronics remains underexplored.[17,18]

In this Article, we model the frequency performance of transistors with Cd$_3$As$_2$ channels, using our experimental measurements of contact resistances, carrier velocities and sheet carrier densities as input parameters. We not only demonstrate that Cd$_3$As$_2$ transistors can reach the THz regime but also show that transistors with topological semimetals possess unique properties, such as linearity in frequency performance, that can address major challenges in RF circuit design.

The most important figure of merit of a high-frequency field effect transistor (FET) is its cut-off frequency, $f_C$, which is determined by the gate transit time of the carriers from source to drain, which depends on the velocity of the carriers of the channel material. In addition, THz applications require that the transistor gate length must be highly scaled, which can cause RC time delays to become significant. For the metal-oxide-topological semimetal FETs (MOTFETs) of interest here, an
analytical expression for $f_T$ can be derived from the small circuit model (see, e.g., refs. [19,20]) shown in Figure 1A

$$\frac{1}{2\pi f_T} = \frac{C_{gs}}{g_{m,1}} \left( \frac{1}{r_0} + \frac{R_S + R_D}{R_0} \right) + \frac{C_{gd}}{g_{m,1}} \left( \frac{1}{r_0} + \frac{R_S + R_D}{R_0} \right) + C_{gd} \left( \frac{R_S + R_D}{R_0} \right)$$  \hfill (1)

Here, $C_{gs}$ is the capacitance between gate and source, $g_{m,1}$ is the intrinsic transconductance, $R_S$ and $R_D$ are the resistances of the source and drain regions, $r_0$ is the output resistance of the transistor, and $C_{gd}$ is the capacitance between gate and drain. The Experimental Section describes the calculation of each of these parameters in detail. Here, we note the materials-specific parameters that enter the calculation, such as the sheet carrier density and the carrier velocity, were all experimentally determined using devices with MBE-grown Cd$_3$As$_2$ channels, as described in the following sections.

Figure 1B shows the calculated $f_T$ of a Cd$_3$As$_2$ channel MOTFET as a function of the gate length ($L_g$), both with (solid line) and without (dashed line) considering the RC time delay, respectively. As expected, RC time delay becomes a significant fraction of the total transit time for short channel FETs. Despite these delays, we predict $f_T$ of the Cd$_3$As$_2$ MOTFET to exceed 1.5 THz for scaled transistors with a gate length of 15 nm. This value is beyond the roadmap projections of semiconductors that are currently under investigation for THz transistors.\cite{21–23}

In addition to the high $f_T$, our calculations show that Cd$_3$As$_2$ MOTFETs, and indeed, FETs with Dirac materials in general, offer additional, significant advantages over conventional semiconductors for application in high-speed circuits. One such advantage is a linear frequency performance. To illustrate this unique property, we show in Figure 1C the calculated external transconductance, $g_{m,ext}$ of a Cd$_3$As$_2$ MOTFET with a gate length of 15 nm as a function of drain current, $I_D$. As seen from Figure 1C, $g_{m,ext}$ of the Cd$_3$As$_2$ MOTFETs does not degrade at higher drive current. Moreover, $f_T$ of the Cd$_3$As$_2$ MOTFETs shows similar linearity behavior without any drop at high drive current, as shown in Figure 1D. The linearity in $g_{m,ext}$ and in $f_T$ is a direct consequence of the Dirac dispersion of the electronic states, which causes the Fermi velocity ($v_F$) of the carriers, and thus their average forward velocity ($v_{avg, Fwd}$), to be independent of $E_T$ or the sheet carrier density (see Experimental Section). In contrast, the velocity of carriers in a semiconductor with parabolic bands is a function of $E_T$ or sheet carrier density (see Experimental Section, Figure 1E,F). In the saturation regime, when lateral electric field in the channel is high, the average velocity of the carriers is high when the sheet carrier density is low. At high sheet carrier densities, the distribution of carriers in momentum space lowers the average velocity. As a result, semiconductor FETs exhibit a maximum in $f_T$, followed by a roll-off at higher current densities (for examples, see Refs. [24–26]).

The unique, linear frequency performance offers crucial and unique advantages for RF analog circuits, because it prevents output signal distortion and improves the gain and bandwidth of such circuits. Currently, because of the non-linearity in frequency performance of transistors with semiconductors, circuit-level measures need to be taken to ensure linearity of the circuit, which negatively affect bandwidth, efficiency and performance of the circuit. Moreover, Figure 1D shows that Cd$_3$As$_2$ MOTFETs allow for THz operation even at low current densities. Advantages of operation at low current densities include...
Figure 2. Schematic diagram of the heterostructure and process flow for Cd₃As₂ devices.

Figure 3. Two-terminal device performance. A) TLM data used to extract the contact resistance. The dashed line is a linear fit to the data to obtain the parameters shown in the inset. B) Two-terminal I–V characteristics of Cd₃As₂ devices with different channel widths. The separation between the contacts is 2 µm. The absolute currents of 50 and 100 µm wide devices reached the compliance of the parameter analyzer before 2 V. C) Four-point probe measurements of resistances of Cd₃As₂ channels plotted as a function of inverse of channel width.

This issue can easily be resolved by using selective doping and gate-recessed FET structures.

The calculated high-frequency performance of Cd₃As₂ MOTFETs shown in Figure 1 depends on assumptions made about the values for \( v_{\text{avg,Fwd}} \), the sheet carrier density, \( n_s \), the current density, \( I_D \), and the contact resistance. To measure these parameters, devices were fabricated from epitaxial heterostructures with Cd₃As₂ channels grown on (111)-oriented GaAs substrates (see Figure 2 and Experimental Section). We note that the thickness (30 nm) of the Cd₃As₂ channel causes the bulk Dirac nodes to be gapped out. As shown previously, transport is then primarily via the gapless topological surface states, which are 2D Dirac states.⁴⁷,⁴⁸ Unless stated otherwise, all data were acquired at room temperature.

We begin with the contact resistance. Figure 3A shows the results of transfer length measurements (TLMs). The contact resistance and specific contact resistances for the Au/Ti contacts used here are 4.7 mΩ mm and 1.9 × 10⁻⁹ Ω cm², respectively. These values are comparable to the best III–V technologies, which have undergone many decades of optimization, and already meet the requirements for THz operation (<10⁻⁸ Ω cm²).⁴¹,⁴²

High current density devices with Cd₃As₂ channels require a high carrier velocity. To measure the carrier velocity, two-ter-

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The intrinsic potential of Cd₃As₂ channel FETs for THz circuits is clear from our calculations and materials parameter measurements reported above. It is, however, also important to identify any practical challenges that the development of such transistor may face due to extrinsic factors. In a previous study, we had shown that large densities of interface traps limited the transconductance of Cd₃As₂ MOTFETs that were fabricated using a low temperature (120 °C) atomic layer deposition (ALD) gate dielectric.⁴⁸ Here, we still employ the low temperature ALD dielectric to avoid channel degradation, but have improved the design and process flow. These modifications better reveal the intrinsic characteristics of Cd₃As₂ MOTFETs, which allows for improved quantitative projections.

A top view of the MOTFET is shown in Figure 4A. Figure 4B shows the drain current–gate voltage (I_D–V_G) and transconductance–gate voltage (g_m–V_G) characteristics. The transistor shows a maximum current density of 4 A mm⁻¹ at a drain voltage (V_D) of 1 V. This current density already compares favorably
with state-of-the-art III–V MOSFETs. The average velocity derived from the $I_D$–$V_G$ characteristics is $4 \times 10^5$ m s$^{-1}$. This is slightly lower than the velocity determined from Figure 3B, but the transistor is still in the linear regime. Therefore, higher velocities are straightforward to achieve either by applying a larger drain voltage or by reducing the gate length.

As noted previously, traps at the interface with the gate dielectric, rather than intrinsic materials properties, limited carrier modulation, because the gate bias modulates the immobile charge in the interface traps, rather than the mobile carriers in the channel. The current modulation is smaller in shorter-channel FETs (Figure 4C), relative to long channel devices, due to interface traps and the relatively larger access regions. Longer channel FETs show a current modulation of over 50% (Figure 4D), comparable to graphene FETs. For the same reason, the maximum value of $g_m$, 120 mS mm$^{-1}$, is lower than expected. Evidence for reduced gate control also comes from comparing the maximum average velocity derived from the transconductance ($v_{axmax} = \frac{g_m}{C_{gd}}$), $4\times10^4$ m s$^{-1}$, with the measured velocity, which is an order of magnitude larger. The important conclusion from this comparison is that reducing the interface trap density will improve the transconductance by a factor of 10.

To summarize, our calculations, which used experimentally measured Cd$_3$As$_2$ channel properties as input parameters, show that Cd$_3$As$_2$ MOTFETs should easily be able to reach the THz regime. Moreover, these FETs will maintain a high $f_T$ over a wide range of carrier densities, offering unique advantages for RF circuit design. The linearity of $f_T$, which had not previously been identified explicitly, is a general property of Dirac materials. While Cd$_3$As$_2$ has the highest carrier velocities, new materials are likely to be discovered. Taken together, the results presented here indicate that FETs with topological semimetals offer major advantages that should warrant the efforts needed to develop devices and circuits for future RF and THz circuits with them. In addition to device scaling, the main task will be to develop suitable gate dielectrics for these materials that allow for reduced interface trap densities.

**Experimental Section**

*Parameters used in the Calculations: Table 1 lists the parameters that were used to calculate the frequency performance of Cd$_3$As$_2$ MOTFETs.*

Equation (1) requires the calculation of $C_{gs}$ and $C_{gd}$. $C_{gs}$ consists of two parts, the channel capacitance and the fringing capacitance, while $C_{gd}$ only contains the fringing capacitance. Most of the capacitances that contribute to $C_{gs}$ and $C_{gd}$ depend on the device structure and gate dielectric thickness, rather than the specific channel material. The
The channel capacitance consists of $C_{\text{barrier}}$, $C_{\text{WF}}$ and the quantum capacitance, $C_{\text{DOS}}$. These three capacitances are connected in series. For $C_{\text{barrier}}$, the capacitance of a 2 nm thick high-k gate dielectric was taken, which is standard for state-of-the-art MOSFETs. $C_{\text{WF}}$ arises from the distance between the 2D surface states and the interface. The confined surface states of Dirac semimetals result in a large $C_{\text{WF}}$ relative to $C_{\text{barrier}}$ and $C_{\text{DOS}}$, which makes the calculated $f_t$ insensitive to $C_{\text{WF}}$. $C_{\text{DOS}}$ is due to the 2D Dirac states, which have linear energy dispersion $\varepsilon(k) = \hbar v_{\text{f}} k$. Their energy dispersion, $E(k)$, is given by

$$E(k) = \hbar v_{\text{f}} k,$$

where $\hbar$ is the reduced Planck’s constant and $k$ is the momentum. The sheet carrier density, $n_s$, is given by

$$n_s(E) = \frac{gE_f^2}{2\pi\hbar^2v_{\text{f}}^2} \tag{3}$$

The valley degeneracy, $g$, is two for Cd$_3$As$_2$\textsuperscript{[27]} and spin degeneracy is taken into account. $C_{\text{DOS}}$ is given as

$$C_{\text{DOS}} = q^2D_{\text{OS}} = q^2 \frac{gE_f}{2\pi\hbar^2v_{\text{f}}^2} \tag{4}$$

where $q$ is the electron charge. Figure 5 shows $C_{\text{DOS}}$ as a function of $n_s$ for different Fermi velocities. The fringing capacitances depend on the device structure rather than the channel material. The fringing capacitance on the source side ($C_{\text{gs},f}$) has almost no effect on $f_t$ as it is small compared to channel capacitance. The drain-side fringing capacitance ($C_{\text{gd},f}$) has a significant impact. Conservative values are used (see Table 1), which are larger than those of highly scaled III–V MOSFETs.$^{[38]}$

For the calculation of $g_{\text{m},j}$, the current density, $I_D$, is differentiated with respect to internal gate voltage, $V_{G_{\text{int}}}$

$$g_{\text{m},j} = \frac{\partial I_D}{\partial V_{G_{\text{int}}}} = \frac{I_D(V_{G_{\text{int}}} + \Delta V_{G_{\text{int}}}) - I_D(V_{G_{\text{int}}})}{\Delta V_{G_{\text{int}}}} \tag{5}$$

Finally, external transconductance, $g_{\text{m,ext}}$, was calculated from $g_{\text{m},j}$ using the following equation$^{[38]}$

$$g_{\text{m,ext}} = \frac{g_{\text{m},j}}{1 + R_g g_{\text{m},j}} \tag{6}$$

Experimental values were used for the sheath carrier density, $n_s$, and for the average forward velocity ($v_{\text{avg,Fwd}}$). The value of $n_s$ ($4.5 \times 10^{16}$ m$^{-2}$) was determined by Hall measurements, shown in Figure 6. The voltage division between $C_{\text{barrier}}$ and $C_{\text{DOS}}$ determines the change in $E_I$ at the channel for a small change in $V_{G_{\text{int}}}$ and then the density-of-states at $n_s$ was used to calculate the change in $n_s$.

$v_{\text{avg,Fwd}}$ is estimated from the measurements shown in Figure 3B, as discussed above. The average forward velocity of 2D Dirac electrons is related to $v_f$, as given by

$$v_{\text{avg,Fwd}} = \frac{\int_{-\pi/2}^{\pi/2} \int_{-\pi/2}^{\pi/2} v_f(k) \cos(\theta) k dk d\theta + \int_{-\pi/2}^{\pi/2} \int_{-\pi/2}^{\pi/2} v_f(k) \sin(\theta) k dk d\theta}{\pi v_f} \tag{7}$$

For 2D electron gases in traditional semiconductors with parabolic bands, the average forward velocity is $\frac{4}{3} v_f$, which is 1.5 times lower than that of a 2D Dirac states that has the same $v_f$. Moreover, as $v_f$ of the 2D Dirac states is independent of energy or sheet carrier density, $v_f$ becomes independent of the gate voltage or drain current. The linearity in $f_t$ of MOTFETs, discussed above, stems from this unique electronic property of Dirac states.

The values for $R_S$ and $R_{D}$ (see Table 1) are also from the experimental data. Like $R_S$ and $R_{D}$, $g_{\text{m},j}$ will be very low. Thus, a small value is assumed for
The calculations show that Cd$_3$As$_2$ channel FETs can still operate in the ohmic contacts, which were deposited by electron beam evaporation. Moreover, the calculations show that Cd$_3$As$_2$ MOTFETs is quite robust against moderate variation of device or material parameters (see also Figure 1). A Quantum Design DynaCool PPMS was used for temperature-varying device or material parameters using a HP 4155B Semiconductor Parameter Analyzer. The devices consisted of a series of 100 μm thick (112)-oriented Cd$_3$As$_2$ films grown on (111) GaAs substrates with a (111) GaSb buffer layer using MBE, as described elsewhere. [14] Different types of devices were fabricated. TLM measurements were carried out using a HP 4155B Semiconductor Parameter Analyzer. A narrow channel increases the resistance below the gate region and thus lowers the effect of additional resistances. As discussed in the main text, narrow channels also have higher current densities and allow for better thermal management. Moreover, the shorter source-to-gate and gate-to-drain distances ensure low access region resistances. The gate lengths and channel widths of longer channel FETs were 300 and 50 μm, respectively. A Quantum Design DynaCool PPMS was used for temperature-dependent Hall measurements. All I–V measurements were carried out using a HP 4155B Semiconductor Parameter Analyzer.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

O.F.S. carried out the calculations, device fabrication and measurements, and analyzed the data. M.G., B.G., D.A.K., and T.S. grew the films. O.F.S. and S.S. wrote the paper and all authors commented on it.

Keywords

dirac materials, RF transistors, terahertz devices, topological semimetals

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