Computing the Best Case Energy Complexity of Satisfying Assignments in Monotone Circuits

Janio Carlos Nascimento Silva\textsuperscript{1} and Uéverton S. Souza\textsuperscript{2,5}

\textsuperscript{1}Instituto Federal do Tocantins, Campus Porto Nacional, Porto Nacional, Brazil
\textsuperscript{2}Institute of Informatics, Faculty of Mathematics, Informatics and Mechanics, University of Warsaw, Warsaw, Poland
\textsuperscript{5}Instituto de Computação, Universidade Federal Fluminense, Niterói, Brasil

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Abstract

Measures of circuit complexity are usually analyzed to ensure the computation of Boolean functions with economy and efficiency. One of these measures is the energy complexity, which is related to the number of gates that output true in a circuit for an assignment. The idea behind energy complexity comes from the counting of ‘firing’ neurons in a natural neural network. The initial model is based on threshold circuits, but recent works also have analyzed the energy complexity of traditional Boolean circuits. In this work, we discuss the time complexity needed to compute the best case energy complexity among satisfying assignments of a monotone Boolean circuit, and we call such a problem as \textsc{MinEC}\textsuperscript{+}\textsc{M}. In the \textsc{MinEC}\textsuperscript{+}\textsc{M} problem, we are given a monotone Boolean circuit $C$, a positive integer $k$ and asked to determine whether there is a satisfying assignment $X$ for $C$ such that $EC(C, X) \leq k$, where $EC(C, X)$ is the number of gates that output true in $C$ according to the assignment $X$. We prove that \textsc{MinEC}\textsuperscript{+}\textsc{M} is NP-complete even when the input monotone circuit is planar. Besides, we show that the problem is W[1]-hard but in XP when parameterized by the size of the solution. In contrast, we show that when the size of the solution and the genus of the input circuit are aggregated parameters, the \textsc{MinEC}\textsuperscript{+}\textsc{M} problem becomes fixed-parameter tractable.

Keywords: energy complexity, monotone circuit, planar, genus, FPT.
1 Introduction

Circuit Complexity is a research field that aims to study bounds for measures (such as size and depth) of circuits that compute Boolean functions. The size of a circuit is its number of logic gates, and its depth is the largest path from any input to the output gate. A circuit complexity analysis can provide lower/upper bounds on circuits classes that represent classic decision problems besides the possibility to identify efficient Boolean circuits according to specific properties (see [14, 19, 30]). In addition, some important bounds are described to deal with different definitions of size [1]. From a combinatorial point of view, several optimization problems address the minimization of measures in some circuits classes, such as the notorious Weighted Circuit Satisfiability problem, where the weight measures the amount of true values assigned to the input variables.

Despite this ‘zoo of measures’, optimizing properties like size and depth does not always guarantee an ‘efficient’ design of a specific circuit class. Depending on the purpose, a circuit with small size (either considering gates or wires) or depth can be inappropriate; such a situation was identified in [27]. When faced with threshold circuits used as an artificial neural network, it is possible to observe a contrast with neurons of the human brain. The authors in [27] (based in neuroscience literature) argue that the activation of neurons in a human brain happens sparsely. It was shown in [17] that the metabolic cost of a single spike in cortical computation is very high in a way that approximately 1% of the neurons can be activated simultaneously. This phenomenon happens due to the asymmetric energy cost between neurons activated and non-activated in natural cases. From the other side, digital circuits, when satisfied (outputting true), on average activate 50% of the gates.

Under different perspectives, ‘energy’ (or ‘power’) of a circuit is a measure that has a lot of attention in the literature. Due to multiple models (from biology, electronics, or purely theoretical), several works address different ways of analyzing the energy of a circuit. In [16], the energy consumption of a circuit considers the switching energy consumed by wires (edges) and gates of VLSI circuits. In [4] and [5], it is analyzed the voltage-to-energy consumed by the gates, taking into consideration the failure-to-energy. Other different models are explored in [23] and [6], such works try to explore concepts of energy too intrinsic to the design of practical circuits on electronics.

In this paper, we deal with a circuit complexity measure called energy complexity (EC). The idea behind this measure is to evaluate the number of gates in a circuit that returns true for an assignment. A similar concept called ‘power of circuit’ was studied by [28]. The term energy complexity
was introduced in [27] as an alternative to the dilemma 
artificial vs natural
described above. In [27], the authors prove that the minimization of circuit
energy complexity obtains a different structure from the minimization of
classical circuit complexity measures and potentially closer to the structure of
neural networks in the human brain. The authors proved initial lower bounds
for energy complexity and other circuit complexity measure called entropy.
For an analysis more focused on circuit complexity and recent bounds for
energy complexity of Boolean functions we refer to [10].

With a different perspective, this work dedicates attention to optimiza-
tion and decision problems related to computing the energy complexity of
a circuit. More precisely, we consider the problem of determining the satis-
fying assignment with minimum energy consumption in monotone circuits,
i.e., the best case energy complexity of a satisfying assignment in the class
of monotone circuits, called \( \text{MinEC}_{M}^{+} \). Our focus is on time (parameterized)
complexity of the \( \text{MinEC}_{M}^{+} \) problem.

The paper’s sequence has some preliminaries and the problem definition,
a discussion of its NP-completeness on planar circuits, a W[1]-hardness proof
and an XP algorithm for the case where the number of gates to be activated is
considered as parameter. Finally, we present an FPT algorithm for \( \text{MinEC}_{M}^{+} \)
when parameterized either by the treewidth of the input circuit or by the
genus of the input plus the size of the solution.

An extended abstract of this paper has been presented in AAIM 2021 [22].

Preliminaries

A **Boolean circuit** is a model that computes a Boolean function 
\( g : \{0, 1\}^{n} \to \{0, 1\} \) over a basis of operators (e.g. \{AND, OR, NOT, ...\}). In terms of Graph
Theory, a Boolean circuit is a directed acyclic graph \( C(V, E) \) where the set of
vertices \( V = (I, G, \{v_{\text{out}}\}) \) is partitioned into: (i) a set of inputs \( I = \{i_{1}, i_{2}, \ldots \} \) composed by the vertices of in-degree 0; (ii) a set of gates \( G = \{g_{1}, g_{2}, \ldots \} \), which are vertices labeled with Boolean operators; (iii) and the
single output (sink) vertex \( v_{\text{out}} \) with out-degree equal to 0 and also labeled
with a Boolean operator (see Fig. [1]). The input vertices represent Boolean
variables that can take values from \{0, 1\} (\{true, false\}, depending on the
conventions), and the label/operator of a gate or output vertex \( w \) is given by
\( f(w) \). A **monotone circuit** is a Boolean circuit where the Boolean operators
allowed are in \{AND, OR\}. An **assignment** of \( C \) is a vector \( X = [x_{1}, x_{2}, \ldots, x_{|I|}] \)
of values for the set of inputs \( I \), where for each \( j \), \( x_{j} \in \{0, 1\} \) is the value
assigned to input \( i_{j} \). We say that \( X \) is a satisfying assignment if the circuit
\( C \) evaluates to 1 (true) when \( X \) is given as input.
Given a Boolean circuit $C$ and an assignment $X$, the Energy Complexity of $X$ into $C$, $EC(C,X)$, is defined as the number of gates that output true in $C$ according to the assignment $X$. The (Worst-Case) Energy Complexity of $C$ (denoted by $EC(C)$) is the maximum $EC(C,X)$ among all possible assignments $X$ (See [10]). Analogously, the Best-Case Energy Complexity of $C$ (denoted by $MinEC(C)$) is the minimum $EC(C,X)$ among all possible assignments $X$.

In [2, 3], a measure called certification-width was described, which is the size of a minimum subset of edges that are enough to certificate a satisfying assignment. Such edges form a structure called succinct certificate that can be seen as a minimal map of edges to be followed in order to activate the output gate. Similar structures, denoted by accepting subtree, positive proof, or solution subgraph, can also be found in [29, 11, 24, 25, 18].

Note that there are similarities between certification-width and energy complexity. Both measures indicate saturation levels of circuits, but while certification-width focuses on edges, energy complexity is about the activation of gates. However, energy complexity presents two additional challenges: (i) $EC$ ignores the ‘firing’ of input gates; (ii) $EC$ counts activated gates even if its signal does not reach the output gate (due to unsatisfied gates – see Fig. [2]). These two issues forbid rushed conclusions about $EC$ based on what we know about certification-width. Nevertheless, the study in [2] also motivates the study of the complexity of computing the best case energy complexity of satisfying assignments in monotone circuits.

Note that in energy complexity problems in addition to working with the gates needed to satisfy the circuit, it is still necessary to handle gates that assignments may collateral activate. Such behavior makes working
with energy complexity problems more challenging than typical satisfying problems where the focus is only on the minimal set of inputs, gates, or wires/edges sufficient to satisfy the circuit.

While computing the worst-case energy complexity of satisfying assignments in monotone circuits is trivial (just activate all inputs), the problem of computing the best-case energy complexity among all satisfying assignments in monotone circuits seems a challenge. Therefore, in this work, we address this particular case where the circuit is monotone, focusing on the following decision problem:

**Best-Case Energy Complexity of Satisfying Assignments in Monotone Circuits – MinEC$^+_M$**

**Instance**: A monotone Boolean circuit $C$ and a positive integer $k$.

**Question**: Is there a satisfying assignment $X$ for $C$ such that $EC(C, X) \leq k$?

Besides, we denote by $k$-MinEC$^+_M$ the parameterized version of MinEC$^+_M$ where $k$ is taking as the parameter.

## 2 Computational complexity analysis

In this section, we present our (parameterized) complexity results regarding MinEC$^+_M$. Since planarity is a notion with significant relevance in the field
of circuit analysis, we started our analysis with a focus on planar circuits.

### 2.1 NP-hardness on planar circuits

Using a reduction from Planar Vertex Cover, similar to that employed in [2], we are able to show that MinEC+M is NP-complete even when restrict to planar circuits.

**Theorem 1.** MinEC+M is NP-complete even when restricted to planar circuits.

**Proof.** Given a circuit $C$ and an integer $k$, forming an instance of MinEC+M, an assignment of Boolean values can be seen as a certificate for this instance. Since it is easy to count the number of gates outputting true according to an assignment, clearly, MinEC+M is in NP.

Now, we show the NP-hardness of MinEC+M by a reduction from Planar Vertex Cover (PVC), a well-known NP-complete problem.

| Planar Vertex Cover (PVC) |
|---------------------------|
| **Instance:** | A planar graph $G$; a positive integer $c$. |
| **Question:** | Is there a set $S$ of size at most $c$, such that for each edge $(u, v) \in E(G)$ either $u \in S$ or $v \in S$? |

First, consider the following preprocessing: let $(H, c')$ be an instance of Planar Vertex Cover, by subdividing twice each edge of $H$, we obtain a graph $G$ where each edge $e = (ab)$ of $H$ is replaced by a $P_4$ $a'b'a'b$, where $a'$ and $b'$ are new vertices (see Fig. 3).

![Figure 3: Green vertices are those $a'$ and $b'$ inserted in $G$ after the preprocessing step.](image)
Notice that $G$ is also planar; $H$ has a vertex cover of size $c'$ if and only if $G$ has a vertex cover of size $c = c' + |E(H)|$; and given a planar embedding of $G$, the boundary of any pair of adjacent faces of $G$ contains at least three edges.

From a fixed planar embedding of the instance $(G, c)$ of PLANAR VERTEX COVER, we proceed with the reduction. We will construct an instance $(C, k)$ of $\text{MINEC}^+_M$ where $C$ is a planar monotone circuit, and $k$ is the target size of the energy complexity.

From the structure of $G$, we apply the following:

1. first, set $V(C) = V(G)$;
2. for each vertex $v_i \in V(G)$, create an input vertex $v_i^\text{in}$, assign $f(v_i) = \text{AND}$, and add a directed edge $(v_i^\text{in}, v_i)$;
3. for each edge $e_i = (u, v) \in E(G)$, create a vertex $v_{e_i}^\text{cover}$ such that $f(v_{e_i}^\text{cover}) = \text{OR}$, and create the directed edges $(v, v_{e_i}^\text{cover})$ and $(u, v_{e_i}^\text{cover})$.

Figure 4: (a) Circuit after Step 3; (b) illustration of $\mathcal{T}_{DG}$.

Notice that $C$ is still planar. Now, preserving the planarity, we will ensure that every $v_{e_i}^\text{cover}$ outputs true for any assignment of $C$ as follows (see Fig. 5, Fig. 6 and Fig. 7):

4. create an output vertex $v_{out}$ such that $f(v_{out}) = \text{AND}$;
5. for each vertex $v_{e_i}^\text{cover}$ which are in the external face of $G$, create one directed edge from $v_{e_i}^\text{cover}$ to $v_{out}$.
Let $D_G$ be the dual graph of $G$, where $f_1$ represents the external face of $G$. Let $T_{D_G}$ be the spanning tree of $D_G$ obtained from a breadth-first search of $D_G$ rooted at $f_1$. (see Fig. 4b) In a top-down manner, according to a level-order traversal of $T_{D_G}$, we visit each edge $e = (f_i, f_j)$ of $T_{D_G}$ applying the following:

6. let $f_j$ be a child of $f_i$ in $T_{D_G}$; by construction of $G$, it follows that the boundary between $f_i$ and $f_j$ contains at least three edges, being at least one of which between vertices $a'$ and $b'$ that do not exist in $H$; thus, create a vertex $v_{f_j}$, add edges from $v_{f_j}$ to such $a'$ and $b'$; and for each $v_{cover}^{e_i}$ in the face $f_j$ that, yet, doesn’t reach $v_{out}$, add an edge from $v_{cover}^{e_i}$ to $v_{f_j}$; after that, if $v_{f_j}$ has in-degree greater than 0 then set $f(v_{f_j}) = \text{AND}$, otherwise create an input vertex $v_{f_j}^{in}$ add an edge from $v_{f_j}^{in}$ to $v_{f_j}$ and set $f(v_{f_j}) = \text{AND}$;

![Diagram](image)

Figure 5: Steps 4 and 5. Edges outgoing from $v_{cover}^{e_i}$ are highlighted in red.

From Step 6 holds that if $v_{out}$ outputs $\text{true}$ then every vertex $v_{cover}^{e_i}$ and $v_{f_j}$ also output $\text{true}$. Besides, as each $v_{f_j}$ can be added in the planar embedding inside its respective face, then the resulting graph still planar, and by using $T_{D_G}$ it holds that the added edges preserve the graph acyclic.

7. finally, set $k = c + |E(G)| + |V(D_G)|$. 

If $G$ has a vertex cover $S$ such that $|S| = c$ then we obtain a satisfying assignment $A$ to $C$ having energy complexity at most $k$ as follows: for each $v_i \in V(G)$ such that $v \notin S$ we set false to its corresponding input $v_i^{in}$ (created in step 2 of the reduction); and we assign true to the other inputs. Thus, in exactly $c$ edges flows true from vertices $v_i^{in}$ to its out-neighbor $v_i$ (so, at most $c$ vertices $v_i$ will output true); and from each $v_i$ set as true flows positive values to each $v_i^{cover}$ such that $e$ is an out-edge of $v_i$. Therefore, since $S$ is a vertex cover, in a bottom-up manner according to $T_DG$, we can observe that each face vertex $v_f$, each vertex $v_i^{cover}$, as well as $v_{out}$ will be set as true. Thus, $A$ is a satisfying assignment to $C$. At this point, it remains to analyze the energy of $A$. Note that $C$ has exactly $|E(G)|$ vertices $v_i^{cover}$, $|V(D_G)| - 1$ face vertices $v_f$, and all of them is set as true by $A$, which with the addition of $v_{out}$ implies energy consumption $|E(G)| + |V(D_G)|$, since at most $c$ vertices $v_i$ will output true, it follows that $A$ has energy $|E(G)| + |V(D_G)| + c$.

Conversely, let $C$ be a circuit with $k$ gates outputting true. By construction, if $C$ is satisfiable, then all vertices $v_i^{cover}$ and $v_f$ also are satisfiable and, consequently, there is at most $c$ vertices $v_i$ outputting true, representing, in this way, a vertex cover with $c$ vertices in $G$. \hfill \qed
Figure 7: Consequences of a minimum vertex cover of $H$ in the circuit $C$. Recall that each blue vertex is an OR-vertex, $v_{e^{\text{cover}}}$, representing an edge $e$ of $G$, while the other vertices are AND-vertices.
2.2 Parameterized Complexity

Next, we investigate the parameterized complexity of $\text{MinEC}_M^+$. 

**Theorem 2.** $k$-$\text{MinEC}_M^+$ is in $XP$.

**Proof.** Let $C = (V, E)$ be a circuit with $V = I \cup G \cup \{v_{\text{out}}\}$, where $I$ is the set of inputs of $C$, $G$ is the set of gates and $v_{\text{out}}$ is the output gate. If $C$ has a satisfying assignment $X$ such that $EC(C, X) \leq k$ then we can find $X$ as follows:

1. suppose that $X$ is the satisfying assignment with $EC(C, X) \leq k$ having minimum weight (i.e., minimum number of inputs assigned as true);

2. first, we “guess” the set $T$ of gates that should be activated by $X$, that is, in $n^{O(k)}$ time, we enumerate each subset $T$ of gates such that $|T| \leq k$ and check each one in a new branch;

3. for each $T$ we can check in polynomial time whether it is consistent, that is:
   - $v_{\text{out}} \in T$;
   - for each OR-gate $v$ in $T$ either it has an in-neighbor in $T$ or it has an in-neighbor in $I$, and for each AND-gate $v$ in $T$ its in-neighborhood is contained in $T \cup I$;
   - conversely, each OR-gate $w \notin T$ has no in-neighbor in $T$, and each AND-gate $w \notin T$ has at least one in-neighbor that is not in $T$;
   - also, no input is mutually in-neighbor of an AND-gate in $T$ and an OR-gate not in $T$;
   - if $T$ is the set of gates activated by $X$ then it holds that: any input $i$ that is in-neighbor of an AND-gate in $T$ should be set as false in $X$; any input $i$ that is in-neighbor of an OR-gate not in $T$ should be set as true in $X$. Let $X'$ be such a partial assignment;
   - at this point, for a consistent $T$, each OR-gate $v$ in $T$ having no in-neighbor in $T$ has at least one in-neighbor in $I$ that is not set as false by $X'$, and each AND-gate $w \notin T$ having no in-neighbor in $G \setminus T$ has at least one in-neighbor in $I$ that is not set as true in $X'$.

4. Since $X$ has minimum weight, from a given consistent set $T$, in order to extend $X'$ into a satisfying assignment $X$ with $EC(C, X) \leq k$ (if any), it is enough to “guess” the minimal set of inputs that should be
set as true to activate the OR-gates in $T$ having no in-neighbor in $T$. As $|T| \leq k$, such subset of inputs is also bounded by $k$, thus, in $n^{O(k)}$ time, we can enumerate (if any) each assignment $X''$ extending $X'$ by setting at most $k$ additional inputs as true in such a way that each OR-gates in $T$ has at least one in-neighbor activated. At this point, from the guessed set $T$ we obtain the assignment $X$ if there is some $X''$ for which each AND-gate $w \notin T$ having no in-neighbor in $G \setminus T$ has at least one in-neighbor in $I$ that is set as false.

Note that for any satisfying assignment $X$ of $C$ the set of activated gates must satisfy the properties described in step 3. Since steps 2 and 4 check in $n^{O(k)}$ time all possibilities, it holds that $\text{MINEC}^+_M$ is XP-time solvable.

Now, we show the W[1]-hardness of $k$-$\text{MINEC}^+_M$ using a reduction from MULTICOLORED CLIQUE.

| MULTICOLORED CLIQUE |
|---------------------|
| **Instance:** A graph $Q$ with a vertex-coloring $\ell : V(G) \to \{1, 2, \ldots, c\}$. |
| **Parameter:** A positive integer $c$. |
| **Question:** Does $Q$ have a $c$-clique containing all $c$ colors? |

**Theorem 3.** $k$-$\text{MINEC}^+_M$ is W[1]-hard.

**Proof.** Let $(Q, c)$ be an instance of MULTICOLORED CLIQUE and let $V_1, V_2, \ldots, V_c$ be the color classes of $Q$. Without loss of generality, we consider that each vertex in $V_i$ has at least one neighbor in $V_j (i \neq j)$. We construct an instance $(C, k)$ of $\text{MINEC}^+_M(k)$ as follows (see Fig. 8 and Fig. 9):

1. create an output gate $v_{\text{out}}$ in $C$ and set $f(v_{\text{out}}) = \text{AND}$;

2. for each color $c_i$ of $Q$, create a gate $w_i$ with $f(w_i) = \text{OR}$ and add an edge from $w_i$ to $v_{\text{out}}$;

3. for each color class $V_i$ of $Q$, create copies $V^1_i, V^2_i, V^3_i$ and $V^4_i$ in $C$;

4. add edges from each vertex in $V^4_i$ to $w_i$;

5. let $v^1, v^2, v^3$ and $v^4$ be the copies of a vertex $v \in V(Q)$; add edges $(v^1, v^2), (v^2, v^3)$ and $(v^3, v^4)$ to $G$; set $V^1_i$ as the input set; and assign $f(v^2) = f(v^3) = \text{OR}$ and $f(v^4) = \text{AND}$;

6. for each vertex $v^4 \in V^4_i (1 \leq i \leq c)$, create $c - 1$ new OR-in-neighbors $a^j_{v^4} (1 \leq j \leq c$ and $i \neq j)$, and for each $u^2 \in V^2_j$ such that $vu \in E(Q)$ create an AND-vertex $b^j_{vu}$ and the following edges: $(b^j_{vu}, a^j_{v^4}), (u^2, b^j_{vu})$ and $(v^2, b^j_{vu})$;
7. finally, set $k = 2c^2 + 2c + 1$.

Figure 8: An instance $Q$ for Multicolored Clique

If $Q$ contains a multicolored clique $K$ such that $|K| = c$, then it is possible to find a satisfying assignment of $C$ that consumes $k$ energy by mapping the set $S$ of gates/vertices that must be activated (outputs $\text{true}$) as follows: (a) $v_{\text{out}}$ and all of its in-neighbors must belong to $S$; (b) for each OR-gate $w_i \in S$, we want include in $S$ exactly the in-neighbor $v^i \in V^i$ such that $v \in K$, therefore, we set $f(v^i) = \text{true}$ if and only if $v \in K$ (At this point, by construction, for each $v \not\in K$ holds that every vertex between $v^1$ and $v^4$ will be inactivated); (c) for each $v^4 \in S$, all of its in-neighbors must be in $S$, and for each $a_{t,4} \in S$, its unique in-neighbor in $S$ must be the AND-gate $b_{vu}$ such that $f(v^1) = f(u^1) = \text{true}$ (recall that $K$ has exactly one vertex per color). (d) finally, a vertex $v^2 \in V_2$ belongs to $S$ if and only if its in-neighbor $v^1$ outputs true. Through a simple count one can conclude that $|S| = 2c^2 + 2c + 1$. Thus, the defined assignment satisfies $C$ by consuming $k$ energy as required.

Conversely, if $C$ has a satisfying assignment $X$ with energy complexity at most $k = 2c^2 + 2c + 1$ then it is possible to obtain a multicolored clique $K$ of $Q$ as follows: a vertex $v$ of $Q$ belongs to $K$ if and only if $v^2$ outputs $\text{true}$. Since, by construction, any satisfying assignment of $C$ activates at least $2c^2 + 2c + 1$ gates in $V(C) \setminus (V_2 \cup V_1)$, the assignment $X$ activates at most $c$ gates in $V_2$. Besides, the construction also implies that at least one input per color must activated in order to satisfy $C$. So, $X$ activates exactly $c$ gates in $V_2$ (one per color). Therefore, $K$ has exactly one vertex per color. Now, to show that $K$ induces a clique is enough to observe the if $v_2$ and $u_2$ are activated in $X$ into $C$ and $vu \not\in E(G)$, then for the color $j$ of $u$ holds that $b_{vu}$ is inactivated by $X$ into $C$ for any neighbor $r$ of $v$ with color $j$. Thus, $v_4$ and $w_i$ are also inactivated, where $i$ is the color of $v$, which contradicts the fact that $X$ satisfies $C$. Therefore, $K$ induces a clique. \qed
2.3 On monotone circuits with bounded genus

A graph $G$ has genus at most $g$ if it can be drawn on a surface of genus $g$ (a sphere with $g$ handles) without edge intersections (see Fig. 10). We consider the genus of a circuit as the genus of its underlying undirected graph. Additionally, We refer the reader to [13] for more information on the genus of a graph.

In this section, we show that $k$-$\text{MiNEC}^+_M$ on bounded genus circuits can be reduced to $k$-$\text{MiNEC}^+_M$ on bounded treewidth circuits.

**Definition 1.** A tree decomposition of a undirected graph $G$ is a pair $\mathcal{T} = (T, \{X_t\}_{t \in V(T)})$, such that $T$ is a tree where each node $t$ is assigned to a set of vertices $X_t \subseteq V(G)$, called bags, according to the following conditions:

- $\bigcup_{t \in V(T)} X_t = V(G)$;
- For each $uv \in E(G)$ there is a node $t$ such that $\{u, v\} \subseteq X_t$;
• For each $v \in V(G)$, the set $T_v = \{ t \in V(T) : v \in X_t \}$ spans a subtree of $T$.

The width of a tree decomposition $T$ is the size of its largest bag minus one. The treewidth of $G$ is the minimum width among all tree decompositions of $G$.

**Definition 2.** A graph $H$ is a minor of a graph $G$ if $H$ can be constructed from $G$ by deleting vertices or edges, and contracting edges.

**Theorem 4** (Excluded Grid Theorem [20]). Let $t$ be a non-negative integer. Then every planar graph $G$ of treewidth at least $9t/2$ contains a grid $t \times t$ as a minor.

From the Excluded Grid Theorem, it is easy to see that there is a connection between the diameter of a planar graph and its treewidth. In [21], Robertson and Seymour presented a bound for the treewidth of a planar graph with respect to its radius, which also implies a bound regarding the diameter.

**Definition 3.** For every face $F$ of a planar embedding $M$, we define $d(F)$ to be the minimum value of $r$ such that there is a sequence $F_0, F_1, \ldots, F_r$ of faces of $M$, where $F_0$ is the external face, $F = F_r$, and for $1 \leq j \leq r$ there is a vertex $v$ incident with both $F_{j-1}$ and $F_j$. The radius $\rho(M)$ of $M$ is the minimum value $r$ such that $d(F) \leq r$ for all faces $F$ of $M$. The radius of a planar graph is the minimum of the radius of its planar embeddings.

**Theorem 5** (Radius Theorem [21]). If $G$ is planar and has radius at most $r$ then its treewidth is at most $3r + 1$. 

![Image](image.png)

(a) Genus 0.  
(b) Genus 1.  
(c) Genus 2

Figure 10: Relation between genus and geometrical shapes.
Using Theorem 5, we are able to either solve \( \text{MinEC}^+_M \) on planar circuits or outputs an equivalent instance \( C' \) with treewidth bounded by a function of \( k \).

**Lemma 1.** Let \( (C,k) \) be an instance of \( \text{MinEC}^+_M \). There is an algorithm that in polynomial time either solves \( (C,k) \) or outputs an equivalent instance \( (C',k) \) of \( \text{MinEC}^+_M \) where the distance from \( v_{out} \) to each vertex in the underlying graph of \( C' \) is at most \( 2k + 1 \).

**Proof.** From an instance \( (C,k) \) of \( \text{MinEC}^+_M \), we apply the following reduction rules to obtain \( C' \):

1. Delete every input vertex which is at a distance greater than \( k \) to \( v_{out} \);
2. Delete every vertex which is at a distance greater than \( k + 1 \) from its nearest input vertex;
3. Delete any AND-vertex which lost one of its in-neighbors;
4. Delete any OR-vertex in which its in-degree became equal to 0;
5. Repeat steps 1 to 4 as long as possible;
6. If \( C' = \emptyset \) then we conclude that \( (C,k) \) is a no-instance of \( \text{MinEC}^+_M \).

We now discuss the safety of the previous reduction rules: if an input vertex \( v \) is at a distance greater than \( k \) from \( v_{out} \), since \( C \) is monotone, then \( v \) is not useful to satisfy \( v_{out} \) in any assignment \( X \) with \( EC(C,X) \leq k \), thus we can assume that \( v \) outputs \text{false} and given the monotonicity of \( C \) we can safely remove \( v \) (Rule 1). Similarly, gates that are at a distance greater than \( k \) from its nearest input vertex must output \text{false} in an assignment \( X \); otherwise, \( X \) consumes energy greater than \( k \). Note that vertices at a distance exactly \( k + 1 \) from its nearest input vertex can be useful to show that a given assignment consumes energy greater than \( k \). However, gates at a distance of at least \( k + 2 \) from its nearest input vertex can be removed once its neighbors are sufficient to certify the negative answer (Rule 2). Besides, if for any assignment \( X \) with \( EC(C,X) \leq k \) holds that some (resp. every) in-neighbor of an AND( resp. OR)-vertex \( v \) must output \text{false}, then \( v \) must output \text{false} as well. Thus, Rule 3 and Rule 4 are safe. From the safety of rules 1-4, it follows that Rule 5 and Rule 6 are safe. Finally, if \( C' \neq \emptyset \) then \( C' \) has only vertices at a distance at most \( 2k + 1 \) from \( v_{out} \) in the underlying undirected graph of \( C' \).
Note that the underlying undirected graph of the circuits obtained from Lemma 1 have diameter bounded by $4k + 2$. Therefore, contrasting with the W[1]-hardness for the general case, Corollary 1 holds.

**Corollary 1.** $k$-$\text{MiNEC}_M^+$ is fixed-parameter tractable when restricted to monotone circuits having bounded maximum in-degree.

**Proof.** First, apply the preprocessing algorithm presented in Lemma 1. After that, each input vertex is at a distance of at most $k$ from $v_{\text{out}}$ in the resulting circuit $C'$. Since each input vertex of $C'$ must reach $v_{\text{out}}$, $C'$ is acyclic, and it has bounded maximum in-degree, then from a BFS algorithm having $v_{\text{out}}$ as root (considering the reverse order of edges) we can visit all input vertices using at most $k$ levels, implying that the number of input vertices in $C'$ is bounded by $c^k$, where $c$ is its maximum in-degree. Also, each gate of $C'$ is at distance at most $k + 1$ from its nearest input vertex, and since the number of input vertices in $C'$ is bounded, by a similar argument, the number of gates of $C'$ is also bounded by a function of $k$. Thus, when the input circuit $C$ has bounded maximum in-degree, after the preprocessing of Lemma 1 the resulting circuit $C'$ is a kernel for $k$-$\text{MiNEC}_M^+$, implying its fixed-parameter tractability.

Notice that a gate with large in-degree can always be replaced by a binary tree using only binary gates, but for or-gates it makes a relevant difference in the energy complexity. Therefore, replacing large in-degree gates is not a useful strategy for dealing with $k$-$\text{MiNEC}_M^+$. On the other hand, Lemma 1 also implies that if $C'$ is planar then it also has bounded radius, thus, by Theorem 5 it follows that the underlying undirected graph of $C'$ has treewidth bounded by a function of $k$. We extend the previous reasoning for bounded genus circuits.

Given a vertex-set $S \subseteq V(G)$ of a simple graph $G$ such that the subgraph of $G$ induced by $S$, denoted $G[S]$, is connected, contracting $S$ means contracting the edges between the vertices in $S$ to obtain a single vertex at the end. We say that a graph $H$ is an $s$-contraction of a graph $G$ if $H$ can be obtained after applying to $G$ a (possibly empty) sequence of edge contractions.

The following is a construction presented in [12] and [15]. Consider an $(r \times r)$-grid. A corner vertex of the grid is a vertex of the grid of degree 2. By $\Gamma_r$ we denote the graph obtained from the $(r \times r)$-grid as follows (see Fig.11): construct first the $\Gamma'_r$ by triangulating all internal faces of the $(r \times r)$-grid such that all internal vertices of the grid are of degree 6, and all non-corner external vertices of the grid are of degree 4 ($\Gamma'_r$ is unique up to isomorphism). Two of the corners of the initial grid have degree 2 in $\Gamma'_r$; let $x$ be one of them. $\Gamma_r$ obtained from $\Gamma'_r$ by adding all the edges having $x$ as an endpoint.
and a vertex of the external face of the grid that is not already a neighbor of \(x\) as the other endpoint. Observe again that \(\Gamma'_r\) is unique up to isomorphism.

The following is a lemma from [15] implied from Lemma 6 in [12].

**Lemma 2** (Lemma 4.5 in [15]). Let \(G\) be a graph of genus \(g\), and let \(r\) be any positive integer. If \(G\) excludes \(\Gamma_r\) as an \(s\)-contraction, then the treewidth of \(G\) is at most \((2r + 4) \cdot (g + 1)^{3/2}\).

**Lemma 3.** Let \(C'\) be the circuit obtained from Lemma 4. It holds that \(C'\) has treewidth at most \((8k + 14) \cdot (g + 1)^{3/2}\), where \(g\) is the genus of \(C'\).

**Proof.** First, notice that for each vertex \(u\) of a \(\Gamma_{4k+5}\) there is another vertex \(v\) such that the distance between \(u\) and \(v\) is at least \(2k + 2\). Now, suppose that \(C'\) has \(\Gamma_{4k+5}\) as an \(s\)-contraction, and let \(u\) be a vertex of a \(\Gamma_{4k+5}\) such that \(u\) is either \(v_{out}\) or a vertex obtained by contracting \(S\) containing \(v_{out}\). Since there is a vertex \(v\) such that the distance between \(u\) and \(v\) is at least \(2k + 2\), it holds that \(C'\) has a vertex at distance greater than \(2k + 1\) from \(v_{out}\), which is a contradiction (see Lemma 1). Thus, by Lemma 2 we have that the treewidth of \(C'\) is at most \((8k + 14) \cdot (g + 1)^{3/2}\). \(\square\)
3 Dynamic programming on bounded treewidth circuits

From Lemma 3, in order to solve $k$-MINEC$^+_M$ in FPT-time on bounded genus instances, it is enough to present an FPT algorithm parameterized by the treewidth of the input. To design a dynamic programming on tree decompositions, without loss of generality, we may consider that we are given a tree decomposition that is a rooted extended nice tree decomposition (see [9] for details), which is defined as follow.

**Definition 4.** A tree decomposition $T$ is an extended nice tree decomposition if the following conditions are satisfied:

- The root bag $X_r$ and the leaf bags are empty;
- Every non-leaf node of $T$ is one of the types described below:
  - Introduce vertex node – a node $t$ with exactly one child $t'$ such that $X_t = X_{t'} \cup \{v\}$ for some $v \notin X_{t'}$, we say that $v$ is introduced in $t$;
  - Introduce edge node – a node $t$, labeled with an edge $uv \in E(G)$ such that $\{u, v\} \in X_t$, and with exactly one child $t'$ such that $X_t = X_{t'}$, we say that edge $uv$ is introduced at $t$;
  - Forget node – a node $t$ with exactly one child $t'$ such that $X_t = X_{t'} \setminus \{v\}$ for some $v \in X_{t'}$, we say that $v$ is forgotten at $t$;
  - Join node – a node $t$ with two children $t'$ and $t''$ such that $X_t = X_{t'} = X_{t''}$.
- every edge of $E(G)$ is introduced exactly once in the whole decomposition.

Based on the following results, we can assume that we are given a nice tree decomposition of $G$ without loss of generality.

**Theorem 6.** [7] There exists an algorithm that, given an $n$-vertex graph $G$ and an integer $k$, runs in time $2^{O(k)} \cdot n$ and either outputs that the treewidth of $G$ is larger than $k$ or constructs a tree decomposition of $G$ of width at most $5k + 4$.

**Lemma 4.** [9] Given a tree decomposition $(T, \{X_t\}_{t \in V(T)})$ of $G$ of width at most $k$, one can in time $O(k^2 \cdot \max(|V(T)|, |V(G)|))$ compute a nice tree decomposition of $G$ with at most $O(k \cdot |V(G)|)$ nodes and width at most $k$. 

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Now, we are ready to use a nice tree decomposition to obtain an FPT-time algorithm for MinEC\textsuperscript{+} parameterized by tw(G), with single exponential dependency on tw(G) and linear with respect to n.

**Theorem 7.** MinEC\textsuperscript{+} can be solved in time 2\(O^{O}(tw)\cdot n\), where tw is the treewidth of the underlying undirected graph of the input.

**Proof.** Let C = (I, G, v\textsubscript{out}) be a monotone circuit where I is the set of inputs of C, G is the set of gates with out-degree greater than 0 and v\textsubscript{out} is a single output vertex. Let \(T = (T, \{X_t\}_{t \in V(T)})\) be a rooted extended nice tree decomposition of C. Consider also \(T_t\) as the subtree of T rooted by node t (bag \(X_t\)) and \(C_t\) be the graph/circuit having \(T_t = (T_t, \{X_t\}_{t \in V(T_t)})\) as tree decomposition. For convenience, we add the vertex v\textsubscript{out} to every bag of T; thus, the width of T is increased by at most one.

Now, note that an assignment X satisfies a monotone circuit C if and only if it induces an activation set \(S_X\) such that:

1. \(v_{out} \in S_X\);
2. for each \(v \in S_X\) holds that:
   - if \(f(v) = \text{AND}\) then every in-neighbor of \(v\) is in \(S_X\);
   - if \(f(v) = \text{OR}\) then at least one among the in-neighbors of \(v\) is in \(S_X\);
3. for each \(v \notin S_X\) holds that:
   - if \(f(v) = \text{AND}\) then at least one among the in-neighbor of \(v\) is not in \(S_X\);
   - if \(f(v) = \text{OR}\) then every in-neighbor of \(v\) is not in \(S_X\);

Properties 1 and 2 describe the necessary and sufficient conditions for a set \(S_X\) of activated gates to certify a satisfying assignment. Property 3 ensures that \(S_X\) is maximal regarding the property of having been activated by \(X\).

Therefore, the problem of finding a satisfying assignment \(X\) which minimizes \(EC(C, X)\) can be seen as the problem of finding a satisfying assignment \(X\) which minimizes \(|S_X \setminus I|\). Thus, we define \(c[t, S, F^{\text{QR}}, F^{\text{AND}}]\) as the cardinality of a minimum set of gates \(S_t\) (if any) of \(C_t\) such that:

- \(v_{out} \in S\) and \(S = X_t \cap S_t\); (we say that \(X_t \setminus S = \overline{S}\))
- for each \(v \in V(C_t) \setminus X_t\) properties 2 and 3 holds with respect to \(S_t\).
• for each \( v \in S \) such that \( f(v) = \text{AND} \), all in-neighbors of \( v \) in \( C_t \) are in \( S_t \);

• The set \( B^\text{OR} \) is the subset of \( \text{OR} \)-gates in \( S \) already having in-neighbors in \( S_t \);

• for each \( v \in \overline{S} \) such that \( f(v) = \text{OR} \), all in-neighbors of \( v \) in \( C_t \) are not in \( S_t \);

• The set \( B^\text{AND} \) is the subset of \( \text{AND} \)-gates in \( \overline{S} \) already having in-neighbors that are not in \( S_t \);

Furthermore, the optimal solution of the main problem can be found either at \( c[t, \{v_{\text{out}}\}, \{\}, \{\}] \) if \( f(v_{\text{out}}) = \text{AND} \), or at \( c[r, \{v_{\text{out}}\}, \{\}, \{\}] \) if \( f(v_{\text{out}}) = \text{OR} \) and \( v_{\text{out}} \notin B^\text{OR} \), or at \( c[r, \{v_{\text{out}}\}, \{\}, \{\}] \) if \( f(v_{\text{out}}) = \text{OR} \) and \( v_{\text{out}} \in B^\text{OR} \).

In order to solve \( \text{MinEC}_M^+ \), the counting of gates that output \text{true} (in the solution) are made in introduce vertex nodes. Note that in the introduce node of an \( \text{OR} \)-vertex \( v \), it can not be simultaneously in \( S \) and \( B^\text{OR} \) because when a vertex is introduced then it is isolated in \( C_t \) (we are considering an extended nice tree decomposition, i.e. the edges are introduced in introduce edge nodes).

**Leaf node** Let \( t \) be a leaf node, then \( X_t = \{v_{\text{out}}\} \). Since \( v_{\text{out}} \) must be in \( S \), then \( B^\text{AND} = \emptyset \). Thus, we have three subproblems in Equation (1).

\[
c[t, \{v_{\text{out}}\}, B^\text{OR}, B^\text{AND}] = \begin{cases} 
1, & \text{if } f(v_{\text{out}}) = \text{AND} \\
1, & \text{if } f(v_{\text{out}}) = \text{OR} \text{ and } v_{\text{out}} \notin B^\text{OR} \\
\infty, & \text{if } f(v_{\text{out}}) = \text{OR} \text{ and } v_{\text{out}} \in B^\text{OR}
\end{cases} \quad (1)
\]

**Introduce vertex node** Let \( t \) be an introduce vertex node with exactly one child \( t' \) such that \( X_t = X_{t'} \cup \{v\} \). In the graph \( C_t \), \( v \) is an isolated vertex; consequently, as in the leaf nodes, there is infeasibility whenever \( v \) belongs to \( B^\text{OR} \) or \( B^\text{AND} \). Besides, we have the possibility of \( v \) be an input vertex \( (f(v) \notin \{\text{AND, OR}\}) \) or \( v \notin S \), such situations only rescue previous subproblems without increment the current subsolution. On the other hand, we increment the subsolution by 1 whenever \( v \in S \). All possibilities are covered in Equations (2), (3) and (4).

• If \( f(v) \notin \{\text{AND, OR}\} \) then
\[
c(t, S, B^{\text{OR}}, B^{\text{AND}}) = c(t', S \setminus \{v\}, B^{\text{OR}}, B^{\text{AND}})
\]

- If \( f(v) = \text{OR} \) then

\[
c(t, S, B^{\text{OR}}, B^{\text{AND}}) = \begin{cases} 
c(t', S, B^{\text{OR}}, B^{\text{AND}}), & \text{if } v \notin S \\
c(t', S \setminus \{v\}, B^{\text{OR}}, B^{\text{AND}}) + 1, & \text{if } v \in S \text{ and } v \notin B^{\text{OR}} \\
\infty, & \text{if } v \in S \text{ and } v \in B^{\text{OR}}
\end{cases}
\]

- If \( f(v) = \text{AND} \) then

\[
c(t, S, B^{\text{OR}}, B^{\text{AND}}) = \begin{cases} 
c(t', S \setminus \{v\}, B^{\text{OR}}, B^{\text{AND}}) + 1, & \text{if } v \in S \\
c(t', S, B^{\text{OR}}, B^{\text{AND}}), & \text{if } v \notin S \text{ and } v \notin B^{\text{AND}} \\
\infty, & \text{if } v \notin S \text{ and } v \in B^{\text{AND}}
\end{cases}
\]

**Introduce edge node**  Let \( t \) be an introduce edge node and \( t' \) its child such that \( X_t = X_{t'} \), which introduces the directed edge \( uv \) such that \( \{u, v\} \subseteq X_t \). Now, by including an edge, we can evaluate each subproblem concerning the sets \( B^{\text{OR}} \) and \( B^{\text{AND}} \); so, for each OR-gate \( v \in S \), at least one in-neighbor also must be in \( S \); so, either \( uv \) attend this demand or another already introduced edge satisfied that. We apply the same reasoning for AND-gates: considering an AND-gate \( v \in \overline{S} \), then at least one in-edge of \( v \) need comes to another vertex in \( \overline{S} \); if \( uv \) do not attend this requirement, the current subproblem is assigned to a previous subproblem where \( v \in B^{\text{AND}} \). All these conditions are handled in Equations (5) and (6).  Recall that we are introducing the directed edge \( uv \).

- If \( f(v) = \text{OR} \) then \( c(t, S, B^{\text{OR}}, B^{\text{AND}}) \) is equal to

\[
\begin{cases} 
c(t', S, B^{\text{OR}}, B^{\text{AND}}), & \text{if } u \notin S \\
\infty, & \text{if } u \in S \text{ and } v \notin S \cap B^{\text{OR}} \\
\min \{c(t', S, B^{\text{OR}}, B^{\text{AND}}), c(t', S, B^{\text{OR}} \setminus \{v\}, B^{\text{AND}})\}, & \text{if } u \in S \text{ and } v \in S \cap B^{\text{OR}}
\end{cases}
\]

- If \( f(v) = \text{AND} \) then \( c(t, S, B^{\text{OR}}, B^{\text{AND}}) \) is equal to

\[
\begin{cases} 
c(t', S, B^{\text{OR}}, B^{\text{AND}}), & \text{if } u \in S \\
\infty, & \text{if } u \notin S \text{ and } v \in S \\
\infty, & \text{if } \{u, v\} \subseteq \overline{S} \text{ and } v \notin B^{\text{AND}} \\
\min \{c(t', S, B^{\text{OR}}, B^{\text{AND}}), c(t', S, B^{\text{OR}} \setminus \{v\})\}, & \text{if } \{u, v\} \subseteq \overline{S} \text{ and } v \in B^{\text{AND}}
\end{cases}
\]

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Forget node  Let \( t \) be a forget node and \( t' \) be its child such that \( X_t = X_{t'} \setminus v \). In this case, we verify the best among either selecting or not \( v \) in current subproblem. If \( v \) is an input vertex, then this verification is trivial (it is enough to rescue the minimum subsolution varying only the membership of \( v \) in \( S \)). For OR-gates and AND-gates, the same verification are made but considering the feasibility of \( v \) through its membership in \( B^{\text{OR}} \) and \( B^{\text{AND}} \). Equations (7), (8) and (9) summarize these three scenarios.

- If \( f(v) \neq \{\text{AND, OR}\} \) then
  \[
  c[t, S, B^{\text{OR}}, B^{\text{AND}}] = \min \left\{ c[t', S, B^{\text{OR}}, B^{\text{AND}}], c[t', S \cup \{ v \}, B^{\text{OR}}, B^{\text{AND}}] \right\}
  \]
  \[\text{(7)}\]

- If \( f(v) = \text{OR} \) then
  \[
  c[t, S, B^{\text{OR}}, B^{\text{AND}}] = \min \left\{ c[t', S, B^{\text{OR}}, B^{\text{AND}}], c[t', S \cup \{ v \}, B^{\text{OR}} \cup \{ v \}, B^{\text{AND}}] \right\}
  \]
  \[\text{(8)}\]

- If \( f(v) = \text{AND} \) then
  \[
  c[t, S, B^{\text{OR}}, B^{\text{AND}}] = \min \left\{ c[t', S, B^{\text{OR}}, B^{\text{AND}} \cup \{ v \}], c[t', S \cup \{ v \}, B^{\text{OR}}, B^{\text{AND}}] \right\}
  \]
  \[\text{(9)}\]

Join node  Let \( t \) be a join node with two children \( t_1 \) and \( t_2 \). For tabulation of the join nodes, we need to combine two partial solutions – one originating from \( C_{t_1} \) and another from \( C_{t_2} \) – in such a way that the merging is a feasible solution. Recall that \( G \) is acyclic so we don’t need to care about cycles. Also, if a gate is activated in \( C_t \) it must be activated in both children, so we must subtract duplicity. However, since each edge of \( C_t \) is in either \( C_{t_1} \) or \( C_{t_2} \), the feasibility of merging children’s solutions is guaranteed assuming that whether \( v \in B^{\text{OR}}/B^{\text{AND}} \) then it is also in the respective set of one of the children, as described in Equation (10).

\[
 c[t, S, B^{\text{OR}}, B^{\text{AND}}] = \min_{B^{\text{OR}}_1, B^{\text{AND}}_1, B^{\text{OR}}_2, B^{\text{AND}}_2} \left\{ c[t_1, S, B^{\text{OR}}_1, B^{\text{AND}}_1] + c[t_2, S, B^{\text{OR}}_2, B^{\text{AND}}_2] \right\} - |S \setminus I|
\]
\[\text{(10)}\]

where \( B^{\text{OR}} = B^{\text{OR}}_1 \cup B^{\text{OR}}_2 \) and \( B^{\text{AND}} = B^{\text{AND}}_1 \cup B^{\text{AND}}_2 \).

Every bag of \( T \) has at most \( tw + 2 \) vertices (including \( v_{\text{out}} \)) and \( v_{\text{out}} \) is fixed in the solution, thus each bag has at most \( 2^{tw+1} \) possible subsets \( S \), there are at most \( 2^{tw+2} \) possible sets \( B^{\text{OR}} \), and there are at most \( 2^{tw+1} \) sets \( B^{\text{AND}} \). Therefore, the entire matrix has size \( 2^{O(tw) \cdot n} \). As each entry of the table can be computed in \( 2^{O(tw)} \cdot n \) time, it holds that the algorithm performs in time \( 2^{O(tw)} \cdot n \).

From Theorem 3 and Theorem 7, it follows that Corollary 2 holds.
Corollary 2. $\text{MinEC}^+_M$ can be solved in time $2^{O(k(g+1)^{3/2})} \cdot n^{O(1)}$, where $g$ is the genus of the input.

Finally, since any satisfying assignment $X$ produces a partition of the vertices of $C$ according to the properties described in Theorem 7 to find $X$ which minimizes $|S_X \setminus I|$ is LinEMSOL$_1$-expressible (see [8] for LinEMSOL details). Thus, the following holds.

Theorem 8. $\text{MinEC}^+_M$ is fixed-parameter tractable when parameterized by the clique-width of the input.

4 Conclusions

The energy complexity measure represents an interesting manner to analyse the activation of gates through a circuit. Previous works address energy complexity in threshold circuits as a model that simulates a neural network. By analyzing such a measure restricted to Boolean circuits, recent bounds in circuit complexity analysis were presented in [10] and [26].

In this paper, we introduce the discussion of energy complexity problems in terms of time complexity. We investigate the time complexity to computing the best-case energy complexity among satisfying assignments of monotone circuits (denoted by $\text{MinEC}^+_M$) and its respective version parameterized by the size of the solution ($k\cdot \text{MinEC}^+_M$). We prove that $\text{MinEC}^+_M$ is NP-complete on planar graphs, and that $k\cdot \text{MinEC}^+_M$ is W[1]-hard, but in XP. In addition, we show that $\text{MinEC}^+_M$ is fixed-parameter tractable when parameterized either by the treewidth of the input circuit or by the genus of the input plus the size of the solution. Besides that, we also remark that $k\cdot \text{MinEC}^+_M$ is FPT when restricted to instances with bounded in-degree, and that $\text{MinEC}^+_M$ is FPT concerning the clique-width of the directed graph/circuit $C$.

Since $k\cdot \text{MinEC}^+_M$ is in XP, we left open whether $k\cdot \text{MinEC}^+_M$ is in W[P]. Also, the parameterized complexity of $k\cdot \text{MinEC}^+_M$ on circuits that are planar but have NOT gates seems also interesting. In addition, the (parameterized) complexity of computing the worst-case energy complexity of circuits that are not monotone is also interesting.

Finally, we remark that there are several interesting energy complexity problems that can arise varying from the options “worst-case or best-case”, “general assignments or satisfying assignments”, “monotone or non-monotone”, and “planar or non-planar”.

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