A hardware-software co-design approach to minimize the use of memory resources in multi-core neuromorphic processors

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Both in electronics and biology, physical implementations of neural networks have severe energy and memory constraints. We propose a hardware-software co-design approach for minimizing the use of memory resources in multi-core neuromorphic processors, by taking inspiration from biological neural networks. We use this approach to design new routing schemes optimized for small-world networks and to provide guidelines for designing novel application-specific multi-core neuromorphic chips. Starting from the hierarchical routing scheme proposed, we present a hardware-aware placement algorithm that optimizes the allocation of resources for arbitrary network models. We validate the algorithm with a canonical small-world network and present preliminary results for other networks derived from it.

Index Terms—compiler, neuromorphic processors, hardware-software co-design, hierarchical routing, small-world networks, multi-core, scaling

I. INTRODUCTION

The large energy costs of Deep Neural Network (DNN) and Artificial Intelligence (AI) algorithms are pushing the development of domain-specific hardware accelerators [1]. Neuromorphic processors are a class of AI hardware accelerators that implement computational models of Spiking Neural Networks (SNNs) adopting in-memory computing strategies and brain-inspired principles of computation [2]–[4]. They represent a very promising approach, especially for edge-computing applications, as they have the potential to reduce power consumption to ultra-low (e.g., sub milliwatt) figures [5]. However, the requirement of SNN hardware accelerators to store the state of each neuron, combined with their in-memory computing circuit design techniques leads to very large area consumption figures, which limits the sizes and numbers of parameters of the networks that they can implement. The current strategy used to support the integration of large SNN models in these accelerators is to use multi-core architectures [6]–[9]. In these architectures, each core either emulates with analog circuits [6] or simulates with time-multiplexed digital circuits [7]–[9], neuro-synaptic arrays in which both the synaptic weight matrix and the network connectivity routing memory blocks occupy a significant proportion of the total layout area. Although the advent of nano-scale memristive devices can mitigate this problem by enabling the construction of dense cross-bar array structures for storing the weight matrices [4], the problem of allocating routing and connectivity resources to allow arbitrary networks (e.g., with all-to-all possible connections) at scale is of a fundamental nature that even memristors or 3D-VLSI technologies cannot solve [10].

Finding trade-offs to optimize both weight-matrix and connectivity/routing memory structures in multi-core neuromorphic processors can therefore have a significant impact on their total chip die area and on the size of the networks they can implement. Following the original neuromorphic engineering approach [11], in this paper, we look at animal brains for inspiration and propose brain-inspired strategies to perform this optimization. Specifically, we show that, by adopting small-world type network size/connectivity, we implement trade-offs that minimize area consumption requirements while still enabling the design of SNN architectures that can solve a wide range of relevant “edge-computing” problems, i.e., the types of sensory-motor processing problems that animals solve in the real world.

II. NEURAL NETWORK CONNECTIVITY SCHEMES

A. In biological systems

In animal brains, computation and other functions emerge from the interaction of neural areas. The diverse patterns of connections found within and across different brain areas are highly correlated with brain functions such as memory, vision and motor control [12]. Recent studies relating structure to function show how the wiring of the brain is far from homogeneous [12]: brain networks have short path length, high clustering, and a modular community structure [13]. These biological neural networks are often highly recurrent and have dense connections among nearby neurons and sparse connections to specific/far-away neurons, showing an exponential decay in the number of connections with increasing distance. In
other words, they express modular, small-world, heavy-tailed, and metabolically constrained organization characteristics. In small-world networks, most edges form small, densely connected clusters and the others maintain connections between these clusters (see Fig. 1). This mixture of local clusters and global interaction generates a structure that provides function and integration in the brain that can support a wide range of complex computations, cognition and behavior.

By restricting the types of SNNs that can be implemented in neuromorphic processors to small-world networks, we can dramatically reduce the memory required to specify the routing/connectivity schemes while still supporting a wide range of computations for solving pattern recognition and signal processing tasks.

B. Routing schemes for small-world networks

Multi-core neuromorphic processors usually use Network-on-Chip (NoC) designs for managing the communication of neurons between cores, especially asynchronous NoCs, which are consistent with the event-driven characteristics of neuromorphic processors, avoiding the use of a global clock, thereby reducing power consumption.

Different neuromorphic chips adopt different NoC architectures according to the application. Mesh architectures represent an easy way to build large-scale systems but at the cost of high routing power and latency. In flattened butterfly architectures, neuron cores belonging to the same row and column can communicate directly, with lower routing latency, but with the disadvantages of large area cost and poor multicasting support. In [15], the authors proposed a hierarchical architecture that overcomes some of these disadvantages. However, it uses off-chip Dynamic Random Access Memory (DRAM) to store the routing lookup table, which significantly increases power consumption.

Current methods for saving power, adopt in- or near-memory computing strategies. However, when on-chip memory is used to store configurable neuron connections the required hardware area increases proportionally with the number of neurons and synapses. For example in the Dynamic Neuromorphic Asynchronous Processor (DYNAP)-SE [6], which uses on-chip hierarchical routing, the routing memory takes around 80% of the area, even though a combination of point-to-point source-address routing and multicast destination-address routing was used to reduce memory usage.

In the small-world networks that we consider, the number of connections decays with distance, i.e., short-range connections are more common than long-range connections. Therefore, the strategy we propose to minimize memory requirements is to reduce the address space (i.e., the number of bits) required to map the (many) connections between nearby neurons, and allocate more bits for larger address space domains for the sparse long range connections.

Fig. 2 shows our hierarchical routing scheme designed to support small-world network connectivity with on-chip memory. It contains three levels of routers: R0 (not explicitly shown) connecting neurons inside the same core (red nodes), R1 connecting a fixed number of cores, and R2 connecting R1 routers. Inside a core, there is no specificity: independent of which neuron is sending a spike, all other neurons inside the same core can receive it. Thus, densely connected clusters are ideal for our core, where a crossbar is used (as R0), requiring almost no memory for these connections. Only a single bit is needed to connect all the neurons in the same core. We need to use more bits at higher router levels since the address space and specificity increase. Connectivity between cores depends on the distance between them. Nearby cores (that use only R1 routers) have an increase in specificity, i.e., a subset of neurons in a core can be the target of another core. At the R1 level, each core is divided into two halves, and two rows of one bit each are used to specify connections. Each neuron in a core can receive spikes from half of the neighboring cores. At the R2 level, connections can be made between neurons below different sets of R1 level routers. Since more neurons can be reached, more bits are necessary to describe the connections. However, fewer connections exist. At the R2 level, each core is divided into four fourths, so four rows of two bits each are used to specify connections. These connections have a constrained address space, i.e., since there is an upper bound on the router to which a spike can be sent, it is not necessary to take into account all of the neurons on the whole chip. In a model going up to the R2 level, each neuron needs two one-bit rows and four two-bit rows (i.e., 10 bits in total), allowing a fan-in from up to half of the neurons in the cores that can be reached through the R1 level plus a fourth of the neurons in the cores that can be reached through R2.

To support this reduction in address space we compute the routing distance by combining the use of computing logic and memory at each router module and update the distance information in the packet, as it transverses the router, thus reducing the address space to the bare minimum needed by the local cluster.

III. HARDWARE-SOFTWARE CO-DESIGN STRATEGIES

The scheme presented is optimal for Winner-Take-All (WTA)-like “canonical” networks that have a small-world connectivity matrix of the type shown in Fig. 3. To map other types of small-world networks in the hardware efficiently (i.e., minimizing memory usage), it is necessary to follow a hardware-software co-design approach, by developing a hardware-aware neuromorphic compiler. A compiler can be
Fig. 3: Example of a “Winner-Takes-All” (WTA) network implemented on a neuromorphic processor (from [16]). Blue blocks represent inhibitory synapses with negative weights, and red blocks represent excitatory synapses with positive weights.

Fig. 4: Canonical network example. A network with 16 neurons divided into four populations of four neurons each. Each population is all-to-all connected. The number of connections between populations depends on the distance between them.

seen as a translation machine, i.e., a program that can translate a high-level description of an SNN model into the hardware-specific configuration without exposing its fine structure. By following the hardware-software co-design approach proposed, in addition to placing SNN models on existing hardware, the tool developed will also allow us to derive specifications for new chip designs.

A. Hierarchical routing placement example

Here we present a placement algorithm that maps neurons of a user-defined neural network model onto physical neuron circuits within specific cores of the neuromorphic processor, while adhering to the specificity and distance-based connectivity constraints imposed by the hardware.

To validate the placement algorithm we test it with a canonical network, as depicted in Fig. 4, and a hypothetical neuromorphic processor comprising four cores, with four neurons per core. The canonical network considered has four populations of four neurons, where each population is all-to-all connected (Fig. 5a), and the number of connections between populations decays with distance. Figure 5b shows the number of connections between neurons and populations.

To place neurons in cores, we find cliques (i.e., the sets of neurons that have the largest number of connections among each other) in the graph of the network. Each clique defines a core. This gives us the number of cores needed to place the network. Figure 6 shows the result of grouping the neurons in the canonical network with this method.

With cores defined, we can calculate the distance between cores $i$ and $j$, with $i \neq j$ as:

$$\text{dist}[i][j] = \text{floor}(n/e(i,j)) + 1$$

where $n$ is the number of neurons per core, and $e(i,j)$ is the number of connections core $i$ is receiving from core $j$. Note that our distance is a quasi-metric that can be non-symmetric, i.e., the distance from core $i$ to $j$ might not be the same as from $j$ to $i$. The maximum distance in the network indicates the maximum router depth we need to use to map the network. We define the distance between the core and itself ($i = j$) as zero, and between two cores that do not share connections as $-1$. Having determined the number of cores and distances between cores, we can place connections, starting with the closest pairs.
software co-design approach, where a heuristic for placing an small-world networks. In this work, we presented a hardware-understanding of to optimize resource allocation in brain-line ware can help to advance AI for edge-computing taks, and our suitable option.

how the average number of neurons required in the hardware even smaller than using cores of size four). Also, we can see that also cores with two neurons canonical network was designed based on four cores of four neurons are generated. The total number of hardware neurons required to map network models depend on the design choice of core size (i.e., the number of neurons allocated per core). Three bars are plotted for cores of size 2 (blue), 3 (orange), and 4 (green).

Each neuron has a limited set of synapses; we try to allocate the nearby connections first because they are more numerous than the further-away ones. If no synapse is available, the connection is flagged as unplaceable. We consider the option of having a few fully programmable synapses to accommodate flagged connections.

IV. PRELIMINARY RESULTS

With this heuristic, using our tailor-made canonical network, we verify that the algorithm places the neurons correctly. To demonstrate how the algorithm performs, we test it using networks that deviate from the canonical example shown in Fig. created by removing an increasing number of nodes.

Figure compares the results of the placement algorithm deviation for three different network variations with one, two and three fewer nodes, and for cores of different size. Our canonical network was designed based on four cores of four neurons, but we can see that also cores with two neurons can map the network efficiently, with a small overhead (and even smaller than using cores of size four). Also, we can see how the average number of neurons required in the hardware increases when using three neurons per core, making it a not suitable option.

V. CONCLUSION

The development of domain-specific neuromorphic hardware also gives direction to guide new chip designs (e.g., specifying how many neurons/core, how many cores, and how many router hierarchy levels to use). The automatic mapping of networks done following biological constraints, and the specifications it provides for designing new multi-core SNN chips will allow us to best exploit future generations of neuromorphic processors. Our placement algorithm gives us some options for optimal hardware parameters for a specific set of network structures. We obtain different viable options for a chip design in terms of the number of neurons per core, cores, and synapses, which can be used to calculate the real area/memory necessary to design a new chip. This way, our co-design approach allows us to reduce the search space of new hardware parameters.

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