Investigation of characteristics of GaAs/AlGaAs p-i-n connecting tunnel diodes

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Abstract. Current-voltage and capacitance-voltage characteristics of tunnel diode structures with GaAs-n++/i-GaAs/i-AlGAs/AlGAs-p++ active region and i-layer thicknesses of 7.5 nm and 10 nm and epitaxial growth temperature of 450 °C and 500 °C have been studied. The tunnel diode structures grown by the molecular beam epitaxy technique are intended for application as connecting elements in multijunction photovoltaic converters of high-power monochromatic optical radiation. According to the results obtained, the peak tunnel current density of up to 200 A/cm² is achieved. Forward current-voltage and capacitance-voltage characteristics of tunnel p-i-n diode structures were measured at room temperature. The capacitance-voltage characteristics of the tunnel diodes being tested were obtained experimentally with the frequency dependence of S-parameters simulated within 10-1000 MHz at bias voltages of 0.4–1 V.

1. Introduction
The advancement of such a field of the modern science as radiophotonics requires that photovoltaic (PV) converters should be elaborated, capable of converting high-power laser radiation (>10W) in the pulsed generation mode with a high efficiency [1]. Such PV converters include monolithic multijunction PV converters (MJ PVCs) based on GaAs/AlGaAs semiconductor materials. An MJ PVC includes several series-connected p-i-n junctions with similar compositions and forbidden bands, but different photoactive junction depths [2]. The photoactive p-i-n junctions are connected by nanoheterostructure tunnel diodes (TDs) integrated in the structure. The improvement of the MJ PVC parameters is associated with the rise in efficiency due to the larger number of photoactive p-i-n junctions. The rise in the number of the photoactive p-i-n junctions leads to an even greater complication of the MJ PVC structure, larger number of connecting TDs and additional operations in the high-temperature treatment of a structure.

During the growth of degenerated GaAs/AlGaAs layers of connecting TDs by the MBE technique, the doping impurities, for example, Si (n-type) and Be (p-type), diffuse under heating. The impurity diffusion towards the p-n junction interface can result in the mutual overcompensation of the degenerated layers and in the subsequent degradation of the TD characteristics [3, 4]. The ways to prevent such degradation consist in lowering the epitaxial growth temperature and including an intermediate undoped i-layer with a thickness of several nanometers between the degenerated p++ and n++ layers. In this study, measurements were
performed to obtain forward dark current-voltage characteristics (IVCs) and high-frequency capacitance-voltage characteristics (CVCs) of two p-i-n TDs structures in the GaAs-n++/i-GaAs/i-Al0.2Ga0.8As/Al0.2Ga0.8As-p++ system marked by A and B with different i-layer thicknesses and different epitaxial growth temperatures.

2. Technology of tunnel p-i-n diodes

The structures of the connecting p-i-n TDs were obtained by the MBE technique in a SemiTEq two-reactor installation (Russia). Figure 1 presents the design of the TD structures being tested. The TDs were grown on 350-µm-thick p+GaAs:Be(001) substrates. All the structures included intermediate undoped i-layers between the degenerated n and p-type layers with a technological thickness of 7.5–10 nm and concentration of impurities 5×10^{16} cm^{-3}. To raise the effective doping level of the degenerated TD layers, modulated δ-doping of Si into the n++ region and Be into the p++ region was applied by forming three δ-layers with impurity concentration exceeding 1×10^{19} cm^{-3}, spaced by 2.5-nm undoped GaAs and Al0.2Ga0.8As layer with impurity concentration of 5×10^{16} cm^{-3}. Structures A and B were tunnel p-i-n heterojunctions with an undoped i-region consisting of two layers: 2.5-nm-thick i-GaAs (structure A) or 5-nm-thick (structure B) and 5-nm-thick i-Al0.2Ga0.8As layer for both structures and an active GaAs-n++-(3×δ-Si)/i-GaAs/i-Al0.2Ga0.8As/Al0.2Ga0.8As-p++-(3×δ-Be) region.

![Figure 1. Design of the structure with an i-GaAs thickness of 2.5 nm (structure A) and 5 nm (structure B) in the active p-i-n region of a TD.](image)

The epitaxial growth temperature of structure A was 500 °C, and that of structure B, 450 °C. The doping levels of the TD active region were 1.7×10^{19} cm^{-3} in the degenerated region δ-doped with n-type Si, and 4×10^{19} cm^{-3} in that δ-doped with p-type Be.

Arrays of diode mesas with resistive AuGe-Ni-Au and AgMn-Ni-Au contacts were formed to n and p-type GaAs, respectively, by the post-growth technology without passivation of the side surface on each epitaxial structure. The mesa diameter was 225 µm. The contact alloying temperature was 500 °C.

According to the concentration profiles of doping atoms in structures A and B, measured by using the depth profiling method of dynamic secondary ion mass spectrometry on the IMS-7f
(CAMECA, France) installation, a diffusion of the Be impurity into the i-layer and then towards the p-n junction interface is observed. In both structures, there is no ideally pure i-layer, and we can only speak about its “effective” thickness due to the overcompensation of the doping impurities. Nevertheless, as shown below, the CVCs indicate that there is an “effective” i-layer and it noticeably affects the peak tunnel current density.

3. Obtaining of p-i-n TD characteristics
3.1. Current-voltage characteristics of the p-i-n TDs

Directly on the epitaxial wafers of A and B structures, measurements were carried out at a positive bias of up to 0.6 V (T=300 K) to obtain current voltage characteristics (IVCs) of TDs with a mesa diameter of 225 µm. Figure 2 presents a set of IVCs obtained for A - (a) and B - (b) structures. According to these characteristics, structure A with a technological i-layer thickness of 7.5 nm and epitaxial growth temperature of 500 °C has a significant spread in the peak current density (∆J_{peak}) of about 55%, from 90 to 200 A/cm² (figure 2a). For 90% of the diodes, the peak tunnel current density lies in a narrower range, from 90 to 115 A/cm². The rest 10% of the diodes located on the periphery of the epitaxial wafer have a substantially greater peak current density of about 200 A/cm² (figure 2a, curve 2). The average peak current density for A wafer is 111 A/cm² (figure 2a, curve 1). Structure B with an i-layer thickness of 10 nm and epitaxial growth temperature of 450 °C demonstrates a smaller ∆J_{peak} of about 20% at tunnel current densities in the range from 125 to 150 A/cm² (figure 2b) and a higher average peak current density, 131 A/cm² (figure 2b, curves 1).

Figure 2. Forward dark IVCs of TDs with a mesa diameter of 225 µm: (a) for A structure, where (curve 1) J_{peak}=111 A/cm², and (curve 2) J_{peak}=190 A/cm² and (b) for B structure, where (curve 1) J_{peak}=131 A/cm²

It should be noted that the ratio between the peak tunnel current density and the valley current density (J_{peak}/J_{val}) is 8.5 for the averaged IVC of structure A and 2.3 for structure B. According to [5], the number of point defects substantially decreases with increasing annealing temperature of the GaAs/Al_{x}Ga_{1-x}As epitaxial structure grown by the MBE technique. This, in turn, results in a drop of the valley current density (J_{val}) and in a rise of the (J_{peak}/J_{val}) ratio.

3.2. Capacitance-voltage characteristics of the p-i-n TDs

CVCs measurements of tested TDs were carried out to estimate the p-i-n TDs depletion region width. For this purpose, the results of IVC measurements (figure 2) were used to select
TDs with the average values of the peak tunnel current density of both structures (figure 2a, curve 1; figure 2b, curve 1) and also a specimen from the periphery of structure A with the maximum tunnel current density of about 200 A/cm² (figure 2a, curve 2).

It was impossible to measure the TD CVCs by the standard low-frequency methods [6]. To obtain CVCs, the TD specimens were mounted on a wafer-adapter, with which a measuring probe with a wave impedance $Z_0=50$ Ohm (MPI T40A-GSG500) was brought in contact. The frequency dependences of the S-parameters were measured at positive bias voltages for GaAs-n++/i-GaAs/i-Al0.2Ga0.8As/Al0.2Ga0.8As-p++ TDs. From these dependences, the parameters of the equivalent circuit for the connecting TDs, including the TD capacitance, were found [6, 7]. In our study, the S-parameters were measured with a vector analyzer (Rohde & Schwarz ZNB40) in the frequency range 10-1000 MHz with increments of 1 MHz. Before the measurements, calibration against reference samples on the calibration substrate (MPI AC-5) was performed. During the calibration, the power of the high-frequency signal of the vector analyzer was 0.1 mW. The dependence of the $S_{11}$ parameter on the signal frequency was measured. The bias voltage was varied within the range 0.4 – 1 V, which corresponded to the TD IVC curve portion after the “valley” (figure 2). Then the $S_{11}$ characteristics was fitted with consideration for parameters of the equivalent circuit presented in the inset in figure 3a.

The frequency dependences of $S_{11}$ parameter were used to determine for each point the TD impedance in accordance with the following expression:

$$Z = 50 \frac{1 + S_{11}}{1 - S_{11}}$$

(1)

For each bias voltage, the frequency dependences of the real (figure 3a) and imaginary (figure 3b) parts of the impedance were constructed. For the equivalent circuit, the frequency dependence of the impedance is described by the expression:

$$Z(f) = R_S + i2\pi fL_S + \frac{1}{R_j + i2\pi fC_j}$$

(2)

where $R_S$ is the series resistance of a TD with a wafer-adapter, $L_S$ is the series inductance of a TD wafer-adapter, $C_j$ is the TD p-i-n junction capacitance, and $R_j$ is the resistance of the TD p-i-n junction. The $R_S$, $R_j$, $C_j$ parameters were determined by fitting of the real part of function (2) by the Levenberg–Marquardt method. The value of $L_S$ for constructing a plot of the impedance imaginary part was selected for each specimen by hand and was considered a constant in the range 0.5-0.55 nH.

Figure 3 presents experimental (curves 1-3) and calculated (curves 1’-3’) frequency dependences of the real (figure 3a) and imaginary (figure 3b) parts of the impedance for three TD specimens (figure 2) at a bias voltage of 0.7 V. The symbols (curves 1-3) in figure 3 show the impedance characteristics calculated on the basis of the values measured for $S_{11}$ parameter independent on signal frequency in accordance with expression (1). The solid lines (curves 1’-3’) represent the impedance values obtained by fitting in accordance with expression (2) and demonstrate a good agreement with the experimental values.

The CVC $C_j$ parameters obtained for three TDs (figure 2) at different bias voltages are presented in figure 4 (curves 1-3). According to the CVCs obtained for the TDs with $J_{peak}=111$ A/cm² (figure 4, curve 1) and $J_{peak}=131$ A/cm² (figure 4, curve 2), a monotonous rise of capacitance is observed in the voltage range of 0.4-0.7 V, whereas, for the periphery specimen ($J_{peak}=190$ A/cm²) in the voltage range of 0.6-1 V, capacitance is practically invariant. In this case, for the B wafer, the average TD capacitance appears to be noticeably smaller than that for the A wafer, what can be explained by a greater depletion region width. At the same time, capacitance-voltage measurements demonstrated an almost doubled TD capacitance drop on
the periphery of the structure A epitaxial wafer, which suggests that a noticeable influence is exerted by an “effective” i-layer.

Figure 3. Experimental (curves 1-3) and calculated (curves 1’-3’) frequency dependences of the real (a) and imaginary (b) parts of the impedance, measured at a forward bias voltage of 0.7 V for TDs with structure A (curves 1 and 3) and structure B (curve 2): $J_{\text{peak}}=111 \text{ A/cm}^2$ (curve 1, 1’), $J_{\text{peak}}=131 \text{ A/cm}^2$ (curve 2, 2’), $J_{\text{peak}}=190 \text{ A/cm}^2$ (curve 3, 3’). $R_S$ is the series resistance, $L_S$ is the series inductance, $C_j$ is the TD capacitance, and $G_j$ is the TD conductance.

Figure 4. CVCs of three TD specimens: $J_{\text{peak}}=111 \text{ A/cm}^2$ (curve 1, structure A), $J_{\text{peak}}=131 \text{ A/cm}^2$ (curve 2, structure B), $J_{\text{peak}}=190 \text{ A/cm}^2$ (curve 3, structure A).

The depletion region width of the p-i-n junction was calculated using the CVCs (figure 4, curves 1-3):

$$d = \frac{\varepsilon \varepsilon_0 S}{C}$$

(3)

where, $\varepsilon$ is the dielectric constant of the semiconductor, $\varepsilon_0$ is the permittivity of free space, $S$ is the cross-section of the p-n junction, and $C$ is capacitance. For TD structure A ($T=500 \degree \text{C}$) with peak tunnel current densities of 111 and 190 A/cm$^2$, the depletion region
widths were 6.6 and 14.5 nm, respectively. For TD structure B (T=450 °C) with peak tunnel current of 131 A/cm², the depletion region width was 7.1 nm.

4. Conclusion
An experimental study of the characteristics of connecting tunnel p-i-n diodes based on n++GaAs/i-GaAs/i-Al0.2Ga0.8As/p++Al0.2Ga0.8As heterostructure was carried out. An analysis of the forward dark IVCs of p-i-n TDs based on structure A with technological thickness of the i-layer of 7.5 nm and epitaxial growth temperature of 500 °C revealed the following: a substantial peak current density scatter (∆J_peak) of about 55%, average tunnel peak current density of 111 A/cm² and current densities of periphery diodes of about 200 A/cm²; for structure B with technological thickness of the i-layer of 10 nm and epitaxial growth temperature of 450 °C, ∆J_peak is about 20%, the average tunnel peak current is 131 A/cm².

On the basis of frequency dependence measured for S11 parameter in the range 10-1000 MHz at bias voltages of 0.4–1 V, the equivalent circuit parameters were determined, and the CVCs of the TDs were constructed. According to the CVCs, TDs with average peak current density show a monotonous rise of capacitance with increasing bias voltage, whereas for the TDs fabricated on the periphery of the epitaxial wafer A, the capacitance is nearly invariable. At a forward bias voltage of 0.7 V, the average capacitance was 680 pF for the structure with a technological i-layer thickness of 7.5 nm (J_peak=111 A/cm²), and 615 pF for the structure with a technological i-layer of 10 nm (J_peak=131 A/cm²). At the same time, the CVCs exhibit a doubled decrease in the TD capacitance on the periphery of the epitaxial wafer of the structure with a 7.5 nm i-layer to 314 pF.

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