1 INTRODUCTION

With the dawn of the big data era, managing the massive volume of data generated by data-intensive applications becomes extremely challenging, particularly for scientific simulations running on leadership-class high-performance computing (HPC) systems and experiments running on federated instruments and sensor platforms. For instance, the XGC dynamic fusion simulation from the Department of Energy (DoE)'s Princeton Plasma Physics Laboratory can generate 1 PB per day when running on DoE’s fastest supercomputers, and may soon generate 10 PB per day. The Square Kilometer Array plans to generate data at 1 PB/s within 10–20 years. Few storage systems can keep up with such data rates. Moreover, even if all data could be stored, the high costs of creating, accessing, reducing, and otherwise operating on such representations. We describe here highly optimized data refactoring kernels for GPU accelerators that enable efficient creation and manipulation of data in multigrid-based hierarchical forms. We demonstrate that our optimized design can achieve up to 264 TB/s aggregated data refactoring throughput—92% of theoretical peak—on 1024 nodes of the Summit supercomputer. We showcase our optimized design by applying it to a large-scale scientific visualization workflow and the MGARD lossy compression software.

Index Terms—Multigrid, Data refactoring, GPU

the limited capacity of fast storage such as parallel file systems means that data are eventually moved to slower storage, such as archival storage systems. For example, on Oak Ridge National Laboratory (ORNL)'s Summit supercomputer, data can only be kept on the parallel file system for 90 days before it is either moved to archival storage systems such as HPSS or permanently deleted. Once moved to archival storage, it can take weeks or longer to retrieve for analysis.

There are no universal solutions to the many technical and domain-specific challenges of large data. In fact, from the domain scientist's perspective, being able to store large amounts of data may not lead to more scientific discoveries. The most valuable scientific insights often come from just a small portion of the original data. Domain scientists would like to be able to retrieve only enough data to guarantee a certain accuracy, so that desired results can be produced when applying a type of analysis on the reduced data representation. However, it is challenging to use existing data compression techniques, given differing data accuracy needs of different analyses, since data need to be compressed and stored separately for different needed accuracies, which brings high computational and storage costs.

Data refactoring is the capability of building a data representation in a hierarchical form such that a reader can easily, efficiently, and transparently access data at varying degrees of fidelity. To enable this capability, new algorithms such as multigrid-based hierarchical data refactoring have recently been developed by the applied mathematics community. That data refactoring approach models a dataset with a series of hierarchically organized coefficient classes, such that an approximation of the original data with a specified fidelity can be reconstructed by using different numbers of coefficient classes. We call the process of building coefficient
classes \textit{decomposition} and the process of reconstructing data from coefficient classes \textit{recomposition}.

Hierarchical data refactoring gives both data producers (e.g., scientific simulations) and consumers (e.g., data analysis routines) the flexibility to store, transport, and access data to satisfy space and/or accuracy requirements. For example, data sharing between two coupled scientific applications \cite{10} can be optimized by intelligently moving coefficient classes through multi-tiered-storage systems (e.g., storage systems containing non-volatile memory, magnetic disks, and tapes) and/or networks based on available capacity and bandwidth. In Figure 1 simulation data are refactored into five coefficient classes and then shared with data analysis routines via multi-tiered-storage systems and networks. When accuracy can be estimated based on the number of selected coefficient classes, users can control the accuracy of the reconstructed data while storing and reading the data. If user-defined accuracy requirements indicate that information encoded in the first four coefficient classes are enough for subsequent data analyses, then the fifth coefficient class can be ignored. Then, the four coefficient classes can be intelligently shared over the storage systems and network based on their size, available bandwidth/capacities, and accuracy requirements from data analysis routines. In the figure, Data Analysis Routine 1 needs only two coefficient classes to achieve desired accuracy, while Routine 2 needs four. The ability to choose a reduced number of coefficient classes allows users to reduce data movement costs substantially.

As great as the benefits of reduction in data movement and management costs may be, if the decomposition and recomposition routines are too expensive, then the total process is less useful in production. The use of Graphics Processing Units (GPUs) has shown significant increases for scientific computations that can be adopted to the streaming execution model. These increases are due to the high parallel computational power and memory throughput in GPUs. As the algorithms involved in multigrid-based hierarchical data refactoring are highly parallelizable, using GPUs to accelerate its routines is attractive. Also, we anticipate that if used with merging GPU communication technologies (e.g., NVLink, GPUDirect RDMA, etc.), GPU data refactoring would be greatly beneficial for speeding up data sharing for both CPU- and GPU-based scientific applications.

We focus here on accelerating the two major routines, decomposition and recomposition, in multigrid-based data refactoring on GPUs and evaluating the benefit for producer and consumer applications. Although the multigrid-based algorithms are naturally parallelizable, achieving good performance require carefully designed parallel algorithms together with deep optimizations for GPU architectures. Our specific contributions, and the sections in which they are described, are as follows.

In §3 we describe the first multigrid-based data refactoring routines for modern GPU architectures. Specifically, we present three optimized kernels for data refactoring on GPU. These optimizations can balance both minimizing memory footprint and improving memory access efficiency. Based on the optimized kernels we introduce the designs of GPU data refactoring that is optimized for spatiotemporal or high dimensional scientific data. We also provide optimizations for consumer-class GPUs commonly used in edge systems and dense multi-GPU architectures commonly used in HPC systems.

In §4 we demonstrate our design by implementing the state-of-the-art non-uniform multi-dimensional multigrid-based data refactoring algorithms of Ainsworth et al. \cite{7, 8, 9}, and show that our methods perform well on both a consumer-class desktop and the Summit supercomputer, achieving 160× and 15× speedups compared with state-of-the-art CPUs and GPUs, and 264 TB/s throughput on 1024 Summit nodes.

In §5 we use two common scenarios in scientific computing to showcase our work: 1) reducing data movement costs between simulations and in situ visualization applications; and 2) speeding up lossy compression for scientific data.

\section{Background}

\subsection{Theory of multigrid-based hierarchical data refactoring}

The multigrid-based hierarchical data refactoring developed by Ainsworth et al. support nonuniformly-spaced structured multidimensional data, commonly found in scientific computations, by using hierarchical representations to approximate data. Specifically, they decompose data from fine grid representation to coarse grid representation in an iterative fashion, with a global correction to account for the impact of missing grid nodes in each iteration. If we use functions to represent the discrete values continuously, the decomposition from fine grid level \( l \) to coarser grid level \( l - 1 \) can be formulated with the notation in Table 1 as follows,

\begin{equation}
Q_{l-1}u = Q_{l}u - (I - \Pi_{l-1})Q_{l}u + (Q_{l-1}u - \Pi_{l-1}Q_{l}u)
\end{equation}

where the piecewise linear function \( u \) takes the same values as the original data for each node; \( Q_{l-1}u \) and \( Q_{l}u \) are the function approximations of \( u \) at levels \( l - 1 \) and \( l \) respectively; \( (I - \Pi_{l-1})Q_{l}u \) is the difference between the values of the fine grid nodes at level \( l \) and their corresponding piecewise linear approximations; and \( (Q_{l-1}u - \Pi_{l-1}Q_{l}u) \) is the global correction. According to Eq. (1), two major steps are involved at each level of the multigrid decomposition: \( 1) \) compute coefficients for the current multigrid level \( l \); and \( 2) \) compute the global correction and add it to the nodes in the next coarse grid (level \( l - 1 \)). In what follows, we introduce how to compute coefficients and corrections.

\subsection{Compute coefficients}

The coefficients store the difference between the data approximated by nodes at levels \( l \) (i.e., \( N_{l} \)) and \( l - 1 \) (i.e., \( N_{l-1} \)) before corrections are added. Since \( N_{l-1} \) is contained in \( N_{l} \) its nodes have the same values in both levels; thus the nonzero differences only occur on nodes in \( N_{l} \setminus N_{l-1} \). Figure 2 shows how coefficients are calculated along one

\begin{table}[ht]
\centering
\caption{Notation used in algorithms, formulations, figures}
\begin{tabular}{||c|c||}
\hline
Symbol & Description \\
\hline
\hline
\( u \) & Function represented by the original data. \\
\hline
\( N_{l} \) & Nodes at grid level \( l \). \\
\hline
\( Q_{l} \) & Coefficients at grid level \( l \). \\
\hline
\( V_{l} \) & Function space with respect to \( N_{l} \). \\
\hline
\( I \) & The \( L^{2} \) projection onto \( V_{l} \). \\
\hline
\( \Pi \) & The piecewise linear interpolant in space \( V_{l} \). \\
\hline
\hline
\end{tabular}
\end{table}
dimension through linear interpolation. It can be generalized to multi-dimensional cases easily by using multi-linear interpolations for approximation.

2.1.2 Compute correction

Ainsworth et al. prove that the correction is the orthogonal projection of the calculated coefficients at grid level \( l \) onto \( V_{l-1} \), thus, adding the correction to the next coarse grid better approximates data in the current grid. To explain, we first define \( z_{l-1} \) as the correction for grid at level \( l-1 \). From Eq. (1), we have that:

\[
z_{l-1} - (I - \Pi_{l-1})Q_l u = -(Q_l - Q_{l-1})u \in V_{l-1}^\perp \tag{2}
\]

If we apply \( L^2 \) projection at grid level \( l-1 \) (i.e., \( Q_{l-1} \)) to both sides of Eq. (2) it leads to a zero function since it belongs to \( V_{l-1}^\perp \). Also, since \( z_{l-1} \) is in \( V_{l-1} \), \( Q_{l-1}z_{l-1} = z_{l-1} \). So, we can see that \( z_{l-1} \) is the orthogonal projection of the coefficients onto \( V_{l-1}^\perp \). Namely, \( Q_{l-1}(I - \Pi_{l-1})Q_l u = z_{l-1} \).

The correction can thus be computed by solving a variational problem: find \( z_{l-1} \in V_{l-1}^\perp \) such that \( (z_{l-1}, v_{l-1}) = ((I - \Pi_{l-1})Q_l u, v_{l-1}) \) for all \( z_{l-1} \in V_{l-1}^\perp \). Then, \( z_{l-1} \) can be found by solving linear systems \( M_{l-1}z_{l-1} = f_{l-1} \) where \( M_{l-1} \) is a tensor product of the mass matrices [13] of each dimension, i.e., \( M_{l-1} = M_{l-1}^1 \otimes M_{l-1}^2 \otimes \cdots \otimes M_{l-1}^d \), where \( d \) is the number of dimensions and \( f_{l-1} \) is the load vector, which can be calculated using: \( f_{l-1} = R_l M_l \text{vec}(C_l) \), where \( R_l \) is a transfer matrix that converts basis functions from \( V_l \) to \( V_{l-1} \) and \( C_l \) is the coefficient matrix at level \( l \), which consists of computed coefficients at \( N_l \setminus N_{l-1} \) and zeros at \( N_{l-1} \).

Overall decomposition/recomposition process

Figure 2 illustrates this process on a 5x5 2D dataset. The original data is on the left, and the refactored representation is on the right. The decomposition process moves from left to right (i.e., from finest to coarsest grid) and involves four steps: computing coefficient and computing correction (ILA.1 and ILA.2) for each of the two levels. For multi-dimensional data, the computation of correction is done by working on each dimension in a prescribed order [14]; in this 2D example, it proceeds first along the rows and then along the columns. Recomposition moves from right to the left: i.e., from coarsest to finest grid. There are again four total stages, but these occur in the reverse order. The approximation of the original data is produced after recomposition. Based on how coefficients are omitted in recomposition, an error bound on data approximation can be computed [9].

2.2 Existing GPU-based data refactoring

The state-of-the-art MGARD [15] GPU-based data refactoring system redesigns original serial algorithms to expose high parallelism to suit the many-core architecture of modern GPUs. It achieves \( O(n^3) \) thread concurrency for computing coefficients and \( O(n^2) \) thread concurrency for computing corrections, and applies node reordering such that each kernel can take advantage of coalesced memory accesses. Theoretically, with large inputs, these levels of thread concurrency are more than enough to fully occupy GPU cores that can help achieve high data refactoring throughput. However, performance evaluation shows that it still suffers from underutilized memory throughput, achieving less than 10% of theoretical peak.

3 Designing GPU-accelerated data refactoring

We next discuss the design of our GPU-accelerated multigrid-based hierarchical data refactoring method. We first focus on the optimizations for each computing kernel involved in data refactoring. Then, we discuss how to use heuristic auto tuning to maximize the refactoring throughput. Finally, we provide overall designs of spatiotemporal refactoring algorithms with optimizations.

3.1 Designing optimized GPU multigrid kernels

Decomposition and recomposition each involve three major steps: 1) computing coefficients; 2) mass-transfer matrix multiplication; and 3) correction solver. Based on their computation pattern, we can classify them into three categories: grid processing style; linear processing style; and iterative processing style. We design kernels dedicated for each processing style.
Grid processing style has the characteristic of processing data grid-wise. Namely, it processes nodes within the domain of a grid in a certain resolution level (e.g., $N_l$) or between neighboring levels (e.g., $N_l$ and $N_{l-1}$). In the multigrid-based data refactoring, the calculation of coefficients follows the grid processing style. The major calculation is to compute the interpolation at nodes in $N_l \setminus N_{l-1}$ using nodal values in $N_{l-1}$. Parallelization can favor either interpolation operations (i.e., parallelism $\propto O(N_l \setminus N_{l-1})$) or accessing nodal values (i.e., parallelism $\propto O(N_l)$). The former can lead to a less thread divergence, while the latter can achieve a higher memory access efficiency. The computation of coefficients is a memory bound operation, as its time complexity is $O(n)$. Therefore, it is essential to optimize in favor of memory access efficiency instead of computation. This is also chosen in the state-of-the-art GPU data refactoring [15].

The key strategy they used to optimize for memory access is to use shared memory to cache a block of data for processing, of which the nodes values are loaded/stored in a coalesced-friendly fashion. However, we identify that keeping efficient data movement on memory bound computation is not enough to achieve good performance. The level of thread divergence in computation can still have a great impact on the overall performance and sometimes it can wrongly convert computation from memory bound to compute bound. The reason is threefold: 1) high degrees of thread divergence can great increase the total cycles cost in computation; 2) variable floating point operation counts caused by different interpolation types further brings workload imbalance which leads to longer idling cycles; 3) as shown in Figure 4 some thread blocks also need to calculate coefficients in the ghost region, which exacerbate the effect of thread divergence.

However, we found that keeping efficient memory access patterns is not exclusive with having low thread divergence. In designing our GPK, we propose to decouple memory access and computation on nodal values in terms of thread-node assignment through a thread reassignment strategy. Specifically, we use two different thread-node assignment for loading/storing nodal values and computing interpolations such that we keep maintaining efficient coalesced memory access pattern while having one warp process the same type of interpolations along the same dimension.

Figure 5 shows the conceptual execution flow of one thread block using existing approach and our proposed GPK when computing coefficients. As nodes in $N_l$ need to be shared with neighbors during interpolation operations, we let each thread block coordinate work on a block of data and use shared memory as a scratch space. We organize threads such that threads in the same warp load values that are consecutive in memory to achieve efficient coalesced memory access patterns. For computing, we apply a thread re-assignment strategy to achieve divergence-free execution.

### 3.1.2 Linear processing kernel (LPK)

The linear processing style computes stencil operations on elements in vectors along one dimension in a grid. In multigrid-based data refactoring, when multiplying the mass and transfer matrices with computed coefficients, the computations become stencil operations, as the matrices are defined as:

$$M_{ij} = \begin{cases} 2(h_i + h_{i+1}) & \text{if } i = j \\ h_i & \text{if } |i - j| = 1 \\ 0 & \text{else} \end{cases}$$

$$R_{ij} = \begin{cases} 1 & \text{if } i = j/2 \\ r_{j-1} & \text{if } i = (j-1)/2 \\ 1 - r_j & \text{if } i = (j+1)/2 \\ 0 & \text{else} \end{cases}$$

where $h_i$ is the spacing between the $i^{th}$ node, and the $i + 1^{th}$ node and $r_i = h_i/(h_i + h_{i+1})$. As shown in Figure 6(a), each value of each node needs to be computed using the original values of its neighbors, which means it cannot update its stored value unless all neighbors have finishing using its original value for computation. Such data
dependencies present a dilemma for kernel design: common out-of-place designs (i.e., element-wise parallelism) bring high parallelism but also high memory footprint; on the other hand, in-place design (i.e., vector-wise parallelism), used in [15], sacrifices the opportunity to exploit intrinsic parallelism.

To eliminate this dilemma, we design a novel linear processing kernel (LPK) with four optimizations. First, we change the original computation from in-place to out-of-place to achieve finer-grain parallelism. Second, we merge the mass and transfer matrices to reduce computational costs. We call the new matrix mass-trans, which is defined as:

\[
K_{ij} = \begin{cases} 
(2 + r_{j-2})h_{j-1} + (1 + r_j) & \text{if } i = j/2 \\
(2r_{j-2} + 1)h_{j-1} + 2r_{j-2}h_{j-2} & \text{if } i = (j - 1)/2 \\
(3 - 2r_j)h_{j+1} + 2r_{j+1}h_{j+1} & \text{if } i = (j + 1)/2 \\
r_{j-2}h_{j-2} & \text{if } i = (j - 2)/2 \\
(1 - r_j)h_{j+1} & \text{if } i = (j + 2)/2 \\
0 & \text{else}
\end{cases}
\]

Third, we use shared memory to cache a tile of nodes to allow sharing of coefficients (input) between different threads, so as to reduce total accesses to global memory. Finally, to reduce extra memory footprint we use kernel fusion technique to fuse the operation of copying coefficients with the multiplication of the mass-trans matrix with coefficients along the first dimension. By eliminating the need of storing a copy of the computed coefficient in the workspace, we avoid large increase in the overall memory footprint.

\[c' = \begin{pmatrix} 
(2 + r_{j-2})h_{j-1} + (1 + r_j) & (2r_{j-2} + 1)h_{j-1} + 2r_{j-2}h_{j-2} & (3 - 2r_j)h_{j+1} + 2r_{j+1}h_{j+1} & r_{j-2}h_{j-2} & (1 - r_j)h_{j+1} & 0 \\
\end{pmatrix}
\]

\[c' = \begin{pmatrix} 
(2 + r_{j-2})h_{j-1} + (1 + r_j) & (2r_{j-2} + 1)h_{j-1} + 2r_{j-2}h_{j-2} & (3 - 2r_j)h_{j+1} + 2r_{j+1}h_{j+1} & r_{j-2}h_{j-2} & (1 - r_j)h_{j+1} & 0 \\
\end{pmatrix}
\]

3.1.3 Iterative processing kernel (IPK)

The iterative processing style has the characteristic of processing nodes in a grid that contains strong data dependencies such that nodes have to be processed iteratively in a certain order. In multigrid-based data refactoring, the correction solver needs to solve for the corrections. We use the Thomas algorithm [16], which needs a forward and a backward pass on the load vector. Since the load vectors along one dimension can be solved independently, they can be solved in parallel. This level of parallelization is well exploited in [15]. Specifically, they assign each thread to handle the solving process of one load vector independently. Although this brings high thread concurrency with divergence free execution, it actually suffers from inefficient memory accesses for two reasons: first when solving vectors on leading dimension full coalesced memory access cannot be achieved (actual achieve efficiencies are about only 12% and 25% for single and double precision data); second, compared with GPK and LPK, IPK only has \(O(n^2)\) degrees of thread concurrency, which may brings less on-the-fly memory accesses to fully utilizes the memory bandwidth.

To address this issue, we proposed a novel processing kernel, IPK, that can guarantee efficient coalesced memory access patterns with high concurrent memory accesses. We first parallelize the vectors by assigning a batch to a thread block. Since the update of each node depends on its neighboring elements, we use shared memory as scratch space to avoid polluting the un-processed nodes. Specifically, we let each thread block iteratively work on a segment of load vectors at a time until the whole vector is updated. Thus, as shown in Figure 7 during the computation we divide the elements in the vectors into six regions: 1) the processed region stores updated elements (gray); 2) the main region consists of elements that the current iteration is working on (green); 3) and 4) due to dependence on the neighboring elements, the original value of elements in the two ghost regions (red and cyan) are needed to update the elements in the main region; 5) for better streaming processor utilization, we pre-fetch data needed for the next iteration (purple); and 6) we mark the unprocessed region as in block. The regions move forward as the computation proceeds. One challenge to design the algorithm is to simultaneously consider maximizing coalesced global memory access patterns, minimize bank conflict in accessing shared memory, and minimize thread divergence. We use a dynamic data-thread assignment strategy [17–21] to optimize both the accessing and computation of coefficients.

3.2 Heuristic Performance Auto Tuning

When launching each proposed kernel, choosing the execution parameters is important for its achieving good performance, since even with optimized design they can still greatly impact the efficiency of memory accesses, warp divergence, context switch overhead, etc. Auto tuning technique is an effective approach for searching the optimum configurations. However, brutal force search can be expensive and thus impractical. Thus, we propose to use a heuristic auto tuning approach guided by theoretical performance models for our GPU data refactoring. We first build performance models for the three kernels we proposed. Among all tunable execution parameters, we find that the
size of the thread block \((B_x, B_y, B_z)\) plays an important role in determining each kernel’s performance. Since we eliminate majority of the thread divergence and inefficient computations, we assume the memory load/store take the majority time, so we only consider total amount of memory transactions with their efficiency. The estimated execution time of each kernel can be modeled as:

\[
T_{\text{GPK}} = \left[ B_x + 1/(S/L) \right] \cdot (S/L) \cdot (B_y + 1) \cdot (B_z + 1) \cdot [N/B_x] \cdot [N/B_y] \cdot [N/B_z] \cdot 2L \cdot (1/\text{Peak Mem. Band.})
\]

\[
T_{\text{LPK}} = \left[ (B_x/(S/L)) \cdot S/L + 2S/L \right] \cdot B_y \cdot B_z \cdot [N/B_x] \cdot [N/B_y] \cdot [N/B_z] \cdot 2L \cdot (1/\text{Peak Mem. Band.})
\]

\[
T_{\text{IPK}} = \left[ \frac{G}{(S/L)} \cdot (S/L) + \left[ B_x/(S/L) \right] \cdot S/L \cdot [N/B_x] \right] \cdot B_y \cdot B_z \cdot [N/B_y] \cdot [N/B_z] \cdot 2L \cdot (1/\text{Peak Mem. Band.})
\]

where \(S\) is the number of bytes per memory transaction, \((32 \text{ in our test GPU}; L \text{ is bytes per float (4 for single, 8 for double); and } G\) is the dimension of the next ghost region, set to \(S/L\) so that ghost data can fit into exactly one memory transaction and do not consume too much shared memory. Table 2 shows the ranking of estimated performance using seven typical thread block size configurations. Numbers in red represent the actual best configuration as determined by profiling. We can see our performance model can help us predict relationship between different configurations in terms of performance with relative high accuracy. It helps us narrow down the searching space for auto tuning. For instance, in our following evaluation, we only let the auto tuning search and pick among the estimated top three configurations to save time.

Table 2: Ranking of estimated performance of seven typical thread block size configurations; actual best in red.

| \(B_x\) | \(B_y\) | \(B_z\) | \(\text{GPK}\) | \(\text{LPK}\) | \(\text{IPK}\) |
|---|---|---|---|---|---|
| 2 | 2 | 2 | 7 | 7 | 7 |
| 3 | 4 | 4 | 6 | 6 | 6 |
| 4 | 4 | 4 | 3 | 3 | 3 |
| 4 | 4 | 16 | 2 | 4 | 3 |
| 3 | 4 | 32 | 1 | 3 | 4 |
| 2 | 2 | 64 | 5 | 2 | 5 |
| 2 | 2 | 128 | 3 | 1 | 6 |

Fig. 9: Illustration of one level of spatiotemporal data refactoring of a variable of five time steps

the value of previously computed coefficients, the correction is computed in a workspace. In the state-of-the-art design \([15]\), the computed coefficients are first copied to the workspace before they are used for computing corrections, which prohibits out-of-place computing unless additional memory space is used. Our previous work leverages kernel fusion \([22]\) to merges the copy of the coefficients with the first mass-trans matrix multiplication, so that it enables us to use LPK out-of-place compute without a significant increase in memory footprint. However, one drawback with our previous design is the degraded memory access efficiency for GPK since accessing nodes in coarser grids leads to larger strided memory accesses. So, in this work, we propose to use an improved data layout to keep the stride always equal to one without bringing extra computation or memory footprint. As shown in figure 3 by separating nodes in the next coarser grid with coefficient, we can always keep nodes compacted. We build this reordering processing in the data store part of GPK, so that it does not bring any overhead.

3.4 Design of spatiotemporal data refactoring

As scientific data generated from simulations or experiments commonly exhibits correlation across time, exploiting the temporal dimension in addition to the spatial dimensions can be used to build a data hierarchical representation across both spatial and temporal dimensions and can potentially enable higher compression ratios when used for lossy compression. So, it is desirable to have an optimized design for spatiotemporal data refactoring for GPUs. Here we consider spatiotemporal data refactoring as \(N + 1\) dimensions of data refactoring, where \(N\) is the number of spatial dimensions and 1 is the temporal dimension. The theory of the multigrid-based data refactoring method \([7]\) can be generalized to refactor data in an arbitrary number of dimensions. However, it is not straightforward to enable efficient GPU data refactoring on data with an arbitrary number of dimensions.

3.4.1 Hierarchical batch optimization

We propose a novel design for efficient high dimensional GPU data refactoring: hierarchical batch optimization. Namely, our hierarchical batch optimization involves two levels of batch optimization: 1) locality batch optimization; and 2) dimensional batch optimization. Batch optimization exploiting data locality in data refactoring on GPUs was proposed in our previous work \([22]\), which is well adopted in GPK, LPK, and IPK. However, it is challenging to use locality batch optimization beyond three-dimensional data refactoring due to limited shared memory space on
3.5 Optimization for consumer-class GPUs

Although to common sense reducing the cost of arithmetic operations has less effect for improving memory-bound computations, we find that is not always true. This is due to the fact that not all GPUs have similar memory bandwidth and computational capacity ratios. Consumer class GPUs are commonly used by scientists especially in the edge systems where data refactoring is particularly useful. However, those GPUs typically offer decent memory bandwidth but limited computational power on high precision floating point data and certain operations such as division on double floating-point numbers, so memory-bound computations can be wrongly converted to compute bound including data refactoring. We find that the fused multiply-and-add (FMA) instructions are typically efficient with high throughput even on high precision data, so we re-implement core calculation in multigrid-based data refactoring in FMA instruction as shown in Table 3, in which \( \text{diag}(i) \) and \( \text{subdiag}(i) \) are the \( i \)th elements of the tridiagonal mass matrix. With this optimization, we convert more than 90% of the floating-point arithmetic operations involved in data refactoring to use FMA.

### Table 3: Core calculations implemented in more efficient FMA instructions

| Operations                      | Implementation in FMA instruction                                      |
|---------------------------------|------------------------------------------------------------------------|
| Linear Interpolation            | result = \text{fma}(r_1, v_{i+1}, -\text{fma}(r_i, v_i, v_i))           |
| Bilinear Interpolation          | \( t_1 = \text{Linear}(v_{i,j}, v_{i,j+1}, r_{i+1}^j) \)  
|                                 | \( t_2 = \text{Linear}(v_{i+1,j}, v_{i+1,j+1}, r_i^j) \)  
|                                 | result = fma(t_1, t_2, r_i^j)                                        |
| Trilinear Interpolation         | \( t_1 = \text{Bilinear}(v_{i,j,k}, v_{i,j+1,k}, v_{i+1,j,k}) \)  
|                                 | \( t_2 = \text{Bilinear}(v_{i+1,j,k}, v_{i+1,j+1,k}, v_{i+1,j+1,k}) \)  
|                                 | result = fma(t_1, t_2, r_i^j)                                        |
| Mass-Trans Matrix Multiplication| \( t_1 = \text{fma}(2, \text{fma}(v_{i,j}, v_{i,j+1} * h_{i+1}) \)  
|                                 | \( t_2 = \text{fma}(2, \text{fma}(v_{i+1,j}, v_{i+1,j} * h_{i+1}) \)  
|                                 | result = fma(t_1, t_2, \text{fma}(v_{i,j}, v_{i+1,j} * h_{i+1}) \)  
| Solv. Corr. Forward             | result = fma(v_{i-1}, diag(t), v_i)                                   |
| Solv. Corr. Backward            | result = fma(-h_{i+1}, v_{i-1}, v_i) * subdiag(t)                     |

3.6 Designing data refactoring for dense multi-GPU systems

As dense multi-GPU systems are commonly used in modern HPC systems, we extend the GPU data refactoring [22] to take advantage of multi-GPU systems. Dense multi-GPU systems refers to systems where multiple GPUs are equipped in each single computing node of supercomputers with fast interconnect such as NVLiks or PCIe. There are two ways of taking advantage of multi-GPU systems: 1) embarrassingly parallel: data are partitioned refactored independently; 2) cooperatively parallel: data are treated as a whole with multiple GPUs work on one refactoring process cooperatively. Comparing between the two, embarrassingly parallel approach potentially have better performance because it does not bring extra communication cost. The cooperative parallel approach leverages data correlation information between partitions, so it potentially can have deeper hierarchical levels for refactored data and higher compression ratios when used in lossy compression. Since the embarrassingly parallel is relatively straightforward, we mainly discuss the design of the cooperative parallel approach in this section. We discuss the cooperative parallel design for each data refactoring kernel separately.
3.6.1 Cooperative parallel grid processing kernel

GPK is used for calculating the multilinear interpolations at nodes in \( N_l \setminus N_{l-1} \) using nodal values in \( N_l \). Essentially, each interpolation at node in \( N_l \setminus N_{l-1} \) needs the nodal values of its neighboring nodes. So, in our cooperative parallel design of GPK, we add communications between GPUs to enable exchanging nodal values near the boundaries of each data partition for interpolation on nodes near boundaries. Since communication only involves nodes on the boundary, the communication cost is low i.e., \( O(n^2) \) for 3D data. Also, the interpolations on the nodes not close to the boundaries (core region) can be done without requiring exchanging nodal values, so we can overlap the interpolation on the core region with communications on the edge region.

3.6.2 Cooperative parallel linear processing kernel

LPK shares similar data dependencies with GPK, except it only needs to exchange boundary nodal values along dimensions it is currently processing. We can also apply similar computation-communication overlapping.

3.6.3 Cooperative parallel iterative processing kernel

Unlike GPK and LPK, strong data dependencies exist between different operations in IPK. In data refactoring IPK is used for solving the corrections. It requires a forward and backward pass along each dimension. So each partition needs to be processed in an orderly fashion. In this case, partitioning the data either row-block wise or column-block wise can lead to serious GPU underutilization. For example, as shown in figure 12(a), when using IPK on the second dimension, the work on the three GPUs needs to be done sequentially. To maximize GPU utilization, we propose to partition in a shifted round-robin fashion as shown in figure 12(b), so that all GPUs can be kept busy no matter which dimension IPK is processing.

4 Experimental Evaluation

We evaluate our work on two GPU-enabled platforms. Each node of the Summit supercomputer at ORNL is equipped with 6 NVIDIA Volta GV100 GPUs with 16 GB memory on each GPU and two 22-core (of which 21 cores/socket are accessible for computation) IBM POWER9 CPUs with 512 GB memory. Turing is a GPU-accelerated desktop with an NVIDIA RTX 2080 Ti GPU with 11 GB of memory and one 8-core Intel i7-9700K CPU with 32 GB of memory.

4.1 Evaluation methodology

We use datasets from a Gray-Scott reaction-diffusion simulation [23][24]. Each node in the input grid data is represented as single or double precision floating point values. Note that our data refactoring algorithms have deterministic computation time complexity regardless of the values in the chosen dataset, so it will yield the same performance for any dataset.

4.2 Evaluation on kernels

We first show the performance improvement we achieve from accelerating the three major operations in data refactoring on GPUs. Figure 13 shows speedups achieved on the three operations on the two GPU platforms with both single and double precision inputs. The input size is \( 513 \times 513 \times 513 \).
For single precision input, with the thread-level load-compute decoupled design, coefficient calculation with GPK outperforms the existing design by 4.9× and 6.9× on Summit and Turing GPUs, respectively. For mass-transfer matrix multiplication, with higher thread concurrency and data dependency free calculation, LFK achieves 6.3× and 4.1× speedups on Summit and Turing GPUs, respectively. For correction solver, LFK triples the performance on Summit and doubles the performance on Turing with the same level of thread concurrency as the state-of-the-art design, thanks to the more efficient memory access patterns. Also, leveraging our heuristic auto tuning capability, the optimum configurations can be selected automatically, yielding additional 1.2-4.9× speedups compared with choosing one configuration for all kernels and input sizes.

4.3 Evaluation on optimization for consumer-class GPUs on edge systems

As shown in Figure 13 comparing with the speedups on Volta GPU on Summit, we observe relative lower speedups for our Turing GPU, since the consumer-class GPU has limited computational power especially for high precision data. In this case, the computation can be wrongly converted to compute bound. Our FMA instruction optimization allows us to eliminate expensive operations, reducing warp latency and register usage, yielding additional 1.3-2.7× speedups on the three kernels.

4.4 Evaluation on overall data refactoring on a single GPU

Figure 16 shows the end-to-end data refactoring throughput achieved on a single GPU with different input sizes. (As decomposition and recomposition are symmetric process, they have identical performance.) To see how close the achieved data refactoring throughput is to the theoretical peak throughput, we estimate the theoretical peak by dividing the achievable single pass throughput with the accumulated number of passes on the entire input data over the data refactoring process. (The achievable single pass throughput is the maximum throughput achievable when data are read and stored on GPU memory once. We measured it through a specially designed benchmark kernel that simultaneously reads and writes the same amount of data from and to the GPU memory without computation.) The accumulated number of passes is calculated by summing the number of passes for all decomposition levels: \( \text{passes per level} \times \frac{1}{1 - \frac{1}{4}} \), where \( \text{passes per level} = 1(\text{coefficient calculation}) + 1(\text{copy to workspace}) + 5.25(\text{correction calculation}) + 0.125(\text{apply correction}) \). The theoretical peaks for Summit and Turing GPUs are 49.8 GB/s and 32.0 GB/s, respectively, for both single and double precision data. The state-of-the-art GPU data refactoring methods that we use as our baseline achieve only up to 10.4% of the theoretical peak throughput; our optimized GPU data refactoring achieves up to 92.2% of theoretical peak.

4.5 Evaluation on single-node multi-GPU performance

To show the potential of taking advantage of dense multi-GPU architecture using our cooperative parallel data refactoring on GPUs, we conduct an evaluation using 6 GPUs on one Summit node. We integrate our GPU data refactoring the MGARD compression workflow to demonstrate the benefit of using cooperative parallel data refactoring in terms of compression ratio. We use a 16 GB dataset from the Gary-Scott simulation as input with \( 1 \times 10^{-3} \) error bound. From the architecture level, the 6 GPUs are grouped into two GPU islands with 3 GPUs in each island interconnected using fast NVLink. Inter-island communication is achieved using X-Bus. In our evaluation, we logically group the 6 GPUs into \( K \) GPUs groups and do cooperative parallel data refactoring among the \( S \) GPUs within each group and keep embarrassingly parallel across GPU groups. We evaluate different combinations and note them as \( K \times S \). As shown in figure 13 in terms of performance, we can see \( 6 \times 1 \) offers the maximum throughput since all 6 GPUs are refactoring data in an embarrassingly parallel fashion. \( 3 \times 2 \) has slightly lower throughput compared with \( 6 \times 1 \) since every two GPUs need to communicate with each other. We see similar throughput between \( 3 \times 2 \) and \( 2 \times 3 \). When all 6 GPUs are participating in cooperative parallel (\( 1 \times 6 \)) we observe noticeable performance degradation due to the heavy communication across the X-Bus. In terms of compression ratios, as we increase the number of GPUs participating in cooperative parallel data refactoring, we observe improvement in compression ratios since compression can take more advantage of the data correlation between partitions.

4.6 Evaluation on optimization for spatiotemporal data refactoring

Next, we evaluate our optimization for refactoring spatiotemporal data on GPUs. For input, we use 16 input steps of Gray-Scott simulation data with 512 MB data per time step. We use one GPU for refactoring and integrate data refactoring the MGARD compression workflow. The compression error bound is set to \( 1 \times 10^{-3} \). We demonstrate the trade-off between compression throughput and ratio when batching different numbers of time steps of simulation data for compression each time. As we can see in figure 15 when we increase the number of time step per compression batch, we effectively improve the compression ratio. However, we also observe performance degradation as we increase the batch size. This is anticipated as exploiting the temporal dimension leads to extra data refactoring costs.

4.7 Evaluation on multi-node multi-GPU performance

To show the potential of GPU-accelerated data refactoring in large-scale scientific applications, we conduct a weak scaling test on Summit. We parallelize the workload by assigning each GPU or CPU core an equal-sized data partition and perform decomposition and recomposition. We assign each GPU device or CPU core to one MPI process and perform data refactoring on 1 GB of simulation.
data. For each computing node, we use the total available number of GPUs and CPU cores. We scale the number of nodes up to 1024 in our tests on Summit. For both SOTA-CPU and SOTA-GPU, we use embarrassingly parallel approach and we test both embarrassingly parallel and cooperative parallel approach for our work. Cooperative parallel is restricted within each computing node, since inter-node communication can bring high overhead. As shown in Figure 17, our optimized GPU data refactoring method achieves much greater throughput than state-of-the-art GPU and CPU designs. For example, we need only four computing nodes to achieve 1 TB/s refactoring throughput, whereas state-of-the-art GPU and CPU designs require 64 and 512 nodes, respectively. With 1024 nodes (i.e., 6144 Volta GPUs), we achieve up to 130 TB/s and 264 TB/s aggregated data refactoring throughput with cooperative parallel and embarrassingly parallel approach, respectively.

5 ShowCase

Data refactoring algorithms were designed to offer much greater flexibility when managing large scientific data than the traditional methods. With well-designed data management, data can be shared between scientific applications more intelligently with a large reduction in I/O costs. However, inefficient data refactoring routines can diminish the benefits brought by data refactoring itself. Here we use two examples to show the benefits of GPU-based data refactoring over the CPU designs.

5.1 Visualization workflow

First we show how our GPU optimizations can make data refactoring effective when used for I/O cost reduction in scientific workflows that rely on file-based data sharing. Figure 18 shows the cost of writing and reading a 4 TB simulation data file using 4096 and 512 processes using the state-of-the-art ADIOS I/O library [25] on Summit with GPU-accelerated data refactoring enabled. By writing or reading fewer coefficient classes, we can see immediate cost reduction in file write and read. When our efficient GPU-accelerated data refactoring is used, we can see this reduction in the cost of file write and read can be effectively translated into a reduction in the total I/O cost. Although multigrid-based data refactoring allows us to encode the most important information in the data with a few coefficient classes, it would not reduce the total I/O cost unless those coefficient classes can be efficiently computed or used for data recovery. For example, in our experiments we achieve \( \sim 95\% \) accuracy for a chosen feature in the visualization result (i.e., the total area of the iso-surfaces [26, 27]) with only three out of ten coefficient classes. This can be effectively translated into \( \sim 66\% \) I/O cost reduction.

5.2 Lossy compression

Multigrid-based hierarchical data refactoring can also be used as a preconditioner in scientific lossy compression software. As one of the key components in lossy compression workflows, it is important to have efficient data refactoring in order to make fast lossy compression possible. We showcase how our GPU-accelerated data refactoring can help improve the performance of lossy compression workflows in the MGARD lossy compression software. MGARD is a CPU-based lossy compressor with three components in its workflow: multigrid-based data refactoring, quantization, and entropy encoding. Figure 19 shows the time breakdown of the each component in MGARD [15] when data refactoring remains on the CPU (left bars) or is off-loaded to the GPU (right bars). In our test, besides the data refactoring process, we also off-load the quantization and de-quantization processes to the GPUs, since it can help reduce the GPU-CPU data transfer cost. The entropy encoding stage (ZLib lossless compression) is kept on the CPU. We can see that our GPU-accelerated data refactoring can greatly reduce the overall execution time of the lossy compression workflows.
6 RELATED WORK

Multigrid-based data refactoring shares some similarities with multigrid solvers, such as the use of multiple interlocking grids. But while multigrid solvers aim to accelerate the solving of linear systems, multigrid-based data refactoring aims to reconstruct scientific data progressively with hierarchical representations. This difference in focus leads to fundamental differences in both algorithms and optimization that prevent direct translation of GPU optimizations.

From an algorithmic perspective, although data refactoring and multigrid solvers have some operations in common, data refactoring composes these operations in a unique way. Further, the correction used in data refactoring is designed specifically for the orthogonal projection, while the correction in multigrid solvers is used to generate the fine grid solution. From a GPU optimization perspective: optimizations for data refactoring need to consider handling large-volume scientific data, which means we need to consider not only limited GPU memory but also cases where refactoring process might share resources with original scientific computations on GPUs. So, it is essential to optimize for low memory footprint as well as performance. Although part of the kernels used in data refactoring share similar computation patterns to those found in multigrid solvers, it is challenging to leverage existing work directly to achieve good parallelism and memory footprint balance in data refactoring. For example, state-of-the-art GPU refactoring [15] uses a parallelization technique proposed by Basu et al. [28], which only use coarse grain vector-wise parallelism, which can cause lower performance for data refactoring. Although fine-grain parallelism has been achieved in previous works [29][33], they generally brings high memory footprint and would require considerable efforts to apply their optimizations to different algorithms.

7 CONCLUSION

We have presented optimized data refactoring kernels that allow for use of GPUs to accelerate multigrid-based hierarchical refactoring for scientific data. We evaluated our designs on two platforms, including the leadership-class Summit supercomputer at ORNL, and showed that our GPU version can speed up data refactoring by up to 160× and 15× compared with state-of-the-art CPU and GPU designs, respectively, and can achieve 264 TB/s throughput using 1024 nodes on Summit. We also showcased our work using a large-scale scientific visualization workflow and the MGARD lossy compression technique. Together, these results demonstrate that scientists have another opportunity for dealing with their high data throughput requirements. Inline refactoring of scientific data can offer performance improvements and temporal fidelity that can benefit a number of science scenarios.

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