Energy Storage Systems Current Ripple Reduction for DC-Link Balancing Method in Hybrid CHB Topology

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Abstract—This paper focusses on a hybrid topology for a CHB, where some or all the modules are equipped with energy storage systems. In addition to the well-known capabilities of the CHB as a STATCOM, the hybrid topology has new advantages as a grid stabilizer. However, the current ripple on the energy storage systems has negative effects which tends to result in expensive solutions. To overcome this inconvenient, a previously known balance strategy is modified to prevent the ripple without compromising the DC-Link balance. This new control method is demonstrated through simulations.

Keywords— Capacitor Balance, Energy Storage Systems, Hybrid CHB, Multilevel Converters, Optimal Control, STATCOM.

I. INTRODUCTION

Multilevel Converters have meant a great revolution in high power applications thanks to their many advantages over well-known technologies such as the conventional 2-level Converter [1]. Due to industrial and economic reasons, the implementation of these Multilevel topologies has been slower than expected. However, Multilevel Converters have become a key element in the search for optimization and exploitation of renewable energy systems. This fact and the maturity of the technique acquired in the last decade have made multilevel converters a very attractive solution. Within Multilevel Converter topologies, Cascaded H-Bridge (CHB) is considered a great deal to provide high voltage levels and modularity. This topology is principally used in power distribution applications [2]-[7] and photovoltaic applications [8]-[11], among others [12]. In this converter, energy storage systems would also be applied as DC power supply of the modules [13]-[15], adding capability of energy management to the converter.

The paper is structured as follow: in section II, a 3-phase Y-connected CHB topology is briefly described, considering the integration of energy storage systems. The system control strategy is presented in section III. The simulation results are shown in section IV. Finally, in section V, the conclusion is outlined.

Fig. 1. Three phase Cascaded H-Bridge topology

II. CASCADED H-BRIDGE

As depicted in Fig. 1, this converter is composed by H-Bridge modules connected in series. Each module has an independent DC power supply that can be different for each module. This converter is presented to operate as Static Synchronous Compensator (STATCOM), providing reactive power on demand. CHB topology is widely used on STATCOM applications due to its modularity and other technical advantages when compared with 2-level topology:

- High power capability using mature medium-power semiconductor technology [1].
- Capability to operate under internal fault conditions thanks to the redundancy of the topology [16].
- High-quality output signals, improving its performance as the number of modules increases.
- No need to use step-up transformers.
- Lower losses in installation due to high voltage cabling and protections compared to former topologies.

A. Hybrid Topology

Another advantage of CHB topology is the ease to add energy storage systems (ESSs) simply by connecting them to the modules DC-Links, without transformers or additional converters. This topology, called Hybrid Cascaded H-Bridge (HCHB), is based on the combination of some modules with capacitors and some others with ESSs. The inclusion of ESSs adds the following possibilities to the topology:

- To contribute to grid stability providing active power and controlling grid frequency.
- To minimize THD, controlling the storage cell in order to eliminate harmonic distortion [17].
- To smooth active power fluctuations typical of renewable sources [14].

As an example, for better understanding, Fig. 2 shows one phase of a 7-level HCHB composed by 2 conventional capacitor modules along with an extra module equipped with an ultracapacitor as DC power supply.

![Fig. 2. HCHB branch based in ultracapacitor](image)

B. Drawbacks of HCHB and Control Motivation

Despite the numerous advantages of using ESS on CHB topology, there is some issues to take into account. The ESS must withstand some current ripple. Current ripple can cause temperature rise and lifetime reduction on ESS [18]-[19]. In addition, DC-Link voltage needs to remain balanced in the converter, so a balance method must be implemented to assure the balance between the converter branches.

In order to mitigate current ripple on ESS, different approaches have been made. In [20]-[21] this situation is faced adding a DC/DC converter as interface between the ESS and the H-Bridge cell. This solution isolates ESSs at the cost of making the system more expensive and bulkier. In [22], a low-pass filter has been proposed to eliminate the harmful harmonics. Just like in the previous approach, global system becomes more expensive, heavier and bulkier.

In this paper, a strategy proposed in [11] is adapted to manage a 3-phase Y-connected HCHB, as represented in Fig. 2. This new approach penalizes the instantaneous power deviation of ESSs modules, effectively reducing the current ripple on these devices.

III. APPROACH TO THE PROPOSED SOLUTION

The proposed control strategy is a variant from a previously presented method [11]. As in that method, a current control is assumed to provide some references $U_1^*, U_2^*$ and $U_3^*$ for the voltages which must be modulated on each phase. The modulation control must select the best output voltage $U_{kj}$ for each module to comply with the indicated line voltages while minimizing a potential value $F$.

In this case, the potential $F$ to be minimized is defined by adding the quadratic deviation of the DC-Link voltages and the time-integral of the power deviation to the original quadratic voltage deviation.

$$F = \sum_{k=1}^{3} \sum_{j=1}^{N} \frac{g_{vkj}}{2} (V_{kj} - V_{kj}^*)^2 + G_{pkj} \int |p_{kj} - p_{kj}^*| dt \ (1)$$

Where $V_{kj}$ and $V_{kj}^*$ are the real and desired DC-Link voltages, $p_{kj}$ and $p_{kj}^*$ are the real and desired instantaneous power that the module provides, $G_{vkj}$ and $G_{pkj}$ are nonnegative gain values for the tracking of DC-Link voltage and power of each module, $kj$ indicates the j-th module of the k-th phase and N is the number of modules. $G_{vkj}$ and $G_{pkj}$ can be tuned to ponder the relative importance of the voltage and power tracking of each module independently. Since instantaneous power tracking of non-ESS modules is not so important, as the current controller will ensure the total active and reactive power is correct, $G_{pkj}$ can be 0 for all non-ESS modules.

In order for a module to provide an average (active) power $\overline{P_{kj}}$, its output voltage $U_{kj}$ would have to be $U_{kj}^*$:

$$U_{kj}^* = \frac{3\overline{P_{kj}}}{\sqrt{i^2_a + i^2_q}} = \frac{3\overline{P_{kj}}}{\sqrt{i^2_a + i^2_q}} \ (2)$$

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where $i_k$ is the current of phase $k$ and $i_\alpha$ and $i_\beta$ are the current components according to the power-invariant $dq$ transformation. The power-invariant $dq$ transformation is valid as well. The power deviation term in (1) can then be written as:

$$G_{p_{kj}} \int [p_{kj} - p^*_{kj}] dt = G_{p_{kj}} \int \{i_k(U_{kj} - U'_{kj}) \} dt. \quad (3)$$

Since $U_{kj}$ is the output of the controller, the power term of $F$ penalizes deviation from the desired control action, while the voltage term penalizes the undesired impacts of such action on the DC-Link. Assuming $U'_{kj}$ is always reachable by the module, the output voltage $U_{kj}$ of each module can be decomposed as follows.

$$U_{kj} = U^*_kj + U_Akj + U_Bkj \quad (4)$$

$$U_Akj = \begin{cases} (U_{kj} - U^*_kj) & \text{if } U_{kj} > U^*_kj \\ 0 & \text{otherwise} \end{cases} \quad (5a)$$

$$U_Bkj = \begin{cases} (U_{kj} - U^*_kj) & \text{if } U_{kj} < U^*_kj \\ 0 & \text{otherwise} \end{cases} \quad (5b)$$

Since $U_{kj}$ must stay within the reachable limits of the module ($-V_{kj}$ and $V_{kj}$), $U_Akj$ and $U_Bkj$ are limited as follows.

$$-V_{kj} - U^*_kj \leq U_{kj} \leq U_Akj \leq V_{kj} - U^*_kj \quad (6)$$

Note that, among $U_Akj$ and $U_Bkj$, at least one must be 0 according to (5a) and (5b). Other than that, only the limits given by (6) need to be observed. Using this decomposition, the power term of $F$ can be written as:

$$G_{p_{kj}} \int [p_{kj} - p^*_kj] dt = G_{p_{kj}} \int \{i_k(U_{kj} - U^*_kj) \} dt. \quad (7)$$

In order to reduce $F$ as much as and as quickly as possible, its time-derivative is minimized. This is equivalent to maximizing an objective function $f$, where values not depending on the modules output $U_{kj}$ are considered a constant and neglected.

$$f = \frac{df}{dt} + cte \quad (8)$$

The time derivative of $F$ is linear with $U_Akj$ and $U_Bkj$ for all modules. Thus, the objective function $f$ can be written as:

$$f = \sum_{k=1}^{3} \sum_{j=1}^{N} B_{Akj}U_{Akj} + B_{Bkj}U_{Bkj} \quad (9)$$

where $B_{Akj}$ and $B_{Bkj}$ are the marginal benefits of respectively increasing $U_{Akj}$ and $U_{Bkj}$ by 1 volt. These benefit values are known in every control cycle:

$$B_{Akj} = G_{v_{kj}} \cdot \frac{\Delta v_{kj}}{c_{kj}v_{kj}} - G_{p_{kj}} \cdot \{i_k\} \quad (10a)$$

$$B_{Bkj} = G_{v_{kj}} \cdot \frac{i_k(v_{kj}-v^*_kj)}{c_{kj}v_{kj}} + G_{p_{kj}} \cdot \{i_k\} \quad (10b)$$

where $C_{kj}$ is the total capacitance of the DC-Link.

If phase voltage references need to be achieved, then the following equation would need to be observed:

$$\sum_{j=1}^{N} U_{kj} + U_{Akj} + U_{Bkj} = U^*_kj \quad (11)$$

To simplify, $\sum_{j=1}^{N} U^*_kj$ can be deducted from $U^*_kj$. The result is $U'kj$.

$$U'kj = U^*_kj - \sum_{j=1}^{N} U^*_kj \quad (12)$$

Since only line voltage references need to be achieved, the final linear optimization problem (LOP) has the same structure as in [11].

$$\max f = \max \sum_{k=1}^{3} \sum_{j=1}^{N} B_{Akj}U_{Akj} + B_{Bkj}U_{Bkj} \quad \text{subject to} \quad U_{Akj} + U_{Bkj} \leq U^*_kj$$

$$U_{Akj} + U_{Bkj} \in [0, V_{kj} - U^*_kj]$$

$$U_{kj} \in [-V_{kj} - U^*_kj, 0]$$

This LOP can be solved with the same method presented in [11]. The number of variables is greater and the formulas for the benefits are different, but the algorithm to solve the LOP remains the same.

It is worth noting that, since only one variable per phase can be non-saturated and $B_{Akj}$ is always lower than $B_{Bkj}$ one of the associated variables ($U_{Akj}$ and $U_{Bkj}$) is guaranteed to be null for each module, thus obeying (5a) and (5b).

It is also worth noting that for modules where $G_{p_{kj}}$ is 0 (such as the non-ESS modules), benefit values $B_{Akj}$ and $B_{Bkj}$ are equal. To reduce the number of variables, instead of $U_{Akj}$ and $U_{Bkj}, U_{kj}$ can be employed on those modules with the same benefit value. This is optional but recommended for speed.

One more recommendation for modules where $G_{p_{kj}}$ is 0 is to select $F_{kj}$ to be null so that $U'_{kj}$ will also be 0. This does not affect the method outcome but reduces the amount of operations.

IV. SIMULATION RESULTS

In order to validate the proposed method, some simulations have been developed. A 7-level HCHB converter has been connected to grid to act as STATCOM. HCHB converter is composed by 3 power cell (two capacitor cells plus an ultracapacitor cell) per phase, as shown in Fig. 1. Converter parameters are shown in Table 1.

In this scenario, capacitor voltages are independently controlled using a global energy controller, implemented by a PI regulator. Good behavior of the method to track voltage references was verified in [11]. Reactive power regulator has
been also implemented using another PI. The current control is done on the typical dq axes. To test the impact of $G_{P_kj}$ in ultracapacitor modules, a complete simulation has been carried out. During the simulation, $G_{P_kj}$ factor of ultracapacitor modules is changed at different times to check its effect on the power deviation and their current ripple. An active power demand is also made to check the ultracapacitors’ capacity to contribute to grid stability.

On the other hand, $G_{V_kj}$ is set to 1 on non-ultracapacitor modules, so that it can be used as a reference. On modules with ultracapacitors $G_{V_kj}$ must be low enough to allow them to exchange energy with the grid without affecting the other modules, but not too low so that their energy remains balanced among them. This value has been heuristically tuned to 0.001.

The total simulation time is 1.25s, with certain events occurring at $t=0.5s$, $t=0.75s$ and $t=1.00s$, and is divided in different parts. The upper graph in Fig. 3 shows the voltage ripple of the DC-Links connected to the first phase. The lower graph of the same figure plots the ultracapacitors current ripple as well as the current and RMS value during the simulation. This way it is possible to observe the impact of $G_{P_kj}$ on both, the capacitors voltage and the ultracapacitors current.

Initially, until $t=0.5s$, $G_{P_kj}$ of ultracapacitor modules is set to 0. All modules are controlled to 300V. STATCOM is controlled to provide 50kVAR but no active power is delivered to the grid. With this settings, ultracapacitor current ripple is 80.5 A (peak to peak) and RMS current ripple value on ultracapacitor is 24.64A.

From $t=0.5s$ to $t=0.75s$, $G_{P_kj}$ of ultracapacitor modules is set to 10. It can be observed current ripple is reduced significantly. Current ripple is 70A (peak to peak) and RMS current ripple value on ultracapacitor is 24.64A.

From $t=0.75s$ to $t=1.00s$, $G_{P_kj}$ of ultracapacitor modules is set to 1. It can be observed current ripple is reduced significantly. Current ripple is 70A (peak to peak) and RMS current ripple value is also reduced to 20A. This reduction, however, leads to an increase in the ripple of the capacitor voltage, from 16V (peak to peak) to 22V (peak to peak).

**Table 1. Model Parameters**

| Parameters                        | Values   |
|-----------------------------------|----------|
| Nominal grid phase-to-phase rms   | 1000V    |
| Voltage                           |          |
| Grid Frequency                    | 50Hz     |
| Modulation Frequency              | 5kHz     |
| Control Frequency                 | 10kHz    |
| Phase Inductance                  | 5mH      |
| DC-Link capacitors                | 2.2mF    |
| Ultracapacitor capacitance        | 6F       |
| Number of phases                  | 3        |
| Number of ultracapacitor modules  | 1 per phase |
| Number of capacitor modules       | 2 per phase |

**Fig. 3.** From top to bottom: DC capacitor voltages (green and red) and DC ultracapacitor voltage (blue) and ultracapacitor current ripple (green) and RMS ultracapacitor current ripple value (red).

**Fig. 4.** Grid currents. Phase a (blue), phase b (red) and phase c (yellow)
From $t=0.75s$ to $t=1s$, $G_{P_kj}$ of ultracapacitor modules is set to 200. A great decrease in the current ripple is appreciated. It drops from $34A_{pp}$ to $4A_{RMS}$. This decrease means a 58% of the ripple value and 84% of the RMS value of the current through the capacitor reduction compared to the initial situation until $t=0.5s$. However, the voltage ripple has increased its value to $40V_{pp}$ though. This ripple has to be taken into account due to the capacitor voltage limits.

At $t=1s$ $G_{P_kj}$ of ultracapacitor modules remain constant and there is a power demand of 10kW. This effect rises up current in the ultracapacitor.

According to Fig. 4, grid currents have not been disturbed by $G_{P_kj}$ changes. As mentioned in [11], the effect of this method on converter currents is theoretically null.

V. CONCLUSIONS

CHB converter with ESS connected on some modules can be used as grid stabilizer in STATCOM applications. Nevertheless, current ripple has negative effects on some ESS, like ultracapacitors. To solve this disadvantage, interface solutions have been proposed which make the system more expensive, heavier and bulkier. This paper presents a voltage regulation method which has been adapted to mitigate this problem. This method is based on an optimization problem, pondering the importance of voltage and power tracking. Each module has been individually treated using different gains for each one. Power deviation has been penalized in ultracapacitor modules in order to prevent current ripple. This modified strategy presents new advantages if compared with the original method.

First, it considers the possibility of a general approach and can be connected with different DC sources generators and ESSs covering some of nowadays needs, like grid stabilization or renewable integration into the grid.

Secondly, ESS damage can be minimized without using new converters or passive elements. New objective function has been proposed to solve that. Adjusting voltage and power deviation gain, current ripple on ultracapacitors can noticeably be decreased, thus preventing premature aging of these ESS. Although the voltage ripple on the regular modules is increased, adding extra capacitors to allow this extra voltage is always cheaper than adding ultracapacitors or batteries.

Finally, neither DC-Link nor phase current balance has been disturbed by the new strategy. In addition, independent voltage control of each module is still possible with the new strategy.

The flexibility of the original method is not compromised by the addition of the power term nor by the gains. On the contrary, the method can now be employed on more situations with additional objectives.

These advantages make this strategy interesting to be employed in many applications as STATCOMs or distributed PV where ESS integration can be implemented to add new advantages.

ACKNOWLEDGMENT

The authors gratefully acknowledge the financial support provided by Spanish Ministry of Education and Science and European Community Fund FEDER under the projects ENE2016-80025-R and RTC-2016-5488-3. This project has also received funding from the European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation program 771066. P. Gómez thanks MICINN for the award of a FPI pre-doctoral grant (BES-2017-079922) cofounded by the ESF.

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