Hybrid CMOS-CNFET based NP dynamic Carry Look Ahead Adder

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Jan 01, 2016

Abstract

Advanced electronic device technologies require a faster operation and smaller average power consumption, which are the most important parameters in very large scale integrated circuit design. The conventional Complementary Metal-Oxide Semiconductor (CMOS) technology is limited by the threshold voltage and subthreshold leakage problems in scaling of devices. This leads to failure in adapting it to sub-micron and nanotechnologies. The carbon nanotube (CNT) technology overcomes the threshold voltage and subthreshold leakage problems despite reduction in size. The CNT based technology develops the most promising devices among emerging technologies because it has most of the desired features. Carbon Nanotube Field Effect Transistors (CNFETs) are the novel devices that are expected to sustain the transistor scalability while increasing its performance. Recently, there have been tremendous advances in CNT technology for nanoelectronics applications. CNFETs avoid most of the fundamental limitations and offer several advantages compared to silicon-based technology. Though CNT evolves as a better option to overcome some of the bulk CMOS problems, the CNT itself still immersed with setbacks. The fabrication of carbon nanotube at very large digital circuits on a single substrate is difficult to achieve. Therefore, a hybrid NP dynamic Carry Look Ahead Adder (CLA) is designed using p-CNFET and n-MOS transistors. Here, the performance of CLA is evaluated in 8-bit, 16-bit, 32-bit and 64-bit stages with the following four different implementations: silicon MOSFET (Si-MOSFET) domino logic, Si-MOSFET NP dynamic CMOS, carbon nanotube MOSFET (CN-MOSFET) domino logic, and CN-MOSFET NP dynamic CMOS. Finally, a Hybrid CMOS-CNFET based 64-bit NP dynamic CLA is evaluated based on HSPICE simulation in 32nm technology, which effectively suppresses power dissipation without an increase in propagation delay.

Keywords: Hybrid CNT-CMOS technology, NP dynamic, Domino logic, Carry look ahead adder.

1 Introduction

Nowadays, Very Large Scale Integrated (VLSI) industry requires ultra high speed, low chip area, low power consuming, and portable processors. To fulfill the above requirements, there is a need to scale the devices and device interconnects. This leads to Moores law of scaling in integrated circuits. But, CMOS device scaling leads to leakage currents, short channel effects like velocity saturation and mobility degradation which are undesirable. These limits can be overcome to some extent by modifying the channel material in the traditional bulk MOSFET structure with a single CNT or an array of CNTs. For the past three decades the scaling of MOSFET has been the driving force towards the technological advancement. However, for VLSI systems, which depend on Silicon MOS technology, Industry Technology Road Map for Semiconductors (ITRS) has predicted that in nano regimes the expected high density integration will encounter substantial difficulties due to fundamental limitations in physics, material, and manufacturing obstacles [1].

There is a pressing need to explore circuit design ideas in new emerging technologies in deep-submicron regime, in order to exploit their full potential during the early stages of their development. According to the Stanford nano electronics lab[2], CNTs could launch a new generation of faster electronic devices that use less energy than those built using silicon-based transistors. Its electrical properties of greater mobility and high current carrying capability offer the potential for evolving towards the next generation of devices and circuits. Therefore, CNT would be a promising candidate for future nano-scale transistor devices.

2 Proposed circuit and logic technique

Dynamic logic circuits are used for high performance and high speed applications. Two different techniques exist in dynamic circuit implementation based on MOS technology. They are the Domino logic circuit technique and
NP dynamic CMOS circuit technique. These techniques are employed to satisfy the monotonicity requirement in dynamic circuits [3]. CLA’s are commonly used in modern processors. CLA improves speed by reducing the amount of time required to calculate carry bits. The CLA calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of larger value bits. CLA implementation with conventional MOSFET technology in both the techniques prefers domino logic circuit to NP dynamic logic. Comparatively, power wastage is less in conventional MOSFET domino logic circuit than NP dynamic CMOS circuit.

Our objective is to implement CLA up to 64-bit value by replacing the MOS technology with CNT technology in both domino logic and NP dynamic logic circuit techniques. Finally, a hybrid CMOS-CNT based NP dynamic 64-bit CLA is implemented and its performance in terms of MOSFET, CNFET and Hybrid CMOS-CNT technologies is analyzed.

3 Implementation of the proposed method

The proposed methodology is the hybrid CMOS-CNT based NP dynamic CLA implementation. The work is carried out in stages initiating with silicon based CLA. The input of CLA stages are considered as 8-bit, 16-bit, 32-bit and 64-bit. Similar steps are followed by replacing silicon with carbon nanotubes. A 64-bit CLA based on CNT technology is implemented with Stanford specifications. Both the domino and NP dynamic circuits are taken under study and results are observed. In CNT method, NP dynamic CLA functioning improves much than that of domino in terms of power dissipation and delay. Therefore, the NP dynamic logic CLA is considered and hybrid CMOS-CNT working on stages respectively is processed.

The CNT specifications are listed below:

- **Chirality**: CNFET utilizes a single carbon nano-tube or an array of carbon nano-tubes as the channel material instead of bulk silicon in the traditional MOSFET structure. It was first demonstrated in 1998. The structure of CNT described by an index with a pair of integers (n, m) that define its chiral vector.

\[
\theta = \tan^{-1}\left(\frac{\sqrt{3}n}{2m+n}\right),
\]

\[
d_t = \frac{L}{\pi} = \frac{a}{\pi} \sqrt{n^2 + nm + m^2},
\]

where \(\theta\) is chiral angle.

For \(n = m\); bonding is metallic. For \(n - m = 3I\); it has a small band gap. Whereas, for \(n - m \neq 3I\); it is semiconducting. The chiral angle is used to separate carbon nanotubes into three classes differentiated by their electronic properties as follows:

- armchair for \(n = m, & \theta = 30^\circ\),
- zig-zag for \(m = 0, n > 0, & \theta = 0^\circ\),
- chiral for \(0 < |m| < n, & 0 < \theta < 30^\circ\).

- **Channel length** (\(L_{ch}\)): The channel length is chosen to reduce the occurrence of scattering. In this paper, we have taken \(L_{ch} = 32\)nm.

- **Diameter** (D): The diameter of CNT is between 1.2nm and 1.8nm. In this range, the chirality vectors for zigzag tubes is (16, 0) (17, 0) (19, 0) (20, 0) (22, 0). In this paper, (17, 0) is chosen as the chirality vector. Diameter of the CNT is given by

\[
D = n\sqrt{3}a_{cc},
\]

where \(n\) denotes chirality vector, and \(a_{cc}\) is lattice constant which is 0.142nm for carbon. Diameter obtained using Eq.(2) was found to be 1.33nm.

- **Pitch**: It is defined as the minimum distance between two adjacent carbon nanotubes. It can be calculated by the formula

\[
\text{Pitch} = \frac{W_g - d}{N - 1},
\]

where \(W_g\) is the gate width, \(d\) is the diameter of the CNT, and \(N\) is the no. of parallel channels. For our simulation, we have chosen \(W_g = 32\)nm, \(d = 1.33\)nm, and \(N = 9\).

- **Oxide thickness** (\(t_{ox}\)): For channel length of 32nm, \(t_{ox}\) is prescribed to be 4nm.

- **Dielectric constant** (\(k_{ox}\)): The dielectric constant for carbon is between 12 and 16. As \(k\) increases, power consumption reduces. So, we have taken \(k_{ox} = 16\).

- **Length of doped CNT source-side** (\(L_{SS}\) and drain side (\(L_{DS}\)) extension: The length of source side as well as drain side extension are taken to same and equal to the channel length, which is 32nm.
In the Stanford CNFET model, physical channel length is set to be 32nm. The results reported in this paper were obtained using “HSPICE” 32nm technology[2,4-6]. In comparison to silicon based devices, CNFET provides better control over channel formation, better threshold voltage, better sub-threshold slope, high mobility, high current density, and transconductance.

Implementation of CLA circuit in NP dynamic and Domino logic techniques with increasing 8-bit, 16-bit, 32-bit and finally reaching to 64-bit operation is referred from our previous work [7], which is further more enhanced and corrections are made wherever necessary to carry on with the proposed design. The proposed design integrates carbon nanotube (CNT) fabrication with standard commercial CMOS very large scale integration on a single substrate suitable for emerging hybrid nanotechnology applications. This co-integration combines the inherent advantages of CMOS and CNTs. This hybrid design demonstrates the successful co-integration on a single chip utilizing both silicon n-channel MOSFET and p-type CNT transistors.

4 Results and Discussion

The observed CLA simulation results using hybrid CMOS-CNT are compared with MOS technology and CNT technology results. The comparisons are assessed in terms [10-12] of total voltage source power dissipation, average power consumption, delay, and power-delay product.

4.1 NP dynamic logic adder

The parameter values of 8-bit and 16-bit CLA implemented using NP dynamic logic is listed in the table[1]. In terms of total voltage source power dissipation and average power consumption CNFET based CLA gives better performance characteristics than MOSFET. Propagation delay and Power delay product calculations also signifies the CLA performance in CNFET technology.

| Parameter                        | 8-bit          | 16-bit         |
|----------------------------------|----------------|----------------|
| Total power dissipation (watts)  | 85.1609µ       | 33.728µ        |
| Average power consumption (watts)| 14.42E-05      | 2.615E-05      |
| Propagation Delay (s)            | 155.61p        | 328.74f        |
| Power delay product(J)           | 22.438E-15     | 3.471E-18      |

Table 1: Comparison between CN-MOSFET and SI-MOSFET CLA based on total power dissipation, average power consumption, propagation delay, power-delay product for 8-bit and 16-bit inputs.

The parameter values of 32-bit and 64-bit CLA implemented using NP dynamic logic is listed in the table[2]. In terms of total voltage source power dissipation and average power consumption CNFET based CLA gives.
better performance characteristics than MOSFET based CLA. Propagation delay, and power delay product calculations also signify the CLA performance in CNFET technology.

| Parameter                        | 32-bit          | 64-bit          |
|----------------------------------|-----------------|-----------------|
|                                 | Silicon         | Carbon          | Silicon         | Carbon          |
| Total power dissipation (watts)  | 323.358µ        | 76.8077n        | 957.513µ        | 164.1022n       |
| Average power consumption (watts)| 43.834E-05      | 11.923E-05      | 122.50E-05      | 15.573E-05      |
| Propagation Delay (s)            | 262.36p         | 680.36f         | 280.43p         | 852.07f         |
| Power delay product(J)           | 115E-15         | 81.1E-15        | 343.52E-15      | 132.69E-15      |

Table 2: Comparison between CN-MOSFET and SI-MOSFET CLA based on total power dissipation, average power consumption, propagation delay, power-delay product for 32-bit and 64-bit inputs.

4.2 Domino logic adder

The parameter values of 8-bit and 16-bit CLA implemented using Domino logic is listed in the table [3]. In terms of total voltage source power dissipation and average power consumption CNFET based CLA gives better performance characteristics than MOSFET based CLA. Propagation delay and Power delay product calculations also signifies the CLA performance in CNFET technology.

| Parameter                        | 8-bit           | 16-bit          |
|----------------------------------|-----------------|-----------------|
|                                 | Silicon         | Carbon          | Silicon         | Carbon          |
| Total power dissipation (watts)  | 85.3174µ        | 35.1642µ        | 212.7797µ       | 63.5934µ        |
| Average power consumption (watts)| 3.0448E-04      | 4.6374 E-05     | 3.6008E-04      | 5.8339E-05      |
| Propagation Delay (s)            | 96.388p7        | 201.578f        | 102.64p         | 339.27f         |
| Power delay product(J)           | 29.348E-15      | 9.347E-18       | 36.958E-15      | 19.792E-18      |

Table 3: Comparison between CN-MOSFET and SI-MOSFET CLA based on total power dissipation, average power consumption, propagation delay, power-delay product for 8-bit and 16-bit inputs.

The parameter values of 32-bit and 64-bit CLA implemented using NP dynamic logic is listed in the table [4]. In terms of total voltage source power dissipation and average power consumption CNFET based CLA gives better performance characteristics than MOSFET based CLA. Propagation delay and Power delay product calculations also signifies the CLA performance in CNFET technology.

| Parameter                        | 32-bit          | 64-bit          |
|----------------------------------|-----------------|-----------------|
|                                 | Silicon         | Carbon          | Silicon         | Carbon          |
| Total power dissipation (watts)  | 234.8754µ       | 79.3373n        | 301.5764µ       | 153.8624n       |
| Average power consumption (watts)| 4.4421E-04      | 1.2223E-04      | 5.8691E-04      | 1.9588E-04      |
| Propagation Delay (s)            | 174.63p         | 658.85f         | 223.85p         | 708.64f         |
| Power delay product(J)           | 77.572E-15      | 80.53E-18       | 131.37E-15      | 138.80E-18      |

Table 4: Comparison between CN-MOSFET and SI-MOSFET CLA based on total power dissipation, average power consumption, propagation delay, power-delay product for 32-bit and 64-bit inputs.
4.3 NP dynamic logic adder: Revisited

The comparison of NP dynamic logic CLA and Domino logic CLA in terms of total power dissipation, average power, delay and power-delay product is given in above tables 1,2,3, and 4, respectively. These results observed in stages of 8-bit, 16-bit, 32-bit and 64-bit signifies the performance improvement in NP dynamic CLA than Domino CLA, when CNFET technology is used. Therefore further work is done by considering the NP dynamic logic CLA.

| Parameter                        | 8-bit        | 16-bit       |
|----------------------------------|--------------|--------------|
|                                  | Silicon      | Carbon       | Hybrid       | Silicon      | Carbon       | Hybrid       |
| Total power dissipation (watts)  | 85.1609 µ    | 33.728n      | 31.162n      | 132.9407 µ   | 61.7694n     | 59.986n      |
| Average power consumption (watts)| 14.42E-05    | 2.615E-05    | 2.147E-05    | 28.147E-05   | 5.605E-05    | 4.263E-05    |
| Propagation Delay (s)            | 155.61p      | 132.74f      | 4.062p       | 195.02p      | 385.05f      | 4.944p       |
| Power delay product (J)          | 22.43E-15    | 3.471E-18    | 8.721E-18    | 54.89E-15    | 21.81E-18    | 210.8E-18    |

Table 5: Comparison among Si-, Carbon-, and Hybrid-MOSFET based on total power dissipation, average power consumption, propagation delay, power-delay product for 8-bit and 16-bit inputs.

The parameter values of 8-bit, 16-bit, 32-bit and 64-bit CLA implemented using NP dynamic logic is listed in the table[5,6]. In terms of total voltage source power dissipation and average power consumption CNFET based CLA and Hybrid CMOS-CNT based CLA gives equally compatible performance characteristics. But in case of propagation delay CNFET based CLA offers less delay, which gains a low power delay product value than Hybrid CMOS-CNT. In comparison with MOSFET technology, implementation of CLA in CNT and Hybrid CMOS-CNT offer better performance.

| Parameter                        | 32-bit       | 64-bit       |
|----------------------------------|--------------|--------------|
|                                  | Silicon      | Carbon       | Hybrid       | Silicon      | Carbon       | Hybrid       |
| Total power dissipation (watts)  | 323.3528µ    | 76.8077n     | 77.843n      | 957.513µ     | 164.1022n    | 163.504n     |
| Average power consumption (watts)| 43.834E-05   | 11.923E-05   | 10.459E-05   | 122.50E-05   | 15.573E-05   | 14.855E-05   |
| Propagation Delay (s)            | 262.36p      | 680.36f      | 14.337p      | 280.43p      | 852.07f      | 20.137p      |
| Power delay product (J)          | 115E-15      | 81.1E-18     | 1.49E-15     | 343.52E-15   | 132.69E-18   | 2.99E-15     |

Table 6: Comparison among Si-, Carbon-, and Hybrid-MOSFET based on total power dissipation, average power consumption, propagation delay, power-delay product for 32-bit and 64-bit inputs.

5 Summary and Conclusion

The performance optimization of 64-bit CLA based on CNFET technology signifies the advantage of NP dynamic logic technique in terms of power and delay. Despite the promising progress of CNFETs, the high fabrication cost of CNFETs and fabrication of p-type CNT and n-type CNT on a single chip might cause issues regarding imperfection and variability [8][9]. The challenge facing the Stanford team was that CNTs are predominately p-type semiconductors and there was no easy way to dope these carbon filaments to add n-type characteristics[2].

For cost-effective and reliable utilization of CNFETs, and the time-gap reduction in migrating from silicon MOSFET to CNFET technology, the CNFET technology has been required to be combined with low-cost and reliable CMOS technology[13-16]. The CMOS technology is better in switching speed, especially for n-MOS. In this work, the high mobility transport in p-type CNFETs is exploited and combined with high-performance conventional n-type MOSFETs, thereby achieving the best overall performance in a hybrid configuration. Therefore, implementing a hybrid device using CMOS and CNT technology is the best approach to the advancement of nanotechnology field.
6 References

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