Single Memristor Logic Gates: From NOT to a Full Adder

Ella Gale
International Center for Unconventional Computing,
Bristol Robotics Laboratory
Bristol, UK BS16 1QY
Current address: Department of Chemistry,
University of Bath, Claverton Down, Bath, UK, BA2 7AY
Email: E.Gale@bath.ac.uk

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Abstract
Memristors have been suggested as a novel route to neuromorphic computing based on the similarity between them and neurons (specifically synapses and ion pumps). The d.c. action of the memristor is a current spike which imparts a short-term memory to the device. Here it is demonstrated that this short-term memory works exactly like habituation (e.g. in *Aplysia*). We elucidate the physical rules, based on energy conservation, governing the interaction of these current spikes: summation, ‘bounce-back’, directionality and ‘diminishing returns’. Using these rules, we introduce 4 different logical systems to implement sequential logic in the memristor and demonstrate how sequential logic works by instantiating a NOT gate, an AND gate, an XOR gate and a Full Adder with a single memristor. The Full Adder makes use of the memristor’s short-term memory to add together three binary values and outputs the sum, the carry digit and even the order they were input in. A memristor full adder also outputs the arithmetical sum of bits, allowing for a logically (but not physically) reversible system. Essentially, we can replace an input/output port with an extra time-step, allowing a single memristor to do a hither-to unexpectedly large amount of computation. This makes up for the memristor’s slow operation speed and may relate to how neurons do a similarly-large computation with such slow operations speeds. We propose that using spiking logic, either in gates or as neuron-analogues, with plastic rewritable connections between them, would allow the building of a neuromorphic computer.

1 Introduction
What is a memristor? It is a resistor with memory. It is neuron-like. And it is more than theoretical, it is physical device acting in the physical world, which means that it is non-conservative with respects to energy. I shall introduce the subject and explain the contents of this paper working from these three simple statements.
A resistor with memory  Chua introduced the memristor concept in 1971 [1] as a device which related its internal state to the time-integral of current or voltage. The concept has been expanded and refined [2–4] and there is still some debate about what definition should be used to describe the memristor (see this recent review [5]) although little of that concerns us here.

In the memristor, a.c. measurements give rise to a distinctive pinched hysteresis loop (taken to be one of the fingerprints of the device [6]), where the memory is encoded in the hysteresis: reading off a current at a specific voltage we see two different currents because one has been taken up to the maximum voltage and back down again and the other has not. The memristor memory is usually stored in ions, for example in the best-known version of the device [7], it is stored in oxygen vacancies, this is also the case in our devices [8–9]. Putting a voltage across the device causes the movement of ions which changes the resistance, leading to an altered current (there is far more detail available than this, see [5,10,11]).

My work has involved looking at the ‘d.c.’ properties of the memristor: how it reacts to a steady non-varying voltage or a series of pulses. It was found that when a voltage is applied in this way there is a resultant current spike which has been seen is our [12,13] and other’s [14–16] devices.

Memory allows the association of events which happen (and have happened) at different points in time. In this paper, I will present how this allows the device to store data temporarily and allow input bits to interact through time see sections ?? . This idea is essentially the opposite of parallelisation, when building parallel circuitry we are essentially replacing the time (as in time for a computation) with space (extra processors). Here we are replacing space (components on a circuit board) with time (increased number of steps) using the memory to store the computation through time. The gates made using this motivates the question of what is the circuit and logical complexity of such a mode of operation; essentially what is our conversion rate between space and time? We need to know the trade-offs to allow us to get the maximum efficiency for a circuit. For example, we are reaching the limits of how far we can continue shrinking computers in accordance with Moore’s law [17]. To overcome this, the International Technology Roadmap for Semiconductors suggested the approach of ‘More-than-Moore’ where the components are capable of performing more functions [18]. To plan a circuit with these components we would need to precisely compare and contrast this extra functionality.

Neuron-like  Memristors have been compared to both neurons [3,19,20] and synapses [21,22], and as such, have been enthusiastically received by the neuromorphic computing community. The first experimental memristor paper [7] suggested that because memristors combined processing and memory in the same component, they were similar to neurons and could be the basis of a brain-like computer. This same group later presented the ‘neuristor’ [23] – a combination of memristors and capacitors that presented repetitive brain-like dynamics.

Brain dynamics are known to be chaotic and it has been suggested that neurons are poised at the edge of chaos [20], so the search for chaos using memristors (a search also inspired by the similarity of the memristor’s operation to the Chua diode in Chua’s circuit [24,25] – the simplest chaotic circuit) is
relevant to us here. From simulations, it has been shown that a Chua circuit can be built including a memristor [26–30]. Experimentally, chaos-like dynamics have been observed in memristor circuits [31] and chaos has been demonstrated as arising from a single memristor [32].

One of Chua’s early papers [3] suggested that memristors were present in the Hodgkin Huxley model [33], a statement he later developed [19, 20, 34]. The ion pumps in neural cell membranes were modelled as time-varying resistors, the existence of which suggested that biological brains should have huge impedances (and resulting power draw) which we know they do not have. By replacing the time-varying resistor with time-invariant memristors running off the time-varying ion concentration, the model no longer requires unnatural impedences [34].

Of interest to us is another property of neurons: habituation. Habituation [35] is the learned ability to ignore unnecessary stimuli, such as an author not attending to the surrounding background noises of a coffee shop when writing (incidentally, as this learning is unconscious, it takes a great deal of mental training to turn it off, although long-time meditators have been shown to be able to do this [36]). One of the first and most famous habituation experiments involved the ‘sea snail’ (confusingly also known as ‘sea hare’) or Aplysia. This invertebrate has a sensitive feeding tube which it doesn’t want to get damaged and so will withdraw if the tube is stimulated (like a child will stop sticking its tongue out if you threaten to grab it). In an experiment the feeding tube was lightly brushed with a delicate paintbrush (a harmless intervention), and, over time, the Aplysia learned not to attend to this stimulus and not to withdraw its tongue. Aplysia is a simple creature with only 20,000 neurons, and the neural pathways for this response has been mapped out (and requires only 4 neurons). The response at the sensory neuron does not diminish, but with training the corresponding motor response signals (recorded at motor neuron L7) decrease in size and this is the physiological cause of habituation.

Chua demonstrated theoretically that an ideal memristor stimulated by repeated voltage spikes would alter its memristive state and present a decreasing current response spike (see figure 7 in [34]) and this result strengthened previous theoretical work demonstrating that the neural protein pumps in the Hodgkin-Huxley model for the neuron [33] was best described theoretically as a memristor [19, 20]. We shall replicate this theoretical result with a real memristor in section 3.1.1.

The advantages of using spike interactions are many-fold. The memristor switching itself can be slow [9] but the spikes can interact much faster, the output of which is ‘held’ in the short-term memory of the memristor, which gives rise to, if not faster processing, more complex operations within a given time-frame than is usually the case in standard electronics.

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1The Hodgkin-Huxley model describes an electrical circuit equivalent for a neuron membrane. A neuron, like all cells, consists of a cell membrane that separates the inside of the cell from the outside. The cell membrane contains proteins called ‘protein pumps’ that pump ions out of the neuron doing work against a chemical gradient. When the neuron fires, the ions flood back in, giving a quick change in charge that leads the voltage spike that transmits the electrical signal. In the Hodgkin-Huxley model the cell membrane is well described as a capacitor and the protein pumps were described as time-varying resistors and the power provided by respiration was represented as a battery. All the components of the model could be bought in a hardware store, but the time-varying resistors, used to model protein pumps, did not really have a hardware analogue.
A real device  The first experimental memristor paper \cite{7} was published in 2008 and concerned a titanium dioxide memristor and made the link to Chua’s theoretical device. However the field of ReRAM which pre-dated this discovery by around 20 years offered many other chemistries that did the same thing and expanded our understanding of the memristor’s operation via their materials science models (the interested reader is referred to the following reviews: \cite{5,11}).

Unconventional computing \cite{37,38} (also sometimes called natural computation \cite{39}) investigates the computation of non-traditional systems, such as biological computers (like Slime mould \cite{40}), bio-inspired computers (like C.A.) \cite{41}, chemical computing (like the B-Z reaction) \cite{41}, reservoir computing, quantum computing, billiard-ball computing (conservative computation).

Knowledge of unconventional computing inspires us to consider the computer as a physical system which is instantiated in the real world. If we look at memristors this way, we start to consider the way it uses energy and obeys the laws of physics, such as the conservation of energy. And thus when designing logic gates for these systems we need to consider the physical reality of the device, rather than just an abstraction. This will be covered in section \ref{section:physicalreality}.

1.1 Logic

To design a circuit, we need to consider circuit complexity. In this paper, we use the Arabic numerals \{1,2,3\} as a set of counting numbers capable of standard arithmetical operations and we use the following set of symbols \{⃝,\} for logical values 0 and 1 in binary.

1.2 Circuit Complexity

To decide how to design a circuit board, we need to be able to compare logically equivalent methods of performing an arbitrary logical function. There have been a few approaches to determining how ‘complex’ a circuit is. Circuit size complexity of a Boolean function is the minimal size of a circuit that can compute that function (in the abstract mathematical sense, how many logic gates required, in the concrete electronic engineering sense we would take into account the size of those components). Circuit depth complexity of a Boolean function is the minimal depth of a circuit, i.e. the maximum length of a path from input to output gate for the physical devices. Another approach is the graph of nodes where each node is a logic gate. Karnaugh maps \cite{42,43} are often used as a method of finding the best approach to build a logical system or express a logical function.

1.3 Synchronous and asynchronous logic

In this section the word ‘logic’ refers not to the operations of $|$ or $\lor$ but the methods of combining them. Currently, most logical operations are done in a synchronous manner, the bits are operated on at the same time and a clock pulse is required to keep the information in time (a delay will lead to incorrect values). Asynchronous logic is older in this type of logic the clock pulse in unnecessary.

We also need to briefly cover reversible and irreversible computation. Most computation is irreversible, for example all 2-bit logic gates lose a bit of infor-
mation and it is this fact that suggested to Shannon that information could be accounted for as an energy and introduced the concept of entropy to computing \[44\]. For example if we do a 2-bit OR operation we have no way of telling if a \( | \) output is the result of a \( \{ 0, 1 \} \), \( \{ 1, 0 \} \) or \( \{ 1, 1 \} \) input. If we can do this, the computation is said to be reversible. Physically reversible computation is extremely rare (examples), logically reversible merely requires that we can reconstruct the inputs from the outputs.

1.4 How logic gates have been instantiated with memristors

This is not the first paper on how to make logic gates with memristors. Strukov et al \[45\] used implication logic to design logic gates which required two memristors (IMP-FALSE \( \{ \rightarrow, \bot \} \)) logic is Turing complete, but somewhat unfamiliar to computer scientists). The most notable Boolean logic gates were simulated by Pershin and di Ventra \[?\] and required a memcapacitor, three or four memristive systems and a resistor. Before the gate was sent the two bits of data, a set of initialization pulses were required to be sent to put the gate into the correct state to give the correct answer. This system, however, is not true Boolean logic because these initialization pulses were different dependent on what the logic to follow would be. Thus the gate can not be considered to be operating only on the two bits of input data and is not a simple Boolean logic gate (it is a Turing machine doing a computation on several bits of data (Boolean input pulses and initialization pulses) which is capable of modelling a Boolean logic gate). Note also that this scheme was tested with memristor emulators, not real devices. There have been other more complex designs for memristor based Boolean logic gates, the simplest of which requires 11 circuit elements \[?\] (and one of the authors, Pino, has several patented memristor logic gates as well). In this paper, we will demonstrate how to perform Boolean logic with a single memristor.

Interesting work involving designing memristor logic gates by Lehtonen and Laiho. In \[46\] they work with implication logic using a memristor reset as the false operation, they also suggest that 3 memristors are sufficient to compute any 2-bit in, 1-bit out Boolean function and state that: \( 2^2 \rightarrow 2^n \) need \( n+2 \) working memristors, for example a full adder would require 10 memristors under this scheme as it is \( 2^3 \). In \[47\] they suggest using parallelism to avoid the sequential nature of memristors, and choose NeIMP as the best version of Implication logic for memristor cross-bars.

This paper starts with the habituation results in section 3.1.1 as an example of memristors natively mimicking neural circuits. I then describe the short-term memory of the memristor in section 3.3, then describe possible methods of performing logic using it in section 3.4. From there, we are in a position to elucidate the rules for spiking memristor logic 3.4.2 and demonstrate them with some examples (section 3.5), simple logic gates like OR (section 3.6), complex logic gates like XOR (section 3.7), before finally describing how to make a logically-reversible full adder in section 3.8.
2 Experimental Methodology

Memristors were fabricated as in [9] using the TiO$_2$ sol-gel as described in [8] and were measured using a Keithley electrometer, with a set time-step of 0.1s, which gives an actual output of 0.16s (time-steps are padded by a settling time to ensure accuracy). After each logical test, the memristor was left for 40 time-steps (∼40s) to lose its short-term memory, i.e. reset to the null state. All presented results plots are experimental data.

Electronic device modelling of a biological habituation learning experiment was performed as follows: 40 0.1V spikes of 0.084s duration were applied 0.084 seconds apart (i.e. it was continuous for 3.35s) which is longer than the duration of the short-term memory of the memristor [48] to give a baseline non-learning response. Then the device was zeroed for the same amount of time. Then 6 spikes of +0.1V of 0.084s (1 timestep) were applied 1.168 (2 times steps) seconds apart and the current response of the device were recorded at each step (to give the response to the spike on the first step, and the ‘bounceback’ response on the second when the device was zeroed). This approach was repeated with a negative voltage input of -0.01V.

3 Results

3.1 Properties of the memristor

We shall explain how the memristor works by demonstrating habituation, before elucidating memristor design rules and using them to design circuits.

3.1.1 Recreation of biological experiment using a memristor

A famous study of an amnesiac patient H.M. who, as a result of ill-advised brain surgery, had his medial temporal lobe removed to treat his epilepsy. As a result he was not able to convert short term memories into long-term memories (a mental deficiency made famous by the film Memento), however, he was able to learn and improve at certain tasks without ever being aware that he had learnt it, this is the type of ‘automatic’ skills learnt through practice, like martial arts or driving a car [49,50]. This type of memory is called non-declarative memory and includes ‘how-to’ types of memory, and elementary reflexive (as in it becomes a reflex) learning such as habituation, sensitisation (ability to attend to dangerous stimuli) and classical (association of two stimuli) and operant (association of a subject’s actions and a stimuli) conditioning (trained ingrained responses), all of which is stored in the unconscious mind.

Figure 1d demonstrates the same response in our memristors, part 1(a) compares the positive current non-habituation response, the line, with the habituation response, the blue bars, to the voltage input in part 1(c). We see a clear decrease in the level of the current response with increasing numbers of stimuli demonstrating electronic habituation with a single memristor. Unlike [34] this response is itself a non-linear decrease which follows the same shape as the decay curves in [12,48]. This is (to our knowledge) the first time habituation has been demonstrated in such a manner in a single memristor circuit (although these results were hinted at in [51] which is very interesting as this is a different type of memrisor and suggests that this is a general property of the devices rather
than being specific to a material). Unlike neurons, this habituation learning is plastic and only persists as long as the short-term memory of the memristor, allowing for plastic habituation and learning in memristor networks (again, see Erokhin’s et al work’s for interesting work involving the plastic (rewriteable) and permanent learning in memristor networks [52]). Our devices also express the state of their memory when the device is returned to zero voltage (bounce-back, see section 3.4.2 for a description) and this is shown in figure 11(b) where the line shows the response of the device to switching to zero after the memory has been lost (non-habituation) and the red bars show the response to zeroing after continued stimuli (habituation), the first bar is the response to the first zero, i.e. after the device has been fully zeroed, and this small value serves as a control for the effect. We see that the negative ‘bounceback’ response (fig 1.b) shows a similar learning effect which is smaller than the positive effect, unlike the positive spike response this effect moves towards the non-habituation response rather than away from it.

3.2 Experimental Schemes for computing with Memristors

The result presented in section 3.1.1 demonstrate that the memristor is capable of subtraction and we can use this effect to design logic gates.

If, as suggested by Hilbert, ‘Mathematics is a game played according to simple rules with meaningless marks on paper’, then we can describe computer logic as a game played with the laws of physics in the natural world. We are free to choose arbitrary properties of the physical world to represent our logic (the ‘meaningless marks’ of the computation game); however, whatever we choose must make sense within the device and how it actually acts (one of the reasons why electronic engineers are so keen on figures of merit that accurately describe what a device will do, rather than theoretical models that tend to be easier to describe and reason about but are not completely accurate). Figure 2 shows the schematic for this process, from experiments and what we know of physical reality we can expect the forward flow of time (which causes directionality, see section 3.4.2) and energy conservation to arise from the material properties of the memristor. Directionality suggests the use of a sequential logic approach. By choosing which material property is associated with our computation.

3.3 Short Term Memory

When there is a change in voltage, $\Delta V$, across a memristor the device exhibits a current spike, the physical cause of which is discussed at length in [13]. This spike is highly reproducible and repeatable and is related to the size of the voltage change ($\Delta V$) [13]. The spike’s size (as measured by the first measurement after the Keithley’s changed voltage) is highly reproducible, the current then relaxes to a stable long-term value (this value is predictable and reproducible), and it takes approximately 2-3 seconds to get to this value.

This slow relaxation is thought to be the d.c. response of the memristor [3].

\[^{2}\text{by which I mean the experimentally testable world of the laboratory}\]

\[^{3}\text{Note that there has been some discussion as to whether the memristors have a d.c. response [Chua's keynote], within which is has been generally agreed that the perfect memristor may not, but non-ideal memristors (which all real devices are) may. This is not a settled issue}\]
Figure 1: Experimental Replication of the Apalsia experiment: (a) bars: current response to positive spikes applied sequentially; line current response to positive spikes applied after the short-term evaporates; (b) bars: negative ‘bounceback’ response to zeroing voltage, note the first bar is the response to zero after zeroing; (c) The applied voltage input: 0.1V spikes. N.B. error bars not shown as the electrometer can measure to fA and µV.
and if a second voltage change happens within this time frame, its resulting current spike is different to that expected from the $\Delta V$ alone. The size and direction of this current spike depends on the direction of $\Delta V$, the magnitude of $\Delta V$ and the short-term memory of the memristor.

As an example, consider a memristor pulsed with a positive 1V voltage square wave as in figure 4 (where the pulses are repeated to demonstrate the repeatability) with a timestep of $\approx 0.02s$. The current response is shown in figure 3 and we can see there is a positive current spike associated with the $+\Delta V$ and a perhaps less obvious negative current spike associated with the $-\Delta V$ transition from $+1V \rightarrow 0V$. At approximately 20s, we shortened the square wave to a single time step, and the memory of the system has caused the response spike (responding to the $-\Delta V$ to be smaller (and as it is smaller, it suggests that there is some physical property of the device which has not adjusted to its $+V$ value. See [?] for an discussion on why this physical property is predicted to be the oxygen vacancies in the $\text{TiO}_2$.) Thus the response is subtractive in current and additive in resistance state.

To try and understand the subtleties of this apparent ‘addition’, consider the following system: two voltages, $V_A$ and $V_B$ are sent to the memristor, one after the other separated by one time-step (i.e. before the memristor has equilibrated), where $V_B > V_A$ and $V_B = 0.12V$, and figure 5 shows the size of the two resulting spikes as a function of increasing $V_A$. We look at two situations:

1. $V_A(t) \rightarrow V_B(t + 1)$;
2. $V_B(t) \rightarrow V_A(t + 1)$.

These two situations are drastically different if we look at the transitions, $\Delta V$, as situation 2 has a negative $\Delta V_{B\rightarrow A}$, all the other transitions are positive see table 3.3. Situation 1 shows that if the smaller voltage is sent first ($V_A \rightarrow V_B$), the current of the first transition $\Delta i_{0\rightarrow A}$ increases with the size of $V_A$, and the second transition $\Delta i_{A\rightarrow B}$ decreases with the size of $\Delta V_A$, due to the decrease in the effective $\Delta V_{A\rightarrow B}$. However, the sum of these two effects is non-linear, and generated much discussion at a recent conference (CASFEST 2014).
Figure 3: The effect of adding spikes close in time. The response spikes are the negative current spikes. When a positive spike it included but not allowed to relax the corresponding negative spike is smaller.

Figure 4: The input voltage for figure 3
so that the total current transferred (approximated as the sum of the spikes here, but actually the area under the two current transients) is not the same as that shown for situation 2 (until $V_B = V_A$). This shows that more current is being transferred and demonstrates that the spikes are dependent on $\Delta V$. Furthermore, it makes it clear that $\Delta i_{0\to A} + \Delta i_{A\to B} \neq \Delta i_{0\to B} + \Delta i_{B\to A}$, (except in the trivial case where $V_B = V_A$) and that spike based ‘addition’ is non-commutative and therefore the order in which the spikes are sent is relevant to the output of the calculation.

3.4 Methods of Performing Logical Operations

3.4.1 Sequential Logic

We shall make use of sequential logic (as first implemented in [53]), which works with the spike interactions seen in the memristor. Memristor sequential logic allows the computation through time by storing a state and allowing it to interact with the input; thus a one terminal device can do two-input (or higher) logical operations, if we are willing to wait for the output.
3.4.2 Elucidated Rules

Essentially, memristors operate a sequence-sensitive ‘subtractive summation’: where inputs add additional energy to the system, but where that additional energy is subject to subtraction due to energy loss and the whole process operates under nonlinear dynamics. The rules required to design a memristor logic gate follow.

Directionality The memristor naturally implements IMP. The memristor is directional: e.g. The response at \( t_1 \), for \( A \rightarrow B \) does not equal the output \( \left( t_1 \right) \) for \( B \rightarrow A \). The cause of this is that the memristor responds to the difference in voltage. This naturally allows memristor-based sequential logic to compute implication logic as Implication, IMP or \( \rightarrow \), requires that \( 0 \rightarrow 1 \neq 1 \rightarrow 0 \) and thus the order in which the two values are input has a meaning. Naturally, sequential logic, as it separates the values in time, implements this ordering.

3.4.3 ‘Summation’ via Energy Conservation

If the logical \( | \) is taken as being a high voltage, i.e. \( M \) instead of \( m \), then more energy is imparted to the system from the logical combination \( || \) compared to \( [0, 0] \). This approach can allow the creation of memristor based time-limited summators of use in leaky integrate and fire neurons.
3.4.4 ‘Bounceback’

The application of a voltage spike produces a resultant current spike in the direction of the difference between the starting voltage and the ending voltage, e.g. the first voltage change $V_0 \rightarrow V_A$ causes a positive current response, $+i_A$, if $V_A$ is positive, and negative, $-i_A$, if $V_A$ is negative. If the system is then returned to zero, there is a smaller current spike of the opposite polarity, i.e. $-i_0$ and $+i_0$ respectively for the two examples mentioned above. If several spikes are input before returning to zero, i.e. a sequence of $[V_0, V_A, V_A, V_0]$ the current spike, $i_0$, is larger than would be the case for $[V_0, V_A, V_0]$, although not twice as large due to losses in the system (as the system is nonconservative).

3.4.5 ‘Diminishing Returns’

As discussed in the example of $[V_0, V_A, V_A, V_A]$ above each addition of each consecutive spike has a reduced effect compared with the first. This property is seen with spikes of the same polarity and with changing polarity i.e. the response spike to $[V_0, +V_A, -V_A, +V_A, -V_A]$ is smaller than $[V_0, +V_A, -V_A]$. This only happens to spikes input into the memristor’s short-term memory as waiting for the device to return to a blank state refreshes the property that reacts to the voltage step. We expect that the physical property in question is related to the ions in the device, as it they that ‘hold’ the memory, but this has not been experimentally verified. The diminishing returns effect is behind the habituation shown in section 3.1.1.

3.5 Examples of Logical Systems

Knowledge of these rules and effects allows us to design logical computation systems which perform a surprising amount of computation with only a single memristor. We have found that, in these schemes that the summation effect is important in magnitude logic, the ‘bounceback’ effect is more relevant in polarity logic (although both affect the outcome). As these can be balanced and set in opposition to each other, the richest effects came from using the mixed logics (as presented in 2) we will now present a few examples.

There are two variables we can utilise when assigning logical values: the magnitude, as represented by $M$ for a high magnitude and $m$ for a low magnitude; and the sign, as represented by a + for positive and − for negative. The 4 different logical assignations that can be applied using these values is shown in table 2. To implement logical operations, voltage spikes are applied for one time-step and the response recorded at the same frequency. In between logical operations, the devices were left for longer than the equilibration time ($\tau_{\infty}$ in 13) which is around 3.5s) to zero the memristor by removing its short term memory.

Changing the values of $M$ and $m$ can allow the results to be tuned or balanced against the effect of polarity, but in this paper we shall just deal with qualitative examples. From investigation of these systems, we have elucidated the following physical rules for the system.
Table 2: Four different methods of implementing logical $|$ and $\bigcirc$ with memristor spikes: $M$ refers to a high magnitude voltage, $m$ to a low magnitude voltage and ‘+’ and ‘−’ refer to its polarity.

| Logical value | Magnitude Logic | Polarity Logic | Mixed Logic 1 | Mixed Logic 2 |
|---------------|-----------------|----------------|---------------|---------------|
| One           | M               | +              | +M            | -M            |
| Zero          | m               | −              | -m            | +m            |

Figure 7: AND Gate Implementation

3.6 Simple Logic Gates

We can do Boolean logic with the spike interactions by sending the second bit of information one time-step (0.02s) after the first. We take the input as the current spikes from the voltage level. The output is the response current as measured after the $2^{nd}$ bit of information, at that timestep, i.e. $V_B$. After a logic operation the device is zeroed by being taken to 0V for approximately 4s, and this removes the memristor’s memory.

We have some freedom in how we assign the $|$ and $\bigcirc$ states to device properties and these give different logic. The following examples will demonstrate some approaches and build an OR gate or an XOR gate: i.e. $|$ is any positive current output, $\bigcirc$ is any negative current output, inputs are positive (+1) and negative (−1) voltages.

3.6.1 Inverter

Using polarity logic and the ‘bounce-back’ effect, it is an easy thing to build an inverter as shown in figure 7. Because the response spike is in the opposite direction, taking that as the result of the operation switches from $|$ to $\bigcirc$ (and vice versa) and can be viewed as performing the NOT operation on the input.
3.6.2 AND Gate

An example of an AND gate is shown in column 5 in figure ??, this example uses mixed logic 2 (see table 3) with a M of -0.5V and a m of +0.001V. If we take the response output as | if current over a threshold (in this case, 0.55µA) is seen, the device implements an AND gate (this is still the case if we choose to limit ourselves to only the value of the t₁ response spike). Due to the summation effect, the amount of energy in the |, | system is larger than the [0, |], [|, 0] and [0, 0] parts of the truth-table, and this causes a larger ‘bounceback’ response which can be measured in the positive current response.

Were we to limit ourselves to the negative current part of the device response, the magnitude of the output picks out an inclusive OR operation, in that the only parts of the truth table that have a response over the threshold are those that contain a | (because these spikes depend on a | input). Although this response is trivial, it is information that can be usefully used with the correct output circuitry.

3.6.3 OR Gate

The truth table for an OR gate is given in column 8 in table 3, essentially, the output should be | if either of the inputs contained a |. We take the 0 output as being below a threshold current and the | output as being above a threshold. The threshold is set to >18nA with the 0 input being set of 0.01V and the | as 0.2V which gives the voltages below:

- 0, 0 = 0.01V, 0.01V
- 0, | = 0.01V, 0.2V
- |, 0 = 0.2V, 0.01V
- |, | = 0.2V, 0.2V.

Figure 8 shows the current data from the voltage inputs above. It can be seen that when a | is input, there is a large spike output. To read the logical state of the device, one merely takes the current value as the second bit is read in.

3.7 Complex Logic Gates

The XOR truth table is shown in column 9 in table 3. If we take logical | to be the current resulting from a positive voltage and a logical 0 to be the current resulting from a negative voltage, then, the response is the current when the 2nd bit is input (not after, although it could be designed that way but it is slower). We get a high absolute value of current if and only if the two inputs are of different signs, i.e. we have {0, 1} or {1, 0} which gives us an exclusive OR operation. For this logical system, we used the same voltage level and allowed a change in sign to indicate logical zero or logical one:

- 0, 0 = -0.1V, -0.1V

4Using 0 as 0V was also tested, it works and is lower power but was not chosen as an example as it is a trivial case.
Figure 8: OR Gate. Using $|$ equal to a current spike caused by a voltage change to 0.2V and $\circ$ equal to a current spike caused by a voltage change to 0.01V we can make a serial OR gate (where logical 1 is considered to be a current which is more than 5nA). At 0.04s ‘0, 0’ was input, giving peaks below the threshold i.e. $\circ$ as an output. The three large peaks are $|$ outputs resulting from ‘0,1’; ‘1,0’ and ‘1,1’ inputs.
- $\triangledown, \triangledown = -0.1V, +0.1V$
- $\triangledown, \bigcirc = +0.1V, -0.1V$
- $|, | = +0.1V, +0.1V$.

As an example, the input voltage is shown in figure 10 and the current output is shown in figure 9. This is based largely on ‘bounceback’, a $|$ or $\bigcirc$ input to a memristor ‘holding’ the opposite polarity in memory causes a bigger change. Essentially we measure the convolution of the ‘state’ and ‘input’, represented as a function $F[S,A]$ i.e. $F[\bigcirc, |] \approx F[|, \bigcirc] > F[|, |] \approx F[\bigcirc, \bigcirc]$.

Figure 9: XOR gate, the modulus of a current response over $\pm 1.25 \times 10^{-8}$A is taken as one, as current response under that threshold is taken as zero.

With a pause between operations to allow the memristor to lose its memory, the XOR operation is reproducible, as shown in figure 11. Note, as our devices are slightly asymmetric, $F[\bigcirc, |]$ does not exactly equal $F[|, \bigcirc]$ and $F[\bigcirc, \bigcirc]$ does not exactly equal $F[|, |]$. This arises from the material and the method of synthesis (see [9]) and has nothing to do with the voltage being positive per se, the devices are always wired up the same way round before measurement. Larger voltage ranges (see figure 11) highlight the difference between positive and negative, demonstrating how different logical combinations can be split out or alternatively balanced by sensitive voltage choice.

As XOR $A = \text{NOT } A$, if we always take the 2nd point after the first (and only bit in this case) as being the response bit (as we did above for the XOR gate), we have a NOT gate.

### 3.8 Full-Adder

It is possible to compute an unconventional instantiation of full-adder, as shown in figure 12 (admitting that we require a voltage spike to current spike conversion). The two input and carry bits are input as a series of spikes using mixed
Figure 10: The input voltage for the XOR gate.

Figure 11: Reproducibility test of XOR function. Here the XOR truth table is run 7 times (using a different set of voltage input values). The threshold between $|$ and $\bigcirc$ is marked as shown.
logic 2 with input | represented by -0.5V and input ○ represented by +0.001V. The input sequence is [A,B,C,1,2,3,4], with the logic input at $t_A - t_C$, the response spike recorded at $t_1$, an extra read voltage of -0.15V input at $t_2$. This gate requires a clock to operate. Figure 12 shows the response of the memristor to this scheme, for the three inputs of a full adder, the read spike at $t_2$ is marked with an * to make it easier to understand, and the data of the memristor losing its short-term memory is not shown.

From this set-up the following things can be deduced from knowing the maximum positive and negative current spikes within 4 time-steps of an input (although this requirement need not be too stringent if we have a way of recording the maximum current within the ranges in between zeroing the system, which we can do with knowledge of the read pulse clock).

The resulting information from the current is thus:

1. if a negative current is recorded in the range -17.5 to -20nA: we have had a | input into the system
2. if a negative current is recorded in the range -5 to -17.5nA: we have a carry bit from the operation
3. if a negative current is recorded in the range 0 to -5nA: we have had a zero in the system (this is redundant information)
4. if the maximum positive current is recorded in the range 0 to +5nA: the result of the calculation is ○
5. if the maximum positive current is recorded in the range +5 to +9nA: the result of the calculation is |
6. if the maximum positive current is recorded in the range +9 to +12.3: the result is ‘2’ (or | for the carry bit, ○ for the summation bit)
7. if the maximum positive current is recorded over 12.5nA: the result is ‘3’ (or | for both the carry and summation bit in binary logic).

The output in the negative is purely a result of the input voltages to the system. The positive system includes the ‘bounceback’, and the summation effect as probed by the read voltage which gives thresholded values of the memristor’s state.

With switches, it would be possible to send on the logical result as binary. Region two of the plot encodes the carry bit for the operation, because only if there are two $-M$ spikes (which encode |) within 3 time-steps of each other we will see a current response in that range. The summation bit is not encoded in as direct a manner, the maximum of the positive currents encodes the numerical sum, and so the summation bit for the value 3 is in a different place to that for the value 1. If we only require knowledge of the carry and summation bit, we can do without the read voltage and corresponding spikes. Changing the values of $M$ and $m$ can tune the effect and might allow us to change the relative values of the output spikes.
Figure 12: A full adder using mixed logic 2. The first three input bits are the logical inputs, the system has one timestep to respond (1s) before a read spike is sent in, as marked by an *. The numbers of the ranges correspond to the list.

Table 3: Selected 2-bit binary Boolean functions and their corresponding gate names (as used in this work). *Function number from [54].

3.9 Logical Complexity of a Full Adder

A half adder is a 2-bit output basic gate, it is equivalent to an XOR and an AND gate.

Now we are in a position to analyse our full adder from the point of view of logical efficiency. The 2-bit full adder separates 8 3-bit inputs into 4 arithmetical groups. Arbitrarily large numbers can be added by chaining full adders as the carry bit out to the carry bit (C) in. Using the same description as before, as standard full adder has $N = 8 \times 2^3$ possible inputs, and 4 distinguishable operations, giving us a logical efficiency of 50%. Our spiking logic full adder allows the differentiation of all 8 operations, and gives us a logical efficiency of 100%. Using standard circuit complexity measures of circuit depth complexity and circuit size complexity we get 1 + selection circuitry for our full adder and $[x]$ for a standard transistor based full adder. This is not a fair comparison, of course, because a standard full adder has multiple ports and all bits are received at the same time, in our full adder we have to take 2 timesteps to get the answer.
Table 4: Full adder truth table

|   |   |   |   |   |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 2 |
| 2 | 0 | 0 | 0 | 2 |
| 3 | 0 | 0 | 0 | 3 |

As an aside, this measure of logical efficiency means that the full adder is less logically efficient than a half adder. A half adder requires 2 input bits and 2 output bits ($B^2 \rightarrow B^2$) and can separate out 4 inputs into 3 groups, giving a logical efficiency f 75%. The full adder has to add an entire extra bit to count up to 3 and separate out 8 inputs into 4 groups. Of course, a single logic gate doing a full adder’s truth table is better (as it involves 3 bits of input not $2^3=8$) and of course he full adder is more useful. However the half adder is 75% efficient on 4 inputs, allowing it to separate out 3 different inputs, the full adder is 50% efficient on 8 inputs which allow it to separate out 4 groups of inputs.

Relatively simply, we can immediately write that for each input port removed from the gate, an extra input time-step must be added. Thus, we can replace circuit connections with extra time steps. Thus we arrive at an answer to the ‘conversion rate’ between space and time where we count space by the number of input wires and time by the time-step (in a spiking clocked system). It seems to be 1:1. In standard electronics a full adder involves 3 input wires (one time-step), in the memristor system, we use 1 input wire and 3 time-steps. Output in standard electronics is 2 output wires, in the memristor system we can either use 1 time output plus.

4 Conclusions

In this paper I have shown: the use of asynchronous logic based on spikes, elucidated the rules governing spike interaction, invented logical assignations for these physical processes, used them to design gates and demonstrated a full adder that possesses extra functionality that leads to it being a logically-reversible gate. This was all done with a single memristor plus the additional circuitry to convert current output spikes to voltage inputs (but we have no reason to expect that this will be bigger than the current state of the art).

These results motivate the question of how far can we take this approach. I have no reason to believe that a 2-bit full adder is the limit of the functionality of a memristor (although I posit that we can’t take it too much further with our devices without reaching a detection limit). In fact, using the memristor as a synapse, integrator or habituator could be considered more complex than a 2-bit full adder.

This paper also suggested a measure of efficiency to compare (computation) time and (circuit) space complexity, and this measure was used to compare the spiking memristor full adder with a standard full adder and put a number to
that improvement.

Nonetheless, this method of full adder creation has possible drawbacks in that one has to wait longer for the solution to a posed question. This is less relevant than might seem for some uses. The brain is much slower than conventional electronics. Furthermore there is the idea that Moore’s law is coming to an end, and the current request from [18] is the concept of ‘More-than-Moore’, where a device has extra functionality ‘riding on top of’ standard shrinkable hardware.

This work shows that by using the memristor’s extra functionality of possessing a memory, we can do a seemingly amazing amount of computation. There are some drawbacks, of course. Our memristors are slow and most memristors operation on neural-spike-like speeds, which are far slower than modern day circuits. To use these logic gates, we need to convert current spikes back into voltage spikes, the circuits to do this are relatively trivial (op-amp, or a 2:1 stage), but will take up circuit board area, so the size reduction isn’t quite as good as calculated here. For this reason, it makes sense to do the maximum amount of processing on the memristor. It seems that the amount of processing is limited by the length of the short-term memory of the memristor (which we suspect is related to the material properties, so can be tuned by materials scientists and chemists) and our instrumentation: the speed and accuracy of input and the accuracy of determining output.

The use of memristor summation approaches in the full adder scheme is similar to how neurons work. For example three inputs received one after the other causes the largest response spike and the only positive $t_2$ spike, either of these outputs could be linked to a thresholded switch which could release a current or voltage spike and thus act like a leaky integrate and fire neuron. The diminishing returns effect could enforce a refractory period. As neurons work by converting a rate-coded spiking voltage to a current spike at the synapse and then to a voltage spike, all of which can be considered transmission of a logical $|$, the memristor with its action whereby input and output are current and voltage, could be ideally suited to neuromorphic computing.

Spiking logic is more brain-like. The brain is a very complex and not very well understood biological machine, but it is known that it operates slower than modern electronics and via spikes (neural spikes are voltage spikes caused by an influx in current rather than current spikes caused by a change in voltage, but the dynamics are very similar). The fact that memristors implement spiking logic naturally supports Chua’s thesis that sodium and potassium ion gate proteins in the neural membranes are memristors and the habituation experimental data in section 3.1.1 provides further evidence.

4.1 Future Work

This work suggests the following design for a memristor computer. A base level of memristors performing operations utilising the time-complexity as outlined here (i.e. interaction of several bits through time). The level above this could use space complexity whereby extra information is stored in how the memristor computing units are wired together. Add in some plasticity within and between the layers to allow learning and development of the system and we have a good model for a neuromorphic computer. This can be also be read as model of the brain, and it is my hope that neuroscientists investigate this point of view to
see if it is useful to them. If the model fits, it would provide further evidence that Chua is correct in his ideas that memristors are related to neural circuits.

I strongly suspect that the Universal Memristor Machine [7], if built with spiking memristor logic, would be a step change in neuromorphic computing, as this approach would combine the extra functionality due to the memory in processing and also circuit layout. Bottom layer: Memristor circuitry operating via memory and utilizing time complexity. Top layer: space complexity, things wired together around it between the two: plasticity to allow for rewiring things on the fly. This is basically a description of the brain. And perhaps, adding in the trinary ideal gates would make it even more efficient and powerful.

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