Silicon nanocrystal memories by LPCVD of amorphous silicon, followed by solid phase crystallization and thermal oxidation

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Abstract. Silicon nanocrystals memory cells of an n-MOSFET type were fabricated and tested, based on a silicon nanocrystal gate MOS structure fabricated by low-pressure chemical vapor deposition (LPCVD) of amorphous silicon (α-Si) on a tunneling silicon dioxide layer, followed by solid phase crystallization and high temperature thermal oxidation. A layer of silicon nanocrystals embedded in SiO2 at a tunneling distance (3.5nm) from the silicon substrate was thus formed. The obtained memory cells showed a full-write, full-erase memory window of the order of 0.5V under charging with pulses of 7V and -8V respectively at 100 ms.

1. Introduction
In silicon nanocrystals memories a layer of silicon nanocrystals embedded in the gate dielectric of a MOSFET structure is used as the charge trapping medium [1]. The silicon nanocrystals layer is situated at a tunneling distance from the silicon substrate and carrier injection from the substrate (electrons or holes) is used to charge the nanocrystals. The 2-D layer of nanocrystals constitutes, thus, a distributed charge storage medium, with important advantages compared to the continuous polycrystalline silicon layer used in conventional floating gate flash memories, namely better possibility of scaling down device dimensions, better isolation and faster write-erase times [2-4]. In this work the fabrication process for the gate dielectric with the embedded Si nanocrystals consists in growing a thermal tunneling SiO2 film (3.5 nm thick), on top of which an amorphous Si layer is deposited by low-pressure chemical vapor deposition (LPCVD). The thickness of this layer is adjusted so as to get, after oxidation and annealing, the desired nanocrystal layer thickness and control oxide thickness. This process shows the advantage of controllable nanocrystal size and a good quality of thermal oxide [5-7]. In a previous paper [7] we investigated the charging properties of the nanocrystals. In this work we present results on the characteristics of the corresponding memory cells.

2. Experimental
The fabrication process of the memory cell uses 0.6 μm technological rules, and is similar to that of a conventional LOCOS-isolated nMOS device, except for the additional steps that are required for the formation of the Si-ncs. After the growth of 3.5 nm thermal oxide, a 9 nm thick LPCVD α-Si layer is deposited. A recrystallization step at 900 °C for 5 min is then performed, followed by 20 min oxidation.
and 30 min high temperature annealing steps at the same temperature. Polysilicon is then deposited and patterned in order to form the gate electrode. The Si-ncs layer outside the active area of the device is also etched-off. Source and drain regions are formed through ion implantation and annealing at 900 °C for 20 min in N₂ ambient. A schematic layout of the structure of the memory cell is shown in Figure 1. In this study aluminum gated p-type MOS test capacitors were also fabricated in the same process and used as test structures.

![Figure 1. Schematic layout of the Si-ncs NMOSFET memory cell.](image)

Figure 2a shows a cross-sectional transmission electron microscopy image of a sample fabricated as above, in which the deposited α-Si, 9 nm thick, has been oxidized for 20 min at 900 °C. A three-layer structure is obtained with the Si-ncs confined between the tunnel and the control oxides. The plan-view image of the same sample shown in Figure 2b reveals the existence of extended Si islands, which are composed of smaller Si-ncs, with sizes ranging from few to 35 nm. Oxidation of the structure for 25 min reduces the thickness of the Si-ncs layer approximately to 2 nm, while the extended Si islands are reduced accordingly to 15 nm [7].

![Figure 2 (a). High-resolution cross-section of TEM micrograph of a sample oxidized for 20 min at 900 °C. (b) Dark-field plan view image from the same sample.](image)

### 3. Results and discussion

Figure 3a shows the obtained flat band voltage shift (ΔVFB) as a function of the applied gate pulse with the pulse width as parameter, of a capacitor structure fabricated as above, with an oxidation time of 25 min and annealing at 1000 °C for 1 h. These results were obtained by applying positive/negative gate pulses and then registering the corresponding C-V characteristics at 1 MHz without discharging the structure between applied pulses, while Figure 3b shows the ΔVFB as a function of the pulse width. In this case discharging was performed between the applied pulses. Both graphs indicate that electrons and holes can be injected and trapped within the Si-ncs, resulting in considerable shifts of the C-V characteristics. Also, the magnitude of the obtainable shifts is highly dependent on the pulse width especially in the case of holes. Finally, clear saturation of ΔVFB at large negative or positive gate voltages occurs and the obtained memory window-determined from the maximum ΔVFB in both directions-is asymmetric, indicating that electron transfer to the Si-ncs is more efficient than that of hole. Figure 4 shows the retention characteristics after the application of 7V (electron injection) or -
12V (hole injection) single pulse at 100 ms. The relaxation of the structures was monitored under zero applied external field. The electrons discharge relatively fast, at a rate of 210 mV/decade, while holes discharge at a slower rate of 90 mV/decade. Figure 5 shows the endurance characteristics obtained after cycling the structure between 7 V for 100 ms (write-electron injection to the Si-ncs) and -10 V for 100 ms (erase- electron ejection from the Si-ncs). The cycling was interrupted at specific times and C-V measurements were recorded. The structure tolerated approximately 10^5 cycles, which is considered satisfactory for the used duty cycle.

Figure 3. (a) Flat-band voltage shift as a function of pulse height with the pulse width as parameter for a capacitor structure oxidized at 900 °C for 25 min and annealed at 1000 °C for 1 hour (sequential charging mode). (b) Dependence of the flat-band voltage shift upon pulse width for pulses of 7 and -10V (single pulse charging).

Figure 4. Retention characteristics under no read-disturb conditions

Figure 5. Endurance characteristics after cyclic stressing of the capacitor with 7V at 100ms and -10V at 100ms.

Figure 6. Transfer characteristics for a +8V/-7V 100ms Write/Erase regime.

Figure 7. Write/Erase characteristics from full Erase/Write memory state conditions.
The transfer characteristics of the memory cell are shown in Figure 6. Application of +8V/-7V write/erase pulses of 100 ms width leads to a memory window of about 0.5V. Although both electrons and holes can be injected and trapped within the nanocrystals the above write/erase regime of operation utilizes transfer of electrons in and out of the trapping nodes. The subthreshold slope is below 90mV/decade indicating that the interface traps have a minor influence on the device transfer characteristics. Memory operation in the 100 ms regime has been evaluated as a function of the write/erase pulse amplitude starting from full erase/write conditions. These two different initial charging conditions correspond to no electron charge within the nanocrystals and to maximum electron storage condition). As depicted in Figure 7, stable erase and write states can be achieved at voltages as low as –6 V and +7V respectively.

4. Conclusions
Si-ncs memory devices have been fabricated using a process of LPCVD deposition of α-Si and subsequent crystallization-oxidation. Memory effect due to injection and trapping of both electrons and holes was clearly demonstrated. Using only electron injection-ejection stable write and erase states were obtained. On the other hand, endurance and especially retention characteristics have to be optimized by suitable tuning of the Si-ncs fabrication process.

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6. References
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