Impact of gate leakage considerations in tunnel field effect transistor design

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Received April 1, 2014; accepted April 13, 2014; published online June 5, 2014

In this paper, we have presented the impact of the gate leakage through thin gate dielectrics (SiO2 and high-κ gate dielectric) on the subthreshold characteristics of the tunnel field effect transistors (TFET) for a low operating voltage of 0.5 V. Using calibrated two-dimensional simulations it is shown that even for such a low operating voltage, the gate leakage substantially degrades several subthreshold parameters of the TFET such as the off-state current, minimum subthreshold swing and average subthreshold swing. While the drain-offset as well as the short-gate are effective methods for reducing the gate leakage, we show that if the gate tunneling leakage is not considered, even for these two methods, the overall TFET off-state current will be significantly underestimated. Our results demonstrate the need to carefully account for the gate leakage in the design of TFETs just as it is done for the conventional nanoscale MOSFETs. © 2014 The Japan Society of Applied Physics

1. Introduction

Devices operated in subthreshold or near-threshold region,1,2 are being aggressively explored for reducing both the operating and the stand-by power consumption. Subthreshold design also enables realization of self-powered applications dependent solely on energy scavenging techniques. Tunnel field effect transistors (TFET) are attractive candidates for subthreshold or near-threshold design due to their steep sub-threshold characteristics.3–14 Leakage currents play a crucial role in this region of operation. Hence, subthreshold and near-threshold circuit design requires much more accurate modelling of leakage currents, particularly in the subthreshold region.

Gate leakage is known to be an important contributor of the off-state leakage in the conventional thin SiO2 gate based MOSFETs.15,16 For the fully depleted silicon-on-insulator (FD-SOI) structures, the ITRS (2012) update predicts an equivalent oxide thickness (EOT) of 0.8 nm going into production for high performance logic in 2014 and for low standby power applications in 2017.17 Such extremely small EOT will require us to look at gate leakage afield even for the MOSFETs. Even in a TFET, the gate leakage could be the most important contributor of off-state leakage. Neglecting the gate leakage results in a very small subthreshold slope and gives surprisingly low Ioff and subthreshold slope values which have not been achieved experimentally.18,19 High-κ dielectrics with larger dielectric thickness or gate stacks have been used in the TFET to reduce the gate leakage.20,21 However, even with the high-κ dielectrics, the fabricated Si TFET devices have not achieved the theoretically predicted subthreshold swing values. Most of the theoretical work on TFET neglects gate leakage. The purpose of this paper is to show that how erroneous it is to assume that there is no gate leakage in TFET. Further, a careful study quantifying the effect of gate leakage on TFET characteristics has also not been undertaken.

In this paper, we have studied the impact of gate leakage on the subthreshold characteristics of TFET with an effective gate dielectric thickness as low as 0.8 nm. For a quantitative validity of our results, we have calibrated both the TFET tunnelling current and gate leakage current with the previous published results. The results in this work show that the gate leakage can substantially alter the subthreshold character-istics of the TFET with both SiO2 and high-κ gate dielectric. We have further studied the effect of gate drain alignment on the TFET off-state current and the gate leakage. TFETs with a drain-offset have been fabricated experimentally for reducing the off-state current.22 Such a structure also reduces the parasitic capacitances.23,24 Another similar method that can be employed for reducing the gate leakage is the short-gate structure.25 In this work, we show that even for these two methods, the overall TFET off-state current will be underestimated if the gate tunneling leakage is not considered. The details of the device structure and simulation parameters are listed in Sect. 2. Mechanism of the gate leakage and calibration of results are discussed in Sects. 3 and 4, respectively. Effect of the gate leakage on device characteristics is presented in Sect. 5. Finally, Sect. 6 draws important conclusions of this study.

2. Device structure and simulation parameters

Figure 1 shows the structures of the simulated double gate TFET including the drain-offset and the short-gate structures. Both SiO2 [Fig. 1(a)] as well as high-κ HfO2/SiO2 gate stack [Figs. 1(b)–1(d)] were used as the gate dielectric. To include the effect of fringing field in the simulations, gate electrodes of finite thickness, surrounded by the oxide were used. The device parameters are listed in Table I and are based on previous work on TFET.20 The drain bias (VDS) and the gate metal work function (ΦM) were chosen as 0.5 V and 4.3 eV, unless otherwise stated. Simulations were carried out using a two-dimensional (2D) device simulator.26 Non-local model for band to band tunnelling (BTBT) was used in the simulations to take into account spatial profile of the energy bands, as well as, spatial separation of the electrons generated in the conduction band from the holes generated in the valence band. Due to the high doping in the source and the drain regions, the effect of band gap narrowing was also included. Fermi Dirac carrier statistics and concentration dependent Shockley–Read–Hall model were used to accurately simulate the device performance. BTBT Tunneling was considered both at the source–channel junction (region of the gate–source overlap) as well as at the drain-channel junction (region of the gate–drain overlap). The tunneling at the drain-channel junction was incorporated to include the impact of gate induced drain leakage on TFET characteristics. Abrupt source channel junction and drain-channel junctions were
assumed in all simulations, in line with several other simulation studies.

3. Gate leakage

For SOI structures, the gate leakage can be conveniently divided into tunnelling from the gate into the source and the drain. At low gate voltages, only direct tunnelling of electrons across the gate dielectric takes place from the gate into the drain. As gate voltage increases, tunnelling begins from the source into the gate, reversing the direction of gate current. This also reduces the availability of carriers in the source for current. This also reduces the availability of carriers in the source into the gate, reversing the direction of gate current.

The leakage through the gate dielectric can be given by

\[
J = \frac{qkT}{2\pi\hbar^2} \sqrt{m_1m_2} \int T(E) \ln \left\{ \frac{1 + \exp[(E_{F_1} - E)/kT]}{1 + \exp[(E_{F_2} - E)/kT]} \right\} dE,
\]

where \( q \) is the charge of the carrier, \( k \) is the Boltzmann constant, \( T \) is the temperature in Kelvin, \( \hbar \) is the Planck’s constant, \( E \) the is energy of the carrier, \( m_1 \) and \( m_2 \) are the effective masses in the lateral direction in the semiconductor, \( E_{F_1} \) and \( E_{F_2} \) are the quasi-Fermi levels on either side of the barrier, \( T(E) \) is the transmission probability of an electron or hole through the dielectric potential barrier. Schenk oxide tunnelling model was used to calculate the transmission probability or tunnelling through the trapezoidal dielectric barrier.27) This model also takes into account the image barrier lowering. Extensive calibration of Schenk’s oxide tunnelling model as well as BTBT model was carried out with previously published simulated and experimental results.

4. TFET calibration

Accurate calibration of the BTBT with experimentally fabricated TFET is a challenging task, as data related to wide design space of TFETs is not easily available for experimental results. Therefore we have calibrated the BTBT model for TFET tunnelling current with Boucart’s earlier work,24) who had calibrated her work with experimentally fabricated IBM tunnel diodes. The calibration was performed simultaneously for \( \kappa = 3.9 \) and 21, corresponding to SiO2 and HfO2. The extracted parameters were further used in calibration of gate leakage through both SiO2 as well as high-\( \kappa \) gate stacks of different thicknesses. For accuracy of gate leakage results, TFET gate leakage through both SiO2 and HfO2 gate stacks of different thicknesses. For accuracy of gate leakage results, TFET gate leakage through both SiO2 and HfO2/\( \text{SiO}_2 \) gate stack.

\[
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tunnelling model with the experimental results for 1.5 nm thick SiO2 (device 2). To consider more technologically relevant EOT, calibration of Schenk’s model with two different high-κ HfO2/SiO2 gate stacks with an EOT of 1 nm (devices 3 and 4), was carried out. As mentioned earlier, 0.8 nm EOT gate dielectrics are soon expected to enter production for FD-SOI. It is, therefore, important to study the impact of leakage through gate dielectric with 0.8 nm EOT on the performance of TFET. To take care of this, we have simulated TFET with EOT of 0.8 nm (device 5). To have an acceptable value of physical dielectric thickness, an interfacial SiO2 layer of 0.4 nm and HfO2 layer of 2.0 nm were used. The calibrated gate leakage for an EOT of 0.8 nm was found to be of the same order of magnitude as the previously published experimental result with similar EOT. Although, in the past the Schenk’s model has been used for single layer oxides, after calibration it was found to accurately predict the gate leakage of even the double layer HfO2/SiO2 gate stacks, at least for the region of TFET operation used in this study. For comparison with high-κ gate stacks, leakage through SiO2 of 1 nm (device 1) was also calibrated. As the leakage through both 1.0 and 1.5 nm SiO2 could be calibrated with similar tunnelling parameters, these parameters are also expected to be valid for the intermediate dielectric thicknesses. The details of calibration and calibrated parameters are listed in Appendix.

### Table II. List of devices with different gate dielectric.

| Gate dielectric (thickness) | EOT (nm) |
|----------------------------|----------|
| Device 1<sup>(30)</sup> SiO2 (1.0 nm) | 1.0      |
| Device 2<sup>(29)</sup> SiO2 (1.5 nm) | 1.5      |
| Device 3<sup>(31)</sup> HfO2 (2.2 nm) + SiO2 (0.55 nm) | 1.0      |
| Device 4<sup>(30)</sup> HfO2 (3.4 nm) + SiO2 (0.4 nm) | 1.0      |
| Device 5                          | 0.8      |

Fig. 3. (Color online) Calibration of the gate leakage for different dielectrics with previous published works.

Fig. 4. (Color online) Spatial distribution of the total current density in the TFET (with gate oxide thickness of 1.5 nm) in (a) the off-state and (b) the on-state.

5. Results and discussion

Figure 4 shows the spatial distribution of the total current density in the TFET at two different bias voltages. In the off-state ($V_{GS} = 0.0$ V and $V_{DS} = 0.5$ V), (i) the gate leakage is the dominant component and appears in the vicinity of the drain and (ii) there is no significant tunneling current from the source to the channel or gate induced drain leakage from the drain into the channel. In the on-state ($V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V), (i) the tunneling current from the source is the dominant component and appears in the vicinity of the source and (ii) the gate leakage is not apparent as it is overshadowed by the TFET tunneling current that is several orders of magnitude larger.

The $I_D-V_{GS}$ characteristics of the TFET for the SiO2 thickness of 1.5 nm and the $\Phi_M$ of 4.3 eV are shown in Fig. 5. At low gate bias voltages, gate leakage is the dominating component of drain current until superseded by BTBT from source into the channel. The gate leakage not only dominates the other leakage currents, but it is several orders of magnitude larger than even the initial tunneling current at the drain-channel junction. Therefore, the gate to drain tunnelling determines the effective $I_{OFF}$ of the TFET. If the gate leakage...
is not included, the off-state current can be attributed to the tunnelling at the drain channel junction near the gate. The \( I_D-V_{GS} \) characteristics of the TFET show \( I_{OFF}<10^{-16} \text{ A/µm} \). With inclusion of gate leakage, \( I_{OFF} \) increases to \( \sim 10^{-13} \text{ A/µm} \), showing that the gate leakage is more than three orders of magnitude larger than the other leakage currents. As the gate voltage is increased further, tunnelling from the source into the gate increases. This gate tunnelling, which occurs at the gate edge near the source, determines the gate leakage under ON conditions. This leakage is considerably small compared to the device ON current for SiO\(_2\) thickness of 1 nm and above. This is reflected by the negligible effect of gate leakage on device ON current. The subthreshold swing (SS) for TFET defined as

\[
SS = \frac{dV_{GS}}{d\log I_D} \text{ (mV/decade)},
\]

which is also shown in the inset of Fig. 5, for the cases with and without considering the gate leakage. The subthreshold swing minimum (SS\(_{MIN}\)) occurs when the bands are just getting aligned and the tunnelling probability increases rapidly. Due to the exponential dependence of tunnelling on the band alignment, TFET have a sharp turn on characteristics. With the inclusion of the gate leakage in the device simulations, a significant portion of the sharp turn-on of TFET is lost. When the gate leakage is not considered, the inset of Fig. 5 shows the SS\(_{MIN}\) to be 20 mV/decade. However, by including the gate leakage, SS\(_{MIN}\) more than doubles to 45 mV/decade.

The parameter that is more important than the point subthreshold swing value of SS\(_{MIN}\) is the average subthreshold swing (SS\(_{AVG}\)), defined over several decades of the drain current. We propose that the point of SS\(_{MIN}\) can be taken as the point at which the TFET turns on. This also allows to better define SS\(_{AVG}\). The average subthreshold swing can be defined between the point the TFET turns on and the point it is able to deliver a drain current of \( 10^{-7} \text{ A/µm} \). Mathematically SS\(_{AVG}\) can be defined as

\[
SS_{AVG} = \frac{1000 \times V_G@I_D=10^{-7} - V_G@SS_{MIN}}{\log(10^{-7}) - \log I_D(SS_{MIN})} \text{ (mV/decade)},
\]

where \( I_D(SS_{MIN}) \) is the drain current when subthreshold slope is minimum and \( V_G@SS_{MIN} \) is the gate voltage at this point. After including the gate leakage, SS\(_{AVG}\) increases by more than 38% from 52 mV/decade over seven orders of magnitude to 72 mV/decade over just four orders of magnitude. Gate leakage has also shifted the point of minimum subthreshold swing \( (V_G@SS_{MIN}) \) by more than 100 mV, necessitating extra 0.1 V to start tunnelling. These observations are extremely important for subthreshold circuit design. Thus, gate leakage severely restricts the advantages of TFET due to the higher operating voltage and higher leakage current. The impact of the gate metal work function on the gate leakage and the TFET characteristics is shown in Fig. 6. After inclusion of the gate leakage, significant differences emerge in the subthreshold characteristics of TFET for \( \Phi_M > 4.1 \text{ eV} \). Gate metal work function has a significant impact on the TFET characteristics. The \( I_{ON} \) and \( I_{OFF} \) can be adjusted by altering the gate metal work function. Reducing the gate work function from 4.5 to 4.2 eV enhances both \( I_{ON} \) and \( I_{OFF} \) by two orders of magnitude.

The thickness of the SiO\(_2\) was varied (from 1.0 to 1.5 nm in steps of 0.1 nm) to understand the relationship between the dielectric thickness and the gate leakage. The effect of SiO\(_2\) thickness (\( t_{ox} \)) on TFET characteristics is depicted in Fig. 7.
As expected, both \( I_{ON} \) and \( I_{OFF} \) are strong functions of the SiO\(_2\) thickness. This is due to the exponential dependence of both BTBT tunnelling and oxide tunnelling on the electric field. It can also be seen that \( I_{OFF} \) increases more rapidly than \( I_{ON} \) with a reduction in \( t_{ox} \). For a 1 nm thick SiO\(_2\), gate leakage causes \( I_{OFF} \) to increase by more than 6 orders of magnitude.

Figure 8 shows the values of \( S_{SMIN} \) for different SiO\(_2\) thicknesses. The impact of gate leakage on the subthreshold characteristics increases with reducing \( t_{ox} \). An interesting observation is the relative order of subthreshold swing minimum (\( S_{SMIN} \)) for different SiO\(_2\) thicknesses. Without considering the gate leakage, \( S_{SMIN} \) increases by increasing the SiO\(_2\) thickness. However, when the gate leakage is included, TFET with thicker SiO\(_2\) has a lower value of \( S_{SMIN} \), indicating a sharp turn-on. This is caused by the reduced gate leakage at a higher SiO\(_2\) thickness. This allows BTBT current to supersede the gate leakage at lower gate voltages. Hence, devices with lower SiO\(_2\) thickness have higher \( I_{ON} \), but their subthreshold characteristics are compromised.

Current devices employ high-\( \kappa \) gate stacks with HfO\(_2\) as gate dielectric and SiO\(_2\) as interfacial layer for reducing gate leakage by having larger physical thickness and lower EOT. We have also studied the impact of gate leakage on the TFET with different high-\( \kappa \) gate stacks having an EOT of 0.8 to 1.0 nm, as mentioned earlier in Table II. The EOT of the HfO\(_2\)/SiO\(_2\) gate stack is given by

\[
EOT = \left( t_{HfO_2} \cdot \frac{k_{SiO_2}}{k_{HfO_2}} + t_{SiO_2} \right),
\]

where \( t \) and \( \kappa \) refer to the thickness and the dielectric constant of HfO\(_2\) and SiO\(_2\), respectively. The \( I_D-V_{GS} \) characteristics for the devices 3–5 are shown in Fig. 9, both with and without including the gate leakage. It can be seen that although the gate leakage is much lower in HfO\(_2\) stacks compared to SiO\(_2\), still incorporation of gate leakage in TCAD simulations significantly alters the TFET characteristics.

The effect of gate leakage on \( I_{OFF} \) is shown in Fig. 10 for all the five devices. Even for device 3 having an EOT of 1.0 nm with 2.2 nm HfO\(_2\) and 0.55 nm SiO\(_2\), \( I_{OFF} \) increases by more than two orders of magnitude, if gate leakage is included. From Eq. (4), we can also see that by reducing the thickness of the interfacial layer, the physical thickness of HfO\(_2\) stack can be increased for the same EOT. Device 4 makes use of this phenomenon and has a total gate dielectric thickness of 3.8 nm and an EOT of 1 nm. This causes the gate leakage to reduce further. However, even with such thick gate dielectric, gate leakage increases \( I_{OFF} \) by more than an order of magnitude. Even this advantage is compromised when the EOT was reduced to 0.8 nm and \( I_{OFF} \) was found to increase by more than three orders of magnitude.

Figures 11 and 12 show the impact of the gate leakage on the subthreshold characteristics for the five device types. For devices 1, 3, and 4, having an EOT of 1 nm, the inclusion of gate leakage in TFET simulations increases \( S_{SMIN} \) by 402, 78, and 52% and increases \( S_{SAVG} \) by 90, 29, and 16%, respectively. Once again it can be observed that even with high-\( \kappa \) gate stacks with an EOT of 1 nm, gate leakage not only affects the \( I_{OFF} \), but it also increases the \( S_{SMIN} \), \( S_{SAVG} \) and shifts the gate voltage at which device turns on (\( V_G@S_{SMIN} \)). For device 5, having EOT of 0.8 nm, \( S_{SAVG} \) also increases by 31%, while \( S_{SMIN} \) increases by 124%, from 13.6 to 30.4 mV/decade, showing a substantial degradation in TFET subthreshold performance parameters.

Figure 13 shows the impact of drain bias on \( I_D-V_{GS} \) characteristics of TFET having high-\( \kappa \) gate stacks with an EOT of 1.0 and 1.5 nm thick SiO\(_2\). Application of drain
bias reduces the $V_{GS}$ required to achieve similar values of drain current, indicating the presence of drain induced barrier lowering (DIBL). The reduction of $V_{GS}$ is 111, 94, 131, and 71 mV in devices 2, 3, 4, and 5 respectively, showing that the impact of DIBL is lowest in device type 5 on account of stronger gate control.

For all the previous simulations the edge of the gate was aligned with the edge of the drain. The gate leakage can be reduced by introducing a gap ($L_{GS}$) between the edge of the gate and the edge of the drain. This can be achieved in two ways, (a) by keeping the gate length ($L_G$) constant and moving the drain away from the gate edge, thereby increasing the channel length ($L_{CH}$), as shown in Fig. 1(c), or 1(b) by keeping the channel length, $L_{CH}$, constant and reducing the gate length, $L_G$, as shown in Fig. 1(d). The two approaches are similar, the first approach is called the drain-offset and the second approach is called the short-gate.

The impact of gate leakage on the off-state current, for the drain-offset and the short-gate approaches is shown in Figs. 14(a) and 14(b), respectively. Simulations were carried out both with and without considering gate leakage for device 3 having an EOT of 1 nm. For drain-offset approach, the gap between the gate edge and the drain edge was varied from 0 nm (aligned gate) to 25 nm, keeping the $L_G$ fixed at 50 nm [Fig. 14(a)]. For the short-gate approach, the gate length was varied from 50 nm (aligned gate) to 25 nm, keeping the $L_{CH}$ fixed at 50 nm [Fig. 14(b)].

From Fig. 14(a), we can observe that when the gate leakage is not included in the simulations, introducing a drain-offset up to 25 nm has no significant impact on $I_{OFF}$, which remains at $\sim 2 \times 10^{-17}$ A/µm. After including the gate leakage in the simulations, the drain-offset of 25 nm is successful in reducing $I_{OFF}$ by a factor of 4 in comparison to the aligned gate (drain-offset of 0 nm). However, inclusion of the gate leakage in the simulations increases $I_{OFF}$ by a factor of $\sim 200$ for the aligned gate, and by a factor of $\sim 50$ for...
the drain-offset of 25 nm. It may also be noted that increasing the drain-offset beyond 10 nm has a diminishing impact on the off-state current.

In the case of the short-gate TFET [Fig. 14(b)], when the gate leakage in not considered, the off-state current starts to increase as the gate length is reduced below 35 nm. This occurs due to an increase in the BTBT tunneling at the source–channel junction. However, when the gate leakage is included in the simulations, the $I_{\text{OFF}}$ decreases as the gate length is reduced from 50 to 25 nm and then increases marginally for the gate length of 20 nm. For $L_G = 20$ nm, the $I_{\text{OFF}}$ both with and without including the gate leakage are comparable as the BTBT tunneling is the major contributor of $I_{\text{OFF}}$ at this gate length. Compared to the aligned gate ($L_{CH} = 50$ nm and $L_G = 50$ nm), TFET with a 25 nm shorter gate ($L_{CH} = 50$ nm and $L_G = 25$ nm) has almost an order of magnitude smaller off-state current of $5 \times 10^{-16} \text{A}/\mu\text{m}$. However, it is still higher by a factor of 5 compared to the case when the gate leakage is neglected in the simulations. Hence, it can be concluded that for the studied device parameters, the inclusion of the gate leakage current will critically affect the estimation of the off-state current in both the drain-offset approach and the short-gate approach, highlighting once again the importance of including gate leakage particularly for structures with EOT of 1 nm and below.

### 6. Conclusions

In this work, we have shown that the gate leakage severely degrades the TFET subthreshold parameters such as $I_{\text{OFF}}$, $SS_{\text{MIN}}$, $SS_{\text{AVG}}$, and $V_G@SS_{\text{MIN}}$. The results were found to be valid for all gate dielectric structures, both SiO$_2$ and high-$\kappa$ gate stacks, studied in this work. The gate leakage has a substantial effect on TFET with sub 1.5 nm SiO$_2$ gate dielectric. It causes $I_{\text{OFF}}$ to increase by three orders of magnitude.

The impact of gate leakage can be reduced with high-$\kappa$ gate stacks. However, even with 3.8 nm thick gate stack with an EOT of 1 nm, gate leakage increases $I_{\text{OFF}}$ by almost two orders of magnitude and $SS_{\text{MIN}}$ by 52%. For an EOT of 0.8 nm, gate leakage increases $I_{\text{OFF}}$ by three orders of magnitude, and $SS_{\text{MIN}}$ and $SS_{\text{AVG}}$ by 124 and 31%, respectively. It can therefore be concluded that with the use of high-$\kappa$ stacks the impact of gate leakage can be reduced, but it cannot be eliminated. We have also studied the two commonly employed TFET strategies, namely the drain-offset and the short-gate and found that the inclusion of gate leakage will significantly affect the estimation of $I_{\text{OFF}}$, even for these structures with an EOT of 1 nm and below. Moreover, future technology nodes are expected to have much lower EOT than 1 nm, indicating that gate leakage would be an even more important phenomenon for future TFET design, particularly for obtaining their subthreshold characteristics. Hence, it is very important to account for the gate leakage for preventing any unrealistic estimation of TFET parameters. The results also highlight the need for improved TFET designs for minimizing the gate leakage to achieve the true potential of TFET.

### Acknowledgements

Poornendu Chaturvedi is thankful to Nitin Goyal for valuable and insightful discussions on the role of the gate leakage in the TFET and the initial TFET simulations incorporating the gate leakage. He is also thankful to the Director, Solid State Physics Laboratory, Delhi for granting the permission to carry out this work and providing the required simulation facilities.

### Appendix

To ensure the validity of the results, extensive calibrations of simulation parameters for BTBT and the gate leakage with previous published works were carried out. First, the BTBT model was simultaneously calibrated for $x = 3.9$ and 21 with Boucart’s earlier work.$^{20}$ The extracted tunnelling masses of the electrons [$m_{e,tunnel}$(Si)] and the holes [$m_{h,tunnel}$(Si)] are listed in Table A-I, and were used in all further calibrations of gate leakage for all the reference device structures, i.e., device 1,$^{30}$ device 2,$^{20}$ device 3,$^{30}$ and device 4,$^{31}$ and TFET simulations.

For all the above mentioned devices, the gate leakage was calibrated with a MOS structure using parameters listed in Tables A-II to A-V, respectively. For gate dielectrics, tunnelling masses of the electrons [$m_{e,tunnel}$(SiO$_2$) and $m_{e,tunnel}$(HfO$_2$)] and the holes [$m_{h,tunnel}$(SiO$_2$) and $m_{h,tunnel}$(HfO$_2$)] were kept equal. The physical parameters of the gate dielectrics were kept similar to the original work. n-type body doping was chosen to improve convergence of simulations.

#### Table A-I. BTBT model calibration parameters.

| Parameter | Value |
|-----------|-------|
| $m_{e,tunnel}$(Si) | 0.1 |
| $m_{h,tunnel}$(Si) | 0.17 |

#### Table A-II. Device 1 calibration parameters.

| Parameter | Value |
|-----------|-------|
| $L_{CH}$ (nm) | 1.0 |
| $\chi$ SiO$_2$ (eV) | 0.89 |
| $m_{e,tunnel}$(SiO$_2$) | 0.77 |
| $m_{h,tunnel}$(SiO$_2$) | 0.77 |
| $\Phi_M$ (eV) | 4.1 |
| Body doping ($n$) (/cm$^3$) | $10^{15}$ |

#### Table A-III. Device 2 calibration parameters.

| Parameter | Value |
|-----------|-------|
| $L_{CH}$ (nm) | 1.5 |
| $\chi$ SiO$_2$ (eV) | 0.89 |
| $m_{e,tunnel}$(SiO$_2$) | 0.77 |
| $m_{h,tunnel}$(SiO$_2$) | 0.77 |
| $\Phi_M$ (eV) | 4.0 |
| Body doping ($n$) (/cm$^3$) | $10^{15}$ |

#### Table A-IV. Device 3 calibration parameters.

| Parameter | Value |
|-----------|-------|
| $L_{CH}$ (nm) | 0.55 |
| $\chi$ SiO$_2$ (eV) | 1.0 |
| $m_{e,tunnel}$(SiO$_2$) | 2.2 |
| $m_{h,tunnel}$(SiO$_2$) | 2.7 |
| $\Phi_M$ (eV) | 0.35 |
| Body doping ($n$) (/cm$^3$) | $10^{15}$ |
of magnitude agree as the previous published experimental result\(^1\) of similar EOT at \(V_G = 1.0\) V. Still, the nonphysical basis of above fitting parameters and limited range of applicability must be kept in mind, while extending these calibrated parameters to other thicknesses and dielectrics.

The \(I_G-V_{GS}\) characteristics of the TFET for all the five device types are shown in Fig. A-1 depicting gate leakage for five device structures after calibration.

**Table A-V.** Device 4 calibration parameters.

| \(t\), SiO\(_2\) (nm) | 0.4 |
| \(\chi\), SiO\(_2\) (eV) | 1.0 |
| \(t\), HfO\(_2\) (nm) | 3.4 |
| \(\chi\), HfO\(_2\) (eV) | 2.7 |
| \(m_{\text{tunnel}}\) (HfO\(_2\)) | 0.2 |
| \(\Phi_M\) (eV) | 4.3 |
| Body doping \((n) /(\text{cm}^3)\) | \(10^{15}\) |

**Table A-VI.** Device 5 calibration parameters.

| \(t\), SiO\(_2\) (nm) | 0.4 |
| \(\chi\), SiO\(_2\) (eV) | 1.0 |
| \(t\), HfO\(_2\) (nm) | 2.0 |
| \(\chi\), HfO\(_2\) (eV) | 2.7 |
| \(m_{\text{tunnel}}\) (HfO\(_2\)) | 0.4 |
| \(\Phi_M\) (eV) | 4.3 |
| Body doping \((n) /(\text{cm}^3)\) | \(10^{15}\) |

![Fig. A-1](Image)

(Color online) Calibrated \(I_G-V_G\) characteristics of the TFET with different gate dielectrics.

Tunnelling mass for the electrons \((m_{\text{tunnel}}\) HfO\(_2\)) and gate metal work function \((\Phi_M)\) were used to calibrate gate leakage. Electron affinity of SiO\(_2\) \((\chi\), SiO\(_2\)) was varied between acceptable limits \((0.89\) and \(1.0))\) to improve fit with previous published results. Although device 4 corresponds to an EOT of 1.06 nm, value of 1.0 nm was used in this study, as done in the original work.

Since, the Schenk’s model does not take into account multilayer dielectrics these tunnelling masses do not represent the true tunnelling masses, but only an empirical fitting parameter. For simulating gate leakage through an EOT of 0.8 nm, tunnelling masses were linearly extrapolated using following equation, obtained from previous two calibrations:

\[
m_{\text{HfO}_2} = -0.1429(t_{\text{HfO}_2} + t_{\text{SiO}_2}) + 0.7429.
\]

Device 5 calibration parameters are listed in Table A-VI. The calibrated gate leakage was found to be of the same order of magnitude of similar EOT at \(V_G = 1.0\) V. Still, the nonphysical basis of above fitting parameters and limited range of applicability must be kept in mind, while extending these calibrated parameters to other thicknesses and dielectrics.

The \(I_G-V_{GS}\) characteristics of the TFET for all the five device types are shown in Fig. A-1 depicting gate leakage for five device structures after calibration.

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