Design of a Ka-band receiver front end using Si-based system in package

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Abstract This letter presents a Ka-band receiver front end in the form of system in package using silicon substrate. The front end adopts a dual-channel superheterodyne structure, two GaAs downconverter chips and a power divider chip are integrated on the silicon substrate with an embedded substrate integrated waveguide bandpass filter. Wire-bonding is used for connections and unique impedance matching structure is designed and embedded into the GSG transmission line to compensate for additional insertion loss. The test results show a conversion gain of −13.4 dB without the gain of low noise amplifier. The work in this letter is one of few presentation of a RF system in the form of stacked silicon system in package, revealing the feasibility of stacked silicon in complex RF system implement.

Keywords: impedance compensation, receiver, RF front end, stacked silicon, system-in-package

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

Radio frequency (RF) circuits have the characteristics of high frequency and high power consumption, thus the reliability and miniaturization of RF systems are facing great challenges [1, 2, 3, 4, 5]. System in Package (SiP) technology, especially 3D SiP, can realize three-dimensional packaging, which has a higher density than traditional planar packaging, and is more suitable for system miniaturization [6, 7, 8, 9]. The main implementations of SiP are through ceramic substrate, organic substrate and silicon substrate dividing by substrate material. Because of the good electrical performance and high reliability of ceramic package, early RF systems mostly adopted integration solutions based on ceramic packages [10, 11, 12, 13, 14, 15, 16], but stacked ceramic packages are costly, heavy, and hard to fabricate. Besides, the 3D packaging form based on organic substrates has the disadvantages of poor heat dissipation and low process accuracy although the packaging cost is low [17, 18, 19, 20, 21, 22, 23]. Compared with ceramic laminated SiP and organic substrate laminated SiP, silicon based SiP solution has gradually become a research hotspot in academia and industry due to its advantages in low-volume, miniaturization, high performance, and easiness for multifunctional heterogeneous integration [24, 25, 26, 27, 28]. However, the application of high-frequency RF system in stacked silicon based SiP has been much fewer than ceramic-based and organic-based in research results. In this letter, a Ka-band receiver front end is designed and implemented using a silicon-based stacked package form, the side-view schematic diagram of the entire stacked package is shown in Fig. 1. Firstly, a RF receiver front end is integrated on the bottom silicon substrate and measured to work in Ka-band. The Ka-band front-end of the receiver realizes the function of converting the radio frequency signal with a center frequency of 29.8GHz into an intermediate frequency signal with a center frequency of 3GHz, and the chip-to-chip interconnection of the Ka-band front-end adopts an innovative impedance compensation method to reduce insertion loss. Secondly, in order to verify the process achievability of a complex and complete RF system based on multi-layer silicon substrates, several silicon dummy dies are mounted on the third layer using ordinary conductive paste, and the manufacturing and assembly process of the overall four-layer silicon substrate package has been designed, simulated and tested. Finally, the measured results of the conversion gain of the front-end receiver of the bottom layer are consistent with the requirements for the indicators of a receiver front-end, and the measured warpage form of the overall package structure is consistent with the simulation, the measured warpage value is far less than the warpage requirements for a multi-layer complex RF system in package, thus verifying the advantages and feasibility of silicon-based multi-layer stacked radio frequency SiP in the realization of complex radio frequency systems.

2. Design of the Ka-band front end on the bottom layer

Fig. 1 Side-view diagram of the four-layer stacked package

The system block diagram of the Ka-band receiver front-end integrated on the bottom silicon substrate is shown in Fig. 2, this system serves as a subsystem of a complete super-
heterodyne receiver system. In the actual complete receiver design, due to the high frequency of the Ka-band, the signal transmission structure between different layers such as through silicon vias, solder balls will introduce great loss to the signal transmission, so in order to avoid this situation, the Ka-band high-frequency receiver front end is completely integrated onto the bottom layer. The design of the Ka-band receiver front-end is mainly divided into four parts, the design of the SIW bandpass filter, the placement and testing of the downconverter chip, the power divider chip placement and testing, and transmission optimization of the chip-to-wirebond transmission structure. The signal transmission path is as follows: the input RF signal with a center frequency of 29.8GHz is selected by the SIW bandpass filter to become the first input of the downconverter chip, and the local oscillator signal with a center frequency of 26.8GHz is attenuated by 3 dB through the power divider to be the second input of the downconverter chip, then because the 3GHz intermediate signal generated by mixing frequency has been greatly reduced in frequency, the return loss suffered when passing through the inter-layer signal transmission structure is hugely avoided, making it can be transmitted to upper layers and performed the remaining RF signal processing.

2.1 SIW filter
The SIW bandpass filter is designed and fabricated using wafer-level silicon-based process as presented in the previous letter [29]. The substrate material is silicon and the filter is embedded in the bottom silicon substrate. The thickness of the silicon substrate is 200um with a upper passivation layer of silicon dioxide (2 um) and a lower passivation layer of polyimide (5 um). Two rows of silicon through vias form the sidewalls and cavity of the SIW filter. The bandpass filter adopts a linear coupling resonant cavity structure and it is designed using the coupling coefficient extraction method. The filter has a center frequency of 29.8GHz with an insertion loss of 3.45 dB at center frequency, the fractional 3 dB bandwidth is 5%. The return loss of the filter in the passband is less than −12 dB. The measured results of the fabricated SIW filter are presented in Fig. 3.

2.2 Power divider chip
The power divider chip presented in Fig. 4 (a) is provided by Beijing Institute of Radio Measurement. The chip is fabricated through GaAs process with working frequency at 29.8 GHz and 26.8 GHz, the former is its RF input frequency, the latter is its LO input frequency, after frequency mixing, an IF signal at 3 GHz is produced. In Fig. 5 (a), the RF input is on the left side, LO input is on the right side, IF output is on the bottom side, all of which are in the form of GSG transmission line and connected to the redistribution layer through wirebond. The chip is tested on a Keysight three-probe high frequency measurement system and the test results are presented in Fig. 5 (b), it can be observed that the conversion gain of the GaAs downconverter chip is stable at 8:6 dB in the RF input frequency range from 20 GHz to 35 GHz.

Keysight high-frequency probe platform is used for bare chip measuring, the signal loss value is about 3 dB as shown in Fig. 4 (b), which is the standard value of a 3 dB power divider.

2.3 Downconverter chip
The downconverter chip shown in Fig. 5 (a) is provided by Beijing Institute of Radio Measurement. The chip is fabricated through GaAs process with working frequency at 29.8 GHz and 26.8 GHz, the former is its RF input frequency, the latter is its LO input frequency, after frequency mixing, an IF signal at 3 GHz is produced. In Fig. 5 (a), the RF input is on the left side, LO input is on the right side, IF output is on the bottom side, all of which are in the form of GSG transmission line and connected to the redistribution layer through wirebond. The chip is tested on a Keysight three-probe high frequency measurement system and the test results are presented in Fig. 5 (b), it can be observed that the conversion gain of the GaAs downconverter chip is stable at 8:6 dB in the RF input frequency range from 20 GHz to 35 GHz.
2.4 RF signal transmission between power divider and downconverter

The signal transmission simulation model between the power divider and the inverter is shown in Fig. 6 (a). Since the power divider chip and the down-converter chip are connected to the redistribution layer by wirebond structure, the inductance effect of the wirebond structure at high frequency will introduce unwanted resonance in the working band, which makes the transmission efficiency reduce rapidly in the working frequency band. For this reason, a novel impedance compensation method is used to move the resonance point out of the working band. The specific steps are as follows. Firstly, two half models of divider plus wirebond and down-converter plus wirebond are constructed and simulated in Ansys HFSS. Secondly, the simulation results are imported into Keysight ADS software, based on microwave circuit principles [30], a transmission line of a certain length can be used as an input impedance converter, thus the Smith chart component in ADS is used to adjust the input impedance to a certain pure resistance value by adding a transitional transmission line on one side of the half model. Thirdly, a segment of transmission line whose characteristic impedance is equal to the pure resistance value in the previous step is inserted between two half models to construct an improved transmission path in ADS environment. Finally, simulate the improved transmission model in Ansys HFSS and make last adjustments to the key parameters. The simulation result comparison between the transmission efficiency before and after the improvement is shown in Fig. 6 (b). From Fig. 6 (b) it can be seen that the resonance point has been moved beyond 40 GHz, which is out of the working band.

After all the components have been placed on the front side of the bottom substrate and all chips have been successfully wirebonded, the fabrication of Ka-band receiver front end is complete, a sample of the front end is presented in Fig. 7, the size of the front end is 2 cm×1.7 cm.

3. Design and fabrication of the four-layer structure

After the front-end subsystem of the Ka-band receiver on the bottom substrate converts Ka-band RF signal to an intermediate frequency signal with a center frequency of 3 GHz, the signal can be transmitted to the upper silicon substrates through vertical transmission structures such as solder balls and through silicon vias. The greatly reduced signal frequency makes it easy to optimize the layout design of chips and redistribution layer. In addition, it is difficult to obtain the chips operating at intermediate and baseband frequency. Therefore, the electrical design on the upper substrate is not repeated here. However, due to the complexity of the stacked silicon package, the structural mechanics indicators such as warpage and maximum stress are much more severely challenged, reliability problems like excessive warpage of the package and cracks at joints between solder balls and solder pads can often occur. To avoid these potential reliability issues, the overall structure of the multi-layer package and the assembly process are simulated and optimized. In or-
der to prevent the risk of solder balls being disconnected after multiple reflows, the four-layer silicon-based package structure and its micro-assembly are designed as shown in Fig. 8. In the process flow, solder balls are used for electrical and structural connections between the first and second layers, the third and fourth layers, copper pillars made by wafer-level manufacturing process are used for connection between the second and third layers. The silicon dummy dies used to approximate the intermediate and baseband chips are attached to the front side of the third-layer substrate. The first step of the assembly process is the fabrication of all the silicon substrates use wafer-level process, including the passivation layer on the front and back of the substrate, the redistribution layer and under-ball metals. After the silicon substrates are fabricated, wafer-level ball implanting are implemented on the back side of the second and fourth layers with ball diameter of 500 um and ball pitch of 1 mm. Besides, copper pillars are electroplated on the back side of the third-layer silicon substrate at the full-wafer scale, the copper pillars have a diameter of 200 um and pitch of 500 um. After previous steps are completed, all the wafer-level silicon substrate are diced and prepared for single sample assembly, the third-layer substrate is fixed on the reflow machine table face down, the second-layer substrate is picked up and aligned with the third-layer substrate by a sucking nozzle. After aligning, the machine table is heated up to the melting point of the copper pillars and then cooled down to complete the reflow cycle of copper pillars between the second and third substrates. Then the dummy dies are mounted on the third silicon substrate by common conductive paste. Next, the downconverter chip and power divider chips are glued on the front side of the bottom substrate using conductive adhesive followed by wirebonding the chip pads to redistribution layer pads. Finally, stack all the four layers of the processed silicon substrates and align all the solder balls to their under ball metals, fix the whole structure and put the four-layer structure into a reflow furnace to complete the last-time solder ball reflow process, the whole four-layer silicon-based SiP is successfully fabricated.

Since the last step of the micro-assembly process involves all four substrates and the structure is the most complex because there are multiple inter-layer interconnections involved in the last reflow process, so the risk of excessive warping and cracking is the hugest. For this reason, structural mechanical simulation is processed in the Ansys mechanical APDL environment and the last step of the reflow process is simulated to evaluate the warpage and maximum stress. The reflow temperature is set from 260 degrees celsius to 22 degrees celsius at room temperature. As presented in Fig. 9 (a), the simulation results indicate that the maximum Z-direction warpage of the entire four-layer stack package structure after the last step of reflow is only 0.3 um, and the maximum stress appears at the outermost copper pillar between the second and third layer, the maximum stress is much smaller than the breaking strength of the copper material. So it can be seen from the simulation results that this four-layer stacked silicon based system in package meets the mechanical requirements for a complex RF system, the complete assembled stacked package sample is shown in Fig. 9 (b).

4. Measured results

The sample of the Ka-band front end on the bottom layer is tested on a Keysight high frequency three-probe platform as shown in Fig. 10. After the probes are calibrated, one probe is connected to the SIW filter input port, another probe is connected to the IF output port of the downconverter, and the 26.8 GHz LO signal is transmitted to the input port of the 3 dB power divider through the last probe which is powered by a Rohde Schwarz high-power RF signal generator. The ratio of the downconverter output signal amplitude to the filter input signal ‘amplitude is the conversion gain of the receiver front end. The measured conversion gain is $\text{−}13.4 \text{ dB}$ at the center frequency as presented in Fig. 11, the 3 dB bandwidth of the receiver front end is 1.5 GHz which is consistent with the designed SIW filter. Excluding the in-band attenuation of the SIW filter and the measured attenuation of the downconverter, it can be calculated that the loss introduced by the wirebond structure and redistribution layer transmission line is only 1.35 dB, proving the practicability of the wirebond impedance compensation structure introduced in the second section. In addition, after introducing extra signal gain of two low noise amplifiers commonly used in the Ka-band before the filter input and behind the filter output [31], the conversion gain of the receiver front end can be raised to 26.6 dB, which is enough for an actual complete RF receiver front end.

The warpage of the whole four-layer system in package sample is measured using TherMoiré Warpage Measurement System. The warpage situation of the top surface of the overall package is measured by spraying gold on the top surface and light reflection. The measured results of warpage are
shown in Fig. 12. It can be seen that the top surface is higher in the surrounding area and lower in the center, which is consistent with the simulation result, and the overall z-axis warpage is 23 μm. Although the warpage value deviates from the simulation result, it can be attributed to the accumulation of warpage in all assembly steps, but still it is a rather small warpage value and will not affect the electrical performance and reliability of the Ka-band receiver system.

5. Conclusion

In this letter, a Ka-band receiver system in package based on a multi-layer stacked silicon substrate structure is designed, manufactured, assembled and tested. The package has four layers, the Ka-band RF signal receiver front-end is integrated on the bottom layer and an innovative impedance compensation method is introduced to optimize the transmission efficiency of the chip-to-wirebond structure. In addition, the assembly process of the four-layer structure is designed and simulated to ensure that the warpage value of the overall structure is within the acceptable range. The measured results are in good agreement with the simulated values. The key transmission parameters of the receiver front end achieve the actual goals. The measured warpage value of the silicon-based stacked package is also within the required range. It can be seen that silicon based multi-layer stacked package solution has the advantages of heterogeneous integration, small warpage and high process precision. Thus, the feasibility of implementing a Ka-band receiver system using a multi-layer silicon substrate stack structure is verified.

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