Design and Research of Key Technology of Coriolis Flowmeter’s Signal Processing System

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Abstract. This paper innovatively presents DSP processor-TMS320F28335 and CYCLONE series FPGA-EP3C16F484 as a dual-core processor to design Coriolis flowmeter’s signal processing system. This paper introduces key techniques of Coriolis flowmeter’s signal processing system in details from hardware to software, using phase difference based on DTFT with negative frequency and sliding DTFT to detect phase difference, then give Cumulative mass flow measurement results.

1 Introduction

Coriolis mass flowmeter is a kind of mass flowmeter based on Coriolis principle. With about thirty years’ development since the invention of Coriolis mass flowmeter by an American company named Micro Motion in the last 70s, its technical performance indicators continue to improve, application area continues to expand.

The basic composition of Coriolis mass flowmeter includes Primary instrument and Secondary instrument. Primary instrument is composed of measuring tube, sensor and vibrator etc. Mass flow can be calculated by formula (1):

\[ q_m = \frac{K \Delta \theta}{16\pi^2 f} \]  

Visibly, the core of signal processing in Coriolis mass flowmeter is the detection and estimation of frequency and phase difference. The main work of this paper is to study the signal processing algorithm used to estimate and detect frequency and phase difference for Coriolis flowmeter, and to package the algorithm in large scale programmable gate array FPGA chip, finally, to construct a dual core digital flow meter transmitter by DSP+FPGA hardware architecture with debugging, measurement, display, alarm and other functions in one.
2 mathematical model

2.1 Mathematical model of Coriolis mass lowmeter

Literature [1,2] presented a kind of time-varying signal whose amplitude, frequency and phase are varying according to random walk model, the time-varying signal is used to simulate the actual signals of Coriolis mass flowmeter. In this model, amplitude, frequency and phase of each point are based on previous moment value plus a random number. For a better signal simulation of Coriolis mass flowmeter, the model in literature [3] is improved based on the random walk model. After the analysis of the measured signal, this paper argues that the model in reference [4] can better describe actual signals of Coriolis mass flowmeter:

\[
\begin{align*}
    y(n) &= A(n) \sin[\omega(n) + \phi(n)] + \sigma \cdot e(n) \\
    A(n) &= A(n-1) + \delta_A \cdot \sigma_A \cdot e_A(n) \\
    \omega(n) &= \omega(n-1) + \delta_\omega \cdot \sigma_\omega \cdot e_\omega(n) \\
    \phi(n) &= \phi(n-1) + \delta_\phi \cdot \sigma_\phi \cdot e_\phi(n)
\end{align*}
\]  

(2)

2.2 Frequency estimation

Lattice ANF proposed by Cho et al. [5] is cascaded by an all zero lattice filter and an all pole lattice filter. Due to Lattice ANF’s convergence speed, simple structure, strong adaptive ability, as a result, it has been widely applied to process the single frequency time-varying sine signal. The literature[6] fixed the zero in the unit circle, , realizing the adaptive notch filter by adjusting a parameter. Its transfer function is:

\[
H(z^{-1}) = \frac{1 + 2k_0 z^{-1} + z^{-2}}{1 + k_0(1 + \rho)z^{-1} + \rho z^{-2}}
\]  

(3)

In type 2.23, \(k_0\) is the weight coefficient, used to calculate the notch frequency of the signals, in the convergence process, \(k_0\) will converge to \(-\cos \omega\), \(\omega\) is discrete circular frequency of the processed signal. The structure of the lattice ANF and its realizing method as shown in Figure 1

![Figure 1. Structure of lattice Aptive notch filter.](image)

Lattice notch filter and frequency estimation process is as follows:
Step1: calculate the intermediate variables.

\[
v(n) = \frac{x(n)}{1 + k_0(n-1)[1 + \rho(n)]z^{-1} + \rho(n)z^{-2}}
\]  

(4)
Step 2: Adjust $k_0$, the method is as follows.

$$C(n) = \lambda(n)C(n-1) + \left[1 - \lambda(n)\right]v(n-1) + v(n) + v(n-2)$$  \hspace{1cm} (5)$$

$$D(n) = \lambda(n)D(n-1) + 2[1 - \lambda(n)]v^2(n-1)$$ \hspace{1cm} (6)$$

$$\hat{k}_0(n) = -C(n)/D(n)$$ \hspace{1cm} (7)$$

Step 4: The output signal for the lattice ANF is:

$$y(n) = v(n) + 2\hat{k}_0(n)v(n-1) + v(n-2)$$ \hspace{1cm} (8)$$

Step 5: $x(n) - y(n)$ is the enhanced signal after filtering, the value of the estimated frequency is $\hat{\omega}(n) = \arccos(-\hat{k}_0(n))$. The trap bandwidth of the trap is determined by the compensation offset parameter to ensure the stability of the trap.

2.3 Detection of phase difference

The calculation method of phase difference based on DTFT with negative frequency, integrating sliding DTFT proposed in this chapter, the phase difference detection method adopted in this paper as shown in Figure 2, the steps are as follows:

Step 1: Calculate the circular frequency of the sampling sequence.

Step 2: At the same time of the step (1), obtain the filtering enhancement signal $y_1(n)$ and $y_2(n)$ by the sampling sequence $s_1(n)$ and $s_2(n)$ through the lattice ANF.

Step 3: Calculate DTFT of fixed window length sequence $y_1(n)$ and $y_2(n)$ at $\hat{\omega}$ using sliding DTFT recursive algorithm, getting $S_1(\hat{\omega})$, $S_2(\hat{\omega})$, and find out $\tan\phi_1$ and $\tan\phi_2$.

Step 4: Calculate $m_1 \sim m_4$ by $\hat{\omega}$ and $N$, and substitute $m_1 \sim m_4$, $\tan\phi_1$ and $\tan\phi_2$, at last obtain the phase difference.

![Figure 2. Flow chart of the phase difference detection method.](image)

3 Key technology of hardware

According to the requirement of Coriolis mass flowmeter for digital signal processing, driver capacity, output signal and other functions, this paper design the system with the hardware architecture of FPGA+DSP. In the system FPGA is used as a digital signal
processor, in addition, its function also includes calculates and generates the drive signals for the interface logic used for LCD and keyboard module etc. The DSP is used to calculate the mass flow, volume flow, cumulative flow, density, temperature etc., in addition, dsp is also responsible for the current output, frequency output, RS485 bus and the implementation of human-computer interaction interface. The overall system hardware block diagram shown in figure 3. Among them, DSP chip select TI's TMS320F28335, and FPGA chip select Cyclone company's Altera chip EP1C6Q240C8.

![Figure 3. Hardware diagram.](image)

The transmitter is divided into five modules as below: digital signal processing module, excitation module, human-computer interaction module and transmission module. The signal conditioning module comprises of two pick-up coil signal conditioning, filtering and amplifying circuit, and a temperature signal processing circuit. Digital signal processing module mainly consists of a FPGA chip and the A/D chip, this module is used to transform the output signal of the conditioning module into digital signals, and then the digital elliptic filter, STFT, Goertzel algorithm processing embedded in FPGA.

### 4 Test and conclusion

This paper take Electronic scale measurement results as prevail, calculating the cumulative flow of a experiment, then calculate the cumulative value of time difference by method in this paper. After 10 experiments, obtaining the flow coefficient by the mean ratio of K=128.3728. After the discharge coefficient is determined, taking 10 independent experiments. Regulating valve opening randomly in each experiment so that the size of the flow past the pipeline in the experimental changes, in order to detect the ability of the flow measurement under the condition of non-steady flow by the signal processing method in this paper. Recording the flow value of electronic scale and calculated flow value of method in this paper at the end of the experiment, the record result as shown in Tab.1. Tab.1 shows that the signal processing method of the measured mass flow is high-precision, Compared with the real value from the electronic scale, error can be controlled less than 2 per thousand.
Table 1. Cumulative mass flow measurement results.

| experimental group number | Mass flow measurement (kg) | error | Relative root mean square error |
|---------------------------|---------------------------|-------|--------------------------------|
|                           | Electronic scale          |       |                                |
|                           | (Tentative for the true value) |       |                                |
|                           | Method in this paper      |       |                                |
| 1                         | 72.54                     | -0.11 | 1.52‰                         |
| 2                         | 97.82                     | -0.076| 0.78‰                         |
| 3                         | 123.78                    | 0.16  | 1.29‰                         |
| 4                         | 135.92                    | 0.08  | 0.61‰                         |
| 5                         | 154.64                    | 0.24  | 1.57‰                         |
| 6                         | 178.08                    | -0.22 | 1.28‰                         |
| 7                         | 195.46                    | 0.16  | 0.84‰                         |
| 8                         | 237.66                    | -0.38 | 1.62‰                         |
| 9                         | 278.42                    | 0.18  | 0.63‰                         |
| 10                        | 319.34                    | 0.49  | 1.53‰                         |

This paper mainly studies the experimental platform of Coriolis mass flowmeter from signal processing method to hardware design. The design in this paper realizes data acquisition, valve control function, and embedded signal processing method proposed in this paper. This paper implement platform design for flow calculation preliminary.

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