Specognitor: Identifying Spectre Vulnerabilities via Prediction-Aware Symbolic Execution

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Abstract—Spectre attacks exploit speculative execution to leak sensitive information. In the last few years, a number of static side-channel detectors have been proposed to detect cache leakage in the presence of speculative execution. However, these techniques either ignore branch prediction mechanism, detect static pre-defined patterns which is not suitable for detecting new patterns, or lead to false negatives.

In this paper, we illustrate the weakness of prediction-agnostic state-of-the-art approaches. We propose Specognitor, a novel prediction-aware symbolic execution engine to soundly explore program paths and detect subtle spectre variant 1 and variant 2 vulnerabilities. We propose a dynamic pattern detection mechanism to account for both existing and future vulnerabilities. Our experimental results show the effectiveness and efficiency of Specognitor in analyzing real-world cryptographic programs w.r.t. different processor families.

Index Terms—Branch prediction, side-channel analysis, spectre attacks, speculative execution, symbolic execution

I. INTRODUCTION

The performance of modern processors have increased significantly during past decades by increasing the working clock frequency and shrinking transistor technology. However, they reached their performance limit due to increased fault rate and increased temperature. To further increase the CPU performance, vendors applied other performance enhancement techniques such as increasing the number of cores and optimizing the instruction pipelining.

Instruction pipelining includes complex parallelization techniques to increase the processor performance. However, un-resolved dependency issues of instructions could stall the pipelines and reduce the instruction-level parallelism. To overcome the dependency issues, modern processors use speculative execution [1]. During speculative execution, the processor uses micro-architectural optimizations to predict the control flow dependencies, data dependencies and even the actual data. CPU prefetch units employ techniques to predict future instruction stream based on previous patterns. The execution continues according to the prediction until the prediction is evaluated. Since the prediction may turn out to be wrong (e.g., mis-predicted branch outcome), the processor might need to roll back the execution in which it discards the executed instructions, retrieves the last valid micro-architectural state (i.e., registers and buffers including PC), and re-fills the CPU pipelines with the correct instruction stream.

Although the correct architectural state of the system is restored while rolling back, the micro-architectural side effects of the speculative execution remains in the system, e.g., loaded cache lines. Based on these side effects, the family of Spectre [2] attacks have been discovered. Spectre attacks use the side-effects of speculative execution to obtain sensitive information. Unfortunately, detecting Spectre attacks is challenging since there are many factors that can affect the system behavior and the length of speculative execution such as the processor speed, the concurrency level, the memory link speed, and etc. The most precise approach for detecting Speculative-type vulnerabilities in a program is to run it on the physical system and to try one input at a time and monitor the micro-architectural side effects of speculation during execution. This approach is extremely slow because of limited hardware resources, large number of inputs, and large number of factors that can affect the execution [3]. Other approaches apply offline techniques to run the code with respect to (w.r.t.) abstractions about the environment and using symbolic values as input. Symbolic execution [4], [5] based techniques have been traditionally used to explore program paths (w.r.t. path conditions) to find software vulnerabilities [6], [7], to generate high coverage test cases [8], and to find inputs that cause program errors [9], [10]. Therefore, they mainly do not consider the micro-architectural components (e.g., prediction logic) in their analysis. However, recent approaches [11]–[14] employ a non-deterministic and history-agnostic prediction logic only for conditional branch instructions. These approaches apply inaccurate and inefficient exploration of the program execution states that results in detecting false positive and false negative cases. These approaches are inaccurate because they do not consider Branch Target Buffer (BTB) for conditional branch prediction while some processors (e.g., Intel Pentium 4 [15]) only employ BTB in their prediction logic as the primary means of prediction. These approaches are also inefficient because they do not consider an accurate prediction logic for speculative execution which results in many infeasible path exploration. For example, our evaluation results show up to 80% additional infeasible speculative path exploration by KLEESPETRE [14].

In addition, some techniques [11], [12], [16] that employ non-interference in their analysis lack the ability to record the system state along the program execution. For example, SpecSafe [11] asks a solver to generate any history trace for prediction logic that could cause information leakage. This approach considers a powerful adversary that can interrupt the victim process and train the branch prediction at
any moment, while modern processors \cite{17}–\cite{19} mainly use process-specific information for branch prediction which can be flushed on a context switch. In other words, training the branch prediction unit by adversary might not reflect the branch prediction outcome of the victim process. Hence, considering all prediction outcomes results in capturing false positives for many processor families. In addition, recent approaches that employ speculation do not address indirect branch prediction.

We propose Specognitor an accurate and efficient prediction-aware symbolic execution framework to soundly explore all feasible program paths and search for information leakage w.r.t. a certain processor. Specognitor simulates the micro-architectural state of the system during symbolic execution, generates the possible speculative paths according to the prediction logic, and searches for certain patterns and information leakage. Our framework explores fewer speculative paths than existing techniques \cite{11}, \cite{12}, \cite{14} because of the underlying prediction logic. However, since it employs a dynamic prediction model, it might explore completely different speculative paths than existing approaches (e.g., in case of using Branch Target Buffer).

To sum up, this paper makes the following contributions:
- We show inaccuracy of the state-of-the-art tools in detecting spectre vulnerabilities w.r.t. the micro-architectural configuration of a system.
- We propose Specognitor\footnote{Specognitor is available at https://github.com/sahraeeali/Specognitor} a prediction-aware symbolic execution framework to automatically explore program paths and detect speculative cache side-channels.
- We propose a pattern detection monitor to effectively define security threats and find them in execution traces.
- We incorporate taint analysis in symbolic execution to propagate meta information.
- We evaluate efficiency, real-world applicability, and scalability of Specognitor to detect speculative cache side-channels w.r.t. spectre variant 1 and variant 2.

Outline. This paper is organized as follows. Section II overviews the technical background of Specognitor. Section III outlines the details of prediction-aware symbolic execution and the pattern detection monitor. Section IV provides technical implementation details of Specognitor. In section V we present our evaluation results. In section VI we further discuss features, limitations, and future works. In section VII we review the related work. We conclude our work in Section VIII.

II. BACKGROUND

Before getting into more details of Specognitor, we discuss the technical backgrounds that we use for implementing it.

A. Prediction Logic

Modern processors use branch predictors to increase the number of instructions available for execution that helps in utilizing instruction level parallelism (ILP). A branch direction predictor speculates whether a conditional branch is likely to be taken or not. A branch target predictor predicts the target of branch/call instructions. These units can employ static or dynamic techniques. Static branch prediction techniques are simple and easy to implement and require little hardware resources. These techniques do not use any run-time information about branch behavior. However, dynamic branch prediction techniques are more complex and use the run-time information to enhance their performance. These techniques can adapt to the behavior of the program during execution \cite{20}. In this paper, we use two common prediction techniques for direction prediction and target address prediction. As we see in section II-B most processors use these two techniques to implement their prediction logic.

1) Two-Level Prediction Table: The two-level prediction table is a branch direction prediction technique that uses two separate levels of information to predict the branch outcome.

The first level consist of the history of the last k branches stored in a Branch History Register (BHR). BHR is an n-bit shift register that records "1" if a branch is taken and "0" if it is not taken. The BHR shifts out the information of oldest branch when the outcome of a new branch is available. The second level of this prediction technique is called Pattern History Table (PHT). PHT is a $2^m$-entry table of saturating counters. There are three implementation schemes for each level, i.e., global history scheme, per-set history scheme, and per-address history scheme. The implemented scheme determines the number of BHRs and PHTs, the number of address bits used (from PC), and the relation between n and m. Elaborate details of these schemes are contained in \cite{21}–\cite{23}. In this paper, we use the global history scheme for both levels parameterized by n. In other words, we use an n-bit BHR and a $2^m$-entry PHT of 2-bit saturating counter. When the actual result of the branch is evaluated, its respective counter is incremented in case of taken or decremented in case of not taken. Since we use the global history scheme, we do not use the PC value. Figure 1a shows a two level prediction table in which both levels use global history scheme. The content of BHR is 0111 which is used to index the PHT. The 2-bit saturating counter of the PHT entry shows the value of 10 which means the prediction outcome is taken.

2) Branch Target Buffer: The Branch Target Buffer (BTB) is a component that stores the target address of branch instructions. BTB architecture is close to cache with sets, tag bits, and different set-associativities. BTB can also be implemented in global history scheme, per-set history scheme, and per-address history scheme. These schemes determine the number of sets and the number of bits used as tag. Figure 1b shows the architecture of a 32-entry direct-mapped BTB (BTB:) with 4 bits of tag implemented with per-set scheme \cite{22}. While speculating, if the branch predictor predicts the branch to be taken and there is a hit in the BTB (BTB-hit), the stored address in the respective BTB set is used as the next PC. If the branch predictor predicts the branch to be taken and the respective entry is not in the BTB (BTB-miss), the processor can stall the execution or behave as if the branch is not taken. When the prediction outcome is resolved, the respective BTB-entry is updated.
B. Branch Predictors in modern Processors

In this section, we study the branch prediction mechanisms implemented by different architectures.

1) ARM - Cortex-A53: [17] is a low-power, mid-range processor that implements ARMv8-A architecture instruction set. It is an in-order 8-stage pipeline processor with symmetric dual-issue unit. The Instruction Fetch Unit of Cortex-A53 processor contains a 2-way set associative cache that can hold 16 instructions (32 16-bit T32 instructions). It uses two prediction schemes. The target predictor contains a 256-entry BTB to predict the address of indirect branches/calls. The direction predictor is implemented according to the global prediction scheme that uses BHRs and a 3072-entry PHT.

2) ARM - Cortex-A7: [19] is a high-performance, low-power processor that implements ARMv8-A architecture instruction set. It is an in-order 8-stage pipeline processor with direct and indirect prediction units [24]. It has a 2-way set associative instruction cache that can hold 8 ARM instructions (16 Thumb 16-bit instructions). Its target prediction unit contains an 8-entry BTB (BTAC) and its direction prediction unit adopts a global prediction scheme that uses BHRs and a 256-entry PHT.

3) ARM - Cortex-A9: [18] is a high-performance, low-power, out-of-order ARM processor that implements ARMv7 architecture instruction set. It is a multi-issue superscalar, 8-stage pipeline processor that predicts all branch instructions, such as conditional, unconditional, and indirect branches regardless of the addressing mode. The prediction logic contains both target prediction and direction prediction. The target prediction unit uses a 2-way BTB (BTAC) with 512, 1024, 2048, or 4096 entries. The direction prediction unit uses a global history scheme that has 1024, 2048, 4096, 8192 or 16384 PHT entries.

4) Alpha - 21264: [25] is a high-speed, superscalar, 7-stage pipeline, out-of-order processor. It accepts 80 in-flight instructions. Its branch prediction unit uses a complex technique which implements two separate branch predictors and dynamically chooses one of their outcomes to fetch instructions. The first technique uses a two-level prediction with local history. Its first level comprises a table that holds 10 bits of history for up to 1024 different branches. The 10-bit history is then used to index a 1024-entry PHT. The second technique uses a global prediction scheme where a 12-bit BHR keeps the history of the last 12 branches and is used to index a 4096-entry table of 2-bit saturating counters.

5) Intel - Pentium 4: [15] is a high-performance processor manufactured by Intel based on NetBurst microarchitecture [26]. It is an out-of-order, 20-stage pipeline processor with branch prediction unit. The dynamic branch predictor uses a 4096-entry BTB to capture the branch history information of the program. In case of BTB-miss, it uses a simple static Backwards Taken Forward Not Taken (BTFNT) [27] branch prediction technique.

6) ARM 11: [28] is a high-performance, low-power, 8-stage pipeline processor that implements ARMv6 architecture instruction set. It uses two branch prediction techniques. The dynamic branch predictor contains a 128-entry BTB (BTAC) to predict the address of a branch instruction. In case of BTB-miss, the prediction unit uses the BTFNT [29], [27] technique.

C. Side-Channel Attacks

Side-channel attacks [29] exploit the side-effects of computation from the physical implementation of a system to infer sensitive information. These side-effects include execution time of cryptographic algorithms [29], power and energy consumption of the system [30], electromagnetic emissions [31], [32], and computation faults [33]. However, cache attacks [34], [36], are the most prominent type of side-channel attacks.

Cache attacks measure the access time of different memory locations to reconstruct the secret information. The CPU cache is a small but fast memory inside the processor which reduces memory access time by storing the frequently accessed data. Different types of cache attacks are Evict+Time [36]–[38], Prime+Probe [36], [39]–[42], and Flush+Reload [43], [44].
Flush+Reload attacks rely on shared cache-line granularity. In this type of side-channel attacks, the adversary flushes the last-level cache and tries to reload the shared data. Small delay in reloading the data shows that the victim has already loaded the cache line into CPU cache. On the other hand, Prime+Probe attacks does not rely on shared memory. The adversary fills the CPU cache and checks whether the victim evicts any cache entry from the cache.

D. Spectre Attack

Spectre [2] is a side-channel vulnerability has been discovered in modern processors. Spectre-style attacks deliberately exploit speculative execution in victim’s code to leak the content of an arbitrary memory location, for example, the secret key of a cryptographic computation. Kocher et al. [2] categorized Spectre vulnerabilities into 4 variants w.r.t. the poisoned architectural component. These variants are as follows: i) in spectre variant 1, the adversary uses conditional branches as the source of misprediction; ii) in spectre variant 2, the adversary uses mispredicted indirect branches/calls to leak information; iii) in spectre variant 3, the adversary poisons Return Address Buffer (RSB) to mis-direct the execution flow; and iv) in spectre variant 4, the adversary uses the memory disambiguation unit to mispredict data flow dependencies.

In this paper, we mainly focus on Spectre variant 1 and variant 2 as they target branch prediction unit of the processor. **Spectre Variant 1.** Figure 3a represents a code fragment taken from [2] which demonstrates a conventional spectre variant 1 vulnerability. In this example, assume array1 and array2 both contain only public data. Moreover, assume the prediction unit predicts the condition in line 4 as taken while $x > array1_{-size}$. Assume the adversary can control the value of $x$ and tries to learn the secret key which is placed somewhere in the victim’s memory space. According to our assumptions, the adversary can access an out-of-bound value (i.e., the key) by controlling the value of $x$ in $array1[x]$. Loading the secret key occurs during speculative execution and the instruction will be discarded after evaluating the condition at line 4, so it does not violate the correctness of the program. However, execution of out-of-bound memory access and its subsequent memory access at line 6 would result in loading a key-dependent cache line into the CPU cache. The adversary can infer the value of the secret key by performing a conventional cache attack. The vulnerability in Figure 3a is based on a specific pattern description: i) a vulnerable branch instruction (line 4), ii) a load secret instruction (line 5), and iii) a load instruction which expose the key to the adversary (line 6). In this paper, we refer to this pattern as BR-LD-LD. However, recent work [11], [16], [45] has shown other patterns categorized as spectre variant 1. Figure 4 shows a code fragment where loading the secret value happens before the branch instruction, thus it could be represented as LD-BR-LD pattern.

**Spectre Variant 2.** Figure 5 shows a code example categorized as spectre variant 2. In this example, assume that the BTB entry for the indirect call at line 10 contains the address of unsafe_function. In other words, when the processor reaches line 10 and asks for a target from BTB, the BTB returns the address of unsafe_function. However, according to line 16, the safe_function should be executed. Further, assume the adversary can control the value of idx. While the processor speculatively executes the unsafe_function, the instruction at line 6 loads an out-of-bound secret key and the instruction at line 7 exposes the secret to cache attacks.

A few defense mechanisms have been proposed to protect the system against spectre side-channel attacks variant 1 and variant 2. Two of the most prevalent techniques used forspectre variant 1 and variant 2 is fencing [47] and Retpoline [48], respectively. Placing fence instructions before branches disables the speculation which increases the execution time significantly. Moreover, applying Retpoline increases both execution time and energy consumption since the processor...
executes some dummy instructions. Compilers use these mechanisms to secure a program against spectre attacks. However, they blindly apply them for all branch instructions in the program. To reduce the cost of these mechanisms, static analysis tools try to optimize usage of defense mechanisms to reduce the execution time and energy consumption of the program while maintaining the system safety and security.

E. Threat and Adversary Model

Here, we consider that the victim and attacker codes are running on the same physical device. We assume our processor is secure from physical attacks such as differential power analysis attacks [30] and timing attacks [29]. Given a specific cache model and a specific prediction model, we assume an adversary who can control the provided inputs to the program and perform cache timing attacks via another thread or process on the same device at any time during execution. Commonly, the inputs provided to the program may correspond to user input, a specific data received via network, or a pre-defined input. We consider common cache timing attacks such as FLUSH+RELOAD [43], [44] or PRIME+PROBE [36], [39]–[42] where the adversary can measure the access time for each cache line or cache set. In our model, branch predictors are process-specific, so we only consider same address-space training [46]. However, the adversary is able to make the victim process use full length of speculation window by mounting denial-of-service (DoS) attacks [49], [50] which can block shared hardware resources that are necessary for evaluation of the prediction outcome.

III. Prediction-Aware Symbolic Execution

Specognitor’s 4 major units as presented in Figure 9 are the symbolic execution engine, the speculative execution model, the cache model, and the monitor. Specognitor also combines taint analysis with symbolic execution to identify secret-dependent values. In the following we elaborate on each unit.

A. Symbolic Execution Engine

Specognitor’s symbolic execution engine takes a program \( P \) that is a sequence of LLVM \([51],[52]\) instructions and symbolically executes it w.r.t. the speculative execution model. Symbolic engine generates program traces according to the input values and the CFG. According to Figure 6, a program trace \( \tau \) is a sequence of instructions determined by the CFG and symbolic values. We use \( \mathcal{T}_P \) to denote the set of all traces of program \( P \). A program trace represents a complete execution of the program w.r.t. a specific set of inputs and the path condition \( \psi \). \( \tau_\psi \) is a program trace in which the path condition \( \psi \) holds. For example, in Figure 3 the two program traces are \( \tau_{[x\geq array1\_size]} \) and \( \tau_{[x< array1\_size]} \). Execution of the program trace \( \tau \) results in generating a sequence of events \( E_\tau \). These events are the communication channel between the execution engine and other components such as prediction logic and cache. Through these events a processor can modify the micro-architectural state of the components. Events are trace-specific that is execution of identical instructions in two different traces might generate different events. An event convey multiple information about the instruction: i) name, ii) the speculation status, iii) whether it uses symbolic operands, iv) whether it uses secret-dependent operands, and v) addresses accessed by memory access instructions (i.e. Store and Load).

| Programs | \( p := p_1; p_2 \mid inst\_label \) |
|-----------------|---------------------------------|
| Program trace   | \( \tau := <\ inst_0, inst_1, inst_2, \ldots, inst_k > \) |
| Event           | \( e := \{ \text{name}, \text{speculation}, \text{symbolic access, secret access, memory info} \} \) |
| Execution Model | \( inst_i \xrightarrow{e_i} inst_{i+1} \) |
| Event projection of a trace | \( inst_0 \xrightarrow{e_0} inst_1 \xrightarrow{e_1} inst_2 \ldots \xrightarrow{e_{k-1}} inst_k \xrightarrow{e_k} \text{EOP} \). |

![Fig. 6: Program and execution semantics.](image)

B. Speculative Execution Model

We parameterize our speculative model on two main features:

- Prediction model: we model two types of branch predictors. The two-level prediction logic is only used for conditional branches and parameterized by the size of BHR. For example, PHT4 corresponds to a two-level branch prediction where the first level uses a 4-bit BHR and the second level uses a 2^4-entry PHT. The branch target buffer can be used for both conditional branches and indirect branches. It is parameterized by the number of BTB sets, the number of BTB ways, and the number of tag bits.
- Speculative execution window \( (\omega) \): in out-of-order processors, instructions are executed speculatively from the reorder buffer, so the size of the reorder buffer is considered as the maximum depth of speculative execution. On the other hand, in in-order pipeline processors, the number of pipeline stages represents an upper bound for the speculative execution window [53].

Based on these two features, Specognitor generates full-length speculative traces during execution w.r.t. \( \omega \) on conditional branches and indirect branches/calls. In Figure 3 for the \( \tau_{[x\geq array1\_size]} \) program trace, when the symbolic execution engine reaches the branch instruction, it asks the prediction logic for next instruction. If the predictor mispredicts the outcome and returns line 5 as the next instruction, Specognitor modifies the program trace and inserts the speculative trace. Since there might be other branch instructions in the speculative trace, Specognitor applies symbolic execution from the new mispredicted instruction and generate all possible speculative traces w.r.t. the prediction logic up to the length of \( \omega \). Specognitor uses the prediction logic for all speculative and non-speculative branches. When the speculative traces...
A monitor is a 5-tuple \((Q, \Sigma, \delta, q_0, F)\), where:

\[
Q := \{\text{Start, Node}_1, \text{Node}_2, \ldots, \text{Node}_n\} \\
\Sigma := \{np_1, np_2, \ldots, np_n\} \\
\delta := \{(\text{Start, Node}_1), (\text{Node}_1, \text{Node}_2), \ldots, (\text{Node}_{n-1}, \text{Node}_n)\} \\
q_0 := \text{Start} \\
F := \{\text{Node}_n\}
\]

Fig. 7: Formal description of a monitor.

are executed, Specognitor updates the branch predictor only for the non-speculative branch instruction, that is line 4 in Figure 3.

C. Cache Component

To model the cache behavior, we use the same cache modeling as KLEESPECTRE [14]. In this model, the cache captures memory access operations and tries to model the cache behavior, i.e., loading a cache line that might evict previous cache lines. Since our cache modeling follows prior work [14], we eliminate the model description. However, we define a communication event \(C\) between the cache and the monitor. Through this communication channel the cache component can send information about its state to the monitor. \(C_i\) shows the state of the cache after receiving the event \(e_i\).

D. Pattern Detection Monitor

To keep records of the system state during execution, we propose a monitoring component. We present our monitor as a directed path, i.e., a finite sequence of distinct nodes which are connected by directed edges (see Figure 7). While executing a program trace, our monitor tries to fire transitions and propagate tokens. A token is a 4-tuple \(t = (id, pid, inst, ttl)\) where \(id\) is the unique identifier of the token, \(pid\) is the id of its predecessor, \(inst\) is a structure containing instruction information, and \(ttl\) is the liveness of the token. The monitor copies and moves a token from \(Node_i\) to \(Node_{i+1}\) when it observes events \((e_{i+1}, C_{i+1})\) that satisfies all properties specified by \(Node_{i+1}\) \((np_{i+1})\). Obviously, \(Node_i\) should contain a token before propagating to \(Node_{i+1}\). The transition rule of a token can be formalized as follows:

\[
(e_j, C_j \models np_{i+1}) \& ((id, pid, inst_k, ttl) \in Node_i) \\
\Rightarrow ((id', id, inst_j, ttl) \in Node_{i+1}) (1)
\]

The monitor’s node properties \((np)\) are as follows:

- **Instruction:** specifies the name of instruction such as branch, call, load, store, and etc.
- **isSpeculative:** checks whether the instruction is executed in the wrong speculative instruction stream w.r.t. the prediction logic.
- **isConst:** checks whether the operands are symbolic.
- **isSensitive:** checks whether the operands are secret-dependent.
- **checkCacheState:** after executing the instruction, checks whether the cache is vulnerable against cache attacks.
- **startTTL:** starts a time-to-live counter for the token and all its successors. This property is used for checking whether certain instructions are executed within a window.
- **stopTTL:** stops the time-to-live counter. This property specifies the end of the execution counter for instructions.

The initial node of the monitor is always the \(\text{Start}\) node in which there is a token. Along execution, the execution engine sends events to the monitor. When a token reaches a node with \(\text{startTTL}\) property, the monitor starts a counter for it. It decrements the counter upon receiving an event. If the token reaches a node in which \(\text{stopTTL}\) property is true, the monitor stops the counter. Otherwise, the monitor decrements the counter until it reaches 0 and expires the token.

We use the following definitions to describe a leakage-free program.

**Definition 1.** In an execution trace, if there is a pair of events \((e_k, C_k)\) that satisfies \(np_i\), then \(P_{(\text{Node}_i)}\) is true in the execution trace. In other words, \(P_{(\text{Node}_i)}\) is true iff \((e_k, C_k) \models np_i\).

**Definition 2.** \(P_{(\text{Node}_{i_1} \rightarrow \text{Node}_{i_2} \rightarrow \cdots \rightarrow \text{Node}_{i_n})}\) is true in an execution trace, iff there exist a pair of events \((e_k, C_k)\) that satisfies \(np_j\) while there is at least one path from \(i\) to \(j - 1\) in which all nodes contain at least one token.

According to definition 1 and 2 we express a leakage free program as follows:

\[
\exists \tau \in T_P : P_{(\text{Node}_1)} \& \\
P_{(\text{Node}_1 \rightarrow \text{Node}_2)} \& \\
P_{(\text{Node}_1 \rightarrow \text{Node}_2 \rightarrow \text{Node}_3)} \& \\
\ldots \& \\
P_{(\text{Node}_1 \rightarrow \text{Node}_2 \rightarrow \cdots \rightarrow \text{Node}_n)} (2)
\]
TABLE I: Taint propagation rules. ⊖ represents a unary operator. ⊗ represents a binary operator.

| Expression          | Description                                                                 |
|---------------------|-----------------------------------------------------------------------------|
| \( e_2 = \ominus e_1 \) | \( e_2 \) is tainted if \( e_1 \) is tainted.                             |
| \( e_3 = e_1 \odot e_2 \) | \( e_3 \) is tainted if \( e_1 \) or \( e_2 \) are tainted.             |
| \( \text{store } \text{memLoc}, \text{reg} \) | The memory content indexed by \( \text{memLoc} \) is tainted if the content of \( \text{reg} \) is tainted. |
| \( \text{load } \text{reg}, \text{memLoc} \) | The content of \( \text{reg} \) is tainted if the memory content indexed by \( \text{memLoc} \) is tainted. |

A program \( P \) is leakage-free w.r.t. the micro-architectural configurations and pattern model if there is no trace \( \tau \) in which the monitor can propagate a token to the last node. Figure 8 shows the monitor workflow in detecting the leakage pattern for the code snippet represented in Figure 3a. In the beginning, the pattern detector starts from the Start node. When the symbolic execution engine reaches the branch instruction at line 4, it generates an event which satisfies \( np_1 \). Therefore, the monitor propagates a token to node \( BR \). Then, the execution engine speculatively executes the load instruction at line 5 which loads the secret. The events generated from this execution satisfy \( np_2 \) and the monitor propagates the token to the next node. Finally, the execution engine speculatively executes the load instruction at line 6 that leaks the secret and generates \( e_6 \). After loading a secret-dependent address to cache, the cache model generates \( C_6 \) which indicates that the cache is vulnerable to cache attacks. The generated events \( e_6 \) and \( C_6 \) satisfy \( np_3 \), so the monitor propagates the token to the last node (Node\( e_3 \)) and reports a new leakage pattern. Checking the cache state is optional and can be used according to the value of checkCacheState defined by the user.

E. Taint Analysis

In Specognitor, we adopt taint analysis to propagate the dependency of instructions and memory locations on secret keys. Since LLVM instruction set uses virtual registers in Static Single Assignment [54] form, it is crucial to propagate the secrecy of key values so that the generated events in the subsequent instructions can use it for detecting leakage. For example, in code fragment of Figure 3a after loading the secret value of array1[x] at line 5 and storing it in the temp variable, it is important to taint the temp variable so that we detect secret-dependent memory access at line 6 (array2[temp+64]). We summarize the taint propagation rules in Table I. According to Table I, the result of binary and unary operations is tainted if the operand(s) are tainted. For store instructions, the content of the memory location with address \( \text{memLoc} \) is tainted if the content of register \( \text{reg} \) is tainted. Similarly, for load instructions, the content of register \( \text{reg} \) is tainted if the content of memory location with address \( \text{memLoc} \) is tainted.

IV. IMPLEMENTATION

We developed Specognitor on top of the state-of-the-art symbolic execution engine KLEE v2.1 [8]. It also adopts cache state modeling from KLEE-Spectre [14]. Specognitor uses clang v6.0 as the back-end compiler and takes programs in LLVM bitcode format generated with LLVM-6.0. In addition, it takes pattern models in JSON format and architecture model as command line options. Input programs containing external function calls are linked with KLEE-uClibc [55] before being processed by Specognitor. We use the SMT solver STP [56] to check the satisfiability of symbolic formulas during execution. Figure 9 shows the front-end view of Specognitor.

V. EVALUATION RESULTS

In this section, we present our evaluation results on effectiveness, real-world applicability, and scalability of the Specognitor. We evaluate the tool by answering the following research questions:

RQ1: How effective is Specognitor in detecting different types of Spectre variant 1 and Spectre variant 2?
RQ2: How effective is the architecture modeling of Specognitor w.r.t. real-world processors?
RQ3: Can Specognitor detect vulnerabilities in real-world cryptographic programs?
RQ4: How computationally efficient is the prediction-aware symbolic execution compared to a state-of-the-art tool without prediction logic?
RQ5: How computationally expensive is the prediction-aware symbolic execution compared to the pure symbolic execution?

Experimental Setup. To conduct our experimental evaluation, we run our benchmarks on a quad-core Intel i7-8665U processor with 16GB of RAM on Ubuntu 18.04.6 LTS. We compile our programs using Clang-6.0 with -O0 optimization level. Since cache modeling is not part of the main contributions of this work and mostly follows prior work [14], we do not consider it in our evaluation results. All BTB configurations are direct-mapped and parameterized by the number of sets unless otherwise stated.

A. Pattern Detection

In the first step, we focus on testing effectiveness of Specognitor on detecting different vulnerability patterns (RQ1) w.r.t. spectre variant 1 and spectre variant 2.

Initially, we use two sets of litmus tests: first, we take 15 examples proposed by Kocher et al. [2] to perform spectre variant 1 attacks targeting PHT of the processor. We add an examples to these 15 examples to create a benchmark...
BTB-based configurations happen in two different locations.

For example, the leakage detected for PHT-based configurations and BTB-based configurations except for example v09. However, in this example, the leakage detected for PHT-based configurations and BTB-based configurations happen in two different locations.

In PHT benchmarks, we mainly use BR-LD-LD pattern, except for example v11 and v12 where the leakage is caused by branching on key-dependent value. For these examples, we use a LD-BR-LD pattern, where i) the first LD loads a secret key, ii) the BR instruction uses the secret value in a comparison, and iii) the last node is a simple load instruction.

The adversary can infer key value by checking whether array[0] is loaded in the cache. By using this pattern description, Specognitor could also successfully detect the three speculative side-channels introduced by [11]. These attacks are all based on a key-dependent branch instruction.

In BTB benchmark, we observe no leakage for PHT-based configurations except for example v09. However, in this example, the leakage detected for PHT-based configurations and BTB-based configurations happen in two different locations.

### Table II: PHT examples

| Benchmarks | w = 16 | w = 32 |
|------------|--------|--------|
| PHT      | PHT-1  | PHT-4  | PHT-1  | PHT-4  |
| v01      | o      | o      | o      | o      |
| v02      | o      | o      | o      | o      |
| v03      | o      | o      | o      | o      |
| v04      | o      | o      | o      | o      |
| v05      | o      | o      | o      | o      |
| v06      | o      | o      | o      | o      |
| v07      | o      | o      | o      | o      |
| v08      | o      | o      | o      | o      |
| v09      | o      | o      | o      | o      |
| v10      | o      | o      | o      | o      |
| v11      | o      | o      | o      | o      |
| v12      | o      | o      | o      | o      |
| v13      | o      | o      | o      | o      |
| v14      | o      | o      | o      | o      |
| v15      | o      | o      | o      | o      |
| v16      | o      | o      | o      | o      |

(* indicates a leakage of BR-LD-LD pattern, (◦) indicates a leakage of LD-BR-LD pattern, and (⋆) indicates no leakage.

### Table III: BTB examples

| Benchmarks | w = 16 | w = 32 |
|------------|--------|--------|
| BTB       | BTB-1  | BTB-4  | BTB-1  | BTB-4  |
| v01      | o      | o      | o      | o      |
| v02      | o      | o      | o      | o      |
| v03      | o      | o      | o      | o      |
| v04      | o      | o      | o      | o      |
| v05      | o      | o      | o      | o      |
| v06      | o      | o      | o      | o      |
| v07      | o      | o      | o      | o      |
| v08      | o      | o      | o      | o      |
| v09      | o      | o      | o      | o      |
| v10      | o      | o      | o      | o      |
| v11      | o      | o      | o      | o      |
| v12      | o      | o      | o      | o      |
| v13      | o      | o      | o      | o      |
| v14      | o      | o      | o      | o      |
| v15      | o      | o      | o      | o      |
| v16      | o      | o      | o      | o      |

(* indicates a leakage of BR-LD-LD pattern, (◦) indicates a leakage of LD-BR-LD pattern, and (⋆) indicates no leakage.

In this code example, for configurations with 1-entry BTB, the leakage happens at line 2 while for other configurations (4-entry BTB and all PHT-based configurations) leakage happens at line 4. The leakage pattern detected at line 4 corresponds to the normal BR-LD-LD. However, the leakage pattern at line 2 is more complex and corresponds to the training of the prediction logic. To expose this leakage, the execution engine executes the instruction at line 2 and since the condition x<(array1_size-1) is true, it takes x+1 as index. By executing this line, the single BTB entry is updated. At line 3, the value of x is changed to a symbolic value (idx). When the execution engine reaches the condition at line 4, it speculatively jumps to the instruction at line 2 and executes it with x+1 index which is symbolic now and might cause information leakage. This example illustrates the importance of using a precise prediction logic and pattern descriptions to detect the root cause of the vulnerability.

Moreover, to address spectre variant 2, we build a small program according to the BTB attacks mounted by Canella et al. [46] to evaluate the effectiveness of Specognitor in detecting Spectre variant 2 attacks. Figure 5 represents the idea behind the example designed for Spectre variant 2. We run Specognitor with different configurations to see whether it can detect the information leakage. Table IV shows the results of our experiment. As can be seen from the Table IV
configurations without BTB are not vulnerable to this variant of spectre attacks. Furthermore, in 1-entry BTB configurations (without PHT), the malicious BTB entry is evicted, therefore these configurations do not expose any information leakage. However, other configurations report vulnerability at line 7 in the code presented in Figure 5.

B. Real World Experiments

In the next step, we designed an experiment in which Specognitor executes the real-world cryptographic programs from libgcrypt library such as hpn-ssh, openssl, Linux-tegra, and libTomCrypt w.r.t. 3 real world processors (Cortex-A53, Cortex-A7, Pentium 4) to address RQ2 and RQ3. We highlight the following results:

- Specognitor could not find any memory access in which the address depends on a secret key in speculative traces except for str2key program. Line 2 of the following code fragment shows the vulnerable code segment of str2key program:

```
1 for (i=0; i<DES_KEY_SZ; i++)
2 (+key)[i]=odd parity((+key)[i]);
```

Our results show that Specognitor reports vulnerability w.r.t. the three processors while executing this code fragment. However, based on the architectural specifications of a processor, the repetitions of line 2 in speculative paths are different. Table V shows the number of detected vulnerabilities according to the configuration.

- According to Table V, the size of speculation window \( \omega \) and the prediction logic both affect the number of vulnerabilities detected on the configurations.

C. Scalability

In this section, we compare the computational cost of Specognitor with KLEESPECTRE [14] and KLEE [8]. To this end, we perform two sets of experiments. For all experiments in this section, we use 10 real-world cryptographic programs from libgcrypt library as the evaluation data set.

- First, to show the efficiency of our tool and its ability to prune infeasible paths (RQ4), we compare the test results to KLEESPECTRE [14], an state-of-the-art speculation-aware symbolic execution engine developed on top of KLEE, but lacks the prediction modeling capability and dynamic pattern detection. To have a meaningful comparison, we use PHT-based configurations of Specognitor since KLEESPECTRE does not implement BTB. We execute each program on KLEE, on KLEESPECTRE with two different speculative execution length (16-32) and on Specognitor with four different configurations, i.e., 1-bit and 4-bit two level branch prediction and two different speculative execution length (16-32). Figure 11 visualize the comparison of the total amount of executed instructions. The experimental results are shown in three groups: i) without speculation, ii) \( \omega = 16 \), and iii) \( \omega = 32 \). As expected, Specognitor removes the infeasible speculative instruction traces. According to the results, Specognitor shrinks the execution space by up to \( \sim 48\% \) for DES program (on average by \( \sim 15\% \) for all programs).

- Second, we compare Specognitor with KLEE symbolic execution engine to assess the computation cost of prediction modeling and symbolic execution (RQ5). Since Specognitor is developed on top of KLEE, the experimental results give us the exact amount of computation cost added to the symbolic execution due to the speculative path exploration and prediction logic. As expected, the speculation modeling of the Specognitor increases the execution time. According to the results shown in Table VI execution time of programs on Specognitor on average takes \( \sim 10x \) more than their execution time on KLEE, for \( \omega = 16 \) (\( \sim 20x \) for \( \omega = 32 \)). However, for 7 out of 10 programs, it takes less than 1 second to execute on KLEE. For examples which require more than 1 second to execute on KLEE (str2key, camellia, and seed), the execution time of Specognitor is on average \( \sim 17\% \) more than KLEE, for \( \omega = 16 \) (\( \sim 22\% \) for \( \omega = 32 \)). This illustrates that Specognitor has a static computation cost due to the monitor and prediction modeling which make it significantly slower for small programs. However, the dynamic computation cost which corresponds to the number of speculative traces explored by the tool and increases by the size of the program is low.

- Table VII shows the number of speculative traces generated for each program on each configuration. It presents a lower-bound on the number of states generated by state-of-the-art tools (No PL), the number of speculative traces generated by Specognitor (with PL), and the number of common speculative traces between them. For PHT-based configurations, Specognitor soundly reduces the number of speculative traces by up to \( \sim 48\% \) for DES program (on average by \( \sim 22\% \) for all programs). Moreover, for BTB-based configurations, only a few common speculative traces exist.

VI. DISCUSSION

Soundness. Specognitor’s pattern detection mechanism is sound w.r.t. the terminology of program analysis for PHT-based configurations. In other words, when Specognitor re-
ports no vulnerability for these configurations, there is no vulnerability as described by the pattern description mechanism w.r.t. the two-level prediction logic. Since Specognitor explores all feasible traces and extends the speculative traces, it does not miss any vulnerability. However, it does not mean that all vulnerabilities reported by Specognitor are reproducible on a real system since we over-approximate the system behavior (e.g., in modeling \( \omega \)) to ensure soundness. Therefore, Specognitor presents an efficient sound over-approximation technique in detecting spectre variant 1 w.r.t. the two-level prediction logic.

**Limitations and Future Work.** Specognitor accepts programs in LLVM bitcode format which results in extensive applications for different instruction sets that is one of the main goals of this work. However, since LLVM language is strongly typed, we cannot exhibit the full capabilities of the BTB. For example, LLVM does not allow jumping in the middle of another function because of function frames. Therefore, in such cases, Specognitor does not generate speculative traces. Thus, Specognitor is not sound for BTB-based configurations; however, it is quite precise and can report the execution traces that were affected by jumping to the middle of another function. This work can be extended to cover other micro-architectural models that correspond to spectre variant 3 and 4 such as Return Stack Buffer (RSB) and Store To Load (STL) dependencies. Another future work is to lift binary information to overcome the limitations of BTB-based configurations.

**VII. Related Work.**

Research in the field of cache side-channels has gained pace in the recent years, especially with the advent of Spectre attacks [2]. We build Specognitor based on symbolic execution. There are some previous attempts that used symbolic execution to address cache side-channel attacks. CacheD [57] is an approach based on symbolic execution which looks at a concrete program trace to find a memory access in which the address depends on a secret. Another future work is to lift binary information to address cache side-channel detection. Spectector [12] provided a security definition called speculative noninterference (SNI). It uses symbolic execution to detect violations of SNI in a program. However, it does not allow any key-dependent branching. In addition, it only analyzes x86 binary programs which limits its applicability to other architectures. KLEESPECTRE [14] extended symbolic execution with cache modeling and speculative execution. It can only detect Bounds Check Bypass (BCB) vulnerabilities, that is a subclass of spectre variant 1 attacks. In addition, it does not consider prediction logic, hence explores infeasible speculative paths and might report false positive vulnerabilities. A recent approach that addressed speculative side-channel detection is SpecSafe [11].

**TABLE VII: Speculative states generated for Libgcrypt benchmark.**

| Libgcrypt | Config. | PHT4-16 | PHT4-16, BTB:8 | BTB:8 |
|-----------|---------|---------|----------------|--------|
| hash      | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| des       | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| strKey    | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| camellia  | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| salsa20   | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| seed      | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| aes       | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| encoder   | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| chacha20  | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |
| ocb3      | No PL   | 0       | 0              | 0      |
|           | with PL | 1       | 1              | 1      |

**Fig. 11:** The number of executed instructions for different Libgcrypt programs on klee, kleespectre, and two different prediction configuration of specognitor, i.e., PHT1, and PHT4. \( \omega = 0 \) presents experimental results of klee. \( \omega = 16 \) and \( \omega = 32 \) presents experimental results of kleespectre and specognitor (PHT1 and PHT4).
This approach introduces CaSym \cite{[58]} to the speculative world. It also improved the security definition proposed by Spectector \cite{[12]} and proposed speculative aware noninterference (SANI). However, it cannot model a precise prediction unit and only detects spectre variant 1 cache side-channels.

VIII. CONCLUSION

In this work, we explained importance of considering prediction logic in detecting vulnerabilities resulting from speculative behavior of programs containing conditional branches and indirect branches/calls. We also proposed dynamically defined patterns to account for existing and future security threats. We built Specognitor that is a novel prediction-aware symbolic execution tool that can model cache behavior, model speculative execution, model prediction logic, and detect vulnerable patterns with a monitor. We showed the effectiveness of these models in detecting leakage in small programs as well as real-world cryptographic benchmarks.

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