Improvement in the peak mobility of silicon metal-oxide-semiconductor field-effect transistors for quantum dots

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Abstract

Recent advances in gate defined semiconductor quantum dots have shown considerable potential for fault tolerant quantum computing in silicon. To assess the quality of any silicon base material for quantum dots, carrier mobility is one of the most essential metrics. Here we report a peak mobility of 1.5 m²/(V s), along with a critical electron density of 2.6×10¹¹ cm⁻², in a commercial silicon wafer by magneto-transport measurements of a series of silicon wafers with different growth types, activation environments and times. By evaluating the Dingle Ratio, we identified the dominant scattering mechanism that limits the mobility is the short-range scattering and the effect of phonon scattering can hardly be observed below 1.5 K. A charge stability diagram of a single quantum dot was also mapped with no visible disturbance caused by disorders, suggesting the high quality of wafers under test. Our results may provide valuable insights into wafer optimization in silicon based quantum computing.
With the rapid development of silicon quantum devices, quantum dots fabricated on silicon have become one of the most promising candidates for quantum computing.\textsuperscript{1} In particular, for nuclear spin-free \textsuperscript{28}Si,\textsuperscript{2} which is abundant in natural silicon, this kind of structure enables high fidelity control of spin qubits by offering long coherence times.\textsuperscript{3-7} The high quality of silicon based material is prerequisite for any implementation of fault-tolerant quantum computing.\textsuperscript{8,9} The quantity of spin qubits is another challenging hurdle in further developments. As silicon metal-oxide-semiconductors are widely used in commercial electronic devices specifically for their stable performance,\textsuperscript{10} leveraging complementary metal-oxide-semiconductor (CMOS) technology to scale up spin-qubit manipulations is attractive. Possible applications in commercial technology of spin qubits have been identified.\textsuperscript{11,12} Therefore, identifying whether commercial silicon wafers are good candidates for quantum devices is worthwhile.

Much of the work on spin qubits in semiconductor quantum dots has been performed on the GaAs/AlGaAs heterostructure 2DEGs with high mobility and low impurity density.\textsuperscript{13,14} Contrastingly, because of the poor interface between Si and SiO\textsubscript{2}, the mobility of 2DEGs in Si MOS is lower than that in GaAs, leading to many obstacles such as the presence of disorders and weak tunability.\textsuperscript{1} Thus, it is important to improve the mobility of MOS devices for silicon spin qubits. There are many factors limiting mobility\textsuperscript{15-17}, and to find out the dominant sources in Si MOS FETs, investigations of magnetotransport in the Hall bars of these structures were performed. By analyzing the mobility ($\mu$) as a function of density ($n$) and quantum life time ($\tau_q$), the dominant source was identified.\textsuperscript{18} These experiments were performed on GaAs/AlGaAs heterostructure,\textsuperscript{19-21} Si MOS FET,\textsuperscript{22} and Si/SiGe heterostructure.\textsuperscript{23-25} On this basis, several means to improve mobility of 2DEGs were found including using strained silicon and annealing samples in N\textsubscript{2} environments.\textsuperscript{26,27} In this Letter, we fabricated silicon metal-oxide-semiconductor(MOS) Hall bars using commercial silicon wafers with different parameter settings, typically comparing growth types, activation environments and times. By studying the magnetotransport, we found the peak mobility can be improved up to 1.5 m\textsuperscript{2}/(V\cdot s) by using both methods of high vacuum annealing during implantation activation and float zone (FZ) growth. Furthermore, we identified the dominant scattering mechanism that limits the mobility is the short-range scattering and the effect of phonon scattering can be ignored below 1.5K. A single quantum dot is also fabricated to identify the possibility of producing quantum dots without many disturbances.
caused by defects.

These devices with Hall bars and quantum dots were fabricated on 8-inch commercial silicon wafers. These kinds of wafers consist of a 10- or 20-nm-thick SiO2 cap formed by thermal oxidation and a 725-μm Si substrate. In fabrication, a standard process was followed for both. The sample preparation is as follows: Regions are ion implanted with a dose of $2 \times 10^{15}$ cm$^{-2}$; the annealing for ion activation is performed at the temperature of 1050°C in either high vacuum ($<10^{-3}$ Pa) or a N$_2$ environment; Ohmic contact regions are formed using buffered oxide etching and successive evaporation of Ti/Au or Al; aluminum oxide is then deposited as an insulator to a thickness of 30 nm at the temperature of 300°C. After that, Ti/Au or Al is deposited above Al$_2$O$_3$ to define the conductive channel. A final annealing with forming gas (15%H$_2$ and 85%N$_2$) at the temperature of 400°C is performed to reduce the defects induced by e-beam lithography and metal evaporation. All measurements were carried out in a dilution refrigerator at a temperature ranging from 0.24 K to 1.5 K.

Channel length $L=300$ μm and width $W=100$ μm are the geometries chosen for Hall bars on the commercial silicon wafers [Fig. 1(a)]. The inset of Fig. 1(b) shows the cross section of the structure. The top gate (faint yellow area) is for applying a DC voltage to accumulate a two-dimensional electron gas (2DEGs) at the Si/SiO$_2$ interface for generating current above a turn-on voltage of $V_t = 1.89$V. The standard ‘turn on’ curve of the current of the 2DEGs were determined in Fig. 1(b).

![Figure 1](image.png)

FIG. 1. (a) Optical micrograph of a Si MOSFET Hall bar showing the ion implantation region (grey areas) with the Ti/Au pads (white squares) and the top gate (faint yellow area) made of Al. (b) Typical current-voltage curve obtained under a source-drain bias of 20 μV. Inset: Cross section of the Si MOSFET.
For mobility improvements, it is important to identify the limitations in our samples. Quantum transport measurements were performed to reveal the scattering mechanism at temperatures $0.24 \, K < T < 4.3 \, K$ using a lock-in amplifier SR830 with the frequency at $\sim 70 \, Hz$. The hall density $n$ of 2DEGs shows a linear increase as a function of the top gate voltage $V_t$ in Fig. 2(a). The classical regime of Hall transport ($0 \, T < B < 1 \, T$) helped us to standardize mobility ($\mu$) and density ($n$) at different top gate voltages. An example of the characteristics of Wafer No.3.4 is presented in Fig. 2(b).

At low density ($n < 6 \times 10^{11} \, cm^{-2}$), the curve follows roughly a $\mu \propto n^3$ trend, corresponding to the effect of fixed charges. The mobility decreases when $n > 1 \times 10^{12} \, cm^{-2}$ because of interface-roughness scattering at the Si/SiO$_2$ interface. The peak mobility reaches $1.5 \, m^2/(V\cdot s)$ at a characteristic density of $9.06 \times 10^{11} \, cm^{-2}$.

At the position of the peak mobility [marked by a yellow star in Fig. 2(b)], various transport measures were studied [Fig. 2(c)] including resistivity $\rho_{xx}$ (along the plateau) and $\rho_{xy}$ (perpendicular to the plateau) for different magnetic field strengths ($B$). The effective magnetic field for Shubnikov-de Haas (SdH) oscillations is $0.7 \, T$. When the magnetic field is above the effective magnetic field, plateaus with even filling factor $\nu = 4, 6, 8, \ldots$ and oscillations are observed. Odd filling-factor plateaus are invisible because of valley degeneracy. In Si MOSFETs, valley splitting energies of $0.7–1.5 \, meV$ were reported. A large valley splitting is beneficial for qubit operations, with no influence on the ground state and the lowest excited state. From Fig. 2(c), the spin-splitting magnetic field $B_s = 3.1 \, T (\nu=10)$ was obtained. A Zeeman splitting energy of $E_z = g \mu_B B_s = 360 \, \mu eV$ is consistent with the Landau-level broadening $\Gamma = \hbar / 2 \tau_q = 410 \, \mu eV$, where $g = 2$ is the electronic Lande factor, $\mu_B$ is the Bohr magneton and $\hbar$ is the reduced Planck constant. The value of $\tau_q = 0.8 \, ps$ is obtained from the Fig. 3(e).

From an analysis of $\rho_{xx}$ ($B=0 \, T$) as a function of density ($n$) and varying the gate voltage ($V_t$), a single line is obtained [Fig. 2(d)]. By changing the temperature, these curves feature a stable crossing point at a critical electron density ($n_c = 2.6 \times 10^{11} \, cm^{-2}$) where the resistivity indicates a transition from metal to insulator behavior. When the density is below $n_c$, resistivity decreases with increasing temperature corresponding to insulating behavior. Contrastingly, the resistivity indicates metal behavior when the density is above $n_c$. This transitional point to a certain extent reflects the impurity...
density. Hence, $n_c$ is an important gauge for the degree of disorder in silicon MOS. When the degree of disorders is sufficiently low that there is no more than one within the size of a quantum dot, detection of single spin events without disturbance is possible.\textsuperscript{36} The value of $n_c$ in MOS FETs is consistent with the value presented.\textsuperscript{34,37}

![Graphs](image-url)

FIG. 2. Typical characteristics of a silicon wafer: (a) Linear relationship between 2DEGs Hall density $n$ and top gate voltages $V_t$. (b) Channel mobility ($\mu$) as a function of density ($n$) measured at different top gate voltages $V_t$. The position of the peak mobility is marked by a yellow star; (c) Longitudinal ($\rho_{xx}$, black) and transverse ($R_{xy}$, blue) resistivity at $n=9.06 \times 10^{11}$ cm$^{-2}$, marked by yellow star in (b); (d) Resistivity $\rho_{xx}$ as a function of density $n$ in the temperature range $T=0.3$–4.3 K.

Fig. 3(a) shows the transport resistivity $\Delta \rho_{xx} = \rho_{xx}(B) - \rho_{xx}(0)$ (denoted by $\Delta \rho$ in the following) as a function of magnetic field $B$ ranging from 0.7 T to 2 T. We can subtract the background of $\rho_{xx}$ and obtain a clear period oscillation in $\Delta \rho$ against $1/B$. Six oscillations against $1/B$ were plotted with different temperature settings. Each line oscillates with a period of 4 in $v$, consistent with the two-fold valley degeneracy and two-fold spin degeneracy. The oscillation in $\Delta \rho$ as a function of
$B$ fits the formula\textsuperscript{38}

$$
\Delta \rho (B) = 4 \rho (0) \cdot \cos \left( \frac{E_F}{\hbar \omega_c} \right) \cdot D (m^*, T) \cdot \exp \left( -\pi / \omega_c \tau_q \right), \tag{1}
$$

where $\rho (0)$ is the longitudinal resistivity at zero magnetic field, $D (m^*, T)$ is the Dingle factor, and at low field $D (m^*, T) = \xi / \sinh \xi$ with $\xi = 2 \pi^2 k_B T / \hbar \omega_c$, $\omega_c = eB / m^*$ is cyclotron frequency, $m^*$ is effective mass, $k_B$ is Boltzmann’s constant, and $\tau_q$ is quantum life time of the electrons.

When $\xi \gg 1$, the extrapolated amplitude for $\Delta \rho$ in Eq. (1) can be deduced to

$$
\ln \left( \frac{\Delta \rho (B)}{T} \right) = C_1 - \frac{2 \pi^2 k_B}{\hbar eB} \cdot m^* \cdot T, \tag{2}
$$

where $C_1$ is a temperature-independent constant. Given the data in Fig. 3(a), $\ln \left( \frac{\Delta \rho (B)}{T} \right)$ as a function of $T$ is fitted with Eq. (2) [see Fig. 3(b)]. The effective mass $m^*$ is derived from the slope of the line for different magnetic fields. The linear relationship varies with magnetic field; nonetheless, the measured $m^*$ is consistent with a constant effective mass, $0.2m_0$, evidencing the reliability of the data.

**FIG. 3.** (a) Fourier spectrum of SdH oscillations with $n = 9.06 \times 10^{11} \text{ cm}^{-2}$ in the temperature range $T = 0.24$–1.5 K, after subtracting the polynomial background. (b) Magnetic-field dependence of the logarithm of $\Delta \rho$ with $T$. (c) Calculated effective mass from the slope of (b) at different magnetic field. (d) Dingle plots for the data shown in (a) for different $T$ settings. (e) Quantum life time $\tau_q$ and transport life time $\tau_t$ as a function of $T$. (f) Dingle Ratio obtained from (e).
A rearrangement of the amplitude of Eq. (1) gives

$$\ln \left( \frac{\Delta \rho(B) \sinh \xi}{\xi} \right) = C_2 - \frac{\pi m^*}{e B \tau_q}$$  \hspace{1cm} (3)$$

where $C_2$ is another temperature-independent constant. Like Fig. 3(b), we plotted $\ln \left( \frac{\Delta \rho(B) \sinh \xi}{\xi} \right)$ as a function of $1/B$ [Fig. 3(d)]; values of $\tau_q$ were extracted from the linear dependence of data. In Fig. 3(e), the transport lifetime $\tau_t$ is obtained from mobility ($\mu$) using $\tau_t = \frac{\mu m^*}{e}$. The quantum lifetime $\tau_q$ and transport lifetime $\tau_t$ were compared as functions of temperature but both show no variation. We note that this differs from previous works on Si/SiGe$^{25}$ and GaAs/AlGaAs$^{21}$ which are temperature dependant. In evaluating the Dingle Ratio $\tau_q / \tau_t$, we identified the dominant scattering mechanism in this sample[Fig.3(f)]. The value of the Dingle Ratio is almost unity and indicates that short-range scattering rather than long-range scattering plays a more important role. This conclusion is consistent with the results of previous work where the fixed charges and defects at the two interfaces between SiO$_2$ and Al$_2$O$_3$ or SiO$_2$ and Si dominate the scattering.$^{39}$ Impurities inside the quantum well also suggest this result. The insensitivity of the Dingle Ratio to temperature implies that phonon effects are not dominant here even if we cannot rule out other effects that limit the mobility of wafers.$^{40}$ To further improve the quality of MOSFET, it is important to overcome the obstacles at the interface.

To investigate further properties of these structures for quantum devices, we fabricated a single quantum dot with Wafer No.2.2. The quantum dot design was based on a double top-gated architecture, similar to previous work conducted on GaAs and Si.$^{41,42}$ Compared with MOSFET devices, a single quantum dot is defined by several gates that confine the potential of the quantum well. The structure of the planar gates is displayed in Fig. 4(a). These gates are fabricated between Al$_2$O$_3$ and SiO$_2$. By detecting the property of the single dot, it provides evidence of the good quality of our devices to some extent. In Fig. 4(b), dozens of tunneling lines are mapped by changing the gate voltage at G3 and G5. These parallel lines show single dot behavior. Moreover, the interval between two proximal lines are gradually larger when lowering the gate voltages, corresponding to the change in the electron number in the dot. Clearly, these lines are not cut off by other lines usually created by disorders. In this regime, no other disturbances are included. This proves that it is possible to fabricate a quantum-dot device without many disorders by following our procedures.
FIG. 4. (a) Scanning electron microscope of a single quantum dot structure with buried oxide on Si MOS heterostructure. G1–G6 are the depleted gates used to define the potential of the quantum well. (b) A charge stability diagram of a single quantum dot monitored via an adjacent quantum point contact (QPC). Each line corresponds to a tunneling event of electrons.

Comparisons of peak mobility of different MOSFETs were made under different conditions; nine of them are listed in Table I. We have compared the peak mobility of wafers grown using the Cz method with those grown by the FZ method. Cz silicon is slightly phosphorus (P+) or boron (B+)-doped having resistivities 20–30 Ω·cm whereas FZ silicon is intrinsic and undoped with a resistivity of around 10 kΩ·cm. In Table I, the first serial number emphasizes the three different batches of fabrication, and the serial number corresponds to the nine different kinds of samples. Each batch of samples has been fabricated with the same parameter settings. After comparing different batches, the first batch has relatively low peak mobility indicating that the properties vary with different wafers even with the same steps in fabrication. It is possible that this variation stems from their industrial manufacturing. For the rest, one notes a trend in that generally the mobility of the 2DEGs fabricated using FZ wafers is higher than that using Cz wafers. We have repeated the process several times under the same conditions. We attribute this trend to fewer donors in FZ wafers than in Cz wafers. For quantum dots in Si MOS, four kinds of charge transitions are usually considered, namely, dopant atoms, E’ centers, P₆ centers, and unintentional quantum dots. Considering dopant atoms, the background doping of Cz wafers and FZ wafers are approximately $10^{14}$ cm⁻³ and $10^{12}$ cm⁻³, respectively. This takes into account the mobility difference between Cz and FZ wafers (Table 1). For FZ wafers, possible effects from dopant atoms is relatively small. For E’ centers, the effect is related to the fixed
charge, typically arising at the interface between Al₂O₃ and SiO₂. This kind of defect is induced by radiation during e-beam evaporation and is usually located further away from the quantum well. Another kind of Pb center is formed by a single dangling bond on silicon.⁴³,⁴⁴ Previous experiments have identified that the most common defects come from the interface between Si and SiO₂.³⁹ The final annealing with H₂ is performed to passivate the Pb centers.⁴⁵ Unintentional quantum dots are formed by strains between different materials, which is not discussed here. More evidence may arise if the component of the atmosphere is quantified to identify which kind of defects eliminates the most.

By comparing the activation step of the same batch, a key aspect in improving mobility is the activation environment. Activation is usually complemented in a N₂ or Ar environment at high temperatures of around 1000°C using peak annealing.⁴⁶,⁴⁷ Here, we introduce a high vacuum environment (<10⁻³ Pa) for annealing, and it is clear that the peak mobility of the 2DEGs fabricated in high vacuum environment is higher than that in nitrogen for the same type of wafer. This could be attributed to the decrease in the component of oxygen after this step as oxygen atoms are more difficult to retain in a high vacuum environment. The peak mobility improvement for the same type of wafer is near half for the third batch, which heightens the quality of our wafers. The peak mobility of the 2DEGs has almost doubled after changing the Cz wafers for FZ wafers and using high vacuum activation.

### TABLE I. Comparison of three batches of samples

| Number & type (Cz) | Activation | Activation times | Peak Mobility(m²/(V·s))/Density(10¹²/cm²) |
|-------------------|------------|-----------------|------------------------------------------|
| 1.1               | N₂         | 1               | 0.48/1.5                                 |
| 1.2               | N₂         | 2               | 0.48/1.5                                 |
| 1.3               | N₂         | 1               | 0.48/1.5                                 |
| 2.1               | N₂         | 1               | 0.70/1.5                                 |
| 2.2               | High vacuum| 1               | 0.88/1.5                                 |
| 3.1               | N₂         | 1               | 0.80/3                                   |
| 3.2               | N₂         | 1               | 1.00/2                                   |
| 3.3               | High vacuum| 1               | 1.20/1.5                                 |
| 3.4               | High vacuum| 1               | 1.50/1                                   |

In conclusion, we investigated the quantum transport characterization of silicon metal-oxide-
semiconductor (MOS) Hall-bars using commercial silicon wafers with different parameter settings, typically comparing growth types, activation environments and times. We obtained a peak mobility of 1.5 m²/(V·s), along with a critical electron density of 2.6×10¹¹ cm⁻², by using both methods of high vacuum annealing during implantation activation and wafers growth by float zone (FZ) method. In evaluating the Dingle Ratio, we identified the dominant scattering mechanism that limits the mobility is the short-range scattering and the effect of phonon scattering can hardly be observed below 1.5 K. We also fabricated a single quantum dot with a clear charge stability diagram without no visible disturbance caused by disorders to prove that the wafers are of high quality with our results. More efforts are needed to handle residual impurities and defects at the interface between Si and SiO₂. Our results may provide valuable insights into wafer optimization in silicon based quantum computing.

Acknowledgements

This work was supported by the National Key Research and Development Program of China (Grant No.2016YFA0301700), the National Natural Science Foundation of China (Grants No. 61674132, 11674300, 11575172, and 11625419), the Strategic Priority Research Program of the CAS (Grant Nos. XDB24030601), the Anhui initiative in Quantum information Technologies (Grants No. AHY080000) and this work was partially carried out at the USTC Center for Micro and Nanoscale Research and Fabrication.

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