The Research on SAR ADC Integrated Circuit

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Abstract. Successive approximation ADCs are widely used in low- and medium-speed applications due to their simpler structure, fewer analog blocks, smaller area, and lower power consumption. The successive approximation ADC mainly includes a sample and hold circuit, a DAC, a comparator, a clock circuit, and a SAR register. The rationality is verified by analyzing, designing and simulating each component circuit. For the research of ADC architecture, SAR type is selected and the key circuit is optimized. Using Cadence layout research, the digital part of ADC circuit can be simulated by Quartus II software and Modelsim software, and the hybrid circuit part is simulated by Candance software PSpice A/D. About layout design, some circuits can be further verified with Proteus software.

1. Introduction
Integrated circuit (IC), which is experienced a semiconductor manufacturing process such as oxidation, photolithography, diffusion, epitaxy, and aluminum evaporation. It contains a semiconductor, a resistor, a capacitor required for a circuit having a certain function. The connecting wires are all integrated on a small piece of silicon and then soldered to the electronics housed in a package. Early ADCs used the bipolar process, which was relatively expensive and consumes a lot of power. ADCs fabricated in CMOS processes are now the most popular design. With the development of CMOS technology, the medium and high speed ADC is realized by CMOS technology. ADC integrated circuit parameters are mainly speed, accuracy and power consumption, which are generally measured internationally by power consumption, resolution and sampling rate. The research of ADC integrated circuits is mainly in structural improvement, critical circuit design and digital calibration technology.

The ADC integrated circuit is divided into an integral type, which converts the input voltage into a pulse width signal or a pulse frequency in the time domain, and then obtains a digital value through a timer/counter. The advantage is that the resolution is high up to 22 bits, the power is low, and the cost is low. The disadvantage is that conversion rate is low and the conversion rate is 100~300SPS at 12 bits. The successive comparison type is internally composed of a comparator and a digital-to-analog converter by successive comparison logic. Starting from the highest bit, the input voltage is compared with the output of the built-in digital-to-analog converter for each bit in sequence, and is obtained output value by n comparisons. The advantage is that when the resolution is lower than 12 bits, the price is lower, the sampling rate is up to 1MSPS, and the power is very low compared with other ADCs. The disadvantage is that when the resolution is higher than 14 bits, the price will become more high, and the signal generated by the sensor needs to be conditioned before AD conversion, which cannot be directly converted and increases the cost. The parallel comparison type/serial parallel comparison type is because the conversion rate is extremely high, and the n-bit conversion requires 2n-1 comparators, resulting in a large circuit scale and high price; the advantage is that the ADC speed...
is the highest; the disadvantage is that the resolution is not high, the work is not high. It is expensive and costly. Σ-type is composed of integrator, comparator, 1-bit DA converter and digital filter; the advantage is that the price of high-speed Σ-Δ ADC is higher, under the condition of the same conversion rate, the integral type and successive approximation type ADC power consumption is high. The pipelined ADC is internally composed of several cascaded circuits, each of which contains a sample and hold amplifier. A low resolution ADC and DAC also has a summing circuit; the advantage is better linearity and low offset, low power consumption, high precision, high resolution; the disadvantage is that the ADCs reference circuit and bias structure are more complex, the input signal needs to be processed, and cannot be directly converted. The frequency-frequency conversion type first converts the input signal into a frequency and converts the frequency into a digital quantity by using a counter; the advantage is high precision, low price, and low power consumption; the disadvantage is that the conversion rate is limited, and the bit rate is 100–300 SPS. The quality factor (FOM) of a 12-bit 20MS/s pipelined ADC using a 0.35 3.3V CMOS process can be reduced to 0.96pJ/step, which is close to BiCMOS process performance[1]. The quality factor of a 14-bit 100MS/s pipelined ADC using a 0.18 3V CMOS process is 0.69 pJ/step[2]. The quality factor (FOM) of a 12-bit 20MS/s pipelined ADC using a 0.35 3.3V CMOS process can be reduced to 0.96pJ/step, which is close to BiCMOS process performance[1]. Gambini proposes a SAR-type A/D converter based on a 90nm CMOS process for wireless sensors that can operate at a low voltage of 0.5V and consumes only 7[3]. Yoshioka et al. designed a 10-bit SAR-type AD converter with calibration. At 1.0V operating voltage, the sampling rate of 50MS/s consumes 820, of which DNL<0.82LSB, INL<0.72LSB[4].

Pipelined ADCs have a good compromise between speed, power, accuracy, and area, leaving design engineers with large optimization space[5], but high-performance pipelined ADCs require high-gain, high-bandwidth op amps. It is very difficult to implement high-performance operational amplifiers based on nano-scale CMOS technology, and successive approximation ADCs are widely used in low- and medium-speed applications due to their simpler structure, smaller analog blocks, smaller area, and lower power consumption[6]. Therefore, the SAR (Successive Approximation)-based ADC is very suitable for the performance requirements of portable electronic products, and has a good development prospect.

In this paper, the SAR type is selected for the research of ADC architecture, and the key circuits are optimized. With Cadence layout research, the results of layout design must comply with the constraints of manufacturing process, timing, area, power consumption and so on. Design Rule Check (DRC) corrects and verifies that the layout of the layout conforms to the design specifications, but DRC cannot guarantee that the line will still maintain the designer's expectations if the layout is fully compliant with the design specifications, while LVS is the most The right solution. The Layout Versus Schematic (LVS) tool generates a netlist by identifying and reading the various graphics and connections that represent the electronic components in the layout, and then comparing it to the original design/circuit diagram netlist. The international standard of ADC signal integrated circuit test adopts IEEE1149.4 standard test[7]. The test time is short, the error is small, the accuracy is high, the data can be repeated, and the test is automatic. Due to the simple operation, small size and low power consumption, it is widely used in the industry. The serial shift register controls the CMOS transmission gates connected to the analog bus and controls the surrounding digital logic functions. The DFT technology proposed for mixed-signal functions is serial digital access[8]. The digital part of the ADC circuit can be simulated by Quartus II software and Modelsim software, and the hybrid circuit part is simulated by Candance software and layout design.

2. Successive approximation ADC

The successive approximation ADC repeatedly compares the input signal with the reference voltage, gradually finds the voltage interval corresponding to the analog input voltage from coarse to fine, and finally outputs the corresponding digital code. It has a relatively simple main structure and can achieve lower power consumption.
In order to improve the common mode noise suppression capability and conversion accuracy, the AD converter usually uses a differential structure.

Working process: The first comparison cycle, $V_{IP}$ is greater than $V_{IN}$, so $D1=1$, while $V_{IP}$ and $V_{IN}$ are respectively shifted to $1/4 V_{REF}$ to the common mode level; in the second cycle, $V_{IP}$ is still greater than $V_{IN}$, so $D2=1$, and $V_{IP}$ and $V_{IN}$ shift $1/8 V_{REF}$ down and up respectively; in the third cycle, $V_{IP}$ is less than $V_{IN}$, so $D3=0$, then $V_{IP}$ shifts up $1/16 V_{REF}$ up, and $V_{IN}$ shifts down $1/16 V_{REF}$; this process repeats until the whole conversion is complete.

The successive approximation ADC mainly includes a sample and hold circuit, a DAC circuit, a comparator, a clock circuit, and a SAR register.

2.1. DAC circuit

When sampling, the lower plate of all capacitors is connected to $V_{IN}$, and the upper plate is connected to $V_{CM}$. At this time, the charge stored in the upper plate is

$$Q=Q_{total}(V_{CM}-V_{IN}),$$

where $Q_{total}=2^{N}C$.

The lower plate of all capacitors is grounded when it is held, and the upper plate is disconnected from the common mode level $V_{CM}$. At this time, the voltage of the upper plate is

$$V=V_{CM}-V_{IN}.$$

In the charge redistribution, first, the lower plate of the highest-position capacitor is connected to the reference voltage $V_{REF}$, and the lower plates of the other capacitors are still grounded, and the charge of the upper plate is conserved.

$$2^{N-1}C(V_{CM}-V_{IN})=2^{N-1}C(V_{REF})+2^{N-1}C, V$$

That is,

$$V=V_{CM}-V_{IN}+\frac{1}{2}V_{REF}$$

The comparator determines the MSB by comparing the sizes of $V_{CM}$ and $V$. If $V_{IN}>1/2V_{REF}$, i.e
V < \text{V}_{\text{CM}}$, the comparator output is 1 and MSB is 1; otherwise, if \( V_{\text{IN}} < \frac{1}{2}V_{\text{REF}} \), \( V > \text{V}_{\text{CM}} \), the comparator output is 0 and MSB is 0. Then, the second highest level capacitor is grounded in turn, and the voltage \( V \) is increased by \( \frac{1}{4}V_{\text{REF}} \) by the principle of conservation of charge. According to the result of the comparator, the second highest bit is 1 or 0. If the bit is 1, the capacitance remains unchanged, otherwise the Bit 0, the next highest level capacitor is re-grounded. And so on, until the minimum is (LSB) determined, the entire conversion is over. As the conversion process \( V \) eventually approaches \( \text{V}_{\text{CM}} \), depending on the comparator output, \( V \) can be expressed as

\[
V = \text{V}_{\text{CM}} - V_{\text{IN}} + \frac{1}{\sum_{i=1}^{N} b_i C_i C_{\text{total}} V_{\text{REF}}}
\]

Then the digital output \( D = [b_{N-1}, b_{N-2}, \cdots, b_1] \).

2.2. SAR logic circuit research

The circuit is shown in Figure 4. The circuit consists of a flip-flop. When the clock cycles to 0, the EN signal is high. At this time, all the flip-flop outputs are reset to 0, and EN is low when the other clock cycles. The cyclic clock action trigger is calculated by the MSB to calculate the associated digital output of \( D_4, D_3, D_2, D_1, D_0 \) based on the output of the comparator.

In order to reduce the number of registers, a non-redundant SAR logic is proposed. For an \( N \)-bit SAR AD converter, only \( N \) registers are needed. The register has three functions: shift, input data, and storage. When starting the ADC cycle, assume that the MSB of the digital output is 1, and the other bits are 0. The SAR logic determines the digital output of the MSB based on the comparison result of the comparator. If the output of the comparison circuit is 1, the MSB digital output does not change. If the output of the comparison circuit is 0, the MSB digital output becomes 0.6 clocks required to complete a 5-bit SAR ADC.

3. Low-Power CMOS Successive Approximation Analog-to-Digital Converter

3.1. CMOS latch type comparator
At reset, Clk is low, the S1 transistor is turned off, and the comparator outputs Out+ and Out- are reset to V\text{DD} through reset transistors S7 and S10. During regeneration, Clk is high, the S1 tube is turned on, and the input of the comparator begins to discharge the D node at different discharge rates. Once the voltage of one of the nodes drops to V\text{DD}-V\text{TN}, the NMOS transistor of the cross-coupled inverter begins to conduct, but begins to discharge the output node Out, the comparator enters the positive feedback phase, and when the voltage of the output node drops to V\text{DD}-|V\text{TP}|, the PMOS transistor of the cross-coupled inverter begins to conduct, eventually pulling one output up to V\text{DD} through positive feedback and the other output going down to ground. This type of CMOS comparator has the advantages of high speed and low power consumption, but it also produces large input offset voltage and noise\[7\].

### 3.2. Two-tailed current type dynamic latch comparator

In order to overcome the shortcomings of CMOS latched comparator offset with common mode voltage variation and unsuitable for low voltage applications, a two-tailed current type dynamic comparator is proposed. This architecture maintains a relatively stable offset voltage over a wide range of common-mode levels while also operating at lower supply voltages. At reset, Clk is low, PMOS transistors S4 and S5 precharge the first stage output D to V\text{DD}, while the second stage output node Out is reset to ground, while the tail current transistors S1 and S12 of the input and output stages are off broken. When Clk is high, the tail current tube of the input stage is turned on, and the output node D\text{a} starts to discharge from V\text{DD}. The discharge speed also differs due to the difference of the input voltage.
4. Performance test of SAR ADC

4.1. Offset error
The offset error of the ADC refers to the amount of the first conversion level of the actual quantization curve deviating from the ideal characteristic curve. The 8-bit SAR ADC with the operating voltage of 1.0V in Fig. 8 has an offset error of 6mV.

\[ n = \frac{6}{(1/256)} = 1.5(\text{LSB}) \]

It can be seen from Fig. 8 that the offset error of 6mV is equivalent to the error of 1.5LSB, and the offset error is eliminated by subtracting 1.5LSB for each conversion process, so the actual full-scale value is 1Vx (254.5/256)=0.994V.

4.2. Gain error
Gain error is the deviation of the slope of the actual quantization curve of the ADC from the slope of the ideal characteristic curve. As shown in Fig. 9, the gain error reflects the error of the linear slope of the transmission characteristic. Similar to the offset error, the presence of a gain error can cause the digital code to not be fully output when the input is full scale, resulting in a reduced dynamic range of the ADC.

4.3. SAR control logic test
The successive compare register control logic sequentially controls the signal output of each bit. The SAR control logic sequentially determines the value of each digital bit based on the output of the comparison circuit. The ring counter and the shift register constitute the control logic and operation timing of the 5-bit SAR type ADC. According to the circuit of FIG. 4, the test result is as shown in FIG. 10.
5. Conclusion
The ADC is used on many integrated chips and integrated into the integrated chip. This paper proposes an improved method for the integrated circuit of the ADC, which is helpful for the construction of the test channel, and provides theoretical and verification basis for the research of the later ADC integrated circuit test channel. As the number of ADCs increases, the simulation test becomes more and more difficult. The research further expands. Through analysis, the CMOS-level circuit can be designed and simulated with Quartus II software. The standard structure of CMOS-level SAR ADC is found to lay the foundation for the test channel construction. The logic structure of SAR ADC is built by MATLAB software to verify its feasibility. The AD simulation verification function of Candance software is used to further improve the performance and design the test channel publishing map. The Proteus software was used to verify and verify the auxiliary functions, which further deepened the research content.

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