Compilation and scaling strategies for a silicon quantum processor with sparse two-dimensional connectivity

O. Crawford, J. R. Cruise, N. Mertig and M. F. Gonzalez-Zalba

Riverlane, Cambridge, United Kingdom

Hitachi Cambridge Laboratory, J. J. Thomson Ave., Cambridge, CB3 0HE, United Kingdom

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Inspired by the challenge of scaling up existing silicon quantum hardware, we investigate compilation strategies for sparsely-connected 2d qubit arrangements and propose a spin-qubit architecture with minimal compilation overhead. Our architecture is based on silicon nanowire split-gate transistors which can form finite 1d chains of spin-qubits and allow the execution of two-qubit operations such as SWAP gates among neighbors. Adding to this, we describe a novel silicon junction which can couple up to four nanowires into 2d arrangements via spin shuttling and SWAP operations. Given these hardware elements, we propose a modular sparse 2d spin-qubit architecture with unit cells consisting of diagonally-oriented squares with nanowires along the edges and junctions on the corners. We show that this architecture allows for compilation strategies which outperform the best-in-class compilation strategy for 1d chains, not only asymptotically, but also down to the minimal structure of a single square. The proposed architecture exhibits favorable scaling properties which allow for balancing the trade-off between compilation overhead and colocation of classical control electronics within each square by adjusting the length of the nanowires. An appealing feature of the proposed architecture is its manufacturability using complementary-metal-oxide-semiconductor (CMOS) fabrication processes. Finally, we note that our compilation strategies, while being inspired by spin-qubits, are equally valid for any other quantum processor with sparse 2d connectivity.}

INTRODUCTION

Qubit connectivity is a primary feature of any quantum computing technology. It represents the architectural arrangement of the qubits within the quantum processor and indicates the number of qubits with which any other qubit can interact. Highly-connected structures are favorable since two-qubit gates between arbitrary qubits require a smaller gate count and hence more complex problems can be solved with lower circuit depth. On the other hand, high qubit connectivity comes at the expense of technological complexity. Therefore, scaling while maintaining high-connectivity is a challenge being faced by many quantum computing technologies. All-to-all connectivity has been demonstrated by photonic [1] as well as ion-trap [2] qubits, but the distributed nature of these technologies puts serious challenges on the path to scaling. On the other hand, solid-state systems, such as superconducting [4] and quantum-dot spin qubits [5], can exhibit 2d hardware topologies, which could be compactly integrated on a chip. This allows for colocating classical support electronics and offers an alternative path to scaling.

Implementations of 2d grids with nearest neighbor connectivity are desirable as this would allow for fault-tolerant quantum computing via the surface code [6] without additional gate overhead. However, scaling 2d nearest neighbor grids in solid-state systems poses substantial contact routing challenges and complicates the integration of classical support electronics in the qubit plane [7] [8]. Quantum-classical integration would require levels of 3d integration unseen to date [9]. Therefore, solid-state platforms explore scaling with sparse 2d connectivity [10] [12] and several works have explored optimized methods for running quantum algorithms on sparsely-connected hardware graphs [13] [15].

Particularly for the spin qubits, progress has been made in the last few years demonstrating high-fidelity gates [16] [17] and readout [18] [19] beyond the fault-tolerance threshold [5] [20] [21]. Further, the first few qubit processors [22] [23] and blueprints [9] [10] [24] [25] are beginning to emerge. Next steps will be focused towards scale-up, for which the use of industrial complementary metal-oxide-semiconductor (CMOS) processes is expected to play an important role [8] [9]. In particular, modules containing industry-manufactured bilinear arrays of quantum dots (QDs) using split-gate nanowire transistor technology are readily manufactured and their qubit properties are widely being tested in experiments [20] [29]. These modules should provide a platform to demonstrate a 1d quantum processor in silicon which should allow for running early noisy intermediate-scale quantum (NISQ) algorithms [13] [30], Shor’s algorithm [31] or demonstrating logical qubits [32]. How best scale this technology to allow for optimized operation of quantum algorithms with minimal compilation overhead is therefore an important question.

Here, we present a concept to utilize and scale QD chains of 1d split-gate transistors by combining them into 2d arrays with sparse connectivity. For this purpose, we introduce a new hardware junction which enables coupling between horizontally and vertically oriented arrays of split-gate transistors via spin shuttling [33]. Given these hardware elements, we propose a modular 2d spin-
qubit architecture with unit cells consisting of diagonally-oriented squares where nanowires form the edges and junctions the corners of a square. We then investigate compilation strategies for the proposed 2d architecture and demonstrate a square-root scaling of the compilation overhead, which outperforms the linear overhead of 1d devices, not only asymptotically, but also down to its smallest building block which is likely to be investigated first in future experiments. This allows for balancing the trade-off between compilation overhead and creating space in between the qubit modules which can be beneficial for colocation of classical control and readout electronics [10, 34, 35] and alleviating contact routing issues [9, 24, 36, 37]. Overall, this proposal should provide a compelling path to scaling, which could be manufactured with industrial CMOS processes.

RESULTS

Topology of the proposed architecture

We start by introducing the hardware topology of the proposed architecture, before describing the detailed embodiment in silicon and discussing compilation strategies in subsequent sections. The core element of the architecture is a bilinear array of QDs using CMOS split-gate nanowire transistors. This gives rise to a 1d arrangement of m qubits along a line, in which neighboring qubits can be involved in two-qubit operations as visualized in Fig. 1(a), where the m = 4 dots indicate qubits and the black lines indicate possible two-qubit operations among neighbors. An additional building block is provided by a junction element which can join up to four linear segments in a perpendicular manner, as depicted in Fig. 1(b). In principle, a two-qubit operation can be executed between any two qubits involved in the junction as indicated by an orange line connecting the qubits. As explained in more detail in the following section, each two-qubit operation across the junction requires 6 additional spin shuttling steps. We consider the regime in which these coherent shuttling steps are fast, invoking negligible overhead as compared to the two-qubit operation. We note that each qubit can only be involved in a single two-qubit operation at a time.

The unit cell of the proposed architecture is then provided by squares, with linear segments along the edges and junctions at the corners of each square, as in Fig. 1(c). To form the complete architecture, we join dx squares in one direction and dy in the perpendicular direction. For convenience, we define the two directions as x and y. The complete architecture and x and y directions are show in Fig. 1(d). Since each square contains 4m qubits and the device consists of dx dy squares, each device contains

\[ N = 4md_xd_y \] (1)

qubits. We note that a crucial feature of the proposed architecture is the tilted orientation of squares at an angle of 45° in each unit cell, which minimizes the compilation overhead as will be explained later on.

Architecture embodiment in silicon

In the following, we introduce the embodiment of the proposed architecture in silicon and the corresponding control schemes in more detail. We focus on an implementation based on electron spins hosted in gate-defined QDs, but note that a similar proposal can be described for hole spin qubits. Readers interested only in the compilation techniques are advised to skip ahead.

Split-gate submodules The principal building block of our proposal is the split-gate transistor [28, 38–40]. It consists of an undoped silicon-on-insulator nanowire of height h and width w (typically 10 nm and 60 nm, respectively). The central part of the nanowire is gated by two metallic surface electrodes of length lg (typically 40-60 nm) which are isolated from the channel by the gate oxide (SiO2) of thickness t (typically 6 nm); see Fig. 2(a). The gate stack is typically formed by 5 nm of TiN followed by 50 nm of polycrystalline silicon. The rectan-
FIG. 2: Split gate submodules. (a) Top view of a single split-gate nanowire transistor, with highly-doped source and drain ohmic contacts in blue, metallic split gates in orange, Si$_3$N$_4$ spacer in green and buried oxide in black. (b) Schematic cross section of the split-gate transistor along the dashed line in panel (a). The gates and silicon nanowire are isolated by the gate oxide. The blue arrowed spheres represent schematically the location of the spins. The vertical arrows represent the magnetic field lines. (c) An 8 split-gate 1d submodule. We highlight a 2 × 2 subset. (d) Energy spectrum versus energy detuning of the two-spin system in a tunnel-coupled DQD. Both energy and detuning are normalized by the $|\uparrow\downarrow\rangle$-|S(20)$⟩$ tunnel coupling, $t_s$. The diagram is simulated using a 5% $g$-factor difference and an average Zeeman energy of three times $t_s$. (e-i) Operation of a 2 × 2 QD subset. Initialization (e-f), one-qubit gates (g), two-qubit exchange interaction (h) and readout via Pauli spin blockade (i).

A cross-section of the channel, as seen in Fig. 2(b), is covered by the pair of split gates which are separated by a face-to-face distance $S_{gg}$ ($\approx 30$ nm) and enable local electrostatic control of the nanowire. At deep cryogenic temperatures, when positive voltages are applied to the gates, few-electron QDs form in the top-most corners of the device due to the corner effect [41–43], as shown in Fig. 2(b). Charges can be drawn into the QDs from charge reservoirs formed of highly-doped silicon located at each side of the split gate.

The qubit that we consider here is the spin of a single electron (or hole) confined to one of the two corner dots in each split-gate transistor. The other spin is used as an ancilla for readout as described later on. To define the spin quantization axis, the structure is placed in a magnetic field. The architecture can be scaled-up by fabricating a series of split-gate transistors placed along the axis of the silicon nanowire, as depicted in Fig. 2(c). The split-gate edge-to-edge separation $S_{ev}$ ($\approx 40-60$ nm) is set to enable sizable exchange coupling between spins, which we use to generate two-qubit interactions. Overall, the module results in a bilinear array of QDs. Given that the two QDs of each split-gate transistor encode one qubit – one dot contains a qubit spin and the other an ancilla spin for readout – the structure embodies a one-dimensional chain of silicon spin qubits of length $m$, as described in the previous section.

Next, we explain control, readout and initialization of the 1d modules in detail. We base our explanation on the energy spectrum of the coupled two-spin system in the single spin basis as a function of the QD energy detuning, $\epsilon$, and a finite magnetic field; see Fig. 2(d). At large positive detuning with respect to the (11)-(20) charge hybridization point, the ground state of the system corresponds to the intradot singlet, |S(20)$⟩$. Here the (nm) notation refers to the charge distribution among the two QDs, i.e. dots are occupied with $n$ and $m$ charges, respectively. At negative detuning, the ground state of the system is the (11) charge configuration whose spin degeneracy is broken by the external magnetic field. We consider the QDs have a tunnel coupling energy $t_s$ and present different $g$-factors due to the variability of the Si/SiO$_2$ interface [44], which further breaks the degeneracy of the $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ states. Here, the first spin refers to the spin with the lower $g$-factor (see the Hamiltonian in Appendix A). Although not strictly necessary for the operation of the processor, we consider that larger Zeeman energy differences exist across the nanowire than along the nanowire, which could be achieved by creating an asymmetry in the gate structure. Using magnetic materials on the gate stack on one side of the split or placing the splits offset with respect to the nanowire axis [45] may produce a difference in the Meissner effect at the location of the QDs. We use the energy spectrum to describe processes involving QDs within a split-gate and QDs on the same corner of the nanowire in different splits.

**Initialization** We start with the 1d module loaded with one charge in each QD. Charges can be drawn in from reservoirs at the periphery following established methods [45]. To initialize to a known spin state, QDs...
in each split gate are positively detuned until the system relaxes to the \(|S(20)\rangle\) state (Fig. 2(e)). Then, the system is pulsed towards negative detuning adiabatically with respect to the \(|\uparrow\downarrow\rangle\) state (Fig. 2(f)). To detect this tunneling process, we suggest using dispersive readout [59]. One of the split gates is connected to a lumped-element electrical resonator which is driven at its natural frequency, \(f_0\). At \(\epsilon = 0\), cyclic tunneling between the \(|\uparrow\downarrow\rangle\) and \(|S(20)\rangle\) states (Fig. 2(d)), driven by the oscillatory resonator voltage, manifests in an additional quantum capacitance that loads the resonator producing a spin-dependent frequency shift that can be readily detected with standard methods [60–64].

**Junctions** Next, we propose a new hardware junction which allows for coupling 1d submodules of split-gate transistors. The junction consists of etched silicon-on-insulator in quadrangular form, as can be seen in the central region of Fig. 3(a). The exact shape of the junction can vary to accommodate different levels of interconnection. Here, we present a square junction that enables connecting up to four submodules at an angle of 90°, 180°, or 270°. On top of the junction, we place a series of metallic gates with the same stack as the split-gate transistors. We propose a five-gate structure arranged in cross geometry – one central square gate flanked by four square gates of the same footprint. The characteristic dimensions of the junction are indicated in Fig. 3(b), with submodule-to-edge-gate separation in the \(x′(y′)\) directions \(L_q (\approx 40 \text{ nm})\), the gate length in the \(x′(y′)\) directions \(L_1 (\approx 80 \text{ nm})\), and a junction gate-to-gate separation \(L_d (\approx 40 \text{ nm})\). The junction is invariant under rotations by 90°.

The purpose of the junction is to create a shuttling path for electrons [33] at the edges of the 1d submodules to be moved around the junction in the \(x′\) and \(y′\) directions. Using the appropriate gate voltages sequence. These electrons can be moved to be in exchange coupling proximity with the electrons at the edge of another submodule where a two-qubit gate will be performed. We illustrate the operation of the junction using an \(x′y′\) coupling example in Fig. 3(c): (i) Shuttle the electron under the top-rightmost gate in the left module \(x′\), to the left gate in the junction by applying a differential voltage between the two gates [33]. (ii) Shuttle from the left gate to the central gate of the junction. (iii) Shuttle from the central gate to the bottom gate of the junction. (iv) Implement a two-qubit gate between the electron under the bottom gate in the junction and the electron under the left-topmost gate in the \(y′\) module, as described above. (v-vii) Shuttle the electron back following the reverse process. Finally, the abstracted hardware topology and the same shuttling sequence are presented in Fig. 3(d).

**Readout** Spin readout is based on spin-dependent tunneling from the \((11)\) to the \((20)\) charge configurations, i.e. Pauli spin blockade [57]. More particularly, the state \(|\uparrow\downarrow\rangle\) is allowed to tunnel to the \(|S(20)\rangle\) state, whereas all remaining two particle spins states are blocked [58]; see Fig. 2(d) and (i).
QDs which have been demonstrated \cite{5, 20, 48, 55}. We consider the regime in which spin shuttling operations are performed coherently and much faster than the two-qubit operation in step (iv). In this case, the overhead is negligible and we use the simplified hardware topology given in Fig. 3(e). See Appendix B for a discussion of the different overhead regimes.

Compilation methods

We now present compilation methods for deploying quantum algorithms on the proposed architecture, following standard approaches. We assume that algorithms are given by a quantum circuit which consists of initialization, followed by a sequence of one- and two-qubit operations, and readout, suitable for execution on a fully-connected device. While most of these operations are readily available on the proposed architecture, the sparse connectivity will prohibit execution of two-qubit gates between arbitrary pairs of qubits that are not directly connected by an edge of the hardware graph. To address this issue, compilation methods re-express a given quantum circuit through an equivalent circuit readily amenable to the sparse hardware topology. More specifically, before executing a given two-qubit gate, one generally applies a sequence of SWAP gates to shuttle the relevant qubits along the hardware graph until they reach neighboring positions. Once neighboring positions are reached, the two-qubit gate is executed and the sequence of SWAP gates is reverted to promote the relevant qubits back to their original position. In applying this compilation strategy, the resulting quantum circuit accumulates a compilation overhead characterized by the number of additional SWAP gates, $N_{\text{SWAP}}$, and the increased circuit depth, $N_d$. Both quantities represent important quality metrics for the compilation which should be minimized to avoid additional decoherence and infidelities introduced through the additional SWAP gates. We note that the proposed architecture uses two $\sqrt{\text{SWAP}}$ gates to implement the SWAP operation.

In what follows, we focus on two major compilation scenarios: (I) The case of moving two arbitrary qubits together along the hardware graph. This covers the general case where each two-qubit operation is addressed individually and usually gives reasonable estimates for the compilation overhead. (II) The case of rearranging qubits in an arbitrary permutation. This compilation method is useful for variational algorithms \cite{66} from chemistry \cite{67, 68} and finance \cite{69} which repeatedly execute some number of up to $|N/2|$ two-qubit operations in parallel. For such algorithms, the compilation must efficiently permute qubits into configurations which allow for executing the relevant two-qubit operations in parallel, even on the sparse hardware topology. To implement such permutations efficiently, one repeatedly applies a layer of SWAP operations during which up to $[N/2]$ SWAP gates are executed in parallel. Ultimately, this results in significantly lower circuit depth and reduced gate count than simply addressing each two-qubit operation individually.

Finally, we compare our compilation methods to two important limiting cases – a 1d device which could be fabricated by joining nanowire submodules along one dimension, as depicted in Fig. 4(a), and a 2d rectangular device consisting of $L_x$ by $L_y$ qubits with nearest-neighbor connectivity, as depicted in Fig. 4(b).

Case I – Moving two qubits together along the shortest path

Algorithm The compilation method for case I requires iterating over all two-qubit operations of a given input circuit and, for each pair of qubits involved in a two-qubit operation, (a) determining the shortest path connecting the two qubits and subsequently (b) executing SWAP gates to connect the qubits along the shortest path, executing the two-qubit operation and shuttling qubits back to their original position. Finding the shortest path, i.e., the distance, between a pair of qubits can efficiently be implemented in polynomial time using, e.g., Dijkstra’s algorithm \cite{70}.
The compilation overhead of this algorithm is determined by the length of the shortest path, \( l \), connecting the pair of qubits involved in each two-qubit operation along the hardware graph. In particular, the overhead of SWAP gates accumulated per two-qubit gate is given by \( N_{SWAP} = l - 1 \) while the increased circuit depth per two-qubit operation will be given by \( N_{d} = \left\lceil \frac{l}{2} \right\rceil \), assuming that SWAP gates on different pairs of qubits can be applied simultaneously.

**Device specific overhead** To compare further the compilation overhead for different devices, we compute the average \( \bar{l} \) and maximal \( l_{\text{max}} \) distances between qubit pairs in a given topology. For the linear layout with \( N \) qubits, we have

\[
\bar{l}_{\text{lin}} = \frac{1}{3}(N + 1), \quad l_{\text{lin}, \text{max}} = N - 1. \tag{2}
\]

For a rectangular grid of \( l_x \) by \( l_y \) qubits, we find that \( l_{\text{rec}} = \frac{1}{2}(l_x + l_y) \) and \( l_{\text{rec}, \text{max}} = l_x + l_y - 2 \) and specifically for the square grid with \( l_x = l_y = \sqrt{N} \) we have

\[
\bar{l}_{\text{rec}} = \frac{2}{3}\sqrt{N}, \quad l_{\text{rec}, \text{max}} = 2(\sqrt{N} - 1). \tag{3}
\]

Finally, considering the proposed architecture for \( d_x = d_y \), the average and maximal qubit distances are

\[
\bar{l}_{\text{2d}} = \frac{1}{45(N - 1)} \sqrt{\frac{m}{N}} \left[ 21N^2 + 5 \left( m + \frac{2}{m} \right) N - 15 \left( \sqrt{m^3} + \frac{2}{\sqrt{m}} \right) \sqrt{N} + 34m^2 + 20 \right], \tag{4}
\]

\[
\bar{l}_{\text{2d}, \text{max}} = \sqrt{mN}. \tag{5}
\]

For details of the derivation, see Appendix C.

We visualize the aforementioned compilation overheads expressed via mean and maximal qubit distances in Figs. 5(a) and 5(b) as a function of increasing qubit number. These figures illustrate several important properties, which we comment on in the following. The linear configuration (labeled 1D) clearly exhibits a linear scaling of the compilation overhead, while the rectangular device with nearest neighbor connectivity (labeled 2D) exhibits a square-root scaling. The compilation overhead of the proposed architecture inherits the favourable square-root scaling of 2D hardware topologies, making the proposed architecture favorable over 1D devices. Interestingly, the compilation overhead of the proposed device never exceeds the compilation overhead of the linear architecture, even for the smallest devices \( d_x = d_y = 1, 2, 3, \ldots \). This is useful as first experimental realizations of the proposed architecture would start from small prototypes. Finally, for increasing sparsity \( m = 4, 8, 16, \ldots \), the compilation overhead of the proposed architecture does increase; however, it never exceeds the overhead of the linear device. This allows for balancing the trade-off between compilation overhead and creating space in between the qubit modules which can be beneficial for colocation of classical support electronics.

**Case II – Rearranging qubits in arbitrary permutations**

We now consider the cost of permuting all qubits at once, making use of sorting networks \([71, 72]\). We begin by recalling qubit permutations on linear and rectangular devices \([73, 74]\) as these underlie the compilation method for the proposed sparse architecture.

**Parallel neighbor sort for 1D** We first consider permutations on 1D linear devices with \( N \) qubits using parallel neighbor sort \([75]\), as depicted in Fig. 5(a). First, each node of the hardware graph is assigned an index \( v = 1, \ldots, N \) in ascending order, and each qubit is labeled by its final position. Consecutive layers of SWAP operations are then applied in up to \( N \) steps. For odd steps 1, 3, 5, ..., qubits on node pairs \((v, u) \in \{(1, 2), (3, 4), \ldots \}\) are compared and a SWAP operation is applied if the final destination of qubit \( v \) is larger than the final destination of qubit \( u \). For even steps 2, 4, 6, ..., the same process occurs for qubits in node pairs \((v, u) \in \{(2, 3), (4, 5), \ldots \}\).

With this method, any permutation can be implemented in a maximum of \( N \) layers leading to an increase in the circuit depth of

\[
N_d = N. \tag{5}
\]

The maximum number of SWAP operations needed is

\[
N_{SWAP} = \frac{N(N - 1)}{2}. \tag{6}
\]

An alternative is to use bubble sort or insertion sort, but the maximum depth increases to \( 2N - 3 \) \([71, 72]\).
FIG. 5: Compilation overhead expressed via (a) average and (b) maximum shortest path as a function of the number of qubits for different layouts – a (1D) linear layout, a (2D) rectangular device with nearest neighbor connectivity with $l_x = l_y$ and the proposed architecture in a square arrangement $d_x = d_y$ with $m = 4$, 8, and 16. Lines indicate the scaling and dots indicate qubit numbers which can be realized by an actual device.

FIG. 6: Qubit permutations on (a) linear and (b) rectangular devices. (a) Parallel neighbor sort for a linear device with $N = 4$ qubits using 4 consecutive layers of SWAPs. Qubits (circles) are labeled by final position. Orange lines indicate qubit pairs which are compared at a given iteration and swapped, if in the wrong order. (b) Permuting $N = 9$ qubits (circles) in a square layout. Labels indicate the final row and column. The permutation is implemented by consecutively using parallel neighbor sort along (i) columns, (ii) rows and (iii) columns, as highlighted by orange lines.

Qubit permutation for the rectangular device Next, we consider permutations on a rectangular device of $N = l_x l_y$ qubits with nearest neighbor connectivity. We follow the algorithm of Ref. [73], which consists of the following three steps: (i) Rearrange the qubits in each column using parallel neighbor sort such that each row contains exactly one qubit with final destination in each column $1, 2, 3, ..., l_x$. (ii) Rearrange the qubits in each row using parallel neighbor sort such that all qubits are in the correct column. (iii) Rearrange the qubits in each column using parallel neighbor sort such that each qubit is in the correct final location. We note that column and row can also be interchanged in the above steps. An example visualizing the method is shown in Fig. 6(b).

Once step (i) provides an arrangement such that each row contains exactly one qubit with final destination in column $1, 2, 3, ..., l_x$, an implementation of steps (ii) and (iii) using parallel neighbor sort is simple. The challenge is to see that an efficient implementation of step (i) is always possible. This was shown in Refs. [73] [74] using Hall’s matching theorem [70] and will be discussed in more detail in its adaption to the proposed architecture with sparse 2d connectivity below. The overhead of the discussed method originates from consecutively using parallel neighbor sort on (i) columns (ii) rows and (iii) columns. This results in a maximum of

$$N_d = 2l_y + l_x$$ (7)

layers of SWAP gates and

$$N_{\text{SWAP}} = \frac{1}{2}l_x l_y(l_x + 2l_y - 3)$$ (8)

total SWAP gates. Specifically, for the square $l_y = l_x = \sqrt{N}$, this gives

$$N_d = 3\sqrt{N}$$ (9)

and

$$N_{\text{SWAP}} = \frac{3}{2}N(\sqrt{N} - 1).$$ (10)
Generalized rows and columns. We now extend the method of Ref. [73] to the proposed architecture with sparse 2d connectivity. Our method is based on the definition of generalized rows and columns as depicted in Figs. 7(a) and 7(b) respectively. In essence, this results in 2\(d_y\) rows and 2\(d_x\) columns with 2\(md_x\) and 2\(md_y\) qubits respectively, where any given row and column share \(m\) qubits. Having defined these generalized rows and columns, we note that every qubit can conveniently be labeled by a combination of its column index, \(a_x = 1, \ldots, 2d_x\), and its vertical position, \(y\). Equivalently, we could choose to label a qubit by its row index, \(a_y\) and its horizontal position, \(x\). The coordinates \(x\) and \(y\) can be seen in figure 1(d). We note that not all constructions of sparsely-connected devices from the linear segments and junction shown in figures 1(a) and 1(b) respectively would have enabled such simple definitions of generalized rows and columns. We show an alternative device construction in figure 8 for which equivalent generalized rows and columns do not exist. It is also not possible to draw a single line through all the qubits in such a device.

Compilation for the proposed architecture. With generalized rows and columns in place, we describe the corresponding compilation algorithm for implementing qubit permutations. Each qubit, in its initial location, carries a label \((a_x, y)\), indicating its final position. An arbitrary qubit permutation can then be implemented using the following three steps: (i) Rearrange the qubits in each generalized column using parallel neighbor sort such that each set of qubits with fixed coordinate \(y\) contains exactly one qubit with final destination in each column \(a_x = 1, 2, 3, \ldots, 2d_x\). (ii) Rearrange the qubits in each generalized row using parallel neighbor sort such that all qubits are moved into the correct column according to their column index \(a_x\). (iii) Rearrange the qubits in each generalized column using parallel neighbor sort such that each qubit is in the correct \(y\) location along the columns. An example visualizing the method is given in Fig. 9.

Bipartite routing graph. We note again that, once step (i) provides an arrangement such that each set of qubits with vertical position \(y\) contains exactly one qubit with final destination in column \(a_x = 1, 2, 3, \ldots, 2d_x\), an implementation of steps (ii) and (iii) using parallel neighbor sort is straightforward. The challenge is again to see that an efficient implementation of step (i) is always possible. The procedure to achieve this is illustrated in Fig. 9(e-g) and shall now be explained in more detail. To begin with, a bipartite graph of \(4d_x\) nodes is constructed, \(l \in 1, \ldots, 2d_x\) on the left and \(2d_y\) nodes \(r \in 1, \ldots, 2d_y\) on the right. Nodes on the left indicate columns in which a qubit is located initially. Nodes on the right indicate columns to which a qubit should be routed. To build the graph, one adds an edge \((l, r)\) to the bipartite graph for each qubit initially located in column \(l\) and having final destination in column \(r\). An example is given in Fig. 9(e).

We note that, since we have \(2md_y\) qubits located in each column initially and since we will have \(2md_y\) qubits with final destination located in each column, the bipartite graph has \(2md_y\) edges incident to each node. Since some qubits may originate and end up in the same column, the bipartite graph can have multiple edges connecting the same nodes.

Hall’s matchings. Next, to determine how qubits should be arranged along columns in step (i), one extracts \(2md_y\) perfect matchings \(\mathcal{M}_y\) with \(y = 1, \ldots, 2md_y\) from the bipartite graph. A perfect matching \(\mathcal{M}_y\) is a set of edges such that each node of the bipartite graph...
is connected to exactly one edge of the matching. See Fig. 9(g) for examples showing one possible set of perfect matchings for the bipartite graph in Fig. 9(e). Finding $2md_y$ perfect matchings for the given type of bipartite graph is always possible due to Hall’s matching theorem \[70\]. In the bipartite graphs that arise due to our compilation problem, each node has the same number of incident edges, a sufficient condition for Hall’s matching theorem to hold. Matchings can efficiently be found using the Ford-Fulkerson algorithm \[70\]. To this end, one attaches virtual nodes $s$ and $t$ to all nodes on the left and right of the bipartite graph, respectively, and determines a minimal network flow from $s$ to $t$; see Fig. 9(f). Finding a minimal flow configuration reveals one matching at a time. Successively removing edges of a matching from the bipartite graph and repeatedly running the Ford-Fulkerson algorithm will reveal all matchings $M_y$ with $y = 1, \ldots, 2md_y$, as visualized in Fig. 9(g). Finally, to route qubits in step (i), one selects qubits which move to vertical position $y$ by iterating over the edges of the $y$th matching $(l, r) \in M_y$. Here, each edge $(l, r)$ signifies that in the generalized column $l$ a qubit destined for the generalized column $r$ should be moved to vertical position $y$. Since edges in each set of matchings $M_y$ point to exactly one final destination per vertical position $y$, the fact that $2md_y$ matchings exist ensures that step (i) arranges the qubits in each column so that each row contains exactly $m$ qubits with final destination in column $1, 2, 3, \ldots, 2md_x$.

**Compilation overhead** We close this section by evaluating the compilation overhead. Considering the succession of parallel neighbor sorts along (i) generalized columns of length $2md_y$, (ii) generalized rows of length $2md_x$, and (iii) again generalized columns of length $2md_y$, the maximum number of required layers of SWAP gates is given by

$$N_d = 4md_y + 2md_x \quad (11)$$

and the maximum total number of SWAP gates by

$$N_{SWAP} = 2md_xd_y(2md_x + 4md_y - 3). \quad (12)$$

For the specific case $d_x = d_y = d$, and using Eq. (1), we have

$$N_d = 6md = 3\sqrt{mN} \quad (13)$$

FIG. 9: Qubit permutation on proposed architecture with $d_x = 2$, $d_y = 1$, and $m = 2$. (a-d) Qubits (circles) labeled by their final destination $(y, a_i)$ are permuted using parallel neighbor sort along generalized (i) columns, (ii) rows, and (iii) columns as indicated by black solid as opposed to gray dashed lines. (e) Bipartite graph corresponding to step (i). Nodes on the left and right indicate qubits with origin and final destination in columns 1, 2, 3, and 4 respectively, while edges represent the corresponding qubit. (f) Same as (e) with virtual nodes $s$, $t$. (g) Matchings extracted from (e). The $y$th matching determines qubits routed to position $y$. An edge $(l, r)$ of $y$th matching indicates that a qubit of column $l$ destined for column $r$ is to be routed to position $y$.

FIG. 10: Compilation overhead given by maximum number of layers of SWAP gates as a function of the number of qubits for (1d) linear qubit chains, (2d) rectangular nearest-neighbor grids and the proposed architecture for $d_x = d_y = d$ with $m = 4, 8$ and 16. Lines indicate scaling and dots indicate qubit layout which exist. Crosses indicate the reduced compilation overhead by using a single parallel neighbor sort for devices with $d_x = d_y = 1$. Such devices consist of a square of qubits, as seen in figure 1(c).
and

\[ N_{\text{SWAP}} = 6m^2d^2(2md - 1) = \frac{3}{2}N\sqrt{mN} - 1. \] (14)

We compare the compilation overhead of the proposed architecture with sparse 2d connectivity to the linear and rectangular hardware graphs in Fig. 10. Again, the linear configuration (labeled 1D) exhibits a linear scaling of the compilation overhead, while the rectangular device with nearest neighbor connectivity (labeled 2D) exhibits a square-root scaling. The compilation overhead of the proposed architecture inherits the favourable square-root scaling of 2d hardware topologies, making the proposed architecture favorable over 1D devices. Interestingly, the compilation overhead of the proposed device never exceeds the compilation overhead of the linear architecture for \( d_x = d_y \geq 2 \). For device structures with \( d_x = d_y = 1 \), the compilation overhead of the proposed architecture can be reduced by recognising that the rearrangement of the sparse device can always be handled with a single parallel neighbor sort, by arranging the qubits along a single line. This ensures that the compilation overhead for the proposed architecture never exceeds the compilation overhead of the 1D architecture even for the smallest devices. This is useful as first experimental realizations of the proposed architecture would start from small prototypes. Finally, for increasing sparsity \( m = 4, 8, 16, ..., \) the compilation overhead of the proposed architecture does increase; however, it again never exceeds the overhead of the linear device. This allows for balancing between compilation overhead and creating space in between the qubit modules which can be beneficial for colocation of classical support electronics.

**DISCUSSION**

Inspired by the challenge of scaling up existing silicon quantum hardware, we investigate compilation strategies for sparsely-connected 2d qubit arrangements and propose a spin-qubit architecture with minimal compilation overhead. Our considerations are inspired by silicon nanowire split-gate transistors which form finite 1d chains of spin-qubits, allowing for the execution of two-qubit operations such as SWAP gates among neighbors. Adding to this, we describe a novel silicon junction which can couple up to four nanowires at one end into 1d or 2d arrangements via spin shuttling and SWAP operations. Given these hardware elements, we propose a modular 2d spin-qubit architecture with unit cells consisting of diagonally-oriented squares with nanowires along the edges and junctions at the corners.

The junction geometry opens space between modules to route the gate lines and/or to place cryogenic classical electronics in the quantum processor plane [10, 54]. Fabricating the qubits and the classical control layer using the same technology is appealing because it will facilitate the integration process, improving feedback speeds in error-correction protocols, and offer potential solutions to wiring and layout challenges [4, 17, 81]. Integrating classical and quantum devices monolithically, using CMOS processes, enables the quantum processor to profit from the most mature industrial technology for the fabrication of large-scale circuits [35]. We show that this architecture allows for compilation strategies which inherit the favorable square-root scaling of compilation overhead in 2d structure and outperform the best in class compilation strategy of 1d chains, not only asymptotically, but also down to the minimal structure of a single square. This result shows that scaling silicon nanowires into 2d structures will have benefits early on, even in experimental demonstrations of the smallest prototypes, thus encouraging building the proposed junction element and expanding silicon architectures into 2d arrangements. We further note that our compilation strategies, while being inspired by spin-qubits, are equally valid for any other quantum processor with sparse 2d connectivity.

The compilation strategies presented here act to demonstrate the square-root scaling in overhead due to routing for the sparsely-connected device, and the advantage of using this device over one with a 1d structure. Many other architecture-aware compilation methods exist and show good results [e.g., 82, 83]. Circuit re-synthesis [82] provides another option. Alternatively, it may be beneficial to consider a compilation method designed with the desired algorithm in mind [e.g., 15, 88]. However, the distance between qubits will clearly affect the overhead introduced through such compilation methods, and thus the results presented here provide some indication of their likely performance. Finally, the methods presented in this paper and discussed above are typically for NISQ-era devices; for the fault-tolerant era, it will clearly be important to investigate how best to perform error correction on the device.

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Competing Interests

The authors declare that they have no competing financial interests.

Correspondence

Correspondence and requests for materials should be addressed to O.C. (email: ophe-lia.crawford@riverlane.com) and M.F.G.Z (email: mg507@cam.ac.uk).

APPENDIX A. TWO-SPIN HAMILTONIAN IN A DOUBLE QUANTUM DOT

To produce the energy spectrum in Fig. 2(d), we use the following Hamiltonian

\[
H = \begin{pmatrix}
\frac{\epsilon}{2} + Z_{av} & 0 & 0 & 0 \\
0 & \frac{\epsilon}{2} + Z_{d} & 0 & t_s \\
0 & 0 & \frac{\epsilon}{2} - Z_{d} & 0 \\
0 & 0 & 0 & \frac{\epsilon}{2} - Z_{av}
\end{pmatrix}
\]  

(15)

where \(Z_{av}\) stands for the Zeeman energy average \(Z_{av} = \frac{(g_1 + g_2)\mu_B B}{2}\) and \(Z_d\) is the Zeeman energy difference \(Z_d = (g_1 - g_2)\mu_B B\). Here \(g_i\) is the g-factor of the particle \(i\), \(\mu_B\) is the Bohr magneton and \(B\) is the external magnetic field. We consider negligible coupling between spins states with different total spin number. This Hamiltonian is given in the basis states \(\{|\uparrow, \uparrow\rangle, |\downarrow, \uparrow\rangle, |\uparrow, \downarrow\rangle, |\downarrow, \downarrow\rangle, |\uparrow\downarrow - \downarrow\uparrow, 0\rangle = |S(20)\rangle\}, assuming \(g_1 < g_2\).

APPENDIX B. TIMESCALE OF THE SHUTTLING SEQUENCE

For silicon electron spin qubits, coherent shuttling has been performed in 8 ns or longer [33]. However, the lower end of this demonstration has been limited by the control hardware and hence faster coherent shuttling may be achieved. Considering state leakage due to non-adiabatic tunneling as the mechanism for loss of shuttling fidelity at short timescales, we estimate the minimum duration of the shuttling sequence. We consider negligible coupling between spins states with different total spin number. This Hamiltonian is given in the basis states \(\{|\uparrow, \uparrow\rangle, |\downarrow, \uparrow\rangle, |\uparrow, \downarrow\rangle, |\downarrow, \downarrow\rangle, |\uparrow\downarrow - \downarrow\uparrow, 0\rangle = |S(20)\rangle\}, assuming \(g_1 < g_2\).

\[P_{LZ} = \exp \left[-\frac{\pi (2t_s)^2}{2v}\right] \]  

(16)

where \(v\) is the driving velocity across the double QD anticrossing. Considering a minimum pulse amplitude of \(4(2t_s)\) and \(t_s \approx 50\) GHz [33], we obtain a shuttling time, \(t_{sh} = 235\) ps for \(P_{LZ} = 10^{-4}\). Considering 6 shuttling steps, the total shuttling time corresponds to \(T_{sh} = 1.4\) ns.

Comparing this figure with the state-of-the-art exchange gate in silicon performed in subnanosecond timescales (0.8 ns) [59], there may be regimes in which shuttling time may add a sizable overhead. However, slower exchange gates (controlled by reducing the QD exchange coupling) or synthesized \(\sqrt{\text{SWAP}}\), from single qubit gates and a CPhase gate (\(\approx 100\) ns [5, 20]) may substantially increase the control fidelity. In that regime, shuttling time becomes negligible.

We note that the number of shuttling steps could be reduced to 4 by shuttling simultaneously two electrons and performing the SWAP gate when one electron is located under the central gate of the junction and the other under one of the neighboring gates.

APPENDIX C. DISTANCE AVERAGING

In this section, we will calculate the average distance between two qubits in different layouts by summing over all pairs of qubits and dividing by the total number of pairs of qubits. The average distance, \(\bar{l}\), is therefore

\[
\bar{l} = \frac{2}{n(n-1)} l_{\text{tot}},
\]  

(17)
where $l_{tot}$ is the total distance between all pairs of qubits. We will make use of the standard sums, which are

\begin{align}
S_0 &= \sum_{i=x_1}^{x_2} 1 = (x_2 - x_1 + 1), \\
S_1 &= \sum_{i=x_1}^{x_2} i = \frac{1}{2}x_2(x_2 + 1) - \frac{1}{2}x_1(x_1 - 1), \\
S_2 &= \sum_{i=x_1}^{x_2} i^2 = \frac{1}{6}x_2(x_2 + 1)(2x_2 + 1) - \frac{1}{6}x_1(x_1 - 1)(2x_1 - 1), \\
S_3 &= \sum_{i=x_1}^{x_2} i^3 = \frac{1}{4}x_2^2(x_2 + 1)^2 - \frac{1}{4}x_1^2(x_1 - 1)^2, \\
S_4 &= \sum_{i=x_1}^{x_2} i^4 = \frac{1}{30}x_2(x_2 + 1)(2x_2 + 1)(3x_2^2 + 3x_2 - 1) - \frac{1}{30}x_1(x_1 - 1)(2x_1 - 1)(3x_1^2 - 3x_1 - 1).
\end{align}

**Sparsely-connected two-dimensional layout**

We will find it useful to define the qubits by the particular square they are in, specified by an $x$ co-ordinate with possible values from 1 to $d_x$ and a $y$ co-ordinate with possible values from 1 to $d_y$. We will use $(a_x, a_y)$ for these co-ordinates, and further use $(b_x, b_y)$ when considering two qubits simultaneously. We will then split the possible pairs of qubits into two – those with $|a_x - b_x| \neq |a_y - b_y|$ and those with $|a_x - b_x| = |a_y - b_y|$.

In the calculations that follow, we will assume $d_x \geq d_y$. A device can be rotated to ensure this is true.

**Pairs of qubits with $|a_x - b_x| \neq |a_y - b_y|$**

When considering these pairs of qubits, we split them again into those with $|a_x - b_x| < |a_y - b_y|$ and those with $|a_x - b_x| > |a_y - b_y|$. We first consider the former. In this case, the shortest distance between any two vertices of the two chosen squares is $|a_y - b_y| - 1$. The shortest path between any one qubit in one square and any other qubit in the other square includes this shortest path between vertices. We will therefore begin by summing over the distances between the nearest vertices of the squares before later including the additional distance to the qubits.
We find that the total sum of distances between pairs of squares is given by

\[
    l_{sq1} = \sum_{a_y=1}^{d_y} \sum_{b_y=a_y+1}^{d_y} 2m(b_y - a_y - 1) \left[ \sum_{i=1}^{b_y-a_y} 2(d_x - i + 1) - d_x \right] 
\]

\[
    = \sum_{f_y=1}^{d_y} \sum_{c_y=1}^{f_y-1} 2m(c_y - 1) \left[ \sum_{i=1}^{c_y} 2(d_x - i + 1) - d_x \right] 
\]

\[
    = \sum_{f_y=1}^{d_y} \sum_{c_y=1}^{f_y-1} 2m(c_y - 1) \left[ c_y(2d_x + 1 - c_y) - d_x \right] 
\]

\[
    = \sum_{f_y=1}^{d_y} \sum_{c_y=1}^{f_y-1} \left[ -c_y^3 + c_y^2(2d_x + 2) - c_y(3d_x + 1) + d_x \right] 
\]

\[
    = \sum_{f_y=1}^{d_y} 2m \left[ -\frac{1}{4} f_y^3(f_y - 1)^2 + \frac{1}{3} f_y (f_y - 1)(2f_y - 1)(d_x + 1) - \frac{1}{2} f_y (f_y - 1)(3d_x + 1) + (f_y - 1)d_x \right] 
\]

\[
    = 2m \sum_{f_y=1}^{d_y} \left[ -\frac{1}{4} f_y^4 + \frac{1}{6} (7 + 4d_x) f_y^3 - \frac{1}{4} (7 + 10d_x) f_y^2 + \frac{1}{6} (5 + 17d_x) f_y - d_x \right] 
\]

\[
    = -\frac{m}{60} d_y(d_y + 1)(2d_y + 1)(3d_y^2 + 3d_y - 1) + \frac{m}{12} (7 + 4d_x)d_y^2(d_y + 1)^2 - \frac{m}{12} (7 + 10d_x)d_y(d_y + 1)(2d_y + 1) 
\]

\[
    + \frac{1}{30} m d_y(d_y - 1)(d_y - 2)(4 + (1 + 10d_x)d_y - 3d_y^2). \tag{23} 
\]

We now consider qubits with \(|a_x - b_x| > |a_y - b_y|\). In this case, the shortest distance between any two vertices of the two chosen squares is \(|a_x - b_x| - 1\). Again, the shortest path between any one qubit in one square and any other qubit in the other square includes this shortest path between vertices. We will therefore now sum over the distances between the nearest vertices of the squares before later including the additional distance to the qubits. We find this total distance is given by

\[
    l_{sq2} = l_{p1} + l_{p2} + l_{p3}, \tag{24} 
\]

where

\[
    l_{p1} = \sum_{a_x=1}^{d_x} \sum_{b_x=a_x+1}^{d_x} \sum_{c_x=1}^{d_x} 2m(b_x - a_x - 1) \left[ \sum_{i=1}^{b_x-a_x} 2(d_y - i + 1) - d_y \right] \tag{25} 
\]

\[
    l_{p2} = \sum_{a_x=1}^{d_x} \sum_{b_x=a_x+1}^{d_x} \sum_{c_x=1}^{d_x} 2m(b_x - a_x - 1) \left[ \sum_{i=1}^{b_x-a_x} 2(d_y - i + 1) - d_y \right] \tag{26} 
\]

\[
    l_{p3} = \sum_{a_x=1}^{d_x} \sum_{b_x=a_x+1}^{d_x} \sum_{c_x=1}^{d_x} 2m(b_x - a_x - 1) \left[ \sum_{i=1}^{d_y} 2(d_y - i + 1) - d_y \right]. \tag{27} 
\]

Evaluating these in turn, we find

\[
    l_{p1} = \sum_{f_y=1}^{d_y} \sum_{c_y=1}^{f_y-1} 2(c_x - 1) \left[ \sum_{i=1}^{c_x} 2m(d_y - i + 1) - d_y \right] 
\]

\[
    = \frac{1}{30} m d_y(d_y - 1)(d_y - 2)(4 + (1 + 10d_y)d_y - 3d_y^2) 
\]

\[
    = \frac{1}{30} m d_y(d_y - 1)(d_y - 2)(7d_y^2 + d_y + 4). \tag{28} 
\]

We note that the total sum of distances between any two vertices of the two chosen squares is given by
\[
l_{p2} = 2 \sum_{a_{x}=1}^{d_{x}-d_{y}} \sum_{c_{x}=1}^{d_{x}} m(c_{x} - 1) \left[ \sum_{i=1}^{c_{x}} 2(d_{y} - i + 1) - d_{y} \right] \\
= \sum_{a_{x}=1}^{d_{x}-d_{y}} 2m \left[ -\frac{1}{4} d_{y}^{2}(d_{y} + 1)^{2} + \frac{1}{3} d_{y}(d_{y} + 1)^{2}(2d_{y} + 1) - \frac{1}{2} d_{y}(d_{y} + 1)(3d_{y} + 1) + d_{x}d_{y} \right] \\
= 2md_{y}(d_{x} - d_{y}) \left[ -\frac{1}{4} d_{y}(d_{y} + 1)^{2} + \frac{1}{3} (d_{y} + 1)^{2}(2d_{y} + 1) - \frac{1}{2} (d_{y} + 1)(3d_{y} + 1) + d_{x} \right] \\
= \frac{1}{6} md_{y}(d_{y} - 1)(d_{x} - d_{y})(5d_{y}^{2} + d_{y} + 2), \quad (29)
\]

\[
l_{p3} = 2m d_{y}^{2} \sum_{a_{x}=1}^{d_{x}-d_{y}} \sum_{c_{x}=1}^{d_{x}-d_{y}-a_{x}} (c_{x} + d_{y} - 1) \\
= 2m d_{y}^{2} \sum_{a_{x}=1}^{d_{x}-d_{y}} \left[ \frac{1}{2}(d_{x} - d_{y} - a_{x})(d_{x} - d_{y} - a_{x} + 1) + (d_{x} - d_{y} - a_{x})(d_{y} - 1) \right] \\
= md_{y}^{2} \sum_{a_{x}=1}^{d_{x}-d_{y}} \left[ a_{x}^{2} + (2d_{x} - 1)a_{x} + (d_{x} - d_{y})(d_{x} + d_{y} - 1) \right] \\
= md_{y}^{2} \left[ \frac{1}{6}(d_{x} - d_{y})(d_{x} - d_{y} + 1)(2d_{x} - 2d_{y} + 1) - \frac{1}{2}(2d_{x} - 1)(d_{x} - d_{y})(d_{x} - d_{y} + 1) + (d_{x} - d_{y})^{2}(d_{x} + d_{y} - 1) \right] \\
= \frac{1}{3} md_{y}^{2}(d_{x} - d_{y})(d_{x} - d_{y} - 1)(d_{x} + 2d_{y} - 2), \quad (30)
\]

We now have the total distance between all squares for which \(|a_{x} - b_{x}| \neq |a_{y} - b_{y}|\). As each square contains 4m qubits, we first need to multiply these distances between the squares by \(16m^{2}\). We also need to add the additional distance due to the fact the qubits are some distance from the vertex involved in the shortest distance between vertices. For each pair of squares, we therefore need to add the distance

\[
l_{q} = 4 \sum_{i=1}^{2m} \sum_{j=1}^{2m} (i + j - 1) = 4m \sum_{i=1}^{2m} [2i + 2m - 1] = 32m^{3}. \quad (31)
\]

The total number of pairs of squares is

\[
n_{sq} = \frac{1}{2} d_{x} d_{y}(d_{x} d_{y} - 1). \quad (32)
\]

The total number of pairs of squares with \(|a_{x} - a_{y}| = |b_{x} - b_{y}|\) is

\[
n_{sq1} = 4 \sum_{i=1}^{d_{x}-1} i \sum_{b_{y}=a_{y}+1}^{d_{y}} \left[ 1 + 2(d_{x} - d_{y} + 1) \right] \sum_{a_{x}=1}^{d_{x}} \sum_{b_{y}=1}^{d_{y}} 1 \\
= 2 \sum_{i=1}^{d_{x}-1} (i^{2} - i) + d_{y}(d_{y} - 1)(d_{x} - d_{y} + 1) \\
= \frac{1}{3} d_{y}(d_{y} - 1)(2d_{y} - 1) - d_{y}(d_{y} - 1) + d_{y}(d_{y} - 1)(d_{x} - d_{y} + 1) \\
= \frac{1}{3} d_{y}(d_{y} - 1)(3d_{x} - d_{y} - 1). \quad (33)
\]

Therefore, the total number of pairs of squares with \(|a_{x} - a_{y}| \neq |b_{x} - b_{y}|\) is

\[
n_{sq2} = n_{sq} - n_{sq1} = \frac{1}{6} d_{y}[3d_{y}^{2}d_{y} - 6d_{x}d_{y} + 3d_{x} + 2d_{y}^{2} - 2]. \quad (34)
\]

The total distance between qubits for which \(|a_{x} - a_{y}| \neq |b_{x} - b_{y}|\) is finally given by

\[
d_{ncq} = 16m^{2}(l_{sq1} + l_{sq2}) + 32m^{3}n_{sq2}. \quad (35)
\]
Pairs of qubits with $|a_x - b_x| = |a_y - b_y|$

We now consider pairs of qubits with $|a_x - b_x| = |a_y - b_y|$. In this case, there is not a unique pair of nearest vertices in the two squares and so we must consider different pairs of qubits in different manners.

We will consider squares with a particular value of $(b_x - a_x)$ in turn, giving us a line of diagonally oriented squares. For the moment, we assume that we have a set of $n$ such squares; we will sum over the different values of $n$ later. We first consider summing over the distances between all pairs of qubits down the sides of the squares, given by

$$l_{ss}^n = 2 \sum_{i=1}^{n} \sum_{j=i+1}^{n} \sum_{k=1}^{m} \sum_{l=1}^{m} [2m(j - i) + (l - k)]$$

$$= 4m^3 \sum_{i=1}^{n} \sum_{j=i+1}^{n} (j - i)$$

$$= 4m^3 \sum_{i=1}^{n} \left[ \frac{1}{2}n(n + 1) - \frac{1}{2}i(i + 1) - in + i^2 \right]$$

$$= 4m^3 \sum_{i=1}^{n} \left[ \frac{i^2}{2} - i(2n + 1) + \frac{1}{2}n(n + 1) \right]$$

$$= 4m^3 \left[ \frac{1}{12}n(n+1)(2n+1) - \frac{1}{4}n(n+1)(2n+1) + \frac{1}{2}n^2(n+1) \right]$$

$$= \frac{2}{3}m^3n(n-1)(n+1). \quad (39)$$

We now consider pairs of qubits on opposite sides of the line of squares; however, to avoid double counting, we do not include pairs of qubits on opposite sides of the same square. This distance sum is given by

$$l_{as}^n = 2 \sum_{i=1}^{n} \sum_{j=i+1}^{n} \sum_{k=1}^{m} \sum_{l=1}^{m} [2m(j - i) + (l - k) + m] \quad (40)$$

$$= l_{ss}^n + m^3n(n-1) \quad (41)$$

$$= \frac{2}{3}m^3n(n-1)(2n+5). \quad (42)$$

We next consider pairs of qubits where one of the pair is on one of the sides of the line of squares and the other is on an edge at right angles to this, on a ‘rung’ of the line of squares. Again, to avoid double counting, we exclude some pairs of qubits here. This sum of distances is given by

$$l_{sr}^n = 2 \sum_{i=1}^{n} \sum_{j=1}^{2i-2} \sum_{k=1}^{m} \sum_{l=1}^{m} [(2i - j - 1)m + l + k - 1] + 2 \sum_{i=1}^{n} \sum_{j=2i}^{2n} \sum_{k=1}^{m} \sum_{l=1}^{m} [(j - 2i + 1)m + l - k]$$

$$= 2 \sum_{i=1}^{n} \sum_{j=1}^{2i-2} [(2i - j - 1)m^3 + m^2(m + 1) - m^2] + 2m^3 \sum_{i=1}^{n} \sum_{j=2i}^{2n} (j - 2i + 1)$$

$$= 2m^3 \sum_{i=1}^{n} \sum_{j=1}^{2i-2} (2i - j) + 2m^3 \sum_{i=1}^{n} \sum_{j=2i}^{2n} \sum_{k=1}^{m} k$$

$$= 2m^3 \sum_{i=1}^{n} \left[ 2i(2i - 2) - \frac{1}{2} (2i - 2)(2i - 1) + (2n - 2i + 1)(2n - 2i + 2) \right]$$

$$= m^3 \sum_{i=1}^{n} \left[ 8i^2 - 8i(n + 1) + 2m^2 + 3n \right]$$

$$= m^3 \left[ \frac{4}{3}n(n+1)(2n+1) - 4n(n+1)^2 + 2n^3 + 3n^2 \right]$$

$$= \frac{2}{3}m^3n(4n^2 + 3n - 4). \quad (43)$$
We finally consider pairs of qubits where both qubits are on a ‘rung’ of the line of squares. Here, the total distance between pairs of qubits is given by

\[ l_{rr}^n = 2n \sum_{k=1}^m \sum_{l=k+1}^m (l-k) + 2n \sum_{i=1}^n \sum_{j=i+1}^n \sum_{k=1}^m \sum_{l=1}^{m-k+1} [(j-i)m+k+l-1] + \sum_{l=m-k+2}^m [(j-i+2)m-k-l+1] \]

\[ = 2n \sum_{k=1}^m \sum_{l=k+1}^m (l-k) + \sum_{i=1}^n \sum_{j=i+1}^n \sum_{k=1}^m \sum_{l=1}^{m-k+1} [(j-i)m+(k+l-1)] + \sum_{l=m-k+2}^m (2m-k-l+1) \]

\[ = \frac{1}{3} nm(m+1)(m-1) + \frac{1}{6} m^3 2n(2n+1)(2n-1) \]

\[ + \sum_{i=1}^n \sum_{j=i+1}^n \sum_{k=1}^m \left[ \frac{1}{2} (m-k+1)(m+k) + (2m-k+1)(k-1) - \frac{1}{2} m(m+1) + \frac{1}{2} (m-k+1)(m-k+2) \right] \]

\[ = \frac{1}{3} nm(m+1)(m-1) + \frac{1}{3} m^3 n(2n+1)(2n-1) + \sum_{i=1}^n \sum_{j=i+1}^n \sum_{k=1}^m \left[ -k^2 + (m+1)k + \frac{1}{2} m(m-1) \right] \]

\[ = \frac{1}{3} nm(m+1)(m-1) + \frac{1}{3} m^3 n(2n+1)(2n-1) + n(2n-1) \left[ -\frac{1}{6} m(m+1)(2m+1) + \frac{1}{2} m(m+1)^2 + \frac{1}{2} m^2(m-1) \right] \]

\[ = \frac{2}{3} nm(2nm^2 + 2n^3m^2 - m^2 + n-1). \tag{44} \]

Taking the sum \( l^n = l_{ss}^n + l_{os}^n + l_{sr}^n + l_{rr}^n \), we find

\[ l^n = \frac{1}{3} nm(13nm^2 + 16n^2m^2 - 17m^2 + 2n - 2). \tag{45} \]

We now need to sum over the different values of \( n \). There are four lines of squares for each \( 1 \leq n \leq d_y - 1 \) and \( 2(d_x - d_y + 1) \) squares with \( n = d_y \). Therefore, the total distance between qubits with \( |a_x - b_x| = |a_y - b_y| \) is

\[ d_{eq} = \frac{4}{3} m \sum_{n=1}^{d_y-1} \left( 13n^2m^2 + 16n^3m^2 - 17nm^2 + 2n^2 - 2n \right) + \frac{2}{3} (d_x - d_y + 1) md_y(13m^2d_y + 16m^2d_y^2 - 17m^2 + 2d_y - 2) \]

\[ = \frac{4}{3} md_y(d_y-1) \left[ \frac{1}{6} (13m^2 + 2)(2d_y - 1) + 4m^2d_y(d_y-1) - \frac{1}{2} (17m^2 + 2) \right] \]

\[ + \frac{2}{3} md_y(d_x - d_y + 1)(13m^2d_y + 16m^2d_y^2 - 17m^2 + 2d_y - 2). \tag{46} \]

**Mean distance**

The mean distance between two randomly selected qubits is given by

\[ \bar{l} = \frac{2}{N(N-1)} (d_{neq} + d_{eq}), \tag{47} \]

where we recall

\[ N = 4md_xd_y. \tag{48} \]

**Linear layout**

Given \( m \) qubits laid out linearly, the average distance between a pair of qubits is

\[ \bar{l} = \frac{2}{m(m-1)} \sum_{i=1}^m \sum_{j=i+1}^m (j-i) \]

\[ = \frac{1}{3m(m-1)} m(m+1)(m-1) \]

\[ = \frac{1}{3}(m+1). \tag{51} \]
Rectangular two-dimensional layout

Given a $l_x \times l_y$ rectangle of qubits, the average distance between a pair of qubits is given by

$$\bar{l} = \frac{2}{l_x l_y(l_x l_y - 1)} \sum_{i=1}^{l_y} \sum_{j=1}^{l_x} \left[ \sum_{k=i+1}^{l_y} \sum_{l=j}^{l_x} (k + l - i - j) + \sum_{k=1}^{l_y} \sum_{l=i+1}^{l_x} (i + l - k - j) \right].$$

(52)

$(i, j)$ and $(k, l)$ are the coordinates of two points. We sum over all possible $i$ and $j$, and, to avoid double counting, sum over the distance between the point $(i, j)$ and any points on the same row and to the right, or on a higher row. The first term sums inside the brackets sums over those points to the right and on the same row or a higher row, whilst the second term sums over those points in the same column or to the left on a higher row. Rearranging terms, we find

$$l_{\text{tot}} = \sum_{i=1}^{l_x} \sum_{k=1}^{l_y} \sum_{j=1}^{l_y} (l - j) + \sum_{j=1}^{l_y} \sum_{l=j}^{l_x} \sum_{k=1}^{l_y} (k - i) + \sum_{j=1}^{l_y} \sum_{l=i+1}^{l_x} \sum_{k=1}^{l_y} (i - k)$$

$$= \frac{1}{6} l_x l_y (l_y - 1)(l_y + 1) + \frac{1}{12} l_x l_y (l_x - 1)(l_x + 1) + \frac{1}{12} l_x l_y (l_y - 1)(l_y + 1)$$

$$= \frac{1}{6} l_x l_y (l_x l_y - 1)(l_x + l_y),$$

(53)

and so

$$\bar{l} = \frac{1}{3} (l_x + l_y).$$

(54)

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1. ophelia.crawford@riverlane.com
2. mg507@cam.ac.uk; Present Address: Quantum Motion Technologies, Cornwall Road, Harrogate, HG1 2PW, United Kingdom
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