Combinatorics and Geometry for the Many-ported, Distributed and Shared Memory Architecture

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Abstract—Manycore SoC architectures based on on-chip shared memory are preferred for flexible and programmable solutions in many application domains. However, the development of many ported memory is becoming increasingly challenging as we approach the end of Moore’s Law while systems requirements demand larger shared memory and more access ports. Memory can no longer be designed simply to minimize single transaction access time, but must take into account the functionality on the SoC. In this paper we examine a common large memory usage in SoC, where the memory is used as storage for large buffers that are then moved for time scheduled processing. We merge two aspects of many ported memory design, combinatorial analysis of interconnect, and geometric analysis of critical paths, extending both to show that in this case the SoC performance benefits significantly from a hierarchical, distributed and staged architecture with lower-radix switches and fractal randomization of memory bank addressing, along with judicious and geometry aware application of speed up. The results presented show the new architecture supports 20% higher throughput with 20% lower latency and 30% less interconnection area at approximately the same power consumption. We demonstrate the flexibility and scalability of this architecture on silicon from a physical design perspective by taking the design through layout. The architecture enables a much easier implementation flow that works well with physically irregular port access and memory dominant layout, which is a common issue in real designs.

Index Terms—Many-core SoC/NoC, Distributed and Shared Memory Architecture, Interconnect Network, Wire Crossing, Speed-up, Butterfly Topology, Directed Randomization

I. INTRODUCTION

Many core SoC architectures based on many ported on-chip shared memory are the preferred backbone for flexible and programmable solutions in many computationally intensive application domains, including machine learning [2], high performance wireless infrastructure [4], and embedded processing [3]. For the wireless application on the order of 30 to 100 processing blocks on a single chip are not uncommon to fulfill the overall processing needs. The Marvel CNF73xx LTE baseband SoC in [9] has similar architecture choices with a common on chip memory of 8 Mega bytes shared among over 30 heterogeneous accelerators and DSP cores. With the introduction of 5G/New Radio, the size of the shared memory has been tripled to 24 Mega byte and shared among 42 DSP cores and some other base band hardware accelerators [4]. Despite the requirement of increasingly large shared memory the performance of the SoC will suffer if the memory throughput to the compute elements (CEs) in the SoC decreases. Many CEs, especially if they have no software optimized prefetch, will suffer rapid performance loss if the average latency to memory increases. Average memory latency is the critical metric because CEs are scheduled to run functions that may take thousands of clock cycles to complete and similarly consume/produce thousands of bytes of data. It is only the completion time of the function, and therefore the average memory access latency, that matters to the performance of the CE. Finally an important practical metric is the effort expended in re-layout when the memory size changes, the memory bounding box shape alters or the number of ports change. A good memory design will cope easily with such changes at layout.

In this paper we address all of the above concerns using a combination of combinatorial analysis of interconnect, and geometric analysis of critical paths, and show that the SoC performance benefits significantly from a hierarchical, distributed and staged architecture with lower-radix switches and fractal randomization of memory bank addressing, along with judicious and geometry aware application of speed up. The results presented show the new architecture supports 20% higher throughput with 20% lower latency and 30% less interconnection area at approximately the same power consumption.

The rest of the paper is organized as follows: Section II surveys related work. Section III presents our architecture, describing in detail its key technologies. In Section IV we share relevant results to validate the effectiveness of our approach, while Section V summarizes our conclusions and findings.

II. RELATED WORK

Shared memory architecture has been explored in multicore and many core settings inside a cluster [13] using Mesh-of-Trees (MoT) topology giving single cycle access but at a very limiting frequency of 310 MHz and 256 Kbytes shared L1 memory in 65nm. A 4x8 MoT is also used in [13] where every level of fan-out dilutes the traffic conflicts by half but doubles the interconnect. As analyzed in [1], even though it can achieve 90% throughput the number of wires increases $O(4n^2)$ and wire crossings increase $O(16n^4)$ where $n$ doubles every routing stage.

In [8] the computing cluster has a 2 Mbytes shared memory in which wire density is reduced by dividing the memory into two sides and introducing a 4-by-2 routing switch for compute element pairs. Each pair has two memory buses (one for each side), which can be utilized in parallel by the
two CEs. The 4-by-2 routing switch reduces the interconnects from around 64 million connections to around 16 million, a 4X reduction, but the ideal throughput drop per port is only 6.25%. This enables 2MB of 550MHz shared memory in 28 nm HP. Some of this performance was due to the high regularity of layout where all the PEs are sandwiched between the memory banks located on the both sides. This regularity of the geometry can be very hard to find once we have many master ports and sea of memory banks spread all over the silicon.

In Dadiannao [2], a Fat tree topology is used inside each tile and the wires occupy almost half of the area. It can be utilized as a hierarchical architecture but global resource sharing is limited due to its intrinsic NUMA nature, which is not suitable for a shared memory architecture.

Flattened butterfly [6] topology can be a good candidate for the shared memory architecture if the size of shared memory is not too big and geometry can be regular, because it collapses all vertical switches and connections but leaves only horizontal connections among collapsed switches. However there are physical challenges once the size of shared memory grows bigger or the physical layout becomes irregular, which is driven by the surrounding heterogeneous PEs.

From the above examples we see that a judicious reduction in connectivity at the right places in the many port interconnect can have a dramatic improvement on area and performance with only little degradation in latency and in this paper we take steps to quantify and understand how this may best be done. To introduce the relevant concepts Fig. 1 gives an example of staged speed-up where \( n \) master ports sharing a logical memory connect to \( k \) memory ports and each memory port can connect \( r \) memory banks, which we define as memory speed-up of \( r \) because transactions that would normally collide at a memory port may now be able to continue onto different banks. When \( r = 1 \), this interconnect network is reduced to what we will call a conventional \( n \times k \) full-crossbar topology. Fig. 2 shows a conventional topology layout with 32 masters and 8 mega bytes of memory. We can observe that non uniform latency to the shared memory architecture is mainly caused by the big physical footprint of many instances of memory. Non-uniform access delay to area A, B and C is unavoidable and will worsen as the geometry becomes more irregular. Therefore, we must address this at the architecture level.

Interconnect has replaced transistors as the main determinant of performance, and this "tyranny of interconnection" will only escalate [10] as interconnect resistance and capacitance (RC) increasingly dominate delay [12]. As pointed out in [7], the number of wire crossings is also critical for the effectiveness and performance of a specific topology. In Fig. 1 if we assume \( n = k \) there are \( O(n^2) \) wires between master ports and memory ports, and there are \( O(n^3) \) wire crossings as analyzed in Formula (10). The number of wire crossings leads to routing congestion and low silicon utilization as shown as the "swimming pool" area in the middle of Fig. 2 where the utilization of interconnect is only a single digit.

III. Architecture

Our architecture takes the concepts of distributed shared memory [11] and extends it with the key technologies described below. All the technologies are effective individually, but provide the best benefits and results when they are applied together. For reasons that will become clear we call this memory architecture the Distributed Shared Memory Controller – DSMC [8].

A. Mathematical Modeling and Analysis on Speed-ups

For the topology shown in Fig 1 there are \( m = k \cdot r \) memory banks in total. Assume all masters and memory banks are running at the same frequency and all of the master requests are statistically independent and identical with probability \( P_a \). Then the probability a specific master port accesses a specific slave port is \( \frac{P_a}{k} \). Define \( P\{q\} \) to be the probability that there will be \( q \) requests at a specific slave port [14].

\[
P\{q\} = \binom{n}{q} \left(\frac{P_a}{k}\right)^q \left(1 - \frac{P_a}{k}\right)^{n-q} \tag{1}
\]

The expected number of requests that will leave the slave port towards the memory banks depends on how the slave port processes requests. If there are \( q < r \) requests to a slave port
then the utilization of the port will be \( f_r(q) \) due to random contentions at memory banks

\[
f_r(q) = r \left(1 - \left(\frac{r-1}{r}\right)^q\right)
\]  

(2)

When there are \( q \geq r \) requests to a slave port we assume that \( r \) requests are randomly chosen and kept for processing while the others are back pressured. This means that the utilization is the same as for \( r \) requests, \( f_r(r) \). So the expected utilization of the slave port is:

\[
E(k, n, r) = \sum_{q=0}^{r-1} f_r(q)P\{q\} + \sum_{q=r}^{n} f_r(r)P\{q\}
\]  

(3)

\[
= \sum_{q=0}^{r-1} f_r(q)P\{q\} + f_r(r)(1 - \sum_{q=0}^{r-1} P\{q\})
\]  

(4)

\[
= r \left[\left(1 - \left(\frac{r-1}{r}\right)^r\right) - \sum_{q=0}^{r-1} F(r,q)P\{q\}\right]
\]  

(5)

where

\[
F(r, q) = \left(1 - \left(\frac{r-1}{r}\right)^r\right) - \left(1 - \left(\frac{r-1}{r}\right)^q\right)
\]  

(6)

The utilization per bank from one interconnect network attached to that bank is then obtained by dividing by \( r \).

\[
E_B(n, r) = 1 - \left(\frac{r-1}{r}\right)^r - \sum_{q=0}^{r-1} F(r,q)P\{q\}
\]  

(7)

In our DSMC we connect \( r \) speed-up networks with one from each building block to share and access the \( nr \) banks together. This produces an \( nr \times nr \) interconnect in a distributed and modular manner. The bank utilization is

\[
U_B(n, r) = 1 - \left(\frac{r-1}{r}\right)^r + \sum_{q=0}^{r-1} F(r,q)P\{q\}\right)^r
\]  

(8)

Alternatively, the utilization of a memory bank for a fully connected \( nr \) port to \( kr \) port topology is \[14\].

\[
U_{flat} = 1 - \left(1 - \frac{\alpha}{kr}\right)^n \rightarrow 1 - e^{-\frac{\alpha}{kr}} \rightarrow 0.6321
\]  

(9)

Fig. [3] shows the case of \( n = k = 16 \) where Formula [9] is the blue line, and Formula [9] is the brown line. It shows the utilization of a memory bank in DSMC is lower than that of a fully connected topology. The drop starts from around 1% per memory bank when \( r = 2 \), to 3.6% when \( r = 3 \), and 5% when \( r \geq 4 \). However, the aggregated utilization per port with speed-up in DSMC is around 77% when \( r = 2 \), 75% when \( r = 3 \), 70% when \( r = 4 \) and 63% when \( r \geq 5 \). Correlate this fact with formula [9] and wire analyses in section [III-C] we can conclude the cost-effective and beneficial speed-up range for DSMC is from 2 to 4 where \( r = 2 \) offers the cost/performance ratio.

Note that in Fig. 4 the number of blocks in each level halves, the others are back pressured. This means that the utilization of memory bank when \( r \), to 3.6% when \( r = 3 \), 70% when \( r = 4 \) and 63% when \( r \geq 5 \). Correlate this fact with formula [9] and wire analyses in section [III-C] we can conclude the cost-effective and beneficial speed-up range for DSMC is from 2 to 4 where \( r = 2 \) offers the cost/performance ratio.

B. Hierarchical and Distributed Architecture with Less Wire Crossings

Fig. [4] shows the basis of a building block that DSMC32M32S is built upon. Formula [7] and [8] can be applied recursively across stages to calculate the throughput. The reason to use Radix 2 switches is they can significantly simplify the layout by reducing dependency among masters. They are more granular than higher index switches and work easily with irregular geometries on silicon. They also help simplifying memory addressing. Switches with index of 3 and beyond, have \([K,3]\) structure as a subgraph [15], making it very difficult to obtain the isomorphic graphs necessary to ease wire crossings. For a multi-stage 2-ary interconnect network, we have three types of crossings at each stage as shown Fig. [4] where each stage has \( n/(2g) \) independent blocks, with each block consisting of two independent crossbars that share the next stage input (as in the example above the banks were shared), each with \( g \) input and output ports:

- **Type A:** \( g/2 \) wires going from the masters on left side in a block connect to the slaves on the right side cross the wires from masters on the right connect to the slaves on the left side as shown as the purple dots in Fig. [4]. This happens once per block and leads to \( g^2/4 \) crossings.

- **Type B:** A master "self" crossing its own internal master to slave connections in the same side. They are shown as the green dots in Fig. [4]. This happens twice per block and leads to \( 2*1 = 2(g/2 - 1) + (g/2 - 2) + \ldots + 1 = g(g-2)/4 \) crossings in total.

- **Type C:** is a slave "self" crossing where two bundles arriving at the same set of slave ports cross coming from different bundles of master ports. Also shown as the red dots in Fig. [4]. As for Type B this leads to \( g(g-2)/4 \) crossings.

The total number of wire crossings among all \( n \) masters and \( k \) memory ports shown in Fig. [4] is, for \( n = k \):

\[
Cr_{kn} = \binom{n}{2} \times \binom{n}{2} = \frac{n^2 \times (n-1)^2}{4} \sim O(n^4)
\]  

(10)

Note that in Fig. 4 the number of blocks in each level halves,
and therefore $g$ doubles, at each stage. For example, there are $n$ ports in the first stage which has $n/4$ crossbar pairs and $g = n/8$. In general the total crossings of a 2-ary based network is

$$C_{n}^{(r=2)} = \frac{\log_{2} n - 1}{2} \sum_{i=1}^{n/8-1} \left(3 \cdot 2^{i} - 4\right) + \frac{3n}{4}$$

Because the "bank sharing" decreases utilization at each stage, we doubled the connections from the second stage onward, so we must multiply the wire crossing count in all stages except the first by 4. This gives the modified crossing count for a building block in DSMC:

$$C_{BxB}^{(r=2)} = 2 \left[ 2n + 4 \sum_{i=1}^{n/8-1} (n - 8i) \right] + \frac{n}{2}$$

For a $32 \times 32$ DSMC, shown in Fig. 3, we divided it into $2 \times 16 \times 16$ blocks and then connected them together with 2 ports going from each stage to its sister stage on the other side, crossing the main highway of $2n$ input ports into the DSMC 4 times and also each other twice. The wire crossings between the two building blocks are:

$$R = \frac{n^{2}(2n - 1)^{2}}{2C_{n}^{(r=2)} + C_{BxB}^{(r=2)}}$$

$$= \frac{n^{2}(2n - 1)^{2}}{\sum_{i=1}^{\log_{2} n - 1} (3 \cdot 2^{i} - 4) + 8 \sum_{i=1}^{n/8-1} (1 - 8i/n) + 3}$$

For this architecture, $n = 16$ in formula (15) gives $R = 415.6$. if we reasonably assume that each wire in this calculation represents a bus which normally consists of around 200 physical wires, the physical wire crossing saving is about $400 \times 200^2$, a seven orders of magnitude reduction, leading to significant area saving in the physical implementation results in the next section.
that receives the burst request in building block 0 breaks the even and odd beats of the request into 2 request groups and sends one each to the upper and lower sides (1 and 2, \textit{directed randomization}). In the lower (upper) side the even (odd) request streams are spread in round robin order to all the blocks of the next stage for the first two levels of radix switches to make sure two beats within the same burst reach different banks (3 and 4, \textit{fractal randomization}). This not only improves average access latency, but will mediate the NUMA effects since it averages out the access latency within a burst request. This is validated by the RTL simulation results in section IV-A.

Speed-up is shown in red in Fig. 5. All the first level switches send speed-up traffic to their sister building block as indicated as 2 and also receive speed-up traffic as indicated by 5. All the necessary address decoding for memory banks are done in the first level of the switches in the building block where the requests are originally generated, thus the traffic from other building block(s) can be merged in directly to every the second level switches.

There is an extra independent interconnect network for a speed up of 2 from the level two switches all the way to the memory banks. The blue switches are modified to handle two streams of traffic independently in parallel and the connections among switches and memory banks are all doubled to serve two times of traffic.

IV. RESULTS

DSMC-32M32S is prototyped with 4 Mbytes of shared memory and one speedup network (\(r = 2\)) in each building block. Synopsys tool suite is used for synthesis, timing closure and physical design, and the design is timing closed above 600 MHz on a 16nm technology node. The data points for comparisons are provided by Huawei Wireless in production settings to properly compare our results and show the benefits. We categorize this group of data as Conventional Memory Controller (CMC) data.

A. RTL Simulation Results

As shown in Fig. 6, the stimulus is generated using uniform random memory access for each traffic pattern and the traffic is applied to each and every master port at the same time. Fig. 6 shows the throughput comparisons with different traffic patterns for the read and write accesses. DSMC has almost the same performance when traffic patterns are single and burst 2, but it starts to have over 20% of combined read and write throughput improvement for the longer bursts beyond 4, and it has about 20% improvement for the mixed traffic as well.

Fig. 7 shows average latency comparison. As expected, the average latency is almost the same between the two architectures when the traffic load is low. However, the average latency from CMC starts to degrade once the injection rate is over 60% versus DSMC can handle heavy traffic much better. DSMC has very slow rising curves for both read requests and write data, and the average access latency still maintains less than 60 clock cycles even when 100% injection rate is applied. As discussed in section III-C, sometimes we insert register slices for timing closure due to the widely spread nature of the layout. This makes the design more NUMA. Results are shown in Fig. 8. With the randomization techniques described in section III-C the write throughput actually improves slightly. The read throughput drops for the burst 8 but burst 2 read improves. This set of results not only correlates well with the findings presented in [5], but also shows that DSMC is resilient to register slice insertion.

B. Physical Design and Power Estimation

In a generic industry setting, DSMC-32M32S with two building blocks is always a challenge for any physical design EDA tool. DSMC is very physical design friendly because it works seamlessly with the hierarchical physical design flow. The entire physical design can be split into two parts and be handled in parallel: one for the top level where each building block is abstracted as a black box with accurate I/O timing;
the other is at building block level where the majority of design resides. One step further, only one rather than two building blocks needs to go through the physical design. Therefore DSMC can significantly improve end-to-end SoC design experience and overall schedule.

Fig. 9 shows how flexible DSMC can adapt to one of extreme layout constraints where all 32 master access ports are located right in the middle of the left edge. To further stress the architecture, the entire design is taken into the EDA tool all together. A decent result is still obtained because of the physical design awareness of the architecture. The utilization for the area located at middle toward left edge is close to 30% with less congestion as indicated in the side window. It saves about 30% silicon area for the interconnect network compared with that of CMC. The multiple level of simple radix switches enable the data path logic to navigate the sea of memory banks easily to reach all the challenging locations across the layout. This result validates the effectiveness of using lower index switches for timing closure since the timing paths are less dependent on each other.

The power consumption is also estimated and compared against the data provided in production setting. The activity vectors are obtained from the same application traces and Synopsys PTPX flow is used to report and compare power consumption. The power consumption is almost the same between DSMC and that of CMC however with different distributions. One observation is that DSMC has 50% more registers than that of CMC versus CMC has more combinational logic than that of DSMC. This result really challenges the industry rule of thumb at least for the wire dominate situation where more registers doesn’t always imply more power.

V. CONCLUSIONS AND FUTURE RESEARCH DIRECTIONS

We present a new shared memory architecture – DSMC and validate its benefits. The results show DSMC supports 20% higher throughput with 20% lower latency, 30% less interconnection area and almost the same power than that of the existing solution. DSMC can easily scale up its capacity by 2x with a much easier implementation flow.

Moving forward, we actively look forward to further improving the access latency, support even more shared memory and access ports with 3D integration techniques. Meanwhile, we will explore how to leverage this architecture in the area of Non-Uniform Cache Access because of the similarities between NUMA and NUCA.

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