FPGA controlled five level soft switching full bridge DC-DC converter for high power applications

J. Sivavara Prasad1*, Y.P. Obulesh2 and Ch. Sai Babu3

Abstract: The objective of the paper is to develop soft switching for the novel five level full bridge DC-DC converter for high power applications. The use of conventional DC-DC converter is likely to decrease the efficiency because of the hard switching, which generates losses during the switch on/off. This paper mainly deals with the development of zero voltage and zero current switching for five level full bridge DC-DC converter. The proposed topology will provide five level DC-DC output voltage, thereby the size of filter in both input and output sides will get reduced as compared to the existing topologies. By increasing the voltage levels, the stress across each switch and DC filter in the rectifier side will get reduced. Only eight switches are used for generating five levels in the proposed converter topology which reduces cost and also total switching losses, thus improves the overall efficiency of a system and it is very much suitable for high power DC-DC applications. The control signals for the proposed converter are developed from the Field Programmable Gate Array. The simulation and experimental results are presented for prototype model of 500 W.

Keywords: zero voltage switching (ZVS); zero current switching (ZCS); full bridge DC-DC converter; field programmable gate array; soft switching converters

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PUBLIC INTEREST STATEMENT
This paper consists of the design, development, and verification of a two-stage converter for high power DC-DC applications. The first stage consists of soft-switching interleaved DC-AC converter and it converts battery input to 1-phase five levels AC voltage. The second stage is a rectifier which provides required DC voltage for high power load applications. The proposed DC-DC converter will provide electrical isolation between battery and load; thereby the changes made in the load may not affect the battery due to isolation. This scheme provides low switching and conduction losses and high efficiency. Because of 1-phase five levels inverter voltage in DC-AC stage, the size of filter in the input and load side will be reduced to a greater value.
1. Introduction

A Three-Level Full-Bridge Zero-Voltage Zero-Current Switching Converter with a Simplified Switching Scheme (Carr, Rowden, & Balda, 2009) is having eight control switches for generating three levels. The size of the filter elements in this paper is high and more number of switches are required for three level operation, hence the cost is high. The Three-Level Combined DC-DC Converter without Added Primary Clamping Devices contains six control switches for three level dc-dc converter operation (Carr et al., 2009; Chen & Ruan, 2008; dos Santos Garcia Giacomini, Scholtz, & Mezaroba, 2008; Lin & Chao, 2013; Lin, Huang, & Wan, 2008; Mousavi, Das, & Moschopoulos, 2012; Nabae, Takahashi, & Akagi, 1981; Shi & Yang, 2014, 2016; Tolbert & Peng, 2000; Wu, Zhang, Ye, & Qian, 2008).

The controlled switches such as IGBTs and MOSFETs are having many advantages in terms of speed of response and system size but these switches are unable to operate at high voltages. The advantages of these smaller size, faster responses, different multi level topologies are been proposed (Choi, Cho, & Cho, 1991; Lai & Peng, 1996; Loh, Holmes, Fukuta, & Lipo, 2003; Wang, Su, Jiang, & Lin, 2008; Zhang, Peng, & Qian, 2004) in order to reduce the voltage across each switching device. The different multi level topologies are flying capacitor, diode clamped and cascaded converters are providing for division of voltage across the switching devices (Loh et al., 2003). During the switching instants, the losses in the switching converter will become increased by increasing the switching frequency. The soft switching converters are proposed in order to reduce the switching losses.

The multi level inverter (Loh et al., 2003) is used to produce the stress across each switch. But this converter is not operating under soft switching scheme. Hence, the switching losses are high and efficiency becomes poor. To overcome all these problems, the proposed five level full bridge zero voltage current switching dc-dc converter is suitable.

In this paper, a soft switching technique has been proposed for five level full bridge converter which reduces total switching losses. The proposed work has been implemented effectively and it is verified through simulation and experimentation results. Because of five level operation, the size of dc filter elements are reduced to a greater value and this topology is very much suitable for high power applications. As voltage levels increases, the stress across a switch and filter size in the dc rectifier gets reduced. Only eight switches are used in proposed converter topology which reduces cost and also total switching losses, thus improves the overall efficiency of a system. The control signals for the proposed converter are developed from the Field Programmable Gate Array.
2. Five level full bridge ZVZCS DC-DC converter

Figure 1 shows the circuit diagram of the proposed five level full bridge DC-DC converter topology. Table 1 gives the proposed switching states and the corresponding output of the transformer for each switching state. The switching frequency is fixed and each switch is ON for exactly half a switching cycle and turn on and turn off of each switch is controlled, so that the DC-bus voltage is applied across the transformer for the desired time. If the switches S1, S4, S5 and S8 are operating or if the switches S2, S3, S6 and S7 are operating then the transformer primary voltage becomes zero. If the switches S1, S2, S5 and S6 are operating then the transformer primary voltage becomes \( V_{DC} \). If the switches S3, S4, S7 and S8 are operating then the transformer primary voltage becomes \(-V_{DC}\). If the switches S1, S5 and S6 are operating or if the switches S2, S5 and S6 are operating then the transformer primary voltage becomes \( V_{DC}/2 \). If the switches S3, S7 and S8 are operating or if the switches S4, S7 and S8 are operating then the transformer primary voltage becomes \(-V_{DC}/2\). Here, the switches S1–S8 are operating under ZVS switching during the time of turn-off and ZCS during the time of turn-on. The filter elements \( L_f \) and \( C_f \) are used to remove the ripple content in the rectifier output voltage.

If the converter is in state 3, then the average voltage at the rectifier will be

\[
V_0 = \frac{D \times V_{DC}}{n}
\]  

(1)

where \( n \) is the turn’s ratio of the transformer. This provides the desired DC voltage conversion and shows that the system operates as a transformer zed buck converter. This topology is an advantage compared to other 3 L FB soft-switching topologies which require complex switching control schemes, such as double-phase-shifted control. The proposed converter is operating in three, four and five level DC-DC operation.

Table 2 shows the comparison of proposed five level DC-DC converter with conventional DC-DC converter. It is clear that, the number of switches in the proposed converter is less than the conventional converter (i.e. cascaded). So, the efficiency of the proposed converter is high and the size of DC side filter is less as compared to conventional.

| Type of element          | Cascaded multi level converter (Loh et al., 2003) | Proposed |
|--------------------------|--------------------------------------------------|----------|
| Main switches            | \((m-1) \times 2\)                               | \((m-1) \times 2\) |
| Main diodes              | \((m-1) \times 2\)                               | \((m-1) \times 2\) |
| Gate-Amp                 | \((m-1) \times 2\)                               | \(m\)     |
| Switching losses         | High                                             | Low      |
| DC-Link capacitors       | Isolated                                         | Bulk capacitors |
3. Operation modes
The operational waveforms of the proposed DC-DC converter are shown in Figure 2. The various operating modes of the five level converter are as follows.

Figures of 3–14 show the operational modes of the ZVZCS DC-DC Full bridge converter. The following analysis is made based on the assumption that the blocking capacitors are large enough to act as a constant voltage source.

3.1. Operational mode 1: \( t_0 \leq t \leq t_1 \)
At time \( t = t_0 \), the switch \( S_1 \) is turned on under ZVS and \( S_5 \) is turned on under ZCS and transformer primary does not receive any DC voltage as shown in Figure 3. In this instant, the primary voltage of the transformer is zero and hence the DC rectified output voltage becomes zero.
Figure 4. Operation mode 2 ($t_1 \leq t \leq t_2$) of the proposed converter.

Figure 5. Operation mode 2 (before time $t = t_2$) of the proposed converter.

Figure 6. Operation mode 3 ($t_2 \leq t \leq t_3$) of the proposed converter.
3.2. Operational mode 2: $t_1 \leq t < t_2$

At time $t = t_1$, the switch $S_8$ is turned off under ZVS and switch $S_6$ is turned on under ZCS and thereby the switch $S_8$ is turned off automatically under ZCS. The capacitor $C_2$ starts discharging through the current in the primary winding of the transformer and hence the transformer primary receiving half of the input voltage with positive polarity as shown in Figure 4 and the capacitor $C_4$ starts charging with the direction of current in the circuit. Before time $t = t_2$, the capacitor $C_2$ is completely discharged to zero, so its body diode $D_2$ starts conducting. And it is shown in Figure 5. If the switch $S_2$ is triggered at this instant then it is operating under ZVS.

Switches $S_1$ and $S_5$ can be gated ON under complete at any time after $t_2$. The duration of this mode is related to the voltage conversion ratio by the duty cycle parameter $D$, which is given by

$$\frac{V_0}{V_{DC/2}} = \frac{D}{n} = \frac{((t_{ON})(T_{sw}/2))}{n} = \frac{(t_2 - t_1)/(T_{sw}/2)}{n}$$

(2)

Since interval $t_1$ is so short, $t_{ON}$ is set equal to $t_2$ and...
Figure 9. Operation mode 5 ($t_4 \leq t \leq t_5$) of the proposed converter.

Figure 10. Operation mode 6 ($t_5 \leq t \leq t_6$) of the proposed converter.

Figure 11. Operation mode 6 (before time $t = t_6$) of the proposed converter.
Figure 12. Operation mode 7 ($t_6 \leq t \leq t_7$) of the proposed converter.

Figure 13. Operation mode 7 ($t_7 \leq t \leq t_8$) of the proposed converter.

Figure 14. Operation mode 8 (before time $t = t_8$) of the proposed converter.
3.3. **Operation mode 3: t_2 \leq t < t_3**

At time $t = t_2$, the switch $S_2$ is turned on under ZVS along with the conducting switches $S_1$, $S_5$, and $S_6$ then the transformer primary receiving full DC input voltage. The rectifying diode $D_1$ is operating and the rectified voltage is supplied to DC load as shown in Figure 6.

At $t = t_2$, switches $S_1$, $S_2$, $S_5$, and $S_6$ being conducting and $(V_{DC})$ is applied to the primary of the transformer. As a result the primary current rapidly rises from 0 to the reflected output current.

\[ I_{P0} = \frac{I_0}{n} \]

where $I_{P0}$ is the peak value of the primary side current going into the transformer, $I_0$ is the current through $L_f$, and $n$ is the turns ratio of the transformer. The voltage applied to the transformer leakage inductor $L_{lk}$ during this period is $V_{DC}$, and the duration of this period is

\[ t_2 - 0 = t_1 = \frac{L_{lk} \times I_{P0}}{V_{DC}} \]

The load current is not completely supplied by $V_{DC}$ during this period, so the excess current freewheels through the secondary rectifier diode $D_1$.

3.4. **Operation mode 4: t_3 \leq t < t_4**

At time $t = t_3$, the switches $S_2$, $S_5$, and $S_6$ are operating then the transformer primary receiving half of the input voltage and simultaneously the switch $S_1$ is turned off under ZVS. The rectifying diode $D_1$ is operating and the rectified voltage is supplied to DC load. The capacitor $C_1$ starts charging and capacitor $C_3$ starts discharging as shown in Figure 7. Assume the width of time between $t_3$ and $t_4$ is long enough to make discharging of capacitor $C_3$ to zero and correspondingly its body diode of $D_3$ is on as shown in Figure 8.

3.5. **Operation mode 5: t_4 \leq t < t_5**

At time $t = t_4$, the switch $S_3$ is turned on under ZVS and switch $S_7$ is turned on under ZCS whereas the switch $S_5$ is turned off under ZCS and it is shown in Figure 9. So, the transformer primary receiving zero voltage and correspondingly the rectified output voltage becomes zero.

3.6. **Operation mode 6: t_5 \leq t < t_6**

At time $t = t_5$, the switch $S_3$ is turned on under ZCS then the transformer primary receiving half of the input voltage in the reverse direction and simultaneously the switch $S_3$ is tuned off under ZVS and switch $S_6$ is turned off automatically under ZCS as shown in Figure 10. The rectifying diode $D_2$ is operating and the rectified voltage is supplied to DC load. The capacitor $C_4$ starts charging and capacitor $C_3$ starts discharging. Before time $t = t_5$, the capacitor $C_3$ is completely discharged to zero and correspondingly the body diode of switch $S_3$ is on and it shown in Figure 11.

3.7. **Operation mode 7: t_6 \leq t < t_7**

At time $t = t_6$, the switch $S_4$ is turned on under ZVS then the transformer primary receiving full DC input voltage in the reverse direction as shown in Figure 12. The rectifying diode $D_2$ is operating and the rectified voltage is supplied to DC load.

3.8. **Operation mode 8: t_7 \leq t < t_8**

At time $t = t_7$, the switch $S_4$, $S_7$, and $S_8$ are operating then the transformer primary receiving half of the input voltage in the reverse direction and simultaneously the switch $S_4$ is tuned off under ZVS as

\[ D = \frac{t_2}{T_{sw}/2} \]
shown in Figure 13. The rectifying diode $D_2$ is operating and the rectified voltage is supplied to DC load. The capacitor $C_1$ starts charging and capacitor $C_3$ starts discharging. Before time $t = t_p$, the capacitor $C_1$ is completely discharged to zero and correspondingly the body diode of switch $S_1$ is on.

4. Design equations

The design of the converter involves determining values for $C_{DC1}$, $C_{DC2}$, $C_1$, $C_2$, $C_3$, $C_4$, $L_{lk}$, and the output filter. The output filter should be large enough to maintain the load current for the entire switching period $T_{sw}$ while the transformer leakage inductance $L_{lk}$ should be minimized in order to minimize the reset time. Beyond these restrictions, transformer and filter design principles also apply.

Capacitors $C_{DC1}$ and $C_{DC2}$ are essential for the proper voltage division across the switching devices. Consequently, they should be selected with identical values using tight tolerance parts. In practice, the DC-bus capacitors are required to maintain the voltage through changes in the input voltage $V_{DC}$ using voltage spikes caused by parasitic inductances, so a large value may be required. Smaller capacitors with high-frequency response may be placed in parallel with the bulk DC-bus capacitors in order to handle high-frequency ripple due to parasitic components.

Figure 2 shows that they conduct during mode 3 and its mirror mode 8. These capacitors must maintain a near-constant voltage during the entire cycle; thus, they should be selected so that they do not experience more than a 5% voltage change during mode 3. Each capacitor conducts $I_{P0}/2$ during mode 3, and its nominal voltage is $V_{DC}/2$.

The size of the parallel capacitors, $C_r$, is determined by the minimum requirement to achieve ZVS during turn-OFF, which requires that the parallel capacitors must be large enough to hold the voltage close to zero during the current fall-time of the device $t_{fi}$, which can be determined from the data sheet. Once this parameter has been determined, $C_r$ can be calculated as follows

$$C_r = \frac{t_{fi} \times I_{P0}}{V_{DC}} \quad (6)$$

A large value of $V_{stop}$ is desirable in order to quickly reset the primary current during mode 4, but for the “OFF” devices, is seen as $(V_{DC} + V_{stop})/2$ at the end of mode 2. Thus, the value of $V_{stop}$ should be limited to one-fifth the DC-bus voltage in order to limit the voltage stress on the devices. Capacitor $C_{b0}$ is charged from $-V_{stop}$ to $+V_{stop}$ during mode 2 by $I_p$ at a value of $I_{P0}$.

4.1. Soft-switching range

ZVS is accomplished when $I_{so}$ discharges the parallel capacitors across the leading switches during mode 3. The length of mode 3, referred to as the dead time, limits the maximum duty cycle that can be commanded by the controller, which, in turn, limits the maximum voltage that can be achieved on the secondary and the maximum power that can be delivered to the load. Since ZVS, and hence the dead time occurs twice per half cycle, the maximum duty cycle is

$$D_{max} = 1 - 2 \times \frac{t_{dead}}{T_{sw}/2} \quad (7)$$

Once the dead time is fixed, there is a minimum value of the load current under which ZVS no longer occurs since the leading switches will be switched before the parallel capacitors are completely discharged. This minimum load current is given by

$$I_{P0,min} = C_r \times \frac{V_{DC}}{t_{dead}} \quad (8)$$

The dead time must not only be selected to maximize the load current range for which ZVS occurs but must also minimize the reduction of the duty cycle. The precise value of the dead time will vary.
depending upon the needs of the application, i.e. whether the application will require high duty cycles or a large soft-switching range.

ZCS is accomplished when the blocking capacitor voltage drives the primary current to zero before the state change occurs at \( T_{sw}/2 \). The current begins to be reset at \( t_2 = D \times T_{sw}/2 \), so the total time available to reset the current is

\[
T_{reset,\text{max}} = (1 - D) \times \frac{T_{sw}}{2}
\]  

(9)

ZCS will be achieved if the reset period from (6) is less than \( T_{reset,\text{max}} \), and using the value for \( V_{cb0} \) from (12)

\[
\frac{4 \times f_{sw} \times C_{DC1} \times L_{ik}}{D} \leq (1 - D) \times \frac{T_{sw}}{2}
\]  

(10)

It can be noted from this equation that achieving ZCS is independent of the load current, though the voltage across \( C_{cb0} \) may become very large if the primary current exceeds the maximum load current used in (6) to calculate the value of the blocking capacitor. There is a limit to the range of duty cycles for which ZCS occurs, given by

\[
1 - \sqrt{1 - 32 \times f_{sw}^2 \times C_{DC1} \times L_{ik}} \leq D \leq 1 + \sqrt{1 - 32 \times f_{sw}^2 \times C_{DC1} \times L_{ik}}
\]  

(11)

5. Simulation results of the five level ZVZCS DC-DC converter

The parameters of the proposed converter are shown in the Table 3. The gate signals of the proposed converter are shown in Figure 15. In the proposed converter, there are total of five control switches. For getting positive output, the diagonal switches (\( S_1 \) and \( S_2 \)) will operate along with switch \( S_5 \) and input voltage is applied to primary of the transformer. Similarly for getting the negative output, the other diagonal switches (\( S_3 \) and \( S_4 \)) will operate along with \( S_5 \) and negative voltage is applied to the primary of the transformer. All the control switches in the proposed converter are operating under soft switching.

The control signals for the switches have been developed and as shown in Figure 15. The dead band is created between the signals \( S_1 \), \( S_5 \), \( S_3 \), and \( S_4 \) to achieve the ZVS condition.

ZVS is accomplished when primary current discharges the parallel capacitors across the leading switches during dead band time.

\[
I_{P0,\text{min}} = C_s \times \frac{V_{DC}}{t_{\text{dead}}}
\]  

(12)

| S. No. | Parameter              | Range   |
|--------|------------------------|---------|
| 1      | DC input voltage       | 200 V   |
| 2      | DC output voltage      | 24 V    |
| 3      | Switching frequency    | 10 KHz  |
| 4      | Load current           | (1–20) A|
| 5      | DC bus capacitance     | 100 mF  |
| 6      | Parasitic capacitance  | 1 PF    |
| 7      | Filter inductor        | 10 mH   |
| 8      | Filter capacitor       | 5 uF    |
Figure 15. Gate pulses for five level DC-DC converter. (a) Gate pulse of switch $S_1$ and $S_2$, (b) Gate pulse of switch $S_3$ and $S_4$, (c) Gate pulse of switch $S_5$ and $S_6$, and (d) Gate pulse of switch $S_7$ and $S_8$.

Figure 15 shows the control pulses for the proposed five level DC-DC converter. Suppose at the time $t = 2.6$ ms, the pulse is given to switch $S_2$ then the voltage across the switch is zero. Similarly at this time, the pulse for switch $S_3$ is off then the voltage across the switch is equal to the supply voltage. So, the Switches $S_3$ and $S_2$ are receiving inverted pulses. But switch $S_1$ is ON at $t = 2.62$ ms and is OFF at $t = 2.63$ ms. The normal switches $S_1$–$S_4$ are operating under frequency ($f$) but the auxiliary switch $S_5$ is operating under frequency ($f/4$).

Figure 16. Transformer primary and secondary voltages.
Figure 16 shows the transformer primary and secondary voltages of the converter circuit. If switches $S_1, S_2$ are in conduction then the transformer primary voltage is $V_{DC}$ from 2.03 to 2.05 ms. If switches $S_1, S_5$ are in conduction then transformer primary voltage becomes $V_{DC}/2$ from 2.01 to 2.03 ms. If switches $S_3, S_4$ are in conduction then transformer primary voltage is $-V_{DC}$ from 2.18 to 2.2 ms. If switches $S_3, S_5$ are in conduction then transformer primary voltage is $-V_{DC}/2$ from 2.16 to 2.18 ms. If t switches $S_1, S_3$ or $S_2, S_4$ are in conduction then the transformer primary voltage becomes zero.

Figure 17 shows the DC output voltage of five level DC-DC converter. If the 200 V DC input voltage is given to five level DC-DC converter then the transformer primary gets five levels these five levels are step down to 24 V by using step down transformer. The output voltage of the transformer is rectified by using diode bridge rectifier and this rectified voltage is filtered by using L-C filter and finally get the DC output voltage of 24 V across load.

Figure 18. (a) Gate pulse and voltage across switch $S_3$ from OFF to ON and (b) Gate pulse and voltage across switch $S_3$ from ON to OFF.
Figure 18(a and b) shows the gate pulse and voltage across $S_3$. If the switch $S_3$ is on at time $t = 2.06 \text{ ms}$, the voltage across the switch is zero before time $t = 2.06 \text{ ms}$. If the switch $S_3$ is off at time $t = 3.3 \text{ ms}$, the voltage across the switch is reached zero before time $t = 3.3 \text{ ms}$. So, it indicates that the switch $S_3$ is operating under ZVS condition. In a similar manner, the switches $S_1$, $S_2$, and $S_4$ are operating under ZVS.

Figure 19(a) and (b) shows the gate pulse and current through switch $S_5$. If the switch $S_5$ is on at time $t = 2.77 \text{ ms}$, the current through the switch is zero before time $t = 2.77 \text{ ms}$. If the switch $S_5$ is off at time $t = 2.79 \text{ ms}$, the current through the switch is reached zero before time $t = 2.79 \text{ ms}$. So, it indicates that the switch $S_2$ is operating under ZCS condition. In a similar manner, the switches $S_6$, $S_7$, and $S_8$ are operating under ZVS.

Figure 20. Efficiency for different load currents.
5.1. Five level- with soft switching

Table 4 shows the efficiency and output power of proposed converter with soft switching. For suppose a load current of 10 Amps, the efficiency of the converter is 89.2%. With soft switching. So, if the converter is operating under soft switching, the switching losses are decreases and efficiency is increased and it is shown in Figure 20 for different load currents. The Table 5 shows the values of filter elements for different voltage levels of the proposed converter. As the voltage levels increased then the size of filter elements will get reduced.

6. Hardware implementation of FPGA based control of ZVS DC-DC converter

Figure 21 shows the hardware implementation of the FPGA controlled zero voltage and zero current switching five level DC-DC converter. The hardware kit consists of the following parts:

- FPGA kit to generate the control signals.
- Driver Circuit to strengthen the control pulses of FPGA kit.

| Table 4. Efficiency of proposed converter for various load currents |
|-----------------|-----------------|-----------------|-----------------|
| S. No. | Load current (Amps) | Output power (Watts) | Input power (Watts) | Efficiency (%) |
|-------|---------------------|---------------------|---------------------|----------------|
| 1     | 3                   | 80.55               | 86.9               | 92.7           |
| 2     | 5                   | 134.6               | 144.3              | 93.3           |
| 3     | 10                  | 261.8               | 278.0              | 94.2           |
| 4     | 16                  | 420                 | 441.7              | 95.1           |
| 5     | 20                  | 523.3               | 548.0              | 95.5           |

| Table 5. Filter elements for different voltage levels |
|-----------------|-----------------|
| S. No. | Inverter level | Selection of filter elements |
|-------|----------------|-----------------|
| 1     | 3               | L (mH) | C (uF) |
|       |                 | 25     | 100   |
| 2     | 4               | 20     | 50    |
| 3     | 5               | 10     | 5     |
Figure 22. Gate pulses for the proposed DC-DC converter (voltage of 10 V/div and time of 25 μS/div).

(a)

(b)

(c)

(d)

Figure 23. Transformer primary voltage (voltage of 100 V/div and time of 25 μS/div).
6.1. Hardware results

Figure 22 shows the control pulses for inverter circuit with 10 KHz frequency. These pulses are getting from driver circuit. The driver circuit is used to amplify the pulse coming from FPGA controller and also, the driver circuit will provide isolation between low power and high power terminals of the switch.

Figures 23 and 24 show the transformer primary and secondary five level voltages of the proposed DC-DC converter and the levels are $+V_{dc}$, $+V_{c/2}$, zero and $-V_{dc}$ and $-V_{c/2}$.

Figure 25 shows the voltage across switch $S_3$. Channel 2 shows the pulse given to the switch and channel 1 represents the voltage across drain and source terminals of the switch. From Figure 26, it

- 12 and 5 V DC power supply circuits.
- Power circuit.
is evident that before turning-ON the switch $S_3$, voltage across it becomes zero. So, the switches are turned on under ZVS condition. Figure 13 (ii) shows the condition for ZVS of the switch $S_3$ during turn on to off period. The channel 2 indicates gate pulse and channel 1 indicates the voltage between drain and source terminals of switch.

The rectifier output voltage is fed to the capacitor filter. The output of the filter is pure DC as shown in Figure 27 and it is equal to 24 V for arc welding applications.

7. Conclusion

This paper proposed a five level full bridge zero voltage and zero current switching DC-DC converter scheme in which all the main switches are operating under soft switching. Hence, the switching losses are reduced. The proposed topology has been suitable for three, four and five level operation with only eight control switches. By increasing the voltage levels, the size of the filter elements and voltage stress across switches were reduced. The control signals for the proposed converter was generating from field programmable gate array. The proposed work has been implemented and it was verified through simulation and experimentation results. Hence, there is scope for developing soft switching mechanism for various multi level topologies also. This topology is very much suitable for high power DC-DC applications.

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