Performance analysis of double tail dynamic comparators

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Abstract : Low power high speed and high precision comparator circuits are studied. Dynamic comparators are key building block for the implementation of analog to digital converters, sense amplifiers. High precision, low voltage operation, lower power consumption, high speed, less offset voltage and more reliability are some of the important factors in designing the dynamic comparators. Since one circuit cannot provide all the mentioned properties, attempt is being made to study the performance of some dynamic comparators and compare their properties to ease the selection of suitable comparator circuit depending on the application. The circuits were rebuilt using GPDK (General Purpose Design Kit) 180nm CMOS technology in Cadence virtuoso tool.

1. INTRODUCTION

The demand for high speed high precision comparator operating at low voltage and high frequencies is increasing because of advanced analog to digital converters (ADC), sense amplifiers and high speed I/O circuits. Dynamic comparators are superior to static counterpart because of positive feedback which increases latching speed and lower static power consumption. The cmos dynamic comparator has two parts pre-amplifier and dynamic latch respectively. The pre-amplifier design determines offset voltage and latch determines the speed of comparator. If offset voltage is reduced, it directly helps in improving precision. This requires the large sized input transistors of pre-amplifier which increases the parasitic capacitance and thus the power consumption. The common mode voltage is applied at the input to operate input transistors in saturation which helps in increasing the speed but variation of common mode input voltage results in variability in delay significantly which makes the circuit not suitable for high speed operations.

Different methods have been proposed so far by various authors to reduce power consumption, increase speed and precision of comparator circuit. Extra circuit is added to provide clock gating [1], some techniques focus on improving the preamplifier circuit to reduce offset [2] while keeping the latch to work as it is, while some focuses on improving dynamic latch to enhance speed [4]. Some techniques provide zero static power consumption [3] but however speed is compromised. The special clocking technique to reduce the power dissipation is mentioned in [5]. Design techniques for high-speed, high resolution comparators is discussed in [7]. The bulk tuned calibration technique is also used to increase precision while keeping the size of input transistors small, but the speed gets affected [8]. Many architectures of comparator circuits are reported in [9-17].

In this paper, the attempt is being made to understand some popular dynamic comparator circuits proposed by various authors and compare their characteristics. It will help in selecting the right
2. CONVENTIONAL DYNAMIC COMPARATOR

The two-stage conventional dynamic comparator is presented in Figure 1a and Figure 1b. The bottom circuit is pre-amplifier and top half is dynamic latch in Figure 1a and vice versa in Figure 1b. Figure 1a represents NMOS type preamplifier and Figure 1b represents PMOS at input preamplifier. Consider Figure 1a to understand the operation of conventional dynamic comparator. CLK and CLKbar are the clock signals provided to make the circuit work in two phases, reset phase and evaluation phase respectively. When CLK = 0 and CLKbar = 1, till 10ns for circuit shown in Figure. 2, M7 and M8 charges the Dp and Dn node to Vdd since M11 is OFF. This also makes M5 and M6 ON, thus OUTp and OUTn nodes are discharged to Gnd. This is called reset phase. During evaluation phase CLK = 1 and CLKbar = 0, after 10ns as shown in Figure 2, the pre-amplifier amplifies the differential signal applied at the two input transistors M9 and M10 respectively, this creates difference at Dp and Dn levels which then gets amplified further by M5 and M6. This difference is the input for the two cross coupled inverters present in dynamic latch which further converts it to Vdd and Gnd because of positive feedback nature as shown in Figure 2. Thus, the circuit performs as a comparator as it produces the output based on the difference in input signal. During evaluation phase, preamplifier keeps on working even if the correct value is latched, this leads to power dissipation. The operation of conventional dynamic comparator represented in Figure 1b is shown graphically in Figure 3a and 3b.

![Figure 1. Conventional dynamic comparator](image)

![Figure 2. Output waveform of conventional dynamic comparator](image)
3. REVIEW OF VARIOUS DYNAMIC COMPARATOR

The conventional comparator can further be optimized to achieve more speed, lesser power, to reduce the offset voltage or to have more common voltage range without affecting the stability. Various authors have proposed modified comparator circuits with different architecture or design. We made an attempt to compare some of the comparators which are good in one or more parameters those are power consumption, delay, offset and the maximum operational frequency.

3.1. Comparator with clock gating

Figure 4. Low-Power Technique for Dynamic Comparator [1]

A. Khorami and M. Sharifkhani reported the low-power dynamic comparator [1] in the year 2016. The
pre-amplification of the comparator is halted by using the feedback mechanism which is highlighted in Figure 4. During the evaluation, once the enough differential output voltage is produced between nodes O1- and O1+, the pre amplifier is turned off using EXOR circuit as shown. This arrangement helps in power reduction but area penalty and speed decreases. In case the comparator is used at multiple places in the circuit the feedback mechanism is to be implemented that many times.

3.2. Comparator with enhanced preamplifier and clock circuit

![Figure 5. Comparator designed for Precise Applications [2]](image)

Ata Khorami and Mohammad Sharifkhani in the year 2018, proposed the High-Speed and low power comparator as shown in Figure 5. In this paper, the drawbacks present in [1] are mitigated. For the input of the preamplifier and the latch stage PMOS transistors are used. The clock generator circuit is also proposed which helps in turning off the preamplifier when the enough amplification is achieved. At the evaluation time, the dynamic latch is turned on after a delay so that power consumption is reduced and preamplification gain is achieved. This circuit is good in terms of power efficiency and area overhead but the maximum operating frequency is limited because of the slow speed of conventional latch used in the design. Speed can further be enhanced by designing same circuit using NMOS at the input of preamplifier and latch instead of PMOS. The EXOR circuit can be implemented efficiently with less transistors and power consumption as presented in [6].

3.3. The StrongARM Latch comparator

Behzad Razavi presented the StrongARM latch [3] in 2015 as shown in Figure 6. This topology is the robust latch with high sensitivity, which can be useful in applications like sense amplifier. The highlights of this design are, negligible static power, output swing is rail-to-rail, less input-referred offset which arise primarily because of input differential pair.
The StrongARM latch sinks high current from supply. This makes it difficult to use for the applications like flash ADC where more comparators are required. By clocking the input devices instead of source through drain, kickback noise can be reduced. To use this circuit for precision operations and to reduce the offset voltage, many capacitors should be connected to X+ and X-, which degrades the speed and increases the power consumption. Offset cancellation can be achieved by other method proposed in [18].

3.4. Low-Power Double-Tail Dynamic Comparator

Figure 6. The StrongARM Latch [3]

Figure 7. Low power double-tail dynamic comparator [4]
Comparator is designed for low power and high-speed operation even with small supply voltages by Samaneh Babayan-Mashhadi and Reza Lotfi in 2014 [4] presented in Figure. 7. When CLK=0 in reset phase, both the tail transistors are off and fp and fn nodes gets charged to VDD. In evaluation mode, when CLK=VDD, the M3 and M4 transistor turns off and both tail transistors are on. The nodes fp and fn which are charged to VDD, starts discharging depending on the voltage present at both the input terminals. This kind of preamplifier design is very useful if implemented as a latch configuration so that the circuit can be designed at lower offset voltage without affecting speed. Because if the input transistor size is increased here, it will cause large delay in this circuit.

3.5. Transconductance-Enhanced dynamic comparator

![Figure 8. Transconductance-Enhanced dynamic comparator [5]](image)

Dynamic comparator with a new latching stage with more transconductance is presented by Y. Wang et al., M. Yao, B. Guo, Z. Wu, W. Fan and J. J. Liou in 2019 [5]. The latching stage consist of cross-coupled transistors as present in the preamplifier instead of the regular back to back connected inverters as shown in Figure. 8. The maximum operating frequency was limited as the many of previously proposed techniques were redesigning the pre amplifier but not the latch. If the total transconductance is more at the starting of comparison, it helps in faster comparison and lower power dissipation. Since the preamplifier is same as conventional the input transistor size required for lower offset is very large and leads to large parasitic capacitance that degrades the speed of amplification.

4. EXPERIMENTAL SETUP AND RESULTS

To produce the fair comparison between different comparators, we tried to achieve lower offset voltage without increasing much power consumption. The common mode voltage is set to VDD/2. All the comparators were designed in 180nm technology node. Circuit behavior is observed over large supply
voltage range 2V-0.6V. Figure. 9 represents the output waveform of dynamic comparator which we tried to achieve for all above mentioned comparators. The offset voltage is calculated considering the systematic offset and random offset. For systematic offset calculation, one input out of differential inputs is kept at VDD/2 and other one with ramp voltage close to VDD/2, with very less slope as shown in Figure 10. When the input difference becomes lesser than the resolution of comparator, the wrong output gets latched at the output. This method helps in determining the offset voltage. For delay calculation, time between the clock falling edge and the time when the output voltage difference reaches VDD/2 is noted.

Table 1 compares the performance of comparator techniques proposed by various authors operating at 1.8V supply voltage. The conventional comparator implemented using NMOS preamplifier operating at 500MHz, provides 5.7mV of offset voltage, 310ps delay while consuming 480μW of power. If we try to reduce the offset voltage further, the size of input transistors would have to be increased, which degrades speed, because of parasitic capacitance. The circuit shown in Figure 4, has significantly lesser power consumption 310μW than the conventional circuit because of the clock gating circuit. This circuit can be designed at lower offset voltage than conventional without much overhead of power but the delay increased to 330ps. Circuit proposed in [2], is able to produce the output with 277ps delay and 260μW of power consumption at the lower offset voltage of 2mV. This is because of redesigned clock circuitry and preamplifier, which reduces the common mode gain and helps in faster amplification the differential gain. The power consumption is excluding the clock generator circuit as its contribution to total power consumption is very less if more comparator circuits are used in design.

Comparator presented in [3] consumes 325μW power and 263ns delay while operating at 500MHz and 2.4mV offset voltage. This type of comparator is useful in applications like sense amplifier where the precision is important, which can be increased with power overhead.

For the double tail comparator topologies, common-mode voltage variation does not affect delay as compared to the conventional dynamic topology, with nearly equal power dissipation.

The delay of comparator in [4] is 250ps while operating at 500MHz frequency. This topology can work at lower supply voltage up to 0.6V with small variation in delay and power. The circuit presented in [5] has a different latch configuration which helps in increasing latching speed, thus decreasing delay to 234ps even when operated at 2GHz. Because of modified latch configuration and clock mechanism, it is able to operate even at 2.5GHz with more power consumption. It consumes significantly lesser area than other compared configurations, around 38% less area than conventional configuration. If offset voltage is to be reduced to 2mV, the maximum operating frequency drops to 1.75GHz with satisfactory delay and power consumption.
5. CONCLUSION

An overview of dynamic comparators which are used in Analog to Digital convertors, sense amplifiers, high speed I/O circuits is presented. Dynamic comparators have the high input impedance, rail to rail swing, almost zero static power consumption they are widely used in industrial applications over static comparators. Depending on the application requirements, the circuit can be chosen which provides less delay, area or higher operating frequency. If circuit is designed efficiently the power consumption can be reduced by 46% as presented in [2] and area can also be optimized by 38.63% as shown in [5], but these configuration lack in some parameters where other circuits are better. Designing the comparator with high precision, low voltage, high dynamic range, lower power dissipation, high speed, robust and less offset voltage is a critical challenge for present and future applications.
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