Fault-tolerant technology based on FPGA: A Research of LogiCORE™ IP Soft Error Mitigation Controller

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Abstract. In a radiation environment, compared with ASIC and FPGA based on anti-fuse structure, SRAM FPGA is more susceptible to single particle effect, in particular, the effect of single-event upset (SEU). How to improve the equipment anti-single particle over conversion reliability has become a key problem to be considered in the design of SRAM FPGA system. Xilinx provides soft error mitigation SEM IP cores that perform SEU detection, correction, and classification. As part of the SEU detection function, the SEM IP core uses ICAP and ECC primitives for clock control and observing the CRC circuit reading back. As far as SEU correction is concerned, the IP core performs the necessity through the built-in ECC function and the operation to locate and correct SEU errors. For the SEU classification, the IP core uses the Xilinx-Essential-Bit technology further to improve system reliability. Through the in-depth analysis of SEM, in this paper, soft error mitigation SEM controller IP core of Xilinx was used to build a verification and test platform based on Zynq-7000 SoC ZC702 in order to simulate the influence of cosmic irradiation on SRAM FPGA. On the basis of completing the functional verification of SEM IP core, we also put forward some improvement ideas based on the experimental results.

1. Introduction
When high-energy particles pass through a specific region of the target device, a large number of electron hole pairs will be generated in its path. The energy release of high-energy particles will ionize the surrounding particles, and these ions will drift, spread and combine with positive and negative charges under the action of electric field. The SEM IP also performs emulation of SEUs by injecting errors into configuration memory. The error injection feature provides a means to evaluate and test the SEU mitigation capabilities of the IP and the system level response to SEU without a radiation effects facility [1]. This optional debug feature was disabled in the DUT used in beam testing at CNL [2]. Proper management of these events can increase reliability and availability. When high-energy particles pass through the FPGA configuration bit sensitive region, they ionize surrounding particles on the path to generate grooves and constantly precipitate energy. When the charge is collected to a sufficient amount, abnormal changes in configuration bit will be caused [3], which will lead to FPGA errors. The occurrence of its behavior is highly random.

Xilinx’s SEM IP error correction and correction capabilities support its mitigation of soft errors caused by SEU. SEM IP core has three working modes: repair mode, enhanced repair mode and replacement mode [4]. The algorithms and principles of each mode are as follows: Repairing mode,
which is based on error check and correction (ECC) algorithm, with a view to combat single-bit soft errors in all parts. It can be alleviated when multi-bit errors occur in configuration memory and spread to single-bit per frame. Enhance recovering mode, which is based on ECC and cyclic redundancy check (CRC) algorithm as the foundation, with a view to fight against all parts of single bit error and adjacent double bit error. It can cover any frame address of single bit error and adjacent bits of SEU effects caused by the soft error. When configuring memory have many scattered mistakes to each frame single bit or adjacent double bits per frame, it also can deal with. Replacement mode, based on data reloading, supports any number of bit errors, even when the exact frame address of the error cannot be detected. In this paper, the Xilinx zynq-7000 SoC ZC702 FPGA-verification platform was built according to the project requirements, completed the test and verification of SEM IP core. After that, the principle and realization process of automatic error injection method are discussed, and some improvement measures are put forward according to the experimental results.

2. SEM IP core overview
The SEM Controller implements five main functions: initialization, error injection, error detection, error correction, and error classification. All functions, except initialization and detection, are optional; desired functions are selected during the IP core configuration and generation process. The SEM Controller initializes by bringing the integrated soft error detection capability of the FPGA into a known state after the FPGA enters user mode. After this initialization, the SEM Controller observes the integrated soft error detection status. When an ECC or CRC error is detected, the SEM Controller evaluates the situation to identify the Configuration Memory location involved. The repair methods use active partial reconfiguration to perform a localized correction of Configuration Memory using a read-modify-write scheme. These methods use algorithms to identify the error in need of correction. The replace method also uses active partial reconfiguration with the same goal, but this method uses a write-only scheme to replace Configuration Memory with original data. This data is provided by the implementation tools and stored outside the SEM Controller. The SEM Controller optionally classifies the soft error as essential or non-essential using a lookup table. Information is fetched as needed during execution of error classification. This data is also provided by the implementation tools and stored outside the SEM Controller. When the SEM Controller is idle, it optionally accepts input from the user to inject errors into Configuration Memory. This feature is useful for testing the integration of the SEM Controller into a larger system design. Using the error injection feature, system verification and validation engineers can construct test cases to ensure the complete system responds to soft error events as expected [5].

The structural diagram of SEM core is shown in figure 1, which mainly includes the logical Configuration module, external setup module, HID setup module, MON module and the Controller. The external setup module, MON module and HID setup module are separated, correspond to External Interface, Status Monitor interface, and Error Injection Interface. There is also a Status Interface for us to get some status information, the Clock Interface provides us with Clock signals.

| The state name | SWITCH COMMAND |
|----------------|----------------|
| Initialization |                |
| Observation    | O              |
| Idle           | I              |
| Injection      | Strobe pin level is set from 0 to 1 |
| Correction     |                |
| Report         |                |
| Reset          | R XX           |
The workflow of SEM IP core is changed by the state switch command Change, and can be in the serial port software view the information. The commonly used is shown in table 1. The general workflow is as follows [6]:

- Initialization, which displays initialization information representing IP core initialization successfully.
- Observation, after initialization, enter the monitoring state.
- Idle, in error or restart before SEM IP, SEM IP should be switched to Idle state.
- Injection, injection into the configuration register according to the linear frame address, trigger strobe internal port will inject 1 bit error, fix-multiple trigger to change the address is equivalent to multiple mistake injection.
- Correction, correct the error before the error report is generated.
- Report, SEM IP core can finally generate report, the report has error classification, error correction based on the algorithm, error in frame address frame, word, bit position, physical frame address, error classified information.

### Figure 1. SEM IP core structure diagram

#### Table 2. State change decoding.

| FPGA Components       | Total Available | Used   |
|-----------------------|-----------------|--------|
| LUTs                  | 53200           | 20327  |
| I/Os                  | 200             | 43     |
| Slice registers       | 106400          | 25772  |
| FPGA Logic Memory     |                 |        |
| RAMB36/FIFO           | 140             | 19     |
| RAMB18                | 280             | 31     |

SEM IP core test platform consists of a Xilinx Zynq-7000 SoC ZC702 FPGA, JTAG interface and PC connection cable, UART interface and PC connection cable and PC host composition. SEM IP has been an example module in system-level design. The connection between the SEM controller and the
standard serial port is the monitoring mode, able to exchange state switches with SEM controller, note wrong command, and output status information to serial port. The connection between the external pins of the SEM controller and the standard serial peripheral interface bus, when configuring memory to check with external SPI flash, pass SEM controller gets data. Human-machine interface device pin, connection with error message injection interface. The interface and SEM controller can exchange state information and switch commands, it is the debugging interface between serial terminal and device. In addition, the user can add more user logic resources to the design, and enable register level design input. After the circuit simulation and test platform is built, the fault injection system will be tested. According to the above research, when VIVADO completes comprehensive download and configuration of the development board, the program running on FPGA will automatically enter the initial state of SEM core and output initialization information. The test procedure is as follows:

(a) The generated data stream is loaded onto the FPGA and add test ports by VIO IP core.
(b) In the VIO debugging interface, use port address and level change to control the working state of IP core. Address internal port is the error address edit interface. The representation of the configuration memory frame address is shown in figure 2. The address of the linear frame in the figure is injected through VIO kernel debugging. A total of 40 binary addresses can be modified in VIO. [39-31] bits is prefix address without modification. [30-29] the two digits are FPGA model SS code, L represents the address of the linear frame, W represents the address of the linear frame word address, and B represents the number of bits per word.

| 11000000 | OS | LLLL | LLLL | LLLL | LLLL | WWWW | WB | BBBB |
|---------|----|------|------|------|------|------|----|------|
| 33333333 | 22 | 2222 | 2222 | 2222 | 1111 | 1111 | 119876543210 |
| 9876543210 | 09 | 876543210 |

Figure 2. Linear frame addressing mode

(c) Port monitoring software Teraterm monitoring serial port output data, according to the data to get the wrong address, correction report and other information. In the process of switching and action, the corresponding information can be monitored in the serial port. Among them, the key error definition is that only a small part of the configuration storage bit error is affected by the system. These errors are critical errors that are associated with the reliability level of the system

Since manual error injection verification cannot cover the frame address, only a limited number of errors are injected, and the focus is on the verification of error injection rules. See table 3 for injection error types and repair, which can repair the centralized error types described in the three working modes.

This study focuses on the internal storage configuration information of FPGA. FPGA is mainly composed of three parts, and CLB is the basic component unit. In the FPGA chip developed by Xilinx, Slice and the corresponding additional logic constitute CLB. A CLB can contain multiple slices or just one, and the Slice structure's utilization rate reflects how much the chip occupies resources. We have used power analysis tools, through our design experiments and data analysis, it can be concluded that the SEM based fault injection system has a very low occupancy rate on the chip, and even if the SEM test module is added, there are not many changes. It shows that the impact on system performance when using it for development is very small. However, when the peripheral asserts monitor starts, if it is waiting, the controller stops the additional data transfer. This can have a negative impact on the performance of the controller for error mitigation. For example, if a correction occurs, the controller successfully corrects (or handles) the error and then sends a status report. When the peripheral asserts that the peripheral cannot accept messages, the controller stops working, preventing it from returning to the observation state. Therefore, custom peripheral must have sufficient buffer depth and data consumption rate balance.
Table 3. Error injection and correcting state in each mode.

| Repair mode                        | Inject error types and patterns                  | Repair situation |
|-----------------------------------|-------------------------------------------------|------------------|
| Repair mode                       | Pour a bit                                       | Can repair       |
|                                   | Continuously inject multiple bits into a frame   | Can repair       |
|                                   | Continuously inject multiple bits, 1 bit per frame | Can repair       |
| Enhanced repair mode              | Inject 1 adjacent 2 bit                          | Can repair       |
|                                   | Note 5 pairs of adjacent 2 bits in different frames | Can repair       |
| Replace mode                      | Inject any frame any word any bit                | Can repair       |

4. Conclusion
With the more and more extensive development of embedded system, FPGA research and development is a very important part of it. In this paper, the validity and completeness of Xilinx's SEM IP core are verified through the test and verification of its functions. At the same time, the performance impact is also studied and analyzed. This paper believes that SEM IP core can greatly improve the system reliability and will play a key role in the development and research of FPGA. However, for the three working modes, only the replacement mode can check any bit and correct any bit. The other two modes are not as powerful. However, SEM IP core supports secondary development. In the following studies, the secondary development of SEM IP core will be focused to make it more suitable for project research.

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