A high-speed low-power SAR ADC in 40nm CMOS with combined energy-efficient techniques

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Abstract In this paper, a high-speed low-power SAR ADC is designed. In this prototype, an improved switching scheme combined with the optimized attenuation capacitor architecture is proposed, showing more power efficiency and is more suitable for high-speed data converters. Meanwhile, an improved synchronous timing strategy is employed, achieving flexible time allocation of DAC settling and comparison in each bit-cycle. In addition, a two-stage non-tail-current-source and single-phase-clock comparator is proposed with more power-efficiency and compatible resolving time. The prototype ADC is fabricated in a 40nm CMOS technology and occupies an active area of 0.04mm². An SNDR of 57.18dB and an SFDR of 75.29dB are achieved with the Nyquist rate input at a sampling rate of 160MS/s, consuming 1.3mW at 1.1V supply voltage.

Keywords: SAR ADC, low-power, dynamic comparator

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

SAR ADCs are popular with the advantages of low power and small area consumption. In the past days, the conversion rate of SAR ADC is limited and the pipelined ADC [1, 2, 3, 4, 5] is the mainstream architecture. With the scaling down of the transistor size, the single-channel SAR ADCs [6, 7, 8, 9, 10] can achieve hundreds of MS/s sampling rate with resolution no less than 10bit. Meanwhile, the hybrid structure pipelined SARs [11, 12, 13] are popular to realize the high-speed medium-resolution ADC.

In the past few years, many power-efficient switching schemes [14, 15, 16, 17, 18, 19, 20, 21] are proposed. Some of these switching schemes are applied in moderate or high speed SAR ADCs. For lower power consumption, the input common mode voltages are at low level. In high-speed application, the input common mode voltage influences the comparison time. In the asynchronous timing strategy, when the comparison time is larger, the time allocated for DAC voltage settling is reduced.

Comparators are the key component for data converters, especially for SAR ADC. In conventional SAR ADCs, one-stage comparators are widely used in many designs [22, 23]. Recently, the two-stage comparators are adopted in some SAR ADCs [24, 25, 26] for lower offset and kickback noise suppression. Compared with the single-stage dynamic comparator, the two-stage comparator requires less voltage headroom and can achieve full-swing output. However, the complementary phase clock is required in the above-mentioned two-stage comparators, which consumes large power consumption. In this design, a two-stage non-tail-current-source single-phase-clock dynamic comparator is proposed with compatible comparison speed and more power-efficiency.

In this paper, a high-speed low-power SAR ADC is proposed. For high conversion rate and low power consumption, an improved switching scheme combined with the optimized attenuation capacitor structure is proposed. Meanwhile, an improved synchronous timing strategy is adopted. The time allocated for the DAC settling and comparator in each bit-cycle is flexible. In addition, a two-stage non-tail-current-source and single-phase-clock comparator is proposed with more power-efficiency and compatible resolving time. The whole paper is arranged as follows: In Section 2, the proposed SAR architecture is demonstrated. Section 3 describes the improved synchronous timing strategy. In Section 4, the improved switching scheme combined with the optimized attenuation structure are illustrated. Section 5 illustrates the non-tail-current-source single-phase-clock dynamic comparator. Section 6 demonstrates the measurement results. The conclusion of the whole data converter is in Section 7.

2. The proposed SAR ADC architecture

The whole structure of the 12-bit SAR ADC is demonstrated in Fig. 1. In this prototype, a binary-weighted DAC capacitor array with an attenuation capacitor is employed. It is composed of the clock generator, the bootstrapped switches, the differential DAC capacitor array, the dynamic comparator, and the digital control logic. Top-plate sampling is employed, so the first bit is decided before the DAC capacitors

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switching. By using the top-plate sampling, one bit-cycle is saved and the corresponding capacitor is reduced [27].

3. Improved synchronous timing strategy

The synchronous timing of the conventional SAR ADC mentioned in [28] is depicted in Fig. 2. In conventional synchronous timing strategy, the fixed comparison time and DAC settling time show low efficiency for different inputs. The improved synchronous timing strategy spares more time for DAC settling if the comparison time is accelerated, the improved timing strategy, the time duration for each bit-cycle is fixed.

In this paper, an improved synchronous timing strategy is adopted and displayed in Fig. 3. In the improved timing strategy, the time duration for each bit-cycle is fixed.

In each bit-cycle, the time allocated for comparison and DAC settling is variable. When the output voltage difference of the comparator exceeds VDD/2, the VALID signal is triggered. The rising edge of the VALID signal starts the DAC settling.

The timing allocation for different common mode voltage variations are displayed in Fig. 4. The synchronous CLK is 2.24GHz and the duration of one bit-cycle is 446ps. When the input common mode voltage is larger than 0.3V, the comparison time for LSB/2 is less than half the bit-cycle. By using the improved synchronous timing strategy, the time allocated for DAC settling is extended.

Compared with the conventional synchronous timing SAR ADC, if the comparison time is accelerated, the improved synchronous timing strategy spares more time for DAC settling. For the same worst case of DAC settling time, the improved synchronous timing scheme consumes less comparison time. As a result, the time duration for each bit-cycle in the proposed scheme is reduced, and the conversion rate is accelerated.

4. Improved switchback switching scheme with the optimized attenuation structure

The proposed switching scheme is illustrated as follows. At the sampling phase, the bottom plate of most-significant-bit capacitor is connected to VREFN and bottom plate of the rest capacitors are connected to VREFP. After the sampling phase, the comparison is performed for the first bit. Either MSB capacitor of the differential DAC capacitor arrays will switch to VREFP if the corresponding input voltage of the side is smaller than the other. However, for the rest DAC capacitors, the capacitor of one side will switch to VREFN if corresponding input voltage of that side is larger than the other. The flow chart of the switching procedure is shown in Fig. 5. Different from the conventional switchback switching scheme, in the improved switchback switching scheme, the first bit is upward switching and the following bits are downward switching.

When the MSB capacitors are switched either to VREFP or VREFN, the switching energy consumed in this step can be expressed as the following expression:

\[
E_{MSB} = C_1 V^2_{REF} - \frac{C_M C_1}{C_M + C_L} || C_A^2 V^2_{REF} - \frac{C_1}{C_A + C_L} \frac{C_M C_1}{C_M + C_L} || C_A^2 V^2_{REF} \quad (1)
\]

In the above expression, assuming that \( V_{REF} = V_{REFP} = V_{REFN} \). In addition, \( C_1 \) represents the MSB capacitor and \( C_A \) represents the attenuation capacitor. \( C_M \) and \( C_L \) represent the total capacitors in the MSB side and the total capacitors in the LSB side, respectively. As a result, \( E_{MSB} = 0 \).

In addition, the reset energy of the proposed switching procedure can be calculated as

\[
E_{RST} = \frac{2 C_1 C_M C_L + 2 C_1 C_A C_L + 4 C_1 C_L C_A}{C_M C_L + C_M C_A + C_L C_A} V^2_{REF} - \frac{2 C^2_1 C_L - 2 C^2_1 C_A}{C_M C_L + C_M C_A + C_L C_A} V^2_{REF} \quad (2)
\]

It can be derived as

\[
E_{RST} = \frac{2^{N-k-2} + 2^{N-1} - 2^{k+1}}{2^{N-1} - 1} C_0 V^2_{REF} \quad (3)
\]

In the above expression, \( N \) represents the resolution of the SAR ADC and \( k \) represents the number of the capacitors in the MSB side. \( C_0 \) represents the unit capacitor.

Meanwhile, in the attenuation capacitor structure, the switching energy for each output code can be calculated as the following expression:

\[
E_N = \sum_{i=2}^{k} \left( D_i \sum_{j=1}^{i-1} C_j + (1 - 2D_i) \sum_{j=1}^{i-1} C_j D_j \right)
\]
In the proposed “N=12, k=6” attenuation capacitor structure equals 32.95V^2/REF and this is a large value. As can be seen from Fig. 4, when the input mode voltage of the comparator is 0.3V, the comparison time is larger than 250ps. When the input mode voltage of the comparator ranges from 0.4~0.85V, the comparison time is less than 160ps. The common mode voltages of the DAC capacitor array in different switching schemes are shown in Fig. 9. For larger DAC settling time, the proposed switching scheme and the split switching scheme [21] can spare more time for DAC settling in each bit-cycle. Increased comparison time results in less time for DAC reference voltage settling. Incomplete DAC reference voltage settling results in the deterioration of the overall linearity. However, the number of switches in split capacitor switching scheme is more than 2 times of the number in the other three switching schemes.

5. Non-tail current source single phase clock comparator

As depicted in Fig. 10, a two-stage non-tail-current-source single-phase-clock dynamic comparator is proposed. In the first stage, a clock-driven preamplifier is adopted. The tail-current-source is removed for lower voltage overhead and more power efficiency. The NMOS transistors M3/M4 and PMOS transistors M5/M6 are driven by CLK. The second stage is composed of a cross-coupled latch and voltage amplification transistors. Adopting the differential signals VP1/VN1 as the inverted CLK, the inverted-phase-clock can be removed in the second stage. The NMOS transistors M7/M8 performs the reset and amplification in the second stage. The PMOS transistors M11/M12 further amplify the
The transient waveform of the proposed comparator is demonstrated in Fig. 11. When CLK is at low level, transistors M5/M6 are in reset state. Meanwhile, nodes VP1/VN1 are quickly charged to VDD and maintain at the high level. Transistors M7/M8 are turned on by VP1/VN1, discharging the output nodes VOP/VON to GND. As a result, the second stage is at the reset state. When CLK turns to high level, the differential pair M1/M2 starts to amplify differential input signals. The nodes VP1/VN1 are discharged to GND at different speeds, depending on the drain currents of the differential input pair. The differential signal on nodes VP1/VN1 are further amplified by transistors M7/M8 and M11/M12. When either of the nodes VOP/VON reaches the voltage of a threshold above GND, the regenerative latch in second stage is activated. The regenerative latch performs large signal settling and generates the rail-to-rail comparison result.

When the differential signals VP1/VN1 are at high level, they can be used to reset the second stage. As a result, only one phase clock is used in the proposed comparator. In the comparator proposed in [29], an additional inverted-phase clock signal is employed to reset the second stage. In high speed data converters, the clock signal driving circuits consume large power dissipation and occupy a large area. Meanwhile, with the reduction of the tail current source in conventional preamplifier, the proposed comparator shows more power efficiency and better performance in low common-mode-voltage.

Based on the above analysis, the proposed comparator, the comparator in [30], and the comparator in [29] are designed in a 40nm technology. The three structures of comparators are designed with the similar size of transistors. Meanwhile, the load capacitors are the same and equal to 10fF.

Fig. 12 shows the resolving time versus differential input voltages for the three comparators. The supply voltage is 1.1V and the common mode voltage is 0.55V, with the 2.24GHz clock. The resolving time ranges from 40ps to 180ps with the differential input voltages varies from 0.1mV to 100mV. When the differential input voltage is less than 100mV, the proposed comparator shows faster resolving time.

The resolving time versus VCM (common mode voltages) for the three comparators is depicted in Fig. 14. When the common mode voltage is smaller than 0.6V, the proposed comparator shows less resolving time. When the common mode voltage ranges from 0.5V to 1.1V, the resolving time of the proposed comparator is compatible with the other two comparators.
In this paper, a high-speed low-power SAR ADC is proposed. A comparison of the proposed design with other SAR ADCs at similar sampling rates is summarized in Table I.

| Reference | This Work | Ref. [13] | Ref. [14] | Ref. [15] |
|-----------|-----------|-----------|-----------|-----------|
| Architecture | SAR | SAR | SAR | SAR |
| Resolution (bits) | 12 | 12 | 12 | 10 |
| Technology | 40nm | 40nm | 40nm | 90nm |
| Sampling Rate (MS/s) | 160 | 100 | 150 | 160 |
| Supply Voltage (V) | 1.1 | 1 | 0.9 | 1 |
| Power (mW) | 1.3 | 2 | 1.5 | 1.97 |
| ENOB (bits) | 9.21 | 10.5 | 9.04 | 8.51 |
| SNDR (dB) | 57.18 | 65 | 56.2 | 53 |
| SFDR (dB) | 75.29 | 84 | 86 | 86 |
| Area (mm²) | 0.04 | 0.02 | 0.04 | 0.11 |
| FoM (fJ/conv.step) | 13.71 | 13.8 | 18.9 | 33.5 |

Compared with other works, the FoM of this prototype is relatively lower. Meanwhile, the sampling rate is compatible with other works and the active area is relatively small.

7. Conclusion

In this paper, a high-speed low-power SAR ADC is designed. In this prototype, an improved switching scheme combined with the optimized attenuation capacitor architecture is proposed, showing more power efficiency and is more suitable for high-speed data converters. In addition, an improved synchronous timing strategy is employed, achieving flexible time allocation of DAC settling and comparison in each bit-cycle. Meanwhile, a two-stage non-tail-current-source and single-phase-clock comparator is proposed with more power-efficiency and compatible resolving time. The prototype ADC is fabricated in a 40nm CMOS technology and occupies an active area of 0.04mm². An SNDR of 57.18dB and an SFDR of 75.29dB are achieved with the Nyquist rate input at a sampling rate of 160MS/s, consuming 1.3mW at 1.1V supply voltage.

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