Advanced motor driving circuit with improved transfer efficiency based on adaptive segmented control

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Abstract An advanced motor driving circuit based on digital sampling load and adaptive segment control of power MOSFET to realize improved transfer efficiency is presented in this paper. A digital block is employed to detect the duty cycle of PWM signal which indirectly reflects the load condition. According to the duty cycle of PWM signal, a digital segment controller is employed to perform adaptively scaling the area of the power MOSFET to ensure current capacity of the power MOSFET just meets the load requirements. The power MOSFET is divided into three segments according to area ratio of 1:2:4. Area scaling step is 1/7 of the whole power MOSFET. The adaptive segmented controller contains duty cycle detector and segment controller is implemented based on FPGA. The correctness and feasibility of the proposed method are verified by experiments of a DC motor driver.

Keywords: motor driving circuit, high transfer efficiency, adaptive control, segment, DC motor driver

Classification: Circuits and modules for electronic instrumentation

1. Introduction

Motors are widely used in the fields that need using electrical signals to control mechanical components. A driver, which connects a motor and its control signal, is needed [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. And the performance of the driver plays a decisive role in the quality of the whole electromechanical system [14, 15, 16, 17]. A slight increase in transfer efficiency of a motor driver will result in a significant decrease in the heat produced by the motor driver itself, which will seriously affect the reliability of the whole electromechanical system [18, 19, 20]. So, improving transfer efficiency is one of the main issues for motor drivers.

At present, a motor driver is always a power switch converter. Pulse Width Modulation (PWM) method is usually employed to control the power MOSFET in the power switch converter [21, 22, 23]. Power consumption of a power MOSFET, which contains conduction and switching loss of the power MOSFET, is the main part of the power consumption of the whole power switch converter. Reducing parasitic resistance of the power MOSFET can decrease conduction loss. Lower parasitic capacitance of the power MOSFET will result in lower switching loss [24, 25]. Switching loss of a power MOSFET can be reduced by reducing frequency and voltage amplitude of the PWM signal, and equivalent gate capacitance of the power MOSFET. The equivalent gate capacitance of the power MOSFET is proportional to its area. Ensuring proper driving capability, the equivalent gate capacitance of the power MOSFET can be adaptively adjusted by adaptively scaling the area of the power MOSFET according to the load condition of the power switch converter. Segment control is effective for adaptively scaling the area of the power MOSFET in a power switch converter [26, 27, 28, 29].

In this paper, an advanced motor driving method based on digital adaptive segmented control of power MOSFETs to improve transfer efficiency is proposed. Power MOSFETs in the driver is divided into three segments according to area ratio of 1:2:4. A digital controller is used to control the segmented power MOSFETs based on detecting and hysteresis comparison of duty cycle of the PWM signal, which is indirectly reflect load condition of a power switch converter, to make sure the working current capacity of the MOSFETs just meets the load requirements. Area scaling step is 1/7 of the whole power MOSFETs. A DC motor driver [1, 4, 6, 11, 13, 14, 16, 30, 31] is used to experimentally verify the proposed digital control method. The digital adaptive segmented controller is implemented based on FPGA demo board. Compared with the traditional load sampling and control scheme, the proposed method can obviously improve the transfer efficiency under light load condition. The tested maximum improved transfer efficiency is 3.21%, when the duty cycle of the PWM signal is around 9%. Under heavy load condition (the duty cycle of PWM signal is large than 90%), both of two driving circuits have almost the same transfer efficiency.

2. Design and analysis

A power device, which is used to provide suitable power to drive load, is usually included in a motor driver. The power consumption of the power device is the main part of that for a motor driver. At present, power MOSFET is widely used in power switch converters profit from its advantages of low driving power and fast switching speed. Motor driver is one of power switch converters.

PWM is the most popular control method for power switch
converters. Power consumption of a power MOSFET in switch mode includes switch consumption and conduction consumption. Under PWM mode, power devices work in on/off state with the control of a high frequency (~kHz or ~MHz) signal. This will cause considerable switching loss and degrade the efficiency of the power switch converter.

As shown in equation (1), the switch consumption of a power MOSFET ($P_{sw}$) can be changed by varying the frequency of switching signal ($f_{sw}$), the equivalent gate capacitance of the power MOSFET ($C_{gate}$), and the voltage amplitude of the switching signal ($V_{gate}$). Reducing $f_{sw}$ and $V_{gate}$ can decrease the switch consumption. But lower $f_{sw}$ will cause increased ripple of output, lower $V_{gate}$ will induce poor driving capability. $C_{gate}$ is proportional to the area of the power MOSFET. And the area of the power MOSFET is determined by the maximum output current of the power switch converter.

$$P_{sw} = f_{sw} \times C_{gate} \times V_{gate}^2$$ (1)

When the load is light, current in the power MOSFET is far less than the maximum value. So, area of the power MOSFET can be significantly shrunk, and $C_{gate}$ can be reduced obviously, under light load condition. Ensuring proper driving capability, $C_{gate}$ can be adaptively adjusted by adaptively scaling the area of the power MOSFET according to the load condition of the power switch converter. Segment control is effective for adaptively scaling the area of the power MOSFET. Power MOSFET in a power switch converter can be divided into ($n+1$) segments according to the area ratio of $1:2^n$. Each segment can be driven by a proper driver with enable pin. And a segment controller can enable a driver or not. Therefore, the area of awake power MOSFET can be adaptively scaled in $1/(2^n – 1)$ step according to the load condition. Remaining parts of power MOSFET are resting.

For a power switch converter, the ratio of load current to the maximum output current reflects the load condition. In order to sample the load condition, the traditional method is to sample the output current by a high precision resistor. And an ADC (Analog to Digital Converter) is needed to convert the sampled analog signal to digital signal for digital controller [26, 27]. Fig. 1 shows the block diagram of traditional load sampling with high precision resistor and digital control by ADC of power MOSFET in power switch converters. Sampling large load current needs high precision small resistor. It is difficult to produce high precision small resistor. The ADC will cause extra power consumption.

For power switch converters, duty cycle of the PWM signal also reflects the load condition. Sampling the duty cycle of the PWM signal by using digital circuit, which is not easy to be disturbed, can indirectly sample the load condition of the power switch converter. And the sampling signal is digital signal. ADC is not needed.

Therefore, in this paper, we propose an advanced DC motor driving circuit with improved transfer efficiency, in which power MOSFET is divided into three segments ($seg_1$, $seg_2$, $seg_3$) according to area ratio of 1:2:4. By detecting and comparing duty cycle of the PWM signal, the load condition of the motor driver is sampled. As shown in Fig. 2, a digital block named segment controller is employed to adaptively control operating mode of the segmented power MOSFET. Both the duty cycle sampling block and the segment controller are composed by digital circuits. Three control signals from the segment controller control appropriate segments of power MOSFET are selected to operate. In any kind of load condition, the maximum working current capacity of the power MOSFET just meets the load requirements. So, under light load condition, power consumption induced by parasitic capacitance of the power MOSFET can be reduced and the transfer efficiency of the motor driver can be improved.

**Fig. 1** Block diagram of traditional load sampling and control of power MOSFET in power switch converters.

**Fig. 2** Block diagram of the proposed adaptive segment control of power MOSFET for improved efficiency motor driver.

Working mode of the proposed motor driving circuit is given in Table I. The duty cycle of the PWM signal is divided into 7 segments. When the duty cycle of the PWM signal is during 0~14%, the working mode of the output stage is Mode_1, only $seg_1$ is awake, $seg_2$ and $seg_3$ are resting. With the increase of load, the area of power MOSFET is gradually increased. Finally, When the duty cycle of the PWM signal is during 86%~100%, the working mode of the output stage is Mode_7, all segments of power MOSFET are awake.

**Table 1** Working mode of the proposed output stage of DC motor driving circuit

| Mode  | Duty cycle of the PWM signal | Operating status of segmented power MOSFET |
|------|-----------------------------|------------------------------------------|
| Mode_1 | 0~14% | $seg_1$ is awake, $seg_2$ and $seg_3$ are resting |
| Mode_2 | 14%~28% | $seg_2$ is awake, $seg_1$ and $seg_3$ are resting |
| Mode_3 | 28%~42% | $seg_1$ and $seg_2$ are awake, $seg_3$ is resting |
| Mode_4 | 42%~58% | $seg_1$ is awake, $seg_1$ and $seg_2$ are resting |
| Mode_5 | 58%~72% | $seg_1$ and $seg_2$ are awake, $seg_3$ is resting |
| Mode_6 | 72%~86% | $seg_2$ and $seg_3$ are awake, $seg_1$ is resting |
| Mode_7 | 86%~100% | $seg_1$, $seg_2$ and $seg_3$ are awake |
3. Experimental verification

In the experimental circuit shown in Fig. 3, digital duty cycle sampling block and segment controller are realized in the Cyclone II FPGA demo board. Seven same MOSFETs (M1–M7) on the Segmented MOSFETs board are divided into three segments (seg1, seg2 and seg3). For every MOSFET, $R_{DS(on)} = 90\, \text{m}\Omega$ and $C_{\text{gate}} = 920\, \text{pF}$. The seg1 is a single MOSFET. The seg2 includes two MOSFETs in parallel. And the seg3 includes four MOSFETs in parallel. PWM signal is directly generated by the Wave Generator. The Voltage Source provides 24V for the DC motor and 5V for the FPGA Demo Board. The DC motor is XD-3420, whose maximum power is 30W and operating voltage is 24V. For the traditional load sampling and control scheme of DC motor driver, the experimental circuit does not include the FPGA demo board. The PWM signal is directly used to drive the power MOSFET (M) which consists of M1–M7 in parallel. For the proposed DC motor driving circuit, three segments of power MOSFET are driven by three AND2 gate. The input PWM signal is connected to one input terminal of each AND2 gate. Three control signals from the FPGA demo board control three AND2 gate to be enable or not. The state of three control signals is monitored by the Oscilloscope.

The proposed digital adaptive segmented controller for improved efficiency DC motor driving circuit is illustrated in Fig. 4. A sampling signal with frequency of 100MHz, which is generated by multiplying the clock by Frequency multiplier (PLL), is used to detect the duty cycle of $V_{in}$ (a voltage pulse signal). Using an 8-bit counter, the pulse width of $V_{in}$ is obtained by sampling $V_{in}$ every 10 ns in one cycle of $V_{in}$. Setting the frequency of $V_{in}$ is 1kHz, the sampling accuracy of duty cycle of $V_{in}$ is 1%. Outputs of Hysteresis comparator $a$, $b$, and $c$ are used to control seg1, seg2, and seg3, respectively. Hysteresis comparison of duty cycle of $V_{in}$ is to prevent switching oscillation. The Display driver makes the duty cycle value of $V_{in}$ is visible on the LED screen on the FPGA demo board. The controller shown in the dashed box in Fig. 4 can be reset by rst signal.

Simulated results of Verilog HDL code of the digital adaptive segmented controller are shown in Fig. 5. Setting $D_R$ to represent the duty cycle of $V_{in}$:

- $0 < D_R \leq 14\%$, $a = 1$, $b = c = 0$.
- $14\% < D_R \leq 28\%$, $a = c = 0$, $b = 1$.
- $28\% < D_R \leq 42\%$, $a = b = 1$, $c = 0$.
- $42\% < D_R \leq 58\%$, $a = b = 0$, $c = 1$.
- $58\% < D_R \leq 72\%$, $a = c = 1$, $b = 0$.
- $72\% < D_R \leq 86\%$, $a = 0$, $b = c = 1$.
- $86\% < D_R \leq 100\%$, $a = b = c = 1$.

When the control signal is ‘1’, the corresponding power MOSFET segment is awake. On the contrary, When the control signal is ‘0’, the corresponding power MOSFET segment is resting. So, working mode of the proposed adaptive segmented control of the DC motor driving scheme given in Table I is verified.

Tested results of transfer efficiency in Fig. 6 indicate that the duty cycle varies directly with load current. Transfer efficiency of traditional load sampling and control scheme of DC motor driver, in which seven power MOSFETs are connected in parallel as a whole during the whole load range, is obviously lower than that of the proposed DC motor driving
circuit, under light load condition. The proposed DC motor driving circuit with adaptive segmented control can visibly improve the transfer efficiency. The maximum improved transfer efficiency is 3.21%, when the duty cycle of PWM signal is around 9%. When the duty cycle of PWM signal is less than 8%, the transfer efficiency of both two driving circuits is obviously decreased, and the difference of transfer efficiency is also significantly reduced. Because switching power consumption of the power MOSFET, in both of two driving circuits, is constant, when the duty cycle of PWM signal is less than 14%. Under heavy load condition (the duty cycle of PWM signal is large than 90%), both of two driving circuits have almost the same transfer efficiency. Because power consumption of the digital adaptive segmented controller is much lower than that of the whole driving circuit.

4. Conclusion

Duty cycle of PWM signal in power switch converters varies with load current. Detecting the duty cycle of PWM signal can indirectly reflect the load condition. DC motor driver is one of power switch converters. In this paper, an advanced motor driving circuit based on digital sampling load and adaptive segment control of power MOSFET to realize improved transfer efficiency is proposed. A digital block named Duty cycle detector is employed to detect the duty cycle of PWM signal. The power MOSFET is divided into three segments according to area ratio of 1:2:4. Another digital block named Segment controller is used to perform adaptively scaling the area of the power MOSFET, according to the duty cycle of PWM signal, to ensure maximum working current capacity of the power MOSFET just meets the load requirements. Area scaling step is 1/7 of the whole power MOSFET. A DC motor driving circuit is used to experimentally verify the proposed scheme. Compared with the traditional load sampling and control scheme, the proposed advanced motor driving circuit based on adaptive segmented control can obviously improve the transfer efficiency under light load condition. The maximum improved transfer efficiency is 3.21%, when the duty cycle of PWM signal is around 9%. Under heavy load condition, although there is an extra adaptive segmented controller in the proposed motor driving circuit, both of two driving circuits have almost the same transfer efficiency.

Acknowledgments

This work was funded by National Natural Science Foundation of China under Grant 61664004, and Open Foundation of Engineering Research Center of Reliability of Semiconductor Power Devices of the Ministry of Education under grant 010201.

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