Research Analysis of PCB Design’s Influence on DDR4 High-speed Signal Integrity

Fang Li1*

1 Software Engineering Institute of Guangzhou, Guangzhou, Guangdong, 510990, China

*Corresponding author’s e-mail: lfang@sise.com.cn

Abstract. With the increase of the signal transmission rate of electronic devices and the increase of the PCB wiring density, PCB design has a growing influence on signal integrity. To reduce the number of the problems concerning signal integrity at the initial stage of electronic product design and increase the success rate of the designing of electronic products, some interference signals of PCB are canceled to improve the accuracy of signal integrity test, with the high-speed parallel bus of DDR4 as an example. Analysis is done through measurement of various simulation tools to change the PCB design parameters of DDR4 data transmission line, hence the optimum wiring method will influence the signal quality. Meanwhile, RC parallel impedance matching optimization is carried out to deal with the impedance mismatch at the network load end. In this way, the problem concerning DDR4 high-speed signal integrity is effectively solved.

1. Introduction

Currently, PCB design has become an important part in the analysis of high-speed signal integrity. Specifically, such factors as board selection, PCB parameter setting and high-speed signal wiring may lead to problems concerning high-speed signal integrity. As a matter of fact, the rationality of PCB design affects, to a considerable extent, the normal operation of the system functions. DDR4, a dynamic random-access memory which has found wide application, has gradually replaced DDR3 and played a dominant role for its lower power dissipation, higher rate and larger storage capacity. However, the higher the data transmission rate is, the greater the impact on signal transmission integrity will be. In view of this, it has become a great concern of hardware designers how to conduct signal integrity simulation in PCB design of DDR4 and take effective PCB wiring control measures [1].

Crosstalk and reflection are two factors which affect high-speed signal integrity. Currently, experts and scholars are dedicated to the study of the problems concerning crosstalk and reflection which occur in DDR4 high-speed signal transmission. However, few research have been done on putting forward corresponding methods to improve PCB wiring for PCB wiring design in the study of signal integrity [2]. To deal with this problem, this paper, starting from PCB design, proposes to improve the signal transmission quality by eliminating some interference signals of PCB, which have conjugate objects featuring double-sideband structure. After denoising, with various simulation tools, simulation testing is done based on such parameters as calculation, simulation, and adjusting the distance between the transmission lines of the DDR4 data channel, length of the coupled lines and transmission rate, hence acquiring the optimum PCB wiring method. In addition, an effective optimization scheme for PCB design is proposed to tackle the problem concerning the impedance mismatch of DDR4 network.
load end, thus solving the problem concerning DDR4 high-speed signal integrity in a comprehensive manner [3].

2. Principle of Analysis

2.1. Principle of Analysis of High-speed Signal Integrity

In high-speed circuit PCB design, the most frequently used models of transmission lines are strip lines and microstrip lines. Strip lines are transmission lines wrapped by materials between two reference levels so that they may guarantee the integrity of the return path of the high-speed signal transmission lines[5]. Strip line structure is selected for DDR4 data channel as shown in Figure 1[4]:

![Diagrammatic figure of strip line structure](image1)

To ensure the quality of signal transmission, the impedance of the transmission line in the high-speed signals should be continuous and equal to the characteristic impedance. Characteristic impedance is an important parameter which ensures the integrity of high-speed signals. The formula of characteristic impedance of strip line is shown as follows [5]:

\[
z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{4H}{0.67\pi(0.8W + T)}
\]

In Formula (1), W is the width of transmission line, T is the thickness of metal, H is the interplanar distance, and \(\varepsilon_r\) is dielectric constant. The characteristic impedance level depends on board selection and laminated design at the initial stage of PCB design. During high-speed signal transmission, change in line width and difference in the distance between the lines lead to change in impedance of transmission line. Abrupt change in impedance of transmission lines will cause reflection noise, which affects the quality of waveform as shown in Figure 2[6]. The level of reflection may be measured by reflectance. The computing formula of reflectance is

\[
\rho = \frac{V_i}{V_r} = \frac{Z_1 - Z_0}{Z_1 + Z_0}
\]
Vi is reflected voltage, Vr is incident voltage, Z0 is the characteristic impedance of the transmission line, and Z1 is its impedance. The larger the difference value between Z0 and Z1 is, and the larger the reflectance is, the louder the noise is, and the more serious the waveform distortion is. When Z0=Z1, the reflectance is 0, which means that no reflection takes place. This is called impedance matching [7]. The ultimate cause of reflection is impedance mismatch. The key to dealing with the problem of reflection is that the impedance of transmission line should be consistent with the characteristic impedance for impedance control in the course of PCB design, and that simulation is done to optimize the system signals.

Crosstalk is one of the important factors influencing the integrity of high-speed signals. By crosstalk, it means in the course of signal transmission through the transmission line, interactional electromagnetic coupling will take place between the neighboring transmission lines, and this coupling will give rise to voltage noise jamming [8]. The circuit model for crosstalk is shown as in Figure 3. Line1 is signaling transmission line which is called interfering line while Line2 is the noise-making transmission line called interfered line.

![Figure 3. Circuit model for crosstalk analysis](image)

The induced voltage generated through coupling transmits in two directions: the near-end and the far-end of Line 2 respectively. The crosstalk in the near-end direction is called near-end crosstalk (Vb) while that in far-end direction is called far-end crosstalk (Vf)[9]. The level of crosstalk may be illustrated through crosstalk coefficients. Assume Line1 and Line2 have the same characteristic impedance(Z0), self-inductance coefficient(L0), and capacitance(C0), the length of transmission line is Len, the coupling coefficients are mutual inductance (LM) and mutual capacitance (CM)[10], the computational formula for the crosstalk coefficients are

\[ \text{NEXT} = \frac{V_b}{V_i} = \frac{1}{4} \left( \frac{C_M}{C_0} + \frac{L_M}{L_0} \right) \]

\[ \text{FEXT} = \frac{V_f}{V_i} = \frac{\text{Len}}{\text{RT}} \times \frac{1}{2} \left( \frac{C_M}{C_0} - \frac{L_M}{L_0} \right) \]

The near-end crosstalk coefficient is NEXT, the far-end crosstalk coefficient is FEXT, and RT is the signal risetime. The formula applied, it is clear that the distance between the transmission lines and the length of coupled line directly affects the crosstalk coefficient. The larger the distance between the lines is, and the shorter the line is, the smaller the crosstalk coefficient is, the lower the noise will be, and the better the signal quality will be.

On PCB of DDR4, due to the high density of routing and small space, a great number of parallel lines in small distance are often generated. This causes large coupling between the signal lines, which gives rise to serious crosstalk and reduction in signal quality. Therefore, such PCB parameters as rational distance between the line and length of the coupled lines need to be designed according to the actual conditions of DDR4 to ensure the quality of signal transmission [11].
In terms of crosstalk analysis, three-parallel-line transmission models are adopted. The three lines in the simulation model are adjacent DDR4 data channel transmission lines, hence the establishment of transmission line composed of two interfering lines (L1 and L3) and one interfered line (L2) [12]. For data transmission line, IBIS model is selected. A simple capacitance is selected at the receiving end of each transmission line as channel load. Tl model of each transmission line is acquired from package with SIWAVE tool, hence acquiring corresponding S-parameter [13].

2.2. Principle of Denoising
To improve the accuracy of DDR4 transmission signal detection, parts of the interference signals need to be erased. Assume that a PCB high-speed signal is x(t), s(t) is the reflected signal of the goal, J(t) is the interfering signal of the noise, and n(t) is the internal thermal noise, the signal expression is

\[ x(t) = s(t) + J(t) + n(t) = A(t) \cdot (w_c t) + (U_0 + U_n(t))((w_d t + \varphi)) + n(t) \]  

In Formula (5), A(t) is baseband signal, \( W_c \) is intermediate frequency of the echo signal, \( U_0 \) is carrier voltage, \( U_n(t) \) stands for white noise, \( \Phi \) stands for the initial phase of the interfering signal, and \( W_j \) stands for intermediate frequency of the interfering signal.

Formula (5) demodulated, solution (6) may be acquired

\[ y(t) = x(t)(w_d t + \varphi) = y_1(t) + y_2(t) \]  

Formula (6) Fourier transformed, solution (7) may be acquired

\[ Y(f') = Y_1(f') + Y_2(f') \]  

If \( F^* \) stands for Fourier transform, \( Y(f') = F^*y(t), Y_1(f') = F^*y_1(t), Y_2(f') = F^*y_2(t) \) is acquired.

If the known signal contains conjugate object featuring double-sideband structure, then

\[ Y(f') = \begin{cases} Y_{1,2}(f') + Y_{2,2}(f'), & f' > 0 \\ Y_{2,2}(f'), & f' \leq 0 \end{cases} \]  

In Formula (8), \( Y_{1,2}(f'), Y_{2,2}(f'), Y_{3,2}(f') \) are the signal components of the half-planes of the left and right frequency domains of \( Y_1(f) \) and \( Y_2(f) \) respectively. What is also obtained is

\[ Y_{2,2}(f') = (Y_{2,2}(-f'))^* \]  

\( \odot \) stands for complex conjugation.

Have the complex conjugates of \( Y(f') \) in \( Y_1(f) \) and \( Y_2(f) \) subtracted, the signal frequency components after interference cancellation are acquired:

\[ Y_{1,2}(f') = Y_{1,2}(f') \cdot \theta = (Y_{1,2}(f'))^\theta \cdot \theta \]  

The above is the process of signal component acquisition through which interference cancellation is done in the course of signal transmission in frequency domain, based on the compound symmetry of the interference signals and double-sideband of conjugate objects of the signals [14].

3. Simulation Analysis of Experiments
For PCB simulation experimental board, one DDR4 internal storage master controller chip drive, and two memory particle chips are used. The width of data bits is 32, and the data are featured by point-to-point topological structure. \( U_0 \) is master control chip, \( U_2 \) and \( U_3 \) are memory particle chip. First, PCB laminated construction design is done. FR-4 dielectric material is selected as the board. Dielectric constant \( \varepsilon_r \) is 4.5, PCB laminate is set to be 6, from top to bottom are TOP, L2VCC (power supply),
L3SIG (signal), L4SIG(signal), L5GND(stratum) and BOTTOM. The aggregate thickness of the board is 1.6mm. The data channel line of DDR4 is within the internal planes of L2 and L3. The line width is set to be 0.20mm. The characteristic impedance of the transmission line is restricted to 50Ω. Now, extract a section of network in L3 internal plane of DDR4 data channel to conduct simulated analysis. Simulation tools involve Advanced Design System (ADS) and Sigrity from Cadence.

3.1. Simulation Comparison Between Denoising and Un-denoising
Conditions for simulation: the transmission line is 100mm, the distance between the lines is 1W(W = 0.15mm), and transmission rate is 2133Mbit/s. Denoise and un-denoise parts of the interference signals of the testing signals. Simulation is shown in Figure 4.

![Eye diagram of un-denoising](image1.png) ![Eye diagram after denoising](image2.png)

Figure 4. Eye diagrams before and after denoising

As shown in the simulation result in Figure 4, the opening degree of the eye diagram after denoising is widened from 450ps to 490ps, which not only optimizes signal quality but also improves the accuracy of simulation [15]. Based on the above analysis, all the testing signals are subject to simulating testing after being denoised.

3.2. Simulation Analysis after denoising
Change such PCB parameters as the distance between the lines, length of coupled lines and transmission rate of DDR4 data channel transmission lines to conduct simulation analysis. The values of simulation parameters are shown in Table 1.

| Transmission rate Mbit/s | Distance between transmission lines space (W)mm | Length of transmission lines mm |
|--------------------------|-----------------------------------------------|---------------------------------|
| 2133                     | 0.15 (1W)                                     | 50                              |
| 2400                     | 0.30 (2W)                                     | 100                             |
| 2666                     | 0.45 (3W)                                     | 150                             |
| 3200                     | 0.60 (4W)                                     |                                 |

3.2.1. Simulation Analysis of Different Lengths of Coupled Lines
In Conditions for simulation: The coupled lines are 50mm, 100mm and 150mm in length respectively, the distance between the lines is 2W, and transmission rate is 2133Mbit/s.
The simulation result in Figure 5 shows that with the increase of the length of coupled lines, the opening degree of the eye diagram becomes smaller, coupled with poorer signal quality. When the line length is 50mm, the degree is relatively greater (543ps), which stands for the optimum signal quality. Therefore, conditions for wiring resources permitted, it is suggested that the length of the parallel lines be reduced as much as possible. If the parallel lines are inevitably long in doing DDR4 actual wiring, and the line length may not be reduced, JOG routing may be used to reduce crosstalk, i.e., enlarge the distance between the lines discontinuously. The routing is shown in Figure 6.

3.2.2. Simulation Analysis of the Different Distances between the Parallel Lines

Conditions for simulation: length of coupled line is 50mm, the distance of parallel lines are 1W, 2W, 3W and 4W (W=0.15mm) respectively, and transmission rate is 2133Mbit/s.

As shown in the simulation data in Table 2, with the increase of the distance, the crosstalk range decreases. For each additional 1W of the distance, the crosstalk decreases by around 50%. When the distance for wiring reaches 4W, the crosstalk value is the minimum, which may be seen as virtual elimination of crosstalk.

| distance between the lines W | 1W   | 2W   | 3W   | 4W   |
|------------------------------|------|------|------|------|
| Near-end crosstalk range mV  | 72   | 34   | 13   | 5    |
| Far-end crosstalk range mV   | 45   | 22   | 9    | 3    |

In doing wiring planning of DDR4, it is suggested that the distance between the parallel lines be increased as much as possible to reduce the generation of crosstalk. The distance between the lines should be larger than 3W. In actual designing, as the DDR4 component is featured by dense layout, some distances between the lines are too small. For example, as shown in Figure 7, the line distance shown in the white area is less than 2W. To reduce crosstalk, the problem of PCB wiring may be solved in an flexible way by reducing the length of coupled lines and widening the line distance at the appropriate position.
3.2.3. Simulation Analysis of Different Transmission Rates

Conditions for simulation: data transmission rates are 2133Mbit/s, 2400Mbit/s, 2666Mbit/s and 3200Mbit/s respectively. The length of the transmission line is 100mm, and the distance between the lines is 2W. The other parameters of the test board remain unchanged.

The result shown in Figure 8 indicates that the higher the transmission rate is, the smaller the opening degree of the eye diagram is, the thicker the eyeliner is, the more disordered the waveform of the eye diagram is, and the poorer the signal quality is. When the transmission rate reaches 2133Mbit/s, the opening degree is 512ps, the largest of its kind. This indicates that the signal quality is the best.

In Figure 8, when the transmission rate is 3200Mbit/s, the simulation waveform of the eye diagram is in disorder, featuring small opening degree of eye diagram and poor signal quality. To ensure the normal operation of the system functions at this rate, the network needs to be optimized. Analysis indicates that the network PCB wiring conforms to the rules and that the problem is mainly caused by impedance mismatch at the network load end. In view of this, RC parallel termination impedance matching may be done at the load end of the network. The method for terminating is shown in Figure 9[16].

![Figure 7. PCB Wiring Diagram](image)

![Figure 8. Eye diagram of different transmission rates](image)

The result shown in Figure 8 indicates that the higher the transmission rate is, the smaller the opening degree of the eye diagram is, the thicker the eyeliner is, the more disordered the waveform of the eye diagram is, and the poorer the signal quality is. When the transmission rate reaches 2133Mbit/s, the opening degree is 512ps, the largest of its kind. This indicates that the signal quality is the best.

In Figure 8, when the transmission rate is 3200Mbit/s, the simulation waveform of the eye diagram is in disorder, featuring small opening degree of eye diagram and poor signal quality. To ensure the normal operation of the system functions at this rate, the network needs to be optimized. Analysis indicates that the network PCB wiring conforms to the rules and that the problem is mainly caused by impedance mismatch at the network load end. In view of this, RC parallel termination impedance matching may be done at the load end of the network. The method for terminating is shown in Figure 9[16].

![Figure 9. RC parallel termination impedance matching](image)
In Figure 9, substitute $Z_0 = R, Z_1 = R + \frac{1}{j2\pi C}, R_T = Z_0 = R$ into Formula (1), and the reflectance is obtained:

$$\rho = \frac{1}{1 + 2\pi f/RC}$$

(11)

Formula (11) indicates that when the signal frequency is given, the larger the capacitance is, and the smaller the reflectance is, the better the signal quality will be. However, after capacitance becomes larger, and the charging time becomes longer, the time for rising edge becomes longer, which affects the time sequence of the circuit. Therefore, to decide the capacitance, accurate simulation testing needs to be done. In the field of engineering, the simulation tool Terminator Wizard in Hyperlynx is frequently used. This tool may help to acquire the recommended value of capacitance according to the actual terminating conditions. After Hyperlynx-based simulation, 150pF capacitance is recommended, i.e., optimization is done while the resistance is characteristic impedance 50Ω, and capacitance is 150pF RC parallel terminal matching. The simulation data before and after terminating are shown in Table 3:

| Situation                      | Degree of opening ps | Near-end crosstalk amplitude mV | Far-end crosstalk amplitude mV |
|--------------------------------|----------------------|---------------------------------|--------------------------------|
| Before termination matching    | 346                  | 120                             | 86                             |
| After termination matching     | 447                  | 65                              | 42                             |

The simulation data in Table 3 shows that after impedance matching, the crosstalk of signal waveform is effectively curbed. The opening degree of the eye diagram increases, which indicates that the optimization helps to improve signal quality, hence conforming to the the requirements for designing. The simulation result may be updated in PCB wiring constraint manager to the constraint rule to help PCB design to achieve the desired results.

4. Conclusion

This paper takes DDR4 high-speed parallel bus as an example. Before simulation, signals are denoised, which improves the accuracy of signal integrity test. Simulation analysis is done with the combination of various simulation tools to change PCB design parameters, hence acquiring a rational PCB wiring rule. Next, on the basis of actual component layout and transmission rate, JOG routing is proposed to change the distance between the lines and the length of coupling lines in a flexible way. With the help of diversified design methods such as RC parallel terminal impedance matching optimization, the influence of crosstalk is effectively reduced, hence improving signal quality. Experiments indicate that PCB design method proposed in this paper is of practical guiding significance in dealing with the problem concerning DDR4 signal integrity.

Acknowledgments

Guangdong Province University Teachers' Characteristic Innovation Research Project (No.2020DZXX07).

References

[1] Nitin Bhagwath, Chuck Ferry, Motoaki Matsumura. DDR4 Board Design and Signal Integrit Verification Challenges[C]//IEC Design Con, Santa Clara, CA. 2015.
[2] Li Chuan, Wang Yanhui & Zhang Hao. Crosstalk Simulation and Analysis of DDR4 Parallel Interconnection[J]. Computer Engineering and Science, 2019, 41(4): 612-616.

[3] Gou Xinke, Wang Ni’er & Ren Chongyu. Influence of PCB Parameters Signal Integrity of LPDDR3[J]. College Journey of College of Electrical and Information Engineering, Lanzhou University of Technology, 2017, 43(2): 92-96. Friedman J H. Multivariate adaptive regression splines[J]. The annals of statistics, 1991: 1-67.

[4] Anonymous. Samsung Develops DDR4 DRAM Using 30nm Class Technology[J]. M2 Presswire, 2011.

[5] Yu Zheng, Secret of Signal Integrity[M]. Beijing: China Machine Press, 2014: 140-152.

[6] Wang Hui & Zhao Aihua, Impedance of Transmission Line Based on Characteristics of Impedance Continuity[J]. Microcomputer & Its Applications, 2014, 33(11): 83-85.

[7] Hruska, Joel. RAMing speed: Does Boosting DDR4 to 3200MHz Improve Overall Performance[J]. Extreme Tech.com, 2015.

[8] Bian Baoping, LPDDR4 High-speed Parallel Bus Signal Integrity Analysis [D]. China Jiliang University, 2016: 22-32.

[9] Cadence. Routing DDR4 Interfaces Quickly and Efficiently [DB/OL](2016-09-15) ..https://www.Cadence.Com/content/cadence-www/global/zh_CN/home/search.Html?q=Routing%20DDR4%20Interfaces%20Quickly%20and%20Efficiently

[10] PARK J, KIM J J, KIM H, Etal.Eye diagram estimation of 8B/10B encoded high-speed serial link for signal integrity test using silicone rubber socket[C]. IEEE International Symposium on Electromagnetic Compatibility.IEEE, 2016: 467-471.

[11] Wang Haisan, Technical Research of DDR Trunk Signal Integrality Analysis[D]. East China University of Science and Technology, 2014: 35-42.

[12] S. Hall and H. Heck, Advanced Signal Integrity for High-Speed Digital Design. New York: Wiley, 2019.

[13] Liu Bo, Simulation Analysis of Signal Integrity for DDR4 High-speed Concurrent Bus[D]. Inner Mongolia University. 2018: 15-22.

[14] Li Fang & Cao Shukuan. High-Speed Signal Transmission Integrity Simulation of Electronic Equipment Printed Circuit Board[J]. Computer Simulation, 2019, 36(8): 178-181.

[15] Hamed A, Reza H A. Compact microstrip dual-narrowband bandpass filter with wider rejection band[J]. Electromagnetics, 2018, 38(6): 390-401

[16] Zhou Zixiang, Analysis of Eye Diagram Based on High-Speed Parallel Bus of DDR4[D]. Xidian University, 2015: 30-45.