Image Classification with CondenseNeXt for ARM-Based Computing Platforms

Priyank Kalgaonkar
Department of Electrical and Computer Engineering
Purdue School of Engineering and Technology
Indianapolis, Indiana 46202, USA.
pkalgaon@purdue.edu

Mohamed El-Sharkawy
Department of Electrical and Computer Engineering
Purdue School of Engineering and Technology
Indianapolis, Indiana 46202, USA.
melshark@purdue.edu

Abstract—In this paper, we demonstrate the implementation of our ultra-efficient deep convolutional neural network architecture: CondenseNeXt on NXP BlueBox, an autonomous driving development platform developed for self-driving vehicles. We show that CondenseNeXt is remarkably efficient in terms of FLOPs, designed for ARM-based embedded computing platforms with limited computational resources and can perform image classification without the need of a CUDA enabled GPU. CondenseNeXt utilizes the state-of-the-art depthwise separable convolution and model compression techniques to achieve a remarkable computational efficiency.

Extensive analyses are conducted on CIFAR-10, CIFAR-100 and ImageNet datasets to verify the performance of CondenseNeXt Convolutional Neural Network (CNN) architecture. It achieves state-of-the-art image classification performance on three benchmark datasets including CIFAR-10 (4.79% top-1 error), CIFAR-100 (21.98% top-1 error) and ImageNet (7.91% single model, single crop top-5 error). CondenseNeXt achieves final trained model size improvement of 2.9 MB and up to 59.98% reduction in forward FLOPs compared to CondenseNet and can perform image classification on ARM-Based computing platforms without needing a CUDA enabled GPU support, with outstanding efficiency.

Index Terms—CondenseNeXt, Convolutional Neural Network, Computer Vision, Image Classification, NXP BlueBox, ARM, Embedded Systems, PyTorch, CIFAR-10, CIFAR-100, ImageNet.

I. INTRODUCTION

ARM processors are widely used in electronic devices such as smartphones and tablets as well as in embedded computing platforms such as the NXP BlueBox, Nvidia Jetson and Raspberry Pi for computer vision purposes. ARM is RISC (Reduced Instruction Set Computing) based architecture for computer processors which results in low costs, minimal power consumption, and lower heat generation compared to its competitor: CISC (Complex Instruction Set Computing) architecture based processors such as the Intel x86 processor family. As of 2021, over 180 billion ARM-based chips have been manufactured and shipped by Arm and its partners around the globe which makes it the most popular choice of Instruction Set Architecture (ISA) in the world [1].

The roots of ARM processors trace back to December 1981 when the first widely successful design, BBC Micro (British Broadcasting Corporation Microcomputer System), was introduced by Acorn Computers [2]. Due to the use of DRAM (Dynamic Random Access Memory) in its design, it outperformed nearly twice as that of Apple II, an 8-bit personal computer, which was world’s first successfully mass-produced publicly available computer designed by Steve Wozniak, Steve Jobs and Rod Holt in June 1977 [3].

Fast forwarding to the 21st century, due to constant advances in computing and VLSI technology, ARM-based chips are found in nearly 60% of all mobile devices and computing platforms produced today. With processor performance doubling approximately every two years with a focus on parallel computing technologies such as multi-core processors, computer vision researchers can now implement sophisticated neural network algorithms to perform complex computations for OpenCV applications without requiring a GPU support.

Convolutional Neural Networks (CNN), a class of Deep Neural Networks (DNN) first introduced by Alexey G. Ivakhnenko and V. G. Lapa in 1967 [4], have been gaining popularity in recent years as researchers focus on creating more advanced intelligent systems. CNNs are popularly used in machine (computer) vision applications such as image classification, image segmentation, object detection, etc. However, implementing a CNN on embedded systems with constrained computational resources for applications such as autonomous cars, robotics and unmanned aerial vehicle (UAV), commonly known as a drone, is a challenging task. In this paper, we present image classification performance results of CondenseNeXt CNN on NXP BlueBox, an ARM-based embedded computing platform for automotive applications.

II. RELATED WORK

Following work has contributed to the research and implementation results presented within this paper:

CondenseNeXt: An ultra-efficient deep convolutional neural network for embedded systems, introduced by P. Kalgaonkar and M. El-Sharkawy in January 2021 [5] has been utilized to train and evaluate image classification performance on three benchmarking datasets: CIFAR-10, CIFAR-100 and ImageNet.
III. NXP BLUEBOX 2.0

The BlueBox 2 family developed and manufactured by NXP Semiconductors N.V, a Dutch-American semiconductor manufacturer with headquarters in Eindhoven, Netherlands and Austin, United States of America, is a Automotive High Performance Compute (AHPC) platform that provides essential performance and reliability for engineers to develop sensor fusion, automated drive and motion planning applications along with functional safety, vision acceleration and automotive interfaces for self-driving (autonomous) vehicles.

NXP BlueBox Gen1 was first introduced in May 2016 at the 2016 NXP FTF Technology Forum held in Austin, Texas, USA. This opened avenues to a host of autonomous and sensor fusion applications. Shortly after, NXP introduced BlueBox Gen2 (BlueBox 2.0), a significant improvement over Gen1, incorporating three new processors: S32V234 ARM-based automotive computer vision processor, LS2084A high performance ARM-based compute processor and S32R274 ASIL-D RADAR microcontroller.

S32V234: The S32V234 automotive computer vision processor comprises of a quad core ARM Cortex-A53 CPU running at 1.0 GHz paired with a ARM Cortex-M4 functional safety core which utilizes the ARMv8-A 64-bit instruction set developed by ARM Holdings’ Cambridge design centre. It has a 4MB internal SRAM in addition to a 32bit LPDDR3 memory controller for external memory support. It is an on-chip Image Signal Processor (ISP) designed to meet ASIL-B/C automotive safety standards and optimized for obtaining maximum performance per watt efficiency.

LS2084A: The LS2084A high performance compute processor comprises of an octa core ARM Cortex-A72 CPU running at 1.8 GHz which utilizes the ARMv8-A 64-bit instruction set developed by ARM Holdings’ Austin design centre. It has two 72 bytes DDR4 RAMs running at up to 28.8GB/s memory bandwidth. The LS2 provides software compatibility with next generation LayerScape LX2 family and offers AEC Q100 Grade 3 reliability with 15 years product longevity.

S32R274: The S32R274 radar micro-controller comprises of a dual core Freescale PowerPC e200z7 32-bit CPU running at 240 MHz and a dual core Freescale PowerPC e200z4 32-bit CPU running at 120 MHz with an additional checker core. It has a 2 MB Flash and 1.5 MB SRAM for radar application storage, message buffering and radar data stream handling. The S32R processor is optimized for on-chip radar signal processing to maximize performance per watt efficiency. It has been designed by NXP to meet the ASIL-D automotive applications standards.

IV. RTMAPS REMOTE STUDIO SOFTWARE

RTMaps (Real-Time Multisensor applications) developed by Intempora is a powerful GUI software that aids in development of applications for advanced driver assistance systems, autonomous driving and robotics. It helps in capturing, processing and viewing data from multiple sensors and offers a multi-modal development and run-time environment for ARM-based computing platforms such as the NXP BlueBox 2.0. This data can also be reviewed and play-backed at a later time for offline development and testing purposes.

RTMaps Remote Studio supports PyTorch, an open-source machine learning library based upon the Torch library, widely used for real-time computer vision (OpenCV) development. Algorithms for OpenCV can be developed using Python scripting language and by the means of block diagrams. It also facilitates the development of algorithms directly on to any supported embedded system without having to connect external user interfacing peripheral devices.
V. CondenseNeXt

CondenseNeXt is an ultra-efficient deep convolutional neural network architecture designed for embedded systems introduced by P. Kalgaonkar and M. El-Sharkawy in January 2021. CondenseNeXt refers to the next dimension of cardinality. In this section, we describe in detail the architecture of this neural network that has been utilized to train and evaluate image classification performance on three benchmarking datasets: CIFAR-10, CIFAR-100 and ImageNet.

A. Convolution Layers

One of the main goals of CondenseNeXt is to reduce the amount of computational resources required to train the network from scratch and for real-time inference on embedded systems with limited computational resources. Following state-of-the-art technique has been incorporated into the design of this CNN:

- Depthwise convolution layer: It acts like a filtering layer where convolution to a single input channel is applied separately instead of applying it to all input channels. Assume there is an input data of size $A \times A \times C$ and filters (kernels) $K$ of size $F \times F \times 1$. If there are $C$ number of channels in the input data, the output will be of size $B \times B \times C$. At this point, the spatial dimensions have shrunk. However, the depth $C$ has remained constant and the cost of this operation will be $B^2 \times F^2 \times C$.

- Pointwise convolution layer: It acts like a combining layer where a linear combination is carried out for each of these layers. At this stage, a $1 \times 1$ convolution is applied to $C$ number of channels in the input data. Thus, the size of filter for this operation will be $1 \times 1 \times C$ and size of the output will be $B \times B \times D$ for $D$ such filters.

Assume a standard convolutional filter $K$ of size $F \times F \times A \times B$ where $A$ is the number of input channels and $B$ is the number of output channels with an input feature map $A$ of size $D_x \times D_y \times A$. This produces an output feature map $Z$ of size $D_x \times D_y \times B$ can be mathematically represented as follows:

$$Z_{k,l,n} = \sum_{i,j,m} k_{i,j,m,n} \cdot A_{k+i-1,l+j-1,m}$$  \hspace{1cm} (1)

In case of a depthwise separable convolution, (1) is factorized into two stages: the first stage applies a $3 \times 3$ depthwise convolution $\hat{K}$ with one filter for every input channel:

$$\hat{Z}_{k,l,m} = \sum_{i,j} \hat{K}_{i,j,m} \cdot A_{k+i-1,l+j-1,m}$$  \hspace{1cm} (2)

Consequently, in the second stage, a $1 \times 1$ pointwise convolution $\hat{K}$ is applied to carry out linear combination and combine the outputs of depthwise convolution from previous stage as follows:

$$Z_{k,l,n} = \sum_{m} \hat{K}_{m,n} \cdot \hat{Z}_{k-1,l-1,m}$$  \hspace{1cm} (3)

This methodology splits a kernel into two discrete filters for filtering and combining stages as shown in Figure 3 above, which results in reduction of computational resources required to train the network from scratch as well for real-time inference.

A widely used model compression technique is also implemented into the design of this CNN where a further significant impact, both in computational efficiency at training time and on the final trained model size is seen.

B. Model Compression

A widely popular model compression technique called Group-wise Pruning is implemented to make CondenseNeXt neural network computationally more efficient by discarding redundant elements without influencing the overall performance of the network.

Group-wise Pruning: The purpose of group-wise pruning is to remove trivial filters for every group $g$ during the training process which is based on the $L_1$-Normalization of $A^{(g)}$ where for every group $g$, $a$ is the input and $z$ is the output. A pruning hyper-parameter $p$ is established and set to 4 which allows the network to decide the number of filters to remove before the first stage of depthwise separable convolution. A class balanced focal loss function [7] is also added to assist and ease the effect of this pruning process.

Consider a group convolution comprised of $G$ groups of size $F \times F \times C_A \times C_B$ where $C_A = \frac{A}{C}$ and $C_B = \frac{B}{C}$. The total number of trivial filters that will be pruned before the first stage of depthwise separable convolution is mathematically represented as follows:

$$G \cdot C_x = A \cdot C - p \cdot A$$  \hspace{1cm} (4)

Cardinality: A new dimension to the network called Cardinality denoted by $C$ is incorporated into the design of CondenseNeXt neural network in addition to the existing width and depth dimensions so that loss in accuracy during the pruning process is reduced. Experiments prove that increasing cardinality is a more efficacious way of accruing accuracy than going deeper or wider, especially when width and depth starts to provide diminishing returns [8].

![Figure 3. A 3D illustration of the overall process of depthwise separable convolution. An image is transformed 128 times whereas an image is transformed by depthwise separable convolution only once and then this transformed image is stretched to 128 channels which allows the neural network to process more data while consuming fewer FLOPs (Floating Point Operations).](image)
C. Activation Function

In deep neural networks, activation functions determine the output of a neuron at particular input(s) by restricting the amplitude of the output. It aids in neural network’s understanding and learning process of complex patterns of the input data. Furthermore, non-linear activation functions such as ReLU6 (Rectified Linear Units capped at 6) enable neural networks to perform complex computations using fewer neurons [9].

CondenseNeXt applies ReLU6 activation function in addition to Batch Normalization technique prior to each convolutional layer. In ReLU6, units are capped at 6 to promote an earlier learning of sparse features and to prevent a sudden blowup of positive gradients to infinity. ReLU6 activation function is defined mathematically as follows:

\[ f(x) = \min(\max(0, x), 6) \]  

(5)

VI. CYBERINFRASTRUCTURE

A. Training Infrastructure

- Intel Xeon Gold 6126 12-core CPU with 128 GB RAM.
- NVIDIA Tesla V100 GPU.
- CUDA Toolkit 10.1.243.
- PyTorch version 1.1.0.
- Python version 3.7.9.

This cyberinfrastructure for training is provided and managed by the Research Technologies division at the Indiana University which supported our work in part by Shared University Research grants from IBM Inc. to Indiana University and Lilly Endowment Inc. through its support for the Indiana University Pervasive Technology Institute [10].

B. Testing Infrastructure

- NXP BlueBox 2.0 ARM-based autonomous embedded development platform.
- Intempora RTMaps Remote Studio version 4.8.0.
- CIFAR-10, CIFAR-100 and ImageNet Datasets.
- PyTorch version 1.1.0.
- Python version 3.7.9.

VII. EXPERIMENT AND RESULTS

Training results presented in this report are based on the evaluation of image classification performance of CondenseNeXt CNN on three benchmarking datasets: CIFAR-10, CIFAR-100 and ImageNet. CondenseNeXt was designed and developed in PyTorch framework and trained on NVIDIA’s Tesla V100 GPU with standard data augmentation scheme [11], Nesterov Momentum Weight of 0.9, Stochastic Gradient Descent (SGD), cosine shape learning rate and dropout rate of 0.1 for all three datasets discussed in this section.

A. CIFAR-10 Classification

CIFAR-10 dataset [9], [12] was first introduced by Alex Krizhevsky in [13]. It is one of the most widely used datasets for evaluating a CNN in the field of deep learning research. There are 60,000 RGB images of 10 different classes of size 32×32 pixels divided into two sets of 50,000 for training and 10,000 for testing.

CondenseNeXt was trained with a single crop of inputs on CIFAR-10 dataset for 200 epochs, batch size of 64 and features \( k \) of 8-16-32. Using RTMaps Remote Studio, an image classification script was developed using Python scripting language and evaluated on NXP BlueBox for single image classification analysis. Table I provides a comparison of performance between CondenseNet and CondenseNeXt CNN in terms of FLOPs, parameters, and Top-1 and Top-5 error rates. Figure 5 provides a screenshot of the RTMaps console.

B. CIFAR-100 Classification

CIFAR-100 dataset was also first introduced by Alex Krizhevsky in [13] along side CIFAR-10 dataset. It is also one of the many popular choices of datasets in the field of deep learning research. Just like CIFAR-10 dataset, there are 60,000 RGB images in total. However, it has 100 different classes, where each class contains 600 images of size 32×32 pixels divided into two sets of 50,000 for training and 10,000 for testing. CIFAR-100 classes are mutually exclusive of CIFAR-10 classes. For example, CIFAR-100’s baby, chimpanzee and rocket classes are not part of the CIFAR-10 classes.

CondenseNeXt was trained with a single crop of inputs on CIFAR-100 dataset for 600 epochs, batch size of 64 and features \( k \) of 8-16-32. Using RTMaps Remote Studio, an image classification script was developed using Python scripting language and evaluated on NXP BlueBox for single image classification analysis. Table I provides a comparison of performance between CondenseNet and CondenseNeXt CNN in terms of FLOPs, parameters, and Top-1 and Top-5 error rates. Figure 6 provides a screenshot of the RTMaps console.
Table I provides a comparison between CondenseNet (the baseline architecture) vs. CondenseNeXt (our ultra-efficient deep neural network architecture) in terms of performance each utilizing the training setup and infrastructure as outlined in section 6 and 7 in this paper.

### C. ImageNet Classification

ImageNet was introduced by an AI researcher Dr. Fei-Fei Li along with a team of researchers at a 2009 IEEE Conference on Computer Vision and Pattern Recognition (CVPR) in Florida [14]. This dataset is built according to the WordNet hierarchy where each node in the hierarchy corresponds to over five hundred images. In total, there are over 14 million images in this dataset that have been hand-annotated and labelled by the team.

CondenseNeXt was trained with a single crop of inputs on the entire ImageNet dataset for 120 epochs with a Group Lasso rate of 0.00001, batch size of 256, features of 8-16-32-64-128 and four Nvidia V100 GPUs using Data Parallelism technique. An image classification script was developed in RTMaps Remote Studio and evaluated on NXP BlueBox for single image classification analysis. Table I provides a comparison of performance between CondenseNet and CondenseNeXt CNN in terms of FLOPs, parameters, and Top-1 and Top-5 error rates. Figure 7 provides a screenshot of the RTMaps console.

### VIII. Conclusion

In this paper, we demonstrate the performance of CondenseNeXt CNN which is an ultra-efficient deep convolutional neural network architecture for ARM-based embedded computing platforms without CUDA enabled GPU(s). Extensive training from scratch and analysis have been conducted on three benchmarking datasets: CIFAR-10, CIFAR-100 and ImageNet. It achieves state-of-the-art image classification performance on CIFAR-10 dataset with a 4.79% Top-1 error rate, on CIFAR-100 dataset with a 21.98% Top-1 error rate and ImageNet dataset with a 7.91% single model and single crop Top-5 error rate. Our experiments on NXP’s BlueBox further validate the effective use Depthwise Separable Convolutional layers and Model Compression techniques implemented to discard inconsequential elements and to reduce FLOPs without affecting overall performance of the neural network. In the future, we will explore different applications with CondenseNeXt such as image segmentation and object detection to better exploit different opportunities for OpenCV applications.
Figure 7. Evaluation of CondenseNeXt on ImageNet dataset when deployed on NXP BlueBox 2.0 using RTMaps Remote Studio version 4.8.0 for classifying an image of a street sign and outputting the predicted class in the RTMaps console.

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