**You Only Search Once: On Lightweight Differentiable Architecture Search for Resource-Constrained Embedded Platforms**

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**ABSTRACT**

Benefiting from the search efficiency, differentiable neural architecture search (NAS) has evolved as the most dominant alternative to automatically design competitive deep neural networks (DNNs). We note that DNNs must be executed under strictly hard performance constraints in real-world scenarios, for example, the runtime latency on autonomous vehicles. However, to obtain the architecture that meets the given performance constraint, previous hardware-aware differentiable NAS methods have to repeat a plethora of search runs to manually tune the hyper-parameters by trial and error, and thus the total design cost increases proportionally. To resolve this, we introduce a lightweight hardware-aware differentiable NAS framework dubbed LightNAS, striving to find the required architecture that satisfies various performance constraints through a one-time search (i.e., *you only search once*). Extensive experiments are conducted to show the superiority of LightNAS over previous state-of-the-art methods. Related codes will be released at https://github.com/stepbystep/LightNAS.

**1 INTRODUCTION**

Deep neural networks (DNNs) are becoming ubiquitous across a plethora of intelligent embedded applications such as virtual reality (VR) [1] and object detection/tracking [2], enabling entirely new on-device experiences [3]. Nonetheless, given that the network design space is tremendously large [4, 5], manually designing competitive DNNs requires considerable human efforts to determine the optimal network configuration. To address this, neural architecture search (NAS) [6] has recently flourished, which is dedicated to automating the design of top-performing DNNs. In the literature, NAS studies can be mainly divided into reinforcement learning [6], evolution [7], and gradient-based [8] (a.k.a., differentiable) categories. However, both reinforcement learning and evolution-based NAS approaches suffer from prohibitive search overheads (e.g., over 2,000 GPU days [6] and 3,150 GPU days [7]), whereas the differentiable counterpart is of great search efficiency that dramatically reduces the search cost by multiple orders of magnitude (e.g., 1 GPU day [8]).

Despite the significant progress achieved so far, the early differentiable NAS approaches [8, 9] are hardware-agnostic since they merely focus on searching for competitive architectures in terms of the accuracy, regardless of other critical performance metrics such as the on-device latency and energy, which are of paramount importance for AI-empowered applications, especially on resource-constrained embedded platforms [3]. Among these, [9] strives to design lightweight DNNs according to the number of floating-point operations (FLOPs), but the number of FLOPs is an inaccurate proxy, which cannot accurately reflect the actual latency and energy consumption on target hardware (see Figure 2). To this end, several hardware-aware differentiable NAS methods are then proposed [4, 5, 10], which incorporate the on-device latency into the search objective as soft constraints to penalize the architecture candidate with high latency, thereby being able to generate hardware-friendly architecture solutions with low inference latency.

But even so, we, in practice, should consider not only the explicit search cost – the time required to run one single search, but also the implicit search cost – the time required for manual hyper-parameter tuning in order to find the desired architecture. For instance, in real-world scenarios like autonomous vehicles, DNNs must be executed under strictly hard latency constraints. Unfortunately, to obtain the architecture with competitive accuracy while satisfying the given latency constraint, previous hardware-aware differentiable NAS methods [4, 5, 10] have to perform multiple search runs to manually tune the hyper-parameters (see \(\lambda\) in Eq (3)) by trial and error. As a result, the total design cost increases proportionally (empirically by \(\times 10\) times). Meanwhile, during the search process [4, 5, 10], multiple sub-networks (paths) need to be optimized at the same time (see Table 1), thereby leading to non-trivial memory overheads. And even worse, the above multi-path paradigm introduces considerable inconsistency between search and evaluation since the stand-alone architecture at the evaluation stage is a single-path sub-network [11]. As such, it is natural to ask the following question:

![Figure 1: An intuitive illustration of the proposed LightNAS method.](https://example.com/figure1)

**Is it possible to find the required architecture that strictly satisfies the given performance constraint through a one-time architecture search in both differentiable and lightweight manners?**

To answer the question outlined above, we propose a lightweight hardware-aware differentiable NAS method dubbed LightNAS, in which we primarily focus on the most dominant performance constraint, i.e., latency (see Figure 1). LightNAS is compared against previous NAS methods in Table 1. Our contributions are as follows:

- We introduce an accurate yet efficient predictor to estimate the latency so as to avoid the tedious on-device measurements, which is also generalizable to other hardware metrics. (see Section 3.2)
- We propose a lightweight differentiable search method to reduce the optimization complexity to the single-path level, thereby effectively resolving the memory bottleneck. (see Section 3.3)
- We incorporate the latency predictor into LightNAS to achieve hardware-aware architecture search. Instead of manually tuning the hyper-parameters to guarantee the given latency constraint,
2 BACKGROUND

In this section, we first introduce the preliminaries on differentiable NAS [8], and then present the motivations of this paper.

2.1 Preliminaries on Differentiable NAS

We begin with the operator space denoted as \( O = \{\alpha_k\}_{K=1}^K \), in which each element \( \alpha_k \) represents an operator candidate. Following the weight-sharing NAS paradigm [8], an over-parameterized network is constructed, namely supernet, where each layer is composed of \( K \) operator candidates laid in \( O \). To relax the discrete network design space to become continuous, operators in the supernet are assigned with a set of architecture parameters \( \alpha \in \mathbb{R}^{L \times K} \), where \( L \) corresponds to the number of layers in the supernet. The structure of the supernet is visualized in Figure 4. Therefore, we are able to formulate the output of the supernet \( F(x) \) as follows:

\[
F(x) = \sum_{l=1}^{L} \sum_{k=1}^{K} \left( \frac{\exp(\alpha_{l,k}^T x)}{\sum_{k'=1}^{K} \exp(\alpha_{l,k'}^T x)} \cdot o_k(x_l) \right), \quad \text{s.t.}, \ \alpha_k \in O
\]

where \( x_l \) is the input of \( l \)-th layer, and \( x \) is the initial input. Due to the continuous relaxation, both network weights \( w \) and architecture parameters \( \alpha \) can be optimized with gradient descent [8], or more specifically, a bi-level optimization strategy is applied, including a training phase to optimize \( w \) and a validation phase to optimize \( \alpha \):

\[
\begin{align*}
\min_{\alpha} & \quad \mathcal{L}_{\text{valid}}(w'(\alpha), \alpha) \\
\text{s.t.} & \quad w'(\alpha) = \arg\min_w \mathcal{L}_{\text{train}}(w, \alpha)
\end{align*}
\]

where \( \mathcal{L}_{\text{train}}(\cdot) \) and \( \mathcal{L}_{\text{valid}}(\cdot) \) are the loss functions accumulated on the training and validation datasets, respectively. Subsequently, once the architecture search process terminates, we can determine the searched architecture by reserving the strongest operator for each layer while other operators are discarded, where the operator strength is defined as \( \exp(\alpha_{l,k}^T) / \sum_{k'=1}^{K} \exp(\alpha_{l,k'}^T) \). For more technical details about differentiable NAS, you may refer to DARTS [8].

2.2 Motivations

The objective defined in Eq (2), however, focuses on the accuracy-only optimization, regardless of other critical performance metrics like the latency and energy on target hardware. As a result, it derives the architecture with competitive accuracy, which comes at the cost of extremely high computational complexity, and thus cannot be deployed on resource-limited embedded systems [3]. To tackle this issue, previous NAS methods [9, 12] exploit the multi-objective optimization scheme to achieve trade-offs between accuracy and efficiency, where they use hardware-agnostic metrics like FLOPs to denote the network efficiency. Unfortunately, the number of FLOPs does not always reflect the on-device latency and energy as shown in Figure 2, where we find that architectures with the same latency or energy could greatly differ regarding the number of FLOPs.

Subsequently, several hardware-aware differentiable NAS works are proposed [4, 5, 10, 13], i.e., they integrate the on-device latency into the optimization objective to penalize the architecture with high latency, which can be formally expressed as follows:

\[
\min_{\alpha} \quad \mathcal{L}_{\text{valid}}(w'(\alpha), \alpha) + \lambda \cdot \mathcal{L}_{\text{diff}}(\alpha)
\]

where \( \mathcal{L}_{\text{diff}}(\cdot) \) denotes the latency of the architecture encoded by \( \alpha \). \( \lambda \geq 0 \) is a constant to control the trade-off magnitude between accuracy and latency. In fact, the above optimization objective is able to derive hardware-friendly architectures with both high accuracy and low latency, but only if a suitable \( \lambda \) is applied. The intuition behind this is that, if \( \lambda \) is too small, the latency penalty term \( \mathcal{L}_{\text{diff}}(\alpha) \) will be effectively ignored. In contrast, if \( \lambda \) is too large, we will end up with the architecture that has extremely low latency on target hardware but sub-optimal accuracy on target task. Meanwhile, in real-world scenarios like autonomous vehicles, DNNs must be executed under strictly hard latency constraints [3]. Thus, to find the architecture that satisfies the specified latency constraint, we have to perform a hyper-parameter sweep to manually tune \( \lambda \) by trial and error.

Nonetheless, the above manual hyper-parameter sweep requires us to run multiple searches (empirically 10), thereby increasing the total design cost by \( \times10 \) times. To illustrate this point, we present a motivational experiment, in which we take FBNet [5] as the search engine and perform a series of search experiments under different settings of \( \lambda \in [0, 1] \). Then, after the search process is finished, we train the searched architecture from scratch on ImageNet for 50 epochs to quickly evaluate the accuracy. Meanwhile, we measure the corresponding latency on Nvidia Jetson AGX Xavier. As seen in Figure 3, \( \lambda \) can effectively control the trade-off magnitude between accuracy and latency, but it is quite difficult to tune. For example, to obtain the architecture with the required latency of 24 ms, we should set \( \lambda \) to 0.001. But, next time if we require an architecture with the latency of 26 ms, we need to manually tune \( \lambda \) within the range of \([0.00075, 0.001]\) as shown in Figure 3, inevitably leading to a plethora of trial-and-errors. Thus, to avoid this, we focus on...
finding the optimal architecture that exactly meets the given latency requirement through a one-time search (i.e., you only search once).

3 METHODOLOGY

In this section, we first elaborate on each component of the proposed LightNAS, and then discuss the relationships with previous methods to further distinguish the technical contributions of this work.

3.1 Search Space Design

In the literature, differentiable NAS methods like DARTS [8] and its variants [9, 13] explicitly advocate for the cell-level architecture search. However, as pointed out in [14], enabling the layer diversity helps to strike the right balance between accuracy and efficiency. Thus, we closely follow the layer-wise architecture space design [4, 5, 10] as illustrated in Figure 4. Specifically, the operator space \( O \) is built upon MobileNetV2 [15], in which we allow a set of MBConv layers with diverse kernel sizes of \{3, 5, 7\} and expansion ratios of \{3, 6\}. Meanwhile, we include SkipConnect, which is computation-free, to achieve flexible architecture search in terms of the network depth [4, 5]. As such, we have \(|O| = 7\), and given that the supernet consists of \( L = 22 \) searchable operators where the first one is fixed [4], the architecture space size of LightNAS is then calculated as \(|A| = 7^{21} = 5.6 \times 10^{17}\). Unless specified otherwise, we do not apply extra techniques like Squeeze-and-Excitation (SE) module [16] and Swish activation [17] in order to ensure fair comparisons with previous hardware-aware NAS methods [4, 5, 10, 18].

3.2 Latency Prediction

Nonetheless, given that the search space of NAS is prohibitively large (e.g., \(|A| \approx 5.6 \times 10^{17}\) in LightNAS), measuring the on-device latency for every possible architecture \( arch \) is computationally expensive [4]. To this end, we introduce an accurate yet efficient predictor to approximate the on-device latency for \( arch \in A \) with negligible computation overheads. With this goal in mind, we first encode \( arch \) with a sparse matrix \( \sigma \in \{0, 1\}^{L \times K} \), where \( \sigma^k_l = 1 \) indicates that the \( k \)-th operator is reserved for the \( l \)-th layer of \( arch \) while others are discarded. As such, we can calculate \( \sigma \) as follows:

\[
\sigma^k_l = \begin{cases} 
1, & \text{if } a^k_l = \arg \max \{|a^k_l|\} \\
0, & \text{otherwise}
\end{cases}
\]  

(4)

Therefore, since the supernet is composed of \( L \) searchable layers, we derive that the architecture encoding matrix \( \sigma \) contains \( L \) entries with values of \( 1 \), whereas other entries are with values of \( 0 \).

Subsequently, we leverage a multi-layer perceptron (MLP) model for the prediction purpose, which consists of three fully-connected layers with 128, 64, and 1 neurons. Meanwhile, we sample 10,000 random architectures from \( A \) and measure the inference latency on Nvidia Jetson AGX Xavier, respectively. The sampled architectures and latency measurements are then split into two folds with 80% as the training set and 20% as the validation set. Next, we flatten \( \sigma \) corresponding to each architecture and feed it into the MLP-based latency predictor. The predicted results on the validation set are illustrated in Figure 5 (Left), where we find that the proposed latency predictor achieves an extremely low root-mean-square error (RMSE) of 0.04 ms. More importantly, once the latency predictor is well trained, it is able to estimate the on-device latency for \( arch \in A \) through a one-time inference, which takes less than one millisecond, and thus introduces trivial computation overheads.

Furthermore, we compare the proposed latency predictor with the latency lookup table (LUT) as widely used in recent NAS works [4, 5, 18]. The predicted results of LUT are shown in Figure 5 (Right), where we find that there exists a consistent gap (about 11.48 ms) between the predicted latency and the measured ground truth. And even though the above prediction gap is eliminated, the RMSE of LUT still remains 0.41 ms, which is much worse than the proposed latency predictor. We note that the goal of this work is to search for the architecture that strictly meets the given latency requirement, and thus an accurate latency predictor is of great necessity.

3.3 Lightweight Architecture Search

Recall that previous differentiable NAS methods [5, 8, 9] require to simultaneously optimize multiple sub-networks (paths), inevitably causing the memory bottleneck [4] as well as violating the equality principle [11]. To this end, we propose a lightweight differentiable architecture search method to reduce the optimization complexity to the single-path level, thereby effectively resolving the memory bottleneck. Let \( arch = \{op_l\}_{l=1}^L \) denote the stand-alone architecture candidate. Therefore, once the search process terminates, we can calculate the probability that \( arch \) is selected as follows:

\[
P(arch) = \prod_{l=1}^L P(op_l = o_l), \quad s.t., \quad o_k \in O
\]  

(5)

where \( P(op_l = o_k) \) is the probability of \( o_k \) being at the \( l \)-th layer:

\[
P(op_l = o_k) = \frac{\exp(a^k_l)}{\sum_{k=1}^K \exp(a^k_l)}
\]  

(6)

For the sake of simplicity, we replace \( P(op_l = o_k) \) with \( p^k_l \). To derive \( arch \), one straightforward method is to optimize the architecture parameters \( \alpha \) over the search space \( A \). However, given that the search space of LightNAS is prohibitively large as seen in Section 3.1, iterating every possible architecture over \( A \) inevitably requires a huge amount of computation resources [5, 8]. To alleviate this issue, we further leverage the Gumbel Softmax reparameterization trick.
where \( \eta \) is the softmax temperature, which is initialized as 5 and then gradually decays to zero. We note that, once converged, the above relaxation is unbiased as proved in [19] that \( \lim_{\tau \rightarrow 0} \bar{P}_i^k = P_i^k \). We then re-formulate the output of the supernet \( F(x) \) as follows:

\[
F(x) = \sum_{l=1}^{L} \sum_{k=1}^{K} \left( \bar{P}_i^k \cdot o_k(x_i) \right), \text{ s.t. } o_k \in O
\]

(8)

where \( \bar{P} \) is the binarization of \( P \) that can be expressed as follows:

\[
\bar{P}_i^k = \begin{cases} 
1, & \text{if } \bar{P}_i^k = \arg \max || \bar{P}_i || \\
0, & \text{otherwise}
\end{cases}
\]

(9)

As a result, we only need to activate one single-path sub-network during the forward propagation of the supernet since \( \bar{P} \in \{0, 1\}^{L \times K} \). The intuition behind this is that the output of the supernet only depends on operators with \( \bar{P}_i^k = 1 \) as seen in Eq (8). To summarize, the above single-path mechanism achieves two main benefits. On the one hand, it brings significant memory efficiency because the optimization complexity has been reduced to the single-path level, and considering that the GPU memory is constant, we are allowed to use a larger batch size to speed up the search process. On the other hand, the above single-path mechanism forces the search process to strictly satisfy the equality principle [11], i.e., the supernet and the searched sub-network should be trained in the same manner.

### 3.4 Hardware-Aware Architecture Search

The search method described above merely optimizes the search process in terms of the accuracy, while ignoring other critical performance metrics, e.g., the on-device latency as the most dominant one [14]. Thus, we further integrate the latency predictor into LightNAS to achieve hardware-aware architecture search. The optimization objective of LightNAS is then formulated as follows:

\[
\min_{\alpha} \mathcal{L}_{\text{coald}}(w', \alpha) + \lambda \cdot \left( \frac{\text{LAT}(\alpha)}{T} - 1 \right)
\]

(10)

where \( \text{LAT}(\alpha) \) represents the predicted latency of the architecture encoded by \( \alpha \), and \( T \) is the specified latency constraint. Besides, \( \lambda \) denotes the coefficient to control the trade-off magnitude between accuracy and latency. Different from previous NAS methods [4, 5], \( \lambda \) in Eq (10) is not a constant but a hyper-parameter to be optimized. Therefore, instead of manual hyper-parameter tuning, LightNAS automatically learns the optimal hyper-parameter configuration during the search process, which maximizes the accuracy while strictly satisfying the specified latency constraint \( \text{LAT}(\alpha) = T \). For the sake of simplicity, we use \( \mathcal{L}(w, \alpha, \lambda) \) to denote the objective defined in Eq (10). Subsequently, \( w \) and \( \alpha \) are updated with gradient descent [8], whereas \( \lambda \) is optimized using gradient ascent:

\[
\begin{align*}
\frac{dw}{dt} &= w - \eta_w \cdot \frac{\partial \mathcal{L}(w, \alpha, \lambda)}{\partial w}, \quad \alpha^* = \alpha - \eta_\alpha \cdot \frac{\partial \mathcal{L}(w, \alpha, \lambda)}{\partial \alpha} \\
\lambda^* &= \lambda + \eta_\lambda \cdot \frac{\partial \mathcal{L}(w, \alpha, \lambda)}{\partial \lambda} = \lambda + \eta \cdot \frac{\text{LAT}(\alpha) - T}{\text{LAT}(\alpha) - 1} 
\end{align*}
\]

(11)

where \( \eta_w, \eta_\alpha, \) and \( \eta_\lambda \) are the learning rates of \( w, \alpha, \) and \( \lambda, \) respectively. After demonstrating what the proposed method is, we then analyze why it guarantees \( \text{LAT}(\alpha) = T \). Recall that a larger \( \lambda \) derives the architecture with low latency, whereas a smaller \( \lambda \) generates the architecture with high latency as shown in Figure 3. Thus, if \( \text{LAT}(\alpha) > T \), the gradient ascent scheme increases \( \lambda \) to reinforce the latency regularization magnitude. As a result, \( \text{LAT}(\alpha) \) decreases towards \( T \) in the next search iteration. Likewise, if \( \text{LAT}(\alpha) < T \), the gradient ascent scheme then decreases \( \lambda \) to diminish the latency regularization magnitude, and the search engine therefore increases \( \text{LAT}(\alpha) \) towards \( T \) in the next parameter update. Consequently, the search engine ends up with the architecture with optimal accuracy while at the same time satisfying the given constraint \( \text{LAT}(\alpha) = T \).

To summarize, unlike previous hardware-aware differentiable NAS methods [4, 5, 10] that require multiple trial-and-errors to find the desired architecture with the latency of \( T \), LightNAS only needs to search once, greatly improving the search efficiency.

Meanwhile, given that \( \mathcal{L}(w, \alpha, \lambda) \) is differentiable with respect to \( w \) as seen in [8], we then provide the differentiable analysis of \( \alpha \):

\[
\frac{\partial \mathcal{L}(w, \alpha, \lambda)}{\partial \alpha} = \frac{\partial \mathcal{L}_{\text{coald}}}{\partial \alpha} + \frac{\lambda}{T} \cdot \frac{\partial \text{LAT}(\alpha)}{\partial \alpha}
\]

(12)

\[
\frac{\partial \mathcal{L}(w, \alpha, \lambda)}{\partial \alpha} = \frac{\partial \mathcal{L}_{\text{coald}}}{\partial \alpha} + \frac{\lambda}{T} \cdot \frac{\partial \text{LAT}(\alpha)}{\partial \alpha}
\]

where \( \frac{\partial \mathcal{L}_{\text{coald}}}{\partial \alpha} \) is the derivative of the coalesced loss function and \( \frac{\partial \text{LAT}(\alpha)}{\partial \alpha} \) is determined by the network weights of the latency predictor, which can be obtained through a one-time backward propagation. In addition to these terms, other terms in Eq (12) are apparently differentiable since only continuous transformations are involved [8, 19]. Please note that the differentiable analysis of \( \lambda \) is given in Eq (11).

### 3.5 Relationships with Previous Methods

First of all, to obtain the architecture that satisfies the given latency constraint, previous hardware-aware differentiable NAS methods [4, 5, 10] require to perform a hyper-parameter sweep to manually tune the trade-off coefficient \( \lambda \) by trial and error (see Section 2.2). The total design cost therefore increases proportionally (empirically by \( \times 10 \) times). We note that previous NAS methods only report the explicit search cost such as the time needed to run one single search, whereas the implicit search cost like the time required to manually tune \( \lambda \) is excluded. In contrast, this paper focuses on finding the required architecture through a one-time search so as to eliminate the implicit search cost, thereby bringing considerable search efficiency and flexibility. It is worth noting that reinforcement learning and evolution-based NAS approaches [14, 18] can achieve the same goal as LightNAS, but suffer from prohibitive search overheads (e.g., 40,000 GPU hours in [14] and 10 GPU hours in LightNAS).

Meanwhile, due to the multi-path paradigm, previous differentiable NAS methods [5, 8, 9] suffer from the memory bottleneck, which violates the equality principle as well [11]. To this end, we propose the lightweight differentiable architecture search method, effectively reducing the optimization complexity to the single-path level. Owing to the single-path mechanism, the optimization gap between the supernet and the searched sub-network is bridged [11]. Besides, different from the latency lookup table (LUT) [5], the
proposed predictor can approximate not only the on-device latency but also other hardware metrics like the runtime energy as seen in Figure 8. Without loss of generality, LightNAS can be effortlessly plugged into various scenarios, in which we only need to replace the latency predictor with the predictor of the target scenario. Finally, we compare LightNAS against previous NAS methods in Table 1.

4 EXPERIMENTS

In this section, we extensively evaluate the proposed LightNAS on a cutting-edge embedded platform called Nvidia Jetson AGX Xavier. Here, the MAXN power mode is applied to maximize the hardware performance. Meanwhile, to avoid resource underutilization, all the measurements are reported with an input batch size of 8 [4].

4.1 Dataset and Implementation Details

Dataset. All the experiments are directly conducted on ImageNet [21]. Specifically, ImageNet consists of 1,000 categories, and 1.28M training images and 50K validation images, all of which are roughly equally distributed across all categories. Following the network design conventions [14, 15], we use the mobile setting, where the image size is set to 224×224, and the number of multi-add operations is strictly under 600M during the runtime inference.

Architecture Search Settings. In LightNAS, the architecture search settings closely follow FBNet [5], in which we randomly sample 100 categories from ImageNet to optimize both network weights w and architecture parameters α. Specifically, we train the stochastic supernet for 90 epochs with an input batch size of 128. In the first 10 epochs, we only update w, whereas α is frozen [5]. Subsequently, the optimization steps of w and α alternate in each epoch. To optimize w, we use the SGD optimizer with a learning rate of 0.1

Table 2: Comparisons with state-of-the-art architectures on ImageNet [21]. † denotes architectures that use extra techniques like Swish activation and Squeeze-and-Excitation (SE) module [16, 17]. (annealed down to zero following the cosine schedule), a momentum of 0.9, and a weight decay of $3 \times 10^{-5}$. To optimize α, we employ the Adam optimizer [8] with a learning rate of 0.001 and a weight decay of $1 \times 10^{-5}$. Besides, as discussed in Section 3.4, the trade-off coefficient λ in LightNAS is not a constant but a parameter to be optimized. For this reason, we initialize λ as zero and optimize λ with the gradient ascent scheme, where the learning rate is fixed to 0.0005. Finally, we denote the architectures searched by LightNAS as LightNets. It is worth noting that all the architecture search experiments are conducted on one single GeForce RTX 3090 GPU.

Architecture Evaluation Setting. We simply follow the training protocols as widely used in previous NAS methods [4, 5] to evaluate the searched LightNets on ImageNet [21]. Specifically, we retrain LightNets from scratch for 360 epochs with a batch size of 1024 on 4 GeForce RTX 3090 GPUs, in which the standard data augmentation protocols are applied [5] throughout this work. The default optimizer is SGD with a momentum of 0.9 and a weight decay of $4 \times 10^{-5}$. Besides, the learning rate is initialized as 0.5, which gradually decays to zero following the cosine schedule. Similar to DARTS [8], we linearly warm up the learning rate from 0.1 to 0.5 in the first 5 epochs. Meanwhile, we insert the Dropout module before the final classification layer, where the dropout ratio is set to 0.2 [5].

4.2 Experimental Results

Architecture Search Results. We visualize the LightNets searched under different latency constraints in Figure 6, which span from 20 ms to 30 ms. Different from MobileNetV2 [15] that simply stacks the same operator across all network layers, LightNAS effectively enables the layer diversity to strike the right balance between accuracy and latency. Meanwhile, given a larger latency constraint, we observe that the search engine of LightNAS encourages to search for the desired architecture that goes deeper and wider.

Architecture Evaluation Results. Results and comparisons with previous state-of-the-art architectures are summarized in Table 2, where we find that the searched LightNets strictly satisfy the given latency constraints, while at the same time coming at an extremely low search cost of 10 GPU hours. More importantly, all LightNets are
obtained through a one-time search, and thus the manual trial-and-errors over the trade-off coefficient $\lambda$ are eliminated (see Section 2.2). Meanwhile, under the same latency constraints, LightNets consistently outperform previous state-of-the-art architectures in terms of the accuracy on ImageNet [21]. We note that FBNet [5] is the most relevant work to LightNAS in the literature. For comparisons, we implement FBNet and exploit FBNet to perform the architecture search on Nvidia Jetson AGX Xavier, where the searched architecture is denoted as FBNet-Xavier. As shown in Table 2, LightNet-24ms achieves a +0.9% higher top-1 accuracy than FBNet-Xavier while with a comparable latency constraint of 24 ms.

![Figure 8: Left: the predicted results with the predictor in Section 3.2. Right: the search process under the energy constraint of 500 mJ.](image)

**4.3 Ablation Studies and Discussions**

**Architecture Search Stability.** We visualize the search process of LightNAS under various latency constraints in Figure 7, where each figure is drawn by averaging three different search runs. Notably, LightNAS always ends up with the architecture that strictly meets the given latency constraint. Meanwhile, the search engine explicitly focuses on searching for the optimal architecture around the target latency, which aligns with the analysis in Section 3.4.

**Generality to Energy-Critical Tasks.** To generalize LightNAS to the energy-critical scenarios, we first apply the proposed predictor to approximate the energy consumption for $\text{arch} \in \mathcal{A}$ as shown in Figure 8 (Left). Please note that the energy measurement inevitably suffers from noises caused by the hardware temperature. Then, we integrate the energy predictor into LightNAS and visualize the search process in Figure 8 (Right), in which find that LightNAS is able to effectively generalize to the energy-critical tasks.

**Transferability to Object Detection.** We next evaluate LightNets on the object detection task, in which we use a popular detection framework named SSDLite [22] and treat different architectures as drop-in backbone replacements. All the architectures are trained from scratch (i.e., without loading pretrained weights) under the same settings on COCO2017. As summarized in Table 3, LightNets achieve better performance than the compared architectures in terms of both detection accuracy and execution efficiency.

### Comparisons with Scaling Techniques

Another alternative to guarantee the specified latency requirements is the model scaling technique [14]. Given that the search space of LightNAS is based on MobileNetV2 [15], we further scale up MobileNetV2 with respect to width/resolution to accommodate different latency requirements. As seen in Figure 9, under the same latency constraints, LightNets clearly outperform those counterparts in terms of the accuracy.

**Ablation of the Squeeze-and-Excitation (SE) module** [16].

![Figure 9: Performance comparisons with different model scaling techniques [14]. Here, all the models are trained for only 50 epochs.](image)

### 5 CONCLUSION

This paper proposes, designs, and validates a lightweight hardware-aware differentiable NAS framework dubbed LightNAS. In contrast to previous NAS methods that require a plethora of trial-and-errors, LightNAS is able to effectively and efficiently find the architecture that strictly satisfies the specified performance constraint through a one-time search. Extensive experiments are conducted to show the superiority of LightNAS over state-of-the-art NAS approaches.

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## Table 3: Comparisons with state-of-the-art backbones on COCO2017.

| Architecture     | Top-1 (%) | Top-2 (%) | FLOPs (M) | Latency (ms) |
|------------------|-----------|-----------|-----------|--------------|
| MobileNetV2 [15] | 34.3      | 20.5      | 40.2      | 72.6         |
| MnasNet-A1 [14]  | 36.0      | 21.4      | 41.5      | 74.2         |
| FBNet-C [5]      | 36.2      | 21.9      | 41.5      | 76.5         |
| OFA-A [18]       | 36.7      | 21.9      | 41.3      | 75.4         |
| LightNet-20ms    | 35.2      | 21.2      | 41.0      | 67.1         |
| LightNet-24ms    | 36.3      | 21.7      | 42.2      | 68.6         |
| LightNet-28ms    | 36.9      | 22.8      | 41.8      | 69.7         |

## Table 4: Ablation of the Squeeze-and-Excitation (SE) module [16].

| Architecture     | Top-1 (%) | Top-2 (%) | FLOPs (M) | Latency (ms) |
|------------------|-----------|-----------|-----------|--------------|
| LightNet-20ms-SE | 75.4 (+0.4) | 92.3 (+0.1) | 356 (+2) | 20.9 (+0.9) |
| LightNet-24ms-SE | 76.1 (+0.1) | 92.5 (+0.3) | 352 (+3) | 23.4 (+1.1) |
| LightNet-24ms-SE | 75.9 (+0.1) | 92.6 (+0.3) | 385 (+2) | 25.5 (+1.6) |
| LightNet-26ms    | 76.3 (+0.1) | 92.8 (+0.2) | 435 (+3) | 27.7 (+1.6) |
| LightNet-28ms    | 76.5 (+0.1) | 92.8 (+0.1) | 464 (+4) | 30.3 (+2.1) |
| LightNet-30ms    | 77.0 (+0.6) | 93.1 (+0.2) | 491 (+4) | 31.9 (+1.8) |
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