HAQ: Hardware-Aware Automated Quantization with Mixed Precision

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Abstract

Model quantization is a widely used technique to compress and accelerate deep neural network (DNN) inference. Emergent DNN hardware accelerators begin to support mixed precision (1-8 bits) to further improve the computation efficiency, which raises a great challenge to find the optimal bitwidth for each layer: it requires domain experts to explore the vast design space trading off among accuracy, latency, energy, and model size, which is both time-consuming and sub-optimal. There are plenty of specialized hardware for neural networks, but little research has been done for specialized neural network optimization for a particular hardware architecture. Conventional quantization algorithm ignores the different hardware architectures and quantizes all the layers in a uniform way. In this paper, we introduce the Hardware-Aware Automated Quantization (HAQ) framework which leverages the reinforcement learning to automatically determine the quantization policy, and we take the hardware accelerator’s feedback in the design loop. Rather than relying on proxy signals such as FLOPs and model size, we employ a hardware simulator to generate direct feedback signals (latency and energy) to the RL agent. Compared with conventional methods, our framework is fully automated and can specialize the quantization policy for different neural network architectures and hardware architectures. Our framework effectively reduced the latency by 1.4-1.95× and the energy consumption by 1.9× with negligible loss of accuracy compared with the fixed bitwidth (8 bits) quantization. Our framework reveals that the optimal policies on different hardware architectures (i.e., edge and cloud architectures) under different resource constraints (i.e., latency, energy and model size) are drastically different. We interpreted the implication of different quantization policies, which offer insights for both neural network architecture design and hardware architecture design.

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A widely adopted approach is to rely on some proxy signals with knowledge of both machine learning and hardware architecture's energy consumption of a given model on the hardware. Therefore, it is important to directly involve the hardware architecture's performance feedback into the design loop. Also, as demonstrated in Table 1, the quantization solution optimized on one hardware might not be optimal on the other, which raises the demand for specialized policies for different hardware architectures.

To this end, we propose the Hardware-Aware Automated Quantization (HAQ) framework that leverages reinforcement learning to automatically predict the quantization policy given the hardware’s feedback. The RL agent decides the bitwidth of a given neural network in a layer-wise manner. For each layer, the agent receives the layer configuration and statistics as observation, and it then outputs the action which is the bitwidth of weights and activations. We then leverage the hardware accelerator as the environment to obtain the direct feedback from hardware to guide the RL agent to satisfy the resource constraints. After all layers are quantized, we finetune the quantized model for one more epoch, and feed the validation accuracy after short-term retraining as the reward signal to our RL agent. During the exploration, we leverage the deep deterministic policy gradient (DDPG) [17] to supervise our RL agent. We also studied the quantization policy on multiple hardware architectures: both cloud and edge neural network accelerators, with spatial or temporal multi-precision design.

The contribution of this paper has four aspects:

1. **Automation**: We propose an automated framework for quantization, which does not require domain experts and rule-based heuristics. It frees the human labor from exploring the vast search space of choosing bitwidths.

2. **Hardware-Aware**: Our framework involves the hardware architecture into the loop so that it can directly reduce the latency, energy and storage on the target hardware instead of relying on proxy signals.

3. **Specialization**: For different hardware architectures, our framework can offer a specialized quantization policy that’s exactly tailored for the target hardware architecture to optimize latency and energy.

4. **Design Insights**: We interpreted the different quantization policies learned for different hardware architectures. Taking both computation and memory access into account, the interpretation offers insights on both neural network architecture and hardware architecture design.

### 2. Related Work

**Quantization.** There have been extensive explorations on compressing and accelerating deep neural networks using quantization. Han et al. [8] quantized the network weights to reduce the model size by rule-based strategies: e.g., they used human heuristics to determine the bitwidths for convolution and fully-connected layers. Courbariaux et al. [4]...
binarized the network weights into $\{-1, +1\}$; Rastegari et al. [23] and Zhou et al. [32] binarized each convolution filter into $\{-w, +w\}$; Zhu et al. [34] mapped the network weights into $\{-wN, 0, +wP\}$ using two bits; Zhou et al. [33] used one bit for network weights and two bits for activations; Jacob et al. [14] made use of 8-bit integers for both weights and activations. We refer the reader to the survey paper by Krishnamoorthi et al. [16] for a more detailed overview. These conventional quantization methods either simply assign the same number of bits to all layers or require domain experts to determine the bitwidths for different layers, while our framework automates this design process, and our learning-based policy outperforms rule-based strategies.

Efficient Models. To facilitate the efficient deployment, researchers designed hardware-friendly approaches to slim neural network models. For instance, the coarse-grained channel pruning methods [11, 20] prune away the entire channel of convolution kernels to achieve speedup. Recently, researchers have explicitly optimized for various aspects of hardware properties, including the inference latency and energy: Yang et al. [30] proposed the energy-aware pruning to directly optimize the energy consumption of neural networks; Yang et al. [31] reduced the inference time of neural networks on the mobile devices through a lookup table. Nevertheless, these methods are still rule-based and mostly focus on pruning. Our framework automates the quantization process by taking hardware-specific metric as direct rewards using a learning based method.

3. Approach

We model the quantization task as a reinforcement learning problem (Figure 2). We use the actor-critic model with DDPG agent to give the action: bits for each layer. We collect hardware counters as constraints, together with accuracy as rewards to search the optimal quantization policy. We have three hardware environments that covers edge and cloud, spatial and temporal architectures for mixed-precision accelerator. Below describes the details of the RL formulation.

3.1. Observation (State Space)

Our agent processes the neural network in a layer-wise manner. For each layer, our agent takes two steps: one for weights, and one for activations. In this paper, we introduce
a ten-dimensional feature vector $O_k$ as our observation:

If the $k^{th}$ layer is a convolution layer, the state $O_k$ is

$$O_k = (k, c, h, c_{out}, s_{kernel}, s_{stride}, s_{feat}, n_{params}, i_{dw}, i_{w/a}, a_{k-1}),$$

where $k$ is the layer index, $c$ is #input channels, $h$ is #output channels, $s_{kernel}$ is kernel size, $s_{stride}$ is the stride, $s_{feat}$ is the input feature map size, $n_{params}$ is #parameters, $i_{dw}$ is a binary indicator for depthwise convolution, $i_{w/a}$ is a binary indicator for weight/activation, and $a_{k-1}$ is the action from the last time step.

If the $k^{th}$ layer is a fully-connected layer, the state $O_k$ is

$$O_k = (k, h, h_{out}, 1, 0, s_{feat}, n_{params}, 0, i_{w/a}, a_{k-1}),$$

where $k$ is the layer index, $h$ is #input hidden units, $h_{out}$ is #output hidden units, $s_{feat}$ is the size of input feature vector, $n_{params}$ is #parameters, $i_{w/a}$ is a binary indicator for weight/activation, and $a_{k-1}$ is the action from the last step.

For each dimension in the observation vector $O_k$, we normalize it into $[0, 1]$ to make them in the same scale.

3.2. Action Space

We use a continuous action space to determine the bitwidth. The reason that we do not use a discrete action space is because it loses the relative order: e.g., 2-bit quantization is more aggressive than 4-bit and even more than 8-bit. At the $k^{th}$ time step, we take the continuous action $a_k$ (which is in the range of $[0, 1]$), and round it into the discrete bitwidth value $b_k$:

$$b_k = \text{round}(b_{min} - 0.5 + a_k \times (b_{max} - b_{min} + 1)), \quad (3)$$

where $b_{min}$ and $b_{max}$ denote the min and max bitwidth (in our experiments, we set $b_{min}$ to 2 and $b_{max}$ to 8).

Resource Constraints. In real-world applications, we have limited computation budgets (i.e., latency, energy, and model size). We would like to find the quantization policy with the best performance given the constraint.

We encourage our agent to meet the computation budget by limiting the action space. After our RL agent gives actions $\{a_k\}$ to all layers, we measure the amount of resources that will be used by the quantized model. The feedback is directly obtained from the hardware accelerator, which we will discuss in Section 3.3. If the current policy exceeds our resource budget (on latency, energy or model size), we will sequentially decrease the bitwidth of each layer until the constraint is finally satisfied.

3.3. Direct Feedback from Hardware Accelerators

An intuitive feedback to our RL agent can be FLOPs or the model size. However, as these proxy signals are indirect, they are not equal to the performance (i.e., latency, energy consumption) on the hardware. Cache locality, number of kernel calls, memory bandwidth all matters. Proxy feedback can not model these hardware functionality to find the specialized strategies (see Table 1). Instead, we use direct latency and energy feedback from the hardware accelerator as resource constraints, which enables our RL agent to determine the bitwidth allocation policy from the subtle differences between different layers: e.g., vanilla convolution has more data reuse and better locality, while depthwise convolution [3] has less reuse and worse locality, which makes it memory bounded. Such difference impacts the optimal quantization policy.

3.4. Quantization

We linearly quantize the weights and activations of each layer using the action $a_k$ given by our agent, as linearly quantized model only needs fixed point arithmetic unit which is more efficient to implement on the hardware.

Specifically, for each weight value $w$ in the $k^{th}$ layer, we first truncate it into the range of $[-c, c]$, and we then quantize it linearly into $a_k$ bits:

$$\text{quantize}(w, a_k, c) = \text{round}(\text{clamp}(w, c)/s) \times s, \quad (4)$$

where $\text{clamp}(-x, x)$ is to truncate the values into $[-x, x]$, and the scaling factor $s$ is defined as $s = c/(2^a-1) - 1$. In this paper, we choose the value of $c$ by finding the optimal value $x$ that minimizes the KL-divergence between the original weight distribution $W_k$ and the quantized weight distribution $\text{quantize}(W_k, a_k, x)$:

$$c = \arg \min_{x} \mathcal{D}_{KL}(W_k \parallel \text{quantize}(W_k, a_k, x)), \quad (5)$$

where $\mathcal{D}_{KL}(\cdot \parallel \cdot)$ is the KL-divergence that characterizes the distance between two distributions. As for activations, we quantize the values similarly except that we truncate them into the range of $[0, c]$, not $[-c, c]$ since the activation values (which are the outputs of the ReLU layers) are non-negative.

3.5. Reward Function

After quantization, we retrain the quantized model for one more epoch to recover the performance. As we have already imposed the resource constraints (latency, energy) by limiting the action space (Section 3.2), we define our reward function $R$ to be only related to the accuracy:

$$R = \lambda \times (\text{acc}_{\text{quant}} - \text{acc}_{\text{origin}}), \quad (6)$$

where $\text{acc}_{\text{origin}}$ is the top-1 classification accuracy of the full-precision model on the training set, $\text{acc}_{\text{quant}}$ is the accuracy of the quantized model after finetuning, and $\lambda$ is a scaling factor which is set to 0.1 in our experiments.
3.6. Agent

For the RL agent, we leverage the deep deterministic policy gradient (DDPG) [17], which is an off-policy actor-critic algorithm for continuous control problem. In our environment, one step means that our agent makes an action to decide the number of bits assigned to the weights or activations of a specific layer, while one episode is composed of multiple steps, where our RL agent makes actions to all layers. We apply a variant form of the Bellman’s Equation, where each transition in an episode is defined as $T_k = (O_k, a_k, R, O_{k+1})$. During exploration, the $Q$-function is computed as

$$
\hat{Q}_k = R_k - B + \gamma \times Q(O_{k+1}, w(O_{k+1}) | \theta^Q),
$$

and the loss function can be approximated by

$$
L = \frac{1}{N_e} \sum_{k=1}^{N_e} (\hat{Q}_k - Q(O_k, a_k | \theta^Q))^2,
$$

where $N_e$ denotes the number of steps in this episode, and the baseline $B$ is defined as an exponential moving average of all previous rewards in order to reduce the variance of the gradient estimation. The discount factor $\gamma$ is set to 1 since we assume that the action made for each layer should contribute equally to the final result. Moreover, as the number of steps is always finite (bounded by the number of layers), the sum of the rewards will not explode.

3.7. Implementation Details

In this section, we present the implementation details about RL exploration and finetuning quantized models.

**Agent.** The DDPG agent consists of an actor network and a critic network. Both using the same network architecture: they take the state vector and the action from the last time step as inputs and feed them into two separate fully-connected layers with hidden sizes of 400. After that, we add the two hidden vectors together and go through another two fully-connected layers with hidden sizes of $\{300, 1\}$. As for the actor network, we use an additional sigmoid function to project the output into the range of $[0, 1]$.

**Exploration.** Optimization of the DDPG agent is carried out using ADAM [15] with $\beta_1 = 0.9$ and $\beta_2 = 0.999$. We use a fixed learning rate of $10^{-4}$ for the actor network and $10^{-5}$ for the critic network. During exploration, we employ the following stochastic process of the noise:

$$
w'(O_k) \sim N_{\text{trunc}}(w(O_k | \theta^w), \sigma^2, 0, 1),$$

where $N_{\text{trunc}}(\mu, \sigma, a, b)$ is the truncated normal distribution, and $w$ is the model weights. The noise $\sigma$ is initialized as 0.5, and after each episode, the noise is decayed exponentially with a decay rate of 0.99.

**Finetuning.** During exploration, we finetune the quantized model for one epoch to help recover the performance (using SGD with a fixed learning rate of $10^{-3}$ and momentum of 0.9). We randomly select 100 categories from ImageNet [5] to accelerate the model finetuning during exploration. After exploration, we quantize the model with our best policy and finetune it on the full dataset.

4. Experiments

We conduct extensive experiments to demonstrate the consistent effectiveness of our framework for multiple objectives: latency, energy, and model size.

**Datasets and Models.** Our experiments are performed on the ImageNet [5] dataset. As our focus is on more efficient models, we extensively study the quantization of MobileNet-V1 [12] and MobileNet-V2 [24]. Both MobileNets are inspired from the depthwise separable convolutions [3] and replace the regular convolutions with the pointwise and depthwise convolutions: MobileNet-V1 stacks multiple “depthwise – pointwise” blocks repeatedly; while MobileNet-V2 uses the “pointwise – depthwise – pointwise” blocks as its basic building primitives.

### Table 2: The configurations of edge and cloud accelerators.

| Hardware | Batch | PE Array | AXI port | Block RAM |
|----------|-------|----------|----------|-----------|
| Edge Zynq-7020 | 1 | 8×8 | 4×64b | 140×36Kb |
| Cloud VU9P 16 | 16×16 | 4×256b | 2160×36Kb |

4.1. Latency-Constrained Quantization

We first evaluate our framework under latency constraints on two representative hardware architectures: spatial and temporal architectures for multi-precision CNN. We show that it’s beneficial to have specialized quantization policies for different hardware architectures. We systematically interpret the policy given by AI to guide future human designs.

**Temporal Architecture.** Bit-Serial Matrix Multiplication Overlay (BISMO) proposed by Yaman et al. [26] is a classic temporal design of neural network accelerator on FPGA. It introduces bit-serial multipliers which are fed with one-bit digits from 256 weights and corresponding activations in parallel at one time and accumulates their partial products by shifting over time.

**Spatial Architecture.** BitFusion architecture proposed by Hardik et al. [25] is a state-of-the-art spatial ASIC design for neural network accelerator. It employs a 2D systolic array of Fusion Units which spatially sum the shifted partial products of two-bit elements from weights and activations.
Table 3: Latency-constrained quantization on BISMO (edge accelerator and cloud accelerator) on ImageNet. Our framework can reduce the latency by $1.4 \times$ to $1.95 \times$ with negligible loss of accuracy compared with the fixed bitwidth (8 bits) quantization.

![Quantization policy under latency constraints for MobileNet-V1. On edge accelerator, our RL agent allocates less activation bits to the depthwise convolutions, which echos that the depthwise convolutions are memory bounded and the activations dominates the memory access. On cloud accelerator, our agent allocates more bits to the depthwise convolutions and allocates less bits to the pointwise convolutions, as cloud device has more memory bandwidth and high parallelism, the network appears to be computation bounded.]

**4.1.1 Quantization policy for BISMO Architecture**

Inferencing neural networks on edge devices and cloud sever can be quite different: batch size, memory bandwidth, peak FLOPs, etc. We use Xilinx Zynq-7020 FPGA [29] as our edge device and Xilinx VU9P [28] as our cloud device.

Table 2 shows our experiment configurations on these two platforms along with their available resources.

As for comparison, we adopt the PACT [2] as our baseline, which uses the same number of bits for all layers except for the first layer which extracts the low level features, they use 8 bits for both weights and activations as it has fewer parameters and is very sensitive to errors. We follow a similar setup for the first layer (8 bits), and explore the bitwidth allocation policy for all the other layers. Under the same latency, HAQ consistently achieved better accuracy than the baseline on both the cloud and the edge (Table 3). With similar accuracy, HAQ can reduce the latency by $1.4 \times$ to $1.95 \times$ compared with the baseline.

**Interpreting the quantization policy.** Our agent gave quite different quantization policy for edge and cloud accelerators (Figure 3). For the activations, the depthwise convolution layers are assigned less bitwidth than the pointwise layers on the edge; while on the cloud device, the bitwidth of these two types of layers are similar. For weights, the bitwidth of these types of layers are nearly the same on the edge; while on the cloud, the depthwise convolution layers got more bitwidth than the pointwise convolution layers.

We explain the difference of quantization policy between edge and cloud by the roofline model [27]. Many previous works use FLOPs or BitOPs as metrics to measure computation complexity. However, they are not able to directly reflect the latency, since there are many other factors influencing the hardware performance, such as memory access cost and degree of parallelism [24, 20]. Taking computation and memory access into account, the roofline model assumes that applications are either computation-bound or memory bandwidth-bound, if not fitting in on-chip caches, depending on their operation intensity. Operation intensity is measured as operations (MACs in neural networks) per byte accessed. A lower operation intensity indicates suffering more from the memory access.
Table 4: Latency-constrained quantization on BitFusion (MobileNet-V1 on ImageNet). Our framework can reduce the latency by 2x with almost no loss of accuracy compared with the fixed bitwidth (8 bits) quantization.

|        | Weights | Activations | Acc.-1 | Acc.-5 | Latency |
|--------|---------|-------------|--------|--------|---------|
| PACT [2] | 4 bits  | 4 bits      | 62.44  | 84.19  | 7.86 ms |
| Ours    | flexible| flexible    | 67.45  | 87.85  | 7.86 ms |
| PACT [2] | 6 bits  | 6 bits      | 70.46  | 89.59  | 19.99 ms|
| Ours    | flexible| flexible    | 70.90  | 89.95  | 19.98 ms|
| Original| 8 bits  | 8 bits      | 70.82  | 89.85  | 20.08 ms|

The bottom of Figure 3 shows the operation intensities (OPS per Byte) of convolution layers in the MobileNet-V1. Depthwise convolution is memory bounded, and the pointwise convolution is computation bounded. Our experiments show that when running MobileNet-V1 on the edge devices with small batch size, its latency is dominated by the depthwise convolution layers. Since the feature maps take a major proportion in the memory of depthwise convolution layers, our agent gives the activations less bits. In contrast, when running MobileNet-V1 on the cloud with large batch size, our agent increases the bitwidth of depthwise convolution to preserve the accuracy at low memory overhead since depthwise convolution only takes a small proportion of the total weights. A similar phenomenon can be observed in Figure 4 on MobileNet-V2. Moreover, as the activation size in deeper layers gets smaller, they get assigned more bits.

4.1.2 Quantization policy for BitFusion Architecture

In order to demonstrate the effectiveness of our framework on different hardware architectures, we further compare our framework with PACT [2] under the latency constraints on the BitFusion [25] architecture (Table 4). Our framework performs much better than the hand-craft policy with the same latency. It can achieve almost no degradation of accuracy with only half of the latency used by the original MobileNet-V1 model (from 20.08 to 11.09 ms). Therefore, our framework is flexible to provide specialized quantization policy for different hardware platforms.

4.2. Energy-Constrained Quantization

We then evaluate our framework under the energy constraints. Similar to the latency-constrained experiments, we compare our framework with PACT [2] that uses fixed number of bits without hardware feedback. From Table 5, we can clearly see that our framework outperforms the rule-based baseline: it achieves much better performance while consuming similar amount of energy. In particular, our framework is able to achieve almost no loss of accuracy with nearly half of the energy consumption of the original MobileNet-V1 model (from 31.03 to 16.57 mJ), which suggests that mixed preci-
Table 6: Model size-constrained quantization on ImageNet. Compared with Deep Compression [7], our framework achieves higher accuracy under similar model size (especially under high compression ratio).

|        | MobileNet-V1 | MobileNet-V2 | ResNet-50 |
|--------|--------------|--------------|-----------|
|        | Weights | Acc.-1 | Acc.-5 | Model Size | Acc.-1 | Acc.-5 | Model Size | Acc.-1 | Acc.-5 | Model Size |
| Han et al. [8] | 2 bits | 37.62 | 64.31 | 1.09 MB | 58.07 | 81.24 | 0.96 MB | 68.95 | 88.68 | 6.32 MB |
| Ours   | flexible | 57.14 | 81.87 | 1.09 MB | 66.75 | 87.32 | 0.95 MB | 70.63 | 89.93 | 6.30 MB |
| Han et al. [8] | 3 bits | 65.93 | 86.85 | 1.60 MB | 68.00 | 87.96 | 1.38 MB | 75.10 | 92.33 | 9.36 MB |
| Ours   | flexible | 67.66 | 88.21 | 1.58 MB | 70.90 | 89.76 | 1.38 MB | 75.30 | 92.45 | 9.22 MB |
| Han et al. [8] | 4 bits | 71.14 | 89.84 | 2.10 MB | 71.24 | 89.93 | 1.79 MB | 76.15 | 92.88 | 12.40 MB |
| Ours   | flexible | 71.74 | 90.36 | 2.07 MB | 71.47 | 90.23 | 1.79 MB | 76.14 | 92.89 | 12.14 MB |

|        | 32 bits | 70.90 | 89.90 | 16.14 MB | 71.87 | 90.32 | 13.37 MB | 76.15 | 92.86 | 97.49 MB |

Figure 5: Quantization policy under model size constraints for MobileNet-V2. Our RL agent allocates more bits to the depthwise convolutions, since depthwise convolutions have fewer number of parameters.

4.3. Model Size-Constrained Quantization

Finally, we evaluate our framework under the model size constraints. Following Han et al. [8], we employ the $k$-means algorithm to quantize the values into $k$ different centroids instead of using the linear quantization for compression, since $k$-means quantization can be more effective reducing the model size.

We compare our framework with Deep Compression [8] on MobileNets and ResNet-50. From Table 6, we can see that our framework performs much better than Deep Compression: it achieves higher accuracy with the same model size. For compact models like MobileNets, Deep Compression significantly degrades the performance especially under aggressive quantization, while our framework can preserve the accuracy much better. For instance, when Deep Compression quantizes the weights of MobileNet-V1 to 2 bits, the accuracy drops significantly from 70.90 to 37.62; while our framework can still achieve 57.14 of accuracy with the same model size. The reason is our framework makes full use of the mixed precision by systematically searching the optimal quantization policy.

Discussions. In Figure 5, we visualize the bitwidth allocation strategy for MobileNet-V2. From this figure, we can observe that our framework assigns more bitwidths to the weights in depthwise convolution layers than pointwise convolution layers. Intuitively, this is because the number of parameters in the former is much smaller than the latter. Comparing Figure 4 and Figure 5, the policies are drastically different under different optimization objectives (fewer bitwidths for depthwise convolutions under latency optimization, more bitwidths for depthwise convolutions under model size optimization). Our framework succeeds in learning to adjust its bitwidth policy under different constraints.

5. Conclusion

In this paper, we propose Hardware-Aware Automated Quantization (HAQ), an automated framework for quantization which does not require any domain experts and rule-based heuristics. We provide a learning based method that can search the quantization policy with hardware feedback. Compared with indirect proxy signals, our framework can offer a specialized quantization solution for different hardware platforms. Extensive experiments demonstrate that our framework performs better than conventional rule-based approaches for multiple objectives: latency, energy and model size. Our framework reveals that the optimal policies on different hardware architectures are drastically different, and we interpreted the implication of those policies. We believe the insights will inspire the future software and hardware co-design for efficient deployment of deep neural networks.
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