Room temperature photoluminescence (RTPL) spectroscopy and Raman spectroscopy were examined as in-line monitoring techniques for characterizing the interface characteristics of ultra-thin (∼7.2 nm) stacked dielectric films (Si/N/SiO2) on 300 mm Si wafers. To investigate the effect of the stacked dielectric films on electronic properties and lattice stress of Si beneath the films, RTPL and Raman signals were measured under various excitation wavelengths with different probing depths. Changes of interface characteristics (mainly, electronic properties and lattice stress of Si beneath the films) of the stacked dielectric films and the Si wafer were investigated using various specimens prepared by different deposition techniques and conditions. The overall interface characteristics of the Si/N/SiO2/Si specimens was found to be very dependent on the SiN deposition technique and process conditions. As the stoichiometry of SiN films change from N-rich to Si-rich conditions, the RTPL signal becomes weaker, indicating the change of electronic properties at the Si/N/SiO2 interface. Within-wafer and wafer-to-wafer variations of the Si/N/SiO2/Si interface characteristics were successfully characterized by RTPL and Raman spectroscopy under various excitation wavelengths.

Other characterization results such as film thickness from ellipsometry, film stress from wafer curvature and film composition from Auger electron spectroscopy (AES) were also discussed.

© The Author(s) 2015. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0291507jss] All rights reserved.

Manuscript submitted March 31, 2015; revised manuscript received May 8, 2015. Published May 16, 2015. This article is a version of Paper 1392 from the Chicago, Illinois, Meeting of the Society, May 24–28, 2015.

Advanced metal-oxide-semiconductor (MOS) and metal-insulator-semiconductor (MIS) devices employ ultra-thin dielectric film(s) as gate dielectrics. The physical dimensions are typically on the order of several nanometers. Pure SiO2 or combinations of SiN and SiO2 films are typically used. Both physical thickness and effective oxide thickness (EOT) are less than 10 nm.1-2 High dielectric constant materials (high-k dielectrics) and metal gates are also frequently used. Low dielectric constant materials (low-k dielectrics) are used as inter-metal dielectrics (IMD) and inter-layer dielectrics (ILD) with Cu interconnects to reduce RC constants (i.e., RC delay) and improve device operation speed.3 As devices scale to smaller size, the complexity of device structures as well as the number of interfaces in dielectric films increases. Proper understanding, monitoring and control of the dielectric/Si interface becomes very important.

Physical dimensions of ultra-thin dielectric film(s) on Si wafers are typically measured using ellipsometry and occasionally verified by high resolution cross-section transmission electron microscopy (HRXTEM). Conventional interface characterization techniques include chemical characterization and electrical characterization. Chemical properties are typically evaluated using Auger electron spectroscopy (AES), secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS).4-6 Films stress is often monitored in blanket Si wafers by measuring the curvature, and its direction, before and after film deposition and treatment.7-10 The stoichiometry, chemical composition and chemical bonding characteristics are examined routinely. For electrical characterization of dielectric films, non-contact I-V, C-V and carrier lifetime measurements are performed for in-line monitoring. However, the electrical characterization often modifies the properties of ultra-thin dielectric films being measured due to the intense electric field applied to the specimen during measurements.11-13 As an alternative interface quality characterization technique, RTPL has been proposed and promising in-line monitoring results on ultra-thin SiO2 layers on Si wafers have been reported.11-15 Multiwavelength Raman spectroscopy has been widely used in lattice stress characterization of various types (blanket, patterned) of Si wafers.16-18 It is important to directly measure Si lattice stress instead of estimating film stress from the curvature of blanket Si wafers before and after film deposition. The same film(s) can have a significantly different impact on Si depending on the presence, sizes, shapes, layouts and material combinations of patterns on Si wafers.

In this study, we have investigated the effect of SiN film deposition techniques on the interface quality of the resulting SiN/SiO2/Si using RTPL and Raman measurements under multi-wavelength excitation. The silicon nitride growth technique, and condition dependence of the RTPL and Raman spectra, was investigated and examined as a potential non-contact dielectric/Si interface characterization technique with high spatial resolution and the virtual depth profiling capability. The RTPL and Raman characterization results were discussed and contrasted with other conventional characterization results.

Experimental

Ultrathin (target thickness of ∼7.2 nm) stacked gate dielectric (Si/N/SiO2) films were prepared on prime 300 mm p–Si (100) wafers by a number of different SiN deposition techniques. The sample preparation procedures were as follows. First, ultrathin (∼2.2 nm thick) gate oxide quality, thermal oxide films were grown on 300 mm Si(100) wafers at 750°C under oxygen radicals in a commercial vertical batch furnace. The surface condition of the wafers was hydrophilic before initial SiN/SiO2 film growth. Nominal 5.0 nm thick SiN films were grown on 2.2 nm thick SiO2 films on Si wafers using commercial batch furnaces, a conventional single-wafer low pressure chemical vapor deposition (LPCVD) system, and an atomic layer deposition (ALD) system under various nitrogen and silicon source flow conditions at either 620°C or 710°C. The silicon nitride film deposition technique, source reagents, gas flow ratio (Si source/N source) and deposition rate were varied to investigate the effect of SiN deposition conditions on the SiN/SiO2/Si interface quality. Thicknesses of SiO2 and SiN films were measured after depositing each film using ellipsometry.

The main purpose of this experiment is to see the effect of stoichiometry of SiN film and SiN film deposition techniques on RTPL measurements. The sensitivity of RTPL techniques on the stoichiometry and interface quality of SiN/SiO2/Si wafers and potential in-line monitoring applications is analyzed. The film thickness was measured after SiO2 film deposition and before and after SiN deposition using ellipsometry. 
The RTPL intensity and spectra from the SiN/SiO2/Si wafers and a reference wafer (SiO2/Si wafer before SiN film deposition) were measured to investigate the effect of SiN deposition techniques and conditions on the SiN/SiO2/Si interface quality as investigated in the wavelength range of 900 ~ 1400 nm under 650 and 827 nm focused laser beam excitation. The spot size of the excitation laser beam was in the range of 50 ~ 100 μm in diameter. The laser power at the wafer surface was 20 ~ 50 mW. The RTPL signal was integrated using a specially designed spectrophotograph for 10 ~ 500 ms per measurement point.11–15

Potential applications of the RTPL characterization techniques for in-line monitoring and screening of the interface quality of ultra-thin (~7.0 nm) SiO2 films on Si wafers have been demonstrated previously.12–15 Details of design concepts and application examples of the multi-wavelength, spectroscopic RTPL system used in this study can be found in previous publications.11–15 In this work, the study has been extended to the ultra-thin (~7.0 nm) stacked (SiN/SiO2) dielectric films on Si wafers.

The SiN/SiO2/Si wafers were also characterized by high spectral resolution Raman spectroscopy under various excitation wavelengths using three different visible excitation wavelengths (457.9, 488.0 and 514.5 nm) of an Ar+ laser. A WaferMasters’ MRS-300 system (WaferMasters, Inc., San Jose, CA 95112) was used. The details of the system, and its various semiconductor material characterization applications, can be found elsewhere.20–22 Raman measurements were done in a 180° backscattering geometry under an optical microscope. The spot size of the excitation laser beam was in the range of ~0.5 μm in diameter. The laser power at the wafer surface was typically between 5 mW and 20 mW, which does not cause a Raman peak shift due to Si wafer heating from the excitation laser beam. Exposure time was varied from 5s to 20s per measurement site, depending on the Raman signal intensity under the specific excitation wavelengths. Ninety-three (93)-point wafer mapping was done under the three excitation wavelengths.

The stoichiometry (Si:N content ratio) of SiN films was measured using Auger electron spectroscopy (AES). The peak-to-peak (p-p) heights of the SiKLL and NKL Auger transition in the first derivative (dN(E)/dE) of the energy distribution were used to determine the atomic ratio of the Si/N content in SiN films.

Bow heights along the scan paths were measured using a laser beam scanning system to estimate elastic film stress after SiN film deposition. A laser beam is directed to the wafer to measure the radius of curvature and bow of wafers. The beam is reflected at an angle that corresponds to the radius of curvature of the wafer. The bow heights along scan paths were measured and global film stress was calculated using Stoney’s equation.7

Results and Discussion

SiN/SiO2 film growth.— Seven ultra-thin stacked SiN/SiO2 films on Si wafers were prepared by various SiN deposition techniques and conditions. All wafers have 2.2 nm thick, thermally grown oxide under oxygen radicals in a commercial vertical batch furnace prior to the SiN deposition. Table I summarizes SiN deposition technique, deposition temperature, targeted stoichiometry and average SiN film thickness measured by ellipsometry under He-Ne laser (633 nm) irradiation. The thickness of the ultra-thin SiN films was in the range of 4.6 ~ 5.7 nm.

Room temperature photoluminescence (RTPL).— Previous RTPL studies of interface quality of various (as deposited, plasma exposed, UV irradiated and/or heat treated) SiO2/Si showed very high sensitivity to the quality of the passivation characteristics and/or integrity of SiO2 films. The RTPL characterization technique can be used for in-line monitoring and screening of the dielectric/Si interface quality, including plasma induced damage (PID) and UV radiation damage. RTPL spectra from the center of all SiN/SiO2/Si wafers (A ~ G) were measured to gain insights into the electronic carrier behavioral properties as an SiN/SiO2/Si interface quality factor. Three excitation wavelengths of 532, 650 and 827 nm were used for RTPL measurements. Estimated RTPL probing depths for Si, under 532, 650 and 827 nm, are ~1.5, ~4.0 and ~10.0 μm, respectively (Fig. 1).11–15

The RTPL probing depth δPL is defined as 1/α, where α is the absorption coefficient at the RTPL excitation wavelength. As the excitation wavelength is near the bandgap (Eg of Si (1.12 eV or ~1100 nm), the absorption coefficient become very smaller and the probing depth becomes very deeper.

Significantly large RTPL intensity variations were measured among the seven SiN/SiO2/Si wafers, depending on the SiN deposition technique and conditions. Fig. 2 shows the RTPL spectra of the seven SiN/SiO2/Si wafers measured under (a) 650 nm and (b) 827 nm excitation. The measurement time was fixed at 1 s under 532 nm and 650 nm excitation for all wafers. The measurement times of 500 ms and 10 ms were used for 827 nm excitation depending on RTPL intensity. All RTPL spectra were normalized to the 1 s measurement time for easy comparisons. Intensity variations of almost two orders of magnitude for RTPL were measured among wafers with very similar physical dimensions (~5.0 nm thick SiN and a 2.2 nm thick thermally grown SiO2 film stack). RTPL intensity and spectra, under all three excitation wavelengths, were very similar. The 532 nm excitation RTPL measurements, with shorter probing depth of ~1.5 μm (the weakest RTPL signal among others), were omitted in this paper. The RTPL spectra and the maximum RTPL counts at ~1.140 nm, under 650 nm and 827 nm excitations, were plotted in Fig. 3 to make RTPL peak intensity comparisons easier. It shows (a) RTPL spectra under 650 nm

---

Table I. Summary of SiN film deposition techniques, conditions and final SiN film thickness. All wafers have a 2.2 nm thick thermally grown SiO2 layer at 750°C under oxygen radicals before receiving SiN deposition.

| Wafer ID | SiN Film Deposition Techniques | Deposition Temperature | SiN Film Thickness | NH3 Flow | Targeted Stoichiometry |
|----------|--------------------------------|------------------------|-------------------|----------|------------------------|
| A        | Furnace Thermal CVD            | 710°C                  | 4.7 nm            | Low      | N-rich                 |
| B        | Furnace Thermal CVD            | 710°C                  | 4.6 nm            | Moderate | N-poor                 |
| C        | Furnace ALD                    | 620°C                  | 5.6 nm            | Moderate | N-rich                 |
| D        | Furnace Thermal CVD            | 710°C                  | 5.0 nm            | High     | N-rich                 |
| E        | Single-Wafer CVD               | 710°C                  | 5.0 nm            | Moderate | N-rich                 |
| F        | Furnace ALD                    | 620°C                  | 5.7 nm            | High     | N-rich                 |
| G        | Furnace ALD                    | 620°C                  | 5.3 nm            | High     | N-poor                 |
G. Wafers A and D were grown under N-rich gas flow conditions in a thermal CVD furnace. Wafers B and G were grown under N-poor gas flow conditions in a thermal CVD furnace and a thermal ALD furnace, respectively. Wafer E, with a SiN layer deposited in a single-wafer CVD reactor, showed a moderate RTPL intensity. The very strong RTPL spectra from wafers C and F showed a typical RTPL spectra from a lightly doped Si wafer with high quality surface passivation thermal SiO₂ layers. Wafers C and F were intended for N-rich SiN film growth in a thermal ALD furnace under very low Si/N (or high N/Si) source gas ratios. The RTPL spectra from the SiC are composed of an asymmetric band-to-band transition RTPL peak centered at ∼1140 nm and a small band tail RTPL peak, extended to ∼1270 nm.

The RTPL signal was from the Si wafer, neither from SiN nor from SiO₂. Since all seven wafers have an identical, thermally grown SiN/SiO₂/Si wafer is similar. In the case of the SiN/SiO₂/Si wafers, the possible cause of the difference when the RTPL intensity from the SiC wafer in the identical commercial batch furnace, the RTPL intensity variations are the influence or signature of the successive SiN layer deposition process. The subsequent SiN film deposition conditions have modified the underlying SiO₂/Si interface characteristics.

When effective non-radiative surface recombination is higher for SiN/SiO₂/Si, with poor passivation characteristics, minority carrier lifetime near the surface is shorter. As a result, RTPL intensity is weaker. When the effective non-radiative surface recombination is very low, as in SiN/SiO₂/Si with excellent passivation characteristics, the minority carrier lifetime near the surface becomes longer. Consequently, the RTPL intensity is higher.

RTPL spectra from Si generally can be deconvoluted into an asymmetric band-to-band transition peak centered at ~1140 nm and a small band tail peak extended to ~1270 nm. Detailed analysis, including deconvolution of RTPL spectra, is necessary to identify the possible cause of the difference when the RTPL intensity from SiN/SiO₂/Si wafers are similar. In the case of the SiN/SiO₂/Si wafers, with large wafer-to-wafer RTPL intensity variations, simple comparisons of RTPL intensity can provide useful clues for the probable cause of wafer-to-wafer variations. The strong RTPL peak intensity variations among wafers implies that the SiN/SiO₂/Si interface state, or quality, plays a very significant role in electronic carrier transport properties. Minority carrier lifetime and the ratio between

![Figure 2](image1.png)

Figure 2. (a) 650 nm and (b) 827 nm excited RTPL spectra measured from the center of various SiN/SiO₂/Si wafers.

excitation, (b) RTPL spectra under 827 nm excitation, (c) linear scale and (d) log scale for RTPL peak intensity under both 650 and 827 nm excitations.

Almost no RTPL signal was measured from wafers A, B, D and G. Wafers A and D were grown under N-rich gas flow conditions in a thermal CVD furnace. Wafers B and G were grown under N-poor gas flow conditions in a thermal CVD furnace and a thermal ALD furnace, respectively. Wafer E, with a SiN layer deposited in a single-wafer CVD reactor, showed a moderate RTPL intensity. The very strong RTPL spectra from wafers C and F showed a typical RTPL spectra from a lightly doped Si wafer with high quality surface passivation thermal SiO₂ layers. Wafers C and F were intended for N-rich SiN film growth in a thermal ALD furnace under very low Si/N (or high N/Si) source gas ratios. The RTPL spectra from the SiC are composed of an asymmetric band-to-band transition RTPL peak centered at ∼1140 nm and a small band tail RTPL peak, extended to ∼1270 nm.

The RTPL signal was from the Si wafer, neither from SiN nor from SiO₂. Since all seven wafers have an identical, thermally grown SiN/SiO₂/Si wafer is similar. In the case of the SiN/SiO₂/Si wafers, the possible cause of the difference when the RTPL intensity from the SiC wafer in the identical commercial batch furnace, the RTPL intensity variations are the influence or signature of the successive SiN layer deposition process. The subsequent SiN film deposition conditions have modified the underlying SiO₂/Si interface characteristics.

When effective non-radiative surface recombination is higher for SiN/SiO₂/Si, with poor passivation characteristics, minority carrier lifetime near the surface is shorter. As a result, RTPL intensity is weaker. When the effective non-radiative surface recombination is very low, as in SiN/SiO₂/Si with excellent passivation characteristics, the minority carrier lifetime near the surface becomes longer. Consequently, the RTPL intensity is higher.

RTPL spectra from Si generally can be deconvoluted into an asymmetric band-to-band transition peak centered at ~1140 nm and a small band tail peak extended to ~1270 nm. Detailed analysis, including deconvolution of RTPL spectra, is necessary to identify the possible cause of the difference when the RTPL intensity from SiN/SiO₂/Si wafers are similar. In the case of the SiN/SiO₂/Si wafers, with large wafer-to-wafer RTPL intensity variations, simple comparisons of RTPL intensity can provide useful clues for the probable cause of wafer-to-wafer variations. The strong RTPL peak intensity variations among wafers implies that the SiN/SiO₂/Si interface state, or quality, plays a very significant role in electronic carrier transport properties. Minority carrier lifetime and the ratio between

![Figure 3](image2.png)

Figure 3. (a) 650 nm and (b) 827 nm excited RTPL spectra measured from the center of various SiN/SiO₂/Si wafers. (c) Linear scale and (d) log scale plots of RTPL peak intensity measured from various SiN/SiO₂/Si wafers measured under 650 and 827 nm excitation.
radiative and non-radiative recombination of carriers at the SiO$_2$/Si interface have very strong SiN film growth technique and condition dependence.

Raman spectroscopy.— Raman spectroscopy in semiconductor materials measures inelastic light scattering with phonons and estimates lattice stress/strain-related material properties, including crystallinity of solids. For semiconductor materials opaque to the excitation wavelength, a 180° backscattering geometry is typically used. Stress-free Si (100) single crystal gives only one sharp symmetrical Raman peak corresponding to the longitudinal optical (LO) phonon at $\sim 520.3$ cm$^{-1}$. The probing depth of Raman spectroscopy depends on the absorption coefficient ($\alpha$) of Si at a specific excitation wavelength (Fig. 1). Unlike RTPL, the probing depth of Raman measurement is defined as $1/2\alpha$ because the wavelength of the Raman signal is almost identical to the excitation wavelength and attenuates at the same rate as the excitation light when it is emitted from a depth in a solid. The Raman signal contains the weighted average of Si lattice conditions at the excitation wavelengths, within the probing depth. The probing depth in Si, under visible (VIS) excitation wavelengths in the range of 400 $\sim$ 700 nm, is between 50 nm and 3 $\mu$m. By selecting appropriate combinations of excitation wavelengths, insight into the change (in the depth direction) in lattice stress/strain-related material properties can be gained. Thus, the effect of oxidation and subsequent nitride deposition techniques and conditions on Si lattice properties underneath the thin oxide layer can be investigated along process steps using Raman spectroscopy under different excitation wavelengths.

To investigate the effect of SiN deposition techniques and conditions on significant (up to two orders of magnitude) RTPL intensity variations, 93-point Raman wafer mapping was done using a high resolution, multiwavelength Raman spectroscopy (MRS-300, WaferMasters, Inc., San Jose, CA 95112) system under 457.9, 488.0 and 514.5 nm excitation. Probing depths of the three Raman excitation wavelengths in Si (100) wafers, with ultra thin SiN/SiO$_2$ films, are illustrated with RTPL probing depths in Fig. 1. 1

The Raman spectra were measured at 93 points on all seven SiN/SiO$_2$/Si wafers (A $\sim$ G). All Raman spectra were fitted to Lorentzian curves using least square approximation to extract Raman shift, full-width-at-half-maximum (FWHM) and intensity values for quantitative comparisons between wafers. The average Raman shift, FWHM and intensity values of 93-point wafer mapping measurements, under the three excitation wavelengths, were plotted in Fig. 4. The maximum and minimum Raman shift, FWHM and intensity values of 93-point wafer mapping measurements were also plotted to show the Raman measurement reliability and homogeneity of the lattice stress/strain-related material properties within wafers.

Raman shifts obtained from the Lorentzian curve fitting of measured spectra, measured under 457.9 nm excitation, were almost identical, within the Raman shift (wavenumber) resolution and repeatability. According to WaferMasters, the resolution and repeatability of MRS-300 are 0.01 cm$^{-1}$ (after curve fitting) and 0.05 cm$^{-1}$, respectively. However, the Raman stress shifts measured from 488.0 and 514.5 nm showed more noticeable variations between wafers. As the excitation wavelength was increased (or as the probing depth is getting deeper), the variations became larger. Wafers D, F and G showed slightly higher Raman stress values compared to the other wafers. This implies that the average lattice stress of Si, within probing depths, of the shortest excitation wavelength (457.9 nm) were almost identical just below the SiN/SiO$_2$/Si interface. All wafers showed Raman shifts larger than the Raman shift (520.3 cm$^{-1}$) of stress-free Si, regardless of excitation wavelengths. Raman peak shift in a positive direction by 0.1 cm$^{-1}$ is equivalent to $-43.5$ MPa of compressive lattice stress in Si. All wafers showed compressive stress between $-35$ MPa and $-80$ MPa, depending on probing depth of Raman measurements.

FWHM values showed similar trends to the Raman shift values. Under the 457.9 nm excitation, the differences between wafers were small. As the excitation wavelength is increased (the probing depth is getting deeper), FWHM values of wafers D, F and G were significantly larger than the rest of wafers.

The intensity seemed to show the opposite behavior. The wafers D, F and G showed lower intensity than the rest of the wafers. Considering the definition of intensity, which is the peak height of Lorentzian fitted Raman peak, wider FWHM values with the same areal intensity implies lower peak intensity. Thus, the opposite trend between FWHM and Raman peak intensity is not surprising.

Although the RTPL and Raman measurements each used three different wafers from the view points of electronic properties and lattice properties, the intensity and FWHM values seem to show consistent trends between the wafers.

**Figure 4.** Multiwavelength Raman wafer mapping (93-point) measurement summary of various SiN/SiO$_2$/Si wafers.
stress, they do not match. RTPL measurements showed wafers C, E, and F are significantly different from the rest. Raman measurements showed wafers D, F, and G are different. Only the wafer F is common to both RTPL and Raman measurements. The correlation between RTPL and Raman measurements are not clear to this point. Further characterizations from different aspects are necessary for additional clues.

Auger electron spectroscopy.—To determine the stoichiometry (Si/N content ratio) of SiN films, AES analysis was done for all SiN films. The peak-to-peak (p-p) heights of the SiKLL and NKL Auger transition in the first derivative (dN(E)/dE) of the energy distribution were used for determining the atomic ratio of Si content in SiN films.

The stoichiometry of all SiN films showed the N content was in the range of 55.8 ~ 60.1%. Table II summarizes the deposition techniques, deposition conditions, relative NH3 flow to the SiH4 flow, target N content, measured N content and SiN film stress of all wafers. The SiN film stress measurement details are described in the following subsection. The SiN films deposited by thermal CVD or single-wafer CVD at higher temperature (710 °C) tends to show higher N content, from 59.6 ~ 60.1%. All other wafers with SiN deposited by furnace ALD at low temperature (620 °C) showed lower N content, between 55.8 and 56.9%.

It has been argued that the high energy Si KLL Auger peak is a better probe than the stronger and easily obtainable SiKLL Auger peak, since the line shape of SiKLL Auger peak is less influenced by the surface chemistry.23 Traditionally, many authors have used the Auger p-p ratio of SiKLL/NKL as an indicator of SiN composition.23–26 The detailed quantitative Auger depth profiling study of LPCVD and PECVD SiN films concluded that the p-p heights of the SiKLL and NKL Auger transition in dN(E)/dE of the energy distribution is a reasonable indicator to determine SiN composition in Auger depth profiles over a wide range of atomic Si/N ratio.23 It is generally agreed that the AES generally has excellent spatial resolution (15 nm), reasonable detection limit (<0.5 at%), good quantification with standards, and excellent speed. However, there are opinions that the main limitation of AES is its diminished ability to analyze insulators, in particular SiN.26

The N content difference of 3.8 ~ 4.3% between high temperature deposited SiN and low temperature deposited SiN is much larger than the sensitivity of AES even though there is an argument on the validity of AES for SiN film. Unfortunately, all SiN films deposited at lower temperature were done by furnace ALD. Thus, it is not definitely conclusive whether the N content differences are due to the difference in deposition temperature effect or deposition technique.

Film stress characterization.—For characterizing stress in SiN films, change of bow heights along the scan paths was measured using a laser beam scanning system to estimate elastic film stress, before and after SiN film deposition. A laser beam was directed to the wafer to measure the radius of curvature and bow heights of wafers. The laser beam reflects at an angle that corresponds to the radius of curvature of the wafer and the reflected beam is traced during scanning. The bow heights along scan paths were measured and averaged to calculated global film stress.7–10,27

When the thickness of the film h, is small compared to that of the substrate h0, the simple average film stress σf, calculation formula, which was first published by Stoney in 1909,2 is:

$$\sigma_f \approx \frac{E_s h_f^2}{6h_{f}^3/R}$$  

where R and Es are radius of curvature and Young’s modulus of the substrate, respectively. It assumes uniaxial stress and generates significant errors in calculating film stress on plate-like substrates. For plate-like substrates, a cap or bowl-like deformation of circular substrate, under the presence of intrinsic stress, is observed. When measuring film deposited on plate-like substrates, the corresponding biaxial deformation has to be taken into account by using the biaxial modulus. The Eq. 1 can be modified for plate-like substrates as follows.8,9

$$\sigma_{rr} \approx \frac{E_s h_f^2}{6(L-\nu_f h_f/R)}$$  

where νf is Poisson ratio of the substrate. Equation 2 is usually referred to as the Stoney formula. It has been extensively used in film stress calculations from wafer curvature changes.8–10,27 The Eq. 2 was used to calculate the SiN film stress to reduce film stress conversion errors.

SiN film stress values were summarized in Table II with other information on the films. All low temperature deposited SiN films (or all furnace ALD SiN films) showed a very small compressive (nearly stress free) film stress while the high temperature deposited SiN films show significantly high compressive stress (~586 MPa ~ 1385 MPa). The difference in SiN film stress between high temperature and low temperature deposited films may also be due to the difference between deposition techniques (thermal CVD vs. ALD) and/or N content (low N content vs. high N content) in the film.

SiN film stress measured from the bow height and curvature of Si wafer does not necessarily agree with Si stress as measured from Raman spectroscopy. Since the SiN films are deposited on ultra-thin (~2.2 nm-thick) SiO2/Si, very strong negative (or inverse) correlation between SiN film stress and Si lattice stress was expected. However, Raman characterization results indicate that the Si lattice stress has very little (or almost no) correlation with measured SiN film stress and is not uniform in the depth direction. The lattice stress of Si is very important and cannot be ignored because the device is made on Si and the properties of Si are largely responsible for the electrical behaviors of final devices. Si lattice stress must be directly measured instead of assuming unproven strong negative (or inverse) correlation with wafer bow height and curvature measurement results on blanket SiN/SiO2/Si. It should be directly and independently characterized whenever possible to avoid speculative assumption errors. Si lattice stress on blanket wafers and device wafers is also very different due to differences in structures, including material combinations, pattern shapes and sizes.

Discussion

Various properties of SiN/SiO2/Si wafers prepared under different SiN film deposition techniques and conditions were characterized.
Table III. Summary of SiN film deposition techniques, conditions and various characteristics of SiN/SiO2/Si wafers. All wafers have a 2.2 nm thick thermally grown SiO2 layer (at 750°C) under oxygen radicals before receiving SiN deposition.

| Wafer ID | SiN Film Deposition Techniques | Dep. Temp. | SiN Thick. | AES N Cont. | SiN Stress | RTPL Intensity | Raman Si Stress | Leakage Current |
|----------|-------------------------------|------------|------------|-------------|------------|----------------|----------------|----------------|
| A        | Furnace Thermal CVD           | High       | Thin       | High        | High       | Low            | Low            | Low            |
| B        | Furnace Thermal CVD           | High       | Thin       | High        | High       | Low            | Low            | Lower          |
| C        | Furnace ALD                   | Low        | Thick      | Low         | High       | Low            | Low            | -              |
| D        | Furnace Thermal CVD           | High       | Medium     | High        | Low        | Low            | High           | Lowest         |
| E        | Single-Wafer CVD              | High       | Medium     | High        | High       | High           | Low            | Medium         |
| F        | Furnace ALD                   | Low        | Thick      | Low         | High       | Low            | High           | -              |
| G        | Furnace ALD                   | Low        | Thick      | Low         | Low        | Low            | Low            | High           |

There is no single characterization technique which can provide definitive correlation with the electrical characteristics of SiN/SiO2 films integrated into the final devices. However, the combinations of various SiN/SiO2 film characterization techniques may provide useful clues for the final outcome without going through lengthy process integration and test cycles, after we identify the effective combinations of characterization techniques. This could dramatically improve overall effectiveness and shorten the process development, process integration and test cycle time.

According to the characterization summary in Table III, an individual characterization technique shows a different aspect of SiN/SiO2 properties and cannot provide conclusive information by itself. A combination of conventional characterization techniques such as ellipsometry, AES and film stress measurements is not sufficient to predict the outcome of electrical test results. By adding RTPL and Raman characterization techniques, the overall effectiveness of SiN/SiO2 in-line interface quality and Si lattice stress monitoring, for screening purposes, increases significantly.

As reported previously, an SiO2/Si interface with lower interface state density, interface trap density and good passivation characteristics yields relatively stronger RTPL intensity. The photogenerated minority carriers seek (either radiative or non-radiative) recombination partners in the diffusion path. In general, thermally grown SiO2/Si, used as gate dielectrics, with high passivation quality, typically yield very strong RTPL signals. Shorter excitation wavelength RTPL measurements are more sensitive to SiO2/Si interface quality, since the majority of electron-hole pairs are generated within the shallower probing depth.

The strong RTPL peak intensity variations from SiN/SiO2/Si wafers prepared by different SiN deposition techniques and conditions strongly suggest that the SiN/SiO2/Si interface quality plays a very important role in electronic carrier transport properties. All wafers with SiN films (wafers A, B and D) from a thermal CVD furnace showed very weak RTPL intensity, regardless of targeted stoichiometry. Waver A, with an N-poor targeted thermal ALD SiN film, also showed a very weak RTPL signal. The other wafers with moderately N-rich targeted (Waver E) SiN films, grown in a single-wafer CVD system, and N-rich (Wafers C and F) SiN films grown in a thermal ALD furnace showed strong RTPL signals. It seems that the RTPL intensity is primarily dependent on the SiN deposition technique and the stoichiometry of SiN films. As the thermal ALD grown SiN film increases its targeted N-content (not necessarily N content measured from AES), the RTPL intensity tends to increase significantly. This strongly suggests that the top SiN film quality strongly influences, and even permanently modifies, the band structure of Si near the interface of the SiO2/Si, below the SiN layer. The RTPL intensity is very sensitive to the resulting electronic state of SiN/SiO2/Si from the SiN deposition technique and targeted stoichiometry of SiN. It also should be noted that the targeted N content may not agree with the N content measured by AES, depending on deposition techniques and flow rates of source gases (SiH4 + NH3) and their ratio. Thus the RTPL intensity and spectra measurements can be used as an alternative film quality monitoring technique. While the conventional characterization techniques such as XPS, SIMS and I-V/C-V characteristics are very useful, they require lengthy turn-around times. They often require special sample preparation and can cause wafer breakage. Moreover, the I-V and C-V measurements are invasive to ultra-thin dielectric films and lack spatial resolution.

For advanced memory devices, ultra-thin SiN/SiO2 stacked dielectric layers are used to control and maintain refresh characteristics (or data leakage characteristics) by optimizing stoichiometry of the SiN layer. A high N-content in SiN (N-rich SiN) deposited by furnace thermal CVD generally results in better refresh characteristics (lower data leakage) of memory devices. For quality assurance, monitor wafers are run periodically to monitor its stoichiometry using the conventional characterization techniques, off-line. If effective in-line monitoring techniques are available, it would significantly improve device development turn around time and quality control practices in device manufacturing. From this standpoint, the non-contact and non-invasive characteristics of the RTPL measurement technique are particularly useful in the characterization, optimization and monitoring of SiN stoichiometry and SiN/SiO2/Si interface quality, as related to electronic band structure near the dielectrics/Si interface, as well as electronic carrier behaviors, including device performance.

Raman measurement results were quite sensitive to Si lattice stress and crystallinity changes due to the differences in SiN film deposition temperature and deposition technique. Wafers D, F and G showed slightly higher Raman shift values (under 488.0 and 514.5 nm excitation) compared to the other wafers indicating the average lattice stress of Si, within probing depths, of the shortest excitation wavelength (457.9 nm) were almost identical just below the SiN/SiO2/Si interface. All wafers showed slightly higher Raman shift values under 488.0 nm and 514.5 nm excitation indicating compressive stress between −35 MPa and −80 MPa, depending on probing depth of Raman measurements. High N content, furnace thermal CVD SiN films, with highly compressive film stress, resulted in low RTPL intensity, high Si lattice stress and low leakage current (or better refresh characteristics) in DRAM devices. The unique combination of high deposition temperature, furnace thermal CVD, high N content, high SiN film stress showed low RTPL intensity, high Si lattice stress and low leakage current. These powerful techniques, RTPL and Raman spectroscopy, can provide advanced indications of the performance of final devices.

RTPL and Raman measurement results do not necessarily match each other because they reflect different properties of the SiN/SiO2/Si wafers. They indicate electronic properties and lattice stress, respectively. Performance of electronic devices is strongly related to the important material properties, including minority carrier lifetime and mobility. When foreign materials are involved, the interface quality and properties are also very important factors of interest. Heretofore, there were no direct and convenient in-line material characterization and monitoring techniques for process and material screening purposes. Previous studies show that multilength
spectroscopic RTPL is a very powerful non-contact and non-invasive optical characterization technique for analyzing electronic carrier transport properties. Many apparent or hidden factors (such as metal contamination, fixed/mobile charges, interface states, defects, mid-gap states, dangling bonds, band bending, dopant concentration etc.) which can influence electronic carrier transport properties can be traced by carefully analyzing multiwavelength RTPL spectra with other material characterization results. From a process and material screening point of view, RTPL and multiwavelength Raman spectroscopy can be very valuable in-line material characterization techniques for identifying hidden property and material variations.

Summary

Multiwavelength RTPL spectroscopy and Raman spectroscopy were used for characterizing dielectric/Si interface quality and Si lattice stress beneath the SiN/SiO2 films. Ultra-thin (~7.2 nm) stacked dielectric films (SiN/SiO2) on 300 mm Si wafers were prepared using various SiN deposition techniques and conditions. A strong dependence of the overall SiN/SiO2/Si interface quality on the SiN film deposition technique, process conditions and stoichiometry of resulting SiN films was verified by RTPL spectroscopy. Very strong SiN deposition technique dependence of RTPL intensity from SiN/SiO2/Si wafers was observed. Strong SiN deposition temperature dependence of Si lattice stress beneath the SiN/SiO2 film was also found by using multiwavelength Raman spectroscopy. Within-wafer and wafer-to-wafer variations of the SiN/SiO2/Si interface characteristics were successfully characterized by RTPL and Raman spectroscopy under various excitation wavelengths.

All wafers with thermal CVD SiN films showed weak RTPL signals, regardless of targeted stoichiometry. Targeted N-rich, thermal ALD SiN films, with better refresh characteristics, resulted in strong RTPL signals. As the stoichiometry of thermal ALD SiN films changes from N-rich to N-poor targeted conditions, the RTPL signal becomes weaker, indicating the change of electronic properties at the SiN/SiO2/Si interface. Within wafer and wafer-to-wafer variations of the SiN/SiO2/Si interface quality and targeted stoichiometry of various SiN films were successfully characterized by RTPL spectroscopy under various excitation wavelengths. Multi-wavelength RTPL and Raman spectroscopy can be used as effective in-line monitoring and screening techniques for interface quality and Si lattice stress variations in SiN films on SiN/SiO2/Si wafers and to observe or screen potential process-originated carrier transport property variations in Si. Other characterization results such as film thickness from ellipsometry, film stress from wafer curvature and film composition from Auger electron spectroscopy (AES) were also discussed along with RTPL and Raman characterization results. The multiwavelength RTPL and Raman spectroscopy are very complimentary dielectric/Si interface and Si lattice monitoring techniques which can be used for in-line monitoring and to enhance other conventional characterization techniques.

References

1. S. Luryi, J. Xu, and A. Zaslavsky, in Future Trends in Microelectronics: The Nano, the Giga and the Ultra, Part 1, Wiley Interscience, New Jersey (2004).
2. K. Fröhlich, B. Hudec, K. Hušeková, J. Jirásk, A. Tarre, A. Kasikov, R. Rammula, and A. Vincze, ECS Trans., 41(2), 73 (2011).
3. M. T. Bohr, JEDM ’95 Technical Digest, 241 (1995).
4. D. K. Schroder, in Semiconductor Material And Device Characterization, 3rd Ed., Chapters 6, 7, 9 and 10, Wiley Interscience, New Jersey (2006).
5. E. H. Nicollian and J. R. Brews, in MOS (Metal Oxide Semiconductor) Physics and Technology, Chapters 8, 10 and 11, John Wiley & Sons, New York (1982).
6. C. Y. Chang and S. M. Sze, in ULSI Technology, Chapter 12, McGraw-Hill, New York (1996).
7. G. G. Stoney, Proc. R. Soc. London, Ser. A, 82, 172 (1909).
8. X. Feng, Y. Huang, and A. J. Rosakis, Trans. ASME, 74, 1276 (2007).
9. G. C. A. M. Janssen, M. M. Abdalla, F. van Keulen, B. R. Pujada, and B. van Venrooy, Thin Solid Films, 517(6), 1588 (2008).
10. J. G. Kim and Jin Yu, Scripta Materialia, 39(6), 807 (1998).
11. J. G. Kim, H. J. Cho, S. K. Park, S. H. Lee, B. G. Choi, J. Y. An, Y. I. Cheon, Y. H. Jeon, T. Ishigaki, K. Kang, and W. S. Yoo, JES Solid State Lett., 3(3), N11 (2014).
12. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS Trans., 61(2) 161 (2014).
13. W. S. Yoo, B. G. Kim, S. W. Jin, T. Ishigaki, and K. Kang, ECS J. Solid State Sci. and Technol., 3(11), N142 (2014).
14. S. K. Jang Jian, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, ECS J. Solid State Sci. Technol., 2(5), P214 (2013).
15. S. K. Jang Jian, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 1269 (2013).
16. I. De Wolf, Semicond. Sci. Technol., 11, 139 (1996).
17. I. De Wolf and H. E. Maes, Microsystem Technologies, 5(1), 13 (1998).
18. S. J. Harris, A. E. ’O’Neill, W. Yang, P. gustafson, J. Boileau, W. H. Weber, B. Majumdar, and N. Gobe, J. Appl. Phys., 96(12), 7195 (2004).
19. W. S. Yoo, J. Kajiwara, T. Ueda, T. Ishigaki, and K. Kang, ECS Trans., 35(4), 861 (2011).
20. W. S. Yoo, K. Kang, T. Ueda, and T. Ishigaki, Appl. Phys. Exp., 2, 116502 (2009).
21. S. K. Jang Jian, C. C. Jeng, T. C. Wang, C. M. Huang, Y. L. Wang, and W. S. Yoo, J. Mater. Res., 28(9), 1269 (2013).
22. W. S. Yoo, T. Ishigaki, T. Ueda, J. Kajiwara, K. Kang, P. Y. Hung, K. W. Ang, and B. G. Mm, ECS Trans., 45(6), 23 (2012).
23. E. G. Keim and K. Aiste, Fresenius’ Zeitschrift für analytische Chemie, 333(4–5), 319 (1989).
24. V. M. Bermudez and F. K. Perkins, Appl. Surf. Sci., 235, 406 (2004).
25. R. Hezel and N. Laoeke, J. Appl. Phys., 53, 1671 (1982).
26. http://www.semitracks.com/reference-material/failure-and-yield-analysis/failure-analysis-materials-characterization/auger-electron-spectroscopy.php
27. M. R. Ardigo, M. Ahmed, and A. Besnard, Advanced in Materials Research, 996, 361 (2014).

Downloaded on 2018-07-21 to IP 207.241.231.81 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).