Turing Machines with Two-level Memory: A Deep Look into the Input/Output Complexity*

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Abstract. The input/output complexity, which is the complexity of data exchange between the main memory and the external memory, has been elaborately studied by a lot of former researchers. However, the existing works failed to consider the input/output complexity in a computation model point of view. In this paper we remedy this by proposing three variants of Turing machine that include external memory and the mechanism of exchanging data between main memory and external memory. Based on these new models, the input/output complexity is deeply studied. We discussed the relationship between input/output complexity and the other complexity measures such as time complexity and parameterized complexity, which is not considered by former researchers. We also define the external access trace complexity, which reflects the physical behavior of magnetic disks and gives a theoretical evidence of IO-efficient algorithms.

Keywords: Computational Theory · Computational Model · Input/output Complexity

1 Introduction

The concept of data intensive computing originates in 1980s [3,6], and has been a hot research field since then [10,11,12]. As we are entering the era of big data, it is becoming more and more common to deal with data up to petabytes in many research fields, such as artificial intelligence [18], bio-informatics [8], data warehouse [17], and so on, which puts even more importance on data intensive computing. In such data intensive computing tasks, the storage and transportation of the data often become the inevitable bottleneck. The reason is that the massive data must be stored in external memory such as hard disks or solid state disks, but the speed of the external memory is usually one or two order of magnitudes slower than that of CPU and main memory. Henceforth, it is important to consider the complexity of data exchanging between main memory

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and external memory in data intensive computing, which is the well-known input/output complexity. Throughout this paper we will use IO for abbreviation of input/output.

The computational models are the canonical tool to study the computational complexity. A computational model formally defines how the computation proceeds on it, and the computational complexity is defined based on different aspects of the computation procedure. For example, the serial time and space complexity is based on the Turing machine, and the parallel time complexity is based on the PRAM model and logic circuit model. However, all classical computational models do not have the ability to model the IO operations and thus do not support the analysis of IO complexity. For example, the classical Turing machine only models the main memory computation. There is no representation of the external memory nor the mechanism of exchanging data between main memory and external memory in Turing machine.

To solve the disadvantages of classical computational models for analyzing IO operation, several models with multi-level of memory have been proposed, such as the hierarchical memory model [1] and uniform memory hierarchy model [4]. However, these models are cost models rather than computational models, which do not formally define how the computation is executed on them. These models only focus on defining the cost parameters of specified aspects of the model, and the goal is to calculate the total cost of running an algorithm on it. Taking the hierarchical memory model [1] as an example, it only defines that the cost of accessing a memory location is proportional to the length of the address. Under the parameters defined in [1], the Fast Fourier Transform algorithm which has $O(n \log n)$ time complexity on RAM model, will have $O(n \log n \log \log n)$ time complexity. In such a sense, the complexity calculated under these cost models is a total cost of main memory computation and IO operation, which can not separate the time complexity and IO complexity. However, understanding the IO complexity is more important in data intensive computing, but these cost models [1,4] fail to do so.

The most well-acknowledged model for analyzing the IO complexity is proposed in [2], which consists of four parameters $N, M, B$ and $P$. $N$ is the number of records in the input, $M$ is the size of the main memory, $B$ is the block size, and $P$ is the number of blocks that can be transferred concurrently. The IO complexity is considered as the number of IO operations to fulfill the computation task. Though well-known and well-studied, the model in [2] does not specify how the computation is executed on it like most of the cost models. Only the mechanism of data exchange between main memory and external memory is explicitly defined. Therefore, it focuses only on the IO complexity, but looses the insight on the relationship between the IO complexity and other complexities such as the time and space complexity.

To remedy the defects of existing models for analyzing the IO complexity, this paper proposes new computational models that can accurately describe the computation procedure involving main memory computation and IO operation, and thus can analyze the time, space and IO complexity simultaneously. Specif-
ically, three new variants of Turing machine are proposed in this paper. Based on these new models, we also study the IO complexity in multiple aspects.

(1) The first model, the Turing machine with two-level memory (TM-TLM), generalizes the Turing machine by equipping it with external memory and the ability to exchange data between main memory and external memory. The time, space and IO complexity of TM-TLM is defined, and the relationship between IO complexity and other kinds of complexity is studied, including the time complexity and parameterized complexity.

(2) The second model is the Random Access Turing machine with two-level memory (RATM-TLM). It is a generalization of the RATM \cite{9} model which is designed to support sub-linear time computation. The sub-linear IO complexity is discussed based on RATM-TLM.

(3) Finally the Random Access Turing machine with Blocking-IO (RATM-BIO) is proposed, which explicitly models the cost of retrieving data on external memory and reflects the behavior of hard disks. Based on RATM-BIO, the external memory access trace complexity is defined, which models the cost of retrieving data on external memory and gives an theoretical point of view of IO-efficient algorithms.

The three proposed models have different dedicated usage. The TM-TLM is the basic model since it directly generalizes the classical Turing machine. It is easier to use when analyzing the IO complexity and time complexity, and most of the results in this paper are based on TM-TLM. However, the TM-TLM can not be used to study the sub-linear time and IO complexity, and this is where the RATM-TLM should be used since it has the power of random access. Both TM-TLM and RATM-TLM consider the IO operations as special oracles and assume that an IO operation takes one unit of time. This simplifies the analysis of IO complexity, but loses the details to reflect the behavior of realistic external memory. Therefore, the RATM-BIO explicitly models the behavior of the external memory, where the pattern of external memory access can influence the cost of external memory access. In this way, RATM-BIO provides the ability to analyze the IO-efficient algorithms.

The rest of the paper is organized as follows. We first go over the related works in Section 1.1. The TM-TLM is defined in Section 2, and the relationship between IO complexity and other complexity measures such as time complexity and parameterized complexity are discussed. In Section 3, the RATM-TLM is defined, and the sub-linear time and IO complexity is studied. Section 4 defines the RATM-BIO, and discusses the external access trace complexity. Section 5 discusses the usage of the three models by raising some concrete examples. Finally Section 6 concludes the paper.

1.1 Related Works

**Two-level memory model and IO complexity.** We have mentioned the model proposed in \cite{2}, and this model is later generalized as the Parallel Disk Model (PDM). There are two variants of PDM. One assumes that there are $D$ channels inside a single disk that can transfer data simultaneously, and the
other considers that there are $D$ independent disks working together to serve one CPU. Armen et al. [5] proved that the power of the former one is strictly stronger than the latter one. The PDM model has been the standard model to analyze IO complexity, and the IO complexity of a variety of problems have been studied. The IO complexity of four basic operations on external memory is studied in [23], including scan, search, sort and output. The researchers also studied the IO complexity of more complicated problems, such as triangle enumeration [15], transitive closure [22], matrix multiplication [16] and so on. As we mentioned before, the PDM model focuses only on the IO complexity, but can not analyze the IO complexity and other complexities simultaneously.

Models with multi-level memory. Although classical computational models rarely consider the external memory, there exist many cost models that do. Some of them even consider a hierarchy of memories, reflecting the modern computer architecture which consists of multi-level cache, main memory and external memory. There are several models that consider multi-level memory, but they differ in the way of modeling the cost of accessing different level of memory.

The Hierarchical Memory Model [1] is an early work in this direction. It assumes $k$ levels of memory, each containing $2^k$ locations, and access to a location $x$ takes $\lceil \log x \rceil$ time. A later model, the Uniform Memory Hierarchy model (UMH) [4], relates the cost of memory access to the memory level number, not the memory address. It also includes several other parameters, such as the block size and the bandwidth of each level of the memory, which increases the hardness to analyze the complexity of algorithms running on this model. Another model $DRAM(h,k)$ [24] is a parallelized model which considers $k$ threads cooperating on $h$ levels of shared memory. Unlike the UMH model, where the cost of accessing data in the same level of memory is the same, $DRAM(h,k)$ considers that the cost of memory access is influenced by the memory access pattern, such as temporal and spatial locality, contiguous and non-contiguous accesses. Thus, different implementations of an algorithm may have different memory access cost on $DRAM(h,k)$ model.

These models with multi-level memory provide details that represent the realistic architecture of modern computers. However, more details make the model more complicated, and make it more difficult to use these models to analyze the performance of algorithms. Actually, two-level memory is enough to analyze the IO complexity.

IO-efficient algorithms. In most of the above models, the IO complexity is modeled as the number of IO operations multiplying the cost of a single IO operation, and the cost of each IO operation is assumed to be the same. However, as pointed out in [24], the behavior of the external memory is radically different with that of the main memory, where the cost of an IO operation may be significantly affected by the access pattern. For example, reading or writing data on contiguous blocks in external memory is a lot faster than reading or
writing data on randomly distributed blocks [19,21]. Thus, it is very important to design algorithms that is IO-efficient by taking the characteristic of external memory into consideration. A widely used technique for IO-efficient algorithm is to turn a set of non-contiguous accesses into contiguous access in a batched manner, e.g., the Log Structure Merge (LSM) tree [14]. See [13] for a good survey of IO-efficient algorithms.

2 Turing Machine with two-level memory

2.1 Definition of Turing Machine with two-level memory

As shown in Figure 1, a Turing Machine with two-level memory, TM-TLM for short, has 3-tapes. The first one is the limited main memory tape, the second one is the unlimited external memory tape, and the third one is the address tape for the external memory. The IO operations of TM-TLM are modeled as two oracles that can execute the Read and Write operations in the following way. There are two sets of special states in TM-TLM that are Read states and Write states. When TM-TLM enters a Read state, it will write an address addr to the address tape, and the content of the cell in the main memory tape where the head of the main memory tape points to will be replaced by the content at address addr in the external memory tape. For a Write state, the TM-TLM will write an address addr to the address tape, and the content of the cell at address addr in the external tape will be replaced by the content of the cell in the main memory tape where the head of the main memory tape points to. The Read and Write operations are included in the transition functions of TM-TLM. The head can shift left or right or stay in the current cell after a Read or Write operation. It is assumed that the Read and Write operations are executed in one unit of time, and they can be regarded as two special oracles. TM-TLM is formally defined in the following Definition 2.1.

Fig. 1: TM-TLM
**Definition 2.1.** A TM-TLM is a system \( \{Q, \Sigma, \Gamma, M, \delta, \text{Read}, \text{Write}, B, q_r, q_w, q_f \} \) where

- \( Q \) is the finite set of states,
- \( \Sigma \) is the finite set of input symbols,
- \( \Gamma \supseteq \Sigma \) is the finite set of tape symbols,
- \( M \) is the size of the finite main memory tape,
- \( \delta \) is the transition function: \( Q \times \Gamma \rightarrow Q \times \Gamma \times \{L, S, R\} \),
- \( \text{Read} \subset \delta \) is the read operations described in the fist paragraph of this section,
- \( \text{Write} \subset \delta \) is the write operations described in the fist paragraph of this section,
- \( B \in \Gamma \setminus \Sigma \) is the blank symbol,
- \( q_r \subset Q \) is the read states defined in the fist paragraph of this section,
- \( q_w \subset Q \) is the write states defined in the fist paragraph of this section, and
- \( q_f \in Q \) is the accepting state.

Next we define the complexity measures of TM-TLM. Since the transitions of a TM-TLM include IO operations, it is necessary to consider the IO complexity of a TM-TLM.

**Definition 2.2 (Time Complexity).** Given a TM-TLM \( M \) and an input string \( x \), the time of \( M \) on \( x \), denoted as \( T_M(x) \), is the number of transition functions except for \( \text{Read} \) and \( \text{Write} \) operations executed during the computation of \( M \) on \( x \). Further, if \( T_M(x) = O(T(n)) \) for almost all \( n \in \mathbb{Z}^+ \) and any \( |x| = n \), we say that the time complexity of \( M \) is \( O(T(n)) \).

**Definition 2.3 (IO Complexity).** Given a TM-TLM \( M \) and an input string \( x \), the IO time of \( M \) on \( x \), denoted as \( IO_M(x) \), is the number of \( \text{Read} \) and \( \text{Write} \) operations executed during the computation of \( M \) on \( x \). Further, if \( IO_M(x) = O(IO(n)) \) for almost all \( n \in \mathbb{Z}^+ \) and any \( |x| = n \), we say that the IO complexity of \( M \) is \( O(IO(n)) \).

**Definition 2.4 (Space Complexity).** Given a TM-TLM \( M \) and an input string \( x \), the space of \( M \) on \( x \), denoted as \( S_M(x) \), is the number of cells used on the external tape during the computation of \( M \) on \( x \). Further, if \( S_M(x) = O(S(n)) \) for almost all \( n \in \mathbb{Z}^+ \) and any \( |x| = n \), we say that the space complexity of \( M \) is \( O(S(n)) \).

Note that the space complexity of TM-TLM is actually the external space complexity. The main memory complexity is a fixed parameter of TM-TLM, since the size of the main memory is \( M \).

**Definition 2.5.** A \( M \)-memory \( (T(n), IO(n))-time \) \( S(n) \)-space TM-TLM \( M \) is a TM-TLM such that, the size of the main memory of \( M \) is \( M \), the time complexity of \( M \) is \( O(T(n)) \), the IO complexity of \( M \) is \( O(IO(n)) \), and the space complexity of \( M \) is \( O(S(n)) \).

Similar with the classical Turing machine, the time and IO complexity is usually more important than the space complexity for TM-TLM, and thus the
space complexity is usually omitted to describe a TM-TLM. Besides, the time and IO complexity of a $M$-memory TM-TLM may include $M$ as a parameter. For simplification, we will omit the parameter $M$ unless necessary in the rest of the paper. Throughout this paper it is assumed that $M < n$ since IO complexity will be meaningless if $M \geq n$.

2.2 TM-TLM v.s. Turing Machine

Lemma 2.1. If a function is computable by a $M$-memory $(T(n), IO(n))$-time TM-TLM, then there is a 1-memory $(T(n), T(n) + IO(n))$-time TM-TLM that can compute $f$.

Proof. Given a $M$-memory TM-TLM $M$, the 1-memory TM-TLM $M'$ simulates $M$ as follows. We use $M$ cells on the external tape of $M'$ to simulate the main memory of $M$. We call the $M$ cells as main memory mapping cells, and the other cells as external memory mapping cells. The main memory mapping cells are put on the left of the leftmost cell of external memory mapping cells, and a splitter symbol $#$ is used to split the two parts, where $#$ is not used anywhere else. The only main memory cell of $M'$ is used to transfer data between the main memory mapping cells and external memory mapping cells. $M'$ also has an register to remember the position of the main memory cell where the head of $M$ points to.

For each transition of $M$, $M'$ simulates it by two IO operations and one transition. Since the transition of $M$ affects one main memory cell, the two IO operations of $M'$ manipulates the affected main memory mapping cell accordingly. The transition of $M'$ changes the register to conform with the position of the head of $M$.

For each IO operation of $M$, $M'$ simulates it by two IO operations. For read operation of $M$, $M'$ reads from the external mapping cell and writes to the main memory mapping cell. For write operation of $M$, $M'$ reads from main memory mapping cell and writes to external memory mapping cell.

The correctness of the above simulation can be easily verified, and the time complexity of the simulation is straightforward. \qed

Theorem 2.1. If a function $f$ is computable by a $T(n)$-time Turing machine $M$, then there is a $(T(n), T(n))$-time TM-TLM $M'$ that can compute $f$.

Proof. A 1-memory TM-TLM $M'$ suffices to simulate the Turing machine. The external memory of $M'$ simulates the working tape of the Turing machine $M$. $M'$ also needs a register to remember the position on the working tape where the head points to. Then similar with the proof of Lemma 2.1, for each transition of $M$, $M'$ simulates it by two IO operations and one transition. The two IO operations changes the cell affected by the transition of $M$, and the transition of $M$ changes the value of the register to remember the new position of the head of $M$. In such way, $M'$ can correctly simulate $M$ in $(T(n), T(n))$-time.
Theorem 2.2. If a function \( f \) is computable by a \( M \)-memory \((T(n), IO(n))\)-time \( S(n) \)-space TM-TLM \( M \), then there is a \( O(T(n) + IO(n) \times S(n)) \)-time Turing machine \( M' \) that can compute \( f \).

Proof. We use a 3-tape Turing machine \( M' \) to simulate TM-TLM \( M \). The three tapes are denoted as tape-1, tape-2 and tape-3, respectively. Tape-1 of \( M' \) simulates the main memory tape of \( M \), and tape-2 and tape-3 of \( M' \) simulates the address tape and external tape of \( M \). For the main memory computations of TM-TLM \( M \), the Turing machine \( M' \) simulates them by doing exactly the same transitions on tape-1. For each IO operation of \( M \), the Turing machine \( M' \) simulates it as follows. First \( M' \) writes the address to tape-2 using \( O(\log S(n)) \) time, then the head on tape-3 moves to the designated cell using \( O(S(n)) \) time. Therefore, the each IO operation of \( M \) is simulated by \( M' \) in \( O(\log S(n)) + O(S(n)) = O(S(n)) \) time. In conclusion, the total time of simulation is \( O(T(n) + IO(n) \times S(n)) \).

2.3 TM-TLM v.s. Block Transfer TM-TLM

The realistic external memory such as magnetic disk has the ability of block transfer, i.e., a single read or write operation can transfer \( B \) records simultaneously between main memory and external memory, where \( B \) is the block size. The TM-TLM is modeled as single cell transfer which makes it easier to design algorithms on it. However, it must be proved that it does not reduce the computational power of TM-TLM by assuming single cell transfer. Here we prove that the block transfer and single cell transfer are equivalent under big-O notation.

Denote TM-TLM-BT as Turing machine with two level memory and block transfer ability. For ease of discussion, we assume that the size of the main memory \( M \) can be divided by the block size \( B \). The data in the main and external memory are aligned to the block boundary, and any IO operation will only affect a single block. Moreover, even if the IO operation asks for transferring a single cell, all the \( B \) cells in the block will be transferred simultaneously.

Theorem 2.3. If a function \( f \) is computable by a \( M \)-memory \((T(n), IO(n))\)-time TM-TLM-BT, then there is a \( M \)-memory \((T(n) + B \cdot IO(n), B \cdot IO(n))\)-time TM-TLM that can compute \( f \).

Proof. Given the \( M \)-memory TM-TLM-BT \( M \), the \( M \)-memory TM-TLM \( M' \) simulates \( M \) as follows. \( M' \) executes the same move as \( M \) for every transition \( \delta \) that is not IO operation. And for each IO operation of \( M \), \( M' \) simulates it by \( B \) consecutive IO operations which transfer exactly the same \( B \) cells between main and external memory. After transferring the data, the head of \( M' \) is moved to the same position as \( M \), using at most \( B \) moves. In conclusion, for each IO operation of \( M \), \( M' \) uses \( B \) IO operations and at most \( B \) transitions to simulate. Thus the result in the lemma follows. \( \square \)
2.4 IO complexity v.s. Parameterized Complexity

Since TM-TLM has a limited main memory of size $M$, there is an intuition that $M$ can be regard as a parameter, and a connection between IO complexity an parameterized complexity can be established.

**Lemma 2.2.** The $k$-clique problem can be solved by a $(k+1)$-memory TM-TLM in $(k^2n^k, k^2n^k)$-time.

*Proof.* The TM-TLM simulates the basic $O(k^2n^k)$-time algorithm for $k$-clique as follows. The input graph is stored on the external memory. For the main memory, the leading $k$ cells in the main memory is used to enumerate the id’s of $k$ nodes, and the last cell is used to read the edges corresponding to the enumerated nodes and check if they form a clique. Note that here we implicitly use the tape-compression technique and assumes that the id of a node or an edge can be stored in one single cell. The number of IO operations is $O(k^2n^k)$ since the algorithm enumerates all possible $k$-set of nodes, and for each $k$-set of the nodes the algorithm reads $k^2$ edges. As to the main memory computation, for each possible $k$-set of nodes, it needs $O(k)$ time to list them on the main memory tape, and $O(k^2)$ time to generate the end points of the edges to read. Then the main memory computation time complexity is $O(k^2n^k)$. □

**Definition 2.6 (Parameterized Reduction, see [7]).** Let $A, B \subseteq \sigma^* \times N$ be two parameterized problems. A parameterized reduction from $A$ to $B$ is an algorithm that, given an instance $(x, k)$ of $A$, outputs an instance $(x', k')$ of $B$ such that: (1) $(x, k)$ is a Yes-instance of $A$ if and only if $(x', k')$ is a Yes-instance of $B$, (2) $k' \leq g(k)$ for some computable function $g$, and (3) the running time of the reduction is bounded by $f(k) \cdot \text{poly}(|x|)$ for some computable function $f$.

**Lemma 2.3.** Any parameterized reduction with input instance $(x, k)$ and computable functions $f, g$ can be computed by a $\text{poly}(g(k))$-memory $(\text{poly}(f(k)) \cdot \text{poly}(|x|), \text{poly}(f(k)) \cdot \text{poly}(|x|))$-time TM-TLM.

*Proof.* By the polynomial time equivalence of Turing machine and other computation models, the parameterized reduction can be computed by a classical Turing machine in $\text{poly}(f(k) \cdot \text{poly}(|x|)) = \text{poly}(f(k)) \cdot \text{poly}(|x|)$ time. Then combining with Theorem 2.1 which uses TM-TLM to simulate Turing machine, it is proved that the parameterized reduction can be computed by a TM-TLM in $(\text{poly}(f(k)) \cdot \text{poly}(|x|), \text{poly}(f(k)) \cdot \text{poly}(|x|))$-time. The main memory size of the TM-TLM is set to $\text{poly}(g(k))$ to support computing $g(k)$ in main memory. □

**Theorem 2.4.** For a problem $\mathcal{P}$ that is FPT with parameter $k$, i.e., there is a $f(k)\text{poly}(n)$-time Turing machine that solves $\mathcal{P}$, then there exists a $\text{poly}(g(k))$-memory $(g(k)^2n^{g(k)}, g(k)^2n^{g(k)})$-time TM-TLM that can solve $\mathcal{P}$, where $g$ is a sufficiently large computable function.

*Proof.* Since the $k$-clique problem is $W[1]$-hard and the class of $\text{FPT} \subseteq W[1]$, then for every problem $\mathcal{P}$ that is FPT, there exists a parameterized reduction
from \( \mathcal{P} \) to \( k \)-clique. Then we have the following process to solve any problem \( \mathcal{P} \) that is FPT. First use the parameterized reduction to reduce \( \mathcal{P} \) to \( k \)-clique, using a \( \text{poly}(g(k)) \)-memory \( \text{poly}(f(k))\text{poly}(n), \text{poly}(f(k))\text{poly}(n) \)-time TM-TLM, as described in Lemma 2.3. The obtained instance of \( k \)-clique has a parameter of \( g(k) \) where \( g \) is a sufficient large computable function. By Lemma 2.2, this instance of \( k \)-clique can be solved using a \( (g(k) + 1) \)-memory TM-TLM in \( (g(k)^2n^{g(k)}, g(k)^2n^{g(k)}) \)-time. In conclusion, the whole above process can be done with a \( \text{poly}(g(k)) \)-memory \( (g(k)^2n^{g(k)}, g(k)^2n^{g(k)}) \)-time TM-TLM.

\[ \Box \]

3 The Random Access Turing Machine with two-level memory

Since the TM-TLM can not be used to analyze sub-linear time complexity, here we propose the Random Access Turing Machine with two-level memory (RATM-TLM), which grants TM-TLM with the ability of random access on the main memory. It is also an extension of the RATM given in [9].

**Definition 3.1.** A RATM-TLM is a system \( \{Q, \Sigma, \Gamma, M, \delta, \text{Read}, \text{Write}, B, q_r, q_w, q_a, q_f \} \) where

- \( Q \) is the finite set of states,
- \( \Sigma \) is the finite set of input symbols,
- \( \Gamma \supseteq \Sigma \) is the finite set of tape symbols,
- \( M \) is the size of the finite main memory tape,
- \( \delta \) is the transition function: \( Q \times \Gamma \rightarrow Q \times \Gamma \times \{L, S, R\} \),
- \( \text{Read} \subset \delta \) is the read operations,
- \( \text{Write} \subset \delta \) is the write operations,
- \( B \in \Gamma \setminus \Sigma \) is the blank symbol,
- \( q_r \in Q \) is the read states,
- \( q_w \in Q \) is the write states,
- \( q_a \in Q \) is the random access state, and
- \( q_f \in Q \) is the accepting state.

According to the idea that RATM-TLM is a combination of random access on the main memory tape and IO operations on the external tape, we have the following corollaries from the results in Section 2 and in [9].

**Corollary 3.1.** If \( f \) is computable by a RATM in \( T(n) \) time, then it is computable by a \( (T(n), T(n)) \)-time RATM-TLM.

If \( f \) is computable by a \( (T(n), IO(n)) \)-time RATM-TLM, then it is computable by a RATM in \( O(T(n) + IO(n)) \) time.

**Corollary 3.2.** If \( f \) is computable by a \( (T(n), IO(n)) \)-time RATM-TLM, then it is computable by a DTM in \( O((T(n) + IO(n))^2 \log (T(n) + IO(n))) \) time.
4 The Random Access Turing Machine with Blocking-IO

4.1 The definition of Random Access Turing Machine with Blocking-IO

The TM-TLM and RATM-TLM consider the IO operations as oracles, which assumes that the cost of performing IO operations and main memory computations are equal. However, in realistic computers the IO operations usually take more time than CPU computations. Therefore, in this section the cost of IO operations are modeled explicitly, which provides a theoretical point of view on IO-efficient algorithms.

The Random Access Turing Machine with Blocking-IO (RATM-BIO) is a Random Access Turing machine that can switch between computation states and IO states. There are two heads in the RATM-BIO, one for main memory computation and the other for external memory data access. They are called the main head and the external head respectively. There are four tapes in RATM-BIO, which are the main memory tape and external memory tape, and the address tapes for the two memory tapes. The main memory head is granted the ability of random access, while the external head must moves consecutively on the external tape like a classical Turing machine.

The transitions of RATM-BIO are grouped into three sets, which are the main memory computation transitions, the external memory access transitions, and read/write transitions. For the main memory computation transitions, the main head moves on the main memory tape and the external head halts. For the external memory access transitions, the main head halts and the external head moves on the external tape. This behavior reflects the blocking IO.

The main memory computation transitions and the external memory access transitions alternate via read/write operations in the following way. When entering the read(write) state, the main head will write the address of the cell in the external tape to the address tape, then the main head halts and the external head starts to move on the external tape to the designated cell. In such way, the RATM-BIO leaves the main memory computation states and enters the external memory access states. When the designated cell is reached, the content in it will replace (be replaced by) the content in the cell where the main head points to, then the external head halts and the main head starts to move again, i.e., the RATM-BIO leaves the external memory access states and enters main memory computation states. The formal definition of RATM-BIO is given below.

**Definition 4.1.** The Random Access Turing Machine with Blocking-IO (RATM-BIO) is a system \( \{Q, Q_m, Q_e, \Sigma, \Gamma, M, \delta_m, \delta_e, \text{Read}, \text{Write}, B, q_f, q_r, q_w, q_a\} \) where

- \( Q \) is the finite set of states,
- \( Q_m \subset Q \) is the finite set of main memory computation states,
- \( Q_e \subset Q \) is the finite set of external memory access states,
- \( \Sigma \) is the finite set of input symbols,
- \( \Gamma \supseteq \Sigma \) is the finite set of tape symbols,
- \( M \) is the size of the finite main memory tape,
\[\delta \text{ is the transition function: } \delta \subseteq Q \times \Gamma \rightarrow Q \times \Gamma \times \{L, S, R\},\]
\[\delta_m \subseteq \delta \text{ is the main memory computation transitions},\]
\[\delta_e \subseteq \delta \text{ is the external memory access transitions},\]
\[\text{Read } \subseteq \delta \text{ is the read operations},\]
\[\text{Write } \subseteq \delta \text{ is the write operations},\]
\[B \in \Gamma \setminus \Sigma \text{ is the blank symbol},\]
\[q_r \subseteq Q \text{ is the read states},\]
\[q_w \subseteq Q \text{ is the write states},\]
\[q_a \in Q \text{ is the random access state, and}\]
\[q_f \in Q \text{ is the accepting state.}\]

4.2 The external access trace complexity

**Definition 4.2 (external access trace complexity).** The external access trace complexity of the RATM-BIO is defined to be the total number of moves of the external head.

**Theorem 4.1.** For a \(M\)-memory \((T(n), IO(n))\)-time RATM-TLM \(M\), a \(M\)-memory RATM-BIO \(M'\) can simulate \(M\) with \(\Omega(IO(n))\) external access trace complexity.

**Proof.** This lower bound is obtained by doing IO operations on consecutive external cells. \(\square\)

**Theorem 4.2.** For a \(M\)-memory \((T(n), IO(n))\)-time \(S(n)\)-space RATM-TLM \(M\), a RATM-BIO \(M'\) can simulate \(M\) with \(O(IO(n) \cdot S(n))\) external access trace complexity.

**Proof.** The upper bound on the external access trace complexity is obtained by the following extreme situation. For each IO operation of \(M\), the external head passes through \(O(S(n))\) cells to get the destination cell. \(\square\)
According to theorem 4.1 and 4.2, the external access trace complexity of an external algorithm varies significantly using different access pattern of the external tape. It is important to make IO operations on consecutive cells, rather than random accessing. This is widely acknowledged in the research of IO-efficient algorithms, and the above two theorems give a theoretical evidence.

5 Usage of proposed models

5.1 Usage of TM-TLM

Here we provide an example to show the usage of TM-TLM on solving FPT problems.

Example 5.1. The $k$-Vertex Cover problem is known to be FPT. Consider the following fixed-parameter tractable algorithm for $k$-vertex cover. Enumerate all possible subsets of the vertex set with size $k$, then verify whether the subset is a valid vertex cover. This algorithm can be simulated on a $(k+1)$-memory TM-TLM in $(kn^k, kn^k)$-time as follows. Enumerate the subset in the main memory using $k$ cells, and read the edges from the external memory iteratively into the last cell of the main memory to verify the vertex cover. Note that the main memory usage is less than $\text{poly}(g(k))$, and the time and IO complexity is actually less than $O(g(k)^2 n^{g(k)})$ given in Theorem 2.4, where $g(k) = k$ here.

5.2 Usage of RATM-TLM

Now we present an example that needs both the ability of random access in main memory and external memory to achieve sub-linear time complexity and sub-linear IO complexity, which is searching on an external $B^+$-tree.

Example 5.2. We present a $k$-memory, $(\log_2 k \log_k n, k \log_k n)$-time TM-TLM $\mathcal{M}$ that simulates the procedure of searching on a $B^+$-tree, where $k$ is the size of a node of the $B^+$-tree. The input is a collection $\mathcal{D}$ of data, and a $B^+$-tree $T$ built for the data, which are stored in the external memory of $\mathcal{M}$ at the beginning of computation. Denote $|\mathcal{D}| = n$, then the height of the $B^+$-tree is $O(\log_k n)$, and the total size of the $B^+$-tree is $O(n)$.

When the computation starts, $\mathcal{M}$ reads the first $k$ cells of the $B^+$-tree which are the search keys stored in the root node, using $k$ IO operations. Then $\mathcal{M}$ conducts binary search in the main memory and finds the address of the next node to read. Note that the binary search in main memory must use the random access ability, which can not be achieved by classical Turing machine transitions. This search procedure is recursively executed until a leaf node is reached. Finally $\mathcal{M}$ gets the address of the data from the leaf node of the $B^+$-tree and use it to retrieve the data stored in the external memory. It can be verified that the number of IO operations is $O(k \log_k n)$, and the number of main memory operations is $O(\log_2 k \log_k n)$. 
5.3 Usage of RATM-BIO

The problem studied on RATM-BIO is the well known depth-first-search (DFS) on directed graphs. We adopt the semi-external setting, where the size of the main memory is set to $O(|V|)$. Algorithm 1 gives an main memory version of DFS.

**Algorithm 1:** DFS-Random Access

```
Input: Graph $G = (V, E)$
1 foreach vertex $u$ do
2     free[$u$]=1;
3 end
4 foreach vertex $u$ do
5     head=0;
6     stack[head]=u;
7 while $head \geq 0$ do
8     v=stack[head];
9     head–;
10    if free[$v$] then
11        free[$v$]=0;
12        foreach neighbor $w$ of $v$ do // Random access IO
13            if free[$v$] then
14                head++;  
15                stack[head]=w;
16            end
17        end
18    end
19 end
```

To execute Algorithm 1 on RATM-BIO, we need two tapes for the main memory computation. One tape stores the $free[v]$ array using $|V|$ cells, and the other tape simulates the stack. It can be verified that the size of the stack does not exceed $O(|V|)$, which satisfies the requirement of semi-external setting.

**Theorem 5.1.** If the edges of the input graph $G = (V, E)$ is given on the external tape as adjacent lists, then the worst case external access trace complexity of Algorithm 1 on RATM-BIO is $O(|V||E|)$.

**Proof.** According to Algorithm 1, the only IO operation is incurred by Line 12, which reads the adjacent list of each node in an unpredictable order. In such way, there always exists a bad access order of the nodes and a bad allocation of the adjacent lists on the external tape, which forces the external head to move for a distance of $\Theta(|E|/2)$ to access the next adjacent list. Figure 3 demonstrates the idea.

Thus, the worst case external access trace complexity is $\sum_{v \in V} \{d_v + |E|/2\} = O(|V||E|)$. $\square$
Theorem 5.2. If the edges of the input graph $G = (V, E)$ is given on the external tape in an arbitrary order, then the worst case external access trace complexity of Algorithm 1 on RATM-BIO is $O(|E|^2)$.

Proof. Given the situation that the edges are stored in an arbitrary order, the neighbors of node $v$ can not be retrieved by consecutive IO operations when executing Line 12. After reading one edge, the external head must move a long distance to get the next edge. Using the same idea in proving the above theorem, there always exists a bad access order to the edges and a bad allocation of the edges on the external tape, which forces the external head to move for distance of $\Theta(|E|)$ between two read operation. Multiplying $|E|$ read operations and $O(|E|)$ moves for each read operation, the result of this theorem is proved. \[\square\]

The above two theorems show the importance of data arrangement on the external memory to avoid random access. It also reveals the importance to design IO-efficient algorithms, whose performance is not affected by the data allocation on the external memory. Here we cite the following algorithm from [20] given in Algorithm 2, which is a good example of IO-efficient algorithm. The performance of it is irrelevant of the allocation order of the edges.

Theorem 5.3. Even if the edges of the input graph $G = (V, E)$ is given on the external tape in an arbitrary order, the worst case external access trace complexity of Algorithm 2 on RATM-BIO is $O(|V||E|)$.

Proof. Then it only need to prove the maximal number of times for scanning the edges. The depth of the initial spanning tree $T$ is at least 1, and we claim that after one full scan of the edge set, the depth grows at least 1. The detailed proof is omitted. Since the depth of the spanning tree is at most $|V|$, the edges are scanned for at most $|V|$ times. Thus the theorem is proved. \[\square\]

6 Conclusion

In this paper we proposed three computation models to analyze the IO complexity deeply. The three models are TM-TLM, RATM-TLM and RATM-BIO, which model the behavior of the main memory and external memory in different
Algorithm 2: DFS-IO-efficient

\begin{algorithm}
\textbf{Input:} Graph $G = (V, E)$, memory size $M$
1 Initialize the spanning tree $T$ of graph $G$;
2 $update \leftarrow \text{true}$;
3 \textbf{while} $update$ do
4 \hspace{1em} $T, \leftarrow \text{Restructure}(G, T, M)$;
5 \textbf{end}
6 \textbf{return} $T$;
7 \textbf{Procedure} Restructure($G, T, M$):
8 \hspace{1em} $update \leftarrow \text{false}$;
9 \hspace{2em} \textbf{for any edge} $(u, v)$ in $G$ do
10 \hspace{3em} \textbf{if} $(u, v)$ is forward-cross edge then
11 \hspace{4em} $update \leftarrow \text{true}$;
12 \hspace{4em} $w \leftarrow$ the parent of $v$ in $T$;
13 \hspace{4em} delete edge $(w, v)$ from $T$;
14 \hspace{4em} add edge $(u, v)$ iton $T$;
15 \hspace{3em} \textbf{end}
16 \hspace{2em} \textbf{end}
17 \hspace{1em} \textbf{return} $(T, M)$;
18 \end{algorithm}

Based on TM-TLM and RATM-TLM, the relationship between IO complexity and other complexity measures are deeply studied. Besides, the external access trace complexity defined based on RATM-BIO can reflect the different cost of different external memory access pattern, and provides a theoretical point of view about the IO-efficient algorithms. These new results provide a deep look into the IOt complexity, and open a new way to study the IO complexity.

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