The Pixel Detector of the ATLAS experiment for LHC Run-2

H. Pernegger on behalf of the ATLAS Pixel collaboration

_CERN Physics Department,
CH-121 Geneve 23, Switzerland

E-mail: Heinz.Pernegger@cern.ch

ABSTRACT: The Pixel Detector of the ATLAS experiment has shown excellent performance during the whole Run-1 of LHC. Taking advantage of the long shutdown, the detector was extracted from the experiment and brought to surface, to equip it with new service quarter panels, to repair modules and to ease installation of the Insertable B-Layer (IBL). IBL is a fourth layer of pixel detectors, and has been installed in May 2014 between the existing Pixel Detector and a new smaller beam pipe at a radius of 3.3 cm. To cope with the high radiation and hit occupancy due to the proximity to the interaction point, a new read-out chip and two different silicon sensor technologies (planar and 3D) have been developed. Furthermore, the physics performance will be improved through the reduction of pixel size while, targeting for a low material budget, a new mechanical support using lightweight staves and a CO$_2$ based cooling system have been adopted. An overview of the refurbishing of the Pixel Detector and of the IBL project as well as the experience in its construction will be presented, focusing on adopted technologies, module and staves production, qualification of assembly procedure, integration of staves around the beam pipe and commissioning of the detector.

KEYWORDS: Detector design and construction technologies and materials; Radiation-hard detectors; Large detector systems for particle and astroparticle physics; Particle tracking detectors (Solid-state detectors)
1 Introduction

The ATLAS Pixel Detector [1] is the inner-most part of the ATLAS tracking system [2]. The ATLAS Pixel Detector for LHC Run-2 consists of 4 layers of barrel pixel detector and two end caps of three pixel disks each. The outer 3 barrel layers and the disks are the 3-Layer Pixel Detector system, which was installed originally in 2007 in ATLAS and serviced during 2013/2014. The innermost pixel layer is a newly constructed high-resolution pixel detector, called Insertable B-Layer (IBL). Figure 1 shows the 4-Layer ATLAS Pixel Detector for LHC Run-2 (left) and the radial placement of concentric pixel barrels, beam pipe and support carbon-fibre cylinders (IPT, IST) (right). The Pixel Detector sits inside the 2T solenoidal magnetic field and contributes to the charged particle tracking of the ATLAS Inner Detector in the pseudo rapidity range of $|\eta| < 2.5$.

Due to its high spatial resolution and 3-dimensional space-point measurement the Pixel Detector has a key-role in reconstruction of charged particle tracks. The 4-Layer Pixel Detector will be crucial in the reconstruction of primary and secondary vertices which is essential for the detection of long-lived particles, e.g. containing b-quarks, and in searches for new physics at LHC.

2 Operation in LHC Run-1 and motivation for Pixel Detector upgrade for Run-2

The initial Pixel Detector was designed to operate at peak instantaneous luminosities of up to $1 \times 10^{34}$ cm$^{-2}$s$^{-1}$ and performed very well during LHC Run-1 with tracking efficiency of 99% and spatial resolution of $\approx 8\mu m$ in $r\phi$ and $75\mu m$ in $z$. It operated with noise of 160 e$^-$, threshold of 3500 e$^-$, data-taking up-time of 99.9%, and its supply and readout system operated stably. Figure 2 (left) shows the hit to track association efficiency for different layers of the Pixel Detector during Run-1. Non-operational modules are removed from the efficiency calculation. The figure gives the hit efficiency in the acceptance area of the active sensor volume of a specific layers, to which the
track is extrapolated and which is not used in the track reconstruction. Figure 2 (right) illustrates the stability of its $dE/dx$-calibration through the stability of proton mass calculated from the momentum measured in the Inner Detector and the specific energy loss measured in the Pixel Detector.

During the coming years LHC is expected to significantly exceed its design peak luminosity and reach $> 2 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$. In its different bunch-spacing operation modes of 25 ns and 50 ns this will lead to many over-lapping interactions in a single bunch-crossing (“pile-up”), hence the necessity to separate different events through their primary vertex positions. During the LHC Long Shutdown 1 (“LS1”) the previous 3-Layer detector system was upgraded to a 4-Layer detector system with the IBL to maintain and even improve its performance in the presence of large pile-up of $> 50$ events per bunch-crossing and to improve its impact parameter resolution in primary and secondary vertex reconstruction [3]. Furthermore the new 4-Layer system will provide increased robustness in pattern recognition and tracking if efficiency is lost due to radiation damage or faults on individual modules. Figure 3 (left) shows the improvement in $z$-impact parameter resolution from 3-Layers (histogram) to 4-Layer pixel system (markers). Figure 3 (right) shows the expected improvement in light-jet rejection at different $b$-tagging efficiency in $t\bar{t}$ events.

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**Figure 1.** Schematic view of the ATLAS 4-Layer Pixel Detector for Run-2.

**Figure 2.** Left: hit to track association efficiency in different sections of the Pixel Detector during Run-1. Right: illustration of signal stability by reconstructing the proton mass from pixel $dE/dx$ and Inner Detector momentum measurement.
Figure 3. Expected performance of the upgraded 4-Layer Pixel system in comparison to the Run-1 3-Layer system — Left: $z$-direction impact parameter resolution versus track $p_T$ of 3-Layer system (histogram) and 4-Layer system (markers). Right: light jet rejection factor versus $b$-tagging efficiency in simulated $t\bar{t}$ events for the 3-Layer system (blue) and 4-Layer system (right) [3].

3 Maintenance and upgrade of the existing Pixel Detector system

The increased peak luminosity beyond design values will also cause saturation of data transmission links from modules to back-end electronics in the outer-most layers which in turn will lead to loss of hit efficiency. First signs of this efficiency loss became apparent at end of Run-1. Furthermore during Run-1 the number of disabled modules increased from 2% at the beginning to 5% at the end of Run-1 due to individual module failures like low voltage or high voltage powering faults or data transmission faults. For these reasons the existing Pixel Detector was deinstalled at the beginning of LS1, disassembled and equipped with new services, the so-called “New Service Quarter Panels” (nSQP). The nSQP provide all electrical and cooling connections between the detector active volume and the outside pixel connectors at $|z| \approx 3.5$ m. Four nSQP serve each side of the Pixel Detector.

The data transmission system was completely renewed by installing new data cables, new electrical-to-optical converter boards (“opto boards”), and new data fibres. This allowed to move the sensitive parts of the data transmission chain (e.g. opto boards) to locations outside the tracker volume, where they can be easily maintained in the future. In addition the number of data links was increased in the two outer-most layers. Increasing the number of data links will allow to overcome the bandwidth saturation up to peak luminosities approaching $3 \times 10^{34}$ $\text{cm}^{-2}\text{s}^{-1}$. The data bandwidth for Pixel Layer 2 (outer-most layer) is now increased to 80 Mbps per module and on Layer 1 (middle layer) to 160 Mbps per module, i.e. a factor two over the Run-1 system. To take full advantage of the new data transmission bandwidth also the backend-electronics readout driver modules (ROD, BOC) will be upgraded from the existing one to the newly developed ones for the IBL on those two layers. The newly developed ROD and BOC cards for IBL provide more computing power as they are based on modern FPGAs rather than obsolete DSPs.

The Pixel detector was de-installed from the ATLAS cavern in April 2013. On the surface the old service quarter panels were disconnected close to the active volume just behind the end cap sections. During the disconnection inspections and fault tests were carried out to determine the reason
for faults. Figure 4 shows the fault analysis results for the 88 malfunctioning modules out of 1744 pixel modules. Data communication faults dominate, followed by broken HV connections. Former are in most cases repairable, while latter ones are often inside the active volume and not accessible for repair. During two years prior to the start of LS1, eight new service quarter panels (nSQP) were constructed and tested to function with 100% of all connections. After the old SQPs were removed, the nSQP were installed and the pixel detector was reconnected. In the process of reconnection, faults which were located outside the pixel active volume could be repaired (e.g. opto-faults, communication faults), faults directly on modules (e.g. disconnected HV lines on modules) could not be repaired as the end caps and barrels were not dismounted. After the pixel detector was reassembled, a final round of tests was made on the surface and the detector was reinstalled into ATLAS in December 2013. In the first half of 2014 the detector was connected to power supply, readout and cooling systems. After the detector connection was completed, the supply and communication to all modules was retested. Figure 5 gives the summary of test results at different phases of assembly and at the end after reinstallation and reconnection. The defect modules are reduced from 5.0% at end of Run-1 to 1.9% now at the start of Run-2. The biggest improvements are achieved on the B-Layer (“L0”) and the outermost layer (“L2”), where the fault fraction is reduced from 6.3% to 1.4% and from 7.0% to 1.9% respectively.

4 Construction, tests and installation of the new Insertable-B-Layer

In order to upgrade the existing 3-Layer system to a 4-Layer system with the benefits outlined in section 2, it was decided to add a fourth pixel layer in the inside of the existing system. This however required the development of several new technologies in order to cope with the expected instantaneous luminosity, high hit rates and track density as well as high radiation damage expected at small radii:

- New beam pipe — installing a new detector layer on the inside of the existing system required additional radial space between the B-Layer and the beam pipe. For this reason a new beryllium beam pipe of 0.8 mm wall thickness with a reduced inner diameter of 47 mm was developed with low-profile flanges to fit inside the IBL. Special emphasis was given to
Number of Module Failures by Layer. Status at the end of Run 1, after reconnection on the surface and after reinstallation in the Pit.

Figure 5. Results of function tests at different stages of pixel detector maintenance: at end of Run-1 (dark blue), after replacement of service quarter panels with nSQP (light blue) and after reinstallation and reconnection completed (middle blue). The figure shows the results for the total pixel detector, as well as split up by barrel layer and disks. The number of pixel modules per layer are: L0=286, L1=494, L2=676, Disks=288.

The reduction of material and tests on a 1:1-scale mock-up of beam pipe and IBL to study the system behaviour, thermal distribution and system safety during the beam pipe bake-out. The tests showed e.g. that the CO$_2$ cooling is capable of keeping the IBL temperatures well within normal range during bake-out even if the 3 mm thick insulation foam on the outside of the beam pipe is removed in the central section, which significantly reduces material.

- **New sensors** were required by the expected radiation damage and the pixel size reduction from 50×400 µm to 50×250 µm. Smaller pixels in z-direction improve impact parameter resolution as well as lead to better cluster separation in high track densities like strongly boosted jets. The new sensors have to cope with radiation damage resulting from 300 fb$^{-1}$ integrated luminosity expected until the LHC-Phase-II upgrade. Including safety factors IBL sensors are qualified for radiation hardness up to 5×10$^{15}$ 1-MeV n$_{eq}$cm$^{-2}$. New n-in-n planar silicon sensors and 3D silicon sensors were developed with minimal dead guard ring area on the edge (< 200 µm inactive edge) and hit efficiency of better than 97% after full irradiation.

- **New readout chip FE-I4** [4] — the IBL sensors are installed at a radius of 33 mm from the beam axis, which results in hit rates beyond the capabilities of the existing FE-I3 pixel chip. A new readout architecture, which includes local data buffering in the pixel region, allows to operate the new pixel chip at a radius of 33 mm and peak luminosity of 3×10$^{34}$cm$^{-2}$s$^{-1}$ without significant efficiency loss. Its large size of 19×21 mm$^2$ reduces the chip area taken by periphery circuitry to less than 11% of the overall area and significantly reduces overall module costs.
organized in a matrix of 80 columns (on 50 µm pitch) by 336 rows (on 250 µm pitch). Each

Figure 6. Left: 3D rendering of the IBL detector with its 14 staves (some staves removed to make the module side of staves visible). Each stave consists of twelve planar double-chip modules and two times four 3D sensor single-chip modules. Right: photo of the IBL during its installation inside the Pixel Detector in the ATLAS cavern.

- **New light weight supports and cooling** — to fully exploit the benefits of a high resolution pixel layer close to the beam it is mandatory to reduce the radiation length per layer from $X/X_0 \approx 3\%$ to the finally achieved $X/X_0 \approx 1.9\%$. Thin (55 µm) prepreg carbon fibre sheets, low-density carbon foam and thin-wall titanium cooling pipes are used in the construction of supports and cooling to reduce material. The staves are cooled using a two-phase CO$_2$ refrigeration with a minimal coolant temperature of $\approx -35^\circ$C inside the staves.

The IBL consists of 14 pixel staves mounted on a central support tube (“IPT”) which supports the staves at their extremities and holds all services from stave ends to outside connectors at $|z|=3.5$ m. The new beam pipe is located inside the IPT and is inserted to the IPT prior to the surface integration of the IBL. The entire IBL package is supported by the IBL Support Tube (IST), which is installed inside the B-Layer of the pixel detector (see figure 1). The IST provides the support and position referencing of IBL to Pixel. Each IBL stave carries 20 modules with 32 FE-I4 chips: in the stave centre twelve planar sensor double-chip modules and four 3D sensor single-chip modules at each end (figure 6). While the modules face the beam on the inside of the staves, a multilayer flex-circuit is glued to the outside of the stave, visible on the photo, to supply each modules with power and readout. In the active detector volume, the radiation length for the total IBL package is $X/X_0=1.9\%$, which is comprised of $X/X_0=0.6\%$ for modules, $X/X_0=0.6\%$ for carbon fibre support staves with cooling and $X/X_0=0.7\%$ for all support cylinders and services.

4.1 **IBL modules**

The IBL double-chip module uses planar n-in-n silicon sensors similar to the outer layers, however the inactive edges are significantly reduced, which allows to maximise the acceptance area without complex $z$-overlapping design. Each planar sensor carries two FE-I4 readout chips with 80 columns.

$^1$Given in the active detector area for perpendicular incident and including all services, support structure and cooling.

$^2$K13C/RS3 carbon fibre prepreg supplied by Tencate/U.S.A.
and 336 rows of pixels each. The IBL single-chip module uses a 3D silicon sensor, with a double column design of vertical electrodes with 50 µm pitch. A fence ring surrounds the active pixel matrix. The 3D sensors were produced by manufacturers CNM\(^3\) and FBK\(^4\). The IBL is the first large-scale use of 3D silicon sensors in a collider experiment. The IBL construction also provided substantial information for future production and operation of 3D sensors also in view of future tracker upgrades.

Sensors, FE-I4 and module design are described in reference \[5\]. Sensor and FE-I4 are bump-bonded together using solder bump-bonding. Prior to bump-bonding the FE-I4 is thinned to 150 µm thickness. A temporary glass wafer supports the thinned chips during the bump-bonding in order to avoid chip warping during reflow. The sensor-FE-I4 assembly is completed to a module by gluing a thin Cu-kapton flex circuit on the sensor back-plane side, which is then wire bonded to all chip and sensor connections. A total of \(\approx 700\) modules were assembled and subjected to burn-in, thermal cycling, source tests and detailed electronics tests. The yield of accepted modules for planar modules is 75% and for 3D modules 63% after initial bump-bonding difficulties were resolved.

### 4.2 Stave construction and tests

The IBL carbon fibre stave is constructed of a 165 µm carbon fibre shell filled with low-density carbon foam. A 1.5 mm titanium cooling pipe in the centre of the stave provides cooling for modules. A cross section of a carbon fibre stave and a photo of modules on staves are shown in figure 7. Modules are fixed to the top face-plate with a 70 µm thick layer of thermal grease and two glue dots. To avoid dusting and electrical shorts, the carbon fibre top surface is parylene coated. After modules are mounted, the completed IBL stave is tested electrically, thermally and the module positions are surveyed \[6\]. A total of 20 staves have been constructed of which 18 fulfilled the acceptance criteria. Of the accepted 18 staves the best 14 were selected for use in the experiment. Figure 8 shows summary plots of stave quality tests. The staves used in the experiment have only 0.09% bad pixels and all chips and sensors are fully operational (acceptance criteria < 1% dead pixels). Plots (c) and (d) show that staves operate stably at thresholds of 1500 e\(^-\), which is important for future operation after irradiation. The ENC noise per chip is shown in plot (d). Planar

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\(^3\)Centro Nacional de Microelectronica. Campus Universidad Autonoma de Barcelona, Spain.

\(^4\)Fondazione Bruno Kessler, Trento, Italy.
modules show a typical noise of $125 \ e^-$, 3D modules a noise of $150 \ e^-$. The staves were cooled at $-20^\circ C$ for the measurements of threshold and noise.

### 4.3 Integration and installation

To prepare the selected staves for mounting to the IPT support, first the titanium cooling pipe extensions need to be brazed to the cooling pipe ends of each stave. The resulting object is 7m long and supported during the integration with carbon-fibre frames. Each stave is placed on stave support rings, which are mounted to the IPT and provide the position referencing. Stave support rings are visible in figure 6 as grey rings. After the stave is mounted services are connected to either side of the stave. Electrical readout and biasing tests of each module confirm the continuity of all services and functioning of all modules. With the surface integration of the IBL completed, the IBL package was installed in the experiment in May 2014 and connected to supply and readout systems. We confirm the continuity of the service connection and test the module function in the final configuration by repeating the stave test procedure in the pit. Figure 9 gives the results of initial commissioning.

5The slight difference between A-side and C-side of 3D modules is due to an artefact of the test system.
Figure 9. Average, minimal and maximum ENC noise per chip for all staves after installation during initial commissioning (a). Chip threshold after tuning for planar, CNM and FBK 3D modules during initial commissioning.

tests after installation. Plot (a) shows the noise per chip as function of chip number of all IBL staves, which confirms the excellent noise performance of the final installed detector. Plot (b) shows the threshold distribution after tuning during the initial commissioning in the pit with a dispersion of 6 e\(^{-}\). All chips and modules are found to be fully functional after IBL installation and connection. These initial commissioning tests were carried out at room temperature (cooling at +15°C) because the final Inner Detector environmental gas seals were not yet in place and at higher threshold.

5 Summary

The ATLAS Pixel detector has performed very well during LHC Run-1. For Run-2 the pixel detector has to cope with increasing instantaneous luminosity and pile-up of > 50 collisions per bunch-crossing. The pixel detector has a key role in the data analysis as it provides primary and secondary vertex reconstruction as well as b-tagging. To maintain and even improve the performance of the ATLAS tracking system in the presence of large pile-up, the Pixel Detector was upgrade from a 3-Layer system to a 4-Layer system by including the newly constructed Insertable B-Layer (IBL) inside the existing system during the LHC shutdown 2013/14. The existing system was equipped with new service quarter panels (nSQP) to increase the data transmission bandwidth from detector to backend electronics and known faults on the detector were repaired. The new 4-Layer Pixel detector for Run-2 is installed and commissioned. The innermost layer, the IBL, shows less than 0.1% defect channels and can operate at 1500 e\(^{-}\) threshold and low noise. On the outer three layers 98% of all modules are fully functional and are equipped to operate up to 3 × 10\(^{34}\) cm\(^{-2}\)s\(^{-1}\) instantaneous luminosity without significant efficiency loss. The new 4-Layer system will provide robust pattern recognition and tracking in the future in case modules are lost accidentally or when the B-Layer will loose efficiency due to radiation damage and high hit rates.
References

[1] G. Aad et al., *ATLAS pixel detector electronics and sensors*, 2008 *JINST* 3 P07007 [inSPIRE].

[2] ATLAS collaboration, *The ATLAS experiment at the CERN Large Hadron Collider*, 2008 *JINST* 3 S08003 [inSPIRE].

[3] ATLAS collaboration, *ATLAS insertable B-layer technical design report*, CERN-LHCC-2010-013, CERN, Geneva Switzerland (2010).

[4] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*, *Nucl. Instrum. Meth.* A 636 (2011) S155 [inSPIRE].

[5] ATLAS IBL collaboration, *Prototype ATLAS IBL modules using the FE-I4A front-end readout chip*, 2012 *JINST* 7 P11010 [arXiv:1209.1906] [inSPIRE].

[6] ATLAS collaboration, *ATLAS Pixel IBL: stave quality assurance*, ATL-INDET-PUB-2014-006, CERN, Geneva Switzerland (2014).