Conversion of Multi-layered MoTe₂ Transistor Between P-Type and N-Type and Their Use in Inverter

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Abstract

Both p-type and n-type MoTe₂ transistors are needed to fabricate complementary electronic and optoelectronic devices. In this study, we fabricate air-stable p-type multi-layered MoTe₂ transistors using Au as electrode and achieve the conversion of p-type transistor to n-type by annealing it in vacuum. Temperature-dependent in situ measurements assisted by the results given by first-principle simulations indicate that n-type conductance is an intrinsic property, which is attributed to tellurium vacancies in MoTe₂, while the device in air experiences a charge transfer which is caused by oxygen/water redox couple and is converted to air-stable p-type transistor. Based on p-type and n-type multi-layered MoTe₂ transistors, we demonstrate a complementary inverter with gain values as high as 9 at VDD = 5 V.

Keywords: MoTe₂, P-type, N-type, Absorbates, Vacancies

Background

Graphene and similar two-dimensional (2D) materials exist in bulk form as stacks of strongly bonded layers with weak interlayer attraction, allowing itself to be exfoliated into atomically thin layers, which have opened up new possibilities for the exploration of 2D physics as well as that of new material applications [1–9]. Of them, semiconductor transition metal dichalcogenides (TMDs) exhibit sizeable bandgaps [2, 3, 10, 11]. In addition, these 2D TMD flakes are flexible and free of dangling bonds between adjacent layers [12, 13]. These unique properties make TMDs promising candidates to construct electronic and optoelectronic devices [2–4, 14], such as next-generation field-effect transistor (FET) at sub 10 nm [15], inverter [16–22], and on-chip light-emitting diode (LED) [23–25] and Van der Waals heterostructure devices [4, 5, 26–28].

2H-type molybdenum ditelluride (2H-MoTe₂) is one of the typical 2D TMDs, which has an indirect bandgap of 0.83 eV in bulk form [29] and a direct bandgap of 1.1 eV when it is thinned to a monolayer [30]. 2H-MoTe₂ has been explored for applications in spintronics [31], FET [32–34], photodetector [35–38], and solar cell [39]. Like most 2D materials, multi-layered 2H-MoTe₂ has very high surface-to-volume ratio, making it sensitive to various influences in the surrounding environment. Thus, it is difficult to obtain its intrinsic properties. The surface and interface of 2D materials and related devices have always been research hotspots in order to achieve higher performance. Here, we fabricate a multi-layered 2H-MoTe₂ transistor, whose source and drain electrode layers are fabricated, and then, a multi-layered MoTe₂ sample is transferred to bridge the source and drain electrodes as a transistor channel. The whole MoTe₂ sample is exposed in air, including the channel and contact part, which is advantageous to investigating the influence of absorbates on charge transport properties of multi-layered MoTe₂ transistor. Measurements of vacuum- and temperature-dependent charge transport are conducted. The experimental data show that multi-layered MoTe₂ transistor is an n-type in terms of intrinsic conductance. However, the device exposed in air can be doped by absorbates and converted...
to air-stable p-type transistor. We infer that the intrinsic n-type conductance of multi-layered MoTe₂ transistor is attributed to tellurium (Te) vacancies, which is confirmed by density functional theory (DFT) calculations. The conversion to p-type conductance in air can be explained by the fact that oxygen and water absorbed in air can induce electron transfer from MoTe₂ to oxygen/water redox couple, which converts n-type multi-layered MoTe₂ transistor to p-type. Finally, based on the n-type and p-type multi-layered MoTe₂ transistors, we demonstrate a complementary inverter, which shows symmetric input/output behavior and gain values of 9 at $V_{DD} = 5 \text{ V}$.

**Results and Discussion**

Different from the previously reported multi-layered MoTe₂ transistor, our device diagram is shown in Fig. 1a. We first fabricate source-drain (SD) electrodes composed of Cr/Au film on SiO₂/p⁺-Si substrate. Then, one of the multi-layered MoTe₂ samples prepared on another SiO₂/p⁺-Si substrate is transferred to bridge the source-drain electrodes as transistor channel. The MoTe₂ sample made by this method is clean and free of polymer contamination in device fabrication. In addition, the whole MoTe₂ sample is exposed in air, including the channel and contact part, making it more convenient to remove absorbates and obtain intrinsic conductance of multi-layered MoTe₂ transistor. An optical image of a fabricated multi-layered MoTe₂ transistor is shown in Fig. 1b, with a channel length of 10 μm. The MoTe₂ channel is characterized by atomic force microscopy (AFM) (see Fig. 1c). Height profile (see Fig. 1d) obtained from the mark in AFM image indicates that the thickness of MoTe₂ sample is about 17 nm (composed of 24 monolayer MoTe₂) [40]. The characteristic Raman-active modes of $A_{1g}$ (172 cm$^{-1}$), $E_{1g}^{1}$ (233 cm$^{-1}$), and $B_{1g}^{2}$ (289 cm$^{-1}$) are clearly observed as shown in Fig. 1e, indicating the good quality of 2H-MoTe₂ after the transfer process [41].

The fabricated back-gated multi-layered MoTe₂ transistors are measured using Agilent B1500A semiconductor analyzer in Lakeshore probe station, which can be pumped to a base pressure of $1 \times 10^{-5}$ mbar and realize 9–350 K temperature adjustment. Figure 2 shows the electric properties of a multi-layered MoTe₂ transistor in air at room temperature (RT). The transfer characteristics at source-drain voltage $V_{sd} = 1 \text{ V}$ in Fig. 2a show that the transistor is in on-state at negative gating voltage and in off-state at positive gating voltage. The transform voltage from on-state to off-state is nearly zero, which is a typical p-type transistor characteristic. Replicate measurements show the same electric gating characteristics (see Additional file 1: Figure S1). Four other multi-layered MoTe₂ transistors also demonstrate similar p-type electric gating characteristics as shown in Additional file 1: Figure S2. We also prepare other devices with thicknesses of 5 nm, 38 nm, and 85 nm as shown in Additional file 1: Figure S3. When the MoTe₂ thicknesses are 5 nm and 38 nm, both the prepared devices show p-type conductance but with small on-current compared with the device in Fig. 2 and Additional file 1: Figure S2. As the thickness increases to 85 nm, the gating effect disappears as shown in Additional file 1: Figure S3 (l). These data show that

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p-type conductance is universal in air for multi-layered MoTe$_2$ transistor. From transfer characteristics in Fig. 2a, we can obtain the on-off ratio, subthreshold swing (SS), and field-effect mobility ($\mu$), which are $6 \times 10^3$, 350 mV/dec, and 8 cm$^2$/V·s, respectively.

Figure 2b shows the output characteristics of multi-layered MoTe$_2$ transistor at back-gate voltage $V_{bg} = -20$ V, $-15$ V, $-10$ V, $-5$ V, 0 V, and 5 V. As seen, the response is essentially linear, especially at low biased voltage of $V_{sd}$ which indicates there is negligible effective Schottky barrier height ($\Phi_{SB}$) between Au and MoTe$_2$ in air. The transfer characteristics at different source-drain biased voltages as shown in Fig. 2c indicate that the on-current increases linearly with biased voltage $V_{sd}$ shown in Fig. 2d, which coincides with the output characteristics. Meanwhile, the off-current increases and on-off ratio decreases as $V_{sd}$ increases. This can be attributed to trap state in MoTe$_2$ channel from absorbates and interface state. The hysteresis in transfer characteristics (see Additional file 1: Figure S4) further confirms the existence of trap state in MoTe$_2$ transistor [42–45].

We further investigate the p-type conductance of multi-layered MoTe$_2$ transistor at different vacuums. This is helpful to understand the influence of absorbed oxygen and water on the charge transport properties. Figure 3a shows the transfer characteristics at $V_{sd} = 1$ V as a function of vacuum (“atm” corresponds to atmosphere). The major changing tendencies are clearly indicated by red arrows, which is similar to that shown in carbon nanotube transistor [44]. First, the on-current decreases as vacuum increases, which is partially due to the shift of threshold voltage caused by absorbates but mainly due to device resistance increase as absorbates decrease, including channel and contact resistance. The
nonlinear output characteristics as shown in Fig. 3b indicate the enhanced effective Schottky barrier between Au and MoTe₂ in 2.9 × 10⁻⁵ mbar vacuum, which suggests that the effective Schottky barrier height is modified by absorbates in air. Second, the off-current at positive voltage gating increases with the vacuum, which means that electron conductance increases as absorbates decrease and suggests that n-type conductance is suppressed in multi-layered MoTe₂ transistor by absorbates in air.

Although the on-current decreases and off-current increases after eliminating partial absorbates in vacuum, the multi-layered MoTe₂ transistor still exhibits p-type conductance. Furthermore, p-type conductance maintains at low temperature as shown in Fig. 4a. This temperature-dependent electric property helps us to further elucidate the charge transport mechanism and extract the effective Schottky barrier height of p-type MoTe₂ transistor. Figure 4a gives the transfer characteristics at biased voltage \( V_{sd} = 1 \) V as temperature varies from 20 to 275 K. Both on-current and off-current decrease as temperature decreases, and the on-off ratio increases at low temperatures as shown in Fig. 4b. Arrhenius plot of the source-drain current \( I_{sd} \) at back-gate voltage \( V_{bg} = -20 \) V and 20 V in Fig. 4c indicates the thermal emission and tunneling contribution for charge transport [46]. When temperature is higher than 100 K, a clear thermal emission region is observed in both negative and positive gating voltages, and the tunneling current dominates when temperature is below 100 K. That is why both on-current and off-current decrease as temperature decreases. Based on the thermal emission current observation and the relationship of \( I_{sd} \sim e^{-\Phi_{SB}/kT} \), where \( k \) is the Boltzmann constant and \( T \) is temperature, we extract the effective Schottky barrier height \( \Phi_{SB} \) as a function of gate voltage at \( V_{sd} = 1 \) V, as shown in Fig. 4d. The effective Schottky barrier heights \( \Phi_{SB} \) in both on- and off-state are smaller than 120 mV.

Vacuum and low temperature make it difficult to desorb the absorbates completely. The residual absorbates still work and alter the conductance of multi-layered MoTe₂ transistor. In order to further desorb the absorbates on MoTe₂ transistor, we heat the device to 350 K in vacuum and carry out in situ electric property measurements. Figure 5a shows the transfer characteristics of MoTe₂ transistor as it is heated from 250 to 350 K. As seen, the electron conductance at positive gate voltage is enhanced, while hole conductance at negative gate voltage is reduced as temperature increases. At temperature \( T = 250 \) K, the device shows a typical p-type conductance. But when temperature increases to \( T = 350 \) K, the device is converted to n-type, which is in off-state at negative gate voltage and in on-state at positive gate voltage. Its on-off ratio, subthreshold swing (SS), and field-effect mobility (\( \mu \)) are 3.8 × 10², 1.1 V/dec, and 2 cm²/V·s, respectively.

Fig. 4 Temperature-dependent electric properties of a p-type multi-layered MoTe₂ transistor. a Transfer characteristics of MoTe₂ transistor at \( V_{sd} = 1 \) V as a function of temperature. b On-current, off-current, and on-off current ratio as a function of temperature. c Arrhenius plot of the source-drain current as a function of temperature at \( V_{sd} = 1 \) V and \( V_{bg} = -20 \) V and 20 V, respectively. d Maps of effective Schottky barrier heights \( \Phi_{SB} \) as a function of back-gate voltage.
The n-type conductance of a MoTe$_2$ transistor is stable in vacuum. The device is kept in probe station in $2 \times 10^{-5}$ mbar vacuum at RT for 12 h after heating. Then, the measurements of electric properties are conducted. As shown in Fig. 6a, the transfer characteristics are still in off-state at negative gate voltage and in on-state at positive gate voltage, demonstrating typical n-type transistor properties. Similar transformations are realized in the other two samples as shown in Additional file 1: Figure S5 (a) and (b). Furthermore, we anneal two samples at 523 K using a high-temperature chemical vapor deposition system for 2 h in Ar gas at 3 mbar vacuum. They both change from p-type to n-type as shown in Additional file 1: Figure S5 (c) and (d). Figure 6b shows the output characteristics of an n-type MoTe$_2$ transistor at different back-gate voltages, which is clearly nonlinear, especially at low biased voltage $V_{sd}$, different from that in Fig. 3b, indicating the existence of enhanced effective Schottky barrier height between MoTe$_2$ and Au electrode after being heated to remove absorbates. Figure 6c shows the temperature-dependent transfer characteristics of n-type multi-layered MoTe$_2$ transistor. As seen, when temperature decreases from 275 to 25 K, the on-current and off-current both decrease as shown in Fig. 6c, d. Arrhenius plot of the source-drain current $I_{sd}$ in Fig. 6e shows that thermal emission and tunneling current are still the main charge transport mechanism in n-type multi-layered MoTe$_2$ transistor. The effective Schottky barrier height thus obtained is smaller than 250 meV. Considering the work function of Au (5.2 eV) and MoTe$_2$ (4.1 eV), the effective Schottky barrier height for electron is as high as 1.1 eV in ideal condition. The difference may be from the Fermi level pinning effect in 2D materials [47]. We also find that the n-type multi-layered MoTe$_2$ transistor returns to p-type when it is exposed to air (see Additional file 1: Figure S6). Based on the above experiment data, we infer that n-type conductance is an intrinsic property for multi-layered MoTe$_2$ transistor. N-type conductance can be attributed to Te vacancy in MoTe$_2$ channel. It is confirmed by DFT calculation as shown in Fig. 7. Figure 7a shows the illustration of the diagram of Te vacancy in monolayer (ML) MoTe$_2$, and Fig. 7b...
shows the corresponding density of states (DOS). Compared with the DOS of MoTe$_2$ with perfect crystal structure, Te vacancy induces a defect state near the conduct band edge. Therefore, MoTe$_2$ transistor with Te vacancy demonstrates n-type conductance.

When the device is exposed to air, oxygen and water in air are absorbed on the device. It has been verified that the absorbates of oxygen and water can induce p-type doping in organic transistor and graphene-related layer material transistor [44, 48, 49]. It works by oxygen/water redox couple, in which the solved oxygen in water sets the condition for the redox reaction. This process will induce charge transfer between the oxygen/water redox couple and MoTe$_2$. Charge transfer direction depends on the work function (or chemical potential) difference. The work function of MoTe$_2$ is 4.1 eV, while that of oxygen/water redox couple is larger than 4.83 eV [48]. Figure 8 illustrates the energy diagram of the oxygen/water redox couple and MoTe$_2$. Due to the energy level difference, the electrons are injected from MoTe$_2$ to oxygen/water redox couple, resulting in hole doping of MoTe$_2$ in air.

Using the p-type and n-type MoTe$_2$ transistors, we explore the construction of a complementary inverter as illustrated in Fig. 9a. A supply voltage of $V_{DD}$ is applied to the source (or drain) of p-type transistors, while the source (or drain) of the n-type transistor is grounded. The inverter is measured in $8 \times 10^{-5}$ mbar vacuum in probe station. Figure 9b, c shows the transfer characteristics of p-type and n-type transistors from the inverter, respectively. Figure 9d shows the voltage transfer characteristics (VTC) curves of the inverter when $V_{DD}$ varies in the range of 1 to 5 V. The transition voltage is located very near to $V_{DD}/2$, which can be attributed to the symmetry between n- and p-type MoTe$_2$ transistors. Figure 9e shows the VTC curves (black lines) and their mirrors (red lines) at $V_{DD} = 5$ V. The shaded “eye” area represents the noise margin of the inverter. As seen, the low-level noise margin ($NM_L$) and high-level noise margin ($NM_H$) are 1.54 V and 1.77 V, respectively, at $V_{DD} = 5$ V. Figure 9f shows $V_{IN}$-dependent voltage gains of the inverter at $V_{DD} = 2$ V, 3 V, 4 V, and 5 V which increases with $V_{DD}$ and reaches 9 at $V_{DD} = 5$ V.

**Conclusions**

In summary, we have fabricated a p-type multi-layered MoTe$_2$ transistor by transferring MoTe$_2$ onto fabricated source-drain electrode in air. Vacuum- and temperature-dependent in situ charge transport measurements demonstrate that the usual p-type conductance of multi-layered MoTe$_2$ transistor is not its intrinsic properties, which is caused by oxygen/water redox couple doping in air. When the MoTe$_2$ transistor is heated in vacuum to remove absorbates, it exhibits n-type conductance, which is attributed to tellurium vacancies in MoTe$_2$ and is its intrinsic transport property. Both p-type and n-type MoTe$_2$ transistors show smaller effective Schottky barrier height, which is partially due to the modification by absorbates. The lowered effective Schottky barrier is beneficial to achieving a high-performance MoTe$_2$ transistor. Based on
these findings, we fabricate a complementary inverter with gain values as high as 9.

**Methods/Experimental**

In order to research the influence of adsorbates on charge transport properties of multi-layered MoTe$_2$ transistor, we choose back-gated multi-layered MoTe$_2$ transistors and the whole MoTe$_2$ sample is exposed to the surroundings. Back-gated multi-layered MoTe$_2$ transistors are fabricated as follows. First, source, drain, and gate electrodes are patterned on 300-nm SiO$_2$/p$^+$-Si substrate using standard UV photolithography techniques, followed by selective etching of 300-nm SiO$_2$ beneath the gate electrode and E-beam evaporation of a 5-nm/100-nm Cr/Au film. Second, multi-layered MoTe$_2$ samples are prepared on other 300-nm SiO$_2$/p$^+$-Si by mechanical exfoliation of millimeter-size semiconducting 2H-MoTe$_2$ single crystals, which are grown by chemical vapor transport using TeCl$_4$ as the transport agent in a temperature gradient of 750 to 700°C for 3 days. Finally, the prepared multi-layered MoTe$_2$ samples are transferred onto patterned source-drain electrode using polyvinyl alcohol (PVA) as medium [50]. PVA is dissolved in H$_2$O and rinsed with isopropyl alcohol (IPA). Device annealing is carried out in a chemical vapor deposition setup with dry pump. Multi-layered MoTe$_2$ samples are identified by an optical microscope, and the corresponding thickness is characterized using SPA-300HV atomic force microscopy (AFM). Raman signals are collected by a LabRAM HR Raman spectrometer with 514-nm wavelength laser excitation in the backscattering configuration using a ×100 objective. The laser power measured from the objective is 2.2 mW. Electrical characterization is performed using a combination of Agilent B1500A semiconductor analyzer with Lakeshore probe station.

The DFT calculations are performed with the projector-augmented wave (PAW) pseudopotential and plane-wave basis set with a cut-off energy of 400 eV implemented in the Vienna ab initio simulation package (VASP) [51]. A vacuum space above 15 Å is chosen in order to eliminate the spurious interaction between periodic images. Enough $k$-point sampling of 12 × 12 × 1 and 24 × 24 × 1 are used for the structure relaxation and electronic calculations, respectively. The generalized gradient approximation (GGA) with Perew-Burke-Ernzerhof (PBE) functional is adopted [52].

**Additional file**

**Additional file 1:** Figure S1. Transfer characteristics of replicate measurements. **Figure S2.** (a)-(d) show the transfer characteristics of other four multi-layered MoTe$_2$ transistors in air, respectively. **Figure S3.** MoTe$_2$ transistor with different thicknesses. (a)–(d) show the optical image, AFM image, height profile, and transfer characteristics of the device with 5-nm thickness, respectively. (e)–(h) show the optical image, AFM image, height profile, and transfer characteristics of the device with 38-nm thickness, respectively. (i)–(l) show the optical image, AFM image, height profile, and transfer characteristics of the device with 85-nm thickness, respectively. **Figure S4.** Hysteresis behavior of transfer characteristics of multi-layered MoTe$_2$ transistor. **Figure S5.** (a)-(d) show the transfer
characteristics of four multi-layered MoTe₂ transistors, respectively. The black line represents the transfer characteristics of as-prepared multi-layered MoTe₂ transistor in air, and the red line represents that measured from the annealed device. Figure S6. (a)-(c) show the transfer characteristics of three multi-layered MoTe₂ transistors at different conditions, respectively. (DOCX 1011 kb)

Abbreviation
2D: Two-dimensional; 2H-MoTe₂: 2H-type molybdenum ditelluride; AFM: Atomic force microscopy; DFT: Density functional theory; DOS: Density of states; FET: Field-effect transistor; GGA: Generalized gradient approximation;IPA: Isopropyl alcohol; Ids: Source-drain current; LED: Light-emitting diode; NIV: High-level noise margin; NIA: Low-level noise margin; PAW: Projector augmented wave; PBE: Perdew-Burke-Ernzerhof; PVA: Polyvinyl alcohol; SD: Source-drain; SSS: Subthreshold swing; TMDs: Transition metal dichalcogenides; VASP: Vienna ab initio simulation package; SB: Schottky barrier height

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Availability of Data and Materials
The datasets supporting the conclusions of this article are included within the article and its supporting information.

Authors’ Contributions
JL conceived the experiment. JL and LX designed the experiment, performed the measurements, and drafted the manuscript with the assistance of NG and YJ. XX fabricated the device with the assistance of QL. YW performed the DFT calculations. KZ grew 2H-MoTe₂ single crystals with the assistance of YW and JL. Authors discussed the results and approved the final manuscript.

Competing Interests
The authors declare that they have no competing interests.

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