A Low Noise 28Gbaud/s Linear PAM4 Receiver Front-End for Optical Communication Applications in 0.13μm BiCMOS Technology

Ming Li¹, Yingmei Chen²³*, Junpeng Hu¹ and Chao Guo²

¹School of Microelectronics, Southeast University, Nanjing, 210016, P. R. China
²School of Information Science and Engineering, Southeast University, Nanjing, 210016, P. R. China
³Purple Mountain Laboratories, Nanjing, 210016, P. R. China

*Corresponding author email: njcym@seu.edu.cn

Abstract. This paper presents a low noise 28 Gbaud/s linear receiver front-end for fourth-order pulse amplitude modulation (PAM4) signal applied in the field of optical communication. The designed receiver front-end includes a transimpedance amplifier (TIA), an automatic gain control (AGC) and a DC offset cancellation (DCOC) circuit. The pseudo-differential structure of the TIA is designed to achieve low noise. The resistance and capacitance degradation technology are introduced in the variable gain amplifier (VGA) and the equalizer (EQ) to improve linearity and optimize the bandwidth. In the AGC mode, the feedback loop controls the output amplitude to be a desired value within a large range of input current. The PAM4 optical receiver front-end achieves a maximum differential transimpedance gain of 76 dBΩ and -3dB bandwidth of 27 GHz. The equivalent input noise current density with the front-end circuit is 11.2 pA/√Hz. In 0.13μm BiCMOS technology, the PAM4 front-end chip consumes 200 mW with a 3.3V voltage supply.

Keywords: Fourth-order pulse amplitude modulation (PAM4); Transimpedance amplifier (TIA); Automatic gain control (AGC); Optical receiver front-end.

1. Introduction

In recent years, in order to adapt to the continuous improvement of the optical fiber communication rate, the technologies related to optical fiber communication have made revolutionary progress. The working rate of current practical optical receivers has reached as high as tens of Gb/s, and even hundreds of Gb/s [1-2]. The non-return-to-zero code (NRZ) transmission format is commonly adopted in short-range interconnected high-speed optical modules. In order to increase the high-speed interconnected network capacity and reduce the transmission cost per bit, the transmission rate can be increased by introducing PAM4 technology. At the same baud rate, the transmission rate of the PAM4 pattern signal is twice that of the NRZ, which can carry more information and has higher transmission efficiency. The work of this paper is mainly devoted to researching the design technology of the front-end amplifier circuit of the optical receiver in the next generation optical communication system. The optical receiver front-end determines the performance of the entire receiver, which has far-reaching significance for the development of the next generation of optical communication systems. The optical receiver has to employ PAM4 format receiver front-end with enough bandwidth according to the bit rate, high linearity and low noise [3-4].
This paper presents a 28Gbaud/s PAM4 linear optical receiver front-end with high linearity and low noise. It is organized as follows. Section II discusses the design details of the PAM4 optical receiver front-end circuits. Section III gives the simulation results of receiver front-end. In Section IV, conclusions are drawn in this paper.

2. Circuit Design

The block diagram of the PAM4 front-end circuit is shown in Fig.1. The TIA converts the current signal from the photodetector (PD) into voltage signal, then it is amplified by the VGA. The EQ broadens the bandwidth and outputs the signal to the latter buffer. The AGC loop is mainly composed of a VGA, a peak detection circuit and an error amplifier. The peak detection circuit generates a comparison signal by detecting the peak value of the buffer and an external reference voltage. And the comparison signal is used as the gain control terminal to the VGA.

In the AGC mode, the gain of the VGA is controlled by the feedback loop. The AGC loop detects the output amplitude from the buffer and gets the corresponding control voltage, which sets the gain of the VGA accordingly, maintaining a constant output amplitude within a large range of input current. The advantage of the analog control loop is that the output amplitude can be controlled to a desired value by changing MC pin.

2.1. Transimpedance Amplifier (TIA)

The schematic of the TIA is proposed in Fig. 2, $I_{PD}$ and $C_{PD}$ constitute the equivalent circuit of PD, which provide the input signal for TIA. In this case, the basic structure of the open loop amplifier is a common emitter amplifier with emitter degradation resistance followed by an emitter follower[5-6]. And the feedback resistor $R_f$ is connected across the input and output to form shunt-feedback.

The output of the TIA is taken from the emitter of Q2, instead of the collector of Q1, because the driving impedance at the output of the emitter follower Q2 is smaller than the driving impedance at the collector of Q1. The disadvantage, however, is providing less headroom to accommodate the tail current sources of VGA. And the excessive output swing at the output of TIA will make the design of the VGA harder in terms of linearity with large input current. In order to solve the issue, a switch is added to realize gain changing-over. As shown in Figure 2. When the input current exceeds a fixed value, M1 is on and the circuit is automatically switched to a small gain. And the gain switching is controlled by the control terminal VA. That is, VA is obtained by comparing the voltage $V_{in}$ converted from the input current $I_{in}$ (as shown in Figure 3) with an external reference voltage $V_{ref}$ through a comparator.

The pseudo-differential structure is applied in TIA stage since the PD current is a single-ended input, while the subsequent VGA is a dual-port one. That is, TIA stage is the structure that single-ended input and double-ended output[7]. And the other input is floating. In this case, the structure of the input side and the floating side is symmetrical, which all adopt the shunt-feedback structure.
Due to the pseudo-differential structure TIA, the DC input current will cause deviation of the output DC points. In order to solve the problem, the DCOC circuit is added to make sure that the DC component in the input signal are subtracted. As shown in the Fig. 4, DCOC is formed by M1 and operational amplifier. The DC value at the output of two low-pass filters is compared by operational amplifier. Then the difference signal from low-pass filters sets the gate voltage of M1, accordingly.

The total noise figure of the optical receiver system is mainly determined by the noise figure of the previous stage circuit, so the optimization of the system noise performance is mainly concentrated in TIA stage.

To analyze the trade-off relationship between various parameters of noise optimization, the noise sources of TIA has been marked in the Fig.5. The input noise current density \( i_{eq} \) will be given by

\[
\overline{i^2_{eq} = i^2_{amp} + \frac{v^2_{amp}}{R_f^2} + i^2_{Rf} + i^2_{MOS}}
\]

In this case, \( \overline{i^2_{amp}} \) and \( \overline{v^2_{amp}} \) are the input noise current density and the input noise voltage density of the open-loop voltage amplifier, respectively.

\[
\overline{i^2_{amp}} = 2q \left(I_B + \frac{I_C}{|\beta|}\right)^2
\]

\[
\overline{v^2_{amp}} = 4kT \left(r_h + \frac{1}{2kTQ}\right)
\]

\[
\overline{i^2_{Rf}} = \frac{4kT}{R_f}
\]

\( \overline{i^2_{MOS}} \) is the thermal channel noise of the MOS transistor M1.

\[
\overline{i^2_{MOS}} = 4kT \gamma \gamma_{m,M1}
\]
\( i_{eq}^2 = 2q \left( I_{b} + \frac{I_C}{\left| \beta \right|^2} \right) + \frac{4kT}{R_f} \left( r_b^+ + \frac{l}{2g_{m,Q1}} \right) + \frac{4kT}{g_{m,M1}} + 4kT R_f + 4kT R \) ...

(6)

First, the noise of the base current and the collector current referred to the input are small, therefore their contribution to noise is negligible. Second, the noise of the base resistance \( r_b \) and the transistor Q1 referred to the input is inversely proportional to the square of the feedback resistance \( R_f \). And the noise contribution from the feedback resistor is inversely proportional to \( R_f \).

To reduce the equivalent input noise, the value of \( R_f \) has to be maximized within the allowable bandwidth. Simultaneously, an important reason for adopting the pseudo-differential TIA is that the input-referred noise current of the pseudo-differential TIA is approximately equal to the input-referred noise current of the single-ended TIA. Therefore, the noise of the receiver front-end referred to the input is \( i_{eq}^2 \), which achieves good noise performance. And the gain of the TIA stage will increase, but the bandwidth of the TIA stage will decrease rapidly. Then we extend the bandwidth of the circuit through the VGA and the EQ afterwards to achieve the required high rate.

2.2. VGA, Equalizer and Output Buffer

The VGA basing on the Gilbert structure is proposed in Fig.6. The gain is related to the voltage difference \( V_{ctrlA} - V_{ctrlB} \) that determine the different current flowing through Q1 (Q4) and Q2 (Q3). The emitter degeneration resistor \( R_e \) is utilized to improve the linearity, which reduces the influence of nonlinear parameter \( g_m \). And the emitter degeneration capacitance \( C_e \) is added to reduce emitter degradation impedance of high frequency, which expand bandwidth. Q5 and Q6 construct emitter-followers, which play the role of buffering and level shifting.

![Figure 6. Schematic of VGA.](image1)

![Figure 7. Schematic of EQ.](image2)

The equalization circuit with negative Miller capacitor technology is shown in Figure 7. The negative Miller capacitor \( C_1 \) is to provide a negative capacitor for the pre-load, which slow down the attenuation of high-frequency and achieve high rates. Since the input signal is a 4-level signal and requires high linearity, the emitter degradation resistor \( R_e \) is added to improve the eye diagram and reduce jitter.

2.3. AGC Loop

Fig. 1 shows the block diagram of the AGC loop. Q1, Q2, C1 and \( I_{ss} \) form a peak detection circuit. According to the corresponding input signal, Q1 and Q2 are turned on in turn to detect the \( V_P \) that is the peak value of the detected output signal of the automatic control stage. C1 has the function of stably detecting the peak value and filtering it. The other output signal \( V_{ref} \) is a reference voltage generated internally, which corresponds to the output amplitude index.

The output signal \( V_P \), that is, half of the signal swing is added to the DC level. Similarly, \( V_{ref} \) is that the DC level of node B plus the half of ideal output swing. And the added signal is determined by the reference current \( I_{ref} \) and the resistance \( R_3 \). Therefore, as mentioned above, the peak detector changes \( I_{ref} \) by controlling the value of MC to obtain different output swing.
The error amplifier is added to compare the peak value $V_p$ with the reference voltage $V_{ref}$, which controls the charge and discharge of the capacitor $C_e$ to obtain the control voltage $V_{ctrl}$. Then the gain of VGA can be adjusted automatically by the AGC loop within a large input current range.

### 3. Simulation Results

The proposed PAM4 optical receiver front-end circuit is designed in 0.13µm SiGe BiCMOS technology, which layout is shown in Figure 10. The layout area, including the bonding pads, is only 900µm*1200µm. The AC simulation result including bonding pad and ESD cell is shown in Figure 11. It can be seen that the front-end circuit achieves a maximum transimpedance gain of 76 dBΩ and a -3dB bandwidth of 27 GHz. The equivalent input noise current density $i_{eq}$ is only 11.2 pA/√Hz.

To test the function of the AGC loop, the front-end amplifier can be set in the AGC mode and the MC was fixed at 2.5V. The analog control loop is to ensure that the output amplitude can be controlled at 400mVpp within a large range of input current. Fig.12 shows the AC simulation results of VGA. The minimum and maximum gain of VGA is -4dB and 18dB, respectively. The VGA has a dynamic range of 22dB and a bandwidth larger than 25GHz.

Fig.13 shows the PAM4 format eye diagrams output at the minimum 40µA input current and maximum 1.1mA input current. For 400mVpp differential output swing, the total harmonica distortion (THD) is less than 3%.

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**Figure 8.** Schematic of the peak detector.
**Figure 9.** Schematic of the error amplifier.

**Figure 10.** Layout of the optical receiver front-end circuit.

**Figure 11.** AC results of the receiver front-end.

**Figure 12.** Simulated VGA gain versus VCTRL.
Figure 13. a. Eye diagram at minimum input current of 40µA. b. Eye diagram at maximum input current of 1.1mA

4. Conclusion
A 28 Gbaud/s PAM4 linear optical receiver front-end with AGC function is presented. By the common emitter and the pseudo-differential structure of TIA stage, it achieves low noise. And the THD is controlled within 3% by negative Miller capacitor, resistance and capacitance degradation technology, showing good linearity. The overall performance validate feasibility of the front-end for low noise, high linearity and high-data rate optical receivers.

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