Performance analysis of undoped cylindrical gate all around (GAA) MOSFET at subthreshold regime

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Abstract
In this work the sensitivity of process parameters like channel length ($L$), channel thickness ($t_{Si}$), and gate work function ($\phi_M$) on various performance metrics of an undoped cylindrical gate all around (GAA) metal-oxide-semiconductor field effect transistor (MOSFET) are systematically analyzed. Undoped GAA MOSFET is a radical invention as it introduces a new direction for transistor scaling. In conventional MOSFET, generally the channel doping concentration is very high to provide high on-state current, but in contrary it causes random dopant fluctuation and threshold voltage variation. So, the undoped nature of GAA MOSFET solves the above complications. Hence, we have analyzed the electrical characteristics as well as the analog/RF performances of undoped GAA MOSFET through Sentaurus device simulator.

Keywords: cylindrical MOSFET, gate all around (GAA), electrical parameters, analog/RF

Classification numbers: 3.02, 6.01

1. Introduction

To achieve low cost, high operational speed and better performance, the dimensions of conventional transistors need to be downscaled to the sub-nanometer region. The reduction of metal-oxide-semiconductor field effect transistor (MOSFET) dimensions will degrade the gate control over the channel due to close proximity between source and drain. This leads to increase various short channel effects (SCEs) such as hot carrier effect, threshold voltage roll-off, and substrate bias effect [1, 2]. Many new devices have been introduced beyond Moore’s era [3–5] to suppress the SCEs and enable further scaling down of the device. Similarly, a number of multi-gate silicon on insulator (SOI) technologies have also been proposed to replace the conventional MOSFET [6, 7]. However, the cylindrical gate all around (GAA) MOSFET is one of the novel devices which further enables scaling without hindering the device performance. Because of the low characteristic length and higher drive current, GAA MOSFETs can achieve higher packing density as compared to double gate (DG) MOSFETs [8–10]. Also GAA MOSFET has excellent electrostatic control of the channel, robustness against SCEs, better scaling options, no floating body effect, larger equivalent number of gates, and ideal subthreshold swing as compared to other multiple gate MOSFETs. Hence, the GAA MOSFET is a promising solution for nanoscale technology complementary metal–oxide–semiconductor (CMOS) devices [11–15]. Recently, MOS devices with sub-50 nm channel length demonstrate more than 100 GHz of cut-off frequency [16–18]. Important device parameters such as threshold voltage ($V_{th}$), on-off ratio ($I_{on}/I_{off}$), and cut-off frequency ($f_T$) are very much sensitive to the device geometry such as channel length ($L$), channel thickness ($t_{Si}$), and gate work function ($\phi_M$). In this work an attempt was taken to present a detailed analysis of the performance dependency of GAA MOSFET on device geometry variation.

In this paper, different performance metrics like drain current ($I_D$), transconductance ($g_m$), total gate capacitance...
(C_{gg}) and cut-off frequency \((f_{T})\) are systematically presented with the variation of \(L_g\), \(\phi_M\), and \(t_{Si}\). Along with the introduction, section 2 describes the device structure description that includes all the dimensions, materials and doping concentrations of GAA MOSFET. This section also analyses the physics of the device using device numerical simulations and models activated for simulation. Section 3 comprises all results and discussion. Finally, the concluding remarks are presented in section 4.

2. Device structure and simulation setup

The schematic diagram of the fully depleted cylindrical GAA MOSFET structure used for modeling and simulation is shown in Figure 1. The radial and lateral directions of the channel are assumed to be along the radius and the z-axis of the cylinder as shown in Figure 1. The source and drain of the device are uniformly doped with doping concentration of \(N_D = 1 \times 10^{20} \text{cm}^{-3}\). The channel is kept undoped. The gate oxide thickness is \(t_{ox} = 1.1 \text{nm}\).

The simulation is carried out by the device simulator Sentaurus, a 3D numerical simulator from Synopsis Inc. [19]. To obtain accurate results for MOSFET simulation we need to account for the mobility degradation that occurs inside inversion layers. The drift-diffusion model is the default carrier transport model in Sentaurus device is activated. For the drift-diffusion model, the current densities for electrons and holes are given by

\[
\mathbf{J}_e = \mu_n \left( n V_{EC} - 1.5 (n/kT) \ln m_n \right) + D_n \left( \nabla n - n \nabla \ln \gamma_n \right),
\]

\[
\mathbf{J}_p = \mu_p \left( \rho V_{EV} + 1.5 (p/kT) \ln m_p \right) - D_p \left( \nabla p - p \nabla \ln \gamma_p \right),
\]

where \(\mathbf{J}_e\) and \(\mathbf{J}_p\) are electron and hole current density, \(\mu_n\) and \(\mu_p\) represent electron and hole mobility, \(n\) and \(p\) describe electron and hole density, \(\gamma_n\) and \(\gamma_p\) are Fermi statistics constants, and \(m_n\) and \(m_p\) present spatial effective masses of electron and hole, respectively. \(T\) and \(k\) describe temperature and Boltzmann constant. \(E_{C}\) and \(E_{V}\) are conduction and valance energy bands. \(D_n\) and \(D_p\) represent the diffusion constants for electron and holes respectively.

The first term takes into account the contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the band gap [20, 21]. The remaining terms take into account the contribution due to the gradient of concentration, and the spatial variation of the effective masses \(m_n\) and \(m_p\). All other terms used have their commonplace meanings. In the simulation, basic mobility model is used that takes into account the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The silicon band gap narrowing model that determines the intrinsic carrier concentration is activated.

3. Results and discussion

In order to analyse the impact of channel length \(L_g\), and channel thickness \(t_{Si}\), and gate work function \(\phi_M\) on the device performance, the simulation is carried out by varying the above parameters. Figures 2(a) and (b) show the drain current \(I_D\) in log scale as a function of gate to source voltage \(V_{GS}\) for different \(L_g\) and \(t_{Si}\), respectively. The GAA MOSFETs are showing a significant low leakage current in the range of \(10^{-12}\) to \(10^{-14} \mu\text{A}\) for all cases. In Figure 2(a), \(L_g\) varies from 28 to 70 nm and we can observe from the figure that a decrease in \(L_g\) results a shift in the characteristics. The off-state current \(I_{off}\) is also prominent for \(L_g\) decreases to below 30 nm with comparison to others. In the short channel device the \(I_{off}\) increases due to random motion of charge carriers. As channel length decreases, it gives rise to high drain current because of the relation \(I_D \propto 1/L\). However, from the log scale, the leakage current is also prominent for lower channel lengths. Figure 2(b) reveals the \(I_D\) dependency on silicon body thickness of the GAA MOSFET. The characteristic of \(I_{off}\) is also influenced by \(t_{Si}\), which is cleared from figure 2(b). As the silicon film gets thinner, there is a significant improvement in leakage current because no further leakage path is available far from the gate.

Figure 3(a) represents the \(I_D-V_{GS}\) characteristic for different values of metal gate work function \(\phi_M\). The work function is varied from 4.6 eV to 5.1 eV for \(V_{DS} = 50 \text{mV}\) (sub-threshold region of operation). The results illustrate that the off-state leakage current (subthreshold performance) of the device improves for higher values of metal gate work function. This is because the higher \(\phi_M\) consequently depicts higher threshold voltage, which further reduces the off-state leakage current and improves the subthreshold behavior of the device. Figure 3(b) shows the intrinsic capacitances (gate to gate capacitance \(C_{gg}\)) as a function of \(I_D\) for subthreshold or weak inversion with variation in channel length. As shown in figure, the intrinsic capacitance increases with increase in \(I_D\). This is because of the increase in the fringing field lines emanating from the gate edges. The device with \(L_g = 28\ \text{nm}\) shows low value for \(C_{gg}\) and as \(L_g\) increases the \(C_{gg}\) also starts increasing and obtains its maximum at \(L_g = 70\ \text{nm}\). Hence, in the case of \(L_g = 28\ \text{nm}\), the intrinsic capacitance value is smallest, which in turn leads to high cutoff frequency.

Transconductance \((g_{m})\) and cut off frequency \((f_{T})\) as a function of \(I_D\) are present in figures 4(a) and (b),...
respectively. From the figure, it is clear that as the channel length decreases the $g_m$ value is increasing because of high drain current. The high $g_m$ will further enhance the trans-conductance generation factor (TGF = $g_m/I_D$) which is the requirement for realization of circuits operating at low supply voltage. From figure 4(b), the variations of cut off frequency ($f_T = g_m/2\pi C_{gg}$) can be observed with respect to $V_{GS}$ for different $L_g$. Here, the value of $f_T$ obtained for the device having low channel length is higher, and gradually decreases as the channel length increases. $f_T$ is inversely proportional to the intrinsic capacitance ($C_{gg}$). So, the $f_T$ value is low due to high capacitance values for higher channel length devices, as discussed in figure 3(b).

All the extracted and calculated values of dc as well as analog/RF performances are tabulated in tables 1–3 with the variation of silicon body thickness ($t_{Si}$), gate work function ($\phi_M$), and channel length ($L_g$) of the GAA MOSFET respectively. Table 1 compares and analyses the sensitivity of
\begin{table}[h]
\centering
\begin{tabular}{lcccc}
\hline
$L_{\text{Si}}$ (nm) & $I_{\text{on}}$ ($\mu$A) & $I_{\text{off}}$ (pA) & $V_{\text{th}}$ (V) \\
\hline
5 & 1.21 & 0.11 & 0.419 \\
10 & 3.99 & 1.27 & 0.405 \\
15 & 8.31 & 7.27 & 0.4 \\
20 & 11.4 & 9.7 & 0.387 \\
\hline
\end{tabular}
\caption{DC performance measures with $L_{\text{Si}}$ variation.}
\end{table}

\begin{table}[h]
\centering
\begin{tabular}{lcccc}
\hline
$\phi_M$ (eV) & $I_{\text{on}}$ (A) & $I_{\text{off}}$ (A) & $V_{\text{th}}$ (V) \\
\hline
4.6 & $3.68 \times 10^{-6}$ & $2.44 \times 10^{-12}$ & 0.382 \\
4.8 & $1.82 \times 10^{-6}$ & $3.99 \times 10^{-15}$ & 0.587 \\
4.9 & $3.91 \times 10^{-7}$ & $1.58 \times 10^{-16}$ & 0.639 \\
5.1 & $1.32 \times 10^{-9}$ & $2.45 \times 10^{-19}$ & — \\
\hline
\end{tabular}
\caption{DC performance analysis with $\phi_M$ variation.}
\end{table}

\begin{table}[h]
\centering
\begin{tabular}{lcccc}
\hline
$L_{\text{Si}}$ (nm) & $I_{\text{off}}$ (A) & $g_m$ (max) $(\mu$S) & $C_{gg}$ (max) $\times 10^{12}$ (F) & $f_T$ (max) (GHz) \\
\hline
28 & $2.44 \times 10^{-12}$ & 16.1 & 1.73 & 222 \\
40 & $1.14 \times 10^{-13}$ & 17.6 & 2.51 & 172 \\
55 & $3.86 \times 10^{-14}$ & 16.4 & 3.47 & 116 \\
70 & $2.48 \times 10^{-14}$ & 15.2 & 4.4 & 83.6 \\
\hline
\end{tabular}
\caption{Analysis of different parameters with $L_{\text{Si}}$ variation.}
\end{table}

$t_{\text{Si}}$ on various important parameters such as $I_{\text{on}}$, $I_{\text{off}}$, and $V_{\text{th}}$. We can effectively control the $V_{\text{th}}$ and SCEs such as off-state leakage current by reducing $t_{\text{Si}}$ with a little compromise in on-state current. Hence, people always prefer ultra-thin body (UTB) fully depleted (FD) SOI MOSFET as the body is completely controlled by the gate and there is no leakage path far from the gate. The percentage of improvement in $I_{\text{off}}$ is 82.53% and 91.33%, while $t_{\text{Si}}$ varies from 15 nm to 10 nm and 10 nm to 5 nm, respectively.

Table 2 reports the similar parameters (as in table 1) but with variation in gate work function ($\phi_M$) for gate length $L_{\text{Si}} = 28$ nm. The $\phi_M$ is one of the main controlling parameters threshold voltage. As we can measure from the table, $V_{\text{th}}$ is increasing with increase in $\phi_M$, which further controls the subthreshold leakage current. While $\phi_M$ changes from 4.6 eV to 4.9 eV, a significant improvement in $I_{\text{off}}$ consequently in SCEs can be observed.

Table 3 summarizes the analog/RF figures of merit (FOMs) for different values of channel lengths. It is clear from the table that, while the gate length is reduced, the RF FOM $f_T$ is increased because of high drain current which results in higher $g_m$ values for shorter gate length devices.

4. Conclusion

A cylindrical gate all around (GAA) MOSFET is explored and the performance evaluation is carried out with extensive device simulation by Sentaurus simulator. The sensitivity of device parameters like $t_{\text{Si}}$, $\phi_M$, and $L_{\text{Si}}$ on various dc and analog/RF FOMs are systematically presented. From our results, by considering an ultra-thin body (UTB) and little higher gate work function can enhance the device performance with well suppressed SCEs. The subthreshold leakage current can be significantly improved for lower $t_{\text{Si}}$ and higher $\phi_M$ values. Similarly, continuous miniaturization of $L_{\text{Si}}$ is required for obtaining high $I_{\text{on}}$, $g_m$, and $f_T$. Hence, an appropriate selection of the silicon thickness, and metal gate work function give rise to an optimum threshold voltage at a given channel length and drain bias.

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