Recent Progress with bioSFQ Circuit Family for Neuromorphic Computing

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Abstract—Superconductor single flux quantum (SFQ) technology is attractive for neuromorphic computing due to low energy dissipation and high, potentially up to 100 GHz, clock rates. We have recently suggested a new family of bioSFQ circuits (V. K. Semenov et al., IEEE TAS, vol. 32, no. 4, 1400105, 2022) where information is stored as a value of current in a superconducting loop and transferred as a rate of SFQ pulses propagating between the loops. This approach, in the simplest case dealing with positive numbers, requires single-line transfer channels. In the more general case of bipolar numbers, it requires dual-rail transfer channels. For this need, a new comparator with dual-rail output has been developed and is presented. This comparator is an essential part of a bipolar multiplier that has also been designed, fabricated, and tested. We discuss strategic advantages of the suggested bioSFQ approach, e.g., an inherently asynchronous character of bioSFQ cells which do not require explicit clock signals. As a result, bioSFQ circuits are free of racing errors and tolerant to occasional collision of propagating SFQ pulses. This tolerance is due to stochastic nature of data signals generated by comparators operating within their gray zone. The circuits were fabricated in the eight-niobium-layer fabrication process SFQ5ee developed for superconductor electronics at MIT Lincoln Laboratory.

Index Terms—artificial neural networks, bipolar multiplier, electronic circuits, neuromorphic computing, superconductor electronics, superconducting integrated circuits, SFQ, RSFQ.

I. INTRODUCTION

This paper is devoted to the development of the family of bioSFQ logic/memory cells proposed in [1] where we presented our basic ideas and the first experimental demonstrations. Here we limit ourselves to the recent advances and intentionally avoid traditional introductory notes, which can be found in [1]. However, we will more accurately define the ultimate goal and boundaries of the proposed bioSFQ technique.

For more than 30 years, superconductor single flux quantum (SFQ) electronics has been bounded by a widely accepted RSFQ approach [2], despite the existence of some applications

Fig. 1. Block diagram (a) and layout (b) of the analog multiplier.
for which RSFQ is not a particularly suitable technology. For instance, from the very beginning, it has been known that “a universal von-Neumann-type computer is probably the worst device for implementation using the RSFQ … technology” [2]. The technology has survived due to impressive progress in other applications heavily using fast ADC and DAC converters. However, there was always a hope that RSFQ technology is just waiting for inherently matched applications. These days it becomes more evident for us that neuromorphic computing could be such a long-awaited application. Our belief is supported by appearance of a number of recent proposals of neuromorphic devices containing borrowed RSFQ components.

Currently, artificial intelligence (AI) and, in particular, deep learning algorithms run on conventional purely digital computers. However, there is a general belief that special, not-yet-invented, computing devices could be much more efficient for AI applications. Carver Mead explained his belief in the following way: “For … problems, … in which the input data are ill-conditioned and the computation can be specified in a relative manner, biological solutions are many orders of magnitude more effective than those we have been able to implement using digital methods” [3]. More exactly he believed that: “Large-scale adaptive analog systems are more robust to component degradation and failure than are more conventional systems, and they use far less power” [3].

To follow these recommendations, we supplemented purely digital RSFQ devices by a number of analog devices. We named the combination as bioSFQ logic/memory cells [1].

II. ANALOG MULTIPLIER

An analog multiplier was suggested in [1]. The block diagram of the present version of the multiplier, shown in Fig. 1, has a few wiring differences from its original block diagram presented in [1, Fig. 4a]. However, some of its components, including the comparator with complementary outputs, have been significantly revised. As a result, its dimensions have been shrunken to 120 µm x 120 µm.

A. Comparator With Complementary Outputs

A nondestructive comparator [1, Fig. 1] is the key component of the unipolar bioSFQ cell family. An inverter cell was used in [1] along with the comparator to convert the composite circuit into a more desired bipolar mode of operation. Here we present a more compact and advanced solution for a comparator with the dual-rail output.

A new comparator (Fig. 2) consists of a conventional Josephson Comparator (junctions J1, J3 and J4), an Amplifier (junctions J5 and J6), and a highly Asymmetric Comparator (junctions J7 and J8). An analog signal is applied via a magnetic coupling with inductor L2. We will discuss coupling details later; for numerical simulations the corresponding circuitry was represented by an ideal phase source P0. Correct operation of our cell requires optimization of the dimensionless McCumber parameter $\beta_C$ of the individual junctions. This differs from the common practice of using Josephson junctions with identical $\beta_C$ values. Numerical values of the optimized $\beta_C$ are shown in Fig. 2 caption as the second property of the junctions. Parameters $\beta_C$ were adjusted by selecting the proper resistive shunts. Evidently this procedure changes values of the $I_c R_n$ products, i.e., the characteristic voltages $V_C$ of the junctions. We omitted numerical values of the characteristic voltages because they could be extracted from the given McCumber parameters $V_C = (\beta_C I_c \Phi_0 / 2\pi C_s)^{1/2}$, where $C_s = 70$ pF/µm² is the junction specific capacitance. We preserved the same notation of the circuit shown in Fig. 2a as was suggested in [1].

During the simulation shown in the upper trace in Fig. 2c, the phase of the input magnetic signal applied via P0 slowly grows from about −0.2 to 0.2 (in PSCAN units of 2π). At the same time interval, we applied to terminal T a sequence of five SFQ
pulses shown by the black trace in the second frame from the top in Fig. 2c. As expected, at negative input signal, the circuit responds by producing three SFQ pulses, marked JN, on the complementary terminal NQ. Alternatively, at positive input signal, the circuit responds by producing two SFQ pulses, marked JP, on terminal Q. The presented voltage traces show voltage drops on external junctions adjacent to the input and output terminals. The traces shown in the panel marked “2π Phase Jumps,” right below the discussed voltage traces, illustrate the dynamics of internal Josephson junctions. Crudely it could be described as two independent sequences of 2π-phase leaps on some Josephson junctions. At negative value of the signal, the sequence is quite straightforward. The switching of the upper (J4) junction of the comparator (J3, J4) indicates that the signal is negative. The pulse propagates via junctions J6 and J7 to the output terminal NQ. At positive signal, the lower junction (J3) of the comparator converts this signal to the SFQ pulse and junction J5 passes this pulse to the terminal Q. Junction J8 prevents the propagation of “positive” pulses to the terminal NQ.

The implemented “isolation” technique is rarely, or perhaps never, used in SFQ circuits. At first glance, it is difficult to imagine how junction J8 distinguishes or discriminates SFQ pulses generated by junctions J5 and J6. Such discrimination is possible if, for example, junctions J5 and J8 have much lower βC than junction J7 and the critical current of J8 is lower than that of J7. In this case, J8 is insensitive to short SFQ pulses generated by J6. At the same time, it easily responds to much wider pulses generated by J5. Two bottom traces in Fig. 2c show currents via J7 and J8, and illustrate the presented technique. At negative signal (left side of the traces) the short pulses activate J7, while wide pulses (right side) slowly increase the bias of J8 over its critical value and hold it until the junction phase completes its 2π leap.

B. Input Transformer of the Comparator

As we mentioned in [1], we need different comparators for copying analog currents and for more complex arithmetic operations with such currents. In the first case, the gray zone of the comparator should be as narrow as possible. This is a conventional requirement, and has been addressed in a number of publications, see, for example [4], [5]. In the second case, the gray zone should be stretched to the whole range of allowed current variations. To achieve this goal, we shunt the transformer, shown in Fig. 4 by a blue meandering trace overlapping the orange horizontal traces, by an inductor seen in Fig. 4 as a blue vertical r1-shape.

III. Fabrication and Measurements

The comparator and multiplier circuits were fabricated in the eight-niobium-layer fabrication process SFQ5ee [6] with the Josephson critical current density of 100 µA/µm² and minimum linewidth of 0.25 µm, developed for superconductor electronics at MIT Lincoln Laboratory. The circuits were tested in a low-speed liquid helium dunk probe using an Octopux [7].
The basic functionality of a single comparator with a complementary output can be seen in Fig. 5. A stream of SFQ pulses with approximately 30 GHz rate, corresponding to a time-averaged input of approximately 60 µV, is generated at the input designated T in Fig. 2b. The stream of pulses is routed to one of the two outputs depending on the amplitude of the current coupled into the inductor L2. The transition between the two outputs takes the shape of an error function, \( \text{erf} \) characteristic of the gray zone of the comparator formed by J3-J4.

The functionality of the analog multiplier, composed of three comparator-based circuits, can be seen in Fig. 6. The circuit performs an analog multiplication of control current \( X \) (see Fig. 1a) and control current \( Y \), and the resulting product is encoded as the output voltage. More precisely, this operation corresponds to the product of the two error functions. A few different values of \( Y \) are supplied to the circuit, corresponding to differently colored traces in Fig. 6, while the value of \( X \) is continuously swept. (Some noticeable asymmetries and offsets are likely due to measurement artifacts.)

The circuit performs an \( X^2 \) function (see Fig. 7) at equal values of \( X \) and \( Y \). The required synchronization of control currents can be achieved by the connection of the control lines in series.

### IV. Discussion

The demonstrated analog multiplier is the key building block for several other analog arithmetic devices. In the previous section we explained how to use the multiplier to execute the second power of the input current. In the previous paper [1], we explained that a sensitive comparator can be used in a feedback loop to reduce a mismatch of two currents or, in other words, to enable the copying of currents; see [1, Fig. 3]. A similar approach can be used, for example, to execute a square root function. This can be achieved if we compare the input current with the result of \( X^2 \) operation and apply the feedback signal to the third current. The numerical value of this third current will be equal to \( \sqrt{X} \) after the mismatch is eliminated. Similarly, we can apply the feedback signals to, say, the multiplicand \( Y \) while we hold the values of the product \( Z \) and the second multiplicand \( X \).

In this case we obtain a division operation: \( Y = Z/X \). Other simple fractions, e.g., \( \sin(x) \) and \( \cos(x) \), can also be easily executed using the proposed approach.

According to Mead [3], neuromorphic applications are much more tolerant to error rate than conventional digital applications. We think that 0.1% and in some cases 1% error rate could be quite satisfactory. In practical terms, it means that critical currents of junctions in bioSFQ cells could be safely reduced from 0.1 mA to, say, 0.02 mA. This task could be easily executed. However, the scaling of critical currents requires inversely proportional increase of all cell inductances. This task could be quite challenging with the fabrication process using Nb wiring because this requires a greatly increased length of inductors. Fortunately, a novel fabrication technology with bilayers of kinetic and geometrical inductors, NbN/Nb bilayers, has been developed and presented at the ASC 2022 [8].

### V. Conclusion

In conclusion, we have demonstrated examples of neuromorphic circuits based on the bioSFQ circuitry proposed in [1] and an analog bipolar multiplier demonstrated in this work. The results show that we are quite close to implementing a wide range of analog functions, using the proposed circuitry.

The desired functionality could be reprogrammed by rerouting feedback streams of SFQ pulses. Several rerouting techniques have been suggested; see, e.g., [9].

It is easy to note that novel neuromorphic circuits are heavily supported by the conventional digital circuitry; see, e.g., [10]. Similarly, it is safe to plan that superconductor neuromorphic components will also be heavily supported by conventional digital superconductor components. New flavors of RSFQ circuitry are currently the most developed and therefore the most suited candidates for such digital support circuitry.

### Acknowledgment

The numerical simulations were performed using PSCAN2 software package developed by Pavel Shevchenko [11]. We thank to Coenrad Fourie for assistance with InductEx software [12] used for inductance extraction from circuit layouts. We are also grateful to Vlad Bolkhovsky and Ravi Rastogi for overseeing the wafer fabrication.

This research was supported by the Under Secretary of Defense for Research and Engineering under Air Force Contract No. FA8702-15-D-0001. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the Under Secretary of Defense for Research and Engineering. Delivered to the U.S. Government with Unlimited Rights, as defined in DFARS Part 252.227-7013 or 7014 (Feb 2014). Notwithstanding any copyright notice, U.S. Government 11 rights in this work are defined by DFARS 252.227-7013 or DFARS 252.227-7014 as detailed above.
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