A simple yet precise capacitance estimation method for on-chip power delivery network towards EMC analysis

Toshiki Kanamoto¹, ², Koki Kasai¹, Kan Hatakeyama¹, Atsushi Kurokawa¹, Tomoyuki Nagase¹, and Masashi Imai¹

Abstract In this letter, we propose a method to precisely extract on-chip capacitance in a transistor level with the minimal signoff data. As electromagnetic compatibility (EMC) concern in this work, a precise estimation of on-chip capacitance is important for designing a power delivery network (PDN) of LSI-package-board systems. However, the conventional methods require additional libraries other than the signoff data to extract the capacitance in a chip level. The proposed method improves accuracy of the extracted capacitance by simulating the device intrinsic capacitance simultaneously in the transistor level and enabling us to utilize commonly used design resources and flow as well. The experimental results show that the capacitance of a fabricated chip in 130nm technology estimated by the proposed method is within 8% error compared to the measurement of the capacitance. The whole extraction process can be done within a short period of time.

Keywords: on-chip capacitance, capacitance measurement, extraction, power delivery network (PDN), electromagnetic compatibility (EMC)

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Recently, a large scale integrated circuit (LSI) is operating at higher speed with lower power consumption owing to the recent trends of scaling down metal-oxide-semiconductor (MOS) transistors and decreasing the power supply voltage [1]. However, as the current density increase [2], the voltage fluctuations or noises in power delivery network (PDN) caused by the switching current of transistors is also increasing [3, 4]. In addition, lowering the power supply voltage relatively reduces the power supply noise margin. Once the noise exceeds a tolerated level, malfunction or performance degradation as well as unacceptable noise emission to external devices are emerging [5, 6].

In order to mitigate the power supply noise, PDN must be designed to absorb the on-chip noise. In general, PDN impedance seen by the LSI looking into the printed circuit board (PCB) is controlled to be lower than a target impedance [7, 8]. To suppress the PDN impedance, it is essential to accurately estimate the parasitic parameters including resistance, inductance and capacitance, which determine characteristics of resonance and anti-resonance. Schematic of the PDN impedance can be expressed by an equivalent circuit [9, 10] shown in the Fig. 1. In the figure, \( R_{CHIP} \) and \( L_{CHIP} \) are on chip resistance, inductance and capacitance, respectively. \( R_{PKG} \) and \( L_{PKG} \) are package resistance and inductance. \( R_{PCB} \) and \( L_{PCB} \) are on board resistance and inductance. \( C_{DECAP} \) is intentional decoupling capacitance. \( R_{DECAP} \) and \( L_{DECAP} \) are effective series resistance and inductance to \( C_{DECAP} \). If there are discrepancies in the parasitic parameters between the values estimated by a certain design flow and the actual values, the PDN will be over-designed or under-designed, which affects the design cost and circuit performance [11].

Here, we focus on on-chip capacitance. It dominates the impedance of PDN and suppress the power supply noise in a high frequency region [12]. However, it is not trivial for the chip vendors to disclose the value of on-chip capacitance [13]. Generally, board designers estimate on-chip capacitance based on the actual measurements, which is contrary to the package and board parasitic elements estimated by well-organized simulations [14]. If an on-chip capacitance is missing from the estimation then the evaluating resonance and anti-resonance characteristics, as shown in Fig. 2, will be missed as well. As indicated by the blue line, anti-resonance occurs due to \( C_{CHIP} \) and package inductance \( L_{PKG} \) so that the impedance of the PDN increases in the high frequency region in the real device operation.

In terms of the on-chip capacitance, portable simulation-based extraction methods have not been conducted yet. Some researchers have proposed simulation based on-chip capacitance extraction methods in a chip level [15, 16, 17, 18]. These extraction methods need extra libraries in both a chip level and a transistor level besides the ordinary signoff tools. Further, for larger on-chip capacitance in the order of 1nF to 100nF, the existing methods underestimate by up to 30%.

In this letter, we propose an on-chip capacitance extraction method using de facto standard signoff verification flow in reasonable processing time. In the proposed method, the intrinsic device capacitances are estimated in static manner along with dynamic AC analysis. We show the effectiveness of the proposed method compared to the measurement, as well as denoting the processing time.

The main contributions are as follows.
- On-chip capacitance extraction flow innovatively combining sign-off resources.
- Include well junction capacitance in extraction in addition to the intrinsic device capacitances to reduce the estimation error.
- As a result, the on-chip capacitance extracted by the
proposed method is correlated with the measured capacitance within 8% error for relatively large on-chip capacitance of 14 nF.

The rest of this paper is organized as below.

In Section 2., we describe components of on-chip capacitance as well as the procedure of how to extract each capacitance component in the proposed method. Section 3. compares capacitance estimated by the proposed method with capacitances retrieved by measurements. The processing time of the proposed method has been also computed. In section 4., conclusion remarks are given.

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2. Proposed extraction method

Estimating intrinsic capacitance from millions of MOS devices in chip design data is a challenging task. The existing methods in chip level [16, 17, 18] need specific macro models corresponding to individual cells to collect the intrinsic capacitance [19]. One of the alternative method is using AC analysis [20]. However, from a computational resource perspective it is not trivial to perform AC analysis from the top-level in transistor level to avoid additional library requirement. The proposed method effectively reduces the extraction cost by distributing computational resources in different ways.

Fig. 3 shows a cross-sectional view of the chip. There are power supply wirings from the top metal layer, which are connected to CMOS (Complementary Metal-Oxide-Semiconductor) circuits. There are four types of capacitance that contribute to on-chip capacitance [21, 22]. Interconnect capacitance(1): Capacitance parasitic to the power wiring. Gate capacitance(2): Intrinsic capacitance of MOS devices between gate(G) and source(S) or between gate(G) and drain(D). Diffusion capacitance(3): Parasitic capacitance between pn junctions of MOS devices. Well capacitance(4): Parasitic capacitance between N-well and P-substrate.

The proposed method estimates on-chip capacitance in three stages from the chip design data, as shown in Fig. 4. The originality of proposed method is especially on the part of well capacitance(4), where there is no organized sign-off tool to extract parasitic capacitance of the well junction. The motivation of the paper is also to provide new methodologies for extracting an intrinsic capacitance which is consist of gate(2) and diffusion(3) capacitances for both AC and static estimations. Interconnect capacitance(1) is extracted from the layout design data. Device intrinsic capacitance consist of gate capacitance(2) and diffusion capacitance(3) is estimated using AC analysis or statically, from netlists for circuit simulation. A part of well capacitance(4), which is not defined as intentional device, is estimated from the corresponding circuit simulation model.

2.1 Interconnect capacitance

In this work, a three dimensional layout parasitic extraction tool [23, 24, 25] extracts the interconnect capacitance of the specified nets.

2.2 Device intrinsic capacitance

To extract gate capacitance(2) and diffusion capacitance(3), we propose two methods based on AC analysis and static estimation.

2.2.1 Estimation with AC analysis

Fig. 5 shows the extraction flow to estimate (2) and (3) based on the AC circuit analysis. In this flow, we estimate the intrinsic capacitance cell by cell to distribute processing. The targeted hierarchy of cells are standard cells, or functional macro cells including SRAMs. We apply AC analysis twice for each cell as shown in Fig. 5. In the first run we tie the input gates to the power node(VDD). During the next execution we tie them to the ground(VSS). We adopt average of the
two estimated values as the intrinsic capacitance of each cell, assuming that number of effectively connected transistors to the power node is medium of the two situations. In this work, AC analysis is achieved by SPICE (Simulation Program with Integrated Circuit Emphasis) compatible circuit simulators [26, 27, 28, 29]. For highly repeatable large cells including SRAMs, we apply FastSPICE simulators [28, 29] to reduce the computational resources by matrix partitioning as well as hierarchical simulation. The capacitance of each cell is determined from the frequency characteristics obtained by AC analysis. From the impedance $Z$ at frequency $f$ (10 MHz here), $C$ is calculated by the following Eq. (1), assuming that $Z$ is dominated by the capacitive reactance.

$$C = \frac{1}{2\pi f |Z|}$$  (1)

Once the capacitance of each cell is determined, multiply the number of that cell in the chip by the capacitance value.

**2.2.2 Static estimation**

Fig. 6 shows the extraction flow to statically estimate the device intrinsic capacitance. This flow enables us to treat the entire netlist at one time. The main concept of this flow is to accumulate effective capacitance on the power node and the directly neighboring nodes, because $k\Omega$ of the MOS channel resisters shield capacitance on the further nodes. In this method, effective gate and diffusion capacitances are calculated by accumulating the capacitance of the device determined as shown in Fig. 7 regarding a three stages inverter chain. In the experiment, one of the FastSPICE simulators [30, 31] is employed to sum up the capacitances of the specified nodes. The total capacitance of the directly neighboring nodes to VDD is statistically halved.

**STEP1** Select the VDD node. This node corresponds to the capacitance on the source side of the pmos transistor.

**STEP2** Select the node on the drain side of the pmos connected to VDD. We call this node neighboring node.

**STEP3** In the calculation, the capacitance of the neighboring node selected in STEP2 is halved to take into account the conduction path. Finally, add the capacitance of the VDD node and effective capacitances of the neighboring nodes.

**2.3 Well capacitance**

We need to explicitly estimate well capacitance (4) because interconnect parasitic extractor do not extract the well capacitance [32]. In this work, the well capacitance is calculated by AC analysis for a N-well to P-substrate diode in Fig. 8, which is not extracted as an ideal device underneath the pmos transistor. Well capacitance is essentially proportional to well area $A$ and perimeter $P$ depicted in Fig. 9. To identify the coordinates, AC analysis is performed on more than two combinations of $A$ and $P$, as expressed in Eq. (2) and (3). Then the actual well capacitance is calculated from the total well area and perimeter, extracted from the entire chip using the design rule checker [23, 25].

$$C_1 = \alpha P_1 + \beta A_1$$  (2)

$$C_2 = \alpha P_2 + \beta A_2$$  (3)

**Fig. 7** Steps to identify the effective capacitance.

**Fig. 8** Cross-section of PMOS transistor.

**Fig. 9** Layout pattern of N-well.
3. Experiment results and discussion

3.1 Measured capacitance

We experimentally verify the proposed method using a NoC (Network-on-Chip) fabricated in an industrial 130nm wafer process technology. Size of the chip is 4954um × 4954um, and power supply voltage to core region is 1.2V. Fig. 12 shows a micrograph of the NoC.

First, we measure the impedance of the power supply to calculate on-chip capacitance, using an impedance analyzer (KEYSIGHT HP4291A RF). The impedance between the core power supply and ground was measured in the frequency range of 1 MHz to 1.8 GHz while applying a power supply voltage of 1.2 V as the bias voltage. Adjacent VDD and VSS pads are probed using a signal-ground (SG) probe (Cascade FPC-GS-550). Rest of the pads are left open. Fig. 10 shows the equivalent circuit to estimate the on-chip capacitance from the measured impedance. There is a probe capacitance on the SG probe that creates anti-resonance in the measured impedance. We exclude the probe capacitance from the equivalent circuit during the on-chip capacitance fitting and ignoring the anti-resonance. Next, on-chip capacitance is calculated by fitting the measured impedance with an RLC series equivalent circuit. Eq. (4) is applied to the RLC series equivalent circuit.

\[ |Z| = \sqrt{R^2 + \left(\frac{1}{\omega L} - \frac{1}{\omega C}\right)^2} \]  

(4)

Fig. 11 shows the fitting results. On-chip capacitance of the NoC is 14.2nF.

3.2 Extracted capacitance by the proposed method

Statistics of the test chip and computer resources during the experiment are shown in Table I and Table II, respectively. In Table I, intentional de-coupling capacitors are included in the mos transistors. Table III and Table IV show components of the capacitance extracted by AC-based analysis and static analysis. Table V describes parameters of the well capacitance estimation.

3.3 Comparison of capacitance and processing time

Fig. 13 shows the total on-chip capacitance and components obtained by each extraction method. Comparing the extracted value of on-chip capacitance with the result of measurement, differences at 1.2V bias voltage are 1.06 nF in the AC-based analysis and 0.53 nF in the partial static analysis, against the measured 14.22nF as shown in Table VI. The intrinsic capacitance estimation with AC analysis indicates that the contribution from memory (SRAM) blocks is almost same as the intrinsic capacitance from the logic cell, regarding this chip. The on-chip capacitance with statically estimated device intrinsic capacitance indicates that the intrinsic capacitance on the neighbouring nodes to VDD contributes 27% to the total capacitance. Table VII shows errors when we omit the well capacitance. Table VI indicates that extracting the well capacitance by the proposed method along with the intrinsic capacitance extraction suppresses
errors within 8%. In terms of the processing time, the static device intrinsic capacitance estimation takes quarter compared to the estimation with AC analysis that occupies 20% of the total time.

3.4 Bias voltage dependence
Except for the interconnect capacitance, the rest of on-chip capacitance has a bias voltage dependence [35]. Fig. 14 shows the bias voltage dependence of on-the-chip capacitance retrieved by measurement and the proposed method. The proposed method correlates with the measurement with 8% or less error where the bias voltage is above 0.5V. The static estimation of the device intrinsic capacitance well traces the measured capacitance above a nominal threshold voltage of 0.35V. A drawback of the static estimation of device intrinsic capacitance is errors appeared in the sub-threshold region or below. Voltage dependence of the estimated capacitance in the static flow comes from the well capacitance which is characterized as bias voltage dependent. Reducing the errors with the AC analysis is also one of our future works.

4. Conclusion
In this letter, we proposed the capacitance extraction method for on-chip power delivery network. The proposed method enables to extract on-chip capacitance from existing chip design resources within reasonable time. Comparing the results of on-chip capacitance extraction by measurement and the proposed method, the accuracy within 8% is achieved at the nominal supply voltage. The proposed method will promisingly contribute to EMC analysis. Reducing the errors in near and sub-threshold regions is one of our future works.

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