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Comparative study of C–V-based extraction methods of interface state density for a low-temperature polysilicon thin film

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Abstract
To extract comprehensive and accurate interface state density \(D_{it}\) distribution for a low-temperature polysilicon (LTPS) thin film, three well-established methods based on capacitance–voltage (C–V) measurements were compared: high–low frequency capacitance, conductance, and quasi-static (QS) capacitance methods. Because of the strong frequency-dependent response of grain boundary traps within the LTPS, C–V measurements are necessary on p- as well as n-type LTPS films, as they provide \(D_{it}\) distribution across the entire LTPS band gap. The QS capacitance method, which uses an optimal high–frequency C–V curve with a minimal grain boundary trap response, provided the best and most comprehensive estimate of \(D_{it}\) distribution across the LTPS band gap, even at room temperature (25 °C). Although the narrow extraction ranges of \(D_{it}\) were extended toward the mid-gap region by increasing the measurement temperature in both high–low frequency capacitance and conductance methods, the responses of the grain boundary traps still overestimated the \(D_{it}\) values near the band edges.

1. Introduction

Among the numerous types of thin-film transistors (TFTs) that are essential for driving displays, compared to conventional amorphous silicon TFTs, low-temperature poly-Si (LTPS) TFTs have been widely used because of their high electron mobility and robust electrical/optical stiffness [1–3]. However, with decreasing thickness of the gate insulator (G.I.) owing to the demand for miniaturization and performance enhancement of TFTs, characterisation as well as in-depth understanding of the G.I./LTPS interface, which directly influence the performance of LTPS TFTs, has become essential. Among the factors that determine characteristics of the G.I./LTPS interface, interface state density \(D_{it}\) is the most important because it largely determines the electrical characteristics of the resulting TFTs. A high \(D_{it}\) generates an insufficient Fermi level response or Fermi level pinning, because of which, it is difficult to control the charge carriers of the channel and thus fabricate TFTs with a low subthreshold swing [4, 5]. Therefore, it is essential to establish an accurate \(D_{it}\) extraction method for LTPS devices to further improve the properties of the G.I./LTPS interface.

Since the establishment of Si technology, numerous \(D_{it}\) extraction methods using the convenient capacitance–voltage (C–V) measurements of metal–oxide–semiconductor (MOS) capacitors have been developed, including the high–low frequency capacitance (Castagné–Vapaille) method [6], quasi-static (QS) capacitance method [7], high-frequency capacitance (Terman) method [8, 9], and conductance method [10, 11]. With considerable development in transistor technology, these methods have been applied even to new single-crystalline materials to replace Si, such as Si1−xGex and III–V compounds, and significant effort has been made to identify the relevant \(D_{it}\) extraction method for each channel material [12–14]. However, in the case of LTPS TFTs, which have an additional grain boundary trap effect, comparative evaluation of these C–V-based \(D_{it}\) extraction methods has rarely been reported, while several studies have reported the results of extracting \(D_{it}\) near...
the LTPS band edges only [15–20], and not across its entire band gap, using the conductance and Terman methods and low-frequency capacitance measurement.

In this study, we applied three representative $C$–$V$-based $D_n$ extraction methods, namely, high–low frequency capacitance, conductance, and QS methods, to the LTPS capacitors, and compared their performance when the response of grain boundary traps was involved. To overcome the limited response of $D_n$ in the LTPS film, we used the $C$–$V$ characteristics of p- as well as n-type LTPS films for determining $D_n$ distribution across the entire band gap of LTPS.

2. Experiments

A 40-nm-thick amorphous Si layer deposited using plasma-enhanced chemical vapor deposition (PECVD) on a glass substrate was fully crystallized via excimer laser annealing ($\lambda = 308$ nm). Both boron-doped (p-type) and phosphorus-doped (n-type) LTPS films with similar doping concentrations ($\sim 1 \times 10^{12}$ cm$^{-3}$) were prepared using ion implantation and annealing processes. On both p- and n-type LTPS films, 100-nm-thick SiO$_2$ was deposited as a G.I. layer using PECVD. For the following electrical measurements, a 300-nm-thick Mo gate electrode (area $= 200 \times 200$ $\mu$m$^2$) was patterned on G.I. using sputtering and lift-off processes. Multi-frequency and QS $C$–$V$ measurements of the LTPS MOS capacitors were carried out using a Keysight E4980A LCR meter and a Keysight B1500A parameter analyzer. For the multi-frequency $C$–$V$ measurement, the imposed ac frequency varied from 100 Hz to 1 MHz with a logarithmic step of 0.1. During the QS $C$–$V$ measurement, sufficient light was irradiated on the samples using a lamp mounted on the probe station to efficiently generate minority carriers in the LTPS film. The measurement noise was suppressed by optimizing the measurement parameters such as the delay time, and an offset correction procedure was adopted to remove the parasitic capacitance effect of the equipment [21].

3. Results and discussion

First, multi-frequency $C$–$V$ characteristics of the capacitors built on both p- and n-type LTPS films were measured at room temperature (RT, $\sim 25$ °C). Because the LTPS films are thin ($\sim 40$ nm) and have a low doping density ($\sim 1 \times 10^{12}$ cm$^{-3}$), their high resistance state can significantly distort the multi-frequency $C$–$V$ curves measured in a parallel mode owing to a decrease in the capacitance values with increasing frequency, particularly in the accumulation region [22, 23]. To minimize the possible series resistance ($R_s$) effect, the measured multi-frequency $C$–$V$ curves were corrected using the following equations [24], and the corrected graphs were compared with the simultaneously measured QS $C$–$V$ curves, as shown in figure 1(a) and (b).

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad \text{and} \quad C_C = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{[G_m^2 - (G_m^2 + \omega^2 C_m^2)R_s]^2 + \omega^2 C_m^2},$$

(1)

where $G_m$ and $C_m$ are the measured capacitance and conductance values, respectively, $\omega$ is the measurement angular frequency, and $C_C$ is the corrected capacitance used for plotting figures 1(a) and (b). After $R_s$ correction, the frequency-dependent reduction in the accumulation capacitance ($C_{acc}$) disappeared in the p-type LTPS sample. However, it remained in the n-type LTPS sample, as shown in figure 1(b), which may be attributed to the lower carrier mobility in n-type polysilicon than in p-type polysilicon induced by the higher barrier heights of the grain boundaries [25]. In contrast to conventional multi-frequency $C$–$V$ characteristics on a single-crystalline Si substrate, the $C$–$V$ curves of both p- and n-type LTPS capacitors widened near the accumulation/depletion boundary region with increasing measurement frequency, as shown in figures 1(a) and (b). An excessively high $D_n$ at each band edge region can induce stretching of $C$–$V$ curves at high frequencies; therefore, a low-temperature measurement was carried out to suppress these interface state responses [26]. As shown in the inset of figure 1(a), no distinct change was identified even at the highest measurement frequency of 1 MHz with decreasing measurement temperature (minimum $-150$ °C). This indicates that the amplified stretching behavior of the $C$–$V$ curves at high frequencies did not originate from the interface states but from the traps located within the grain boundaries in the LTPS film, as observed in several studies [27, 28].

To locate the interface states within the band gap of an LTPS film, the applied gate voltage ($V_G$) was converted to surface potential ($\Psi_S$) using the Berglund integral of the RT-measured QS $C$–$V$ curves (figure 1), expressed using equation (2) [24]:

$$\Psi_S (V_G) = \int_{V_{FB}}^{V_G} \left( 1 - \frac{C_{QS}}{C_{OX}} \right) dV + \Psi_S (V_{FB}),$$

(2)

where $V_{FB}$, $C_{QS}$, and $C_{OX}$ are the flat-band voltage, measured QS capacitance, and oxide capacitance (corresponding to the maximum $C_{QS}$ in the accumulation region), respectively. $V_{FB}$ is determined by reading the
$V_G$ corresponding to the calculated flat-band capacitance ($C_{FB}$) of the 10 kHz $C-V$ curve to minimize the effects of the interface state and grain boundary state responses. As shown in figure 2, $\Psi_S$ increases linearly as $V_G$ approaches a mid-gap region from the valence and conduction band edges for the p- and n-type LTPS samples, respectively, and then starts to be underestimated. On a single-crystalline Si substrate, the applied voltage can modulate $\Psi_S$ efficiently across the entire band gap because of the sufficient generation of minority carriers with a long lifetime [29]. However, for the LTPS film, the effective lifetime of minority carriers was shortened because of the presence of grain boundary traps [30], which impeded band bending from the mid-gap to opposite band edges in response to the applied voltage. These results suggest that both p- and n-type LTPS samples are necessary to acquire $D_{it}$ distribution across the entire band gap of LTPS, and the $D_{it}$ distributions within the lower and upper halves of the LTPS band gap can be obtained from the p- and n-type LTPS capacitor samples, respectively.

Figure 3 compares the $D_{it}$ distributions obtained by combining the extraction results for both p- and n-type LTPS capacitors (RT-measured $C-V$ data sets shown in figure 1) based on the three calculation methods, high–low frequency capacitance, conductance, and QS capacitance. The following equations [24] were used to calculate the $D_{it}$ values at each $V_G$ that was converted to $\Psi_S$ only for the valid regions—linearly varying regions in figure 2—corresponding to the lower and upper halves of the LTPS band gap for the p- and n-type LTPS samples, respectively.

High–low frequency capacitance method:

$$D_{it} = \frac{1}{Aq} \left[ \left( \frac{1}{C_{LF}} - \frac{1}{C_{OX}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{OX}} \right)^{-1} \right]$$

(3)

Conductance method:

$$D_{it} = \frac{2.5}{Aq} \left( \frac{\omega C_{OX}^2 C_c}{G_c^2 + \omega^2 (C_{OX} - C_c)^2} \right)$$

(4)

Figure 1. Multi-frequency and QS $C-V$ characteristics measured from (a) p- and (b) n-type LTPS capacitors at RT. For multi-frequency $C-V$ characteristics, the imposed ac frequency varied from 100 Hz to 1 MHz with a logarithmic step of 0.5. Inset in panel (a) shows 1 MHz $C-V$ characteristics as a function of measurement temperature for p-type LTPS capacitors.
QS capacitance method:

\[
D_{\text{it}} = \frac{1}{Aq} \left[ \left( \frac{1}{C_{\text{QS}}} - \frac{1}{C_{\text{OX}}} \right)^{-1} - \left( \frac{1}{C_{\text{HF}}} - \frac{1}{C_{\text{OX}}} \right)^{-1} \right]
\]  

(5)

Here, \(C_{\text{HF}}\) and \(C_{\text{LF}}\) are the capacitances measured at the highest and the lowest frequencies, respectively, \(A\) is the capacitor area, and \(q\) is the elementary charge. As shown in figure 3, the high–low frequency capacitance and conductance methods, that use an ac signal for the response of interface states, provide a distribution only near the valence and conduction band edges with similar \(D_{\text{it}}\) values. In contrast, a much wider \(D_{\text{it}}\) distribution toward the mid-gap region can be acquired using the QS capacitance method based on a linear dc voltage ramp to capture the response of the interface states. When the highest frequency of 1 MHz was used for \(C_{\text{HF}}\), all three distribution curves overlapped well in the regions (colored regions) close to the valence and conduction band edges. However, as discussed above, the LTPS samples exhibited a strong stretching behavior at the accumulation/depletion boundary region during the high–frequency measurement because of the additional response of traps located within the grain boundaries in the LTPS film, which might have resulted in erroneous
overestimation of $D_{it}$ near each band edge region. Therefore, to minimize this, the 10 kHz $C-V$ curves with lower stretching behavior than that of the 1 MHz $C-V$ curves were used as the $C_{HF}$ values for the QS method-based extraction, and the results are shown in figure 3. As a result, the $D_{it}$ values near each band edge region were reduced, probably reaching real values, and those within the mid-gap region remained well matched with the values estimated by the QS method using the 1 MHz $C-V$ data. The $D_{it}$ values near the mid-gap region determined by the QS method were in the range of mid-$10^{11}$ eV$^{-1}$ cm$^{-2}$.

As discussed above, when both high–low frequency capacitance and conductance methods were used, the response range of the interface states was limited close to the band edge regions and overestimated because of the additional response of grain boundary traps. To extend the response of the interface states toward the mid-gap region for both methods, high-temperature $C-V$ measurements were carried out at 100 °C. High-temperature measurements were used only for the high–low frequency capacitance and conductance methods because of the presence of a large electrical noise during the QS measurement. As shown in figure 4, an increase in the measurement temperature did not alter the $C-V$ characteristics at high frequencies (>10 kHz). However, the frequency-dependent dispersion near the depletion region at low frequencies (<10 kHz) became more prominent with decreasing frequency, confirming the onset of the response of interface states located deep in the band gap [31, 32]. The $D_{it}$ distributions calculated via high–low frequency capacitance and conductance methods using the high-temperature $C-V$ results are plotted in figure 5 and compared with that extracted via the QS capacitance method at RT (also shown in figure 3). By providing sufficient thermal energy, the $D_{it}$ response was extended deep into the mid-gap region for both high–low frequency capacitance and conductance methods, matching the $D_{it}$ distribution extracted using the QS capacitance method measured at RT. However, the high–low frequency capacitance and conductance methods still underestimated the $D_{it}$ values near the mid-gap region compared to the RT-measured QS capacitance method. In addition, the response of the grain boundary traps by the ac-based measurement made it impossible to extract the exact $D_{it}$ values near the band edge regions.

Considering these results, it can be concluded that the dc-based QS capacitance method is the most appropriate approach for extracting exact $D_{it}$ values for LTPS capacitors even at RT and that the use of both p- and n-type

![Figure 4](image_url). Multi-frequency $C-V$ characteristics measured from (a) p- and (b) n-type LTPS capacitors at 100 °C. The imposed ac frequency varied from 100 Hz to 1 MHz with a logarithmic step of 0.5.
LTPS capacitors facilitates the extraction of $D_{it}$ distribution across the entire LTPS band gap. Nevertheless, choosing appropriate $C_{HF}$ values with a minimal response of grain boundary traps in equation (5) is essential to minimize the erroneous overestimation of $D_{it}$ near each band edge region.

4. Conclusions

We applied three conventional $D_{it}$ extraction methods, namely, high–low frequency capacitance, conductance, and QS capacitance methods, based on C–V measurements to LTPS capacitors with an additional response of grain boundary traps. The advantages and disadvantages of these methods were discussed based on high- and low-temperature C–V measurements, and the extraction of the $D_{it}$ distribution across the entire LTPS band gap was demonstrated using both p- and n-type LTPS capacitors, as summarized below.

1. Both high–low frequency capacitance and conductance methods allowed $D_{it}$ estimation only within the narrow regions near the LTPS valence and conduction band edges of the p- and n-type LTPS capacitors, respectively. However, the extracted $D_{it}$ was overestimated because of the additional response of the grain boundary traps in the LTPS film.

2. The QS capacitance method with a proper choice of high-frequency C–V data with a minimal effect of grain boundary traps allowed accurate $D_{it}$ estimation near the LTPS band edges. Nevertheless, the insufficient minority carrier response within the LTPS film required measurements of both p- and n-type LTPS capacitors to determine the $D_{it}$ distribution across the entire LTPS band gap.

3. High-temperature C–V measurements could extend the $D_{it}$ extraction range toward the mid-gap region for the high–low frequency capacitance and conductance methods. However, the response of the grain boundary traps in the LTPS still overestimated the $D_{it}$ value near the LTPS valence and conduction band edges.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).
Conflicts of interest

There are no conflicts to declare.

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