Charge-Resistance Approach to Benchmarking Performance of Beyond-CMOS Information Processing Devices

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Abstract—Multiple beyond-CMOS information processing devices are presently under active research and require methods of benchmarking them. A new approach for calculating the performance metric, energy-delay product, of such devices is proposed. The approach involves estimating the device properties of resistance and switching charge, rather than dynamic evolution characteristics, such as switching energy and time. Application of this approach to a wide class of charge-based and non-charge-based devices is discussed. The approach suggests pathways for improving the performance of ‘beyond-CMOS’ devices and a new realistic limit for energy-delay product in terms of the Plank’s constant.

Index Terms—Energy-delay, beyond-CMOS devices, electronic devices, spintronic devices, benchmarking

I. INTRODUCTION

SCALING of complementary metal-oxide-semiconductor (CMOS) transistors has enabled the impressive improvement in computing power over the last few decades. However, this shrinking of device dimensions is expected to reach a limit in the near future [1]. This has led to an intensive search for the next information processing device that could potentially supplement CMOS [2]. A wide range of physics has been invoked for different ‘beyond-CMOS’ device proposals (see for example [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]), making comparison of their performance a challenging task. In this paper, we present a simple, yet universal equation relating the dynamic evolution characteristics of switching energy (E) and time (τ) to the device properties of resistance (R) and the switching charge (Q). This relation allows us to propose a new approach for benchmarking and comparing the energy-delay performance of all information processing devices.

Energy for switching all information processing devices, be it CMOS or proposed beyond-CMOS devices, has to be provided by an electrical power supply that causes charges to move through metals, semiconductors or insulators. In this paper, we use this observation to formulate a new approach for calculating the energy-delay performance metric of devices and circuits in terms of two quantities: (a) the total charge, Q, that is involved in switching a device; (b) the resistance, R, of a device along the current path used for switching. Q, R for all devices switched by a constant voltage supply, are related to the switching energy E and switching delay τ through the central equation of this paper:

\[ E \tau = Q^2 R. \] (1)

From a physical standpoint, it is surprising that the dynamic evolution quantity of \( E \tau \) can be determined solely from the static charge transport characteristics of Q,R even for non-electronic devices. The analytic proof of Eqn 1, valid irrespective of the state variable, is presented in Appendix A. In this paper, we would concentrate on the insight that can be obtained by evaluating device performance from its Q, R; since these parameters can be related to the underlying physical mechanisms of device switching along with pertinent assumptions, and fundamental and technological limitations. This ‘Q−R approach’ essentially reduces the ‘search for next logic switch’ [2] to a problem of identifying the device physics that would allow operation with low Q and low R.

\( E \tau \) metric of information processing devices has traditionally been evaluated from the estimation or measurements of E and τ, which easily communicate their potential as a fast or a low-power digital switch. It would be very relevant to ask why we need a different approach. We emphasize that the Q − R approach provides a more convenient way to estimate the same value of \( E \tau \) for all devices, while relating it to the unique underlying physics of each device. Given our long experience with transistors, the methods for estimation of \( E \tau \) of CMOS devices are well known. However, for beyond-CMOS devices, the Q − R approach for estimating energy-delay performance offers two distinct advantages.

Firstly, if we were to estimate E and τ directly for such devices, we would need to perform complex high-speed measurements or develop a theory of the device’s dynamic evolution and obtain the energy and delay by solving time-dependent equations. The Q − R approach allows us to evaluate \( E \tau \) just from static characteristics - Q,R which are directly connected to underlying physical properties of any
Fig. 1. Comparison of device performance with the $Q - R$ approach (a) The energy-delay ($E - \tau$) plot comparing the performance of various logic devices (data taken from Ref [31]) (b) $E - \tau$ can be translated to a charge-resistance ($Q - R$) plot using Eq. 4 that gives more insight into device performance. (c) However Eq. 4 is not valid for devices where $\tau > \tau_{pu}$, the pulse width (d) To put all devices on the same footing it might be better to translate the $E*\tau$ plot to an analogous $Q-R(\tau/\tau_{pu})$ plot. Similar to the equi-$E$ lines in (a), we draw equi-$Q^2 R$ (b) and equi-$Q^2 R(\tau/\tau_{pu})$ lines in (d) to enable comparison between different devices. Please refer to Appendix, Table I for data and device nomenclature. The acronyms used are as follows: CMOS-HP (high performance CMOS), CMOS-LP (low power CMOS), HomJTFET (Homojunction III-V tunneling FET), HetJTFET (Heterojunction TFET), grnTFET (Graphene nanoribbon TFET), GpnJ (Graphene pn-junction), BisFET (Bilayer pseudospin FET), SpinFET (Sughara-Tanaka SpinFET), STT/DW (Spin torque domain wall), STMG (Spin torque majority gate), STT-triad (Spin transfer torque triad), STOlogic (Spin torque oscillator), ASL (All spin logic), SWD (Spin wave device), NML (Nanomagnetic logic); $e$: Charge of an electron ($1.6 \times 10^{-19}$C), $h$: Planck’s constant.

II. CHARGE-RESISTANCE APPROACH

Recently, Nikonov et. al. [31] presented a comparative study of beyond-CMOS devices and circuits. They compared the projected performance of various devices based on their position on an $E - \tau$ plot (Fig 1a). Ideally, we would like devices which are both low-power and low-delay and occupy the lower left corner of the $E - \tau$ plot. However, from Fig 1a, it is apparent that few beyond-CMOS devices have projected $E*\tau$ better than CMOS. The extraordinary $E - \tau$ of CMOS has
been achieved by years of scaling, also evident from Moore’s law [32]. The possibility of scaling the beyond-CMOS devices to lower their $E \ast \tau$ product cannot be inferred from the $E - \tau$ plot.

Nevertheless, translating the $E - \tau$ data in Fig 1i into $Q - R$ (Appendix B) allows us to analyze and compare performance of devices on a $Q - R$ plot (Fig 1h), which immediately suggests the scaling potential and pathways for improvement of different devices. Similar to the $E - \tau$ plot, we would like to have devices occupying the lower left corner of a $Q - R$ plot i.e. devices which have a low $Q$ as well as low $R$. However, it can be observed that in general, the electronic devices have higher $R$ and lower $Q$, ranging from tens to hundreds of electrons. It may be difficult to scale the already low $Q$ further. However, in general, $Q$ of electronic devices can be decreased by lowering the supply voltage ($V_{DD}$) or by using a more efficient device which would allow switching with a smaller capacitance since switching of electronic devices involves charging/discharging a capacitance ($C$) by $V_{DD}$ such that $Q = CV_{DD}$. The $R$ of these electronic devices may be decreased by choosing a different material, preferably metallic conductors.

Most spintronic/magnetic devices are metallic, leading to favorable low $R$ (Fig 1j); but switch tens of thousands of electrons. Thus, to make $E \ast \tau$ comparable or better than CMOS, $Q$ should be reduced. Relationship of $Q$ to the device hardware and lay-out for electronic devices is easy to comprehend (Appendix B). Since $E$ is provided by electrons driven by an electrical power supply, $Q$ can indeed be related to physical device parameters for most information processing devices, even for spintronic and magnetic devices. Consider for example, the case of All spin logic (ASL) device [26] which involves switching of nanomagnets by the phenomenon of spin transfer torque, where each injected spin-polarized electron flips one Bohr Magneton or spin in the magnet. This leads to a simple relation between $Q$ and $N_s$, the number or spins comprising the magnet [30]:

$$Q \sim \frac{2qN_s}{\eta},$$

where $\eta$ is the efficiency related to the spin to charge current ratio. Owing to large $N_s$, the $Q$ for the state of the art magnets is much greater than corresponding electronic devices (Supp II). Thus, $Q$ can be scaled by reducing $N_s$ in a way that does not compromise the stability of the magnet [30]. Another way of decreasing $Q$ is to increase $\eta$, which seems possible in the light of the recent experiments which switch huge magnets using spin Hall effect [33] where $\eta > 1$.

The $Q - R$ approach, applied to ASL or similar spin torque based logic devices, helped us identify the device properties that should be changed to improve the $E - \tau$ performance of these devices. A similar exercise for relating the $Q,R$ to physical device parameters can be done for almost all information processing devices (Appendix. Table II). $Q,R$ are sufficient to determine $E \ast \tau$ of any device switching with a constant $V_{DD}$. Comparison of the position of devices in the $E - \tau$ (Fig 1h) and $Q - R$ plot(Fig 1b) brings to light a few ‘special cases’. Some of the spintronic devices (colored in green, Fig 1p) appear to have low $Q$ and low $R$ despite not comparing favorably with other logic devices on the $E - \tau$ plot, since $E\tau > Q^2R$ for these devices(Fig 1h). Physically, this is because these devices are switched by a short voltage pulse($\tau_{pu}$) leading to a small $Q$; but the long magnet switching time ($\tau > \tau_{pu}$) affects its $E - \tau$ performance. Eqn 4 is still valid for the duration the voltage pulse is on ($\tau_{pu}$) and to consider such devices where $\tau > \tau_{pu}$, Eqn 4 can be rewritten as (Appendix A):

$$E\tau = Q^2R(\tau/\tau_{pu}); \tau \geq \tau_{pu}$$

Eq. 6 is universally valid for all information processing devices switched by a voltage pulse of constant amplitude. Thus, to compare all devices on the same footing irrespective of the relation between $\tau$ and $\tau_{pu}$, it might be better to compare the plot of $Q$ vs $R(\tau/\tau_{pu})(Fig 1i)$ which is analogous to the $E - \tau$ plot for all logic devices. Indeed in Fig 1j, the position of the special cases outlined in Fig 1i reflect their position on the $E - \tau$ plot.

III. LIMIT OF ENERGY-DELAY

One of the main advantages of re-mapping $E - \tau$ to $Q - R$ is the evaluation of the possibility of scaling down $E \ast \tau$ product by scaling $Q,R$ Thus, it is important to investigate the minimum possible $E \ast \tau$ product for information processing devices. $E \ast \tau$ product involved in the switching a single electron is limited by the Uncertainty relation [34]:

$$E\tau \geq h$$

which relates $E \ast \tau$ to $h$, the Plank’s constant. While the Uncertainty relation is definitely valid for a multi-electron switching event, it may be possible to have a stricter lower bound on the $E\tau$ product depending on whether the electrons are switching simultaneously, sequentially or a combination of both. Such a limit for $E \ast \tau$ product, involved in any fast switching event, can be presented using Eqn 4 since $Q$ is fundamentally quantized and $R$ is limited by the interface resistances.

Consider a switching event which involves $N$ charges:

$$Q = Nq.$$  

If the charges pass through a $M$-moded resistor, the resistance of a device is limited by

$$R \geq \frac{h}{q^2\sigma M}$$

where $\sigma$ is the effective ‘spin’ of the electrons ($\sigma = 2$ if we consider the up and down spin of electrons, $\sigma = 4$ for graphene due to its ‘pseudospin’ [35]). If we apply these values of $Q,R$ to Eqn 4 we get an important result:

$$Q^2R = E\tau \geq h \left( \frac{N^2}{\sigma M} \right)$$

where each of the three quantities ($N, \sigma, M$) on the right side of Eqn 5 are well-defined physical quantities.

It is easy to see that if we consider charging a capacitor with a single electron through a single moded conductor, Eqn 3
reduces to the uncertainty relation. However, most real devices involve charging of at least tens to hundreds of electrons and Eqn [3] predicts a realistic stricter lower bound on $E \tau$ product than that given by the uncertainty relation for these devices. An explanation of the limit in Eqn [3] can be suggested if we consider the switching event as a transport of N electrons through M parallel paths or modes in ($N/\sigma M$) sequential batches.

Feynman [36] argued that if we arrange $sp$ logic units: $p$ parallel rows of $s$ logic units in series, the net energy-delay product would be

$$E \tau = p s^2 E_0 \tau_0,$$

where $E_0$ and $\tau_0$ are energy and delay for each unit. The transport of N electrons can be considered as N logic events of switching one electron, $\sigma M$ of which occur simultaneously through the M modes. If $E_0 - \tau_0$ is the energy-delay involved in the switching of one electron, the transport of N electrons, sequentially in ($N/\sigma M$) batches, through $\sigma M$ parallel paths should have an energy delay of

$$E \tau = \sigma M (N/\sigma M)^2 E_0 \tau_0$$

since $p = \sigma M$ and $s = (N/\sigma M)$ in this case. Assuming, $E_0$ and $\tau_0$ abide by the uncertainty principle, we get the relation in Eqn [3] for the case of switching N electrons.

Eqn [3] indicates that energy-delay product can possibly approach $h$ only for a scaled system with low $N$ if the charges are transported through metals where $M$ is high. Scaling of CMOS has reduced the $N$ at the device level; we estimate N=168 for CMOS-HP projections in Ref [31]. However, $M$ is low in these scaled semiconductors. Considering the width (W) of 60nm [31] and Fermi wavelength ($\lambda_f$) of $\sim 11\text{nm}$, $M$ can be estimated to be $\sim 11$ using $M = \text{Int}[W/(\lambda_f/2)]$ [38]. According to Eqn [3] this leads to $E \tau \geq 2465h$ for CMOS-HP. This crude estimate is 3 times lower than the $E \tau$ product of CMOS (Fig 2), assuming $\sigma = 1$. However, scaling of CMOS makes it more efficient, operating closer to the $E \tau$ limit (Fig 2).

The above example of evaluating the limits of CMOS operation brings forth the utility of the quantum limit in Eqn [3] for practical information processing devices. It is well known that there is a trade-off in switching energy and delay; faster switching requires higher overdrive and higher energy consumption. Infinitely slow or adiabatic switching requires a minimum reversible energy expenditure, sometimes referred to as the Landauer limit [39]. Currently, this limit is of academic interest since most future-generation CMOS and ‘beyond-CMOS’ devices aim to operate at the other extreme of switching with as low $\tau$ as possible without raising the energy consumption of the device above present day CMOS. The limit in Eqn [3] addresses this energy-delay trade-off. For a real device, Eqn [3] helps us estimate how low the $E \tau$ product can be, given the technological and cost constraints that determine $N, \sigma$ and $M$.

### IV. Conclusion

In essence, the $Q - R$ approach presented in this paper helps us appreciate the insight into device characteristics that can be obtained from the energy-delay performance metric. If a device is projected to have spectacular energy-delay performance, the $Q - R$ approach immediately indicates that we need to investigate what device physics leads to low $Q.R$. A low projected device $Q$ (say tens of electrons, Appendix Table I), would raise questions on the effect of various electronic noise sources and device parasitic capacitances on the value of $Q$. A low $R$ (tens of Ohms) would raise questions on the effect of parasitic resistances on the projected value of $R$. On the other hand, if a device has unimpressive energy-delay, the $Q - R$ approach can help us judge whether the energy-delay can potentially scaled down further. Essentially, the $Q - R$ approach reduces the ‘search for next switch’ to a problem of identifying the device physics that would allow operation with low $Q$ and low $R$.

We end the paper by noting that the $Q - R$ approach presented for individual devices, can also be extended to larger systems and circuits. We have applied the $Q - R$ approach to evaluate $E \tau$ of few simple logic circuits, where it can seamlessly incorporate even the parasitic charge and resistance of interconnects. Neglecting parasitics, the total $Q$ of such circuits is simply the product of individual device $Q$ and the total number of devices involved in the circuit. However, $Q$ in the presence of interconnect charge and the relation of overall circuit $R$ to device $R$ is non-trivial and we leave the treatment to future publications. Nevertheless, the possibility of extending $Q - R$ approach to larger systems also suggests the validity of the limit on $E \tau$ product for larger systems, where it could provide the quantitative formulation of the energy-delay tradeoff that is fundamental to the operation of most systems.
APPENDIX A
THE CHARGE-RESISTANCE METRIC

Our aim in this section is to justify the simple relation for the energy (E)-delay (τ) product introduced in the paper:

\[ E\tau = Q^2 R. \] (4)

where \( Q \) is the total charge that is involved in switching a device; \( R \) is the resistance of a device along the current path used for switching. The relation can be easily derived for the simplified case of constant voltage \( V_{DD} \) and current \( I \) in a current path with capacitance \( C \) and resistance \( R \). Then the energy and delay are:

\[ E = CV_{DD}^2 = QV_{DD}, \]
\[ \tau = Q/I, \]

and their product is

\[ E\tau = RC^2V_{DD}^2 = RQ^2 \]

which is the same as Eq. 3. The relation between \( E - \tau \) and \( Q - R \) in case of capacitor charging has been pointed out by other authors (see for example Ref. [36]). However, in this section, we introduce Eq. 4 as a generic relation valid for all information processing devices that derive the switching energy from a voltage pulse with constant amplitude \( V_{DD} \).

Consider a generic switch in which the voltage is applied as a pulse of duration \( \tau_{pu} \):

\[ V(t) = \begin{cases} \frac{V_{DD}}{\tau_{pu}} & t \leq \tau_{pu} \\ 0 & t > \tau_{pu} \end{cases} \]

For most switching events (e.g. the case of switching a capacitor), the switching time is limited by the charging time \( \tau = \tau_{pu} \). However, in some logic devices, e.g. spintronic devices switched by magnetoresistive effect (see for example Ref. [40]), switching of the state variable (magnetization) takes much longer than the time period over which the voltage pulse is turned on. Hence, no energy is supplied by the source in this process since \( V(t)=0 \) for \( t > \tau_{pu} \). Hence the energy supplied by the power supply can be evaluated by integrating the power supplied from \( t=0 \) to \( t=\tau_{pu} \):

\[ E = \int_0^{\tau_{pu}} V(t)I(t)dt = V_{DD}Q \] (5)

where \( Q = \int_0^{\tau_{pu}} I(t)dt \). If the current varies as a function of time, the average current can be defined as \( I_{avg} = \int_0^{\tau_{pu}} I(t)dt/\tau_{pu} \). In other words,

\[ \tau_{pu} = Q/I_{avg} \]

Thus the relations for \( E \) and \( \tau_{pu} \) lead to

\[ E\tau_{pu} = Q^2(V_{DD}/I_{avg}) = Q^2 R \]

which is a generalization of Eq. 4(Q and \( R \) can thus be related to \( E\tau \) by the general relation:

\[ E\tau = Q^2 R(\tau/\tau_{pu}) ; \tau \geq \tau_{pu} \] (6)

Eq. 6 is thus universally valid for all information processing devices switched by a voltage pulse of constant amplitude \( V_{DD} \).

APPENDIX B

Q – R APPROACH FOR BEYOND-CMOS DEVICES

In the previous section, we discussed that Eq. 6 holds if (a) energy is supplied by voltage pulse with constant amplitude and, (b) \( \tau \geq \tau_{pu} \). These conditions are valid for most beyond-CMOS devices, especially those considered in Ref [31]. As such, the \( Q, R \) for different devices can be extracted from Table I from the \( E, \tau, \tau_{pu} \) data in Ref [31] using Eqs. 5 and 6. In this paper we have only considered the devices investigated by Nikonov and Young [31]. These device broadly span different state variables of charge (CMOS-HP (Si MOSFET high performance), CMOS-LP (Si MOSFET low power), HomJTFET (III-V tunneling FET), Heterojunction TFET, gnnTFET (Graphene nanoribbon TFET), GpnJ (Graphene pn-junction), BisFET (Bilayer pseudospin FET), SpinFET (Sughara-Tanaka SpinFET) and spin/magnetization (STT/DW (Spin torque domain wall), STMAG (Spin torque majority gate), STT-triad (Spin transfer torque triad), STOlogic (Spin torque oscillator), ASL (All spin logic), SWD (Spin wave device), NML (Nanomagnetic logic)).

To obtain the \( Q, R \) numbers in Table I, we utilized Eqs 5,6 and the \( E, \tau \) data in Ref. [31]. However, as mentioned earlier, the benefit of the \( Q – R \) approach is \( Q, R \) can be easily estimated from device parameters. For most charge based devices, \( Q, R \) can be easily related to: \( Q \) is the charge that is stored in a capacitor involved in the switching event; while \( R \) is the resistance through which the capacitor is charged. Consider for example the case of CMOS-HP. The \( Q \) and \( R \) numbers (Table I) for CMOS-HP can be easily reconciled to by considering the numbers on the ITRS (International Technology Roadmap for Semiconductors [37]) roadmap for 15 nm MOSFETs, namely:

Supply voltage, \( V = 0.73 \) volts
On Current, \( I_{ON} = 1.805 \) mA/m
Intrinsic delay (\( \tau \))=0.25ps.

Assuming a width of \( W = 4F \) (F=15nm) =0.06 \( \mu \)m, we have

\[ Q = I_{ON} \tau \sim 168e \]

where \( e \) is the charge of an electron.

The resistance \( R = V_{DD}/I_{ON} = 6.7 \times 10^3\)Ω.

Hence \( Q^2 R = 0.0046J-\)ps \~7355h

where \( h \) is the Plank’s constant.

Analysis of the device from the \( Q – R \) viewpoint immediately suggests that to improve the performance of CMOS-HP or similar charge based devices, we should move towards devices with smaller resistance (or lower \( V_{DD} \), the same or slightly higher \( I_{ON} \)) and attempt to decrease the charge by lowering \( V_{DD} \) or by using a more efficient device which would allow switching with a smaller capacitance of the switch.

Relationship of \( Q \) to physical device parameters for electronic devices is easy to comprehend. We mentioned in the paper that \( Q \) can be related to physical device parameters for most devices, even for spintronic and magnetic devices e.g. All spin logic (ASL) device where the information is stored in the magnetization of magnets which communicate via spin currents. The \( Q \), in this case, is easily understood from Ref [40] which establishes that

\[ Q \sim \frac{2qN_s}{\eta} \] (7)
where $\eta$ is the efficiency related to the spin to charge current ratio, assumed to be 0.2 based on today’s devices; $N_s$ is the number of Bohr Magneton or spins comprising the magnet and is given in general by

$$N_s = \frac{2Ku_2\Omega}{\mu_BH_k},$$

where $Ku_2$ is the uniaxial anisotropy constant, $\Omega$ is the volume of the magnet such that $Ku_2\Omega$ is the energy barrier for magnet switching, $\mu_B$ is the Bohr Magneton and $H_k$ is the uniaxial anisotropy field. In Ref [31], Nikonov and Young assumed the barrier for magnet switching, $Ku_2\Omega = 90kT$, $H_k = 3T$ for ASL. This translates to $N_s \sim 15000$. Though this value of $N_s$ corresponds to a relatively small magnet compared to those used in spin-torque experiments (see for example Ref [31]), the corresponding Q is huge, contributing to the higher $E\tau$ of ASL and other spin torque switching based switches.

A similar exercise for relating the Q,R to physical device parameters can be done for almost all information processing devices. Such an exercise would help identify the device properties that should be changed to improve the $E\tau$ performance. The relationship of Q and R to physical device parameters for a few logic devices has been summarized in Table I. The expressions of Q,R can be easily derived from the discussion describing the operation of these devices presented in Ref [31].

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### Table I

| Device    | State Variable | Voltage $V_{(D)}$ V | Delay (τ) ps | Pulse width (τ$_{pu}$) ps | $E\tau = Q^2R(\tau/\tau_{pu})$ h | Charge (Q) e | Resistance (R) Ω |
|-----------|----------------|---------------------|--------------|---------------------------|------------------------------------|--------------|------------------|
| CMOS-HP   | Charge         | 0.7                 | 0.25         | 0.25                      | $7.4 \times 10^4$                  | 168          | $6.8 \times 10^4$ |
| CMOS-LP   | Charge         | 0.3                 | 92.08        | 92.08                     | $4.6 \times 10^5$                  | 69           | $2.5 \times 10^6$ |
| HEMT      | Charge         | 0.2                 | 3.27         | 3.27                      | $4.8 \times 10^4$                  | 1            | $1.3 \times 10^4$ |
| STT/DW    | Spin           | 0.01                | 1762.90      | 1762.90                   | $3.0 \times 10^8$                  | 69           | $1.6 \times 10^4$ |
| STLOGIC   | Spin           | 0.01                | 1000.00      | 1000.00                   | $5.3 \times 10^8$                  | 284          | 190              |
| STMG      | Spin           | 0.1                 | 297.61       | 0.25                      | $6.2 \times 10^4$                  | 86           | $1.8 \times 10^4$ |
| STT-triad | Spin           | 0.1                 | 298.03       | 0.67                      | $4.9 \times 10^6$                  | 682          | 615              |
| NML       | Spin           | 0.1                 | 297.61       | 0.25                      | $6.2 \times 10^4$                  | 86           | $1.8 \times 10^4$ |

### Table II

Q, R can be related to physical device parameters, even for devices with state variable other than charge. This allows improvement of $E\tau = Q^2R$ by tuning device parameters. (C-capacitance, NC-number of charges in the capacitator, $I_{ON}$-ON current, $N_s$-number of Bohr Magneton comprising a magnet, $\eta$-Injection Efficiency [30]; $R_{wire}$-required magnetic induction from a wire, $\mu_m$-wire permeability, $R_{wire}$-required magnetic switching time of nanomagnets in an array, $\mu_m$-Permeability of Vacuum, $R_{coil}$-resistance, $R_{wire}$-resistance of the interface between the magnet and the channel, $I_{on}$-current required to change the polarization of the piezoelectric material, $R_{wire}$-resistance, $A$-area of magnet).

#### Switching of magnet with current

- Spin torque (e.g. ASL) $\frac{2QN_s}{\eta} R_{wire}$
- Magnetic field (NML) $2eV_{on}/I_{on}$

#### Voltage switching of magnet

- NML, SMG, SWD, STT trial $P_{bias}A + CV_{DD}$
- $V_{DD}/I_{on}$

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