Configurable Independent Component Analysis Preprocessing Accelerator
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Abstract—Independent component analysis (ICA) has been used in many applications, including self-interference cancellation for in-band full-duplex wireless systems and anomaly detection in industrial internet of things. This paper presents a high-throughput and highly efficient configurable preprocessing accelerator for the ICA algorithm. The proposed ICA accelerator has three major blocks that perform data centering, covariance matrix for computation, and eigenvalue decomposition (EVD). Specifically, the proposed accelerator is based on a high-performance matrix multiplication array (MMA). The proposed MMA architecture uses time-multiplexed processing so that the efficiency of hardware utilization is greatly enhanced. Furthermore, the processing flow utilizes parallel processing such that the centering, the calculation of the covariance matrix, and EVD are conducted simultaneously and are individually pipelined to maximize throughput. This paper presents the architecture, circuit design, and performance estimates based on post-layout extraction of the proposed preprocessing ICA accelerator. The proposed design achieves a throughput of 40.7 kMatrices per second at complexity of 73.3 kGE.

I. INTRODUCTION

The blind source separation (BSS) problem lies in the separation of a mixed-signal which is a combination of many independent sources. For instance, the cocktail problem, where individual voice signals of multiple speakers need to be separated is a well-known BSS problem. In the BSS problem, the mixed signal is constructed by mixing independent source signals through an unknown channel. Without prior knowledge of the mixing channel, independent source signals can be separated only by observing the mixed received signals [1]. In this context, independent component analysis (ICA) algorithm is one of the most widely used approaches for separating source signals in BSS problems [1]–[3]. The ICA algorithm separates the mixed-signal by taking advantage of the statistical independence and non-Gaussian properties of source signals [1]. The ICA algorithm has been applied in many applications. For example, it is proposed in [4], [5] that the self-interference cancellation (SIC) for the In-Band Full-Duplex (IBFD) wireless communication system can be considered a BSS problem. The ICA algorithm is applied to separate the self-interference signal and the signal of interest. Furthermore, the ICA algorithm is applied to separate multiple superimposed signals to identify the cyclic features of each transmitted signal in cognitive radio (CR) system [6].

Recently, it is proposed in [7], [8] that ICA can be used in a temporal-critical industrial internet of things (IoT) application for anomaly detection or identification. A common theme of these previous use cases is that the source signals are expected to be extracted in real-time thus demanding high-performance ICA architectures.

The ICA algorithm has two main stages: the preprocessing stage and the iterative stage [1], [3], [9]. ICA preprocessing aims to whiten the received signal so that the correlation between the signals is reduced. The whitened received signal is sent to the iterative stage where the demixing matrix is estimated and the mixed signals are separated. The preprocessing stage is an essential step in ICA, as it enhances the quality of the separated signals and accelerates the convergence in the iterative stage. However, ICA preprocessing requires several highly complex vector and matrix computations, including the calculation of the covariance matrix and the eigenvalue decomposition (EVD). According to our simulation profiling, discussed in detail in Section II.A, based on the system in [4], [5], preprocessing occupies between 17.3% to 46.9% of ICA processing time for different targeted SIC performance. Therefore, designing an efficient preprocessing accelerator is a great challenge in realizing efficient ICA circuits and systems.

Several VLSI architecture designs for ICA preprocessors have been reported in the literature. Reference [10] proposed an ICA-based signal separation architecture for a biomedical application. The preprocessor in this design is based on a serial processing flow, which results in a very low processing speed. While in [11], a low-power ICA processor was proposed to improve the processing throughput of the EVD in the ICA preprocessor based on a highly parallel systolic array structure. However, the area complexity of the preprocessor occupies about 90% of the entire ICA system. Furthermore, [12] and [13] reported an improved ICA architecture that benefits from parallel processing. However, the processing flow of the proposed preprocessor is still inherently sequential in nature and thus, cannot achieve high throughput.

A common drawback of many ICA preprocessors described in the literature is that they only support real-valued signals and operate at low processing speeds. However, new applications of ICA in use cases such as wireless communications [16]–[18] where high data rates, latency-sensitive [7], [8], complex-valued samples are common demand novel, high throughput ICA architectures.

This work presents a configurable, high-throughput, and highly efficient ICA preprocessing accelerator. The main contributions of this paper are summarized as follows:
• A novel ICA preprocessing accelerator that can perform centering, covariance, and EVD is presented. The proposed architecture supports complex-valued signals whereas the number of received signals and sample lengths is configurable.
• A high-performance matrix multiplication array (MMA) is presented. The proposed MMA architecture uses time-multiplexed processing, such that the hardware utilization is greatly enhanced. Therefore, compared to prior designs, the proposed MMA unit achieves high processing throughput with low area complexity.
• A low-latency centering unit and covariance unit based on the proposed MMA are presented. The operating flow is highly improved, so that the centering and calculating of the covariance matrix can be performed in parallel.
• A highly efficient EVD unit is proposed. The designed EVD engine is optimized for processing Hermitian matrices and has a low processing latency.
• Experimental results show that the proposed preprocessor outperforms prior designs. It achieves high throughput with reduced area and higher efficiency (defined as a throughput to gate count) compared to prior work.

The remainder of this paper is organized as follows. The background of ICA and preprocessing for ICA are introduced in Section II. The proposed centering and covariance units are presented in Section III and the proposed EVD unit is described in Section IV. The experimental results and comparisons with prior designs are given in Section V. Conclusions are drawn in Section VI.

II. BACKGROUND AND RELATED WORK

This section introduces the basic concepts of the ICA. The state-of-the-art ICA designs with focus on preprocessors are also reviewed.

A. The Basic Concept of ICA and the ICA Preprocessing

Considering the BSS problem, the received signal is constructed by mixing independent source signals through an unknown channel. Without prior knowledge of the mixing channel, independent source signals can be separated only by observing the mixed received signals \( Y \). The ICA algorithm is the most widely used approach for separating source signals in BSS problems \([1]–[3]\). In the ICA algorithm, the mixed signals are separated by utilizing the statistical independence and non-Gaussianity of the source signals. Furthermore, the number of observed signals must be equal to the number of source signals, so in the generic ICA representation the mixed received signals and the source signals can be expressed in matrix form as follows:

\[
Y = \begin{bmatrix}
Y_1 \\
Y_2 \\
\vdots \\
Y_N
\end{bmatrix} =
\begin{bmatrix}
h_{11} & h_{12} & \ldots & h_{1N} \\
h_{21} & h_{22} & \ldots & h_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
h_{N1} & h_{N2} & \ldots & h_{NN}
\end{bmatrix}
\begin{bmatrix}
X_1 \\
X_2 \\
\vdots \\
X_N
\end{bmatrix} = Y = \begin{bmatrix}
X_1 \\
X_2 \\
\vdots \\
X_N
\end{bmatrix} = \mathbf{H}X \quad (1)
\]

where \( Y \) and \( X \) are the mixed received signals and the source signals, respectively. \( Y_i \) and \( X_i \) are both row vectors with \( M \) elements where \( M \) is the sample length. The matrix \( \mathbf{H} \) has size \( N \times N \), where \( N \) is the number of signals. After receiving the mixed received signals \( Y \), the ICA estimates a demixing matrix \( \mathbf{W} \) and uses it to separate the received signals. The separated signals \( \hat{X} \) can be defined as follows:

\[
\hat{X} = \begin{bmatrix}
\hat{X}_1 \\
\hat{X}_2 \\
\vdots \\
\hat{X}_N
\end{bmatrix} = \begin{bmatrix}
w_{11} & w_{12} & \ldots & w_{1N} \\
w_{21} & w_{22} & \ldots & w_{2N} \\
\vdots & \vdots & \ddots & \vdots \\
w_{N1} & w_{N2} & \ldots & w_{NN}
\end{bmatrix}
\begin{bmatrix}
Y_1 \\
Y_2 \\
\vdots \\
Y_N
\end{bmatrix} = \mathbf{W}Y \quad (2)
\]

where the demixing matrix \( \mathbf{W} \) is the inverse of the mixing matrix, assuming the estimation is perfect.

In band full-duplex (IBFD) can be considered as a prime example application that demands high performance ICA architectures \([4], [5]\), where the successive interference cancellation (SIC) in IBFD systems is considered as a BSS problem. In this case, the ICA algorithm is applied to separate the self-interference signal (SI) and the signal-of-interest (SOI). It is shown in \([4]\) that the received signal that contains the mixture of SOI and SI and a direct feedback digital transmitted signal are the input to the ICA algorithm. Thus, the BSS problem can be formulated as follows:

\[
\begin{bmatrix}
Y_{si} \\
Y_{mix}
\end{bmatrix} = \begin{bmatrix}
1 & 0 \\
H_{ord} & H_{soi}
\end{bmatrix}
\begin{bmatrix}
X_{si} \\
X_{soi}
\end{bmatrix} \quad (3)
\]

where \( Y_{si} \) and \( Y_{mix} \) are the two input signals to the ICA algorithm. The signal \( Y_{si} \) is the direct input from the SI signal \( X_{si} \) whereas \( Y_{mix} \) is the mixture of the SI and the SOI signal \( X_{soi} \). The \( H_{ord} \) and \( H_{soi} \) denote the SI and SOI channels respectively. The ICA algorithm then estimates the demixing matrix and separate the SI and SOI signals. The simulation results shown in \([4]\) illustrate that the output SINR of the ICA-based SIC scheme outperforms the conventional SIC approach. Furthermore, it is shown in \([5]\) that different ICA algorithms such as FastICA \([3]\) or ICA-EBM \([9]\) can be applied to this ICA-based SIC scheme.

In ICA, the demixing matrix is estimated by searching for orthogonal vectors iteratively. Prior work in literature \([1], [3], [9]\) shows that including a preprocessing stage before searching for the orthogonal vectors is crucial for reducing the number of iterations required and for improving the quality of the estimated demixing matrix.

The main purpose of ICA preprocessing is to whiten the received signal as shown in Fig. I. In the first step of ICA preprocessing, the received signals are centered by subtracting the mean of signals, described as follows:

\[
\hat{Y}_i = Y_i - E\{Y_i\} \quad (4)
\]

Specifically, \( \hat{Y}_i \) and \( E\{Y_i\} \) are the \( i \)-th centered mixed received signal and its mean, respectively. The second step of preprocessing stage is whitening where the centered signals are whitened to have unit variance. In order to whiten the centered signals, the covariance matrix is calculated first as follows:

\[
Y_c = E\{\hat{Y}\hat{Y}^H\} \quad (5)
\]

where \( Y_c \) is the covariance matrix of the centered signals, which is also a \( N \times N \) Hermitian matrix. In the following, the EVD is performed on the covariance matrix as follows:
Numerous VLSI architectures for ICA and ICA preprocessors have been reported in the literature. Reference [10] proposes a real-valued signal separation architecture based on the FastICA algorithm. The preprocessor in this architecture has a centering unit, a covariance unit, and an EVD engine. Since the units in this preprocessor operate in a very sequential manner, the latency is extended. Specifically, the centering and covariance unit sequentially access the same memory several times, leading to very long delays. According to our analysis, for $N$ complex-valued received signals and a sample length of $M$, a total of $8 \times N \times M + 6 \times M \times N \times N$ cycles are consumed by the centering and covariance units of [10]. Furthermore, to increase the throughput, parallelism is introduced in the preprocessor in [19]. An MMA based on a systolic array structure is proposed in this design for calculating the covariance matrix. This MMA uses a real-valued matrix with a size of $3 \times 64$. It takes three cycles to multiply a column vector and a row vector. However, the utilization of the MMA is not optimized, especially for complex-valued matrices. In addition, in [12] and [13], the preprocessor has to share computing units, resulting in excessive processing delays.

Moreover, the EVD engine is one of the core units in the ICA preprocessor and has a high degree of complexity. An EVD unit in the preprocessor based on the approximate Jacobi algorithm was presented in [11]. This EVD unit has very long critical path and results in low operating frequency. A configurable SVD unit based on the CORDIC operation and folded systolic array structure was described in [14]. Although these authors produced a low-complexity circuit, the processing had high latency and was slow. Furthermore, a sorting network was proposed in [15] to enhance the efficiency of memory accesses in the EVD architecture. However, a matrix multiplier was employed in this design to perform matrix rotations, which resulted in high area complexity.

Modern wireless communication systems operate at a data rate of hundreds of megabits per second [16]–[18] with complex-valued signals. Furthermore, IoT applications usually require strict real-time processing [7], [8]. Therefore, it is crucial to design a high-throughput ICA preprocessor for these systems. No relevant improvements for the operational flow and architecture of ICA preprocessors have been reported in the literature. To achieve a high-throughput and highly efficient ICA preprocessor, in this work, we design the architecture by jointly considering the operational flow and circuit structure for the centering, covariance, and EVD units. The proposed centering and covariance units are operated in parallel so that the processing throughput is much higher. Furthermore, the covariance unit is based on a proposed novel highly efficient MMA circuit. To reduce the amount of computation, a novel diagonalization process for a Hermitian matrix was designed for the EVD. In addition, we would like to point out that the proposed preprocessor can be used in different ICA algorithms that have been proposed in literature such as [1], [3], [9].

![Operational flow in ICA preprocessing.](image)

**Fig. 1: Operational flow in ICA preprocessing.**

| Processes       | Iteration=5 | Iteration=15 | Iteration=25 |
|-----------------|-------------|--------------|--------------|
| Centering       | 11.1        | 5.2          | 4.2          |
| Covariance      | 11.1        | 5.9          | 4.1          |
| EVD             | 9.1         | 4.8          | 3.3          |
| Whitening       | 15.4        | 8.4          | 5.7          |
| Preprocessing   | 46.9        | 25.3         | 17.3         |
| Iteration       | 53.1        | 74.7         | 82.7         |

**TABLE I: The Normalized Execution Time (%) for FastICA Algorithm**

\[ Y_c = EDE^H \]  \hspace{1cm} (6)  
\[ Z = D^{-1/2}E^H \bar{Y} \]  \hspace{1cm} (7)
III. THE PROPOSED CENTERING AND COVARIANCE UNITS

A. The Proposed Efficient MMA Architecture

A matrix multiplication unit (MMA) is presented in [19] to compute the multiplication of a real-valued $3 \times 64$ matrix with its transpose. The structure of this MMA is shown in Fig. 2(a) for calculating equations as follows

$$
\begin{bmatrix}
    u_{1,1} & \cdots & u_{1,64} \\
    u_{2,1} & \cdots & u_{2,64} \\
    u_{3,1} & \cdots & u_{3,64}
\end{bmatrix}
\begin{bmatrix}
    u_{1,1} & u_{2,1} & u_{3,1} \\
    \vdots & \vdots & \vdots \\
    u_{1,64} & u_{2,64} & u_{3,64}
\end{bmatrix}

= 
\begin{bmatrix}
    u_{1,1}u_{1,1} + \cdots + u_{1,64}u_{1,64} \\
    u_{2,1}u_{1,1} + \cdots + u_{2,64}u_{1,64} \\
    u_{3,1}u_{1,1} + \cdots + u_{3,64}u_{1,64}
\end{bmatrix}
\begin{bmatrix}
    u_{1,1}u_{1,1} + \cdots + u_{1,64}u_{3,64} \\
    u_{2,1}u_{1,1} + \cdots + u_{2,64}u_{3,64} \\
    u_{3,1}u_{1,1} + \cdots + u_{3,64}u_{3,64}
\end{bmatrix}

(8)
$$

The operation flow of applying this MMA [19] to a complex-valued $3 \times 64$ matrix is shown in Fig. 2(b). It is shown in Fig. 2(b) that the PEs are not efficiently utilized as they are idled in multiple cycles. Furthermore, there is only one multiplier in each row as shown in Fig. 2(a) and four real-valued multiplications are needed for one complex-valued multiplication. As a result, a total of $3 \times 64 \times 4 = 768$ cycles are consumed.

In this work, an efficient complex-valued MMA (ECMMA) is employed in centering and covariance units in the preprocessor where the architecture is shown in Fig. 3(a) assuming a $3 \times 64$ matrix. It is noted that the architecture, shown in Fig. 3(a), is based on the example of a $3 \times 64$ matrix for a fair comparison with the design shown in [19]. It is shown in Fig. 3(a) that three complex-valued multipliers are used instead of the original real-valued multiplier to process the real and imaginary parts of the covariance matrix. Since the proposed ECMMA directly performs complex-valued operations, the real and imaginary parts of the elements in the covariance matrix are computed concurrently. Thus, one cycle is consumed by the PE in the accumulation of the real and imaginary parts of the element. Furthermore, it is shown in Fig. 3(a) that one column of PEs is designed where three registers and one multiplexer and demultiplexer are contained in the PE. Specifically, each PE in the proposed MMA is utilized to compute and store the multiply-and-accumulate (MAC) for different columns of data using time-multiplexing. Figure 3(b) shows operational flows for the proposed ECMMA assuming the $3 \times 64$ matrix. It can be seen from Fig. 3(b) that due to the time-multiplexed utilization of the PE, the efficiency of the proposed MMA is much higher. In particular, a total of $3 \times 64 = 192$ cycles are consumed.

Table 1 compares the number of hardware elements in the proposed efficient MMA and the MMA in [19] for an $m \times n$ complex-valued matrix. This table shows that, although additional multiplexers are needed, the number of adders is much lower. Moreover, the number of adders required for the MMA of [19] increases exponentially with the size of the matrix, whereas the number of adders for the proposed efficient MMA increases linearly.

| TABLE II: Comparison of MMAs | MMA of [19] | Proposed MMA |
|-----------------------------|-------------|--------------|
| Matrix size                 | $m \times n$| $m \times n$|
| PEs                         | $2 \times m^2$ | $2 \times n$ |
| Adders                      | $2 \times m^2$ | $2 \times m$ |
| Multiplexors                | $0$         | $4 \times m$ |
| Registers                   | $2 \times m^2 + 2 \times m$ | $2 \times m^2 + 2 \times m$ |
| Cycles                      | $m \times n$ | $m \times n$ |
B. The Proposed Centering and Covariance Units

As mentioned in Section III-A, the prior centering and covariance units sequentially access the memory multiple times and incur excessive delays. To achieve high-throughput preprocessing for the ICA, this work optimizes the operational flow so that the centering unit and the covariance unit run in parallel. Furthermore, the covariance unit is based on the proposed efficient ECMMA, which strikes a balance between high speed and low complexity. In particular, \( N \) received signals lead to a \( N \times N \) Hermitian covariance matrix, and the proposed operational flow is based on the characteristic of the Hermitian matrix. The main idea is that the Hermitian covariance matrix has three different parts, and the elements in each part are generated at different stages by different approaches. Figure 4 is an example of an \( 8 \times 8 \) Hermitian covariance matrix \( \mathbf{Y}_c \) assuming eight received signals where \( \mathbf{Y}_1 \) denotes the \( i \)-th row vector in the centered received signals \( \bar{\mathbf{Y}} \). The lower-triangular elements highlighted in red in Fig. 4 do not need to be calculated. Furthermore, the elements highlighted with solid lines, such as \( y_{c11}, y_{c12}, \) and \( y_{c22} \), can be computed once the centered signals \( \bar{\mathbf{Y}}_1 \) and \( \bar{\mathbf{Y}}_2 \) are generated. Therefore, in this design, a novel processing flow is proposed so that the elements highlighted with solid lines are computed concurrently with the operation of the centering unit while other centered signals, such as \( \bar{\mathbf{Y}}_3 \) and \( \bar{\mathbf{Y}}_4 \), are being generated. Finally, the remaining upper-triangular elements, such as those highlighted with dotted lines, are decomposed as \( 2 \times 2 \) submatrices and each submatrix is processed independently. Considering a case with \( N \) received signals, the number of \( 2 \times 2 \) submatrices is \( (N^2 - 2 \times N)/8 \). The proposed design is based on the processing flow with a high degree of regularity and can be applied to any covariance Hermitian matrix with an even number of received signals.

Based on the proposed processing flow, the architecture of the centering and covariance units is presented in Fig. 5. It is shown in Fig. 4 that, for a \( 2 \times 2 \) matrix, the centering unit has four centering components (CCs) and the covariance unit has one diagonal submatrix component (DSC) and one ECMMA. The DSC computes those elements shown in solid lines in Fig. 4 whereas the ECMMA unit computes the elements shown in dashed lines. Furthermore, the four CCs compute two complex-valued signals concurrently. Each CC sequentially accumulates data from the input signal and calculates the average value. The same signal is then read by the next CC in the sequence and the average value is subtracted to generate the centered signal. The centered signal is output in sequence and is both written into the memory and sent to the DSC in the covariance unit. Therefore, based on the proposed processing flow, the centering unit outputs the centered data in sequence while the DSC in the covariance unit calculates elements of the covariance matrix at the same time. After all the received signals have been centered and the elements in each L-shaped region marked by a solid line in Fig. 4 have been calculated by the DSC, the elements in the squares marked with a dotted line continue to be calculated through the ECMMA in the covariance unit. Given \( N \) received signals, the ECMMA unit calculates \( (N^2 - 2 \times N)/8 \) submatrices in sequence. Furthermore, it can be seen that the centering and covariance operations overlap in time and the elements of covariance matrix are generated as soon as possible. Therefore, the throughput of the overall architecture is greatly enhanced.

Figure 6 shows a detailed timing diagram for the proposed centering and covariance units assuming \( N \) received signals and the sample length is \( M \). After taking \( (N \times M)/2 \) cycles to write received signals into the received memory, row vectors \( \mathbf{Y}_1 \) and \( \mathbf{Y}_2 \) are read by the four CCs in the centering unit in sequence to calculate the average values where \( M \) cycles are consumed. The vectors \( \mathbf{Y}_1 \) and \( \mathbf{Y}_2 \) are read again and the average values are subtracted to generate the centered signals of \( \bar{\mathbf{Y}}_1 \) and \( \bar{\mathbf{Y}}_2 \) by taking \( M \) cycles. It is shown in Fig. 6 that \( N \times M \) cycles are consumed by the centering unit given \( N \) received signals and the sample length is \( M \). The centered signals are saved into the memory and sent to the DSC of the covariance unit at the same time. While the centering unit is centering the data, the DSC takes \( M \) cycles to calculate \( y_{c11} \) and \( y_{c22} \) for the covariance matrix. In particular, the \( N \times N \) Hermitian covariance matrix is decomposed as diagonal submatrices and \( 2 \times 2 \) off-diagonal submatrices, whereas the DSC computes diagonal terms in the covariance matrix. The block diagram of DSC is shown in Fig. 5, which is composed of a complex multiplier and two accumulators. Since the diagonal elements is the multiplication of the variable with its complex conjugate, the result must be a real number. Thus, the imaginary part of the computation can be omitted. Therefore, the computation of \( y_{c11} \) and \( y_{c22} \) can be calculated concurrently. Subsequently, the centering unit reads vectors \( \mathbf{Y}_3 \) and \( \mathbf{Y}_4 \) sequentially and performs the accumulation. Since the centering unit does not write any data to the memory at this time, the DSC reads \( \bar{\mathbf{Y}}_3, \bar{\mathbf{Y}}_2, \bar{\mathbf{Y}}_1, \) and \( \bar{\mathbf{Y}}_2 \) from the memory and calculates \( y_{c12} \) for the covariance matrix. It can be observed from Fig. 6 that while the centering operations are being performed on all \( N \) complex signals, \( (N/2) \times 3 \) out of \( ((1 + N) \times N)/2 \) elements in the covariance matrix (i.e., those in the L-shaped region marked by a solid line in Fig. 4) are computed at the same time. A total of \( N \times M \) cycles are consumed by the DSC given \( N \) received signals and the
sample length is \( M \).

The remaining covariance elements are decomposed into \((N^2 - 2 \times N)/8\) 2 \( \times \) 2 submatrices and are processed by the ECMMA unit. It is shown in Fig. 6 that 2 \( \times \) \( M \) cycles are consumed by the ECMMA unit for calculating four elements. Furthermore, considering \( N \) for each sample. Thus, it is shown in Fig. 6 that the processing of the centering and covariance units overlap for the second matrix while the ECMMA unit is processing. Figure 6 shows the processing of a \( 2 \times 2 \) ECMMA for the first matrix and the processing of the centering and covariance units overlap for the second matrix. The covariance matrix is generated every \((N^2 \times M - 2 \times N \times M)/4\) cycles assuming \( N \geq 8 \). For example, the covariance matrix is computed every 6144 cycles for an \( 8 \times 512 \) complex-valued matrix. Therefore, based on the architecture and the operational flow, a balance between the high-throughput and low-complexity can be achieved.

C. Configurability of Centering and Covariance Units

It is noted that the proposed processing flow of the centering and covariance units shown in Fig. 6 is applied to any covariance Hermitian matrix with an even number of received signals without changing the architecture presented in Fig. 5. In other words, the same architecture is applied with different matrices sizes whereas the operating cycles are adaptive to the size of signals. To be specific, given \( N \) received signals and the sample length is \( M \), the proposed centering unit is operated to accumulate \( M \) samples and to calculate the mean. The centered result is computed by subtracting the mean value for each sample. Thus, it is shown in Fig. 6 that \( N \times M \) cycles are consumed by the centering unit presented in Fig. 5 to calculate centered results. Similarly, \( N \times M \) cycles are consumed by the DSC in Fig. 5 to calculate the diagonal values. Furthermore, considering \( N \) received signals, a \( N \times N \) Hermitian covariance matrix has resulted. The number of \( 2 \times 2 \) off-diagonal submatrices is then \((N^2 - 2 \times N)/8\) according to Fig. 4. The ECMMA unit presented in Fig. 5 calculates the \((N^2 - 2 \times N)/8\) submatrices in sequence. Thus, based on the architecture shown in Fig. 5 the covariance matrix is generated every \((N^2 \times M - 2 \times N \times M)/4\) cycles assuming \( N \geq 8 \). Therefore, to process with different sizes of input data, the controller and finite state machine (FSM) in the proposed design are realized such that data sizes are treated as parameters and the operating cycles are adaptive to those parameters. For example, the covariance matrix is computed in every 6144 cycles for an \( 8 \times 512 \) complex-valued matrix and in every 5120 cycles for an \( 10 \times 256 \) complex-valued matrix.

IV. PROPOSED EVD UNIT

A. Proposed EVD Design

The most commonly used approach for EVD is based on the Jacobi algorithm [11], [15] where a series of rotation transformations is exploited to find the eigenvalues and eigenvectors of a matrix. Specifically, in the Jacobi algorithm, an \( N \times N \) matrix is decomposed into multiple \( 2 \times 2 \) submatrices and the submatrices that are on the diagonal of the matrix (known as diagonal submatrices) are diagonalized. Those non-diagonal submatrices are rotated according to the angles of the diagonalization process. This diagonalization-rotation process is performed iteratively.

In the ICA preprocessing, the input to the EVD unit is the Hermitian covariance matrix. The covariance matrix is decomposed into multiple \( 2 \times 2 \) submatrices and, to achieve an optimized balance between throughput and complexity, the proposed EVD unit fully utilizes the Hermitian properties in the design of the processing sequence and the architecture for the diagonalization and rotation of a \( 2 \times 2 \) submatrix. The
proposed processing sequence is presented in Fig. [7] It requires five stages for the EVD diagonalization of a $2 \times 2$ submatrix. Note that this $2 \times 2$ submatrix is the diagonal submatrix of the covariance matrix, so it must be Hermitian. In other words, the non-diagonal elements $p_{12}$ and $p_{21}$ in Fig. [7] are complex conjugates of each other. The processing sequence is based on calculating the angle and the matrix rotation. Stages 1 and 2 eliminate the imaginary parts of $p_{12}$ and $p_{21}$ in the submatrix. The rotation angle $\theta$ is computed accordingly. In the following stage 3, the corresponding rotation angle $\phi$ is computed. Finally, stages 4 and 5 eliminate the non-diagonal elements of the submatrix, resulting in a diagonal $2 \times 2$ submatrix. Note that, since the $2 \times 2$ submatrix is a Hermitian matrix, the diagonal elements have real values. As a result, all the elements in the submatrix will be real after stage 2. Furthermore, since the non-diagonal elements are complex conjugates of each other, the rotation angle $\theta$ needs to be computed only once.

Figure [8] presents the architecture of the proposed EVD unit to process the flow shown in Fig. [7]. There are CORDIC elements in each stage, and it is architected as a 10-cycle pipeline. In this figure, DR and DI are the real and imaginary parts of the eigenvalues, and ER and EI are the real and imaginary parts of the eigenvectors, respectively. A subscript represents the corresponding position in the submatrices. $D$ is initialized to the value of the submatrix, and $E$ is initialized to the identity matrix. The diagonal $2 \times 2$ submatrices are sent into the EVD unit one by one. In stage 1, the first CORDIC operates in vectoring mode and obtains the right-hand side (RHS) rotation direction. The corresponding RHS rotations are performed by the other three CORDICs based on the direction provided by the first CORDIC. Thus, the imaginary part of $D_{12}$ is eliminated. Since $D_{12}$ and $D_{21}$ are complex conjugates of each other, in stage 2, two CORDICs perform the left-hand side (LHS) rotation on the submatrix using the same rotation direction as stage 1. The imaginary part of $D_{21}$ is eliminated in stage 2 and the diagonal $2 \times 2$ submatrix is transformed into a real symmetric matrix. In stage 3, the CORDIC calculates the rotation angle to eliminate the non-diagonal elements of the submatrix for the subsequent stages. In stage 4, the first...
CORDIC performs the LHS rotation with the rotation angle calculated in stage 3 and provides the rotation direction for the other three CORDICs. In stage 5, eight CORDICs perform the RHS rotation to eliminate the non-diagonal elements based on the rotation direction generated by stage 4. Therefore, each diagonal 2 × 2 submatrix can be converted into a real-valued diagonal matrix. After all diagonal 2 × 2 submatrices have been so converted, the non-diagonal 2 × 2 submatrices are input one by one, and the corresponding rotation is performed by the EVD unit operating in rotation mode. The rotation of a non-diagonal 2 × 2 submatrix is through the corresponding rotation direction and angle.

B. EVD Processing Sequence

The EVD of an \(N \times N\) matrix is an iterative process involving the diagonalization of 2 × 2 diagonal submatrices and the corresponding rotations of 2 × 2 non-diagonal submatrices. How those 2 × 2 diagonal and non-diagonal submatrices are constructed and the processing order affect the efficiency of the EVD \([15]\). To accelerate the iterative process, a concept of parallel ordering \([14]\) has been widely applied and is illustrated in Fig. 9(a) for the example of an 8 × 8 matrix.

According to the parallel ordering \([14]\), the 8 × 8 matrix is decomposed into seven orderings, each of which has four 2 × 2 diagonal submatrices. These submatrices can be diagonalized simultaneously without interfering with each other. The notation \((i,j)\) in Fig. 9(a) denotes the 2 × 2 diagonal submatrix with elements at \((i,i), (i,j), (j,i), \) and \((j,j)\) in the 8 × 8 matrix. For example, given the 8 × 8 matrix with elements \(h_{ij}\) where \(i\) is the row and \(j\) the column, the notation \((1,2)\) represents the 2 × 2 submatrix of elements \([h_{11}, h_{12}; h_{21}, h_{22}]\).

In each ordering, the diagonalization processes for the 2 × 2 diagonal submatrices are independent of each other, and thus, can be conducted in parallel. For example, the diagonalization of the four 2 × 2 submatrices \((1,2), (3,4), (5,6), (7,8)\) are conducted in parallel in ordering 1.

In this design, each ordering is processed by the proposed EVD engine in a pipelined fashion. However, the sequence for rotating the non-diagonal submatrices also affects the efficiency of the EVD and needs to be optimized. To reduce the latency and improve the throughput, a novel processing flow for the EVD is also proposed in this work. Figure 8 shows that the proposed EVD unit has five stages so that five 2 × 2 submatrices are processed concurrently in a pipeline. To achieve this, the ordering for processing different submatrices needs to be specially designed. In particular, each ordering is processed based on the result from the prior ordering. For example, the calculations for ordering 2 cannot start until all the submatrices of ordering 1 have been output. This results in processing delays between the orderings. To reduce the latency, this design proposes a processing sequence such that the data dependency between two orderings can be eliminated and the efficiency can be significantly enhanced. Consider an 8 × 8 matrix. The matrix that is reconstructed based on the parallel ordering is illustrated in Fig. 9(b). Orderings 1 and 2 are shown as examples. Each 2 × 2 submatrix in the reconstructed matrix of Fig. 9(b) is denoted as \(S_i\). The proposed processing sequence for processing the 2 × 2 submatrix in each ordering is shown in Fig. 9(c).

Figure 10 depicts the timing analysis diagram for EVD for an 8 × 8 matrix using the proposed EVD architecture and based on the proposed sequence shown in Fig. 9. The submatrix is input to the EVD unit according to the parallel ordering and the designed processing sequence for every ten cycles. The main purpose of the proposed processing sequence is to make the beginning of the processing for each new ordering and the end of the processing for each previous ordering independent. Figure 10 shows that the processing of the last four submatrices for ordering 1 and the processing of the first four submatrices for ordering 2 can be performed in parallel. This greatly enhances the efficiency of the proposed pipelined EVD engine. Before the calculation of ordering 2, there must be a 40-cycle idle time to avoid a data hazard. However, by sorting the input submatrices, ordering 2 can be calculated before the submatrices of ordering 1 are completely output and no data hazard will occur. Finally, the last block to perform the whitening is presented in Fig. 11. The CORIC unit in this block calculates the inverse square root of the diagonal entries of the D matrix and the 2 × 2 ECMMA units compute the multiplications of the matrices.

C. Configurability of EVD and Whitening Units

The proposed EVD operational flow and timing analysis shown in Fig. 9 and Fig. 10 can support different matrices sizes without changing the hardware structure. In other words, the controller and FSM of the proposed EVD unit control the operating cycles according to the parameter of \(N\). For an \(N \times N\) matrix, the \(N/4\) 2 × 2 submatrices are sent into the EVD unit to be processing according to the order shown in Fig. 9(c). Considering an \(N \times N\) matrix, the total processing time for the EVD unit can be approximately calculated as \((N^2/4) \times (N - 1)\) × 10. Similarly, the whitening unit processes with different parameters of \(N\) using different numbers of clock cycles based on the same hardware structure. Once the EVD Unit is completed, the CORDIC in the whitening
in [10], the area complexity was estimated to be 2.76 kGE. Furthermore, according to Figs. 2 and 18 in that paper. Furthermore, according to Figs. 2 and 18 in the designs. For example, the latency of the centering and covariance parts of the system were estimated for the prior work [10], [11], [13]. Since the implementation results reported in the literature are for the entire ICA system, the latency and complexity for the centering and covariance units operate in a parallel and pipelined fashion. Moreover, the floating-point design of [13] has a higher throughput and lower latency compared with the designs of [10] and [11]. Furthermore, since the design in [13] has multipliers doubled and the matrix type is complex-valued, the latencies were increased by eight times compared to the designs of [10] and [11] due to a difference in the data widths. Moreover, the design of [13] processes real-valued 8 × 1024 data using four parallel computing units. The complexity is based on Table I and the layout of Fig. 4.5 in [13]. In addition, since the designs in [10], [11], and [13] use serialized processing, the throughput was calculated as the processing latency. For a fair comparison, the latencies for the prior designs were scaled for a complex-valued 8 × 512 matrix. We assumed that the architectures of the prior designs were unchanged. The processing time was scaled according to the type and size of the matrix. A real-valued multiplier executes four times for a complex-valued multiplication. Thus, since the matrix size is doubled and the matrix type is complex-valued, the latencies were increased by eight times compared to the designs of [10] and [11]. Furthermore, since the design in [13] has multipliers operating in parallel, the latency was the same for a reduced-size complex matrix. 

Table IV shows that the proposed design achieves much higher throughput and lower latency compared with the designs of [10] and [11], although at the cost of slightly increased area complexity. This is because these designs are based on serialized processing architectures, whereas the proposed covariance and centering units operate in a parallel and pipelined fashion. Moreover, the floating-point design of [13] has a larger number of signals than eight and the sample length is 512. Thus, the area complexity of the complete timing diagram for the implemented preprocessor is 73.3 kGE in terms of two-input NAND gates with 30 kB of on-chip single-port SRAM.

Based on the proposed operational flow and architecture, an ICA preprocessor was designed and implemented. The preprocessor was synthesized, and placed-and-routed using the TSMC 90 nm process with a nominal power supply voltage of 1.1 V. Table III reports estimates for the operating frequency, latency, throughput, and complexity based on the post-layout simulations. It is noted that the proposed architecture is configurable for different numbers of signals \( N \) and sample lengths \( M \). The memory size limits the largest size of the sample lengths \( M \) that can be supported and the estimates summarized in Table III is based on the memory size supports up to a sample length of 512. Thus, the area complexity of this preprocessor is 73.3 kGE in terms of two-input NAND gates with 30 kB of on-chip single-port SRAM. Figure 12 is the complete timing diagram for the implemented preprocessor assuming number of signals is equal to eight and the sample length is 512. The figure shows that 6144 and 4480 cycles are consumed for the centering and covariance units and the EVD unit, respectively. Furthermore, the whitening unit is operated in parallel with the other units. Therefore, a throughput of 40.7 kMatrices per second with a latency of 78.33 µs is achieved given the operating frequency of 250 MHz. The processing time can be scaled with the values of \( N \) and \( M \) according to the timing diagram of Figs 6, 10, and 12. For example, assuming \( N = 16 \) and \( M = 512 \), the latency will be 94976 cycles for the proposed preprocessor. The corresponding latency and throughput are summarized in Table III. Figure 13 shows the layout of the proposed preprocessor including centering, covariance, EVD, and whitening units of which architectures are illustrated in Fig. 5, Fig. 8, and Fig. 11.

\[ 11 \times \frac{1}{8} \times 16 \times 512, \]  
\[ 30 \text{kB} \text{ single-port SRAM}. \]

The centering and covariance units reported in [11] are similar to those in [10], and so the latency is the same. However, the area complexity was estimated according to Tables I and IV in [11] due to a difference in the data widths. Moreover, the design of [13] processes real-valued 8 × 1024 data using four parallel computing units. The complexity is based on Table I and the layout of Fig. 4.5 in [13]. In addition, since the designs in [10], [11], and [13] use serialized processing, the throughput was calculated as the processing latency.

For a fair comparison, the latencies for the prior designs were scaled for a complex-valued 8 × 512 matrix. We assumed that the architectures of the prior designs were unchanged. The processing time was scaled according to the type and size of the matrix. A real-valued multiplier executes four times for a complex-valued multiplication. Thus, since the matrix size is doubled and the matrix type is complex-valued, the latencies were increased by eight times compared to the designs of [10] and [11]. Furthermore, since the design in [13] has multipliers operating in parallel, the latency was the same for a reduced-size complex matrix.

Table IV shows that the proposed design achieves much higher throughput and lower latency compared with the designs of [10] and [11], although at the cost of slightly increased area complexity. This is because these designs are based on serialized processing architectures, whereas the proposed covariance and centering units operate in a parallel and pipelined fashion. Moreover, the floating-point design of [13] has a

V. EXPERIMENTAL RESULTS AND COMPARISONS

A. Implementation Results

The latency, throughput, and complexity for the centering and covariance units reported in [11] are similar to those in [10], and so the latency is the same. However, the area complexity was estimated according to Tables I and IV in [11] due to a difference in the data widths. Moreover, the design of [13] processes real-valued 8 × 1024 data using four parallel computing units. The complexity is based on Table I and the layout of Fig. 4.5 in [13]. In addition, since the designs in [10], [11], and [13] use serialized processing, the throughput was calculated as the processing latency.

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The memory block is generated, and the complexity is estimated based on the area of two-input NAND gates. The total complexity is the sum of the logic latency and complexity are analyzed proportionally according to the timing and architecture diagram reported in the literature. The latency and complexity are analyzed based on Fig. 2 and 18 in [10]. Furthermore, the throughput and complexity for [11] are analyzed based on Table 1 in [10]. The latency and complexity for the design [13] is analyzed based on Fig. 3 and Fig. 4.5 in [13].

### TABLE V: Comparison of EVD units for different designs of preprocessor

| Parameter          | Original | Scalled | Original | Scalled | Original | Scalled | This work |
|--------------------|----------|---------|----------|---------|----------|---------|-----------|
| Technology (nm)    | 90       | 90      | 90       | 90      | 90       | 90      | 90        |
| Arithmetic type    | Real     | Real    | Real     | Real    | Real     | Real    | Complex   |
| Arithmetic type    | Fixed    | Fixed   | Fixed    | Fixed   | Floating | Floating| Fixed     |
| Frequency (MHz)    | 100      | 100     | 11       | 11      | 100      | 100     | 250       |
| Matrix type        | Real     | Complex | Real     | Complex | Real     | Complex | Complex   |
| Matrix size        | 8 × 512  | 8 × 512  | 8 × 512  | 8 × 512  | 8 × 1024 | 8 × 512 | 4 × 512   |
| Latency (cycles)   | 24576   | 196608b | 24576    | 196608b | 24576    | 24576b  | 1792 / 3584 / 5376 / 10752 |
| Throughput (μMatrices/cycle) | 40.7a  | 5.1b    | 40.7a    | 5.1b    | 40.7a    | 40.7b   | 976.56 / 488.28 / 223.21 / 162.76 |
| Throughput (kMatrices/s) | 4.07a | 0.51b | 4.05b | 0.06b | 4.07a | 4.07b | 244.1 / 122.1 / 55.8 / 40.7 |
| Complexity (kGE)   | 2.76a   | 2.76a   | 1.16a    | 1.16a   | 486a     | 486a    | 11.8      |
| Power (mW)         | 16.35a  | n/a     | 0.0816c  | n/a     | 65.0b    | n/a     | 50.2      |
| Efficiencyd        | 14.75   | 1.85    | 53.086   | 4.397   | 0.08     | 0.08    | 82.759 / 41.380 / 18.916 / 13.793  |

### TABLE VI: Comparison with state-of-the-art ICA preprocessors

| Parameter          | Original | Scalled | Original | Scalled | Original | Scalled | This work |
|--------------------|----------|---------|----------|---------|----------|---------|-----------|
| Technology (nm)    | 90       | 90      | 90       | 90      | 90       | 90      | 90        |
| Arithmetic type    | Real     | Real    | Real     | Real    | Real     | Real    | Complex   |
| Arithmetic type    | Hybrid   | Hybrid  | Fixed    | Fixed   | Floating | Floating| Fixed     |
| Frequency (MHz)    | 100      | 100     | 11       | 11      | 100      | 100     | 250       |
| Matrix type        | Real     | Complex | Real     | Complex | Real     | Complex | Complex   |
| Matrix size        | 8 × 512  | 8 × 512  | 8 × 512  | 8 × 512  | 8 × 1024 | 8 × 512 | 4 × 512   |
| Latency (cycles)   | 137472a | 422400a | 26256a   | 199968a | 137472a  | 250368a | 3424 / 6240 / 12160 / 19584 |
| Throughput (μMatrices/cycle) | 7.27a  | 2.37a   | 38.09a   | 5.001a  | 7.27a    | 3.99a   | 976.56 / 488.28 / 223.21 / 162.76 |
| Throughput (kMatrices/s) | 0.727a | 0.237a | 0.419a | 0.055a | 0.727a | 0.399a | 244.1 / 122.1 / 55.8 / 40.7 |
| Memory (KB)        | 8b       | 32a     | 3.5      | 14b     | 32a      | 32a     | 30        |
| Logic complexity (kGE) | 79.26b  | 79.26b  | 62.36a   | 62.36a  | 562.5a   | 562.5a  | 113.3     |
| Memory complexity (kGE) | 50.81a  | 129.91c | 24.7c    | 63.75c  | 129.91c  | 129.91c | 123.51    |
| Total complexity (kGE) | 130.07a | 209.17a | 87.06a   | 126.11c | 692.41c  | 692.41c | 236.81    |
| Power (mW)         | 16.35b   | n/a     | 0.0816b  | n/a     | 65.0b    | n/a     | 58.2      |
| Efficiencyd        | 0.06     | 0.011   | 0.437    | 0.04    | 0.01     | 0.006   | 4.124 / 2.062 / 0.943 / 0.687  |

*The latency and complexity are analyzed proportionally according to the timing and architecture diagram reported in the literature. The latency and complexity for the design [10] is analyzed based on Fig. 2 and 18 in [10]. Furthermore, the throughput and complexity for [11] are analyzed based on Table 1 in [10]. The latency and complexity for the design [13] is analyzed based on Fig. 3 and Fig. 4.5 in [13].

*The latency and throughput are scaled based on the processing of the complex-valued 8 × 512 matrix. It is assumed that the architecture remains the same and the processing time is scaled for processing larger complex-valued matrices. The memory is scaled for storing a complex-valued 8 × 512 matrix.

*Power consumption is for the entire chip, not just the centering and covariance units.

*Efficiency = Throughput (μMatrices/cycle) / Complexity (kGE).

*The latency and throughput are scaled based on the EVD of a complex-valued 8 × 8 matrix.

*Standalone (SA) is where the throughput is estimated by assuming only the EVD is operating. ICA is where the throughput is calculated by assuming the centering and covariance units reported in this work are the front stages of the EVD.

*The power is for the entire chip. *The unit is kMatrices/cycle. *The unit is kMatrices/s.
faster processing speed because it has four parallel computing units. While the accuracy is enhanced by the floating-point operation, the processing delay and area complexity are also greatly increased.

To illustrate the balance between throughput and complexity, efficiency was used as the figure of merit (FOM) in the comparisons [14], [15]. Efficiency is defined as the ratio of throughput and complexity indicating the performance gain for the cost. Table VI shows that, due to the highly optimized processing flow and the highly efficient utilization of hardware resources, the proposed design achieves the best efficiency compared to the prior designs.

Table VII compares the proposed EVD architecture with prior work. The latency for the EVD in the prior work was estimated if the results reported in the literature are based on the entire ICA system. In particular, the EVD in [10] and [13] is based on a single floating-point CORDIC component, so the latency and complexity are analyzed according to Fig. 4 in [10] and Fig. 4.5 in [13]. Furthermore, the complexity of the design of [11] was analyzed according to Table I in [11]. On the other hand, the SVD unit in [14] has a fully pipelined architecture, so the latency was analyzed based on Fig. 6 in [14]. The EVD unit proposed in [13] is based on a structure containing four PEs, so the latency was calculated according to Section IV-B in that work. Moreover, the latency for processing a real-valued 8 × 8 matrix in the design of [20] is reported in Table 3 in [20]. The complexity was estimated based on Tables 2 and 5 in that work.

For a fair comparison, the latency for the prior designs was scaled for a complex-valued 8 × 8 matrix, as shown in Table VII. We again assumed that the architectures were unchanged. The processing time was scaled according to the size and the type of the matrix. For example, the latency of [10] was increased by two times for the EVD of the complex-valued 8 × 8 matrix since the Jacobi algorithm operates on the real and imaginary parts separately. Furthermore, to evaluate the performance of EVD in ICA preprocessing, the throughput was also estimated by assuming that the centering and covariance units proposed in this work are the front stages of the EVD unit, which is referred to as ICA throughput in Table VII. The throughput for [10] was calculated by assuming that the EVD operates by itself, which is referred to as SA throughput. Since the proposed centering and covariance units output a result every 6144 cycles, the throughput is still dominated by the latency of EVD, so ICA throughput was the same as SA throughput for that design. The latency for [11] was doubled for the complex-valued matrix, and SA throughput was calculated accordingly. Since the architecture of [14] was designed for a complex-valued matrix, the scaled latency is the same as the original latency. The scaled latency was doubled and the scaled SA throughput was halved for the designs in [15] and [20] because of the complex-valued EVD. However, the scaled ICA throughput for [11], [15], [20] was limited by the input of the matrix from the centering and covariance units.

It can be seen from Table VII that compared to [10], the proposed EVD unit achieves a higher throughput with reduced complexity due to the highly optimized pipelined processing flow. Furthermore, the architecture in [11] is based on the systolic array structure, so its latency is greatly reduced. While the latency of [11] in terms of clock cycles is lower than the proposed design, the throughput is limited by the very low operating frequency. Moreover, the fully pipelined design in [14] achieves high SA throughput because multiple matrices can be processed at the same time. However, the throughput is degraded for ICA preprocessing. On the other hand, the proposed EVD unit is specifically optimized for ICA, and compared with [14], it strikes the best balance between throughput and complexity. In addition, the architecture of [15] maximizes the throughput by using multiple fully pipelined CORDIC elements and matrix multipliers. Compared to [15], the throughput of the proposed EVD unit is lower while the complexity is also much reduced. The design in [20] leads to a heavily degraded throughput due to the low operating frequency. The efficiency FOM is also used to compare the proposed EVD in ICA preprocessing by the different designs. Table VII shows that the proposed design outperforms the other designs in terms of efficiency. This is attributed to the highly optimized processing flow and the highly efficient utilization of hardware resources.

Table VII compares the proposed preprocessor with the prior ICA preprocessor designs. For a fair comparison, the latencies for the prior designs were scaled for a complex-valued 8 × 512 matrix. The latency and complexity of the ICA are due to the centering and covariance units as well as the EVD unit, as shown in Tables VII and VII. Furthermore, the total complexity in Table VII includes the logic as well as the memory. Specifically, to store an 8 × 512 complex-valued matrix, the size of the memory in [10] and [11] has to be increased by four times. Since the design in [13] has multipliers operating in parallel, the size of the memory is the same for a reduced-size complex matrix. Table VII shows that the preprocessor of [10] results in low throughput due to the serialized processing flow. Furthermore, the EVD in [10] has a floating-point structure, which results in high complexity. Moreover, the throughput of [11] is degraded due to the lower efficiency of the processing flow and the low operating frequency. In addition, due to its fully floating-point design, the throughput of [13] is higher at the cost of greatly increased area complexity. Table VII shows that the proposed design outperforms the other designs in terms of the efficiency FOM. This is attributed to the highly optimized processing flow and the highly efficient utilization of hardware resources. It is noted that the proposed design has a higher power consumption compared to the designs of [10] and [11] due to the higher operating frequency and the support of complex-valued operations. Furthermore, the fully floating-point design [13] leads to a high power consumption albeit a lower operating frequency.

### C. Case Study: SIC in IBFD Systems

As mentioned in Section II-A, the SIC in IBFD system is a prime example application that demands high performance ICA architectures [4], [5]. In this case, the ICA algorithm is applied to separate the self-interference signal and the signal of interest. An experimental platform in Matlab for the SIC in IBFD system is set up in [4], [5]. This system emulates a WiFi
data structure where a data frame contains 512 symbols and 48 subcarriers are employed. According to the normalized execution time reported in Table III the preprocessing time should be less than 29.5µs in this system. As a result, considering the latency of 78.33 µs as shown in Table IV, three preprocessors would be needed for achieving real-time preprocessing. This further pushes the need for designing a more accelerated preprocessor architecture. Moreover, the proposed architecture is configurable to support different sample lengths and applies to different types of data frames in wireless communications.

VI. CONCLUSION

This paper presents a high-throughput and highly efficient configurable preprocessor for the ICA algorithm. Moreover, a high-performance MMA is also described. The proposed MMA architecture uses time-multiplexed processing, which greatly increases the efficiency of hardware utilization. Furthermore, the novel processing flow of the proposed preprocessor is highly optimized, so that the centering, the calculation of the covariance matrix, and the EVD are conducted in parallel and are pipelined. Thus, the processing throughput is maximized while the required number of hardware elements can be minimized. The proposed ICA preprocessor is designed and implemented with a circuit design flow. The performance estimates are based on post-layout evaluations. The proposed preprocessor achieves a throughput of 40.7 kMatrices per second with a complexity of 73.3 kGE. Compared with prior work, the proposed preprocessor achieves the highest processing throughput and best efficiency.

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