Digital CMOS Temperature Sensor Implemented using Switched-Capacitor Circuits

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Abstract

A novel CMOS temperature sensor with binary output is implemented by using fully differential switched-capacitor circuits for resistorless implementation of the temperature sensor core. Temperature sensing is based on the temperature characteristics of the pn diodes implemented by substrate pnp transistors fabricated using standard CMOS processes. The binary outputs are generated by using the charge-balance principle that eliminates the division operation of the PTAT voltage by the bandgap reference voltage. The chip was designed in a MagnaChip 0.35-µm CMOS process, and the designed circuit was verified using Spectre circuit simulations. The verified circuit was laid out in an area of 950 µm × 557 µm and is currently under fabrication.

Keywords: Temperature sensor, CMOS, Switched-capacitor, Charge-balance, Sigma-delta modulation

1. INTRODUCTION

CMOS temperature sensors with digital output are attractive due to the advantages of low cost and ease of the digital controller user interface. Most CMOS temperature sensors are based on the temperature characteristics of the pn diode [1-3]. A proportional-to-absolute temperature (PTAT) voltage can be readily generated by taking the voltage difference between the two diodes forward-biased at different current densities. The forward-biased diode voltage has complementary-to-absolute temperature (CTAT) characteristic, which is needed to compensate for the PTAT characteristic to obtain the reference voltage required for measurement.

In this paper, we present a novel digital CMOS temperature sensor implemented by fully differential switched-capacitor circuits. The temperature sensing diodes are implemented by the substrate pnp transistors fabricated using a standard CMOS process. Switched-capacitor circuits are used to minimize the use of resistors that can lead to an increased power consumption at low resistance and an increased chip area at high resistance.

To simplify the hardware, the digital output is obtained by using the charge-balance principle [3]. The complete temperature sensor was designed using a 0.35-µm CMOS process. The designed circuit is currently under fabrication after verification using Cadence Spectre.

This paper is organized as follows. Section 2 discusses the operating principles of the designed temperature sensor. The circuit designs of the major blocks are covered in Section 3. The most important sub-block used in most of the blocks is the OTA. The design of a fully differential folded cascode OTA is discussed in Section 4. Section 5 shows the verification results obtained by circuit simulations. Finally, conclusions are given in Section 6.

2. PRINCIPLE OF OPERATION

2.1 Temperature sensing

The starting equation is the approximate current-voltage (I_D–V_D) relationship of the forward-biased pn diode as expressed in (1).

\[ I_D = \frac{qV_D}{kT} \]

where \( I_s \) is the saturation current of the diode, whereas \( q \), \( k \), and \( T \) are the electronic charge, Boltzmann constant, and absolute temperature, respectively.

\[ I_D \approx I_s e^{\frac{qV_D}{kT}}, \] (1)
From (1), the diode voltage can be solved as shown in (2):

$$V_D = \frac{kT}{q} \ln \left( \frac{I_D}{I_0} \right)$$  \hspace{1cm} (2)

In (2), the diode voltage seems to be a PTAT voltage, but it turns out to be a CTAT voltage as will be discussed below. This is because \( I_b \) is a rapidly increasing function with temperature. However, if we take the difference between the two diode voltages with different current densities, the resulting difference in voltage can be expressed as in (3).

$$\Delta V_D = V_{D2} - V_{D1} = \frac{kT}{q} \ln(p),$$  \hspace{1cm} (3)

where \( p \) is the current density ratio.

In (3), we can see that the difference voltage is a PTAT voltage that depends on the physical constants and the current density ratio. Thus, the difference voltage is fairly independent of the process and supply voltage variations.

To understand why the diode voltage is a CTAT voltage, let us examine the temperature dependence of the saturation current that can be expressed as in (4).

$$I_S = \frac{kT A n_b^2 \mu_b}{G_b},$$  \hspace{1cm} (4)

where \( A \), \( n_b \), \( m_b \), and \( G_b \) are the diode area, intrinsic carrier density, carrier mobility, and Gummel number, respectively.

If the temperature dependencies of the intrinsic carrier density and the mobility are substituted into (4), we obtain (5).

$$I_b(T) = CT^\eta e^{-\frac{kT}{q} \ln[I_b(T) - \eta \ln(C) + \ln(T)]}$$  \hspace{1cm} (5)

where \( \eta \) is approximately 2.5 and \( V_{go} \) is the bandgap voltage extrapolated to \( T = 0 \) K, which is approximately 1.2 V.

Now we can solve (5) for the diode voltage to obtain (6).

$$V_b(T) = V_{go} + \frac{kT}{q} \ln[I_b(T)] - \frac{kT}{q} \ln(C) + \ln(T)$$  \hspace{1cm} (6)

It is more convenient to express the diode voltage with respect to some reference temperature, \( T_r \), as in (7).

$$V_b(T) = V_{go} \left( 1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_b(T_r) - \frac{kT}{q} \ln \left( \frac{I_b(T)}{I_b(T_r)} \right) - \eta \ln \left( \frac{T}{T_r} \right)$$  \hspace{1cm} (7)

The temperature dependence of the diode current can be expressed as in (8).

$$I_b(T) = I_b(T_r) \left( \frac{T}{T_r} \right)^\eta$$  \hspace{1cm} (8)

If we substitute (8) into (7), we obtain (9).

$$V_b(T) = V_{go} \left( 1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_b(T_r) - (\eta - m) \frac{kT}{q} \ln \left( \frac{T}{T_r} \right)$$  \hspace{1cm} (9)

If we neglect the nonlinear logarithmic term, the diode voltage expression can be simplified to (10).

$$V_b(T) = V_{go} - \frac{T}{T_r} [V_{go} - V_b(T_r)]$$  \hspace{1cm} (10)

Note that (10) shows that the diode voltage is a CTAT voltage, since the bandgap voltage is greater than the diode voltage. If we set the reference temperature as 300 K and assume that the diode voltage is 600 mV, (10) gives a temperature coefficient of \(-2 \text{ mV/C}\). Let us define the diode voltage as \( V_{CTAT} \). Now this negative coefficient of \( V_{CTAT} \) can be compensated for by adding a PTAT voltage, \( V_{PTAT} \), properly scaled by 2 mV/C, to generate the bandgap reference voltage, \( V_{BGR} \), which has a value of 1.2 V and virtually independent of the process, voltage and temperature variations.

### 2.2 Sigma-delta conversion for digital readout

Now we can determine the temperature by taking the ratio of \( V_{BGR} \) to \( V_{BGR} \). The ratio changes from 0 to 1 as the absolute temperature increases from 0 K to 600 K, with its practical validity restricted to part of the entire range. A division operation is needed to obtain the ratio. The division operation can be eliminated if we use a charge-balance-based analog-to-digital conversion. The charge balance is achieved by the combined action of the integrator and the comparator shown in Fig. 1, resulting in almost equal amounts of charge flow into and out of the capacitor in the integrator on the average [3]. Note that the density of “1” in the sigma-delta modulated data should be proportional to the temperature. Since \( V_{PTAT} \) increases with the temperature and \( V_{PTAT} \) decreases with the temperature, the charge balance can be expressed as in (11). In this implementation, \( V_{CTAT} \) is subtracted from the accumulated output for the data of “1”, while \( V_{PTAT} \) is added to the accumulated output for the data of “0”.

$$N_i V_{CTAT} = N_i V_{PTAT}$$  \hspace{1cm} (11)

Resistive loads are difficult to drive using CMOS circuits. To minimize the use of resistors, the required amplifiers and integrator are implemented by using switched capacitor circuits.
Fully differential switched capacitor circuits are used to eliminate the signal-independent charge injection and the clock feedthrough.

3. DESIGN OF MAJOR BLOCKS

3.1 CTAT & PTAT voltage generators

To generate the CTAT voltage, a substrate pnp transistor is diode-connected and is driven by a PMOS current source. The simulated temperature dependence of the diode voltage is shown in Fig. 2. We can see that the temperature coefficient is approximately -1.76 mV/°K.

To obtain a fully differential CTAT voltage, a switched-capacitor amplifier shown in Fig. 3 is used [4]. The gain is determined by the ratio of $C_{11}$ (2 pF) to $C_{21}$ (5 pF), which is set for adequate sigma-delta modulator loop gain.

To generate the PTAT voltage, two identical substrate pnp transistors are diode-connected and are driven by two different PMOS current sources with a current ratio of 13. The difference between the two diode voltages is a PTAT voltage. This PTAT voltage must be amplified by a gain of 8 to make the temperature coefficient approximately equal to +1.76 mV/°K. Fig. 4 shows that the bandgap reference voltage can be generated by summing the CTAT voltage and the properly scaled PTAT voltage.

To convert the single-ended PTAT voltage to the differential version, another switched-capacitor amplifier shown in Fig. 5 is used with 3.2 pF for $C_{11}$ and 1 pF for $C_{21}$ to make the relative gain with respect to the CTAT voltage equal to 8.
3.2 Integrator

A fully differential switched-capacitor integrator with offset cancellation is used in this design [5]. The integrator circuit schematic is shown in Fig. 6.

3.3 Comparator

The comparator core is implemented by NMOS and PMOS latches for fast operation, as shown in Fig. 7. To reduce the effect of the kick-back noise, the comparator core is preceded by a simple differential amplifier (not shown).

3.4 Peripheral circuits

Non-overlapping two-phase clocks and an additional clock slightly advanced in phase for enabling the input of the OTA to float to allow the charge injection to be independent of the input signal are generated by a clock generator [6]. The reference current needed in driving the substrate pnp transistors, OTA, and pre-amplifier for the comparator is generated by a self-biased resistorless CMOS current reference circuit with the MOSFETs in the b-multiplier operating in subthreshold region [7].

4. FULLY DIFFERENTIAL OTA DESIGN

4.1 OTA core

A folded-cascode topology shown in Fig. 8 is chosen based on comparison of key performance indicators including gain, speed, voltage headroom, and power consumption. PMOS transistors are used as an input pair because the low input common-mode level allows NMOS switches to be used, which results in higher non-dominant pole frequency. In addition, PMOS devices have smaller flicker noise.

The common-mode feedback voltage is applied to the NMOS loads of the differential pair. Bias currents are equally divided between the input stage and the cascode stage for high slew rate. PMOS clamps are used to prevent worst case slewing conditions.
4.2 Common mode feedback

A common-mode feedback is needed in fully differential OTAs to ensure their operation in the saturation region. In this work, a source-coupled pair shown in Fig. 9 is used to sense the common-mode output voltage. An elaborate frequency compensation based on a lead-lag network consisting of a 4.37-$\Omega$ resistor and a 10-pF capacitor is required to prevent the oscillation in switching mode operations.

4.3 Biasing circuit

A wide-swing constant-$g_m$ biasing circuit shown in Fig. 10 is used for the OTA core. Wide swing is made possible by careful sizing of the MOSFETs. A start-up circuit is needed to lift the circuit out of the zero-current operating condition.

5. SIMULATION RESULTS

The designed circuit was verified through circuit simulations. The uncompensated folded-cascode OTA has a gain of 58.98 dB with the 3-dB frequency at approximately 327 kHz, as shown in the frequency response characteristics in Fig. 11. However, the phase margin of the uncompensated OTA is approximately 35°, which might not be sufficient for some applications.

For fully differential operation, both the CTAT and the PTAT voltages must be converted from single-ended signal to differential signal. Figs. 12 and 13 show the differential CTAT and

![Fig. 11. Bode plot for the folded-cascode OTA](image)
the differential PTAT voltage waveforms, respectively. The glitches generated by switching do not affect the operation of the temperature sensor because they are ignored by sampling operation inherent in the switched capacitor circuits.

Fig. 14 shows the differential output waveforms of the integrator with its differential input alternating in polarity. Fig. 15 shows the output waveforms of the comparator with its differential input alternating in polarity. Note that both outputs are periodically reset to the VDD level.

The key waveforms of the temperature sensor are shown in Fig. 16. As can be seen in Fig. 16, the integrator input voltage is \(-V_{CTA}\) when the data is “1,” whereas the integrator input voltage is
The number of “1”s in the data for different temperature was extracted from the simulation results in 400 ms intervals, each equivalent to 200 bits. Fig. 17 shows an almost linear increase in the number of “1”s with temperature.

The verified circuit was laid out for fabrication by MagnaChip’s 0.35-mm CMOS process. The layout of the entire temperature sensor is shown in Fig. 18. The chip occupies an area of 950 μm × 557 μm.

6. CONCLUSIONS

A novel resistorless CMOS temperature sensor with a binary output is implemented using fully differential switched-capacitor circuits. The new temperature sensor has the advantages of low cost and simple interface with digital controllers. Thus, it is expected to find wide use in smart sensor applications.

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