Low-power LDO Design of High-efficiency Class AB OTA Based on Adaptive Biasing

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Abstract. This design proposes a new low-dropout linear regulator (LDO) with low input voltage and low standby power consumption. A new type of adaptive bias circuit is proposed, which uses a high-efficiency class AB OTA based on class AB differential input stage and local common mode feedback (LCMFB), which not only increases the gain bandwidth product (GBW), but also improves current efficiency, in addition, a dynamic charging transistor (DCT) is used to enhance the transient characteristics of the circuit. The circuit design uses 0.18μm standard CMOS technology to achieve a stable output of 1.0V after the power supply voltage is adjusted from 1.2V, and the maximum output current is 100mA. The quiescent current is only 2.3μA at no-load, when the load current is converted from 1mA to 100mA within 1μs, the overcharge voltage is less than 130mV, and the full range of load current stability from 1mA to 100mA is achieved under the maximum 100pF load capacitor.

1. Introduction
In recent years, with the requirement of power of portable electronic products become more and more stringent, high-efficiency power management units and low-dropout linear regulators (LDO) have been widely used due to their low output noise, small ripple, and low electromagnetic interference. In order to facilitate integration, capacitor-free LDOs have been extensively studied [1]. Among them, the operational transconductance amplifier (OTA) plays a vital role in the LDO circuit. The adaptive bias circuit [2] is very helpful in improving the OTA performance. It can provide a variable bias current in the presence of an input signal in the absence of such a signal input, it only provides a constant quiescent current, which can be accurately controlled, finally, reducing the static power consumption. These circuits are widely used in Class AB operational amplifiers. However, most of them cannot work at low power supply voltages or have an excessive bias currents under dynamic conditions.

In this paper, a new adaptive bias topology is proposed and local common mode feedback (LCMFB) is introduced, which combines excellent performance, simple design and suitable for low-voltage operation, so that it not only has good static and dynamic characteristics performance, but also can work under the minimum power supply voltage \(V_{DD_{min}} = |V_{GS}| + 2|V_{DSAT}|\). The arrangement of this article is as follows: Section one introduces the important position of LDO in today's electronic product applications and the problems that arise, section two introduces the new LDO schematic and specific circuit, and conducts stability analysis. The rest of the paper is organized as, section three stated the proposed circuit simulation and evaluate results, followed by a section four conclusion.
2. LDO architecture
The overall circuit of this design is shown as in Fig. 1. The circuit mainly includes a high-efficiency OTA composed of adaptive bias and local common mode feedback (LCMFB), a dynamic transistor (DCT) composed of MDCTP and MDCTN, a power tube PT, and a resistance feedback network realized by R3 and R4. LCMFB provides additional current boost, improves current efficiency, and increases gain bandwidth product. The introduction of DCT forms a fast non-linear feedback loop.

2.1. OTA
Figure 2 shows the basic structure of the adaptive bias circuit and local common mode feedback (LCMFB). The active load of the differential pair is rearranged, and through the local feedback loop of matching resistors R1 and R2, the drain voltage of R6 and R7 is fed back to the gate in common mode, that is, local common mode feedback (LCMFB). This provides additional current boost, optimizes current efficiency, and increases the gain bandwidth product to the class AB amplifier. At the same time, small signal analysis is performed on OTA, namely

\[ i_1 = -i_2 = \frac{k g_{m1,2} v_{id}}{2} \]  \hspace{1cm} (1)

Among them, \( v_{id} \) is the AC small signal differential input voltage, and \( k \) is usually 1. If it is assumed that the values of R1 and R2 are much smaller than \( r_{o6} \) and \( r_{o7} \), where \( r_{o6} \) and \( r_{o7} \) are the small signal models of the source and drain resistances of M6 and M7, then the small signal current

\[ i_R = i_1 = -i_2 \]

will have complementary AC voltage changes at the X and Y nodes, which is

\[ u_X = -u_Y = R_{1,2} i_R = \frac{R_{1,2} k g_{m1,2} v_{id}}{2} \] \hspace{1cm} (2)

Therefore, \( u_Z = 0 \), in other words, point Z becomes an AC virtual ground, which not only eliminates the capacitance influence of \( C_{GS6} \) and \( C_{GS7} \) on nodes X and Y, but also increases high-frequency poles \( f_X \) and \( f_Y \). Increase the small signal resistance of the node through resistors R1 and R2, namely

\[ R_{X,Y} \approx R_{1,2} / / r_{o6,7} / / r_{o1,2} \] \hspace{1cm} (3)

Due to the stability of the circuit, R1,2 has an upper limit, and the gain bandwidth product is

\[ GBW = \frac{k g_{m1,2} g_{m5,8} R_{X,Y}}{2 \pi C_t} \] \hspace{1cm} (4)

Therefore, the OTA can achieve a high conversion rate without the need for large resistance values R1 and R2.

The specific adaptive bias circuit is shown in Figure 3. When the adaptive bias circuit senses a large differential input signal, it will automatically increase the bias current provided. When the load of the LDO suddenly rises, an undershoot voltage will be generated, which forces the gate voltage of M16 in the adaptive bias to drop, and then the voltage across M15 decreases, resulting in a decrease in the gate voltage of M18, which increases the source of M1 and M2. The current, on the contrary, reduces the source current of M1 and M2, and plays a current adaptive effect.

2.2 DCT
The DCT of the circuit design is shown as in Fig. 1. The DCT is composed of MDCTP and MDCTN, which form a fast non-linear feedback loop. When the load current suddenly produces a large current change, a large charge and discharge current is also generated on the gate capacitance of the power transistor. At this time, the input stage of the amplifier changes in voltage, so the gate voltage of MDCTP and MDCTN will be controlled by a natural transient voltage. When the load current changes from a light load to a heavy load, the output voltage will suddenly decrease, and the feedback voltage will decrease accordingly. At this time, the gate voltage of the MDCTP will decrease, making the MDCTP turn on, initially turning off in a steady state. This way the power transistor can be charged.
quickly. Similarly, when the load current changes from a heavy load to a light load, the output voltage will increase. At this time, the gate voltage of the MDCTN will increase, so that the MDCTN transistor turns on and discharges quickly.

![Diagram of LDO structure](image)

**Figure 1.** The LDO structure proposed in this article

![Diagram of adaptive biasing](image)

**Figure 2.** Adaptive bias and local common mode feedback

**Figure 3.** Adaptive biasing

### 3. Simulation results

The analog transient response output result is shown in Figure 4. When the input voltage is 1.2V, the output voltage is stable at 1V; when the circuit introduces a 100mA load at 50us, the circuit only generates an undershoot voltage of 129mV within 2.03us. When the load is removed, the circuit only generates an overshoot voltage of 76mV within 2.16us and then returns to a stable state. The transient response simulation of the adaptive bias circuit is shown in Figure 5. When the circuit load suddenly increases to 100mA, in order to maintain a steady state of the circuit, the adaptive bias immediately starts to adjust the current, which increases the current of the differential pair M1 and M2. The bias circuit only consumes 200nA current, which can be ignored. Table 1 shows the performance comparison between this design and other designs.
Figure 4. Simulated transient response \( V_{in}=1.2V, V_{out}=1.0V \)

Figure 5. Transient response of adaptive bias circuit

| Table 1. Performance comparison |
|-------------------------------|
| Parameter | [3] | [4] | [5] | [6] | This work |
| Year | 2011 | 2019 | 2018 | 2017 | 2020 |
| Technology(um) | 0.5 | 0.11 | 0.18 | 0.056 | 0.18 |
| \( V_{IN}(V) \) | 2.4-6 | 2.2 | 1.2 | 1.5-2.5 | 1.2 |
| \( V_{OUT}(V) \) | 0.6-1.3 | 2.0 | 1.0 | 1.2 | 1.0 |
| Dropout(mV) | 3000 | 200 | 200 | 300 | 200 |
| \( I_{out_{max}}(mA) \) | 220 | 200 | 100 | 10 | 100 |
| \( I_{Q}(uA) \) | 220 | 41.5 | 100 | 100 | 2.3 |
| \( C_{L}(pF) \) | 40 | 40 | 100 | 10 | 100 |
| \( T_{edge}(us) \) | 500 | 0.5 | 0.3 | 1 | 1 |
| \( T_{settle}(us) \) | 650 | 0.65 | 1.56 | 1.1 | 2 |

4. Conclusion
This design proposes a low-power LDO using a new adaptive bias circuit and an efficient class AB OTA, which is based on class AB differential input stage and local common mode feedback (LCMFB). Finally, under the simulation of 0.18 um standard CMOS process, the stable output of the power supply voltage adjusted from 1.2V is realized, and the maximum output current is 100mA. The quiescent current is only 2.3μA at no-load, and when the load current is converted from 1mA to 100mA within 1μs, the overcharge voltage is less than 130mV, and the range of load current stability from 1mA to 100mA is achieved under the maximum 100pF load capacitor.
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