A front-end ASIC for ionising radiation monitoring with femto-amp capabilities

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ABSTRACT: An ultra-low leakage current Application Specific Integrated Circuit (ASIC) called Utopia (Ultralow Picoammeter) has been designed and fabricated in AMS 0.35 µm CMOS, in order to be used as the front-end for ionising radiation monitoring at CERN. It is based on the topology of a Current to Frequency Converter (CFC) through charge balancing and demonstrates a wide dynamic range of 8.5 decades without range changing. Due to a design aimed at minimising input leakage currents, input currents as low as 10 fA can be measured.

KEYWORDS: Analogue electronic circuits; Radiation monitoring; Front-end electronics for detector readout

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1 Introduction

One field that requires ultra-low current measurements is radiation detection and monitoring. Exposure to ionising radiation accompanies all work at a particle accelerator and in the associated experimental facilities. CERN has a legal obligation to protect the public and persons working on its site from any unjustified exposure to ionising radiation, so the ambient dose must be monitored [1]. CERN is not unique in this respect and other domains where ambient radiation levels must be monitored include but are not limited to nuclear facilities, synchrotrons, hadron therapy institutes and hospitals.

Although several readout systems for radiation detectors like ionisation chambers and pixel detectors have been proposed in the bibliography and they all demonstrate a wide dynamic range of more than 5 decades as shown in [2, 3] and [4], they are all limited in the lower current range, typically being able to measure current as low as 300 fA. The main limitation is the leakage currents of the CMOS input devices, of the ESD protection and of the Printed Circuit Board (PCB). This research focuses on the low range, specifically on the leakage current minimisation, in order to provide an ultra-low leakage current ASIC that can even measure the background radiation, which means currents starting from less than 50 fA after averaging over a sufficient time period. The proposed ASIC is able to digitise currents from tens of fA after leakage current compensation and is able to measure up to 5 µA.
Table 1. Utopia requirements.

| Requirement                                      | Value           |
|--------------------------------------------------|-----------------|
| Input current polarity                          | Negative        |
| Dynamic range for constant input current         | 60 fA to 250 nA |
| Maximum pulsed input current                    | 1.72 µA         |
| Maximum charge per pulse                         | 5 nC            |
| Detector capacitance $C_{in}$                    | 9 pF or 65 pF   |
| Measurement time window                          | 100 ms          |
| Maximum linearity error                          | ±5%             |
| Temperature range                                | −15°C to 55°C   |

2 Utopia ASIC specifications and architecture

2.1 Specifications

The required radiation measurement range should start from 50 nSv/h up to 0.1 Sv/h and for pulsed radiation fields it is extended up to 10 Sv/h. The detectors that are used at CERN for radiation monitoring, are mainly ionisation chambers. The ionising current that is produced from the chambers depends on the type of the chamber and represents a measure of the total ionising dose entering the chamber in a fixed time interval. Using the typical conversion factor for γ rays of the detector that is $1.6 \cdot 10^{-6}$ A/Sv/h, the output current range spans from 80 fA to 160 nA. For the chambers used closer to the accelerator where the conversion factor is $2.5 \cdot 10^{-8}$ A/Sv/h, the output current range spans from 25 fA up to 250 nA. The initial values that correspond to lower radiation are not obtainable with existing solutions. The specifications of the front-end to be connected to the ionisation chambers are presented in table 1. The input capacitances, $C_{in}$, of the two different chambers used in this project were measured to be 65 pF and 9 pF for the low gain and high gain respectively.

2.2 Topology

The circuit’s basic architecture does not differ from similar implementations presented in [3] and [5] and is based on a Current to Frequency Converter (CFC) operating principle through charge balancing, as shown in figure 1(a). The input current $I_{in}$ that is generated from the radiation detector is integrated along with the leakage currents on the capacitor $C_f$ and the output voltage, $V_{out}$, of the integrator is compared with an externally set voltage threshold $V_{th}$ using a discriminator. The discriminator output is brought into an externally provided clock domain, typically 10MHz (mode 1). A logic high triggers the injection of a fixed amount of charge, termed $Q_{ref}$. Following this, the charge injection circuit must recharge itself. In the case where the $V_{out}$ remains above the threshold, the discharging circuit injects again after recharging. The same architecture could also be implemented asynchronously, where instead of using a clock, the discharging circuit would trigger a monostable after the comparator crosses the threshold (mode 2).

However, instead of measuring the integration time, the input current is calculated by counting. An FPGA is connected to the digital output $V_{Dout}$ and is used for the data acquisition. The frequency of charge injection $f$ is evaluated by counting the number of charge injections $N_{counts}$ in a reference time window, noted as $T_w$. By counting how many times the reference charge $Q_{ref}$ is injected in that
measuring time window \( T_w \), the total input current can be calculated using eq. (2.1) or equivalently eq. (2.2):

\[
I_{in} = f \cdot Q_{ref} \quad (2.1)
\]

\[
I_{in} = \frac{N_{counts} \cdot Q_{ref}}{T_w} \quad (2.2)
\]

where the reference charge, \( Q_{ref} \) is given from:

\[
Q_{ref} = C_{ref} \cdot (V_{charge} - V_{in}) \quad (2.3)
\]

3 Circuit design and results

The Utopia ASIC is implemented in AMS 0.35 \( \mu \)m CMOS C35B4/C3 4M/2P/HR/5V IO, a technology specially selected for its low leakage current behaviour, since the sum of the leakage currents increases with technology scaling [6]. The ASIC is single-ended, supplied by 3.3 V single power supply and is biased in order to accept negative polarity input current as required by the detector’s polarity. Its size is 2.6 mm \( \times \) 2.6 mm. The integrator is a two-stage Miller Operational Transconductance Amplifier (OTA), where the pMOS input devices of the differential pair are biased in moderate inversion. The schematic of the OTA is shown in figure 1(b). The Gain Bandwidth (GBW) of the OTA is 100 MHz, the phase margin is 62\(^\circ\) and the open loop gain \( A_0 \) is 86 dB. The comparator shown in figure 1(c) is designed with internal positive feedback and with 5 mV hysteresis. The discharging circuit that injects the reference charge \( Q_{ref} \) is a stray insensitive switched capacitor circuit (figure 1(d)) and the \( C_{ref} \) is matched to the \( C_f \) of the feedback loop of the OTA. The switches of the discharging circuit are managed from the non overlapping clocks noted as \( NOC \) in figure 1(a).

The Utopia ASIC was designed in order to be used for prototyping and testing and to estimate the minimum and the maximum currents that can be measured using a single range implementation.

Figure 1. Utopia system architecture and schematics.
The ASIC has four similar channels but with modifications to the inputs in order to estimate the contribution of each leakage current source to the net input leakage current. The reference voltages and biasing currents must be provided externally and are common for all the channels. Moreover, the analogue output, $V_{\text{out}}$, after a source follower level shifter, the comparator’s output, $V_{\text{Dout}}$, and the non overlapping clock’s input, $\text{NOC}_{\text{inv}}$, are accessible for debugging. One of the channels, CH4, provides the possibility to run in asynchronous operation (mode 2), while the other three channels are clocked. The PCB that hosts the ASIC is shown in figure 2. The inputs were routed with no ground plane to reduce the leakage currents in the signal traces. The ASIC is encapsulated in a 44 pin ceramic package. Four different clocks can be used in order to provide the possibility to work with each channel separately, while the integrator output of the other channels $V_{\text{out}}$ will saturate to the power rails.

### 3.1 Femto-ampere range

The lowest current that can be measured using the CFC is given from eq. (3.1):

$$I_{\text{min}} = \frac{Q_{\text{ref}}}{T_w} \quad \text{(3.1)}$$

In a single range implementation, the reference charge, $Q_{\text{ref}}$, should be selected as a compromise to satisfy both the low (fA) and the high current (µA) requirements. For simplicity, the values that were initially selected are $C_{\text{ref}} = 1 \text{ pF}$, $V_{\text{charge}} = 2.5 \text{ V}$, $V_{\text{cm}} = 1.5 \text{ V}$ and $V_{\text{th}} = 2.5 \text{ V}$. Then the $Q_{\text{ref}} = 1 \text{ pC}$ and in a $T_w$ of 100 ms, a minimum current of 10 pA can be integrated. This is not a hard limit, because if the measurement time is increased, lower currents can be integrated and measured. Equivalently, multiple $T_w$ can be added together in order to increase the resolution and provide a non zero count, since the input charge is accumulated in $C_f$. However independently of the time window, the lowest possible current that can be measured is limited by the sum of the
leakage currents that are added to the signal current along its path from the ionisation chamber to the input of the integrator.

3.1.1 Design for ultra-low leakage current

In order to achieve the ultra-low leakage current behaviour, the leakage current sources connected to the input should be identified. They include the subthreshold leakage current of the switches \( S_{\text{init}} \) and \( S_2 \) connected to the input, the ESD protection leakage current, the package leakage current and the printed circuit board leakage current. Additionally there is the cable leakage current and the detector’s leakage current. All these various leakage current sources that contribute to the net leakage are depicted in figure 3(a) and are noted with (1), (2), (3) and (4).

The main source of a transistor’s leakage current in 0.35 \( \mu \)m CMOS technology is the subthreshold leakage current. It can be decreased by biasing the gate voltages beyond the power supply rails or by shifting the source voltages higher than the bulk. This is thoroughly analysed in [7] and [8]. If the source to bulk voltage \( V_{SB} \) is increased, the threshold voltage increases and the subthreshold leakage of the switches can be reduced as shown in the simulation in figure 3(b) for a minimum size transistor \( W/L = 1/0.35 \) where \( V_D = 1.65 \) V and the \( V_S \) sweeps from 0 V to 1.5 V. In order to minimise the subthreshold leakage of the switches in the input of the OTA, the \( V_{cm} \) that can indirectly manage the voltage of the \( V_{in} \) that is equivalent to the voltage \( V_{SB} \) of that switches is at a different potential relative to the bulk, \( V_B \) that is zero. The subthreshold leakage is pushed from the fA to the aA range.

The largest source of leakage current in the system, is the ESD protection circuit. The effect of the ESD protection leakage current was studied by implementing a channel (CH2), where the standard ESD protection cells were modified. The leakage current related to the modified ESD protection diodes compared to the standard ESD cells was measured that way. The PCB leakage current and the package leakage current were also considered, measured and subtracted. The methodology that was used to estimate each leakage current source effect, measure accurately the leakage current contribution and minimise it is presented in [9]. By changing the \( V_{cm} \) value, the total leakage current that is mainly dominated by the ESD protection leakage and the leakage due to parasitics in the input nodes, changes polarity. In order to minimise the total leakage current

**Figure 3.** (a) Leakage current sources in the Utopia’s input, (b) Simulation of \( I_D \) vs \( V_g \) when \( V_s \) sweeps from 0 V to 1.5 V.
for the following measurements, an optimum value for $V_{cm}$ that limited the leakage current of CH1 to 12 fA was selected. This was measured by the Utopia system, by leaving the input open and integrating the net leakage current for long periods of time.

### 3.1.2 Measurement results (fA range)

A high precision current source accurate to approximately 10 fA (Keithley 6430) was used in order to inject input currents in CH1 starting from 1 fA up to 100 fA in 11 steps. The measurement results are presented in figure 4(a). These measurements were performed inside a climatic chamber where the temperature and humidity were kept constant at 10°C and 0% respectively. The measurement time used was 600 s. The leakage current can be regarded as an offset (12 fA) that can be subtracted. It should be noted, that the net leakage dominated by the ESD protection leakage current, is strongly affected from temperature and it doubles for every 10°C of temperature increase. This is shown in figure 4(b) that presents the dependence of the leakage current of CH2 on temperature.

### 3.2 Micro-ampere range

The maximum current that can be measured using the CFC can be calculated from (3.2):

$$I_{\text{max}} = \frac{Q_{\text{ref}}}{T_{\text{charge}} + T_{\text{discharge}}}$$

(3.2)

Using $Q_{\text{ref}} = 1 \text{ pC}$ and if we consider that the limit is given when $T_{\text{charge}} = T_{\text{discharge}} = 100 \text{ ns}$, the maximum current limit is $5 \mu\text{A}$.

#### 3.2.1 Design to increase the upper current limit

In the higher input current range, due to the integrator’s GBW limitations and to the increase of the input current, at some point the reference charge can not discharge the integrator. This problem is inherent to the single range implementation since the integrating curve becomes steeper. The $V_{\text{out}}$ increases and although the discharging circuit is injecting charge in the input, the integrator’s output does not fall below the threshold $V_{\text{th}}$, so the comparator does not return to zero and the system is blocked from normal operation. Finally the $V_{\text{out}}$ saturates to $V_{\text{DD}}$. This is observed in figure 5(a) taken from the oscilloscope when measuring CH4 in the asynchronous mode. Near the upper limit,
noise on the signal pushed the system into saturation. In order to increase the robustness of the system a control system re-injects \( Q_{\text{ref}} \) if the first injection was not enough to bring the \( V_{\text{out}} \) below \( V_{\text{th}} \) as shown in figure 5(b). The input current \( I_{\text{in}} \) was 2 \( \mu \)A. Although the comparator’s output \( V_{\text{Dout}} \) remains high, the charge injection circuit that is managed from the FPGA alternates between charge discharge cycles and re-injects \( Q_{\text{ref}} \). With this technique, it was possible to increase the maximum range limit up to 5 \( \mu \)A without increasing the integrator’s GBW.

### 3.2.2 Measurement results (dynamic range)

The dynamic range of the Utopia ASIC when using a precise laboratory current source to inject currents is presented in figure 6. The error after leakage current compensation is also shown. The leakage current in this measurement had a value of +12 fA. This measurement was performed in CH4 using the asynchronous operation (mode 2) of the CFC that demonstrates better performance in terms of noise and crosstalk due to the absence of the clock.
4 Conclusion

A very wide dynamic range Current to Frequency Converter with fA sensitivity for radiation monitoring was presented along with measurements that are forcing the ASIC to the edge of its operating conditions. Currents in the femto-ampere range can be measured, after averaging for more than 1 s for better sensitivity, but also measurements up to 5 µA can be achieved if the reference charge, \( Q_{\text{ref}} \), is injected in more than one step. The ASIC is expected to work mainly in the fA to the nA range due to the lower radiation levels expected in areas accessible from personnel, where it demonstrates excellent linearity. In that range, the slow acquisition is not a main issue since lower radiation levels are compatible with seconds of integration time. However, this ASIC will be revised and will include some extra functionalities like faster acquisition in the ultra-low range of femto-amperes and auto-calibration for long term stability, in order to operate in the required temperature range. The increase in the leakage currents due to the temperature increase will be compensated. The new version of the ASIC is expected to be used as the front-end for the new radiation monitoring system at CERN.

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