Charging characteristics of Si nanocrystals embedded within SiO$_2$ in the presence of near-interface oxide traps

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Abstract. In this work we report on the influence of oxide traps - located near the Si substrate-tunnel oxide interface - on the charging characteristics of Si-nanocrystals embedded within SiO$_2$ layers, by monitoring the admittance characteristics at room temperature. We study this effect in the case of Si-nanocrystals fabricated by LPCVD deposition of $\alpha$-Si and high temperature thermal oxidation. In the samples investigated in this work, oxide hole traps located almost at the Si-SiO$_2$ interface of the silicon substrate were found to control hole injection and transfer to the Si nanocrystals. Upon capturing a hole the defect energy levels undergo a transition due to lattice relaxation effects and hole charging of the Si-nanocrystals occurs via an inelastic two-step tunneling mechanism. High temperature annealing was found to reduce the density of these near-interfacial defects, therefore reducing the coupling between the Si-nanocrystals and the substrate.

1. Introduction

Silicon nanocrystals (Si-ncs) based memory structures are considered as potential candidates for the replacement of conventional floating gate memory devices, since the latter have come to their ultimate limits by the continuous downscaling process [1]. Nanocrystals structures for memory applications are composed of a two-dimensional layer of Si-ncs embedded within SiO$_2$. Charge trapping and storage occurs not in a continuous medium but in discrete and non-interacting storage nodes located in close proximity to the silicon substrate [2]. Such a distributed charge storage medium offers the possibility to scale further the tunneling oxide without compromising retention and reliability characteristics, allowing thus an overall upgrade of the performance of the memory cell [2].

The formation of Si-ncs embedded within SiO$_2$ has been implemented by a variety of self-assembly techniques, utilizing direct deposition methods [3,4] or ultra-low-energy ion beam synthesis [5]. Our approach for the formation of Si-ncs is based on low-pressure chemical vapor deposition of amorphous silicon on a thin tunneling oxide followed by controlled oxidation. Previous reports demonstrated that this method synthesizes Si-ncs within SiO$_2$ and it constitutes a single and reliable process for the fabrication of silicon nanocrystals memory structures [6]. In this respect, full investigation of the different parameters involved in charge trapping is necessary for device optimization. Defects introduced during the various fabrication steps in the oxide play a crucial role on the overall electrical characteristics of the memory cells. In this work we report on the influence of near-interfacial oxide traps on the charging characteristics of Si-ncs structures using admittance measurements at room temperature.
2. Experimental
Structures with a two dimensional array of Si-ncs in-between two oxide layers were fabricated by depositing a layer of amorphous silicon approximately 9 nm thick, on top of a 3.5 nm thermally grown silicon oxide. Subsequently the structure was thermally oxidized for 20 min at 900 °C. During this process the amorphous silicon is partially oxidized, while the remaining silicon recrystallizes forming a three-layer structure with well-defined interfaces, corresponding to the top oxide, the 2-D array of Si-ncs and the tunnel oxide. The duration of oxidation determines the size of the Si-ncs. Transmission electron microscopy on similar processed samples showed that oxidation for 20 min results in a Si-ncs layer 3.5 nm thick, while the overall thickness of the gate stack was 17 nm [7]. Part of the sample was subsequently annealed at 1000 °C for 1 h. Test capacitors having an area 1x10⁻⁴ cm² were finally fabricated by depositing and patterning aluminum for the gate metal and forming a back ohmic contact. No post metallization anneal was performed.

3. Results and discussion
Admittance measurements were carried out at room temperature in a shielded probe station using a HP 4284A LCR meter. Charge injection was performed by applying positive or negative pulses via a HP 8110A pulse generator and subsequently monitoring the resulting shift of the C-V and G-V characteristics. Charge injection and trapping within the silicon nanocrystals shifts the C-V characteristics towards more positive (electron) or negative (hole) gate voltages (figures 1a and b). No restoration to the initial charging state of the structure was attempted between the applied pulses. Positive pulses with amplitude up to 5 V results in a small shift of 50 mV in the C-V, which must be due to charge rearrangement effects due to charging of the interface traps and not to charge injection. Charging of the structure due to injected electrons starts at 6 V corresponding to an average electric field across the structure above 3 MV/cm. Increasing the pulse amplitude shifts further the characteristics and at 9V we obtain the maximum charging with \( \Delta V_{FB} \) (flat-band voltage shift) reaching 0.9 V. Higher positive pulse amplitudes shift the characteristic in the opposite direction due to initiation of high field conduction. Similarly, positive charging due to injected holes is obtained after pulsing at –8 V corresponding to an average field around 4.5 MV/cm, with a slight distortion of the C-V characteristics. Higher pulse amplitudes increase the charging while the C-V curves become grossly non-parallel. At –11 V the \( \Delta V_{FB} \) reaches 1 V and the C-V characteristic becomes parallel again to the initial. The corresponding G-V characteristics monitored after pulsing with negative gate voltages reveals a prominent double peak structure that appears at the beginning of the positive charging, an indication of two distinct interfacial defects. Moreover, the evolution of the double peak structure as the pulse amplitude increases indicates that the two peaks are strongly interrelated since the one peak (peak B) grows at the expense of the other (peak A).

The response of the two conductance peaks with frequency is shown in figure 3. The measurements were performed after applying negative pulses of amplitude –10 V and width 200 ms within the frequency range 1 MHz to 8 kHz. Both peaks follow a similar response with frequency, typical of interfacial defects with an energy distribution close to the valence band edge. The ability of peak B to exchange charge with the silicon substrate at high frequencies (1 MHz) indicates further that this defect is at the interface and very near to the valence band edge.

The evolution of the positive charging process was also monitored by applying pulses of increasing width from 50 ms to 1 s, while the height was kept constant at –10 V (figure 4). In this case prior to each pulse the structure was discharged to its initial uncharged state. The results are almost identical to those of figure 2 and showing the transient nature of the positive charging process. Increasing the pulse width results in increased charging, with a simultaneous development of a double peak structure, which disappears at the higher values of the pulse width.
The presented results suggest that electron trapping occurs within the Si-ncs away from the tunnel oxide substrate interface, while holes are initially trapped to oxide defects located at the tunnel oxide-substrate interface and then they are transferred to the Si-ncs. This results to the non-parallel shift of the C-V characteristics. This process of near interfacial oxide trap filling requires an electric field approximately of 4.5 MV/cm, indicating that in their uncharged state the distribution of the defect energy levels is located well below the Si valence band edge. By increasing the electric field the upper part of this distribution is gradually aligned with the substrate valence band edge and thus hole injection from the accumulation layer occurs to the near-interfacial traps [8]. The positively charged near-interfacial oxide traps interact strongly with the interface traps producing a splitting of the continuous distribution into two separate contributions. Once positively charged, these defects can transfer further their charge to the Si-ncs. For fields below 5 MV/cm this charge transfer is relatively slow giving rise to a time dependent effect. For fields higher than 5MV/cm the trapped holes cannot be sustained to the near-interfacial traps and they are transferred to the Si-ncs, restoring thus the C-V and G-V characteristics to their initial shape, although shifted almost by 1V.

**Figure 1.** C-V characteristics of capacitors structures obtained after charging by applying sequential positive (a) or negative (b) gate voltage pulses of width 100 ms. The structures were not discharged prior to the application of a new pulse.

**Figure 2.** Evolution of the conductance characteristics as a function of negative gate pulses, illustrating the development of a double peak structure.

**Figure 3.** Frequency response of the conductance characteristics obtained after a single gate voltage pulse of –10 V amplitude at 200 ms.
A high-temperature annealing step at 1000 °C for 1 h was found to decrease both the density of the interface and the near-interface oxide traps. This reduction has a strong impact on the hole charging characteristics. This is illustrated in figure 5 where a shift of the G-V characteristics of the order of 1 V requires a fivefold increase in the pulse width as compared to the as-grown sample.

4. Conclusions
The charging characteristics of Si-ncs embedded within SiO₂ in the investigated samples were controlled by the presence of near-interfacial oxide hole traps. These traps couple the substrate holes and the Si-ncs and give rise to a time dependent charging effect. Holes are initially injected to these oxide traps and they are then transferred to the Si-ncs. Hole charging of the near-interfacial oxide traps was found to modify substantially the distribution of the interface traps. Reduction of the density of these traps by high temperature annealing reduces accordingly this coupling between the Si-ncs and the substrate.

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6. References
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