Silicon-based Packaging Platform with Embedded Solder Interconnections for Light Emitting Diode

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Abstract. In this paper, we demonstrate a silicon-based packaging platform for a package component of Light Emitting Diode (LED) using silicon bulk micromachining technique and using the silicon substrate with embedded solder interconnections to dissipate heat and the match thermal expansion coefficient (CTE). The objective is to develop an LED package that can overcome life time, high operating voltage, package degradation and has the ability to drive the devices at higher power and higher brightness. The results reported in before show that the silicon substrate can enhance heat removal for safe junction temperature operation and minimize thermal stress caused by mismatch of CTE. Moreover, silicon-based packaging platform with embedded solder interconnections has been fabricated in this study, and this technique can be used for packaging conventional optoelectronic semiconductor devices such as laser diode or MEMS devices.

1. Introduction

The conventional LEDs have superior characteristics such as long life, low power consumption, high brightness, and low cost. These characteristics have resulted in a variety of applications such as household illumination, full color display, automotive taillight, backlight, and traffic signals. However, even the most powerful LED being made is still an order of magnitude too low in flux per LED, and two orders of magnitude too high in cost per lumen to significantly penetrate the general illumination market. These problems make the realization of high-resolution, high-brightness, high-density and low-cost luminous devices or displays difficult. In particular, a typical thermal design problem for LED system is depending on the efficiency of LED packaging [1-3].

With the continuous improvement in LED packaging, several packaging methods for improving high-power LED performance have been proposed [4, 5]. These packages use a conducting layer deposited on the surface of silicon substrate to accomplish electrode interconnections and signal propagation. However, an LED array unit of higher density is always poses limitation to the layout of connected electrodes with the complicated arrangement of conducting wires. Although previous works [6, 7] have been proposed the through-hole-wafer interconnection pins fabricated by combining Deep Reactive Ion Etching (DRIE) with electroplating techniques to eliminate the need for wire bonding and to reduce packaging size, but these methods needed more complex fabrication processes and higher cost.
To solve above-mentioned problems, this study develops and fabricates a silicon-based packaging platform with embedded solder interconnections for a package component of LED. The major advantages of this packaging method are that it enhances heat removal for safe junction temperature operation, and minimizes thermal stresses caused by mismatch of CTE between package substrate and LED crystallite. Another advantage is the design can minimize the final package size and be integrated with a circuit board, so that it can therefore adequately meet the requirement of high-density LED array unit for display panel application.

2. Design
The packaging design we developed is shown in Fig. 1. A silicon wafer serves as a substrate. The cavity (micro-reflector) and two electrode-guided through holes are formed by photolithography and anisotropic wet-etching techniques. The solder interconnections embedded in the through holes are taken as positive and negative electrodes. The through hole contact design offers the advantages of shorter signal line length and smaller package size. In this designing figure, \( L \) and \( h \) denote the square length of open area and the depth of micro-reflector, respectively; and \( \theta \) denotes the angle of reflection.

![Fig. 1 Schematic structures of the proposed packaging platform](image)

3. Fabrication and Results

3.1. Micro-reflector fabricatio
Figure 2 shows the basic fabrication processes of silicon micro-reflector. First, the bulk micromachining process starts with a \(<100>\) p-type silicon wafer (Fig. 2a). Then the single-crystal silicon wafer is placed in a furnace and then thermally oxidized to grow a layer of 1 \( \mu \)m thick silicon dioxide (Fig. 2b). Second, the oxide layer is patterned (mask#1 and mask#2) to define the etching windows of the silicon wafer (Fig. 2c), and then the protective layers within the etching regions being etched by BOE to expose the etching regions of silicon (Fig. 2d). Third, the etching regions are etched by non-isotropic wet etching (KOH) to a certain depth, which forms a depression in the silicon wafer and at the same time two through holes on the bottom (Fig. 2e). Fourth, the silicon substrate is placed in the furnace to grow a layer of silicon dioxide as an insulation layer (Fig. 2f). Finally, the larger open window of the through hole is set face up and conductive materials such as solder past are respectively printed into the through holes at the bottom (Fig. 2g). Then the substrate is placed on a hotplate and heated to soften the solder materials, making them fill up the through holes to form metal interconnections (Fig. 2h).
Figure 3 shows the SEM diagram of the fabricated silicon substrate with four through holes for each micro-reflector. The thickness of the p-type silicon substrate is around 430 μm. The exposed silicon area was etched in KOH (25%) at 80°C for 5 hours, giving the square length L of micro-reflectors from 1.8 to 3 mm and an etching depth of around 330 μm. The measured height and upper width of the through holes are approximately 100 μm and 290 μm, respectively. However, the dimensions of the fabricated micro-reflector are defined by the actual wafer thickness, etching time, and the patterned etching window of micro-reflector or/and through holes.

3.2. Embedded solder interconnections

3.2.1. Solder paste printing

The embedded solder interconnection was fabricated by solder paste printing and reflow processes. In this experiment, the soldering process involved the following two steps. First, solder paste (Sn63/Pb37) is printed on the silicon backside by manual filling as the micro-reflector placed face down and up during the heating process to make the solder flow into the through holes. The solder paste was then melted by a heater at a heating temperature of 185°C. The typical fabrication results are shown in Fig. 4 and Fig. 5, respectively. As show in Fig. 4, the solder paste has formed out of the front end and within the back end of the through holes. However, the result shown in Fig. 5 is contrary to that of Fig. 4, indicating that the weight of the solder material could directly affect the formed geometry during the heating process.
Fig. 4 Microphotography of the solder interconnection forming under the expression placed face down during reflow process: (a) Front view, and (b) Back view.

Furthermore, the variation of these protruding sizes shown in Fig. 4(a) is attributed to the different sizes of these through holes, and the concave profile on the top of the protrusion is caused the thermal shrinkage effect. However, in the case shown in Fig. 5, not only a flat surface profile can be seen on the front end of the solder interconnections but also a protruding shape is found on the backside of the silicon substrate. Comparing these results of solder interconnection formed in this research shows that using solder paste reflow technique according to the arrangement of micro-reflectors faced up during heating is beneficial to the subsequent of step of mounting LED crystallize and connecting electrodes. Moreover, this technique can not only reduce the final packaging size but also manufactured in batch process.
3.2.2. Mechanical / Electrical performance

The electrical interconnection fabricated by solder paste reflow process was polished from the bottom side by fine-grain sandpaper. The typical SEM cross-section view on the plane was shown in Fig. 6. There is a flat solder surface with a local oxide layer and multi-scratches resulted from the sandpaper scrape. However, there is no obvious crack or any residual hole existing within the solder interconnection. This reveals that the solder paste reflow formed can provide excellent electrical interconnect reliability.

Fig. 5 Microphotography of the solder interconnection forming as the expression placed face up during reflow process: (a) Front view, and (b) Back view.

(a) 
(b) 

Fig. 6 Microphotographs of the solder interconnection after being polished by sandpaper: (a) surface profile, and (b) close view of the box dotted-line.

DC resistance of the embedded solder conductor in Fig. 5 has also been measured using a simple two-point probe. Two probes are brought into contact to both ends of solder interconnections. The measured DC resistance of the solder interconnections for all dimensions are around 4–6 Ω and for probing two solder interconnections at a distance of 150 μm are approach to infinity, and therefore it has the potential for improving the performance of the electrical interconnection.
4. Conclusion
A novel silicon-based packaging platform with embedded solder interconnections has been developed for packaging optoelectronic semiconductor devices such as LED. The fabrication processes and mechanical/electrical characteristics were experimented and measured. This packaging structure fabricated by silicon bulk micromachining can be used to effectively improve the reliability and thermal fatigue of high-power LED package, and a high-density LED array unit for display panels can be realized at a low production cost because a batch process can be used to fabricate the micro-reflector array units. We also experimentally confirmed that the embedded interconnection can be fabricated by appropriate reflow condition of solder paste. This technique will enhance the packaging potential and incorporate some advantages of MEMS/IC packaging.

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