Low Noise, High Input Impedance Digital-Analog Hybrid Offset Suppression Amplifier for Wearable Dry Electrode ECG Monitoring

Weilin Xu *, Taotao Wang, Xueming Wei, Hongwei Yue, Baolin Wei, Jihai Duan and Haiou Li

Guangxi Key Laboratory of Precision Navigation Technology and Application, Guilin University of Electronic Technology, Guilin 541004, China; wtao_1994@163.com (T.W.); scuweixue@guet.edu.cn (X.W.); guetyhw@163.com (H.Y.); guilinwxb@163.com (B.W.); djh@guet.edu.cn (J.D.); Lihaiou@guet.edu.cn (H.L.)

* Correspondence: xwl@guet.edu.cn; Tel.: +86-0773-229-0203

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Abstract: The portable real-time electrocardiogram (ECG) is a convenient and promising electronic device for cardiovascular diseases patients. However, unlike wet gel electrodes in traditional clinical applications, dry electrodes are competent for comfortable long-time wearing and can prevent skin ulceration. Its ultra-high source impedance and electrode offset (EOS) make traditional chopper amplifiers with low input impedance and limited EOS range difficult to apply to this area. To overcome these challenges, this paper proposes a novel chopper amplifier topology. This architecture includes a gain control loop, a ripple reduction loop, and a DC-servo loop (DSL). The proposed sampling input stage and digital-analog hybrid DSL are employed to boost input impedance and extend the EOS handing range. Designed with a 0.18 µm 1P6M 1.8 V CMOS salicide process, the proposed chopper capacitively coupled instrumentation amplifier achieves an ultra-high input impedance of 120 GΩ (<0.05 Hz) or 2.1 GΩ (0.6~250 Hz), an EOS handing range of ±325 mV and a low noise of 1.9 µVrms at 0.6~250 Hz. It occupies an area of 0.36 mm² and only consumes a quiescent current of 11 µA.

Keywords: (electrocardiogram) ECG; sampling input stage; chopper amplifier; ultra-high input impedance; (electrode offset) EOS

1. Introduction

Cardiovascular diseases (CVDs) are the biggest killer of global human health. Of all worldwide deaths every year, nearly 31%, a conservatively estimated 17.9 million, are caused by CVDs [1]. As one of the major physiological vital signs, the electrocardiogram (ECG) is widely recognized as a diagnostic tool and standard for medical and research purposes. Real-time ECG monitoring shows clear advantages in preventing CVDs [2]. However, the traditional clinical ECG with wet gel electrodes (usually Ag/AgCl electrodes) normally requires a galvanic contact to the body and often skin preparation, which may cause skin irritation. Dry electrodes solve this problem by eliminating the need for gel, which in turn enables a faster setup time and improves patients’ comfort. However, the flaw is its high electrode-skin impedance. Typical dry-electrode impedance is in a range from a few hundreds of kiloohms to a few tens of megaohms [3], leading to a large signal attenuation and a significant increase in noise and offset [4].

A reliable, real-time portable ECG monitoring system has to satisfy some challenging requirements. First of all, it must be able to cope with the effects of large skin-electrode impedance changes on the signal, usually by a pre-amplifier with very high input-impedance to minimize signal attenuation and degeneration [5]. Chopper-stabilized amplifier is a popular front-end topology for ECG monitoring and neural recording [6–10], as the chopper technique is an effective way to suppress low-frequency
flicker noise of the amplifier [11]. However, chopping reduces the DC input impedance of the amplifier because the passive mixer at the input together with the input capacitor forms a switched-capacitor resistance. To boost the input impedance, a positive-feedback loop has been used in [7]. However, the positive-feedback loop is rendered inoperative at DC, and due to the parasitic capacitance appearing at the input node, the realized impedance boost is limited to a factor of 5 [8]. Another challenge is the electrode offset voltage, which can be as large as several hundred millivolts. It may reduce the pre-amplifier’s headroom or even easily saturate its output [5]. In such a case, a DC-servo loop (DSL) is usually employed to attenuate the electrode offset (EOS) at the output. However, it has to tradeoff between capability of handling EOS and noise [12].

This paper presents a low noise, high input impedance digital-analog hybrid offset suppression amplifier to address the aforementioned challenges. The main amplification path is a chopper-stabilized amplifier, which effectively suppresses the low-frequency flicker noise. To boost the input impedance at the ECG frequency range of 0~250 Hz, a sampling input stage has been adopted. A digital-analog hybrid servo loop is employed to attenuate the EOS at the output, which can reduce the noise contribution of the servo loop and keep the capability of handling EOS voltage. A ripple reduction loop (RRL) is used to attenuate the ripple at the outputs. The gain of the circuit is determined by the gain control loop. This paper is organized as follows. Section 2 describes the architecture of the proposed circuit. Section 3 discusses the detail circuit implementation. Section 4 presents the results of system characterization and a comparison table. Section 5 concludes the paper.

2. System Overview

The proposed system diagram is shown in Figure 1. This ECG amplifier system consists of sampling input stage, chopper amplifier, ripple reduction loop, gain control loop and digital-analog hybrid DSL. The chopper amplifier adopts a basic two-stage Miller compensated amplifier, which is composed of MX1, MX2, \( C_{IN} \), \( G_{m1} \), \( G_{m2} \), \( C_{31} \) and \( C_{32} \). It has two feedback connections for gain control and ripple reduction, respectively. Its circuit implementation will be described in Section 3. The gain control loop of the ECG amplifier consists of \( MX_4 \), \( C_{1x} \), \( C_{2x} \) and \( FB_1 \), which defines the pass-band gain as:

\[
G_0 = \frac{G_{m1} C_{21} + C_{11}}{FB_1 C_{11}} \tag{1}
\]

![System diagram of the proposed digital-analog hybrid offset suppression electrocardiogram (ECG) amplifier.](image-url)
The drawback of chopper amplifier is that its input signal becomes DC-coupled, because the input signal is shifted to its chopping frequency. Hence a DSL should be added to suppress the EOS and implement a high-pass corner frequency at $f_L \approx 0.6$ Hz. The high-pass corner frequency is [12]:

$$f_L = \beta G_0 f_0$$  

(2)

where $\beta$ is the attenuation coefficient of the attenuator in the analog DSL, $G_0$ is the closed-loop gain of the chopper amplifier, and $f_0$ is the unity gain frequency of the analog DSL. In this design, $G_{m1}/F_{B1} = 6.2$, $C_{21}/C_{11} = 34$, $\beta = 0.1$, $f_0$ is about 35.6 mHz. Thus, the pass-band gain and the high-pass corner frequency are around 217 and 772 mHz, respectively.

As shown in Figure 1, the input of $G_{m1}$ is not a voltage feedback node or a “virtual ground”, because the RRL, analog DSL and gain control loop are not connected to the input of $G_{m1}$. Thus, the input equivalent capacitance is equal to the series capacitance of $C_{IN}$ and $C_{par}$. The differential input impedance is determined by the equivalent switched-capacitor resistance:

$$Z_{in} = \frac{1}{4f_{CH}(C_{IN}C_{par})(C_{IN}+C_{par})} \approx \frac{1}{4f_{CH}C_{par}}$$  

(3)

where $f_{CH}$ is the chopping frequency, $C_{par}$ is the parasitic capacitance appearing at the input of $G_{m1}$. Usually $C_{par}$ is very small so that the input impedance $Z_{in}$ is high enough. In this design, the input differential pairs work in sub-threshold region to minimize the parasitic capacitance, and $C_{par}$ is about 5 fF, $f_{CH} = 20$ kHz. Thus, the input impedance is around 2.5 GΩ at the passband.

The input-referred noise of the whole chopper amplifier due to the white noise of the pseudo resistor (P-RES) and $G_{DSL}$ can be estimated as [12]:

$$V_{n, in}^2 \approx \frac{1}{2\pi C_{G0} C_{61}} + \beta^2 V_{n,GDSL}^2 f_H$$  

(4)

where $f_H$ is the $-3$ dB frequency of the chopper amplifier. In order to minimize the noise, a smaller attenuation coefficient $\beta$ of the attenuator is preferred. However, a small $\beta$ will limit the capability of handling EOS. Hence the digital DSL was used to extend the EOS handling range.

3. Circuit Implementation

In the previous section, we have presented an overview of the system, and in this section, we will discuss the circuit-level implementation issues in details.

3.1. Two-Stage Chopper Amplifier

The main two-stage amplifier ($G_{m1}$, $G_{m2}$), the gain control transconductance ($F_{B1}$), and the ripple compensation transconductance ($F_{B2}$) are shown in Figure 2. In order to achieve high input impedance, $F_{B1}$ and $F_{B2}$ are added to provide current feedback. Additional feedback increases circuit noise unavoidably. It means that there should be distributed current properly to minimize noise. Additionally, to increase the noise efficiency, the input pairs are biased in sub-threshold region and the current of $G_{m1}$ is seven times larger than that of $F_{B1}$ and $F_{B2}$. The Miller compensation capacitors are $C_{3x}$ and are also used as a low-pass filter capacitor.
structure to implement a continuous-time system. K1x and K2x are controlled by a non-overlapping clock. During the signal phase \( \Phi_1 \), K2x are open and K1x are closed. During the signal phase \( \Phi_2 \), K2x are closed and K1x are open.

3.2. Sampling Input Stage and Input Impedance

3.2.1. Sampling Input Stage

To boost the input impedance at low frequency, the DSL feedback loop cannot be connected to the input of \( G_m1 \). Therefore, the sampling input stage is added to the system for easy access to DSL feedback. The sampling input stage is shown in Figure 3. Block1 and block2 act as a ping-pong structure to implement a continuous-time system. \( G_{m1} \) and DSL feedback are connected to the input of \( G_m1 \). Therefore, the sampling input stage is added to the system for easy access to DSL feedback.

\[ V_{CS1} = V_{inm} - V_{DDSLn} \]
\[ V_{CS2} = V_{inm} - V_{DDSLp} \] (5)

During the sampling phase \( \Phi_1 \), the voltages over the sampling capacitors \( C_{S1} \) and \( C_{S2} \) can be expressed as:

During the signal phase \( \Phi_2 \), the input voltage \( V_{ampp} \) can be expressed as:

\[ V_{ampp} = V_{ampp} - V_{ampn} = (V_{CS2} + V_{ADSLP}) - (V_{CS1} + V_{ADSLn}) \]
\[ = V_{inm} - V_{inm} - [(V_{ADSLn} - V_{ADSLP}) + (V_{DDSLP} - V_{DDSLn})] \] (6)
Let $V_{ADSL} = V_{ADSLp} - V_{ADSLn}$, $V_{DDSL} = V_{DDSLp} - V_{DDSLn}$, $V_{DSL} = V_{DDSL} - V_{ADSL}$, we have:

$$V_{ampin} = V_{inp} - V_{inn} - (V_{DDSL} - V_{ADSL})$$

$$= V_{inp} - V_{inn} - V_{DSL} \tag{7}$$

A point of note from Equation (7) is that the sampling input stage can effectively implement DSL feedback. If $V_{DSL}$ is equal to the EOS, the DC portion of the input signal will be removed.

3.2.2. Input Impedance

The traditional chopper capacitively coupled instrumentation amplifier with DSL is shown in Figure 4a. According to the analysis in [8,12], the positive feedback loop is rendered inoperative at DC. Therefore, the DC input impedance can be expressed as:

$$Z_{in,dc} = \frac{1}{4f_{CH}C_{in}} \tag{8}$$

With the typical values of $C_{in} = 10 \text{ pF}$ and $f_{CH} = 20 \text{ kHz}$, the DC input impedance is limited to $1.25 \text{ M} \Omega$, which is significantly lower than the basic requirement of $1 \text{ G} \Omega$.

![Figure 4. DC input impedance analysis: (a) traditional (b) proposed.](image-url)

The equivalent input impedance of the proposed sampling input stage circuit is shown in Figure 4b. As the RRL is a narrow bandpass feedback, it has little effect on the input impedance at the frequency of interest. Thus, the RRL is not included in Figure 4b. During the sampling phase $\Phi_1$, the voltage of $C_S$ tracks the input signal. During the signal phase $\Phi_2$, the electronic charge transferred from $C_S$ to the chopper amplifier. According to the principle of switched capacitor, the charge charged to $C_S$ in the sampling phase of the previous cycle is equal to the charge transferred to the chopper amplifier in the next cycle ($Q_1 = Q_2$). Ignoring the sampling loss, the input terminal current is equal to the input
current of the chopper amplifier. Thus, the differential input impedance is determined by the input parasitic capacitance of the chopper amplifier and the chopping frequency; the expression has been given as Equation (3). With the typical values $C_{par} = 5 \, \text{fF}$ and $f_{CH} = 20 \, \text{kHz}$, the input impedance up to 2.5 GΩ in the signal frequency. Meanwhile, if the loop gain is infinite, $V_{DSL}$ is equal to EOS in Equation (7) and $V_{ampin,dc} = 0$. Therefore, the DC input current is zero and the DC input impedance is infinite. In fact, the DC input impedance is higher than 170 GΩ, even in view of the limited loop gain.

### 3.3. Digital-Analog Hybrid DC-Servo Loop

The DC-servo loop is employed to attenuate the EOS at the output, which is actually equivalent to a low pass filter. It can be seen from Figure 1 that the noise of the DSL circuit is chopped twice. Therefore, the DSL circuit noise cannot be reduced by chopping and it directly affects the noise performance of the entire circuit. In order to analyze the noise of the DSL, the circuit can be simplified to Figure 5a, where $V_n$ is the equivalent input-referred noise of the DSL amplifier. Since $f_{H}$ is much smaller than $f_{sig,min}$, the impedance of the capacitor is much smaller than the impedance of the resistor. Ignoring the impedance of the capacitor as shown in Figure 5b, we can find that the output noise is equal to the input noise and it is independent of the amplifier gain.

![Figure 5](image_url) **Figure 5.** Noise analysis of the DC-servo loop (DSL) circuit: (a) complete version, (b) simplified version.

In Figure 1, the attenuator was added to reduce the noise contribution of the DSL. The behavioral level model of the DSL with attenuator is shown in Figure 6. $V_{n1}$ and $V_{n2}$ are the main sources of noise in the system, being $V_{n1}$ and $V_{n2}$ the input-referred noise sources of the chopper amplifier and the DSL, respectively. The system input noise can be expressed as:

$$V_{n,tol} = V_{n1} + \beta V_{n2}$$

(9)

![Figure 6](image_url) **Figure 6.** Behavioral level model of the DSL with attenuator.
In order to minimize the noise due to the DSL, a smaller $\beta$ is preferred. As an example, if $\beta = 0.1$, the total noise is reduced by 10 times, because the noise of the chopper amplifier is far less than that of the DSL. Meanwhile the noise of the DSL is independent of the gain $A_2$, which can maintain the loop gain by increasing the gain of the DSL. However, since $|V_{EOS}| < \beta V_{supply}$, $V_{EOS}$ is limited to $\pm 180$ mV when $\beta = 0.1$ and $V_{supply} = 1.8$ V. It is lower than the required $\pm 300$ mV. To extend $V_{EOS}$ without increasing noise, a digital DSL is added in Figure 7a.

**Figure 7.** (a) Circuit implementation of the digital-analog hybrid DSL, (b) the digital-to-analog converter (DAC) of the digital DSL, (c) the shift of the DAC flow chart.
The digital-analog hybrid DSL has two comparators to monitor the differential outputs of the low pass filter ($V_{Lp}$ and $V_{Ln}$). The analog compensation voltage $V_{ADSLp}$ and $V_{ADSLn}$ are obtained from $V_{Lp}$ and $V_{Ln}$ through the attenuator. When $V_{Lp}$ is higher than reference voltage $V_{CM}$, the DAC will decrease the output voltage at the next clock. From Equations (6) and (7), $V_{Lp}$ will decrease when the differential outputs of the DAC decreases. Likewise, $V_{Ln}$ will decrease when the differential outputs of the DAC increase. In this way, when the DAC output range is ±210 mV, LSB is 70 mV and the output range of the low pass filter is bigger than 1 LSB, the EOS handling range is extended to

$$V_{EOS} \leq \pm [\beta V_{supply} + 210\text{mV}]$$  \hfill (10)

Furthermore, the cycle time of the DAC has to longer than the settling time of the analog DSL loop. The DAC of the DSL is shown in Figure 7b. The shift register controls eight switches to encode the output voltage, and the rest module monitors the output. At the same time, $M_{11}$~$M_{14}$ or $M_{21}$~$M_{24}$ turn on only one, otherwise, the shift register output will be reset to 1. The working flow chart of the shift register is shown in Figure 7c.

3.4. Ripple Reduction Loop (RRL)

As shown in Figure 8, the offset of the transconductance $G_{m1}$, being chopped by MX2, appears as a square wave voltage. Then, the square wave voltage is integrated into a triangular wave to form an output ripple [13]. The RRL is used to suppress the output ripple, which consists of capacitor $C_4$, chopper MX3, integrator and feedback transconductance $FB_2$. This can be explained as follows. The capacitor $C_4$ converts the output ripple into a square wave current. This current is chopped by MX3, and the resulting DC current is integrated to generate a DC compensation voltage that can eliminate the offset of the transconductance $G_{m1}$.

![Figure 8. Simplified block diagram of the Ripple Reduction Loop (RRL).](image)

4. Simulated Results

The proposed ECG amplifier was designed in a 0.18 µm 1P6M 1.8 V CMOS salicide process and simulated with Spectre of Cadence EDA software. The layout is shown in Figure 9. This chopping and DAC sampling frequencies are 20 kHz and 100 Hz respectively.
The input impedance of the ECG amplifier using different impedance-boost techniques is shown in Figure 10. This clearly shows that the proposed sampling input stage has better impedance improvement effect than aux-path technique and positive feedback (FB) technique. As described above, the DC input impedance is boosted to 120 GΩ at 0.05 Hz by the sampling input stage; at pass-band, the input impedance is 2.1 GΩ, which is determined by the equivalent switched-capacitor resistance of the chopper amplifier. The proposed ECG amplifier with very high input impedance characteristic can be applied to dry electrodes applications easily, which can effectively reduce the effects of signal attenuation and impedance variation interference, and its ultra-high DC impedance can reduce its input offset and DC current.

Figure 10. The input impedance of the ECG amplifier using different impedance-boost techniques.

Figure 11 shows the transient waveform of the ECG amplifier with and without digital DSL. The range of EOS handling is less than ±300 mV when only use analog DSL. Its output is obviously saturated. However, the digital-analog hybrid DSL can effectively expand the EOS handling range.
0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5
-2
-1
0
1
2
only analog DSL

digital-analog hybrid DSL

Figure 11. The transient waveform of the ECG amplifier with and without digital DSL.

Figure 12 shows the input-referred noise power spectral density with and without attenuator, respectively. The results show that the system noise can be suppressed by adding an attenuator to the output of the analog DSL, and the integrated noise with attenuator on 0.6 Hz to 250 Hz is 1.9 µVrms.

Figure 13 shows the AC frequency response of the ECG amplifier at different EOS. The passband gain is 46 dB, and the high-pass cut-off frequency is 0.6 Hz. Their variations are less than 1 dB and 0.4 Hz respectively when the EOS changes within ±325 mV. The very low high-pass cut-off frequency can effectively filter out ECG baseline drift and EOS interference.

Figure 14 shows the Monte Carlo simulation results, which can predict the reliability of physical implementation in advance. The simulation results show that the CMRRR is greater than 88 dB in 84.13 %, the gain fluctuation is less than 1 dB at the same EOS, and the input offset voltage is less than 181 µV in 95.44 %. The results show that the proposed circuit has good process stability.

Figure 12. The input-referred noise of the ECG amplifier with and without attenuator.
Figure 13. The AC frequency response of the ECG amplifier at different electrode offset (EOS).

Figure 14. The Monte Carlo analysis of: (a) CMRR, (b) Closed-loop gain, (c) Input offset.
Table 1 summarizes the main performance parameters of this work, and compares the parameters with the state-of-the-art implementations. The portable ECG and neural monitoring applications tend to implement low noise, high input impedance and low power consumption. The capacitively coupled instrumentation amplifier without chopping in [14] has very high input impedance, but its input-referred noise and power consumption are higher than chopper amplifiers in [8,12,15,16]. On the other hand, the chopper amplifier without DSL in [15], must have a large off-chip capacitor to avoid the influence of EOS. In this work, the DC input impedance (120 GΩ@0.05 Hz) and passband impedance (2.1 GΩ) are boosted significantly, while achieving the state-of-the-art EOS range and noise performance. It effectively balances the performance of input impedance, EOS range and noise.

Table 1. Performance Comparison and Summary.

| Parameter                  | [12]  | [8]  | [14]  | [15]  | [16]  | This Work   |
|----------------------------|-------|------|-------|-------|-------|-------------|
| Technology                 | 130 nm| 40 nm| 180 nm| 130 nm| 180 nm| 180 nm      |
| Supply (V)                 | 1.2   | 1.2  | 5     | 1.2   | 1.2   | 1.8         |
| Bandwidth (Hz)             | 0.6–8 k| 1–200| 0.5–100| 0.2–100| 0.5–500| 0.6–1k      |
| Low-frequency cut-off (Hz) | 0.6   | 10   | 0.5   | 0.2   | 0.5   | 0.6         |
| Input Impedance (Ω)        | -     | 20 M | 5 G   | 10 M  | 1 G   | 2.1 G       |
| dc Input Impedance (Ω)     | 2.5 M | 300 M| 400 G | 200 M | -     | 120 G       |
| EOS range (mV)             | ±50   | ±50  | -     | ±200  | ±325  | ±325        |
| Input-referred Noise (µVrms)| 1     | 2    | 3.7   | 1.31  | 1.8   | 1.9         |
| GAIN (dB)                  | 40    | 26   | 0/9/13/20| 40   | 40    | 46          |
| Supply current (µA)        | 2.9   | 1.7  | 18    | 0.36/ch| 2     | 11          |
| CMRR (dB)                  | 85    | -    | 70    | 98    | 90    | 96          |
| AREA (mm²)                 | 0.2   | 0.071/ch| 1.23 | 0.68  | 0.46  | 0.36        |
| Application                | ECG   | Neural| ECG   | ECG   | ECG   | ECG         |

5. Conclusions

This paper presents a chopper stabilized amplifier capability of wearable dry electrode ECG monitoring in the presence of large EOS and source impedance. By the chopper stabilized technology, the 1/f noise was effectively suppressed, while the noise of the DSL was suppressed obviously by the attenuator. The digital-analog hybrid DSL with sampling input stage, which feedback by the switched capacitor technology, boosted the DC input impedance up to 120 GΩ and extended the EOS handling range to ±325 mV. The high passband input impedance was achieved by the current feedback technology. The ECG amplifier only has 1.9 µVrms integrated noise from 0.6 Hz to 250 Hz, which effectively balance the performance of the input impedance, EOS range and noise. The low noise, ultra-high input impedance digital-analog hybrid offset suppression amplifier is appropriate for wearable dry electrode ECG monitoring applications.

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