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ABSTRACT

Two-dimensional (2D) materials have gained huge attention due to their ultimate thinness that can help dominate the short channel effect caused by transistor miniaturization. Molybdenum disulphide (MoS$_2$) is one of the most promising 2D materials that has an extremely thin body, facilitates aggressive scaling, and has a high intrinsic bandgap, which allows it to be utilized fairly for transistor applications. In this work, we report a 2D MoS$_2$ based negative capacitance field effect transistor with a novel HfO$_2$/TiO$_2$/HfO$_2$ tri-layer structure as the high-K gate oxide and lead zirconate titanate, Pb(Zr$_{1-x}$Ti$_x$)$_2$O$_3$ (PZT), as the ferroelectric in the gate stack. The extensively high $I_{on}/I_{off}$ of $3 \times 10^{14}$ (~six orders higher) and the large transconductance of 1.15 mS/μm (~25 times higher) are the most spectacular output characteristics of the device, which outperforms all the previous results. The incorporation of a negative capacitance effect exhibits a minimum subthreshold swing of 42.6 mV/dec, which can be realized by introducing 50 nm of a ferroelectric PZT layer over the gate dielectric. Furthermore, a high improvement in the on-state current of ~177 μA/μm was reported. These results indicate that the proposed device structure provides a new insight into nanoelectronic devices with ultra-low power consumption.

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I. INTRODUCTION

To meet the demand of the modern era of information revolution as well as performance improvement, the constant advancement of MOSFET scaling is a vital issue. The miniaturization of the transistor and its high-density integration on a chip results in short-channel effects (SCEs), which has brought a large amount of power dissipation of the device. Getting rid of the SCE for low-power applications is becoming a major challenge. A possibility to overcome the restrictions of Si MOSFETs is the concept of incorporating novel channel materials with the field effect transistor (FET) technology. From this perspective, two-dimensional (2D) transition metal dichalcogenides (MoS$_2$, WS$_2$, and MoTe$_2$) have gained much popularity. In particular, single-layer MoS$_2$ is of great research interest due to its device applicable large intrinsic bandgap, high on/off ratio, and high carrier mobility. Its ultra-thin body is useful for electrostatic control within the channel and aggressive scaling that enables size-scalable transistors. The use of 2D MoS$_2$ gives improved stability of the device capacitance ($C_d$), offering a greater area of the surface to the volume ratio, and a more obvious negative capacitance (NC) effect is produced.

To decrease power dissipation in nanoscale devices, the use of NC exhibited by ferroelectric (FE) materials is a promising way and found to be of great interest in recent years. One of the key parameters of switching devices is how sharp they change their state from the off-state to the on-state. This parameter can be realized by the “subthreshold swing” (SS) of the device. It is, therefore, a very important parameter which reduces the transistor’s power consumption within the switching event. In general, the SS of a FET can be expressed as $SS = \frac{\partial V_t}{\partial \log(I_d)}$. In the case of incorporating an FE layer, the surface potential $\psi_s$ is formed within the...
TABLE I. MoS$_2$ parameters used for the device simulation.

| Parameter name          | Unit | Value   |
|-------------------------|------|---------|
| Bandgap energy          | eV   | 1.8     |
| Dielectric constant     |      | 7       |
| Electron affinity       | eV   | 4.0     |
| Electron effective mass |       | 0.52    |
| Hole effective mass     |       | 0.64    |
| Saturation velocity     | V/cm | $2 \times 10^{-7}$ |
| Electron mobility       | cm$^2$/V s | 25   |
| Hole mobility           | cm$^2$/V s | 25   |

gate oxide and the FE layer. Hence, the above expression can also be written as $SS = \frac{Q_{G}}{Q_{SS}} \times \frac{Q_{SS}}{Q_{VSS}}$. The Boltzmann thermal limit dictates that the second term $\frac{Q_{SS}}{Q_{VSS}}$ for a conventional FET cannot be lower than 60 mV/decade at room temperature (300 K). However, the magnitude of SS can be reduced to below 60 mV/dec by using the NC effect shown by FE materials. Several experiments until now were demonstrated for MoS$_2$ MOSFETs having NC effects. Good results of the SS were also found from those experiments. In those studies, the SS was pulled down within the sub-60 mV/dec region, and ferroelectric materials like polyvinylidene fluoride-co-trifluoroethylene [P(VDF-TrFE)], hafnium zirconium oxide (HfZrO$_2$), and Al-doped HfO$_2$ were used. On the other hand, a comparatively lower on–off current ratio and transconductance are the important challenges requiring further study. Hence, a new device concept or new physics is the urgent need to further improve device performance.

The present work demonstrates an MoS$_2$ FET with a lead zirconate titanate, Pb(Zr$_{0.3}$,Ti$_{0.7}$)O$_3$ (PZT), FE material in the gate stack to form a NCFET having a higher on–off ratio, a lower subthreshold swing, superior transconductance, and reduced device dimension to the nanoscale range. We propose a novel HfO$_2$/TiO$_2$/HfO$_2$ tri-layer structure as the high-K gate oxide on the MoS$_2$ channel. A remarkably enhanced current on–off ratio of $3 \times 10^{14}$ (~six orders higher) as well as a highly enriched transconductance value of 1.15 mS/µm (~25 times higher) has been obtained, which outperforms all the previous results. A high improvement in the on-state current of ~177 µA/µm and the minimum subthreshold swing of 42.6 mV/dec have been attained. The proposed MoS$_2$ FET with the PZT and the HfO$_2$/TiO$_2$/HfO$_2$ tri-layer structure in the gate stack helps increase the limits of transistor dimension scaling and power scaling, and it shows a new insight into the continuous progress of the functionality of electronic devices.

II. DEVICE STRUCTURE

The schematic of the proposed device structure and the equivalent capacitance model is shown in Fig. 1. As depicted in Fig. 1(b), the series combination of the FE capacitor ($C_{FE}$) and a positive capacitor [realized by a dielectric material ($C_{SiO_2}$)] can be visualized from the model. Here, the entire structure below the PZT layer is considered as the baseline 2D MoS$_2$ FET. In the baseline FET structure, an atomically thin monolayer of MoS$_2$ is considered over a SiO$_2$ layer. The thickness and the bandgap of the monolayer MoS$_2$ channel are taken as 6.5 Å$^2$ and 1.8 eV, respectively. A novel tri-layer structure of HfO$_2$/TiO$_2$/HfO$_2$ is proposed as the high-K gate oxide on the MoS$_2$ channel. A similar type of tri-layer structure has recently been experimentally verified for resistive random access memory devices. TiO$_2$ ($e_{TiO_2} \approx 80$) is sandwiched between two layers of HfO$_2$ ($e_{HfO_2} \approx 25$). 1 nm thickness of each HfO$_2$ layer and the sandwiched TiO$_2$ of 6 nm thickness were used in the device structure. The channel length and gate length ($L_G$) are considered as 150 nm and 50 nm, respectively. The device parameters used in the calculations are shown in Table I. The drain and source contact depth is 9 nm, and other structural parameters are shown in Table II. Theoretical calculation recommended that the intrinsic phonon-limited carrier mobility in a single layer of MoS$_2$ is roughly 410 cm$^2$/V s. However, the mobility of monolayer MoS$_2$ may vary under different circumstances. Scaling of the channel length, as well as the use of SiO$_2$ for MoS$_2$ growth and the presence of HfO$_2$ as the device gate oxide, dramatically reduces the mobility of this 2D material. Hence, a mobility of 25 cm$^2$/V s is considered in this work.

TABLE II. Device parameters used for the proposed NCFET.

| Bulk Si doping concentration | Gate oxide thickness | Gate length | SiO$_2$ dielectric constant | Bulk Si thickness | SiO$_2$ thickness | Device width | HfO$_2$ dielectric constant | TiO$_2$ dielectric constant |
|-----------------------------|---------------------|------------|----------------------------|------------------|-----------------|--------------|-----------------------------|-----------------------------|
| $1 \times 10^{25}$/cm$^2$ (p-type) | 8 nm | 50 nm | 3.9 | 40 nm | 10 nm | 1 µm | 25 | 80 |
III. METHODS

2D electrostatics for the MoS$_2$ channel FET and 1-D Landau–Khalatnikov (LK) equations for FE capacitor dynamics are solved self-consistently. In the case of the 2D MoS$_2$ FET, the transfer curve and output characteristics were found by solving the 2D electrostatics of the baseline device in terms of Poisson’s equation, the carrier continuity equation, the drift-diffusion transport model, and the Shockley–Reed–Hall recombination model based on TCAD Silvaco. The charge gathered at the top gate metal of the device is found from the output charge and gate voltages, which can be used in the Landau model in order to simulate the behavior of PZT. Hence, the NC effect of the ferroelectric is verified using the result extracted from MoS$_2$ FET simulation, and the final NCFET simulation is accomplished by combining these two effects.

The dynamics shown by FE capacitors can be explained on the basis of the LK equation. For an FE, the free energy $U(P)$ can be expressed as an even order polynomial of polarization $P$ as follows:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - EP.$$  

(1)

Here, $E = \frac{V_{FE}}{t_{FE}}$, the terms $\alpha$, $\beta$, and $\gamma$ are the anisotropy constants for the FE material (PZT), $E$ is the applied electric field, $t_{FE}$ is the FE thickness, and $V_{FE}$ is the voltage across the FE layer. The FE materials represent inverted parabolic shapes in their energy landscape around the origin. This inverted parabolic shape represents the NC state of the ferroelectrics.\(^{36}\) Setting $P = Q$, the equilibrium state of the FE can be determined by searching the minima of $U$, where we have

$$\frac{dU}{dQ} = 2\alpha t_{FE}Q + 4\beta t_{FE}Q^3 + 6\gamma t_{FE}Q^5 - V_{FE} = 0.$$  

From this,

$$V_{FE} = 2\alpha t_{FE}Q + 4\beta t_{FE}Q^3 + 6\gamma t_{FE}Q^5.$$  

(2)

Due to polarization vs electric field characteristics exhibiting high non-linearity, there is a negative-going slope in the curve, and an “S-shaped” curve is originated. There is a negative-going slope around the origin, which represents the NC state.\(^{37}\) Pb(Zr$_{1-x}$Ti$_x$)O$_3$ with a concentration $x = 0.8$ is considered as the FE in this work, and the values of $\alpha$, $\beta$, and $\gamma$ are provided from the study by Rabe et al.\(^{38}\)

Figure 2(a) represents the energy landscape, and Fig. 2(b) represents the polarization $(P)$ vs electric field $(E)$ characteristics for PZT. The inverted parabolic shape originating from the energy landscape, shown in Fig. 2(a), is a strong sign of the existence of NC within PZT.\(^{39}\) The presence of the NC state is clear from the negative-going slope of the $P$ vs $E$ curve, as shown in Fig. 2(b).\(^{40}\)

The NC state of the material is highly unstable, and stabilizing it while using with MOS devices is a major challenge. Hence, dielectric capacitance has to be chosen in such a way that the series combination provides a stable NC state. Here, we have proposed a novel HfO$_2$/TiO$_2$/HfO$_2$ tri-layer structure as the high-K gate oxide on the 2D MoS$_2$ channel. To stabilize the FE within the NC state, the following criterion must be fulfilled, within the ferroelectric–dielectric heterostructure:

$$|C_{FE}| > C_{MOS}.  

(3)$$

If $C_{MOS}$ is greater than the $C_{FE}$, a hysteretic jump of polarization occurs at the zero crossing that inhibits NC behavior by PZT. In the present case, the total gate capacitance $C_{MOS}$ should be made close to $|C_{FE}|$, which reduces the $SS$ to a comparatively lower value (less than 60 mV/dec). The FE capacitance ($C_{FE}$) can be determined from Eq. (2) and can be written as

$$C_{FE} = \frac{dQ}{dV_{FE}} = \left(2\alpha + 12\beta Q^2 + 30\gamma Q^4\right) \times t_{FE}^{-1}.  

(4)$$

To form a device showing the NC effect, the device has to be designed in such a way that mismatch between $C_{MOS}$ and $C_{FE}$ can be lowered as much as possible.

IV. RESULTS AND DISCUSSION

First, the simulation was performed on the baseline 2D MoS$_2$ FET, considering the standard Shockley–Reed–Hall recombination and the drift-diffusion model as implemented in the ATLAS Silvaco commercial simulator. Figure 3 shows the simulated results for the baseline MoS$_2$ channel FET. In Fig. 3(a), the transfer curve of the 2D MoS$_2$ FET is shown for different drain voltages at the logarithmic scale. The drain voltage varies from a lower value of 10 mV to a value as high as 500 mV. A higher current on/off ratio, as well as a lower value of the subthreshold slope of the device, is demonstrated with the increase in the drain voltage. Drain current can be increased simply by increasing the drain voltage depending on the channel of carrier conduction. Hence, the superior performance of the device with the increase in drain current detects the satisfactory conduction of charge carriers through the MoS$_2$ channel. The average subthreshold slope between the transition from the on-state to the off-state is 66.3 mV/dec. It is obvious that the lowest $SS$ of the device at the transition from the off-state to the on-state can be found at a relatively higher drain voltage level. At $V_{drain} = 500$ mV, the value of the $SS$ was detected as 66.3 mV/dec. A very high $I_{on}/I_{off}$ of about $1 \times 10^{14}$ was found from the simulation. This high value of the on–off current ratio indicates good control of carrier conduction through the MoS$_2$ channel. The obtained high on–off current ratio is six orders higher than that of the previously proposed 2D MoS$_2$ FET\(^{41}\) and outperforms any previous results as well. The saturation current is around 139 $\mu$A/$\mu$m, which is a fair superior result as compared with previous work,\(^{14}\) where the maximum on-current demonstrated was 38 $\mu$A/$\mu$m. Transconductance is an important characteristic of MOS devices, and a large maximum transconductance of 0.1 mS/$\mu$m was obtained from the simulation. This result is about 100 times larger.
than that found in Ref. 20 at the same drain voltage ($V_d = 500$ mV). A minimum threshold voltage ($V_{th}$) of about 0.03 V was obtained from the transfer characteristics. This represents a low threshold voltage, close to zero. Hence, the transistor can be completely switched off below 0.03 V and retains only a very low leakage current of about 10^{-14} pA. Drain voltage dependency shown by the drain current for a gate voltage above the threshold value ($V_g$), as shown in Fig. 3(b), is an indication of the ohmic relationship between these two quantities above $V_{th}$.

Steep switching acts as an important factor in the reduction of power consumption of the device. Steeper switching of the device results in a lower SS. The physical limit of this SS value (which is 60 mV/dec, which comes from the Boltzmann distribution), can be overcome by the use of the NC effect. The significance of the NC effect is that in the NC state, the FE ($C_{FE} < 0$) offsets the positive capacitance of the device so that the resulting gate capacitance, $C_G$, can be made larger than the capacitance of the device, causing SS improvement. 1- This NC effect results in internal amplification of the voltage within a passive network, 0 and hence, amplification begins within the subthreshold region. Improvement in the subthreshold slope results in the improvement of other performance parameters such as $I_{on}/I_{off}$, on-state current, and transconductance.

The FE becomes stabilized in the NC state by being connected in series with a dielectric. The PZT layer is assumed as the FE capacitor integrated into the series with the gate stack of the FET. The gate metal will now act as an intermediate metallic layer in the middle of the ferroelectric, and the gate dielectric and the metallic layer at the top of the FE capacitor will now become the gate metal having a potential $V_G$. The potential across the intermediate metallic layer will become the surface potential ($\psi_s$), which is actually the gate voltage ($V_g$) used for the baseline MoS$_2$ FET simulation. Thus, from the expression of the SS, the derivative $\frac{\partial V_G}{\partial \psi_s}$ can be expressed as

$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}. \quad (5)$$

Here, “$m$” is called the body factor, and the derivative $\frac{\partial V_G}{\partial \psi_s}$ becomes greater than unity if NC exists ($C_{FE} < 0$), making it possible for $\psi_s$ to vary more than the variation of $V_G$ applied externally. Thus, the thin film of the FE material turns into a step-up voltage transformer, a property that sounds impossible in the case of dielectrics. Now, the amplified voltage found is the effect of using the NC phenomenon, and the subthreshold slope can be reduced using this effect.

Figure 4 displays the transfer characteristics of the 2D MoS$_2$ FET with an FE capacitor over the top gate. In the figure, the dotted black line indicates the transfer curve of those of the baseline 2D MoS$_2$ FET without introducing any PZT layer. Hence, it has a minimum saturation (on) current level (139 $\mu$A/μm), as described earlier, for baseline MoS$_2$ FET. The next five solid lines in Fig. 4 indicate the non-hysteretic operation of the 2D MoS$_2$ NCFET, where the thickness of the PZT film is varied from 10 nm to 50 nm. The maximum permissible thickness of PZT is about 50 nm, above which the criteria shown in relation (3) will get violated, and hysteretic operation of the transistor will arise. This hysteretic behavior of the transfer curve in logic device application is quite unwanted and need to be avoided. Moreover, the hysteretic behavior resembles that PZT is unstable within its NC state, and hence, it cannot be efficiently used for the voltage amplification purpose. The other two dashed lines having PZT thicknesses of 55 nm and 60 nm, respectively, represent the hysteretic operation of the FET. This indicates that the hysteresis of PZT has started above 50 nm, and increasing the thickness beyond this value brings a severe hysteretic effect in the device. The use of more than 50 nm thick PZT as the FE capacitor aligned with the top gate of the device results in undesirable degradation in performance. Thus, it is now clear that the PZT layer having 50 nm thickness provides the best improvement before the operation of the device becomes hysteretic.

As shown in Fig. 4(a), a higher on–off current ratio is obtained, which suppresses $I_{on}/I_{off}$ of the baseline MoS$_2$ FET, which was presented earlier. As observed from our simulation results, the usage of the HfO$_2$/TiO$_2$/HfO$_2$ dielectric in the MoS$_2$ channel has extended the current conduction facility of the device to a new stage. Moreover, the addition of the PZT layer is expected to bring the current conduction capacity to a much higher level.
FET) is obtained. The on–off current ratio of the following device is quite large (∼six orders higher) as compared with that of the other related works. Hence, the NC phenomenon lifts $I_{on}$ (about 27% compared with that of the baseline MoS$_2$ FET) as well as improves the SS at the lower current region.

Now, there should also be evidence that the criteria of relation (3) do not get disturbed for a PZT thickness of below 50 nm. This phenomenon is demonstrated in Fig. 5(a). In this figure, the solid lines from 10 nm to 50 nm PZT thickness always satisfies the $|C_{FE}| > C_{MOS}$ condition. On the contrary, the dashed lines having $t_{FE} > 50$ nm create intersections between $C_{FE}$ and $C_{MOS}$, where the $|C_{FE}| < C_{MOS}$ condition is satisfied within a certain region. The dotted black line indicates the capacitance characteristics ($C_{MOS}$) of the 2D MoS$_2$ FET, which is our baseline device. This is clear that 50 nm is the critical thickness above which hysteresis may occur. Another important fact is that the 50 nm PZT thin film produces the lowest body factor ($m$) via capacitance matching, which results in a minimum subthreshold slope by the non-hysteretic operation of the transistor, considering Eq. (5). Without the proper design of the dielectric gate oxide, there is a chance for capacitance mismatch up to a large thickness of the PZT stack. Hence, it is quite undesirable to use the FE material over the top gate of a device in the nanoscale dimension having a FE layer thickness of about three or four times greater than the size of the baseline FET. This requires the FE
capacitance to have a reduced thickness. Different thicknesses of FEs were used in previous studies. This work suggests the use of the maximum PZT thickness of 50 nm for the finest outcome. Moreover, to support the spectacularity of our proposed trilayer high-K dielectric and lower PZT thickness, here, we have also shown the effect of single layer HfO$_2$ on MOS capacitance ($C_{\text{MOS}}$) and FE capacitance ($C_{\text{FE}}$) in terms of Q for different PZT thicknesses, which is depicted in Fig. 5(b). As can be observed from Fig. 5, the finest capacitance matching occurs for the single layer HfO$_2$ NCFET at 100 nm PZT thickness, whereas it is found at 50 nm thickness when the trilayer HfO$_2$/TiO$_2$/HfO$_2$ is introduced.

Figure 6 shows the subthreshold slope characteristics of the device. The results are shown only for the non-hysteretic operation of the transistor. Using the trilayer HfO$_2$/TiO$_2$/HfO$_2$, the minimum subthreshold slope of $\approx 42.6$ mV/dec is obtained at the critical ferroelectric thickness of 50 nm. The SS found from the result is lower than 60 mV/dec, and this is more improved than the previous work on the 2D MoS$_2$ NCFET (57 mV/dec) and equal to that (42.5 mV/dec). Therefore, the accomplishment of reducing the SS value beneath the physics limit was attained by the use of the ferroelectric (PZT) based NC effect. Besides, a comparison of the trilayer HfO$_2$/TiO$_2$/HfO$_2$ and single layer HfO$_2$ structures on drain current...
and the SS has been made. Figures 7(a) and 7(b) show the drain current and SS behaviors of MoS$_2$ NCFET, respectively. As the figures suggest, our proposed HfO$_2$/TiO$_2$/HfO$_2$ trilayer with PZT of 50 nm thickness shows an outstanding result than the single layer HfO$_2$ with a PZT thickness of even more than 50 nm.

Finally, the improvement in transconductance is shown in Fig. 8. Using the trilayer HfO$_2$/TiO$_2$/HfO$_2$, the maximum transconductance of about 1.15 mS/$\mu$m (at $t_{FE} = 50$ nm) is found from the MoS$_2$ NCFET, whereas the MoS$_2$ FET without the NC effect offers a maximum transconductance of $\approx 0.1$ mS/$\mu$m, which signifies a great improvement in the transconductance characteristics using the consequence of NC. This value of maximum transconductance is far improved than the previous work, where a maximum transconductance of 45.5 $\mu$S/$\mu$m was found from the device. Additionally, the comparison of transconductance of the MoS$_2$ NCFET using single layer HfO$_2$ and the trilayer HfO$_2$/TiO$_2$/HfO$_2$ is also demonstrated in Fig. 9. The NCFET using HfO$_2$/TiO$_2$/HfO$_2$ with a PZT thickness of 50 nm provides better performance than the NCFET with HfO$_2$, considering even a larger (e.g., 100 nm) thickness of PZT.

V. CONCLUSION

In conclusion, the usage of 2D materials in the channel has created a massive improvement within the transistor. Introduction of the tri-layer HfO$_2$/TiO$_2$/HfO$_2$ to act as a high-K gate oxide was a novel approach. As an FE material, Pb(Zr$_{1-x}$Ti$_x$)$_3$O$_3$ showed negative capacitance within a certain region of operation. $I_{on}/I_{off}$ was very high for the HfO$_2$/TiO$_2$/HfO$_2$ based MoS$_2$ FET, while the use of 50 nm PZT films has further extended that to a higher value of $3 \times 10^{14}$. A higher transconductance (1.15 mS/$\mu$m) was found from the HfO$_2$/TiO$_2$/HfO$_2$ based MoS$_2$ NCFET, indicating a better current conduction capability. A higher on-current of about 177 $\mu$A/$\mu$m, as well as an improved transfer curve of the device, denotes superior performance. Moreover, the incorporation of the PZT layer in the gate stack reduces the SS to a minimum value of 42.6 mV/dec. Our results have shown tremendous improvement in the current on–off ratio as well as the transconductance value that suppresses all the results found from other works performed until now. These findings yield a new insight into extending the restrictions of scaling the dimension, as well as the power of a transistor,
and manifesting a new path for the continuous progress of the functionality of electronic devices.

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