High Efficiency Common Mode Coupled Inductor Bridgeless Power Factor Correction Converter With Improved Conducted EMI Noise

JU-YOUNG LEE, HYO-SEO JANG, JEONG-IL KANG, AND SANG-KYOO HAN

1Power Electronics System Laboratory, POESLA, College of Creative Engineering, Kookmin University, Seoul 02707, South Korea
2Samsung Electronics Company Ltd., Suwon-si, Gyeonggi-do 16677, South Korea
Corresponding author: Snag-Kyoo Han (djhan@kookmin.ac.kr)

This work was supported in part by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) Grant through the Korea Government (MOTIE) (Development of High Efficiency Power Converter Based on Multidisciplinary Design and Optimization Platform) under Grant 20212020800020, and in part by Samsung Electronics Company Ltd.

ABSTRACT

The conventional power factor correction (CPFC) converter suffers from excessive heat generation due to high conduction loss from the input bridge diode. Various bridgeless PFCs (BPFCs) have been proposed to overcome this drawback. Among them, the conventional BPFC (CBPFC) features the significantly reduced conduction loss but has very poor conducted electromagnetic interference (EMI) noise. Further, the semi-BPFC features the reduced input diode loss and good EMI, but the input diode loss is too significant to ignore. Although another solution, totem-pole BPFC, features high efficiency and good EMI, it usually requires expensive current sensors and microprocessor. A BPFC with the integrated magnetics common mode coupled inductor (ICC) is proposed to overcome the drawbacks of traditional BPFCs. The ICC can significantly reduce the system size by integrating three inductive components into a single magnetic core. Moreover, the small magnetizing current of the ICC, not the main input current, flows through input diodes; thus, experimental results from a 600 W rated prototype prove that the input diode loss can be significantly reduced by about 10 W compared to the CPFC, and the input diode exhibits a low heat generation of 49.8 ° despite the absence of a heat sink. In particular, with the help of input diodes, the EMI noise spectra of the ICC BPFC can meet the EMI standard with a sufficient margin. The detailed analysis, design guide and experimental results from a 600 W rated prototype are provided to confirm the validity of the ICC BPFC.

INDEX TERMS
Power factor correction, bridgeless power factor correction, common mode coupled inductor, integrated magnetics, conducted electromagnetic interference.

I. INTRODUCTION

Line current harmonics generated in a power converter can cause malfunctions in other electronic devices connected to the same grid. Therefore, they are globally limited by international standards such as EN 61000-3-2 [1]. Electronic devices using grid power of over 75 W must employ a power factor correction (PFC) converter to satisfy these standards.

Fig. 1a illustrates the most representative conventional PFC (CPFC) featuring a straightforward structure and a small number of components. Either a live or neutral input line voltage $V_{ac}$ is always connected to the circuit ground through the bridge diode; thus, the CPFC features excellent conducted electromagnetic interference (EMI) noise characteristics [2]. In addition, the inductor current always flows in one direction due to the input bridge diode; therefore, it can be simply and cost-effectively sensed through a shunt resistor placed in the return path. However, the conduction loss of the bridge diode proportional to the output power $P_o$ can cause severe heat generation; thus, thermal management in the CPFC is very difficult. Therefore, numerous parallel-connected input bridge diodes and large heat sinks are required in high power
A. CONVENTIONAL BRIDGELESS POWER FACTOR CORRECTION

The conventional BPFC (CBPFC) in Fig. 1b features significantly reduced conduction loss and high efficiency due to the absence of a bridge diode. However, the absence of a bridge diode can lead to three disadvantages. First, the direction of the inductor current changes every half cycle of $V_{ac}$; thus, sensing the current is impossible through the shunt resistor in the CPFC. Therefore, another complex current sensing circuit is needed [3], [4], [5], [6]. Section II-C presents various current sensing methods for BPFCs, along with the proposed circuit in detail.

Second, the zero current detection (ZCD) circuit for the operation in critical conduction mode (CrM) is complex in the CBPFC. The CrM is advantageous for the switching loss and reverse recovery characteristics of the output diode. Various ZCD circuits for BPFCs and the proposed circuit are presented in detail in Section II-D.

Third, during the negative half cycle of $V_{ac}$, the voltage at the neutral line of $V_{ac}$ in Fig. 1b changes rapidly between the circuit ground and $V_o$ depending on the switching frequency, which can significantly deteriorate the conducted EMI noise characteristics. Thus, many difficulties occur in the practical application of the CBPFC.

B. SEMI-BRIDGELESS POWER FACTOR CORRECTION

The semi-BPFC (SBPFC) in Fig. 1c can improve the poor EMI noise characteristics of the CBPFC. One of the two input diodes $D_{acp}$ and $D_{acn}$ conducts according to the polarity of $V_{ac}$, and either a live or neutral line of $V_{ac}$ is always connected to the circuit ground. Therefore, the SBPFC has the advantage of good conducted EMI characteristics like the CPFC [2]. However, the inductor current always flows through one of two input diodes during the entire cycle of $V_{ac}$; thus, the conduction loss can be halved compared to the CPFC but is too large to ignore.

Moreover, two additional disadvantages exist compared to the CPFC. First, two inductors are required, and operate alternately according to the polarity of $V_{ac}$, reducing their utilization by half. In addition, an auxiliary ZCD winding for CrM operation is required for each inductor [7]. Second, as mentioned the two inductors operate alternately depending on the polarity of $V_{ac}$. Therefore, the main current proportional to the load flows through one active inductor, and the circulating current flows through the other inactive inductor. However, the circulating current cannot be specified or predicted due to various parasitic components of the field effect transistor (FET), diode, line impedance, and others. At this time, the return current $i_{rt}$ in Fig. 1c, which corresponds to the difference between the main current and circulating current, cannot represent the input current. As a result, the current
sensing through the shunt resistor placed in the return path is not possible. Therefore, another complex and expensive current sensing method is required to obtain input current information [3], [8].

C. TOTEM-POLE BRIDGELESS POWER FACTOR CORRECTION

Fig. 1d depicts the totem-pole BPFC (TBPFC) recently widely applied to high-power applications of over 1 kW. The TBPFC has no bridge diode like the CBPFC, therefore, it also features low conduction loss and good heat generation. In addition, the neutral line of $V_{ac}$ in Fig. 1d is always connected to the circuit ground or $V_o$ alternately every half cycle of $V_{ac}$. Thus, the TBPFC has the advantage of good conducted EMI characteristics.

However, a digital microprocessor is usually instead of an analog PFC integrated circuit (IC) because of its complex driving algorithm. For example, when $V_{ac}$ changes from a negative to a positive half cycle, the slow input diode $D_{o2}$ is still conducting due to reverse recovery characteristics. Thus, the $V_o$ applied to the inductor induces a large current spike during the first switching transient [6]. This problem can be more severe when using synchronous FETs to reduce conduction loss instead of $D_{o1}$ and $D_{o2}$. Therefore, the soft-start function is essential at the zero crossing of $V_{ac}$, which can be implemented by the microprocessor [9], [10]. Moreover, the TBPFC has other drawbacks, such as a complex and expensive current sensing circuit, an additional gate driver for the high side FET, and a complex ZCD circuit for CrM operation. Therefore, the TBPFC is a somewhat expensive and complex solution for low to medium power applications due to these disadvantages, making it suitable for high-power applications.

This paper proposes a new BPFC with a common mode coupled (CMC) inductor to overcome the disadvantages of traditional PFCs. In addition, the integrated magnetic common mode coupled inductor (ICC) for the proposed BPFC is also proposed to integrate three inductors, including the CMC inductor, into a single magnetic core.

The concept of the proposed ICC BPFC is briefly described in the next section. Then, the detailed analysis of the proposed ICC BPFC according to the operation of the ICC is presented. Finally, the proposed ICC BPFC is validated through the experimental results from a 600 W rated prototype.

II. ANALYSIS OF THE PROPOSED ICC BPFC

A. CONCEPT OF THE PROPOSED ICC BPFC

The CPFC has advantages, such as the small number of components and good EMI noise characteristics, but has inherent problems such as excessive heat generation due to high conduction loss of the bridge diode. Various BPFCs have been proposed to solve these problems. Among them, the CBPFC has low conduction loss but poor EMI noise characteristics. Nevertheless, the SBPFC has good EMI noise characteristics but high conduction loss of the input diode.

The proposed ICC BPFC employs a CMC inductor and input diode as displayed in Fig. 2, to improve both the conduction loss and EMI noise characteristics. Assuming that the CMC inductor is ideal with $L_{cm} = \infty$, it can make $i_1$ and $i_2$ exactly equal through the common mode operation. Practically, finite $L_{cm}$ makes $i_1$ larger than $i_2$ by $h_{cm}$ during the positive half cycle and makes $i_2$ larger than $i_1$ by $h_{cm}$ during the negative half cycle. In addition, if $L_{cm}$ is designed to be large, a small $h_{cm}$ can be obtained. Therefore, unlike traditional PFC converters, a small $h_{cm}$ corresponding to the difference between $i_1$ and $i_2$ flows through the input diode of the ICC BPFC, which can minimize the conduction loss of the input diode and consequent heat generation. In addition, a small $h_{cm}$ flows through one of the two input diodes $D_{acp}$ and $D_{acm}$ according to the polarity of $V_{ac}$. Thus, either a live or neutral line of $V_{ac}$ is always connected to the circuit ground. Therefore, the proposed circuit suppresses the conducted EMI noise in the same way as the CPFC and SBPFC featuring good conducted EMI characteristics. As a result, the proposed circuit shows conducted EMI characteristics similar to the CPFC and SBPFC and has superior EMI characteristics to the CBPFC [11].

Moreover, as illustrated in Fig. 2, the ICC BPFC requires three inductive components: one CMC inductor and two input inductors. The proposed ICC can integrate three inductive components into a single magnetic core to improve the power density by reducing the number of inductors, as presented in Fig. 3. In addition, the magnetizing and leakage inductance of the ICC can be freely adjusted. Fig. 4 shows the concept of adjusting the leakage inductor $L_k$ in the ICC. As shown in Fig. 4a, since the reluctance of the center leg is large due to the large air gap of the center leg, most of the magnetic flux generated in the primary outer leg flows to the secondary outer leg. Therefore, $L_k$ becomes small. On the other hand, as shown in Fig. 4b, since the air gap of the center leg is small, a significant portion of the magnetic flux generated in the primary outer leg flows to the center leg, and thus the magnetic flux flowing to the secondary outer leg decreases. As a result, $L_k$ becomes large. That is, $L_k$ can be freely adjusted according to the size of the air gap in the center leg.

The gate signal of the proposed circuit can be driven in two ways. The first method is to simultaneously apply gate
signals of the same pulse width to \( M_1 \) and \( M_2 \) regardless of the polarity of input voltage. The operation of the proposed circuit will be explained in detail in section II-B mode analysis. When \( M_2 \) is off in the positive half cycle, the body diode of \( M_2 \) conducts and conduction loss occurs due to the forward voltage drop. In addition, since the proposed circuit operates symmetrically according to the polarity of the input voltage, the body diode of \( M_1 \) conducts when \( M_1 \) is off during negative half cycle. Since the same gate signal is applied to both FETs regardless of the polarity of the input voltage, the gate driver circuit is as simple as the CPFC. The second method is to always turn on one of the two FETs depending on the input voltage polarity. During the positive half cycle, \( M_2 \) is always on, and during the negative half cycle, \( M_1 \) is always on. Therefore, the second method has an advantage over the first method in terms of conduction loss because the body diode does not conduct. However, in order to apply different gate signals to \( M_1 \) and \( M_2 \) according to the polarity of the input voltage, an additional circuit including the input voltage sensing circuit is required. In this paper, the first method is applied to the prototype of the proposed circuit due to its simplicity and ease of implementation. That is, a general purpose PFC integrated controller (IC) is employed and the gate signal of the IC is simultaneously applied to both FETs. In addition, other advantages of the proposed ICC BPFC are as follows:

- Input current sensing with a shunt resistor is possible.
- Only one ZCD winding for the CrM operation is needed.
- A floating gate driver is not required.
- General purpose PFC ICs can be used instead of an expensive digital microprocessor.
- The current of the input diode can be reduced as desired.

The detailed analysis, implementation method, and design guide of the proposed ICC BPFC are presented below.

B. MODE ANALYSIS OF THE PROPOSED ICC BPFC

The operation of the proposed circuit is exactly symmetrical with respect to the positive and negative half cycles of \( V_{ac} \). Therefore, the mode analysis is presented only for the positive half cycle. The following assumptions are made to explain the steady state operation of the proposed circuit:

- Input inductors \( L_{k1} \) and \( L_{k2} \) are equal to \( L_k \), and the magnetizing inductance \( L_{cm} \) is very large compared to \( L_k \).
- All other components except those illustrated in the circuit are ideal.
- The output capacitor is large enough to be considered a constant voltage source \( V_o \).
- The gate signals of \( M_1 \) and \( M_2 \) have the same pulse width and are turned on/off simultaneously.
- The shunt resistor \( R_{sen} \) is ignored because it has little effect on the overall circuit operation.
- The turn ratio of the primary and secondary windings of the CMC inductor is \( N_p/N_s = 1:1 \).
- The proposed ICC BPFC operates in CrM.

Mode 1 \([t_1 \sim t_2]\): When \( M_1 \) and \( M_2 \) are on, \( D_{acr} \) is off and \( D_{acp} \) is on by \( V_{ac} \), as displayed in Fig. 5a. Therefore, \( V_{ac} \) is applied to the equivalent inductor \( L_{eff} \) comprising a CMC inductor and input inductors, as presented in Fig. 3b, and the input current \( i_1 \) increases linearly as follows:

\[
i_1(t) = \frac{V_{ac}}{L_{eff}} (t - t_1) . \tag{1}
\]

At this time, because \( M_2 \) and \( D_{acr} \) are on and the turn ratio of the CMC inductor is 1:1, the equivalent inductor \( L_{eff} \) between nodes ① and ④ is equal to the sum of \( L_{cm} || L_{k2} \) and
Fig. 5 reveals that the input diode current \( i \) positive half cycle (a) Mode 1: M1 and M2 are turned on during the positive half cycle, (b) Mode 2: M1 and M2 are turned off during the positive half cycle.

**FIGURE 5.** Operational mode of the proposed ICC BPFC during the positive half cycle (a) Mode 1: M1 and M2 are turned on during the positive half cycle, (b) Mode 2: M1 and M2 are turned off during the positive half cycle.

From the operations in Modes 1 and 2, \( L_{k1} \) as follows:

\[
L_{eff} = \frac{L_{cm}||L_{k2} + L_{k1}}{L_{cm} + L_k} = \frac{L_k(2L_{cm} + L_k)}{L_{cm} + L_k}. \tag{2}
\]

As \( V_{ac} \) is divided by \( L_{cm}||L_{k2} \) and \( L_{k1} \), as illustrated in Fig. 5a, \( V_{Lcm}, V_{Lk2}, \) and \( V_{Lk1} \) are obtained as follows:

\[
V_{Lcm} = V_{Lk2} = \frac{L_{cm}||L_{k2}}{L_{cm} + L_k} V_{ac} = \frac{L_{cm}}{2L_{cm} + L_k} V_{ac},
\]

\[
V_{Lk1} = \frac{L_{k1}}{L_{cm}||L_{k2} + L_{k1}} V_{ac} = \frac{L_{cm} + L_k}{2L_{cm} + L_k} V_{ac}. \tag{4}
\]

Additionally, because \( i_1 \) is divided by \( L_{cm} \) and \( L_{k2} \), \( i_{Lcm} \) and \( i_2 \) are calculated as follows:

\[
i_{Lcm} (t) = \frac{L_{k2}}{L_{k2} + L_{cm}} i_1 (t) = \frac{L_k}{L_k + L_{cm}} i_1 (t), \tag{5}
\]

\[
i_2 (t) = \frac{L_{cm}}{L_{k2} + L_{cm}} i_1 (t) = \frac{L_{cm}}{L_k + L_{cm}} i_1 (t). \tag{6}
\]

Applying Kirchhoff’s current law to Nodes A and B in Fig. 5a reveals that the input diode current \( i_{acp} \) is equal to \( i_{Lcm} \), as follows:

\[
i_{Lcm} (t) = i_1 (t) - i_2 (t) = i_{acp} (t). \tag{7}
\]

Therefore, the input diode current of the proposed circuit is much smaller than the main input current \( i_1 \) by first assumption and (5), so the conduction loss of the input diode can be significantly reduced compared to the CPFC and SBPFC.

Mode 2 \([t_2 \sim t_3]\): When \( M_1 \) and \( M_2 \) are off, as depicted in Fig. 5b, \( i_1 \) flows to the output side through \( D_{o1} \) and decreases linearly, as follows:

\[
i_1 (t) = -\frac{V_o - V_{ac}}{L_{eff}} (t - t_2) + i_1 (t_2). \tag{8}
\]

Because \( i_1 \) is divided by \( L_{cm} \) and \( L_{k2} \), as in Mode 1, \( i_{Lcm} \) and \( i_{acp} \) are equal to (5) and (7), respectively. In addition, \( V_{ac} - V_o \) is divided by \( L_{cm}||L_{k2} \) and \( L_{k1} \), as presented in Fig. 5b; thus, \( V_{Lcm}, V_{Lk2}, \) and \( V_{Lk1} \) are obtained as follows:

\[
V_{Lcm} = V_{Lk2} = \frac{L_{cm}}{2L_{cm} + L_k} (V_{ac} - V_o), \tag{9}
\]

\[
V_{Lk1} = \frac{L_{cm} + L_k}{2L_{cm} + L_k} (V_{ac} - V_o). \tag{10}
\]

Fig. 6 illustrates the operational mode during the negative half cycle, and the operation is exactly symmetrical with the positive half cycle.

From the operations in Modes 1 and 2, \( i_{Lcm} \) continues to flow through \( D_{acp} \) during the positive half cycle of \( V_{ac} \). In addition, the symmetrical operation indicates that \( i_{Lcm} \) continues to flow through \( D_{acp} \) during the negative half cycle of \( V_{ac} \). Thus, during the entire cycle of \( V_{ac} \), either a live or neutral line of \( V_{ac} \) is always connected to the circuit ground.
through $D_{acp}$ or $D_{acn}$, so low conducted EMI noise characteristics can be expected.

C. CURRENT SENSING METHOD

For the CPFC in Fig. 1a, the inductor current always flows in one direction regardless of the polarity of $V_{ac}$ due to the bridge diode. Moreover, one node of the current sensing resistor is connected to the circuit ground. Thus, it is easy to transfer the current information to the PFC IC. Therefore, the inductor current in the CPFC can be simply and cost-effectively sensed through only a shunt resistor placed in the return path [3], [4].

However, because the CBPFC and TBPFC do not have a bridge diode, as depicted in Figs. 1b and 1d, the direction of the inductor current changes every half cycle of $V_{ac}$. In addition, it is very difficult to sense the inductor current through the shunt resistor. Furthermore, for the SBPFC in Fig. 1c, the return current $i_{rt}$ corresponding to the difference between the main current and circulating current cannot represent the input current as described in Section I-B. Thus, current sensing through the shunt resistor placed in the return path is not possible [6], [8], [12].

Therefore, three representative current sensing methods for traditional BPFCS have been proposed as follows [5].

First, because hall-effect sensors are electrically isolated and can sense the dc, they can be used to sense the inductor current floating from the circuit ground, as presented in Fig. 1b. This method is simple and accurate, but the hall-effect sensor is expensive. Therefore, it is not suitable for low to medium power applications where the price is important.

Second, current transformers (CTs) can also sense the current floating from the circuit ground. Although CTs have a reasonable price, high bandwidth, and low power loss, they cannot sense the dc due to the nature of the transformer. Therefore, as displayed in Fig. 1c, CTs should be placed in series with each FET, and sensed signals should be summed through diodes.

Third, differential mode amplifiers are also widely used to sense the current. This method first senses the current through a small shunt resistor and then amplifies the sensed signal with the differential mode amplifier. The differential mode amplifier senses the inductor current floating from the ground but is sensitive to noise. In addition, its bandwidth is low, making it difficult to sense the instantaneous current for peak current mode control.

Consequently, all three methods are more complex and expensive than the current-sensing method using only a shunt resistor.

However, in the proposed ICC BPFC, current sensing is possible through only a shunt resistor. The return current $i_{rt}$ equals $i_{Lcm}$, corresponding to the difference between $i_1$ and $i_2$, as illustrated in Figs. 4 and 5. Moreover, (5) indicates that $i_{Lcm}$ is proportional to the main inductor current $i_1$ during the positive half cycle and the main inductor current $i_2$ during the negative half cycle. Therefore, the main inductor current in the proposed ICC BPFC can be simply and cost-effectively sensed by sensing $i_{rt}$ proportional to the main inductor current through only a shunt resistor placed in the return path. In addition, the return current $i_{rt} = i_{Lcm}$, which is much smaller than the main inductor current, flows through the shunt resistor. Therefore, the loss of the sensing resistor can be significantly reduced compared with the CPFC, enabling the use of a low-power resistor. The detailed loss analysis of the ICC BPFC, including the shunt resistor is presented in Section III.

D. ZERO CURRENT DETECTION METHOD

The CrM operation is advantageous in improving the switching loss of the FET and the reverse recovery characteristics of the output diode by operating the converter at the boundary between the continuous and discontinuous conduction modes. To drive PFC in the CrM, the ZCD circuit to detect the zero current point of the input inductor is essential.

The most common method for the ZCD is to use an auxiliary winding coupled to the input inductor. Figs. 1 and 7 illustrate the ZCD blocks of traditional PFC converters and the typical detailed ZCD circuits for various CrM PFCs, respectively [13], [14]. Fig. 8a reveals that the CPFC requires only one auxiliary winding coupled to the input inductor. Moreover, as the inductor current $i_{lin}$ flows in one direction due to the bridge diode, the ZCD signal $V_{aux}$ from the auxiliary winding is unipolar, as depicted in Fig. 9a. Therefore, the zero current of the input inductor can be easily detected at every falling edge of $V_{aux}$ regardless of the polarity of $V_{ac}$. However, because the inductor currents of the CBPFC and

![Figure 7. Theoretical waveforms of the proposed ICC BPFC during the positive half cycle.](image-url)
TBPFC flow in both directions according to the polarity of $V_{ac}$, as indicated in Fig. 9b, two auxiliary windings coupled to the input inductor are required. Moreover, the ZCD signal $V_{aux}$ from the auxiliary winding is bipolar; thus, additional circuits making $V_{aux}$ unipolar are required (Fig. 8b). Moreover, the SBPFC has two input inductors, and each inductor operates alternately every half cycle of $V_{ac}$ (Fig. 9c). Therefore, an auxiliary winding coupled to each of the two input inductors is required, and ZCD signals $V_{aux, L1}$ and $V_{aux, L2}$ from each auxiliary winding should be ORed through additional circuits (Fig. 8c).

Nevertheless, the proposed ICC BPFC has equivalent circuits (Fig. 10) when $M_1$ and $M_2$ are on. As illustrated in this figure, $V_{Lcm}$ across the CMC inductor is independent of the polarity of $V_{ac}$ as follows:

$$V_{Lcm} = \frac{L_{cm}}{2L_{cm} + L_k} |V_{ac}|. \quad (11)$$

When $M_1$ and $M_2$ are off, equivalent circuits in Fig. 11 indicate that $V_{Lcm}$ is independent of the polarity of $V_{ac}$, as follows:

$$V_{Lcm} = \frac{L_{cm}}{2L_{cm} + L_k} (|V_{ac}| - V_o). \quad (12)$$

Therefore, as $V_{Lcm}$ has the same waveform regardless of $V_{ac}$, the ZCD through only one auxiliary winding coupled to the CMC inductor is possible (Fig. 8d). Moreover, the ZCD signal $V_{aux, CM}$ from the auxiliary winding is unipolar.
(Fig. 9d); thus, the zero current of the input inductor can be easily detected at every falling edge of $V_{\text{aux,CM}}$ regardless of the polarity of $V_{\text{ac}}$.

### E. DESIGN GUIDE OF THE ICC

Fig. 3 reveals that each leg of the proposed ICC is defined as $\text{Leg}_1$, $\text{Leg}_2$, and $\text{Leg}_c$, the paths of magnetic fluxes $\phi_1$, $\phi_2$, and $\phi_c$, respectively. The relationship between the inductance model in Fig. 3b and the reluctance model in Fig. 12 should be derived to obtain the maximum magnetic flux density $B_{\text{max}}$ of each leg. Then, the $B_{\text{max}}$ of each leg can be obtained in the form of (13) by substituting the current equations of the ICC into the relationship between the inductance and reluctance models, and is determined at the maximum current:

$$B_{\text{max}} = \frac{L \cdot i_{\text{L, max}}}{A_e \cdot N},$$  \hspace{1cm} (13)

where $L$ is the magnetizing inductance of the inductor, $i_{\text{L, max}}$ is the maximum current of the inductor, $A_e$ is the effective area of the core, and $N$ is the number of turns in the inductor.

Fig. 13 presents currents $i_1$, $i_2$, and $i_{\text{Lcm}}$ of the ICC BPFC operating in the CrM during the positive half cycle, where $i_1$, $i_2$, and $i_{\text{Lcm}}$ indicate the maximum values of $i_1$, $i_2$, and $i_{\text{Lcm}}$, respectively. As the operation of the ICC BPFC during the negative half cycle is symmetrical with the positive half cycle, only the positive half cycle is treated for the convenience of analysis.

If it is assumed that the overall system efficiency is 100%, the maximum current $I_1$ is calculated from the input and output specifications as follows:

$$I_1 = 2\sqrt{2} \frac{P_o}{V_{\text{ac(min)}}},$$  \hspace{1cm} (14)

where $P_o$ is the maximum output power and $V_{\text{ac(min)}}$ is the minimum voltage specified in Table 1.

The equivalent inductance and reluctance between terminals ①-④ with terminals ②-③ open are obtained to derive the relationship between the inductance model in Fig. 3b and the
obtained as follow:

\[ L = \frac{N^2}{\mathcal{R}_o + 2\mathcal{R}_c}. \]

The relationship between inductance and reluctance is equal to (17); thus, (18) is obtained from (15)–(17) [15]:

\[ L = \frac{N^2}{\mathcal{R}_o + 2\mathcal{R}_c}. \]

Moreover, from (18) and (21), \( L_{cm} \) can be determined as follows:

\[ L_{cm} = N^2 \frac{\mathcal{R}_o + \mathcal{R}_c}{\mathcal{R}_o + 2\mathcal{R}_c}. \]

The magnetic flux flowing through each leg can be obtained by deriving the magnetomotive force (MMF) applied to \( \mathcal{R}_c \) in Fig. 12. MMF \( N I_2 \) by the secondary winding is derived as (23) from (6), and (23) is expressed as (24) by substituting (21) and (22) into (23).

\[ N I_2 = N \frac{L_{cm}}{L_k + L_{cm} + I_1}, \]

\[ N I_2 = N \frac{\mathcal{R}_c}{\mathcal{R}_o + \mathcal{R}_c} I_1. \]

If kirchhoff’s current law is applied to node R in Fig. 12, the relationship as shown in (25) is satisfied. Therefore, \( F_{\mathcal{R}e} \) can be expressed as (26).

\[ \frac{F_{\mathcal{R}e} - NI_1}{\mathcal{R}_o} + \frac{F_{\mathcal{R}e} - N \frac{\mathcal{R}_c}{\mathcal{R}_o + \mathcal{R}_c} I_1}{\mathcal{R}_o} = 0, \]

\[ F_{\mathcal{R}e} = N \frac{\mathcal{R}_c}{\mathcal{R}_o + \mathcal{R}_c} I_1. \]

Since (24) and (26) are the same, the MMF applied to the reluctance \( \mathcal{R}_o \) of Leg2 is 0 and \( F_2 \) is 0. Therefore, \( \Phi_1 \) and \( \Phi_2 \) are as follows:

\[ \Phi_2 = \frac{NI_2 - F_{\mathcal{R}e}}{\mathcal{R}_o} = 0, \]

\[ \Phi_1 = \frac{NI_1 - F_{\mathcal{R}e}}{\mathcal{R}_o} = \frac{1}{\mathcal{R}_o + \mathcal{R}_c} NI_1. \]

As the operation of the ICC BPFC during the negative half cycle is exactly symmetrical to the positive half cycle, the roles of \( i_1 \) and \( i_2 \) are reversed during the negative half cycle. That is, \( \Phi_1 \) becomes 0, and \( \Phi_2 \) and \( \Phi_2 \) have the same relationship as (28) and (29).

From these results, the magnetic flux of the ICC becomes zero in one of the two outer legs according to the polarity of \( V_{ac} \), and the same magnetic flux flows through the other outer and center legs. Therefore, as all legs of the ICC have the same maximum magnetic flux, their magnetic cores must be designed to have the same cross-sectional area \( A_c \). If (21) and (22) rearranged for \( \mathcal{R}_c \) and \( \mathcal{R}_o \) are substituted into (28) and (29) and expressed in the form of (13), the maximum magnetic flux density of each leg is as follows:

\[ B_2 = 0, \]

\[ B_{1(max)} = B_{c(max)} = \frac{I_1 L_k}{A_c N} \left( 1 + \frac{L_{cm} + L_k}{L_{cm} + L_k + I_1} \right) = \frac{I_{1\text{eff}}}{A_c N}. \]

The saturation magnetic flux density \( B_{sat} \) is determined according to the material of the core. If the maximum magnetic flux density \( B_{max} \) (31) approaches \( B_{sat} \) and the magnetic flux change has non-linearity, the core is saturated. In order to prevent this, \( B_{max} \) should not exceed a specific magnetic flux density. Therefore, by referring to the datasheet of the core, the \( A_c \) and \( N \) and \( L_{eff} \) should be chosen to have an appropriate \( B_{max} \) less than \( B_{sat} \). For the ferrite GP95 material applied to the proposed circuit, the saturation level of the magnetic flux is 460 mT. Therefore, \( B_{max} \) can be selected as 370 mT considering a margin of 20%. Fig. 14 shows the relationship between \( L_{eff} \), \( A_c \) and \( N \) to ensure \( B_{max} = 0.37 \) mT, which is based on (31) under the worst-case conditions of \( V_{ac} = 90 \) Vrms, \( V_o = 400 \) V, and \( P_o = 600 \) W. From these results, \( N = 20, L_{eff} = 70 \) \( \mu \)H and \( A_c = 180 \) mm\(^2\) are chosen for the proposed prototype.

Fig. 15 illustrates the magnetic flux density waveform in each leg during the entire period of \( V_{ac} \).
The inductance ratio $L_R$ and relationship between reluctance and core geometry are defined as follows:

$$L_R = \frac{L_{cm}}{l_k}, \quad (32)$$

$$R = \frac{l_g}{\mu_0 A_e}, \quad (33)$$

where $l_g$ is air gap length, and $\mu_0$ is the permeability of free space.

Therefore, from (21), (22), and (33), the equivalent inductance $L_{eff}$ and $L_R$ can be expressed as follows:

$$L_{eff} = \frac{N^2}{R_{o} + R_{c}} = \frac{\mu_0 A_e N^2}{l_o + l_c}, \quad (34)$$

where $l_o$ ($l_c$) is the air gap length of the outer (center) leg.

$$L_R = \frac{R_{c}}{R_{o}} = \frac{l_c}{l_o}. \quad (35)$$

From these results, if the magnetic core and number of turns in the ICC inductor are predetermined, $L_{eff}$ is determined by $l_o + l_c$, the sum of the air gaps, and $L_R$ is determined by $l_o/l_c$, the ratio of the air gaps. Fig. 16 presents an example of the ICC inductor designed according to the prototype specifications.

### III. OPTIMAL DESIGN CONSIDERING THE HEAT GENERATION OF THE INPUT DIODE

The operation of the proposed ICC BPFC is completely symmetric with respect to the polarity of $V_{ac}$; thus, the optimal design is carried out only for the positive half cycle. The design specifications are $V_{ac} = 90–264 V_{rms}$, $V_o = 400 V$, and $P_o = 600 W$, and the details are listed in Table 1 in Section IV.

One of the best features of the proposed ICC BPFC is that the input diode current equal to $i_{cm}$ can be adjusted by $L_{cm}$ and $L_k$, as in (5). In addition, $I_2$ is adjusted by $L_{cm}$ and $L_k$, as in (6). Fig. 17 indicates a normalized $I_{cm}$ and $I_2$ according to the inductance ratio $L_R$. As presented in this figure, $I_{cm}$ and $I_2$ approach $I_1$ and 0 A as $L_R$ decreases, respectively, which means that the proposed ICC BPFC with a large $L_R$ tends to behave similarly to the SBPFC. In contrast, as $L_R$ increases, $I_{cm}$ and $I_2$ approach 0 A and $I_1$, respectively. Thus, the proposed ICC BPFC with a small $L_R$ tends to behave similarly to the CBPFC.

Based on $L_{eff} = 70 \, \mu H$ designed under the worst case conditions of $V_{ac} = 90 V_{rms}$ and $P_o = 600 W$, the loss values of the main components and the total according to $L_R$ are analyzed (Fig. 18). A large $L_R$ makes $i_{cm}$ small; thus, the input diode loss $P_{Dac}$ and shunt resistor loss $P_{Resen}$ decrease, but the conduction loss of $M_2$ $P_{M2 \, \text{cond}}$ and the ICC loss $P_{IM}$ increase. Therefore, in Fig. 18, the large $L_R$ decreases the total loss, but increases the losses of the FET and ICC. Thus, the heat generations of the FET and ICC may become higher than that of the input diode with a small loss. An imbalance may occur in heat generation among circuit elements, according to $L_R$. Therefore, although the total losses increase slightly, designing the converter so that $L_R$ is not too large is desirable for evenly distributed heat generation throughout the entire circuit.

Fig. 19 illustrates an optimal design flowchart for balancing the heat generation throughout the entire circuit while minimizing the total loss. As indicated in this flowchart, the ICC BPFC is designed to minimize the total loss by increasing the dissipation of the input diode up to a maximum allowable level in the system while reducing losses in the FET and ICC. The values of $\Delta T_{Dac}$ and $\Delta T_{Dac \, \text{spec}}$ indicate...
FIGURE 18. Loss values of the main components according to $L_R$ at $V_{ac} = 90$ Vrms and $P_o = 600$ W: (a) loss breakdown, (b) total loss.

FIGURE 19. Optimal design flowchart considering the thermal balance.

The temperature rise in $D_{ac}$ and the allowable temperature rise compared to the ambient temperature, respectively. The value of $\alpha$ is the designer’s choice constant, which is greater than 0 and less than 1. As $\alpha$ approaches 1, $\Delta T_{Dac}$ approaches $\Delta T_{Dac, spec}$. To increase the power density of the ICC BPFC, $L_R$ should be designed so that $\alpha$ is as close to 1 as possible without a heat sink for input diode $D_{ac}$.

A small $i_{Lcm}$ flows through the input diode; thus, a low cost two-lead type diode with a low current capacity can be used as the input diode. For example, the STTH5L06 (DO-201AD, 600 V, 5 A) manufactured by the STMicroelectronics company has a thermal resistance $R_{th}$ of 75 $^\circ$C/W (junction to ambient). Therefore, if the loss of STTH5L06 employed as the input diode is about 0.5 W, $\Delta T_{Dac}$ of the diode can be maintained at 40 $^\circ$C without a heat sink.

As presented in Fig. 19, $L_{eff}$ and $L_R$ should be designed to maximize the overall efficiency of the ICC BPFC by considering the losses of major elements, such as the ICC, switches, output diodes, output capacitor, current sensing resistor, and input diodes [16], [17]. Thus, Fig. 20 reveals that the ICC BPFC has a maximum efficiency of $L_{eff} = 70$ $\mu$H and $L_R = 30$. However, in Fig. 18b, the difference between the total losses at $L_R = 4$ and $L_R = 30$ is as low as 0.4 W. Moreover, if STTH5L06 is used as the input diode, $L_R = 4.4$ can make the loss of $D_{acp}$ or $D_{acn}$ about 0.5 W, and $\Delta T_{Dac}$ is expected to be about 40 $^\circ$C without a heat sink. Thus, to achieve reasonable loss and heat generation values of the ICC, FET, and input diode with no heat sink, it is appropriate to select $L_R$ as 4.4 rather than 30. Consequently, based on $L_{eff} = 70$ $\mu$H and $L_R = 4.4$, $L_{cm} = 170$ $\mu$H and $L_k = 39$ $\mu$H can be obtained from (2) and (32).

Fig. 16 demonstrates the ICC geometry suitable for prototype specifications in Table 1 of Section IV. As mentioned, the magnetic cores of the outer and center legs have the same cross-sectional area [18]. From (30), the maximum flux density of this the ICC is calculated as 0.367 T under the worst case conditions of $V_{ac} = 90$ Vrms and $P_o = 600$ W.

For a more accurate comparison between the proposed ICC BPFC and CPFC, the inductor of the CPFC is designed using a magnetic core with the area product $A_p$, similar to that of the ICC core, where $A_p$ of the ICC core is about 5.36 cm$^4$. To implement the 600 W rated PFC, EER4445S ($A_p = 5.27$ cm$^4$) was selected for the CPFC inductor core, most similar to the ICC. Except for the input diode and inductor, all components are identical for a fair comparison.

FIGURE 20. Overall efficiency of the proposed ICC BPFC according to $L_R$ and $L_{eff}$ at $V_{ac} = 90$ Vrms, $P_o = 600$ W.
inductance according to the number of turns $N$ at reveals that the maximum efficiency of 96.04% is obtained cross-sectional area within a given window area. This figure and (5). Therefore, path of the CPFC or ICC PFC, and the return current through temperatures of components are presented in Section IV. to the CPFC. Details about the heat sink size and measured cost of the ICC BPFC can be significantly reduced compared larger or similar to that of the CPFC. Hence, the size and of the ICC BPFC for the switch and output diode is slightly than that of the CPFC by about 3.6 W. Thus, the heat sink losses of the ICC BPFC are about 6.7 W but are slightly larger a bulky heat sink to dissipate the large loss of about 10 W, whereas the total switch loss is slightly increased by about 3.6 W. Therefore, the input bridge diode of the CPFC requires a bulky heat sink to dissipate the large loss of about 10 W, but the proposed ICC BPFC can eliminate the heat sink for the input diode. In addition, the total switch and output diode losses of the ICC BPFC are about 6.7 W but are slightly larger than that of the CPFC by about 3.6 W. Thus, the heat sink of the ICC BPFC for the switch and output diode is slightly larger or similar to that of the CPFC. Hence, the size and cost of the ICC BPFC can be significantly reduced compared to the CPFC. Details about the heat sink size and measured temperatures of components are presented in Section IV.

The current sensing resistor $R_{sen}$ is placed in the return path of the CPFC or ICC PFC, and the return current through $R_{sen}$ is equal to $i_{Lcm}$ and can be expressed as (36) from (32) and (5). Therefore, $R_{sen}$ can be chosen from (37) considering the current sensing gain and maximum level of the sensed current signal:

$$i_{Lcm} = i_1 \frac{1}{L_R + 1}, \quad (36)$$

$$R_{sen} = \frac{V_{cs}}{A_1 \cdot i_{Lcm}} = \frac{V_{cs}}{A_1 \cdot i_1} (L_R + 1), \quad (37)$$

where $A_1$ is the current sensing gain, and $V_{cs}$ is the maximum level of the sensed current signal applicable to the PFC IC.

As all of the input inductor current $i_1$ of the CPFC flows through $R_{sen}$, the $R_{sen}$ loss is equal to $i_1^2 R_{sen}$. In contrast, the ICC PFC has a non-zero $L_2$; thus, the return current $i_{Lcm}$ flowing through $R_{sen}$ is $L_R + 1$ times smaller than the input inductor current $i_1$. Accordingly, $R_{sen}$ of the ICC BPFC should be set as $L_R + 1$ times larger than that of the CPFC, and the $R_{sen}$ loss is expressed as follows:

$$P_{Rsen} = i_{Lcm}^2 (L_R + 1) R_{sen} = \frac{1}{L_R + 1} i_1^2 R_{sen}. \quad (38)$$

Therefore, from (38), the $R_{sen}$ loss of the ICC BPFC can be reduced to $L_R + 1$ times smaller than that of the CPFC.

IV. EXPERIMENTAL RESULTS

The ICC BPFC and CPFC prototypes are implemented with the specifications in Table 1 to verify the feasibility of the proposed ICC BPFC. For a fair comparison, all components used in each converter are identical except for the input diode and inductor (Table 1).

In addition, the following equipment is used to measure the performance of the proposed ICC BPFC: NF DP015S as input power supply, YOKOGAWA WT1804 as power analyzer for input current and power factor measurement, NF DL1000H as electronic load for output load and output current measurement, FLUKE 8808A digital multimeter for input and output voltage measurement, TELEDYNE LECROY waveRunner604 Zi as oscilloscope, and FLIR E30 as thermal imaging camera for thermal measurement. The efficiency is calculated by considering the measured power factor and input and output voltage and current. The measurements are conducted under the following conditions: input voltage $= 90 - 264 V_{ac}$, output voltage $= 400 V_{dc}$, output load $= 600 W$.

Fig. 23 illustrates the experimental key waveforms of the proposed ICC BPFC. In Fig. 23a, $i_{Lcm}$ is almost proportional to $i_1$ and $i_2$, and the value of $i_{Lcm}$ agrees with the result of (5). These results prove that the main inductor current in the ICC BPFC can be simply and cost-effectively sensed by sensing $i_{fit} = i_{Lcm}$ proportional to the main inductor current through only a shunt resistor placed in the return path. Fig. 23b reveals that $i_{Lcm}$ is very small and almost identical to the difference between $i_1$ and $i_2$, suggesting that the low cost two-lead type diode with a low current capacity can be used as the input diode.

![FIGURE 21. Overall efficiency of the CPFC according to L and N at $V_{ac} = 90 V_{rms}$ and $P_o = 600 W$.](image)

![FIGURE 22. Loss comparison between the proposed ICC BPFC and CPFC at $V_{ac} = 90 V_{rms}$ and $P_o = 600 W$.](image)
Fig. 23. Experimental key waveforms of the proposed ICC BPFC at $V_{ac} = 110$ Vrms and $P_o = 600$ W (a) each current of ICC and input line voltage, (b) enlarged waveforms during the positive half cycle of $V_{ac}$.

Fig. 24 and Fig. 25 depict the key components used in each converter and the prototype of the proposed converter, respectively. The bridge diode heat sink of the CPFC and the FETs and output diodes heat sink of the two prototypes were designed to have a similar temperature rise to the input diode of the proposed circuit. For this, the temperature rise of the components was made to 40 $^\circ$C considering the losses of the bridge diode, FETs and output diodes. The two FETs and two output diodes of the proposed circuit are attached to one heat sink, and the sum of the losses of the four components is about 6.73 W as obtained from the loss analysis. In order for the heat generation of the four components to be 40 $^\circ$C, the thermal resistance of the junction to case of the four components should be about 6 $^\circ$C/W when the heat sink is applied. The size and surface area of the heat sink is 205 mm (width) \times 45 mm (length) \times 5.5 mm (height) and 285.7 cm$^2$, respectively so that the thermal resistance of the four components is 6 $^\circ$C/W. The heat sink size of the CPFC bridge diode was derived in the same way. Four bridge diodes were applied in parallel, and the sum of components loss was about 11 W as obtained from the loss analysis, and the amount of temperature rise was selected as 40 $^\circ$C. The thermal resistance of the junction to case of the bridge diodes are about 3.6 $^\circ$C/W so that the heat generation is less than 40 $^\circ$C. The size and surface area of the heat sink is 220 mm (width) \times 35 mm (length) \times 5.5 mm (height) and 241.4 cm$^2$, respectively, so that the thermal resistance of the bridge diodes is 3.6 $^\circ$C/W. The FETs and output diodes heat sink of the CPFC uses the heat sink designed in the proposed circuit as it is for a fair comparison of the two prototypes [19]. To dissipate the large loss expected to be about 11 W, a heat sink as large as 220 mm \times 35 mm is applied to the input bridge diode of the CPFC. In contrast, as the input diode loss of the ICC BPFC is expected to be about 0.5 W per diode,
no heat sink for the input diode $D_{ac}$ is required. Hence, while the input bridge diode of the CPFC exhibits heat generation of 58.1 °C, the input diode of the ICC BPFC exhibits low heat generation of 49.8 °C despite the absence of a heat sink as shown in Fig. 26 and Fig. 27. Hence, the switches and output diodes of the ICC BPFC exhibit higher heat generation than those of the CPFC by about 10 °C but are as low as about 50 °C. This result is because the expected total loss dissipated in switches and output diodes of the ICC BPFC is slightly larger than that of the CPFC by about 3.6 W, as revealed in Fig. 22.

In addition, the heat generation of the proposed ICC is measured as 61.1 °C and 58.8 °C in the wire and core, respectively. The results prove that the magnetics design for the proposed ICC is reasonable.

Fig. 28a displays the measured efficiency according to the line input voltage $V_{ac}$ under the conditions of $P_o = 600$ W and $V_o = 400$ V. Moreover, Fig. 28b reveals the measured efficiency according to the load. These results
FIGURE 28c indicates that the ICC BPFC has an excellent power factor greater than 0.96 at $V_{ac} = 110 \, V_{rms}$. Further, it has a good power factor greater than 0.9 at $V_{ac} = 220 \, V_{rms}$ and $P_o > 200$ W. However, at $V_{ac} = 220 \, V_{rms}$ and $P_o < 200$ W, the power factor is less than 0.9, originating from the skip mode function of NCP1611. Namely, to improve efficiency, PFC IC NCP1611 can be configured to skip the switching operation near the line zero crossing when the line current is low. Furthermore, in Fig. 28d, the line current harmonics of the proposed ICC BPFC satisfy EN 61000-3-2 Class A at a fairly low level.

In Fig. 29, the conducted EMI noise spectra in the proposed ICC BPFC meets the EMI standard with a sufficient margin. These results confirm that the proposed circuit features low conducted EMI characteristics with the aid of cost-effective low current input diodes.

V. CONCLUSION
A new BPFC with a CMC inductor was proposed to overcome the drawbacks of traditional PFCs in this paper. The ICC for the proposed BPFC was also proposed to increase the power density by integrating three inductors into a single magnetic core.

Unlike traditional PFC converters, the magnetizing current $i_{Lcm}$ of the ICC, not the main input current, flows through the input diode. Therefore, a small $i_{Lcm}$ due to the large designed $L_{cm}$ makes it possible to use a low cost and low current two-lead type diode as the input diode. Moreover, as the conduction loss and heat generation of input diodes can be minimized, no heat sink for the input diodes is required. In addition, a small $i_{Lcm}$ flows through one of the two input diodes $D_{acp}$ and $D_{acn}$ according to the polarity of $V_{ac}$; thus, either a live or neutral line of $V_{ac}$ is always connected to the circuit ground, providing good conducted EMI characteristics.

Unlike the CBPFC, SBPFC, and TBPFC, the main inductor current of the proposed ICC BPFC can be simply and cost-effectively sensed by sensing the return current $i_{rt}$ proportional to the main inductor current through only a shunt resistor. In addition, as $i_{rt} = i_{Lcm}$ through the shunt resistor is much smaller than the main current, the sensing resistor loss can be significantly reduced, enabling the use of a low power resistor. The voltage across the CMC inductor has the same waveform regardless of $V_{ac}$. Thus, the ZCD for the CrM operation can be simply and cost-effectively achieved through only one auxiliary winding coupled to the CMC inductor.
The validity of the proposed ICC BPFC was confirmed through a 600 W rated prototype, where the ICC BPFC was simply implemented with the general purpose CrM PFC IC without a floating gate driver. While the input bridge diode of the CPFC requires a large size heat sink of 220 mm × 35 mm, the input diode of the ICC BPFC requires no heat sink. Nevertheless, the input diode of the ICC BPFC demonstrated a low heat generation of 49.7 °C, with 8.4 °C lower heat generation than the input bridge diode of the CPFC.

Moreover, the ICC BPFC demonstrated about 1% higher efficiency than the CPFC due to the reduced conduction loss of the input diode. The line current harmonics of the ICC BPFC satisfied EN 61000-3-2 Class A at a fairly low level. In particular, with the help of low current and cost-effective input diodes, the conducted EMI noise spectra of the ICC BPFC satisfied EN 61000-3-2 Class A at a fairly low level. Moreover, the input diode of the ICC BPFC demonstrated a low heat generation of 49.7 °C, with 8.4 °C lower heat generation than the input bridge diode of the CPFC.

Therefore, the proposed ICC BPFC is expected to be suitable for applications where high efficiency, high power density, and cost-effectiveness are required.

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JU-YOUNG LEE was born in Republic of Korea, in 1989. He received the B.S. and M.S. degrees in electrical engineering from Kookmin University, Seoul, Republic of Korea, in 2015 and 2017, respectively, where he is currently pursuing the Ph.D. degree with the Power Electronic System Laboratory, College of Creative Engineering. His current research interests include high-power-density dc–dc power converters and power-factor-correction ac–dc converters. He is a member of the Korean Institute of Power Electronics (KIPE).