H2Learn: High-Efficiency Learning Accelerator for High-Accuracy Spiking Neural Networks

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Abstract—Although spiking neural networks (SNNs) take benefits from the bio-plausible neural modeling, the low accuracy under the common local synaptic plasticity learning rules limits their application in many practical tasks. Recently, an emerging SNN supervised learning algorithm inspired by backpropagation through time (BPTT) from the domain of artificial neural networks (ANNs) has successfully boosted the accuracy of SNNs, and helped improve the practicability of SNNs. However, current general-purpose processors suffer from low efficiency when performing BPTT for SNNs due to the ANN-tailored optimization. On the other hand, current neuromorphic chips cannot support BPTT because they mainly adopt local synaptic plasticity rules for simplified implementation.

In this work, we propose H2Learn, a novel architecture that can achieve high efficiency for BPTT-based SNN learning which ensures high accuracy of SNNs. At the beginning, we characterized the behaviors of BPTT-based SNN learning. Benefited from the binary spike-based computation in the forward pass and the weight update, we first design look-up table (LUT) based processing elements in Forward Engine and Weight Update Engine to make accumulations implicit and to fuse the computations of multiple input points. Second, benefited from the rich sparsity in the backward pass, we design a dual-sparcity-aware Backward Engine which exploits both input and output sparsity. Finally, we apply a pipeline optimization between different engines to build an end-to-end solution for the BPTT-based SNN learning. Compared with the modern NVIDIA V100 GPU, H2Learn achieves 7.38× area saving, 5.74×10.2× speedup, and 5.25–7.12× energy saving on several benchmark datasets.

I. INTRODUCTION

While the research of artificial neural networks (ANNs) such as deep neural networks (DNNs) have enjoyed great success in the past years [1]–[5], extensive research of spiking neural networks (SNNs) are motivated by the bio-plausible neuron modeling, based on the observations that neurons use spike signals to represent information and communicate with each other. Researchers have provided evidences that SNNs have unique advantages in processing naturally sparse and noisy information [6], [7].

How to train an SNN model with expected functionality is an essential problem for the SNN community. Many early studies have proposed unsupervised local learning based on the biological observation of local synaptic plasticity. In this family, spike timing dependent plasticity (STDP) [8]–[13] has been widely explored, wherein each synaptic weight is modified locally based on the local spiking timing of the neurons wired by the synapse. However, such local synaptic plasticity suffers low accuracy and limited model scale, that is why its use in practical applications has been limited.

In order to improve the accuracy of SNNs, the algorithms in training ANNs are borrowed. For example, the ANN-to-SNN-conversion learning [14]–[16] converts a trained ANN model into its SNN counterpart during inference. Although this method significantly improves accuracy of the resulting SNN, it needs to introduce an extra model switch and results in a long time duration to maintain accuracy, which is not friendly for hardware implementation. Recently, an explicit format of gradient descent to train ANNs has been adapted and applied in training SNNs [17]. Due to the spatio-temporal data paths in SNNs, backpropagation through time (BPTT) is a good fit. Previous studies in the algorithm level have demonstrated the effectiveness of BPTT for SNN learning [18]–[23], which can achieve high accuracy and eliminate the issues of extra model switch and long time duration in the ANN-to-SNN-conversion learning.

Besides the functionality, how to train SNNs efficiently is also an important research topic. Currently, GPUs are still the mainstream platform for neural network training, while they are tailored for ANNs rather than SNNs. This can be reflected by the ANN-aware optimization for the GPUs’ hardware architectures, programming libraries, training frameworks, etc. However, such optimization cannot fully utilize the special data format and computing paradigm of SNNs, thus causing inefficiencies when training SNNs on GPUs.

Beyond GPUs, researchers have also developed domain-specific chips for SNNs, usually termed as neuromorphic chips [24]–[30]. Here we focus on the ones targeting SNN learning rather than inference [31]–[36]. Nearly all currently available SNN learning chips adopt local synaptic plasticity such as STDP for weight update. The good locality without backpropagation makes it easier to implement on decentralized many-core neuromorphic architectures. Although they enjoy low power and fast response, it still cannot escape from the low accuracy of these local learning rules. This is also one of the major reasons why neuromorphic chips have not yet achieved the similar commercial success as deep learning accelerators.

In this work, we propose H2Learn, a specific architecture for high-efficiency BPTT-based SNN learning. After a detailed profiling, we find special characteristics of BPTT in the context of SNNs, which are different from those for recurrent ANNs. Each learning iteration includes a forward pass, a backward
pass, and a weight update stage. One of the two operands for the computational operations in the forward pass and weight update is the binary spike (0 or 1); moreover, the inputs and outputs of the computational operations in the backward pass are quite sparse. For the former feature, we propose a look up table (LUT) based processing element (PE) design that directly stores the partial sums of the results in the LUT and uses the input spikes as addresses to access them. For the latter feature, we design a dual-sparsity-aware architecture and compress the membrane potentials in memory. In this way, the redundant computation and storage can be significantly reduced. Finally, an overall pipeline to optimize the entire learning process is implemented. We summarize our contributions as follows:

- We identify opportunities to achieve both high accuracy and high efficiency in the BPTT algorithm for SNN learning, which overcomes the low accuracy of local synaptic plasticity and the high cost of backpropagation.
- We propose the H2Learn architecture for SNN learning, which consists of a Forward Engine, a Backward Engine, and a Weight Update Engine to execute the three phases in BPTT. In Forward Engine and Weight Update Engine, we design LUT-based PEs to make accumulations implicit and fuse the computations of multiple input points; in Backward Engine, we design an architecture that is aware of both input and output sparsity with less compute overhead and compress the membrane potentials with less memory overhead. The pipeline between different engines is also elaborated to improve the overall performance.
- We conduct extensive experimental evaluations. Our LUT-based Forward Engine/Weight Update Engine and dual-sparsity-aware Backward Engine achieve significant superiority compared with the non-LUT and dense baselines, respectively. On several widely used benchmark datasets, we achieve significantly higher accuracy than prior neuromorphic chips that use local synaptic plasticity; furthermore, H2Learn demonstrates 7.38× area saving, 5.74-10.20× speedup, and 5.25-7.12× energy saving compared with NVIDIA V100 GPU.

II. PRELIMINARIES OF SNNs

SNNs represent the neural networks inspired by the behaviors of neural circuits in the brain. Leaky integrate-and-fire (LIF) is the most widely used spiking neuron model which can capture the typical neuronal behaviors and easy for implementation in hardware. In this work, we focus on the learning of LIF-based SNNs.

Fig. 1(a) illustrates the behaviors of a spiking neuron. The inputs are first weighted by synapses and then integrates by dendrites to update the state of membrane potential (termed as potential in the rest of this work for simplicity) at soma. Once the potential exceeds a threshold ($th_f$), the neuron fires a spike event to its post-connected neurons and resets its potential to a reset value (usually zero); otherwise, nothing happens but the leakage of the potential. A spiking neuron in SNNs is different from an artificial neuron in ANNs. Specifically, (1) there is an intrinsic temporal domain in a spiking neuron but not in an artificial neuron; (2) the potential updating of a spiking neuron depends on both the historic state and the input integration, while the accumulated pre-activation in an artificial neuron just integrates inputs; (3) spiking neurons communicate with each other using binary spike events (0 or 1) while artificial neurons use continuous activations.

![Figure 1: Introduction of SNNs: (a) behaviors of a single spiking neuron; (b) a spiking network; (c) the input format.](image)

III. MOTIVATION

Currently, two bottlenecks hinder the progress of SNNs: (1) low accuracy of conventional local learning rules (e.g., STDP), limiting their competitiveness and application scope in practice; (2) low execution efficiency on GPUs, limiting the exploration of the model scale and space (indirectly limiting accuracy). The former can be significantly improved by the BPTT algorithm, and the latter is due to GPUs’ specific optimization for ANNs, rather than for SNNs with special data format and computing paradigm. Therefore, we propose to design an efficient accelerator for BPTT-based SNN training to improve the competitiveness of neuromorphic chips.

A. LOW-ACCURACY SNN LEARNING ON NEUROMORPHIC CHIPS

In order to build high-efficiency domain-specific chips for SNN learning, researchers have designed neuromorphic chips. However, almost all of them [24]–[30] adopt unsupervised learning rules inspired by bio-plausible synaptic plasticity, such as STDP [8], the good locality of which makes it hardware friendly. However, in practical applications, this rule cannot be accepted due to the low accuracy when performing mainstream tasks (see Table I) and the difficulty in scale-up

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Note: The table (Table I) mentioned in the text is not provided in the image. The specific details in the table are not included in the natural text representation.
when encounter complex tasks, which are the major reasons why neuromorphic chips are suffering skepticisms and are not applied widely as deep learning accelerators.

Table I: Accuracy comparison for SNN learning: STDP vs. BPTT.

| Method | Ref | Dataset | Net | Accuracy |
|--------|-----|---------|-----|----------|
| STDP   | [13] | MNIST   | CNN | 91.10%   |
|        | [14] | MNIST   | CNN | 93.30%   |
|        | [15] | MNIST   | MLP | 95.00%   |
|        | [16] | MNIST   | CNN | 97.50%   |
|        | [17] | MNIST   | CNN | 98.40%   |
| BPTT   | [18] | MNIST   | MLP | 98.60%   |
|        | [19] | MNIST   | MLP | 98.89%   |
|        | [19] | MNIST   | CNN | 99.49%   |
|        | [20] | N-MNIST | MLP | 98.88%   |
|        | [21] | N-MNIST | CNN | 99.20%   |
|        | [22] | N-MNIST | CNN | 99.44%   |
|        | [23] | CIFAR10 | CNN | 89.83%   |
|        | [24] | CIFAR10-DVS | CNN | 58.10%   |

B. Low-Efficiency SNN Learning on GPUs

GPUs play the backbone role in neural network training. However, current GPU hardware architectures (e.g., tensor cores on NVIDIA GPUs), programming libraries (e.g., cuDNN), and model training frameworks (e.g., TensorFlow and Pytorch) are mainly optimized for ANNs rather than SNNs, causing inefficiencies when training SNN models.

Specifically, the inefficiencies come from several aspects. First, the neuronal activities in SNNs are binary spikes, while the computation and storage data formats on GPUs are floating points for the continuous activations in ANNs. Second, there is rich sparsity during backpropagation of SNN training, while GPUs prefer dense computation and storage. At last, the ANN-aware dataflow optimization on GPUs to reduce the memory footprint for intermediate data is not suited for SNNs due to the distinct model behaviors. Table II shows that SNN training is much slower than ANN training on GPU under the same network structure.

Table II: Latency of one training epoch for ANNs and SNNs under the same network structure on NVIDIA V100 GPU.

| Dataset          | Latency of ANNs | Latency of SNNs | Performance Drop |
|------------------|-----------------|-----------------|------------------|
| MNIST            | 12.12s          | 138.55s         | 11.43×           |
| CIFAR10          | 12.98s          | 147.07s         | 11.33×           |
| ImageNet         | 0.73ms          | 4.008s          | 5.56×            |

C. High-Accuracy and High-Efficiency SNN Learning

BPTT Learning for High Accuracy. Recently, researchers began to borrow ideas from the learning of ANNs. Typically, the gradient-descent-based backpropagation algorithms have been applied in SNN training [17–23], among which the backpropagation through time (BPTT) algorithm has become an effective way to train SNN models with high accuracy via global optimization. Table I lists some reported accuracies for SNNs learnt by STDP and BPTT. Apparently, BPTT shows superior accuracy. For the more difficult datasets like CIFAR10, ImageNet, and CIFAR10-DVS, STDP cannot provide good results while BPTT can do (see Table I and Table III). Recent studies [27], [28] also try to reveal the connection between backpropagation and the brain, which is interesting but out of the scope of this work.

Spike-based and Sparse Computing for High Efficiency.

BPTT is a costly learning algorithm with backpropagation across the entire network and all timesteps. Fortunately, we find opportunities after a detailed algorithm profiling.

Table III: Sparsity in the backward pass of BPTT during SNN learning. Abbreviation: I-input, O-output.

| Dataset          | Layer | conv1 | conv2 | conv3 | conv4 | conv5 | conv6 |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| MNIST            | O sparsity (%) | 22.66 | 85.99 | 52.74 | 74.74 | 53.82 | -     |
| Acc: 99.67%      | I sparsity (%)  | 99.18 | 97.46 | 98.76 | 97.44 | 97.93 | -     |
| CIFAR10          | O sparsity (%) | 54.06 | 83.22 | 80.22 | 82.75 | 87.24 | -     |
| Acc: 87.63%      | I sparsity (%)  | 91.41 | 83.89 | 89.92 | 88.63 | 84.39 | -     |
| N-MNIST          | O sparsity (%) | 59.89 | 86.13 | 92.95 | -     | -     | -     |
| Acc: 98.97%      | I sparsity (%)  | 97.24 | 96.36 | 99.26 | -     | -     | -     |
| CIFAR10-DVS      | O sparsity (%) | 62.93 | 88.23 | 82.01 | -     | -     | -     |
| Acc: 63.00%      | I sparsity (%)  | 87.69 | 74.14 | 95.77 | -     | -     | -     |
| ImageNet         | O sparsity (%) | 17.97 | 16.21 | 14.65 | 19.82 | 16.65 | 15.09 |
| Acc: 60.90%      | I sparsity (%)  | 94.95 | 94.11 | 92.94 | 96.02 | 94.38 | 93.35 |

There are three phases in the BPTT learning: forward pass, backward pass, and weight update. In the forward pass and weight update, one of the two operands for the computational operations is a binary spike, which implies that the costly multiplication units are no longer needed. In the backward pass, although multiplication operations cannot be avoided, there is rich sparsity that can be exploited. On one side, one of the operands for the computational operations in the backward pass is the potential gradient that is sparse; on the other side, the outputs are the gradients of spike activities, a part of which will be zeroed out when backpropagating through the firing function. The detailed BPTT for SNN learning can be found in Section IV-A. In Table III we present the input and output sparsity values of each layer during backpropagation. We take several SNN models and datasets for illustration, and the detailed network configuration can be found in Table VI. It can be seen that the sparsity is quite rich, indicating opportunities to reduce compute and storage.

IV. Architecture Design

A. Analysis of BPTT for SNN Learning

In this subsection, we detail the BPTT learning process for SNNs [18], [22], [23]. Table IV summarizes the commonly used variables. We use $\triangledown$ to denote the gradient of the loss function with respect to an intermediate variable, e.g., $\triangledown s = \frac{\partial L}{\partial s}$ and $\triangledown u = \frac{\partial L}{\partial u}$.

Table IV: Definition of variables.

| Var  | Description  | Var  | Description  |
|------|--------------|------|--------------|
| s    | spike        | u    | membrane potential |
| $\triangledown s$ | spike gradient | $\triangledown u$ | potential gradient |
| $\triangledown u$ | spike gradient mask | $\triangledown u$ | potential gradient mask |
| w    | weight       | $\triangledown w$ | weight gradient |
The neuronal behaviors of LIF-based SNNs \([39]\) in the forward pass are governed by

\[
\begin{align*}
\dot{u}_t^i[i] &= \alpha u_{t-1}^i[i](1 - s_{t-1}^i[i]) + \sum_j s_{t-1}^j[j]w_{t-1}^i[j, i], \\
\dot{s}_t^i[i] &= \text{fire}(u_t^i[i] - th_f).
\end{align*}
\]

Here \(u_t^i[i]\) and \(s_t^i[i]\) represent the potential and spike of neuron \(i\) in layer \(l\) at timestep \(t\), respectively. The potential update includes temporal and spatial parts. The temporal part is determined by the potential and spike in the previous timestep and a leakage factor \(\alpha\); the spatial part is determined by the integration of weighted spikes from the previous layer. When the potential crosses a threshold \(th_f\), the neuron fires a spike and resets its potential to zero. \(\text{fire}(\cdot)\) is the Heaviside step function, i.e., \(\text{fire}(x) = 1\) if \(x \geq 0\); \(\text{fire}(x) = 0\) otherwise. Fig. 2(a) illustrates the propagation of the forward pass.

![Figure 2: Information propagation path of (a) the forward pass and (b) the backward pass in BPTT for SNN learning.](image)

During the backward pass, the gradients of spike and potential can be expressed as

\[
\begin{align*}
\nabla s_t^i[i] &= \nabla u_{t+1}^i[i](-\alpha u_t^i[i]) + \sum_j \nabla u_{t+1}^j[j]w_t^i[j, i], \\
\nabla u_t^i[i] &= \nabla u_{t+1}^i[i]\alpha(1 - s_t^i[i]) + \nabla s_t^i[i]\text{fire}'(u_t^i[i]).
\end{align*}
\]

The spike gradient \(\nabla s_t^i[i]\) is also comprised of temporal and spatial parts. The temporal part is determined by the potential gradient and potential at the next and the current timestep, respectively. The spatial part is determined by the integration of weighted potential gradients from the next layer. The propagation in the backward pass is illustrated in Fig. 2(b). The final weight gradient is calculated by

\[
\nabla w_t[i, j] = \sum_i \nabla u_{t+1}^i[j]s_t^i[i].
\]

Originally, the derivative of the step function \((\text{fire}'(\cdot))\) does not exist (a Dirac-like curve), which is known as the non-differentiability of the spike activity. In \([18]\), a pulse curve is proposed to approximate the Dirac-like derivative, as follows

\[
\text{fire}'(u_t^i[i]) \approx \begin{cases} 
\beta, & th_t < u_t^i[i] < th_r, \\
0, & \text{otherwise}.
\end{cases}
\]

This derivative implies that \(\nabla s_t^i[i]\) in the backward pass is valid only when \(\nabla u_t^i[i]\) in the forward pass lies in \([th_t, th_r]\).

We have the following observations for the BPTT learning:

- The spatial parts in Eq. (1) & (2) and the weight gradient calculation in Eq. (3) require the Conv or matrix multiplication (MM) operation in a Conv or FC layer, respectively. Other operations are element-wise, which have much fewer workloads. Therefore, our architecture design makes more efforts to accelerate the costly Conv or MM operations in the context of SNN learning.

- The spikes are in the binary format, i.e. either 0 or 1. It is efficient to store the spike data in a compact format and use LUT-based operation to reduce computation.

- Based on the \(\text{fire}'(\cdot)\) in Eq. (4), we can determine the valid neurons (marked by \(\nabla s\)) that allow the gradient to pass through during the backward pass, according to their potential values in the forward pass. Specifically, when a neuron’s potential is within \([th_t, th_r]\) in the forward pass, it is valid and needs to calculate its spike gradient in the backward pass; otherwise, we can skip the computation (termed as output sparsity in the Backward Engine design, see Section IV-B3). During forward pass, there is also no need to store the potentials (for the use in the temporal part of Eq. (2)) of invalid neurons.

- The goal of learning is to update weights of the model via calculating weight gradients. From Eq. (3), we find that \(\nabla w\) only requires potential gradients and does not involve spike gradients. Therefore, \(\nabla s\) can be treated as intermediate data and merged into the \(\nabla u\) calculation.

We list inputs, outputs, and the major operation of an SNN layer for each training stage in Table V. The variables in the binary format are marked in red. We use bit masks \(\nabla s\) and \(\nabla u\) to indicate which neurons have valid spike gradients and non-zero potential gradients in the backward pass, respectively.

### B. Architecture Design for Individual Engines

In this subsection, we first introduce how to handle data with different formats and then detail the architecture design for each engine in H2Learn. Unlike the training accelerators for ANNs that usually adopt one engine for all training stages \([40, 41]\), we design different engines for each SNN training stage. The philosophy behind this design is that the behavior of...
each training stage is distinct from each other. Specifically, (1) different data formats, i.e., one of the operands in the forward pass and weight update is a spike, however, all operands in the backward pass are real values; (2) different computation characteristics, i.e., the forward pass and weight update can take benefits from spikes to improve efficiency, however, the backward pass utilizes the input and output sparsity to simplify computation; (3) different dataflows, i.e., the Conv (or MM) dataflows in the forward and backward passes are distinct from that in weight update. Based on these special features, that are distinct from ANNs, we design a Forward Engine, a Weight Update Engine, and a Backward Engine, which form the backbone of our \textit{H2Learn}. Finally, these engines can be pipelined during training to gain optimized overall performance.

![Figure 3: Illustration of feature map (FM) tiling: (a) an example of FM tiling; (b) configuration of a tile with different data types.](image)

Fig. 3 shows the feature map (FM) tiling. The dimension of the FMs is $T \times C \times H \times W$, where $T$ represents the total number of timesteps, $C, H,$ and $W$ stand for the height, width, and depth, respectively. For an FM locating at timestep $t$ and channel $c$, we split it into several tiles as shown in Fig. 3a, and the tile corresponds to the basic handling data unit in our design. In this work, we need to consider two data types: binary spike data and floating-point 16-bit (FP16) data. Fig. 3b shows the example of a tile in the two data formats.

![Figure 4: Forward Engine: (a) operation; (b) microarchitecture.](image)

1) **Forward Engine:** We design Forward Engine to handle the forward pass in BPTT learning. From Table V, the Conv of the spatial part in Eq. (1) is the most costly operation, which is shown in Fig. 4a. Each time, Forward Engine takes $T_{\text{max}} \times C_{w'l}$ tiles from $s_{t-1}'$ and performs Conv with a part of weights whose size is $k^2 \times C_{w'l} \times C_{w'l}$ to produce $T_{\text{max}} \times C_{w'l}$ tiles of partial sums $ps_{t}'$ which belong to the spatial part of $u_{l}$. $C_{s'l}$ and $C_{w'l}$ are the numbers of channels of $s_{t-1}'$ and $u_{l}'$, respectively. $T_{\text{max}}$, $C_{s'l}$, and $C_{w'l}$ represent the maximum number of timesteps, channels of $s_{t-1}'$ and $u_{l}'$ that Forward Engine can process at one time. $k$ denotes the weight kernel size. In this work, we call such processing as one grid iteration.

Fig. 4(b) shows the microarchitecture of Forward Engine. In this example, the layout of the PE array is $C_{w'l}$ rows by $C_{w'l}$ columns. In Forward Engine, each row shares the same Tile$_s$ from $s_{t-1}'$ and each column contributes to the same Tile$_u$ in $u_{l}'$. The workflow of Forward Engine in a Conv layer includes following steps: (1) the PE array receives sliding windows from $s_{t-1}'$ and performs the LUT-based Conv (detailed later); (2) each accumulator (Acc) integrates outputs from PEs of the same column; (3) when the partial sum $ps_{t}'$ includes all $C_{s'l}$-1 channels, the result will be sent to Soma to get $s_{t}'$, $u_{l}'$ (abandoned if out of $\lfloor th_{l}, th_{r}\rfloor$), and $\nabla s_{t}'$ (needed in the backward pass). The processing of different sliding windows, timesteps, and samples reuses the PE array resource.

Fig. 5 details each block. Fig. 5(a) shows how to realize spike Conv using LUT. In this example, we perform a Conv between a $2 \times 2$ weight kernel and a sliding window in $s_{t-1}'$. The 2D Conv is traditionally executed as a dot product. However, the inputs are binary spikes in SNNs, thus each sliding window can be represented as one of fixed states, i.e., $2^n$ states for $n$ elements. Here, 4 binary input elements in a sliding window have 16 patterns. We can calculate the Conv results for all possible patterns in advance and store them in an LUT. With this design, we use the input spikes as an access address to load results from the LUT.

However, the LUT-based solution might increase the data need to store. We mitigate the storage consumption by splitting a large LUT into several small sub-LUTs. In Fig. 5a, we use two sub-LUTs to cover different regions of the sliding window, and the LUT size in one PE can be reduced from 16 to 8. Notice that one extra adder is required to accumulate the partial results from sub-LUTs. We call this kind of PE units as LUT PE. Section V-BII shows the detailed analyses for optimal LUT setting. In our design, each LUT PE loads the partial Conv results from all of its sub-LUTs, and the Acc unit accumulates the outputs from the LUT PEs in the same column using an adder tree with FP16 precision as Fig. 5b.

After finishing the spatial part compute, we feed the final $ps_{t}'$ to the Soma unit which will update the potential and determine whether to fire a spike $s_{t}'$ or not as in Fig. 5c. According to our previous analysis, during the backward pass, we only need to store the potentials of valid neurons whose potentials fall into $\lfloor th_{l}, th_{r}\rfloor$. Therefore, Soma generates a compressed $u_{l}'$ without storing zero elements and also produces the corresponding binary spike gradient mask $\nabla s_{t}':$

$$\nabla s_{t}'[i] = \begin{cases} 
1, & \text{if } th_{l} < u_{t}[i] < th_{r}, \\
0, & \text{otherwise}.
\end{cases} \quad (5)$$

For FC layers, the weight matrix size is $C_{s,l-1} \times C_{w,l}$. Each column of the PE array belongs to a $u_{l}'$ channel. We can treat the sub-LUTs in the same column as weight buffers that contain weights of the same output channel but many input channels. The number of input channels for each PE row relies...
Figure 5: Details of each function unit in Forward Engine: (a) LUT PE that performs a part of LUT-based Conv; (b) Acc unit that performs the rest of LUT-based Conv via inter-PE accumulation; (c) Soma unit that produces the spike, compressed potential, and spike gradient mask.

on the size of sub-LUTs in each PE. During processing, each sub-LUT exports a weight element to Acc if the corresponding input spike is 1; otherwise exports 0. We do not compress $u_i$ in FC layers during the forward pass, since the data volume is far smaller than that in Conv layers.

2) Weight Update Engine: We design Weight Update Engine to calculate the weight gradient. From Eq. 3, the weight gradient is calculated by performing a Conv between $s^i$ and $\nabla u^{i+1}$, as shown in Fig. 6(a). Weight Update Engine takes $T_{\text{PE}} \times C_w \times \text{Tile}_a$ as inputs and performs Conv with $T_{\text{PE}} \times C_{\text{PE}}^{i+1} \times \text{Tile}_u$ to produce the partial sum $ps^i_s$ of $\nabla u^l$ whose size is $k^2 \times C_w \times C_{\text{PE}}^{i+1}$.

Forward Engine. Fig. 6(c) shows an example of LUT-based Conv in the Weight Update Engine.

For FC layers, the weight gradient calculation requires a dot product between two matrices whose sizes are $C_w \times T_{\text{PE}}$ and $T_{\text{PE}} \times C_{\text{PE}}^{i+1}$. We directly feed elements in $\nabla u^{i+1}$ to the sub-LUTs. Every PE row shares inputs at the same timestamp. Similar to Forward Engine, each sub-LUT exports an element to the Acc unit based on the state of the spike input.

3) Backward Engine: We design Backward Engine to compute the potential gradient in the backward pass. From table Conv is the major operation, as shown in Fig. 7(a). Backward Engine takes $T_{\text{PE}} \times C_{\text{PE}}^{i+1} \times \text{Tile}_u$ and performs Conv with corresponding weight kernels (after 180° rotation) whose size is $k^2 \times C_{\text{PE}}^{i+1} \times C_w$ to generate $T_{\text{PE}} \times C_{\text{PE}}^{i+1}$ tiles of partial sum $ps^l_s$ for $\nabla s^i$. The operand data type here is FP16, which increases the compute cost. However, we can exploit the output sparsity (indicated by $\nabla s^i$ pre-generated in the Soma unit during the forward pass). Moreover, we can utilize the input sparsity in $\nabla u$ to further simplify computation. Specifically,

Figure 6: Weight Update Engine: (a) operation; (b) microarchitecture; (c) LUT-based Conv.

Figure 7: Backward Engine: (a) operation; (b) microarchitecture.
we use a bitmap $\nabla u$ to record the input sparsity information:

$$\nabla u[l] = \begin{cases} 1, & \nabla u[l] \neq 0, \\ 0, & \text{otherwise.} \end{cases}$$

(6)

From the hardware perspective, we use input and output neuron IDs in a tile to locate valid operands according to the corresponding bitmaps, which will be introduced later.

The microarchitecture of Backward Engine is shown in Fig. 7(b). The PE array layout is $C^{PE} \times \Theta^{s}$ rows by $C^{PE}$ columns. PEs in the same row share the same Tile $v_{s}$ from $u[l]^{1}$ and the corresponding $\nabla u[l]^{1}$. PEs in the same column generate the partial sum $s_{l}$ of the spatial part of the same Tile $v_{s}$ of $s^{l}$, also these PEs share the same $\nabla s_{l}$. The workflow of Backward Engine in a Conv layer has the following steps: (1) Effectual O Finder gets the valid output neuron IDs ($\nabla s$) for Conv according to $\nabla s_{l}$, and decompresses the compressed $u[l]^{1}$ into the original dense format; (2) Effectual I/O Finder further generates valid input and output neuron IDs for Conv according to $\nabla u[l]^{1}$ and the above $\nabla s$; (3) PEs perform Conv that exploits both input and output sparsity; (4) the Acc unit accumulates partial sums from PEs of the same column; (5) the Grad unit calculates $\nabla s_{l}$ and $\nabla u[l]^{1}$. Finally, the produced $\nabla u[l]^{1}$ and the corresponding $\nabla s_{l}$ serve as outputs. The processing of different sliding windows, timesteps ($T^{PE}_{idle}$), and samples reuses the PE array resource.

Fig. 8 shows each function unit in Backward Engine. We consider multi-PEs in a PE group to improve the parallelism of processing a tile. The first functionality of the Effectual O Finder unit is to get the valid output neuron IDs ($\nabla s$) according to the stored spike gradient mask $\nabla s_{l}$ in the forward pass. As an example shown in Fig. 8(a), we take two Output ID Buffers to store the coordinates of $\nabla s$ IDs, which are shared by the PE groups in the same column. ID Decoder scans the elements in $\nabla s_{l}$ row by row, and then writes $\nabla s$ IDs into Output ID Buffers alternatively. In this way, the two buffers can save close amount of $\nabla s$ IDs that need to be processed by PEs in a PE group. Each PE in a PE group would process the workloads stored in one of the buffers. The second functionality of Effectual O Finder is to decompress $u[l]^{1}$ that is stored in a compressed form during the forward pass. This decompression can make the element-wise operations in the Grad unit easier to execute.

Then, each Effectual O Finder unit sends $\nabla s$ IDs to the Effectual I/O Finder units in the same column to search valid multiplications in Conv (termed as valid Conv IDs) wherein both input ($\nabla u[l]^{1}$) and output ($\nabla s_{l}$) are valid (i.e., non-zero). The procedure is shown in Fig. 8(b). We process two Output ID Buffers separately (marked in blue and red). For example, computing the point $\nabla u[2,3]$ (marked in red) needs a Conv between the sliding window $\nabla u[2,3] = \lbrack 2 : 3 : 4 \rbrack$ and the weight kernel. Given the binary potential gradient mask $\nabla u[l]^{1}$, we use a Tag to indicate the state (valid/invalid) of the elements in the sliding window. Next, the Priority Encoder produces a valid Conv ID per cycle based on the Tag. The valid weight value can be found through $w$ ID which corresponds to the valid Conv ID and $\nabla u$ ID can be easily acquired based on the Conv ID and $\nabla u$ ID in $\nabla u$ ID Decoder.

Next, PE units perform the valid MACs. Fig. 8(c) shows an example of the workflow in one PE. Each PE in a PE group executes the MACs according to one of the tasks in the corresponding Effectual I/O Finder. The weight from $w$ and the input from $\nabla u[l]^{1}$ are read according to $w$ ID and
\( \nabla u \cap \) and \( \nabla u \cap \) are generated in the Grad unit. In Eq. (2), we split the gradient calculation into two phases. In phase 1, Grad takes \( ps_t \), \( u_t \) and \( \nabla u_t \) to generate \( \nabla s_t \). In phase 2, besides the calculation of \( \nabla u_t \), we need to generate the potential gradient mask \( \nabla u_t \) that reflects the input sparsity of the next backpropagated layer. These two phases can be easily implemented with element-wise operations.

For FC layers, we do not consider any sparsity, since the computation workloads in FC layers are much fewer than those in Conv layers. We disable Effectual O Finders and Effectual I/O Finders when performing FC layers. In the PE array, the weight buffers in the same column store the weights of different \( \nabla u_t \) channels but of the same \( \nabla s_t \) channel.

C. Overall Architecture and Pipeline

1) Overall Architecture: Fig. [9] shows the overall architecture of H2Learn. In order to reduce the conflicts in data load and store, we use three external memory spaces for simplicity. Specifically, Mem 0 and Mem 1 are used to store spikes, potentials, potential gradients, gradient masks, and weights. During the current forward pass, Forward Engine writes the results into Mem 0(1); while in the next forward pass, the results will be alternatively written into Mem 1(0). Weight Update Engine and Backward Engine request the saved data in the forward pass as their inputs. Mem 2 is designed to store weight gradients that are only used by Weight Update Engine. In real implementation, a single external memory space with a high-bandwidth arbiter is also a possible solution.

![Figure 9: Overall architecture of H2Learn.](image)

We consider the scalability of each processing engine in two directions. The first direction is to increase the size of PE arrays. However, with this change, we should also increase the capacity of global buffers and the off-chip memory bandwidth. Notice that the numbers of rows and columns in each PE array correspond to the number of FMs and timesteps in Conv layers, thus a too large PE array size will decrease the resource utilization for a given Conv layer. Another direction is to increase the number of compute units in a PE group and the number of Acc units. Specifically, in Forward Engine and Weight Update Engine, we increase the number of Acc units to process multiple tiles simultaneously; in Backward Engine, we increase both the number of compute units in a PE group and the number of Acc units. Besides the above scalability directions, we can further use multiple H2Learn to build a distributed system. Each of them runs the learning algorithm with different input samples, and the weight gradients are gathered after all of them finish training.

2) Execution Pipeline: Fig. [10] shows the execution flow of training. The yellow, blue, and red boxes indicate the execution in Forward Engine, Backward Engine, and Weight Update Engine, respectively. The sub-batch represents the batch size that each engine can process at a time. The batch group represents the number of sub-batches for the update of weights. Although every sub-batch involves the calculation of weight gradients, only the last sub-batch in a batch group triggers the weight update. Therefore, the overall batch size can be flexibly reconfigured by adjusting the batch group size. During training, the three engines can be pipelined for higher throughput, i.e., when Backward Engine and Weight Update Engine are processing the current sub-batch, Forward Engine can process the next sub-batch. To enhance the overlap between forward and backward passes and reduce the amount of data need to store in the forward pass, each sub-batch should contain as few samples as possible. We set the sub-batch size to 4 in our design to well utilize the hardware resource.

![Figure 10: Overall pipeline during learning.](image)

V. Evaluation

A. Experimental Setup

Our experiments focus on pattern recognition tasks in both image and spike based datasets that are widely used for SNN evaluation. The image-based datasets include MNIST [42], CIFAR10 [43], and ImageNet [44] that are sampled to spikes; while the spike-based datasets include N-MNIST [45] and CIFAR10-DVS [46] that are originally acquired through DVS [47]. The network configurations are detailed in Table VI.

| Dataset     | Input Size | Network Structure       |
|-------------|------------|-------------------------|
| N-MNIST     | 32 \times 32 \times 2 + T | 128C3-128C3-AP2-384C3-384C3-AP2-512FC-512FC-10FC |
| CIFAR10-DSV | 42 \times 42 \times 2 + T | 64C3(Exo-2)-128C3-AP2-256C3-256C3-AP2-512C3-512C3-AP2-512FC-10FC |
| MNIST       | 28 \times 28 \times 1 + T | 64C3(Exo-2)-128C3-AP2-256C3-256C3-AP2-512FC-512FC-10FC |
| CIFAR10     | 32 \times 32 \times 3 + T | 64C3(Exo-2)-128C3-AP2-256C3-256C3-AP2-512FC-512FC-10FC |
| ImageNet    | 224 \times 224 \times T | 64C3S2(Exo-2)-128C3S2-256C3S2-256C3S2-384C3-256C3-256C3S2-4096FC-4096FC-1000FC |

Table VI: Network configurations. \( T \) is set to 10.
We build cycle accurate simulators for H2Learn and the accelerator baselines in our experiments. The area and energy are measured through synthesized implementations. We implement H2Learn’s RTL and synthesize it in Synopsis Design Compiler with TSMC 28nm library. The area and energy of GLBs are estimated via Cacti [48]. In our simulation, we evaluate the average energy per operation for all compute and storage units, and the total energy is obtained by estimating the number of operations.

| LUT PE Array Size | PE Group Array Size | PE Group Size | # Effective O Finders |
|-------------------|---------------------|---------------|-----------------------|
| 16 (rows) \times 16 (cols) | 16 (rows) \times 64 (cols) | 4           |

Table VII: Specifications of engines in H2Learn.

The configuration of all engines in H2Learn are listed in Table VII. In our evaluation, we build a different baseline model for each engine. Specifically, for Forward Engine and Weight Update Engine, the baseline models adopt non-LUT implementation which consume 36,864 and 40,960 adders, under the parallelism of 4. For the baseline model of Backward Engine, the Effectual O Finder and Effectual I/O Finder units are removed and we do not exploit any sparsity.

Since H2Learn focuses on the training scenario of SNNs, our final target comparison platform is the modern GPU, which is the backbone hardware for training. Table VIII compares the overall specifications between H2Learn and NVIDIA V100 GPU [39]. We will demonstrate that H2Learn can achieve substantial speedup and energy efficiency improvement with far less area consumption in Section V.C.

| H2Learn | GPU V100 |
|---------|----------|
| Technology | TSMC 28 nm | TSMC 12 nm |
| Area | 110.46 mm² | 815 mm² |
| Clock Frequency | 800 MHz | 1530 MHz |
| Off-chip Memory Bandwidth | 128 GB/s \times 3 | 900 GB/s |
| Throughput | 27.85 TFLOPS | 15.7 TFLOPS |
| Power | 20.57 W | 300 W |

B. Evaluation of Engines in H2Learn

1) Forward Engine & Weight Update Engine: Now, we evaluate the LUT-based Engines, i.e., Forward Engine and Weight Update Engine. Fig. 11 shows how the PE configuration affects the area and energy consumption, where both PEs and Acc units are considered. The baseline is a non-LUT design. The LUT configuration is determined by the number of sub-LUTs per PE (#sub-LUTs/PE) and the size of each sub-LUT (sub-LUT size). We assume that the size of each sliding window in Conv is 3 \times 3. We find that when we decrease the #sub-LUTs/PE, the area and energy of computation units (i.e., adders) are reduced, however, the requirement for register files is increased. This is actually a trade-off, i.e., fewer sub-LUTs per PE can save more adders for compute but require more register files for storage.

Figure 11: Evaluation of LUT PE in Forward Engine under different configurations: (a) and (b) energy.

We also estimate the area and energy consumption with different parallelism settings in Acc units. Here the parallelism means that multiple tiles are simultaneously processed in the LUT PE array and the resources for Acc units are copied accordingly. From the results, it can be seen, besides the increased adders in Acc units, the requirement for register files is also increased with a slower slope, since we do not scale up the number of sub-LUTs but use MUX to make sure multiple elements can be read from each sub-LUT in the meantime.

In our design, considering the unified sub-LUT size and lower overhead, we set the #sub-LUTs/PE to 3 and the sub-LUT size to 8 in Forward Engine, corresponding to 3 \times 3 sliding windows. In Weigh Update Engine, the #sub-LUTs/PE is 2 and the sub-LUT size is 16, corresponding to 1 \times 8 sliding windows. For a larger Conv kernel size, we can partition it into multiple smaller kernels and map onto multiple LUT PEs. The overall LUT sizes in Forward Engine and Weight Update Engine are 48 KB and 80 KB, respectively.

Next, we analyze the entire Forward Engine and Weight Update Engine when performing a Conv layer. The size of s, u, and \n are $4 \times 10 \times 256 \times 56 \times 56$ ($N \times T \times C_s$ (or $C_u$, or $C_v$)) \times W \times H), and the size of w is $3 \times 3 \times 256 \times 256$ ($k \times k \times C_s \times C_u$ (or $C_v$)). The results are shown in Fig. 12, where the baseline architecture adopts the naive accumulation-based rather than LUT-based PE. We have the following observations: (1) The PE array consumes most of the area and the LUT-based design can significantly reduce the area overhead; (2) Although the outputs of both Forward Engine and Weight Update Engine are in FP16, the number of columns in the PE array of Weight Update Engine is much larger, leading to a larger GLB size; (3) The energy consumption with different parallelism setting is close, because the amount of total workloads under different parallelism is identical; (4) The throughput can be improved as the parallelism increases and the leakage energy can be
the speedup results are similar when we consider the input or output sparsity only. Finally, when we consider both the input and output sparsity, we can achieve 5.19× speedup and 9.24× energy saving compared with the dense baseline architecture.

3) Design Space Analysis: Table VII shows the configurations of H2Learn. We adopt output stationary dataflow in all engines. Since the inputs of Forward Engine are binary spikes that are more compact than the outputs, we set a larger number of rows (64) in the PE array. Because of the output stationary dataflow, the result is written to external memory for every $C_s/64$ grid iterations, which can help reduce the data traffic. Note that we use ping-pong buffer in GLBs. In Backward Engine, both inputs and outputs are in the FP16 format. We shrink the number of rows (16) but increase the number of columns (64), such that the amount of inputs needing to feed is reduced and the outputs can take longer time ($C_v/16$ grid iterations) to be written to external memory. For Weight Update Engine, the number of rows is set to 10 (allowing to deal with 10 timesteps during a grid iteration), and the number of columns (128) is selected according to the PE array sizes in other two engines.

![Figure 12: Area, energy, and throughput of (a) Forward Engine and (b) Weight Update Engine.](image)

reduced; (5) Compared to the baseline architecture when the parallelism equals 4, our LUT-based solution can achieve 2.35× area saving, 2.58× energy saving in Forward Engine and 2.56× area saving, 3.00× energy saving in Weight Update Engine.

![Figure 13: Backward Engine evaluation: (a) area overhead; (b) energy consumption and speedup.](image)

2) Backward Engine: We adopt the same Conv layer as we used in Section V-B1. As depicted in Fig. 13(a), as the PE group size grows, the area overhead increases but the GLB size does not change obviously since the resulting output volume keeps the same. In Fig. 13(b), we measure the energy and throughput, where we set both the sparsity of $\nabla s^t$ (output sparsity) and $\nabla u^{t+1}$ (input sparsity) to 75%. We first build a dense baseline model without considering any input and output sparsity. We also adopt our architecture to exploit only input or output sparsity as two other baselines. From the results, we find that the leakage consumes a huge amount of energy, which mainly comes from GLB. Another observation is that the energy consumption of the PE array (including the Acc units) occupies the most in the dense architecture, because it cannot bypass any computation. Also, the energy consumed by PE array is much higher when we consider the input sparsity only, since more accumulations of the partial sums are needed when compared with those considering the output sparsity. Since the sparsity settings of $\nabla s^t$ and $\nabla u^{t+1}$ are the same,

![Figure 14: Evaluation of engines in H2Learn with different (a) number of PE array rows, (b) number of PE array columns, and (c) parallelism.](image)

Fig. 13 estimates the throughput of each engine in H2Learn with different architecture configurations, including the number of PE array rows, columns, and the parallelism. The configurations within the red boxes are our optimal selections for each engine in Table VII which consider both optimal performance and balanced compute resources in different engines. The optimal selection can fully utilize but will not be blocked by the off-chip memory bandwidth. Notice that when we evaluate one architecture configuration, we will fix the other two at the optimal settings. We also adopt the same Conv layer for evaluation as in Section V-B1. From the results, we find that the optimal settings can always gain a 2× speedup when compared with the corresponding halved settings. This implies that the external memory bandwidth can satisfy our optimal settings. However, if we keep scaling up the PE array size or
the parallelism, the throughput gain would degrade. In Forward Engine, all architecture configurations cannot get another 2× speedup by doubling the optimal settings. In Weight Update Engine, each PE array row deals with a unique timestep, thus the increase of extra rows is useless if the number of timesteps is small; however, the throughput can be doubled when we scale up the PE array columns or the parallelism. The reason is that, the final outputs of Weight Update Engine is the weight gradients which have a small volume and can stay on-chip until the entire Conv across all FMs finished. This lowers the bandwidth requirement and leaves room for the increase of compute resources. For Backward Engine, the inputs (i.e., $\nabla u$) become the key factor to determine the external memory bandwidth requirement, because the input data type is FP16 and the load of inputs across all channels is more frequently than the write of stationary outputs. The further increase of PE array rows and PE group size cannot achieve 2× performance gain due to the memory bandwidth limitation. In contrast, when the number of PE array columns is doubled, 2× speedup can be obtained, since the amount of input loads is unchanged.

C. Comparison with SpinalFlow and GPU

We compare H2Learn with a state-of-the-art SNN inference accelerator SpinalFlow [36] and NVIDIA V100 GPU [49] on CIFAR10. The input and output sparsity of the networks are shown in Table III. Since SpinalFlow only supports inference, in Fig. [15]a), we compare our Forward Engine with it. We find that H2Learn achieves improvement in terms of area and energy. Although SpinalFlow skips the computations with zero inputs, they need to store entire weights of all output channels to perform computations associated with a valid input, which consumes large area for weight storage and significant power consumption for data accesses. From the functionality perspective, H2Learn shows three distinctive characteristics: 1. H2Learn targets learning while SpinalFlow focuses on inference; 2. H2Learn does not have restrictions on coding schemes, while SpinalFlow only supports temporal coding; 3. H2Learn can support the first encoding layer with hybrid data formats while SpinalFlow cannot.

Then, we compare the throughput of engines in H2Learn with NVIDIA V100 GPU in Fig[15]b). We implement the GPU version of SNN learning in Pytorch. Different from the sub-batch-wise pipeline in H2Learn as Fig[10] the forward pass and backward pass (along with weight update) are performed sequentially at the grain of the whole batch on GPUs as common handling. We find that H2Learn achieves speedup especially in early layers during weight update. In shallow layers, the FM sizes are larger but the number of channels is smaller; besides, weight update needs a 4D rather than 2D Conv. GPU might be inefficient to handle these situations.

Fig. 16 shows the comparison between H2Learn and NVIDIA V100 GPU during training. Because we focus on the processor design and do not estimate the power of the off-chip memory, here we exclude the HBM power of GPU for fairness. Among the results, H2Learn achieve 5.74-10.20× speedup and 5.25-7.12× energy saving. We find that H2Learn takes more benefits on the ImageNet dataset. The potential reason might be caused by more data preprocessing on GPUs under a large FM size. At last, H2Learn is 7.38× more efficient in area overhead.

VI. RELATED WORK

A. Chips for SNN Inference

Many neuromorphic chips target SNN inference. The early ones adopt mixed-analog-digital circuits based designs [31], [33] that are usually power efficient but suffer low accuracy and poor programmability. The modern neuromorphic chips prefer fully digital designs [32], [34]–[36]. In particular, TrueNorth [32] achieves low power via event-driven asynchronous circuits; Tianjic [34], [35] bridges ANNs and SNNs using a hybrid architecture with a unified routing infrastructure; Spinalflow [36] designs an accelerator that can skip redundant computations via input scattering. Different from them for SNN inference, H2Learn targets SNN learning.

B. Chips for SNN Learning

Most of SNN learning chips are designed to implement local synaptic plasticity rules. Similarly, there are also early analog circuits based designs [24], [26] and modern digital solutions [27]–[30]. Specifically, ODIN [27] is the digital version of ROLLS [26] with only one core per chip, and Morphic [28] is an enhanced version with a hierarchical routing topology; Loihi [29] adopts a many-core architecture, while FlexLearn [30] further extends the scope of synaptic plasticity rules. Some studies exploit either SNN inference or training on FPGA [50]–[52]. Unlike implementing the local synaptic plasticity rules with lower accuracy, H2Learn selects the BPTT learning rule to achieve high accuracy and elaborates the architecture to achieve high efficiency. We also notice a recent work [33] supporting BP (not BPTT) for SNNs, but it adopts a LIF variant without temporal propagation, focuses on exploiting the non-volatile memory technology, and only shows results on the small MNIST dataset with two FC layers.
We propose H2Learn, an end-to-end accelerator that can implement BPTT-based SNN learning for both high accuracy and high efficiency. Our LUT-based PE design in Forward Engine and Weight Update Engine exploits the spike-based computation; our dual-sparsity-aware Backward Engine exploits both input and output sparsity. Compared with the modern NVIDIA V100 GPU, H2Learn demonstrates 7.38× area saving, 5.74-10.20× speedup, and 5.25-7.12× power saving on several typical benchmark datasets.

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