A New Software Phase-locked Loops

Cunbing Gui¹, Zhangbao Chen² and Xuehui Luo¹

¹Guangzhou Institute of Technology, Guangdong, China
²The Education Training and Evaluation Center of Guangdong Power Grid Co., Guangdong, China
E-mail: ahui200491@126.com

Abstract. A new type software phase-locked loops is proposed. The amplitude integral and selective characteristic of frequency are used to form the positive frequency fundamental filter. The $K$ is derived, the principle of the variable sampling period phase-locked loops is further analyzed, it’s mathematical is established, and the regulators parameters is optimize designed. Simulation and experiment show that the proposed phase-locked loops can lock the phase and frequency of the positive sequence fundamental voltage quickly and accurately, So it can provides a reliable base for grid-connected system.

1. Introduction
Phase-locked loop is a way to stabilize the frequency, it is mainly composed of a voltage-controlled oscillator and a phase-locked loop integrated circuit, the voltage-controlled oscillator gives a signal, part of this signal is output, and part of this signal is compared in phase with the local oscillator signal, the local oscillator signal is produced by the frequency division and phase-locked integrated circuit, in order to maintain the consistency of their frequencies, the phase difference between them should not change, if there is change of the phase difference, the phase-locked loop integrated circuit voltage output voltage will change to make the phase difference recovery. With the rapid development of new energy power generation, the quality of phase-locked loop directly affects the performance of various grid control performance of the inverter, the detect accuracy of the grid voltage synchronizing signal will affect the normal operation and control of the converter [1]. The influence of 100 hz signal can be eliminated, but the filtering effect of the traps will be affected when the frequency changes. A decoupled double synchronous reference frame phase-locked loop (DDSRF-PLL) is proposed, it can efficiently reduce the influence of negative sequence component to the synchronous signal, but the structure is complicated. Adaptive notch filter (ANF) and double second-order generalized integrator (DSOGI) were also proposed to detect the fundamental positive and negative sequence components [2], but it cannot distinguish positive sequence and negative sequence components from the fundamental component, it is need to use the instantaneous symmetrical component method for the separation of positive and negative sequence component, the algorithm is complicated. Multiple second order generalized phase-closed loops (MSOGI-PLL) was proposed, multiple complex coefficient filter based phase-locked loops (MCCF-PLL) was also proposed in reference, but all these two methods need to set the specific harmonic frequency in advance, multiple basic computing units should be designed, thus make the system structure complicated, a three-phase phase-locked loops method was also proposed, which is based on four extended phase-locked loops (EPLL), but the parameter design process is more complicated, a phase locked loops based on double synchronous reference frame (DSRFPLL) was also proposed, in which the orthogonal signal generator, the positive and negative sequence component calculator were included to extract the positive sequence component and
eliminate the influence of voltage unbalance. An adaptive complex filtering phase locking method based on the crossover decoupling frequency was also proposed, but these two kinds of methods are also more complex. According to the research on above, a new phase-locked loops is proposed in this paper, this new phase-locked loops, without more software resources, it can fast and precisely track the changing frequency and phase of power grid, it has adaptability to the frequency and distortion of power grid.

2. The positive sequence fundamental filter

2.1. The positive sequence fundamental filter

If the sine signal is \( u_1 = U \sin(\omega t + \varphi) \), the corresponding auxiliary signal is \( u_2 = U \cos(\omega t + \varphi) \) when \( u_1 \) is shifted 90° phase, then it can be derived:

\[
u(s) = \frac{s}{s^2 + \omega_0^2} u_1(s) + \frac{\omega_0}{s^2 + \omega_0^2} u_2(s)
\]

(1)

It also can be derived that when the integral process accumulated to per unit time, \( u(s) = u_1(s) \), \( u(s) = u_2(s) \), in order to improve the speed of tracking, the negative feedback is introduced respectively to the input, proportional control is used, the proportion coefficient is selected as K, the corresponding closed-loop transfer function is shown as follows:

\[
G(s) = \frac{2Ks}{s^2 + 2Ks + \omega_0^2}
\]

(2)

When the the distorted power grid voltage is used as the input, then the \( u(s) \) is the corresponding positive sequence fundamental voltage filter. The schematic diagram of positive sequence fundamental voltage filter in time field is shown in Figure 1.

![Figure 1. Schematic diagram of positive sequence fundamental voltage filter in time field](image)

Where \( \alpha_{in}(t) \) and \( \beta_{in}(t) \) is the input power grid voltage in two-phase static coordinate, \( \alpha_{out}(t) \) and \( \beta_{out}(t) \) is the positive sequence fundamental voltage in two-phase static coordinate.

When the input voltage signal is the positive sequence signal, it can derived:

\[
\alpha_{in}(t) = (K \frac{s + K}{(s + K)^2 + \omega_0^2}) (A \frac{s \cos \varphi - \omega \sin \varphi}{s^2 + \omega_0^2}) - (K \frac{s}{(s + K)^2 + \omega_0^2}) (A \frac{s \sin \varphi + \omega \cos \varphi}{s^2 + \omega_0^2})
\]

(3)

When the input voltage signal is the negative sequence signal, the expression of \( \alpha_{in}(s) \) can be derived similarly.

2.2. The choice of K

The relation between K and the frequency deviation and phase deviation can be derived as following:
\[
\tan(90^\circ - \Delta \phi) \approx \frac{K}{2\pi \Delta f}
\]  

(4)

Where \( \Delta f \) is the frequency deviation of the power frequency, \( \Delta \phi \) is the phase deviation of power voltage, so take the K value as 60 [3].

3. The adaptive sampling period technique

Sampling points is kept as constant in a fundamental period, sampling period is defined as follows:

\[
T_S = \frac{T_0}{N}
\]  

(5)

Where: N is the sampling points in one fundamental period, \( T_0 \) is the fundamental period of power grid.

The voltage-controlled oscillator transfer function in z domain of three-phase phase-locked loops, which is controlled base on adjustable control period, can be derived as follows[1]:

\[
V_{co}^{'}(z) = \frac{\hat{\theta}(z)}{T(z)} = -\frac{\omega_0}{z^2 - z}
\]  

(6)

It can be seen from equation (6) that the Phase-locked loops voltage controlled oscillator is a second order system, when the non-dominant pole \( z=0 \) is ignored, \( V_{co}^{'}(z) \) can be simplified as follows:

\[
V_{co}^{'}(z) = -\frac{\omega_0}{z - 1}
\]  

(7)

When the sampling time is \( t_s = 0.0001 \text{ s} \), the corresponding closed-loop transfer function can be derived as following: \( \bar{\xi} \) is set to 0.707, \( t_s \) is set to 5ms. Considering response speed and steady accuracy, \( K_p \) is set to 20, \( K_i \) is set to 1.

\[
\Phi_i(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{K_p(s) + K_I}{s^2 + K_p s + K_I}
\]  

(8)

New software phase-locked loops block diagram base on variable sampling period and the positive sequence fundamental voltage filter is shown in Figure 2.

![Figure 2](image_url)

Figure 2. The block diagram of new software phase-locked loop.

4. Simulation

At the time of \( t=0.5 \text{ s} \), the dc bias component of \( d_a = 5 \text{ V} \), \( d_b = 10 \text{ V} \), \( d_c = -10 \text{ V} \) is separately added the symmetric three-phase voltage system, in this case, the frequency information extracted by the method
proposed in this paper, the method of SRF-PLL, the method proposed in reference [4], is respectively shown in Figure 3.

As shown in Figure 3, the yellow line parts is corresponding to the extracted synchronization signals of frequency used with the method proposed in this paper, orange color line parts is corresponding to the extracted synchronization signals of frequency used with the method of SRF-PLL, green color line parts is corresponding to the extracted synchronization signals of frequency used with the method proposed in reference [4], it can be easily deduced that When there are dc bias component contained in the input three-phase voltage, the extracted synchronization signals of frequency is ac component fluctuating around 50hz when it is extracted by the SRF-PLL or by the method proposed in reference [4], so the synchronization performance is greatly affected, when the method proposed in this paper is used the affection of the dc bias component can be eliminated, so the synchronization performance is good.

At the time of 0.10s, third harmonic voltage which it’s amplitude is 15% of the positive sequence fundamental voltage amplitude is added to the three-phase voltage, the waveform of positive sequence fundamental voltage and the synchronous phase angle is shown in Figure 4.

As shown in Figure 4, the yellow line parts is corresponding to the extracted synchronization signals of frequency used with the method proposed in this paper, orange color line parts is corresponding to the extracted synchronization signals of frequency used with the method of SRF-PLL, green color line parts is corresponding to the extracted synchronization signals of frequency used with the method proposed in reference [4], it can be easily deduced that When there are dc bias component contained in the input three-phase voltage, the extracted synchronization signals of frequency is ac component fluctuating around 50hz when it is extracted by the SRF-PLL or by the method proposed in reference [4], so the synchronization performance is greatly affected, when the method proposed in this paper is used the affection of the dc bias component can be eliminated, so the synchronization performance is good.

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At the time of 0.10s, third harmonic voltage which it’s amplitude is 15% of the positive sequence fundamental voltage amplitude is added to the three-phase voltage, the waveform of positive sequence fundamental voltage and the synchronous phase angle is shown in Figure 4.
In this case, the peak synchronous phase difference is less than 1 degree.
At the time of 20ms, the power grid frequency changes from 50Hz to 60Hz, the frequency and phase of power grid is locked after about two cycles by the new software phase-lock loop, the power grid voltage of A phase and positive sequence fundamental voltage output from the new software phase-locked loops are shown in Figure 5.
It can find that the rapidity and accuracy of locking frequency and phase is demonstrably superior.

5. Experiments
When the dc bias component of \( d_a = 5\text{V} \), \( d_b = 10\text{V} \), \( d_c = -10\text{V} \) is separately added the symmetric three-phase voltage system, the extracted synchronization signals of frequency is shown in Figure 6.

![Figure 6. The experimental extracted synchronization signals of frequency](image)

As shown in Figure 6, the existence of dc bias component have little effect on the extraction of synchronization signals of frequency.
When the third harmonic voltage which it’s amplitude is 15% of the positive sequence fundamental voltage amplitude is added to the three-phase voltage, the experimental waveform of three-phase voltage is shown in Figure 7

![Figure 7. The experimental waveform of positive sequence fundamental voltage and the synchronous phase angle when third harmonic voltage is added](image)

As shown in Figure 7, the peak synchronous phase difference is very small.
When the power grid frequency changes from 50Hz to 60Hz, the power grid voltage of A phase and positive sequence fundamental voltage output from the new software phase-locked loops are shown in Figure 8.
Figure 8. The experimental power grid voltage of A phase and positive sequence fundamental voltage waveform when the power grid frequency changes.

As shown in Figure 8, the frequency and phase of power grid can locked in about two periods by the new software phase-lock loop.

6. Conclusion
The theory of positive sequence fundamental filter and function model of variable sampling period phase-locked loops are first analyzed in this paper, the relatively design parameters were given, on this basis, a kind of frequency adaptive software phase-locked loops is proposed which combine the advantages of the above filter and variable sampling period phase-locked loops. The results of simulation and experiment indicate that the effects of some disturbances can be eliminated effectively, synchronous fundamental frequency voltage sign can be got quickly, so the new software phase-locked loops proposed in this paper has strong advantage. The application research of software phase-locked loop in the new energy field should be intensified in the future.

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