Current-Mode Deep Level Transient Spectroscopy of a Semiconductor Nanowire Field-Effect Transistor

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One of the main limiting factors in the carrier mobility in semiconductor nanowires is the presence of deep trap levels. While deep-level transient spectroscopy (DLTS) has proved to be a powerful tool in analysing traps in bulk semiconductors, this technique is ineffective for the characterisation of nanowires due to their very small capacitance. Here we introduce a new technique for measuring the spectrum of deep traps in nanowires. In current-mode DLTS (I-DLTS) the temperature-dependence of the transient current through a nanowire field-effect transistor in response to an applied gate voltage pulse is measured. We demonstrate the applicability of I-DLTS to determine the activation energy and capture cross-sections of several deep defect states in zinc oxide nanowires. In addition to characterising deep defect states, we show that I-DLTS can be used to measure the surface barrier height in semiconductor nanowires.

I. INTRODUCTION

Semiconductor nanowires are promising candidates for application in nanoelectronics. Various nanowire-based devices including field-effect transistors [1, 2], sensors [3], axial and core-shell heterostructures [4] and single-electron transistors [5] have been reported. The electrical properties of nanowires dramatically depend on defects located both in the nanowire core and on the nanowire surface [6]. Thus the understanding of defect behaviour is crucial for controlling nanowire transport properties. The investigation of electrically active deep level defects in bulk semiconductors is usually carried out by means of transient techniques such as deep level transient spectroscopy (DLTS) [7] and its derivatives (e.g. photoinduced current spectroscopy PICTS [8] and current transient spectroscopy [9]), thermostimulated current [10], electron paramagnetic resonance and others. Here the term “deep level” denotes a state that is located deep in the semiconductor band gap (i.e. at energies lower than $E_C - k_B T$ and higher than $E_V + k_B T$, $E_C$ and $E_V$ being the conduction band minimum and valence band maximum, respectively).

Investigation of the electrically active deep defect states in nanowires by DLTS is a challenging task, mainly due to the difficulties of measuring the very small capacitances of nanowire devices. Only a few papers have therefore been published on nanowire deep levels: DLTS in combination with PICTS was used to study catalyst-related electrical defects in an array of Si nanowires [11]; DLTS was used to study a single GaN nanowire pn-junction [12]; and low frequency noise spectroscopy (LFNS) was applied by Motayed et al. to investigate the effects of metal catalysts on Si nanowires [13].
A different approach has been used to study nanoscale devices (such as thin film field-effect transistors), exploiting current-mode DLTS (I-DLTS) as opposed to the conventional capacitance-mode DLTS \[15\]. In I-DLTS the relaxation of the current through the channel in response to a gate voltage pulse is measured. I-DLTS is a non-destructive technique which can be carried out directly on a device in a transistor geometry and does not need any additional fabrication steps. Since nanowire field effect transistors may become constituents of future electronic devices, I-DLTS is a promising technique to study them.

In this paper we present I-DLTS measurements carried out on individual semiconductor nanowire field effect transistors. Theoretical models for conductivity relaxation driven by states on the nanowire surface are proposed. In addition to the usual characterisation of the deep traps in the semiconductor, an analytical model allows the measurement of the surface band-bending of a ZnO nanowire. These results corroborate data obtained using surface sensitive techniques such as ultraviolet photoelectron spectroscopy \[16\] and surface photovoltage measurements \[17\].

A. Current-mode deep level transient spectroscopy in nanowires

1. I-DLTS method

In I-DLTS measurements on nanowire FETs, a fixed drain-source voltage $V_{ds}$ is applied to the nanowire resulting in a constant current $I_{ds,0}$ through the nanowire. The gate voltage is kept at a quiescent value $V_{GQ}$ and a gate voltage pulse $\Delta V_G$ is applied periodically with period $T_P$ and width $t_P$ (figure 1.a). In n-type nanowires (like ZnO), a positive pulse $\Delta V_G$ populates deep trap states with electrons, which, after the end of the pulse, get emitted from the deep traps with an emission rate $e_n$, contributing to the relaxation current $\Delta I(t) = I(t) - I_{ds,0}$ through the nanowire (figure 1.b). The I-DLTS signal is constructed by measuring the relaxation current at times $t_1$ and $t_2$ after the end of the pulse and subtracting them: $I_{DLTS} \equiv I(t_1) - I(t_2)$.

The rate of carrier emission $e_n$ from the deep traps can be expressed as: $e_n \propto \sigma_0 \exp(-E_{dl}/k_BT)$, where $E_{dl}$ is the deep trap activation energy, $\sigma_0$ the trap cross-section and $k_B$ Boltzmann’s constant. Hence the emission rate will vary with the temperature $T$. At sufficiently low temperatures the emission rate will be much lower than $t_2^{-1}$, resulting in $I(t_1) - I(t_2)$ being close to zero. Conversely, at high temperatures the emission rate will be much higher than $t_1^{-1}$, also resulting in $I(t_1) - I(t_2) = 0$. At some intermediate temperature, $T_{max}$, $I_{DLTS}$ will reach a peak value (figure 1.c). The value of $T_{max}$ depends on the choice of $t_1$ and $t_2$. Assuming an exponential time dependence of the current $\Delta I(t) \propto \exp(-e_n t)$, at temperature $T_{max}$ there is an unambiguous relation between the emission rate and the times $t_1$ and $t_2$: $e_n(T_{max}) = \frac{\ln(t_2/t_1)}{t_2-t_1}$ \[7\]. By choosing different values of $t_1$ and $t_2$ and measuring the temperature at which the maximum in $I_{DLTS}(T)$ occurs, we obtain the dependence of $e_n$ on temperature. From this dependence we can obtain the apparent cross-section of the trap $\sigma_0$ and its energy position in the band gap $E_{dl}$.

It will be shown later that electron emission from the electron traps generally results in a negative current transient signal as shown in figure 1.b. This gives rise to an I-DLTS minimum (figure 1.c). Conversely, hole emission will result in the opposite current transient sign, giving rise to an I-DLTS maximum. Semiconductor nanowires have different types of trap residing in the core of the nanowire, on its surface, and on the semiconductor-dielectric or semiconductor-metal interfaces. These traps will affect the current through the nanowire in different ways. An account of the physical phenomena that govern the dynamics of the carriers due to the deep surface trap states is given in the next section.
FIG. 1: I-DLTS principle of operation. (a) Time-dependence of the gate voltage; (b) time-dependence of the current through the nanowire; (c) I-DLTS spectra constructed using two different sets of times ($t_1$, $t_2$) and ($t'_1$, $t'_2$)

2. Current through the nanowire FET

In general, surface band bending affects the conductivity in a nanowire. For example, ZnO nanowires have a surface charge depletion layer due to a negative surface charge with the dominant conductivity happening in the core of the nanowire [16, 17]. InAs nanowires, on the other hand, have a surface electron accumulation layer which accounts for the main contribution to the conductivity [18].

It can be shown (Supplementary information I) that the current through a nanowire can be expressed as:

$$I_{ds} = \frac{\mu_{\text{eff}} C_{\text{oxide}}}{L^2} [V_G + V_T] V_{ds};$$

$$V_T = \frac{Q_{ss}/C_{\text{oxide}}}{} + \frac{q\pi R^2 N_d L}{C_{\text{oxide}}},$$

where $\mu_{\text{eff}}$ is the effective carrier mobility, $V_G$ and $V_{ds}$ are the gate voltage and drain-source voltage respectively, $V_T$ is the threshold voltage, $Q_{ss}$ the surface state charge, $N_d$ the concentration of ionised shallow donors, $L$ the distance between contacts and $R$ the radius of the nanowire. Capacitance $C_{\text{oxide}}$ is calculated based on the model of a metallic wire above a charged plane (Supplementary information I). Equation (1) coincides well with the usual transistor formula in the linear regime [1] [19] with the additional term $Q_{ss}/C_{\text{oxide}}$. Because it is usually difficult to estimate the surface
state concentration, this extra term can cause ambiguity in the estimation of the ionised donor concentration $N_d$.

![Diagram](image)

**FIG. 2:** Model of nanowire band bending for an n-type nanowire with a negative surface charge and surface depletion region. (a) equilibrium condition, $V_G = 0$; (b) band diagram of the nanowire under applied negative gate voltage; (c) graphic representation, with orange region being the conductive core and blue region being the depletion region; (d) dependence of the surface barrier voltage on the effective negative gate voltage for ZnO nanowires with different donor concentrations, according to equation [2].

Figure 2 schematically depicts a standard ZnO nanowire with a surface depletion region due to negatively charged surface states which are attributed to the absorbed oxygen molecules. Carrier capture onto the surface states depends on the surface barrier height $qV_B = E_b$. It can be seen in figures 2a,b that the surface barrier for electrons is affected by the gate voltage. The relationship between the gate voltage and the nanowire surface barrier height for a partially depleted nanowire can be expressed as (Supplementary information I):

$$V_B(V_{G,\text{eff}}) = \frac{qN_d W_d(V_{G,\text{eff}}) [2R - W_d(V_{G,\text{eff}})] \ln(R/[R - W_d(V_{G,\text{eff}})])}{2\epsilon_0\epsilon_{\text{ZnO}}},$$  

(2)
where $W_d$ is the depletion region width:

$$W_d(V_{G,\text{eff}}) = R - \sqrt{R^2 - \frac{C_{\text{oxide}}V_{G,\text{eff}}}{qN_d\pi L}}. \quad (3)$$

Here $V_{G,\text{eff}}$ is the effective gate voltage $V_{G,\text{eff}} = Q_{ss}/C_{\text{oxide}} + V_G$ and $\varepsilon_{\text{ZnO}}$ the dielectric constant of ZnO. Figure 2.d shows the dependence of the barrier height $V_B$ on $V_{G,\text{eff}}$. In particular, for a typical ZnO nanowire with surface barrier of 0.3 eV and with donor concentration $N_d = 5 \cdot 10^{19}$ cm$^3$, an increase of the surface barrier by 0.1 eV (i.e. from 0.3 to 0.4 V) requires the gate voltage to change by 5 V.

3. Current transient in nanowires. Emission and capture from the surface trap

Deep electron traps located in the semiconductor volume (in bulk) will affect the current and capacitance transient behaviour \cite{7}. The current transients in thin film transistors are affected by both bulk and surface traps. Since nanowires exhibit very high surface-to-volume ratio, the current transient will predominantly depend on the surface states. Moreover, ZnO is known to be very surface sensitive \cite{20}, therefore we will consider here only the surface traps.

Let us consider surface electron traps that are uniformly distributed on the surface of the n-type nanowire (figure 3). At quiescent gate voltage bias $V_{GQ}$, surface traps below the Fermi energy (with activation energy $E_{\text{ss,2}}$) are filled with electrons, while those traps above the Fermi energy (with activation energy $E_{\text{ss,1}}$) are empty (figure 3a). When a positive gate voltage pulse $\Delta V_G$ is applied, the Fermi energy changes its position, with surface traps below the Fermi energy capturing electrons. According to Shockley-Read-Hall statistics \cite{21, 22}, the capture of electrons onto the surface states follows an exponential law with capture rate $c_n$ which depends on the surface barrier $qV_B$ (figure 3b). The change in time of the number of electrons captured on the surface state $n_{ss}(t)$ is:

$$n_{ss}(t) = n_{ss,max} \left(1 - \exp(-c_n t)\right);$$

$$c_n = \sigma_{ss} \gamma T^2 \exp(-qV_B/k_BT), \quad (4)$$

where $\sigma_{ss}$ is the surface state capture cross-section, $n_{ss,max}$ the maximum possible number of trapped electrons and

$$\gamma = 2\sqrt{3}(2\pi)^3/2h^{-3}k^2m^*, \quad \text{with } m^* \text{ the effective electron mass. We assume as an approximation that the barrier height } V_B \text{ is constant in time during the charge capture. It will however depend on the gate voltage as outlined in section 1A.2}

At the end of the positive gate voltage pulse, the number of electrons trapped on the surface traps is $n_{ss,0} = n_{ss,max} \left(1 - \exp(-c_n t_p)\right)$. When the gate voltage returns to the quiescent bias value, the filled levels start emitting electrons into the conduction band (figure 3c). The time-dependence of the number of carriers trapped on the surface levels $n_{ss}(t)$ is:

$$n_{ss}(t) = n_{ss,0} \exp(-c_n t);$$

$$c_n = \sigma_0 \gamma T^2 \exp(-E_{\text{ss}}/k_BT), \quad (5)$$
FIG. 3: Mechanism of the current transient in nanowires due to surface states: (a) quiescent gate voltage conditions \( V_{GQ} \); (b) positive gate voltage pulse \( \Delta V_G \) and electron capture onto surface states; (c) emission of electrons from the filled traps into the conduction band at the quiescent gate voltage.

where \( E_{ss} \) is the energy difference between the energy level of the surface trap and the conduction band and \( \sigma_0 \) is an effective minority carrier capture cross section.

The change in population of the surface levels will result in a current transient through the nanowire. Both surface and bulk traps will effectively change the surface state charge \( Q_{ss} \) in equation [4]. Surface charge may be represented as a sum of the constant surface charge and the transient surface charge: \( Q_{ss}(t) = Q_{ss,0} + qn_{ss}(t) \). Taking into account negative charge of electrons for n-type nanowire, we get the current transient through the nanowire:

\[
\Delta I(t) = -\frac{qV_{ds}\mu_{eff}}{L^2} \Delta Q_{ss}(t); \\
\Delta I_{emission}(t) = -\frac{\mu q}{L^2} V_{ds} n_{ss,0} \exp(-e_{n}t); \\
\Delta I_{capture}(t) = \frac{\mu q}{L^2} V_{ds} n_{ss,max} \exp(-c_{n}t).
\] (6)

Emission mode and capture mode I-DLTS may be used to infer trap energies \( E_{ss} \) and the barrier height \( V_B \), respectively. Both methods were exploited in this work. Here, we will neglect the temperature dependences of the Fermi level position and the carrier concentration. Therefore, we assume that the values of \( n_{ss,0} \) and \( n_{ss,max} \) are independent of temperature for given quiescent gate voltage, gate voltage pulse magnitude and gate voltage pulse width.

4. I-DLTS. Measurement setup

The I-DLTS measurement setup is shown in figure [4]. A ZnO nanowire field effect transistor with back-gate is used for the measurement. The drain-source voltage through the nanowire is kept constant at \( V_{ds} = 0.2 \) V. A negative
quiescent gate voltage bias of $V_{GQ} = -10$ V keeps a large area of the n-type nanowire cross-section depleted. Gate voltage pulses $\Delta V_G$ of 10 V amplitude and 100 $\mu$sec duration are applied to the gate of the nanowire FET with repetition rate between 0.1 and 1 kHz. The current through the nanowire is probed by the differential pre-amplifier across a reference resistor whose resistance is much smaller than the nanowire resistance. The DC component of the current is filtered out and the relaxation current is amplified. The signal is supplied to the oscilloscope, averaged and digitised. The I-DLTS signal $I_{DLTS} = I(t_1) - I(t_2)$ is measured at different temperatures.

The behaviour of the $I_{DLTS}$ peak depends on the prefactor in equation 6. It can be shown, that if we choose times $t_1$ and $t_2$ so that $t_1$ varies but the ratio $t_2/t_1$ is fixed, then the magnitude of the $I_{DLTS}/I(T)$ peak corresponding to a specific trap level will be independent of temperature.

Here for the deep level analysis, the $t_2/t_1$ ratio is fixed to 2. The time value $t_1$ ranges from 50 $\mu$sec to 4 msec.
II. EXPERIMENTAL DETAILS

A. ZnO nanowire field effect transistor

ZnO nanowires were grown on Al₂O₃(0001) substrates by oxygen plasma assisted molecular beam epitaxy using gold as a catalyst. Details of the growth conditions and nanowire properties are published elsewhere [24]. Nanowires are 40–100 nm thick and 1–4 μm long. The as-grown sample was ultrasonicated in 2-propanol to remove nanowires from the substrate. A droplet of the nanowire-2-propanol solution was deposited and dried on an oxidised silicon substrate with 120 nm silicon oxide thickness. Metal contacts to the nanowires were patterned by electron beam lithography. Nanowires were argon ion-beam milled for 30 seconds and Ti/Au contacts were sputtered onto them (figure 5.a) without breaking vacuum. The Ar ion milling was performed to remove an amorphous surface layer and thereby to decrease the contact resistance [25]. After fabricating the sample, the substrate was mounted onto the copper block of a chip carrier, which, in turn, was mounted on the end of the dip probe. Liquid helium was used to cool the sample down to 4.2 K.

FIG. 5: (a) Scanning electron image of a connected nanowire; b) room temperature current voltage characteristics of the nanowire at different gate voltages; c) the gate voltage dependence of drain-source current; d) semi-logarithmic plot of the temperature dependence of nanowire resistance; inset: resistance on a logarithmic scale as a function of inverse temperature.

Room temperature transport characteristics were measured with a Keithley 4200 semiconductor characterization system. The drain-source voltage dependence of the current of a typical ZnO nanowire is shown in figure 5.b, showing...
Ohmic behaviour. Four-point probe measurements showed negligible contact resistance. The resistance of the ZnO nanowires ranged from 100 kΩ to 1 MΩ. The dependence of the drain source current on the gate voltage is depicted in figure 5.c. The On/Off ratio was approximately $10^6$. The field effect mobility of the nanowire was calculated from the drain-source current using equation [1]. The nanowire effective mobility at room temperature varied from 3 to 70 cm$^2$/V·sec from wire to wire. The effective carrier concentration of the nanowires ranged from $10^{18}$ to $10^{19}$ cm$^{-3}$. Resistance, mobility and carrier concentration values are in agreement with data obtained by other researchers [1, 16].

The temperature dependence of the 2-point probe DC resistance of a single nanowire is shown in figure 5.d. The activation energy derived from the high temperature region was 30 meV (figure 5.d, inset).

B. I-DLTS. Trap characterisation

I-DLTS measurements were performed on four ZnO nanowires. Current transients at different temperatures for one nanowire are presented in figure 6.a. A transient drain current response to a gate voltage pulse similar to the one shown here was previously observed in ZnO nanowire FETs at room temperature in [26]. Authors attributed the current transients on a time-scale of seconds to adsorption and desorption of oxygen molecules. However, no temperature dependence was carried out. Here, the time-scales are much faster (micro- and milliseconds) and the temperatures are lower. We therefore assume that the current transients in our measurements depend only on the charging and discharging of carrier traps in the nanowire and the model for the carrier emission given above may be applied for the analysis of this data.

We shall now consider the transients in figure 6.a. A short negative relaxation immediately after the end of the gate voltage pulse with a time constant of approximately 50 µsec is attributed to the equipment response and is similar among all the measured samples. The relaxation curves show the temperature-evolution of the current behaviour due to the deep trap. As expected from the exponential behaviour of the emission rate (equation 5), the emission rate increases with temperature.

I-DLTS spectra for ZnO nanowire No.1 are shown in figure 6.b. Peaks in this particular I-DLTS dependence may be attributed to two electron trap levels SE1 and SE2 and one hole-like trap level SH1. The activation energies and apparent capture cross sections of these traps can be determined from the Arrhenius plots (figure 6.b, inset). Parameters of the deep levels measured on four different nanowires are listed in table 1. The nanowires exhibit similar hole-like traps but different electron traps. The normalised amplitude of the traps $I_{DLTS}/I(T)$ is relatively large (reaching 0.5 for the level SE1 in nanowire No.1), which indicates a high density of surface traps. It is difficult, however, to accurately estimate the density of the particular traps SE1, SE2 and SH1 due to the unknown number of equilibrium surface traps $Q_{ss}$ in equation 1.

The levels observed in this work have several pronounced traits that are not expected from simple bulk deep traps. First, whereas the I-DLTS SH1 magnitude at different rate-windows stays constant at different temperatures, absolute values of the peak magnitudes attributed to the electron traps, SE1, SE2 and SE3, rapidly increase with temperature (figure 6.b shows levels SE1 and SE2). This rapid increase in I-DLTS peak magnitude was observed in various reports and was attributed to the surface states at the un-gated area of a FET [15, 27]. Since the nanowire FETs in the present work are back-gated, the larger part of the nanowire surface is exposed to air and this affects the I-DLTS signal through the nanowire surface states.
FIG. 6: a) Current transients of the nanowire at different temperatures for $\Delta V_G = 10$ V; the negative current peak at $t < 0.1$ msec is due to the equipment response; b) I-DLTS signal normalized to static current with deep levels indicated; inset: Arrhenius plots of levels SE1, SE2 and SH1 taken from the I-DLTS graphs in figure b).
TABLE I: Activation energies and apparent cross-section of trap levels derived from Arrhenius plots for four ZnO nanowires. For I-DLTS spectra and Arrhenius plots of all the nanowires see Supplementary Information II.

| Levels | Nanowire No. | Energy, eV | Cross-section cm$^2$ |
|--------|--------------|-----------|---------------------|
| SE1    | 1, 2         | 0.11      | $7 \times 10^{-21}$ |
| SE2    | 1, 2         | 0.15-0.2  | $4 \times 10^{-19}$ - $2 \times 10^{-18}$ |
| SE3*   | 1            | 0.25-0.3  | $(1-5) \times 10^{-18}$ |
| E4     | 4            | 0.45      | $3 \times 10^{-12}$ |
| SH1–SH3| 1, 2, 3, 4   | 0.10-0.20 | $2 \times 10^{-19}$ - $2 \times 10^{-18}$ |

* – Level SE3 can be seen only in spectra with emission rate windows larger than those shown in Figure 6.b or at higher temperatures (see Supplementary Information II).

In addition, we can compare the measured trap signatures with trap signatures of the levels studied in bulk ZnO. ZnO films, bulk crystals and microwires have been studied by capacitance-mode DLTS with various electron traps levels observed [28–33]. Although the energies of the levels SE1, SE2 and SE3 coincide with the energies of the levels E1, E2 and E3 from these reports, the trap cross-sections are several orders of magnitude lower in the present work. Level E4, however, coincides by both energy and cross-section with the level E4 from [28, 29, 33], where it is attributed to oxygen vacancies. This corroborates our assumption of the surface origin of the levels SE1, SE2 and SE3.

Levels SH1, SH2 and SH3 show very similar activation energies, temperature and amplitude behaviour, and can be examined together. Hole-like levels have been observed in some n-type FETs and are usually ascribed to the surface traps, in particular to hole-traps on the un-passivated surface of the FET ([23] and references therein). In the case of n-type ZnO nanowires, it is very unlikely for the levels SH1 to SH3 to be real hole traps, the reasons for that being as follows. For some ZnO nanowires, the amplitude of the current transient corresponding to the hole-like level is comparable to the static current through the nanowire ($I_{DLTS}(T_{max})/I(T_{max}) \approx 0.1 - 0.5$), which, assuming the hole-like level being real hole traps, would indicate concentration of holes comparable to that of electrons. On the contrary, no inversion current was observed in the FET transfer characteristics at large negative gate biases down to –60 V, indicating a negligible concentration of holes. Therefore, the levels SH1 to SH3 cannot be real hole traps. Further study is needed to fully understand the origin of the levels SH1 to SH3.

In conclusion, all the levels observed in ZnO nanowire transistors I-DLTS, except the E4 level, appear to be surface state related. We tentatively ascribe the E4 level to the oxygen vacancies in the nanowire core. This corroborates our initial assumption about ZnO nanowires being mostly affected by the surface states. Here, we cannot unambiguously determine the exact origin of the observed surface levels. Therefore we will restrict our discussion to the phenomenological description of the trap recharging characteristics.

C. I-DLTS. Surface barrier height measurement

As it was outlined in section 1A.3 capture mode I-DLTS may provide information on the nanowire surface barrier height. Any surface state that can trap electrons at positive gate voltages and de-trap electrons at negative gate voltages can be used for this purpose (equation 4). The surface barrier height depends on the effective gate voltage (figure 8b.2, equation 3), therefore temperature of the capture-mode I-DLTS peak will depend on the quiescent gate.
voltage value as well.

Capture-mode I-DLTS was carried out on the nanowire sample No.4 (figure 7). Figure 7a shows capture-mode I-DLTS spectra at two different quiescent voltages with the most prominent peaks at 220 K and 230 K. We assume that these two peaks correspond to the process of carrier capture over the surface barrier by the same surface trap level which we denote by C1. The surface barrier heights obtained from the I-DLTS measurements are 0.3 eV and 0.4 eV (for \( V_{GQ} = 10 \) V and \( V_{GQ} = 0 \) V respectively, see Supplementary Information II). This values of the surface band bending in ZnO nanowire are similar to those obtained by Soudi et al. [17] (0.3 eV) and Chen et al. [16] (0.74 eV).

According to the model in figure 8b.2, the level C1 exhibits a varying capture activation energy (and consequently, surface barrier height) which depends on the quiescent voltage. The surface barrier \( qV_B \) decreases by 0.1 eV (from 0.4 eV to 0.3 eV) when the quiescent voltage increases from 0 to +10 V (figure 7a). This value is on the same order of magnitude with that obtained from the model described in section IA 2, figure 2d. The capture cross-section \( \sigma_{ss} \) stays approximately the same and is equal to \( 5 \times 10^{-18} \text{ cm}^2 \).

Figure 7b shows more detailed quiescent voltage dependence of the I-DLTS signal magnitude, with fixed gate voltage pulse of \( \Delta V_G = -4 \) V. The peak increases with quiescent voltage. Since the capture follows an exponential time-dependence (figure 7b, inset), the capture time-constant can be inferred from the fit. It changes from 0.5 to 0.17 msec when the quiescent voltage increases from +4 to +10 V. The capture activation energy (or barrier energy \( E_b \)) is calculated using equation 4 for \( V_{GQ} > 4 \) V and plotted in figure 7b, blue squares. The barrier energy monotonically decreases from 325 to 300 meV as expected from the depletion region model.

We can estimate the surface charge concentration from the barrier height (equations 2 and 3). Assuming a carrier concentration of \( 10^{19} \text{ cm}^{-3} \), the surface charge density at zero gate bias is \( 3.5 \times 10^{12} \text{ cm}^{-2} \).

### III. CONCLUSIONS AND PROSPECTS

In conclusion, we have proposed and successfully implemented the I-DLTS method with gate-voltage pulsing to probe deep electronic states in individual ZnO nanowires. A variety of deep levels (SE1, SE2, SE3, E4, SH1, SH2 and SH3) were observed, with both electron-like and hole-like character. A comparison with the literature showed that levels SE1, SE2 and SE3 are most likely surface trap levels, whereas E4 is a bulk nanowire level related to oxygen vacancies. Different types of I-DLTS measurement setups (emission-mode, capture-mode and quiescent voltage dependence) were applied to the nanowire FETs. Surface barrier was established from the capture-mode I-DLTS to be 0.3–0.4 eV at 240 K.

The hole-like trap levels were discovered to affect all the nanowire FET transients. Their amplitude was found to depend on the quiescent voltage (and hence surface Fermi level). The origin of these levels is still in question.

Although the levels observed originate from the features of the ZnO nanowire FET and are most likely surface related defects, it is not clear yet whether these levels are intrinsic to ZnO nanowires, or whether they are ZnO-SiO\(_2\) or ZnO-contact interface levels.

In general, I-DLTS, especially with combination with other characterization methods, has the prospects to be widely applied to nanowire research. A variety of material systems can be studied by this method: I-DLTS can be used to study the effect of the metal catalyst atom incorporation into nanowires during growth; it may give information
FIG. 7: (a) Capture-mode I-DLTS measurement on a ZnO nanowire with different quiescent gate voltage: $V_{GQ} = +10$ V (red), $V_{GQ} = 0$ V (blue), emission rate constant $t_1/t_2$ was 0.4/0.8 msec. Hole-like peaks are observed at 220–240 K; (b) quiescent voltage dependence of the capture-mode I-DLTS signal and capture activation energy, gate voltage pulse is $-4$ V; inset: current transient at $V_{GQ} = 10$ V, $\Delta V_G = -4$ V, blue line shows the exponential fit to the experimental data.
on defect states that account for sensing properties in nanowires; and a more sophisticated analysis of the quiescent gate-voltage sweeping technique on wrap-gate FETs may give information on the spatial location of defect states in nanowires with non-uniform composition (such as axial and core-shell nanowires).

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Supporting Information

I. CURRENT THROUGH THE NANOWIRE FIELD EFFECT TRANSISTOR

Surface band bending determines the conductivity in a nanowire. For example, ZnO nanowires have a surface charge depletion layer due to a negative surface charge with the dominant conductivity happening in the core of the nanowire [16, 17]. InAs nanowires, on the other hand, have a surface electron accumulation layer which accounts for the main contribution to the conductivity [18]. A simple model for non-degenerate n-type semiconductor nanowires is given here. The effect of holes is omitted for clarity.

We assume the nanowire to have cylindrical symmetry, a uniform distribution of ionised shallow donors with concentration $N_d$ and uniform distribution of surface states. The charge on the nanowire surface is the sum of the negative surface state charge $Q_{ss}$ and the charge induced by the gate voltage, $Q_{surf} = Q_{ss} + C_{oxide}V_G$. Here $V_G$ is the gate voltage and the oxide capacitance $C_{oxide}$ for a back-gated nanowire FET is calculated based on the model of a metallic wire above a charged plane:

$$C_{oxide} = \frac{2\pi \varepsilon_0 \varepsilon_{SiO,eff} L}{\ln(d/R + \sqrt{(d/R)^2 - 1})}, \quad \text{(S1)}$$

where $L$ is the distance between contacts, $R$ the radius of the nanowire, $\varepsilon_{SiO,eff}$ is the effective relative permittivity of air and silicon oxide which can be taken to be equal 2.2 [34], and $d$ the oxide thickness.

The charge on the outer walls of the wire should be balanced by the nanowire charge $Q_{surf} = -Q_{NW}$. The nanowire charge is constituted of the positive charge of the ionised shallow donors with concentration $N_d$ and the negative charge of the free carriers $-qL \int_0^R n(r)2\pi r dr$, where $n(r)$ is the distribution of the free carrier density which depends on the conduction band profile in the nanowire. The charge in the nanowire is

$$Q_{NW} = -qL \int_0^R n(r)2\pi r dr + \frac{q\pi R^2 N_d L}{\varepsilon_{SiO,eff}}. \quad \text{(S2)}$$

Since $Q_{surf} = Q_{ss} + C_{oxide}V_G$, the charge of free carriers is equal to:

$$Q_{\text{free carriers}} = qL \int_0^R n(r)2\pi r dr = Q_{ss} + C_{oxide}V_G + \frac{q\pi R^2 N_d L}{\varepsilon_{SiO,eff}}. \quad \text{(S3)}$$

The equation for the drain-source current $I_{ds}$ through the nanowire may be derived from [19], assuming the drain-source voltage $V_{ds}$ is much smaller than the gate voltage and the surface barrier voltage:

$$I_{ds} = \frac{qV_{ds}}{L} \int_A \mu n \, dA =$$

$$= \frac{qV_{ds}}{L} \int_0^R \mu(r)n(r)2\pi r \, dr, \quad \text{(S4)}$$
where $\mu(r)$ is the mobility which depends on the position (the scattering will be different at the nanowire surface and in the nanowire core) and $A$ the nanowire cross-sectional area. Next, we introduce the effective carrier mobility $\mu_{\text{eff}}$ as:

$$\mu_{\text{eff}} = \frac{\int_0^R \mu(r)n(r)2\pi r \, dr}{\int_0^R n(r)2\pi r \, dr}.$$  \hspace{1cm} (S5)

Now the current through the nanowire becomes:

$$I_{ds} = \frac{V_{ds}\mu_{\text{eff}}}{L^2} Q_{\text{free carriers}}$$  \hspace{1cm} (S6)

Putting equations S3 and S6 together we get:

$$I_{ds} = \frac{V_{ds}\mu_{\text{eff}}}{L^2} \left( Q_{ss} + C_{\text{oxide}}V_G + q\pi R^2 N_d L \right),$$  \hspace{1cm} (S7)

or, equivalently,

$$I_{ds} = \frac{\mu_{\text{eff}} C_{\text{oxide}}}{L^2} \left[ V_G + V_T \right] V_{ds},$$  \hspace{1cm} (S8)

where $V_T = Q_{ss}/C_{\text{oxide}} + q\pi R^2 N_d L/C_{\text{oxide}}$ is the threshold voltage. Equation 1 coincides well with the usual transistor formula in the linear regime [19]. The usual expression of the threshold voltage does not contain surface charge [1] and is used to infer the concentration of ionised shallow donors $N_d$ in nanowires, which at high temperatures coincides with carrier concentration. The appearance of the term $Q_{ss}/C_{\text{oxide}}$ in the threshold voltage shows that the usual way of obtaining concentration of ionised shallow donors gives an incorrect result (either underestimating or overestimating the concentration depending on the sign of surface charges). The negative ($Q_{ss} < 0$) or positive ($Q_{ss} > 0$) surface charge will create surface depletion or accumulation layer respectively.

Figure 2 schematically depicts a standard ZnO nanowire with a surface depletion region due to negatively charged surface states which are attributed to oxygen adsorption. We will consider this ZnO nanowire in order to obtain a relation between the gate voltage and the nanowire surface barrier height.

Under applied gate bias, the surface charge becomes $Q_{\text{surf}} = Q_{ss} + C_{\text{oxide}}V_G = C_{\text{oxide}}V_{G,\text{eff}}$, where $V_{G,\text{eff}}$ is the effective gate voltage. The surface charge is balanced by the charge of ionised donors in the depletion region:

$$|Q_{\text{surf}}| = Q_{NW} = qN_d\pi W_d(2R - W_d)L,$$  \hspace{1cm} (S9)
where $W_d$ the depletion region width. The depletion region width therefore depends on the effective gate voltage:

$$ W_d/R = 1 - \sqrt{1 - \frac{C_{\text{oxide}}V_{G,\text{eff}}}{R^2qN_d\pi L}}, \quad (S10) $$

The charge of the depletion region may also be expressed as $Q_{NW} = C_{DR}V_B$, where $qV_B = E_b$ is the surface barrier height, $C_{DR}$ the depletion region capacitance. According to a simple cylindrical capacitor model:

$$ C_{DR} = \frac{2\pi\epsilon_0\epsilon_{ZnO}L}{\ln(R/(R-W_d))}, \quad (S11) $$

where $\epsilon_{ZnO}$ is the dielectric constant of ZnO. The barrier height can be found from combining equations $S9$ and $S11$:

$$ V_B = \frac{qN_dW_d(2R-W_d)\ln(R/(R-W_d))}{2\epsilon_0\epsilon_{ZnO}}, \quad (S12) $$

Combination of equations $S10$ and $S12$ gives the relationship between the nanowire surface barrier height $V_B$ and the effective gate voltage $V_{B,\text{eff}}$.

II. I-DLTS SPECTRA OF ALL THE NANOWIRES AND ARRHENIUS PLOTS
FIG. 1: (a) Combined I-DLTS spectra taken on the four nanowires with the same emission rate window. Deep electron and hole-like levels indicated. (b) Combined Arrhenius plots of all the levels measured in this work.
FIG. 2: Arrhenius plots of the peaks measured during capture mode I-DLTS for barrier height calculation.