A heterogeneous many-core platform for experiments on scalable custom interconnects and management of fault and critical events, applied to many-process applications: Vol. II, 2012 technical report

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We acknowledge the cooperation with all the members of the project. The expected project duration is January 2010 — September 2014; during the period 2010-2012 the full EURETILE team was composed by:

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Abstract

This is the second of a planned collection of four yearly volumes describing the deployment of a heterogeneous many-core platform for experiments on scalable custom interconnects and management of fault and critical events, applied to many-process applications. This volume covers several topics, among which: 1- a system for awareness of faults and critical events (named LO|FA|MO) on experimental heterogeneous many-core hardware platforms; 2- the integration and test of the experimental hardware heterogeneous many-core platform QUoNG, based on the APEnet+ custom interconnect; 3- the design of a Software-Programmable Distributed Network Processor architecture (DNP) using ASIP technology; 4- the initial stages of design of a new DNP generation onto a 28nm FPGA. These developments were performed in the framework of the EURETILE European Project under the Grant Agreement no. 247846.
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6 Glossary

1 Introduction

1.1 Project abstract

EURETILE investigates and implements brain-inspired and fault-tolerant foundational innovations to the system architecture of massively parallel tiled computer architectures and the corresponding programming paradigm.

The execution targets are either a many-tile HW platform and a many-tile simulator. A set of SW process - HW tile mapping candidates is generated by the holistic SW toolchain using a combination of analytic and bio-inspired methods. The Hardware dependent Software is then generated, providing OS services with maximum efficiency/minimal overhead. The many-tile simulator collects profiling data, closing the loop of the SW tool chain.

Fine-grain parallelism inside processes is exploited by optimized intra-tile compilation techniques, but the project focus is above the level of the elementary tile. The elementary HW tile is a multi-processor, which includes a fault tolerant Distributed Network Processor (for inter-tile communication) and ASIP accelerators.

Furthermore, EURETILE investigates and implements the innovations for equipping the elementary HW tile with high-bandwidth, low-latency brain-like inter-tile communication emulating 3 levels of connection hierarchy — namely neural columns, cortical areas and cortex — and develops a dedicated cortical simulation benchmark: DPSNN-STDP (Distributed Polychronous Spiking Neural Net with synaptic Spiking Time Dependent Plasticity). EURETILE leverages on the multi-tile HW paradigm and SW toolchain developed by the FET-ACA SHAPES Integrated Project (2006-2009).

For an overview of the full project scope and its activities during the first three years, see the EURETILE 2010-2012 summary.[1]

1.2 Roles of the project partners

The APE Parallel Computing Lab of INFN Roma is in charge of the EURETILE HW Design (QUonG system [2]/APEnet+ board [3,4]/DNP (Distributed Network Processor [5]) and Scientific Application Benchmarks.

The Computer Engineering and Networks Laboratory (TIK) of ETH Zurich (Swiss Federal Institute of Technology) designs the high-level explicit parallel programming and automatic mapping tool (DOL/DAL) and a set of "Embedded Systems" benchmarks.

The Software for Systems on Silicon (SSS) of the ISS institute of RWTH Aachen, investigates and provides the parallel simulation technology and scalable simulation-based profiling/debugging support.

The TIMA Laboratory of the University Joseph Fourier in Grenoble explores and deploys the HdS (Hardware dependent Software) including the distributed OS architecture.
TARGET Compiler Technologies, the Belgian leading provider of retargetable software tools and compilers for the design, programming, and verification of application-specific processors (ASIPs), is in charge of the HW/SW Co-design tools for custom components of the EURETILE architecture.

1.3 Structure of this document

This publication is a derivative of the project deliverable document D6.2 and it is the second of a planned collection of four yearly volumes reporting the disclosable activities of Workpackage 6 (WP6) which is dedicated to the deployment of a heterogeneous many-core platform for experiments on scalable custom interconnects and management of fault and critical events, applied to many-process applications. All project deliverable documents have been peer-reviewed by a committee of four experts of the field.

The 2012 activities of WP6: Second Report on Innovations on HW Intellectual Properties planned to achieve multiple goals in the areas of fault tolerance, experimental HPC Platform integration and design of programmable DNP.

Fault tolerance issues focused on the implementation of the LO|FA|MO approach to fault awareness on the HPC experimental platform. The activity, reported in chapter 2 (see also [6]), delivered a consolidated specification of the LO|FA|MO architecture, the preliminary integration of the VHDL code of DNP Fault Manager, the introduction of a controller of the diagnostic messages flow over the 3D Torus Network (the Link Fault Manager, LiFaMa), and a first implementation of the Host Fault Manager as a Linux daemon.

The HPC platform integration and test activity (detailed in chapter 3) provided the mass production of the APEnet+ boards and their integration in a 16 nodes, 16 Kcores, 32 TFlops QUonG system, selected as the EURETILE HPC experimental hardware platform. Extensive test sessions, based on synthetic benchmarks and scientific application kernels, validated the architecture and provided measurements of scalability and global performance analysis. Furthermore, software development activities were devoted to the support of the HW innovations and of the complete EURETILE toolchain on the IP (APEnet+) aiming to achieve the best performances and usability for the hardware platform. Lastly, several exploitation initiatives were launched in the area of high-level trigger systems of the current and future High Energy Physics colliders.

In chapter 4 we report on one activity related to the design of ASIPs in the EURETILE platform. This activity, jointly carried out by INFN and TARGET, was the design of a software-programmable DNP architecture using ASIP technology trying to overcome the current latency limitations of the communication structure in the HPC platform.

Finally, chapter 5 details the preliminary exploration of the achievable performance of the last generation 28nm high-end FPGA. Understanding the real capabilities of such components in our system is the key point to plan future developments and designs. Preliminary porting of the DNP IP on the ALTERA Stratix V development kit allowed to measure the target torus link speed, micro-controller top frequency and hardware resources occupation.
2 Awareness of faults and critical events on the Experimental HW Platform

Fault-tolerance issues have been addressed in EURETILE since 2011 with the LO|FA|MO HW/SW approach [6], whose principles were presented in D6.1 [7] have been applied in the DNP SystemC model and lately demonstrated over the VEP simulator at the 2012 review meeting (see D5.2 [8]). This section describes the implementation of LO|FA|MO on QUonG, the EURETILE HW Platform, introduced by a complete and consolidated specification of the LO|FA|MO approach.

2.1 Consolidated Specification

2.1.1 Introduction

Features like resilience, power consumption, and system availability strongly depend both on the complexity of individual components (e.g. the gate count of each chip) and the number of components in the system. HPC systems in the peta/hexa-scale especially require techniques that aim to maintain a low Failure In Time (FIT) ratio to guarantee reasonable functionality. A first step is the adoption of hardware design techniques which improve the individual components to reduce their FIT. This design trend is already clear in the transition between past tera-scale systems, adopting commodity processors with 0.1÷ 0.5 fails per year per socket, to peta-scale systems, where the failure rate could be reduced to 0.001 fails per year per socket [9] adopting hardware design techniques like memory and bus encoding, memory scrubbing, provision of spare processors and memories. Even considering those reduced FIT rates and a very limited number of components, mission critical/life support systems mandate for architectures adopting double or triple redundancy. In practice, petaFLOPS designs based on resilient sockets adopting such countermeasures are characterized by a rate of system-stopping features in the range of a few days, while a system failure rate in the range of few hours is displayed by systems mounting less resilient sockets. [10]. Without additional measures, the FIT rate of exa-scale systems becomes unacceptable due to the scaling in the number of components. Analogously, for what regards power and thermal issues, each socket and component is nowadays designed keeping the energetic concerns as key drivers but systemic countermeasures are required due to the numerosity of components. In our vision, a necessary feature on larger scale architectures is the detection and collation of relevant information about faults and critical events and, due to the distributed nature of the system, the reliable propagation of this awareness up through the system hierarchy. In other words, the system must be rendered fault-aware to be able to choose and enact the actual system fault response.

Based on these considerations, the EURETILE project starts bottom-up proposing a mechanism that creates a systemic awareness of fault and critical events, the LO|FA|MO design: a distributed, mutual watchdog paradigm which enables the management of faults and critical events in large scale systems. The LO|FA|MO design can complement a pro-active mitigation approach, i.e. the enforcing of preventive actions (e.g. preemptive process migration, dynamic clock frequency reduction for individual components, dynamic routing strategies, etc.) before the failure occurs, so as to avoid faults that can reasonably
be expected or minimize the impact of those that can not.

In this document, we will mainly focus on the requirements imposed by exa-scale systems \[11\], i.e. an assembly of tens or hundreds of thousands of processors, hundreds of I/O nodes and thousands of disks, and future many-tile sockets; however, similar techniques could be applied to large networks of independent, autonomous devices. Our approach should mitigate the performance penalty and productivity reduction due to work loss and failure recovery, obtainable using exclusively the conventional approach to fault-tolerance (checkpointing/failure/rollback), which is foreseen to be problematic \[9\]. With the assistance of some hardware components located in the DNP (Distributing Network Processor) - the core of our APEnet+- the LO|FA|MO design paradigm employs some 'watchdog' techniques for reciprocal fault diagnosis between the DNP itself and a companion 'host processing element' within a node or on nodes which are neighbouring in the APEnet+ mesh topology; moreover, it employs a number of best-effort heuristics for delivering the diagnostic data even in case of faulty or broken links along an auxiliary support network. This network is a possibly low-speed, but highly reliable, diagnostic-dedicated, independent one, which leans on its high-speed 3D toroidal companion mesh in the extreme case of its own failing. Once complemented with diagnostic facilities that monitor whatever metrics are deemed relevant to the prediction of faults (e.g. temperature and voltage/current probes, BER counters, etc.), LO|FA|MO is a keystone upon which a fault management system can draw inferences that drive its strategies and actions to keep the system up and running.

2.1.2 Terminology and global picture

First of all, from now on we will use fault as abbreviation for fault and critical event.

Then, we split the fault-tolerance problem in two major key areas: fault awareness and fault reactivity.

- **Fault awareness** is the capability of the system to assess its own health status, in order to acknowledge faults that have already appeared or to make guesses about those likely to occur. Going bottom-up, this 'introspection' can be reduced to two aspects:
  - **Local fault detection**, the capability of a device to perform a number of HW and SW tests to detect a condition of fault in itself or other contiguous devices.
  - **Systemic fault awareness**, the collation of diagnostics propagated throughout the whole network by the local detecting sub-systems to compose a global picture of the system's health.

- **Fault reactivity** is the range of initiatives that the system enacts, under the presumptions it can make when its own global health is known to it, to prevent a fault situation which is about to occur or to gracefully degrade its performance instead of bringing the whole system to a stop when the fault has occurred. Going top-down, this 'self-adjustment' can be reduced to two aspects:
  - **Systemic response**, the set of strategies that the system can choose to apply, following inferences that it can make from its own diagnostic self-image, to prevent and counter the faults.
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- **Local readjustment**, the set of readjustments that can be locally enacted to prevent and counter the faults, *e.g.* reduction in clock frequency, changes to the routing tables to bypass a faulty link, remapping the assignment of tasks to nodes, *etc.*.

It is clear that a complete design of a fault-tolerant architecture must give detailed specifications in each of the above-mentioned areas. On the other hand, the challenging part for the most interesting fault-tolerant features is the actual implementation, which cannot be detached from a low-level specification of the host architecture. For example, task migration capabilities are derived from process management features of the host operating system; application checkpointing is strictly bound to storage options available to the host node; protection from memory errors by ECC is a low-level addition to the host memory architecture, *etc.*.

Figure 1: The Network Processor of each leaf in the many-tile HW system is equipped with its own LO|FA|MO components. The local Fault Awareness is propagated towards the upper hierarchy levels, creating systemic Fault Awareness. Fault reactions could be autonomously initiated by sub-system controllers or could require a systemic response.

Our idea with LO|FA|MO is that of a fault-tolerant framework which is as host-agnostic as possible. By encapsulating as many features as can be accommodated independently from such host specifications in LO|FA|MO, we strive to achieve a clear separation of problems - with the hope this leads to easier solution - and a degree of design reuse. By saying this, we make clear from the start that LO|FA|MO, by
its very nature, has to be restricted to the side of fault-awareness. In a hierarchical system the LO|FA|MO approach is then integrated as shown in figure [1]. The local Fault Awareness is propagated towards the upper hierarchy levels, creating a Systemic Fault Awareness. The reactivity starts from a Systemic Response and follows the inverse path from the upper layers, that have a global picture of the system status, towards the lower ones, where actions are enacted to adjust the system components behaviour to the fault condition. The many-tiled structure also requires the blocks able to reach Fault Awareness to be distributed and the presence of paths to propagate the Awareness towards some centralized intelligence able to make decisions.

We give here a sketch of an architecture where LO|FA|MO is employed. We assume a computing mesh where every node is a combination of the hardware supporting LO|FA|MO, i.e. a DNP, mated to a host processing element; beyond the communication facilities provided by the DNP, the host exposes another communication interface towards an auxiliary 'service network' (more details in section 2.1.3.2).

Failures can generally be of commission and omission type: the former encompasses the case of failing elements performing their tasks in an incorrect or inconsistent way (e.g. corruption in node memory, corruption in transmitted messages, packet misrouting, etc.); the latter deals with the case of failing elements skipping their tasks altogether (e.g. node stops responding due to crash failure, power outage or burn-out, message passing does not progress due to link disconnection, etc.). The most general kind of faults are those where the behaviour of a faulty component is assumed to possibly be completely random as to its correctness; in literature, fault-tolerance to this kind of faults is defined Byzantine fault-tolerance [12]. Byzantine failures can be seen as undetectable commission failures or, where possible, as malicious activity by some agent which is trying to sabotage the network. This kind of failures is explicitly not covered here.

With this restriction, detectable commission failures signal either a component that is about to break or keeps on working wrong, while omission failures, when permanent, mostly stand for an already broken or disconnected component. In this picture, the LO|FA|MO design is charged of polling the supplied sources of diagnostic data; any inconsistent value, being it any value beyond a certain threshold or a timed-out update of a watchdog counter, is a failure to report. LO|FA|MO attempts then to push this report along the service network - which means, in emergency cases, leaning against the neighbouring DNP's - towards an upper layer Fault Supervisor. As per previous definitions, we remark that the only behaviours LO|FA|MO foresees for a failing component are two:

- **sick** - the component has a rate of detected commission failures beyond the compatibility threshold of normal operativity → this may need action;

- **failed** - the component has a permanent commission failure (it keeps on working wrong) or simply stops participating in the network, i.e. it has a permanent omission failure (it has broken) → this needs action.
2.1.3 LOFAMO specification

The Local Fault Monitor (LO|FA|MO) is the mechanism chosen to obtain the fault-awareness; it imple-
ments health self-tests for a number of hardware devices and takes care of propagating the deriving
information. Moreover, the devices are able to monitor other contiguous devices and communicate their
faulty status. Synthetically, each device is able to:

- check/elaborate/store/transmit its own status;
- monitor other contiguous devices.

In the EURETILE platform, the actors of the described mechanism are the DNP/APEnet+ and the host
sub-system (Intel for the QUonG platform, a RISC-like model for the Virtual EURETILE Platform). The
DNP is able to run self-tests on its own links and logic, as well as to retrieve information from its own
temperature and electrical sensors. All information pertaining to the sub-systems status is gathered by
the LO|FA|MO-appointed component inside the DNP itself and stored in the DNP Watchdog Register
(see section 2.1.3.3). A second register inside the DNP is dedicated to the surveillance of the health
status of the host, with LO|FA|MO performing periodic checks of the Host Watchdog Register. In
the event the host on one or more nearest neighbouring nodes were faulty, a third register, the Remote
Fault Descriptor Register, would end up containing information about the nature of the remote
fault. The self-test capabilities of the DNP links and logic allow mutual monitoring between nearest
neighbour DNP’s, all of them acting as watchdog for one another. The key points for this LO|FA|MO
implementation are:

- the presence of a HOST FAULT MANAGER (HFM), a software process running on the host that
  is aware of the host local status, is able to read/write the DNP internal registers and the DNP
  Watchdog Register and Host Watchdog Register and can send messages through the Service Network.
- the presence of a DNP FAULT MANAGER (DFM), a component residing on the DNP that is able to
  collect the information about the DNP health status, to read/write the DNP Watchdog Register
  and Host Watchdog Register and to send messages through the 3D Network.
- a 3D toroidal network connecting all the nodes, implemented by the DNPs
- a service network, connecting all the nodes, as a primary and redundant path to communicate di-
  agnostic messages (offloading the 3D network from services duties when it’s not strictly required).
- a Fault Supervisor, an high level software layer that can gather diagnostic information from all
  the system components, composing the global picture of the system status, and that can make
decision about how to react to faults.

Thanks to these key components, the LO|FA|MO mechanism allows the system to cope with faults and
critical events, also under the following peculiar circumstances:
The DNP breaks down, consequently the DNP does not respond to queries from the host - the host acknowledges the omission fault and signals it via the service network to the Fault Supervisor (this does not differ from the ordinary condition).

The host breaks down, consequently the host does not respond to queries from the DNP - although from that node the service network is inaccessible, the DNP has a last chance of relaying its reports along to its neighbours in the high-speed 3D mesh and from there, all receiving DNP's can relay the data to their own host and then on to the Fault Supervisor.

In the showstopping event of both host and DNP breaking down in a node, the system has a way to become aware of the situation: no more activity from the node means that all the neighbouring nodes in the 3D mesh become eventually aware of a permanent omission fault in one of their channels; as soon as reports of this fact reach the Fault Supervisor, this latter can infer the node has died and take relevant action.

Figure 2 illustrates the basic platform configuration detailing the position and the communication paths of the HOST FAULT MANAGER and the DNP FAULT MANAGER. Keeping to the definitions given above, the task of LO|FA|MO thus encloses the whole of Local fault detection and the interface to the Fault Awareness system.

2.1.3.1 Fault Supervisor
The Fault Supervisor is the generic term that encompasses the set of processes receiving the output of the LO|FA|MO machinery; its duty is to create systemic Fault Awareness and to issue appropriate systemic Fault Responses. For a small number of nodes, the Fault Supervisor could be implemented as a single software process running on an appointed 'master node' of the system; for larger systems, a process cloud residing on a subset of nodes participating in a hierarchy would certainly be more scalable. The Fault Supervisor is kept timely fed by the set of DNP FAULT MANAGER and HOST FAULT MANAGER, with periodic updates about their health. This supervisor is the 'systemic intelligence' that embodies the fault awareness for the system and drives its response; all information (or lack thereof, in case of omission failures from faulty nodes, which is information as well) is brought by the LO|FA|MO network to the Fault Supervisor system, so that it can choose any fault prediction, prevention and reaction strategy it deems feasible.

We don't give here a detailed specification for the Fault Supervisor; we acknowledge its presence - after all, it is the target of all communications from the LO|FA|MO components - and we briefly describe (see section 2.4) its implementation for the QUonG Platform for what regards the obtaining of the systemic Fault Awareness. A more detailed specification would require a discussion on the Fault Reactivity strategies and on how HW and SW interact to apply them, but at the moment this is out of the scope of this document.

2.1.3.2 Service Network
Besides APEnet+'s high speed 3D mesh, LO|FA|MO expects the system nodes to partake in a secondary, diagnostic-dedicated network fabric to which only the host has access. In ordinary conditions,
Figure 2: The basic EURETILE platform configuration showing the position and the communication paths of the HOST FAULT MANAGER and the DNP FAULT MANAGER in a LO|FA|MO implementation. The Host Watchdog Register stores info about Host Faults. The DNP Watchdog Register stores info about local or global faults of the networking system. The Host Remote Fault Descriptor Register contains information about the nature of remote host Faults.

the DNP relays the gathered diagnostic data to its host companion which, through this network, in turn relays them to the Fault Supervisor. In this way, the high speed network is unencumbered from dealing with the added traffic of the health status reports. We expect this service network to be a relatively inexpensive local interconnect. On the HPC market, Ethernet is a mature technology, mostly ubiquitous presence for any architecture we think to match the APEnet+ board with - e.g., our QUonG platform cluster node prototype is a Supermicro R board equipped with dual GbE. For this reason, the presence of such service network is regarded as a rather unconstraining addition on the HPC flavour of the EU-RETILE architecture. On many-tile embedded systems, represented in our case by the VEP platform, we maintain at this stage open the definition of the service network. We are positing that the bulk of diagnostic data does need neither high bandwidth nor extremely low latency. This means that performance concerns are not overtly constraining in the building of this service network and all effort can be instead put in pushing its reliability, by means of ruggedness of components (for the switches, routers, NICs, cabling, etc.) or some kind of redundancy; reliable Ethernet is a wide ranging subject with many possible approaches [13]. However, this diagnostic network is a system element itself subject to failure. So, the problem must be raised of how to deliver fault awareness data in presence of criticality of the service network itself or the DNP’s. First, we analyze the case of host and DNP not affected by simultaneous fail, then the case of simultaneous fail of the DNP and host on a tile. The hypothesis we put forward is that
the probability for a node of host and DNP simultaneously failing is smaller than their individual failure rate. This means that having the host and the DNP mutually cross-checking each other, LO|FA|MO has meaningful escape routes in both the scenarios: when the DNP breaks down or when the Host breaks down. If both the components are completely faulty a Systemic Awareness can be reached thanks to the fact that the neighbouring nodes in the 3D mesh can sense the non-operative status of the channels towards the faulty node and spread the information.

2.1.3.3 Watchdog implementation

One of the foundations of the LO|FA|MO design is the mutual watchdog mechanism, that for the EURETILE platform is implemented in the following way: the DNP acts as watchdog for the host, i.e. it periodically monitors the host status as reported in the Host Watchdog Register updated by the host itself; the host acts as watchdog for the DNP, i.e. it periodically monitors the DNP status as reported in the DNP Watchdog Register updated by the DNP itself. Although both the mentioned registers are located inside the DNP, they are written (updated) and validated by their ‘owner’ and read and invalidated by the other device. Validation/invalidation consists of setting the Valid Bit to 1 or 0, respectively. The update period is such that $T_{\text{write}} < T_{\text{read}}$, in this way is guaranteed that the reader always founds a valid status and viceversa, unless a destructive omission fault occurs that makes the writer unable to update its status register (see section 2.1.3.5).

Figure 3: The host and the DNP act as reciprocal watchdogs. Even if both the host and DNP WD Registers are located inside the DNP, they are periodically updated by their owner and invalidated by the other device.
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2.1.3.4 Faults, Fault detection and paths to local/global awareness
Table [1] shows for each kind of fault that we chose here to consider which component is responsible to detect the fault and how the LO|FA|MO mechanism allows to reach a local/global awareness. A description of each fault listed in table is reported here:

- **Link 'sick'**
  - **Fault Description**: the DNP link (physical link) malfunctions and introduces errors during the packet transmission.
  - **Fault Detection**: Errors are detected by the links logic using CRC: the sender DNP calculates the CRC word of the packet and puts such word into the packet footer; the receiving DNP calculates the CRC word by itself and checks the matching with the CRC word in the packet footer, in case it doesn't match exception bits are raised in the proper register.

- **Link broken**
  - **Fault Description**: the DNP link is broken, the packet can't be transmitted.
  - **Fault Detection**: the RX side of the linked DNP sends continuously, back along the cable and towards the TX side, information (called credits) about the space available in FIFO to receive the data transfer. In this way the TX logic can sense whether the cable is ok or not (credits not received and timeout reached).

- **Temperature, power, voltage over/under threshold**
  - **Fault Description**: the DNP temperature (or power, or voltage) is over (or under) the threshold values, contained in the registers and set on the basis of the values for a correct hardware operativity.
  - **Fault Detection**: the hardware provides sensors to monitor temperature, power consumption and voltage. The control logic that reads the sensors and checks if the values are within the limits is part of the DNP FAULT MANAGER.

- **Host side faults**
  - **Fault Description**: the Host is broken or a peripheral in tile is faulty.
  - **Fault Detection**: the DNP FAULT MANAGER is able to detect these situations on the basis of the watchdog mechanism.

2.1.3.5 LO|FA|MO registers
There are three key registers used by the LO|FA|MO components:

- **DNP Watchdog Register**. It contains information about:
  - the status of the local DNP
  - the status of the hosts on first neighbouring tiles;
### Fault class | Faulty Elem | Faults | Detector | Diagnostic info storage | Diagnostic path | info
--- | --- | --- | --- | --- | --- | ---
DNP side | Link | Link sick (CRC errs) | receiving Link self-test → receiving DFM | bits in DNP Watchdog Register | DFM → Host → Service Net |
| | | Link broken | DFM on both the receiving and transmitting side (if link logic still working), otherwise on a single side | | |
| DNP °C/W/V alert | | Temperature over/under threshold | Sensors → DFM | bits in DNP Watchdog Register | | |
| | | Power over/under threshold | | | | |
| | | Voltage over/under threshold | | | | |
| DNP logic | | DNP core sick | DFM | bits in DNP Watchdog Register | Host → Service Net |
| | | DNP core meltdown | Host (DFM misses to update DNP Watchdog Register) | bit in DNP Watchdog Register | |
| Host side | Host fault | Memory, Peripherals (…, Service Net) | Machine dependent but managed by the HFM | Spare room in Host Watchdog Register | DNP → 3D net → Neighbour DFM → Neighbour Host → Service Net |
| | | Bus or total Host breakdown | DFM (Host misses to update Host Watchdog Register) | bit in RISC watchdog register | | |

Table 1: A summary of how faults are detected (which component is responsible to detect them) and how the information is conveyed bottom-up to obtain the Global Fault Awareness. (Abbreviations: DFM = DNP Fault Manager; HFM= Host fault manager; Net = Network)

- **Host Watchdog Register.** It contains the local host status;
- **Remote Fault descriptor Register.** In case of one or more host(s) on first neighbour tiles...
are faulty, it contains information about the nature of the fault.

More registers can be used in the different implementations to control the behaviour of the various LO|FA|MO components.

### 2.1.3.6 Example

An example of how the LO|FA|MO approach is applied in case of Host Breakdown fault is shown by figures 4, 5, 6.

**Figure 4:** A - Implementing the LO|FA|MO approach on 8 Nodes connected through the DNPs (D) equipped with a DNP Fault Manager. Each Host (H) runs an Host Fault Manager which has access to the Service Network (S) to send diagnostic messages to the Host Fault Manager running on the Master Node.
Figure 5: B - If one of the hosts comes down, the DNP in the same tile is able to detect the fault thanks to the watchdog mechanism and it sends a diagnostic message to its first neighbouring DNPs via the 3D network.
Figure 6: C - As each host exchanges status information with his companion DNP in the watchdog mechanism, the Hosts first neighbours of the faulty Host become aware of the fault and can signal it to the Master node via Service Network.
2.1.4 LO|FA|MO on the QUonG platform

In the following we give details on how to specialize the LO|FA|MO mechanism over the QUonG platform peculiarities, i.e. each host is a x86_64 Linux based machine mounting an APEnet+ card.

- **Registers:**
  - **DNP Watchdog Register.** It has got 3 macro fields: the local part, containing informations about the status of the Local DNP; the remote part, which contains the status of the first neighbours hosts (thus it can be propagated by the local and well functioning node) in terms of faulty/non-faulty; the valid field, that states the aliveness of the local DNP and certifies the reported DNP status as up to date.
  - **Host Watchdog Register.** It has got 2 macro fields: the (local) host status and the valid field. The host status is specified for each meaningful host device or periphery like memory or (service) network. The valid field is used to state that the host is alive and the status contained in the other field up to date.
  - **Remote Fault Descriptor Registers.** One or more registers used to specify the nature of the fault occurred on remote host signaled as faulty in the global (remote) part of the DNP Watchdog Register.
  - **Temperature/Voltage/Power consumption thresholds registers.** Registers used to set the boundaries for normal, warning and alarm ranges for temperature, voltage and DNP/APEnet+ power consumption. The thresholds must be set coherently with the ranges of correct operativity of the board.
  - **Link Related Thresholds.** Other registers can be used to set the thresholds to define the correct behaviour ranges of the 3D channels, e.g. maximum number of hops, the threshold for the CRC errors/transferred bytes ratio, etc.
  - **LO|FA|MO timer register.** Used to set the watchdog write and read period on the DNP side. The DNP FAULT MANAGER uses this information to update the DNP Watchdog Register and read the Host Watchdog Register at the right pace.
  - **LO|FA|MO masks register.** Allows to control the behaviour of the DNP FAULT MANAGER, e.g. to mask or unmask the signaling of fault type.

- **DNP FAULT MANAGER (DFM):** it’s an hardware component within the DNP core of APEnet+; it can access the board sensors and link control logic, gathering information about the DNP status; it can as well access periodically the DNP registers to implement the mutual watchdog together with the host as defined in section 2.1.3.3. More details on VHDL implementation of the DNP Fault Manager for QUonG is reported in section 2.2.

- **HOST FAULT MANAGER (HFM):** it’s a software running on each host able to access the APEnet+ device through calls to its driver handles. It’s also able to test the host itself to check its health status and retrieve and collect information about faults that may affect the host and his peripherals. One or more hosts in the network are initially configured as Master Nodes and the HFM running on them is also responsible to collect the fault awareness information and store them. The initial
configuration of the HFMs must match the topology programmed in the DNP device. The HFM is also able to configure the behaviour of the DNP Local Fault Manager, by properly setting the LO|FA|MO mask register on the DNP. In case of fault (either DNP or host class), once the information reach the HFM or the master HFM, a mechanism of acknowledge is necessary to shutdown the alarms and avoid network (service network or 3D) congestion due to the diagnostic messages. The implementation of the HFM for QUonG is detailed in section 2.4.

| Register Name                                      | address (BAR5) | #reg (BAR5) | Description                      |
|----------------------------------------------------|----------------|-------------|----------------------------------|
| LO|FA|MO DNP local/global watchdog                       | 0x474         | 29                      | DNP Watchdog Register           |
| LO|FA|MO Host watchdog                                    | 0x478         | 30                      | Host Watchdog Register          |
| LO|FA|MO Remote Fault Descriptor +X                        | 0x44C         | 19                      | Remote fault descriptor         |
| LO|FA|MO Remote Fault Descriptor -X                        | 0x450         | 20                      | Remote fault descriptor         |
| LO|FA|MO Remote Fault Descriptor +Y                        | 0x454         | 21                      | Remote fault descriptor         |
| LO|FA|MO Remote Fault Descriptor -Y                        | 0x458         | 22                      | Remote fault descriptor         |
| LO|FA|MO Remote Fault Descriptor +Z                        | 0x45C         | 23                      | Remote fault descriptor         |
| LO|FA|MO Remote Fault Descriptor -Z                        | 0x460         | 24                      | Remote fault descriptor         |
| LO|FA|MO thresholds                                        | 0x46C         | 27                      | Boundaries for the normal, warning, alarm temperature ranges |
| LO|FA|MO timer                                             | 0x464         | 25                      | Set the watchdog R/W periods    |
| LO|FA|MO mask                                              | 0x468         | 26                      | Mask or unmask fault signaling  |

Table 2: APEnet+ registers meaningful for fault detection and awareness.

### 2.2 VHDL coding of DNP FAULT MANAGER

The DNP FAULT MANAGER is an hardware component within the DNP core. It mainly implements, together with the HOST FAULT MANAGER, the Mutual Watchdog mechanism. It communicates to the host the Neighbours Status, on-board sensors values, DNP Core self test results and Link Status, updating the DNP Watchdog Register (DWR). Moreover it collects information about the local host status, Host Memory and Service Network, reading the Host Watchdog Register (HWR) updated by the HOST FAULT MANAGER.

Furthermore in case of Service Network faults the DNP FAULT MANAGER can initialize Link Fault Manager (LiFaMa) transactions to communicate the fault status to the six neighbour nodes. This additional fault communication approach can be requested also when the Service Network is operating without reporting faults to exploit a redundancy of the critical status communication.

Referring to figure 7 the DNP FAULT MANAGER implements two additional elementary blocks:

- the R/W TIMER is a programmable timer to set the frequency of Host Watchdog Register reading process and DNP Watchdog Register writing process. Current implementation allows
to vary the interval between two consecutive operations from 1ms up to 65s depending on the accuracy required.

• the SENSOR HANDLER compares the measured Temperature, Voltage and Current values with programmable threshold stored in the Configuration Register (see table 5) and evaluates the health status of the board.

In order to transfer information about the local board and remote node status to the local host, the DNP FAULT MANAGER performs the following tasks:

• It collects RX LiFaMa messages containing the remote nodes status and it updates the Remote Fault Descriptor Register (see table 5).

• It collects information about the board local status (DNP core status, Sensor measured values, Local Link Status).

• It updates the DNP Watchdog Register at the frequency set in the R/W TIMER with the information stressed in table 3.

In order to communicate the local host and board status to the six neighbour nodes, the DNP FAULT MANAGER performs the following tasks:

• It evaluates the health status of the host verifying the regular updating of the Host Watchdog Register at the frequency set by the R/W TIMER (DNP FAULT MANAGER checks the valid bit status, see table 4).
### DNP Watchdog Register (DWR)

| # Bits | Bit Range | Field Name            | Protocol                                      |
|--------|-----------|-----------------------|-----------------------------------------------|
| 1      | 0         | Valid                 | 1=DWR content valid; 0=DWR content not valid |
| 1      | 1         | Z- Neighbours Status  | 1=fails; 0=healthy;                           |
| 1      | 2         | Z+ Neighbours Status  |                                               |
| 1      | 3         | Y- Neighbours Status  |                                               |
| 1      | 4         | Y+ Neighbours Status  |                                               |
| 1      | 5         | X- Neighbours Status  |                                               |
| 1      | 6         | X+ Neighbours Status  |                                               |
| 2      | 8 - 7     | DNP core Status       | 00=normal; 01=sick; 10=broken                 |
| 2      | 10 - 9    | Current Status        | 00=normal; 01=warning; 10=alarm               |
| 2      | 12 - 11   | Voltage Status        | 00=normal; 01=warning; 10=alarm               |
| 2      | 14 - 13   | Temperature Status    | 00=normal; 01=warning; 10=alarm               |
| 2      | 16 - 15   | Z- Link Status        | 00=normal; 01=sick; 10= broken                |
| 2      | 18 - 17   | Z+ Link Status        | 00=normal; 01=sick; 10= broken                |
| 2      | 20 - 19   | Y- Link Status        | 00=normal; 01=sick; 10= broken                |
| 2      | 22 - 21   | Y+ Link Status        | 00=normal; 01=sick; 10= broken                |
| 2      | 24 - 23   | X- Link Status        | 00=normal; 01=sick; 10= broken                |
| 2      | 26 - 25   | X+ Link Status        | 00=normal; 01=sick; 10= broken                |
| 4      | 30 - 27   | Spare                 |                                               |
| 1      | 31        | LiFaMa Busy           | 1=LiFaMa Busy; 0=LDM Sent; see table 6        |

Table 3: DNP watchdog register layout

- It collects the status of the Service Network, Memory and Peripheral reading Host Watchdog Register.
- It collects information about the board local status (DNP core status, Sensor measured values, Local Link Status).
- It initializes TX LiFaMa transfers to communicate the node local status to the six neighbour nodes.

#### 2.3 Link Fault Manager (LiFaMa)

As explained above the LO|FA|MO approach leverages on the redundancy of the fault communication mechanism. The first method expects that the host communicates the occurrence of faults through the Service Network. An additional fault communication mechanism is to exploit the 3D Torus Network to
host watchdog register (hwr)

| # bits | bit range   | field name | protocol                        |
|--------|-------------|------------|---------------------------------|
| 1      | 0           | valid      | 1=hwr content valid; 0=hwr content not valid |
| 2      | 2 - 1       | service net status | 00=normal; 01=sick; 10=broken; |
| 2      | 4 - 3       | memory status | 00=normal; 01=sick; 10=broken; |
| 2      | 6 - 5       | peripheral status | 00=normal; 01=sick; 10=broken; |
| 24     | 30 - 7      | spare      |                                 |
| 1      | 31          | send ldm   | see table 6                     |

Table 4: Host Watchdog Register layout

remote fault descriptor registers

| # bits | field name                                | description                        |
|--------|-------------------------------------------|------------------------------------|
| 32     | x+ neighbour node status                  | see table 6 for details            |
| 32     | x- neighbour node status                  | see table 6 for details            |
| 32     | y+ neighbour node status                  | see table 6 for details            |
| 32     | y- neighbour node status                  | see table 6 for details            |
| 32     | z+ neighbour node status                  | see table 6 for details            |
| 32     | z- neighbour node status                  | see table 6 for details            |

configuration registers

| # bits | field name            | description                                    |
|--------|-----------------------|------------------------------------------------|
| 32     | mask enable           | activate the dnp fault manager                 |
| 32     | sensor threshold      | set threshold for the sensor handler           |
| 32     | timer configuration   | set frequency of read/write operation          |
| 32     | emulation             | test the lo|fa|mo approach                                  |

Table 5: Remote Fault Descriptor and Configuration Registers of the DNP Fault Manager.

Transfer fault informations. The latter approach is necessary in case of fault of the host and/or of the Service Network and it guarantees a fast broadcast of critical status to the neighbour nodes.

The Link Fault Manager (LiFaMa) is an hardware component in charge of handle the Diagnostic Message Flow as shown in figure 8. As explained in section 3.1.1.1 the adopted transmission protocol provides the communication of the RX LINK FIFO status to avoid the FIFOs overflow: the LINK CTRL sends to the neighbour node a 128-bit word called Credit containing information about the status of its receiving FIFOs. In the same section we also motivate the requirement of stopping the data transmission to update the RX LINK FIFO status every C cycles. In order to avoid performance degradation, LiFaMa Diagnostic Message (see table 6) are embedded in the spare bits of the Credit without
adding protocol overhead.

In the current implementation LiFaMa performs two main tasks:

- On the transmit side it handles the reading process of the TX LiFaMa FIFO. It updates the LiFaMa Diagnostic Message only when the LINK CTRL completes sending a Credit containing the previous one. This protocol guarantees the integrity of fault communication.

- On the receive side it simply collects LiFaMa Diagnostic Message into the RX LiFaMa FIFO avoiding the overflow.

### 2.4 Host Fault Manager implementation

As described in section 2.1.3, the HOST FAULT MANAGER is the software component in the LO|FA|MO approach that is responsible to gather information about the health status of the host; that implements, together with the DNP FAULT MANAGER, the Watchdog mechanism described in section 2.1.3.3 and that creates a global awareness in case of fault thanks to diagnostic messages sent via a Service Network towards the Fault Supervisor.

On the QUonG platform the HFM implementation is characterized by the following features:

- it is a Linux daemon, \textit{i.e.} a program running in background and using system calls to interact with the OS;
LiFaMa Diagnostic Message (LDM)

| # Bits | Bit Range | Field Name            | Protocol                      |
|--------|-----------|-----------------------|-------------------------------|
| 2      | 1 - 0     | Service Network Status | 00=normal; 01=sick; 10=broken |
| 2      | 3 - 2     | Memory Status         | 00=normal; 01=sick; 10=broken |
| 2      | 5 - 4     | Peripheral Status     | 00=normal; 01=sick; 10=broken |
| 2      | 7 - 6     | DNP Core Status       | 00=normal; 01=sick; 10=broken |
| 2      | 9 - 8     | Current Status        | 00=normal; 01=sick; 10=broken |
| 2      | 11 - 10   | Voltage Status        | 00=normal; 01=sick; 10=broken |
| 2      | 13 - 12   | Temperature Status    | 00=normal; 01=sick; 10=broken |
| 2      | 15 - 14   | Z- Link Status        | 00=normal; 01=sick; 10=broken |
| 2      | 17 - 16   | Z+ Link Status        | 00=normal; 01=sick; 10=broken |
| 2      | 19 - 18   | Y- Link Status        | 00=normal; 01=sick; 10=broken |
| 2      | 21 - 20   | Y+ Link Status        | 00=normal; 01=sick; 10=broken |
| 2      | 23 - 22   | X- Link Status        | 00=normal; 01=sick; 10=broken |
| 2      | 25 - 24   | X+ Link Status        | 00=normal; 01=sick; 10=broken |
| 5      | 30 - 26   | Spare                 |                               |
| 1      | 31        | Valid                 |                               |

Table 6: LiFaMa Diagnostic Message Layout

- it spawns Pthreads to take care in parallel of the different duties as shown in figure 9;
- it uses sockets to communicate via Ethernet network (Service Network) to the HFM running on the Master node;
- it accesses the APEnet+ LO|FA|MO registers using the APEnet+ API.

For what regards the checking of the host and the Service Network status, the HFM can parse `/proc/*` files to check - for example - for memory errors (`/proc/meminfo`), Ethernet interface errors (`/proc/net/dev`), etc. A number of tools can be used to check for more host status parameters, e.g. temperature. All these techniques, together with the watchdog mechanism, allow to obtain awareness of the host Sick condition.

Moreover, each HFM instance is able to determine if the Service Network is completely cut off on the node it runs on: a HFM thread sends a UDP message (`snet_ping`) to the Master node every `SNET_MON_PING_TMOUT` seconds (3 for example, but it is configurable), if the Master node does not reply (`snet_pong`) it waits more `SNET_MON_PING_TMOUT` seconds and retries. If a `snet_pong` is not received by then, the Service Network is set as broken on that node, situation that is managed by the watchdog mechanism.
In case of complete breakout of the host the watchdog mechanism is alerted by the missing update of the Host Watchdog Register, and managed as described before.

To summarize, table 7 describes the work done by each thread in the HFM:

| Thread                  | Function                                                                                   |
|-------------------------|-------------------------------------------------------------------------------------------|
| host_wd_thread          | Gathers the Host status and writes the Host Watchdog Register                              |
| DNP_wd_thread           | Reads the DNP Watchdog Register and enqueues a diagnostic message in case of faulty DNP   |
| snet_monitor_thread     | Continuously pings the master to check for the snet status.                                |
| snet_master_thread      | Receives the pings from the nodes and replies with a pong; receives and manages diagnostic messages. |
| snet_fault_notifier_thread | Sends diagnostic messages to the Master node.                          |

Table 7: HFM Pthreads and their function.

Note that the HFM does not make decisions about how to react to faults and it does not have the big picture of the system status, but as part of the LO|FA|MO approach, it is a means to spread information about faults and critical events and make the software high level layers (like DAL) to obtain systemic fault awareness.

Every time the HFM is launched — typically at the platform start up — the main() function initializes the LO|FA|MO mechanism on the basis of a configuration file. The initialization procedure requires the following steps:

- acquire the system topology and wait for the links to be aligned;
- set DFM masks and thresholds;
- set watchdog timers;
- enable DFM;

The LO|FA|MO registers mapping for APEnet+/QUonG is reported in table 2.
Figure 9: Structure of the HFM daemon running on different nodes, where one is the Master node. Each bubble is a Pthread.
3 Experimental HW Platform Integration and Test

During the 2012 the HPC platform integration and test activity provided the massive production of the APEnet+ boards, their integration to the full QUonG [2] tower and the validation of the system through synthetic benchmarks.

In this year we implemented architectural improvement of APEnet+ with the aim of achieving the best performances and usability for the hardware platform (sections 3.1.1.2, 3.1.1.3 and 3.1.1.1). Furthermore, we developed the VHDL coding of the DNP Fault Manager required to interface to the APEnet+’s sensors and to transfer the information to the DNP status registers (section 3.1.1.4).

The software development consisted in the implementation of the necessary support to the hardware innovations as well as a continuous tuning to reduce the latency due to the driver itself (section 3.1.2). Besides the fundamental middleware needed to implement a working API for communication with the board, a large number of small test codes (mostly in C supplemented by scripts in Bash/TCSH) were written (section 3.1.2).

3.1 APEnet+

The APEnet+ network architecture [14, 3, 4] has, at its core, the Distributed Network Processor (DNP) [5]. This acts as an off-loading network engine for the computing node, performing inter-node data transfers. The DNP hardware blocks structure, depicted in figure 10 is split into a Network interface (the packet injection/processing logic comprising host interface, TX/RX logic and Microcontroller), a Router component and six Torus Links.

The network interface block has basically two main tasks: on the transmit data path, it gathers data coming in from the PCIe port - either from host or GPU memory - and forwards them to the relevant destination ports; on the receiving side, it provides hardware support for the Remote Direct Memory Access (RDMA) protocol, allowing remote data transfer over the network without involvement of the CPU of the remote node.

The router establishes dynamic links among the ports of the DNP, managing conflicts on shared resources.

The torus link block manages the data flow and allows point-to-point, full-duplex connection of each node with its 6 neighbours with coordinates both increasing and decreasing along the X, Y and Z axes, forming a 3D torus.

3.1.1 Architectural Improvements

3.1.1.1 Link Bandwidth and Latency

In this section we show the performance achieved with the current implementation of the TORUS LINK...
Figure 10: Overview of APEnet+. The DNP is the core of the architecture - composed by the Torus Links, Router and Network Interface macro blocks - implemented on the FPGA. The system interfaces to the host CPU through the PCIe bus.

and we will argue the results of the tests, analyzing the limits being reached and providing a set of possible changes to overcome them.

Referring to the Open Systems Interconnection (OSI) model, the TORUS LINK plays the dual role of the Physical Layer and Data Link Layer.

The Physical Layer is constituted by Altera transceivers of the Stratix IV, able to reach 8.5 Gbps per line (each link is formed by 4 lines for a total of 34 Gbps). Dynamic reconfiguration of Physical Medium Attachment’s analog settings are guaranteed by Reconfig Block. We have performed various trials to increase the operating frequency of transceivers, minimizing the noise level of the channel. At present transceivers operate at a frequency of 350 MHz (28 Gbps) to maximize the reliability of data transmissions. The Altera transceiver ensures DC-balancing on the serial data transmitted exploiting the 8B10B...
encoder. In addition it implements a Word Aligner Block to restore the word boundary lost during the operation of serialization and deserialization and a Byte Ordering Block. Finally the bonding of four independent lanes on a single a channel is gained with four DESKEW FIFOs.

The Data Link Layer is constituted by LINK CTRL. It manages the data flow by encapsulating packets into a light, low-level, word-stuffing protocol able to detect transmission errors via CRC.

Figure 11: TORUS LINK Overview. $L_R$ and $L_L$ are the latency observed during a data-transaction between two neighbour nodes.

As shown in figure 12 measurements of bandwidth were taken by varying the frequency of the transceivers to evaluate the performance of the existing implementation of the LINK CTRL.

In order to have a thorough evaluation of the present deployment of LINK CTRL, it must be taken into account that 8B10B encoder causes a loss of 20% for bandwidth. Then the maximum achievable link bandwidth ($BW_L^{MAX}$) at the four different operating frequency is 3.4 GB/s, 2.8 GB/s, 2.4 GB/s and 2.0 GB/s. Our plots show an Efficiency Factor $E_{TOT}$ of approximately 60% of the theoretical maximum bandwidth, due to the implemented protocol regardless of the set frequency.

A deeper analysis of the adopted transmission protocol can help to understand the reasons for the performance degradation. The typical APEnet+ data packet is formed by 1 Header, 1 Footer (two 16-byte words) and a Payload of maximum size equal to 4096 bytes. The LINK CTRL adds two additional 16-byte words (Magic and Start) to initiate a new data transaction. Then 64 bytes of protocol ($P$) are necessary for each data packet. By focusing on maximum data packet size ($S_{MAX}$) we can define a Efficiency Factor $E_1$ equal to:

$$E_1 = \frac{S_{MAX}}{P + S_{MAX}} = \frac{4096}{64 + 4096} = 0.985$$
Figure 12: APEnet+ Link Bandwidth. The curves were obtained by setting the frequency of transceivers respectively at 425 MHz (34Gbps), 350 MHz (28 Gbps), 300 MHz (24 Gbps) and 250 MHz (20 Gbps). The Link Bandwidth $BW_L$ overlaps the Host Read Bandwidth $BW_{READ}$ until message size of 8KB-32KB, depending of the operating frequency of the transceivers.

The LINK CTRL is responsible for managing the data flow between two neighboring nodes preventing the FIFO overflow. The LINK CTRL keeps track of how many 16-byte data words have been sent. When it reaches the values set in a programmable threshold ($T_{RED}$) the data transmission is interrupted. The LINK CTRL ensures that the receiving FIFOs (RX LINK FIFO) have been emptied at least up to value $T_{YELLOW}$, yet programmable and with the constraint $T_{YELLOW} < T_{RED}$. The information about the status of RX LINK FIFO (how many words are placed into the receiving FIFOs) is contained in 16-byte word called Credit. Referring to figure [12] it is possible to estimate the data-interruption cycles. LINK CTRL is able to measure the flight time of a 16-byte word over the Physical Layer (Remote Latency):

$$L_R = 35 \text{ cycles}$$

The LINK CTRL has to wait for the flight time of the last sent data and of Credit containing the actual status of RX LINK FIFO before resuming data transmission. Furthermore, we must consider the time needed to transfer the occupancy information from the RX LINK FIFO to the LINK CTRL of the receiv-
ing node and from the RX CTRL to the TX CTRL of the transmitting node. The receiving side of a LINK CTRL clock is reconstructed from the incoming data (Clock Data Recovery) while on the transmitting side the clock is locally generated by PLLs. A synchronization is essential to exchange data between receiving and transmitting side (Local Latency):

\[ L_L = 20 \text{ cycles} \]

Then the Total Latency of the updated status of FIFOs is:

\[ L_T = 2 \times L_R + 2 \times L_L = 110 \text{ cycles} \]

Unfortunately waiting for \( L_T \) cycles is not enough. Indeed, the TX CTRL of the receiving node might be busy in transferring data packets. Since the maximum packet size is 4096 bytes and for each cycle a 16-byte word will be transmitted, the transmitter could be committed over 256 cycles. To avoid this latency addiction TX CTRL sends a Credit every \( C \) cycles. The transmission protocol requires the submission of a 16-byte word (Magic) every time that a Credit is submitted, to distinguish it from the Payload (Word-Stuffing Protocol). Therefore, this mechanism introduces a new factor of efficiency:

\[ E_2 = \frac{C}{C+2} \]

At this point we can define the \( W \) cycles of transmission interruption to get a Credit containing the updated status of the RX LINK FIFO. In the worst case the receiving node takes \( C \) cycles to submit the proper Credit so the interruption at the transmitting node is:

\[ W = L_T + C \]

When the value contained in the Credit is less than \( T_{YELLOW} \) the TX CTRL resumes data transmission.

In case of normal data traffic (in a test this means just one transmitting node and one receiving node, with data coming from a single channel and the other channels in idle) writing and reading speed of the RX LINK FIFO are basically equal. Thus the first Credit that arrives to the transmitter should contain a value below the \( T_{YELLOW} \), and with good approximation we can say that the RX LINK FIFO are empty and the transmitting node can resume data transmission. Summarizing, the transmitting node is able to send words for \( T_{RED} \) cycles continuously and stops for \( W \) cycles waiting for the Credit before resuming the transmission and so on, with an additional Efficiency Factor:

\[ E_3 = \frac{T_{RED}}{T_{RED} + W} \]

We can then define the Total Efficiency Factor:
\[ E_T = E_1 \times E_2 \times E_3 \]

\( T_{RED} \) is set to 506 (to maintain a margin of safety in writing \texttt{RX LINK FIFO}) and thus we define \( E_T \) as a function of the only variable \( C \):

\[ E_T = 0.985 \times \frac{C}{C + 2} \times \frac{506}{616 + C} \]

Maximizing this function for \( C \) in the range \( C \in [0; 55] \), we obtain:

\[ C = 35.1 \]

Then setting \( C = 35 \) and substituting in formulas for \( E_2, E_3, E_T \)

\[ E_2 = \frac{C}{C + 2} = 0.946 \]

\[ E_3 = \frac{T_{RED}}{T_{RED} + W} = 0.777 \]

\[ E_T = E_1 \times E_2 \times E_3 = 0.724 \]

Therefore with the current settings, we expect a bandwidth equal to 72.4\% of the theoretical maximum and instead we observe a plateau at 60\% regardless of the set frequency. This additional loss is due to the routing algorithm adopted. We must take into account that no transaction starts if the receiving module does not have sufficient space to accommodate the entire message. The information contained in the \texttt{Credit} is available for the \texttt{ROUTER}. The \texttt{ROUTER} does not instantiate a new transaction if there is not enough space in the \texttt{RX LINK FIFO} to accommodate the whole data-packet. Once that the sending of a data packet is complete the \texttt{FLOW CTRL} underestimates the space available in the remote FIFO until receiving a \texttt{Credit}:

\[ \text{SPACE IN FIFO} = T_{RED} - S_{MAX} = 250 < 256 \]

Then the \texttt{ROUTER} does not allow sending a packet with payload of 4KB before the arrival of a \texttt{Credit} that updates the status of the \texttt{RX LINK FIFO}. This changes the efficiency factor \( E_3 \). After sending every packet, \texttt{TX CTRL} waits for \( W \) cycles:

\[ E_3 = \frac{S_{MAX}}{S_{MAX} + W} = 0.638 \]

With this correction the Total Efficiency Factor is in line with the observed data:
Figure 13: A comparison between the results obtained in a point-to-point bandwidth test and the theoretical bandwidth calculated considering the Total Efficiency Factor $E_T$.

Observing figure 12 we note that if the host read bandwidth ($BW_H$) is less than the link maximum bandwidth $BW_{LMAX}$ then the $BW_L = BW_H$. With this arrangement it is possible to estimate the bandwidth as a function of message size with good results, as shown in figure 13.

It is straight-forward that to improve the LINK CTRL performance you need to increase the Total Efficiency Factor $E_T$.

$E_1$ and $E_2$ are closely related to the transmission protocol and the hardware implementation of the transceiver. Modifying these factors leads to a major re-write of the hardware code. The factor $E_1$ could benefit from a different choice for the transmission protocol but would involve a re-write of the LINK CTRL state machine. $E_2$ is related to the latency of transceivers due to DC-balancing, alignment and bonding of the channels. In addition, the current values are acceptable considering that together they result in a loss of 7% of performance.

As mentioned earlier, $E_3$ is related to the latency of the channel and to the programmable threshold
$T_{\text{RED}}$. With currently set value (506) is not possible to allocate two packets of maximum size (4KB) at the same time inside the receiving FIFOs. The only condition that would make it possible is to set the programmable threshold equal to the depth of RX LINK FIFO ($T_{\text{RED}} = \text{FIFO\_DEPTH}$). This choice is not safe in case of transfers between remote nodes. A minimum misalignment (due to jitter, noise, synchronization of signal at different clock frequency) could result in the overflow of the receiving FIFOs with consequent loss of transmitted data. Thus the most straight way to increase $T_{\text{RED}}$ is to increase the depth of the RX LINK FIFO, then change $E_3$, resulting in improved performance, without any major changes to the hardware code. Table 8 and figure 14 show the benefits that would be obtained by changing the depth of the FIFOs, at the attained clock frequency 350MHz (28Gbps) and at 425MHz (34Gbps), which is the maximum frequency that can be achieved by Altera Stratix IV GX transceivers.

| FIFO DEPTH | $E_3$  | $E_T$  | $BW_{\text{MAX}}$ @28Gbps | $BW_{\text{MAX}}$ @34Gbps |
|------------|--------|--------|-----------------------------|-----------------------------|
| 512        | 0.638  | 0.595  | 1666 MB/s                   | 2023 MB/s                   |
| 1024       | 0.841  | 0.784  | 2195 MB/s                   | 2665 MB/s                   |
| 2048       | 0.925  | 0.862  | 2414 MB/s                   | 2931 MB/s                   |
| 4096       | 0.964  | 0.898  | 2514 MB/s                   | 3060 MB/s                   |

Table 8: Efficiency Factor at varying the RX LINK FIFO depth.

Observing the values that could be obtained at 425 MHz can be taken as immediate the choice to quadruple (or even make 8 times greater) the RX LINK FIFO. In this way the maximum link bandwidth becomes larger than host read bandwidth and the transmission protocol does not slow down the data transfer. Unfortunately we have to deal with the resources available on the Stratix IV. Increasing 4 (8) times the depth of the FIFOs implies that each FIFO occupies 32 KB (64 KB) compared to the current 8KB. It should also be noted that each of the 6 channels is equipped with two receiving data FIFOs to ensure a deadlock free routing (virtual-channel) for a total of 384 KB (768 KB). Whereas the Stratix IV provides (1.74 MB) of embedded memory it is necessary to limit the amount of memory to allocate for data transfer. For this reason, we have scheduled a new revision of the LINK CTRL in the near future with receiving data FIFOs 2 times larger (16 KB). This option seems to be the right balance between used resources and expected performance improvement.

Indeed, with these conditions it will be possible to achieve a maximum link bandwidth of 2650 MB/s, with a loss of ~5% compared to the host read bandwidth. This result can be achieved only setting the maximum operating frequency for the links (425 MHz). Currently the transceivers are considered stable at a frequency of 350 MHz. In the future we will try to optimize the operating frequency changing Equalization, Pre-Emphasis and DC Gain. However because of the noise of the cables, the coupling between connector and cable and especially the delicate coupling between daughter-card and board, it could not be possible to achieve the maximum frequency for all channels. This could lead to a further loss of performance (for example at 350 MHz the maximum achievable bandwidth is 2200 GB/s). Obviously, this obstacle can be easily circumvented by doubling the size of the FIFOs further (32 KB). During the next year, very demanding memory optimizations will be completed (RX processing accelerator) and we can assess more precisely the amount of available memory. Nevertheless, a further analysis factor $E_3$ leads to focus on another limitation that affects performance negatively. The LINK CTRL is forced to
interrupt the data transmission waiting for an update on the status of the remote FIFO to avoid overflow them. At a later stage it may be interesting to evaluate the possibility of modifying the LINK CTRL to avoid the interruption of data transmission. This change would result in a re-write of only a portion of the link code hardware: the one responsible of the data flow FLOW CTRL.

3.1.1.2 Tx Acceleration

On the transmit data path the DNP handles transfers from CPU/GPU through the PCIe port, forwarding the data stream to the TX FIFOs (figure 15).

Referring to figure 15, PCI read transactions (TX) are issued by command-packets, each one composed by four 128bit-words: Header, Footer, CMD0 and CMD1. The first two are the Header and the Footer of the data-packet that will be sent to the 3D network, while CMD0 and CMD1 are commands that contain information used respectively to program the data PCI DMA read and to communicate to the EVENT QUEUE DMA CTRL the completion of data reading (for more details see section 3.1.1.3).

Command-packets are written by the host in a Ring Buffer, which has a fixed size and is managed by two pointers: a Write Pointer and a Read Pointer. The Write Pointer is controlled by
the software main processor and it is written in the DNP register \( wr\_ptr \); on the contrary, the Read Pointer is managed by the MULTI_PKT_INST, and it is recorded in a read only register \( rd\_ptr \).

A difference between \( wr\_ptr \) and \( rd\_ptr \) informs the DNP of the presence of new command-packets to execute. In this case, the MULTI_PKT_INST programs a PCI DMA read transaction of \( N \) command-packets, starting from the address of the last received command-packet, where

\[
N = wr\_ptr - rd\_ptr
\]

As soon as PCI DMA read transaction ends, MULTI_PKT_INST computes the new Ring Buffer Read Pointer and updates the \( rd\_ptr \) register (this mechanism is explained in detail in D6.1 [7]).

In case of CPU TX transaction, Header and Footer are directly written in TX FIFO HD CPU, while CMD0 and CMD1 are pushed in FIFO CMD TX (figure 16).

Using size and address specified in the CMD0, TX DMA_CTRL is able to program the requested DMA to load the packet’s payload. In order to accelerate the data transfers, the DNP implements two separated
DMA channels (DMA0 and DMA1): it instantiates transactions on the PCIe bus switching from one channel to the other, reducing the latency between two consecutive data requests.

TX CPU FSM 0 and TX CPU FSM 1 pop commands from the FIFO CMD TX alternatingly; data received from channel DMA0 are written by RAM WRITE FSM 0 in the pages 0 and 2 of the DMA RAM, while RAM WRITE FSM 1 is in charge of pages 1 and 3.

At the end of the DMA RAM writing process, TX DMA CTRL analyzes the CMD1. In case of not dummy command (that is CMD1 bit 3 - 2="00"), the TX DMA CTRL communicates to the main processor that required operation has been executed through EVENT QUEUE DMA CTRL (see section 3.1.1.3); dummy CMD1 is simply dismissed. Finally RAM READ FSM recursively reads all written RAM pages and pushes the Payload in TX FIFO DATA CPU.

Figures 17 and 18 show waveforms of a simulation of two READ commands sent to APEnet+.

In the first case only one DMA is enabled, and the DMA RAM uses 2 pages; time elapsed between two consecutive DMA requests is very long (1152 ns) and the Payload of the second packet is written in TX FIFO HD CPU.

Figure 16: APEnet+’s CPU TX flow.
Figure 17: APEnet+'s CPU TX simulation with 1 DMA channel. Time elapsed between two consecutive DMA requests is very long (1152 ns) and the payload of the second packet is written in TX FIFO after 896 ns.
Figure 18: APEnet+'s CPU TX simulation with 2 DMA channels. The second request occurs only 40 ns after the first one, and the complete Payload of the second packet is available only 392 ns after the first packet Payload.
FIFO DATA CPU after 896 ns. In the second case the DMA 1 channel requests data after 40 ns despite of DMA 0, and the complete Payload of the second packet is available only 392 ns after the first one.

Figure 19 compares the read bandwidth measured using one or two DMA channel implementation, showing a bandwidth improvement of 40%.

Figure 19: Bandwidth with one or two DMA channels for HOST to HOST transactions.

Unlike host buffer transmission, which is completely handled by the kernel driver, GPU data transmission is delegated to APEnet+. In particular, the APEnet+ board is able to take part in the so-called PCIe peer-to-peer (P2P) transactions: it can target GPU memory by ordinary RDMA semantics with no CPU involvement and dispensing entirely with intermediate copies.

In case of GPU read transaction, command-packets are pushed into FIFO GPU CMD (figure 20). GPU_P2P_TX reads the FIFO GPU CMD and moves Header and Footer towards TX FIFO HD GPU and CMD0 in FIFO P2P TX to request data to the GPU. Finally it sends CMD1 to the EVENT QUEUE DMA CTRL to generate a completion.

The first version of GPU_P2P_TX (version V1) reads just one command-packet at a time, waiting for the
reception of the whole packet’s Payload from the GPU before accomplishing the following command-packet. The slow rate of read requests emitted by the GPU_P2P_TX towards the GPU and the additional latency of the GPU response cause poor performance.

In the last year we modified GPU_P2P_TX, implementing the packet-command multiple-read functionality, in order to collect a huge amount of data from the GPU memory, managing many APEnet+ packets simultaneously. For this purpose we implemented a pipelining system, which requires some additional features to manage flow of request to the GPU: a FIFO DATA GPU overflow control (GPU TX CHECK) and a request controller (GPU DATA REQUESTING). As in the previous version, WRITE TX FSM sends Header and Footer to TX FIFO HD GPU and CMD0 to the FIFO P2P TX. Differently GPU_P2P_TX (version V2) pushes the Header also in FIFO LEN QUEUE and CMD1 in FIFO CMD QUEUE (1 in figure 20).

The Nios II exploits the information contained in FIFO P2P TX(CMD0) to generate GPU data request: it fills FIFO GPU NIOS CMD with the necessary information to instantiate PCI transactions and FIFO GPU NIOS DATA with the messages for the GPU (2).
GPU DATA REQUESTING pops data from NIOS FIFO (3) and transmits the packet’s size to GPU TX CHECK (4); this block prevents FIFO DATA GPU overflow following the equation:

\[ W_{\text{REQ}} - W_{\text{WRT}} + W_{\text{NEW}} < W_{\text{FREE}} \]  

in which \( W_{\text{REQ}} \) is the number of words already requested to the GPU, \( W_{\text{WRT}} \) is the number of words already written in FIFO DATA GPU, \( W_{\text{NEW}} \) is the number of word to request and \( W_{\text{FREE}} \) is the free space in FIFO DATA GPU.

At the same time WRITE DATA FSM pops the length of the processing packet from the FIFO LEN QUEUE (as explained above this FIFO contains Header in GPU_P2P_TX) and sends it to the GPU DATA Cnt which monitors, by means of a data counter, the data writing process in FIFO DATA GPU (4b).

GPU TX CHECK is in charge of limiting the number of requests for the GPU; for this purpose it registers the number of sent requests (\( R_{\text{SENT}} \)) and served requests (\( R_{\text{DONE}} \)), and it compares their difference with a programmable value written in a dedicated register (\( R_{\text{MAX}} \)).

\[ R_{\text{SENT}} - R_{\text{DONE}} < R_{\text{MAX}} \]  

In case that inequalities (1) and (2) are true (the space in FIFO DATA GPU is enough to contain the entire Payload of the requested packet and the number of pending request is acceptable) GPU DATA CHECK asserts check_ok signal (5) and GPU DATA REQUESTING starts the transaction (6). The end of writing operation is asserted by Pkt_Sent signal (7), and WRITE DATA FSM starts sending CMD1 to EVENT QUEUE DMA CTRL to program the TX completion (8).

As already explained, GPU DATA REQUESTING reads the FIFO GPU NIOS CMD and programs fixed sized DMA write transaction (8 bytes) popping GPU command from FIFO GPU NIOS DATA, that contains the physical address of the requested data.

The calculation of this physical address is a demanding task for the Nios II, that reduces its performance and slows the whole system. For this reason we developed a new component inside GPU DATA REQUESTING: the ACCELERATOR (GPU_P2P_TX version V3).

This block, enabled by a Nios II special word that acts as template, produces a GPU command’s sequence exploiting the information contained in the template.

In this way GPU DATA REQUESTING is able to send one request per cycle to the GPU despite of many cycle required to Nios II. This improvement increases significantly the bandwidth of P2P GPU, from \( \sim 500 \text{ MB/s} \) to \( \sim 1600 \text{ MB/s} \) as shown in section 3.1.3.3.

3.1.1.3 Software Interface Accelerator (Event Queue)

The Completion Event Queues (CQs) is one of the main component of The Remote Direct Memory Access (RDMA) event-based protocol.
The APEnet+ communicates to the CPU the completion of each performed operation by generating an event, \textit{i.e.} writing in the \textit{Completion Event Queues}.

![Diagram of EVENT QUEUE DMA CTRL and typical completion flow.](image)

The \textit{EVENT QUEUE DMA CTRL} (see figure 21) is able to accelerate this communication via fast PCI write transfers.

Currently we define 5 types of event:

- \textbf{Channel 0 TX Event}: \texttt{TX BLOCK} completes the data read transfer from the host memory through DMA channel 0.
- \textbf{Channel 1 TX Event}: \texttt{TX BLOCK} completes the data read transfer from the host memory through DMA channel 1.
- \textbf{GPU TX Event}: \texttt{GPU_TX BLOCK} completes the data read transfer from the GPU memory through DMA channel 4.
- \textbf{RX Event}: \texttt{RX BLOCK} completes the data write transfer to the host/GPU memory through the DMA channel 6.
- \textbf{NIOS Event}: it can be used to accelerate communication between the CPUs in the host and the micro-controller in the FPGA on board (for future development).
The completion event consist of two 128-bit words. As shown in table 9 the Software Interface Protocol provides a well defined message for each event.

| Logic Block            | First Completion Word | Second Completion Word |
|------------------------|------------------------|-------------------------|
| TX BLOCK DMA0          | CMD1                   | TX0 MAGIC WORD          |
| TX BLOCK DMA1          | CMD1                   | TX1 MAGIC WORD          |
| GPU_TX BLOCK           | CMD1                   | GPUTHX MAGIC WORD       |
| RX BLOCK               | HEADER                 | RX MAGIC WORD           |
| Nios II                | NIOS CMD               | NIOS MAGIC WORD         |

| Word                  | MSB        | LSB                                |
|-----------------------|------------|------------------------------------|
| TX0 MAGIC WORD        | 11111111DAD0DAD0 | 11111111DAD0DAD0                  |
| TX1 MAGIC WORD        | 22222222DAD0DAD0 | 22222222DAD0DAD0                  |
| GPUTHX MAGIC WORD     | 00000000DAD0DAD0 | 00000000DAD0DAD0                  |
| RX MAGIC WORD         | PHYS. ADDRESS     | FOOTER(63 downto 0)               |
| NIOS MAGIC WORD       | 33333333DAD0DAD0  | 33333333DAD0DAD0                  |

| Field | Name | Description                                         |
|-------|------|-----------------------------------------------------|
| 1 - 0 | pad0 | spare bits                                          |
| 3 - 2 | tag  | COMP_EQ or COMP_NONE                                |
| 18 - 4| code | Nios II or hardware COMP                             |
| 20 - 19| port id| process id                                         |
| 31 - 21| pad2 | spare bits                                          |
| 63 - 32| data | in case of Nios II COMP contains message from the µC |
| 127 - 64| magic| TX queue entry address                              |

Table 9: A detailed view of the completion events.

Thus, once a Logic Block completes a PCI transfer, it writes the completion words in the corresponding FIFO. The EVENT QUEUE DMA CTRL Finite State Machine checks the FIFO Interface continuously. When anyone of the FIFOs contains the completion words, the EVENT QUEUE DMA CTRL instantiates a fixed size PCI write transfer (32 bytes). In this way the completion process adds just few overhead cycles to initialize the PCI transaction (about 10 cycles, 40 ns). Furthermore we reserved a DMA channel (DMA7) for EVENT QUEUE DMA CTRL then the completion process is totally parallelized to the process of the corresponding Logic Block. Summarizing the typical completion-flow is:

- Logic Blocks perform the entrusted tasks at the same time.
- One of the Logic Blocks completes its task and it writes the two words of completion in the corresponding EVENT QUEUE FIFO.
• The Logic Block continues performing its tasks while the EVENT QUEUE DMA CTRL instantiates a 32 bytes PCI write transfer through DMA7 to communicate the event completion.

In this way no latency is introduced with a relevant performance gain.

### 3.1.1.4 Logic for Sensors Interface

APEnet+ card carries a number of on-board sensors for power and temperature monitoring. They are organized in two groups, one for on board temperature, FPGA temperature and 12V power monitoring, the second group for all others on board voltages (i.e. 3.3V used by DDR3, 1.1V and 1.4V needed by Stratix transceivers, ...). The two groups have separated serial interface directly connected to Altera’s MAX2 CPLD (which is responsible for configuration and setting of all on board devices).

Temperature is monitored with IC Maxim MAX1619, which features an internal temperature sensor and a connection to an external temperature diode, which in our case is connected to Altera Stratix internal sensor. 12V voltage and current is sampled with a single IC Linear LTC4151. Both ICs are interfaced to the programmable configuration device through the same I2C line at different addresses.

Dedicated circuitry has been implemented to sample all others power rails, using two Linears LTC2418 – 8 lines differential analog to digital converters suited for sensing applications –. The ICs communicate with the programmable configuration device through a 4-wire digital protocol (SPI-like).

On the MAX2 device is implemented all the logic needed to gather and decode data from the sensors and to configure them at start up time, in particular I2C and SPI protocols. A number of internal 16-bit registers are used to store the data from sensors upon request. These registers are read and controlled from the main FPGA, through a 16-bit wide bus, and are memory mapped in the Altera Nios II embedded microprocessor address space through the Avalon bus. Hence, a configuration or a data read from a sensor is performed with a specific Nios II instruction in the system firmware.

### 3.1.2 Software Development

For what regards 2012, the objectives of the Software Development activities were the support to the HW innovations on the APEnet+ IP and to open the path towards the support of the EURETILE complete toolchain. A lot of effort is employed to achieve the best performances and usability for the hardware platform. The software layers have to match the same requisites. As a result the software development done during 2012 consisted in the implementation in the APEnet+ Kernel Driver of the necessary support to the new hardware blocks and features (TX accelerator, Event Queue, NIOS completion) as well as a continuous tuning to reduce the latency due to the driver itself, and the support to a newer version of the Linux Kernel (v3). To make easier the exploitation of the 3D network and the advantages that come, from the application point of view, from the use of the APEnet+ device, more standardized and user friendly APIs have been ported and developed, including an OpenMPI first implementation. To address the project objective of a final and complete integration between all the EURETILE HW and SW layers the development of a preliminary version of the DNA-OS driver for APEnet+ has been started together with TIMA.
The software stack for DNP/APEnet+ is outlined, for what regards communication, in figures 22 and 23. In the following paragraphs we describe the components of this stack relevant to highlight the work done during 2012. The RDMA API has been described in D2.1 and some more can be found in section 3.1.3.2.

Figure 22: Communication software stack for the APEnet+ card in the QUonG platform.

### 3.1.2.1 PCI Kernel Driver
All the RDMA primitives included in the RDMA API are actually implemented in a Linux kernel driver properly developed for APEnet+. The kernel driver is a run-time loadable dynamic object which abstracts the APEnet+ card as a simple character device, a simple abstraction of an I/O unformatted data stream. Most of the RDMA APIs are channeled towards the kernel driver through the IOCTL system call. The most complex APIs are those involving buffer registration, which is mandatory for receive buffers, involves memory-pinning and virtual-to-physical translation, and persists until an explicit buffer deregistration. Pinning and translation are also implicitly done for communication primitives, like RDMA PUT and GET. As memory pinning is a time-consuming operation, involving the manipulation (locking, traversal, etc.) of the data structures related to the OS memory management (MM) subsystem, we developed a Pin-Down Cache (PDC), a caching subsystem which keeps pinned memory areas in a proper data structure and delays the un-pinning to the closing (program tear-down) phase. The MM traversal related to pinning...
Figure 23: Communication software stack for the DNP (DNP SystemC model) in the Virtual EURETILE Platform.
of memory buffers is also used for the population of the virtual-to-physical (V2P) translation tables. The physical address of buffer memory is the address of that memory as it is seen from the peripheral bus, PCIe. As the concept of virtual/physical addressing scheme is also present for the GPU of our choice, a similar technique is implemented for the GPU as well. V2P tables are produced during buffer pinning and communicated to the APEnet+ firmware, which uses them, for example, in the receive path to translate virtual addresses carried by packets into physical addresses, suitable to be used on the PCIe bus.

During 2012 a number of new features have been implemented in the APEnet+ driver:

- Support to the novel hardware features in the GPU TX side, described in section 3.1.1.2.
- Support to the NIOS completions (see 3.1.1.3).
- Management of overlapping entries in the PDC; user buffers may overlap, the driver is able to manage both the case of intersecting and inclusive memory ranges by merging the entries and maintaining a list of collisions.
- Support to Linux kernels version 3.X.X.

3.1.2.2 MPI for APEnet+

MPI is a standard syntax and semantics for message-passing for parallel computing platforms [16]. The MPI primitives integrate with commonly used programming languages in a number of efficient implementations. OpenMPI [17] is the one we chose to port MPI for the APEnet+ interconnection card: it is open source, it is portable and it is used by many TOP500 supercomputers [18], which testify its value for the HPC community and the necessity for our project to put effort in this activity.

The MPI API basically provides a virtual topology, synchronization and communication functionalities between processes that are mapped onto computing nodes instances. The MPI library functions include (but are not limited to) point-to-point rendezvous-type send/receive operations, choosing of logical process topology, combining partial results of computations (gather and reduce operations), synchronizing nodes (barrier operation) as well as obtaining network-related information (number of processes, process id, etc.). Point-to-point operations come in synchronous, asynchronous, buffered, and ready forms, to allow both relatively stronger and weaker semantics for the synchronization aspects of a rendezvous-send.

The OpenMPI library has a layered structure in terms of dependency (figure 24):

- **Open MPI (OMPI)** - The uppermost layer, contains the proper implementation of the MPI API.
- **Open Run-time Environment (ORTE)** - The middle layer: it is a common interface to the runtime system, it is responsible of launching processes, out of bound communication, resource management.
- **Open Portability Access Layer (OPAL)** - The bottom layer, it mostly contains utility code.
The substructure is based on the concepts of frameworks and components: the components are runtime loadable plugins, each of them is included in a framework. Components of the same type are in the same framework. This modular structure allows for example to specify at run-time which type of communication device to use when running an MPI program. Each component can have one or more instances, called modules.

Here we restrict our description to the frameworks shown in figure 25 organized hierarchically:

- **PML - Point-to-point Message Layer**, it implements the high level MPI point-to-point semantics and manages messages scheduling and matching as well as the progress of the different communication protocols (for long or short messages). The most important component in the PML framework is ob1, which is specifically targeted to BTLs, while the PML cm supports MTLs.

- **BTL - Byte Transfer Layer**, it is the framework that provides a uniform method for raw data transfer for numerous interconnects, both send/receive and RDMA based. BTLs components of common use are: sm, for intra-node communication between processes; self, for intra-process communication (a process that sends data to itself, useful to implement the collective semantics); tcp, for inter-node communication via sockets; etc.

- **MTL - Matching Transport Layer**, it’s the framework designed for networks that are able to implement message matching inside the communication library.

- **BML - Byte Management Layer**, in this framework the r2 component is responsible of opening and multiplexing between the BTLs.

In this context, the work of porting MPI communication library for the APEnet+ card can be seen as the implementation of a new BTL component called apelink that relies on the APEnet+ RDMA API (see 3.1.3.2).

Writing a new BTL basically consists in defining a series of functions, which are used by the upper PML component to manage communication. For the apelink BTL these handles can be summarized in table 10. These are necessary for a minimal support to the MPI API, a few more can be defined to enable advanced features, like efficiency-tuned RDMA protocols, fault-tolerance, etc.

A minimal and non-optimized implementation of the apelink BTL is available and aligned with the OpenMPI repository trunk at July 2012. This implementation has not been completely tested yet, but has been proven to work with simple MPI applications, like DPSNN as reported in section 3.3.4.

The apelink BTL can be selected at launch time instead of the usual ones (infiniband, tcp,...) for example:

```bash
mpirun -mca btl apelink,sm,self -n PROCESSES -host HOSTLIST program_name
```

Obviously the MPI frameworks add a substantial overhead to the communication latency so a consistent optimization work on the BTL is necessary to obtain interesting performances. We are now working on implementing the necessary logic inside the APEnet+ OpenMPI module to support GPU-aware point-to-point primitives implemented via the GPU peer-to-peer technique. The problem with GPU-aware MPI is
the one with small message size, where the eager protocol, which is often used in MPI implementations, cannot be used effectively. In the eager case, the matching between the MPI Send and the MPI Recv is handled by the receiving node and so it is arbitrarily delayed. This means that the sender does not know whether the destination buffer will end up on either host or GPU, and, more importantly, the APEnet+ firmware, on processing the incoming packet on the receiver side, does not know which kind of buffer to put the data onto. Of course, this will be resolved as soon as the application code on the receiving node posts a matching request, but it will be too late to avoid memory copies; more importantly, this does not fit with the RDMA model. One option we would like to experiment with is to embed additional GPU-related meta-data, necessary for the Send/Recv matching, in the eager packet, and to delay the processing of the packet, probably buffering it on the card, until the MPI Recv is actually executed by the application and its information are uploaded to the card; this would give the receiving card the opportunity to put the data in the correct final destination. With eager intensive traffic, this would probably be limited by on-board buffer space, and the additional processing could easily become counter-effective. The easiest solution would be to disable eager for GPU buffers altogether and to always employ rendez-vous. In this case, when a GPU buffer is used on the send side, the sender initiates the rendez-vous protocol, but the receiver side code has to be properly modified to handle this case.

3.1.2.3 Presto

Presto is an MPI-like communication library that implements RDMA data transfers using an eager or
Figure 25: The OpenMPI structure is based on frameworks and components. Each framework can have multiple components, for example the PML framework has the ‘ob1’ or the ‘cm’ components. Each of them supports a different low level communication framework, BTL for ‘ob1’ and MTL for ‘cm’. Each BTL component allows a different communication means or device, for example the BTL ‘apelink’ is the one written to use the APEnet+ card.
| Function name                               | Description                                                                 |
|--------------------------------------------|-----------------------------------------------------------------------------|
| mca_btl_apelink_add_procs                  | Discovers which processes are reachable by this module and create endpoints structures. |
| mca_btl_apelink_del_procs                  | Releases the resources held by the endpoint structures.                      |
| mca_btl_apelink_register                   | Registers callback functions to support send/recv semantics.                 |
| mca_btl_apelink_finalize                   | Releases the resources held by the module.                                   |
| mca_btl_apelink_alloc                      | Allocates a BTL specific descriptor for actual data.                         |
| mca_btl_apelink_free                       | Releases a BTL descriptor.                                                  |
| mca_btl_apelink_prepare_src                | Registers user buffer or pack data into pre-registered buffer and return a descriptor that can be used for send/put. |
| mca_btl_apelink_prepare_dst                | Prepares a descriptor for send/rdma using the user buffer if contiguous or allocating buffer space and packing. |
| mca_btl_apelink_send                       | Initiates a send.                                                            |
| mca_btl_apelink_put                        | Initiates a RDMA WRITE from a local buffer to a remote buffer address.       |
| mca_btl_apelink_get                        | Initiates a RDMA READ from a remote buffer to a local buffer address.        |
| mca_btl_apelink_register_error_cb          | Registers callback function for error handling.                             |

Table 10: Functions defined by the BTL apelink.

The Presto library have been available to the EURETILE partners since the early stages of the project, allowing the early integration and use of the DNP SystemC model in the Virtual EURETILE Platform (see D5.1 [19] and D5.2 [8]).

More effort is still necessary to make the Presto library optimized in order to extract the best performances from the APEnet+ card. Even if MPI is a more standard tool for application development, Presto can be seen as the simplest way to reach the best performance and usability for the APEnet+ card even with legacy MPI applications, that in principle would require just a renaming of the communication primitives to run in a Presto+APEnet+ environment. Also the similarities in the implementation of MPI and...
Presto and the lack of complexity of the latter, make our library a good testbench to experiment a GPU-RDMA integration and find solutions to fix the communication protocol in case of small GPU packets as mentioned in section 3.1.2.2.

3.1.2.4 DNA-OS Driver
DNA-OS was developed targeting MP-SoC’s and embedded systems; devices using the PCIe are not usually represented in such an IT ecosystem. The target of adapting DNA-OS to run within an x86 platform and drive a PCIe device like APEnet+ required significant work:

- accommodating the basic requirements of a generic PCIe device needed modifications to the DNA-OS Hardware Abstraction Layer (HAL) and the creation of an API for a generic bus driver (described in detail in section 6.1.2 and 6.1.3 of D4.2 [20]);

- the addition of services in DNA-OS to manage the sources of interrupts within an x86 platform — peripherals like timers and Ethernet/APEnet+ cards — and interaction with a user (described in detail in section 5.1 and 5.3 of D4.2 [20]);

- ex novo development of a prototype driver specific to the APEnet+ card (described in detail in section 2.6.1 of D8.1 [21]).

First two items are structural modifications which were mandatory for having the chance of running the DNA-OS run on x86 platform as a ‘lightweight’ OS while the third item is specific to the APEnet+ card. With these additions in place, the modified infrastructure was tested and validated by a simple program produced by the DNA-OS toolchain and running on x86 that queries and sets some board internal registers through the PCIe Base Address Register 0 (BAR0). This program — more complete details on its operation are available in section 6.1.5 of D4.2 [20] — is the first stage of what will become the complete APEnet+ driver for DNA-OS.

3.1.3 Test, Debugging & Measures

3.1.3.1 Setup of Test & Debug (T&D) environment
The environment where the APEnet+ card is being developed — from now on the T(est) & D(egug) platform — which is actually also a prototype for the EURETILE HPC platform, the QUonG cluster, consists of a mostly homogeneous x86 cluster where the nodes are 1U units equipped with dual Xeon CPUs. More precisely, the T&D is composed of (not mentioning off-the-shelf components like the Gbit Ethernet switch, ECC DRAM banks, etc.):

- 10 SuperMicro X8DTG-D dual Xeon SuperServers;

- 9 Mellanox ConnectX VPI MT26428 InfiniBand Host Channel Adapters (HCAs)

- 1 SuperMicro X8DAH+ dual Xeon SuperWorkstation;
• 1 SuperMicro X8DTG-QF dual Xeon SuperWorkstation;
• 1 Mellanox MTS3600/U1 QDR 36-port switch;
• 13 NVIDIA GPUs systems:
  – 2 Tesla arch. discrete cards (2xC1060);
  – 7 Fermi arch. discrete cards (2xC2050, 3xM2050, 2xM2070);
  – 4 Fermi arch. cards housed into 1 S2070 multi-GPU rack.

The diversity of the nodes is partly due to different procurement epochs but also to cater to different needs; e.g., the two SuperWorkstation units are 4U tower systems which, although more bulky than the 1U SuperServer ones, allow for easy 'open-heart' inspection of the APEnet+ board when it is attached to a protocol analyzer — e.g. the Teledyne LeCroy Summit T2-16 — to peruse the low-level workings of the PCIe bus. The S2070 multi-GPU rack of the T&D was the first assembly of the elementary building block which is the keystone for the QUonG cluster, made of two 1U SuperServers that ‘sandwich’ the 1U S2070 rack; the result is a unit with the optimal ratios of 4 GPUs vs. 4 CPUs and 4 GPUs vs. 2 APEnet+ cards compacted into a 3U volume.

The CPUs are quad-core (X5570/E5620) and hexa-core (X5650/X5660) variants of Sandy-Bridge dual-core Xeons with frequencies in the 2.40÷2.93 GHz range and ECC RAM from 12 to 48 GB per node. Differently populated topologies can be tested on the T&D rearranging the connections of the APEnet+ cards: closed 1-dim loops, 2-dim and 3-dim torus meshes (4x2 is actually in test), etc. The InfiniBand HCAs and switch are necessary for comparison purposes to a network fabric fat-tree topology having the high bandwidth and low latency currently considered state-of-the-art for an HPC cluster.

A worth mentioning feature of the SuperMicro SuperServers is the compliance with the Intelligent Platform Management Interface (IPMI) for out-of-band management. This means that every T&D node has onboard a subsystem (called a Baseboard Management Controller or BMC) which operates independently of the host OS and lets an administrator perform a number of tasks that would usually require physical proximity with the device — as accessing BIOS settings, temperature/voltage probing or even power-cycling for the unit — through an out-of-band connection, in this case conveyed over an auxiliary Ethernet plug. The value of IPMI is twofold:

• the debug phase of low level, potentially system-disrupting software is made considerably easier — a machine locked hard by an unstable, under development kernel device driver can be power-cycled without compelling the programmer to physically reach the cluster and flip the switch;
• it provides essentially for free a number of machine stats — like voltages, fan speeds or system temperatures — that can be logged in real-time and eventually used to assess the health status of the machine.

The operating system is a stock CentOS 5.X GNU/Linux, with standard 2.6.18 kernel line; we are currently evaluating migration to the newer CentOS 6.X with 2.6.32 kernel line, which is to be the target OS for the QUonG cluster. The software stack for the GPUs — driver and development kit — is standard NVIDIA CUDA in both versions 4.2 and 5.0.
3.1.3.2 Software Testsuite (Tools, Synthetic Benchmarks)

The development of the APEnet+ card required writing a great deal of software; besides the fundamental middleware needed to implement a working API for communication with the board — see 3.1.2 for more details —, a large number of small test codes (mostly in C supplemented by scripts in Bash/TCSH) were written. They are necessary for automation of the procedure that ‘kickstarts’ the board to a usable state at system startup and, more importantly, to stimulate in the most punctual way all the device’s subsystems, in order either to timely verify that each modification to the firmware was not causing regressions or to help in debugging them when they appeared. Moreover, especially when the APIs are under development so that resorting to extensive rewrites of a more complete application is unfeasible, these synthetic tests are invaluable to immediately gauge the gains or losses in performance for every optimization that was added to the board design along the course of its evolution.

An exhaustive list of these tests is not very informational and a recap of the relevant data — aggregated bandwidth and latency — are given in 3.1.3.3 together with a comparison to results gathered by the equivalent OSU benchmarks [22] over the InfiniBand fabric of the T&D platform described in 3.1.3.1. We just show here an example of the data gauged by one of these tests, \texttt{p2p\_gpu\_perf}, that measures the bandwidth of a loopback GPU-to-GPU data transfer; it exercises one of the most complex path inside the APEnet+. In figure 26 we have the aggregated data of the test as seen by the host together with some debugging output. In this test, data packets in transit through the RX path of the transfer are processed in a number of steps performed by the Nios II processor.

```
[biagioni@ape2 niostest]$ ./p2p_gpu_perf -n10000 -s131072
Apelink Device 0 opened
test is: 10000 131072 bytes pkt(s) from a GPU memory (TX) buffer in loopback toward a persistent GPU memory (RX) buffer
my addr (0,1,0): 0
sending to addr (0,1,0): 0
msg size=131072
initializing CUDA
There is 1 device supporting CUDA
[pid = 26166, dev = 0] device name = [Tesla M2050]
creating CUDA Ctx
making it the current CUDA Ctx
cuMemAlloc() of 131072 bytes GPU TX buffer
allocated GPU TX buffer address at 0000000b00100000
filling TX GPU buffer with a 32bit ramp [0,1,...]
cuMemAlloc() of a 4194304 bytes GPU RX buffer
allocated GPU RX buffer address at 0000000b00200000, filled with '0xa5' !!!!
registering GPU buf=0xb0020000 as APEnet RX persistent RDMA buffer
registration returned buffer vaddr=0000000b00200000
sending 10000 pkts and waiting for both 10000 TX & 10000 RX events....
Bandwidth measured: 452.615MB/s (skipped first 0 msgs)
unregistering RX GPU vaddr=0000000b00200000
deallocating RX GPU buffer
deallocating TX GPU buffer
destroying current CUDA Ctx
[biagioni@ape2 niostest]$ [biagioni@ape2 niostest]$ 
```

Figure 26: Host console output with \texttt{p2p\_gpu\_perf} results.

In figure 27 we see a binning histogram with a run-down of these steps — e.g. B2A is the time taken by looking up a buffer in a virtual-to-physical address conversion plus the initialization of the memory write, while B2B is the time taken by the actual virtual-to-physical memory address translation — and their duration in cycles, averaged over a large number of runs and output directly by the Nios II.
This highly granular profiling allowed us to focus the activity on the areas that benefited mostly of tight optimization or were worth the extra effort of an hardware implementation.

Figure 27: Nios II console output with snapshot of profiling histogram.

3.1.3.3 Bandwidth & Latency Measures
The APEnet+ benchmarks were performed on the T&D platform — hardware and software details are in section 3.1.3.1. The APEnet+ cards used were preliminary with a reduced link speed of 28 Gbps.

To give an idea of the performance and limitations of the current implementation, in table 12 we collected the memory read performance, as measured by the APEnet+ device, for buffers located on either host or GPU memory and figure 28 shows a comparison between HOST and GPU memory read bandwidth at varying of the message size.

The complexity of the GPU peer-to-peer read protocol and the limitations of our implementation set a limit of 1.5 GB/s to the Fermi GPU memory read bandwidth, which is roughly half that obtained for host memory read (2.8 GB/s). For reference, the GPU-to-host reading bandwidth, as obtained by cudaMemcpy, which uses the GPU DMA engines, peaks at about 5.5 GB/s on the same platform (note NVIDIA GPU is an x16 I/O slot wide PCI Express card, while APEnet+ is only x8 wide). We underline that this is the reading bandwidth as measured from APEnet+ through the GPU peer-to-peer protocol, neither the internal device bandwidth, which is instead available to kernels running on the GPU, nor the GPU DMA engine bandwidth, e.g. cudaMemcpy(). The last two lines of table 12 and figure 28 show that, when the packet RX processing is taken into account by doing a loop-back test, the peak bandwidth decreases from 2.8 GB/s to 1.2 GB/s in the host-to-host case, and from 1.5 GB/s to 1.1 GB/s in the GPU-to-GPU
Figure 28: A comparison between HOST mem read and GPU mem read. The plots are obtained in a loop-back test flushing the TX injection FIFOs.

case, i.e. an additional 10% price to pay in the latter case. The last column in the table shows that the Nios II micro-controller is the main performance bottleneck. We are currently working on adding more hardware blocks to accelerate the RX task. The values reported in table 12 are obtained as the peak values in a loop-back performance test, coded against the APEnet+ RDMA API. The test allocates a single receive buffer (host or GPU), then it enters a tight loop, enqueueing as many RDMA PUT as possible to keep the transmission queue constantly full. Figure 29 is a plot of GPU reading bandwidth at varying message size, estimated by using the test above and by flushing TX injection FIFOs, effectively simulating a zero-latency infinitely fast switch.

The original V1 GPU_P2P_TX implementation without pre-fetching (for more details see 3.1.1.2) shows its limits. GPU_P2P_TX V2 (HW acceleration of read requests and limited pre-fetching) shows a 20% improvement while increasing the pre-fetch window size from 4KB to 8KB. Unlimited pre-fetching and more sophisticated flow-control in GPU_P2P_TX V3 partially shows its potential only in the full loop-back plot of figure 30. Here the Nios II handles both the GPU_P2P_TX and the RX tasks, therefore any processing time spared thanks to a more sophisticated GPU TX flow-control logic reflects to an higher bandwidth.

As shown above, reading bandwidth from GPU memory and RX processing are the two keys limiting factors of the current APEnet+ implementation. Therefore, it can be expected that they influence the communication bandwidth between two nodes in different ways, depending of the type of the buffers used.

To measure the effect of those factors independently, we run a two node bandwidth test on APEnet+, in
Figure 29: Single-node GPU memory reading bandwidth, showing the performance at varying message size, obtained by flushing TX injection FIFOs. Different curves correspond to the three GPU_P2P_TX implementations and to different pre-fetch window sizes, where appropriate. Figures are highly unstable for small message sizes, mainly due to software related issues under queue-full conditions.

Figure 30: Single-node GPU memory loop-back bandwidth, at varying pre-fetch threshold size. Different curves are as in the the previous plot. The full loop-back send-and-receive bandwidth is plotted and it is limited by the Nios II micro-controller processing capabilities.

principle similar to the MPI OSU [22] uni-directional bandwidth test, although this one is coded in terms of the APEnet RDMA APIs. The benchmark is basically a one-way point-to-point test involving two nodes. The receiver node allocates a buffer, on either host or GPU memory, registers it for RDMA, sends its address to the transmitter node, starts a loop waiting for N buffer received events and ends by sending back an acknowledgment (ACK) packet. The transmitter node waits for an initialization packet containing the receiver node buffer (virtual) memory address, writes that buffer N times in a loop with RDMA PUT, then waits for a final ACK packet.

The plot in figure [31] shows the bandwidth of APEnet+ for the four different possible combinations of source and destination buffer types: for source buffers located in host memory, the best performance of 1.2 GB/s is reached, with a 10% penalty paid when receive buffers are on the GPU, probably related to the additional actions involved, i.e. switching GPU peer-to-peer window before writing to it. For GPU source buffers, the GPU peer-to-peer reading bandwidth is the limiting factor, so the curves are less steep and only for larger buffer sizes, i.e. beyond 32KB, the plateau is reached. Clearly, the asymptotic bandwidth is limited by the RX processing, but the overall performance is affected by the transmission of GPU buffers. Interestingly, the Host-to-GPU performance seems to be a very good compromise bandwidth-wise, e.g. for 8KB message size the bandwidth is twice that of the GPU-to-GPU case. Of course this plot is good for analyzing the quality of the APEnet+ implementation, but it says nothing about which method is the best for exchanging data between GPU buffers, i.e. in which ranges GPU peer-to-peer is better than staging on host memory.

To this end, figure [33] is a plot of the GPU-to-GPU communication bandwidth, with three different methods: APEnet+ using GPU peer-to-peer; APEnet+ with staging of GPU data to host memory; OSU band-
Figure 31: Two-nodes uni-directional bandwidth test, for different combinations of both the source and the destination buffer types. When source is in GPU memory, the overhead is visible; at 8KB, the bandwidth is almost half that in the host memory case. The bandwidth cap is related to the limited processing capabilities of the Nios II micro-controller.

Figure 32: APEnet+ latency, estimated as half the round-trip latency. Different combinations of both the source and the destination buffer types.

width test, using MVAPICH2 [23] over Infiniband, which uses a pipelining protocol above a certain threshold, used for reference. The GPU peer-to-peer technique is definitively effective for small buffer sizes, i.e. up to 32KB; after that limit, staging seems a better approach.

Figure 34 is more useful to explore the behaviour of GPU peer-to-peer on small buffer size. Here the latency, estimated as half the round-trip time in a ping-pong test, shows a clear advantage of the peer-to-peer implementation with respect to staging (P2P=OFF in the figure), even on a very low-latency network as Infiniband. Indeed, the APEnet+ peer-to-peer latency is 8.2 µs, while for APEnet+ with staging and MVAPICH2/IB it is respectively 16.8 µs and 17.4 µs. In the latter case, most of the additional latency comes from the overhead of the two CUDA memory copy (cudaMemcpy) calls necessary to move GPU data between temporary transmission buffers. By subtracting the APEnet+ H-H latency (6.3 µs in figure 32) from the APEnet+ latency with staging (16.8 µs), the single cudaMemcpy overhead can be estimated around 10 µs, which was confirmed by doing simple CUDA tests on the same hosts.

The run times of the bandwidth test, for short message size, are plot in figure 35. In the LogP model [24], this is the host overhead, i.e. the fraction of the whole message send-to-receive time which does not overlap with subsequent transmissions. Of those 5 µs in the Host-to-Host case, at least a fraction can be accounted to the RX processing time (3 µs estimated by cycle counters on the Nios II firmware). When staging is used instead (P2P=OFF), out of the additional 12 µs (17 µs- 5 µs of the host-to-host case), at least 10 µs are due to the cudaMemcpy device-to-host, which is fully synchronous with respect to the host, therefore it does not overlap.

In conclusion, the GPU peer-to-peer, as implemented in APEnet+, shows a bandwidth advantage for message sizes up to 32KB. Beyond that threshold, at least on APEnet+ it is convenient to give up
Figure 33: Two-nodes uni-directional bandwidth test, GPU-to-GPU. P2P=OFF case corresponds to the use of staging in host memory. MVAPICH2 result on OSU MPI bandwidth test is for reference.

Figure 34: APEnet+ latency, GPU-to-GPU case. peer-to-peer has 50% less latency than staging. The MVAPICH2 plot is the GPU OSU latency test on Infiniband.

Figure 35: APEnet+ host overhead, estimated via bandwidth test.

on peer-to-peer by switching to the staging approach. Eventually that could have been expected, as architecturally GPU peer-to-peer cannot provide any additional bandwidth, which is really constrained by the underlying PCIe link widths (X8 Gen2 for both APEnet+ and Infiniband) and bus topology.

Figure 36 and figure 37 show a comparison between APEnet+ and Infiniband in case of Host-to-Host transaction. In this case APEnet+ can not exploit any optimization for small message size, as peer-to-
peer in case of GPU-to-GPU transaction. On the other hand Infiniband takes advantage of dedicated path for different message sizes to optimize the latency. When the message size increases (greater than 8 KB) the APEnet+ RX processing is limited by the reduced performance of the Nios II. This limitation explains the huge gap in bandwidth for great size messages. In section 3.1.1.1 we define a roadmap to increase the performance of the link equalizing the HOST memory read bandwidth. Thus the only critical part remaining is the RX processing one. At the moment we are defining a re-working strategy of the hardware code to remove several tasks from Nios II, trying to relieve it, optimizing the performance of the RX path. Referring to table 12 and figure 28 the maximum bandwidth that APEnet+ can achieve is the HOST memory read one (2.8 GB/s) not much less than the Infiniband Host-to-Host bandwidth (3.3 GB/s).

3.1.3.4 Effective Frequency: theoretical approach to APEnet+ optimization

The results of benchmarks reported in section 3.1.3.3, allowed us to select hardware/software blocks to be optimized, in order to further speed-up the APEnet+ design. An alternative approach to the physical benchmarking leading to similar results is the analysis sketched in this paragraph, where a new blocks evaluation index is introduced. The amount of available memory is one of the FPGA most critical resources. The on-chip memory available in Stratix IV EP4SGX290NF45C2, the APEnet+ card device, is limited to 1.74 MB. Thus, the architectural choices performed during the hardware development phase aims to minimize the amount of used memory and to achieve the target performance. The right balance between these two aspects is one of the factors behind the success of a project.

To perform a deeper analysis about the connection between memory consumption and achieved bandwidth, we introduce the parameter Effective Frequency \( f_{eff} \) defined as the ratio of used memory to the achieved peak bandwidth with the implemented architecture.
Then we introduce the ratio \( O \) of effective bandwidth to the operating frequency \( f_{\text{real}} \).

\[
O = \frac{f_{\text{eff}}}{f_{\text{real}}}
\]

The aim of these parameters is to detect the limitations of the architectural decisions and to assist in re-allocating the available memory resources. \( O \) is defined in a range \( O \in [0; 1] \). The closer to 1 the value approaches, the higher the level of memory optimization. The proper use of parameter \( O \) is clarified by the following points.

- First of all, implement and optimize the architecture to achieve the desired performance.
- Once the desired performance is reached, analyze the memory consumption and calculate the \( f_{\text{eff}} \) and \( O \).
- Optimize the memory consumption without affecting the achieved performance.
- Uniform memory optimization level of all logic blocks of the implementation, eliminating the presence of bottlenecks.

We identified 5 key logic blocks to evaluate the performance of the APEnet+ card:

- the **TX BLOCK** is responsible of reading from the host memory.
- the **GPUTX BLOCK** is responsible of reading from the GPU memory, implementing the *peer-to-peer* capabilities to optimize the latency of the reading process.
- the **RX BLOCK** is responsible of writing to the host/GPU memory.
- the **TORUS LINK** is responsible of data-transmission between neighbouring nodes.
- the **Nios II** the on-board micro-controller simplifies the tasks of GPUTX BLOCK and mainly of RX BLOCK.

In table 13 we collect the amount of memory used in the current implementation of the main logic blocks. The first line of the table reports the memory consumption due to the implementation of the **TX BLOCK**. **TX BLOCK** is the more performing logic block and it satisfies our expectation. It defines a good balance between performance and memory consumption (only 6%) then \( O_{\text{TX}} \) can be taken as reference to evaluate the memory optimization level of the remaining logic blocks.

The second line collects the **GPUTX BLOCK** status. In this case \( O_{\text{GPUTX}} \) is lower than the **TX BLOCK** one. We have to consider that *peer-to-peer* is a convenient optimization for small size messages. The
size limitation prevents to reach the maximum performance. The effective frequency is an evaluating parameter in case of peak performance. Then it confirms that for greater size messages a different GPU memory reading protocol is necessary. As explained above the staging approach is a good alternative to increase the peak bandwidth of the GPU memory read process considering also the high level of optimization of the TX BLOCK.

To analyze the RX block by itself we modified the one-way point-to-point test involving two nodes described before, to bypass the Nios II during the memory writing process. Basically the receiver node communicates to the transmitter node the physical memory address of the allocated buffer, on host memory, instead of the virtual one. In this way when the RX BLOCK receives the data-packet can use the physical memory address contained in the Header to perform the PCI transaction without questioning the Nios II. This make it possible to eliminate the bottleneck introduced by the micro-controller. At the moment the result of these tests is afflicted by the reduced capabilities of TORUS LINK (as shown in section [3.1.1.1] but it allows to establish that RX BLOCK can sustain a bandwidth equal to or greater than 2.0 GB/s. In this case \( O_{RX} \) is in line with \( O_{TX} \) but it could be better once we discover the real architecture limitation.

The last line shows the memory resources reserved for Nios II. Obviously a micro-controller needs a huge amount of memory compared to normal hardware blocks. In this case we want to evaluate the choice to use the Nios II in the RX chain (Nios II plus RX BLOCK). \( O_{Nios} \) is an order of magnitude lower of \( O_{RX} \). It results in a dramatical loss of performance. This consideration may lead to produce an effort to move some RX functionalities from Nios II to RX BLOCK, re-allocating memory resources, in order to maximize the performance.

Finally, the TORUS LINK has the higher value of \( O \) ratio (three times higher than \( O_{TX} \)). The value reported is the total memory used by 6 channels and we consider the aggregated bandwidth. The optimization of the memory resources is too high and clearly it limits the TORUS LINK performance. The modification proposed in section [3.1.1.1] (doubling RX LINK FIFO) is strengthened by this observation even if it should cause a decrease in the effective frequency of the TORUS LINK. In this case a reduction of memory optimization homogenizes the resources usage and increases the performance.

### 3.1.3.5 HW instrumentation for debugging

In APEnet+ we implemented two main components devoted to debugging: we monitor data transferred between two APEnet+ cards by means CRC (Cyclic Redundancy Check) blocks, and internal data path by means of a DATA PARITY CHECKER (figure [38]).

CRC_TX calculates the check value for the whole data-packet to be sent (header+payload+footer) using the CRC-32 IEEE standard polynomial. The check value is appended to the Footer. The error detection is performed by CRC_RX, that calculates the check value and compares it with the received one. The chosen polynomial (CRC-32 IEEE) is able to detect a maximum number of errors that ranges from 2 to 6.

A TORUS LINK is considered sick when the ratio between the number of errors and the number of
packets received overruns a given (programmable) threshold.

The **DATA PARITY CHECKER** block detects error on each 128-bit data word transferred inside APEnet+. This error-detection technique requires a software support: the 128th bit of each payload’s word have to contain the **parity bit** of the first 127 bits. The **DATA PARITY CHECKER** checks the **parity bit**.

We implement a **DATA PARITY CHECKER** in the input of each data FIFO (as shown in figure 38); it calculates for each 128-bit data word pushed in FIFO the **parity bit** according to the first 127 bits, and then it compares the result with the bit 128. If the comparison fails, indicating that a parity error occurred, the block sends an interrupt request and writes in a dedicated register the incorrect word. Parity calculation is made by a XOR chain, as show in picture 39.

Once got interrupt, we can investigate and then modify the path between data FIFO connected at the **DATA PARITY CHECKER** that founds error. Usually these problems are due to a long path between a

---

**Figure 38: Hardware instrumentations for debugging on APEnet+.**
signal's source and its destination.

![Diagram of DATA PARITY CHECKER Block]

**Figure 39: Architecture of DATA PARITY CHECKER Block.**

3.1.3.6 Resource's utilization, power measurements and link characterization

APEnet+ is developed on an EP4SGX290 FPGA, which is part of the Altera 40 nm Stratix IV device family.

In Table 14 and 15 is shown an outline of the FPGA logic usage measured with the synthesis software Quartus II.

The thermal power dissipation measurements are obtained from the power analyzer tool by Altera, with a value for the power input I/O toggle rate set to 25%. The power dissipation associated to a single channel (4 lanes and related logic) amounts to slightly more than 1 Watt.
The Stratix IV GX provides up to 32 full-duplex Clock-Data-Recovery-based transceivers with Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA). In order to produce the clearest signal and thus being able to increase signal clock frequency on cable, a fine tuning of PMAs analog settings is required. Since the transmitted signal is sensitive to the physical route that it must travel toward the receiver (cable, connectors, PCB lanes), a number of analog settings must be appropriately tuned to offset for distortions. Altera provides the Transceiver Toolkit as a specific tool to choose the appropriate values for these analog controls. The Transceiver Toolkit performs its job by tuning the Reconfig block; it can dynamically reconfigure analog settings of the PMAs such as Pre-emphasis and DC Gain on the transmitter side and Equalization and VOD on the receiver side; furthermore, it offers a simple GUI to tweak these settings and to see immediate feedback on receiver side. By means of this tool we found the optimal settings for each of the four lanes in all six channels (figure 40).

Figure 40: Transceiver Toolkit GUI: analog settings for transmitter and receive channels of X+ channel’s lane 0.

Once the tuning phase is done, a following step is the testing of these settings on our board with our custom logic. Our testing firmware is made of a random signal generator (PRBS @32 bits) on the transmitting side and a data checker on the receiving side. Transmitter and Receiver are synchronized by a dedicated protocol implemented in the TORUS LINK. The numbers of correctly and incorrectly transferred 128-bits words are stored in registers. In this way we can either measure the bit error rate of the channels (number of incorrectly transferred words/number of transferred words) and verify our alignment custom logic. In the table 16 we report some of the measures performed, taken with different cable lengths, channel ports, and data rate.

We verified successful data transfer up to the maximum declared rate per single lane (8.5 Gbps) in a defined range of the analog settings. Anyway at this moment, for reliable operations and upper level firmware and software validation, we use a more conservative setting for all transceivers lanes.
Project: **EURETILE** - European Reference Tiled Architecture Experiment
Grant Agreement no.: **247846**
Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

![Eye Pattern](image)

| a) 5 Gbps. | b) 6 Gbps. |
|------------|------------|
| ![Eye Pattern](image) | ![Eye Pattern](image) |

(c) 8.5 Gbps.

Figure 41: Eye Pattern.

at 7.0 Gbps, which makes the channels raw aggregated bandwidth at 28 Gbps.

In order to verify link quality, we prepared a testbed for measuring signal integrity for the received data. Testbed is composed by an APEnet+ board which acts as a sender, a QSFP+ cable, and a QSFP+ to SMA breakout custom card. We prepared a special firmware for APEnet+, in which all the transmitter part of the transceivers are sending a random data pattern, with no waiting for the receive side to be aligned (as it is a one way measurement). Measurements were performed with a 20 GHz, 40 GS/s high bandwidth sampling scope (a LeCroy WaveMaster 820Zi-A) connected to the SMA test points on the break-out card. In figure 41 we show the Eye Pattern at 5 Gbps, 6 Gbps and 8.5 Gbps obtained using a cable of 1 m. length. Signal integrity could be improved by receiver side optimizations (like VOD or equalization) and by the insertion of a 100 Ω differential termination (as required by QSFP+ standard).

### 3.1.4 Board Production

A production batch of 15 boards has been processed during 2012. Some minor changes were introduced in this batch, with respect to the prototypal batch (4 boards) produced during 2011. These changes were including fixes of previous design mistakes.

A request for tender has been initiated at the beginning of the year, and the selected vendor resulted to
be Seco S.r.l. with the lowest bid and satisfactory technical proposal. Vendor was encharged with complete board production, component procurement (excluding the Altera Stratix IV component, which were provided directly by an Altera re-seller) and complete board assembly. Basic electrical tests have been performed at this stage.

Before validation, boards need to be initialized with a list of tasks:

- Altera EPM240 component programming — in order to have on-board Altera USB blaster capabilities on mini-USB connector.
- FTDI component initialization — for USB connection to JTAG properly working.
- Altera EPM2210 component programming — in order to have all on-board controllers working (sensors, clock management, JTAG capabilities, . . .).
- Altera Stratix IV programming.

Thus, production batch has been validated with a test suite on latest available software and firmware.

### 3.2 Assembly of the QUonG Hybrid Cluster

During 2012 a 16 nodes QUonG system has been deployed. The hardware procurement procedure carried out during 2011 has been further extended in order to reach the 16 nodes count of the currently available system (figure 42).

The QUonG hybrid computing node integrates an Intel Xeon E5620 double processor host with 48 GB of system memory, two S2075 NVIDIA Fermi class GPUs and an APEnet+ 3D network card. A 40 Gb/s Infiniband Host Controller Adapter is also available, in order to provide a de facto standard network interface to users and to perform comparative benchmarks with our custom 3D network interface.

The QUonG elementary mechanical unit is a 3U "sandwich" built assembling two Intel dual Xeon servers with a Next/IO vCORE Express 2075, a 1U PCIe bus extender hosting 4 NVIDIA Tesla M2075 GPU (figure 43). Topologically it corresponds to 2 vertexes on the APEnet+ 3D network.

Currently, only 4 out of 16 nodes are actually equipped with an APEnet+ board, enabling a bidimensional 2x2x1 network topology on these nodes. By Q2 2013 the whole system will be connected by the APEnet+ 3D network, with a 4x2x2 topology.

The software environment of the cluster is based on CentOS 6.3, with a diskless setup where the computing nodes are bootstrapped via the GbE network interface, and employs the NVIDIA CUDA 4.2 driver and development kit for the GPUs. Both OpenMPI and MVAPICH2 MPI libraries are available.

Users can submit parallel jobs using the SLURM batch system, with full support for task launch for OpenMPI and MVAPICH2 applications. Programs linking the OpenMPI library can perform communications both over APEnet+ and Infiniband fabrics, those linking the MVAPICH2 can use only the Infiniband.
### Project: EURETILE - European Reference Tiled Architecture Experiment
Grant Agreement no.: 247846
Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

| **Basic functions** |
|---------------------|
| `pr_init(pr_mgr_t m)` |
| `pr_fini(pr_mgr_t m)` |
| `pr_get_num_procs(pr_mgr_t m, int &n_procs)` |
| `pr_get_self_rank(pr_mgr_t m, pr_rank_t &rank)` |
| `pr_get_clock(pr_mgr_t m, pr_clock_t &clk)` |
| `pr_get_clock_res(pr_mgr_t m, int &clk_res)` |
| `pr_get_time(pr_mgr_t m, pr_time_t &tm)` |

| **like** |
|---------------------|
| `MPI_Init()` |
| `MPI_Finalize()` |
| `MPI_Comm_size()` |
| `MPI_Comm_rank()` |
| `MPI_Comm_rank()` |
| `MPI_Barrier()` |

| **fast cycle counter, in usec** |
|---------------------|
| `get_clock_resolution()` |

| **get wall-clock time in msec like** |
|---------------------|
| `gettimeofday()`, `MPI_Wtime()` |

| **peer-to-peer primitives** |
|---------------------|
| **blocking** |
| `pr_send(pr_mgr_t m, pr_rank_t dest, pr_word_t buf, size_t nw)` |
| `pr_recv(pr_mgr_t m, pr_rank_t src, pr_word_t buf, size_t nw)` |
| `pr_bcst(pr_mgr_t m, pr_rank_t orig, pr_word_t buf, size_t nw)` |

| **non-blocking** |
|---------------------|
| `pr_isend(pr_mgr_t m, pr_rank_t dest, pr_word_t buf, size_t nw, pr_req_t r)` |
| `pr_irecv(pr_mgr_t m, pr_rank_t src, pr_word_t buf, size_t nw, pr_req_t r)` |
| `pr_wait(pr_mgr_t m, pr_req_t r)` |
| `pr_waitall(pr_mgr_t m, pr_req_t r, size_t n)` |
| `pr_test(pr_mgr_t m, pr_req_t r)` |
| `pr_req_free(pr_mgr_t m, pr_req_t r)` |

| **Collective primitives** |
|---------------------|
| `pr_barrier()` |

| **like** |
|---------------------|
| `MPI_Bcast()` |
| `MPI_Isend()` |
| `MPI_Irecv()` |
| `MPI_Barrier()` |

| **wait for a request to complete, like** |
|---------------------|
| `MPI_Wait()` |
| `MPI_Waitall()` |
| `MPI_Test()` |

| **free a request, like** |
|---------------------|
| `MPI_Request_free()` |

Table 11: Functions defined by the Presto API.
| Test                  | Bandwidth | GPU/method          | Nios II active tasks |
|----------------------|-----------|---------------------|----------------------|
| Host mem read        | 2.8 GB/s  |                     | none                 |
| GPU mem read         | 1.5 GB/s  | Fermi/P2P           | GPU_P2P_TX           |
| GPU mem read         | 1.6 GB/s  | Kepler/P2P          | GPU_P2P_TX           |
| GPU-to-GPU loop-back | 1.1 GB/s  | Fermi/P2P           | GPU_P2P_TX + RX      |
| Host-to-Host loop-back | 1.2 GB/s |                     | RX                   |

Table 12: APEnet+ low-level bandwidths, as measured with a single-board loop-back test. The memory read figures have been obtained by flushing the packets while traversing APEnet+ internal switch logic. Kepler results are for a pre-release K20 (GK110), with ECC enabled. Fermi results are with ECC off. GPU and APEnet+ linked by a PLX PCIe switch.

| Logic Block             | Used Mem | % of Mem | Peak Bandwidth | $f_{eff}$ | $f_{real}$ | $O$  |
|-------------------------|----------|----------|----------------|-----------|-----------|------|
| TX BLOCK                | 0.105 MB | 6.0%     | 2.8 GB/s       | 26.7 MHz  | 250 MHz   | 0.107|
| GPUTX BLOCK             | 0.088 MB | 5.1%     | 1.5 GB/s       | 17.0 MHz  | 250 MHz   | 0.068|
| RX BLOCK                | 0.070 MB | 4.0%     | >2.0 GB/s      | >28.6 MHz | 250 MHz   | >0.114|
| TORUS LINK              | 0.167 MB | 9.6%     | 9.6 GB/s       | 57.5 MHz  | 175 MHz   | 0.328|
| Nios II                 | 0.402 MB | 23.1%    | 1.2 GB/s       | 3.0 MHz   | 200 MHz   | 0.015|

Table 13: An overview of memory consumption and its connection to the achieved performance.

| Logic utilization                      | 42%        | 13,191 mW   |
| Total Thermal Power Dissipation        |            |             |
| Combinational ALUTs                    | 70,673 / 232,960 (30%) |             |
| Memory ALUTs                           | 228 / 116,480 (< 1%) |             |
| Dedicated logic registers              | 61,712 / 232,960 (26%) |             |
| Total pins                            | 242 / 1,112 (22%) |             |
| Total block memory bits                | 7,533,432 / 13,934,592 (54%) |             |
| DSP block 18-bit elements              | 4 / 832 (< 1%) |             |
| Total GXB Receiver Channel PCS         | 32 / 32 (100%) |             |
| Total GXB Receiver Channel PMA         | 32 / 48 (67%) |             |
| Total GXB Transmitter Channel PCS      | 32 / 32 (100%) |             |
| Total GXB Transmitter Channel PMA      | 32 / 48 (67%) |             |
| Total PLLs                            | 3 / 12 (25%) |             |

Table 14: Summary of APEnet+ logic usage on Stratix IV EP4SGX290 FPGA.
Project: **EURETILE** - European Reference Tiled Architecture Experiment
Grant Agreement no.: **247846**
Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

|                                | Network Interface Block | Switch Block | Single Link Block |
|--------------------------------|-------------------------|--------------|-------------------|
| Combinational ALUTs           | 32,858                  | 12,879       | 4,216             |
| Memory ALUTs                   | 228                     | 0            | 0                 |
| ALMs                           | 25,893                  | 12,810       | 0                 |
| Dedicated logic registers      | 29,622                  | 12,321       | 4,413             |
| Block memory bits              | 4,609,848               | 2,875,392    | 8,032             |
| Power Dissipation              | 914 mW                  | 3,464 mW     | 1,134 mW          |

Table 15: Logic usage per logic block on Stratix IV.

| BER    | Direction | Cable length | Data Rate |
|--------|-----------|--------------|-----------|
| < 7.04 E-11 | X+       | 5m           | 8.5 Gbps  |
| < 8.12 E-11 | Y+       | 5m           | 8.5 Gbps  |
| < 7.04 E-10 | Z+       | 5m           | 8.5 Gbps  |
| < 9.8 E-13  | X+       | 5m           | 7 Gbps    |
| < 2.46 E-14 | X+       | 2m           | 7 Gbps    |

Table 16: BER measurements on APEnet+’s channel, taken with different cable lengths and data rate.
Figure 42: The QUonG Hybrid Cluster
Figure 43: How to assemble a QUonG sandwich.
3.3 Applications

Since its first deployment, QUonG cluster is available to users from different research areas like Lattice Quantum Chromo-Dynamics [25], Laser-Plasma Interaction [26], Complex Systems [27] and N-Body simulation for astrophysics [28]. Herebelow we give an outlook of the codes that were more thoroughly examined and customized to exploit the peer-to-peer capabilities of the APEnet+ boards equipping the QUonG cluster.

3.3.1 OSU Micro Benchmarks

A cluster like QUonG must be graded against what is currently considered standard reference for network performance gauging, i.e. the synthetic tests MPI_latency and MPI_bandwidth from the Ohio State University Micro Benchmarks (OSU-MB) suite [22]. Starting from version 3.5, they are also able to exercise any GPU-aware directives that the MPI infrastructure should offer. The pipelining strategies employed by different MPI stacks can be tested over the InfiniBand network fabric on QUonG and compared to the more advanced peer-to-peer capabilities employed by APEnet+; a detailed run-down of these runs and the results of the comparison can be found in section 3.1.3.3.

3.3.2 Heisenberg Spin Glass

One application that was used as testbench of the APEnet+ capabilities comes from the statistical mechanics field; it is the simulation of a prototypical complex system called Heisenberg Spin Glass (HSG) [29]. This system models a cubic lattice of magnetic classical 3D spins $\sigma_i$ subject to an Hamiltonian function $H = -\sum_{i\neq j} J_{ij} \sigma_i \cdot \sigma_j$ with the $J_{ij}$ couplings distributed with a normal Gaussian distribution law restricted to next-neighbours interaction ($J_{ij} = 0$ if $|i - j| > 1$).

Scanning the lattice, site after site, is needed for every computation performed onto the system, like in the heat-bath and over-relaxation algorithms for lattice dynamics or computation of observables like the internal energy. Standard techniques of domain decomposition are applied to this scan; the lattice is partitioned along one or more dimensions and different processes on different nodes scan a partition each, synchronizing with each other by exchange of lattice sites along the partition edges. The criticality of this exchange is apparent as soon as the processes are scaled up to make the ratio of computation time vs. exchange time smaller and smaller, all the more so when the computing processes are on GPUs and the exchange must take into account the staging needed to bounce back and forth the lattice partition from GPU memories.

This is exactly the scenario where the peer-to-peer capabilities of the APEnet+ board can be made to shine. After code rearrangement — replacing a small number of key MPI calls with equivalent ones to the RDMA API — a thorough study of the performance improvements was performed on the HSG application; results are published here [30] and here [31].
3.3.3 Lattice Quantum Chromo-Dynamics

Lattice Quantum Chromo-Dynamics is a challenging application and a staple of INFN research work. The LQCD field has greatly benefited of the strong boost given by GPU acceleration to stencil computations: in this regard, the QUDA library [32] is a renowned, advanced software package for multi-GPU Lattice QCD simulation that, in its standard form, employs MPI for communication but has not yet been modified to exploit the GPU-aware directives [33].

![Strong-scaling plot of GFlops per node for a QUDA run on QUonG.](image)

Moreover, since the domain decomposition techniques employed for the LQCD algorithms are exactly the same as in the HSG, the scaling issues hindering the HSG application belong to the LQCD application as well [34]. Out-of-the-box QUDA was installed and run on the QUonG cluster to verify those issues; in figure 44 we see the decrease of efficiency when strong-scaling the application of the Wilson-Dirac operator over a $48^3 \times 96$ lattice up to 24 GPUs — all twelve QUonG nodes (2 GPUs per node) which were available when the test was run.

The Gantt diagrams in figure 45 clarify the problem. On the 'K' row, the bars show the span of the computation in the bulk ('Int') and the frame of the lattice along the dimensions ('T', 'Z' and 'Y') for one GPU. On the 'T+/-', 'Z+/-' and 'Y+/-' rows, the bars show the span of consecutive 'P'repare, 'G'ather,
'C'ommunication and 'S'catter phases for the frame exchange between GPUs.

On the left side of figure 45, it is seen that on a \(48^3 \times 96\) lattice split over 4 GPUs, the span of 'P', 'G', 'C' and 'S' phases is completely overlapped to the 'Int' one, so that computation is not delayed by communication. On the contrary, the GPU computation kernel is throttled on 24 GPUs by the wait for completion of the frames exchange between neighbouring nodes (along the 'T', 'Z' and 'Y' axes in the '+' and '-' directions), especially so since the various 'G' and 'S' phases imply a number of GPU-to-host and host-to-GPU memory transfers that must be scheduled one after the other, interfering with the scheduling of the CUDA stream performing the computation kernel and adding an overall significant latency to the computing over the frames — see the blank areas of the 'K' row in the right side of the figure.

Since usage of peer-to-peer primitives should do not require the 'G' and 'S' phases, porting of QUDA to APEnet+ is foreseen to alleviate this degradation. Work for adding this support to the QUDA library is underway; it is a large and complex endeavour made even harder due to the fact that the application was not designed from the start with GPU-awareness for the communication primitives.

In the mean time, parts of the EURETILE toolchain were put to the test with LQCD on QUonG— especially the DAL functional simulator and the AED of the VEP simulator — with a reduced kernel of the main LQCD computation that was rewritten from scratch using either the DAL syntax and the RDMA low-level API. A more complete description of the various forms of this LQCD reference application for EURETILE is in section 4 of D7.2 [35].

### 3.3.4 Distributed Polychronous Spiking Neural Networks (DPSNN)

The investigation on "brain-inspired" techniques for the design of hardware and software components of future many-tile computing systems is among EURETILE key topics. In the proposal, we stated a set of
intuitions about the potentiality of such architectural concepts to many tile software and hardware architectures. Actually, we expect to exploit hints coming from the cortical architecture, a system capable of extreme parallelism and low power operation. We identified the development of a dedicated benchmark as a key asset to get quantitative and qualitative way-points along the project.

Such a cortical simulation benchmark should be used:

- as a source of requirements and architectural inspiration towards the extreme parallelism which will be exhibited by future many-tile systems;
- as a parallel/distributed coding challenge;
- as a scientific grand challenge. A well designed code could produce interesting scientific results.

During the previous reporting period (2011), in the framework of **WP7: Challenging Tiled Applications** we defined the characteristics of the DPSNN-STDP application benchmark (Distributed Polychronous Spiking Neural Network with synaptic Spiking Time Dependent Plasticity), as described by [D7.1](#).

This benchmark will be coded during the temporal framework of the EURETILE project both using a standard C/C++ plus MPI environment, as well as using the C/C++ plus XML DAL environment. This will allow to compare the features of the new environment in comparison to a classical environment on a benchmark which will be coded "from scratch" using an explicit description of parallelism.

Here, we highlight only a few results directly related to the development of the QUonG platform and APEnet+ interconnection board that are fully described by [D7.2](#).

In summary, during 2012, we designed and implemented the C++ code of a complete prototype of the DPSNN-STDP simulator. Then we run the full simulation cycle (initialization and dynamic phases of a network including $10^5$ synapses) in the C++ plus MPI environment on a QUonG prototype, using the standard InfiniBand interconnections, and obtaining the same behavior with different number of processes. Then we ported and run the initialization phase of the DPSNN-STDP code under the DAL plus C++ environment on a prototype environment where two QUonG nodes were interconnected by two APEnet+ card. We used the same C++ classes as building blocks to construct the DAL and MPI network of processes.

This will permit, during 2013, to start a comparison activity between the APEnet+ interconnect system and the InfiniBand system, and among the performances offered by the DNA-OS, MPI and Presto message passing software layers, when applied to the DPSNN-STDP benchmark. Then we will identify the middleware and hardware bottlenecks, and derive architectural improvements for future generations of interconnect systems.

### 3.3.5 Breadth-First Search

Breadth-First Search (BFS) is a fundamental graph algorithm that systematically explores the nodes in a graph. BFS is typically considered one of the most important graph algorithms because it serves as
a building block for many others, including betweenness centrality calculation, connected component identification, community structure detection and max-flow computation. Benchmark suites targeting graph applications perennially include BFS as a primary element.

Most of graph algorithms have low arithmetic intensity and irregular memory access patterns. In this context, those irregular computation and communication patterns are very interesting; the typical traffic among nodes that BFS traversal is able to generate is non-deterministic all-to-all, depending on the edge partitioning. The buffer sizes vary as well, so that the performance of the networking compartment is exercised in different regions of the bandwidth plot.

Recent works [37] have shown that, by using a Level Synchronous BFS, a single-GPU implementation can exceed in performance high-end multi-core CPU systems. To overcome the GPU memory limitation, some authors proposed [38] a multi-GPU code that is able to explore very large graphs (up to 8 billion edges) by using a cluster of GPU connected by InfiniBand.

The communication code of this BFS application was modified to use the peer-to-peer calls from the RDMA API of APEnet+; although the trials were conducted with APEnet+ still in a development and testing stage, the results obtained [39, 31], albeit preliminary, show an advantage of APEnet+ with respect to InfiniBand.

3.3.6 TRIGGU (RDMA API)

A very different endeavour for the APEnet+ card is within TRIGGU [40], a simulation of the data flow and processing — the track fitting — of a real time event selection system in a High Energy Physics experiment. Data produced by the silicon detector at the Collider Detector at Fermilab is sent from a transmitter node (simulating the detector) to a receiver node (the selection system) where it is processed on the GPU to look for tracks left by charged particles.

The system allows measuring both data transfer and processing latency. The time to copy memory into and out of the GPU represents a significant overhead for the total latency.

A number of strategies were tested in the software infrastructure to improve upon this overhead, exploiting the GPU-Direct functionalities of latest CUDA by NVIDIA and the RDMA API of the APEnet+ card. Using GPU-Aware MPI leads to a decrease in the memory transfer time for large data sizes, while usage of peer-to-peer communication strategies by means of the RDMA API over APEnet+ shows a strong boost to performance (10 $\mu$s on average) for even small data sizes.

3.4 IP exploitation

3.4.1 NaNet Project

The NA62 experiment at CERN aims at measuring an ultra-rare decay of the charged kaon ($K^+ \rightarrow \pi^+ \nu \bar{\nu}$); signal has to be extracted from a huge background which is ten orders of magnitude more frequent.
With an input particle rate of 10 MHz, some tens of thousands detector channels and the requirement of avoiding zero suppression as much as possible, triggerless readout into PCs is not feasible.

Very promising results in increasing selection efficiency of interesting events come from a pilot project within NA62 that aims at integrating GPUs into the central L0 trigger processor, exploiting their computing power to implement more complex trigger primitives [41].

Independently, in the framework of the EURETILE project, we were developing the low latency, scalable, GPU-accelerated PC cluster interconnect APEnet+, which is the first non-NVIDIA device to exploit the NVIDIA GPUDirect P2P protocol to enable zero-copy transfers to and from GPU memory.

From the joint effort of these two projects comes the next step of GPUs integration for the NA62 L0 trigger: the NaNet project.

The NaNet board is a custom FPGA-based NIC featuring a standard GbE interface and GPUDirect P2P capabilities, able to inject the UDP input data stream from the detector front-end directly into the Fermi/Kepler GPU(s) memory, with rates compatible with the low latency real-time requirements of the trigger system.

This makes for a modular and customizable hybrid (CPU+FPGA+GPU) system able to sustain low response time and real-time features and potentially re-usable in analogous contexts of strict timing requirements.

As main design rule, we partitioned the system in a way such that we could offload the CPU from any data communication or computing task, leaving to it only system configuration and GPU kernel launch tasks.

This choice was really a step in the right direction for the real-time requirement, eliminating the unavoidable OS Jitter effects that usually hinder system response time stability.

Data communication tasks have been entirely offloaded to NaNet by implementing a dedicated UDP protocol handling block that communicates with the P2P logic: this allows a direct (no data coalescing or staging is performed) data transfer with low and predictable latency on the GbE link-GPU data path.

The UDP OFFLOAD is an open core module [42]. It implements a method for UDP packet traffic offloading from a Nios II system such that can be processed in hardware rather than in software. The open core design is built for a Stratix II 2SGX90 development board. UDP OFFLOAD collects data coming from the Avalon Streaming Interface (Avalon-ST) of the Altera Triple-Speed Ethernet Megacore (TSE MAC) and redirects UDP packets into a hardware processing data path. Nios II subsystem executes the InterNiche TCP/IP stack to setup and tear down high speed UDP packet streams which are processed in hardware at the maximum data rate achievable over the GbE network.

Within the NaNet project we adapted the open core for our purposes. Above all we ported the hardware code to the Stratix IV family. This operation made possible to exploit the very improved performance of a two technology steps forward FPGA. In the Stratix II, the hardware components of the Nios II subsystem are synthesized at the operating frequency of 35 MHz. The limited operating frequency forces to implement multiple channels to sustain the data flow over a GbE Network. The synthesis performed on a Stratix IV achieves the target frequency of 200 MHz (in current implementation of APEnet+ the
The optimization allows to reduce the number of channels necessary to sustain the data-flow. Current implementation of NaNet board provides a single 32-bit width channel (at the present operating frequency it achieves the capabilities of 6.4 gbps, 6 times greater of the GbE requirements).

Data coming from the single channel of the modified UDP OFFLOAD are collected by the NaNet CTRL (see figure 46). NaNet CTRL is an hardware module in charge of managing the GbE flow by encapsulating packets in the typical APEnet+ protocol (Header, Payload, Footer).

The NaNet CTRL main functionalities are:

- It implements an Avalon-ST Sink Interface (the hardware modules of the UDP OFFLOAD communicates through Avalon-ST protocol) collecting the GbE data flow.
- It generates the Header for the incoming data, analyzing the UDP packet Header (message size)
and several configuration registers (see table 17 and table 18).

- It parallelizes 32-bit data words coming from the Nios II subsystem into 128-bit APEnet+ data words.

- It redirects data packets towards the corresponding FIFO (one for Header and Footer and another for the Payload). NaNet HEADER FIFO and NaNet DATA FIFO are connected to the RX BLOCK that exploits the commands stored in the Header to perform the GPU write transactions.

| Register Name                      | Description                                          |
|------------------------------------|------------------------------------------------------|
| NaNet RDMA virt addr LSB           | LSB of virtual address used in RDMA protocol         |
| NaNet RDMA virt addr MSB           | MSB of virtual address used in RDMA protocol         |
| NaNet RDMA command                 | Commands to initialize the RDMA process              |

Table 17: NaNet Configuration Register Overview.

| Bit Range | Name     | Description                      |
|-----------|----------|----------------------------------|
| 27 - 26   | port id  | process ID                       |
| 28        | is gpu   | Identify a GPU packet            |
| 29        | gpuid    | Identify the target GPU          |
| 30        | NaNet Last Frag | Identify the last part of a buffer |
| 31        | NaNet Phys Addr | Enable the Nios II bypass       |

Table 18: NaNet RDMA Command Register Layout.

Preliminary benchmarks for latency and bandwidth were carried out. Latency was measured adding timing info in the APEnet+ Footer with a resolution of 4 ns, and it shows that a packet traversal time ranges between 5.2 us and 6.8 us from input of NaNet CTRL to the completion signal of the DMA transaction on the PCIe bus (see figure 47).

Currently we are investigating the spread of the measure. Measured bandwidth was of about 120 MB/s, saturating the GbE channel capabilities.

We foresee several improvements on the NaNet design:

- Adding a buffering stage to the NaNet CTRL, enabling the coalescing of consecutive UDP payload data into a single APEnet+ packet payload, improving bandwidth figure also with small-sized UDP packets.

- Increasing the number of GbE channel in input, in order to sustain higher bandwidth demand coming from the experimental requirements.

- Moving towards a 10-GbE data link interface.
Figure 47: NaNet Latency; distribution plot over 60000 samples of a NaNet packet traversal time
4 Design of a Software-Programmable DNP architecture using ASIP technology

EURETILE’s many-core platforms critically depend on efficient packet-based communication between tiles in the 3D network. Efficiency refers to both high-bandwidth and low-latency. To reduce the latency, a significant acceleration of networking functions is needed. Target and INFN are jointly investigating the use of ASIP technology for this purpose, which will result in a low-latency software-programmable ‘DNP ASIP’. This section of the report describes the design of a first version of this DNP ASIP, which was delivered in 2012. The design was made using IP Designer, a retargetable tool-suite for the design and programming of ASIPs [43].

4.1 Introduction

The purpose of the new DNP ASIP is to accelerate time-critical network tasks. By providing the right instruction set specialization, a significant reduction can be obtained of the latency of key network management tasks. We focus on the APEnet+ network architecture. In APEnet+, each network node has two compute processors: an Intel x86 processor and an NVidia GPU. Network related tasks are offloaded onto a Distributed Network Processor (DNP). The DNP acts as an off-loading network engine for the computing node, performing inter-node data transfers. Currently, a DNP contains a Nios II processor. The firmware on the Nios II implements the following tasks [7]:

- Command processing. Commands are exchanged between the Nios II and the DNP core via command FIFOs.
- Packet RX, reading incoming packet headers in FIFO REQ and computing the final destination memory address, be it on either the host or the GPU, of the packet data.
- GPU TX, reading the virtual address and length of the source GPU memory buffer from FIFO P2P TX and stimulating the GPU to send the data to the GPU PKT CTRL.

4.2 The DLX template for architectural exploration

A first step in the development of an ASIP architecture is the selection of a suitable basic processor template. The characteristics of the template should be aligned with the requirements of the ASIP architecture. For the acceleration of the DNP tasks, the following characteristics are important:

- The architecture should have a fairly deep pipeline. This requirement is motivated by the fact that the architecture will be mapped onto an FPGA. Compared to a standard cell based mapping, on an FPGA the delay on the interconnections between architecture elements is long. It is then required to insert pipeline registers on these connections.
• The applications use 32 bit and 64 bit data. The ideal template architecture should therefore have hardware support for 32 bit and 64 bit operations.

• The applications contain quite a lot of control code. The template architecture should therefore be able to efficiently support the full complement of C language constructs.

• The applications make use of C library functions such as `malloc()`. The template architecture should therefore come with a C run time library that supports these functions.

Based on these requirements, we have selected the DLX processor template. DLX is the RISC processor architecture that is used as an example processor in the seminal book on computer architecture of John Hennessy and David Patterson [44]. The DLX processor has been modeled in nML, the processor description language supported by the IP Designer tool-suite.

DLX is a reduced instruction set architecture (RISC) with the following features:

• 32 bit wide data path, with an ALU, shifter and multiplier.

• 32 bit wide instruction word with an orthogonal, easy to decode, instruction encoding.

• 32 field central register file.

• a load/store architecture, which supports 8, 16 and 32 bit memory transfers and an indexed addressing mode.

• a 5 stage pipeline with separate stages for operand reads and writes.

More details of the DLX architecture are provided below.

### 4.2.1 Instruction Formats

Being a RISC architecture, DLX has only three main instruction formats. These are:

• The **R format**. This format is used for three register instructions. It has two fields, s1 and s2, to specify operand registers; one field, d, for the destination register, and a function field to select the instruction. For all current R type instructions, the opcode field is set to zero.

• The **I format**. This format is used for two register instructions with a 16 bit immediate operand. It has two fields, s1 and d, to specify operand or destination registers; and an opcode field to select the instruction.

• The **J format**. This format is used for control flow instructions with a 26 bit immediate operand.

The encoding of the opcode and function fields is specified in figure [48]
**4.2.2 Pipeline**

DLX has a 5 stage pipeline, with the following stages:

1. **Fetch Stage (IF)**
   (a) A new instruction is fetched from program memory and is issued.

2. **Decode Stage (ID)**
   (a) The instruction is decoded and the operands are read from the register file.
   (b) The unconditional jump instruction also executes in this stage: the target address is sent to program memory.

3. **Execute Stage (EX)**
   (a) This is the stage in which the ALU and shifter units execute their operation.
   (b) The pipelined multiply unit starts operating in this stage (the multiplications are finished in the next stage).
   (c) The multi-cycle iterative division is started in this stage.
   (d) For memory load operations, the effective address is computed and is sent to the memory. For store operations both address and data are sent to the memory. The load or store operation is started.
   (e) The conditional and indirect jump instructions execute in this stage.

4. **Memory Access Stage (ME)**
   (a) The multiply operations are completed.
   (b) The result of memory load operations is available on the data bus.

5. **Write Back Stage (WB)**
   (a) The result of ALU, shift, multiply or load operations is written to the destination field on the register file.
4.2.3 Data Path

Figure 49 shows the data path of the DLX processor, with the names of the main functional units and pipeline registers. In the ID stage the operands are read from R, using ports r1 and r2, and are stored in pipeline registers pS1 and pS2.

In EX, the outputs of the pipeline registers are connected to the inputs of the functional units, aluA and aluB, shA and shB, mpyA and mpyB or aguA and dm_wr; depending on the instruction that is being executed.

The ALU and shifter (SH) produce results at the end of EX. Their results are then stored in pD1 and pE1 before being written to the register file.

The 32x32 bit pipelined multiplier produces a full 64 bit result, with the low part in mpyC and the high part in mpyD. These two parts become available at the end of ME and are stored in pE1 and pE2 before being written to the register file.

The result of a load is also available in ME. It goes through a sign/zero extension unit SX, and is then stored in pE1 before it is written to the register file.
In case of a store operation the relevant part of the data is extracted in the SX unit.

For both load and store operations, the effective address is computed on the AGU. For the indexed addressing mode, an immediate offset is assigned to aguB, and is added to the address of aguA. The output aguC is copied to the address bus dm_addr. For indirect addressing with post-increment, the aguA input is copied to the address bus, and is also post-incremented by the value on aguB.

Operands are fetched from the register file in an early stage (ID) and written back three stages later (in WB). Consider a pair of data dependent instructions A and B: A produces a result in r3, and B uses this result. The B instruction can only read its operand if it is scheduled as the fourth instruction after A. Therefore three independent instructions (possibly NOP instructions) must be scheduled between A and B.

4.2.3.1 A. Bypasses

By adding register bypasses, it becomes possible to schedule A and B closer to each other. Register bypasses are connections that are added to the data path so that a result can be fed back to the operand pipeline registers as soon as it is available. For the ALU and shifter results, three bypasses can be added:

- When the A instruction is in the EX stage, the result is produced on the pd1w wire. It can be used by the B instruction in the next cycle. This requires that pd1w is written into pS1 or pS2.
- When the A and B instructions are scheduled two cycles apart, the result is present on the pe1w wire. It can be used by the B instruction when pe1w is written into pS1 or pS2.
- When the A and B instructions are scheduled three cycles apart, the result is present on the w1 transitory. It can be used by the B instruction when w1 is written into pS1 or pS2.

4.2.3.2 B. Stalls

Not all data hazards can be avoided by means of bypasses. The result of the pipelined multiplier, and the data that is loaded from memory are available only in the ME stage. A 1 cycle bypass is therefore not possible. The 2 and 3 cycles bypasses do apply here. To deal with the data hazard for the case of a 1 cycle delay, hardware stalls are used. A hardware stall means that the issuing of the dependent instruction is postponed until the hazard is gone.

4.2.4 Instructions

The DLX instruction set is partitioned into three groups:

- arithmetic instructions;
- load/store instructions;
These are explained in this section.

4.2.4.1 Arithmetic instructions

The following arithmetic instructions are supported:

*Additive Instructions:*

- addition (add);
- subtraction (sub);
- addition with carry (addx);
- subtraction with carry (subx);
- addition and subtraction with a signed immediate (addi and subi);
- addition and subtraction with a signed immediate and carry (addix and subix);
- addition and subtraction with an unsigned immediate (addui and subui);
- addition and subtraction with an unsigned immediate and carry (adduix, and subuix);

*Bitwise Instructions:*

- bitwise AND;
- bitwise OR;
- bitwise exclusive OR;

*Shift instructions:*

- logical shift left (sll);
- arithmetic shift right (sra);
- logical shift right (srl);

*Compare instructions:*

- set when equal (seq and seqi);
• set when greater or equal (signed compare) (sge and sgei);
• set when greater or equal (unsigned compare) (sgeu and sgeui);
• set when greater (signed compare) (sgt and sgti);
• set when greater (unsigned compare) (sgtu and sgtui);
• set when less or equal (signed compare) (sle and slei);
• set when less or equal (unsigned compare) (sleu and sleui);
• set when less (signed compare) (slt and slti);
• set when less (unsigned compare) (sltu and sltui);
• set when not equal (sne and snei);

4.2.4.2 Load and Store Instructions
The data memory supports 8, 16 and 32 bit wide load and store operations. Note that 16 bit values must be stored at addresses that are even, and 32 bit values at addresses that are a multiple of 4.

Five different load operations are possible:

• word load (lw);
• signed half word load (lh);
• unsigned half word load (lhu);
• signed byte load (lb);
• unsigned byte load (lbu);

For the signed loads, the 8 or 16 bit value is sign extended and then stored in the destination register. For the unsigned loads, the 8 or 16 bit value is zero extended.

Three different store operations are possible: word store (sw), half word store (sh), and byte store (sb). For the 8 and 16 bit stores, the least significant bits of the source register are stored in memory.

The load and store operations can be combined with indexed addressing mode, lw d1, i(s1) or sw s2, i(s1), the 16 bit signed immediate i is added to the content of register s1, to obtain the effective address. Indexed load store instructions use format I.
4.2.4.3 Control flow instructions

The DLX core supports conditional branch instructions with a PC-relative target address, unconditional jumps with either PC-relative or register indirect target address, and unconditional jumps with subroutine linkage.

- The conditional branch instructions `beqz s1,#imm` and `bnez s1,#imm` implement a conditional jump to the target instruction T, at address PC + imm, where imm is a 16 bit signed offset. The branch is taken when the operand register s1, contains zero for the `beqz` instruction, or a non-zero value for the `bnez` instruction. Conditional branches require three cycles before the target instruction can be issued. In the first cycle, the branch is issued; the following two cycles are filled with two delay slot instructions. The `imm` offset is relative to the address of the second delay slot instruction.

- The `j #imm` instruction implements an unconditional jump to the target address PC + imm, where imm is a 26 bit signed offset. It takes two cycles to complete and has one delay slot. The `imm` offset is relative to the address of the delay slot instruction.

- For the `jr` instruction, the absolute target address is obtained from the register specified by s1. The instruction takes three cycles to complete and has two delay slots.

- For the `jal` instruction, the target address is obtained by adding a 26 bit signed immediate to the PC. The instruction takes two cycles to complete and has one delay slot. The `imm` offset is relative to the address of the delay slot instruction. The return address is the address of the instruction after the delay slot instruction and is stored in the LR register.

- For the `jalr` instruction, the target address is obtained by adding the register specified by s2 to the PC. The instruction takes three cycles to complete and has two delay slots. The return address is the address of the instruction after the two delay slot instructions and is stored in the LR register.

4.3 The Buffer Management Application

Buffer management is a part of Remote Direct Memory Access (RDMA). RDMA allows to directly read/write information in the memory of another processor with minimal demands on memory bus bandwidth and CPU processing overhead. The micro-controller in the DNP simplifies the architecture by implementing in firmware some RDMA tasks. Its role is to manage the RDMA look-up table allocated in the on-board memory, with the following basic operations:

- To add/delete entries in case of register/unregister buffer operations;

- To retrieve the appropriate entry to satisfy buffer info requests for the incoming `DNP_put` or `DNP_get` operands.

A buffer is characterized by the following record
typedef struct buf_desc {
    addr64_t VirtAddr;
    u32 Len;
    u32 Flags;
    addr64_t MagicWord;
} buf_desc_t

Elements of this type are stored in some form of storage. In a pure software based implementation they are stored in a double linked list of which the nodes are dynamically allocated. In the ASIP implementation, we will add a dedicated hardware structure to store the buf_desc information.

There is a software API for manipulating the pool of buffer descriptors. The most important functions of that API are the following:

- Add an element to the pool of buffers;

```c
int append_persistent_buf(buf_lists_t *bls,
    addr64_t VirtAddr,
    u32 Len,
    u32 Flags,
    addr64_t MagicWord)
```

- Check if an address range given by a start and end address lies within one of the buffers of the pool, and return the properties of that buffer.

```c
int search_persistent_buf_by_range(buf_lists_t *bls,
    addr64_t start_addr,
    addr64_t end_addr,
    buf_desc_t *buf)
```

- Search for a buffer based on the parameters start address and length, and remove the buffer from the pool when found.

```c
int remove_persistent_buf(buf_lists_t *bls,
    addr64_t start_addr,
    size_t len)
```

For the development and the benchmarking of an ASIP architecture, it is useful to have a benchmark program for these API calls. The benchmark that we use in our design contains the following API calls:

- First 32 buffers are added (append_persistent_buf);
- Next three buffers are searched:
  - the buffer that was added first;
– the buffer that was added as 16th buffer;
– the buffer that was added last;

• The first, 16th and final buffers are removed;
• The 16th buffer, which is no longer present in the pool is searched again;

This benchmark will give a good impression of the average, minimum and maximum execution times for the three main operations. Table 19 shows the cycle counts for the execution of the benchmark program on different processor architectures, for a typical set of data. These results will be discussed further in the next sections.

| Operations      | Nios II | DLX | D64 | D64AC | D64SB | D64OPT |
|-----------------|---------|-----|-----|-------|-------|--------|
| Append 0...31   | 6839    | 4836| 4836| 418   | 419   |        |
| Search 0, 16, 31| 1802    | 2454| 1938| 1644  | 794   | 304    |
| Remove 0, 16, 31| 1192    | 3523| 2732| 2438  | 1504  | 560    |
| Search 16       | 596     | 787 | 517 | 455   | 483   | 166    |
| Total           | 10433   | 11631|10023| 9373  | 3199  | 1449   |

Table 19: Measured Cycle counters for benchmark program on different processor architecture.

4.4 Architectural exploration using IP Designer

The IP Designer tool-suite was used to design and optimize the DNP ASIP architecture, starting from the initial DLX implementation. The architectural exploration process is described in the next sections.

4.4.1 Implementation on Nios II and DLX32

For the pure software implementation, the pool of buffers is implemented as a double linked list, of which the elements are dynamically allocated on the heap. The reference code makes use of the type agnostic list implementation of the Linux kernel code (include/linux/list.h). In order to implement the double linked list, a list_head member is added to the buffer descriptor

```c
struct list_head {
    struct list_head *next, *prev;
};
typedef struct buf_desc {
    struct list_head node;
    addr64_t    VirtAddr;
    u32         Len;
};
```
The results obtained for the benchmark code on the Nios II architecture are captured in first column of Table 19. The results obtained for the benchmark code on the DLX architecture are captured in second column of Table 19. These results will serve as a reference to measure the speedup of architecture specializations.

From the profiling information that is produced by the ChessDE debugger (Table 20), we can learn that a lot of time, almost 35%, of the total number of cycles, is spent in the memory allocation when adding new buffers to the pool.

| Function                    | Cycles | % of total |
|-----------------------------|--------|------------|
| malloc                      | 2215   | 34.65%     |
| search_buf_by_range_nocopy  | 1528   | 23.90%     |
| append_buf                  | 940    | 14.70%     |
| memcpy                      | 702    | 10.98%     |
| main _main                  | 490    | 7.66%      |
| remove_buf                  | 214    | 3.35%      |

Table 20: ChessDE profiling information.

Another important observation is that the application contains many 64 bit operations. These are emulated as dual precision operations, making use of 32 bit instructions. For example, the important address range check

```c
if(p->VirtAddr<=start_addr && end_addr<(p->VirtAddr+p->Len-1))
```

requires 23 DLX instructions to implement it.

### 4.4.2 Implementation on D64

A first important step that is required to achieve a speedup of the buffer management code is the extension of the data width of the processor. A variant of the DLX architecture, which we call **D64**, has been created to achieve this purpose. The **D64** has the following features:

- The width of the central register file is increased from 32 to 64 bit. This allows to store 64 bit data in a single register field. The 64 bit values can be used to store the virtual addresses that are present in the packet headers.

- The width of the ALU has been increased from 32 to 64 bit. While all 32 bit op codes are still supported, new opcodes have been added to the following operations:
- long addition (ladd);
- long subtraction (lsub);
- long addition with 16 bit signed and unsigned immediate operand (laddi, laddui);
- long subtraction with 16 bit signed and unsigned immediate operand (lsubi, lsubui);
- long logical left shift (lsll);
- long logical left shift with immediate shift factor (lsll);
- long signed and unsigned compare instructions (lsge, lsgeu, lsgt, lsgtu, lsle, lsleu, lslt, lsltui).

- long signed and unsigned compare instructions with immediate operand (lsgei, lsgeui, lsgti, lsgtui, lslei, lsleui, lslt, lsltui).

- The bitwise logical operations AND, OR and XOR, are only present in a 64 bit form. These 64 operations can also be used to implement 32 bit bitwise operations.

- The arithmetic and logical right shift operations are only present in a 64 bit form. These 64 operations can also be used to implement 32 bit shift operations.

- The size of the multiplier is kept at 32x32 bit. Indeed, multiplication is not a critical operation in the buffer manipulation code. Allocating a 64x64 bit multiplier would significantly increase the size of the design. It would also have a negative impact on the achievable clock frequency, or would require a deeper pipeline.

- The width of the data memory interface has been extended to 64 bit, and 64 bit load and store instructions have been added.

Concerning the use of the 64 bit architecture by the C compiler, following decisions were made:

- The 64 bit data type is used to implement the C built in types long long and unsigned long long. The unsigned long long type in its turn, is used in the buffer manipulation code to represent 64 bit addresses.

- The 32 bit type is kept for representing the int, unsigned, long and unsigned long C types, as well as pointers (the D64 still has a 32 bit address bus).

The results obtained for the benchmark code on the D64 architecture are captured in third column of table Table 19.

- The append function does not benefit from the 64 bit instruction. This is because most of the time is spent in malloc. The malloc function still exclusively uses 32 bit data and instructions. This is so because addresses on D64 are still 32 bit, which is sufficient because the data structures that need to be manipulated are limited in size.

- The search and remove functions do benefit from the 64 bit instructions. The address range check now requires 10 instructions.
To further specialize the D64 architecture we will add an address compare instruction. A new functional unit, called ACU, specialized for doing 64 bit address range compares is added. The unit implements the following operation:

```c
w64 check_addr_in_range(w64 start, w64 end, w64 VirtAddr, w64 Len)
{
    return VirtAddr <= start && end <= (VirtAddr + Len - 1);
}
```

The register file of the DLX architecture has only two read ports. The address compare unit on the other hand, needs four operands. Because it would be too costly to add two additional read ports for accessing the complete register file, we have decided to read the VirtAddr and Len parameters from dedicated fields R12 and R13. This is modeled as follows in the processor model:

```c
opn rdS1(r: c5u) {
    action: stage ID: pS1=r1=R[r]; syntax: "r"r; image: r;
}
opn rdS2(r: c5u) {
    action: stage ID: pS2=r2=R[r]; syntax: "r"r; image: r;
}
opn rdS12() {
    action: stage ID: pS12=r12=R12; syntax: "r12";
}
opn rdS13() {
    action: stage ID: pS13=r13=R13; syntax: "r13";
}

opn alu_check_addr(d1: wrD1, s1: rdS1, s2: rdS2, s12: rdS12, s13: rdS13) {
    action {
    stage ID: // read operands
        s1;
        s2;
        s12;
        s13;
    stage EX: // execute range check
        acuA=pS1;
        acuB=pS2;
        acuC=pS12;
        acuD=pS13;
        acuX = check_addr_in_range(acuA,acuB,acuC,acuD);
        pd1w = acuX;
    stage EX..WB: // write back result
```
As can be seen in column D64AC of table Table 19, adding the ACU has little impact in the cycle count. The unit will however be an important component in the following architecture.

### 4.4.4 Dedicated Storages for the Buffer Table

The main inefficiencies that still remain can be attributed to the fact that the pool of buffers is still allocated as a linked list in memory.

- A first consequence is that the append operation calls `malloc`, which is time consuming.
- Secondly, the `VirtAddr` and `Len` inputs of the address range check need to be loaded from memory. Since DLX has only one memory read port, these reads are executed sequentially.
- Going from one list element to the next during a search operation requires an additional load of the next pointer.

A fundamental solution to the problem is to allocate the buffer descriptors in a dedicated storage, in such a way that there is sufficient bandwidth to access all operands of the range check in parallel. For the application domain of scientific computing, it has been established that typical applications use only a limited number of large buffers. Typically, a network node will need to keep track of 10 to 20 buffers. Based on this property, we decided to implement the `buf_desc` record in dedicated registers files of 32 fields each. These register files, BVA, BLN, BFL and BMW are shown in figure 50.

The BVA register file is 64 bit wide and holds the virtual address of a buffer (the `VirtAddr` member of `buf_desc`).

The BLN register file is 32 bit wide and holds the length of a buffer (the `Len` member of `buf_desc`).

The BFL register file is 32 bit wide and holds the flags associated to a buffer (the `Flags` member of `buf_desc`).

The BMW register file is 64 bit wide and holds the magic word of a buffer (the `MagicWord` member of `buf_desc`).

In addition to these data registers, there is a single 32 bit register BM (buffer mask). Each BM bit indicates whether the corresponding fields in the BVA, BLN, BFL and BMW register are in use.

The BI register is a 5 bit pointer register that is used to select a common field in the BVA, BLN, BFL and BMW registers, as well as select a bit of the BM mask.
Finally, there is a condition register BC. BC is set or cleared by the instructions that manipulate the buffer storages to indicate whether the instruction was successful or not.

4.4.5 Instructions

In this section, we describe the instructions that were added to manipulate the buffer storages.

Instructions needed by the append operation.

- **bufffree** This instruction inspects the BM registers and looks for the first unused entry. When an unused entry is found, its index is written to BI and the corresponding BM bit is set to indicate that a new buffer descriptor will be written to this location. The instruction indicates that a free location was found by setting the BC condition register. When no unused entry was found, a false condition is written to BC. The C language intrinsic for this instruction is buf_free().

- **bufadd** This instruction implements a 4-way parallel write, from the central register file, to the buffer descriptor fields that are pointed to by BI. The VirtAddr and Len parameters can be read from any field of the central register file. The Flags and MagicWord parameters are read from dedicated registers R12 and R13 respectively.

- **bbc/bnbc** This is a conditional jump, which jumps if the BC register is set (bbc) or not set (bnbc).

The C implementation of the add operation is given below:

```c
buf_add(unsigned long long virt_addr,
        unsigned len,
        unsigned flags,
        unsigned long long magic_word)
```
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Grant Agreement no.: **247846**
Call: FP7-ICT-2009-4 Objective: FET - ICT-2009.8.1 Concurrent Tera-device Computing

```c
{
    bool ok = buf_free();
    if (ok) {
        *pVA = virt_addr; // pVA is a pointer to BVA
        *pLN = len;
        *pFL = flags;
        *pMW = magic_word;
    }
    return ok;
}
```

This C code maps into the following instruction sequence:

- **buffree**
- **bnbc #next**
- **bufadd r4,r5,r12,r13**
- **next: ...**

*Instructions needed by the append operation.*

- **mv bi,<imm5>** This instruction loads a 5 bit immediate value into the BI register. It is mainly used at the start of a search to set BI to zero.
- **bufnxt** This instruction inspects the BM registers and looks for the first used entry. When a used entry is found, its index is written to BI. The instruction then also sets the BC register. When no used entry was found, a false condition is written to BC. The C intrinsic for this instruction is called `buf_next()`.
- **bufmv Rn,[bva,bln]** This instruction moves the fields of the BVA and BLN registers filed that are pointer to by the current BI index to a filed in the central register file.
- **bufrng** This instruction performs the address range check on operands that are stored in the central register file. The matching condition is written to the central register file. The C intrinsic for this instruction is called `buf_check_addr_in_range()`.

The C implementation of the search operation is given below:

```c
inline bool buf_search(unsigned long long start_addr,
                        unsigned long long end_addr,
                        unsigned long long& virt_addr,
                        unsigned& len,
                        unsigned& flags,
                        unsigned long long& magic_word)
{
    buf_first();
    int ret = 0;
```
for (int i = 0; i<32; i++) {
    if (buf_next()) {
        if (buf_check_addr_in_range(start_addr,
                               end_addr,
                               *pVA,
                               *pLN)) {
            virt_addr = *pVA;
            len = *pLN;
            flags = *pFL;
            magic_word = *pMW;
            ret = 1;
            break;
        }
    }
}
return ret;

This C code maps into the following instruction sequence:

bufnxt ; locate next used buffer entry
bnbc, #13 ; skip range check if not found
nop
nop
bufmv r12,bva ; move buffer parameters to R
bufmv r13,bln
bufrng r11,r2,r8,r12,r13 ; range check
beqz r11,#7 ; skip if no match
nop
nop
bufmv r11,bln ; copy parameters when match
bufmv r14,bfl
bufmv r8,bmw
ori r16,r0,#1
j #7
bufmv r2,bva
addi r9,r9,#1
slt r11,r9,#32
bnez r11,#-20 ; loop back

Instructions needed by the remove operation.

- **bufeq** This instruction evaluates whether two sets of address parameters (virtual address and length) are equal. It is used to check if a certain buffer is present in the BVA/BLN registers. The C intrinsic for this instruction is called `buf_check_buf_equal()`.
• **bufrem** This instruction clears the bit in the BM register that is pointed to by the BI index. The C intrinsic for this instruction is called `buf_rem()`.

The C implementation of the remove operation is given below:

```c
inline bool buf_remove(unsigned long long virt_addr,
                        unsigned len)
{
    buf_first();
    for (int i = 0; i<32; i++) {
        if (buf_next()) {
            if(buf_check_buf_equal(virt_addr,len,*pVA,*pLN)) {
                buf_rem();
                return 1;
            }
        }
    }
    return 0;
}
```

This C code maps into the following instruction sequence:

```
bufnxt ; locate next used buffer entry
bnbcc, #9 ; skip equal check if not found
nop
nop
bufmv r12,bva ; move buffer parameters to R
bufmv r13,bln
bufeq r11,r0,r14,r12,r13 ; equal test
beqz r11,#3
nop
nop
j #6
bufrem ; remove by clearing mask register
addi r2,r2,#1
slt r11,r2,#32
bnez r11,#-16
```

### 4.4.5.1 Results

The results obtained for the benchmark code on the architecture with the dedicated storages are captured in fifth column "D64SB" of Table[19]. This architecture update has a significant impact on all operations that are in the benchmark code.

• The append function no longer calls `malloc()`. The `buffree` and `bufadd` instructions are single
cycle instructions. This has led to a speedup of a factor 11.6.

• For the search and remove functions, the dedicated storages and the hardware intrinsics for range and equal tests have led to a speedup of 3.1 and 2.4 respectively.

The overall improvement for the complete benchmark is a factor 3.6. In the following section, we will present further architecture improvements that will improve the speedup even further.

4.4.6 Further Architecture Improvements

The D64SB architecture still has three areas of inefficiency:

• The address compare unit reads operands from the central register file. The two operands that are related to the buffer pool therefore have to be moved from the BVA and BLN registers to the central register file. This is done in separate instructions.

• The results of a search operation (virtual address, buffer length, flags and magic word) need to be copied from the dedicated registers to the data structures of the application program, which typically reside in memory. Currently this is done in two steps:
  – from the dedicated registers to the central register file;
  – from the central register file to memory;

• The conditional branch instruction requires three cycles to fetch the target instruction. One cycle to execute the branch and two cycles which are implemented as delay slots. In the buffer search code, there are no useful instructions that can be scheduled in the delay slots. We will therefore look for architecture improvements with which we can reduce the number of conditional branches.

Following instructions have been added in this architecture variant:

• **bufrngbd** and **bufeqbd**. These are variants of bufrng and bufeq, but differ in two ways:
  – The operands are read directly from the BVA and BLN registers. This will avoid register moves.
  – The resulting conditions are not stored in the central register file, but are written to a second dedicated condition register RC.

• **sva**, **sln**, **sfl** and **smv**. These are store instructions, which directly store a value from a BVA, BLN, BFL or BWM register to the memory. The indexed addressing mode of DLX is used to provide the memory address.

• **bend** and **bnend**. The bend instruction is a conditional branch which tests the BC condition register (next buffer found) and the RC condition register (range or equal match), according to the following predicate:
It is used to terminate the search loop when all new buffers have been tested ( !BC) or when a match is found (BC & RC). The bnend instruction tests the complementary predicate.

• **band** and **bnand**. The bend instruction is a conditional branch which tests the BC and the RC condition registers according to the following predicate: BC & RC. It is used after the search loop, to test if valid match was found. The bnend instruction tests the complementary predicate.

The C implementation of the search operation can now be programmed as follows:

```c
inline bool buf_search(unsigned long long start_addr,
                        unsigned long long end_addr,
                        unsigned* presult)
{
    buf_first();
    int ret = 0;
    dlx_primitive::uint1 found;
    dlx_primitive::uint1 match;
    do {
        found = buf_next_bool();
        match = check_addr_in_range_bool(start_addr,
                                           end_addr,
                                           *pVA,
                                           *pLN);
    } while (!buf_end(found, match));
    if (buf_and(found, match)) {
        *((unsigned long long*)presult) = *pVA;
        presult += 2;
        *((unsigned*)presult) = *pLN;
        presult += 1;
        *((unsigned*)presult) = *pFL;
        presult += 1;
        *((unsigned long long*)presult) = *pMW;
        ret = 1;
    }
    return ret;
}
```

Note that the buf_search function now has an argument which is a pointer result, to the user data structure that holds the buffer parameters; and that the results are copied directly from the buffer storages to the user space.

Given these new instructions, the search loop reduces to the following instructions:

```c
bufnxt ; locate next used buffer entry
```
bufrngbd r2,r5 ; range check
bnend, #-4 ; loop back when not found
nop
nop

The results obtained for the benchmark code on the architecture with the dedicated storages are captured in the sixth column of Table 19. Compared to the D64SB versions, there is an improvement of a factor 2.6 for the search and remove operations.

### 4.5 Hardware Characteristics

In order to gain insight in the hardware cost of the architecture specialization, in a first experiment an RTL implementation of the different DLX variants was generated with the IP Designer tool-suite and subsequently synthesized into a standard cell based implementation. The target library uses a 65nm general purpose technology. As a synthesis tool, Synopsys DC Expert was used. For a target frequency of 200MHz, the gate count results shown in Table 21 were obtained.

| DLX | D64 | D64AC | D64SB | D64OPT |
|-----|-----|-------|-------|--------|
| 34722| 42700| 44152 | 101987| 107712 |

Table 21: Gate counts for different ASIP architectures.

The gate count increase from the 32 bit to the 64 bit data path and register file is 23%, which is reasonable. The cost of the ACU is 3% of the total cost of D64AC, which can also be considered a small increase. A big increase in gate count, of a factor 2.3, can be found in the designs to which the dedicated storages were added. However, this hardware cost pays off since these architectures also give the best acceleration of the application code.

Note that, while these results were obtained for a clock frequency of 200 MHz, the maximal achievable frequency for this design in the 65nm technology is 330 MHz.

The D64OPT design was also mapped onto FPGAs. For a first mapping on Altera Cyclone V (device type 5CEFA7F23I7), the logic utilization was at 13%, while the maximum frequency was 93 MHz (table 22).

For a second mapping on Altera Stratix V, the maximum clock frequency is 180 MHz, which is approximately the same frequency at which the Nios II core is clocked.

### 4.6 Conclusion and Next Steps

In this chapter of the deliverable report, we described the design of an ASIP to accelerate the DNP functionality, with the aim of reducing the latency of RDMA transfers. The new DNP ASIP architecture
includes the basic functionality of a 32-bit microprocessor. The architecture has been further optimized in a stepwise refinement process, analyzing e.g. the cycle count and storage profiles produced by the IP Designer tool-suite.

Key architectural features of the DNP ASIP include support for 64-bit operations, a dedicated register-file structure for efficient data buffer storage, and a dedicated address generation unit with a 64-bit range instruction.

The DNP ASIP can be programmed in C using IP Designer’s retargetable C compiler. For buffer management, intrinsic function calls are available in C code, e.g. to locate the next active entry in the buffer table, or to perform address range comparisons.

Benchmark buffer-search programs were compiled on the new DNP ASIP architecture. Results show a cycle-count reduction by more than 85% compared to the existing implementation on the Nios II microprocessor. The clock frequency of the ASIP is comparable to that of Nios II. Therefore the buffer search already executes significantly faster on the ASIP compared to NIOS. Further cycle-time improvements are within reach.

Further extensions of the DNP ASIP are planned in the next project period. First we will investigate to what extent dedicated functional units, storages and instructions can speed up the execution of virtual-to-
physical memory address translation. Secondly we will investigate if more data computation (as opposed to data communication) support can be integrated in the DNP ASIP. Possible extensions could include the addition of a floating-point unit or a bit-manipulation unit in the ASIP.
5 Development on 28nm FPGA

5.1 DNP on Altera Development kit Stratix V

Stratix V FPGA is an Altera 28-nm device, which has an enhanced core architecture and offers up to 66 integrated 14.1 Gbps transceivers. Moreover, its design advancements such as the PCIe HARD IP implementation, partial reconfiguration and programmable power technology, ensure that designs implemented in the Stratix V GX FPGAs operate faster, with lower power consumption than in previous FPGA families.

We ran a preliminary synthesis of APEnet+ on the Stratix V; some changes to the APEnet+ firmware have been performed to adapt the hardware code to a different FPGA family.

The main responsible of the management of PCIe interface are Altera PCIe HARD IP and PLDA core. For the past generation of FPGA, Altera provided the ALTGX megafunction as a general purpose transceiver solution. On the contrary, the Stratix V family offers protocol-specific IPs, which guarantee high performance and simplify the parameterization process. The PCIe HARD IP supports Gen3, Gen2, and Gen1 end point and root port up to x8 lane configurations. Current implementation provides a PCIe HARD IP in Gen2 mode (5.0 Gbps/lane), but we plan the development of a new version that takes advantage of Gen3 data rate (8.0 Gbps/lane).

Stratix V HARD IP for PCIe includes an embedded reset controller and provides an Avalon interface to access to the Application Layer (for more information about the Avalon protocol refer to http://www.altera.com/literature/manual/mnl_avalon_spec.pdf).

The multi-port DMA engine for PCIe for Altera Devices is a PLDA IP; the core PLDA wraps around Altera PCIe HARD IP and leverages on the renowned PLDA EZDMA interface, providing multi-channel DMA capability.

The **TORUS LINK** block is composed by an Altera Custom IP Core with the correspondent reconfiguration block, and a proprietary channel control logic (SYNC_CTRL) (as shown in figure [51]). The Altera transceiver supports proprietary protocols and implements 4 bi-directional lanes bonded into a single channel. On the receiving side each transceiver includes Word Aligner, Deskew FIFO, 8B/10B decoder, Byte Ordering Block and RX phase compensation FIFO. The Deserializer clocks serial input data using the high-speed serial clock recovered from the receiver clock data recovery (CDR) block, and deserializes the data using the low-speed parallel recovered clock. The Word Aligner receives parallel data from the Deserializer and restores the word boundary based on a pre-defined alignment pattern that must be received during link synchronization. In Stratix IV design the word alignment operation was manually controlled by the input signal rx_enapatternalign: a rising edge on the rx_enapatternalign signal triggers the Word Aligner to look for the word alignment pattern in the received data stream.

In Stratix V Custom IP rx_enapatternalign is a status register that can be asserted using the Avalon interface. In the current implementation of the DNP on Stratix V, we used the automatic synchronization State Machine mode Word Aligner. The status ports rx_syncstatus high indicates that synchro-
nization is acquired. The Deskew FIFO circuitry is able to align the data across multiple lanes. Unfortunately this circuitry is available only in XAUI protocol, thus we implement our DESKEW FIFOs connected to the lanes of the channels. The rate match FIFO compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks. The 8B/10B decoder receives 10-bit data from the Word Aligner and decodes it into 2-bit control identifier and 8-bit data; this data may or may not match the original byte ordering of the transmitted data. The byte ordering looks for the user-programmed byte ordering pattern in the parallel data: if it finds the byte ordering pattern in the MSB position of the data, it inserts pad bytes to push the byte ordering pattern to the LSB(s) position, thereby restoring proper byte ordering. Finally, the RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric clock. Similarly on the transmitter side each transceiver includes TX phase compensation FIFO, 8B/10B encoder and Serializer.
To ensure the correct initialization of the Custom IP Core, a right reset sequence has to be followed. In Stratix IV design we implemented a custom reset controller block to reset the ALTGX Transceiver; Stratix V's Custom IP allows to implement an external reset controller logic with a sequence very similar to the Stratix IV ALTGX's one, but it also supplies an embedded reset control which automatically performs the entire transceiver's reset sequence. After reset sequence is completed the tx_ready and rx_ready status signals are asserted, and the Sync_ctrl can start the synchronization’s procedure: transceivers of different nodes connected together have to be align to allow a correct data transmission.

\[\text{Sync_ctrl} \text{ sends the alignment pattern } \text{Align Word} \text{ for a constant number of clock cycles (Check Align phase), at the same time looking for the same word in the received data stream. If } \text{Align Word} \text{ is received, this block signals that synchronization is acquired by sending the } \text{Align_ok Word}, \text{ otherwise the Check Align phase restarts after the Restart Align state. When both nodes are aligned and receive the Align_ok Word, channel alignment is assured and the deskewing operation starts: Desk_FIFO write enable is asserted, while the read enable signal is asserted when all FIFOs are no longer empty.}\]

We developed the APEnet+ design on the Altera DK-DEV-5SGXEA7N development kit, a complete design environment that features a Stratix V GX FPGA (5SGXEA7K2F40C2N). This kit also includes a PCIe slot, a 40G QSFP connector and two HSMC ports (figure 52).

![Architecture of APEnet+'s channel.](image)

The PCIe edge connector supports up to x8 signaling in either Gen1, Gen2, or Gen3 mode.
The QSFP connector uses four transceiver lanes from the FPGA device; we used this component to achieve the X+ channel. The signal generated by a 282.500 MHz on-board oscillator is used as a reference clock; in the next versions we will use the 644.53125 MHz on-board oscillator.

The development board contains also two High-Speed Mezzanine Card (HSMC) connectors, called port A and port B, to provide 8 channels in port A and 4 channels in port B of 10.0 Gbps transceivers. Both ports use a 625.000 MHz on-board oscillator as reference clock, and can be removed or included in the active JTAG chain by means of a DIP switch.

In Table 24 is shown the Altera Quartus II synthesis report for our system.

| Logic utilization (in ALMs)  | 37,345 / 234,720 (16%) |
|------------------------------|------------------------|
| Dedicated logic registers     | 56,834 (12%)           |
| Total pins                   | 215 / 864 (25%)        |
| Total block memory bits      | 7,450,168 / 52,428,800 (14%) |
| DSP block                    | 2 / 256 (< 1%)         |
| Total PLLs                   | 28 / 80 (35%)          |

Table 24: Stratix V logic usage overview.
6 Glossary

The following table contains acronyms and terms used in this document.

| Acronym | Definition |
|---------|------------|
| AED     | Abstract Execution Device. |
| ALUT    | Adaptive LookUp Table. |
| API     | Application Programming Interface. |
| APEnet+ | An FPGA-based card for low latency, high bandwidth direct network interconnection based on the DNP. |
| ASIP    | Application Specific Instruction Set Processor. |
| BER     | Bit Error Rate. |
| BFS     | Breadth-First Search. |
| BML     | Byte Management Layer, framework of the OpenMPI library. |
| BTL     | Byte Transfer Layer, framework of the OpenMPI library. |
| CDR     | Clock Data Recovery. |
| CPLD    | Complex Programmable Logic Device. |
| CQ      | Completion Queue. |
| CRC     | Cyclic Redundancy Check. |
| DAL     | Distributed Application Layer. |
| DFM     | DNP Fault Manager. |
| DNAOS   | DNA is Not just Another Operating System. |
| DNP     | Distributed Network Processor, it is the core of the APEnet+ board. |
| DPSNN   | Distributed Polychronous Spiking Neural Networks (a PSNN code natively redesigned and rewritten to exploit parallel/distributed computing systems). |
| DWR     | DNP Watchdog Register. |
| ECC     | Error Correcting Code. |
| ELF     | Extensible Linking Format. |
| EURETILE | European Reference Tiled Architecture Experiment. |
| FIT     | Failures In Time. |
| FLOPS   | Floating-point Operations Per Second. |
| FM      | Fault Manager. |
| FPGA    | Field-Programmable Gate Array. |
| HAL     | Hardware Abstraction Layer. |
| HCA     | Host Channel Adapters. |
| HDS     | Hardware dependent Software. |
| HFM     | Host Fault Manager. |
| HPC     | High Performance Computing. |
| HW      | Hardware. |
| HWR     | Host Watchdog Register. |
| IC      | Integrated Circuit. |
| IDE     | Integrated Development Environment (tools to develop and debug embedded software, integrated in a GUI). |
| Acronym | Description |
|---------|-------------|
| INFN    | Istituto Nazionale di Fisica Nucleare (National Institute for Nuclear Physics). |
| I/O     | Input/Output. |
| IOCTL   | Input/Output Control, is a system call for device-specific input/output operations and other operations which cannot be expressed by regular system calls. |
| IP      | Intellectual Property. |
| IP Designer | TARGET's tool-suite for the design and programming of ASIPs. |
| IPMI    | Intelligent Platform Management Interface. |
| ISS     | Instruction Set Simulator. |
| IT      | Information Technology. |
| LDM     | LiFaMa Diagnostic Message. |
| LiFaMa  | Link Fault Manager. |
| LO/FA/MO| Local Fault Monitor, an HW/SW approach to obtain Systemic Fault Awareness. |
| LQCD    | Lattice Quantum-ChromoDynamics. |
| LSB     | Least Significant Bit. |
| LTP     | Long Term synaptic Potentiation. |
| LUT     | Look-Up Table. |
| MM      | Memory Management. |
| MPI     | Message Passing Interface. |
| MP-SoC  | MultiProcessor System-on-Chip. |
| MSB     | Most Significant Byte. |
| MTL     | Matching Transport Layer, framework of the OpenMPI library. |
| NIC     | Network Interface Controller. |
| NIOS II | 32-bit microprocessor available as soft-core in Altera FPGAs (often shorthanded as "NIOS"). |
| nML     | Not a Modelling Language (a processor architectural description language). |
| OMPi    | Open MPI, an implementation of the MPI standard. |
| OPAL    | Point-to-point Message Layer. |
| ORTE    | Open Run-time Environment, part of the OpenMPI library. |
| OS      | Operating System. |
| OSI     | Open Systems Interconnection. |
| OSU     | Ohio State University. |
| OMB     | OSU Micro-Benchmarks. |
| PCS     | Physical Coding Sublayer. |
| PCU     | Processor Control Unit. |
| PDC     | Pin-Down Cache. |
| PDG     | Primitives Definition and Generation. |
| PMA     | Physical Medium Attachment. |
| PML     | Point-to-point Message Layer, framework of the OpenMPI library. |
| Presto  | MPI-like library for APEnet+/DNP. |
| PRBS    | Pseudorandom Binary Sequence. |
| PSNN    | Polychronous Spiking Neural Network. |
| Abbreviation | Description |
|--------------|-------------|
| P2P          | peer-to-peer. |
| QUonG        | LQCD on GPU platform. |
| RB           | Ring Buffer. |
| RDMA         | Remote Direct Memory Access. |
| RDMA GET     | RDMA READ operation that implies an handshake between the sender and the receiver. |
| RDMA PUT     | RDMA WRITE operation that implies an handshake between the sender and the receiver. |
| RTL          | Register Transfer Level (also used to refer to register-transfer languages, such as VHDL or Verilog) |
| RX           | Receive. |
| SIMD         | Single Instruction Multiple Data (also known as vector processing, a processor architectural concept to implement data-level parallelism). |
| SIP          | Software Interface Protocol. |
| SNET         | Service Network. |
| STDP         | synaptic Spiking Time Dependent Plasticity. |
| SW           | Software. |
| TCL          | Tool Command Language. |
| T&D          | Test & Debug. |
| TX           | Transmission. |
| UDP          | User Datagram Protocol. |
| V2P          | Virtual To Physical. |
| VEP          | Virtual EURETILE Platform. |
| VHDL         | VHSIC Hardware Description Language. |
| WD           | WatchDog. |
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