Impact of body-biasing for negative capacitance field-effect transistor

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Abstract

In this study, the body-bias effects on negative capacitance FET (NCFET) are analyzed using technology computer-aided design (TCAD) device simulation with drift-diffusion model and Landau-Khalatnikov. To understand the physical origin the effects, electrical characteristics are evaluated with various ferroelectric (FE) layer thickness for NCFET as compared to the conventional MOSFET. With thicker FE layer, the total capacitance ($C_{\text{total}}$) becomes larger, while MOS capacitance ($C_{\text{MOS}}$) is sustained, leading to voltage amplification because the difference between $C_{\text{FE}}$ and $C_{\text{MOS}}$ gets smaller. It gives the strong gate controllability and less sensitivity for threshold voltage ($V_{\text{TH}}$) according to body-bias variations unlike the conventional MOSFET. Moreover, it is confirmed that the surface band-bending at the interface of NCFET is rarely changed with changing body-bias from 0V to $-3V$.

1. Introduction

Over the several decades, supply voltage ($V_{\text{DD}}$) has been successfully reduced with continual miniaturization of CMOS devices. Unfortunately, it is no longer sustained for sub-45 nm due to short channel effects (SCEs) and subthreshold swing (SS) limitation [1, 2]. Nevertheless, the demands for $V_{\text{DD}}$ scaling and energy efficiency have been extensively increasing for complementary MOS (CMOS) technology. Thus, many researchers have investigated steep SS devices such as impact-ionization FET (1-MOS), tunnel FET, and negative capacitance FET (NCFET) as a breakthrough [3–13]. Among those devices, NCFET has recently attracted much attention for low power CMOS applications because it is perfectly compatible with conventional CMOS process. NCFETs can be fabricated by replacing only the high-$\kappa$ gate dielectric with ferroelectric (FE) layer in conventional MOSFET process without additional process changes.

The basic operation concept of NCFET is utilizing the polarization in the FE layer. The polarization-induced negative differential capacitance amplifies the gate voltage, which leads to SS of sub-60 mV dec$^{-1}$ at room temperature. Therefore, to scale down $V_{\text{DD}}$, most studies have been mainly focused on how NCFET can show the better SS and on-current than previous CMOS devices by handling various FE materials with different compositions [6, 14]. However, there are a few reports about the intrinsic characteristics on NCFET such as body-bias effects and reliability. Hence, numerous fundamental understandings should be required in advance for integrated circuit (IC) chip applications with diverse functionalities. Particularly, body-bias technique is very important to control threshold voltage ($V_{\text{TH}}$) in logic applications where multiple $V_{\text{TH}}$ are utilized because circuit speed as well as power consumption can be improved by optimizing $V_{\text{TH}}$ [15–17]. In 2017, there is a report for back-gate biasing effects of 2D material-based NCFET which is studied considering the body-bias with thin insulator (BOX) underlying channel regions, not substrate biasing [18].

In this study, the effects of body-bias (i.e., substrate biasing) for Si-based NCFETs are investigated with technology computer-aided design (TCAD) simulations. To clearly understand the underlying physical origin of the body-bias effects, a planar NCFET with long channel of 100 nm is intentionally adapted to exclude SCEs for
the simplicity. Then, the body-bias ($V_B$)-induced $V_{TH}$ change by various FE thickness is analyzed and compared to that of conventional planar MOSFET which is well known for body-bias effects.

2. Simulation model and parameters

The schematic of the bulk silicon planar NCFET analyzed in this study is depicted in figure 1(a). Key structure parameters are designated that gate length ($L_G$), interfacial oxide thickness ($T_OX$), and body thickness ($T_BODY$) are 100 nm, 1 nm, and 100 nm, respectively. Also, the dopant concentrations of source/drain ($2 \times 10^{20} \text{cm}^{-3}$) and body ($5 \times 10^{17} \text{cm}^{-3}$) regions are applied. For the FE material, HfZrO$_2$ (HZO) with 25 dielectric constant is used on the SiO$_2$ interfacial oxide (IL) and its thickness varies from 4 nm to 7 nm to evaluate the effects of body-bias. All device evaluations are performed by commercial TCAD tool (Synopsys Sentaurus$^{TM}$) [19]. In order to reflect polarization effects in the FE material, Poisson’s and carrier continuity equations are self-consistently calculated with Landau-Khalatnikov model which has the relationship between electric field and polarization in
thickness, it is clearly observed that there is hysteresis in the first hysteretic drain current.

3. Results and discussion

Figure 1(a) shows the equivalent capacitance model of NCFETs. Typically, NCFETs can be represented with three capacitance components: (1) FE capacitance ($C_{FE}$); (2) SiO$_2$ IL capacitance ($C_{OX}$); and (3) semiconductor capacitance ($C_S$). Therefore, the potential difference between the gate and the body is written as below:

$$V_{GS} - V_{FB} = V_{FE} + V_{MOS} = \frac{Q_G}{C_{FE}} + \frac{Q_G}{C_{MOS}}$$

where $Q_G$ and $C_{MOS}$ represent total gate charge and $C_{MOS}^{-1} = C_{OX}^{-1} + C_S^{-1}$, respectively.

3. Results and discussion

First, hysteretic drain current ($I_{DS}$)-gate voltage ($V_{GS}$) characteristics are investigated using forward and reverse $V_G$ sweepings for FE thickness from 6 nm to 12 nm to confirm hysteresis-free FE thickness. From 10 nm FE thickness, it is clearly observed that there is hysteresis in the $I_{DS}$- $V_G$ characteristics as shown in figure 1(c).

Hence, in this work, FE thickness under 7 nm is considered for hysteresis-free operations. Then, to confirm the polarization effects, the $Q_{FE}$- $V_{FE}$ characteristics over the FE layer are evaluated with various FE thickness. Figure 1(d) shows that there is the negative slope (namely, negative capacitance: NC) regardless of FE thickness and the slope becomes steeper with the thinner FE layer. In terms of voltage amplification by the NC [i.e., $A_V = |C_{FE}|/(|C_{FE}|-C_{MOS})$], figure 1(e) indicates that the thicker FE can have the larger voltage amplification because the difference between $|C_{FE}|$ and $C_{MOS}$ is smaller. Especially, in the case of 7 nm FE, it is found that the voltage amplification can be obtained by around 5 times than applied voltage. Notably, this voltage amplification is not constant since both $C_{FE}$ and $C_{MOS}$ are changeable with respect to $V_{GS}$.

Figure 2(a) shows $I_{DS}$- $V_G$ characteristics with various FE thickness at $V_{DS} = 50$ mV. Although all the $I_{DS}$ are similar till $V_{GS} = 0.4$ V regardless of FE thickness, SS and on-current get remarkably improved beyond $V_{GS} = 0.4$ V with the thicker FE since the voltage amplification starts to occur from around $V_{GS} = 0.4$ V and the thicker FE has the larger voltage amplification as shown in figure 2(b). These polarization effects are also observed in the changes of the $C_{Total}$ and the $C_{MOS}$ with respect to $V_{GS}$. Here, the $C_{Total}$ is the total capacitance in which the $C_{FE}$ and the $C_{MOS}$ are connected in series (Inset of figure 2(b)). Figure 2(b) shows that the $C_{Total}$ is more enhanced with the thicker FE although the $C_{MOS}$ keeps unchanged because all the NCFETs with different
FE thickness are identical except for the FE layer thickness, which is consistent with the NC-induced voltage amplification. However, when $V_{GS}$ reaches to 1.0 V, there is no significant amplification for all FE thickness since the $C_{FE}$ starts to have positive values out of the NC region (figure 1(c)), which means that the NC effects disappear.

As a reference, conventional MOSFETs with the identical structure to the NCFET are also investigated with various HfO$_2$ thickness at $V_{DS} = 50$ mV as depicted in figure 3(a). In contrary to the NCFETs, the thicker HfO$_2$ induces the increase of equivalent oxide thickness (EOT), implying that $V_{TH}$ gets increased and on-current becomes degraded by the weaker gate controllability. Also, the $C_{Total}$-$V_G$ characteristics of figure 3(b) confirm that both inversion and minimum capacitances get reduced as EOT increases by thicker HfO$_2$.

To investigate the body-bias effects on NCFETs, the changes of the $I_{DSS}$-$V_G$, the $C_{Total}$-$V_G$, and the $C_{MOS}$-$V_G$ by various $V_{BIAS}$ (from 0 V to −3.0 V) are investigated in both NCFETs and conventional MOSFETs. Note that the NCFETs with 4 nm (small $A_V$) and 7 nm (large $A_V$) FE thickness are simulated to verify the effects of polarization or $A_V$ on the $V_{TH}$-induced changes of electrical characteristics. For the comparison, the conventional MOSFETs with HfO$_2$ thickness of 4 nm and 7 nm are also evaluated. Figures 4(a) and (c) show that the $V_{DS}$ of the conventional MOSFETs is positive-shifted by negative $V_{FB}$ (−$V_{FB}$) regardless of HfO$_2$ thickness and the thicker HfO$_2$ makes the $V_{TH}$ more shifted in the positive direction. This can be understood by classical MOSFET theory which explains that the surface potential ($\Phi_{surf}$) is determined by the coupling between $C_{Total}$ and channel depletion capacitance ($C_{Dep}$). Thus, the $V_{TH}$ shift in the positive direction by negatively increasing $V_{FB}$ is strongly correlated to the ratio of $C_{Dep}/C_{Total}$ and the MOSFET with thicker HfO$_2$ (smaller $C_{Total}$ and larger EOT in figures 4(b) and (d)) becomes more affected by $−V_{FB}$.

However, for the NCFET with 4 nm FE thickness, figure 5(a) shows that the $V_{TH}$ shift in the positive direction by $−V_{FB}$ is significantly reduced compared to that of the MOSFET. To analyze the $V_{TH}$ shift reduction, the $C_{Total}$-$V_G$ and the $C_{MOS}$-$V_G$ are separately extracted with respect to $−V_{FB}$. Although the $C_{MOS}$-$V_G$ is the same as that of the MOSFET, the $C_{Total}$ is enhanced by the NC-induced voltage amplification (see figure 5(b)), which leads to the reduction of the $V_{TH}$ shift by diminishing the $C_{Dep}/C_{Total}$. Interestingly, figure 5(c) indicates that there is almost no $V_{TH}$ change by $−V_{FB}$ in the NCFET with 7 nm FE layer. This phenomenon cannot be explained by classical MOSFET theory where the thicker gate dielectric accelerates the $V_{FB}$-induced $V_{TH}$ shift. The insensitive $V_{TH}$ change by $V_{FB}$ in the NCFET with the thicker FE can be also explained by the $C_{Total}$ enhancement. As shown in figure 5(d), the $C_{Total}$ gets more enhanced with the thicker FE layer by the larger voltage amplification and thus the $C_{Dep}/C_{Total}$ becomes small enough that the NCFET with the thicker FE can have the negligible $V_{FB}$-induced $V_{TH}$ change.

Furthermore, in the NCFET with 7 nm FE layer, the $I_{DSS}$ is hardly changed in subthreshold region whereas the on-current is reduced as $V_{FB}$ is negatively increased. The on-current reduction can be explained through the $C_{Total}$-$V_G$ and the $C_{MOS}$-$V_G$ characteristics. Figure 5(d) presents that the $C_{MOS}$ is positive-shifted by negatively increasing $V_{FB}$ and hence the $C_{Total}$ at the on-current region is reduced since the difference between $C_{FE}$ and $C_{MOS}$ becomes larger by the positive-shifted $C_{MOS}$. Consequently, the on-current decreases by the reduction of the $C_{Total}$ because the on-current is related to the charges ($Q$) induced in the channel and the $Q$ is determined by the integration of $C_{Total}$ multiplied by $V_G$.

Figures 6(a) and (b) summarize the dependence of $V_{RS}$ on $V_{TH}$ at $V_{DS} = 50$ mV for NCFETs and MOSFETs with various FE or HfO$_2$ thickness. Here, $V_{TH}$ is extracted by constant current method at $I_D = 100$ nA um$^{-1}$. In the NCFETs, it is observed that there is the smaller $V_{TH}$ sensitivity by the change of $V_{FB}$ with the thicker FE. Remarkably, the $V_{TH}$ shift of 52 mV by $V_{RS} = −3$ V is reduced to 9 mV when the FE thickness is increased from 4 nm to 7 nm. However, for the MOSFETs, the $V_{FB}$-induced $V_{TH}$ shift becomes much more sensitive with the thicker HfO$_2$ as compared to the NCFET and the $V_{TH}$ shift of 187 mV by $V_{RS} = −3$ V is increased to 250 mV.
when the HfO2 thickness is changed from 4 nm to 7 nm. In addition, the effects of L_G scaling are evaluated with L_G = 70 nm and 50 nm (figures 6(c)–(f)). For both NCFET and MOSFET, it is observed that the V_TH sensitivities are slightly changed by FE or HfO2 thickness variations regardless of the L_G. However, for NCFET, when the L_G decreases from 100 nm to 50 nm, the V_TH reduction by SCEs is much smaller than that of MOSFET.

Figure 4. For 4 nm HfO2 thickness, (a) I_D–V_G characteristics at V_D = 50 mV and (b) C_Total–V_G characteristics depending on V_BS. For 7 nm HfO2 thickness, (c) I_D–V_G characteristics and (d) C_Total–V_G characteristics depending on V_BS. By the increase of EOT, it shows larger V_TH sensitivity and smaller inversion capacitance (C_INV).

Figure 5. For 4 nm FE thickness, (a) I_D–V_G characteristics at V_D = 50 mV and (b) C_Total–V_G and C_MOX–V_G characteristics depending on V_BS. For 7 nm FE thickness, (c) I_D–V_G characteristics and (d) C_Total–V_G and C_MOX–V_G characteristics depending on V_BS. By large polarization effects, V_TH sensitivity is not observed in spite of the change of V_BS.
At $V_{BS} = 0 \text{V}$, the $V_{TH}$ reductions of 25 mV and 5 mV occur for 4 nm and 7 nm FE thickness, respectively. On the contrary, for MOSFET, the $V_{TH}$ reductions of 80 mV and 102 mV are observed with 4 nm and 7 nm HfO$_2$ thickness. As a result, the $V_{TH}$ of NCFET is less sensitive to $V_{BS}$ and $L_G$ scaling by the voltage amplification which makes the gate controllability stronger.

Figure 6. At $V_{DS} = 50 \text{mV}$, $V_{TH}$ sensitivity by negatively increasing $V_{BS}$ with thicker FE for NCFET and HfO$_2$ for MOSFET with $L_G = 100 \text{nm}, 70 \text{nm}$, and $50 \text{nm}$, respectively.

Figure 7. Based on 7 nm thickness, energy band diagrams along to the vertical direction with changing $V_{BS}$ at $V_{GS} = 0.4 \text{V}$ (a) for NCFET and (b) for MOSFET.
To figure out the $V_{TH}$ sensitivity for NCFETs and MOSFETs, energy band diagrams are investigated with 7 nm FE/HfO$_2$ thickness along the vertical direction at the center of Lg as shown in figure 7. In the energy band diagrams, both the NCFET and the MOSFET show the band rising at the body electrode when changing $V_{BS}$ from 0 V to $-3$ V. However, at the surface between SiO$_2$ and channel, the change of the energy band rarely occurs in the NCFET while the energy band rises up for the MOSFET, resulting in the difference of the $V_{TH}$ sensitivity between them. This comes from the stronger gate controllability by the NC-induced $C_{Total}$ enhancement in the NCFET, which reduces the change of the surface potential by $-V_B$ and thus mitigates the $V_B$-induced $V_{TH}$ change compared to the MOSFET.

4. Conclusion

In this study, the body-bias effects on NCFETs are analyzed using TCAD device simulations with the calibrated Landau-Khalatnikov model parameters. As contrast to conventional MOFETs, the $V_B$-induced $V_{TH}$ change is reduced with the thicker FE layer in NCFETs. Through the $C_{Total}$-$V_G$ and the $C_{MOS}$-$V_G$ analysis, it is found that the $C_{Total}$ becomes more enhanced by the larger NC-induced voltage amplification with the thicker FE and thus the $V_B$-induced $V_{TH}$ change is decreased by the reduction of the $C_{DVG}/C_{Total}$ (namely, the stronger gate controllability). To verify the hypothesis, energy band diagrams are examined for the NCFET and the MOSFET with 7 nm FE/HfO$_2$ thickness. It is revealed that the energy band at the surface is hardly changed by negatively increasing $V_{BS}$ in the NCFET. As a result, unlike MOSFETs, less $V_{TH}$ sensitivity on $V_{BS}$ should be considered by voltage amplification in terms of circuit design using NCFET.

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