Improved Energy Management System for Low-Voltage, Low-Power Energy Harvesting Sources

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Abstract. This paper focuses on improving the energy conversion process for low-voltage energy harvester powered wireless sensors by optimising the conversion stages for pulsed sensor operation. The proposed circuit has been designed to operate efficiently with both a low-voltage low-power energy harvester source and a low-power pulsed load. This ensures that continuous conversion losses are kept to a minimum and power is only delivered to the sensor when required. This has shown an increase in energy delivered to a sensor of up to 10% versus that of the best existing solution.

1. Introduction
Energy harvesting (EH) sources, including dye-sensitised solar cells (DSSCs), thermoelectric generators (TEGs), microbial fuel cells (MFC’s) and piezoelectrics, provide a low-cost, reliable and convenient solution to powering wireless sensors compared to both batteries and mains connections [1]. By utilising EH sources, wireless sensors can become autonomous and may be fitted in a larger range of locations when compared with conventional power sources. However, to date, power levels provided by EH sources have proven insufficient to enable fully autonomous sensor operation; this is explained by the combination of limited power production by EH sources and low power conversion efficiency due to low source voltage or current levels.

This paper focuses on improving the energy conversion process for low-voltage EH sources by optimising system operation for the pulsed nature of wireless sensor loads. The best performing step-up converter found for a solar cell powered wireless sensor is a boost converter operating under burst mode, with an efficiency of between 70% to 80%, depending on input lux [2]. Due to the low source power levels, efficiency is found to be limited by baseline losses associated with monitoring and control circuitry. In terms of sensor operation, many low-power wireless sensors operate in a pulsed manner consuming high levels of power (relative to the EH source) for short bursts of time. This means that conversion of the EH source voltage may only be needed during the time intervals when the wireless sensor is operating.

The circuit solution proposed in this work has been developed to exploit the pulsed nature of typical EH loads by reducing the operating on-time of voltage step-up converters and therefore the associated losses. It consists of a bank of energy storage supercapacitors connected directly to the EH source in a switched capacitor configuration. In this way, the circuit provides dual functionality of energy storage and voltage step-up conversion; it can be connected to supply a wireless sensor load directly or it can be fed into another converter stage, e.g. a boost converter, where its higher voltage...
can result in increased converter efficiency. For the latter, connection to the next conversion stage may be restricted to time intervals when the wireless sensor needs to complete an operation, thereby reducing baseline converter losses.

2. Switched Capacitor Energy Buffer

As discussed, wireless sensors operate in a pulsed manner to perform periodic sense and data transmission/store actions. For example a sensor might perform an action once every 15 minutes, remaining in low-power, sleep mode between actions. This operating mode is compatible with low-power EH sources whose energy can be built up to a sufficient level between each sense operation. However, many existing step-up conversion circuits for EH sources operate continuously to deliver energy to the load, with excess energy stored either in a capacitor, battery or a combination of both. These storage devices ensure that the wireless sensor has sufficient energy when the source is not available. However, due to ultra-low source power levels, baseline converter losses are significant and therefore a more optimum system design would allow the converter to deliver power only when required by the wireless sensor, while also delivering excess energy to a long-term storage element only during the sensor operating time.

![Figure 1: EH energy management system including a 2-stage switched capacitor energy buffer circuit.](image)

Figure 1 shows the circuitry involved in a 2-stage version of the proposed switched capacitor energy buffer block that supports such operation. The circuit is similar in operation to that of a series-parallel charge pump, [3] and [4], but supercapacitors [5] rather than regular capacitors are utilised (for C1, C2) to provide sufficient energy storage capacity, while their robustness under repeated charge-discharge cycling is superior to that of batteries. In comparison with regular charge pumps, the proposed circuit operates at a very low frequency, as seen in Figure 2, to match the long time periods between wireless sensor operations. Note that the number of switched capacitor stages can be varied depending on output voltage requirements.

![Figure 2: Switched capacitor output voltage for 2 and 4-capacitor circuits.](image)

The circuit operates in two states, charging and discharging, to maintain the EH source at its maximum power point (MPP), as outlined in Table 1. During the charging stage, supercapacitors C1 and C2 are in a parallel configuration and are charged directly from the energy harvesting source. Once
the voltage on the supercapacitors reaches a predetermined value set as the maximum power point (MPP) voltage + 10%, $V_{\text{MPP}+}$, the supercapacitors stop charging. At this point, $S_1$ and $S_3$ are open while $S_2$ and $S_4$ are closed, and the supercapacitors discharge to the load in a series connection. In this way, the output voltage is increased, doubled in the case of the circuit in Figure 1. The supercapacitor voltage is again monitored until the value reaches a predetermined minimum, MPP voltage – 10%, $V_{\text{MPP}-}$, when the switches are changed to the charging state and the cycle repeats. This hysteretic control method ensures that the energy harvesting source is kept at its MPP [6]. Figure 2 shows the output voltages of 2- and 4-cap implementations of the switched capacitor block of Figure 1.

3. Loss Analysis

Losses for the proposed switched capacitor block comprise of MOSFET conduction for each of the switches, S1-S4:

$$P_{\text{MOS,cond}} = I_{\text{rms}}^2 R_{\text{DS(on)}} \ , \ (1)$$

where $I_{\text{rms}}$ is the rms current through each MOSFET over a complete charge-discharge cycle and $R_{\text{DS(on)}}$ is their on-resistance. In addition there are MOSFET switching losses:

$$P_{\text{SW}} = \frac{t_{\text{sw, on}} V_{\text{out, peak}} F_{\text{sw}}}{2} + \frac{t_{\text{sw, off}} V_{\text{out, peak}} F_{\text{sw}}}{2} , \ (2)$$

where $F_{\text{sw}}$ is the switching frequency and $t_{\text{sw, on}}$ and $t_{\text{sw, off}}$ are the MOSFET turn-on and turn-off times respectively. Note that due to the large capacitance values applied, $F_{\text{sw}}$ is very low (approximately 30 mHz in this case), which reduces switching losses significantly compared to the other switched capacitor circuits [7].

The circuit also encounters significant capacitor related losses. As the circuit utilises supercapacitors, an accurate model is required to understand the losses within the supercapacitor structure. Figure 3 shows an equivalent circuit model of a supercapacitor [8], which shows that there are losses through multiple branches, each of which contributes losses of:

$$P_{\text{CAP,x}} = I_{\text{rms,x}}^2 R_x \ , \ (3)$$

where $x$ relates to the rms current and resistance of each branch over a complete switched capacitor cycle. Table 2 shows the equivalent circuit values that were obtained by characterising the supercapacitor according to methods described in [9]. Here, $R_{\text{ESR}}$ accounts for the usual internal interconnect and dielectric material losses, while $R_{\text{LEAKAGE}}$ accounts for dielectric leakage losses. In addition, there is a component of $R_{\text{REDISTRIBUTION}}$ which is explained by the double layer structure of supercapacitors. By adding a third branch the long-term characteristics can be modelled more accurately [10].

![Supercapacitor equivalent circuit model and equivalent circuit values.](image)

| Table 2: Equivalent supercapacitor circuit values. |
|---------------------------------|
| $C_1$ | 0.195 F |
| $C_{\text{Redistribution}}$ | 16.5 mF |
| $C_3$ | 27.5 mF |
| $R_1$ | 6 Ω |
| $R_{\text{Redistribution}}$ | 4 kΩ |
| $R_{\text{Redistribution}}$ | 45 kΩ |

Following a charging period of the supercapacitor, the voltage on capacitors $C_{S1}$ is charged to the source voltage, $V_{\text{MPP+}}$ in the proposed circuit. However, due to a higher time constant in the redistribution branch, it takes a longer time for the voltage on $C_{\text{REDISTRIBUTION}}$ to reach $V_{\text{MPP+}}$. Therefore, during the discharge cycle, some energy flows from branch 1 ($C_{S1}$), to branch 2,
(CREDISTRIBUTION), incurring losses in $R_{ESR}$ and $R_{RESISTION}$. This effect may be minimised by charging the supercapacitor sufficiently to $V_{MPP}$ before connecting it into the circuit, but some losses remain due to the variation in voltage applied to enable hysteretic control. These losses are included in capacitor conduction losses in Figure 4 (b).

Similarly equalisation losses, [11], occur between each of the supercapacitors, $C_1$ & $C_2$, in Figure 1. This imbalance is caused by the fact that the EH source always remains connected in parallel with the first supercapacitor, $C_1$. Figure 4 (a) shows this voltage imbalance between $C_1$, red, and $C_2$, blue, and the current difference between the supercapacitors during a discharge cycle. It is clear to see that $C_2$ supplies more current to the load in comparison with $C_1$. These losses are detailed as equalisation losses in Figure 4, where it is clear that both they and capacitor conduction losses are the most significant.

In a bid to reduce equalisation losses, the EH source was disconnected from the circuit during discharging but, mainly due to reduced input power, the efficiency was found to be significantly lower. Tests were also performed with the EH source connected in series with the switched supercapacitor stages to overcome the imbalance. In this case the DSSC severely limited the output current and therefore had a major impact on the circuit performance and efficiency. Sense resistors are required to measure the current flowing into and out of the switched capacitor circuit. These losses would not feature in a final version of the circuit but for the prototype these losses play a significant part due to the overall low-power being supplied by the source.

4. Measurements/Results

A prototype of the proposed switched capacitor block has been built and initial testing performed with a DSSC source and a variable load resistance. Figure 5 (a) shows measured output waveforms of a 2-capacitor version, while Figure 5 (b) includes measured efficiency for 1- and 2-capacitor implementations. Figure 5 (b) also shows the predicted efficiency of the switched capacitor stage, of a compatible boost converter stage [2] (during discharging) and the overall combined system efficiency.

The overall trend is a decrease in efficiency of the switched capacitor circuit with an increase in number of capacitors. However due to the sense resistors the efficiency of the 1-capacitor circuit is reduce significantly. There is also a significant difference between the measured and predicted efficiency of the 2-capacitor circuit. This requires a review of the equalisation model as well as examining new methods to increase the accuracy of the efficiency measurements. This is due to the low current values, mA, that are being measured on both the input and output of the switched capacitor circuit. When the switched capacitor circuit is combined with a boost converter to deliver the required 3.3 V output, the overall step-up conversion efficiency is improved versus the standard boost converter.
The higher total conversion efficiency is mostly due to the increased boost converter efficiency which is enabled by the switched capacitor buffer stage. At higher number of capacitors the overall step-up conversion efficiency remains at a value around 15% higher than that of the best existing solution conversion solution.

5. Conclusions & Future Work

Results for the proposed switched-capacitor buffer block show a very promising increase of up to 10% in efficiency of power delivered from low-voltage low-power EH sources over an existing boost converter. This increases the energy available to wireless sensor loads which can increase their data transfer rate or functionality/accuracy. This increase is due to the switched capacitor circuit enabling operation in a similar pulsed manner as the wireless sensor, thus reducing the continuous conversion losses encountered by many converters. It also provides a voltage step-up function that increases the boost stage efficiency. Future work will involve determining the optimum number of capacitors and boost converter configuration to give the highest possible overall step-up efficiency.

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