The Decidability of Verification under Promising 2.0

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In PLDI’20, Kang et al. introduced the promising semantics (PS 2.0) of the C++ concurrency that captures most of the common program transformations while satisfying the DRF guarantee. The reachability problem for finite-state programs under PS 2.0 with only release-acquire accesses (PS 2.0-ra) is already known to be undecidable. Therefore, we address, in this paper, the reachability problem for programs running under PS 2.0 with relaxed accesses (PS 2.0-rlx) together with promises. We show that this problem is undecidable even in the case where the input program has finite state. Given this undecidability result, we consider the fragment of PS 2.0-rlx with a bounded number of promises. We show that under this restriction, the reachability is decidable, albeit very expensive: it is non-primitive recursive. Given this high complexity for PS 2.0-rlx with bounded number of promises and the undecidability result for PS 2.0-ra, we consider a bounded version of the reachability problem. To this end, we bound both the number of promises and the “view-switches”, i.e., the number of times the processes may switch their local views of the global memory. We provide a code-to-code translation from an input program under PS 2.0, with relaxed and release-acquire memory accesses along with promises, to a program under SC. This leads to a reduction of the bounded reachability problem under PS 2.0 to the bounded context-switching problem under SC. We have implemented a prototype tool and tested it on a set of benchmarks, demonstrating that many bugs in programs can be found using a small bound.

Additional Key Words and Phrases: Model-Checking, Weak Memory Models, Promising Semantics

1 INTRODUCTION

An important long-standing open problem in PL research has been to define a weak memory model that captures the semantics of concurrent memory accesses in languages like Java and C/C++. A model is considered good if it can be implemented efficiently (i.e., if it supports all usual compiler optimizations and its accesses are compiled to plain x86/ARM/Power/RISCV accesses), and is easy to reason about. After many attempts at solving this problem (e.g., [Batty et al. 2011; Crary and Sullivan 2015; Jeffrey and Riely 2019; Lahav et al. 2017; Manson et al. 2005; Pichon-Pharabod and Sewell 2016; Zhang and Feng 2013]), a breakthrough was achieved by Kang et al. [Kang et al. 2017], who introduced the promising semantics. This was the first model that supported basic invariant reasoning, the DRF guarantee, and even a non-trivial program logic [Svendsen et al. 2018].

In the promising semantics, the memory is modeled as a set of timestamped messages, each corresponding to a write made by the program. Each process/thread records its own view of the memory—i.e., the latest timestamp for each memory location that it is aware of. A message has the form \((x, v, (f, t), V)\) where \(x\) is a location, \(v\) a value to be stored for \(x\), \((f, t)\) is the timestamp interval corresponding to the write and \(V\) is the local view of the process who made the write to \(x\). When reading from memory, a process can either return the value stored at the timestamp in its view or advance its view to some larger timestamp and read from that message. When a process \(p\) writes to memory location \(x\), a new message with a timestamp larger than \(p\)’s view of \(x\) is created, and \(p\)’s view is advanced to include the new message. In addition, in order to allow load-store reorderings, a process is allowed to promise a certain write in the future. A promise is also added

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as a message in the memory, except that the local view of the process is not updated using the timestamp interval in the message. This is done only when the promise is eventually fulfilled. A consistency check is used to ensure that every promised message can be certified (i.e., made fulfillable) by executing that process on its own. Furthermore, this should hold from any future memory (i.e., from any extension of the memory with additional messages). The quantification prevents deadlocks (i.e., processes from making promises they are not able to fulfil). The promising semantics generally allows program executions to contain unboundedly many concurrent promised messages, provided that all of them can be certified. As one can immediately see, this is a fairly complex model, and beyond its support for some basic reasoning patterns, it is not at all obvious whether it is easy to reason about concurrent programs running under this model. Furthermore, the unbounded number of future memories, that need to be checked, makes the verification of even simple programs practically infeasible. Moreover, a number of transformations based on global value range analysis as well as register promotion were not supported in [Kang et al. 2017].

To address the above concerns, a new version of the promising semantics PS 2.0 [Lee et al. 2020] has been proposed, by redesigning key components of the promising semantics [Kang et al. 2017]. Mainly, PS 2.0 supports register promotion and global value range analysis, while capturing all features (thread local optimizations, DRF guarantees, hardware mappings) of the promising semantics of [Kang et al. 2017]. PS 2.0 simplifies also the consistency check and instead of checking the promise fulfilment from all future memories, PS 2.0 checks for promise fulfilment only from a specially crafted extension of the current memory called capped memory. PS 2.0 also introduces the notion of reservations, which allows a process to secure a timestamp interval in order to perform a future atomic read-modify-write instruction. The reservation blocks any other message from using that timestamp interval. Reservations allows register promotions.

The wide umbrella of features of PS 2.0 allowing two memory access modes, relaxed (rlx) and release-acquire (ra) along with promises, reservations and subsequent certification make PS 2.0 a very complex model. While the PS 2.0 semantics is a breakthrough contribution, a natural and fundamental question is to investigate the verification of concurrent programs under PS 2.0. For that, investigating the decidability of verification problems as well as defining efficient analysis techniques are two extremely important problems.

One of the problems addressed in this paper is to investigate the decidability of the reachability problem for PS 2.0. Let PS 2.0-rlx and PS 2.0-ra represent respectively, the fragment of PS 2.0 allowing only relaxed (rlx) and release-acquire (ra) memory accesses. The reachability with only ra accesses has been shown to be undecidable [Abdulla et al. 2019], even without the features of promises and reservations. That leaves only the fragment PS 2.0-rlx of PS 2.0 for investigation. We show that if unbounded number of promises is allowed, the reachability problem is undecidable in PS 2.0-rlx, while it becomes decidable if we bound the number of promises at any time (however, the total number of promises made with a run can be unbounded). Our undecidability is obtained with just 2 threads, with an execution where the number of context switches between the two processes is three, where a context is a computation segment in which one process is active. The proof of decidability is done by proposing a new memory model with higher order words LoHoW, and showing the equivalence of PS 2.0-rlx and LoHoW. Under the bounded promises assumption, we use the decidability of the coverability problem of well structured transition systems (WSTS) [Abdulla and Jonsson 1996; Finkel and Schnoebelen 2001] to show that the reachability problem for LoHoW with bounded number of promises is decidable.

Given this high complexity for PS 2.0-rlx with bounded number of promises and the undecidability result for PS 2.0-ra [Abdulla et al. 2019], we consider a bounded version of the reachability problem. To this end, we propose a parametric under-approximation in the spirit of context bounding [Abdulla et al. 2019, 2017; Atig et al. 2011; La Torre et al. 2009; Lal and Reps 2009; Musuvathi and
The decidable properties of verification under promising 2.0 [Qadeer 2007; Norris and Demsky 2016; Qadeer and Rehof 2005]. The bounding concept chosen for concurrent programs depends on aspects related to the interactions between the processes. In the case of SC programs, context bounding has been shown experimentally to have extensive behaviour coverage for bug detection [Musuvathi and Qadeer 2007; Qadeer and Rehof 2005]. A context in the SC setting is a computation segment where only one process is active. The concept of context bounding has been extended for weak memory models. For instance, in TSO, the notion of context is extended to one where all updates to the main memory are done only from the buffer of the active thread [Atig et al. 2011]. In the case of RA [Abdulla et al. 2019], context bounding was extended to view bounding, using the notion of view-switching messages. Since PS 2.0 subsumes RA, we propose a bounding notion that extends the view bounding proposed in [Abdulla et al. 2019]. Using this new bounding notion, we propose a source to source translation from programs under PS 2.0 to context-bounded executions of the transformed program in SC. The main challenge in the code-to-code translation of [Abdulla et al. 2019] was to keep track of the causality between different variables. In our case, the challenge is fundamentally different and is to provide a procedure that (i) handles different memory accesses r1x and ra, (ii) guesses the promises and reservations in a non-deterministically manner, and (iii) verify that each promise so guessed is fulfilled using the capped memory. This reduction is implemented in a tool, called PS2SC. Our experimental results demonstrate the effectiveness of our approach. We exhibit cases where hard-to-find bugs are detectable using a small view-bound $K$. Our tool displays resilience to trivial changes in the position of bugs and the order of processes.

Related Work. The decidability of the verification problems for programs running under weak memory models has been addressed for TSO [Atig et al. 2010], PS 2.0-ra [Abdulla et al. 2019], Power [Abdulla et al. 2020], and for a subclass of PS 2.0-ra [Lahav and Boker 2020]. To the best of our knowledge, this is the first time that this problem is investigated for PS 2.0-rlx and PS2SC is the first tool for automated verification of programs under PS 2.0, which also works for the promising semantics [Kang et al. 2017]. Most of the existing work concerns the development of stateless model checking (SMC), coupled with (dynamic) partial order reduction techniques (e.g., [Abdulla et al. 2018; Kokologiannakis et al. 2017, 2019; Norris and Demsky 2013, 2016]) and do not handle promises. Context-bounding has been proposed in [Qadeer and Rehof 2005] for programs running under SC. This work has been extended in different directions and has led to efficient and scalable techniques for the analysis of concurrent programs (see e.g., [Emmi et al. 2011; La Torre et al. 2008, 2009, 2010; Lal and Reps 2009; Musuvathi and Qadeer 2007]). In the context of weak memory models, context-bounded analysis has been only proposed to programs running under TSO/PSO in [Atig et al. 2011; Tomasco et al. 2017] and under POWER in [Abdulla et al. 2017].

2 PRELIMINARIES

In this section, we introduce the simple programming language and the notation that will be used throughout. Then, we review PS 2.0 definition, and present the model following [Lee et al. 2020].

2.1 Notations

Given two natural numbers $i, j \in \mathbb{N}$ s.t. $i \leq j$, we use $[i, j]$ to denote the set $\{k | i \leq k \leq j\}$. Let $A$ and $B$ be two sets. We use $f : A \rightarrow B$ to denote that $f$ is a function from $A$ to $B$. We define $f[a \mapsto b]$ to be the function $f'$ such that $f'(a) = b$ and $f'(d') = f(d')$ for all $d' \neq a$. For a binary relation $R$, we use $[R]^*$ to denote its reflexive and transitive closure. Given an alphabet $\Sigma$, we use $\Sigma^*$ (resp. $\Sigma^+$) to denote the set of possibly empty (resp. non-empty) finite words over $\Sigma$. Let $w = a_1a_2 \cdots a_n$ be a word over $\Sigma$, we use $|w|$ to denote the length of $w$. Given an index $i$ in $[1, |w|]$, we use $w[i]$ to
denote the $i^{th}$ letter of $w$. Given two indices $i$ and $j$ s.t. $1 \leq i \leq j \leq |w|$, we use $w[i, j]$ to denote the word $a_i a_{i+1} \cdots a_j$. Sometimes, we consider a word as a function from $[1, |w|]$ to $\Sigma$.

### 2.2 Program Syntax

The simple programming language we use is described in Figure 1. A program $Prog$ consists of a set $Loc$ of (global) variables or memory locations, and the definition of a set $P$ of processes. Each process $p$ declares a set $Reg(p)$ of (local) registers followed by a sequence of labeled instructions. We assume that these sets of registers are disjoint and we use $= \lambda$ with a unique initial instruction labeled by $PS 2.0$ Timestamps.

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In this section, we recall the promising semantics [Lee et al. 2020]. We present here 2.3 The Promising Semantics of $PS 2.0$, since they do not affect the results of this paper.

A local assignment instruction $s_r = e$ assigns to the register $s_r$ the value of $e$, where $e$ is an expression over a set of operators, constants as well as the contents of the registers of the current process, but not referring to the set of locations. The fence instruction SC-fence is used to enforce sequential consistency if it is placed between two memory access operations. Finally, the conditional, assume and iterative instructions have the standard semantics. For simplicity, we will write $\text{assume}(x = e)$ instead of $s_r = x; \text{assume}(s_r = e)$. This notation is extended in the straightforward manner to conditional statements.

### 2.3 The Promising Semantics

In this section, we recall the promising semantics [Lee et al. 2020]. We present here $PS 2.0$ with three memory accesses, relaxed (this is the default mode), release writes (rel) and acquire reads (acq). Read-modify-writes (RMW) instructions have two access modes - one for read and one for write. We keep aside the release and acquire fences (and subsequent access modes) which are part of $PS 2.0$, since they do not affect the results of this paper.

**Timestamps.** $PS 2.0$ uses timestamps to maintain a total order over all the writes to the same variable. We assume an infinite set of timestamps $Time$, densely totally ordered by $\leq$, with 0 being the minimum element. A view is a timestamp function $V: Loc \rightarrow Time$ records the largest known timestamp for each location. Let $T$ be the set containing all the timestamp functions, along with the special symbol $\perp$. Let $V_{\init}$ represent the initial view where all locations are mapped to 0. Given two views $V$ and $V'$, we use $V \leq V'$ to denote that $V(x) \leq V'(x)$ for $x \in Loc$. The merge operation $\sqcup$ between the two views $V$ and $V'$ returns the pointwise maximum of $V$ and $V'$, i.e., $(V \sqcup V')(y)$.
is the maximum of \( V(y) \) and \( V'(y) \). Let \( I \) denote the set of all intervals over Time. The timestamp intervals in \( I \) have the form \( (f, t] \) where either \( f = t = 0 \) or \( f < t \), with \( f, t \in \text{Time} \). Given an interval \( I = (f, t] \in I, I.\text{frm} \) and \( I.\text{to} \) denote \( f, t \) respectively.

**Memory.** In PS 2.0, the memory is modelled as a set of concrete messages (which we just call messages), and reservations. Each message represents the effect of a write or a RMW operation and each reservation is a timestamp interval reserved for future use. In more detail, a message \( m \) is a tuple \( (x, v, (f, t), V) \) where \( x \in \text{Loc}, v \in \text{Val}, (f, t) \in I \) and \( V \in \mathbb{T} \). A reservation \( r \) is a tuple \((x, (f, t))\). Note that a reservation, unlike a message, does not commit to any particular value, but only specifies the interval which is reserved. We use \( m.\text{loc} (r.\text{loc}), m.\text{val}, m.\text{to} (r.\text{to}), m.\text{frm} (r.\text{frm}) \) and \( m.\text{View} \) to denote respectively \( x, v, t, f \) and \( V \). Two elements (either messages or reservations) are said to be disjoint \((m_1 \# m_2)\) if they concern different variables \((m_1.\text{loc} \neq m_2.\text{loc})\) or their intervals do not overlap \((m_1.\text{to} < m_2.\text{frm} \lor m_1.\text{frm} > m_2.\text{to})\). Two sets of elements \( M, M' \) are disjoint, denoted \( M \# M' \), if \( m \# m' \) for every \( m \in M, m' \in M' \). Two elements \( m_1, m_2 \) are adjacent denoted \( \text{Adj}(m_1, m_2) \) if \( m_1.\text{loc} = m_2.\text{loc} \) and \( m_1.\text{to} = m_2.\text{frm} \). A memory \( M \) is a set of pairwise disjoint messages and reservations. Let \( \overline{M} \) be the subset of \( M \) containing only messages (no reservations). For a location \( x \), let \( M(x) = \{ m \in M \mid m.\text{loc} = x \} \). Given a view \( V \) and a memory \( M \), we say \( V \in M \) if \( V(x) = m.\text{to} \) for some message \( m \in \overline{M} \) for every \( x \in \text{Loc} \). Let \( \mathcal{M} \) denote the set of all memories.

**Insertion into Memory.** Following [Lee et al. 2020], a memory \( M \) can be extended with a message (due to the execution of a write/RMW instruction) or a reservation \( m \) with \( m.\text{loc} = x, m.\text{frm} = f \) and \( m.\text{to} = t \) in a number of ways:

- **[Additive insertion]** \( M \xleftarrow{A} m \) is defined only if (1) \( M\#\{m\} \); (2) if \( m \) is a message, then no message \( m' \in M \) has \( m'.\text{loc} = x \) and \( m'.\text{frm} = t \); and (3) if \( m \) is a reservation, then there exists a message \( m' \in \overline{M} \) with \( m'.\text{loc} = x \) and \( m'.\text{to} = f \). The extended memory \( M \xleftarrow{A} m \) is then \( M \cup \{m\} \).

- **[Splitting insertion]** \( M \xleftarrow{S} m \) is defined if \( m \) is a message, and, if there exists a message \( m' = (x, v', (f, t'), V) \) with \( t < t' \) in \( M \). Then \( M \) is updated to \( M \xleftarrow{S} m = (M \setminus \{m'\} \cup \{m, (x, v', (t, t'), V)\}) \).

- **[Lowering Insertion]** \( M \xleftarrow{L} m \) is only defined if there exists \( m' \in M \) that is identical to \( m = (x, v, (f, t), V) \) except for \( m.\text{View} \leq m'.\text{View} \). Then, \( M \) is updated to \( M \xleftarrow{L} m = M \setminus \{m'\} \cup \{m\} \).

- **[Cancellation]** \( M \xleftarrow{C} m \) is defined if \( m \) is a reservation in \( M \). Then \( M \) is updated as \( M \setminus \{m\} \).

**Transition System of a Process.** Given a process \( p \in \mathcal{P} \), a state \( \sigma \) of \( p \) is defined as a pair \( (\lambda, R) \) where \( \lambda \in \mathbb{L} \) is the label of the next instruction to be executed by \( p \) and \( R : \text{Reg} \rightarrow \text{Val} \) maps each register of \( p \) to its current value. (Observe that we use the set of all labels \( \mathbb{L} \) (resp. registers \( \text{Reg} \)) instead of \( \mathbb{L}_p \) (resp. \( \text{Reg}(p) \)) in the definition of \( \sigma \) just for the sake of simplicity.) Transitions between the states of \( p \) of the form \( (\lambda, R) \xrightarrow{t} (\lambda', R') \) with \( t \in \{e, \text{rd}(o, x, v), \text{wt}(o, x, v), \text{U}(o_r, o_w, x, v_r, v_w), \text{SC-fence} \mid x \in \text{Loc}, v \in \text{Val}, o \in \{r1x, ra\} \} \). A transition of the form \( (\lambda, R) \xrightarrow{\text{rd}(o, x, v)} (\lambda', R') \) denotes the execution of a read instruction of the form \( S_r = x^o \) labeled by \( \lambda \) where (1) \( \lambda' \) is the label of the next instructions that can be executed after the execution of the instruction labelled by \( \lambda \), and (2) \( R' \) is the mapping that results from the replacement of the value of the register \( S_r \) in \( R \) by \( v \). The transition relation \( (\lambda, R) \xrightarrow{t} (\lambda', R') \) is defined in similar manner for the other states of \( t \) where \( \text{wr}(o, x, v) \) stands for a write instruction that writes the value \( v \) to \( x \), \( \text{U}(o_r, o_w, x, v_r, v_w) \) stands for a RMW that reads the value \( v_r \) from \( x \) and write \( v_w \) to it, \( \text{SC-fence} \) stands for a SC-fence instruction, and \( \epsilon \) stands for the execution of the other local instructions. Observe that \( o, o_r, o_w \) are the access modes which can
We first describe the transition process configurations in \( \mathcal{P} \) from which we induce the transition relation between machine states.

**Transition Relation.** We first describe the transition \( (\sigma, V, P, M, G) \rightarrow (\sigma', V', P', M', G') \) between process configurations in \( \mathcal{P} \) with the label of the initial instruction to be executed, \( R : \mathcal{R} \rightarrow \mathbb{M} \) maps each register to its current value, \( \mathcal{V} = \mathcal{P} \rightarrow \mathbb{T} \) is the process view map, which maps each process to a view, \( M \) is a memory and \( \mathcal{P} : \mathcal{P} \rightarrow \mathbb{M} \) maps each process to a set of messages (called promise set), and \( G \in \mathbb{T} \) is the global view (that will be denoted by all PCSC fences). We use \( C \) to denote the set of all machine states.

Given a machine state \( MS = ((J, R), VS, PS, M, G) \) and a process \( p \), let \( MS \downarrow p \) denote the projection, \( (\sigma, VS(p), PS(p), M, G) \) with \( \sigma = (J(p), R(p)) \), of the machine state to the process \( p \).

We call \( MS \downarrow p \) the process configuration. We use \( C_\mathcal{P} \) to denote the set of all process configurations.

The initial machine state \( MS_\text{init} = ((J_\text{init}, R_\text{init}), VS_\text{init}, PS_\text{init}, M_\text{init}, G_\text{init}) \) is one where: (1) \( J_\text{init}(p) \) is the label of the initial instruction of \( p \); (2) \( R_\text{init}(Sr) = 0 \) for every \( Sr \in \mathcal{R} \); (3) for each \( p \), we have \( VS(p) = V_\text{init} \) as the initial view (that maps each location to the timestamp 0);

(4) for each process \( p \), the set of promises \( PS_\text{init}(p) \) is empty; (5) the initial memory \( M_\text{init} \) contains exactly one initial message \( (x, 0, (0, 0], V_\text{init}) \) for each location \( x \); and (6) the initial global view maps each location to 0.

**Memory Helpers**

\[
\begin{array}{|c|c|}
\hline
\text{(MEMORY : NEW)} & \text{(MEMORY : FULFILL)} \\
\hline
(P, M) \mapsto (P', M \leftarrow m) & m = (x, \cdot, \cdot, \cdot) \in M \quad V(x) \leq t \\
\text{Write} & a = rlx \Rightarrow V' = V[x \mapsto t] \\
\text{Reserve} & a = rlx \Rightarrow V' = V[x \mapsto t] \cup K \\
\text{Promise} & a = ra \Rightarrow V' = V[x \mapsto t] \cup K \\
\hline
\end{array}
\]

**Process Helpers**

\[
\begin{array}{|c|c|}
\hline
m = (x, \cdot, \cdot, \cdot) \in M \quad V(x) < t \\
\text{Cancel} & a = rlx \Rightarrow K = \perp, a = ra \Rightarrow P(x) = 0 \wedge K = V' \\
\hline
\end{array}
\]
location $x$ along with a timestamp interval $(-, t]$. Then, the process view of location $x$ is updated to $t$. In case of a release write $\text{wt}(\text{ra}, x, v)$ the updated process view is also attached to $m$, and ensures that the process does not have an outstanding promise on location $x$. (MEMORY : FULFILL) allows to split a promise interval or lower its view before fulfilment.

**Update.** When a process performs a RMW, it first reads a message $m = (x, a, (f, t], K)$ and then writes an update message with $\text{frm}$ timestamp equal to $t$; that is, a message of the form $m' = (x, a', (t, t'], K')$. This forbids any other write to be placed between $m$ and $m'$. The access modes of the reads and writes in the update follow what has been described for the read and write above.

**Promise, Reservation and Cancellation.** A process can non-deterministically promise future writes which are not release writes. This is done by adding a message $m$ to the memory $M$ s.t. $m^\#M$ and to the set of promises $P$. Later, a relaxed write instruction can fulfil an existing promise. Recall that the execution of a release write requires that the set of promises to be empty and thus it can not be used to fulfil a promise. In the reserve step, the process reserves a timestamp interval to be used for a later RMW instruction reading from a certain message without fixing the value it will write. A reservation is added both to the memory and the promise set. The process can drop the reservation from both sets using the cancel step in non-deterministic manner.

**SC fences.** The process view $V$ is merged with the global view $G$, resulting in $V \sqcup G$ as the updated process view and global view.

**Machine Relation.** We are ready now to define the induced transition relation between machine states. For machine states $MS = ((J, R), VS, PS, M, G)$ and $MS' = ((J', R'), VS', PS', M', G')$, we write $MS \rightarrow MS'$ iff (1) $MS\downarrow p \rightarrow MS'\downarrow p$ and $(J(p'), VS(p'), PS(p')) = (J'(p'), VS'(p'), PS'(p'))$ for all $p' \neq p$.

**Consistency.** According to Lee et al. [Lee et al. 2020], there is one final requirement on machine states called consistency, which roughly states that, from every encountered machine state encountered, all the messages promised by a process $p$ can be certified (i.e., made fulfillable) by executing $p$ on its own from a certain future memory (called capped memory), i.e., extension of the memory with additional reservation. Before defining consistency, we need to introduce capped memory.

**Cap View, Cap Message and Capped Memory.** The last element of a memory $M$ with respect to a location $x$, denoted by $\overline{m}_{M,x}$, is an element from $M(x)$ with the highest timestamp among all elements of $M(x)$ and is defined as $\overline{m}_{M,x} = \max_{m \in M(x)} m \cdot t$. The cap view of a memory $M$, denoted by $\overline{V}_M$, is the view which assigns to each location $x$, the $t$ timestamp in the message $\overline{m}_{M,x}$. That is, $\overline{V}_M = \lambda x.\overline{m}_{M,x} \cdot \to$. Recall that $\overline{M}$ denote the subset of $M$ containing only messages (no reservations). The cap message of a memory $M$ with respect to a location $x$, is given by the message $\overline{m}_{M,x} = (x, \overline{m}_{M,x} \cdot \text{val}, (\overline{m}_{M,x} \cdot \to, \overline{m}_{M,x} \cdot \to + 1], \overline{V}_M)$.

Then, the capped memory of a memory $M$, wrt. a set of promises $P$, denoted by $\overline{M}_P$, is an extension of $M$, defined as: (1) for every $m_1, m_2 \in M$ with $m_1 \cdot \text{loc} = m_2 \cdot \text{loc}, m_1 \cdot \to < m_2 \cdot \to$, and there is no message $m' \in M(m_1 \cdot \text{loc})$ such that $m_1 \cdot \to < m' \cdot \to < m_2 \cdot \to$, we include a reservation $(m_1 \cdot \text{loc}, (m_1 \cdot \to, m_2 \cdot \text{frm}))$ in $\overline{M}_P$, and (2) we include a cap message $\overline{m}_{M,x}$ in $\overline{M}_P$ for every variable $x$ unless $\overline{m}_{M,x}$ is a reservation in $P$.

**Consistency of machine states.** A machine state $MS = ((J, R), VS, PS, M, G)$ is consistent if every process $p \in P$ can certify/fulfil all its promises from the capped memory $\overline{M}_{PS(p)}$, i.e., $((J, R), VS, PS, \overline{M}_{PS(p)}, G) \rightarrow^* ((J', R'), VS', \emptyset, M', G')]$. 

The Reachability Problem in PS 2.0. A run of $\text{Prog}$ is a sequence of the form: $\text{MS}_0 \xrightarrow{P_i_1} \text{MS}_1 \xrightarrow{P_i_2} \text{MS}_2 \xrightarrow{P_i_3} \cdots \xrightarrow{P_i_n} \text{MS}_n$ where $\text{MS}_0 = \text{MS}_{\text{init}}$ is the initial machine state and $\text{MS}_1, \ldots, \text{MS}_n$ are consistent machine states. In this case, the machine states $\text{MS}_0, \ldots, \text{MS}_n$ are said to be reachable from $\text{MS}_{\text{init}}$.

Given an instruction label function $\mathcal{J}: P \to L$ that maps each process $p \in P$ to an instruction label in $L_p$, the reachability problem asks whether there exists a machine state of the form $((\mathcal{J}, \mathcal{R}), \mathcal{V}, P, M, G)$ that is reachable from $\text{MS}_{\text{init}}$. In the case of a positive answer to this problem, we say that $\mathcal{J}$ is reachable in $\text{Prog}$ in PS 2.0.

2.4 Examples

In the following, we describe some examples to demonstrate PS 2.0. For readability, instead of referring to reachable instruction labels, we consider possible program outcomes represented using the program comment annotation "//". All writes and reads are relaxed in both examples below.

Example 2.1. The annotated program outcome in Figure 3 is not allowed by PS 2.0. We list the execution steps of PS 2.0 showing that the annotated behaviour is not possible. We give a proof by contradiction. Assume that the annotated behaviour is possible. The only way for this is that the first process $p_1$ (whose code on the left side) to execute the else branch. For this, it needs to read 2 from $x$. This can be provided only by the second process using the write $x=2$. For this to happen, $p_2$ first executes the write $z=3$ by adding a message $(z, 3, (r, s], \perp)$ to the memory. Next, $p_2$ has to read a message of the form $(z, 2, (f, t], \perp)$ which can only be generated by $p_1$ as a promise.

Note that $p_1$ can promise the write $z = 2$ in its if ... then branch. To certify this promise, $p_1$ starts from the capped memory, and first executes the write $z=1$ in the if ... then branch. To do this, it can split the promise interval $(f, t]$ and add a message $(z, 1, (f, t'], \perp)$ while modifying $(z, 2, (f, t], \perp)$ in the memory to $(z, 2, (t', t], \perp)$. Note that since we work from the capped memory, there are no available intervals in $[0, \max(t, s)]$, and the only way to add a message for the write $z=1$ of $p_1$, in such a way that $p_1$ can read the 3 written by $p_2$, and also to fulfil its promise, is to split the promise interval. Next, $p_1$ reads $(z, 3, (r, s], \perp)$ to go past the assume($z=3$) statement. This imposes $f < t' \leq r < s$. However, since $p_2$ wrote 3 to $z$ before reading the promise $(z, 2, (t', t], \perp)$, we also need $r < s \leq f < t'$ which contradicts $f < r$. Hence, the annotated behaviour is not reachable, since $p_1$ fails the certification.

Example 2.2. In Figure 4, we present an example having a run realising the program outcome which has unboundedly many reservations and subsequent cancellations. We list the execution steps of PS 2.0 leading to the annotated behaviour. Items prefixed with "C" represent certification steps.

1. Process 2 writes 1 to $w$. 

---

$\text{r1}=x$

\textbf{if}($\text{r1} \neq 2$){
  \textbf{z}=1
  $\text{r1}=z$
  \textbf{assume}($\text{r1}=3$)
  $\text{z}=2$
}

\textbf{else}{
  $\text{z}=2$ \textbf{ //}
}

\textbf{\textbf{Fig. 3.}} The annotated behaviour is not reachable.
3 UNDECIDABILITY OF CONSISTENT REACHABILITY IN PS 2.0

In this section, we show that reachability is undecidable for PS 2.0 even for finite-state programs. The proof is by a reduction from Post’s Correspondence Problem (PCP) [Post 1946]. Our proof works with the fragment of PS 2.0 having only relaxed (r1x) memory accesses and crucially uses unboundedly many promises to ensure that a process cannot skip any writes made by another process. It also works even when we restrict our analysis to executions that can be split into a bounded number of contexts, where within each context, only one process is active. We need just 3 context switches. Our undecidability result is also tight in the sense that the reachability problem becomes decidable when we restrict ourselves to machine states where the number of promises is bounded. Given our proof (Theorem 3.1) where undecidability is obtained with the r1x fragment of PS 2.0, a natural question is the decidability status of the ra fragment of PS 2.0. This is known to be undecidable from [Abdulla et al. 2019] even in the absence of promises. Let us call the fragment of PS 2.0 with only r1x memory accesses PS 2.0-rlx.

**Theorem 3.1.** The reachability problem for concurrent programs over a finite data domain is undecidable under PS 2.0. In fact, the undecidability still holds for the PS 2.0-rlx fragment.

The rest of this section is devoted to the proof of Theorem 3.1. The undecidability is obtained by a reduction from Post’s Correspondence Problem (PCP) [Post 1946]. A PCP instance consists of two sequences $u_1, \ldots, u_n$ and $v_1, \ldots, v_n$ of non-empty words over some alphabet $\Sigma$. Checking whether there exists a sequence of indices $j_1, \ldots, j_k \in \{1, \ldots, n\}$ s.t. $u_{j_1} \ldots u_{j_k} = v_{j_1} \ldots v_{j_k}$ is undecidable.
We construct a concurrent program with two processes $p_1$ and $p_2$ (see Figure 5), six memory locations $\text{Loc} = \{x, y, \text{validate}, \text{index}, index', \text{term}\}$, and two registers \{$r, r'$\}. The finite data domain of $\text{Prog}$ is defined as $\text{Val} = \Sigma \cup \{0, 1, \ldots, n\} \cup \{$\$, \#\}$, where \$ and \# are two special symbols (not in $\Sigma \cup \{0, 1, \ldots, n\}$). All the locations and registers are initialized to zero. We show that reaching the instructions annotated by // and // in $p_1, p_2$ is possible iff the PCP instance has a solution. We give below an overview of the execution steps leading to the annotated instructions.

1. To begin, process $p_2$ writes 1 to the location $term$.
2. Process $p_1$ promises to write letters of $u_i$ (one by one) to location $x$, and the respective indices $i$ to the location $\text{index}$. The number of made promises is arbitrary, since it depends on the length of the PCP solution. Observe that the sequence of promises made to the variable $\text{index}$ corresponds to the guessed solution of the PCP problem.

(C1) Using the if branch, $p_1$ certifies its promise before switching out of context. Note that fulfilment of promises is yet to be done.
3. Process $p_2$ reads from the sequences of promises written to $x$ and $\text{index}$ and copies them (one by one) to variables $y$ and $\text{index}'$ respectively, and reaches //.

---

**Table 1:**

| Process $p_1$ | Process $p_2$ | Module$^{C_{p_1}}$ | Module$^{C_{p_2}}$ |
|---------------|---------------|---------------------|---------------------|
| /* generation mode */ | /* validation mode */ | assume($y = u_i[1]$) | assume($x = u_i[1]$) |
| if validate = 0 then | while validate = 1 do | assume($y = #)$ | assume($x = #$) |
| while term = 0 do | $r$ = index; | assume($y = u_i[2]$) | assume($x = u_i[2]$) |
| index = 1 | assume($y \in [1, n]$) | ... | ... |
| Module$^{p_1}$ | while $r \neq \#$ do | assume($y = #)$ | assume($x = #)$ |
| $r$ = 1 then | $x = u_i[1]$ | assume($y = u_i[|u_i|]$) | assume($x = u_i[|u_i|]$) |
| Module$^{p_2}$ | $x = \#$ | assume($x = #)$ | assume($x = #)$ |
| else if $r = 2$ then | $x = u_i[2]$ | ... | ...
| Module$^{p_2}$ | $y = #)$ | ... | ...
| ... | $y = u_i[2]$ | ... | ...
| index = n | $x = u_i[|u_i|]$ | $y = u_i[|u_i|]$ | ...
| Module$^{p_2}$ | index = $i$ | index' = $i$ | ...
| $r$ = $\#$ | index' = $\#$ | ...
| $r$ = $\#$ do | index = $\#$ |
| $r$ = $\#$ | assume(true) // |

**Fig. 5:** Simulation of the PCP problem using two processes.
(4) The else branch in $p_1$ is enabled at this point, where $p_1$ reads the sequence of indices from $index'$, and each time it reads an index $i$ from $index'$, it checks that it can read the sequence of letters of $v_i$ from $y$.

(C1) $p_1$ copies (one by one) the sequence of observed values from $y$ and $index'$ back to $x$ and $index$ respectively. To fulfill the promises, it is crucial that the sequence of read values from $index'$ (resp. $y$) is the same as the sequence of written values to $index$ (resp. $x$). Since $y$ holds a sequence $u_{i_1} \ldots u_{i_k}$, the promises are fulfilled iff this sequence is same as the promised sequence $u_{i_1} \ldots u_{i_k}$. This happens only when $i_1, \ldots, i_k$ is a PCP solution.

(5) At the end of promise fulfilment, $p_1$ reaches $//$. Let us now give more details about the code of the two processes given in Figure 5. Depending on the value of the validate flag read, process $p_1$ can run in generation mode (then branch) or validation mode (else branch). In generation mode, $p_1$ writes in sequential manner the sequence of indices (alternated with the special symbol #) of a potential solution of the PCP problem to the location $index$ and writes, letter by letter, the sequence of letters of the word $u_i$ to location $x$ each time $p_1$ sets the location $index$ to $i$ (using the $Module^{\text{gen}}_{u_i}$ procedure). In validation mode, $p_1$ reads from locations $index'$ and $y$ and writes back what it has read, to the locations $index$ and $x$, respectively (using the $Module^{\text{val}}_{u_i}$). The second process proceeds in a similar manner as the else branch of the first process: It reads from locations $index$ and $x$ and writes the values read to $index'$ and $y$, respectively (using the $Module^{\text{val}}_{u_i}$). We will show that a solution of the PCP problem exists iff we can reach the annotations $//$, $//$ respectively in processes $p_1, p_2$.

Assume that a solution of the PCP problem exists. This means that there is a sequence of indices $i_1, i_2, \ldots, i_k$ such that $v_1 v_2 \cdots v_k = u_1 u_2 \cdots u_k$. Let $w = u_1 u_2 \cdots u_k$. Let us show that the pair of annotations $//$, $//$ are reachable in $Prog$. For that aim, consider the following run of the program $Prog$: $p_2$ starts first by setting the location term to 1. Then, $p_1$ will use the then branch of its conditional statement and make the two following sequences of promises ($index, i_1, (1, 2)$), ($index, i_2, (2, 3)$), \ldots, ($index, i_k, (k, k + 1)$) and ($x, w[1], (1, 2)$), ($x, w[2], (2, 3)$), \ldots, ($x, w[|w|], (|w|, |w| + 1)$). Observe that $p_1$ can certify such sequences of promises by iterating its iterative statement in the then branch of its alternative statements. Once these promises are performed, $p_2$ reads these two sequences and writes them back to the locations $index'$ and $y$, respectively. $p_2$ then sets the location validate to 1. Now $p_1$ can resume its execution by reading the location validate written by the second process and enter its else branch of its alternative statement. Then, $p_1$ will iteratively read the values written by $p_2$ on the location $index'$ and $y$ and write them back to the locations $index$ and $x$, respectively. By doing this $p_1$ fulfills also the sequence of promises that has been issued.

Now assume that we can reach the pair of annotations $//$, $//$. In order for $p_1$ to reach $//$, it must execute the else branch of its conditional statement. Let us assume it does so. Then, $p_1$ will read the sequence of indices $i_1, i_2, \ldots, i_k$ written by the process $p_2$ on the location $index'$. Let us assume that the process $p_2$ writes the sequence of indices $j_1, j_2, \ldots, j_m$ on the location $index'$ (by reading the sequence of promises made by $p_1$). Each time that the process $p_1$ reads an index from the location $index'$, it writes it back on the location $index$. The process $p_1$ (resp. $p_2$) alternates between writing/reading an index in $\{1, \ldots, n\}$ and the special symbol # in order to make sure that each written index is at most read once. In similar manner, the process $p_2$ reads the sequence of indices $j_1, j_2, \ldots, j_m$ written by the process $p_1$ on the location $index$ and it writes it back on the locations $index'$. This implies that the sequence $j_1, j_2, \ldots, j_m$ is a subsequence of $i_1, i_2, \ldots, i_k$ (since the process $p_2$ can miss reading some written indices by the process $p_1$) and also that the sequence $i_1, i_2, \ldots, i_k$ is a subsequence of $j_1, j_2, \ldots, j_m$ (since $p_1$ can miss reading some written index by the process $p_2$). Thus, we have that the sequences $i_1, i_2, \ldots, i_k$ and $j_1, j_2, \ldots, j_m$ are the same. Every time
the process $p_1$ (resp. $p_2$) reads an index $i$ from the location $index'$ (resp. $index$), it (1) tries to read in sequential manner the sequence of letters appearing in $v_i$ (resp. $u_i$) (alternated with the special symbol #) from the location $y$ (resp. $x$), and (2) writes the same sequence of letters to the location $x$ (resp. $y$). Using a similar argument as in the case of indices, we can deduce that if $p_1$ (resp. $p_2$) writes the words $v_1, v_2, \ldots, v_k$ (resp. $u_j, u_k, \ldots, u_m$), letter by letter (with an alternation with the symbol #), to the location $x$ (resp. $y$), then $v_1, v_2, \ldots, v_k$ (resp. $u_j, u_k, \ldots, u_m$) is a subsequence of $u_j, u_k, \ldots, u_m$ (resp. $v_1, v_2, \ldots, v_k$). Thus, if the pair of annotations $/\backslash, /\backslash$ are reachable then there exist two sequences $i_1, i_2, \ldots, i_k$ and $j_1, j_2, \ldots, j_m$, written, respectively, by $p_1$ and $p_2$ such that $i_1, i_2, \ldots, i_k$ is equal to $j_1, j_2, \ldots, j_m$, and $v_1, v_2, \ldots, v_k$ is equal to $u_j, u_k, \ldots, u_m$. Observe that sequence of indices $i_1, i_2, \ldots, i_k$ is non-empty due to the assume statement $\text{assume} (\forall r' \in [1, n])$.

4 DECIDABLE FRAGMENTS OF PS 2.0

Since keeping ra memory accesses renders the reachability problem undecidable [Abdulla et al. 2019] and so does having unboundedly many promises when having rlx memory accesses (Theorem 3.1), we address in this section the decidability problem for PS 2.0-rlx with a bounded number of promises in any reachable configuration. Observe that bounding the number of promises in any reachable machine state does not imply that the total number of promises made during that run is bounded. Let bdPS 2.0-rlx represent the restriction of PS 2.0-rlx to boundedly many promises where the number of promises in each reachable machine state is smaller or equal to a given constant. In the following, we show the decidability of the reachability problem for bdPS 2.0-rlx. For establishing this result, we introduce an alternate memory model for concurrent programs which we call LoHoW (for “lossy higher order words”). We present the operational semantics of LoHoW, and show that PS 2.0-rlx is operationally equivalent to LoHoW. Then, under the bounded promise assumption, we show how LoHoW is used to decide the reachability problem for bdPS 2.0-rlx.

4.1 Introduction to LoHoW

Given an alphabet $A$, a simple word over $A$ is an element of $A^*$, while a higher order word is an element of $(A^*)^*$ (i.e., word of words). A state of LoHoW maintains a collection of higher order words, one per location, along with the states of all processes. The higher order word $\text{HW}_x$ corresponding to the location $x$ is a word of simple words, representing the sub memory $M(x)$ in PS 2.0-rlx. Each simple word in $\text{HW}_x$ is an ordered sequence of “memory types”, that is, messages or promises in the memory corresponding to $x$, maintained in the order of their to timestamps in the memory. Unlike PS 2.0-rlx, the LoHoW does not store timestamps in the messages and promises; instead, it takes advantage of the word order which induces a natural ordering amongst these without explicit use of timestamps. The key information to encode in each memory type occurring in $\text{HW}_x$ is: (1) whether it is a message (msg) or a promise (prm), (2) which process (p) added it to the memory, and the value (val) it holds, (3) the set $S$ (called pointer set) of processes that are aware of this message/promise (processes which point to this message/promise), and (4) whether the time interval to the right has been reserved by some process.

Memory Types. A memory type is an element of $\Sigma = \{\text{msg}, \text{prm}\} \times \text{Val} \times {\mathcal{P}} \times 2^{{\mathcal{P}}} \cup \Gamma = \{\text{msg}, \text{prm}\} \times \text{Val} \times {\mathcal{P}} \times 2^{{\mathcal{P}}} \times {\mathcal{P}}$. The first component represents a message (msg) or a promise (prm) in the memory $M$ of PS 2.0-rlx, the second component the value in the message/promise, the third component is the process which adds the message/promise to the memory and the fourth component is a pointer set, which contains all processes whose local view agree with the to time stamp of the message/promise. In the case of $\Gamma$, we have a fifth component which holds the id of the process that has reserved the time slot to the right of this message/promise.
For a memory type \( m = (r, v, p, S) \) (or \( m = (r, v, p, S, q) \)), we use \( m.\text{value} \) to denote \( v \). For a memory type \( m = (r, v, p, S) \) (resp. \( m = (r, v, p, S, q) \)) and a process \( h \in \mathcal{P} \), we use \( \text{add}(m, h) \) to denote the memory type \( m = (r, v, p, S \cup \{h\}) \) (resp. \( m = (r, v, p, S \cup \{h\}, q) \)). We use also \( \text{delete}(m, h) \) to denote the memory type \( m = (r, v, p, S \setminus \{h\}) \) (resp. \( m = (r, v, p, S \setminus \{h\}, q) \)). This corresponds to the addition/deletion of the process \( h \) to/from the set of pointers of the memory type \( m \).

**Simple Words.** A simple word is a word \( \in \Sigma^*\#(\Sigma \cup \Gamma) \), and each \( \text{HW}_x \) is a word \( \in (\Sigma^*\#(\Sigma \cup \Gamma))^\ast \). # is a special symbol not in \( \Sigma \cup \Gamma \), which separates the last symbol from the rest of the simple word. Consecutive symbols of \( \Sigma \) in a simple word represent adjacent messages/promises in the memory of PS 2.0-rlx, and are hence unavailable for a RMW. The special symbol \# segregates these from the last symbol of \( \Sigma \cup \Gamma \) in a simple word. \# does not correspond to any element from the memory; its job is simply to demarcate the messages/promises which are not available for RMW from the last symbol of the simple word. If the last symbol in a simple word is in \( \Sigma \), then it is available for a RMW; if the last symbol is in \( \Gamma \), then it is not available for a RMW since the next message adjacent to this symbol is a reservation. The last symbol from \( \Sigma \cup \Gamma \) in a simple word \( \Sigma^*\#(\Sigma \cup \Gamma) \) thus represents a message/promise (combined with or not a reservation) in the memory which is adjacent to the messages represented by the symbols immediately preceding \# (if any).

![Fig. 6. A higher order word HW.](image)

**Higher order words.** A higher order word is a sequence of simple words. Figure 6 depicts a higher order word with four simple words. We use a left to right order in both simple words and higher order words. Furthermore, we extend in the straightforward manner the classical word indexation strategy to higher order words. For example, the symbol at the third position of the higher order word \( \text{HW} \) given in Figure 6 is \( \text{HW}[3] = (\text{msg}, 2, p, \{p, q\}) \). A higher order word \( \text{HW} \) is well-formed iff for every \( p \in \mathcal{P} \), there is a unique position \( i \) in \( \text{HW} \) having \( p \) in its pointer set; that is, \( \text{HW}[i] \) is of the form \((-,-,-,S) \in \Sigma \) or \((-,-,-,S,-) \in \Gamma \) s.t. \( p \in S \). Observe that the higher order word given in Figure 6 is well-formed. We will use \( \text{ptr}(p, \text{HW}) \) to denote the unique position \( i \) in \( \text{HW} \) having \( p \) in its pointer set. Next, we assume that all the manipulated higher order words are well-formed.

As already mentioned, for each \( x \in \text{Loc} \), we have a higher order word \( \text{HW}_x \). The higher order word \( \text{HW}_x \) represents the entire space \([0, \infty) \) of available timestamps. Each simple word in \( \text{HW}_x \) represents a timestamp interval \( (f, t) \), with consecutive simple words representing disjoint timestamp intervals (while preserving order). The memory types in each simple word take up adjacent timestamp intervals, spanning the timestamp interval of the simple word. This adjacency of timestamp intervals within simple words is mainly used in RMW steps and reservations. The memory type in \( \Sigma \) occurring at the end of a simple word denotes a message/promise which is available for a RMW operation. The memory type in \( \Gamma \) occurring at the end of a simple word denotes a message/promise followed by a reservation and therefore it is not available for a RMW operation. The memory types at positions other than the rightmost in a simple word, represent messages/promises which are not available for RMW. Figure 7 presents a mapping from a memory of PS 2.0-rlx to a collection of higher order words (one per location) in LoHoW.

Given a higher order word \( \text{HW} \), a position \( i \in \{1, \ldots, |\text{HW}|\} \), and \( p \in \mathcal{P} \), we use \( \text{add}(\text{HW}, p, i) \) (resp. \( \text{delete}(\text{HW}, p) \)) to denote the higher order word \( \text{HW}[1, i - 1] \cdot \text{add}(\text{HW}[i], p) \cdot \text{HW}[i + 1, |\text{HW}|] \) (resp. \( \text{HW}[1, i - 1] \cdot \text{delete}(\text{HW}[\text{ptr}(p, \text{HW})], p) \cdot \text{HW}[i + 1, |\text{HW}|] \)). This corresponds
to the addition/deletion of \( p \) to/from the set of pointers of \( HW[i]/HW[ptr(p, HW)] \). We use \( move(HW, p, i) \) to denote \( add(delete(HW, p), p, i) \).

![Diagram](image-url)

**Fig. 7.** A mapping from memories \( M(x), M(y) \) to higher order words \( HW_x, HW_y \), respectively.

**Initializing higher order words.** For each location \( x \in \text{Loc} \), the initial higher order word \( HW_x^{\text{init}} \) is defined as \( \#(\text{msg}, 0, p, \mathcal{P}) \), where \( \mathcal{P} \) is the set of all processes and \( p_1 \) is some process in \( \mathcal{P} \). The set of all higher order words \( HW_x^{\text{init}} \) for all locations \( x \) represents the initial memory of PS 2.0-rlx where all locations have value 0, and all processes are aware of the initial message.

**Simulating Reads, Writes, RMWs in LoHoW.** In the following, we informally describe how to handle PS 2.0-rlx instructions in LoHoW. Since we only have the r1x access mode, we denote Reads, Writes and RMWs as \( wt(x, v) \), \( rd(x, v) \) and \( U(x, v_r, v_w) \), dropping the access modes.

**Reads.** A \( rd(x, v) \) step by a process \( p \) (reading \( v \) from \( x \)) is handled as follows in LoHoW.

There exists an index \( j \geq \text{ptr}(p, HW_x) \) in \( HW_x \) such that \( HW_x[j] \) is of the form \((-, v, -, S')\) or \((-, v, -)\). This corresponds to the existence of a memory type holding the value \( v \) in \( HW_x \) and this symbol is on the right of the current view/pointer of the process \( p \).

Add \( p \) to the set of pointers \( S' \) and remove it from its previous position.

**Writes.** A \( wt(x, v) \) step by a process \( p \) (writing the value \( v \) to the location \( x \)) in PS 2.0-rlx is done by adding a new message with a timestamp higher than the local view of \( p \) for \( x \): the timestamp interval of this new message can be adjacent to the timestamp of the local view of \( p \), or much ahead. These two possibilities are captured in LoHoW as follows.

1. Add the simple word \( \#(\text{msg}, v, p, \{p\}) \) to \( HW_x \) to the right of \( \text{ptr}(p, HW_x) \), or
2. there is a symbol \( \alpha \in \Sigma \) and two words \( w \) and \( w' \) such that \( HW_x = w \cdot \# \cdot \alpha \cdot w' \). Then, update the higher order word \( HW_x \) to \( w \cdot \# \cdot (\text{msg}, v, p, \{p\}) \cdot w' \).

Finally, remove \( p \) from its previous pointer set.

**RMW.** Capturing RMWs is similar to the execution of a read followed by a write. In PS 2.0-rlx, a process \( p \) performing RMW reads from a message with a timestamp interval \((t, \cdot]\) and adds a message to the memory with timestamp interval \((\cdot, -]\). This is handled as follows in LoHoW, and shows the need for the higher order words. Consider a \( U(x, v_r, v_w) \) step by \( p \). Then,

there is a symbol \( \cdots \#(\cdot, v_r, \cdot, S) \) in \( HW_x \) having \((\cdot, v_r, \cdot, S)\) as the last memory type in it, and the position of the memory type \((\cdot, v_r, \cdot, S)\) is on the right of the current pointer of \( p \) in \( HW_x \). \( p \) is removed from its pointer set, \( \#(\cdot, v_r, \cdot, S) \) is replaced with \((\cdot, v_r, S \setminus \{p\})\# \) and \((\cdot, v_w, p, \{p\}) \) is appended, resulting in extending \( \cdots \#(\cdot, v_r, \cdot, S) \) to \( \cdots \#(\cdot, v_r, \cdot, S \setminus \{p\})\#(\cdot, v_w, p, \{p\}) \).

**Example 4.1.** We illustrate the read, write and RMW in LoHoW on an example. Figure 8 depicts a run in PS 2.0-rlx and the corresponding run in LoHoW. The run of PS 2.0-rlx shows how the
memory evolves, and the corresponding run in LoHoW faithfully simulates this using higher order words \(HW_x\) and \(HW_y\).

\[
\begin{align*}
x &:= 1 & x &:= 5 \\
y &:= 2 & \textcolor{red}{r1} &:= x / 3 \\
x &:= 3 & \textcolor{red}{r2} &:= \text{FADD}(y, 1) / 2
\end{align*}
\]

![Diagram showing changes to memory and corresponding run in LoHoW.](image)

**Fig. 8.** Below, a run in PS 2.0 showing the changes to memory, and above, the corresponding run in LoHoW.

Observe that \(\text{init}\) stands for the initial memory.

**Promises in LoHoW.** Next, we discuss how to handle promises.

Promises. Handling promises made by a process \(p\) in PS 2.0-rlx is similar to handling \(\text{wt}(x, v)\): we add the simple word \(#(\text{prm}, v, p, \{\})\) to the right of the position \(\text{ptr}(p, HW_x)\), or append \((\text{prm}, v, p, \{\})\) at the end of a simple word with a position larger than \(\text{ptr}(p, HW_x)\). Other than tagging the symbol as a promise \((\text{prm})\), the pointer set is empty.

**Reservations and Cancellations in LoHoW.** Next, we come to one of the new features of PS 2.0 over the first version, namely, reservations and cancellations. In PS 2.0-rlx, a process \(p\) makes a reservation by adding the pair \((x, (f, t))\) to the memory, given that there is a message/promise in the memory with timestamp interval \((-f, f]\). In LoHoW this is captured by “tagging” the rightmost memory type (message/promise) in a simple word with the name of the process that makes the reservation. This requires us to consider the memory types from \(\Gamma = \{\text{msg}, \text{prm}\} \times \text{Val} \times \text{P} \times 2^\text{P} \times \text{P}\) where the last component stores the process which made the reservation. Such a memory type always appears at the end of a simple word, and represents that the next timestamp interval adjacent to it has been reserved. Observe that we can not add new memory types to the right of a memory type of the form \((\text{msg}, v, p, S, q)\). Thus, reservations are handled as follows.

1. **(Res)** Assume the rightmost symbol in a simple word as \((\text{msg}, v, p, S, q)\). To capture the reservation by \(q\), \((\text{msg}, v, p, S)\) is replaced with \((\text{msg}, v, p, S, q)\).
2. **(Can)** A cancellation is done by removing the last component \(q\) from \((\text{msg}, v, p, S, q)\) resulting in \((\text{msg}, v, p, S)\).

**Empty Memory Types, Redundant simple words.** When a process \(p\) reads from a message, the pointer of \(p\) is updated, and moves forward. As a result, we may have memory types of the form \((\text{msg}, v, p, \{\})\) as well as \((\text{msg}, v, p, \{\}, q)\) representing those messages in the memory whose pointer set is empty. Call such symbols of \(\Sigma \cup \Gamma\) empty memory types. It is then possible to lose an empty memory type of \(\Sigma\) from a simple word if it is not at the rightmost position. This will not have any
consequence with respect to the reachability problem, since processes can non-deterministically skip reading some messages in the memory. Likewise, a simple word of the form $w \# m \in \Sigma^*(\Sigma \cup \Gamma)$ where all symbols in $w$ are empty memory types from $\Sigma$ and $m$ is an empty memory type from $\Sigma \cup \Gamma$ can be lost entirely. Such simple words are called redundant simple words. Given this, what cannot be lost from $\text{HW}_x$? The following:

- memory types $(\text{prm}, \epsilon, \epsilon, \epsilon)$ or $(\text{prm}, \epsilon, \epsilon, \epsilon, \epsilon)$ representing promises. This is due to the fact promises should be fulfilled and therefore can not be lost.
- non empty memory types: the pointer set of these contain at least one process. Since losing any of these memory types will result in losing the pointer/view of at least one of the processes.
- Only rightmost memory type (right next to #) in a simple word. Losing only this memory type will result in a non well-defined higher order word.

Certification and Fulfilment. In PS 2.0-rlx, certification, for a process $p$, happens from the capped memory, where intermediate time slots (other than reserved ones) are blocked, and any new message can be added only at the maximal timestamp. This is handled in LoHoW by one of the following:

- addition of new memory types is only allowed only at the right end of any $\text{HW}_x$.
- If the rightmost memory type $m$ in $\text{HW}_x$ is of the form $(\epsilon, v, \epsilon, \epsilon, q)$ with $q \neq p$ (i.e., tagged by a reservation for $q$), then a simple word $\#(\text{msg}, v, q, \{\})$ is appended at the end of $\text{HW}_x$.

Memory is altered in PS 2.0-rlx during certification phase to check for promise fulfilment, and at the end of the certification phase, we resume from the memory which was there before. To capture this in LoHoW, we work on a duplicate of $(\text{HW}_x)_{x \in \text{Loc}}$ in the certification phase. Notice that the duplication allows losing some of empty memory types and redundant simple words non deterministically (as described in the previous paragraph). This copy of $\text{HW}_x$ is then modified during certification, and is discarded once we finish the certification phase.

The fulfilment of a promise by $p$ using the rule $\xrightarrow{\text{L}}$ (see rule (MEMORY : FULFILL) in Figure 2) will be handled in a similar manner as using the rule $\xrightarrow{\text{A}}$ (since we are only dealing with the fragment of PS 2.0 restricted to rlx). This will result in replacing a memory type of the form $(\text{prm}, v, p, S)$ (resp. $(\text{prm}, v, p, S, q)$) by $(\text{msg}, v, p, S)$ (resp. $(\text{msg}, v, p, S, q)$) if this memory type is in a position which is on the right of the current pointer of the process $p$. Then, the process $p$ is added to the pointer set $S$ while removing it from the previous pointer set it belongs to.

The fulfilment of a promise by a process $p$ in PS 2.0 using the rule $\xleftarrow{\text{S}}$ (see rule (MEMORY : FULFILL) in Figure 2) results in splitting the intervals of the promise, when adding a new message $(x, v', (f, t), \perp)$ to the memory. To capture this, we allow insertion of a memory type right before the promise whose interval is split. This will result in replacing a memory type of the form $(\text{prm}, v, p, S)$ (resp. $(\text{prm}, v, p, S, q)$) by $(\text{msg}, v', p, \{\})$ if this memory type is in a position which is on the right of the current pointer of the process $p$. Then, the process $p$ is removed from the previous pointer set it belongs to. We may also need to update the position of the separator # so that it is just before the last symbol of a simple word.

SC fences. SC-fences are handled by adding a dummy process $g$ to $P$. Whenever a process $p$ performs a SC fence, $g, p$ are added to the same pointer set, by moving $g(p)$ to the pointer set of $p$ (g) depending on which is more to the right.

Example 4.2. Figure 9 illustrates a run in LoHoW on a program where promises are necessary to reach the annotated part $//$. To reach the annotated part in P1, the execution proceeds as follows. C1, C2 represent two certification phases.

1. P1 promises the write of 42 to $x$, by a message $(x, 42, (f, t), \perp)$.
(C1) To certify, P1 begins from the capped memory, and enters the else branch. It begins a duplicate of the higher order words, and works on them in this phase.

- Since all positions in \((0, t]\) are blocked, P1 splits the interval \((f, t]\) to write 41 to \(x\), and modifies the memory to \((x, 42, (t', t], \bot), (x, 41, (f, t'], \bot)\).
- P1 fulfils its promise

(2) P2 reads 42 from \(x\) and writes 42 to \(z\)
(3) P1 reads 42 from \(z\)
(4) P1 fulfils its promise, and reaches the annotated part.

![Diagram](Fig. 9. Run in LoHoW. The certification phase works on the duplicates of HW_1, HW_2 denoted in yellow.)

### 4.2 Formal Model of LoHoW

In the following, we formally define LoHoW and state the equivalence of the reachability problem in PS 2.0-rlx and LoHoW.

**Insertion into higher order words.** A higher order word HW can be extended in position \(1 \leq j \leq |HW|\) with a memory type \(m\) of the form \((r, v, p, \{p\})\) in a number of ways:

- **Insertion as a new simple word.** \(HW \xrightarrow{N_j} m\) is defined only if \(HW[j - 1] = \#\) (i.e., the position \(j\) is the end of a simple word). Let \(HW'\) be the higher order word defined as delete(HW, \(p\)) (i.e., removing \(p\) from its previous set of pointers). Then, the extended higher order HW \(\xrightarrow{N_j} m\) is defined as \(HW'[1, j] \cdot \#m \cdot HW'[j + 1, |HW|]\) (i.e., inserting the new simple word just after the position \(j\)).

- **Insertion at the end of a simple word.** \(HW \xrightarrow{E_j} m\) is defined only if \(HW[j - 1] = \#\) (i.e., the position \(j\) is the end of a simple word) and \(HW[j] \in \Sigma\) (i.e., the last memory type in the simple word should be free from reservations). Let \(HW'\) be the higher order word defined as delete(HW, \(p\)). Then, the extended higher order HW \(\xrightarrow{E_j} m\) is defined as \(w_1 \cdot m' \cdot \#m \cdot w_2\) with HW' = \(w_1 \cdot \#m' \cdot w_2\), and \(m' \in \Sigma\), and \(|w_1 \cdot \#m'| = j\) (i.e., inserting the new memory type just after the position \(j\)).

- **Splitting a promise.** \(HW \xrightarrow{SP_j} m\) is defined only if HW[j] is of the form \((\text{prm}, -, p, -)\) or \((\text{prm}, -, p, -, -)\) (i.e., the memory type at position \(j\) is a promise). Let \(HW'\) be the higher order word defined as delete(HW, \(p\)). Then, the extended higher order HW \(\xrightarrow{SP_j} m\) is defined as (1) \(HW'[1, j - 2] \cdot m \cdot \#m' \cdot HW'[j + 1, |HW|]\) if \(HW'[j] = m'\) and \(HW'[j - 1] = \#\), or (2) \(HW'[1, j - 1] \cdot m \cdot m' \cdot HW'[j + 1, |HW|]\) if \(HW'[j] = m'\) and \(HW'[j - 1] \neq \#\). Observe that in both cases we are inserting the new memory type \(m\) just before the position \(j\).

- **Fulfilment of a promise.** \(HW \xrightarrow{FP_j} m\) is defined only if HW[j] is of the form \((\text{prm}, v, p, S)\) or \((\text{prm}, v, p, S, q)\). Let \(HW'\) be the higher order word defined as delete(HW, \(p\)). Then, the extended
higher order HW \overset{FP}{\longleftarrow} m is defined as HW'[1, j - 1] \cdot m'. HW'[j + 1, |HW'|] with m' = (msg, v, p, S \cup \{p\}) if HW[j] = (prm, v, p, S) and m' = (msg, v, p, S \cup \{p\}, q) if HW[j] = (prm, v, p, S, q).

- **Splitting a reservation.** HW \overset{SR}{\longleftarrow} j m is defined only if HW[j] is of the form (r', v', q, S, p). Let HW'

be the higher order word defined as delete(HW, p). Then, the extended higher order HW \overset{SR}{\longleftarrow} j m is defined as HW'[1, j - 2] \cdot (r', v', q, S) \cdot \#(r, v, p, \{p\}, p) \cdot HW'[j + 1, |HW'|]. Observe that the new message (r, v, p, \{p\}, p) is added to the right of the position j which corresponds to the slot that has been reserved by p. This special splitting rule will be used during the certification phase. This will allow the process p to use the reserved slots. Recall that it is not allowed to add memory types in the middle of the higher order words (other than the reserved ones) during the certification phase.

**Making/Canceling a reservation.** Another higher order word HW can also be modified through making/cancelling a reservation at a position 1 \leq j \leq |HW| by a process p. Thus, we define the operation Make(HW, p, j) (resp. Cancel(HW, p, j)) that reserves (resp. cancels) a time slot at the position j. Make(HW, p, j) (resp. Cancel(HW, p, j)) is only defined if HW[j] is of the form (r, v, q, S) (resp. (r, v, q, S, p)) and HW[j - 1] = \#. Then, the extended higher order Make(HW, p, j) (resp. Cancel(HW, p, j)) is defined as HW[1, j - 1] \cdot (r, v, q, S, p) \cdot HW'[j + 1, |HW'|] (resp. HW[1, j - 1] \cdot (r, v, q, S) \cdot HW[j + 1, |HW'|]).

**Process configuration in LoHoW.** A configuration of p ∈ P in LoHoW consists of a pair (σ, HW) where (1) σ is the process state maintaining the instruction label and the register values (see Subsection 2.3), and HW is a mapping from the set of locations to higher order words. The transition relations \overset{std}{\to} and \overset{cert}{\to} between process configuration is given in Figure 10. The transition relation \overset{cert}{\to}_p is used only in the certification phase while \overset{std}{\to}_p is used to simulate the standard phase of PS 2.0-rlx. A read operation in both phases (standard and certification) is handled by reading a value from a memory type which is on the right of the current pointer of p. A write operation, in the standard phase, can result in the insertion, on the right of the current pointer of p, of a new memory type at the end of a simple word or as a new simple word. The memory type resulting from a write in the certification phase is only allowed to be inserted at the end of the higher order word or at the reserved slots (using the rule splitting a reservation). Write can also be used to fulfil a promise or to split a promise (i.e., partial fulfilment) during the both phases. Making/canceling a reservation will result in tagging/untagging a memory type at the end of a simple word on the right of the current pointer of p. The case of RM is similar to a read followed by a write operations (whose resulting memory type should be inserted to the right of the read memory type). Finally, a promise can only be made during the standard phase and the resulting memory type will be inserted at the end of a simple word or as a new word on the right of the current pointer of p.

**Losses in LoHoW.** Let HW and HW' be two higher order words in (Σ^* #(Σ ∪ Γ))^+. Let us assume that HW = u_1 #a_1 u_2 #a_2 \ldots u_k #a_k and HW' = v_1 #b_1 v_2 #b_2 \ldots v_m #b_m, with u_i, v_i ∈ Σ^* and a_i, b_j ∈ Σ ∪ Γ. We extend the subword relation ⊆ to higher order word as follows: HW ⊆ HW' iff there is a strictly increasing function f : \{1, \ldots, k\} → \{1, \ldots, m\} s.t. (1) u_i ⊆ v_{f(i)} for all 1 ≤ i ≤ k, (2) a_i = b_{f(i)} and (3) we have the same number of memory types of the form (prm, v, p, S) or (prm, v, p, S, q) in HW and HW'. The relation ⊆ corresponds to the loss of some special empty memory types and redundant simple words (as explained earlier). The relation ⊆ is extended to mapping from locations to higher order words as follows: HW ⊆ HW' iff HW(x) ⊆ HW'(x) for all x ∈ Loc.

**LoHoW states.** A LoHoW state st is a tuple ((J, R), HW) where J : P ↦ Loc maps each process p to the label of the next instruction to be executed, R : Reg ↦ Val maps each register to its current
The Decidability of Verification under Promising 2.0

Fig. 10. LoHoW inference rules at the process level, defining the transition \( \sigma, \text{HW} \xrightarrow{a \in \{\text{std, cert}\}} \sigma', \text{HW}' \) where \( p \in \mathcal{P} \) and \( a \in \{\text{std, cert}\} \) is the current mode. \( \sigma = (J, R) \) and \( \sigma' = (J', R') \) represent local process states.

value, and \( \text{HW} \) is a mapping from locations to higher order words. The initial LoHoW state \( s_{\text{init}} \) is defined as \( (J_{\text{init}}, R_{\text{init}}, \text{HW}_{\text{init}}) \) where: (1) \( J_{\text{init}}(p) \) is the label of the initial instruction of \( p \); (2) \( R_{\text{init}}(sr) = 0 \) for every register \( sr \in \mathcal{R} \); and (3) \( \text{HW}_{\text{init}}(x) = \text{HW}_{X}^{\text{init}} \) for all \( x \in \mathcal{L} \).

Now we are ready to define the induced transition relation between LoHoW states. For two LoHoW states \( s = ((J, R), \text{HW}) \) and \( s' = ((J', R'), \text{HW}') \) and \( a \in \{\text{std, cert}\} \), we write \( s \xrightarrow{a \in \{\text{std, cert}\}} s' \) if one of the following cases holds: (1) \( ((J(p), R), \text{HW}) \xrightarrow{a \in \{\text{std, cert}\}} ((J'(p), R'), \text{HW}') \) and \( J(p') = J'(p') \) for all \( p' \neq p \), or (2) \( (J, R) = (J', R') \) and \( \text{HW} \sqsubseteq \text{HW}' \).

**Two phases** LoHoW states. A two-phases state of LoHoW is \( S = (\pi, p, s_{\text{std}}, s_{\text{cert}}) \) where \( \pi \in \{\text{std, cert}\} \) is a flag describing whether the LoHoW is in "standard" phase or "certification" phase, \( p \) is the process which evolves in one of these phases, while \( s_{\text{std}}, s_{\text{cert}} \) are two LoHoW states (one for each phase). When the LoHoW is in the standard phase, then \( s_{\text{std}} \) evolves, and when the LoHoW is in certification phase, \( s_{\text{cert}} \) evolves. A two-phases LoHoW state is said to be initial if it is of the form \( (\text{std}, p, s_{\text{std}}, s_{\text{init}}) \), where \( p \in \mathcal{P} \) is any process. The transition relation \( \rightarrow \) between two-phases LoHoW states is defined as follows: Given \( S = (\pi, p, s_{\text{std}}, s_{\text{cert}}) \) and \( S' = (\pi', p', s'_{\text{std}}, s'_{\text{cert}}) \), we have \( S \rightarrow S' \) if one of the following cases hold:

- **During the standard phase.** \( \pi = \pi' = \text{std} \), \( p = p' \), \( s_{\text{cert}} = s'_{\text{cert}} \) and \( s_{\text{std}} \xrightarrow{p} s'_{\text{std}} \). This corresponds to a simulation of a standard step of the process \( p \).
• During the certification phase. \( \pi = \pi' = \text{cert} \), \( p = p' \), \( s_t\text{std} = s'_t\text{std} \) and \( s_t\text{cert} \xrightarrow{\text{cert}} p \xrightarrow{\text{p}} s'_t\text{cert} \).

This corresponds to a simulation of a certification step of the process \( p \).

• From the standard phase to the certification phase. \( \pi = \text{std} \), \( \pi' = \text{cert} \), \( p = p' \), \( s_t\text{std} = s'_t\text{std} = ((J, R), \text{HW}) \) and \( s_t\text{cert} \) is of the form \(((J, R), \text{HW})'\) where for every \( x \in \text{Loc} \), \( \text{HW}'(x) = \text{HW}(x)\#(\text{msg}, v, q, \{\}) \) if \( \text{HW}(x) \) is of the form \( w \cdot \#(-, v, -, q) \) with \( q \neq p \), and \( \text{HW}'(x) = \text{HW}(x) \) otherwise. This corresponds to the copying of the standard LoHoW state to the certification LoHoW state in order to check if the set of promises made by the process \( p \) can be fulfilled. The higher order word \( \text{HW}'(x) \) (at the beginning of the certification phase) is almost the same as \( \text{HW}(x) \) (at the end of the standard phase) except when the rightmost memory type \((-v, -, -, q)\) of \( \text{HW}(x) \) is tagged by a reservation of a process \( q \neq p \). In that case, we append the memory type \((\text{msg}, v, q, \{\})\) at the end of \( \text{HW}(x) \) to obtain \( \text{HW}'(x) \). Note that this is in accordance to the definition of capping memory before going into certification: to cite, (item 2 in capped memory of [Lee et al. 2020]), a cap message is added for each location unless it is a reservation made by the process going in for certification. It is easy to see that this transition rule can be implemented by a sequence of transitions which copies one symbol at a time, from \( \text{HW} \) to \( \text{HW}' \).

• From the certification phase to standard phase. \( \pi = \text{cert} \), \( \pi' = \text{std} \), \( s_t\text{std} = s'_t\text{std} \), \( s_t\text{cert} = s'_t\text{cert} \), and \( s_t\text{cert} \) is of the form \(((J, R), \text{HW})'\) with \( \text{HW}(x) \) does not contain any memory type of the form \((\text{prm}, -, p, -)/(\text{prm}, -, p, -, -)\) for all \( x \in \text{Loc} \) (i.e., all promises made by \( p \) are fulfilled).

The Reachability Problem in LoHoW. Given an instruction label function \( J : P \rightarrow \mathbb{L} \) that maps each \( p \in P \) to a label in \( \mathbb{L} \), the reachability problem in LoHoW asks whether there exists a two phases LoHoW state \( S \) of the form \((\text{std}, -), ((J, R), \text{HW}), ((J', R'), \text{HW}')\) s.t. (1) \( \text{HW}(x) \) and \( \text{HW}'(x) \) do not contain any memory type of the form \((\text{prm}, -, p, -)/(\text{prm}, -, p, -, -)\) for all \( x \in \text{Loc} \), and (2) \( S \) is reachable in LoHoW (i.e., \( S_0[\rightarrow]^* S' \) where \( S_0 \) is an initial two-phases LoHoW states). In the case of a positive answer to this problem, we say that \( J \) is reachable in \( \text{Prog} \) in LoHoW.

Theorem 4.3. An instruction label function \( J \) is reachable in a program \( \text{Prog} \) in LoHoW iff \( J \) is reachable in \( \text{Prog} \) in PS 2.0-rlx.

4.3 Decidability of LoHoW with Bounded Promises

The equivalence of the reachability in LoHoW and PS 2.0-rlx, coupled with Theorem 3.1 shows that reachability is undecidable in LoHoW. To recover decidability, we look at LoHoW with only bounded number of the promise memory type in any higher order word. Let K-LoHoW denote LoHoW with a number of promises bounded by \( K \). (Observe that K-LoHoW corresponds to bdPS 2.0-rlx.)

Theorem 4.4. The reachability problem is decidable for K-LoHoW.

As a corollary of Theorem 4.4, the decidability of reachability follows for bdPS 2.0-rlx. The proof makes use of the framework of Well-Structured Transition Systems (WSTS) [Abdulla and Jonsson 1996; Finkel and Schnoebelen 2001], and follows from lemmas 4.5 to 4.8.

Well-Structured Transition Systems (WSTS). We recall the main ingredients of WSTS. For more details, the reader is referred to Abdulla and Jonsson [1996]; Finkel and Schnoebelen [2001].

Well-quasi Orders. Given a (possibly infinite set) \( C \), a quasi-order on \( C \) is a reflexive and transitive relation \( \leq \subseteq C \times C \). An infinite sequence \( c_1, c_2, \ldots \) in \( C \) is said to be saturating if there exists indices \( i < j \) s.t. \( c_i \leq c_j \). A quasi-order \( \leq \) is said to be a well-quasi order (wqo) on \( C \) if every infinite sequence in \( C \) is saturating. Given a quasi-order \( \leq \) on \( C \), the embedding order \( \sqsubseteq \) on \( C^* \) (i.e., the set of finite words over \( C \)) is defined as \( a_1a_2 \ldots a_m \sqsubseteq b_1b_2 \ldots b_n \) if there exists a strictly increasing
function $g : \{1, 2, \ldots, m\} \rightarrow \{1, 2, \ldots, n\}$ s.t. for all $1 \leq i \leq m$, $a_i \leq b_{g(i)}$. It is well-known that if $\leq$ is a wqo on $C$, then the embedding order $\sqsubseteq$ is also a wqo on $C^*$ [Higman 1952].

**Upward Closure.** Given a wqo $\leq$ on a set $C$, a set $U \subseteq C$ is upward closed if for every $a \in U$ and $b \in C$, with $a \leq b$, we have $b \in U$. The upward closure of a set $U \subseteq C$ is $U^\uparrow = \{ b \in C \mid \exists a \in U, a \leq b \}$. It is known that every upward closed set $U$ can be characterized by a finite minor. A minor $M \subseteq U$ is s.t. (i) for each $a \in U$, there is a $b \in M$ s.t. $b \leq a$, and (ii) for all $a, b \in M$ s.t. $a \leq b$, we have $a = b$.

For an upward closed set $U$, let min be the function that returns the minor of $U$.

**Well-Structured Transition Systems (WSTS).** Let $\mathcal{T}$ be a transition system with (possibly infinite) set of states $C$, initial states $C_{\text{init}}$ and transition relation $\leadsto \subseteq C \times C$. Let $\leq$ be a well-quasi ordering on $C$. We define the set of predecessors of a subset $U \subseteq C$ of states as $\text{Pre}(U) = \{ c \in C \mid \exists c' \in U. c \leadsto c' \}$. For a state $c$, we denote the set $\min(\text{Pre}(\{c\}^\uparrow) \cup \{c\}^\uparrow)$ as $\minpre(c)$. $\mathcal{T}$ is called well-structured if $\leadsto$ is monotonic w.r.t. $\leq$ that is, given $c_1, c_2$ and $c_3$ in $C$, if $c_1 \leadsto c_2$ and $c_1 \leq c_3$, then there exists a state $c_4$ s.t. $c_3 \leadsto c_4$ and $c_2 \leq c_4$.

Given a finite set of states $C_{\text{target}} \subseteq C$, the coverability problem asks if there is a state $c' \in C_{\text{target}}$ reachable in $\mathcal{T}$. The following conditions are sufficient for the decidability of this problem: (i) for every two states $c_1, c_2 \in C$, it is decidable if $c_1 \leq c_2$, (ii) for every $c \in C$, we can check if $\{c\}^\uparrow \cap C_{\text{init}} \neq \emptyset$, and (iii) for all $c \in C$, the set $\minpre(c)$ is finite and computable.

The algorithm for checking WSTS coverability is based on a backward analysis. The sequence $(U_i)_{i \geq 0}$ with $U_0 = \min(C_{\text{target}})$ and $U_{i+1} = \min(\text{Pre}(U_i) \cup U_i)$ reaches a fixpoint and is computable [Abdulla and Jonsson 1996; Finkel and Schnoebelen 2001].

**LoHoW with bounded promises is a WSTS.** We will show that the K-LoHoW transition system is a well-structured transition system. Let $C$ denote the set of two-phases K-LoHoW states of Prog. Given an instruction label function $J : \mathcal{P} \rightarrow \mathcal{L}$, let $C_{\text{target}}$ be a finite subset of $C$ of the form $(\text{std}, - , ((J, R), \mathcal{H}), ((J', R'), \mathcal{H}'))$ such that for every $x \in \text{Loc}$, we have: (1) $\mathcal{H}(x)$ and $\mathcal{H}'(x)$ do not contain any memory type of the form $(\text{prom}, -, p, -) / (\text{prom}, -, p, -)$, and (2) $\|\mathcal{H}(x)\|, \|\mathcal{H}'(x)\| \leq |\mathcal{P}|$. We define the well-quasi ordering $\sqsubseteq$ on $C$ in a way that the upward closure of $C_{\text{target}}$ consists of all two-phases K-LoHoW states of the form $(\text{std}, - , ((J, R), \mathcal{H}), ((J', R'), \mathcal{H}'))$ such that for every $x \in \text{Loc}$, $\mathcal{H}(x)$ and $\mathcal{H}'(x)$ do not contain any memory type of the form $(\text{prom}, -, p, -) / (\text{prom}, -, p, -)$. Then, the coverability of $C_{\text{target}}$ is equivalent to the reachability of $J$ in K-LoHoW.

In the following, we define the well-quasi ordering $\sqsubseteq$ on on $C$ (Lemma 4.5). Then, we show the monotonicity of the K-LoHoW transition relation $\rightarrow$ w.r.t. $\sqsubseteq$ (Lemma 4.7). Finally, we show how to compute the set of predecessors of a given two-phases K-LoHoW state (Lemma 4.8). Observe that the first and second sufficient conditions for the decidability of the coverability problem, namely comparing two states and checking whether an upward closure set contains the initial state, are trivial (the second condition can be reduced whether a minimal state is equal to the initial state).

The ordering $\sqsubseteq$ defined on mapping from locations to higher order words can be extended to two phases K-LoHoW states by component wise extension: $(\pi, p, ((J_1, R_1), \mathcal{H}_1), ((J_2, R_2), \mathcal{H}_2)) \sqsubseteq (\pi', p', ((J'_{1}, R'_{1}), \mathcal{H}'_{1}), ((J'_{2}, R'_{2}), \mathcal{H}'_{2}))$ holds iff $\pi' = \pi$, $p' = p$, $(J_1, R_1) = (J'_{1}, R'_{1})$, $(J_2, R_2) = (J'_{2}, R'_{2})$, $\mathcal{H}_1 \sqsubseteq \mathcal{H}'_1$, and $\mathcal{H}_2 \sqsubseteq \mathcal{H}'_2$. Since the embedded ordering $\sqsubseteq$ is a wqo on higher order words when the number of promises is bounded [Higman 1952], we obtain the following lemma.

**Lemma 4.5.** The relation $\sqsubseteq$ is a well-quasi ordering on the two phases K-LoHoW states.

Consider now a two-phases K-LoHoW state $S$ of the form $(\text{std}, - , ((J, R), \mathcal{H}), ((J', R'), \mathcal{H}'))$ such that for every $x \in \text{Loc}$, $\mathcal{H}(x)$ and $\mathcal{H}'(x)$ do not contain any memory type of the form $(\text{prom}, -, p, -) / (\text{prom}, -, p, -)$, then it is easy to see that $S \in C_{\text{target}}$. This implies that:

**Lemma 4.6.** The coverability of $C_{\text{target}}$ is equivalent to the reachability of $J$ in K-LoHoW.
**Monotonicity.** The following lemma shows the monotonicity of the K-LoHoW transition relation $\rightarrow$ w.r.t. $\sqsubseteq$. This allows the backward algorithm for coverability to work with only upward closed sets, since the set of predecessors of an upward closed set is also upward closed [Abdulla and Jonsson 1996; Finkel and Schnoebelen 2001].

**Lemma 4.7.** The transition relation $\rightarrow$ is monotonic w.r.t. $\sqsubseteq$.

**Computing the set of predecessors.** The last sufficient condition for the decidability of the coverability problem in K-LoHoW is stated by the following lemma

**Lemma 4.8.** For each two-phases K-LoHoW state $c$, the set $\text{minpre}(c)$ is effectively computable.

Next, we state that the reachability problem for K-LoHoW (even for $K = 0$) is highly non-trivial (i.e., non-primitive recursive). The proof is done by reduction from the reachability problem for lossy channel systems, in a similar to the case of TSO [Atig et al. 2010] where we insert SC-fence instructions everywhere in the process that simulates the lossy channel process (in order to ensure that no promises can be made by that process).

The proof is done by reduction from the reachability problem for lossy channel systems (LCS). We construct a concurrent program with 2 processes, the first process $p_1$ keeps track of the finite state control of the LCS, while the second process $p_2$ simulates the lossy channel. Two shared variables $x_c, y_c$ are used to simulate the lossy channel $c$. $p_1$ writes to $x_c$ on each transition that writes to $c$ in the LCS. $p_2$ reads from $x_c$ and writes to $y_c$. A read from the channel $c$ in the LCS is simulated by $p_1$ reading from $y_c$, thereby simulating the lossiness of $c$ ($p_2$ can skip some messages of $x_c$, and $p_1$ can also skip some messages of $y_c$). Every two instructions of $p_1, p_2$ have a SC-fence to ensure no promises can be made (and fulfilled).

**Theorem 4.9.** The reachability problem for K-LoHoW is non-primitive recursive.

## 5 SOURCE TO SOURCE TRANSLATION

We consider a parametric under-approximation in the spirit of context bounding [Atig et al. 2011], [La Torre et al. 2009], [Lal and Reps 2009], [Norris and Demsky 2016], [Musuvathi and Qadeer 2007], [Qadeer and Rehof 2005], [Abdulla et al. 2019], [Abdulla et al. 2017]. The bounding concept chosen for concurrent programs depends on aspects related to the interactions between the processes. In the case of SC programs, context bounding has been shown experimentally to have extensive behaviour coverage for bug detection [Musuvathi and Qadeer 2007], [Qadeer and Rehof 2005]. A context in the SC setting is a computation segment where only one process is active. The concept of context bounding has been extended for weak memory models. For instance, in TSO, the notion of context is extended to one where all updates to the main memory are done only from the buffer of the active thread [Atig et al. 2011]. In the case of POWER [Abdulla et al. 2017], context was extended to consider propagation actions performed by the active process. In the case of PS 2.0-ra without promises and reservations [Abdulla et al. 2019], context bounding was extended to view bounding, using the notion of view switching messages. The notion of bounding appropriate for a model depends on its underlying complexity. From a theoretical point of view, we have already seen that PS 2.0 is very complex, and bounding contexts is not sufficient. Our bounding notion for PS 2.0 is based on its various features which includes relaxed as well as RA memory accesses, promises and certification. Since PS 2.0 subsumes RA, we recall the bounding notion used in RA first, using view altering messages.

**View Altering Reads.** A read from the memory is view altering if it changes the view of the process reading it. The message which is reads from in turn is called a view altering message. The under approximate analysis for RA [Abdulla et al. 2019] considered view bounded runs, where the number of view altering reads is bounded.
The Bounded Consistent Reachability Problem. Consider a run \( r \) of a concurrent program under PS 2.0 that has a bounded context. Now we define the notion of bounding for \( r \), in two modes: a ‘normal’ mode and a ‘check’ (consistency check) mode. In the normal mode, a promise, a reservation or a view altering read by some process in the run.

**Essential Events.** An essential event in a run \( r \) of a concurrent program under PS 2.0 is either a promise, a reservation or a view altering read by some process in the run.

**Bounded Context.** A context is an uninterrupted sequence of actions by a single process. In a run having \( K \) contexts, the execution switches from one process to another \( K - 1 \) times. A \( K \)-bounded context run is one where the number of context switches are bounded by \( K \in \mathbb{N} \). The \( K \)-bounded context reachability problem in SC checks for the existence of a \( K \)-bounded context run reaching some chosen instruction. A SC program is called a \( K \)-bounded context program if all its runs are \( K \)-bounded context. Now we define the notion of bounding for PS 2.0.

**The Bounded Consistent Reachability Problem.** Consider a run \( r \) of a concurrent program under PS 2.0, \( MS_0 \xrightarrow{\rho_1} MS_1 \xrightarrow{\rho_2} ... \xrightarrow{\rho_n} MS_n \). A run \( r \) of a concurrent program \( Prog \) under PS 2.0 is called \( K \)-bounded if the number of essential events in \( r \) is \( \leq K \). The \( K \)-bounded reachability problem for PS 2.0 checks for the existence of a run \( r \) of \( Prog \) which is \( K \)-bounded. Assuming \( Prog \) has \( n \) processes, we propose an algorithm that reduces the \( K \)-bounded reachability problem to a \( K + n \)-bounded context reachability problem under SC.

**Translation Overview.** Let \( Prog \) be a concurrent program under PS 2.0 with set of processes \( P \) and locations Loc. Our algorithm relies on a source to source translation of \( Prog \) to a bounded context SC program \( ||Prog|| \), as shown in Figure 11 and operates on the same data domain. The translation adds a new process \( \text{MAIN} \) that initializes the global variables of \( ||Prog|| \). The translation of a process \( p \in P \) adds local variables, which are initialized by the function \( \text{INIPROC} \).

This is followed by the code block \( \langle \text{CSO} \rangle^{p_,\lambda_0} \) (Context Switch Out) that optionally enables the process to switch out of context. For each instruction \( i \) appearing in the code of \( p \), the map \( ||i||^P \) transforms it into a sequence of instructions as follows: the code block \( \langle \text{CSI} \rangle \) (Context Switch In) checks if the process is active in the current context; then it transforms each statement \( s \) of instruction \( i \) into a sequence of instructions following the map \( ||s||^P \), and finally executes the code block \( \langle \text{CSO} \rangle^{p_,\lambda} \). \( \langle \text{CSO} \rangle^{p_,\lambda} \) facilitates two things: when the process is at an instruction label \( \lambda_0 \), (1) allows \( p \) to make promises/reservations after \( \lambda \), s.t. the control is back at \( \lambda \) after certification; (2) it ensures that the machine state is consistent when \( p \) switches out of context. Translation of \text{assume}, \text{if} and \text{while} statements keep the same statement. Translation of read and write statements are described later. Translation of RMW statements are omitted for ease of presentation.

The set of promises a process makes has to be constrained with respect to the set of promises that it can certify, since processes can generate arbitrarily many promises/reservations, while, in reality only a few of them will be certifiable. To address this, in the translation, processes run in two modes: a ‘normal’ mode and a ‘check’ (consistency check) mode. In the normal mode, a
process does not make any promises or reservations. In the check mode, the process may make promises and reservations and subsequently certify them before switching out of context. In any context, a process first enters the normal mode, and then, before exiting the context it enters the check mode. The check mode is used by the process to (1) make new promises/reservations and (2) certify consistency of the machine state. We also add an optional parameter, called certification depth (certDepth), which constrains the number of steps a process may take in the check mode to certify its promises. Figure 12 shows the structure of a translated run under SC.

To reduce the PS 2.0 run into a bounded context SC run, we use the bound on the number of essential events. From the run $\rho$ in PS 2.0, we construct a $K$ bounded run $\rho'$ in PS 2.0 where the processes run in the order of generation of essential events. So, the process which generates the first essential event is run first, till that event happens, then the second process which generates the second essential event is run, and so on. This continues till $K+n$ contexts: the $K$ bounds the number of essential events, and the $n$ is to ensure all processes are run to completion. The bound on the number of essential events gives a bound on the number of timestamps that need to be maintained. As observed in [Abdulla et al. 2019], one view altering read requires two timestamps; additionally, each promise/reservation requires one timestamp. Since we have $K$ such essential events, $2K$ time stamps suffice. We choose $\text{Time} = \{0, 1, 2, \ldots, 2K\}$ as the set of timestamps.

Data Structures. We mention the significant ones. The message data structure represents a message generated as a write or a promise and has 4 fields (i) var, the address of the memory location written to; (ii) the timestamp $t$ in the view associated with the message; (iii) $v$, the value written; and (iv) flag, that keeps track of whether it is a message or a promise; and, in case of a promise, which process it belongs to. The View data structure stores, for each memory location $x$, (i) a timestamp $t \in \text{Time}$, (ii) a value $v$ written to $x$, (iii) a Boolean $l \in \{\text{true, false}\}$ representing whether $t$ is an exact timestamp (which can be used for essential events) or an abstract timestamp (which corresponds to non-essential events).

Global Variables. The Memory is an array of size $K$ holding elements of type message. This array is populated with the view switching messages, promises and reservations generated by the program. We maintain counters for (1) the number of elements in Memory; (2) the number of context switches that have occurred; and (3) the number of essential events that have occurred.

Local Variables. In addition to its local registers, each process has local variables including
- a local variable view, which stores a local instance of the view function (this is of type View),
- active: a boolean variable which is set when the process is running in the current context, and
- checkMode: a boolean denoting whether the process is in the certification phase. We implement the certification phase as a function call, and hence store the process state and return address, while entering it.

Subroutines. We use certain helper subroutines as follows:
- genMessage is a subroutine which generates an instance of the message data structure;
- saveState($p$) is a subroutine which saves the values of the global variables and the local states (instruction labels and local variables) of process $p$. This is used when switching into check mode.
- loadState($p$) is a subroutine which loads the values of global variables and local states of $p$ which was saved using saveState($p$). This is use when switching out of check mode.

5.1 Translation Maps

In what follows we illustrate how the translation simulates a run under PS 2.0. At the outset, recall that each process alternates, in its execution, between two modes: a normal mode (n in Figure 12) at the beginning of each context and the check mode at the end of the current context (cc in Figure 12), where it may make new promises and certify them before switching out of context.

**Context Switch Out (CSO$^h,\lambda$).** We describe the CSO module (Algorithm 1 provides its pseudocode). CSO$^h,\lambda$ is placed after each instruction $\lambda$ in the original program and serves as an entry and exit point for the consistency check phase of the process. When in normal mode ($n$) after some instruction $\lambda$, CSO non-deterministically guesses whether the process should exit the context at this point, and sets the checkMode flag to true and subsequently, saves its local state and the return address (to mark where to resume execution from, in the next context). The process then continues its execution in the consistency check mode (cc) from the current instruction label ($\lambda$) itself. Now the process may generate new promises (see Algorithm 2) and certify these as well as earlier made promises. In order to conclude the check mode phase, the process will enter the CSO block at some different instruction label $\lambda'$. Now since the checkMode flag is true, the process enters the else branch, verifies that there are no outstanding promises of $p$ to be certified. Since the promises are not yet fulfilled, when $p$ switches out of context, it has to mark all its promises uncertified.

When the context is back to $p$ again, this will be used to fulfil the promises or to certify them again before the context switches out of $p$ again. Then it exits the check mode phase, setting checkMode to false. Finally it loads the saved state, and returns to the instruction label $\lambda$ (where it entered check mode) and exits the context.

**Write Statements.** We now discuss the translation of a write instruction $\llbracket x := \{r, l, a\} \rrbracket_o$, where $o \in \{rl, l, ra\}$ of a process $p$, the intuitive pseudocode for which is given in Algorithm 2.

This is the general pseudocode for both kinds of memory accesses, with specific details pertaining to the particular access mode omitted.

Let us first consider execution in the normal mode (i.e., checkMode is false). First, the process updates its local state with the value that it will write. Then, the process non-deterministically chooses one of three possibilities for the write, it either (i) does not assign a fresh timestamp
Algorithm 3: Read

```plaintext
if nondet() then  /* local read */
    check local state is valid
    update local state with read
else  /* nonlocal (view-switching) read */
    check that local state allows read
    get message from Memory
    check variable, value, view are allowed
    update local state with message view
end
```

Let us now consider a write executing when `checkMode` is true, and highlight differences with the normal mode. In case (i), non essential events exclude promises and reservations. Then, while in certification phase, since we use a capped memory, the process can make a write if either (1) the write interval can be generated through splitting insertion or (2) the write can be certified with the help of a reservation. Basically the writes we make either split an existing interval (and add this to the left of a promise), or forms a part of a reservation.

Thus, the time stamp of a neighbour is used. In case (ii) when a fresh time stamp is used, the write is made as a promise, and then certified before switching out of context. The analogue of case (iii) is the certification of promises for the current context; promise fulfilment happens only in the normal mode. To help a process decide the value of a promise, we use the fact that CBMC allows us to assign a non-deterministic value of a variable. On top of that, we have implemented an optimization that checks the set of possible values to be written in the future.

**Read Statements.** The translation of a read instruction $\langle r \rangle_o, o \in \{r1x, ra\}$ of process $p$ is given in Algorithm 3. The process first guesses, whether it will read from a view altering message in the memory of from its local view. If it is the latter, the process must first verify whether it can read from the local view; for instance, reading from the local view may not be possible after execution of a `fence` instruction when the timestamp of a variable $x$ gets incremented from the local view $t$ to $t' > t$. In the case of a view altering read, we first check that we have not reached the context switching/essential event bound. Then the new message is fetched from Memory and we check the view (timestamps) in the acquired message satisfy the conditions imposed by the access type $\in \{ra, r1x\}$. Finally, the process updates its view with that of the new promise.
message and increments the counters for the context switches and the essential events. Theorem 5.1 proves the correctness of our translation.

**Theorem 5.1.** Given a program $Prog$ under PS 2.0, and $K \in \mathbb{N}$, the source to source translation constructs a program $\llbracket prog \rrbracket$ whose size is polynomial in $Prog$ and $K$ such that, for every $K$-bounded run of $Prog$ under PS 2.0 reaching a set of instruction labels, there is a $K + n$-bounded context run of $\llbracket prog \rrbracket$ under SC that reaches the same set of instruction labels.

### 6 IMPLEMENTATION AND EXPERIMENTAL RESULTS

In order to check the efficiency of the source-to-source translation, we implement a prototype tool, PS2SC which is the first tool to handle PS 2.0. PS2SC takes as input a C program and a bound $K$ and translates it to a program $Prog'$ to be run under SC. We use CBMC version 5.10 as backend to verify $Prog'$. CBMC takes as input $L$, the loop unrolling parameter for bounded model checking of $Prog'$. We supply the bound on Essential Events, $K$ as a parameter to PS2SC. PS2SC then considers the subset of executions respecting the bounds $K$ and $L$ provided as input. If it returns unsafe, then the program has an unsafe execution. Conversely, if it returns safe then none of the executions within the subset violate any assertion. $K$ may be iteratively incremented to increase the number of executions explored. We provide a functionality with which the user optionally selects a subset of processes for which promises and reservations will be enabled. While in the extreme cases we can run PS2SC in the promise-full (all processes can promise) and promise-free modes, partial promises (allowing subsets of processes to promise) turns out to be an effective technique.

We now report the results of experiments we have performed with PS2SC. We have two objectives: (1) studying the performance of PS2SC on benchmarks which are unsafe only if promises are enabled and (2) comparing PS2SC with other model checkers when operating in the promise-free mode (since they can not handle promises). In the first case, we show that PS2SC is able to uncover bugs in examples with low interaction (reads and writes) with the shared memory. When this interaction increases, however, PS2SC does not scale, owing to the huge non-determinism in PS 2.0. However, with partial promises, PS2SC is once again able to uncover bugs in reasonable amounts of time. In the second case, our observations highlight the ability to detect hard to find bugs with small $K$ for unsafe benchmarks, and scalability by altering $K$ as discussed earlier in case of safe benchmarks.

We compare PS2SC with three state-of-the-art stateless model checking tools, CDSChecker [Norris and Demsky 2013], GenMC [Kokologiannakis et al. 2019] and Rcmc [Kokologiannakis et al. 2017] that support the promise-free subset of the PS 2.0 semantics. In the tables that follow we provide the value of $K$ (for PS2SC only) and the value of $L$ (for all tools). We do not consider compilation time for any tool while reporting the results. For PS2SC, the time reported is the time taken by the CBMC backend for analysis. The timeout used is 1 hour for all benchmarks. All experiments are conducted on a machine with a 3.00 GHz Intel Core i5-3330 CPU and 8GB RAM running a Ubuntu 16 64-bit operating system. We denote timeout by ‘TO’, and memory limit exceeded by ‘MLE’.

#### 6.1 Experimenting with Promises

In this section we check the efficiency of the source-to-source translation in handling promises for PS 2.0 (which is the most difficult part due to the non-determinism).

We first test PS2SC on litmus-tests adapted from [Chakraborty and Vafeiadis 2019b; Kang et al. 2017; Lee et al. 2020; Manson et al. 2005]. These examples are small programs that serve as barebones thin-air tests for the C11 memory model. Consistency tests based on the Java Memory Model are proposed in [Manson et al. 2005]. These were also experimented on in [Paviotti et al. 2020] with the MRDer tool. Like MRDer, PS2SC is able to verify most of these tests within 1 minute which shows its ability to handle typical programming idioms of PS 2.0.
| testcase  | K | PS2SC |
|-----------|---|-------|
| ARM_weak  | 4 | 0.765s|
| Upd-Stuck | 4 | 1.252s|
| split     | 4 | 25.737s|
| LBd       | 3 | 1.481s|
| LBfd      | 3 | 1.512s|
| CYC       | 5 | 1.967s|
| Coh-CYC   | 5 | 42.67s|

Table 1. Litmus Tests

| testcase  | K | PS2SC |
|-----------|---|-------|
| fib_local_3 | 4 | 0.742s|
| fib_local_4 | 4 | 0.761s|
| fib_local_cas_3 | 4 | 1.132s|
| fib_local_cas_4 | 4 | 1.147s|

Table 2. Performance of PS2SC on cases with local computation

| testcase  | K | PS2SC |
|-----------|---|-------|
| fib_global_2 | 4 | 55.972s|
| fib_global_3 | 4 | 2m4s|
| fib_global_4 | 4 | 4m20s|
| exp_global_1 | 4 | 19m37s|
| exp_global_2 | 4 | 41m12s|

Table 3. Performance of PS2SC on cases with global computation

In Table 2 we consider unsafe examples in which a process is required to generate a promise (speculative write) with value as the $i$th fibonacci number (Fibonacci-based benchmarks for SV-COMP 2019 [Beyer 2019]). This promise is certified using computations local to the process. Thus though the parameter $i$ increases the interaction of the promising process with the memory remains constant. The CAS variant requires the process to make use of reservations. We note that PS2SC uncovers the bugs effectively in all these cases.

Now we consider the case where promises require some interaction between processes. We consider an example adapted from the Fibonacci-based benchmarks for SV-COMP 2019 [Beyer 2019], where two processes compute the $i$th fibonacci number in a distributed fashion. Unlike the previous case, here, the amount of interaction increases with $i$. Here however, our tool times out.

How do we recover tractable analysis in this case? We tackle this problem by a modular approach of allowing partial-promises, i.e. subsets of processes are allowed to generate promises/reservations. In the experiments, we allowed only a single process to do so. The results obtained are in Table 3, where PS2SC[1p] denotes that only one process is permitted to perform promises. We then repeat our experiments on two other unsafe benchmarks - ExponentialBug from Fig. 2 of [Huang 2015] and have similar observations. With this modular approach PS2SC uncovers the bug. To summarize, we note that the source to source approach performs well on programs requiring limited global memory interaction. When this interaction increases, PS2SC times out, owing to the
The Decidability of Verification under Promising 2.0

Table 4. Comparison on a set of parameterized benchmarks

| benchmark         | L  | K  | PS2SC  | CDSChecker | GenMC | RCMC  |
|-------------------|----|----|--------|------------|-------|-------|
| exponential_10_unsafe | 10 | 10 | 1.854s | 1.921s     | 0.367s | 3m41s |
| exponential_25_unsafe | 25 | 10 | 3.532s | 7.239s     | 3.736s | TO    |
| exponential_50_unsafe | 50 | 10 | 6.128s | 36.361s    | 39.920s | TO    |
| fibonacci_2_unsafe  | 2  | 20 | 2.746s | 2.332s     | 0.084s | 0.086s |
| fibonacci_3_unsafe  | 3  | 20 | 9.392s | 46m8s      | 0.462s | 0.544s |
| fibonacci_4_unsafe  | 4  | 20 | 34.019s | TO         | 12.437s | 18.953s |

Table 5. Comparison on concurrent data structures

| benchmark         | L  | K  | PS2SC  | CDSChecker | GenMC | RCMC  |
|-------------------|----|----|--------|------------|-------|-------|
| hehner2_unsafe    | 4  | 5  | 7.207s | 0.033s     | 0.094s | 0.087s |
| hehner3_unsafe    | 4  | 5  | 28.345s| 0.036s     | 2m53s | 1m13s |
| linuxlocks2_unsafe| 2  | 4  | 0.547s | 0.032s     | 0.073s | 0.078s |
| linuxlocks3_unsafe| 2  | 4  | 1.031s | 0.031s     | 0.083s | 0.081s |
| queue_2_safe      | 4  | 4  | 0.180s | 0.031s     | 0.082s | 0.085s |
| queue_3_safe      | 4  | 4  | 0.347s | 0.037s     | 0.090s | 0.092s |

huge non-determinism of PS 2.0. However, the modular approach of partial-promises enables us to recover effectiveness.

6.2 Comparing Performance with Other Tools

In this section we compare performance of PS2SC in promise-free mode with CDSChecker ([Norris and Demsky 2013]), GenMC ([Kokologiannakis et al. 2019]) and RCMC ([Kokologiannakis et al. 2017]) on safe and unsafe benchmarks. We provide a subset of the experimental results, the remaining can be found in the full version. The results of this section indicate that the source-to-source translation with essential event bounding is effective at uncovering hard to find bugs in non-trivial programs. We will observe that in most examples discussed below, we had $K \leq 10$. Additionally, the bound $K$ allows incremental verification of safe programs in cases where the other tools timeout.

Parameterized Benchmarks. In Table 4 we compare the performance of these tools on two parametrized benchmarks: ExponentialBug (from Fig. 2 of [Huang 2015]) and Fibonacci (from SV-COMP 2019). In ExponentialBug($N$) $N$ represents the number of times a process writes to a variable. We note that in ExponentialBug($N$) the number of executions grows as $N!$, while the processes have to follow a specific interleaving to uncover the hard to find bug. In Fibonacci($N$), two processes compute the value of the $n^{th}$ fibonacci number in a distributed fashion. Our tool performs better than the other tools on the ExponentialBug and competes well on Fibonacci for larger values of the parameter. These results show the ability of our tool to uncover bugs with a small value of $K$.

Concurrent data structures based benchmarks. We compare the tools in Table 5 on benchmarks based on concurrent data structures. The first of these is a concurrent locking algorithm originating from Hehner and Shyamasundar [1981]. The second, LinuxLocks($N$) is adapted from evaluations of CDSChecker [Norris and Demsky 2013]. We note that if not completely fenced, it is unsafe. We fence all but one lock access. Queue is a safe benchmark adapted from SV-COMP 2018, parameterized by the number of processes. We note the ability of the tool to uncover bugs with a small value of $K$. 
Variations of mutual exclusion protocols. We now consider safe and unsafe variants of mutual exclusion protocols from SV-COMP 2018. The fully fenced versions of the protocols are safe. We modify these protocols by introducing bugs and comparing the performance of PS2SC for bug detection with the other tools. These benchmarks are parameterized by the number of processes.

In Table 6, we unfence a single process of the Peterson and Szymanski protocols making them unsafe. For PS2SC, the value of $K$ taken is 6 and 2 respectively, asserting that bugs can be found (even for non-trivial examples) with small $K$. We note that the other tools eventually timeout for larger values of $n$.

In Table 7 we keep all processes fenced but introduce a bug into the critical section of a process (write a value to a shared variable and read a different value from it). We note that all other tools timeout, while PS2SC is able to detect the bug within one minute, showing that essential event-bounding is an effective technique for bug-finding. Additionally in Peterson2C, we vary the example by changing the process in which we add the bug. We note that CDSChecker, can uncover the bug in Peterson2C(5) in around two minutes, while for Peterson1C(5) it timed out. Thus, CDSChecker algorithm is sensitive to changes in the position of the bug due to its DPOR exploration strategy.

We consider in Table 8 completely fenced versions of the mutual exclusion protocols. In this experiment, we increase the loop unwinding bound and with it, the value of $K$. These examples exhibit the practicality of iterative increments in $K$. The other tools eventually timeout, while PS2SC is able to provide at least partial guarantees.
7 CONCLUSION

In this paper, we investigate decidability of the promising semantics, PS 2.0 from Lee et al. [2020]. The release-acquire (ra) fragment of PS 2.0 with RMW operations is known to be undecidable [Abdulla et al. 2019]. However, the decidability of the fragment of PS 2.0 with only relaxed (rlx) accesses (denoted PS 2.0-rlx) was open. We started with this fragment, and obtained undecidability of the reachability problem, when there is no bound on the number of promises. In the quest for decidability, we considered an underapproximation of PS 2.0-rlx where we bound the number of promises in any execution. The fragment of PS 2.0-rlx with bounded promises is denoted as bdPS 2.0-rlx. We showed that reachability is decidable for bdPS 2.0-rlx. Our decidability proof includes the introduction of a new memory model LoHoW, and proving the equivalence of PS 2.0-rlx and LoHoW. The decidability of bdPS 2.0-rlx is shown using the theory of well structured transition systems. This also gives non-primitive recursive complexity of bdPS 2.0-rlx, with a proof similar to RMW-free fragment of release-acquire [Abdulla et al. 2019].

Having explored the decidability landscape of PS 2.0 thoroughly, we moved towards practical verification techniques for PS 2.0. Motivated by the success of context bounded reachability in SC [Qadeer and Rehof 2005], and subsequent notions in weak memory models, we introduced a notion of essential events bounded reachability for PS 2.0, which bounds the number of promises and view altering messages in any execution. We provide a source to source translation from a concurrent program under PS 2.0 with this bounded notion to a bounded context SC program, and implemented this in a tool PS2SC. PS2SC is the first tool capable of handling the promising framework, PS 2.0 from Lee et al. [2020] and the PS model from Kang et al. [2017]. PS2SC allows modularity with respect to allowing/disallowing promises on a thread-by-thread basis. We exhibit the efficacy of this modular technique in the face of non-determinism induced by PS 2.0. We also compare the performance of PS2SC with existing tools which do not support promises by operating it in the promise-free mode (in which no threads are allowed to promise). In this case, we exhibit the effectiveness of the bounding technique in uncovering hard-to-find bugs.

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A DETAILS FOR SECTION 4
In this section, we give details of lemmas from Section 4.

A.1 Equivalence of PS 2.0-rlx and LoHoW
To prove Theorem 4.3, we show the following: Given a program \( \text{Prog} \), starting from the initial machine state \( M_{\text{S}_{\text{init}}} = ((J_{\text{init}}, R_{\text{init}}), V_{\text{init}}, PS_{\text{init}}, M_{\text{init}}, G_{\text{init}}) \) in PS 2.0-rlx, we can reach in PS 2.0-rlx the machine state \( M_{\text{S}_{n}} = ((J_{n}, R_{n}), V_{n}, PS_{n}, M_{n}, G_{n}) \) with \( PS_{n}(p) = \emptyset \) for all \( p \in P \) iff, starting from an initial LoHoW two phases state \( S_{\text{init}} = (\text{std}, p, st_{\text{init}}, st_{\text{init}}) \), we reach the state \( (\text{std}, -, ((J_{n}, R_{n}), \text{HW}_{n}), -) \), such that \( \text{HW}_{n}(x) \) does not contain any memory type of the form \((\text{prm}, -, p, -)\) or \((\text{prm}, -, p, -)\) for all \( x \in \text{Loc} \). The equivalence of the runs follows from the fact that the sequence of instructions followed in each phase \( \text{std} \) and \( \text{cert} \) are same in both PS 2.0-rlx and LoHoW; LoHoW allows lossy transitions which does not affect reachability. Moreover, the LoHoW run satisfies the following invariants.

Invariants for HW. The following invariants hold good for \( \text{HW}(x) \) for all \( x \in \text{Loc} \). We then say that \( \text{HW}(x) \) is faithful to the sub memory \( M(x) \) and the view mapping.

(Inv1) For all \( x \in \text{Loc}, \, \text{HW}(x) \) is well-formed : for each process \( p \in P \), there is a unique position \( i \) in \( \text{HW}(x) \) having its pointer set;

(Inv2) For all \( i > \text{ptr}(p, \text{HW}(x)) \), we have \( \text{HW}(x)[i] \notin \{(\text{msg}, -, p, -), (\text{msg}, -, p, -), (\text{msg}, -, p, -)\} \). This says that memory types at positions greater than the pointer of \( p \) cannot correspond to messages added by \( p \) to \( M(x) \).

LEMMA A.1. The higher order words \( \text{HW}(x) \) for all \( x \in \text{Loc} \) appearing in the states of a LoHoW run satisfy invariants Inv1 and Inv2.

Lemma A.2 can be proved by inducting on the length of a LoHoW run, starting from the initial states, using the following.

- For each memory type \((\text{msg}, v, p, S, -)\) or \((\text{msg}, v, p, S, -)\) in \( \text{HW}(x) \), there is a message in \( M(x) \) which was added by process \( p \), having value \( v \). Similarly, for each memory type \((\text{prm}, v, p, S, -)\) or \((\text{prm}, v, p, S, -)\) in \( \text{HW}(x) \), there is a promise in \( M(x) \) which was added by process \( p \), having value \( v \).

- The order between memory types in \( \text{HW}(x) \) and the corresponding messages in \( M(x) \) are the same. That is, for \( i < j \), the messages or promises \( m, m' \in M(x) \) corresponding to \( \text{HW}(x)[i] \) and \( \text{HW}(x)[j] \) are such that \( m.\text{to} < m'.\text{to} \).

- The elements in the pointer set of a memory type \( m \) in \( \text{HW}(x) \) are exactly the set of processes whose local view is the \text{to} stamp of the element of \( M(x) \) corresponding to \( m \).

The base case is easy : the initial two-phases LoHoW state has the same local process states as the initial PS 2.0 machine state; moreover, the invariants trivially hold, since all process pointers are at the same position.

For the inductive hypothesis, assume that both invariants hold in a LoHoW run after \( i \) steps. To show that they continue to hold good after \( i+1 \) steps, we have to show that for all LoHoW transitions that can be taken after \( i \) steps, they are preserved. Assume that the two phases LoHoW state at the end of \( i \) steps is \((\text{std}, p, st, st')\). The proof for the case when we have a state \((\text{cert}, p, st, st')\) after \( i \) steps of the LoHoW run is similar.

- Assume that we have the transition \( \overset{rd(x,v)}{\underset{p}{\rightarrow}} \). Then \( \text{ptr}(p, \text{HW}(x)) \) is updated in the resultant state, and so are \((J, R)\). Clearly, the higher order word in the resultant state satisfies both invariants since the starting state does.
• Assume that we have the transition $\frac{wt(x, o)}{\rho}$. Then we remove $\rho$ from the pointer set at position $i = \text{ptr}(\rho, \text{HW}(x))$. A new simple word is added at a position $> i$, or a memory type $(\text{msg}, v, p, \{p\})$ is added at a position $j > i$, right next to a $\#$, by moving the memory type at $j$ to position $j - 2$. In either case, the resultant higher order word satisfies both invariants, since the starting state does.

• The update rule $\frac{\text{msg}(x, o, w)}{\rho}$ combines the above two cases, by first performing a read and then atomically the write. From the above two cases, the invariants can be seen to hold good in the higher order words in the state obtained after the transition.

• Consider the Promise rule. In this case, we do not remove $\rho$ from its pointer set, and only add the memory type $(\text{prm}, v, p, \{\})$ ahead of $\text{ptr}(p, \text{HW}(x))$. Note that Inv2 only requires that there are no memory types of the form $(\text{msg}, v, p, S, -)$ ahead of $\text{ptr}(p, \text{HW}(x))$. Clearly, both invariants continue to hold.

• Consider a fulfill rule obtained as a write. In this case, $p$ is deleted from the position $\text{ptr}(p, \text{HW}(x))$; and the memory type $(\text{prm}, v, p, S)$ (or $(\text{prm}, v, p, S, -)$) is replaced with $(\text{msg}, v, p, S \cup \{\})$ (or $(\text{msg}, v, p, S \cup \{\})$). It is easy to see both invariants holding good.

• Consider the reservation rule. This does not affect the invariants since we only tag the last component of a memory type with the process making the reservation.

• Consider the SC fence rule. If $\text{ptr}(p, \text{HW}(x)) > \text{ptr}(g, \text{HW}(x))$, then, in the resultant word, $p$ is moved to $\text{ptr}(g, \text{HW}(x))$. The case when $\text{ptr}(p, \text{HW}(x)) < \text{ptr}(g, \text{HW}(x))$, is handled by moving $g$ to $\text{ptr}(p, \text{HW}(x))$. Since this is the only change in the resultant higher order words, clearly, both invariants hold good.

Notice that the arguments above hold good for both modes $\alpha \in \{\text{std}, \text{cert}\}$.

To prove Theorem 4.3, we show the following: Given a program Prog, starting from the initial machine state $\text{MS}_{\text{init}} = ((J_{\text{init}}, R_{\text{init}}), V_{\text{init}}, PS_{\text{init}}, M_{\text{init}}, G_{\text{init}})$ in PS 2.0-rlx, we can reach the machine state $\text{MS}_n = ((J_n, R_n), V_n, PS_n, M_n, G_n)$ with $PS_n(p) = \emptyset$ for all $p \in P$ iff, starting from an initial LoHoW two phases state $S_{\text{init}} = (\text{std}, p, \text{st}_{\text{init}}, \text{st}_{\text{init}})$, we reach the state $(\text{std}, -, ((J_n, R_n), \text{HW}_n), -)$, such that $\text{HW}_n(x)$ does not contain any memory type of the form $(\text{prm}, -, p, -)$ or $(\text{prm}, -, p, - -)$ for all $x \in \text{Loc}$. The equivalence of the runs follows from the fact that the sequence of instructions followed in each phase std and cert are same in both PS 2.0-rlx and LoHoW; LoHoW allows lossy transitions which does not affect reachability. Moreover, the LoHoW run satisfies the following invariants.

Invariants for HW. The following invariants hold good for $\text{HW}(x)$ for all $x \in \text{Loc}$. We then say that $\text{HW}(x)$ is faithful to the sub memory $M(x)$ and the view mapping.

(Inv1) For all $x \in \text{Loc}$, $\text{HW}(x)$ is well-formed: for each process $p \in P$, there is a unique position $i$ in $\text{HW}(x)$ having $p$ in its pointer set;

(Inv2) For all $i > \text{ptr}(p, \text{HW}(x))$, we have $\text{HW}(x)[i] \notin ((\text{msg}, -, p, -), (\text{msg}, -, p, - -))$. This says that memory types at positions greater than the pointer of $p$ cannot correspond to messages added by $p$ to $M(x)$.

All $\text{HW}(x)$ respect Invariants Inv1 and Inv2

Lemma A.2. The higher order words $\text{HW}(x)$ for all $x \in \text{Loc}$ appearing in the states of a LoHoW run satisfy invariants Inv1 and Inv2.

Lemma A.2 can be proved by inducting on the length of a LoHoW run, starting from the initial states, using the following.
• For each memory type \((\text{msg}, v, p, S, -)\) or \((\text{msg}, v, p, S)\) in \(\text{HW}(x)\), there is a message in \(M(x)\) which was added by process \(p\), having value \(v\). Similarly, for each memory type \((\text{prm}, v, p, S, -)\) or \((\text{prm}, v, p, S)\) in \(\text{HW}(x)\), there is a promise in \(M(x)\) which was added by process \(p\), having value \(v\).

• The order between memory types in \(\text{HW}(x)\) and the corresponding messages in \(M(x)\) are the same. That is, for \(i < j\), the messages or promises \(m, m' \in M(x)\) corresponding to \(\text{HW}(x)[i]\) and \(\text{HW}(x)[j]\) are such that \(m.\text{to} < m'.\text{to}\).

• The elements in the pointer set of a memory type \(m\) in \(\text{HW}(x)\) are exactly the set of processes whose local view is the to stamp of the element of \(M(x)\) corresponding to \(m\).

The base case is easy: the initial two-phases LoHoW state has the same local process states as the initial PS 2.0 machine state; moreover, the invariants trivially hold, since all process pointers are at the same position.

For the inductive hypothesis, assume that both invariants hold in a LoHoW run after \(i\) steps. To show that they continue to hold good after \(i+1\) steps, we have to show that for all LoHoW transitions that can be taken after \(i\) steps, they are preserved. Assume that the two phases LoHoW state at the end of \(i\) steps is \((\text{std}, p, \text{st}, \text{st}')\). The proof for the case when we have a state \((\text{cert}, p, \text{st}, \text{st}')\) after \(i\) steps of the LoHoW run is similar.

• Assume that we have the transition \(\xrightarrow{\text{rd}(x,v)}_p\) \(\text{ptr}(p, \text{HW}(x))\) is updated in the resultant state, and so are \((J, R)\). Clearly, the higher order word in the resultant state satisfies both invariants since the starting state does.

• Assume that we have the transition \(\xrightarrow{\text{wt}(x,v)}_p\). Then we remove \(p\) from the pointer set at position \(i = \text{ptr}(p, \text{HW}(x))\). A new simple word is added at a position \(> i\), or a memory type \((\text{msg}, v, p, \{p\})\) is added at a position \(j > i\), right next to a \#, by moving the memory type at \(j\) to position \(j - 2\). In either case, the resultant higher order word satisfies both invariants, since the starting state does.

• The update rule \(\xrightarrow{\text{U}(x,v,p)}_p\) combines the above two cases, by first performing a read and then atomically the write. From the above two cases, the invariants can be seen to hold good in the higher order words in the state obtained after the transition.

• Consider the Promise rule. In this case, we do not remove \(p\) from its pointer set, and only add the memory type \((\text{prm}, v, p, \{\})\) ahead of \(\text{ptr}(p, \text{HW}(x))\). Note that Inv2 only requires that there are no memory types of the form \((\text{msg}, v, p, S)\) or \((\text{msg}, v, p, S, -)\) ahead of \(\text{ptr}(p, \text{HW}(x))\). Clearly, both invariants continue to hold.

• Consider a fullfil rule obtained as a write. In this case, \(p\) is deleted from the position \(\text{ptr}(p, \text{HW}(x))\); and the memory type \((\text{prm}, v, p, S)\) (or \((\text{prm}, v, p, S, -)\)) is replaced with \((\text{msg}, v, p, S \cup \{p\})\) (or \((\text{msg}, v, p, S \cup \{p\})\)). It is easy to see both invariants holding good.

• Consider the reservation rule. This does not affect the invariants since we only tag the last component of a memory type with the process making the reservation.

• Consider the SC fence rule. If \(\text{ptr}(p, \text{HW}(x)) > \text{ptr}(g, \text{HW}(x))\), then, in the resultant word, \(p\) is moved to \(\text{ptr}(g, \text{HW}(x))\). The case when \(\text{ptr}(p, \text{HW}(x)) < \text{ptr}(g, \text{HW}(x))\), is handled by moving \(g\) to \(\text{ptr}(p, \text{HW}(x))\). Since this is the only change in the resultant higher order words, clearly, both invariants hold good.

Notice that the arguments above hold good in both modes \(a \in \{\text{std, cert}\}\).
Proof of Theorem 4.3

To show the equivalence of PS 2.0-rlx and LoHoW we show that the transitions in each phase of PS 2.0-rlx (standard, certification) is handled in LoHoW by an appropriate state (std, −, −, −) or (cert, −, −, −), and conversely. The first direction we consider is from PS 2.0-rlx to LoHoW.

To see the proof, we consider the four kinds of transitions between phases.

- Switching from certification phase to the standard phase is possible in PS 2.0-rlx only when the promise set of the process in the certification phase becomes empty. Any process can non deterministically begin the standard phase when the certification of one process ends successfully. These conditions are the simulated in LoHoW by allowing a transition from a two phases state (cert, p, ((J, R), HW), ((J′, R′), HW′)) to (std, q, ((J, R), HW), ((J′, R′), HW′)) only when there are no memory types (prm, −, p, −) in HW′.

- The switch from standard phase to certification phase happens in PS 2.0-rlx from a capped memory. This is simulated in LoHoW as follows. When entering the certification phase, LoHoW duplicates the higher order words. When the last memory type in any HW(x) is not tagged by the reservation of a process q ≠ p, the duplicated higher order word accounts for the capped memory, since we do not allow insertions in between during certification. When the last memory type in HW(x) is tagged by a reservation of process q ≠ p, then we add a new simple word #(msg, −, q, {}) at the end of the duplicated higher order word. This respects the semantics of reservation by a process q ≠ p. Thus, the capped memory during certification of PS 2.0-rlx is simulated in LoHoW by disallowing insertions inside a higher order word, and making explicit the reservations of a process.

- Once we are in a phase an continue in that phase, the proof in both directions is done by showing that each instruction simulated in PS 2.0-rlx can be simulated by the corresponding rule in LoHoW preserving the invariants, and conversely.

The first direction from PS 2.0-rlx to LoHoW is done as follows. For each transition by a process p on an instruction in PS 2.0-rlx, we show that we can simulate the same instruction in LoHoW.

1. Consider the read rd(x, v) rule in PS 2.0-rlx. In LoHoW, the read rule updates ptr(p, HW(x)) in such a way that HW(x) is faithful to M(x) and the view V. In case the read operation in PS 2.0-rlx uses a message whose timestamp is not the local view of any process, the corresponding memory type may or may not be present in HW(x) due to lossiness. Considering the case when this memory type is not lost, it is used exactly in the same manner as the respective message in PS 2.0-rlx. Rule 1 from Figure 10 handles this.

2. Consider the wt(x, v) rule in PS 2.0-rlx. In LoHoW, the write rule either appends memory types or adds simple words to HW(x) in the standard phase, and appends the memory type at the end of HWx in a certification phase due to the capping of memory. HW(x) is faithful to M(x) and V in these simulations. Mapping memory types in HW(x) to M(x), the relative ordering of the new memory type which gets added with respect to existing memory types in HW(x) is exactly same as the order the newly added message has, with respect to others in M(x) in either phase. Rules 3,4 in Figure 10 handles this.

A wt(x, v) rule can be done in PS 2.0-rlx during a certification phase by splitting a promise, or in standard phase for the fulfillment of a promise. These cases are handled respectively in LoHoW by (1) inserting a new message immediately preceding a promise in HWx, and (2) replacing a promise memory type (prm, −, −, −) with a message memory type ((, −, (, −)), −) and updating the pointer of p in each case. Rule 2 in Figure 10 handles these cases.
(3) Consider the \( U(x, v_r, v_w) \) rule in PS 2.0-rlx. In LoHoW, the RMW rule appends memory types to a simple word. The memory type corresponding to the message \( m \) in \( M(x) \) on which RMW is done, if available in \( HW(x) \), will be the rightmost in a simple word (right to a \#) in the standard phase, ahead of \( ptr(p, HW_{\alpha}) \), while in the certification phase, this will be the rightmost symbol in \( HW_x \) due to the implementation capped memory. The memory type which is appended to \# after moving \( m \) to the left of \#, corresponds to the new addition, right adjacent to \( m \) in \( M(x) \). The append operation captures the adjacency of the new message added to \( M(x) \) with respect to the one on which RMW is performed. This results in \( HW(x) \) being faithful to \( M(x) \) and view V. Rules 8, 9 in Figure 10 handle these cases. An \( U(x, v_r, v_w) \) rule can be done in PS 2.0-rlx during a certification phase by splitting a promise, or in standard phase for the fulfillment of a promise. These cases are handled respectively in LoHoW by (1) inserting a new message immediately preceding a promise in \( HW_x \), and (2) replacing a promise memory type \((prm, -, -, -)\) with a message memory type \(((-, -, (, -)), -)\) and updating the pointer of \( p \) in each case. Rule 10 in Figure 10 handles these cases.

(4) Next consider the promise rule in PS 2.0-rlx by a process \( p \). Promises take place only in the standard phase. The simulation in LoHoW is similar to the write rule. A new memory type \((prm, v, p, \{\})\) is added to \( HW(x) \) at a position \( > ptr(p, HW_{\alpha}) \) with an empty pointer set. This corresponds to the fact that the process \( p \) which makes the promise has its local view smaller than the to time stamp of the promise. Promise memory types are not lost from \( HW(x) \). Rule 12 in Figure 10 handles this.

Notice that when the promise is fulfilled, \( p \) is added to the pointer set of \((prm, v, p, S)\) and the promise memory type is replaced with the msg memory type. This corresponds to removing a promise from the promise set of \( P \). As already explained above, rules 2, 10 in Figure 10 handle this. Thus, \( HW(x) \) is faithful also to the promise set. If there is a promise which cannot be fulfilled in PS 2.0-rlx, the corresponding promise memory type will stay in \( HW(x) \), disallowing to reach a state \((std, -, -, -)\) in LoHoW.

(5) Let us now look at reservations in PS 2.0-rlx. These are done in the standard phase. The reserve rule done by a process \( p \) reserves a timestamp interval adjacent to an existing message \( m \) in \( M(x) \). To simulate this in LoHoW, if the memory type corresponding to \( m \) is available in \( HW(x) \), then it will be the rightmost in a simple word of \( HW(x) \). The reservation is done by tagging this memory type as a reservation by \( p \), thereby blocking this memory type from participating in any RMW. Rule 6 in Figure 10 handles this.

Similar to splitting promise intervals in a certification phase in PS 2.0-rlx, reservation intervals are also allowed to be split in PS 2.0-rlx during certification. This can happen as part of a write or an update in PS 2.0-rlx. To simulate this in LoHoW, we allow a process \( p \) to make use of its reservation.

- **Splitting a reservation.** \( HW \xrightarrow{SR} j m \) is defined only if \( HW[j] \) is of the form \((r', v', q, S, p)\). Let \( HW' \) be the higher order word defined as \( del(HW, p) \). Then, the extended higher order \( HW \xrightarrow{SR} j m \) is defined as \( HW'[j + 1, |HW|] \cdot (#(r, v, p, \{p\}, p) \cdot HW'[j + 1, |HW|]) \).

Observe that the new message \((r, v, p, \{p\}, p)\) is added to the right of the position \( j \) which corresponds to the slot that has been reserved by \( p \). This special splitting rule will be used during the certification phase. This will allow the process \( p \) to use the reserved slots. Recall
that it is not allowed to add memory types in the middle of the higher order words (other than the reserved ones) during the certification phase.

This is achieved by removing $p$ from its pointer set and replacing $(r', v', q, S, p)$ in $\text{HW}_X$ with $(r', v', q, S) \# (r, v, p, \{p\}, p)$. Rules 5, 11 in Figure 10 handle these.

(6) Cancelling a reservation in PS 2.0-rlx frees up the reserved timestamp interval in $M(x)$. To simulate this in LoHoW, if the corresponding tagged memory type is available in $\text{HW}(x)$, then it is unblocked from doing RMW by removing the reserve tag of $p$ from it. Rule 7 in Figure 10 handles this.

(7) Finally, SC fence rules in PS 2.0-rlx updates the views of the performing process to the most recent one. To simulate this in LoHoW, a dummy process $g$ simulating the global view is added. We update the pointer sets of $p$ (or $g$) depending on which one is ahead. Rule 13 in Figure 10 handles this.

Thus, for every run that reaches a consistent state in PS 2.0-rlx with local process states $(J, R)$, there is a run in LoHoW that reaches a two phases state $(\text{std}, (J, R), \text{st})$, following the same sequence of instructions. Note that rules 1-13 in Figure 10 are mutually non interfering since they apply to distinct rules and phases. Thus, for each rule in PS 2.0-rlx we have a unique rule in LoHoW from Figure 10 which simulates that while the PS 2.0-rlx is any of the phases, standard or certification.

The converse argument from LoHoW to PS 2.0-rlx is similar. The crucial argument is the memory types in each $\text{HW}(x)$ form a subset of $M(x)$, which has all the “necessary” messages (promises, non empty memory types in non redundant simple words). Lossiness of empty memory types/redundant simple words in $\text{HW}(x)$ can be interpreted as messages which are skipped over, or which have already been used in $M(x)$. It is easy to see that any sequence of transitions of instructions in LoHoW can be simulated by exactly the same instruction sequence in PS 2.0-rlx.

A.2 Proof of Lemma 4.8

Recall that $\text{minpre}(c)$ is defined as $\text{min}(\text{Pre}([\{c\}] \cup \{c\}])$. In the following, we show the set $\text{minpre}(c)$ is effectively computable for any two-phases K-LoHoW state $c$. To do that, we will use a transducer based approach. Lemma 4.8 is an immediate consequence of Lemma A.3, Lemma A.4, Lemma A.5, and Lemma A.6.

Lemma A.4 shows the regularity of $\{c\}^\dagger$, Lemma A.6 and A.5 show the regularity of $\text{Pre}([\{c\}]^\dagger)$, while Lemma A.3 shows the effective computability of $\text{min}(\text{Pre}([\{c\}] \cup \{c\}])$.

Finite-state automata. A finite state automaton $A$ is a tuple $A = (\Sigma_1, P, I, E, F)$, where $\Sigma_1$ is the finite input alphabet, $P$ is a finite set of states, $I, F \subseteq P$ are subsets of initial and final states, and $E \subseteq P \times \Sigma_1 \times P$ is a finite set of transition rules. A word $u = a_1 \ldots a_n$ is accepted by $A$ if there is a run $p_0 \xrightarrow{a_1} p_1 \xrightarrow{a_2} \ldots p_{n-1} \xrightarrow{a_n} p_n$ such that $p_0 \in I$, $p_n \in F$ and $(p_{i-1}, a_i, p_i) \in E$. We use $L(A)$ to denote the set of words accepted by $A$.

Regular set of two-phases K-LoHoW-states We use an encoding of two-phases K-LoHoW states as words over a finite alphabet, and use this encoding to define a regular set of two-phases K-LoHoW states. Let $\text{st}$ denote $((J, R), \text{HW})$. Consider a two-phases K-LoHoW state $c = (\text{std}, p, \text{st}, \text{st}')$ or $(\text{cert}, p, \text{st}, \text{st}')$. Recall that $(J, R)$ gives the local instruction labels of all processes and the local register values. Assuming we have locations $x_1, \ldots, x_m, \text{HW} = (\text{HW}_{x_1})_{1 \leq i \leq m}$. The state $c$ is encoded by the word $w = \text{std}spJSR0\text{HW}_{x_1}s_1 \ldots \text{HW}_{x_m}s_m \overset{\varepsilon}{\vdash} J's_0\text{HW}'_{x_1}s'\text{HW}'_{x_2} \ldots \text{HW}'_{x_m}s'_m$ or $\text{cert}spJSR0\text{HW}_{x_1}s_1 \ldots \text{HW}_{x_m}s_m \overset{\varepsilon}{\vdash} J's_0\text{HW}'_{x_1}s'\text{HW}'_{x_2} \ldots \text{HW}'_{x_m}s'_m$ where $J$ defines the local state of each process, and the $\overset{\varepsilon}{\vdash}, s_0, s_i$’s act as delimiters between the contents of the higher order
Assume \( \langle \Sigma, P, I, E, F \rangle \) be the finite state automaton that accepts \( \text{Enc}(R) \). The main idea to effectively compute \( \min(R) \) is to bound the size of the words accepted by \( A \) that encode minimal two-phases \( K \)-LoHoW states. Observe that the cycles in \( A \) can be only labeled by the empty memory type. Otherwise there will be a violation of invariant (Inv1). Now consider a word \( w \) accepted by \( A \). We will first construct another word \( w' \) from \( w \) such \( \text{decode}(w') \subseteq \text{decode}(w) \) and the number of \#e where \( e \) is an empty memory type from the subset \( \langle \text{msg}, P, \{\} \rangle \) of \( \Sigma \) or \( \langle \text{msg}, - P, \{\} \rangle \) of \( \Gamma \) occurring in \( w' \) is polynomially bounded by the size of \( A \). In the following, for convenience, we use macro transitions on \#a rather than two separate transitions on \# followed by a transition for \( a \).

Let us assume that \( w \) is accepted by \( A \) using the following run \( p_0 \xrightarrow{a_1} p_1 \xrightarrow{a_2} \ldots \xrightarrow{a_{k-1}} p_k \). Let \( i_1 < i_2 < \cdots < i_b \) be the maximal sequence of indices such that \( a_{i_j} \) is an empty memory type \( \in \langle \text{msg}, - P, \{\} \rangle \) or \( \langle \text{msg}, - P, \{\} \rangle \). Now if \( b > |P| \cdot |\Sigma| \), then there are two indices \( i_j \) and \( i_k \) such that \( i_j < i_k \), \( a_{i_j} = a_{i_k} \) and \( p_{i_j-1} = p_{i_k-1} \). Furthermore, all the symbols occurring between \( i_j \) and \( i_k \) are empty memory types (from (Inv1)). This means that \( p_0 \xrightarrow{a_1} p_1 \xrightarrow{a_2} \ldots \xrightarrow{a_{k-1}} p_{i_j} \xrightarrow{a_{i_j}} p_{i_k} \) is an accepting run of \( A \) (accepting the word \( w_1 \)). Furthermore, \( \text{decode}(w_1) \subseteq \text{decode}(w) \). We can now proceed iteratively on \( w_1 \) in order to obtain the word \( w' \) that is accepted by \( A \), \( \text{decode}(w') \subseteq \text{decode}(w) \), s.t. the number of \#e, with \( e \) an empty memory type from \( \Sigma \cup \Gamma \) occurring in \( w' \) is bounded by \( |P| \cdot |\Sigma| \). Observe that the number of \#b where \( b \) is a non empty memory type from \( \Sigma \cup \Gamma \) occurring in \( w' \) is also bounded by \( |P| \cdot |\Sigma| \). These are either \( K \) promise memory types \( \langle \text{prom}, - - \rangle \) or \( \langle \text{prom}, - - \rangle \) or those of the form \( \langle \text{msg}, - - \rangle \) or \( \langle \text{msg}, - - \rangle \) where \( S \neq \emptyset \). For the latter, we have a bound of \( |P| + 1 \). This comes from Inv1 since each process in \( \Sigma \cup \{g\} \) appears in a unique pointer set. Thus, the number of \#e where \( e \in \Sigma \cup \Gamma \) occurring in \( w' \) is polynomially bounded by the size of \( A \).

Now from \( w' \) we will construct another word \( w'' \) accepted by \( A \) and such that \( \text{decode}(w'') \subseteq \text{decode}(w') \) and \( |w''| \) is polynomially bounded by the size of \( A \). Let \( \rho := g_0 \xrightarrow{b_1} g_1 \xrightarrow{b_2} \ldots g_{t-1} \xrightarrow{b_t} g_t \) be the run of \( A \) accepting \( w' \). Let \( i_1 < i_2 < \cdots < i_r \) be the maximal sequence of indices such that \( b_{i_j} \in \Sigma \cup \Gamma \). Observe that \( r \) is polynomially bounded by the size of \( A \) as we have shown previously. Assume \( i_0 = 1 \) and \( i_{r+1} = t \). Now we can iteratively remove any cycle between two indices \( i_f \) and \( i_{f+1} \) in \( \rho \) that is only labeled by empty memory types from \( \Sigma \) to obtain \( w'' \) satisfying the previous conditions.

**Lemma A.4.** Given a regular set \( R \) of \( K \)-LoHoW states, the set \( R \uparrow \) is also regular.

**Proof.** Let \( A = (\Sigma, P, I, E, F) \) be the finite state automaton that accepts \( \text{Enc}(R) \). To construct a finite state automaton \( A' \) that accept \( \text{Enc}(R \uparrow) \), we proceed as follows: The automaton \( A' \) is constructed by replacing each macro transition \( (p, ba, p') \in E \) labeled by the letter \( a \in \Sigma, b \neq \# \) by the following macro-transition \( (p, e^* \cdot ba \cdot e^*, p') \) in \( A' \), where \( e \) is over the empty memory types of \( \Sigma \). Furthermore, any macro transition \( (p, \#a, p') \in E \) labeled by the letter \( a \in \Sigma \cup \Gamma \) is replaced in \( A' \) by the macro-transition \( (p, \#a \cdot (w \#b)^*, p') \), where \( w \in \Sigma^* \) is over the empty memory types of \( \Sigma \) and \( b \in \Sigma \cup \Gamma \) is an empty memory type in \( \Sigma \cup \Gamma \). We can also have a loop on empty memory types.
of $\Sigma$ on the initial state. Observe that any macro-transition can be easily translated to a sequence of simple transitions by using extra-intermediary states. \hfill $\square$

**Rational Transducers.** A rational transducer $T$ is a non-deterministic finite state automaton which outputs words on each transition. Formally, a *rational transducer* is a tuple $T = (\Sigma_1, \Sigma_2, Q, I, E, \eta, F)$, where $\Sigma_1, \Sigma_2$ are finite input and output alphabets, $Q$ is a finite set of states, $I, F \subseteq Q$ are subsets of initial and final states, $E \subseteq Q \times \Sigma_1 \times Q$ is a finite set of transition rules, and $\eta: E \rightarrow 2^{\Sigma_2}$ is a function specifying a regular language of partial outputs for each transition rule (i.e., $\eta(e)$ is a regular language for all $e \in E$). The relation defined by $T$ contains pairs $(u, v)$ of input and output words, where $u = a_1 \ldots a_n$ and $v = v_1 \ldots v_m$, for which there is a run $q_0 \xrightarrow{a_1|v_1} q_1 \xrightarrow{a_2|v_2} \ldots \xrightarrow{a_n|v_m} q_n$ such that $q_0 \in I$, $q_n \in F$, $(q_{i-1}, a_i, q_i) \in E$, $v_i \in \eta(q_{i-1}, a_i, q_i)$. The set of pairs $(u, v)$ defined by $T$ is denoted $L(T)$.

**Lemma A.5.** Given a regular language $R$ (described by a finite-state automaton), we can easily compute a finite state automaton $A$ such that $L(A) = \{u \mid (u, v) \in L(T) \land v \in R\}$.

**Proof.** Trivial. \hfill $\square$

**Lemma A.6.** It is possible to construct a transducer $T$ that accepts any pair $(\text{Enc}(s), \text{Enc}(s'))$, with $s$ and $s'$ are two two-phases $K$-LoHoW states, such that $s'$ is reachable from $s$ in one step.

**Proof.** Observe that the class of rational transducers are closed under union and therefore it is sufficient to construct the transducer $T$ for each transition rule. Furthermore, we always assume that the input and output tape of the transducer $T$ satisfy the two invariants (Inv1) and (Inv2) (these can be easily specified as a regular language). The proof is about simulating the rules in the transition system in LoHoW as defined in Section 4.2. We reproduce the rules for easy reference.

**The global transition rules in LoHoW**

Given $S = (\pi, p, st_{\text{std}}, st_{\text{cert}})$ and $S' = (\pi', p', st'_{\text{std}}, st'_{\text{cert}})$, we have $S \rightarrow S'$ iff one of the following cases hold:

(a) **During the standard phase.** $\pi = \pi' = \text{std}$, $p = p'$, $st_{\text{cert}} = st'_{\text{cert}}$ and $st_{\text{std}} \xrightarrow{\text{std}} st'_{\text{std}}$. This corresponds to a simulation of a standard step of the process $p$.

(b) **During the certification phase.** $\pi = \pi' = \text{cert}$, $p = p'$, $st_{\text{std}} = st'_{\text{std}}$ and $st_{\text{cert}} \xrightarrow{\text{cert}} st'_{\text{cert}}$. This corresponds to a simulation of a certification step of the process $p$.

(c) **From the standard phase to the certification phase.** $\pi = \text{std}$, $\pi' = \text{cert}$, $p = p'$, $st_{\text{std}} = st'_{\text{std}} = ((J, R), \text{HW})$, and $st_{\text{cert}}$ is of the form $((J, R), \text{HW}')$ where for every $x \in \text{Loc}$, $\text{HW}'(x) = \text{HW}(x)\#(\text{msg}, v, q, \{\})$ if $\text{HW}(x)$ is of the form $w \cdot \#(\rightarrow, v, \rightarrow, q)$ with $q \neq p$, and $\text{HW}'(x) = \text{HW}(x)$ otherwise. This corresponds to the copying of the standard LoHoW state to the certification LoHoW state in order to check if the set of promises made by the process $p$ can be fulfilled. The higher order word $\text{HW}'(x)$ (at the beginning of the certification phase) is almost the same as $\text{HW}(x)$ (at the end of the standard phase) except when the rightmost memory type $(\rightarrow, v, \rightarrow, q)$ of $\text{HW}(x)$ is tagged by a reservation of a process $q \neq p$. In that case, we append the memory type $(\text{msg}, v, q, \{\})$ at the end of $\text{HW}(x)$ to obtain $\text{HW}'(x)$. Note that this is in accordance to the definition of capping memory before going into certification: to cite, (item 2 in capped memory of [Lee et al. 2020]), a cap message is added for each location unless it is a reservation made by the process going in for certification.
Copying HW to HW’ symbol by symbol

We can implement copying of HW to HW’ by copying symbol by symbol as follows. Consider any HW(x). Let HW = (aₓWₓ)ₓ∈Loc where HW(x) = aₓWₓ ∈ (Σ⁺(#ΣΓ))⁺, |aₓ| = 1. Define the function copy on the two phases LoHoW state (std, p, ((J, R), (aₓWₓ)ₓ∈Loc), −), and then recursively to subsequent states until we end up in (cert, p, ((J, R), HW), ((J, R), HW)).

The copy function is defined recursively as follows.

(Base) copy(std, p, ((J, R), (aₓWₓ)ₓ∈Loc), −) = (cc, p, ((J, R), (cc ¯aₓUₓ)ₓ∈Loc), ((J, R), (Wₓ)ₓ∈Loc)).

This is copying the first symbol of each HW(x). cc is an intermediate phase used only in copying. Notice that the over lined symbol shows the progress of copying, one symbol each time.

(Inter) Next, we copy subsequent symbols. copy(cc, p, ((J, R), (cc ¯aₓUₓ)ₓ∈Loc), ((J, R), (Wₓ)ₓ∈Loc)) is defined as (cc, p, ((J, R), (cc ¯aₓUₓ)ₓ∈Loc), ((J, R), (Wₓ)ₓ∈Loc)).

(Last) Finally, when all higher order words have been copied, we move from cc to cert. When a higher word has been completely copied, it has the form cc, where a ∈ (Σ⁺#Γ)⁺. Then we define copy(cc, p, ((J, R), (cc ¯aₓUₓ)ₓ∈Loc), ((J, R), (Wₓ)ₓ∈Loc)) as (cert, p, ((J, R), (cc ¯aₓUₓ)ₓ∈Loc), ((J, R), (Wₓ)ₓ∈Loc)), by removing the overline, and having the phase cert.

If the last symbol aₓ in HW(x) is of the form (−, v, −, −, q), for q ≠ p, then copy appends aₓ#(msg, v, q, {}) instead of just aₓ in (Inter).

(d) From the certification phase to standard phase. π = cert, π’ = std, ststd = st’std, stcert = st’cert, and stcert is of the form ((J, R), HW) with HW(x) does not contain any memory type of the form (prm, −, p, −)/(prm, −, p, −) for all x ∈ Loc (i.e., all promises made by p are fulfilled).

Description of the Transducer. We consider 4 cases based on the 4 cases we have in the transition rules (a)-(d) as above.

1. We first consider the case when s and s’ have the same phase (std or cert). If the location involved in the instruction is xᵢ, then the transducer copies all HWₓᵢ, j ≠ i as is. For HWₓᵢ, if the phase we have in Enc(s) is std, then the transducer copies ‡ as well as all symbols after that in the output, while if the phase we have in Enc(s) is cert, the the transducer copies ‡ as well as all symbols before that in the output. This is common to all items below and we will not mention it separately.

(a) Consider a Read instruction of the form λ : $r = xᵢ of the process p. Then the transducer will first guess the value v that will be read and update the local states of the processes (as an output). The only change that the transducer will do concerns the i-th higher order word HWₓᵢ. For each symbol that the transducer reads on the input tape of HWₓᵢ before ‡, it outputs the same symbol. Once the symbol pointed by the process p is read on the input tape, the transducer will check the value of each symbol read on the input tape and if it corresponds to v, the transducer will non-deterministically add p to its pointer set, otherwise it will output the same read symbol (while removing p from its pointer set, which has bee read, if needed).

(b) Consider a Write instruction of the form λ : xᵢ = $r of the process p. Then the transducer will first update the local states of the processes (as an output). The only change that the transducer will do concerns the i-th higher order word HWₓᵢ. For each symbol that the transducer reads on the input tape of HWₓᵢ, it outputs the same symbol. Once the symbol having p in its pointer set is read on the input tape, the transducer will output the same read symbol (while removing p from the pointer set). When the transducer reads a symbol
after #, it can decide to output the new message corresponding to the write instruction and after that, go on by outputting any read symbol.

c) The case of RMW is very similar to the case of a write instruction of the process p.
d) The case of a promise rule is similar to the write. The main difference is that when the transducer reads the symbol pointed by the process p on the input tape, the transducer will output the same read symbol (without removing p from the pointer set). When the transducer reads a symbol right after #, it can decide to output the new promise message, such that the pointer set is empty. After that, it goes on by outputting any read symbol.
e) The case of a reservation rule is similar to RMW.
f) The case of a cancel rule by a process p is as follows. The transducer reads on symbols and outputs the same, till it finds the symbol (−, −, −, p). On reading this, it outputs ε. After that, it goes on by outputting any read symbol.
g) The case of a fulfil rule is as follows. The transducer outputs what it reads till it finds a symbol having p in its pointer set. It outputs the same symbol removing p from the pointer set. Then it continues outputting the read symbol till it reads a symbol (prm, v, p, S). It outputs (msg, v, p, S ∪ {p}) by adding p to the pointer set. After that, it goes on by outputting any read symbol.

h) Consider a SC-fence instruction. In this case the transducer will output any read symbol except the ones that have g or p in its pointer set. If p and g are in the same pointer set, then the transducer will continue outputting any read symbol. If the transducer reads the first encountered symbol that contains only p or g in its pointer set, then the transducer will output the same symbol without the pointer set containing either g or p. Once the transducer reads the second encountered symbol whose pointer set contains only p or g then the transducer will output the same symbol with the pointer set containing both g and p. This is done for each HW

(2) If the phase in Enc(s) is cert and that of Enc(s’) is std, then the transducer simply replaces cert by std, and the process p by any process q, and copies the rest as is in the output.

(3) If the phase in Enc(s) is std and that of Enc(s’) is cert, then the transducer implements the copy function described above. Each copy is implemented by a transducer, and the final result is obtained by composing all these transducers. Note that rational transducers are closed under composition, so it is possible to obtain one rational transducer that achieves the effect of all the copy functions, starting with the std phase and ending in the cert phase. Note that this is easily done, since in each step, the transducer progressively marks a symbol before ¥ with overline, and copies the same at the end.

□

A.3 Proof of Lemma 4.7

Consider K-LoHoW states c₁, c₂ s.t. c₁ → c₂, and let c₃ be a state s.t. c₁ ⊆ c₃. We make a case analysis based on the transition chosen.

Let c₁ = (std, p, ((J₁, R₁), HW₁)), ((J₂, R₂), HW₂)), c₂ = (π, q, ((J₃, R₃), HW₃), ((J₄, R₄), HW₄)), c₃ = (std, p, ((J₁, R₁), HW₅)), ((J₂, R₂), HW₆)), and c₄ = (π, q, ((J₇, R₇), HW₇), (J₈, R₈), HW₈)). The case when c₁ = (cert, p, −, −) is similar to the case we discuss here.

(1) Consider the transition c₁ → c₂ by a read instruction $r = x$ in process p. Then ∃k ≤ j, k = ptr(p, HW₁(x)), and the memory type at HW₁(x)[j] has the form (−, v, −, S), v = R($r$). HW₃(x) is obtained by updating ptr(p, HW₁(x)) to j, so that p is in the pointer set S. Since c₁ ⊆ c₃, there is an increasing function f from the positions of HW₁(x) to that of HW₃(x)
such that $f(k) \leq f(j)$, $\text{ptr}(p, \text{HW}_5(x)) = f(k)$ in $\text{HW}_5(x)$ and the memory type at $f(j)$ has the form $(-, v, -, S')$, $v = R[Sr]$. Indeed, one can update $\text{ptr}(p, \text{HW}_5(x))$ to $f(j)$, obtaining a state $c_4$ from $c_3$. The local process states of $c_4$ is same as that of $c_2$. All higher order words $\text{HW}_5(y)$, $y \neq x$ of $c_3$ remain unchanged in $c_4$ (and all higher order words $\text{HW}_1(y)$, $y \neq x$ of $c_1$ remain unchanged in $c_2$), hence the $\subseteq$ relation holds for these higher order words in $c_2$, $c_4$. The same function $f$ between positions of $\text{HW}_1(x)$ and $\text{HW}_5(x)$ can be used on positions of $\text{HW}_3(x)$ of $c_2$ and $\text{HW}_7(x)$ of $c_4$ to see that $c_2 \subseteq c_4$ and $c_3 \subseteq c_4$.

(2) Consider the transition $c_1 \xrightarrow{\lambda;x=Sr} c_2$. Then, there is a position $k$ in $\text{HW}_1(x)$ such that $k = \text{ptr}(p, \text{HW}_1(x))$. Let the memory type at $\text{HW}_1(x)[k]$ be $(-, v_1, -, S_1 \cup \{p\})$. After the transition, we obtain $\text{HW}_3(x)$ such that $\text{ptr}(p, \text{HW}_3(x)) = j - 1 > k$. There are 2 possibilities.

(a) $j - 1, j$ form the positions of the 2 symbols $\#$, $(\text{msg}, R[Sr], p, \{p\})$ in the newly added simple word in $\text{HW}_1(x)$. Figure 13 depicts this case. Notice that in $\text{HW}_1(x)$, $k = \text{ptr}(p, \text{HW}_1(x))$, and positions $j - 3, j - 2$ represent the last two positions of a simple word. The new simple word is added right after this in $\text{HW}_3(x)$, at positions $j - 1, j$.

![Diagram](13)

Fig. 13. The higher order words in $c_1, c_2, c_3, c_4$ in case (a). The two pink positions correspond to the newly added simple word. The positions $j - 3, j - 2$ have $\#$ and $a \in \Sigma \cup \Gamma$ denoting the end of a simple word in $\text{HW}_1(x)$, so that a new simple word can be inserted right after. The position $k$ in $\text{HW}_1(x)$ is $\text{ptr}(p, \text{HW}_1(x))$. $\text{HW}_4(x) \subseteq \text{HW}_5(x)$ witnessed by the increasing function $f$. $\text{HW}_3(x), \text{HW}_7(x)$ respectively are obtained from $\text{HW}_1(x), \text{HW}_5(x)$ by the $\text{wt}(x, v)$ transition.

Since $c_1 \subseteq c_3$, let $f$ be an increasing function from the positions of $\text{HW}_1(x)$ to those of $\text{HW}_3(x)$. $\text{HW}_7(x)$ is obtained from $\text{HW}_5(x)$ by inserting the new simple word right after position $f(j - 2)$, at positions $f(j - 2) + 1, f(j - 2) + 2$. The position $f(j - 1)$ in $\text{HW}_5(x)$ is shifted to the right by two positions in $\text{HW}_7(x)$. Thus, we can define an increasing function from positions of $\text{HW}_3(x)$ and $\text{HW}_7(x)$ as follows.

- For $i \in \{1, \ldots, j - 2\}$, $g(i) = f(i)$,
- $g(j - 1) = f(j - 2) + 1$, $g(j) = f(j - 2) + 2$, (note that $g(j - 1), g(j)$ are the two new positions in $\text{HW}_7(x)$ corresponding to the new positions $j - 1, j$ in $\text{HW}_3(x)$),
- For $i \in \{j + 1, \ldots, n + 2\}$, $g(i) = f(i - 2) + 2$

It is easy to see that $g$ is an increasing function between the positions of $\text{HW}_3(x)$ and $\text{HW}_7(x)$: we know that $f(j - 2) < f(j - 1)$. Hence, $g(j) = f(j - 2) + 2 < f(j - 1) + 2 = g(j + 1)$. This also gives $\text{HW}_3(x) \subseteq \text{HW}_7(x)$.

(b) $j - 1$ is the position obtained by appending to a simple word in $\text{HW}_1(x)$. Figure 14 illustrates this case. $\text{HW}_1(x) \not\subseteq \text{HW}_5(x)$ is witnessed by the increasing function $f$. The new memory type is added at position $f(j - 2) + 1$ (right next to $\#$), and all subsequent symbols are shifted right by one position. It is easy to see that $\text{HW}_7(x)$ is obtained from $\text{HW}_5(x)$ by the $\text{wt}(x, v)$ transition. The increasing function $g$ from the positions of $\text{HW}_3(x)$ to that of $\text{HW}_7(x)$ is defined as follows.

- For $i \in \{1, \ldots, j - 2\}$, $g(i) = f(i)$,
Fig. 14. The higher order words in \( c_1, c_2, c_3, c_4 \) in case(b). The pink position in \( \text{HW}_3(x) \) corresponds to the newly added memory type, right after \( # \) at position \( j - 3 \) in \( \text{HW}_1(x) \). The position \( k \) in \( \text{HW}_1(x) \) is \( \text{ptr}(p, \text{HW}_1(x)) \). \( \text{HW}_1(x) \subseteq \text{HW}_5(x) \) is witnessed by the increasing function \( f \). \( \text{HW}_3(x), \text{HW}_7(x) \) respectively are obtained from \( \text{HW}_1(x), \text{HW}_5(x) \) by the \( \text{wt}(x, o) \) transition.

- \( g(j - 1) = f(j - 2) + 1 \),
- For \( i \in \{j, \ldots, n + 1\} \), \( g(i) = f(i - 1) + 1 \)

Notice that \( g \) is an increasing function: \( g(j - 2) = f(j - 2) < f(j - 2) + 1 = g(j - 1) \),
\( g(j) = f(j - 1) + 1 > f(j - 2) + 1 = g(j - 1) \), and the same relationship holds for subsequent indices.

(3) The case of \( c_1 \xrightarrow{\lambda \cdot \text{CAS}(x; r_1, r_2)} \text{HW}_5(x) \) is trivial by using the observation that the relative ordering of the pointers \( p \) and \( g \) are same in \( \text{HW}_1(x) \) and \( \text{HW}_5(x) \). \( \text{HW}_3 \) and \( \text{HW}_7 \) are obtained respectively by moving the pointers of \( p, g \) to the rightmost one (whichever it is). So the same increasing function that was used for \( \text{HW}_1 \subseteq \text{HW}_5 \) will work for \( \text{HW}_3 \subseteq \text{HW}_7 \).
B SOURCE TO SOURCE TRANSLATION AND PROOF OF CORRECTNESS

B.1 Intuition for the Translation

2K Timestamps. We bound the number of essential events by K. Why do 2K timestamps suffice?. Intuitively timestamps are used to determine relative order between the events. We track timestamps of the view-switching messages (messages read by other processes), promises and reservations. For each view-switch there are two timestamps of consequence. The timestamp of the reading process before the read and the timestamp of the message to be read. Hence for each view switch, the comparison operation requires us to maintain two timestamps. For a promises (reservation) we maintain the timestamp of the promise (reservation). We do not explicitly store timestamps of messages that will not view switch. These messages however may be read by the same process that generated them. We keep track of whether the latest write can be read by the same process by using some thread-local state.

K + n Contexts. It suffices to have K + n contexts since we can run the processes in the order in which they generate view-switching messages. In each context, the process only depends on the essential messages generated in previous contexts. If this were not the case we would get a deadlock. We require n additional contexts to initialize each process.

B.2 Glossary of Global and Local Variables used in the SC Program

We first give a glossary of all the variables used in the code. The list contains variables global to all processes or local to a process. A small description of their role is also mentioned, which serve as invariants.

(1) **numEE**: a global variable, initialized to 0, keeps track of the number of essential events (promises, reservations and view switches) so far. Each time an essential event occurs, **numEE** is incremented.

(2) **numContexts**: a global variable, initialized to 0, keeps track of the number of context switches so far. This is used in the translation to SC.

(3) **view[x].v**: a local variable, stores the value of x ∈ Loc in the local view of the process.

(4) **view[x].t**: local variable, stores the time stamp ∈ Time of x ∈ Loc in the local view of the process.

(5) **view[x].l**: local variable, boolean, which is set to true when **view[x].t** is a valid timestamp, and can be used in comparisons with timestamps of other messages.

(6) **view[x].f**: local variable, boolean. A true value indicates that **view[x].v** is recent, and can be used for reading locally.

(7) **view[x].u**: local variable, boolean. A true value indicates that the sequence of events starting from the one that resulted in the timestamp **view[x].t** till the most recent, form a chain of CAS operations on x. Whenever a write is published, **view[x].u** is set to true. **view[x].u** is set to false on an unpublished write. On a sequence of CAS operations, **view[x].u** is left unchanged.

(8) **checkMode**: local variable, boolean. Set to true when the process is in certification phase, which means the process is making and certifying promises.

(9) **liveChain[x]**: local variable, for each x ∈ Loc, boolean. Can be true only when **checkMode** is true. A true value indicates that the last write done while the process is in certification phase is not a published promise message.

(10) **extView[x]**: local variable, for each x ∈ Loc, boolean. A true value represents that the local value **view[x].v** of the process comes from a message generated external to the certification phase.
(11) blockPromise[x]: a global boolean array, which for each \( x \in \text{Loc} \) stores whether promises should be blocked on variable \( x \). This is used in the case of \( ra \) writes when we cannot have promises on the same variable later (refer to PS 2.0, \( ra \) accesses).

(12) avail[x][t]: for each \( x \in \text{Loc} \), a global boolean array of length \( 2K + 1 \) corresponding to the \( 2K + 1 \) time stamps, checks availability of a time stamp on a fresh write.

(13) usedReservations[x][t]: denotes whether the reservation on variable \( x \) with timestamp \( t \) has been used by the process during the certification check. If this not true, the reservation will be cancelled.

(14) reserv[x][t]: denotes whether the reservation following timestamp \( t \) on variable \( x \) has been claimed, and if so which process has claimed it.

(15) upd[x][t]: for each \( x \in \text{Loc} \), a global boolean array of length \( 2K + 1 \) corresponding to the \( 2K + 1 \) time stamps, checks whether a certain timestamp has been used to read in a CAS.

(16) globalTimeMap[x]: global variable, for each \( x \in \text{Loc} \), stores a time stamp \( \in \text{Time} \). This is used for simulating SC Fences where this functions as the \( G \) timemap from PS 2.0.

(17) messageStore: This is an array of messages, where each message is of type Message as described in the main paper. The length of the array is \( K \), the bound on the number of promises + view switches.

(18) messagesUsed: a number from 0 to \( K \) which keeps track of the number of populated messages in messageStore.

(19) messageNum: a number from 0 to \( K \) which chooses a number from the available free cells in messageStore.

In addition, the message object stores the following data:

1. mess.var is the shared variable on which the message has been generated
2. mess.t[x] stores for each \( x \in \text{Loc} \) the timestamp of \( x \) in the view object stored in the message
3. mess.l[x] stores for each variable \( x \in \text{Loc} \), a boolean signifying whether the corresponding timestamp stored in mess.t[x] was one of the exact timestamps \( \{0...K\} \) or an abstract timestamp.
4. mess.val stores the value of the message
5. mess.flag stores the promise state of the message, that is whether (1) it is has been fulfilled/is not a promise (2) if it is a promise then the process that it belongs to. mess.flag takes values from 0, -1, PIDs. If it is a simple message (not a promise), mess.flag = 0. If it is a promise, mess.flag is set to the PID of the process which has made the promise. mess.flag is set to -1 when the process has temporarily certified it in the current certification phase but will be reset tp PID after exiting the certification phase.

Next we discuss the context switching modules.

### B.3 Context Switching Modules

**CSI Context-Switch-In.** The CSI module switches the process into context by setting active to true and incrementing numContexts. Finally we check numContexts does not exceed the context switch bound.

```plaintext
Listing 1. CSI
1 if (!active){
2   atomic_begin();
3   active = true;
4   numContexts ++;
5   assume(numContexts <= K + n);
} 
```
CSO Context-Switch-Out. The CSO module has two functions- (1) moving the process from normal to check mode and (2) switching the process out of context. When a process enters the CSO block, with checkMode set to false, it enters the ‘if’ branch on line 2, sets checkMode to true and saves the return label (of the current instruction pointer) in retAddr and saves the process state before entering check mode (lines 9-10). This ensures that the process returns to the current instruction after the consistency check. Now after the consistency check phase the process switches out of context. At this point, checkMode is true, and hence the process enters the ‘else’ branch on line 13. Consequently, we check whether there are no outstanding uncertified promises for the process (line 15). All the promises that have been certified are reset to belong to the process by setting mess.flag to the PID (lines 16-18). Then it is checked that there are no uncertified splitting insertions, by ensuring that liveChain[x] is not true (lines 20-22). Finally we check for unused reservations during certification and cancel them (lines 23-30). Once these checks for consistent configuration are complete, we reload the saved state from before the consistency check phase and reload the return address from retAddr. Then we move control to the instruction label in retAddr. After returning control to label, we set checkMode and active to false and exit context.

Listing 2. CSO

```c
if (*){
  if (!checkMode){
    atomic_begin();
    active = true;
    numContexts ++;
    assume (numContexts <= K+n);
  }
  checkMode = true;
  retAddr = label_i;
  saveState(PID);
}
else {
  for (mess in messageStore){
    assume(mess.flag != PID);
    if (m.flag == -1){
      m.flag = PID;
    }
  }
  loadState(IPID);
  gotoLabel(retAddr);
  label_i:
  checkMode = false;
  active = false;
  atomic_end();
}
```

loadState and saveState subroutines. The saveState subroutine copies the local state of the calling process and the global state into a what we refer to as ‘copy’ variables. We note that it does not however copy numEE, reserv[x][t] and contents of messageStore. The reason for this being, the promises the process makes in check mode are retained even after exiting check mode is made false. Hence the increments made to numEE and the messages added to messageStore should be maintained even after exiting check mode. This is even true for reservations, which are marked in reserv[x][t], which are maintained even after the process exits check mode.

Analogously in loadState, we load the contents of the (saved) ‘copy variables’ into their original counterparts. Another subtle point to be noted is that when the process publishes a message (as a promise) when checkMode is true, we also update the ‘copy’ variables corresponding to avail[x][t]. This is done so that when the process returns to normal mode, the changes are reflected in
their original counterparts (which is essential since promise messages are maintained beyond the time $checkMode$ is false and hence their timestamps must be unavailable).

**B.4 Reads**

We provide the translation codes for reads of both access types, $rlx$ and $ra$. We will first explain with respect to $rlx$ access reads.

*$rlx$ reads. The read can be one of two types, view switching, in which a message from $messageStore$ is acquired or a non view-switching (local) read. We guess non-deterministically, one amongst these.

In case of a local read (line 2), the process checks that the local value is usable (line 3) by checking $view[x].f$ which denotes whether $view[x].v$ is a valid value which can be read. It then loads its local value $view[x].v$ into $r$. The local value may become unusable if the process crosses an SC-fence which increases its $view[x].t$ (see SC-fence).

In the case of a view-switching read (line 6), we check that we have not reached the essential-event bound $K$ (line 7). We ensure that $liveChain[x]$ is false before the read in order to forbid additive insertions when checking consistency. Recall from the $liveChain$ invariant that $liveChain[x]$ is true only when the process is in certification mode and the last write on $x$ was neither published as a promise message nor was it certified with a reservation. Reading a message from the memory when $liveChain[x]$ is true implies additive insertion during certification, as illustrated by the following example.

*liveChain* Assume the process is in the promise certification mode, with $view[x].t$ set to $t_1$, and let the first write use a timestamp $t_2 > t_1$ with the message not published as promise, with $liveChain[x]$ as true. Now the instruction $a:=x$ uses a message in the memory with a timestamp $t_3 \geq t_2$.

If the next write certifies a promise message, the interval in the message will be $t_3 + 1$, since $liveChain[x]$ is true. This results in two writes during the certification, with non-adjacent timestamps $t_2,t_3 + 1$, with only the latter being promised. This behaviour is forbidden in PS 2.0 due to capped memories. Notice that if the earlier write also resulted in a promise message then we do not have additive insertion (since both are promised) and the read with timestamp $t_2$ is allowed since $liveChain[x]$ is false.

Finally a new message is fetched from $messageStore$ with a larger timestamp that the one in the current view (lines 8-11), the process view is updated to include that new message. Whenever a process makes a global read during check mode, it must reads from a message which has been created outside its current certification phase. Hence, $extView[x]$ will be set to true (see $extView$ invariant in the glossary).

```
Listing 3. readrlx
1  // local read
2  if(*){
3    ASSUME(view[x].f);  
4  }
5  // (non-local) view-switching read
6  else {
7     ASSUME(!liveChain[x]);
8     ASSUME(numEE < K);
9     messNum = nondet(0, messageUsed-1);
10    mess = messageStore[messNum];
11    ASSUME(mess.var == x);
12    ASSUME(mess.t[x] > view[x].t or (mess.t[x] == view[x].t and view[x].l == true));
13                        // merge views on x
14    view[x].t = mess.t[x];
15    view[x].l = true;
16    view[x].v = message.val;
```
ra reads. This case is almost similar to the earlier and hence only state the point of difference. The main difference is that due to ra access, we merge (take the join of) all the timestamps rather than just \( x \) as we did for rlx.

Listing 4. readra

```plaintext
// local read
if (*) {
  ASSUME(view[x].f);
}

// (non-local) view-switching read
else {
  ASSUME(numEE < K);
  messNum = nondet(0, messageUsed - 1);
  mess = messageStore[messNum];
  ASSUME(mess.var == x);
  ASSUME(mess.t[x] > view[x].t or (mess.t[x] = view[x].t and view[x].l == true));

  // merge views
  for (y in X) {
    if (mess.t[y] == view[y].t) {
      view[y].l = (mess.l[y]) and (view[y].l);
    } else if (mess.t[y] > view[y].t) {
      ASSUME(!liveChain[y]);
      view[y].t = mess.t[y];
      view[y].l = mess.l[y];
    }
  }
  view[x].v = mess.val;
  extView[x] = true;
  numEE ++;
}

val($r) = view[x].v;
```

B.5 Writes

We now provid the translation of a write instruction \( x = \$r \) of process. Once again we simulate two access modes, rlx and ra. we first describe the relaxed mode and then discuss the changes for the ra mode.

```plaintext
rlx writes. When in normal mode
```

Let us first consider execution in the normal phase (i.e., when checkMode is false). The value of \( \text{val($r$)} \) is recorded in the local view, \( \text{view[x].v} \) and \( \text{view[x].f} \) is set to true meaning that the value in \( \text{view[x].v} \) is a valid value and can be read from. Then, we non-deterministically choose one of three possibilities for the write: it either (i) is not assigned a fresh timestamp, (ii) is assigned a fresh timestamp, (iii) fulfils some outstanding promise. These nondeterministic branches are given on lines 5, 24 and 60 of the code.

Listing 5. writerlx

```plaintext
view[x].v = val($r$);
view[x].f = true;

// no fresh timestamp
if (*){
  view[x].l = false;
  if (checkMode and !liveChain[x]){
    // new write does not rely on reservation
    if (*){
      liveChain[x] = true;
      view[x].t = nondet(view[x].t, MAXTS);
    }
  } else {
    // new write relies on reservation
    view[x].t = nondet(view[x].t, MAXTS);
  }
}
```
In case (i), no message is created, and view[x].l is set to false, signifying that the timestamp recorded in the view does not correspond to the most recent write to x and should therefore not be used in the comparisons. The ‘if’ branch on line 7 is not taken checkMode is false.

In case (ii), since in this case, the timestamp in the view is by definition valid, we set view[x].l to true (line 25). Since the write is relaxed, the message generated will only store the timestamp on the variable written to (i.e. x) and 0 for all other variables (line 27-30). Now we allocate a new timestamp to the write. Since we are in normal mode, liveChain[x] is false (see liveChain invariant in glossary). Thus we choose a timestamp nondeterministically (line 36) and store it into
view[x].t. We use the avail[x][.] array to ensure that allocated timestamps are unique: (1) we check that the selected timestamp is available (i.e., not allocated) on line 40, and remove it from the array of available stamps (line 41). Now this message can either be published (for consumption by another thread) or not. In the former case, the appropriate message is constructed with newView, newViewL. Note that the last component of the message stores the flag mess.flag. This flag is set to false since the message is not a promise (see mess.flag invariant in glossary). In the latter case non of this is done (‘else’ branch on line 55). The assume(!checkMode) is satisfied.

In case (iii) Finally, if the process decides to fulfill a promise, a message is fetched from messageStore and checked to be an unfulfilled promise by the current process (checking flag == p on line 68), and mess.flag is set to 0 and message reinserted into messageStore. Additionally we set extView[x] to true maintaining the extView invariant.

r1x writes. When in check mode

Let us now consider a write executing in the certification phase (i.e., when checkMode is true). We will only highlight differences between the normal and certification phase writes.

In case (i), that is when a fresh timestamp is not assigned, the write is certified either by deferring certification to a promise by using splitting insertion (line 9) or by the a presence of a reservation (line 15). In the case where, liveChain[x] is already true (line 7), certification for the current sequence of writes is already deferred and hence we do none of the two. While certification by either of splitting/reservation we nondeterministically choose an timestamp t after which the current write occurs (line 12). We note that this is not the timestamp of the write itself, but specifies between which two timestamps from Time the write occurs. If we rely on splitting insertion (line 9), we set liveChain[x] to true, and In case of certification by reservation we reserve an interval adjacent to the timestamp t (line 19) after ensuring that it is available (line 18). Finally since this reservation has been used in some certification, we mark this fact (line 20).

In cases (ii), the write is assigned a timestamp from Time and hence consequently published as a promise. We allocate a fresh timestamp and store it into view[x].t. The most important point to note is that we maintain and use the liveChain invariant whenever a fresh timestamp is assigned. Indeed, if liveChain is true, the process must assign consecutive timestamps, otherwise it can non-deterministically choose any timestamp greater than view[x].t (line 32-37). Additionally, when generating a message, the mess.flag is set to −1 denoting that the message is promise but has been certified and publish the message. We also increment numEE (line 48) as a promise is an essential event.

In case (iii) we fulfill an older promise, and thus first retrieve an uncertified promise belonging to the current process (mess.flag == PID) from messageStore (line 68). The main difference with the normal mode is that we set mess.flag to -1 signifying that the promise is (temporarily) certified but not fulfilled. We set the extView[x] to false signifying that the processes’ view has come from checkMode and hence is not external.
ra writes. The ra writes have some minor differences w.r.t rlx. Firstly, the timestamps for all variables view[x][t] are added to the published messages, (lines 27-30). Next we set blockPromise [x] to true signifying that henceforth there cannot be any promises on x (refer to PS 2.0, ra accesses). This also implies that cases (ii) and (iii) (generating new promises and certifying earlier promises) is not possible for ra writes as enforced on (line 23). Note that blockPromise[x] is also assumed to be false in rlx writes when either generating new promises (ii) or certifying earlier ones (iii).

B.6 CAS operations

We only provide code for the CAS(rlx, rlx) variant since the others are implemented similarly, carrying over the access dependent changes from the corresponding read and write codes. CAS is bootstrapping a read and write, additionally enforcing that the timestamps are consecutive.

```plaintext
ASSUME(upd[x][view[x].t] or reserve[x][view[x].t] == p);
reserve[x][view[x].t] = p;
usedReservation[x][view[x].t] = true;
}
else {
ASSUME(! checkMode);
view[x].l = true;
for (y in X){
newView[y] = view[y].t;
newViewL[y] = true;
}
}
// a new timestamp is assigned to this write
else if (*){
view[x].l = false;
if (checkMode and ! liveChain[x]){  // new write does not rely on reservation
if (*){
// only true if process is in checkMode
liveChain[x] = true;
view[x].t = nondet(view[x].t, MAXTS);
}
// a new timestamp is assigned to this write
else if(*){
view[x].l = true;
for (y in X){
newView[y] = 0;
newViewL[y] = true;
}
}
```
newView[x] = view[x].t + 1;
else {
    newView[x] = nondet(view[x].t + 1, MAXTS);
}

view[x].t = newView[x];
ASSUME(avail[x][newView[x]]);
avail[x][newView[t]] = false;

// essential message
if (*) {
    if (checkMode)
        ASSUME(! blockPromise[x]);
    mess = genMessage(x, newView, newViewL, val($r), -1);
    liveChain[x] = false; numEE ++;
} else {
    mess = genMessage(x, newView, newViewL, val($r), 0);
}
Publish(mess);
}
else {
    ASSUME(! checkMode);
}

// a previous Promise is certified
else {
    ASSUME(! blockPromise[x]);
    view[x].l = true;

B.7 Fences

SC-fence. The SC-fence command essentially merges the thread local view with the globally stored view in globalTimeMap. For each shared variable x we do the following. On line 3 we check whether the globally stored view globalTimeMap[x] is greater than the process local view. if that is the case, we increase the process-local view view[x].t to the globally stored view. Additionally, we set view[x].f to false since, the value in view[x].val is no more valid (cannot be read from again, since the process timestamp has increased). In the order case, (line 8), we raise the globalTimeMap[x] either to view[x].t (if it is valid, checked by line 9) or to the next higher timestamp, view[x].t + 1.

Listing 8. SC-fence

assume(! checkMode);
for (x in Loc){
    if (globalTimeMap[x] > view[x].t){
        view[x].t = globalTimeMap[x];
        view[x].f = 0;
    }
}

view[x].l = true;
} else {
    if (!checkMode){
        extView[x] = true;
    } else {
        extView[x] = false;
    }
}
view[x].u = true;
B.8 Correctness of Translation (Proof of Theorem 5.1)

The proof is in two parts. In the first part, we show that every $K + n$ context bounded run of $Prog'$ in SC corresponds to a $K$-bounded run of $Prog$ under PS 2.0, and in the second part, we show that for every $K$-bounded run in PS 2.0, there is a $K + n$ context bounded run in SC.

At the outset we review a high level description of the translation. We denote by normal and checkMode, the two phases respectively where checkMode is false and checkMode is true. These are the two phases in which a process functions. Each process executes instructions in the normal phase by skipping over the CSO blocks of code. When a process needs to switch out, it enters the CSO block following the most recent instruction executed and sets checkMode to true. Now, it makes a “ghost” run in checkMode, a terminology to indicate that this phase of the run does not change the the global state and local state of the process permanently (this is facilitated by the saveState and loadState functions). One exception to this is the writes that the process makes as reservations, and published promises which are maintained permanently. Hence, this part of the run is equivalent to the process making fresh promises after a normal execution; providing a witness for consistency and then switching out of context. The run then is a sequence of interleaved normal and checkMode phases. Moreover, the local states of the process is identical at the start and end of any given checkMode phase.

We request the reader to refer to the glossary [B.2] of the variables used which will aid in better understanding of the translation.

We give the proof of correctness of the translation through two sections.

**Intuition** The translation relies on the fact that in a run of the $K$-bounded PS 2.0 program, it suffices to store the relative order only between $K$ totally ordered timestamps for each variable. Additionally, these $K$-timestamps are precisely those corresponding to the $K$ essential events - promises, reservations, view-altering reads. While we maintain an exact ordering between essential events, those of non-essential events (which are none of view-altering reads, reservations or promises) are abstracted in the SC run. Thus in the original run under PS 2.0, all timestamps are exact, while in the run under SC, the non-essential timestamps are abstracted away.

The correctness of the translation then relies on being able to faithfully concretize the abstract timestamps from the SC run. We account for these concretizations by separating the essential timestamps by sufficiently large intervals, so that, the non-essential timestamps can be inserted in between, respecting their order.

**SC to PS 2.0**

**Details** We start from SC to PS 2.0. We show that every $K + n$ context bounded run of $Prog'$ under SC corresponds to a $K$-bounded run of $Prog$ under PS 2.0-rlx. Keeping in mind the description above, we split this proof into two parts.

1. First, we consider only runs in normal mode and prove that they have an analog in PS 2.0.
2. Second, we prove that any run in checkMode is indeed an analog of a process making fresh promises and reservations and certifying them along with previous unfulfilled promises, before switching out of context.

Combining these two, indeed, we will have a run under PS 2.0.

We begin by defining some terminology. Consider a run $\tau$ of program $Prog'$. Each event of the run $\tau$ is an execution of either a read, write, CAS or SC-fence. A read in this run is called global...
(and otherwise local) if the process decides to read from the global array $messageStore$. Only global reads can be view-altering in the corresponding run under PS 2.0. A write can be of three types - publishedS, publishedF and local. These represent, ‘simple published’, ‘fulfilling published’, and ‘timestamp not assigned writes’ respectively. Note that each of these types can be performed in normal as well checkMode. A CAS can therefore be of 6 types since it involves a read and write. At a high level this translation is facilitated by the following two key observations:

- The number of publishedS, publishedF writes are bounded due to the bound $K$, and hence the requisite data-structure for these can be maintained using bounded space.
- Local writes are unbounded, however, these writes are only used (read-from) locally by the writing process and need not be stored permanently by the algorithm.

Let $w_1$ be the number of write events in the normal mode of run $\tau$, $w_2$ be the maximum number of write events, maximum being taken over all checkMode phases of the run, $u - 1$ be the number of CAS events in the run, and let $\ell = w_1 + w_2 + u$. Let $M_x$, for each shared variable $x$, be an increasing function from $[2K]$ to $\mathbb{N}$ representing a mapping from the notion of time-stamps in SC to time-stamps in PS 2.0. For each variable $x$, and each process $p$, let $\text{View}_{SC}(x) = \text{view}[x].t$ (defined above) and $\text{View}_{PS\ 2.0}(x)$ be the time stamp of $x$ in the view of $p$ in $\rho$. Given a run $\tau$, we will construct a $K$ bounded run of $\text{Prog}$ which reaches the same set of labels after $i$ events, for any $i$.

We will first treat the normal (non-checkMode) part of the run. While going through the steps, we will also construct the increasing functions $M_x$. In addition to the invariants in B.2, we maintain the following timestamp-based invariants for all processes $p$ and variables $x$.

1. If $\text{view}[x].l$ is true for a process in $\tau$, then $M_x(\text{View}_{SC}(x)) = \text{View}_{PS\ 2.0}(x)$.
2. If $\text{view}[x].l$ is true and the time-stamp $\text{view}[x].t$ corresponds to a write message instead of a message added due to a CAS, then $M_x(\text{view}[x].t) = \text{view}[x].t \cdot \ell \cdot u$.
3. If $\text{view}[x].l$ is false, then $M_x(\text{view}[x].t) < \text{View}_{PS\ 2.0}(x) < (\text{view}[x].t + 1) \cdot \ell \cdot u$. Moreover, if the last event to assign false to $\text{view}[x].l$ was a write, then $\text{View}_{PS\ 2.0}(x)$ is a multiple of $u$.
4. If a message is of type CAS, then its time-stamp $t$ in $\rho$ satisfies $t \equiv 0 \pmod{u}$.
5. The sum of view-switch points and promises is at most $K$ in $\rho$.
6. The time-stamps of essential messages in $\tau$ and the corresponding message in $\rho$ are related by $M_x$. That is, $M_x(\text{View}_{SC}(x)) = \text{View}_{PS\ 2.0}(x)$.

The base case, that is, after 0 events ($i = 0$) is trivial since the configurations are semantically equivalent and we define $M_x(0) = 0$ for all variables, which satisfies the invariants. We make the following three cases depending on the $i^{th}$ event of $\tau$.

- Case 1. $e_i$ is an execution of a write for process $p$, variable $x$ and value $v$.
  - If the write is of publishedS or publishedF type, then $\text{view}[x].t$ is updated from $t$ to a new time-stamp $t'$ (which in the case of publishedF is the timestamp of the retrieved message) and $\text{view}[x].l$ is assigned true. In $\rho$, if we can make $\text{View}_{PS\ 2.0}(x) = t'' = t' \cdot \ell \cdot u$ then the invariants are satisfied. It is not possible for $t''$ to have been assigned already to some write message in $\rho$ since $t'$ was not assigned to some message in $\tau$ (checked using $\text{avail}[x][t']$). A CAS message could not have been assigned $t''$ either, by the fourth invariant. Since $t < t'$, $\text{View}_{PS\ 2.0}(x) < t''$ (by invariants 2 and 3). Hence, $\text{View}_{PS\ 2.0}(x)$ can be updated to $t''$ since it is available and is greater than the current view. If the write is published, then the message is added to $messageStore$. This is done to maintain invariant (6). Note how, if the write is of publishedF type, the message flag is set to 0, effectively removing it from the promise bag and maintaining the flag invariant (refer to [B.2]).
  - If the write is local, then we pick the smallest available multiple of $u$ between $M_x(\text{view}[x].t)$ and $(\text{view}[x].t + 1) \cdot \ell \cdot u$. This can always be done since there are $\ell - 1$ multiples of $u$.
between \( \text{view}[x].t \cdot \ell \cdot u \) and \((\text{view}[x].t + 1) \cdot \ell \cdot u \) and there are \( \leq (\ell - 1) \) messages (even considering those produced in \( \text{checkMode} \)) in total. Notice that multiples of \( u \) have been reserved for writes by invariant 4.

- **Case 2.** \( e_i \) is an execution of a read for process \( p \), variable \( x \).
  - If the read is local in \( \tau \), then the process is either reading a local message written by itself or a useful message (a useful message is one which is read by a process, but does not create a change of view). In either case, this read can be performed in \( \rho \) without any change in time-stamps. Note that this cannot be a view-switching event. Moreover note that the local value in \( \text{view}[x].v \) has been ascertained to be usable.
  - If the read is global, then \( \text{numEE} < K \) before the read and therefore \( \text{numEE} \leq K \) afterwards. In this case, a message is fetched from \( \text{messageStore} \) and the process view is updated according to this message. Since \( M_x \) is an increasing function, the results of comparisons in \( \text{SC} \) will be the same as in PS 2.0 and the read operation has the same effect on values and time-stamps of the variables. Moreover \( \text{view}[x].f \) is set to true maintaining the \( \text{view}[x].f \) invariant [B.2].

- **Case 3.** \( e_i \) is an execution of a CAS for process \( p \), variable \( x \) and values \( v \), \( v' \).
  - If the read here is local and \( \text{view}[x].u \) is true then we need to ensure that the timestamp chosen for the write immediately follows \( M_x(\text{view}[x].t) \). It is first checked if \( \text{view}[x].t \) has been used for an update earlier or not. If it has not been, then the time-stamp \( M_x(\text{view}[x].t) + 1 \) is available in PS 2.0 since all messages that come from writes have time-stamps in multiples of \( u \) and \( M_x(\text{view}[x].t) \) is a multiple of \( u \). Note, that we also ensure that \( \text{view}[x].f \) is true in this case, which implies that the local value is usable.
  - If the read here is local and \( \text{view}[x].u \) is false (and hence so is \( \text{view}[x].l \)), then it definitely has not been used for an update (CAS) in \( \tau \) since the process reading the message is the only one that knows of its existence. Now, if this message was a result of a local write, then its time-stamp \( t \) in PS 2.0 is a multiple of \( u \) and \( t + 1 \) is available for the update message. Otherwise, this message was a result of a CAS whose write was local and has a time-stamp of the form \( a \cdot u + b \) where \( b < u \). Note that this implies \( b + 1 \) consecutive CASs were made to get here since all the messages that are a result of (non-CAS) write operations get time-stamps that are multiples of \( u \). Since \( u - 1 \) is the total number of CASs in \( \tau \), \( b < u - 1 \) (at most \( u - 2 \) CASs have taken place before this one). This implies \( a \cdot u + b + 1 \) is available and can be used for the write.
  - If the read is global, then it is done correctly as explained in Case 2. The write part of the CAS goes through as explained above.

- **Case 4:** \( e_i \) is an SC-fence
  - We iterate over the variables, updating \( \text{globalTimeMap}[x] \) and \( \text{view}[x].t \) to the maximum of the two.
  - In case the former was greater, we set \( \text{view}[x].l \) to true, signifying that \( \text{view}[x].t \) is valid and maintaining invariant (1) above. Moreover we set \( \text{view}[x].f \) to false. This is necessary since, the timestamp of the message corresponding to \( \text{view}[x].v \) is now less than \( \text{view}[x].t \) and hence the locally stored value is unusable.
  - If the latter is greater, we check whether \( \text{view}[x].l \) is true (which signifies that \( \text{view}[x].t \) is valid). If it is we can set \( \text{globalTimeMap}[x] \) to it. If not, then the \( M_x(\text{view}[x].t) < \text{View}_{\text{PS 2.0}}(x) \) (by invariant (6)), and hence we set it to \( \text{view}[x].t + 1 \). Finally we note that \( \text{View}_{\text{PS 2.0}}(x) < (\text{view}[x].t + 1) \cdot \ell \cdot u \) and hence \( M_x(\text{globalTimeMap}[x]) \) now matches the essential event immediately following the event with timestamp \( \text{view}[x].t \).
We now briefly justify the checkMode phase of the run. For any such phase, we need to ascertain that the run has analogous run in PS 2.0 which respects the notion of consistency. The management of timestamps is identical to the normal phase explained above so we only highlight the special aspects. First we recall some invariants:

1. \( \text{liveChain}[x] \) is true only when the most recent write made in the current checkMode phase was unpublished (was not a promise) and neither was it certified using a reservation.
2. \( \text{extView}[x] \) is true if \( \text{view}[x].v \) corresponds to a message from outside checkMode.
3. For the process \( p \) currently in checkMode, \( \text{message\_flag} \) is -1 for temporarily (only within current checkMode phase) certified promises and is \( p \) for as yet uncertified promises. If it is \( p' \neq p \), then the message is in the promise bag of some other process. Additionally if it is 0, it is not in the promise bag of any process. Note how this is maintained in the write, CAS sections above.

We review how these invariants are maintained and used throughout the code. When entering checkMode, \( \text{liveChain}[x] \) is false. For any write happening in normal phase we set \( \text{extView}[x] \) to true. Otherwise we set it to false. Once again we consider cases for a particular event \( e_i \):

- **Case 1.** \( e_i \) is a write event.
  - In the case, the process performs a local write, the process can either set \( \text{liveChain}[x] \) is set to true, maintaining the invariant or it can generate a reservation which will be used to certify the write. In this case the reservation is marked as used.
  - In the case the process decides to publish a write it must publish it as a promise, incrementing \( \text{numEE} \) (after checking that the bound of \( K \) has not been crossed), setting the promise flag to -1, maintaining invariant (3) above (leading to a publishedS write). Also, if it decides to certify a previous promise, it does so, similar to the normal phase, though it now sets the timestamp to -1, indicating that the certification is local to the current phase and must be reset when normal phase resumes. Moreover (publishedF write) note that \( \text{liveChain}[x] \) is set to false maintaining invariant (1).
  - Also, note that \( \text{extView}[x] \) is set to true maintaining invariant (2).
- **Case 2.** \( e_i \) is a read event.
  - The main highlight of read events in checkMode, is that we ascertain that \( \text{liveChain}[x] \) is false while making a global read. This is to ensure that we forbid additive insertion. Indeed, following invariant (1) above, if \( \text{liveChain}[x] \) were true during a global read, it would mean that the interval corresponding to the previous message (which caused \( \text{liveChain}[x] \) to be true) is additively.
- **Case 3.** \( e_i \) is a CAS event.
  - Once again similar to normal phase we guess whether we make a local or a global read. Crucially however, we note that we forbid making a local write for a CAS when \( \text{extView}[x] \) is true. Considering the invariant (2) above, this is done precisely to forbid CAS where, the promised interval containing the write is non-adjacent to the message being read from. The remainder book keeping is identical to previous cases.
- **Case 4.** \( e_i \) is a SC-fence event. This case does not arise since a process in checkMode may not execute a SC-fence instruction, as otherwise the run will not be consistent [Kang et al. 2017; Lee et al. 2020].

To conclude, note due to loadState and saveState functions, only used reservations and promises are retained after the checkMode phase. Moreover due to the check of message flags after termination of a checkMode phase, it is ensured that the process is in a consistent state while switching contexts. Noting that we keep track of promises as well as view-switches using \( \text{numEE} \) we may only generate a run in which the sum of the two is bounded by \( K \).
Next, we consider the converse direction from PS 2.0-rlx to SC.

**PS 2.0 to SC**

We now prove the second part, from PS 2.0 to SC. We prove that for every $K$-bounded run $\rho$ in PS 2.0, there is a $K + n$ context bounded run $\tau$ in SC. We will show this in two steps.

- Given the $K$-bounded $\rho$, first we will construct a run $\rho''$ which is $K$-bounded and $K + n$ context bounded that reaches the same configuration as $\rho$.
- We will then construct a run $\tau$ of SC using $\rho''$.

**Intuition** While we concretized the abstract (non-essential) timestamps when going from SC to PS 2.0 earlier now we do the opposite. However, we will additionally show that $K + n$ SC contexts suffice for the translation. The way we account for the $K + n$ contexts is as follows - $n$ contexts for the process initializations and (atmost) one context for each essential event.

Hence, we ensure that at least one essential event occurs in each context. This is possible for the following reason. Consider a run with $K$ essential events occurring in some order executed by processes $p_1$ to $p_K$. If we schedule the processes $p_i$ in the run under SC in the same order, then we will get a valid run under SC. Since view-switches account for all the external reads-from dependencies, the run which we obtain is also valid.

More concretely, we ensure that each process only switches out of context only when it is awaiting a message for an external read from another process or when it has made at least one promise or reservation. Since the total number of such essential events along a normal phase + additional messages in all checkMode phases is bounded above by $K$, we need at most $K + n$ context switches. We add $n$ for the concluding contexts required to reach the term configurations.

**Details** Let $rf$ (called reads-from) be a binary relation on events such that $(e_a, e_b) \in rf$ iff $e_b$ reads from a message published by $e_a$. Note that every run under PS 2.0 semantics defines a $rf$ relation as the reads are executed. For construction of $\rho''$, the intuition is that a context switch is required only when the current process has reached term or it needs a message that is yet to be published by some other process. At a configuration $\varsigma_i$ of $\rho$, we say that an event of $\rho$ is a requesting event if it is a view-altering event in $\rho$ and it reads a message that is not in the message pool at $\varsigma_i$. Also, we call the events that publish messages for these events as servicing events (write or CAS, either simple or promises). Note that the set of servicing and requesting events is dependent on the configuration $\varsigma_i$. The two sets change along the run $\rho$. Specifically, an event is removed from the requesting event set as soon as the servicing event corresponding to it is executed. Let the size of the set of requesting events be $r$. At $\varsigma_{\text{init}}, r = K$. We will prove by induction that given a set of processes $(n)$, the $rf$ relation, and a run $\rho$ in PS 2.0 that maintains the $rf$ relation, there is a run which uses at most $r+n$ context switches and defines the same $rf$ relation.

**The Base Case.** For $r + n = 1$, there is only one process so the number of context switches is 0 and the run $\rho$ itself uses 0 context switches.

**The Inductive Step.** Assume the hypothesis for $r + n = \ell$ and we prove the claim for $r + n = \ell + 1$. Clearly at $\varsigma_{\text{init}}$, there is at least one process which either has no requesting events, or has a servicing event before any requesting events in its instruction sequence. Otherwise, the run $\rho$ will not be able to execute all the events since no process will be able to move past its requesting event. If we have a process that can reach termination directly, then in $\rho''$, we run that process and reduce $r + n$. Otherwise, consider the instructions of the process $(p_j)$ that has a servicing event before any of its requesting events. The instructions of $p_j$, till the first requesting event, can be executed since all the messages they need are already in the pool and hence we can create a new run $\rho_t$ in which these instructions are executed first and the remaining ones follow the same order as $\rho$. Note that $\rho_t$ reduces $r$ by at least 1 while executing the instructions of $p_j$. By applying the hypothesis on the
remaining sequence of instructions, we have a run that uses \( r - 1 + n \) context switches and that
maintains \( rf \) of the remaining instructions. This can now be combined by the instructions of \( p_j \)
that have already been executed to give \( \rho'' \).

We now construct the run \( \tau \) from \( \rho'' \). As explained in the text above, at most \( 2K \) time-stamps are
needed to simulate the \( \rho'' \). Let the set of such time-stamps be \( U \times x \) for each variable \( x \). Let \( M_x \) be an
increasing (mapping) function for each variable from \( U \times x \cup \{0\} \) to \( \{0, \ldots, 2K\} \) such that \( M_x(0) = 0 \).

We will construct the run \( \tau \) in SC from \( \rho'' \), event by event, while maintaining the following
invariants

1. All the time-stamps, in a particular message in \( messageStore \), are related to the time-stamps
   in the corresponding essential messages in PS 2.0 by \( M_x \).
2. For a process \( p \), \( View_{PS \ 2.0}(x) \in U \times x \) iff \( view[x] \).l is true at that point in SC and \( view[x] \).t =
   \( M_x(View_{PS \ 2.0}(x)) \)

The \( i^{th} \) event of \( \rho'' \) can be one of the following:

- Case 1. \( e_i \) is a write to variable \( x \) with value \( v \).
  - If the time-stamp \( t \) of this write belongs to \( U \times x \), then we first allocate \( M_x(t) \) in SC to this
    write and make \( view[x] \).l true. This maintains invariant (2).
  - If the event is a servicing event, then the time-stamp of this message satisfies the require-
    ments of invariant (1) and hence it can be added to \( messageStore \). Otherwise, we do not
    update the \( View_{SC}(x) \) of the process and make \( view[x] \).l false.

- Case 2. \( e_i \) is a read of variable \( x \).
  If this event is a view-altering event, then the current timestamp in the \( View_{PS \ 2.0} \) will be
  used for comparison. The effect of the read in SC will be same as in PS 2.0 since \( V \times x \) is
  an increasing function. All the invariants will still hold after this, since all the messages in
  \( messageStore \) satisfy the invariants.

- Case 3. \( e_i \) is a CAS to variable \( x \) with values \( v, v' \). If this event is not view-altering, then the
  process either reads some other process’s message again or reads its own. If it reads its own
  message, then no change to the \( View_{SC}(x) \) has to be done for the read part and the new
  message is added to \( messageStore \) if \( e_i \)'s message is essential. If it reads some other processes’
  message again, then \( view[x] \).l is true, and since this message has not been used for a CAS
  yet, the check of \( upd_{x}[view[x] \cdot t] \) will go through in \( Prog' \). Now, it needs to be decided if
  the new message is essential. If the read is view-altering, then it is similar to Case 2 followed
  by the decision of adding the new message to \( messageStore \).

- Case 4. \( e_i \) is an SC-fence If \( globalTimeMap[x] \) is greater than \( view[x] \).t, we maintain
  invariants (2) by setting \( _view[x] \).l to true and the \( view[x] \).f invariant [B.2] by setting it to
  \( view[x] \).f. On the other hand, if \( view[x] \).t is greater, we set \( globalTimeMap[x] \) to the small-
  est member \( t \in Time \), which satisfies \( t \geq M_x(View_{PS \ 2.0}(x)) \). In case \( view[x] \).t is true, \( t \) is
  \( view[x] \).t itself by invariant (2). If not, then we set it to \( view[x] \).t + 1, since we note that
  \( view[x] \).t is the largest member of Time, that \( p \) has had as \( View_{PS \ 2.0}(x) \), and currently the
  former is lower than \( M_x(View_{PS \ 2.0}(x)) \).
C COMPLETE EXPERIMENTAL RESULTS

We report the results of experiments we have performed with PS2SC. We have two objectives: (1) studying the performance of PS2SC on benchmarks which are unsafe only with promises and (2) comparing PS2SC with other model checkers when operating in the promise free mode. In the first case, we show that PS2SC is able to uncover bugs in examples with low interaction with the shared memory. When this interaction increases, however, PS2SC performs poorly, owing to the huge non-determinism required by PS 2.0. However, with partial promises, PS2SC is once again able to uncover bugs in reasonable amounts of time. In the second case, our observations highlight the ability to detect hard to find bugs with small $K$ for unsafe benchmarks, and scalability by altering $K$ as discussed earlier in case of safe benchmarks. We compare PS2SC with three state-of-the-art stateless model checking tools, CDSCHECKER [Norris and Demsky 2013], GenMC [Kokologiannakis et al. 2019] and Rcmc [Kokologiannakis et al. 2017] that support the promise-free subset of the PS 2.0 semantics.

We now report results of all the experiments we have performed with PS2SC. In the tables that follow we provide the value of $K$ used (for our tool only). We also specify the value of $L$ used (for all tools).

We do not consider compilation time for any tool while reporting the results. For our tool, the time reported is the time taken by the CBMC backend for analysis. The timeout used is 1 hour for all benchmarks. All experiments are conducted on a machine equipped with a 3.00 GHz Intel Core i5-3330 CPU and 8GB RAM running a Ubuntu 16 64-bit operating system. We denote timeout by ‘TO’, and memory limit exceeded ‘MLE’.

C.1 Experimenting with Promises

In this section we experiment with PS2SC in the promise-enabled mode.

Litmus Tests. We first test the tool on a number of litmus tests obtained from various sources. This has two objectives: (a) to perform sanity checks on the correctness of the tool (b) to gain an understanding of the causes of performance bottlenecks when handling promises. The results of these tests are summarized in Table 9 below. We tested PS2SC on many litmus tests from [Chakraborty and Vafeiadis 2019a; Kang et al. 2017; Lee et al. 2020; Svendsen et al. 2018]. In these PS2SC terminated with the correct result within one minute, with the value of $K$ used for the unsafe trace being at most 5. We also tested PS2SC on the Java Causality Tests of Pugh [Manson et al. 2005], which were also experimented on in Paviotti et al. [2020]. In these too we were able to verify most examples within one minute. However, PS2SC timed out (TO = 30 mins) on two tests.

| testcase   | $K$ | PS2SC       |
|------------|-----|-------------|
| ARM_weak   | 4   | 0.765s      |
| Upd-Stuck  | 4   | 1.252s      |
| split      | 4   | 25.737s     |
| LB         | 3   | 1.469s      |
| LBd        | 3   | 1.481s      |
| LBfd       | 3   | 1.512s      |
| LBcu       | 4   | 5.255s      |
| LB2cu      | 4   | 5.748s      |
| CYC        | 5   | 1.967s      |
| Coh-CYC    | 5   | 42.67s      |

Table 9. Performance of PS2SC on PS 2.0 idioms
Modular Promises. In this section we ask whether the source-to-source translation technique can effectively scale while handling promises for PS 2.0. In conclusion, we note that our approach performs well on programs requiring limited global memory interaction. When this interaction increases PS2SC times out, owing to the huge non-determinism of PS 2.0. However, the modular approach of partial-promises enables us to recover effective verification.

| testcase       | K | PS2SC[1p] |
|----------------|---|-----------|
| fib_global_2   | 4 | 55.972s   |
| fib_global_3   | 4 | 2m4s      |
| fib_global_4   | 4 | 4m20s     |
| exp_global_1   | 4 | 19m37s    |
| exp_global_2   | 4 | 41m12s    |
| tri_global_2   | 4 | 52.973s   |
| tri_global_3   | 4 | 1m57s     |
| tri_global_4   | 4 | 3m58s     |

Table 10. Performance of PS2SC on cases with global update

C.2 Comparing Performance with Other Tools

| benchmark      | L  | K  | PS2SC   | CDSChecker | GenMC | RCMC   |
|----------------|----|----|---------|------------|-------|--------|
| exponential_5_unsafe | 10 | 10 | 1.312s  | 0.900s     | 0.135s| 6.692s |
| exponential_10_unsafe | 10 | 10 | 1.854s  | 1.921s     | 0.367s| 3m41s  |
| exponential_25_unsafe | 25 | 10 | 3.532s  | 7.239s     | 3.736s| TO     |
| exponential_50_unsafe | 50 | 10 | 6.128s  | 36.361s    | 39.920s| TO     |
| exponential_70_unsafe | 10 | 10 | 9.509s  | 1m33s      | 2m29s | TO     |
| fibonacci_2_unsafe | 2  | 20 | 2.746s  | 2.332s     | 0.084s| 0.086s |
| fibonacci_3_unsafe | 3  | 20 | 9.392s  | 46m8s      | 0.462s| 0.544s |
| fibonacci_4_unsafe | 4  | 20 | 34.019s | TO         | 12.437s| 18.953s|

Table 11. Comparison of performance on a set of parameterized benchmarks

| benchmark      | L  | K  | PS2SC   | CDSChecker | GenMC | RCMC   |
|----------------|----|----|---------|------------|-------|--------|
| hehner2_unsafe | 4  | 5  | 7.207s  | 0.033s     | 0.094s| 0.087s |
| hehner3_unsafe | 4  | 5  | 28.345s | 0.036s     | 2m53s | 1m13s  |
| linuxlocks2_unsafe | 2  | 4  | 0.547s  | 0.032s     | 0.073s| 0.078s |
| linuxlocks3_unsafe | 2  | 4  | 1.031s  | 0.031s     | 0.083s| 0.081s |
| queue_2_safe   | 4  | 4  | 0.180s  | 0.031s     | 0.082s| 0.085s |
| queue_3_safe   | 4  | 4  | 0.347s  | 0.037s     | 0.090s| 0.092s |

Table 12. Comparison of performance on concurrent data structures based benchmarks
| benchmark       | L  | K  | PS2SC | CDSChecker  | GenMC  | RCMC    |
|-----------------|----|----|-------|-------------|--------|---------|
| readerwriter_7  | 0  | 5  | 0.719s| 0.005s      | 0.057s | 0.690s  |
| readerwriter_8  | 0  | 5  | 0.839s| 0.006s      | 0.056s | 7.425s  |
| readerwriter_9  | 0  | 5  | 1.068s| 0.007s      | 0.053s | 1m17s   |
| readerwriter_10 | 0  | 5  | 1.393s| 0.007s      | 0.056s | 14m49s  |
| redundant_co_10 | 10 | 5  | 0.470s| 0.114s      | 0.087s | 38m12s  |
| redundant_co_20 | 20 | 5  | 1.031s| 0.548s      | 0.218s | TO      |
| redundant_co_50 | 50 | 5  | 3.219s| 8.965s      | 4.143s | TO      |
| redundant_co_70 | 70 | 5  | 6.095s| 13.843s     | 18.185s| TO      |

Table 13. Evaluation using two synthetic safe benchmarks. We note that the value of \( K \) is chosen to be large enough to consider all executions.

| benchmark       | L  | K  | PS2SC | CDSChecker  | GenMC  | RCMC    |
|-----------------|----|----|-------|-------------|--------|---------|
| peterson1U(4)   | 1  | 6  | 1.408s| 0.039s      | TO     | 9.129s  |
| peterson1U(6)   | 1  | 6  | 7.286s| 0.010s      | TO     | TO      |
| peterson1U(8)   | 1  | 6  | 47.786s| 0.010s     | TO     | TO      |
| peterson1U(10)  | 1  | 6  | 4m19s | TO          | TO     | TO      |

Table 14. Comparison of performance on mutual exclusion benchmarks with a single unfenced process.

| benchmark       | L  | K  | PS2SC | CDSChecker  | GenMC  | RCMC    |
|-----------------|----|----|-------|-------------|--------|---------|
| peterson1C(3)   | 1  | 2  | 0.487s| 0.053s      | 0.083s | 0.087s  |
| peterson1C(4)   | 1  | 2  | 1.193s| 3.500s      | TO     | 3.360s  |
| peterson1C(5)   | 1  | 2  | 2.713s| TO          | TO     | TO      |
| peterson1C(6)   | 1  | 2  | 6.045s| TO          | TO     | TO      |
| peterson1C(7)   | 1  | 2  | 11.008s| TO         | TO     | TO      |

Table 15. Comparison of performance on completely fenced peterson mutual exclusion benchmarks with a bug introduced in the critical section of a single process.

| benchmark       | L  | K  | PS2SC | CDSChecker  | GenMC  | RCMC    |
|-----------------|----|----|-------|-------------|--------|---------|
| peterson3       | 1  | 2  | 0.878s| TO          | 9.665s | 26.208s |
| peterson2       | 1  | 2  | 0.321s| 0.325s      | 0.087s | 0.068s  |
| peterson3       | 2  | 4  | 1.695s| TO          | MLE    | TO      |
| peterson2       | 2  | 4  | 0.539s| 15m22s      | 0.039s | 0.428s  |
| peterson3       | 4  | 4  | 15.900s| TO         | MLE    | TO      |
| peterson2       | 4  | 4  | 3.412s| TO          | TO     | TO      |

Table 16. Evaluation using safe mutual exclusion protocols.