Analog Multiplication in Random Demodulation
Analog–to–Information Converters

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Abstract. Aim of this paper is to compare in Analog-to-Information Converters the working principles of the two devices typically used to perform the operation of multiplication: mixers and analog multipliers. The comparison has been experimentally realized on two AIC prototypes based on the Random Demodulation principle: the former employing a mixer, the latter employing an analog multiplier.

Keywords: Analog-to-Information Converters; Mixers; Analog Multipliers; Testing

1. Introduction

The actual need of data monitoring at even increasing bandwidths cannot be easily satisfied by existing acquisition schemes because of limited sampling rates of Analog-to-Digital Converters (ADCs) that rely on the Nyquist-Shannon theorem. This desire to overcome limitations on frequency has encouraged the implementation of a new signal acquisition framework, the Compressive Sampling [1]. Such framework admits signals to be represented by a lower rate in case they are compressible, i.e. if they carry much smaller information than the signal support in a certain domain. By exploiting the CS theory, an Analog-to-Information Converter (AIC) is a device that accepts as input an analog signal and generates as output a compressed digital version of the input. In other words, the output is composed of a down–sampled number of measurements than required by the Nyquist-Shannon theorem: the purpose of an AIC is to realize in only one step sampling and compression of the original signal. This technology has been applied to many research fields especially for monitoring purposes, such as cognitive radios [2] and code division multiple access receivers [3].

AIC architectures require an accurate model of the analog front–end to enable a correct recovery in the digital domain of the input. In fact, AIC hardware components deviate from their desired design behavior and reconstruction algorithms are sensitive to such deviations. Although several efforts have been made in the research community to propose AIC architectures and schemes, only few papers face the problem of testing these new devices. The most widespread type of AIC prototypes show a common...
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architectural block in the acquisition section intended to modulate the input signal before sampling it. In such architectures the non–linear intermodulation of the mixer is a significant non–ideality that distances the practical behavior of the AIC from the ideal one. In [4] the frequency–domain second order Volterra kernels is proposed to evaluate simultaneously non–linearity and dynamic behavior of a broadband mixer.

Aim of this paper is to experimentally evaluate the AIC behavior in case an analog multiplier replaces a mixer. The rest of the paper is structured as it follows. Section 2 explains the multiplication process in AICs based on the principle of the modulation. In Section 3 the behavior of mixer and analog multiplier in AIC has been experimentally compared through a Random Demodulation (RD) AIC prototype and the results obtained are discussed.

2. Multiplication process in modulation–based AIC architectures

AIC prototypes are generally diversified depending on the structure of the acquisition section. Among all types of AIC architectures, it is possible to identify a major group based on the principle of modulating the input signal with a Pseudo Random Binary Sequence (PRBS) before a sub-sampling step. Such architectures can be found structured either on a single channel - as the RD [5] - or multiple channels - as the Modulated Wideband Converter [6]. The mathematical law modeling the acquisition process in this case is typically considered linear. However, in practice an AIC cannot be modeled as perfectly linear. To support this, mathematical laws to linearly model the same AIC architecture can lead to different results [7]. Moreover, several non–idealities come into play in the pre–modulation step of the input signal, such as actual shape and jitter of each symbol of the PRBS modulating the input signal [8, 9]. An other significant non–ideality coming into play in the modulation–based AICs is the non–linear intermodulation of the mixer which is in charge of multiplying the input signal with the PRBS. In fact, the output of the mixer is not linear but it is located in all the possible combinations of the input frequencies [10]: $f_{OUT} = n_1f_{IN2} \pm n_2f_{IN2}$, with $n_1$ and $n_2$ two generic integer numbers. As a consequence, the wideband use of the mixer implies the presence of harmonic distortion that fall in the same band of the signal.

Alternatively, the analog multiplier performs the multiplication between two input signals, too. Compared to the mixer, the analog multiplier has a more similar behavior to the ideal multiplication, showing a better linearity on both input channels [11]. In case of multipliers, the multiplication provides an outcome that is simply located at the difference and the sum of the input frequencies: $f_{OUT} = f_{IN1} \pm f_{IN2}$.

3. AIC prototypes and experimental comparison

Aim of the analysis is to evaluate whether the behavior of the analog multiplier, compared to a mixer, can bring to an improvement of the RD AIC performances. The two AIC prototypes used in this work abide by the block scheme reported in Fig. 1.
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Figure 1. RD block scheme: the red circuit symbol represents either a mixer or an analog multiplier.

Analog input $x(t)$ is multiplied with a PRBS $p(t)$, coming from a Tektronix AWG420 Arbitrary Waveform Generator. In this work, the Analog Devices AD8342 and the Analog Devices AD834 are employed respectively as mixer and analog multiplier of the modulation block of the two AIC prototypes. Then, the mixed signal $m(t)$ is low-pass filtered by means of the Analog Devices ADRF6510 evaluation board. Finally, the filtered signal $f(t)$ is acquired by the Analog Devices AD9230 evaluation board that is in charge of digitizing and transferring to the computer the $M$–samples of the AIC output, $y_r$, by means of a HSC-ADC-EVALC capture board. A clock signal is given to the capture board by means of an Agilent E4438C Analog Signal Generator. The performances of the AIC prototype have been quantified in terms of the Model Error ($ME$):

$$ME_{dB} = 20 \log \left( \frac{(y_r - y_i)_{rms}}{(y_i)_{rms}} \right) = 20 \log \left\{ \frac{\sqrt{\sum_{m=1}^{M} [y_r(m) - y_i(m)]^2}}{\sqrt{\sum_{m=1}^{M} y_i^2(m)}} \right\}$$  (1)

where $y_i$ represents the ideal output, obtained according to a mathematical model. Let $x$ be the vector of $N$–samples of the input signal that would be acquired if an ADC replaced the AIC, with $N > M$; $y_i$ is evaluated as:

$$y_i = \Phi x = \frac{1}{N} F^{-1} H F P x,$$  (2)

with $H$, $P$ and $F$ all $N \times N$ diagonal matrices. In particular, $P$ has as elements the PRBS symbols $\{p_n\}_{n=1}^{N}$ and $F$ is the DFT matrix. $H$ represents the frequency response of the filter and its elements $\{H_n\}_{n=1}^{N}$ are experimentally acquired by characterizing the Analog Devices ADRF6510 low-pass filter.

The results of the experiments show the $ME_{dB}$ versus the frequency of the sinusoidal input in the range $[1, 24.22]$ MHz on an average of 20 runs. The PRBS has been generated with a bit rate of 200 MHz. Both the AIC input signal and the PRBS are of length $N = 512$. The figures show a lower $ME_{dB}$ in case of the architecture based on the analog multiplier, than in case of the architecture based on the mixer. Specifically, Fig. 2a highlights a trend of the $ME_{dB}$ in case of mixer decreasing as the input frequency increases: it tends to become stable around the value of $-17.5$ dB. Fig. 2b shows the $ME_{dB}$ in case of analog multiplier: it ranges around the value of $-31$ dB and its gain is at least of about 10 dB compared to $ME_{dB}$ of the mixer.
4. Conclusions

The experimental results show that the analog multiplier has the capability of representing the ideal AIC output with a lower error in comparison to the mixer. Further work will be devoted to compare the experimental output of the two AICs with a calibration model in order to include the non-idealities of the architecture.

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