Analytical Expressions of Time-Domain Responses of Protection Circuits to ISO Reverse Transients in Automotive Applications

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ABSTRACT As the use of semiconductors and electronic control units (ECU) in automobiles has increased, electromagnetic susceptibility has become more essential for the reliability of the ECUs. As a result, automotive ECUs are subjected to electromagnetic compatibility tests to control quality. The Test pulses for electromagnetic immunity testing in automotive industry, such as reverse transients 1 and 3a, defined in the International Organization for Standardization (ISO) 7637-2 standard document, are examined. In practice, it is necessary to analytically investigate the performance of the protection circuits against those reverse pulses. In this paper, theoretical expressions of time-domain responses of the capacitor filter to those reverse pulses are derived. Also, the expressions of the avalanche energy as well as the time during avalanche mode are presented. The analytical results, validated by LTspice simulation, show that for the case of pulse 1, the reversal battery-polarity protection device after the filter, i.e., low-voltage power metal-oxide-semiconductor field-effect transistor (MOSFET), is safe despite entering the avalanche breakdown mode. For the case of pulse 3a, the filter can almost completely remove the transient voltage and hence avoid the avalanche effect of the MOSFET. The verified expressions when the suppressed voltage reaches maximum are very helpful for hardware design engineers to quickly determine whether the MOSFET goes into avalanche breakdown.

INDEX TERMS Automotive applications, avalanche breakdown, circuit analysis, electromagnetic interference (EMI), immunity testing, MOSFET, time-domain analysis

I. INTRODUCTION As the use of semiconductors and electronic control units (ECU) in automobiles has increased, electromagnetic susceptibility...
susceptibility has become more essential for the reliability of the ECUs and the safety of automobiles [1]–[2]. In the harsh automotive environment, ECUs are exposed to different electrical and electromagnetic disturbances, which can degrade their performance or even damage the electronic hardware. The origin and electrical characteristics of the electrical transients and their simulated test pulses are presented in the International Organization for Standardization (ISO) 7637 standard document [3]. Low-voltage power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely used in the ECUs, such as body control module, power steering, multimedia head unit and window lifter, etc., as they have low on-resistance, which makes them suitable for high current operation with low power loss and high efficiency [4]–[5]. Specifically, they are known to be an effective strategy to protect the ECUs against reverse polarity of the battery for high current applications. Low-voltage power MOSFETs are more likely to enter avalanche breakdown region as compared to high-power MOSFETs if the ISO 7637 reverse voltage pulses are applied into the system because the applied reverse voltage may exceed their limited maximum breakdown voltage. As a result, the passive filter components are commonly employed to suppress the maximum voltage of the ISO reverse pulses in order to avoid the avalanche breakdown or reduce its energy and hence ensure the MOSFET is safe during electromagnetic compatibility (EMC) compliance testing and in vehicle operation.

In [6], the authors examined Spice models including the linear model and the non-linear models provided by the manufacturers of the overvoltage suppression devices against the electrical fast transients (EFT) and electrostatic discharge (ESD). The test pulses 1, 3a, and 3b from ISO 7637-2 standard were compared with the actual transient events and the observed waveforms were explained as a result of contact arcing phenomena in [7]. N. Lambrecht et al. [8] proposed a circuit modeling technique for the ISO 7637-3 capacitive coupling clamp (CCC) test by making use of the transmission line theory and the concept of surface transfer impedance and surface transfer admittance.

In order to improve design efficiency, both free and licensed circuit simulation software programs can be used for simulating an electronic circuit’s behavior such as LTspice by Analog Devices, TINA-TI by Texas Instruments, NgSpice (open source) [9], SiMetrix by SiMetrix Technologies and PSPICE by Cadence, etc. However, the availability of many simulation programs, created by different electronic component manufacturers in the market, may lead to difficulty in their usage if the circuit components are selected from different manufacturers. The reason is that the component manufacturer companies usually allow the usage of their Simulation Program with Integrated Circuit Emphasis (SPICE) models only in their own simulation software program, but restrict them in other software programs. A typical example is that most of the MOSFET SPICE models from Texas Instruments are encrypted and cannot be used in LTspice. Therefore, in some designs with mixed components from different manufacturers, the analytical expressions for the electronic circuit are extremely important tool for the hardware design engineers as these expressions only need the electrical parameters from the datasheets, which are always available to the designers.

From the literature survey, it appears that no prior research has been done for analytical expression derivation of the suppressed voltage on the protection circuits with respect to the ISO 7637-2 reverse test pulses. Therefore, in this paper, the voltage formulas for the capacitor filter will be derived for the ECUs employing N-channel power MOSFET reverse polarity protection scheme when the reverse transients are applied. These expressions can be a valuable tool for the hardware design engineers to assess the performance of the protection filter and determine whether the MOSFET can sustain the avalanche energy especially in the design cases where the electronic components are chosen from different manufacturers. Additionally, these analytical expressions aim to be used for the purpose of optimization of the capacitor filter by finding the optimum value, where the energy during avalanche breakdown has the largest margin from the energy limit. These expressions will help the hardware engineers to minimize the design effort and increase the chance to pass the immunity testing, and in the end to save the cost and meet the product timeline because it is more effective to consider EMI issues at the design stage [10]. Here, immunity is defined as the ability of the ECUs to function correctly whilst being subjected to all kinds of undesired disturbances [11].

The remainder of the paper is organized as follows. In the next section, the ISO 7637-2 reverse test pulses are described. In Section III, the voltage expressions are derived. Section IV presents simulation circuit in LTspice. Section V provides the numerical results, discussion, as well as the validation of the derived expressions via comparison with the simulation. The conclusion is given in the last section.

II. REVERSE PULSES AND PROTECTION CIRCUIT

Automotive electrical and electronic (EE) architecture is tremendously complex with ECUs, actuators, sensors and wiring harness. In addition, these electronic components, as well as the wiring harness, have been increased continuously in terms of number, complexity, weight, and volume [12]. Consequently, there are many electrical transients caused by inductance, capacitance, resistance and switching processes in the EE system during vehicle operation. The ISO test pulses 1, 2a, 2b, 3a and 3b are defined in ISO 7637-2 standard document. Among them, pulses 1 and 3a are the reverse conducted transients along power supply lines.

Test pulse 1 appears when power supply is disconnected from the inductive loads which are connected in parallel with a device under test (DUT). In such a case, the DUT will be interfered by the test pulse 1, which is presented in Fig. 1 [3].
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The detailed electrical characteristics of this pulse are provided in Table I for 12 V electrical system. Test pulse 3a, illustrated in Fig. 2, is a simulation of transient caused by the switching process in EE system including fuse blowing or pulling out. This pulse is a burst transient which electrical parameters are given in Table II [3]. It should be noted that transient 3a is applied to the system in form of a burst of multiple pulses, which is separated by $t_s$.

The main idea is to derive calculation formula of the suppressed voltage for the commonly-used capacitor filter and investigate the avalanche breakdown of the polarity-protection MOSFET. The circuit diagram is presented in Fig. 3 [13, Fig. 1a]. The ECU load can be protected against reverse-polarity connection by inserting a MOSFET in the right direction in the battery line. For high-side reversal battery protection, an N-channel MOSFET has been widely employed as it has the lowest power loss as compared to diode and P-channel MOSFET. Despite this, a charge pump is required to provide a gate voltage greater than the battery voltage to be able to turn the N-channel MOSFET on. This in turn increases the circuit complexity, bill of material cost and electromagnetic interference (EMI) issue [13]. When power of correct polarity is applied, the intrinsic body diode in MOSFET $Q_1$ conducts and provides power to the charge pump and the rest of the circuit. Within a few milliseconds, the charge pump has produced enough voltage to turn the MOSFET on and then bypass its own diode. During reverse polarity of the battery, the control circuit connects gate to source and the MOSFET will be switched off.

In order to meet EMC requirements, two 4.7 µF capacitors ($C_1$, $C_2$) are included and placed orthogonally (OP) to avoid thermal incident. $R_1$, $R_2$, $D_1$, $D_2$, $Q_2$, and $C_3$ form a control circuit. This control circuit will short the gate and source of $Q_1$ in case of reverse battery, and by contrast, it will allow current flow if the battery is installed properly. The resistors $R_1$ and $R_3$ are used for limiting the current to the MOSFET $Q_1$’s gate and to the transistor $Q_2$’s base, respectively, whereas the resistor $R_2$ creates a discharge path for the MOSFET $Q_1$’s gate. The capacitor $C_3$ is employed to filter high-frequency noise at the base of transistor $Q_2$. In addition, the diodes $D_1$ and $D_2$ are added to prevent reverse current to the microcontroller charge pump pin and reverse-bias of the emitter-base junction of the transistor $Q_2$ from the battery input voltage, respectively. As mentioned, the transistor $Q_2$ is used to connect gate to source of the MOSFET in case of reverse battery. The MOSFET $Q_2$ used here is an Automotive Electronics Council (AEC) Q101 qualified device (BUK7Y7R6-40EX of Nexperia B.V.), which can handle the junction temperature from -55°C to 175°C. This MOSFET has the maximum on-state resistance of 7.6 mΩ and the minimum breakdown voltage of 40 V. The MOSFET with small on-state resistance is chosen so that the power loss is reduced [14]. In addition, all other components used in the circuit are also selected as AEC qualified. KL30 UBAT12V is connected to the battery positive terminal of a 12V vehicle system, whereas UBAT12V_RPP is connected to the ECU circuit. In most applications, MOSFETs are directly driven by a logic circuit or a microcontroller [15].

**TABLE I**

| Parameter                  | Symbol | Value   |
|----------------------------|--------|---------|
| Peak amplitude             | $U_i$  | -75 V to -150 V |
| Internal resistance        | $R_i$  | 10 Ω    |
| Pulse duration             | $t_d$  | 2 ms    |
| Pulse rise time            | $t_r$  | 1 µs    |
| Pulse repetition time      | $t_r$  | ≥ 0.5 s |
| Time between supply disconnects | $t_s$ | 200 ms |
| Time from supply disconnection to pulse application | $t_s$ | < 100 µs |

**TABLE II**

| Parameter                  | Symbol | Value   |
|----------------------------|--------|---------|
| Peak amplitude             | $U_i$  | -112 V to -220 V |
| Internal resistance        | $R_i$  | 50 Ω    |
| Pulse duration             | $t_d$  | 150 ns ± 45 ns |
| Pulse rise time            | $t_r$  | 5 μs ± 1.5 μs |
| Pulse repetition time      | $t_r$  | 100 μs  |
| Burst duration             | $t_b$  | 10 ms   |
| Time between bursts        | $t_b$  | 90 ms   |

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In this circuit, VCP is connected to the microcontroller charge pump pin.

III. ANALYSIS

The double exponential pulse shape of transients 1 and 3a, as shown in Fig. 1 and Fig. 2, can be generated by a transient generator and its voltage function is given by [3]

$$U(t) = \frac{U_0 R_L}{R_i + R_L} e^{\frac{2.3}{t_d}}$$  \hspace{1cm} (1)

where $U_0$ denotes the open circuit output voltage, $R_i$ and $R_L$ denote the source resistance of the generator and the load resistance of the generator, respectively. $t_d$ is the reverse pulses’ duration, provided in Tables I and II.

In (1), the term $U_0 R_L/(R_i + R_L)$ is the peak amplitude $U_i$ of the reverse pulses, listed in Tables I and II. Therefore, the corresponding voltage function of those pulses in general form can be expressed in terms of Heaviside function and (1) as

$$v(t) = U_i e^{\frac{2.3}{t_d}} u(t - \beta) + \alpha U_{BAT}$$  \hspace{1cm} (2)

Note that

$$\beta = t_0 + i(1 - \alpha)t_1 + (i-1)t_1$$  \hspace{1cm} (3)

where $t_0$ denotes the moment at which the transient voltage starts falling down from the battery voltage $U_{BAT}$ and $i$ is the pulse cycle order in the transient burst. $t_1$ and $t_3$, provided in Tables I and II, are the pulse repetition time and the time from supply disconnection to pulse application, respectively. $u(t - \beta)$ denotes the Heaviside function. Note that in (2) and (3), the term $\alpha = 0$ represents pulse 1, whereas $\alpha = 1$ represents pulse 3a.

It is important for a hardware design engineer to know the peak suppressed voltage in order to determine if the MOSFET $Q_1$ goes into avalanche breakdown mode. To do so, we can disconnect the MOSFET $Q_1$ and the control circuit ($R_1, R_2, R_3, D_1, D_2, Q_2,$ and $C_3$) from the reverse voltage source and its capacitor filter. Then we analyze and determine the peak suppressed voltage on the capacitor filter. The ISO pulse, as shown in Fig. 3, has the internal source resistance. Therefore, it can be separated into the pulse voltage source and its internal resistance. These two circuit elements together with the two orthogonal capacitors $C_1$ and $C_2$ form a voltage divider network, which can be converted into frequency domain, as depicted in Fig. 4. The Laplace transform of the voltage across the capacitors can be expressed as

$$V_c(s) = \frac{V_s(s)}{R C (s + \frac{1}{R C}) + \frac{1}{R C}},$$

where $V_s(s)$ is the Laplace transform of $v(t)$ and $C$ is the effective capacitance of $C_1$ and $C_2$. By applying $t$-transition rule [16], the Laplace transform of (2) can be obtained as

$$V_s(t) = U_s e^{-\beta t} + \frac{\alpha U_{BAT}}{s}$$

Following that, by substituting (5) into (4) and after some mathematical manipulations, the Laplace transform of the voltage across the capacitors can be derived as
The corresponding expression of the suppressed voltage in time domain can be obtained by performing the inverse Laplace transform:

\[ v_c(t) = \mathcal{L}^{-1}v_c(s) = \frac{U_i t_d}{t_d - 2.3RC} u(t - \beta) \left( e^{\frac{2(1-\beta)}{t_d}} - e^{\frac{1-\beta}{RC}} \right) + \alpha U_{BAT} \left( 1 - e^{\frac{1-\beta}{RC}} \right) + V_c(\beta^+) e^{\frac{1-\beta}{RC}}. \]  

(7)

The peak suppressed voltage can be calculated by substituting the time to reach the peak voltage \( t_{peak} \) into (7). The time \( t_{peak} \) can be obtained by taking derivatives of the double exponential curve of the suppressed voltage. For a 12V vehicle system, considering less than 100 uF value of \( C_1 \) and \( C_2 \), in (7), the fourth and fifth terms are very small as compared to the first term. As a result, in order to simplify the algebraic manipulations, these terms and the third term (the derivative of a constant is zero) can be ignored when taking the derivatives of (7). The simplified form of (7) can be expressed as

\[ v_{cde}(t) = \frac{U_i t_d}{t_d - 2.3RC} u(t - \beta) \left( e^{\frac{2(1-\beta)}{t_d}} - e^{\frac{1-\beta}{RC}} \right). \]  

(8)

After some algebraic manipulations of differential equation \( \frac{dv_{cde}(t)}{dt} = 0 \), the peak time can be achieved as

\[ t_{peak} = \beta + \frac{t_d RC}{t_d - 2.3RC} \ln \left( \frac{t_d}{2.3RC} \right). \]  

(9)

The detailed derivation of (9) is provided in the Appendix.

In case that the MOSFET goes to avalanche mode, we need to investigate whether it can withstand this avalanche condition. To do so, the avalanche energy of the MOSFET needs to be evaluated. On the basis of the suppressed voltage expression derived in (7), the MOSFET’s time in avalanche can be obtained as

\[ t_{ava} = \beta + \frac{t_d}{2.3} \ln \left( \frac{V_{ava}(t_d - 2.3RC)}{U_i t_d} \right). \]  

(10)

The derivation of (10) is introduced in the Appendix. Note that \( V_{ava} \) is the MOSFET’s avalanche breakdown voltage. As the current during avalanche follows the shape of the reverse voltage pulse applied [3], it can be expressed as

\[ i_{ava}(t) = I_{ava, peak} e^{-\frac{2t}{t_{ava}}}. \]  

(11)

where \( I_{ava, peak} \) represents the peak avalanche current. Owning the fact that the ECU load’s capacitance is large and the MOSFET’s time in avalanche is short, the voltage on the ECU load is assumed to be almost unchanged during the avalanche. Hence, the avalanche current, which depends on the potential difference between the ECU load voltage UBAT12V_RPP, the avalanche breakdown voltage \( V_{ava} \), and the reverse pulse voltage, reaches its maximum when the reverse pulse voltage is equal to the peak amplitude \( U_i \). As a result, the peak avalanche current can be expressed as

\[ I_{ava, peak} = \frac{U_i - V_{ava}}{R_i}. \]  

(12)

Since the avalanche breakdown is constant, the corresponding avalanche energy can be obtained by integrating (11) and is evaluated as

\[ E_{ava} = V_{ava} \int_0^{t_{ava}} I_{ava, peak} e^{-\frac{2t}{t_{ava}}} dt. \]  

(13)

After some simplifications, the avalanche energy can be obtained as

\[ E_{ava} = \frac{1 - e^{-2.3}}{2.3} V_{ava} I_{ava, peak} t_{ava}. \]  

(14)

IV. SIMULATION

In Fig. 5, a complete circuit with test pulse 1 is built in LTspice software to validate the theoretical expressions derived in Section III. For the reverse test pulse 3a, the Spice model of \( U_1 \) in Fig. 5 will be replaced with Pulse3a_12V. The total capacitance after the input reverse polarity protection is assumed to be 270 µF. In LTspice, by default, \( t_0 \) is defined as 1ms for both test pulses, whereas \( t_3 \) is set to be 50 µs for pulse 1 [17].

V. NUMERICAL RESULTS AND DISCUSSIONS

In this section, both analytical and simulated results of the suppressed voltage at the capacitor filter are presented. For a fair comparison, \( t_0 \), used in calculation formulas (2) – (9), is assumed to be the same with the one in LTspice ISO pulse models, i.e., \( t_0 = 1 \) ms for both transients. In addition, the avalanche breakdown of the MOSFET is also investigated. The values of parameters \( U_i, t_d, t_1, t_3 \) and \( R_i \) of the reverse test transients 1 and 3a can be found in Tables I and II, respectively. Note that \( t_3 \) does not exist for pulse 3a. In this study, the pulse amplitudes \( U_i \) are selected as -150 V and -220 V, respectively, which are the highest severity levels according to Table A.1 of [3].
Fig. 6 shows the test pulse 1 voltage, both theoretical and simulated results of the voltage suppressed by the two orthogonally placed capacitors $C_1$ and $C_2$ against the reverse pulse 1. Note that these results were obtained when separating the circuits as mentioned in Section III. The effective capacitance $C$ is calculated as $C = C_1C_2/(C_1 + C_2) = 2.35 \mu F$. The battery voltage $U_{BAT}$ is 13.5 V for a 12 V automotive system. The close match in both results validates the theoretical expressions (2) – (9) derived in Section III. Moreover, the peak voltage at the capacitors can be quickly obtained by substituting the peak time $t_{peak}$, calculated from (9), into (7). It can be observed that the capacitor filter can reduce the pulse voltage to -135.69 V at $t_{peak} = 1.137$ ms.

In this case, the MOSFET goes to avalanche mode as the breakdown voltage of the MOSFET is significantly exceeded (as a rule of thumb: avalanche occurs at 1.3 times [18] the rated breakdown voltage of a low voltage MOSFET (52 V for $Q_1$)). This may lead to a high electric field applied between source and drain, and the fast increased avalanche current in an exponential way may in turn damage the component [19], because the reverse current flow through the device causes high power dissipation, associated temperature rise, and potential device destruction [18]. In Fig. 7, the simulated MOSFET’s Source-Drain voltage and current waveforms are provided to verify the theoretical expressions (10) – (12) derived in Section III. It can be observed that the MOSFET’s Source-Drain voltage is clamped to its avalanche voltage $V_{ava} = -44$ V and the peak avalanche current is $I_{ava,peak} = 11.43$ A. From this figure, the time in avalanche $t_{ava}$ is measured to be 1.006 ms. By using formulas (10) and (12), the calculated results of $t_{ava}$ and $I_{ava,peak}$ are 0.994 ms and 11.9 A, respectively. Thus, the close match in the simulated and theoretical results validates the derived expression (10) – (12).
Numerical result of the avalanche energy can be obtained by using the analytical expression (14). By substituting the calculated values of $t_{ava}$ and $I_{ava,peak}$ into this equation, it can be found that $E_{ava} = 195.2 \text{ mJ}$, which approximately agrees with the simulated result shown in Fig. 8. In order to determine the limit of avalanche energy that the device can sustain $E_{ava,limit}$, we need to convert the power in double exponential shape, illustrated in Fig. 8, to a square pulse. This can be achieved by equating their energies, as depicted in Fig. 9.

With the help of (16), for the case of power waveform in the avalanche mode, as shown in Fig. 8, it can be found that $t_{d,sq} = 0.389 \text{ ms}$. From Fig. 10, it can be found that the transient thermal impedance $Z_{th(j-mb)} = 0.318 \text{ K/W}$. According to [21] – [23], the transient thermal impedance is calculated as

$$Z_{th(j-mb)} = \frac{T_{j} - T_{mb}}{P}$$

(17)

where $T_{j}$ and $T_{mb}$ represent the MOSFET’s junction temperature and the operating temperature, respectively. $P$ is the dissipated power on the MOSFET. As a result, the avalanche energy limit can be derived as

$$E_{ava,limit} = \frac{T_{j,max} - T_{mb,max}}{Z_{th(j-mb)}} I_{ava} = 280.9 \text{ mJ}.$$  

(18)

Note that $T_{j,max} = 175^\circ\text{C}$ denotes the maximum junction that the MOSFET can withstand and $T_{mb,max} = 85^\circ\text{C}$ is the maximum operating temperature, which is commonly defined in automotive applications. It can be concluded that the MOSFET is safe since $E_{ava} < E_{ava,limit}$ with a good margin.

In Fig. 11 (a), the reverse test pulse 3a waveform is presented with the highest severity level for 12V system, i.e., $U_s = -220 \text{ V}$. In order to emphasize the accuracy of the
general-form theoretical equations derived in Section III, both analytical and simulated results of the suppressed voltage by the capacitor filter against test transient 3a are illustrated in Fig. 11 (b). Note that these results were obtained when disconnecting the MOSFET and its control circuit as mentioned in Section III. Again, it can be observed that the close match in both results validates the derived expressions. It should be noted that the close match occurs for all the pulses in the transient burst, which consolidates the generality of the obtained equations for the whole burst for both reverse test pulses. As it can be seen from this figure, the capacitor filter can almost completely remove the applied pulses, which helps to prevent the MOSFET $Q_1$ from entering avalanche mode. This is because the effective capacitance is large enough to mitigate the transients with short duration like pulse 3a. In addition, the peak time and the peak voltage across the capacitors, as shown in Fig. 11 (b), are also quickly calculated with help of derived expressions (7) and (9).

The expressions derived in Sections III and V can be used to optimize the passive capacitor filter. Based on these expressions, the time to reach the peak voltage $t_{peak}$, the peak suppressed voltage $V_{c, peak}$, the MOSFET’s time in avalanche $t_{ava}$, the avalanche energy $E_{ava}$, the avalanche energy limit $E_{ava, lim}$ and the margin of avalanche energy are calculated for the ISO reverse pulses and are then summarized in Table III. Note that in case the MOSFET enters avalanche breakdown, the margin of avalanche energy can be determined by the calculated avalanche energy and the avalanche energy limit. As an example of optimization of the suppression filter, the values of the capacitors $C_1$ and $C_2$ are selected from 1 uF to 10 uF. From Table III, it can be found that the value of 3.3 uF is the optimum value as the margin of the avalanche energy from its limit is the largest (30.58%). The more the margin is, the less the MOSFET is derated.

### VI. CONCLUSION

In this paper, the analysis of protection performance of the capacitor filter from the reverse EMC immunity test transients along power supply lines has been presented. The paper briefly describes the electrical characteristics of those automotive test pulses, and introduces the circuit design, as well as the LTspice circuit simulation in detail. Based on the forward and inverse Laplace transforms, including the $t$-transition rule, as well as by using the Heaviside function, analytical expressions for the suppressed voltage and its peak value of the employed filter, as well as the MOSFET’s avalanche energy have been derived. All theoretical derived expressions have been validated by simulation results. Furthermore, the strength of those theoretical expressions is the accuracy for all the pulses of the testing burst. In addition, these derived expressions are quite helpful in the design cases where the electronic components are selected from different manufacturers.

| Reverse Pulse 1 | Reverse Pulse 3a |
|-----------------|-----------------|
| $C_1$, $C_2$ (uF) | $V_{c, peak}$ (V) | $t_{peak}$ (ms) | $E_{ava}$ (mJ) | $E_{ava, lim}$ (mJ) | Margin of $E_{ava}$ (%) | $V_{c, peak}$ (V) | $t_{peak}$ (ms) |
| 1                | 0.975           | 203.4          | 280.2          | 27.41            | 1.04039          | 12.84          |
| 2.2              | 0.981           | 199.6          | 281.6          | 30.58            | 1.40044          | 13.14          |
| 3.3              | 0.994           | 195.2          | 280.9          | 30.51            | 1.40047          | 13.23          |
| 4.7              | 1.048           | 195.6          | 280.2          | 30.19            | 1.40049          | 13.28          |
| 6.8              | 1.021           | 196.9          | 278.6          | 29.33            | 1.40051          | 13.32          |
| 10               | 1.022           | 196.1          | 278.6          | 29.33            | 1.40054          | 13.34          |

**TABLE III**

**COMPARISON BETWEEN DIFFERENT TYPICAL VALUES OF THE CAPACITOR FILTER**

**APPENDIX**

### A. DERIVATION OF THE TIME TO REACH THE PEAK VOLTAGE $t_{peak}$

The differential equation of the simplified form of the suppressed voltage $\frac{dV_{c, peak}(t)}{dt} = 0$ can be obtained as

$$
\frac{2.3(t_{peak} - 6)}{t_d - 2.3RC} e^{\frac{2.3(t_{peak} - 6)}{t_d}} + \frac{U_{t_d}}{R_C(t_d - 2.3RC)} e^{\frac{t_{peak} - 6}{R_C}} = 0.
$$

By moving the first term of (19) to the right side and then taking the natural logarithm of both sides of (19), we obtain

$$
\ln\left(\frac{U_{t_d}}{R_C(t_d - 2.3RC)}\right) - \frac{t_{peak} - 6}{R_C} = \ln\left(\frac{2.3U_c}{t_d - 2.3RC}\right)
$$

Following that, the expression of the peak time $t_{peak}$ is derived, as given in (9).

### B. DERIVATION OF THE MOSFET’S TIME IN AVALANCHE $t_{ava}$
When the MOSFET goes into avalanche breakdown mode, the suppressed voltage on the capacitor filter is equal to the MOSFET’s avalanche breakdown voltage

\[
\frac{U_{s}t_{d}}{t_{d} - 2.3RC} \left( e^{-\frac{2.3(t_{ava} - \beta)}{t_{s}}} - e^{-\frac{t_{ava} - \beta}{RC}} \right) = V_{ava}.
\]  (21)

Following that, (21) can be rewritten as

\[
- e^{-\frac{2.3(t_{ava} - \beta)}{t_{s}}} - e^{-\frac{t_{ava} - \beta}{RC}} = \frac{V_{ava}(t_{d} - 2.3RC)}{U_{s}t_{d}}.  \tag{22}
\]

As the second term at the left side of (22) is very small as compared to the first term, (22) can be simplified to

\[
e^{-\frac{2.3(t_{ava} - \beta)}{t_{s}}} = \frac{V_{ava}(t_{d} - 2.3RC)}{U_{s}t_{d}}.  \tag{23}
\]

By taking the natural logarithm of both sides of (23) and after some mathematic manipulations, the expression of MOSFET’s time in avalanche \( t_{ava} \) is derived, as given in (10).

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