Effect of wafer defects on electrical properties and yields of SiC Devices

Ling Li1,2, *, Hailiang Yan1,2, Jialin Li1,2, Qingling Li1,2, Tao Zhu1,2, Hao Wu1,2, Rui Liu1,2, Rui Jin1,2 and Junmin Wu1,2

1State key laboratory of advanced power transmission technology, Beijing, China
2Global energy interconnection research institute CO., LTD., Beijing, China

*Corresponding author: liling@geiri.sgcc.com.cn

Abstract. Silicon Carbide is an excellent representative of the third-generation semiconductor materials, which can break the physical limit of silicon and achieve higher voltage of large power electronic devices. Such defects as dislocations and stacking faults in SiC epitaxial wafers have been shown to adversely affect SiC devices by introducing leakage paths and by reducing conductivity in the device drift region. This work discusses the effect of defects on the electrical properties and yields of SiC Schottky Barrier Diode. The diodes with voltage breakdown as 1200V were obtained and characterized. The phenomenon of the lowering of the Schottky barrier around the defect areas was analyzed.

1. Introduction

The advantages of using silicon carbide to fabricate power electronics devices were recognized several decades ago [1]. High power, low loss SiC devices can be widely used in electric power system, new energy vehicles, rail transit and so on. The fabrication of them requires large-size, low-defect, thick epitaxial silicon carbide wafers. Despite recent advances in SiC single crystal and epitaxy growth, the reduction of defects in large-scale thick epitaxy remains a big challenge. Those defects such as in-grow SF, carrot and triangular defects [2], down-fall, basal plane dislocations (BPD), screw dislocations and micropipes can affect the performance of SiC devices and reduce the yields of devices on one SiC wafer.

All kinds of defects that are generated during epitaxial growth cause considerable increase in leakage current and reduction of blocking voltage, and have a negative effect on the performance of SiC devices. These defects usually contain stacking faults in a basal plane or a prismatic plane, or contain a 3C-lamella. The density of these defects is typically 0.1~1 cm⁻², and tends to increase in thick epitaxial layers [3]. Lots of researches have shown that in-grow SF, carrot/triangular defects and down-fall can course Vθ reduction both in bipolar devices and in unipolar devices. BPD has less effect on Schottky barrier diodes (SBDs), but can increase the positive on resistance of MOSFETs because of majority carriers is reduced in forward bias. For bipolar junction transistor, (threading screw dislocation) TSD and (threading edge dislocation) TED result in a reduced of local carrier lifetime, while BPD causes bipolar degradation, which leads to an increase in on-resistance and leakage current.

In this work, the SiC SBDs were realized on 4H-SiC n-type wafers. Different kinds of defects such as down-fall, carrot/triangular, BPD, in-grow SF and so on have been characterized. The phenomena of barrier height inhomogeneity and the influence of the yields were studied.
2. Experimental details
SiC SBDs were fabricated using 4H-SiC wafers with a 12-μm thick lightly doped (9E15 cm⁻³) n-type epi-layer on Si-face. Figure 1 shows the schematic of the SBD structure. First, a thin film of silicon oxide was deposited and photolithography etched to form the mask of ion implantation. Then Al ions were injected into the epi-layer at 500°C to form the guard ring. A carbon film was made to protect the wafer surface in 1750°C anneal. After the carbon film was removed, silicon oxide was deposited and photolithography etched. Ohmic contact was made on the backside of the wafer. Then a titanium film was sputtered and annealed to form a Schottky barrier on the frontside of the wafer. Finally, a polyimide film was coated to protect the terminal of SBDs.

![Schottky Contact](image)

**Figure 1.** The schematic of the SBD structure.

The defects of the bare wafer were investigated by Candela CS920. I-V analysis was performed by Keysight B1505A.

3. Results and discussion
3.1. Defects' analysis
Defects mapping of the wafer which measured by Candela CS920 is shown in Figure 2. The colored dots showed the location of different defects. Pictures in Table 1 are optical images of the typical defects. Carrot and triangular defects can be clearly investigated through Topography and NUV-PL channels. Bar shaped stacking faults (BSF) can be observed through VIS-PL and NUV-PL channels.

![Defects mapping](image)

**Figure 2.** The defects mapping of the wafer.
Table 1. Optical images of the typical defects.

| Defect Type | Topography | VIS-PL | NUV-PL |
|-------------|------------|--------|--------|
| Carrot      |            |        |        |
| Triangle    |            |        |        |
| BSF         |            |        |        |

3.2. Electrical analysis

Schottky diodes were electrically characterized using Keysight B1505A. The forward I-V data were collected and the log($J$) versus $V_a$ curve was plotted. The inhomogeneity phenomenon can be found around the structural defects’ areas, as shown in Figure 3.

Figure 3. Forward J-V characteristic of the diodes.

The current density in forward bias $V_a$ is given by:

$$J = J_{sT} \exp \left( \frac{eV_a}{nkT} \right)$$

(1)

Where $n$ is the ideality factor, $J_{sT}$ the reverse saturation current density:

$$J_{sT} = A^* T^2 \exp \left( \frac{-e\phi_B}{kT} \right)$$

(2)

Where $A^*$ is the Richardson’s constant, $\phi_B$ the effective barrier height. The published value of $A^*$ in 4H-SiC is $145 \text{A/cm}^2\text{K}^2$ [4]. The ideality factor n is calculated from ln$J$ versus forward voltage drop $V_a$. 

The barrier height is calculated from $J_{ST}$ in Eq. (2):

$$
\phi_B = \frac{kT}{q} \ln \left( \frac{A^* T^2}{J_{ST}} \right)
$$
(4)

The barrier height can also be extracted from the $C-V$ curve: [5]

$$
\phi_B = V_I + \frac{kT}{q} \ln \left( \frac{N_{DM}}{N_C} \right) + \frac{kT}{q} - \Delta \phi_b
$$
(5)

$$
N_{DM} = \frac{2}{q \varepsilon_s} \left[ - \frac{d(1/C^2)}{dV} \right] A^2
$$
(6)

Where $N_C$ is the density of conduction band of SiC (4H-SiC is $1.7 \times 10^{19} \text{cm}^{-3}$) [6], $V_I$ is the voltage intercept of the $1/C^2$ voltage curve, and $A$ is the area of the diode.

A barrier height map was realized in Figure 4. A circle with a cross indicates that the potential barrier reduction of the device is due to the presence of a structural defect at that location. The number of these devices caused by defects of triangle, carrot, downfall and BSF has reached 37% of the total potential barrier reduction device. Other potential barrier reduction phenomenon maybe caused by other defects or process inhomogeneity. All the devices with barrier lowering phenomenon failed to pass the breakdown voltage and leakage current test, probably due to the enhanced tunneling current through the low-barrier-height region at high electric field [7]. Typical values of different defects on the wafer are shown in Table 2.

Figure 4. Barrier height maps of the wafer.
Table 2. Typical values of different defects on the wafer.

| Kinds of defect | $\Phi_B$ [eV] | $V_B$ |
|-----------------|---------------|-------|
| None            | 1.21          | 1450V |
| Triangle        | 0.86          | 30V   |
| Carrot          | 1.05          | 30V   |
| Downfall        | 1.09          | 30V   |
| BSF             | 0.97          | 30V   |

All failed devices were statistically analysed by defect type. The statistical chart is shown in Figure 5. Downfall and BSF are killer defects which cause 100% damage of the devices. Carrot and triangular defects cause partial failure of the device in the static test. But the rest non-failure devices with these defects may not pass the reliability tests.

4. Conclusions
Structural properties of different defects in the epilayer of 4H-SiC wafers were studied. 1200V SiC SBD were realized and characterized. The defects influenced the I-V characteristics of the SBDs. Some devices exhibit barrier lowering phenomenon which attributed to the structural defects. The SBDs that contain downfall and BSF exhibited 100% failure of the breakdown voltage and leakage current test while carrot and triangular defects cause 50%–80% failure of the static test. These structural defects seriously affect the yields of devices.

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