(i) Transient Response Test System Based on FPGA

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Abstract. A test system based on FPGA for second-order system transient response has been designed. The system uses the XC3S400 as the control core, and the VHDL hardware description language has been used to program FPGA to achieve the function of measuring the transient response parameters of the second-order system. The transient response waveform and the measurement result are displayed through VGA. The test results are within the error range, the overall index is good, and the curve storage and playback function are also implemented.

1. Introduction

In recent years, with the rapid development of electronic technology, people have put forward higher requirements for the performance of transient response test system in military, aerospace, testing and measurement fields. The traditional test method for transient response is inconvenient to use and obviously can not meet the needs of the development of modern technology.

In this paper, a transient response test system is designed. The core technology of the system is to generate a step signal by using the FPGA. After the second-order system, the response is collected and quantified by A/D, then the response is analyzed by the FPGA to calculate the peak time, overshoot, adjusting time and display by VGA. At the same time, the waveform can be stored and replayed. The features of this system are: fast measurement speed, high stability, error is less than 5%, perfect function, etc. It is an ideal transient response tester.

2. System composition and working principle

With XC3S400 as the control core, the system consists of DC signal source module, second-order system circuit, A/D conversion circuit, DC regulator power supply, keyboard and display, etc[1].The overall system diagram is shown in Figure 1.

![System overall diagram](image)

Figure 1. System overall diagram

The time required for the output response to exceed the first peak of the steady-state value is the peak time. The difference between the maximum peak of the output response of the second-order system and the steady-state value is overshoot. The time required for the output response value to be less than 2% of the steady-state value is the adjustment time.

In this system, programmable logic device (PGD) is used as the control and data processing core. DC signal source output 0.5V-1.5V step-adjustable (step size 0.1V) signal is generated and sent to the second-order system. Transient response signal is output to A/D module. A/D conversion control module is formed inside the GA to sample external A/D control. Various response parameters are calculated by software programming. Moreover, using the internal hierarchical memory structure of the GA, the storage of response curves can be easily achieved.
3. Hardware design

3.1. FPGA Core board design
The FPGA core board is responsible for data sending and analysis, which is the most critical part of the system. Considering the system resources and the price of the FPGA, the Spartan 3 Series XC3S400 chip of Xilinx Company is selected, which uses 40MHz active crystal oscillation to meet the high-speed design requirements [2-4].

Core board can only output 3.3V DC signal, so this system first uses the method of resistor voltage dividing to get 1.5V voltage, then uses dial switch to control different resistor connections in the resistance network to achieve the purpose of resistor voltage dividing, so that the output of signal source can be adjusted from 0.5V to 1.5V. Because there are more resistors in the circuit, step capacitance is produced, and capacitor charging and discharging delay the rise time of step signal. To eliminate the effect of step capacitance, we parallel the acceleration capacitance at both ends of the resistor to increase the rise time of step signal.

3.2. ADC circuit design
This system uses AD9224 of ADI company as A/D conversion chip to complete dual A/D sampling function. The reference voltage used in the design is an internal reference voltage, which shortens the pin between SENSE and REFCOM, where the voltage range is 0-4V. It has a sampling frequency of 40MHz, uses 12 bits, integrates a high-performance sample-hold amplifier and reference voltage source in the chip, has logic function to correct error output, accurately provides 12 bits output data at 40 Mbps sampling rate, and guarantees no code leakage in fully operational temperature range. The circuit diagram is shown in Figure 2.

3.3. Second-order system circuit design
The schematic diagram of the second-order system circuit is shown in Figure 3. This circuit is a common two-Thomas second-order filter circuit, A1 constitutes a lossy integrator, A2 constitutes an ideal integrator, A3 and A4 constitute a reverse amplifier.

Following is a complex frequency domain analysis of this second-order network. KCL is applied to the direction input endpoint M of A1:

\[
\frac{U_{\text{in}}}{R_1} + \frac{U_{\text{in}}(s)}{R_n} + \frac{U_1(s)}{C_1} + \frac{U_2(s)}{R_n} = 0
\]  

(1)
Figure 3. Second-order system circuit schematic

$U_3(s)$ can be got from the inverse of the ideal integral of $U_1(s)$:

$$\frac{U_3(s)R_s}{sRRC_s} = U_3(s)$$

$$U_3(s) = -U_{out}(s)$$

The above three equations are derived:

$$H(s) = \frac{U_{out}(s)}{U_{in}(s)} = \frac{R_s / R_s RcR_s C_2}{s^2 + s / R_s C_1 + R_s / R_s RcR_s C_2}$$

The second-order differential equation can be obtained by the inverse Laplace transformation of the transfer function, by substituting into the data we can get

$$U''_{out}(t) + 10U'_out + \frac{R_s}{1000}U_{out}(t) = \frac{R_s}{1000}U_{in}(t)$$

The standard form of transfer function for second-order networks is as follows:

$$H(s) = \frac{A\omega_d^2}{s^2 + 2\xi\omega_d s + \omega_d^2}$$

The second-order network parameters are obtained by comparing the formulas (4) and (6) with each other.

- **Natural frequency**:
  $$\omega_n = \frac{R_s}{\sqrt{R_s R_s RcR_s C_2}} = 10 \sqrt{\frac{R_s}{R_s}} \text{rad/s}$$

- **Damped oscillation frequency**:
  $$\omega_d = \omega_n \sqrt{1 - \xi^2}$$

- **Damping ratio**:
  $$\xi = \frac{1}{2C_sR_s} \sqrt{\frac{R_s R_s RcR_s C_2}{R_s}} = \frac{1}{2} \sqrt{\frac{R_s}{R_s}}$$

- **Magnification**:
  $$A = \frac{R_s}{R_s \sqrt{R_s R_s RcR_s C_2}} = 1$$
4. Software design
The software part mainly includes step signal generation, AD acquisition control, measurement function, storage and playback, VGA user interface implementation and so on [5-6].

Dial the switch to trigger the timer to start timing, A/D samples a point every 1ms, multiple points are sampled according to measurement and display requirements.

Peak measurement: Compare the points collected to find the maximum value, record the value $U_1$ and the corresponding sample point n when $U_1$ is the maximum value, then the peak time $t_p = n(\text{ms})$, the peak size is $U_1$.

Stability value measurement: Because the response curve fluctuates greatly and the single point error is large when the stability value is determined, when the stability value is determined, stability value $U_2$ is the average of last 20 points. The overshoot will be:

$$\sigma_p = U_1 - U_2$$ (11)

Adjustment time measurement: Use the method of reverse comparison, start from the last sample point value, reverse forward to compare the collected value with the stable value, when the value is greater than 102% of $U_2$ or less than 98% of $U_2$, record the number of sample points m, adjustment time is $t_s = m(\text{ms})$.

5. System debugging and testing
After completing the hardware and software design of the system, comprehensive debugging and testing are required. Through debugging, program code is continuously optimized, and problems in the program are corrected and modified in time, so that the performance of the system can be improved and the working state can be more stable. During the testing process, the parameters of the components in the circuit can be corrected to avoid the gap between the theoretical analysis and the actual state causing the system parameters not to meet the requirements.

At present, this system can realize that step signal passes through the second-order system, FPGA calculates the peak time, overshoot and peak time. Table 1, Table 2 and Table 3 are measurements of different R values measured by the system.

| Table 1. Measurement result of R=620KΩ. |
|--------------------------|-----------------|------------------|
| Parameters               | $t_p(s)$        | $\sigma_p(V)$    | $t_s(s)$        |
| 1                        | 0.1241          | 0.478            | 0.85            |
| 2                        | 0.1201          | 0.492            | 0.84            |
| 3                        | 0.1196          | 0.502            | 0.80            |
| 4                        | 0.1243          | 0.511            | 0.81            |
| Theoretical value        | 0.1216          | 0.525            | 0.820           |
| Average error            | 1.75%           | 1.95%            | 2.0%            |

| Table 2. Measurement result of R=300KΩ. |
|--------------------------|-----------------|------------------|
| Parameters               | $t_p(s)$        | $\sigma_p(V)$    | $t_s(s)$        |
| 1                        | 0.1660          | 0.429            | 0.86            |
| 2                        | 0.1750          | 0.413            | 0.85            |
| 3                        | 0.1608          | 0.414            | 0.89            |
| 4                        | 0.1890          | 0.432            | 0.90            |
Theoretical value 0.176 0.421 0.86
Average error 1.81% 1.87% 2.3%

Table 3. Measurement result of R=100KΩ.

| Parameters | $t_{p}(s)$ | $\sigma_p(V)$ | $t_s(s)$ |
|------------|------------|---------------|---------|
| 1          | 0.2790     | 0.260         | 0.910   |
| 2          | 0.2801     | 0.254         | 0.879   |
| 3          | 0.2737     | 0.256         | 0.877   |
| 4          | 0.2750     | 0.263         | 0.934   |
| Theoretical value | 0.2795     | 0.259         | 0.920   |
| Average error | 1.85%      | 1.97%         | 2.5%    |

From the above results, we can see that the response parameters of the second-order system designed by us can be measured accurately. This system can measure the response parameters of a certain range of resistance values under the condition of under-damping of the second-order system.

6. Conclusion
The overall scheme of second-order system transient response test is studied, which is composed of step signal generation module, second-order system module, A/D conversion module, signal analysis module and display module. In the design, the hardware description language is used to program the field programmer. Several modules, such as digital signal generation module and data storage module, are concentrated on a single chip, which greatly simplifies the design of peripheral hardware circuit, increases the stability and reliability of the system. At the same time, the measurement results of various parameters are displayed through VGA as well as the measurement results of various parameters are achieved. Storage and playback of waveforms are also achieved.

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