Introduction of deep impurity levels of S, Se, and Zn into Si wafers for high-temperature operation of a Si qubit

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To realize high-temperature operation of Si qubits, deep impurity levels with large confinement energy, which are hardly thermally excited, have been introduced into Si wafers. Group II-VI impurities S, Zn, and Se, which are known to form deep levels, were introduced into the Si substrates by ion implantation. These samples were analyzed for concentration-depth profiles, energy level depths, and absence of defects. To introduce deep impurities into the channel of Si transistors, the conditions to introduce the impurities were found so that the concentration-depth profiles have maximum values at less than 50 nm from the Si surface. Then, the formation of the deep levels and absence of defects were experimentally examined. By using the conditions to introduce deep impurities into Si wafer obtained from the experiments, single-electron transport at room temperature, high-temperature operation of qubit, and room-temperature quantum magnetic sensors are promising.
1. Introduction

Many studies on silicon qubit have been conducted worldwide due to their potential to be highly consistent with integrated circuit technology. Operation of silicon qubits has been reported at extremely low temperatures such as 0.1K.\textsuperscript{1)} If the operation temperature of qubit can be increased, it is expected to accelerate research and extend applications of the technology. The depth of deep impurity levels of S, Se, and Zn in silicon are 10 – 20 times larger than the room temperature energy (26 meV), and electrons trapped in the deep levels are hardly thermally excited. It would be possible to realize high-temperature operation of silicon qubit by introducing deep levels on purpose into silicon devices. Then, we are studying to realize qubit and quantum sensors utilizing deep impurity levels in silicon.

In a previous study, single-electron transport up to 300 K and electron spin resonance and qubit operation (Rabi oscillation) at 10 K in Al-N isoelectronic trap-introduced Si tunnel FETs\textsuperscript{2)} have been reported.\textsuperscript{3)} By introducing deep impurity levels into the channel of a tunnel FET, \textit{i.e.} a gated p-i-n structure, single electron transport through deep levels can be realized. Furthermore, spin blockades\textsuperscript{4)} via double quantum dot formed by two deep levels enables the readout of single electron spin states and the observation of electron spin resonance and Rabi oscillation of the spin qubit. In this previous study,\textsuperscript{5)} the deep impurity level of Al-N and the shallow acceptor level were presumed to compose the double quantum dot. The reason that the operation temperature of the qubit is limited to 10 K can be interpreted as the shallow levels are subject to thermal excitation. To increase the operation temperature of the qubit, it is necessary to realize double quantum dot structure that consists of two deep impurity levels. Thus, we focused on group II-VI elements that form deep impurity levels in silicon. In our previous study,\textsuperscript{6)} we introduced Be into Si wafers and confirmed the formation of impurity levels by photoluminescence, and conducted experiments to introduce Be into Si devices.

The II-VI group elements S, Se, and Zn have been introduced into Si by diffusion or ion implantation (I/I), and the formation of deep donors and acceptors have been reported by many groups.\textsuperscript{7)-17)} However, I/I and post-implantation annealing (PIA) conditions that realize concentration-depth profiles having maximum values at less than 50 nm from the Si wafer surface, which are compatible with Si CMOS technology, have not been reported. We have conducted this study, as in our previous work, for the purpose of introduction of deep impurity levels into a 50-nm-thick Si-on-insulator (SOI) layer and process integration into tunnel FET devices. In this study, we introduced S, Se, and Zn into Si substrates by I/I, investigated PIA conditions, and examined the formation of deep impurity levels and the
presence of defects. To distinguish deep impurity levels from defect levels in the study, it is preferable to suppress defect formation with the introduction of the impurities. Therefore, the formation of deep impurity levels and the presence of defects were examined by multiple analysis methods. We found fabrication conditions to introduce deep impurity levels into Si wafers without defect formation and realized a concentration depth profile with the highest impurity concentration at less than 50 nm from the wafer surface.

This paper relates to the presentation held at the International Conference on Solid State Devices and Materials (SSDM) 2022 and discusses the optimization of I/I and PIA conditions to form deep impurity levels in Si wafers by introducing S, Zn, and Se, confirmation of the formation of deep levels, and analysis of the presence of defects, in detail.

2. Experimental methods

Ion implantations (I/I) of $^{32}\text{S}$, $^{64}\text{Zn}$, and $^{80}\text{Se}$ into Si wafers were carried out and their concentration-depth profiles and the presence of defects were examined. Here, we used CZ P-doped (n-type) Si(100) wafers with a resistivity of 5 – 10 $\Omega\cdot$cm or B-doped (p-type) Si(100) with a resistivity of 10 – 20 $\Omega\cdot$cm. In the following, $^{32}\text{S}$, $^{64}\text{Zn}$, and $^{80}\text{Se}$ are denoted as S, Zn, and Se, respectively. The I/I energy and dose for S, Zn, and Se are 15 keV and $1\times10^{13}$ cm$^{-2}$, respectively. PIA was performed by flash lamp annealing (FLA) at a peak temperature of 1200°C for 1.5 to 20 msec. For these samples, concentration-depth profiles were measured by secondary ion mass spectrometry (SIMS). Then, the presence of defects was examined by cross-sectional TEM observation and photoluminescence (PL) measurements.

Subsequently, CC-DLTS (Constant Capacitance Deep Level Transient Spectroscopy) analysis was performed to observe the deep impurity levels of S, Zn, and Se. The fabrication process of planar Schottky diodes (500 µm diameter) for CC-DLTS analysis is as follows: First, S, Se, and Zn were introduced by I/I into Si wafers, respectively. The I/I energy and dose are 15 keV and $1\times10^{13}$ cm$^{-2}$, respectively. For S and Se I/I, n-type Si(100) wafers (5 – 10 $\Omega$cm) were used, and for Zn implantation, p-type Si(100) wafer (10 – 20 $\Omega$cm) was used. Next, PIA by FLA was performed at 1200°C for 3 msec for the S-implanted wafer and 1200°C for 1.5 msec for the Se and Zn-implanted wafers in N$_2$ gas. Next, metal electrodes were formed by sputtering and reactive ion etching to form Schottky barriers. Here, Al was used for the n-type Si wafers and Ti was used for the p-type Si wafer for the metal electrodes. Next, Al 300 nm was sputtered on the backsides of the wafers as electrodes. Finally, annealing was performed at 450°C for 30 min in 3% H$_2$/N$_2$ gas. CC-DLTS analysis of the Schottky diodes was performed with Phystech FT1030.
3. Results and discussion

3.1 Results

Fig. 1(a) presents the concentration-depth profiles of S obtained by SIMS analysis for Si(100) wafers with S I/I and PIA at a peak temperature of 1200°C for 3 to 20 msec, and with S and Zn I/I and PIA at 1200°C for 1.5 msec by FLA. S areal density obtained from the depth concentration profile of the as-implanted one (black line in Fig. 1(a)) is $1.1 \times 10^{13}$ cm$^{-2}$, which is consistent with the implantation dose $1 \times 10^{13}$ cm$^{-2}$. As shown in Fig. 1(a), the S areal density decreases with increasing FLA time compared to the as-implanted one: the S areal density is $1.6 \times 10^{12}$ cm$^{-2}$ at 3 msec (orange line in Fig. 1(a)) and $4.4 \times 10^{11}$ cm$^{-2}$ at 20 msec (purple line in Fig. 1(a)). This result suggests S desorption by FLA, and the longer the time of FLA, the larger the amount of S desorption. The wafer with both S and Zn I/I and 1.5 msec FLA has an S areal density of $1.4 \times 10^{12}$ cm$^{-2}$ (red line in Fig. 1(a)), comparable to that of 3 msec FLA. On the other hand, the value of the S concentration peak was $\approx 3 \times 10^{18}$ cm$^{-3}$ for the 1.5msec wafer with S and Zn I/I, which is higher than that of $\approx 1 \times 10^{18}$ cm$^{-3}$ at 3msec. The condition of FLA at 1200°C and 1.5 msec, which results in the closest profile to the Al-N concentration profile obtained in the Al-N implanted TFETs in the previous study, is mainly employed in the following experiments. Fig. 2(b) shows the concentration-depth profiles of S and Zn in the Si(100) wafer after S and Zn I/I (15keV, $1 \times 10^{13}$ cm$^{-2}$) and the FLA, and that of $^{80}$Se in the Si(100) wafer after $^{80}$Se I/I (15keV, $1 \times 10^{13}$ cm$^{-2}$) and the FLA. Here, the FLA was performed at 1200°C and 1.5 msec for the both wafers. The concentration-depth profiles of S, Zn, and Se in Fig. 2(b) are similar with a maximum concentration of $\approx 2$ to $3 \times 10^{18}$ cm$^{-3}$ at depths of less than 10nm. From these results, appropriate I/I and PIA condition for the introduction of S, Zn, and Se impurities into Si channels less than 50 nm thick was obtained.

Fig. 2 shows cross-sectional TEM images of (a) S and Zn implanted and (b) $^{80}$Se implanted Si(100) wafers. S, Zn, and Se I/I were conducted at 15 keV and $1 \times 10^{13}$ cm$^{-2}$, and FLA was conducted at 1200°C for 1.5 msec in the both wafers. The insets in Fig. 2(a) and (b) show magnified views of the respective TEM images. No apparent amorphization or defects such as \{311\} defects were observed in the S and Zn-implanted and Se-implanted wafers as shown in Fig. 2(a) and (b).

Fig.3 (a) – (c) present CC-DLTS spectra measured for the Schottky diodes with (a) S, (b) Se, and (c) Zn I/I, respectively. Here, n-type Si(100) wafers ($5 \sim 10 \Omega$cm) are used for S and Se implanted diodes, and p-type Si(100) wafer ($10 \sim 20 \Omega$cm) is used for Zn implanted diodes. S, Se, and Zn I/I were performed at 15 keV and $1 \times 10^{13}$ cm$^{-2}$ into the Si wafers. Then, FLA at
1200°C was conducted for 3 msec for S-implanted wafers and 1.5 msec for Se- and Zn-implanted wafers. Carrier densities at 300 K obtained by C-V measurements were $9 \times 10^{14}$ cm$^{-3}$, $1.1 \times 10^{15}$ cm$^{-3}$, and $1.7 \times 10^{15}$ cm$^{-3}$ for S, Se, and Zn implanted diodes, respectively. The spectra of the CC-DLTS signal (mV) at period widths $T_W = 19.2, 192$, and 1920 ms are shown in Fig. 3 (a) – (c). DLTS$^{19}$ is a method to measure the capacitance transient at constant voltage and is analyzed using an approximation under the condition that the trap density is less than the carrier density. On the other hand, CC-DLTS$^{20)-22)}$ is a method to measure voltage transients with constant capacitance and can be analyzed even if the trap concentration is larger than the carrier density. The concentration-depth profiles of S, Se, and Zn obtained by SIMS (Fig. 1) have maximum concentrations of about $1 \times 10^{18}$ cm$^{-3}$, which is larger than the carrier density value of $\sim 1 \times 10^{15}$ cm$^{-3}$. Therefore, the CC-DLTS method was used in this study. CC-DLTS spectra in Fig. 3 (a), (b), and (c) were measured with a constant bias capacitance of 15pF, a voltage pulse width of 0.1 msec, and pulse heights of (a) 3.5V, (b) and (c) 2.0V. CC-DLTS peaks E1 and E2 were observed for the S- and Se-implanted Schottky diodes in Fig. 3(a) and (b), and CC-DLTS peaks H1 and H2 were observed for the Zn-implanted diodes in Fig. 3(c). A tail seen on the low-temperature side in Fig. 3(a) is not discussed here, since it is presumed to originate from a shallow level.

Fig.3(d) – (f) present Arrhenius plots for the (d)S, (e)Se, and (f)Zn implanted Schottky diodes. In these figures, $\tau$ and $T$ represent the time constant of the thermal emission of electrons and temperature, respectively. These plots were obtained from CC-DLTS spectra obtained by the correlation function method$^{23)-26)}$. Deep double donor levels were observed at 0.25 eV (E1) and 0.50 eV (E2) for the S-implanted diode in Fig. 3(d), and at 0.23 eV (E1) and 0.46 eV (E2) for the Se-implanted diode in Fig. 3(e). For the Zn-implanted diode, deep double acceptor levels were observed at 0.26 eV (H1) and 0.62 eV (H2) in Fig. 3(f). From these results, the formation of deep impurity levels was confirmed for the Si wafers with the S, Se, and Zn I/I and FLA. In particular, no unexpected defect levels were observed for the Zn and Se-implanted Si wafers. The activation energies $E_C - E$ or $E - E_V$, carrier capture cross sections $\sigma_n$ or $\sigma_p$, and trap concentration $N_T$ for each level obtained from the Arrhenius plots in Fig. 3(d) – (f) are shown in Table. I.

Fig. 4 shows PL spectra from Si(100) wafers with (a) both Se and Zn I/I, and (b)Se I/I at 20 K. These wafers were subjected to S, Zn, and Se I/I at 15keV and $1 \times 10^{13}$ cm$^{-2}$, and PIA at 1200°C for 1.5 msec. The 1.132-eV, 1.093-eV, and 1.028-eV lines in Fig. 4 originated from the TA, TO, and TO+O$^f$ phonon of Si, respectively.$^{27}$ All peaks observed in Fig. 4 originated from Si only, and no other peaks were observed. Although emission lines due to S,$^{28,29}$
Zn,\(^{30-32}\) and Se\(^{33}\) were reported in some previous studies, they were not observed in Fig. 4. Differences of S, Zn, and Se introduction and PIA conditions may affect the results. Defects-related emission lines\(^{36,36}\) such as X-line (1.018eV)\(^{34}\) and W-line (1.040eV),\(^{35}\) which have been observed in ion-irradiated Si, were also not observed. These results from Fig. 1 – 4 confirm that the formation of deep impurity levels in the Si wafers was realized without the formation of unintended defect levels.

3.2 Discussion
We introduced S, Zn, and Se by I/I at 15 keV and \(1\times10^{13}\) cm\(^{-2}\) into Si(100) wafers and with PIA by the FLA, and confirmed the formation of deep impurity levels by CC-DLTS analysis (Fig.3), respectively. Furthermore, S, Zn, and Se were successfully introduced at a concentration of \(\sim1\times10^{19}\) cm\(^{-3}\) into the depth range of \(\sim10\) nm from the silicon surface (Fig. 2). The data in Fig. 1(a), Fig. 2(b), and Fig. 4(a) suggest that both S and Zn I/I does not interfere or change the concentration profiles or form new defects. From these results, we have clarified the conditions to introduce the deep impurity levels into Si devices compatible with Si CMOS technology. By the introduction of deep impurity levels into Si devices under the conditions of I/I and PIA obtained from this study, a high-temperature qubit could be realized. By introducing two deep impurity levels into a p-i-n structure in a Si device with the procedure obtained in this study, a spin state can be read out via spin blockade.\(^{31}\) By using this technique, high-temperature Si qubit and room-temperature quantum sensors devices would be realized. No defects were observed in the cross-sectional TEM (Fig. 2), PL analysis (Fig. 4) for the S/Zn and Se-implanted Si(100) wafers, and the CC-DLTS analysis for the Se and Zn-implanted Si diodes (Fig. 3(b) and (c)). These results suggest that deep levels of Se and Zn can be introduced into Si wafers without defects. In the Schottky diodes used in this study with a carrier concentration of \(\sim1\times10^{15}\) cm\(^{-3}\), the depth of impurities from the metal/Si interface that can be measured by the CC-DLTS method is about 200nm – 1\(\mu\)m. To realize the high-temperature operation of Si qubits and quantum sensor devices with deep impurity levels in the future, we plan to introduce the two deep impurity levels into tunnel FETs with 50 nm thick SOI layers. However, we have not examined by DLTS analysis the existence of defects or impurity complex levels such as S-Zn and Se-Zn in the range of 50 nm from the surface when two impurities, such as S and Zn or Se and Zn, are introduced. Hence, further investigation would be needed to examine this issue.
4. Conclusions

To form deep impurity levels in Si(100) wafers, we have introduced S, Zn, and Se by I/I and PIA was performed by FLA. By SIMS analysis, I/I and PIA conditions were found with a concentration maximum (~2 to 3×10^{18} \text{cm}^{-3}) at less than 10nm from the Si surface. Then, we confirmed the formation of deep donor and acceptor levels of S, Se, and Zn in Si wafers by CC-DLTS analysis. No defects were observed for Zn and Se-implanted Si(100) wafers in the DLTS analysis of the high sensitivity. In addition, no defects were observed in S/Zn and Se-implanted Si (100) wafers by TEM observation and PL analysis. From these results, we have successfully obtained the conditions to introduce deep impurity levels of S, Zn, and Se into Si wafers such as SOI wafers with thin Si layers (~50 nm). By introducing S, Zn, and Se into tunnel FETs with the conditions found in this study, high-temperature operation of Si qubit, and room-temperature quantum magnetic sensors can be realized in the future.

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Fig. 1. S depth profiles measured by SIMS of S- and S/Zn-implanted Si(100) substrates at different post-implantation annealing (PIA) times. PIA was performed by flash lamp annealing (FLA) at 1200°C for a range of 1.5 msec to 20 msec. (b) S, Zn, and Se depth profiles measured by SIMS of S/Zn- and Se-implanted Si(100) substrates annealed by FLA at 1200°C for 1.5 msec. S, Zn, and Se ion implantations were conducted with the energy and dose of 15 keV and $1 \times 10^{13}$ cm$^{-2}$, respectively.
Fig. 2. Cross-sectional TEM pictures of (a) S/Zn and (b) Se-implanted Si (100) substrates at a PIA condition of 1200 °C for 1.5 msec. S, Zn, and Se ion implantations (I/I) were conducted with the energy and dose of 15 keV and $1 \times 10^{13}$ cm$^{-2}$. 
Fig. 3. CC-DLTS spectra of (a) S-, (b) Se-implanted n-type, and (c) Zn-implanted p-type Si Schottky diodes with rate windows of 19.2, 192, and 1920 msec. Arrhenius plots obtained from CC-DLTS measurements in (d) S, (e) Se implanted n-type, and (f) Zn implanted p-type Si (100) substrates. S, Se, and Zn ion implantations (I/I) were conducted with the energy and dose of 15 keV and $1 \times 10^{13}$ cm$^{-2}$. PIA condition for S-implanted sample is 1200°C for 3 msec, and Se- and Zn-implanted samples is 1200°C for 1.5 msec by FLA.
Fig. 4. Photoluminescence spectra from (a) S/Zn and (b) Se-implanted Si (100) substrates at a PIA condition of 1200 °C for 1.5 msec. S, Zn, and Se ion implantations (I/I) were conducted with the energy and dose of 15 keV and $1 \times 10^{13}$ cm$^{-2}$. 
Table I. CC-DLTS analysis results for S-, Se-implanted n-type and (c) Zn-implanted p-type Si (100) samples obtained from the data of Fig. 3.

| Samples                  | Levels | $E_C$ - $E$ or $E$ - $E_V$ (eV) | $\sigma_n$ or $\sigma_p$ (cm$^2$) | $N_T$ (cm$^{-3}$) |
|-------------------------|--------|---------------------------------|-----------------------------------|-------------------|
| S-implanted n-type Si   | E1     | 0.25                            | $3\times10^{-18}$                 | $4.3\times10^{13}$ |
|                         | E2     | 0.50                            | $4\times10^{-16}$                 | $2.3\times10^{13}$ |
| Se-implanted n-type Si  | E1     | 0.23                            | $5\times10^{-18}$                 | $5.1\times10^{14}$ |
|                         | E2     | 0.46                            | $5\times10^{-17}$                 | $7.0\times10^{14}$ |
| Zn-implanted p-type Si  | H1     | 0.27                            | $8\times10^{-15}$                 | $7.7\times10^{13}$ |
|                         | H2     | 0.62                            | $2\times10^{-14}$                 | $2.6\times10^{13}$ |