Organic field-effect transistors with low-temperature curable high-k hybrid gate dielectrics

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Abstract

We report a low-voltage-operated organic field-effect transistor that uses a hybrid gate insulator that has a high dielectric constant $k$. The gate insulator consists of a high-k polymer cyanoethylated pullulan (CEP) that can be efficiently cross-linked by glycidoxypropyltrimethoxysilane (GOPTMS) at low temperature ($\sim$110 °C). The very low curing temperature is below the glass transition temperature $T_g$ of conventional plastic substrates for plastic electronics, and is therefore compatible with many plastic substrates for plastic electronics. The cross-linking is very efficient in that only 1/10 (w:w) GOPTMS: CEP produced densely cross-linked thin films with a smooth surface, good insulating property, high capacitance density and high $k$. The devices functioned at low voltage, and exhibited charge carrier mobility $\sim$1.83 cm$^2$ V$^{-1}$ s$^{-1}$, and steep subthreshold swing $\sim$88 mV Dec$^{-1}$. These results imply that high quality polymer gate insulators are achievable at low temperature with a very small fraction of blended crosslinking agents; this characteristic offers a method to achieve portable all-plastic flexible electronics that function at low voltage.

Introduction

Organic field-effect transistors (OFETs) have the potential application in realizing economical, lightweight, mechanically flexible electronics [1–7]. The charge-carrier mobility $\mu$ of semiconducting molecules and polymers have been improved to $> 1$ cm$^2$ V$^{-1}$ s$^{-1}$. However, realization of all-organic electronics that function at low temperature requires development of a gate insulator with high dielectric constant $k$ and low processing temperature.

The gate insulator is one of the most critical components in OFETs, and its dielectric and surface properties have important influences on electrical properties. In low-cost and flexible considerations, several polymeric materials have been investigated for use as dielectric layers; these materials include Poly(methyl methacrylate) (PMMA) [8], polyvinyl phenol (PVP) [9], polystyrene (PS) [10] and polyvinyl alcohol (PVA) [11]. However, most of these materials have a low dielectric constant $k$, so OFETs that use them require a relatively high operating voltage. To reduce the operating voltage and power consumption, high-k dielectrics are required. PVDF [12] and its copolymers have high $k$, but have the disadvantages of severe hysteresis behavior and a rough dielectric surface, so they are usually used only for nonvolatile memory applications [13]. Synthesis approaches have also been demonstrated for high-k dielectric materials [14–18]. Another option is to use cyanyl-substituted natural polymers, such as cyanoethylated pullulan, which is suitable for scalable production at low cost. However, they suffer from high electrical leakage and are not suitable for dielectric applications [19]. This problem was solved by chemically cross-linking cyanoethylatedpullulan (CEP); this process suppressed electrical leakage by reducing the free volume in polymeric films [20], so this class of materials provide good candidates for high-k dielectrics. However, these cross-linking processes require relatively high reaction
temperature (∼200 °C) [21], which exceeds the glass transition temperatures \( T_g \) of conventional plastic substrates such as polyethylene terephthalate (PET) \( (T_g \sim 78 \, ^\circ C) \) and polyethylene naphthalate (PEN) \( (T_g \sim 121 \, ^\circ C) \). Although some low-temperature (110 °C) cross-linked gate insulators have been proposed, they are all low-\( k \) materials [22–29]. Our recent attempt using trimethylolpropane triglycidyl ether (TTE) as a cross-linking agent reduced the curing temperature [30]. However, when used in dielectric thin films, it suffers from an excess OH groups, which are usually regarded as the origin of charge traps that result in electrical leakage and hysteresis behaviors and thus degrade the device performance. To eliminate these problems, further efforts to develop novel cross-linking systems are required.

In this paper, we report the fabrication of a high-\( k \) hybrid polymer gate insulator by low-temperature curing of a blended thin film of CEP polymer and an efficient cross-linking agent, glycidoxypropyl trimethoxysilane (GOPTMS). We also studied the surface and insulating properties of the cross-linked thin films (CEPGOP). We fabricated OFETs that had CEPGOP dielectrics to evaluate its feasibility for use in organic electronics.

### Experimental

Top-contact bottom-gate OFETs were fabricated (figure 1). The cross-linkable solutions were prepared in a co-solvent (N, N-dimethylformamide: acetonitrile 1 : 1 v:v) with 5 wt% CEP (Mw ∼489,000, Shin Etsu Chemical Co.) and 0.5 wt% GOPTMS. The solutions were spin-coated onto cleaned p-type (for Fourier transform infrared (FT-IR) and metal-insulator-semiconductor (MIS) capacitors) or heavily-doped n-type silicon wafer (n + Si, for OFETs), which were then baked in a vacuum oven for 1 h at 110 °C. A 60 nm-thick pentacene active layer (Aldrich, without purification) was then vacuum-deposited at a rate of 0.2–0.3 Å s\(^{-1}\). For MIS capacitors, Au top electrodes were evaporated through a shadow mask to form a circular dot with an area of 8.02 × 10\(^{-4}\) cm\(^2\). For OFETs, gold source/drain electrodes were deposited through a shadow mask with a channel length \( L = 150 \, \mu m \) and width \( W = 1500 \, \mu m \) (figure S1 (available online at stacks.iop.org/MRX/9/076301/mmedia)). Scanning electron microscopy (SEM) was used to capture the cross-sectional image to estimate the dielectric film thickness. FT-IR spectra of solid films were recorded using a Nicolet700 in transmission mode. Atomic Force Microscopy (AFM) images were obtained using a Dimension\(^{TM}\) 3100 microscope (Digital Instruments). Capacitance density–voltage (\( C–V \)) characteristics of MIS capacitors were obtained using a HP 4284 A Precision LCR meter (Agilent Tech.) to evaluate the dielectric constant and its dependence on frequency. Electrical characteristics of the OFETs were measured using a Keithley 4200 semiconductor analyzer in an N\(_2\) atmosphere.

![Figure 1. Schematic of the top-contact field-effect transistor and chemical structure of CEP, GOPTMS and CEPGOP.](image-url)
Results and discussion

Thin film properties
FT-IR spectra of the dielectrics
FT-IR spectra (figure 2) were recorded in transmission mode to monitor the chemical changes in the dielectric thin film. At high wave numbers, the band centered at 3450 cm\(^{-1}\) is assigned to the OH groups in the unsubstituted position in CEP polymer. The quantity of OH functional groups was suppressed after baking; this change implies that the chemical reactions proceeded as indicated in figure 1. At low wave numbers, the band centered at 1027 cm\(^{-1}\) is assigned to Si–O–C and the band centered at 913 cm\(^{-1}\) is assigned to cyclic ether. The reduction in the intensity of Si–O–C and cyclic ether signals (reduction in number of groups) further confirmed the occurrence of the cross-linking reaction.

SEM of the dielectrics
Cross-sectional image (figure S2) was captured by using scanning emission microscope (SEM). According to the cross-sectional view, the dielectric thin film thickness was 370 nm.

AFM images of dielectric surface and pentacene layers
Stacking of semiconducting molecules is strongly dependent on interfacial properties, so the morphology of bare dielectric surfaces were captured using AFM to investigate the possible influence of the dielectric surface (figure 3(a)). The dielectric surface was very smooth with a root-mean-square roughness ~0.2 nm. The very smooth dielectric surface may have negligible effect on the pentacene deposition mode.

Most charge transport occurs within the first few layers of semiconducting molecules near the dielectric/semiconductor interface, and is significantly influenced by the stacking manner of semiconducting molecules in this region. To investigate the micro-structure of initial molecule layers, an AFM image of 2 nm thick pentacene film was captured (figure 3(b)). The initial layer of pentacene molecules covered most of the dielectric surface with very small portion of voids. Furthermore, in the cross-sectional view (figure 3(c)), the clear vertical thickness of each layer was ~1.5 nm, which is approximately the length of a pentacene molecule. These observations suggest that pentacene in thin-film mode grows vertically in two dimensions; this growth pattern of pentacene on dielectrics ensures \(\pi-\pi\) conjugative stacking along the channel and thus facilitates charge transport in the device. Correspondingly, AFM images of a 60 nm-thick pentacene layer exhibited large grains with dendritic microstructures (figure 3(d)).
Metal-insulator-semiconductor (MIS) capacitors

Capacitance-voltage curves
Al/CEGOP/p-Si MIS capacitors were fabricated to study the dependence of capacitance $C_i$ on bias voltage $V$ and frequency $f$. The $C_i$ - $V$ characteristics at $f = 1$ MHz exhibited clear accumulation, depletion and saturation regions (figure 4(a)). The maximum capacitance density was $\sim 36.3$ nF cm$^{-2}$. Accordingly, $k$ value was calculated to be 15.2, which could be an effective value under device operation.

Organic field-effect transistors
Top-contact bottom-gated OFETs with CEGOP as a gate insulator were fabricated to study the electrical characteristics (figure 5). Transfer curves were measured at driving voltages of $-3$ V (figure 5(a)). Field-effect
mobility $\mu$ was extracted from the saturation regime as

$$I_D = \frac{W}{2L} C_i (V_G - V_T)^2,$$

where $I_D$ [A] is the drain current in the saturated regime, $W$ [cm] is channel width and $L$ [cm] is channel length, $C_i$ [F m$^{-2}$] is the gate dielectric capacitance per unit area, $V_G$ [V] is the gate voltage, and $V_T$ [V] is the threshold voltage. Devices driven at $V_D = -3$ V exhibited good performance with the best $\mu$ as high as 1.83 cm$^2$ V$^{-1}$ s$^{-1}$ and a steep SS of 0.088 V dec$^{-1}$. The average values of $\mu$ and SS are 1.73 cm$^2$ V$^{-1}$ s$^{-1}$ and SS = 0.095 V dec$^{-1}$, respectively (table S1). The high $\mu$ might result from facilitated charge transport along the channel direction due to the vertically-aligned and densely stacked pentacene molecules in the first few layers near the semiconductor/dielectric interface, and to the overlapped $\pi$-$\pi$ conjugation along the surface plane. The mobility is analogous to other top-contact pentacene field-effect transistors [31–33]. The steep SS is one of the lowest so far, and approaches the theoretical minimum of $\sim$0.059 V dec$^{-1}$. The steep SS is consistent with other reports using high-k polymer gate dielectrics [34].

Driving voltage affected the output curves (figure 5(b)). The devices functioned successfully at a relatively low voltages. The high output current driven by the low voltage would be very useful in portable electronics that usually have a relatively low-voltage power supply.

**Estimation of trap states**

Remnant functional groups and impurities can form charge traps. The upper limit $N_{trap}^{\text{Max}}$ of trap density can be estimated as

$$N_{trap}^{\text{Max}} = \left[ \frac{qS \log(e)}{k' T} \right] - 1, \frac{C_i}{q}$$

where $q$ [1.65 × 10$^{-19}$ C] is the charge on an electron, $S$ is the reciprocal [dec V$^{-1}$] of SS, $k'$ [1.38 × 10$^{-23}$ J K$^{-1}$] is Boltzmann’s constant, $T$ [K] is absolute temperature, and $C_i$ [F m$^{-2}$] is the capacitance of the gate dielectric.
per unit area. A sharp SS yields low densities of charge traps inside and on the surface of the gate insulator. Charge trap density was calculated to be $1.09 \times 10^{11}$.

From the data, we conclude that the trap states have been significantly eliminated. These results show the superiority of the cross-linking system for gate insulator applications.

Conclusion

Organic field-effect transistors were fabricated with a low-temperature curable high-$k$ gate dielectric using a high-$k$ CEP polymer as matrix and GOPTMS as an efficient cross-linking agent. The devices functioned successfully at low voltage. These characteristics are benefits of the high capacitance density ($36.3$ nF cm$^{-2}$) of the gate insulator. The devices exhibited the best mobility $\sim 1.83$ cm$^2$ V$^{-1}$ s$^{-1}$. Curing is achieved at $\sim 110$ °C, which is compatible with most flexible substrates; therefore this insulator has great potential for use in fabrication of plastic electronics.

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Data availability statement

The data generated and/or analysed during the current study are not publicly available for legal/ethical reasons but are available from the corresponding author on reasonable request.

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