Opening the Doors to Dynamic Camouflaging: Harnessing the Power of Polymorphic Devices

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Abstract—Hardware-centric security threats have emerged in every stage of the IC supply chain. Prior defenses have been developed to protect against intellectual property (IP) piracy at different stages. However, so far only logic locking can protect the IP end to end. We present dynamic camouflaging to thwart IP reverse engineering at all stages in the supply chain. We exploit the multi-functionality, post-fabrication reconfigurability, and run-time polymorphism of spin-based devices, specifically the magneto-electric spin-orbit (MESO) device. Leveraging these properties, dynamic camouflaging is resilient to state-of-the-art attacks such as SAT, approximate SAT (AppSAT) and HackTest, and can further impede side-channel analysis. For MESO-based full-chip dynamic camouflaging we anticipate massive improvements in power (7,400×), performance (5.9×), and area (73×) over spin- and CMOS-based camouflaging. We outline the prospects of dynamic camouflaging for error-tolerant image processing applications.

I. INTRODUCTION

GLOBALIZATION of the electronics industry has resulted in the outsourcing of the integrated circuit (IC) supply chain. Such a distributed supply chain enables intellectual property (IP) piracy, illegal overproduction of ICs and insertion of malicious circuits called hardware Trojans [1]. IP piracy, in particular, is multi-faceted and an attacker has different avenues to mount such an attack, ranging from an untrustworthy foundry, an untrustworthy test facility to malicious end-users. While an untrusted foundry or end-user could pirate the design by reverse engineering (RE) and/or mounting Boolean satisfiability (SAT) attacks [2], [3], an adversary in the test facility can misuse test patterns to compromise the security of a chip [4]–[6]. Various schemes have been proposed to counter IP piracy:

1) Camouflaging the layout and the devices makes the circuit implementation indistinguishable across several functions (e.g., using dummy contacts [7], threshold-voltage-dependent cells [8], AND-tree camouflaging [9]),
2) Split manufacturing fabricates the front-end-of-line (FEOL) and back-end-of-line (BEOL) parts of a chip in different foundries. This avoids the dissemination of the full layout to one untrustworthy foundry (e.g., split manufacturing for RF designs [10]),
3) Logic locking uses additional gates to obfuscate the functionality at the netlist level (e.g., Anti-SAT [11] and stripped-functionality logic locking [12]).

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TABLE I

| Technique          | Foundry | Test Facility | End-User |
|--------------------|---------|---------------|----------|
| Camouflaging       | ☑       | ☐             | ☑        |
| Split Manufacturing | ☑       | ☑             | ☐        |
| Logic Locking      | ☑       | ☑             | ☑        |
| Dynamic Camouflaging | ☑   | ☑             | ☑        |

Only logic locking protects the IC supply chain end to end. Even for logic locking, the resilience depends on a tamper-proof memory to store the secret key. Realizing such memories is an area of active research [13].

Emerging spin devices like the magneto-electric spin-orbit logic (MESO) [14] and the charge-spin logic [15] are prime candidates for augmenting hardware security [16], [17]. This is due to their innate run-time polymorphism and post-fabrication reconfigurability. Recent research [18], [19] has used polymorphic devices for static camouflaging. However, the true potential of polymorphic devices lies in dynamic camouflaging, which is unexplored and is the focus of this paper.

Dynamic camouflaging involves switching and obfuscating the device-level functionality post-fabrication, as well as during run-time. We study dynamic camouflaging using polymorphic spin devices, and establish security and computational accuracy as two entangled design variables, especially for error-tolerant applications such as image processing. For such applications, dynamic camouflaging can thwart exact [2] and approximate SAT (AppSAT) attacks [3]. Further, we discuss securing the supply chain end to end using spin-based devices, and circumventing the risks associated with untrusted foundries, test facilities, and end-users (see Fig. 1 and Table I).

A. Background and Motivation

Dynamic camouflaging builds on the foundations of polymorphic computing [20], a subset of reconfigurable computing. Reconfigurable computing using programmable devices such as FPGAs fix the logic functionality of the chip before run-time. In polymorphic computing, the devices are reconfigured in time and space during run-time. Dynamic camouflaging dynamically obfuscates the circuit at the device level. Individual gates are configured correctly only after fabrication and test and can switch between different functionalities at run-time. Contrary to static camouflaging [7]–[9], dynamic camouflaging requires polymorphic logic gates.
Prior work using programmable CMOS for IP protection leverage reconfigurable logic barriers [21] and reconfigurable key gates [22]. These techniques do not use polymorphism and fix the key bits. Randomly-triggered dynamic key obfuscation has been proposed in [23]. This scheme requires additional circuitry to alter the key, which is potentially prone to removal attacks. Another study leverages hot-carrier injection (HCI) to program threshold-voltage-based CMOS gates after fabrication [24]. However, they do not support runtime reconfiguration and suffer from large PPA overheads.

Run-time polymorphism (and hence dynamic camouflaging) is difficult to implement in CMOS owing to fundamental limits of CMOS devices. Our scheme enables a radically different solution, wherein we use the unique properties of spin devices to achieve truly polymorphic chips. This is particularly useful for error-tolerant applications such as image processing [25]. We argue that dynamic camouflaging is also promising for approximate computing, as dynamic camouflaging introduces errors inherently (See Sec. III-E).

The contributions of this work are four-fold:

1) Develop dynamic camouflaging using the inherent functional polymorphism of spin devices;
2) Counter IP piracy across the IC supply chain (untrusted foundry, test facility, and end-user). We demonstrate resilience to state-of-the-art SAT and test attacks and discuss the implications of side-channel attacks;
3) Show the benefits of dynamic camouflaging in error-tolerant applications such as image processing;
4) Summarize the superior layout-level cost in terms of power, performance, and area (PPA) of the approach in contrast to other spin-based camouflaging schemes.

II. DYNAMIC CAMOUFFAGING: WORKING PRINCIPLE

The spin device considered in this study is the magneto-electric spin-orbit (MESO) device, whose operation is based on the phenomena of magneto-electric (ME) switching [26] and inverse spin-orbit effects [27]. The schematic of the MESO device implementing different Boolean functions is shown in Fig. 2. The inputs/outputs are electric currents and the logical information is encoded as the direction of the current flow. A detailed description can be found in [14].

During the writing phase, an input electric current flowing in the \( \pm \hat{y} \) direction through the non-magnetic interconnect sets up an electric field in the \( \pm \hat{z} \) direction within the ME capacitor (red in Fig. 2). The resulting ME field switches the magnetization state of the ferromagnet (purple) along the \( \pm \hat{z} \) direction. Information is written into the MESO device by transducing the input electric current into the magnetization state of the device. After the writing process is complete (which takes \( \sim 200 \text{ ps} \)), the supply voltages \( V^+ \) and \( V^- \) are turned on to initiate the reading phase.

In the reading phase, a spin-polarized current is injected into the spin-orbit coupling layer, which converts the spin current into electrical current at the output node \( (I_{\text{out}}) \), due to the inverse spin-Hall and Rashba-Edelstein effects [28]. The direction of the output current is determined by the polarity of the supply voltages \( V^+/V^- \) applied on the nanomagnet, and the magnetization state of the nanomagnet.

By switching the polarity of the supply voltages, we can implement a buffer (BUF) or an inverter (INV) using the same device (Fig. 2(a,b)). Further, we can implement complex gates such as majority logic, by leveraging the additive nature of the input signals. As shown in Fig. 2(c,d), \( A \) and \( B \) are the inputs and \( X \) is the tie-breaking control input. The polarity of \( X \) decides the mode of operation of the MESO gate. Here,
XOR and XNOR gates, the tie-breaking input polarities of the supply voltages are flipped (Fig. 2(e,f)). For realizes an OR gate. To implement NAND and NOR gates, the control signal uration between AND/OR and NAND/NOR, on flipping the input and control signals can either be derived from a control block or from a true random number generator (TRNG). A and B are the inputs, S is sum, D is difference, Ca is carry, and Bo is borrow. Dummy contacts are omitted for simplicity.

for \( X = -I \), it realizes an AND gate and for \( X = +I \), it realizes an OR gate. To implement NAND and NOR gates, the polarities of the supply voltages are flipped (Fig. 2(e,f)). For XOR and XNOR gates, the tie-breaking input \( X \) is eliminated, and one signal is provided at the input terminal. The other input signal is encoded in the voltage domain and applied directly at the \( V^+/V^- \) terminals (Fig. 2(g,h)).

The MESO device with peripheral circuitry is shown in Fig. 2(i). A timing diagram showing the functional reconfiguration between AND/OR and NAND/NOR, on flipping the control signal \( X \), is shown in Fig. 3(a). The key bits deciding the input and control signals can either be derived from a control block or from a true random number generator (TRNG) (Fig. 3(b)), if random reconfiguration is applicable, e.g., for error-tolerant applications. Configuring the MESO device via different supply voltages and electric currents allows us to dynamically implement all basic Boolean gates at run-time within a single structure.

III. Security Analysis

A. Threat model

An adversary seeks to decipher the design IP and has various opportunities to launch attacks. We assume that the foundry, the test facility, and the end-user are all untrustworthy (Fig. 1).

(1) A malevolent employee in the foundry has access to the design, including material and layout parameters of the MESO gates and the chip interconnects. Prior camouflaging schemes have trusted the foundry to implement their device/circuit-level obfuscation, while we do not require a trusted foundry for our scheme. Defending against an untrusted foundry is an achievement by itself.

(2) An untrusted test facility has all test patterns and corresponding responses. Test patterns can compromise logic locking and static camouflaging because they are generated to maximize fault coverage and this inherently exposes internal circuit details [4]–[6].

(3) An untrusted end-user has the know-how to RE a chip. He/she can mount analytical attacks such as [2], [3] to decipher the IP obtained from RE. Further, he/she can apply side-channel attacks [29]. Consistent with the prior art, he/she cannot invasively probe. Hence, probing individual wires or MESO gates is not possible.1

We assess the security guarantees offered by dynamic camouflaging by evaluating all these threat scenarios. We then present a case study of dynamic camouflaging for approximate computing, wherein we demonstrate the inherent trade-off between accuracy and resilience against RE attacks.

B. Untrusted foundry

The design house can either provide a fully-camouflaged layout composed of MESO devices or a camouflaged layout, where selected CMOS gates are replaced by MESO gates.2 The proportion of the design that is camouflaged by a designer depends on the scope of application and impact on PPA overheads. An attacker in the foundry can RE the IP implemented in CMOS whereas the MESO gates appear as black boxes without any fixed functionality. While a foundry-based adversary can readily obtain the dimensions and material composition of the nanomagnet in each MESO gate (and hence understand its magnetic properties including saturation magnetization, energy barrier, and critical ME field for switching), these design details do not leak any information about the intended function of the gate. This is because MESO gates are configured post-fabrication. In contrast, CMOS gates have a fixed function once fabricated (static camouflaging). Recently, attacks exploiting an untrusted foundry have been proposed [32], [33], where no activated working chip is leveraged as an oracle; this contrasts with SAT attacks which require a working oracle. Having no access to the attacks [32], [33], we refrain from a comprehensive study, but since our approach relies on post-fabrication reconfigurability, it is intuitive to note that our scheme is resilient to such attacks. Assuming the end-user is also untrusted, besides dynamic camouflaging, one can also apply large-scale static camouflaging to thwart analytical SAT attacks [18], [34], [35].

C. Untrusted test facility

An attacker in a test facility, with access to the test patterns and responses (generated and supplied by the design house),

1Shielding can be applied as an additional measure [30].
2Hybrid spin-CMOS designs have been realized in prior works [31].

![Fig. 4. Dynamic reconfiguration of gate X4 in a representative circuit. Circuit implementing \( f_1 \) is the original template and \( f_2, f_3 \) are the morphed versions.](image-url)
TABLE II
STATISTICS OF BENCHMARKS. THE ATTACK SUCCESS RATE OF HackTest IS REPORTED AS THE PERCENTAGE OF KEY BITS INFERRED BY THE ATTACK FOR STATIC AND DYNAMIC CAMOUFLAGING. TEST PATTERNS ARE GENERATED BY Tetramax ATPG FOR 100% FAULT COVERAGE.

| Benchmark | Original | [7] | [17] | [36] | [8], Proposed |
|-----------|----------|-----|------|------|--------------|
|           | Test Patterns | Inputs | Outputs | Gates | Camouflaged Gates | Static | Dynamic | Static | Dynamic | Static | Dynamic | Static | Dynamic |
| h14       | 469       | 275   | 245   | 4,125 | 350           | 59.21  | 17.06   | 38.56  | 16.08   | 18.45  | 7.92    | 28.92  | 17.56   |
| b15_1     | 811       | 485   | 449   | 6,978 | 350           | 20.26  | 4.65    | 20.32  | 3.38    | 15.21  | 0.71    | 15.34  | 2.55    |
| b20       | 896       | 522   | 512   | 9,226 | 350           | 56.43  | 15.36   | 40.80  | 12.10   | 20.86  | 4.39    | 20.19  | 11.63   |
| b22       | 1,355     | 767   | 757   | 14,457| 350           | 55.81  | 16.17   | 63.03  | 10.92   | 21.62  | 4.25    | 34.23  | 8.63    |
| Average   | N/A       | N/A   | N/A   | N/A   | N/A           | 47.92  | 13.31   | 40.15  | 11.12   | 19.04  | 4.32    | 24.07  | 10.09   |

can jeopardize the IP security, thwarting logic locking and IC camouflaging. ATPG algorithms are designed to maximize the fault coverage with minimum test data and in doing so, these test patterns leak the internal circuit structure [4]–[6].

In logic locking where pre-test activation is performed (i.e., test patterns are generated with the correct key), such an approach is vulnerable to hill-climbing [4] and test-data mining attacks [5]. For static camouflaging, the functionality of logic gates cannot be configured post-fabrication and hence test patterns are always generated for the correct assignment of camouflaged gates. This vulnerability is leveraged in HackTest to reveal the identity of camouflaged gates within minutes [6].

MESO-based dynamic camouflaging circumvents this threat by allowing post-test configuration. The fabricated IC is configured with an incorrect I/O mapping and functionality. This is equivalent to loading a locked IC with an incorrect key. The reconfigured IC and test data are then send to the test facility. An attacker ends up with an incorrect IP by mounting the test data mining attack on the IC. After testing, before being deployed in the market, the MESO gates are reconfigured (by the design house) to reflect the true, intended functionality.

Even if the chips are configured prior to test, dynamic camouflaging provides superior resilience compared to static camouflaging. To model an adversary in the test facility, we implement HackTest [6], with identical setup details. We camouflage a fixed set of gates (64/128 gates were camouflaged in [6]) using various camouflaging schemes and execute the attacks for static and dynamic camouflaging for 72 hours. Each experiment is repeated 10 times and the findings are reported in Table II. We observe that (i) as the number of functions that a camouflaged gate can implement increases, there is a reduction in the attack success rate, and (ii) the attack success rate for dynamic camouflaging is lower when compared to static camouflage.

For larger HIC-99 benchmarks like b17_1, b18, and b19, the attack success rate is close to 0% (for both cases). The attack success rate is related to (i) size of the benchmark, (ii) number and type of camouflaged gates, and (iii) number of functions implemented by a camouflaged gate.

D. Untrusted end-user

A hostile end-user with sophisticated RE equipment, SAT algorithms, and computational resources may circumvent the IP protection employed by a design house. However, dynamic camouflaging has the potential to thwart such an attacker right in his/her tracks. We illustrate dynamic camouflaging through a conceptual example; consider the circuit implementing a majority-of-inputs (majority-of-inputs) in Fig. 4. Initially, the circuit is configured with gate X4 performing a NAND operation. Subsequently, X4 morphs into NOR and then into XNOR. Here, X4 is the sole camouflaged (and polymorphic) gate with three key bits determining its function. Assuming a key distribution such that INV, BUF, AND, OR, NAND, NOR, XOR, and XNOR gates correspond to key bits {000, 001, ..., 111} respectively, the dynamic key of the circuit cycles from 100 to 101, and then to 111 as per the outlined reconfiguration in Fig. 4. Application of the SAT attack [2] for this scenario is explained below.

Consider that the oracle implements f1 during the first iteration of the SAT solver, where the input applied is 101 (Fig. 5). The SAT solver is oblivious to the function being active in any iteration. The first iteration prunes key combinations k0, k2, k5, and k7. While this is happening, the gate X4 morphs into NOR and the oracle is now implementing function f2. In the second iteration, the input pattern 100 eliminates keys k3, k4, and k6. Thereafter, the SAT solver concludes that the correct key bit and identity of gate X4 are 001 and BUF, respectively.

In this way, dynamic camouflaging deceives the SAT solver to converge to an incorrect key, leading to an incorrect gate assignment. Thus, the IP is protected against analytical RE. As for physical RE, the interconnect fabric which routes the control signals to the MESO gates has to be resilient against probing. Shielding may deter probing [30].

For error-tolerant applications, the circuit may also be randomly reconfigured by deriving the control signals of the MESO gates from a TRNG (recall Fig. 3(b)). Removal attack targeting the TRNG will result in floating control lines for the MESO gates, leading to noisy outputs and loss of functionality. Advanced attacks directed at distorting the entropy of the TRNG to change its bias [37] are out-of-scope for this study.

To evaluate the resilience of run-time polymorphism, we extend the open-source framework from [38] to execute SAT attacks on polymorphic versions of HIC-99 benchmarks. Even for 100,000 runs, the attacks fail due to inconsistent I/O

![Fig. 5. SAT attack [2] on the polymorphic circuit of Fig. 4. For k0 and k1, the INV and BUF operations performed on the output of X2.](image-url)
mappings, which induce an unsatisfiable (UNSAT) scenario for the SAT attack [2]. The primitive is modeled as per the methodology outlined in [35]: each MESO gate with inputs $A$ and $B$ with control signal $X$ is modeled as an 8-to-1 MUX with three select lines. The select lines represent the “key bits”, and allow the SAT solver to select one of the eight possible functions at a time.

E. Case study of image processing IP

To show how dynamic camouflaging can protect approximate circuits, we design a cellular neural network (CeNN) using MESO gates, as shown in Fig. 6. We use the same methodology for its construction as the all spin logic (ASL)-based spintronic CeNN in [39], using parameters for the MESO device from [14]. Fig. 6 shows the connectivity of cells in the CeNN, and the transient switching of a MESO CeNN cell. The central MESO device is connected to eight other MESO devices in a $3 \times 3$ grid. The inset of Fig. 6(b) depicts the CeNN templates $\{A, B, I\}$ used for simple image reconstruction. In contrast to [39], there is no voltage-to-current transduction between CeNN cells since the output of the MESO device remains in the current domain.

We investigate the implications of attacking an approximate image processing IP with AppSAT [3]. Approximate circuits are vulnerable to such attacks since the attacker can recover a functionally-similar IP. To safeguard the MESO-based CeNN against AppSAT, we use run-time polymorphism for dynamic reconfiguration (as shown in Fig. 4). This implies that the image processing IP works at sub-optimal accuracy, depending on the Hamming distance (HD) between the different morphing circuit templates ($f_1$, $f_2$, and $f_3$ in Fig. 4). By tuning this HD through system level design (selecting gates that need to be polymorphic) one can control how similar the IP recovered by AppSAT is, when compared to the original IP. The HD between the polymorphic templates inside the original IP, which decides the accuracy at the system level, is different from the HD between the AppSAT-recovered IP and the original IP.

Since CAD tools and synthesizable Verilog models for emerging spin devices like MESO are at a nascent stage in the research community, we perform simulations on ITC-99 benchmarks. In experiments on $b14$ benchmark, a $\sim 11\%$ HD between polymorphic templates translates to $\sim 28\%$ HD between the AppSAT-recovered IP and the original IP (Table III). In Table III, templates 1-3 are approximate versions of each benchmark, with their respective HD from the original design. We execute AppSAT (setup details same as in [3]) considering that the benchmark morphs between its original form and three approximate templates. AppSAT provides an approximate-key after time-out unlike the SAT attack [2]. Using this approximate key, we calculate the HD between the AppSAT-recovered IP and the original IP, which is quoted in the last column.

The image reconstructed by the CeNN at various representative values of HD between the AppSAT-recovered IP and the original IP is shown in Fig. 7. As seen in Fig. 7(e), at a sufficiently large HD of $25\%$, the AppSAT-recovered IP fails to faithfully reconstruct the original image. For the AppSAT-recovered IPs incurring an even larger HD in Table III, the reconstructed image will naturally be more noisy.

There is a clear trade-off between the accuracy of the original IP and the resilience to AppSAT attacks, in terms of how closely AppSAT is able to resolve the original IP. However, for approximate applications like image processing, which can tolerate a certain degree of error, our scheme can thwart any attempts to recover even an approximate version of the IP. Advanced IP protection mechanisms based on point...

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**TABLE III**

| Benchmark | HD from the original design | HD from AppSAT after| HD inferred between AppSAT recovered IP and original IP calculated using Synopsys VCS for 100,000 patterns |
|-----------|-----------------------------|---------------------|-------------------------------------------------|
| $b14$     | 11.22                       | 9.26                | 13.78, 28.81                                    |
| $b15\_1$  | 12.35                       | 9.62                | 12.88, 32.15                                   |
| $b17\_1$  | 11.14                       | 10.62               | 15.24, 36.22                                   |
| $b20$     | 12.51                       | 14.37               | 17.86, 34.34                                   |

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$^4$Dynamic camouflaging does not require “key bits” as opposed to logic locking. We use the notion of keys to illustrate conceptual equivalence of the scheme with logic locking [35] and to assess the attack framework [2], [3].

$^5$These templates represent the weights of synapses connecting adjacent cells of the CeNN.

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![Fig. 6. MESCO-based CeNN for image reconstruction. Each cell in the network is implemented by a MESCO device. (b) Magnetization vs. time shows the switching of the central MESCO CeNN cell, when inputs from its nearest neighbor cells are applied. The switching delay is $\sim 200$ ps. The MESCO CeNN is simulated using a Landau-Lifshitz-Gilbert dynamics framework on CUDA-C, with 1000 nanomagnet simulations per cell. The inset shows the templates $\{A, B, I\}$ used to configure the CeNN.](image_url)
functions [9], [11] and stripping of functionality [12] may not be suitable for protecting error-tolerant systems, such as the image processing IP considered in this work. That is because these techniques trade-off output corruptibility for SAT-attack resilience; the lower the output corruptibility, the stronger the resilience.

Attacks working on the notion of recovering an approximate version of the protected IP (e.g., AppSAT) are thereby able to successfully recover a satisfactorily functional similar IP if protected using [9], [11], [12]. Also, dynamic reconfiguration at run-time cannot protect systems which demand accurate and error-free computations, for e.g., cryptographic applications.

F. Side-channel attacks

Side-channel attacks exploiting the electromagnetic (EM) radiation traces emitted from devices have gained traction [40]. Such attacks rely on detecting the electric current-induced magnetic field set up in the device or the interconnects. With regards to the MESO device, the typical currents in the interconnects are in the order of $\sim 10 \mu A$. Such small currents result in extremely minute magnetic fields of $\sim 10 \mu T$, which are smaller than the earth’s magnetic field. These fields cannot distort the magnetic moments of the ferromagnets in the adjacent device. Hence, detecting EM traces requires a resolution beyond the capabilities of state-of-the-art EM probes. The MESO device is resilient to other side-channel attacks plaguing CMOS systems, such as photonic and acoustic. Spin devices operate inherently differently owing to the underlying physics, and hence are devoid of the vulnerabilities that these attacks seek to exploit. Still, a system-level security analysis is necessary once applications are constructed using these devices.

G. Layout analysis

The baseline designs are implemented in CMOS leveraging the NangateOpenCellLibrary [41] using Cadence Innovus 18.1. The PPA numbers assume a simple replacement of all CMOS gates with MESO gates.7 We use PPA numbers from respective publications for a comparative study (Table IV). The PPA metrics for the MESO device are 0.04 μW, 200 ps and 0.0014 μm² respectively [14], ASL and giant spin-Hall effect (GSHE)-based [18], [42] full-chip camouflaging incur excessive power and timing overheads. MESO-based camouflaging offers substantial PPA reductions relative to these spin devices and are expected to be even better when compared to CMOS-based camouflaging [7]–[9].

IV. CONCLUSION

Functional polymorphism for IP protection has been largely unexplored in the context of securing hardware. We present dynamic camouflaging as a design-for-trust technique, based on the foundations of run-time polymorphism and post-fabrication reconfigurability exhibited by emerging spin-based devices. We harness this unique attribute of spin devices, specifically the MESO switch, to implement a scheme which thwart state-of-the-art SAT attacks by transforming the I/O mapping of the chip on-the-fly, misleading SAT algorithms to converge to a false assignment. Dynamic camouflaging can secure the supply chain end to end, including foundry, test facility, and end-user. Securing error-tolerant IP, such as image processors, is shown to be a suitable application for dynamic camouflaging. MESO-based full-chip camouflaging offers savings of 7,439×, 5.88×, and 73× in PPA respectively compared to ASL-based camouflaging. Compared to GSHE-based camouflaging, the savings are 5×, 4.8×, and 1.1× in PPA respectively. This is because the polymorphic MESO device consumes significantly lower switching energy (on the order of $\sim 10$ atto Joules) than other spin devices, due to its energy-efficient electric-field-driven reversal.

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