The TMC2010 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 160 nanosecond cycle time (more than 60 MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a three bit eXTended Product (XTP), a sixteen bit Most Significant Product (MSP), and a sixteen bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW's state-of-the-art 2-micron CMOS process, the TMC2010 is pin and function compatible with the industry standard TDC1010 and operates with the same speed at one-sixth or less power dissipation, depending on the multiply-accumulate rate.

Features
- Low Power Consumption CMOS Process
- Pin And Function Compatible With TRW TDC1010
- 160ns Multiply—Accumulate Time (Worst Case)
- 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Available In 64 Lead DIP, 68 Contact Chip Carrier Or 68-Leaded Chip Carrier

Applications
- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram
Pin Assignments

| Pin | Description |
|-----|-------------|
| X9  | 1           |
| X7  | 64          |
| X8  | 53          |
| X9  | 56          |
| X10 | 55          |
| X11 | 54          |
| X12 | 53          |
| X13 | 52          |
| X14 | 51          |
| X15 | 50          |
| X16 | 49          |
| X17 | 48          |
| X18 | 47          |
| X19 | 46          |
| X20 | 45          |
| X21 | 44          |
| X22 | 43          |
| X23 | 42          |
| X24 | 41          |
| X25 | 40          |
| X26 | 39          |
| X27 | 38          |
| X28 | 37          |
| X29 | 36          |
| X30 | 35          |
| X31 | 34          |
| X32 | 33          |

64 Lead DIP - J3 Package

68 Contact Or Leaded Chip Carrier - C1, L1 Package

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TRW Electronic Components Group
Functional Description

General Information

The TMC2010 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 16-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two’s complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two’s complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TMC2010 to be used on a bus, or allow the outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC2010 operates from a single +5 Volt supply. All power and ground lines must be connected.

| Name    | Function       | Value | J3 Package | C1, L1 Package |
|---------|----------------|-------|------------|---------------|
| vDD     | Positive Supply Voltage | +5.0V | Pin 49     | Pins 17, 18, 19, 20 |
| GND     | Ground         | 0.0V  | Pin 16     | Pins 53, 54   |

Data Inputs

The TMC2010 has two 16-bit two’s complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X15 and Y15, carry the sign information for the two’s complement notation. The remaining bits are denoted X14 through X0 and Y14 through Y0 (with X0 and Y0 the Least Significant Bits). Data present at the X and Y inputs is clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two’s complement notation, fractional unsigned magnitude notation, integer two’s complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

| Name    | Function   | Value | J3 Package | C1, L1 Package |
|---------|------------|-------|------------|---------------|
| X15     | X Data MSB | TTL   | Pin 56     | Pin 10        |
| X14     |            | TTL   | Pin 57     | Pin 9         |
| X13     |            | TTL   | Pin 58     | Pin 8         |
| X12     |            | TTL   | Pin 59     | Pin 7         |
| X11     |            | TTL   | Pin 60     | Pin 6         |
| X10     |            | TTL   | Pin 61     | Pin 5         |
| X9      |            | TTL   | Pin 62     | Pin 4         |
| X8      |            | TTL   | Pin 63     | Pin 3         |
| X7      |            | TTL   | Pin 64     | Pin 2         |
| X6      |            | TTL   | Pin 1      | Pin 1         |
| X5      |            | TTL   | Pin 2      | Pin 68        |
| X4      |            | TTL   | Pin 3      | Pin 67        |
| X3      |            | TTL   | Pin 4      | Pin 66        |
| X2      |            | TTL   | Pin 5      | Pin 65        |
| X1      |            | TTL   | Pin 6      | Pin 64        |
| X0      | X Data LSB | TTL   | Pin 7      | Pin 63        |
Data Inputs (Cont.)

| Name | Function | Value | J3 Package | C1, L1 Package |
|------|----------|-------|------------|---------------|
| Y15  | Y Data MSB | TTL   | Pin 24     | Pin 45        |
| Y14  | TTL      | Pin 23 | Pin 46     |
| Y13  | TTL      | Pin 22 | Pin 47     |
| Y12  | TTL      | Pin 21 | Pin 48     |
| Y11  | TTL      | Pin 20 | Pin 49     |
| Y10  | TTL      | Pin 19 | Pin 50     |
| Y9   | TTL      | Pin 18 | Pin 51     |
| Y8   | TTL      | Pin 17 | Pin 52     |
| Y7   | TTL      | Pin 15 | Pin 55     |
| Y6   | TTL      | Pin 14 | Pin 56     |
| Y5   | TTL      | Pin 13 | Pin 57     |
| Y4   | TTL      | Pin 12 | Pin 58     |
| Y3   | TTL      | Pin 11 | Pin 59     |
| Y2   | TTL      | Pin 10 | Pin 60     |
| Y1   | TTL      | Pin 9  | Pin 61     |
| Y0   | Y Data LSB | TTL   | Pin 8      | Pin 62        |

Data Outputs

The TMC2010 has a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the Most Significant Product (MSPI) and Least Significant Product (LSPI), and one 3-bit output word, the eXtended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

| Name | Function | Value | J3 Package | C1, L1 Package |
|------|----------|-------|------------|---------------|
| P34  | Product MSB | TTL   | Pin 43     | Pin 26        |
| P33  | TTL      | Pin 42 | Pin 27     |
| P32  | TTL      | Pin 41 | Pin 28     |
| P31  | TTL      | Pin 40 | Pin 29     |
| P30  | TTL      | Pin 39 | Pin 30     |
| P29  | TTL      | Pin 38 | Pin 31     |
| P28  | TTL      | Pin 37 | Pin 32     |
| P27  | TTL      | Pin 36 | Pin 33     |
| P26  | TTL      | Pin 35 | Pin 34     |
| P25  | TTL      | Pin 34 | Pin 35     |
| P24  | TTL      | Pin 33 | Pin 36     |
| P23  | TTL      | Pin 32 | Pin 37     |
| P22  | TTL      | Pin 31 | Pin 38     |
| P21  | TTL      | Pin 30 | Pin 39     |
| P20  | TTL      | Pin 29 | Pin 40     |
| P19  | TTL      | Pin 28 | Pin 41     |
| P18  | TTL      | Pin 27 | Pin 42     |
| P17  | TTL      | Pin 26 | Pin 43     |
| P16  | TTL      | Pin 25 | Pin 44     |
Data Outputs (Cont.)

| Name   | Function       | Value | J3 Package | C1, L1 Package |
|--------|----------------|-------|------------|---------------|
| P15    | TTL            | Pin 24| Pin 45     |               |
| P14    | TTL            | Pin 23| Pin 46     |               |
| P13    | TTL            | Pin 22| Pin 47     |               |
| P12    | TTL            | Pin 21| Pin 48     |               |
| P11    | TTL            | Pin 20| Pin 49     |               |
| P10    | TTL            | Pin 19| Pin 50     |               |
| P9     | TTL            | Pin 18| Pin 51     |               |
| P8     | TTL            | Pin 17| Pin 52     |               |
| P7     | TTL            | Pin 16| Pin 53     |               |
| P6     | TTL            | Pin 15| Pin 54     |               |
| P5     | TTL            | Pin 14| Pin 55     |               |
| P4     | TTL            | Pin 13| Pin 56     |               |
| P3     | TTL            | Pin 12| Pin 57     |               |
| P2     | TTL            | Pin 11| Pin 58     |               |
| P1     | TTL            | Pin 10| Pin 59     |               |
| P0     | TTL            | Pin  9| Pin 60     |               |
|        | Product LSB    | TTL   | Pin  8     | Pin 61       |

Clocks

The TMC2010 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers is loaded into the registers at the rising edge of the appropriate clock. The Round (RND), Two's Complement (ITC), Accumulate (ACC), and Subtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

| Name   | Function       | Value | J3 Package | C1, L1 Package |
|--------|----------------|-------|------------|---------------|
| CLX    | Clock Input Data X | TTL   | Pin 51     | Pin 15       |
| CLX Y  | Clock Input Data Y | TTL   | Pin 50     | Pin 16       |
| CLX P  | Clock Product Register | TTL   | Pin 44     | Pin 25       |
The TMC2010 has eight control lines: TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is HIGH, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating it.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and their sum is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

| Name  | Function                        | Value | J3 Package | C1, L1 Package |
|-------|---------------------------------|-------|------------|---------------|
| TSX   | XTP Three-State Control         | TTL   | Pin 47     | Pin 22        |
| TSM   | MSP Three-State Control         | TTL   | Pin 45     | Pin 24        |
| TSL   | LSP Three-State Control         | TTL   | Pin 55     | Pin 11        |
| PREL  | Preload Control                 | TTL   | Pin 46     | Pin 23        |
| RND   | Round Control Bit               | TTL   | Pin 54     | Pin 12        |
| TC    | Two's Complement Control        | TTL   | Pin 48     | Pin 21        |
| ACC   | Accumulate Control              | TTL   | Pin 52     | Pin 14        |
| SUB   | Subtract Control                | TTL   | Pin 53     | Pin 13        |
**Absolute maximum ratings** (beyond which the device will be damaged)

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

### Supply Voltage
- Min: -0.5 V
- Nom: 5.0 V
- Max: 5.25 V
- Units: V

### Input Voltage
- Applied voltage: -0.5 V to (VDD + 0.5 V)
- Forced current: -1.0 mA to 6.0 mA
- Short-circuit duration (single output in high state to ground): 1 sec

### Temperature
- Operating, case: -60°C to +120°C
- Junction: 175°C
- Lead, soldering (10 seconds): 300°C
- Storage: -65°C to +150°C

### Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
### Electrical characteristics within specified operating conditions

| Parameter             | Test Conditions                                  | Temperature Range | Units |
|-----------------------|--------------------------------------------------|-------------------|-------|
|                       |                                                  | Standard          |       |
|                       |                                                  | Min   | Max |       |
| $I_{DD}$ Quiescent    | $V_{DD} = 5.0V, V_{IN} = 0V$ TSL, TSM, TSX = 5.0V | 1     |     | mA   |
| Supply Current        | $V_{DD} = 5.0V, F = 6MHz$ TSL, TSM, TSX = 5.0V | 40    |     | mA   |
| Supply Current        | $V_{DD} = 5.0V, F = 6MHz$ TSL, TSM, TSX = 0V   | 120   |     | mA   |
|                       | Load = Load 1                                    | 1     |     | µA   |
| $I_{IL}$ Input Current, Logic Low $^1$ | $V_{DD} = MAX, V_{I} = 0.5V$ | -75   | +75 | µA   |
| $I_{IH}$ Input Current, Logic High $^1$ | $V_{DD} = MAX, V_{I} = 2.4V$ | -75   | +75 | µA   |
| $I_{I}$ Input Current, Max Input V | $V_{DD} = MAX, V_{I} = V_{DD}$ | 200   |     | µA   |
| $V_{OL}$ Output Voltage, Logic Low | $V_{DD} = MIN, I_{OL} = MAX$ | 0.4   |     | V    |
| $V_{OH}$ Output Voltage, Logic High | $V_{DD} = MIN, I_{OH} = MAX$ | 2.4   |     | V    |
| $I_{OS}$ Short-Circuit Output Current | $V_{DD} = MAX, Output high, one pin to ground, one second duration max$ | -100  |     | mA   |
| $C_{I}$ Input Capacitance | $T_{A} = 25^\circ C, F = 1MHz$ | 15     |     | pF   |
| $C_{O}$ Output Capacitance | $T_{A} = 25^\circ C, F = 1MHz$ | 15     |     | pF   |

Note:
1. These values are also valid for outputs in high-impedance state.

### Switching characteristics within specified operating conditions

| Parameter             | Test Conditions                                  | Temperature Range | Units |
|-----------------------|--------------------------------------------------|-------------------|-------|
|                       |                                                  | Standard          |       |
|                       |                                                  | Min   | Max |       |
| $t_{MA}$ Multiply–Accumulate Time | $V_{DD} = MIN, Load 1$ | 160   |     | ns   |
| $t_{D}$ Output Delay   | $V_{DD} = MIN, Load 1$ | 45    |     | ns   |
| $t_{ENA}$ Three–State Output Enable Delay | $V_{DD} = MIN, Load 1$ | 40    |     | ns   |
| $t_{DIS}$ Three–State Output Disable Delay | $V_{DD} = MIN, Load 2$ | 35    |     | ns   |

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TRW Electronic Components Group
Preload Truth Table 1

| PREL | TSX | TSM | TSL | XTP       | MSP       | LSP       |
|------|-----|-----|-----|-----------|-----------|-----------|
| L    | L   | L   | L   | Register  | Output pin| Register  |
| L    | L   | L   | H   | Register  | Output pin| Hi-Z      |
| L    | L   | H   | L   | Register  | Output pin| Hi-Z      |
| L    | H   | L   | L   | Hi-Z     |           | Register  |
| L    | H   | L   | H   | Hi-Z     |           | Hi-Z      |
| L    | H   | H   | H   | Hi-Z     |           | Hi-Z      |
| H2   | L   | L   | H   | Hi-Z     | Hi-Z Preload| Hi-Z      |
| H2   | L   | H   | L   | Hi-Z     | Hi-Z Preload| Hi-Z      |
| H2   | H   | L   | L   | Hi-Z Preload| Hi-Z Preload| Hi-Z      |
| H2   | H   | H   | L   | Hi-Z Preload| Hi-Z Preload| Hi-Z      |
| H2   | H   | H   | H   | Hi-Z Preload| Hi-Z Preload| Hi-Z      |

Notes:  
1. PREL, TSX, TSM, and TSL are not registered.  
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Application Notes

Multiplication by a Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC2010 does not differentiate between this operation:

6 x 2 = 12

and this operation:

$6/8 \times 2/8 = 12/64$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.
## Ordering Information

| Product Number | Temperature Range | Screening                  | Package          | Package Marking |
|----------------|-------------------|----------------------------|------------------|-----------------|
| TMC2010J3C     | STD-\(T_A\) = 0°C to 70°C | Commercial                 | 64 Lead DIP      | 2010J3C         |
| TMC2010J3G     | STD-\(T_A\) = 0°C to 70°C | Commercial With Burn-In    | 64 Lead DIP      | 2010J3G         |
| TMC2010C1C     | STD-\(T_A\) = 0°C to 70°C | Commercial                 | 68 Contact Chip Carrier | 2010C1C         |
| TMC2010C1G     | STD-\(T_A\) = 0°C to 70°C | Commercial With Burn-In    | 68 Contact Chip Carrier | 2010C1G         |
| TMC2010L1C     | STD-\(T_A\) = 0°C to 70°C | Commercial                 | 88 Leaded Chip Carrier | 2010L1C         |
| TMC2010L1G     | STD-\(T_A\) = 0°C to 70°C | Commercial With Burn-In    | 88 Leaded Chip Carrier | 2010L1G         |

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**Preliminary Information** describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact TRW for current information.
TMC2010
· Use TMC2210 for New Design

CMOS Multiplier—Accumulator
16 x 16 Bit, 160ns

The TMC2010 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 160 nanosecond cycle time (more than 6MHz multiply-accumulate rate). The input data may be specified as two’s complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 16-bit Most Significant Product (MSP), and a 16-bit Least Significant Product (LSPI). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW’s state-of-the-art 2-micron CMOS process, the TMC2010 is pin and function compatible with the industry standard TDC1010 and operates with the same speed at one-sixth or less power dissipation, depending on the multiply-accumulate rate.

Features
• Low Power Consumption CMOS Process
• Pin And Function Compatible With TDC1010
• 160ns Multiply—Accumulate Time (Worst Case)
• 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
• Selectable Accumulation, Subtraction, Rounding, And Preloading
• All Inputs And Outputs Are Registered TTL Compatible
• Three-State Output
• Two’s Complement Or Unsigned Magnitude Operation
• Single +5V Power Supply
• Available In 64 Lead DIP, 68 Contact Chip Carrier Or 68 Leaded Chip Carrier

Applications
• Array Processors
• Video Processors
• Radar Signal Processors
• FFT Processors
• General Purpose Digital Signal Processors
• Microcomputer/Minicomputer Accelerators
Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC2009 does not differentiate between this operation:

\[ 6 \times 2 = 12 \]

and this operation:

\[ \frac{6}{8} \times \frac{2}{16} = \frac{12}{64} \]

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

| Product Number | Temperature Range | Screening       | Package | Package Marking |
|----------------|-------------------|----------------|---------|----------------|
| TMC2009JC      | STD – TA = 0°C to 70°C | Commercial     | 64 Lead DIP | 2009JC         |
| TMC2009JG      | STD – TA = 0°C to 70°C | Commercial With Burn-In | 64 Lead DIP | 2009JG         |
| TMC2009JGV     | EXT – TC = -55°C to 125°C | MIL-STD-883    | 64 Lead DIP | 2009JGV        |
| TMC2009C1V     | EXT – TC = -55°C to 125°C | MIL-STD-883    | 64 Contact Chip Carrier | 2009C1V       |

Notes:
1. Contact factory for availability.

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TMC2110
· Use TMC2210 for New Design

CMOS Multiplier-Accumulator
16 x 16 Bit, 100ns

The TMC2110 is a high-speed 16 x 16 bit parallel multiplier-accumulator which operates at a 100 nanosecond cycle time (10MHz multiply-accumulate rate). The input data may be specified as two's-complement or unsigned magnitude, yielding a full-precision 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 16-bit Most Significant Product (MSP), and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and the MSP; the LSP is multiplexed with the Y input. The output register can be preloaded directly via the output ports.

Built with TRW's state-of-the-art 1-micron OMICRON-C™ CMOS process, the TMC2110 is pin and function compatible with the industry standard TDC1010, yet operates at more than 50% greater speed.

Features
- 100ns Multiply-Accumulate Time
- Pin And Function Compatible With TRW TDC1010 And TMC2010
- 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State TTL Compatible CMOS Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 64 Lead Ceramic DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

Applications
- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram

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CMOS Multiplier–Accumulator
8 x 8 Bit, 40ns

The TMC2208 is a high-speed 8 x 8-bit parallel multiplier–accumulator which operates at a 40ns cycle time (25MHz multiply–accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. Products may be accumulated to a 19-bit result.

Individually clocked input and output registers are used to provide maximum system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), an 8-bit Most Significant Product (MSP), and an 8-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, MSP, and LSP. The output register can be preloaded directly via the output ports.

The TMC2208 is pin and function compatible with the TDC1008 in the 48-lead DIP. Built with TRW's OMICRON-C™ one micron CMOS process, power consumption is greatly reduced.

Features
- Function Compatible With The TDC1008 (Pin Compatible In 48 Lead Dip Package)
- 35ns Multiply–Accumulate Time (Worst Case Commercial)
- 8 x 8 Parallel Multiplication With Accumulation To 19-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Accumulator Preload
- All Inputs And Outputs Are Registered And TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Low Power CMOS Construction
- Available In 48 Lead Ceramic DIP Or 68 Lead Pin Grid Array

Applications
- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Micro/Mini-Computer Accelerators

Functional Block Diagram