PANDA: Processing-in-MRAM Accelerated De Bruijn Graph based DNA Assembly

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Abstract—Spurred by widening gap between data processing speed and data communication speed in Von-Neumann computing architectures, some bioinformatic applications have harnessed the computational power of Processing-in-Memory (PIM) platforms. However, the performance of PIMs unavoidably diminishes when dealing with such complex applications seeking bulk bit-wise comparison or addition operations. In this work, we present an efficient Processing-in-MRAM Accelerated De Bruijn Graph based DNA Assembly platform named PANDA based on an optimized and hardware-friendly genome assembly algorithm. PANDA is able to assemble large-scale DNA sequence data set from all-pair overlaps. We first design PANDA platform that exploits MRAM as a computational memory and converts it to a potent processing unit for genome assembly. PANDA can execute not only efficient bulk bit-wise X(N)OR-based comparison/addition operations heavily required for the genome assembly task but a full-set of 2/-3-input logic operations inside MRAM chip. We then develop a highly parallel and step-by-step hardware-friendly DNA assembly algorithm for PANDA that only requires the developed in-memory logic operations. The platform is then configured with a novel data partitioning and mapping technique that provides local storage and processing to fully utilize the algorithm-level’s parallelism. The cross-layer simulation results demonstrate that PANDA reduces the run time and power, respectively, by a factor of 18 and 11 compared with simulation results. This shows in Fig. 1a.

Today’s bioinformatics application acceleration solutions are mostly based on the von-Neumann architecture with separate computing and memory components connecting via buses and inevitably consumes a large amount of energy in data movement between them [4], [5]. In the last two decades, Processing-in-Memory (PIM) architecture, as a potentially viable way to solve the memory wall challenge, has been well explored for different applications [5], [6], [7], [8], [9], [10], [11]. Especially processing-in-non-volatile memory architecture has achieved remarkable success by dramatically reducing data transfer energy and latency [12], [13], [14], [15], [16]. The key concept behind PIM is to realize logic computation within memory to process data by leveraging the inherent parallel computing mechanism and exploiting large internal memory bandwidth. Besides, most of CPU [17]/GPU [18]/FPGA [19] and even PIM [4], [5]-based efforts have only focused on the DNA short read alignment problem, while the de novo genome assembly problem still relies mostly on CPU-based solutions [20]. De novo assemblies are categorized into Overlap Layout Consensus (OLC), greedy, and de Bruijn graph-based designs. Recently, de Bruijn graph-based assemblers have gained much more attention as they are able to solve the problem using Euler path in a polynomial time rather than finding Hamiltonian path in OLC-based assemblers as an NP hard problem [21]. There are multiple CPU-based genome assemblers implementing the bi-directed de Bruijn graph model, such as Velvet [22], Trinity [23], etc. However,
only a few GPU-accelerated assemblers have been presented such as GPU-Euler [20], [24], [25]. This mainly comes from the nature of the assembly workload that is not only compute-intensive but also extremely data-intensive requiring very large working memories. Therefore adapting such problem to use GPUs with their limited memory capacities has brought many challenges [26]. A graph-based genome assembly process, shown in Fig. 1a, as the main focus of this work, basically consists of multiple stages, i.e. k-mer analysis for creating a Hashmap, graph construction and traversal, and scaffolding and gap closing. Fig. 1b depicts the breakdown of execution time for the well-known Meraculous assembler [3] for the human and wheat data sets. We observe that Hashmap and graph construction/traversal are the two most expensive components, which together take over 80% of the total run time.

This motivates us to show that the genome assembly problem and especially computationally-loaded components can exploit the large internal bandwidth of Magnetic Random Access Memory (MRAM) chip for PIM acceleration. Moreover, with a careful observation of genome assembly workload, it turns out this task heavily relies on comparison and addition operations. However, due to the intrinsic complexity of X(N)OR logic, the throughput of processing-in-memory platforms [12, 13, 5, 27, 28] unavoidably diminishes when dealing with such bulk bit-wise operations. This is because multi-cycle majority/AND/OR-based operations. In this work, we explore a highly-parallel and PIM-friendly implementation of de Bruijn graph-based genome assembly that can accelerate especially the first two stages of the algorithm. Overall this paper makes the following contributions:

1. To the best of our knowledge, this work is the first that designs a high-throughput comparison/addition-friendly processing-in-MRAM architecture for the de Bruijn graph-based genome assembly. We develop PANDA based on a set of innovative microarchitectural and circuit-level schemes to realize a data-parallel computational core for genome assembly;
2. We reconstruct the existing genome assembly algorithm in a step-by-step fashion to be fully implemented in PIM platforms. It supports short read analysis, graph construction, and traversal; (3) We propose a dense data mapping and partitioning scheme to process the indices locally and handle various length DNA sequences; (4) We extensively assess and compare PANDA’s performance, energy-efficiency, and memory bottleneck ratio with a CPU and recent potential PIM platforms.

II. PANDA PLATFORM

A. SOT-MRAM

Fig. 2a shows a Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) device structure. The storage element in SOT-MRAM is SHE-MTJ [29], [30], a composite device structure of a Spin Hall Metal (SHM) and Magnetic Tunnel Junction (MTJ). The binary data is stored as resistance states of MTJ. Data-‘0’(‘1’) is encoded as the MTJ’s lower(higher) resistance or parallel(anti-parallel) magnetization in both magnetic layers (free and fixed layers). Here the flow of charge current (±y) through the SHM (Tungsten, $\beta - W$ [31]) will cause accumulation of opposite directed spin on both surfaces of SHM due to spin Hall effect [29]. Thus, a spin current flowing in ±z is generated and further produces spin-orbit torque (SOT) on the adjacent free magnetic layer, causing switch of magnetization. Each cell located in the computational sub-array is connected with a Write Word Line (WWL), Write Bit Line (WBL), Read Word Line (RWL) Read Bit Line (RBL), and Source Line (SL). The bit-cell structure of 2T1R SOT-MRAM and its biasing conditions are shown in Fig. 2b and 2c, respectively. In this work, the magnetization dynamics of Free Layer (m) are modeled by LLG equation with spin-transfer torque terms, which can be mathematically described as [29]:

$$\frac{dm}{dt} = -|\gamma| m \times H_{eff} + \alpha \left( m \times \frac{dm}{dt} \right) + |\gamma| |\beta| (m \times m_p) - |\gamma| \beta' (m \times m_p)$$  \hspace{1cm} (1)

$$\beta = \frac{\hbar}{2 \mu_0 e A_{MTJ} M_s t_{FL} \ell_s}$$  \hspace{1cm} (2)

where $\hbar$ is the reduced plank constant, $\gamma$ is the gyromagnetic ratio, $I_c$ is the charge current flowing through MTJ, $t_{FL}$ is the thickness of free layer, $\ell_s$ is the second Spin transfer torque coefficient, and $H_{eff}$ is the effective magnetic field, $P$ is the effective polarization factor, $A_{MTJ}$ is the cross sectional area of MTJ, $m_p$ is the unit polarization direction. Note that the ferromagnets in MTJ have In-plane Magnetic Anisotropy (IMA) in x-axis [29]. With the given thickness (1.2nm) of the tunneling layer (MgO), the Tunnel Magneto-Resistance (TMR) of the MTJ is $\sim 171.2\%$.

B. Architecture Design

We develop PANDA platform based on typical SOT-MRAM hierarchy. Each memory chip consists of multiple memory banks divided into 2D sub-arrays of SOT-MRAM cells as shown in Fig. 3. We then apply our modification on the sub-array level to make it reconfigurable to support both memory operation and in-memory bit-line computation. As depicted
method on top of a novel reconfigurable SA design shown in Fig. 3 to handle memory read and in-memory computation. The main idea of reference selection is to simultaneously compare the resistance state of selected SOT-MRAM cell(s) with one or multiple reference resistors in SA(s) to generate the results. PANDA’s SA consists of three sub-SAs with a total of four reference resistors. The ctrl unit could pick the proper reference using control bits \((C_{AND}, C_{MAJ}, C_{OR}, C_{M})\) to realize the memory read and a full-set of 2- and 3-input logic functions, as tabulated in the Table I. We designed and tuned the sense circuit based on StrongARM latch [32] shown in Fig. 3. Each read-in-memory computing operation requires two clock phases: pre-charge (Clk ‘high’) and sensing (Clk ‘low’). For instance, to realize the read operation, the memory row decoder first activates the corresponding RWL, then a small sense current (I\(_{sense}\)) flows from the selected cell to ground, and generates a sense voltage (V\(_{sense}\)) at the input of SA-III. This voltage is accordingly compared with the memory mode reference voltage activated by C\(_{M}\) (V\(_{sense, P} < V_{ref,M} < V_{sense,AP}\), as shown in Fig. 4). The SA-III produces high (low) voltage if the path resistance is higher (lower) than R\(_{M}\) (memory reference resistance), i.e. \(R_{AP} (R_{P})\). PANDA could implement one-threshold in-memory operations \((\llcorner \llcorner AND, (\llcorner \llcorner OR, etc.) by activating multiple RWLs simultaneously, and only by activating one SA’s enable at a time e.g. by setting C\(_{AND}\) to ‘1’, 3-input AND/NAND logic can be readily implemented between operands located in the same bit-line. To implement 2-input logics, two rows initialized by ‘0’/’1’ are considered in every sub-array such that functions can be made out of 3-input functions.

**Addition:** PANDA’s SA is enhanced with a unique circuit design that allows single-cycle implementation of addition/subtraction (add/sub) operation quite efficiently. By activating three memory rows at the same time (RWL1, RWL2, and RWL3 in Fig. 3b), OR3, Majority (MAJ) and AND3 functions can be readily realized through SA-I, SA-II, and SA-III, respectively. Each SA compares the equivalent resistance of parallel connected input cells and their cascaded access transistors with a programmable references by SA \((R_{OR3}/R_{MAJ}/R_{AND3})\). The idea of voltage comparison between V\(_{sense}\) and V\(_{ref}\) to realize these functions is depicted in Fig. 4. While there are several addition-in-memory designs in non-volatile memory domain, they typically apply a large circuitry after SA to realize a multi-cycle design. In order to implement a single-cycle addition operation, we then reformulate the full-adder Boolean expression to make it PIM-friendly. We noticed when majority function of three input is 0, the Sum can be implemented by OR3 function and when majority function is 1, Sum can be achieved through AND3 function. This behavior can be implemented by a multiplexer circuit shown in Add-box in Fig. 3b. The Boolean logic of such in-memory addition function is written as:

\[
\text{Carry} = AB + AC + BC = \text{Maj}(A, B, C) \tag{3}
\]

\[
\text{Sum} = ((AB + AC + BC)\cdot(A + B + C)) + ((AB + AC + BC)\cdot(ABC)) = \text{Maj}(A, B, C) \cdot \text{OR}(A, B, C) + \text{MAJ}(A, B, C) \cdot \text{AND}(A, B, C) \tag{4}
\]
The carry-out of the full-adder can be directly produced by MAJ function (Carry in Fig. 3) just by setting \( C_{\text{MAJ}} \) to ‘1’ in a single memory cycle. For MAJ operation, \( R_{\text{MAJ}} \) is set at the midpoint of \( R_P//R_P//R_{\text{AP}} \) (‘0’, ‘0’, ‘1’) and \( R_P//R_{\text{AP}}//R_{\text{AP}} \) (‘0’, ‘1’, ‘1’), as depicted in Fig. 4. Now, assume M1, M2, and M3 operate (Fig. 3), the PANDA can generate Carry-MAJ and Sum-XOR3 in-memory logics in a single memory cycle. The ctrl’s configuration for such add operation is tabulated in Table I.

**Comparison:** PANDA platform offers a single-cycle implementation of XOR3 in-memory logic (Sum). To realize the bulk bit-wise comparison operation based on XNOR2, one memory row in each PANDA’s sub-array is initialized to ‘1’. In this way, XNOR2 can be readily implemented out of XOR3 function. Therefore, every memory sub-array can potentially perform parallel comparison operation without need to external add-on logic or multi-cycle operation.

![Figure 4. (a) Reference comparison to realize in-memory operations, (b) Monte-Carlo simulation of \( V_{\text{sense}} \).](image)

**D. Performance Analysis**

**Functionality:** To verify the circuit functionality of PANDA’s sub-array, we first model SOT-MRAM cell by jointly applying the Non-Equilibrium Green’s Function (NEGF) and Landau-Lifshitz-Gilbert (LLG) with spin Hall effect equations [29, 30]. We then develop a Verilog-A model of 2-transistor 1-resistor SOT-MRAM device with parameters listed in Table II to co-simulate with other peripheral CMOS circuits displayed in Fig. 3 in Cadence Spectre and SPICE. We use 45nm North Carolina State University (NCSU) Product Development Kit (PDK) library [33] for our circuit analysis. The transient simulation result of a single 256×256 sub-array is shown in Fig. 5. We take M1, M2, and M3 as three SOT-MRAM cells located in the first column as the inputs for our evaluation.

| Parameter                       | Value                        |
|---------------------------------|------------------------------|
| Free layer dimension \((W \times L \times t)_F\) | \(60 \times 40 \times 2\) nm\(^2\) |
| SHM dimension                  | \(60 \times 80 \times 2\) nm\(^2\) |
| Demagnetization Factor, \(D_x\), \(D_y\), \(D_z\) | 0.066; 0.911; 0.022 |
| Spin flip length, \(\lambda_{sh}\) | 1.4 nm                      |
| Spin hall angle, \(\theta_{sh}\) | 0.3                        |
| Gilbert Damping Factor, \(\alpha\) | 0.007                       |
| Saturation Magnetization, \(M_s\) | 850 kA/m                   |
| Oxide thickness, \(t_{ox}\) | 1.2 nm                      |
| RA product, \(R_{\text{AP}}//\text{TMR}\) | 10.58 Ω\(\mu\)m\(^2\)/171.2% |
| Supply voltage                  | 1 V                         |
| CMOS technology                 | 45 nm                       |
| SOT-MRAM cell area              | 69 F\(^2\)                 |
| Access transistor width         | 4.5 F                       |
| Cell aspect Ratio               | 1.91                        |

![Figure 5. Transient simulation wave-forms of PANDA’s sub-array and its reconfigurable SA for performing single-cycle in-memory operations.](image)

Here, we consider four input combination scenarios for the write operation, as indicated by 000, 100, 110, and 111 in Fig. 5. For the sake of clarity of wave-forms, we assume a 3ns period clock synchronizes the write and read operation. However, a 2ns period can be used for a reliable read and in-memory computation.

During the precharge phase of SA (Clk=1), \(\pm V_{\text{write}}\) voltage is applied to the WBL to change the MRAM cell resistance to \(R_{\text{low}}=5.6\Omega\) or \(R_{\text{high}}=15.17\ k\Omega\). Prior to the evaluation phase (Eval.) of SA, WWL and WBL is grounded while WBL is fed by the very small sense current, \(I_{\text{sense}}=3\mu A\). In the evaluation phase, RWL goes high and depending on the resistance state of parallel bit-cells and accordingly SL, \(V_{\text{sense}}\) is generated at the first input of SAs, when \(V_{\text{ref}}\) is generated at the second input of SAs. The voltage comparison between \(V_{\text{sense}}\) and \(V_{\text{ref}}\) for AND3 and OR3 and the output of SAs are plotted in Fig. 5. For example, we observe only when \(V_{\text{sense}}\geq V_{\text{ref,AND}}\) (M1M2M3=111), the SA-III outputs binary ‘1’, whereas output is ‘0’. Fig. 5 also shows the in-memory XOR3 function (Sum) accomplished in a single memory cycle through three SA outputs.

**Reliability:** We assess the variation tolerance in the proposed sub-array and SA circuit by running a rigorous Monte-Carlo simulation. We run the simulation for 10000 iterations considering two source of variations in SOT-MRAM cells, first \(\sigma = 5\%\) process variation on the tunneling Magnetoresistive (TMR) and second a \(\sigma = 2\%\) variation on the Resistance-Area product (RA\(\text{P}\)). The results illustrated in Fig. 5 proves that the sense margin reduces by increasing the number of selected input cells for in-memory operations. This can be alleviated by increasing the oxide thickness \(t_{ox}\) of SHE-MTJ as thoroughly discussed in [34]. In this way, the \(t_{ox}\) was increased from 1.5nm to 2nm. This increased the sense margin by \(~45\text{mV} which considerably enhances the reliability.

**Sub-array level Performance:** To explore the hardware overhead of PANDA on top of an standard unmodified SOT-MRAM platform, we perform an iso-capacity performance comparison. We develop both platforms with a sample 32Mb-
single Bank, 512-bit Data Width in NVSim memory evaluation tool. The circuit level data is adopted from our circuit level simulation and then fed into an NVSim-compatible PIM library to report the results. Table III lists the performance measures for dynamic energy, latency, leakage power, and area. We observe there is a ∼30% increase in the area to support the proposed in-memory computing functions for genome assembly. As for dynamic energy, the PANDA shows an increase in R (Read) energy in spite of power gating mechanism used in the reconfigurable SA to turn off non-selected SAs (SA-I and -II while reading operation). In this way, C-Add (C stands for Computation) requires ∼2.4× more power compared with a single SA read operation. However, Table III shows PANDA is able to offer a close-to-read latency for C-AND3 and C-Add compared with the standard design. There is also an increase in leakage power obviously coming from the add-on CMOS circuitry.

### Table III

**Performance Comparison Between an Standard SOT-MRAM Chip and PANDA.**

| Designs  | Area (um²) | Energy (nJ) | Latency (ms) | Leak. power (mW) |
|----------|------------|-------------|--------------|------------------|
| Standard | 0.7        | 3.91        | 4.59         | 3.91             |
| PANDA    | 0.78       | 586         | 0.85         | 402              |

**E. Software Support**

PANDA is designed to be an efficient and independent accelerator for DNA assembly, nevertheless it needs to be exposed to programmers and system-level libraries to use it. PANDA could be directly connected to the memory bus or through PCI-Express lanes as a third party accelerator. Thus, it could be integrated similar to that of GPUs. So, an ISA and a virtual machine for parallel and general-purpose thread execution need to be developed like the NVIDIA’s PTX [35]. With that, at install time, the programs are translated to the PANDA’s ISA discussed here to implement the in-memory functions listed in Table 1. We introduce PANDA_Mem_insert (des, src, size) instruction to read a source data from the memory and write it back to a destination memory location consecutively. The size of input vectors for in-memory computation could be at most a multiple of PANDA’s sub-array row size. PANDA_Cmp (src1, src2, size) performs parallel bulk bit-wise comparison operation between source vector 1 and 2. PANDA_Add (src1, src2, size) runs element-wise addition between cells located in a same column as will be explained in next section.

### III. PANDA Algorithm and Mapping

The genome assembly algorithm consists of three main stages visualized in Fig. 6. First, creating a hash table out of k-mers and keeping a count of each distinct k-mer; second, constructing a de Bruijn Graph with Hashmap; third, traversing through de Bruijn Graph for Euler Path. There is a final stage called scaffolding to close the gaps between contigs, which is the result of the denovo assembly [2].

The first three stages always take most fraction of execute time and computational resources (over 80%) in both CPU and GPU implementations [2]. To effectively handle the huge number of short reads, we modularized the assembly algorithm by focusing on parallelizing the main steps by loading only the necessary data at each stage into PANDA platform, and leave stage-4 as our future work.

#### A. Stage One: Hash Table

Algorithm 1 shows the reconstructed Hashmap(S,k) procedure in which the algorithm takes k-mer from the original sequence (S) in each iteration, creates a hash table entry (key) for that, and assigns its frequency (value) to 1. This step is visualized in Fig. 7. If the k-mer is already in the table, it will calculate a new frequency (New_frq) by adding the previous frequency by one and update the value. As indicated, Hashmap procedure can be implemented through PANDA_Cmp (comparison), PANDA_Add (addition), and PANDA_Mem_insert (memory W/R) in-memory operations. Such functions are iteratively used in every step of for loop and PANDA is specially designed to handle such computation-intensive load through performing comparison, summing, and copying operations.

![Figure 6. The genome assembly stages.](image)

![Figure 7. The hash table generation out of k-mers.](image)
of k-mer (980 rows) vectors, where each row stores up to 128 bps (A,C,G,T encoded by 2 bits) and value (32 rows) vectors in the same sub-array. For counting the frequencies of each distinct k-mer, the ctrl first reads and parses the short reads from the original sequence bank to the specific sub-array. As depicted in Fig. 8, assuming S=CGTGTGCA as the short read, the k-mers- k_{i-3}k_{i-2}, are extracted and written into the consecutive memory rows of k-mer region. However, when a new query such as k_{i-3}k_{i-2} arises (while k_{i-2}k_{i+1} are already in the memory), it will be first written to the temp region. A parallel in-memory comparison operation (PANDA_Cmp) will be performed between temp data and already-stored k-mers. Fig. 8 intuitively shows PANDA_Cmp procedure, where entire temp row can be compared with a previous k-mer row in a single cycle. Then, a built-in ctrl’s AND unit in DPU readily takes all the results to determine the next memory operation according to the algorithm. To increase the frequency of a specific k-mer, PANDA Add is leveraged to perform in-memory addition without sending data to off-chip processor.

**Algorithm 1 Procedure Hashmap(S, k)**

1. hashable named Hashmap = {}
2. Fill out the table:
   - for i = 0 to length(S)-k+1 do
     - \( k_{\text{mer}} \leftarrow S[i : i+k] \)  \( \rightarrow \) copy values of \( S[i] \) to \( i+k \) into variable \( k_{\text{mer}} \)
   - if PANDA_Cmp(k_{\text{mer}}, Hashmap) == 0 then
     - PANDA_Mem_insert(k_{\text{mer}}, 1)
   - else
     - New_fq \( \leftarrow \) PANDA_Add(k_{\text{mer}}, 1)  \( \rightarrow \) increment fq by 1
     - PANDA_Mem_insert(k_{\text{mer}}, New_fq)  \( \rightarrow \) insert into Hashmap again
   end if
end for
return Hashmap

Figure 9. Graph construction with sparse matrix with partitioning, allocation and parallel computation.

**Algorithm 2 Procedure DeBruijn(Hashmap, k)**

1. Get\[\].Nodes_List[], i=1
2. Sparse Graph Construction:
   - for \( k_{\text{mer}} \in \text{Hashmap.keys()} \), i++ do
     - node_1 \( \leftarrow k_{\text{mer}}[0 : k-2]
     - node_2 \( \leftarrow k_{\text{mer}}[1 : k-1]
     - PANDA_Mem_insert(G[1], node_1)
     - PANDA_Mem_insert(G[2], node_2)
     - PANDA_Mem_insert(G[3], Hashmap[k_{\text{mer}}])
   end for
   return G

To balance workloads of each PANDA’s chip and maximize parallelism, we leverage interval-block partitioning method. We use hash-based approach by splitting the vertices into \( M \) intervals and then divide edges into \( M^2 \) blocks as shown Fig. 9 (step 3: mapping). Then each block is allocated to a chip (step 4: allocation) and mapped to its sub-arrays. Having an \( m \)-vertex sub-graph with \( N_s \) activated sub-arrays (size=x \( \times y \)), each sub-array can process \( n \) vertices \((n \leq f|n \in N, f = \min(x,y))\) (step 5: parallel computation). In this way, the number of processing sub-arrays for an \( N \)-vertex sub-graph can be formulated as \( N_s = \lceil \frac{N}{f} \rceil \).

After graph construction, it is possible to perform a round of simplification on the sparse graph stored in PANDA without loss of information to avoid fragmentation of the graph. As
a matter of fact, the blocks are broken up each time a short read starts or ends leading to linear connected subgraphs [22]. This fragmentation imposes longer execution time and larger memory space. The simplification process easily merges two nodes within memory if a node-A has only one out-going edge directed to node-B with only one in-going edge.

### C. Stage Three: Traversal for Euler Path

The input of this stage will be a sparse representation of graph $G$. For traversing all the edges, we will use Fleury’s algorithm to find the Euler path of that graph (a path which traverses all edges of a graph). Basically, a directed graph has a Euler path if the in_degree and out_degree of every vertex is same or, there are exactly two vertices which have —in_degree - out_degree— = 1. Finding the starting vertex is very important to generate the Eulerian path and we cannot consider any vertex as a starting vertex. The reconstructed PIM-friendly algorithm for finding the start vertex in graph $G$ is shown in Algorithm 3. For each node, this stage deals with massive number of iteratively-used $PANDA\_Add$ to calculate the number of in_degree, out_degree and edge_cnt (total number of edges). Moreover, in order to check the condition (—out_degree = in_degree —= 1), parallel $PANDA\_Cmp$ operation is required.

After finding the start node, $PANDA$ has to traverse through the length of sparse matrix $G$ from the starting vertex and check two conditions for each edge and accordingly add qualified edges to the Eulerian Path. We show the reconstructed Fleury algorithm in Algorithm 4. If an edge is not a bridge and is not the last edge of the graph, we will add ($start, v$) in the Eulerian path and remove that edge. $isValidNextEdge()$ function will check if the edge $(u, v)$ is valid to be included into our Euler path. If $v$ is the only adjacent vertex remaining for $u$, it means that, we have traversed all other adjacent vertices, so we will take this edge, otherwise we wont. The second condition counts the number of reachable nodes from $u$ before and after removing the edge.

If the number changes/decreases, it means that, the edge was a bridge (removing it will disconnect the graph into two parts). If it is a bridge, we cannot remove the edge from our Graph; otherwise we will remove the edge and add it into Euler path.

### IV. PERFORMANCE Estimation

#### A. Setup

**Accelerator:** To the best of our knowledge, this work is the first to explore the performance of a PIM platform for genome assembly problem, therefore, we have to create the evaluation test bed from scratch to have an impartial comparison with both von-Neumann and non-von-Neumann architectures. We configure the $PANDA$’s computational memory sub-array with...
1024 rows and 256 columns, 4×4 memory matrix (with 1/1 as row/column activation) per bank organized in H-tree routing manner, 16×16 banks (with 1/1 as row/column activation) in each memory chip. For comparison, we consider five computing platforms: 1) A general purpose processor (GPP): a Quad Core Intel Core i7-7700 CPU @ 3.60GHz processor with 8192MB DIMM DDR4 1600MHz RAM and 8192KB Cache; 2) A processing-in-STT-MRAM platform capable of performing bulk bit-wise operations [39]; 3) A recently developed processing-in-SOT-MRAM platform for DNA sequence alignment optimized to perform comparison-intensive operations [3]; 4) A processing-in-ReRAM accelerator designed for accelerating bulk bit-wise operations [40]; 5) A processing-in-DRAM accelerator based on Ambit [7] working with triple row activation mechanism to implement various functions. The detailed evaluation framework developed for PIM platforms is shown in Fig. 11. All PIM platforms have an identical physical memory configuration as PANDA. Additionally, we developed a similar cross-layer simulation framework starting from device-level simulation all the way to circuit- and architectural level as explained for PANDA in Section II.D. The results of the architecture evaluation of all PIM platforms were then fed to a high-level in-house simulator developed in Matlab to perform each genome assembly stage based on our customized and PIM-friendly algorithm and estimate the overall performance. It is noteworthy that DPU was developed in HDL and the performance results was extracted with synopsys design compiler [41] and fed to the developed NVSim library for each PIM platform.

To evaluate the CPU performance, we use Trinity-v2.8.5 [23] which was shown to be sensitive and efficient in recovering full-length transcripts. Trinity constructs de Bruijn graph from short-read sequences and employs an enumeration algorithm to score all branches, and keeps possible ones as isoforms/transcripts.

**Experiment:** In our experiment, we create 60952 short reads through Trinity sample genome bank with 519771 unique k-mers. We initially set the k-mer length, k, to default 25, and then change it to 22, 27, and 32 as typical values for most genome assemblers. To clarify, the CPU executes the *Inchworm*, *Chrysalis*, and *Butterfly* steps in Trinity, while PIM platforms run three main procedures in genome assembly shown in Fig. 4 i.e. Hashmap, DeBruijn, and Traverse for under-test PIM platforms. We compare Trinity’s power consumption and execution time to that of other PIM assemblers by several measures. To have a fair comparison with such a comprehensive assembler (that performs full genome assembly task with scaffolding step), we penalized the PIM platforms with ~25% excessive time and power. We believe this could provide a more realistic comparison with a von-Neumann architecture-based assembler.

**B. Run Time**

The execution time of genome assembly task for different platforms is reported in Fig. 12. For k=25, the CPU platform executes the *Inchworm*, *Chrysalis*, and *Butterfly* steps of Trinity in ~32s, where Chrysalis for clustering the contigs and constructing complete de Bruijn graph takes the largest fraction of the run time (28s) as expected. However, the comparison operation-intensive Hashmap procedure for k-mer analysis takes the largest fraction of execution time in all PIM platforms (over 40% of total run time). Larger k-mer length typically diminishes the de Bruijn graph connectivity by simultaneously reducing the number of ambiguous repeats in the graph and chance of overlap between two reads. That is why run time for all platforms reduces with increase of k-mer length.

We can observe that PIM platforms reduce the run time remarkably compared to the CPU. As shown, PANDA reduces the run time by ~18× compared to the CPU platform for
The PANDA platform essentially accelerates the graph construction and traversal stages by \( \sim 21.5 \times \) compared with CPU platform. Now, by increasing the \( k \)-length to 32, the higher speed-up is even achievable. Compared with counterpart PIM platforms, our X(N)OR-friendly design reduces the run time on average by \( 4.2 \times, 2.5 \times \), compared to STT-PIM [39], and SOT-PIM [5] platforms as the fastest counterparts, respectively. This comes from the fact that under-test PIM platforms require multi-cycle operations to implement addition operation. Besides, the SOT-based device intrinsically shows higher write speed compared to STT devices. Compared to DRAM and RRAM platforms, PANDA achieves on average \( 10.9 \times \) and \( 6 \times \) speed-up for various length \( k \)-mer processing. It is worth pointing out that the processing-in-DRAM platforms possess a destructive computing operation and require multiple memory cycle to copy the operands to particular rows before computation. As for Ambit [7], 7 memory cycles are needed to implement in-memory-X(N)OR function.

**C. Power Consumption**

We estimated the power consumption of different PIM platforms for running different length \( k \)-mers compared to the CPU platform as shown in Fig. 13. Based on our results, a significant reduction in power consumption can be reported for all under-test PIM platforms compared with the CPU. The breakdown of energy consumption is also shown for the PIM platforms, however this couldn’t be accurately achieved for the CPU and overall power consumption is reported. In our experiment, processing-in-SOT-MRAM design [5] achieves the smallest power consumption (on average) to run the three main procedures, as compared with the CPU and other PIM platforms. The PANDA platform stands as the second most power-efficient design. This is mainly due to the three-SA based bit-line computing scheme in PANDA compared with two-SA per bit-line technique in the counterpart design. While the proposed scheme brings more speed-up compared with the design in [5], it requires relatively more power. The PANDA reduces the power consumption by \( \sim 9.2 \times \) on average compared with the CPU platform over different length \( k \)-mers. Besides, it reduces the power consumption by \( \sim 18% \) compared with STT-MRAM [39] platform. The main reason behind this improvement is more efficient addition operation in PANDA. Addition operation requires additional memory cycles in the STT-MRAM [39] platform to save carry bit back to the memory and use it again for the computation of next bits. Compared to DRAM and RRAM platforms, PANDA obtains on average \( 2.11 \times \) and \( 55% \) power reduction for various length \( k \)-mer processing.

**D. Speed-up/Power-Efficiency Trade-off**

We investigate the power-efficiency and speed-up of three best under-test PIM platforms, based on the run time and power consumption results in the previous subsections, by tuning the number of active sub-arrays (\( N_s \)) associated with the comparison and addition operations. A parallelism degree (\( P_d \)) can be then defined as the number of replicated sub-arrays to boost the performance of the PIM platforms through parallel processing as shown in prior works [5], [12]. For example, when \( P_d \) is set to 2, two parallel sub-arrays are undertaken to process the in-memory operations, simultaneously. We expect such parallelism to improve the performance of genome assembly at the cost of sacrificing the power consumption and area. Fig. 14 plots the existing trade-off between run time and power consumption vs. \( P_d \) for \( k=25 \). The estimated CPU power budget required to execute Trinity is also shown. It can be seen that for all platforms the run time reduces by increasing the parallelism. For example for PANDA platform in an extreme case, increasing \( P_d \) from 1 to 8 increases the power consumption from \( \sim 19W \) to 128W (\( \sim 7 \times \)) and reduces the execution time by a factor of 3, which might not be a favorable case. Therefore, a user can meticulously tailor the PANDA performance to meet the system/application constraints. Here, we show the optimum theoretical performance of PANDA and other PIM platforms by pinpointing the intersection between power and run time curves in Fig. 14. We observe that PANDA achieves the smallest run time and power consumption task with a \( P_d \sim 2 \) compared with the others.

**E. Memory Wall Challenge**

The power-efficiency and speed-up of PIM platforms against the von-Neumann architecture-based CPU was discussed in prior subsections. Here, we further explore the reasons behind the numbers reported by considering two new measures i.e. Memory Bottleneck Ratio (MBR) and Resource Utilization Ratio (RUR). We define MBR as the time fraction needed for data transfer from/to on-chip or off-chip, when computation has to wait for data i.e. memory wall happens. We also
define RUR as the time fraction in which the computation resources are loaded with data. The memory wall is considered as the main bottleneck that brings large power consumption and lengthen execution time in CPU. The MBR is reported in Fig. 15. The peak throughput for each design in four distinct k-mer lengths is taken into account for performing the evaluation. This evaluation mainly considers the number of memory access. As shown, the PANDA uses less than ~17% time for data transfer due to the PIM acceleration schemes, while CPU’s MBR increases to 65% when k=25. Besides, we observe that all the other PIM platforms except DRAM also spend less than ~17% time for data communication. The smaller MBR can be translated as the higher RUR for the accelerators plotted in Fig. 15b. The less MBR can be understood as a higher RUR. We can see that with up to ~82%, PANDA achieves the highest RUR. Taking everything into account, PIM acceleration schemes offer a high utilization ratio (>60% excluding DRAM) confirming the conclusion drawn in Fig. 15a. The memory wall evaluation shows the efficiency of the PANDA platform for solving memory wall challenge.

![Memory Bottleneck Ratio and Resource Utilization Ratio](image)

**Figure 15.** (a) The memory bottleneck ratio and (b) resource utilization ratio for CPU and three under-test PIM platforms for running genome assembly task.

V. CONCLUSION

In this paper, we presented PANDA as a new processing-in-SOT-MRAM platform to accelerate the comparison/addition-intensive genome assembly application using PIM-friendly operations. We developed PANDA based on a set of new circuit-level schemes to realize a data-parallel computational core for genome assembly. The platform is configured with a novel data partitioning and mapping technique that provides local storage and processing to fully utilize our customized algorithm-level’s parallelism. The cross-layer simulation results demonstrate that PANDA reduces the execution time and power respectively by ~18× and ~11× compared with the CPU. Besides, speed-ups of up-to 2-4× can be obtained over recent processing-in-MRAM platforms to perform the similar task.

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