Flexible control for power-sharing in the CHB-based SST under voltage unbalance conditions

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Abstract
Solid-state transformers (SSTs) have flexible capabilities to improve the power quality issues. These improvements impose disturbances into the SST converters that require proper control algorithms. In this paper, the problems of the unequal active power flow in different phases of the SST due to the grid voltage unbalance conditions and the negative sequence current injection are discussed, and an effective method is proposed to equally sharing the active powers between the SST clusters by creating an optimum zero sequence current. Based on the power dependencies, an analytical vector for the zero-sequence current is proposed, which can equally share the power among the SST clusters and balance the HVDC-link voltages. Also, the proposed control strategy by using PIR controllers can achieve the zero-sequence current based on a direct current control method. The provided equal power-sharing among the clusters is kept in the considerable unbalanced voltage of the grid and prevents the SST outage during faults. The simulation and experimental results confirm the proposed control method to equalise the power-sharing among the SST clusters and voltage equalisation of the HVDC-links while the SST tries to improve the grid voltage unbalance and in the fault conditions of the grid.

1 INTRODUCTION

Solid state transformers (SSTs) are flexible power electronic equipment whose applications are rapidly growing. They can improve the power quality issues of the distribution networks on both sides. The SST applications are very diverse such as distribution networks, renewable energies, electrical railway transportation systems, smart and microgrids, and electric vehicle charging stations [1–4]. The SST can provide extra benefits compared to a traditional transformer in terms of power quality and controllability such as reactive power compensation, harmonic elimination, voltage unbalance improvement, voltage regulation, power factor correction, and fault current limitation [5–7]. The SSTs topologies depend on the number of their stages can be classified into different groups. One, two, and three stages are commonly proposed and the three-stage topology is much more attractive because of high controllability [8]. Cascaded H-bridge (CHB) converters and modular multi-level converters (MMC) are generally used for the high-voltage side of the SSTs [9, 10]. The voltage unbalance is one of the power quality problems which should be limited to less than 2% according to IEEE-1459-2010 and IEC 61000-3-13 in a medium voltage grid. Up to now, many cases of the grid voltage unbalances, outside of the standard definition, have been reported [11, 12]. The voltage unbalance is generally created by single-phase loads in the steady-state conditions and shown in fault occurrence or single-phase load starting in the transient conditions. The negative sequence component of the voltage unbalance is transmitted to the medium voltage through the distribution transformer. The SSTs not only do not transmit the unbalanced currents from the low-voltage output loads but also can improve the voltage unbalance condition of the medium-voltage (MV) grid by injecting a proper negative sequence (ns) current. In other words, The SSTs can improve the voltage unbalance factor (VUF) of a point of common coupling (PCC) in the MV grids like an active filter [13]. The voltage unbalance conditions or the ns current injection create unbalanced currents in the different phases of the SST first stage converters, which lead to some problems. These unbalanced currents cause unequal active power-sharing among the different
clusters. In a CHB based STATCOM (or no load SST), unequal power-sharing leads to unequal voltages in HVDC-link capacitors. Therefore, the modulation index decreases or increases significantly, which leads to an increase in the THD of the output currents. An excessive increase in capacitor voltage can also damage the capacitor or semiconductor switches [14, 15]. In the loaded SST, the unbalanced grid voltage and the SST current causes unbalanced active power flow in the different clusters (first and second stages). This becomes more important at higher loads because of the limitation of the current capacity of each cluster. Therefore, the total active power capacity of the SST is significantly reduced in these conditions. Besides, the unequal active power flow creates unequal heat distribution in the different clusters [16]. Various methods have been proposed to balance the voltages of the HVDC-link capacitors in CHB-based converters. In [17], the voltage of the HVDC capacitors can be balanced by estimating the zero sequences (zs) current in a delta connected CHB-based STATCOM. This current is calculated by estimating the active power with the presence of the zs current in each phase without considering the voltage unbalance condition of the grid. In another study, by changing the structure and connections in the DC–DC stage of a largescale CHB-based PV power plant converters with Y connection, the problem of unbalanced production in the different phases has been solved, but this method cannot be implemented for SSTs because of considerable differences in their topologies [18]. In the method presented in [19], unbalance grid voltage, and unbalanced current injection for the VUF compensation are not considered for CHB PV converter and DC capacitor voltage equilibrium is analysed for normal network operation. In another method, by adjusting the voltage of the DC-link capacitors of a Y connected STATCOM to the desired values, a balanced modulated voltage with the maximum modulation index has been created [20]. In this method, the reference voltage of the HVDC-link capacitors of the different phases is obtained by using the ns and zs of the PCC voltage. Then, the equally active power flow in the different phases is performed by a determined zs voltage. In other solutions, by estimating a suitable zs voltage, the DC capacitors voltages of a CHB-based STATCOM are equalised in the event of an unbalanced condition or a faulty grid, however, in these studies, the ns current injection was not considered [21–23]. In this paper, the unequal power sharing in the first and second stages of the CHB-based SST is analysed by considering the grid voltage unbalance condition and the unbalanced current injection into the grid. Then, an effective control system is proposed to share the SST active powers at different operating points. In this method, the desired zero sequence current has been calculated based on extracted relations of the active powers in the voltage unbalance condition. This control method creates equal power-sharing in the SST clusters, voltage balancing of the HVDC-link capacitors, equal heat sharing in the second stage converters, and reduces the output current distortion of the SST as the novelties of this paper. Simulation and experimental results based on a similar platform confirm the ability of the proposed control method.

2 | THREE-STAGE CHB-BASED SSTs

The CHB-based SSTs because of the control flexibility, modular capability, and a classical form of configuration are a reasonable option, and the three-stage SSTs have many capabilities to improve the power quality of the grids. This type of SSTs is composed of an MV AC/DC stage, an isolation DC/DC stage, and an LV DC/AC stage, that enables input/output current control-ability, guarantees four-quadrant power flow, and as a result, provides the system control more degrees of freedom [24–26]. Therefore, many researchers have been focused on different structures of the three-stage SSTs.

2.1 | Three-stage SST configuration

In the first stage of the SSTs due to the high input voltages, series HB converters are used and the voltages are divided among the series HB cells. Figure 1 shows a modular three-stage CHB-based SST that is considered in this paper. There are delta connections of the three single-phase converters in the input stage (first stage). Lower rated current, non-aligned switching pattern, and independent to null wire/point are the main advantage of the delta connection in this configuration.

Dual active bridges (DABs) change the DC high voltage of the first stage to a lower level DC voltage at the end of the second stage. Isolated high-frequency DC/AC and AC/DC converters are utilised to transform the HVDC to LVDC. These converters have bidirectional power transferability. The LVDC is converted to a three-phase four-wire AC voltage to supply low voltage loads by the third stage. To avoid the effects of the output unbalanced loads on power-sharing of the first and second stages, the LVDC capacitors parallelisation of the DAB converters is suggested [27]. The LVDC is converted to a three-phase four-wire AC voltage to supply output low voltage loads by the third stage. These loads are usually single-phase and unbalanced, so the system needs a null wire. One of the suitable structures is a four-wire voltage source inverter (VSI) based on full-bridge (FB) or multilevel neutral-point clamped (NPC) structures that are selected for the third stage in this research.
VOLTAGE UNBALANCE EFFECT ON POWER-SHARING OF THE SST CLUSTERS

2.2 Basic control schemes for first stage of the SST

The control system of the first stage is the most important part of the SST control structure. This stage is connected to a medium voltage grid and is synchronised with the grid voltage. The control strategies have to control active and reactive powers. Moreover, they can be designed to reduce the low-frequency harmonics and the grid VUF [28]. The control of the HVDC-link voltage is one of the inevitable purposes for a practical control algorithm. The next control objective is the requirements of the output current based on the power quality conditions of the PCC. The block diagram of the fundamental control system of the first stage is shown in Figure 2. Starred parameters represent the reference values and the + sign represents the positive sequence (ps) components. The PS and NS subscripts represent the positive sequence reference frame (+ωt) and the negative sequence reference frame (−ωt), respectively. \( v_{sst,PS}^g \) and \( v_{sst,NS}^g \) are the first stage of the SST reference voltages, \( i_{sst,PS}^{d} \) and \( i_{sst,NS}^{d} \) are the \( dpq \) component of the SST first stage current, \( i_{sst,PS}^{q} \) and \( i_{sst,NS}^{q} \) are the \( dq \) component of the grid voltages in \( dpq \) reference frame, and \( \omega \) is the grid angular frequency. In this process, \( i_{sst,PS}^{d} \) and \( i_{sst,NS}^{d} \) control the HVDC-link voltage and the reactive power, respectively. The \( zs \) component of the SST current \( (i_{sst}^{0}) \) is controlled by the \( zs \) component of the voltage \( (v_{sst}^{0}) \), which is usually used to eliminate this component. The three-phase reference voltages can be easily determined by park inverse transform and applied to the SST first stage.

3 VOLTAGE UNBALANCE EFFECT ON POWER-SHARING OF THE SST CLUSTERS

Unequal single-phase and unbalanced three-phase loads are the main factors for the voltage unbalance in the distribution networks. Grid-connected converters with a suitable control can decrease the VUF when their currents are lower than the nominal current and they have an unused current capacity. The principles of compensation control methods are based on \( zs \) current injection; however, the \( zs \) current amplitude is limited by the operating point of the SST. It is initially assumed that there is no \( zs \) current component in the SST currents. Figure 3 shows vector diagrams of the grid voltages and the SST currents under the unbalanced grid voltage conditions. Based on these diagrams, the active powers in the different phases are simply calculated as follows:

\[
P^{AB} = Re \left\{ v_{g,PS}^d + I^+ e^{\phi} + I^- e^{-\phi} \right\}
\]

\[
P^{BC} = Re \left\{ v_{g,PS}^d + I^+ e^{\phi} + I^- e^{-\phi} \right\}
\]

\[
P^{CA} = Re \left\{ v_{g,PS}^d + I^+ e^{\phi} + I^- e^{-\phi} \right\}
\]

where \( u \) is the per-unit ns value of the grid voltage. By converting the above relations from polar to Cartesian coordinates and extracting real terms, the active powers can be achieved from Equation (2).

\[
P^{AB} = v_{g,PS}^d + l^{-}.\cos(\gamma) + u. I^+.\cos(\gamma - \phi)
\]

\[
P^{BC} = v_{g,PS}^d + l^{-}.\cos(\gamma - \frac{2\pi}{3}) + u. I^+.\cos(\gamma - \phi)
\]

\[
P^{CA} = v_{g,PS}^d + l^{-}.\cos(\gamma - \frac{2\pi}{3}) + u. I^+.\cos(\gamma - \phi)
\]

Equal power-sharing in the different phases of the SST is defined according to Equation (3).

\[
P^{AB} = P^{BC} = P^{CA}
\]
Based on Equations (2) and (3), in order to equal power-sharing among the SST clusters, the desired $ns$ current components are determined by Equations (4) and (5).

\[ I^-.cos(\theta^-) = -u.I^+.cos(\theta^+ - \phi) \]  \tag{4}

\[ I^- .sin(\theta^-) = -u.I^+.sin(\theta^+ - \phi) \]  \tag{5}

By decomposition the above relations and using the components of positive and negative sequences of the grid voltage and the SST current in PS and NS reference frames, Equations (4) and (5) can be rewritten as follows:

\[ I^p_{NS} = [-v^-_{gNS}.I^p_{PS} - v^-_{NS}.I^p_{PS}] \]  \tag{6}

\[ I^-_{NS} = [-v^-_{gNS}.I^+_{PS} + v^-_{NS}.I^+_{PS}] \]  \tag{7}

where $v^p_{gNS}$ and $v^-_{gNS}$ are the per-unit $dq$ ns components of the grid voltage vector in the $-\omega t$ reference frame, $I^p_{PS}$ and $I^+_{PS}$ are the $dq$ components of the SST ps current in $\omega t$ reference frame, and $I^p_{NS}$ and $I^-_{NS}$ are the $dq$ components of the SST ns current in $-\omega t$ reference frame. Based on these analyses, the active powers in the different clusters are equalised only by applying the $ns$ current vector from Equations (6) and (7), and the active powers are not equal while another ns current vector is injected into the grid under the voltage unbalance conditions.

4 | ANALYTICAL STRATEGY FOR EQUAL POWER-SHARING

To achieve equal distribution of the active powers, a zs current vector with amplitude $I^0$ and angle $\theta^0$ in the delta connected converters is assumed while a ns current is injected into the grid to reduce the PCC unbalanced voltages (Figure 4). In this condition, the active powers in the different phases of the SST are calculated according to Equation (8).

\[ P^{AB} = Re\{v^d_{gPS}(1 + ne^{j(\theta^0 + \beta)}), (I^+e^{j\phi} + I^-e^{j(\theta^- + \phi)} + I^0e^{j(\theta^0 + \beta)})\} \]

\[ P^{BC} = Re\{v^d_{gPS} \left( 1 + ne^{j(\theta^0 - \frac{2\pi}{3})} \right), 
(\frac{I^+e^{j\phi} + I^-e^{j(\theta^- - \frac{2\pi}{3})} + I^0e^{j(\theta^0 + \frac{2\pi}{3})}}{3}) \} \]  \tag{8}

\[ P^{CA} = Re\{v^d_{gPS} \left( 1 + ne^{j(\theta^0 + \frac{2\pi}{3})} \right),
(\frac{I^+e^{j\phi} + I^-e^{j(\theta^- + \frac{2\pi}{3})} + I^0e^{j(\theta^0 - \frac{2\pi}{3})}}{3}) \} \]

By equating the active powers and solving them based on $I^0$ and $\theta^0$, the orthogonal components of the zs current are obtained as follows:

\[ I^{0\cos\theta^0} = \beta (1 - v^-_{gNS}) - \alpha I^+_{gNS} \]  \tag{9}

\[ I^{0\sin\theta^0} = \alpha - v^-_{gNS}.I^{0\cos\theta^0} - \frac{1}{1 - v^-_{gNS}} \]  \tag{10}

where:

\[ \alpha = v^+_{gNS}.I^{0\sin\theta^0} - v^-_{gNS}.I^{0\sin\theta^0} + v^0_{NS} \]  \tag{11}

\[ \beta = -v^0_{NS}.I^+_{PS} - v^-_{NS}.I^+_{PS} - v^0_{NS} \]  \tag{12}

Therefore, in the time domain, the instantaneous value of the proper zs current for equal active power-sharing is calculated as follows:

\[ i^0(t) = I^0\cos(\omega t + \theta^0) = I^0\cos\theta^0\cos(\omega t) - I^0\sin\theta^0\sin(\omega t) \]  \tag{13}

Power-sharing among the converters are achieved by injecting this zs current into the $\Delta$ connection of the SST first stage. For very small values of the voltage unbalance factor, VUF $\approx 0$ and then $|I^0| = |I^-|$ and $\theta^0 = \pi - \theta^-$. In this condition, the desired zs current is simply calculated by Equation (14).

\[ i^0(t) = |I^-|\cos(\omega t + \pi - \theta^-) \]  \tag{14}

5 | PROPOSED CONTROL STRATEGY TO SHARING POWERS

Equal power-sharing and HVDC-link voltages balancing are of the same concept. The second and third stage equivalent circuit of the SST is shown in Figure 5 to express this concept.
According to this figure, the HVDC-link voltages are determined by Equation (15).

\[ V_{\text{HVDC}}^{\text{out}} = V_{\text{LVDC}}' + Z_{\text{DAB}} i_{\text{avg}}^{\text{out}} \]  

where \( Z_{\text{DAB}} \), \( V_{\text{LVDC}}' \) and \( i_{\text{avg}}^{\text{out}} \) (\( \gamma \gamma \gamma \): AB, BC, CA) are equivalent impedances of the second stage, the transferred LVDC voltage and output average current of the second stage to the primary side, respectively. By assuming that the leakage impedances of the high-frequency transformer in the different clusters are equal, clusters with the higher HVDC-link voltage have the more average DC current and consequently have more active power.

By injecting the zero-sequence current from Equation (13) to the delta connection clusters, equal active power flow can be created. Immediately after calculating Equation (13), the zero-sequence current is applied to the first stage converters, so a high-speed operation can be expected by this method. However, an accurate and fast calculation of Equation (13) depends on the accuracy of the voltage and current sensors as well as the PLL system to determine the voltage components of the grid. Also, feed-forward utilisation and power losses of the SST inductors and switching in the first-stage converters can create a slight error in the power-sharing process which is negligible. According to Figure 5, the transferred active power \( P_{\text{out}}^{\gamma\gamma\gamma} \) as the output power of the first stage through each cluster of the second stage is achieved by Equation (16).

\[ P_{\text{out}}^{\gamma\gamma\gamma} = V_{\text{HVDC}}^{\gamma\gamma\gamma} \left( \frac{V_{\text{HVDC}}^{\gamma\gamma\gamma} - V_{\text{LVDC}}'}{Z_{\text{DAB}}} \right) \]  

Therefore, the voltage variation of HVDC capacitors in each phase according to the input and output active powers is determined as follows:

\[ (\Delta V_{\text{HVDC}}^{\gamma\gamma\gamma})^2 = \frac{2}{C_{\text{HVDC}}'} (P_{\text{in}}^{\gamma\gamma\gamma} - P_{\text{out}}^{\gamma\gamma\gamma}) \]  

If \( P_{\text{in}}^{\gamma\gamma\gamma} > P_{\text{out}}^{\gamma\gamma\gamma} \), the \( \Delta V_{\text{HVDC}}^{\gamma\gamma\gamma} \) will increase over time, and based on (16), \( P_{\text{in}}^{\gamma\gamma\gamma} \) is incremented up to \( P_{\text{out}}^{\gamma\gamma\gamma} \). Also, if \( P_{\text{in}}^{\gamma\gamma\gamma} < P_{\text{out}}^{\gamma\gamma\gamma} \), the \( P_{\text{out}}^{\gamma\gamma\gamma} \) will decrease over time until \( P_{\text{in}}^{\gamma\gamma\gamma} = P_{\text{out}}^{\gamma\gamma\gamma} \). In other words, the active power flows in the second-stage clusters confirm the stability of the HVDC capacitor voltages as an effective control for underload SSTs. Based on the proposed method, the zs current reference is replaced from zero to the obtained value from Equation (13) in Figure 2. Also, the zs component of the fundamental SST currents oscillates by the power frequency of the network. Hence, a 50 Hz resonance controller is added to the PI controller as a PIR controller with the following transfer function.

\[ T(s) = \frac{k_p + \frac{k_i}{s}}{s^2 + \omega_n^2} \]  

where \( s \) is the Laplace operator and \( k_p, k_i \) and \( k_r \) are proportional, integral, and resonance controller factors, respectively.

Unbalanced currents in the different clusters of the second stage increase power losses, which include two switching and conduction losses. According to Figure 5, the dependence of the switching losses \( P_{\text{sw}} \) in the second-stage converters on the cluster currents can be expressed as follows:

\[ P_{\text{sw}} \propto \left[ (V_{\text{AB}}' i_{\text{avg}}^{\text{AB}} + V_{\text{BC}}' i_{\text{avg}}^{\text{BC}} + V_{\text{CA}}' i_{\text{avg}}^{\text{CA}}) + V_{\text{diode}}' (i_{\text{avg}}^{\text{AB}} + i_{\text{avg}}^{\text{BC}} + i_{\text{avg}}^{\text{CA}}) \right] \]  

where \( V_{\text{diode}}' \) is the forward voltage drop on diodes of the second stage rectifier. Also, at a certain operating point, the output active power of the SST from Equation (20) is constant.

\[ P_{\text{out}} = V_{\text{LVDC}}' (i_{\text{avg}}^{\text{AB}} + i_{\text{avg}}^{\text{BC}} + i_{\text{avg}}^{\text{CA}}) \]  

The sum of the cluster currents is constant because \( P_{\text{out}} \) and \( V_{\text{LVDC}}' \) are constant, and according to Equation (19), it can be concluded that the unbalanced currents do not affect the switching losses in the converters. The conduction losses \( P_{\text{cond}} \) of the power semiconductors and HF transformer windings are proportional to the quadratic of the cluster currents based on Equation (21), and these losses are minimised when the cluster currents are equal.

\[ P_{\text{cond}} \propto (i_{\text{avg}}^{\text{AB}})^2 + (i_{\text{avg}}^{\text{BC}})^2 + (i_{\text{avg}}^{\text{CA}})^2 \]  

As a result, any unbalance current in different clusters will lead to increased conduction losses and thus reduce the overall efficiency of the system. Therefore, the proposed method minimises the conduction losses of the second-stage converters by balancing the \( i_{\text{avg}} \) currents. Figure 6 shows the control block diagram of the proposed DZCC method. The \( i_{\text{in,PS}} \) and \( i_{\text{out,PS}} \) are the ns current vectors in the synchronous reference frame which are added to the first stage of the SST control system. These vectors are created by a separate control section to compensate VUF with 100 Hz frequency according to [28]. Therefore, a PIR controller with a resonance
TABLE 1  The technical specification of the SST

| Parameters                  | value     |
|-----------------------------|-----------|
| SST nominal power           | 6 kVA     |
| SST input line to line voltage | 400 V   |
| Grid VUF                    | 2.6 %     |
| SST output line to line voltage | 110 V   |
| Power system frequency      | 50 Hz     |
| Connection type of the SST first stage | Delta (Δ) |
| Number of modules in a cluster | 3       |
| Number of first stage voltage level | 7       |
| SST HVDC-link voltage       | 3×233 V   |
| SST LVDC-link voltage       | 200 V     |
| Switching frequency         | 10 kHz    |
| Microprocessor              | ARM and FPGA |

frequency of 100 Hz is used to simultaneously control the ps and ns components of the current in the synchronous reference frame. In this proposed control method, there is no need to separate the ps and ns components of the measured currents, and the positive and negative sequence components of the current are controlled simultaneously using this PIR controller.

6  | SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed control system is evaluated by simulation and experimental tests by using a three-stage SST setup that its specifications are presented in Table 1 for both simulation and the laboratory systems, and the SST laboratory setup is shown in Figure 7. In order to better compare the results, the specifications of the simulation in the MATLAB Simulink and laboratory system were selected as similar as possible. The ns current injection to compensate the VUF, and the voltage unbalance condition due to the grid faults are the main objectives of the tests to evaluate the power-sharing ability of the proposed method. A three phase, 3 kW, wye-connected load is fed by the SST, and \( i_{\text{sst,NS}}^{+*} \) is adjusted to 4 A. These values are selected according to the SST capacity and significant variations to investigate the dynamic responses of the control system. The following five time intervals are considered to illustrate the performance of the method in the grid voltage unbalance compensation condition.

- Step 1 \( (t_0 \leq t < t_1) \): In both simulation and experiment process, the system starts without any ns current;
- Step 2 \( (t_1 \leq t < t_2) \): At \( t_1 = 2 \text{ s} \), \( i_{\text{sst,NS}}^{*} = 4\pi/2 \) is applied to the SST;
- Step 3 \( (t_2 \leq t < t_3) \): From \( t_2 = 4 \text{ s} \) the proposed control system is activated;
- Step 4 \( (t_3 \leq t < t_4) \): The phase angles of the ns current vector is changed from \( \pi/2 \) to \( \pi/6 \) at \( t_3 = 6 \text{ s} \);
- Step 5 \( (t_4 \leq t < t_5) \): The phase angles of the ns current vector is replaced by \( 5\pi/6 \) at \( t_4 = 8 \text{ s} \);

Figure 8 shows the phase and amplitude of the ns current reference in the test process according to the mentioned time intervals. As can be seen from this figure, the VUF of the laboratory local grid has dropped from 2.6% to 1.7% by the injected ns current at \( t_1 \).

Figure 9 shows the simulation results of the SST with the proposed control system under the categorised ns current injection. In step 1, the average output currents of the second stage \( i_{\text{avg}}^{(y)} \) in the different clusters are approximately equal to 5.2 A, and the average voltage of the HVDC capacitors

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FIGURE 6  The main control structure of the proposed method

FIGURE 7  Laboratory setup of the three-stage 6 kVA SST

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(V_{HVDC-avg}) is approximately 233 V, and also the average active powers of the first stage converters in each phase ($P_{in}^{CA}$) are approximately 1100 W, which are reasonable values by considering the converters losses of the different stages. By injecting the ns current at $t_1$, the average output currents of the second stage, the average voltage of the HVDC-links, and the average active powers become different as shown in Figure 9(a-c), respectively. According to Figure 9(a), in the step 2, $P_{avg}^{BC}$ increases to more than 9 A, while $P_{avg}^{CA}$ reduces less than 1 A. As shown in Figure 9(e), $P_{avg}^{CA}$ is approximately 7.2 times of $P_{avg}^{CA}$ that not only limits the power flow in the overload clusters but also disturbs the thermal balancing of the SST converters. After activating the proposed control system at $t_2$, they converge in an acceptable trend in the different angles of the injected ns current vectors, and by changing the phase angle of the ns current vector to $\pi/6$ and $5\pi/6$ at $t_3$ and $t_4$, the proposed control system quickly unifies the powers and the voltages. According to Equation (21) and Figure 9(a), when the proposed control system is activated in step 3, the conduction losses of the second stage converter are about 33% less than in step 2, when the proposed control system is inactive.

Figure 9(d) depicts the phase currents of the SST along with the created zs currents in the $\Delta$ connected converters during step 3. In fact, this zs current adjusts the active power flow and the HVDC-link voltages in the different clusters according to Equation (13). Figure 9(e) shows the reference and actual zs currents as well as the reference of the zs voltage, that generated by the PIR controller block with a focus on the activation time ($t_2$). As seen in this figure, the actual zs current tracks the reference current quickly that approves the fast response of the control process. There is no control over the zs current ($I_{avg}^{sat}$) and it includes an intrinsic zs current along with the third multiple harmonic before $t_2$. Also, instantaneous values of the HVDC capacitors voltage are presented in Figure 9(f) which show the proper and fast performance of the proposed control system in voltage balancing of the HVDC capacitors. It can be seen that in less than 10 ms, the capacitor voltages have reached equilibrium and their average values have converged to 233 V.

Experimental results to evaluate the performance of the proposed method are given in Figures 10 and 11. After each change in the ns current vector in the mentioned five steps, the presented control system has properly balanced the clusters average currents and the average voltage of the HVDC-links as seen in Figure 10(a, b), respectively. According to Figure 10(c, d), the amplitude and angle of the zs current nearly follow the amplitude and $\pi - \theta^z$ of the ns current to improve the powersharing, respectively. This means that the approximation of zs current by Equation (14) can reasonably be reliable. Between $t_1$ and $t_2$ when the balancing control system is not active, the zs current vector is not large enough to cause a perfect equilibrium in the active power flow as seen as in Figure 10(c). When the proposed control system is activated, the amplitude of the zs current vector changes according to Equation (13) and balances the active powers flow in the SST clusters. Figure 11(a) shows the created zs current based on Equation (13) and the consequent three-phase SST currents to balance the active powers and HVDC-link voltages in the laboratory test, which are similar to Figure 9(d) in the simulation results. The fast response of the control system to following the zs current reference is clear from Figure 11(b) in the experiment, which is similar to Figure 9(c) in the simulation results.

The ns current injection by the grid-tie converters causes oscillations with twice the power frequency on the active and reactive power characteristics. The PIR controllers properly follow the $dq$ reference components of the SST currents ($d\dot{q}_{sst}^{PS}$, $d\dot{q}_{sst}^{PS}$) to create and inject the desired ns current based on Figure 11(c) and its laboratory counterpart in Figure 11(d). It can be seen that the PIR controllers in the control structure of Figure 6 are very fast and suitable for following the reference values in both the simulation and experimental tests. In the next part of the evaluation, the reaction of the proposed control method is investigated under fault conditions. It is assumed that the SST works under the voltage unbalance condition of the grid with VUF=2.6%, without the ns current injection. A line-line fault happens in the grid from $t_{f1} = 2s$ to $t_{f2} = 4s$ as a VUF of 69% is created in PCC of the SST. Figure 12(a,b) show the instantaneous and average values of the HVDC capacitors voltage, respectively. As expected, the voltage balance of the capacitors is disturbed under the fault condition, and the active powers in the different phases of the SST become unequal according to Figure 12(c). Obviously, with the elimination of the fault, the situation returns to the normal state. The test process is repeated by considering the proposed control system to evaluate the method for significant values of the VUF. Figure 12(d, e) depict the instantaneous and average values of the HVDC capacitors voltage at $t_{f1}$ again. According to these figures, the proposed control system maintains the voltage balancing of the HVDC capacitors under the fault conditions. Also, the active powers of the SST clusters are converged before, during, and after the fault based on Figure 12(f). This indicates that without a proper control method, the active power of some clusters will be overloaded under fault conditions, which will cause the SST to be disconnected from the grid.

7 | CONCLUSION

SSTs can improve voltage unbalance conditions in the distribution grids by injecting a controlled negative sequence current. For this purpose, they need multi-objective, fast, and flexible control algorithms to be able to correct the voltage unbalance...
FIGURE 9 Simulation results: (a) average output currents of the second stage in the different clusters, (b) average voltage of the HVDC capacitors in the different phases, (c) average active power of the different phases of the SST first stage, (d) phase currents of the SST along with the zs currents in the Δ connected input converters during the step 3, (e) reference and actual zs currents and the zs voltage reference around $t_2$, (f) instantaneous value of HVDC capacitors voltage of the different phases around $t_2$

FIGURE 10 Experimental results: (a) average output current of the second stage in the different clusters, (b) average voltage of the HVDC capacitors in the different phases, (c) magnitude of the zs and ns current vectors, (d) phase angle of the zs and ns current vectors
FIGURE 11  Experimental results: (a) phase currents of the SST along with the zs currents in the Δ connected input converters during the step 3, (b) reference and actual zs currents around t₂; (c) simulation and (d) experimental results of the dq reference and actual current of the SST

FIGURE 12  SST under the fault condition without (and with) the proposed control algorithm: (a) and (d) HVDC-links voltages waveform, (b) and (e) average voltage of the HVDC-links, (c) and (f) average active powers flow among the SST clusters
situation of the grid along with other features. In this paper, the unequal power-sharing problem has been presented when the SST is under the grid unbalanced voltage, fault condition, or tries to improve the voltage unbalance condition of the grid by injecting negative sequence currents. An exclusive zero-sequence current vector is proposed to apply in the first stage converters in order to equal sharing the active powers and balancing the HVDC-link voltages. It has been shown that by equalising the powers, more capacity is created to improve the voltage unbalance, and also the power loss in the SST converters is reduced. The simulation and experimental results approve the abilities of the proposed method to create equal power-sharing in the SST clusters, voltage balancing of the HVDC-link capacitors, and equal heat sharing in the second stage converters. Under laboratory voltage unbalance conditions, the difference between the active powers of the clusters is more than 7.2 times without using the proposed method, which significantly limits the SST capacity, and by using this method, the active powers and the HVDC link voltages converge acceptably. According to the results, the presented control algorithms prevent outages of the SST because of the unequal power-sharing and overload of some clusters under the grid fault conditions. This method can be implemented to other same grid-tie converters such as CHB-based STATCOMs, active power filters, and renewable energy converters.

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