Analysis and evaluation of coupling between adjacent TSVs with considering the discharging path

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Abstract: Different from the conventional way to investigate the coupling between adjacent TSVs, we take the discharging path into consideration as the impedance of silicon substrate is actually finite. This paper first analyzes the discharging path which exists between the victim TSV and the silicon substrate, and then by transforming the tapped capacitor circuit into a RC parallel circuit for the discharging path, the frequency-dependent expressions of the parasitic elements in the discharging path are obtained. Furthermore, we vary the impedance of silicon substrate to evaluate the impact of discharging path on the coupling noise. Through simulations, it indicates that the coupling noise on the victim can be reduced significantly by lowering the impedance of discharging path.

Keywords: 3D integration, through silicon via (TSV), coupling noise, discharging path, doping concentration

Classification: Integrated circuits

References
[1] D. W. Kim, R. Vidhya, B. Henderson, U. Ray, S. Gu, W. Zhao, R. Radojcic and M. Nowak: Proc. of ECTC (2013) 77. DOI:10.1109/ECTC.2013.6575553
[2] M. Wordeman, J. Silberman, G. Maier and M. Scheuermann: ISSCC Dig. Tech. Papers (2012) 186. DOI:10.1109/ISSCC.2012.6176968
[3] P. M. Yaghini, A. Eghbal, M. Khayambashi and N. Bagherzadeh: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. (2015). DOI:10.1109/TVLSI.2014.2379263
[4] A. E. Engin and S. R. Narasimhan: IEEE Trans. Electromagn. Compat. 55 (2013) 149. DOI:10.1109/TEM.C.2012.2206816
[5] Y. Peng, T. Song, D. Petranovic and S. K. Lim: Proc. of ICCAD (2013) 281. DOI:10.1109/ICCAD.2013.6691133

1 Introduction
Stacking dies with through silicon vias (TSVs) is recognized as a promising technology for 3D integration as TSVs provide the short interconnect length
between stacked dies, which reduces the time delay, the power dissipation and the area overhead of 3D ICs [1, 2]. However, since the TSV is a vertical via filled with metal which buries in the silicon substrate, the coupling noise induced by the TSV is non-negligible and should be fully investigated. Previous literatures [3, 4] reported about the TSV coupling consider the silicon substrate which covers around the TSV is in a state of floating, and thus charges around the victim TSV is unable to be discharged through the silicon substrate to the ground. In practical, the impedance of silicon substrate is finite, and it is essential to analyze and evaluate the coupling with considering the discharging path [5]. Otherwise, the coupling noise on the victim TSV will be overestimated.

In this paper, we first analyze the discharging path of the victim TSV, and then by transforming the tapped capacitor circuit into a \( RC \) parallel circuit for the discharging path, the frequency-dependent expressions of the parasitic elements in the discharging path are obtained. Furthermore, we adjust the impedance of discharging path to evaluate the impact of discharging path on the coupling noise.

2 Analysis of the parasitic elements in the discharging path

In 3D ICs, the TSV penetrates the entire silicon substrate to provide a vertical interconnect, and thus this usually leads to a more complicated coupling environment compared with traditional 2D interconnect. Moreover, the permittivity of the inter-metal dielectric (IMD) material in 2D circuits is typically smaller (around \( 4\varepsilon_0 \)) than the silicon substrate (\( 11.8\varepsilon_0 \)) which is the material covering around the TSV in 3D circuits, therefore the TSV-induced coupling is non-negligible and needs to be fully taken into account in the early 3D designing stage.

The general structure of a TSV is a copper cylinder surrounded with a very thin insulator (\( \text{SiO}_2 \)) which is intended to prevent the DC current leakage from the TSV to the silicon substrate. The thickness of the insulator is basically less than one micrometer, and as a result, a large capacitance \( C_{ox} \) exists between the silicon substrate and the TSV. For two adjacent signal TSVs, the conventional model for coupling analysis is shown in Fig. 1. Due to the lossy silicon substrate between the two TSVs, the resistance \( R_{si} \) and capacitance \( C_{si} \) in the silicon substrate are in parallel which form the coupling channel connecting the two TSVs. Eqs. (1)–(3) to calculate these elements \( (C_{ox}, R_{si} \text{ and } C_{si}) \) have been extensively used in many previous literatures, such as in [3] and [5].

![Fig. 1. Conventional model of two adjacent TSVs for coupling analysis.](image-url)
\[ C_{ox} = \frac{2\pi \varepsilon_{0} \varepsilon_{r} l_{TSV}}{\ln\left(\frac{d_{TSV}/2 + t_{ox}}{d_{TSV}/2}\right)}, \quad (1) \]

\[ R_{si} = \left[ \frac{\pi \sigma_{si} l_{TSV}}{\cosh^{-1}(p/d_{TSV})}\right]^{-1}, \quad (2) \]

\[ C_{si} = \frac{\pi \varepsilon_{si} \varepsilon_{r} l_{TSV}}{\cosh^{-1}(p/d_{TSV})}, \quad (3) \]

where \( l_{TSV} \) and \( d_{TSV} \) are the height and diameter of the TSV, \( p \) is the pitch between two parallel conductors, \( \sigma \) and \( \varepsilon \) are the material conductivity and dielectric constant, respectively.

If one TSV is treated as an aggressor and the other the victim, the charges will flow through the coupling channel to the victim TSV and accumulate around the interface between the silicon substrate and the victim’s insulator. As the impedance of silicon substrate is finite, the charges around the victim due to the coupling will be discharged through the silicon substrate to the ground. However, many conventional models [3, 4] ignore the charge-discharging phenomenon of the victim and consider the silicon substrate to be floating, which leads to an overestimated coupling noise.

The formation of the victim’s discharging path is the \( C_{ox} \) in series with the \( RC \) parasitics as shown in Eq. (3). To distinguish the \( RC \) parasitics in the discharging path from \( R_{si} \) and \( C_{si} \) in the coupling channel, \( R_{si(GND)} \) and \( C_{si(GND)} \) are noted to represent the \( RC \) parasitics in the discharging path.

![Fig. 2. Formation of the victim’s discharging path.](image)

Due to the three elements (\( C_{ox}, R_{si(GND)} \) and \( C_{si(GND)} \)) in the discharging path, the impedance of discharging path varies in different frequency ranges. In the low frequency region, since the impedance of \( C_{si(GND)} \) is very high compared with \( R_{si(GND)} \), the charges accumulated around the victim will bypass \( C_{si(GND)} \) and flow through \( R_{si(GND)} \) to complete the discharging process. Similarly, in the high frequency region, the charges will bypass the \( R_{si(GND)} \) and flow through \( C_{si(GND)} \) to discharge itself as in this case the impedance of \( C_{si(GND)} \) becomes smaller than that of \( R_{si(GND)} \). Therefore, it is important to analyze the charge-discharging process considering frequency changes.

In order to obtain the frequency-dependent expressions of the parasitic elements in the discharging path, we transform the tapped capacitor circuit (Fig. 2) into a \( RC \) parallel circuit as shown in Fig. 3, which is based on the consideration that these two circuits have the same overall impedance. \( R_0 \) and \( C_0 \) are the equivalent parasitics.
resistance and capacitance in the discharging path, and as can be seen in Eqs. (4) and (5), both of them become the functions of frequency.

\[ C_0(\omega) = C_{ox} \left( 1 + \frac{R_{si}^2}{R_{si}^2 + C_{si}^2} C_{si} (C_{si} + C_{ox}) \right) \] (4)

\[ R_0(\omega) = \frac{1}{\frac{1}{R_{si}^2} C_{si} (C_{si} + C_{ox})} \left( \frac{C_{si}^2}{R_{si}^2} \right) \] (5)

The quasi-static EM field extractor ANSYS Q3D is employed to verify the accuracy of the equivalent capacitance and resistance in the discharging path as expressed in Eqs. (4) and (5). For the quasi-static simulation, the structure of two adjacent TSVs and their reference ground is shown in Fig. 4. Here, it is worth to mention that, with considering the impedance of silicon substrate as finite, the placement of reference ground becomes an important factor to extract \( R_0 \) and \( C_0 \) in the discharging path, as its position determines how large the value of \( R_0 \) and \( C_0 \) can be. Theoretically, the reference ground can be placed on the left side of the aggressor or on the right side of the victim, but if the pitch between the two TSVs is sufficiently large, this placement will be less realistic in terms of application. In this paper, for simplified analysis, the reference ground is placed along the central axis between the two TSVs, and its shape is cylindrical with the radius of 5 µm. The distance from the center of reference ground to the node \( m \) is defined as \( x \), and we set \( x \) as 30 µm to perform the simulation. For the analytical calculation, we use Eqs. (1)–(3) to obtain the values of \( C_{ox} \), \( R_{si} \), and \( C_{si} \) in Eqs. (4) and (5), and the design parameters used in the paper are listed in Table I. Here, it should be noted that the parameter \( p \) in Eqs. (2) and (3) should be replaced with \( p_0 \) as shown in Fig. 4(b).

### Table I. Design parameters used in this paper

| Design parameter      | Symbol | Value        |
|-----------------------|--------|--------------|
| TSV diameter          | \( d_{TSV} \) | 10 µm        |
| TSV height            | \( l_{TSV} \) | 60 µm        |
| Insulator thickness   | \( t_{ox} \) | 0.5 µm       |
| Pitch between TSVs    | \( p \) | 30 µm        |
| Dielectric constant of silicon | \( \varepsilon_{si} \) | 11.8         |
| Dielectric constant of insulator | \( \varepsilon_{ox} \) | 4            |
| Vacuum permittivity   | \( \varepsilon_0 \) | \( 8.85 \times 10^{-12} \) F/m |
The comparison results between the calculation and the simulation is shown in Fig. 5. As can be seen, the calculated values of equivalent capacitance and resistance show a good correlation with that obtained from the quasi-static simulation especially in the high frequency region. However, the discrepancy of the comparison for the capacitance in the low frequency region indicates that the analytical calculation slightly overestimates the value.

3 Evaluation of coupling with considering the impact of discharging path

As the impedance of discharging path is finite, the conventional model (shown in Fig. 1) which ignores the discharging path overestimates the coupling noise on the victim TSV. If we take the discharging path into account for coupling analysis, the charges interfered with the victim due to the coupling is divided into two branches, one flowing through the coupling channel to accumulate around the victim, the other (accumulated charges) being discharged through the silicon substrate to the ground.

From Eqs. (2) and (3), we obtain the expression for the product of RC relationship as shown in Eq. (6), which indicates that the product of RC in the
silicon substrate is only dependent to the dielectric constant and the conductivity of the silicon.

\[ R_{si}C_{si} = \frac{E_{si}d_0}{\sigma_{si}} \]  

(6)

This equation is also applied to express the product of \( RC \) in the discharging path as it is also in the silicon substrate. As can be seen in Eq. (6), if the resistance gets smaller, the capacitance will get larger correspondingly. In this case, both the resistance and capacitance impedance are decreased, which provides an easier way for the accumulated charges around the victim to be discharged. Therefore, the coupling noise on the victim can be reduced by the lowering the impedance of discharging path.

In order to verify our analysis, we change the value of silicon conductivity (\( \sigma_{si} \)) by varying the substrate doping concentration to investigate if the coupling noise can be reduced by lowering the impedance of discharging path. The p-type silicon substrate with the temperature at 300 K is used to perform the simulation. By varying the substrate doping concentration, we obtain different values of \( \sigma_{si} \). For instance, if the p-type silicon substrate with doping concentration \( (N_A) = 2 \times 10^{15} \) cm\(^{-3} \), \( \sigma_{si} \) is 14.58 S/m. By increasing \( N_A \), \( \sigma_{si} \) gets larger, and this is mainly due to the fact that the density of majority carriers increases with more highly doping. Meanwhile, we change the distance \( x \) as shown in Fig. 4(b) from 0 to 100 \( \mu \)m to investigate how the placement of reference ground affects the coupling noise. Simulations are performed to observe the changes of coupling noise on the victim caused by different values of substrate doping concentration and various placement of reference ground, and the simulation results are shown in Fig. 6. The input signal injected on the aggressor is a 1 GHz rectangular wave which changes between 0 V and 1 V with a rising/falling time of 10 ps.

![Fig. 6. Noise voltage on the victim TSV with varying the doping concentration of silicon substrate and varying the distance x as shown in Fig. 4(b).](image)

As shown in Fig. 6, the distance \( x \) between the reference ground and TSVs plays an indispensable role in affecting the coupling noise. When the reference ground is placed in node \( m \) (\( x = 0 \)) as shown in Fig. 4(b), the coupling noise is smallest, and this is due to the fact that most of E-field between the two TSVs is decoupled by the reference ground. By gradually increasing \( x \), the coupling noise is increased correspondingly as the position of reference ground becomes far away...
from the concentrated area of E-field, and thus the impact of reference ground on sharing the E-field declines. Meanwhile, the impedance of discharging path becomes higher by increasing the distance $x$, and as a result the coupling noise becomes larger as fewer charges accumulated around the victim can be discharged though the discharging path to the ground.

On the other hand, the doping concentration has an obvious impact on coupling noise. When the doping concentration is the $2 \times 10^{15}$ cm$^{-3}$, the coupling noise is larger compared to the one with doping concentration of $5 \times 10^{15}$ cm$^{-3}$. This is due to the fact that, in this case the impedance of discharging path is higher as the resistance and the capacitance in the discharging path are larger and smaller, respectively, based on the analysis above from Eq. (6). Thus, the high impedance of discharging path allows fewer charges accumulated around the victim to be discharged. By increasing the doping concentration to $5 \times 10^{15}$ cm$^{-3}$, as more charges around the victim being able to be discharged through the discharging path, the coupling noise on the victim is reduced significantly by the maximum value of 50.3% when $x = 0$. Meanwhile, we compare one condition in which the substrate resistance is close to 0 (with sufficiently high silicon conductivity $\sigma_{si}$). In this condition, the substrate can be considered to be a good conductor functioning as ground. Since most of coupling charges flowing from the aggressor to the victim will be discharged through the substrate, the coupling noise on the victim remains almost as 0. Moreover, we set silicon conductivity $\sigma_{si}$ as 0 to emulate the substrate with infinite resistance. As can be seen, the coupling noise is the largest one compared to others when the substrate is doping, and this further indicates that the impedance of discharging path determines whether it is easy or not for the accumulated charges around the victim to be discharged through the silicon substrate to the ground.

4 Conclusion

In this paper, we first analyzed the discharging path existing between the victim TSV and the silicon substrate. By transforming the tapped capacitor circuit into a RC parallel circuit for the discharging path, we obtained the analytical expressions of the parasitic elements in the discharging path, which were validated by comparing with the quasi-static simulation. Furthermore, in order to evaluate the impact of discharging path on the coupling noise, we varied distance between the reference ground and TSVs, and also varied the doping concentration of silicon substrate to adjust its impedance. Through simulations, it showed that the impedance of discharging path determines the degree of difficulty for the accumulated charges around the victim to be discharged through the silicon substrate. By lowering the impedance of discharging path, the coupling noise on the victim can be reduced significantly.

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