Modelling of Multigate MOSFET Short Channel Structure for Low Power Application

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Abstract. The paper proposes a multi-gate structure for MOSFET and focuses on studying the structure with variations in parameters such as channel length, dielectric material, source material, and gate work function. By ensuring small device dimensions, the proposed structure has been simulated using the Silvaco-TCAD tool along with analysis of short-channel effects. The proposed structure can find its usage in low power and high-frequency applications due to high switching rates. The structure also possesses high transconductance at low gate voltages, increasing intrinsic gain and proving useful in RF devices. As the device is nano-scaled, it can prove worthy for fast switching applications with low losses.

Keywords: MOSFET, multi-gate, short channel effects, Silvaco-TCAD, nano-scale devices

1. Introduction
The metal-oxide-semiconductor field-effect transistor, commonly called MOSFET, was first developed in 1959 at Bell Labs. Since then, it has evolved effectively and is now of utmost importance [12] in every electronic device. It went through several structures during its evolution, with every structure being better than the previous one. Initially, a simple bulk MOSFET structure [11], placing two pn junction diodes consecutively, which is commonly called the classical structure, was proposed. With time, the various structures such as planar double gate, tri-gate Fin FET [10], ultra-thin-body SOI, and gate all around NWFET were evolved, with each structure having its variants. In all these structures, researchers and scientists is aimed to decrease [9] the transistors’ size with high current and switching capacity alongside reducing the off the current and subthreshold slope. In this paper, we obtained a structure with minimum dimensions and lowered off the current. The subthreshold slope has also been taken care of without compromising with the current [8].
2. Literature Review
Relevant research has been made since ever the invention of MOSFET. Researchers have considered the size of the device, performance, efficiency, power output, phenomenon taking place due to variation, etc. Papers have focussed on Pi-gate MOSFET, which is defined as a triple-gate device with side walls extended into buried oxide. The structure gives the advantage of easier fabrication of pi-gate MOSFET than gates all around structure with similar characteristics as gate-all-around structure [7].

The channel's electrostatic regulation is enhanced by increasing the effective number of gates, which decreases the short-channel effects. One- and two-dimensional confinement effects have been observed due to the small dimensions of the devices, necessitating the use of advanced tools for reliable estimation of the device's electrochemical properties [6]. Quick channel and body doping results can be analysed using a compact paradigm for multi-gate MOSFETs with two separately biased gates,[5].The region over which impact ionization occurs is much larger in the junction-less devices, thereby reducing the drain voltage and obtaining a sharp subthreshold slope[4]. We also counter the increased SCEs as we reduce the size of ICs and increase the number of transistors on the chips. The study of different gate materials has been performed with efficient mathematical operations to reduce the power consumption and increase short-channel effects [3]. The variation of the threshold voltage and Drain Induction Barrier Lowering when high dielectric constant material is used as the gate oxide of the double gate MOSFET was also observed. This implies that when a gate oxide made up of high-κ material was used, the threshold voltage was considerably more, although the rate of change with respect to channel size and oxide thickness decreased [2]. Increasing the On-Off ratio of drain current considerably and improving the subthreshold slope further enhances the transconductance at the lower gate voltage, raises the output conductance and intrinsic gain making the structure suitable for RF applications [1].

3. Structure of Multi-Gate MOSFET
When gate control over the channel is affected by electric field lines from source to drain, short channel effects arise. The multi-gate MOSFET is a propitious device as it can suppress short-channel effects and reduce device variations. Under the same category is our structure, in which four equally biased gates are incorporated in MOSFET (Figure 1). Thus, this structure can achieve superior electrostatic integrity and hence scalability. For example, if we use segregated-gate devices, back-gate dynamic feedback helps resolve the leakage current issues. When it comes to nano-scale CMOS processes with large variations in threshold voltages within the circuit, our structure can be efficiently used by biasing the back-gate, reducing the subthreshold slope. In analog circuits, it can be used for low-power applications. Figure 2 represents the proposed MOSFET structure with doping concentration marked to facilitate circuit design using segregated gate FETs. It gives us an idea about doping and how carrier transportation occurs when a positive voltage equal to threshold voltage is applied to the gates and when a positive voltage is applied to the drain simultaneously.
4. Device Modelling and Simulation Methodology

The proposed structure is a four-gate structure with all gates equally biased and can be considered as a single gate segregated into four. Increasing the number of gates reduces the electric field at the drain end of the device to bring improvements in terms of drain breakdown voltage and transconductance. Moreover, to mitigate leakage currents and short channel effects, greater gate control is necessary over the channel. Hence, this technique can be identified as a critical factor, resulting in a higher ON current. We have simulated our proposed structure in Silvaco TCAD with the dimensional diagram shown in Figure 3. The models used in TCAD are CONMOB, SRH, AUGER, BGN, FLDMOB, along with the Newton Trap method. We have used high doping concentration for the source channel and drain, which reduces the leaking current and makes the subthreshold slope steeper. Hence, we get a good $I_{on}/I_{off}$ ratio.
Designing an NPN transistor using a multi-gate structure becomes easy with TCAD and can be simulated for different parameters using the same. Using the results of the simulation, graphs of the parameters were plotted and were used in data analysis. We tried to get the standard graphs from our structure which are similar to the classical MOSFET, so that the principle, which is gate-voltage controlled, is preserved along with the increased performance of the device.

The section provides detailed data on the parameters of the proposed MOSFET structure in Table 1. To obtain the best output from the structure, we have set the gate, source, drain and channel length as 20nm, work function of gate one and gate 2 = 4.3ev, the work function of gate three and gate 4 = 4.9ev, doping concentration of source, drain and channel = $10^{19} \text{cm}^{-3}$ and Newton trap method is used for simulation.

**Figure 3:** Dimensional diagram of the proposed structure

**Table 1:** Performance parameters of the MOSFET structure

| Channel Length (nm) | I\text{ON} (A/μm) | I\text{OFF} (A/μm) | $\frac{\text{I\text{ON}}}{\text{I\text{OFF}}}$ | Subthreshold slope(V/decade) |
|---------------------|-------------------|-------------------|-----------------------------|-----------------------------|
| 10                  | $4.9693\times10^{-4}$ | $10^{-13.91402}$ | $4.9693\times10^{9}$ | 0.0654745                  |
| 20                  | $4.96927\times10^{-4}$ | $10^{-12.462}$ | $4.96927\times10^{8}$ | 0.0621905                  |
| 30                  | $2.69981\times10^{-4}$ | $10^{-12.94666}$ | $2.699\times10^{8}$ | 0.0618376                  |

**5. Results and Discussions**

The analytical modeling of the proposed structure and performance are discussed in detail.

**5.1. Dielectric Material**

The need for smaller devices demands us to deal with the scaling of the thickness of the dielectric material, which is no exception. Many researchers have suggested that the gate oxide thickness should be of a minimum of 2nm to circumvent the possible short channel ill effects. A 2nm oxide thickness was...
used in the structure. To avoid leakage current in the gate, we cannot further reduce the oxide thickness. In order to increase the gate capacitance, high-k dielectric materials were exploited. These high permittivity materials succor gate to get back the lost control over the channel due to SCEs by augmenting the oxide capacitance. The graph is shown in Figure 4 using several dielectrics. This is legit since the relation between Id and capacitance can be given as:

\[ I_{d_{sat}} = \frac{w\mu C_{ox}(V_{gs} - V_{th})}{2t} \]  

Thus, \( I_d \propto C_{ox} \)

\[ \text{Figure 4: } I_{ds} \text{ vs. } V_g \text{ graph for different dielectric materials} \]

5.2. **Channel Length**

\( R_{ds(ON)} \) is a crucial current rating factor of the MOSFET. Ideally, for a lesser \( R_{ds(ON)} \), the current losses between the source and drain get reduced. The lower the ON resistance and the lesser the heat generation is in part by the current passing through it. Inherently, if the channel length is more, then \( R_d \) will be more which suppresses current drawing efficiency. Hence an appropriate channel length has to be given to the device to mitigate SCEs (short channel effects) and increase ON current. This could also help MOSFET to operate efficiently in high RF applications. Hence, different channel lengths were investigated in which it was identified that the smaller the channel length, the smaller will be the ON resistance which gives improved drive current. Moreover, the short channel MOSFETs also contribute to lesser threshold voltages, and they try to supply more charge carriers to pinch off regions

\[ \lambda = \frac{\Delta L}{V_{gL}} \]  

where \( L = \) channel length

\( \lambda = \) channel length modulation parameter.

If \( L \) decreases, then \( \lambda \) increases i.e.

\[ r_o \text{ (output resistance)} = \frac{1}{\lambda Id} + \frac{V_{ds}}{Id} \]  

decreases. Figure 5 gives the plot for gate voltage vs. drain current with varying channel length.
5.3. Source Material
The selection of source material is an important factor for deciding the leakage current and sub-threshold slope. When used at the source side, lesser band gap materials offer a smaller energy barrier for the electrons to pass through and get into the conduction band. This simple process greatly affects the ON current of the device. Figure 6 gives the graph between gate voltage and drain current for different source materials.

5.4. Work Function
The band bending is determined by the difference in the value of metal $\phi_m$ and semiconductor $\phi_s$ work functions. The work function is to be selected carefully to visualize higher $I_{ON}/I_{OFF}$ ratios. Moreover, a good selection of work function values promises efficient carrier transportation across the channel by altering barrier heights. In our structure, $\phi_{M3}$ and $\phi_{M4}$ have been given the responsibility of producing high barrier height at the channel-drain interface to keep low off the current. As $\phi_{M1}$ and $\phi_{M2}$ are responsible for polarized charge formation at the source end, identifying the appropriate value of these work functions will result in higher ON current, and it also helps in decreasing leakages and hot carrier effect by eliminating lateral electric field. Moreover, an increment in the work function difference between gate and substrate makes the threshold voltage value increase (right shifting in the graph). Figure 7 gives us the plot for different work functions.
5.5. Energy Band
The alignment of the energy band levels (both conduction band and valence band) has been shown in Figure 8. The x-axis can be taken as the cross-sectional view of the MOS device, and the y-axis represents the energy.

5.6. Acceptor and Donor Concentration
The concentration distribution depends mainly on the amount of doping we give to a particular region in the device. The below mentioned Figure 9 is displayed the plot. It depicts the acceptor and donor concentration distribution in the proposed structure. The figure shows a substantial difference between acceptor and donor concentration levels[13] by which we can curb the generation/recombination activity defects (such as ionized metallic impurities which can drift under electric field influence, altering of surface potential, threshold voltage), especially in depletion regions.
5.7. Potential and Electric Field

Potential and electric field variations depend on the concentration of donor and acceptor ions across the device's length. Figure 10 (a) gives the plot for potential variations across the length that remains constant across the device and increases and decreases at the extreme ends according to the polarity. Figure 10 (b) gives the plot of an electric field across the length of the device. The electric field decreases as we move from source to drain.

Figure 9: Acceptor and Donor Concentration

![Figure 9](image_url)

Figure 10. (a) Potential graph

![Figure 10. (a)](image_url)

Figure 10. (b) Electric field graph

![Figure 10. (b)](image_url)
5.8. Trans Conductance

Trans conductance, also called mutual conductance, sometimes gives us the relation between the current through the output of the device and the voltage applied across the device's input. It can be calculated by using the formula

\[ g_m = \frac{dI_d}{dv_g} \]  

(4)

It is regarded as a crucial factor in doing analog performance analysis of the device. Figure 11 gives the graph for Trans conductance. While going close to the drain region, the value of Trans conductance got reduced due to the quasi-saturation of electron velocity[14].

![Figure 11: Trans conductance curve](image)

5.9. Mobility

Figure 12 gives the plot for electrons, and holemobility’s inside our device. Since it is subjected to the external electric field, which pushes the carriers to attain some drift velocity, the mobility measures the charge carriers' ability to move freely in the device [15]. The magnitude of the mobility also decides the operational speed and frequency of the device. Generally, both electrons and holes possess different mobility magnitudes under the same applied electric field, as shown in the figure. The mobility inversely varies with the potential difference across the structure.

![Figure 12: Mobility Plot](image)
Figure 13: Recombination Rate Plot

Figure 13 gives the recombination rate plot along the length of the proposed structure.

6. Conclusion

The paper has a detailed analysis of our proposed structure and all the parameters plotted in the graph. It also gives us the methodology used in making the structure and the working of the same. We varied parameters to study the behavior of the structure and got satisfying results. We conclude that the structure can be effective for use in low-power applications due to its enormous properties described with the help of the graphs above. Better switching ratios for this device, as shown in Table 1, made this device suitable for high RF applications. Further studies can be done using the same structure by introducing a trench gate /U-gate/fifth gate in the center and then simulating the results and analyzing the data obtained.

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