Single Supply PWM Fully Implantable Cochlear Implant Interface Circuit With Active Charge Balancing

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Abstract

Low powered fully implantable cochlear implants (FICIs) untangle the aesthetic concerns and battery replacement problems of conventional cochlear implants. However, the reported FICIs lack proper charge balancing and require multiple external supplies to operate. In this work, a complete low power FICI interface circuit is designed that operates with a single supply and uses short-pulse-injection method for charge balancing. The system takes input from multi-channel piezoelectric transducers and stimulates the auditory neurons with pulse width modulated (PWM) output currents. By utilizing pulse width modulation technique with continuous interleaved sampling (CIS) sound processing strategy, a time gap is formed between two consecutive channels. Then, this gap is used for charge balancing operation. Overall power consumption of the low power FICI interface is decreased by clocked gated subthreshold amplifier and rectifier design. Furthermore, power efficient design of analog to digital converter (ADC) enhances the power reduction. The system is tested with an in-vitro test setup and it stimulates a single channel cochlear electrode with 50 dB input dynamic range while consuming 695 $\mu$W power from a single 1.8 V supply. The implemented FICI system can safely stimulate neurons for more than 18 days (with 16-hour daily operation) with an implantable 200 mWh battery without recharging. Furthermore, the short charge balance current pulses keep the electrode voltage difference after the stimulation within $\pm$100 mV range, which ensures the residual charge is not hazardous for the auditory neurons.

Index Terms

Charge balanced neural stimulation, fully implantable cochlear implant, low power electronics.

I. INTRODUCTION

Nearly half a billion people around the world, which is more than 5% of the world population, suffer from disabling hearing loss. Cochlear implants are one of the most successful neural prostheses and help more than 120000 deaf people in the world [1], [2]. Conventional cochlear implants consist of two parts. The outer part collects sound data via a microphone, then the data is digitalized and processed. The processed sound data and power are transmitted to the inner part with a radio frequency (RF) link. The inner part decodes the processed data for channel and amplitude information and stimulates the electrodes with the transmitted power [3]–[5]. In years, improvements are made for the speech recognition and perception of patients. These improvements are made at the sound-processing, stimulation rate, intracochlear electrode structure and channel numbers [6]–[8]. However, CIs’ main problem is the outer part because the outer part cannot be used on rainy days, in water sports and the shower. Also, they create aesthetic concerns for younger users. Besides, their battery should be replaced daily due to the high-power consumption and energy inefficiency. These problems can be

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solved with fully implantable cochlear implants (FICI) by combining internal and external parts of the CIs on a single chip [9], [10].

The main requirements of the FICI systems are an implantable sound transducer, an implantable battery, and low power interface electronics. There are studies for implantable microphones [11], [12]; however, these systems require electrical filtering as they process single microphone output, and hence the overall power consumption may increase. In a previous study in our group [13], [14], a piezoelectric sensor array is proposed as an acoustic sound transducer with 8 distinct bandpass channels. Using the proposed sensor array with an ultra-low power interface electronics, a low-power FICI system can be constructed. The previous studies in [15] and [16] are focused on the low power front-end cochlear implant interface circuits where the sound transducers of these studies are microphones and neural stimulation parts are not integrated on-chip. In [17], a single channel piezoelectric transducer takes the sound input and after amplification, the signal is digitized with state of art analog to digital converter (ADC). After filtration and compression of the digitalized signal, the electrodes are stimulated with arbitrary waveform. In [18], the sound input is taken from 8 channel input transducers [14] and clock gated logarithmic amplifiers amplify and compress it. The logarithmically compressed sound envelope is taken with a peak detector and its level determines the amplitude of the biphasic current. However, none of these systems utilize power management circuits for single battery use. Besides, they employ passive charge balance circuits. The charge balance is crucial for the functional electrical stimulation technique used by cochlear implants. The biphasic current pulse (Fig.1) is a commonly used technique for the stimulation of the neurons, and it consists of two phases: anodic and cathodic. In the cathodic phase, current flows from common electrode and current flow direction is reversed in the anodic phase with the same amplitude. However, matching of the anodic and cathodic phase currents is impossible due to the imperfections and mismatches of the integrated circuits. The mismatch between two phases results in charge accumulation which may cause tissue lesions and electrode corrosion [19]. Therefore, using a charge balance circuit is a must for long term implantable devices. The system in [17] uses blocking capacitor technique for charge balancing by adding a large capacitor on the stimulation path. Although it is a reliable method; it suffers from area limitations because of the large capacitors. The system in [18] use electrode shorting method, where a switch is presented between the electrodes and enabled after the stimulation to dissipate the accumulated charge. This technique generates an uncontrollable current at the electrode and may harm the tissue and the charge balancing currents may interfere with other channels in multichannel applications.

The aforementioned problems can be overcome by utilizing active charge balance techniques. For a multichannel FICI system most suitable charge balance technique is the pulse insertion method [19]. The generated charge balance current should not overlap with another channel’s stimulation current to prevent crosstalk between different channels. The pulse insertion method offers lower power consumption, lower area occupancy compared with other active charge balance techniques [20]. It is also suitable for multi-channel CIS strategy. In the proposed system, the single charge balance circuit can balance all channels with a smart switching.

A charge balanced FICI system requires single battery implantation due to restricted volume of the ear. To comply with high voltage compliance of neural stimulation and low voltage requirement of minimal power design more than one supply level is necessary. Due to supply limitation, an inductive or capacitive switching converter must be utilized. Monolithic integration of quality inductors is an issue and off-chip implementation results in bulky size. Designs implementing capacitor-based converters exist [21], however, the off-chip surface mounted devices (SMD) flying capacitors are still undesirable. Fully integrated examples also exist, in which various techniques are developed to construct multistage high voltage charge pumps with low voltage transistors without using level shifters [22], [23]. Similarly, in [24] an on-chip boost converter is reported, and this work utilizes a modified version of that converter according to the FICI system’s specifications to keep volume at the minimum.

II. FICI SYSTEM DESCRIPTION

The block diagram of the FICI system is given in Fig. 2. The FICI system is designed according to FLAMENCO PROJECT (https://cordis.europa.eu/project/id/682756) which includes an 8-channel piezoelectric transducer, interface circuit, cochlea electrodes and an implantable battery. The piezoelectric transducer is placed on the eardrum and converts sound vibrations into electrical signal. The electrical signals are transmitted to the interface electronics, which is placed in the middle ear. Stimulation current is generated by the interface circuit according to the input vibration. The system is powered by an implantable battery and an RF coil is placed under the skin above the ear, to be used for charging and patient fitting.

Piezoelectric sensors designed in our group [13], [14] detect input sound and generate low voltage signals due to their limited size. Therefore, the first stage of the interface circuit is transconductance amplifiers that boost up the low voltage. The amplifiers are designed to achieve low power consumption (<5 μW) with moderate gain to cover 50 dB daily speech range for adequate speech perception [25]. The amplifiers provide differential current outputs that are...
rectified with a current rectifier. The amplifiers are enabled one by one with EN_{1−8} signals for 125 µs according to the well-known CIS processing strategy, which offers the lowest power consumption. In this strategy, the rectified output current of each channel is sequentially fed to the same branch by adding operation. Since only one channel is active at a time, the other seven channel currents are zero and the total rectified current (\sum I_{REC}) is equal to the active channel output. The summed current is compressed on a diode to fit the electrical stimulation range of the cochlea which is below 15 dB [26].

The diode voltage is transferred into the digital domain with a low power 6-bit ADC. The digital output is used to determine the pulse width of the stimulation current. Digital control blocks generate the stimulator circuit inputs from ADC output and synchronize the whole system with enable and clock signals. The 8-channel single supply H-Bridge stimulator circuit is used for stimulating neurons with generated electrode currents (I_{EL}). The stimulation current amplitude is determined with a 6-bit digital to analog converter (DAC) which is controlled with patient fitting bits. Moreover, the stimulation current can be adjusted up to 2 mA. PWM technique is used instead of amplitude modulation (AM) in the generation of stimulation currents. In AM technique creating a time interval between two consecutive channels leads to a decrease in the maximum charge limit and limits the channel number in contrary the PWM technique, the required charge balance time is attained without affecting maximum charge limit and the channel number.

Unlike other FICIs, proposed system uses active charge balancing for ensuring safe stimulation. The short charge balance pulses are generated at unused time gap between two consecutive channels. By this way, crosstalk between the charge balance pulses and stimulation current of another channel is avoided. Moreover, the charge balance circuit is deactivated and does not consume any power at the stimulation time. When it is activated after the stimulation, the charge balance circuit monitors the electrode voltages, and if the electrode voltage difference is higher than a certain threshold, it generates short current pulses by using the same stimulator circuit to neutralize the unbalanced charge. The stimulator and charge balance circuits require high supply voltages due to high stimulation currents. High voltage supply is generated from 1.8 V battery voltage, and single supply...
implantation is performed by switch capacitor based on-chip DC-DC converter.

III. CIRCUIT DESIGN AND DESCRIPTION

A. INPUT TRANSCONDUCTANCE AMPLIFIERS AND CURRENT RECTIFIER

The moderate gain transconductance amplifier (Fig. 3) detects the piezoelectric transducer voltage and converts it to differential current as the output. The gain of the amplifier is set to 10 \( \mu \text{A/V} \) to cover 50 dB input dynamic range without saturation. The minimum output level of the transducers is around 150 \( \mu \text{V} \) therefore the amplifiers are designed to operate with low input noise and provide high signal to noise ratio. The low noise characteristic was met by deep n-well implementation of the input pair and proper sizing with sub-threshold operation. The integrated input referred noise from 10 Hz to 10 kHz is simulated as 13 \( \mu \text{V}_{\text{rms}} \).

To decrease power consumption of the amplifiers, all transistors are biased in sub-threshold operation and the supply voltage is set to 1.8 V. The cascoded current mirror is used for bias generation to decrease common mode gain by increasing the resistance at the source of the input pair. Fig. 4 shows the current rectifier circuit, which has a symmetrical structure and provides full wave rectification. The final rectified current is generated with subtraction operation. If the positive current (\( I_{\text{POS}} \)) is higher than the negative current (\( I_{\text{NEG}} \)), only left side of the circuit is contributed to the output current which is equal to the difference of \( I_{\text{POS}} \) and \( I_{\text{NEG}} \). If \( I_{\text{NEG}} \) is higher, only the right side of the circuit operates and constructs the rectified current at the output. Therefore, the output is full wave rectified current with the absolute value of \( I_{\text{POS}} - I_{\text{NEG}} \). The full wave rectified current is then compressed by a diode.

Fig. 5 shows the measured transient response of the amplifier and rectifier circuit. The electrical input signal with a 200 mV_{\text{PP}} and 100 Hz frequency is connected, and diode voltage is observed. The test frequency is chosen low as 100 Hz to observe the rectification and amplification operation. The front-end analog blocks which are rectifier and transconductance amplifier consume 3.6 \( \mu \text{W} \) power from 1.8 V supply. The eight front-end blocks are connected to the eight different piezoelectric transducers and enabled one by one for 125 \( \mu \text{s} \) intervals.

B. ANALOG TO DIGITAL CONVERTER

The compressed signal is digitized according to its peak value to determine the injected charge value of the stimulation. ADC works as a digital counter and the counter time determines the pulse width of the stimulation current. Fig. 6 shows the block diagram of the ADC. The amplified, rectified, and compressed input signal is used for peak detection at the sample hold circuit which can be seen from Fig. 7(a). The sample hold circuit contains three exact branches and one diode at the input. Every branch contains 3 switches and an
FIGURE 7. ADC subblock schematics: (a) sample hold circuit, (b) DAC and (c) hysteresis comparator.

on-chip capacitor. The sample hold operation is controlled by 3 control signals \( Q_{1-3} \) which are enabled sequentially for 125 \( \mu s \). Each branch has three operation phases, in the first phase the peak is determined by a diode and a capacitor. Then, the capacitor is shorted to the output and holds the peak value at the second phase. As the final phase, the capacitor is discharged to ground to keep the initial state as zero. The three identical branches of the sample and hold circuit enables to sample and hold all channels sequentially with single sample hold unit and reduces the area and power dissipation by eliminating components.

6-bit differential DAC (Fig.7(b)) is used for reference voltage generation. DAC bits are reset every 125 \( \mu s \) with \( ADC_R \) signal synchronously with \( Q_{1-3} \) signals. The current generated in the DAC is provided to the on-chip high-poly resistor to create the reference voltage for ADC. The DAC is designed with differential structure by sacrificing power consumption to eliminate charge feedthrough. The measured DAC characteristic is given in Fig. 8 and least significant bit (LSB) is calculated as 7.23 mV. The measured integral nonlinearity (INL) and differential nonlinearity (DNL) errors are smaller than 1 LSB for every bit.

The ADC comparator is a two-stage hysteresis comparator where the hysteresis value is smaller than half of LSB. The comparator output is connected to the SR-Latch in the control block to eliminate glitches. The ADC control block contains two 7-bit counters and a 7-bit digital comparator. One of the counters is operated at the charging cycle and controls the DAC current. Other counter is operated at the discharging cycle of the stimulation. After the reset signal \( ADC_R \), the discharging counter starts the counting until the comparator output changes. Then \( C/D \) signal goes to high and the charge cycle starts. The second counter starts with \( C/D \) signal and ends with the digital comparator output. After the stimulation is completed, end of conversion (EOC) signal is generated.

The ADC goes into the off state until the next reset pulse comes. The ADC is chosen as 6-bit to decrease the power consumption of the implantable device without losing the accuracy. The stimulation charge resolution is around 1 nC with 1 mA stimulation current. The ADC power is further decreased by standby operation where the analog blocks (DAC and Comparator) are turned off with the \( C/D \) signal and digital control block turned off with the \( EOC \) signal.

C. CONTROL BLOCK

The control unit generates clock signals for the synchronization of the system (Fig.9). Control block generates enable signals for the input amplifiers, reset signal for the ADC, and control signals for stimulator switches. The core of the control block is an 8-bit shift register which generates \( EN_{1-8} \) signals. The \( EN_{1-8} \) signal determines the active channel and controls
the stimulator switches with ADC outputs (EOC and C/D). The C/D signal determines the charge or discharge cycle and with EOC signal the stimulation operation is finalized and charge balancing operation is started. To control the shift register a pulse generator and start clock (CLKS), which is generated from CLKCH with a 4-bit frequency divider circuit, is utilized. The main clock of the system is CLKADC which is generated by the current starved VCO and oscillates with 1 MHz frequency. The channel control and charge balance circuit clocks are generated from CLKADC by 7-bit and 2-bit frequency dividers, respectively. The CLKCH controls the 8-bit shift register and its frequency determines the maximum stimulation time. The ADCR signal is generated from CLKCH by a 1-bit counter and pulse generator. The 1-bit counter divides the frequency by two and pulse generator generates the short pulses at every translation.

Fig. 9 (b) illustrates the operation time diagram of the control block where the pulse-width of the ADCR and CLKCB pulse widths are prolonged for simplicity. The EN1−8 signal is given in hexadecimal format. The EOC, C/D and CLKCB signal is changing with the ADC output which is not shown here. Stimulator control signals are level shifted for high voltage switching.

D. STIMULATOR CIRCUIT AND PATIENT FITTING DAC

Single supply H-bridge stimulator is used for the biphasic current output generation. Fig. 10(a) shows the schematic of the stimulator circuit and its current generator. Stimulator circuit consists of 9 branches, which are 8 electrode (EL1−8) branches and one common electrode (ELCOM) branch. Each branch is controlled by one NMOS (MN) and one PMOS (MP) switches. Fig. 10(b) illustrates the two-channel stimulation currents and common electrode switches. Cathodic pulse generation occurs when C switches are enabled and stimulation current flows from common electrode to channel electrode. Then current direction reversed by A switches and anodic pulse is generated. The supply voltage of the stimulator is VDDH which is generated by the charge pump.

Fig. 11. 6-bit patient fitting DAC characteristic.
circuit to cover high output impedance range. The switch sizes are optimized by considering the power dissipation, voltage headroom, and area.

Stimulation current peak value is determined by a programmable 6-bit DAC ($M_{0-5}$). The peak value can be changed for each channel to set stimulation current rating for maximum patient comfort. Fig. 11 shows the stimulation current with respect to digital input, where the LSB is 36 $\mu$A and maximum current rating is 2.3 mA. Even though LSB of the stimulation current is 36 $\mu$A, the LSB of the injected charge is 36 pC due to PWM control of stimulation current. The DNL and INL errors of the DAC are smaller than 1 LSB and calibration of the minimum and the maximum comfort levels of each channel can be done according to the patient. The DAC inputs are digital bits and do not require extra cascode stage unlike [18] and using single stage DAC extends the voltage headroom of the stimulator. The combined stimulator and DAC block decrease the power consumption of the system compared with the previous stimulators [17], [27] due to less current steering operation. Furthermore, the same DAC is used for determining current rating of the charge balance current for area and power efficiency. The stimulation and charge balance current ratings can be differed from each other by connecting the $EOC$ signal as a DAC bit, since $EOC$ signal is low when charge balance operation occurs.

After the implantation, maximum current ratings of each channel can be adapted according to patient comfort levels with 6-bit patient fitting control. If the tissue impedance is increased with time, voltage compliance may not be enough for proper operation. In this case, the current rating and system frequency may be decreased to reduce resistive effect at the tissue impedance.

### E. CHARGE BALANCE CIRCUIT

The pulse insertion method is used for active charge balancing due to its area and power efficiency with multichannel operation compatibility. The designed active charge balance circuit can be seen on Fig.12 (a). The charge balance circuit is enabled after the stimulation, which then monitors the electrode voltage. If the electrode voltage difference passes the predefined threshold value, a charge balance current is generated. The charge balancing operation is illustrated in...
Fig. 12(b) and performed in two cycles and these cycles are controlled with the $CLK_{CB}$ signal. After the stimulation, $CLK_{CB}$ signal is generated by the control block. The monitoring phase occurs when the clock is high where the switches are shorted to the window comparators. When $CLK_{CB}$ is low, charge balance current is generated to limit electrode voltage difference in the $\pm 80$ mV range. Sign of the charge balance current is determined according to the comparator outputs.

The window comparators are designed with differential two stage hysteresis comparator and common drain stage at the input. The hysteresis comparator topology is the same as Fig. 7(c) and it is optimized for high supply voltage. The hysteresis value is selected according to the window value of the charge balancing. Since the stimulator circuit is connected to the high voltage supply, electrode voltages can vary up to high. The common drain stage is used to generate offset for the charge balancing operation. To create the offset voltage, a mismatch is introduced in the biasing of the common drain stages. The offset value is chosen as 60 mV and the hysteresis is set to 20 mV. Overall, the charge balance circuit limits the electrode voltage difference under 80 mV which is in the safety region ($\pm 100$ mV) [28].

The charge balance circuit uses two different supplies for the low-power operation. The switch and comparators use high voltage, and the control block uses 1.8 V supply. The comparator output voltage level is decreased with the level shifters and the control block generates the stimulator switch signals according to these signals. The implanted charge balance circuit consumes 31.82 $\mu$W and occupies 200 $\mu$m$^2$.

**F. DC-DC CONVERTER**

The implemented DC-DC converter must provide the necessary high voltage for proper neural stimulation. Hence, the two-stage boost converter in [24] is optimized according to the load conditions of the FICI system. A total of 520 pF capacitance was implemented on-chip using 2 fF/$\mu$m$^2$ metal-insulator-metal (MIM) capacitors in bulk CMOS process. Two-stage boost converter is used in order to supply 5.4 V from 1.8 V supply voltage under no load condition. One stage of the converter is shown in Fig. 13(a).

The circuit uses 12 switches and 6 on chip capacitors. Two-phase non-overlapped clock signal is used for driving switches. In one of the phases, node X or Y is charged to $V_{N-1}$ (N: stage number) voltage and then boosted with the input voltage (VDD). When $\phi_1$ is high, node X is equal to $V_{N-1}$ and when $\phi_2$ is high, it is boosted with the input voltage (VDD). The same operation is valid for node Y with reverse of the clocks. The switch gates ($M_{N3-6}$ and $M_{P3-6}$) are driven by bootstrap capacitors ($C_{3-6}$). Bootstrap capacitors are used as a level shifter to supply high gate voltage for switching.

Fig 13(b) shows the DC supply voltage and stimulation currents respect to ramp input voltage. The output has no regulation or output capacitance, because of that the output voltage is decreased down to 4.65 V. The output voltage decrease does not affect the system operation however, maximum tolerable resistance is decreased. The design was optimized to operate in a load current range of 100 $\mu$A to 1 mA according to the stimulators needs. A maximum efficiency of 81.3% is achieved for a load current of 500 $\mu$A at 5 MHz switching frequency.

**IV. TEST RESULTS AND DISCUSSION**

Fig. 14 shows the micrograph of the FICI interface circuit occupying 2.44 mm$^2$ active area. The interface circuit is designed and implemented in a 180 nm High Voltage CMOS process. The 8-channel FICI system is tested with a single ramp input while 8 inputs are connected and shown in Fig. 15. At the output, a series RC circuit is connected as an artificial neural load (2.3 k$\Omega$ and 66 nF). The pulse widths of the biphasic current outputs are changing logarithmically with the input voltage. The output currents are generated based on CIS stimulation strategy and maximum duration of each channel is limited to 125 $\mu$s with 1 kHz frequency. The
The current amplitude is set to 500 µA by 6-bit patient fitting DAC and the stimulator voltage is controlled with DC-DC converter. The implemented FICI interface circuit is tested with single channel animal cochlear platinum electrode (manufactured by MED-EL) and piezoelectric transducer. In-vitro test setup can be seen from Fig. 16. The input is given from a headphone and recorded with probe-microphone to detect pressure levels. The 8-channel piezoelectric transducer array in [13] converts the sound signal into the electrical signals. Then, the electrical signals are processed with the FICI interface circuit and PWM modulated charge balanced output currents are generated. The output currents stimulate the single channel cochlear electrode and electrode voltages are observed from an oscilloscope. The circuit model of electrode impedance is verified by observing the impedance of two electrode terminals, which were placed in saline, with an Agilent E4980A LCR Meter. The LCR Meter is set to Cs-Rs configuration and impedance recorded as series 2.3 kΩ resistor and 66 nF capacitor. Acoustical characterization of the multi frequency piezoelectric transducer’s 2nd channel (mechanical characterization was presented in [13]) is shown in Fig. 17. This channel can generate 200 µV at 50 dB SPL and 50.6 mV at 100 dB SPL for a 652 Hz sound input. Fig. 18 shows the single channel electrode voltage difference where the input is 652 Hz sound signal with a changing pressure level. The system generates biphasic current pulses of 1 mA peak value. The system can operate with minimum 50 dB input SPL and generate current with 20 µs

**TABLE 1.** Power consumption of the FICI system.

| Circuit Blocks     | Current (µA) | Supply (V) | Power (µW) |
|--------------------|-------------|------------|------------|
| Front-end Blocks   | 2.0         | 1.8        | 3.60       |
| ADC                | 3.6         | 1.8        | 6.48       |
| Control Block      | 14.0        | 1.8        | 25.20      |
| Stimulator         | 98.1        | 4.8        | 471        |
| Charge Balance     | 6.1         | 5.2        | 31.72      |
| Front End          | 19.6        | 1.8        | 35.28      |
| Charge Pump (CP)   | 87.2        | 1.8        | 157        |
| Total w/o CP       | -           | -          | 538        |
| Total w/ CP        | 386.1       | 1.8        | 695        |

**FIGURE 16.** (a) The in-vitro test setup, (b) block diagram of the setup (c) the cochlea electrode connections, (d) the cochlea electrode array, (e) piezoelectric transducer holder, (f) the probe microphone and headphone, (g) 8 channels piezoelectric transducer.

**FIGURE 17.** Piezoelectric transducer output voltage respect to SPL.

**FIGURE 18.** Single channel FICI system electrode voltage difference for different input SPL.
pulse width. The maximum pulse width is 62.5 µs and it is generated when the input value is higher than 100 dB.

The circuit can compress the 50-dB input dynamic range to 10 dB electrical range for the stimulation. Fig. 19 shows the generated biphasic currents with and without charge balance circuits under the same testing conditions. The stimulation occurs with 1 kHz frequency with 1 mA generated current output. Without charge balance, the residual voltage value saturates at 400 mV after the stimulation, which implies unbalanced stimulation. The charge balance circuit controls the residual voltage at the electrode capacitance and neutralizes the unbalanced condition with short pulses and residual voltage is limited between −100 mV and +100 mV.

For power calculations, the 8 channel is connected to single sinusoidal input signal with 1 kHz frequency and 1 mV peak voltage which is equal to piezoelectric sensor output for 60 dB SPL. Fig. 20 shows the charge pump circuit output and single supply current. The DC-DC circuit generates 4.8 V when stimulation occurs and 5.2 V at the charge balancing. The average power of the system is calculated as 695 µW which is consumed from a single battery and it is low enough for a long term fully implantable operation. Table 1 shows the power consumption of the subblocks of the system. While analog blocks, ADC, control block work with 1.8 V supply, charge balance and stimulator circuits operate with DC-DC converter output which operates with 78% efficiency and calculated by considering the total power consumption.

In this work, a FICI system is presented with a novel stimulation technique which consists of the combination of multi-channel CIS sound processing technique with short pulse injection charge balance method. To combine these techniques the PWM FICI system is designed and verified with in-vitro tests. The system’s overall power consumption is decreased by clocked gated subthreshold amplifier and rectifier design, and power efficient ADC. The ADC is turned off after the first phase of the stimulation to save power and the whole system consumes a total of 695 µW from a single battery.
battery and limits the electrode voltages with charge balance currents while stimulating 8 distinct channels with 50 dB dynamical range.

The comparison with the state of the art FICI interface circuits is given in Table 2. Although there are lower power consuming FICIs in the table, none of them utilize on-chip active charge balancing. They also require additional DC-DC converters for single battery implementation. The proposed circuit has lower dynamical range and voltage compliance compared with the state of the art, however, the implemented circuit can be placed into the middle ear without using any off-chip components other than a single battery while ensuring safe electrical stimulation.

V. CONCLUSION

The implemented FICI interface circuit takes input from 8 distinct bandpass piezoelectric sensors and amplifies with transconductance amplifiers. The output currents of the clock gated 8 amplifiers are added, rectified, and compressed by a diode. The compressed diode voltage is digitalized with a 6-bit ADC. Digital output determines the pulse width of the biphasic current. After stimulation, charge balancing is achieved by monitoring the electrode voltage and generating short charge balance current pulses if the difference is higher than the threshold value. The electrodes are stimulated according to CIS strategy and the maximum pulse width is 62.5 µs. The system has a 50-dB input dynamical range and every channel stimulates with 1 kHz frequency. The system is tested with in-vitro test environment and provides 34 nC/phase for 70 dB single tone input. The implanted system consumes 695 µW power from single 1.8 V supply and operate up to 18 days (16 hours daily operation) with an implantable 200 mWh battery without recharging. The interface circuit is implantable and provides safe operation for the patients. The implemented system is the first single supply FICI with active charge balance circuit in the literature according to our knowledge.

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