Building Application-Specific Overlays on FPGAs with High-Level Customizable IPs

Hongbo Rong
Parallel Computing Lab (PCL), Intel
hongbo.rong@intel.com

Abstract
Overlays are virtual, re-configurable architectures that overlay on top of physical FPGA fabrics [8]. An overlay that is specialized for an application, or a class of applications, offers both fast reconfiguration and minimized performance penalty. Such an overlay is usually implemented by hardware designers in hardware “assembly” languages at register-transfer level (RTL).

This short article proposes an idea for a software programmer, instead of hardware designers, to quickly implement an application-specific overlay using high-level customizable IPs. These IPs are expressed succinctly by a specification language, whose abstraction level is much higher than RTL but can nonetheless express many performance-critical loop and data optimizations on FPGAs, and thus would offer competitively high performance at a much lower cost of maintenance and much easier customizations.

We propose new language features to easily put the IPs together into an overlay. A compiler automatically implements the specified optimizations to generate an efficient overlay, exposes a multi-tasking programming interface for the overlay, and inserts a runtime scheduler for scheduling tasks to run on the IPs of the overlay, respecting the dependences between the tasks. While an application written in any language can take advantage of the overlay through the programming interface, we show a particular usage scenario, where the application itself is also succinctly specified in the same language.

We describe the new language features for expressing overlays, and illustrate the features with an LU decomposer and a convolutional neural network. A system is under construction to implement the language features and workloads.

1. Introduction
An FPGA has massive amount of logical elements that are distributed, locally connected and running in parallel, interleaved with memory blocks and often with hardened DSP blocks. The logical elements, interconnects, memory and DSP blocks can be synthesized to match a dataflow compute for the best performance and power efficiency. However, the synthesis time tends to be very long: even a small design may take tens of minutes, and a larger design can easily take hours or even days.

Overlays have been proposed to cut down the synthesis time. Overlays are virtual, re-configurable architectures that overlay on top of physical FPGA fabrics [8]. An overlay usually has (much) coarser granularity, and thus (much) smaller amount, of resources that can be re-configured. Therefore, the resources of an overlay can be synthesized for a dataflow compute at a radically faster speed than the traditional hardware synthesis [8, 3, 2].

An overlay offers software programmers a software-like programming experience: An overlay is built with hardware IPs on top of an FPGA; the hardware IPs have a higher-abstraction level (e.g. matrix or vector level), and thus programmers can program the overlay at that higher abstraction level instead, reaching higher productivity at a reasonable performance cost.

However, there are remaining problems:

• An overlay itself is usually still implemented at RTL, and by hardware experts, with a high development cost.

• Overlays are often available only for hot domains or applications (e.g. deep learning these days [4, 6, 1]). Existing overlays might not necessarily well match new algorithms, applications or domains.

This short article proposes an idea to enable a software programmer, instead of hardware experts, to quickly build an application-specific overlay on an FPGA using high-level customizable IPs. These IPs are succinctly specified: the dataflow of an IP is expressed in a functional notation, followed by a description how to efficiently map the dataflow onto the spatial FPGA architecture with many loop and data optimizations, e.g. how to map the dataflow onto a systolic array that well matches the underlying FPGA architecture and thus is critical for performance.
The IPs are only specified, while the detailed implementation of the specified optimizations is left to a compiler. The specification language and compiler used is T2S (Temporal To Spatial) [7]. Our previous work on T2S has proved that a smart compiler can generate efficient IPs with a fraction of development time but with competitive performance, compared with the same IPs that are optimized in the same set of optimizations but the optimizations are implemented manually by experts in high-level synthesis (HLS) languages [9, 5].

Since the IPs are written at an abstraction level much higher than RTL, the IPs require much lower maintenance cost, are much easier to customize by software programmers, and on the hand, with the right set of optimizations, can offer competitively high performance.

The compiler will automatically expose a multi-tasking programming interface for an overlay, and insert a runtime scheduler for scheduling tasks to run on the overlay, respecting the dependences between the tasks. While an application written in any language can take advantage of the overlays through the programming interfaces, we show a particular usage scenario, where the application itself is also succinctly specified in the same language.

This approach is generally applicable to many applications that have many tasks and the tasks need share limited FPGA resources. We will illustrate the approach with a VGG convolutional neural network and a blocked LU decomposer. We will define an overlay for each of them; each overlay contains a few IPs on an FPGA. For the neural network, we map and schedule all the layers to an overlay. For the blocked LU decomposer, we dynamically generate tasks, and schedule them to the other overlay.

This article focuses on describing the idea. We are building a prototype to implement the proposed idea, leveraging our current systems [9, 5]. We will report the progress in future publications.

2. Overall Flow

Fig. 1 shows the overall flow. A programmer specifies a definition of an overlay. Directed by the specification, a compiler automatically links the overlay definition with a pre-written runtime system and synthesize them into a bitstream for an FPGA, and generates a programming interface for the overlay. The runtime system includes command queues, a task graph and a scheduler.

The overlay generated on the FPGA can be invoked to run by an application written in any language by calling the programming interface. A particular interesting scenario is that the application is also written in the same specification language. In Fig. 1, we show that a programmer specifies an application to run on the overlay. The compiler synthesizes the application with the programming interface into another bitstream.

Then the compiler offloads both the overlay and the application to an FPGA. When the programmer invokes the application to run, the application automatically generates tasks for the runtime system to schedule to run on the overlay. The example application shown in the figure is an LU decomposer, which has many tasks of 4 kinds generated during the execution, dispatched by the runtime to run on the 4 corresponding hardware IPs in the overlay. We will describe this example in more detail below.

3. Examples

In this section, we illustrate our idea with an LU decomposer and VGG convolutional neural network. Instead of using formal definitions, we will intuitively and effectively explain our language features through these examples.

3.1 Example 1: Blocked LU decomposition

For a matrix $A = \begin{pmatrix} A_{00} & A_{01} \\ A_{10} & A_{11} \end{pmatrix}$, we would like to decompose it into $A = LU = \begin{pmatrix} L_{00} & 0 \\ L_{10} & L_{11} \end{pmatrix} \begin{pmatrix} U_{00} & U_{01} \\ 0 & U_{11} \end{pmatrix}$.

Therefore, it is easy to see that

\[
A_{00} = L_{00}U_{00} \quad (1)
\]
\[
A_{01} = L_{00}U_{01} \quad (2)
\]
\[
A_{10} = L_{10}U_{00} \quad (3)
\]
\[
A_{11} = L_{10}U_{01} + L_{11}U_{11} \quad (4)
\]

Therefore,

\[
A_{00} = L_{00}U_{00} \quad (5)
\]
\[
U_{01} = L_{00}^{-1}A_{01} \quad (6)
\]
\[
L_{10} = A_{10}U_{00}^{-1} \quad (7)
\]
\[
L_{11}U_{11} = A_{11} - L_{10}U_{01} \quad (8)
\]

We can generalize this example. Suppose the original square matrix $A$ is divided into $m \times m$ square blocks, each block having $m \times m$ elements. The algorithm of blocked LU is shown in Algorithm 1.

We vision that a T2S specification can be written as shown in Fig. 1. There are 4 hardware IPs:
**Algorithm 1**: The blocked LU decomposition algorithm.

1. for \(i = 0; i < n; i++\)
2. Task 0: decompose \(A_{ii} = L_{ii}U_{ii}\)
3. Task 1: calculate \(U_{i,(i+1):n} = L_{i,(i+1):n}^{-1}A_{i,(i+1):n}\)
4. Task 2: calculate \(L_{(i+1):n, i} = A_{(i+1):n, i}^{-1}U_{i,(i+1):n}\)
5. Task 3: calculate \(A_{(i+1):n, (i+1):n} = \cdots\)

- **LU**, which accepts a square block \(A\) with the size of \(m \times m\), and decomposes it into matrix \(L\) and \(U\), and store them at the same space of \(A\). Note the diagonal of \(L\) contains only 1’s, and thus not stored.
- **TransformRowPanel**, which accepts a row panel with a number of blocks, each block with the size of \(m \times m\), and uses the first block (corresponding to \(L_{ii}\)) to transform the other blocks, i.e. \(L_{ii}^{-1}A_{i,(i+1):n}\).
- **TransformColumnPanel**, which accepts a column panel with a number of blocks, each block with the size of \(m \times m\), and uses the first block (corresponding to \(U_{ii}\)) to transform the other blocks, i.e. \(A_{(i+1):n, i}U_{i,(i+1):n}^{-1}\).
• **GEMM**, which accepts a matrix \(C, A, B\) and co-efficient \(\alpha, \beta, \gamma\), and computes \(C = \alpha C + \beta A \ast \gamma B\).

All the 4 IPs do in-place update: they write their outputs into the same space of their inputs.

In Fig. 1, the specifications use several features new to the T2S language:

- **The Overlay** type is a container for the IPs and runtime system.
- **F.command(queueNo, parameters)** specifies a programming interface for Func \(F\): the command queue and the parameters.
- **O.enqueue(queueNo, parameters)** is to enqueue a command to the given command queue of the overlay \(O\) with the given parameters.
- **T1.depend(T2, d, [condition])** says that under an optional condition, task \(T1\) in the current iteration depends on task \(T2\) in \(d\) iterations before.
- **A.BCropped(m, startRow, endRow, startCol, endCol)** means to crop, in blocks of \(m \ast m\), from a buffer \(A\), from the given start to end row (included), and from the given start to end column (included). The cropping is in-place, and thus the cropped buffer shares the space with the original buffer.

We can explain Fig. 1 in more detail. A software programmer writes two specifications, one for the overlay, and the other for the application (i.e. LU decomposer).

In the specification of the overlay, Line 1-3 declare the 4 IPs on an (FPGA) device. Line 4-7 declare the inputs of the IPs. Line 8 defines the IPs. We assume that the IPs have already been specified with necessary optimizations in the T2S language by experts, and are provided to the programmer as a library of building blocks. Therefore, we skip the details of the definitions of the IPs here. Line 9-12 define a programming interface for each IP. Each is driven by a command queue, which is automatically provided by a runtime system. Finally, Line 13-14 put the IPs into an overlay, and compile the overlay to a named bitstream.

In the specification of the application, Line 1-2 declare the matrix to be decomposed, and 4 kinds of tasks corresponding to the 4 IPs. Line 3-9 defines some macros that are only for the convenience of usage next. Line 10 offloads the overlay’s bitstream to an FPGA, if not yet, and returns a handle. Line 11-14 generate 4 tasks and enqueue them into the command queues of the corresponding IPs. Note that there is an implicit loop 1 around the tasks. In this way, Algorithm 1 is expressed. Line 15-18 specify the dependences between the tasks. Line 19-22 set up the input matrix, compile the application into a bitstream, and run it on the FPGA.

The two specifications are compiled to run on the same FPGA. The compiler will automatically generate a programming interface, which is used for compiling the application specification.

A runtime system is automatically linked to the overlay by the compiler. The runtime system is composed of command queues and a task graph and scheduler. Each IP has a command queue containing tasks to be executed. The dependences between any two tasks are represented by a task graph and managed by a scheduler dynamically. How to write such a runtime system is a known technique.

### 3.2 Example 2: VGG convolutional neural network

A design for VGG is shown in Fig 2. There is an overlay and an application on an FPGA. The overlay has 2 hardware IPs: Convolution and Maxpool. All convolution layers (with and without ReLU) and fully-connected (FC) layers can be computed by the Convolution IP, and all the max pooling layers can be computed by the Maxpool IP. The feature map between two layers can be communicated by external DDR, or by an on-chip feature buffer. Inside a layer, the Convolution IP has a weight buffer.

Algorithm 2 shows for VGG two specifications, following the same principle for the previous LU example. We leave a detailed explanation to the comments there.

### 4. Conclusion and Future Work

We have proposed an idea for a software programmer to quickly build an application-specific overlay on an FPGA, using high-level customizable IPs. We have illustrated the idea with LU decomposition and VGG convolutional neural network. We are building a system to implement the proposed idea, leveraging our previous work on T2S. We will report the progress in future publications.
Algorithm 2: Example specifications for VGG.

1 /* Specification 1: Define an overlay */
2 Func Convolution(Place::Device), Maxpool(Place::Device); // Two HW IPs on the device (FPGA)
3 ImageParam X(Float(32), 3), Y(Float(32), 3); // Input and output feature map
4 ImageParam W(Float(32), 4); // Weights
5 Expr read_input_from_buffer, store_output_to_buffer, // Control signals to reconfigure
6 with_ReLU, is_FC_layer; // the overlay.
7
8 Functional notations and spatial mapping for the Funcs // Expressible in known state-of-
9 // art [9, 5]. Details skipped.
10
11 // Define a programming interface for each HW IP. Each IP is driven by a command queue.
12 // The command queues are automatically provided by the runtime.
13 Convolution.command(0, X, Y, W, read_input_from_buffer, store_output_to_buffer, with_ReLU,
14 is_FC_layer);
15 Maxpool.command(1, Y, store_output_to_buffer)
16
17 // Put the IPs into an overlay, and compile to a named bitstream.
18 Overlay(Convolution, Maxpool).compile("overlay.aocx");

1 /* Specification 2: Define an application on the overlay */
2 ImageParam X(Float(32), 4), // Input feature map
3 Y(Float(32), 4), // Output feature map after the last FC layer.
4 W01(Float(32), 5), W23(Float(32), 5), // Weights for convolution layer 0-1, 2-3
5 W46(Float(32), 5), W79(Float(32), 5), // Weights for convolution layer 4-6, 7-9
6 W1012(Float(32), 5), // Weights for convolution layer 10-12
7 WFO0(Float(32), 2), WFC1(Float(32), 2), // Weights for FC layer 0 and 1
8 WFO2(Float(32), 2); // Weights for FC layer 2
9 Func ConvLayers[13](Place::Device), // 13 convolution layers
10 FCLayers[3](Place::Device), // 3 fully connected layers
11 MaxpoolLayers[5](Place::Device); // 5 max pooling layers
12
13 Overlay overlay = load_overlay("overlay.aocx"); // Offload the overlay bitstream to FPGA, if
14 // not yet, and return a handle
15
16 #define INPUT(f, i) f.cropped(3, i, 1)//Reference to i'th channel of the input feature map f
17 #define WEIGHT(w, i) w.cropped(4, i, 1)//Reference to the i'th set of weights
18 #define DUMMY_I X //Arbitrary input. Not to be used anyway.
19 #define DUMMY_O Y //Arbitrary output. Not to be used anyway.
20 #define YES true
21 #define NO false
22
23 // Push to queue 0 a convolution task that reads input from DDR, stores output to the feature
24 // buffer, with ReLU, and not a FC layer.
25 ConvLayers[0](i)=overlay.enqueue(0, INPUT(X, i), DUMMY_O, WEIGHT(W01, 0), NO, YES, YES, NO);
26
27 // Next layer. Similar to the first layer, but reads from the feature buffer
28 ConvLayers[1](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W01, 1), YES, YES, YES, NO);
29
30 // Push to queue 1 a Maxpool task. A Maxpool task always reads input from the feature buffer.
31 // Here the task stores output to the feature buffer as well.
32 MaxpoolLayer[0](i)=overlay.enqueue(1, DUMMY_O, YES);
33
34 ConvLayers[2](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W23, 0), YES, YES, YES, NO);
35 ConvLayers[3](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W23, 1), YES, YES, YES, NO);
36 MaxpoolLayer[1](i)=overlay.enqueue(1, DUMMY_O, YES);
37 ConvLayers[4](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W46, 0), YES, YES, YES, NO);
38 ConvLayers[5](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W46, 1), YES, YES, YES, NO);
39 ConvLayers[6](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W46, 2), YES, YES, YES, NO);
40 MaxpoolLayer[2](i)=overlay.enqueue(1, DUMMY_O, YES);
ConvLayers[7](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W79, 0), YES, YES, YES, NO);
ConvLayers[8](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W79, 1), YES, YES, YES, NO);
ConvLayers[9](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W79, 2), YES, YES, YES, NO);
MaxpoolLayer[3](i)=overlay.enqueue(1, DUMMY_O, YES);
ConvLayers[10](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W1012, 0), YES, YES, YES, NO);
ConvLayers[11](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W1012, 1), YES, YES, YES, NO);
ConvLayers[12](i)=overlay.enqueue(0, DUMMY_I, DUMMY_O, WEIGHT(W1012, 2), YES, YES, YES, NO);
MaxpoolLayer[4](i)=overlay.enqueue(1, Y, NO);//The last MaxPool layer store results to DDR

// An FC layer always reads input from DDR, and stores output to DDR.
FCLayers[0](i)=overlay.enqueue(0, Y, Y, WFC0, NO, NO, YES, YES);
FCLayers[1](i)=overlay.enqueue(0, Y, Y, WFC1, NO, NO, YES, YES);
FCLayers[2](i)=overlay.enqueue(0, Y, Y, WFC2, NO, NO, YES, YES);

// Specify dependences between tasks in different command queues.
// Tasks in the same queue are executed in order.
MaxpoolLayer[0].depend(ConvLayers[1], 0);//Maxpool layer 0 depends on convolution layer 1
    //with distance=0(i.e. in the same loop iteration).
MaxpoolLayer[1].depend(MaxpoolLayer[0], 0);
MaxpoolLayer[2].depend(MaxpoolLayer[1], 0);
MaxpoolLayer[3].depend(MaxpoolLayer[2], 0);
MaxpoolLayer[4].depend(MaxpoolLayer[3], 0);
MaxpoolLayer[5].depend(MaxpoolLayer[4], 0);
MaxpoolLayer[6].depend(MaxpoolLayer[5], 0);
MaxpoolLayer[7].depend(MaxpoolLayer[6], 0);
MaxpoolLayer[8].depend(MaxpoolLayer[7], 0);
MaxpoolLayer[9].depend(MaxpoolLayer[8], 0);
MaxpoolLayer[10].depend(MaxpoolLayer[9], 0);
MaxpoolLayer[11].depend(MaxpoolLayer[10], 0);
MaxpoolLayer[12].depend(MaxpoolLayer[11], 0);
FCLayers[0].depend(MaxpoolLayer[4], 0);

// Set input, compile and run
set X, W*, and WFC* with real data, and allocate Y a space.
Target target = get_host_target(); // Get the CPU
target.set_feature(Target::IntelFPGA); // The CPU has a FPGA device
FCLayers[2].realize(n, target); // Compile all the Funcs into a bitstream, offload
// and run on the FPGA. Here n is #input feature maps
Y contains the results of the final FC layer. The results can be post-processed on the
// host side for softmax.
References

[1] U. Aydonat, S. O’Connell, D. Capalija, A. C. Ling, and G. R. Chiu. An openc1 deep learning accelerator on arria 10. In Proceedings of the 2017 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA ’17, page 55-64, New York, NY, USA, 2017. Association for Computing Machinery.

[2] D. Capalija and T. S. Abdelrahman. Towards synthesis-free jit compilation to commodity fpgas. In 2011 IEEE 19th Annual International Symposium on Field-Programmable Custom Computing Machines, pages 202–205, 2011.

[3] J. Coole and G. Stitt. Fast, flexible high-level synthesis from openc1 using reconfiguration contexts. IEEE Micro, 34(1):42–53, 2014.

[4] J. Fowers, K. Ovtcharov, M. Papamichael, T. Massengill, M. Liu, D. Lo, S. Alkalay, M. Haselman, L. Adams, M. Ghandi, S. Heil, P. Patel, A. Sapek, G. Weisz, L. Woods, S. Lanka, S. K. Reinhardt, A. M. Caulfield, E. S. Chung, and D. Burger. A configurable cloud-scale dnn processor for real-time ai. In 2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA), pages 1–14, 2018.

[5] Y.-H. Lai, H. Rong, S. Zheng, W. Zhang, X. Cui, Y. Jia, J. Wang, B. Sullivan, Z. Zhang, Y. Liang, Y. Zhang, J. Cong, N. George, J. Alvarez, C. Hughes, and P. Dubey. Susy: A programming model for productive construction of high-performance systolic arrays on fpgas, 2020. To appear at ICCAD 2020.

[6] T. Moreau, T. Chen, L. Vega, J. Roesch, E. Yan, L. Zheng, J. Fromm, Z. Jiang, L. Ceze, C. Guestrin, and A. Krishnamurthy. A hardware-software blueprint for flexible deep learning specialization. IEEE Micro, 39(5):8–16, 2019.

[7] H. Rong. Programmatic control of a compiler for generating high-performance spatial hardware. CoRR, abs/1711.07606, 2017.

[8] H. K.-H. So and C. Liu. Fpga overlays. In FPGAs for Software Programmers, chapter 16, pages 285–305. Springer, Cham, 2016. Available: https://doi.org/10.1007/978-3-319-26408-0_16.

[9] N. Srivastava, H. Rong, P. Barua, G. Feng, H. Cao, Z. Zhang, D. Albonesi, V. Sarkar, W. Chen, P. Petersen, G. Lowney, A. Herr, C. Hughes, T. Mattson, and P. Dubey. "t2s-tensor : Productively generating high-performance spatial hardware for dense tensor computation". In Proceedings of the International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2019.