An Almost Tight RMR Lower Bound for Abortable Test-And-Set

Aryaz Eghbali
Department of Computer Science, University of Calgary, Canada
aryaz.eghbali@ucalgary.ca

Philipp Woelfel
Department of Computer Science, University of Calgary, Canada
woelfel@ucalgary.ca

Abstract
We prove a lower bound of $\Omega(\log n / \log \log n)$ for the remote memory reference (RMR) complexity of abortable test-and-set (leader election) in the cache-coherent (CC) and the distributed shared memory (DSM) model. This separates the complexities of abortable and non-abortable test-and-set, as the latter has constant RMR complexity [25].

Golab, Hendler, Hadzilacos and Woelfel [27] showed that compare-and-swap can be implemented from registers and TAS objects with constant RMR complexity. We observe that a small modification to that implementation is abortable, provided that the used TAS objects are abortable.

2012 ACM Subject Classification Theory of computation → Shared memory algorithms

Keywords and phrases Abortability, Test-And-Set, Leader Election, Compare-and-Swap, RMR Complexity, Lower Bound

Funding This research was undertaken, in part, thanks to funding from the Canada Research Chairs program and from the Discovery Grants program of the Natural Sciences and Engineering Research Council of Canada (NSERC).

1 Introduction

In this paper, we study the remote memory references (RMR) complexity of abortable test-and-set. Test-and-set (TAS) is a fundamental shared memory primitive that has been widely used as a building block for classical problems such as mutual exclusion and renaming, and for the construction of stronger synchronization primitives [35, 39, 19, 18, 7, 6, 27].

We consider a standard asynchronous shared memory system in which $n$ processes with unique IDs communicate by reading and writing shared registers. A TAS object stores a bit that is initially 0, and provides two methods, $\text{TAS}()$, which sets the bit and returns its previous value, and $\text{read}()$, which returns the current value of the bit. TAS is closely related to mutual exclusion [17]: a TAS object can be viewed as a one-time mutual exclusion algorithm, where only one process (the one whose $\text{TAS}()$ returned 0) can enter the critical section [18].

TAS objects have consensus-number two, and therefore they have no wait-free implementations. In particular, in deterministic TAS implementations, processes may have to wait indefinitely, by spinning (repeatedly reading) variables. It is common to predict the performance of such blocking algorithms by bounding remote memory references (RMRs). These are memory accesses that traverse the processor-to-memory interconnect. Local-spin algorithms achieve low RMR complexity by spinning on locally accessible variables. Two models are common: In distributed shared memory (DSM) systems, each shared variable
is permanently locally accessible to a single processor and remote to all other processors. In cache-coherent (CC) systems, each processor keeps local copies of shared variables in its cache; the consistency of copies in different caches is maintained by a coherence protocol. Memory accesses that cannot be resolved locally and have to traverse the processor-to-memory interconnect are called remote memory references (RMRs).

Golab, Hendler, and Woelfel [25] devised deadlock-free TAS algorithms with \(O(1)\) RMR complexity for the DSM and the CC model, which in turn have been used to construct equally efficient comparison-primitives, such as compare-and-swap (CAS) objects [27]. These constructions are particularly useful in the study of the complexity of the mutual exclusion problem, for which the RMR complexity is the standard performance metric [10, 9, 34, 12, 13, 31, 32, 33, 15, 29, 30, 40, 22, 11, 36, 16, 37, 23].

In the context of mutual exclusion, it has been observed that systems often require locks to support a “timeout” capability that allows a process waiting too long for the lock, to abort its attempt [41]. In database systems, such as Oracle’s Parallel Server and IBM’s DB2, the ability of a thread to abort lock attempts serves the dual purpose of recovering from a transaction deadlock and tolerating preemption of the thread that holds the lock [41]. In real time systems, the abort capability can be used to avoid overshooting a deadline. Solutions to this problem have been proposed in the form of abortable mutual exclusion algorithms [41, 31, 40, 37, 16, 24]. In such an algorithm, at any point a process may receive an abort signal upon which, within a finite number of its own steps, it must either enter the critical section or abort its current attempt to do so, by returning to the remainder section.

The complexity of the mutual exclusion problem is not affected by abortability: The abortable algorithm by Danek and Lee [16, 38] achieves \(O(\log n)\) RMR complexity, which asymptotically matches the known lower bound for non-abortable mutual exclusion [22]. But abortable mutual exclusion algorithms seem to be much more difficult to obtain than non-abortable ones, and it is not surprising that all such algorithms preceding [16, 38] used stronger synchronization primitives (e.g., LL/SC objects in [31]). Moreover, no RMR efficient randomized abortable mutual exclusion algorithms are known, unless stronger primitives are used [40, 24]; on the other hand, several non-abortable randomized implementations use only registers [25, 29, 23, 13].

As mentioned earlier, CAS objects with \(O(1)\) RMR complexity can be obtained from registers [27], but they cannot be used in an abortable mutual exclusion algorithm without sacrificing its abortability: if a process receives the abort signal while being blocked in an operation on a CAS object, it has no option to finish that operation in a wait-free manner, and thus can also not abort its attempt to enter the critical section. In general, implemented blocking strong objects, cannot be used to obtain abortable mutual exclusion objects.

One way of dealing with this impasse can be to make implementations of strong primitives also abortable, and to devise mutual exclusion algorithms in such a way that they accommodate operation aborts. Similarly, other algorithms and data structures that may require timeout capabilities, can potentially be implemented from abortable objects, but not from non-abortable ones.

We define abortability in the following, natural way: In a concurrent execution, a process executing an operation on the object may receive an abort signal at any point in time. When that happens, it must finish its method call within a finite number of its own steps (wait-free), and as a result the method call may fail to take effect, or it may succeed. The resulting execution must satisfy the safety conditions of the object (e.g., linearizability), if all failed operations are removed. Moreover, a process must be able to find out, by looking at the return value, whether its aborted operation succeeded, and if it did, then the return value
must be consistent with a successful operation.

It may be tempting to define a weaker forms of abortability, e.g., where a return value of an aborted operation does not indicate whether the operation succeeded or not. But the usefulness of such a weaker notions is not clear. For example, abortable TAS objects (according to our definition) can easily be used to implement an abortable mutual exclusion algorithm (TAS-lock): One can store a pointer to a “current” TAS object in a single register \( R \). To get the lock, a process calls \( \text{TAS}() \) on the TAS object that \( R \) points to, and if the return value is 0, then the process has the lock, and otherwise it keeps reading \( R \) until its value changes. To release the lock, the process simply swings the pointer \( R \) so that it points to a new, fresh TAS object (this technique was proposed in \([5]\), and \([1, 2]\) showed how to bound the number of involved TAS objects). This also works in the case of aborts, because a process knows whether its operation took effect, and thus whether it is allowed to swing the pointer (and in fact must, to avoid dead-locks).

For the weaker definition of abortability mentioned above, a process whose \( \text{TAS}() \) aborted may not be able to find out whether it has the lock or not, and then it can also not swing the pointer to a new TAS object, even though its \( \text{TAS}() \) may have set the bit from 0 to 1. In fact, suppose that two processes call \( \text{TAS}() \), and both \( \text{TAS}() \) calls abort without receiving the information whether the aborted operation took effect. Then the TAS bit may be set, but none of the processes has received any information regarding who was successful, and reading the TAS object also provides no information.

Even though our notion of abortability may seem strong, any abortable mutual exclusion algorithm can be used to obtain any abortable object from its corresponding sequential implementation, by simply protecting the sequential code in the critical section. An interesting question is therefore, whether abortable objects can be obtained at a lower RMR cost than mutual exclusion.

We observe that this is true for implementations of abortable CAS objects from abortable TAS objects on the CC model: a straight-forward modification of the constant RMR implementation of non-abortable CAS from TAS objects and registers \([27]\), immediately yields an abortable CAS object, provided that the used TAS objects are atomic or also abortable.

\[ \text{Theorem 1.} \] There is a deadlock-free implementation of abortable CAS from atomic registers and deadlock-free abortable TAS objects, which has \( O(1) \) RMR complexity on the CC model.

Note that there are efficient randomized implementations of TAS from registers, where the maximum number of steps any process takes in a \( \text{TAS}() \) operation is \( O(\log^* n) \) against an oblivious adversary \([21]\). In the construction of CAS above, we can use such a randomized TAS implementation in place of abortable TAS.

\[ \text{Corollary 2.} \] There is a deadlock-free randomized implementation of abortable CAS from atomic registers, such that on the CC model against an oblivious adversary each abort is randomized wait-free, and each operation on the object incurs at most \( O(\log^* n) \) RMRs.

Recall that there is also a deterministic constant RMR implementation of TAS from registers \([25]\), and thus making this implementation abortable, would, together with the result mentioned above, immediately yield deterministic constant RMR abortable implementations of CAS from registers. Unfortunately, it turns out that a deterministic constant RMR implementation of abortable TAS from registers cannot exist. In particular, we define the abortable leader election (LE) problem, which is not harder and possibly easier than abortable TAS (with respect to RMR complexity). Our main technical result is an RMR lower bound of \( \Omega(\log n / \log \log n) \) for that object.
In a (non-abortable) LE protocol, every process decides for itself whether it becomes the leader (it returns \textit{win}) or whether it loses (it returns \textit{lose}). At most one process can become the leader, and not all participating processes can lose. I.e., if all participating processes finish the protocol, then exactly one of them returns \textit{win} and all others return \textit{lose}. Note that then in an abortable LE protocol all participating processes allowed to return \textit{lose}, provided that all of them received the abort signal.

An abortable TAS object immediately yields an abortable LE protocol: Each process executes a single \textsc{TAS()} operation and returns \textit{win} if the \textsc{TAS()} call returns 0, and otherwise \textit{lose} (i.e., it returns \textit{lose} also when the \textsc{TAS()} return value indicates a failed abort).

Our main result is the following:

\begin{quote}
\textbf{Theorem 3.} For both, the DSM and the CC model, any deadlock-free abortable leader election algorithm has an execution in which at least one process incurs $\Omega(\log n/\log\log n)$ RMRs.
\end{quote}

Leader election is one of the seemingly simplest synchronization primitives that have no wait-free implementation. In particular, as argued above, the lower bound in Theorem 3 immediately also applies to abortable TAS. This is in stark contrast to the $O(1)$ RMRs upper bound for non-abortable TAS and even CAS implementations \cite{25, 27}. It shows that adding abortability to synchronization primitives is almost as difficult as solving abortable mutual exclusion, which has an RMR complexity of $\Theta(\log n)$ \cite{16, 38}.

In our lower bound proof we identify the crucial reason for why abortable LE is harder than its non-abortable variant: According to standard bi-valency arguments, for any deadlock-free LE algorithm, there is an execution in which some process takes an infinite number of steps. But it is not hard to see that one can design an (asymmetric) 2-process LE protocol in which one fixed process is wait-free, because the other one waits for the first one to make a decision if it detects contention. It turns out that this is not the case for abortable LE: Here, for any process, there is an execution in which that process takes an infinite number of steps.

\section*{Other Related Work.}

Aguilera, Frølund, Hadzilacos, Horn, and Toueg \cite{4} define a different notion of abortable object, where no abort signals are sent by the system, but a process may decide for itself to abort an ongoing operation, e.g., when it detects contention. According to their definition, the caller of an aborted operation may not find out whether its operation took effect or not. Since this uncertainty may not be acceptable, they also introduce query-abortable objects, where a query operation allows a process to determine additional information about its last non-query operation.

Note that their notion of abortability is quite different from the one used commonly for mutual exclusion and adopted by us, where the system, and not the implementation, dictates when a process needs to abort.

\section{Abortable Compare-And-Swap in the CC Model}

In this section we consider the cache-coherent (CC) model. Each process obtains a cache-copy with each read of a register, and the cache-copy gets only invalidated if some process later writes to the same register. Writes as well as reads of non-cached registers incur RMRs, while reads of cached registers do not.
A CAS object provides two operations, \( \text{CAS}(\text{cmp}, \text{new}) \), and \( \text{read()} \). Operation \( \text{read()} \) returns the current value of the object. Operation \( \text{CAS}(\text{cmp}, \text{new}) \) writes \( \text{new} \) to the object, if the current value is \( \text{cmp} \), and otherwise does not change the value of the object. In either case it returns the old value of the object.

Golab et al. \[26\] gave an implementation of CAS from TAS and registers, which has constant RMR complexity in the CC model, i.e., each \( \text{CAS()} \) and \( \text{read()} \) operation incurs only \( O(1) \) RMRs. In this section we show how to make that implementation abortable, provided that we have access to abortable TAS objects. The pseudocode is in Figure 1. The original (non-abortable) version of the code is shown in black and our additional code to make it abortable in red (lines 6 and 20).

2.1 From TAS to Name Consensus

The implementation in \[26\] first constructs a name consensus object from a single TAS object \( T \). This implementation provides a method \( \text{NameDecide()} \), which each process is allowed to call at most once. All \( \text{NameDecide()} \) calls return the same value (agreement), which is the ID of a process calling \( \text{NameDecide()} \) (validity).

The non-abortable implementation in \[26\] uses a TAS object \( T \) and a register \( \text{leader} \) that is initially \( \bot \). In a \( \text{NameDecide()} \) call, a process \( p \) first calls \( T.\text{TAS()} \). If the \( \text{TAS()} \) returns 0, then \( p \) wins, and writes \( p \) to \( \text{leader} \). Otherwise, \( p \) loses, and so it repeatedly reads \( \text{leader} \), until \( \text{leader} \neq \bot \), upon which \( p \) can return the value of \( \text{leader} \). It is easy to see (and was formally proved in \[26\]) that this is a correct name consensus algorithm.

We now show how this implementation can be made abortable, assuming the TAS object \( T \) is abortable. We assume that when a process receives the abort signal, a static process-local variable \( \text{abort} \), which is initially false, changes to \( \text{True} \).

Recall that abortability requires that the return value of a TAS() operation indicates whether it failed or succeeded. We assume a failed \( \text{TAS()} \) simply returns \( \bot \). In \( \text{NameDecide()} \), processes are only waiting until \( \text{leader} \) changes. If a process is receiving the abort signal while waiting for \( \text{leader} \) to change, then it can also simply return \( \bot \). The rest of the algorithm is the same as the original name consensus algorithm.
Clearly, the new code (line 6) does not affect RMR complexity, and following an abort the code is wait-free. Moreover, correctness (validity and agreement) in case of no failed NameDecide() operations follow immediately from correctness of the original algorithm. If a NameDecide() operation fails (i.e., returns ⊥), then it did not change any shared memory object (its TAS() must have either failed, or returned 1). Hence, removing an aborted and failed NameDecide() operation from the execution does not affect any other processes, and therefore the resulting execution must be correct.

2.2 From Name Consensus to Compare-And-Swap

We now show how the abortable name consensus algorithm can be used to obtain abortable CAS. Consider the implementation of CAS(cmp, new) on the right hand side in Figure 1. The black code is logically identical to the one in [26]. It uses a register $D$ that points to a page, which stores two registers, value and flag, as well as a name consensus object $N$. Register value at the page pointed to by $D$ stores the current value of the object. (Thus, a read() operation, for which we omit the pseudo code, simply returns $D \rightarrow value$.) The CAS() operation assumes a wait-free method getNewPage(), which returns an unused page from a pool of pages (for simplicity assume this pool has infinitely many pages, but there are methods for wait-free memory management that allow using a bounded pool [27, 3]).

For a description of how the algorithm CAS(cmp, new) works, we refer to [26]. We can prove that the abortable version presented here is correct, provided that the non-abortable version (with line 20 removed) is: First of all, obviously line 20 does not change the RMR complexity. Moreover, if a process receives the abort-signal, then its abortable NameDecide() call terminates within a finite number of steps, and the process also does not wait in the while-loop, so its CAS() call completes within a finite number of its steps. Finally, notice that a CAS() call returns ⊥ only if an abort signal was received, and in that case no shared memory objects are affected (the process cannot have won the NameDecide() call). Hence, all aborted and failed operations can be removed from the execution without changing anything for the remaining operations. As a result we obtain Theorem 1.

3 RMR Lower Bound for Abortable Leader Election

In this section, we give an overview of the RMR lower bound proof for abortable leader election (and thus TAS) as stated in Theorem 3. First, we define some notation, the system model, RMR complexity, and the abortable leader election problem.

3.1 Lower Bound Preliminaries

System Model and Notation. For a set $Q$, set $Q^k$, for some non-negative integer $k$, denotes the set of all sequences of length $k$ that contain only the elements in $Q$. Furthermore, $Q^*$ denotes the sets of all sequences that contain only elements of set $Q$.

For the lower bound we assume a set $P$ of $n$ processes, and an arbitrary large but finite set $R$ of shared registers. Processes are infinite state machines. In each shared memory step (corresponding to a state transition), a process either reads or writes a register in $R$. At an arbitrary point, a process may also receive an abort signal which does not result in a shared memory access, but in a state change of that process, provided the process has not earlier received the abort signal. Once a process has reached a halting state, it will remain in that state forever, and does not execute any further shared memory steps.
For each process \( p \in \mathcal{P} \), we define a special abort symbol \( p^\top \). For a set \( P \subseteq \mathcal{P} \) let \( P^\top = \{p^\top | p \in P\} \), and \( P^\Delta = P \cup P^\top \). A configuration is a sequence that describes the state of each process in \( \mathcal{P} \) and each register in \( \mathcal{R} \). A schedule is a sequence \( \sigma \) over \( P^\Delta \). Thus, any schedule \( \sigma \) is in \( (P^\Delta)^* \). The length of an schedule \( \sigma \) is denoted by \( |\sigma| \). Let \( \sigma_1 \) and \( \sigma_2 \) be two schedules. Then \( \sigma_1 \circ \sigma_2 \) is the schedule obtained by concatenating \( \sigma_2 \) to the end of \( \sigma_1 \), without changing the order within \( \sigma_1 \) and \( \sigma_2 \). Let \( \text{Proc}(\sigma) \) denote the set of processes \( p \in \mathcal{P} \) that occur in \( \sigma \) at least once, not counting symbols in \( P^\top \).

A configuration \( C \) and a schedule \( \sigma \in P^\Delta \) of length one result in a new configuration \( \text{Conf}(C, \sigma) \), obtained from \( C \) by process \( p \) taking its next step, if \( \sigma = p \in \mathcal{P} \), or by process \( p \) receiving the abort signal, if \( \sigma = p^\top \in P^\top \). If \( \sigma = \sigma_1 \sigma_2 \ldots \sigma_k \) is a schedule of length \( k > 1 \), then the new configuration is determined inductively as \( \text{Conf}(\text{Conf}(C, \sigma_1); \sigma_2 \ldots \sigma_k) \).

Configuration \( C \) and schedule \( \sigma = \sigma_1 \ldots \sigma_k \) also define an execution \( \text{Exec}(C, \sigma) \), which is a sequence \( s_1 s_2 \ldots s_k \), where \( s_i \) is the step executed or the abort signal received in the transition from \( C_{i-1} = \text{Conf}(C, \sigma_1 \ldots \sigma_{i-1}) \) to \( C_i = \text{Conf}(C_{i-1}, \sigma_i) \). To specify that an execution starting in \( C \) and running by schedule \( \sigma \) is running algorithm \( A \), we use \( \text{Exec}_{\Delta}(C, \sigma) \).

The length of an execution \( E \) is denoted by \( |E| \). We call \( s_i \) an abort step by process \( p \), if in \( s_i \) process \( p \) receives the abort signal. Let \( E_1 \) and \( E_2 \) be two executions. Then \( E_1 \circ E_2 \) is the execution obtained by concatenating the steps of \( E_2 \) after the steps of \( E_1 \), without changing the order of steps within \( E_1 \) and \( E_2 \).

The initial configuration is denoted by \( \Gamma \). A configuration \( C \) is reachable, if there exists a schedule \( \sigma \) such that \( \text{Conf}(\Gamma, \sigma) = C \). Since only reachable configurations are important in our algorithms and proofs, we use configuration instead of reachable configuration from this point on. For a configuration \( C \) we let \( \sigma \rightarrow_C \) denote an arbitrary but unique schedule such that \( \text{Conf}(\Gamma, \sigma \rightarrow_C) = C \), and we define \( E \rightarrow_C = \text{Exec}(\Gamma, \sigma \rightarrow_C) \).

The projection of a schedule \( \sigma \) to a set \( Q \subseteq P^\Delta \) is denoted by \( \sigma|Q \). For an execution \( E \) and a set \( Q \) of processes, \( E|Q \) denotes the sub-sequence of \( E \) that contains all (abort and shared memory) steps by processes in \( Q \).

Recall that a configuration \( C \) determines the state of each process. I.e., for any two executions \( E \) and \( E' \) resulting in the same configuration \( C \), each process is in the same state at the end of \( E \) as at the end of \( E' \), and in particular \( E|p = E'|p \). Therefore, we associate the state of a process in configuration \( C \) with \( E \rightarrow_C[p] \). (But note that if two executions \( E \) and \( E' \) are indistinguishable to each process in \( Q \subseteq \mathcal{P} \), then this does not in general imply that \( E|Q = E'|Q' \).) The value of register \( r \) in configuration \( C \) is denoted by \( \text{val}_C(r) \). Configurations \( C \) and \( D \) are indistinguishable to some process \( p \), if \( E \rightarrow_C[p = E \rightarrow_D[p \text{ and } \text{val}_C(r) = \text{val}_D(r) \text{ for every register } r \in \mathcal{R} \). For a set \( Q \subseteq \mathcal{P} \), we write \( C \sim_Q D \) to denote that configurations \( C \) and \( D \) are indistinguishable to each process in \( Q \); for a set consisting of a single process \( p \) we write \( C \sim_p D \) instead of \( C \sim_{\{p\}} D \).

**RMR Complexity.** Our lower bound applies to both, the standard asynchronous distributed shared memory (DSM) model and cache-coherent (CC) model. In fact, we use a model that combines both, caches as well as locally accessible registers for each process.

We assume that set of registers, \( \mathcal{R} \), is partitioned into disjoint memory segments \( \mathcal{R}_p \), for \( p \in \mathcal{P} \). The registers in \( \mathcal{R}_p \) are local to process \( p \) and remote to each process \( q \neq p \). We say that at the end of execution \( E \) a process \( p \) has a valid cache copy of register \( r \), if in \( E \) process \( p \) reads or writes \( r \) at some point, and no other processes writes \( r \) after that. Note that the configuration obtained at the end of an execution starting in \( E \) uniquely determines whether \( p \) has a valid cache copy of a register \( r \). The reason is that the state of \( p \) in configuration \( C \) determines the value that was written to or read from \( r \) when \( p \) accessed \( r \) last, and \( p \) has a valid cache copy of \( r \) if and only if \( \text{val}_C(r) \) equals that value. Let \( \text{Cache}_p(C) \) denote the
union of $\mathcal{R}_p$ and the set of registers of which process $p$ has a valid cache copy in configuration $C$ if $p$ has not terminated in $C$, and the empty set if $p$ is terminated in $C$.

A step in an execution $E$ is either local or remote (we say it incurs an RMR if it is remote). All abort steps are local. A non-abort step by process $p$ is local, if and only if it is either a read or a write of a register in $\mathcal{R}_p$, or it is a read of a register of which $p$ has a local cache copy.

For an execution $E$ and a process $p$, $RMR_p(E)$ is the number of RMR steps by process $p$ in execution $E$. Further, $RMR(E)$ is the number of RMR steps incurred by all processes in execution $E$. For $Q \subseteq P$ we define $RMR_Q(E) = \sum_{q \in Q} RMR_q(E)$, which is equal to the total number of RMRs incurred by processes in $Q$ in $E$. For the sake of conciseness, we use $RMR(E)$ instead of $RMR_P(E)$.

**Abortable Leader Election.** An algorithm solves abortable leader election, if for any schedule $\sigma$, in $Exec(\Gamma, \sigma)$ each process that terminates returns win or lose, at most one process returns win, and if all processes in $Proc(\sigma)$ return lose, then all processes in $Proc(\sigma)$ receive the abort signal.

We usually assume without explicitly saying so that an abortable leader election satisfies deadlock-freedom and bounded abort, defined as follows: Bounded abort means that after a process received the abort signal it terminates within a finite number of its own steps. An infinite execution $\sigma$ is $P$-fair for $P \subseteq \mathcal{P}$, if each process appears infinitely many times in $\sigma$. An infinite execution $E$ is $P$-fair for $P \subseteq \mathcal{P}$, if for some configuration $C$ and a $P$-fair schedule $\sigma$, it holds $E = Exec(C, \sigma)$. We use fair schedule and fair execution, instead of $P$-fair, when $P = \mathcal{P}$. An algorithm is deadlock-free if for any schedule $\sigma$ all processes terminate in $Exec(\Gamma, \sigma)$, provided this execution is fair.

### 3.2 Properties of Abortable Leader Election

In this section we derive the critical property that distinguishes non-abortable from abortable leader election for the purpose of the lower bound. We consider algorithms in which each process returns either win or lose upon termination. We call such algorithms binary. Note that any (abortable) leader election algorithm is a binary algorithm.

Several results in this section will concern only two arbitrarily selected processes in the $n$-process system for $n \geq 2$. For ease of notation, we will call these processes $a$ and $b$.

For an execution $E$ of a binary algorithm in which $a$ returns $x$ and $b$ returns $y$, let $(x, y)$ denote the outcome vector of $E$. For a binary algorithm $A$ and a configuration $C$, let $V_A(C)$ denote the set of all outcome vectors of $\{a, b\}$-only executions starting in $C$, in which processes $a$ and $b$ terminate.

First we observe that the outcome vectors of two indistinguishable configurations are equal.

**Observation 4.** For any binary algorithm $A$, if configurations $C$ and $D$ are indistinguishable to processes $a$ and $b$, then $V_A(C) = V_A(D)$.

**Proof.** Since $C$ and $D$ are indistinguishable to processes $a$ and $b$, $E_{\rightarrow C}[a = E_{\rightarrow D}[a, E_{\rightarrow C}[b = E_{\rightarrow D}[b]$, and for any register $r$, $val_C(r) = val_D(r)$. Thus, for any $x$ in $\{a, b\}^\Delta$, we have $(E_{\rightarrow C} \circ Exec(C, x))[a = (E_{\rightarrow D} \circ Exec(D, x))[a$, $(E_{\rightarrow C} \circ Exec(C, x))[b = (E_{\rightarrow D} \circ Exec(D, x))[b$, and for any register $r$, $val_{Conf(C,x)}(r) = val_{Conf(D,x)}(r)$. So by induction, for any $\{a, b\}$-only schedule $\sigma$, $Conf(C, \sigma) \sim_{\{a, b\}} Conf(D, \sigma)$. Therefore, if in $Exec(C, \sigma)$ process $p \in \{a, b\}$ terminates, it also terminates in $Exec(D, \sigma)$ and it returns the same value in both executions. Hence, the outcome vector $V_A(C)$ is equal to $V_A(D)$. \hfill $\blacksquare$
For a binary algorithm $A$, configuration $C$ is \textit{bivalent} if $\{(\text{win}, \text{lose}), (\text{lose}, \text{win})\} = V_A(C)$. This definition of bivalency refers to two fixed but arbitrarily chosen processes, $a$ and $b$. In a system with more than two processes, we may write $(a, b)$-bivalent to indicate the two processes $a$ and $b$ to which this definition applies. A configuration is \textit{strongly bivalent} (or strongly $(a, b)$-bivalent) if it is bivalent and a solo-run by any process $p \in \{a, b\}$, starting in $C$, results in $p$ winning.

A similar argument to the FLP Theorem \cite{20} implies that for any deadlock-free binary algorithm and for any reachable bivalent configuration, there exists an infinite execution, where no process terminates.

\textbf{Lemma 5.} Let $A$ be a deadlock-free binary algorithm and $C$ an $(a, b)$-bivalent configuration. There exists an infinite schedule $\sigma \in \{a, b\}^*$, such that in $\text{Exec}_A(C, \sigma)$ none of $a$ and $b$ terminate.

To prove this lemma we first prove Claim 6 and use the fact that none of $a$ and $b$ can be terminated in an $(a, b)$-bivalent configuration.

\textbf{Claim 6.} In any deadlock-free binary algorithm $A$, if configuration $C$ is $(a, b)$-bivalent, then either one of $\text{Conf}(C, a)$ and $\text{Conf}(C, b)$ is $(a, b)$-bivalent, or there exists an infinite $(a, b)$-only execution, where none of $a$ and $b$ terminate.

\textbf{Proof.} Since configuration $C$ is $(a, b)$-bivalent, $V_A(C) = \{(\text{win}, \text{lose}), (\text{lose}, \text{win})\}$. Suppose neither $\text{Conf}(C, a)$ nor $\text{Conf}(C, b)$ is $(a, b)$-bivalent. Then there exist distinct $x, y \in \{\text{win}, \text{lose}\}$ such that

\begin{align*}
V_A(\text{Conf}(C, a)) &= \{(x, y)\}, \quad \text{and} \\
V_A(\text{Conf}(C, b)) &= \{(y, x)\} \quad (1)
\end{align*}

We now distinguish two cases.

\textit{Case 1:} In $C$, processes $a$ and $b$ are poised to access different registers or poised to read the same register. Thus,

\begin{align*}
\text{Conf}(C, a \circ b) &= \text{Conf}(C, b \circ a). \quad (2)
\end{align*}

By (1), $(y, x) \notin V_A(\text{Conf}(C, a))$. Since $V_A(\text{Conf}(C, a \circ b)) \subseteq V_A(\text{Conf}(C, a))$, it holds $(y, x) \notin V_A(\text{Conf}(C, a \circ b))$. Thus, by (2), $(y, x) \notin V_A(\text{Conf}(C, b \circ a))$. Since $V_A(\text{Conf}(C, b \circ a)) \subseteq V_A(\text{Conf}(C, b)) = \{(y, x)\}$, this means $V_A(\text{Conf}(C, b \circ a)) = \emptyset$. But this contradicts deadlock-freedom, as in a fair schedule starting in $\text{Conf}(C, b \circ a)$ both processes must terminate and output something.

\textit{Case 2:} In configuration $C$, both processes are poised to access the same register $r$, and at least one of them is poised to write $r$. Without loss of generality, assume that $a$ is poised to write register $r$. If $a$ takes its write step after $b$’s step, then $a$’s state and shared register values are no different than if only $a$ takes its write step and $b$ does not take its step. So $\text{Conf}(C, a) \sim_a \text{Conf}(C, b \circ a)$. If process $a$ does not terminate in a solo-run starting in $\text{Conf}(C, a)$, then the claim is true, because there exists an infinite execution starting in $C$ that neither $a$ nor $b$ terminates. However, if process $a$ terminates in a solo-run starting in $\text{Conf}(C, a)$, by (1), we can conclude that $(x, y) \in V_A(\text{Conf}(C, b \circ a))$. Since $V_A(\text{Conf}(C, b \circ a)) \subseteq V_A(\text{Conf}(C, b))$, it holds that $(x, y) \in V_A(\text{Conf}(C, b))$. This contradicts $V_A(\text{Conf}(C, b)) = \{(y, x)\}$.

Any deadlock-free (non-abortable) 2-process leader election algorithm has a bivalent initial configuration. But in any fair schedule, both processes terminate. Therefore, the
infinite execution that is guaranteed by the above corollary cannot be fair; in particular, it requires one of the two processes to run solo at some point. However, one can construct a deadlock-free (non-abortable) leader election algorithm in which one process never takes an infinite number of steps, no matter what the schedule is. The lemma below shows that this is not true for abortable two-process leader election algorithm.

Lemma 7. Let $A$ be a deadlock-free abortable 2-process leader election algorithm with bounded aborts. For any process $p$, there exists an execution starting in the initial configuration, in which $p$ takes an unbounded number of steps.

Proof. Let $\Gamma$ be the initial configuration of $A$. For the purpose of contradiction, assume there is a fixed process, $a$, that terminates within a finite number of its own steps in all executions. Let $b$ be the other process.

By the safety property of abortable leader election, there is no execution in which both processes win, i.e.,

$$(\text{win, win}) \notin V_A(\Gamma).$$  (3)

Let algorithm $A'$ be the same as $A$ except that during any execution,

1. if any of the two processes receive the abort signal, the abort signal is ignored; and
2. if in step $s$ process $b$ reads $(a, x)$, where $x \neq \bot$, then $b$ continues its program, as if it had received the abort signal immediately after step $s$.

In any execution of $A'$, $a$ and $b$ can only both lose, if they both receive the abort signal. Since both ignore the abort signals (and only $b$ possibly simulates having received an abort signal), there is no execution of $A'$ in which $a$ and $b$ both lose. Thus, for the initial configuration $\Gamma'$ of $A'$,

$$(\text{lose, lose}) \notin V_{A'}(\Gamma').$$  (4)

Consider any execution $E' = \text{Exec}(\Gamma', \sigma')$ of algorithm $A'$ starting in $\Gamma'$. We now create an execution $E = \text{Exec}(\Gamma, \sigma)$ of $A$ starting in $\Gamma$, by scheduling the processes in exactly the same order as in $E'$, but removing all abort signals. Moreover, when for the first time $b$ reads a value of $(a, x)$ in $E$, where $x \neq \bot$ (if that happens), then we send process $b$ the abort signal. By construction of $A'$, processes $a$ and $b$ execute exactly the same shared memory steps in execution $E$ of algorithm $A$ as in execution $E'$ of algorithm $A'$. Thus, for every schedule $\sigma'$ there is a schedule $\sigma$ such that processes $a$ and $b$ execute in $\text{Exec}_{A'}(\Gamma', \sigma')$ the same shared memory steps as in $\text{Exec}_A(\Gamma, \sigma)$. This implies

$$V_{A'}(\Gamma') \subseteq V_A(\Gamma).$$  (5)

Note that in the construction above, if $\sigma'$ is fair, then so is $\sigma$. Hence, the fact that $A$ is deadlock-free implies

$$A'$$ is deadlock-free.  (6)

In algorithm $A$, in a sufficiently long solo-run by $a$, in which $a$ does not receive the abort-signal, process $a$ terminates (by deadlock-freedom) and returns $\text{win}$ (by the safety property of abortable leader election). Hence, in $A'$ process $a$ also terminates and returns $\text{win}$ after a sufficiently long solo-run, because it takes exactly the same steps as in $A$. Since $A'$ is deadlock-free by (6), process $b$ terminates after a sufficiently long solo-run following $a$’s solo-run, and by (5) process $b$ returns $\text{lose}$. With a symmetric argument, for algorithm
Lemma 8. Suppose \((3)\) and \((4)\) we conclude \(\{\text{terminate in any}\}
\). Applying a symmetric argument to a sufficiently long solo-run by \(b\) we have \(\{\text{lose}\}\). Then \(a\) processes \(a\). Similarly, since \(\text{Conf}\) receives the abort-signal in \(b\), \(b\) process \(b\) runs solo in \(\{\text{terminate in any}\}\). Hence, \(b\) returns \(\{\text{lose}\}\). Thus, \(\text{Conf}\) terminates within a finite number of its own steps. As a result, the same is true for \(A^{'\prime}\).

One of the core properties of the abortable leader election problem that allows us to prove the lower bound is that there are no reachable strongly bi-valent configurations in any execution.

**Lemma 8.** Let \(A\) be an abortable \(n\)-process leader election algorithm with bounded aborts for \(n \geq 2\). Further, let \(C\) be a reachable configuration and \(a, b\) two distinct processes that terminate in any \(\{a, b\}\)-fair execution starting in \(C\). For any schedule \(\sigma \in P^*\) configuration \(C = \text{Conf}(\Gamma, \sigma)\) is not strongly \(\{a, b\}\)-bivalent.

**Proof.** Suppose \(C\) is strongly \(\{a, b\}\)-bivalent. Then it is \(\{a, b\}\)-bivalent, so

\[ V_A(C) = \{(\text{lose}, \text{win}), (\text{win}, \text{lose})\}, \tag{8} \]

and if \(a\) or \(b\) runs solo in \(C\), then that process wins. Because \(\sigma \in P^*\), neither \(a\) nor \(b\) receives the abort-signal in \(\text{Exec}(\Gamma, \sigma)\). By the assumption that aborts are bounded, processes \(a\) and \(b\) both terminate in sufficiently long solo runs starting in \(\text{Conf}(C, a^\top)\) and \(\text{Conf}(C, b^\top)\), respectively. Let \(x\) and \(y\) be the return values of \(a\) in \(\text{Exec}(C, a^\top \circ a^{k_a})\) and of \(b\) in \(\text{Exec}(C, b^\top \circ b^{k_b})\), respectively, for sufficiently large integers \(k_a\) and \(k_b\).

Since \(\text{Conf}(C, a^\top) \sim_a \text{Conf}(C, a^\top b^\top)\),

\[ a \text{ returns } x \text{ in } \text{Exec}(C, a^\top b^\top \circ a^{k_a}). \tag{9} \]

Similarly, since \(\text{Conf}(C, b^\top) \sim_b \text{Conf}(C, a^\top b^\top)\),

\[ b \text{ returns } y \text{ in } \text{Exec}(C, a^\top b^\top \circ b^{k_b}). \tag{10} \]

We distinguish the following cases.

**Case 1:** \(x = y = \text{win}\): In a sufficiently long solo-run by \(b\) following \(\text{Exec}(C, a^\top b^\top \circ a^{k_a})\), process \(b\) must terminate (by deadlock-freedom). Since \(a\) wins in that execution, \(b\) must lose. Thus,

\[ (\text{win}, \text{lose}) \in V_A(\text{Conf}(C, a^\top b^\top)). \tag{11} \]

Applying a symmetric argument to a sufficiently long solo-run by \(a\) following \(\text{Exec}(C, b^\top a^\top \circ b^{k_b})\), we obtain

\[ (\text{lose}, \text{win}) \in V_A(\text{Conf}(C, a^\top b^\top)). \tag{12} \]
Hence, using (8), we get \( \{\text{win}, \text{lose}\}, \{\text{lose}, \text{win}\}\} = \mathcal{V}_A(\text{Conf}(C, a^\top b^\top)) \). Then by Lemma (8) there exists an infinite execution starting in \( \text{Conf}(C, a^\top b^\top) \), such that \( a \) and \( b \) do not terminate. This contradicts bounded aborts.

Case 2: \( x = y = \text{lose} \): In a sufficiently long solo-run by \( b \) following \( \text{Exec}(C, a^\top b^\top \circ a^k) \), process \( b \) must terminate (by deadlock-freedom). Since \( a \) loses in that execution, by (8), process \( b \) must win. Thus, \( (\text{lose}, \text{win}) \in \mathcal{V}_A(\text{Conf}(C, a^\top b^\top)) \), and with a symmetric argument \( (\text{win}, \text{lose}) \in \mathcal{V}_A(\text{Conf}(C, a^\top b^\top)) \). We get a contradiction for the same reasons as in Case 1.

Case 3: \( \{x, y\} = \{\text{win}, \text{lose}\} \): Without loss of generality, assume \( x = \text{win} \). Then in \( \text{Exec}(C, a^\top a^k) \) process \( a \) wins. On the other hand, since \( C \) is strongly bivalent, \( b \) wins in a sufficiently long solo-run starting in \( C \). Since \( C \sim_b \text{Conf}(C, a^\top) \), process \( b \) also wins in a long enough solo-run starting in \( \text{Conf}(C, a^\top) \). Hence, we have shown that any of the two processes in \( \{a, b\} \) wins in a solo-run starting in \( \text{Conf}(C, a^\top) \). By deadlock-freedom and (8) the other process loses, if it performs a long enough solo-run afterwards. This shows that \( \text{Conf}(C, a^\top) \) is strongly bivalent.

Now let \( A' \) be the 2-process algorithm in which \( a \) and \( b \) act exactly as in algorithm as \( A \), but the initial configuration is \( \Gamma' = \text{Conf}(C, a^\top) \). Then \( A' \) is a deadlock-free abortable 2-process leader election algorithm with bounded aborts: The bounded abort property is inherited from \( A \). Deadlock-freedom follows from the assumption that \( a \) and \( b \) terminate in any fair execution starting in \( C \). The safety property of abortable leader election follows from (8) and the fact that each process wins in a long enough solo-run starting in the initial configuration \( \text{Conf}(C, a^\top) \) (because that configuration is strongly bivalent).

Moreover, in \( A' \) process \( a \) always terminates within a finite number of its own steps. This follows from the bounded abort property of \( A \) and the fact that both processes simulate \( A \) starting in configuration \( \text{Conf}(C, a^\top) \), in which \( a \) has already received the abort-signal. This contradicts Lemma (7).

### 3.3 Properties of Executions and Safe Configurations

#### 3.3.1 Additional Assumptions

We make the following assumptions that do not restrict the generality of our results. Recall that processes are state machines, each using some infinite state space \( Q \). We assume that during an execution a process never enters the same state twice. Further, we assume that each register stores a pair in \( P \times (Q \cup \{\bot\}) \), where \( \bot \notin Q \). The initial value of each register in \( R_p \) is \( (p, \bot) \), and when a process \( p \) writes to any register, it writes a pair \( (p, x) \), where \( x \) is \( p \)'s state before its write operation. I.e., we are using a full information model, where processes write all information they have observed in the past. As a result, no two writes in an execution write the same value.

Each process’s first shared memory step is a read outside of its local shared memory segment, that we call invocation read, and thus incurs an RMR. Adding such a step to the beginning of each process’s program does not affect the asymptotic RMR complexity of the algorithm. We will assume that at the end of its execution, each process \( p \) reads all registers in \( R_p \) once. Since those reads do not incur any RMRs, this assumption can be made without loss of generality. We call \( p \)'s last read of register \( r \in R_p \) the terminating read of \( r \), and we assume that after \( p \)'s last terminating read, \( p \) will immediately enter a halting state.

#### 3.3.2 Terminology and Notation

We define some additional terms and notation.
We say process \( p \) is visible on register \( r \) in configuration \( C \) if \( \text{val}_C(r) = (p, x) \), for some \( x \in Q \). Let \( L(C) \) be the set of processes that have lost in configuration \( C \).

When we construct our high RMR execution, we need to make sure that whenever a process gains information about some other process that has not yet lost, someone pays for that with an RMR. To keep track of who knows who, we define a set \( K(C) \) that contains pairs \( (p, q) \) of processes. Informally, \( (p, q) \) is in \( K(C) \) if \( p \) has already gained information about process \( q \) in the execution leading to configuration \( C \), or \( p \) can gain such information for “free” (i.e., without an RMR being paid for that). Gaining information does not only mean that \( p \) reads a register that \( q \) has written; it means anything that might affect \( p \)’s execution, e.g., \( p \)’s cache copies being invalidated. \( K(C) \) is the union of three sets \( K_1(C) \), \( K_2(C) \), and \( K_3(C) \), defined as follows:

- \( K_1(C) \) is the set of all pairs \( (p, q) \), \( p \neq q \), such that in \( E_{\rightarrow C} \) process \( p \) reads a register while \( q \) is visible on that register. I.e., \( p \) reads a value of \( (q, x) \), where \( x \in Q \).
  
  Informally: \( p \) has learned about \( q \) in \( E_{\rightarrow C} \).

- \( K_2(C) \) is the set of all pairs \( (p, q) \), \( p \neq q \), such that in \( E_{\rightarrow C} \) process \( q \) takes at least one shared memory step and process \( p \) reads a register in \( R_q \).
  
  Informally: Process \( p \) may have a valid cache copy of a register \( r \in R_q \), and by writing to \( r \) process \( q \) can invalidate that cache copy without incurring an RMR.

- \( K_3(C) \) is the set of all pairs \( (p, q) \), \( p \neq q \), such that in \( E_{\rightarrow C} \) process \( p \) takes at least one shared memory step, and \( q \) writes to a register \( r \in R_p \) before \( p \)’s terminating read of \( r \).

  Informally: \( p \) may learn about \( q \) without incurring an RMR by scanning all its registers in \( R_p \).

Let \( K(C) = K_1(C) \cup K_2(C) \cup K_3(C) \). We say process \( p \) knows process \( q \) in configuration \( C \) if \( (p, q) \in K(C) \).

Recall that in our inductive construction of an RMR expensive execution, we will sometimes erase processes from the constructed execution. For that reason, if \( p \) knows about \( q \), i.e., \( (p, q) \in K(C) \), then we will not remove a process \( q \) from the execution \( E_{\rightarrow C} \). We achieve this by ensuring that whenever \((p, q) \in K(C), q \in L(C)\), and as discussed earlier no lost processes will be erased.

However, we have to be careful about cases in which \( p \) does not know directly about \( q \). For example, suppose process \( q \) writes to register \( r \) in execution \( E \), and later some process \( z \) overwrites \( r \) and finally \( p \) becomes poised to read \( r \). In our inductive construction we may want to remove either \( z \) or \( p \) from the execution, because we do not want \( z \) to be discovered by \( p \). However, removing \( z \) reveals \( q \) on register \( r \), and so now \( p \) may discover \( q \). To account for that we introduce the concept of hidden processes.

In particular, for a configuration \( C \) and a register \( r \) we define a set \( H_r(C) \) of processes hidden on \( r \) as follows:

1. For \( r \notin R_p, p \in H_r(C) \) if and only if either \( p \) does not access \( r \) in \( E_{\rightarrow C} \), or \( p \) accesses \( r \) in \( E_{\rightarrow C} \) at some point \( t \), and either no process writes \( r \) after \( t \), or at least one process that writes \( r \) after \( t \) is in \( L(C) \):
   
   Idea: If \( p \)'s write to \( r \) was overwritten by some processes, then at least one of them has lost and thus will not be erased from the execution. Hence, erasing a process does not reveal \( p \)'s write to any other process.

2. For \( r \in R_p, p \in H_r(C) \) if and only if any process other than \( p \) that writes to \( r \) in \( E_{\rightarrow C} \) is in \( L(C) \):
   
   Idea: If a process \( q \) wrote to a register \( r \) in \( p \)'s local memory segment, then \( q \) has lost. Therefore, \( q \) will not be erased from the execution. This is important because \( p \) can
read $r$ for free and we have to assume that it does so frequently, so erasing $q$ from the execution might change what $p$ observes in the execution.

Let $H(C) = \bigcap_{r \in R} H_r(C)$. We say process $p$ is hidden in configuration $C$, if $p \in H(C)$.

We finally define the concept of a safe configuration as follows. Configuration $C$ is safe, if

(S1) for any pair $(p, q) \in K(C)$, $q \in L(C)$, and
(S2) if $p \notin H(C)$, then either $p \in L(C)$, or $p$ takes no shared memory step in $E \to C$.

The first property ensures that no process $p$ knows another process $q$ that has not yet lost, and the second property says that all processes that are not hidden must have lost, or not even started participation. As a result, in an execution leading to a safe configuration, we can erase all processes that do not lose, without affecting any other processes. Formally, we will prove for a schedule $\sigma$, a safe configuration $C = \text{Conf}(\Gamma, \sigma)$ and a set of processes $P \supseteq L(C)$,

\[
\begin{align*}
\text{Exec}(\Gamma, \sigma) | P &= \text{Exec}(\Gamma, \sigma | P^\Delta); \\
\text{RMR}_P(\text{Exec}(\Gamma, \sigma)) &= \text{RMR}_P(\text{Exec}(\Gamma, \sigma | P^\Delta)); & \text{and} \\
\text{Cache}_p(C) &= \text{Cache}_p(\text{Conf}(\Gamma, \sigma | P^\Delta)) \text{ for all } p \in P.
\end{align*}
\]

Moreover, if $C$ is safe, then $\text{Conf}(\Gamma, \sigma | P^\Delta)$ is also safe.

### 3.3.3 Forcing Processes to Lose

Lemma 8 is a core lemma in the construction of an RMR-expensive execution, which states that we can force two processes to lose starting in a reachable configuration, that the two processes terminate in any fair execution of those two processes and win in their solo execution.

**Lemma 9.** Let $C$ be a reachable configuration, and $a, b \in P \setminus L(C)$ two distinct processes that do not receive the abort signal in $E \to C$. Further, assume that processes $a$ and $b$ both terminate in any $\{a, b\}$-fair execution starting in $C$. If each process in $\{a, b\}$ wins in its solo-run starting in $C$, then there exists a schedule $\sigma \in (\{a, b\}^\Delta)^*$, such that $a$ and $b$ lose in $\text{Exec}(C, \sigma)$.

**Proof.** For the purpose of contradiction, assume that for any execution $\text{Exec}(C, \sigma)$, where $\sigma \in (\{a, b\}^\Delta)^*$, in which $a$ and $b$ both terminate, one of the processes wins. Then $(\text{lose}, \text{lose}) \notin \mathcal{V}_A(C)$. Since a solo-run by either $a$ or $b$, starting in $C$, results in that process winning, $C$ is $\{a, b\}$-strongly bivalent. This contradicts Lemma 8. ▮

### 3.3.4 Projections

We continue by proving properties of the projection operation. First, the projection of a schedule to a superset of lost processes, $P$, does not change the execution of those processes, if any process that is known by a process in $P$ is lost.

**Claim 10.** Let $\sigma$ be a schedule, $C = \text{Conf}(\Gamma, \sigma)$, and $P \subseteq P$. If $L(C) \subseteq P$, and $q \in L(C)$ for any pair $(p, q) \in K(C)$, then

\[
\text{Exec}(\Gamma, \sigma) | P = \text{Exec}(\Gamma, \sigma | P^\Delta).
\]

**Proof.** We prove the claim by induction on the length of $\sigma$. If $\sigma$ is the empty schedule, then the claim is trivially true.
Now suppose that $\sigma = \sigma'\lambda$, where $\lambda \in \mathcal{P}^\Delta$ is a schedule of length one, and the inductive hypothesis is true for $\sigma'$, i.e.,

$$\text{Exec}(\Gamma, \sigma')|P = \text{Exec}(\Gamma, \sigma'|P^\Delta).$$

(14)

Let $D = \text{Conf}(\Gamma, \sigma')$, and $D' = \text{Conf}(\Gamma, \sigma'|P^\Delta)$. We will show that

$$\text{Exec}(D, \lambda)|P = \text{Exec}(D', \lambda|P^\Delta).$$

(15)

Then it follows from (14) that $\text{Exec}(\Gamma, \sigma'|\lambda)|P = \text{Exec}(\Gamma, \sigma'|P^\Delta)$, which completes the inductive step.

If $\lambda \notin P^\Delta$, then each of the two executions on the left and right hand side of (15) is the empty execution, so (15) is true. Now suppose $\lambda \in \{p, p^\top\}$ for some process $p \in P$. Then in $\text{Exec}(D, \lambda) = \text{Exec}(D, \lambda)|P$, either process $p$ receives the abort signal or process $p$ executes a shared memory operation. First assume that $p$ receives the abort signal or writes some value $x$ to a shared register $r$ in that step. By (14) process $p$ is in the same state in $D$ as in $D'$, so $p$ receives the abort signal or writes $x$ to register $r$, respectively, in $\text{Exec}(D', \lambda) = \text{Exec}(D', \lambda|P^\Delta)$. In either case (15) follows.

Now assume that in $\text{Exec}(D, \lambda) = \text{Exec}(D, \lambda)|P$, process $p = \lambda$ reads a register $r$. Since $p$ is in the same state in $D$ as in $D'$, it reads the same register $r$ in $\text{Exec}(D, \lambda|P^\Delta)$. We will show that $\text{val}_D(r) = \text{val}_{D'}(r)$. As a result, $p$ reads the same value in both executions, and thus (15) follows.

For the purpose of a contradiction, assume $\text{val}_D(r) \neq \text{val}_{D'}(r)$. First assume $\text{Exec}(\Gamma, \sigma')$ contains no write to register $r$. Then, by the assumption that $\text{val}_D(r) \neq \text{val}_{D'}(r)$, execution $\text{Exec}(\Gamma, \sigma'|P^\Delta)$ contains a write to $r$ by some process $q$. Since only processes in $P$ take steps in that execution, $q \in P$. But since $q$ does not write in $\text{Exec}(\Gamma, \sigma')$, we have $\text{Exec}(\Gamma, \sigma'|P \neq \text{Exec}(\Gamma, \sigma'|P^\Delta)$, contradicting (14).

Now assume $\text{Exec}(\Gamma, \sigma')$ contains a write to $r$, and let $w$ be the last such write, executed by some process $q$. Thus, $\text{val}_D(r) = (q, x)$ for some value $x \in Q$. Since in $\text{Exec}(D, \lambda)$ process $p$ reads register $r$, $(p, q') \in K_1(\text{Conf}(D, \lambda))$. Since $C = \text{Conf}(\Gamma, \sigma) = \text{Conf}(D, \lambda)$, we have $(p, q') \in K(C)$. Therefore, $q \in L(C)$ by the assumption of the claim that $C$ is safe. Because $L(C) \subseteq P$, it follows that $q \in P$. Therefore, by (14), $q$’s write $w$, with value $(q, x)$, also occurs in $\text{Exec}(\Gamma, \sigma'|P^\Delta)$, and $q$ does not write to $r$ again after $w$. By the assumption that $\text{val}_D(r) \neq \text{val}_{D'}(r)$, $\text{Exec}(\Gamma, \sigma'|P^\Delta)$ must contain another write $w'$ that is executed after $w$ by some process $q' \neq q$. All steps in that execution are performed by processes in $P$, so $q' \in P$. But then by (14), $w$ and $w'$ are executed in the same order in $\text{Exec}(\Gamma, \sigma')$, contradicting that $w$ is the last write to $r$ in that execution.

If $C$ is a safe configuration, then by (S1) $q \in L(C)$ for each pair $(p, q) \in K(C)$. Hence, from Claim (14) we immediately get:

**Corollary 11.** Let $\sigma$ be a schedule, $C = \text{Conf}(\Gamma, \sigma)$ and $P$ a set of processes such that $L(C) \subseteq P$. If $C$ is safe, then

$$\text{Exec}(\Gamma, \sigma)|P = \text{Exec}(\Gamma, \sigma|P^\Delta).$$

(16)

The projection of a schedule leading to a safe configuration to a superset of lost processes does not change the cached values of those processes.

**Claim 12.** Let $\sigma$ be a schedule, $P \subseteq P$, $C = \text{Conf}(\Gamma, \sigma)$, and $C' = \text{Conf}(\Gamma, \sigma|P^\Delta)$. If $C$ is safe and $L(C) \subseteq P$, then $\text{Cache}_p(C) = \text{Cache}_p(C')$ for each process $p \in P$. 
Proof. Let $E = \text{Exec}(\Gamma, \sigma)$, and $E' = \text{Exec}(\Gamma, \sigma|P^\Delta)$. Since $C$ is safe, and $L(C) \subseteq P$, by Theorem 11

$$E|P = E'.$$

(17)

Fix a process $p \in P$. First assume $p \in L(C)$. Thus, since $L(C') \subseteq L(C)$, we have $p \in L(C')$. By definition, $\text{Cache}_p(C) = \text{Cache}_p(C') = \emptyset$.

Now assume $p \notin L(C)$. We first show $\text{Cache}_p(C) = \text{Cache}_p(C')$. Let $r \in \text{Cache}_p(C)$. Then in some step $s$ of $E$ process $p$ accesses $r$, and no process writes to $r$ after step $s$. By (17), $p$ also executes step $s$ in $E'$. For the purpose of a contradiction assume $r \notin \text{Cache}_p(C')$. Then in $E'$ some process $q$ writes to $r$ after step $s$. Since only processes in $P$ take steps in $E'$, $q \in P$. But then by (17) process $q$ also writes to $r$ after step $s$ in $E|P$ and thus in $E$—a contradiction.

We now prove $\text{Cache}_p(C') \subseteq \text{Cache}_p(C)$. If $r \in \text{Cache}_p(C')$. If $r \in R_p$, then by definition $r \in \text{Cache}_p(C)$. So assume $r \notin R_p$. Then

in $E'$ process $p$ accesses $r$ and no process writes to $r$ after $p$’s last access.

(18)

By (17), $p$ also accesses $r$ in $E|P$, and thus in $E$. For the purpose of a contradiction assume $r \notin \text{Cache}_p(C)$. Therefore, some process writes to $r$ in $E$ after $p$’s last access of $r$. Since $C$ is safe, $p \notin L(C)$, and $p$ takes at least one shared memory step in $E_{\rightarrow C}$, we obtain from (S2) that $p \in H(C)$. Thus, by the assumption that $r \notin R_p$, by (H1) at least one process, $q$, that writes to $r$ in $E$ after $p$’s last access of $r$, must be in $L(C)$. Therefore, $q \in P$. Since $p \in P$, by (17), $q$ writes $r$ after $p$’s last access in $E'$. This contradicts (18).

Removing a winning process from a schedule that leads to a safe configuration does not affect the state and cache values of other processes.

Claim 13. Let $\sigma$ be a schedule, such that $C = \text{Conf}(\Gamma, \sigma)$ is safe. Further, let $p \in P$ and $P = P \setminus \{p\}$. If $p$ wins in $\text{Exec}(\Gamma, \sigma)$, then $\text{Exec}(\Gamma, \sigma|P = \text{Exec}(\Gamma, \sigma|P^\Delta)$, and $\text{Cache}_q(\text{Conf}(\Gamma, \sigma)) = \text{Cache}_q(\text{Conf}(\Gamma, \sigma|P))$, for all $q \in P$.

Proof. Because $p$ wins in $\text{Exec}(\Gamma, \sigma)$, we have $L(C) \subseteq P \subseteq P$. Now the claim follows immediately from the fact that $C$ is safe and Theorem 11 and Claim 12.

3.3.5 Safe Configurations

The following claims and lemmas describe the properties of safe configurations. First we show that if starting in a safe configuration, a process that has not yet received the abort signal takes a step which does not incur an RMR, then the resulting configuration is also safe.

Claim 14. Let $C$ be a safe configuration and $x \in \text{Proc}(\sigma_{\rightarrow C})$, such that $x^\top$ does not appear in $\sigma_{\rightarrow C}$. If $\text{RMR}(\text{Exec}(C, x)) = 0$, then $C' = \text{Conf}(C, x)$ is safe.

Proof. Let $s$ be the single step $\text{Exec}(C, x)$, and $r$ the register accessed in $s$. Since $x$ takes at least one shared memory step in $E_{\rightarrow C}$ (because $x \in \text{Proc}(\sigma_{\rightarrow C})$ and $x^\top$ does not appear in $\sigma_{\rightarrow C}$),

$s$ is not $x$’s first shared memory step in $E_{\rightarrow C} \circ s$.

(19)
Thus, we have shown that \( C \) does not suffice. Hence, in-visible on \( v \) does not write \( v \) to \( v \) after that. Since \( C \) is safe, \( q \) is not \( q \)’s first shared memory step in \( E_{\rightarrow C} \circ s \), in step \( s \) process \( p \) reads \( r \in R_q \), and \( p \) does not read any register in \( R_q \) throughout \( E_{\rightarrow C} \). Hence,

\[
q \text{ takes at least one shared memory step in } E_{\rightarrow C}.
\]  

Since \( s \) does not incur an RMR, \( r \in Cache_p(C) \), and \( p \) reads or writes \( r \) in \( E_{\rightarrow C} \), and no other process writes \( r \) after that. If \( p \) reads \( r \in R_q \) during \( E_{\rightarrow C} \), then by \( (23) \) \( p \notin K_2(C) \), which is a contradiction. Hence, in \( E_{\rightarrow C} \) process \( p \) writes \( r \), and no other process writes \( r \) after that. Since \( r \in R_q \) and \( p \notin L(C) \) (as in \( C \) \( p \) is poised to executes step \( s \)), we have \( q \notin H_s(C) \) according to (H2), and thus, \( q \notin H(C) \). By \( (24) \), \( q \notin L(C) \) and by the claim assumption \( q \) takes at least one step in \( E_{\rightarrow C} \). Therefore, (S2) is not satisfied, which contradicts the assumption that \( C \) is safe.

If \( (p, q) \notin K_3(C) \), then either \( s \) is a write by process \( q \) and \( r \in R_p \), or \( s \) is \( p \)’s first shared memory step. The latter is not possible because of \( (19) \). And if the former is the case, then \( s \) incurs an RMR, which contradicts the assumption that \( RMR(Exec(C, x)) = 0 \). Thus, we have shown that \( C \) satisfies (S1).

We will now prove that \( C' \) also satisfies (S2). Suppose not. Then there exists a process \( p \notin H(C) \), such that \( p \notin L(C') \) and \( p \) takes at least one shared memory step in \( E_{\rightarrow C} \). Since \( L(C) \subseteq L(C') \), we have \( p \notin L(C) \).

Recall that \( C \) is safe. If \( p \notin H(C) \), then by (S2) process \( p \) takes no shared memory steps in \( E_{\rightarrow C} \). As \( p \) takes a shared memory step in \( E_{\rightarrow C} \circ s \) we have \( x = p \), and in particular \( s \) is \( x \)’s first shared memory step. This contradicts \( (19) \).

If \( p \in H(C) \), then \( p \notin H(C) \), which means there exists some register \( v \), such that \( p \notin H_s(C') \). For \( v \in R_p \), then since \( p \notin H(C') \), by (H2) in \( E_{\rightarrow C} \) process \( z \notin L(C), z \neq p \), writes to \( v \). Then \( z \notin L(C) \), and so since \( p \in H(C) \), by (H2) process \( z \) does not write \( v \) in \( E_{\rightarrow C} \). Hence, \( Exec(C, x) \) is a write to \( v \in R_p \) by \( z \neq p \), and this write incurs an RMR. This contradicts the claim assumption, \( RMR(Exec(C, x)) = 0 \).
Now suppose $v \notin R_p$. Let $q' \neq p$ be the process such that $v \in R_{q'}$. Because $p \in H_v(C)$, there is a non-empty set $Z$ of processes that write $v$ after $p$’s last access of $v$ during $E_{\rightarrow C}$, and $Z \cap L(C) \neq \emptyset$. Since $L(C) \subseteq L(C')$, we have $Z \cap L(C') \neq \emptyset$. If step $s$ is not an access of register $v$, $Z$ is also the set of processes that write to $v$ after $p$’s last access of $v$ during $E_{\rightarrow C'}$. So $p$ is in $H_v(C')$. If step $s$ is an access of register $v$, then because $RMR(E_{\rightarrow C}) = 0$, process $p$ is not the process performing step $s$. Thus, $Z$ is a subset of processes that write to $v$ after $p$’s last access of $v$ during $E_{\rightarrow C'}$. Hence, $p$ is in $H_v(C')$.

We now show that a process $p$, which executes a solo-run starting from a safe configuration, must eventually either terminate or incur an RMR.

\textbf{Claim 15.} Let $C$ be a safe configuration, and let $p$ be an arbitrary process in $Proc(\sigma \rightarrow C) \setminus L(C)$, such that $p^\top$ does not appear in $\sigma_{\rightarrow C}$. There exists a non-negative integer $k$, such that in $Exec(C, p^k)$, process $p$ terminates or incurs an RMR.

\textbf{Proof.} Assume that there exists a process $p$ that does not terminate and does not incur any RMRs in an infinite solo-run starting in $C$. Let $P = L(C) \cup \{p\}$ and $\sigma = \sigma_{\rightarrow C}$. Since $C$ is safe, $p \in Proc(\sigma_{\rightarrow C})$, and $p$ incurs no RMRs in its solo-run starting in $C$, the conditions of Claim 14 are met. Hence, for any non-negative integer $t$, by applying Claim 14 $t$ times,

$$C_t = Conf(C, p^t) = Conf(\Gamma, \sigma \circ p^t)$$ is safe. (24)

Since only $p$ takes steps in $Exec(C, p^t)$, and $p$ does not terminate in its solo-run starting in $C$, we obtain $L(Conf(C, p^t)) = L(C) \subseteq P$. This together with (24) allows us to apply Theorem 11 to obtain

$$Exec(\Gamma, \sigma \circ p^t)|P \overset{\text{Theorem 11}}{=} Exec(\Gamma, (\sigma \circ p^t)|P^\Delta) = Exec(\Gamma, (\sigma|P^\Delta) \circ p^t).$$

Therefore, if process $p$ does not terminate or incur any RMRs in its $t$-step solo-run starting in $C$, then $p$ does not terminate or incur any RMRs in its $t$-step solo-run starting in $Conf(\Gamma, \sigma|P^\Delta)$. Since this is true for all $t \geq 0$, in the infinite execution $Exec(\Gamma, \sigma')$, where $\sigma' = (\sigma|P^\Delta) \circ p \circ p \circ ...$, process $p$ does not terminate. But schedule $\sigma'$ is fair, because each process in $Proc(\sigma') \setminus \{p\}$ is in $L(C)$ and thus loses in $Exec(\Gamma, \sigma')$, and $p$ performs infinitely many shared memory steps. This contradicts deadlock-freedom.

If at the end of an execution, which starts in a safe configuration, a process that terminates knows the same set of processes as in the beginning of that execution, then that process returns win.

\textbf{Claim 16.} Let $C$ be a safe configuration, $p \in \mathcal{P} \setminus L(C)$, and $\sigma$ a schedule, such that $p^\top$ does not appear in $\sigma_{\rightarrow C} \circ \sigma$, and

for any $(p, q) \in K(Conf(C, \sigma))$ either $q \in L(C)$ or $(p, q) \in K(C)$.

If $p$ terminates in $Exec(C, \sigma)$, then $p$ wins.

\textbf{Proof.} Let $C' = Conf(C, \sigma)$ and $P = L(C) \cup \{p\}$. First note that for any pair $(p, q) \in K(C')$ either $q \in L(C)$ or $(p, q) \in K(C)$ by (26), and since $C$ is safe, $q \in L(C)$ according to (S1). Thus, we can apply Claim 11 to configuration $C'$ and obtain

$$Exec(\Gamma, \sigma_{\rightarrow C'}|P^\Delta) = E_{\rightarrow C'}|P.$$ If $p$ terminates in $Exec(C, \sigma)$, then $p$ also terminates in $Exec(\Gamma, \sigma_{\rightarrow C} \circ \sigma) = E_{\rightarrow C'}$, and thus by the above in $Exec(\Gamma, \sigma_{\rightarrow C'}|P^\Delta)$. Thus, it suffices to show that $p$ does not lose in that
We prove that Lemma 17.

Then process \( p \) (27), and Claim 16, not appear in \( \sigma \rightarrow_C r \), and by the inductive hypothesis, \( \sigma \rightarrow_C r \). By deadlock-freedom, there is an integer \( k \geq 0 \) such that \( p \) terminates in \( \sigma \rightarrow_C \). The inductive hypothesis, \( p \) is in the same state in \( Conf(\Gamma, \sigma \rightarrow_C \Delta) \) as in \( Conf(\Gamma, (\sigma \rightarrow_C \Delta) \circ p_k) \). Thus, either \( x \) and \( y \) are both read steps, or they are both write steps, and in the latter case, the value written in step \( x \) also gets written in step \( y \). Thus, if \( x \) and \( y \) are both write steps, then \( x = y \).

Hence, assume \( x \) and \( y \) are both read steps. In that case, \( p \) reads the same register \( r \) in \( x \) as in \( y \). Let \( (a, b) \) be the value \( p \) reads in \( x \), and \( (c, d) \) the value \( p \) reads in \( y \). It suffices to show that \( (a, b) = (c, d) \).

First assume that \( r \) gets written in the last \( k \) steps of \( Exec(\Gamma, \sigma \rightarrow_C \Delta) \). Then it must be \( p \) that writes \( (a, b) \) to \( r \) itself (i.e., \( a = p \)), and by the inductive hypothesis (29), \( p \) writes the same pair in the last \( k \) steps of \( Exec(\Gamma, (\sigma \rightarrow_C \Delta) \circ p_k) \). Moreover, in neither execution it writes to \( r \) after writing \( (a, b) \) to that register. Hence, \( (a, b) = (c, d) \).

Now assume that \( r \) does not get written in the last \( k \) steps of \( Exec(\Gamma, \sigma \rightarrow_C) \). Then by the inductive hypothesis, \( r \) does not get written in the last \( k \) steps of \( Exec(\Gamma, (\sigma \rightarrow_C \Delta) \circ p_k) \). In particular, \( r \) has value \( (a, b) \) in configuration \( C = Conf(\Gamma, \sigma \rightarrow_C) \), and value \( (c, d) \) in configuration \( D = Conf(\Gamma, (\sigma \rightarrow_C \Delta)) \).

First assume no process writes to \( r \) in \( Exec(\Gamma, \sigma \rightarrow_C) \). Then by (28), no process writes to that register in \( Exec(\Gamma, \sigma \rightarrow_C \Delta) \), so \( (a, b) = (c, d) \) is the initial value of \( r \).
Hence, suppose \( r \) gets written in \( \text{Exec}(\Gamma, \sigma \rightarrow C) \), and thus the last process writing to \( r \) in that execution is \( a \). Recall that in step \( x \) process \( p \) reads \((a, b)\) from register \( r \), so \((p, a) \in K_1(C_1) \subseteq K(C_1)\). Then \((p, a) \in K(C)\). Since \( C \) is safe and by (S1), \( a \in L(C) \subseteq P \). Since \( a \in P \) is the last process to write to \( r \) in \( \text{Exec}(\Gamma, \sigma \rightarrow C) \), by (28), it is also the last process to write \( r \) in \( \text{Exec}(\Gamma, \sigma \rightarrow C | P^\Delta) \), and in both executions it writes the value \((a, b)\). Hence, \( r \) has the same value \((a, b)\) in configuration \( C \) as in \( D \).

Starting in a safe configuration, if the executions of two schedules from two disjoint sets of processes do not incur any RMRs, then the execution made up of the concatenation of those schedules does not incur any RMRs and the ordering does not matter.

**Claim 18.** Let \( C \) be a safe configuration, and \( Q_0, Q_1 \subseteq \text{Proc}(\sigma \rightarrow C) \) two disjoint sets of processes, such that for any \( j \in \{0, 1\} \) there exists \( \sigma_j \in (Q_0^\Delta)^* \) with \( \text{RMR}(\text{Exec}(C, \sigma_j)) = 0 \). Then

\[
\begin{align*}
(a) & \quad \text{Exec}(C, \sigma_0 \circ \sigma_1)(Q_j) = \text{Exec}(C, \sigma_j), \text{ for all } j \in \{0, 1\}, \\
(b) & \quad \text{RMR}(\text{Exec}(C, \sigma_0 \circ \sigma_1)) = 0.
\end{align*}
\]

**Proof.** In \( \text{Exec}(C, \sigma_0 \circ \sigma_1) \) all the steps by processes in \( Q_0 \) are executed before any of the steps by processes in \( Q_1 \). Thus, using \( Q_0 \cap Q_1 = \emptyset \), we obtain \( \text{Exec}(C, \sigma_0 \circ \sigma_1)(Q_0) = \text{Exec}(C, \sigma_0) \). Hence, Part (a) is true for \( j = 0 \). We now use induction on \(|\sigma_1|\) to prove Part (a) for \( j = 1 \), as well as to prove Part (b).

First consider the base case, \(|\sigma_1| = 0\). Then \( \sigma_0 \circ \sigma_1 = \sigma_0 \) and

\[
\text{Exec}(C, \sigma_0 \circ \sigma_1) = \text{Exec}(C, \sigma_0). \tag{30}
\]

Therefore, \( \text{Exec}(C, \sigma_0 \circ \sigma_1)(Q_j) = \text{Exec}(C, \sigma_j) \). Since \( Q_0 \cap Q_1 = \emptyset \) and \( \sigma_0 \in (Q_0^\Delta)^* \), \( \text{Exec}(C, \sigma_0)(Q_1) \) is the empty execution, which is equal to \( \text{Exec}(C, \sigma_1) \). Thus \( \text{Exec}(C, \sigma_0 \circ \sigma_1)(Q_1) = \text{Exec}(C, \sigma_1)|Q_1 \). This proves Part (a). From the claim’s assumption \( \text{RMR}(\text{Exec}(C, \sigma_0)) = 0 \), and (30) we obtain \( \text{RMR}(\text{Exec}(C, \sigma_0 \circ \sigma_1)) = 0 \). This proves Part (b).

Now suppose \(|\sigma_1| > 0\), and the inductive hypothesis has been proven for the prefix \( \sigma'_1 \) of \( \sigma_1 \) of length \(|\sigma_1| - 1 \). I.e.,

\[
\text{Exec}(C, \sigma_0 \circ \sigma'_1)(Q_1) = \text{Exec}(C, \sigma'_1); \quad \text{and} \tag{31}
\]

\[
\text{RMR}(\text{Exec}(C, \sigma_0 \circ \sigma'_1)) = 0. \tag{32}
\]

First, assume that \( \sigma_1 = \sigma'_1 \circ p^\top \) for \( p \in Q_1 \). Then \( \text{RMR}(\text{Exec}(C, \sigma_0 \circ \sigma_1)) = \text{RMR}(\text{Exec}(C, \sigma_0 \circ \sigma'_1)) \). Thus, by (32), Part (b) is true. Moreover,

\[
\begin{align*}
\text{Exec}(C, \sigma_0 \circ \sigma_1)(Q_1) & = \text{Exec}(C, \sigma_0 \circ \sigma'_1 \circ p^\top)(Q_1) \tag{33} \\
& = \text{Exec}(C, (\sigma_0 \circ \sigma'_1)(Q_1) \circ p^\top) \\
& = \text{Exec}(C, \sigma'_1 \circ p^\top) \tag{34} \end{align*}
\]

This proves Part (a) for \( j = 1 \).

Now assume \( \sigma_1 = \sigma'_1 \circ p \) for \( p \in Q_1 \). Let \( s \) be the last step in \( \text{Exec}(C, \sigma_0 \circ \sigma_1) \), and \( s' \) the last step in \( \text{Exec}(C, \sigma_1) \). We will show:

\[
s = s'; \quad \text{and} \tag{33}
\]

\[
\text{step } s \text{ incurs no RMR in execution } \text{Exec}(C, \sigma_0 \circ \sigma_1) = \text{Exec}(C, \sigma_0 \circ \sigma'_1) \circ s. \tag{34}
\]
Then Part (b) follows immediately from \( [32] \) and \( [34] \), and Part (a) for \( j = 1 \) from

\[
\text{Exec}(C, \sigma_0 \circ \sigma_1)|Q_1 = (\text{Exec}(C, \sigma_0 \circ \sigma'_1)|Q_1) \circ s \quad \text{and} \quad \text{Exec}(C, \sigma'_1) \circ s \quad \text{and} \quad \text{Exec}(C, \sigma_1).
\]

First note that using \( [31] \) and because \( p \in Q_1 \) we have

\[
\text{in } \text{Conf}(C, \sigma'_1) \text{ process } p \text{ is in the same state as in } \text{Conf}(C, \sigma_0 \circ \sigma'_1).
\]

(35)

We separately consider the case that \( s \) is a read and that \( s \) is a write.

Case 1: Step \( s \) is a write. By \( [34] \) process \( p \) writes the same value to the same register in \( s \) as in \( s' \). This implies \( [33] \). Moreover,

\[
\text{RMR(Exec}(C, \sigma'_1) \circ s') = \text{RMR(Exec}(C, \sigma'_1 \circ p)) = \text{RMR(Exec}(C, \sigma_1)) = 0,
\]

where the last equality follows from the claim’s assumption. Hence, \( s' \) does not incur an RMR, which is only possible if in \( s' \) process \( p \) writes a register in \( R_p \). Because \( s = s' \), \( s \) does not incur an RMR either, and so \( [34] \) follows.

Case 2: Step \( s \) is a read. Let \( r \) be the register process \( p \) reads in step \( s \), and thus by \( [34] \), also in \( s' \).

We first prove \( [34] \). To that end we will show that the value of \( r \) is the same in \( \text{Conf}(C, \sigma_0 \circ \sigma'_1) \) as in \( \text{Conf}(C, \sigma'_1) \). As a result, in step \( s \) process \( p \) reads the same value from \( r \) as in step \( s' \), and so \( s = s' \).

All writes to \( r \) in \( \text{Exec}(C, \sigma'_1) \) are by processes in \( Q_1 \) and thus they occur also in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \) in the same order. Hence if there is a write to \( r \) in \( \text{Exec}(C, \sigma'_1) \), then the value at the end of \( \text{Exec}(C, \sigma'_1) \) is the same as at the end of \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \). In that case \( p \) reads the same value in \( s \) as in \( s' \).

Therefore, assume that \( r \) does not get written in \( \text{Exec}(C, \sigma'_1) \). If it also does not get written in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \), then \( r \) has the same value at the end of both executions, and \( p \) reads that value in both, \( s \) and \( s' \). So suppose \( r \) gets written in \( \text{Exec}(C, \sigma_0) \) but not in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \), and for the last time it gets written by a process \( q \). Then \( q \in Q_0 \), and since \( \text{RMR(Exec}(C, \sigma_0)) = 0, r \notin R_q \).

Since \( p \in Q_1 \), we have \( p \neq q \), and thus \( r \notin R_p \). Process \( p \) reads \( r \) during \( \text{Exec}(C, \sigma_1) \) at least once (in its last step \( s \)). By the claim’s assumption no such read by \( p \) incurs an RMR, so \( r \in \text{Cache}_{p}(C) \). But then in \( E \rightarrow C \) process \( p \) reads or writes register \( r \in R_q \) before \( q \)'s terminating read (because \( q \) writes \( r \) in \( \text{Exec}(C, \sigma_0) \)). If \( p \) reads \( r \) in \( E \rightarrow C \), then \( (p, q) \in K_2(C) \), and if \( p \) writes \( r \) in \( E \rightarrow C \), then \( (q, p) \in K_3(C) \). Hence, we have either \( (p, q) \in K(C) \) or \( (q, p) \in K(C) \). Since \( C \) is safe, \( (81) \) implies either \( q \in L(C) \) or \( p \in L(C) \). But neither is possible, as \( q \) takes a step in \( \text{Exec}(C, \sigma_0) \) (its write to \( r \)) and \( p \) a step in \( \text{Exec}(C, \sigma_1) \) (step \( s \)). This is a contradiction, and completes the proof of \( [34] \).

Thus, it remains to show \( [34] \), i.e., that \( s \) incurs no RMR in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \circ s \). If \( r \in R_p \), then this is obviously true, so assume \( r \notin R_p \). Since \( s' = s \) does not incur an RMR in \( \text{Exec}(C, \sigma'_1) \circ s' \) process \( p \) reads \( r \) during \( \text{Exec}(C, \sigma'_1) \), and \( r \) does not get written afterwards. By \( [34] \) the same is true in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \). Hence, at the end of that execution \( p \) has a valid cache copy of \( r \), so \( s \) does not incur an RMR in \( \text{Exec}(C, \sigma_0 \circ \sigma'_1) \circ s \). □

Starting in a safe configuration, if a process terminates without incurring any RMR steps, it does not gain information and hence wins.
Claim 19. Let $C$ be a safe configuration, and $p$ a process in $\text{Proc}(\sigma \rightarrow C) \backslash L(C)$, such that $p \uparrow$ does not appear in $\sigma \rightarrow C$. If $p$ terminates without incurring any RMRs in $E = \text{Exec}(C, p^k)$, for some positive integer $k$, then $p$ wins in $E$.

Proof. Let $C' = \text{Conf}(C, p^k)$, for arbitrary $k' \in \{1, \ldots, k\}$. Because $p$ is the only process that takes steps in $E$, it is true that $(K_3(C') \backslash K_3(C)) \cap \{\{p\} \times P\} = \emptyset$ (remember that $K_3(C)$ is the set of all pairs $(a, b), a \neq b$, such that in $E \rightarrow C$ process $a$ takes at least one shared memory step, and $b$ writes to a register $r \in R_p$ before $a$’s terminating read of $r$). Since $p$ does not incur any RMRs in $E$, if $p$ reads some register $r$ during $E$, then either $r \in R_p$, or $r \in \text{Cache}_p(C)$. Thus, $(K_2(C') \backslash K_2(C)) \cap \{\{p\} \times P\} = \emptyset$, and $(K_1(C') \backslash K_1(C)) \cap \{\{p\} \times P\} = \emptyset$. Hence, $(K(C) \backslash K(\text{Conf}(C, p^k))) \cap \{\{p\} \times P\} = \emptyset$, for any $k' \in \{1, \ldots, k\}$. Thus, by Lemma 10, $p$ wins in $E$. \hfill \blacktriangle

As long as the set of knowing relations does not change during an execution starting from a safe configuration, at most one process terminates.

Claim 20. Let $C$ be a safe configuration, such that if $p \uparrow \in P \uparrow$ appears in $\sigma \rightarrow C$, then $p \in L(C)$. Then for any schedule $\sigma \in \mathcal{P}^*$, when $K(C) = K(\text{Conf}(C, \sigma))$, at most one process terminates in $\text{Exec}(C, \sigma)$.

Proof. Let $\sigma \in \mathcal{P}^*$, such that $K(C) = K(\text{Conf}(C, \sigma))$. Assume that in $E = \text{Exec}(C, \sigma)$ two distinct processes, $p$ and $q$, terminate. Since we assumed that $p$ terminates in $E$, process $p$ is not terminated in $C$, and hence, $p \in P \backslash L(C)$. Because $K(C) = K(\text{Conf}(C, \sigma))$, the set $K(C) \backslash K(\text{Conf}(C, \sigma)) \cap \{\{p\} \times P\} = \emptyset$. Further, by the claim statement, $p \uparrow$ does not appear in $\sigma \rightarrow C$ and $\sigma$. Thus, by Claim 10, $p$ wins in $\text{Exec}(C, \sigma)$, and by symmetry, $q$ wins in $\text{Exec}(C, \sigma)$. This contradicts the safety property of abortable leader election. \hfill \blacktriangle

Projecting a schedule, that leads to a safe configuration, to a superset of all lost processes leads to a safe configuration.

Claim 21. Let $\sigma$ be a schedule, such that $C = \text{Conf}(\Gamma, \sigma)$ is safe. Let $P$ be a set of processes, such that $L(C) \subseteq P \subseteq \text{Proc}(\sigma)$. Then $C' = \text{Conf}(\Gamma, \sigma[P^\Delta])$ is safe.

Proof. For the purpose of contradiction assume that $C'$ is not safe. First assume there exists a process $p \notin H(C')$, such that $p$ takes at least one shared memory step in $E \rightarrow C'$ and $p \notin L(C')$. Because $p$ takes at least one shared memory step in $E \rightarrow C'$, $p \in P$. Since $C$ is safe, for any pair $(p,q) \in K(C)$, process $q$ is in $L(C)$. Hence, by Claim 10, $\text{Exec}(\Gamma, \sigma)[P = \text{Exec}(\Gamma, \sigma[P^\Delta])$. Therefore, $p$ takes at least one shared memory step in $E \rightarrow C'$ and $p \notin L(C')$. Because $p \notin H(C')$, there exists a register $r \in \mathcal{R}$, such that $p \notin H_r(C')$.

If $r \in R_p$, then at least one process that writes to $r$ in $E \rightarrow C'$ is not in $L(C')$. Let $q$ be one of the processes that write to $r$ in $E \rightarrow C'$ and are not in $L(C')$. Since $q$ takes a step in $E \rightarrow C'$, process $q$ is in $P$, and by Claim 10 takes the same write step to $r$ and is not in $L(C)$. Therefore, $p \notin H_r(C)$, which contradicts $C$ being safe.

If $r \notin R_p$, then in $E \rightarrow C'$, process $p$ writes to $r$, and at least one process, $q$, writes to $r$ after $p$’s write, such that $q \notin L(C')$. Since $q$ takes a step in $E \rightarrow C'$, process $q$ is in $P$, and by Claim 10 takes the same write step to $r$ and is not in $L(C)$. Therefore, $p \notin H_r(C)$, which contradicts $C$ being safe.

Now assume that for any $p \notin H(C')$, either $p \in L(C')$ or $p$ does not take any shared memory steps in $E \rightarrow C'$. Then there exists a pair $(p,q) \in K(C') \backslash K(C)$, such that $q \notin L(C')$.

If $(p,q) \in K_1(C') \backslash K_1(C)$, then both $p$ and $q$ take steps in $E \rightarrow C'$ ($p$ takes at least a read step, and $q$ takes at least a write step), and thus, are in $P$. If $(p,q) \in K_2(C') \backslash K_2(C)$, then
both \( p \) and \( q \) take steps in \( E \rightarrow C \) (\( p \) takes at least a read step, and \( q \) takes at least a shared memory step), and thus, are in \( P \). If \( (p,q) \in K_3(C') \setminus K_3(C) \), then both \( p \) and \( q \) take steps in \( E \rightarrow C \) (\( p \) takes at least a shared memory step, and \( q \) takes at least a write step), and thus, are in \( P \). Hence, by Claim 10, \( p \) and \( q \) take the same steps in \( E \rightarrow C \) and \( E \rightarrow C' \). This contradicts \( (p,q) \in K(C') \setminus K(C) \).

\[\Box\]

### 3.3.6 Auxiliary Claims

We now show that during an execution, the knowing relations can only change as a result of a shared memory step by one of the processes, that is in the difference of the relation sets.

**Claim 22.** Let \( E = \text{Conf}(C,A) \), \( C \) a configuration, and \( C' = \text{Conf}(C,A) \). If there exists a pair \( (p,q) \) in the symmetric set difference of \( K(C') \) and \( K(C) \), then \( \text{Exec}(C,A) \) is a shared memory step by \( p \) or \( q \).

**Proof.** Let \( s = \text{Exec}(C,A) \), and \( (p,q) \) be a pair in the symmetric set difference of \( K(C) \) and \( K(C') \). Step \( s \) causes the difference between \( K_1(C) \cup K_2(C) \cup K_3(C) \) and \( K_1(C') \cup K_2(C') \cup K_3(C') \). If \( K_1(C) \neq K_1(C') \), then in step \( s \) process \( p \) reads a register on which \( q \) is visible. If \( K_2(C) \neq K_2(C') \), then either \( s \) is \( q \)'s first shared memory step, or in step \( s \) process \( p \) reads a register in \( R_q \). Finally, if \( K_3(C) \neq K_3(C') \), then \( s \) is \( p \)'s first shared memory step, or in step \( s \) process \( q \) writes to a register in \( R_p \). In all cases, \( s \) is a shared memory step by \( p \) or \( q \).

If two executions are equal when projected to a set of processes, \( P \), then each process in \( P \) takes the same number of RMR steps and knows the same set of processes in \( P \) at the end of the execution.

**Claim 23.** Let \( P \) be a set of processes, \( \sigma \) and \( \sigma' \) schedules, and define \( E = \text{Exec}(\Gamma,\sigma) \), \( E' = \text{Exec}(\Gamma,\sigma') \), \( C = \text{Conf}(\Gamma,\sigma) \), and \( C' = \text{Conf}(\Gamma,\sigma') \). If \( E \mid P = E' \mid P \), then

(a) \( RMR_p(E) = RMR_p(E') \), for any process \( p \in P \), and

(b) \( K(C) \cap (P \times P) = K(C') \cap (P \times P) \).

**Proof.** Recall that we assume without loss of generality, that a value does not get written twice in the same execution. Hence, if \( p \) reads a value \( v \) from register \( r \) in execution \( E \), then that read incurs no RMR if and only if \( p \) accessed \( r \) earlier, and in its preceding access of \( r \) process \( p \) either read or wrote the same value \( v \). Therefore, \( E \mid P \) uniquely determines which of \( p \)'s steps are RMRs, and in particular \( RMR_p(E) \). This proves Part (a).

We will show that \( K(C) \cap (P \times P) \subseteq K(C') \cap (P \times P) \). By symmetry, this implies \( K(C') \cap (P \times P) \subseteq K(C) \cap (P \times P) \), and thus Part (b). Let \((a,b) \in K(C) \cap (P \times P) \). Then \( a, b \in P \), and \((a,b) \in K_1(C) \cup K_2(C) \cup K_3(C) \).

If \((a,b) \in K_1(C) \), then in some step of execution \( E \) process \( a \) reads a value \((b,x) \), for some register \( r \). Since \( E \mid P = E' \mid P \), in \( E' \) process \( a \) reads \((b,x) \) from \( r \). Thus, \((a,b) \in K(C') \).

If \((a,b) \in K_2(C) \), then in \( E \) process \( a \) reads a register \( r \in R_b \), and \( b \) takes at least one shared memory step. As \( E \mid P = E' \mid P \), process \( b \) takes at least one shared memory step in \( E' \) and \( a \) reads \( r \) in \( E' \). Therefore, \((a,b) \in K(C') \).

If \((a,b) \in K_3(C) \), then in \( E \) process \( a \) takes at least one shared memory step, and \( b \) writes a register \( r \in R_a \), before \( a \)'s terminating read of \( r \). Since \( E \mid P = E' \mid P \), process \( a \) takes at least one shared memory step in \( E' \), and \( b \) writes \( r \) in \( E' \), before \( a \)'s terminating read of \( r \). Hence, \((a,b) \in K(C') \).

Thus, \( K(C) \cap (P \times P) \subseteq K(C') \cap (P \times P) \).
3.4 Constructing an RMR-Expensive Execution

We now consider an abortable leader election algorithm. We will construct a schedule such that in an execution starting in the initial configuration at least one process takes $\Omega(\log n / \log \log n)$ RMR steps, where $n$ is the number of processes.

3.4.1 Overview of the Construction

Let $n \geq 4$, $\ell = \lfloor \log n/c \log \log n \rfloor$ for some sufficiently large constant $c$ (which we determine in the appendix). We inductively construct a schedule $\sigma_i$ and a set of processes $P_i \subseteq \mathcal{P}$, for all $i \in \{0, ..., \ell\}$. For the sake of conciseness, let $E_i = \text{Exec}(\Gamma, \sigma_i)$, $C_i = \text{Conf}(\Gamma, \sigma_i)$, and $L_i = L(C_i)$.

The construction will satisfy the following invariants for $i \in \{0, ..., \ell\}$:

(I) $C_i$ is safe.

(II) $|P_i \setminus L_i| \geq (n - 1)/(\log n)^c$.

(III) $\text{RMR}_P(P_i \setminus \text{L}_i)(C_i) \geq i |P_i \setminus L_i| - i$.

(IV) For each process $p \in P_i \setminus L_i : \text{RMR}_p(C_i) \leq i$.

(V) For each process $p \in P_i \setminus L_i$, $p^\top$ does not appear in $\sigma_i$.

Invariant (II) for $i = \ell$ implies $|P_\ell \setminus L_\ell| \geq 2$. Hence, by (III) there are at least two processes that each incur $\Omega(\ell) = \Omega(\log n / \log \log n)$ RMRs. Theorem 3 follows.

We now sketch how we construct $\sigma_i$ and $P_i$ inductively so that the invariants are satisfied. We start with $P_0 = \mathcal{P}$ and the initial configuration $C_0$. We then schedule processes in rounds. In round $i$, we choose a subset $P_{i+1}$ of the processes in $P_i \setminus L_i$ and remove all processes in $\mathcal{P} \setminus (P_{i+1} \cup L_i)$ from the execution constructed so far. This does not affect any of the remaining processes, because $C_i$ is safe. Then we schedule the processes in $P_{i+1}$ in such a way that each of them incurs an RMR, and only a small fraction of them lose.

To decide which processes to remove and to schedule the remaining processes, we proceed as follows: First we let each process in $P_i \setminus L_i$ take sufficiently many steps until it is poised to incur an RMR. It is not hard to see that in an execution in which no process incurs an RMR, processes do not learn about each other, so the resulting configuration, $D_i$, is again safe. Moreover, in a safe configuration processes only know about lost processes, so they cannot lose.

We then distinguish between a high contention write case, where a majority of processes are poised to write to few registers, and a low contention write case, where either many registers are poised to be accessed or a majority of processes are poised to read. Let $S_i$ be the set of registers processes in $P_i \setminus L_i$ are poised to access in configuration $D_i$. The high contention write case occurs if there are few such registers and a majority of processes are poised to write, i.e., $|S_i| = O(|P_i \setminus L_i| / \log n)$, and otherwise the low contention write case occurs.

In the low contention write case, we choose a set $Q_i$ of processes, which contains for each register $r \in S_i$ at most one process poised to write to $r$ in $D_i$. We consider the step $s_p$ each process $p \in Q_i$ is poised to take. We then create a directed graph $G$ with processes as vertices, and an edge from $p$ to $q$ if in the resulting configuration (I) due to $s_p$ or $s_q$ process $p$ knows $q$, or (II) due to step $s_p$ process $q$ is not hidden. Each application of rule (I) must be paid for by RMRs in the execution, and for each application of (II) a process $p$ must overwrite some process $q$. As a result graph $G$ is sufficiently spares, and by Turán’s theorem we obtain a large independent set $J$. We let each process $p \in J$ take one step, $s_p$, and erase all remaining processes that haven’t lost yet from the execution. It is not hard to see that no process loses in any of the steps added, the resulting configuration is safe.
Claim 24. Since this follows from how we added edges to \( G \) and, because of the sparsity of the graph, a sufficiently large number of processes survive. From that we obtain Invariants (I1) and (I2).

Since each process \( p \) performs an RMR in step \( s_p \) and only local steps before that, we get (I3) and (I4). Moreover, we don’t abort any processes, so (I5) is true.

In the high contention write case, we erase all readers from the execution. For each register \( r \in S_i \), let \( W_r \) denote the set of processes poised to write to \( r \). Since this is a high contention case, \(|W_r|\) is large for most registers \( r \). For each register \( r \) with sufficiently large \(|W_r|\), we choose two distinct processes \( a, b \in W_r \).

We then argue that, after erasing some \( O(\log n) \) processes, we obtain a configuration \( D'_i \) and an \( \{a, b\} \)-only schedule \( \sigma \) such that in execution \( \text{Exec}(D'_i, \sigma) \) processes \( a \) and \( b \) both lose and see no process other than those in \( L_i \), which have lost already. The argument is based on Lemma \[\text{Lemma}\] but quite involved. We now let, starting from \( D'_i \), all processes in \( W_r \setminus \{a, b\} \) execute one step, in which they write to \( r \). After that we schedule \( a \) and \( b \) as prescribed by \( \sigma \). Then \( a \) and \( b \) will both first write to \( r \), and thus overwrite the writes by all other processes in \( W_r \), then continue to take steps and lose without seeing any processes that haven’t lost, yet. As a result, all processes in \( W_r \setminus \{a, b\} \) have taken a step but are now hidden, two processes \( (a \text{ and } b) \) have lost, and \( O(\log n) \) processes have been removed. It is not hard to see that the resulting configuration is safe again. We repeat this for all registers \( r \) for which \(|W_r|\) is large enough. Then, we let \( P_{i+1} \) denote the set of all surviving processes and \( C_{i+1} \) the resulting configuration.

Configuration \( C_{i+1} \) is safe, and sufficiently few processes are removed or have lost so that (I1) and (I2) remain true. Moreover, each process that does not lose performs exactly one RMR, so (I3) and (I4) are true. (I5) is true because all processes that received the abort signal lost.

3.4.2 Partial Execution Constructions

One of the critical properties that results in constructing a long enough execution, is that we can keep many processes running while keeping them from gaining information. What follows are the formal description and proofs of this property.

First, we claim that the information exchanged during specific executions is bounded.

Claim 24. Let \( C \) be a safe configuration, \( P = \text{Proc}(\sigma \rightarrow C) \setminus L(C) \), and \( \sigma \in P^* \), such that in \( C \) each process in \( P \) is poised to perform an RMR step, and in \( \text{Exec}(C, \sigma) \) each process takes at most one step and each register gets written at most once. Then

\[
\begin{align*}
\text{(a)} & \quad |K(\text{Conf}(C, \sigma)) \cap (P \times P)| \leq 2RMR(\text{Exec}(C, \sigma)). \\
\text{(b)} & \quad \text{Let } M \text{ be the set of pairs } (p, q) \in (P \times P), \quad p \neq q, \quad \text{such that in } \text{Exec}(C, \sigma), \quad \text{process } q \quad \text{writes a register in } R_p \cup \text{Cache}_p(C). \quad \text{Then } |M| \leq RMR(\text{Exec}(C, \sigma)).
\end{align*}
\]

Proof. Since \( C \) is safe, by (S1), \( K(C) \cap (P \times P) \) is the empty set. Thus, to prove Part (a) it is sufficient to show that each step in \( \text{Exec}(C, \sigma) \) adds at most two pairs of processes to \( K(\text{Conf}(C, \sigma)) \setminus K(C) \) \cap (P \times P). Let \( \sigma' \) be a proper prefix of \( \sigma \), and \( p \) a process so that \( \sigma' \circ p \) is also a prefix of \( \sigma \). Since \( p \)’s state is the same in \( \text{Conf}(C, \sigma') \) as in \( C \), and \( p \) is poised to perform an RMR step in \( C \), the step \( \text{Exec}(\text{Conf}(C, \sigma'), p) \) incurs an RMR. Now let \( C_1 = \text{Conf}(C, \sigma') \) and \( C_2 = \text{Conf}(C, \sigma' \circ p) \).

First assume step \( \text{Exec}(C_1, p) \) is a read from some register \( r \in R_{q_2}, q_2 \in P \). Let \((q_1, x) = \text{val}_{C_1}(r) \) (if \( r \) is in its initial state, then \( x = \bot \) and \( q_1 = q_2 \)). We prove that no pair other than \((p, q_1)\) and \((p, q_2)\) is in \( K(C_2) \setminus K(C_1) \). Suppose \((p', q') \in K(C_2) \setminus K(C_1), p', q' \in P \). Hence, \((p', q')\) is in one of the sets \( K_1(C_2) \setminus K_1(C_1), K_2(C_2) \setminus K_2(C_1) \), and
K₃(C₂) \ K₃(C₁). If (p', q') ∈ K₁(C₂) \ K₁(C₁), then in \text{Exec}(C₁, p) process p' reads a register on which q' is visible. Since p takes the step \text{Exec}(C₁, p) and only q₁ can be the process visible on r, we have p = p' and q = q₁. If (p', q') ∈ K₂(C₂) \ K₂(C₁), then since q' takes at least one shared memory step in \text{Exec}(C₁), in \text{Exec}(C₁, p) process p' reads a register in \mathcal{R}_{q'}.

Since p takes the step \text{Exec}(C₁, p) and r ∈ \mathcal{R}_{q₂}, we have p = p' and q' = q₂. If (p', q') ∈ K₃(C₂) \ K₃(C₁), then since p' takes at least one shared memory step in \text{Exec}(C₁, p), process q' writes a register in \mathcal{R}_{q'} during \text{Exec}(C₁, p). This contradicts \text{Exec}(C₁, p) being a read step.

Now assume step \text{Exec}(C₁, p) is a write to register r ∈ \mathcal{R}_q. We prove no pair other than (q, p) is in K(C₂) \ K(C₁). Suppose (q', p') ∈ K(C₂) \ K(C₁). Hence, (q', p') is in one of the sets K₁(C₂) \ K₁(C₁), K₂(C₂) \ K₂(C₁), or K₃(C₂) \ K₃(C₁). Since \text{Exec}(C₁, p) is a write step, no process reads a register in that step and thus, (q', p') \notin K₁(C₂) \ K₁(C₁). If (q', p') ∈ K₂(C₂) \ K₂(C₁), then in \text{Exec}(C₁, p) process p' takes at least one shared memory step and q' reads a register in \mathcal{R}_{q'}. Since \text{Exec}(C₁, p) is a write step, it must be the first shared memory step by p' and p = p'. This contradicts p ∈ P. If (q', p') ∈ K₃(C₂) \ K₃(C₁), then in \text{Exec}(C₁, p) process p' writes a register in \mathcal{R}_{q'}.

Thus, p' = p, and since r ∈ \mathcal{R}_q, we have q' = q. Therefore, (q, p) is the only pair in K(C₂) \ K(C₁).

In order to prove Part (b), we map each pair in M to an RMR step in \text{Exec}(C, σ) in such a way that the mapping is injective. Consider a pair (p, q) ∈ M. Let, during \text{Exec}(C, σ), process q writes to a register r ∈ \mathcal{R}_p \cup \text{Cache}_p(C). If r ∈ \mathcal{R}_p, then we map (p, q) to q's write step to r. Recall that in \text{Exec}(C, σ) each process executes at most one step, and that step incurs an RMR. So (p, q) is mapped to a unique RMR step. Now suppose r \notin \mathcal{R}_p, so r ∈ \text{Cache}_p(C). Then there exists a step in \text{Exec}(C, σ) or in \text{Exec}(C, σ), prior to q's write, in which p caches r. Let (p, q) be mapped to the last such step. That step incurs an RMR, so it suffices to show that the mapping is injective. First note that if (p, q) is mapped to a step s, then in its unique step in \text{Exec}(C, σ) process q writes to the register that is accessed in step s. Suppose two distinct pairs, (p₁, q₁) and (p₂, q₂) are mapped to the same step s. Let r be the register accessed in s. Then in their steps in \text{Exec}(C, σ), processes q₁ and q₂ must both write to r. Since only one process writes to r during \text{Exec}(C, σ), we have q₁ = q₂. Therefore, p₁ ≠ p₂, and so r \notin \mathcal{R}_{p_j} for some j ∈ \{1, 2\}. Without loss of generality assume j = 1. Then r ∈ \text{Cache}_{p₁}(C), and step s is by p₁. If r \notin \mathcal{R}_{p₂}, then (p₂, q₂) would not be mapped to s (it would be mapped to a step by p₂). Thus, r ∈ \mathcal{R}_{p₂}, so (p₂, q₂) is mapped to q₂'s step in \text{Exec}(C, σ). This means that step s is performed by process q₂. Hence, p₂ = q₂, which contradicts the definition of M.

Then, we construct and prove the properties of an execution where we have a low-contention write case (where either most processes are poised to read, or many registers are poised to being accessed).

\textbf{Lemma 25.} Let ℓ be a positive integer, C a safe configuration, and P = \text{Proc}(σ_{₁→ C}) \setminus L(C), such that in \text{Exec}(C, σ) each process in P takes at most ℓ RMR steps and does not receive the abort signal, and in C each process in P is poised to perform an RMR step. If in C at least half of the processes in P are poised to read or at least \lceil |P|/(10ℓ) \rceil different registers are poised to being accessed by processes in P, then there exists a set of processes Q ⊆ P and a schedule σ ∈ ((Q \cup L(C))^{Δ})^*, such that

(a) \(|Q| ≥ |P|/(60ℓ^2) − 1,
(b) \text{Conf}(Γ, σ) \text{ is safe},
(c) \text{RMR}_{Q}(\text{Exec}(Γ, σ)) = \text{RMR}_{Q}(E_{→ C}) + |Q|, \text{ and}
(d) \text{no process in Q receives the abort signal in Exec}(Γ, σ).
Proof. Let $V = \{x_1, \ldots, x_m\}$ be a maximal subset of $P$ such that for each register $r$, set $V$ contains none of the processes that are poised to write to $r$ in $C$, or $V$ contains at most one process that is poised to access $r$ in configuration $C$. Let $C' = Conf \left( \Gamma, \sigma_{\rightarrow C'} \right) \left( V \cup L(C) \right)^{\Delta}$.

Hence, by Theorem 11 processes in $V$ are in the same state in $C'$ as they are in $C$, and by Claim 12 have the same cache. Therefore, all processes in $V$ are poised to perform an RMR step and access the same registers in $C'$ as in $C$. Create a directed graph $G$, where each process in $V$ forms a vertex, and where there is an edge from $p$ to $q$, $p \neq q$, if one of the following is true:

(i) in $Conf(C', x_1 \circ \ldots \circ x_m)$, process $p$ knows process $q$, (i.e. $(p, q) \in K \{Conf(C', x_1 \circ \ldots \circ x_m)\}$); or

(ii) in $Exec(C', x_1 \circ \ldots \circ x_m)$, process $q$ writes to a register $r \in R_p \cup cache_p(C')$.

Let $M$ be the set of edges in $G$ because of (ii). Since each process in $V$ is poised to perform an RMR step in $C'$, each process takes at most one step, and each register gets written at most once in $Exec(C', x_1 \circ \ldots \circ x_m)$, by Claim 21 Part (a), the number of edges in $G$ from condition (i) is at most $2RMR(Exec(C', x_1 \circ \ldots \circ x_m))$. From Claim 21 Part (b), the number of edges in $G$ from condition (ii) is $|M| \leq RMR(Exec(C', x_1 \circ \ldots \circ x_m)) + RMR(E_{\rightarrow C'})$. Let $Q'$ be a largest independent set in graph $G$, where the direction of edges are ignored.

By Theorem 11 $E_{\rightarrow C'} \left( Q' \cup L(C) \right) = Exec \left( \Gamma, \sigma_{\rightarrow C'} \left( Q' \cup L(C) \right)^{\Delta} \right)$. Further, since no two processes in $Q'$ satisfy condition (i), by Claim 10 if a process terminates in $Exec(C', x_1 \circ \ldots \circ x_m)(Q')$ it wins. Let $X$ be the set containing any process that terminates in $Exec(C', x_1 \circ \ldots \circ x_m)(Q')$. Let $Q = Q' \times X, O = Q \cup L(C')$, and $\sigma = (\sigma_{\rightarrow C'} \circ (Q')) \circ (x_1 \circ \ldots \circ x_m)(Q)$. Because at most one process wins in a leader election algorithm $|X| \leq 1$, and thus, $|Q| \geq |Q'| - 1$.

By Turán’s theorem 12, the size of the largest independent set in a graph with average degree $d$ and $k$ vertices, is at least $k/(d + 1)$. The number of edges in $G$ is at most

$$2RMR(Exec(C', x_1 \circ \ldots \circ x_m)) + RMR(Exec(C', x_1 \circ \ldots \circ x_m)) + RMR(E_{\rightarrow C'}) = 3RMR(Exec(C', x_1 \circ \ldots \circ x_m)) + RMR(E_{\rightarrow C'}) \tag{36}$$

Since each step in $Exec(C', x_1 \circ \ldots \circ x_m)$ incurs an RMR and each process takes at most $\ell$ RMR steps during $E_{\rightarrow C'}$, the number of edges in $G$ is $3m + m\ell$. Because $|V| = m$, the average degree of $G$ is at most $2(3m + m\ell)/m$. Hence, the size of $Q'$ is at least

$$\frac{m}{2(3m + m\ell)} + 1 = \frac{m}{6 + 2\ell + 1} = \frac{m}{7 + 2\ell} \tag{37}$$

The assumption is that in $C$ either at least $|P|/2$ processes are poised to read, or at least $|P|/(10\ell)$ registers are poised to being accessed. Hence, $m \geq \min \{|P|/2, |P|/(10\ell)\} \geq 2|P|/(10\ell)$ and so by (37)

$$|Q'| \geq \frac{m}{7 + 2\ell} \geq \frac{|P|}{(7 + 2\ell)10\ell} \geq \frac{|P|}{(4\ell + 2\ell)10\ell} = \frac{|P|}{60\ell^2} \tag{38}$$

Since $|Q| \geq |Q'| - 1$, Part (a) is proven.

First, we observe that $C'$ is safe by Claim 21. Hence, each process $p \in Q$, we have $E_{\rightarrow C'}(p = Exec(\Gamma, \sigma_{\rightarrow C'} \circ (Q \cup L(C'))^{\Delta})p$ (this is true by $C'$ being safe and Theorem 11). Further by Claim 22 process $p$ has the same cache in $Conf(\Gamma, \sigma_{\rightarrow C'} \circ (Q \cup L(C'))^{\Delta}$ as in $C'$. Hence, each process in $Q$ is poised to take the exact same step that incurs an RMR in $Conf(\Gamma, \sigma_{\rightarrow C'} \circ (Q \cup L(C'))^{\Delta})$. Therefore, since no two processes that satisfy (i) or (ii) are
By Theorem 11, processes in 
$$0:28 \text{RMR Lower Bound for Abortable TAS}$$

(i) no process in 
$$\mathcal{Q} \mid \mathcal{C} \subseteq \mathcal{Q} \mid \mathcal{C}$$

$$(\mathcal{C} \mathcal{E})$$

shared memory step in 
$$\mathcal{C}$$

process that receives the abort signal in 
$$\mathcal{C}$$

such that 
$$r / \mathcal{R} \mathcal{E} \mathcal{M} \mathcal{R} \mathcal{E}$$

exists a pair 
$$(p, q) / \mathcal{P} \mathcal{C} \mathcal{O}$$

there is an edge from 
$$r$$

and at least one other process writes to 
$$r$$

after that. This, completes the proof of Part (b).

Claim 26. Let 
$$C$$

be a safe configuration, such that for a fixed register 
$$r$$

each process in 
$$P_r \subseteq \mathcal{P}(\mathcal{C}) \mid \mathcal{L}(\mathcal{C})$$

is poised to perform an RMR write step to 
$$r$$

in 
$$C$$

no process incurs more than 
$$\ell$$

RMRs during 
$$\mathcal{E}_\mathcal{C} \circ \mathcal{E}$$

and any 
$$\mathcal{E}$$

process that receives the abort signal in 
$$\mathcal{E}_\mathcal{C}$$

is in 
$$\mathcal{L}(\mathcal{C})$$

There exists a set of processes 
$$Q \subseteq \mathcal{P}(\mathcal{C}) \mid \mathcal{L}(\mathcal{C})$$

and a schedule 
$$\mathcal{E}$$

such that for configuration 
$$C' = \mathcal{C} \mid \mathcal{C} \mid \mathcal{L}(\mathcal{C}) \mid \mathcal{L}(\mathcal{C})$$

(a) 
$$\mathcal{C}$$

is safe,

(b) 
$$|Q| \geq |\mathcal{P}(\mathcal{C}) \mid \mathcal{L}(\mathcal{C})| - (8\ell - 1),$$

(c) in 
$$\mathcal{E}_\mathcal{C}$$

each process in 
$$(Q \cap P_r) \mid \mathcal{L}(\mathcal{C})$$

takes exactly one RMR step,

(d) any process that receives the abort signal in 
$$\mathcal{E}_\mathcal{C}$$

in 
$$\mathcal{L}(\mathcal{C})$$

and 
$$|\mathcal{L}(\mathcal{C})| \leq 2.$$
If \(|P_r| < 8\ell - 1\), then let \(Q = \text{Proc}(\sigma \rightarrow C) \setminus P_r\), and \(\sigma\) be the empty schedule. Since \(\sigma\) is the empty schedule, \(\text{Conf}(C', \sigma) = C'\), which is a safe configuration. This proves Part (a). Because \(Q = \text{Proc}(\sigma \rightarrow C) \setminus P_r\), we have

\[
Q \setminus (\text{Conf}(C', \sigma)) = \text{Proc}(\sigma \rightarrow C) \setminus \left(\left(\text{L}(\text{Conf}(C', \sigma)) \cup P_r\right) = \text{Proc}(\sigma \rightarrow C) \setminus (\text{L}(C) \cup P_r)\right).
\]

This means

\[
|Q \setminus \text{L}(\text{Conf}(C', \sigma))| \geq |\text{Proc}(\sigma \rightarrow C) \setminus \text{L}(C)| - |P_r| \geq |\text{Proc}(\sigma \rightarrow C) \setminus \text{L}(C)| - (8\ell - 1),
\]

which proves Part (b). Since \(Q \cap P_r = \emptyset\), Part (c) is true. Further, no process receives the abort signal in \(\text{Exec}(C', \sigma)\), which proves Parts (d) and (e).

Now suppose \(|P_r| \geq 8\ell - 1\). Let \(P = \text{Proc}(\sigma \rightarrow C) \setminus \text{L}(C)\). For each process \(p \in P_r\), let \(Z_p \subseteq P \setminus \{p\}\) be the set of all processes \(q\), such that process \(p\) reads a register \(r'\) in its solo-run starting in \(C\), where either \(r' \in R_q\) or in \(C\) process \(q\) is visible on \(r'\). Note that because \(C\) is safe and \(p \in P_r\), for any process \(q\) visible on a register in \(R_q\), we have \((p, q) \in K_3(C)\). Hence, none of the processes in \(Z_p\) are visible on any register in \(R_p\). Since \(C\) is safe and \(Z_p \cap \text{L}(C) = \emptyset\), for any process \(q \in Z_p\), we have \((p, q) \notin K(C)\). Hence, \(p\) does not have a cache copy of any register that \(q\) is visible on (otherwise, \((p, q) \in K_1(C)\) or any register in \(R_q\) (otherwise, \((p, q) \in K_2(C)\)). Thus, in a solo-run by \(p\) starting in \(C\) the first read from a register on which \(q\) is visible or a register in \(R_q\) incurs an RMR. Hence, since each process incurs at most \(\ell\) RMRs during any execution, \(|Z_p| \leq 2\ell\), for any \(p \in P_r\). We want to choose two processes \(a\) and \(b\) from \(P_r\), such that \(a \notin Z_b\) and \(b \notin Z_a\). We have \(\binom{|P_r|}{2}\) many possibilities to choose 2 processes. However, for each process \(p\) at most \(|Z_p|\) many choices need to be removed. Therefore, by

\[
\binom{|P_r|}{2} - \sum_{p \in P_r} \left| \left|Z_p\right| + \left|Z_p\right| \geq 8\ell - 1, \right|\leq 2\ell
\]

we have at least one pair of processes \(a\) and \(b\), such that \(b \notin Z_a\) and \(a \notin Z_b\). Fix a pair of processes \(a\) and \(b\), such that \(b \notin Z_a\) and \(a \notin Z_b\). Let \(D = \text{Conf}(\Gamma, \sigma \rightarrow C)|\text{L}(C) \cup \{a, b\}\rangle\). By Claim 14, configuration \(D\) is safe. Hence, because for any pair \((p, q) \in K(\text{Conf}(D, a^k))\), for any \(p \in \{a, b\}\) and any positive integer \(k\), we have \(q \in \text{L}(D)\), by Claim 13 in a solo-run by \(p\) starting in \(D\), in which \(p\) does not receive the abort signal \(p\) wins. Hence, a solo run by \(p \in \{a, b\}\), in which \(p\) does not receive the abort signal, starting in \(\text{Conf}(D, a)\) also results in \(p\) winning. That is because when \(p = a\), we have \(\text{Exec}(D, a^k) = \text{Exec}(\text{Conf}(D, a), a^{k-1})\), for any positive integer \(k\), and when \(p = b\), in \(\text{Exec}(\text{Conf}(D, a), b^k)\), for any positive integer \(k\), the value written by process \(a\) is overwritten by \(b\) and thus, \(D\) and \(\text{Conf}(D, a)\) are indistinguishable to process \(b\). Since \(a\) and \(b\) have not received the abort signal in \(\text{Conf}(D, a)\) and in any fair execution starting in \(\text{Conf}(D, a)\) both \(a\) and \(b\) terminate (because the algorithm that we are running is deadlock-free), by Lemma 19, there exists a schedule \(\lambda \in (\{a, b\}^\omega)^*\), such that in \(\text{Exec}(\text{Conf}(D, a), \lambda)\) both \(a\) and \(b\) lose.

\[
\text{(43)}
\]

Let \(R\) be the set of registers that are being read during \(\text{Exec}(\text{Conf}(D, a), \lambda)\) by any process in \(\{a, b\}\). Further, let \(Y \subseteq P \setminus \{a, b\}\) be a set of all processes \(q\), such that \(q\) is visible on at
least one register in $R$ in configuration $C$ or $R \cap R_q \neq \emptyset$. Since $C$ is safe, for any process $y \in Y$, we have $(a, y) \notin K(C)$ and $(b, y) \notin K(C)$. Thus, $(\text{Cache}_a(C) \cup \text{Cache}_b(C)) \cap R = \emptyset$. Hence, in any $(a, b)$-only execution starting in $C$, for each register $r \in R$ on which a process $q \in Y$ is visible or $r \in R_q$, the first read by each process in $(a, b)$ from $r$ incurs an RMR. Thus, because $a$ and $b$ incur at most $\ell$ RMRs in $\text{Exec}(\text{Conf}(C, a), \lambda)$, it is true that $|Y| \leq 4\ell$.

Let $w$ be the process, such that $r \in R_w$. Note that since all processes in $P_r$ are poised to perform an RMR step on $r$, we have $w \notin P_r$. Further let $X = Z_a \cup Z_b \cup Y \cup \{w\}$, and $D' = \text{Conf}(\Gamma, \sigma \rightarrow C|\{(L(C))|\{(P \setminus X)\}^\Delta\})$. Since $C$ is safe, by Theorem 11 processes in $P_r \setminus X$ are in the same state in $D'$ as they are in $C$, which means they are poised to write to $r$. Let $\{q_1, ..., q_k\} = P_r \setminus (X \cup \{a, b\})$, $Q = (P \cup \{a, b\}) \setminus X$, and $\sigma = q_1 \circ \circ q_k \circ a \circ \lambda$. Configurations $\text{Conf}(D, a), \text{Conf}(C', a)$, and $\text{Conf}(C', q_1 \circ \circ q_k \circ a)$ are indistinguishable to processes $a$ and $b$. Hence, by (44),

$$a, b \in L(\text{Conf}(C', \sigma)).$$

We now show that (S1) and (S2) are satisfied for $\text{Conf}(C', \sigma)$. For (S1) we need to show for any pair $(p, q) \in K(\text{Conf}(C', \sigma))$, that $q \in L(\text{Conf}(C', \sigma))$. Fix a pair $(p, q) \in K(\text{Conf}(C', \sigma))$. If $(p, q) \in K(\text{Conf}(C', \sigma))$, then since $C'$ is safe, $q \in L(C')$. Because $L(C') \subseteq L(\text{Conf}(C', \sigma))$, we have $q \in L(\text{Conf}(C', \sigma))$. If $(p, q) \notin K(\text{Conf}(C', \sigma))$, then since any visible process on a register read by $a$ or $b$ in Exec$(C', \sigma)$ is lost (otherwise, it is a process in $Y$, which does not make any steps in $E_{\rightarrow C'} \circ \text{Exec}(C', \sigma)$), we have $(p, q) \notin K_1(\text{Conf}(C', \sigma)) \setminus K_1(C')$. Further, because $P \subseteq \text{Proc}(\sigma)$, no process takes its first shared memory step in Exec$(C', \sigma)$. Hence, $(p, q) \notin K_2(\text{Conf}(C', \sigma)) \setminus K_2(C')$. Thus, $(p, q) \in K_3(\text{Conf}(C', \sigma)) \setminus K_3(C')$. Therefore, since $Q \subseteq \text{Proc}(\sigma)$, during Exec$(C', \sigma)$ process $q$ writes to a register in $R_q$. Because of (44), if $q \in \{a, b\}$, then $q \in L(\text{Conf}(C', \sigma))$. Since each process in $P_r$ is poised to perform an RMR step in $C'$ and both $a$ and $b$ are poised to write to $r$ in $C'$, we have $r \notin R_a \cup R_b$. Thus, $p \notin \{a, b\}$. Since for the process $w$ that $r \in R_w$, it holds $w \notin Q$, we have $p \notin Q$. Hence, (S1) is satisfied. Since $C'$ is safe, for any $p \notin H(C')$, either $p$ does not take any shared memory steps in $E_{\rightarrow C'}$, or $p \in L(C')$. Thus, because any register that is accessed in Exec$(C', \sigma)$ is last accessed by either $a$ or $b$, and by (44), (S2) is also satisfied. This proves Part (a).

From $Q = (P \cup \{a, b\}) \setminus X$ we get

$$|Q| \geq |\text{Proc}(\sigma \rightarrow C) \setminus L(C)| + 2 - |X|.$$  \hspace{1cm} (45)

Thus, to prove Part (b) is suffices to prove $|X| \leq 8\ell + 1$. As $X = Z_a \cup Z_b \cup Y \cup \{w\}$, where $w$ is the process that $r \in R_w$, it holds $|X| \leq |Z_a| + |Z_b| + |Y| + 1 \leq 8\ell + 1$.

In Exec$(C', \sigma)$, each process in $\{q_1, ..., q_k\}$ takes a single write step to $r$. Since $(P_r \cap Q) \setminus L(\text{Conf}(C', \sigma)) = \{q_1, ..., q_k\}$, Part (c) is true.

Processes $a$ and $b$ are the only processes that receive the abort signal in Exec$(C', \sigma)$, and they both lose. Thus, Parts (d) and (e) are true.

We use the execution constructed in Claim 20 to create an execution to handle the high-contention write case (where most processes are poised to write and few registers are poised to being accessed).

**Lemma 27.** Let $C$ be a safe configuration and $P = \text{Proc}(\sigma \rightarrow C) \setminus L(C)$, such that in $E_{\rightarrow C}$ each process in $P$ does not receive the abort signal, and is poised to perform an RMR step. Also no process takes more than $\ell$ RMR steps in any execution. If in $C$ more than $|P|/2$ processes are poised to write and at most $|P|/(10\ell)$ registers are poised to being accessed, then there exists a set of processes $Q \subseteq P$ and schedule $\sigma \in \left((Q \cup L(C))^\Delta\right)^\ast$, such that
Let $W$ e now describe our inductive construction in detail.

This proves Part (b). From Part (c) of Claim 26, Part (c) follows. Since any process that

achieved by applying Claim 26 to configuration $P_{0}$, for each $i \in \{1, ..., k\}$. Our inductive hypothesis is that for $i \in \{1, ..., k\}$,

\[ \text{(IH1) configuration } C_{i} = Conf(\Gamma, \sigma_{i}) \text{ is safe}, \]

\[ \text{(IH2) } |P_{i}| \geq |P| - i(8\ell - 1), \]

\[ \text{(IH3) any process that receives the abort signal in } E \to C_{i} \text{ is in } L(C_{i}). \]

Since $C$ is safe, by Claim 21 configuration $C_{0}$ is safe. By Claim 10 it holds $E \to C | P = E \to C_{0} | P$. Therefore, any process that receives the abort signal in $E \to C_{0}$ is in $L(C_{0})$. Thus, by (IH3) it holds that any process in $Proc(C_{i}) \setminus L(C_{i})$, for $i \in \{0, ..., k\}$, does not receive the abort signal in $E \to C_{i}$. Hence, by (IH1) and the fact that no process takes more than $\ell$ RMR steps in any execution starting in $\Gamma$, we can apply Claim 26 to configuration $C_{i-1}$, where $r_{i}$ is the fixed register. For $i \in \{1, ..., k\}$, let $\sigma'$ and $P_{i}$ be the schedule and set of processes achieved by applying Claim 26 to configuration $C_{i-1}$ and the fixed register $r_{i}$. Then let

\[ \sigma_{i} = \left( \sigma_{\to C_{i-1}}(P_{i} \cup L(C_{i-1})) \right) \circ \sigma'. \]

By Claim 26 Part (a), (b), and (d), the inductive hypothesis is true.

Let $\sigma = \sigma_{k+1}$, and $Q = P_{k} \setminus L(C)$. (IH1) implies Part (a). Since at most $|P|/10\ell$ registers are poised to be accessed in $C$, we have $k \leq |P|/(10\ell)$. Further, by Claim 26 Part (c), for each $i \in \{1, ..., k\}$ at most 2 processes are in $L(C') \setminus L(C)$. Hence, by the inductive hypothesis,

\[ |Q \setminus L(C')| \geq |P| - k(8\ell - 1) - 2k \geq |P| - 9k\ell \geq |P| - |P|/10\ell \geq |P|/10 \geq |P|/9. \]

This proves Part (b). From Part (c) of Claim 26 Part (c) follows. Since any process that receives the abort signal in $E \to C$ is in $L(C)$, and by Part (d) of Claim 26 Part (d) follows.

\[ \text{3.4.3 Detailed Construction} \]

Let $n \geq 4, c = 10$, and $\ell = \lfloor \log n/(c \log n) \rfloor$. We inductively construct a schedule $\sigma_{i}$ and a set of processes $P_{i} \subseteq \mathcal{P}$, for all $i \in \{0, ..., \ell\}$. For the sake of conciseness, let $E_{i} = Exec(\Gamma, \sigma_{i})$, $C_{i} = Conf(\Gamma, \sigma_{i})$, and $L_{i} = L(C_{i})$.

The following invariants are satisfied for $i \in \{0, ..., \ell\}$:

\[ \text{(I1)} \ C_{i} \text{ is safe.} \]

\[ \text{(I2)} \ |P_{i} \setminus L_{i}| \geq (n - 1)/(\log n)^{c_{3}}. \]

\[ \text{(I3)} \ \text{RMR}_{P_{i} \setminus L_{i}}(E_{i}) \geq i |P_{i} \setminus L_{i}| - i. \]

\[ \text{(I4)} \ \text{For each process } p \in P_{i} \setminus L_{i} : \text{RMR}_{p}(E_{i}) \leq i. \]

\[ \text{(I5)} \ \text{For each process } p \in P_{i} \setminus L_{i}, p^{-} \text{ does not appear in } \sigma_{i}. \]

We now describe our inductive construction in detail.

**Base Case:**

Schedule $\sigma_{0}$ is a schedule in which each process scans its own shared memory segment, and $P_{0} = \mathcal{P}$. Note that $Proc(\sigma_{0}) = \mathcal{P}$. 
In $C_i$, we let each process in $P_i \setminus L_i$ that does not win in a solo-run take solo-steps until it is poised to perform an RMR. By Claim 15, there is at most one process that wins in a solo-run starting in $C_i$, so in our execution all but one process participate. By Claim 10, each process performs the same steps in the solo-run starting in $C_i$ as in the constructed execution, and by Claim 16, each process will eventually become poised to perform an RMR. If there is a process that wins in a solo-run starting from $C_i$, then we remove that process from the entire execution constructed so far.

More precisely, let $\{q_1, ..., q_k\} = P_i \setminus L_i$ and let $t_j$ be the largest integer, such that $RMR(\text{Exec}(C_i, q_j^{t_j})) = 0$ and $q_j$ does not terminate in Exec($C_i, q_j^{t_j}$), for $j \in \{1, ..., k\}$ (since by (II), $C_i$ is safe, and by (III) $q_j$ does not receive the abort signal in $E_{\rightarrow C_i}$, such an integer $t_j$ exists according to Claim 13). By (III), no process in $P_i \setminus L_i$ receives the abort signal in $E_{\rightarrow C_i}$. Thus, by Claim 19, any process that starting in $C_i$ terminates in its solo-run wins. Hence, by the safety property of leader election, at most one process terminates in its solo-run starting in $C_i$. If such a process does not exist, then let $\lambda_i = q_1 q_2 \ldots q_{k-1}$, and $P'_i = P_i \setminus \{q_k\}$. If such a process exists, we assume, without loss of generality (by renaming variables $q_1, ..., q_k$), that $q_k$ is the process that wins in its solo-run starting in $C_i$ without incurring any RMRs. Then let $\lambda_i = q_1 q_2 \ldots q_{k-1}$, $P'_i = P_i \setminus \{q_k\}$. Finally, let $D_i = \text{Conf}(\text{Conf}(\Gamma, \sigma_i | P'_i), \lambda_i)$.

We define for register $r$, set $R_i(r)$ as the set of processes that are poised to read $r$ in $D_i$, and set $W_i(r)$ as the set of processes that are poised to write $r$ in $D_i$. Let $S_i = \{r \in R | W_i(r) \cup R_i(r) \neq \emptyset\}$.

First, we prove some properties of configuration $D_i$.

Claim 28. The following are true for configuration $D_i$.

(a) Configuration $D_i$ is safe.
(b) For any process $p \in P'_i \setminus L_i$, $RMR_p(E_{\rightarrow C_i}) = RMR_p(E_{\rightarrow D_i}).$
(c) For any process $p$ in $R_i(r) \cup W_i(r)$, it is true that $r \not\in R_p$.

Proof. Let $k' = |P'_i \setminus L_i|$. Since $C_i$ is safe, by Claim 13,

$$\text{Exec}(\Gamma, \sigma_i | P'_i) = E_{\rightarrow C_i} | P'_i.$$  \hfill (47)

Further, by Claim 14 for each process $p \in P'_i$, it holds that $\text{Cache}_p(C_i) = \text{Cache}_p(\text{Conf}(\Gamma, \sigma_i | P'_i))$.

Therefore, when $RMR(\text{Exec}(C_i, q_j^{t_j})) = 0$, for $j \in \{1, ..., k'\}$, it is true that $RMR(\text{Exec}(\text{Conf}(\Gamma, \sigma_i | P'_i), q_j^{t_j})) = 0$. Thus, by applying Claim 15 Part (b) several times (first $Q_1 = \{q_1\}$ and $Q_2 = \{q_2\}$), the next time, $Q_1 = \{q_1, q_2\}$ and $Q_2 = \{q_3\}$, and so on),

$$RMR(\text{Exec}(\text{Conf}(\Gamma, \sigma_i | P'_i), \lambda_i)) = 0.$$  \hfill (48)

Hence, since by (III) none of the processes in $P'_i \setminus L_i$ receive the abort signal in $\text{Conf}(\Gamma, \sigma_i | P'_i)$ or during $\text{Exec}(\text{Conf}(\Gamma, \sigma_i | P'_i), q_j^{t_j})$, by applying Claim 14 multiple times, $D_i$ is safe. This proves Part (a).

By (IV), for each process $p \in P'_i$, it holds that $RMR_p(E_{\rightarrow C_i}) = RMR_p(\text{Exec}(\Gamma, \sigma_i | P'_i))$.

Thus, Part (b) follows from (15).

By Claim 13, each process in $P'_i \setminus L_i$ has the same cache in $C_i$ and $\text{Conf}(\Gamma, \sigma_i | P'_i)$. Hence, by (IV) and the construction of $\lambda_i$, each process in $R_i(r) \cup W_i(r)$ is poised to perform an RMR step in $D_i$. Therefore, the register that each process $p \in R_i(r) \cup W_i(r)$ is poised to access is not in its own memory segment.

Let $X_i = \bigcup_{r \in S_i} W_i(r)$, and $Y_i = \bigcup_{r \in S_i} R_i(r)$. We distinguish the following cases to complete the inductive step of our construction:

Inductive Step:
**Case 1:** $|S_i| \geq |P_i \setminus L_i|/(10\ell)$ or $|X_i| < |Y_i|$: 

Let $\sigma_{i+1} = \sigma$ and $P_{i+1} = Q \cup L(D_i)$, where $Q$ and $\sigma$ are the set of processes and the schedule we know from Lemma 25. From Part (b), we get that $C_{i+1}$ is safe. By Part (a),

$$|P_{i+1} \setminus L_{i+1}| \geq \frac{|P_i|}{60\ell^2} \geq \frac{n-1}{(\log n)^c 60\ell^2} \geq \frac{n-1}{60(\log n)^c 10^{(\ell^2)}} \geq \frac{n-1}{(\log n)^{c(\ell+1)}}.$$ 

Hence, (I2) is true. From (I3), (I4), and Part (c), it immediately follows that (I3) and (I4) are true for $i+1$. Invariant (I5) directly follows Part (d).

**Case 2:** $|S_i| < |P_i \setminus L_i|/(10\ell)$ and $|X_i| \geq |Y_i|$: 

Applying Lemma 27 to configuration $D_i$, results in a set of processes $Q$, and a schedule $\sigma$. Let $P_{i+1} = Q \cup L(D_i)$ and $\sigma_{i+1} = \sigma$. From Lemma 27, we prove Invariants (I1)-(I5). Invariant (I1) follows Part (a). From Part (b), we have

$$|P_{i+1} \setminus L_{i+1}| \geq \frac{|P_i \setminus L_i|}{10} \geq \frac{n-1}{10(\log n)^c} \geq \frac{n-1}{(\log n)^{c(\ell+1)}}.$$ 

which proves (I2). From (I3), (I4), and Part (c), Invariants (I3) and (I4) are true. Part (d) and (I5) immediately imply (I5).

**Proof of Theorem 3**

Using Invariants (I1)-(I5), we obtain our main theorem. As shown above, for any abortable leader election algorithm, there exists an execution $Exec(\Gamma, \sigma_{\ell-1})$ that satisfies (I1)-(I5). We have

$$\frac{n-1}{(\log n)^{(\ell-1)}} \geq \frac{n-1}{(\log n)(\log n/\log \log n)^c} \geq \frac{(n-1)(\log n)^c}{\log n} \geq 2.$$ 

Hence, by (I2) in $Exec(\Gamma, \sigma_{\ell-1})$ at least two processes participate and don’t lose. By (I3) at least one of these processes incurs $\Omega(\ell) = \Omega(\log n/\log \log n)$ RMRs.
References

1. Zahra Aghazadeh, Wojciech Golab, and Philipp Woelfel. Making objects writable. Under review, 2014.

2. Zahra Aghazadeh and Philipp Woelfel. Space- and time-efficient long-lived test-and-set objects. In Proceedings of 18th International Conference On Principles Of Distributed Systems (OPODIS), pages 404–419, 2014. URL: https://doi.org/10.1007/978-3-319-14472-6_27

3. Zahra Aghazadeh and Philipp Woelfel. Upper bounds for boundless tagging with bounded objects. In Proceedings of the 30th International Symposium on Distributed Computing (DISC), pages 442–457, 2016. URL: https://doi.org/10.1007/978-3-662-53426-7_32

4. Marcos Kawazoe Aguilera, Svend Frølund, Vassos Hadzilacos, Stephanie Lorraine Horn, and Sam Toueg. Abortable and query-abortable objects and their efficient implementation. In Proceedings of the 26th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 23–32, 2007.

5. Dan Alistarh and James Aspnes. Sub-logarithmic test-and-set against a weak adversary. In Proceedings of the 25th International Symposium on Distributed Computing (DISC), pages 97–109, 2011.

6. Dan Alistarh, James Aspnes, Keren Censor-Hillel, Seth Gilbert, and Morteza Zadimoghaddam. Optimal-time adaptive strong renaming, with applications to counting. In Proceedings of the 30th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 239–248, 2011.

7. Dan Alistarh, James Aspnes, Seth Gilbert, and Rachid Guerraoui. The complexity of renaming. In Proceedings of the 52nd Annual IEEE Symposium on Foundations of Computer Science (FOCS), pages 718–727, 2011.

8. Dan Alistarh, Hagit Attiya, Seth Gilbert, Andrei Giurgiu, and Rachid Guerraoui. Fast randomized test-and-set and renaming. In Proceedings of the 24th International Symposium on Distributed Computing (DISC), pages 94–108, 2010.

9. James H. Anderson and Yong-Jik Kim. Adaptive mutual exclusion with local spinning. In Proceedings of the 14th International Symposium on Distributed Computing (DISC), pages 29–43, 2000.

10. James H. Anderson and Yong-Jik Kim. An improved lower bound for the time complexity of mutual exclusion. Distributed Computing, 15:221–253, 2002.

11. T. Anderson. The performance of spin lock alternatives for shared-memory multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 1:6–16, 1990.

12. Hagit Attiya, Danny Hendler, and Philipp Woelfel. Tight RMR lower bounds for mutual exclusion and other problems. In Proceedings of the 40th Annual ACM Symposium on Theory of Computing (STOC), pages 217–226, 2008.

13. Michael Bender and Seth Gilbert. Mutual exclusion with $O(\log^2 \log n)$ amortized work. In Proceedings of the 52nd Annual IEEE Symposium on Foundations of Computer Science (FOCS), pages 728–737, 2011.

14. Harry Buhrman, Alessandro Panconesi, Riccardo Silvestri, and Paul M. B. Vitányi. On the importance of having an identity or, is consensus really universal? Distributed Computing, 18(3):167–176, 2006.

15. Robert Danek and Wojciech M. Golab. Closing the complexity gap between FCFS mutual exclusion and mutual exclusion. Distributed Computing, 23(2):87–111, 2010.

16. Robert Danek and Hyonho Lee. Brief announcement: Local-spin algorithms for abortable mutual exclusion and related problems. In Proceedings of the 22nd International Symposium on Distributed Computing (DISC), pages 512–513, 2008.
17 E. W. Dijkstra. Solution of a problem in concurrent programming control. Communications of the ACM, 8:569, 1965.
18 Cynthia Dwork, Maurice Herlihy, and Orli Waarts. Contention in shared memory algorithms. Journal of the ACM, 44(6):779–805, 1997. doi:10.1145/268999.269000
19 Wayne Eberly, Lisa Higham, and Jolanta Warpechowska-Gruca. Long-lived, fast, wait-free renaming with optimal name space and high throughput. In Proceedings of the 12th International Symposium on Distributed Computing (DISC), pages 149–160, 1998.
20 Michael J. Fischer, Nancy A. Lynch, and Mike Paterson. Impossibility of distributed consensus with one faulty process. Journal of the ACM, 32(2):374–382, 1985.
21 George Giakkoupis and Philipp Woelfel. On the time and space complexity of randomized test-and-set. In Proceedings of the 31st SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 19–28, 2012.
22 George Giakkoupis and Philipp Woelfel. A tight RMR lower bound for randomized mutual exclusion. In Proceedings of the 44th Annual ACM Symposium on Theory of Computing (STOC), pages 983–1002, 2012.
23 George Giakkoupis and Philipp Woelfel. Randomized mutual exclusion with constant amortized RMR complexity on the DSM. In Proceedings of the 55nd Annual IEEE Symposium on Foundations of Computer Science (FOCS), 2014. To appear.
24 George Giakkoupis and Philipp Woelfel. Randomized abortable mutual exclusion with constant amortized RMR complexity on the CC model. In Proceedings of the 36th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 221–229, 2017. URL: http://doi.acm.org/10.1145/3087801.3087837
25 Wojciech Golab, Danny Hendler, and Philipp Woelfel. An O(1) RMRs leader election algorithm. SIAM Journal on Computing, 39(7):2726–2760, 2010.
26 Wojciech M. Golab, Vassos Hadzilacos, Danny Hendler, and Philipp Woelfel. Constant-RMR implementations of cas and other synchronization primitives using read and write operations. In Proceedings of the 26th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 3–12, 2007.
27 Wojciech M. Golab, Vassos Hadzilacos, Danny Hendler, and Philipp Woelfel. RMR-efficient implementations of comparison primitives using read and write operations. Distributed Computing, 25(2):109–162, 2012.
28 Danny Hendler and Philipp Woelfel. Randomized mutual exclusion in O(log N/ log log N) RMRs. In Proceedings of the 28th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 26–35, 2009.
29 Danny Hendler and Philipp Woelfel. Adaptive randomized mutual exclusion in sublogarithmic expected time. In Proceedings of the 29th SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 141–150, 2010.
30 Danny Hendler and Philipp Woelfel. Randomized mutual exclusion with sublogarithmic RMR-complexity. Distributed Computing, 24(1):3–19, 2011. URL: http://dx.doi.org/10.1007/s00446-011-0128-6
31 Prasad Jayanti. Adaptive and efficient abortable mutual exclusion. In Proceedings of the 22nd SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC), pages 295–304, 2003. doi:http://doi.acm.org/10.1145/872035.872079
32 Prasad Jayanti, Srdjan Petrovic, and Neha Narula. Read/write based fast-path transformation for FCFS mutual exclusion. In 31st Conference on Current Trends in Theory and Practice of Informatics (SOFSEM), pages 209–218, 2005.
33 Y.-J. Kim and J. Anderson. A time complexity bound for adaptive mutual exclusion. In Proceedings of the 15th International Symposium on Distributed Computing (DISC), pages 1–15, 2001.
Yong-Jik Kim and James H. Anderson. Nonatomic mutual exclusion with local spinning. *Distributed Computing*, 19(1):19–61, 2006.

Clyde P. Kruskal, Larry Rudolph, and Marc Snir. Efficient synchronization on multiprocessors with shared memory. *ACM Transactions on Programming Languages and Systems*, 10(4):579–601, 1988.

Hyonho Lee. Transformations of mutual exclusion algorithms from the cache-coherent model to the distributed shared memory model. In *Proceedings of the 25th International Conference on Distributed Computing Systems (ICDCS)*, pages 261–270, 2005.

Hyonho Lee. Fast local-spin abortable mutual exclusion with bounded space. In *Proceedings of 14th International Conference On Principles Of Distributed Systems (OPODIS)*, pages 364–379, 2010. URL: [https://doi.org/10.1007/978-3-642-17653-1_27](https://doi.org/10.1007/978-3-642-17653-1_27).

Hyonho Lee. *Local-spin Abortable Mutual Exclusion*. PhD thesis, 2011.

Alessandro Panconesi, Marina Papatriantafilou, Philippas Tsigas, and Paul M. B. Vitányi. Randomized naming using wait-free shared variables. *Distributed Computing*, 11(3):113–124, 1998.

Abhijeet Pareek and Philipp Woelfel. RMR-efficient randomized abortable mutual exclusion. In *Proceedings of the 26th International Symposium on Distributed Computing (DISC)*, pages 267–281, 2012.

Michael L. Scott. Non-blocking timeout in scalable queue-based spin locks. In *Proceedings of the twenty-first annual symposium on Principles of distributed computing*, pages 31–40. ACM, 2002.

Paul Turán. Eine extremalaufgabe aus der graphentheorie. *Mat. Fiz. Lapok*, 48(436-452):61, 1941.