A nanomechanical computer—exploring new avenues of computing

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Abstract. We propose a fully mechanical computer based on nano-
electromechanical elements. Our aim is to combine this classical approach with
modern nanotechnology to build a nanomechanical computer (NMC) based on
nanomechanical transistors. The main motivation behind constructing such a
computer is threefold: (i) mechanical elements are more robust to electromagnetic
shocks than current dynamic random access memory (DRAM) based purely on
complimentary metal oxide semiconductor (CMOS) technology, (ii) the power
dissipated can be orders of magnitude below CMOS and (iii) the operating
temperature of such an NMC can be an order of magnitude above that of
conventional CMOS.

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1. Introduction

Power dissipation in highly integrated circuits turns out to be a major concern for the semiconductor industry as well as for energy producers. The US wide power consumption by computers reaches about 20% of the total energy provided and is rising [1]. On a more fundamental level the question is what the actual limit for energy dissipation is without compromising data integrity. An early estimate was performed by Landauer [2], whose extrapolation sets the energy consumed by a single gate operation to reach the fundamental energy of $k_B T$ of around $10^{-21}$ Joule by 2015, where $k_B$ is the Boltzmann constant and the temperature is assumed to be 300 K. The main point in Landauer’s paper was that if this temperature limit is reached, one would have to consider Carnot-efficient computing, i.e. ‘reversible computing becomes significant’ [2]. In other words new approaches to computing will have to be found, which reduce the overall power dissipated and which finally might allow reversible computing. Here, we offer a possible solution for reducing dynamic power dissipation in the first place by using nanomechanical devices for building computational elements. This approach might also have potential for reversible computing, if one makes use of the thermal energy of the environment.

It has to be clearly stated that current operating speeds of nano-electromechanical single electron transistors (NEMSETs) are of the order of 1 GHz [3], which is not competitive with standard complimentary metal oxide semiconductors (CMOS). However, this is sufficient for many families of micro-processors, which are used for a broad range of mundane tasks. A nanomechanical computer (NMC) will not address the issue of clock-speed (which actually enhances dissipation), but will be most effective for micro-processor applications which demand robustness, low power consumption and high-temperature applications ($T > 200^\circ$C). Finally, it needs to be added that an NMC can be realized in silicon substrates and naturally allows for combining with traditional CMOS circuitry. Hence, we are able to offer a new principle for computational tasks, which is compatible with existing technology.

Based on ultra-hard materials such as diamond, which can be doped and processed straightforwardly, such an NMC can withstand extreme temperatures. The operating temperature can be as high as 500$^\circ$C. This is of great interest for space-born operation and other harsh environments or when the available power is limited. We estimate that operation with externally applied dc voltages is feasible. These voltages can be generated either by a battery or by a manually actuated battery charger. Another possible energy supply for the NMC can be found in mechanically actuating the supporting substrate either by an acoustic transducer (quartz) or by relying on the thermal lattice vibrations. The NMC thus might constitute the first step towards a Carnot-efficient computing device.

As we have found in recent measurements [4] self-excitation can be exploited to generate mechanical oscillations without any ac excitation. Hence, dc voltages are sufficient to operate the NMC. Basically, a dc voltage creates an electric field to support mechanical oscillations of the nanopillars. A classical example is straightforward to construct [5]. It has to be noted that onset of the mechanical oscillations is induced by a thermal fluctuation, which is found to be enhanced, if the electrical field is inhomogeneous.

2. Logic elements

In order to construct an NMC we need to have the following logic element implemented: the NEMSET. To the earlier work we have to add that we recently were able to demonstrate...
Figure 1. Typical NEMSET: using FE the current can be increased by an order of magnitude. The bias-tee on the left hand side allows application of an ac signal and dc voltage bias. The recorded current depends on the nanomechanical pillar in the centre. The gate electrodes are grounded in this particular experiment.

field emission (FE) in these devices [6]. This enhances the current level by an order of magnitude—see figure 1 for an example of a NEMSET of the current generation. Standard NEMSET configurations are realized in silicon-on-insulator (SOI) substrate with gold contacts added by thermal evaporation. The circuit in figure 1 was defined by using electron-beam lithography, however, standard industry optical lithography now realizes feature sizes of 90 nm by UV-light. Hence, an integrated nanomechanical circuit can be fabricated via inexpensive optical lithography. Other methods, such as nanoimprint lithography with proven feature sizes of only 20 nm, can be applied for large-scale integration. The latter point should especially be important, considering that for the most simple NMC only a single metallic top layer will be required, i.e. all transistor functions should be defined in one litho-step and then transferred into the supporting material (SOI, SSOI, SGOI, GOI, GaAs, AlGaAs and diamond) via dry-etching techniques.

In figure 2, a typical measurement of current versus applied radio frequency on a single NEMSET is shown for a variety of bias voltages. We find two mechanical resonances around 150 and 240 MHz. The inset shows the $IV$-characteristics for ON- and OFF-mechanical resonance cases. Due to the simultaneously applied ac voltage the threshold for current flow is very low. This is an indication that dc or ac voltages below 1 V will be sufficient for operating the NMC [4] and hence the overall power required can be further reduced. It should be noted that pure dc excitation is preferable for operating an NMC with a large number of logic gates.

Key to any computing machine are logic elements. These require gain to provide a noise margin. It seems that gain might be achieved in a NEMSET by mechanically coupling two sets of pillars. One set, the input set, puts the output set in motion. Gain is achieved if the input set consumes less charge than the output set delivers to the load. This is implemented when the input set contains fewer pillars or if each pillar transfers less charge than a pillar in the output set. The two sets have independent source and drain connections. This provides isolation between input and output and allows for logic restoration.

We constructed a simple model to explore how such a gate can work. If we assume that charge transfer in the NEMSET takes place only during the brief time that the pillar is closest to the
source or drain, we can model the NEMSET as a switched-capacitor network with low duty cycle. There are two extremes to the modes of operation for such a network: the pillar might charge or discharge fully in each contact cycle, or the pillar might charge or discharge only infinitesimally. Assuming the latter situation, the average current flow is given by

\[ i_{\text{AVE}} = \frac{V_{\text{DD}}}{2R_p} \frac{\Delta t}{T} \]

where \( R_p \) is the pillar contact resistance, \( V_{\text{DD}} \) is the voltage of the power-supply, and \( \Delta t / T \) is the duty cycle: source/pillar or drain/pillar contact time divided by the period of oscillation. The NEMSET can then be modelled as an effective resistance, \( R_{\text{Pe}} = 2R_p \frac{T}{\Delta t} \) in parallel with the source-drain capacitance. Since \( R_{\text{Pe}} \) is only present once oscillation begins, a self-starting oscillator will look purely capacitive until oscillation begins and then \( R_{\text{Pe}} \) will appear in parallel. The switched capacitor model and its effective equivalent for low duty cycle are shown in figure 3.

Both the figure 3 models can be used to model more complex NEMSET circuits. We model mechanical self-excitation using a comparator connected across the source and drain. When the voltage reaches the threshold of oscillation, the switches of figure 3 (left) begin to toggle. The figure 3 (right) switch simply switches on when the oscillation threshold is reached. Since the full model requires extremely short contact times, \( \Delta t \), simulation can be time consuming. The low-duty-cycle equivalent provides for extremely fast simulation.

To model a device with gain, two mechanically coupled NEMSETs are required. In the simplest approximation, the mechanical coupling can be represented through the switch actuation. When the drain–source (D–S) voltage gets large enough to initiate switching in the input set, the output set is made to switch as well. In reality, the amplitude of the oscillation produced by the input set of pillars will critically affect the contact resistance of the pillars in the

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Figure 3. Switched-capacitor model for the NEMSET (left) and low-duty-cycle equivalent (right). In the left figure, the switches actuate alternately for time, $\Delta t$, and period, $T$, to represent pillar FM near the source and drain contacts. The switch in the right figure is on continuously to represent charge lost when the pillar is oscillating.

Figure 4. Coupled NEMSET model using a comparator to switch in the effective resistance when applied voltage is sufficient for oscillation (top), and the schematic symbol for the coupled NEMSET (bottom).

output set. The simple model only accounts for a fixed contact resistance. The coupled-NEMSET device model using the simplified low-duty-cycle equivalent is shown below in figure 4.

A basic inverter using the coupled NEMSET is shown in figure 5. The bottom device will be on for $V_{in} > V_l$ where $V_l$ is the threshold for mechanical self-excitation. The top device will be on for $V_{in} < (V_{DD} - V_l)$, where again $V_{DD}$ is the power-supply voltage. If $V_l$ is around $V_{DD}/2$, then the top device is on for $V_{in}$ up to $V_{DD}/2$ at which point the bottom device turns on and the top one turns off. If $V_l$ is less than $V_{DD}/2$, there will be a range of voltages where both devices are on and the shape of the transfer curve will be determined by the variation of contact resistance with input voltage which in turn depends on the strength of mechanical excitation of the two
gates. More complex gates can be formed by adding series and parallel connected devices as is done in designing CMOS gates (see figure 6).

With the model of figure 5, we can predict how such an inverter would perform when driving $N$ identical inverters (fan-out of $N$). Since we know that input-current is undesirable, it would be best to form the coupled NEMSETs from two types of pillars: a high-contact-resistance pillar for the input and a low-contact-resistance pillar for the output. However, if all the pillars are identical for ease of processing, the following simple rules will apply. The effective resistance varies inversely with the number of pillars connected in parallel. If $R_P$ is the contact resistance of a single pillar, and $R_{Pe}$ is the effective resistance of a single pillar, and given $L$ input pillars and $M$ output pillars, the equivalent circuit for the fan-out of $N$ is given by figure 7.

Notice that due to the charge transfer of the NEMSETs, there is a static dc voltage drop given by

$$\frac{V_{DD} - V_{OUT}}{V_{DD}} = \frac{N}{N + M/L},$$

to keep the voltage drop at less than 10%, we need $M/L = 9N$. So, for a fan-out of 4, we require 36 times more coupled output pillars than coupled input pillars. This ratio could be reduced if the contact resistance of the input pillars was increased relative to the output pillars while maintaining the same mechanical strength of oscillation.

We can also use this model to examine the switching speed. The time constant of the circuit in figure 7 is simply $R_{Pe}C_{sd}$. Assuming we can transfer five electrons per cycle with an oscillation frequency of 1 GHz and 1 V bias, $R_{Pe}$ can be estimated at 1.25 GΩ, and the estimated pillar capacitance is 10 aF. The resulting time constant is $\sim 12$ ns which permits logic toggle rates over 10 MHz.

Figure 5. Basic inverter using two coupled-NEMSET devices.
3. Memory

The concept of nanomechanical memory can be pushed beyond the conventional logic based on the expression of two states with nanomechanical elements (binary logic) [7]. It can be assumed that a nanomechanical system can have several instead of only two stable positions, which then corresponds to a multi-valued logic. A memory state in the conventional sense can be established with a NEMSET by simply starting from a bistable state, where the NEMSET can fall back into two potential minima. This can be achieved by either a magnetic island on the tip of the NEMSET, which can be spin-polarized, or using a bistable pillar in a three-terminal set-up. An example is a conducting magnetic pillar that can be attracted to either the left or the right electrode of a three-terminal set-up and maintain current flow in each state. A NEMSET thus can resonate between the input and either of the two output signals.

Figure 6. Two-input NAND gate formed with coupled-NEMSET devices.
4. Power

The scaling of the power of the nanomechanical circuits we find by applying the standard relation for CMOS dynamic power consumption $P = CV^2f$. Assuming an operating frequency of $f = 1$ GHz, a typical operating voltage of $V = 1$ V and a NEMSET total capacitance of $C = 10$ aF, we find a total dynamic power of $P = 10$ nW. This value can be further reduced by lowering the gating voltage to some 100 mV and the overall capacitance to below 10 aF. Under the assumption that the gate is switched at a speed of 1 GHz the total power corresponds to an energy of $E = 10$ aJ per switching event for nanomechanical transistors. At this stage this is only two orders of magnitude above the thermal energy limit $E_{th} = k_B T$ for 300 K. A computing architecture made from nanomechanical transistors thus is competitive with 45 nm CMOS technology\(^2\), while taking a step towards enabling reversible computing.

In summary, we have shown how to construct a computational device purely based on nanomechanical elements—the NMC. Single nanomechanical switches are operational and simulation shows that the concept is feasible for circuit integration.

Acknowledgments

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\(^2\) Based on an inverter with total $n$ and $p$-type device width of three times the 45 nm minimum feature size and $8.3 \times 10^{-16}$ F $\mu$m$^{-1}$ total gate capacitance.
References

[1] Gellings C W and Samotyj M 2002 Electric infrastructure to power a digital society IEEE Power Eng. Rev. 1 15–7
[2] Landauer R 1988 Dissipation and noise-immunity in computation and communication Nature 335 779
[3] Scheible D V and Blick R H 2004 Silicon nano-pillars for mechanical single electron transport Appl. Phys. Lett. 84 4632
[4] Kim H-S, Qin H and Blick R H 2007 Self-excitation in a nanomechanical resonator Nature Nanotechnol. submitted
[5] Tuominen M T, Krotkov R V and Breuer M L 1999 Stepwise and hysteretic transport behavior of an electromechanical charge shuttle Phys. Rev. Lett. 83 3025
[6] Scheible D V, Weiss Ch, Kotthaus J P and Blick R H 2004 Periodic field emission from an oscillating nano-scale electron island Phys. Rev. Lett. 93 186801
[7] Ruckes T, Kim K, Joselevich E, Tseng G Y, Cheung C-L and Lieber C M 2000 Carbon nanotube-based nonvolatile random access memory for molecular computing Science 289 94