In this paper, we propose a novel method to reduce power consumption during scan testing caused by test responses at scan-out operation for logic BIST. The proposed method overwrites some flip-flops (FFs) values before starting scan-shift so as to reduce the switching activity at scan-out operation. In order to relax the fault coverage loss caused by filling new FF values before observing the capture values at the FFs, the method employs multi-cycle scan test with partial observation. For deriving larger scan-out power reduction with less fault coverage loss and preventing hardware overhead increase, the FFs to be filled are selected in a predetermined ratio. For overwriting values, we prepare three value filling methods so as to achieve larger scan-out power reduction. Experiment for ITC99 benchmark circuits shows the effectiveness of the methods. Nearly 51% reduction of scan-out power and 57% reduction of peak scan-out power are achieved with little fault coverage loss for 20% FFs selection, while hardware overhead is little that only 0.05%.

**key words:** low power, BIST, multi-cycle test, shift power

1. Introduction

Power dissipation during testing has become a vital issue in the latest process technology. Particularly, it is known that power in scan-based testing is far higher than that in normal operation. In scan-shift mode, simultaneous switching activity (toggles) at many FFs may cause excessive power consumption, and it might result in large amount of IR-drop or di/dt-induced voltage violation, which causes a timing violation, or delay degradation due to overheating. In capture mode, excessive power caused by launch may result in setup-time variation or delay degradation, which causes yield loss or a quality problem [1].

Scan test is widely used not only for manufacturing test but also for system debug or field test. Even for logic BIST, at-speed testing is crucial to guarantee or improve the efficiency of debug and test. There exist many low power scan test methods that can be classified into two approaches: software-based approach and hardware-based approach. The software-based approach [1] such as utilizing don’t-care (X) bits reduces the test power by modifying the deterministic test patterns. However it is not applicable to logic BIST because random test patterns are used in logic BIST. The hardware-based approach such as blocking circuitry inserting [2], [3], scan segmentation technique [4], vector inhibition and selection techniques [5]–[7] have problems in terms of test application time increase, large area overhead or circuit performance degradation.

Methods inserting some logics that modify the scan-in patterns [8]–[12] have been proposed that can control power dissipation at scan-shift operation. Power dissipation at scan-shift operation consists of the scan-in power determined by test patterns and the scan-out power determined by test responses. While the methods in [8]–[12] focus on controlling the scan-in power by modifying test patterns with low switching activity, scan-out power control is out of considering. Although scan-out power is reduced as bi-product of scan-in power reduction as well as capture power reduction, the amount of reduction is not enough compared to that of scan-in power. It is also difficult to control the total scan-shift power only from scan-in power control. Therefore, scan-out power control still remains as important issue.

In this paper, we propose a scan-out power reduction method for logic BIST that allow us to control the total scan-shift power. The method selects some FFs of scan chain at logic design phase, and the values of the selected FFs are overwritten before starting scan-shift operation so as to reduce the switching activity associated with scan-out. Since filling new values to the selected FFs before observing the capture values at the FFs would result in fault coverage loss, we employ multi-cycle scan test with partial observation [14]. Capturing the FF values with multi-cycle before scan-shift operation brings more chances of fault sensitization, and observing the captured values of a part of scan FFs in many capture cycles brings more chances of fault detection. For achieving larger scan-out power reduction with less fault coverage loss, we theoretically analyze factors for scan-out power reduction and fault coverage improvement independently, and then propose a selection method with a ratio of FFs to be selected. For filling the selected FFs with new values, we prepare two scan FF architectures without delay penalty compared to conventional scan FFs and three value filling methods. Experimental results for ITC99 benchmark circuits show that the proposed method could reduce the scan-out power on average by 51% with 0.4% fault coverage loss for 20% FFs selection. In addition, the peak scan-out power is also reduced significantly (57% reduction in average) while hardware overhead increase is little that only 0.05%.

This paper is organized as follows. In Sect. 2, we introduce related works. In Sect. 3, we explain the proposed scan-out power reduction method. In Sect. 4 we give some experimental data for benchmark circuits, and conclude the
paper in Sect. 5.

2. Preliminaries

2.1 Power Metrics

Power consumption during scan-shift operation can be divided into the following two parts: 1) Scan-in power: The power consumed when scan test patterns are fed into scan chains. 2) Scan-out power: The power consumed when scan out the test responses are dumped from scan chains. It should be noted that scan-in and scan-out operate concurrently. Therefore, the total scan-shift power is defined as the sum of the scan-in power and the scan-out power.

In [1], [12], Weighted Transition Metrics (WTM) used for power evaluation is introduced. However, the formulations for scan-in power and scan-out power does not correctly treat the toggle occurred between the last bit of scan-in vector and the first bit of scan-out vector. In this paper, we reformulate the metrics in [1], [12] for evaluation of the scan-in power, the scan-out power and the scan-shift power as follows.

- **Scan-in power**: The formulation for a scan-in test vector $t$ is as follows.
  \[
  WTM_{in}(t) = \frac{1}{\sum_{i=1}^{L-1} i} \sum_{i=1}^{L-1} (t_i \oplus t_{i+1}) \times i + (t_L \oplus r_1) \times L
  \]  
  where $L$ is the scan chain length, $t_i$ is the $i$th bit of $t$ and $t_L$ is the last bit of $t$. $r$ denotes the captured test response in the scan chain and the $r_1$ is the first bit of $r$. $WTM_{in}$ is the average of (1) for all the test vectors.

- **Scan-out power**: The formulation for a test response $r$ is given as follows.
  \[
  WTM_{out}(r) = \frac{1}{\sum_{i=1}^{L-1} (L-i)} \sum_{i=1}^{L-1} (r_i \oplus r_{i+1}) \times (L-i)
  \]  
  where $L$ is the scan chain length and $r_i$ is the $i$th bit of $r$. $WTM_{out}$ is the average of (2) for all the test response vectors.

- **Scan-shift power**: The sum of $WTM_{in}$ and $WTM_{out}$ is used as the metric of the total scan-shift power. This is the same as average weighted transition metric. The metric for test vector $t$ and test response $r$ is as follows.
  \[
  WTM(t, r) = \frac{1}{2} [WTM_{in}(t) + WTM_{out}(r)]
  \]  
  $WTM$ is the average of (3) for all the test vectors and the test responses.

2.2 Low Power Multi-Cycle BIST

Many low power BIST methods have been proposed. For example, LT-RTPG [8], ALP-RTPG [9] and PLF [12] can reduce scan-shift power by reducing the number of toggles in scan-in test patterns. Figure 1 shows the concept of LT-RTPG and ALP-RTPG. In these two methods, some logic gates are inserted between a test pattern generator (LFSR) and a scan chain to reduce the number of toggles in the scan-in test patterns and hence shift power can be reduced. Figure 2 illustrates a structure of low power multi-cycle BIST scheme proposed in [12]. A pseudo low-pass filter (PLPF) is inserted between LFSRs and the scan chain inputs, where the PLPF is a combinational circuit that works as a filter to generate a modified low power scan-in vector. The generated vector is calculated from the moving average of logic values in the past vectors (feedback from the scan chain), a current vector and future vectors (extracted by PSF: Phase Shifter for Filter). Through the PLPF, the high frequency toggles in scan-in patterns are eliminated. In consequence, the scan-in vector will be smoother with low switching activity. In order to reduce the capture power (instantaneous power consumed by captured vectors at capture time), a multi-cycle test scheme [13] is employed. For preventing decrease in fault coverage, multi-cycle test with partial observation of flip-flops [14] is introduced, where a part of FFs are connected directly to an additional response compactor (compactor $B$), and their values that are captured during multiple capture cycles are compressed into compactor $B$. The values of all the FFs captured at the last capture cycle are observed by compactor $A$ in the shift mode.

Figure 3 shows the comparison of the scan-in power and the scan-out power reductions in LT-RTPG, ALP-RTPG and PLPF for 5 ITC99 benchmark circuits. It shows that three methods achieve significant scan-in power reduction. Although the scan-out power is reduced as the effect of scan-in power reduction, it is almost 2-times higher than scan-in power. For further reduction of the scan-shift power that is the sum of the scan-in and scan-out powers, the reduction of the scan-out power is indispensable.

In this paper, we employ the low power multi-cycle approach.
BIST scheme in [12] and focus on reducing the scan-out power.

3. Proposed Scan-Out Power Reduction Method

Figure 4 shows the idea of the proposed scan-out power reduction method [16]. First, the method selects some FFs for scan out control at logic design phase. We call the FFs “control FFs” (denoted as “C”). In scan testing, it fills the control FFs with proper values after the last capture before starting scan-shift operation using additional control circuits to make the scan-out vector smoother so as to reduce the switching activity associated with scan-out vectors. It should be noted that because capture power caused by launch affects delay propagation in the capture cycle, value-filling after the last capture will not affect the capture power. Since filling new values to the control FFs before observing the original captured values would affect the fault coverage. For compensating fault coverage loss, we employ multi-cycle scan test with partial observation [14], where the responses of CUT captured into the control FFs are compressed directly into an additional compactor (compactor B) during many captures (except the last capture) and the output (signatures) of compactor B are observed in shift mode as well as compactor A. Multi-cycle test consists of many capture cycles, which brings more chances of fault sensitization [15], and capturing the values of control FFs into compactor B during multiple clock cycles increases the number of fault detection chances. Therefore, even if the captured values of the control FFs are modified after the last capture, the loss of fault coverage could be compensated.

The proposed scan-out power reduction method has two issues to be solved as follows.

1. Control FF selection: It is needed to determine FFs that could reduce the scan-out power mostly by value filling and with less fault coverage loss by partial observation.

2. Value filling method: For the selected control FFs, we need to determine that what value to fill them could achieve the largest scan-out power reduction and control circuit will cause less hardware overhead increase.

3.1 Control FFs’ Selection

When controlling the scan out power, we need to consider not only scan-out power reduction but also fault coverage loss simultaneously. Although a part of fault coverage loss caused by filling new logic values in the control FFs might be compensated by multi-cycle test and partial observation, it is still needed to reduce fault coverage loss as far as possible. In this paper, we first theoretically analyze factors for the scan-out power reduction and the fault coverage improvement independently, and then propose a control FFs selection method that takes the factors into consideration simultaneously.

3.1.1 Factor for Scan-Out Power Reduction

In multiple captures test, high frequency bits in the test responses (i.e., “101010” or “010101”) that often produce high switching activity in shift operation [12] appear intensively in some groups of FFs in scan chains. Figure 5 shows the state of a scan chain after the last capture for b14 benchmark circuit. Each row denotes the state of the scan chain at different tests, and each cell denotes a scan FF in the scan chain (gray: state 1, white: state 0). We can see that a part of FFs that locates at the scan-in side of the scan chain toggles frequently during test, and high frequency bits concentrate there. Other parts of FFs in the scan chain almost do not toggle for most of the tests. Since high frequency bits have large number of toggles which result in big power [12], controlling the FFs that often produce high frequency bits should be effective for the scan-out power reduction.

We use toggle density to determine the FFs where high frequency bits concentrate in the scan chain. Toggle density is defined as the average toggle rate in the area of N bit adjacent of each FF at the last capture before scan-out operation. For a FF, the toggle density is computed by dividing the toggle number of the current vector by the maximum toggle number (e.g., vector as “...101010...”) in the area of N bit adjacent FFs ((N − 1)/2 bit adjacent FFs on the scan-in side and scan-out side, respectively). An example for toggle density computation is shown in Fig. 6. Suppose the state of a part of FFs in the scan chain after the last capture is “10010”, toggle density of \( f_i \) is \( 3/4 = 0.75 \) as \( N \) is set to 5 bits. It should be noted that for the FFs on the head of
scan-in or scan-out side of a scan chain, toggle density is the average toggle rate in the area of \((N-1)/2\) adjacent FFs on the scan-out side or the scan-in side, respectively. As shown in Fig. 7, \(ff_1\) and \(ff_x\) are the first scan FFs from the input and output side of the scan chain, respectively. The toggle density of \(ff_1\) is the average toggle rate in the area of \([ff_1, ff_2, ff_3]\), and toggle density of \(ff_x\) is the average toggle rate in the area of \([ff_{x-2}, ff_{x-1}, ff_x]\) as \(N\) is 5. For \(ff_2\) and \(ff_{x-1}\), toggle density is the average toggle rate in the area of \([ff_1, ff_2, ff_3, ff_4]\) and \([ff_{x-3}, ff_{x-2}, ff_{x-1}, ff_x]\), respectively. Figure 8 shows the toggle density of FFs in a scan chain for b14 circuit computed by logic simulation using 30k test vectors generated by PLPF [12]. Note the state of scan chain in Fig. 4. FFs that high frequency bits are concentrated are well denoted by toggle density.

It should be noted that elimination of the high frequency bits close to the scan-in side of the scan chain should be more effective for power reduction than that of close to the scan-out side. In order to determine FFs that are most effective for power reduction, we compute the toggle density weighted by location numbers for each FF by multiply their toggle density by the location number in the scan chain. Here, the location number of FFs is counted from the first scan-out FF (i.e., \(=1\)) to the first scan-in FF (i.e., \(=\) the scan chain length) in scan chain which shows the contribution to the scan-out power of the scan chain in which the FF belongs, because the number of scan-out clocks of the FF is proportional to its location number.

We consider that select the FFs with larger toggle density weighted by location numbers for scan-out control could achieve the most scan-out power reduction.

\[\text{Toggle number: 3} \quad \text{Maximum toggle number: 4 (for vector “10101”)} \quad \text{Toggle density: } \frac{3}{4} = 0.75\]

Fig. 6 Computation of toggle density.

The results of Fig. 7 and Fig. 8 show the special cases of toggle density computation. Fig. 7 shows the toggle density of a scan chain of b14.

\[\text{Area of 5 bit} \quad \text{Area of 3 bit} \quad \text{Area of 3 bit}\]

Fig. 7 Special cases of toggle density computation.

\[\text{Scan-in side (2 bit)} \quad \text{Scan-out side (2 bit)}\]

Fig. 8 Toggle density of a scan chain of b14.

3.1.2 Factors for Fault Coverage Improvement

While fault coverage loss caused by value filling might be relaxed by partial observation of FFs, resulting fault coverage depends on how to select FFs for partial observation. We select the FFs that have large fault coverage contribution for partial observation. A fault simulation-based method could maximize the fault coverage for a specified ratio of FFs. However, it requires huge computation time because sequential fault simulation without fault dropping for pseudo random patterns is time-consuming. In this paper, we evaluate the fault coverage contribution of each FF by analyzing the fault observation capacity and fault propagation capacity for each FF using logic cone analysis that is structural circuit analysis. The collapsed single stuck-at fault model is used in the evaluation because it has less number of faults that requires less computation time than transition delay fault model. In addition, circuits that have high stuck-at fault coverage should also have high transition fault testability. Evaluating the fault observation/propagation capacity based on stuck-at fault model should be appropriate for transition fault coverage estimation.

Fault observation capacity of a FF is defined as the number of faults that can be observed at the FF without passing through any another FF. Figure 9 shows the logic cone analysis for fault observation capacity. In the combinational logic of a sequential circuit, each FF has possibility of detection of faults in a specific region (e.g., region I for \(ff_1\), region II for \(ff_2\)) denoted by an input cone. Faults in region I can be observed at \(ff_1\) as effects of the faults may be propagated to \(ff_1\). Some faults in region I also can be observed at \(ff_2\) due to the region overlapping with II. If faults that can only be observed at \(ff_1\) are more than those at \(ff_2\) (i.e., number of faults in the non-overlapped region of I is larger than that of II), fault observation capacity of \(ff_1\) should be higher than \(ff_2\). On the other hand, if the number of faults that are only observed at \(ff_1\) is small, fault observation capacity of \(ff_1\) should be lower.

Fault propagation capacity of a FF is defined as the number of faults that can be propagated to the FF without through any other FFs. Figure 10 gives an example for fault propagation capacity analysis. In a sequential circuit, the effect of a fault that is only observed by \(ff_1\) might be propagated to another FF (e.g., \(ff_2\)) in the later time frames while propagation paths exist between them. These faults might be detected by another FF in the later capture cycles. However, if no propagation path exists between an FF and any other FFs (e.g., \(ff_3\)), the effect of a fault cannot be propagated to any other FFs. Such a fault cannot be detected at
any FF except $ff_3$ even with multiple-cycle test. Therefore if more faults only can be propagated (no propagation paths from a FF to any other FF), fault propagation capacity of the FF should be higher.

FF with high fault propagation capacity and fault observation capacity indicates that more faults will be only observed (propagated) at (to) the FF. These faults should have less chance of detection due to the faulty value masking during multi-capture [14]. Observing the FF during multiple captures brings more chances for these faults detection. Therefore, in this paper, we consider that select the FFs with higher fault propagation capacity and fault observation capacity for partial observation in multi-cycle test could increase the fault coverage.

3.1.3 Proposed Control FFs’ Selection Method

In order to achieve larger scan-out power reduction with less fault coverage loss, the control FFs’ selection method should take the factors of scan-out power reduction and fault coverage improvement into consideration, simultaneously. In this paper, we employ a multiple criteria decision analysis TOPSIS (Technique for Order Preference by Similarity to Ideal Solution) in [17] to select the FFs for scan-out control. The selection procedure is given as follows.

Step1: Create an evaluation matrix consisting of $M$ alternatives (#of FFs) and $N$ criteria (#of factors discussed above) with the intersection of each alternative and criteria given as $t_{ij}$, we therefore have a matrix:

$$T = (t_{ij})_{M \times N}, (i = 1, 2, \ldots, M, j = 1, 2, \ldots, N)$$  \hspace{1cm} (4)

Step2: Normalize matrix $T$ using following formula.

$$R = (r_{ij})_{M \times N}, \quad r_{ij} = \frac{t_{ij}}{\sqrt{\sum_{j=1}^{M} t_{ij}^2}}$$  \hspace{1cm} (5)

Step3: Calculate the weighted normalized decision matrix $v_{ij}$ by (6).

$$v_{ij} = w_j r_{ij}, \quad \sum_{j=1}^{N} w_j = 1$$  \hspace{1cm} (6)

Step4: Determine the worst alternative ($v_j^-$: minimum value of each factor) and the best alternative ($v_j^+$: maximum value of each factor), and calculate the distance between the target alternative $i$ and the worst condition ($S_i^-$) and the distance between the alternative $i$ and the best condition ($S_i^+$) by formula (7).

$$S_i^+ = \sqrt{\sum_{j=1}^{N} (v_{ij} - v_j^+)^2}, \quad S_i^- = \sqrt{\sum_{j=1}^{N} (v_{ij} - v_j^-)^2}$$  \hspace{1cm} (7)

Step5: Calculate the similarity to the worst condition ($C_i$) for each alternative by (8):

$$C_i = \frac{S_i^-}{S_i^- + S_i^+}$$  \hspace{1cm} (8)

Step6: Select the FFs with large $C_i$ for scan-out control.

3.2 Value Filling Methods

For the selected control FFs, we propose three value filling methods for achieving the largest scan-out power reduction.

3.2.1 Fixed-Value Filling

The selected control FFs can be filled with a fixed value (0 or 1) after the last capture [16]. As 0 appears more often than 1 in scan-out empirically, 0-value is used as the fixed value. Figure 11 shows the control circuit structure for 0-filling. The capture clock (CLK) and a last capture signal (LCAP) go through a NAND gate and generate a reset signal to set the control FF to 0 before starting scan-shift operation. Here, LCAP is generated by a clock counter just before the last capture cycle in the capture mode of multi-cycle test. The control structure for 0-filling is very simple and has small impact on area overhead, in addition, without delay penalty.

A fixed-value filling method can achieve great scan-out power reduction when the selected control FFs are consecutive, however, is not so effective for the alternate control FFs. Figure 12 shows a part of the distribution of the control FFs (denoted as “C”) in the scan chains of b14 circuit using the proposed selection method in Sect. 3.1. It shows that many selected FFs are consecutive and a part of the control FFs are alternate. Figure 13 and Fig. 14 give examples of 0-filling for consecutive control FFs and alternate control FFs, respectively. In Fig. 13, suppose that five control FFs (denoted as “C”) in the scan chain are consecutive and a response “01110101” is captured at the last capture. After 0-
filling, scan-out vector becomes “00000001” so that significant scan-out power reduction can be achieved. In Fig. 14, we use the same original vector as Fig. 13 and suppose two alternate control FFs are selected for 0-filling. The scan-out vector becomes “01010101”. In this case, 0-filling does not eliminate the high frequency bits \(p_1\), instead produces new high frequency bits \(p_2\) in the scan-out vector which results in scan-out power increase.

### 3.2.2 Adjacent-Value Filling (Ad-Filling)

The selected control FFs also can be filled with the value of its adjacent FF that locates in the scan-in direction [16]. Figure 15 shows the concept of the adjacent-value filling. Compared with the 0-filling method, the adjacent-value filling works better for the alternate control FFs, because the control FFs are dynamically filled with the values observed from the adjacent FFs so that high frequency bits such as “010” or “101” will always be eliminated and the original low frequency bits in scan chain will be unaffected. However, for the consecutive control FFs, the scan-out power reduction of the adjacent-value filling is smaller than that of the 0-filling.

Figure 16 and Fig. 17 give examples, in which the same original vector as Fig. 13 is used. In Fig. 16, the position of control FFs is the same as Fig. 14, but a filling method is changed to the adjacent-value filling. It shows that the high frequency bits \(p_1\) in the original scan-out vector is eliminated, and also the original low frequency bits are not affected. In Fig. 17, suppose five consecutive FFs can be selected as control FFs for 0-filling method (in the area with thick line as the same as in Fig. 13). The 2nd and 4th FF of the five consecutive FFs should not be assigned as control FFs in adjacent-value filling method because each control FF requires its adjacent FF for Ad-filling value feeding. When filling the control FFs (denoted as “C”) after the last capture, scan-out vector becomes “00110001”. Although the high frequency bits in the original scan-out vector is eliminated, scan-out power reduction is not so effective as the 0-filling method where the modified scan-out vector is “00000001”.

We view the distribution of control FFs in scan chains shown in Fig. 12. Many selected control FFs are consecutive. If we could feed the consecutive control FFs with the same FF value, it should be more effective for scan-out power reduction. However, control the path delay between FFs would become difficult. Therefore, in this paper we feed at most two control FFs by one adjacent FF value synchronously to avoid the affect of path delay as far as possible. An example is given in Fig. 18, in which two consecutive control FFs are filled with the same value of the adjacent FFs of them synchronously after the last capture. It shows that value filling not only eliminate high frequency bits “010” but also eliminate “0110”.

Figure 19 shows the control circuit structure for the adjacent-value filling. The capture clock (CLK) and the last capture signal (LCAP) generate a control signal through an AND gate to drive two NAND gates. The input DI of the adjacent FF is directly applied to one NAND gate and the other NAND gate through a NOT gate. The output of two NAND gates set the control FF to the same value as its adjacent FF's.

### 3.2.3 Hybrid Value Filling

Consider the merits and demerits of the 0-filling and the adjacent-value filling discussed above, combining with these two methods should be more effective for scan-out power reduction. Therefore, we propose a hybrid value filling method in which a threshold \(N\) of the length of consecutive control FFs is set to determine the value filling method for the selected control FFs. If a group of FFs are consecutive and the length is larger than the threshold \(N\), they will be filled with a fixed value 0, otherwise filled with the adjacent value after the last capture. Here, the threshold \(N\) is equal to the specified bit number of the area for toggle density computation discussed in Sect. 3.1 in order to unite control FF.
We evaluated the proposed methods using ITC99 benchmark data. A 16-bit internal type LFSR (characteristic polynomial: \(X^{10} + X^{15} + X^{13} + X^{4} + 1\)) and a pseudo low-pass filter (PLPF) in [12] are used to generate 30k test vectors. A parallel scan structure with 100 FF-length of scan-chains is adopted (when # of FFs > 1600, 200 FF-length). Because the capture power of a circuit becomes stabilized at a rather low level as applying many capture cycles (i.e., 20 capture cycles) [13], it suggests that IR-drop-induced yield loss could be avoided. Therefore, a multi-cycle BIST with 10 slow-captures (focused on stuck-at faults) and 10 fast-captures (focused on transition delay faults) are used in the experiments. Experiments are executed in 2 cases. In Case1: We focus on achieving the most scan-out power reduction and fault coverage was ignored. We select a specified ratio of FFs for scan-out control only according to the toggle density weighted by location numbers discussed in Sect. 3.1.1 where the bit number of the area for toggle density computation is set to 5. In Case2: In order to compensate the fault coverage loss, we execute the experiments using the selection method proposed in Sect. 3.1.3 in which the factors of fault coverage improvements are considered simultaneously. To prevent the increase of area overhead, only 20% of FFs are selected for scan-out control. The weighted transition metric discussed in Sect. 2.1 is used for power evaluation and a home-made fault simulator is used to estimate the single stuck-at fault coverage and transition fault coverage.

### 4. Experimental Results

Table 1 shows the comparison of the 0-filling (0), the adjacent-value filling (Ad) and the hybrid value filling (Hd) for Case1 and Case2. Here, “SI” and “SO” shows scan-in power and scan-out power respectively. The results of scan-in power and the original scan-out power without scan-out control (No-Ctrl) are shown in the second and third columns for comparison. Peak power reduction is very crucial because greater IR-drop or crosstalk is caused by high peak current. Therefore, we also evaluated the peak scan-out power and peak shift-power in Table 2, which are denoted by “P.Out” and “P.Shift”, respectively.

Table 1 shows the proposed value filling methods significantly reduce scan-out power. In Case1, the 0-filling could reduce the scan-out power of all circuit from the original 17.2% to 8.6% (i.e., 50% reduction) on average. The adjacent-value filling also achieves 37% scan-out power reduction (i.e., from 17.2% to 10.9%) which is smaller than that of 0-filling. This can be explained by Fig. 16. Many control FFs are consecutive so that scan-out power reduction of the adjacent-value filling is smaller than the 0-filling. The most power reduction is achieved by the hybrid value filling in which the original 17.2% scan-out power is reduced to 8.4% (i.e., 51% reduction) on average. In Case2, scan-out power also has been significantly reduced where the original 17.2% is reduced to 8.9% (i.e., 48% reduction) on average by hybrid value filling. Although the reduced scan-out power is bigger than Case1 (i.e., 8.4%), the difference is very small (i.e., 0.4%) and fault coverage loss can be compensated which will be discussed later. Table 2 shows that the proposed methods significantly reduced the peak scan-out power and peak shift power. The most peak scan-out power reduction is achieved by hybrid value filling that the original 23.5% is reduced to 10.0% (i.e., 57% reduction) in Case1. Peak scan-out power also has been reduced from the original 23.5% to 11.2% (i.e., 52% reduction) by hybrid value filling in Case2. As the scan-shift power is already at a very low level, nearly 40% reduction of peak shift power is a big advantage, which is not achieved by the conventional methods.

| Circuit | SI | No-Ctrl | Case1 Ad | Case1 Hd | Case2 Ad | Case2 Hd |
|---------|----|---------|-----------|-----------|-----------|-----------|
| b14     | 8.24 | 22.82 | 7.36 | 12.24 | 7.36 | 8.52 | 12.61 | 8.29 |
| b15     | 7.74 | 13.06 | 8.76 | 9.54 | 8.46 | 8.59 | 10.69 | 8.59 |
| b20     | 7.54 | 16.4 | 9.12 | 10.93 | 8.93 | 9.68 | 11.15 | 9.23 |
| b21     | 7.54 | 16.4 | 9.09 | 10.77 | 8.89 | 9.67 | 10.99 | 9.23 |
| b22     | 7.69 | 17.37 | 8.7 | 11.06 | 8.49 | 9.28 | 10.98 | 9.88 |
| AVE     | 7.75 | 17.21 | 8.61 | 10.91 | 8.42 | 9.15 | 11.28 | 8.86 |

### 4.2 Fault Coverage Estimation

Table 3 shows the comparison of fault coverage for stuck-at faults (SA) and transition delay faults (TD) using the proposed value filling methods. In Case1, it shows that no stuck-at fault coverage is lost and transition fault coverage loss is little that 0.43%, 0.28% and 0.43% is lost by the 0-filling, the adjacent value filling and the hybrid value filling, respectively. The adjacent value filling have less transition fault coverage loss. This is because it dynamically fills the control FFs with the values observed from the adjacent FFs after the last capture which has less impact on fault detection. In Case2, fault coverage of most of circuits is improved and transition fault coverage loss is only 0.01% on average by the hybrid value filling, and 0.42% fault coverage loss in Case1 is compensated. It is because the control FFs’ selection method takes the factors of fault coverage improvements into consideration simultaneously, so that FFs with high fault coverage contribution are selected for scan-out control and are observed during multi-cycle test which
brings more chances for detecting more faults.

4.3 Area Overhead (Investment) Estimation

Discussing hardware overhead of the proposed scan-out power control method on small circuits is not appropriate. We evaluated the area overhead imposed by the proposed value filling methods on a large data model that is based on the SoC model in the Test and Test Equipment chapter of ITRS2009 [18]. We consider that FFs in the SoC model are set-reset type flip-flops for area overhead computing. Since partial observation of FFs requires an additional compactor (consists of an XOR tree and a MISR) which causes 1.93% area overhead as 20% FFs observation [14], it will be included in our evaluation. In order to estimate the area overhead for the hybrid value filling, we evaluate the ratio of FFs that are controlled as the 0-filling and the adjacent value filling in the hybrid value filling for all circuits. Table 4 shows the results, where the number of control FFs is shown in the second column. We can see that approximately 97% of control FFs are controlled as the 0-filling and 3% are controlled as the adjacent value filling for the hybrid value filling. Therefore, we use ratio 97% for the 0-filling and ratio 3% for the adjacent value filling to compute the area overhead of the hybrid value filling on the evaluation model. Figure 21 shows the estimation result. It shows that the 0-filling increases very little area overhead (i.e., 0.01%) and the adjacent-value filling causes the most increase of area overhead (i.e., 1.4%). The hybrid value filling only causes 0.05% increase of area overhead because most of the selected FFs are controlled by the 0-filling method.

5. Conclusions

In this paper, we proposed a novel approach to reduce scan-out power for logic BIST. The proposed method selected some FFs of scan chains at logic design phase, and filled the selected FFs with proper values before starting scan-shift operation so as to reduce the switching activity associated with scan-out. In order to prevent the fault coverage loss caused by value filling, the selected FFs are directly observed during many captures in multi-cycle BIST. Three methods of value filling were proposed and compared. Experimental results showed the effectiveness of the methods.

The original scan-out power was reduced from 17.2% to 8.4% (i.e., 51% reduction) with 0.4% transition fault coverage loss for 20% FFs selection. In addition, 57% reduction of peak scan-out power and 40% reduction of peak scan shift power were achieved, while hardware overhead increase was little that only 0.05%.

Because the scan-out power was already at a very low level, nearly 51% reduction is a big advantage, which is not achieved by the conventional methods. Peak shift-power is
very sensitive to the timing issues such as a hold time error during scan-shifting, a very severe reduction is needed in the very deep submicron technologies. Then, the proposed approach will contribute to this problem.

References

[1] P. Girard, N. Nicolici, and X. Wen, Power-Aware Testing and Test Strategies for Low Power Devices, Springer, ISBN 978-1-4419-0927-5, New York, 2010.

[2] S. Gerstendorfer and H.-J. Wunderlich, “Minimized power consumption for scan-based BIST,” Proc. Int’l Test Conf., pp.77–84, Sept. 1999.

[3] A. Hertwig and H.-J. Wunderlich, “Low power serial built-in self-test,” Proc. European Test Workshop, pp.49–53, May 1998.

[4] L. Whetsel, “Adapting scan architecture for low power operation,” Proc. Int’l Test Conf., pp.863–872, Oct. 2000.

[5] F. Corno, M. Rebauendo, M.S. Recorda, and M. Violante, “A new BIST architecture for low power circuits,” Proc. European Test Workshop, pp.160–164, May 1999.

[6] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, “A test vector inhibiting technique for low energy BIST design,” Proc. VLSI Test Symp., pp.407–412, April 1999.

[7] C. Zoellin, H.-J. Wunderlich, N. Maeding, and J. Leenstra, “BIST test generation with preselected toggling for low power built-in self-test,” Proc. Int’l Test Conf., paper 32-3, Oct. 2006.

[8] S. Wang and S.K. Gupta, “LT-RTPG: A new test-per-scan BISTTPG for low heat dissipation,” Int. Test Conf., pp.85–94, Oct. 1999.

[9] X. Lin and J. Rajski, “Adaptive low shift power test pattern generator for logic BIST,” Asian. Test Symp., pp.355–360, Dec. 2010.

[10] M. Filipek, Y. Fukui, H. Iwata, G. Mrugalski, J. Rajski, M. Takakura, and J. Tyszer, “Low power decompressor and PRPG with constant value broadcast,” Asian. Test Symp., pp.84–89, Nov. 2011.

[11] J. Rajski, J. Tyszer, G. Mrugalski, and B.N.-Dostie, “Test generator with preselected toggling for low power built-in self-test,” Proc. VLSI Test Symp., pp.1–6, April 2012.

[12] Y. Sato, S. Wang, T. Kato, K. Miyase, and S. Kajihara, “Low power BIST for scan-shift and capture power,” Asian. Test Symp., pp.173–178, Nov. 2012.

[13] E.K. Moghaddam, J. Rajski, S.M. reddy, and M. Kassab, “At-speed scan test with low switching activity,” Proc. VLSI Test Symp., pp.177–182, April 2010.

[14] Y. Sato, H. Yamaguchi, M. Matsuzono, and S. Kajihara, “Multi-cycle test with partial observation on scan-based BIST structure,” Asian Test Symp., pp.54–59, Nov. 2011.

[15] J. Abraham, U. Goel, and A. kumar, “Multi-cycle sensitizable transition delay faults,” IEEE VLSI Testing Symp., pp.306–311, April 2006.

[16] S. Wang, Y. Sato, K. Miyase, and S. Kajihara, “A scan-out power reduction method for multi-cycle BIST,” Asian. Test Symp., pp.272–277, Nov. 2012.

[17] K. Yoon, “A reconciliation among discrete compromise situation,” J. Operational Research Society, vol.38, no.2, pp.277–286, 1987.

[18] W. Wang, V. Reddy, A.T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, “Compact modeling and simulation of circuit reliability for 65-nm CMOS technology,” IEEE Trans. Device and Material Reliability, vol.7, no.4, pp.509–507, 2007.