SIMPLEX: Repurposing Intel® Memory Protection Extensions for Information Hiding
Salvaging Endangered Hardware Features for Security

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ABSTRACT
With the rapid increase in software exploits, the last few decades have seen several hardware-level features to enhance security (e.g., Intel MPX, ARM TrustZone, Intel SGX, Intel CET). Due to security, performance and/or usability issues, these features have attracted steady criticism. One such feature is the Intel® Memory Protection Extensions (MPX), an instruction set architecture extension promising spatial memory safety at a lower performance cost due to hardware-accelerated bounds checking. However, recent investigations into MPX have found that it is neither as performant, accurate, nor precise as cutting-edge software-based spatial memory safety. As a direct consequence, compiler and operating system support for MPX is dying, and Intel has begun to manufacture desktop CPUs without MPX. Nonetheless, given how ubiquitous MPX is, it provides an excellent yet under-utilized hardware resource that can be aptly salvaged for security purposes. In this paper, we propose SIMPLEX, a library framework that re-purposes MPX registers as general purpose registers. Using SIMPLEX, we demonstrate how MPX registers can be used to store sensitive information (e.g., encryption keys) directly on the hardware. We evaluate SIMPLEX for performance and find that its overhead is small enough to permit its deployment in all but the most performance-intensive code. We refactored the string buffer manipulation functions and found a geometric mean 0.9% performance overhead. We also modified the deeps jeng and lbm SPEC CPU2017 benchmarks to use SIMPLEX and found a 1% and 0.98% performance overhead respectively. Finally, we investigate the behavior of the MPX context with regards to multi-process and multi-thread programs.

1 INTRODUCTION
Intel® Memory Protection Extensions (MPX) is an instruction set architecture (ISA) extension for modern Intel processors providing spatial memory safety using compile-time intentions. MPX is comprised of three key components working in harmony: architectural support through a set of two configuration, one status, and four bounds registers; compile-time instrumentation; and run-time support integrated with the operating system. This run-time manages enabling and disabling CPU interpretation of MPX instructions through the configuration registers, sets up the pointer bounds lookup table, interprets error codes indicated in the status register, and coordinates with the operating system to handle memory management and error handling.

In practice, MPX is unusable in its intended form. It was intended to be performant, interoperable with uninstrumented legacy code, and configurable for both debug and release environments without rewriting the source. However, Oleksenko et al. and Serebryany independently showed that MPX does not perform as well as software- and language-based memory safety, demonstrating a 50% amortized performance overhead with good compiler optimizations, and a 400% worst-case performance overhead [25, 31].

As such, MPX has steadily lost support in the software community. The GNU C Compiler (GCC) recently removed its libmpx library and eliminated the instrumentation code, while Clang has never supported MPX beyond specifying the instruction opcodes in its x86 targets. Additionally, Linux recently removed its support for kernel compilation with MPX because of the lack of support from the GNU community. In short, it now appears that MPX will not achieve widespread adoption as a memory safety tool that it was designed for. Yet, MPX is already a supported feature on widely deployed processors (e.g., Skylake). For example, Passmark reported that by 2017 all of the Intel CPUs that they sold were the first-generation Skylake model or later [2]. Even a conservative estimate puts the number of MPX-supported deployments at 100s of millions worldwide. Therefore, MPX is a ubiquitous—yet unused—resource.

In this paper, we leverage MPX for general purpose data storage with emphasis on data hiding. Ability to hide data is a valuable resource in security. For example, in the enforcement of control-flow integrity using a shadow stack, it is necessary to ensure integrity of the shadow stack while accommodating frequent updates to the shadow stack whenever there is a call or a ret instruction. Similarly, it is often beneficial to isolate critical encryption keys and passwords from memory in order to protect their integrity and confidentiality in case of memory corruption and/or information leakage. On the one hand, hiding data in the kernel is often impractical as it incurs (sometimes prohibitive) performance overhead due to the expensive transition to/from user and kernel modes. But on the other hand, recent attacks demonstrate that hiding data in userland is ineffective even in a 64-bit address space[24].

Our contribution is codenamed SIMPLEX, which is comprised of a library enabling extrospection and manipulation of the MPX context, a minimalist runtime that avoids the overhead associated with the compiler-provided MPX runtime, a test suite verifying correctness, and evaluations demonstrating the practicality of SIMPLEX. SIMPLEX provides abstractions to the underlying MPX operations such that its “bounds” registers appear to behave identically to general purpose registers, even though Intel does not provide specific access and mutation instructions in the MPX extension. SIMPLEX completely avoids the bounds lookup table and associated runtime costs, which form the main source of overhead for MPX use [25, 27]. SIMPLEX provides storage in MPX registers optimally used to store...
data that is undesirable or risky to be stored in userspace memory, when the data size is small (ideally 8×64 bits, although Simplex also provides 4×128-bit operations), and when the data is infrequently accessed. Simplex is particularly beneficial to use in cases such as information hiding because previous works use a modified compiler to reserve a general purpose register for hiding (e.g. [19, 21, 22, 34]). Reserving registers is undesirable for two reasons: (1) it removes a register from the allocation pool, which could in-turn impact performance due to sub-optimal register allocation [5], and (2) it affects interoperability when handwritten assembly or binaries not compiled using the modified compiler may accidentally access or modify the reserved register. This in turn may compromise confidentiality or integrity of the hidden data. Because Simplex uses the MPX bounds registers, and because the bounds registers are not used unless the application was also explicitly compiled with MPX support, we can ensure that no other code will access or modify the hidden data or pointer stored inside the bounds register.

Our evaluation shows that Simplex is practical, and confirms initial observations by Otterstad [27] and Oleksenko et al. [25] that the majority of MPX’s performance cost comes from interacting with the bounds lookup table and associated costs within the runtime. We avoid this overhead because Simplex avoids using the bounds lookup table by writing to the bounds registers directly using the `bndmov` instruction and reading from the bounds registers using the `bndmov` instruction to spill the contents into memory. We evaluated for performance in two different ways. First, we created three custom benchmark fixtures: a microbenchmark testing the rate at which load and store operations can be completed to both the %r15 general purpose register and the `%bnd0` MPX register, a macrobenchmark simulating information unhiding by traversing and combining two hidden half-buffers, and a series of benchmark implementations of memory operations from the `string.h` header. Second, we compiled sandboxed versions of two SPEC CPU2017 benchmarks: 519.ibm, a particle-fluid simulation written in C, and 531.deepsjeng, a chess engine written in C++. Finally, we evaluated for usability and correctness by modifying the OpenSSL Blowfish cipher, then running the included integration and unit test suites. We further discuss these evaluations in §5.

2 BACKGROUND

2.1 Intel MPX

In 2012, Intel introduced PointerChecker, which provides bounds checking in the software layer through the Intel Composer XE development environment for C and C++ [13]. Recognizing the potential for greatly improved performance through hardware support, Intel moved much of the Pointer Checker functionality into MPX, announced in 2013 [30] and subsequently debuted in the Skylake architecture in 2015.

MPX is a combination of an instruction set extension, compiler and operating system support, and runtime library. It provides four new 128-bit bounds registers (%BND0 through %BND3), each of which are split into an upper half and lower half which have the purpose of holding an upper bound and lower bound address. MPX also employs the %BNDCFGx register pair to hold user-space and kernel-space configuration, and a %BNDSTATUS register to hold status information in case of a bounds check failure. Intel designed MPX with the overarching goal of compatibility with uninstrumented code and unextended architectures. Where an MPX-supported CPU encounters uninstrumented code, such as a vendor-provided library, program execution continues with the cost that the CPU can no longer provide memory safety because the bounds checks are not performed unless a bndc1, bndcu, or bndcn instruction is executed. Where an MPX-unsupported CPU encounters instrumented code, or when MPX has not been initialized by setting `%bndcfg[0]`, the instructions are interpreted as nop instructions instead of triggering unrecognized instruction exceptions.

2.2 Ubiquity of MPX

Although no direct count of deployed processors with MPX support exists, we nonetheless believe that MPX is ubiquitous based on inferences from publicly available data. For example, the Steam Hardware and Survey for May 2019 – which automatically polls the hardware of the Steam gaming service’s users – shows that 81.97% of users have an Intel processor [3]. Likewise, PassMark reported that based on the benchmark baselines submitted from July 2013 (when MPX was introduced) through the present, Intel has had a market share between 73.60% and 82.50% [2]. This is an important contrast to the Steam survey because it does a better job of accounting for the server market, whereas the Steam survey highlights the desktop market, specifically gaming computers. More optimistically, Intel’s 2018 financial reports indicated that they held 84.2% of the desktop market, 87.9% of the notebook market, and 96.8% of the server market, for a weighted share of 90.41% [17].

Second, within Intel’s large market share, we believe that the overwhelming majority are compatible with MPX based on sales data. For example, according to Mindfactory – a leading German computer parts retailer – not later than 2017, all of the Intel processors that they sold were of the first MPX generation Skylake architecture or more recent. By 2019, Skylake represented only 1% of Mindfactory’s sales, with 92% belonging to the most recent Coffee Lake or Coffee Lake-Refresh architectures [16]. This suggests that the CPU sales dynamic heavily favors recent models, and thus ISA extensions are quick to penetrate the market share. Lastly, we note a 2016 estimate that by 2019 there would be over 1.3 billion desktop computers worldwide [12]. Thus it is reasonable to conclude that the potential impact of Simplex is high as numerous computers – possibly hundreds of millions – will gain register storage through repurposing their bounds registers. This benefit comes without modification to the underlying architecture or perceptible cost to the end user and has security-sensitive applications including information hiding or cryptographic operations.

2.3 Present State of MPX

MPX is impractical to use in its intended form. Although MPX achieves a four- to five-fold speedup compared to Pointer Checker [25], it is not without significant issues hindering its widespread adoption, foremost of which is the execution cost. MPX-enabled benchmarks experience worst-case 200% performance overhead, 480% memory overhead and 5.4x more page faults [25]. Additionally, bounds table lookups appear to cause significant cache pressure.
Even on legacy hardware, where the MPX instructions are interpreted in an idempotent manner, there is still up to a 50% slowdown [31]. Furthermore, MPX cannot catch temporal memory safety issues such as heap use-after-free and stack use-after-return [25], it has false positives from otherwise legal C idioms due to restrictions on structure memory layouts [25, 31], it experiences false negatives in response to undefined behaviors which cause inappropriate bounds loads [27], it conflicts with other Intel ISA extensions such as SGX and TSX [25], and it has no explicit support for multithreading [25].

As a result, support for MPX has waned. Currently MPX’s only compiler support is Intel’s own ICC since version 15.0 and Microsoft’s Visual Studio 2015 Update 1. GCC has dropped support and Clang never supported MPX.

Despite the sunset of support for MPX in its memory safety usage, we must emphasize that Simplex does not rely on either compiler or operating system support to function. The Simplex library provides all necessary runtime components and functions for instrumentation, and the MPX context is part of the broader XSAVE context, thus it is still saved and restored on context switches even though Linux formally removed all MPX support as of kernel version 5.6.

2.4 Information Hiding

Recent works demonstrate that information hiding techniques relying on probabilistic mechanisms can be defeated. Göktaş et al. demonstrated thread spraying [14] as a means of disclosing the safe regions with a known structure. By repeatedly creating objects that have safe stacks and regular stacks, then probing the space to find one of these hidden safe stacks, they can effectively de-randomize the address space. They also discovered that information in the thread local storage (TLS) and the thread control block (TCB) provide clues to locating these stacks. Furthermore, Oikonomopoulos et al. introduced allocation oracles which eliminate the need for probing [24]. The idea is that an allocation oracle takes the size of an area to allocate as input, and if successful returns the location allocated. From this information and applying a binary search technique, an attacker can locate “holes” in the allocatable memory. If the attacker has knowledge of how a defense’s sensitive data is laid out, then these holes reveal where the sensitive data is not hidden. With enough queries to the oracle, eventually the sensitive data can be located, and the process avoids crashes or distinguishable behavior usable by a runtime detector. Likewise, Evans et al. used timing side channels to read the contents of hidden metadata with or without crashes (the former is faster, the latter is difficult to detect) [11]. Using this technique, they can de-randomize the location of libraries such as libc, then use this to calculate the start of the safe region. Once complete, modifying the contents of the safe region permits an attacker to violate at least one implementation of CPI.

Recent work has shown that having registers to simulate segmentation as available in the IA-32 architecture can be used to provide deterministic rather than probabilistic information hiding. Koning et al. introduce MemSentry, a collection of implementations of information hiding relying on a variety of hardware support [18]. One common point of these implementations is that they would benefit from dedicated registers. Finally, two of the implementations of Code Pointer Integrity require a dedicated register for information hiding [19]. In the implementation released at the time of publication, the %fs register was reserved, however this may affect other legitimate usages of the register. For example, operating systems...
sometimes use this register to access thread local storage (TLS). Providing register storage via Simplex helps return reserved general purpose registers to the compiler’s allocation list and restores special purpose registers to their expected usage.

3 SIMPLEX

3.1 Threat Model
We assume a threat model similar to that offered by other work on information hiding, namely Koning [18] and Yun [33]. Our system under threat has an effective defense against code reuse, which in turn prevents an attacker from arbitrarily calling the Simplex library functions, even though he or she may have an arbitrary read or write primitive. Although Simplex might be used to store a pointer to a hidden memory region, it does not itself provide isolation. We assume that the programmer has a Trusted Code Base comprised of at least a privileged, trusted operating system and a trusted build toolchain used to build the Simplex library. We concede that an attacker may be able to load a Loadable Kernel Module (LKM) that enables or disables MPX at a privileged operating system level (and in fact, we provide one such implementation within the Simplex code base). However, this would imply a compromised kernel, which is outside our scope. That said, we show in §3.4, that is not sufficient for an attacker to emplace values into the bounds registers or leak values from the bounds registers in a way that is beneficial to the attacker. Finally, we assume that Simplex is correctly implemented and is trusted by the programmer. We release our code as open source, and offer a full test suite within that code base as an assurance to that assumption.

3.2 Design Decisions
Previous works seeking to hide information from attackers have chosen one of three options. 1) Storing information in the kernel or in pages that can only be accessed in a privileged hardware mode (e.g. [1, 15]) is secure as long as the operating system is not compromised. However these schemes come with the obligation of additional context switches for each query or update, hampering performance. 2) A more performant choice is storing information in a hidden region within the program’s address space (e.g. [9, 19, 22]). Yet it relies on either probabilistic hiding measures which can be defeated if the attacker has knowledge of the type of information being hidden, or if the attacker is able to tolerate crashes and restarts while searching. 3) Alternatively, it is possible to reserve registers from the compiler’s allocation pool and use these registers exclusively for storing sensitive data. Once the registers are selected, the defender can formally verify that no other code accesses these registers, guaranteeing security. Nonetheless, there is still the concern that available registers are limited and may conflict with other defenses or dynamically linked code that use the reserved register.

3.3 Simplex-Enabled Compilation
In our evaluations, we manually replaced global pointer objects and their reference/dereference statements with the necessary code to enable bounds register usage. However, we do not feel this is scalable. Consider the modifications made to the SPEC CPU2017 benchmarks: 519.1bm has just 1 KLOC and required 22 modifications, 531. deeps.jeng has only 10 KLOC and required 173 modifications - these are very small code bases compared to 502. gcc (1.3 MLOC) and 526. blender (1.6 MLOC), the largest C/C++ benchmarks in CPU2017. Making these modifications are expensive in terms of developer effort and time, requiring both discovering and understanding the global variables’ utilization. For example, modifying the two SPEC CPU2017 benchmarks took about two days of development time each. If the number and complexity of changes necessary were to scale, implementing the larger benchmarks by hand could take months! Therefore, we have designed but not yet implemented a system using Clang’s annotation system to mark variables as candidates for placement in a bounds register. This reduces the developer’s workload to simply recognizing which variables should go into a bounds register, applying annotations to the declarations, then compiling the source code with the options necessary to enable Simplex.

First, the developer applies the necessary annotation at the variable’s declaration. The compiler recognizes the annotation, and maps that variable to one of the bounds registers, depending on its size or throws a compilation error if no more register space is available. Next, the compiler pass replaces references to these variables with appropriate Simplex function calls. If the variable is an lvalue, it is replaced with a call to one of the mutator functions; if it is a rvalue, it is replaced with a call to one of the accessor functions.

Developer annotation vs Automated discovery: On the one hand, developer annotation has the benefit of precisely capturing what is of security relevance and importance as per software design, but on the other hand, developers are prone to make mistakes. Therefore, we recommend 3 modes of operation that makes a trade off between security and performance.

Whitelisting: In this mode, we allow a developer to whitelist security-sensitive data that is stored in the MPX bounds registers by the compiler. This is the most conservative and performance-friendly, yet error-prone option.

Automatic inference: In this mode, the compiler employs a heuristic approach to automatically profile and identify security sensitive information and accordingly provisions MPX bounds registers to manage such sensitive data. One option is to identify security-sensitive documented API functions and perform backward slicing to identify data of interest. This is the most aggressive option that favors security over performance.

Blacklisting: Finally, as an intermediate option, blacklisting allows a developer to define data items that should not be stored in the MPX registers. While blacklisting is just as prone to human error as is whitelisting, it is likely to have less adverse effects on security as compared to mistakes in whitelisting.

3.4 Context Behavior
We performed experiments to determine the behavior of the MPX context using the system under evaluation described in §5. We identified three phases in the lifespan of a scheduling entity: its creation (i.e. calling fork() for processes, or pthread_create() for threads), mid-life – specifically when a parent or sibling modifies
3.4.1 Processes. According to the POSIX standard, upon calling fork(), a new process is created by duplicating the parent. As part of this duplication, the child has a memory space, processor context and file descriptor table that are initially identical but separate from the parent. However, the child has a unique process ID (and thus is scheduled independently from its parent). Furthermore, the child does not inherit the parent’s memory locks, signals, semaphores, processor timers or counters.

At process creation, the child inherits an identical MPX context to that of the parent because the MPX context is itself part of the larger CPU context (see Figure 1). If MPX is enabled or disabled because of the values on the %BNDCFGx[1:0] bits for the parent, it will be likewise enabled or disabled for the child upon its creation via fork(). Additionally, the values in the parent’s bounds registers will be inherited by the child’s bounds registers, because the bounds registers are a component of the MPX context. Meanwhile, during the lifespan of both the child and the parent, changes in one process’ context do not affect another process even if one is an ancestor or sibling of the other. Subsequently disabling or enabling MPX in a parent does not confer this change in status to the child, nor does changing the values of a parent’s bounds registers propagate to the child. Furthermore, terminating one process does not change the MPX context of any related process.

The reader may question whether a child might inadvertently pass information about its Simplex state to the parent through wait(). At a minimum, wait() passes the process id through its return value. Optionally, it may pass a developer specified integer values using wstatus from child to parent, and may pass an integer error code through the errno flag. However no processor context is contained in this information and therefore two processes using Simplex are fully independent from each other beginning immediately after process creation. Thus there is no risk of leaking secrets across processes when using Simplex above and beyond the risk that is incurred by hiding that information in the process address space or in a reserved register.

Briefly, upon creation of a process, the child inherits the context of the parent, but this context is unshared thereafter. We summarize these findings in Table 1.

3.4.2 Threads. POSIX threads are a kernel scheduling entity, such that a single process contains multiple threads, all of which are executing the same program. Thus although each process’ threads share global memory, the threads must have their own call stack and its own CPU context in order to perform its own program counter. When a process creates a new thread using pthread_create(), the newly created thread initially inherits the calling process’ CPU state, except that in order to begin execution at the specified start routine, the program counter must be set to the appropriate address. Accordingly, the newly created thread inherits the calling process’ MPX configuration and bounds registers context, similar to the inheritance between a parent and child process described above. Similar to the behavior shown by processes, the various threads of a single process do not share the configuration nor bounds registers’ values once the thread is initialized; the created thread’s MPX context is immediately independent from that of its creator.

Briefly, upon creation of a thread, the child inherits the context of the parent, but this context is unshared thereafter. We summarize these findings in Table 2.

3.4.3 Repetitive Initialization and Finalization. Because Simplex provides methods to initialize and finalize its minimal MPX context, the reader may question what would happen if a programmer or attacker called these methods repeatedly (whether by accident or malice). We created a toy program that tests these corner cases.

First, we initialize the program, setting the bounds registers to known values, then initialize the program a second time. We found that each time the MPX context is initialized, the bounds registers’ lower bounds are set to the system maximum unsigned value, and the upper bounds are set to 0. In MPX’s design use case, this results in a guaranteed passed bounds check until the bounds register is set to some allocated object’s bounds. In the Simplex use case, repeated initialization destroys the values inside the bounds registers by resetting them to the conservative bounds values. Although this may allow an attack against availability, it does not allow an attack seeking disclosure. Furthermore, it is no more dangerous than the numerous xor reg reg gadgets which are used by the compiler to place a zero value in a register.

We also found that after finalization, each of BND1 through BND3 are reset. However, BND0 displays unusual behavior in that while the lower bound is reset, the upper bound receives a random large value (the most significant bit is always set, but otherwise there is no identifiable behavior). Thus subsequent repeated finalizations are similar to repeated initializations in that they can cause availability but not disclosure problems. We summarize these findings in Figure 3.

4 IMPLEMENTATION

4.1 Components of Simplex

Unfortunately, there is no means of directly accessing the MPX bounds registers via a mov instruction. Each of GCC, ICC and Microsoft’s Visual C++ compiler do offer intrinsics, although there are only available if a MPX runtime is available and providing bounds checking [29]. This means it is not possible to use these intrinsics for accessing the bounds registers without also suffering the continual risk of a bounds check clobbering the bounds registers. Therefore, within Simplex we provide a system readiness check, a minimal runtime to enable and disable MPX execution without the additional overhead of bounds checking and a bounds lookup table, accessor and mutator functions, and a test suite to verify proper operation of the library. We demonstrate usage of this functionality in Figure 2.

System Readiness Check. Although it is possible for a user to test whether their system can support MPX from the command line using commands such as lscpu and sysctl, a program must be able to verify readiness itself and abort further execution if it cannot prove its readiness. This is because CPUs which do not support MPX will silently interpret these MPX instructions as NOPs. We have isolated the necessary checks from the GCC 5.0 MPX runtime library. These checks verify that %SCPUID[14] is set (indicating that the CPU supports the MPX extension), and that %XCR0[3:4] are
Table 1: Simplex context behavior for a parent and child process.

| Event | Parent | Child |
|-------|--------|-------|
|       | Enabled? | BND0 | Enabled? | BND0 |
| Parent calls process_specific_init() and setbnd(BND0, 1) | ✓ | 1 |    |   |
| Parent calls fork() | ✓ | 1 | ✓ | 1 |
| Child calls setbnd(BND0, 2) | ✓ | 1 | ✓ | 2 |
| Child calls process_specific_finish() | ✓ | 1 | ✗ | - |
| Child calls exit() | ✓ | 1 |    |   |

Table 2: Simplex context behavior for a parent and two child threads.

| Event | Parent | Child 1 | Child 2 |
|-------|--------|---------|---------|
|       | Enabled? | BND0 | Enabled? | BND0 | Enabled? | BND0 |
| Parent calls process_specific_init() and setbnd(0, 0) for Child 1 | ✓ | 0 |    |   |
| Parent calls pthread_create() for Child 2 | ✓ | 0 | ✓ | 1 | ✓ | 2 |
| Child 1 calls setbnd(0, 1) for Child 2 | ✓ | 0 | ✓ | 1 | ✓ | 2 |
| Child 2 calls setbnd(0, 2) | ✓ | 0 | ✓ | 1 | ✓ | 2 |
| Child 2 calls process_specific_finish() | ✓ | 0 | ✓ | 1 | ✗ | - |
| Child 1 calls process_specific_finish() | ✓ | 0 | ✗ | - | ✗ | - |

Table 3: Simplex context behavior during repetitive initialization and finalization.

| Initialization | Finalization |
|----------------|--------------|
|                | First | Subsequent | First | Subsequent |
| Config Registers | Enabled | Enabled | Disabled | Disabled |
| Bounds Registers | Reset | Reset | BND0: Undefined, BND1-3: Reset | BND0: Undefined, BND1-3: Reset |

Accessor and Mutator Functions. For each of the four bounds registers, a common accessor and mutator wrapper function provides a handle to the bounds register. There are four varieties of each wrapper function: lower-half 64 bits only, upper-half 64 bits only, all 128 bits, and a “quick” lower-half only which does not attempt to save the upper-half nor clean the stack of any spilled values. The applicable bounds register is selected through an enumerator with four values, thus corresponding “BND0” to the integral value 0 and so forth. Within each wrapper function is the necessary extended assembly statements to either set or get the values from the bounds register. When writing to the bounds registers, the value to be written is marshaled from the function arguments into a sub-addressed bndmk instruction. When getting, the bounds register is spilled onto the stack above the stack pointer without moving the stack pointer as there is no bounds register-to-general set (indicating that the CPU should include the MPX registers as part of a context save and restore).

Enabling and Disabling Functions. We also provide a way of enabling and disabling MPX operations within both kernel mode and user mode applications. This can be done by setting flags on the %BNDCFGS and %BNDCFGU registers respectively. %BNDCFGx[0] enables interpretation of the MPX instruction extension, and %BNDCFGx[1] enables bounds register preservation when legacy instructions are encountered. Before these flags are set, we perform a system readiness check. Unlike the GCC runtime, we do not set %BNDCFGx[63:12] with the base address of the bounds table. This minimizes startup overhead, and also provides a small measure of security since attempting to access the bounds table as a means of leaking the contents of a bounds register will result in a segmentation fault.


```c
#include <sys/stat.h>
#include "simplex.h"

-static LBM_GridPtr srcGrid, dstGrid;

void MAIN_initialize( const MAIN_Param* param ) {
    process_specific_init();
    - LBM_allocateGrid( (double**) &srcGrid );
    - LBM_allocateGrid( (double**) &dstGrid );
    double* ptr;
    - LBM_allocateGrid(&ptr);
    + qsetbndl(BND0, (uint64_t) ptr);
    + ptr = 0;
    + LBM_allocateGrid(&ptr);
    + qsetbndl(BND1, (uint64_t) ptr);
    + ptr = 0;
    - LBM_initializeGrid( &srcGrid );
    - LBM_initializeGrid( &dstGrid );
    + LBM_initializeGrid( ((LBM_GridPtr)qgetbndl(BND0)) );
    + LBM_initializeGrid( ((LBM_GridPtr)qgetbndl(BND1)) );
}

void MAIN_finalize( const MAIN_Param* param ) {
    - LBM_freeGrid( (double**) &srcGrid );
    - LBM_freeGrid( (double**) &dstGrid );
    + double* pl = (double*) qgetbndl(BND0);
    + double* pl = (double*) qgetbndl(BND1);
    + LBM_freeGrid(&pl);
    + pl = 0;
    + LBM_freeGrid(&pl);
    + pl = 0;
    + process_specific_finish();
}
```

Figure 2: A diff file example of modifications needed to store global pointers in bounds registers from the lbm benchmark. In this example, the global pointers `srcGrid` and `dstGrid` are placed in `BND0` and `BND1` respectively.

4.2 Security Impact of the Simplex Implementation

Canella et al. recently reported a variety of Meltdown transient execution attacks, one of which is the Meltdown-BR (Bounds Check Bypass) attack [7, 20]. Dekel also describes a post-exploitation technique called BoundHook, which allows an attacker to cause a bounds check exception in a user-mode context, then catch the exception to gain control over the thread execution [10]. With both of these vulnerabilities, Simplex does not increase a program’s attack surface because both require a BR exception to be raised in order to initiate exploitation. Since Simplex does not use the `bndl1`, `bndcu`, or `bndcn` instructions, no such exception will be raised by our code. Additionally, because BoundHook requires that the attacker has also already compromised machine administrator rights, any attacker who can successfully execute a BoundHook intrusion can simply observe and modify the MPX context without the need to further compromise Simplex.

Because Simplex can be used in multi-threaded applications, we must address the dangers that an attacker-controlled thread could victimize a thread using Simplex to interact with the MPX bounds registers. There is a short time window where data being loaded from the bounds register to a system register is spilled onto the stack. We provide one mitigation in that Simplex will zero out the memory used by the `bndmov` spill instruction immediately after copying to the destination register in all accessor functions except for `qgetbndl()` which is performance- rather than security-optimized. Because this zeroing is not guaranteed to be atomic, there is still a small risk that the attacker-controlled thread with a pointer to the bottom of the victim thread’s stack could read this memory in a race condition assisted by a scheduler interrupt sometime between the spill from the bounds register to the time the stack memory is sanitized. We instrumented our library using a PAPI API [4] software defined event to measure the frequency of context switches within the Simplex accessor functions and discovered that such a sequence of events did not occur. We hypothesize that this is because the accessor functions do not require any system calls and are very short-lived, and thus unlikely to trigger the scheduler’s watchdog timer.

5 Evaluation

We conducted our evaluation on an 8-core Intel Core i7-7700K CPU at 4.20 GHz with 62.8 GiB RAM running Ubuntu 20.04 LTS and the Linux 5.4 kernel. The system under evaluation conforms to POSIX.1-2017, and uses GNU libc and POSIX thread implementation version 2.27.

5.1 Benchmarks

We authored three benchmark fixtures to evaluate whether Simplex attains performance that is comparable to using general purpose registers.

5.1.1 Load-Store Benchmark. First, we authored a micro-benchmark that tests load and store performance when Simplex employs the `bndl0` MPX bounds register compared to handwritten assembly using general purpose registers using `movl`, segmentation registers using `gs:0`, and the MMX and XMM instruction set extension registers using `%mm0` and `%mm1` respectively, see Figure 3. We find that the mean of writing to the MPX bounds registers is comparable to writing to the general purpose registers (1.00x), segmentation registers (0.91x), and MMX registers (0.98x). This is because all four of these operations have a fast, dedicated assembly instruction for writing to the register - either `mov` or `bndmk`. The fastest assembly instruction option for writing to the XMM registers is `movaps`, which moves four aligned, packed, single-precision floating point values to the XMM register. However, it incurs significant overhead compared to the `mov` instruction because of microarchitectural limitations and thus the rate of MPX bounds register writes is 13.90x faster.

Loading from the MPX bounds registers is a different story. Additional benchmark results because the MPX extension does not contain an instruction to move from a bounds register directly to another

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This page contains code examples and documentation for Simplex, a library that leverages Intel MPX for secure data movement. The code snippet demonstrates how to allocate and initialize memory grids using the Simplex API, as well as how to access these grids using accessor functions. The section on security impact details vulnerabilities such as Meltdown and BoundHook, and discusses how Simplex mitigates these risks. The evaluation section outlines the methods used to compare Simplex's performance against general purpose registers and other instruction sets.
register, whether a bounds register or otherwise; bndmov only provides a bounds register to memory spill operation. Therefore load operations from a bounds register require that the data is first spilled to the quadword above the stack pointer through a bndmov instruction, then recovered through two additional mov instructions. General purpose register, segmentation register and MMX register loads can all be accomplished by a single mov instruction and thus MPX bounds register loads are only 0.74x, 0.32x, and 0.73x as fast, respectively. Segmentation register loads are particularly fast when repeatedly executed because of cache effects. Conversely, MPX bounds register loads are 1.69x faster than XMM register loads because these loads also must spill to stack, and because of the aforementioned micro-architectural limitations of the apsmov instruction.

Our findings also confirm the micro-architectural analysis of Oleksenko et al. [25] which found that it was not necessarily the MPX bounds operations that were particularly expensive, but the management of the bounds table through a two-level table lookup – particularly the bndstx and bndldx instructions. Simplex uses neither of these instructions and thus avoids their overhead.

5.1.2 Traversal Benchmark. We authored a benchmark simulating unhiding information from two hidden buffers by combining their contents, as first suggested by Shamir [32]. In our benchmark, a buffer is split into two halves, with two registers dedicated to pointing at the half-buffers. These pointers are repeatedly indexed and de-referenced to traverse the buffer, which ranges in size from 4 KiB to 16 MiB (chosen to reflect common page sizes for target operating systems and the x86-64 ISA). We repeat this unhiding traversal for 100 runs of 1000 iterations, and measure an elapsed time for all iterations to determine a geometric mean in order to calculate a performance overhead. Because this requires two load operations from a register for each byte unhidden, performance overhead rapidly accumulates, in this case between 272.45% and 282.17% depending on buffer size. See Table 4 for full results.

| Size  | General Purpose | Simplex | Overhead |
|-------|----------------|---------|----------|
|       | X              | Med     | X        | Med       |
| 4K    | 1.1            | 1.0     | 3.9      | 3.9       |
| 8K    | 2.1            | 2.1     | 7.8      | 7.8       |
| 1M    | 266.5          | 265.9   | 1018.3   | 1018.1    |
| 16M   | 4277.3         | 4274.5  | 16335.7  | 16334.1   |

Table 4: Performance overhead incurred during a simulation of traversing two buffers and combining their values to decode an information-hidden buffer (as in Shamir’s secret hiding scheme). Each experiment is run on four buffer sizes for 1000 iterations and measured for elapsed time. Buffer size is expressed in bytes, measurements are expressed in seconds, and overhead in percentage. X = Mean, Med = Median.

5.1.3 String Operations. Third, we implemented five memory operations from the string.h header, using reference implementations from the libgcc codebase. We then reimplemented these functions for Simplex to replace any passed argument that contains the address of a buffer with calls to instead load the address from an applicable bounds register. These benchmarks show that the performance cost of Simplex is easily amortized, as we found that the maximum overhead was only 5.86%, and a 0.69% overall geometric mean. In the specific case of these function implementations, benchmarks that do not short-circuit (i.e. memcmp, memmove and memset) are able to amortize the cost fully compared to functions that do short-circuit (i.e. memcmp, memchr). We do not claim that there is a performance benefit to Simplex, simply that if there is a performance cost, it is small enough to be unnoticeable to the user and that it is offset by the utility of the additional registers provided by Simplex.

5.2 Modifications to Existing Codebases
5.2.1 SPEC CPU2017. We hand-modified two SPEC CPU2017 benchmarks, 519.1bm which simulates fluid flow through lattices, and 531. deepsjeng which plays chess. In both cases, we selected the two global pointers to data structures that had the highest number of uses in order to fully stress the Simplex library. Although we selected global objects, it should be emphasized that Simplex is not limited to just globals; heap or local objects could also be placed in the bounds registers. Using the SPEC benchmarks proves both correctness – the output is verified against a known correct output – and demonstrates performance cost of using Simplex. We measured the performance rate ratio between runs with an unmodified benchmark and one where frequently used pointers to global variables were placed into a bounds register. This performance ratio was between 1.000 and 1.006 for 519.1bm, and 0.975 and 0.985 for 531.1bm (see Table 5). Higher performance rate ratios indicate faster execution, but differ from performance overhead measurements since performance rate takes into account the number of threaded copies running simultaneously.

5.2.2 OpenSSL. We then modified the OpenSSL Blowfish symmetric key cipher to demonstrate how Simplex might be used in a security application. In our modified Blowfish cipher, the address of the cipher’s global key schedule structure is stored in a bounds register. Therefore wherever an encryption or decryption function would ordinarily receive a pointer to the key schedule as a function parameter, we instead pass a null value as the parameter and thus de-reference the bounds register at each usage of the parameter. Although the OpenSSL test suite provides test run time in its output, the Blowfish correctness test is very short in duration. As a result, our observed runtime overheads are smaller than the reported measurement resolution and not particularly useful as a metric of performance. We do not wish to imply that replacing function parameters with Simplex function calls is a way to achieve higher performance, only to state that Simplex presents minimal performance cost. We also wish to emphasize that although we placed a pointer to a key schedule structure in the bounds registers for this evaluation, this structure is stored on the heap in the unmodified Blowfish cipher and therefore we did not introduce attack surface in our modified cipher. Additionally, some other OpenSSL ciphers’ keys are less than 512 bits in size and would fit entirely within the bounds registers. The MPX bounds registers can hold any value, not just pointer values.
Figure 3: Rate of load and store operations. Box and whisker plot shows median, minimum/maximum, and first/third quartile operation rates. We use %r15 for **General**, %gs:0 for **Segmentation**, %mm0 for **MMX**, %xmm1 for **XMM** and %bnd0 for **MPX**. The test consisted of $10^4$ runs, with $10^6$ iterations per run. We report the steady-state rate of operations accomplished per second.

| Variables in Bounds Register | Copies | **Run Time** | **Base Rate** | **Ratio** |
|-----------------------------|--------|--------------|---------------|-----------|
| 519.lbm_r                   |        |              |               |           |
| None                        | 1      | 202          | 5.21          |           |
| None                        | 4      | 605          | 6.96          |           |
| srcGrid → bnd0              | 1      | 201          | 5.24          | 1.006     |
| srcGrid → bnd0              | 4      | 605          | 6.96          | 1.000     |
| srcGrid → bnd0, dstGrid → bnd1 | 1     | 202          | 5.23          | 1.004     |
| srcGrid → bnd0, dstGrid → bnd1 | 4     | 606          | 6.96          | 1.000     |
| 531.deepsjeng_r             |        |              |               |           |
| None                        | 1      | 283          | 4.04          |           |
| None                        | 4      | 290          | 15.8          |           |
| state → bnd0, gamestate → bnd1 | 1     | 288          | 3.98          | 0.985     |
| state → bnd0, gamestate → bnd1 | 4     | 297          | 15.4          | 0.975     |

Table 5: **Simplex** SPEC CPU2017 evaluation data. **Run time** refers to how long the benchmark took to complete. **Base Rate** refers to the raw performance of this benchmark relative to the SPEC CPU2017 reference machine and thus provides insight into the underlying system under test. **Ratio** refers to the ratio of the modified benchmark’s performance to the unmodified benchmark’s performance taking into account the number of copies running on a multi-threaded system. **Ratio** < 1 implies the modified benchmark ran slower than the unmodified benchmark.

5.2.3 **DPlus**. Finally, we modified DPlus, a simple web browser written entirely in pure C++. The choice of implementation language is critical since **Simplex** is not compatible with interpreted languages like Javascript, and the majority of modern browsers implement at least some portion of the code in Javascript for compatibility with popular web toolkits. We verified correctness using the DW window toolkit’s native functionality tests.

6 RELATED WORK

**Existing Evaluations.** Significant exploration of Intel MPX generally find MPX to be flawed as a memory safety tool, and thus inspired our investigation as to whether MPX could be repurposed. Serebryany unfavorably evaluated the performance of Intel MPX versus the Address Sanitizer memory safety tool. [31] Notably, he discovered not only up to a 2.5x performance slowdown and 4.0x memory overhead on some benchmarks, but that the MPX instructions still exhibit a 50% slowdown even when they should be ignored on a system which does not have MPX support or has disabled it. He also identifies three categories of false positives that Address Sanitizer does not have: atomic pointers, un-instrumented bounds changes, and those caused by compiler optimizations after instrumentation. Otterstad examined the effectiveness of early implementations of MPX, identifying eight new categories of false positives and false negatives beyond those explored by Serebryany. [27] Furthermore, he demonstrates at least one toy program which can be victimized by ROP attacks because of these false positives and false negatives. Oleksenko et al. performed a study of the performance, security guarantees, and usability issues of MPX after it became available in production hardware. [25] Furthermore, their empirical study was backed by an exhaustive investigation of how MPX is
We note that Simplex when modified to pass pointer arguments in bounds registers as with hardware levels. This investigation is used to support their quantitative findings.

Other Uses of Intel MPX. We are not the only members of the community to propose repurposing MPX. Code Pointer Integrity (CPI) maintains a safe region to protect function pointers, return addresses and other pointers to code called a “safe stack”. [19] The authors propose one implementation of CPI using MPX to store the safe region’s metadata, gaining performance benefits by moving some of the implementation into MPX’s hardware accelerated checks. Burow further investigates using MPX to isolate CPI’s shadow stacks and provide a highly-efficient implementation. [6] We note that Simplex performs much of the management functionality they described, and could be used in conjunction with their defenses. Opaque Control-Flow Integrity (O-CFI) combines fine-grained code layout randomization with coarse-grained CFI in order to defeat sophisticated attacks seeking in-memory layout information to launch code-reuse attacks. [22] O-CFI uses MPX instructions to perform branch instrumentation, where legal branch targets are “chunked” together into a minimal address range, similar to a buffer. Oleksenko proposes a system combining MPX for hardware fault detection with Intel Transactional Synchronization Extensions (TSX) for fault rollback. [26] The underlying principle is that if a pointer’s value is corrupted by a fault, then it will likely point to a dramatically different address outside the bounds of the referent object. MemSentry is a deterministic memory isolation framework addressing the threats of allocation oracles, thread spraying, crash-resistant memory disclosure primitives, and various side channels. [18] The authors use MPX and Intel Memory Protection Keys (MPK) to describe a more efficient method of intra-process isolation, similar to that provided by the kernel through mprotect and Software Fault Isolation (SFI). CFIXX is a C++ defense for virtual table pointers providing Object Type Integrity (OTI). [6] CFIXX protects against corruption attacks against OTI by protecting the memory region containing the OTI metadata with selective MPX instrumentation. By reimagining the layout of the address space, they are able to halve the number of bound checks compared to a full memory safety solution provided by MPX. BOGO extends the MPX bounds tables to not only provide spatial memory safety, but also temporal memory safety. [35] Since MPX already initializes bounds table entries at allocation, BOGO additionally invalidates these entries upon deallocation and thus gains temporal memory safety. Since doing this operation at every deallocation can be expensive, the authors also introduce more efficient techniques for managing the deallocation metadata updates and for scanning the bounds table. DataShield provides three methods for coarse-grained bounds checks for non-sensitive pointer dereferences, one of which utilizes MPX to avoid the need to information hide the non-sensitive data regions. [8] Up to four of these regions’ addresses are initialized in the MPX bounds register at program startup, with each pointer dereference in order to assure that the pointer does not escape the non-sensitive region. The Linux kernel can be protected against Just-in-Time code reuse attacks by kR®X, which hardens benign read operations that an attacker might reuse to disclose code to find useful JIT gadgets. [28] Intel MPX is used in one implementation of kR®X to accelerate the execute-only range checks to reduce the performance overhead.

Repurposing Hardware Registers. The idea of repurposing hardware registers as with Simplex is not unique. TRESOR is a patch that implements the AES encryption algorithm for the Linux kernel, but provides additional security by utilizing the Intel AES-NI instruction set extension and by keeping encryption keys instead of in RAM. [23] Ginseng keeps secrets in an encrypted secure stack until they are needed, then moves the secret into dedicated registers. [33] This has the effect of reducing the amount of sensitive data kept in the ARM TrustZone Trusted Execution Environment (TEE) and thus reduces the TEE’s attack surface and does not require placing the operating system within the trusted computing base.

7 CONCLUSION

Simplex is an open-source library repurposing the Intel®MPX instruction set (ISA) extension. We present evidence that suggests that MPX is ubiquitous, and show that MPX bounds registers can be repurposed as general purpose storage. In particular, they can be used to hide security sensitive data. We demonstrate that although the MPX ISA lacks a dedicated instruction to move data directly to and from the bounds registers, it is still possible to do so through the available spill and fill instructions, bndmk and bndmov. Furthermore, we show that such operations are not overly-burdensome,
especially once the operations are amortized across the entire execution of a program. We do this through a collection of refactored programs and a partial implementation of the C standard library.

8 AVAILABILITY
We make SIMPLEX available to the community as open-source software at https://github.com/bingseclab/simplex.

REFERENCES
[1] 2019. Control-flow Enforcement Technology Specification. https://software.intel.com/sites/default/files/managed/4d/2a/control-flow-enforcement-technology-preview.pdf publisher: Intel Corporation.
[2] 2019. PassMark CPU Benchmarks - AMD vs Intel Market Share. https://www.cpubenchmark.net/market_share.html
[3] 2019. Steam Hardware & Software Survey. https://store.steampowered.com/handbook/processor/
[4] S. Browne, J. Dongarra, N. Garner, K. London, and P. Mucci. 2000. A Scalable Cross-Platform Infrastructure for Application Performance Tuning Using Hardware Counters. In SC ’00: Proceedings of the 2000 ACM/IEEE Conference on Supercomputing. https://doi.org/10.1145/300100.3001029
[5] Derek Bruening, Evelyn Duesterwald, and Saman Amarasinghe. 2000. Design and Implementation of a Dynamic Optimization Framework for Windows. In 4th ACM Workshop on Feedback-Directed and Dynamic Optimization (FDDO-4).
[6] Nathan Burrow, Derrick Mckee, Scott A. Carr, and Mathias Payer. 2018. CFIXX: Object Type Integrity for C++. In Network and Distributed Systems Security Symposium 2018. https://doi.org/10.14722/ndss.2018.23279
[7] Claudio Canella, Jo Van Bulck, Michael Schwarz, Moritz Lipp, Benjamin von Berg, Philipp Ottmer, Frank Piessens, Dmitriy Evtushikin, and Daniel Gruss. 2018. A Systematic Evaluation of Transient Execution Attacks and Defenses. (2018). arXiv:1811.05441 [cs.CR]
[8] Scott A. Carr and Mathias Payer. 2017. DataShield: Configurable Data Confidentiality and Integrity. In Proceedings of the 2017 ACM on Asia Conference on Computer and Communications Security - ASIA CCS ’17. https://doi.org/10.1145/3072973.3052983
[9] Lucas Davi, Christopher Liebenich, Ahmad-Reza Sadeghi, Kevin Z Snow, and Fabian Monroe. 2015. Isomeron: Code Randomization Resilient to (Just-In-Time) Return-Oriented Programming. https://doi.org/10.1145/2738920.2741726
[10] Kasif Dekel. [n.d.]. BoundHook: Exception Based, Kernel-Controlled User-Mode Hooking. https://cyberark.com/threat-research-blog/boundhook/exception-based-kernel-controlled-usermode-hooking/
[11] I Evans, S Fingeret, J Gonzalez, U Ogotnaaat, T Tang, H Shrode, S Sadeghloosousi, M Rinaud, and H Okhravi. 2015. Missing the Pointer?: On the Effectiveness of Code Pointer Integrity. In 2015 IEEE Symposium on Security and Privacy. 781–796. https://doi.org/10.1109/SP.2015.53
[12] Amy Ann Forri and Rob van der Meulen. [n.d.]. Gartner Says PC Leaders Must Overhaul Their Businesses or Leave the Market by 2020. https://www.gartner.com/newsroom/press-releases/2016-04-19-gartner-says-pc-leaders-must-overhaul-their-businesses-or-leave-the-market-by-2020
[13] Kittur Ganesh. 2012. Pointer Checker: Easily Catch Out-of-Bounds Memory Accesses. https://software.intel.com/sites/products/parallelmag/singlearticles/issue11/7080_2_IN_ParallelMag_Issue11_Pointer_Checker.pdf
[14] Enes Göktas, Robert Gawlik, Benjamin Kollenda, Elias Athanasopoulos, Georgios Portokalidis, Cristiano Giuffrida, and Herbert Bos. 2016. Undermining Information Hiding (and What to Do about It). In Proceedings of the 25th USENIX Conference on Security. 105–119.
[15] Daniel Gruss, Moritz Lipp, Michael Schwarz, Richard Fellner, Clementine Maurice, and Stefan Mangard. 2017. KASLR is Dead: Long Live KASLR. In Engineering Secure Software and Systems. 161–176. https://doi.org/10.1007/978-3-319-62105-0_11
[16] Ingebor. [n.d.]. Mandibory Project. May 2019. https://ingemur.ca/a/beU5HR/HRKSSAP
[17] Khaveen Jeyaratnam. 2019. Intel vs. AMD: Battle for Market Share. https://seekingalpha.com/article/4247790-intel-vs-amd-battle-market-share
[18] Koen Koning, Xi Chen, Herbert Bos, Cristiano Giuffrida, and Elias Athanasopoulos. 2017. No Need to Hide: Protecting Safe Regions on Commodity Hardware. In Proceedings of the Twelfth European Conference on Computer Systems. 437–452. https://doi.org/10.1145/3064176.3064217
[19] Volodymyr Kuznetsov, Laszlo Szekeres, Mathias Payer, George Candea, R Sekar, and Dawn Song. 2014. Code-pointer Integrity. 147–163 pages.
[20] Moritz Lipp, Michael Schwarz, Daniel Gruss, Thomas Pescher, Werner Haas, Anders Fogh, Jann Horn, Stefan Mangard, Paul Kocher, Daniel Genkin, Yuval Yarom, and Mike Hamburg. 2018. Meldtown: Reading Kernel Memory from User Space. In 27th USENIX Security Symposium. 973–990.
[21] Kangjie Lu, Chengyu Song, Byongyoungh Lee, Simon P. Chung, Taesoo Kim, and Wenke Lee. 2015. ASLR-Guard: Stopping Address Space Leakage for Code Reuse Attacks. In Proceedings of the 22nd ACM SIGSAC Conference on Computer and Communications Security. 2804-2810. https://doi.org/10.1145/2810103.2813604
[22] Vishwath Mohan, Per Larsen, Stefan Brunthaler, Kevin W Hamlen, and Michael Franz. 2015. Opaque Control-Flow Integrity. In Network and Distributed Systems Security Symposium 2015. https://doi.org/10.14722/ndss.2015.23271
[23] Tilo Müller, Felix C. Freiling, and Andreas Diewald. 2011. TRESOR Runs Encryption Securely Outside RAM. In Proceedings of the 20th USENIX Conference on Security (SEC’11). https://doi.org/10.5555/2028067.2028084
[24] Angelos Oikonomopoulos, Elias Athanasopoulos, Herbert Bos, and Cristiano Giuffrida. 2016. Poking Holes in Information Hiding. In 25th USENIX Security Symposium. Austin, TX, 121–138.
[25] Oleksii Oleksenko, Dmitriy Kuvaiskii, Pramod Bhatotia, Pascal Felber, and Christof Fetzer. 2017. Intel MPX Explained. An Empirical Study of Intel MPX and Software-based Bounds Checking Approaches. (2017). arXiv:1706.00719 [cs.CR]
[26] Oleksii Oleksenko, Dmitriy Kuvaiskii, Pramod Bhatotia, Christof Fetzer, and Pascal Felber. 2016. Efficient Fault Tolerance using Intel MPX and TSX. In Fast Abstract in the 46th Annual IEEE/IFIP International Conference on Dependable Systems and Networks. Toulouse, France.
[27] Christian W Otterstad. 2015. A Brief Evaluation of Intel MPX. In 2015 Annual IEEE Systems Conference Proceedings. IEEE, 1–7. https://doi.org/10.1109/SYSCON.2015.7116720
[28] Marios Ponomis, Theofilos Pitasios, Angelos D Komeritis, Michalalis Poleychronakis, and Vasileios P Kemerlis. 2017. KR’X: Comprehensive Kernel Protection Against Just-In-Time Code Reuse. In Proceedings of the Twelfth European Conference on Computer Systems (EuroSys ’17). https://doi.org/10.1145/3064176.3064216
[29] Sundaram Ramakasan and Juan Rodriguez. 2016. Intel® Memory Protection Extensions Enabling Guide. https://software.intel.com/en-us/articles/intel-memory-protection-extensions-enabling-guide
[30] RB (Intel). [n.d.]. Introduction to Intel Memory Protection Extensions. https://software.intel.com/en-us/articles/introduction-to-intel-memory-protection-extensions
[31] Kostya Serebryany. [n.d.]. Address Sanitizer Intel Memory Protection Extensions. https://github.com/google/sanitizers/wiki/AddressSanitizerIntelMemoryProtectionExtensions
[32] Adi Shamir. 1979. How to Share a Secret. Commun. ACM 22, 11 (Nov. 1979), 622–631. https://doi.org/10.1145/359168.359176
[33] Min Hong Yun and Lin Zhong. 2019. Ginseng: Keeping Secrets in Registers When You Disturb the Operating System. In Network and Distributed Systems Security Symposium 2019. 15. https://doi.org/10.14722/ndss.2019.23327
[34] Mingwei Zhang and R Sekar. 2015. Control Flow and Code Integrity for COTS Binaries: An Effective Defense Against Real-World ROP Attacks. In Proceedings of the 31st Annual Computer Security Applications Conference. 91–100. https://doi.org/10.1145/2818000.2818016
[35] Tong Zhang, Dongyoon Lee, and Changlee Jung. 2019. BOGO: Buy Spatial Memory Safety, Get Temporal Memory Safety (Almost) Free. 631–644. https://doi.org/10.1145/3297858.3304017