UTANGO: an open-source TEE for the Internet of Things

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Abstract—Security is one of the main challenges of the Internet of Things (IoT). IoT devices are mainly powered by low-cost microcontrollers (MCUs) that typically lack basic hardware security mechanisms to separate security-critical applications from less critical components. Recently, Arm has started to release Cortex-M MCUs enhanced with TrustZone technology (i.e., TrustZone-M), a system-wide security solution aiming at providing robust protection for IoT devices. Trusted Execution Environments (TEEs) relying on TrustZone hardware have been perceived as safe havens for securing mobile devices. However, for the past few years, considerable effort has gone into unveiling hundreds of vulnerabilities and proposing a collection of relevant defense techniques to address several issues. While new TEE solutions built on TrustZone-M start flourishing, the lessons gathered from the research community appear to be falling short, as these new systems are trappng intto the déjá vu pitfalls of the past. In this paper, we present UTANGO, the first multi-world TEE for modern IoT devices. UTANGO proposes a novel architecture aiming at tackling the major architectural deficiencies currently affecting TrustZone(-M)-assisted TEEs. In particular, we leverage the very same TrustZone hardware primitives used by dual-world implementations to create multiple, equally-secure execution environments within the normal world. We demonstrate the benefits of UTANGO by conducting an extensive evaluation on a real TrustZone-M hardware platform, i.e., Arm Musca-B1. UTANGO will be open-sourced and freely available on GitHub in hopes of engaging academia and industry on securing the foreseeable trillion IoT devices.

Index Terms—Trusted Execution Environment, TrustZone, TEE, separation, isolation, IoT, Arm.

I. INTRODUCTION

With the increasing complexity of Internet of Things (IoT) devices and the door left open by Internet connectivity to hackers and attackers, developing secure IoT devices is becoming increasingly challenging [1]–[3]. Complex functional requirements are met by integrating multiple codebases, drivers, and libraries from different 3rd party entities with different assurance levels. The problem is exacerbated by the lack of simple and reliable mechanisms to enforce separation among these multi-source and mixed-criticality components [4]–[6].

In the context of secure computing systems, security through separation is a well-established principle implemented by microkernels, hypervisors, and Trusted Execution Environments (TEEs) [7]–[23]. In particular, billions of mobile devices worldwide rely on TEEs leveraging TrustZone hardware primitives for the protection of security-critical applications (e.g., digital rights management, fingerprints, and keys) [11], [14], [15], [18], [19], [24]–[25]. TrustZone enables the partition of system resources into two domains: the secure world for secrets and critical functionality, and the normal world for everything else, including the rich operating system (OS) and its applications. Within the realm of the IoT, Arm has adapted TrustZone technology for the Cortex-M family, introducing TrustZone-M into new Armv8-M MCUs, e.g., Cortex-M33 [6], [27], [28].

Problem and Motivation. TrustZone-assisted TEEs are assumed to be highly secure. However, over the past years, TrustZone-assisted TEEs have been attacked hundreds of times [19], [29]–[34]. A recent study performed on five major commercial TrustZone-assisted TEEs (i.e., Qualcomm, Trustonic, Huawei, Nvidia, and Linaro) has identified that TrustZone-assisted TEEs have several architectural deficiencies, critical implementation bugs, and overlooked hardware properties [34]. From these three classes of problems, the architectural issues have the largest share. Among the identified deficiencies, we highlight (i) the excessively large trusted computing base (TCB), e.g., QSEE has 1.6 MiB, (ii) the large number of interfaces, e.g., QSEE has 69 syscalls, (iii) the existence of several privileged secure kernel drivers, and (iv) the asymmetrical isolation between the worlds, e.g., trusted applications can map normal world memory [34]. Furthermore, the majority of the implementation issues could be mitigated with adequate architectural mechanisms [34].

In general, although these problems have mainly affected commercial implementations targeting Cortex-A processors, new TEE solutions built on TrustZone-M MCUs are falling in the same pitfalls of the past. The Arm Trusted Firmware-M (ATF-M) [35] implementst a large number of kernel components and security services within the secure world, and existing memory protection mechanisms (i.e., secure MPU) are configured with too coarse-grained regions. As a result, ATF-M has a TCB with hundreds of KiloBytes (150+ KiB). The Kinibi-M was adapted from the original Kinibi TEE for mobiles and not re-invented for the IoT [36]. And lastly, Arm is currently spreading an ambiguous message with regard to what should be deployed within the secure world. Multiple official Arm TrustZone-M documents [37]–[39] suggest different approaches. In particular, in Ref. [37], for an IoT application targeting a wireless communication interface, Arm suggests including (i) the secure boot, (ii) the communication stack, (iii) device drivers, (iv) OS kernel, and (v) firmware update within the secure world and a single communication buffer on the normal world.

Thus, we argue that the current dual-world model is falling...
short to address the increasing complexity and requirements of modern IoT devices, as the number of functional blocks expected to be consolidated largely exceeds two. We believe that a novel multi-world architecture, enabling execution of multiple environments within strongly isolated compartments would provide higher flexibility and increasing security guarantees in the context of the IoT.

**Contributions.** In this paper, we present uTANGO, an open-source TEE for the IoT that aims at tackling the main architectural deficiencies that currently affects TrustZone(-M)-assisted TEEs. To do so, uTANGO proposes a novel TEE architecture that leverages the very same TrustZone-M hardware primitives used by dual-world implementations to provide multiple equally-secure execution environments and augmented TEE capabilities (e.g., SGX-like enclaves, availability guarantees). To the best of our knowledge, uTANGO is the first multi-world TEE for TrustZone-M MCUs. To create an unlimited number of virtual worlds, uTANGO leverages the dynamic reconfiguration capabilities of TrustZone-M controllers. Each controller is dynamically programmed to partition system resources according to each execution environment memory, devices, and interrupts assignments.

The design follows three main principles: (i) principle of minimal implementation, by providing a minimal and clean slate implementation, with a small number of well-defined interfaces, thereby drastically reducing the overall system TCB; (ii) principle of least privilege, by ensuring that uTANGO, as the highest privilege entity, is the single component running within the secure world; (iii) and principle of containment, by enforcing that each functional block executes on its isolated execution domain, which inherently prevents lateral movement and privilege escalation. The proof-of-concept implementation leverages best-in-class techniques to minimize performance penalties and to make the TEE suitable for formal verification. The evaluation conducted on the Arm Musca-B1 shows that uTANGO has a minimal impact on the performance and the TCB of the system is an order of magnitude smaller than alternative solutions.

To summarize, our main contributions are as follows:

1) We present the design of uTANGO as a novel TEE architecture leveraging TrustZone-M hardware primitives to provide an unlimited number of equally-secure execution environments (Section III).

2) We provide a proof-of-concept implementation of uTANGO targeting the first public available TrustZone-M platform, i.e., Arm Musca-B1 (Section IV), and we have also developed a Reference IoT Application. All software components will be open-sourced and available on GitHub.

3) We perform a comprehensive security analysis and discuss how uTANGO can mitigate potential attack vectors that a malicious adversary may explore (Section V).

4) We extensively evaluate uTANGO focusing on security metrics, performance, interrupt latency, and TCB size and complexity (Section VI).

**II. BACKGROUND**

**A. Arm TrustZone-M**

Arm TrustZone follows a system-wide approach to security, providing hardware-enforced protection mechanisms at the CPU and System-on-Chip (SoC) level [19]. This technology is centered around the concept of protection domains named secure world and normal world. TrustZone was firstly introduced into Arm application processors (Cortex-A) in 2004, achieving mainstream adoption in the mobile industry. In 2016, Arm decided to span TrustZone for the new generation of Arm MCUs, i.e., Armv8-M (e.g., Cortex-M23, Cortex-M33), naming this new version of the technology as TrustZone-M. From a high-level perspective, both technologies follow the same dual-world architecture. However, at the low-level, there are significant differences, mainly because TrustZone-M is entirely optimized for low-end devices (e.g., deterministic behavior, low overhead, and low-power consumption) [37].

**Programming Model.** Armv7-M MCUs provide two operation modes: thread and handler mode. In thread mode, the processor executes application code, which can be either privileged or unprivileged. In handler mode, the processor executes exception handler code, which is always privileged. In (Armv8-M) TrustZone-enabled MCUs, these operation modes are orthogonal to the two security states, i.e., there is both a thread and handler mode for each security state. The security state does not depend on a specific security bit, but the division is memory map based. This means that, when the code is running from the secure memory, the processor state is secure, and, when the code runs from non-secure memory, the processor state is non-secure. Transitions between the two worlds are supported by three new instructions: branch with exchange to non-secure state (BXNS), secure gateway (SG), and branch with link and exchange to non-secure state (BLXNS). Calling non-secure software from the secure state is possible by performing a BLXNS instruction. In contrast, non-secure software cannot directly call secure software. Instead, non-secure software must use indirect entry points located in a Non-Secure Callable (NSC) memory region. The first instruction of any entry point must be an SG, which marks a valid branch to secure code. After the secure function completes, a BXNS instruction issues a return to the non-secure software. Furthermore, state transitions can also happen due to exceptions or interrupts.

**Resources Partitioning.** In Armv8-M MCUs, the memory space is partitioned through the so-called Attribution Units. The Security Attribution Unit (SAU) is always available and provides dynamic address partitioning. The number of regions is defined by the chip designer, which is typically 8. The SAU is programmable in secure state. The Implementation-Defined Attribution Unit (IDAU) is external to the core, and it is implementation-defined. The IDAU provides static address partitioning and supports up to 256 non-programmable regions. The configuration of the memory region’s security state results from the logical OR operation between the SAU and IDAU. Memory can also have a set of privilege permissions, which are defined by a TrustZone-aware Memory
Protection Unit (MPU). MPUs are banked among worlds; however, MPUs are optional and implementation-defined. Additionally to the attribution units, other components, referred to as security gates, ensure the overall system’s security. Besides the CPU, additional bus masters within the SoC are connected to the bus (e.g., DMA controllers, crypto engines). TrustZone-enabled MCUs provide security gates, which act as firewalls on TrustZone-oblivious slaves. These components are controlled by a central system security controller, specified by silicon providers.

**Interrupt Handling.** In TrustZone-enabled MCUs interrupts can be set as secure or non-secure by configuring the Interrupt Target Non-secure (ITNS) interface on the Nested Vector Interrupt Control (NVIC). Arm’s M-profile architectures support automatic hardware stacking and un-stacking of some CPU registers during exception entrance to reduce interrupt latency. Armv8-M-based architectures follow the same concept, although with a few differences. If the arriving exception or interrupt has the same state as the current processor state, the exception sequence is almost identical. The main difference occurs when a non-secure interrupt triggers while secure code is executing. To avoid information leakage, the processor automatically pushes all non-banked registers to the secure stack and erases all its contents, which incurs in a slightly longer interrupt latency. The vector table (and exception handlers) are banked between states, i.e., the processor supports two separated exception vector tables. Furthermore, secure and non-secure interrupts can share the same priority level, or secure interrupts can be programmed to have higher priority than non-secure ones (i.e., to avoid denial-of-service attacks).

**B. Arm Trusted Firmware-M**

The Arm Trusted Firmware-M (ATF-M) is an open-source, secure world firmware reference implementation, which offers the foundations of a TEE for Armv8-M MCUs. The ATF-M implements: (i) a secure boot to verify the integrity and authenticity of secure and non-secure binaries; (ii) a core module (i.e., ATF-M Core) that controls the isolation, communication, and execution; and (iii) a set of security services offering secure storage, crypto, and attestation mechanisms. The implementation follows the traditional TrustZone multi-world architecture, i.e., all secure components (e.g., bootloader, kernel modules, secure services, and 3rd party security functions) are encapsulated within the secure world. The solution implements the isolation levels defined in the Platform Security Architecture (PSA) [40], which rely on platform hardware (e.g., SAU, secure MPU) to enforce isolation boundaries. As of this writing, ATF-M only implements isolation levels 1 and 2, which partitions the system into three major domains. Isolation level 1 establishes the two specific security domains enabled by TrustZone (i.e., the secure and non-secure worlds). Isolation level 2 goes a step further and leverages the secure MPU to isolate the ATF-M core and services from 3rd party security services. The latter are expected to be developed by multiple entities, and are not the same services as the ones provided by the ATF (i.e., secure storage, attestation). Isolation level 3 is still under development and will provide fine-grained isolation among different 3rd party security services.

**ATF-M preliminary evaluation.** To understand the ATF-M codebase complexity, we performed a preliminary evaluation with regard to binary size, code size, and security metrics of the ATF-M implementation for two different platforms: Arm Musca-B1 and STM NUCLEO-L552ZE-Q. Table I summarizes the assessed results. The off-the-shelf implementation of the ATF-M for the Arm Musca-B1 has a total size of 50 KiB for the secure bootloader and 250 KiB for the ATF-M core and security services. The implementation has a large code size, encompassing approximately 40 K source lines of code (SLoC). We also evaluated the number of indirect calls and Return-Oriented Programming (ROP) gadgets, which are important security metrics as further explained in Section VI.

We counted a total of 257 indirect calls and 15597 ROP gadgets across the different binaries that comprise the TCB. The numbers for the STM port are a bit better, but in the same order of magnitude, i.e., 192 KiB for the ATF-M core and security services, 33 K SLoC, 9957 ROP gadgets, and 147 indirect calls. In summary, this preliminary evaluation suggests that the same architectural issues highlighted in the literature [34], are being repeated. Furthermore, the formally verified microkernel seL4 [7], which targets high-end Linux-capable platforms endowed with memory management unit (MMU), has a TCB smaller and a codebase simpler [34] than ATF-M, that is expected to run on resource-constrained MCUs.

### Table I: ATF-M TCB size, code size, and security metrics for NUCLEO-L552ZE-Q and Musca-B1 platforms.

|                      | STM32L5   | Musca-B1 |
|----------------------|-----------|----------|
| **Binary Size (KiB)**|           |          |
| bootloader           | 103       | 50       |
| core+services        | 192       | 250      |
| total                | 295       | 300      |
| **Code Size (SLoC)** |           |          |
| total                | 33        | 40       |
| **Security Metrics** |           |          |
| # ROP Gadgets        | 9957      | 15597    |
| # Indirect Calls     | 147       | 257      |

**Fig. 1:** Classic TEE’s dual-world model mapped to uTANGO multi-world architecture.
UTANGO aims at tackling the main architectural deficiencies prevailing on TrustZone-assisted TEE systems [34]. To do so, UTANGO evolves from the classic dual-world security model to a multi-world architecture (Figure 1). The multi-world architecture is based on the zero-trust model, which dictates that every single software component, with exception of the TEE kernel, cannot be trusted. Thus, UTANGO enables the consolidation of multiple applications, services, or workloads (e.g., embedded OSes) on equally secure, isolated domains - called Non-Secure Virtual Worlds (NSVW).

Another particularity of the UTANGO design, is related to the augmentation of the TEE model and capabilities. TrustZone-(M)-assisted TEEs implement remote procedure call (RPC) architectures, i.e., a client-server model mainly used for mobiles. Modern TEEs aim at providing a broader range of features and fulfilling a much large spectrum of use cases and requirements [22], [11]. Thus, UTANGO not only supports the traditional core of the TrustZone design but also provides capabilities similar to SGX-like enclaves [11], [18], [20]. Within the NSVWs, UTANGO runs unmodified binaries, which can be user-space applications, services, and libraries, or privileged OS/RTOS and respective applications. Furthermore, UTANGO goes a step further by providing increasing availability guarantees.

The design of the UTANGO multi-world architecture is centered on three fundamental principles: (i) principle of minimal implementation, (ii) principle of least privilege, and (iii) principle of containment. We comply with these construction principles, and we show that its systematic application results in (i) a reduced TCB and attack surface, (ii) a well-defined layered access control to prevent privilege escalation, and (iii) strong isolation boundaries to restrict workloads access to only their own resources (preventing exploits containment).

**Principle of minimal implementation.** To contain the system’s attack surface, UTANGO must rely on hardware support as much as possible, and provide a minimal and clean implementation of well-defined structures and interfaces. Moreover, UTANGO must de-privilege secure applications/services to the normal world, thus reducing the amount of code to be trusted and deployed on the secure side.

**Principle of least privilege.** To mitigate privilege escalation, UTANGO kernel must be granted the highest privilege of execution while de-privileging secure applications/services to the normal world. Furthermore, each execution domain must only have access to those resources that are absolutely required (e.g., devices, system services).

**Principle of containment.** To limit the extent of an attack, UTANGO must ensure that the multiple execution domains are well-defined and self-contained with clear boundaries. The system must use hardware-enforced mechanisms to sandbox each domain to its own resources (e.g., memory, devices), thereby limiting the reach of an attacker and preventing lateral movement across other system components.

### III. UTANGO Design

#### A. Architecture Overview

Figure 1 depicts, at the top, the traditional dual-world TrustZone-M architecture. At the bottom, it illustrates an example of UTANGO architecture mapping legacy dual-world systems into a multi-world horizontal scheme, where each functional block (i.e., IoT-OS and trusted applications) is assigned to an individual NSVW. Besides, as highlighted in the figure, the UTANGO kernel is the single component running at the most privileged level (i.e., secure handler mode), while all NSVWs run in the non-secure state. Following the aforementioned design principles, UTANGO must strive for a clean-slate minimal implementation. Thereby, as depicted in Figure 1 the UTANGO is built around three components: (i) the system partitioner (SP), (ii) the worlds scheduler (WS), and (iii) the worlds’ communication channel (WCC). The SP relies on a configuration file detailing the overall system configuration and partition.

**System Configuration.** The first piece of UTANGO workflow starts with a configuration file (CFG file in Figure 1) that defines the properties of each NSVW. These properties encompass memory regions (e.g., code, data), devices (e.g., serial peripherals, timers), and interrupts assigned to each NSVW, as well as the overall system time quantum.

**System Partitioner.** According to the system configuration, the SP is responsible for statically partitioning the platform resources at boot-time. The SP leverages the SAU and additional platform-specific bus filters (security gates) to achieve such partitioning. Based on each NSVW configuration, the SP prepares a corresponding SAU configuration and saves it on the world’s control block (WCB). Regarding the security gates, the SP only performs a one-time setup. UTANGO enforces that all accesses and transactions issued by NSVWs to other bus masters are always trapped and mediated. This prevents the reconfiguration of each bus filter during the context switch, avoiding additional performance burdens.

**Worlds Scheduler.** UTANGO enforces temporal separation through the WS. According to the system time quantum, the WS, supported by an architectural timing unit (e.g., Arm SysTick), schedules each NSVW in a round-robin fashion. Every NSVW has a unique WCB data structure for preserving the world state, i.e., CPU register bank, selective System Control Block (SCB) registers, SAU configuration table, and interrupts state. At every scheduling point, the WS performs four main activities: (i) saves the suspended NSVW context to the WCB; (ii) schedules a new NSVW to be resumed; (iii) sets new partition regions on SAU; and (iv) restores the context of the new NSVW. Notice that, while setting a new configuration to the SAU, resources belonging to the suspended NSVWs are preserved and marked as secure, preventing possible unauthorized accesses from the running NSVW.

**Worlds Communication Channel.** The UTANGO offers a communication infrastructure that allows the exchange of secure messages across NSVWs using message-passing, i.e., no-shared memory. Messages have a fixed 12-byte data stream length. UTANGO provides four APIs (i.e., blocking and non-blocking) to send and receive messages. The WCC acts as
a messaging gateway, checking each NSVW’s inbox and forwarding each message to the respective NSVW. The system designer is responsible for defining messages and semantic for the target application. Standardized APIs, such as the Global Platform TEE API, can be built atop these primitives.

IV. uTANGO IMPLEMENTATION

System Setup. The uTANGO TEE was firstly implemented for the Arm Musca-B1 Test Chip Board [42], which implements the SSE-200 subsystem that features a multi-core system with two Cortex-M33 processors. Despite the dual-core architecture, uTANGO currently only supports a single-core configuration. The majority of MCU-based platforms are powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs. There are a few platforms that are starting to include dual-core architectures, thus, multi-core powered by single-core CPUs.

uTANGO Hardware Components. The main software components of uTANGO rely on hardware primitives available on TrustZone-based MCUs. As previously mentioned, the WS uses the secure SysTick, as the temporal source for scheduling all NSVWs. To partition the system, the SP configures the SAU to overlap the fixed IDAU memory security regions and specify the overall system memory layout. With the SAU correctly configured, core transactions (including data read/write, instruction fetches, and debug access) are secured. As previously stated, we assume bus masters are always secured and managed by uTANGO, so TrustZone-aware bus slaves (i.e., memories and peripherals) need to be configured according to the overall system security model. We configure Musca-B1 security gates, i.e., the Memory Protection Controller (MPC) and the Peripheral Protection Controller (PPC), to match all NSVW’s memory and devices assignments. The remaining memory blocks or device sets are kept secure.

A. Execution Life Cycle

The uTANGO execution life cycle for a system configured with 2 NSVWs is depicted in Figure 3. The complete boot process consists of three stages: (i) Initialization; (ii) SP Partitioning; (iii) and finally Kicking-off. At run-time, uTANGO is just responsible for the WS Scheduling. In the following, we describe each stage.

1) uTANGO Initialization. After reset, the uTANGO boot agent initializes preliminary CPU- and platform-specific hardware components. Then, it reads the full system raw binary file (loaded onto the FLASH) and copies each software piece (i.e., uTANGO kernel and NSVWs) to its respective memory region. The boot agent is also responsible for verifying the integrity and authenticity of the uTANGO kernel image and, in case of success, to copy the image to the Tightly-Coupled Memory (TCM). This implementation detail ensures almost all uTANGO kernel instructions and memory accesses takes 1-2 clock cycles and that there is no additional burden due to wait states and bus/memory stalls (performance) and that code and data are never cached (security). After copying each NSVW to the respective memory segment, the initialization concludes by configuring the secure MPU to enforce policies among TEE kernel code and data sections, setting up the vector table address of uTANGO, and jumping to the main initialization routine. After boot, the uTANGO kernel starts executing by...
first enabling and configuring fault exceptions. Non-secure exceptions are configured with lower priority than secure ones, thus preventing starvation of the secure side, i.e., avoid DoS attacks. The secure SysTick timer is then configured according to the system quantum configuration, i.e., the reload value is loaded, and the timer exception is enabled. The last part of the Initialization process fills the internal WCB structures with the respective NSVWs’ static configurations. The WCB encompasses 9 general-purpose registers (r4-r14), 8 special purpose registers (i.e., msp, psp, msp_lim, psp_lim, basepri, primask, faultmask, control), and a subset of specific SCB registers (e.g., vtor, scr). To speed up the SAU re-configuration the world switching operation, the SAU configuration for each NSVW is defined as part of the WCB. The last part of the WCB includes an interrupt descriptor that keeps the NVIC registers’ context (e.g., priority level, enable and pending status, and security state), which we further detail in Section IV-B.

2) SP Partitioning. After the UTANGO Initialization, the execution flow continues through the SP Partitioning. The SP is responsible for leveraging all available hardware mechanisms to partition the system resources according to the NSVW’s settings. First, the SP unrolls all NSVW’s memory regions and checks for overlapping regions; if an overlap is identified, UTANGO aborts execution. If all memory regions are valid, the SP starts programming the SAU with the memory regions assigned to the first NSVW (NSVW #1 in Figure 2). The SAU is programmed through a set of memory-mapped registers, namely the Region Number Register (RNR), Region Base Address Register (RBAR), and Region Limit Address Register (RLAR). The RNR controls which region is active or selected, while the RBAR and RLAR set the region’s start address and its limit, respectively. This process results in a configuration similar to the SAU table depicted in Figure 2. After programming the SAU, the SP uses the platform-specific memory gates, i.e., the MPCs, to configure the system’s overall memory partition. The MPC is a block-based gate that divides the memory into multiple, alternating blocks of secure and non-secure regions. Transactions are filtered based on the programmed regions. Each block has a well-defined size, which can be configured as secure or non-secure. Therefore, the SP needs to check first if a set of blocks can represent all of NSVW’s memory regions. If regions are within the bounds of the MPCs, the SP configures the controller, which results in a configuration similar to the FLASH and RAM MPC’s tables depicted in Figure 2. Next, the SP configures the PPC to define non-secure access settings for each NSVW’s devices, and, lastly, the SP configures the NVIC’s ITNS registers to direct the interrupts of the first NSVW to the normal world.

3) UTANGO Kicking-off. In the last boot stage, UTANGO is responsible for configuring the CPU state for the first NSVW and kick off the execution. A non-secure call is issued to the entry point of the NSVW #1 (Figure 3). This function will switch the CPU state from secure to non-secure by issuing a BLXNS instruction. All the register banks are cleared to avoid information leakage. At this stage, the boot sequence is complete, and the processor starts executing the first NSVW.

4) WS Scheduling. At run-time, UTANGO is mainly responsible for scheduling and context switching NSVWs. The WS keeps the suspended NSVW states and resources in the secure world while remapping the next-to-run NSVW resources as non-secure. The WS process consists of four main steps (4.1-4.4). In the first step (4.1), the WS saves the context of the suspended NSVW. Thus, all general-purpose and special CPU registers, as well as selective SCB registers, are stored in the respective WCB. The WS is implemented in assembly, enabling these multiple accesses to the WCB memory segment to be combined into a single store-multiple instruction (STM) to improve performance. The NVIC state is also preserved in the WCB interrupt descriptor (details in Section IV-B). Next (4.2), the scheduler selects the next-to-run NSVW according to a round-robin policy. The WS retrieves the stored SAU data table from the scheduled NSVW’s WCB entry to program SAU in step three (4.3). The SAU re-configuration also leverages fine-grain assembly customizations by leveraging load-multiple instructions (LDM). However, due to the lack of fast-reconfiguration optimization mechanisms available in the SAU, the WS needs to program all eight SAU’s regions by iteratively accessing the RNR register. Finally, in step (4.4), the context of the scheduled NSVW is loaded to the CPU. At this point, a branch is issued and processor execution is switched to the non-secure state.

B. Worlds Interrupt Handling

In TrustZone-M MCUs, the NVIC registers are not banked between security states. The ITNS register enables the configuration of the interrupt’s security target. Thus, once an interrupt is configured as secure, accesses to the associated fields in non-secure aliases are read-as-zero. Thus, NVIC’s non-secure state must be preserved for each interrupt assigned to an NSVW. The WCB structure features a descriptor that holds the Interrupt Set Enable Register (ISER), Interrupt Set Pending Register (ISPR), Interrupt Priority Register (IPR), and ITNS. Interrupt management was first implemented using a non-preemptive mechanism where interrupts are served as soon as
the respective NSVW is scheduled. In this case, i.e., the worst-case scenario, the interrupt latency is delayed by the amount of time needed to perform a complete round of NSVWs (i.e., \(((NSVW - 1) \times tick) + schedtime\)). However, for real-time applications, this latency may be prohibitive. Current efforts are going through the extension of uTANGO to implement a preemptive priority-based mechanism. In the following, we only explain the current implementation. However, for the sake of clarity, we illustrate an example of the execution flow of both approaches in Figure 4.

**Non-preemptive World Interrupt Handling.** Figure 4(a) illustrates the non-preemptive interrupt handling flow. The vertical axis depicts the execution environment and its respective execution priority. uTANGO is represented as the system’s higher-priority workload (smaller number in priority level) since, by design, the secure world is more privileged than the normal world. NSVW #1 and NSVW #2 have the same priority level and take equal CPU quantum. A timer interrupt is assigned to NSVW #1, while an SPI interrupt is assigned to the NSVW #2. As previously explained, interrupts assigned to non-executing NSVWs, such as the SPI triggered at \(t_2\), will only be served as soon as its respective NSVW is put into context (from \(t_4\) to \(t_6\)). For this particular case, the SPI interrupt latency is equal to \(t_4 - t_2\). The same behavior happens to the timer interrupt. The interrupt is triggered at \(t_5\) (while NSVW #2 is running) but just served when NSVW #1 is resumed at \(t_7\). uTANGO enables this non-preemptive behavior by saving and restoring each interrupt state during the context switching of NSVWs (\(t_3\) to \(t_4\) and \(t_6\) to \(t_7\)). In particular, at the first scheduling point (\(t_3\) to \(t_4\)), the WS will save the NVIC’s state for the timer interrupt and restore the SPI’s pending bit and security target before resuming the NSVW #2. Once NSVW #2 is resumed at \(t_4\), if the SPI interrupt is enabled, the pended request will force the processor to attend the interrupt and start executing the respective SPI’s interrupt handler.

Figure 4(b) illustrates the priority-based interrupt handling flow. NSVWs are assigned (i.e., system designer) with a priority according to their criticality level. Higher-priority

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**C. Worlds Communication**

uTANGO implements a secure blocking and non-blocking request-response messaging mechanism to enable NSVWs to communicate with each other. Messages exchanged between NSVWs are limited to a 12-byte data stream and are sent via registers, avoiding sharing memory across worlds. The WCC uses the internal inbox structure of each NSVW to pass messages across senders and receivers. uTANGO exposes four secure APIs for sending and receiving messages. These APIs are implemented through secure entry points located in a predefined NSC memory region (light-blue NSC region in Figure 2), i.e., the WCC gateway. When an NSVW uses the sending API, the 12-byte data stream is copied to registers (i.e., \(r_4-r_6\)), which are read and placed into the receiver’s inbox by the WCC. When the receiver NSVW reads the message, it calls the WCC via the receiving API that copies the inbox message (if full) to the registers. The WCC carefully avoids information leakage by clearing the remaining CPU registers, before returning to the active NSVW.

**D. Reference IoT Application**

Figure 5 depicts the uTANGO IoT reference application. It implements a set of building blocks aiming at demonstrating the applicability of uTANGO to develop secure IoT devices. These building blocks implement the main features required by IoT devices, ranging from secure connectivity, real-time operation, and local management. Specifically, the NSVW #1 encapsulates an entire RTOS stack, i.e., the Zephyr RTOS, which has an application operating a servo motor via a PWM device. The NSVW #2 connects to a PC terminal via serial port (UART), implementing a local console to interact with the system. The NSVW #3 runs Mbed TLS, an open-source library that implements cryptographic primitives, certificate manipulation, and the SSL/TLS protocols. Finally, the NSVW #4 implements a full-blown TCP/IP stack to connect to the Internet. The uTANGO TEE provides hardware-enforced separation among all consolidated workloads.
V. Security Analysis

TrustZone-M hardware primitives ensure hardware-enforced isolation of system resources, i.e., code, data, devices, and interrupts. Thus, TrustZone-M hardware hooks are sufficient to materialize the UTango’s vision of providing a new security model that allows the consolidation of multiple, equally-secure, execution environments. Despite offering a strong foundation for system-level security, such as data and code protection, TrustZone lacks defining anti-tampering mechanisms and side-channel protection. Therefore, physical and side-channel attacks are out-of-the-scope. Hence, we trust Arm to provide a non-compromised TrustZone-M design in the Musca-B1 platform.

Our threat model is based on the very same assumptions delivered by the TrustZone-M [37], [39]. Firstly, we assume that an adversary cannot attack the secure software (i.e., UTango) through a compromised piece of non-secure software (i.e., an NSVW) via a local or remote software attack. Secondly, our multi-world security model takes advantage of the same hardware mechanisms that isolate the secure and non-secure worlds to guarantee that a compromised NSVW cannot hijack other execution environments. In a nutshell, we must assume the following:

- NSVWs running on the non-secure side are untrusted.
- UTango kernel, including all its software components, e.g., WS, and SP, are trusted.
- TrustZone-M hardware security extensions guarantee strong isolation between secure and non-secure states.
- The misuse of the TrustZone-M hardware components, such as the SAU and IDAU, can compromise the security model. Thus, the configuration file which defines the overall system partition must be trusted.

Next, we discuss how UTango can mitigate potential attack vectors that a malicious adversary could exploit.

Protection of UTango Kernel. Enabled by TrustZone hardwares controllers, the first isolation layer of the system separates the UTango kernel from the NSVWs. When the kernel partitions the system using the SAU, it ensures that all NSVWs run in the normal world, while the kernel is kept protected in the secure world. Therefore, the SAU controller validates all NSVW’s memory transactions, blocking access to resources outside of its domain. NSVWs can also attempt to extract information from UTango by leaking non-banked CPU registers. The attack can be carried out after a state transition, i.e., from secure to non-secure, which can happen after the (i) boot stage or (ii) after context switching periods.

The kernel prevents the leakage by (i) clearing all registers before jumping to the non-secure state and by (ii) inherently replacing the CPU state with the scheduled NSVW context.

Isolation of NSVWs. The UTango partition prevents NSVWs to share memory regions, devices, and interrupt sources. The bi-directional isolation of the NSVWs is enforced by the SAU and additional SoC security gates. In TrustZone-M platforms the configuration of the SAU and security gates is restricted to the secure world and managed by the UTango kernel. The UTango architecture allows developers to easily deploy 3rd party workloads. This feature can be leveraged by attackers to install malicious libraries or applications. Nevertheless, UTango hardware-enforced isolation prevents a compromised NSVW from overcoming its boundaries and escalating to other domains.

Secure Bus Masters. As discussed in Section VI, we assume that NSVWs interactions with additional bus masters are protected and mediated by the UTango. This design decision avoids the overhead of configuring each bus filter (i.e., MPC, PPC) during context switching, saving a considerable amount of CPU clock cycles. Moreover, this also prevents an attacker from gaining access to the overall system’s secure or non-secure memory. However, in an application scenario where an NSVW needs access to a DMA controller, UTango will offer a set of secure services to interface these hardware modules.

Secure Boot. By default, the processor starts in secure state, enabling root-of-trust implementations such as the secure boot. UTango features a 2-stage secure bootloader to verify the firmware image’s integrity and authenticity against a store signature (SHA-512) held in secure memory. Upon detecting a verification error, the UTango boot is aborted and the system is locked in a secure state until the next reset / power cycle. If the image is valid, the boot process continues until it handles control to the first NSVW to run.

Secure Services. As UTango continuous to mature, we intend to develop and include a set of secure services, such as secure storage, cryptography operations, audit logs, and secure updates over-the-air. These secure services will be encapsulated in dedicated NSVWs. However, depending on the peculiarities of the target platform, some hardware modules may be hardwired to the secure world. To address this challenge, we envision the development of lightweight (de-privileged) secure gates to mediate access to secure world resources. Additional hardware primitives (i.e., secure MPU) will be leveraged to enforce isolation within the secure world.

VI. Evaluation

We evaluated UTango on an Arm Musca-B1 Test Chip Board, which features two Cortex-M33 processors, running at 40 MHz (CPU0) and 160 MHz (CPU1). Firstly, in Section VI-A we assess a set of security metrics derived from the BenchIoT suite [43]. On Section VI-B we evaluate performance, and in Section VI-C we focus on the interrupt latency. Lastly, in Section VI-D we evaluate code and binary sizes.

A. Security Metrics

BenchIoT [43] is a recent benchmark suite and an evaluation framework to evaluate security solutions for IoT-based MCUs. The suite enables the automatic collection of 14 metrics for security, performance, memory usage, and energy consumption. As of this writing, BenchIoT can only support Armv7-M architectures [43], i.e., BenchIoT cannot be used to evaluate UTango. Notwithstanding, we performed a best-effort evaluation of UTango’s security based on the BenchIoT’s eight security metrics while keeping as close as possible to the framework principles and metrics criteria.
According to the evaluation model presented in Ref. [43], we organized the security metrics in three goals: (i) minimizing privileged execution (i.e., total of privileged and system call cycles); (ii) enforcing memory isolation (i.e., maximum code and data region ratio); and (iii) control-flow hijacking protection (i.e., number of available ROP gadgets and indirect calls, and data execution prevention).

**Minimizing Privileged Execution.** For Armv7-M MCUs, BenchIoT counts as privileged cycles all instructions executed in privileged thread and handler mode. For TrustZone-enable Armv8-M MCUs, all CPU modes are banked, but the secure world is always considered more privileged than the normal world. Thus, we count as privileged cycles all instructions executed in the secure privileged thread and secure handler mode. In the context of our architecture, UTANGO is the single component running in secure privilege thread mode, at boot time, and secure handler mode, at run-time. All NSVWs run within the normal world, and so all execution cycles are not taken into consideration. Our results show that, at run-time, UTANGO runs a total of 215 privileged cycles at each system tick (Section VI-B). At boot-time, the total number of thread privileged cycles is 7749 cycles (for 1 NSVW) and increases, on average, 1236 cycles for each extra added NSVW.

BenchIoT also counts the number of SVC cycles. Unprivileged code can leverage this instruction to trigger a system call intended at executing privileged thread code. This mechanism can be leveraged as a potential attack vector. In the context of TrustZone-M MCUs, SVC calls can be issued in secure and non-secure states. As aforementioned, non-secure SVCs are not taken into consideration as normal world code is always considered not privileged. UTANGO does not issue any SVC call, i.e., the number of secure SVC calls is 0. The execution flow has a well-defined entry and exit point, always running in secure handler mode.

**Enforcing Memory Isolation.** Another two security metrics evaluated by BenchIoT are the (i) maximum data region ratio and (ii) maximum code region ratio. These two metrics aim at assessing memory isolation’s effectiveness by computing the size ratio of the maximum available code/data regions to an attacker with respect to the total code/data size of the application binary [43]. UTANGO isolates each environment within a strong compartment, with boundaries of the NSVW defined per binary needs. Thus, the maximum data and code region ratio is 0.

**Control-Flow Hijacking Protection.** Code reuse attacks (i.e., ROP gadgets and indirect calls) are among the most common attack vectors used to hijack the control flow of an application. To measure the number of ROP gadgets, we used the ROPGadget tool [44]. UTANGO has a total of 303 ROP gadgets. Notwithstanding, a deeper investigation unveiled that these ROPs belong to the boot-related code and are not executed during runtime. As stated in Section IV-A, all the world scheduling logic is implemented in assembly. Although this number is an order of magnitude smaller comparing to ATF-M and the results presented in Ref. [43], we are aiming at squeezing this value in the near future, by implementing also the boot logic in assembly or leveraging inline substitution optimizations. Indirect calls are another type of code reuse attacks that relies on using function pointers to hijack the control flow. In the case of UTANGO, we parsed the binary file and we found only one indirect call related to the secure to non-secure exit point, issued through a BLXNS instruction.

Another important aspect in defending against control-flow hijacking is related to data execution prevention (DEP) mechanisms. In the context of Arm MCUs, proposed defense mechanisms leverage the MPU to enforce memory regions, either writable (data) or executable (code) [43]. UTANGO currently leverages the secure MPU to enforce DEP among kernel code and data sections. Furthermore, as mention in Section V, we will also leverage the secure MPU to enforce isolation and deploy a DEP defense mechanism among security gates.

### B. Performance Overhead

**World Switch Time.** The world switch time is defined as the amount of time that the UTANGO kernel takes to switch between NSVWs. As explained in Section IV-A, this operation includes saving and restoring the worlds’ context (i.e., core registers, system registers, and NVIC), re-configuring the SAU regions (to enforce memory isolation), and run the scheduler algorithm. To measure the world switch time, we used the Data Watchpoint and Trace (DWT) unit [45] from the CoreSight debug system, which features a 32-bit cycle counter running at the CPU clock frequency. The DWT cycle counter is read before and after completing the WS operation. We collected 1000 samples. All the collected samples reported exactly 215 clock cycles (i.e., 5.4 microseconds @ 40 MHz). The high determinism is a reflex of (i) the characteristics of the Armv8-M architecture and (ii) from the fact UTANGO runs from a TCM (Section IV-A). The reduced world switch time is a consequence of (i) the raw assembly implementation of the WS logic and the (ii) TCM. For instance, when configured with a 10 milliseconds (ms) tick rate, the expected performance penalty is a negligible 0.054%.

**Run-time Overhead.** To evaluate the run-time overhead, we have used Embench (version 0.5) [46]. Embench is a free and open-source benchmark suite specially designed for deeply embedded systems. Assuming the presence of no OS and minimal C library support, Embench targets small devices with at least ≤64 KiB of Flash (ROM) and ≤16 KiB of RAM. Embench consists of 19 real programs, representatives of the following metrics: branch, memory, and computing requirements. Each benchmark reports a single summarizing performance score that outputs the geometric mean and geometric standard deviation ratios relative to a reference platform or setup, which in our case represents the target Musca-B1 Test Chip Board. Benchmarks and UTANGO were compiled using the target platform and toolchain configuration described in Table I. Despite Arm Musca-B1 featuring a dual asymmetric Cortex-M33 MCU, UTANGO currently only supports a single-core configuration. Thus, in our experiments, we have only enabled the CPU0, running at 40 MHz.

We have run the benchmarks natively on the target platform. Then, each benchmark was executed with UTANGO, config-
Looking at Figure 6, we can draw four main conclusions. Firstly, for a configuration with 1 NSVW, the overhead in parentheses). The achieved results for 0.5 and 10 ms are illustrated in Figure 6, where each bar (representing 1, 2, 3, and 4 NSVWs) depicts the respective ratios relative to the baseline. On top of the first and second bar, it is also presented the absolute execution time, in clock cycles, and total execution time in ms (within parentheses).

Looking at Figure 6, we can draw four main conclusions. Firstly, for a configuration with 1 NSVW, the overhead introduced by UTANGO is almost residual. For instance, for a 10 ms tick rate, the average performance overhead is 0.05%, which is within the expected theoretical overhead (see world switch time). For a 500 microseconds tick rate, which is considered an abnormal high switching rate (i.e., highly responsive system), the average performance overhead is less than 1%. Secondly, we can observe that the performance overhead increases (almost) linearly with the number of NSVW’s, i.e., the third, fourth, and fifth bars (2, 3, and 4 NSVWs, respectively) increase the performance overhead by a similar ratio. This impact is expected and is a natural consequence of sharing the CPU among all NSVWs, i.e., each NSVW gets a CPU quantum equal to the tick rate. A third and interesting observation is related to the heterogeneity on the performance overhead ratio when the system is configured with multiple NSVWs, in particular, for 3 and 4 NSVWs. This phenomenon becomes even more evident for the experiments conducted with a 10 ms tick rate. We observed that increasing the UTANGO tick rate may suggest that, for the majority of the benchmarks, the system gets an increase of performance (i.e., decrease of the performance overhead ratio). The most evident case is observed for the huffbench benchmark, which for a 10 ms tick rate, suggests that there is no performance penalty, i.e., the ratio is always 1 no matter how many NSVWs are running a toy bare-metal application, implementing a bare infinite loop (i.e., other worlds are just consuming their CPU quantum). Experiments were repeated for different tick rate configurations, ranging from 0.5 ms to 10 ms.

TABLE II: Platform, toolchain, and compilation details.

| Platform | Tool chain |
|----------|-----------|
| frequency | 40 MHz (CPU) |
| max. frequency | 160 MHz (CPU) |
| architecture | Armv8-M |
| isa | Thumb/Thumb-2 |
| address size | 32-bit |
| code mem-ory size | 512 Kib eRAM |
| data mem-ory size | 512 Kib iRAM |
| processor name | Cortex-M33 |
| caches | 2 Kib lCache |
| active cores | 1 (CPU) |
| Compiler | GNU Arm Embedded Toolchain |
| Compiler version | arm-none-eabi-gcc 9.3.1 |
| Flags | -Os -march=armv8-m.main-mcpu=cortex-m33+nodsp-ffunction-sections-mfloat-abi=softfp -mthumb |
| linker | GNU binutils ld version 2.34.0 |

Fig. 6: Performance overheads (ratio) of Embench benchmark suite relative to bare-metal execution.
time slots in the first round are wasted, which results in an additional impact in the final performance overhead ratio.

Figure 7 depicts the impact of the uTANGO tick rate variation on the overall performance overhead. We have repeated this experiment for four different tick rates (0.5 ms, 1 ms, 2 ms, and 10 ms), where each obtained value corresponds to the geometric mean ratio for the full-run of the Embench suite running in systems configured with different NSVWs. From the obtained results, we can validate the phenomenon described above. While increasing the uTANGO tick rate, there is an apparent decrease of the performance overhead (Figure 7). Looking at Figure 7b, we can also conclude that the performance overhead increases exponentially while decreasing the tick rate. However, this exponentially increase is very acceptable, because for a 500 microseconds tick rate, the performance overhead is less than 1%. This impact will be less noticeable in platforms running at higher frequency, e.g., the NXP LPC55S69-EVK and STM NUCLEO-L552ZE-Q, which running at a frequency approximately three times higher, the overhead would decrease by a factor of three.

C. Interrupt Latency

To measure the interrupt latency, we crafted a minimal bare-metal benchmark application, running in the NSVW#1, that continuously configures a timer (25 nanoseconds resolution) to trigger an interrupt every 10 ms. Since the time stamp when the interrupt was triggered is known, the latency can be calculated as the difference between the expected wall-clock time and the actual instant it starts handling the interrupt. We have performed two experiments for different uTANGO tick rates (0.5 ms and 10 ms), while varying the number of NSVWs to be scheduled. The results were obtained by taking 1000 samples. Figure 8 depicts the relative frequency of each interrupt latency measurements. The results are expressed in the number of clock cycles required by the CPU to start executing the timer handler. According to Figure 8, we can draw two major conclusions.

Firstly, depending on when the interrupt is triggered, we can achieve better or worse execution times: (1) if the interrupt is triggered while the NSVW handler is executing, the measured latency is near its native values (observed for all configurations with one world). The NSVW receives the interrupt transparently through normal hardware interrupt behavior, and the final interrupt handler executes within a fixed 24 clock cycles; (2) if the interrupt triggers when a different NSVW is active, the interrupt latency increases significantly since the interrupt will only be handled when the assigned NSVW is scheduled.

The second takeaway point comes from observing a direct relation between the system tick rate, the number of NSVWs, and the time interval selected for the interrupting timer (10ms). Considering the scenario with 2 NSVW, depicted in Figure 8a, the interrupt latency for the 1000 collected samples shows a relative frequency of 100% for 24 clock cycles. Such results are explained by the number of rounds (each one taking 1 ms) needed to complete the 10 ms interval (at a tick rate of 0.5 ms) when two worlds are configured, which is 20. This means that the timer interrupt will be triggered approximately when the handling world is executing. On the other hand, in the scenario with 3 NSVW, each round takes 1.5 ms to complete; therefore, the system needs ≈6.67 rounds to complete 10 ms. Such variation shifts the trigger point of the interrupt to a specific point in time where a different NSVW is executing, delaying the interrupt to be serviced.

D. Code and Binary Size

uTANGO was developed from-scratch with no dependencies on compiler or external libraries. Table III reports (i) the number of SLoC and (ii) the binary size.

Source lines of code. To count the number of SLoC, we used the SLOCCount tool [47]. uTANGO implementation code is divided into three main directories: (i) arch, targeting Armv8-M architectural-specific functionalities; (ii) platform, containing platform-specific code (e.g., memory and peripheral protection controllers); and (iii) core, i.e., uTANGO boot and scheduler logic (e.g., memory and devices partition, and system timer
From Table [III] it is possible to conclude that the architectural and platform-specific code represent most of the total SLoC. Since uTANGO’s heavy lifting work is during boot-time, i.e., system resources partition, hardware initialization, and configuration, it is normal that these two components reflect the major part of the uTANGO code complexity (∼2K SLoC). On the other side, the run-time logic, i.e., worlds scheduling and the re-partition of system resources, which is implemented in assembly, encompasses a total of ∼200 SLoC, corresponding to 4.6% of the total SLoC.

Binary size. To measure the size (bytes) of uTANGO, we use the GCC size tool (Berkeley format). Table [III] presents the text, data, and bss sections, according to system component, i.e., organized by directories. As highlighted above, target-specific functionality (e.g., SAU, SysTick, MPC, and PPC drivers) included in arch and platform directories represent approximately 2/3 of the total uTANGO’s size. At boot-time, uTANGO core allocates the WCB structure and performs initialization routines. For each configured world, the system allocates 324 bytes of data for its private WCB. During WCB’s initialization, uTANGO retrieves from the config structure (60 bytes) each world’s configuration. This structure is filled by the system designer to describe, per world, the memory layout, available devices, and assigned interrupts. Regarding run-time code, the total size is 488 bytes, which represents the code implementing the scheduling logic. Thus, the resulting TCB size is 4.3 KiB.

VII. RELATED WORK

There is a rich body of runtime environments, isolation techniques and mechanisms, and architectures for secure execution and isolated environments [7], [9]–[23], [48]. Due to the extensive list of works, we will focus on the two following classes of solutions that target IoT devices powered by resource-constrained MCUs.

**TEE systems for the IoT.** TEE systems for resource-constrained IoT devices are in their infancy, and only a few commercial and academic solutions have been proposed so far. Janjua et al. [17] have developed the Security MicroVisor (SuV), a pure-software TEE for resource-constrained devices that lack basic hardware-based security features such as MPU (e.g., AVR ATmega). MultiZone TEE [25] is an innovative hardware-enforced, software-defined TEE for (Armv7-M) Cortex-M and RISC-V MCUs. MultiZone leverages the Arm MPU or the RISC-V Physical Memory Protection (PMP) to create multiple isolated environments. In the context of TrustZone-M MCUs, ATF-M [35] provides an open source reference implementation of a TEE for Armv8-M devices. Kinibi-M [36] and ProvenCore-M [49] are preeminent examples of commercial TEE solutions adapted from existing well-established Cortex-A implementations. mTower [50] is an open source initiative from Samsung aiming at developing a TEE specially designed to protect size-constrained IoT devices based on the Cortex-M23. Contrary to the aforementioned TrustZone-M solutions, which are a strict materialization of the TrustZone dual-world architecture, uTANGO relies on a multi-world design, providing multiple isolated environments within the normal world, and thus addressing the main architectural deficiencies observed in commercial TrustZone systems while providing augmented TEE capabilities. To the best of our knowledge, MultiZone [26] is the closest solution to uTANGO. Notwithstanding, comparing to our approach, MultiZone for Arm Cortex-M requires (i) static binary translation to handle special privileged instructions and imprecise bus faults and (ii) implements trap and emulation. There is also a preeminent class of solutions that proposes a set of mechanisms for TrustZone-M devices. CoreLockr-TZ [51] is a lightweight service dispatch layer and CFI CaRE [27] implements a prime control-flow integrity (CFI) mechanism. Finally, ASSURED [28] proposes a secure firmware update framework for TrustZone-M devices.

| Directory                          | SLoC     | size (bytes)         |
|-----------------------------------|----------|----------------------|
| /arch/armv8-m                      | 787      | 393                  |
| /platform/MUSCABI                  | 1140     | 0                    |
| /core                             | 264      | 0                    |
| /config (2 worlds)                | 93       | 0                    |
| **total**                          | **2284** | **393**              |

**TABLE III: uTANGO: SLoC and binary size (bytes) per directory.**
In this paper, we presented uTANGO, the first multi-world TEE for TrustZone-M IoT devices. Our innovative design enables the execution of multiple environments within strongly isolated compartments with increasing flexibility and security guarantees. uTANGO will be publicly available in hopes of engaging both academia and industry on research and deployment of innovative TEE solutions for the IoT.

REFERENCES

[1] S. L. Keoh, S. S. Kumar, and H. Tschofenig, “Securing the internet of things: A standardization perspective,” IEEE Internet of Things Journal, vol. 1, no. 3, pp. 265–275, 2014.

[2] O. Alrawi, C. Lever, M. Antonakakis, and F. Monrose, “SoK: Security Evaluation of Home-Based IoT Deployments,” in 2019 IEEE Symposium on Security and Privacy (SP), 2019, pp. 1362–1380.

[3] E. Cozzi, P. Veroor, M. Delli’Amico, Y. Shen, L. Bilge, and D. Balzarotti, “The Tangled Genealogy of IoT Malware,” in Annual Computer Security Applications Conference (ACSAC), 2020, p. 16.

[4] A.-R. Sadeghi, C. Wachsmann, and M. Waidner, “Security and privacy challenges in industrial Internet of Things,” in 2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC), 2015, pp. 1–6.

[5] R. Pan, G. Peach, Y. Ren, and G. Parmer, “Predictable virtualization on memory protection unit-based microcontrollers,” in 2018 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2018, pp. 62–74.

[6] S. Pinto, H. Araujo, D. Oliveira, J. Martins, and A. Tavares, “Virtualization on TrustZone-Enabled Microcontrollers? Void!” in 2019 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), 2019, pp. 293–304.

[7] G. Klein, K. Elphinstone, G. Heiser, J. Andronick, D. Cock, P. Derrin, D. Elkdauwe, K. Engelhardt, R. Kolanski, M. Norrish, T. Sewell, H. Tsch, and S. Winwood, “SeL4: Formal Verification of an OS Kernel,” in ACM SOSP, New York, NY, USA, 2009, p. 207–220.

[8] M. Payer and T. R. Gross, “CFI CaRE: Hardware-Compliant Pure-Software Trusted Execution Environment for Resource-Constrained Embedded Devices,” in Proceedings of the 4th Workshop on System Software for Trusted Execution, ser. SystEX’19, New York, NY, USA, 2019.

[9] F. Brasser, D. Gent, P. Jauernig, A.-R. Sadeghi, and E. Stapf, “SANC- TUARY: ARMin TrustZone with User-space Enclaves,” in Network and Distributed Systems Security (NDSS) Symposium, 2019.

[10] S. Pinto and N. Santos, “Demyxifying Arm TrustZone: A Comprehensive Survey,” ACM Comput. Surv., vol. 51, no. 6, pp. 130:1–130:36, Jan. 2019.

[11] W. Li, Y. Xia, L. Lu, H. Chen, and B. Zang, “TEE: Virtualizing Trusted Execution Environments on Mobile Platforms,” in Proceedings of the 15th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments, ser. VEE 2019, New York, NY, USA: ACM, 2019, pp. 19, 2019–2019.

[12] S. il Hahn, J. Kim, A. Jeong, H. Yi, S. Chang, K. SN, A. Chauhan, and S. P. Cherian, “Reliable Real-Time Operating System for IoT Devices,” IEEE Internet of Things Journal, pp. 1–1, 2020.

[13] D. Lee, D. Kohlbrenner, S. Shinde, K. Asanović, and D. Song, “Kernelize: An Open Framework for Architecting Trusted Execution Environments,” in Proceedings of the Fifteenth European Conference on Computer Systems, ser. EuroSys ’20, New York, NY, USA: Association for Computing Machinery, 2020.

[14] R. Bahmani, F. Brasser, G. Dessouky, P. Jauernig, M. Klümmer, A.-R. Sadeghi, and E. Stapf, “CURE: A Security Architecture with Customizable and Resilient Enclaves,” in 30th USENIX Security Symposium (USENIX Security 21), Vancouver, B.C.: USENIX Association, Aug. 2021.

[15] N. Santos, H. Raj, S. Saroia, and A. Wolman, “Using arm trusterne to build a trusted language runtime for mobile applications,” SIGARCH Comput. Archit. News, vol. 42, no. 1, pp. 67–80, Feb. 2014.

[16] H. Hua, J. Gu, Y. Xia, H. Chen, B. Zang, and H. Guan, “VTZ: Virtualizing ARM TrustZone,” in USENIX Security Symposium. USENIX Association, 2017, pp. 541–556.

[17] S. Pinto and C. Garlati, “Multi Zone Security for Arm Cortex-M Devices,” in Embedded World Conference 2020, no. March, 2020, p. 6.

[18] T. Nyman, J. Ekberg, L. Davi, and N. Asokan, CFI CaRe: Hardware-Supported Call and Return Enforcement for Commercial Microcontrollers. Springer International Publishing, 2017, pp. 259–284.

[19] N. Asokan, T. Nyman, N. Rattanavipanon, A.-R. Sadeghi, and G. Tsudik, “ASSURED: Architecture for Secure Software Update of Realistic Embedded Devices,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 11, pp. 2290–2300, Nov. 2018.

[20] N. Zhang, H. Sun, K. Sun, W. Lou, and Y. T. Hou, “CacheKit: Evading Memory Introspection Using Cache Incoherence,” in IEEE European Symposium on Security and Privacy, March 2016, pp. 337–352.

[21] M. Lipp, D. Gruss, R. Spreitzer, C. Mauric, and S. Mangard, “ARMageddon: Cache Attacks on Mobile Devices,” in USENIX Conference on Security Symposium. USENIX Association, 2016, pp. 549–564.

[22] A. Machiry, E. Gustafson, C. Spensky, C. Sails, N. Stephens, R. Wang, A. Bianchi, Y. R. Choe, C. Kruegel, and G. Vigna, “BOOMERANG: Exploiting the Semantic Gap in Trusted Execution Environments,” in Network and Distributed System Security Symposium, 2017.

[23] A. Tang, S. Sethumadhavan, and S. Stolfo, “CLKSCREW: Exposing the perils of security-oblivious energy management,” in USENIX Security Symposium. USENIX Association, 2017, pp. 1057–1074.

[24] K. Ryan, “Hardware-Backed Heist: Extracting ECDSA Keys from Qualcomm’s TrustZone,” in Proceedings of the 2019 ACM SIGSAC Conference on Computer and Communications Security, ser. CCS ’19, New York, NY, USA: Association for Computing Machinery, 2019, p. 181–194.

[25] D. Cerdeira, N. Santos, P. Fonseca, and S. Pinto, “SoK: Understanding the Prevailing Security Vulnerabilities in TrustZone-assisted TEE Systems,” in IEEE Symposium on Security and Privacy (SP), 2020, pp. 1416–1432.

[26] Arm, “Arm Trusted Firmware,” accessed: 2021-01-12. [Online]. Available: https://www.trustedfirmware.org/.

[27] Trustonic, “Trustonic Kit,” accessed: 2021-01-12. [Online]. Available: https://www.trustonic.com/technology/.

[28] Arm, “Arm trustzone technology for the armv8-m architecture,” Arm Ltd., Tech. Rep., Oct 2018.
[38] ——, “Platform Security Architecture Application Guide,” Arm Ltd., Tech. Rep., 2019.
[39] ——, “Using trustzone on armv8-m,” Arm Ltd., Tech. Rep., Sep 2019.
[40] ——, “Arm Platform Security Architecture,” accessed: 2021-01-30. [Online]. Available: https://www.arm.com/why-arm/architecture/platform-security-architecture
[41] C. Garlati and S. Pinto, “A Clean Slate Approach to Linux Security RISC-V Enclaves,” in Embedded World Conference 2020, no. March, 2020, p. 5.
[42] Arm, “Arm® musca-a test chip and board technical reference manual,” Arm Ltd., Tech. Rep., Jan 2018.
[43] N. S. Almakhdhub, A. A. Clements, M. Payer, and S. Bagchi, “Benchiot: A security benchmark for the internet of things,” in 2019 49th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), 2019, pp. 234–246.
[44] J. Salwan, “ROPgadget - Gadgets finder and auto-roper,” accessed: 2021-01-29. [Online]. Available: http://shell-storm.org/project/ROPgadget/
[45] Arm, “Armv8-m architecture reference manual,” Arm Ltd., Tech. Rep., Dec 2019.
[46] D. Patterson, J. Bennett, P. Dabbel, C. Garlati, G. S. Madhusudan, and T. Mudge, “Embencb: A Modern Embedded Benchmark Suite,” accessed: 2020-12-22. [Online]. Available: https://www.embench.org/
[47] D. Wheeler, “SLOCCount,” accessed: 2020-12-15. [Online]. Available: https://dwheeler.com/sloccount/
[48] J. Noorman, P. Agten, W. Daniels, R. Strackx, A. V. Herreweghe, C. Huygens, B. Preneel, I. Verbauwhede, and F. Piessens, “Sancus: Low-cost trustworthy extensible networked devices with a zero-software trusted computing base,” in 22nd USENIX Security Symposium (USENIX Security 13). Washington, D.C.: USENIX Association, Aug. 2013, pp. 479–498.
[49] Prove&Run, “ProvenCore-M,” accessed: 2021-01-12. [Online]. Available: https://www.provenrun.com/products/provencore/
[50] T. A. Drozdovskyi and O. S. Moliavko, “itower: Trusted execution environment for mcu-based devices,” Journal of Open Source Software, vol. 4, no. 40, p. 1494, 2019.
[51] Sequitur Labs, “CoreLockr-TZ,” 2017, accessed: 2021-01-01. [Online]. Available: https://www.sequiturhowspublishedabs.com/corelockrtz/
[52] A. Levy, B. Campbell, B. Ghena, D. B. Giffin, P. Pannuto, P. Dutta, and P. Levis, “Multiprogramming a 64kB Computer Safely and Efficiently,” in Symp. on Operating Systems Principles (SOSP), 2017, pp. 234–251.
[53] A. A. Clements, N. S. Almakhdhub, K. S. Saub, P. Srivastava, J. Koo, S. Bagchi, and M. Payer, “Protecting Bare-Metal Embedded Systems with Privilege Overlays,” in 2017 IEEE Symposium on Security and Privacy (SP), 2017, pp. 289–303.
[54] D. Kwon, J. Shin, G. Kim, B. Lee, Y. Cho, and Y. Paek, “uxom: Efficient execute-only memory on ARM cortex-m,” in 28th USENIX Security Symposium (USENIX Security 19). Santa Clara, CA: USENIX Association, Aug. 2019, pp. 231–247.
[55] G. Peach, R. Pan, Z. Wu, G. Parmer, C. Haster, and L. Cherkasova, “eWASM: Practical Software Fault Isolation for Reliable Embedded Devices,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 11, pp. 3492–3505, 2020.
[56] O. Hahn, E. Baccelli, H. Petersen, and N. Tsiftes, “Operating systems for low-end devices in the internet of things: A survey,” IEEE Internet of Things Journal, vol. 3, no. 5, pp. 720–734, 2016.
[57] M. Silva, D. Cerdeira, S. Pinto, and T. Gomes, “Operating Systems for Internet of Things Low-End Devices: Analysis and Benchmarking,” IEEE Internet of Things Journal, vol. 6, no. 6, pp. 10 375–10 383, 2019.
[58] F. Bruns, D. Kuschnerus, and A. Bilgic, “Virtualization for Safety-critical, Deeply-embedded Devices,” in ACM Symposium on Applied Computing (SAC), 2013, pp. 1485–1492.
[59] F. Paci, D. Brunelli, and L. Benini, “Lightweight IO virtualization on MPU enabled microcontrollers,” ACM SIGBED Review, vol. 15, no. 1, pp. 50–56, 2018.
[60] Arm, “Mbed OS,” accessed: 2021-01-12. [Online]. Available: https://os.mbed.com/mbed-os/
[61] Amazon, “FreeRTOS,” accessed: 2021-01-12. [Online]. Available: https://www.freertos.org/
[62] L. F. Project, “Zephyr,” accessed: 2021-01-12. [Online]. Available: https://zephyrproject.org/