Synchronized Multi-Rate Test Pattern Generation Using Hybrid Twisted Ring Counter and LFSR for BIST Application

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Abstract. This work presents a new approach for built-in test pattern generation (BIST) based on the variable rate clock-driven linear feedback shift register (LFSR) and twisted-ring counters (TRCs). The proposed technique operates on different operating clocks for generating deterministic test pattern sequence for the circuit under test (CUT). The test vectors generated by LFSR are transformed and reproduced with TRC results. The TRC design constitutes of only flip-flops, which be used as a potential alternative to improved seed storage and complex multi polynomial configurations in LFSR. Moreover, the control logic is simplified with synchronized multi-rate clock generation and can be easily extended for any test cubes among multiple CUTs. The randomness characteristics of LFSR are retained with improved memory efficiency and considerable complexity reduction. Experimental results validate the proposed test pattern generator (TPG) over existing well-known LFSRs models, and its randomness is proved with ISCAS benchmark circuits.

Keywords: Twisted-ring counters (TRC), Linear feedback shift register (LFSR), Built-in self-test (BIST), test pattern generation (TPG), circuit under test (CUT) etc.

1. Introduction
In recent years BIST has emerged as a prominent solution for many complex digital systems to improve its performance by detecting and diagnosing some defects. On the other Low energy consumption is also reduced drastically with the invention of many battery-operated hand-held devices such as vision-based multimedia products and mobile phones. Low power BIST is an increasingly important design concern since the resulting heat during testing limits the performance of the overall system. This makes testing a difficult task to accomplish, which requires new methodologies in the BIST. It has to meet some design requirements in addition to fault coverage as follows: the least possible energy consumption and hardware complexity overhead during testing. In general, TPG is the most dominant processing unit while optimizing the parametric constrains in BIST architecture [2].
Intensive research efforts towards BIST, LFSRs the most widely used pattern generator model in-circuit testing [3]. LFSR has numerous advantages as compared to other TPG models, such as high robustness and fault coverage. In general, any BIST test pattern generators (TPGs) target the different categories while generating test patterns. First test patterns are highly motivated to increase the fault coverage with the least possible test pattern length. Then the successive energy consumption due to exhaustive pseudo sequences in CUT is minimized with controlled bit transmission during testing. This can be achieved by addressing the randomness of TPG and its fine control using post-processing blocks. Several methodologies have been investigated to accomplish this task, such as toggle controlled TPG [4], fault coverage has driven- pattern generation [5], and hybrid integration of various forms of TPGs [6], etc. In the case of LFSR TPG, its performance metrics are statistically pre-determined using (i) pre-computation of seed which is required to store in memory, and (ii) formulation of feedback polynomial, which requires solving some complex polynomial terms.

According to the design specifications, the deterministic test patterns are generated in two ways, (i) encoded seeds and multiple polynomial configurations in LFSR (ii) using counters or TRC. In exiting methods, bit fixing or bit-flipping techniques are widely used in the LFSR test sequence to generate highly randomized test vectors with reduced complexity overhead. In general, LFSR-based mixed-mode BIST large number of seeds needs to be employed at least one for each deterministic pattern. Moreover, to cover hard-to-detect faults, a large number of test patterns is required, which will increase the testing time and complexity overhead.

In this paper, we propose an LFSR unit integrated with TRC that can be used in conjunction with an All digital phase-locked loop (ADPLL) based clock controller to significantly reduce the memory requirement to generate test patterns and to reduce the testing power. Here both memory space requirements and polynomial computation kernels of conventional LFSR are suppressed without compromising the LFSR randomness characteristics. This work is intended to operate LFSR and TRC units with different clocks to get the maximum number of test vectors from each LFSR generated test pattern for a given seed. Moreover, the problems related to synchronization are also solved with appropriate phase match among various computational blocks. The potential metrics of the proposed TPG is it doesn’t require reseeding routinely and not used polynomial characterization, which raises major concern in many BIST situations. The proposed test pattern generator can be useful for detecting hardware to detect faults with improved randomness and low power BIST as well. The overall testing time required to achieve 100% fault coverage over CUT with random faults is also minimized.

This paper presents a BIST TPG, which combines LFSR and TRC to generate the test patterns to reduce the power consumption and hardware complexity overhead without compromising the fault coverage. This is obtained by reducing the memory space requirement and excluding the complex polynomial computation associated with the conventional LFST and TRC drove post-processing with LFSR random results called weighted control units. The paper is organized as follows. Section 2 presents some preliminaries on various test pattern generators testing and BIST implementations. The proposed hybrid LFSR design and its functionality are presented in section 3. Experimental results for performance validation are performed using the ISCAS benchmark circuits in section 4. The conclusion is given in section 5.

2. Related Works
In existing BIST implementations, many types of TPG techniques are developed for low power testing with maximum fault coverage. Among them, LFSR and TRC are widely used in BIST applications due to their capability of generating both test cube and non-test cube vectors. Reseeding is extensively used for both LFSR and TRC based TPG models. It has been investigated in many exiting works for producing both pseudo-random and deterministic test vectors, and memory blocks can be optimized using appropriate encoded units. For many BIST applications, test-per-clock BIST widely preferred choice for high-performance due to its least critical path overhead. In [7], reseeding-based TRC TPG is developed where the seed values are stored in the form of an encoded version to reduce the memory
space requirements. In some hybrid approaches [8], test sets are generated from both TRC and LFSR reseeding schemes, significantly reducing the sizes and pattern length. Also, experimental results prove that the integration of TRC with LFSR design increases the encoding efficiency and reduces the memory storage requirements of LFSR seeds. The deterministic test patterns can be generated only by selecting appropriate seed values. It will be stored as compressed vectors that can produce any arbitrary seed dynamically to accommodate a wide range of seeds. It is shown in [9] that the compression of seeds provides the same fault coverage with the increased number of test vectors. In [10] Berlekamp-Massey algorithm and the Sidorenko-Bossert theorem is used to compute LFSR polynomials to get 100% fault coverage. However, computing a polynomial of higher degree for given test cubes always required to solve multiple non-linear systems, and also fixing a polynomial degree before testing is also a difficult task to accomplish in many BIST applications.

The power-related problems in existing LFSR TPGs are solved by transforming random test patterns into weighted random patterns using some pre-determined weights. Then overall bit transitions are considerably reduced either by change the bit position or using the XOR network. In [11], low transition Test Pattern Generators is developed using Modified Low Transition LFSR to reduce power consumption. Here the switching activity between successive sequences is reduced by inserting random bit in the two consecutive. In [12], basis transition densities test sequences are selected to reduce switching activity. However, finding appropriate weight vectors to control the test patterns transition is needed to be carried out externally before applying test vectors to circuits. In [13], bits transitions between test pattern sequences are reduced by combining the scalable Single Input Change (SIC) counter and Thermometer Code Counter for designing TPGs. The performance metrics are validated in both Test-Per-Scans, Test-Per-Clock models during testing. In [14] introduce non-volatile embedded resistive random access memory (RRAM) devices to implement LFSR-based BIST. This memristor ratioed logic (MRL)-based LFSR design reduces the complexity overhead considerably. In [15], testing power is reduced by monitoring the correlation measures between the sequences.

![Figure 1](image-url)  
**Figure 1.** Variable-rate clock-controlled TRC - LFSR pattern generator

Whenever the patterns are positively correlated, the generated sequences are post-processed using the XOR network. In [16], ring-based LFSR is proposed to reduce the existing LFSR model's power-related problems. This TPG combines two different LFSR sets and is controlled separately using two different clocks to generate highly randomized test patterns. Bit Swapping-LFSR TPG developed in [17] includes pre-charge, set-reset, and mux-based gated logic to overcome shift registers' limitations.
Here pre-charge is used to reduce the path delay and energy consumption overhead, and set-reset helps to increase the fault coverage. Finally, the Bit Swapping logic regulates the bit transition and switching activities. Modified dynamic current mode logic is introduced for implementing high-speed LFSR pattern generation, which includes power-down modes and provides a cost-effective solution to reduces static power dissipation.

However, all of the above-mentioned TPGs for area-efficient BIST implementations have some limitations like performance trade-off over fault coverage, insignificant testing power reduction, memory-related problems, etc. Moreover, CUT'S with random faults and conventional TPGs required more time and pattern length for 100% fault coverage. Therefore, it is essential to narrow down the existing LFSR design's complexity and memory space requirements without compromising the testing time and randomness characteristics.

3. Proposed Hardware Architecture

Fig. 1 shows the proposed clock-controlled LFSR-TRC test pattern generator. This system is initialized with the generation of three different clock signals using an all-digital phase-locked loop. Here both LFSR and TRC units are configured as a group of n flip-flops connected as a shift register. And these registers are acted as an n-bit ring counter for TRC and a cyclic shift register for LFSR, where the output is fed back to the input. TRC counter provides n distinct states with a binary inversion are performed between the outputs. Both TRC and LFSR units are driven by the initial value known as a seed. The randomness of LFSR is statistically pre-determined using polynomial configuration and seed values. At the same time, the n-bit TRC can provide 2^n distinct states based on seed value alone. During pattern generation, a slow rate clock is used to select the seed values to stimulate the LFSR chains that produce the pseudo-random test patterns. A mid-rated clock drives the LFSR bit shifting process to generate a maximum number of test patterns for given seed values without changing the polynomial configuration. The high-speed clock operates the TRC unit, which transforms the LFSR generated patterns into highly randomized pattern sets. Here TRC applies fine control over LFSR results, and the essential randomness characteristics of LFSR are regulated with appropriate changes in each individual block's operating clocks. Here, modulo two operations are used to transform compound LFSR test vector into multiple streams of random sets to perform fine toggle control with appropriate binary weightage selection by selectively fixing bits to specific logic values.

Procedure TPG();
Input: Random seed (∅) to LFSR and TRC
Output: Random test vectors.
begin
s=1 / seed index
∅ ← N; / seed selection
Initialize ADPLL
Clk => slow_clk1,mid_clk2,fast_clk3
@ (posedge slow_clk1)
LFSR, TRC ← ∅;
@ (posedge mid_clk2)
T1 = LFSR;
@ (posedge mid_clk2)
T2 <= TRC;
@ (posedge fast_clk3)
{Tg1, Tg2,...,Tgn}=Toggle_control{ T1 ⊕ T2};
Z← {Tg1, Tg2,...,Tgn};
return(Z);
end
3.1. Memory efficient seed computation

After polynomial computation, which follows conventional modulo-2 operations reseeding is performed as post computation to change the LFSR initialization to increase the pattern length and randomness. This process involves a large number of seeds that are stored in ROM. Here the only minimum number of seed values are pre-computed and stored in memory, and randomization is achieved through the post computation process. It will reduce the LFSR unit’s design complexity since all these ROM elements are converted into dedicated logical elements during FPGA hardware synthesis.

3.2. ADPLL clock generation

Here the flexibility of generating variable rate clock is performed using PLL with the least complexity overhead by deploying configurable delay elements for phase match. In order to retain LFSR randomness, it is essential to provide a multi-rate clock during the pattern generation process; this can be achieved through a reconfigurable clock divider that generated the sub clock into any integer multiples of the original clocks, and accordingly, each computation blocks controlled. Here, the voltage control oscillator unit is replaced with fully digitalized hardware to link the divided clock phases. Simply by placing delay elements, the phase difference can be controlled without causing any path delay overhead. Particularly, it helps increase operating speed, and these dynamic clock changes increase the randomization for detecting hard-to-detect faults.

4. Experimental Results

In this section, experiments are conducted on open-source benchmark CUTs from ISCAS ‘85 and ISCAS ‘89 circuits to prove the randomness and fault coverage metrics of the proposed hybrid TPG over conventional LFSR configurations such as LFSR reseeding and multi polynomial TPGs. Here pseudo-random sequence is generated to detect random combinational faults with 100% fault coverage. Here digital design is carried out using Verilog HDL, and its functionality is verified using ModelSim simulation as shown in Figure 2, and its metrics are evaluated using FPGA QUARTUS II hardware synthesis using CYCLONE III devices as shown in Table 1. The experimental results show that the proposed TPG model gives considerable path delay reduction with significant resource optimization level, as shown in Figure 3. Table 2 presents the results of the proposed TPGs hardware complexity comparison and its fault coverage metrics.

Figure 2: Multi-rate clock-driven test pattern generation simulation results.
Flow Summary

| Flow Status          | Successful - Fri Oct 09 02:47:00 2020 |
|----------------------|---------------------------------------|
| Quartus II Version   | 9.0 Build 132 02/25/2009 SJ Web Edition |
| Revision Name        | TDP                                   |
| Toplevel Entity Name | TOPMODULE                            |
| Family               | Cyclone III                          |
| Device               | EP3C16F484C6                         |
| Timing Models        | Frial                                |
| Met timing requirements | N/A                                 |
| Total logic elements | 42 / 15,406 (> 1 %)                  |
| Total combinational functions | 42 / 15,406 (> 1 %)                |
| Dedicated logic registers | 30 / 15,406 (> 1 %)                |
| Total registers      | 30                                    |
| Total pins           | 14 / 347 (4 %)                       |
| Total virtual pins   | 0                                     |
| Total memory bits    | 0 / 516,096 (0 %)                    |
| Embedded Multiplier 9-bit elements | 0 / 112 (0 %)          |
| Total PLLs           | 0 / 4 (0 %)                          |

**Figure 3**: Area summary

**Table 1**: Performance comparison of clock-driven TRC-LFSR with existing methods

| Test pattern generator (TPG) | Design parameters |
|------------------------------|-------------------|
|                              | Area (Logical Elements) | Frequency (f_{max}) | Power dissipation report |
| LFSR reseeding scheme        | 169                | 149.08 MHz          | 67.77mW                  |
| (reference [1])              |                    |                    |                          |
| Proposed TRC LFSR            | 42                 | 928.51 MHz          | 65.28mW                  |

**Table 2**: Performance metric comparison of proposed LFSR with state-of-the-art TPG methods

|                        | LFSR reseeding | Proposed TRC - LFSR | Test pattern reduction (%) |
|------------------------|----------------|---------------------|----------------------------|
| C880 (ALU and control) | 3423           | 1980                | 42.15                      |
| C1355 (xor gates)      | 1780           | 1123                | 36.81                      |

5. Conclusion

Variable-rate clock-driven TRC combined LFSR TPG presents here to narrow down the limitations of existing LFSR TPGs, such as the embedding of large sets of seeds and polynomial computations. The proposed schemes operate with three different clock signals generated from reconfigurable ADPLL LFSR and generate random patterns at a fast rate for reducing the testing time. Experimental results prove that the proposed TPG requires less memory space for seed storage than its counterpart model approaches while providing the same characteristics with improved randomness.
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