Fully Solution-Processed Flexible Organic Thin Film Transistor Arrays with High Mobility and Exceptional Uniformity

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Printing fully solution-processed organic electronic devices may potentially revolutionize production of flexible electronics for various applications. However, difficulties in forming thin, flat, uniform films through printing techniques have been responsible for poor device performance and low yields. Here, we report on fully solution-processed organic thin-film transistor (TFT) arrays with greatly improved performance and yields, achieved by layering solution-processable materials such as silver nanoparticle inks, organic semiconductors, and insulating polymers on thin plastic films. A treatment layer improves carrier injection between the source/drain electrodes and the semiconducting layer and dramatically reduces contact resistance. Furthermore, an organic semiconductor with large-crystal grains results in TFT devices with shorter channel lengths and higher field-effect mobilities. We obtained mobilities of over 1.2 cm² V⁻¹ s⁻¹ in TFT devices with channel lengths shorter than 20 μm. By combining these fabrication techniques, we built highly uniform organic TFT arrays with average mobility levels as high as 0.80 cm² V⁻¹ s⁻¹ and ideal threshold voltages of 0 V. These results represent major progress in the fabrication of fully solution-processed organic TFT device arrays.

Printed electronics has garnered significant attention from research and industry because the pairing of conductive, insulating, and semiconducting materials with printing technologies enables one to make thin, lightweight and low-cost electronic devices and systems. Organic semiconductors are particularly suitable for printed electronics because they can be processed in solution. Moreover, several promising solution-processable organic semiconductor materials have recently been reported. Organic materials possess intrinsic mechanical flexibility because of their loose Van der Waals bonding between organic molecules, and they make durable flexible organic devices feasible. In particular, flexible thin-film transistor (TFT) devices have recently been developed that have good electrical performance, low operating voltages, and operational stability.

Several novel applications using organic TFT devices or circuits have been developed for purposes such as flexible displays, RFID tags, sensors, and actuators. These devices have generally been fabricated using vacuum evaporation and photolithography; these mature processes are high resolution, repeatable, and uniform. Yet there are only a few reports on fully printed organic circuits or devices, and wide disparities exist in resolution, electrical performance, and device yield. There is also a wide variability in these device parameters in comparison with devices made using photolithographic processes.

When printed ink dries on the surface of a substrate, the solute is transported from the center to the edge, and the resulting solute film forms a non-uniform ring-like profile, a phenomenon known as the “coffee ring effect”. This effect makes it difficult for fully solution-processed organic electronic devices to be fabricated with high yields or operate at low voltages and with small variations in electrical performance. In addition, printed layers for use in electronic devices have typically possessed deficiencies, such as low conductivities, work functions that deviate from their bulk values, and rough or porous surfaces. These problems point to a need for comprehensive studies to be done before fully solution-processed organic electronic devices can be commercialized.

In this study, we fabricated an array of fully solution-processed organic TFT devices on flexible plastic substrates and obtained excellent electrical performance and high yields. The use of profile-controlled printed gate electrodes resulted in TFT devices with a very high yield rate (99%) and relatively low operating voltage (20 V). In addition, the use of a source-drain modification layer improved the contact between the electrodes and the semiconducting layers. The resulting TFT devices exhibited mobilities that exceeded 1.0 cm² V⁻¹ s⁻¹ in ambient.
air and a low contact resistance (1.8 kΩcm) at gate-source voltage of 20 V. The high yields enabled us to conduct statistical analyses of many solution-processed organic TFT devices produced on the same flexible substrate. The analysis revealed a normal distribution in electrical performance, and this information can be used to simplify the circuit design for fully solution-processed organic electronics.

**Results and discussion**

Fabrication of organic TFT device arrays on plastic films. Fully solution-processed organic TFT devices were fabricated in a 10 × 10 array on 125-µm-thick polyethylene naphthalate (PEN) films with a maximum process temperature of 150 °C. Figure 1 shows a schematic illustration and photographs of the TFT device. New materials developed by Merck were employed for the organic semiconductor, gate dielectric, and electrode treatment layers. For the electrodes, two formulations of silver nanoparticle ink were used, one for the gate electrodes, in order to form flat surface profiles, the other for the source/drain electrodes, to improve carrier injection into the semiconducting layer. Apart from these materials, cross-linked poly-4-vinylphenol (PVP) and fluoropolymer were used for the planarization layer and bank layer, respectively. An ink-jet printing system and dispenser equipment were used to pattern these materials.

To reduce their surface roughness, the PEN substrates were coated with a 80-nm-thick cross-linked PVP layer, which was deposited using a spin-coating process and cured at a temperature of 150 °C. The surface of the cross-linked PVP layer was treated using an oxygen plasma to change the surface wettability. Silver nanoparticle ink was patterned with an inkjet printer onto the cross-linked PVP layers to form the gate electrodes. Following printing, the substrates were stored under controlled temperature and relative humidity conditions in order to planarize the printed electrodes. After the drying process, the substrates were heated at 140 °C for 1 hour to sinter the silver nanoparticles. The fabricated silver gate electrodes had uniform thicknesses of about 100 nm. After forming these electrodes, a solution of dielectric polymer materials was spin-coated to form 600-nm-thick gate dielectric layers. After spin coating the dielectric layers, the substrates were heated at 120 °C for 1 min on a hotplate, and then cross-linked by using a UV treatment. A separate silver nanoparticle ink was then patterned using an inkjet printer to form the source/drain electrodes, which defined the TFT device geometries. The source/drain electrodes were treated using a self-assembled monolayer (SAM), which was prepared by immersing the substrate for 1 min. 200-nm-thick fluoropolymer bank layers were then printed by using dispenser equipment. The bank layers were used for separation of the semiconducting layers between devices. Finally, a p-type organic semiconducting layer was deposited using dispenser equipment into the area defined by the bank layer, which was then baked at 100 °C for 1 min on a hotplate. The ionization potential of the layer used in this study was 5.4 eV. We fabricated several individual TFT devices, which had differing channel widths and lengths. The channel width and length in the array were 1061 ± 8 and 22 ± 5 µm, respectively (see supporting figure S3). The details of the processing can be found in the methodologies section.

**Organic TFT device characterization.** Figure 2a shows the transfer characteristics of the fabricated TFTs, having the same W/L ratio of 50, with and without applying a SAM treatment to the source-drain electrodes. The SAM modification process improved the transistor electrical characteristics dramatically, whereby on-current increased from 1.6 µA to 27 µA and the estimated mobility the in saturation regime increased from 0.02 cm² V⁻¹ s⁻¹ to 0.9 cm² V⁻¹ s⁻¹. We also observed the crystallinity of semiconducting layer between source/drain electrodes with a polarization microscope, as shown in Figure 2b. Both devices had nearly identical crystalline domains, even though there were large differences in mobility between the devices with the SAM treatment and those without it. The experimental values summarized in Table 1 are the work functions of the treated and untreated silver electrodes measured by using photoemission spectroscopy and their surface energies estimated with the Owens-Wendt method. The work function changed from 4.7 eV before the SAM treatment to 5.3 eV after, but the surface energy did not change.

The carrier injection barrier at the interface between the metal and organic material layers is commonly described by conventional metal-to-semiconductor contact mechanisms. The addition of a carrier injection layer to reduce the energy barrier between the

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**Figure 1** Fully solution-processed organic thin-film transistors on flexible substrates. (a) Schematic cross-section of the TFTs. (b) Photograph of a 10 × 10 TFT array on a flexible PEN substrate. (c) and (d) Optical microscope images of the TFT array.
Figure 2 | Effect of source-drain electrode modification by SAM treatment on transistor characteristics. (a) Transfer characteristics of fabricated TFTs. The black lines represent the transfer curve for the device without the SAM treatment, and the red lines those with the SAM treatment. Both transistors had almost the same W/L ratio (~50). (b) Polarization microscope images of channel region of fabricated TFTs with untreated and (c) with treated electrodes.

Table 1 | Measured work function, surface energy, and transistor characteristics of treated and untreated silver electrodes

|          | Work function (eV) | Surface energy (mN m⁻¹) | μ (cm²V⁻¹ s⁻¹) | On-current (μA) |
|----------|--------------------|-------------------------|---------------|---------------|
| With SAM | 5.3                | 30.7                    | 0.9           | 27            |
| Without SAM | 4.7               | 33.1                    | 0.02          | 1.6           |

Figure 3 | Estimation of contact resistance. The contact resistance of the TFT devices with treated source-drain electrodes were estimated by using the transfer-line method. (a) Channel width-normalized total on-resistance (R_ON) as a function of channel length. (b) Width-normalized contact resistance as a function of gate-source voltage (V_GS).

Dependence of TFT electrical characteristics on channel length. Next, we evaluated the dependence of the electrical performance of fabricated TFT devices on the channel length. Figure 4a shows the field effect mobility of the TFT devices with SAM-treated source/drain electrodes in the saturation region as a function of channel length. These plots clearly show a correlation between the channel length and mobility, such that mobility decreases almost linearly with channel length between 10 μm and 150 μm. A fitted regression line has negative slope and a correlation coefficient R² of 0.57. In general, the mobility of organic TFTs decreases as the channel length decreases below 20 μm because of large contact resistance values²⁴.²⁵. Gundlach reported a similar channel length dependence in organic TFTs with solution-processed semiconductors and discussed the
Figure 4 | Dependence of field-effect mobility in saturation region on channel-length. (a) Mobility as a function of channel length. The black dots represent the experimental data, and the solid line is a fitted curve. (b)–(e) Polarization microscope images of the channel region of fabricated TFTs. The channel length and mobility are as follows: (b) 110 \( \mu \text{m} \) and 0.81 cm\(^2\) V\(^{-1}\) s\(^{-1}\), (c) 110 \( \mu \text{m} \) and 0.34 cm\(^2\) V\(^{-1}\) s\(^{-1}\), (d) 20 \( \mu \text{m} \) and 1.23 cm\(^2\) V\(^{-1}\) s\(^{-1}\), (e) 140 \( \mu \text{m} \) and 0.45 cm\(^2\) V\(^{-1}\) s\(^{-1}\).

Mechanical and operation stability. To demonstrate the flexibility of the fabricated devices, tensile strains were applied to the organic TFT devices. The strains were parallel to the source-drain current paths, and the electrical performances of the devices were evaluated before, during, and after the application of strain. We applied bending strains with radii (R) ranging from 11 mm to 4 mm, corresponding to an induced surface strain from 0.57% to 1.6%. The electrical behavior of the devices was characterized during the systematic application of tensile strain. Figure 5a shows the transfer characteristics of a device with a channel length of 60 \( \mu \text{m} \). The gate voltage \( V_{\text{GS}} \) was swept from 10 to \(-20\) V while \( V_{\text{DS}} \) was kept at \(-20\) V. In agreement with previous reports, this fully printed device exhibited a decrease in saturation on-current \( I_{\text{DS}} \) upon the application of tensile strain\(^{51-53}\). The transfer characteristics completely returned to the initial state after the tensile strain. The change in the on-current was \(-15\%\) at 1.6% tensile strain. The normalized on-current is plotted as a function of tensile strain in Figure 5b. The current change was linearly proportional to the applied surface strain. This indicates that the origin of the current change in fully printed organic TFT devices under strain is essentially the same as that of the evaporated organic TFT devices\(^{51-53}\). A stress cycle was also applied to the TFT devices. First, the device was bent upwards from a flat state into one with a 6.25 mm radius which corresponded to a 1.0% tensile strain, and was immediately released to unbend back into the flat state. After that, the FET was bent downwards to \( R = 6.25 \) mm and released. The bending cycle was repeated at a rate of 30 times a minute. Figure 5c plots the normalized \( I_{\text{DS}} \) as a function of the number of outward bending cycles. Even after 1000 full cycles, the change in on-current amounted to less than 5%. This excellent flexibility is attributed to the strong fusion of the electrodes with the underlying dielectric surfaces and semiconducting layers. These results show the feasibility of using fully printed electronic devices in flexible systems.

We also evaluated the operational stability of the devices. We estimated the change in threshold voltage (\( \Delta V_{\text{TH}} \)) as the devices were...
Organic TFT array characterization. A fully solution-processed organic TFT array (10 × 10 layout) was fabricated on a 40 mm × 40 mm PEN film, and 99% of the fabricated TFT devices functioned well. The high yield was largely the result of fully solution-processed gate electrodes with flat profiles, and it enabled a statistical combination of dielectric layers.

The on-current was normalized by its initial value. (c) Mechanical durability during repeated 1.0% tensile strain and relaxation. Even after 1000 cycles, the change in on-current was less than 5%.

Figure 6 | Operational stability. (a) Transfer characteristics of the device taken before and after continuous application of bias voltage (V_{GS} = V_{DS} = −20 V). The black lines represent the results before applying bias stress, the blue lines represent those after applying bias stress for 10^5 s, and the red lines represent those after applying bias stress for 10^6 s. (b) Threshold voltage shift (ΔV_{TH}) as a function of time while applying continuous bias voltages (V_{GS} = V_{DS} = −20 V). The black circles represent the experimental results, and the red dashed line is the fitted curve.

Figure 5 | Mechanical flexibility of fully solution-processed organic TFT devices. (a) Transfer characteristics of pentacene-based TFT device before (gray solid line), during (red solid line), and after (blue dashed line) application of 1.6% tensile strain. The on-current was normalized by its initial value. (b) Change in current as a function of tensile strain. (c) Mechanical durability during repeated 1.0% tensile strain and relaxation. Even after 1000 cycles, the change in on-current was less than 5%.
in two dimensions with the intensity of the color representing the measured performances. These plots indicate that the variations in device performance appear randomly on the same substrates.

The remaining variations in performance of devices within the array were caused by differences in the crystallinity of the semiconducting layer. Indeed, the crystallinity varied from device to device (see supporting Figure S2), and this indicates that the crystal growth of the solution-processed organic semiconducting layer should be more precisely controlled in order to achieve uniform electrical characteristics. In addition, deviations in critical device dimensions such as the channel length and channel width were responsible for some of the variation. Both the channel width and length followed statistically normal distributions (see supporting Figure S3). Interestingly, mobility and threshold voltage also followed normal distribution curves, as shown in Figures 7c and 7d, despite the variations in the crystallinity of the semiconducting layer. These variations (standard deviations) in performance across TFT devices could be suppressed by better controlling the device dimensions. The high performance and relatively high uniformity of our fully solution-processed organic TFT device arrays demonstrate the feasibility of using them in the design of reliable digital logic circuits.

**Conclusion**

We fabricated organic TFT arrays on plastic film substrates by using solution processes performed on ink-jet printer and dispenser equipment. The results of our study demonstrate the tremendous potential that exists for printed electronics. By making improvements to the materials, modifications to the design of the electrodes, and forming uniform and flat electrodes, we can fabricate fully solution-processed organic TFT arrays with a high yield and excellent electrical characteristics at low operating voltages. Our results show a clear correlation between the semiconductor layer’s crystallinity and the channel length with the electrical performance of the organic TFTs. The statistical analysis of the TFT array obtained useful data for designing organic TFT devices and circuits for practical applications. These fabrication methods will help enable novel low-temperature, low-cost, large-area manufacturing of printed electronics.
Methods

Device fabrication. A 125-μm-thick PEN film (Teijin DuPont Films, Teone®) was used as the flexible substrate, and cross-linked PVP was used as the planarization layer. PVP (Mw ~ 250000, Sigma Aldrich Co.) and poly(methyl methacrylate-co-ethyl acrylate) (Mn ~ 432, 84 wt%, Sigma Aldrich Co.) as a sintering agent were mixed in propylene glycol monomethyl ether acetate (PGMEA). The PEN substrates were stored in air ambient for 10 min to evaporate the solvent from the bank layers. After printing of the bank layer, the substrates were used as the flexible substrate, and cross-linked PVP was used as the planarization layer was then treated for 1 min with oxygen plasma (plasma power of 100 W) to change the surface wettability. Silver (Ag) nanoparticle ink in aqueous solvent (DIC Corp., JAGLT-01) was patterned with an inkjet printer coated with an 80-nm-thick cross-linked PVP layer to reduce the surface roughness, propylene glycol monomethyl ether acetate (PGMEA). The PEN substrates were used as the flexible substrate, and cross-linked PVP was used as the planarization layer.

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Author contributions
K.F., Y.T. and M.M. carried out experimental work and data analysis. K.F., D.K. and S.T. conceptualized the research and wrote the manuscript.

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