Effect of Process-Related Impurities on the Electrophysical Parameters of a MOS Transistor

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Abstract—It is established that the electrophysical characteristics of MOS transistors largely depend on the quality of a gate dielectric. The presence of an extra built-in charge in the dielectric and fast surface states at the SiO₂/Si interface leads to both an increased threshold voltage and decreased saturation current and voltage, decreased slopes of the characteristics of the MOS transistor in the linear and saturation regions, and a decreased structure conductance in the linear region. The gate leakage currents also increase. It is shown that the view and shape of the capacity–voltage characteristics are determined by the value of an extra positive charge in the bulk of the dielectric and the density of fast surface states at the Si/SiO₂ interface. These values are correlated to the profile of the distribution of the surface concentration of the process-related impurities adsorbed at the wafer surface during the manufacturing of the device, which allows us to judge the quality of the materials used, adherence to the production conditions, and, if necessary, correct them opportunistically as required.

Keywords: MOS transistor, dielectric, surface states, leakage current, interface

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INTRODUCTION

In the production of CMOS structures, a large number of production steps are required, especially when MIS technology is used [1–3]. Manufacturing quality control is a constituent part of the typical manufacturing process and is reduced to the determination of two components: obvious defects characterizing the yield of the device and latent defects reducing their reliability. The aim of the production control is not only to obtain the desired quality of devices but also to timely reject the defective items at different steps of the production of the device.

The choice of the chemical reagents and assignment of such a sequence of production operations, in particular, high-temperature ones, which would preclude uncontrolled (process-related) impurities falling into a semiconductor structure as far as possible, is critically important. The changes in the parameters of a manufacturing process, taking place as the characteristic size of a transistor becomes smaller, should not lead to a decrease in the yield of the device.

As a result of this, revealing the reasons for the labile reproducibility of the main characteristics of MOS transistors in order to establish the factors determining the reliability and stability of the performance of integrated microcircuits is a topical task. One of the reasons for the degradation of the electrophysical parameters of MOS transistors is the contamination of a silicon substrate with process-related impurities during the manufacturing process. To check these suppositions, we investigated the MOS structures using the technique of current–voltage (I–V) characteristics and high-frequency capacity–voltage (C–V) characteristics, and measured the concentration of the process-related impurities both on the surface and in the bulk of silicon wafers.

OBJECTS AND METHODS OF RESEARCH

Using an Agilent B1500A semiconductor device parameter analyzer with a Cascade Summit1100 probe station, the I–V and C–V characteristics of two batches (A and B, hereinafter) of n-channel MOS transistors produced via the same process routes with the same process materials, but at different times, were measured. Pockets of MOS transistors 70 × 70 μm in size were created on p-type silicon wafers with a resistivity of 10 Ω cm by ion-implantation doping with boron (BF₂) for the p pocket, and phosphorus and arsenic doping for the n pocket. The size of a polysilicon gate of a transistor doped to degeneracy was 10 × 10 μm. The gate dielectric’s (SiO₂) thickness was
7 nm. The C–V characteristics were measured at a frequency of \( f = 1.0 \) MHz with the voltage (\( U \)) sweep from –5 to +3 V at a step of 50 mV for testing on the \( p \) pocket, and, at the voltage of ±3 V and the same step for testing on the \( n \) pocket. The content of metal impurities on the wafer’s surface was investigated by the total external reflection of the X-ray radiation on the setup [4, 5].

RESULTS AND DISCUSSION

Comparing the output \( I–V \) characteristics of the MOS structures (Fig. 1) revealed that the transistors of batch B have both higher drain current \( I_D \) values in the saturation mode and higher pinch-off voltages \( U_{p-off} \).

For instance, at the gate voltage of \( U_G = 3.3 \) V, the drain current for B-batch devices is \( I_D = 0.3 \) mA, and the analogous value for A-batch devices is 0.14 mA. The pinch-off voltage \( U_{p-off} \) is 2.1 and 1.4 V, respectively.

If the electron mobility \( \mu_n \) does not depend on the electric field strength, the saturation current \( I_{Dsat} \) in the channel with width \( W \) of an insulated-gate field-effect transistor is determined as follows [6]:

\[
I_{Dsat} = \frac{1}{2} \mu_n W C_{SC} (U_G - U_{thr})^2, \tag{1}
\]

where \( C_{SC} \) is the dielectric specific capacitance and \( U_{thr} \) is the threshold voltage starting from which the charge in a semiconductor induced by the gate is determined by mobile charge carriers; and, consequently, a conductive channel (with a characteristic width of ~100 Å) appears in the semiconductor’s near-surface layer.

At constant \( U_G \), according to (1), and a constant ratio of the channel width \( W \) to its length \( L \), the observed differences in the \( I_D \) value are firstly due to the change in the pinch-off voltage \( U_{p-off} = U_G - U_{thr} \). Since the ratios of the experimental values

\[
\frac{I_C^B}{I_C^A} = 0.30 \text{ mA} / 0.14 \text{ mA} = 2.14
\]

and

\[
\left( \frac{U_{p-off}^B}{U_{p-off}^A} \right)^2 = (1.7 \text{ V} / 1.2 \text{ V})^2 = 2.01
\]

\((U_G = 3.3 \) V) for the A-batch and B-batch devices are correlated to each other closeley and agree with (1), we can conclude that the differences between the values \( I_D \) and \( U_{p-off} \) for the A-batch devices and those for the B-batch devices are caused by the same reason, which, apparently, determines the threshold voltage value \( U_{thr} \)

\[
U_{thr} = 2\psi_B + \frac{2e_g N_A (2\psi_B)}{C_{SC}}, \tag{2}
\]

where \( \psi_B \) is the difference in the Fermi level in the employed material and the intrinsic semiconductor and \( N_A \) is the doping impurity concentration of the \( p \) substrate. It follows from (2) that the reason for the change in \( U_{thr} \) (on condition that the substrate is doped uniformly) is the change in \( C_{SC} \) due to the uncontrollable charge localized in the region of the MOS capacitor (gate). From analyzing the \( I–V \) characteristics, a series of other important parameters of the MOS structure was determined: the saturation current, the drain current, the MOS transistor’s conductivity in the linear region of the \( I–V \) characteristic, the slope of the characteristic of the MOS transistor in the linear region, and the slope of the characteristic of the MOS transistor in the saturation region (Table 1).

For A-batch transistors, the values of the saturation current and voltage, the slopes in the linear and saturation regions, and the conductance in the linear region are smaller than those for the B-batch transistors. The threshold voltage value for the A-batch transistors is higher than for the B-batch transistors. This
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indicates that the B-batch MOS transistors have a higher performance than those of the A-batch transistors.

One of the possible reasons for the differences in the parameters of the two batches of MOS transistors is also likely to be the capacitance and quality of the gate dielectric, which are determined by the built-in charge. To check this supposition, ratios between the capacitances of the gate dielectrics of MOS transistors from different batches ($C_A / C_B$), which were determined in agreement with [7, 8] in different regions of the $I–V$ characteristics based on the conductance in the linear region, the slope of the characteristic in the linear region, the saturation current value, and the slope in the saturation region, were compared (Table 2).

From Table 2 it follows that, irrespective of the technique used for estimating the $C_A / C_B$ ratio, the $C_B$ capacitance is larger than the $C_A$ capacitance by about 20%, which is unambiguous evidence of an extra charge [2, 6, 7, 9] built into the oxide layer of the gate dielectric of the A-batch MOS transistors. This is due to the fact that, at the Si/SiO$_2$ interface obtained by silicon thermal oxidation, there always exist four different types of charge sources: the charge of fast surface states in a semiconductor, the constant charge in an oxide, the charge on traps in an oxide layer, and the charge of mobile ions.

The energetic density of the fast surface states located immediately at the Si/SiO$_2$ interface greatly depends on the conditions of obtaining an oxide. The value of the constant charge in an oxide depends on the oxidation and annealing conditions, a type of pre-oxidation treatment of silicon wafers, and contamination of the Si/SiO$_2$ system with cationic impurities. The charge on traps in an oxide layer is the space charge captured by the energy levels of the defects in SiO$_2$. This charge type is associated with slow surface states. The charge of mobile ions is due to the presence of alkali-metal ions (Na$^+$, K$^+$, Li$^+$) and heavy-metal ions in the oxide, which penetrate into it from the environment and the materials used in the manufacturing process. Other constituents of the charge can be protons and H$_3$O$^+$ ions, the ions adsorbed on the surface, oxygen vacancies, traps in the oxide, and polar molecules entering the oxide from the environment and the materials used in the manufacturing process. The surface density of these charges is typically $10^{10}$ to $10^{12}$ cm$^{-2}$.

Investigations of the gate dielectric leakage current versus the gate voltage established that the current through the gate dielectric for the B-batch structures is smaller by a factor of about 5 than the corresponding current for the A-batch structures (Fig. 2). The experimental data are evidence that the electric resistance of the gate dielectric films for the B-batch structures is higher than that for the analogous A-batch structures. Another reason for the observed differences in the leakage current through the dielectric for the A- and B-batch devices is probably the substantial contamination of the gate dielectric of the A-batch devices with the process-related impurities during the manufacturing of the device.

Additional data on the quality of the gate dielectric were obtained from analyzing the capacity—voltage characteristics of MOS structures (Fig. 3). For A-batch devices, in the case of measurements on the $n$ pocket, a shift in the characteristics along the voltage axis toward more negative values is observed. For devices of this batch, this is evidence of the presence of an extra immobile effective positive charge, the charge

### Table 1. Parameters of MOS transistors determined from analyzing current–voltage and drain characteristics

| Parameters of MOS transistor | A batch | B batch |
|-----------------------------|---------|---------|
| Saturation current $I_{Dsat}$ at $U_G = 3.3$ V, μA | 138 | 280 |
| Saturation voltage $U_{DSsat}$, V | 1.20 | 1.90 |
| Threshold voltage $U_{thr}$, V | 1.25 | 0.76 |
| Slope of characteristics of MOS transistor in linear region at $U_{DS} = 0.2$ V, μA/V | 19 | 22.1 |
| Slope of characteristics of MOS transistor in saturation region at $U_{DS} = 2.9$ V | 100.3 | 175 |
| Conductance of MOS transistor in linear region at $U_{GS} = 0.2$ V, μA/V | 174 | 274 |

### Table 2. Ratio between specific capacitances of gate dielectric in A- and B-batch transistors

| Method of determination | Gate and drain voltages | $C_A / C_B$ |
|-------------------------|-------------------------|-------------|
| From conductance        | $U_{DS} = 0.2$ V, $U_{GS} = 3.3$ V | 0.79 |
| From slope in linear region | $U_{DS} = 0.2$ V | 0.86 |
| From saturation current | $U_{GS} = 3.3$ V | 0.76 |
| From slope in saturation region | $U_{DS} = 3.5$ V, $U_{GS} = 2.9$ V | 0.75 |
states of which are located in the bulk of the dielectric and cannot be recharged during the experiment due to the small electronic conduction of the dielectric. In addition, in the curves of the capacity—voltage characteristics for both A- and B-batch devices, there is a peak typical of the low-frequency C–V characteristics (Fig. 3a). This is caused by the fact that the surface states located in the vicinity of the middle of the band gap have relaxation times of 1.0 to 10 μs, and the surface states located in the vicinity of the allowed bands (conduction band and valence band) have relaxation times of ~0.01 to 1.0 μs, and the frequency dependence of the C–V characteristics for them shifts to a higher frequency range. The difference in the slope of the curves for both batches of devices is caused by the differences in the capacitance and voltage of the flat bands, which were, respectively, 19.72 pF and 0.174 V for the B-batch devices, and 21.08 pF and 0.213 V for the A-batch devices.

The capacitance and voltage of the flat bands measured on the p pocket for the B-batch devices are, respectively, 21.78 pF and −1.05 V, and, for the A-batch devices, these values are 21.72 pF and −1.22 V. The shift in the curves of the C–V characteristic along the voltage axis in this mode of measurements was insignificant (Fig. 3b). The shift relative to the theoretical curve was nearly the same for both types of devices, which indicates that the values of an immobile extra charge in the dielectric are nearly the same. The difference in the slopes of curves for devices of different B batches arises from the difference in the density of fast surface states, as in the case of the investigations on the n pocket. The largest discrepancy in the C–V characteristics measured on the p pocket for the A- and B-batch devices is observed in the inversion region (Fig. 3b), while, in the enhancement region, the curves almost coincide. This leads us to conclude that the difference in the density of fast surface states is the largest for the centers which have energy levels in the upper part of the band gap. Inasmuch as the surface states are located at the top of the band gap and are donor states, they are neutral when being filled with electrons and charged when being empty. In addition, for a number of MOS structures in the case of measurements on the p pocket for B-batch devices, there is the peak characteristic of the low-frequency C–V characteristics (curve A'). This is evidence that the devices of this batch, unlike the B-batch devices, contain fast surface states with relaxation times shorter than 1 μs, as a result of which the generation of minority carriers and filling of surface states manage to keep pace with the changes in the external voltage. Note that the peak in the curves of the C–V characteristics was not observed for all the A-batch devices (Fig. 3b) (curves A and A', the experiments were carried out at more than 20 points across the wafer’s surface), which suggests that the distribution of fast surface states across the wafer’s surface is nonuniform.
Taking into account the fact that these states can be due to the presence of alkali-metal ions (Na⁺, K⁺, Li⁺) and heavy-metal ions in the oxide, H₂O⁺ ions, ions adsorbed on the surface, oxygen vacancies, traps in the oxide, and polar molecules entering the oxide from the environment and the materials used in the manufacturing process, we investigated the distribution of varied process-related impurities across the surface of the wafers.

The topograms of the distribution of process-related impurities across the surface of wafers on which the A-batch devices were produced are shown in Fig. 4.

There are local areas containing Cl (1.2 × 10¹² atoms/cm²), K (1.6 × 10¹¹ atoms/cm²), and Ca (7.4 × 10¹⁰ atoms/cm²), as well as Ti, Cr, Cu, Zn, and other impurities. The entire wafer surface is covered with Fe at the average concentration of 2.0 × 10¹¹ atoms/cm², with the distribution of this impurity across the wafer surface being appreciably nonuniform. The typical distributions of the process-related iron impurity across the wafer surface are shown in Fig. 5. Note that this process-related impurity has quite a negative effect on the breakdown voltage of the gate silicon dioxide 3 to 10 nm thick. Thus, at the iron concentration in the bulk higher than 5 × 10¹¹ atoms/cm³, a sharp decrease in the field strength causing a breakdown of the gate silicon dioxide occurs [10].

On the topograms of the wafers on which the B-batch devices were produced, only local areas with the elevated Cl content at the wafer’s periphery are observed. The content of all the other impurities was lower than the detection limit (Fe < 4.0 × 10⁹ atoms/cm²). The number of particles captured by the surface at the given temperature is determined by their physicochemical properties and concentration at the initial surface. An increase in the number of adsorbed particles, as a rule, leads to an increase in their concentration in the oxidized samples and, as a consequence, a change in the energetic density of the fast surface states, the value of the constant charge in the oxide, the charge on traps in the dielectric layer, and the charge of the mobile ions.

During the thermal oxidation of silicon and other high-temperature production operations used in manufacturing devices, many uncontrolled impurities adsorbed on its surface desorb partially and partially pass into the silicon/silicon dioxide system, changing its electrophysical properties. An extra positive charge is formed in the dielectric layer, and the density of fast surface states at the Si/SiO₂ interface, distributed nonuniformly across the wafer surface, increases. Their density is correlated to the surface concentration of the process-related impurities adsorbed on the wafer’s surface during the manufacturing of the device.

CONCLUSIONS

The investigations carried out revealed that the uncontrolled extra charge located in the gate region of the MOS transistor is largely determined by the presence of the process-related (background) impurities falling into the semiconductor’s structure during pro-
duction or that are present in the initial semiconductor crystal. The presence of an extra built-in charge in the dielectric, as well as the fast surface states at the SiO₂/Si interface, leads to both the increased threshold voltage and the decreased saturation current and voltage, the decreased slopes of the characteristic of the MOS transistor in the linear and saturation regions, and the decreased structure conductance in the linear region. The gate leakage currents also increase. It is demonstrated that measurements of the capacity–voltage characteristics of MOS structures allow one to control the quality of the gate dielectric. The view and shape of the measured characteristics are determined by the value of the extra positive charge in the bulk of the dielectric and the density of the fast surface states at the Si/SiO₂ interface. These values are correlated to the profile of the distribution of the surface concentration of the process-related impurities adsorbed at the wafer’s surface during the manufacturing of the device, which allows us to judge the quality of the materials used, adherence to production conditions, and, if necessary, correct them opportunistically as required.

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