The WaveDAQ integrated Trigger and Data Acquisition System for the MEG II experiment

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Abstract—The WaveDAQ is a newly-designed digitization Trigger and Data Acquisition system (TDAQ) allowing Multigigasamples waveform recording on a large amount of channels (up to 16384) by using the DRS4 analog switched capacitor array as downconverting ASIC. A high bandwidth, programmable input stage has been coupled with a bias generator to allow SiPM operation without need of any other external apparatus. The trigger generation is tightly coupled within the system to limit the required depth of the analog memory, allowing faster digitization speeds. This system has been designed for the MEG experiment upgrade but also proved to be highly scalable and already found other applications.

I. INTRODUCTION

The MEG experiment [1] pioneered the use of multigigasample digitizer to achieve the stringent timing and charge resolutions needed to disentangle the high pileup environment the detectors face. In the framework of the global upgrade plan [2], that aims to a factor 10 higher sensitivity on \( \mu^+ \rightarrow e^+\gamma \) (current limit was set by MEG to \( BR < 4.2 \cdot 10^{-13} \) at 90% CL), a global redesign of the trigger and data acquisition systems was needed. In particular the number of channels increased by a factor of 4 by switching from PMTs to SiPMs while the electronics had to fit in the same rack space. Built on the experience gained with the former Trigger [3] and DAQ [4] systems, the new WaveDAQ can exploit the features of DRS4 analog switched capacitor array to an unprecedented level, in particular the readout time will be decreased by moving from the VME standard to gigabit ethernet interfaces and by merging the two former systems in a single, tightly integrated system to ease the interplay.

II. SYSTEM DESCRIPTION

While designing the new system no available standard delivered the required compactness, connection topology and clock distribution requirements. Therefore, a system with a fully custom backplane had to be designed. This system features a fully custom backplane with dual-star serial link capability and a skew-compensated low jitter clock distribution. In a standard 3U rack format, 16 slave boards are connected to the two central slots for trigger and data processing as shown in figure [1] where we also highlighted the various connections between the boards fully described in the next sections.

The crate housekeeping is accomplished by a microcontroller board integrated into the 360W crate power supply, rightmost in picture [1] that handles the shared power lines and the temperature-controlled fans while providing a low level interface to the boards in the crate for slow control and configuration though a dedicated Ethernet network connection.

A. WaveDREAM Frontend Board

Usually slave positions in a crate are occupied by the Waveform Drs4 REadout Module (WaveDREAM), pictured in figure [2]. That board contains two DRS4 chips, capable of 0.5-5 GSPS sampling speeds, together with 900MHz bandwidth variable gain amplifiers to allow direct connection of detector signals. The same 80MSPS ADC used to digitize analog amplitudes stored in the DRS4 will provide also an independent sampling while the analog digitizer is running, to be used inside the trigger logic in combination with fast analog comparators. The information from the analog comparators is also fed to a time to digital conversion logic implemented in the readout FPGA by means of high speed shift registers to result in low resource usage while achieving 450ps time resolution, limited by the fastest available clock in the FPGA. A voltage bias generator may provide channel-by-channel biasing for single SiPM or for multi-SiPM arrays without requiring any external power supply. When inside the crate up to 256 channels on 16 boards can be digitized simultaneously.

The WaveDREAM can be used outside a crate using the onboard Gbit Ethernet interface. In this configuration a single board provides a benchtop DAQ platform with 16 acquisition channels.

B. Data Concentrator Board and Trigger Concentrator Board

The two central slots in a crate are reserved for custom designed boards that take care of crate-level functions mandatory for multi-board DAQ operation:

- The Data Concentrator Board (DCB), figure [3] generates and distributes the main reference clock while handling the data received by WaveDREAMs, combining them into
Fig. 1. Sketch of a single WaveDAQ crate: green boards are WaveDREAM frontend boards, the magenta board is the Data Concentrator Board and the blue board is the Trigger Concentrator Board. Arrows show connections in the backplane: red arrows for data transmission to backend machines, blue arrows for trigger serial links, orange arrows to distribute back the trigger signal and green arrows for hardware compensated clock distribution. Brown arrows show low level access for slow control and configuration.

Fig. 2. WaveDREAM board housing DRS4 digitizers, ADCs and TDCs for trigger. The ethernet plug on the back may not be populated when used inside a crate. The piggy back HV module is not shown in picture.

a single Gigabit Ethernet interface. The onboard Zynq SystemOnChip acts as master of the crate, handling the interface to the other boards for configuration.

- The Trigger Concentrator Board (TCB), figure 3b, receives all trigger informations from the WaveDREAMs using low-latency serial links to generate a shared trigger signal when amplitude and time based algorithms detect an event of interest. All online selection strategies for MEG II will be based on the ones used in MEG with the necessary modifications and improvements by the different detector segmentations.

C. Use in experiments

In experiments which require more than 256 channels, a shared trigger generation and distribution is necessary. trigger generation, a dedicated so-called trigger concentrator crate filled with TCBs in slave and master positions can collect data from TCBs sitting in up to 64 crates by using high speed serial cables on the front panel. The TCB in the master position of the trigger concentration crate can receive trigger informations from all boards in the system and eventually generate the trigger signal.

Another crate, using fanout cards, will account for the clock generation and the trigger signal distribution. Using such a design 16384 channels can fit in ten 21U racks, resulting in more than 4 times the channel density achieved in MEG.

III. Prototype operation

Several tests with prototype systems were performed during the last two years, ranging from single board tests, for signal checks or small detector tests, to 6-crate multi-detector systems used during beam tests of the upgraded detectors. One of those systems is shown in figure 4. Even if smaller than the final MEG II system, lots of features such as board synchronization, busy handling and trigger communications have been studied and optimized in this setup before the final system production.

The two crate system of picture 4 showed very good timing characteristics when tested with the new MEG II Timing Counter detector[6], made by scintillating tiles readout by SIPMs: the electronics contribution have been measured to be of the order of 10 ps and have proved to be stable over a few month period. During the beam test period the Timing Counter detector has achieved its goal of about 35ps time resolution on positron tracks without being limited by digitizer performances (for details see [2]).

During the same test beam four crates have been devoted to readout a subset of the Liquid Xenon detectors [7], so that the full trigger reconstruction, involving pedestal-subtraction,
weighted sum and discrimination with veto, has been tested and proved to generate a trigger within 700ns, as visible from the recorded DRS4 waveform shown in figure [3]. Using such logic we succeeded in selecting beam-induced photon events, cosmics, and other photon calibration sources. The latency will be improved by $\sim 200\text{ns}$ in the next WaveDREAM board revision by using an ADC with a shorter pipeline.

Outside the MEG experiment, a single crate system has been chosen to readout the dE/TOF Detector of the FOOT Experiment [8], few prototypes have been tested with single-board DAQ, achieving the required timing and charge performance.

IV. CONCLUSION

We showed a new digitizing Trigger and Data Acquisition system being assembled for the MEG II experiment. The system allows the use of several DRS4 digitizers on a large number of channels and is easy to scale from a 16 channel single board setup to $\sim 16000$ channels. Several configurations involving smaller size systems have been tested and all underlying functionalities have been proved to be operational.

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