Impact on Current-Interrupting Characteristic by Parameter Settings of Superconducting Hybrid DC Circuit Breaker

Sang-Jae Choi and Sung-Hun Lim *

Article

Department of Electrical Engineering, Soongsil University, 369, Sangdo-ro, Dongjak-gu, Seoul 156-743, Korea; choijsj203@soongsil.ac.kr
* Correspondence: superlsh73@ssu.ac.kr; Tel.: +82-2-828-7268

Abstract: DC faults cause severe disruption in not only the DC system but also the AC system because the fault current is very large and rapidly increases. The DC circuit breaker used to separate the DC faults from the power system is still being researched, but it is very expensive due to the use of multiple power semiconductors to interrupt a large fault current in a short time. However, if the quench characteristic of a superconductor is used, the amplitude of fault current can be reduced. Therefore, it is possible to effectively interrupt a large fault current even if a relatively cheap mechanically passive DC circuit breaker is used. In the current study, a superconducting hybrid DC circuit breaker is proposed, and the limiting characteristics of each element are analyzed. By using two superconducting elements, the quench occurs sequentially twice according to the magnitude of the fault current, and the current-limiting reactor and resistance are used. If a current-limiting reactor is used in the DC system, the fault current rises slowly at the beginning of the fault, and the use of resistance can reduce the magnitude of the fault current. The inductance of the current-limiting reactor and resistance parameter settings of the hybrid DC circuit breaker was analyzed by the step-changing case method, and the interrupting characteristic of the DC circuit breaker was improved.

Keywords: superconducting hybrid DC circuit breaker; quench characteristic; step-changing case method; parameter settings

1. Introduction

The MTDC (multiterminal DC) system, called the electrical power system of the future, is expected to improve power quality and system stability. Since end power devices such as PVs (photovoltaics) and batteries use DC, it is also more advantageous in terms of power losses. However, the problem of fault interruption is more complex than for the AC power system because the DC fault current is larger, and there is no natural zero crossing. Therefore, the research of developing DCCBs (direct current circuit breakers) that enable the circuit breaker to operate in a short time is conducted. A solid DCCB, using a high-cost power switch to interrupt fault current in a short time, is too expensive to apply in practice. To solve this problem, a hybrid DCCB, using a mechanical switch and a small number of power electronic switches, has been proposed. Nevertheless, since several power electronic switches are required to reduce the interrupting time, the power burden by the power electronic switch must be reduced.

The superconducting element performs a quench operation in which resistance occurs above the critical current, and the superconducting current limiter using this characteristic is effective in limiting the fault current. The SFCL (superconducting current limiter) generally helps to reduce the interrupting capacity of a circuit breaker, but it also protects power devices and prevents their lifespan from being shortened. However, the superconducting element takes a long time to recover after removing the fault compared to quenching. This is a disadvantage in the protection coordination of the circuit breaker relaying system. Therefore, reducing this recovery time is also an important task to be solved.
To be used as a SFCL in a power system, its heat dissipation must be good, and high normal conduction resistance is advantageous for current limiting. In general, thin-film YBCO is often used, and a coil-type HTS (high-temperature superconductor) is also used. Physical structure is also related to the recovery characteristics of the superconducting element. Recovery of the superconducting element refers to a situation in which the superconducting element returns to the superconducting state after quenching; the faster it returns to the superconducting state, the more helpful it is in stabilizing the protection coordination system. There are studies that reduced the recovery time of superconducting elements through thermal analysis using conductors with solid polymer coatings [1,2]. The heat transfer of HTS can be increased by coating the surface of the superconductor, which improves the recovery characteristics [2]. Additionally, Song et al. suggested a method to reduce the recovery time while increasing the limiting effect of SFCLs by examining the recovery characteristics of helical-resistive HTSs [3].

Since the fault current can be limited by using the quench characteristic of the superconductor, the power burden of the power electronic switch can be reduced [4–7]. In particular, in the case of MCB, it was confirmed that the energy dissipation rate was reduced to 1/3 [8]. The application of SFCLs can definitely improve the performance of DCCB, but there is a site problem. In general, the cryostat system, in order to maintain the superconductivity of the high-voltage SFCL, requires a large site. Therefore, research has shown that a current-limiting-type circuit breaker system that is capable of current interrupting and limiting at the same time is more efficient than a system in which SFCL and DCCB are separated [9,10]. However, in the case of the existing model, it is difficult to expect a large effect on the current limit through the superconducting element. Structurally, the superconducting element and the coil are connected in parallel, so the fault current flowing through the MCB cannot be greatly reduced. In addition, since it is a structure that cannot protect the superconducting element, it cannot avoid damage from a large fault current. Therefore, in this paper, a superconducting hybrid DCCB, having two stages according to the magnitude of fault current, is devised by applying two superconducting elements. Normally, the current flows through the superconducting element without loss, and when a small fault current occurs, HTSC1 (the first high-temperature superconductor) is quenched to limit the fault current, and when a large fault current occurs, both HTSCs are quenched to limit the fault current. The energy burden of the DCCB can be divided and shared by two superconducting elements, reducing the energy burden rate of each superconducting element.

The proposed DCCB uses the superconducting characteristics of HTSC1 to quickly limit the current in case of fault and reduce the power burden of the MS (mechanical switch). At this time, HTSC1 distributes power to dissipate energy, and the auxiliary circuit is configured in parallel with the main circuit to reduce the power capacity of HTSC1. In the auxiliary circuit, two CLRs (current limiting reactor/resistor), a second superconducting element, and a power switch are connected. They reduce the current flowing to the MS to make interrupting faster or to reduce the peak current of the MS. However, since the disadvantage of increasing the breaking capacity of the power switch exists at the same time, an overall analysis according to the parameter characteristics of the CLR is required [9–11].

To verify the current interrupting and limiting characteristics of the superconducting hybrid DCCB, a simulation tool, PSCAD/EMTDC (power system computer-aided design/electromagnetic transient program, including direct current analysis, Version 4.5, Power by Manitoba Hydro Internation Ltd., Winnipeg, MB, Canada) was used. In Section 2, the structure of the proposed model and the modeling of each element constituting it are designed, and, in Section 3, the overall characteristics and the factors affecting the parameter sweep are investigated through a case study. In Section 4, a parameter sweep is also carried out by making the step unit smaller, and, through it, a characteristic table of the model proposed in this paper is prepared, and its meaning is discussed.
2. Modeling of Superconducting Hybrid DCCB

The proposed DCCB operates sequentially through the resistance of an HTSC (high-temperature superconductor), an MS (mechanical switch) that generates an arc, and a varistor. The resistance of the HTSC is made to generate resistance when a current above the critical current flows; when the current flowing through the MS flows above the threshold current, the MS interrupts the fault current by generating arc resistance. In the normal state, the resistance of the HTSC is large, near infinity, but when the surge voltage generated after complete interruption is higher than the breakdown voltage, the resistance decreases, and the surge energy is dissipated.

In this section, we introduce how each element is modeled, how they are constructed, and how DCCB operates as a whole.

2.1. Equivalent Circuit and Operational Process

The modeling of the elements of the superconducting hybrid DCCB is reviewed in Section 2.2. In this section, the overall configuration, equivalent circuit, and operation process of the proposed superconducting hybrid DCCB is reviewed. Figure 1 below shows the equivalent circuit of the proposed superconducting hybrid DCCB.

First, there is the main circuit, with an MS acting as the main circuit breaker, and an auxiliary circuit connected in parallel to it [9–11]. The main circuit has an LC resonance circuit connected in parallel with the MS, and when an arc occurs in the MS, a circulating current flows through the LC circuit and resonates. As a result, the arc current is zero; the moment the current becomes zero, the arc is removed, and the MS is completely interrupted. At this time, the smaller the current flowing through the MS, the shorter the time it takes for complete interruption. Therefore, the interruption time can be reduced by connecting $R_{SC1}$ (resistance of HTSC1) in series with the MS. However, in a situation where the fault current is large, the current flowing through HTSC1 increases, so the power burden in HTSC1 increases, which may lead to damage. To prevent this, the auxiliary circuit is connected in parallel with the main circuit.

![Figure 1. Equivalent circuit of proposed superconducting hybrid DCCB.](image)

The auxiliary circuit consists of $R_{SC2}$ (resistance of HTSC2), CLR1 connected in series, and CLR2 connected in parallel. When RSC1 is quenched, fault current flows toward $R_{SC2}$, and the current may or may not flow toward CLR2, depending on the critical current value setting of $R_{SC2}$. In this paper, the critical current setting of RSC2 is set to 140% of RSC1, and, as a result, the commutated current first flows toward RSC2, and then, when the fault current becomes larger, RSC2 is quenched, and the current flows toward CLR2. The reason
for connecting CLR1 in this way is to increase the limiting effect of the fault current, and the reason for connecting CLR2 is to reduce the power burden by RSC2.

2.2. Resistance Modeling of HTSC, Arc, and Varistor

2.2.1. Resistance Modeling of HTSC

The resistance of HTSC should be modeled to have superconducting properties. Therefore, when the current flowing through the superconductor is less than the critical current, the resistance of HTSC is 0; when it exceeds that, resistance is rapidly generated. When resistance is generated by a fault current, the resistance increases more rapidly while dissipating heat by generated resistance. The resistance of the HTSC increases gradually, and the rate of increase becomes slow as it approaches conducting state resistance. The series of actions in which a superconductor generates resistance is called quench, and it has different patterns depending on the physical structure of the superconductor or the properties of the material. In this paper, a thin-film type YBCO (yttrium barium copper oxide) superconductor is considered. The critical temperature of YBCO is 90 K (−183 °C), which is higher than 77 K, which is the boiling point of liquid nitrogen, so it is the most widely used superconducting element because maintenance cost is more economical than using liquid helium. Therefore, the resistance of YBCO is modeled, and the formula is expressed as follows [11–14]:

\[ R_{SC_{\text{quench}}}(t) = R_n \left[ 1 - \exp \left(\frac{-(t-t_0)}{\tau}\right) \right]^{\frac{1}{2}} \quad (t_0 \leq t < t_1) \]  

\[ R_{SC_{\text{recovery}}}(t) = R_n \left[ 1 - a \cdot \left[ 1 - \exp \left(\frac{-(t-t_2)}{\tau}\right) \right]^{\frac{1}{2}} \right] \quad (t_1 \leq t < t_2) \]

RSC stands for HTSC resistance. Equation (1) is a curve representing a resistance that is quenched at \( t_0 \) and increases to conducting state resistance \( R_n \). \( t_1 \) refers to the time at which the quench condition is released due to reasons such as fault elimination. After that, it is set to follow the recovery curve, as in Equation (2). \( \tau \) means the time constant; the closer it is to 0, the faster it gets closer to conducting state resistance. \( a \) means the reference slope of the recovery curve.

2.2.2. Resistance Modeling of Arc

If the MS is opened while the current is flowing, arc discharge occurs between the two electrodes. This discharge is a self-sustained discharge. When a large current flows through the cathode, resistance heat is generated accordingly, and a large number of electrons are released by heat absorption. Therefore, a large current continuously flows, and a process in which a large number of electrons are released is repeated, and the discharge sustains without external ionization. The conductance of arc can generally be expressed as a function of the heat quantity between the electrodes [14–19]. The heat quantity \( Q \) between the two electrodes is expressed as Equation (3) below.

\[ Q(t) = \int_0^t (P_{in}(t) - P_o) \, dt \]  

\( P_{in}(t) \) means the difference between the incoming power of the two electrodes, and \( P_o \) means the power emitted as thermal energy of the arc channel (=column). \( P_o \) also means the amount of heat that MS can withstand. Using Equation (3), the arc conductance
expressed as Equation (4) can be obtained, and then, it can be expressed as Equation (5) through the mathematical process.

\[ g(t) = f(Q(t)) = f \left[ \int_0^t (P_{in}(t) - P_{out}) \, dt \right] \]  

\[ \frac{d(ln(g(t))}{dt} = f\left(\frac{Q(t)}{f(Q(t))}\right)(P_{in}(t) - P_{out}) \]  

Equation (5) is called the general arc equation, and by applying Mayr’s assumption to it, the arc equation can be obtained as Equation (6).

Mayr’s assumption: \( f(Q(t)) = ke^{Q(t)} / e^{Q_0} \)

\[ \frac{d(ln(g(t)))}{dt} = \left( u_{arc}(t) i_{arc}(t) - P_0 \right) / Q_0 \]  

where \( k \) denotes the Boltzmann constant. \( Q_0 \) is expressed as \( Q_0 = \tau_o \cdot P_o \) through the arc generation time constant \( \tau_o \). Based on this equation, the arc resistance can be modeled by applying the black-box model.

2.2.3. Resistance Modeling of Varistor

Varistor is a compound word of variable and resistor and is one of the transient current suppression devices developed to protect the circuit from sudden fluctuations in voltage or current. In this paper, a ZnO varistor composed of zinc oxide was used. The microstructure of the ZnO varistor, a polycrystalline ceramic element, consists of a ZnO grain and an intergranular boundary surrounding it. It is known that ZnO grains supply electric charge, and the intergranular boundary causes breakdown characteristics. Therefore, varistor resistance usually has a resistance of 1 to 10 kΩ, and, during operation, resistance occurs according to the curve, as shown in Equation (7) below. \( \alpha \) means the resistance ratio linear index; the higher the value, the closer the ideal varistor. Usually, it has a value of 6 to 8, and, in this paper, it is assumed to be 8. \( V_b \) stands for breakdown voltage [19–23].

\[ i = \left( \frac{v}{V_b} \right)^\alpha \]  

The equivalent circuit of the varistor is composed of a series resistance and a capacitor, as shown in Figure 2 below. The series resistance is the ZnO grain resistance \( R_{ZnO} \) and is constant, but \( R_{gb} \) is the resistance of the intergranular boundary, which follows Equation (7) above. \( L \) is an inductance of conducting leads, and \( C \) denotes the capacitance of the intergranular boundary.

**Figure 2.** Equivalent circuit of the varistor.

2.3. Equivalent Circuit and Operational Process

The limiting and interrupting characteristics are completely different depending on whether CLR1 and CLR2 are set to resistance or inductance. For example, if CLR1 is set to
resistance and CLR2 is set to inductance, $R_{SC1}$ is quenched, causing rapid commutation toward the auxiliary circuit. On the other hand, if CLR1 is set to inductance and CLR2 is set to resistance, the change of commutating current in the auxiliary circuit will be smooth. Figures 3 and 4 below are graphs showing current-limiting and -interrupting characteristics according to the impedance setting of CLR1 and CLR2.

**Figure 3.** The waveform of DCCB current ($i_{DCCB}$), Arc current ($i_{arc}$), LC circuit current ($i_{LC}$), HTSC1 current ($i_{SC1}$), HTSC2 current ($i_{SC2}$), CLR1 current ($i_{CLR1}$), CLR2 current ($i_{CLR2}$) and varistor current ($i_{varistor}$), 10 times resistance of HTSC1 ($R_{SC1}$), and resistance of HTSC2 ($R_{SC2}$); impedance setting CLR1: Inductance 2 (mH), CLR2: Resistance 1.0 (Ω).

**Figure 4.** The waveform of DCCB current ($i_{DCCB}$), Arc current ($i_{arc}$), LC circuit current ($i_{LC}$), HTSC1 current ($i_{SC1}$), HTSC2 current ($i_{SC2}$), CLR1 current ($i_{CLR1}$), CLR2 current ($i_{CLR2}$) and varistor current ($i_{varistor}$), 10 times resistance of HTSC1 ($R_{SC1}$), and resistance of HTSC2 ($R_{SC2}$); impedance setting CLR1: Resistance 1.0 (Ω), CLR2: Inductance 2 (mH).

Figure 3 shows CLR1 with an inductance of 2 mH and CLR2 with a resistance of 1.0 Ω, and Figure 4 shows CLR1 with a resistance of 1.0 Ω and CLR2 with an inductance of 2 mH. There is no significant difference between Figures 3 and 4 in the time that HTSC1 is quenched. However, after HTSC1’s quenching, the current flowing toward the
auxiliary circuit rises faster in Figure 4, where only the resistance is connected, and HTSC2’s quenching is also fast. After HTSC2 is quenched, the current begins to flow toward CLR2. In the case of Figure 4, since inductance is connected in parallel with HTSC2, there is a slight current-limiting effect. In Figure 3, it can be seen that since the current-limiting effect is large after quenching, the current reaches the zero point immediately, resulting in a complete interruption (arc discrimination).

In terms of the overall operation, the peak value of $i_{arc}$ is smaller in Figure 3 than in Figure 4, so it has the advantage of lowering the MS performance; however, there is also a disadvantage in that the interrupting time is longer than that in Figure 4.

3. Simulation and Results

In Section 2, the element modeling and operation process of the proposed superconducting hybrid DCCB and how the CLR impedance setting affects the overall operation process are reviewed. In this section, we review the simulation setting conditions and the case-by-case results.

Figure 5 is a simulated DC system for verification of the proposed superconducting hybrid DCCB. It is converted to DC using a three-phase rectifier from the AC grid and smoothed using a capacitor to make it closer to DC. In the DC terminal, it is connected to the load $Z_{Load}$ through the DC line impedance $Z_{line}$ and the fault resistance $R_{fault}$, and the closing switch is connected in parallel with the load to simulate a fault. Detailed parameters of the DC system are listed in Table 1. And the modeling parameters of the proposed superconducting hybrid DCCB are specified in Table 2.

![Simulated DC system for the review of the proposed superconducting hybrid DCCB.](image)

The cases were largely divided into the case where CLR1 is the inductance and CLR2 is the resistance (CASE1), and the case where CLR1 is the resistance and CLR2 is the inductance (CASE2). When the inductance is 2 and 3 mH, the resistance is set to 0, 0.5, 1, 2, 4, 8, 16 Ω. Figure 6 shows a case where CLR1 is the inductance and CLR2 is the resistance. Inductance is 2 mH, and the resistance is changed. Figure 7 shows the results when the inductance value is set to 3 mH.

| Index     | Description          | Value | Unit |
|-----------|----------------------|-------|------|
| $V_{DC}$  | DC Terminal Voltage  | 15    | kV   |
| $Z_{line}$| Line Impedance       | 0.01  | Ω    |
| $Z_{Load}$| Load Impedance       | 10    | Ω    |
| $R_{fault}$| DC Fault Resistance  | 0.6   | Ω    |

Table 1. Parameters of the DC system for simulation.
Table 2. Parameters of the proposed superconducting hybrid DCCB.

| Item                  | Classification | Value | Unit   |
|-----------------------|----------------|-------|--------|
| Main Circuit          | Cooling Power ($P_0$) | 15    | MW     |
|                       | Arc Generation Time Constant ($\tau_0$) | 1     | $\mu$s |
|                       | Conductive Resistance of HTSC1 | 1     | $\Omega$ |
|                       | Time Constant of HTSC1 | 0.1   | ms     |
|                       | Critical Current of HTSC1 | 5     | kA     |
|                       | Recovery Constant of HTSC1 ($a$) | $-10$ | $\Omega$/ms |
|                       | Inductance of Resonance Circuit ($L$) | 87    | mH     |
|                       | Capacitance of Resonance Circuit ($C$) | 3.33  | $\mu$F |
| Auxiliary Circuit     | Conductive Resistance of HTSC2 | 20    | $\Omega$ |
|                       | Time Constant of HTSC2 | 0.1   | ms     |
|                       | Critical Current of HTSC2 | 7     | kA     |
|                       | Recovery Constant of HTSC2 ($a$) | $-10$ | $\Omega$/ms |
| Varistor              | Breakdown Voltage ($V_B$) | 20    | kV     |
|                       | Nonlinear Index ($\gamma$) | 8     | -      |
|                       | Shunt Capacitor ($C$) | 0.6   | $\mu$F |

Figure 6. The waveform of DCCB current ($i_{DCCB}$) and arc current ($i_{arc}$) in the case where CLR1 is set to Inductance 2 (mH) and CLR2 is set to Resistance 0, 0.5, 1, 2, 4, 8, 16 ($\Omega$).

Figure 7. The waveform of DCCB current ($i_{DCCB}$) and arc current ($i_{arc}$) in the case where CLR1 is set to Inductance 3 (mH) and CLR2 is set to Resistance 0, 0.5, 1, 2, 4, 8, 16 ($\Omega$).
As can be seen from Figure 6, at 2 mH, the smaller the resistance, the faster the breaking speed, and the lower the peak value of the arc current $i_{\text{arc}}$. Figure 7 shows that as the resistance decreases to 3 mH, the peak of the arc current greatly decreases, but the interrupting time does not change significantly. In both Figures 6 and 7, it can be seen that the arc current fluctuates greatly, but the peak value of the CB current, which is the total current, is not significantly different. This means that in the case of CASE1, the total impedance of the proposed superconducting hybrid DCCB is not significantly affected by the CLR impedance, but the interrupting characteristic can be improved. In Figures 8 and 9, unlike Figures 6 and 7, CLR1 is the resistance and CLR2 is the inductance. Inductance and resistance settings are shown in Figures 6 and 7 above.

**Figure 8.** The waveform of DCCB current ($i_{\text{DCCB}}$) and arc current ($i_{\text{arc}}$) in the case where CLR1 resistance is 0, 0.5, 1, 2, 4, 8, 16 (Ω) and CLR2 is set to Inductance 2 (mH).

**Figure 9.** The waveform of DCCB current ($i_{\text{DCCB}}$) and arc current ($i_{\text{arc}}$) in the case where CLR1 resistance is 0, 0.5, 1, 2, 4, 8, 16 (Ω) and CLR2 is set to Inductance 3 (mH).

As mentioned in Section 2, when CLR1 is the resistance and CLR2 is the inductance, the impedance of the auxiliary circuit is greatly affected by CLR1. In addition, since HTSC2’s quenching does not occur when the resistance is greater than 1Ω, there is no significant difference in Figures 8 and 9. It can be seen that the interrupting time is delayed in Figure 9 only when RCLR1 is 0, 0.5 Ω. This is because when HTSC2 is quenched, the current change
toward the auxiliary circuit decreases as the inductance increases, so the current flowing
toward the MS becomes larger than when the inductance is small. Therefore, the time for
zero crossing through LC resonance is longer. As a result, the smaller the resistance of the
CLR circuit, the shorter the interrupting time and the smaller the peak value of $i_{arc}$.

Based on these results, in the case of Figures 6–9, it can be confirmed that the interrupt-
ing time is shortest when CLR resistance is 0. In particular, when the CLR resistance
in Figure 8 is 0, it can be seen that the interrupting time is the shortest among all cases.
However, if CLR1 resistance becomes 0, the discharging current of L will flow largely after
SW is opened, so setting it to 0 may cause damage to the device. In addition, overcurrent
flows through HTSC2, causing damage to HTSC2. Therefore, an appropriate parameter
setting is needed.

4. Discussion

The importance of setting parameters has been mentioned earlier. In this section, we
check the appropriate parameter setting through a case study.

The circuit using inductance for CLR1 and resistance for CLR2 shows relatively good
results. Although the interrupting time is slow, the peak of arc current decreases to a large
value. In this case, the smaller the resistance and inductance, the shorter the interrupting
time (arc dissipation time). However, the peak of the arc current does not show a constant
aspect. The aspect is that the smaller the resistance, the smaller the peak of the arc current,
but there are many exceptions. Tables 3 and 4 below describe the interrupting time and
peak of arc current results according to the case study.

As can be seen from the tables, as the resistance and inductor decrease, the peak of the
arc current also decreases. However, when the resistance of CLR2 decreases, the current
flowing to the power SW of the auxiliary circuit, CLR1, increases. This causes an increase
in the capacity of the power SW, which leads to economic losses. The cut-off current of
power SW is more related to CLR2 than CLR1. This is because HTSC2 is squeezed out of
the auxiliary circuit, and the resistance of the auxiliary circuit is greatly affected by CLR2.
Therefore, the larger the resistance, the lower the unit cost of the power SW. The unit price
of the power SW occupies a large portion of the proposed superconducting hybrid DCCB,
so the overall unit price is also expensive.

| Case | CLR1 Inductance (mH) | CLR2 Resistance (Ω) |
|------|----------------------|---------------------|
| 0.05 | 1.645 1.930 2.135 2.340 2.448 2.658 2.771 |
| 0.10 | 1.732 1.932 2.137 2.343 2.454 2.661 2.866 |
| 0.15 | 1.734 1.935 2.140 2.346 2.553 2.665 2.868 |
| 0.20 | 1.736 1.934 2.144 2.350 2.556 2.761 2.872 |
| 0.25 | 1.739 1.942 2.150 2.355 2.559 2.764 2.876 |
| 0.30 | 1.742 1.952 2.244 2.451 2.565 2.768 2.973 |
| 0.35 | 1.746 2.040 2.247 2.454 2.660 2.772 2.976 |
| 0.40 | 1.841 2.044 2.251 2.458 2.664 2.869 2.979 |
| 0.45 | 1.844 2.048 2.258 2.465 2.668 2.873 2.984 |
| 0.50 | 1.847 2.056 2.350 2.560 2.767 2.877 3.082 |
| 0.55 | 1.852 2.150 2.357 2.565 2.771 2.885 3.085 |
| 0.60 | 1.949 2.154 2.364 2.574 2.775 2.980 3.090 |
| 0.65 | 1.954 2.163 2.462 2.669 2.875 2.984 3.189 |
| 0.70 | 1.959 2.259 2.467 2.675 2.879 3.084 3.193 |
| 0.75 | 2.059 2.265 2.568 2.775 2.986 3.089 3.197 |
| 0.80 | 2.065 2.366 2.574 2.781 2.985 3.094 3.297 |
| 0.85 | 2.167 2.373 2.676 2.882 3.091 3.194 3.301 |
| 0.90 | 2.174 2.474 2.682 2.888 3.092 3.199 3.309 |
| 0.95 | 2.277 2.578 2.785 2.990 3.098 3.301 3.407 |
| 1.00 | 2.381 2.586 2.799 2.998 3.199 3.306 3.412 |
Overall, the largest portion of cost of the proposed superconducting hybrid DCCB is the power electronic switch. Since the price of the SW increases exponentially as the capacity of the SW increases, it is important to lower the current capacity. The current flowing through the SW varies according to the impedance type and size of CLR1 and CLR2. If CLR1 is set to resistance and CLR2 is set to inductance, the current flowing through the SW is greatly reduced, but on the contrary, the interrupting time is lengthened because the current flowing through the mechanical switch is large. Therefore, when inductance in CLR1 and resistance in CLR2 are set, the current flows more toward the SW, so the overall proposed system cost is higher, but the interrupting time is shorter. Additionally, depending on the size of resistance and inductance, the interrupting time can be further shortened, and the fault current flowing through the SW can be further increased. In conclusion, due to the application of the superconducting element, the magnitude of the fault current can be effectively reduced. Compared with a conventional hybrid DCCB, it is confirmed that the number and capacity of power electronic SWs can be significantly reduced, and the larger the applied system size, the more advantageous in terms of cost.

5. Conclusions

The proposed superconducting hybrid DCCB is advantageous in terms of price and site compared to other DCCBs, but the review on parameter settings was insufficient to increase its performance. Therefore, in the current study, the operation of the proposed superconducting hybrid DCCB, according to parameter settings, was simulated, and the results were reviewed.

Modeling for each element of the proposed DCCB was proposed, and its behavior was examined. The overall operating characteristics were different depending on the impedance setting of CLR1 and CLR2. When CLR1 is set to inductance and CLR2 to resistance (CASE1), the current limiting effect is excellent, but since the quenching of RSC2 is delayed, the interrupting time is relatively delayed. On the contrary, when CLR1 is set to resistance and CLR2 to inductance (CASE2), the interrupting time is faster, but the peak of the arc current is increased, and, after interrupting, a large overcurrent is caused by the discharge current of CLR2 inductance. Therefore, HTSC2 could be damaged.
The interrupting time and arc current were reviewed when the parameters were changed for the two cases above the simulation. Through this, the effect of changing the resistance and inductance on the results was examined. As a result, CASE1 of inductance was greatly influenced by inductance, with relatively little influence by resistance. In CASE2, above a specific inductance value, the result was constant regardless of the resistance change. CASE1 and CASE2 had similar minimum interrupting times, but CASE2 had a significantly larger arc current peak value.

The following contents were verified through this simulation.

- Changing the parameters of CASE1 greatly affects the result value.
- The smaller the CLR1 inductance and CLR2 resistance, the shorter the interrupting time and the smaller the peak of the arc current tends to be.
- There are many exceptions where the peak of the arc current decreases when CLR2 resistance increases.
- As CLR2 resistance increases, the capacity of the power SW in the auxiliary circuit should increase.

Through the parameter case study, we reviewed the interrupting characteristic and found a parameter setting that could be improved. However, it was confirmed that the price could be disadvantageous when considering the capacity of the power SW. In a system where system stability is prioritized, the optimal parameter setting can be used, but if not, an optional parameter setting will be required. This study contributes to the protection and stability improvement of power systems using DC, such as future DC-powered systems or railway systems.

Author Contributions: Writing—original draft, S.-J.C.; Writing—review and editing, S.-H.L. All authors have read and agreed to the published version of the manuscript

Funding: This research was supported by Korea Electric Power Corporation (Grant number: R19XO01-19) and was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MOE) (No. 2020R1F1A1077206).

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

References
1. Yazdani-Asrami, M.; Staines, M.; Sidorov, G.; Eicher, A. Heat transfer and recovery performance enhancement of metal and superconducting tapes under high current pulses for improving fault current-limiting behavior of HTS transformers. *Supercond. Sci. Technol.* 2020, 33, 095014. [CrossRef]
2. Yazdani-Asrami, M.; Staines, M.; Sidorov, G.; Davies, M.; Bailey, J.; Allpress, N.; Glasson, N.; Gholamian, S.A. Fault current limiting HTS transformer with extended fault withstand time. *Supercond. Sci. Technol.* 2019, 32, 035006. [CrossRef]
3. Song, W.; Pei, X.; Alafran, H.; Xi, J.; Zeng, X.; Yazdani-Asrami, M.; Xiang, B.; Liu, Z. Experimental and Simulation Study for Resistive Helical HTS Fault Current Limiter: Quench and Recovery Characteristics. *IEEE Trans. Appl. Supercond.* 2021. [CrossRef]
4. Pei, X.; Cwikowski, O.; Smith, A.C.; Barnes, M. Design and Experimental Tests of a Superconducting Hybrid DC Circuit Breaker. *IEEE Trans. Appl. Supercond.* 2018, 28, 1–5. [CrossRef]
5. Xiang, B.; Liu, Z.; Geng, Y.; Yanabu, S. DC Circuit Breaker Using Superconductor for Current Limiting. *IEEE Trans. Appl. Supercond.* 2015, 25, 1–7. [CrossRef]
6. Hwang, S.; Choi, H.; Jeong, I.; Choi, H. Characteristics of DC Circuit Breaker Applying Transformer-Type Superconducting Fault Current Limiter. *IEEE Trans. Appl. Supercond.* 2018, 28, 1–5. [CrossRef]
7. Novello, L.; Gaio, E.; Piovan, R. Feasibility Study of a Hybrid Mechanical-Static DC Circuit Breaker for Superconducting Magnet Protection. *IEEE Trans. Appl. Supercond.* 2009, 19, 76–83. [CrossRef]
8. Xiang, B.; Zhang, L.; Yang, K.; Tan, Y.; Liu, Z.; Geng, Y.; Wang, J.; Yanabu, S. Arcing Time of a DC Circuit Breaker Based on a Superconducting Current-Limiting Technology. *IEEE Trans. Appl. Supercond.* 2016, 26, 1–5. [CrossRef]
9. Sakai, M.; Kato, Y.; Tokuyama, S.; Sugawara, H.; Arimatsu, K. Development and field application of metallic return protecting breaker for HVDC transmission. *IEEE Trans. Power Appar. Syst.* 1981, 4860–4868. [CrossRef]
10. Baran, M.E.; Mahajan, N.R. Overcurrent Protection on Voltage-Source-Converter-Based Multiterminal DC Distribution Systems. *IEEE Trans. Power Deliv.* 2007, 22, 406–412. [CrossRef]
11. Bucher, M.K.; Franck, C.M. Fault Current Interruption in Multiterminal HVDC Networks. *IEEE Trans. Power Deliv.* 2016, 31, 87–95. [CrossRef]
12. Mangtha, S.Y. Superconducting Fault Current Limiter for Energy Storage Protection under Grounded Faults in a Microgrid. *Int. J. Adv. Technol. Innov. Res.* 2017, 1506–1511.

13. Lim, S.; Lim, S. Analysis on Operational Improvement of OCR Using Voltage Component in a Power Distribution System for Application of SFCL. *J. Electr. Eng. Technol.* 2019, 14, 1027–1033. [CrossRef]

14. Langston, J.; Steurer, M.; Woodruff, S.; Baldwin, T.; Tang, J. A Generic Real-Time Computer Simulation Model for Superconducting Fault Current Limiters and Its Application in System Protection Studies. *IEEE Trans. Appl. Supercond.* 2005, 15, 2090–2093. [CrossRef]

15. van der Sluis, L. *Transients in Power Systems*; John Wiley & Sons: Hoboken, NJ, USA, 2001.

16. Andrea, J.; Bournat, M.; Landfried, R.; Testé, P.; Schweitzer, S.W.P. Model of an Electric Arc for Circuit Analysis. In Proceedings of the 28th International Conference on Electric Contacts ICEC, Edinburgh, UK, 6–9 June 2016; pp. 361–366.

17. Rao, B.K.; Gajjar, G. Modelling of SF6 Circuit Breaker Arc Quenching Phenomena In PSCAD. *SWICON 2008*, 163–168.

18. Schavemaker, P.H.; van der Sluis, L. The Arc model Blockset. In Proceedings of the Second IASTED International Conference, Crete, Greece, 25 June 2002; pp. 644–648.

19. Bijl, N.D.H.; van der Sluis, L. New Approach to the Calculation of Electrical Transients, Part I: Theory. *Eur. Trans. Electr. Power Eng.* 1998, 8, 175–179. [CrossRef]

20. Matsuoka, M. Nonohmic Properties of Zinc Oxide Ceramics. *Japan Soc. Appl. Phys.* 1971, 10, 736–746. [CrossRef]

21. Eda, K. Destruction mechanism of ZnO varistors due to high currents. *J. Appl. Phys.* 1984, 56, 2948. [CrossRef]

22. Nakao, H.; Nakagoshi, Y.; Hatano, M.; Koshizuka, T.; Nishiwaki, S.; Kobayashi, A.; Murao, T.; Yanabu, S.D.C. Current Interruption in HVDC SF6 Gas MRTB by Means of Self-Excited Oscillation Superimposition. *IEEE Trans. Power Deliv.* 2001, 16, 687–693. [CrossRef]

23. Yang, J.; Fletcher, J.E.; O’Reilly, J. Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables. *IEEE Trans. Ind. Electron.* 2012, 59, 3827–3837. [CrossRef]