Design of Low Power Low Noise Amplifier using Gm-boosted Technique

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ABSTRACT

This paper presents the development of low noise amplifier integrated circuit using 130nm RFCMOS technology. The low noise amplifier function is to amplify extremely low noise amplifier without adding noise and preserving required signal to a noise ratio. A detailed methodology and analysis that leads to a low power LNA are being discussed throughout this paper. Inductively degenerated and Gm-boosted topology are used to design the circuit. Design specifications are focused for 802.11b/g/n IEEE Wireless LAN Standards with center frequency of 2.4 GHz. The best low noise amplifier provides a power gain (S21) of 19.841 dB with noise figure (NF) of 1.497 dB using the gm-boosted topology while the best low power amplifier drawing 4.19mW power from a 1.2V voltage supply using the inductively degenerated.

Keywords: CMOS, Integrated circuits, LNA, Noise figure

1. INTRODUCTION

The fast growth of wireless communication system has made radio frequency integrated circuit, CMOS-based technology, an attractive package for radio transceiver front-end circuits in numerous wireless communication systems. In the communication system, Low noise amplifier is the first block of receiver [1]. This amplifier is one of an electronic amplifier that used to amplify very weak signals. Mobile handphones and wireless local area network (WLAN) communication are becoming a part of our daily lives. Design of LNA involves many trade-offs between between its requirements. Thiese involve getting simultaneous high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. The LNA design in this paper used inductively degenerated topology with Gm-boosted technique to minimize the noise figure and reduce the power consumption at the same time.

2. RESEARCH METHOD

Figure 1 presents the typical inductively degenerated CMOS LNA topology. The inductively degenerated CMOS LNA are chosen because it is widely used and its low noise performance [2-3]. It is nowadays used both in single and multi-standard transceivers because of the better NF and the lower power consumption with respect to other topologies for narrow band applications [3-5]. Inductively degenerated cascode LNA consists of an input signal source RFin. The source resistance Rs of 50Ω, an inductance gate, Lg, source inductor, Ls, load inductor Ld, additional capacitor Cext. Lg and Ls are used to match input impedance while Ld is used to match output impedance. The LNA designed in this paper uses a Gm-boosted technique structure with inter-stage inductors as shown in Figure 2. In this circuit M1, M2 are the cascade
transistors, M3 is used to build the bias for the LNA, Lg and Ls are used for the input matching. While Ld, Lg and Cext are the inter-stage components.

In this LNA design, the suitable value of inductor, $L_s$ is chosen. Then the value of $g_m$ and $C_{gs}$ are calculated to give required $Z_{in}[6]$.

$$Z_{in} = \frac{V_g}{I_g} = \frac{I_g R_g + V_c + j\omega L_s L_s}{I_g}$$  \hspace{1cm} (1)

$$Z_{in} = \frac{L_s g_m}{C_{gs}} \text{ where } Z_{in} \text{ may be } 50\Omega$$  \hspace{1cm} (2)

Degeneration Inductor $L_s$ can be found by using equation 2. Then the optimal Q factor of inductor $L_s$ can be calculated by using equation 3.

$$\omega_f = \frac{g_m}{C_{gs}} = \frac{R_s}{L_s}$$ \hspace{1cm} (3)

Optimal Q of Inductor,

$$Q_L = \sqrt{\frac{1 + \frac{1}{\beta}}{\beta}}$$ \hspace{1cm} (4)

Where $\beta = \frac{\delta \alpha^2}{5. \gamma}$

The value of inductor $L_g$ can be found by using equation 5.

$$L_g = \frac{Q_L R_s}{\omega_0} - L_s$$ \hspace{1cm} (5)

After obtaining the gate-source Capacitance and then the width, W of the transistor can be found by using the equation below:

$$C_{gs} = \frac{1}{\omega_0^2 (L_{gs} + L_s)}$$ \hspace{1cm} (6)
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Where, $\varepsilon_{ox} = \varepsilon_{ox} \cdot \varepsilon_0$ and $C_{ox} = \frac{\varepsilon_{ox}}{\varepsilon_0}$

Then, the optimum Noise Figure can be estimated as below:

$$NF_{opt} = 1 + \frac{2\gamma}{\alpha} \left( \frac{\omega_r}{\omega_p} \right) \sqrt{P} \left( |c| + \sqrt{p} + \sqrt{1+p} \right)$$

Gain-boosting is a well-established technique that uses an amplifier in place of A(s) to increase the dc gain of a cascade stage [7-10]. A gm-boosted MOS cascade with enhanced bandwidth as shown in Figure 2 can increase the transconductance of M2 by a factor of [1 + A(s)], $g_m = [1 + A(s)]g_{m2}$

![Figure 2. A Gm-boosted Technique Circuit](image.png)

![Figure 3. Inductively degenerated LNA with Gm-boosted Circuit](image.png)

In order to reduce the even-order harmonics of the receiver, the LNA is needed to act as a single-to-differential conversion as well [8]. The cross connection can be used in a fully-differential circuit to provide the polarity of the feedback. The first order of high pass response can be provided by using a simple CR-section for the cross connection.

$$A(s) = \frac{RC_s}{1 + RC_s}$$

The formula for frequency dependent transconductance can be obtained by substituting equation (2) into (1).

$$g_{m1} = \frac{1 + 2RC_s}{1 + RC_s} g_{m2}$$

Thus, $g_{m1} \approx g_{m2}$ when $f \ll \frac{1}{2\pi RC}$ or at low frequency. While at high frequency $f \gg \frac{1}{2\pi RC}$, $g_{m1} \approx 2g_{m2}$. The schematic as shown in Figure 3 is the combination technique between inductively degenerated and gm-boosted. Both techniques are used in one circuit to optimize the result of the gain bandwidth and noise factor.

3. RESULTS AND ANALYSIS

Table 2 compares the Scattering parameter graphs obtained from the simulation of LNA circuit design utilizing inductively degenerated topology and Gm-boosted techniques. What stands out in the table is that, by using Gm-boosted technique to the inductively degenerated topology the gain obtained higher which is 19.841dB.
Table 2.1 Graph Comparison of LNA performance using Gm-boosted technique

| Parameter                           | Inductively degenerated topology only | With Gm-boosted |
|-------------------------------------|--------------------------------------|-----------------|
| S_{11} and S_{22}                   | ![Graph1]                            | ![Graph2]       |
| S_{21} and S_{12}                   | ![Graph3]                            | ![Graph4]       |
| Noise Factor (NF)                   | ![Graph5]                            | ![Graph6]       |

The output matching circuit does not change the bias of the active device. It is very easy to achieve the required output matching without any filter network at the output since the LNA has very low output impedance. The graph of S_{22} illustrates the inductively degenerated LNA manage to get -26.329 dB instead of the gm-boosted value is -12.260 dB. The output reverse isolation is very important criteria to ensure better stability and lower NF. The simulated noise figures of the LNA topologies is 1.68 dB for the inductively degenerated while the gm boosted is 1.497 db. The power dissipation for inductively degenerated topology is 4.19 mW while for gm-boosted topology is 6.933 mW. Table 2 presents the comparison of LNA design with other published works.

Table 2.2 Performance comparison with other published works

| References | This work |
|------------|-----------|
|            | Process technology | Frequency (GHz) | Power supply (V) | S_{11} (dB) | S_{12} (dB) | S_{21} (dB) | S_{22} (dB) | Noise Factor (dB) | Power Dissipation (mW) |
| [9]        | 180nm     | 1.5-11.7     | 1.8         | 12.26     | -8.6      | 4.3          | -26        | 3.74-4.74        | 10.34                 |
| [10]       | 180nm     | 1.4-9.5      | 1.8         | 13        | -9.5      | 4.3          | n.a        | 4.3            | 20                    |
| [11]       | 130nm     | 1.25-11.34   | 1.2         | 11        | -11       | 2.38-3.4     | n.a        | 2.38-3.4        | 5.8                   |
| This work  | 130nm     | 2.4 GHz      | 1.2 V       | 19.16     | -18.61    | 1.67         | -37.16     | 3.67            | 4.73                  |
|            | Inductively degenerated | 2.4 GHz | 1.2 V | 19.84 | -18.61 | 1.67 | -37.16 | 3.67 | 4.73 |
|            | Gm-boosted | 2.4 GHz | 1.2 V | 19.84 | -18.61 | 1.67 | -37.16 | 3.67 | 4.73 |

Figure 4 shows the layout design of the combination between inductively degenerated and gm boosted topology. The size of this layout is 693μm x 723μm. All the component chosen to make this layout are using the RFCMOS technology.

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4. CONCLUSION

The design of low power LNA were successfully implemented using Inductively Degenerated topology and gm-boosted topology. The LNA design achieved a power gain (S21) of 19.841 dB with noise figure (NF) of 1.497 dB while also managed low power at 4.19mW.

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REFERENCES

[1] A. A Amin, M. S. Islam, M. A. Masud, M. N. H. Khan. Design and Performance Analysis of 1.8 GHz Low Noise Amplifier for Wireless Receiver Application. Indonesian Journal of Electrical Engineering and Computer Science. Vol. 6, No. 3, June 2017, pp. 656 - 662.

[2] A. N. A. Z. Badri, N. M. Noh, S. K. Kunhi, M. A. A. Manaf, A. Marzuki, M. T. Mustaffa. Layout Effects on High Frequency and Noise Parameters in MOSFETs. Indonesian Journal of Electrical Engineering and Computer Science. Vol. 6, No. 1, April 2017, pp. 88 - 96.

[3] S. Kumar, “A 1.8V and 2GHz Inductively Degenerated CMOS Low Noise Amplifier,” 2012, vol. 2, no. 4: 150 - 154.

[4] K. Pongot, A.R Othman, Z. Zakaria Z, M.K Suaidi, A.H Hamidon. New Topology LNA Architecture using Inductive Drain Feedback Technique for Wireless Application. Indonesian Journal of Electrical Engineering and Computer Science. Vol. 12, No. 12, December 2014, pp. 8257 - 8267.

[5] S. Toofan, A.R Rahmati, A. Abrishamifar, G.R Lahiji. Low power and high gain current reuse LNA with modified input matching and inter-stageinductors. Microelectronics Journal, 2008,39(2):1534-1537.

[6] S. U. Shankar and M. D. K. Dhas, “Design and Performance Measure of 5.4 GHz CMOS Low Noise Amplifier Using Current Reuse Technique in 0.18μm Technology,” Procedia Comput. Sci., vol. 47, pp. 135 - 143, 2015.

[7] T. Nguyen, C. Kim, G. Ihm, M. Yang, S. Lee, and A. C. N. M. Technique, “CMOS Low-Noise Amplifier Design Optimization Techniques,” vol. 52, no. 5, pp. 1433 – 1442, 2004.

[8] A. Dharmik, A. Y. Deshmukh, and P. S. Tembhurne, “Design Methodology for Inductively Degenerated CMOS Low Noise Amplifier for 2.47 GHz Frequency at 0.18μm Technology for T-Matching.”, pp. 37 – 42, 2014.

[9] “A Design Flow for Inductively Degenerated LNA’ S D. Guermandi, E. Franchi, A. Gnaudi ARCES - DEIS University of Bologna Viale Risorgimento 2, 40126 Bologna, ITALY, 2004,” pp. 615 – 618.

[10] P. Kavyashree and S. S. Yellampalli, “The Design of Low Noise Amplifiers in Nanometer Technology for WIMAX Applications,” 2013, vol. 3, no. 10, pp. 1 – 6.

[11] M. Hossain, A. C. Carusone, and I. S. -S. C. Society, “A 19-GHz broadband amplifier using a gm-boosted cascode in 0.18-μm CMOS,” IEEE 2006 Cust. Integr. Circuits Conf. CICC 2006, pp. 829 – 832.

[12] H. C. Lee, C. S. Wang, and C. K. Wang, “A 0.2-2.6 GHz wideband noise-reduction Gm-boosted LNA,” IEEE Microw. Wirel. Components Lett., 2012, vol. 22, no. 5, pp. 269 – 271.

[13] Y. S. Lin, C. Z. Chen, H. Y. Yang, C. C. Chen, J. H. Lee, G. W. Huang, and S. S. Lu, “Analysis and design of a CMOS UWB LNA with dual-RLC-branch wideband input matching network,” IEEE Trans. Microw. Theory Tech., 2010, vol. 58, no. 2, pp. 287 – 296.

[14] A. Jamalkhah and A. Hakimi, “An Ultra-Wideband Common Gate LNA With Gm-Boosted and Noise Canceling Techniques,” 2014, vol. 2, no. 2, pp. 113 – 118.

[15] B Guo and X Li. A 1.6 – 9.7 GHz CMOS LNA Linearized by Post Distortion Technique. IEEE Microwave and Wireless Components Letters. 2013; 23(11): 608-610.