Research of Design Technologies for 8-bit High Speed Low Power Pipelined ADC

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Abstract. 8-bit, 80MS/s low power ADC is presented in this paper by using seven stage Pipelined architecture. To reduce the chip size and power of total ADC, and improve the harmonic distortion and noise property, MDAC in first sub-ADC is considered focused, The whole ADC was designed in 0.18μm CMOS process, the SNR of the ADC is 53dB, ENOB is 7.98bits. The total chip size is only 0.56mm², as well as the typical power current is only 22mA. The Performance requirement of the ADC is achieved.

Key words: ADC Integrated Circuit, Design Technology, Chip Size, Low Power.

1. Introduction
The article introduces an 8-bit pipelined ADC based on a 0.18μm process with a sampling rate of 80MHz to solve these problems. By means of optimizing the design of MDAC and operational amplifier in the first-level sub-ADC, It can cut down on the sample-and-hold circuit module of the entire AD; In addition, a step-by-step scaling technique is adopted in the design of the circuit structure of the second to seventh sub-ADCs, and an optimized layout design technology is adopted. The chip area of the entire ADC is reduced by these innovative design techniques, reduce the power consumption of the ADC, and improve the signal to noise ratio of the ADC, making the ADC widely applied to wireless communications, instrumentation, ultrasound systems, and high-resolution image processing and high-definition television (HDTV) and other occasions.

2. The overall design idea of 8 bit high speed low power pipelined ADC
Figure 1 is a kind of structure block diagram of 8 bit high speed low power pipelined ADC, among them, the core module of the whole ADC is framed with the dotted line-- Converter module. The module is mainly composed of a sample-and-hold circuit S/H and 7-level sub-ADC; the output of the 7-level sub-ADC is finally passed through the digital calibration and output register module to form the output of the entire ADC.

The core unit of the converter module in Figure 1 is a 7-level sub-ADC, where the structure of the first to sixth level is basically similar: Each sub-ADC consists of a sample-and-hold circuit S/H, a 1.5-bit-accuracy flash ADC, and a multiplying DAC. It is the most critical part of the entire pipelined converter, and its performance determines the performance of the entire pipelined ADC, while the seventh-level sub-ADC is a 2-bit flash ADC. The working process of each sub-ADC is similar: First, the input signal is sampled and held, and the held signal is converted into a digital signal by a 1.5-bit flash ADC; then, it is converted into an analog signal by a multiplication DAC (MDAC). This analog
signal is subtracted from the hold signal to calculate the remainder, and the remainder is amplified by an operational gain amplifier and sent to the next stage.

In order to achieve superior performance such as high speed, low power consumption, high signal-to-noise ratio, etc., and reduce the chip area of the whole ADC, there are some key technologies to be solved in the above pipelined ADC design. First of all, the design of the first-level sub-ADC is very important, which determines the performance of the entire ADC. Therefore, there are key technologies about how to design a first-level sub-ADC with low power consumption, high speed, signal-to-noise ratio, and minimum chip area in a pipelined ADC, especially the design of the operational gain amplifier in the MDAC; Secondly, after the first level ADC completes the design, the second to the sixth level can use the same structure as the first level sub ADC. However, considering the power consumption, signal-to-noise ratio, and chip area of the entire ADC, it can be optimized for the later stages of ADC. For example, a step-by-step scaling technique may be employed, that is, under the premise of satisfying the performance of the overall ADC, the subsequent sub-ADC is lower than that of the first sub-ADC, such as the size of the switch tube, the capacitance and the performance of the amplifier and so on, which can be significantly reduced. This can significantly reduce the chip area of the entire ADC and improve the signal-to-noise ratio of the ADC and other performance indicators. This article focuses on the relevant research on the above two key technologies.

3. Design of the first level sub-ADC
Since the design of the first-level sub-ADC is very important, which determines the performance of the entire ADC. The following describes the circuit structure, simulation results and layout design and so on aspects of the first-level sub-ADC in detail.

3.1. Design of MDAC
The main module in the first-level sub-ADC-- the multiplying DAC (MDAC) has three functions: 1) To calculate the margin, the MDAC divides the input signal and the output of the sub-DAC for Differential operation to calculate the remainder; 2) operation gain, for the convenience of digital calibration, the gain of each level MDAC is best selected as the 2N sub square. The more accurate the gain, the smaller the gain error, the more accurate multiplicative 2 circuit of the switched capacitor is used in the design; 3) Sampling function, Similar to the sample-and-hold circuit.

The structure of the MDAC and the two working states are shown in Figure 2. Fig. 2 (a) is MDAC's circuit structure. Fig. 2 (b) is MDAC’s two working states.
In Fig. 2(b), the two working states of MDAC are the sampling phase and the operation phase. These two states are controlled by the clock signal. Each level requires a three-phase clock to complete the sampling. In the first clock phase, the signal is sampled on capacitors Cs and Cf, that is the so-called double sampling; In the second clock phase, that is the operational gain phase, Cf is flipped to connect as the feedback capacitor, and the sampling capacitor Cs in the input end of the first clock is connected to the reference potential at the second clocks phase, which causes charge redistribution and finally realizes the MDAC’s margin and gain function. This process can be summarized by double sampling and single flipping.

Figure 2. The structure of the MDAC and the two working states

Together with the 1.5 bit precision flash ADC, MDAC can implement the following input and output relationships:

\[
V_o(n) = \begin{cases} 
2V_m + V_{ref} & \text{if } -V_{ref} \leq V_m < -\frac{1}{4}V_{ref} \\
2V_m & \text{if } -\frac{1}{4}V_{ref} \leq V_m < \frac{1}{4}V_{ref} \\
2V_m - V_{ref} & \text{if } \frac{1}{4}V_{ref} \leq V_m < V_{ref}
\end{cases}
\]

In the ADC designed in this paper, the sample-and-hold function is implemented by a clock-controlled switch, that is, the switch in the dotted line in Figure 2(a) and the capacitance module, which
can realize the sampling and holding of the input signal and save the first level sampling and holding circuit. This is the unique feature of the design in this article ADC.

The design of operational amplifier in MDAC is introduced specifically below. The gain of op amp cannot be too low, otherwise it will affect the error of differential nonlinearity in the whole pipelined ADC. The gain requirement of the op amp in the first-level sub-ADC is greater than 63 dB through calculation, and the unity-gain bandwidth requirement is greater than 400 MHz. Therefore, a two-stage op amp architecture is adopted. The first level is the folded cascade, which provides large gain, and the second level provides large swing.

3.2. The results of first-stage ADC simulation
The first stage ADC is simulated. The simulation conditions are: power supply AGND=0 V, AVDD=1.8 V; the temperature is 27°C; the bias current is 101μA; the load capacitance is 400fF.

The input signal during simulation is a differential wave signal. At 300 ns, the differential output voltage is 1.275 V and the differential output voltage is 525 mV at 1μs. The main purpose of this simulation is to verify the transmission function of this level ADC.

Next, the signal processing capabilities of the first level ADC are simulated. A differential sinusoidal signal with a frequency of 11.25 MHz is input, recovered by the ideal DAC, and the recovered signal precision is detected. Then, a fast Fourier transform is performed to obtain the spectrum diagram of the first stage ADC. The SFDR of the first level ADC is 75.01 dB, from which we can know the signal distortion situation of the first level ADC. The above data is exported, and processed by MATLAB tool. The SNR of the first stage ADC is 74.1 dB, and the effective digit ENOB is 11.2 bits.

4. The layout of the entire ADC and actual test results
Based on the above design idea, the design of the entire ADC is completed. Figure 3 is the layout of the entire 8 bit Pipelined ADC.

![Figure 3. The layout of an 8-bit pipelined ADC](image-url)
The above ADC is designed based on 0.18μm process platform. The actual test result after tape-out is: Power consumption current is 22mA; Sample rate is 80MHz, under input signal at 11.25MHz, signal-to-noise ratio SNR can reach 53dB, and the effective number of bits is 7.98bits.

5. Conclusion
This article introduces an 8-bit ADC with a sampling rate of 80 MHz based on 0.18μm process. In this ADC design, the non sample-and-hold technique is realized by accurately designing the op amp structure in each sub-ADC, In addition, the unique design techniques such as step-by-step scaling in the sub-ADC circuit structures at various levels are used, this makes the ADC has a smaller power consumption and chip area, and has a higher signal-to-noise ratio and superior overall performance.

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