Automatic SDF-based Code Generation from Simulink Models for Embedded Software Development

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ABSTRACT
Matlab/Simulink is a wide-spread tool for model-based design of embedded systems. Supporting hierarchy, domain specific building blocks, functional simulation and automatic code-generation, makes it well-suited for the design of control and signal processing systems. In this work, we propose an automated translation methodology for a subset of Simulink models to Synchronous dataflow Graphs (SDFGs) including the automatic code-generation of SDF-compatible embedded code. A translation of Simulink models to SDFGs, is very suitable due to Simulink actor-oriented modeling nature, allowing the application of several optimization techniques from the SDFG domain. Because of their well-defined semantics, SDFGs can be analyzed at compiling phase to obtain deadlock-free and memory-efficient schedules. In addition, several real-time analysis methods exist which allow throughput-optimal mappings of SDFGs to Multiprocessor on Chip (MPSoC) while guaranteeing upper-bounded latencies. The correctness of our translation is justified by integrating the SDF generated code as a software-in-the-loop (SIL) and comparing its results with the results of the model-in-the-loop (MIL) simulation of reference Simulink models. The translation is demonstrated with the help of two case studies: a Transmission Controller Unit (TCU) and an Automatic Climate Control.

CCS Concepts
- Computer systems organization → System on a chip; Embedded hardware;

1. INTRODUCTION
Model-based Design (MBD) of embedded systems is nowadays a standard, easy and efficient way for capturing and verifying embedded software functional requirements. The main idea is to move away from manual coding, and with the help of mathematical models create executable specifications using a certain modeling framework. These frameworks typically provide automatic code generators which generate consistent imperative code ready to be deployed in real environments. Matlab/Simulink [13] is one of the most wide-spread tools for model-based design of embedded systems which combines above features in a single framework. Simulink utilizes block-diagram to represent system models at the algorithmic level. For instance, in case of a control system, the model consists of the controller algorithm block which controls the environment block (or the process to be controlled typically modeled as a set differential equations).

A translation of Simulink models to Synchronous Dataflow Graphs (SDFGs) [12] which are, opposed to Simulink, formally based, is beneficial. Such a translation would pave the way towards the application of several optimization and formal verification techniques well-established for the SDFG domain. For e.g. in a recent work in [7] the formal real-time verification (based on model-checking) of SDF applications running on Multiple-Processor-System-On-Chip (MPSoCs) with shared communication resources was shown to be more viable than the real-time (RT) verification of generic tasks. Also for SDFGs deadlocks and bounded buffer properties are decidable [12]. In addition with the help of mathematical methods easy-to-analyze compile-time schedules can be constructed for SDFGs. Furthermore, memory-efficient code optimization are available [11] to enable efficient implementations of embedded systems.

In this paper, we present a translation procedure of a defined subset of Simulink models to SDFGs based on the work in [24]. We extend the approach in [24] by enabling the translation of Simulink models with multirates features to SDFGs. In addition, we integrate the translation procedure within Matlab/Simulink and utilize the automatic code-generation feature to generate SDF-based code from Simulink models. Moreover, we enable an automatic setup of a verification flow which allows a Software-In-the-Loop (SIL) simulation showing the functional equivalence of the generated code to the reference model.

The paper is structured as follows. We will first recap the basic concepts of synchronous dataflow graphs and Simulink models identifying their main differences. Afterwards, we discuss the related work in Sect. 3 mainly addressing translation approaches of Simulink models to SDFGs. Next we elaborate on our translation procedure in Sect. 4 starting...
Simulink is a framework for modeling of dynamic systems and simulating them in virtual time. Modeling of such systems is carried out graphically through a graphical editor consisting mainly of blocks and arrows (connections) between them representing signals. Each block has its input, output and optionally state variables. The relationship of the inputs with the old state variables and the outputs update is realized through mathematical functions. One of the powerful features of Simulink is the ability to combine multiple simulation domains (continuous and discrete). This is very useful for embedded systems, where in general the controller has discrete model and the environment often needs to be modeled as a continuous one.

Simulink also supports a state-based MoC the Stateflow[21] which is widely used to model discrete controllers. Simulink allows a fast Model-in-the-Loop (MIL) verification, where the functional model (of the controller for example) is simulated and results are documented to be compared with further refinements. In addition, a Software-in-the-Loop (SIL) verification is also possible in which the controller model is replaced by the generated code from the Embedded Coder[19] (usually embedded in a S-function) and the behavior of the code is compared with the reference data achieved from MIL (described above).

In[15] a method was presented to automatically transform SDFGs into SBDs (Synchronous Block Diagrams), such that the semantics of SDF are preserved, and it was proven that Simulink can be used to capture and simulate SDF models. Also authors in[8] support this fact that dataflow models fit well to concepts of block diagrams and are used by Simulink. In general, the MoC of Simulink is much more expressive than that of the SDF having the advantage of being able to relax all limitations of the SDF MoC but at the cost of its analyzability.

3. RELATED WORK

In the last decade, several research[4, 5, 22, 25] have been conducted to enable a translation of Simulink models to other formal models for the purpose of formal analysis. In the following, we merely discuss previous work enabling the translation of Simulink models to SDFGs.

In[14], only the source code of a so-called Simulink2SDF tool was published which enables a very simple translation of Simulink models to SDFGs. In this work all Simulink blocks, without any distinction, were translated to data-flow actors and similarly connections were translated in data-flow channels, the fact which makes the translation incomplete as we will see in Sec.4. In addition, our approach allows the generation of executable SDF-code which is not possible in this approach.

In[6] a translation of Simulink models to homogeneous SDFGs (HSDFGs) was pursued with the objective of analyzing concurrency. HSDFGs are SDFGs with the restriction that the number of consumed and produced tokens of each actor must be equal to 1[10]. The translation has been done for a fixed number of functional blocks but important attributes, such as the data type of a connection between blocks, have
not been taken into consideration by the the translation.

In [13] it was shown how a case study of a vehicle climate control modeled in Simulink is imported to a tool (MoDAL) supporting SDF MoC. MoDAL, in turn, exports the model in a format which can be imported by the Ptolemy tool [11]. Ptolemy is then used to generate code from the SDF model. In [13], only the use-case model have been translated to an SDFG without general defining a translation concept applicable at least to a subset of Simulink models.

In [3] a translation from Simulink models to SDFGs was described. The aim of this work was to apply a methodology for functional verification of Simulink models based on Contracts. Contracts define pre- and post-conditions to be fulfilled for programs or program fragments. In [3], the ability of SDFGs to model multi-periodic Simulink systems was formally proved. There, in addition to systems with harmonic periods, also non-harmonic periods are supported (unlike our work and that of [6] where only harmonic periods are supported). However, authors in above work, give no clear classification of critical Simulink functional blocks (e.g. the switch block with dynamic rates see Sec. [3] which cannot be supported in the translation. In addition, Triggered/Enabled subsystems and other important attributes such as the data type of a connection are not supported. Furthermore, SDF-based code-generation was not considered.

Unlike the above work, we present a general translation concept based on a classification of blocks and connections in Simulink models. Our approach enables the translation of critical blocks (such as Enabled/Triggered subsystems) including the enrichment of the translated SDFG with important attributes such as the data types of tokens, tokens’ size and sampling rates of actors (in case of multi-rate models). This enables a seamless code generation of the model into SDF-based embedded software ready to be deployed on target architecture. We also provide an automation of the process of SDF-based code generation together with the SIL verification to prove the soundness of the translation.

4. SIMULINK TO SDFG TRANSLATION

As already stated (see Sec. 2.2), Simulink MoC is much more expressive than the SDFG MoC. Unlike SDFGs, Simulink supports following additional features:

**U1 Hierarchy** (e.g. subsystem blocks): While in Simulink multiple functional blocks can be grouped into a subsystem, in SDFGs each actor is atomic and therefore no hierarchy is supported.

**U2 Control-flow logic/Conditional** (for e.g. switch block or triggered subsystem see [15]): In Simulink control flow is supported on the block level. This means that depending on the value of a control signal at a block, different data rates could be output by the block. In contrary, in SDFGs data rates at input and output ports of an actor are fixed and control structures are only allowed within the functional code of an actor and can’t be represented in an SDFG.

**U3 Connections**:  

1. **Dataflow without connections** (e.g. Goto/From blocks): In contrast to Simulink, there is no dataflow without a channel connection in connected and consistent SDFGs considered in this paper.

2. **Grouping of connections** (e.g. BusCreator block for bus signals): In Simulink, connections with different properties (e.g. different data types) can be grouped into one connection. This is not possible in an SDFG since the tokens transferred among a channel must have the same properties.

3. **Connection style**: While in Simulink the storage of data between blocks has the same behavior as that of a register where data can be overwritten (in case of multi-rate models), the inter-actor communication via channels in SDFGs follows a (data-flow) FIFO buffer fashion, where tokens must be first consumed before being able to buffer new ones.

**U4 Sampling rates**: In addition to the number of data transported over a connection by every block activation, a periodic sampling rate is assigned to each block in Simulink to mark its periodic activation at this specific frequency. If all blocks exhibit the same sampling periods in a model, then this model is called a single-rate model otherwise it is a multi-rate model. In SDFGs, however, an actor is only activated based on the availability of inputs. Actors do not have explicit sampling periods and therefore data rates can only be represented by the rates assigned to their (input/output) ports.

Because of the above differences, some constraints must be imposed on the Simulink input model in order to enable its translation to an equivalent SDFG, which we will discuss in the following section.

4.1 **Constraints on the Simulink Model**

Only Simulink models with fixed-step solver are supported in the translation. In case of multi-rates, rate transitions should be inserted to the Simulink model and the rates should be harmonic (divisible). These constraints are indispensable to enable deterministic code generation since we aim with the help of Simulink built-in code-generator to generate SDF-compatible executable code for the translated SDF application. Even though it is possible to translate a Simulink model to multiple SDFGs, we deal only with one application (implemented in Simulink) at a time in this paper, which results after translation into one equivalent SDFG. This application is considered to be a control application having the general structure depicted in Fig. 6. Moreover, a correct functional simulation of the Simulink model is a prerequisite for the translation in order to get an executable SDFG. In addition to above general prerequisites, the following constraints are imposed on the input Simulink model to enable the translation:

**E1 Hierarchy**: Hierarchical blocks (e.g. subsystems), in which one or more functional blocks of the types described in U3-1 and U3-2 exist, are not allowed to be translated to

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1Inconsistent SDFGs require unlimited storage or lead to deadlocks during execution[10].
atomic actors. Either these blocks should be removed from
the entry Simulink model (for they serve only visualization
improvement purpose) or the model should be dissolved at
the hierarchy level at which these components exist where
these blocks are translated and connected in accordance
with the rest of the SDFG. This constraint is mandatory,
otherwise if we allow an atomic translation of such hierar-
chical functional blocks, their contained functional blocks
of the form U3-1 and U3-2, which may be connected with
functional blocks in different hierarchical levels, would dis-
appear in the target SDFG. A translation of these blocks
would thus no longer be possible and would cause a mal-
function of the target SDFG (see restriction E3).

E2 Control-flow logic/Conditional: Blocks such as
Triggered/Enabled subsystems can be translated just like
the general subsystems. Upon dissolving the hierarchy of
such subsystems, the control flow takes place now within
the atomic functionality of the actor without being in con-
tradiction to SDFG semantics (c.f. Sec. 2.1). In such a
translation, however, additional control channels must be
defined (see Sec. 4.2). Yet, the case described in U2
must still be prohibited. In order to do that, there is an option
“allowing different data input sizes” in Simulink for such
blocks, which when disabled, prohibits outputs of variable
sizes of a control block

E3 Connections

1. Dataflow without connections: For blocks hav-
ing the same behavior described in U3-1 (such as
From/Goto or DataStoreRead/DataStoreWrite blocks),
we assume that the source block (e.g. DataStoreWrite
block), intermediate block (e.g. DataStoreMemory
block) and the target block (e.g. DataStoreRead block)
which communicate without connections are available in
the input Simulink model. This constraint is important
for Simulink allows instantiating a source blocks without
for instantiating e.g. the sink block.

2. Grouping of connections: In order to support the
translation of Simulink models with blocks having the
same behavior as those described in U3-2, two con-
straints must be imposed. The first one is that every
block which groups multiple signals (e.g. BusCreator)
to one signal must be directly connected to a block
which have the opposite functionality (e.g. BusSelec-
tor). The second constraint is imposed on the block
(e.g. BusSelector) which takes the grouped signals and
splits them again. An “Output as bus” should be prohi-
bited in the options of this block. By doing this, grouping
of signals for better visibility in the Simulink model is
still with the limitation above allowed, while prohibiting
grouping of signals of different parameters in one signal
in the target translation.

Figure 2: Original Simulink model: Red having a sample
time of 2, Green having a sample time 4

4.2 Translation Procedure

In the following, we will roughly describe the translation procedure implemented to extract an SDFG from a Simulink
model with the help of an academical Simulink multirate
example in Fig. 2. For the translation two main phases
are required: the pre-translation phase where the original
Simulink model is prepared and checked for the above de-
finied constraints and the translation phase where the trans-
lation takes place.

1. Pre-Translation phase:

(a) Checking Requirements: Here the Simulink
model is checked if it fulfills the constraints described
above. If this is not the case the translation is
aborted with an output of the list of unfulfilled con-
straints.

(b) Dissolving hierarchy: In this step, a top-down
flattening of the Simulink model (respecting E1),
till the required depth level is reached, is done (see
Fig. 3).

(c) Removing connecting blocks of type U3-
1/U3-2: Here, blocks respecting the E3-1/E3-2
constraint are removed. When doing this, the pre-
decessor block of the source block (e.g. DataS-
toreWrite block) is directly connected either to the
intermediate (if existent) block (e.g. DataMem-
ory block) or to the successor block of the target
block (e.g. DataStoreRead block) and these con-
necting blocks (source and target blocks) are re-
moved (see Fig. 4 where BusCreator/BusSelector
and Goto/From blocks are removed).

2 According to [18] blocks having this option are: Action-
Port, Stateflow, Enable/Trigger Subsysteme, Switch, Multi-
port Switch and Manual Switch.

3 e.g. BusCreator/BusSelector, Bus Assignment and Merge
blocks [18].
2. **Translation phase:** In this step, the modified Simulink model is directly translated into an SDFG (see Fig. 8) according to the following procedure:

(a) **Translation of blocks:** If \( B \) is the set of all blocks in Simulink model \( M \) then each block \( b_i \in B \) in \( M \) is translated into an unique actor in the translated SDFG \( a_i \in A \) (where \( A \) is the set of actors see Fig. 8).

(b) **Translation of connections:** Each output port \( b_{i.o} \) is translated into a unique output port \( a_{i.p_o} \) and each input port \( b_{i.i} \) is translated into a unique input port \( a_{i.p_i} \). In case multiple connections \( t_1, t_2, \cdots, t_n \) going out from an output port \( p_{o1} \) in Simulink (which is permitted in Simulink but not in the SDFG, see connections of statechart before Fig. 2) and after translation Fig. 5, then for each one of these connections, the output port is replicated \( p_{o1}, p_{o2}, \cdots, p_{o1m} \) (each having the same properties) in the resulting SDFG, in order to guarantee that every channel \( d \in D \) (set of all channels in an SDFG) has unique input and output ports. Now, each connection \( t \in M \) in the Simulink model is translated into a channel \( d \in D \) in the SDFG (see Fig. 8).

(c) **Extraction of Tokens’ sizes and types:** The number of the data transferred over a connection represents the size of a token produced/consumed when an actor fires (e.g. \texttt{Constant} actor produces a token of size 2 in Fig. 8) and their data type represents the data type of that token (e.g. \texttt{double} in Fig. 8). These parameters can be extracted from the model for every connection.

(d) **Handling Multi-rates:** The following method for handling multirates was inspired from [25]. To determine the rates of the actors’ input and output ports we must differentiate between three cases: \textit{fast-to-slow} transition, \textit{slow-to-fast} transitions and transitions between blocks having the same rates. For the latter case, source and destination actors are denoted by a rate of 1 on their ports indicating the production/consumption of one token (of specific size per channel) whenever activated. In case of \textit{slow-to-fast} transition (see e.g. in Fig. 6 and in Fig. 10), the rate of the output port of the rate-transition actor

\[ R.p_0.ratio = \frac{b_{src}.sp}{b_{dst}.sp}, \]  

where \( p_0 \) is the output port of the actor \( R \), \( b_{src} \) and \( b_{dst} \) are the source and destination blocks connected via rate-transition block and \( sp \) the sample time of the corresponding block. The rate of the input port of \( R \) is set to 1. This basically realizes multiple copies of tokens of the slower actor for the faster actor to run.

In case of \textit{fast-to-slow} transition, the rate \( R.p_i.ratio \) of the input port \( (p_i) \) of the rate-transition actor \( R \) can be calculated as follows:

\[ R.p_i.ratio = \frac{b_{dst}.sp}{b_{src}.sp}, \]
The output port rate is set to 1. This mainly accumulates tokens on the rate-transition actor and outputs the most fresh token of the faster actor. Furthermore, in this case a number of delay tokens equal to:

$$d_{\text{delay}} = \left( b_{\text{dst}}/b_{\text{src}} \right) - 1, \tag{3}$$

are placed on the input channel $d \in \mathcal{D}$ of the rate-transition actor in order to enable considering the initial token produced by the fast actors at the first firing (see Fig. 7 and Fig. 8).

\( e \) Adding event channels: if the subsystem is a triggered one, depending on the hierarchy level chosen, extra connections are added in this step for handling (enabling/triggering) events. These edges are needed when the hierarchy of a enabled/triggered subsystem has to be sensitive to the (triggering/enabling) event and thus is connected with the event source.

Finally, the actors in the resulting SDF graph can be statically scheduled to obtain a minimal periodic static schedule (Constant Constant1 Product)\(^2\) (RateTransition UnitDelay Chart Out1 Out2).

### 4.3 Code-generation and SIL Simulation

After describing the translation procedure of Simulink models into SDFGs, we will describe in the following the corresponding implementation on top of Simulink and how to utilize Simulink code-generator to enable SDF code generation and SIL verification. Generating an equivalent SDF-compatible C code is useful to verify the functional equivalence between Simulink models and the generated SDFGs on one side, and to enable the direct code deployment on
target hardware platforms, on the other side.

Fig. 9 shows the different steps involved in the model transformation process within our code-generation framework. The code generator constitutes the major part of our model transformation, taking the Simulink model as an input and generating the SDF code and the verification (SIL) model as output. We implemented the code generator as a Matlab script taking use of the Matlab API to manipulate and extract needed information from Simulink models. The implemented code generator constitutes mainly of the following functions:

- **Check Requirements:** the Simulink model is checked if it fulfills the constraints described Sect. 4.1 For e.g. in case of multirates, the rates are checked whether or not these are integers and divisible.

- **Clean Model:** in this step, the chosen subsystem (to be translated) is restructured according to the pre-translation phase (see Sect. 4.2); hierarchies dissolved, routing blocks dissolved and rate-transition blocks inserted. In addition, every block of the desirable hierarchy is packaged in a subsystem and the connections are updated since the code-generation is only possible for subsystems.

- **Generate SDF Code:** this function uses the Simulink Embedded Coder and an SDF API to generate SDF-based embedded C code from the modified model of the previous step (see example at the right of Fig. 9). In this case, embedded C code is first generated for each block at the chosen hierarchy level. The SDF-based C code is generated by using the predefined SDF library files (.sdfg.h, .sdfg.c) implemented according to description in [23]) that have been already loaded into the folder structure. The output are two files (.sdfg.<name>.h, .sdfg.<name>.c) for every SDFG, in which the actors and channels are defined and instantiated according to the translation concept. For each actor a corresponding function is generated (E.g. Product_actor() see Fig. 9, in which data availability of every input channel is checked (implemented as FIFO queue) and, if all inputs are read (E.g. dequeue(q1, P_U_In1)), the actor executes its own computation behavior (implemented in a step function for e.g. Product_step()) and the results are written into its output channels (E.g. enqueue(q3, P_Y_Out1)). Addition, a basic valid static schedule is generated and implemented for the SDFG (see sdfg_step() in Fig. 9).

- **Generate Verification model:** the latest step targets the realization of a SIL-simulation (see bottom-right of Fig. 9). For this, we further enhance the code generator to allow the automatic integration of the generated SDF-compatible code into a C file of an S-function block. The S-function block is then automatically generated and inserted into a new-created verification model. The verification model includes also the original subsystem (controller) with the environment model. The S-function has the same interfaces as the original subsystem which allows a seamless SIL simulation with the environment model. Doing this, the functional equivalence of the translated model and the original one, can be verified automatically.

5. **EVALUATION**

We have conducted two experiments to demonstrate the viability of our approach being able of translating a Transmission Controller Unit (TCU) model (c.f. [16]) and a Climate Controller model (c.f. [17]) each to a corresponding SDGF and to generate for each case an equivalent SDF C code.

The TCU model depicted in Fig. 10 is a typical model exhibiting multirates. The translation for the TCU subsystem (see at the bottom of Fig. 10) was straightforward since the model respected (per construction) the constraints made in Sect. 4.2. Fig. 11 shows that the outputs (impeller torque, output torque) of both the reference TCU and the generated SDFG-compatible TCU code are equivalent.

More complexity is exhibited by the Automatic Climate Control System (seen in Fig. 12), where the Heater controller subsystem was translated. In addition to the variety of blocks used, the Heater subsystem is a triggered system which only executes when the enable signal is true. As seen in the generated SDFG (see Fig. 12), the Enable actor is connected via extra-created channels to all actors within the Heater_Control SDGF. Only if a true value arrives at these dedicated channels, then the corresponding actor will be activated to perform its internal computation. If this is not the case, the actor will read its input queues, skip the computation part (step function) and update output queues with values of the previous step results. Also the SIL and MIL results of this experiment show equivalent values as depicted in Fig. 13 concluding a functionally equivalent SDF code-generation.

6. **CONCLUSION**

In this work, a translation approach for Simulink models (respecting defined rules) to SDGFs was presented. Thanks to the automated code-generation of SDF code from the original Simulink model and the Software-in-the-loop simulation, tests can be automated to show the functional equivalence of this translation. The translation was demonstrated successfully with a medium-sized Transmission Controller Unit model from the automotive domain and with a Climate Controller use-case. In future work, we will take a look at the possibility of optimizing the code-generation of Simulink models for MPSoCs. For this, we can take use of the generated SDF code and mature optimizing/parallelization techniques from the SDF research domain [1] [2] to enable efficient implementations of embedded systems.

7. **ACKNOWLEDGMENTS**

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Figure 10: SDF code-generation of the transmission controller model [16] (with slow-to-fast transitions)

Figure 11: Verification results of the Transmission control model showing equivalent outputs of the SIL (see Fig. 11b) and the MIL (see Fig. 11a) simulations.

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Figure 12: SDF code-generation of the single-rate triggered Climate controller model [17].

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