Offset Cancellation and Programmable Gain Design for Switched Capacitor Amplifier in Digital DC-DC Converter

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Abstract. This paper presents a fully differential switched capacitor amplifier with programmable gain design and offset cancellation technique used in digital DC-DC converter. To trade off the effective resolution for dynamic range of the error ADC, the gain of the switched capacitor amplifier is designed programmable that can be configured 1X, 2X, 4X or 8X. To improve system offset performance, the first stage is utilized full-differential switch-capacitor architecture conducive to common mode noise rejection and differential offset cancellation caused by charge injection. In addition, to cancel the offset brought by amplifier input stage, offset cancellation techniques are also implemented. The offset voltage is stored in calibration capacitor in sampling phase and cancels the input offset in amplification phase. This proposed circuit is simulated in 180nm 4P6M CMOS technology. From the simulation result, the offset voltage is fully cancelled. In addition, programmable gain design is also verified that dynamic adjustment accuracy in DC-DC feedback loop in X8 is superior than X1.

1. Introduction
Digital controllers offer advantage of low power, flexibility of configuration, immunity to analog component variation, compatibility with digital system and high-speed operation in faster design process compared with analog controllers. Owning to these characters, digital DC-DC converters become necessary in applications of networking, telecommunication equipment or FPGA, DSP and memory power.

The overall digitally controlled buck converter architecture is shown in Fig. 1. The Analog Front End (AFE) consists of differential amplifier, error amplifier, reference generation block and error ADC. The output voltage of the DC-DC converter is sensed onto the P-side of the differential amplifier, and the N-side of the differential amplifier is connected to Gnd. The differential input voltage is sensed, and then the voltage is transferred to the error amplifier where the value is subtracted from the set-point reference which is generated by the DAC. The obtained analog error voltage is converted to a digital value by the error ADC (EADC) and is fed into the digital compensation filter. The compensated error signal out of the digital compensator is applied to the high resolution digital pulse width modulator (DPWM). The driving force of the pulse width signal is enhanced by the driver and then the signal is implemented on the power stage. Through the whole closed loop operation, the output voltage of the DC-DC converter is regulated almost equal to the reference value.
When choosing the architecture of amplifier, offset may be a major consideration which can cause deviation from reference voltage to output voltage various between chips due to random device mismatches. In high-speed application, conventional analogy amplifier exhibits a tradeoff between speed and system offset [1]. Offset voltage gradually increases with CMOS scaling, as does the $V_{TH}$ variation. To address this problem, this paper develops a kind of switched capacitor topology amplifier, which exhibits low offset performance. With offset cancellation technique, the offset of switched capacitor amplifier is fully cancelled. To improve the effective quantization resolution in relatively stable operation condition and to improve the dynamic response in fast change in working condition, the amplifier is added programmable gain design. What’s more, this structure also owns the character of combination of signal sensing and error amplification.

What’s more, to improve the flexibility that trades off the effective resolution for dynamic range of the error ADC. The gain of the amplifier is designed programmable that can be configured 1X, 2X, 4X or 8X.

This paper mainly presents and analyzes the new architectures and techniques used in the amplifier in AFE. The structure is organized as follows. Section II describes the whole structure of switched capacitor amplifier and new design analysis. Section III presents the simulation results with the 180-nm CMOS technology.

2. Switched capacitor amplifier

2.1. Switched capacitor amplifier structure
Switched capacitor amplifier proposed in this paper, combine the function of signal sensing and error amplification. Namely, the switched capacitor topology replaces the function of differential amplifier and error amplifier in AFE shown in Fig. 1.

Programmable gain design is proposed in this structure. The gain is designed programmable that can be configured 1X, 2X, 4X or 8X, namely, $G_{AFE} = 1, 2, 4, 8$. This flexibility trades off the effective resolution for dynamic range of the error ADC.

When the output dynamic fluctuation varies not so much with small or no change in the load in DC-DC loop, the gain can be set 8X or 4X to improve the effective quantization resolution of AD. When DC-DC system is undergoing a fast change in the load or performing a soft-start in DC-DC system, the gain can be set 1X or 2X to improve the dynamic response in feedback loop.
Low offset performance in amplifier are also the most important consideration [2, 3]. Offset in amplifier may bring in system offset and finally induce deviation from reference voltage to output voltage which varies between chips due to random device mismatches.

The key circuit design includes two stages as shown in Fig. 9. The first stage utilized full-differential switch-capacitor architecture conducive to common mode noise rejection realizes sample-and-hold and signal amplification using two-phase clock. The second stage converts the difference signal of the full-differential switch-capacitor amplifier’s output to single signal which is then fed into error ADC.

In Fig. 9, C_a1, C_a2 and C_a3 are sampling capacitor. The charges accumulated in C_a1 ~ C_a3 during sampling period are redistributed in both C_a1 ~ C_a3 and C_b1, C_b2 in amplifier phase. In this design C_a1=C_a2=C_b1=C_b2=C_a3/2=C. C_calibca is used to calibrate the offset voltage in input stage of the full-differential amplifier. S_samp and S_conv controlled by two phase non-overlap clock are sampling and converting switches. The amplifier is in sampling phase when S_samp is closed, and in converting phase when S_conv closed. S_gc1, S_gc2, S_gc3 and S_gc4 are gain setting switches. Gain of switched capacitor amplifier can be configured 1X, 2X, 4X or 8X through setting S_gc1 ~ S_gc3. S_d2s determines when difference output of the first stage converts to single signal. The timing diagram of S_samp, S_conv and S_d2s is shown as Fig. 2. ‘1’ represents switch closed and ‘0’ represents open.

![Timing diagram of S_samp, S_conv, and S_d2s](image)

In sampling period, input voltage is sampled and hold. The sampled input signal is amplified in amplification phase, and during the differential to single period, the full-differential output of first stage is converted to single signal.

### 2.2. Programmable Gain Design

As described, to improve the flexibility that trades off the effective resolution for dynamic range of the error ADC. The gain is designed programmable that can be configured 1X, 2X, 4X or 8X, namely, \( G_{AFE} = 1, 2, 4, \) or \( 8 \). The switch configuration between different gain settings is shown in TABLE I. ‘1’ represents switch closed and ‘0’ represents open.

| Gain | S_gc4 | S_gc3 | S_gc2 | S_gc1 |
|------|-------|-------|-------|-------|
| 1X   | 0     | 1     | 0     | 0     |
| 2X   | 1     | 0     | 0     | 0     |
| 4X   | 1     | 0     | 0     | 1     |
| 8X   | 1     | 0     | 1     | 1     |
$S_{gc3}$ and $S_{gc4}$ control the topology in 1X mode or multiple gain mode. $S_{gc1}$ and $S_{gc2}$ determine the value of sampling capacitor. As $C_{a1}=C_{a2}/2=C$, when $S_{gc1}$ and $S_{gc2}$ are all in ‘0’ state, the sampling capacitor value is $C$. When $S_{gc1}$ in ‘1’ state and $S_{gc2}$ in ‘0’, the sampling capacitor value is $2C$. When $S_{gc1}$ and $S_{gc2}$ are all in ‘1’. The sampling capacitor value is $4C$.

In 1X setting, $S_{gc3}$ is closed and $S_{gc1}$, $S_{gc2}$, $S_{gc4}$ are open, as shown in Fig. 10. The simplified circuit is shown in detail in Fig. 3. Fig. 3 (a) shows the key circuit operating in sampling period, and Fig. 3 (b) display the circuit in amplification period.

Fig 3. (a) (b) Simplified circuit in 1X setting.
In 2X setting, \( S_{gc4} \) is closed and \( S_{gc1}, S_{gc2}, S_{gc3} \) are open. The simplified circuit is shown in detail in Fig. 4. Fig. 4 (a) shows the key circuit operating in sampling period, and Fig. 4 (b) display the circuit in amplification period.

![Simplified circuit in 2X setting](image)

(a) Circuit in sampling phase.

![Simplified circuit in 2X setting](image)

(b) Circuit in amplification phase.

**Fig 4.** (a) (b) Simplified circuit in 2X setting.

In 4X setting, \( S_{gc4}, S_{gc1} \) are closed and \( S_{gc2}, S_{gc3} \) are open. Replacing \( C_{a3} \) in 2X setting with \( C_{a3}+C_{a1} \), the sampling capacitor value is 2C, and gain of the switched capacitor amplifier is changed to 4X. In similar, In 8X setting, \( S_{gc3} \) is open and \( S_{gc1}, S_{gc2}, S_{gc4} \) are closed. Replacing \( C_{a3} \) in 2X setting with \( C_{a3}+C_{a2}+C_{a1} \), the sampling capacitor value is 4C, and the gain is changed to 8X, as shown in Fig. 11.

With the programmable gain design, effective ADC resolution and digital error voltage dynamic range in input of the switched capacitor circuit is shown in TABLE II.
TABLE II. SWITCH configuration between different gain setting.

| AFE Gain | Effective ADC resolution (mV) | Digital error voltage dynamic range (mV) |
|----------|-------------------------------|----------------------------------------|
| 1X       | 8                             | -32 to 31                               |
| 2X       | 4                             | -64 to 62                               |
| 4X       | 2                             | -128 to 124                             |
| 8X       | 1                             | -256 to 248                             |

2.3. Offset Analysis
To cancel the offset in amplifier, offset cancellation techniques are also implemented in this paper. The offset cancellation process is analyzed in 2X setting and simplified circuits analyzing offset are shown Fig. 5. The node voltages used in calculation is noted as below and an offset voltage $V_{OS}$ is added in the input end of the fully differential amplifier.

(a) Simplified circuit analyzing offset in sampling phase.

(b) Simplified circuit analyzing offset in amplification phase.

**Fig 5.** (a) (b) Simplified circuit analyzing offset in 2X setting.
In sampling phase, \( V_X = V_Y = V_{CM} \). \( V_P \) and \( V_N \) are equal in negative feedback stable state, assuming \( V_P = V_N = V_{CM} \). In P-side of the amplifier, the node voltage of right plate in \( C_{calibra} \) is \( V_P + V_{OS} = V_{CM} + V_{OS} \), and the left plate is \( V_{CM} \). So the voltage among \( C_{calibra} \) is \( V_{OS} \). In N-side of the amplifier, the voltage among \( C_{calibra} \) is 0V, as shown in Fig. 5(a). In addition, charges in node \( V_X \) and \( V_Y \) can be expressed as:

\[
Q_{\text{sample,} \, V_X} = (V_{CM} - V_{in}) C_a - V_{OS} C_{calibra} \quad (1)
\]

\[
Q_{\text{sample,} \, V_Y} = (V_{CM} - V_{ip}) C_a \quad (2)
\]

In amplification phase, as shown in Fig. 5(b). The voltage among \( C_{calibra} \) in P-side and N-side are also \( V_{OS} \) and 0V, as the right plate of \( C_{calibra} \) has no voltage connected. Assuming A is the gain of the fully differential amplifier and \( V_P - V_N = (V_{op} - V_{on})/A \), \( V_X - V_Y \) can be calculated as:

\[
V_X - V_Y = (V_P + V_{os} - V_{os}) - (V_N + 0)
= V_P - V_N = (V_{op} - V_{on})/A \quad (3)
\]

As can be seen, the offset voltage is stored in \( C_{calibra} \) in sampling phase and cancels the input offset in amplification phase. So \( V_X - V_Y \) is irrelevant to \( V_{OS} \). In this phase, charges in node \( V_X \) and \( V_Y \) can be expressed as:

\[
Q_{\text{amp,} \, V_X} = (V_X - V_{ip}) C_a + (V_X - V_{in}) C_{b1} - V_{OS} C_{calibra} \quad (4)
\]

\[
Q_{\text{amp,} \, V_Y} = (V_Y - V_{in}) C_a + (V_Y - V_{ip}) C_{b1} \quad (5)
\]

According to charge conservation, \( Q_{\text{sample,} \, V_X} = Q_{\text{amp,} \, V_X} \), \( Q_{\text{sample,} \, V_Y} = Q_{\text{amp,} \, V_Y} \). So, \( Q_{\text{sample,} \, V_X} - Q_{\text{sample,} \, V_Y} = Q_{\text{amp,} \, V_X} - Q_{\text{amp,} \, V_Y} \). \( C_{b1} = C_{b2} = C_b \), the relationship between input and output is then reduced to:

\[
V_{op} - V_{on} = \frac{2C_a}{C_b} (V_P - V_{in}) - \left( \frac{C_a + C_b}{C_b} \right) (V_X - V_Y) \quad (6)
\]

As \( V_X - V_Y = (V_{op} - V_{on})/A \), we can get:

\[
V_{op} - V_{on} = \frac{2C_a}{C_b} (V_P - V_{in})
= \frac{2C_a}{AC_b} (V_P - V_{in})
= \frac{2C_a}{1 + \frac{1}{AF}} (V_P - V_{in}) \quad (7)
\]

In the equation above, \( F = C_b / (C_a + C_b) \), and we can see that the offset \( V_{OS} \) can fully be cancelled in the relationship between input and output. When \( 1/AF \) is ignored compared to 1, the equation of \( V_{op} - V_{on} \) can be rewritten as:
In 2X setting, \( C_a \) is configured equal to \( C_b \). In 4X setting, \( C_a = 2C_b \), and in 8X setting, \( C_a = 4C_b \). Replace \( V_{ip} \) with \( V_{ip} + V_{\text{CON}} \) and \( V_{in} \) with \( V_{in} + V_{\text{REF}} \), the equation of \( V_{op} - V_{on} \) from Fig. 4. Can be reduced to:

\[
V_{op} - V_{on} = \frac{2C_a}{C_b} (V_{ip} + V_{\text{CON}} - (V_{in} + V_{\text{REF}}))
\]

\[
= \frac{2C_a}{C_b} (V_{ip} - (V_{\text{REF}} - V_{\text{CON}}) - V_{in})
\] (9)

3. Simulation results

This proposed switched capacitor amplifier is designed in 180nm 4P6M CMOS technology. The amplifier pre-layout simulation is done at 3.3V and 4MS/s sampling rate. When verifying the architecture in the whole digitally DC-DC loop, switch frequency is set to 1M Hz.

Fig.6 shows the influence of offset in switched capacitor amplifier on DC-DC loop. When offset of amplifier is 0V, output of the DC-DC loop is 1V, and when offset is increased to 10mV and 20mV, output voltage also has the same change tendency. To warrant the output accuracy of the whole DC-DC loop, offset cancellation must be taken into consideration.

Fig.7 illustrates offset cancellation function of the proposed switched capacitor amplifier. The common mode output voltage of the amplifier is 0.8V. So the output of the second stage of the amplifier equals to 0.8V as well when there is no offset. The upper curve shows the offset influence on switched capacitor amplifier without offset cancellation. When offset voltage in input stage is increased to 5mV and 10mV, output of the second stage also has the same deviation value to 0.8V. So, offset voltage in input stage is transferred to output with the same magnification. The lower curve shows the offset influence on switched capacitor amplifier with offset cancellation. To verify the offset cancellation function effectively, add 25mV and 50mV in offset voltage to input stage. Though offset is increased to 25mV and 50mV, output voltage just changes smaller than 0.2mV. The 0.2mV voltage change is due to the DC operating point variation caused by offset voltage. So the offset voltage is almost fully cancelled.
Programmable gain design is also verified in behavior model. Fig.8 shows the influence of gain setting on loop adjustment process. If the resolution of AD in DC-DC loop is 8mV/LSB, the effective resolution changes to 1mV when gain is set to X8. So the dynamic adjustment accuracy in X 8 is superior than X1.

4. Conclusion
A fully differential switched capacitor amplifier with programmable gain design and offset cancellation technique is presented in this paper. Gain of switched capacitor amplifier can be configured 1X, 2X, 4X or 8X through setting the switches which determine whether the sample capacitors or proportional capacitors are connected in the circuit. The offset cancellation technique are also implemented in this structure with the offset calibration capacitor. This proposed circuit is simulated in 180nm 4P6M CMOS technology. From the simulation result, the offset voltage is fully cancelled. In addition dynamic adjustment accuracy in DC-DC feedback loop in X8 is superior than X1. So that X8 or X4 is used in small output dynamic fluctuation condition and X1 or X2 is used in fast change in the load or performing a soft-start in DC-DC system.
Fig 9. the whole structure of the switch-capacitor amplifier.

Fig 10. switch configuration in 1X setting.
Fig 11. switch configuration in 8X setting.

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