Development of monolithic dye sensitized solar cell fabrication with polymer-based counter electrode

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Abstract. Fabrication of monolithic dye sensitized solar cell (DSSC) has been developed by using a poly(3,4 ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) polymer as counter electrode. The number of layers and annealing temperature of PEDOT:PSS layers which is prepared by screen printing technique has been investigated to find the optimum performance of monolithic DSSC. The best performance of monolithic DSSC with 0.61 V open circuit voltage, 1.26 mA short circuits current, and 1.77% efficiency were resulted in 3 layers of PEDOT: PSS with annealing temperature at 120°C. The conductivity of counter electrode layer increase with the increasing of number of polymer layer, produce a high short circuit current. Otherwise, increasing the annealing temperature of PEDOT:PSS layer increases the conductivity of counter electrode layer, but decreases the I_{SC} value.

1. Introduction

Dye-sensitized solar cell (DSSC) has been considered as a promising alternative to replace solid-state silicon based solar cells due to its lower production cost. The attractive and colourful appearance, flexibility, transparency, as well as its short energy payback time have also became selling points that boost interest on the further development of DSSC. Conventional DSSC constructed by two transparent fluorine-doped tin oxide (FTO) coated glass substrates. One substrate is coated with titania (TiO2) as an electrode, another substrate is coated with platinum (Pt) as counter electrode. After TiO2 layer is immersed in ruthenium dye, the substrates then assembled with sealant, leaving a gap between substrates used to fill the electrolyte. In order to reduce the fabrication cost of conventional DSSC, a monolithic structure was developed. In monolithic structure of DSSC, the substrate used is reduced by using a single FTO glass substrate and a low-cost carbon layer as a counter electrode [1]. TiO2 electrode layer and carbon counter electrode layer were formed on the same FTO glass substrate. To prevent contact between TiO2 electrode layer and carbon counter electrode layer, zirconia (ZrO2) layer was introduced. ZrO2 layer also serves as an electrolyte storage. To protect cells from the outside environment, the cell is covered with a transparent glass slide (not FTO covered glass). The structure of conventional and monolithic DSSC is presented in figure 1.

Counter electrode is one of the important components in DSSC. Besides having a main function as a cathode, it also serves as a catalyst for reducing the electrolyte that regenerates dye. The choice of
material to be used as a counter electrode shall be materials having high catalytic activity and stability to the electrolyte used in the cell. Superficial electron transfer between counter electrode and electrolyte reduces the series resistance. This will improve filling factor and result in high conversion efficiency. The reaction occurring at the counter electrode depends on the redox species used to transfer electrons between the electrode and counter electrode [2]. Large surface area, chemically stable forms, mechanical integrity, and low charge transfer resistance are important things to consider in making a good counter electrode. Platinum is the first choice as an electrode counter to DSSC because of its ability to rapidly reduce tri-iodide. However, the drawbacks are platinum price is still quite expensive to be produced commercially [3].

Typically, carbon is used as a counter electrode in monolithic DSSC. However, carbon-based materials do not have conductivity and catalytic ability comparable to those of commercialized TCO/Pt. The carbon-based counter electrode is too thick to attain adequate conversion efficiency, and it is also not suitable for flexible type DSSC. Therefore, there is still a lot of space for adapting new materials for counter electrode [4]. In this research, polymer-based was developed as a counter electrode in monolithic DSSC. Poly(3,4 Ethylenedioxythiophene):poly(Styrene Sulfonate) (PEDOT:PSS) conductive polymer was used because it has high electrical conductivity and the easy process of printing into coating [5, 6]. Influence of the number of layers made by screen printing method and the annealing temperature of PEDOT:PSS counter electrode were investigated in order to optimize the monolithic DSSC performance.

2. Experimental Methods
2.1 Preparation and characterization of PEDOT:PSS counter electrode layer
FTO glass substrates (TEC 15) were ultrasonically cleaned in detergent, deionized water, and isoprophyl alcohol for 10 min, respectively. After being dried in air, PEDOT:PSS paste (EL-P 5015) was printed on the conductive side of the FTO glass using semi-automatic screen printer (LS-15G1N Newlong Seimitsu Kogyo). The printing area was 1 x 1 cm². The the number of layers was varied from one to four layers, wherein the film was dried in a vacuum oven at 70 °C for 20 min after each cycle. The films were subsequently annealed with various temperatures at 100, 120, 140 and 160°C for 30 min in a vacuum oven production of The Grieve Corporation.

The thickness of PEDOT:PSS counter electrode layer were measured using thickness gauge meter. The conductivity of the films was measured using four-point probe (Alessi) with Hewlett-Packard 3468A multimeter and 6186C DC current source. Meanwhile, the surface roughness of the films was observed using atomic force microscopy (AFM) Park Systerm XE7.

2.2 Fabrication and characterization of monolithic DSSC
FTO glass substrates were scribed with sandblasting to separate the designated anode and cathode side. Then, the substrates were cleaned ultrasonically in detergent, deionized water, and isoprophyl alcohol, successively, for 10 min each. After being dried in air, TiO₂ paste (18NR-AO) was printed on the conductive side of substrates with an area of 0.7 x 1 cm². The deposition was carried out in two cycles, wherein the film was dried in an oven at 150°C for 10 min after each cycle. The films were subsequently annealed at 450 °C for 30 min in a conveyor belt furnace (Radiant Technology
Corporation). The annealed films were then immersed in 40 mM of TiCl₄ aqueous solution at 70°C for 30 min as a post-treatment, followed by annealing at 450 °C for 30 min. A porous ZrO₂ paste (Solaronix) with an area of 0.7 x 0.7 cm² was screen printed on the top of the TiO₂ layer and then annealed at 500 °C for 30 min. PEDOT:PSS paste was subsequently deposited on top of the TiO₂ and ZrO₂ with an area of 0.8 x 0.5 cm². The deposition was carried out in four cycles to vary the number of layers from one to four layers, wherein the film was dried in a vacuum oven at 70 °C for 20 min after each cycles. After that, the films were annealed in various temperatures at 100, 120, 140 and 160 °C, respectively, for 30 min in a vacuum oven.

To sensitize the TiO₂ particles, all samples were soaked in dye solution Z 907 with a concentration of 20 mg/L overnight under dark condition. After dried in air, the cells were then encapsulated using thermoplastic sealant (Surlyn). Liquid electrolyte containing I²⁻/I⁻ redox mediators were immediately injected through the empty space allocated in the Surlyn, followed by sealing the cells.

The current-voltage characteristics has been done to analyze the photovoltaic properties of the cells using a national instrument I-V measurement system under simulated solar irradiation with AM1.5G filter and an intensity of 500 W/m². The measurements were conducted at room temperature under illuminated condition. The active area of each cell was defined to be 0.5 x 0.5 cm².

3. Results and Discussion

3.1. Analysis of PEDOT:PSS counter electrode layer

In this research, the number of layer and the annealing temperature of PEDOT:PSS layer were varied in order to produce the optimum monolithic DSSC characteristic. Figure 2 shows the thickness relationship to the number of layers and annealing temperatures of PEDOT:PSS.

It can be seen in figure 2 that the number of layers linearly increasing the layer thickness. The increasing in thickness occurs due to the addition of the number of layers reaches in the range of 40-60%. On the contrary, the higher annealing temperature produces a thinner layer. The decreasing in thickness reaches about 60-90%. The loss of solvent content, especially in the inter-particle fluid at low temperature levels and then adsorbed fluid between particles at high temperatures is suggested as the cause of PEDOT:PSS layer thickness decrease when the annealing temperature increase [8].

The influence of number of layers and annealing temperatures of PEDOT:PSS layer on sheet resistivity values also presented in figure 2. By increasing the number of layers, the resistivity of the layer becomes decreased or the conductivity increased. The similar results were obtained with the annealing process, where the sheet resistivity is decreased with increasing temperature annealing. The shrinkage of the PSS shell that surrounds the conductive PEDOT grains caused by the evaporation of
solvent is suggested as the cause of PEDOT:PSS sheet resistivity decrease when the annealing temperature increase [8]. Nursam et.al reported that the sheet resistivity of the FTO glass is 13.6 Ω/sq, platinum deposited by printing method is 10.9 Ω/sq, and carbon deposited by printing method is 9.9 Ω/sq [7]. The sheet resistivity of the PEDOT:PSS layer resulted from the data in figure 4 is 7.5 Ω/sq, which is smaller than FTO glass, platinum, and carbon. The sheet resistivity of 7.5 Ω/sq was resulted from sample in 4 layers and 160°C annealing temperature.

Observation of surface morphology of PEDOT:PSS layer using atomic force microscopy (AFM) is shown on figure 3. The observation was done on the samples in 3 layers and annealing temperature of 100, 120, 140 and 160 °C. The average roughness of 117.54 nm, 115.35 nm, 96.05 nm, and 80.44 nm were obtained for the annealing temperature of 100, 120, 140 and 160 °C. The loss of solvent content caused reduction in PEDOT:PSS particle size which is suggest as the cause of PEDOT:PSS surface roughness decrease as the annealing temperature increases [8].

3.2. Analysis of monolithic DSSC performance

The performance of a monolithic DSSC can be determined by measuring the I-V curve characteristic of current and voltage measurements. A maximum power (Pmax), a short-circuit current (Isc), and an open-circuit voltage (Voc) can be obtained from the curve. Fill factor (FF), and power conversion efficiency (PCE) can be calculated according to equation (1) and (2):

\[
FF = \frac{V_{\text{max}} I_{\text{max}}}{V_{\text{oc}} I_{\text{sc}}}
\]

\[
PCE = \frac{P_{\text{max}}}{P_{\text{in}}} \times 100\%
\]

where \(V_{\text{max}}\), \(I_{\text{max}}\), \(P_{\text{in}}\) are the maximum voltage, the maximum current, the power received from the incident illumination, which is dependent on the irradiation intensity and the active area of the cell [9].

The electrical characteristic of monolithic DSSC on the variation of number of layers and annealing temperature of PEDOT:PSS counter electrode is presented in Table 1. It can be noted, the highest efficiency of 1.77% is achieved by the sample with 3 layers variation and annealing temperature at 120°C. This result is higher compared to another research which used carbon as the

Figure 3. Atomic force microscopy (AFM) result from PEDOT:PSS with 3 layers and annealing temperatures of (a) 100, (b) 120, (c) 140, and (d) 160°C.
material for counter electrode in monolithic DSSC, 1.52% as their highest efficiency [10]. However, the filling factor (FF) of the monolithic DSSC is still low, probably due to the high series resistance of the cells in this research it still high. Series resistance value gives a huge impact on the filling factor of monolithic DSSC [11]. The high series resistance in this research was probably due to poor contact between the photoactive area and the FTO glass, which was due to the construction of planar cells [7]. To make the better contacts between photoactive areas and FTO glass and minimize the series resistance of monolithic DSSC, a TiCl₄ pre-treatment is required before the TiO₂ layer being deposited on the FTO glass as a blocking layer. The function of blocking layer is to tighten the contact between the TiO₂ photo-anode and FTO glass in order to make the electron transfer process to the external circuit smoothly [12].

Figure 4 shows the influence of number of layers and annealing temperature on the short circuit current (Iₛₑ) and efficiency (PCE) of monolithic DSSC. It is found that the number of layers tends to increase both Iₛₑ and PCE. This is closely related to what has been obtained from figure 2, where it is obtained that the more number of layers causes a decrease in sheet resistivity, which indicates an increase in conductivity. The high conductivity improves Iₛₑ and efficiency as well. Different things occur with the effect of annealing temperature on current and efficiency. It is also shows in figure 4 that in general Iₛₑ and PCE tend to decrease with increasing annealing temperatures. The decreasing in Iₛₑ and PCE may be caused by the decreasing in PEDOT:PSS surface roughness as the annealing temperature increases. The surface roughness of the counter electrode layer can affect the catalytic performance of the counter electrode in the reduction process of where I₃⁻ in the electrolyte the higher the surface roughness of the counter electrode layer can improve better catalytic ability [13,14].

There is an exception such as the number of layers of 3 where Iₛₑ and PCE is inconsistent to decrease. If the data for each number of layer are linear regressed they will show to tend to decrease. However, annealing temperature at 120 °C has a higher Iₛₑ and PCE. The high in Iₛₑ and PCE was obtained due to the high conductivity as mention above. Vitoratos et.al reported that annealing of PEDOT:PSS at 393K (120°C) exhibits a maximum conductivity compared to 423, 438, 443, 448 and 463 K [15].

### Table 1. Electrical characteristic in monolithic DSSC with number of layers and annealing temperature of PEDOT:PSS counter electrode.

| Number of layers | Annealing temperature (°C) | Iₛₑ (mA) | Voc (V) | FF | Rs (Ω) | Pₑₘₐₓ (mW) | Eff (%) |
|------------------|---------------------------|----------|---------|----|--------|-------------|---------|
| 1                | 100                       | 0.89     | 0.65    | 0.27 | 679.87 | 0.16        | 1.28    |
|                  | 120                       | 0.76     | 0.63    | 0.24 | 1085.55| 0.11        | 0.91    |
|                  | 140                       | 0.93     | 0.63    | 0.28 | 579.68 | 0.16        | 1.30    |
|                  | 160                       | 0.64     | 0.59    | 0.25 | 1063.77| 0.09        | 0.74    |
| 2                | 100                       | 0.92     | 0.61    | 0.24 | 857.31 | 0.13        | 1.10    |
|                  | 120                       | 1.15     | 0.61    | 0.26 | 535.58 | 0.18        | 1.42    |
|                  | 140                       | 0.94     | 0.59    | 0.25 | 711.86 | 0.14        | 1.08    |
|                  | 160                       | 0.56     | 0.55    | 0.23 | 1539.12| 0.07        | 0.57    |
| 3                | 100                       | 1.05     | 0.61    | 0.24 | 666.91 | 0.16        | 1.28    |
|                  | 120                       | 1.26     | 0.61    | 0.29 | 419.10 | 0.22        | 1.77    |
|                  | 140                       | 0.65     | 0.51    | 0.24 | 1229.41| 0.08        | 0.62    |
|                  | 160                       | 0.79     | 0.53    | 0.27 | 723.23 | 0.11        | 0.89    |
| 4                | 100                       | 1.21     | 0.59    | 0.25 | 565.65 | 0.18        | 1.43    |
|                  | 120                       | 1.00     | 0.59    | 0.23 | 911.72 | 0.14        | 1.10    |
|                  | 140                       | 0.91     | 0.55    | 0.23 | 894.76 | 0.12        | 0.92    |
|                  | 160                       | 0.92     | 0.53    | 0.34 | 346.99 | 0.17        | 1.33    |
Figure 4. The influence of number of layers on the short circuit current (left) and efficiency of monolithic DSSC (right).

Figure 5. The influence of number of layers (left) and annealing temperature (right) on open circuit voltage of monolithic DSSC.

Figure 5 shows the influence of annealing temperature and number of layers on open circuit voltage of monolithic DSSC. We can see that open circuit voltage tend to decrease with decreasing in number of layers and annealing temperature. However, the decreasing in open circuit voltage is not significant as the decreasing in short circuit current and efficiency. This may be due to the main factors affecting the $V_{OC}$ value is the suitability of the redox potential energy level with the HOMO level of the dye and the energy level of the semiconductor with the LUMO level of the dye as well as the electron recombination occurring in the semiconductor [11]. Therefore, counter electrode layer has no significant effect on the $V_{OC}$ value.

The $V_{OC}$ value of the monolithic DSSC can be determined theoretically from the energy level mechanism. $V_{OC}$ represents dye-absorbed energy reduced by overpotential 1 and 2 (the suitability of redox potential energy levels with HOMO levels of dye and semiconductor energy levels with LUMO levels of dye) [16]. Dye used in this study is dye ruthenium Z907 which has a magnitude of energy at the level of HOMO is 0.93 V and LUMO is -0.65 V, so it requires energy absorbed from sunlight of 1.58 V. Electrolyte used in this study is an EL-HPE electrolyte that reduce $I^- / I^-$ and has an energy level of 0.35 V. The Fermi level of the TiO$_2$ layer is -0.25 V. From these data, the $V_{OC}$ value of monolithic DSSC made in this study can be known that $1.58 \text{ V} - (0.93 \text{ V} - 0.35 \text{ V}) + (-0.25 \text{ V} - (-0.65 \text{ V})) = 1.58 \text{ V} - 0.58 \text{ V} = 0.6 \text{ V}$. Theoretically, it can be seen that the $V_{OC}$ value of the monolithic DSSC produced is 0.6 V. Based on the data obtained from the IV curve measurement, it
was found that the $V_{OC}$ value of the resulting monolithic DSSC was in the range of 0.53 - 0.65 V, which is quite appropriate with theoretical calculation. However, the difference in $V_{OC}$ values generated in this study may be due to PEDOT:PSS is an organic material that can be dissolved in electrolytes and complex formations [17].

4. Conclusions

Fabrication of Monolithic DSSC by using PEDOT:PSS polymer counter electrode has been successfully developed. The more number of PEDOT:PSS layers increasing the resistivity of the counter electrode layer. The more number of PEDOT:PSS layers increasing the resistivity of the counter electrode layer, consequently improves $I_{SC}$ and efficiency. The higher the annealing temperature causing the decreasing of the surface roughness of PEDOT:PSS layer, which results in the decreased of $I_{SC}$ and the efficiency. The best performance of monolithic DSSC with $V_{OC} = 0.61$ V; $I_{SC} = 1.26$ mA, and efficiency = 1.77\% was resulted in 3 layers and-annealing temperature at 120°C.

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