Research on control technology of RS422A differential time-unified signal

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Abstract. RS422A differential signal is a kind of bipolar pulse signal formed by level conversion of TTL signal through RS422A differential transmission device. Using shielded twisted pair transmission, the signal level is determined by the voltage difference between the two twisted pairs at the same time. It has the characteristics of long transmission distance and strong anti-interference ability. The time system signal is a standard RS422 differential signal, which plays an important role in the fire control system. The complex programmable logic device CPLD, the high-precision temperature-compensated crystal oscillator, and the standard RS422A differential transceiver device are used as the control device in this article. The control methods for generating, detecting, sending and receiving, adjusting the pulse width and synchronizing the timing signals are elaborated in detail. This method has the characteristics of simple circuit, high reliability, flexible control, high control accuracy, etc. It is widely used in fire control systems.

1. Introduction
Time signal is widely used as a very important "heartbeat" trigger signal in the fire control system. Under the unified trigger of the time pulse, each sub-system sends and receives data messages within a time period, and is in accordance with the regulations. Data calculation and task processing are carried out at any time, and relevant task data is sent to other extension devices in the system at a specific time to achieve specific control functions. Each packet that each subsystem needs to send or receive at a specific time is received or sent by the other party at a specific time, so it is necessary to unify the time when each sub-system receives or sends data. The system sends a uniform periodic time interval pulse signal to each sub-device (ie: time-integrated signal), each extension the device responds to the time-of-day signal in an interrupted manner and completes the corresponding data sending and receiving operations. Therefore, it requires high precision and high reliability, and strong anti-interference ability.

The control of timing signals in this paper mainly includes the generation of differential pulse timing signals with different periods of 1ms, 10ms and 20ms, automatic detection and reception of differential pulse timing signals with different periods, timing synchronization and timing delay of generating and external timing signals the pulse signal at the time, the pulse width of the control pulse signal (duty cycle) and the accuracy (error) of the control of the pulse signal are analysed, and the standard differential pulse timing signal is sent. The use of complex programmable logic devices CPLD, high-precision temperature-compensated crystal oscillator (clock source) and standard RS422A differential transceiver devices to complete the control of differential timing signals. The
control method has the characteristics of simple circuit, high reliability, flexible control, high control accuracy, etc. It is widely used in time signal detection of fire protection system.

1.1 Monostable IC detection

Monostable IC detection is the use of monostable output IC integrated circuit (74LS123) as the detection controller, by configuring the timing resistor \(R_t\) and timing capacitor \(C_{ext}\) to automatically complete the detection of income time pulse signal, when the input terminal is input for a pulse signal, the edge trigger (rising edge trigger) mechanism is used to pull the rising edge high for a certain period of time under the combined action of the timing resistor and the capacitor. The output terminal outputs a positive pulse synchronized with the rising edge of the input signal, the pulse width \(t_w\) is the duration of the high level, and the pulse width can be changed by setting different timing resistance and timing capacitance. When the input is detected, the pulse signal period (detection period) is less than the set pulse width, the controller can output a continuously stable high level "1", if the input detection pulse is interrupted, the output terminal will delay a certain time and output low level "0", so as to realize the detection of external time synchronization pulse signal.

According to the working principle of the monostable IC controller, for ease of calculation, when the timing capacitor \(C_{ext} > 1000\) pf, the size of the timing resistance can be based on the following

\[
t_w = 0.45 R_t C_{ext} \tag{1}
\]

\[
R_t = \frac{t_w}{0.45 C_{ext}} \tag{2}
\]

In order to improve the reliability of detection, generally, \(t_w\) takes 1.5 external time periods \(T\), and when the external time pulse periods \(T\) are 20ms, 10ms, and 1ms, and \(C_{ext} = 22\) μF, then the formula (2) gives:

\[
R_{t1} = \frac{t_w}{0.45 C_{ext}} = 1.5 \times 0.02 / (0.45 \times 0.000022) = 3k \Omega \tag{3}
\]

\[
R_{t2} = \frac{t_w}{0.45 C_{ext}} = 1.5 \times 0.02 / (0.45 \times 0.000022) = 1.5k \Omega \tag{4}
\]

\[
R_{t3} = \frac{t_w}{0.45 C_{ext}} = 1.5 \times 0.02 / (0.45 \times 0.000022) = 0.15k \Omega \tag{5}
\]

Among them, \(R_{t1}, R_{t2}, R_{t3}\) are the timing resistance when the detection period is respectively 20ms, 10ms, 1m. The detection principle is shown in Figure 1.

![Figure 1. Schematic diagram of monostable IC detection.](image)

1.2 CPLD logic detection

Using programmable logic device (CPLD), high-precision crystal oscillator (clock source), through logic programming to detect the external time pulse signal, programming in CPLD to achieve 2 binary counters (Counter1 and Counter2) and 2 D trigger (Dff1, Dff2), use Counter1 counter, clock source and Dff1 trigger to set the width of the external clock pulse to 2 clock cycles, the pulse output from the Dff1 trigger is the synchronization pulse, and the synchronization pulse is used as the Counter2 counter. Set the control signal to let the counter start counting. The signal output from the Counter2 calculator is inverted by the inverter and used as the "clear" control signal of the Dff2 trigger. Set the counting time of the Dff2 calculator to be greater than 1 external clock cycle When there is an external clock signal input, the Dff2 trigger will output a high level "1", otherwise it outputs a low level "0", so as to realize the detection of the external clock signal.

If the period \(T\) of the external time pulse signal is 20ms, the clock source frequency is 10MHz, and the counting time of the Counter2 calculator is set to 30ms, the logical detection of the external time pulse signal can be realized. The detection principle is shown in Figure 2.
1.3 Detection accuracy and error

The monostable IC controller is used to detect the detection error of the external time system, which is mainly determined by the resistance $R_t$ and the capacitor $C_{ext}$. In order to reduce the detection error and improve the accuracy, the theoretical value of the resistance and capacitance is calculated according to the period of the external time system. Choose the appropriate resistor and capacitor according to the theoretical value. Because there is a certain capacitance error in the resistor and capacitor itself, and it is very difficult to find the resistor and capacitor that are exactly the same as the theoretical value, it is difficult to ensure that the pulse width of the monostable output is the same as the theoretical value. If the pulse width is much larger than the detection period, it will cause an increase in detection error. In general, the pulse width is about 1.1 to 1.3 times the detection period. Therefore, the detection accuracy of this method can generally only reach the millisecond level.

Using CPLD for combinational logic programming to detect the detection error of the external time system is only related to the frequency of the clock source. The larger the clock frequency and the smaller the period, the smaller the detection error. The theoretical maximum detection accuracy can be controlled within 1 clock cycle in fact, it takes 1 clock cycle to detect the rising edge of the external clock, the counter set and the carry output require 1 clock cycle, and the detection error can be controlled within 2 clock cycles. The detection accuracy of this method can be controlled in nanoseconds level.

The two methods of monostable IC hardware and CPLD combination logic need to determine the external time period of detection in advance. The former is realized by configuring resistors and capacitors of different sizes, the latter is realized by CPLD logic programming, and the detection accuracy is higher than the former. It is flexible to program the external time system for detecting different cycles, easy to change logic, and is widely used in the system.

2. Time signal reception

Differential timing signals are generally differential pulse signals that conform to the RS422A differential characteristics. A set of differential pulses is transmitted using a set of shielded twisted-pair wires. Each set of shielded twisted-pair wires is shielded and isolated by a shielding layer. The reception of differential signals is obtained by obtaining the same moment the voltage difference between the two twisted pairs determines the signal. If the voltage difference is a positive voltage, the output is high, otherwise it is low, so the differential signal has the characteristics of long transmission distance and strong anti-interference ability. The receiving of differential signals is generally accomplished by using a dedicated controller that conforms to the standard RS422A differential characteristics (such as the DS26LS33 from Texas Instruments). During the transmission of differential signals, it is easy to produce differential mode interference and common mode between the positive and negative signals. Interference and interference signals such as noise reflection caused by long-distance cables, in order to eliminate differential mode interference, it is necessary to connect a terminal load matching resistor ($R_t$) in series between the positive and negative poles of the receiving controller. The resistance of the terminal resistance is approximately equal to the total impedance of...
the transmission cable, under normal circumstances, Rt is preferably 100Ω ~ 120Ω, while the load resistance can also output the current of the transmitter into a voltage signal. In order to improve the anti-interference ability and reliability of the circuit and reduce the influence of the interference signal on the received signal, it is necessary to configure a pull-up bias resistor (R1) and a pull-down bias resistor (R2) on the positive and negative poles of the receiving controller respectively. In this case, the pull-up and pull-down bias resistance should be about 2.2KΩ. In order to eliminate the common mode interference formed on the long-distance cable and avoid the impact or destruction of the current surge formed during the high-speed signal transmission on the chip, it is necessary to add a TVS transient surge on the positive and negative signals at the receiving end of the chip, respectively. Suppression diodes (V1, V2), the principle of receiving differential signals is shown in Figure 3.

![Figure 3. Schematic diagram of differential pulse timing system signal reception.](image)

3. Time signal generation

The principle of counting frequency division is used to realize the generation of unified pulse signals at different cycles. The principle is to use a binary counter to divide the high-precision clock crystal oscillator, set different count values for the counter, and use the counter carry principle to generate different periods Carry pulse, the count value is calculated as follows

\[ \frac{1}{f} \cdot n = t \]  

(6)

From (6), we can get

\[ n = f \cdot t \]  

(7)

Where \( t \) is the counting period, \( n \) is the counter count value, and \( f \) is the clock frequency. In general, the clock frequency \( f = 10MHz \). If a 20ms pulse signal needs to be generated (ie: \( t = 20ms \)), then according to formula (7)

\[ n = f \cdot t = 10000000 \times 0.01 = 100000 \]

When \( n = 100000 \) is converted into hexadecimal as "186A0", five 16-bit binary counters can be cascaded. The counting logic diagram is shown in Figure 4.

![Figure 4. Control logic with a generation period of 10ms.](image)
In the same way, the count value \( n \) that generates a 1ms period pulse is "10000", which is converted into hexadecimal to "2710", which can be achieved after cascading four 16-bit binary counters, and the count value \( n \) that generates a 20ms period pulse is "200000" can be converted into "30D40" in hexadecimal, and it can be realized by cascading five 16-bit binary counters. The control logic is the same as Figure 4.

4. Time signal control

4.1 Pulse duty ratio setting of time signal

The duty cycle of the pulse signal (i.e., pulse width) is the ratio of the high-level duration and the low-level duration of the pulse in a pulse period. The larger the ratio, the wider the pulse width. In general, the duty cycle of the pulse signal is less than 1, and the duty cycle of the square wave signal is 1. The processing of the pulse signal by the computer system is generally interrupted by the pulse rising edge trigger (edge trigger), and some computer systems use the signal High level trigger interrupt method, this method requires a high level for a long time, that is, the duty cycle is not less than 1, therefore, I adapt to different computer systems, I need to adjust and control the duty cycle of the timing signal. Using the edge trigger of the D flip-flop and the counter frequency division principle of the counter, combined with a high-precision clock, the duty cycle of the pulse signal can be adjusted, and different pulse widths can be achieved by setting different counter values of the counter. The control principle is to input the pulse signal to the trigger end of the D flip-flop, connect the output end of the D flip-flop to the counting time end of the counter, let the counter begin to work, and let the output end of the counter pass the "NOT" to reverse as "clear" signal is connected to the clear end of the D flip-flop, so that the output of the flip-flop is low, and the counter stops working. In this way, the signal output by the D flip-flop is a pulse signal with the same period and different pulse widths, and its timing is completely synchronized with the original pulse signal, but the pulse width changes. The schematic diagram is shown in Figure 5, and the waveform simulation is shown in Figure 6.

![Figure 5. Schematic diagram of pulse duty cycle control.](image)

![Figure 6. Simulation waveform of pulse width adjustment.](image)

4.2 Timing synchronization control of timing signal

In order to carry out data communication with the superior large system, the time signal period of the two systems is not the same. Generally, the time period of the large system is longer, the time period of the system is shorter, and the time of the two systems is the same. The starting time is also different. Therefore, in order to realize the unification of the starting time of the two systems, it is necessary to fully synchronize the timing of the system and the large system, using the clock source, D flip-flop and 2 binary counters (Counter1, Counter2) Complete the timing synchronization of the external time system. The method is to use the clock source and Counter1 counter to adjust the pulse width of the external time system pulse signal to 2 times the clock source period, and get a synchronous count.
pulse from the Dff trigger output. Signal, the timing and period of the pulse signal and the original external pulse signal are exactly the same, but the pulse width is different. The synchronous count pulse is reversed by the "not gate" as the "Ldn" set signal of the Counter2 counter, and the count is set after the counter is set, so that the new pulse signal generated after the counter works is the synchronous pulse signal. The timing is completely synchronized with the original pulse signal. By setting the counter value of the Counter2 counter, different synchronization cycles are achieved, and then the synchronization pulse signal and the external time signal are logically ORed to obtain the final synchronization pulse signal. The external time pulse is the same. If the period of the external time system (ST) is 200us and the synchronization period of the Counter2 counter is 20us, then 10 synchronization pulses will be generated in one external time system cycle. The principle of timing synchronization is shown in Figure 7.

![Figure 7. Schematic diagram of timing synchronization.](image)

4.3 Time-delay control of timing signals

In the system application, it is necessary to delay the received external time signal within the system by a certain time interval in time sequence, to generate an internal time system signal delayed by a certain time interval from the external time sequence, as a system trigger pulse Send a specific data message, using the clock source, D flip-flop, and binary counter to complete the time delay of the external time system. The implementation method is to use the D flip-flop to convert the rising edge of the external time system to a high level "1". As the enable signal of the delay counter, under the drive of the clock source, the delay computer starts to count periodically, and the pulse output by the counter is reversed by the "NOT gate" as the "clear" signal of the D flip-flop, allowing the trigger the output signal of the converter is low level "0", thus stopping the delay counter counting. In this way, the pulse signal output from the counter is a timing delay signal. By setting the count value of the delay counter, different delay time intervals are realized. The principle of timing delay is shown in Figure 8:

![Figure 8. Schematic diagram of timing delay.](image)

If the period of the external time system ST is 200us, the local clock source CLK is 10MHz, the pulse signal after the external time system delay 100us is YCST, and the 20us pulse signal synchronized with the external time system ST pulse timing is TBST, simulation the waveform is shown in Figure 9:

![Figure 9. Timing synchronization and timing delay simulation waveforms.](image)
4.4 Control accuracy and error

Logic programming of CPLD to achieve logic control such as timing synchronization pulse signal, timing delay pulse signal, pulse width control, etc. When the counter receives the external enable signal of the rising edge, if the rising edge of the clock source comes at the same time, the counter starts to work, otherwise, the counter will only work when the rising edge of the clock source arrives. In fact, the rising edge of the clock cannot come at the same time as the rising edge of the external time, which has a time interval error, this error is not greater than 1 clock cycle. In the timing synchronization control, a timing pulse is generated using the rising edge of the external time synchronization, as the counter's "set" control signal, the counter uses the count pulse width to "set", if the calculated pulse width is larger, the longer the counting time, the longer the timing delay will increase the control error. Conversely, if the count pulse width is smaller, the count error will be smaller. The minimum count pulse width is 2 clock cycles to ensure the reliable operation of the counter. Therefore, in CPLD combinational logic control, the minimum error is 2 clock cycles. The larger the clock frequency and the smaller the cycle, the smaller the control error. The larger the clock frequency will increase the CPLD's logic programming unit, so in general, it is more appropriate to use a clock of 10MHz, and the maximum control error is 200ns, which fully meets the system requirements.

5. Time signal transmission

In the fire control system, the intervals between the sub-systems are relatively far away. In order to reduce the interference of the transmission line and ensure the reliable transmission of the signal, the RS422A differential transmission controller (such as: DS26LS31) is used to convert the time system signal into a differential pulse signal, and then use Double comparison transmission cables are used for long-line transmission. In order to improve the anti-interference ability and reliability of the circuit and reduce the signal interference caused by long-distance transmission, TVS transients must be configured on the "+" and "-" poles of the differential controller output. Suppress the diode and connect at least one 0.01uF ~ 0.1uF high-frequency capacitor in parallel between the power supply of the differential controller and the ground to reduce the influence of the power supply on the IC. The transmission principle is shown in Figure 10.

![Figure 10. Schematic diagram of differential transmission of timing signals.](image)

6. Conclusion

RS422 differential timing system signal is widely used as an important "heartbeat" pulse signal fire control system. It uses the online programming technology of programmable logic device CPLD. By modifying the control program online, it can flexibly implement logic control functions such as external time system detection, pulse width adjustment, multi-channel distribution, and timing delay for different periods. It has the characteristics of strong anti-interference ability and high reliability. It can meet the requirements of different systems for timing signals and has strong practicality.

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