Automating Deductive Verification for Weak-Memory Programs

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Abstract. Writing correct programs for weak memory models such as the C11 memory model is challenging because of the weak consistency guarantees these models provide. The first program logics for the verification of such programs have recently been proposed, but their usage has been limited thus far to manual proofs. Automating proofs in these logics via first-order solvers is non-trivial, due to reasoning features such as higher-order assertions, modalities and rich permission resources.

In this paper, we provide the first implementation of a weak memory program logic using existing deductive verification tools. We tackle three recent program logics: Relaxed Separation Logic and two forms of Fenced Separation Logic, and show how these can be encoded using the Viper verification infrastructure. Many ingredients of our encoding are not specific to the particular logics tackled, and we explain the general techniques applied. We evaluate the encoding on examples from existing papers and on code from an open-source library.

1 Introduction

Reasoning about programs running on weak memory is challenging because weak memory models admit executions that are not sequentially consistent, that is, cannot be explained by a sequential interleaving of concurrent threads. Moreover, weak-memory programs employ a range of operations to access memory, which require dedicated reasoning techniques. These operations include fences as well as read and write accesses with varying degrees of synchronisation.

Some of these challenges are addressed by the first program logics for weak-memory programs, in particular, Relaxed Separation Logic (RSL) [28], GPS [26], Fenced Separation Logic (FSL) [13], and FSL++ [12]. These logics apply to interesting classes of C11 programs, but their tool support has been limited to embeddings in Coq. Verification based on these embeddings requires substantial user interaction, which is an obstacle to applying and evaluating these logics.

In this paper, we present a novel approach to automating deductive verification for weak memory programs. We encode large fractions of RSL, FSL, and FSL++ into the intermediate verification language Viper [19], and use the existing Viper verification backends to reason automatically about the encoded programs. This encoding reduces all concurrency and weak-memory features as well as logical
features such as higher-order assertions and custom modalities to a much simpler sequential permission logic.

Our approach is much more lightweight than developing a dedicated verifier for any given weak-memory logic because it utilises Viper's existing verification backends based on symbolic execution or verification condition generation. On the other hand, our approach achieves a higher degree of automation than Coq, without requiring tactics that are specific to a particular logic. Saving the effort to develop dedicated backends or tactics is especially useful for prototyping and evaluating logics.

The contributions of this paper are: (1) The first automated verification approach for weak-memory logics. We demonstrate the effectiveness of this approach on examples from the literature, which are available online [3]. (2) An encoding of large fractions of RSL, FSL, and FSL++ into Viper. Various aspects of this encoding (such as the treatment of higher-order features and modalities, as well as the overall proof search strategy) are generic and can be reused to encode other advanced separation logics. In the following, we will refer to RSL, FSL, and FSL++ collectively as the RSL logics.

Related Work. The existing weak-memory logics RSL [28], GPS [26], FSL [13], and FSL++ [12] have been formalized in Coq and used to verify small examples. The proofs were constructed mostly manually, whereas our approach automates most of the proof steps. The degree of automation in Coq could be increased through logic-specific tactics [24,8], whereas our approach benefits from Viper’s automation for the intermediate language, which is independent of the encoded logic. On the other hand, the Coq formalizations are foundational whereas the soundness of our verification results depends on the correctness of the Viper tool. While foundational proofs are important for critical applications, a more lightweight approach is useful especially to gain experience with new logics.

Jacobs [15] proposed a program logic for the TSO memory model that has been encoded in VeriFast. However, verification in this encoding requires a substantial amount of annotations, whereas our approach provides a higher degree of automation and handles the more complex C11 memory model. Caper [11] is a verifier targeting programs with fine-grained concurrency; the implemented proof technique does not, however, tackle weak memory reasoning.

Automating logics by an encoding into intermediate verification languages has proven useful for sequential programs, as witnessed by the many existing verifiers (e.g. [17,16,10,19]) which target Boogie [4] or Why3 [5]. Our work is the first that applies this approach to logics for weak-memory concurrency.

Outline. The next four sections present the encoding for the core features of the C11 memory model: we discuss non-atomic locations in Sec. 2, release-acquire accesses in Sec. 3, fences in Sec. 4, and compare and swap in Sec. 5. We introduce the necessary background on Viper along the way. We discuss additional features in Sec. 6 and evaluate our approach in Sec. 7. Sec. 8 concludes. The appendix
\[ s ::= l := \text{alloc}_n() \mid l := \text{alloc}_\rho(Q) \mid [l]_\rho := e \mid x := [l]_\rho \]
\[ | \text{fence}_{\text{acq}} \mid \text{fence}_{\text{rel}}(A) \mid x := \text{CAS}_\tau(l, e_1, e_2) \]
where \( \rho \in \{\text{acq}, \text{RMW}\} \), \( \sigma ::= \text{na} \mid \tau \), \( \tau \in \{\text{acq}, \text{rel}, \text{rel}_{\text{acq}}, \text{rlx}\} \)

Fig. 1. Syntax for memory accesses. \( \text{na} \) indicates a non-atomic operation; \( \tau \) indicates an atomic access mode (as defined in C11), discussed in later sections. \( \rho \), and assertions \( A \) and invariants \( Q \) are program annotations, needed as input for our encoding. Expressions \( e \) include boolean and arithmetic operations, but no heap accesses. We assume that source programs are type-checked.

\[ A ::= e \mid l \leftrightarrow e \mid A_1 * A_2 \mid e \Rightarrow A \mid (e ? A_1 : A_2) \]
\[ | \text{Uninit}(l) \mid \text{Acq}(l, Q) \mid \text{Rel}(l, Q) \mid \text{Init}(l) \mid \triangle A \mid \nabla A \mid \text{RMWAcq}(l, Q) \]

Fig. 2. Assertion syntax of the RSL logics. The top row of constructs are standard for separation logics; those in the second row are specific to the RSL logics, and explained throughout the paper. Invariants \( Q \) are functions from values to assertions (cf. Sec. 3). We replace RSL’s \( \text{emp} \) assertion by \( \text{true} \); see Sec. 6.

contains further details on the encoding and our examples. The Viper code for all examples is available online [3].

2 Non-atomic Locations

We present our encoding for a small imperative programming language that reflects the core operations relevant for C-like programs using C11 atomics, and is similar to the languages supported by the RSL logics. C11 supports non-atomic memory accesses and different forms of atomic accesses. The access operations are summarised in Fig. 1. We adopt the common simplifying assumption \([28, 26]\) that memory locations are partitioned into those accessed only via non-atomic accesses (non-atomic locations), and those accessed only via C11 atomics (atomic locations). Read and write statements are parameterised by a mode \( \sigma \), which is either \( \text{na} \) (non-atomic) or one of the atomic access modes \( \tau \). We focus on non-atomic accesses in this section and discuss atomics in subsequent sections.

RSL proof rules. Non-atomic memory accesses come with no synchronisation guarantees; programmers are obliged to ensure that all accesses to non-atomic locations are data-race free. The RSL logics enforce this requirement using standard separation logic \([20, 23]\). We show the syntax of assertions in Fig. 2 which will be explained throughout the paper. A points-to assertion \( l \leftrightarrow e \) denotes a transferrable resource, providing permission to access the location \( l \), and expressing that the location has been initialised and its current value is the

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1 C11 provides further “consume” and “sequentially consistent” access modes. The former is not supported by the RSL logics, while the latter has the same proof rules as for the rel.acq mode; both are omitted here, for brevity.
Fig. 3. Adapted RSL rules for non-atomics. Read access requires a non-zero permission. Write access requires either write permission or that the location is uninitialised. The underscore _ stands for an arbitrary value.

value of expression e. Here, k is a fraction 0 < k ≤ 1; k = 1 denotes the full (or exclusive) permission to read and write location l, whereas 0 < k < 1 provides (non-exclusive) read access [7]. Points-to resources can be split and recombed, but never duplicated or forged; when transferring such a resource to another thread it is removed from the current one, avoiding data races by construction. The RSL assertion Uninit(l) expresses exclusive access to a location l that has been allocated, but not yet initialised; l may be written to but not read from (in C11 this would be undefined behaviour). The main proof rules for non-atomic locations, adapted from RSL [28], are shown in Fig. 3.

**Encoding.** The Viper intermediate verification language [19], which we use to encode the RSL logics, supports an assertion language based on Implicit Dynamic Frames [25], a program logic related to separation logic [21], but which separates permissions from value information. Viper is object-based; the only memory locations are field locations e.f (in which e is a reference, and f a field name). Permissions to access these heap locations are described by accessibility predicates of the form acc(e. f, k), where k is a fraction as for points-to predicates above (k defaults to 1). Assertions that do not contain accessibility predicates are called pure. Unlike in separation logics, heap locations may be read in pure assertions.

We model C-like memory locations l using a field val of a Viper reference l. Consequently, a separation logic assertion l \rightarrow e is represented in Viper as acc(l.val, k) \& \& l.val == e. In this paper, we assume that memory locations have type int, but a generalisation is trivial. Viper’s conjunction \&\& treats permissions multiplicatively, requiring the sum of the permissions in each conjunct, and acts as logical conjunction for pure assertions (just as * in separation logic).

Viper provides two key statements for encoding proof rules. An inhale statement inhale A has the effect of adding the permissions denoted by the Viper assertion A to the current state, and assuming pure assertions in A. This can be used to model gaining new resources, e.g., acquiring a lock in the source program. Dually, exhale A checks that the current state satisfies A (otherwise a verification error occurs), and removes the permissions that A denotes; the values of any locations to which no permission remains are havoced (assigned arbitrary values). For example, when forking a new thread, its precondition is exhaled to reflect transferring ownership of the necessary resources from the forking thread. Inhale
Fig. 4. Viper encoding of the RSL assertions and rules for non-atomic memory accesses.

and exhale statements can be seen as the permission-aware analogues of the assume and assert statements of first-order verification languages [17].

The encoding of the rules for non-atomics from Fig. 3 is presented in Fig. 4. \(\llbracket A \rrbracket \rightsquigarrow \ldots\) denotes the encoding of an RSL assertion \(A\) as a Viper assertion, and analogously \(\llbracket s \rrbracket \rightsquigarrow \ldots\) for source-level statements \(s\).

The first two lines show background declarations employed in our encoding. The assertion encodings follow the explanations above. Allocation is modelled by obtaining a fresh reference (via \texttt{new()} and inhaling permissions to its \texttt{val} and \texttt{init} fields; Assuming \texttt{!l.init} reflects that the location is not yet initialised. Viper implicitly checks the necessary permissions for field accesses (verification fails otherwise). Hence, the translation of a non-atomic reads only needs to check that the read location is initialised before obtaining its value. Analogously, because of Viper’s implicit permission check, the translation of a non-atomic write only stores the value and records that the location is now initialised.

Note that Viper’s implicit permission checks are both necessary and sufficient to encode the RSL rules in Fig. 3. In particular, the assertions \(l \mapsto \_\) and \(\text{Uninit}(l)\) both provide the permissions to write to location \(l\). By including \(\text{acc}(l, \text{val})\) in the encoding of both assertions, we avoid the disjunction of the RSL rule.

Our approach requires programmers to annotate their code with access modes for locations (as part of the \texttt{alloc} statement), and specifications such as pre and postconditions for methods and threads. Given these inputs, Viper constructs the proof automatically. In particular, it automatically proves entailments, and splits and combines fractional permissions (hence, the equivalence in Fig. 3 need not be encoded). Automation can be increased further by inferring some of the required assertions, but this is orthogonal to the encoding presented in this paper.

3 Release-Acquire Atomics

The simplest form of C11 atomic memory accesses are \texttt{release write} and \texttt{acquire read} operations. They can be used to synchronise the transfer of ownership of

\footnote{In fact, Viper does not support disjunction over impure assertions. This does not restrict expressiveness in practice, since disjunctions used in RSL specifications typically include a pure condition which disambiguates the cases such that they can be encoded using implications and conditional expressions.}
(and information about) other, non-atomic locations, using a message passing idiom, illustrated by the example in Fig. 5. This program allocates two non-atomic locations \( a \) and \( b \), and an atomic location \( l \) (initialised to 0), which is used to synchronise the three threads that are spawned afterwards. The middle thread makes changes to the non-atomics \( a \) and \( b \), and then signals completion via a release write of 1 to \( l \); conceptually, it gives up ownership of the non-atomic locations via this signal. The other threads loop attempting to acquire read a non-zero value from \( l \). Once they do, they each gain ownership of one non-atomic location via the acquire read of 1 and access that location. The release write and acquire reads of value 1 enforce ordering constraints on the non-atomic accesses, preventing the left and right threads from racing with the middle one.

RSL proof rules. The RSL logics capture message-passing idioms by associating a location invariant \( Q \) with each atomic location. Such an invariant is a function from values to assertions; we represent such functions as assertions with a distinguished variable symbol \( V \) as parameter. Location invariants prescribe the intended ownership that a thread obtains when performing an acquire read of value \( V \) from the location, and that must correspondingly be given up by a thread performing a release write. The main proof rules \[28\] are shown in Fig. 6.

When allocating an atomic location for release/acquire accesses (first proof rule), a location invariant \( Q \) must be chosen (as an annotation on the allocation). The assertions Rel\((l, Q)\) and Acq\((l, Q)\) record the invariant to be used with subsequent release writes and acquire reads. To perform a release write of value \( e \) (second rule), a thread must hold the Rel\((l, Q)\) assertion and give up the assertion \( Q[e/V] \). For example, the line \( [l]_{\text{rel}} := 1 \) in Fig. 5 causes the middle thread to give up ownership of both non-atomic locations \( a \) and \( b \). The assertion Init\((l)\) represents that atomic location \( l \) is initialised; both Init\((l)\) and Rel\((l, Q)\) are duplicable assertions; once obtained, they can be passed to multiple threads.

Multiple acquire reads might read the value written by a single release write operation; RSL prevents ownership of the transferred resources from being obtained (unsoundly) by multiple readers in two ways. First, Acq\((l, Q)\) assertions
cannot be duplicated, only split by partitioning the invariant \( Q \) into disjoint parts. For example, in Fig. 5, \( \text{Acq}(l, Q_1) \) is given to the left thread, and \( \text{Acq}(l, Q_2) \) to the right. Second, the rule for acquire reads adjusts the invariant in the \( \text{Acq} \) assertion such that subsequent reads of the same value will not obtain any ownership.

Encoding. A key challenge for encoding the above proof rules is that \( \text{Rel} \) and \( \text{Acq} \) are parameterised by the invariant \( Q \); higher-order assertions are not directly supported in Viper. However, for a given program, only finitely many such parameterisations will be required, which allows us to apply defunctionalisation [22], as follows. Given an annotated program, we assign a unique index to each syntactically-occurring invariant \( Q \) (in particular, in allocation statements, and as parameters to \( \text{Rel} \) and \( \text{Acq} \) assertions in specifications). Furthermore, we assign unique indices to all immediate conjuncts of these invariants. For the program in Fig. 5, we assign indices \( 1 \), \( 2 \) and \( 3 \) to invariants \( Q_1 \), \( Q_2 \) and \( Q_1 \ast Q_2 \), respectively. We write \( \text{indices} \) for the set of indices used. For each \( i \) in \( \text{indices} \), we write \( \text{inv}(i) \) for the invariant which \( i \) indexes. For an invariant \( Q \) from the source program, we write \( \langle Q \rangle \) for its index, and \( \langle\langle Q \rangle\rangle \) for the set of indices assigned to its immediate conjuncts. In our example, \( \langle Q_1 \ast Q_2 \rangle \) is \( 3 \), while \( \langle\langle Q_1 \ast Q_2 \rangle\rangle \) is \( \{1, 2\} \).

Our encoding of the RSL rules from Fig. 6 is summarised in Fig. 7. To encode duplicable assertions such as \( \text{Init}(l) \), we make use of Viper’s wildcard permissions [19], which represent unknown positive permission amounts. When exhaled, these amounts are angelically chosen [14]: provided some positive permission is held, the amount exhaled will always be strictly smaller. So after inhaling an \( \text{Init}(l) \) assertion (that is, a wildcard permission), it is possible to exhale two wildcard permissions, corresponding to two \( \text{Init}(l) \) assertions. Note that for atomic locations, we only use the \( \text{init} \) field’s permissions, not its value.

We represent a \( \text{Rel}(l, \_\_) \) assertion for some invariant via a \textit{wildcard} permission to a \textit{rel} field; this is represented via the \texttt{SomeRel(l)} macro\footnote{Viper macros can be defined for assertions or statements, and are syntactically expanded (and their arguments substituted) on use.}, and is used as the precondition for a release write (we must hold some \textit{Rel} assertion, according to Fig. 6). The specific invariant associated with the location \( l \) is represented by

\[
\vdash \{\text{true}\} l := \text{alloc}(Q) \{\text{Rel}(l, Q) \ast \text{Acq}(l, Q)\}
\]
\[
\vdash \{Q(e) \ast \text{Rel}(l, Q)\} [l]_{\text{rel}} := e \{\text{Init}(l) \ast \text{Rel}(l, Q)\}
\]
\[
\vdash \{\text{Init}(l) \ast \text{Acq}(l, Q)\} x := [l]_{\text{acq}} \{Q[x/\forall] \ast \text{Acq}(l, \forall x \Rightarrow Q)\}
\]
\[
\text{Init}(l) \iff \text{Init}(l) \ast \text{Init}(l) \quad \text{Rel}(l, Q) \iff \text{Rel}(l, Q) \ast \text{Rel}(l, Q)
\]
\[
\text{Acq}(l, Q_1 \ast Q_2) \iff \text{Acq}(l, Q_1) \ast \text{Acq}(l, Q_2) \quad Q_1 \models Q_2 \Rightarrow \text{Acq}(l, Q_1) \models \text{Acq}(l, Q_2)
\]

Fig. 6. Adapted RSL rules for release-acquire atomics.
storing its index as the value of the rel field; when encoding a release write, we branch on this value to exhale the appropriate assertion.\footnote{The RSL logics provide rules for rewriting and splitting the invariants of Rel assertions; these can be used to make the invariant stronger than necessary, which is not useful in practice \cite{27}, and thus not considered here.}

Analogously to Rel, we represent an Acq assertion for some invariant using a \texttt{wildcard} permission (the \texttt{SomeAcq} macro), which is the precondition for executing an acquire read. However, to support splitting, we represent the invariant in a more fine-grained way, by recording individual conjuncts separately. Each conjunct \texttt{i} of the invariant is modelled as an abstract predicate instance \texttt{AcqConjunct(l, i)}, which can be inhaled and exhaled individually, just like individual field permissions. This encoding handles the common case that invariants are split along top-level conjuncts, as in Fig. 5. More complex splits can be supported through additional annotations, see App. C.

\begin{figure}[h]
\centering
\begin{verbatim}
field rel: Int
field acq: Bool
predicate AcqConjunct(l: Ref, idx: Int)

function valsRead(l: Ref, i: Int): Set[Int]
    requires AcqConjunct(l, i)

define SomeRel(l)  acc(l.rel, wildcard)
define SomeAcq(l)  acc(l.acq, wildcard) && l.acq == true

\text{\texttt{Init(l)}} \leadsto \texttt{acc(l.init, wildcard)}
\text{\texttt{Rel(l, Q)}} \leadsto \texttt{SomeRel(l) \&\& l.rel == \langle Q \rangle}
\text{\texttt{Acq(l, Q)}} \leadsto \texttt{SomeAcq(l) \&\& (foreach i in \langle Q \rangle: AcqConjunct(l, i) \&\& \texttt{valsRead(l, i) == Set[Int]()})}\\
\text{\texttt{l := alloc}_{acq}(Q)} \leadsto \texttt{l := new(); inhale \langle Rel(l, Q) \rangle \&\& \langle Acq(l, Q) \rangle}
\text{\texttt{[l].rel := e}} \leadsto \texttt{assert SomeRel(l);}\\
\text{\texttt{foreach i in indices do}}
\text{\texttt{if (i == l.rel) \{ exhale inv(i)[e/V] \}}}
\text{\texttt{end}}
\text{\texttt{inhale Init(l)}}\\
\text{\texttt{x := [l].acq}} \leadsto \texttt{assert Init(l) \&\& SomeAcq(l); x := havoc(); // unknown Int}
\text{\texttt{foreach i in indices do}}
\text{\texttt{if (perm(AcqConjunct(l, i)) == 1 \&\& !(x in valsRead(l, i))) \{}}
\text{\texttt{inhale inv(i)[x/V]}}
\text{\texttt{tmpSet := valsRead(l, i)}}
\text{\texttt{exhale AcqConjunct(l, i)}}
\text{\texttt{inhale AcqConjunct(l, i) \&\& valsRead(l,i) == tmpSet union Set(x)}}\\
\text{\texttt{end}}
\end{verbatim}
\caption{Viper encoding of the RSL rules for release-acquire atomics. The operations in italics (in particular, the \texttt{foreach...end} repetitions) are expanded statically in our encoding (into conjunctions or statement sequences). The (here, always \texttt{true}) value of the acq field will be explained in Sec. 5.}
\end{figure}
A release write is encoded by checking that some \texttt{Rel} assertion is held, and then exhaling the associated invariant for the value written. Moreover, it records that the location is initialised. The RSL rule for acquire reads adjusts the \texttt{Acq} invariant by obliterating the assertion for the value read. Instead of directly representing the adjusted invariant (which would complicate our numbering scheme), we track the set of values read as state in our encoding. We complement each \texttt{AcqConjunct} predicate instance with an (uninterpreted) Viper function \texttt{valsRead}(\textit{l, i}) depending on it, returning a set of indices\footnote{Viper’s heap-dependent functions are mathematical functions of their parameters and the resources stated in their preconditions (here, \texttt{AcqConjunct}(\textit{l, i})).}

A require read checks that the location is initialised and that we have some \texttt{Acq} assertion for the location. It assigns an unknown value to the lhs variable \(x\), which is subsequently constrained by the invariant associated with the \texttt{Acq} assertion as follows: We check for each index whether we both currently hold an \texttt{AcqConjunct} predicate for that index\footnote{A \texttt{perm} expression yields the permission fraction held for a field or predicate instance.} and if so, have not previously read the value \(x\) from that conjunct of our invariant. If these checks succeed, we inhale the indexed invariant for \(x\), and then include \(x\) in the values read.

The encoding presented so far allows us to automatically verify annotated C11 programs using release writes and acquire reads (e.g., the program of Fig. 5) without any custom proof strategies \cite{3}. In particular, we can support the higher-order \texttt{Acq} and \texttt{Rel} assertions through defunctionalisation and enable the splitting of invariants through a suitable representation.

4 Relaxed Memory Accesses and Fences

In contrast to release-acquire accesses, C11’s \textit{relaxed} atomic accesses provide no synchronisation. Consequently, RSL’s proof rules for relaxed atomics provide weak guarantees, in particular, do not support ownership transfer.

Memory fence instructions can eliminate this problem. Intuitively, a \textit{release fence} together with a subsequent relaxed write allows a thread to transfer away ownership of resources, similar to a release write (provided that the transferred resources are not accessed between the fence and the relaxed write). Dually, an \textit{acquire fence} together with a prior relaxed read allows a thread to obtain ownership of resources, similar to an acquire read (again, provided that the transferred resources are not accessed between the relaxed read and the fence); this reasoning is justified by the ordering guarantees of the C11 model \cite{13}.

**FSL proof rules.** FSL and FSL++ provide proof rules for fences (see Fig. 8). They use \textit{modalities} \(\uparrow\) (“up”) and \(\downarrow\) (“down”) to represent resources that are transferred through relaxed accesses and fences. An assertion \(\uparrow A\) represents a resource \(A\) which has been prepared, via a release fence, to be transferred by a relaxed write operation; dually, \(\downarrow A\) represents resources \(A\) obtained via a relaxed read, which may not be made use of until an acquire fence is encountered. The
A \triangle fence_{rel} \{A\} \quad \nabla A \triangle fence_{acq} \{A\}

\{\triangle Q(e) \ast \text{Rel}(l, Q)\} [l]_{rlx} := e \{\text{Init}(l) \ast \text{Rel}(l, Q)\}

\{\text{Init}(l) \ast \text{Acq}(l, Q)\} x := [l]_{rlx} \{\nabla Q[x/V] \ast \text{Acq}(l, V \neq x \Rightarrow Q)\}

(A_1 \Rightarrow A_2) \Leftrightarrow (\triangle A_1 \Rightarrow \triangle A_2) \Leftrightarrow (\nabla A_1 \Rightarrow \nabla A_2)

\nabla (A_1 \ast A_2) \equiv (\nabla A_1) \ast (\nabla A_2) \quad \text{and analogously for } \triangle \text{ and other binary connectives}

\textbf{Fig. 8.} Adapted FSL rules for relaxed atomics and fences.

proof rule for relaxed write is identical to that for a release write (cf. Fig. 6), except that the assertion to be transferred away must be under the $\triangle$ modality; this can be achieved by the rule for release fences. The rule for a relaxed read is the same as that for acquire reads, except that the gained assertion is under the $\nabla$ modality. The modality can be removed by a subsequent acquire fence. Finally, assertions may be rewritten under modalities, and both modalities distribute over all other logical connectives.

\textbf{Encoding.} The main challenge in encoding the FSL rules for fences is how to represent the two new modalities. Since these modalities guard assertions which cannot be currently used or combined with modality-free assertions, we model them using two \textit{additional heaps} to represent the assertions under each modality. The program heap (along with associated permissions) is a built-in notion in Viper, and so we cannot directly employ three heaps. Therefore, we construct the additional “up” and “down” heaps, by axiomatising bijective mappings \textit{up} and \textit{down} between a real program reference and its counterparts in these heaps. That is, technically our encoding represents each source location through three references in Viper’s heap (rather than one reference in three heaps). Assertions $\triangle A$ are then represented by replacing all references $r$ in the encoded assertion $A$ with their counterpart $\text{up}(r)$. We write $[A]^{\text{up}}$ for the transformation which performs this replacement. For example, $[\text{acc}(x.\text{val}) \&\& x.\text{val} == 4]^{\text{up}} \rightsquigarrow \text{acc}(\text{up}(x).\text{val}) \&\& \text{up}(x).\text{val} == 4$. We write $[A]^{\text{down}}$ for the analogous transformation for the $\text{down}$ function.

The extension of our encoding is shown in Fig. 9. We employ a Viper \textit{domain} to introduce and axiomatise the mathematical functions used to represent our $\text{up}$ and $\text{down}$ mappings. By axiomatising inverses for these mappings, we guarantee bijectivity. Bijectivity allows Viper to conclude that (dis)equalities and other information is preserved under these mappings. Consequently, we do not have to explicitly encode the last two rules of Fig. 8; they are reduced to standard assertion manipulations in our encoding.

An additional \textit{heap} function labels references with an integer identifying the heap to which they belong (we use 0 for real references, and -1 and 1 for their
domain threeHeaps {
  function up(x: Ref) : Ref;  function upInv(x: Ref) : Ref;
  function down(x: Ref) : Ref;  function downInv(x: Ref) : Ref;
  function heap(x: Ref) : Int; // identifies which heap a Ref is from
}

axiom { forall r:Ref :: upInv(up(r)) == r &&
  (heap(r) == 0 ==> heap(up(r)) == 1 ) }

axiom { forall r:Ref :: up(upInv(r)) == r &&
  (heap(r) == 1 ==> heap(upInv(r)) == 0 ) }

axiom { forall r:Ref :: downInv(down(r)) == r &&
  (heap(r) == 0 ==> heap(down(r)) == -1 ) }

axiom { forall r:Ref :: down(downInv(r)) == r &&
  (heap(r) == -1 ==> heap(downInv(r)) == 0 ) }

⌊⌊ A ⌋⌋ ⇝ ⌈ ⌊⌊ A ⌋⌋ ⌉ down

⌊⌊ △ A ⌋⌋ ⇝ ⌈ ⌊⌊ A ⌋⌋ ⌉ up

[ [ l ] ] rlx := e ... encoded as for release writes (Fig. 7) except using ⌈ inv(i) ⌉ up in place of inv(i)

[ [ l ] ] r lx := ... encoded as for acquire reads (Fig. 7) except using ⌈ inv(i) ⌉ down in place of inv(i)

[ fence_acq(A) ] ⇝ exhale ⌈ A ⌉; inhale ⌈ ⌊⌊ A ⌋⌋ ⌉ up

[ fence_rel(A) ] ⇝ var rs : Set[Ref]; rs := havoc() // unknown set of Refs
  assume forall r: Ref :: r in rs <=⇒ perm(down(r).val) > none
  inhale forall r: Ref :: r in rs <=⇒ acc(r.val, perm(down(r).val))
  assume forall r: Ref :: r in rs <=⇒ r.val == down(r).val
  exhale forall r: Ref :: r in rs <=⇒ acc(down(r).val, perm(down(r).val))
  // analogously for each other field, predicate (in place of val)

Fig. 9. Viper encoding of the FSL rules for relaxed atomics and memory fences. We omit triggers for the quantifiers for simplicity, but see [3].

“down” and “up” counterparts, respectively): this labelling provides the verifiers with the (important) information that these notional heaps are disjoint.

Our handling of relaxed read and write is almost identical to that of acquire reads and release writes in Fig. 7; this similarity comes from the original proof rules, which only require that the modalities be inserted when dealing with the invariant. Our encoding for release fences requires an annotation in the source program to indicate which assertion to prepare for release by placing it under the ⌈ modality. Inferring these assertions automatically is future work.

For the dual case of acquire fences, we can provide an encoding which does not require any user annotations. Any assertion that is under the △ modality can (and should) be converted to its corresponding version without the modality because △A is strictly less-useful than A itself. We encode this conversion as follows. We find all permissions currently held in the down heap, and transfer the permissions to (and values of) these locations over to the real heap. We encode this conversion for each field and predicate separately; the steps for the val field are shown at the end of Fig. 9. We first define a set rs to be precisely the set of all references r to which some permission to the field location down(r).val is currently held, i.e., perm(down(r).val) > none. Then, for each such location we inhale exactly the same amount of permission to the corresponding r.val location.
Viper allows such pointwise updates to the permissions held, via its support for permissions under quantifiers [19,18]. Having added permission to these locations, we can equate the heap values, and then remove the permission to the down locations, completing the conversion of these locations.

With our encoding based on multiple heaps, reasoning about assertions under modalities automatically inherits all of the natively-supported automation that Viper provides for permission and heap reasoning. We will reuse this idea for a different purpose in the following section.

5 Compare and Swap

C11 includes atomic read-modify-write operations, commonly used to implement high-level synchronisation primitives such as locks. In particular, the FSL++ logic [12] provides proof rules for compare and swap (CAS) operations, as supported natively by many architectures and libraries. An atomic compare and swap \( \text{CAS}_{\tau}(l,e,e') \) reads and returns the value of location \( l \); if the value read is equal to \( e \), it also writes the value \( e' \) (otherwise we say that the CAS fails).

**FSL++ proof rules.** The latest proof rules for C11 CAS operations come from FSL++. They extend the previously-presented logic with a new assertion \( \text{RMWAcq}(l,Q) \), which is similar to \( \text{Acq}(l,Q) \), but is used for transferring ownership via CAS operations instead of acquire reads. The essential idea is for a successful CAS operation to both obtain ownership of an assertion via its read operation, and give up ownership of an assertion via its write operation.

FSL++ does not support general combinations of atomic reads and CAS operations on the same location; the way of reading must be chosen at allocation via the annotation \( \rho \) on the allocation statement (see Fig. 1). In contrast to the \( \text{Acq} \) assertions used for atomic reads, \( \text{RMWAcq} \) assertions can be freely duplicated and their invariants need not be rewritten for a successful CAS: when using only CAS operations, each value read from a location corresponds to a different write.

Fig. 10. Adapted FSL++ rules for compare and swap operations. \( FV \) yields the free variables of an assertion.
Our presentation of the relevant proof rules is shown in Fig. 10. Allocating a location with annotation RMW provides a Rel and a RMWAcq assertion, such that the location can be used for release writes and CAS operations.

For the CAS operation, we present a single, general proof rule instead of four rules for the different combinations of access modes in FSL++. The rule requires that l is initialised (since its value is read), Rel and RMWAcq assertions (the fact that Rel is required is a technicality, which we will not explain here), and an assertion P that provides the resources needed for a successful CAS. If the CAS fails (that is, \( x \neq e \)), its precondition is preserved.

If the CAS succeeds, it has read value \( e \) and written value \( e' \). Assuming for now that the access mode \( \tau \) permits ownership transfer, the thread has acquired \( Q[e/V] \) and released \( Q[e'/V] \). As illustrated in Fig. 11(i), these assertions may overlap. Let \( T \) denote the assertion characterizing the overlap; then assertions \( A \) denotes \( Q[e/V] \) without the overlap, and \( P \) denotes \( Q[e'/V] \) without the overlap. The net effect of a successful CAS is then to acquire \( A \) and to release \( P \), whereas \( T \) remains with the location invariant across the CAS. The proof rule is phrased in terms of \( T, A, \) and \( P \). Automating the choice of these parameters is one of the main challenges of encoding this rule. Finally, if the access mode \( \tau \) does not permit ownership transfer (that is, fences are needed to perform the transfer), \( A \) and \( P \) are put under the appropriate modalities.

**Encoding.** Our encoding of CAS operations uses several techniques presented in earlier sections; see App. E for details. We represent RMWAcq assertions analogously to our encoding of Acq assertions (see Sec. 3). We use the value of field \( \text{acq} \) (cf. Fig. 7) to differentiate between holding some RMWAcq assertion.

---

\[ FSL++ \] also includes a fifth rule for learning that, in certain cases, a CAS operation is guaranteed to fail. We have not yet modelled this rule directly (which was not needed for our examples), but believe the extension to be fairly simple if required. Similarly, the general proof rules include optional parameterisation by additional quantifiers, which can be handled, but would complicate the presentation.
from some Acq assertion. Since RMWAcq assertions are duplicable (cf. Fig. 10), we employ wildcard permissions for the corresponding AcqConjunct predicates.

Our encoding of the proof rule for CAS operations is somewhat involved; we give a high-level description of our approach here, and relegate the details to App. E. We focus on the more-interesting case of a successful CAS operation here. The key challenge is how to select an appropriate assertion $T$ to satisfy the premises of the rule; while we could take $T$ as an annotation, we observed that choosing this overlap to be as large as possible is desirable in practice (since this reduces the resources to be transferred, and which must interact in some cases with the modalities). We write out Viper code to indirectly compute this largest-possible $T$ as follows (see Fig. 11(ii) for an illustration).

We introduce yet another heap (“tmp”) in which we inhale the invariant for the value read ($Q[e/V]$). Now, we attempt to exhale the invariant for the value written ($Q[e'/V]$), but adapt the assertions as follows: for each permission in the invariant, we take the maximum possible amount from our “tmp” heap; these permissions correspond to $T$. Any remainder is taken from the current heap (either the real or the “up” heap, depending on $\tau$); these correspond to $P$. We can express this by rewriting the assertion: for example, if $\tau = rlx$ and $[Q[e'/V]] \equiv \text{acc}(x.f,p)$, we exhale let $p' = \min\text{perm}(\text{tmp}(x).f,p)$ in $\text{acc}(\text{tmp}(x).f,p') \land \text{acc}(\text{up}(x).f,p - p')$. If this modified exhale succeeds, any remaining permissions in the “tmp” heap correspond to the assertion $A$ and are moved (in a way similar to our fence encoding in Fig. 9) to either the real or “down” heap (depending on $\tau$).

This combination of techniques results in an automatic support for CAS statements and their corresponding proof rule: all of the above steps can be statically generated. This completes the core of our Viper encoding, which now handles the complete set of memory access constructs from Fig. 1.

6 Additional Features

Our encodings support a number of additional features which, for space reasons, we describe only briefly here. Firstly, FSL++ adds rules for ghost state to the program logics; ghost locations are fictitious (non-atomic) heap locations added to a program purely for reasoning purposes. For ghost locations, the modalities collapse: if an assertion $A$ depends only on ghost locations, then $\Delta A \equiv A \equiv \nabla A$ holds [12]. Extending our encoding is simple; we track ghost status with an extra boolean function, and tweak our axiomatisation of multiple heaps (Sec. 4) to make the up and down functions act as identities on ghost locations (details in App. D).

Atomic read and CAS operations are often employed in simple spin loops which wait to read a particular value. Our encoding requires loops to be annotated with invariants in the general case; however, for spin loops (i.e. loops which poll a location via atomic reads or CAS operations until a certain value is read) we can avoid this, based on the following observation: every loop iteration except for the very last (and the first, for atomic reads rather than CAS operations) will make no change to the owned resources. For verification purposes, therefore, it is
sufficient to encode only these iterations of spin loops, removing the need for a loop and invariant at the Viper level.

Our encoding also supports fetch-update instructions (such as atomic increment) commands natively. These differ from CAS operations in two ways: they never fail, and the updated value can be a function of the value read. Such commands could also be implemented with CAS operations and loops [12], but this is less efficient for architectures which support atomic fetch-update instructions natively.

The RSL logics do not allow resources to be directly leaked; there are no rules for weakening an assertion in order to drop unneeded permissions or assertions such as Rel and Acq assertions during a proof. Nevertheless, the RSL logics do not guarantee absence of memory leaks in general, due to the rules for atomics; there is no guarantee that resources transferred by one thread will be received by another. In order to get rid of unneeded resources, postconditions proved in the RSL logics typically include true as a conjunct, which can be used to hide unwanted assertions. (In such separation logics, true is used to represent arbitrary resources, while emp represents no resources at all). We reflect this practice by adapting the RSL rules to use true instead of emp throughout. In Viper, resources can be leaked by default, at any time. However, using Viper’s perm construct, we can nonetheless encode additional checks that e.g. ownership of non-atomic locations is never leaked (we do this in our examples).

7 Examples and Evaluation

We have evaluated our encoding by applying it to a number of examples (described below). We are in the process of developing a front-end to generate the appropriate Viper code; for the present time, we have done so by hand. The encoded examples are available in the online appendix [3], and examples of the corresponding input source code (in the language of this paper) are given in App. B.

The encoded versions of the examples make heavy use of Viper macros, to aid readability. Each example consists of three parts: a set of background definitions (e.g. macros to encode each statement), a set of invariant definitions (specific to the example; these reflect the image of the indexing discussed in Sec. 3 along with, e.g., their ⌈ down variants), and a set of method definitions, corresponding to the translation of the original source code. The three parts are presented in reverse order (so that the source code translation comes first in each file). We also constructed some variations which exercise, e.g., the support for rewriting Acq invariants, since in all other examples our automatic support for tracking conjuncts was sufficient.

As a starting point, we took the examples from the RSL [28] and FSL [13] papers, along with variants of these to demonstrate and test additional features of the logics and our encoding. We also investigated encoding the main example from the latest FSL++ paper [12], which is the Rust reference-counting library [11]. Our encoding does not yet support all of the features of the latest paper; in particular, the proof in [12] requires customising the underlying permission model,
which Viper does not directly support. Following the suggestion of one of the authors [27], we were however able to encode two variants of the original example, in which some of the access modes are strengthened, making the code slightly less efficient but enabling a proof using a simpler permission model. These variants still require counting permissions [6], which we were able to express with additional background definitions (reusable for other examples) in the Viper file.

Finally, we tackled seven functions taken from a reader-writer-spinlock in the Facebook Folly library [2]. We were able to verify five of the functions simply, but two employ code idioms which seem to be beyond the scope of the RSL logics, at least without sophisticated extra ghost state; the code depends on the combined effects of multiple atomic accesses (rather than reasoning about these individually). For both functions, we developed alternative implementations which could be handled by the logics and our encoding.

Our initial experiences with our encoding are promising; verification times were reasonable (generally around 10 seconds, and always under a minute), and several errors in our initial specification attempts (and typos in the example code) were uncovered during their development. It is clear that a front-end for our encoding will be necessary to evaluate it on larger codebases; this is largely a matter of engineering (and good error reporting!), and is already underway. The Rust and Facebook code quickly demonstrated a key advantage of working in a general verification framework such as Viper; both examples required support for extra theories (counting permissions as well as modulo and bitwise arithmetic), and we were able to plug such reasoning in simply.

In terms of annotation overhead, the examples require specifications (the ratio between specifications and code was roughly 1:1 for each example tackled so far), but no manual assertions (e.g., between statements) were necessary to make the verification go through. The overhead involved compares favourably to a manual proof effort; an informal proof outline would also require (at least) one intermediate assertion between every statement, while the Coq-formalised proofs of the first RSL examples require roughly ten lines of proof per line of code [28], and for the Rust reference counting example (albeit for an unmodified version of the implementation; i.e., a harder proof), the ratio is around 100:1. Such ratios are consistent with other recent Coq-mechanised proofs based on separation logic [29].

8 Conclusions and Future Work

We have presented the first encoding of modern program logics for weak memory models into a deductive program verifier. The encoding enables programs (with suitable annotations) to be verified automatically by existing back-end tools. Moreover, the encoding into a general-purpose verification framework such as Viper provides additional features such as theory reasoning in a straightforward manner (an example being the counting permissions used in our reference counting proofs).
Building front-end verifiers for such advanced logics will enable them to be applied to more, and larger, examples; we are currently working on building a front-end for the translation presented here. In future work, we plan to prove the soundness of the presented encoding; a key ingredient will be the mapping back from a Viper program state to the analogous program state in the RSL logics.

We are interested in tackling other modern program logics such as GPS, which also handles weak memory. We believe that many of the techniques described in this paper can be carried over, and applied to build practical tools that implement these advanced logics. The quick feedback provided by such tools will also enable us to identify weaknesses in the logics themselves, inspiring further developments.

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A Full Source Encoding

The encoding of the general source language of assertions is given below (we assume the encoding of pure expressions, which can typically be the identity mapping, assuming all operators supported such as addition, equality etc. are all supported natively by Viper).

$$\lfloor \lceil \lfloor \text{emp} \rfloor \rceil \rceil \rightarrow \text{true}$$

$$\lfloor l \mapsto e \rfloor \rightarrow \text{acc}(l.\text{val}, k) \& \& \text{acc}(l.\text{init}, k) \& \& \ l.\text{val}=\lfloor e \rfloor \& \& l.\text{init}$$

$$\lfloor [A_1 \ast A_2] \rfloor \rightarrow \lfloor A_1 \rfloor \& \& \lfloor A_2 \rfloor$$

$$\lfloor (b \Rightarrow A) \rfloor \rightarrow \lfloor b \rfloor \Rightarrow \lfloor A \rfloor$$

$$\lfloor (b \ ? \ A_1 : A_2) \rfloor \rightarrow \lfloor [b] \ ? \lfloor A_1 \rfloor : \lfloor A_2 \rfloor \rfloor$$

$$\lfloor \text{Uninit}(l) \rfloor \rightarrow \text{acc}(l.\text{val}) \& \& \text{acc}(l.\text{init}) \& \& \l.\text{init}$$

$$\lfloor \text{Acq}(l, Q) \rfloor \rightarrow \text{acc}(l.\text{acq}, \text{wildcard}) \& \& l.\text{acq}=\text{true} \& \& \ (\text{foreach } i \text{ in } \langle Q \rangle : \text{AcqConjunct}(l, i) \& \& \ \text{valsRead}(l, i)==\text{Set[Int]}() \text{ end})$$

$$\lfloor [\text{Rel}(l, Q)] \rfloor \rightarrow \text{acc}(l.\text{rel}, \text{wildcard}) \& \& l.\text{rel}==\langle Q \rangle$$

$$\lfloor [\text{Init}(l)] \rfloor \rightarrow \text{acc}(l.\text{init}, \text{wildcard})$$

$$\lfloor A \rfloor \uparrow \rightarrow \lfloor A \rfloor$$

$$\lfloor A \rfloor \downarrow \rightarrow \lfloor A \rfloor$$

$$\lfloor [\text{RMWAcq}(l, Q)] \rfloor \rightarrow \text{acc}(l.\text{acq}, \text{wildcard}) \& \& l.\text{acq}=\text{false} \& \& \ (\text{foreach } i \text{ in } \langle Q \rangle : \text{acc}(\text{AcqConjunct}(l, i), \text{wildcard}) \text{ end})$$

B Example Details

To give an impression of the input required for our encoding, we provide source code corresponding to some of our encoded examples from the Online Appendix [3], given in Figures 12 to 16.

C Rewriting Invariants

It is unusual (at least, in the examples we have investigated so far) for very many different invariants for atomic locations to be needed; it is even less common for there to be a need for many different invariants for the same atomic location. Indeed, for Rel and RMWAcq assertions, since the assertions are duplicable, one may as well always use the same invariant. For Acq assertions the situation is more interesting; it may be desirable to split the invariant (as used e.g. in Fig. 15) across several Acq assertions, and programmer-annotated assertions may not always syntactically match up precisely (since there might be more readable ways of expressing an equivalent assertion). Since our indexing of Acq invariants matches their conjuncts syntactically, additional work is required if this syntactic match would be overly restrictive. For example, in the example shown in Fig. 15 the initial Acq invariant is expressed more succinctly in a way which does not provide the immediate conjuncts needed by the (left and
\[ Q \equiv (V = 0 \ ? \ true : (V = 1 \ ? \ J : false)) \]

\[ Lock(x) \equiv \text{Init}(x) \ast \text{RMWAcq}(x, Q) \ast \text{Rel}(x, Q) \]

new_lock() returns (x)
\begin{align*}
\text{requires } J \\
\text{ensures Lock}(x) \\
\{ \\
x := \text{alloc}_{acq}(Q); \\
[x]_{\text{ret}} := 1; \\
\} 
\end{align*}

unlock(x)
\begin{align*}
\text{requires } J \ast Lock(x) \\
\text{ensures Lock}(x) \\
\{ \\
[x]_{\text{ret}} := 1; \\
\} 
\end{align*}

lock(x)
\begin{align*}
\text{requires Lock}(x) \\
\text{ensures } J \ast Lock(x) \\
\{ \\
\text{while}(\text{CAS}_{\text{rel,acq}}(x, 1, 0) \neq 1); \\
\} 
\end{align*}

\[ (V = 0 \ ? \ a \mapsto 7) \]

\begin{align*}
\{ \text{emp} \\
a := \text{alloc}_{acq}(); \\
c := \text{alloc}_{acq}(Q); \\
[e]_{\text{rel}} := 1; \\
\{ \text{Uninit}(a) \ast \text{Rel}(c, Q) \} \\
[a]_{\text{acq}} := 7 \\
[e]_{\text{rel}} := 1 \\
\{ \text{Rel}(c, Q) \} \\
\{ a \mapsto 8 \ast true \} \\
\end{align*}

Fig. 12. RSL Figure 7 example, written in our source language. Annotations in blue.

\[ (V = 0 \ ? \ a \mapsto 7) \]

\begin{align*}
\{ \text{emp} \\
a := \text{alloc}_{acq}(); \\
c := \text{alloc}_{acq}(Q); \\
[e]_{\text{rel}} := 1; \\
\{ \text{Uninit}(a) \ast \text{Rel}(c, Q) \} \\
[a]_{\text{acq}} := 7 \\
[e]_{\text{rel}} := 1 \\
\{ \text{Rel}(c, Q) \} \\
\{ a \mapsto 8 \ast true \} \\
\end{align*}

Fig. 13. RSL Figure 8 example, written in our source language. Annotations in blue.
\[ Q_1 \equiv (V \neq 0 \Rightarrow a \mapsto 42) \quad Q_2 \equiv (V \neq 0 \Rightarrow b \mapsto 7) \]
\[
\begin{array}{l}
a := \text{alloc}_{na}(); \quad b := \text{alloc}_{na}(); \quad x := \text{alloc}_{acq}(Q_1); \quad y := \text{alloc}_{acq}(Q_2);
\end{array}
\]
\[
\begin{array}{l}
[x]\rl := 0; \quad [y]\rl := 0;
\end{array}
\]
\[
\begin{array}{l}
\{\text{true}\} \quad \{\text{Acq}(x, Q_1) \land \text{Init}(x)\}
\end{array}
\]
\[
\begin{array}{l}
\{\text{true}\} \quad \{\text{Acq}(y, Q_2) \land \text{Init}(y)\}
\end{array}
\]

\[ \begin{array}{l}
\text{while } ([x]\rlx == 0); \\
fence_{acq}; \\
z := [a]_{na} \\
[a]_{na} := z + 1 \\
\{\text{true} \land a \mapsto 43\}
\end{array} \]
\[
\begin{array}{l}
\text{while } ([y]\rlx == 0); \\
fence_{acq}; \\
w := [b]_{na}; \\
[b]_{na} := w + 1 \\
\{\text{true} \land b \mapsto 8\}
\end{array}
\]

\[ \begin{array}{l}
\text{fence}_{rel}(a \mapsto 42 \land b \mapsto 7); \\
\{\text{true} \land \text{Init}(x) \land \text{Init}(y)\}
\end{array} \]
\[
\begin{array}{l}
\text{fence}_{rel}(a \mapsto 43 \land b \mapsto 8);
\end{array}
\]

Fig. 14. FSL Figure 2 example, written in our source language. Annotations in blue.

right) forked threads. In such cases, we support an additional rewrite statement rewrite \text{Acq}(l, Q) \text{ as } \text{Acq}(l, Q') in the source program to explain the intended rewriting. To check that such a statement is justified, we need to check the entailment between the original and new invariants, for all values of \( V \). Furthermore, this entailment check cannot be made directly in the current state, since that might already contain permissions and value information which could unsoundly weaken the check made, or even contradict the invariants involved, resulting in an infeasible program state from there onwards.

To avoid these issues, we perform the following steps (shown in Fig. 17). For simplicity, we do not handle the case of rewriting invariants for which values have already been read (we check that this is not the case, here, but an extension is possible). Firstly, we create a non-deterministic if-branch. Inside the branch we remove all permissions from the current state. We then havoc an integer variable, representing the arbitrary value of \( V \) for which the subsequent check should hold. We inhale the original invariant (using our indexing as usual), and exhale the invariant to which it is to be rewritten. If this succeeds, we know that the rewriting is justified; the one invariant entails the other, for all values of \( V \). We then kill this branch, by adding an assume false to it; subsequently, only the other branch (in which no changes were made) will be considered for verification.

Lastly, we perform the rewriting itself by discarding all of the original \text{AcqConjunct} instances, and replacing them with the new ones. Verification can then proceed as usual.

D Ghost Locations

We extend our encoding to handle ghost locations in a simple manner. Firstly, we add a boolean function \text{is / - ghost} on references, to identify whether or not a location is ghost. We added macros \text{realRef}(r) to add the appropriate assumptions for a real program reference, and \text{ghostRef}(r) for ghost locations; this can be seen
\[ Q_1 \equiv (V \neq 0 \Rightarrow a \mapsto 42) \quad Q_2 \equiv (V \neq 0 \Rightarrow b \mapsto 7) \]
\[ Q_3 \equiv (V \neq 0 \Rightarrow a \mapsto 42 \ast b \mapsto 7) \]
\[
\begin{align*}
\{\text{true}\} & \\
\end{align*}
\]
\[
\begin{align*}
\text{a} & := \text{alloc}_{\text{na}}(); \quad \text{b} := \text{alloc}_{\text{na}}(); \quad \text{x} := \text{alloc}_{\text{acq}}(Q_3); \\
\text{rewrite Acq}(x, Q_3) & \text{ as } \text{Acq}(x, Q_1 \ast Q_2); \\
[x]_{\text{rlx}} & := 0; \\
\{\text{Acq}(x, Q_1) \ast \text{Init}(x)\} & \text{ while }([x]_{\text{rlx}} == 0); \\
& \text{fence}_{\text{acq}}; \\
& \text{z} := \text{[a]}_{\text{na}} \\
& \text{[a]}_{\text{na}} := \text{z} + 1 \\
& \{\text{true} \ast a \mapsto 43\} & \text{[true} \ast a \mapsto 43 \ast b \mapsto 8\} \\
& \text{[true} \ast a \mapsto 43 \ast b \mapsto 8\} \\
& \{\text{true} \ast b \mapsto 8\} \\
\end{align*}
\]

Fig. 15. Variant of FSL Figure 2 example (using invariant rewriting), written in our source language. Annotations in blue.

as the translation of “type information”, since we assume that ghost locations are labelled as such in the original program.

For ghost locations we tweak our multiple heaps encoding to change the assumptions about the \text{up} and \text{down} mappings to instead require them to act as the identity (correspondingly, the result of \text{heap} is no longer constrained to be different after applying these mappings to a ghost reference). This immediately gives us that, for assertions depending only on ghost locations in the heap, \( \triangle A \), \( A \) and \( \nabla A \) will be handled equivalently; since (up to syntactic applications of these identify mappings) they will be encoded as identical assertions.

Finally, we add an assumption of \text{realRef}(r) to our existing statements for allocating references, and add a new ghost allocation statement, for which the analogous \text{ghostRef}(r) assumption is added. The most-relevant details are summarised in Fig. 18.

E Compare and Swap Details

The details of our encoding of the FSL++ compare and swap rules (cf. Fig. 10) are shown in Fig. 19. We represent \text{RMWA} assertion similarly to \text{Acq} assertions (cf. Fig. 7), but and a \text{false} value of the \text{acq} field to differentiate holding one from the other. Recall that we must choose at allocation whether atomic reads or compare and swaps will be used to gain ownership via the atomic location; this choice is then reflected in the field value. The encoding of allocation is then straightforward.

The handling of a CAS statement itself involves initially checking that we indeed hold some \text{Init}, \text{RMWA} and \text{Rel()} assertions for the location, according to the precondition of the rule, and then using an if-condition over the fresh read value \( x \) to narrow us down to the case of a successful CAS. The subsequent
\[ Q \equiv V \geq 0 \ast g \overset{1 \xrightarrow{V+rd}}{\ast} \_ \ast (V \geq 1 \Rightarrow d \overset{1 \xrightarrow{V+rd}}{\ast} \_) \]

\[ ARC(d, c, g, v) \equiv d \overset{V \ast}{\xrightarrow{V + rd}} \ast \text{RMWA}(c, Q) \ast \text{Rel}(c, Q) \ast \text{Init}(c) \]

new(v) returns (d,c,g)

\textbf{requires} true

\textbf{ensures} ARC(d, c, g, v)

\{
\begin{align*}
\ d &\coloneqq \text{alloc}_{na}(); \\
\ g &\coloneqq \text{alloc}_{ghost}(); \\
\ c &\coloneqq \text{alloc}_{RMW}(Q); \\
\ [d]_{na} &\coloneqq v; \\
\ [c]_{rel} &\coloneqq 1;
\end{align*}
\}

\textbf{drop}(d,c,g)

\textbf{requires} ARC(d, c, g, \_)

\textbf{ensures} true

\{
\begin{align*}
\ t &\coloneqq \text{fetch}_{\_\text{and\_add}}_{rel}(c, -1); \\
\text{if } (t==1) \{ \\
\ &\quad \text{fence}_{acq}; \\
\ &\quad \text{free}(d); \\
\\}
\end{align*}
\}

\textbf{read}(d,c,g) returns (v)

\textbf{requires} ARC(d, c, g, \_)

\textbf{ensures} ARC(d, c, g, v)

\{
\begin{align*}
\ v &\coloneqq [d]_{na}; \\
\\}
\}

\textbf{clone}(d,c,g)

\textbf{requires} ARC(d, c, g, v)

\textbf{ensures} ARC(d, c, g, v) \ast ARC(d, c, g, v)

\{
\begin{align*}
\ &\quad \text{fetch}_{\_\text{and\_add}}_{acq}(c, 1); \\
\\}
\}

\textbf{Fig. 16.} Rust reference counting variant 2 (in online appendix). Compared to the original code (see [12]) we modified the write in \textit{new} to use a release rather than relaxed mode, and the update in \textit{clone} to use acquire rather than relaxed. As discussed in the paper body, the original version of the example is proved in [12] using features which are not yet supported by our encoding. We do, however, exploit the CAS rules and rules for fences here. We write \textit{rd} for a read permission, in the sense of counting permissions \[6\]. The ghost location \textit{g} must be identifiable as such for the encoding, for example by considering this a type annotation, or using a distinguished class of variables for ghost locations. We model the \textit{free} statement by exhaling the corresponding permissions.
Viper code reflects the three steps described in Sec. 5 and Fig. 11. Firstly, we perform the inhale of newly-gained resources (corresponding to \( Q[e/V] \)) into the \texttt{tmp} heap.

Secondly, we attempt to exhale the assertion \( Q[e'/V] \), modified so that the permissions are taken preferentially from the \texttt{tmp} heap, and failing this, from the real heap or \texttt{up} heaps, depending on whether or not the write synchronises. This modification of the assertion (which splits the permission amounts across the two heaps, as described in Sec. 5) is denoted by the \( 
\left\lfloor .\right\rfloor^\text{tmp/real} \) and \( 
\left\lfloor .\right\rfloor^\text{tmp/up} \) mappings; if the \texttt{values} of heap locations are also mentioned in the parameter assertions, then these heap dereferences must also be rewritten to a dereference in the corresponding heap (e.g. \( x.val == 4 \) might become \( \texttt{tmp}(x).val == 4 \)). In case permission to the corresponding location is taken partly from both heaps,
define realRef(x) !is_ghost(x) && heap(x) == 0
define ghostRef(x) is_ghost(x) && heap(x) == 0

domain parallelHeaps {
  function up(x: Ref) : Ref
  function down(x: Ref) : Ref
  function up_inv(x: Ref) : Ref
  function down_inv(x: Ref) : Ref
  function temp(x: Ref) : Ref
  function temp_inv(x: Ref) : Ref
  function heap(x: Ref) : Int
  function is_ghost(x: Ref) : Bool

  axiom { forall r:Ref : up_inv(up(r)) == r &&
    (is_ghost(r) ? up(r) == r : heap(r)==0 ==> heap(up(r)) == 1) }
  axiom { forall r:Ref : {up_inv(r)} up(up_inv(r)) == r &&
    (is_ghost(r) ? up_inv(r) == r : heap(r)==1 ==> heap(up_inv(r)) == 0) }
  axiom { forall r:Ref : {down_inv(r)} down_inv(down(r)) == r &&
    (is_ghost(r) ? down_inv(r) == r : heap(r)==-1 ==> heap(down_inv(r)) == 0) }
  axiom { forall r:Ref : {down(r)} down_inv(down(r)) == r &&
    (is_ghost(r) ? down(r) == r : heap(r)==-1 ==> heap(down_inv(r)) == 0) }
  axiom { forall r:Ref : {temp(r)} temp_inv(temp(r)) == r &&
    (is_ghost(r) ? temp(r) == r : heap(r)==0 ==> heap(temp(r)) == -3) }
  axiom { forall r:Ref : {temp_inv(r)} temp(temp_inv(r)) == r &&
    (is_ghost(r) ? temp_inv(r) == r : heap(r)==-3 ==> heap(temp(r)) == 0) }
}

[l := alloc_ghost()] ~>
x := new(); assume ghostRef(x); // ghost location
inhale Uninit(x) // ghost locations are non-atomics

Fig. 18. Extension of our Viper encoding to handle ghost locations.

the extra assumption that the two values are the same can be explicitly added by these mappings.

Finally (assuming the exhale has succeeded, otherwise a verification failure will have been encountered), all remaining permissions in the tmp heap are transferred to either the real or down heap, depending on whether the read synchronises.
define SomeRMWAcq(l) acc(l.acq, wildcard) && l.acq == false

RMWAقل(l, Q) ⇝ SomeRMWAcq(l) &&
(∀ i ∈ Q : acc(AcqConjunct(l, i), wildcard))

l := allocRMW(Q) ⇝

x := new(); assume realRef(x); // not a ghost location

inhale Rel(l, Q) & RMWAقل(l, Q)

x := havoc();

Casτ(l, e, e') ⇝

assert Init(l) && SomeRMWAcq(l) && SomeRel(l)

x := havoc();

// inhale into tmp heap

if(x == e) {
    foreach i in indices do
        inhale AcqConjunct(l, i)
    end
}

// exhale from tmp & real/up heaps (depending on τ)

foreach i in indices do
    if (i == l.rel) { // write synchronises
        if (τ ∈ {rel, rel_acq}) {
            exhale AcqConjunct(l, i)
        } else {
            exhale AcqConjunct(l, i)
        }
    }
end

// ... move tmp heap to real/down heap (depending on τ)

var rs : Set(Ref); rs := havoc(); // unknown set of Refs
assume forall r : Ref : r ∈ rs ⇐⇒ perm(tmp(r).val) > none
if(τ ∈ {acq, rel_acq}) {
    inhale forall r : Ref : r ∈ rs ⇐⇒ acc(r.val, perm(tmp(r).val))
    assume forall r : Ref : r ∈ rs ⇐⇒ r.val == tmp(r).val
} else {
    inhale forall r : Ref : r ∈ rs ⇐⇒ acc(down(r).val, perm(tmp(r).val))
    assume forall r : Ref : r ∈ rs ⇐⇒ down(r).val == tmp(r).val
}

exhale forall r : Ref : r ∈ rs ⇐⇒ acc(tmp(r).val, perm(tmp(r).val))

// analogously for each other field, predicate (in place of val)

Fig. 19. Viper encoding of the RSL rules for compare and swap operations.

26