Ground Current Suppression for Grid Connected Transformerless Photovoltaic Inverter with Filter Capacitor

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Abstract. The full-bridge inverter with unipolar PWM (UPWM) or hybrid PWM (HPWM) has higher efficiency and lower filtering requirement. However, when it is used for grid-connected transformerless photovoltaic system, the ground current may be high due to the parasitic capacitors and high frequency common-mode voltage. In this paper, the output filter capacitor is proposed to suppress the ground current. In this method, the output filter capacitor is paralleled with the parasitic capacitors. The analytical method is established to calculate the ground current. The effect of the novel method under different modulation technique is studied. Efficiency estimation is done for comparison of different topologies. Finally, the validity of the proposed method is verified by simulation and experimental results.

1. Introduction
Grid connected photovoltaic (PV) systems have an important role in distributed power generation. Many grid-connected PV systems have a transformer for the electrical isolation between the conversion stage and the grid for safety reasons. The transformer increases the weight, size, cost, and reduces the overall efficiency [1]. Transformerless structure seems to be more advantageous. However, without the isolation transformer, the grid connected transformerless PV system has a galvanic connection between the PV arrays and the grid, due to the existence of parasitic capacitors. The capacitors are formed between the solar cell and the normally ground frame [2]. The parasitic capacitors, the PV inverter, the filter and the grid constitute a common-mode loop where the ground current flows through.

The circulation of the ground current leads to increased electromagnetic emissions, grid current distortion, additional power losses in the system, and especially safety hazards in the event of ground faults [3]. Therefore, it needs to be limited. The ground current is dependent on the amplitude and frequency content of the voltage fluctuations which present at the PV panel terminals, and the parasitic capacitors [4]. The parasitic capacitors are determined by many factors, such as physical structure of the array and the weather conditions. For crystalline silicon cells, 50~150 nF/kW are expected. When for thin-film modules, the capacitance up to 1μF/kW has been observed [5]. The voltage fluctuations are determined by the topologies and the inverter’s modulation technique.

The ground current suppression methods can be normally divided into three types. The first method is to reduce the common mode voltage, such as HERIC topology [6], the full-bridge zero voltage rectifier (FB-ZVR) [7], H5 topology [8] and the full-bridge inverter with DC bypass (FB-DCBP) [9]. In these topologies, some additional power devices are used to achieve the decoupling of AC side and DC side. The second method is to increase the common mode loop impedance to
reduce ground current, such as the common mode filter and the common mode transformer. The third method is to use additional capacitors which are paralleled with the parasitic capacitors. Then, the ground current is diverted to the paralleled capacitors. It has been widely used in three-phase systems, such as 3FB-SC (the three-phase half-bridge inverter) and 3xNPC (the mid-point clamped three-phase level inverter) using the DC-link capacitor to divert the ground current. Another bypass method is to connect the LC filter star point to the DC-link terminals. It has an important advantage over the classical output filter due to its suppression on both common-mode and differential mode current. The ground current can be reduced due to the current shut without the additional active device.

In this paper, a ground current suppression method is proposed by using output filter capacitors for the non-isolated full-bridge inverter. The rest of the paper is organized as follows. Section 2 gives the common-mode model to estimate the ground current using different modulation techniques. Section 3 gives the efficiency estimation of different topologies. Simulation and experimental results are given in section 4.

2. FB inverter with the output filter capacitors

2.1. Common-mode model of FB inverter

![Figure 1: Transformerless FB inverter with output filter capacitors](image)

Figure 1 shows the grid connected transformerless FB inverter with the output filter capacitors C′1, C′2 connected to the dc-link terminals. The parasitic capacitors Cpv1 and Cpv2, which is shown as dashed lines in Figure 1, present between the PV terminals and ground connection points of the inverter (0). L1 and L2 are the output filter inductors which are used to filter out the switching component of the output current. Zg is the grounding resistance.

In order to simplify the analysis, the following conditions are assumed. The inverter has reached steady state. All power devices are assumed as ideal switches. The dc-link voltage is kept constant. Modulation wave is a sine-wave signal. The grid impedance and the line impedance are not considered. The mismatch of the power devices and the dead-time are not considered.

![Figure 2: Common-mode model of FB inverter with the output filter capacitors](image)

The model of the grid connected transformerless full-bridge inverter with the neutral-point-clamped capacitors is shown in Figure 2, where Cpv is the parasitic capacitor, and Cpv = Cpv1 + Cpv2, C′ is the output filter capacitors, and C′ = C′1 + C′2. The impact of the grid voltage uG on the common mode current is small due to its low frequency of 50 or 60 Hz. The total common mode voltage ucmc is defined by (1),

$$u_{cmc} = \frac{u_{AN}L_2 + u_{BN}L_4}{L_4 + L_2} = u_{cm} + u_{mn}$$
Where the contribution of the inductor unbalance $u_{im}=(u_{AN}-u_{BN})(L_2-L_1)/2(L_1+L_2)$ and the common-mode voltage sources $u_{cm}=(u_{AN}+u_{BN})/2$. The equation of the ground current $i_{in1}$ can be derived as

$$i_{in1} = -\frac{G}{sL_2(L_2+S+1)}u_{cm}G = \frac{1}{(1/sC_p + Z_s)}$$

(2)

Based on the assumption of the output filter inductor $L_1=L_2=L$, (2) can be simplified to

$$i_{in1} = -\frac{G}{(sL/2)}(G + sC')u_{cm}$$

(3)

It can be seen that the ground current is determined by the parasitic capacitor $C_p$, the output filter inductor $L$, the output filter capacitor $C'$ and the common-mode voltage $u_{cm}$. The common-mode voltage is determined by the dc-link voltage and the modulation technique.

2.2. Modulation technique

The modulation technique determines the switch states of each phase in the inverter. Once the switch states and the dc-link voltage are known, the magnitude and the frequency of the common mode voltage are decided.

![Modulation Technique Diagram](image)

Figure 3 Schematic of modulation technique for FB inverter

The schematic of modulation technique for full-bridge inverter is shown in Figure 3, where $u_{AB}$ is the output voltage of inverter. Using HPWM, Leg A is switched with high PWM frequency and leg B is switched with low grid frequency, which is shown in Figure 3(a). Using UPWM, Leg A and leg B are both switched with high frequency with mirrored sinusoidal reference $u_a$, $u_b$. $S_1(S_3)$ and $S_2(S_4)$ are operated complementarily, shown in Figure 3(b).

The double Fourier series of $u_{cm}$ for HPWM is deduced as follows.

$$u_{cm} = \frac{U_{cm}}{2} + \frac{U_{cm}}{\pi} \sum_{n=1}^{\infty} \frac{(1+\cos n\pi)}{m} \sin \left(\frac{n\pi}{2}\right) J_n \left(\frac{m+n}{2}\right) \left[ \sin \left(\frac{n\pi}{2}\right) \cos \left(\frac{(m+n)\alpha}{2}\right) \right]$$

(4)

And for UPWM,

$$u_{cm} = \frac{U_{cm}}{2} + \frac{U_{cm}}{\pi} \sum_{n=1}^{\infty} \frac{(1+\cos n\pi)}{m} \sin \left(\frac{n\pi}{2}\right) J_n \left(\frac{m+n}{2}\right) \left[ \sin \left(\frac{n\pi}{2}\right) \cos \left(\frac{(m+n)\alpha}{2}\right) \right]$$

(5)

where $m_m$ is the amplitude modulation ratio, $m_f$ is the frequency modulation ratio; $\alpha$ is the fundamental angular frequency; $\phi_m$ is the phase angle of the fundamental wave; $\phi_m$ is the phase angle of the carrier wave harmonic and $m$ order harmonics of the carrier wave harmonics; $\phi_m$ is the phase angle of their corresponding upper and lower side band harmonics. Using HPWM, the ground current will not be suppressed very well due to the sideband harmonics of the fundamental component. UPWM is chosen for the following analysis.

2.3. Ground current analysis

Figure 4 shows the harmonic spectrum of the ground current $i_{in1}$ for FB inverter with UPWM, where $h$ is the harmonic order, $i_{inhm}$ is the amplitude of $h$th order harmonic. In this study, the parameters of the PV systems are listed as follows.

System power $P=3.6$ kW,
PV array output voltage \( U_{pv} = 360 \text{ V} \),
Amplitude modulation ratio \( m_a = 0.87 \),
Frequency modulation ratio \( m_f = 400 \),
Switching frequency \( f_s = 20 \text{ kHz} \),
Output filter inductor \( L_1 = L_2 = L = 0.86 \text{ mH} \),
Grounding impedance \( Z_g = 0.5 \Omega \),
Parasitic capacitor \( C_{pv1} = C_{pv2} = C_{pv}/2 = 0.3 \mu \text{ F} \),
Output filter capacitor \( C_1' = C_2' = C'/2 = 50 \mu \text{ F} \).

The calculation results of the FB inverter without output filter capacitors are shown in Figure 4(a).

It is seen that the amplitude of ground current is high. The switching frequency harmonic has been significantly reduced with the output capacitors in Figure 4(b).

Figure 4 Harmonic spectrum of \( i_{N1} \) for FB inverter

Figure 5 shows the ground current rms value \( I_{N1\text{rms}} \) decreases with the increase of the output filter capacitors \( C \) using UPWM. The expression of ground current rms value is 

\[
I_{N1\text{rms}} = \sqrt{\sum_{n=1}^{\infty} (I_{n\text{rms}})^2}
\]

with the harmonics above 50 kHz ignored. It can be seen that when the capacitor \( C \) is larger than \( 11 \mu \text{ F} \), the ground current rms value will be smaller than \( 0.3 \text{ A} \) even when the voltage \( U_{pv} \) has a high value of \( 550 \text{ V} \).

Figure 5 \( i_{N1\text{rms}} \) varies with output filter capacitors

Therefore, UPWM is suitable to the PV system with the neutral-point-clamped capacitors.

2.4. Design of output filter capacitor

Figure 6(a) shows the relationship between the amplitude-frequency characteristic of \( H(s) \) and the output filter capacitor \( C' \), where the parasitic capacitor \( C_{pv} = 0.6 \mu \text{ F} \), and the output filter inductor \( L = 0.86 \text{ mH} \). The transfer function is defined as:

\[
H(s) = \frac{G}{(sL/2)(sL/2 + sC' + 1)} = \frac{sC_{pv}}{sL/2 + s(C_{pv} + C'C/L + 1)}
\]

(6)

From Figure 6(a), a larger value of the output filter capacitor will result in a larger value of the impedance at the switching frequency. Thus, the switching frequency component will be suppressed better. However, the resonant frequency will be closer to the fundamental frequency. The equation of the resonant frequency can be derived as
The relationship between the common-mode loop’s resonant frequency $f_r$ and the output filter capacitor $C'$ is shown in Figure 6(b). The resonant frequency decreases as the output filter capacitor $C'$ increases. When $C'$ is larger than 2.5 mF, the resonant frequency will be smaller than 150 Hz. And when $C'$ is larger than 0.23 mF, the resonant frequency will be smaller than 500 Hz.

\[
f_r \approx \frac{1}{2\pi} \sqrt{\frac{1}{(C_p + C')L/2}}
\]  

(7)

3. Efficiency estimation

Figure 7 shows the efficiency estimation and loss breakdown of FB inverter with UPWM, and H5 topology. In order to limit the ground current rms value to 300 mA, the output filter capacitor should be larger than 11 μF. In order to reduce the impact of the grid voltage on the ground current, the output filter capacitor should be smaller than 230 μF. Therefore, the range of the output filter capacitor is (11 μF, 230 μF).

![Amplitude-frequency characteristic of H(s)](a) Amplitude-frequency characteristic of H(s)

![Resonant frequency of the common-mode loop](b) Resonant frequency of the common-mode loop

In order to limit the ground current rms value to 300 mA, the output filter capacitor should be larger than 11 μF. In order to reduce the impact of the grid voltage on the ground current, the output filter capacitor should be smaller than 230 μF. Therefore, the range of the output filter capacitor is (11 μF, 230 μF).

![Efficiency estimation of different topologies](a) Efficiency estimation

![Loss breakdown when P=3.65 kW](b) Loss breakdown when P=3.65 kW

Figure 7 Efficiency estimation and loss breakdown of different topologies

It can be seen that the efficiency of FB inverter with UPWM is higher than that of H5. The switch loss and the inductor loss is almost the same due to the reduced switch frequency of FB inverter with UPWM. H5 has higher conduction loss due to the conduction of three power devices when the output voltage $u_{AB}$ ≠ 0.

The FB inverter with the output filter capacitor modulated by UPWM has high efficiency. And it does not need additional power device to suppress the ground current.

4. Simulation and Experimental Results

The simulation is implemented in Matlab/Simulink. Figure 8 shows the simulation results of full-bridge inverter with and without the output filter capacitors. The waveforms are the grid voltage $u_g$, the grid current $i_g$ and the ground current $i_N$. And the comparison of the simulation and calculation
results is also presented. The output filter capacitor is $C_1=C_2=5.5 \ \mu F$. It can be seen that the simulation and calculation results are nearly the same. The ground current has been significantly reduced with the output filter capacitors.

![Figure 8 Simulation results of FB inverter with and without the output filter](image)

**Figure 8** Simulation results of FB inverter with and without the output filter using UPWM

An experimental platform is built to test the proposed ground current suppression method. The grid voltage is 220 V with a frequency of 50 Hz. The dc-link voltage source is provided by a three-phase rectifier bridge. The parasitic capacitor of the PV array is simulated by the capacitors $C_{pv1}=C_{pv2}=0.22 \ \mu F$. The power inverter parameters are as follows, the dc-link voltage $U_{pv}=400 \ \text{V}$, the output filter inductor is $L_1=L_2=5 \ \text{mH}$, the switching frequency $f_s=10 \ \text{kHz}$.

![Figure 9 Waveforms with UPWM](image)

**Figure 9** Waveforms with UPWM

Figure 9 is the waveforms of the full-bridge inverter using UPWM, where the waveforms are the grid voltage $u_g$, the grid current $i_g$ and the ground current $i_N$. Figure 9(a) is the waveforms without the output filter capacitors. Figure 9(b) are the waveforms with the neutral-point-clamped capacitors $C_1=C_2=8 \ \mu F$. It can be seen that with the capacitor, the ground current has been significantly suppressed.

### 5. Conclusion

This paper proposed a novel ground current suppression for full-bridge inverter, using the output filter capacitors. The suppression effect is analyzed using different modulation methods. The efficiency estimation is done. The proposed topology has high efficiency without the additional power devices. The validity of the proposed method is verified by simulation results from the prototype. Unipolar modulation proves to be more suitable for the proposed method.

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