Filter-Clamped Two-Level Three-Phase Transformerless Grid-Connected Photovoltaic Inverter for Leakage Current Reduction

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Abstract—Transformerless Photovoltaic (PV) grid-connected systems benefit from improved cost, size, weight, and efficiency compared to the isolated alternatives. A drawback of the transformerless PV inverters is the leakage current that flows through the parasitic capacitance formed between the PV cells and panel metal frame connected to the earth. The leakage current increases the current harmonics injected into the utility grid, the radiated and conducted electromagnetic interference (EMI), and losses. In this paper, a two-stage three-phase Filter-Clamped (FC) transformerless PV system is employed that reduces the leakage current and output current THD compared to the conventional three-phase inverters. Unlike other transformerless PV inverters, the FC inverter does not require any additional component. The FC transformerless PV inverter is analyzed mathematically and its excellence is compared to the conventional three-phase inverter through simulation results.

Keywords—Photovoltaic (PV) systems, grid-connected inverter, transformerless inverter, common mode voltage, leakage current.

I. INTRODUCTION

In recent years, renewable energy resources have grown dramatically due to environmental pollution and shortage of fossil fuels. Among renewable energy resources, photovoltaic (PV) systems are popular due to unique characteristics including scalability and generation time [1-3]. Power converters optimize the PV energy and can deliver it to standalone loads and the grid. The efficiency of the PV converters is mandatory to benefit the most from the investment in the PV plant. In addition, the power converter system must be cost-effective, reliable, secure, and long lasting [4, 5]. Earlier generations of the PV grid-connected inverter were isolated by transformer. Galvanic isolation was achieved by either high-frequency or line-frequency transformers. The high-frequency isolated topologies include several power converter stages, which reduces the system efficiency and increases the cost. Line-frequency isolated transformers are bulky; it makes the PV inverter large and heavy, which is difficult to carry and install. In comparison, Transformer-less (TL) PV grid-connected systems benefit from improved size, cost, weight, and efficiency [6-14]. Additionally, three-phase inverters will not suffer from double-line-frequency ripples at the dc-link and thus smaller capacitive filters will be sufficient to maintain the voltage in the dc-link [15-18], making the entire system more reliable [19]. An adaptive control design approach is proposed in [20, 21] to regulate the dc side of the photovoltaic inverter by controlling the dc-dc converter connecting the photovoltaic to the inverter.

In TLPV inverters, the leakage current can flow through a conductive connection between the parasitic capacitance of the PV panels and the grid [22]. This parasitic capacitance can have a value of 60–110 nF/kW for modules with crystalline silicon cells (monocrystalline, polycrystalline); and up to 100-160 nF for modules with thin-film cells. Parasitic capacitance depends on the surface of the cells, the distance between cells, panel and frame structure, and atmospheric conditions. Leakage current appears through the parasitic capacitance formed between PV array and the earth plane [23]. The leakage current is superimposed to the line current; therefore, the harmonic content is increased compared with inverters with the transformer. Also, the leakage current can cause electromagnetic interferences (EMI) and additional losses in the system. The amplitude of the leakage current depends on the converter topology and the modulation scheme. According to the VDE 0126-01-01 standard, the RMS value of the leakage current has to be limited below 300 mA [8, 24-28].

Minimizing the leakage current and improving the efficiency in TL PV inverters have been widely investigated in earlier works. In H7 topology [29], using specific pulse width modulation (PWM) techniques, the PV panels are disconnected from the grid on dc side of the inverter to reduce the leakage current. In [30], the middle point of the dc-link is connected to neutral point of the grid. This method has been applied to neutral point clamped and full bridge topologies. This approach is not possible for three-phase three-wire grid where the neutral point is not available. A full-bridge three-phase zero voltage rectifier has been proposed in [31]. In [25], a Z-Source Inverter with an additional fast-recovery diode is introduced along with a specific modulation method to reduce leakage current. Additionally, reduced common mode voltage PWM methods have been proposed to reduce the leakage current [29, 32-35]. In these methods, the bipolar output line
to line voltage generates overvoltage transients, large current ripples across the filter inductors, and high switching losses that reduces the efficiency of the system. In [36], a new space-vector modulation was proposed to reduce leakage current for three-phase T-type inverters. In [37], a new modulation strategy was proposed to eliminate the leakage current in three-phase TL four-leg inverter. In [38], a modified full-bridge single-phase inverter was presented to suppress the leakage current by using the common-mode choke combined with the output LCL filter and the common-mode choke neutral point is connected to the dc-link midpoint. In [39], an improved full-bridge three-phase inverter with modified LC filter was proposed to reduce the leakage current in a 50 kW transformer-less inverter; where the output LC neutral is connected to the dc bus midpoint.

This paper employs a Filter Clamped Inverter (FCI) for TL PV grid-connected systems. FCI is utilized to address the leakage current issue and improve the performance of three-phase grid-connected inverters. In this topology, the output filter of the inverter is clamped to the midpoint of the dc link. This topology reduces the leakage current and improves the output current THD without modification in either modulation method or topology.

II. LEAKAGE CURRENT IN FULL BRIDGE AND FILTER CLAMPED GRID CONNECTED INVERTERS

A three-phase grid-connected TLPV system using FB inverter is shown in Fig. 1. The PV array parasitic capacitor is indicated with \( C_{PE} \). The leakage current appears through \( C_{PE} \) that is formed between the PV array and the earth plane. The popular LCL filter is used to interface the PV inverter and the grid.

![Fig. 1. Three-phase TL grid-connected PV system using FB inverter.](image)

The common mode model of Fig. 1 is shown in Fig. 2; where, \( V_{PE} \) is parasitic capacitor voltage and \( I_{leakage} \) is the leakage current. It should be noted that \( V_{aN}, V_{bN}, \) and \( V_{cN} \) are the voltages between the inverter outputs and the negative terminal of the PV array and \( V_{a,g}, V_{b,g}, \) and \( V_{c,g} \) are the voltages of three-phase grid.

![Fig. 2. Common mode model for three-phase TL grid-connected PV system using FB inverter.](image)

In the following, the leakage current phenomenon is analyzed by applying Kirchhoff laws to the common mode model shown in Fig. 2.

\[
V_{PE} = -V_{aN} + sL_{a,g}I_{a,g} + L_{a,g}I_{a,g}(0) + sL_{a,g}I_{a,g} + L_{a,g}I_{a,g}(0) + V_{a,g} \\
V_{PE} = -V_{bN} + sL_{b,g}I_{b,g} + L_{b,g}I_{b,g}(0) + sL_{b,g}I_{b,g} + L_{b,g}I_{b,g}(0) + V_{b,g} \\
V_{PE} = -V_{cN} + sL_{c,g}I_{c,g} + L_{c,g}I_{c,g}(0) + sL_{c,g}I_{c,g} + L_{c,g}I_{c,g}(0) + V_{c,g} \\
I_{a,g} = I_{a,f} + I_{a,g} \\
I_{b,g} = I_{b,f} + I_{b,g} \\
I_{c,g} = I_{c,f} + I_{c,g} \\
I_{Leakage} = -(I_{a,g} + I_{b,g} + I_{c,g}) \\
I_{a,f} + I_{b,f} + I_{c,f} = 0
\]

On the other hand, the common mode voltage is defined as:

\[
V_{CM} = \frac{V_{aN} + V_{bN} + V_{cN}}{3}
\]

In a balanced system, the following conditions are established:

\[
V_{a,g} + V_{b,g} + V_{c,g} = 0 \\
L_{a,c} = L_{b,c} = L_{c,c} = L_c \\
L_{a,g} = L_{b,g} = L_{c,g} = L_g
\]

The leakage current flowing through PV array parasitic capacitor is as:

\[
I_{Leakage}(t) = C_{PE} \frac{dV_{PE}(t)}{dt}
\]

\[
I_{Leakage} = sC_{PE}V_{PE} + C_{PE}V_{PE}(0)
\]

By using (1) to (11), the parasitic capacitor voltage of \( V_{PE} \) can be obtained as:

\[
V_{PE} = -\frac{3}{3 + s^2C_{PE}(L_c + L_g)}V_{CM} \\
+ \frac{1}{3 + s^2C_{PE}(L_c + L_g)} \left[ -sC_{PE}(L_c + L_g)V_{PE}(0) + \right. \\
+ \left. L_c(I_{a,g}(0) + I_{b,g}(0) + I_{c,g}(0)) + \right. \\
+ \left. L_g(I_{a,g}(0) + I_{b,g}(0) + I_{c,g}(0)) \right]
\]

In the above equations, \( L_{a,c}, L_{b,c}, \) and \( L_{c,c} \) are the inverter side inductances; these inductances are equal to \( L_c, L_{a,g}, L_{b,g}, \) and \( L_{c,g} \) are the grid side inductances; these inductances are equal to \( L_g, I_{a,g}(0), I_{b,g}(0), \) and \( I_{c,g}(0) \) are the initial currents of the inverter side inductors and \( L_{a,g}(0), I_{b,g}(0), \) and \( I_{c,g}(0) \) are the initial currents of the grid side inductors. \( V_{PE}(0) \) is the initial voltage of the parasitic capacitance.

A sinusoidal PWM (SPWM) strategy is applied to the FB inverter. Fig. 3 shows SPWM method. Where \( V_a^*, V_b^*, \) and \( V_c^* \) are sinusoidal voltage references generated by the closed loop control system. The PWM carrier is a triangular waveform where its frequency is switching frequency; \( g1 \) to \( g6 \) are the gate pulses for the switches S1 to S6. In each leg of the FB inverter, the gate commands of the upper switch and lower switch are complementary. There are eight switching states in the SPWM method for FB inverter. The CMV value
in these eight switching states is shown in Table I, where \( V_{dc} \) is the dc-link voltage. According to Table I, CMV changes in different switching states.

From (11), it can be observed that the leakage current depends on both the parasitic capacitance of \( C_{PE} \) and derivative of \( V_{PE} \). Thus, the leakage current flows because of the variations in the parasitic capacitor voltage. On the other hand, from (12), \( V_{PE} \) is dependent on the CMV and initial conditions of LCL filter inductors and the parasitic capacitor structure. The initial conditions of the LCL filter inductors and parasitic capacitor do not change in steady state; so their effect on the \( V_{PE} \) can be neglected. Thus, the variations in CMV cause variations in parasitic capacitance voltage. These variations in parasitic capacitance voltage result in leakage current flowing through the \( C_{PE} \) between PV array and ground. Therefore, the variations of CMV need to be reduced in order to reduce the leakage current.

![Fig. 3. SPWM method.](image)

**TABLE I. Common Mode Voltage values for FB**

| Upper Switching States | Common Mode Voltage in FB |
|------------------------|---------------------------|
| 000                    | 0                         |
| 100, 010, 001          | \( \frac{1}{3} V_{dc} \) |
| 110, 101, 011          | \( \frac{2}{3} V_{dc} \) |
| 111                    | \( V_{dc} \)              |

In contrast, in the FCI, as shown in Fig. 4, the \( V_{PE} \) is not dependent on the CMV. The FC inverter is analyzed below.

In the FCI, the output LCL filter of the inverter is clamped to the midpoint of the dc-link as shown in Fig. 4. The common mode model for the grid-connected three-phase PV systems using FC inverter is shown in Fig. 5.

Below, the leakage current in FC inverter is analyzed by applying Kirchhoff laws to the common mode as shown in Fig. 5.

\[
\begin{align*}
V_{PE} &= -\frac{V_{dc}}{2} - V_{a,f} + sL_{a,g}I_{a,g} + L_{a,g}I_{a,g}(0) + V_{a,g} \\
V_{PE} &= -\frac{V_{dc}}{2} - V_{b,f} + sL_{b,g}I_{b,g} + L_{b,g}I_{b,g}(0) + V_{b,g} \\
V_{PE} &= -\frac{V_{dc}}{2} - V_{c,f} + sL_{c,g}I_{c,g} + L_{c,g}I_{c,g}(0) + V_{c,g} \\
\end{align*}
\]

(13) to (15) as follows:

\[
V_{PE} = -\frac{3}{2} V_{dc} + (V_{a,f} + V_{b,f} + V_{c,f})
\]

\[
\begin{align*}
&- 3s^2C_{PE}L_s \\
&+ \frac{1}{3 + s^2C_{PE}L_s} \left( -sL_sC_{PE}V_{PE}(0) + s^2L_sC_{PE}L_sI_{a,g}(0) + I_{a,g}(0) + I_{b,g}(0) + I_{c,g}(0) \right)
\end{align*}
\]

Similar to the FB inverter, unipolar SPWM modulation is applied to FCI; there are eight switching states; also, CMV has four values \( V_{dc}/3, 2V_{dc}/3, \) and \( V_{dc} \). From (16), it is observed that \( V_{PE} \) is dependent on the dc-link voltage, voltage of Resistive-Capacitive (RC) branches of LCL filter, and the initial conditions of LCL filter inductors and parasitic capacitor. Unlike the traditional three phase inverter, which is modeled in (12), \( V_{PE} \) is independent of the CMV, and, thereby, the variations in CMV do not produce transient voltage across the parasitic capacitance.

![Fig. 5. Common mode model for three-phase TL grid-connected PV system using FC topology.](image)

In the FCI, since the RC branches of LCL filter are connected to the inverter and the grid through the inductor, pulse-form currents cannot flow through these RC branches. Consequently, RC branch voltages are continuous and do not have sudden transients. Hence, the sum of three voltages \( V_{a,f}, V_{b,f}, \) and \( V_{c,f} \) is a continuous voltage with zero average; this fact is also shown by simulation in Fig. 6 which shows the voltages of the RC branches of the LCL filter. As shown in Fig. 6 (a), the shape of these voltages is sinusoidal with 50 Hz frequency. The sum of three voltages \( V_{a,f}, V_{b,f}, \) and \( V_{c,f} \) is a continuous voltage with zero average as shown in Fig. 6 (b). Consequently, the sum of these three voltages is independent of the CMV.

Also, \( V_{dc} \) is a constant voltage with small ripples. The initial conditions of the LCL filter inductors and parasitic capacitor do not change in steady state; so their effect on the \( V_{PE} \) can be neglected. As a result, \( V_{PE} \) has a constant dc bias with a small ripple. As a conclusion, due to small variations of the \( V_{PE} \), the leakage current is significantly reduced in the FCI.
A simulation testbed is developed in the MATLAB/SIMULINK platform in order to verify the FCI
configuration. The system includes two stages, boost converter and inverter which are interconnected through a dc-link capacitor. The boost stage operates as the Maximum Power Point Tracker (MPPT). The well-known perturb and observe controller is adopted for the MPPT.

The control structure consists of two parts, which can operate independently decoupled by the dc-link capacitor. The dc-link voltage is regulated at 696 V through a closed loop Proportional-Integral (PI) controller. The output of the PI controller generates the required instantaneous active power reference. The three-phase output currents and grid voltages are transformed into the stationary reference frame, which is the αβ-frame. The current references are derived from the grid voltages, and active and reactive power references through (17) and (18).

\[
\begin{align*}
    i_\alpha^* & = \frac{1}{V_\alpha^2 + V_\beta^2} (V_\alpha P^* + V_\beta Q^*) \\
    i_\beta^* & = \frac{1}{V_\alpha^2 + V_\beta^2} (V_\alpha P^* - V_\beta Q^*)
\end{align*}
\]

The current controller block includes two Proportional-Resonant (PR) controllers that separately control the injected currents according to the provided active and reactive power references. In addition, in order to compensate 5-th and 7-th order harmonics from the injected currents, two extra PR controllers are implemented at 250 Hz, (5×50), and 350 Hz, (7×50).

In order to do simulation, two case studies are provided to verify the advantages of the FCI topology, which are the leakage current reduction and the improvement of the output current THD. The case studies are performed with closed loop controls. Fig. 8 (a) and Fig. 9 (a) show \( V_{ab} \), which is the output line-to-line voltage for FB and FC inverters, respectively. \( V_{ab} \) is measured at the inverter side prior the filter. The voltages are identical; the output voltage amplitude is 696 V for both topologies. The output current injected to the grid is shown in Fig. 8 (b) for FB inverter and Fig. 9 (b) for FCI. The output current THD is 4.5 % and 1.8 % for FB and FC inverters, respectively. The output current THD is lower in the FCI compared to the FB according to the simulation results.

Fig. 10 (a) and Fig. 11 (a) show the parasitic capacitor voltage of \( V_{PE} \) for FB and FC inverters, respectively. In the FB inverter, \( V_{PE} \) varies; in contrast, in the FC inverter \( V_{PE} \) is relatively constant. As a result, a non-zero leakage current flows in the FB topology such as shown in Fig. 10 (b); the leakage current RMS value is 406 mA for FB topology; this violates VDE 0126-1-1 limits, where, it is stated that the maximum level for RMS value of the leakage current should be limited to 300 mA. Fig. 11 (b) shows the simulation result of the leakage current for FC topology. In the FC inverter the leakage current is measured as 4 mA, which is much lower than the 300 mA limit. Therefore, the leakage current characteristics in the FC topology fulfills the requirements set by the standard VDE 0126-1-1. The simulation results validate the analysis presented in section II.
Consequently, the output current THD is reduced in FCI owing to the leakage current reduction. Therefore, FCI offers lower leakage current and lower harmonic contents injected to the grid.

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