Warpage of QFN Package in Post Mold Cure Process of integrated circuit packaging

Nattha Sriwithoon1*, Kessararat Ugsornrat1, Warayoot Sirisuwitthanon2, and Panakamon Thonglor1

1Department of Industrial Physics and Medical Instrumentation, Faculty of Applied Science, King Mongkut’s University Technology North Bangkok, Bangkok, 10800, Thailand

2Stars microelectronics (Thailand) public company limited, Bang Pa-In Industrial Estate (I-EA-T Free Zone) 605-606 Moo 2, Klongjig, Bang Pa-In Ayutthaya 13160, Thailand

*Email: Sr.Nattha@gmail.com

Abstract. This research studied about warpage of QFN package in post mold cure process of integrated circuit (IC) packages using pre-plated (PPF) leadframe. For IC package, epoxy molding compound (EMC) are molded by cross linking of compound stiffness but incomplete crosslinked network and leading the fully cured thermoset by post mold cure (PMC) process. The cure temperature of PMC can change microstructure of EMC in term of stress inside the package and effect to warpage of the package due to coefficient of thermal expansion (CTE) between EMC and leadframe. In experiment, cure temperatures were varied to check the effect of internal stress due to different cure temperature after completed post mold cure for TDFN 2×3 8L. The cure temperature were varied with 180 °C, 170 °C, 160 °C, and 150°C with cure time 4 and 6 hours, respectively. For analysis, the TDFN 2×3 8L packages were analyzed the warpage by thickness gauge and scanning acoustic microscope (SAM) after take the test samples out from the oven cure. The results confirmed that effect of different CTE between EMC and leadframe due to different cure temperature resulting to warpage of the TDFN 2×3 8L packages.

Keywords: Integrated circuit (IC) packaging, post mold cure process, epoxy molding compound (EMC), warpage of QFN package, the coefficient of thermal expansion (CTE), cure temperature

1. Introduction

Molding is the important process of integrated circuit (IC) packaging for protection the die inside IC package. The encapsulation of chip or die using a transfer epoxy molding compound (EMC) by cross linking of compound stiffness but incomplete crosslinked network and leading the fully cured thermoset by post mold
cure (PMC) process. Post mold cure (PMC) is one of the most significant processes in electrical industry. This process exposes part of a mold to elevated temperatures in order to speed up the curing process and to optimize some physical properties of the material. The total stress in the packages can be occurred from curing which depends on the chemistry of the compound and thermal mismatch between various materials.

EMC is a plastic polymer that features a sturdy structure can change the temperature of the environment and it is highly flexible. A thermosetting resin is a prepolymer in a soft solid or viscous liquid state that changes irreversibly into an infusible, insoluble polymer network by curing. Curing is induced by the action of heat or suitable radiation often under high pressure, or by mixing with a catalyst or crosslinking agent often under atmospheric conditions at ambient temperature. Epoxy molding compound (EMC) is a common material used in IC packaging. One of its defects is warpage. Warpage could be a serious issue for some IC encapsulation processes. The cure temperature of PMC can change microstructure of EMC in turn of stress inside the package. Temperature is a factor effect to EMC base on the coefficient of thermal expansion (CTE). Effect of differences CTE between EMC and leadframes resulting to warpage of the packaging of integrated circuits.

Therefore, this research interested in the effects of post mold cure temperature from packages were studied for TDFN 2×3 8L, EMC and PPF leadframes. The cure temperature were varied to check the effect of internal stress due to temperature. Analyzed of the warpage of the package by thickness gauge and reliability test inside the packages by scanning acoustic microscope after take the test samples out from the oven cure. To demonstrate the efficiency of the packaging did not change to the original feature and can also help reduce the amount of time at ramp down temperatures until room temperatures (25°C) so increase productivity. Finally, we conclude this paper.

2. Methodology

This section, we describe the methodology of the studying about warpage of QFN package in post mold cure process of using pre-plated (PPF) leadframe. The experiment starts from selecting EMC was used with TDFN 2×3 8L package. In experiment, the cure temperature were varied to check the effect of internal stress due to temperature. Experiment parameter of the cure temperature were varied form 180,170,160 and 150°C and cure time were varied form 4 and 6 hrs, respectively. Moreover, the general process of IC packaging manufacturing is shown as Figure 1. And analyzed of the warpage of the package by thickness gauge and reliability test inside the packages by scanning acoustic microscope (SAM). The diagram of experiment as shown in Figure 2.

![Figure 1. The general process of IC packaging manufacturing.](image-url)
3. Results and Discussion

The thermal stress can be generated by coefficient of thermal expansion mismatch between over-molded EMC, silicon chip, substrates, and various materials in the packages due to unbalanced from a thermomechanical stress standpoint which leads to bowing upon cooling from the cure process temperature to room temperature (25°C) effect to warpage the package. The results of warpage between before and after PMC of PMC temperature at 180, 170, 160 and 150°C, PMC time at 4 is shown as Figure 3 and PMC time at 6 hrs. is shown as Figure 4.

![Figure 3. Warpage results of EMC and various materials for TDFN 2x3 8L package between before and after PMC of PMC temperature at 180, 170, 160 and 150°C, PMC time at 4 hrs.](image-url)
Figure 4. Warpage results of EMC and various materials for TDFN 2×3 8L package between before and after PMC of PMC temperature at 180, 170, 160, and 150°C, PMC time at 6 hrs.

From Figure 3 and 4 shown the results of warpage of EMC and various materials for TDFN 2×3 8L package. The results reveal that no warpage on these areas before and after PMC which 150°C cure temperature and time at 4 hrs. cannot found the points of delamination more than lower cure temperature on the packages. Moreover, the lower cure temperature on the packages can reduce production costs and help reduce the amount of time at ramp down temperatures until room temperatures (25°C) so increase productivity.

The results of delamination by C-SAM after post mold cure (PMC) in 150°C cure temperature and time at 4 hrs of TDFN 2×3 8L as shown in Table 1. The results of help reduce the amount of time at ramp down temperatures as shown in Figure 5, respectively.

Table 1 Delamination results for Post Mold Cure (PMC) in 150°C cure temperature and time at 4 hrs. of TDFN 2×3 8L.

| Delamination | PMC Temp (°C) | 150  | 160  | 170  | 180  |
|--------------|--------------|------|------|------|------|
| Result (units) | 0/1,620      | 0/1,620 | 0/1,620 | 0/1,620 | 0/1,620 |
| 4 hr.        |              |      |      |      |      |
| C-SAM Top view |            |      |      |      |      |
| Bottom view  |              |      |      |      |      |
| 6 hr.        |              |      |      |      |      |
| C-SAM Top view |            |      |      |      |      |
| Bottom view  |              |      |      |      |      |
4. Conclusion

This research studied the effect of cure temperature on the warpage of TDFN 2×3 8L package in the post mold cure process of integrated circuit packaging. The results revealed that no warpage occurred on these areas before and after the process, which had a cure temperature of 150°C and a time of 4 hours. The opposite way, the results show no delamination points on the packages. Moreover, the results showed that reducing production costs and helping to reduce the amount of time at ramp down temperatures until room temperatures (25°C) can increase productivity. Therefore, the results confirmed that the study of warpage of QFN packages in the post mold cure process can be used for information in the IC packaging manufacturing.

5. References

[1] Guohua Gao, Honghui Wang and Guoji Yang “A New Method for The Investigation of Strip Warpage of MAP-QFN” Electronic Packaging Technology & High Density Packaging, 2008. ICEPT-HDP 2008. International Conference on Electronic Packaging Technology & High Density Packaging. (July 2008) 486-493

[2] J. de Vreugd, K.M.B. Jansen, A. Xiao, L.J. Ernst, C. Bohm, A. Kessler, H. Preu and M. Stecher “Advanced viscoelastic material model for predicting warpage of a QFN panel” Electronic...
Components and Technology Conference, 2008. ECTC 2008. 58th Electronic Components and Technology Conference, 2008. ECTC 2008. 58th. (May 2008)

[3] Belton D.J. “The Effect of Post-Mold Curling Upon the Microstructure of Epoxy Molding Compounds” IEEE Transactions on Components, Hybrids, and Manufacturing Technology. 10(3)(Sep 1987)

[4] Narasimalu S. “Warpage analysis of epoxy molded packages using viscoelastic based model” Journal of Material Science. 41(12) (June 2006) : 3773-3780

[5] Alpern P. and Lee K.C. “Moisture-Induced Delamination in Plastic Encapsulated Microelectronic Devices : A Physics of Failure Approach” IEEE Transactions on devices and materials reliability. 8(3)(September 2008) : 478-483

[6] Lee C.H., Lin L.F., Ho T.H. and Cheng S.S. “Study on paddle delamination for quad flat no leads package” Department of Chemical and Materials Engineering, National Kaohsiung University of Applied Sciences. (March 2003) : 1-8

[7] Tsai M.Y., Wang C.T. and Hsu C.H. “The Effect of Epoxy Molding Compound on Thermal/Residual Deformations and Stresses in IC Package During Manufacturing Process” IEEE Transactions on components and packaging Technology. 29(3) (September 2006) : 625-635

Acknowledgment

This research was supported by Stars microelectronics (Thailand) public company limited and King Mongkut's University of Technology North Bangkok.