Paper

Sigma-delta domain bandpass and band-elimination wave filters

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Abstract: This paper presents sigma-delta (SD) domain bandpass and band-elimination wave filters modeled after analog distributed parameter filters (ADPF) built up of coupled transmission lines. The bandpass and band-elimination filters have the following advantages: (i) Design techniques of ADPFs can be applied directly and (ii) shift registers and sorting networks both of which are spatially uniform in structure and local in internal connections are the main parts of the SD domain filters. We designed an SD domain bandpass filter and confirmed by computer simulation that it possessed the same frequency response characteristics with the theoretical characteristics of the reference ADPF. We also designed a band-elimination filter from which coefficient multipliers were removed and for which shift registers of different lengths were employed to simplify further the filter structure. Finally, we investigate the fault-tolerant capability of a bandpass block for transient errors of internal circuit cells. With the help of computer simulation, we found that the bandpass block did not fail in operation and did not output high surge noise in the presence of the errors although its output quality decreased.

Key Words: digital filter, distributed parameter filter, sigma-delta modulation, bandpass filter, band-elimination filter

1. Introduction
High-performance devices and circuits that exploit quantum mechanical phenomena have been invented [1]. Their characteristics are discontinuous because of the wave nature of the electrons [2]. The discontinuous quantum phenomena make construction of nanometer-scale analog circuits impossible. In addition, the devices and the circuits are vulnerable to elektromagnetic interference, atmospheric neutrons, and other physical attacks to cause transient errors [3-5].

Fault-tolerant architectures have long been researched [3-6]. Well-known fault tolerant techniques include hardware and information redundancies. State-of-the-art techniques are error corrections based on artificial intelligence and probability theories. In addition, stochastic computing is getting attention in recent years as a measure of fault tolerance because of the simplicity of signals and hardware [7, 8]. The signals are in the form of dichotomous Bernoulli sequences.
Sigma-delta domain signal processing (SDSP) is a scheme that allows quantum effect circuits to inherit analog circuit design properties and acquire tolerance of transient device errors [9]. The inheritance makes it possible to construct a wide range of SDSP circuit library including four arithmetic circuits [9–12], algebraic and transcendental function circuits [9, 12, 13], and piecewise linear circuits [14]. All of inputs, outputs, and internal signals of SDSP circuits are in sigma-delta (SD) modulated bit-stream form [15, 16]. Since SDSP circuits consist of modules each of which repeats simple task synchronously with a clock, the circuits have no operation sequence controller. The fault tolerance is due to the signal form and the circuit architecture.

Digital filters employing SD modulated signal form have been developed [10, 17–21]. However, they employ fault-intolerant long word-length multi-bit signal forms partially for internal signals. A full SD domain lowpass wave filter without such multi-bit signal form has been proposed recently [22]. Since the lowpass filter is a spatio-temporally discretized and two-level-quantized model of an analog distributed parameter filter (ADPF), it inherits the techniques for ADPF design [23–25]. The lowpass filter is built up mainly of two kinds of circuit modules, shift registers and binary sorting networks. Shift registers are lines of flip-flops or unit time delays. Binary sorting networks are built by arranging AND and OR gates regularly and connecting the gates locally. The spatial regularity and the local connections in the two modules are advantageous in the physical design of circuits built of quantum effect devices.

In this paper, we will design full sigma-delta domain bandpass and band-elimination filters. They are spatio-temporally discretized and two-level-quantized models of ADPFs constructed of coupled transmission lines while the SD domain lowpass filter is modeled after an ADPF built by connecting single transmission lines. In spite of the difference, the bandpass and band-elimination filters will also possess the three properties, inheritance of ADPF design techniques, tolerance of transient device errors, uniform structure with local connections.

The coupling between transmission lines is represented by weighted sum circuits in the bandpass and band-elimination filters. The main parts of the weighted sum circuits are binary sorting networks. As explained in [26], sorting networks are not linear circuits. We attempt to construct linear weighted sum circuits operating on sigma delta modulated signals in the filters with the binary sorting networks. The rest of the paper is organized as follows: In Section 2, wave propagation on coupled transmission lines is investigated. Weighted sum circuits are introduced in Section 3. Based on the results of the investigation and using the weighted sum circuits, we design SD domain bandpass and band-elimination filters in Sections 4 and 5. In Section 6, we evaluate the fault-tolerant capability of the block of the bandpass filter for transient device errors. In Section 7, we conclude the paper.

2. Coupled transmission lines

In this section, we will analyze coupled lossless transmission lines [23–25, 27] used for bandpass and band-elimination ADPFs. Figure 1(a) shows two lossless transmission lines TL1 and TL2 of characteristic impedance \( Z = \sqrt{L/C} \). They are inductively and capacitively coupled. We denote the mutual inductance and capacitance per unit length by \( L_M \) and \( C_M \), respectively. The voltage and current
waves propagating on the coupled transmission lines are described by

\[
\begin{align*}
\frac{\partial}{\partial x} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} &= - \begin{bmatrix} L & L_M \\ L_M & L \end{bmatrix} \frac{\partial}{\partial t} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \\
\frac{\partial}{\partial x} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} &= - \begin{bmatrix} C & -C_M \\ -C_M & C \end{bmatrix} \frac{\partial}{\partial t} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}
\end{align*}
\]

(1)

where \( x \) and \( t \) are independent spatial and temporal variables.

We define even and odd mode voltage and current waves \( v_e, v_o, i_e, \) and \( i_o \) as

\[
v_e = \frac{v_1 + v_2}{2}, \quad i_e = \frac{i_1 + i_2}{2}, \quad v_o = \frac{v_1 - v_2}{2}, \quad i_o = \frac{i_1 - i_2}{2}
\]

(2)

By this variable transformation, Eq. (1) is transformed into

\[
\begin{align*}
\frac{\partial v_e}{\partial x} &= -(L + L_M) \frac{\partial i_e}{\partial t}, \quad \frac{\partial i_e}{\partial x} = -(C - C_M) \frac{\partial v_e}{\partial t} \\
\frac{\partial v_o}{\partial x} &= -(L - L_M) \frac{\partial i_o}{\partial t}, \quad \frac{\partial i_o}{\partial x} = -(C + C_M) \frac{\partial v_o}{\partial t}
\end{align*}
\]

(3)

Equation set (3) implies that coupled lines, \( TL_1 \) and \( TL_2 \), are transformed to two independent transmission lines, \( TL_e \) and \( TL_o \), on which the even and odd mode waves propagate, as Fig. 1(b) shows. The characteristic impedance values of the independent lines are

\[
Z_e = \sqrt{\frac{L + L_M}{C - C_M}}, \quad Z_o = \sqrt{\frac{L - L_M}{C + C_M}}
\]

(4)

We assume here that \( TL_1 \) and \( TL_2 \) are coupled in a finite interval \([0, l]\). Forward and backward power waves on \( TL_{1/2} \) are defined outside the interval as

\[
w_{F,1/2} = \frac{v_{1/2}}{\sqrt{2}} + \sqrt{2} i_{1/2}, \quad w_{B,1/2} = \frac{v_{1/2}}{\sqrt{2}} - \sqrt{2} i_{1/2}
\]

(5)

Notations \( TL_{1/2} \), \( w_{F,1/2} \), \( w_{B,1/2} \), \( v_{1/2} \), and \( i_{1/2} \) respectively mean \( TL_s \), \( w_{F,s} \), \( w_{B,s} \), \( v_s \), and \( i_s \) with \( s \) being 1 or 2 in the above sentence and equations. Hereafter, similar notations will be used. Forward and backward power waves on \( TL_{e/o} \) are defined inside the interval similarly as

\[
w_{F,e/o} = \frac{v_{e/o}}{\sqrt{Z_{e/o}}}, \quad w_{B,e/o} = \frac{v_{e/o}}{\sqrt{Z_{e/o}}} - \sqrt{Z_{e/o}} i_{e/o}
\]

(6)

From Eqs. (2), (5), and (6), we derive the following relation between \( w_{F,B,1/2} \) and \( w_{F,B,e/o} \) at \( x = 0 \) and \( x = l \):}

\[
\begin{bmatrix} w_{F,e} \\ w_{B,e} \\ w_{F,o} \\ w_{B,o} \end{bmatrix} = K \begin{bmatrix} w_{F,1} \\ w_{B,1} \\ w_{F,2} \\ w_{B,2} \end{bmatrix}, \quad K = \frac{1}{4} \begin{bmatrix} k_{ze} + k_{ze}^{-1} & -k_{ze} + k_{ze}^{-1} & k_{ze} + k_{ze}^{-1} & -k_{ze} + k_{ze}^{-1} \\ -k_{ze} + k_{ze}^{-1} & k_{ze} + k_{ze}^{-1} & k_{ze} + k_{ze}^{-1} & -k_{ze} + k_{ze}^{-1} \\ k_{zo} + k_{zo}^{-1} & -k_{zo} + k_{zo}^{-1} & k_{zo} + k_{zo}^{-1} & -k_{zo} + k_{zo}^{-1} \\ -k_{zo} + k_{zo}^{-1} & k_{zo} + k_{zo}^{-1} & k_{zo} + k_{zo}^{-1} & -k_{zo} + k_{zo}^{-1} \end{bmatrix}
\]

(7)

Assume that the transmission lines are driven by a sinusoidal source of frequency \( \omega \). Although voltage, current, and power waves on the transmission lines are temporally periodic functions of frequency \( \omega \), we do not show it explicitly. Hereafter, we stress only that they are functions of location \( x \) and express them as \( v_\bullet(x) \), \( i_\bullet(x) \), and \( w_{F,B,\bullet}(x) \). \( \bullet \): 1, 2, e, or o. From Eqs. (3) and (6), ordinary differential equations of \( w_{F,B,e/o}(x) \) are derived. When wave conditions at \( x = 0 \) are given, we can express the solutions of the derived equations at \( x = l \) as
Then, Eq. (9) is simplified to
\[
\begin{bmatrix}
w_{F,c}(l) \\
w_{B,c}(l) \\
w_{F,o}(l) \\
w_{B,o}(l)
\end{bmatrix} = P
\begin{bmatrix}
w_{F,c}(0) \\
w_{B,c}(0) \\
w_{F,o}(0) \\
w_{B,o}(0)
\end{bmatrix}, \quad P = \begin{bmatrix}
\exp(-\gamma_c l) & 0 & 0 & 0 \\
0 & \exp(+\gamma_c l) & 0 & 0 \\
0 & 0 & \exp(-\gamma_o l) & 0 \\
0 & 0 & 0 & \exp(+\gamma_o l)
\end{bmatrix}, \quad (8)
\]

\[
\gamma_c = j\omega \sqrt{(L + L_M)(C - C_M)}, \\
\gamma_o = j\omega \sqrt{(L - L_M)(C + C_M)}
\]

From Eqs. (7) and (8), we obtain
\[
\begin{bmatrix}
w_{F,1}(l) \\
w_{B,1}(l) \\
w_{F,2}(l) \\
w_{B,2}(l)
\end{bmatrix} = K^{-1}PK
\begin{bmatrix}
w_{F,1}(0) \\
w_{B,1}(0) \\
w_{F,2}(0) \\
w_{B,2}(0)
\end{bmatrix}
\]

Assume that
\[
\frac{L_M}{L} = \frac{C_M}{C} = \epsilon \quad (10)
\]

In this case, we have
\[
\gamma_c = \gamma_o = \gamma, \quad \gamma = \sqrt{LC} \sqrt{(1 + \epsilon)(1 - \epsilon)} \quad (11)
\]

and
\[
Z = \sqrt{Z_c Z_o}, \quad Z_c \neq Z_o \quad (12)
\]

Then, the elements of \( K \) in Eq. (7) are given by
\[
k_{2c} = k_z^{-1}, \quad k_{2o} = k_z, \quad k_z = (Z_o/Z_c)^{1/2} \quad (13)
\]

We extract equations from Eq. (9) and express the equations using \( k_z \) and \( \gamma \) as follows:
\[
\begin{align*}
w_{F,1/2}(l) &= \frac{1}{4}(k_z + k_z^{-1}) \{ (k_z + k_z^{-1})w_{F,1/2}(0) + (k_z - k_z^{-1})w_{B,2/1}(0) \} \exp(-j\theta), \\
w_{B,1/2}(0) &= \frac{1}{4}(k_z + k_z^{-1}) \{ (k_z + k_z^{-1})w_{B,1/2}(l) + (k_z - k_z^{-1})w_{F,2/1}(l) \} \exp(-j\theta), \\
j\theta &= \gamma l
\end{align*} \quad (14)
\]

In case that
\[
Z = Z_c = Z_o, \quad \gamma_c \neq \gamma_o \quad (15)
\]

we have
\[
k_{2c} = k_{2o} = 1 \quad (16)
\]

Then, Eq. (9) is simplified to
\[
\begin{align*}
w_{F,1/2}(l) &= \frac{1}{2}\{w_{F,1/2}(0) + w_{F,2/1}(0)\} \exp(-j\theta_c) + \frac{1}{2}\{w_{F,1/2}(0) - w_{F,2/1}(0)\} \exp(-j\theta_o), \\
w_{B,1/2}(0) &= \frac{1}{2}\{w_{B,1/2}(l) + w_{B,2/1}(l)\} \exp(-j\theta_c) + \frac{1}{2}\{w_{B,1/2}(l) - w_{B,2/1}(l)\} \exp(-j\theta_o), \\
j\theta_c &= \gamma_c l, \quad j\theta_o = \gamma_o l
\end{align*} \quad (17)
\]

Suppose that the coupled lines in Fig. 1 are finite in length and the length is \( l \). Regarding the line pair as a four-port circuit, we derive its impedance \( (Z) \) matrix. For the matrices expressing multi-port circuits, see [23]. Even and odd mode voltages and currents at the left and the right terminals of TL\(_c\) and TL\(_o\) satisfy the following equations:
\[
\begin{bmatrix}
v_e(0) \\
v_e(l)
\end{bmatrix} = Z_c \begin{bmatrix}
i_e(0) \\
i_e(l)
\end{bmatrix}, \quad \begin{bmatrix}
v_o(0) \\
v_o(l)
\end{bmatrix} = Z_d \begin{bmatrix}
i_o(0) \\
i_o(l)
\end{bmatrix},
\]

\[
Z_{c/d} = Z(Z_{c/o}, \gamma_{c/o}), \quad Z(Z, \theta) = Z_c \begin{bmatrix}
\coth \theta & 1 \\
\frac{1}{\sinh \theta} & \coth \theta
\end{bmatrix}
\]

\[
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\]
From Eqs. (2) and (18), we obtain the following relation between the voltages and currents at the left and the right terminals of TL$_1$ and TL$_2$:

$$\begin{bmatrix} v_1(0) \\ v_1(l) \\ v_2(0) \\ v_2(l) \end{bmatrix} = Z \begin{bmatrix} i_1(0) \\ -i_1(l) \\ i_2(0) \\ -i_2(l) \end{bmatrix}, \quad Z = \begin{bmatrix} Z_c + Z_d & Z_c - Z_d \\ Z_c - Z_d & Z_c + Z_d \end{bmatrix}$$  

3. Sigma-delta domain weighted sum circuits

In this section, SD domain weighted sum circuits and coefficient multipliers are introduced. For more details, refer to [22].

Figure 2(a) shows a circuit weighting $B$ inputs and summing the weighted inputs. It consists of a binary sorting network and a parallel register. The binary sorting network is built of AND-OR gate pairs or linear threshold gates (LTG) as shown in Fig. 3(a) or (b) [12]. The input and the output signals, $x(n)^{(j)}$ and $y(n)$, are $(A + 1)$ and $(L + 1)$-level first-order SD modulated signals, respectively. They are represented by the sum of the binary signals as
The sorting network with feedback paths through the register functions as an integrator. Suppose that $A$ divides $L$. Extracting every $A/L$ bits from the register corresponds to quantization of the register content $u(n)$. The quantized signal is the output $y(n)$. Then, we find that the weighted sum circuit is designed based on a first-order digital SD modulator. The weighted sum operation of the circuit is expressed in the $z$-domain by the following equation:

$$Y(z) = \frac{1}{M} \sum_{j=1}^{B} N_j X^{(j)}(z) + \frac{1}{M} \frac{1}{1 - z^{-1}} E(z)$$

(21)

where $E(z)$ is the $z$-domain expression of the quantization error $e(n) = y(n) - u(n)$.

Figure 2(a) shows a circuit operating on second-order binary SD modulated inputs and outputting their weighted sum in the same signal form. Its operation is expressed by

$$Y(z) = \frac{1}{M} z^{-1} \sum_{j=1}^{B} N_j X^{(j)}(z) + \frac{1}{M} \frac{(1 - z^{-1})^2}{F(z)} E(z),$$

(22)

$$F(z) = \frac{1}{M} - \frac{2 - M_1 - M_2}{M_2} z^{-1} - \frac{M_1 - 1}{M_2} z^{-2}$$

(23)

in the $z$-domain.

The weighted sum circuits in Fig. 2 are referred to as adders when $N_1 = N_2 = \cdots = N_B$. The weighted sum circuits with single input, i.e., $B = 1$, are called coefficient multipliers.

Coefficient multipliers can be built also by cascading two-input adders as shown in Fig. 4. The adders are $(1/2)$-weighted sum circuits. Multiplicand $x(n)$ or zero-average signal is inputted to the adders. Let a set of the suffixes of the adders to which $x(n)$ is applied be denoted by $S_I$. Then, the multiplier or the coefficient $c$ is given by

$$c = \sum_{i \in S_I} 2^{-i}, \quad S_I \subset \{1, 2, \cdots, K\}, \quad K: \text{the number of the adders}$$

(24)
4. Sigma-delta domain bandpass filter

In this section, we will design an SD domain bandpass filter modeled after an ADPF. In Subsection 4.1, we will show a design procedure of a bandpass ADPF which consists of coupled lossless transmission lines. In the design of this kind of ADPFs, it is assumed that even and odd mode impedance values $Z_e$, $Z_o$ of the coupled transmission lines are different but even and odd mode electrical lengths $\theta_e$, $\theta_o$ or propagation constants $\gamma_e$, $\gamma_o$ are equal, as given by Eqs. (11) and (12). We will determine $Z_e$ and $Z_o$ such that the ADPF satisfies given specifications. In Subsection 4.2, we will construct an SD domain bandpass filter by connecting circuit blocks corresponding to the coupled transmission lines of the ADPF. The circuit blocks are built of shift register pairs and weighted sum circuits. The register lengths and the weights are determined from the center frequency and impedance values $Z_e$, $Z_o$ of the ADPF so that the SD domain bandpass filter possesses the same frequency characteristics as the ADPF. In Subsection 4.3, we will compare the frequency characteristics of the SD domain bandpass filter with the theoretical characteristics of the ADPF.

The real coupled transmission lines of an implemented ADPF might have different impedance values from the determined $Z_e$ and $Z_o$. The lines might have resistive component although they are assumed to be lossless when the ADPF is designed. However, the difference and the loss do not affect on the characteristics of the SD domain bandpass filter because it is modeled after the ideal ADPF in its design stage.

4.1 Reference ADPF

We briefly show an ADPF after which an SD domain bandpass filter will be modeled. For more details on the ADPF, refer to [23–25].

Figure 5(a) shows an $n$-th order lumped parameter prototype lowpass filter with cutoff frequency $\omega_c$. Generally, the frequency is normalized to $\omega_c = 1$. In Fig. 5(a), $g_0$ and $g_{n+1}$ are source and load resistance (or conductance) values. Other $g$-values are inductance and capacitance values. We transform the lowpass filter to a narrow bandpass filter shown in Fig. 5(b) with center frequency $\omega_0$ and passband $[\omega_1, \omega_2]$, $\omega_1\omega_2 = \omega_0^2$. The series and shunt resonators $jX_k(\omega) = j\omega L_k + 1/j\omega C_k$, $jB_i(\omega) = j\omega C_i + 1/j\omega L_i$ are determined so that they satisfy the following equations of reactance and susceptance slope parameters $x_k$, $b_i$:

$$x_k \equiv \frac{\omega_0}{2} \frac{dX_k}{d\omega} \bigg|_{\omega=\omega_0} = \omega_0 L_k = \frac{\omega_c g_k}{\Delta\omega_{\text{norm}}}$$

$$b_i \equiv \frac{\omega_0}{2} \frac{dB_i}{d\omega} \bigg|_{\omega=\omega_0} = \omega_0 C_i = \frac{\omega_c g_i}{\Delta\omega_{\text{norm}}}$$

where normalized bandwidth $\Delta\omega_{\text{norm}}$ is given by

$$\Delta\omega_{\text{norm}} = \frac{\omega_2 - \omega_1}{\omega_0}$$
Another type of bandpass filter is constructed of admittance inverters (J-inverters) and shunt resonators, as shown in Fig. 5(c). Admittance inverter with suffix \((i, i+1)\), \(i = 0, 1, \ldots, n\), should be given in \(F\)-matrix form by

\[
F_{\text{inv},i,i+1} = \begin{bmatrix} 0 & \pm \frac{1}{jJ_{i,i+1}} \\ \mp jJ_{i,i+1} & 0 \end{bmatrix},
\]

\((28)\)

where \(b_i\) is a susceptance slope parameter of a shunt resonator consisting of \(L_{pi}\) and \(C_{pi}\) in Fig. 5(c).

Figure 6(a) shows coupled quarter wavelength transmission lines with the right terminal of TL_1 and the left terminal of TL_2 open-circuited. The open-circuited coupled lines are considered as a two-port circuit possessing bandpass frequency response characteristic. A bandpass ADPF is constructed by connecting \(n+1\) coupled-line blocks as shown in 6(b). Length of the coupled lines is a quarter of the wavelength of a sinusoidal wave whose frequency is \(\omega_0\). The ADPF whose coupled line block with label \((i, i+1)\) has the following even and odd mode characteristic impedance values possesses the same frequency response characteristics as the lumped parameter bandpass filter in Fig. 5(c).

\[
Z_{i,i+1}^{e} = Z_{io}(1 + Z_{io}J_{i,i+1} + Z_{io}^2J_{i,i+1}^2),
\]

\[
Z_{i,i+1}^{o} = Z_{io}(1 - Z_{io}J_{i,i+1} + Z_{io}^2J_{i,i+1}^2),
\]

\[
Z_{io} = Z_S = Z_L : \text{characteristic impedance of terminating lines connected to source and load.}
\]

\((29)\)

We design a bandpass ADPF from a prototype lumped parameter lowpass filter with \(\omega_c = 1\). The prototype filter is a Chebyshev filter whose order is \(n = 3\) and whose passband ripple is less than 0.1dB. It consists of the following components:

\[g_0 = 1 \text{ ohm}, \ g_4 = 1 \text{S}, \ g_1 = g_3 = 0.6292 \text{H}, \ g_2 = 0.9703 \text{F}\]

Our target bandpass characteristics are as follows:

Center frequency: \(\omega_0 = \frac{\pi}{2}\) \quad Passband width: \(\omega_2 - \omega_1 = \frac{2\pi}{100}\)

We determine circuit elements of a bandpass filter of the type shown in Fig. 5(c) from Eq. (28) so that it possesses above characteristics. Finally, we build a bandpass ADPF of \((n + 1 = 4)\) blocks of coupled transmission lines, as shown in Fig. 6(b). Table I shows even and odd mode characteristic impedance obtained from Eq. (29) when \(z_{io}\) is normalized to 1ohm. The impedance values of blocks (2, 3) and (3, 4) are the same with those of blocks (1, 2) and (0, 1) respectively.
Table I. Even and odd mode characteristic impedance values of the coupled transmission lines for the bandpass ADPF and the coefficients of the SD domain bandpass filter.

| Block | $z_e$ [ohm] | $z_o$ [ohm] | Coefficient $c_e$ | Coefficient $c_o$ |
|-------|-------------|-------------|------------------|------------------|
| Block_1 | 1.2734 | 0.8265 | 0.5931 | 2/7+1/10 |
| Block_2 | 1.0418 | 0.9614 | 0.5196 | 1/3+1/7 |

4.2 Structure of SD domain bandpass filter

We consider the structure and the parameters of an SD domain bandpass filter modeled after the bandpass ADPF.

We derive equations describing a spatio-temporally discretized model of the block in Fig. 6(a) from Eq. (14) in Section 2. Let the position of the left and the right terminals of the block be given by $x = 0$ and $l$ respectively. Reflection conditions at the open-circuited terminals of the two lines are

$$w_{B,1}(l) = w_{F,1}(l), \quad w_{F,2}(0) = w_{B,2}(0)$$

(30)

In Eq. (14), we find equations expressing relations between $w_{F,2}(l)$ and $w_{F,2}(0)$ for the forward wave on TL2 and between $w_{B,1}(0)$ and $w_{B,1}(l)$ for the backward wave on TL1. The equation of $w_{F,2}$ and that of $w_{B,1}$ respectively contain opposite-directional components $w_{B,1}(0)$ and $w_{F,2}(l)$. We interpret the components as flow of electric energy into the block through the left terminal of TL1 and the right terminal of TL2. Electric energy decreases outside the block. Then, we may replace the opposite-directional components on the right hand side of Eq. (14) by reversely signed same directional components, that is,

$$w_{B,1}(0) \rightarrow -w_{F,1}(0), \quad w_{F,2}(l) \rightarrow -w_{B,2}(l)$$

(31)

Term $\exp(-j\theta)$ in Eq. (14) expresses equivalent propagation delay of sinusoidal waves on lossless transmission lines. Suppose that we employ shift registers of length $l_D$. They and bit-streams shifted on them represent the lossless transmission lines and the waves on the lines. Then, term $\exp(-j\theta)$ corresponds in the $z$-domain to $z^{-l_D}$. By imposing condition (30) and applying replacement (31) to Eq. (14) and by the $z$-transformation of the equation, we obtain the following equations describing a spatio-temporally discretized model of the block:

$$\begin{bmatrix} W_{F,1}(l_D) \\ W_{B,2}(0) \end{bmatrix} = A_{BP,blk} \begin{bmatrix} W_{F,1}(0) \\ W_{B,2}(l_D) \end{bmatrix} - B_{BP,blk} \begin{bmatrix} W_{F,1}(l_D) \\ W_{B,2}(0) \end{bmatrix},$$

$$\begin{bmatrix} W_{B,1}(0) \\ W_{F,2}(l_D) \end{bmatrix} = A_{BP,blk} \begin{bmatrix} W_{F,1}(l_D) \\ W_{B,2}(0) \end{bmatrix} + B_{BP,blk} \begin{bmatrix} W_{F,1}(0) \\ W_{B,2}(l_D) \end{bmatrix},$$

(32)

where variables $W_{F/B,1/2}(0/l_D)$ represent the $z$-transforms of the temporal local averages $w_{F/B,1/2}(0/l_D)$ of inputs and outputs $w_{F/B,1/2}(0/l_D)$ of employed shift registers and coefficients $c_e$ and $c_o$ are given by

$$c_e = \frac{1}{4}(k_z + k_z^{-1})k_z^{-1}, \quad c_o = \frac{1}{4}(k_z + k_z^{-1})k_z$$

(33)

A circuit block described by Eq. (32) is shown in Fig. 7(a). An SD domain bandpass filter corresponding to the ADPF in Fig. 6(b) is constructed by connecting four blocks as shown in Fig. 7(b). Shift registers LSR1/2, RSR1/2 represent transmission line TL1/2 whose length is equal to the quarter-wavelength of a sinusoidal wave at frequency $\omega_0$. Then, shift register length of the blocks is given by $l_D = \omega_{z}/\omega_0/4$, $\omega_z = 2\pi f_s$, $f_s$: SD modulated signal rate. Even and odd mode characteristic impedance values $Z_e$ and $Z_o$ for the reference bandpass ADPF are given in Table I. Then, coefficients of the
blocks are determined by Eqs. (13) and (33). Since the blocks are models of coupled lines with no power dissipation nor amplification, the coefficients by which discretized power waves $w_{F/B,1/2}^c$ are multiplied should be normalized to satisfy

$$2(c_e^2 + c_o^2) = 1$$  \hspace{1cm} (34)

Coefficients of the SD domain filter are shown in Table I. The coefficients in Block3 and Block4 are respectively the same as those of Block2 and Block1. The coefficients are approximated by rational numbers so that weighted sum circuits in Section 3 can be employed. In the approximation, the rational coefficients are determined to be slightly smaller than the real coefficients in order to prevent the phenomenon corresponding to the power amplification and to stabilize the SD domain filter.

We estimate the number of necessary circuit cells to construct the SD domain bandpass filter with first-order single-bit SD modulated signal form. The filter is built of four blocks of coupled lines. Each block consists of four shift registers of length $l_D = 2^{10}$ and four weighted sum operators. The shift registers are cascaded unit time delays (UDs). Each weighted sum operator consists of two 2-input adders, four coefficient multipliers ($c_e$ and $c_o$ are sums of two rational numbers as given in Table I), and one 4-input adder, which can be built as explained in Section 3. Sorting networks built of AND-OR gate pairs are used for them. Table II shows the number of necessary circuit cells to build the filter. The gate count of a digital CMOS circuit designed to simulate the behavior of the SD domain filter is also shown in Table II for grasping the scale of the filter circuit.

### 4.3 Frequency response characteristics

Two coupled lines TL1, TL2 are considered as a four-port circuit and described in $Z$-matrix form by Eq. (19). The right terminal of TL1 and the left terminal of TL2 are open when they are used for

---

**Table II.** The number of necessary circuit cells to construct the SD domain bandpass and band-elimination filters.

| Filter type | Compare & Exchange | Unit time delay | NOT gate | Equivalent CMOS gate count (approx.) |
|-------------|--------------------|-----------------|----------|--------------------------------------|
| BPF         | 15856              | 17472           | 144      | 119K gates                           |
| BEF         | 240                | 18084           | 24       | 91K gates                            |

---

---
the bandpass ADPF. We derive a two-port expression of a bandpass block whose terminals are the left terminal of TL₁ and the right terminal of TL₂. Substituting the open condition, i.e., $i₁(l) = i₂(0) = 0$, in Eq. (19) and using the assumption that $\theta_e = \theta_o = \theta_w$, we obtain a $Z$-matrix of the two-port circuit as

$$
Z_{BP,blk} = \begin{bmatrix}
\frac{1}{j \tan \theta} & \frac{1}{j \sin \theta} \\
\frac{1}{Z_e + Z_o} & \frac{1}{Z_e - Z_o}
\end{bmatrix}
$$

(35)

Let the $Z$-matrix of the block with index $i$ in the bandpass ADPF be denoted by $Z_{BP,blk,i}$. Transforming $Z_{BP,blk,i}$ to transmission ($F$) matrix $F_{BP,blk,i}$, we obtain the $F$-matrix of the bandpass ADPF as

$$F_{a-bpf} = \prod_{i=1}^{4} F_{BP,blk,i}
$$

(36)

A block of the SD domain bandpass filter is expressed by Eq. (32). The equation contains many variables with similar denotations. We distinguish the inputs $W_{F,1}(0), W_{B,2}(l_D)$ and outputs $W_{B,1}(0), W_{F,2}(l_D)$ from other state variables by using the following denotations:

$$X_b = W_{F,1}(0), \quad Y_b = W_{B,2}(l_D), \quad U_b = W_{B,1}(0), \quad V_b = W_{F,2}(l_D)
$$

(37)

Eliminating $W_{F,1}(l_D)$ and $W_{B,2}(0)$ from Eq. (32), we obtain the following scattering ($S$) matrix expression of the block:

$$
\begin{bmatrix}
V_b \\
U_b
\end{bmatrix} = S_{BP,blk} \begin{bmatrix}
X_b \\
Y_b
\end{bmatrix}, \quad S_{BP,blk} = A_{BP,blk}(E + B_{BP,blk})^{-1}A_{BP,blk} + B_{BP,blk},
$$

(38)

$$E : 2 \times 2 \text{ identity matrix}
$$

We transform the $S$-matrix of the $i$-th block in the SD domain bandpass filter to a transfer scattering ($T$) matrix $T_{BP,blk,i}$. Let $X$, $Y$, $U$, and $V$ denote the $z$-transforms of the temporal local averages of the inputs $x$, $y$ and outputs $u$, $v$ of the filter. Then, the filter is described by

$$
\begin{bmatrix}
X \\
U
\end{bmatrix} = T_{sd-bpf} \begin{bmatrix}
V \\
Y
\end{bmatrix}, \quad T_{sd-bpf} = \prod_{i=1}^{4} T_{BP,blk,i}
$$

(39)

Figure 8 shows the frequency response characteristics of the SD domain bandpass filter designed in Subsection 4.2. The characteristic curves $V/X$ obtained numerically with a digital circuit simulator and analytically from Eq. (39) are shown in the figure. The frequency response characteristics of the reference ADPF, which is estimated from Eq. (36), are not shown in the figure. They overlap the analytical response curves of the SD domain filter.
5. Sigma-delta domain band-elimination filter

Equation (17) describes wave propagation on coupled lossless transmission lines on an assumption that even and odd mode characteristic impedance values $Z_e$ and $Z_o$ are equal. Although the assumption may be impractical, the difference between even and odd mode electrical lengths $\theta_e$ and $\theta_o$ will theoretically give bandpass or band-elimination characteristic to ADPFs built of coupled transmission lines. The practicability of ADPFs to be referenced is not important since our interest is to construct SD domain filters modeled after the theoretical ADPFs. The important point is to construct the SD domain filters without coefficient multipliers. In this section, we consider band-elimination SD domain filters on the conditions that $Z_e = Z_o$ and $\gamma_e \neq \gamma_o$, as given by Eq. (15).

5.1 Reference ADPF

Figure 9 shows a band-elimination ADPF consisting of blocks, each built up of coupled lines $TL_1$, $TL_2$ and an open-circuited stub [25]. The length of the three lines is $l$. We express the block in Fig. 9(a) in $Z$-matrix form. Let the characteristic impedance and the propagation constant of the stub be $Z = \sqrt{L/C}$ and $\gamma_{stb} = j\omega\sqrt{LC}$. We assume that $Z_e = Z_o = Z$. The voltage and the current at the left and right ends of $TL_1$ and $TL_2$ and at the open-circuited end of the stub are denoted as in Fig. 9(a).

We describe the stub using Eq. (18) as

$\begin{bmatrix} v_2(l) \\ v_3(l) \end{bmatrix} = Z_{stb} \begin{bmatrix} i_2(l) \\ -i_3(l) \end{bmatrix}$, \[ Z_{stb} = Z(Z, \theta_{stb}), \theta_{stb} = \gamma_{stb} l \] (40)

From Eqs. (19), (40), and that $i_2(0) = i_3(l) = 0$, we obtain

$\begin{bmatrix} v_1(0) \\ v_1(l) \end{bmatrix} = Z_{BE, blk} \begin{bmatrix} i_1(0) \\ -i_1(l) \end{bmatrix}$, \[ Z_{BE, blk} = \frac{1}{2} \left\{ Z_c + Z_d - \frac{1}{z_{c,22} + z_{d,22} + 2z_{stb,11}} \right\} \begin{bmatrix} z_{c,12} - z_{d,12} \\ z_{c,22} - z_{d,22} \end{bmatrix} \begin{bmatrix} z_{c,21} - z_{d,21} \\ z_{c,22} - z_{d,22} \end{bmatrix} \]

where $z_{c,ij}$, $z_{d,ij}$, and $z_{stb,ij}$ are the $i,j$ elements of $Z_c$, $Z_d$, and $Z_{stb}$ respectively.

We obtained frequency response characteristics of the block from Eq. (41) by transforming $Z_{BE, blk}$ to an $F$-matrix as we did to investigate the characteristics of the bandpass ADPF in Section 4. Then,
we confirmed that the ADPF possessed band-elimination characteristics even on the conditions that 
\(Z_a = Z_o\) and \(\theta_e \neq \theta_o\). However, no method for designing band-elimination ADPFs has been established on these conditions. Thus, SD domain band-elimination filters presented in the next subsection inherit only the structure shown in Fig. 9(b).

### 5.2 Structure of SD domain band-elimination filter

Starting from Eq. (17) in Section 2, we design a spatio-temporally discretized model of the analog distributed parameter block in Fig. 9(a). The open-circuited terminal of the stub causes total reflection. Then, we have

\[
w_{B,2}(l) = w_{F,2}(l) \exp(-j2\theta_{stb})
\]

at the right terminal of TL. The total reflection at the left terminal of TL is expressed by

\[
w_{F,2}(0) = w_{B,2}(0)
\]

Assume that coupled lines TL\(_1\) and TL\(_2\) are replaced by two independent lines TL\(_e\) and TL\(_o\). Let \(l_{D,e}\), \(l_{D,o}\), and \(l_{D,\text{stb}}\) be the length of shift register pairs to be employed to represent TL\(_e\), TL\(_o\), and the stub. From Eq. (17) with delay terms \(\exp(-j\theta_e)\) and \(\exp(-j\theta_o)\) replaced respectively by \(z^{-l_{D,e}}\) and \(z^{-l_{D,o}}\), Eq. (42) with term \(\exp(-j2\theta_{stb})\) substituted by \(z^{-2l_{D,\text{stb}}}\), and Eq. (43), we obtain the following equations expressing a spatio-temporally discretized model of the distributed parameter circuit block in the \(z\)-domain:

\[
\begin{bmatrix}
W_{F,e}(0)
\\W_{B,e}(l_{D,e})
\\W_{B,o}(l_{D,o})
\end{bmatrix}
= 
\begin{bmatrix}
A_{BE,blk}
\\B_{BE,blk}
\\C_{BE,blk}
\end{bmatrix}
\begin{bmatrix}
W_{F,e}(0)
\\W_{B,e}(l_{D,e})
\\W_{B,o}(l_{D,o})
\end{bmatrix}
+ \begin{bmatrix}
X_b
\\Y_b
\end{bmatrix},
\]

(44)

\[
A_{BE,blk} = \frac{1}{2}
\begin{bmatrix}
0 & z^{-l_{D,e}} & 0 & -z^{-l_{D,o}}
\-z^{-l_{D,e}} & 0 & -z^{-l_{D,o}} & 0
\0 & -z^{-l_{D,e}} & 0 & z^{-l_{D,o}}
\-z^{-l_{D,e}} & 0 & z^{-l_{D,o}} & 0
\end{bmatrix},
\]

\[
B_{BE,blk} = \frac{1}{2}
\begin{bmatrix}
1 & 0
\0 & 1
\1 & 0
\0 & 1
\end{bmatrix},
\]

\[
C_{BE,blk} =
\begin{bmatrix}
0 & z^{-l_{D,e}} & 0 & z^{-l_{D,o}}
\0 & z^{-l_{D,e}} & 0 & z^{-l_{D,o}}
\end{bmatrix},
\]

New denotations \(X_b\), \(Y_b\), \(U_b\), and \(V_b\) in Eq. (44) represent the \(z\)-transforms of the temporal local averages of the power waves at the left and the right ends of TL\(_1\), that is,

\[
X_b = W_{F,1}(0), \quad Y_b = W_{B,1}(l_D), \quad U_b = W_{B,1}(0), \quad V_b = W_{F,1}(l_D)
\]

Then, they will be inputs and outputs of the block. Let left and right-shift register pairs representing TL\(_e\), TL\(_o\), and the stub be denoted by (LSR\(_e\), RSR\(_e\)), (LSR\(_o\), RSR\(_o\)), and (LSR\(_{stb}\), RSR\(_{stb}\)). The state variables in Eq. (44) are \(z\)-transformed temporal local averages of even and odd mode power waves at the inputs of LSR\(_e\), RSR\(_e\), LSR\(_o\), and RSR\(_o\), that is,

\[
\begin{bmatrix}
W_{F,e}(0)
\\W_{B,e}(l_{D,e})
\\W_{F,o}(0)
\\W_{B,o}(l_{D,o})
\end{bmatrix}
= \frac{1}{2}
\begin{bmatrix}
1 & 0 & 1 & 0
\1 & 0 & -1 & 0
\0 & 1 & 0 & -1
\1 & 0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
W_{F,1}(0)
\\W_{B,1}(l_D)
\\W_{F,2}(0)
\\W_{B,2}(l_D)
\end{bmatrix},
\]

(46)
Figure 10(a) shows the spatio-temporally discretized block model described by Eqs. (44), (45), and (46). The shift registers corresponding to TL\(_e\), TL\(_o\) are determined differently in length to represent \(\gamma_e \neq \gamma_o\) or \(\theta_e \neq \theta_o\). Adders in the block are weighted sum circuits presented in Section 3. More complex weighted sum circuits are not used at all.

An SD domain band-elimination filter modeled after the ADPF in Fig. 9(b) can be built by connecting the blocks as shown in Fig. 10(b). The frequency response characteristics of the SD domain filter are determined only by the length of shift registers. The multiplier-less simple structure is highly advantageous in fabricating nanometer-scale SD domain filter circuits.

We estimate the circuit scale of the SD domain band-elimination filter with first-order single-bit SD modulated signal form. The filter is built by cascading three blocks. Each block consists of six shift registers of length \(l_D \approx 1000\) and eight 2-input adders that are weighted sum circuits with equal weights. We assume that odd-even transposition sorters are used for the adders. The number of necessary circuit cells to construct the SD domain band-elimination filter is shown in Table II. We see that most of the cells in the filter circuit are UD cells used for shift registers. The band-elimination filter without weighted sum circuits is smaller in circuit scale than the bandpass filter with many coefficient multipliers, just as we intended.

### Table III.
The number of blocks, register lengths, and center frequencies of the elimination bands of the blocks used for the SD domain band-elimination filters.

| Example | \(N_{blk}\) | Block No. | \(lD_{odd}\) | \(lD_e\) | \(lD_o\) | \(f_{c,i}\) |
|---------|----------|-----------|-----------|-----------|-----------|-----------|
| (a)     | 2        | 1         | 995       | 796       | 1194      | \(f_e(995x4)\) |
|         |          | 2         | 1005      | 804       | 1206      | \(f_e(1005x4)\) |
| (b)     | 3        | 1         | 995       | 796       | 1194      | \(f_e(995x4)\) |
|         |          | 2         | 1000      | 800       | 1200      | \(f_e(1000x4)\) |
|         |          | 3         | 1005      | 804       | 1206      | \(f_e(1005x4)\) |
| (c)     | 3        | 1         | 990       | 792       | 1188      | \(f_e(990x4)\) |
|         |          | 2         | 1000      | 800       | 1200      | \(f_e(1000x4)\) |
|         |          | 3         | 1010      | 808       | 1212      | \(f_e(1010x4)\) |

Figure 10(a) shows the spatio-temporally discretized block model described by Eqs. (44), (45), and (46). The shift registers corresponding to TL\(_e\), TL\(_o\) are determined differently in length to represent \(\gamma_e \neq \gamma_o\) or \(\theta_e \neq \theta_o\). Adders in the block are weighted sum circuits presented in Section 3. More complex weighted sum circuits are not used at all.

5.3 Frequency response characteristics

An \(S\)-matrix \(S_{BE,blk}\) for the \(i\)-th block is obtained from Eq. (44) as
$$\begin{bmatrix} U_b \\ V_b \end{bmatrix} = \begin{bmatrix} S_{BE,blk}X_b \\ Y_b \end{bmatrix}, \quad S_{BE,blk} = C_{BE,blk}(E - A_{BE,blk})^{-1}B_{BE,blk}$$  \hspace{1cm} (47)

We transform the $S$-matrix of the $i$-th block in the SD domain band-elimination filter to a $T$-matrix $T_{BE,blk,i}$. Let $X$, $Y$, $U$, and $V$ denote the $z$-transforms of the temporal local averages of the inputs $x$, $y$ and outputs $u$, $v$ of the filter. Then, the filter built of $N_{blk}$ blocks is described by

$$\begin{bmatrix} X \\ U \end{bmatrix} = T_{sd-bef} \begin{bmatrix} V \\ Y \end{bmatrix}, \quad T_{sd-bef} = \prod_{i=1}^{N_{blk}} T_{BE,blk,i}$$  \hspace{1cm} (48)

We build SD domain band-elimination filters. Table III shows the number $N_{blk}$ of cascaded blocks, the length of shift registers, and the center frequencies $f_{c,i}$, $i = 1,\cdots,N_{blk}$, of the elimination bands of the filter blocks. All the blocks of the three examples have the same register length ratio, $|l_{D,e} - l_{D,o}|/(2l_{D,sth}) = 0.2$. Figure 11 shows frequency response characteristics of the filters when they operate on first-order single-bit SD modulated signals. The characteristic curves $V/X$ obtained numerically with a digital circuit simulator and analytically from Eq. (48) are shown in the figure. Increasing the number of blocks makes attenuation in the elimination band large or the elimination band wide.

6. Evaluation of fault-tolerance
6.1 A multi-bit wave digital filter

Transient errors of circuit cells in a multi-bit digital signal processing (DSP) circuit may cause a serious problem, long lasting disturbance at the output of the DSP circuit. We show here behavior of a bandpass wave digital filter [28, 29] with multi-bit signal form when the most significant bit of an internal register flips.

Wave digital filters are temporally discretized models of lumped parameter filters consisting of reactance components and resistive terminations. Figure 12 shows the specifications of a wave digital filter, a Chebychev-type bandpass analog LC filter, and the wave digital filter modeled after the LC filter. The word-length of the digital filter is 24-bit. Figure 13 shows a response of the digital filter when a sinusoidal signal of frequency $f_{in} = f_o$: the center of passband) is inputted and the most significant bit of the register denoted by D of adaptor 3 is flipped. The error causes high output surge. It takes about $15/f_{in}$ for the filter to become steady again. As long as multi-bit signal form is employed, high surge noises caused by the errors can not be removed perfectly since an equipped fault tolerance inevitably misses the errors even at a very low probability.

6.2 An SD domain filter block to be evaluated

Shift registers used in SD domain filters can be replaced by cascaded UD cells. Weighted sum circuits, coefficient multipliers, and adders consist of binary sorting networks and NOT gates in addition to UD cells. Binary sorting networks can be built of LTGs as shown in Section 3. Then, the SD domain filters can be designed by using only three kinds of circuit cells, namely, UD cells, LTGs, and NOT gates. These circuit cells built of single-electron tunneling (SET) junctions [30, 31] were designed in [9] by referring to [32–34]. Using the SET cells, we can design SET circuits of the SD domain filters. Quantum-dot cellular automata (QCA) which function as SD domain lowpass wave filters were also designed in [35].

We design a circuit of the bandpass block shown in Fig. 7(a) by using UD cells, LTGs, and NOT gates. The parameters of the block are as follows:

- Length of cascaded UD cells: $l_D = 1024$
- Coefficients: $c_e = 19/32 (= 1/2 + 1/16 + 1/32)$,
  $c_o = 12/32 (= 1/4 + 1/8)$

Figure 14(b) and (c) show two circuits multiplying their inputs by coefficients $c_e$ and $c_o$. We designed them according to the explanation at the end of Section 3. That is, the circuits are respectively built
Fig. 11. Frequency response characteristics of the SD domain band-elimination filters. \( l_D (=1000) \): average of \( l_{D,\text{sth}} \).

by cascading five and three 2-input adders that are weighted sum circuits with weights of 1/2. The two-input adder operating on first-order SD modulated signals is shown in Fig. 14(a). We simulate the designed bandpass filter block by using SET circuit simulator SIMON [36]. The rate of the bit-stream input, the rate of clocking the bandpass block equivalently, is \( f_s = 10\text{MHz} \). Input \( x_b \) is a first-order binary SD modulated sinusoidal signal. Input \( y_h \) is an SD modulated zero constant. An example of noise shaped output obtained as a result of the circuit simulation is presented in the frequency domain in Fig. 15. Frequency response characteristics obtained by the simulation are shown in Fig. 16 along with analytically obtained curves. From the figures, we confirmed that the designed SET circuit
6.3 Evaluating fault tolerance

As mentioned in Section 1, quantum effect devices including SET junctions are sensitive to various external and internal interferences and cause frequent transient errors. From the architecture of SDSP circuits, it is expected that transient errors do not make SDSP circuits fail in operation and do not cause high surge noise at the outputs of the circuits [9]. We define fault tolerance of the SDSP circuits as these two persistences. In this subsection, we investigate whether a block of the bandpass SD domain filter in Section 4 is also fault-tolerant in the sense defined above. Even though the bandpass block may possess the fault-tolerant characteristics mentioned above, its output quality may degrade gradually with the transient error rate. We evaluate the output quality and attempt to keep the quality by employing hardware-redundancy in this subsection. We assume that errors of quantum effect devices induce transient errors of circuit cells. We then carry out the investigation and the evaluation by logic level circuit simulation. That is, the unreliable cells are fundamental elements in the simulation.

Let the transient error of a cell be independent of errors of other cells and a probability that a cell causes a transient error for a clock period be \( p \). The cell operations are assumed to become normal at the subsequent clock after the error although the error propagates forward. In the simulation, the
unreliable cells are made by placing a random sequence generator and an exclusive-OR gate at the outputs of normal cells as shown in Fig. 17. The generator outputs “1” and “0” independently in each clock period at probabilities $p$ and $1 - p$.

We evaluate output quality in the presence of transient errors of circuit cells. Several fault-tolerant schemes by hardware redundancy have been developed. We employ triple modular redundancy (TMR) [5] for cascaded UD cells as follows: Each UD cell line of length $l_D$ is divided into $N_{seg}$
short lines and TMR scheme is applied to the short lines. Specifically, the short lines are replaced by fault-tolerant segments shown in Fig. 18. A segment consists of redundant three lines of length \( l_{seg} = l_D/N_{seg} \) and single or triple majority gates. The majority gates are three-input LTGs. In the circuit simulation, the LTGs are also assumed to cause error at probability \( p \).

Figure 19(a) shows output noise power plotted against error probability \( p \) for the bandpass block with and without the hardware redundancy. The noise at \( p = 0 \) is due to the in-band components of SD modulation noise spectrum exemplified in Fig. 15. Figure 20 shows examples of the averaged waveform of output \( v_o \) when input \( x_b \) is a first-order single-bit SD modulated sinusoidal signal of amplitude 0.5 and frequency \( \omega_s/4l_D \), the hardware redundancy in Fig. 18(b) is applied, and transient errors are caused at the rate of \( p = 10^{-6}, 10^{-5}, 10^{-4}, \) and \( 10^{-3} \). In the simulation, the filter block was not found to fail in operation and output high surge noise even without the hardware redundancy.

We evaluate the quality of the signals outputted from the bandpass block in which transient errors are caused, by comparing with Bernoulli bit-streams of \( \{+1, -1\} \) employed in stochastic computing (SC). Both SC and SDSP employ dichotomous bit-stream signal forms and no operation sequence controller. The Bernoulli bit-streams and first-order SD modulated binary signals contain in-band quantization noise of the power \( P_{SC} \) and \( P_{SD} \) given by

\[
P_{SC} = \frac{2}{3 \cdot OSR} \quad \text{OSR : Oversampling ratio} \tag{49}
\]

\[
P_{SD} = \frac{1}{3 \cdot OSR^3}
\]

respectively [12]. Equation (49) implies that SD modulated signals are higher than the Bernoulli bit-streams in quality. When \( OSR = 2^{10} \), Eq. (49) gives \( P_{SC} = -32 \text{dB} \). Figure 19(a) shows that the bandpass block with no redundant UD cell line outputs signals containing noise of \(-80\text{dB}\) at \( p = 0 \). The noise power rises to that of the errorless Bernoulli bit-streams as \( p \) increases to \( 3 \times 10^{-5} \). From the viewpoint of signal quality, the architecture of the SD domain filter is superior to the SC architecture.

Figure 19(b) shows output noise power plotted against the number \( N_{seg} \) of segmentations when the lines of UD cells are equipped with the hardware redundancy. Increasing \( N_{seg} \) is effective in reducing SNR drop. However, excess segmentation with the redundant lines of the type shown in Fig. 18(a) is ineffective for frequent transient errors because of increasing errors in majority gates that are meant to correct errors.

7. Conclusions

We saw that two coupled transmission lines were transformed into two mutually independent transmission lines on which even and odd mode waves propagated. It was shown in [22] that a lossless transmission line corresponded to a pair of left and right-shift registers. Hence, a spatio-temporally discretized and two-level-quantized model of coupled transmission lines was built from four shift reg-
isters. Thus, SD domain bandpass and band-elimination filters modeled after ADPFs built of parallel line pairs as well as SD domain lowpass filters modeled after ADPFs built of single-lines can be constructed by using shift registers.

Weighted sum circuits and coefficient multipliers are also used for the filters. It is interesting that nonliner sorting networks were employed for these linear circuits.

We confirmed by circuit simulation and theoretical analysis that the designed SD domain bandpass filter possessed the same frequency response characteristics with the theoretical characteristics of the reference ADPF.

For further simplification of filter structure, we removed coefficient multipliers and employed shift registers of different lengths as we exemplified in the design of band-elimination filters. To establish a new procedure for the design of SD domain multiplierless filters that meet given specifications is one of our future works.

We investigated the fault-tolerant capability of the bandpass block for transient errors of internal circuit cells. Circuit simulation presented that the bandpass block did not fail in operation and did not output high surge noise in the presence of the errors although its output quality decreased. Digital circuits based on SC architecture also possess the fault-tolerant capability. However, Eq. (49)
implies that the quantization noise spectrum of the Bernoulli bit-stream signals for SC is uniform in the frequency domain. This means that the signals contain large in-band components of quantization noise while the quantization noise of SD modulated signals is swept out of their signal bands, as Fig. 15 has presented. Unlike SDSP, the in-band noise components influence nonlinear SC operation because of the difficulty of removing the noise components without signal components being attenuated [12].

References
[1] R. Waser (Ed.), “Nanoelectronics and information technology,” Third Edition, Wiley-VCH, 2012.
[2] B.J. van Wees, H. van Houten, C.W. Beenakker, J.G. Williamson, L.P. Kouwenhoven, D. van der Marel, and C.T. Foxon, “Quantized conductance of point contacts in a two-dimensional electron gas,” Physical Review Letters, vol. 60, no. 9, pp. 848–850, 1988.
[3] P. Graham and M. Gokhale, “Nanocomputing in the presence of defects and faults: A survey,” in S.K. Shukla, and R.I. Bahar (Eds.), Nano, Quantum and Molecular Computing, pp. 39–72, Kluwer Academic Publishers, 2004.
[4] S. Roy and V. Beiu, “Majority multiplexing — Economical redundant fault-tolerant designs for nanoarchitectures,” IEEE Trans. Nanotechnology, vol. 4, no. 4, pp. 441–451, 2005.
[5] C. Huang, “Robust computing with nano-scale devices — Progresses and challenges,” Lecture Notes in Electrical Engineering, vol. 58, Springer, 2010.
[6] M. Haselman, “The future of integrated circuits: A survey of nanoelectronics,” Proc. IEEE, vol. 98, no. 1, pp. 11–37, 2010.
[7] W. Qian, X. Li, M.D. Riedel, and D.J. Lilja, “An architecture for fault-tolerant computation with stochastic logic,” IEEE Trans. computers, vol. 60, no. 1, pp. 93–105, 2011.
[8] A. Alaghi and J.P. Hayes, “Survey of stochastic computing,” ACM Trans. Embedded Computing Systems, vol. 12, no. 2, Article 92, 2013.
[9] H. Fujisaka, M. Sakamoto, C.-J. Ahn, T. Kamio, and K. Haeiwa, “Sorter-based arithmetic circuits for sigma-delta domain signal processing — Part II: Multiplication and algebraic functions,” IEEE Trans. Circuits and Systems I, vol. 59, no. 9, pp. 1966–1979, 2012.
[10] N. Kouvaras, “Operations on delta-modulated signals and their application in the realization of

Fig. 20. Locally-averaged output waveforms of the SD domain filter block.
digital filters,” The Radio and Electronic Engineer, vol. 48, no. 9, pp. 431–438, 1978.

[11] D. Lagoyannis and N. Kouvaras, “Multipliers of delta-sigma sequences,” The Radio and Electronic Engineer, vol. 51, no. 6, pp. 281–286, 1981.

[12] H. Fujisaka, T. Kamio, C.-J. Ahn, M. Sakamoto, and K. Haeiwa, “Sorter-based arithmetic circuits for sigma-delta domain signal processing – Part I: Addition, approximate transcendental functions, and log-domain operations,” IEEE Trans. Circuits and Systems I, vol. 59, no. 9, pp. 1952–1965, 2012.

[13] M. Freedman and D.G. Zrilić, “Nonlinear arithmetic operations on the delta-sigma pulse stream,” Signal Processing, vol. 21, pp. 25–35, 1990.

[14] H. Fujisaka, T. Kamio, C. Ahn, and K. Haeiwa, “Sequence characteristics of multi-level and second-order sigma-delta modulated signals,” NOLTA, vol. 4, no. 3, pp. 313–339, 2013.

[15] J.C. Candy and G.C. Temes, “Oversampling methods for A/D and D/A conversion,” in J.C. Candy and G.C. Temes (Eds.), Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation, IEEE Press, pp. 1–29, 1992.

[16] J.M. de la Rosa, “Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey,” IEEE Trans. Circuits and Systems I, vol. 58, no. 1, pp. 1–21, 2011.

[17] P.W. Wong and R.M. Gray, “FIR filters with sigma-delta modulation encoding,” IEEE Trans. Acoustics, Speech, and Signal Processing, vol. 38, no. 6, pp. 979–990, 1990.

[18] P.W. Wong, “Fully sigma-delta modulation encoded FIR filters,” IEEE Trans. Signal Processing, vol. 40, no. 6, pp. 1605–1610, 1992.

[19] S.M. Kershaw, S. Summerfield, M.B. Sandler, and M. Anderson, “Realisation and implementation of a sigma-delta bit-stream FIR filter,” IEE Proc. Circuits, Devices, and Systems, vol. 143, no. 5, pp. 267–273, 1996.

[20] A. Pneumatikakis, V. Anastassopoulos, and T. Deliyannis, “Realization of higher-order IIR delta sigma filters,” Int’l Journal on Electronics, vol. 78, no. 6, pp. 1071–1089, 1995.

[21] D.A. Johns and D.M. Lewis, “Design and analysis of delta-sigma based IIR filters,” IEEE Trans. Circuits and Systems II, vol. 40, no. 4, pp. 233–240, 1993.

[22] H. Fujisaka, T. Kamio, C. Ahn, M. Sakamoto, and K. Haeiwa, “A sigma-delta domain lowpass wave filter,” IEEE Trans. Circuits and Systems I, vol. 62, no. 1, pp. 167–176, 2015.

[23] D.M. Pozar, Microwave Engineering, Fourth Edition, John Wiley & Sons, 2011.

[24] G. Matthaei, L. Young, and E.M.T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures, Artech House Publishers, 1980.

[25] J. Hong and M.J. Lancaster, Microstrip Filters for RF/Microwave Applications, Wiley Interscience Publishers, 2001.

[26] W. Li, J.-N. Lin, and R. Unbehauen, “Unification of order-statistics based filters to piecewise-linear filters,” IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 11, pp. 1397–1403, 1999.

[27] C.R. Paul, Analysis of Multiconductor Transmission Lines, Second Edition, Wiley-IEEE Press, 2007.

[28] A. Fettweis, “Wave digital filters: Theory and practice,” Proc. IEEE, vol. 74, no. 2, pp. 270–327, 1986.

[29] S. Lawson and A. Mirzai, Wave Digital Filters, Ellis Horwood, 1990.

[30] H. Grabert and M.H. Devoret (Eds.), Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures, Plenum Press, 1992.

[31] J. Hoekstra, Introduction to Nanoelectronic Single-Electron Circuit Design, Pan Stanford Publishing, 2010.

[32] C. Lageweg, S. Cotofana, and S. Vassiliadis, “A linear threshold gate implementation in single-electron technology,” Proc. IEEE Computer Society VLSI workshop, pp. 93–98, 2001.

[33] J.R. Tucker, “Complementary digital logic based on the coulomb blockade,” Journal of Applied Physics, vol. 72, no. 9, pp. 4399–4413, 1992.

[34] M.W. Keller, J.M. Martinis, N.M. Zimmerman, and A.H. Steinbach, “Accuracy of electron counting using a 7-junction electron pump,” Applied Physics Letters, vol. 69, no. 12, pp. 1804–
1806, 1996.

[35] Y. Suzuki, H. Fujisaka, T. Kamio, and K. Haeiwa “Sorter-based digital wave filters – An approach to nanoelec-tronic signal processing,” Proc. IEEE Int’l Workshop on Nonlinear Dynamics of Electronic Systems, pp. 18–21, 2007.

[36] C. Wasshuber, H. Kosina, and S. Selberherr, “SIMON – A simulator for single-electron tunnel devices and circuits,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 16, no. 9, pp.937–944, 1997.