An Ultra-low Power Off Chip Capacitor-less LDO With High Transient Response

Zihang Zhang\textsuperscript{1,*}, Xiaoning Xin\textsuperscript{2}, Rongyan Chua\textsuperscript{3} and Meng Han\textsuperscript{4}

\textsuperscript{1}College of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning, 110020, China.
\textsuperscript{2}College of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning, 110020, China.
\textsuperscript{3}College of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning, 110020, China.
\textsuperscript{4}College of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning, 110020, China.

*Corresponding author’s e-mail: hak22@smail.sut.edu.cn

Abstract. This paper presents a low-dropout linear regulator (LDO) with ultra-low power, high transient response. This LDO adopts GAP-dynamic-bias circuit to achieve quiescent current as low as 242nA under 0-20mA load. A transient enhancement circuit based on window comparator is used to sense the output voltage change and further enhance the transient response. The circuit is designed and implemented using TSMC0.18um technology, and is verified by simulation using Spectre software. The simulation results show that when the load changes in the range of 10uA-20mA with a 1ns transition edge, the slowest overshoot and undershoot recovery times are only 2.36us and 2.15us. In the input voltage range of 2.5-3.6V, the linear regulation rate and load regulation rate are 0.479mV/V and 2.61nV/mA, respectively.

1. Introduction
Low-dropout regulator (LDO) as a power management chip has the advantages of low noise, low ripple, and small size, and is widely used in the market. Low power, high current and fast transient response are one of the development trends of LDO. The traditional LDO is usually based on the feedback loop of the error amplifier to respond to the change of the load current. When the load current jumps at a speed of ns, to improve the transient response speed, a high-bandwidth error amplifier is required. This achieves high transient response while making it difficult to reduce power consumption. There are many ways to improve the transient response of LDO. Zhan et al. [1] used a dynamic bias circuit to improve response speed; Or P.Y. et al. [2] used capacitive coupling to detect voltage peaks; Lu Y. et al. [3] regard the output pole as the main pole, which significantly increases the bandwidth and compensates the DC accuracy through another slow loop. The appeal method requires a complicated conversion circuit or compensation circuit, and it is difficult to reduce the power consumption and design complexity of the system.

In this paper, a low quiescent current and high transient response capacitance-less LDO is designed. A GAP-dynamic-bias circuit is used to achieve extremely low quiescent current; and a transient
enhancement circuit based on window comparator is used to improve the transient response. There is a good performance compromise between transient response capability and static power.

2. The structure and principle of LDO

![Figure 1. LDO overall architecture](image)

The structure of the LDO circuit proposed in this paper is shown in Figure 1, including an error amplifier, a GAP-dynamic-bias circuit, and a current feedback voltage driver buffer. The LDO includes a fast path composed of M22, M23, M24, M25, MN tubes and a slow path based on a telescope cascode amplifier. The function of the fast path is to improve the transient response capability of the system. The function of the slow path is mainly used to adjust the influence of temperature, power supply voltage, and process on the output voltage to improve the static index of the system. M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20 and M21 compose a Gap-dynamic-bias circuit, which dynamically provides bias voltage to the current feedback voltage driver by detecting the change of system output voltage, so as to improve the transient response ability and greatly reduce the static power consumption of the system.

Closed-loop gain based on error amplifier feedback loop $A_F$:

$$A_F = \frac{V_{\text{out}}}{V_{\text{ref}}} = \frac{A_v}{1 + A_v} = 1 - \frac{1}{1 + A_v}$$  \hspace{1cm} (1)

The above formula shows that there is a gain error $\frac{1}{1 + A_v}$ (A_v, the loop open loop gain value). To reduce the gain error and improve the static DC index of the LDO, it is necessary to increase the system open loop gain. Therefore, a telescope cascode amplifier is used to increase the gain.

The fast path is a negative feedback loop. When the load current increases, the branch current of the M24 tube decreases, and the M23 and M25 tubes form a circuit mirror. The decrease of the branch current of the M23 tube increases the grid voltage of the MN tube to generate current for the load application. Among them, the bias voltage of the M22 tube is provided by the dynamic bias circuit. The M10, M11, M18, and M19 tubes respectively constitute a differential pair, and the $V_{rh}$ and $V_{rl}$ voltages are set to 1.14V and 1.26V, respectively, provided by the bias voltage, and the output voltage of the system is detected at the other end. When the output voltage Vout is at the intermediate value of $V_{rh}$ and $V_{rl}$ at 1.2V (steady state), the bias current is the lowest; When the output voltage is higher than 1.2V (light load state) or lower than 1.2V (heavy load state), the highest bias current is provided to increase the bandwidth and increase the response speed.

In the case of a load of 20mA, the power tube MN will have leakage. Consider improving the current efficiency, capacitor $C_3$ and resistance $R_3$ are introduced. The introduction of $C_3$ suppresses the sudden change of output voltage. The function of resistance $R_1$ prevents the bulk from being directly connected to the output voltage (power tube source).
3. Stability analysis
In the entire LDO system, it can be seen as a two-stage circuit structure, which are the first-stage telescope cascode amplifier and the second-stage voltage driver.

The output stage of the voltage driver is composed of power tubes MN and M24, which is equivalent to a super source follower. The M24 tube is equivalent to the common drain connection for the same direction amplification. Since the Miller compensation technology requires the output stage to be amplified in the reverse direction, the parallel capacitor $C_1$ is used when compensating the system loop. $C_1$ further pushes the main pole of the system to low frequencies. The circuit diagram part of the voltage driver and its small signal model diagram are shown in Figure 2.

![Figure 2. a) Driver circuit diagram b) Small signal diagram](image)

According to the small signal circuit diagram above, we can know the output admittance of the output terminal $R_{out}$:

$$ R_{out} = \frac{1}{\frac{1}{g_{m2}+R_{on}} + \frac{1}{g_{m24}+\frac{1}{C_{gs}}}} $$

(2)

The LDO system open loop gain $A_v$ can be expressed as:

$$ A_v = \frac{g_{m2}(g_{m6}r_{os}r_{os2}g_{m4}r_{os2})}{1+g_{m24}+g_{mb}R_{out}} \approx g_{m2} \cdot (g_{m6}r_{os}r_{os2} \parallel g_{m4}r_{os2}) $$

(3)

The main pole $P_1$ and the secondary point $P_2$ are respectively expressed as:

$$ P_1 = \frac{1}{R_3C_1} \approx \frac{1}{g_{m24}+\frac{1}{C_{gs}}+g_{m24}R_{out}} $$

(4)

$$ P_2 = \frac{1}{R_{out}C_1} \approx \frac{1}{\frac{g_{m24}+\frac{1}{C_{gs}}}{g_{m24}+\frac{1}{C_{gs}}+g_{m24}R_{out}}} $$

(5)

The gain bandwidth $GBW$ is:

$$ GBW \approx A_vP_1 = \frac{g_{m2}}{C_1} $$

(6)

According to the above formula, it can be known that the output pole of the system $P_2$ will appear in the high frequency stage, far away from the origin. When the load current gradually decreases from heavy load to light load, the bandwidth of the output pole of the system gradually decreases. In order to ensure stability that the secondary point is higher than the gain bandwidth, shunt capacitor compensation technology is adopted. By designing a suitable parallel compensation capacitor $C_1$, the main pole of the system can be reduced, thereby reducing the gain bandwidth of the system, thereby ensuring sufficient phase margin of the system.

4. Window comparator transient enhancement circuit
The power tube in Figure 1 is an NMOS tube and has an inherent advantage of negative feedback compared to a PMOS tube. When the load changes rapidly, the transient response speed will be faster. Due to the large size of the power tube, there is also the gate-source parasitic capacitance. Because of the coupling of the parasitic capacitance, the NMOS tube’s innate negative feedback advantage will be weakened, and the overshoot or undershoot values will be too large. In order to solve the appeal problem, a ground compensation capacitor $C_2$ is connected to the grid of the power tube. But $C_2$
will affect the bandwidth of the voltage driver itself, so the transient enhancement circuit based on the window comparator in Figure 3 is designed to improve the transient response speed.

In Figure 3, the bias voltage $V_b$ is provided by GAP-dynamic-bias circuit, and the reference voltages $V_{rh}$ and $V_{rl}$ are provided by a bandgap reference voltage source. The circuit includes two positive feedback loops, the gate-drain interconnection structure composed of M4 and M7 tubes and M13 and M16 tubes respectively. When the load jumps from light load to heavy load, the output voltage $V_{out}$ decreases rapidly, and the differential pair composed of M5 and M8 is used for voltage comparison to drive the M10 transistor to generate a current $I_{10}$ to quickly charge the capacitor $C_2$. Similarly, when the load jumps from heavy load to light load, the output voltage $V_{out}$ rises rapidly, and the differential pair composed of M13 and M16 is compared to drive the M18 transistor to generate a current $I_{18}$ to quickly discharge the capacitor $C_2$, thereby reducing the power tube MN generate a large current.

5. Simulation results

The LDO proposed in this article supports an input voltage range of 2.5V-3.6V. The typical output voltage is 1.2V, the load current range is 100uA-20mA, and the load capacitance range is 0-100pF.

When the load current is 100uA and the load capacitance is 100pF, the output pole of frequency is the lowest, which corresponds to the worst case of stability. The amplitude-frequency characteristic curve under no-load and the load of 100uA and 100pF is shown in Figure 4. It can be seen that the phase margin is $85.9^\circ$, which can maintain the stability of the system.

![Figure 4. Amplitude-frequency characteristic curve under no-load and 100uA, 100pF load](image)

Figure 5 shows the transient response of the LDO when the load current undergoes 10uA-20mA and 20mA-10uA jumps within 1ns($C_L = 0pF$). When the 10uA-20mA jumps, the time for the output voltage to recover to $V_{OUT} \pm 5\%$ is only 2.15us; when the 20mA-10uA jumps, the time for the output voltage to recover to $V_{OUT} \pm 5\%$ is only 2.36us.
Figure 5. Transient simulation of load transient

Figure 6. LDO quiescent current power

$\left( I_L = 0\mu\text{A}\mid 100\mu\text{A}\mid 20\text{mA} \right)$

Figure 6 shows that under no load, 100μA load, and 20mA load, the quiescent current of 242nA remains basically unchanged.

The parameter comparison of this article and other literature heavy LDO is shown in Table 1.

| Publication | [4] | [5] | [6] | This work |
|-------------|-----|-----|-----|-----------|
| Technology [µm] | 0.065 | 0.35 | 0.18 | 0.18 |
| Input Voltage [V] | 1.3 | 3.7 | 2.3-3.3 | 2.5-3.6 |
| Output Voltage [V] | 1.1 | 3.25 | 1.8 | 1.2 |
| $C_{\text{load}}$ [pF] | 0-2000 | 100 | 100 | 0-100 |
| $I_{\text{load}}$ [mA] | 0.1-50 | 0.1-50 | 0.1-200 | 0.1-20 |
| Quiescent Current [µA] | 50-190 | 26 | 1.2 | < 0.242 |
| Line Regulation [mV/V] | 50 | 1.046 | 15.38 | 0.479 |
| Load Regulation [nV/mA] | 40 | 75.2 | 400 | 2.61 |
| Edge Time [nS] | 2 | 100 | 100 | 1 |
| Transient Response [µS] | - | 0.2 | 10 | 2.36 |

6. Conclusions
In this paper, an ultra-low power off chip capacitor-less LDO with high transient response is designed, and the static power consumption is only 242nA. The window comparator transient enhancement circuit is designed in this LDO to increase the transient response capability. The simulation results show that when the load current changes in the range of 10μA-20mA with a 1ns transition edge, the slowest time for the output voltage to recover VOUT±5% is only 2.36us.

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