Charge transfer and partial pinning at the contacts as the origin of a double dip in the transfer characteristics of graphene-based field-effect transistors

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Abstract
We discuss the origin of an additional dip other than the charge neutrality point observed in the transfer characteristics of graphene-based field-effect transistors with a Si/SiO\textsubscript{2} substrate used as the back-gate. The double dip is proved to arise from charge transfer between the graphene and the metal electrodes, while charge storage at the graphene/SiO\textsubscript{2} interface can make it more evident. Considering a different Fermi energy from the neutrality point along the channel and partial charge pinning at the contacts, we propose a model which explains all the features observed in the gate voltage loops. We finally show that the double dip enhanced hysteresis in the transfer characteristics can be exploited to realize graphene-based memory devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Graphene field-effect transistors (GFETs) have attracted substantial interest for applicability to high-speed electronics and spintronics and have been extensively used to investigate the electronic transport properties of graphene. In such devices, an electric current is injected/extracted from metallic electrodes (source/drain) through a graphene channel whose conductance is modulated by the electric field from a back- or top-gate. The linear energy dispersion, with zero bandgap and a double-cone shape with intrinsic Fermi level at the vertex, gives symmetric valence and conduction bands; differently from most materials, current modulation by means of a gate in GFETs is possible even without a bandgap, due to the vanishing density of states at the vertex [1, 2].

Metal/graphene contacts have been shown to play a significant role in the electrical characteristics of the transistors, and various metals (Al, Au, Co, Pd, Pt, Ti, …) have been employed as electrodes. Transfer characteristics of GFETs, i.e. the drain-to-source current versus gate voltage, $I_{DS}$–$V_{GS}$, curves, typically display a symmetric V-shape, with a hole dominated conductance (p-branch) at lower $V_{GS}$ and electron-type transport at more positive gate voltages (n-branch), separated by a valley corresponding to the charge neutrality condition (also known as the Dirac point) with equal electron and hole concentrations. This V-shape reflects the energy distribution of the density of states ($D(E) \propto |E|$), and a conductance dropping to zero at the Dirac point should be expected at low temperature; however, in actual devices, impurities and interaction with the surrounding dielectric introduce local fluctuations in the potential causing a finite density of states at the Dirac point; from the carrier viewpoint, these fluctuations result in localized puddles of electrons and holes which produce an appreciable conductance [3]. Noticeably asymmetric [4, 5] and/or anomalously distorted
p-branches [6–8] have been reported. The asymmetry between p- and n-branches was initially explained in terms of different cross sections of electron/hole scattering from charge impurities [9, 10], but more recently the metal/graphene interaction at the contacts has been considered as a key element [5, 11–14]. It has been found in particular that, even in the case of weak adhesion, as with Au, the metal electrodes cause the Fermi level $E_F$ to shift from the conical point in graphene bands, resulting in doping of graphene either with electrons or with holes; the amount of doping can be deduced from the difference of the metal and graphene work functions ($\Phi_M - \Phi_G$) and from the potential step ($\Delta V$) due to the metal/graphene chemical interaction ($E_F = \Phi_M - \Phi_G - \Delta V$) [11–14]. Depending on the polarity of carriers in the bulk of the graphene channel, charge transfer between metal and graphene leads to p–p, n–n or p–n junctions in the vicinity of the contacts which can cause asymmetry.

Nouchi et al [6, 7] have studied transfer characteristics in devices with ferromagnetic metal electrodes, reporting anomalously distorted p-branches, with a sort of additional minimum other than the Dirac point. They explain this effect by considering charge transfer from graphene to metal leads and assuming that the presence of an oxide layer spontaneously formed at the metal/graphene interface suppresses the charge-density pinning effect, i.e. favours the modulation of the charge-density of graphene at the metal electrodes by the gate voltage. A second conductance minimum to the left of the original Dirac point has also been very recently investigated by Chiu et al [15] for Ti-contacted graphene transistors in the high field regime. They showed that the original Dirac point stays unaffected, while the position of a second Dirac point caused by a drain stress depends on the back-gate voltage, and they argue that a positive charge is trapped at the graphene/oxide interface in the vicinity of the drain; such a charge induces the formation of a p–n junction in the drain region and accordingly they use a model based on a step-potential to account for the observed double Dirac point.

A double dip in the transfer characteristic has been also discussed by Barraza-Lopez et al [16] with a first-principles study of the conductance through graphene suspended between Al contacts. They show that the charge transfer at the leads and into the freestanding section gives rise to an electron–hole asymmetry in the conductance; more importantly they suggest that, for sufficiently long junctions, this charge transfer induces two conductance minima at the energies of the two Dirac points of the suspended and clamped regions, respectively.

In this paper we present measurements on Cr/Au-contacted long-channel (~10 μm) graphene transistors on Si/SiO2 substrate. We report the observation of hysteresis as well as double dips in the transfer characteristics, that, as far as we know, have never been reported before on GFETs with Cr/Au electrodes.

Charge trapped in the surrounding dielectric and in particular in silanol groups at the SiO2 surface is at the origin of the hysteresis; while, the gradient of carriers along the channel caused by electron transfer from the graphene to the Au/Cr contacts and the band shift induced by the back-gate voltage and the SiO2-trapped charge are proposed to account for the double dip feature. We show in particular that p–n junctions are spontaneously formed by charge transfer between the graphene and the electrodes and that a double Dirac point can be achieved when low-resistivity contacts are fabricated. We further clarify the role of charge stored at the SiO2 interface in the formation of the double dip and we propose partial charge pinning at the contacts to explain the current saturation observed at high back-gate voltages. Accordingly, a phenomenological modeling of experimental data is successfully implemented.

We finally show that the hysteresis, enhanced by a double dip, can conveniently be exploited to build graphene-based memory devices.

2. Device fabrication and measurement setup

Micron-scale graphene flakes were deposited by the Scotch-Tape method on 300 nm thick SiO2 thermally grown on top of a highly p-doped Si substrate. Natural graphite flakes (from NGS Naturgraphit GmbH) were repeatedly cleaved with adhesive tapes and then transferred to SiO2 substrates. The surface of the chip was inspected by optical microscopy to identify suitable few- and mono-layer graphene flakes according to the color contrast [17]. Single-layer graphene flakes were further confirmed by Raman spectroscopy [18]. Metal contacts of Cr/Au (5 nm/150 nm, with Cr as adhesion layer) were sputtered after electron beam lithography and structured by lift-off on selected single-layer graphene flakes. Soon after, some devices were covered by 250 nm thick polymethyl methacrylate (PMMA). PMMA was spin-coated on the whole chip and cross-linked, and thus made resistant to acetone etch, by exposure to 30 keV electrons at a dose of $3 \times 10^5 \mu C \text{cm}^{-2}$ on the device area.

Figures 1(a) and (b) show the layout and the SEM top view of a typical device before PMMA coverage, respectively. Figure 1(c) shows the Raman spectrum of the flake used as bulk channel with the G and 2D peaks typical of single-layer graphene. Single-layer graphene in a junction with a few layer graphene film (as in figure 1(b)) was preferred in the attempt to minimize the graphene doping due to interaction with the SiO2 substrate [19].

We performed three-terminal measurements, with the Si substrate as the back-gate and the metal electrodes as the source and drain. All the measurements were performed in air and at room temperature using an HP4140B semiconductor parameter analyzer. Back-gate voltage sweeps, in the interval (~80 V, 80 V), were performed at constant low drain bias (20 mV). Higher gate voltages were avoided to prevent oxide damage; indeed higher voltage stresses ($V_{GS} > 100$ V) were often observed to increase gate leakage until oxide breakdown.

3. Results and discussion

Figure 1(d) shows the transfer characteristic of the device. A minimum $I_{DS}$, i.e. a lower conductance, corresponding to the charge neutrality point, is observed at $V_{GS} \sim 60$ (45) V in an initial reverse (forward) $V_{GS}$ sweep with an amplitude of 70 V; the low on/off ratio of about 5 is expected for a graphene
flake with low or zero bandgap. A positive charge neutrality point $V_{GS}^*$ indicates that the graphene is unintentionally highly p-doped. We observed this behavior on all fabricated GFETs; indeed, the Dirac point was often located behind the sweeping upper limit of 80 V, especially for devices not covered by PMMA.

The formation of weak C–O bonds between graphene and SiO$_2$ has been proven [19, 20] to support p-type conductivity in graphene by transfer of charge from the carbon in graphene to the oxygen of the SiO$_2$. This increases the hole concentration and favors the formation of p-type conductivity at an unbiased gate, thus forward shifting the Dirac point. Moreover, molecules adsorbed on the surface of the channel or at the graphene/SiO$_2$ interface during the fabrication process, consisting mainly of hydrocarbons, carbon dioxide, oxygen and water, are known as a further cause of the forward shift of the charge neutrality point. Indeed, for H$_2$O [21], CO$_2$ and O$_2$ [22], it has been shown that there is an electron transfer from graphene to the adsorbed molecules, which results in p-doping for graphene. The use of PMMA as coverage of our devices prevents further adsorption and helps to maintain the neutrality point within the swept $V_{GS}$ range. This enabled us to measure and study both the p- and part of the n-branch of the transfer characteristic.

A second important feature observed in the measured $I_{DS}$–$V_{GS}$ curve of figure 1(d) is a clear hysteresis between the forward and reverse sweeps.

Several recent reports have shown a strong hysteretic behavior in the field-effect characteristics of Si/SiO$_2$ supported GFETs. In analogy to single-walled carbon-nanotube-based field-effect transistors [23, 24], gate hysteresis has been attributed mainly to charge trapping in silanol groups (Si–OH) with surface-bound H$_2$O molecules facilitating the process of charge transfer and trapping [25, 26]. Consequently the concentration, distribution and reactivity of the silanol groups of the underlying SiO$_2$ play a decisive role in the transfer characteristics of a GFET. A high concentration of silanol groups makes the SiO$_2$ surface hydrophilic (in general dipolar molecules can easily attach to SiOH), but special treatment can turn this surface hydrophobic; indeed, nearly hysteresis-free GFETs have been achieved on SiO$_2$/Si substrates covered by a thin hydrophobic self-assembled organic layer of HMDS solution (hexamethyldisilazane/acetone 1:1) [27]. Thermal annealing or vacuum pumping can also help to reduce hysteresis [14]. Nevertheless, we decided not to apply any treatment or annealing (other than the electrical one) to avoid the risk of introducing unwanted damage or stresses. Charges can be trapped in the PMMA as well; nevertheless, since the back-gate field is screened by the graphene layer, tunneling between the graphene channel and the top PMMA layer is suppressed with respect to tunneling between graphene and SiO$_2$ during $V_{GS}$ sweeps.

In figure 2 we report the evolution of transfer characteristics for successive $V_{GS}$ sweeps, acting as electrical...
annealing. Remarkably, figure 2(a) shows that the electrical cycles produce an increase of the current and the appearance of a double Dirac point, i.e. of two conductance minima. Further sweeps demonstrate the stabilization of the device (figure 2(b)). Swapping the drain and source has no effect. Two clear dips appear both in the reverse (where they are closer and less pronounced) and in the forward $V_{GS}$ sweep. Figure 2(c) shows that a slower sweeping rate, which favors charge injection and trapping at the SiO$_2$ surface, widens the hysteresis loop.

The electrical stabilization, due to current self-annealing, is mainly the result of graphene–electrode interface modifications, which reduce and stabilize the contact resistance; we exclude bulk channel changes since the PMMA layer prevents removal of contaminants from its surface [8] that may vary its conductance. The contact resistivity [28], $\rho_C = RW \sim 5 \, \text{k} \Omega \, \mu\text{m}$ ($W$ is the width of the channel), is on the low side of the range usually reported for Cr/Au-contacted GFETs ($2 \times 10^3 \, \Omega \, \mu\text{m} \leq \rho_C \leq 10^6 \, \Omega \, \mu\text{m}$) [29]; $\rho_C$ is estimated at $V_{GS} = -80 \, \text{V}$ when the source-to-drain resistance is dominated by the contacts, the graphene bulk channel being at its maximum conductance. A further confirmation of the good contacts stems from the calculation of the mobility [30]. Despite the top coverage, which may affect the mobility [31], the contact resistivity cannot be increased; this means that the Fermi energy at the contacts can vary only within a limited range from the Fermi energy within the graphene double-cone at the metal contacts with respect to the bulk channel; the Fermi level alignment within the graphene double-cone at the contacts with respect to the bulk channel: the Fermi level within the band diagrams is shifted by the back-gate voltage and is influenced by the charge trapped at the SiO$_2$/graphene interface.

Due to different work functions (4.6 eV for Cr and 5.1 eV for Au and 4.5 eV for graphene [12]) electrons transfer from the graphene to the metal electrodes, thus forming a doping gradient from the contacts to the bulk channel. Underneath and close to the electrodes, the graphene is more p-doped than in the channel [11]. The doping of the graphene by the contacts is not limited to only underneath the metal electrodes but extends for 0.2–0.3 $\mu$m [34] or longer [35] in the inner channel, since the graphene, having zero density of states at the Dirac point, is not able to absorb all the transferred charge at the interface.

While charge-density pinning (i.e. gate uncontrollability of charge-density at the metal contacts) could occur at Au/graphene contacts [5, 13, 34], reactive materials have been proven to lead to charge depinning [7], especially when an oxide layer is formed at the graphene/metal interface. We assume here partial charge pinning with charge at the contacts controlled by the back-gate up to a certain limit, over which the charge cannot be increased; this means that the Fermi energy at the contacts can vary only within a limited range from the conical point of the graphene bands. This assumption can be seen as a consequence of the low contact resistance which makes the potential of the graphene at the contacts be anchored to the bias of source and drain; in such a case, the field of the back-gate is expected to affect mainly the carrier concentration in the bulk graphene channel. We will also show that the assumption of partial pinning leads to a good fit of the $I_{DS}$–$V_{GS}$ curves on the whole $V_{GS}$ range.

The effect of charge transfer at the contacts can be taken into account by shifting the energy band diagram (double-cone) of the graphene upward with respect to that in the bulk channel for unbiased $V_{GS}$ (figure 3). The application of the back-gate voltage moves the Fermi level with respect to the double-cone, determining different conduction regions between source and drain. At $V_{GS} \geq 80 \, \text{V}$, n-type conduction takes place everywhere, thus giving a high conductance

![Figure 2](image-url)
respectively). Going to more negative local neutrality point in the channel and at the metal contacts, longer). Consequently, the n/n$^+$ at the contact regions (where graphene stays n-doped for i.e. a first Dirac point, is reached in the channel before that move away through contacts, so a charge neutrality condition, at the SiO$_2$/graphene interface, which, as already said, is at the origin of the leftward shift of the transfer characteristic during the following forward sweep, i.e. of the hysteresis. This trapped charge acts as a reduction of the overall p-doping and can be taken into account with a down-shift of the graphene bands (configuration 5). During the forward sweep the p-doping of the graphene is neutralized by attracting electrons from the contacts and a neutral condition is soon reached at the contacts, thus resulting in a first Dirac point (point 6 at $V_{GS}$ $\sim$ $-18$ V in figure 3(a)). Further increase of $V_{GS}$ creates a second dip (at $V_{GS}$ $\sim$ $48$ V) when neutrality is reached in the bulk channel (point 7). The second Dirac point happens at a $V_{GS}$ value slightly below the one observed during the reverse sweep as an effect of the charge stored at the SiO$_2$/graphene interface; finally a low-conductance n/n$^+$ structure (point 8) is formed again. The $\Delta V_{GS}$ $\sim$ $65$ V separation between the two dips in the forward sweep is increased with respect to the previous $\Delta V_{GS}$ $\sim$ $10$ V since the downward band shift created by the SiO$_2$ trapped charge and the injection of electrons from the contacts greatly favors the appearance of a Dirac point in the contact regions. The position of this point, being related to the SiO$_2$ trapped charge, depends also on the maximum negative voltage applied during the previous reverse sweep. Indeed, figure 4 shows that the position of the additional Dirac point depends on the starting value of the back-gate voltage sweep.

Very importantly, our model predicts that, whatever the choice of the metal leads is, the extra Dirac point appears always in the p-branch of the transfer characteristic. Indeed, a second dip has been searched for but not found under n-type transport conditions also on Ti- or Co-contacted GFETs [7, 15]; this observation has been explained by considering that positive charges are much easier to inject into the SiO$_2$ trap centers than electrons [15].

Furthermore, since the transfer characteristic of a GFET roughly reflects the density of states, our finding can also be considered as a measurement of the overall density of state of an Au-contacted graphene sheet, that as calculated in [36] is expected to present a double minimum. While [36] provides a theoretical description of the conductance based on the non-equilibrium Green function method in the ballistic limit, in the following we numerically reproduce the double dip behavior of the density of state in the context of the diffusive transport regime.

![Figure 3](image.png)
dependence only modifies the constant factor $A$ the two contact regions and divided the channel into three regions and taken the Fermi level at the contacts and in the bulk channel, we have $\rho$ that in the expression $\lambda$ (where $A$ E transport equation in describing the diffusive dynamics of the proved by a numerical simulation exploiting the Boltzmann The validity of the proposed phenomenological model has been

4. Numerical simulation

The validity of the proposed phenomenological model has been proved by a numerical simulation exploiting the Boltzmann transport equation in describing the diffusive dynamics of the device. Considering that the Fermi energy $E_F$ is linearly controlled by $V_{GS}$, and assuming that the charge stored at the SiO$_2$/graphene interface is uniformly distributed across the channel and its density $\rho_0$ is at most a second power of $V_{GS}$ [23, 24], the total carrier density $\rho$ along the graphene channel is, to a good approximation, a quadratic function of the Fermi energy. The dependence of $\rho$ on $E_F$ can be easily understood by considering that the energy dependence of the density of states of graphene is $D_{\rho}(E) \propto |E|$ and observing that in the expression $\rho = \rho_0 + A \sum_i \lambda f_i^\infty(D_i(E) f_i(E)) dE$ (where $A$ is a constant, $f_i(E)$ is the Fermi function, and $\lambda = \pm 1$ for electrons and holes, respectively) the integral roughly shows a quadratic behavior on $E_F$ whose temperature dependence only modifies the constant factor $A$.

Accordingly we have assumed an overall quadratic dependence of $\rho$ on $V_{GS}$. The value of $\rho$ so obtained has been used to calculate the graphene conductance $g$: $g \propto \frac{e^2}{h} \frac{\lambda}{E_F} \rho(E_F)$, with $v_F \approx 10^6$ m s$^{-1}$ the Fermi velocity and $T$ the temperature [1]. To take into account the mismatch of the Fermi level at the contacts and in the bulk channel, we have divided the channel into three regions and taken $E_F = E_C$ at the two contact regions and $E_F = E_M$ in the bulk channel (with $|E_M| > |E_C|$ at equilibrium), and both $E_C$ and $E_M$ quadratic functions of $V_{GS}$. Finally, the conductances of the three regions have been combined in series: $G^{-1} = \sum_{i=1}^3 \frac{1}{|G_i|} + Z$ (we have also included a parasitic impedance $Z$ originating from the contacts and leads).

In figure 4 we report experimental data for $G$–$V_{GS}$ recorded in a whole $V_{GS}$ loop starting at zero bias. The data (colored curves) are compared with the numerical simulation (black curves) resulting from our theoretical model. The dotted lines evidence the mismatch from the experimental data when no charge pinning is considered in the model; the introduction of an upper limit for $|E_C|$, i.e. the hypothesis of partial charge pinning, instead, well reproduces the measured $G$–$V_{GS}$ behavior. An additional element pointing towards our interpretation is obtained from the consideration that the pinned value of $|E_C|$, as extracted from the experimental data, asymptotically reaches the difference between the gold and graphene work functions (i.e. $\Phi_{Au} - \Phi_G \approx 0.6$ eV). However, we notice that the double dip feature is reproduced independently from the pinning. Furthermore, from the fit of the starting curve ($V_{GS} = 0 \rightarrow 80$ V (orange online)) we swept a value $|E_C - E_M| \approx 0.5$ eV. This value, compared with the quoted $\Phi_{Au} - \Phi_G = 0.6$ eV, allows us to estimate an interface voltage step $\Delta V = 0.1$ eV [11].

We highlight that the presence of a double dip results in an effective widening of the hysteretic loop. The hysteresis observed in carbon-nanotubes-based transistors has been exploited to build memory devices [24, 37, 38]. Similarly, here, the two values of the current at a given gate voltage can be considered as the two logic levels (on and off state) of a memory device; positive or negative $V_{GS}$ pulses can be used to switch between these two states to implement the write and erase operations. Figure 5 is a proof of the concept, where reading is performed at $V_{GS} = 0$ and ±80 V pulses are used for write and erase. The programming pulses are of course enormous for practical applications; nevertheless, with proper treatment of the SiO$_2$/Si or by ionic screening [39], it could be possible, in principle, to obtain transfer characteristics with the deeper dip around $V_{GS} = 0$ and accordingly considerably reduce the operating voltages. For practical technological applications, the same device could be implemented with a top-gate, thus leading to significantly lower write/erase voltages.
5. Conclusion

In conclusion, we have clarified the nature of the double dip often observed in the p-branch of the transfer characteristic of a GFET. We have shown that it is related to charge transfer between the graphene and the metal contact and that it is enhanced by the hysteresis provoked by charge storage at the graphene/SiO₂ interface. Elucidation of the origin of such an anomaly is of technological importance since the observed distortion indicates a deterioration of the gate voltage response of the device, i.e., a decrease in the field modulation of the channel conductance. Although a possible drawback of the device, i.e., a decrease in the field modulation of the channel conductance, we have also suggested that such a feature can be conveniently exploited to develop graphene-based memory devices.

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