Timing margin enhancement technique for current mode interface

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Abstract: This paper presents a circuit technique to enhance a timing margin between internal data and clock by enlarging an eye opening of the internal data in a unique current mode transceiver [1]. This technique compensates a systematic timing offset of the internal data, which is caused by unbalanced transmission current. The test-chip exhibits 0.1UI (Unit Interval) improvement of the internal data eye opening without significant power penalty, and achieves stable data communication through 50% longer transmission lines compared to the previous work [1].

Keywords: interface, current mode, low power

Classification: Integrated circuits

References

[1] T. Yoshikawa, T. Ogino and M. Nagata: IEICE Trans. Electron. \textbf{E91-C} (2008) 1453. DOI:10.1093/ietele/e91-c.9.1453
[2] T. Saeki and Y. Terao: FUJITSU Sci. Tech. J. \textbf{49} (2013) 245.
[3] D.-U. Park: U.S. Patent Application US2009/0132843 A1 (2009).

1 Introduction

An interface of middle-class bandwidth (312 Mbps~635 Mbps) is still demanded in a cellular phone and portable equipment for transmitting decompressed data from RF frontend LSI to baseband LSI, because the 3\textsuperscript{rd} generation (3G) of mobile telecommunications technology is still required for wide area coverage even in recent 4G Long Term Evolution (LTE) era [2]. On the other hand, a current mode approach is continuously considered for data bus and interface systems in portable equipment [3].

A unique current mode interface has been disclosed for the data transmission in the cellular phone [1]. It showed 625 Mbps data rate and 3.5 mW power dissipation with 150 µA driving current through 5 cm transmission line.

Considering the size of recent portable equipment such as Tablet PCs, stable communication through longer transmission lines is desired. To meet this require-
ment without power penalty, an internal timing margin should be enhanced with the minimum additional circuits.

2 Concept of timing margin enhancement

2.1 A flow of internal clock and data generation

Fig. 1 shows a block diagram of the current mode transceiver [1]. Transmitted data are fed to receiver inputs (RIN, /RIN) as the differential driving current through the transmission lines. Combinations of the differential driving current are \((3^*Id, 0)\), \((Id, 0)\), \((0, 3^*Id)\) and \((0, Id)\), where \(Id\) is base amount of the driving current (typically 150 µA). The driving currents through “RIN” and “/RIN” are converted to the differential internal voltage signals \((OUTPp, OUTMp)\) by the I/V converter, and “OUTPp” and “OUTMp” are fed to the Internal Clock and Data Generator.

![Fig. 1. Block diagram of the current mode transceiver](image1)

A block diagram of the Internal Clock and Data Generator is depicted in Fig. 2. A voltage amplitude of “OUTPp” and “OUTMp” has 4 combinations of \((V_{i3}, 0)\), \((V_{i1}, 0)\), \((0, V_{i3})\) and \((0, V_{i1})\), which are corresponding to the driving current of \((3^*Id, 0)\), \((Id, 0)\), \((0, 3^*Id)\) and \((0, Id)\), respectively.

![Fig. 2. Internal clock and data generator](image2)
To separate the state of the combinations, a reference voltage \( V_{i3} \) is prepared by \( I/V \) conversion of a reference current \( 2^*Id \) and utilized as offset voltage in a couple of comparators to recognize the voltage transition between \( V_{i3} \) and \( V_{i1} \) at “OUTPp” and “OUTMp”. The offset voltage is applied to the plus input of both comparators, then the comparators’ outputs \( (pclkp, pclkm) \) have a duty cycle offset, i.e. wide high and narrow low. Therefore, the internal clock signal \( (inpclk) \) also has the duty cycle offset of narrow high and wide low through the NAND cell.

To adjust the duty cycle, the Duty Corrector is applied to generate an internal clock \( (pclk) \) from “inpclk” as depicted in Fig. 1. This duty correction is performed with referencing an internal data \( (pdata) \). This “pdata” is a simply delayed version of the internal data signal \( (inpdata) \) by the Delay Adjuster, which is produced by a non-offset comparator in Fig. 2. Therefore, “pdata” has much better duty cycle than “pclk”, and can be used as the reference for the duty correction of “pclk”.

The Phase Comparator in Fig. 1 compares rising and falling edges of “pdata” and “pclk”, and changes the digital code \( (code1) \) according to the comparison results until the duty cycle of “pclk” becomes almost equivalent to “pdata”. The Duty Corrector switches internal delay paths in accordance with “code1” and changes the pulse width of output signal for the duty correction. Another digital code \( (code2) \) is also generated through the comparison results and used to switch the delay paths in the Delay Adjuster to set suitable latch timing between “pdata” and “pclk” for Serial-to-Parallel Converter.

### 2.2 Timing margin degradation by the internal data

In this scheme, “pclk” is adjusted with referencing “pdata”, because a signal quality of “pdata” is much better than “pclk” thanks to the non-offset comparator. However, a systematic timing offset still exists in this scheme as expressed below.

Figs. 3(a) and 3(b) illustrate “OUTPp” and “OUTMp” at all cases of transmitted data transition (0 to 1, or 1 to 0) with considering voltage amplitudes of \( V_{i1} \) and \( V_{i3} \), which are related to the driving current of \( Id \) and \( 3^*Id \), respectively. As shown in the figures, there are 4 cases (a through d) as combinations of data polarity (0 and 1) and signal amplitude \( (V_{i1}, V_{i3} \text{ and } 0) \). Other cases are just for “inpclk” generation by crossing the reference voltage \( (V_{i2}) \) between 2 levels \( (V_{i1} \text{ and } V_{i3}) \), which is a result of changing the driving current between \( 3^*Id \) and \( Id \). These cases are not critical timing for data acquisition because no data polarity is changed.

Figs. 3(a) and 3(b) depict data transition from \( V_{i3} \) to \( V_{i1} \) and from \( V_{i1} \) to \( V_{i3} \), respectively. The data trigger points are marked as a blue square. The comparisons for the cases of a through d clarify that a systematic timing offset exists in this scheme due to unbalanced signal amplitude of \( V_{i1} \) and \( V_{i3} \), i.e. \( V_{i1} \) and \( 3^* V_{i1} \). This timing offset is illustrated as blue and white squares in Fig. 3(b), and causes improper duty cycle in “inpdata”. This duty cycle offset is much better than “inpclk” which comes from the offset comparators. However this timing offset may deteriorate the eye opening of “inpdata”, then degrades the timing margin for data latching between “pdata” and “pclk”.

On the other hand, a timing offset of the clock trigger point (red circle in Fig. 3) is negligible compared to an output timing offset of the offset comparators in...
Fig. 2. The output timing offset of the offset comparators can be adjusted by the Duty Corrector and the Delay Adjuster with referencing “pdata” as described above.

Therefore, the timing offset for “inpclk” can be compensated, if the trigger point for “inpdata” is stabilized.

![Diagram](image)

(a) Late Data Trigger Point (case a and b)

(b) Fast Data Trigger Point (case c and d)

Fig. 3. Data transition cases in the current mode interface

3 Circuit implementation

As depicted in Fig. 2, the offset comparators are used to separate signal amplitudes ($V_{i1}$ and $V_{i3}$) of “OUTPp” and “OUTMp”. Therefore, the comparators’ outputs (pclkp and pclkm) can indicate voltage states of “OUTPp” and “OUTMp”.

Table I shows signal states of “pclkp”, “pclkm”, “inpdata” and “inpclk” in each case (a through d). As shown in this table, the combination of “pclkp” and “pclkm” is (0,1) or (1,0) at the large amplitude ($V_{i3}$) and (1,1) at the small amplitude ($V_{i1}$), respectively. To compensate timing offset between the blue and white squares in Fig. 3(b), a proper delay should be added onto “inpdata”, when the data transition starts from the small amplitude ($V_{i1}$) situation (case c and d). This situation can be expressed by that “pclkp” and “pclkm” are waiting at (1,1).
In other situations, any delay is not added. The proper delay can be estimated through the timing gap between the blue and white squares in Fig. 3(b).

Table 1. Signal states of comparator results

| Case   | a     | b     | c     | d     |
|--------|-------|-------|-------|-------|
| inpdata| 1     | 0     | 0     | 1     |
| OUTPp  | $V_{i3}$ | 0     | 0     | $V_{i1}$ | 0     | 0     | $V_{i3}$ |
| OUTMp  | 0     | $V_{i1}$ | $V_{i3}$ | 0     | 0     | $V_{i1}$ | 0     |
| pclkp  | 1     | 1     | 0     | 1     | 1     | 0     | 1     |
| pcklm  | 0     | 1     | 1     | 1     | 1     | 1     | 0     |
| Proper delay | not added | not added | added on transition | added on transition |

Fig. 4 depicts a circuit diagram for the timing offset compensation. The concept is that the proper delay is added onto a “inpdata” path at the situation of the signal transition from the small amplitude ($V_{i1}$) to the large amplitude ($V_{i3}$). Namely, when “pclkp” and “pcklm” are in the (1,1), the proper delay is applied onto the “inpdata” path by switching an input node from 0 to 1 at the MUX. As depicted in the figure, an amount of the proper delay is programmable by external digital codes (2bit). Using a decoding result of the codes, the delay amount can be adjusted by selecting from 4 sets of pre-determined delay based on actual measurements. The timing offset compensation circuit has just additional 18 gates (calculated by standard 2 input NAND equivalent) compared to previous transceiver [1].

4 Measurement results

A test-chip has been fabricated by in a 0.18-µm and 5 metal layer CMOS technology. The proposed timing offset compensation circuit has been additionally
implemented in the previous design [1]. Fig. 5 shows the internal data eye opening of “pdata” through an experimental monitor pin. A bathtub curve is also shown in accordance with the data eye opening.

The driving current (Id) is 150 µA without the timing compensation circuit through 7.5 cm transmission line in Fig. 5(a). A bias current (Ib) of the I-V converter is set to 400 µA. As shown in the figure, 0.6UI is obtained at criteria of 10E-12 BER.

![Image](a) Without the Timing Offset Compensation

![Image](b) With the Timing Offset Compensation

Fig. 5. Internal data eye measurements

Fig. 5(b) exhibits the internal data eye opening of “pdata” with the timing offset compensation circuit. Other conditions are same as Fig. 5(a). As shown in this figure, larger data eye opening has been achieved, and additional 0.1U has been gained by the timing offset compensation circuit. In this measurement, the pre-determined delay is set to about 150 ps by digital codes.

The figures show that the signal quality of “pdata” has been significantly improved. As a result, a timing margin between “pdata” and “pclk” has been enhanced because the duty correction and delay adjustment are done with referencing “pdata”. This signal quality improvement affects directly to the timing margin enhancement between the internal clock and data.

Fig. 6 shows measurement results using two circuit settings. In Setting 1, the bias current (Ib) and the driving current (Id) are set to 400 µA and 150 µA respectively. In Setting 2, Ib and Id are set to 550 µA and 200 µA. In Setting 1, the possible length of transmission line has been improved from 5 cm to 7.5 cm thanks to the timing offset compensation circuit. In Setting 2, the possible length has enlarged from 7.5 cm to 11.5 cm.
5 Conclusion

The proposed circuit compensates the timing offset which comes from unbalance driving current, then enhances timing margin between internal data and clock via improvement of the internal data eye opening. The timing offset compensation circuit is constructed by adding just 18 gates of combination logic, and its power increase is negligible. As the results, stable data communication has been achieved through about 50% longer transmission line compared to previous transceiver [1] without power penalty.

Therefore, this work has a significance that small additional logic can make the transceiver to be applicable to recent tablet PCs in 3G/4G LTE era by achieving longer and low power data transmission.

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