Harmonic mitigation technique using active three-phase converters utilised in commercial or industrial distribution networks

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Abstract: Current harmonics generated by adjustable-speed drives (ASDs) are one of the main power quality concerns in commercial and industrial distribution networks due to a high number of ASDs. These harmonics affect the grid power quality, instability, resonances, and power losses. Therefore, different harmonic mitigation strategies using active front end have been proposed to tackle this issue. However, due to the cost-effectiveness, conventional front end such as diode rectifier is still recommended in industries for a broad range of three-phase power electronics systems. Thus, in this study, a new DC modulation method is proposed using three-phase diode rectifier with controlled DC-link current (boost converter) for grid harmonic elimination approach. Simulations and experiments have been carried out to validate the proposed concept that a selective harmonic can be eliminated from the grid using the developed strategy.

1 Introduction

The utilisation of power electronics based devices in the power distribution network has been increased in the past decades. The demand to improve machines control, efficiency, and energy conservation are the main reasons behind employing power electronics devices [1]. The motor drive is one of the applications that have faced vast utilisation of power electronics. It has been estimated that around 43% of the global electrical power is consumed by motor drives, where 60% of these drives belong to industrial sector [2]. Thus, power electronic converters have been used to improve motor drives efficiency and control. Adjustable-speed drive (ASD) has the ability to improve energy efficiency by adjusting speed and torque based on load demand [3]. However, using power electronic switching devices makes ASDs one of the main sources of harmonics in distribution networks [4–7]. These harmonics lead to power losses in the system components such as cables and transformers.

The ASD topology is mainly based on two stages as shown in Fig. 1. The first stage, called front end, converts AC voltage to DC. At the second stage (rear end), DC voltage is converted back to an AC voltage with desired magnitude and frequency [7]. A DC-link capacitor is installed in the DC side to keep the DC voltage constant and reduce the ripples. To reduce the current harmonics in the grid side, different filter topologies have been used in the front end. These topologies need to comply with recommended harmonic standards and are chosen based on the load power, cost, and reliability.

Active front end (AFE), which is based on bidirectional switches, can reduce input current harmonics by shaping the current signal as close as possible to sinewave [8–10]. However, its control complexity and high cost have made it an uncommon choice in ASDs. Another topology is phase-shifting transformer, which can increase the number of AC pulses to improve the input current quality [11–13]. The main drawbacks of this technique are high cost and size of the system, which make it unsuitable for high-power rectifier applications. Thus, conventional three-phase diode bridge rectifier (DR) is still recommended for a broad range of ASD applications due to its simplicity, low cost, and reliability. Although, DRs with passive filter (DC or AC choke types) have the problem of load-dependent current harmonics. That is, at partial power, where ASDs normally operate, current total harmonic distortion (THD) drastically increase. Hence, replacing the passive filter by electronic inductor (EI) can resolve this issue. The EI is a technique based on utilising a boost converter in the DC side and capable of improving THD [14].

Notably, it has been found that the phase angles of some of the low-order harmonics (5th and 7th) are counter phase in three-phase and single-phase diode rectifiers equipped with passive filters [15]. Consequently, a right combination of single-phase and three-phase diode rectifiers can help to mitigate some of the current harmonics at the point of common coupling (PCC) [16]. However, single-phase diode rectifier with a passive filter has been widely replaced by power-factor-correction (PFC) topology. PFC, which is based on utilising boost converter in the DC side, boosts the DC-link voltage and shapes the input current to a sinewave. Thus, harmonic cancellation between single- and three-phase rectifiers no longer exists. Hence, current harmonics generated by three-phase rectifiers need to be mitigated by other suitable methods.

According to IEC 61000-3-12 standard [17], it has been discussed by many researchers that the phase-angle value of the 5th harmonic at different grid locations has been changed. The nature of the phase-angle variation, however, is not discussed as it depends on many factors such as the penetration level of single-phase systems with PFC or passive filters. On the other hand, the penetration level of the exiting three-phase converters designed based on IEC 61000-3-12 is significantly high in low-voltage (LV) distribution networks. Thus, new equipment needs to be introduced, as single-phase, conventional converters are being replaced by PFC circuits.

A harmonic elimination technique in three-phase diode rectifier with EI is introduced in [18, 19], where a modulated current is applied to the boost converter to achieve selective harmonic elimination. This technique is further expanded to be used in a system with a combination of DR and SCR units in [20]. Suitable modulation parameters for each unit and right firing angle for SCR units can result in specific harmonic mitigation as well as low THD, at the PCC [21, 22]. However, in industrial grids, other non-
linear loads with different filtering topologies may exist, which can increase current harmonics at the PCC. Another issue is that using SCR can worsen the displacement factor.

For three-phase ASD systems, some techniques have been proposed in the literature to reduce the input current harmonics [23–25]. These techniques, however, target harmonic reduction at the unit level. For instance, AFE, Vienna rectifier, and Swiss rectifier presented in [24] can improve the input current quality but these techniques are uncommon choices in ASDs due to their complexity, a high number of active and passive components, and high cost. Additionally, active harmonic filtering can be used to mitigate harmonics caused by conventional drives as discussed in [8] but it requires a high number of switches and control system. Besides, international standards allow relatively high THD in ASD systems, which make bridge diode rectifier a preferred choice in ASD systems. For single-phase systems, PFC is used as harmonics mitigation for other non-linear loads, which are connected at the same PCC [26–28]. For instance, in [26], the PFC is used as a harmonic mitigation function in telecommunication applications, which have several single-phase rectifiers connected at the same PCC. This method has significantly improved grid power quality. However, in many applications, the three-phase rectifier system is required, which makes it impossible to use PFC for harmonics mitigation.

The existing literature indicates that there is a gap in the application of diode rectifiers with EI to mitigate harmonics in multi-rectifier systems. Thus, in this paper, a modified current modulation technique is proposed for a three-phase diode rectifier using EI, which can compensate a certain current harmonic from the grid while delivering the desired power to the load. The advantage of the proposed technique is its ability to control the magnitude and phase angle of a specific harmonic. Therefore, with the modified technique, certain current harmonic with a specific magnitude and phase angle is injected to the grid for harmonic cancellation at the PCC. The proposed modulation and control technique is a novel method to mitigate grid current harmonics generated by other conventional ASDs in commercial and industrial distribution networks. The main aim of the proposed technique is to mitigate current harmonics generated by conventional DRs with passive filters connected to the same PCC. To verify the effectiveness of the proposed method, different cases are modelled in simulation software and practically implemented in the laboratory. Both stiff and weak grids have been considered to examine the proposed technique.

The rest of this paper is organised as follows. The harmonics emission of three-phase diode rectifier at unit and system levels is analysed in Section 2. Details of the proposed technique to mitigate harmonics and its principles of operation and implementation are then discussed in Section 3. Next, Section 4 explains the controller and hardware implementation of the technique. Simulation and practical results are then presented and discussed in Section 5. Finally, Section 6 concludes the research outcomes of this paper.

2 Harmonics analysis of DR with passive filter

To mitigate current harmonics caused by DRs with passive filters, magnitude and phase angle of these harmonics need to be first identified. Current harmonics behaviour can be changed from unit level to system level due to the possibility of harmonics mitigation between the units. Also, the level of load power can influence the harmonic behaviour of the DR with passive filter. Therefore, low-order current harmonics and THD are evaluated in both unit and system levels in this section as follows.

2.1 Harmonic analysis at the unit level

Harmonics magnitude and phase angle of DR with passive filtering depend on the load profile and need to be studied at different power levels. To illustrate that, Fig. 2 shows the input current waveform in different power levels of 25, 50, and 100% of 11 kW rated power in a DC choke. For these three cases, the harmonics up to the 13th order and THD, have been calculated as given in Table 1.

It can be seen from this table that phase angle of the fifth harmonic is in the range of 110–125°, which has a 15° variation at different power levels. Also, phase angle of the seventh harmonic varies by 38° between 240° and 278°. Notably, the 13th harmonic has the highest range of phase-angle variation around 115°. To fully eliminate an existing harmonic, another harmonic with the same frequency and magnitude but 180° phase shift needs to be injected to the PCC. However, any phase-angle difference between the two harmonics higher than 120° can still be considered as harmonic mitigation, as the sum of the two vectors is smaller than the larger vector. In the next step, a system with several DR units is considered to investigate the harmonics behaviour and mitigation possibility in the system level as follows.

2.2 Harmonic analysis at the system level

To study the phase-angle range of current harmonic of DR with passive filter, a system with 20 parallel rectifiers as shown in Fig. 3 has been modelled and simulated in MATLAB/Simulink. The system includes a three-phase voltage source of 11 kV representing medium-voltage level connected to 11 kV/380 V Y–Y transformer with both leakage reactance and resistance of 0.02 pu. The line section connecting the LV side of the transformer to loads is
Table 2 Low-order harmonic and THD, at the system level in different cases

| Current harmonic | Case | 1 | 2 | 3 | 4 |
|------------------|------|---|---|---|---|
| $I_5$, %         |      | 32.1 | 43.4 | 34.4 | 45.8 |
| $\Theta_5$, deg  |      | 122 | 118 | 101 | 108 |
| $I_7$, %         |      | 11.3 | 21.5 | 9.72 | 20.2 |
| $\Theta_7$, deg  |      | 208 | 243 | 195 | 237 |
| $I_{11}$, %      |      | 7.5 | 7.5 | 6.3 | 7.3 |
| $\Theta_{11}$, deg |    | 288 | 311 | 228 | 270 |
| $I_{13}$, %      |      | 4.20 | 4.96 | 3.04 | 4.22 |
| $\Theta_{13}$, deg |    | 310 | 8.30 | 262 | 352 |
| THD, %           |      | 35.5 | 49.7 | 36.6 | 51.0 |

As it can be seen from Table 2, the phase angle of the fifth harmonic at the system level has not changed much compared with its phase-angle value at the unit level. However, the phase angle at the system level has shifted clockwise around 35° for the seventh harmonic, and around 100° for the eleventh harmonic. Notably, the 13th harmonic has a high phase-angle variation at the system level similar to the unit level. Finally, it can be noted that THD, at the system level has decreased compared with the unit level at all operation power levels.

3 Modified current modulation technique: shifted pulse position

In a three-phase DR with EI as shown in Fig. 4a, the DC can be modulated by controlling the input current of the boost converter [29]. This DC modulation technique can be used to control the input AC harmonics.

3.1 Principle of operation

The pulses created by adding $I_{dc1}$ and $I_{dc2}$ can be shifted to start at 30° or end at 150°. For that purpose, $\delta$ has been defined as the delay shown in Fig. 4b. To illustrate, Fig. 5 shows the effect of the proposed technique on low-order harmonics (5th and 7th) when $I_{dc2} = 0.8 \times I_{dc1}$ and $\delta = 30^\circ$, whereas $\delta$ is changing between $-15^\circ$ and $15^\circ$. Fig. 5a presents the low-order harmonics when $I_{dc2} = 0.8 \times I_{dc1}$ and Fig. 5b presents the low-order harmonics when $I_{dc2} = -0.8 \times I_{dc1}$. These figures show that the phase angles of the low-order harmonics can be controlled by changing $\delta$, which confirms that the modified current modulation technique can mitigate current harmonics at the PCC.

Although this example is to illustrate the proposed technique, any magnitude and phase angle can be injected for a specific harmonic based on (2). As the objective of this technique is to mitigate a specific harmonic from the PCC, (2) can be solved to inject the same amount of that harmonic with a counter phase. It was shown in the previous section that the main harmonics on the three-phase systems are 5th and 7th. Thus, having a unit with the proposed technique connected to the same PCC would be beneficial to eliminate one of these two harmonics.

This technique aims to mitigate specific low-order current harmonics in a grid. Although this technique can mitigate current

Fig. 4 Three-phase rectifier with EI
(a) System diagram, (b) Phase-a current and modulated DC waveforms with the proposed technique

Fig. 5 Variation of low-order current harmonics with $\delta$ when $I_{dc1} = 1$ pu and $\theta = 30^\circ$
(a) $I_{dc2} = 0.8$ pu, (b) $I_{dc2} = -0.8$ pu

modelled as a series resistor and inductor (RL) with 0.01 Ω resistance and 20 µH inductance. The rectifiers have either DC or AC chokes and are in five different power levels of 1 kW (units 1–4), 4 kW (units 5–8), 11 kW (units 9–12), 22 kW (units 13–16), and 30 kW (units 17–20).

Table 2 shows the measured magnitudes and phase angles of different current harmonics at the PCC, that is, the summation of the currents of all the units for the following cases:

(i) DC choke converters operating at full load (272 kW).
(ii) DC choke converters operating at 50% load (136 kW).
(iii) AC choke converters operating at full load (272 kW).
(iv) AC choke converters operating at 50% load (136 kW).

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harmonics up to 2 kHz, higher-order harmonics in the range of 2–150 kHz can be generated due to the switching frequency. This has two main sources: differential and common mode noises. The whole ASD system parameters such as AC motor, cable, Electromagnetic interference (EMI), and DC-link filter can generate different resonances creating different harmonics. Thus, the proposed ASD can generate some differential mode harmonics around the switching frequency and its multiples, which can be mitigated by EMI filter.

Additionally, the oscillations and unbalance load condition coming from the rear-end inverter are the main sources of interharmonics in ASDs. Hence, the resonance characteristic of the employed intermediate circuit plays an important role in injecting the interharmonics to the grid. However, as it has been discussed in [30] that employing EI as an intermediate circuit will attenuate the low-frequency oscillations coming from the inverter side, which will reduce the input current interharmonics. Implementation steps of the proposed method are presented in the coming section.

3.2 Implementation of DC control

To implement the proposed technique, a boost converter is used to control the DC-link current. The boost converter connected to the DC link of three-phase rectifier (EI) can control the current harmonics independently while boosting the DC voltage [31]. In this way, the DC-link current is controlled to create the signal shown in Fig. 6a. As can be seen from this figure, a square pulse is repeated every 1/6 of the period, where the pulse parameters are pre-programmed based on harmonics injection by solving (2).

Fig. 6 DC-link current modulation and generated AC-side currents

(a) DC, (b) Three-phase AC

\[ L_{dc} = \frac{V_o D (1 - D)}{f_{sw} \Delta I_L} \]  

where \( V_o \) is the DC output voltage, \( D \) is the duty ratio, \( f_{sw} \) is the switching frequency, and \( \Delta I_L \) is the inductor peak-to-peak current. Notably, a boost converter consists of two main semiconductor devices, a switch and diode, and it can be applied to low- and medium-power applications. The optimum switching frequency can be achieved to control power quality (ripple and harmonics at the switching frequency) and efficiency (switching losses). Additionally, the boost converter filter should also be optimised as well to control high-frequency harmonics (mainly above 9 kHz). The target of this paper is the ASDs operating at low- and medium-power levels, which comply with the IEC 61000-3-2 and 12 standards. Therefore, the proposed technique aims at the ASDs in the range of 0–75 A input current connected to the LV distribution system. The details of the system control and hardware setup are discussed in the next section.

4 Control and hardware setup

To implement the proposed technique, a proper controller is first designed using MATLAB control system designer. Then, it is implemented in the hardware. Design details are presented as follows.

4.1 Boost converter control

To ensure accurate tracking of the modulated current, a fast and reliable current controller is required. In this paper, a hysteresis current controller with a fast response is adopted. The idea of this controller is based on limiting the current between the hysteresis bands (minimum and maximum) of the current reference. Fig. 7 depicts the general block diagram of the system with the control system.

To implement a hysteresis controller, at the first stage, a proportional–integral (PI) controller is used to generate the current reference signal from the voltage error. Afterwards, the generated current reference signal is multiplied by a modulation signal, which was described in the previous section. A three-phase PLL block is used to synchronise the modulation signal with the grid voltage (\( V_{gs} \)). Eventually, a hysteresis function is utilised to generate the duty cycle of the converter switch.

The hysteresis block is extremely fast, so its transfer function can be neglected in the overall system. Therefore, to design the PI controller, the open-loop transfer function can be considered as the ratio between \( V_{gs} \) and \( i_L \). This transfer function can be obtained as given in the equation below [32]:

\[ G_{open\text{-}loop} = \frac{V_{gs}(s)}{I(s)} = \frac{1}{2} \frac{V_{dc}}{R/2 + \frac{R}{2} + \frac{1}{C}} \]  

Then, the parameters of the PI controller can be easily calculated using the root locus of the open-loop transfer function. Fig. 8 demonstrates the root locus and step response of the overall system.

Having designed the PI controller, the overall control system should be programmed and downloaded onto a microcontroller. It should be highlighted that digital implementation of an accurate
hysteresis controller requires a high sampling frequency of the voltage and current signals (or equivalently, the low cycle time of the microcontroller), which restricts the volume and complexity of the control programme. To overcome this problem, the programme is written in two different interrupt routines, one for the PLL with a very low sampling frequency (10 kHz) and another routine for the PI and hysteresis blocks with a high sampling frequency (300 kHz). Furthermore, a pulse-width modulation unit of the microcontroller is utilised to synchronise the analogue-to-digital units with the output pulse generation unit.

4.2 Hardware setup
The hardware prototype of the proposed method (EI unit) is shown in Fig. 9. A three-phase variac is used to step down the grid voltage to 57.7 V \((V_{an})\) and SEMIKRON-SKD 30 is used for the three-phase rectification. For the boost converter, SEMIKRON-SKM75 is employed as the insulated-gate bipolar transistor (IGBT) switch, SKYPER 32 R as the IGBT driver, and Texas instrument F28379D as the controller of the boost converter. Current and voltage probes are used for control and measurement purposes. As the current is controlled with a hysteresis controller, the average switching frequency of the boost converter can be calculated from (3). In this case, the current ripple is set to 1.5 A and the inductor size is 2 mH. Thus, the average switching frequency is 14.6 kHz. Also, the output power is set to 810 W as the full power; hence, the average current of the inductor is around 6 A.

5 Results
A system with two units as shown in Fig. 10 is implemented to validate the proposed technique. As shown in this figure, Unit 1 (U1) is a three-phase bridge rectifier with passive filter (DC choke) and Unit 2 (U2) is based on EI to apply the modulated current. As it has been discussed in Section 2, the two major harmonics of U1 that need to be mitigated are the 5th and 7th with phase angles at around 125° and 240°, respectively. Thus, U2 is employed with the proposed technique to mitigate harmonics at PCC generated by U1. To validate the proposed technique, three cases are considered in this section: case 1 is based on flat DC for comparison, case 2 targets elimination of the 5th harmonic from PCC, and case 3 is to eliminate the 7th harmonic. Moreover, to validate the proposed technique under different grid conditions, stiff grid with \(L_s = 20 \mu H\) and weak grid with \(L_s = 0.7 \text{mH}\) are evaluated. Different simulation and experimental tests are examined to verify the effectiveness of the proposed technique.

5.1 Simulation results
The system is modelled and simulated in MATLAB/Simulink, where the parameters are set similar to the hardware setup presented in Table 3. Hence, for comparison, Fig. 11 shows the result of case 1 when U2 has a flat DC (non-modulated current) in a stiff grid. As it can be seen from Fig. 11b, PCC current \(i_g\) contains 26% of the 5th harmonics and 16.2% of the 7th harmonics. Under same grid conditions, Fig. 12 shows the results of case 2 when U2 is programmed to mitigate the fifth harmonic from the PCC by injecting that harmonic with a magnitude similar to U1 but an opposite phase angle. As it can be seen from Fig. 11b, PCC current \(i_g\) contains 26% of the 5th harmonics and 16.2% of the 7th harmonics. Notably, compared with case 1, the 7th, the 11th, and the 13th harmonics
have been increased resulting in 46% THD, at the PCC. These higher-order harmonics are caused by the high pulse waveform of the AC of U2.

It is worth mentioning that the majority of ASDs with low- (0–16 A per phase) and medium-power (16–75 A per phase) are complied with IEC-61000-3-2 and 12 standards, respectively. The proposed technique aims to mitigate harmonics below 2 kHz and keeps the THD around 30% at the system level. This is due to the fact that other conventional drives, which are utilised in industrial networks, generate low-order harmonics, and increase the harmonic level and THD in the power system. The EI can control individual harmonics or THD at 30% to comply with standards and regulations at different power levels, while the minimum THD generated by a conventional ASD based on IEC standard can be 48% at full power and much higher at a partial power.

Fig. 13 shows the results of case 3 when U2 is controlled to mitigate the 7th current harmonic from the PCC. As it can be seen from Fig. 13b, the 7th harmonic of \( i_g \) has been eliminated and dropped to only 1%. In this case, THD of \( i_g \) is 36%, which is similar to case 1 and lower than case 2.

From the presented results so far, it can be seen that the proposed technique works effectively for stiff grid condition. To investigate the weak grid condition, Fig. 14 presents the simulation results of all three cases under that condition. Fast Fourier transform (FFT) of the signal in this figure confirms the expected harmonic mitigation for both cases 2 and 3, where case 2 reduces the 5th harmonic to around 4% and case 3 reduces the 7th harmonic to around 4.4%. Notably, applying current modulation in the weak grid increases the PCC voltage harmonics due to the impact of high grid impedance.

As ASDs work at partial power most of the time, the proposed technique needs to be also tested under that condition. For that purpose, Fig. 15 presents the simulation results when both units operate at 50% (405 W) and U2 current is modulated to mitigate the 5th harmonic (case 2). In this case, the phase angle of the 5th harmonic injected by U2 is the same as before; however, as the power is 0.5 pu, the magnitude is halved this time. It is evident from Fig. 15b that the 5th harmonic of \( i_g \) has been again reduced. The overall level of harmonics, however, is higher in this case, which could be related to the partial power operation of the units.

Another aspect of EI behaviour with the proposed method, which might be of interest for researchers, is its interharmonics emission behaviour. There are different sources of interharmonics

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**Table 3 System parameters**

| Symbol | Parameter | Value       |
|--------|-----------|-------------|
| \( V_{abc} \) | grid-phase voltage | 58 Vrms |
| \( f_g \) | grid frequency | 50 Hz |
| U1 | filter inductor and capacitor | 1.8 mH, 570 µF |
| | output voltage | 200 Vdc |
| | average switching frequency | 14.6 kHz |
| | PI controller | 0.12, 18 |
| | hysteresis band | 1.5 A |
| | rated output power | 810 W |

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Fig. 11 Simulation results of case 1, U2 with flat DC, both units at full power in a stiff grid
(a) Time domain, (b) Harmonic contents of phase-a currents of U1, U2, and grid

Fig. 12 Simulation results of case 2, U2 is mitigating \( i_g \) 5th harmonic, both units at full power in a stiff grid, \( I_{dc1} = 1 \) pu, \( I_{dc2} = -0.85 \) pu, \( \alpha_1 = 42^\circ \), and \( \alpha = +5^\circ \)
(a) Time domain, (b) Harmonic contents of phase-a currents of U1, U2, and grid

Fig. 13 Simulation results of case 3, U2 is mitigating \( i_g \) 7th harmonic, both units at full power in a stiff grid, \( I_{dc1} = 1 \) pu, \( I_{dc2} = 2.2 \) pu, \( \alpha_1 = 45^\circ \), and \( \alpha = -6^\circ \)
(a) Time domain, (b) Harmonic contents of phase-a currents of U1, U2, and grid
in motor drives such as oscillations and unbalance load condition coming from the inverter side or multicycle and firing-angle control at the grid side. Hence, the resonance characteristic of the employed intermediate circuit plays an important role in injecting the interharmonics to the grid. As it has been discussed in [30], using the EI as an intermediate circuit can attenuate the inverter-side low-frequency oscillations. Therefore, the proposed technique will not have much impact on interharmonics since it relies on modifying the EI control.

To investigate the effect of the proposed modulation technique on the input interharmonics, FFT analysis is conducted for all three cases. Fig. 16 shows the interharmonics of unit 2 (EI unit) for all three cases under a stiff grid. As can be seen from Fig. 16a, the interharmonics for case 1 (non-modulated current) are mostly <0.02% of the fundamental. The modulation technique has a slight effect on interharmonics as it can be seen from Figs. 16b and c. The interharmonics of case 2 (5th harmonic cancellation) are mostly <0.1% and for case 3 <0.07%.

Further analysis can be done for high-frequency (9–150 kHz) behaviour of the system with the proposed technique. The high-frequency distortions (9–150 kHz) are mainly determined by the switching frequency and has two main sources, differential, and common mode noises. All the system parameters such as AC motor, cable, EMI filter, and DC-link filter can generate different resonances generating different harmonics. In this paper, the EI is designed with the switching frequency around 14.6 kHz and it has some harmonics around multiples of this frequency. On the other hand, the proposed modulation technique has a high impact on low-order harmonics (below 2 kHz) and it has been shown by simulation and practical results in this paper.

For more details, high-frequency distortions generated by the switching frequency is analysed for all three cases (unit 2). Fig. 17 presents the high-order harmonic distortions for all the cases are almost similar, where the distortions concentrations are around 14.6 kHz ($f_{sw}$) and 29 kHz (2 × $f_{sw}$).

5.2 Practical verification

To verify the proposed technique in practical condition, the two units shown in Fig. 10 have been implemented in the laboratory. Fig. 18 shows the built prototype of the system, where the employed parameters are given in Table 4. The practical tests have been carried out on the implemented system for all three cases, similar to the simulated ones, with system parameters presented in Table 3. Similar to simulation results, the first case is based on flat DC for U2, which means the system operates normally without harmonic mitigation at PCC. The test results for case 1, presented in Fig. 19, show that $i_g$ has 24% of 5th and 10% of 7th harmonics.
It is clear from the plots that the practical results are similar to the simulated results under a weak grid. The reason behind that is in practical verification, a three-phase variac is used to step down the grid voltage, which increases the grid impedance and makes the grid condition similar to a weak grid.

In the second case, $U_2$ is controlled to mitigate the 5th harmonic of $i_g$, as shown in Fig. 20. It is notable that the 5th harmonic has significantly decreased to 3.4% at the PCC with a grid current THD of 30%. Fig. 21 shows the results of case 3, where $U_2$ is controlled to mitigate the 7th harmonic of $i_g$. In this case, the 7th harmonic has been effectively reduced to 3.6%.

Finally, the three-phase currents plot of $i_g$ for case 2 is presented in Fig. 22, which shows that all three-phase currents have symmetrical harmonics spectra.

To sum up, both simulation and experimental results have validated the proposed technique for grid harmonics mitigation. The proposed technique has been tested under different grid conditions, where the results proved the effectiveness of the proposed harmonic mitigation technique using EI topology.
6 Conclusion

This paper proposes a strategy to modulate the DC in three-phase DR with a boost converter known as EI to reduce current harmonics at the grid side generated by other non-linear loads. EI converter operates as an active filter integrated into frequency converters and can be utilised in industrial networks, where a high number of conventional motor drives are installed. The proposed strategy is based on controlling the shape of the DC boost converter current to inject current harmonics with selective magnitude and phase angle to mitigate the grid harmonics.

Both simulation and practical results have validated that the proposed strategy can be used to eliminate and reduce various current harmonics at the grid side.
current harmonic components and THD, in a grid. Two different case studies have demonstrated that the proposed strategy can be used to eliminate specific harmonic at the grid side.

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