High Density Integration of Semiconductor Optical Amplifiers in InP Generic Photonic Integration Technology

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Abstract—We present experimental studies of semiconductor optical amplifiers (SOA) with a high integration density in an InP generic photonic integration platform. We study the active-passive butt joint integration of dense arrays of active islands with widths ranging from 2 to 30 μm, and pitches ranging from 4 to 270 μm. We show that there is significant room for increasing the density of active island arrays while keeping a similar growth rate enhancement in between the active islands. The impact of narrow active islands on SOA performance is also studied with an array of Fabry-Pérot lasers fabricated in a commercial generic platform. We demonstrate the manufacturability of lasers with a pitch of 25 μm and evaluate individual device performance. Threshold currents and slope efficiencies are not impaired with narrow active island down to 6 μm, with values of 19–26 mA and 0.08–0.15 W/A respectively.

Index Terms—Butt-joint integration, generic photonic integration, high density, photonic integrated circuits, very-large scale integration.

I. INTRODUCTION

The increasing maturity of photonic integrated circuit (PIC) platforms is enabling the fabrication of more complex circuits [1]. Over the time, the record number of integrated components on a chip keeps increasing with new designs [2], [3], [4]. The high-complexity PICs find applications where a high number of parallel channels is key, such as optical phased arrays [5], photonic neural networks [6], or programmable photonics [7], [8]. Offering high integration density PICs is essential to increase performance for these applications (e.g. by parallelization) and enable novel applications in the future.

The use of high complexity PICs with a large number of components called for the development of versatile generic integration platforms [9], [10]. These generic platforms enable the integration of a set of individual building blocks (BBs) sharing the same standard fabrication process. The BBs can then be seamlessly combined in countless variations to build PICs for a broad range of applications. To provide comprehensive PICs, integration platforms including both active (which amplifies or absorbs light) and passive components are highly desirable.

Silicon-InP (Si-InP) hybrid solutions provides very high performance when a large number of passive components is needed thanks to low waveguide propagation loss and small passive device footprint [11]. But it comes with a cost from higher complexity of integration because of low-tolerance wafer or die bonding which can reduce the yield of fabrication. Thermal dissipation can also be a challenge depending on the hybridization technique used [12]. On monolithic InP integration, the direct integration of amplifiers and efficient phase shifters can compensate for higher passive waveguide loss by enabling compact designs for complex PICs [1], [5]. Together with the high maturity and yield of the technology, it enables complex and versatile designs on generic integration platforms [6], [13]. Besides, the combination of a fully fabricated InP die made in a versatile monolithic InP platform with high density Silicon photonics passive circuit can be beneficial for some applications [14]. Therefore, the development of both Si-InP hybrid and monolithic InP approaches can benefit PIC technologies overall.

For InP monolithic integration, several active-passive integration schemes have been developed (butt-joint regrowth (BJR), selective area growth, quantum wells intermixing, vertical twin waveguides, polarization-based integration scheme) [15], [16]. Among these techniques, the butt-joint regrowth offers both low footprint and high design flexibility, advantages which makes it widely used, with a pathway to high density integration [2], [16], [17], [18]. It is therefore the focus of this study.

When using a butt-joint regrowth technique, a growth rate enhancement (GRE) occurs due to the presence of a dielectric mask pattern during selective area epitaxy [19]. It locally increases the thickness of the regrown layers and modifies their material composition [20]. If not properly controlled, this modification...
of the core guiding layer can disturb the performance of some devices such as multimode interference couplers [21]. This issue is generally avoided in PIC platforms by placing devices at a far distance from each other (typically larger than one hundred micrometers) [22] to be able to integrate passive devices without too much performance change. However, this large spacing between active components limits significantly the capability for high density integration.

Recently, a new BJR fabrication scheme has been proposed to fabricate arbitrarily large areas of active material [23]. This method enables the fabrication of dense arrays of active devices. However, it requires additional lithography steps, and reduces the design flexibility by dedicating a large area to active devices only. For example, this prevents the design of interleaved arrays of active and passive devices.

In this paper we study the integration of dense arrays of active devices in a commercial InP PIC platform. In the first section, we characterize the GRE induced by arrays of active islands. We measure the regrown layer stack thickness in between active islands, and identify the improvements obtained by narrowing down the island dimensions. In the second section, we validate the possibility to use devices with narrow active islands through the design and measurement of a dense array of Fabry-Pérot lasers in a PIC generic integration platform.

II. HIGH DENSITY ARRAYS OF ACTIVE ISLAND

A. Growth of Active Island Arrays

An active-passive epitaxy regrowth process has been performed with arrays of active islands with widths ranging from 2 to 30 µm, and pitches ranging from 4 to 270 µm. Each active island was 500 µm-long in the waveguide direction and each array of active islands extended over 1 mm in the perpendicular direction to cover the precursors vapor-phase diffusion length. Fig. 1(a) shows the layout of an array of active islands of width 8 µm and gap 32 µm.

The active-passive butt-joint integration process of the SMART Photonics commercial generic PIC platform, described in [17], was used for this study. The active layer stack was first grown by metal-organic vapor-phase epitaxy (MOVPE). It consists of a 500 nm-thick active core layer including quantum wells, and a variable thickness of InP layer. On top of the active layer stack, a SiO₂ hard mask was patterned to define the active islands. Then, a selective wet etch was used to etch the full active layer stack. This was followed by the regrowth of the passive layer stack consisting of 500 nm of InGaAsP quaternary material with bandgap corresponding to a 1.25 µm wavelength (noted Q1.25), and a thin InP cladding layer. The Q1.25 layer serves as core layer for light propagation and matches the thickness of the active layer stack core layers for mode matching considerations. The epitaxial growth was performed at 650°C of temperature and 100 mbar of reactor pressure.

After the passive regrowth, the active island arrays were inspected under optical microscope. Fig. 1(b) shows the picture of an array of active islands of width 12 µm and gap 12 µm.

One can see on Fig. 1(b) the uniform green color of the flat active islands and the gradual color change of the material grown in between and around the array. This inhomogeneous color in the passive area is indicative of a thickness variation induced by GRE around the active areas. The grown wafer did not show visual defects around the active islands, even in the case of high densities of islands such as the one in Fig. 1(b).

B. Characterization of the GRE Between Active Islands

For each array, the surface topology has been measured with a profilometer across the center of the active islands. Fig. 2 shows an example of such profilometer measurement with an array of 8 µm-wide active islands separated by gaps of 32 µm. The SiO₂ hard mask was covering the top of the active islands during this measurement.

The thickness difference between the passive layer stack away from the active islands and the active layer stack plus the hard
Fig. 2. Profilometry of an array of active islands of width $= 8 \mu m$ and gap $= 32 \mu m$ after passive regrowth. The loading value indicates the maximum overgrowth measured in the middle of the gaps between active islands.

Fig. 3. Measured loading versus pitch for arrays made with different active island widths (Wa).

The measurement of the surface topology as described in Fig. 2 has been carried out for arrays of active islands with active widths ranging from 2 to 30 $\mu m$ and pitches between actives ranging from 4 to 270 $\mu m$ (close to the current standard pitch of 250 $\mu m$ in the SMART Photonics platform). For each array, the value of loading has been extracted. Fig. 3 summarizes the measured loading values, grouped by active island width (Wa).

The measurements show loading values ranging from 15 to 178 nm. This study shows that significant reduction of loading can be achieved by narrowing down the active island width. A reference sample was used to estimate the maximum GRE obtained for passive devices when staying within the design rules of the platform (minimum 40 $\mu m$ distance from the active island, and active island pitch above 250 $\mu m$). Fig. 4 shows the surface topology for a 270 $\mu m$ pitch between standard active islands, and shows a maximum GRE of 40 nm at a 40 $\mu m$ distance from the active islands. Since the platform guarantees passive device performance in this case, we consider the same amount of GRE as a reference in our study. With this target of 40 nm GRE, the results of Fig. 3 demonstrates that narrowing down the active islands from 20 $\mu m$ to 4 $\mu m$ allows a reduction of the pitch from 140 to 36 $\mu m$.
III. GAIN SECTIONS WITH NARROW ACTIVE ISLANDS

A study of single active device performance with narrow active islands in dense arrays has been carried out to validate the possibility to use such devices in a commercial platform.

A. Measurement Method

A chip with a dense array of Fabry-Pérot lasers has been designed and fabricated in a multi project wafer run using the commercial generic PIC process of SMART Photonics. The gain sections of the Fabry-Pérot lasers are designed using semiconductor optical amplifier (SOA) building blocks with active island widths ranging from 4 to 30 µm. The SOAs are grouped by lengths of 400, 500, and 600 µm in 3 arrays. The pitch of each array of SOAs is 75 µm, and the arrays are shifted by 25 µm with respect to each other. Each SOA is butt-coupled to a passive waveguides extended until the cleaved facets of the chip (the total cavity length is 4.6 mm), providing a Fabry-Pérot cavity with a 33 % of reflection on each side at the semiconductor-air interface. For each device, a shallow-etched waveguide with a 2 µm ridge width is used. The shallow waveguide structure, shown in Fig. 6, consists of a 500 nm-thick core (bulk InGaAsP material for the passive waveguides, and including 4 InGaAsP quantum wells in the center for the active waveguides). More details can be found in [17]. Fig. 5 shows the layout of the lasers and a photograph of a fabricated chip.

To characterize the laser performance, the chip was placed on a copper holder maintained at 18°C with a Peltier element and driven with a probe needle making contact with the metal pads at the edge of the chip. The connection to ground was made at the metallized back of the n-doped substrate. An integrating sphere was placed next to the chip facet to collect the output light. In total, 15 lasers from 2 different chips were measured. The two chips are identified with the names H7 and K11.

The lasers were driven one after another by applying a bias voltage up to 2 V (corresponding to current densities up to 13.8 kA·cm⁻²), using a Keithley 2602. The current and output power have been recorded and the measured data has been analyzed to extract the main characteristics. Out of the 15 lasers measured, only one did not show lasing behavior (6 µm-wide active island and 500 µm-long gain section). The reason for this has not been investigated.
B. Laser Performance

Fig. 7(a), (b), (c), and (d) show the summary of the extracted characteristics for each laser as a function of the active island width used for the SOAs. Fig. 7(a) presents the threshold current identified as the maximum of the second derivative of the measured power-current (L-I) characteristic. The slope efficiency reported on Fig. 7(b) is the maximum value of the first derivative of the L-I characteristic over a range of 1–5 mA above the threshold current. The series resistance presented in Fig. 7 is extracted from the derivative of the voltage-current characteristics at a current of 45 mA. Fig. 7(d) shows the voltage-current density (V-J) characteristics of all laser diodes at low values of current density.

For all lasers with active island width of 6 µm and above (except for one outlier), the threshold current is between 19 and 26 mA, the slope efficiency is between 0.08 and 0.15 W/A, and the series resistance at 45 mA is between 8.7 and 12.2 Ω. All V-J characteristics for these lasers are very close to each other around the turn-on voltage. The performance variation between devices of different active island widths is of the same order as the variations between same type of devices. In conclusion, no significant impact of the active island width is observed for this group of devices. The measurements of devices with 4 µm-wide active island show a different result compared to lasers with wider active islands. Their threshold current is significantly higher, with values from 28 to 40 mA, and their current density at low voltage is increased (e.g. by 1.20 to 1.35 kA/cm² at 0.8 V, see blue curves on Fig. 7(d)). This is likely due to the proximity of the non-ideal lateral active-passive interfaces, which induce leakage currents. The contrast between the performance of devices with 4 µm-wide active island and all other devices shows that this detrimental effect on laser performance only appears when using active islands narrower than 6 µm. This result demonstrates the manufacturability of Fabry-Pérot lasers with a pitch of 25 µm from 3 interleaved arrays with a pitch of 75 µm between gain sections. It is, to the best of our knowledge, the smallest pitch reported in literature for a laser array when using butt-joint regrowth.

Such a narrow pitch between SOAs enables design freedom for fabricating PICs beyond the appearance of other parasitic effects, such as thermal cross-talk. A previous study on the same platform showed that moderate thermal cross-talk occurs at a distance of 60 µm from an SOA operating at 100 mA (0.7°C increase) [24]. This level of cross-talk is not expected to have a detrimental effect on simultaneous device operation, but further considerations are needed when designing temperature-sensitive PIC functionalities.

IV. Conclusion

In this paper we studied the potential to increase the density of active devices in a commercial generic PIC platform. We first showed the impact of growth rate enhancement between active islands in arrays with pitches ranging from 4 to 270 µm. The thickness increase in between active islands could be significantly reduced by narrowing down the active islands width. As a result, a reduction of active island width from 20 to 4 µm enables a density increase by almost 4 times when keeping a 40 nm GRE. Moreover, we showed the characterization of individual lasers fabricated in a multi-project wafer run from a commercial platform with a pitch of 25 µm from 3 interleaved arrays with a pitch of 75 µm between gain sections. We concluded that device performance is uncompromised for SOAs with active island widths from 6 µm to 30 µm.

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