A Primer on Techtile: An R&D Testbed for Distributed Communication, Sensing and Positioning

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Abstract

The Techtile measurement infrastructure is a multi-functional, versatile testbed for new communication and sensing technologies relying on fine-grained distributed resources. The facility enables experimental research on hyper-connected interactive environments and validation of new wireless connectivity, sensing and positioning solutions. It consists of a data acquisition and processing equipment backbone and a fabric of dispersed edge computing devices, Software-Defined Radios (SDRs), sensors, and LED sources. These bring intelligence close to the applications and can also collectively function as a massive, distributed resource. Furthermore, the infrastructure allows exploring more degrees and new types of diversity, i.e., scaling up the number of elements, introducing ‘3D directional diversity’ by deploying the distributed elements with different orientations, and ‘interface diversity’ by exploiting multiple technologies and hybrid signals (RF, acoustic, and visible light).

Keywords — Testbed, 6G, Software-Defined Radio, Precision Time Protocol, Power-over-Ethernet, RadioWeaves

1 Techtile – A Teaser

As envisioned in [1], new wireless access infrastructures will be integrated in existing structures, bringing them in closer proximity of devices and eventually becoming truly ubiquitous. The Techtile infrastructure (Figure 1) is the first testbed capable of evaluating this RadioWeaves concept. To support this, the measurement room or –more general– the testbed, hosts 140 detachable tiles of equal size on the walls, floor, and ceiling. A versatile set of equipment can be mounted on these panels, effectively embedding the electronics into the room.

Figure 1: Left: Support structure (top view) – Right: Tile with embedded edge device. The support structure is designed to support 140 detachable panels.

The main technical challenges, in both the testbed and future distributed infrastructures, are the scalability and synchronization. In contrast to other testbeds [2]–[4], this testbed does not utilize dedicated connections for communication and synchronization to each processing point, i.e., –in our case– tile. The conventional approach to time synchronization requires all cables to have the same length, making deployment cumbersome...
and not scalable. In order to support high-speed connections between the tiles and the central processing, multiple hierarchies of processing must be organized to aggregate the high number of separate connections. To tackle these issues, all tiles are connected, powered (PoE++ IEEE802.3bt) and time synchronized (PTP IEEE 1588) over Ethernet. By default, each tile has a processing unit, an SDR and a power supply, as depicted in Figure 2. This base configuration can be extended with custom solutions to support other use cases. To facilitate other research activities, all developed equipment and software is open-source available.

In this paper we further provide more details on how the testbed is established in a modular way, and its features. The article is structured as follows. First, the support structure is discussed, focusing on the modular design of the detachable tiles. Thereafter, the backbone of the testbed is elaborated. It consists of a central processing unit or server and Ethernet connections to all tiles. The on-tile equipment is introduced in Section 4 with a focus on the default setup. In Section 5 we discuss the rover supporting automated 3D sampling of the room, thereby reducing the time-consuming and labor-intensive task of conducting experiments manually. Lastly, the foreseen research and development activities are summarized in Section 6. The list is by no means exhaustive and we welcome other R&D activities and applications from industry and academic.

2 Techtile Construction – Modular and Open

The Techtile support structure, illustrated in Figure 2, is based on the WikiHouse concept. WikiHouse is an open-source building system. Such constructions are made of standardized wooden parts. Building further on the modular design, the walls, floor and ceiling of the structure are comprised of 140 detachable tiles. The two walls of the building support 28 tiles each. The ceiling and ground floor support 42 and 52 tiles, respectively. The room is 4 m by 8 m. A tile has a size of 120 cm by 60 cm. To mount the electronics, the tile features a 5 cm by 5 cm grid. The grid is made of M3 inserts, allowing conveniently installing components with standardized M3 screws. In addition to attaching equipment and custom electronics to the tile, we allow designing your own tile for specific applications. For instance, Visible Light Communication (VLC) and Visible Light Positioning (VLP) systems using LED fixtures can permanently be mounted in the ceiling. We also support attaching equipment to the inside of the room by means of overlays. An overlay has the same grid structure as a tile and is mounted on top of the tile. This keeps the aesthetics, while still supporting attaching equipment inside. As the infrastructure is mainly designed for embedding electronics inside walls, we emphasize on only using the overlays if absolutely required. By using overlays, research demanding a Line-of-Sight (LoS), e.g., visible light and acoustics, are supported. Overlays are more flexible compared to designing your own tile, as overlays can be installed on all tiles.

Figure 2: Left: The Techtile support structure – Right: The back of three tiles, equipped with the default setup, i.e., a software-defined radio (USRP B210), processing unit (Raspberry Pi 4) and power supply with Power-over-Ethernet. Each tile is connected to the central unit with an Ethernet cable, providing both power and data.

*github.com/techtile-by-dramco
†www.wikihouse.cc
3 Techtile Backbone – Everything over Ethernet

The backbone of the infrastructure consists of a central server which is connected to all tiles over Ethernet. By means of Power over Ethernet (PoE) midspans, 90 W of power is supplied to each tile. Furthermore, the Ethernet switches support the IEEE-1588 Precision Time Protocol (PTP), enabling high-accuracy clock distribution to all connected devices. Hence, the testbed provides communication, synchronization and power over Ethernet. As everything is connected over Ethernet, the developed system is easily scalable and is flexible in the manner in which devices are added and removed from the network.

3.1 Central Processing and Networking

The central server (Dell PowerEdge R7525) has 512 GB RAM, two NVIDIA Tesla T4 16 GB Graphical Processing Units (GPUs) and two AMD 7302 3 GHz Central Processing Units (CPUs), running Ubuntu Server 20.04 LTS.

Apache Kafka is used as a communication and processing platform between the server and the tiles. It follows the publish/subscribe paradigm. Events and streams are organized and stored in topics. Events can be thought of as files residing in a topic acting as a folder. Besides communication, Kafka support stream processing, database integrations, searching and querying data, management, logging and monitoring, making it very flexible to support future applications. Furthermore, data is generated and processed following a consumer/producer scheme, decoupling the systems. This allows to easily let the same data be processed by different clients and to dynamically plug-in and shutdown consumers.

At the networking side, the Dell S4148 switch is used. It features 48 10 Gbit Ethernet ports with IEEE 1588v2 support. In Techtile, four switches are deployed with a total of 192 connections. A Dell Virtual Edge Platform (VEP), running VyOS, handles routing and firewall.

3.2 Power-over-Ethernet

In order to keep the cable management practical, power to the tiles is provisioned with PoE technology, where both data and power go over the same Ethernet cable. With the introduction of the latest standard, IEEE 802.3bt, a power of maximum 90 W can be provided. While this maximum is not required for the default setup, implementing the latest standard ensures a generic solution, supporting also high-power applications.

Our PoE architecture consists of a Power Sourcing Equipment (PSE) and 140 Powered Devices (PDs), supporting all PoE standards, i.e., IEEE 802.3af (PoE), IEEE 802.3at (PoE+) and recent 802.3bt (PoE++). To provision the PoE, the PD-96XXGC series midspans from Microchip is selected as PoE injectors, supporting also the latest 802.3bt PoE++ standard. Each midspan has a 10/100/1000 Mbps data rate pass through. In total a PoE budget of approximately 9 kW is available.

3.3 Synchronization-over-Ethernet

In order to provide time synchronization for all the tiles, PTP IEEE 1588v2 is used. This protocol achieves a clock accuracy in the sub-microsecond range –and depending on the network, configuration and version even sub-nanosecond. The protocol follows a master-slave architecture. The root time reference is hold by the grandmaster clock and distributed to the other clocks in the network. Precision Time Protocol supports both L2 and UDP transport. It has an operation similar to Network Time Protocol (NTP), where the master and slave exchange messages to determine the path delays and correct their clocks accordingly. In PTP, different profiles are defined, each having different configurations and requirements. Such profiles are tailored for specific application and are, for example, used in Time-Sensitive Networking (TSN) [5]. Different clocks are defined based on their capabilities. For instance, transparent clocks are network devices which alter the timestamps in the packets to remove the time spent in these devices, effectively making them transparent to the PTP protocol. A boundary clock on the other hand, serves as both master and slave. It functions as a master at some connections, while synchronizing to a master on another port. One of the ongoing work is to tune the configuration of the protocol to achieve nanosecond accuracy and determine the impact on the processing capabilities of the Raspberry Pi (RPi) and the load on the network.

3.4 Data Acquisition System

The data acquisition system will provide panels with a synchronized analog data acquisition channel, able to sample at 1.25 MS/s, a resolution of 16 bit, and for a total number of 192 channels. This sample frequency and number of bits is sufficient to sample almost every sensor which allows us to move the state-of-the-art in sensor
fusion and federation and underpins our aim for multi-modal sensing and positioning research. It includes sampling of full continuous audio streams (i.e., microphones recording audible or ultrasonic sound) and sensors registering high-bandwidth visible light communication. The high number of synchronized channels allows for setting up truly dispersed architectures, so large and distributed arrays can be obtained.

The data acquisition system also has 48 synchronized 16-bit DAC output channels able to steer a variety of actuators. For example an array of speakers, ranging into the deep ultrasonic range, can be implemented in research on transmit beam forming and backscattering for fully passive mobile devices. Additional possibilities are the generation of modulated signals and multiple access coding schemes to drive power LEDs in VLC applications.

The combination of the data-acquisition system and the edge devices forms the infrastructure that is required to validate new concepts based on distributed nodes. By using the fully synchronized sensing capabilities of the central data acquisition and processing infrastructure, a baseline performance can be established. This baseline performance can act as a reference for more realistic scenario’s where distributed edge devices collaborate in a loosely coupled (and varying) configuration.

4 On-Tile – Sensors, Radios, Processing, and Other Cool Stuff

Each tile can accommodate a diversity of sensors and actuators, transmitters and receivers for radio - and other waves, host processing resources to add distributed intelligence in the environments, and potential other cool stuff that creative researcher may want to experiment with. In this section we elaborate on the custom PoE board, the SDR and the RPi. The PoE board delivers power to the tile and the RPi processes the SDR signals and serves as a platform for edge computing.

4.1 PoE Board

The standard PoE Hardware Attached on Top (HAT) for the Raspberry Pi, or other derivative forms, are readily available but do not support the latest PoE version. For this reason, a 802.3bt supported PD circuit was developed, as shown in Figure 3. The system is based on the ON Semiconductor NCP1096 which is the PoE-PD interface controller. On top of the 802.3bt support, the board features several connectors and voltages to power different devices and sensors, as illustrated in Figure 3b. PoE distributes 48 V over Ethernet.

Connectors and Usage. The 48 V output is directly available on the board through terminal block C. In case other voltages are required, an external DC/DC converter can be connected through terminal blocks E, and the output is available on terminal block C. The other output connections are connected to the internal flyback converter providing 5 V with a maximum power of 20 W. We adopted two bistable switches. One switch (S1) is dedicated to the USB-C connector for the RPi, the other (S2) is used for the other USB-C connector, the two USB-A connectors and terminal block B. These switches prevent that the peripherals – and especially – the RPi will boot-up every time there is a power cycle. Furthermore, we can ensure that not all systems are powered, saving energy and mitigating any damage due to unintentional power outages.

Power Classification. The PoE PD interface controller supports 8 different PoE classes, which are programmable with resistors. The classification is adjustable by means of replacing the classification board and consists of two resistors and a connector (Figure 3a [D]). The connector makes it convenient to switch the class rapidly although a power cycle is required. The most regular classes: 3 (13 W), 4 (25.5 W) and 8 (71.3 W–90 W) are provided. Besides a fixed power class, the class assignment is negotiated automatically. For instance, when only the RPi and Universal Software Radio Peripheral (USRP) is connected, a power class of 3 is sufficient. However, as the class is determined at the beginning of power delivery – and fixed afterwards –, it is crucial that sufficient energy is extracted during start-up. Because the RPi and USRP power consumption and the tile setup is variable, it is not recommended to use autoclass, rather select the desired class in advance. Furthermore, as we have a finite power budget, knowing the consumption of each tile ensures that we adhere to the power constraint. Not respecting the agreed power, leads unfortunately to a power disconnection by the PSE and results in an abrupt power shutdown, causing potential damage and loss of measurement data.
4.2 Wireless RF Communication through Software-Defined Radio

The testbed hosts a fabric of distributed SDRs. Each tile is equipped with one USRP B210, featuring two RF channels. The B210 has a maximum transmit power of 20 dBm. This SDR supports up to 56 MHz of real-time bandwidth through the AD9361 direct-conversion transceiver. The B210 can operate over a frequency range of 70 MHz to 6 GHz, thereby covering most licensed and unlicensed bands. The B210 hosts an open and reprogrammable Spartan6 XC6SLX150 Field-Programmable Gate Array (FPGA). The baseband signal is processed by the host, i.e., RPi 4, using USB 3.0. GNURadio, supported by the B210, enables adopting and designing a high range of protocols and standards, e.g., IEEE 802.11 (Wi-Fi), Bluetooth, LoRaWAN, provided by the open-source community. The B210 can be fed with an external 10 MHz clock and Pulse Per Second (PPS) for synchronized operation. The reference clock is used to generate all data clocks, sample clocks and local oscillators. In addition, an external PPS signal can be used for time synchronization between the SDRs. In this manner, it is possible to coherently transmit and receive on all SDRs.

4.2.1 Architecture

A simplified architecture of the USRP 210 is depicted in Figure 4. It illustrates the connection with the host through the USB interface. The external time and frequency reference is used in the FPGA and radio-frequency integrated circuit (RFIC). The RF frontend consists of mixers, filter, oscillators and amplifiers translating the signal from the RF domain to an intermediate frequency (IF). In receive mode, the complex baseband of the IF signal is sampled and clocked into the FPGA. National Instruments has published the stock FPGA in open-source, and provides, o.a. digital down-conversion and filters for decimation. The resulting I/Q samples are transferred to the host through USB 3.0. The B210 features 2 RX/TX connections and 2 RX connections. The RX/TX connections are switched by an RF switch, thereby using only two identical transmit chains and two received chains sharing the same local oscillator for each TX or RX chain.

4.2.2 Processing the Baseband Signals

The baseband signals are processed by the Raspberry Pi 4 and transferred over USB 3.0. Depending on the application, the distributed signals are aggregated to the central server for further processing. By having both local processing and central processing, different techniques regarding local, edge and cloud processing can be studied. Designing RF communication networks with the B210 is facilitated by the open-source USRP Hardware Driver (UHD) from National Instruments. This library is supported in GNURadio and OpenBTS. In order to coherently transmit and receive, i.e., at the same time, over multiple USRPs, we output 10 MHz and PPS with a custom Printed Circuit Board (PCB). The 10 MHz clock is derived from the 54.0 MHz oscillator on the RPi and tuned with the on-board phase-locked loop (PLL). By using a device tree overlay in Linux, the 10 MHz signal is always present and independent on the state of the Operating System (OS). The PPS is generated
in a loadable kernel module. The PCB, installation procedure and drivers are available in open-source.

4.3 Edge Processing

The default setup contains a RPi capable of edge computing. To latest RPi model, i.e., RPi 4, is adopted. It has a rich feature set, such as 8 GB of LPDDR4-3200 SDRAM and a powerful processor, i.e., Quad core Cortex-A72 (ARM v8) 64-bit SoC 1.5GHz, tailored for high computing tasks. For dedicated and more computation-intensive applications, custom edge computing platforms can be used, e.g., NVIDIA Jetson Nano, Google Coral and Intel NCS.

To speed-up read/write operations, we adopted a solid state drive (SSD) opposed to the standard micro-SD card storage. Besides the speed improvement, the SSD is less sensitive to power failure and has a higher capacity to price ratio. Furthermore, SD cards are designed to store data, while SSDs are tailored for a high number of read/write operations, resulting from running an OS. These characteristics make SSD a more robust and suitable technology.

5 Automated 3D Sampling – a Rover in the House

To speed-up measurements, reduce labor-intensive tasks and mitigate human-errors, we have designed a rover to perform automated 3D sampling inside the testbed. The rover consists of a baseplate, hosting the processing unit and batteries, and a scissor lift to move the measurement equipment to the required height.

Baseplate. The baseplate contains a Raspberry Pi running Robot Operating System (ROS). It controls the wheels, reads-out the sensors and performs navigation. By adopting ROS, the development of the rover is sped-up and is more easily extendable for future applications. ROS consists of software packages dedicated for building robots, containing the necessary drivers and algorithms. The communication, employed in ROS, between nodes, i.e., processing entities, is handled by an asynchronous publish/subscribe message passing system. In this manner, ROS forces the developer to decouple different parts of the system. For synchronized communication, the request/response pattern is used.

A 16 cells battery pack, in a 4S4P configuration, powers the system. The battery voltage ranges from 10 V to 16.2 V depending on the charge state. The battery back, based on Lithium Cobalt Oxide (LCO) technology, has a capacity of 170 W h and can handle up to 480 W peak power. Besides powering the rover, the battery pack provides power to the peripherals and measurement equipment in order to conduct the experiments. When the battery is low, the rover is able to navigate to its charging station, recharge and resume the measurements.

Navigation. Marvelmind indoor RTLS is used as a positioning system. It has a precision of 2 cm. Ultrasonic beacons are used to acquire the position of the mobile beacon (mounted on the baseplate). Four beacons are fixed in the Techtile infrastructure. The position is determined by trilateration. To filter out outliers, we make use of a Kalman filter. The recursive algorithm uses consecutive inputs to estimate the current state. Based on the uncertainties of the inputs and the uncertainties of the previous estimates, the current state is approximated. Besides localization, the rover features obstacle detection to mitigate crashing.

†github.com/techtile-by-dramco/raspberrypi-sync
‡This section contains work realized by two students, Arne Reyniers and Jonas De Schoenmacker, in the context of their master thesis.
into objects in the room. Ultrasonic sensors mounted on the sides of the rover’s baseplate are used and have a resolution of 3 mm and a range of 2 cm to 400 cm.

**Scissor lift.** The baseplate of the rover can navigate through the room in 2D space. By mounting the scissor lift (Figure 5b) on top of the baseplate, the rover is able to measure in 3D space. The lift has a range of 55 cm to 185 cm. The equipment can be mounted on top of the lift. Power is supplied to the equipment from the battery pack. The scissor lift can be controlled with AT-commands. The height of the lift is determined by the VL53L1X Time-of-Flight (ToF) sensor using a 940 nm invisible Class 1 laser. An advertised accuracy and ranging error of ± 20 mm in both ambient light and dark light conditions.

![Image](image.png)

(a) Baseplate hosting the omnidirectional wheels, Controller (Raspberry Pi running ROS), battery pack and Marvelmind beacon. 
(b) Scissor lift having a range of 55-185 cm.

Figure 5: Rover to perform automated 3D sampling.

6 Research and Development Activities - Inviting Creative Experiments

The TechTile experimental facility has been designed to enable a wide range of experiments. We foresee, a.o., the following research and development activities: i) development of next-generation Internet-of-Things solutions, ii) experimental validation of beyond-5G communication, e.g., RadioWeaves, iii) positioning and sensing based on acoustic signals, iv) wireless charging and v) visible light communications and positioning.

**Internet-of-Things.** We develop the next generation IoT solutions that should accommodate a massive number of low power devices and upgrade them to get smarter, leveraging AI approaches. We conceive auto-discovery, self-diagnostics, and recovery approaches, to ultimately achieve zero e-waste impact.

**(Beyond) 5G communication.** We pursue experimental validation of (distributed) multi-antenna systems to support huge number of (low power) devices and provide ultra-reliable low latency connectivity. We will investigate cell-free operation and Large Intelligent Surfaces, new paradigms that may serve 6G systems.

**Acoustic sensing and indoor positioning.** We sense acoustic signals for a better understanding of the environment. Through hybrid RF-acoustic signaling we pursue positioning of low energy devices with unprecedented accuracy.

**Secure connected devices.** We exploit physical features of propagation and directivity to increase the security of connected devices, and enable private local networking solutions.

**Wireless charging.** We investigate whether/how devices can get charged without the need for cables, and eventually ‘on their spot’.

**Visible Light Communication and positioning.** We develop communication and positioning systems that modulate LED light sources without impacting their illumination functionality. They complement conventional RF systems where the interference poses aggravating problems.
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