A Second-order 16.5 Bit Analog-to-Digital Converter with a 145 dB Operational Amplifier Gain

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Abstract: In this study, an IDC applicable for use with temperature and humidity sensors was designed. To this end, we take into account the factors of area and accuracy, a simple second-order chain of integrators with forward (CIFF) architecture was used to achieve an effective number of bits (ENOB) of 16.5. A gain-boosted operational amplifier (op amp) with a gain of up to 145 dB was adopted for the first-order integrator, and the digital filter adopted a sincL structure. In Section 2.1, the working principle of the proposed second-order. IDC is introduced. In Section 2.2, the design specifications are presented, the system timing and circuit structure are introduced, the circuit structure of the first-order integrator is described in detail, and the overall simulation results are provided. In Section 3, the test results obtained for a physical chip implemented using the SMIC 0.18 μm process are presented and compared with those obtained by similar previously proposed designs. Measurements show that the incremental converter achieves 99.1 dB SNR higher than the other second-orders or even some three-order IDC. And the chip occupied an effective area of 0.211 mm² smaller than the other IDC. Finally, the conclusions of this study are given in Section 5.

1. Introduction

The processing, storage, and transmission of digital signals are far more convenient than these operations are for analog signals. However, continuous analog signals are the standard forms arising in nature, e.g., temperature, humidity, and sound signals. Sensors have been designed to convert environmental analog signals into electrical analog signals, which are then converted into more convenient digital signals via analog-to-digital converters (ADCs) [1, 2]. However, in contrast to sound signals, temperature and humidity signals are of low frequency, typically on the order of Hz. Therefore, ADC circuits employed in conjunction with temperature and humidity sensors have high accuracy and linearity requirements, but a relatively low bandwidth requirement. Unfortunately, ADCs based on conventional architectures generally provide a resolution less than 16 bit, and require complicated external calibration circuits with relatively large power consumption to realize higher accuracy [3].

In 1978, Van der Plassche proposed first-order delta-sigma modulator theory applicable to low frequency modulation [4]. This modulator structure usually operates in a discrete single-shot mode, i.e., the circuit is powered on to complete and output a conversion, and then the circuit enters a dormant state to reduce power consumption. A delta-sigma ADC process conducted in this operation mode is denoted as an incremental ADC (IDC). Because of the modulation process, IDCs can easily achieve high accuracy by employing oversampling and noise shaping. Furthermore, because an IDC is in the sleep
state between conversions, it has low circuit power consumption, which makes it suitable for use with temperature and humidity sensors [5-8].

In this study, an IDC applicable for use with temperature and humidity sensors was designed. To this end, a simple second-order chain of integrators with forward (CIFF) architecture was used to achieve an effective number of bits (ENOB) of 16.5. A gain-boosted operational amplifier (op amp) with a gain of up to 145 dB was adopted for the first-order integrator, and the digital filter adopted a sincL structure. In Section 2, the working principle of the proposed second-order IDC is introduced. In Section 3, the design specifications are presented, the system timing and circuit structure are introduced, the circuit structure of the first-order integrator is described in detail, and the overall simulation results are provided. In Section 4, the test results obtained for a physical chip implemented using the SMIC 0.18 μm process are presented and compared with those obtained by similar previously proposed designs. Finally, the conclusions of this study are given in Section 5.

2. Material and Methods

2.1 Working Principle of the IDC with Second-order CIFF Architecture

For a first-order IDC, the integrator must firstly be reset, followed by the conversion process conducted over some number of cycles, and then the output value is obtained by a digital filter [9]. An equivalent process applies to a second-order IDC, which employs two integrators rather than one. Figure 1 shows an IDC system schematic with a second-order CIFF architecture. In the figure, \( V_{in} \) is the input voltage, \( V_{i1} \) denotes the output voltage of the first-order integrator, \( V_{i2} \) is the output voltage of the second-order integrator, reset represents a reset signal, \( d_i \) is the output of the comparator, and \( D_{out} \) represents the final result output from the digital filter, where \( N \) is the oversampling rate.

![Figure 1. IDC system schematic with second-order CIFF architecture](image)

When the coefficient \( G \) satisfies [10]

\[
G = \frac{2}{N(N-1)} ,
\]

\( D_{out} \) can be expressed as

\[
D_{out} = \frac{2}{N(N-1)} \sum_{k=0}^{N-1} \sum_{l=0}^{l_1} d_k .
\]

The least significant bit (LSB) voltage of the IDC, denoted as \( V_{LSB} \), can be expressed as

\[
V_{LSB} = \frac{2}{N(N-1)bc} V_{ref} .
\]

Here, \( b \) and \( c \) are coefficients of the system.
Therefore, the relative quantization error, denoted as $e_q$, is calculated as follows:

$$e_q = \frac{D_{\text{out}} - V_{\text{in}}}{V_{\text{LSB}}} = \frac{1}{2} b_c \sum_{i=0}^{K+1} \sum_{k=0}^{L} d_k - \frac{1}{2} b_c \frac{N(N-1)}{2} V_u V_{\text{ref}}.$$

(4)

The relationship between the ENOB, the signal-to-noise ratio (SNR), and $V_{\text{LSB}}$ can be expressed as follows.

$$\text{ENOB} = \log_2 \left( \frac{V_{\text{LSB}}}{V_{\text{LSB}}} \right) = \log_2 \left[ \frac{N(N-1)}{2} \right]$$

$$= 2 \log_2(N) + \log_2(bc) - 1$$

(5)

$$\text{SNR} = 10 \log \left( \frac{3}{2} \times 2^{-2n} \right).$$

(6)

Here, $n$ is ENOB.

2.2 PROPOSED SECOND-ORDER IDC ARCHITECTURE

In this study, a 16.5 bit IDC was designed. To retain the most adequate performance margin, an 18 bit resolution was planned in the design phase, with a corresponding SNR of 110 dB. In this design, a 1.6 V voltage supply $V_{\text{DD}}$ was applied and the reference voltage $V_{\text{ref}}$ was also set as 1.6 V, i.e., $V_{\text{DD}} = V_{\text{ref}} = 1.6$ V. Based on practical experience, the input signal voltage range of the second-order modulator is usually less than $0.75 V_{\text{ref}} = 1.2$ V. According to the discussion in Section 2, the SNR of the system can be calculated based on the input signal voltage and the in-band noise energy. The calculated in-band noise voltage is 2.46 µV with an in-band noise power spectral density (PSD) of 140 nV√Hz (based on a 300 Hz signal bandwidth). The basic design specifications of the modulator are summarized in Table 1.

| Table 1. Design specifications of the proposed IDC modulator |
|---------------------------------|
| **Topology** | **Second-order** |
| Conversion time | <2 ms |
| Sampling frequency | 1 MHz |
| Input range | ±1.2 V |
| Reference voltage | 1.6 V |
| Signal-to-noise ratio | 110 dB |
| Number of bits | 18 bit |
| Output noise | 2.46 µV |
| Noise power spectral density | 140 nV√Hz |

The main approach for setting the coefficients in the structure of a basic delta-sigma modulator is to select reasonable coefficient values that ensure a feedback signal that is substantially equivalent to the input signal. Because the input signal of the first-order integrator contains only quantization errors and the signal amplitude is relatively small, the slew rate and input range requirements of the op amp employed in the first-order integrator are greatly reduced. It can be seen from Equation (5) that the accuracy (i.e., the ENOB) increases with increasing $N$ (i.e., the number of conversion cycles), and with increasing values for coefficients $b$ and $c$. Because we adopted a folded cascode for the first-order integrator, the value of $b$ should be as small as possible and the value of $c$ should be relatively large. Therefore, we selected the coefficients as $b = 0.2$ and $c = 0.6$. According to these values and Equation (5), $N$ can be calculated as 2,048. However, we selected $N = 2,500$ to reserve a sufficient performance
margin. The values of the coefficients $a_1$, $a_2$, and $a_3$ were obtained via system simulation, which yielded values of $a_1 = 0.4$, $a_2 = 0.8$, and $a_3 = 0.5$.

Figure 2 presents a circuit diagram of the modulator employed in the proposed design. Here, the switch control signals $S_1$ and $S_2$ are a pair of non-overlapping clocks of equivalent frequency, but separated in phase by half a clock cycle, and $S_{1d}$ and $S_{2d}$ are the delay clocks of $S_1$ and $S_2$, respectively. The first-order output of the modulator is sampled in the $S_2$ phase and integrated in the $S_1$ phase. The second-order output of the modulator is sampled in the $S_1$ phase and integrated in the $S_2$ phase. The output of the summing capacitor is sampled in the $S_1$ phase and the summing result is directly input into the comparator, whereas the electric charge on the capacitor is cleared only in the $S_2$ phase. Here, the power consumption of the comparator is 12.5 µA. The values of $C_{S1}$ and $C_{S2}$ were obtained via MATLAB simulation, which yielded values of $C_{S1} = 4$ pF and $C_{S2} = 0.6$ pF.

![Circuit diagram of the proposed IDC modulator with second-order CIFF architecture](image)

Figure 2. Circuit diagram of the proposed IDC modulator with second-order CIFF architecture

The $1/f$ noise and offset voltage are the primary noise components at low frequencies. The offset voltage can be regarded as a low-frequency input-referred noise, which can be eliminated by self-zeroing techniques such as correlated double sampling (CDS). As a self-zeroing technique, CDS has been widely used in switched capacitor circuits since it was proposed more than 30 years ago [11, 12]. In the $S_1$ sampling phase, the op amp noise and the switching noise are stored on capacitor $C_{cds}$, and then the noise components are eliminated in the $S_2$ phase. The application of CDS increases the number of switches and capacitors, which may result in an increased in-band thermal noise energy. In addition, because $C_{cds}$ and the sampling capacitor are parallel with the parasitic capacitance at the op amp input end, the application of CDS may also increase the load capacitance of the op amp. However, the benefit of the reduced input $1/f$ noise and offset voltage is worth the potential liabilities of the CDS circuit.

Operational amplifiers suffer from nonidealities, associated with finite gain, bandwidth, and slew rate (SR), which result in performance degradation such as the incomplete transfer of charge in the switched capacitor (SC) integrator [13]. The finite DC gain can be determined based on the accuracy requirements of the modulator [14]. For a feedback loop with a feedback factor of $\beta$, the transfer function is

$$A = \frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \beta A_0} = \frac{1}{\beta} \left( \frac{1}{1 - \beta A_0} \right).$$

Here, $A0$ is the finite open-loop DC gain. Therefore,

$$\frac{1}{\beta A_0} < 0.5\text{LSB} \Rightarrow A_0 > \frac{\beta}{0.5\text{LSB}} = \beta \cdot 2^{-1}$$

(8)
The SR can be expressed as
\[ SR = \frac{V}{t}, \]
where \( V \) is the output voltage, and \( t \) is the slewing time. Allocating half of a clock phase (i.e., one quarter of a clock period \( T \)) for slewing \[14\] yields the minimum SR value:
\[ \text{SR}_{\text{min}} \geq \frac{V_{dd}}{4T}, \]
where the supply voltage \( (V_{dd}) \) represents the maximum value of \( V \). The time constant \( \tau \) of the integrator is given as
\[ \tau = \frac{1}{(2\pi GBW)}, \]
where \( GBW \) is the gain-bandwidth. If we require linear settling to provide 140 dB of attenuation for the initial condition \[14\], then
\[ T/4 = \tau \ln(10^{14}) = 16\tau = 16/(2\pi GBW), \]
\[ GBW = \frac{32}{T \cdot \pi}. \]
However, MATLAB simulation is still required after conducting these calculations to determine the final value.

To fully suppress the presence of low-frequency noise and meet the accuracy requirements, the first integrator must have a gain of up to 140 dB, and the second integrator amp must have a gain of up to 80 dB. However, the amplification ability of an ordinary folded cascode cannot meet these requirements for the first integrator. Therefore, we employed a gain-boosted op amp structure for the first integrator, with the main op amp and auxiliary gain op amp both achieving a 70 dB gain. Finally, the power consumptions of OTA1 and OTA2 shown in Figure 2 are 104 \( \mu \)A and 26 \( \mu \)A, respectively.

The bias circuit for the gain-boosted op amp is shown on the left-hand side of Figure 3, where the reference current \( IB \) is generated by a bandgap circuit, and the folded cascode structure is shown on the right-hand side of the figure, where the op amps otan and otap provide auxiliary gain. The op amp structure employs \( M_2 \) and \( M_3 \) as differential input transistors. Transistors \( M_1, M_6, M_7, M_{12}, \) and \( M_{13} \) are current sources of the main op amp while transistors \( M_8, M_9, M_{10}, \) and \( M_{11} \) form the cascode structure. The gate voltage of transistors \( M_4 \) and \( M_5 \) represents a common-mode feedback (CMFB) control terminal. While a closely spaced pole and zero (doublet) exist in gain-boosted amplifiers, which can seriously degrade the settling behavior of an op amp[15-16]. But a small capacitor in parallel with the output resistor of the op amplifier can alleviate this problem. Therefore, the compensation capacitors \( Cc \) at the output ends of gain boosting amplifiers otan and otap are employed to improve the stability of
the gain-boosted amplifiers. Switched capacitor common-mode feedback (SC-CMFB) circuits were employed to realize CMFB of the main op amp.

The folded cascode structure was also applied for the auxiliary gain op amps otan and otap, as shown in Figures 4 and 5, respectively. Because the auxiliary op amps are connected to the gate terminals of the NMOS and PMOS output transistors in the main op amp, the differential output voltage changes within a very small range, so the CMFB circuits can apply a continuous time structure. Taking Figure 4 as an example, the transistor pairs Mc7, Mc8 and Mc1, Mc2 are the current sources producing equivalent current values I. The voltage of Mc8 at the gate terminal is the feedback control signal. If the common mode voltage of op amp output voltages \( V_{out+} \) and \( V_{out-} \) equals the standard value of \( V_{com} \), whereas the differential mode signals are \( \Delta v^+ \) and \( \Delta v^- \), which are equivalent in magnitude, but opposite in polarity, then Mc5 and Mc4 have equivalent current magnitudes of \( I/2 + \Delta i \), and Mc6 and Mc3 have equivalent current magnitudes of \( I/2 - \Delta i \). However, when the common mode outputs of \( V_{out+} \) and \( V_{out-} \) deviate from \( V_{com} \), e.g., are less than \( V_{com} \), then the current flowing through Mc3 and Mc4 will increase, the current of Mc8 will increase, and the voltage \( V_{cmfb} \) will increase as well. As the current of M10 and M11 in the op amp increases, the output voltages \( V_{out+} \) and \( V_{out-} \) increase, and tend towards \( V_{com} \). Therefore, the CMFB circuit can effectively stabilize the common mode voltage.

![Figure 4. Auxiliary operational amplifier otan (Figure 3) and the common-mode feedback circuit](image1)

![Figure 5. Auxiliary operational amplifier otap (Figure 3) and the common-mode feedback circuit](image2)
Figure 6. Difference module loop gain (top) and phase Bode plot (bottom) of the gain-boosted operational amplifier

Closed loop alternating current simulation results for the first integrator are shown in Figure 6, where the total gain achieves a value of up to 145 dB (top figure), the unit frequency bandwidth is 44 MHz, and the phase margin achieves a value of 70 deg (bottom figure), which meet the requirements of the first integrator. The second integrator is a relatively simple design; therefore, it is not described here.

The digital filter employed at the output of the op amp (between \(d_i\) and \(D_{out}\) in Figure 1) is important for suppressing both DC and low-frequency input interferences due to environmental noises. Because these periodic interference sources and various other non-ideal factors can affect circuit performance, a high-performance sinc\(L\) filter circuit was adopted in this study. The order of the filter must be at least as high as that of the modulator, but preferably greater by 1\[17\]. Therefore, we employed a value of \(L = 3\) for the second-order modulator with CIFF architecture, and the corresponding sinc3 filter illustrated in Figure 7 was adopted. The transfer function of the filter is as follows:

\[
H(z) = \left(\frac{1}{1-z^{-1}}\right) \left(\frac{1}{1-z^{-1}}\right) \left(\frac{1-z^{-M}}{M}\right) \left(\frac{1-z^{-M}}{M}\right),
\]

where \(M\) is the decimation rate.

Figure 7. Structure of the sinc\(L\) filter (\(L = 3\))

Figure 8 shows the simulation results for \(e_q\) relative to an ENOB of 18 within the input voltage range. The input voltage range is plotted relative to a reference voltage of 1.6 V. It can be seen that, within the valid input voltage range (−1.2 V, 1.2 V), the value of \(e_q\) meets the requirement of \(\pm 0.8V_{LSB}\), which verifies that the overall system simulation achieves an ENOB of 18.
Figure 8. Relative resolution (quantization error $e_q$) within the effective input voltage range

3. RESULTS

Figure 9 presents an image of the proposed IDC design implemented using the SMIC 0.18 $\mu$m process. The chip is a 28-lead dual in-line package (DIP28L) with an effective area of 0.651 mm $\times$ 0.324 mm = 0.211 mm$^2$. Figure 10 shows the experimental setup for the physical testing of the proposed ADC chip. The chip’s DC input signal was generated by a KEYSIGHT 33600A signal generator, and a KEYSIGHT E3620A was employed as the 5 V power supply of the printed circuit board (PCB). Both the clock and switch sequence of the chip were generated through an FPGA program. The reset signal of the chip was controlled by the keys on the FPGA board. The chip’s output signals were collected by a National Instruments USB-6353 data acquisition (DAQ) board, and the output code streams were recorded and stored by Labview software and DAQ Assistant. The obtained code streams were input into MATLAB for digital filtering, and the ADC resolution was calculated through fast Fourier transform (FFT) analysis.

Figure 9. Proposed IDC design implemented using the SMIC 0.18 $\mu$m process
Figure 10. Experimental setup for the physical testing of the proposed ADC chip.

Figure 11 presents a PSD plot of the output code stream of the chip. During testing the input was a DC signal, and the number of sampling periods was 8,192. The measured waveform shows that the chip realizes a second-order noise-shaping function, because the PSD increased at a rate of 40 dB/decade, and the low-frequency noise energy level is about −120 dB. The SNR and ENOB of the modulator were obtained through MATLAB analysis as 99.8 dB and 16.5 bits, respectively. Figure 12 shows the linearity of the chip under reference voltages of 1.6 V and 1.5 V. It can be seen that the linearity and output resolution remain good for both reference voltages.
Figure 12. Input-output voltage curves of the chip under different reference voltages

4. Discussion

Table 2 summarizes the actual test results of the chip along with those of similar previously reported IDC designs. Compared with the design proposed by Chen et al. [19], we note that, while the bandwidths of the input signal are similar, the first-order integrator design adopted in the present study employs an op amp with a higher accuracy, better noise suppression effect, and higher SNR. The design proposed by Quicquempoix et al. [20] achieved a higher SNR than the presently proposed design, but the presently proposed design employed a lower order integrator, and therefore provides lower power consumption. Finally, compared with the designs proposed by Agah et al. [18] and Garcia et al. [21], the current design not only achieved a higher SNR, but also a smaller chip area. In summary, the unique low-frequency advantages of the IDC designed in the present study ensure that it is more suitable than previously proposed IDCs for processing the signals derived from temperature and humidity sensors.

Table 2. Performance comparison of the present IDC design and similar previously proposed IDC designs

| Parameters               | This work | [18] | [19] | [20] | [21] |
|--------------------------|-----------|------|------|------|------|
| Architecture             | 2nd-order | 2nd-order | 2nd-order | 3rd-order | 3rd-order |
| Process                  | 0.18 µm   | 0.18 µm | 0.16 µm | 0.6 µm | 0.15 µm |
| Area (mm²)               | 0.211     | 3.5   | 0.45  | 2.08  | 1.02  |
| VDD (V)                  | 1.6       | 1.8   | 1     | 3     | 1.6   |
| Sampling frequency       | 1 MHz     | 45.2 MHz | 750 kHz | 30.7 kHz | 320 kHz |
| SNR (dB)                 | 99.8      | 86.3  | 81.9  | 120   | 64    |
| Bandwidth                | 300 Hz    | 500 kHz | 667 Hz | 7.5 Hz | 2 kHz |
| Power consumption        | 228 µW    | 38.1 mW | 20 µW  | 300 µW | 96 µW |
| FOMw (pJ/conv)           | 4.1       | 1.46  | 1.48  | 24.46 | 18.5  |
| FOMS (dB)                | 161       | 161.3 | 157.1 | 164   | NA    |
5. Conclusion
In this study, an IDC applicable for converting the signals derived from temperature and humidity sensors was designed. The modulator design was based on second-order CIFF architecture, and a sinc\(^4\) filter was adopted as the digital decimation filter. Simulations verified that the proposed circuit achieved a resolution of 18 bit with a sampling frequency of 1 MHz and a supply voltage of 1.6 V. The proposed IDC design was physically implemented using the SMIC 0.18 \(\mu\)m process, and the chip occupied an effective area of 0.211 mm\(^2\). Test results for the physical ADC chip demonstrated that the output SNR of the IDC was 99.8 dB, the power consumption of the entire modulator was 228 \(\mu\)W, and the figure of merit FOM\(_w\) was 4.1 pJ/conv, which meets the design requirements for an ADC applied for processing the signals derived from temperature and humidity sensors.

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