The ferroelectric field-effect transistor with negative capacitance

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Integrating ferroelectric negative capacitance (NC) into the field-effect transistor (FET) promises to break fundamental limits of power dissipation known as Boltzmann tyranny. However, realizing the stable static negative capacitance in the non-transient non-hysteretic regime remains a daunting task. The problem stems from the lack of understanding of how the fundamental origin of the NC due to the emergence of the domain state can be put in use for implementing the NC FET. Here we put forth an ingenious design for the ferroelectric domain-based field-effect transistor with the stable reversible static negative capacitance. Using dielectric coating of the ferroelectric capacitor enables the tunability of the negative capacitance improving tremendously the performance of the field-effect transistors.

INTRODUCTION

Dimensional scalability of field effect transistors (FETs) has reached the Boltzmann tyranny limit because of transistors’ inability to handle the generated heat1. To reduce the power dissipation of electronics beyond this fundamental limits, negative capacitance (NC) of capacitors comprising ferroelectric materials has been proposed as a solution2. The FET with a negative-capacitance ferroelectric layer has gained an enormous attention of researchers3–12. However, after impressive initial progress that has resulted in a rich lore massaging the aspects of technological benefits of the prospective stable static negative capacitance, the advancement in the field decelerated considerably. The lack of a clear self-consistent physical picture of the origin and mechanism of the stable static negative capacitance7,11–14 not only retarded the craved technological progress, but has led to numerous invalid fabrications and misleading claims9.

In this work, we put forth a foundational mechanism of the NC in ferroelectrics demonstrating inevitable emergence of the NC due to formation of polarization domains. We establish a practical layout. The proposed device is tunable and downscales to the 2.5–5 nm technology node.

In what follows we review the state-of-the-art and basic concepts behind exploring ferroelectrics as the NC elements which constitute the base for our new results. We also mark the potential pitfalls in the NC implementing in the so far suggested NC FETs caused by depreciating the immanent role of domains. Figure 1 demonstrates the principles of integrating the ferroelectric layer with the NC into the FET and the crucial role of domains. The performance of the FET is quantified by the so-called subthreshold swing $SS = \frac{SS_b}{(\log_{10}I_d/\partial \log_{10}V_s)}$ that describes the response of the drain current $I_d$ to the gate voltage $V_s$. The lower the value of the $SS$, the lower power the circuit consumes. In a basic bulk metal-insulator-semiconductor field-effect transistor (MIS FET), shown in Fig. 1a, which generalizes the MOSFET structure, the subthreshold swing is

$$SS = \frac{SS_b}{m \partial \log_{10}I_d/\partial \log_{10}V_s}, \quad m = 1 + \frac{C_i}{C_g}. \quad (1)$$

Here the first factor, $SS_b$, presents the response of $I_d$ to the voltage $V_s$ at the conducting channel region, and the second factor, the so-called body factor, $m$, characterizes the response of the voltage $V_s$ to the applied voltage $V_p$. Figure 1a shows the equivalent electronic circuit, with $C_g$ and $C_i$ standing for the gate dielectric and semiconducting substrate capacitancies, respectively.

The fundamental constraint of the energy/power efficiency of the MIS FETs arises from the thermal injection of electrons over an energy barrier enabling drain current flow and thus preventing the reduction of factor $SS_b$ below the 60 mV dec$^{-1}$, because the body factor $m > 1$ at $C_p/C_i > 0$. To overcome this limitation, the FETs incorporating the NC into its design has been proposed2. Indeed, replacing the gate dielectric with material with negative capacitance $C_{NC}$ would make the body factor $m < 1$, thus, pushing the $SS$ below the Boltzmann limit.

Ferroelectric materials appear as best candidates for realizing negative capacitance in FETs2. The emergence of the NC in a ferroelectric capacitor follows from the Landau double-well landscape of the capacitor energy $W$ as a function of the applied charge $Q$15 (blue line in Fig. 1b). The downward curvature of $W(Q)$ at small $Q$ implies that the addition of a small charge to the ferroelectric capacitor plate, induces non-zero polarization and reduces its energy. Hence the negative value of the capacitance $C_{NC} = dW/dQ$. Remarkably, even the domain formation due to fundamental instability of a monodomain state16–21, maintains the negative capacitance16,22–26. The energy $W(Q)$ of the multidomain state is lower then that of the monodomain state while the downward curvature at $Q = 0$ is conserved, see the red line in Fig. 1b illustrating an exemplary $W(Q)$ for the capacitor hosting two domains. A detailed parsing of particularities related to the monodomain state instability and specific manifestations of the multidomain state is presented in Supplementary Note 1.

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An inevitable multidomain formation poses the need for a detailed exploring possible ways of realization design of the NC FETs. While the multidomain configuration preserves the NC, the domain formation may trigger some undesired effects detrimental to realizing the NC FET. In particular, domains cause inhomogeneous charge\(^2\) and electric field\(^2\) distribution, endangering the conducting channel in the most commonly discussed metal-ferroelectric-semiconducting MFS FETs (Fig. 1c), as the voltage dispersion they cause becomes comparable with the transistor operation voltage. This problem can be mended by putting the ferroelectric layer into the pretransitional (incipient) regime just above the transition temperature, where the NC effect still persists, but the field-induced polarization distribution is uniform\(^5\)\(^,\)\(^12\). However, this would limit the desirable decreasing of the body factor keeping it above 0.99\(^15\). Another way out is introducing an intermediate dielectric (insulating) buffer layer between the ferroelectric and semiconductor\(^3\), which corresponds to MFS FET architecture shown in Fig. 1d. This, in its turn, would not help much because smoothing the field nonuniformity would occur only at distances well exceeding the spatial scale on which the NC potential amplification effect is still actual. A detailed analysis of particularities related to pitfalls of the discussed above architectures of the specific multidomain state is presented in Supplementary Note 2.

The design with the floating gate electrode placed between ferroelectric and dielectric layers\(^30\)\(^,\)\(^31\) appeared to resolve this problem and to level the field inhomogeneities right below the electrode. The resulting MFMIS structure is the conventional FET with the overimposed MFM capacitor, see Fig. 1e. This architecture has attracted some critique\(^32\), since it was believed that the antiparallel domains formation inside the MFM capacitor would destabilize the NC. However, as we established in Luk’yanchuk et al.\(^24\), it is precisely the two-domain configuration that provides the stable and operable NC because of the possibility of manipulating the domain wall by the applied charges, not accounted for in Hoffmann et al.\(^32\).

Here we introduce and devise the working regime of the MFMIS FET in which the NC effect emerges from the integrated MFM capacitor hosting two domains. We show that the MFMIS architecture not only free from the perils mentioned above but allows for an enormous improving MFMIS FET characteristics by coating the MFM capacitor with the dielectric capacitor in parallel connection. The proposed coating design that we call c-MFMIS FET, shown in Fig. 1f, provides degrees of freedom enabling a complete tunability of the dielectric parameters of the NC FET.

**RESULTS AND DISCUSSION**

**Two-domain negative capacitance of the MFM capacitor**

The nanodot-scale two-domain MFM is a major element of the MFMIS FET enabling the NC response via the charge-controlled motion of the DW. Following\(^24\), we discuss in detail the negative capacitance of the MFM capacitor, which is the base of our proposed device. Shown in Fig. 2a is the general view of MFMIS FET. Figure 2b presents the vertical and horizontal cross-sections of a nanoscale ferroelectric disc-shape MFM capacitor integrated in the MFMIS FET. At the zero charge \(Q_0\) at the electrodes of the MFM capacitor, corresponding to the zero voltage at the transistor, the DW sits in the middle of the capacitor, see left hand side of Fig. 2b. The intrinsic charges at the respective electrodes redistribute in order to compensate the depolarization charges of each domain (keeping the total charge \(Q_0 = 0\)) and to banish the electric field inside the ferroelectric disc, reducing thus the electrostatic energy. The finite charge \(Q_0\) induced by the voltage \(V = V_0\) applied to the transistor gate, displaces the DW from its middle zero-voltage position, see right hand side of panels b. Accordingly, the intrinsic charges rearrange (maintaining
the total charge $Q_d$ to compensate the depolarization fields of now unequal domains.

The NC response arises since the length, hence the energy of the displacing DW, is sensitive to the shape of a ferroelectric capacitor. To ensure the best controlled performance of the NC, we choose a disc-like form of a capacitor. When moving apart from the middle, the DW not only compensates the electric field arising due to the charge transferred to the electrodes but, minimizing its surface self-energy, shrinks in the width $w$ and bends because of the cylindrical shape of a ferroelectric. As a result, the DW overshoots towards the edge beyond the electrostatics-demanded equilibrium position at which the internal electric field would have disappeared. Hence the net electric field does not vanish but flips over and goes from the negatively charged electrode to the positively charged one. This counterintuitive outcome precisely expresses the phenomenon of the negative capacitance. Note, however, that at some threshold value of the applied charge, $Q_f^*$, when it becomes approximately equal to the depolarization charge of the uniformly oriented polarization, $Q_0$, the DW reaches the edge of the ferroelectric layer and leaves the sample. The monodomain state with positive capacitance restores; this corresponds to the termination of the red branch in Fig. 1b.

The quantitative description of the NC of the disk-shape two-domain ferroelectric capacitor is given by Luk'yanchuk et al.\textsuperscript{24}

$$C_{NC} = -\gamma_f \frac{D_f}{\xi_0} C_r,$$

where we explicitly spotlighted the capacitance $C_r = \varepsilon_0 \varepsilon_S S_d / d_h > 0$, which is the capacitance of the monodomain MFM capacitor in the stable state at $Q = \pm Q_0 = \pm S_d P_0$ (minima of the $W(Q)$ dependence in Fig. 1b). The negative factor, $-\gamma_f D_f / \xi_0$, reflects the features brought in by the DW displacement in the two-domain configuration. Here $D_f$ and $d_h$ are the diameter and height of the capacitor, respectively, $S_d = nD_f^2 / 4$ is the area of the ferroelectric plate surfaces, and $P_0$ is the polarization of the ferroelectric in the equilibrium state. The coherence length $\xi_0 \approx 1$nm describes the DW thickness, the dimensionless geometric factor $\gamma_f \approx 4.24$ reflects the internal profile of polarization inside the DW and the DW bending in the cylindrical gate, and $\varepsilon_m$ and $\varepsilon_0$ are the dielectric constant of the ferroelectric material and the vacuum permittivity, respectively.

Figure 1b displays the energy advantage of the two-domain state (whose energy is shown by the red curve), with respect to the usually considered uniform NC state (the blue dashed curve), both states preserving the same charge $Q$ at the electrodes. To create the two-domain state from the uniformly-polarized state one has to suppress polarization in a fraction of the ferroelectric occupied by the DW, while to depolarize the monodomain state by the electric field due to the uniformly distributed charge $Q$, one would have had to suppress the ferroelectricity within the whole volume which is much more energetically costly.

As a next step, we integrate the MFM two-domain NC-capacitor into the MFMIS FET architecture.

The MFMIS FET

This device comprises the gate stack overimposed on a semiconducting substrate in which the source and drain parts are connected by the gate-operated conducting channel, see Fig. 2a. The gate stack includes the MFM capacitor and the gate insulating layer separating it from the substrate. This is the high-$\kappa$ dielectric layer, preventing a charge leakage between the lower capacitor's plate and the semiconducting channel.

The top MFM capacitor plate is the gate electrode connecting the transistor to the external voltage source. The bottom capacitor electrode is an intermediate electrically isolated floating gate electrode of the transistor that preserves the entire charge, most commonly the zero total charge, constant, stabilizing the ferroelectric two-domain state. Furthermore, the floating gate makes the potential along the ferroelectric interface even, maintaining, therefore, a uniform electric field across the gate stack and substrate. Along the way, the floating gate resolves a frequent issue of neutralizing the parasitic charges that may be trapped by
interfaces during the fabrication and functioning. Maintaining the working charge and providing a regular rubbing out the parasitic leaking charges with the removal time faster than the leakage time\(^{3\text{1}}\) is achieved via the standard discharging methods. For instance, it is implemented by either harnessing the Fowler-Nordheim tunneling and the hot electrons injection\(^{3\text{3}}\), or by circuiting the gate by the auxiliary charge-carrying current, \(I_{ch}\), contact, see Fig. 1e, to a certain source for a given combination of electric inputs ensuring the proper sequence of discharging and high resistance modes\(^{34}\).

An effective electronic circuit of the MFMIS FET, shown in Fig. 1e, is similar to that of the multidomain MFIS FET (Fig. 1d). The difference is that now the task of leveling the depolarization field inhomogeneities is taken by the floating gate electrode. Therefore, the gate dielectric layer can be safely engineered as an unusually thin one, down to the technologically-acceptable limit of a few nanometers. This increases \(C_g\) with respect to \(|C_{NC}|\), opening doors to making the gate capacitance negative, \(C^{-1}_g = C^{-1}_C - |C^{-1}_{NC}| < 0\). Yet it is hard to achieve a required large change of \(C_g\) with respect to \(|C_{NC}|\) due to the restrictions imposed by materials compatible with the silicon CMOS technologies. To meet the challenge, we devise a coated c-MFMIS FET that critically changes the situation and breaks ground for the unlimited enhancement of the performance of the NC FET transistor.

### The c-MFMIS FET

The coating of the ferroelectric layer with the dielectric oxide sheath confined by the same electrodes, see Fig. 2c, d straightforwardly incorporates an additional capacitor with the capacitance \(C_g > 0\) in parallel to \(C_{NC}\). This results in a radical improvement of the controlled tuning of the gate capacitance. In particular, manipulating with the sizes of the coating oxide layer and with the geometrical design of the device as a whole, provides a broad variation in its performance characteristics and functioning regimes. The panels (c) and (d) exemplify possible designs. The panel (c) shows an annulus-like coating capacitor, while panel (d) displays a rectangular design of the coating layer and, in addition, the possibility of increasing the area of the floating gate electrode with respect to the top gate electrode. The latter design allows for controllable increasing capacitances of the coating and gate-dielectric layers most efficiently, maintaining the miniaturization of the device. Note, that in all the geometries, the core ferroelectric should maintain its disc-like shape ensuring the optimal manipulation with the DW.

Shown in Fig. 1f is the equivalent circuit of c-MFIS FET. The important advance is that the gate capacitance becomes

\[
C_g = \frac{1}{C^{-1}_g + (C_C - |C_{NC}|)}
\]

which permits tuning \(C_g\) over the widest range of values by the appropriate modifying the parameters of the coating capacitor. We reveal the rich dependence of \(C_g\) on the coating layer size, \(L_c\), choosing the rectangular geometry of the coating layer (Fig. 2c).

The capacitance of the disk-shaped two-domain ferroelectric capacitor, \(C_{NC}\), is given by Eq. (2). The capacitances of the coating and gate dielectric layers are taken in a standard form as \(C_C = \varepsilon_0S_C/d_C\) and \(C_g = \varepsilon_0S_g/d_g\), respectively. Here \(S_C = mL_C^2\) is the area of the ferroelectric, coating dielectric and gate dielectric plate surfaces, respectively.

The behavior of \(C_g\) defined by Eq. (3) is most generic and does not depend critically on the specific choice of materials. For practical applications, we choose both, the coating layer and the gate-dielectric layer, be composed of the Si-compatible dielectric HfO\(_2\) with the respective dielectric constants \(\varepsilon_g\), \(\varepsilon_C\) being approximately equal to 25. The ferroelectric disc of the diameter \(D_f \approx 6\) nm and thickness \(d_f \approx 3\) nm, can be fabricated out of the ferroelectric phase of HfO\(_2\) or its Zr-based modification, Hf\(_{0.75}\)Zr\(_{0.25}\)O\(_2\) with \(\varepsilon_f \approx 50^{3\text{3}}\). In fact, \(\varepsilon_f\) is the only relevant material parameter that defines the NC properties of the two-domain ferroelectric layer; therefore, the consideration applies equally well to other similar ferroelectrics, for instance, to pervoskite oxides, like strained PbTiO\(_3\) with about the same \(\varepsilon_f\). The height of the gate dielectric layer is taken as \(d_C \approx 3\) nm, whereas the thickness of the coating layer, \(d_g\), is equal to \(d_f\). The size of the rectangular floating-gate electrode, \(L_o\), defining the size of the gate dielectric capacitor, is taken as \(1.2L_c\).

Figure 2e displays the derived normalized gate capacitance, \(C_g = C_g/d_g\) as function of \(L_c\). The presented \(C_g(L_c)\) dependencies are the Eq. (3) plots, into which the given above capacitances, \(C_{NC}, C_C(L_c)\) and \(C_g(d_g)\) are substituted. Looking at the plots, one discriminates the three distinct regimes of the gate functioning set by two critical sizes, \(L_c < L_{c1}\), of the coating layer: (i) the super-capacitance, \(L_{c2} < L_c < L_{c1}\), (ii) the negative-capacitance, \(L_{c1} < L_c < L_{c2}\), and (iii) the near-zero capacitance, \(L_c < L_{c1}\). All these three distinct regimes are of tremendous relevance for applications. Below, we restrict ourselves to the detailed analysis of the NC regime, i.e., the regime where \(c_g < 0\), leaving the detailed discussion of regimes (i) and (iii) to forthcoming publication. Note that although in the NC regime the average polarization of the ferroelectric nanodot is aligned with the voltage drop across the capacitor, the electric field inside the coated layer is directed oppositely to it. Accordingly, the polarization induced inside the dielectric oxide sheath is opposite to the polarization of the ferroelectric nanodot, see Fig. 2f. It is important that the absolute value of the NC capacitance can be done arbitrary small on approach to the resonance regime \(|C_{NC}| = C_C\), of Equation (3), i.e., upon \(L_c \approx 0\). In regime the nonlinear effects in the \(Q-V\) characteristics of the MF capacitor become of prime relevance.

An unrestricted range of variation of \(C_g\), from minus infinity to zero, as seen from Fig. 2e, allows for the unlimited tuning of the magnitude of the gate NC. In particular, the possibility of making it arbitrary small, enables us to overcome a previously insurmountable obstacle of the proper matching between the gate, \(C_g\) and substrate, \(C_s\), capacitances and obtain the desirable value of the body factor

\[
m = 1 + \frac{C_s}{C_g} = 1 + \frac{C_s}{C_C} + \frac{C_s}{C_C - |C_{NC}|}
\]

within the NC FET operational interval \(0 < m < 1\), getting thus the remarkably low values of \(SS(I)\), the task not achievable by previously suggested architectures.

Now the task is to find the optimal coating size \(L_o\), given the normalized substrate capacitance \(C_s = C_s/d_S\) that ensures matching to targeted value of \(m\). To that end, we employ Eq. (4) which defines the implicit \(L\) dependence of \(C_g\) at given \(m\). The shown in Fig. 3a family of \(L_c(m)\) curves for different \(m\), confined between \(m = 0\) (red) and \(m = 1\) (brown) characteristics, represents the stable working interval for our exemplary c-MFMIS FET.

The region below the brown line where \(m > 1\), i.e., \(SS > 60\) mV dec\(^{-1}\), corresponds to small sizes of the coating layer, \(L_c < L_{c1}\). The region above the \(m = 0\) curve but below the \(L_c = L_{c2}\) line is the hysteretic loss of the reversibility region. Therefore, the proper choice of \(L_o\) in the interval \(L_{c2} < L_c < L_{c1}\), enables the desired magnitude of \(m\) for a given value of the substrate capacitance \(C_s\).

Although in our model example, the lateral size of the coating layer varies between \(L_{c1} \approx 24\) nm and \(L_{c2} \approx 38\) nm, it can be significantly reduced down to practically the diameter of the ferroelectric disc, by increasing the dielectric constant of the coating material by factor of four.

### Practical design. Optimal match between gate and substrate

The established characteristics of the c-MFMIS FET enable us to go beyond the past prima facie technological concepts and turn to the practical design in relevant industrial environment. The critical
To exemplify the nonlinear behavior of the substrate, we take the SS ensuring the best-performance capacitance and the semiconducting substrate capacitance steepest point of the SS having the steeper initial c subthreshold values, reduces near-threshold regime. Next, we set the condition with the voltage-independent substrate capacitance than the shown by the green curve commonly assumed NC FET the designed c-MFMIS FET with Fig. 3a, provides us with the optimal value of the size of the capacitancies region. The location of points A and B corresponds to the steep slope of the SS according to the devised above operating procedure starts with c-MFMIS FET, the green and blue curves show the I(Vd) dependencies for transistors with the steeper independent (green) and nonlinear in voltage (blue, with hysteresis) substrate capacitancies.

While being of a relatively low value when coming mainly from injected into the conducting channel, from the interface charges, comprises contributions from the capacitance of the depleted region. The location of points A and B corresponds to the steep slope of the SS according to the devised above operating procedure starts with c-MFMIS FET, the green and blue curves show the I(Vd) dependencies for transistors with the steeper independent (green) and nonlinear in voltage (blue, with hysteresis) substrate capacitancies.

In order to provide incorporating the two-domain c-MFMIS FET architecture into the industrially-standardized circuiting, we design the scalable compact model describing the Qg–Vg characteristics of the coated NC gate stack. In the low-voltage and low-charge operational mode of the NC FET, this compact model is defined by the linear relation Qg = CgVf where Cg is given by Eqs. (2) and (3). Looking forward to extensive applications of our compact model for the description of the c-MFMIS FET, we expand the compact model’s working range over to the nonlinear regime where substantial shifts of the domain wall and even its escape from the sample may occur.

The complete set of the Qg–Vg characteristics of the gate is defined by the individual electric properties of its components, including the gate dielectric capacitor, coating capacitor, and the MFM capacitor which form the equivalent circuit shown in Fig. 1f and which are characterized by the linear, Vd = CgQd, Vf = CgQf, and nonlinear, Vf = Vf(Qf), constitutive relations respectively. In general, the Vg–Qg characteristics can be parametrically plotted as functions of the running parameter Qf.

$$V_g = \left(1 + \frac{C_g}{C_{vd}}\right)V_f(Q_f) + \frac{Q_f}{C_{vd}}$$

$$Q_g = C_gV_f(Q_f) + Q_f$$

based on the relations Qg = Qd + Qf, Vg = Vd + Vf, and Vf = Vd for the circuit in Fig. 1f.

The nonlinear constitutive relation, Vf(Qf), of the MFM capacitor is the core relation that defines different regimes of the gate functioning. Shown in the Fig. 3c, are the results of the phase-field simulations (crosses), see Methods, and the analytical outcome of the developed scalable compact model (solid lines). The Qg–Vf characteristic reveals two different operational modes of the MFM capacitors. The NC low-charge branch, Vf(Qf) (red curve), corresponds to the two-domain state where the domain wall motion is responsible for the electric properties of capacitor. The high-charge branch, Vf(Qf) (blue curve), with the positive differential capacitance, Cg = dV/dQ > 0, corresponds to the monodomain state where the domain wall is gone. As a result, the Qg–Vf characteristic of the ferroelectric capacitor is presented.
by the synthetic dependence
\[ V_r(Q_r) = \begin{cases} V_2(Q_r) & \text{if } |Q_r| < Q_f^r(\alpha) \\ V_1(Q_r) & \text{if } |Q_r| > Q_f^r(\alpha) \end{cases} \]

where \( Q_f^r(\alpha) \) is the charge at which the branches \( V_2(Q_r) \) and \( V_1(Q_r) \) meet.

The corresponding to the monodomain state branch of the \( V_r(Q_r) \) characteristic, is given by the parametric dependence of \( V_1(Q_r) \) upon the polarization \( P \):
\[ V_1(P) = -d_f(2\alpha^2_P + 4\alpha_{33}^s P^3 + 6\alpha_{333}^s P^5) \]
\[ Q(P) = -\alpha^0 \left( P - \epsilon_0 \frac{\nabla \phi}{\epsilon_f} \right), \]

derived from the uniform Ginzburg-Landau equation. The coefficients \( \alpha^2_P \), \( \alpha_{33}^s \) and \( \alpha_{333}^s \), and the background dielectric constant \( \epsilon_f \) are defined in Methods.

For the \( V_2(Q_r) \) function describing the two-domain case we use the analytical approximation
\[ V_2(Q_r) \approx -0.27 \frac{Q_r}{Q_f^r(\alpha)} \frac{\psi(Q/Q_f^r(\alpha))}{C_f} \frac{D}{\epsilon_f}, \]

where \( \psi(s) \) (0 < s < 1), introduced in Luk’yanchuk et al., is the function accounting for the geometry of the system which we fit by
\[ \psi(s) \approx (1.0 - 0.027s - 0.95s^2 - 0.34s^3 + 0.32s^4)^{1/2}. \]

In the linear in \( Q_r \) approximation, where \( s \to 0 \), Eq. (8) gives \( C_{NC} \) in Eq. (2).

Combining branches given by Eqs. (7) and (8) provides an excellent approximation for the results of the numerical simulations of the compact model, see Fig. 3c. The slight shoots at \( \pm Q_f^r(\alpha) \) correspond to numerical singularities appearing at the moments when the DW leaves the MFM capacitor.

To summarize, the achieved understanding that the fundamental mechanisms of the NC is the domain action, bestows the spatial distribution of the polarization, is solved on the each respective relaxation step.

For practical implementation of simulations, we have used the open-source FEniCS computing platform. To create the tetrahedral finite-element meshes we used an open-source 3D mesh generator gmsh. For the case of the MFM capacitor, the computational region is a cylindrical domain, restricted by the side boundary, \( \partial_\Omega \), and by the top, \( \partial_\Omega_b \), and bottom, \( \partial_\Omega_w \), boundaries, see Fig. 4a. For the case of the MFSM heterostructure, the computational region is a rectangular box \( \Omega \) that includes the ferroelectric layer, \( \Omega_f \), and the semiconducting layer, \( \Omega_s \), see Fig. 4b. The computational region, \( \Omega \), is restricted by the left, right, front and back-side boundaries \( \partial_\Omega \), and by the top, \( \partial_\Omega_b \), and bottom, \( \partial_\Omega_w \), boundaries.

The solutions for the polarization, \( \mathbf{P}(t) \), and electrical potential, \( \phi(t) \), distribution were sought in the functional space of the piece-wise linear polynomials. For simulation of the MFM-capacitor, controlled by charge \( Q \), we use free boundary conditions for \( \mathbf{P}(t) \) on the whole surface of the cylinder. At the same time, it was assumed that the electrodes produce almost uniform \( z \)-directed electric field, \( E_z = -\partial \phi / \partial z \), spreading through the capacitor. The boundary constraint \( -Q/S_f = \mathbf{P} \cdot \mathbf{E}_z \) was used at the electrode interfaces to fix the applied charge \( Q \) that tunes the displacement of the DW in the spontaneously emerging two-domain structure. The bar denotes averaging over the interface surface.

For simulation of the MFSM heterostructure, the relaxation Eq. (11) was solved for the ferroelectric part of the sample while the electrostatic Poisson equation was solved for the whole domain. Boundary conditions for all the variables were taken to be periodic in the \( x \) direction. The size of the simulation rectangular box in \( x \)-direction, corresponding to the period of the spontaneously emerging domain structure was considered as an energy-minimizing parameter which was optimized for each series of calculations. Boundary conditions for \( \mathbf{P} \) on \( \partial_\Omega_b \) and \( \partial_\Omega_w \) as well as on the front- and back-side boundaries of the rectangular box were taken as free boundary conditions. The Dirichlet boundary conditions were imposed on \( \phi \) at the bottom and top surfaces of the box such that \( \phi(\partial_\Omega_w) = 0 \) and \( \phi(\partial_\Omega_b) = V \), to reproduce the application of the voltage \( U \) to the electrodes. The effective charge at the electrode was calculated as \( Q_e = -S_f(\mathbf{P} \cdot \mathbf{E}_z) \).

To approximate the time derivative in Eq. (11), we used the variable-time BDF2 stepper. The initial conditions for polarization distribution were taken to be random in the range of \( -10^{-6} \text{ C m}^{-2} \) for the polarization...
magnitude at the first time-step of simulation. The system of the nonlinear equations arising from the discretization of Eq. (11) was solved using the Newton-based nonlinear solver with line search and generalized minimal residual method with the restart. On each time step of the simulation in MFSM heterostructure, the linear system of equations obtained from the discretization of electrostatic Poisson equation was solved separately using a generalized minimal residual method with restart.

DATA AVAILABILITY
The data generated and analyzed during this study are available from the corresponding author upon reasonable request.

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I. Luk'yanchuk et al.

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I.L., Y.T., A.R., A.S. and V.M.V. conceived the work and performed calculations. I.L. and A.R. contributed to the theoretical analysis. V.M.V. wrote the manuscript.

COMPETING INTERESTS
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