PSCNN: A 885.86 TOPS/W Programmable SRAM-based Computing-In-Memory Processor for Keyword Spotting

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Abstract—Computing-in-memory (CIM) has attracted significant attentions in recent years due to its massive parallelism and low power consumption. However, current CIM designs suffer from large area overhead of small CIM macros and bad programmability for model execution. This paper proposes a programmable CIM processor with a single large sized CIM macro instead of multiple smaller ones for power efficient computation and a flexible instruction set to support various binary 1-D convolution Neural Network (CNN) models in an easy way. Furthermore, the proposed architecture adopts the pooling write-back method to support fused or independent convolution/pooling operations to reduce 35.9% of latency, and the flexible ping-pong feature SRAM to fit different feature map sizes during layer-by-layer execution. The design fabricated in TSMC 28nm technology achieves 150.8 GOPS throughput and 885.86 TOPS/W power efficiency at 10 MHz when executing our binary keyword spotting model, which has higher power efficiency and flexibility than previous designs.

I. INTRODUCTION

Convolution neural network (CNN) is widely used in many artificial intelligence and deep learning applications, such as classification, object detection, and keyword spotting [1]. To achieve higher accuracy in different applications, deeper and more complicated network structures have been developed that significantly increases the demands of computation and memory bandwidth. Thus, speedups with deep learning accelerators (DLAs) are necessary for low power and real-time applications. However, digital DLAs will consume considerable energy consumption and latency on data transmission between PE and memory due to separated computing and storage. Thus, computing-in-memory (CIM) becomes a more viable solution that combines computing and storage together [2]. The CIM macro uses its crossbar array structure for both weight storage and parallel computation that can achieve massive parallelism for computation and save energy for data transfer.

Previous CIM designs [2]–[4] are dedicated for certain applications or fail to consider programmability to execute models efficiently without complex control. This makes them hard to adapt to different layer execution or incur high control costs. Besides, these designs use multiple small macros to map the model, which is not area and energy efficient due to the large area overhead in small macros and lower available parallelism.

To address this issue, we propose a programmable SRAM-based CIM processor for CNN: PSCNN. This design uses a single large CIM macro for high power efficiency up to 886.5 TOPS/W for the keyword spotting application. With this large macro, we propose a comprehensive instruction set architecture that is easily programmable to support various binary 1-D CNN mode executions. Together with this, we adopt the pooling write-back method to accelerate fused or independent convolution/pooling operations, and the flexible ping-pong feature SRAM to fit various feature map sizes during layer-by-layer execution.

The rest of the paper is organized as follows. Section II presents the proposed architecture and its data flow. Section III shows the experimental results and comparisons with other designs. Finally, this paper is concluded in Section IV.

II. ARCHITECTURE AND DATAFLOW

A. Instruction set

Fig. 2 shows the proposed instruction set to program this processor. The instruction set is 32-bit wide and includes four types of instructions: multiply-accumulate (MAC), weight replacement, pointer and halt, depending on the first three bits of the instruction code.

The MAC instruction sets the layer execution type to be convolution or pooling, which is decided by the layer parameters. The weight replacement instruction controls the weight data exchanging between the CIM macro and the weight SRAM if the CIM macro cannot store the whole model. The pointer instruction sets the address of feature map access to dynamically decide the read starting address.
Fig. 2. Proposed instruction set

of the input feature map (IFM) and the write address of the output feature map (OFM) during model execution. The halt instruction stops the controller fetching instructions as long as the model execution is finished. With these instructions, we can easily program CIM without complex control.

B. Overview

Fig. 1 shows the overall architecture of PSCNN that is composed of a system controller, a flexible Ping-Pong SRAM system for I/O feature maps, and one CIM core. The controller extracts the instruction codes from the instruction register file and sends the corresponding control signal to the whole system. The CIM core contains a CIM macro, weight SRAM, a 1024-bit line buffer, and a pooling-write block (PWB). The adopted CIM macro based on [5] is a 1Mb SRAM CIM macro and consists of 1024 wordlines, 1024 bitlines, and 128 sense amplifiers (SAs).

C. Single core architecture with a large sized CIM macro

The small-sized CIM macro is not area and energy efficient. Previous works [3], [4] uses multiple small-sized CIM macros for large memory storage to store model parameters for model execution. A small-sized single CIM macro computes only a few multiplications and accumulations (MACs), or a partial sum of one output channel. The partial sums from different CIM macros need to be summed up together additionally by digital circuits. Thus, the output of the CIM macro is not the desired activation output but only intermediate values, which demands high-resolution analog-to-digital converters (ADCs) to sample the output of CIM macros for low truncation error of partial sum, and incurs large area and high power consumption. This situation occurs even for the binary activation network. This implies that the benefits of low precision network no longer exist.

In contrast, this paper adopts a single core architecture with a large-sized CIM macro for binary activation ternary weight networks. With 1024 wordlines, our CIM macro can compute 1024 MACs on a bitline to generate the final activation output directly without intermediate partial sums and corresponding burdens. Thus, simple SA instead of high resolution ADCs can be used for low power consumption. Besides, the communication network between macros is not necessary due to

one CIM core. This high parallelism enables high throughput and allows one channel one bitline mapping for low power consumption.

Besides, when executing a large CNN model, a small-sized CIM macro cannot accommodate the whole model and thus needs to update the weight frequently that will lead to considerable latency and energy consumption. To minimize the impact of weight updating, a large-size SRAM CIM macro is chosen in this work instead of a small-sized one. A large memory storage makes it possible to execute a large model without or with less weight updating need.

D. Ternary-weight mapping

The target model for this design is binary neural network (BNN) [6] models using binary precision \{+1, -1\} for weight and \{+1, 0\} for activation. A typical BNN mapping on a CIM macro will use one SRAM cell for one weight as shown in Fig. 3(a). After activating the wordlines, the currents on a bitline pair present the positive popcount and the negative popcount, respectively. An SA compares the currents between the positive one and the negative one instead of

Fig. 3. Difference between binary-weight and ternary-weight mapping

However, due to the nonideal effect of SA, if the current difference is too small, the actual result will not be detected correctly.

To prevent the functional failure from SA sensing variation, we replace binary weight mapping (BWM) by ternary weight mapping (TWM) [5]. As shown in Fig. 3(b), different from BWM, each weight of TWM occupies a pair of SRAM cells on two adjacent bitlines. After activating the wordlines, the currents on a bitline pair present the positive popcount and the negative popcount, respectively. An SA compares the currents between the positive one and the negative one instead of

\[
Dout \begin{cases} 
1, & I_{BL} - I_{Ref} \geq 0 \\
0, & I_{BL} - I_{Ref} < 0 
\end{cases}
\]
Fig. 4. Weight Mapping

comparing with the reference bitline. By this way, TWM requires no additional reference bitline, and the sensing margin is doubled as illustrated in Fig. 3(c). Thus, to increase the immunity to variation, we adopt TWM strategy instead of BWM in this work.

E. Data flow

The CIM macro stores weights in the memory and thus uses weight stationary dataflow for computation. Besides, since most of the model weights are available on chip, it is nature to route the macro output directly back to the macro input. Thus, the order of OFM has to be identical to the order of IFM for smooth execution.

Fig. 4 illustrates how to map IFM onto the input line buffer and weights to a crossbar array. The IFM and weights are both grouped based on position indexes, and are arranged in order sequentially. To make sure all outputs are in a correct order, the weights with the same output channel index are placed on the same bitline pair. Convolution layer computations can be done by shifting the IFM downward and activating wordlines alternately. By this mapping method, the order of the OFM can be ensured identical to the IFM, and thus the OFM can be written back directly without data reordering.

F. Flexible ping-pong feature SRAM

With the whole model stored on chip, it is nature to execute a model layer by layer and store OFM of each layer in the internal buffer instead of the external buffer to reduce external memory access. Thus, the OFM of the next layer, which can be implemented by a ping pong buffer. Fig. 5 shows the proposed flexible ping-pong feature SRAM with four 64Kb buffers to store input and output feature maps. This buffer works like a typical ping pong buffer that one buffer will serve as input and another buffer will serve as output for one layer execution and their roles will be switched for the next layer execution. In our design, the read pointer of IFM and the write pointer of OFM can be switched through the instruction assignment of each layer.

However, the conventional ping pong buffer design allocates a fixed size buffer for IFM and OFM, respectively, which could lead to the buffer underutilized as in Fig. 5 (a) due to the gradually shrinking OFMs by the pooling layers. To reduce such waste, this paper uses four 64Kb single port SRAM macros instead of two larger size ones. Through the instruction assignment, the addresses of IFM and OFM can be determined individually. The memory allocation can be assigned much appropriately, making the processor able to deal with a large-sized feature map, as shown in Fig. 5(c). Moreover, only two SRAMs will be either read or written during the convolution calculation. The other two SRAMs can be turned off to save power, as shown in Fig. 5(d).

G. Weight SRAM

Due to the TWM, the effective memory size of CIM macro is 512Kb for weight storage. Although this size is large, the modern model size could easily exceed this limit. Thus, weight updating is inevitable. However, weight updating from DRAM does not enjoy the parallelism of CIM macro and will cause significant latency and power consumption. To reduce latency and power, a 512Kb SRAM is used to store the remaining parameters of a large-sized CNN model. Through the instruction assignment, the parameters of the SRAM CIM macro can be replaced with the weight data stored in the weight SRAM if needed. With additional memory storage, PSCNN can handle large-sized CNN models in high speed and low power.

H. Pooling-Write Block (PWB)

A typical model usually has a pooling layer following a convolution layer. Separately executing these two layers will need to fetch convolution data from SRAM again for pooling, which consumes additional latency and power.

To avoid this, this paper proposes PWB that adds pooling operations after the output of SRAM CIM macro to skip the redundant data transfers because the OFM of a convolution
layer generated by CIM macro in every cycle is in order. Moreover, by this way, the pipelined convolution and pooling can avoid stalls and improve hardware utilization. By running the test model shown in Fig. 7, with the PWB supporting fused convolution and pooling operation, the execution latency is reduced by 35.9%. However, simply adding pooling units after the macro will limit its flexibility. In some cases, convolution and pooling need to be executed individually. In such a case, a shortcut path can be activated to bypass the SRAM CIM macro, as illustrated in Fig 6. In summary, by the instruction assignment, the convolution layer and pooling layer can be executed independently, or be fused together to reduce latency depending on the situation.

III. EXPERIMENTAL RESULTS

A. Network simulation result

Fig. 7 shows our binary keyword spotting model with 652Kb model size. The performance of the model is evaluated on the Google speech commands dataset (GSCD) [7]. The input sound data is 1 second length at 16kHz sampling rate, and quantized into 8 bits fixed point. The network detects 12 classes of keywords including unknown and silence from the input sound data. The inference accuracy is 92.53%.

B. Implementation results and comparison

The proposed design has been implemented on TSMC 28nm CMOS process. It can achieve 150.8 GOPS throughput and 885.86 TOPS/W power efficiency at 10 MHz with 23.4K gate counts (8,485.34 $\mu$m$^2$ in area), one 1Mb CIM macro, four 64Kb SRAM macros, and one 512Kb SRAM macro.

The performance is evaluated with PSCNN running the keyword spotting model shown in Fig. 7. For the test model, its 652Kb model size exceeds the size of the CIM macro. The remaining 140Kb parameters are stored in weight SRAM, and are used to update the weight of CIM macro when needed. Assume all weights have been preload in the CIM macro and the weight SRAM. Table. I shows the performance summary and comparison with other CIM-based designs for keyword spotting. [4] has lower throughput and power efficiency due to their high precision on weight and activation, which needs high resolution ADCs. [3] adopts tile-based architecture, high resolution ADCs, and additional adder trees to deal with multibit partial sum, which leads to lower power efficiency and higher energy consumption. Both [4] and [3] design dedicated dataflows for their own algorithms, which cannot be reconfigured for other models. Compared to other designs, this design has higher power efficiency and high flexibility for model execution.

IV. CONCLUSION

In this paper, we adopt the single large CIM core architecture to eliminate digital hardware overheads and to avoid the truncation error issue. Furthermore, we use ternary weight mapping instead of binary weight mapping to increase the immunity to SA variation. The proposed accelerator is easily programmed with a flexible instruction set to support various binary 1-D CNN models. In addition, the proposed architecture further reduces the latency by the pooling write back method and reduces the memory size requirement with a flexible ping-pong feature SRAM. The proposed design implemented with TSMC 28nm CMOS technology achieves 150.8 GOPS throughput and 885.86 TOPS/W power efficiency at 10 MHz when executing our binary keyword spotting model, which has better power efficiency than the the state-of-the-art designs.

ACKNOWLEDGMENT

This work was supported by the Ministry of Science and Technology, Taiwan, under Grant 109-2634-F-009-022, 109-2639-E-009-001, 110-2221-E-A49-148-MY3 and 110-2622-8-009-018-SB, and TSMC.
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