**ABSTRACT**

Despite the great success of High-Level Synthesis (HLS) tools, we observe several unresolved challenges: 1) the high-level abstraction of programming styles in HLS conceals optimization opportunities; 2) existing HLS tools do not provide flexible trade-offs among different objectives and constraints; 3) the actual quality of the resulting RTL designs is hard to predict. To this end, we propose an end-to-end framework, **IronMan**. The primary goal is to enable a flexible and automated design space exploration (DSE), which can provide either optimized solutions under user-specified constraints, or Pareto trade-offs among different objectives (e.g., resource types, area, and latency). **IronMan** consists of three components: 1) **GPP** (a highly accurate graph-neural-network-based performance predictor), 2) **RLMD** (a reinforcement-learning-based DSE engine that explores the optimized resource allocation strategy), and 3) **CT** (a code transformer that assists RLMD and GPP by extracting data flow graphs from original HLS C/C++) experimental results show that, 1) GPP achieves high prediction accuracy, reducing prediction errors of HLS tools by 10.9x in resource usage and 5.7x in timing; 2) RLMD obtains optimized or Pareto solutions outperforming genetic algorithm and simulated annealing by 12.7% and 12.9%, respectively; 3) **IronMan** can find optimized solutions perfectly matching various DSP constraints, with 2.5x fewer DSPs and up to 6x shorter latency than those of HLS tools. **IronMan** is also up to 400x faster than meta-heuristic techniques and HLS tools.

**CCS CONCEPTS**

- Hardware → Electronic design automation.

**KEYWORDS**

High-Level Synthesis; Graph Neural Network; Reinforcement Learning; Design Space Exploration

**1 INTRODUCTION**

High-Level Synthesis (HLS) benefits ASIC and FPGA design automation by enabling automated transformation from behavioral descriptions in high-level languages (C/C++, etc.) to RTL-level designs. In addition to widely used commercial HLS tools for FPGA [18] and ASIC [1], recent efforts focus on improving RTL design quality [2, 22], performance and resource prediction [8, 19, 20], design space exploration (DSE) [12], etc.

Despite great achievement shown by previous efforts, there are several crucial challenges unaddressed. 1) **Higher level abstractions in HLS can obstruct optimization opportunities.** The structured HLS coding style, such as loops and function calls, hinders advanced or fined-grained performance and resource optimization. Meanwhile, the irregular logic, cascaded and imperfect loops in HLS programs usually require manual or complicated code transformations to improve hardware implementation performance [7]. Table 1 demonstrates a simple multiplication-accumulation function using a for-loop. To explore trade-offs between the DSP usage and the number of clock cycles (latency), typical ways are to use **unroll** pragmas or manual loop-tiling, as line 1-4. However, when the loop boundary (e.g., 8) is not divisible by the DSP constraint (e.g., 3), it results in a **partial unrolling** as line 4, introducing undesired latency increment (from 4 to 8) and worsening the critical path (CP) timing (from 5ns to 7.4ns). The nested loops further complicate this problem (imagine a 5-layer nested loop with a DSP constraint of 17). Motivated by the necessity of **better performance and more flexible optimization choices**, we propose a **code transformer (CT)**. CT easily allows to use directives, such as **allocation** and resource pragmas, to conduct finer-grained DSEs for resource and performance, as line 7-11 in Table 1.

2) **HLS tools do not always provide the best solution, nor automatically provide trade-offs (Pareto solutions).** Existing DSE approaches as well as commercial HLS tools do not provide flexible trade-offs among different objectives and constraints (e.g., different types of resources), and they usually sacrifice design latency for less resource, or vise versa [12]. In contrast, one potential alternative is to trade one type of resource for another (e.g., LUT and DSP in FPGA) while maintaining the latency, which is unexplored and only can be done through tedious manual efforts. An example shown in Fig. 2 explores fine-grained trade-offs between LUTs and DSP’s: first, the HLS default solution is not on the Pareto frontier; second, there is a large design space for finding the Pareto solutions, and thus the **DSE for Pareto solutions is non-trivial.** Notably, the solution space grows exponentially even for a binary selection of DSP/LUT for each multiplication, which is further complicated by different data precisions (bitwidth). Motivated by the necessity...
and difficulty of flexible and fine-grained DSE, we propose a deep reinforcement learning (RL) based DSE tool, RLMD.

3) The real quality of the resulting RTL designs is hard to predict, especially for irregular data paths. Most existing model-based predictors target well-structured data flows, such as perfect and nested loops with high-level directives [19, 21]. As such, these predictors and high level DSE tools are not suitable for irregular logic and data paths (especially for timing estimation).

While machine-learning-based predictions are feasible [3, 8, 20], they often require abundant features after design synthesis and/or implementation. Fortunately, the inherent graph structure of dataflow graphs (DFGs) provides a promising opportunity to exploit the representative power of graph neural networks (GNNs) [4, 6, 11]. Motivated by the necessity of DSE and high-accuracy prediction for irregular data paths and the intrinsic graph structure of DFGs, we propose a GNN-based HLS performance predictor, GPP, enabling RLMD for DSE on arbitrary DFGs.

By seamlessly integrating the three aforementioned components, we propose an end-to-end framework, namely IronMan, as depicted in Fig. 1. IronMan has two major goals: 1) to enable a flexible and automated DSE, aiming to explore various trade-offs among different objectives such as resource types and latency; 2) to provide an accurate RTL design performance predictor, which does not require any additional features except the original DFG, supporting both regular and irregular data paths. We briefly introduce the components and summarize our contributions as follows.

• **GPP**: a highly accurate GNN-based performance predictor for HLS designs, including resource utilization (DSP/LUT) and critical path (CP) timing. It predicts the actual performance after physical synthesis (placement and routing) rather than the synthesized results by HLS tools, and can generalize to unseen DFGs.

• **RLMD**: a deep RL-based multi-objective DSE engine for resource allocation in HLS. Assisted by GPP, RLMD explores optimized resource allocation strategy under user-specified constraints. The objectives include minimizing resource utilization, optimizing CP timing and/or minimizing DFQ computation latency. RLMD also provides Pareto solutions among different objectives, which are unavailable in HLS tools.

• **CT**: a code transformer that extracts DFGs from original HLS C/C++ and re-generates synthesizable code with HLS directives optimized by RLMD. CT reveals concealed optimization opportunities for achieving higher parallelism, and enables flexible and finer-grained DSE under user-specified constraints.

• **IronMan**: while each proposed component alone can contribute to the HLS community (performance prediction, DSE, code transformation), we integrate them into a framework, IronMan, and demonstrate the end-to-end benefits on real-world benchmarks.

### Table 1: Approaches to meeting DSP constraints (e.g., \( \leq 3 \)). This work explores CT+resources approaches (line 9-11), which achieve the best latency under the constraint. An alternative to constrain DSP is to use #pragma HLS allocation instance=mul, while increasing latency (line 7,8).

| Method | Cycles | DSP | LUTs | CP (ns) |
|--------|--------|-----|------|---------|
| 1      | Orig.  | 17  | 1    | 75      | 4.07    |
| 2      | unroll (factor=3, complete) | 2 | 8 | 100 | 3.04 |
| 3      | unroll (factor=4) | 4 | 4 | 87 | 4.83 |
| 4      | unroll (factor=3) | 8 | 3 | 109 | 7.44 |
| 5      | unroll + allocation (limit=3) | 4 | 6 | 168 | 8.76 |
| 6      | t-code transform (t=1) | 2 | 8 | 100 | 3.03 |
| 7      | C1 + allocation (limit=2) | 3 | 3 | 196 | 9.91 |
| 8      | C1 + allocation (limit=3) | 4 | 6 | 168 | 8.54 |
| 9      | C1 + resource (5 Mul, LUT) | 2 | 2 | 1742 | 4.24 |
| 10     | C1 + resource (4 Mul, LUT1) | 2 | 2 | 1741 | 4.01 |
| 11     | C1 + resource (3 Mul, LUT1) | 2 | 2 | 1661 | 3.98 |

* HLS pragmas do not always behave as expected.

### Figure 2: Pareto solutions between DSPs and LUTs on an FPGA, achieved by specifying certain multiplications using LUTs instead of DSPs. The input DFG has 200 operations.

### 2 OVERALL FRAMEWORK

The overall framework of IronMan is shown in Fig. 1. The inputs are HLS C/C++ code and user-specified constraints. The output is the re-generated code with optimized HLS directives, either meeting the user-specified constraints (e.g., resource or latency), or providing Pareto solutions among different optimization objectives.

CT extracts the intrinsic DFGs from the intermediate representations (IRs) of HLS tools to release more optimization opportunities, and then re-generates synthesizable C/C++ code with optimized directives. Fig. 3 (a) exemplifies how CT re-generates C++ code, with the extracted DFG in (b). Each intermediate operator may have various bit-width, e.g., (12) means a 12-bit data precision.

**GPP**, a GNN-based performance predictor, estimates the actual resource usage after physical synthesis of DFGs. GNNs [4, 6, 11] are adopted for three reasons. 1) DFGs are graphs, which are naturally suitable for GNNs to learn the underlying information from graph structures. 2) DFGs vary in topologies and sizes, and in order to generalize predictions to unseen graphs, it is necessary to use inductive GNNs [4] to learn fixed-size graph embeddings. 3) IronMan runs inferences of trained GNN models during execution, which is orders of magnitude faster than running HLS tools.
RLM, an RL-based DSE engine, takes DFGs, their corresponding graph embeddings, and user-specified constraints as inputs, to make endeavors for optimal resource allocation strategy. RL is adopted for two main reasons. 1) The design space grows exponentially with the size of DFGs, different graph topologies, and various data precision. RL has been widely applied for proactive DSE in computer systems [17], and a well pre-trained agent can generalize to new problems by minimal fine-tuning efforts. 2) By carefully defining reward functions, RL agents can achieve multi-objective optimization automatically, getting rid of manual efforts to craft useful heuristics. An informative and well-crafted state representation will significantly benefit the learning process in RL problems, motvating the integration of GPP and RLMD. Consequently, the graph embeddings enable RLMD to generalize across different DFG topologies, and GPP largely accelerates the training process of RLMD by quickly evaluating solutions generated by RLMD.

As a case study of IronMan, the specific problem solved is to find a resource allocation solution that strictly meets the DSP constraint, to find Pareto solutions between DSPs and LUTs on FPGAs, without sacrificing computation latency. For simplicity, the DFGs only have additions and multiplications, where the key role of a GNN is to extract adequate information of node types, graph topology and connectivity within a large DFG, and encode the information into low-dimension vector representations that can be used for downstream tasks.

### 3 PROPOSED GPP AND RLMD

#### 3.1 GPP

The key role of a GNN is to extract adequate information of node types, graph topology and connectivity within a large DFG, and encode the information into low-dimension vector representations that can be used for downstream tasks.

**Node Feature Vector.** In a DFG, each node is encoded into a 10-dimension node feature vector, as the example shown in Fig. 3(d). The 1st to 4th dimension use one-hot representations to encode the node types, including input nodes, intermediate nodes/operations (additions and multiplications), and output nodes. The 5th to 9th dimension encode the data precision of an intermediate operation, which in this work ranges from INT2 to INT32. We use a binary representation to encode the precision minus one, so the bit-width can be expressed in 5 bits. The 10th dimension indicates whether an HLS directive #pragma HLS resource is applied to this node. Note that such an encoding scheme can be easily extended to support more types of nodes/operations or pragmas.

**Graph Embedding.** We employ three CNN models of the same structure to separately predict LUT/DSP usage and CP timing, as illustrated in the left part of Fig. 4. For each CNN model, the inputs are adjacency matrices and node feature matrices of DFGs. The first two layers are graph convolutional [6], with 64 and 128 units respectively and ReLu activations. In each graph convolutional layer, the node embedding is updated by aggregating feature vectors from its neighbors, and one node can receive information from farther nodes by stacking multiple layers. Next, the learned node embeddings are summarized by a mean pooling to create a graph representation (i.e., a 128 × 1 vector). This representation is then passed to a feed-forward network with three fully connected layers and leaky ReLu (α = 0.1) activations to generate a graph embedding (i.e., a 64 × 1 vector). The last layer is the output, involving a single unit with ReLu activation to provide the prediction result.

**Integration with RLMD.** To integrate with RLMD, we combine the three embedding vectors that focus on different characteristics of DFGs into one graph embedding, shown as the 192 × 1 vector in Fig. 4. Finally, the graph embedding vector is concatenated with the meta data of the input DFG, and passed to RLMD as its inputs. The DFG meta data include the size of the DFG (i.e., the number of input/intermediate/output nodes and the number of edges) and the number of multiplications in this DFG. Given predictions of LUT/DSP/CP, solutions generated by RLMD can be quickly evaluated, providing feedback to further improve the policy of RLMD.

#### 3.2 RLMD

**RL Formulation.** The resource allocation problem in HLS, as a typical RL [13] problem, can be formulated as a Markov Decision Process (MDP), with four key components.

- **States:** the set of possible states. In this problem, a state can be every possible partially assigned DFGs.
- **Actions:** the set of eligible actions under a state. In this problem, given the current state and the currently considered node of the DFG, the action is whether to assign the directive to this node.

```plaintext
Original Code:
for (int i=0; i<4; i++) sum += a[i] * b[i];
```

```plaintext
Transformed Code with resource pragma
#pragma HLS resource variable=a core=Mul_LUT
#pragma HLS resource variable=b core=Mul_LUT
```

- **Rewards:** given the current state and the currently considered node of the DFG, the action is whether to assign the directive to this node.
- **Policy:** a mapping from state to action: π(s) = a. 

Figure 3: An example of IronMan solution. (a) The original HLS code and transformed code with resource pragma, indicating the importance of CT for IronMan. (b) HLS default solution (4 DSPs and a latency of 3); (c) HLS solution with naive constraints (2 DSPs while increasing latency from 3 to 4); (d) IronMan solution (2 DSPs and an unchanged latency).

RLM, an RL-based DSE engine, takes DFGs, their corresponding graph embeddings, and user-specified constraints as inputs, to make endeavors for optimal resource allocation strategy. RL is adopted for two main reasons. 1) The design space grows exponentially with the size of DFGs, different graph topologies, and various data precision. RL has been widely applied for proactive DSE in computer systems [17], and a well pre-trained agent can generalize to new problems by minimal fine-tuning efforts. 2) By carefully defining reward functions, RL agents can achieve multi-objective optimization automatically, getting rid of manual efforts to craft useful heuristics. An informative and well-crafted state representation will significantly benefit the learning process in RL problems, motvating the integration of GPP and RLMD. Consequently, the graph embeddings enable RLMD to generalize across different DFG topologies, and GPP largely accelerates the training process of RLMD by quickly evaluating solutions generated by RLMD.

As a case study of IronMan, the specific problem solved is to find a resource allocation solution that strictly meets the DSP constraint, to find Pareto solutions between DSPs and LUTs on FPGAs, without sacrificing computation latency. For simplicity, the DFGs only have additions and multiplications, where the key role of a GNN is to extract adequate information of node types, graph topology and connectivity within a large DFG, and encode the information into low-dimension vector representations that can be used for downstream tasks.

**Node Feature Vector.** In a DFG, each node is encoded into a 10-dimension node feature vector, as the example shown in Fig. 3(d). The 1st to 4th dimension use one-hot representations to encode the node types, including input nodes, intermediate nodes/operations (additions and multiplications), and output nodes. The 5th to 9th dimension encode the data precision of an intermediate operation, which in this work ranges from INT2 to INT32. We use a binary representation to encode the precision minus one, so the bit-width can be expressed in 5 bits. The 10th dimension indicates whether an HLS directive #pragma HLS resource is applied to this node. Note that such an encoding scheme can be easily extended to support more types of nodes/operations or pragmas.

**Graph Embedding.** We employ three CNN models of the same structure to separately predict LUT/DSP usage and CP timing, as illustrated in the left part of Fig. 4. For each CNN model, the inputs are adjacency matrices and node feature matrices of DFGs. The first two layers are graph convolutional [6], with 64 and 128 units respectively and ReLu activations. In each graph convolutional layer, the node embedding is updated by aggregating feature vectors from its neighbors, and one node can receive information from farther nodes by stacking multiple layers. Next, the learned node embeddings are summarized by a mean pooling to create a graph representation (i.e., a 128 × 1 vector). This representation is then passed to a feed-forward network with three fully connected layers and leaky ReLu (α = 0.1) activations to generate a graph embedding (i.e., a 64 × 1 vector). The last layer is the output, involving a single unit with ReLu activation to provide the prediction result.

**Integration with RLMD.** To integrate with RLMD, we combine the three embedding vectors that focus on different characteristics of DFGs into one graph embedding, shown as the 192 × 1 vector in Fig. 4. Finally, the graph embedding vector is concatenated with the meta data of the input DFG, and passed to RLMD as its inputs. The DFG meta data include the size of the DFG (i.e., the number of input/intermediate/output nodes and the number of edges) and the number of multiplications in this DFG. Given predictions of LUT/DSP/CP, solutions generated by RLMD can be quickly evaluated, providing feedback to further improve the policy of RLMD.
where which is an estimate of total rewards starting from state \( \pi \) on the current node, and a scalar as the state-value function.

of a DFG), leading to the updates as follows:

after one complete episode (i.e., one complete assignment process in the right part of Fig. 4, there are shared parameters in the actor \( \pi \) following policy \( V \) Carlo learning \[ 13 \]: the actor aims to learn an optimal policy to maximize the expected rewards received. The goal is to maximize the expected rewards received. Based on their node IDs. Given \( s \) unassigned. At each time step \( t \) \( r \) reward \( \delta \) is defined as a negative weighted sum of predicted \( \alpha \) and \( \beta \) are hyper-parameters.

At the initial state \( s_0 \), all the multiplication nodes in a DFG are unassigned. At each time step \( t \), the RL agent observes the current state \( s_t \), takes an action \( a_t \), receives a reward \( r_{t+1} \) and arrives at a new state \( s_{t+1} \). The nodes are assigned with directives sequentially based on their node IDs. Given \( T \) multiplication nodes in total, the final state \( s_T \) corresponds to a DFG completely assigned with proper directives. The goal is to maximize the expected rewards received.

**RLMD Training.** We adopt the actor-critic method with Monte-Carlo learning \[ 13 \]: the actor aims to learn an optimal policy \( \pi_\theta(a_t|s_t) \) parameterized by \( \theta \), which is a probability distribution of valid actions under the current state; the critic approximates the state-value function \( V(s_t) = \mathbb{E}_\pi[\sum_{t'=t}^{T} \gamma^{t'-t} r_{t'+1} | s_t] \) by parameters \( w \), which is an estimate of total rewards starting from state \( s_t \) to \( s_T \) following policy \( \pi \). The \( \gamma \in (0, 1) \) is the discount factor. As shown in the right part of Fig. 4, there are shared parameters in the actor \( \pi_\theta \) and the critic \( V_\psi \), and for clarity we denote \( \theta \) and \( \psi \) separately. By Monte-Carlo learning, the parameters are updated only once after one complete episode (i.e., one complete assignment process of a DFG), leading to the updates as follows:

where \( T \) is the total time steps in one episode. Through repeated episodes (i.e., sequences of states, actions, and rewards), the actor learns optimized policy that will maximize cumulative rewards.

Our ultimate goal is to enable RLMD to generate higher-quality results and transfer knowledge across various DFGs as it gains experience from exploring resource allocation strategies on more and more DFGs. Thus, we formally formulate the overall optimization objective function as:

\[
J(\theta, w, G) = \frac{1}{K} \sum_{g,l} \mathbb{E}_{s_{g,l}} \left[R_{g,l}\right].
\]

where \( J(\theta, w, G) \) measures the total expected rewards over all training DFGs. The dataset \( G \) has \( K \) different DFGs, each of which is denoted as \( g, R_{g,l} \) is the episode reward (i.e., \( r_T \) in Eq.(1)) under the resource allocation \( l \) on the DFG \( g \). To get better exploration during training, we apply \( \epsilon \)-greedy algorithm for action selections \[ 13 \].

**RLMD Fine-tuning.** Given an unseen DFG, the simplest way is to directly apply the pre-trained RLMD for inference, which can generate a solution within a second. When higher quality solutions are expected, the pre-trained RLMD can be further finetuned on this particular DFG. The fine-tuning step provides the flexibility to trade off between a quick solution using the pre-trained RLMD (which has learned rich knowledge of resource allocation strategies on other DFGs) and a longer yet better one for a particular DFG.

## 4 EXPERIMENT

### 4.1 Experiment Setup

**Dataset Generation.** To train GPP and RLMD, we build a dataset of both synthetic and real-case DFGs, which are generated by our CT. For synthetic DFGs, we randomly generate 47 different topologies, each of which has 100 to 200 operations (i.e., intermediate nodes) of either multiplication or addition. Upon each distinct topology, we generate 100 sets of directives, specifying a subset of multiplications to be implemented by LUTs rather than DSPs. This makes up 4700 (i.e., \( 47 \times 100 \)) different synthetic DFGs. For real-case DFGs, 8 benchmarks from MachSuite \[ 10 \], CHStone \[ 5 \] and PolyBench/C \[ 9 \] are considered: gemm, kernel_2mm, kernel_durbim (small, large), spmv, stencil3d (small, large), and kernel_adi. Similarly, we randomly generate 100 sets of directives per benchmark, making up 800 real-case DFGs. The ground-truth (actual) resource usage (LUT/DSP) and CP timing are synthesized by Vivado HLS \[ 18 \] and implemented by Vivado \[ 15 \] targeting Xilinx Ultra96 part xc7z020clg484.
4.2 Evaluation

**Baselines.** To evaluate GPP, we compare with the commercial tool Vivado HLS [18] and the learning-based performance predictor, Pyramid [8]. To evaluate IronMAN, we compare with genetic algorithm (GA) [16], simulated annealing (SA) [14], and the solutions provided by Vivado HLS [18]. Notably, none of the state-of-the-art DSE methods for HLS [12] can do such a fine-grained resource allocation as we proposed in this work, which is enabled by our CT.

GPP vs. HLS tool and Pyramid [8]. GPP is evaluated on both synthetic and real-case DFGs. Fig. 5 compares GPP predictions with HLS synthesis reports regarding LUT, DSP and CP timing. For LUT usage, the mean absolute percentage errors (MAPEs) of GPP on synthetic and real-case DFGs are 7.4% and 9.2%, whereas the MAPEs of Vivado HLS are 122.4% and 92.2%, respectively. For DSP usage, the prediction accuracy is measured by root-mean-square error (RMSE) since MAPE is not applicable when the ground truth appears to be zero. GPP achieves 5.6 and 2.1 in RMSE for synthetic and real-case DFGs, while Vivado HLS reaches 26.9 and 19.7, respectively. For CP timing, the MAPEs of GPP are 4.2% and 4.6% on synthetic and real-case DFGs, whereas the MAPEs of Vivado HLS are 7.7% and 42.1%. On average, GPP reduces the prediction error of Vivado HLS by 10.9× in resource and 5.7× in timing.

Pyramid [8] is also an ML-based framework for resource and timing prediction. The major difference between GPP and Pyramid is the features required for predictions. Pyramid needs 72 features from HLS reports as inputs, which enforce the running of HLS to get VHDL designs, possibly consuming hours for large designs; whereas GPP can make high-accuracy predictions simply from raw DFGs (within a second). Pyramid considers four ML models and an ensemble of these four, none of which includes graphical structure. The reported results show that the averaged prediction error of a single ML model is 17.8% for resource and 17.3% for timing, with the ensemble reaching 5.5% for resource and 4.1% for timing.

**RLMD vs. GA/SA.** Fig. 6 compares RLMD with GA and SA regarding the Pareto solutions between LUTs and DSPs. Obviously, RLMD outperforms GA and SA by a large margin. Given the same number of DSPs, RLMD can find solutions reducing the LUT usage by 12.7% and 12.9%, compared with SA and GA. After fine-tuning, additional 11.6% reduction in LUT utilization is achieved.

These promising results show great potentials of applying RL for DSE in HLS. Through trials and interactions with GPP and user-specified constraints, RLMD is able to gradually understand which directive should be assigned to which node, and proactively learn proper resource allocation strategies by balanced exploration and exploitation. In contrast, one underlying assumption in GA is that the offspring of two strong individuals among a population is often stronger, which is not the case in DSE for HLS problems, thus reducing its effectiveness. Similarly, SA is a probabilistic technique and uses meta-heuristic aiming to approximate the global optima,
which ignores past experiences and searches solutions to some extent hinging on randomness, thus not always reliable.

**IronMan vs. All.** As depicted in Fig. 7, IronMan is fully evaluated by comparing with SA, GA and Vivado HLS on four real-case benchmarks, whose sizes are 2 – 4x larger than synthetic DFGs. To showcase IronMan capable to perfectly satisfy user specifications without sacrificing latency, we specify different DSP constraints within 20% to 80% of the maximal number of DSPs for each case.

Among four real-case benchmarks with 40 different DSP constraints in total, IronMan is able to meet 39 (97.5%) of them, and can further improve to 40 (100%) by fine-tuning. Whereas SA, GA and Vivado HLS only meet the constraints for 2 (5%), 6 (15%) and 0 cases, respectively. Specifically, IronMan on average consumes 98.5% of the targeted DSPs (improved to 99.3% with fine-tuning), whereas those found by SA, GA and Vivado HLS use 1.29\% × 1.43\% × 2.54\% targeted DSPs, respectively. Not only can IronMan meet user-specified constraints much more accurately than its counterparts and HLS tools, but it also maintains the shortest latency whereas Vivado HLS results in an increased latency by up to 6x.

Reducing DSPs without sacrificing latency is at the cost of increased LUTs, because the DSP resource is often more critical in FPGAs while LUTs are more adequate. By perfectly satisfying DSP constraints, IronMan slightly increases the LUT usage by 1.2% and 3.0%, compared with SA and GA; with further fine-tuning, IronMan achieves additional 8.9% LUT reduction, resulting in 7.7% and 5.9% lower LUT usage than SA and GA.

**Execution Time.** During inference, i.e., being applied on real applications, IronMan only takes a few seconds for prediction and solution generation. Vivado HLS takes tens of minutes to synthesize C++ code, and up to hours to get the exact resource usage after implementation. SA and GA take hours in average, as they struggle to closely meet the DSP constraint, and cannot generalize across different DFGs or DSP constraints. The fine-tuning for RL agent can balance between a quick solution using the pre-trained model and a longer yet better one for a particular DFG, which is optional and the number of episodes is adjustable regarding users’ requirements.

**Conclusion**

IronMan is an end-to-end framework, aiming to help HLS tools generate higher quality solutions under user-specified constraints, or perform more flexible DSEs to provide Pareto solutions that are not currently supported by HLS tools. IronMan is equipped with a GNN-based performance predictor GPP, an RL-based DSE engine RLMD, and a code transformer. Independently, GPP achieves high prediction accuracy; RLMD obtains Pareto solutions surpassing GA and SA. Integrated, IronMan is capable to find optimized solutions perfectly matching various DSP constraints, with up to 400× faster than the heuristic algorithms and HLS tools.

**References**

[1] Cadence. Accessed: 2021. Cadence Stratus High-Level Synthesis. https://www.cadence.com/en_US/home/tools/digital-design-and-sigoff/synthesis/stratus-high-level-synthesis.html.
[2] Jason Cong et al. 2012. Optimizing memory hierarchy allocation with loop transformations for high-level synthesis. In 49th DAC.
[3] Steve Dai et al. 2018. Fast and accurate estimation of quality of results in high-level synthesis with machine learning. In FCCM.
[4] Will Hamilton et al. 2017. Inductive representation learning on large graphs. In NeurIPS.
[5] Yuko Hara et al. 2009. Proposal and quantitative analysis of the CHStone benchmark program suite for practical C-based high-level synthesis. J. BIP 17 (2009), 242–254.
[6] Thomas N Kipf and Max Welling. 2017. Semi-supervised classification with graph convolutional networks. ICLR (2017).
[7] Johannes de Fine Licht et al. 2018. Transformations of High-Level Synthesis Codes for High-Performance Computing. arXiv:1805.08288 (2018).
[8] Hosein Mohammadi Makrani et al. 2019. Pyramid: Machine Learning Framework to Estimate the Optimal Timing and Resource Usage of a High-Level Synthesis Design. In 29th FPL.
[9] Louis-Noël Pouchet and Tomofumi Yuki. 2016. PolyBench/C - the Polyhedral benchmark suite. http://web.cs.ucla.edu/~pouchet/software/polybench.
[10] Brandon Reagen et al. 2014. MachSuite: Benchmarks for Accelerator Design and Customized Architectures. In ISWSC.
[11] Franco Scarselli, Marco Gori, Ah Chung Tsoi, Markus Hagenbuchner, and Gabriele Monfardini. 2008. The graph neural network model. IEEE Transactions on Neural Networks. 20, 1 (2008), 61–80.
[12] Benjamin Carrión Schafer and Zi Wang. 2019. High-level synthesis design space exploration: Past, present and future. IEEE TCAD (2019).
[13] Richard S Sutton and Andrew G Barto. 2018. Reinforcement learning: An introduction. MIT press.
[14] Peter JM Van Laarhoven and Emule HL Aarts. 1987. Simulated annealing. In Simulated annealing: Theory and applications. Springer, 7–15.
[15] Vivado. Accessed. 2021. Vivado Design Suite - HLS Editions. https://www.xilinx.com/products/design-tools/vivado.html.
[16] Darrell Whitley. 1994. A genetic algorithm tutorial. Statistics and computing 4, 2 (1994), 65–85.
[17] Nan Wu and Yuan Xie. 2021. A Survey of Machine Learning for Computer Architecture and Systems. arXiv preprint arXiv:2102.07952 (2021).
[18] Xilinx. Accessed: 2021. Xilinx Vivado High-Level Synthesis. https://www.xilinx.com/products/design-tools/vivado/integration/els-design.html.
[19] Jieru Zhao et al. 2017. COMBA: A comprehensive model-based analysis framework for high level synthesis of real applications. In ICCAD.
[20] Jieru Zhao et al. 2019. Machine learning based routing congestion prediction in fpga high-level synthesis. In DATE.
[21] Guanzwen Zhong et al. 2016. Lin-analyzer: a high-level performance analysis tool for FPGA-based accelerators. In 53rd DAC.
[22] Wei Zuo et al. 2013. Improving high level synthesis optimization opportunity through polyhedral transformations. In FPGA.