A Survey and Perspective on Artificial Intelligence for Security-Aware Electronic Design Automation

DAVID KOBLAH, RABIN ACHARYA, DANIEL CAPECCI, and OLIвора DIZON-PARADIS, University of Florida
SHAHIN TAJIK and FАTEMEH GANJI, Worcester Polytechnic Institute
DAMON WOODARD and DOMENIC FORTE, University of Florida

Artificial intelligence (AI) and machine learning (ML) techniques have been increasingly used in several fields to improve performance and the level of automation. In recent years, this use has exponentially increased due to the advancement of high-performance computing and the ever-increasing size of data. One of such fields is that of hardware design—specifically the design of digital and analog integrated circuits, where AI/ML techniques have been extensively used to address ever-increasing design complexity, aggressive time to market, and the growing number of ubiquitous interconnected devices. However, the security concerns and issues related to integrated circuit design have been highly overlooked. In this article, we summarize the state-of-the-art in AI/ML for circuit design/optimization, security and engineering challenges, research in security-aware computer-aided design/electronic design automation, and future research directions and needs for using AI/ML for security-aware circuit design.

CCS Concepts: • Hardware → Electronic Design Automation; • Security and privacy → Security in hardware; • Computing Methodologies → Machine Learning;

Additional Key Words and Phrases: Integrated circuit, deep learning, reinforcement learning, security primitive

ACM Reference format:
David Koblah, Rabin Acharya, Daniel Capecci, Olivia Dizon-Paradis, Shahin Tajik, Fatemeh Ganji, Damon Woodard, and Domenic Forte. 2023. A Survey and Perspective on Artificial Intelligence for Security-Aware Electronic Design Automation. ACM Trans. Des. Autom. Electron. Syst. 28, 2, Article 16 (March 2023), 57 pages. https://doi.org/10.1145/3563391

1 INTRODUCTION

With the proliferation of IoT devices, and the ever-increasing design complexity of electronic systems, artificial intelligence (AI) and machine learning (ML) techniques have been increasingly used to optimize electronic design automation (EDA) frameworks and accelerate the overall

D. Koblah and R. Acharya contributed equally to this research.
Authors’ addresses: D. Koblah (corresponding author), R. Acharya, D. Capecci, O. Dizon-Paradis, D. Woodard, and D. Forte, Florida Institute for Cybersecurity (FICS) Research, University of Florida, 601 Gale Lemerand Dr, Gainesville, FL 32603; emails: dkoblah@ufl.edu, rabin.acharya@ufl.edu, dcapecci@ufl.edu, paradiso@ufl.edu, dwoodard@ece.ufl.edu, dforte@ece.ufl.edu; S. Tajik and F. Ganji, Worcester Polytechnic Institute, 100 Institute Road, WPI - Atwater Kent Laboratories, Worcester, MA 01609; emails: stajik@wpi.edu, fganji@wpi.edu.
Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyrights for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, or republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permissions from permissions@acm.org.
© 2023 Association for Computing Machinery.
1084-4309/2023/03-ART16 $15.00
https://doi.org/10.1145/3563391

ACM Transactions on Design Automation of Electronic Systems, Vol. 28, No. 2, Article 16. Pub. date: March 2023.
process. The physical platform, or hardware, represents the first stage for any layered security approach and provides the initial protection mechanisms to help ensure that preliminary security controls can be trusted. Hence, it is considered to be the “root of trust” of any electronic system. However, research over the past two decades has revealed that the hardware establishing these systems can no longer be considered secure and trusted. Incidents like Meltdown [153] and Spectre [130], the Big Hack of 2018 [212], the 63% rate of security breaches among organizations due to hardware vulnerabilities in 2019 [27], and the recent surge of fake components on the market due to the ongoing global chip shortage [141] are some of the most recent examples of hardware security-related issues. They are partly the result of the shift in the supply chain paradigm from a vertical model to a horizontal one. With multiple untrusted entities involved in the design process, and the rich connectivity features of the modern day computing systems, the critical hardware resources and intellectual property (IP) are left exposed to attackers who in some cases can attack such resources remotely. In addition, the modern complexity of chip designs with billions of transistors and interactions among hundreds of IPs, coupled with the lack of security-aware computer-aided design (CAD)/EDA tools and short time to market, can allow security weaknesses to be introduced or go unnoticed during design.

Hardware security threats can arise during various stages of the integrated circuit (IC) design cycle. They are generated from unintentional design flaws, system-based side effects, and intended malicious design modifications. With the advancement in AI and ML, hardware security threats such as physical attacks (invasive, semi-invasive, and non-invasive) and hardware Trojans are evolving as well [121, 133, 245]. However, the development of AI/ML-based models to defend IP and detect known and potentially unknown attacks has yet to catch up. Nevertheless, in the past few years, researchers in both academia and industry have turned to AI to not only speed up chip design but improve upon various figures of merit. To buttress the importance of pursuing a more secure EDA pipeline, we throw the spotlight on a recent article [78] from Jason Fung, CWE/CAPEC board member and Intel’s current Director of Offensive Security Research and Academic Research Engagement. It is an ideal reference material enumerating seven essentials for modern security-aware EDA across both academia and industry. We believe that our work is a guide to executing all requirements of the following essentials. Each point includes potential use cases of AI/ML, some of which are further discussed in later sections:

1. **Guide users to make design tradeoffs by taking both functionality and security into consideration.** Today’s EDA tools are primarily driven by traditional metrics, such as area, power, and delay. Security metrics are challenging because oftentimes security cannot be modeled analytically. AI/ML, however, can learn models from data and learn tradeoffs/policies through trial-and-error actions with an environment.

2. **Educate users on security best practices when design decisions are being made.** Most design engineers are either untrained in security or at best experts on one particular topic. Security-aware tools would ideally train and retrain engineers to keep up with new attacks and threats. Although AI/ML, especially deep learning (DL), is often considered as a black box, interest in explainable AI (XAI) [25] is growing and should help fulfill/support this directive.

3. **Detect security issues in real time when code is being written.** According to the rule-of-10 in VLSI [37], the cost of dealing with a fault, bug, or security issue grows by a factor of 10 after completing each step within a chip’s design and fabrication lifecycle. For example, finding and fixing a bug at the register transfer level (RTL) is 10 times less expensive than finding it after synthesis. At the extreme case, a bug found during the pre-silicon phase might be 1,000 times less expensive to fix than if the same bug were found within a chip of a fielded system, and so on. Thus, it is essential to find security weaknesses as early as possible. AI
has recently found success in the software domain for vulnerability detection [148] and fuzzing [89], among others. For digital IC design, many of these can be directly transferred to hardware weaknesses at the source code level or RTL. In the domain of analog ICs, there is already progress to speed up performance evaluation of circuits [188].

(4) **Beyond just finding problems, provide reliable mitigation options to address them.** It is not enough to just point out vulnerabilities. Engineers may need guidance on the available mitigation options and how they might impact the rest of the design. Once again, in the software domain, there is evidence that real-time recommendation and completion [237] are possible. At a minimum, it seems that AI can already provide reasonable **high-level synthesis (HLS)** [169], **place-and-route (P&R)** [271], physical implementation [67], and predictions for digital and analog circuits in terms of traditional metrics and, in rare cases, security metrics (e.g., SAT attack time [49]). It may only be a matter of time before AI-based optimizers, especially **reinforcement learning (RL)**, can automatically insert solutions and countermeasures to meet an objective and constraints.

(5) ** Seamlessly integrate best-in-class protections.** Aside from tradeoffs with traditional design metrics, metrics for certain hardware attacks and vulnerabilities may be at odds. For example, in the area of logic locking, the community has often mentioned an unavoidable tradeoff between resistance to SAT attacks and corruptibility [158, 273]. In such situations, a combination of methods or protections may be the best approach. In the area of AI-based digital circuit design, “decision-making” tools have been developed that select the right combination of algorithms and tools [184, 280] for a given IP to achieve optimal **quality of result (QoR).**

(6) **Recommend the most efficient test strategy for a given coverage guarantee.** Not all security properties can be verified statically. In such cases, hardware simulation, emulation, or formal verification can be used. AI-based prediction and classification can be used to predict performance and avoid simulations entirely or narrow the simulation space down. Further, “decision-making” tools can guide the development team’s choice of what tests to run and what parameters should be used for a specific IP.

(7) **Learn continuously from users.** The continuous evolution of attacks and new threats implies the need for moving target defenses. Similarly, EDA itself needs to keep up with new challenges facing the industry, such as the end of Moore’s law and 3D integration. Advancement in AI, especially DL and **federated learning (FL)** [175], is coming at the perfect time to promote continuous learning by crowdsourcing EDA problems and solutions while still maintaining privacy of user inputs and IPs.

Several works are available that address various topics also covered in this text. For example, the focus of Azar et al. [19] is a detailed overview of **system-on-chip (SoC)** security validation using automation techniques including AI/ML, fuzz testing, and penetration testing. In this survey, we summarize both constructive and destructive use of AI/ML techniques in the security-aware design of ICs. In other words, we review the recent works in design/attack of security approaches at every level of the IC design flow and the design/attack of hardware-based security primitives using AI/ML-based approaches. As such, this survey is organized as follows. Section 2 provides a brief background on ML, AI, and DL. Section 3 reviews the studies that utilize AI/ML for general and security-aware design of digital ICs. Section 4 reviews the AI/ML and optimization techniques involved in the design of analog ICs, analog security primitives, and attacks on analog ICs and security primitives. Section 5 discusses the outstanding needs and requirements for a security-aware design of ICs. Finally, Section 6 concludes the survey by highlighting the future trends and opportunities in the field of security-aware IC design.
2 BACKGROUND

2.1 Machine Learning and Artificial Intelligence

AI is a general term for any machine and/or program that displays some level of intelligence. ML is a sub-field of AI concerned with algorithms that are capable of learning patterns from data without explicitly being told those patterns by a human. Over the years, the availability of large amounts of data and computational resources has led to a rise in the use of ML in a variety of fields. DL is a sub-field of ML that involves the use of artificial neural networks (ANNs), which are organized algorithmic structures that mimic how humans learn as shown in Figure 1(b). In recent years, DL has been favored over traditional ML techniques for highly complex tasks with large amounts of complex data.

2.1.1 Types of ML. There are three main types of ML algorithms: supervised learning, unsupervised learning, and RL. An overview of these three main types is provided in the following paragraphs, and example methods are summarized in Figure 1(a).

Supervised learning is a form of task-driven ML that maps inputs to an output, given labeled training examples. Supervised ML is often used for classification and regression tasks. Classification tasks involve mapping inputs to a discrete value (i.e., class label), whereas regression tasks involve mapping inputs to a continuous value. Note that regression is the general form of classification, since all classification tasks can be conceptualized as predicting the likelihood (which is a continuous value) that an input belongs to each class and returning the class with the highest likelihood. Popular supervised ML methods include support vector machines (SVMs) and random forest (RF) for classification tasks, and linear and logistic regression for regression tasks [12].

Unsupervised learning is a form of data-driven ML that finds patterns in input data, without the need for labeled training examples. Unsupervised ML is often used for clustering and dimensionality reduction tasks. Clustering tasks involve grouping data based on similar underlying structures, whereas dimensionality reduction tasks involve simplifying data to its most principle (i.e., salient) underlying structures. Common unsupervised ML methods include $k$-means and $k$-nearest neighbors for clustering, and principal component analysis (PCA) and singular value decomposition for dimensionality reduction [12].
RL is a form of feedback-based ML that involves learning from mistakes in a trial-and-error fashion. RL is often used for prediction and control in problem domains where time and event sequences matter, feedback may be delayed, and actions have consequences. In RL, prediction involves predicting the performance of some policy, whereas control involves determining the optimal policy that yields the best performance. Although practical applications are mostly concerned with control, the problem of prediction must oftentimes be solved first. Popular RL methods include Monte Carlo and temporal difference learning for prediction, and SARSA and Q-learning for control [12].

Another noteworthy method of ML gaining popularity is semi-supervised learning, which uses principles of both supervised and unsupervised learning. It can solve classification problems by training on both labeled and unlabeled data. It is extremely useful when labeled data is scarce [296]. Note that there are other, less mainstream types of ML such as self-supervised learning, multiple instance learning, inductive learning, deductive learning, transductive learning, multi-task learning, and active learning. In addition, there are other ML tasks including generative modeling and association rule learning.

2.1.2 ML Pipeline. Regardless of which type of ML model is used for security-aware EDA, it is important to carefully plan the ML pipeline. The pipeline provides opportunities for AI/ML practitioners to support hardware designers by combining the domain knowledge of both fields. The next sections enumerate various intersections between AI/ML and security-aware EDA, but they cannot be exploited without following these steps. The generalized ML pipeline is described in the following paragraphs and summarized in Figure 2.

The first step of the ML pipeline, problem definition, involves thoroughly understanding the problem to be solved. This involves determining what the end goal is in terms of desired model outputs, what inputs might be needed for a model to yield such desired outputs, and what existing techniques have already been applied to similar problems and their assumptions, benefits, and limitations. In other words, problem definition involves gaining enough domain knowledge to make informed decisions for the remaining steps in the ML pipeline. It requires communication from the hardware designers who require solutions. It is imperative that this is done as precisely as possible due to the high cost of obtaining data, especially in the EDA industry.

During data collection, information relevant to the problem is gathered. Data can be collected historically and/or in an online fashion, and includes organized and unorganized data structures such as text, images, videos, and audio clips. In supervised ML, human subject matter experts are often employed to label the data so ML systems have training examples. Unlike most AI/ML applications, EDA is hampered by data insufficiency and improper representation of the problem space. Data storage in the EDA industry must encompass useable formats, secure access without compromising privacy, and efficiency for use.

In the preprocessing stage, the collected data is cleaned and converted to a machine-readable format in preparation for feature extraction. Common preprocessing methods concern handling missing values (e.g., removing all datapoints with missing values from the study, replacing missing values with a zero), handling categorical data (e.g., creating dummy variables), and standardizing the data (e.g., normalizing values from 0 to 1). The data must be explainable to both models and users (AI/ML practitioner and hardware designer) for maximum utilization.

After preprocessing, the data is then transformed in the feature extraction stage. The goal of feature extraction is to ensure only the most salient information relevant to the problem will be used for training the ML model. In other words, this step helps ensure that no unnecessary features are used during training. At best, unnecessary features do not degrade ML model performance, at the cost of increasing the amount of data needed (as is characteristic of the curse of dimensionality). At
worst, unnecessary features can significantly degrade ML model performance (as is characteristic of irrelevant and/or highly correlated inputs). The various stages of the EDA flow provide different features that both the practitioner and designer must carefully select. Common feature extraction techniques include feature selection (e.g., linear discriminant analysis), dimensionality reduction (e.g., PCA), and computer vision techniques for input images (e.g., color, shape, and texture feature extraction methods).

During training and validation, the extracted features are used to train the ML model. The type of ML model(s) to use will depend on a variety of factors, such as the nature and amount of input data, format of the desired output, and the given problem’s associated ML task. Note that in DL, feature extraction and training can occur simultaneously. Ideally, the type of ML model(s) to use were considered at the problem definition stage, but sometimes it is accomplished by trial and error.

After the ML model is trained and its performance is validated, the testing and verification stage ensures the model is ready for deployment. Testing involves evaluating the trained model on unseen data and validation typically involves humans ensuring the model is performing up to standards. Validation data is different from testing data in that validation data is used to evaluate the model during the training process, whereas testing data is completely unseen throughout the training process (i.e., testing data is a separate holdout set). Separate training, validation, and testing data ensures the model is not overtraining (i.e., memorizing rather than actually learning). The testing process for security-aware EDA must be executed in an environment as close to the proposed deployment environment as possible.

After the ML model achieves desired performance on testing data and has been verified, the model is ready for deployment in the field. Depending on the nature of the problem, the ML model may require updates. If so, it may be necessary to periodically monitor performance changes over time, collect additional data, and refine or retrain the model. Thorough security involves dealing with developing threats and requires extensive collaboration between model and hardware designers.

2.1.3 Deployment and Tools. The popularity of Python for data science applications helped drive the development of AI, ML, and DL frameworks coded in Python. Python packages such as Scikit-Learn [196], TensorFlow [2], and PyTorch [194] make AI accessible and have hence garnered the support of a large community of developers and researchers over the years. These tools have become widely used for experimentation, evaluation, and deployment with the help of application program interfaces. Advances in hardware and software such as parallel processing, GPUs, and cloud computing help optimize computing resources to be more suitable for training large, complex AI models. Moreover, data is becoming more available than ever for training and testing ML models.
A Survey and Perspective on AI for Security-Aware EDA

2.2 Deep Learning

DL models have become a hot topic again in the past decade because of the availability of a huge amount of data and deserve a short description here. They are made up of multiple processing layers that learn representations of training data with multiple levels of abstraction, and are used for speech recognition, object visualization, and detection tasks, among others. DL has helped address complex problems that have persisted in various industries for many years [137]. The core of DL is the use of neural networks (NNs), as seen in Figure 1(b), which consist of an input layer, one or more hidden layers, and an output layer. Most deep neural networks (DNNs) flow in one direction only from input to output. However, backpropagation is used to change internal parameters or weights that are used to compute the representation between a current and previous layer. And it is very efficient for computing gradients in deep networks [73]. Some examples of DL models include convolutional neural networks (CNNs), graph neural networks (GNNs), and graph convolutional networks (GCNs).

2.2.1 Convolutional Neural Networks. CNNs, like most NNs, are made up of self-optimizing neurons. The raw input made up of data in a grid pattern produces a class score using adjustment functions, known as weights, throughout the network. It is typically composed of convolution, pooling, and fully connected layers. The first two, for convolution and pooling, execute feature extraction. The fully connected layer maps the extracted features into final output. The loss functions of the final layer perform classification at the output. Thus, CNNs differ from other NNs because they encode image-specific features and use the patterns identified to tune the model [186].

2.2.2 Geometric Deep Learning. Perhaps most relevant to EDA applications is geometric deep learning (GDL), which provides a blueprint for generalizing DL to non-Euclidean data (e.g., circuits) [35]. The success of DL approaches is owed largely to their ability to capture local statistics of the input data. For example, CNNs have been widely useful in computer vision tasks due to the shift invariant properties of the convolution operator. Traditional formulations of DL models (CNNs, recurrent neural networks (RNNs), etc.) rely on Euclidean structures in the data (grid structures), such as image, video, and speech signals. Figure 4 shows examples of Euclidean (grid) and non-Euclidean (graph) data. The geometric prior on grid data is the ordering of the nodes, which is the structure that RNNs and CNNs implicitly take advantage of. Graph data, however, requires no explicit ordering on the nodes and operations on the graph are permutation invariant.
Yet graphs have permutation invariant structure in that the nodes are not assumed to be in any specific ordering.

GNNs and GCNs are examples of GDL models that can learn directly from graph data (this category of approaches is also referred to as graph representation learning and is a subset of GDL) [97]. These models are able to leverage graph structure as well as node and/or edge features to learn a useful representations of data. GCNs possess the same shift invariance power of traditional CNNs [272].

Recent work by Mirhoseini et al. [178] demonstrates the power of combining graph representation learning techniques with RL training algorithms to improve placement in chip layout. The Edge-GNN in the work of Mirhoseini et al. [178] was first trained to create graph embeddings that predict reward labels (in this case a reward derived from wire length, congestion, and density metrics). Then the Edge-GNN is used as an “encoder” for training the CNN-based policy networks in the RL training algorithm. Figure 3 shows the general structure of GNN layers and demonstrates how the embedded graph vectors can be passed to various downstream tasks. The ability to capture relationship and interaction statistics in the circuit data using graph embeddings enabled the policy network to reduce placement costs.

2.3 Electronic Design Automation

The general EDA flow is as follows.

2.3.1 Design Specification. In design specification, the designer must accurately describe the overall design requirements. The system may be proposed by a design team to initiate the production of a chip. The IC designers decide on functionality and plan out verification and testing procedures for the entire process.

2.3.2 High-Level Synthesis. HLS tools translate a design written in high-level languages such as C/C++/SystemC into a low-level hardware description language. Hardware components can be modeled at high levels of abstraction, allowing the designer to map both hardware and software components [56].

2.3.3 Logic Synthesis. Logic synthesis is a direct translation from the behavioral domain (RTL) to the structural domain (gate level) [119]. The gate-level netlist is mapped to the standard cell library. The optimization part of logic synthesis minimizes hardware by finding equivalent
representations of larger blocks. Design constraints used as input may also be met for circuit area, power, and performance.

2.3.4 Design for Testability. **Design for testability (DFT)** encompasses the techniques used to generate cost-effective tests for the gate-level netlist obtained from logic synthesis. These techniques are geared toward increasing observability, controllability, and predictability of the design [172]. Ad hoc methods like partitioning and test point insertion are relatively easier to implement, whereas structured ones like scan registers, scan chains, scan architectures, and algorithms ensure good testability at the expense of additional area and delay overhead. The resulting tests utilize test programs that drive automatic test equipment. The automatic test equipment also uses **automatic test pattern generation (ATPG)** to identify input sequences that trigger errant circuit behavior arising from manufacturing defects [106].

2.3.5 Floorplanning. Floorplanning focuses on the sizes and arrangement of the physical blocks created during logic synthesis. It affects the optimization results of the increasing physical stages. It is the first major step in physical design. Pins and ports are also assigned a rough location, which can further be refined depending on the placement and routing results [151].

2.3.6 Placement and Routing. After a successfully proposed floorplan, P&R addresses the structural design of a circuit. The designer places and connects all of the blocks that make up the chip such that they meet design criteria and constraints. After the initial P&R attempts, the design’s timing constraints are analyzed. If unsatisfactory, the P&R software in use tries different placements and signal routing to try to meet the designated constraints [151].

3 SECURITY-AWARE DESIGN OF DIGITAL ICS

ML is already applied to some extent in the digital IC design process, albeit with primary focus on general design prediction and optimization. Some needs tackled at this stage include logic and design optimization [95], low-power approximation [192], timing prediction [169, 268], and area estimation [77]. Careful assessment of available publications incorporating learning into digital IC design will reveal an absolute truth; very little work has been done to directly address hardware security vulnerabilities. The use of intelligent models presents the opportunity to not only optimize designs but also to secure them against the array of tools and attacks that malicious parties have at their disposal. This is especially important for some security properties that cannot be modeled analytically and situations where multiple security constraints are at odds. According to Huang et al. [108], ML approaches in EDA can be broken down into four main directions: decision making, performance prediction, black box optimization or design space exploration, and AI-assisted EDA. In the rest of this section, we follow this same organization to discuss security-aware CAD research and opportunities. Figure 5 also highlights the general EDA steps and the applicable directions for each one.
3.1 Decision Making

The decision-making perspective encapsulates the replacement of traditional, brute-force design-for-security methods with more automated and efficient techniques. In most cases, brute-force techniques involve countless trial-and-error steps until the best-performing configuration is found and used on a design. From a heuristic perspective, the knowledge gained may prove to be invaluable. However, they are only feasible on simpler designs; increased complexity transforms them into cumbersome requirements that most designers would gladly bypass. Further, the trade-offs between security and traditional metrics as well as between different security metrics might be unknown or too complex for manual tuning. Automation becomes valuable only when it is characterized by efficiency. ML can definitively make decisions on the most suitable settings and parameters for countermeasures with varying levels of human input (Figure 6).

3.1.1 High-Level Synthesis and/or Register Transfer Level.

Encoding optimization. Another aspect that stands to benefit from the addition of ML-powered decision making is finite state machine (FSM) encoding optimization. The encoding schemes are selected based on design constraints, including power and area. The two most common options are the following:

- **Binary encoding**: In the binary encoding scheme, states are encoded as a binary sequence where the states are numbered starting from 0 and up. The number of state flip-flops (FFs), \( q \), required for binary encoding scheme is given by \( q = \log_2(n) \), where, \( n \) is the number of states. The binary encoding scheme is better suited for FSM with a fewer number of states [152].

- **One-hot encoding**: This encoding scheme is designed with only one bit of the state variable as “1,” whereas all other state bits are “0.” It requires as many state FFs as the number of states. This creates the need for more state FFs than binary encoding [39].

The one-hot encoding scheme is less vulnerable to fault injection attacks, whereas binary is more resistant to hardware Trojans that exploit don’t care states. This is demonstrated by Nahiyen et al. [181] using the FSM of the SHA-256 digest engine. With this knowledge, a secure encoding scheme was proposed by Nahiyen et al. [181] that combines binary and one-hot schemes to achieve the best of both worlds. In future work, AI/ML may be used to determine the best mix given a specific FSM.

**Hardware security primitive deployment at higher levels of abstraction.** The Automatic Implementation of Secure Silicon (AIISS) program was developed by DARPA (the Defense Advanced Research Projects Agency) to automate the process of incorporating scalable defense mechanisms into chip designs, by allowing designers to explore chip economics versus security tradeoffs based on the expected application and intent while maximizing designer productivity [139]. Deployment of security methods pre-silicon are always cost effective and less time consuming. With this in mind, AI/ML can be used to make decisions as early as during HLS, or at RTL. Based on the discernible features at these levels of abstraction, a classification-based model can use vector embeddings to
suggest suitable hardware security primitives and their associated parameters (e.g., size). For example, silicon odometers are inserted into IC designs to measure aging and detect recycled counterfeit chips [91]. Their accuracy and yield are determined by various parameters [224], which can be optimized through AI/ML.

Physically unclonable functions (PUFs) [82] provide digital fingerprints using the internal process variations (entropy) of a physical device. An example is the arbiter PUF circuit shown in Figure 7. The translation of these unique and unclonable manufacturing variations into challenge-response pairs provides unique chip identifiers or authentication mechanisms. One of the main issues with PUFs is their reliability—that is, the ability to provide the same output in the presence of environmental variations and aging. To combat this, they often rely on error correcting codes [105], which can be designed to handle a specific number of bit flips. Another primitive is the true random number generator, which uses an entropy source to generate non-deterministic data with a given throughput to seed security algorithms like cipher keys [79] or masking [247]. For any design that contains all three of these primitives, their characteristics can be tuned together for a specific application or to fit within a dedicated silicon area.

3.1.2 Logic Synthesis.

Tuning EDA parameters and commands during logic synthesis. Although a constraint set may be part of the design specification, the gate-level netlist provides a better understanding of functionality to a designer. Area constraints guide the P&R tool to locate a specified design block partition, whereas timing constraints specify path delays [55]. To tune high-level directives, it is important to accurately predict their impact. This is a tall order for most designs due to complex optimizations throughout the design process. These complex optimizations create disparity between desired results at the HLS stage and implemented values post-synthesis. Conventional tools assist with optimization tasks, but ML is already being used to mitigate the latter problem. For example, Yu et al. [280] have developed IP-specific synthesis flows (i.e., sequence of synthesis transformations for TCL scripts) using CNNs that improve QoR. In the work of Neto et al. [184], DL is used to automatically decide which logic optimizer (And-Inverter Graph and Majority-Inverter Graph) should handle different portions of the circuit for better performance and lower area. Makrani et al. [169] proposed a Pyramid framework to estimate best performance and resource usage. The input features are derived from the HLS report, and a stacked regression model provides accurate timing, delay, and resource values before reaching post-implementation.

Optimization goals during tuning can be geared toward obtaining a more secure, synthesized design with minimum overhead. Although this would only be evident with the combination of other design parts, early-stage deployment saves time and labor. For example, secure split-test is
Table 1. Security Requirements under Decision Making with Applicable AI/ML Algorithms

| Design Stage       | Security Task                                           | Applicable AI/ML Algorithms                      |
|--------------------|---------------------------------------------------------|--------------------------------------------------|
| High-Level Synthesis | Encoding Optimization                                    | Polynomial Regression                             |
|                    | Hardware Security Primitive Deployment at Higher Levels of Abstraction | Polynomial Regression, SVM                       |
| Logic Synthesis    | Tuning EDA Parameters and Commands During Logic Synthesis | CNN [280], Stacked Regression [169]              |
| Cross-Abstraction  | Standard Cell Selection                                  | SVM                                              |
|                    | Benchmark Selection for Security-Aware EDA Tool Evaluation | GNN, GCN                                         |

The cited options indicate optimization or security implementations available for reference.

a method of securing the manufacturing process by mandating test results to be verified by the IP owner and by using a "key" to unlock the IPs' correct functionality after tests are passed. For the functional locking block, XOR logic is added in series to non-critical paths. If the two inputs are different, the XOR logic will act as an inverter [59] causing any locked (still untested or failed chip) to act deliberately incorrect. The optimal number of XOR gates to insert into the circuit, insertion algorithm [42, 138, 206], or partitioning algorithm [9] to employ for a given IP’s function and/or structure can be determined using ML techniques.

**Standard cell selection.** A specific category of available standard cells may be used in an IC design to address specific security vulnerabilities. As far back as 2004, sleep transistor cells were proposed as a method for sub-threshold leakage current reduction [20]. The sleep transistor cells are picked from a library designed to target high layout efficiency. The results were shown to have achieved a minimum reduction percentage of 74%. A trained SVM can be used to decide from a set of available libraries with specific target optimizations.

**3.1.3 Cross-Abstraction.**

**Benchmark selection for security-aware EDA tool evaluation.** One additional optimization activity that may easily be overlooked is the evaluation of EDA tools used during the IC design process. Companies and research groups that develop EDA tools constantly update features to enhance their output. To properly target specific problem areas, the testing process must involve specific benchmarks. For example, if a designer intends to assess the scalability of the tool, the most important requirement for the test benchmark would be its size. If more nuanced conditions must be met, an automated method would make this process faster and more efficient. Succinct features of a benchmark and a tool's problem area in a DNN can determine the most suitable sample for testing.

In the area of hardware security, benchmarking has played a critical role in development and comparison of hardware Trojan detection schemes [225] and recently in de-obfuscation [15, 16, 240]. Thus far, however, none of these benchmarking activities have explicitly incorporated AL/ML. Table 1 provides suggested AI/ML algorithms for future endeavors.

**3.2 Performance Prediction**

Performance prediction describes forecasting and modeling tradeoffs associated with adding countermeasures, especially at earlier design stages. Although an ideal scenario would involve achieving optimum design goals while guaranteeing near-perfect security awareness, a designer must be aware of the inevitable compromises that a secure design may entail. A more achievable target is finding the balance between optimization and security, as seen in Figure 8. This is where AI/ML comes into the picture. The automation of the balance-seeking process will not only speed up the IC design pipeline but will also ensure that the most suitable operating parameters and

ACM Transactions on Design Automation of Electronic Systems, Vol. 28, No. 2, Article 16. Pub. date: March 2023.
modifications are available to the designer. From a business standpoint, time to market of ICs in production may also decrease.

3.2.1 Physical Design.

**Security-aware layouts and tradeoff modeling.** Invasive physical attacks are expensive to execute but difficult to protect against. Attackers resort to focused ion beam (FIB) to extract an asset’s value by milling to its location in the IC layout, creating a metal contact to it, and probing the contact while the chip is in operation. There are two main sets of countermeasures proposed to combat probing attacks: the preventive strategy utilizes active or analog shields, such as meshes, whereas the detection strategy checks for attacks by sensing any probing or editing and alerting the operators [255]. To improve the effectiveness of active shields, an automated anti-FIB probing flow called iPROBE was proposed [80, 256] (Figure 9). iPROBE uses ad hoc rules to determine the areas and metal layers where CAD tools should place shields to reduce exposed area (EA). For a physical IC, the EA metric (as described in the work of Shi et al. [228]) is used to measure the design’s vulnerability to probing attacks. A larger EA means more flexibility with the expense that an attacker can probe without triggering contingencies. Although iPROBE did improve EA while reducing overhead as compared to traditional shields, the security and overheads cannot yet be explicitly controlled by the designer. In other words, trial and error needs to be performed to make sure that constraints are met. To further boost efficacy of the anti-probing method described earlier, it may be possible to model the relationship between EA and power, timing, and area with a multiple linear regression model or even DL. Then, iPROBE parameters could be chosen with security, area, power, and so forth, in mind.

3.2.2 Cross-Abstraction.

**Modeling area, power, timing, and security impacts of IP protection.** In general, design optimization problems have always been modeled based on area, power, and timing; timing is used here because it directly relates to performance. Even at the HLS stage, ML implementations, like Pyramid [169], have been used to predict optimal timing. There has also been work to predict area at both HLS [286] and logic synthesis [77]. Deep-PowerX is a DNN-based dynamic power consumption minimization tool that exploits the power-area and delay-area relationships within a netlist [192]. Even at the placement and routing stage, timing prediction is possible using ML [24]. Optimization tasks can be modified to meet security needs without deviating from the original goals. For example, IP protection is meant to counteract one of the most significant threats to design integrity—IP piracy. The availability of a design to malicious parties gives way to overuse, modification, cloning, overproduction, and/or reverse engineering. There are various defense-centered modifications available to an engineer at various stages of the IC design cycle, and ideas from ML-based optimization can be used to assess their effects on desired area, power, and timing configurations. Some of these modifications are IP watermarking and hardware obfuscation.
Fig. 9. iPROBE version 2 with protection for frontside and backside probing attacks [80]. The light blue metal lines and darker blue metal lines form active shields that protect against frontside attacks (through top passivation and metal) and backside attacks (silicon substrate), respectively. The metal lines sandwiched between the shields carry critical information that the attacker wants to probe. An FIB cut though an entire shield line of frontside/backside will be detected because the signal present on it will not match its counterpart in backside/frontside.

**IP watermarking.** A watermark is a specific modification of an IP core that allows it to be uniquely identifiable, which is useful for piracy detection. However, IP core watermarking in general must never alter the functionality of the design [44]. One popular method of watermarking is the don’t-care condition based technique. It involves adding function blocks with unspecified input combinations to the original design. Their outputs can be forced and used to verify the authenticity of a circuit [72]. However, additional logic may mean area, timing, and power overhead. To hasten the design cycle, these overhead metrics must be readily available to a designer. If a trained algorithm can accurately model and predict these values, the design house would be able to ascertain the viability of a specific watermarking scheme, like the don’t-care condition based method.

**Hardware obfuscation.** Hardware obfuscation is used to actively protect IP and has been applied at all major design stages preceding fabrication and assembly. It is intended to obscure an original design to prevent IP piracy and reverse engineering. Hardware obfuscation also addresses IP overuse and hardware Trojan insertion. The set of approaches that can be implemented until the DFT stage are typically keyed approaches. These techniques attempt to prevent black box use by key gates/inputs. One common example is logic locking, which hides the functionality and the implementation of a design by inserting additional gates ("key gates") into the original netlist. The circuit will only function correctly if the acceptable inputs or keys are provided to the key gates [277]. The additional gates must provide low overhead and be usable for larger designs. This can be assessed using a predictive AI/ML algorithm measuring the usual metrics as stated earlier. For stand-alone logic locking, a significant challenge, however, has been making schemes secure against the entire suite of oracle-based attacks (e.g., SAT [233], AppSAT [227], key sensitization [205]) and oracle-less attacks (e.g., desynthesis [173], signal probability skew [276]). The former use an unlocked chip as an oracle to non-invasively derive its key, whereas the latter operate solely on the netlist. Preventing oracle attacks implies that the time to recover the key should be prohibitively high for an attacker. Recently, ML has been used to predict the obfuscation strength in terms of the predicted time taken to de-obfuscate an obfuscated circuit using the SAT attack.
Chen et al. [49] demonstrate this using a GCN. They combine graph structure with gate feature by using an enhanced graph convolutional operator named ICNet. The features employed are divided into the graph structure, which describes connections, and gate features, including gate mask and gate type. Although this approach has only been applied to predict SAT attack time, it can nonetheless be used to predict resistance to other oracle attacks. Recently, oracle-less attacks such as SAIL [41] have employed ML to recover the original (unobfuscated) netlist by reverse engineering logic synthesis rules.

Another key-based countermeasure that can be considered is FSM locking [42]. FSM locking adds extra states into the FSM of an IC design. The correct “key” is the right sequence of state transitions, which guarantees non-erroneous functionality. The additional states are materialized by FFs with their corresponding combinational logic. Active hardware metering [11], a version of FSM locking, creates boosted FSMs from the new states. At this stage, it would be imperative to be able to predict the overhead created by the added states. This is because the design house sends the verified netlist to the untrusted foundry to create PUFs (challenge-response pairs) from the fabrication process variation. This may introduce additional overhead that could affect overall functionality. Depending on the complexity of the circuit, either a regression model or a DNN may suffice.

The keyless variety of obfuscation does not require keys and cannot affect functionality. The desire is to conceal design intent. Without some form of obfuscation, a malicious party can either copy an IP or seek and exploit design vulnerabilities using reverse engineering. The most noteworthy example of keyless obfuscation is IC camouflaging [51], which replaces original gates with “camo gates” that are difficult to discern by pattern recognition. It is worth noting, however, that most camouflaging techniques can be “mapped” into logic locked circuits [278] where the preceding oracle attacks are quite effective [74]. Hence, the prediction schemes mentioned earlier for logic locking may also apply to camouflaging. Further, the replacement of gates with camo gates to facilitate camouflaging will almost always alter power consumption and area. With the right set of features extracted from a report (HLS report), a trained regression model could predict the parameter values with near-perfect accuracy. There is evidence of this in other EDA applications. For example, Zennaro et al. [286] combine an RTL generation framework with ML algorithms to estimate the area of the final design based on the features of an abstract specification. They retrieve the number of configurable logic blocks information from synthesized RTL design reports created from an automation framework. They mainly use a multilayer perceptron (MLP) but also experiment with RFs and gradient boosting (GB) [286].

Another popular keyless approach is split manufacturing [113], where a design is split, each part is fabricated at one or more untrusted entities, and a trusted entity puts them together. Split manufacturing can have significant overheads and security concerns (e.g., proximity attacks [168]) if P&R is performed poorly. Ad hoc and linear programming (LP) approaches to perturb P&R [261] and/or split designs [229] have met with some success but can likely be improved further through the incorporation of AI-based modeling and prediction.

Side-channel attack resistance. Side-channel leakage allows an attacker to break cryptographic systems. Signals that a cipher’s implementation inadvertently emits allow for systematic extraction of underlying information. Examples include instantaneous power consumption, timing/delay, and electromagnetic emissions. Whether the attacker targets the understanding of device operation (simple) or uses leakage information to correlate data values (differential), there are generic countermeasures to reduce the effect of side-channel leakage [171]. A high signal-to-noise ratio (SNR) implies the availability of more meaningful leakage information. Hiding countermeasures reduce the SNR by either dampening the signal with low power designing and shielding,
or flooding the leak-prone areas with noise using noise generators [142]. To measure the value of hiding on a design, a predictive, regression-based model could provide an accurate percentage reduction in side-channel leakage. An obvious feature would be the tuning of the technique used.

Another available countermeasure is **masking**, which seeks to remove the correlation between input data and side-channel leakage [202]. Unlike hiding, masking is applied at the algorithmic level with logic gates. Nonetheless, higher-order side-channel analysis allows an attacker to bypass the routine masking schemes. A higher-order masking may be employed, but it may require significant overhead [203]. To evaluate the effectiveness of masking, various types of AI and ML algorithms have been employed to accomplish (1) the assessment of side-channel resiliency against a specific attack [200] and (2) the full leakage assessment methodology [179]. However, both of these evaluation techniques need the actual ASIC or a correctly programmed FPGA, as well as special equipment to be performed (cf. [18]). To overcome these obstacles, another line of research has been pursued, which is devoted to (1) theoretical conditions for a design to be SCA-resistant [26, 32, 61] or (2) model the implementation for simulating its behavior [28, 208] in the pre-silicon steps. In the first category, the AMASIVE framework [112, 297] can be mentioned that identifies hypothesis functions for leakage models (cf. [36]). An example from the second class is VerMI, which is a verification tool in the form of a logic simulator that checks the properties of a class of masking methods (threshold implementation) [18] at both algorithmic and implementation levels. Nevertheless, at this level of abstraction (i.e., pre-silicon), AI techniques have not found direct applications yet. Perhaps the most straightforward way of incorporating such a technique can be imagined to examine whether the conditions for SCA resiliency are fulfilled (the first category).

Yet another step further, Ma et al. [167] presented a security-driven placement and routing tool to protect designs against EM side-channel attacks [167] that attempts to break the balance of signal delays by register reallocation under the condition of layout constraints. A CAD-based tool, named **CAD4EM-P**, uses register reallocation and wire length adjustments to reduce the data dependency of EM leakage with acceptable area and power overheads [167]. Opportunities to improve the effectiveness and efficiency of this approach can rely on more advanced forms of ML for prediction. For example, a GNN can replace the graph-based algorithms that are the basis of the original version.

**Fault injection tolerance.** In contrast to most SCA attacks, fault injection attacks involve an active adversary. In other words, the adversary tries to observe a faulty behavior of the target device by forcing it to function outside of its specified operating range or feeding it undefined data. For example, an attacker can cause erroneous operation of the target platform by tampering with the supply voltage (a.k.a. voltage glitching), modifying the clock signal’s frequency (a.k.a. glitching), or flipping bits in the memory using a laser beam [23]. Although most fault attacks require physical access to the victim device, recent studies have shown that in certain cases similar fault attacks can also be carried out remotely on a variety of systems [8]. Cryptographic devices and secure hardware have been the main targets of fault injection attacks. For example, an adversary could inject faults into an FSM implemented on a hardware platform to bypass authentication states and obtain unauthorized access to security-sensitive states. However, an adversary may be able to extract the secret key by injecting faults into a cryptographic implementation and applying mathematical tools, like differential fault analysis, on faulty generated ciphertexts.

Several protection/detection-based countermeasures have been proposed to mitigate the vulnerabilities of circuits against fault attacks. Although device-level countermeasures can be effective against fault injection attacks, the cost and extra manufacturing steps make the algorithmic and circuit-based countermeasures more attractive. EDA tools can be deployed to improve the circuits’ resiliency for such countermeasures. However, conventional countermeasures are generic and
Table 2. Security Requirements under Performance Prediction with Applicable AI/ML Algorithms

| Design Stage     | Security Task                                      | Applicable AI/ML Algorithms                |
|------------------|----------------------------------------------------|-------------------------------------------|
| Physical Design  | Security-Aware Layouts and Tradeoff Modeling       | Multiple Linear Regression                |
|                  | Modeling Area, Power, Timing, and Security Impacts of IP Protection | DNN [192], GCN [49], MLP [286]           |
|                  | Side-Channel Attack Resistance                     | Polynomial Regression, GNN                 |
|                  | Fault Injection Tolerance                          | GNN, SVM                                  |
|                  | Hardware Trojan Detection Rates                    | SVM, Polynomial Regression                 |
|                  | Vulnerabilities across Design                      | GNN, RL [163]                             |
|                  | Abstractions and/or Process Design Kits            |                                          |

The cited options indicate optimization or security implementations available for reference.

create high overhead in terms of area and power. Several protection/detection-based countermeasures have been proposed to mitigate the vulnerabilities of circuits against laser fault injection attacks. Although physical countermeasures, such as tamper-proof packaging and light sensors, can be effective, the cost and extra manufacturing steps make the algorithmic and circuit-based countermeasures more attractive. For such countermeasures, EDA tools can be deployed to improve the circuits’ resiliency. However, conventional countermeasures are generic and not tailored to specific fault injection techniques. For instance, by using triple-modular redundancy [166], error-detection/correction codes [123, 185, 236, 246], and MAC tags/infective computation [66, 209], the circuit becomes more resilient in general. In these cases, however, depending on the capabilities of the adversary and how these countermeasures are synthesized, placed, and routed, they can still be bypassed by powerful fault attacks. AI/ML can support creating circuit netlists and layouts during the design phase that are more resistant to fault injection attacks by taking the physical models of fault attacks into account. For instance, by considering fault propagation together as a new feature, the impact of fault resilient placement and routing on security and overhead can be predicted. As shown in Table 2, GNNs and SVMs are viable algorithms for use.

Hardware Trojan detection rates. Malicious modifications such as hardware Trojans, are possible during the IC design and fabrication process. Hardware Trojan detection has been extensively researched within the hardware security research domain [242]. Salmani et al. [217] proposed a method of increasing the probability of Trojan activation using dummy scan FFs. They place a dummy scan FF with a net having low transition probability. To test the concept, Trojan samples have to be deployed on benchmarks. The rate of Trojan detection could be derived from the available data that these simulations produce. Likely features that would be valuable for a prediction-based ML model include nets with dummy scan FFs, their fanouts, and their corresponding transition probabilities.

Assertions are typically used for formal verification of specification patterns. The behavior of circuits determines the correctness of the design. Alsaiai and Gebali [13] propose RACs (reconfigurable assertion checkers), which are able to detect hardware Trojan updates on SoCs. The design flow can be seen in Figure 10. Even with traditional assertion checkers where selection only occurs pre-synthesis, it is possible to ascertain the rate of Trojan detection using the assertion checkers, the Trojan type, as well as the point(s) of insertion.

Built-in self-authentication (BISA) relies on the incorporation of functional filler cells into white spaces at the layout level to form BIST (built-in self-test) circuitry [270]. The latter is designed to verify that no BISA cell is tampered with by an untrusted foundry. The possible failure of the BIST circuitry allows inserted Trojans to be detected. To reduce the risk of
compromising BISA design during manufacturing, *split manufacturing* can also be applied. On its own, split manufacturing cannot be used to detect Trojans, but the technique known as OBISA (obfuscated BISA) \[229\] combines both BISA and split manufacturing. OBISA’s ability to detect hardware Trojans can be predicted by training an ML model.

**Vulnerabilities across design abstractions and/or process design kits.** There is evidence that designs become more prone to certain security vulnerabilities as they move across different levels of abstraction. One example provided by Jiang et al. \[120\] presented a timing side-channel vulnerability introduced during HLS to produce an optimized RTL representation. Another pointed out fault-injection vulnerabilities after logic synthesis due to FSM encoding styles and newly generated don’t-care states \[181\]. It is important to have foreknowledge of these potential risks as they develop during the EDA process. This is possible with predictive algorithms. In one instance, the data flow graph representation of the RTL could be combined with features from the HLS report to produce a GNN capable of identifying less-secure design areas. This may also apply to porting designs across different **process design kits (PDKs)**. The available gate sizes are discrete values that are usually specific to the underlying technology. Process variations may introduce parametric alterations that could make a device more susceptible to malicious parties. For this scenario, PDK electrical and design rules are possible input features for the same GNN described earlier. As the solution space scales exponentially with respect to the size of the netlist, gate sizing algorithms integrated into EDA tools rely on either heuristics or analytical methods, which leads to sub-optimal sizing solutions. To combat this shortcoming, Lu et al. \[163\] have demonstrated the feasibility of applying RL algorithms equipped with GNNs that encode design and technology features. Specifically, the problem of gate sizing for timing optimization at the post-route stage has been the main focus of the study. Although the proposed sizer adopts a more global optimization approach, it does not always outperform the commercial tool. Nevertheless, it has the great advantage that is automatic gate sizing for timing optimization without any human intervention.
3.3 Black Box Optimization or Design Space Exploration

For design space exploration, AI/ML seeks the solution that best meets requirements from available choices with little to no human intervention. The expanse of the search space creates the need for automation to execute selection, generation, and evaluation of the solutions. However, the exhaustive option may not always be the optimal one, regardless of the availability of automation techniques. Design space exploration employs the application of different methods: stochastic optimization methods like random search, evolutionary algorithms (EAs), and black box optimization \[38\]. Black box optimization uses a set of configurable parameters as inputs instead of results from the design stages, as seen in Figure 11. The circuit may either be too complex to model or the engineer lacks details of the design to work with. At the training stage, most AI/ML algorithms are being optimized to find the best fit for input parameters, constraints, and design features. Hence, finding the most suitable design based on specifications may be the most intuitive application to the digital IC design.

3.3.1 High-Level Synthesis and/or Register Transfer Level.

Crafting side-channel-resilient circuits. Referring to Section 3.2.2, masking has been introduced to stop an attacker from mounting side-channel analysis. AI has become an integral part of this—for instance, RL has been applied to combine a set of countermeasures, which leads to the enhancement of target resilience to, at least, some types of attacks \[210\]. Seen from another perspective, ML algorithms, and in particular, NNs, can defeat some countermeasures, including masking \[127, 199, 266\]. As an example of such attacks, RL has been employed to determine proper side-channel leakage models and training of NNs to extract leakage profiles \[211\]. Hence, robustness against such attacks has become one of the objectives of the tests conducted to evaluate the effectiveness of countermeasure, specifically, masking.

Given the nature of such tests, the security-aware designer may have to deal with the higher levels of abstraction corresponding to a black box leakage model because there is no information, including physical placement or routing signals \[36\]. Therefore, masking schemes may be implemented, but there is no guaranteed measure of effectiveness before the RTL stage. To enhance this process, full access to the design’s layout available to the implementing party could be useful and even be bolstered with an understanding of the device’s functionality via RTL or gate-level implementation. This is in line with the studies focused on modeling the implementation and simulating its behavior as discussed previously \[28, 208\]. In this context, AI has not yet reached its full potential, as security-critical implementations are still designed manually. The manual design and implementation pose a series of drawbacks stemming from (1) the lack of integration between the various designs, (2) erroneous designs due to human errors, and (3) high consumption of resources, including time (both execution and design times), silicon area, and/or power/energy consumption.

3.3.2 Physical Design.

Porting of cryptographic and hardware security primitives to different technology nodes. Security-aware updates to designs are hardly ever direct “out-of-box” additions to devices. For integration
of an IP or hardware security primitive, it is imperative that the design still fulfills its intended purpose. Selecting the most appropriate parameters for a hardware security primitive is one aspect, but another is porting it to a different technology node [125]. Although technology nodes no longer categorically correspond to transistor gate length and half pitch, they nonetheless vary considerably with respect to manufacturing processes, design rules, noise sensitivity, and so forth [21]. These variations are noteworthy because they may disrupt the transferability of primitives. For example, an optimized PUF applied to an IC manufactured using the 28-nm process is not guaranteed to transfer to the 22-nm process due to factors like geometric variation and transistor type [125]. The knowledge of process-specific parameters allows for assessment of the hardware primitive porting activity using ML. It is possible to use a classifier model as simple as an SVM to select the most suitable match between circuit and primitive without explicit knowledge of the design’s functionality.

**Anti-counterfeit and anti-tamper sensor optimization.** The scourge of IC counterfeiting continues to plague the semiconductor industry by flooding the consumer market with unauthorized, defective, and inferior versions of original chips and designs. From as far back as 2006, electronic companies have missed out on $100 billion of revenue due to counterfeiting [195]. The recent global chip shortage has created the avenue for these illegal devices due to demand exceeding current supply chain capabilities [141]. Recycled and remarked counterfeit ICs account for more than 80% of the counterfeits sold worldwide [92]. Hence, their detection has become a necessity to tackle IC counterfeiting. Recycled counterfeits are used chips fraudulently sold as new, whereas remarked counterfeits are inferior chips sold as higher grades.

Different sensors have been designed as a solution to these counterfeits, as seen in the work by Zhang and Tehranipoor [288] and shown in Figure 12. Their first of two proposed techniques uses frequency difference retrieved from paired ring oscillators (ROs) between an original and recycled chip to distinguish the two. RO frequency tends to degrade more with aging because the transistors in the RO gets slower with time [69]. Guin et al. [92] also add anti-fuses and fuses for CDIR (combating die and IC recycling). Their RO-CDIR implementation is negative temperature instability aware, which is valuable for flagging ICs with shorter usage [92]. To date, the design of these sensors such as number of inverting stages, choice of threshold voltage, and overall structure are chosen in an ad hoc manner or through empirical means. Further, foundries do not always provide aging models to users. Both of these limits the age estimation of such sensors and their classification accuracy. AI approaches, such as Bayesian optimization, would be preferable, especially for its ability to optimize black box functions. Automating the optimization process will ultimately make it less exhaustive.

Another source of hardware security issues is tampering. Once the device is physically compromised, it may leak on-chip information to the attacker. Hence, insertion of hardware Trojans may also be considered as tampering [242]. One common example of tampering is FIB-based circuit edit, which allows an attacker to remove or bypass a security countermeasure [160]. Similar to recycling, sensors have been proposed to combat or detect tampering. A technique proposed by Liu and Kim [155] uses logic-compatible embedded Flash (eFlash)-based tamper sensor built on an exposed floating gate structure to detect physical attacks. Any change in charge stored on the exposed floating gate can be detected by this sensor. This includes humidity, high temperature, dust particles, chemicals, and electrostatic charges. A regression-based model or an NN could fine-tune the configuration of such tamper sensors.

**Hiding countermeasure optimization.** If an attacker is aware that a sensor has been deployed to detect a certain attack modality, the attacker may start by circumventing the sensor. For example, the attacker may apply the minimum possible mechanical force on the metal wires or use a low
intensity light source for a longer duration of time. Assuming the maximum throughput possible, it is crucial to supplement successful optimization with robust defense. Hiding can dampen the signal accessible to the attacker. With limited knowledge of the sensor-IC design and operation, the designer could possibly rely on ensemble methods to find the most suitable hiding framework. The same sensors used to protect against tampering and detect counterfeits may also be vulnerable to side-channel attacks. Since they are sensitive to changing parameters like voltage and frequency, they are prime targets for malicious parties. Sugarawa et al. [234] show that an attacker can reveal the internal state of a chip by observing how a sensor reacts to laser fault injection. The leakage leads to a feasible, non-invasive, probing attack. The sensor type, the bit-flip detector, detects a short-circuit current induced by a laser fault injection [234]. Thus, it is advisable to supersede sensor optimization with robust hiding schemes; the ideal framework could combine both activities to boost resistance to side-channel attacks. For example, if a noise generator is used as the default hiding mechanism, a simple regression model could predict the amount of noise required to achieve a lower SNR. A more versatile system could have options like shielding in addition to noise generators, with decisions and settings also based on countermeasure optimization.

3.3.3 Cross-Abstraction.

Obfuscation for black box designs. Obfuscation is best implemented with complete structural and functional understanding of a circuit, but different levels of abstraction may present the challenge of having only one available. At the gate level, logic locking, as described in Section 3.2.2, may be viable, but the implementing party may also be restricted by their limited knowledge. Here again, a GNN seems capable of modeling the complex connections within the design, the competing needs to resist attacks, and narrowing down the most suitable implementation for balancing security and overhead. Ideally, the complete framework should provide locking options for each design and generate keys for a user discretely. Genetic algorithms (GAs) have been applied to logic locking attacks like GenUnlock [47], where the evolutionary process is a black box procedure overseen by an objective function. Conversely, this concept may be applicable to not only logic locking but also general obfuscation.

The physical design stage also presents opportunities for obfuscation to the designer with black box access using ML/DL. The current state of the art in camouflaging is the covert gate approach [226]. Covert gates are inserted randomly into the design/layout, but a CNN or ViT (vision-based transformer) can be incorporated to quantify the impact of insertion and ultimately identify the most viable gates to replace. Table 3 provides possible algorithms for the security tasks provided in this subsection.
Table 3. Security Requirements under Black Box Optimization or Design Space Exploration with Applicable AI/ML Algorithms

| Design Stage                                      | Security Task                                      | Applicable AI/ML Algorithms                     |
|--------------------------------------------------|----------------------------------------------------|-------------------------------------------------|
| High-Level Synthesis and Register Transfer Level | Crafting Side-Channel-Resilient Circuits           | RL [211], ANN                                  |
|                                                  | Porting of Cryptographic and Hardware Security Primitives to Different Technology Nodes | SVM                                             |
| Physical Design                                  | Anti-Counterfeit and Anti-Tamper Sensor Optimization | Bayesian Optimization, ANN, Multiple Linear Regression |
| Cross-Abstraction                                | Hiding Countermeasure Optimization                 | Bayesian Optimization, Ensemble Learning         |
|                                                  | Obfuscation for Black Box Designs                  | GAs [47], ViT                                   |

The cited options indicate optimization or security implementations available for reference.

3.4 Assimilation of Security Rules for EDA

The incorporation of AI/ML into EDA describes replacing traditional heuristics with DL and AI-based decision-making policies that integrate the preceding steps (decision making, performance prediction, and optimization) into a single EDA framework, as shown in Figure 13. This will ultimately lead to a custom-based EDA pipeline based on the specific design and/or security application rather than relying on generic, somewhat-archaic EDA tools. Unlike Section 3.3, the design space may stretch beyond what a designer has at their disposal. A valuable point to make is the possibility of utilizing a trainable decision-making policy in contrast to exploring the available decisions. The use of AI/ML almost guarantees more efficient results with shorter runtimes. There is budding research within the IC design community to incorporate learning-based tools into the EDA pipeline. The OpenROAD project is a DARPA-funded initiative that seeks to solve EDA cost and turnaround time. The goal is to complete the design process without performance, power, or quality tradeoffs using ML, cloud-based optimization, and other techniques [6, 58]. Their work so far has incorporated problem-specific tools like ioPlacer for fast and scalable input/output pin assignment [22], TritonCTS for clock tree synthesis [98], and RTL-MP for macro placement using RTL information and clustering [122]. Commercial companies continue to make strides in this aspect. A team of researchers at Google also presented a floorplanning tool for the physical design stage that can successfully place macro blocks using deep RL [178]. Its results demonstrated improvement over traditional manual efforts across performance, power consumption, and area, and allowed its application to a recent tensor processing unit product. Synopsys has been investigating the use of AI/ML for design space exploration to improve general QoR. Their DSO.ai tool searches for optimization targets in large solution spaces of chip design, using RL to enhance PPA metrics. Cadence also stakes their claim in this area with the Cerebrus Intelligent Chip Explorer. Like the DSO.ai tool, it seeks to enhance PPA metrics with improved productivity.

With AI/ML firmly established in the pipeline, design optimization and security could be combined. Design-specific EDA will make extraneous steps obsolete and ultimately reduce the time to market for ICs. Table 4 highlights some major security aspects of interest for each major design stage with accompanying AI/ML techniques. The Implemented column contains examples of existing work, whereas the Suggested column provides possible directions for future work.

The manufacture of secure ICs must begin with embedding of security rules at major steps of the design process. This encompasses the acts of identifying, assessing, and incorporating prerogatives and properties within specific stages. All design steps follow defined rules during their series of actions on the input design [126]. For example, during logic synthesis, minimization may occur by combining gate terms where applicable to reduce circuit size [34]. Even design constraints can
Table 4. Major IC Design Stages in EDA with Security Needs and Applicable AI/ML Techniques

| Design Stage                                      | Security Task                        | Design Type | AI/ML Algorithms Applicable |
|--------------------------------------------------|--------------------------------------|-------------|-----------------------------|
| High-Level Synthesis and Register Transfer Level | Obfuscated Design                    | ASIC, FPGA  | RL                          |
|                                                  | Masking                              |             | GNN [274]                   |
|                                                  | Information Flow Security            |             | GCN                         |
|                                                  | Obfuscated Design                    |             | ANN [230]                   |
|                                                  | Masking                              | ASIC, FPGA  | RL, GNN                     |
| Logic Synthesis                                  | Information Flow Security            |             | GNN                         |
|                                                  | Side-Channel Resistance              |             | GNN                         |
|                                                  | Fault Tolerance                      | ASIC        | Bayesian Optimization, DNN  |
| Device Sizing/ Technology Mapping                | Crosstalk Mitigation                 |             | Decision Trees              |
|                                                  | Anti-Tamper Layouts                  | ASIC, FPGA  | Logistic Regression, XGBoost [149] |
|                                                  | FDNs for Anti-Side-Channel and Fault Injection | | GCN, RL |
|                                                  | Anti-RF Layouts                      |             | GNN                         |
|                                                  | Personal Fabric                     |             | Linear Regression [249]     |
|                                                  | Custom eFPGA Fabric                  |             | GCN                         |
|                                                  | Test Point Insertion and Pattern     |             | CNN [283]                   |
|                                                  | Generation for Trojan Detection      |             | RL                          |
|                                                  | Information Flow Security            |             | GNN, DNN, RL                |
| Floorplanning and Physical Design                | Comparison of Original Specification to Final Design | | GNN                         |
|                                                  |                                     |             | Natural Language Processing [282] |

The implemented ones available are supplemented with possible methods for future work.

be described as rules because they define the behavior of the design at each point of usage. In the same vein, it is necessary to apply security rules as rigorous requirements throughout the entire design sequence.

Efforts to support such assimilation are starting to grow. For example, the Hardware Common Weakness Enumeration Special Interest Group (HW CWE SIG) [63] consists of researchers and representatives from organizations operating in hardware design, manufacturing, and security who interact, share opinions and expertise, and leverage each other’s experiences in defining hardware security weaknesses and identifying them with analysis tools. However, the current initiative is manual and quite subjective. Data-driven and AI-based approaches could make this less tedious and more objective in nature.

3.4.1 High-Level Synthesis and Register Transfer Level. The overall design of a circuit depends on the requirements stated in its specifications. Traditional execution of HLS results in an RTL description of the design, which is a better hardware-based representation of the intended IC. During the design process, it is difficult to ascertain certain features and how they may impact the entire circuit, but significant work has been done to mitigate this using ML [64, 169, 286]. One noteworthy ML-based optimization framework combines a GNN with RL to predict design results and obtain optimal solutions under user-specified constraints and objectives like area and latency [267]. The security-aware designer can also leverage ML to anticipate and solve security problems that an IC is vulnerable to. Security rules at this early stage of the design process are less tedious and reasonably inexpensive to enforce.
Obfuscated design. Pre-synthesis obfuscation is applied to a design prior to the logic synthesis stage. Although the most prevalent techniques are used post-synthesis, there has been work done on this early stage method of obfuscation. Obfuscation can be implemented at the high-level stage before conversion into RTL. One group uses MUXes driven by a locked controller units to create decoy connections [204]. Exploiting the MUX’s use of inputs and a control signal, only the correct control signals can unlock the design. Chakraborty and Bhunia [43] convert RTL code into control and data flow graph form, apply locking by superimposing an authentication FSM, and then return to RTL. Both applications may be deployed as security rules with DL-based execution. The control and data flow graph form could be implemented as a GNN for optimum modeling of a design’s complexity.

Masking. Masking to mitigate the effectiveness of differential power analysis during a side-channel attack is also possible at this level of abstraction. Konigsmark et al. [132] create an HLS flow that addresses side-channel leakage by inferring security critical operations from user-specified confidential variables in HLS input. Their modified framework rectifies imbalanced branches that pose easy attack targets and changes functional units based on leakage potential [132]. This experiment could be the foundation for learning-based masking solutions to prevent SCA; it stands to be improved by feature-based rectification.

Information flow security. It is important to verify that systems adhere to information flow security policies, especially during the design phase. All assets flowing through the system must be identified; this is known as information flow tracking [107]. Achieving this at higher levels of abstraction reduces the effort required to rectify potential problems. One publication presents RTLIFT as a means of measuring all digital flows through RTL designs to formally prove security properties related to integrity, confidentiality, and logic side channels [17]. Perhaps its most impressive property is the ease of integration into the design flow. Intelligent decisions surrounding security policies means adaptability to different designs tradeoffs such as the RL-based policy iteration to calculate digital flows and possibly flag irregularities [17].

3.4.2 Logic Synthesis. In general, logic synthesis has been extensively researched under AI/ML [184, 191, 192]. The RTL-to-gate-level process provides viable data to train models that have mostly been used for design optimization. The conversion from behavioral level to the gate level is the bridge between a design idea and its generation because the specific logic functions are implemented from combinations of gates selected in a given cell library.

Obfuscated design. At the gate level, the first form of obfuscation that may come to the security-aware designer’s mind is logic locking. One proposed work that could be the baseline for future AI/ML exploration is LeGO [10]. The authors point out that it can iteratively harden a design against a set of attacks. The framework begins by performing a simple key-based locking and continues with an iterative feedback process that considers a set of possible attacks to defend against [10]. The attacks are provided with corresponding countermeasures for integration. The rule selection algorithm, which uses prior knowledge from a database of mitigation rules, identifies the best protection to be applied for each key-bit against a specific attack. The “convergence point” occurs when all security issues are addressed [10]. The learning design could be improved with an RL-based policy iteration framework. With a suitable representation of the gate-level netlist and its features, there are many possibilities.

Masking/side-channel resistance. Similarly, in the quest for side-channel resistant designs, gate-level masking has been researched since the early 2000s. Masking is most ideal for implementation at this stage, because of the gate design’s correlation to the physical design’s functionality. In 2005,
masked dual-rail pre-charge logic (MDPL) was proposed as a promising differential power analysis resistant logic style [201]. MDPL circuits are based on a standard cell libraries and have no routing constraints concerning the balancing of complementary wires. The dual-rail pre-charge property of MDPL specifically prevents glitches in the circuit. A more recent implementation uses a technique that combats the phenomena of glitches and early propagation using only cell-level “don’t touch” constraints [140]. Their framework LMDPL (LUT-masked dual-rail with precharge logic, which is a derivative of MDPL) can work for both FPGA and ASIC designs. MDPL may be used as a rule-based template for masking gate-level designs. A GCN can be used to identify sections of the circuit that are vulnerable and would require MDPL implementation. Kolhe et al. [131] also introduce LOCK&RROLL to combat power side-channel attacks and SAT attacks using DL. Their best-performing technique is a DNN with an accuracy of 35.01%.

Information flow security. Information flow tracking at the gate level also serves to check adherence to security policies. The well-defined gate-level information flow tracking (GLIFT) technique has been widely used to design secure hardware architectures and detect security violations from visible timing flows. Hardware Trojan detection has even been accomplished based on harmful information flows that point to sensitive information leakage and data integrity violation [182]. From Figure 14, the RTL synthesis that produces the gate-level representation is followed by standard cell augmentation with shadow logic gate. Design stage verification is the most suitable application of GLIFT to the EDA pipeline. The technique only checks for violation of information flow security policies without addition of logic to the fabricated design. Once again, a GCN representation with sufficient features may be used to supplement, or even replace, GLIFT.

3.4.3 Device Sizing and/or Technology Mapping. Modern physical design flow includes gate sizing for PPA optimization, used in different steps ranging from synthesis to signoff. This process is algorithmic, assigning a proper size (gate type) to each optimizable design instance from a set of equivalent standard cell libraries for different process, voltage, and temperature (PVT) corners. For each of the instances, the available gate sizes are discrete values specific to the underlying technology. As the solution space scales exponentially with respect to the size of the netlist, gate sizing algorithms integrated into EDA tools rely on either heuristics or analytical methods, which leads to sub-optimal sizing solutions. To combat this shortcoming, Lu et al. [163] have demonstrated the feasibility of applying RL algorithms equipped with GNNs that encode design and technology features. Specifically, the problem of gate sizing for timing optimization at the post-route stage has been the main focus of the study. Although the proposed sizer adopts a more global optimization approach, it does not always outperform the commercial tool. Nevertheless, it has the great advantage that is automatic gate sizing for timing optimization without any human intervention.
The technology-mapping step converts internal representation and the optimized logic based on the designated technology library [57]. To improve the effectiveness of this process in terms of energy consumption, delay, and area overhead, approximate logic synthesis (ALS) is discussed in the literature, where the accuracy of mapping is compromised to meet the design requirements. However, techniques for ALS suffer from long execution time, which has been addressed by Pasandi et al. [191] by adopting RL-based strategies. Academic state-of-the-art ALS tools are considered to evaluate the performance of the proposed RL-based ALS. The results have demonstrated a great deal of improvement with regard to runtime and area and delay when the RL-based ALS is applied against academic and industrial benchmarks. Security-based optimization can also be added as a design goal for this automatic process.

**Fault tolerance.** Critical assets in devices may be compromised by taking advantage of errors from fault injection. Single event upsets affect sequential elements, whereas single event transients arise from combinational logic [33]. A single event upset may lead to a single event latchup, which results in a high operating current, or a short circuit. Fault tolerance reduces the sensitivity of devices to particle or laser attacks that cause these events. Glitches can be used to progressively break cryptography schemes or disable internal protection mechanisms [85]. Redundant computation is one way of making designs impervious to upsets. It uses double computation (in time or space) with a final comparison; if the results from redundant computations do not match, the output of the encryption function is suppressed/randomized. Redundancy may cause increased area and power consumption, but methods like the one presented by Petrovic et al. [198] show that high tolerance with moderate overhead is possible. The optimization procedure can be refined using a Gaussian process to find the best tradeoff value.

3.4.4 Floorplanning and Physical Design. The floorplanning step formalizes the high-level design established at the beginning of the process, and is followed by P&R to connect all blocks such that they meet design criteria and constraints. After initial P&R attempts, the design’s timing constraints are analyzed [172]. If unsatisfactory, the P&R software in use tries different placements and signal routing to try to meet the designated constraints. Even outside academia, work has been done on automating floorplanning to benefit the physical layout. Researchers at Google modeled chip floorplanning as an RL problem, and used a GCN representation of the design to optimize power, area, and performance [178].

To place application-specific integrated circuits (ASICs), designers must deal with millions or even billions of gate-level instances to be placed on constrained physical layouts. The placement directly impacts the quality of the final full-chip design, which is supposed to be assured by employing commercial EDA tools and spending a significant amount of time in optimization iterations (cf. [164]). In a series of work, the problem of providing automated and accurate placement guidance has been tackled through ML methods [76, 164, 165, 177]. Among these proposals, Mirhoseini et al. [177] have reintroduced RL into the chip placement domain of study. Goldie and Mirhoseini [86] provide roadmaps for placing an ASIC or FPGA netlist onto a grid, whereas Mirhoseini et al. [177] give more concrete answers to the problem of placing a netlist graph of macros (e.g., SRAMs) and standard cells (logic gates, e.g., NAND, NOR, and XOR) onto a chip canvas. The goal of these studies is to perform chip placement such that power, performance, and area are optimized according to the constraints on placement density and routing congestion.

Global routing is performed on a coarse grid map to find an approximate routing of all nets that is the basis for the detailed routing to specify the routing of each net and satisfy all design rules. Another pressing issue with electronic systems design is automatic routing considering wire length, crosstalk, via, and layer selection. Maze routers are traditionally used for this purpose, although they have two major limitations, namely (1) being not smart enough to perform detailed
routing considering signal integrity [102], and (2) needs for additional constraints and optimization variables to offer global routing. RL has been proposed to resolve these by integrating the concept of SI [128]. For this, Kim et al. [128] have designed an RL agent including an encoder-decoder model that is an effective tool for solving combinatorial optimization problems. Similarly, **deep Q-network (DQN)** agents are trained in the RL framework to encounter the global routing problem [150], where a single DQN conjointly routes the nets and pins in an IC. In this process, the DQN acts as an agent and interacts with the environment. Upon receiving the state information from the environment, the Q-values of all potential next states are evaluated, and an action is taken and executed. Consequently, the environment is updated.

These optimization-based techniques provide possibilities for applications toward more security-aware designs.

**Crosstalk mitigation.** Design scaling from a technology process may reduce spacing between adjacent interconnects; the resulting increased coupling capacitance between wires causes crosstalk [293]. The affected signal’s value may either change or have delayed signal transition. False clocking, where a clock changes states unintentionally, may also occur [244]. Good signal integrity is necessary for optimum functionality of an IC [88]. Large signal-integrity problems may cause intermittent success or complete system failure. To address crosstalk, the design tool must be able to measure its value. Chang et al. [46] find a closed form expression of crosstalk using a number of wires. With accurate metrics, a linear regression model coupled with the RL method applied in the work of Mirhoseini et al. [178] could address crosstalk expeditiously.

**Power distribution networks for anti-side-channel and fault injection.** Side-channel leakage is one of the results of the nature of an IC’s **power distribution network** (PDN). The PDN is responsible for the supply of stable voltage and power to each functional component of the circuit [172], but it may also inadvertently introduce side-channel leakages throughout the design [289]. The growing complexity of devices introduces sophisticated PDNs with the potential to allow successful side-channel attacks or fault injection. To improve the security of a design, it is important to use ML to build on existing work on this topic. PowerScout is a framework geared toward evaluating side-channel vulnerabilities by modeling possible attacks to improve PDN designs [294]. It can effectively predict leakage strength and also identify fault injection soft spots. The side-channel and fault injection attacks are modeled using non-learning-based design space exploration. A decision tree or an MLP could predict these with the same parameters being extracted. There may also be promise in modeling the PDN using a graph-based network and optimizing leakage-prone nodes for the physical design.

**Anti-tamper layouts.** Anti-tamper designs are meant to deny an adversary’s opportunity to monitor or affect the correct operations of an IC. At the layout level, one CAD assessment technique allows a designer to gauge a design’s susceptibility to frontside probing attacks [256]. The assessment is performed by varying attack parameters (FIB aspect ratios and angles), shield parameters (layers and shape), and the assets under attack (keys, buses, etc.). Two of the most useful aspects of the work are the EA, which is free to probe without impacting transmission, and shield structure taxonomy, which is a set of documented shield patterns [256]. Based on the attack parameters, EA and the shield taxonomy, an RL model could help recommend the best shield design for a layout.

**Anti-reverse engineering layouts.** At the layout level, IC camouflaging is an EDA engineer’s most suitable option to prevent successful RE. The camouflaged layout is a functional replica of the original design with camo gates (see Section 3.1). A novel framework for secure layout generation could focus on generating camo gates using GANs. Recommendations for camouflage points on an IC can be modeled using a GCN or a CNN.
Custom embedded FPGA fabrics. The **embedded FPGA (eFPGA)** is an IP core integrated into an ASIC that offers the reprogramming flexibility of FPGAs without their overhead costs. They are added to systems that require frequent updates; by adding their fabric to an SoC or ASIC, teams are able to modify applications seamlessly. One security evaluation in the work of Bhandari et al. [29] points out that eFPGAs can contribute to SAT attack resilience. The eFPGAs have combinational loops that a specific cyclic SAT solver like CycSAT [292] cannot solve. Increasing attack difficulty can be considered when creating eFPGA fabrics at the physical design stage. The incorporation of a policy-based model that incorporates this into an ASIC design could improve security considerably.

3.4.5 Testing and Verification. As an IC reaches its physical state, the designers must implement design testing and verification. It is important to point out that most major design stages reach completion via some form of verification step [260]. For example, the logic synthesis step utilizes an RTL and gate-level netlist verification procedure to guarantee functionality retention of the gate-level design [172]. Testing and verification combined ensure that an IC has maintained original specifications and functionality throughout the design process. For physical testing, the two most significant options are wafer-level testing and package-level testing [197]. Conventional software-focused methods to detect also provide avenues for AI/ML hardware verification. Mandouh and Wassal [170] proposed using $k$-means clustering to group signals trace segments that show high similarity and detect bugs that are rarely triggered during simulation. Using AI/ML provides increased coverage with better efficiency. Conversely, a supervised learning and RL method presented in the work of Hughes et al. [111] uses constrained-random IC design verification environment tools and is applicable to software verification.

**Test point insertion and pattern generation for Trojan detection.** DFT is a technique employed in designing ICs for the purposes of reducing test costs and associated time. A very common technique for DFT is scan-chain insertion; regular FFs in the design are replaced with scan FFs. ATPG is a test methodology used to identify faulty behavior(s) in circuits due to design defects. The goal of ATPG is to create a set of test patterns that achieve a desired test coverage, TC, and fault coverage, FC, through fault simulation [243]. ATPG and formal methods have been researched for Trojan detection, but most do not consider partial-scan instances of a third-party IP. Cruz et al. [62] generate a set of constraints using the model checker to facilitate directed test generation using the ATPG tool. A constraint generation procedure uses model checking to produce a set of signal traces. A test vector generation method then uses ATPG with the design, rare nodes, and signal traces to produce a set of test vectors for activating each rare node [62].

**Information flow security.** At the verification stage of the design flow, information flow tracking can be executed using static or dynamic techniques. Static techniques assess the design’s compliance with security policies using simulation, formal verification, emulation, or virtual prototyping. They are applicable within the EDA pipeline and are removed when verification is completed [107]. Due to the unique goals of each specific static technique, AI/ML can be added to decrease resource usage, and improve results. For hardware security simulation, levels of abstraction like gate level and RTL are viable. As described in logic synthesis, graph-based networks are ideal solutions. The simulation process links security labels to signals. Formal verification guarantees proof of security for the desired properties, but it is known to have scaling issues [107]. The large design state space of complex systems requires a policy-based learning solution that RL provides. Emulation can perform hardware-software co-verification, using FPGA emulation servers. Learning-based models could make these servers more robust to even detect software vulnerabilities that impact hardware. The abstract models of hardware components created by virtual prototyping can be tested a different RL-based approach. If the policy used is geared toward creating security problems while
verifying software, the designer becomes aware of impending problems. Dynamic techniques use dedicated hardware to track information flow during runtime. An NN could validate results to predicting flow inconsistencies.

Comparison of original specification to final design. Furthermore, natural language processing can be applied to circuit designs at different levels of abstraction. One of the most promising bridges to this is HW2VEC, a graph learning tool to extract graph representations from a hardware design in either RTL or gate level [282]. It is divided into two main parts: a HW2GRAPH stage, which converts the design to a graph while retaining structural information, and GRAPH2VEC, which converts the graph into Euclidean-based embeddings (Figure 15). GRAPH2VEC is just one of a number of graph-to-vector-embedding algorithms that utilizes concepts from the skipgram word embedding model [183]. The resulting vector representation may be applied with measures of similarity, like cosine similarity, to verify designs. If HW2VEC can be leveraged at physical design stages, the final IC product can be verified for structural authenticity.

4 AI FOR SECURITY-AWARE DESIGN OF ANALOG ICS

Analog ICs are the fundamental components that interface with the real-world signals that are continuous and arbitrary in nature. Hence, the design of analog circuits are considered the foundation for all IC design. In this regard, analog IC design comprises of design of analog, radio frequency, and mixed-signal ICs such as amplifiers, oscillators, filters, power regulators, and data converters. Analog IC design traditionally involves a lot of manual work and hence relies heavily on expert knowledge and intuition. This is the case because unlike their digital counterparts, analog design steps typically overlap and have a higher number of complex design constraints and specifications that need to be met simultaneously. Thus, the automation of design of analog circuits and consequently analog security primitives has not gathered a lot of traction compared to digital circuits. Nevertheless, it has become paramount that the design of analog circuits be automated with the inclusion of security-aware features for the following reasons:

- **Bottleneck of the design process:** Design of analog ICs involves a lot of manual steps as explained earlier and are hence considered the bottleneck in any electronic system design [238]. Since analog ICs are prevalent in almost all ICs, it is imperative that they be designed as swiftly as their digital counterparts to meet the current demands of low power, high performance, and quick time to market. Furthermore, this increasing demand coupled with error-prone manual process demands an inclusion of security-aware features in the design.
- **High susceptibility to reverse engineering:** Analog ICs are generally fabricated in higher or older technology nodes compared to digital ICs. They also have fewer number of
transistors (in orders of hundreds compared to billions) and have a lower current density, which makes it easier for the attacker to figure out the underlying IP using the process of reverse engineering [7].

- **Lack of cryptomodules, error tolerance, and security primitives:** There is a severe lack of security features and primitives applicable for analog ICs, as a large amount of research has focused on digital ICs [7].

- **Impact of process variation:** Robust analog design has become ever so challenging with the continuous advancement in technology node and device scaling because the analog parameters are affected significantly more across PVT variations. This has made the design of reliable analog circuits quite strenuous [207].

- **Lack of comprehensive descriptiveness of design and security issues in conventional CAD approaches:** Depending on the type of analog IC, the specifications and requirements vary quite a lot. Hence, one unified framework or CAD approach is not applicable to the design of analog ICs. Hence, there is a severe lack of comprehensive description of design and security issues in traditional CAD approaches [221].

- **Inapplicability of most digital based security solutions:** The design flow of digital ICs is significantly different compared to analog ICs. Hence, the design and security approaches proposed for digital ICs are not applicable for analog and even mixed-signal ICs. Furthermore, the design of these security features require design and cost overheads that are only expendable in the case of large digital ICs.

Henceforth, in this section, we focus on the recent developments of the use of automated techniques including AI-based approaches and optimization techniques in the design of analog ICs and security primitives.

### 4.1 Optimization Techniques for EDA

ML models instead of pure optimization algorithms have been extensively used to automate the design of digital circuits, which has significantly reduced the time complexity associated with designing a robust digital IC. Furthermore, they are able to learn from the previously explored designs and datasets [108]. However, training ML models is a challenge specifically in the analog domain compared to digital ICs. Hence, one unified framework or CAD approach is not applicable to the design of analog ICs.

- The specifications of analog design are variable for different applications. Thus, it becomes difficult to construct a uniform framework to evaluate and optimize different analog designs [176].
- It is challenging to design a well-performing model because analog parameters are highly non-linear and susceptible to noise and PVT variations [84].
- The models trained for design automation have worked well for digital circuits compared to analog because analog designs suffer more in terms of area, power, and reliability when porting from a higher node to a lower technology node.
- The search space for analog design is significantly larger compared to digital IC design. There is variety of circuit schematics and device sizes that a designer can consider to get a reasonable performance. Plus, there are more specifications to meet for an analog IC compared to their digital counterparts. This makes it computationally expensive and time consuming to train a decent model.
- Analog design is less systematic and more heuristic and intuitive in nature [84]. Thus, there has been a substantial amount of automated design software tools available for digital IC design, which makes it easier to generate data and train models to optimize the design process.
Because of the reasons outlined previously, there is an abundance of “automation” frameworks that use one or more optimization algorithms in conjunction with the simulation software to optimize the design of a specific analog circuit. Many situations call for multi-objective optimization problems, as is the case when designing security primitives, as they have additional challenges and specifications to meet depending on the type of analog circuit at hand. Nevertheless, depending on the search space and the problem at hand, optimization techniques can be divided into three categories:

1. **Random or brute-force search**, which involves randomly generating a solution until the optimization criteria is satisfied. Both are time consuming.

2. **Gradient- or derivative-based optimization** utilizes gradient or derivatives within the data or the objective function to guide the search for the optimal solution [235]. Gradient descent is one of the most widely used techniques, specifically in ML algorithms. Both are computationally efficient and quick but prone to getting stuck at a local minimum rather than a global optimum if not designed properly. Further, both require functions that are differentiable.

3. **Heuristic derivative-free optimization** methods utilize heuristic techniques characterized by empirical rules to guide the search process to find an optimal solution. The most popular algorithms are EAs and simulated annealing, which are inspired by Charles Darwin’s theory of evolution and the annealing techniques in metallurgy, respectively. They are highly effective especially when derivatives or gradients do not exist and the search space is highly non-linear or noisy. However, they are quite time consuming, and the quality of solution is highly dependent on the initial configuration and learning rules.

However, with the progress in high-performance computing hardware and ability to model nonlinear problems, DL and RL methods have gained a lot of popularity in recent years. Specifically, RL has gained a lot of traction in analog design and optimization, where their counterparts, EAs, have been applied for more than a decade [284].

### 4.2 Analog IC Design Flow and AI/ML Techniques

Figure 16 provides a general overview of analog IC design, which is drastically different compared to the digital circuit flow shown in Figure 5. This is a top-down design approach as described by Giel- len and Rutenbar [84]. First, the analog IC designer chooses a topology and designs the schematic such that a given set of design constraints and specifications are fulfilled. Then, the transistors and other analog elements are sized very carefully and simulated using a circuit simulator. Next, the layout engineer generates the physical implementation of the IC based on the schematic, performs physical verification (DRC and LVS), extracts the parasitics, optimizes the location of circuit elements to fulfill the area and power specifications, and performs the post-layout simulation. This process of layout and simulation continues until the specified physical constraints are met, after which the IC is ready to be fabricated. The design process is completed by testing the analog IC against the design specifications. If the IC fails the test, then the analog designer has to repeat the whole process and either resize the design or choose a different topology altogether. This process usually goes for several iterations until the IC is ready to be fabricated at a large scale.
Table 5. AI/ML Techniques Used in Every Design Stage of the Analog IC Design Process

| Design Stage         | Techniques                          | AI/ML Algorithms Used                                                                 |
|----------------------|-------------------------------------|---------------------------------------------------------------------------------------|
| Topology selection   | Selection                           | CNN [174], Polynomial regression [124]                                                |
|                      | Feature extraction                  | Supervised/unsupervised learning [143], GNN [136]                                     |
|                      | Generation                          | RNN [214]                                                                             |
|                      |                                     | SVM [68], RBF/MLP [193], Bayesian NN [81], ANN with sparse regression [241], DNN [239], ANN [71, 162], Gaussian-based regression model [218], SVM [262], BO [109], RL [291] |
|                      | Model based                         | CNN [174], Polynomial regression [124], Bayesian NN [81], ANN with sparse regression [241], DNN [239], ANN [71, 162], Gaussian-based regression model [218], SVM [262], BO [109], RL [291] |
| Circuit sizing and biasing | Simulation based                   | ANN [30, 114, 115, 147, 265], RL [222, 258], GA [65, 101], Hybrid EA [154], RNN and DNN [264], GCN [257], ANN with polynomial regression [161] |
|                      | Behavioral modeling                 | Time-delay NN [87], ANN [287], RNN [180], Bayesian linear regression and SVM [188], Augmented NN [281], RNN [50], NN [103], ANN with GA [70] |
|                      | Placement                           | ML [135], Spectral graph analysis [48]                                                |
|                      | Routing                             | ANN [90, 94], GNN [146], (SVM, NN, RF) [145], LP [48]                                 |
|                      | Performance modeling                | Generative NN [295], grid-based A* [48]                                               |
|                      | Post-layout and test                | DNN with ES [96], ANN with polynomial regression [161], (SVM, NN, FL) [145], CNN with TL [156] |
|                      | Fault diagnosis                     | Decision tree [231], RideNN [31], GB-DBN [159], DBN [290], BMF [254]                 |

4.2.1 Topology Selection. Topology design and selection is the first step in the design of analog ICs. This step is one of the most critical and time-consuming steps due to its impact on the circuit performance. Traditionally, it is carried out manually by designers with expert knowledge and intuition. With demands for high-performing analog circuits increasing, researchers, as shown in Table 5, began to explore ML techniques that speed up the topology design process. Most of the early work focused on small functional units such as amplifiers and filters using simple search-based algorithms. Recently, Matsuba et al. [174] attempted to use CNN to select from only four topologies of an amplifier with 13 different characteristics. Similarly, Kaya et al. [124] used design space exploration to generate different Pareto-optimal fronts in the context of balancing design specifications across different topologies. These Pareto-optimal front based topologies are then fitted into a polynomial regression model for the final selection; however, the performances of these techniques are highly dependent on the created datasets. Some researchers [136, 143] have instead used feature extraction techniques to ensure that the complex relationships between various topological components are well understood by the algorithm. Li et al. [143] use both supervised and unsupervised methods to extract features of sub-blocks and connections within a topology, whereas Kunal et al. [136] use GNNs to extract symmetry constraints among different topologies. However, none of these techniques generate a topology automatically. One of the recent works [214] uses RNNs and hypernetworks to generate a topology for a two-port circuit.

4.2.2 Circuit Sizing and Biasing. After a topology is selected for a specific design, the next step is to size the components within the circuit and bias the design appropriately to meet the desired specifications. This step is also referred to as analog synthesis. Depending on the number of components, this step is one of the most tedious ones, as the design space is fairly large. As shown in Table 5, there have been even more ML and optimization techniques to automate this step. These works can be briefly categorized into two different techniques: model based and simulation based.

Model-based techniques. These use regression models or surrogate models to represent the performance of the circuit. They are thus quicker than the simulation-based approaches that rely on
circuits to continuously optimize the parameters of the circuit. Most of the model-based works have either used NNs [71, 81, 162, 193, 239] or regression models [218, 241], all in the attempt to speed up the circuit optimization and evaluation process.

**Simulation-based techniques.** These are considered superior since they are able to closely match real world (or post-silicon) circuit performance. Traditionally, simulation-based techniques have used evolutionary approaches (EA) such as GAs as seen in other works [65, 101, 154] to synthesize a wide range of analog circuits. There have been a lot of works using NNs [30, 114, 115, 147, 265] to help find appropriate circuit parameters and biases; however, these techniques only work for a specific circuit, such as an amplifier or a filter. The goal has always been to either reduce human effort or mimic human intuition in designing these analog circuits. In this regard, some works [222, 258, 291] have used RL to design common analog circuits as much as 25 times faster than traditional optimization algorithms. Zhao and Zhang [291] used the RL framework along with a symbolic analysis based approach that rapidly evaluated the circuit output without invoking a simulator.

One of the reasons that RL-based approaches are gaining more traction these days is because of their ability to quickly learn and find the balance across different specifications. The other reason is their ability to transfer their knowledge, which experts expect will enable IP reuse, rapid automation, and porting between different technology nodes. Inspired by this ability, Wang et al. [257] used GCNs to extract features of components and connections within the circuit and the RL agent to transfer these features whenever possible (e.g., features between a two-stage and a three-stage amplifier) and tune the circuit parameters quickly. In both cases of transfer learning (TL) (i.e., between technology nodes and circuit topologies), the proposed RL-based sizing achieved the highest figures of merit when compared with conventional black box optimization methods and human expert designs. Similarly, Settaluri et al. [222] use the NN as their RL agent (Figure 17). TL is also enabled here since the RL agent trained by running inexpensive schematic simulations can transfer its knowledge to a different environment (i.e., the design including layout parasitics). The results for post-layout simulations provided in the work of Settaluri et al. [222] demonstrate that it can converge faster than the traditional EA-based approaches.

4.2.3 **Simulation.** The next step in the design process is simulation to check whether the synthesized circuit satisfies the design specifications or not. Analog designers heavily rely on circuit simulators such as HSPICE and Cadence Spectre to assess the performance of their designs. However, behavioral modeling based techniques as shown in Table 5 have been proposed to speed
up the simulation process and depending on the circuit application tune these models to assess application-specific performance metrics with more accuracy. In this regard, researchers have turned to NN-based learning and modeling [87, 180, 188, 287]. For instance, Grabmann et al. [87] used time-delay NN to generate energy-aware AMS IP cores. Similarly, ML algorithms along with optimization techniques have been used to find optimal solutions across a wider search range effectively and efficiently. In this regard, Pan et al. [188] first create the data by exploring different device behaviors across different technologies, which is then fitted to a Bayesian regression model. Finally, SVM along with GA is employed in parallel to reduce the runtime compared to a pure EA-based optimization framework.

4.2.4 Layout. ML and AI techniques have also been employed to automate the layout of analog circuits. Kunal et al. [135] summarize early efforts in putting together an open-source quick layout generation flow for analog circuits that leverages template-driven design and ML techniques without human designers in the loop. In this regard, the recent work MAGICAL [48] takes an unannotated netlist and design rules as inputs to create a complete GDSII using an automation framework. They use spectral graph analysis for layout, LP for placement, and a grid-based A* algorithm for efficient optimized routing. Recently, graph-based ML networks such as GNN have been used to create models that predict the performance for a given placement and allows knowledge transfer between different analog circuits [146], which achieves better performance than CNN and regression-based plug-in approaches. Similarly, GeniusRoute [295] uses variational autoencoders to extract latent layout strategies based on human expertise and then trains a generative NN based model to guide the automatic routing.

4.2.5 Post-Layout and Test. Post-layout simulation involves numerous iterations of verification and redesigns until the desired specifications are met. This is mainly due to the domination of layout parasitics. Performance modeling techniques such as BagNet [96] use DNNs along with cross-entropy and canonical evolutionary strategies to reduce this number of iterations significantly by leveraging past information and improving the optimizer’s sample efficiency. Similarly, the recent work by Liu et al. [156] uses CNN and TL to enable early design pruning for effective design space exploration and ensure robust well-performing placement features. Further, the difficulty in obtaining accurate performance models of analog circuits has led to data-driven fault-diagnosis models for correctly assessing the analog circuit design. However, because of the highly non-linear and complex nature of analog performance faults, DL-based techniques [31, 159, 290] have fared better compared to shallow networks [231, 254]. Specifically, the use of deep belief networks (DBNs) have proven to be most effective, as evident in other works [159, 290], because of their ability to use raw time domain signals as inputs and employ an adaptive feature extraction and fault classification techniques.

4.3 Security Issues in the AMS IC Design and Fabrication Flow
The security issues pertaining to analog ICs are summarized by the supply-chain vulnerabilities that have increased within the past decade or so as a result of globalization. These issues, as shown in Figure 18, can be categorized into hardware Trojans and IC counterfeiting.

4.3.1 Hardware Trojans. As discussed previously for digital ICs, Trojans are intentionally created anomalies that remain hidden and difficult to detect because they are triggered by rare conditions. Analog Trojans can be further categorized into charge-based Trojans [129] and hidden backdoors such as covert channels established by exploiting process variations [232]. Charge-based Trojans either use switched capacitors to design a trigger circuit or exploit capacitive couplings to design Trojans with no area overhead [129]. Hidden backdoors in the case of analog ICs
mainly pertain to wireless RF networks where a Trojan circuit is designed to establish a previously unknown channel by exploiting process variation margins of the target circuit [232]. Although it is difficult to design purely analog Trojans (analog payload with analog trigger), they are more attractive than their digital counterparts because of their smaller footprint and their incompatibility/invisibility to digital functional testing and verification techniques. As such, there are works in AMS ICs where the trigger is hidden in the digital portion of the IP and its payload is transferred to the analog portion via a test access mechanism [75]. With the advent of analog EDA tools and ML-based approaches to circuit design, it opens up more opportunities to exploit such tools and approaches to design analog hardware Trojans efficiently.

4.3.2 IC Counterfeiting. Analog ICs are one of the most widely reported counterfeited parts among all types of ICs [1]. The major reasons for analog counterfeiting are twofold. First, they are easy to reverse engineer because of low transistor count and large transistor footprint. Second, analog IP design is cumbersome, manual labor intensive, and highly dependent on knowledge expertise; hence, their value is significantly higher in the black market [216]. IC counterfeiting can be briefly categorized into IP piracy, IC recycling, reverse engineering, overproduction, and sale of defective ICs, as shown in Figure 18. As these are supply chain related issues, the use of automation tools and AI/ML techniques does not change the degree of vulnerability of the analog IPs. However, the use of such techniques does give rise to more opportunities in terms of security-aware design and security primitive optimization. The next section describes some of the security primitives that can be designed and exploited at different design stages.

4.4 Design of Analog Security Primitives within the Design Flow

Table 6 summarizes analog security primitives that employ either ML algorithms or an automation framework based on popular optimization techniques at various stages of the analog IC design flow. The table also mentions the associated security issues that are tackled by these proposed security primitives.

4.4.1 Physically Unclonable Functions. As discussed earlier, PUFs are hardware security primitives that can either be used to create hardware authentication mechanisms or generate unique keys for cryptographic schemes. PUFs are devised by exploiting the inherent process variation or uncontrollable randomness present in every IC from manufacturing. This capability makes them a low-overhead, volatile security primitive that is more resistant to physical, side-channel, and software-based attacks. PUF design usually involves utilizing a specific circuit structure present inside an IC during the design step to function as a PUF. For example, the analog PUF proposed in the work of Alvarez et al. [14] leverages the threshold voltage mismatch between transistors in a cascode current mirror. With the size of ICs shrinking over the past few years, the limited number of input/output pins and the difficulty of meeting both analog- and PUF-based specifications has made it challenging to devise a PUF suitable for analog ICs. In recent years, a few researchers have leveraged circuit sizing based automation and optimization tools to design robust PUFs that can produce unique yet random and reliable output bit suitable for device authentication.
Table 6. AI/ML-Based Techniques and Primitives to Tackle Security Issues in Analog ICs

| Design Stage  | Techniques                        | AI/ML Algorithm                      | Security Issues Tackled                  |
|---------------|-----------------------------------|--------------------------------------|-----------------------------------------|
| Circuit Design| PUF [52, 223]                     | RNN [223], GA and LP [55]           | IP Piracy and Counterfeiting            |
|               | Logic Locking [93, 253]           | ANN [253], Simulated annealing [93] | IP Piracy [253], Overproduction [93]    |
| Layout        | ObfuscX [285]                     | Explanability with RepTree           | IP Piracy, Hardware Trojans             |
| Simulation    | Aging simulation                  | RNN [213], k-means, NN, and SVM [219]| IC Recycling                            |
| Fabrication   | Split Chip Design [187],          | Branch-and-bound algorithm [187],    | IP Piracy                               |
|               | Fab-of-origin [5]                 | PCA, DNN, etc. [5]                   |                                         |
| Test          | Side-channel fingerprinting and   | ANN [157], MLP and CNN [99], PCA [40],| Hardware Trojan [157],                  |
|               | Authentication mechanisms         | SVM [4, 45], k-means, k-nearest neighbors, SVM [54] | Counterfeiting and Cloning [40],        |
|               |                                   |                                      | IC Recycling [4, 45, 54, 110]           |

Chowdhury et al. [52] use GA and LP to size the transistors of an asynchronous null conventional logic (NCL)-based gate (e.g., the NCL TH22 gate) to devise a PUF circuit. This PUF utilizes the startup characteristics of cross-coupled inverters to produce a metastable output. The circuit is sized such that this output is only affected the inherent process variations and mismatch of the inverters inside the NCL structure. Because of the asynchronous nature of the circuit, this PUF is applicable for AMS circuits. Similarly, the recent work of Shah et al. [223] demonstrates a way to convert any circuit to a recurrent PUF. This is accomplished by utilizing an RNN-inspired technique involving combination of recurrence and XOR to generate a response (PUF output) that has very little correlation to its corresponding challenge (PUF input). They use the current mirror array (CMA) architecture proposed in the work of Wang et al. [263] and improve its output reliability and its resiliency against ML-based attacks. In CMA-PUF [263], transistors are sized small and are operated in sub-threshold region to maximize the mismatch. Further, the PUF utilizes a current-controlled oscillator (CCO) to digitize the current values of each column in the CMA. Subramanyan et al. [223] propose an Rec-CMAPUF where they replace a CCO with a shared comparator to eliminate each column CCO’s bias. They then feed the comparator’s digitized output back to the input and perform the XOR operation to get the final output. This feedback or recurrence operation introduces non-linearity in the challenge-response pair space and increases the resistance to ML attacks. As analog PUFs are becoming more attractive, especially in the context of cryptographic ICs, the DL-based sizing tools like RL-based tools will surely be used to explore the design space and devise more reliable PUFs. For example, the sizing tools in other works [222, 257, 258] can easily be used to include the PUF specifications as the additional design requirement and size the circuit to design a PUF robust across all possible challenge-response pairs.

4.4.2 Analog Locking Techniques. There have been several attempts to expand logic locking to protect analog ICs from piracy and counterfeiting. These techniques either try to obfuscate the circuit current or the voltage biasing to hide the correct functionality of an analog IC. However, most of these techniques are susceptible to logic removal and model approximation attacks [3, 117] because of low transistor count, large transistor size, and the fact that the key is implemented in digital domain. To improve the resiliency against such attacks, logic locking techniques utilizing ML algorithms have been proposed. Volanis et al. [253] proposed the use of an on-die analog NN where the trained ANN acts as a lock and its analog input acts as a key. This is achieved by eliminating direct access to the biasing inputs of the analog IC by utilizing the ANN for biasing the IC to its operating point. The ANN is made programmable by the use of floating gate transistors that serves as a permanent storage for the synapse weights. Furthermore, the keys are in analog domain and are continuous in nature allowing for a large number of key options making this locking technique resilient against brute-force and logic removal attacks. However, because of the very same fact, there exist several possible keys that can give one similar performance as the oracle.
output. A possible way to ensure that does not happen is to find a global solution using methods such as the one described in the work of Li et al. [147] that utilizes GA-based global search and ANN-based local minima search techniques.

Similarly, Jayasankaran et al. [93] attempt to tackle the issue of overproduction of an IC by a foundry. This technique, however, implements the lock in the digital section of an AMS circuit to minimize the effects of process variation by implementing a tuning knob to optimize the values of passive components in an analog circuit. The lock essentially controls the tuning knob based on an on-chip simulated annealing based digital optimizer [259] to help nullify process variation-related effects. This optimizer hence acts as an post-processing tool that helps obtain a robust output. However, the area overhead of implementing the self-optimization architecture and the lock is too high for a typical AMS circuit such as band-pass filter, LNA, and a low-dropout oscillator (LDO) as proposed in the work. This could be overcome by designing robust analog models using learning-based approaches [103, 188] to find optimal design parameters without the use of additional circuitry. Moreover, the RL-based techniques [222, 257] can tune the design to be robust against process variations by using multiple design runs and leveraging its TL abilities.

#### 4.4.3 Layout Obfuscation

Zeng et al. [285] proposed an obfuscator for split manufacturing that relied on explainability of ML-based attacks. As discussed earlier, split manufacturing is a technique where the untrusted foundry only receives and fabricates a partial layout to prevent the attacker from extracting the full design or IP of an IC. However, this still does not prevent ML-based attacks if the layout is either not obfuscated properly or is not obfuscated at all. The method in the work of Zeng et al. [285] implements different routing-based obfuscation techniques such as blockage insertion, routing perturbation, and wire lifting based on an explanatory metric devised by leveraging ML attack models. The metric SHAP (Shapely additive explanation) value essentially helps identify the most vulnerable connections within a layout and helps the obfuscator redo the obfuscation until the desired SHAP value is reached. This obfuscator can be easily incorporated with automated layout tools such as MAGICAL [48] to perform highly secure layouts of analog ICs.

#### 4.4.4 Aging Simulation

Incorporating aging analysis and simulation in the design step helps the designer or the IP owner characterize the performance of the circuit according to its life cycle or usage. Such characterization can also help classify if the chip has been recycled or not. There are commercially available tools such as RelXpert by Cadence [220] and MOSRA by Synopsys [248] that calculate the damage to transistors at incremental simulation times. There are also behavioral models utilizing RNNs to model aged circuits, as RNNs are compatible with transient current simulation. The trained RNN models can effectively predict the behavior of a “fresh” circuit if it is aged and inversely can help predict the age of an used or aged chip [213]. In this regard, some works [45, 54, 213, 219] utilize different ML algorithms to predict the age of an used IC. The recent work of Krishnan and Palanisamy [219] can predict as low as just 1-day of aging. However, the success of this classification is highly dependent on the aging model developed during the design step, which uses the model library, the aging models, and Monte Carlo simulations to help distinguish between process variation related changes and aging-related effects. Incorporating circuit specific behavioral models developed using ML techniques such as the operational amplifier model in the work of Murphy and McCarthy [180], the LNA model of Dumesnil et al. [70], and the oscillator model of Yu et al. [281] can help design more accurate and robust aging models for various analog circuits. These aging characteristics can be further used after the chip is fabricated by comparing the output performance of fresh, unused ICs to a used one. There are several such techniques proposed that will be explained in Section 4.4.6.
4.4.5 Split Chip Design and Fab-of-Origin. Split chip design as proposed in the work of Pagliarini et al. [187] differs from its previous counterpart split chip manufacturing proposed in the work of Vaidyanathan et al. [250]. The split chip design consists of dividing the entire chip design into two parts such that they can later be integrated to produce the intended functionality. By doing this, split chip design avoids technological complexity and logistical challenges of split manufacturing. The design partitioning into multiple sections is then formulated as an optimization problem that is solved using a branch-and-bound algorithm. The objective function is devised based on the vulnerability metric, which is essentially the product of exposure (effectiveness of a particular configuration) and criticality (importance of individual models) [187]. Split chip design has been described as being effective in tackling the problems of IP theft and piracy within the IC supply chain. However, the chip is split into multiple parts after the design is finalized, meaning that the appropriate topology is selected and the circuit is already sized and biased appropriately. The circuit designer can easily incorporate this vulnerability metric based optimization with the automated circuit sizing tools such as the one shown in Table 5 to design even more secure analog circuits. Similarly, Ahmadi et al. [5] proposed a fab-of-origin attestation technique that leverages wafer-level parametric measurements without any information of the design underneath the die to distinguish between chips fabricated in different facilities. The authors proposed solutions for different scenarios related to this attestation problem and relied on several ML techniques such as PCA and DNN.

4.4.6 Side-Channel-Based Fingerprinting and Authentication Mechanisms. The side-channel parameters such as power, delay, and EM emitted by an electronic device can be used as a fingerprint of such device to statistically assess if the device is authentic or not. There are several works that make use of behavioral models developed during the design stage to help characterize a fabricated chip as authentic or not. In this regard, the concurrent hardware Trojan detection technique proposed in the work of Liu et al. [157] helps detect Trojans in a wireless RFICs specifically in cryptographic ICs by continuously extracting side-channel fingerprints and evaluating them on a trained on-chip neural classifier. This classifier essentially looks for systematic variations introduced by the hardware Trojan in the transient supply current to expose the malicious operation. Similarly, the work of Hanna and Cabric [99] trains behavioral models (MLP and CNN) of RF transmitters to devise an authentication mechanism. Essentially, these models exploit the non-linear characteristics exhibited by the power amplifier to uniquely identify each RF transmitter deployed in the field. The authors evaluated these models under various factors concerning the effects of signal quality, packet length, channel model, and modulation type to demonstrate its effectiveness. Similarly Casto [40] proposes to use process-specific functions (PSFs) for authenticating AMS ICs such as data converters. The harmonic frequencies and their corresponding magnitude levels are used to develop the PSF-based device identification model. The presented results showed the detection rate of 90% using PCA and the PSF-based model. These side-channel-based fingerprints, however, may not be as effective once the circuit starts to age. Hence, integrating aging models during the design step such as that in the work of Rosenbaum et al. [213] can help design robust fingerprinting mechanisms. Similarly, there are several techniques (e.g., [45, 53, 54, 110]) that instead exploit aging characteristics without the behavioral models to train a classifier that can successfully distinguish between an aged and an authentic IC. However, these techniques require the use of a golden IC to train an effective model.

One of the recent works [4] that is basically the extension of the work of Chowdhury et al. [54] instead devises an odometer by repurposing the existing LDO structure present inside almost every IC. This LDO odometer basically contains two different paths: a reference path that is not aged even when its send out to the field, and a normal path that is activated when out in the field. This
Table 7. Security Vulnerabilities Faced by Analog ICs

| Attacks on:                  | Technique          | AI/ ML Algorithm               |
|------------------------------|--------------------|-------------------------------|
| Analog design                | Reverse engineering [60] | Evolutionary computation [60] |
| PUFs                         | Poster attack [279], Ensemble meta-algorithms [252] | Simulated annealing and EA [279], Bagging and GB [252] |
| Logic locking techniques     | Attack of the genes [3] | GA [3]                        |

self-referencing approach and a trained one-class SVM is then exploited to help characterize if the chip is recycled or not [4] without the use of a golden IC. These aging-based classifiers can be improved by developing behavioral models at the design step, which can help better characterize the profiles of these analog devices. For example, the learning methodology to develop behavioral models for complex MIMO system in the work of Hasani et al. [103] can be used to characterize the LDO in the work of Chowdhury et al. [54] and the oscillator and LNA in the work of Chang et al. [45] at the design stage, which helps improve the robustness of these aging-based authentication mechanisms. Furthermore, the automated synthesis techniques (e.g., [222, 257, 258]) can be used to size the odometer in the work of Acharya et al. [4] without incurring extra area and performance overhead.

4.5 Security Issues for Analog Security Primitives

Table 7 summarizes some of the techniques that utilize ML and optimization algorithms to execute attacks on an analog IC.

4.5.1 Attacks on Analog Design. The reverse engineering technique proposed by Cornforth and Lipson [60] was one of the earliest works that used evolutionary computation to reverse engineer the netlist of a simple non-linear analog IP by treating the circuit as a "black box." Although the reverse-engineered netlist might differ from the actual netlist, the performance of both of these circuits matched rendering the success of such an approach. The recent automated design approaches, especially the ones using DL- and RL-based techniques, may be used to reverse engineer an analog circuit. For example, the automated CNN-based topology selection technique in the work of Matsuba et al. [174] and the RL-based circuit sizing tool in the work of Wang et al. [258] can figure out the netlist with comparable performance within a day. Furthermore, MAGICAL [48], the automated layout technique, can perform an optimized layout that might even outperform the actual design.

4.5.2 Attacks on PUFs. Although PUFs could be resilient to physical as well as ML-based attacks, there are several works that leverage ML techniques to attack a PUF. The work proposed by Ye et al. [279] was one of the first works that used a compound heuristics of the evolutionary strategy, simulated annealing, and the ant colony to efficiently attack current mirror PUF [134] and the voltage transfer PUF [251] with an accuracy of 99%. Similarly, Vijayakumar et al. [252] use bagged trees and a boosting technique to attack the non-linear analog PUFs. Bagged trees basically aggregates predictions from different instances of decision trees that are fed with disjoint subsets of training set to obtain the final response, whereas the boosting ensemble of meta-algorithms is used to reduce the inherent bias present in decision trees by increasing the model complexity. Nonetheless, Vijayakumar et al. [252] elaborate on some analytical techniques based on the principle of functional composition to evaluate a PUF on its ML-attack resistance. These techniques can be used as security constraints during the process of analog synthesis using automated sizing frameworks (e.g., [222, 258]) to size the PUF accordingly and design an ML-attack-resistant PUF.

4.5.3 Attacks on Logic Locking Techniques. There are several methods proposed to attack analog logic locking techniques (e.g., [3, 116]). Both of these works assume that the attacker has...
access to the obfuscated netlist and knows where in the IC the key is being applied. The work of Jayasankaran et al. [116] uses the SMT solver to extract the correct key locking the analog circuit, whereas the work of Acharya et al. [3] uses GA to find the obfuscated parameter and the secret key. For this purpose, they devise an objective function based on the difference of the oracle output and the simulated output where the simulated output represents the output obtained by applying a random key generated using GA. Then given the oracle output and the obfuscated netlist, they demonstrate how the attacker can easily estimate the value of the obfuscated parameter to reduce the search space for finding the correct key.

5 GAPS AND OPPORTUNITIES IN AI-BASED SECURITY-AWARE EDA

5.1 Ecosystem Essentials for Accelerating Research and Development

5.1.1 Open-Source Benchmarks, Benchmark Generation Tools, and Data Augmentation. The academic community is plagued by a lack of benchmarks to facilitate research and experimentation. For pre-silicon tool development, most researchers rely on common sets such as the ISCAS (‘85, ’89, ’99) and OpenCores benchmarks [118]. Although these have varying degrees of complexity, the available designs do not accurately capture the entire space of today’s IC industry. Companies are particularly hesitant to make even their most outdated designs available due to confidentiality of IPs. The result is a dissonance between academic research and industrial development, which is even more problematic for AI-based EDA. To develop effective AI/ML models, vast amounts of quality data are required. This requires a concerted effort from industry giants, irrespective of their own internal research and development investments.

Hardware security-focused benchmarks like the ones available on Trust-Hub seek to push research in the field. This online resource provides a few hundred examples of board-level Trojans [100], chip-level Trojans [217, 225], and obfuscation [16] benchmarks. Without benchmark generation tools, the samples become tedious to create. It is imperative that such tools are developed and made open source, especially for AI training and validation that require large datasets. For this, Amir and Forte [15] propose a technique that leverages linear optimization to generate synthetic combinational benchmarks that are adaptable to user input constraints and structurally different from input reference benchmarks. This can be viewed as a form of data augmentation to increase variation of features seen by AI/ML/DL algorithms, which should make them learn better and avoid overfitting. Similarly, behavioral models of common analog circuits can act as benchmarks for analog ICs that designers can easily evaluate and integrate security-related constraints and metrics within those models.

5.1.2 Standardized Domain Knowledge. As the academic community needs vast amounts of data, researchers also need standardized domain knowledge. Domain knowledge helps standardize data collection processes so that data collected from different labs is consistent. It also guides researchers to identify relevant features for their specific applications; such prior knowledge means more informed feature selection and dimensionality reduction. Both allow practitioners to reduce the number of features in a dataset by only focusing on important ones. The EDA pipeline produces reports and tunable parameters that may be useful to a model. Without that distinction, an ML model may not achieve its improved automation and efficiency goals. The general benefits include requiring less data for high-accuracy models, creating more robust models, and utilizing interpretable features that help advance XAI in EDA.

5.1.3 Open-Source EDA Tools and PDKs. As this survey demonstrates, designing ICs requires many stages; IP cores must be verified and tested for synthesis to different FPGA architectures and various standard cell libraries. Tools like ones available on OpenCores.org are suitable for less complex demands and foster collaboration among users. However, they are not industry standard,
hence they differ in functionality from commercial tools provided by Synopsys, Cadence, and Xilinx. They are also less reliable and may have trouble scaling up to modern designs.

Some tools have been provided through extensive research within the academic and industrial communities. The OpenROAD initiative seeks to reduce effort, cost, and time for hardware designs by providing 24-hour layout implementation [6]. Their GitHub repository also allows designers with available PDKs to add to the ones available. Similarly, the ALIGN initiative consists of a joint academic/industry team to develop open-source software for analog/mixed-signal circuit layout to translate a netlist into a physical layout, with 24-hour turnaround and no human in the loop [135]. The development of more security-aware designs needs a similar effort from interested parties. With the same emphasis on automation, AI/ML requires working EDA tools to build from.

5.2 Advanced AI Techniques to Explore and Benefits

5.2.1 Transfer Learning. TL is built on the knowledge of previously learned tasks; the knowledge gained from solving one ML problem can be used to address another one (Figure 19). The benefits of utilizing TL are faster training times, increased accuracy, and eliminating the need for large amounts of data. Pan and Yang [189] use domain, task, and marginal probabilities to describe TL. Take a domain \( D \), a two-element tuple with feature space \( \chi \), and marginal probability \( P(X) \). \( X \) is a sample data point, and the entire domain is represented as

\[
D = \{\chi, P(X)\}. \tag{1}
\]

Now consider a task \( T \), another two-element tuple of label space \( \gamma \) and predictive function \( \eta \). The objective function can be denoted as \( P(\gamma|X) \). In addition, \( Y \) is a corresponding label point for \( X \). Therefore,

\[
T = \{\gamma, P(Y|X) \} = \{\gamma, \eta\}. \tag{2}
\]

A source domain can be represented as \( D_s \), a source task as \( T_s \), a target domain as \( D_t \), and a target task as \( T_t \). Hence, the aim of TL is to learn the target conditional probability function \( \eta_t \) or \( P(Y_t|X_t) \) in \( D_t \) with information gained from \( D_s \) and \( T_s \).

TL is ideal for applications within the IC design domain because general design rules are used globally. Design libraries and technology nodes may differ, but pre-trained DL models can be applied to various optimization and security-aware problems. This is especially the case in analog IP design where the lack of portability and reusability across different circuits, design stages, and technology nodes has acted as impediments to the advancement of analog EDA tools. TL has become common in the community for its ability to help train models and quickly deploy models in applications where data is not readily available, as is often the case in the hardware assurance domain.

5.2.2 FL for Collaboration without Hardware IP Compromise. FL or collaborative learning involves training an algorithm in a decentralized manner across multiple edge devices or servers,
which each possess their own local data. FL, first coined by McMahan and Ramage [175], combines ML with edge computing for training (and data collection). Each endpoint, a low-powered computation device, has a copy of the model, improves the model locally, summarizes changes, and sends the updates to the cloud where the global model is updated, updates are then aggregated in the cloud, and updates are sent back to edge devices. Li et al. [144] summarize the problem as follows:

$$\min_w F(w), \text{ where } F(w) \coloneqq \sum_k p_k F_k(w),$$

(3)

where $N$ is the number of total devices, $p_k \in [0, 1]$, and $\sum_k p_k = 1$; $F_k$ is the local objective function for the $k$th device.

Ideally, FL allows for smarter models, reduced latency, and power consumption, all while securing privacy [175]. Distributed data resources also eliminate the need for a central massive data store.

A limiting factor for AI-based IC design is the confidentiality of IPs. Large datasets are required from many existing AI-based design approaches as well as updates over those designs to generate labels. However, companies and governments are typically reluctant to share their IPs, which might include proprietary algorithms, novel design techniques, or in-house countermeasures. The lack of data stifles any one organization’s ability to build sufficient datasets and robust models. For instance, a single company’s data might provide a lot of data on a particular corner case or vulnerability but have little or no data on others, resulting in class imbalance. One solution to this data sharing problem is differential privacy based FL, which allows datasets to be computed over at each edge point without compromising IP. Note, however, that for hardware security applications, this architecture may only be meaningful for cases where the model provides benefits to all participating organizations, such as piracy detection [275] and security rule checks [269].

5.2.3 XAI and Engineer Education. XAI is a field of AI concerned with making ML models understandable by humans. For perspective, take an ANN and attempts to understand the decisions it makes. ANNs are opaque (a.k.a. black-box) predictors, and their experimental performance is largely due to their large parametric space, efficient learning algorithms, and computation advances in hardware. Transparent (a.k.a. white-box) models expose directly how the model/ mechanism works. Decision tree models (and other rule-based models) are largely considered an example of an easily interpretable model for both local and global explanations. Other transparent models include k-nearest neighbors, generative additive models, and Bayesian models [25].

Due to their successes, ANNs are increasingly being deployed for high-stakes decision making. The opaque nature of ANNs raises critical issues because without an understanding of how the mechanism is predicting, there is no way of justifying the rationale behind any prediction. The complex latent manifolds within which ANNs operate are difficult to visualize and reason around. Further complicating things, explainability is defined not only by the details and reasons behind its processes but also the audience doing the observing [25]. Essentially, explanation methods are intended to be a useful interface/translation between a complex model and a stakeholder.

A variety of post hoc methods that attempt to explain opaque predictors have been proposed that can be broadly characterized into model-agnostic and model-specific techniques. Explainers can be considered global (a.k.a. the model explanation problem) or local (a.k.a. the prediction explanation problem). Global explainers attempt to approximate the original model but also remain understandable. Often, global explanation approaches represent the final explanation as a decision tree. Local explanations focus on creating explanations for a particular input—that is, for a given input, explain a specific prediction. In the model-agnostic case, this often results in explanations
Fig. 20. Examples illustrating how small perturbations in input do not change predictions but create very different attribution maps. Reprinted from the work of Ghorbani et al. [83].

that quantify the contribution of each feature to the prediction. However, explainers themselves tend to be fragile. As shown in Figure 20, explanations can vary widely due to small changes in the input. Or more problematically, they can be equivalent for very different predictions. The landscape of XAI is still evolving, and there is much work still needed to be done. Explanation tooling can provide some guidance as to “where the model is looking,” but there is also a need for designing interpretable models [215].

In the semiconductor industry, many design engineers do not have the experience and background to deal with hardware security issues. Even those that do may have very specialized experience, such as experts in applied cryptography but novices in supply chain security. Further, security is a domain in a constant state of flux with new attack vectors popping up each year. XAI is an important research area and could provide feedback to organizations and help them train or retrain their design engineers to keep up with new attacks and vulnerabilities. The lessons learned from XAI both in its limitations and possibilities can provide useful insight to the appropriate application, or more importantly interpretation, of ML models in security applications.

6 CONCLUSION

In this survey, we summarized the state-of-the-art AI/ML-based EDA techniques, as well as their contemporary and potential use in security-aware design, and provide a general perspective on needs and requirements for an automated security-aware IC design process. Our literature review showed that ML/AI is remarkably suitable for tuning the design to incorporate security constraints without deteriorating performance, develop reliable and robust security primitives to tackle supply chain related vulnerabilities, and make the designs more resilient against both invasive and non-invasive, side-channel, and fault-injection attacks. In that regard, we have extensively covered the intersection between learning and design with the objective of protecting electronic systems against malicious parties, whether it be by AI-based integration of multiple primitives and protections, guidance and optimization of design tradeoffs, or real-time feedback/training for users. We also discussed problems and solutions within this domain, such as scarcity of data, confidentiality, and open-source tools, and highlighted opportunities that will make the AI-based design more formidable and help solidify hardware as the root of trust for industry and government.

REFERENCES

[1] Victoria Fraza Kickham. 2012. Top 5 Most Counterfeited Parts Represent a 169 Billion Potential Challenge for Global Semiconductor Market. Retrieved September 20, 2022 from https://www.electronicdesign.com/21194728.
[2] Martin Abadi, Ashish Agarwal, Paul Barham, Eugene Brevdo, Zhifeng Chen, Craig Citro, Greg S. Corrado, et al. 2015. TensorFlow: Large-Scale Machine Learning on Heterogeneous Systems. Retrieved September 20, 2022 from https://www.tensorflow.org/.

[3] Rabin Yu Acharya, Sreeja Chowdhury, Fatemeh Ganji, and Domenic Forte. 2020. Attack of the genes: Finding keys and parameters of locked analog ICs using genetic algorithm. In Proceedings of the 2020 IEEE International Symposium on Hardware Oriented Security and Trust (HOST'20). IEEE, Los Alamitos, CA, 284–294.

[4] Rabin Yu Acharya, Michael Valentin Levin, and Domenic Forte. 2021. LDO-based odometer to combat IC recycling. In Proceedings of the 2021 IEEE 34th International System-on-Chip Conference (SOCC’21). IEEE, Los Alamitos, CA, 206–211.

[5] Ali Ahmadi, Mohammad-Mahdi Bidmeshki, Amit Nahar, Bob Orr, Michael Pas, and Yiorgos Makris. 2016. A machine learning approach to fab-of-origin attestation. In Proceedings of the 35th International Conference on Computer-Aided Design. 1–6.

[6] Tutu Ajayi, David Blaauw, Tuck-Boon Chan, C.-K. Cheng, Viren Chhabria, D. K. Choo, M. Coltella, et al. 2019. OpenROAD: Toward a self-driving, open-source digital layout implementation tool chain. In Proceedings of the Government Microcircuit Applications and Critical Technology Conference. 1105–1110.

[7] Mahbub Alam, Sreeja Chowdhury, Beomsoo Park, David Munzer, Nima Maghari, Mark Tehranipoor, and Domenic Forte. 2018. Challenges and opportunities in analog and mixed-signal (AMS) integrated circuit (IC) security. Journal of Hardware and Systems Security 2, 1 (2018), 15–32.

[8] Mahbub Alam, Shahin Tajik, Fatemeh Ganji, Mark Tehranipoor, and Domenic Forte. 2019. RAM-Jam: Remote temperature and voltage fault attack on FPGAs using memory collisions. In Proceedings of the 2019 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC’19). IEEE, Los Alamitos, CA, 48–55.

[9] Abdulrahman Alaql and Swarup Bhunia. 2021. SARO: Scalable attack-resistant logic locking. IEEE Transactions on Information Forensics and Security 16 (2021), 3724–3739.

[10] Abdulrahman Alaql, Saranyu Chattopadhayay, Prabuddha Chakraborty, Tamzidul Hoque, and Swarup Bhunia. 2021. LeGo: A learning-guided obfuscation framework for hardware IP protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 41, 4 (2021), 854–867. https://doi.org/10.1109/TCAD.2021.3075939

[11] Yousra Alkabani and Farinaz Koushanfar. 2007. Active hardware metering for intellectual property protection and security. In Proceedings of the USENIX Security Symposium, Vol. 20. 1–20.

[12] Ethem Alpaydin. 2020. Introduction to Machine Learning. MIT Press, Cambridge, MA.

[13] Uthman Alsaiari and Fayez Gebali. 2019. Hardware Trojan detection using reconfigurable assertion checkers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 27, 7 (2019), 1575–1586. https://doi.org/10.1109/TVLSI.2019.2908964

[14] Anastacia Alvarez, Wenfeng Zhao, and Massimo Alioto. 2015. 14.3 15fJ/b static physically unclonable functions for secure chip identification with <2% native bit instability and 140× Inter/Intra PUF Hamming distance separation in 65nm. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference (ISSCC’15) Digest of Technical Papers. IEEE, Los Alamitos, CA, 1–3.

[15] Sarah Amir and Domenic Forte. 2020. Adaptable and divergent synthetic benchmark generation for hardware security. In Proceedings of the 39th International Conference on Computer-Aided Design. 1–9.

[16] Sarah Amir, Bicky Shaky, Xiaolin Xu, Yier Jin, Swarup Bhunia, Mark Tehranipoor, and Domenic Forte. 2018. Development and evaluation of hardware obfuscation benchmarks. Journal of Hardware and Systems Security 2, 2 (2018), 142–161.

[17] Armaiti Ardestirecham, Wei Hu, Joshua Marxen, and Ryan Kastner. 2017. Register transfer level information flow tracking for provably secure hardware design. In Proceedings of the Design, Automation, and Test in Europe Conference and Exhibition (DATE). 1691–1696. https://doi.org/10.23919/DATE.2017.7927266

[18] Victor Arribas, Svetla Nikova, and Vincent Rijmen. 2018. VerMI: Verification tool for masked implementations. In Proceedings of the 2018 25th IEEE International Conference on Electronics, Circuits, and Systems (ICECS’18). IEEE, Los Alamitos, CA, 381–384.

[19] Kimia Zamiri Azar, Muhammad Monir Hossain, Arash Vafaei, Hasan Al Shaikh, Nurun N. Mondol, Fahim Rahman, Mark Tehranipoor, and Farimah Farahmandi. 2022. Fuzz, penetration, and AI testing for soc security verification: Challenges and solutions. Cryptology ePrint Archive 2022 (2022), 1–22.

[20] Pietro Babighian, Luca Benini, Alberto Macii, and Enrico Macii. 2004. Post-layout leakage power minimization based on distributed sleep transistor insertion. In Proceedings of the 2004 International Symposium on Low Power Electronics and Design (ISLPED ‘04). ACM, New York, NY, 138–143. https://doi.org/10.1145/1013235.1013275

[21] Alessandra Bagnato, Leandro Soares Indrusiak, Imran Rafiq Quadri, and Matteo Rossi. 2014. Handbook of Research on Embedded Systems Design. Information Science Reference.

[22] Vitor Bandeira, Mateus Fogaça, Eder Matheus Monteiro, Isadora Oliveira, Mingyu Woo, and Ricardo Reis. 2020. Fast and scalable I/O pin assignment with divide-and-conquer and hungarian matching. In Proceedings of the 2020 18th
A Survey and Perspective on AI for Security-Aware EDA

IEEE International New Circuits and Systems Conference (NEWCAS’20). 74–77. https://doi.org/10.1109/NEWCAS49341.2020.9159791

[23] Hagai Bar-El, Hamid Choukri, David Naccache, Michael Tunstall, and Claire Whelan. 2006. The sorcerer’s apprentice guide to fault attacks. *Proceedings of the IEEE* 94, 2 (2006), 370–382.

[24] Erick Carvajal Barboza, Nishchal Shukla, Yiran Chen, and Jiang Hu. 2019. Machine learning-based pre-routing timing prediction with reduced pessimism. In *Proceedings of the 56th Annual Design Automation Conference (DAC’19)*. ACM, New York, NY, Article 16, 6 pages. https://doi.org/10.1145/3316781.3317857

[25] Alejandro Barroso Arrieta, Natalia Diaz-Rodriguez, Javier Del Ser, Adrien Bennetot, Siham Tabik, Alberto Barbado, Salvador Garcia, et al. 2020. Explainable artificial intelligence (XAI): Concepts, taxonomies, opportunities and challenges toward responsible AI. *Information Fusion* 56 (June 2020), 82–115. https://doi.org/10.1016/j.inffus.2019.12.012

[26] Gilles Barthe, Sonia Belaïd, François Dupressoir, Pierre-Alain Fouque, Benjamin Grégoire, and Pierre-Yves Strub. 2015. Verified proofs of higher-order masking. In *Proceedings of the Annual International Conference on the Theory and Applications of Cryptographic Techniques*. 457–485.

[27] Macy Bayern, Bill Detwiler, TechRepublic Academy, Erik Eckel, and Jack Wallen. 2019. 63% of organizations face security breaches due to hardware vulnerabilities. *TechRepublic*. Retrieved September 20, 2022 from https://www.techrepublic.com/article/63-of-organizations-face-security-breaches-due-to-hardware-vulnerabilities/.

[28] Guido Bertoni, Marco Martinoli, and Maria Chiara Molteni. 2017. A methodology for the characterisation of leakages in combinatorial logic. *Journal of Hardware and Systems Security* 1, 3 (2017), 269–281.

[29] Jitendra Bhandari, Abdul Khader Thalakkattu Moosa, Benjamin Tan, Christian Pilato, Ganesh Gore, Xifan Tang, Scott Temple, Pierre-Emmanuel Gaillardron, and Ramesh Karri. 2021. Exploring eFPGA-based redaction for IP protection. In *Proceedings of the 2021 IEEE/ACM International Conference on Computer Aided Design (ICCAD’21)*. 1–9. https://doi.org/10.1109/ICCAD51958.2021.9643548

[30] Veepsa Bhatia, Neeta Pandey, and Asok Bhattacharyya. 2016. Modelling and design of inverter threshold quantization based current comparator using artificial neural networks. *International Journal of Electrical & Computer Engineering* 6, 1 (2016), 320.

[31] D. Binu and B. S. Kariyappa. 2018. RideNN: A new rider optimization algorithm-based neural network for fault diagnosis in analog circuits. *IEEE Transactions on Instrumentation and Measurement* 68, 1 (2018), 2–26.

[32] Roderick Bloem, Hannes Groß, Rinat Iusupov, Bettina Könighofer, Stefan Mangard, and Johannes Winter. 2018. Formal verification of masked hardware implementations in the presence of glitches. In *Proceedings of the Annual International Conference on the Theory and Applications of Cryptographic Techniques*. 321–353.

[33] J. Bogaerts. 2014. Complementary metal-oxide-semiconductor (CMOS) image sensors for use in space. In *High Performance Silicon Imaging*, Daniel Durini (Ed.). Woodhead Publishing, 250–280. https://doi.org/10.1533/9780857097521.2.250

[34] R. K. Brayton, G. D. Hachtel, and A. L. Sangiovanni-Vincentelli. 1990. Multilevel logic synthesis. *Proceedings of the IEEE* 78, 2 (1990), 264–300. https://doi.org/10.1109/5.52213

[35] Michael M. Bronstein, Joan Bruna, Yann LeCun, Arthur Szlam, and Pierre Vandergheynst. 2017. Geometric deep learning: Going beyond Euclidean data. *IEEE Signal Processing Magazine* 34, 4 (July 2017), 18–42. https://doi.org/10.1109/MSP.2017.2693418

[36] Ileana Buhan, Lejla Batina, Yuval Yarom, and Patrick Schaumont. 2021. SoK: Design tools for side-channel-aware implementations. arXiv:cs.CR/2104.08593.

[37] Michael Bushnell and Vishwani Agrawal. 2004. *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Vol. 17. Springer Science & Business Media.

[38] João M. P. Cardoso, José Gabriel F. Coutinho, and Pedro C. Diniz. 2017. Source code analysis and instrumentation. In *Embedded Computing for High Performance*, João M. P. Cardoso, José Gabriel F. Coutinho, and Pedro C. Diniz (Eds.). Morgan Kaufmann, Boston, MA, 99–135. https://doi.org/10.1007/978-0-12-804189-5_00004-1

[39] M. Cassel and F. Lima. 2006. Evaluating one-hot encoding finite state machines for SEU reliability in SRAM-based FPGAs. In *Proceedings of the 12th IEEE International On-Line Testing Symposium (IOLTS’06)*. 6. https://doi.org/10.1109/IOLTS.2006.32

[40] Matthew James Casto. 2018. *Multi-Attribute Design for Authentication and Reliability (MADAR)*. Ph.D. Dissertation. Ohio State University.

[41] Prabuddha Chakraborty, Jonathan Cruz, and Swarup Bhunia. 2018. SAIL: Machine learning guided structural analysis attack on hardware obfuscation. In *Proceedings of the 2018 Asian Hardware Oriented Security and Trust Symposium (AsianHOST’18)*. IEEE, Los Alamitos, CA, 56–61.

[42] Rajat Subhra Chakraborty and Swarup Bhunia. 2009. HARPOON: An obfuscation-based SoC design methodology for hardware protection. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 28, 10 (2009), 1493–1502.
[43] Rajat Subhra Chakraborty and Swarup Bhunia. 2010. RTL hardware IP protection using key-based control and data flow obfuscation. In Proceedings of the 2010 23rd International Conference on VLSI Design. 405–410. https://doi.org/10.4108/VLSIDesign.2010.54

[44] Chip-Hong Chang, Miodrag Potkonjak, and Li Zhang. 2016. Hardware IP Watermarking and Fingerprinting. Springer International Publishing, Cham, Switzerland, 329–368. https://doi.org/10.1007/978-3-319-14971-4_10

[45] Doohwang Chang, Sule Ovez, Ozgur Sinanoglu, and Ramesh Karri. 2014. Approximating the age of RE/analog circuits through re-characterization and statistical estimation. In Proceedings of the 2014 Design, Automation, and Test in Europe Conference and Exhibition (DATE’14). IEEE, Los Alamitos, CA, 1–4.

[46] Po-Hao Chang, Jia-Ming Chen, and Chao-Ying Shen. 2006. On an efficient closed form expression to estimate the crosstalk noise in the circuit with multiple wires. In Proceedings of the 2006 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS’06). 1329–1332. https://doi.org/10.1109/APCCAS.2006.342429

[47] Huili Chen, Cheng Fu, Jishen Zhao, and Farinaz Koushanfar. 2019. GenUnlock: An automated genetic algorithm framework for unlocking logic encryption. In Proceedings of the 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’19). 1–8. https://doi.org/10.1109/ICCAD45719.2019.8942134

[48] Hao Chen, Mingjie Liu, Biying Xu, Keren Zhu, Xiuyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan. 2020. MAGICAL: An open-source fully automated analog IC layout system from netlist to GDSII. IEEE Design & Test 38, 2 (2020), 19–26.

[49] Zhiqian Chen, Gaurav Kolhe, Setareh Rafatirad, Chang-Tien Lu, Sai Manoj, Houman Homayoun, and Liang Zhao. 2020. Estimating the circuit de-obfuscation runtime based on graph deep learning. In Proceedings of the 2020 Design, Automation, and Test in Europe Conference and Exhibition (DATE’20). 358–363. https://doi.org/10.23919/DATEN48585.2020.9116544

[50] Zaichen Chen, Maxim Raginsky, and Elyse Rosenbaum. 2017. Verilog—A compatible recurrent neural network model for transient circuit simulation. In Proceedings of the 2017 IEEE 26th Workshop on Electronic Packaging and Systems (EPEPS’17). IEEE, Los Alamitos, CA, 1–3.

[51] Lap Wai Chow, James P. Baukus, Bryan J. Wang, and Ronald P. Cocchi. 2012. Camouflaging a standard cell based integrated circuit. US Patent 8,151,235, April 3, 2012.

[52] Sreeja Chowdhury, Rabin Acharya, William Boullion, Andrew Felder, Mark Howard, Jia Di, and Domenic Forte. 2020. A weak asynchronous REset (ARES) PUF using start-up characteristics of null conventional logic gates. In Proceedings of the 2020 IEEE International Test Conference (ITC’20). IEEE, Los Alamitos, CA, 1–10.

[53] Sreeja Chowdhury, Fatehme Ganji, and Domenic Forte. 2020. Low-cost remarked counterfeit IC detection using LDO regulators. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems (ISCAS’20). IEEE, Los Alamitos, CA, 1–5.

[54] Sreeja Chowdhury, Fatehme Ganji, and Domenic Forte. 2020. Recycled SoC detection using LDO degradation. SN Computer Science 1, 6 (2020), 1–21.

[55] R. C. Cofer and Benjamin F. Harding. 2006. Design constraints and optimization. In Rapid System Prototyping with FPGAs, R. C. Cofer and Benjamin F. Harding (Eds.). Newnes, Burlington, MA, 137–154. https://doi.org/10.1016/B978-075067866-7/50010-X

[56] Jason Cong, Bin Liu, Stephen Neuendorffer, Juanjo Noguera, Kees Vissers, and Zhiru Zhang. 2011. High-level synthesis for FPGAs: From prototyping to deployment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 30, 4 (2011), 473–491. https://doi.org/10.1109/TCAD.2011.2110592

[57] Katherine Connor. 2018. UC San Diego selected to lead development of open-source tools for hardware design automation. UC San Diego Today. https://ucsdnews.ucsd.edu/pressrelease/uc_san_diego_selected_to_lead_development_of_open_source_tools_forハードwear_design_automation

[58] Gustavo K. Contreras, Tauhidur Rahman, and Mohammad Tehranipoor. 2013. Secure split-test for preventing IC piracy by untrusted foundry and assembly. In Proceedings of the 2013 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS’13). 196–203. https://doi.org/10.1109/DFT.2013.6653606

[59] Theodore W. Cornforth and Hod Lipson. 2014. Reverse-engineering nonlinear analog circuits with evolutionary computation. In Proceedings of the International Conference on Unconventional Computation and Natural Computation. 105–116.

[60] Jean-Sebastien Coron. 2018. Formal verification of side-channel countermeasures via elementary circuit transformations. In Proceedings of the International Conference on Applied Cryptography and Network Security. 65–82.

[61] Jonathan Cruz, Farimah Farahmandi, Alif Ahmed, and Prabhat Mishra. 2018. Hardware Trojan detection using ATPG and model checking. In Proceedings of the 2018 31st International Conference on VLSI Design and the 2018 17th International Conference on Embedded Systems (VLSID’18). 91–96. https://doi.org/10.1109/VLSID.2018.43
Proceedings of the 26th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM'18). 129–132. https://doi.org/10.1109/FCCM.2018.00029

Angan Das and Ranga Vemuri. 2007. An automated passive analog circuit synthesis framework using genetic algorithms. In Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI’07). IEEE, Los Alamitos, CA, 145–152.

Lauren De Meyer, Victor Arribas Abril, Sveta Nikola, Ventzislav Nikol, and Vincent Rijmen. 2018. M&M: Masks and MACS against physical attacks. IACR Transactions on Cryptographic Hardware and Embedded Systems 2019, 1 (2018), 25–50.

Duo Ding, Jhui-Rong Gao, Kun Yuan, and David Z. Pan. 2011. AENEID: A generic lithography-friendly detailed router based on post-RET data learning and hotspot detection. In Proceedings of the 48th Design Automation Conference (DAC’11). 795–800.

Mengmeng Ding and R. I. Vemuri. 2005. An active learning scheme using support vector machines for analog circuit feasibility classification. In Proceedings of the 18th International Conference on VLSI Design Held Jointly with the 4th International Conference on Embedded Systems Design. IEEE, Los Alamitos, CA, 528–534.

S. Docking and M. Sachdev. 2003. A method to derive an equation for the oscillation frequency of a ring oscillator. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications 50, 2 (2003), 259–264. https://doi.org/10.1109/TCSI.2002.808235

Etienne Dumesnil, Frederic Nabki, and Mounir Boukadoum. 2014. RF-LNA circuit synthesis by genetic algorithm-specified artificial neural network. In Proceedings of the 2014 21st IEEE International Conference on Electronics, Circuits, and Systems (ICECS’14). IEEE, Los Alamitos, CA, 758–761.

Etienne Dumesnil, Frederic Nabki, and Mounir Boukadoum. 2015. RF-LNA circuit synthesis using an array of artificial neural networks with constrained inputs. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS’15). IEEE, Los Alamitos, CA, 573–576.

Carson Dunbar and Gang Qu. 2015. Satisfiability Don’t Care condition based circuit fingerprinting techniques. In Proceedings of the 20th Asia and South Pacific Design Automation Conference. 815–820.

IBM Cloud Education. n.d. What Is Deep Learning? Retrieved September 20, 2022 from https://www.ibm.com/cloud/learn/deep-learning.

Mohamed El Massad, Siddharth Garg, and Mahesh V. Tripunitara. 2015. Integrated circuit (IC) decamouflaging: Reverse engineering camouflaged ICs within minutes. In Proceedings of the 2015 Network and Distributed System Security Symposium (NDSS’15). 1–14.

Mohamed Elshamy, Giorgio Di Natale, Antonios Pavlidis, Marie-Minerve Louérat, and Haralampous-G. Stratigopoulos. 2020. Hardware Trojan attacks in analog/mixed-signal ICs via the test access mechanism. In Proceedings of the 2020 IEEE European Test Symposium (ETS’20). IEEE, Los Alamitos, CA, 1–6.

Mateus Fogaça, Andrew B. Kahng, Ricardo Reis, and Lutong Wang. 2019. Finding placement-relevant clusters with fast modularity-based clustering. In Proceedings of the 24th Asia and South Pacific Design Automation Conference. 569–576.

Jens Froemmer, Yara Gowayed, Nico Bannow, Wolfgang Kunz, Christoph Grimm, and Klaus Schneider. 2020. Area estimation framework for digital hardware design using machine learning. In Proceedings of Methods and Description Languages for Modelling and Verification of Circuits and Systems; GMM/ITG/GI-Workshop (MBMV’20). 1–10.

Jason Fung. 2022. 7 essentials for more security-aware design automation. DAKReading. Retrieved September 20, 2022 from https://www.darkreading.com/vulnerabilities-threats/7-essentials-for-more-security-aware-design-automation.

Christian Gabriel, Christoffer Wittmann, Denis Sych, Rufang Dong, Wolfgang Mauerer, Ulrik L. Andersen, Christoph Marquardt, and Gerd Leuchs. 2010. A generator for unique quantum random numbers based on vacuum states. Nature Photonics 4, 10 (2010), 711–715. https://doi.org/10.1038/n photon.2010.197

Minyan Gao, Huanyu Wang, Mark M. Tehranipoor, and Domenic Forte. 2020 iPROBE V2: Internal shielding-based countermeasures against both back-side and front-side probing attacks. SRC TECHCON/2020 (2020), Article 10174121. https://par.nsf.gov/biblio/10174121.

Zhengqi Gao, Jun Tao, Fan Yang, Yangfeng Su, Dian Zhou, and Xuan Zeng. 2019. Efficient performance trade-off modeling for analog circuit based on Bayesian neural network. In Proceedings of the 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’19). IEEE, Los Alamitos, CA, 1–8.

Blaise Gassend, Dwaine Clarke, Marten Van Dijk, and Srinivas Devadas. 2002. Silicon physical random functions. In Proceedings of the 9th ACM Conference on Computer and Communications Security. 148–160.
[83] Amirata Ghorbani, Abubakar Abid, and James Zou. 2019. Interpretation of neural networks is fragile. AAAI 33, 1 (July 2019), 3681–3688. https://doi.org/10.1609/aaai.v33i01.33013681
[84] Georges G. E. Gielen and Rob A. Rutenbar. 2000. Computer-aided design of analog and mixed-signal integrated circuits. Proceedings of the IEEE 88, 12 (2000), 1825–1854.
[85] Christophte Giraud and Adrian Thilllard. 2010. Piret and quisquater’s DFA on AES revisited. IACR Cryptology ePrint Archive 2010 (2010), 440.
[86] Anna Goldie and Azalia Mirhoseini. 2020. Placement optimization with deep reinforcement learning. In Proceedings of the 2020 International Symposium on Physical Design. 3–7.
[87] Martin Grabmann, Frank Feldhoff, and Georg Gläser. 2019. Power to the model: Generating energy-aware mixed-signal models using machine learning. In Proceedings of the 2019 16th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’19). IEEE, Los Alamitos, CA, 5–8.
[88] L. Green. 1999. Understanding the importance of signal integrity. IEEE Circuits and Devices Magazine 15, 6 (1999), 7–10. https://doi.org/10.1109/108850
[89] Zhibin Guan, Xiaomeng Wang, Wei Xin, Jiajie Wang, and Li Zhang. 2020. A survey on deep learning-based source code defect analysis. In Proceedings of the 2020 5th International Conference on Computer and Communication Systems (ICCCS’20). IEEE, Los Alamitos, CA, 167–171.
[90] Daniel Guerra, António Canelas, Ricardo Póvoa, Nuno Horta, Nuno Lourenço, and Ricardo Martins. 2019. Artificial neural networks as an alternative for automatic analog IC placement. In Proceedings of the 2019 16th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’19). IEEE, Los Alamitos, CA, 1–4.
[91] Ujjwal Guin, Domenic Forte, and Mark Tehranipoor. 2015. Design of accurate low-cost on-chip structures for protecting integrated circuits against recycling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24, 4 (2015), 1233–1246.
[92] Ujjwal Guin, Xuehui Zhang, Domenic Forte, and Mohammad Tehranipoor. 2014. Low-cost on-chip structures for combating die and IC recycling. In Proceedings of the 2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC’14). 1–6. https://doi.org/10.1145/2593069.2593157
[93] Nithyashankari Gummidipoondi Jayasankaran, Adriana Sanabria Borbon, Edgar Sanchez Sinencio, Jiang Hu, and Jeyavijayan Rajendran. 2022. Towards provably-secure analog and mixed-signal locking against overproduction. IEEE Transactions on Emerging Topics in Computing 10, 1 (2022), 386–403.
[94] António Gusmão, Fábio Passos, Ricardo Póvoa, Nuno Horta, Nuno Lourenço, and Ricardo Martins. 2020. Semi-supervised artificial neural networks towards analog IC placement recommender. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems (ISCAS’20). IEEE, Los Alamitos, CA, 1–5.
[95] Winston Haaswijk, Edo Collins, Benoît Seguin, Mathias Soeken, Frédéric Kaplan, Sabine Süssstrunk, and Giovanni De Micheli. 2018. Deep learning for logic optimization algorithms. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS’18). 1–4. https://doi.org/10.1109/ISCAS.2018.8351885
[96] Kourosh Hakhamaneshi, Nick Werblun, Pieter Abbeel, and Vladimir Stojanović. 2019. BagNet: Berkeley analog generator with layout optimizer boosted with deep neural networks. In Proceedings of the 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’19). IEEE, Los Alamitos, CA, 1–8.
[97] William L. Hamilton. 2020. Graph representation learning. Proceedings of the 2020 International Symposium on Circuits and Systems (ISCAS’20). IEEE, Los Alamitos, CA, 5–8.
[98] Kwangsoo Han, Andrew B. Kahng, and Jiajia Li. 2020. Optimal generalized H-tree topology and buffering for high-performance and low-power clock distribution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 39 (2020), 478–491.
[99] Samer S. Hanna and Danijela Cabric. 2019. Deep learning based transmitter identification using power amplifier nonlinearity. In Proceedings of the 2019 International Conference on Computing, Networking, and Communications (ICNC’19). IEEE, Los Alamitos, CA, 674–680.
[100] Jacob Harrison, Navid Asadizanjani, and Mark Tehranipoor. 2021. On malicious implants in PCBs throughout the supply chain. Integration 79 (2021), 12–22. https://doi.org/10.1016/j.ivlsi.2021.03.002
[101] M. V. Harsha and B. P. Harish. 2018. An integrated maxFit genetic algorithm-SPICE framework for 2-stage op-amp design automation. In Proceedings of the 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI’18). IEEE, Los Alamitos, CA, 170–174.
[102] Peter E. Hart, Nils J. Nilsson, and Bertram Raphael. 1968. A formal basis for the heuristic determination of minimum cost paths. IEEE Transactions on Systems Science and Cybernetics 4, 2 (1968), 100–107.
[103] Ramin M. Hasani, Dieter Haerle, Christian F. Baumgartner, Alessio R. Lomuscio, and Radu Grosu. 2017. Compositional neural-network modeling of complex analog circuits. In Proceedings of the 2017 International Joint Conference on Neural Networks (IJCNN’17). IEEE, Los Alamitos, CA, 2235–2242.
[104] Charles Herder, Meng-Day Yu, Farinaz Koushanfar, and Srinivas Devadas. 2014. Physical unclonable functions and applications: A tutorial. Proceedings of the IEEE 102, 8 (2014), 1126–1141. https://doi.org/10.1109/JPROC.2014.2320516

[105] Matthias Hiller, Ludwig Kürzinger, and Georg Sigl. 2020. Review of error correction for PUFs and evaluation on state-of-the-art FPGAs. Journal of Cryptographic Engineering 10, 3 (2020), 229–247.

[106] Michael S. Hsiao. 2006. Test generation. In VLSI Test Principles and Architectures, Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen (Eds.). Morgan Kaufmann, San Francisco, CA, 161–262. https://doi.org/10.1016/B978-012370597-6/50008-1

[107] Wei Hu, Armaitt Ardestiricham, and Ryan Kastner. 2021. Hardware information flow tracking. ACM Computing Surveys 54, 4 (May 2021), Article 4, 39 pages. https://doi.org/10.1145/3447867

[108] Guyue Huang, Jingbo Hu, Yifan He, Jialong Liu, Mingyuan Ma, Zhayong Shen, Juejian Wu, et al. 2021. Machine learning for electronic design automation: A survey. ACM Transactions on Design Automation of Electronic Systems 26, 5 (2021), 1–46.

[109] Jiangli Huang, Shuhan Zhang, Cong Tao, Fan Yang, Changhao Yan, Dian Zhou, and Xuan Zeng. 2021. Bayesian optimization approach for analog circuit design using multi-task Gaussian process. In Proceedings of the 2021 IEEE International Symposium on Circuits and Systems (ISCAS’21). IEEE, Los Alamitos, CA, 1–5.

[110] Ke Huang, John M. Carulli, and Yiorgos Makris. 2012. Parametric counterfeit IC detection via support vector machines. In Proceedings of the 2012 IEEE International Conference on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT’12). IEEE, Los Alamitos, CA, 7–12.

[111] William Hughes, Sandeep Srinivasan, Rohit Suvarna, and Maithilee Kulkarni. 2019. Optimizing design verification using machine learning: Doing better than random. CoRR abs/1909.13168 (2019).

[112] Sorin A. Huss, Marc Stöttinger, and Michael Zohner. 2013. AMASIVE: An adaptable and modular autonomous side-channel vulnerability evaluation framework. In Number Theory and Cryptography. Springer, 151–165.

[113] Frank Imeson, Ariq Emtenan, Siddharth Garg, and Mahesh Tripunitara. 2013. Securing computer hardware using 3D integrated circuit (IC) technology and split manufacturing for obfuscation. In Proceedings of the 22nd USENIX Security Symposium (USENIX Security’13). 495–510.

[114] Gamze İslamoğlu, Tuğberk Oğulcan Çakici, Engin Afacan, and Günhan Dündar. 2019. Artificial neural network assisted analog IC sizing tool. In Proceedings of the 2019 16th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’19). IEEE, Los Alamitos, CA, 9–12.

[115] Ali Jafari, Saeed Sadri, and Maryam Zekri. 2010. Design optimization of analog integrated circuits by using artificial neural networks. In Proceedings of the 2010 International Conference of Soft Computing and Pattern Recognition. IEEE, Los Alamitos, CA, 385–388.

[116] Nithyashankari Gummipipoondi Jayasankaran, A. Sanabria Borbon, Amr Abuellil, Edgar Sánchez-Sinencio, Jiang Hu, and Jeyavijayan Rajendran. 2019. Breaking analog locking techniques via satisfiability modulo theories. In Proceedings of the 2019 IEEE International Test Conference (ITC’19). IEEE, Los Alamitos, CA, 1–10.

[117] N. G. Jayasankaran, A. Sanabria Borbon, A. Abuellil, E. Sánchez-Sinencio, J. H., and J. Rajendran. 2019. Breaking analog locking techniques via satisfiability modulo theories. In Proceedings of the 2019 IEEE International Test Conference (ITC’19). 1–10. https://doi.org/10.1109/ITC4170.2019.9000113

[118] Maksim Jenihhin. (n.d.) Benchmark Circuits. Retrieved September 20, 2022 from https://pld.ttu.ee/~maksim/benchmarks/.

[119] Jie-Hong (Roland) Jiang and Srinivas Devadas. 2009. Logic synthesis in a nutshell. In Electronic Design Automation, Laung-Terng Wang, Yao-Wen Chang, and Kwang-Ting (Tim) Cheng (Eds.). Morgan Kaufmann, Boston, MA, 299–404. https://doi.org/10.1016/B978-0-12-374364-0.50013-8

[120] Zhenghong Jiang, Steve Dai, G. Edward Suh, and Zhiru Zhang. 2018. High-level synthesis with timing-sensitive information flow enforcement. In Proceedings of the 2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’18). 1–8. https://doi.org/10.1145/3240765.3240813

[121] Sunghyun Jin, Suhi Kim, HeeSeok Kim, and Seokhie Hong. 2020. Recent advances in deep learning-based side-channel analysis. ETRI Journal 42, 2 (2020), 292–304.

[122] Andrew B. Kahng, Ravi Varadarajan, and Zhiang Wang. 2022. RTL-MP: Toward practical, human-quality chip planning and macro placement. In Proceedings of the 2022 International Symposium on Physical Design (ISPD’22). 3–11.

[123] Mark Karpovsky and Alexander Taubin. 2004. New class of nonlinear systematic error detecting codes. IEEE Transactions on Information Theory 50, 8 (2004), 1818–1819.

[124] Ezgi Kaya, Engin Afacan, and Gunhan Dündar. 2018. An analog/RF circuit synthesis and design assistant tool for analog IP: DATA-IP. In Proceedings of the 2018 15th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’18). IEEE, Los Alamitos, CA, 1–9.

[125] Michael Keating and Pierre Bricaud. 2007. Reuse Methodology Manual: For System-on-a-Chip Designs. Springer.

[126] Amir A. Khwaja. 1997. Enhancing extensibility of the design rule checker of an EDA tool by object-oriented modeling. In Proceedings of the 21st International Computer Software and Applications Conference (COMPSAC’97). IEEE, Los Alamitos, CA, 104–108.
[127] Jaehun Kim, Stjepan Picek, Annelie Heuser, Shivam Bhasin, and Alan Hanjalic. 2019. Make some noise: Unleashing the power of convolutional neural networks for profiled side-channel analysis. *IACR Transactions on Cryptographic Hardware and Embedded Systems* 2019 (2019), 148–179.

[128] Minsu Kim, Hyunwook Park, Seongguk Kim, Keeyoung Son, Subin Kim, Kyunjune Son, Seonguk Choi, Gapyeol Park, and Jongho Kim. 2020. Reinforcement learning-based auto-router considering signal integrity. In *Proceedings of the 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS’20)*. IEEE, Los Alamitos, CA, 1–3.

[129] Christian Kison, Omar Mohamed Awad, Marc Fyrbjøk, and Christof Paar. 2019. Security implications of intentional capacitive crosstalk. *IEEE Transactions on Information Forensics and Security* 14, 12 (2019), 3246–3258.

[130] Paul Kocher, Jann Horn, Anders Fogh, Daniel Genkin, Daniel Gruss, Werner Haas, Mike Hamburg, et al. 2019. Spectre attacks: Exploiting speculative execution. In *Proceedings of the 2019 IEEE Symposium on Security and Privacy (SP’19)*. IEEE, Los Alamitos, CA, 1–19.

[131] Gaurav Kolhe, Tyler Sheaves, Kevin Immanuel Gubbi, Soheil Salehi, Setareh Rafatirad, Sai Manoj, Avesta Sasan, and Houman Homayoun. 2022. LOCK&ROLL: Deep-learning power side-channel attack mitigation using emerging reconfigurable devices and logic locking. In *Proceedings of the 59th ACM/IEEE Design Automation Conference (DAC’22)*. ACM, New York, NY, 85–90. https://doi.org/10.1145/3489517.3530414

[132] S. T. Choden Konigsmark, Deming Chen, and Martin D. F. Wong. 2017. High-level synthesis for side-channel defense. In *Proceedings of the 2017 IEEE 28th International Conference on Application-Specific Systems, Architectures, and Processors (ASAP’17)*. 37–44. https://doi.org/10.1109/ASAP.2017.7995257

[133] Thilo Krachenfels, Tuba Kiyani, Shahin Tajik, and Jean-Pierre Seifert. 2021. Automatic extraction of secrets from the transistor jungle using laser-assisted side-channel attacks. In *Proceedings of the 30th USENIX Security Symposium (USENIX Security’21)*. 627–644.

[134] Raghavan Kumar and Wayne Burleson. 2014. On design of a highly secure PUF based on non-linear current mirrors. In *Proceedings of the 2014 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’14)*. IEEE, Los Alamitos, CA, 38–43.

[135] Kishor Kunal, Meghna Madhusudan, Arvind K. Sharma, Wenbin Xu, Steven M. Burns, Ramesh Harjani, Jiang Hu, Desmond A. Kirkpatrick, and Sachin S. Sapatnekar. 2019. ALIGN: Open-source analog layout automation from the ground up. In *Proceedings of the 56th Annual Design Automation Conference (DAC’19)*. 1–4.

[136] Kishor Kunal, Jitesh Poojary, Tommoy Dhar, Meghna Madhusudan, Ramesh Harjani, and Sachin S. Sapatnekar. 2020. A general approach for identifying hierarchical symmetry constraints for analog circuit layout. In *Proceedings of the 2020 IEEE/ACM International Conference on Computer Aided Design (ICCAD’20)*. IEEE, Los Alamitos, CA, 1–8.

[137] Yann Lecun, Yoshua Bengio, and Geoffrey Hinton. 2015. Deep learning. *Nature Cell Biology* 21, 7, 553 (May 2015), 436–444. https://doi.org/10.1038/nature14539

[138] Yu-Wei Lee and Nur A. Touba. 2015. Improving logic obfuscation via logic cone analysis. In *Proceedings of the 2015 16th Latin-American Test Symposium (LATS’15)*. IEEE, Los Alamitos, CA, 1–6.

[139] Lok Yan. (n.d.) Automatic Implementation of Secure Silicon (AISS). Retrieved September 20, 2022 from https://www.darpa.mil/program/automatic-implementation-of-secure-silicon.

[140] Andrew J. Leiserson, Mark E. Marson, and Megan A. Wachs. 2014. Gate-level masking under a path-based leakage metric. In *Cryptographic Hardware and Embedded Systems—CHES 2014*, Lejla Batina and Matthew Robshaw (Eds.). Springer, Berlin, Germany, 580–597.

[141] Daphné Leprince-Ringuet. 2021. The global chip shortage is creating a new problem: More fake components. *ZDNET*. Retrieved September 20, 2022 from https://www.zdnet.com/article/the-global-chip-shortage-is-creating-a-new-problem-more-fake-components-as-fraudsters-cash-in/.

[142] Ilamar Levi, Davide Bellizia, David Bol, and François-Xavier Standaert. 2020. Ask less, get more: Side-channel signal hiding, revisited. *IEEE Transactions on Circuits and Systems I: Regular Papers* 67, 12 (2020), 4904–4917.

[143] Hao Li, Fanshu Jiao, and Alex Doboli. 2016. Analog circuit topological feature extraction with unsupervised learning of new sub-structures. In *Proceedings of the 2016 Design, Automation, and Test in Europe Conference and Exhibition (DATE’16)*. IEEE, Los Alamitos, CA, 1509–1512.

[144] Tian Li, Anit Kumar Sahu, Ameet Talwalkar, and Virginia Smith. 2020. Federated learning: Challenges, methods, and future directions. *IEEE Signal Processing Magazine* 37, 3 (May 2020), 50–60. https://doi.org/10.1109/MSP.2020.2975749

[145] Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin S. Sapatnekar, Ramesh Harjani, and Jiang Hu. 2020. Exploring a machine learning approach to performance driven analog IC placement. In *Proceedings of the 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI’20)*. IEEE, Los Alamitos, CA, 24–29.

[146] Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin S. Sapatnekar, Ramesh Harjani, and Jiang Hu. 2020. A customized graph neural network model for guiding analog IC placement. In *Proceedings of the 2020 IEEE/ACM International Conference on Computer Aided Design (ICCAD’20)*. IEEE, Los Alamitos, CA, 1–9.
A Survey and Perspective on AI for Security-Aware EDA

[147] Yaping Li, Yong Wang, Yusong Li, Ranran Zhou, and Zhaojun Lin. 2019. An artificial neural network assisted optimization system for analog design space exploration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 39, 10 (2019), 2640–2653.

[148] Zhen Li, Deqing Zhu, Shouhuai Xu, Xinyu Ou, Hai Jin, Sujuan Wang, Zhijun Deng, and Yuyi Zhong. 2018. VulDeepEcker: A deep learning-based system for vulnerability detection. arXiv preprint arXiv:1801.01681 (2018).

[149] Rongjian Liang, Zhiyao Xie, Jinwook Jung, Vishnavi Chauha, Yiran Chen, Jiang Hu, Hua Xiang, and Gi-Joon Nam. 2020. Routing-free crosstalk prediction. In Proceedings of the 2020 IEEE/ACM International Conference on Computer Aided Design (ICCAD’20). 1–9.

[150] Haiguang Liao, Wentai Zhang, Xuliang Dong, Barnabas Poczos, Kenji Shimada, and Levent Burak Kara. 2020. A deep reinforcement learning approach for global routing. Journal of Mechanical Design 142, 6 (2020), Article 061701, 12 pages.

[151] Jens Lienig and Juergen Scheible. 2020. Steps in Physical Design: From Netlist Generation to Layout Post Processing. Springer International Publishing, Cham, Switzerland, 165–211. https://doi.org/10.1007/978-3-030-39284-0_5

[152] Kuang Tsan Lin. 2012. Based on binary encoding methods and visual cryptography schemes to hide data. In Proceedings of the 2012 8th International Conference on Intelligent Information Hiding and Multimedia Signal Processing. 59–62. https://doi.org/10.1109/IH-MSP.2012.20

[153] Zhen Li, Deqing Zou, Shouhuai Xu, Xinyu Ou, Hai Jin, Sujuan Wang, Zhijun Deng, and Yuyi Zhong. 2018. VulDeepEcker: A deep learning-based system for vulnerability detection. arXiv preprint arXiv:1801.01681 (2018).

[154] Moritz Lipp, Michael Schwarz, Daniel Gruss, Thomas Prescher, Werner Haas, Anders Fogh, Jann Horn, et al. 2018. Meltdown: Reading kernel memory from user space. In Proceedings of the 27th USENIX Security Symposium (USENIX Security’18). 973–990.

[155] Yi-Chen Lu, Sai Pentapati, and Sung Kyu Lim. 2021. The law of attraction: Affinity-aware placement optimization system for analog design space exploration. In Proceedings of the 2020 21st International Symposium on Quality Electronic Design (ISQED’20). IEEE, Los Alamitos, CA, 199–205.

[156] Zhenbao Liu, Zhen Jia, Chi-Man Vong, Shuhui Bu, Junwei Han, and Xiaojun Tang. 2017. Capturing high-discriminative fault features for electronics-rich analog system via deep learning. IEEE Transactions on Industrial Informatics 13, 3 (2017), 1213–1226.

[157] Yi-Chen Lu, Siyuan Tang, and Jinbo Yu. 2019. Using polynomial regression and artificial neural networks for reusable analog ic sizing. In Proceedings of the 2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD’19). IEEE, Los Alamitos, CA, 13–16.

[158] Yi-Chen Lu, Sai Pentapati, and Sung Kyu Lim. 2020. VLSI placement optimization using graph neural networks. In Proceedings of the 2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’20). IEEE, Los Alamitos, CA, 733–738.

[159] Yi-Chen Lu, Sai Pentapati, and Sung Kyu Lim. 2020. VLSI placement optimization using graph neural networks. In Proceedings of the 34th Advances in Neural Information Processing Systems Workshop on ML for Systems (NeurIPS’20).

[160] R. Livengood, S. Tan, P. Hack, M. Kane, and Y. Greenzweig. 2011. Focused ion beam circuit edit—A look into the past, present, and future. Microscopy and Microanalysis 17, S2 (2011), 672–673. https://doi.org/10.1017/S1431927611004235

[161] Nuno Lourenço, Engin Afacan, Ricardo Martins, Fábio Passos, António Canelas, Ricardo Póvoa, Nuno Horta, and G. Dundar. 2019. Using polynomial regression and artificial neural networks for reusable analog ic sizing. In Proceedings of the 2019 16th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’19). IEEE, Los Alamitos, CA, 13–16.

[162] Nuno Lourenço, João Rosa, Ricardo Martins, Helena Aidos, António Canelas, Ricardo Póvoa, and Nuno Horta. 2018. On the exploration of promising analog IC designs via artificial neural networks. In Proceedings of the 2018 15th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD’18). IEEE, Los Alamitos, CA, 733–738.

[163] Yi-Chen Lu, Siddhartha Nath, Vishal Khandelwal, and Sung Kyu Lim. 2021. RL-Sizer: VLSI gate sizing for timing optimization using deep reinforcement learning. In Proceedings of the 2021 58th ACM/IEEE Design Automation Conference (DAC’21). IEEE, Los Alamitos, CA, 733–738.

[164] Yi-Chen Lu, Sai Pentapati, and Sung Kyu Lim. 2020. VLSI placement optimization using graph neural networks. In Proceedings of the 34th Advances in Neural Information Processing Systems Workshop on ML for Systems (NeurIPS’20).

[165] Yi-Chen Lu, Sai Pentapati, and Sung Kyu Lim. 2021. The law of attraction: Affinity-aware placement optimization using graph neural networks. In Proceedings of the 2021 International Symposium on Physical Design. 7–14.

[166] Robert E. Lyons and Wouter Vanderkulk. 1962. The use of triple-modular redundancy to improve computer reliability. IBM Journal of Research and Development 6, 2 (1962), 200–209.

[167] Haocheng Ma, Jiaji He, Yanjiang Liu, Leibo Liu, Yiqiang Zhao, and Yier Jin. 2021. Security-driven placement and routing tools for electromagnetic side-channel protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 40, 6 (2021), 1077–1089. https://doi.org/10.1109/TCAD.2020.3024938

ACM Transactions on Design Automation of Electronic Systems, Vol. 28, No. 2, Article 16. Pub. date: March 2023.
[168] Jonathon Magaña, Daohang Shi, Jackson Melchert, and Azadeh Davoodi. 2017. Are proximity attacks a threat to the security of split manufacturing of integrated circuits? IEEE Transactions on Very Large Scale Integration (VLSI) Systems 25, 12 (2017), 3406–3419.

[169] Hosein Mohammadi Makrani, Farnoud Farahmand, Hossein Sayadi, Sara Bondi, Sai Manoj Pudukotai Dinakarrao, Houman Homayoun, and Setareh Rafatirad. 2019. Pyramid: Machine learning framework to estimate the optimal timing and resource usage of a high-level synthesis design. In Proceedings of the 29th International Conference on Field-Programmable Logic and Applications (FPL'19), 397–405. https://doi.org/10.1109/FPL.2019.00069

[170] Eman Mandouh and Amir G. Wassall. 2018. Application of machine learning techniques in post-silicon debugging and bug localization. Journal of Electronic Testing 34, 2 (April 2018), 163–181. https://doi.org/10.1007/s10836-018-5716-y

[171] Olivier Markowitch, Liran Lerman, and Gianluca Bontempelli. 2011. Side channel attack: An approach based on machine learning. In Proceedings of the International Conference on Constructive Side-Channel Analysis and Secure Design (COSADE’11).

[172] Grant Martin, Louis Scheffer, and Luciano Lavagno. 2016. Electronic Design Automation for Integrated Circuits Handbook. CRC Press, Boca Raton, FL.

[173] Mohamed El Massad, Jun Zhang, Siddharth Garg, and Mahesh V. Tripunitara. 2017. Logic locking for secure outsourced chip fabrication: A new attack and provably secure defense mechanism. arXiv preprint arXiv:1703.10187 (2017).

[174] Teruki Matsuba, Nobukazu Takai, Masafumi Fukuda, and Yusuke Kubo. 2018. Inference of suitable for required specification analog circuit topology using deep learning. In Proceedings of the 2018 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS’18). IEEE, Los Alamitos, CA, 131–134.

[175] Brendan McMahen and Daniel Ramage. 2017. Federated Learning: Collaborative Machine Learning without Centralized Training Data. Retrieved February 1, 2022 from https://ai.googleblog.com/2017/04/federated-learning-collaborative.html.

[176] Rayan Mina, Chadi Jabbour, and George E. Sakr. 2022. A review of machine learning techniques in analog integrated circuit design automation. Electronics 11, 3 (2022), 435.

[177] Azalia Mirhoseini, Anna Goldie, Mustafa Yazgan, Joe Jiang, Ebrahim Songhori, Shen Wang, Young-Joon Lee, et al. 2020. Chip placement with deep reinforcement learning. arXiv preprint arXiv:2004.10746 (2020).

[178] Azalia Mirhoseini, Anna Goldie, Mustafa Yazgan, Joe Wenjie Jiang, Ebrahim M. Songhori, Shen Wang, Young-Joon Lee, et al. 2021. A graph placement methodology for fast chip design. Nature 594 7862 (2021), 207–212.

[179] Thorben Moos, Felix Wegener, and Amir Moradi. 2021. DL-LA: Deep learning leakage assessment: A modern roadmap for SCA evaluations. IACR Transactions on Cryptographic Hardware and Embedded Systems 2021 (2021), 552–598.

[180] Sean D. Murphy and Kevin G. McCarthy. 2021. Automated design of CMOS operational amplifier using a neural network. In Proceedings of the 2021 32nd Irish Signals and Systems Conference (ISSC’21). IEEE, Los Alamitos, CA, 1–6.

[181] Adib Nahiyani, Farimah Farahmandi, Prabhat Mishra, Domenic Forte, and Mark Tehranipoor. 2019. Security-aware FSM design flow for identifying and mitigating vulnerabilities to fault attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 38, 6 (2019), 1003–1016. https://doi.org/10.1109/TCAD.2018.2834396

[182] Adib Nahiyani, Mehdi Sadi, Rahul Vittal, Gustavo Contreras, Domenic Forte, and Mark Tehranipoor. 2017. Hardware trojan detection through information flow security verification. In Proceedings of the 2017 IEEE International Test Conference (ITC’17). 1–10. https://doi.org/10.1109/TEST.2017.8242062

[183] Annamalai Narayanan, Mahinthan Chandramohan, Rajasekar Venkatesan, Lihui Chen, Yang Liu, and Shantanu Jaiswal. 2017. graph2vec: Learning distributed representations of graphs. arXiv preprint arXiv:1707.05005 (2017).

[184] W. L. Neto, Max Austin, Scott Temple, L. Amari, Xifan Tang, and P. Gaillardon. 2019. LSOracle: A logic synthesis framework driven by artificial intelligence. Invited paper. In Proceedings of the 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’19). 1–6.

[185] Yaara Neumeier and Osnat Keren. 2012. Punctured Karpovsky-Taubin binary robust error detecting codes for cryptographic devices. In Proceedings of the 2012 IEEE 18th International On-Line Testing Symposium (IOLTS’12). IEEE, Los Alamitos, CA, 156–161.

[186] Keiron O’Shea and Ryan Nash. 2015. An introduction to convolutional neural networks. ArXiv E-prints arXiv:1511.08458 (2015).

[187] Samuel Pagliarini, Joseph Sweeney, Ken Mai, Shawn Blanton, Larry Pileggi, and Subhasish Mitra. 2020. Split-chip design to prevent ip reverse engineering. IEEE Design & Test 38, 4 (2020), 109–118.

[188] Po-Cheng Pan, Chien-Chia Huang, and Hung-Ming Chen. 2019. Late breaking results: An efficient learning-based approach for performance exploration on analog and RF circuit synthesis. In Proceedings of the 2019 56th ACM/IEEE Design Automation Conference (DAC’19). IEEE, Los Alamitos, CA, 1–2.

[189] S. J. Pan and Q. Yang. 2010. A survey on transfer learning. IEEE Transactions on Knowledge and Data Engineering 22, 10 (2010), 1345–1359. https://doi.org/10.1109/TKDE.2009.191
A Survey and Perspective on AI for Security-Aware EDA

[190] Zhixin Pan and Prabhak Mishra. 2021. Automated test generation for hardware Trojan detection using reinforcement learning. In Proceedings of the 26th Asia and South Pacific Design Automation Conference (ASPDAC’21). ACM, New York, NY, 408–413. https://doi.org/10.1145/3394885.3431595

[191] Ghasem Pasandi, Shahin Nazarian, and Massoud Pedram. 2019. Approximate logic synthesis: A reinforcement learning-based technology mapping approach. In Proceedings of the 20th International Symposium on Quality Electronic Design (ISQED’19). IEEE, Los Alamitos, CA, 26–32.

[192] Ghasem Pasandi, MacKenzie Peterson, Moises Herrera, Shahin Nazarian, and Massoud Pedram. 2020. Deep-PowerX: A deep learning-based framework for low-power approximate logic synthesis. In Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED’20), 73–78. https://doi.org/10.1109/ISLPED5406555

[193] Márcio G. Passos, P. H. da Silva, and Humberto C. C. Fernandes. 2006. A RBF/MLP modular neural network for microwave device modeling. International Journal of Computer Science and Network Security 6, 5A (2006), 81–86.

[194] Adam Paszke, Sam Gross, Francisco Massa, Adam Lerer, James Bradbury, Gregory Chanan, Trevor Killeen, et al. 2019. PyTorch: An imperative style, high-performance deep learning library. In Advances in Neural Information Processing Systems 32, H. Wallach, H. Larochelle, A. Beygelzimer, F. d’Alché-Buc, E. Fox, and R. Garnett (Eds.). Curran Associates, 8024–8035. http://papers.neurips.cc/paper/9015-pytorch-an-imperative-style-high-performance-deep-learning-library.pdf.

[195] M. Pecht and S. Tiku. 2006. Bogus: Electronic manufacturing and consumers confront a rising tide of counterfeit electronics. IEEE Spectrum 43, 5 (May 2006), 37–46. https://doi.org/10.1109/MSPEC.2006.1628506

[196] F. Pedregosa, G. Varoquaux, A. Gramfort, V. Michel, B. Thirion, O. Grisel, M. Blondel, et al. 2011. Scikit-learn: Machine learning in Python. Journal of Machine Learning Research 12 (2011), 2825–2830.

[197] Guy Perry. 2007. The Fundamentals of Digital Semiconductor Testing. Soft Test Inc.

[198] Vladimir Petrovic, Marko Ilic, Gunter Schoof, and Zoran Stamenkovic. 2012. Design methodology for fault tolerant ASICs. In Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS’12), 8–11. https://doi.org/10.1109/DDECS.2012.6219014

[199] Stjepan Picek, Annelie Heuser, Alan Jovic, Shivam Bhasin, and Francesco Regazzoni. 2019. The curse of class imbalance and conflicting metrics with machine learning for side-channel evaluations. IACR Transactions on Cryptographic Hardware and Embedded Systems 2019, 1 (2019), 1–29.

[200] Stjepan Picek, Guilherme Perin, Luca Mariot, Lichao Wu, and Lejla Batina. 2021. SoK: Deep learning-based physical side-channel analysis. Cryptology ePrint Archive 2021 (2021), 1–19.

[201] Thomas Popp and Stefan Mangard. 2005. Masked dual-rail pre-charge logic: DPA-resistance without routing constraints. In Cryptographic Hardware and Embedded Systems—CHES 2005, Josyula R. Rao and Berk Sunar (Eds.). Springer, Berlin, Germany, 172–186.

[202] Emmanuel Prouff and Matthieu Rivain. 2013. Masking against side-channel attacks: A formal security proof. In Advances in Cryptology—EUROCRYPT 2013, Thomas Johansson and Phong Q. Nguyen (Eds.). Springer, Berlin, Germany, 142–159.

[203] Emmanuel Prouff, Matthieu Rivain, and Regis Bevan. 2009. Statistical analysis of second order differential power analysis. IEEE Transactions on Computers 58, 6 (2009), 799–811. https://doi.org/10.1109/TC.2009.15

[204] Jeyavijayan Rajendran, Aman Ali, Ozgur Sinanoglu, and Ramesh Karri. 2015. Belling the CAD: Toward security-centric electronic system design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 34, 11 (2015), 1756–1769. https://doi.org/10.1109/TCAD.2015.2428707

[205] Jeyavijayan Rajendran, Youngok Pino, Ozgur Sinanoglu, and Ramesh Karri. 2012. Security analysis of logic obfuscation. In Proceedings of the 49th Annual Design Automation Conference (DAC’12). 83–89.

[206] Jeyavijayan Rajendran, Huan Zhang, Chi Zhang, Garrett S. Rose, Youngok Pino, Ozgur Sinanoglu, and Ramesh Karri. 2015. Fault analysis-based logic encryption. IEEE Transactions on Computers 64, 2 (2015), 410–424. https://doi.org/10.1109/TC.2013.193

[207] Behzad Razavi. 2000. Design of Analog CMOS Integrated Circuits. McGraw-Hill Education.

[208] Oscar Reparaz. 2016. Detecting flawed masking schemes with leakage detection tests. In Proceedings of the International Conference on Fast Software Encryption. 204–222.

[209] Oscar Reparaz, Laurent De Meyer, Begül Bilgin, Victor Arribas, Svetla Nikola, Ventzislav Nikola, and Nigel Smart. 2018. CAPA: The spirit of a beaver against physical attacks. In Proceedings of the Annual International Cryptology Conference. 121–151.

[210] Jorai Rijsdijk, Lichao Wu, and Guilherme Perin. 2021. Reinforcement learning-based design of side-channel countermeasures. Cryptology ePrint Archive 2021 (2021), 1–21.

[211] Jorai Rijsdijk, Lichao Wu, Guilherme Perin, and Stjepan Picek. 2021. Reinforcement learning for hyperparameter tuning in deep learning-based side-channel analysis. Cryptology ePrint Archive 2021 (2021), 71.

[212] Jordan Robertson and Michael Riley. 2018. The big hack: How China used a tiny chip to infiltrate us companies. Bloomberg Businessweek 4, 2018 (2018).
[213] E. Rosenbaum, J. Xiong, A. Yang, Z. Chen, and Maxim Raginsky. 2020. Machine learning for circuit aging simulation. In *Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM’20)*. IEEE, Los Alamitos, CA, 39.

[214] Michael Rotman and Lior Wolf. 2020. Electric analog circuit design with hypernetworks and a differential simulator. In *Proceedings of the 2020 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP’20)*. IEEE, Los Alamitos, CA, 4157–4161.

[215] Cynthia Rudin. 2019. Stop explaining black box machine learning models for high stakes decisions and use interpretable models instead. *Nature Machine Intelligence* 1, 5 (May 2019), 206–215. https://doi.org/10.1038/s42256-019-0048-x

[216] Rob A. Rutenbar. 2006. Design automation for analog: The next generation of tool challenges. In *Proceedings of the 2006 IEEE/ACM International Conference on Computer-Aided Design*. IEEE, Los Alamitos, CA, 458–460.

[217] Hassan Salmani, Mark Tehranipoor, and J. Plusquellec. 2012. A novel technique for improving hardware Trojan detection and reducing trojan activation time. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 20 (2 2012), 112–125. https://doi.org/10.1109/TVLSI.2010.2093547

[218] Adriana C. Sanabria-Borbón, Sergio Soto-Aguilar, Johan J. Estrada-López, Douglas Allaire, and Edgar Sánchez-Sinencio. 2020. Gaussian-process-based surrogate for optimization-aided and process-variations-aware analog circuit design. *Electronics* 9, 4 (2020), 685.

[219] Udaya Shankar Santhana Krishnan and Kalpana Palanisamy. 2021. Recycled integrated circuit detection using reliability analysis and machine learning algorithms. *IET Computers & Digital Techniques* 15, 1 (2021), 20–35.

[220] A. Schaldenbrand. 2019. *Analog Reliability Analysis for Mission-Critical Applications*. White Paper. Cadence Design Systems Inc.

[221] Juergen Scheible and Jens Lienig. 2015. Automation of analog IC layout: Challenges and solutions. In *Proceedings of the 2015 International Symposium on Physical Design*. 33–40.

[222] Keertana Settaluri, Ameer Haj-Ali, QiQing Huang, Kourosh Hakhamaneshi, and Borivoje Nikolic. 2020. AutoCkt: Deep reinforcement learning of analog circuit designs. In *Proceedings of the 2020 Design, Automation, and Test in Europe Conference and Exhibition (DATE’20)*. IEEE, Los Alamitos, CA, 490–495.

[223] Nimesh Shah, Durba Chatterjee, Brojogopal Sapui, Debdeep Mukhopadhyay, and Arindam Basu. 2021. Introducing recurrence in strong PUFs for enhanced machine learning attack resistance. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* 11, 2 (2021), 319–332.

[224] Bicky Shaya, Ujjwal Guin, Mark Tehranipoor, and Domenic Forte. 2015. Performance optimization for on-chip sensors to detect recycled ICs. In *Proceedings of the 2015 33rd IEEE International Conference on Computer Design (ICCD’15)*. IEEE, Los Alamitos, CA, 289–295.

[225] Bicky Shaya, Tony He, Hassan Salmani, Domenic Forte, Swarup Bhunia, and Mark Tehranipoor. 2017. Benchmarking of hardware Trojans and maliciously affected circuits. *Journal of Hardware and Systems Security* 1, 1 (2017), 85–102.

[226] Bicky Shaya, Haoting Shen, Mark Tehranipoor, and Domenic Forte. 2019. Covert gates: Protecting integrated circuits with undetectable camouflaging. *IACR Transactions on Cryptographic Hardware and Embedded Systems* 2019 (2019), 86–118.

[227] Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin. 2017. AppSAT: Approximately deobfuscating integrated circuits. In *Proceedings of the 2017 IEEE International Symposium on Hardware Oriented Security and Trust (HOST’17)*. IEEE, Los Alamitos, CA, 95–100.

[228] Qihang Shi, Navid Asadizanjani, Domenic Forte, and Mark M. Tehranipoor. 2016. A layout-driven framework to assess vulnerability of ICs to microprobing attacks. In *Proceedings of the 2016 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’16)*. IEEE, Los Alamitos, CA, 155–160.

[229] Qihang Shi, Mark M. Tehranipoor, and Domenic Forte. 2018. Obfuscated built-in self-authentication with secure and efficient wire-lifting. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 38, 11 (2018), 1981–1994.

[230] Dominik Sisejkovic, Farhad Merchant, Lennart M. Reimann, Harshit Srivastava, Ahmed Hallawa, and Rainer Leupers. 2021. Challenging the security of logic locking schemes in the era of deep learning: A neuroevolutionary approach. *ACM Journal of Emerging Technologies in Computing Systems* 17, 3 (May 2021), 1–26. https://doi.org/10.1145/3431389

[231] Haralampos-G. Stratigopoulos and Stephen Sunter. 2014. Fast Monte Carlo-based estimation of analog parametric test metrics. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 33, 12 (2014), 1977–1990.

[232] Kiruba Sankaran Subramani, Angelos Antonopoulos, Ahmed Attia Abotabi, Aria Nosratinia, and Yiorgos Makris. 2017. ACE: Adaptive channel estimation for detecting analog/RF Trojans in WLAN transceivers. In *Proceedings of the 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’17)*. IEEE, Los Alamitos, CA, 722–727.

[233] Pramod Subramanyan, Sayak Ray, and Sharad Malik. 2015. Evaluating the security of logic encryption algorithms. In *Proceedings of the 2015 IEEE International Symposium on Hardware Oriented Security and Trust (HOST’15)*. IEEE, Los Alamitos, CA, 137–143.
A Survey and Perspective on AI for Security-Aware EDA

[234] Takeshi Sugawara, Natsu Shoji, Kazuo Sakiyama, Kohei Matsuda, Noriyuki Miura, and Makoto Nagata. 2019. Side-channel leakage from sensor-based countermeasures against fault injection attack. *Microelectronics Journal* 90 (2019), 63–71. https://doi.org/10.1016/j.mejo.2019.05.017

[235] Shiliang Sun, Zehui Cao, Han Zhu, and Jing Zhao. 2019. A survey of optimization methods from a machine learning perspective. *IEEE Transactions on Cybernetics* 50, 8 (2019), 3668–3681.

[236] Berk Sunar, Gunnar Gaubatz, and Erkay Savas. 2007. Sequential circuit design for embedded cryptographic applications resilient to adversarial faults. *IEEE Transactions on Computers* 57, 1 (2007), 126–138.

[237] Alexey Svyatkovskiy, Ying Zhao, Shengyu Fu, and Neel Sundaresan. 2019. Pythia: AI-assisted code completion system. In *Proceedings of the 25th ACM SIGKDD International Conference on Knowledge Discovery and Data Mining*. 2727–2735.

[238] Koen Swings, Georges Gielen, and Willy Sansen. 1990. An intelligent analog IC design system based on manipulation of design equations. In *Proceedings of the IEEE Custom Integrated Circuits Conference*. IEEE, Los Alamitos, CA, 8–6.

[239] Nobukazu Takai and Masafumi Fukuda. 2017. Prediction of element values of OPamp for required specifications utilizing deep learning. In *Proceedings of the 2017 International Symposium on Electronics and Smart Devices (ISESD’17)*. IEEE, Los Alamitos, CA, 300–303.

[240] Benjamin Tan, Ramesh Karri, Nimisha Limaye, Abhrajit Sengupta, Ozgur Sinanoglu, Moshiur Rahman, Swarup Bhunia, et al. 2020. Benchmarking at the frontier of hardware security: Lessons from logic locking. *arXiv preprint arXiv:2006.06806* (2020).

[241] Jun Tao, Changhui Liao, Xuan Zeng, and Xin Li. 2015. Harvesting design knowledge from the Internet: High-dimensional performance tradeoff modeling for large-scale analog circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 35, 1 (2015), 23–36.

[242] Mohammad Tehranipoor and Farinaz Koushanfar. 2010. A survey of hardware trojan taxonomy and detection. *IEEE Design Test & Test of Computers* 27, 1 (2010), 10–25. https://doi.org/10.1109/MDT.2010.7

[243] Mohammad Tehranipoor and Cliff Wang. 2011. *Introduction to Hardware Security and Trust*. Springer.

[244] Apichat Terapasirdsin and Naruemon Wattanapongsakorn. 2010. Crosstalk minimization in VLSI design using signal transition avoidance. In *Proceedings of the 2010 10th International Symposium on Communications and Information Technologies*. 911–915. https://doi.org/10.1109/ISCIT.2010.5665117

[245] Benjamin Timon. 2019. Non-profiled deep learning-based side-channel attacks with sensitivity analysis. *IACR Transactions on Cryptographic Hardware and Embedded Systems* 2019 (2019), 107–131.

[246] Victor Tomashevich, Yaara Neumeier, Raghavan Kumar, Osnat Keren, and Ilia Polian. 2014. Protecting cryptographic hardware against malicious attacks by nonlinear robust codes. In *Proceedings of the 2014 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT’14)*. IEEE, Los Alamitos, CA, 40–45.

[247] Elena Trichina. 2003. Combinational logic design for AES subbyte transformation on masked data. *Cryptology ePrint Archive* 2003 (2003), 1–13.

[248] Bogdan Tudor, Joddy Wang, Weidong Liu, and Hany Elhak. 2011. *MOS Device Aging Analysis with HSPICE and CustomSim*. White Paper. Synopsys.

[249] Dmitry Utyamishhev and Inna Partin-Vaisband. 2020. Real-time detection of power analysis attacks by machine learning of power supply variations on-chip. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 39, 1 (2020), 45–55. https://doi.org/10.1109/TCAD.2018.2883971

[250] Kaushik Vaidyanathan, Bishnu P. Das, Ekin Sumbul, Renzhi Liu, and Larry Pileggi. 2014. Building trusted ICs using split fabrication. In *Proceedings of the 2014 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’14)*. IEEE, Los Alamitos, CA, 1–6.

[251] Arunkumar Vijayakumar and Sandip Kundu. 2015. A novel modeling attack resistant PUF design based on non-linear voltage transfer characteristics. In *Proceedings of the 2015 Design, Automation, and Test in Europe Conference and Exhibition (DATE’15)*. IEEE, Los Alamitos, CA, 653–658.

[252] Arunkumar Vijayakumar, Vinay C. Patil, Charles B. Prado, and Sandip Kundu. 2016. Machine learning resistant strong PUF: Possible or a pipe dream? In *Proceedings of the 2016 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’16)*. IEEE, Los Alamitos, CA, 19–24.

[253] Georgios Volanis, Yichuan Lu, Sai Govinda Rao Nimmalapudi, Angelos Antonopoulos, Andrew Marshall, and Yiorgos Makris. 2019. Analog performance locking through neural network-based biasing. In *Proceedings of the 2019 IEEE 37th VLSI Test Symposium (VTS’19)*. IEEE, Los Alamitos, CA, 1–6.

[254] Fa Wang, Paolo Cachecho, Wangyang Zhang, Shupeng Sun, Xin Li, Rouwaida Kanj, and Chenjie Gu. 2015. Bayesian model fusion: Large-scale performance modeling of analog and mixed-signal circuits by reusing early-stage data. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 35, 8 (2015), 1255–1268.

[255] Huanyu Wang, Domenic Forte, Mark M. Tehranipoor, and Qihang Shi. 2017. Probing attacks on integrated circuits: Challenges and research opportunities. *IEEE Design & Test* 34, 5 (2017), 63–71. https://doi.org/10.1109/MDAT.2017.2729398
[256] Huanyu Wang, Qihang Shi, Domenic Forte, and Mark M. Tehranipoor. 2019. Probing assessment framework and evaluation of anti-biogram solutions. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 27, 6 (June 2019), 1239–1252. https://doi.org/10.1109/TVLSI.2019.2901449

[257] Hanrui Wang, Kuan Wang, Jiacheng Yang, Linxiao Shen, Nan Sun, Hae-Seung Lee, and Song Han. 2020. GCN-RL circuit designer: Transferable transistor sizing with graph neural networks and reinforcement learning. In *Proceedings of the 2020 57th ACM/IEEE Design Automation Conference (DAC’20)*. IEEE, Los Alamitos, CA, 1–6.

[258] Hanrui Wang, Jiacheng Yang, Hae-Seung Lee, and Song Han. 2018. Learning to design circuits. *arXiv preprint arXiv:1812.02734* (2018).

[259] Jiafan Wang, Congyin Shi, Edgar Sanchez-Sinencio, and Jiang Hu. 2015. Built-in self-optimization for variation resilience of analog filters. In *Proceedings of the 2015 IEEE Computer Society Annual Symposium on VLSI*. IEEE, Los Alamitos, CA, 656–661.

[260] Laung-Terng Wang, Yao-Wen Chang, and Kwang-Ting Tim Cheng. 2009. *Electronic Design Automation: Synthesis, Verification, and Test*. Morgan Kaufmann.

[261] Yujie Wang, Pu Chen, Jiang Hu, Guofeng Li, and Jeyavijayan Rajendran. 2018. The cat and mouse in split manufacturing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 26, 5 (2018), 805–817.

[262] Yi Wang and Paul D. Franzon. 2018. RFIC IP redesign and reuse through surrogate based machine learning method. In *Proceedings of the 2018 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO’18)*. IEEE, Los Alamitos, CA, 1–4.

[263] Zheng Wang, Yi Chen, Aakash Patil, Jayasanker Jayabal, Xueyong Zhang, Chip-Hong Chang, and Arindam Basu. 2017. Current mirror array: A novel circuit topology for combining physical unclonable function and machine learning. *IEEE Transactions on Circuits and Systems I: Regular Papers* 65, 4 (2017), 1314–1326.

[264] Zhenyu Wang, Xiangzhong Luo, and Zheng Gong. 2018. Application of deep learning in analog circuit sizing. In *Proceedings of the 2018 2nd International Conference on Computer Science and Artificial Intelligence*. 571–575.

[265] Glenn Wolfe and Ranga Vemuri. 2003. Extraction and use of neural network models in automated synthesis of operational amplifiers. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 22, 2 (2003), 198–212.

[266] Lichao Wu, Guilherme Perin, and Stjepan Picek. 2020. I choose you: Automated hyperparameter tuning for deep learning-based side-channel analysis. *IACR Cryptology ePrint Archive* 2020 (2020), 1293.

[267] Nan Wu, Yuan Xie, and Cong Hao. 2021. IRONMAN: GNN-assisted design space exploration in high-level synthesis via reinforcement learning. In *Proceedings of the 2021 Great Lakes Symposium on VLSI (GLSVLSI’21)*. ACM, New York, NY, 39–44. https://doi.org/10.1145/3453688.3461495

[268] Nan Wu, Hang Yang, Yuan Xie, Pan Li, and Cong Hao. 2022. High-level synthesis prediction using GNNs: Benchmarking, modeling, and advancing. In *Proceedings of the 59th ACM/IEEE Design Automation Conference (DAC’22)*. ACM, New York, NY, 49–54. https://doi.org/10.1145/3489517.3530408

[269] Kan Xiao, Adib Nahiyan, and Mark Tehranipoor. 2016. Security rule checking in IC design. *Computer* 49, 8 (2016), 54–61.

[270] Kan Xiao and Mohammed Tehranipoor. 2013. BISA: Built-in self-authentication for preventing hardware Trojan insertion. In *Proceedings of the 2013 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’13)*. 45–50. https://doi.org/10.1109/HST.2013.6581564

[271] Zhiyao Xie, Haoxing Ren, Brucek Khailany, Ye Sheng, Santosh Santosh, Jiang Hu, and Yiran Chen. 2020. PowerNet: Transferable dynamic IR dropestimation via maximum convolutional neural network. In *Proceedings of the 2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC’20)*. IEEE, Los Alamitos, CA, 13–18.

[272] Keyulu Xu, Weihua Hu, Jure Leskovec, and Stefanie Jegelka. 2018. How powerful are graph neural networks? *arXiv preprint arXiv:1810.00826* (2018).

[273] Xiaolin Xu, Bicky Shakya, Mark M. Tehranipoor, and Domenic Forte. 2017. Novel bypass attack against all known logic locking attacks. In *Proceedings of the International Conference on Cryptographic Hardware and Embedded Systems*. 189–210.

[274] Rozhin Yasaei, Shih-Yuan Yu, Emad Kasaeyan Naeini, and Mohammad Abdullah Al Faruque. 2021. GNN4IP: Graph neural network for hardware intellectual property piracy detection. *CoRR abs/2107.09130* (2021).

[275] Rozhin Yasaei, Shih-Yuan Yu, Emad Kasaeyan Naeini, and Mohammad Abdullah Al Faruque. 2021. GNN4IP: Graph neural network for hardware intellectual property piracy detection. In *Proceedings of the 2021 58th ACM/IEEE Design Automation Conference (DAC’21)*. IEEE, Los Alamitos, CA, 217–222. https://doi.org/10.1109/DAC18074.2021.9586150

[276] Muhammad Yasin, Bodhisatwa Mazumdar, Ozgur Sinanoglu, and Jeyavijayan Rajendran. 2017. Security analysis of anti-SAT. In *Proceedings of the 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC’17)*. IEEE, Los Alamitos, CA, 342–347.

[277] Muhammad Yasin, Jeyavijayan (J. V.) Rajendran, and Ozgur Sinanoglu. 2020. A brief history of logic locking. In *Trustworthy Hardware Design: Combinational Logic Locking Techniques*. Springer International Publishing, Cham, Switzerland, 17–31. https://doi.org/10.1007/978-3-030-15334-2_2
[278] Muhammad Yasin and Ozgur Sinanoglu. 2015. Transforming between logic locking and IC camouflaging. In Proceedings of the 2015 10th International Design and Test Symposium (IDT’15). IEEE, Los Alamitos, CA, 1–4.

[279] Jing Ye, Yu Hu, and Xiaowei Li. 2016. POSTER: Attack on non-linear physical unclonable function. In Proceedings of the 2016 ACM SIGSAC Conference on Computer and Communications Security. 1751–1753.

[280] Cunxi Yu, Houping Xiao, and Giovanni De Micheli. 2018. Developing synthesis flows without human knowledge. In Proceedings of the 55th Annual Design Automation Conference (DAC’18). 1–6.

[281] Huan Yu, Madhavan Swaminathan, Chuanyi Ji, and David White. 2017. A method for creating behavioral models of oscillators using augmented neural networks. In Proceedings of the 2017 IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS’17). IEEE, Los Alamitos, CA, 1–3.

[282] Shih-Yuan Yu, Rozhin Yasaei, Qinqrong Zhou, Tommy Nguyen, and Mohammad Abdullah Al Faruque. 2021. HW2VEC: A graph learning tool for automating hardware security. arXiv:cs.CR/2017.12328 (2021).

[283] Amir Hosein Afandizadeh Zargari, Marzieh Ashrafiamiri, Minjun Seo, Sai Manoj Pudukotai Dinakarao, Mohammed E. Fouda, and Fadi J. Kurdahi. 2021. CAPTIVE: Constrained adversarial perturbations to thwart IC reverse engineering. CoRR abs/2110.11459 (2021).

[284] Ricardo Salem Zebulum, Marco Aurélio Pacheco, and Marley Maria Be Vellasco. 2018. Evolutionary Electronics: Automatic Design of Electronic Circuits and Systems by Genetic Algorithms. CRC Press, Boca Raton, FL.

[285] Wei Zeng, Azadeh Davoodi, and Rasit Onur Topaloglu. 2021. ObfusX: Routing obfuscation with explanatory analysis of a machine learning attack. In Proceedings of the 2021 26th Asia and South Pacific Design Automation Conference (ASP-DAC’21). IEEE, Los Alamitos, CA, 548–554.

[286] Elena Zennaro, Lorenzo Servadei, Keerthikumara Devarajegowda, and Wolfgang Ecker. 2018. A machine learning approach for area prediction of hardware designs from abstract specifications. In Proceedings of the 21st Euromicro Conference on Digital System Design (DSD’18). 413–420. https://doi.org/10.1109/DSD.2018.00076

[287] Zhiming Zhang, Jaya Dofe, and Qiaoyan Yu. 2020. Improving power analysis attack resistance using intrinsic noise in 3D ICs. Integration 73 (2020), 30–42. https://doi.org/10.1016/j.vlsi.2020.02.007

[288] Guangquan Zhao, Xiaoyong Liu, Bin Zhang, Yuqiang Liu, Guanxi Liu, and Cong Hu. 2018. A novel approach for analog circuit fault diagnosis based on deep belief network. Measurement 121 (2018), 170–178.

[289] Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z. Pan. 2019. GeniusRoute: A new analog routing paradigm using generative neural network guidance. In Proceedings of the 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD’19). IEEE, Los Alamitos, CA, 1–8.

[290] Xiaojin Jerry Zhu. 2005. Semi-Supervised Learning Literature Survey. University of Wisconsin–Madison.

[291] Michael Zohner, Marc Stöttinger, Sorin A. Huss, and Oliver Stein. 2012. An adaptable, modular, and autonomous side-channel vulnerability evaluator. In Proceedings of the 2012 IEEE International Symposium on Hardware-Oriented Security and Trust (HOST’12). 43–48. https://doi.org/10.1109/HST.2012.6224317

Received 17 March 2022; revised 7 July 2022; accepted 31 August 2022