Development of Tibetan Multifunctional Digital Clock Based on FPGA

Huimei Fan¹, Shuqun Wang*, Ning Mao and Kexin Dai

¹Fan Huimei (1997-), female, Yunnan, Southwest University for Nationalities, undergraduate reading.
²Wang Shuqun (1976-), female, lecturer, master. Research direction: Practice of electronic technology and measurement and control system (electrical&information engineering, Southwest Minzu University, Chengdu, China, 610225)

Abstract. This paper presents an digital clock design based on FPGA which implements the function of displaying the year, month, day, week and temperature in a Tibetan language. The whole system is designed and compiled on vivado2017.1 with verilog hardware description language, and programed on FPGA development board. The results show that the design of the Tibetan digital clock is successful and feasible.

1. Introduction
The digital clock is an essential item in daily life. Currently, there is a fully functional digital clock on the market, but the digital clock with Tibetan display function has not yet been developed. FPGA has the characteristics of flexibility and rapid prototyping. The Tibetan digital clock designed by FPGA can provide more convenient and accurate timing tools for Tibetan compatriots, and has certain market application value.

The basic functions of this design digital clock include calibration, perpetual calendar adjustment, hourly chime and alarm function, as well as Tibetan display and temperature and humidity display.

2. System Overall Framework

2.1. System Architecture
The overall topology of the system is shown in Figure 1. It consists mainly of the basys3 development board, the LCD control module, the sensor module, and the buttons, switches, and digital tubes.

![Figure 1. Overall block diagram of the system.](image)
Function of each module:\(^1\):

Switch, input module: de-jitter the input buttons and switches, and decode the output to control other functional modules;

Time, minute and second timing module: counting 1Hz low frequency clock, generating time, minute and second data;

Stopwatch module: counting 100Hz to generate stopwatch data;

Perpetual calendar module: Counts the date, generates the year, month and day data, and provides the adjustment function of the year, month and day; the time comparison, the output pulse control LED flashes when the whole point or the alarm time coincides;

The digital tube display control module: displays the time of the clock and the stopwatch and the alarm clock, and the three switches the display through the switch;

Liquid crystal display control module: Tibetan display of year, month, day, week and temperature and humidity.

2.2. System Verilog Implementation

2.2.1. Each module function Verilog implementation. The digital clock design is shown in Figure 2, including the clock crossover module, key switch input module, time division second timing module, stopwatch module, Tibetan module, time and alarm module, digital tube display control module and liquid crystal display control module.

\[
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- The digital tube display control module: displays the time of the clock and the stopwatch and the alarm clock, and the three switches the display through the switch;
- Liquid crystal display control module: Tibetan display of year, month, day, week and temperature and humidity.

2.2. Clock divider module. Basys development board crystal oscillator is 100MHz, because the processing speed required by this system is not high, so the system clock is set to 50MHz, the frequency divider mainly produces 4 low frequency clocks: respectively, the standard second pulse 1Hz clock signal for timing, clock and alarm setting 2HZ flicker signal for use, 100Hz clock signal for button and switch debounce, and 1KHz clock signal for scanning display\(^2\). Their crossover relationship is shown in Figure 3 below.

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\text{Figure 2. Digital clock internal module block diagram.}
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\text{Figure 3. Digital Clock Dividing.}
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2.2.3. The clock module. The clock module mainly counts the input 1Hz clock through the counter to generate the hour, minute and second value output to the digital tube for display, and provides the clock correction function\cite{3}.

2.2.4. Hourly hour and alarm clock module. The hourly chime function is a sensitive table with minutes and seconds. When the detection is divided into 59, when the second is greater than 50 and less than 59, the whole point signal is output.

The alarm clock module compares the set hours and minutes with the current hours and minutes. If the two are equal, the alarm signal is output. Since there is no buzzer available on the basys3 development board, both the timekeeping and the alarms alert the user by flashing a fixed LED.

2.2.5. Digital tube display module. The liquid crystal display uses 12864 module. Because the limited display area on the 12864 liquid crystal displays the contents of temperature and humidity, week and perpetual calendar, the digital tube\cite{4} display time.

2.2.6. Tibetan module. It mainly includes the display of the year, month, day and day of the week. The Arabic numerals are used to directly indicate the year, month and day. Since the Tibetan text in this design only needs to display the fixed year, month and day and Monday to Sunday, it only needs to be used. The Tibetan language is converted into dot matrix data for preservation\cite{5}, then select and display as needed. Figure 4 shows the Tibetan representation from Monday to Sunday and the year, month and day.

![Figure 4](image)

**Figure 4.** Tibetan pictures of the week and the date of the month.

After obtaining the Tibetan picture, it was modeled using pctolcd2002 font software\cite{6}, converted to a dot matrix mode is stored in the ROM in the FPGA. Figure 5 is a schematic diagram of the modulo on Monday.

![Figure 5](image)

**Figure 5.** Modulo software modulo Tibetan.
Get the modulo lattice information of all pictures\textsuperscript{(7)}, save them to the txt file, use the following verilog syntax for ROM modeling, FPGA integrated implementation software Vivado will automatically recognize the following statements and save them into ROM in the BRAM.

The ROM modeling program is as follows:

```verilog
reg [7:0] week_1234[0:2047];
reg [7:0] week_567[0:1535];
reg [7:0] number[0:1151];
initial
begin
    $readmemh("./week1234.txt", week_1234);
    $readmemh("./week567.txt", week_567);
    $readmemh("./number.txt", number);
end
```

2.2.7. **LCD control module**

There are two ways of data transmission on the LCD screen: serial and parallel. Here, 8-bit parallel transmission is adopted. The control flow of the FPGA control interface is shown in Figure 6. The first is to wait for 42ms, then perform mode setting, display setting, display clear, display switch, cursor setting, and then send a loop to display the picture\textsuperscript{(8)}.

![Figure 6. Control flow chart.](image)

2.2.8. **Temperature and humidity acquisition module design.** DHT11\textsuperscript{(9)} is an internal digital signal containing calibration. The output temperature and humidity sensor internally includes a resistive wetted component and an NTC temperature measuring component. The 8-bit microcontroller is used for data calibration and processing in parallel. The calibrated data is output through a bidirectional serial signal line. The interface control state machine of DHT11 is shown in Figure 7. There are 6 states. The first is the IDLE state, in which it waits for the 2s system power-on time. After the power-on waits, it begins to read the temperature and humidity data\textsuperscript{(10)}.

Dynamic selection based on collected temperature and humidity data. The fixed display portion includes the Celsius °C symbol for temperature and the 100% % symbol for humidity, which also initializes its lattice data into registers.
3. Conclusion
This article uses the basys3 FPGA development board, 12864 liquid crystal display and HDT11 temperature and humidity sensor to complete the multi-function Tibetan digital clock design. The implemented Tibetan digital clock has the following functions:

(1) Multi-function digital clock
The multi-function digital clock is completed by FPGA design, in which the timing, calibration, alarm clock and stopwatch display are switched by switch combination, which is displayed on the 12864 LCD screen from Monday to Sunday and the year and month, and also on the 12864 display. Display temperature and humidity measured data.

(2) Tibetan display
The dot matrix data is obtained by modulating the Tibetan character shape from Monday to Sunday, and then the dot matrix data is output to a specific area on the 12864 for display.

4. The Conclusion
In general, after testing, the functions of the Tibetan digital clock meet the requirements. The Tibetan display shows the week and the year and month are normal. The display effect is shown in Figure 8. The system has great practical value for Tibetan compatriots and has broad market application prospects.

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