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An ambipolar transistor based on a monolayer WS$_2$ using lithium ions injection

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Abstract

Ambipolar field-effect transistor (FET) devices based on two-dimensional (2D) materials have been attracted much attention due to potential applications in integrated circuits, flexible electronics and optical sensors. However, it is difficult to tune Fermi level between conduction and valence bands using a traditional SiO$_2$ as dielectric layer. Here, we employed the lithium-ion conductive glass ceramic (LiICGC) as the back-gate electrode in a monolayer WS$_2$ FET. The effective accumulation and dissipation of Li$^+$ ions in the interface induce a wide tune of Fermi level in the conducting channel by electron and hole doping, which show an ambipolar transport characteristics with threshold voltages at 0.9 V and −1.3 V, respectively. Our results provide an opportunity for fabricating ultra-thin ambipolar FET based on 2D materials.

Introduction

Two-dimensional (2D) transition metal dichalcogenides (TMDCs) have been attracted much attention due to their basic characteristics of semiconductors with high carrier mobility [1–8], which is suitable for fabricating the conducting channel in 2D field-effect transistor (FET) [9]. A monolayer TMDCs consists of one sheet of M (transition metal) atoms sandwiched by two sheets of X (chalcogen elements) atoms to form a layer of covalently bonded hexagonal quasi-2D structure [10–12]. This kind of material exhibits very special physical properties, such as chemical stability [13], low impurity [14], no dangling bonds [12], electrostatic integrity [15] and high thermal stability [16]. Moreover, strong photoluminescence emission indicates its characteristic of a direct band gap semiconductor [17–21], leading to fabricating nano-scale optoelectronic devices such as photodetectors [22], light-emitting devices [10, 23], or solar cells [24].

As a conducting channel of FET transistor, a large energy gap of TMDCs guarantees the high 'on/off' ratio at room temperature, even at higher temperature. In contrast, it is a disadvantage for achieving continuous change between hole- and electron-dominated conducting channels, which is very important in fabricating an ambipolar transistor. Some groups reported to achieve ambipolar transistors using multilayer WSe$_2$ [25], MoTe$_2$ [26] as a conduction channel on SiO$_2$/Si substrate. However, using traditional SiO$_2$ as a dielectric layer to tune the Fermi level of a monolayer TMDCs with large bandgap has the risk of oxide breakdown under high gate voltage. Some selective methods were used to improve the interface between metal and monolayer TMDCs to achieve ambipolar transistors, such as oxygen plasma irradiation [27]. Recently, the so-called ionic-liquid gating has been applied to serve as a back-gate of field effect transistor, which is based on electrostatic ionic gating in the
The WS₂ monolayers were mechanically exfoliated from 2H-phase WS₂ single crystal. Experiments involving the interface between an ionic medium and a semiconductor channel. Since the narrow space between two peaks, a dense sheet of carriers can be used to achieve novel device functionalities. Holes seen for positive gate voltage, whereas no transistor action was observed for negative gate voltages applied. LICGC (by the intrinsic doping of Li⁺ ions in the interface, which achieves effective injection of carriers into the semiconductor). Therefore, solid electrolytes, such as lithium-ion conductive glass ceramic (LICGC), are considered as a choice for electrostatic gating. Philippi reported a LICGC-gated device with a monolayer WSe₂ as the conducting channel. The devices worked well when negative gate voltages were applied, whereas no transistor action was seen for positive gate voltage. Here, we reported the electron state of a monolayer WS₂ FET can be tuned between n-type and p-type semiconductor using this kind of solid electrolyte, namely lithium-ion conductive glass ceramic (LICGC), exhibiting an ambipolar transport characteristic. It is attributed to accumulation and dissipation of lithium (Li⁺) ions in the interface, which achieves effective injection of carriers (electrons and holes) to the monolayer WS₂ material. Our results pave the way for potential applications of 2D materials in FETs and photodetectors.

**Experiments**

The WS₂ monolayers were mechanically exfoliated from 2H-phase WS₂ single crystal (purchased from HQ Graphene Company) using PDMS films, and were transferred onto a Si substrate with 300 nm SiO₂ and a LICGC (purchased from Ohara Corporation, see [36] for more information) substrate, respectively. The optical images of monolayer WS₂ on two substrates are shown in figures 1(a) and (b), where the blue dashed line indicates the location of the sample. The number of layer of samples was confirmed by a combination of photoluminescence (PL) and Raman spectroscopies. As shown in figure 1(c), two Raman peaks were experimentally observed at 359 cm⁻¹ and 420 cm⁻¹ for monolayer WS₂ on both substrates, which correspond to the in-plane (E₂g) and out-of-plane (A₁g) vibration modes, respectively [11, 12]. The energy difference between two peaks (61 cm⁻¹) is consistent with the reported value for a monolayer WS₂ [37]. Moreover, figure 1(d) shows a very strong PL emission with the peak energy at 2.003 eV for WS₂ on SiO₂ and 2.012 eV for that on LICGC substrates, respectively. It also supports that they are monolayer WS₂ with the characteristic of direct band gap semiconductor. A slight shift of peak energy (~9 meV) between two PL spectra may be induced by the intrinsic doping of Li⁺ ions for WS₂ on LICGC, absorption of environmental gas or in-plane strain during sample transfer [38–41].

![Figure 1](image-url)

**Figure 1.** The optical image of monolayer WS₂ deposited on the surface of SiO₂ substrate (a) and LICGC substrate (b), respectively. The blue lines indicate the location of samples and the black squares are the region for SHG mapping. The scale bar is 20 μm. (c) Raman spectra of the monolayer WS₂ on two substrates with two Raman modes at 359 cm⁻¹ and 420 cm⁻¹, respectively. (d) PL spectra of the monolayer WS₂ on two substrates with a representative peak around 2.0 eV. (e) SHG signals excited by a 1266 nm pulse laser in the monolayer WS₂ deposited on two substrates (black curve for SiO₂ and red curve for LICGC). (f) Polarization-resolved SHG intensity in monolayer WS₂ as a function of an angle between laboratory and crystalline coordinates, where black and red curves represent parallel and perpendicular components of SHG intensity. The spatial mapping of SHG signals in monolayer WS₂ on the SiO₂ substrate (g) and the LICGC substrate (h), respectively.
Moreover, figure 1(e) shows the signal of second-harmonic generation (SHG) spectra of the WS$_2$ on SiO$_2$ (black line) and LICGC (red line) substrates, where the SHG peaks locate at 633 nm for both samples. Figure 1(f) shows the polarization-resolved SHG spectra of the two samples, where the parallel and perpendicular components of SHG intensity exhibits \( \sin 3\theta \) and \( \cos 3\theta \) relation with respect to incident fundamental wave (FW), where \( \theta \) is the angle between laboratory and crystalline coordinates. It reflects the beneath three-fold rotational symmetry of monolayer WS$_2$ \[42–44\]. A spatial mapping for polarization-resolved SHG signal reveals the homogeneity of the entire sample on SiO$_2$/Si substrate, but fluctuation appears for sample on LICGC substrate, as shown in figures 1(g) and (h). After that, the WS$_2$ monolayers on two substrates are used to fabricate a conducting channel of FET. For the sample on LICGC, 100 nm SiO$_2$ was first deposited on the entire surface of LICGC except the location of sample, so as to avoid reaction between metal electrode and Li$^+$ ions in the substrate. Then using traditional photolithography and E-beam evaporation, a Cr (100 Å)/Au (400 Å) stacked layer serving as drain and source electrodes was deposited on sample on both substrates with a 10 \( \mu \)m channel length. Figures 2(a) and (b) show the optical images of mechanically exfoliated single-layer WS$_2$ with Cr/Au electrical contacts on SiO$_2$ substrate and SiO$_2$/Cr/Au electrical contacts on LICGC, respectively. Meanwhile the schematic of two FET structures and measurement method are also shown in two figures. All the transport measurements were performed at room temperature in air under ambient pressure.

**Results and discussion**

To check the different transport properties between two devices, electrical transport measurements were performed in our homemade semiconductor characterization system at room temperature. Figure 3(a) shows the representative transfer characteristics (\( I_{sd} - V_{gs} \)) of a monolayer WS$_2$ FET on SiO$_2$/p$^{++}$ Si substrate at the source–drain bias (\( V_{sd} \)) from 1 V to 3 V with a 0.5 V step. The curves in the inset of figure 3(a) are plotted in the logarithmic scale for clearance. The conducting state is gradually switched on with an increasing \( V_{gs} \) and switched off by applying an opposite \( V_{gs} \). The small conducting current at zero \( V_{gs} \) suggests that the monolayer WS$_2$ is an n-type doping semiconductor in the pristine state. The output current on/off ratio of the monolayer WS$_2$ FET is evaluated to be \( \sim 10^3 \). The threshold voltage (\( V_{th} \)), which is defined as the intercept of the \( V_{gs} \) axis obtained by extrapolating the linear portion of the curve of \( I_{sd} \) versus \( V_{gs} \), is around \(-10 \) V. Meanwhile, output
Characteristic curves (\(I_{ds}-V_{th}\)) at various gate voltages ranging from 0 V to +40 V in a step of 10 V are shown in figure 3(b). The non-linear output (\(I_{ds}-V_{ds}\)) characteristics at the ‘on’ state indicate that there is a large contact resistance between Cr/Au metal and WS2, which suppresses the carriers injection in the conducting channel [26,45]. The mobility of monolayer WS2 FET was estimated from the linear region in the \(I_{ds}-V_{gs}\) curve in figure 3(a) using the equation \(\mu = \frac{dI_{ds}}{dV_{gs}} \times L / (WC_{ox})\), where \(W\) is the channel width, \(L\) is the channel length, and \(C = 1.15 \times 10^{-4} \text{ F m}^{-2}\) is the capacitance per unit area of the SiO2 layer. The calculated mobility was about 0.076 cm\(^2\) V\(^{-1}\) s\(^{-1}\). Moreover, the sub-threshold swing \(S\), which is extracted from the logarithmic plot of \(I_{ds}-V_{gs}\), is 180 mV dec\(^{-1}\). The performance of SiO2-based device is not very good compared with the results reported in literature [46]. We believe that the lack of annealing treatment is main reason.

For comparison, the transfer characteristics (\(I_{ds}-V_{gs}\)) of a monolayer WS2 FET on LICGC substrate is shown in figure 3(c) with \(V_{ds}\) from -2 V to 2 V and \(V_{ds}\) from 0.1 V to 0.5 V. The curves in the inset are also plotted in the logarithmic scale for clearance. In this case, \(I_{ds}-V_{gs}\) characteristic of this device displays an ambipolar behavior with a nearly systematic gate voltage. The magnitude of current at on-state is of the order of microampere, which is approximately two orders of magnitude higher than that of leak current as shown in figure S2. It means that the conducting channel becomes conductive under large positive and negative \(V_{gs}\), respectively. The threshold voltages under two conductive cases (as shown by the black dashed lines in figure 3(c)) are around \(V_{th} = 0.9\) V and \(V_{th} = -1.3\) V, respectively. It indicates the dominated carriers in the channel are electrons under positive \(V_{gs}\) and holes under negative \(V_{gs}\), respectively. A tiny asymmetry on \(V_{th}\) indicates the n-type doping characteristic in pristine WS2, as justified in Si-based device. The output current on/off ratio of this device is calculated to be \(10^3\), which is an order of magnitude larger than that on Si substrate. Moreover, the linear output characteristic curves (\(I_{ds}-V_{ds}\)) at gate voltages ranging from 0 V to 2.0 V in steps of 0.2 V, as shown in figure 3(d), also show a nonlinear increase at ‘on’ state. It suggests that there is also a large contact resistance between Cr/Au metal and WS2 in the LICGC-based device, which is consistent with SiO2-based device. For LICGC-based device, the mobility of electron and hole were evaluated, using the formula mentioned above with \(C = 1.2 \times 10^{-12} \text{ F m}^{-2}\), to be 4.246 cm\(^2\) V\(^{-1}\) s\(^{-1}\) and 0.220 cm\(^2\) V\(^{-1}\) s\(^{-1}\), respectively. And the sub-threshold swings are 6.47 V dec\(^{-1}\) for electrons and -4.81 V dec\(^{-1}\) for holes, respectively, which is two orders of magnitude larger than the values in Philipi’s work. We believe that the residues on the top surface of WS2,

\[\text{Figure 3. (a) Transfer characteristics (}\ I_{ds}-V_{gs}\text{) of the pristine monolayer WS2 FET on SiO2/Si substrate at five biases, } V_{ds} = 1.0, 1.5, 2.0, 2.5 \text{ and } 3.0 \text{ V, respectively. (Inset shows transfer characteristics in the logarithmic scale). The current on/off ratio of the device is evaluated to be } \sim 10^3. \text{(b) The corresponding output characteristics (}\ I_{ds}-V_{ds}\text{) of the device shown in (a) at different } V_{gs} \text{ ranging from } 0 \text{ V to } +40 \text{ V in steps of } 10 \text{ V. (c) Transfer characteristics (}\ I_{ds}-V_{gs}\text{) of the pristine monolayer WS2 FET on LICGC at } V_{ds} = 0.1, 0.2, 0.3, 0.4 \text{ and } 0.5 \text{ V, respectively. (Inset is draw in logarithmic scale). The on/off ratio of the device is evaluated to be } \sim 10^3. \text{(d) The corresponding output characteristics (}\ I_{ds}-V_{ds}\text{) at different } V_{gs} \text{ ranging from } 0 \text{ V to } 2 \text{ V in steps of } 0.2 \text{ V.}\]
wrinkles or fluctuations of monolayer WS2 on LICGC and lack of annealing will be appropriate reasons. As shown in figure S3, we also observed the hysteresis loop in transfer characteristics of both devices as the applied gate bias was swept back and forth. Actually, there are many studies on the origins of hysteresis loop in literature [47, 48], such as the charging and recharging processes of LICGC, ambient environment, defects and temperature. However, it is difficult to separate the different origins in our devices, and further studies are needed in future work. For LICGC-based FET, we successfully achieved to effectively tune the carrier-type of WS2 conducting channel using a lithium-ion injection method, although the n-type doping in the pristine WS2. In the work of Philipi et al [35], ambipolar behavior of FET with similar solid electrolytes for electrostatic gating was absent. We suspect that some reasons, such as different source of LICGC materials, the quality of interface between TMDCs and LICGC, may induce the different performance of devices. Further studies to improve our performance for LICGC-based devices are needed in our future work.

For the traditional Si-based WS2 FET, the modulability of Fermi level depends on the dielectric coefficient and the thickness of dielectric materials. The thinner dielectric layer is reduced, the wider Fermi level is tuned. However, it has the risk to breakdown the devices under high voltage. However, for the LICGC-based FET, it depends on Li\(^+\) ion accumulation and dissipation at the interface. The equivalent electrical circuit is shown in figure S1 is available online at stacks.iop.org/MRX/7/076302/mmedia. Therefore, it has the advantage to widely tune Fermi level at low gate voltage. As shown in figure 4(b), for the \( V_{gs} > V_{th}^+ \), a large amount of Li\(^+\) ions are pushed to the interface between LICGC material and monolayer WS2 due to Coulomb repulsion effect. It induces the formation of abundant electrons in the conducting channel, namely the monolayer WS2. When a bias is applied between source and drain electrodes, the monolayer WS2 shows a low resistance state. The magnitude of resistance gradually decreases as the \( V_{gs} \) increases, as shown in figure 3(c). From the energy band theory, the Fermi level is tuned to the conduction band of monolayer WS2 in this case. Moreover, when the negative \( V_{gs} \) is applied to the LICGC, the most of Li\(^+\) ions are pulled back toward the lower interface between the gate electrode and the LICGC. Most of anions are left at the upper interface, which induce the formation of large number of holes in the monolayer WS2. In this case, the Fermi level is pined to the valence band at \( V_{gs} < V_{th}^- \). So when bias voltage is applied, the magnitude of resistance is also very low and decreases with increasing \( V_{gs} \) as shown in figure 3(c). At zero bias, the Fermi level is just pined to the band gap of monolayer WS2, which means a high resistance state. It is noted that the device shows off-state for FET on LICGC substrate, which is different from that on Si substrate with on-state at zero bias. We think it is attributed to the diffusion of Li\(^+\) ions at zero bias, which neutralize the electrons in the WS2 layer.

Conclusions

In summary, we have successfully demonstrated an ambipolar monolayer-WS2-based field effect transistor using solid-state electrolyte, namely LICGC. With the Li\(^+\) ions injection, the Fermi level of monolayer WS2 is continuously tuned between conduction and valence bands within 2 V gate voltage, which is much lower than that of transitional Si-based FET. The threshold voltages for two kinds of carriers are evaluated to be 0.9 V and −1.3 V, respectively. The high modulation efficiency and compatibility with traditional semiconductor process make the LICGC a potential material to apply in future 2D electronic devices.
Methods

Sample cleaning process
First, the silicon wafers were washed with acetone, alcohol and isopropanol solution in an ultrasonic cleaning machine and then dried with nitrogen. For the LICGC, we only clean its surface with dry nitrogen after unpacking to avoid any residue on the uneven surface. Second, we directly exfoliated the WS$_2$ flakes from single crystal using PDMS films. The thickness was decided through non-destructive micro-Raman and micro-PL spectroscopies. The lower surface of monolayer WS$_2$ should be very clean due to its direct exfoliation from single crystal using PDMS photoresist using spin coater with the time of 30 s and rotation speed of 3000 rad min$^{-1}$. Then they were put on hotplate for drying with the parameters of 90 °C and 5 min. By means of electron beam lithography (EBL), the electrode patterns were cross the monolayer part of samples. Then, Cr (10 nm)/Au (40 nm) metals were deposited using electron beam evaporation. At last, PMMA photoresist was lifted-off with degumming solution, and then the samples were cleaned with isopropanol solution and dried with nitrogen.

Experimental setup
The monolayer WS$_2$ on SiO$_2$ and LICGC substrates were characterized with optical microscopy, photoluminescence (PL) spectroscopy, Raman spectroscopy and second-harmonic generation (SHG) spectroscopy. For the PL and Raman measurements, a continuous-wave (CW) laser with the wavelength of 532 nm was used as an excitation, and its power was kept below 1.0 mW to avoid laser-induced heating. The PL and Raman signals were collected by a spectrometer equipped with a thermoelectric cooled charged-coupled device (CCD). For SHG measurement, a pulse-laser with a wavelength of 1266 nm was used to excite the materials, and SHG signal at 633 nm was collected by the same spectrometer. For the transport measurement, a homemade semiconductor characterization system including a source meter (Keithley 2636B), a microscope and a probe station was used to measure the transfer characteristics and output characteristics of monolayer-WS$_2$-based FET at room temperature.

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Conflict of interest
The authors declare no conflict of interest.

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