Attacks of the Knights: Exploiting Non Uniform Cache Access Time

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Abstract—Intel Knights Landing Processors have shared last level cache (LLC) across all the tiles using MESIF protocol and uses a mesh network of Caching and Homing Agents(CHA)s. Due to the structure of the network, the cache access is non uniform in nature having significant difference in cache hit times. In this paper, we try to exploit this idea to leak secret from a victim process. First, we show a naive implementation of the attack using a gem5 simulator that achieves 100% accuracy of extracting the secret bits. Then we replicate the attack in a Intel Xeon Phi 7290@ 1.50 GHz Knight’s Landing CPU to show the efficacy of the attack. In real machine we can leak the secret from a victim process at 85% accuracy and 350 kbps bandwidth. All the attacks were done on a machine without any root or sudo privileges, so this shows the strength of the attack. This can be further extended to leak secrets from different processes given the vulnerable patterns may exist in many libraries. Other processors with similar architecture (last level distributed cache in mesh networks) can also be vulnerable to similar attack strategy.

I. A SIDE CHANNEL ATTACK IN NUCA LLC

A side channel attack in a NUCA LLC (NUCA timing attack, for short) can be performed by accessing two different cache banks in the LLC. If an attacker can time the accesses, he(she) can exploit the latency difference to leak a secret. To demonstrate a NUCA timing attack, we first explain it using a simulated machine in Gem5 [2] because of the ease of explanation. Then, we show the details of the attack in a real Intel machine.

To perform the attack, we need to identify two addresses that have significant difference in LLC hit times. So, we configure a tiled architecture with 64 tiles in Gem5. Each tile contains a core, a private L1I and L1D cache, and a shared LLC (L2) bank. The size of a cache line is 64B. Each L1D is a 2-way associative 4kB cache. Each LLC bank is a 8-way associative 2MB cache. 64 tiles are connected using a 8 × 8 MESH network. With this configuration both L1D cache and LLC use the bit[10:6] of the physical address for indexing. LLC bank is selected using bit[12:6] of the physical address.

An example attack code is shown in Figure 1. Before the attack, we allocate a large array (line 1 in Figure 1) and start accessing all cache lines belonging to the array (line 12-13). At the end of those accesses, we can conclude that the initial entries of L1D cache are evicted but they still reside in LLC. This step is similar to priming the cache as used in prior cache side channel attacks [7]. Next, we design a victim function that accesses two addresses (depending on the secret) such that the addresses reside in two different LLC banks. This approach of writing victim function is inspired from the Spectre attack code [6].

For determining which addresses would be useful for the victim function, we analyze the LLC hit latency for all the entries of the array indexed from 0 to 511*64. We found that the entry at index 117*64 and 118*64 is mapped to the virtual address 0x4c7fc0 and 0xc7000, respectively. Using the LLC bank selection bits, we can verify that entry at index 117*64 (virtual address 0x4c7fc0, physical address 0xc6fc0) is mapped to bank 63. On the other hand, the entry at index 118*64 is mapped to bank 0. With this mapping, the victim function accesses either index 117*64 or 118*64 depending on the secret (Lines 5-6). As a result, when an attacker times the victim function (Lines 16-18), he(she) can infer the secret one bit at a time by comparing the access latency with the access latency of bank 63 (or 0). Thus, we can launch a NUCA timing attack on a simulated machine.

Now, we take Intel(R) Xeon Phi(TM) CPU 7290 @ 1.50GHz Knight’s Landing [8] CPU as an example real machine. This CPU has a cache structure with 32KB L1D
3 DDR4 Channels

### Task 3: Determining LLC Hit Latency at Different Tiles
To launch the attack, we need to find two cache lines whose LLC hit latencies show a significant difference when accessed from a certain core/tile. For this purpose, we profile few cache lines before executing the attack. Let us consider the cache line \( L \) (mentioned in Task 2). We want all the profiled cache lines to map to set 0 in L1D (to make it easier to perform Task 2). Therefore, we keep bits \( b_0 \) to \( b_{11} \) from \( L \) fixed. The bits that we can change to form different cache lines are bits \( b_{12} \) to \( b_{26} \) (we did not go beyond \( b_{26} \)). So, we profile cache lines with address \( L_{addr} + 1 << Shift \), for \( 12 \leq Shift \leq 26 \), one at a time. We denote those lines as \( L_{b_{12}} \) to \( L_{b_{26}} \).

We use `sched_setaffinity` to pin our profiler to core 0 and profile \( L_{b_{12}} \). We apply the technique in Task 2 to ensure that \( L_{b_{12}} \) causes L1D miss but LLC hit. The profiler then accesses the address \( L_{b_{12}} \) and times it. This is done 100,000 times in the same profiling run to get the average LLC hit latency of \( L_{b_{12}} \). Note that we are changing high order bits (bit 12 or higher) during profiling. So, the prefetcher is not able to capture the pattern and the LLC hit latency remains unaffected by the prefetcher. We profile other cache lines from \( L_{b_{13}} \) to \( L_{b_{26}} \). The latency distribution is shown in Figure 3a. We performed the profiling task in an unloaded machine multiple times. The results remained consistent. The distribution clearly shows that different cache lines have different LLC hit latency due to the NUCA organization. Based on this data, we picked \( L_{b_{14}} \) and \( L_{b_{26}} \) as our choice of addresses because they showed one of the highest latency differences.

### Task 4: Attack Demonstration
We demonstrate the NUCA timing attack by developing a victim code similar to the one in Figure 1 except \( L_{b_{14}} \) and \( L_{b_{26}} \) are accessed inside the if-else constructs. The attack code first allocates a Hugepage. Then, instead of Line 12-13 in Figure 1, the attack code implements the technique in Task 2 to ensure that both \( L_{b_{14}} \) and \( L_{b_{26}} \) cause L1D misses but LLC hits. Then, the victim function is called and the attacker times it. If the latency of the victim function is beyond \( Threshold \), the secret bit is 0. Otherwise, it is 1. We initially choose \( Threshold = 90 \) based on Figure 3a. However, since the victim code has a number of other instructions and memory accesses besides \( L_{b_{14}} \) and \( L_{b_{26}} \), we need to set the \( Threshold \) higher than 90. As shown in Figure 3b, both access latencies of the victim function with \( L_{b_{14}} \) and \( L_{b_{26}} \) are increased. So, we can increase the \( Threshold \) to 120. This achieves 85% accuracy for leaking the secret.\(^\text{1}\)

\(^\text{1}\)The detailed code for profiling and attack is available here [anonymous://open.science/r/NUCA-side-channel/poc2.c](https://anonymous://open.science/r/NUCA-side-channel/poc2.c)
(a) LLC Hit Latency distributions with Intel Xeon Phi 7290 Processor for different cache lines that have miss in L1D. bit indicates which bit is changed. For $L_{612}$, bit 12 is changed and so on.

(b) Latency changes from LLC Hit to Victim function.

Fig. 3: LLC Hit Latency Distribution profiling and implications on Victim Function based on the secret value

REFERENCES

[1] Andrea Arcangeli. Transparent hugepage support. In KVM forum, volume 9, 2010.

[2] Nathan Binkert, Bradford Beckmann, Gabriel Black, Steven K Reinhardt, Ali Saidi, Arkapraava Basu, Joel Hestness, Derek R Hower, Tushar Krishna, Somayeh Sardashti, et al. The gem5 simulator. ACM SIGARCH computer architecture news, 39(2):1–7, 2011.

[3] Daniel Hackenberg, Daniel Molka, and Wolfgang E Nagel. Comparing cache architectures and coherency protocols on x86-64 multicore smp systems. In Proceedings of the 42Nd Annual IEEE/ACM International Symposium on microarchitecture, pages 413–422, 2009.

[4] Marcos Horro, Mahmut T Kandemir, Louis-Noël Pouchet, Gabriel Rodriguez, and Juan Touriño. Effect of distributed directories in mesh interconnects. In Proceedings of the 56th Annual Design Automation Conference 2019, pages 1–6, 2019.

[5] Gorka Irazoqui, Thomas Eisenbarth, and Berk Sunar. SS a: A shared cache attack that works across cores and defies vm sandboxing–and its application to aes. In 2015 IEEE Symposium on Security and Privacy, pages 591–604. IEEE, 2015.

[6] Paul Kocher, Jann Horn, Anders Fogh, Daniel Genkin, Daniel Gruss, Werner Haas, Mike Hamburg, Moritz Lipp, Stefan Mangard, Thomas Prescher, Michael Schwarz, and Yuval Yarom. Spectre attacks: Exploiting speculative execution. In 2019 IEEE Symposium on Security and Privacy (SP), pages 1–19, 2019.

[7] Dag Arne Osvik, Adi Shamir, and Eran Tromer. Cache attacks and countermeasures: the case of aes. In Cryptographers’ track at the RSA conference, pages 1–20. Springer, 2006.

[8] Avinash Sodani. Knights landing (knl): 2nd generation intel® xeon phi processor. In 2015 IEEE Hot Chips 27 Symposium (HCS), pages 1–24. IEEE, 2015.

[9] Simon Winwood, Yefim Shuf, and Hubertus Franke. Multiple page size support in the linux kernel. In Proceedings of the Ottawa Linux Symposium, pages 573–593, 2002.